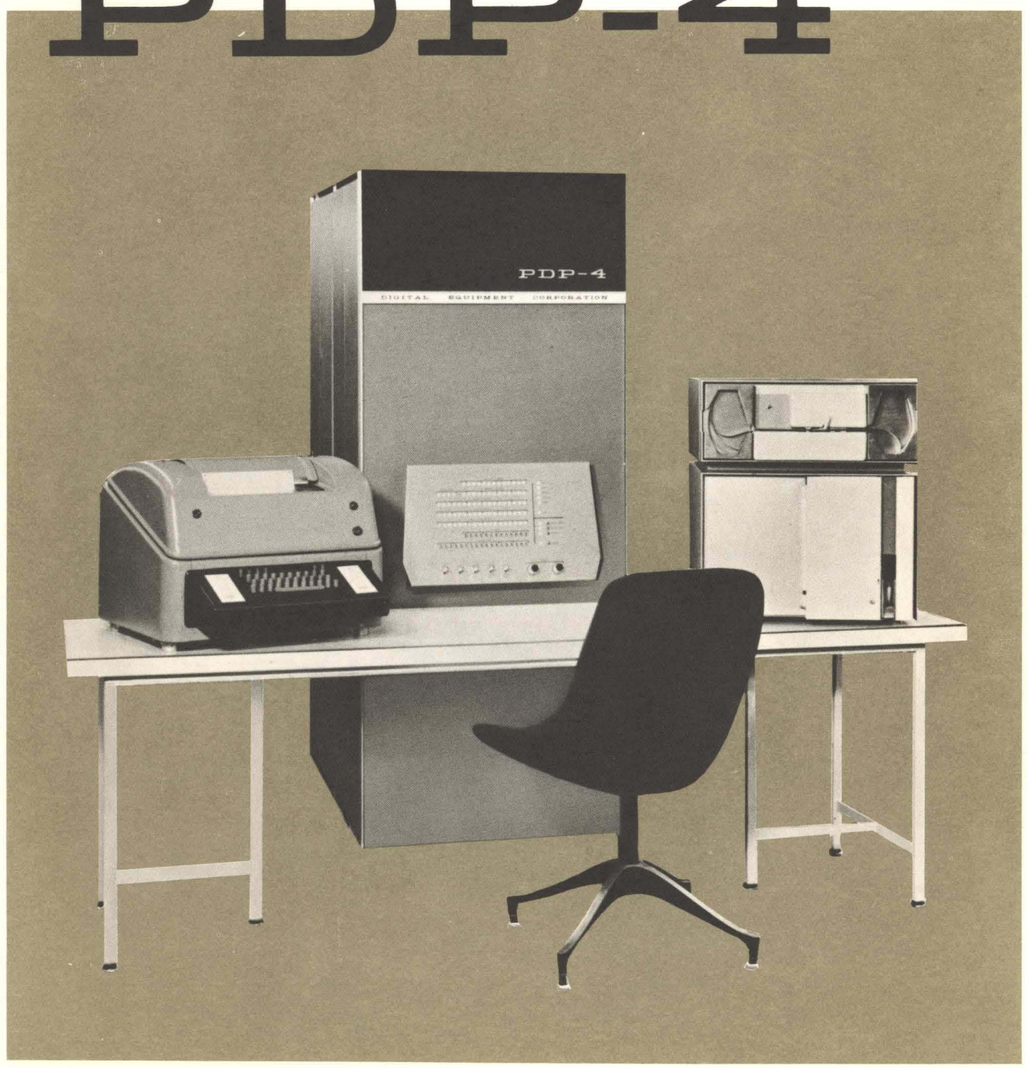
digital

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS
Los Angeles San Francisco Washington Parsippany, N.J. Ottawa Munich

10 M-9/63 PRINTED IN U.S.A. F-41D

PDP-4



DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

Programmed Data Processor-4 has been developed to meet the requirements of the engineering and scientific profession. Special emphasis has been placed on a powerful input-output interface in the computer. Extensive applications in the system control and data reduction fields are well within PDP-4's capability.

Programmed Data Processor — 4 (PDP-4) is a general purpose, high speed, solid state computer designed to be the control element in an information processing system or a complete scientific computer. It is a single address, parallel, binary machine with an 18-bit word length using 1's or 2's complement arithmetic. A random access magnetic core memory with a complete cycle time of 8 microseconds is used to achieve a computation rate of 62,500 additions per second. Other features include:

FORTRAN II COMPILER Including symbolic assembly with debugging and floating point arithmetic packages.

REAL TIME CONTROL Provides buffering and control for multiple input-output connections, program and data interrupt facilities, and a real time clock.

MULTIPLE AUTO-INDEXING Eight Auto-Indexing Memory locations simplify programming and increase the speed of table look-up and other routines.

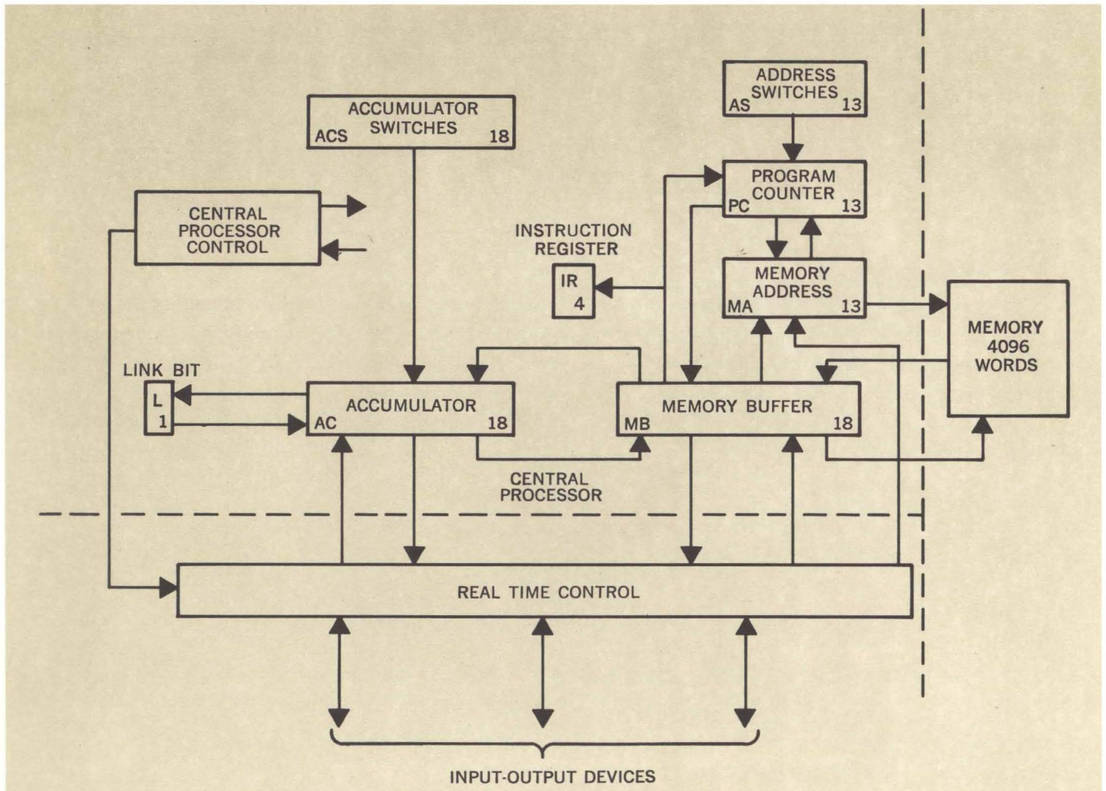
HIGH SPEED OPERATION Basic instructions require only 8 or 16 microseconds to be completely executed.

LINK BIT Provides facilities which simplify and speed up multiple precision operations.

STANDARD IN-OUT OPTIONS Magnetic Drums, Display Scopes, Magnetic Tape, Line Printers, Punched Cards, Punched Tape, and Analog Converters.

ECONOMICAL MEMORY EXPANSION Provision is made for memory expansion up to 32K.

EXTENDED ARITHMETIC UNIT (OPTIONAL) Adds 23 instructions to a standard PDP-4 including Multiply, Divide, Normalize and Long-Shift.



PDP-4 SYSTEM DIAGRAM

STANDARD PDP-4

The PDP-4 includes all essential elements for optimum performance as a systems component. The standard machine consists of:

A CENTRAL PROCESSOR — which performs arithmetic operations, controls the memory, and handles information entering and leaving the machine;

AN OPERATOR CONSOLE — which contains all controls needed to observe and modify the status of the Central Processor;

A 4096-WORD MEMORY — which provides storage for information being collected or distributed and instructions for the Central Processor;

A REAL TIME CONTROL — which provides the computer with an additional capability to operate a large variety of input-output devices with different information handling rates.

A PAPER TAPE READER — which permits information and instructions to be read from 5, 7 or 8-hole perforated paper tape into the Central Processor at the rate of 300 lines per second.

Various options which extend the usefulness of the PDP-4 are described on Pages 7, 8 and 9.

CENTRAL PROCESSOR OPTIONS

FIRST EXTRA 4096-WORD CORE MEMORY MODULE—TYPE 134

The Type 134 extends the memory capacity of the PDP-4 from 4096 to 8192 words. Additional modules require the use of a memory extension control (see below).

CORE MEMORY MODULE—TYPE 135

The Type 135 extends the memory capacity of the PDP-4 by 8192 words.

CORE MEMORY EXTENSION CONTROL—TYPE 16

The Type 16 extends the memory control capability of the PDP-4 from 8192 to 32,768 words.

BLOCK TRANSFER DRUM SYSTEM—TYPE 24

The drum system operates on a serial transfer basis in 256-word blocks. It is available in three capacities: 16, 32, 65 thousand words.

EXTENDED ARITHMETIC ELEMENT—TYPE 18

The Extended Arithmetic Element (EAE) adds 23 micro coded instructions to PDP-4 which facilitate high speed multiplication, division, and shifting. The EAE contains an 18-bit register, the Multiplier Quotient (MQ); a 6-bit register, the Step Counter (SC); and a 3-bit Instruction Register.

REAL TIME CONTROL

The Real Time Control of the PDP-4 provides the following functions:

DEVICE SELECTION — consists of decoding elements to select and control external devices by various combinations of input-output transfer instructions. Pulses may be used to: (a) control external devices; (b) read out information from PDP-4 through the Information Distributor; (c) read in information to PDP-4 through the Information Collector, and (d) test the status of external devices.

INFORMATION COLLECTION — information is received from input devices (selected by the Device Selector) and is transferred to the Central Processor. Information is read in parallel (up to 18 bits) from multiple inputs.

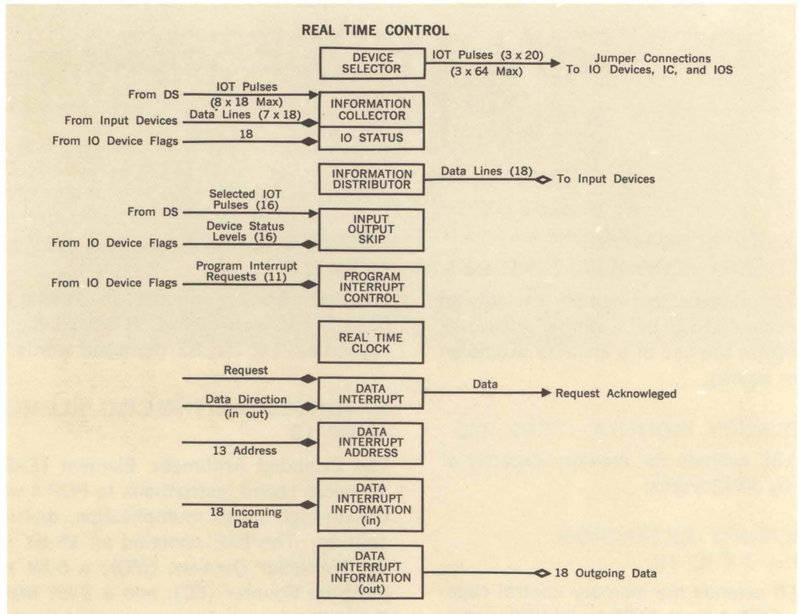
INFORMATION DISTRIBUTION — permits distribution of information from the Central Processor to all output devices. Only the output device selected (or addressed) by the Device Selector samples and reads the information contained in the Information Distributor.

IN-OUT SKIP FACILITY — provides program skip instructions conditioned by the state of input-output device logic lines. The instruction following a skip instruction will not be executed if the line is active.

PROGRAM INTERRUPT — permits conditions from input-output devices to interrupt the program and initiate a subroutine which may return to the original program when the cause for interruption has been processed. The machine state is preserved during a Program Interrupt. This type of interrupt is suited for information or event rates in the range of 1 to 2,000 cycles per second.

DATA INTERRUPT — allows a device to interrupt the program and deposit or extract data from the Core Memory at an address specified by the device. The Data Interrupt is suited for high speed information transfers. Up to 125,000 18-bit words may be transferred per second.

REAL TIME CLOCK — produces a signal which increments a Core Memory register at a rate of 60 cycles per second. When the register overflows, a Program Interrupt occurs.



INPUT-OUTPUT OPTIONS

Cathode Ray Tube Displays

PRECISION CRT DISPLAY—TYPE 30D

Displays data on a 16-inch cathode ray tube. Information is plotted point by point to form either graphical or tabular data. Separately variable 10-bit X and Y coordinates and programmable intensity control.

LIGHT PEN—TYPE 32

A photoelectric device with which the operator can sense displayed data and input modifying signals to the computer. The computer can then change its operation according to previously programmed instructions.

DIGITAL SYMBOL GENERATOR—TYPE 33

Automatically translates digital computer words into format information for display. Plots symbols on a 35-dot matrix in one of four sizes on the Type 30 CRT Display. Average plotting rate: 140 microseconds per symbol.

OSCILLOSCOPE DISPLAY—TYPE 34

Plots data point by point on a Textronix oscilloscope. Ten bits per axis. (Oscilloscope not included.)

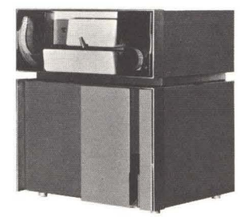
Paper Tape and Card Equipment

CARD READER AND CONTROL—TYPE 41

Operates at a rate of up to 200 cards per minute. Cards are read column by column. Column information may be read in alphanumeric or binary mode. The alphanumeric mode converts the 12-bit Hollerith Code of one column into the 6-bit binary-coded decimal code with code validity checking. The binary mode reads a 12-bit column directly into the PDP-4. Approximately one per cent of a Card Reader program running time is required to read the 80 columns of information at the 200 cards per minute rate.

CARD PUNCH CONTROL—TYPE 40

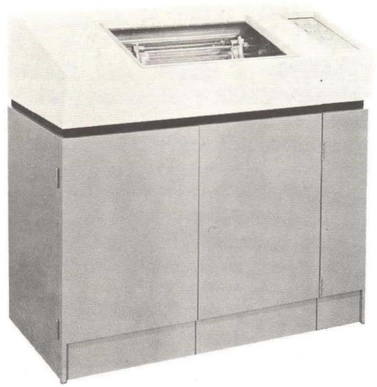
Enables the operation of a standard IBM Type 523 Summary Punch with PDP-4. Cards are punched row by row at a rate of 100 cards per minute. Approximately 0.3 per cent of program running time is required to operate the Card Punch at the 100-card-per-minute rate. Buffer holds one 80-bit row.



PERFORATED TAPE PUNCH AND CONTROL—TYPE 75

The Type 75 is a Teletype BRPE Punch with an operating speed of 63.3 lines or characters per second. It punches 5, 7 or 8-hole tape. (Shown with Standard Perforated Tape Reader.)

Printers



AUTOMATIC LINE PRINTER AND CONTROL—TYPE 64

Prints 300 lines per minute, 120 columns per line, 64 characters per column.

PRINTER-KEYBOARD AND CONTROL—TYPE 65

The Type 65 is a Teletype Model KSR-28 Printer and Keyboard with an input and printing speed of 10 characters per second.

Magnetic Tape Equipment

AUTOMATIC MAGNETIC TAPE CONTROL—TYPE 57A

Controls a maximum of eight tape transports automatically. Provides information transfer through computer's data interrupt facility. Controls reading or writing of tape at various rates compatible with IBM, BCD or binary parity modes.

The Type 57A can be used in conjunction with one of the following interfaces.

- Tape Control Interface Type 520 — permits attachment of the Type 50 Tape Transport.
- Tape Control Interface Type 521 — permits attachment of the Type 570 Tape Transport.
- Tape Control Interface Type 522 — permits attachment for one of the following type transports: IBM series 729 model II, IV, V, VI or IBM series 7330. Character transfer capabilities of 7.2 to 90 KC at densities of 200, 556, and 800.

MAGNETIC TAPE CONTROL—TYPE 54

Controls up to four Magnetic Tape Transport Units, Type 50. Information is read from or written on the tape under program control. Subroutines are available to read and write IBM compatible tapes having a density of 200, 6 + 1 bit characters per inch.

MAGNETIC TAPE TRANSPORT—TYPE 570

Reads and writes IBM formats on ½ inch tape at transfer rates from 15 to 62.5 KC. Tape speed is 75 or 112.5 ips with densities of 200 or 556 bits per inch. The transport has optional capability for multiplexed time shared operation.

MAGNETIC TAPE TRANSPORT—TYPE 50

Used with Type 54 and Type 57A controls. Transfers from 1 to 15,000 characters per second on ½ inch tape at a speed of 75 inches per second. The number of characters per inch is variable from 1 to 200; the number of bits per character is 7.

MICRO TAPE DUAL TAPE TRANSPORT AND CONTROL—TYPE 555-550

Fixed address magnetic tape for high speed loading and readout as well as program updating. Two logically independent tape drives handle 260 foot pocket-size reels of ¾ inch Mylar tape at a speed of 80 inches per second. Information is written on non-adjacent, redundant tracks in the Phase Recording System at densities of 375 bits per track inch and may be transferred at a rate of 90,000 bits per second. Tape handling and utility transfer routines available.

In-Out Connections and Controls

18-BIT OUTPUT RELAY BUFFER—TYPE 140

Provides contacts which operate devices of higher power rating. The relays have form "D" contacts, which open and close in approximately 3 milliseconds.

INTERFACE FOR IBM 7090 CONNECTION—TYPE 150

Provides communication between PDP-4 and IBM 7090 at a 10,000 cps, 18-bit word rate.

DATA CONTROL—TYPE 131

Controls and double buffers high speed transfer between the computer and external devices at word rates to 125 KC.

CLOCK MULTIPLEXER—TYPE 132

Provides 16 inputs to the PDP-4 enabling 16 memory registers to be used as 18-bit counter. Priority addressing system permits combined input counting rate to 125,000 cps.

DATA INTERRUPT MULTIPLEXER—TYPE 133

Provides high-speed transfer between PDP-4 Core Memory and three input-output devices. Maximum combined transfer rate: 125,000 cps, 18-bit words.

Analog-to-Digital Equipment

GENERAL PURPOSE ANALOG TO DIGITAL CONVERTER—TYPE 138

A general purpose analog to digital converter used to convert input analog voltages into digital numbers for computer entry.

GENERAL PURPOSE 64 CHANNEL MULTIPLEXER CONTROL—TYPE 139

Controls up to 64 channels of analog input to be multiplexed into the analog to digital converter.

HIGH SPEED ANALOG TO DIGITAL CONVERTER—TYPE 142

Converts analog signals to digital information with 10-bit accuracies in 8 microseconds for computer entry.

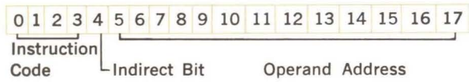
HIGH SPEED MULTIPLEXER CONTROL TYPE 141

High speed multiplexer for use with the Type 142 Analog to Digital Converter.

Special purpose analog to digital converters, multiplexers, multiplex switches, digital to analog converters, plotters and loggers with various speeds, accuracies, and input ranges are available for special requirements.

PROGRAMMING

The PDP-4 instruction format includes 4 bits for instruction code, 1 bit for indirect modified addressing and 13 bits for memory address or variations of the basic instructions.



When the indirect bit is a ONE, indirect addressing (or deferring) is specified. A defer memory cycle is required during which time the contents of the memory cell addressed are selected and the address part of this cell is used as the effective address of the original instruction. The instruction part of the cell and the indirect bit are ignored when obtaining the effective address. In addition, if the cell indirectly addressed is 10_8-17_8, a ONE is added to the contents of that cell before the address part is used as the effective address (auto-indexing).

Operating times of PDP-4 instructions are in multiples of the 8 microsecond memory cycle. Add, deposit, and load for example, are two-cycle instructions completed in 16 microseconds. Input-output connections are programmed by specifying iot instructions which affect the state of selected devices. The instructions may be microprogrammed to allow one basic instruction to handle one or more devices by changing the bits of the command.

MEMORY REFERENCE INSTRUCTIONS

Addressable or memory reference instructions which contain a memory address. The address portion of the instruction word specifies the location of an operand in the memory.

Mnemonic Code	Octal Code	Time (μsec)	Operation
cal	00	16	Same as jms 20. The address portion of this instruction is ignored. The cal instruction may be used for calling subroutines via a master central program which keeps track of exit addresses, allocates storage, and supplies parameters to the subroutines.
dac Y	04	16	Deposit Accumulator. C(AC)* are deposited in memory register Y. The C(AC) are unaffected by this operation.
jms Y	10	16	Jump to Subroutine. C(PC) are deposited in memory register Y. The next instruction will be taken from Y + 1, the beginning of the subroutine.
dzm Y	14	16	Deposit zero in memory. The contents of register Y are changed to zero. The original contents of Y are lost.
lac Y	20	16	Load AC. The C(Y) replace the C(AC). The previous C(AC) are lost. The C(Y) are unaffected.
xor Y	24	16	Exclusive OR. The exclusive "OR" logical function is performed on a bit-by-bit basis between the C(AC) and C(Y). The result is left in the AC and the original C(AC) are lost.
add Y	30	16	Add (ONE's Complement). The C(Y) are added to the C(AC) in ONE's complement arithmetic. The result is left in the AC and the original C(AC) is lost. This type add instruction is commonly used for most arithmetic. The Link bit is set to a ONE if the sum of the magnitude of C(Y) and C(AC) is greater than $2^{17} - 1$.
tad Y	34	16	Add (TWO's Complement). The C(Y) are added to C(AC) in TWO's complement arithmetic. If there is a carry out of bit 0, the Link will be set to ONE. This type of add instruction is useful in multiple precision arithmetic.

* C(AC): contents of the accumulator.

PDP-4 Instructions

Mnemonic Code	Octal Code	Time (μsec)	Operation
xct Y	40	8+ instruction execute time	The instruction in register Y will be executed. The computer will act as if the instruction located in Y were in the place of the xct Y.
isz Y	44	16	Index and Skip if zero. The C(Y) are replaced by C(Y) + 1. The C(AC) are unaffected by this instruction. The addition is done using two's complement arithmetic. If the sum is +0, the next instruction is skipped.
and Y	50	16	Logical AND. The logical "AND" function is performed on a bit-by-bit basis between C(AC) and C(Y). The result is left in the AC and the original C(AC) are lost.
sad Y	54	16	C(Y) are compared with the C(AC). If the two numbers are different, the next instruction in the sequence is skipped. The C(AC) and C(Y) are both unaffected by the instruction.
jmp y	60	8	Jump. The C(PC) are reset to address Y. The next instruction to be executed is taken from memory register Y. The original contents of the PC are lost.

AUGMENTED INSTRUCTIONS

Augmented instructions provide micro programming capability by using the address portion of the instruction to select logical operations. These instructions do not address a memory register.

The following instruction loads itself into the AC.

law	76	8	The address postion of this instruction may be used to specify a constant.

OPERATE GROUP

The operate instructions use bits 5 through 17 to specify variations of the basic instructions.

opr	74xxxx	8	Operate. The operate instruction is also the conditioning (skip) instruction. When a particular condition is present, the following instruction will be skipped. The various micro program events occur at different times to allow several events to be programmed which affect the same element. This is a micro program instruction using bits 4-17 to specify the desired operations. Combinations of the individual operations can be made. The operations are specified by bits as follows

Mnemonic Code	Octal Code	Operation	Sequence of Occurrence
cma	1	Complement AC.	3
cml	2	Complement Link.	3
oas	4	Inclusive OR AC switches with AC.	3
ral	10	Rotate AC and Link left one place.	3
rtl	2010	Rotate AC and Link two places left.	2, 3
rar	20	Rotate AC and Link right one place.	3
rtr	2020	Rotate AC and Link two places right.	2, 3
hlt	40	Halt the machine	4
sma	100	Skip on minus AC. If $AC_0 = 1$, the next instruction in sequence is skipped.	1
spa	1100	Skip on plus AC. If $AC_0 = 0$, the next instruction in sequence is skipped.	1
sza	200	Skip if AC = 0.	1
sna	1200	Skip if AC ≠ 0.	1
snl	400	Skip if Link ≠ 0.	1
szl	1400	Skip if Link = 0.	1
skp	1000	Skip unconditionally.	1
cll	4000	Clear Link.	2
cla	10000	Clear AC.	2

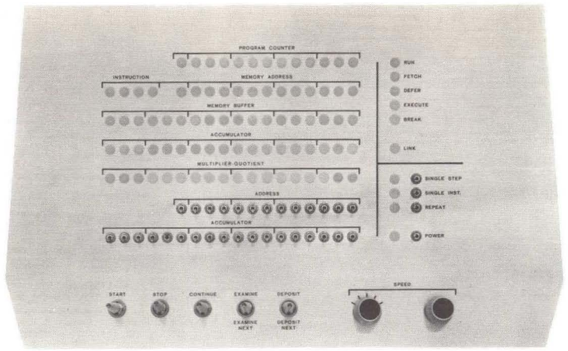
IN-OUT TRANSFER GROUP

The instructions in this group are similar to the Operate Group instructions except they pertain to the transfer of information between the Central Processor and various input-output devices. Bits 4 through 17 select and control input-output devices.

Mnemonic Code	Octal Code	Time (μsec)	Operation
iot	70xxxx	8	In Out Transfer. This instruction which forms a micro program is used to select an input or output device. The instruction forms a micro program and has the following format:

Function	Command Bits
Specifies the in-out instruction (Operation Code 1110)	0-3
May be used to select sub-device	4-5
Selects the device	6-11
May be used to select sub-device	12-13
Clears the AC at event time 1 if a ONE	14
Transfers an IOT pulse at event time 3 if a ONE	15
Transfers an IOT pulse at event time 2 if a ONE	16
Transfers an IOT pulse at event time 1 if a ONE	17

Bits 13-17 may be used together in any combination to allow various types of in-out command structures, and these may handle 1, 2, or 3 devices per selection (bits 4-12) depending upon the requirements of the devices.



Keys and toggle switches available on the PDP-4 control panel provide maximum ease of operation. Their functions are as follows:

Console Keys

START

Starts the processor. The first instruction is taken from memory cell specified by the setting of the ADDRESS switches. The START operation clears the AC and Link, and turns off the Program Interrupt.

STOP

Causes the processor to halt functional operations at the completion of the memory cycle in progress at the time of key operation.

CONTINUE

Causes the processor to resume operation beginning at the address specified by the Program Counter (PC).

EXAMINE

Sets the contents of the memory location indicated by the Address Switches into the Accumulator (AC) and Memory Buffer.
The Memory Address Register will contain the address of the memory location being examined and the program counter will contain the address of the next location.

DEPOSIT

Sets the word selected by the Accumulator Switches (ACS) into the memory at the location specified by the Address Switches. The results will remain in the Accumulator and the Memory Buffer. The Memory Address Register will contain the address of the memory location holding the information, and the Program Counter will contain the address of the next location.

EXAMINE NEXT

Sets the contents of the memory at the address specified by the Program Counter into the Accumulator and the Memory Buffer. The C(PC) are indexed by one, and the Memory Address Register will contain the address of the location examined.

DEPOSIT NEXT

Sets the contents of the Accumulator Switches into the memory at the location specified by the Program Counter. The C(PC) will be indexed by one, and the Memory Address Register will contain the address of the location holding the information.

Console Toggle Switches

POWER

Turns on the power.

SINGLE STEP

Causes the processor to halt at the completion of each memory cycle. This switch is particularly useful in maintenance tasks. Repeated operation of the Continue Key will step the program one cycle at a time so that the state of the machine can be examined at each step.

SINGLE INSTRUCTION

Causes the processor to stop at the completion of each instruction.

REPEAT

Causes operations initiated by console keys to be repeated as long as the keys are depressed. The operations are performed at the rate set by the Speed Switch.

SPEED

Controls the speed of the repeat function.

PROGRAMMING AIDS

The PDP-4 Programming System includes FORTRAN II, a Symbolic Assembly and Debugging System, maintenance routines, and numerous other programming aids.

FORTRAN II

PDP-4 FORTRAN II allows the programmer an unusual degree of freedom in many instances: For example, mixed expressions and n-dimensional arrays are allowed. An important feature is the retention of the original symbols from the FORTRAN source language tape through the final binary program, making the system easy to use and reducing debugging time. Compilation of the original FORTRAN source program is performed alone, with subprograms compiled and assembled separately. Hence, should mistakes occur in FORTRAN coding, only the main program need be recompiled.

PDP-FORTRAN II FEATURES

FIXED POINT CONSTANTS:	1-6 decimal digits absolute value $\leqq 131{,}071$
FLOATING POINT CONSTANTS:	10 decimal digits precision. Exponent range $2^{(2^{17}-1)}$ to $-2^{(2^{17}-1)}$
VARIABLE NAMES:	1-6 alphanumeric characters
SUBSCRIPTS:	Any arithmetic expression representing an integer quantity: Variables in a subscript may themselves be subscripted to any depth. N dimensional arrays are permitted.
STATEMENTS:	Mixed expressions containing both fixed and floating point variables are permitted. A maximum of 300 characters are allowed (statement numbers not counted)
STATEMENT NUMBERS:	1-99999
FUNCTIONS AND SUBROUTINES:	Subroutines not contained in the FORTRAN library may be compiled by the use of Function and Subroutine statements. Functions and subroutines may be fixed or floating point valued as defined by initial letter of F-type function convention. Arguments may be arbitrary arithmetic expressions, including functions.
INPUT AND OUTPUT:	MICRO-TAPE, paper tape, punched cards, teletype, display. Format may be specified by use of a FORMAT statement.
STATEMENTS AVAILABLE:	Arithmetic statements, I/O statements with FORMAT, DO, Dimension, Common, IF, GOTO, Assign, Continue, Call, Subroutine, Function, Return.

Symbolic Assembly and Debugging System

ASSEMBLY PROGRAM

A one-pass assembler that allows mnemonic symbols to be used for addresses and instructions. Constant and variable storage registers are automatically assigned. This assembler will produce relocatable or absolute binary output, as desired by the user.

RELOCATING LOADER

Performs relocation and linking of binary programs that have been assembled separately.

DDT-4 (DEC DEBUGGING TAPE-4)

Debugging may be done at run time using the teleprinter. Break points may be inserted into a program at arbitrary points so that the state and operation of a program may be observed. The source program symbols may be used for communication.

EDMUND THE EDITOR

Allows the editing of symbolic tapes.

Arithmetic Routines

DOUBLE PRECISION INTEGER PACKAGE

A collection of subroutines which allow the user to perform double precision arithmetic with 35-bit signed numbers.

MULTIPLY AND DIVIDE SUBROUTINES

Single precision signed one's complement.

DOUBLE PRECISION FLOATING POINT

Performs operations upon floating point numbers, with approximately 10 decimal digits of precision, and an exponent which may be as large as $2^{(2^{17}-1)}$ in magnitude.

AUTOMATIC MULTIPLY AND DIVIDE

Provided by the Extended Arithmetic Element Type 18, also includes shift and normalize functions permitting fast floating point operations.

STANDARD FUNCTION GENERATORS

Routines to calculate floating point, arctan (x), sin (x), cos (x), e^x, log (x), x^y, $\sqrt{x}$.

I/O Programs

MAGNETIC TAPE PACKAGE

Facilitates use of Type 57A and Type 54 Control units.

MICRO TAPE PACKAGE

For use with Micro Tape 555.

SYMBOL GENERATOR ROUTINES

A high speed plotting routine for use with the Type 33 Symbol Generator.

PEN FOLLOW

Tracks the light pen across the face of the Type 30 Precision CRT Display.

BUFFERED I/O PACKAGE

Permits simultaneous use of the paper tape reader, paper tape punch, card reader, card punch, high speed line printer, teleprinter and keyboard, buffering all input and output.

Utility Routines

CAL HANDLER

Facilitates the calling of subroutines. Permits greater freedom in the use of subroutines, including recursive calls.

MASTER TAPE DUPLICATOR

Verifies and duplicates tapes.

PUNCH ROUTINES

Allow punching in either block format binary or read-in mode format.

Maintenance Routines

Many of these maintenance routines are also used on DEC's standard acceptance tests. Special I/O test programs are available as required.

CONTEST

(Continuous Test) Repeatedly tests all basic machine functions.

MAINDEC 401 INSTRUCTION TEST

A sequence of programs which test the operation of all PDP-4 instructions except the iot group.

MAINDEC 402 CHECKERBOARD

Provides continuous memory testing with four different patterns.

MAINDEC 403 ADDRESS SET

Maintenance programs to check the memory module for proper address selection.

READER AND PUNCH TEST

Checks the operation of the reader and punch using different patterns and variable times.

TELEPRINTER TEST

Tests the input and output facilities of the teleprinter by repeating the typed message, echo checking, etc.