

**PDP-10**  
KA10 CENTRAL PROCESSOR  
MAINTENANCE MANUAL  
VOLUME 2

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CONTENTS

Page

CHAPTER 1  
ENGINEERING DRAWINGS

1.1	Drawing Codes	1
1.2	Drawing Number Index	1
1.3	Content Index	1
1.4	Signal Glossary	1

TABLES

1-1	Drawing Number Index	2
1-2	Alphabetical Index	4
1-3	KA10 Signal Glossary	7

## CHAPTER 1 ENGINEERING DRAWINGS

This manual contains a set of engineering drawings and a signal glossary for the KA10 Central Processor. A complete set of drawings, including those for the peripheral equipment, is supplied with each PDP-10 System. If a discrepancy should exist between the drawings in this manual and those supplied with the system, it is safe to assume that those supplied with the system are the latest versions.

### 1.1 DRAWING CODES

Engineering drawings generated by Digital Equipment Corporation are coded as to drawing type, major assembly, and series. A drawing number such as D-BS-KA10-0-MC1 contains the following information:

D	"D" size (22 x 34 inches)
BS	Block Schematic (type of drawing)
KA10	The processor of the PDP-10
0	The manufacturing variation
MC1	The first drawing in the Memory Control series.

A list of drawing type codes follows:

AD	Assembly Drawing
AR	Arrangement Drawing
BD	Functional Block Diagram
BS	Block Schematic
CD	Cable Diagram
CL	Cable List
CP	Component List
CS	Circuit Schematic
DI	Drawing Index List
FD	Flow Diagram
IC	Interface Cabling Diagram
ML	Master Drawing List
MU	Module Utilization Drawing
PL	Parts List
RS	Replacement Schematic
SP	Specification Drawing
TD	Timing Diagram

UA	Unit Assembly
WD	Wiring Diagram
WL	Wiring List

### 1.2 DRAWING NUMBER INDEX

Table 1-1 is the index of engineering drawings arranged by class and by drawing number in alphanumeric order.

### 1.3 CONTENT INDEX

Table 1-2 is the index of engineering drawings by subject. Alphanumeric order is used. Note that for this index, terms such as "AR" or "IR" are treated as if spelled out as "Arithmetic Register" or "Instruction Register."

### 1.4 SIGNAL GLOSSARY

Table 1-3 is a signal glossary in alphanumeric order by signal name and gives source drawing code and a brief description of what the signal is or does. Note that the drawing code is actually only the last three or four characters of the full drawing number.

Input/output devices have not been included in this glossary nor have register transfer pulses. It is sufficient to define the register transfer pulses general form as follows:

XX FM YY (Z)

Where XX is the receiving register, in whose control circuits the pulse originates; "FM" in this context means "from"; YY is the sending register, unaffected by the transfer; and Z describes the flip-flop inputs affected. "Z" may be 1, 0, or J. When Z is a "1", the 1 outputs of the sending register affect the set inputs of the receiving register; when Z is "0", the 0 outputs of the sending register affect the clear input of the receiving register. When Z is a "J" (Jam transfer), a combined 0's and 1's transfer is effected.

Summary description of register transfers:

Example	Result
BR FM AR (0)	Logically AND the AR contents with BR contents with result in BR
AR FM AD (1)	Logically IOT the AD outputs with AR contents with result in AR
PC FM MA (J)	Replace the contents of PC with a copy of contents of MA



Table 1-1  
Drawing Number Index

Drawing Number	Title	Size (original drawing) and Type	Page
Drawing Lists and Indexes			
KA10-A-0	KA10 Processor 60 Hz 115V	A-ML	19
KA10-0-3	Drawing Index List KA10	D-D1	23
Block and Flow Diagrams			
KA10-0-BIF1	Basic Instruction Flow	D-FD	27
KA10-0-BIF2	Basic Instruction Flow	D-FD	28
KA10-0-BIF3	Basic Instruction Flow	D-FD	29
KA10-0-BIOR	Basic I-O Registers	D-FD	30
KA10-0-BYTF	Byte Instruction Flow	D-FD	31
KA10-0-DIVF	Fixed Point Divide & Divide Subroutine	D-FD	32
KA10-0-ESC	Execute and Store Cycles	D-FD	33
KA10-0-FAF	Floating Add, Sub & UFA Flow	D-FD	34
KA10-0-FC	Fetch Cycle Flow	D-FD	35
KA10-0-FDVF	Floating Divide	D-FD	36
KA10-0-FPMC	FP EXP Calculate SUBR FM & MPY SUBR	D-FD	37
KA10-0-FSDN	Floating Scale & Double Floating Negate	D-FD	38
KA10-0-IAC	Instruction and Address Cycles	D-FD	39
KA10-0-IOTF	In-Out Transfer Control Flow	D-FD	40
KA10-0-KO	Key Operations Flow Diagram	D-FD	41
KA10-0-MCFM	Memory Control & Fast Memory Flow	D-FD	42
KA10-0-NRF	Normalize Return Subroutine	D-FD	43
KA10-0-PIF	Priority Interrupt Isolated Flow	D-FD	44
KA10-0-REG	KA10 Register Interconnections	D-FD	45
KA10-0-RIMF	Read-in Function Isolated Flow	D-FD	46
KA10-0-SCAF	Shift Count Action Flow	D-FD	47
KA10-0-SCBT	Shift Count Subroutine & BLT Flow	D-FD	48
KA10-0-SMF	Shift & MUL & JFFO Flow	D-FD	49

Table 1-1 (Cont)  
Drawing Number Index

Drawing Number	Title	Size (original drawing) and Type	Page
Block Schematics			
KA10-0-AD1	Adder Control Flip-Flops Levels	D-BS	50
KA10-0-AD2	Adder Control Levels	D-BS	51
KA10-0-AD3	Adder Left Half	D-BS	52
KA10-0-AD4	Adder Right Half	D-BS	53
KA10-0-AR1	AR Register	D-BS	54
KA10-0-AR2	AR Register	D-BS	55
KA10-0-AR3	AR Register	D-BS	56
KA10-0-AR4	AR Register	D-BS	57
KA10-0-ARC1	AR Control Pulses	D-BS	58
KA10-0-ARC2	AR Control Pulses	D-BS	59
KA10-0-ARC3	AR Control Levels	D-BS	60
KA10-0-ARF	Arithmetic Flags	D-BS	61
KA10-0-ARI	AR Inputs	D-BS	62
KA10-0-ARMQ	AR & MQ Shift Connections	D-BS	63
KA10-0-AS	Address Switch Comparators	D-BS	64
KA10-0-BR1	BR Control	D-BS	65
KA10-0-BR2	BR Register	D-BS	66
KA10-0-BTMP	Block Transfer and Multiply	D-BS	67
KA10-0-BYTE	Byte Instruction (First Part)	D-BS	68
KA10-0-CPA	Arithmetic Process Status Register	D-BS	69
KA10-0-DBLB	Byte Instruction Deposit and Load (Second Part)	D-BS	70
KA10-0-DSDV	Divide Subroutine & Fixed Divide	D-BS	71
KA10-0-E	Execution Cycle	D-BS	72
KA10-0-EX	Executive Control	D-BS	73
KA10-0-F1	Fetch Cycle Time Pulses	D-BS	74
KA10-0-F2	Fetch Cycle Levels	D-BS	75
KA10-0-FA	Floating Add Instruction	D-BS	76
KA10-0-FDV	Floating Divide	D-BS	77
KA10-0-FE	Floating Exponent Reg & Control	D-BS	78
KA10-0-FM	Fast Memory	D-BS	79

Table 1-1 (Cont)  
Drawing Number Index

Drawing Number	Title	Size (original drawing) and Type	Page
KA10-0-FMA	Fast Memory Address	D-BS	80
KA10-0-FPFM	EXP CALC Floating Multiply	D-BS	81
KA10-0-HWT	Half Word Transfer	D-BS	82
KA10-0-IA	Instruction & Address Cycles	D-BS	83
KA10-0-IOB1	I/O Bus 0-17	D-BS	84
KA10-0-IOB2	I/O Bus 18-35	D-BS	85
KA10-0-IOBC	I/O Bus Control and I/O Selection	D-FD*	86
KA10-0-IOBI	IOB Inputs	D-BS	87
KA10-0-IOT	In-Out Transfer Control	D-BS	88
KA10-0-IR	Instruction Register	D-FD*	89
KA10-0-IR1	IR Decoding	D-BS	90
KA10-0-IR2	IR Decoding	D-BS	91
KA10-0-IR3	IR Decoding	D-BS	92
KA10-0-JFFO	JFFO Instruction Control	D-BS	93
KA10-0-KEY1	Key and Switches Controls	D-BS	94
KA10-0-KEY2	Keys & Switches Controls	D-BS	95
KA10-0-KEY3	Keys & Switches Controls	D-BS	96
KA10-0-MA1	MA Control	D-BS	97
KA10-0-MA2	MA Register	D-BS	98
KA10-0-MAI	Memory Address Interface	D-BS	99
KA10-0-MBDI	Memory Bus Data Interface	D-BS	100
KA10-0-MC1	Memory Control	D-BS	101
KA10-0-MC2	Memory Control	D-BS	102
KA10-0-MI	Memory Indicator	D-BS	103
KA10-0-MQ1	MQ Control	D-BS	104
KA10-0-MQ2	Multiplier Quotient (MQ 00-17)	D-BS	105
KA10-0-MQ3	Multiplier Quotient (MQ 18-35)	D-BS	106
KA10-0-MR	Master Clear and Power Clear	D-BS	107
KA10-0-NRNL	Normalize Return & NR Long	D-BS	108

\*Type shown on drawing is in error.

Table 1-1 (Cont)  
Drawing Number Index

Drawing Number	Title	Size (original drawing) and Type	Page
KA10-0-PB	Parity Buffer Register	D-BS	109
KA10-0-PC1	Program Counter Control	D-BS	110
KA10-0-PC2	Program Counter Register	D-BS	111
KA10-0-PI1	PI Control	D-BS	112
KA10-0-PI2	Priority Interrupt PIH, PIR, PIO	D-BS	113
KA10-0-PN	Parity Network	D-BS	114
KA10-0-PR	Protect Register	D-BS	115
KA10-0-PTP1	Paper Tape Punch Control 1	D-BS	116
KA10-0-PTP2	Paper Tape Punch Control 2	D-BS	117
KA10-0-PTR1	Paper Tape Reader Control	D-BS	118
KA10-0-PTR2	Paper Tape Reader Control	D-BS	119
KA10-0-PTR3	Paper Tape Reader Control	D-BS	120
KA10-0-RL	Relocate Register	D-BS	121
KA10-0-S1	Store Cycle Time Pulses	D-BS	122
KA10-0-S2	Store Cycle Levels	D-BS	123
KA10-0-SC	Shift Count Register	D-BS	124
KA10-0-SCAD	Shift Count Adder	D-BS	125
KA10-0-SCC1	Shift Counter Control	D-BS	126
KA10-0-SCC2	Shift Counter Control	D-BS	127
KA10-0-SCSR	Shift & Cnt Subrtn & Shift Inst	D-BS	128
KA10-0-TTY1	Teletype Control	D-BS	129
KA10-0-TTY2	Teletype Control	D-BS	130
Module Utilization			
KA10-0-IA1D	Module Utilization PDP-10 (Panels 1A-1D)	D-MU	131
KA10-0-1E1J	Module Utilization PDP-10 (Panels 1E-1J)	D-MU	132
KA10-0-1K1N	Module Utilization PDP-10 (Panels 1K-1N)	D-MU	133
KA10-0-1P1T	Module Utilization PDP-10 (Panels 1P-1T)	D-MU	134
KA10-0-2A2D	Module Utilization PDP-10 (Panels 2A-2D)	D-MU	135
KA10-0-2E2J	Module Utilization PDP-10 (Panels 2E-2J)	D-MU	136
KA10-0-2K2N	Module Utilization PDP-10 (Panels 2K-2N)	D-MU	137

Table 1-1 (Cont)  
Drawing Number Index

Drawing Number	Title	Size (original drawing) and Type	Page
KA10-0-2P2T	Module Utilization PDP-10 (Panels 2P-2T)	D-MU	138
KA10-0-3A3D	Module Utilization PDP-10 (Panels 3A-3D)	D-MU	139
KA10-0-3E3F	Module Utilization PDP-10 (Panels 3E-3F)	D-MU	140
KA10-0-MC	Module Count	A-PL	141
Wiring and Components			
7005607-0-0	Cable Set	D-AD	144
KA10-0-1	DC Power Wiring	D-IC	145
KA10-0-2	AC Power Wiring	D-IC	149
KA10-0-CP	External Component List for KA10	A-CP	152
KA10-0-GW	General Wiring Sheet for TTY Socket Wiring of KA10	A-WL	155
KA10-0-IBC1	Inter-Bay Cables	D-CL	156
KA10-0-IBC2	Inter-Bay Cables	D-CL	157
KA10-0-ICSC1	Indicator and Console Switch Connections	D-IC	158
KA10-0-ICSC2	Indicator and Console Switch Connections	D-IC	159
KA10-0-TERM	Pulse & Level Terminations (Bay 1 & Bay 2)	D-CL	160
KA10-0-0	KA10 Assembly	D-UA	161
KA10-0-0	KA10 Assembly	A-PL	164

Table 1-2  
Alphabetical Index

Subject	Drawing Number	Type Code	Page
AC Power Wiring	KA10-0-2	D-IC	149
Adder Control Flip-Flops	KA10-0-AD1	D-BS	50
Adder Control	KA10-0-AD2	D-BS	51
Adder Left Half	KA10-0-AD3	D-BS	52
Adder Right Half	KA10-0-AD4	D-BS	53
Address Cycles	KA10-0-IAC	D-FD	39
Address Cycles	KA10-0-IA	D-BS	83
Address Switch Comparators	KA10-0-AS	D-BS	64
Arithmetic Register (AR)	KA10-0-AR1	D-BS	54
Arithmetic Register (AR)	KA10-0-AR2	D-BS	55
Arithmetic Register (AR)	KA10-0-AR3	D-BS	56
Arithmetic Register (AR)	KA10-0-AR4	D-BS	57
Arithmetic Register (AR) Control Pulses	KA10-0-ARC1	D-BS	58
Arithmetic Register (AR) Control Pulses	KA10-0-ARC2	D-BS	59
Arithmetic Register (AR) Control Levels	KA10-0-ARC3	D-BS	60
Arithmetic Flags	KA10-0-ARF	D-BS	61
AR Inputs	KA10-0-ARI	D-BS	62
Arithmetic Processor Status Register	KA10-0-CPA	D-BS	69
AR and MQ Shift Connections	KA10-0-ARMQ	D-BS	63
Basic Instruction Flow	KA10-0-BIF1	D-FD	27
Basic Instruction Flow	KA10-0-BIF2	D-FD	28
Basic Instruction Flow	KA10-0-BIF3	D-FD	29
Basic I/O Control	KA10-0-MR	D-BS	107
Basic I/O Registers	KA10-0-BIOR	D-FD	30
Block Transfer	KA10-0-BTMP	D-BS	67
Block Transfer Flow	KA10-0-SCBT	D-FD	48
BR Control	KA10-0-BR1	D-BS	65
BR Register	KA10-0-BR2	D-BS	66
Byte Deposit and Load (Second Part)	KA10-0-DBLB	D-BS	70
Byte Instruction First Part	KA10-0-BYTE	D-BS	68
Byte Instruction Flow	KA10-0-BYTF	D-FD	31
Cable Set	7005607-0-0	D-AD	144

Table 1-2 (Cont)  
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Console Switch Connections	KA10-0-ICSC1	D-IC	156
Console Switch Connections	KA10-0-ICSC2	D-IC	157
DC Power Wiring	KA10-0-1	D-IC	145
Divide Subroutine and Fixed Divide	KA10-0-DIVF	D-FD	32
Double Floating Negate	KA10-0-FSDN	D-FD	38
Drawing Index List	KA10-0-3	D-DI	23
Execute and Store Cycle	KA10-0-ESC	D-FD	33
Execution Cycle	KA10-0-E	D-BS	72
Executive Control	KA10-0-EX	D-BS	73
External Component List	KA10-0-CP	A-CP	152
Fast Memory	KA10-0-FM	D-BS	79
Fast Memory Address	KA10-0-FMA	D-BS	80
Fast Memory Flow	KA10-0-MCFM	D-FD	42
Fetch Cycle Flow	KA10-0-FC	D-FD	35
Fetch Cycle Levels	KA10-0-F2	D-BS	75
Fetch Cycle Time Pulse	KA10-0-F1	D-BS	74
Fixed Divide and Subroutine	KA10-0-DSDV	D-BS	71
Fixed Point Divide and Subroutine	KA10-0-DIVF	D-FD	32
Floating Add Instruction	KA10-0-FA	D-BS	76
Floating ADD, SUB, UFA Flow	KA10-0-FAF	D-FD	34
Floating Divide	KA10-0-FDV	D-BS	77
Floating Divide	KA10-0-FDVF	D-FD	36
Floating Exponent Calculation	KA10-0-FPFM	D-BS	81
Floating Exponent Calculation Subroutine	KA10-0-FPMC	D-FD	37
Floating Exponent Register and Control	KA10-0-FE	D-BS	78
Floating Multiply and Multiply Subroutine	KA10-0-FPMC	D-FD	37
Floating Scale and DBL Floating Negate	KA10-0-FSDN	D-FD	38
Half Word Transfer	KA10-0-HWT	D-BS	82
Indicator and Console SW Connections	KA10-0-ICSC1	D-IC	156
Indicator and Console SW Connections	KA10-0-ICSC2	D-IC	157
I/O Bus Control and I/O Selection	KA10-0-IOBC	D-BS	86
I/O Bus Inputs	KA10-0-IOBI	D-BS	87

Table 1-2 (Cont)  
Alphabetical Index

Subject	Drawing Number	Type Code	Page
I/O Bus (0-17)	KA10-0-IOB1	D-BS	84
I/O Bus (18-35)	KA10-0-IOB2	D-BS	85
In-Out Transfer Control	KA10-0-IOT	D-BS	88
In-Out Transfer Control Flow	KA10-0-IOTF	D-FD	40
Instruction and Address Cycles	KA10-0-IAC	D-FD	39
Instruction and Address Cycles	KA10-0-IA	D-BS	83
Instruction Register	KA10-0-IR	D-BS	89
Instruction Register Decoding	KA10-0-IR1	D-BS	90
Instruction Register Decoding	KA10-0-IR2	D-BS	91
Instruction Register Decoding	KA10-0-IR3	D-BS	92
Inter-Bay Cables	KA10-0-IBC1	D-CL	156
Inter-Bay Cables	KA10-0-IBC2	D-CL	157
JFFO Flow	KA10-0-SMF	D-FD	49
JFFO Instruction Control	KA10-0-JFFO	D-BS	93
KA10 Assembly	KA10-A-0	D-UA	161
KA10 Assembly Parts List	KA10-A-0	A-PL	164
KA10 Register Interconnections	KA10-0-REG	D-FD	45
Key and Switches Controls	KA10-0-KEY1	D-BS	94
Key and Switches Controls	KA10-0-KEY2	D-BS	95
Key and Switches Controls	KA10-0-KEY3	D-BS	96
Key Operations Flow Diagram	KA10-0-KO	D-FD	41
Level and Pulse Terminations Bay 1 and 2	KA10-0-TERM	D-CL	160
Master Clear and Power Clear	KA10-0-MR	D-BS	107
Memory Address Control	KA10-0-MA1	D-BS	97
Memory Address Register	KA10-0-MA2	D-BS	98
Memory Address Interface	KA10-0-MAI	D-BS	99
Memory Bus Data Interface	KA10-0-MBDI	D-BS	100
Memory Control	KA10-0-MC1	D-BS	101
Memory Control	KA10-0-MC2	D-BS	102
Memory Control and Fast Memory Flow	KA10-0-MCFM	D-FD	42
Memory Indicator	KA10-0-MI	D-BS	103
Module Utilization Panels 1A-1D	KA10-0-1A1D	D-MU	131

Table 1-2 (Cont)  
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Module Utilization Panels 1E-1J	KA10-0-1E1J	D-MU	132
Module Utilization Panels 1K-1N	KA10-0-1K1N	D-MU	133
Module Utilization Panels 1P-1T	KA10-0-1P1T	D-MU	134
Module Utilization Panels 2A-2D	KA10-0-2A2D	D-MU	135
Module Utilization Panels 2E-2J	KA10-0-2E2J	D-MU	136
Module Utilization Panels 2K-2N	KA10-0-2K2N	D-MU	137
Module Utilization Panels 2P-2T	KA10-0-2P2T	D-MU	138
Module Utilization Panels 3A-3D	KA10-0-3A3D	D-MU	139
Module Utilization Panels 3E-3F	KA10-0-3E3F	D-MU	140
Module Count	KA10-0-MC	A-PL	141
Multiplier Quotient (MQ 0-17)	KA10-0-MQ2	D-BS	105
Multiplier Quotient (MQ 18-35)	KA10-0-MQ3	D-BS	106
Multiplier Quotient	KA10-0-MQ1	D-BS	104
Multiply	KA10-0-BTMP	D-BS	67
Multiply Flow	KA10-0-SMF	D-FD	49
Normalize Return and NR Long	KA10-0-NRNL	D-BS	108
Normalize Return Subroutine	KA10-0-NRF	D-FD	43
Paper Tape Punch Control	KA10-0-PTP1	D-BS	116
Paper Tape Punch Control	KA10-0-PTP2	D-BS	117
Paper Tape Reader Control	KA10-0-PTR1	D-BS	118
Paper Tape Reader Control	KA10-0-PTR2	D-BS	119
Paper Tape Reader Control	KA10-0-PTR3	D-BS	120
Parity Buffer Register	KA10-0-PB	D-BS	109
Parity Network	KA10-0-PN	D-BS	114
PI Control	KA10-0-PI1	D-BS	112
Power Clear	KA10-0-MR	D-BS	107
Priority Interrupt Isolated Flow	KA10-0-PIF	D-FD	44
Priority Interrupt PIH, PIR, PIO	KA10-0-PI2	D-BS	113
Program Counter Control	KA10-0-PCP	D-BS	110
Program Counter Register	KA10-0-PC2	D-BS	111
Protect Register	KA10-0-PR	D-BS	115

Table 1-2 (Cont)  
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Pulse and Level Terminations Bay 1 and 2	KA10-0-TERM	D-CL	158
Readin Function Isolated Flow	KA10-0-RIMF	D-FD	46
Register Interconnections	KA10-0-REG	D-FD	45
Relocate Register	KA10-0-RL	D-BS	121
Shift Connections	KA10-0-ARMQ	D-FD	63
Shift Count Register	KA10-0-SC	D-BS	124
Shift Count Adder	KA10-0-SCAD	D-BS	125
Shift Counter Control	KA10-0-SCC1	D-BS	126
Shift Counter Control	KA10-0-SCC2	D-BS	127
Shift and Count Subroutine and Shift Instruction	KA10-0-SCSR	D-BS	128
Shift Count Subroutine and BLT Flow	KA10-0-SCBT	D-FD	48
Shift Count Action Flow	KA10-0-SCAF	D-FD	47
Shift and MUL and JFFO Flow	KA10-0-SMF	D-FD	49
Store Cycle	KA10-0-ESC	D-FD	33
Store Cycle Time Pulse	KA10-0-S1	D-BS	122
Store Cycle Levels	KA10-0-S2	D-BS	123
Switch Controls	KA10-0-KEY1	D-BS	94
Switch Controls	KA10-0-KEY2	D-BS	95
Switch Controls	KA10-0-KEY3	D-BS	96
Teletype Control	KA10-0-TTY1	D-BS	129
Teletype Control	KA10-0-TTY2	D-BS	130
TTY Socket Wiring	KA10-0-GW	A-WL	155

Table 1-3  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
AD0-35	AD3	Adder. Performs arithmetic and logical operations using AR and BR register contents as inputs.
AD0-7=0	AD2	Level. True when bits AD0 through 7 contain all zeroes.
AD 1 AR INP	AD3	Level. Used to generate AD CRY1 on AD2.
AD 1 BR INP	AD3	Level. Used to generate AD CRY1 on AD2.
AD9-35=0	AD2	Level. True when bits AD9 through 35 all contain zeroes.
AD10-35=0	AD2	Level. True when bits AD10 through 35 all contain zeroes.
AD AR NEGATE (FT9)	AD2	Level. Setup for two's complement of AR contents. Produces AD AR-EN (FT9) and AD CRY 36 (FT9).
AD AR+ EN	AD1	When set, gates ARn (1) to ADn.
AD AR+ EN (FT9)	AD2	Level. Prevents FT9 from clearing AD AR+ EN.
AD AR- EN	AD1	When set, gates ARn (0) to ADn.
AD AR- EN (FT9)	AD2	Level. Allows FT9 pulse to set AD AR- EN.
AD BR± (FT9)	AD2	Level. Produces AD BR+ EN (FT9) and AD BR- EN (FT9). Used to form arithmetic -1 at AD inputs.
AD BR+ EN	AD1	When set, gates BRn (1) to ADn.
AD BR+ ONLY EN (ET0)	AD2	Level. Enables ET0 pulse to clear AD AR+ EN, AD AR- EN, AD CRY 36, and to set AD BR+ EN.
AD BR- EN	AD1	When set, gates BRn (0) to ADn.
AD BR- EN (FT9)	AD2	Level. Enables FT9 pulse to set AD BR- EN.
AD COND	AD2	Level. Provides sign/overflow compensation for arithmetic compare instructions (CAMX and CAIX).
AD CRY 0	AD2	Level. Indicates carry out of bit AD0.
AD CRY 1	AD2	Level. Indicates carry out of bit AD1.
AD CRY 36	AD1	When set, produces carry into AD35. Used for incrementing or for two's complement subtraction.
AD CRY 36 (FT9)	AD2	Level. Enables FT9 pulse to set AD CRY 36.
AD CRY ALLOW	AD2	Level. Completes the carry logic through AD bits 5, 14, 23, 32 (B138's). When false, speeds up carry de-propagation, important to multiply instructions.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
AD CRY INS	AD1	When set, produces carry into summing network of all adder bits turning the adder into an "EQUIVALENCE" gate for the normal inputs.
AD CRY INS (FT9)	AD2	Level. Enables FT9 pulse to set AD CRY INS.
AD = 0	AD2	Level. True when all adder bits are zero.
AD MD+	AD2	Level. Enables SCT3 pulse (and others) to set AD BR+ EN during multiply or divide subroutine, as determined by operands.
AD MD-	AD2	Level. Enables SCT3 pulse (and others) to set AD BR- EN and AD CRY 36 during multiply or divide subroutine, as determined by operands.
AD MINUS BR (FT9)	AD2	Level. Produces AD BR- EN (FT9) and AD CRY 36 (FT9). Setup for subtraction of BR contents from AR contents.
AD+1 BOTH (FT9)	AD2	Level. Produces AD CRY 36 (FT9) and permits FT9 pulse to set AD+1 LH.
AD+1 LH	AD1	When set, causes a "one" input to AD17.
AD-1 LH	AD1	When used in conjunction with AD BR+ EN and AD BR- EN, causes a "zero" input to AD17.
AF2	IA	Address cycle memory subroutine flip-flop. Also causes AT3 to deliver indexed address to AR from AD
AR0-35	AR1	Arithmetic register. Used for holding arithmetic operand. Communicates with memory bus, in-out bus, and fast memory.
AR0 = BR0	ARC3	Level. True for equal signs of AR and BR operands. Used during floating point exponent calculation. (FMP or FDV).
AR0 = SCAD0	ARC3	Level. True for equal signs of AR and SCAD (shift counter adder). Used during floating point exponent calculation. (FMP or FDV).
AR0 SHLT INP	ARMQ	Level. Provides left shift inputs to AR0 as shown on SCAF diagram.
AR35 SHLT INP	ARMQ	Level. Provides left shift inputs to AR35 as shown on SCAF diagram.
AR CRY 0 FLAG	ARF	Stores condition of AD CRY 0 resulting from certain arithmetic operations.
AR CRY 1 FLAG	ARF	Stores condition of AD CRY 1 resulting from certain arithmetic operations.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
AR DCK	ARF	Divide check flag. Set when fractional dividend not smaller than divisor.
AR FOV	ARF	Floating point overflow flag. Set for various error conditions by floating point instructions. Interrupt possible.
AR FXU	ARF	Floating point exponent underflow. Set by normalize return subroutine if result exponent is too negative to represent.
AR OV COND	ARF	True when overflow occurs during an additive process. An inequality (XOR) of AD CRY 0 and AD CRY 1. Used to set AR OV FLAG.
AR OV FLAG	ARF	Arithmetic overflow flag. Set by any arithmetic overflow condition. Interrupt possible.
AR SWAP	ARC1	Pulse. Causes the two 18-bit halves of AR contents to be exchanged.
ARO XOR AR1	ARF	Level. Used to set AR OV FLAG during an arithmetic left shift.
ARF CRY STB	ARF	Pulse. Causes AD CRY 0 and AD CRY 1 to be stored in AR CRY0 FLAG and AR CRY1 FLAG; and stores AR OV COND in AR OV FLAG.
AS COND	AS	Level. True when contents of console address switches equal the absolute core memory address. Used for address stop or break (MC2) and memory indicator loading (MI).
AS = FMA	AS	Level. True when contents of address switches equals output of FMA address selector.
AS = RLA	AS	Level. True when contents of address switches equals the memory bus memory address. (RLA is obsolete)
BIO CPA SEL	MR	Level. True when IR 3-9 contain 000. Processor device address.
BIO PI SEL	MR	Level. True when IR 3-9 contain 004. Priority interrupt device address.
BIO PTP SEL	MR	Level. True when IR 3-9 contain 100. Paper tape punch device address.
BIO PTR SEL	MR	Level. True when IR 3-9 contain 104. Paper tape reader device address.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
BIO TTY SEL	MR	Level. True when IR 3-9 contain 120. Console teletype device address.
BLT FI	BTMP	Subroutine flop for block transfer. Used when storing word in destination location.
BR0-35	BR2	Buffer register. Holds arithmetic operand.
BYF4	BYTE	Subroutine flop for restoring incremented pointer in byte instructions. Also enables MQ to shift left (MQ1) to generate mask.
BYF5	BYTE	Control flop for byte instructions. When zero causes "first part" activities (incrementation and/or size mask generation); when one causes "second part" activities (operand fetch and loading or depositing). BYF5 (0) produces PC+1 INH.
BYF6	BYTE	Byte increment status (BIS) flag. Set by ILDB and IDPB in "first part" and cleared in "second part". Prevents double incrementation if instruction is interrupted between parts as may happen. BYF6 is the "Byte Interrupt" stored by JSR, JSP, PUSHJ and restored by JRSTF.
BYTE PTR INC	BYTE	Level. Allows ET0 pulse to start "first part" at BYT1 for those conditions and instructions which require byte pointer incrementation.
BYTE PTR NOT INC	BYTE	Level. Causes bypassing of the incrementation sequence for those instructions which load or deposit but do not want to change the pointer at this time. Allows ET0 to pulse BYT6.
CPA ADR BREAK	CPA	Set by an address break condition. Interrupt possible.
CPA AR OV EN	CPA	When set, enables AR OV FLAG to processor interrupt decoder.
CPA CLK EN	CPA	When set, enables power frequency clock to processor interrupt decoder.
CPA CLK FLAG	CPA	Set by CPA PWR CLK once each cycle of line current. Interrupt possible.
CPA FOV EN	CPA	When set, enables AR FOV to processor interrupt decoder.
CPA MEM PROT FLAG	CPA	Set by MC ILLEG ADR when a memory reference in user mode uses a relative address larger than the protection constant. Interrupt possible.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
CPA NON EX MEM	CPA	Level. Set by MC NON EX MEM when no core module responds. Interrupt possible.
CPA PAR ENB	CPA	Level. Enables CPA PAR ERR to processor interrupt decoder.
CPA PAR ERR	CPA	Set by MC PAR ERR when even parity is detected in a word read from core memory.
CPA PDL OV	CPA	Push down list pointer overflow. Set if left half of pointer goes to zero when incremented or decremented by the pushdown instructions.
CPA PIA 33-35	CPA	Processor interrupt bus address storage flops. Non-zero to allow interrupt.
CPA PWR CLR	CPA	Pulse. One pulse per cycle of line current.
CPA PWR FAIL	CPA	Sets if two consecutive CPA PWR CLK pulses are missed. Interrupt possible.
DB BYTE DEP	DBLB	Level. Common to DPB and IDPB to condition "second part" operations such as shifting AR and MQ to the left.
DIV LOW ZERO COND	DSDV	Level. During the negation of two word dividends (floating or fractional) this indicates that second word is zero.
DSFI	DSDV	Divide subroutine flop. Enables left shift of AR and MQ at SCT3 with connections as shown on SCAF diagram. Permits AD MD+ and AD MD- to be controlled by BR0 and ADO.
DSF7	DSDV	Flip-flop used to store the original sign of the dividend in a divide instruction. (Divide subroutine requires a positive dividend.)
DSF7 XOR BR0	DSDV	Level. True when dividend and divisor are of opposite sign. Used at end of divide to correct the quotient sign.
E LONG	E	Level. Enabled by those instructions which use a long execution cycle (ET0, ET1, ET2). Permits ET0 DEL to pulse ET1.
E LONG V ST INH	E	Level. Prevents ET0 DEL from pulsing ST1.
E UUOF	E	Set by UUO instruction. Causes the following ITO to set MA35.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
E XCTF	E	Set by UUO, XCT, or KEY RDI DONE pulse to prevent the following ITO from disturbing the MA, which points to the instruction to be executed.
EFO LONG	E	Level. Causes a long delay to occur between FT9 and ET0 to allow for additive processes (AD XX EN set and carry propagation times).
EVEN 0-8	PN	Level. True when PB bits 0-8 contain even parity.
EVEN 0-26	PN	Level. True when PB bits 0-26 contain even parity.
EVEN 9-17	PN	Level. True when PB bits 9-17 contain even parity.
EVEN 18-26	PN	Level. True when PB bits 18-26 contain even parity.
EVEN 27-35	PN	Level. True when PB bits 27-35 contain even parity.
EX ALLOW IOTS	EX	Level. Indicates that machine is in executive mode or privileged user mode. Used on IR UUO.
EX ILL OP	EX	Set by UUO's which trap to absolute locations 40 or 60. Suppresses relocation by producing EX TRAP COND. Cleared by an IOT BLK executed from a PI location if UUO interrupted between halves. (Prevents unwanted memory reference by an unrelocated user PC.) Normal clear is by subroutine jump instruction in 41 or 61.
EX IOT USER	EX	Set by executive mode JRSTF only. Allows user program to use all instructions, does not affect relocation, however.
EX MODE SYNC	EX	When set, causes entry into user mode at subsequent ITO (MR CLR).
EX PI SYNC	EX	Set by PI CYC (1). Prevents relocation of PI trap address (40+2n) by producing EX TRAP COND.
EX REL A, B	EX	True when in user mode and not referencing an AC, UUO or PI trap location, or performing an examine or deposit. When true, causes address checking by the protection adder (PR) and use of relocated address (MAI).
EX TRAP COND	EX	Level. True when fetching an instruction from a PI trap location or a non-relocated UUO trap location. Prevents relocation by making EX REL A and EX REL B false. If fetched instruction is JSR, JSP, PUSHJ, will cause EX USER to clear (to exec. mode).



Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
EX USER	EX	When a one, machine is in user mode. Determines decoding of IR UO, EX REL A, EX REL B (chiefly).
FAC INH	F2	Level. ("Fetch AC Inhibit") When true, causes (AC) fetch to be bypassed in fetch cycle.
FAC2	F2	Level. ("Fetch AC <sub>2</sub> ") When true causes fetch of (AC+1) to occur (FT5).
FAF1	FA	Shift subroutine flop set by floating add routine.
FCC ACLT	F2	Level. ("Fetch C ( C (AC) Left)") When true causes the left half contents of fetched AC to be used as an operand address from which a word is fetched (FT7).
FCC ACRT	F2	Level. ("Fetch C ( C (AC) Right)") When true causes the left half contents of fetched AC to be used as an operand address from which a word is fetched (FT7).
FCE	F2	Level. ("Fetch C(E)") When true causes the contents of the location addressed by MA to be fetched by MC RD RQ. (FT0).
FCE PSE	F2	Level. ("Fetch C(E); Pause") When true causes the contents of the location address by MA to be fetched by MC RD/WR RS. (FT1). This level is produced instead of FCE by those instructions which store a result in the location from which a memory operand was fetched, and which have a relatively short execution time. (e.g. FADM doesn't meet the latter requirement, SUBM meets both.)
FDF1	FDV	Memory subroutine flop set when floating divide fetches dividend exponent from memory.
FDF3	FDV	Flop set to store fact that dividend was unnormalized by one right shift. Used at end of floating divide to assure proper remainder exponent (which is related to dividend exponent).
FMA AC EN	FMA	Level. Makes FMA 32-35 a copy of IR 9-12. (Accumulator address).
FMA AC2 EN	FMA	Level. Makes FMA 32-35 equal to (IR 9-12) +1.
FMA MA EN	FMA	Level. Makes FMA 32-35 a copy of MA 32-35. Also inhibits FMA AC EN, FMA AC2 EN, and FMA XR EN. Produced when a core memory request is initiated to read out of a fast memory location (e.g. PC or E is 0-18).

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
FMA XR EN	FMA	Level. Makes FMA 32-35 a copy of IR 14-17. (Index register address).
FMD 0-17	FMA	Level. Binary to 1 out of 16 decoder. One output selects a 36 bit fast memory location (FM).
FP EXP ADD	FPFM	Level. Used during exponent calculation to change SCAD inputs so that exponent magnitudes are added during FMPX and subtracted during FDVX instructions.
HWT 3 LET	HWT	Level. ("half-word transfer (3 Letter)") in direct mode which specify that "other half" is to be preserved. (e.g. HRL).
HWT ARLT CLR (ET0)	HWT	Level. True for half-word transfers which zero the left half. (e.g. HXRZX). The action occurs at ET0 because of this level.
HWT BR ± EN (FT9)	HWT	Level. Produces AD BR ± EN (FT9) for those half word instructions which set to ones the "other half" receiving word.
HWT DIR	HWT	Level. Direct or blank mode for half word instructions. (IR7 and 8 = 0).
HWT E TEST	HWT	Level. Used for HXXEX instructions to determine the four outcomes: 0 to left, 0 to right, 1's to left, 1's to right.
IFO	IA	Instruction fetch/indirect word fetch memory subroutine flop. Also used in address condition test (MC2).
IOB0-35	IOB1	In-out bus data lines
IOB BUS RESET A-D	IOBC	A 2 μs pulse that switches 20 mA additional clamped load to each bus data line (IOB0-35) to restore the zero state (-3V).
IOB CONO CLR	IOBC	Conditions out clear. A 400 ns pulse that may be used by a device to clear its command/status register.
IOB CONO SET	IOBC	Conditions out set. A 400 ns pulse used by devices to load command register from IOB0-35.
IOB DATAI	IOBC	A 2.5 μs pulse used to gate an input device data register to IOB0-35.
IOB DATAO CLR	IOBC	Data out clear. A 400 ns pulse used by output device to clear data register.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
IOB DATAO SET	IOBC	Data out set. A 400 ns pulse used by output device to load its data register from IOB0-35.
IOB DR SPLIT	IOBC	"Drum split." May be activated by a device attached to memory port to prevent processor from doing read-modify-write cycles. (See MC SPLIT CYC SYNC).
IOB PI 1-7	IOBC	Bus priority interrupt lines. Grounded by a device requesting service on that channel.
IOB RDI DATA	IOBC	Readin data flag. Activated by device during a key read in operation when a data word is ready.
IOB RDI PULSE	IOBC	Readin pulse. A 400 ns pulse issued to start the selected device for key readin operations.
IOB RESET	IOBC	General clear pulse going to all devices.
IOB STATUS	IOBC	A 2.5 $\mu$ s pulse used to gate a device status register to IOB0-35. Called IOB CONI on IO bus.
IOS 3-9	IOBC	Device selection code. A buffered version of IR 3-9.
IOT BLK	IOT	Level. True for either BLKI OR BLKO op codes.
IOT CONSX	IOT	Level. True for either CONSO or CONSZ op codes.
IOT DATA XFER	IOT	A 2.5 $\mu$ s pulse. Basic timing for placing information on IOB0-35.
IOT F1	IOT	Memory subroutine flop used by BLKI, BLKO when restoring incremented pointer.
IOT GO	IOT	Synchronizing flip-flop that is set at ET0 to request entry into IOTT0-5.
IOT OUT GOING	IOT	Level. True for either CONO or DATAO or second part of BLKO.
IR 0-17	IR	Instruction register. Holds OP, AC, I, X during execution.
IR OXX	IR1	Level. Means op code in range 000 to 077.
IR 13X	IR2	Level. Indicates op code in range 130 to 137.
IR 26X E LONG	IR3	Level. True for those codes in this range requiring long execution cycle. Pushdowns, JSR, JSA, JRA.
IR AOJX	IR3	Level. True for Add one and jump, any mode.
IR AOSX	IR3	Level. True for Add one and skip, any mode.
IR AOXX	IR3	Level. True for AOJX or AOSX.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
IR AS	IR1	Level. True for add or subtract, any mode.
IR AS BOTH	IR3	Level. True for ADDB, SUBB. Used to provide fetch cycle levels (F2).
IR AS DIR	IR3	Level. True for ADD, SUB. Used to provide fetch cycle levels. (F2).
IR AS IMM	IR3	Level. True for ADDI, SUBI.
IR AS MEM	IR3	Level. True for ADDM, SUBM. Used to provide fetch cycle levels. (F2)
IR BOOLE 0-17	IR2	Levels. Decoding of the 16 Boolean instructions, any mode. (See BIF1.)
IR FDV NOT L	IR3	Level. True for FDV, FDVR, all modes except FDVL.
IR FP	IR2	Level. True for op codes 140-177 (Floating point) unless floating point trap switch is on (IR UUO, IR2 drawing),
IR IOT	IR2	Level. True when IOT op code in IR and IOT's are permissible (See IRUUO).
IR IOT A	IR1	Level. True when IR0-2 = 7 (IOT op code).
IR JRST	IR2	Level. True when JRST op code in IR and JRST is permissible. (See IRUUO)
IR JRST A	IR1	Level. True when 254 op code in IR (JRST op code).
IR JUMPS	IR3	Level. True for JUMPX, AOJX, SOJX op codes. Used to condition PC from MA transfer during these instructions (PC1).
IR LT EN	IR	When set, enables IR bits 0-12 to receive input from memory bus.
IR MD	IR2	Level. True for MUL, IMUL, DIV or IDIV op codes, any mode.
IR RDI SETUP	IR	Pulse. Issued by key readin operation to force IR to contain DATAI DEV, or BLKI DEV, depending on RDI PART 2 flop. "DEV" (IR3-9) determined by readin device switches on maintenance panel.
IR RT EN	IR	When set, enables IR bits 13-17 to receive input from memory bus.
IR TEST	IR1	Level. True when op code 600-677 in IR. Boolean test class of instructions.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
IR UO	IR2	Level. Unimplemented User Operation True for op codes 000-127 and 130-177 if FP trap switch is on. Also true for IOT, HALT, JEN in non-privileged user mode. When true, inhibits IR IOT and IR JRST.
ITO-IT1	IA	Instruction cycle time pulses.
KEY ADR BRK	KEY1	Level. True when console ADR BREAK switch is on.
KEY ADR INST	KEY1	Level. True when console ADDRESS CONDITION INST FETCH switch is on.
KEY ADR RD	KEY1	Level. True when console ADDRESS CONDITION DATA FETCH switch is on.
KEY ADR STOP	KEY1	Level. True when console ADR STOP switch is on.
KEY ADR WR	KEY1	Level. True when console ADDRESS CONDITION WRITE switch is on.
KEY AS STROBE EN	KEY3	Level. True for those key operations which use data switch information.
KEY AT INH	KEY2	100 $\mu$ s level. Produced by RESET with RUN (1). Holds IFO cleared to stop instruction cycle, preventing data from being clobbered when clear pulse is issued.
KEY CONT SW	KEY1	Continue. Momentary level true when console CONT switch is held on.
KEY DEP NXT SW	KEY1	Deposit next. Momentary level, true when console DEPOSIT - NEXT switch is held on.
KEY DEP SW	KEY1	Deposit this. Momentary level, true when console DEPOSIT - THIS switch is held on.
KEY EX NXT	KEY1	Examine next. Momentary level, true when console EXAMINE - NEXT switch is held on.
KEY EXA SW	KEY1	Examine this. Momentary level, true when console EXAMINE - THIS switch is held on.
KEY EXE SW	KEY1	Execute. Momentary level, true when console XCT switch is held on.
KEY F1	KEY3	Memory subroutine flop used by examines and deposits. Also used in MI control to allow data to be displayed.
KEY FCN CLR	KEY1	Pulse. Clears key function storage register at termination of function execution.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
KEY FCN STROBE	KEY1	Pulse. Loads corresponding function register flop from momentary key level.
KEY ITO EN	KEY3	Level. True when FT9 to be allowed to pulse ITO.
KEY MANUAL	KEY1	Level. Produced by key functions to initiate timing chain.
KEY MEM REF	KEY3	Level. True for those key functions (examines and deposits) which reference memory.
KEY MID INST STOP	KEY3	Level. True when a memory stop or shift counter stop has occurred. Used to condition action of CONT key on RUN flip-flop.
KEY NEXT	KEY3	Level. True for examine next or deposit next. Causes key flow to increment MA.
KEY NXM STOP	KEY1	Level. Non-existent memory stop. True when console NXM STOP switch is on. Used in memory control (MC2).
KEY PAR STOP	KEY1	Level. Parity stop. True when console PAR STOP switch is on. Used in memory control (MC2).
KEY PI INH	KEY1	Level. True during key execute operation to prevent interrupts and PC incrementation at FT9. (PI1 and PC1).
KEY PROG STOP	KEY3	Level. True for HALT instruction, enables clearing of RUN flop.
KEY RDI DLY	KEY2	One-shot. Used to produce IOB RDI PULSE to start read in device. Delay permits device selection levels to settle down on bus.
KEY RDI DONE	KEY3	Read in done. Pulse sets up machine to execute the last word read in by setting RUN and E XCTF.
KEY RDI PART 2	KEY3	Determines how IR12 is affected by IR RDI SETUP pulse to cause either DATAI or BLKI op code.
KEY RDI SW	KEY1	Momentary level. True when console READ IN switch is held on.
KEY REPEAT BYPASS SW	KEY1	Level. True when maintenance panel REPEAT BY-PASS switch is on. Used when troubleshooting key time pulses. Allows KTO to be retriggered by the repeat delay.
KEY REPEAT SW	KEY1	Level. True when console REPT switch is on. Inhibits KEY FCN CLR and allows KEY DONE to retrigger KTO after the delay as controlled by maintenance panel speed knobs.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
KEY REPT DLY	KEY1	Variable delay controlled by speed knobs on maintenance panel. Used to retrigger KT0.
KEY REPT SYNC	KEY1	Set by KEY REPEAT operations, inhibits KEY FCN CLR.
KEY RESET SW	KEY1	Momentary level. True when console RESET switch is held on.
KEY RIM	KEY3	Remains set during readin operation. Allows entry to IT0 when IOB RDI DATA pulse occurs (for each data word). Also allows BLKI pointer overflow to set PI OV.
KEY RUN CLR	KEY3	Pulse. Clears RUN flop at time appropriate to operation (HALT, STOP switch, or SING INST switch).
KEY SING CYCLE	KEY1	Single cycle. True when console SING CYCLE switch is on. Causes memory stop after each reference.
KEY SING INST	KEY1	Single instruction. True when console SING INST switch is on. Used to clear RUN during instruction execution.
KEY SP CNTL-X	KEY1	Connections to coarse and fine speed controls on maintenance panel. (See KEY REPT DLY)
KEY STA SW	KEY1	Momentary level. True when console START switch is held on.
KEY STOP SW	KEY1	Momentary level. True when console STOP switch is held on.
KEY SYNC	KEY3	Set to allow ST9 to pulse KT1 for those key functions which operate when RUN is a one (EXA THIS, DEP THIS, EXE).
KEY SYNC RQ	KEY3	Set by certain key functions (see KEY SYNC) to enable FT9 to set KEY SYNC.
KNT1-3	KEY3	Pulse chain used by key next operations to increment MA.
KST1-2	KEY2	Pulse chain used by STOP and RESET functions.
KT0-KT4	KEY2	Key timing pulse chain.
LB BYTE LOAD	DBLB	Level. Produced for LDB, ILDB "second part" to cause fetching of operand, loading of byte.
M BUS 0-35	MBDI	Memory bus data lines, bi-directional. Connect to AR and IR. Called MBD0-35 on Memory Bus.
MA 18-35	MA2	Memory address register.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MA 18-31 = 0	MAI	True when MA contains an address in range 0-17. Used to cause MC access to fast memory if one exists or to suppress relocation (EX REL A, B) if one does not.
MA 29-35 SET	MAI	Pulses. Used to force reserved location addresses into a cleared MA. Used in PI, UJO Operations.
MA FM PICH (1)	MAI	Pulse. Sets address $40 + 2N$ into MA in response to interrupt on channel N.
MA TRAP OFFSET	MAI	Level. True when switch in bay 1 is on. Used to change references to non-relocated 40-61 to 140-161 as in a dual processor system.
MAI 18-35	MAI	Memory address interface. The address bits that go on the memory bus. May be copy of MA, RLA and MA, or FMA.
MAI CMC ADR ACK	MAI	Pulse. Core memory address acknowledge. Issued by addressed module at start of memory cycle.
MAI CMC RD RS	MAI	Pulse. Core memory read restart. Issued by core memory at same time data strobed onto bus to enter the AR.
MAI FMA SEL	MAI	Set when core locations 0-17 are to be addressed from FMA address selector. Makes MAI 18-31 = 0 and MAI 32-35 a copy of FMA 32-35.
MAI IGN PAR PULSE	MAI	Core memory ignore parity pulse. May be issued by memory at same time as ADR ACK to inhibit processor parity checking.
MAIB 21-35	MAI	Buffered MAI bits. Called MADR 21 to 35 on memory bus.
MAIB FMC SELECT	MAI	For bus compatibility with PDP-6. Pin T must be negative and pin V ground to allow memory modules to accept requests.
MAIB MC RD	MAI	Buffered read signal (level) to core memory. Called RD REQ on memory bus.
MAIB MC REQ CYC	MAI	Buffered request level to core memory. Used to start memory access. Inhibited during power up process. Called REQ CYC on memory bus.
MAIB MC WR	MAI	Buffered write signal (level) to core memory. Called WR REQ on memory bus.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MAIB MM 18-21,35	MAI	Bipolar module selection levels to bus. Four bits to address a module, may be 18-21 (normal) or 18-20, 35 (interleaved) as determined by switches on module. Called MADR18-22, 35 on memory bus.
MC ADR ACK	MC1	Local acknowledge pulse triggered by MAI CMC ADR ACK. Clears parity buffer and MC RQ flop to end nonexistent memory check.
MC ADR BREAK SET	MC2	Pulse to set CPA address break flop when conditions are met.
MC BUS WR RS	MC1	Pulse to core memory to enable write portion of cycle. Issued after data sent to module.
MC FM EN	MC1	Level. True when maintenance panel FM DISABLE switch is off. Causes all references to address 0-17 to go to fast memory. If false, causes core memory references to these addresses and prevents read-modify-write (pause) operations.
MC FM RD RQ	MC1	Pulse to initiate reading core locations 0-17 when in address or fetch cycles. (AC or AC2 fetch).
MC FM WR RQ	MC1	Pulse to initiate writing core locations 0-17 when in store cycle (AC or AC2 store).
MC IGNORE PARITY	MC2	Flop set by MAI IGN PAR PULSE to inhibit parity checking when reading from a 36 bit (no parity plane) core memory.
MC ILLEG ADR	MC2	Pulse. Happens if protection violation in user mode memory reference. Sets CPA MEM PROT FLAG and causes exit from memory subroutine with no reference to core memory.
MC NON EX MEM	MC2	Pulse occurs 100 $\mu$ s after memory request if no response (ADR ACK). Sets CPA NON EX MEM flop and causes exit from the memory subroutine.
MC NXM RD	MC2	Pulse. Uses NON EX MEM pulse to simulate action of read restart.
MC NXM RST	MC2	Pulse. Uses NON EX MEM pulse to simulate action of address acknowledge.
MC PAR ERR	MC1	Parity error pulse. Occurs during read if 37 bits have even parity unless told to ignore parity. Sets CPA PAR ERR flop.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MC PAR STOP	MC2	Set by request pulse if console PAR STOP switch is on. Lengthens read timing to allow parity checking to take place between RD RS and MC RST0. Will enable MC STOP to set if error detected.
MC PARITY PULSE	MC1	Bidirectional pulse generated by a one in plane 36 of core memory during a read and sent to the parity buffer (PB) also generated by processor during a write at same time as MC WR RS, if necessary.
MC RD	MC2	Read command flop. Produces MAIB MC RD. Enables MBDI 0-35 to receive data from M BUS 0-35.
MC RD RQ PULSE	MC1	Pulse triggered from instruction flow to start a memory read operation. Sets MC RD.
MC RD RS	MC1	Local pulse produced by MAI CMC RD RS. Starts parity checking.
MC RD/WR RQ PULSE	MC1	Pulse triggered from instruction flow to start a read-pause operation. Sets both MC RD and MC WR.
MC RD/WR RS	MC1	Pulse triggered from instruction flow to restart a paused memory in the write cycle.
MC REQ CYC	MC2	Level. When true, causes a request to core memory.
MC RQ	MC2	Flop set by read, read-pause, or write requests. Causes a core memory or fast memory cycle to begin depending upon the contents of MA and MC FM EN.
MC RQ PULSE	MC1	Pulse common to all memory requests. Starts non-existent memory timer, and address checking. Causes PI system to strobe requests from I/O bus.
MC SPLIT CYC EN	MC2	Level. True for those cases in which read-modify-write (pause) operations must be prevented.
MC SPLIT CYC SYNC	MC2	Flop set to prevent read-modify-write (pause) cycles. Enables MC RD/WR RQ pulse to trigger MC RD RQ pulse and MC RD/WR RS pulse to trigger MC WR RQ.
MC STOP	MC2	Flop set to inhibit normal exit from MC subroutine by any memory stop condition. Allows continue key to pulse MC RS T0.
MC STOP EN	MC2	Level. Allows MC STOP SET pulse to set MC STOP flop if doing single cycle or satisfied address stop condition.
MC SW COND	MC2	Level. True when ADDRESS CONDITION conditions are satisfied. Distinguishes between instruction fetch, data fetch, or write.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MC WR	MC2	Write command flop. Produces MAIB MC WR and conditions actions occurring after ADR ACK is received.
MC WR RQ PULSE	MC1	Pulse triggered from instruction flow to start a write operation. Sets MC WR.
MC RST0-1	MC1	Final pulses of MC subroutine. Cause return to instruction flow depending on subroutine flop.
MI 0-35	MI	Memory indicator register. Displays data on console lights. Loaded by key functions (examine, deposit) or by program (DATAO PI).
MI PROG	MI	When set, prevents MI from automatically displaying contents of location addressed by console address switches. Preserves program display.
MI PROG DIS SW	MI	True when maintenance panel MI PROG DIS switch is on. Forces automatic display of location addressed by switches.
MIT0-1	MI	Pulses produced by references to a location addressed by the address switches. Will cause loading of MI from AR if MI PROG is zero. (So-called automatic display).
MPF1	BTMP	Fixed point multiply subroutine flop. Enables return to MPT2 from SCT4.
MPF2	BTMP	Multiply sign storage. Set if both operand signs negative. Used for fractional overflow test at MPT2.
MPT2-4	BTMP	Fixed point multiply execution time pulses.
MQ 0-35	MQ2	Multiplier-quotient register. Can be loaded from AD, and shifted left or right one place.
MQ 0 SHLT INP	ARMQ	Level. Provides input to MQ bit 0 for left shift operations shown on SCAF diagram.
MQ 0 SHRT INP	ARMQ	Level. Provides input to MQ bit 0 for right shift operations shown on SCAF diagram.
MQ 1 SHRT INP	ARMQ	Provides input to MQ bit 1 for right shift operations shown on SCAF diagram.
MQ 7 SHLT INP	ARMQ	Provides input to MQ bit 7 for left shift operations shown on SCAF diagram.
MQ 8 SHRT INP	ARMQ	Provides input to MQ bit 8 for right shift operations shown on SCAF diagram.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MQ 9-35 = 0	MQ1	Level. True as stated. Used by normalize subroutine for making rounding and zero result decisions.
MQ 35 SHLT INP	ARMQ	Provides input to MQ bit 35 for left shift operations shown on SCAF diagram.
MR CLR, A, B	MR	"Master clear". (Mister Clear). Clears subroutine flops, SC, MQ, IR, sets adder enables for indexing, enables IR to memory bus, and generally prepares processor for fetching and executing the current instruction.
MR PWR CLR	MR	B-series clear pulses produced at a 500 kHz rate when powering up or down.
MR PWR CLR R	MR	R-series (400 ns) pulses at 500 kHz rate.
MR PWR CLR ENB	MR	A 5 second level occurring shortly after power turn-on and 100 ms after power turn-off. Enables 500 kHz pulse source for MR PWR CLR.
MR START, A, B	MR	A general system clear, more general than MR CLR. Resets peripheral devices as well as processor. Caused by PWR CLR, console RESET operation, and at start of readin operation.
MR START R	MR	R-series (400 ns) pulse produced by MR START.
MSFI	BTMP	Multiply subroutine-shift counter subroutine flop. Causes right shift of AR, MQ at SCT3 (ARC2, MQ1) and qualifies register connections (ARMQ). Also allows AD MD+ and AD MD- to be controlled by MQ 34 and 35.
MST0-1	BTMP	Multiply subroutine time pulses.
NLT0-4	NRNL	Pulses. "Normalize long time". Part of normalize return subroutine that determines exponent for second word in floating point long mode instructions.
NR ALL ZERO	NRNL	Level. True when floating point result is zero in both AR and MQ.
NR NORMAL	NRNL	Level. True when a floating result is normalized or if UFA op code in IR.
NR ROUND	NRNL	Level. True when data condition and op code specify rounding to take place. Permits NRT3 delayed to pulse NRT6.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
NR SH RT COND	NRNL	Level. True when a significant bit of result mantissa is in AR bit 8. Causes NRT10 to make one right shift.
NRFI	NRNL	Normalize return rounding control flop. Prevents rounding the same result more than once.
NRT0-7, 10, 99	NRNL	Normalize return subroutine pulses.
ODD 0-8	PN	True when PB bits 0-8 contain odd parity.
ODD 0-26	PN	True when PB bits 0-26 contain odd parity.
ODD 9-17	PN	True when PB bits 9-17 contain odd parity.
ODD 18-26	PN	True when PB bits 18-26 contain odd parity.
ODD 27-35	PN	True when PB bits 27-35 contain odd parity.
PB 0-35	PB	Parity buffer data bits. Loaded from memory bus. Drives parity computing network (PN).
PB PAR	PB	Parity buffer parity bit. May be set during a read. Is held clear during write to force PN to compute parity of ones in PB 0-35.
PC 18-35	PC2	Program counter register. Contents used to address memory to fetch instruction.
PC COND P	PC1	Level used by arithmetic compare or test (op 300-377) instructions. True when Equal, Not equal, or Always conditions are satisfied. Allows PC to be changed at ET0.
PC COND Q	PC1	Level used by arithmetic compare (op 300-317) instructions. True when Less than or Greater than conditions are met. Allows PC to increment at ET0.
PC COND R	PC1	Level used by arithmetic test (op 320-377) instructions. True when less than or greater than conditions are met. Allows PC to be changed at ET0.
PC SET (ET0)	PC1	Level. True to allow ET0 pulse to load PC from MA.
PC+1 (ET2)	PC1	Level. True to allow ET2 pulse to increment the PC.
PC+1 INH	PC1	Level. True to prevent FT9 pulse from incrementing PC.
PCLT+1	PC1	Pulse. Transfers increment network outputs to PC 18-26.
PCRT+1	PC1	Pulse. Transfers increment network outputs to PC 27-35.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
PI ACT	PI1	Priority interrupt system active. When zero, no interrupt requests will be recognized. When true, enables priority network at PI REQ 1 and PI OK 2.
PI CYC	PI1	Flop set during execution of PI location contents. Prevents interruption of instruction in that location, also inhibits PC incrementation. Sets EX PI SYNC to inhibit relocation.
PI DATA I/O	PI1	Level. DATAI or DATAO op code in IR. (Intent is second half of BLKI or BLKO).
PI ENC 32-34	PI1	Level. Octal to binary encoding of channel number whose PI REQ n is currently true. Used in MA control to generate address 40+2N or 40+2N+1.
PI HOLD	PI1	Level. When true allows PIHn flop to set for channel now being serviced. Allows PI OV and PI CYC to be cleared.
PI OV	PI1	Flop set during BLKI/BLKO instruction if left half of pointer overflows, but only during interrupt or key read in situations. Inhibits PI HOLD, PI RESTORE, causes ITO to generate 40+2N+1 in MA.
PR REQ 1-7	PI2	Priority network "request granted" outputs. Only one can be true at a time (highest priority one, lowest number).
PI RESTORE	PI1	Level. When true allows the highest priority (lowest numbered) PI in progress flop (PIH) to be cleared.
PI RQ	PI1	Priority interrupt request. Alters instruction flow after ITO, BLTT3. Produced by any PI REQ n level but is inhibited by KEY PI INH (key execute) or PI CYC (1).
PIH 1-7	PI2	PI Hold register. (PI IN PROGRESS lights on console). PIHn (1) feeds back to priority network preventing PI REQ n through PI REQ 7 from being produced. Also clears PIRn.
PIO 1-7	PI2	PI On. Channel on/off switch or enable. PION must be a one to allow IOB PI RQn to be loaded into PIRn.
PIOK 2-7	PI2	Priority network functions. PIONn must be true to allow PI REQ n to happen. PIONn means there is nothing currently in progress or being requested for channels 1 through n-1.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
PIR 1-7	PI2	PI Request storage. Stores requests for enabled channels. PI bus strobed each core memory reference by MC RQ PULSE. Can also be set by CONO PI, to initiate interrupt from within program. Outputs go to priority network.
PN PAR EVEN	PN	Level. True for even parity in PB 0-35 and PB PAR. Used in MC subroutine (MC1).
PN PAR ODD	PN	Level. True for odd parity in PB 0-35 and PB PAR.
PR 18-25	PR	First protection register. Holds protection constant.
PRB 18-25	PR	Second protection register.
PRA ILL ADR	PR	Protection adder illegal address. True when MA 18-25 are greater than PR 18-25, or PRB 18-25 and memory protection is desired. Used in memory control (MC2).
RDI SEL 3-9	IR	Read in device selection switches. Located on maintenance panel.
RL 18-25	RL	First relocation register. Holds relocation constant.
RLA 18-25	RL	First relocation adder. Forms sum of MA 18-25 and RLA 18-25. Outputs may be used by MAI logic.
RLB 18-25	RL	Second relocation register.
RLC 18-25	RL	Second relocation adder, sum of MA 18-25 and RLB 18-25.
RUN	KEY3	Run flip-flop. When set, allows repetition of IT0-ST9 sequence. Clearing run causes a program to stop with ST9 of current instruction.
SAC = 0	S2	True when IR9-12 = 0000. Used by store cycle to inhibit storing result in AC zero for Self mode and skip instructions.
SAC INH	S2	Store AC inhibit. Prevents storage of AR in location addressed by FMA.
SAC2	S2	Store AC2. Causes store cycle to write MQ into location AC+1.
SAR ≠ BR	S2	Causes store cycle to write AR contents into (AC) and BR contents into (MA).
SC 0-8	SC	Shift counter register. Used to control shift count subroutine and for floating exponent calculation.

Table 1-3 (Cont)  
KA10 Signal Glossary

Signal Name	Source Drawing	Description
SC 0-8 CLR or SET	SC	Outputs of shift counter incrementation network.
SC0 = AR0	SCC2	True when SC sign equals AR sign. Used by floating add to make AR contain operand with smaller exponent. (FAT3A).
SC DATA 0-8	SCAD	Outputs of a data multiplexer that supplies data to be arithmetically combined with SC by SCAD (shift count adder.)
SC FP SETUP	SCC2	Shift count pre-load for floating multiply ( $745_8$ ) or divide ( $744_8$ ).
SC MD SETUP	SCC2	Shift count pre-load for fixed point multiply or divide ( $735_8$ ).
SC NEGATE SETUP	SCC1	Sets the SCAD controls to cause the negative of SC to appear at the SCAD outputs.
SC SBR (ET0)	SCSR	Level to allow ET0 to pulse SCT0 for certain instructions.
SC STOP	SCSR	When set, inhibits SCT1 pulse until continue key is set. Controlled by SC STOP.
SC STOP SW	SCSR	When maintenance panel switch is on, allows SCT0 to set SC STOP.
SC+1	SC	Pulse that transfers SC incrementing network outputs to SC during shift count subroutine.
SC+ EN	SCC1	Sets the SCAD controls to cause an addition of the SC and DATA.
SC- EN	SCC1	Sets the SCAD controls to cause the data to be subtracted from the SC. Result at SCAD outputs.
SCAD 0-8	SCAD	Shift counter adder. Performs arithmetic operations on SC contents and selected other data.
SCAD 200 EN	SCC1	When set, makes SC DATA equal $200_8$ .
SCAD 33 EN	SCC1	When set, makes SC DATA equal 033. (May be 032 if FDF3(1) during floating divide).
SCAD ALL DIS	SCC1	Sets the SCAD controls to cause SCAD outputs to be only a copy of SC.
SCAD AR 6-11 EN	SCC1	When set, makes SC DATA a copy of AR 6-11 contents. (Byte pointer size field).
SCAD BR EN	SCC1	When set, makes SC DATA a copy of BR0-8. (Floating point operand exponent).



Table 1-3 (Cont)  
KA10 Signal Glossary

<u>Signal Name</u>	<u>Source Drawing</u>	<u>Description</u>
SCAD DATA 0	SCC1	When set, gates SC DATA true to SCAD B138's.
SCAD DATA 1	SCC1	When set, gates SC DATA false (complement) to SCAD B138's.
SCAD SC COMP	SCC1	When set, gates SCn(0) to SCADn. When cleared, gates SCN(1) to SCADn.
SCAD SC COMP SETUP	SCC1	Sets SCAD controls to make SCAD outputs the complement of SC contents.
SCAD SC+1 SETUP	SCC1	Sets SCAD controls to make SCAD output equal (SC) +1.
SCAD SC+BR SETUP	SCC1	Sets SCAD controls to make SCAD take sum of SC and BR 0-8.
SCAD SC-BR SETUP	SCC1	Sets SCAD controls to make SCAD take difference between SC and BR 0-8.
SCAD +1 EN	SCC1	When set, causes carry into SCAD 8.
SCE	S2	Store contents of E. Causes store cycle flow to write AR into (MA).
SCT0-4	SCSR	Shift count subroutine time pulses.
SF1	S1	Store cycle memory subroutine flop.
SF6	S1	Store cycle memory subroutine flop.
SF8	S1	Store cycle memory subroutine flop.
SR GO LEFT	SCSR	Level. True for shift-rotate instructions with positive effective address. Enables SCT3 to produce AR and MQ shift left pulses.
SR GO RIGHT	SCSR	Level. True for shift-rotate instructions with negative effective address. Enables SCT3 to produce AR and MQ shift right pulses.
SR OP	SCSR	Level. True for shift or rotate instructions.
SRT1	SCSR	Shift-rotate time pulse. Used to negate shift counter for left shifts and rotates.
ST INH	S2	Store inhibit. When true prevents ET0 or ET2 from pulsing ST1. Used by instructions which have special execution pulse chains.
ST0-9	S1	Store cycle pulses.

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DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-KA10-A-0	L	3	KA10 ASSEMBLY
A-PL-KA10-A-0	L	8	KA10 ASSEMBLY PARTS LIST
D-BS-KA10-0-AD1	A	1	ADDER CONTROL FLIP-FLOPS
D-BS-KA10-0-AD2	A	1	ADDER CONTROL
D-BS-KA10-0-AD3		1	ADDER LEFT HALF
D-BS-KA10-0-AD4		1	ADDER RIGHT HALF
D-BS-KA10-0-AR1		1	AR REGISTER
D-BS-KA10-0-AR2		1	AR REGISTER
D-BS-KA10-0-AR3		1	AR REGISTER
D-BS-KA10-0-AR4		1	AR REGISTER
D-BS-KA10-0-ARC1	C	1	AR CONTROL PULSE
D-BS-KA10-0-ARC2	A	1	AR CONTROL PULSE
D-BS-KA10-0-ARC3	A	1	AR CONTROL PULSE
D-BS-KA10-0-ARF	B	1	ARITHMETIC FLAG
D-BS-KA10-0-ARI		1	AR INPUTS
D-BS-KA10-0-ARMQ		1	AR & MQ SHIFT CONNECTIONS
D-BS-KA10-0-AS		1	ADDRESS SWITCH COMPARATORS
D-BS-KA10-0-BR1	A	1	BR CONTROL
D-BS-KA10-0-BR2		1	BR REGISTER
D-BS-KA10-0-BTMP		1	BLOCK TRANSFER AND MULTIPLY

REVISIONS				DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
REV.	DATE	CHG. NO.	APP'D.	W. STEPHENSON	3/27/67	
A	2/26/68	7	R.C.	W. Stephenson	3/27/67	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS  TITLE KA10 PROCESSOR (60 HZ 115V)
B	2/68	7A	D.A.			
C	4/68	21	J.S.			
D	4/68	25	R.C.	A. Kotch	25 JAN 68	
E	5/68	25	R.C.			
F	5/68	25	R.C.			
G	5/68	26A	R.C.			
H	8/68	00003	T.L.			
J	12/68	00007	A.K.			
K	1/69	00008	A.K.			
L	1/69	00010	A.K.			
M	1/69	00011	A.K.			
N	1/69	00012	A.K.			
P	2/4/69	00014	P.S.			
S	2/21/69	00015	A.K.			
T	2/21/69	00017	A.K.			

SIZE	CODE	NUMBER	REV.
A	ML	KA10-A	AT
SCALE		SHEET 1 OF 8	DIST.

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D-BS-KA10-0-BYTE		1	BYTE INSTRUCTION FIRST PART
D-BS-KA10-0-CPA	B	1	ARITHMETIC PROCESSOR STATUS REG
D-BS-KA10-0-DBLB		1	BYTE DEPOSIT AND LOAD
D-BS-KA10-0-DSDV	A	1	DIVIDE SUBROUTINE & FIXED DIVIDE
D-BS-KA10-0-E	A	1	EXECUTION CYCLE
D-BS-KA10-0-EX	B	1	EXECUTIVE CONTROL
D-BS-KA10-0-F1		1	FETCH CYCLE TIME PULSE
D-BS-KA10-0-F2		1	FETCH CYCLE LEVELS
D-BS-KA10-0-FA		1	FLOATING ADD INSTRUCTION
D-BS-KA10-0-FDV		1	FLOATING DIVIDE
D-BS-KA10-0-FE		1	FLOATING EXPONENT REGISTER & CONTROL
D-BS-KA10-0-FM		1	FAST MEMORY
D-BS-KA10-0-FMA	A	1	FAST MEMORY ADDRESS
D-BS-KA10-0-FPFM		1	FP EXP CALC FLOATING MULTIPLY
D-BS-KA10-0-HWT		1	HALF WORD TRANSFER
D-BS-KA10-0-IA		1	INSTRUCTION & ADDRESS CYCLES
D-BS-KA10-0-IOB1	A	1	I/O BUS (0-17)
D-BS-KA10-0-IOB2	A	1	I/O BUS (18-35)

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REV.	DATE	CHG. NO.	APP'D.	W. STEPHENSON	3/6	
U	2/27/69	00019	A.K.	W. Stephenson	3/6	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS  TITLE KA10 PROCESSOR (60 HZ 115V)
V	3/19/69	KA10-20	A.K.			
W	4/18/69	00021	H.G.			
Y	4/23/69	00022	A.K.			
Z	5/16/69	00023	A.K.			
AA	5/69	00024	A.K.			
AB	5/69	00025	A.K.			
AC	6/69	00026	A.K.			
AD	6/69	00033	A.K.			
AE	7/69	00034	A.K.			
AF	7/69	00035	A.K.			
AH	7/69	00037	A.K.			
AJ	7/69	00040	A.K.			
AK	9/69	00045	A.K.			
AL	10/69	00049	A.K.			

SIZE	CODE	NUMBER	REV.
A	ML	KA10-A	AT
SCALE		SHEET 2 OF 8	DIST.

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D-BS-KA10-0-I0BC	A	1	I/O BUS CONTROL & I/O SELECTION
D-BS-KA10-0-I0BI	B	1	I/OB INPUTS
D-BS-KA10-0-I0T	A	1	IN-OUT TRANSFER CONTROL
D-BS-KA10-0-IR	A	1	INSTRUCTION REGISTER
D-BS-KA10-0-IR1	A	1	IR DECODING
D-BS-KA10-0-IR2	A	1	IR DECODING
D-BS-KA10-0-IR3		1	IR DECODING
D-BS-KA10-0-JFFO	A	1	JFFO INTRUCTION CONTROL
D-BS-KA10-0-KEY1		1	KEY & SWITCHES CONTROLS
D-BS-KA10-0-KEY2		1	KEY & SWITCHES CONTROLS
D-BS-KA10-0-KEY3		1	KEY & SWITCHES CONTROLS
D-BS-KA10-0-MA1	B	1	MA CONTROL
D-BS-KA10-0-MA2	A	1	MA REGISTER
D-BS-KA10-0-MAI	B	1	MEMORY ADDRESS INTERFACE
D-BS-KA10-0-MBDI		1	MEMORY BUS DATA INTERFACE
D-BS-KA10-0-MC1		1	MEMORY CONTROL
D-BS-KA10-0-MC2	A	1	MEMORY CONTROL
D-BS-KA10-0-MI		1	MEMORY INDICATOR
D-BS-KA10-0-MQ1	C	1	MQ CONTROL
D-BS-KA10-0-MQ2	A	1	MULTIPLIER QUOTIENT (MQ 0-17)

REVISIONS				DRN.	DATE	<b>digital</b> EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>	TITLE		
REV.	DATE	CHG. NO.	APP'D.	CHK'D	DATE				
AM	11/69	KA10-51	A.K.	<i>W. Stephenson</i>	3/67	KA10 PROCESSOR (60 HZ 115V)			
AN	1/70	KA10-58	A.K.	<i>W. Stephenson</i>	1/13/68				
AP	2/70	KA10-59	A.K.	<i>W. Stephenson</i>	1/25/68				
AR	2/70	KA10-60	A.K.	<i>W. Stephenson</i>	1/25/68				
AS	2/70	KA10-62	A.K.	<i>W. Stephenson</i>	1/25/68				
AT	3/70	KA10-63	A.K.	<i>W. Stephenson</i>	1-26-68				
FIRST USED ON						SIZE	CODE	NUMBER	REV.
SCALE						A	ML	KA10-A	AT
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D-BS-KA10-0-MQ3	B	1	MULTIPLIER QUOTIENT (MQ18-35)
D-BS-KA10-0-MR		1	MASTER CLEAR & POWER CLEAR
D-BS-KA10-0-NRNL	A	1	NORMALIZE RETURN & NR LONG
D-BS-KA10-0-PB		1	PARITY BUFFER REGISTER
D-BS-KA10-0-PC1	B	1	PROGRAM COUNTER CONTROL
D-BS-KA10-0-PC2	A	1	PROGRAM COUNTER REGISTER
D-BS-KA10-0-PI1		1	PI CONTROL
D-BS-KA10-0-PI2		1	PRIORITY INTERRUPT PIH,PIR,PIO
D-BS-KA10-0-PN		1	PARITY NETWORK
D-BS-KA10-0-PR	B	1	PROTECT REGISTER
D-BS-KA10-0-PTP1	A	1	PAPER TAPE PUNCH CONTROL 1
D-BS-KA10-0-PTP2	A	1	PAPER TAPE PUNCH CONTROL 2
D-BS-KA10-0-PTR1	B	1	PAPER TAPE READER CONTROL
D-BS-KA10-0-PTR2	B	1	PAPER TAPE READER CONTROL
D-BS-KA10-0-PTR3		1	PAPER TAPE READER CONTROL
D-BS-KA10-0-RL	B	1	RELOCATE REGISTER
D-BS-KA10-0-S1	B	1	STORE CYCLE TIME PULSES
D-BS-KA10-0-S2	B	1	STORE CYCLE LEVELS

REVISIONS				DRN.	DATE	<b>digital</b> EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>	TITLE		
REV.	DATE	CHG. NO.	APP'D.	CHK'D	DATE				
				<i>W. Stephenson</i>	3/67	KA10 PROCESSOR (60 HZ 115V)			
				<i>W. Stephenson</i>	1/13/68				
				<i>W. Stephenson</i>	1/25/68				
				<i>W. Stephenson</i>	1/25/68				
				<i>W. Stephenson</i>	1-26-68				
FIRST USED ON						SIZE	CODE	NUMBER	REV.
SCALE						A	ML	KA10-A	AT
SHEET 4 OF 8						DIST.			

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DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-BS-KA10-0-SC	A	1	SHIFT COUNT REGISTER
D-BS-KA10-0-SCAD		1	SHIFT COUNT ADDER
D-BS-KA10-0-SCC1		1	SHIFT COUNTER CONTROL
D-BS-KA10-0-SCC2	A	1	SHIFT COUNTER CONTROL
D-BS-KA10-0-SCSR	A	1	SHIFT & COUNT SUBROUTINE SHIFT INST
D-BS-KA10-0-TTY1	A	1	TELETYPE CONTROL
D-BS-KA10-0-TTY2	H	1	TELETYPE CONTROL
D-FD-KA10-0-BIF1	A	1	BASIC INSTRUCTION FLOW
D-FD-KA10-0-BIF2	A	1	BASIC INSTRUCTION FLOW
D-FD-KA10-0-BIF3	A	1	BASIC INSTRUCTION FLOW
D-FD-KA10-0-BIOR	A	1	BASIC I-O REGISTERS
D-FD-KA10-0-BYTF		1	BYTE INSTRUCTION FLOW
D-FD-KA10-0-DIVF	B	1	FIXED POINT DIVIDE & SUBROUTINE
D-FD-KA10-0-ESC	C	1	EXECUTE AND STORE CYCLE
D-FD-KA10-0-FAF	A	1	FLOATING ADD, SUB, UFA FLOW
D-FD-KA10-0-FC	A	1	FETCH CYCLE FLOW

REVISIONS				DRN. W. Stephenson 2/6	DATE 1/19/68	 <b>digital</b> CORPORATION <small>MAYNARD, MASSACHUSETTS</small>	<b>KA10 PROCESSOR</b> (60 HZ 115V)
REV.	DATE	CHG. NO.	APP'D.	CHK'D.	DATE		
				ENG. G. Katoh	DATE 18 JAN 68	TITLE	
				PROJ. ENG. R. Clements	DATE 18 JAN 68		
				PROD. G. Katoh	DATE 1-26-68		
				FIRST USED ON			
				SCALE		SIZE CODE	NUMBER
						A ML	KA10-A
							REV. AT
				SHEET 5	OF 8	DIST.	

DEC FORM NO. DRA 103

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### MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-FD-KA10-0-FDVF	C	1	FLOATING DIVIDE
D-FD-KA10-0-FPMC		1	FP EXP CALCULATE SUBR FM & MPY SUBR
D-FD-KA10-0-FSDN		1	FLOATING SCALE & DBL FLOATING NEGATE
D-FD-KA10-0-IAC	B	1	INSTRUCTION & ADDRESS CYCLES
D-FD-KA10-0-KO	C	1	KEY OPERATIONS FLOW DIAGRAM
D-FD-KA10-0-MCFM	C	1	MEMORY CONTROL & FAST MEMORY FLOW
D-FD-KA10-0-NRF	A	1	NORMALIZE RETURN SUBROUTINE
D-FD-KA10-0-PIF		1	PRIORITY INTERRUPT ISOLATED FLOW
D-FD-KA10-0-SCAF		1	SHIFT COUNT ACTION FLOW
D-FD-KA10-0-SMF	C	1	SHIFT & MUL & JFFO FLOW
D-FD-KA10-0-IOTF	A	1	IN-OUT TRANSFER CONTROL FLOW
D-FD-KA10-0-REG	A	1	KA10 REGISTER INTER-CONNECTIONS
D-FD-KA10-0-RIMF	B	1	READ-IN FUNCTION ISOLATED FLOW
D-FD-KA10-0-SCBT		1	SHIFT COUNT SUBROUTINE & BLT FLOW
D-IC-KA10-0-ICSC1	A	1	INDICATOR & CONSOLE SW CONNECTIONS
D-IC-KA10-0-ICSC2	A	1	INDICATOR & CONSOLE SW CONNECTIONS
D-CL-KA10-0-IBC1	A	1	INTER-BAY CABLES
D-CL-KA10-0-IBC2	B	1	INTER - BAY CABLES

REVISIONS				DRN. W. Stephenson 3/6	DATE 1/19/68	 <b>digital</b> CORPORATION <small>MAYNARD, MASSACHUSETTS</small>	<b>KA10 PROCESSOR</b> (60 HZ 115V)
REV.	DATE	CHG. NO.	APP'D.	CHK'D.	DATE		
				ENG. G. Katoh	DATE 18 JAN 68	TITLE	
				PROJ. ENG. R. Clements	DATE 18 JAN 68		
				PROD. G. Katoh	DATE 1-26-68		
				FIRST USED ON			
				SCALE		SIZE CODE	NUMBER
						A ML	KA10-A
							REV. AT
				SHEET 6	OF 8	DIST.	

DEC FORM NO. DRA 103

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MASTER DRAWING LIST			
DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-MU-KA10-0-1A1D	B	1	MODULE UTILIZATION PANELS 1A-1D
D-MU-KA10-0-1E1J	C	1	MODULE UTILIZATION PANELS 1E-1J
D-MU-KA10-0-1K1N	C	1	MODULE UTILIZATION PANELS 1K-1N
D-MU-KA10-0-1P1T	C	1	MODULE UTILIZATION PANELS 1P-1T
D-MU-KA10-0-2A2D		1	MODULE UTILIZATION PANELS 2A-2D
D-MU-KA10-0-2E2J	A	1	MODULE UTILIZATION PANELS 2E-2J
D-MU-KA10-0-2K2N	D	1	MODULE UTILIZATION PANELS 2K-2N
D-MU-KA10-0-2P2T	C	1	MODULE UTILIZATION PANELS 2P-2T
D-MU-KA10-0-3A3D	C	1	MODULE UTILIZATION PANELS 3A-3D
D-MU-KA10-0-3E3F	C	1	MODULE UTILIZATION PANELS 3E-3F
A-PL-KA10-0-MC	B	6	MODULE COUNT
A-CP-KA10-0-CP	F	6	EXTERNAL COMPONENT LIST
D-CL-KA10-0-TERM	D	1	PULSE & LEVEL TERMINATIONS BAY 1 & 2
D-IC-KA10-0-1	H	3	DC POWER WIRING
D-IC-KA10-0-2	C	3	AC POWER WIRING
D-AD-7005607-0-0	D		CABLE SET
D-DI-KA10-0-3	R	4	DRAWING INDEX LIST
K-WL-KA10-0-4	T		WIRE LIST KA10
A-WL-KA10-0-GW	A	1	TTY SOCKET WIRING OF KA10
A-WL-KA10-0-TWP1	F	17	TWP LIST KA10 BAY 1

REVISIONS				DRN.	DATE	digital CORPORATION MAYNARD, MASSACHUSETTS	TITLE
REV.	DATE	CHG. NO.	APP'D.	WAS	3/27/67		
							KA10 PROCESSOR (60 HZ 115V)
FIRST USED ON				SIZE	CODE	NUMBER	REV.
SCALE				A	ML	KA10-A	AT
SHEET 7 OF 8				DIST.			

DEC FORM NO. DRA 103

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MASTER DRAWING LIST			
DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-WL-KA10-0-TWP2	E	22	TWP LIST KA10 BAY 2
A-ML-KM10-0		1	FAST MEMORY
A-ML-KE10-0		1	EXTENDED INSTRUCTION SET
A-ML-KT10-0		1	TIME SHARING OPTION
A-ML-KT10A-0		1	TIME SHARING OPTION
A-WL-KA10-0-TWP3		1	TWP WIRE LIST BAY 3

REVISIONS				DRN.	DATE	digital CORPORATION MAYNARD, MASSACHUSETTS	TITLE
REV.	DATE	CHG. NO.	APP'D.	WAS	3/27/67		
							KA10 PROCESSOR (60 HZ 115V)
FIRST USED ON				SIZE	CODE	NUMBER	REV.
SCALE				A	ML	KA10-A	AT
SHEET 8 OF 8				DIST.			

DEC FORM NO. DRA 103





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MECHANICAL				MECHANICAL			
FIND NO.	DESCRIPTION	PART NO.	DEPT USAGE	FIND NO.	DESCRIPTION	PART NO.	DEPT USAGE
46	LOGIC FRAME ASSEMBLY BAY #1 LOGIC FRAME ASSY BAY #1 (P.L.) LOGIC FRAME 144 PIN CONNECTOR BLK MTG BAR MTG BAR SCOTCHCAL (CLR BACKGND, WHT LTR)	D-AD-7005354-0-0 A-PL-7005354-0-0 D-IA-7405584-0-0 D-MD-100095 D-IA-7405543-1-0 D-IA-7405543-2-0 A-SS-7406201-0-0		59	702A MARGINAL CHK POWER SUPPLY 702A MARG CHK POWER SUPPLY (P.L.) 702 MARGINAL CHK POWER SUPPLY 702 MARG CHK POWER SUPPLY (P.L.)	D-UA-702A-0-0 A-PL-702A-0-0 D-UA-702-0-8 A-PL-702-0-8	
47	LOGIC FRAME ASSEMBLY BAY #2 LOGIC FRAME ASSY BAY #2 (P.L.) LOGIC FRAME 144 PIN CONNECTOR BLK MTG BAR MTG BAR SCOTCHCAL (CLR BACKGND, WHT LTR)	D-AD-7005350-0-0 A-PL-7005350-0-0 D-IA-7405584-0-0 D-MD-100095 D-IA-7405543-1-0 D-IA-7405543-2-0 A-SS-7406200-0-0		60	FRONT DOOR ASSEMBLY BAY #3 FRONT DOOR ASSY BAY #3 (P.L.) DOOR FRAME HINGE PIN, TOP HINGE PIN, BOTTOM SPACER, DOOR	E-AD-7005355-0-0 A-PL-7005355-0-0 E-IA-7405725-0-0 B-MD-20400-7 B-MD-20400-8 B-MD-7405501-0-0	
48	LOGIC FRAME ASSEMBLY BAY #3 LOGIC FRAME ASSY BAY #3 (P.L.) LOGIC FRAME 144 PIN CONNECTOR BLOCK MTG BAR MTG BAR SCOTCHCAL (CLR BACKGND, WHT LTR)	D-AD-7005329-0-0 A-PL-7005329-0-0 D-IA-7405317-0-0 D-MD-100095 D-MD-7405543-2-0 D-MD-7405543-1-0 A-SS-7406199-0-0		61	PC09-A READER & PUNCH DWG INDEX	D-UA-PC09-A-0 D-DI-PC09-A-4	
49	FAN HOUSING ASSEMBLY BAY #3 FAN HOUSING ASSEMBLY BAY #3 FAN HOUSING ASSY BAY #3 (P.L.) FAN HOUSING, LOGIC DOOR MTG PLATE, FAN HOUSING SCREEN, FAN PROTECTION COVER BOTTOM PLATE, FAN HOUSING	D-AD-7005346-1-0 D-AD-7005346-2-0 A-PL-7005346-0-0 E-IA-7405661-0-0 C-MD-7405663-0-0 C-MD-7404881-0-0 B-MD-5303154-0-0 C-IA-7405665-0-0		62	SWITCH INTERLOCK ASSEMBLY SWITCH INTERLOCK ASSY (PL) PLATE CONNECTOR <del>PLATE STRIPPER</del> COVER	C-MD-7005683-0-0 A-PL-7005683-0-0 B-IA-7406415-0-0 <del>C-MD-7406413-0-0</del> B-MD-7406413-0-0	
50	MARG CHK & MAINT PANEL ASSEMBLY MARG CHK & MAINT PANEL ASSEMBLY MARG CHK & MAINT PANEL ASSEMBLY MARG CHK & MAINT PNL ASSY (PL)	E-AD-7005352-1-0 E-AD-7005352-2-0 E-AD-7005352-3-0 A-PL-7005352-0-0		63	MAINT SWITCH BRKT (ASSY) MAINT SWITCH BRKT (ASSY) (PL) BRKT, MAINT SWITCH DECAL	C-MD-7005675-0-0 A-PL-7005675-0-0 C-MD-7406397-0-0 A-DC-7406404-0-0	
51	CHECK PANEL MAINT & MARGINAL SILK SCREEN (SEE NOTE #2)	D-IA-7405692-0-0 C-SS-7405428-0-0		64	703 POWER SUPPLY 703 POWER SUPPLY (PL)	D-UA-703-0-0 A-PL-703-0-0	
52	PANEL (CONN) MARG CHECK CONT PANEL (CONN) MARG CHK CONT	C-IA-7405697-0-0 B-SS-7405776-0-0		65	846 OVER VOLTAGE PROTECTOR	D-UA-846-0-0	
53	SWITCH BOARD ASSY (MARG CHK & MAINT) 18 PIN RECEPTACLE REWORK SPACER BAR ROCKER TO SW (PEACOCK BLU) ROCKER TO SW (CHK BLU)	C-IA-5404051-0-0 B-MD-5503954-0-0 B-MD-7405509-0-0 C-AD-5404424-2-0 C-AD-5404424-1-0		50	SWITCH REWORK PHENOLIC BOARD METER REWORK (HOBBS)(240V 50 HZ) METER REWORK (HOBBS)(115V 60 HZ) METER REWORK (HOBBS)(115V 50 HZ)	B-MD-7405975-0-0 C-MD-7406490-0-0 B-MD-7406249-1-0 B-MD-7406249-2-0 B-MD-7406249-3-0	
54	SWITCH BOARD, MARG CHK & MAINT BOARD GLASS EPOXY, BLANK	C-IA-5004034-0-0 D-MD-1402230-0-0		CONT.	DECALS KAIO	A-DC-7406473-0-0	
55	HEAT SWITCH ASSEMBLY HEAT SWITCH ASSY (P.L.) RETAINER BRACKET, SIDE COVER INSULATING WASHER	C-AD-7005510-0-0 A-PL-7005510-0-0 C-MD-7406108-0-0 B-IA-7406108-0-0 B-MD-7406107-0-0 B-MD-7407546-0-0			CABLE HARNESS, DC BAY 1 CABLE HARNESS, DC BAY 2 CABLE HARNESS, DC BAY 3 CABLE HARNESS, AC BAY 3 MARGINAL CHECK CABLE BAY 3	J-IA-7006164-0-0 J-IA-7006165-0-0 J-IA-7006166-0-0 J-IA-7006168-0-0 J-IA-7006169-0-0	
56	728 POWER SUPPLY 728 POWER SUPPLY (P.L.) 729A POWER SUPPLY 729A POWER SUPPLY (P.L.)	D-MA-728-0-1 A-PL-728-0-1 D-MA-728A-0-1 A-PL-728A-0-1					
57	779 POWER SUPPLY 779 POWER SUPPLY (P.L.) 779A POWER SUPPLY 779A POWER SUPPLY (P.L.)	D-MA-779-0-1 A-PL-779-0-1 D-MA-779A-0-1 A-PL-779A-0-1					
58	778 POWER SUPPLY 778 POWER SUPPLY (P.L.) 778A POWER SUPPLY 778A POWER SUPPLY (P.L.)	D-MA-778-0-1 A-PL-778-0-1 D-MA-778A-0-1 A-PL-778A-0-1					

REV	NO	DATE	BY
CHK	CHANGE		

UNLESS OTHERWISE SPECIFIED		DWN <i>M. L. Dow</i> DATE <i>9/16/67</i>	
DIMENSION IN INCHES		CHK'D. <i>H. Stone</i> DATE <i>9-18-67</i>	
TOLERANCES		ENG. <i>H. Stone</i> DATE <i>9-22-67</i>	
DECIMALS	FRACTIONS	ANGLES	DATE
= .005	= 1/64	= 0°30'	
FINAL SURFACE QUALITY		PROJ. ENGR. <i>H. Stone</i> DATE <i>9/22/67</i>	
REMOVE BURRS AND BREAK SHARP CORNERS		PRD'D. <i>H. Stone</i> DATE <i>9/22/67</i>	
MATERIAL		FIRST USED ON	
FINISH		SCALE NONE	
		SHEET 3 OF 4	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TITLE DWG INDEX LIST KAIO	
SIZE CODE	NUMBER
D I KAIO - 0 - 3	CR
DIST. G	



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ELECTRICAL					ELECTRICAL					ELECTRICAL																																																																																																																																					
FIND NO.	DESCRIPTION	PART NO.	DEPT	USAGE	FIND NO.	DESCRIPTION	PART NO.	DEPT	USAGE	FIND NO.	DESCRIPTION	PART NO.	DEPT	USAGE																																																																																																																																	
			PROD	CUST	F/C																																																																																																																																										
1	KA10 (50 HZ 115V) KA10 (50 HZ 220V) ADDER CONTROL FLIP-FLOP ADDER CONTROL ADDER LEFT HALF ADDER RIGHT HALF AR INPUTS AR REGISTER AR REGISTER AR REGISTER AR REGISTER AR CONTROL PULSE AR CONTROL PULSE AR CONTROL PULSE ARITHMETIC FLAGS AR & MQ SHIFT CONNECTIONS ADDRESS SWITCH COMPARATORS BR CONTROL BR REGISTER BLOCK TRANSFER AND MULTIPLY BYTE INSTRUCTION FIRST PART ARITHMETIC PROCESSOR STATUS REG BYTE DEPOSIT AND LOAD DIVIDE SUBROUTINE & FIXED DIVIDE EXECUTION CYCLE EXECUTIVE CONTROL FETCH CYCLE TIME PULSE FETCH CYCLE LEVELS FLOATING ADD INSTRUCTIONS FLOATING DIVIDE FLOATING EXPONENT REG & CONTROL FAST MEMORY FAST MEMORY ADDRESS FP EXP CALC FLOATING MULTIPLY HALF WORD TRANSFER INSTRUCTION & ADDRESS CYCLES I/O BUS (#-17) I/O BUS (18-35) I/O BUS CONTROL & I/O SELECTION IOB INPUTS IN-OUT TRANSFER CONTROL INSTRUCTION REGISTER IR DECODING IR DECODING IR DECODING KEY & SWITCHES CONTROLS KEY & SWITCHES CONTROLS KEY & SWITCHES CONTROLS MA CONTROL MA REGISTER MEMORY ADDRESS INTERFACE MEMORY BUS DATA INTERFACE MEMORY CONTROL MEMORY CONTROL MQ CONTROL MULTIPLIER QUOTIENT (MQ8-17) MULTIPLIER QUOTIENT (MQ18-35) MASTER CLEAR & POWER CLEAR NORMALIZE RETURN & NR LONG PARITY BUFFER REGISTER PROGRAM COUNTER CONTROL PROGRAM COUNTER REGISTER PI CONTROL PRIORITY INTERRUPT PIH, PIR, PIO PARITY NETWORK PROJECT REGISTER PAPER TAPE PUNCH CONTROL 1 PAPER TAPE PUNCH CONTROL 2 PAPER TAPE READER CONTROL PAPER TAPE READER CONTROL PAPER TAPE READER CONTROL RELOCATE REGISTER STORE CYCLE TIME PULSES STORE CYCLE LEVELS SHIFT COUNT REGISTER SHIFT COUNT ADDER SHIFT COUNTER CONTROL SHIFT COUNTER CONTROL SHIFT & CNT SUBROUTINE TELETYPE CONTROL TELETYPE CONTROL BASIC INSTRUCTION FLOW BASIC INSTRUCTION FLOW BASIC INSTRUCTION FLOW BASIC I/O REGISTERS BYTE INSTRUCTION FLOW	A-WL-KA10-A A-WL-KA10-B A-WL-KA10-C D-BS-KA10-C-AD1 D-BS-KA10-C-AD2 D-BS-KA10-C-AD3 D-BS-KA10-C-AD4 D-BS-KA10-C-ARI D-BS-KA10-C-AR1 D-BS-KA10-C-AR2 D-BS-KA10-C-AR3 D-BS-KA10-C-AR4 D-BS-KA10-C-ARC1 D-BS-KA10-C-ARC2 D-BS-KA10-C-ARC3 D-BS-KA10-C-ARF D-BS-KA10-C-ARMQ D-BS-KA10-C-AS D-BS-KA10-C-BR1 D-BS-KA10-C-BR2 D-BS-KA10-C-BTMP D-BS-KA10-C-BYTE D-BS-KA10-C-CPA D-BS-KA10-C-DBLB D-BS-KA10-C-DSDV D-BS-KA10-C-E D-BS-KA10-C-EX D-BS-KA10-C-F1 D-BS-KA10-C-F2 D-BS-KA10-C-FA D-BS-KA10-C-FDV D-BS-KA10-C-FE D-BS-KA10-C-FM D-BS-KA10-C-FMA D-BS-KA10-C-FPFM D-BS-KA10-C-HWT D-BS-KA10-C-IA D-BS-KA10-C-IOB1 D-BS-KA10-C-IOB2 D-BS-KA10-C-IOBC D-BS-KA10-C-IOBI D-BS-KA10-C-IOT D-BS-KA10-C-IR D-BS-KA10-C-IR1 D-BS-KA10-C-IR2 D-BS-KA10-C-IR3 D-BS-KA10-C-KEY1 D-BS-KA10-C-KEY2 D-BS-KA10-C-KEY3 D-BS-KA10-C-MA1 D-BS-KA10-C-MA2 D-BS-KA10-C-MAI D-BS-KA10-C-MBD1 D-BS-KA10-C-MC1 D-BS-KA10-C-MC2 D-BS-KA10-C-MQ1 D-BS-KA10-C-MQ2 D-BS-KA10-C-MQ3 D-BS-KA10-C-MR D-BS-KA10-C-NRNL D-BS-KA10-C-PB D-BS-KA10-C-PC1 D-BS-KA10-C-PC2 D-BS-KA10-C-PC1 D-BS-KA10-C-PC2 D-BS-KA10-C-PI1 D-BS-KA10-C-PI2 D-BS-KA10-C-PN D-BS-KA10-C-PR D-BS-KA10-C-PTP1 D-BS-KA10-C-PTP2 D-BS-KA10-C-PTR1 D-BS-KA10-C-PTR2 D-BS-KA10-C-PTR3 D-BS-KA10-C-RL D-BS-KA10-C-S1 D-BS-KA10-C-S2 D-BS-KA10-C-SC D-BS-KA10-C-SCAD D-BS-KA10-C-SCC1 D-BS-KA10-C-SCC2 D-BS-KA10-C-SCSR D-BS-KA10-C-TTV1 D-BS-KA10-C-TTV2 D-FD-KA10-D-BIF1 D-FD-KA10-D-BIF2 D-FD-KA10-D-BIF3 D-FD-KA10-D-BIOR D-FD-KA10-D-BYTF				1	FIXED POINT DIVIDE & SUBROUTINE EXECUTE & STORE CYCLE FLOATING ADD, SUB & UFA FLOW FETCH CYCLE FLOW FLOATING DIVIDE FP EXP CAL SUBR FM & MPY SUBR INSTRUCTION & ADDRESS CYCLE KEY OPERATIONS FLOW DIAGRAM MEMORY CONTROL & FAST MEM FLOW NORMALIZE RETURN SUBROUTINE PDP-10 REGISTER ORGANIZATION SHIFT COUNT ACTION FLOW SHIFT & MUL FLOW IN-OUT TRANSFER CONTROL FLOW READ-IN FUNCTION ISOLATED FLOW SHIFT CNT SUBROUTINE & BLT FLOW INDICATOR & CONSOLE SW CONN INDICATOR & CONSOLE SW CONN INTER-BAY CABLES INTER-BAY CABLES MODULE UTILIZATION PNL 1A-1D MODULE UTILIZATION PNL 1E-1J MODULE UTILIZATION PNL 1K-1N MODULE UTILIZATION PNL 1P-1T MODULE UTILIZATION PNL 2A-2D MODULE UTILIZATION PNL 2E-2J MODULE UTILIZATION PNL 2K-2N MODULE UTILIZATION PNL 2P-2T MODULE UTILIZATION PNL 3A-3D MODULE UTILIZATION PNL 3E-3F PULSE & LEVEL TERMS BAY 1 & 2 PDP-10 PROCESSOR LAYOUT DC POWER WIRING AC POWER WIRING MEMORY INDICATOR FLOAT SCALE & DBL FLOAT NEG PRIORITY INT ISOLATED FLOW	D-FD-KA10-D-DIVF D-FD-KA10-D-ESC D-FD-KA10-D-FAF D-FD-KA10-D-FC D-FD-KA10-D-FDVF D-FD-KA10-D-FPMC D-FD-KA10-D-IAC D-FD-KA10-D-KD D-FD-KA10-D-MCFM D-FD-KA10-D-NRF D-FD-KA10-D-REG D-FD-KA10-D-SCAF D-FD-KA10-D-SMF D-FD-KA10-D-IOTF D-FD-KA10-D-RIMP D-FD-KA10-D-SCBT D-IC-KA10-D-ICSC1 D-IC-KA10-D-ICSC2 D-IC-KA10-D-IBC1 D-IC-KA10-D-IBC2 D-MW-KA10-D-1A4D D-MW-KA10-D-1E1J D-MW-KA10-D-1KH D-MW-KA10-D-1P4T D-MW-KA10-D-2A2D D-MW-KA10-D-2E2J D-MW-KA10-D-2K2N D-MW-KA10-D-2P2T D-MW-KA10-D-3A3D D-MW-KA10-D-3E3F D-IC-KA10-D-TERM D-IC-KA10-D-PRL D-IC-KA10-D-1 D-IC-KA10-D-2 D-BS-KA10-D-1A4D D-BS-KA10-D-FSDN D-FD-KA10-O-PIF				41	LIGHT BOARD ASSEMBLY CIRCUIT SCHEMATIC	D-IA-5404029-0-0 B-CS-5404029-0-1				46	LOGIC FRAME ASSY BAY #1 WIRE LIST KA10	D-AD-7005354-0-0 K-WL-KA10-0-4				47	LOGIC FRAME ASSEMBLY BAY #2 WIRE LIST KA10	D-AD-7005350-0-0 K-WL-KA10-0-4				48	LOGIC FRAME ASSEMBLY BAY #3 WIRE LIST KA10	D-AD-7005329-0-0 K-WL-KA10-0-4				49	FAN HOUSING ASSEMBLY BAY #3	D-AD-7005346-0-0				50	MARGINAL CHK & MAINT PANEL	E-AD-7005352-0-0				53	SWITCH BOARD ASSEMBLY CIRCUIT SCHEMATIC	C-IA-5404051-0-0 B-CS-5404051-0-3				55	HEAT SWITCH ASSEMBLY	C-AD-7005510-0-0				62	SWITCH INTERLOCK ASSEMBLY	C-AD-7005683-0-0				1 CONT	MODULE COUNT EXTERNAL COMPONENTS LIST TWP LIST KA10 BAY 1 TWP LIST KA10 BAY 2 FAST MEMORY EXTENDED INSTRUCTION SET TIME SHARING OPTION TWP LIST KA10 BAY 3	A-PI-KA10-D-WC A-WL-KA10-D-EW A-WL-KA10-D-TWP1 A-WL-KA10-D-TWP2 A-WL-KM10-D-0 A-WL-KE10-D-0 A-WL-KT10-D-0 A-WL-KA10-TWP-3				11	BLOWER ASSEMBLY	D-AD-7005363-0-0				12	MARGINAL CHECK ASSY BAY #1	E-AD-7005378-0-0				14	MARG CHK SW BOARD ASSEMBLY #1 CIRCUIT SCHEMATIC	C-IA-5404110-0-0 B-CS-5404110-0-1				16	MARGINAL CHECK ASSEMBLY BAY #2	E-AD-7005377-0-0				18	MARGINAL CHECK ASSEMBLY BAY #3	E-AD-7005348-0-0				20	MARG CHK SW BOARD ASSEMBLY #2 CIRCUIT SCHEMATIC	C-IA-5404113-0-0 B-CS-5404113-0-1				23	CONTROL LIGHT PANEL #1 CIRCUIT SCHEMATIC	D-AD-5404031-0-0 B-CS-5404031-0-1				25	CONTROL LIGHT PANEL #2 CIRCUIT SCHEMATIC	D-AD-5404030-0-0 B-CS-5404030-0-1				27	SWITCH BOARD ASSEMBLY #1 CIRCUIT SCHEMATIC	C-IA-5404010-0-0 B-CS-5404010-0-2				29	SWITCH BOARD ASSEMBLY #2 CIRCUIT SCHEMATIC	D-IA-5404012-0-0 B-CS-5404012-0-1				31	SWITCH BOARD ASSEMBLY #4 CIRCUIT SCHEMATIC	D-IA-5404023-0-0 B-CS-5404023-0-1				35	FAN HOUSING ASSEMBLY, PLENUM	E-AD-7005269-0-0			

REV.	NO.	DATE
CHK		

DEC FORM NO. DRD 102

DO NOT SCALE DRAWING	DRN	DATE	3/18/67
UNLESS OTHERWISE SPECIFIED	DRK	DATE	3/18/67
DIMENSION IN INCHES	ENG	DATE	3/18/67
TOLERANCES	PROJ	DATE	3/18/67
DECIMALS FRACTIONS ANGLES	PRD	DATE	3/18/67
± .005 ± 1/64 ± .030			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			

PARTS LIST	
QTY.	DESCRIPTION
PARTS LIST	
QTY.	DESCRIPTION
PARTS LIST	
QTY.	DESCRIPTION

SCALE NONE SHEET 4 OF 4

DIST. G

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INSTRUCTION	BOOLE	ADD SUBTRACT	FWT	HWT -HLR(-) HRL(I)	HWT HLR(-) HRL(I)	EXCH	UUO
INITIAL SWITCHES	BOOLE 2,10,13,16: E LONG BOOLE 0,3,14,17: FAC INH BOOLE A-(0,5,12,17)XXX <sup>M</sup> : FCE BOOLE A-(0,5,12,17)XXX <sup>B</sup> : FCE PSE	EF 0 LONG XXX <sup>M</sup> : FCE XXX <sup>B</sup> : FCE PSE	MOV <sup>M</sup> X: EF 0 LONG MOV <sup>S</sup> X: FAC INH MOVX <sup>M</sup> : FCE MOVX <sup>S</sup> : FCE PSE		0 - HXXXSVHXXZ: FAC INH ES HXXX <sup>M</sup> : FCE HXXXSVHXX-M: FCE PSE	FCE PSE	FAC INH PC+1 INH
INITIAL REGISTERS	AR: C(AC) or Z BR: (0, E) or C(E) MA: E	AR: C(AC) BR: (0, E) or C(E) MA: E	AR: C(AC) or (0, E) or C(E) BR: (0, E) or C(E) MA: E	AR: C(AC) or (0, E) or C(E) BR: (0, E) or C(E) NOTE: IF HWT IS F(1 OPERAND), OPERAND IS IN AR. IF TWO OPERANDS, MEM IS IN BR, AC IS IN AR	AR: C(AC) BR: C(E) or (0, E)	AR: C(AC) BR: C(E)	MA: 0 AR: 0, E IR: INST
FT9	BOOLE 6,11,12,17: AD AR-EN SET BOOLE 1,6,7,10,16: AD BR+EN SET BOOLE 2,9,11,13,14,15: AD BR-EN SET BOOLE 6,11: AD CRY INS SET	AD AR+EN SET ADDX: AD BR+EN SET SUBX: AD BR-EN SET AD CRY 36 SET	MOV <sup>M</sup> X: AD AR NEGATE		AD BR+EN SET HXXOXVHXXE: AD BR±EN	AD BR+EN SET	
ET0	BOOLE 0,6,11,12,14: AR FM AD(J) BOOLE 1,9,13,16: AR FM AD(J) BOOLE 2,7,10,15,17: AR FM AD(J)	AR FM AD(J) ARF CRY STB	MOVX: AR SWAP MOVXV (MOVX A AR0(1)): AR FM AD(J) ARF CRY STB	HLRXX: ARRT FM ARLT(J) HRLXX: ARLT FM ARRT(J) HXLOV(HXLEX A HWT E TEST) VHXL-MVHXR-: ARRT FM AD(J) HXROXV(HXREX A HWT E TEST) VHXR-MVHXL-: ARLT FM AD(J) HXLZXV(HXLEX A-HWT E TEST): ARRT CLR HXRXV(HXREX A-HWT E TEST): ARLT CLR	AR FM AD(J) BR FM AR(J) AD BR+ ONLY EN	AR FM AD(J) BR FM AR(J)	ARLT FM IR0-12(R) MA30 SET IR2(I) VIR3(I): EX ILL OP SET EXCTF SET EUUOF SET IR1XX: MA31 SET
ET1	AD CRY INS CLR AD AR-EN SET AD BR+EN CLR AD BR-EN CLR						HLRXX: ARRT FM ARLT(J) HRLXX: ARLT FM ARRT(J) HXRXX: ARLT FM AD(J) HXLXX: ARRT FM AD(J)
ET2	AR FM AD(J)						
FINAL SWITCHES	XXX <sup>M</sup> : SAC INH XXX <sup>A</sup> : FCE PSE: SCE B	XXX <sup>M</sup> : SAC INH	MOVX <sup>M</sup> : SCE MOVX <sup>A</sup> AC(0) VMOVX <sup>M</sup> : SAC INH		(HXXXS A AC=0) V HXXX <sup>M</sup> : SAC INH 0 HXXX <sup>M</sup> : SCE E	SAR+BR	SCE SAC INH

BOOLE #	MNEMONIC
0	SET Z
1	AND
2	ANDCA
3	SETM
4	ANDCM
5	SETA
6	XOR
7	IOR
10	ANDCB
11	EQV
12	SETCA
13	ORCA
14	SETCM
15	ORCM
16	ORCB
17	SETO

NOTES:  
 1. UUO=(IR JRTA A-EX ALLOW IOTS A IR9(1)) V (IR JRTA A-EX ALLOW IOTS A IR10(1)) \* OPEN IR2(0) FROM TERM TO DISABLE FLOATING POINT HARDWARE  
 V (IR IOT A A-EX ALLOW IOTS A EX PI SYNC(0)) V (IR 0(0) A IR1(0) A IR2(0)) V IR 10-12 7  
 2. FLAGS: 0) AR OV FLAG 6) EX IOT USER (CANNOT BE TURNED ON IN USER MODE)  
 1) AR CRY 0 FLAG 7)  
 2) AR CRY 1 FLAG 8)  
 3) AR FOV 9)  
 4) BYFG 10)  
 5) EX USER (SAVED) 11) AR FNU  
 EX MODE SYNC (RESTORE) 12) AR DCK  
 3. AR OV COND=(AD CRY 0(0) A AD CRY 1(1)) V (AD CRY 0(1) A AD CRY 1(0))  
 4. HWT E TEST=(IR3(0) A IRG(0) A AR0(1)) V (IR3(1) A IRG(1) A AR0(2)) V (IR3(0) A IRG(1) A AR18(1)) V (IR3(1) A IRG(0) A AR18(1))  
 5. ARF CRY STB 1) AR OV COND: AR OV FLAG SET  
 1) AD CRY 0(1): AR CRY 0 FLAG SET  
 1) AD CRY 1(1): AR CRY 1 FLAG SET

REVISIONS	CHK	CHANGE NO.	REV.
		1	A
		2	B
		3	C
		4	D
		5	E
		6	F
		7	G
		8	H
		9	I
		10	J
		11	K
		12	L
		13	M
		14	N
		15	O
		16	P
		17	Q

UNLESS OTHERWISE SPECIFIED	DRN.	DATE	11-10-66
UNLESS OTHERWISE SPECIFIED	CHKD.	DATE	1-16-69
DIMENSION IN INCHES	ENG.	DATE	7-27-68
TOLERANCES	PROL-ENG.	DATE	1-7-68
DECIMALS FRACTIONS ANGLES	PROD.	DATE	1-19-68
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			

digital EQUIPMENT CORPORATION  
 MAYNARD, MASSACHUSETTS

TITLE  
**BASIC INSTRUCTION FLOW**

SIZE CODE NUMBER REV.  
 DFDKAI0-0-BIFI A

SHEET OF DIST.

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INSTRUCTION	JSR	JSP	JSA AC FM (E, PC) E FM C(PC) PC FM E+1	JRA AC FM C(C(ACLT)) PC FME	JFCL	JRST	TEST	AOBJX
INITIAL SWITCHES	FAC INH E LONG	FAC INH	E LONG	FCC ACLK E LONG	FAC INH	FAC INH IR 10 (1): E LONG	TDXX: FCE TSXX: FCE E LONG	EF 0 LONG
INITIAL REGISTERS	AR; 0, E BR; 0, E MA; E	MA; E	AR; C(AC) BR; 0, E MA; E	AR; AC SWAPPED BR; 0, E MQ; C(C(ACLT)) MA; C(ACLT)	MA; E	MA; E BR; LAST MEM REF (FLAGS LT HALF)	AR; C(AC) BR; 0, E) C(E); MASK	AR; C(AC) MA; E
FT9			AD BR+EN	AD BR+EN			TXOX: AD BR+EN SET TXCX: AD AR+EN SET TXC X: AD BR-EN SET TXCX: AD CRY INS SET	AD AR+EN SET AD+1 BOTH
ET 0	PC FM MA(J) ARLT FM PC(J) ARLT FM FLAGS(J) BYF6 CLR	PC FM MA(J) ARLT FM PC(J) ARLT FM FLAGS(J) BYF6 CLR	ARLT FM PC(J); PC BE FM AR(J); C(AC) PC FM MA(J); E	AR FM AD(J); 0, E	CONDITION 2: PC FM MA(J) IR9(1): AR OV CLR IR10(1): AR CRY 0 CLR IR11(1): AR CRY 1 CLR IR12(1): AR FOV CLR	AR FM PC(J) PC FM MA(J) IR12(1): EX MODE SYNC SET IR11(1): ARF FLAGS FM BR(J) IR9(1): PLOK CLEARS PIH IR10(1): RUN CLR	T S XX: AR SWAP	AR FM AD(J) (ARBJN/AD 0(1)): PC FM MA(J) (ARBJP/AD 0(2)): PC FM MA(J)
ET 1	NOTE 3	NOTE 3	NOTE 3	ARLT FM ARLT(J); PC ARLT FM PC(J); E	MA FM AR(J); E AR FM MQ(J); C(C(ACLT))	MA FM AR (J)	AD CRY INS CLR BE FM AR(0) TXC X: AR FM AD(1) TXC X: AR FM AD(0) AD BR-EN CLR AD BR+EN SET AD AR+EN CLR	
ET 2	PC+1; E+1		PC+1; E+1 AR SWAP	PC FM MA(J); E			T S XX: AR SWAP L TXXAV(TXXE/AD=0)V (TXXN/AD#0): PC+1	
FINAL SWITCHES	SCE SAC INH		SAR+BR		SAC INH	SAC INH	TXNX: SAC INH	

NOTES:  
 1. CONDITION 2 = (IR9(2) AND AR OV(1)) V (IR10(2) AND AR CRY 0 FLAG(1)) V (IR11(1) AND AR CRY 1 FLAG(1)) V (IR12(1) AND AR FOV(1))  
 2. FLAGS: 0) AR OV FLAG 7) EX IOT USER (CANNOT BE TURNED ON IN USER MODE)  
 1) AR CRY 0 FLAG 8)  
 2) AR CRY 1 FLAG 9)  
 3) AR FOV 10)  
 4) BYF6 11) AR FXU  
 5) EX USER (SAVED) 12) AR DCK  
 EX MODE SYNC (RESTORE)  
 3. EX TRAP COND= EX PI SYNC (N) V EX ILL (OP 0)  
 EX TRAP CONDA ET 0 DEL A (JSR, JSP, JSA, JRST, PUSH J): CLEAR EX USER

REV. A	DATE 11-11-66
REV. B	DATE 1-16-68
REV. C	DATE 1-27-68
REV. D	DATE 1-27-69
REV. E	DATE 1-19-68

DEC FORM NO. 144

UNLESS OTHERWISE SPECIFIED	DRN	DATE	11-11-66
UNLESS OTHERWISE SPECIFIED	CHRD	DATE	1-16-68
DIMENSION IN INCHES	ENG	DATE	1-27-68
TOLERANCES	PROJ. ENG.	DATE	1-27-69
DECIMALS ± .005	PROD.	DATE	1-19-68
FRACTIONS ± 1/64			
ANGLES ± 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			

digital EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

TITLE  
**BASIC INSTRUCTION FLOW**

SIZE CODE NUMBER REV.  
D FDKA10-0-BIF2 A

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INSTRUCTION	SKIP AOSX SKIPX SOSX	JUMP A0JX JUMPX SOJX	CAM CAI	PUSH	PUSH J	POP	POPJ	XCT
INITIAL SWITCHES	EFØ LONG YOSX:FCE PSE SKIPX:FCE FACINH	EFØ LONG	EFØ LONG CAMX:FCE	EFØ LONG FCE E LONG	EFØ LONG E LONG	EFØ LONG FCC ACET E LONG		FACINH PC+1, INH
INITIAL REGISTERS	AR;C(E)	AR;C(AC) MA;E	AR;C(AC) BR;Ø,E) OR C(E)	AR;C(AC) BR;C(E) MA;E	AR;C(AC) BR;E MA;E MQ;Ø	AR;C(AC) BR;Ø,E) MQ;C(ACRT) MA;C(ACET)		MA;E
FT9	AD AR+EN SET AOXX:CRY36 SOXX:AD BR+EN SET AD BR-EN SET		AD MINUS BR AD AR+EN SET		AD AR+EN SET AD CRY 36 SET AD+1 LH SET		AD AR+EN SET AD BR+EN AD-1 LH SET	
ETØ	AR FM AD(J) PC COND PV PC COND R:PC+1	AR FM AD(J) PC COND PV PC COND R:PC FM MA(J)	AR FM AD(J) PC COND PV PC COND Q:PC+1	AR FM AD(J) AD CRY Ø: CPA PDL OV SET	AR FM PC FLAGS(J) MQ FM AD(J) PC FM MA(J) AD CRY Ø: CPA PDL OV SET BYF6 CLR NOTE 4	MQ FM AD(J) AR FM MQ(J) -AD CRY Ø:CPA PDL OV SET AD BR+ ONLY EN		EXCTF SET
ET1				MA FM AR(J)	BR FM AR(J) AR FM MQ(J)	AR FM AD(J) BR FM AR(J)	MA FM AR(J) AR FM MQ(J)	
ET2					MA FM AR(J)	MA FM AR(J) AR FM MQ(J)	PC FM MA(J)	
FINAL SWITCHES	AC=Ø: SAC INH	JUMPX:SAC INH	SAC INH	SAR+BR	SAR+BR	SAR+BR		SAC INH

NOTES:  
 1. PC COND P = (IR6(Ø) AND Ø AND IR7(1)) V (IR6(1) AND IR7(Ø) AND IR8(Ø)) V (IR6(2) AND AD=Ø AND IR8(Ø))  
 PC COND Q = (IR6(Ø) AND COND AND IR8(1)) V (IR6(1) AND IR7(Ø) AND AD COND) V (IR6(2) AND AD=Ø AND AD COND)  
 PC COND R = (IR6(Ø) AND IR8(Ø) AND Ø(1)) V (IR6(1) AND IR7(Ø) AND AD(Ø)) V (IR6(2) AND AD=Ø AND AD(Ø))  
 2. AR OV COND = (AD CRY Ø(Ø) AND AD CRY 1(1)) V (AD CRY Ø(1) AND AD CRY 1(Ø))  
 3. AD COND = (AD Ø(1) AND CRY Ø(1) AND CRY 1(1)) V (AD Ø(2) AND CRY Ø(Ø) AND CRY 1(Ø)) V (AD Ø(Ø) AND CRY Ø(1) AND CRY 1(Ø))  
 V (AD Ø(Ø) AND CRY Ø(Ø) AND CRY 1(1))  
 4. EX TRAP COND = EX PI SYNC (1) V EX ILL OP(Ø)  
 EX TRAP COND AND ETØ DEL AND (JSR, JSP, JSA, JRST, PUSHJ): CLEAR EX USER

REVISIONS	CHANGE NO.	REV.
CHK	1	A
DATE	1-14-68	
BY	R. W. KENT	
DATE	1-14-68	

UNLESS OTHERWISE SPECIFIED	DRN	DATE	11-14-66
UNLESS OTHERWISE SPECIFIED	CHKD	DATE	1-14-68
DIMENSION IN INCHES	ENG	DATE	1-14-68
TOLERANCES	PROL ENG	DATE	1-14-68
DECIMALS FRACTIONS ANGLES	PROD	DATE	1-14-68
± .005 ± 1/64 ± 0'30"			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			

digital EQUIPMENT CORPORATION  
 BATHURST, MASSACHUSETTS

TITLE: BASIC INSTRUCTION FLOW

SCALE: DIST. OF

SIZE CODE: NUMBER: DFDKAIØ-Ø-BIF3 REV. A

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DEVICE NAME	ABBREV	DEV#	FUNCTION	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	DATA/DATAO ACTIONS	
PROCESSOR	CPA	000	CONO	CPA PDL OV CLR	CPA IOB RESET	—	CPA ADR BREAK CLR	CPA MEM PROT FLAG CLR	CPA NON-EX MEM CLR	CPA CLK EN SET	CPA CLK EN SET	CPA CLK FLAG CLR	CPA FOV EN CLR	CPA FOV EN SET	CPA FOV EN SET	CPA MA TRAP OFFSET	CPA AR OV EN(1)	CPA AR OV (1)	CPA PIA 33	CPA PIA 34	CPA PIA 35	NONE	
			CONI	—	CPA PDL OV (1)	EX IOT USER(1)	—	CPA ADR BREAK (1)	CPA MEM PROT FLAG(1)	CPA NON-EX MEM(1)	—	CPA CLK EN (1)	CPA CLK FLAG(1)	—	CPA FOV EN (1)	CPA FOV(1)	—	—	—	CPA PIA 33	CPA PIA 34	CPA PIA 35	NONE
			DATAO LEFT HALF	RL18	RL19	RL20	RL21	RL22	RL23	RL24	RL25	—	—	—	—	—	—	—	—	—	—	—	—
DATAI LEFT / RIGHT	DS0 / DS18	DS1 / DS19	DS2 / DS20	DS3 / DS21	DS4 / DS22	DS5 / DS23	DS6 / DS24	DS7 / DS25	DS8 / DS26	DS9 / DS27	DS10 / DS28	DS11 / DS29	DS12 / DS30	DS13 / DS31	DS14 / DS32	DS15 / DS33	DS16 / DS34	DS17 / DS35	—	—	—	—	
PRIORITY INTERRUPT SYSTEM	PI	004	CONO	CPA PWR FAIL CLR	CPA PAR ERR CLR	CPA PAR EN CLR	CPA PAR EN SET	—	PI RESET	PIE FM IOB(1)	PIO(1) FM IOB(1)	PIO(0) FM IOB(1)	PI ACT CLR	PI ACT SET	PI 1 SELECT	PI 2 SELECT	PI 3 SELECT	PI 4 SELECT	PI 5 SELECT	PI 6 SELECT	PI 7 SELECT	DATAO SET MI PROG	
			CONI	CPA PWR FAIL (1)	CPA PAR ERR (1)	CPA PAR EN (1)	PIH 1 (1)	PIH 2 (1)	PIH 3 (1)	PIH 4 (1)	PIH 5 (1)	PIH 6 (1)	—	PIH 7 (1)	PI ACT (1)	PIO 1 (1)	PIO 2 (1)	PIO 3 (1)	PIO 4 (1)	PIO 5 (1)	PIO 6 (1)	PIO 7 (1)	—
			DATAO	MI 0/18	1/19	2/20	MI 3/21	4/22	5/23	MI 6/24	7/25	8/26	—	MI 9/27	10/28	11/29	MI 12/30	13/31	14/32	MI 15/33	16/34	17/35	—
PAPER TAPE PUNCH	PTP	100	CONO	—	—	—	—	—	—	—	—	—	—	—	—	PTP BIN	PTP BUSY	PTP DONE	PTP PIA 33	PTP PIA 34	PTP PIA 35	DATAO SET MI PROG	
			CONI	—	—	—	—	—	—	—	—	—	—	—	PTP NO TAPE	PTP BIN(1)	PTP BUSY(1)	PTP DONE(1)	PTP PIA 33 (1)	PTP PIA 34 (1)	PTP PIA 35 (1)	—	
			DATAO	—	—	—	—	—	—	—	—	—	—	PTP HOLE 8	PTP HOLE 7	PTP HOLE 6	PTP HOLE 5	PTP HOLE 4	PTP HOLE 3	PTP HOLE 2	PTP HOLE 1	—	PTP DONE CLR PTP BUSY SET
PAPER TAPE READER	PTR	104	CONO	—	—	—	—	—	—	—	—	—	—	—	PTP EOT	PTP BIN	PTP BUSY	PTP DONE	PTP PIA 33	PTP PIA 34	PTP PIA 35	DATAO SET MI PROG	
			CONI	—	—	—	—	—	—	—	—	—	—	—	PTP TAPE FLAG(1)	PTP BIN(1)	PTP BUSY(1)	PTP DONE(1)	PTP PIA 33 (1)	PTP PIA 34 (1)	PTP PIA 35 (1)	—	
			DATAI LEFT / RIGHT	PTR0 / PTR18	PTR1 / PTR19	PTR2 / PTR20	PTR3 / PTR21	PTR4 / PTR22	PTR5 / PTR23	PTR6 / PTR24	PTR7 / PTR25	PTR8 / PTR26	—	PTR9 / PTR27	PTR10 / PTR28	PTR11 / PTR29	PTR12 / PTR30	PTR13 / PTR31	PTR14 / PTR32	PTR15 / PTR33	PTR16 / PTR34	PTR17 / PTR35	—
TELETYPE	TTY	120	CONO	—	—	—	—	—	—	TTY TEST SET	TTI BUSY CLR	TTI FLAG CLR	TTI BUSY SET	TTI FLAG SET	TTI BUSY SET	TTI BUSY SET	TTI DONE SET	TTY PIA 33	TTY PIA 34	TTY PIA 35	DATAO SET MI PROG		
			CONI	—	—	—	—	—	—	—	TTY TEST (1)	—	—	—	—	TTY BUSY (1)	TTY FLAG (1)	TTY DONE (1)	TTY PIA 33 (1)	TTY PIA 34 (1)	TTY PIA 35 (1)	—	
			DATAO	—	—	—	—	—	—	—	—	—	—	—	—	TTY 0	TTY 1	TTY 2	TTY 3	TTY 4	TTY 5	TTY 6	TTY 7
DATAI	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TTY DONE CLR TTY BUSY SET TTY FLAG CLR		
PROGRAM COUNTER FLAGS SAVED BY JSP, ETC.	—	—	—	AR OV FLAG(1)	AR CRV 0 FLAG(1)	AR CRV1 FLAG(1)	AR FOV(1)	BYFG(1)	EX USER(1)	—	—	—	—	—	AR FAV(1)	AR DCK(1)	*	*	*	*	*		

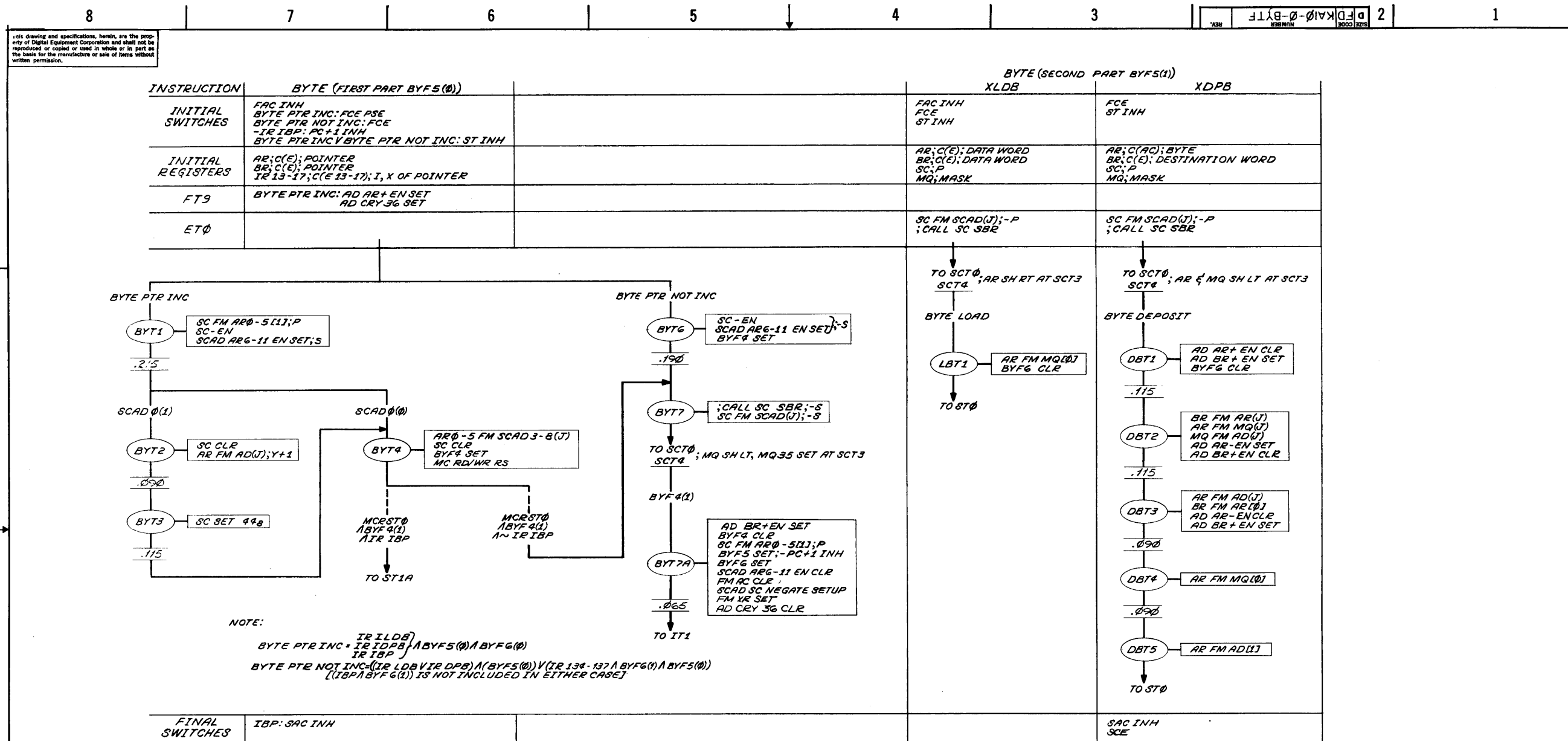
\* THESE BITS NOT AVAILABLE FOR FLAGS SINCE THEY WILL CAUSE ADDRESS MODIFICATION WHEN INDIRECTED THRU

REV. 1	DATE 1-19-68	BY A. KENT
REV. 2	DATE 1-19-68	BY A. KENT
REV. 3	DATE 1-19-68	BY A. KENT

DEC FORM NO. 482 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DATE 1-19-68	
DIMENSION IN INCHES		DATE 1-19-68	
TOLERANCES		DATE 1-19-68	
DECIMALS FRACTIONS ANGLES		DATE 1-19-68	
± .005 ± 1/64 ± 0°30'		DATE 1-19-68	
FINAL SURFACE QUALITY		DATE 1-19-68	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE 1-19-68	
MATERIAL		DATE 1-19-68	
FINISH		DATE 1-19-68	
SCALE		DATE 1-19-68	
SHEET OF		DATE 1-19-68	

digital EQUIPMENT CORPORATION	MAYNARD, MASSACHUSETTS
TITLE	
BASIC I-O REGISTERS	
SIZE CODE	NUMBER
D FDKA I 0 - 0 - BIOR	A
REV.	REV.
A	A



BYTE LOAD = (IR ILDB V IR LDB) ^ BYF 5(1)  
 BYTE DEPOSIT = (IR IDPB V IR DPB) ^ BYF 5(1)

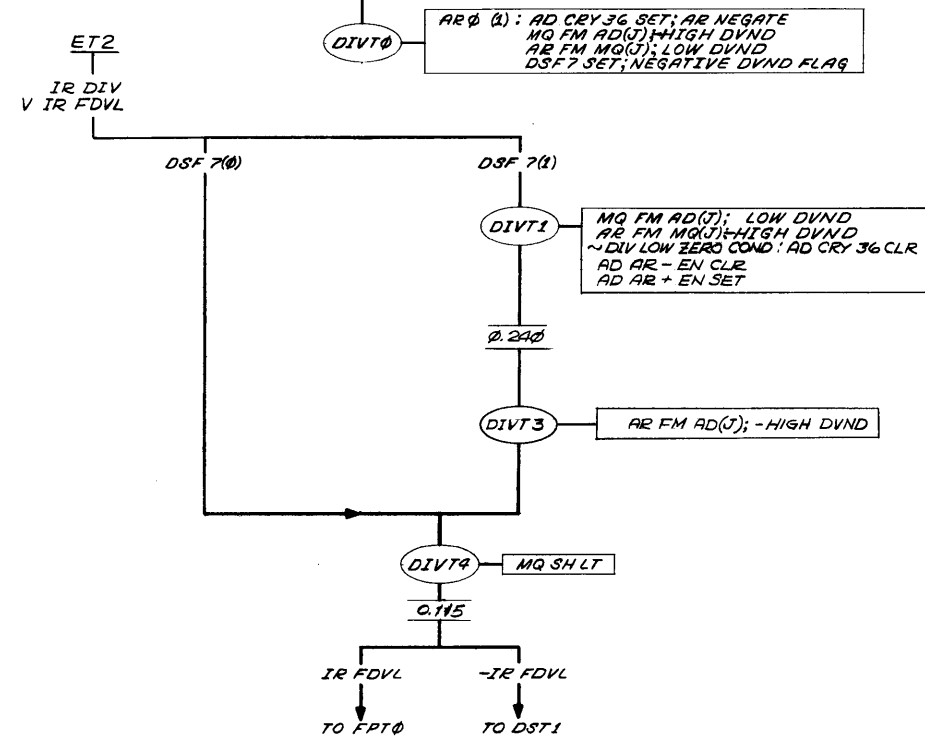
REV.	CHG.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DRN	DATE	11-2-66	
CHRD	DATE	1-16-68	
ENG	DATE	7/17/64	
PRD	DATE	1-7-64	
PRD	DATE	1-19-68	
MATERIAL			
FINISH			
SCALE			
SHEET OF			
TITLE			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
BYTE INSTRUCTION FLOW			
SIZE CODE NUMBER REV.			
DFDKAI0-0-BYTF			

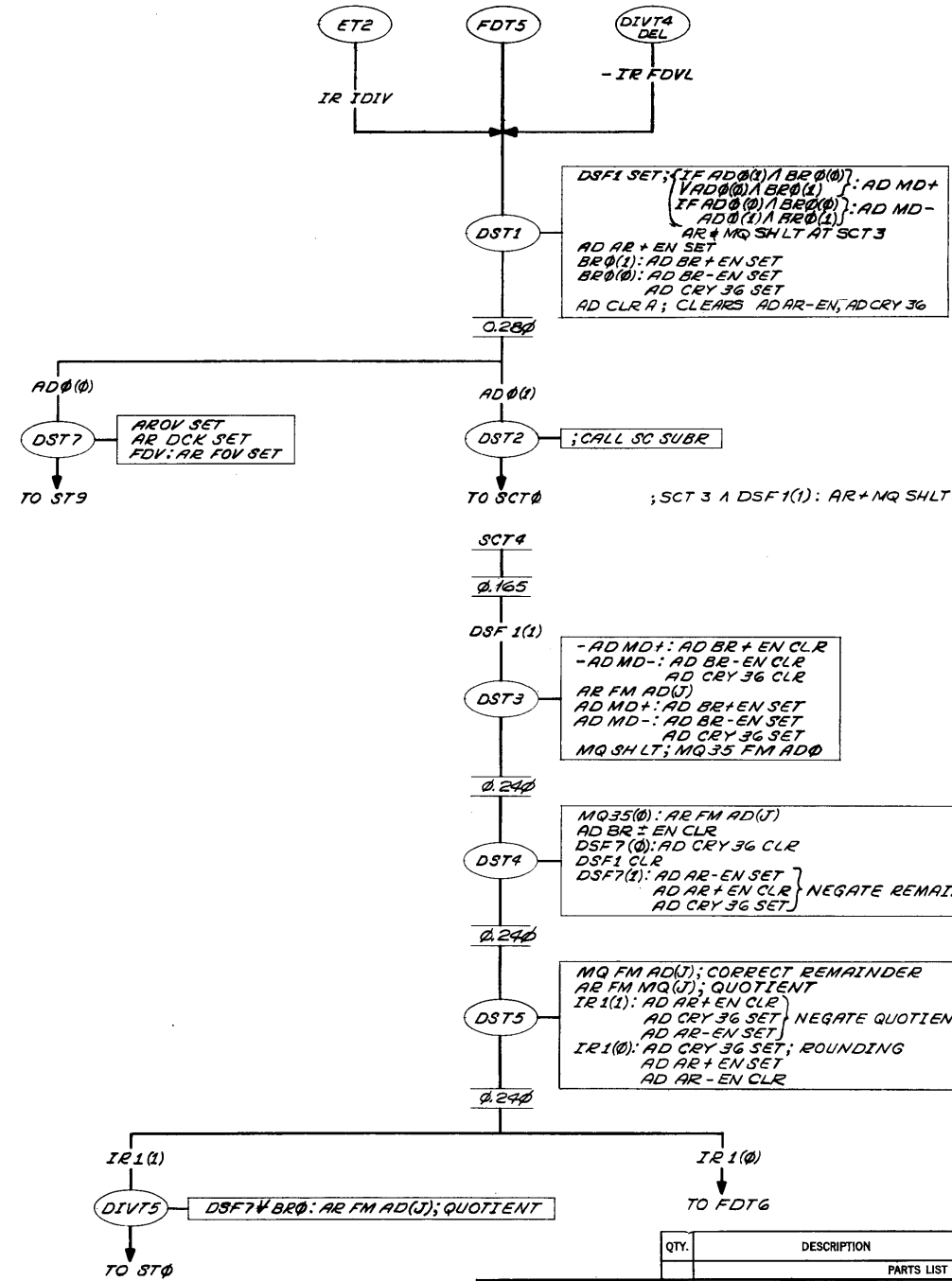
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INSTRUCTION	IDIVX	DIVX
INITIAL SWITCHES	-DIVI: FCE EF0 LONG E LONG ST INH	FAC2 -DIVI: FCE ST INH E LONG
INITIAL REGISTERS	AR; C(AC); DIVIDEND BR; 0, E or C(E); DIVISOR MQ; 0	AR; C(AC); HIGH DIVIDEND BE; 0, E or C(E); DIVISOR MQ; C(AC2); LOW DIVIDEND
FT9	AD AR NEGATE	AD AR-EN SET
ET0	AR0B(1): AR FM AD(J); -DVND DSF7 SET SC MD SETUP AD AR-EN CLR AD AR+EN SET AD CRY36 CLR	SC MD SETUP (TO DIVT0)
ET1	MQ FM AD(J) AR CLR	
ET2	MQ SHLT (TO DST1) AR RT SHLT	(TO DIVT1 OR DIVT4)
FINAL SWITCHES		XDIVM: SAC INH XDIV(I): SAC2 XDIV(B): SCE

FIXED POINT DIVIDE  
ET0 ^ IR DIV      ET0 ^ IR FDVL



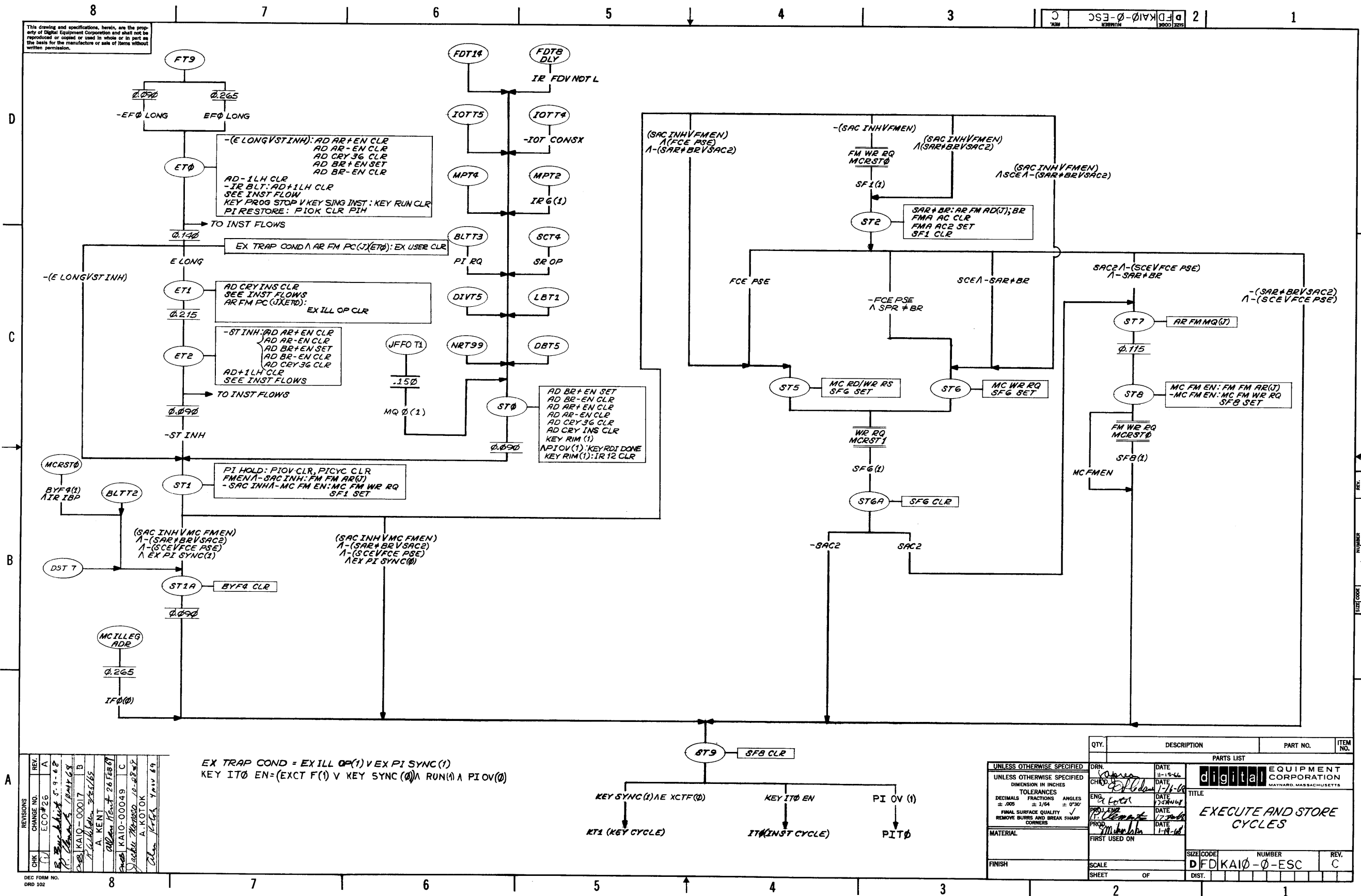
DIVIDE SUBROUTINE



REV.	CHG.	NO.	DATE	BY	APP.
1	0001	1	1-16-68	A. KENT	
2	0002	2	1-16-68	A. KENT	
3	0003	3	1-16-68	A. KENT	
4	0004	4	1-16-68	A. KENT	
5	0005	5	1-16-68	A. KENT	
6	0006	6	1-16-68	A. KENT	
7	0007	7	1-16-68	A. KENT	
8	0008	8	1-16-68	A. KENT	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
± .005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL		DATE	
FINISH		DATE	
SCALE		DATE	
SHEET OF		DATE	
DIST.		DATE	
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE <b>FIXED POINT DIVIDE &amp; DIVIDE SUBROUTINE</b>			
SIZE CODE	NUMBER	REV.	
D FDKAI0-0-DIVF	5	S	

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REV.	CHG. NO.	DATE	BY	CHK.
A	ECO#26	11-18-66	A. KENT	
B	104118	1-18-67	A. KENT	
C	104118	1-18-67	A. KENT	
D	104118	1-18-67	A. KENT	

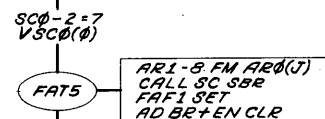
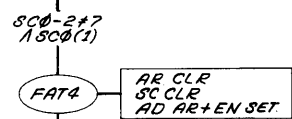
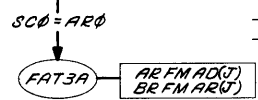
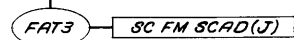
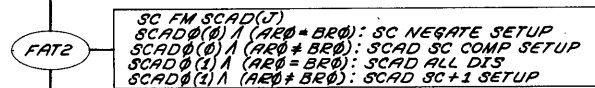
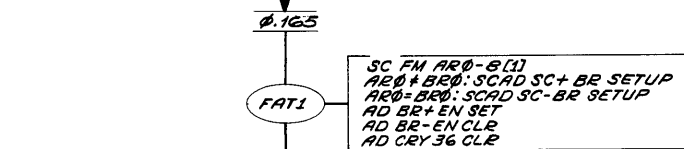
EX TRAP COND = EX ILL OP(1) V EX PI SYNC(1)  
 KEY IT0 EN = (EXCT F(1) V KEY SYNC(0)) A RUN(1) A PI OV(0)

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	UNLESS OTHERWISE SPECIFIED		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS FRACTIONS ANGLES		
	± .005 ± 1/64 ± 0'30"		
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET OF		
	DISTRIBUTION		
	REV. C		



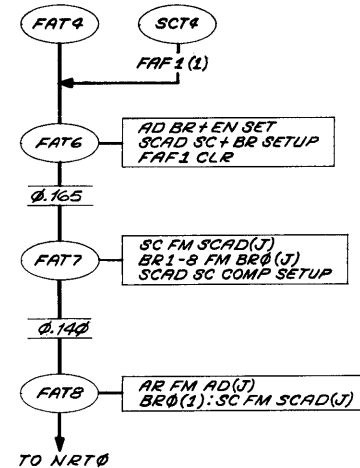
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INSTRUCTION	FAD	FSB	UFA
INITIAL SWITCHES	IRFP-IMM:FCE ST INH	EFØ LONG IRFP-IMM:FCE ST INH	FCE ST INH
INITIAL REGISTERS	AR:C(AC) BR:C(E)/E,Ø SC:Ø MQ:Ø	AR:C(AC) BR:C(E)/E,Ø SC:Ø MQ:Ø	AR:C(AC) BR:C(E) SC:Ø MQ:Ø
FT9		AD MINUS BR	
ETØ		AR FM AD(J) BR FM AR(J)	FMA AC2 SET FMA AC CLR



	FAD, FSB	LONG	UFA
FINAL SWITCHES	- LONG XXX <sup>M</sup> :SCE XXXM:SAC INH	SAC2	

NOTE:  
UFA STORES IN AC2  
BY CLEARING FMA AC  
AND SETTING FMA AC2  
AT ETØ



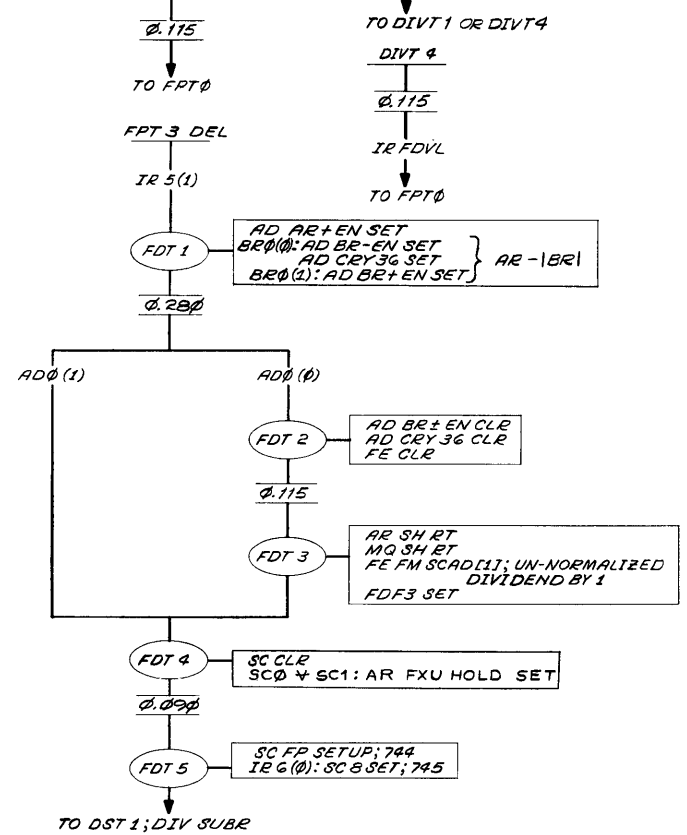
REV.	CHG	NO.	DATE	BY
A	00017			
A	00018			
A	00019			

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DRN	DATE	TITLE	
CHKD	DATE	FLOATING ADD, SUB, & UFA FLOW	
ENG	DATE	SCALE	
DESIGNED BY	DATE	SHEET	
PROD. BY	DATE	OF	
FIRST USED ON	SIZE CODE		
	D FDKAIØ-Ø-FAF		
	NUMBER		
	REV. A		

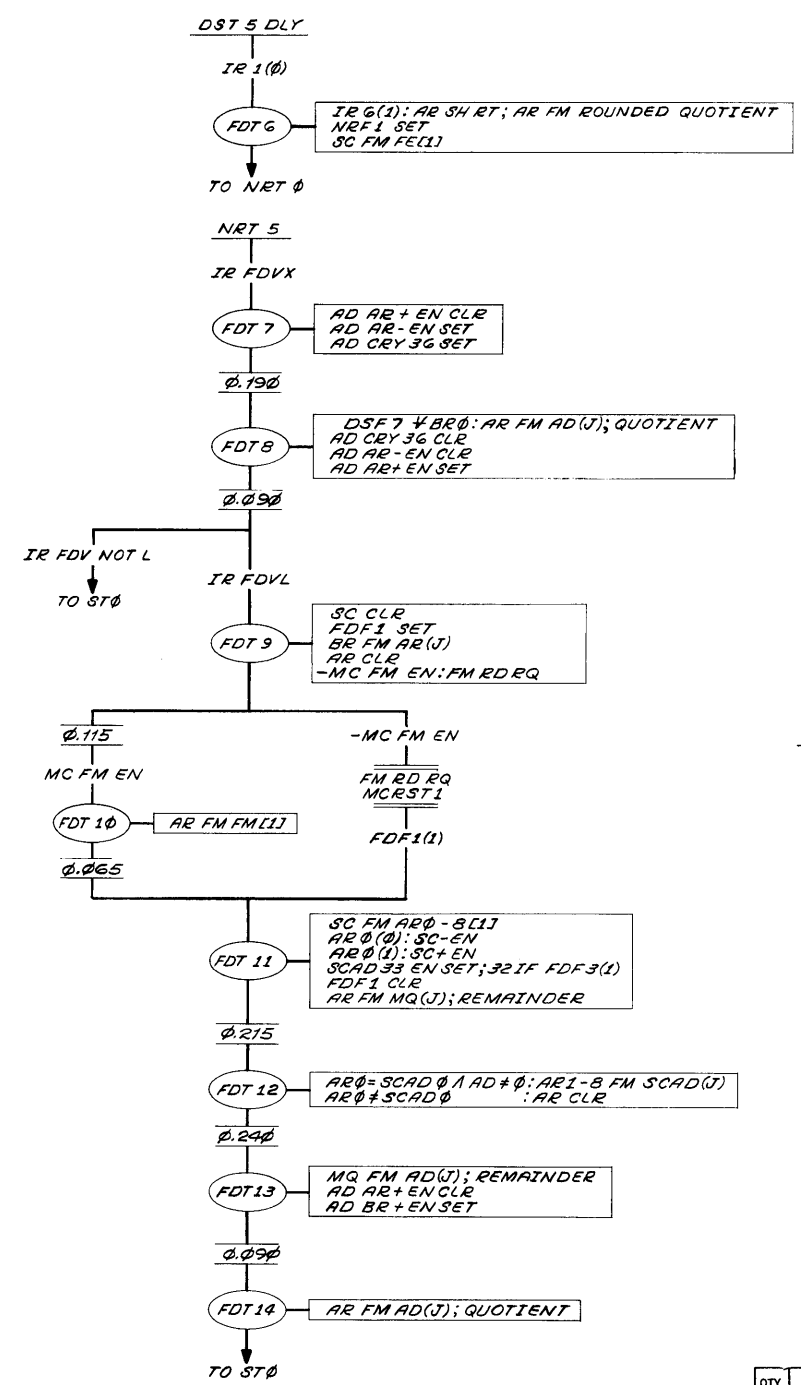


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INSTRUCTION	FDV	FDVL
INITIAL SWITCHES	EF0 LONG	FAC2 E LONG IR EP-IMM:FCE ST INH
INITIAL REGISTERS	AR, AC; DIVIDEND BR; C(6) OR E, 0; DIVISOR SC; 0 MQ; 0 OR C(AC2) FE; 0	
FT9	AD AR NEGATE	AD AR-EN SET
ET0	AR0B(1): AR FM AD(J) DSF7 SET	ET0 ET1 ET2



FINAL SWITCHES	XXX M: SCE	SAC 2
	XXX B: SAC INH	



**SUMMARY**  
 BR; QUOTIENT W/ EXPONENT  
 MQ; REMAINDER W/O EXPONENT  
 AR; DIVIDEND W/ EXPONENT  
 SC; EXPONENT OF DIVIDEND

REV.	CHANGE NO.	DATE	BY	CHK
A	KAIO-00017	10-29-66	A. KENT	
B	KAIO-00049	1-16-68	A. KENT	
C	KAIO-00060	1-19-68	A. KENT	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE: <b>FLOATING DIVIDE</b>			
UNLESS OTHERWISE SPECIFIED		DRN. DATE 10-29-66	
DIMENSION IN INCHES		CHKD. DATE 1-16-68	
TOLERANCES		ENG. DATE 1-19-68	
DECIMALS ±.005		DATE 1-19-68	
FRACTIONS ± 1/64		DATE 1-19-68	
ANGLES ± 0°00'		DATE 1-19-68	
MATERIAL			
FINISH			
SCALE		SIZE CODE	
SHEET OF		NUMBER	
		REV.	
		C	



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SIZE CODE NUMBER  
D F D KAIØ-Ø-FSDN 2

INSTRUCTION	FSC FLOATING SCALE (132)	DFN DOUBLE FLOATING NEGATE (131)
INITIAL SWITCHES	ST INH E LONG	E LONG FCE PSE EFØ LONG
INITIAL REGISTERS	BR; Ø, E AR; C(AC) SC; Ø	BR; C(E) AR; C(AC) SC; Ø
FT9		AD MINUS BR SCAD SC+BR SETUP
ETØ	SC FM BR(1); E BR FM AR(J) ARØ(Ø): SCAD SC+BR SETUP ARØ(1): SCAD SC-BR SETUP ; SC+1 EN INH.	SC FM SCAD(J) BR FM AR(J) AR FM AD(J) AD 9-35+Ø: AD CRY 36 CLR SCAD ALL DIS
ET1	AR1-8 FM ARØ(J)	ARØ-8 FM SCAD(J)
ET2	SC FM SCAD(J)	BR FM AR(J) AR FM AD(J)
↓ TO NRTØ		
FINAL SWITCHES		SAR ≠ BR

REV.	
CHANGE NO.	
CHK	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN <i>Scania</i> DATE 11/1/66 CHG <i>W. Adams</i> DATE 1-16-68 ENG. <i>A. Latch</i> DATE 1/27/68 PROJ. ENG. <i>A. Adams</i> DATE 1/27/68 PROD. <i>J. Moulton</i> DATE 1-19-68	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ±.005 ± 1/64 ± 0°30' FINAL SURFACE QUALITY ✓ REMOVE BURRS AND BREAK SHARP CORNERS		TITLE <b>FLOATING SCALE &amp; DOUBLE FLOATING NEGATE</b>	
MATERIAL	FIRST USED ON	SIZE CODE	NUMBER
FINISH	SCALE	D F D KAIØ-Ø-FSDN	REV.
	SHEET OF	DIST.	

DEC FORM NO. DFD 102

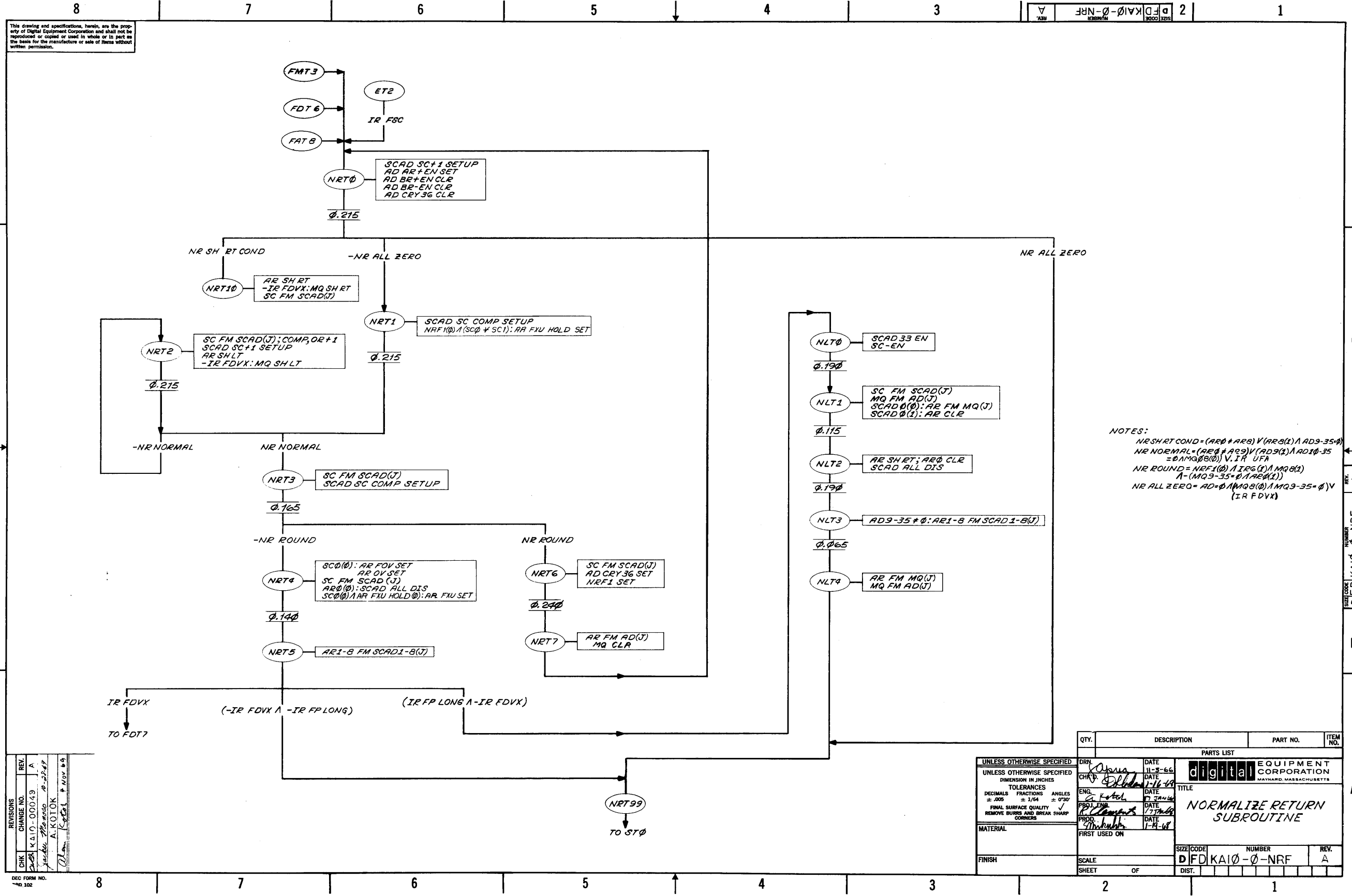












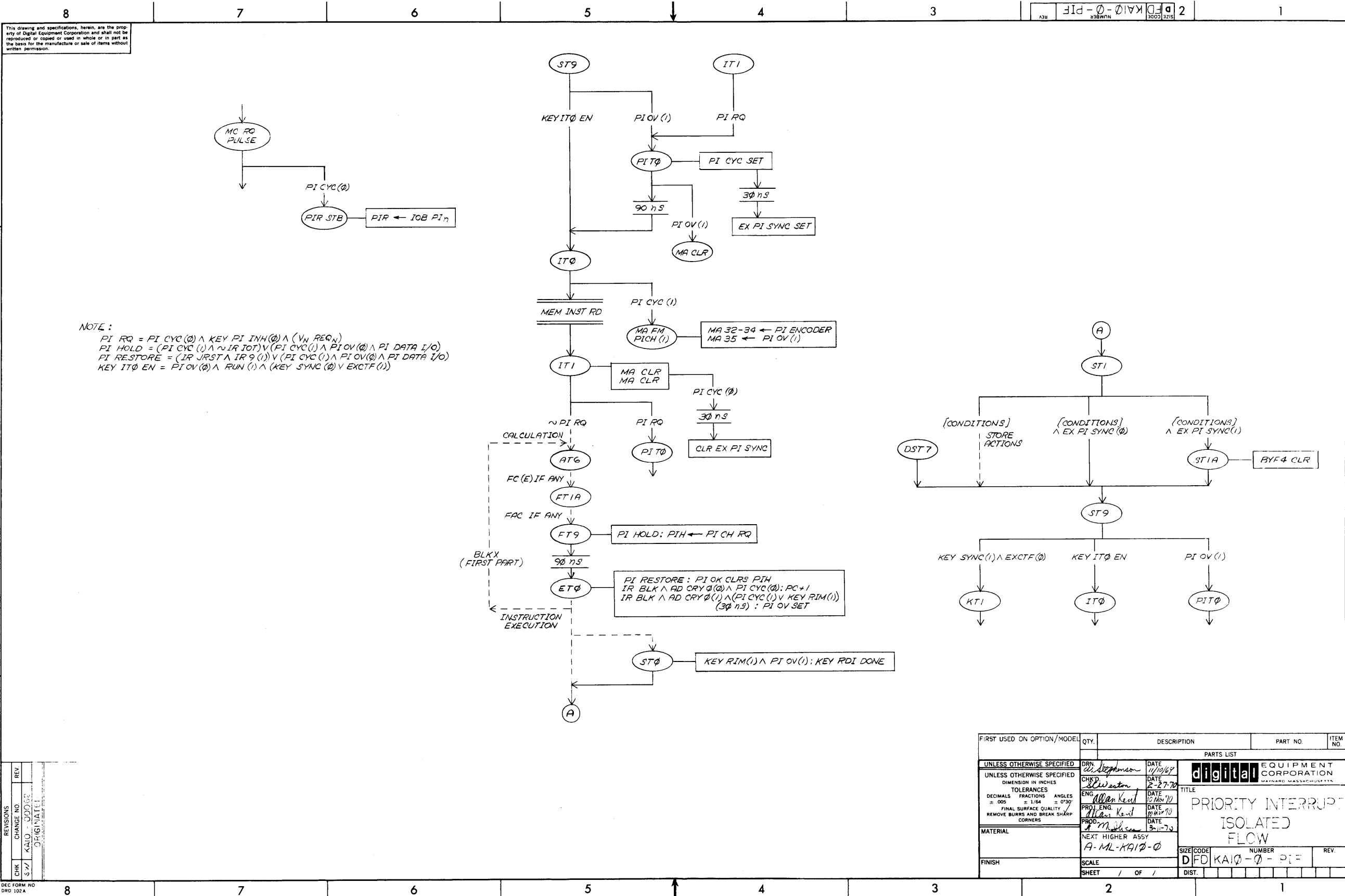
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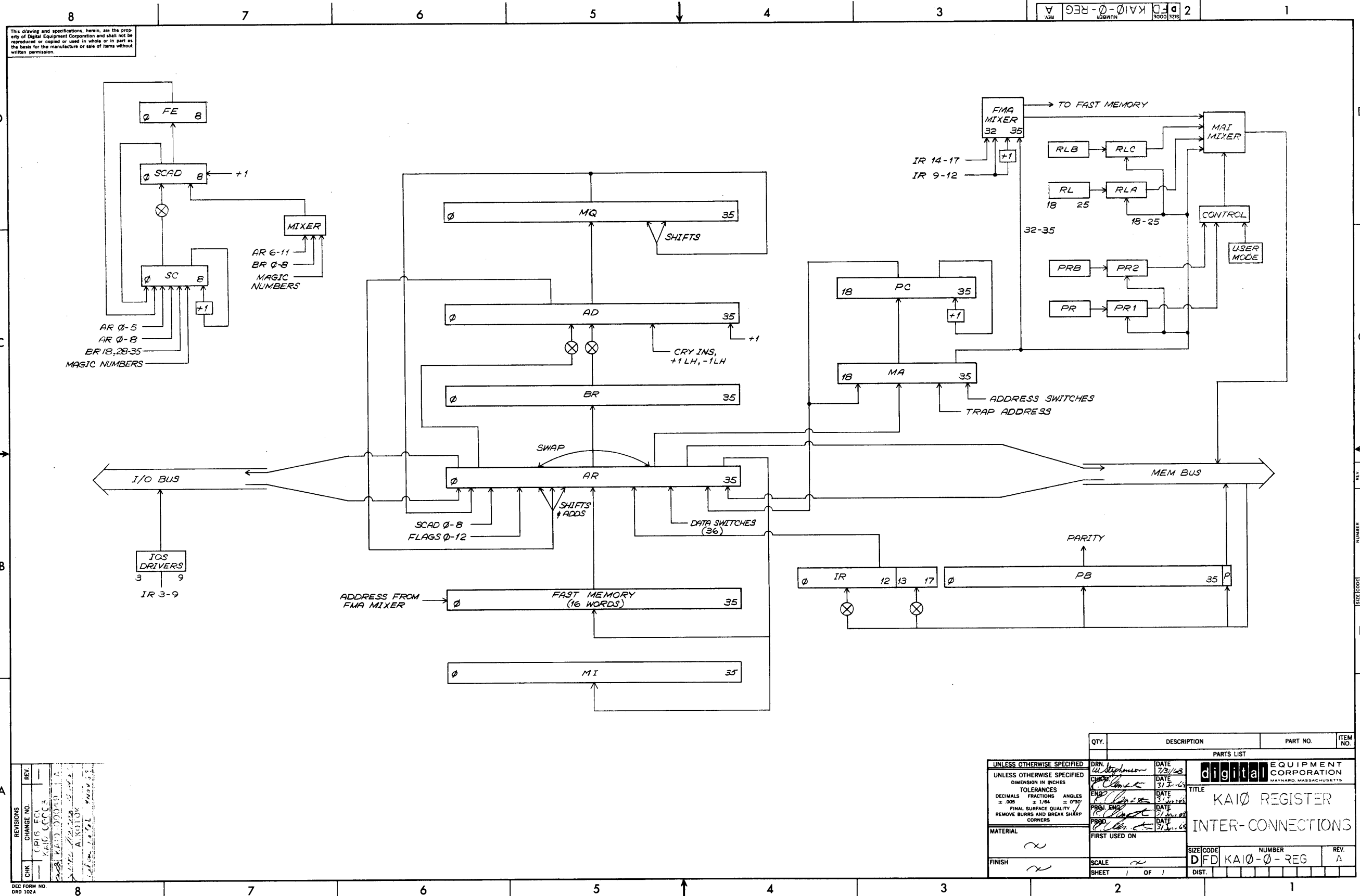
NOTES:  
 NR SH RT COND = (AR0 \* AR8) V (AR8(1) ^ AD9-35-0)  
 NR NORMAL = (AR0 \* AR9) V (AD9(1) ^ AD10-35 = 0) ^ AMQ0(0) V, I R UFA  
 NR ROUND = NRT1(0) ^ I R G(1) ^ M Q 8(1) ^ (M Q 9-35 = 0) ^ A R 0(1)  
 NR ALL ZERO = AD = 0 ^ M Q 8(0) ^ M Q 9-35 = 0 ^ V (I R F D V X)

REV	CHG	NO.	DATE
A		1	11-8-66
A		2	1-16-68
A		3	7-24-68
A		4	7-27-68
A		5	1-14-68

DEC FORM NO. 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE <b>NORMALIZE RETURN SUBROUTINE</b>			
UNLESS OTHERWISE SPECIFIED		SCALE	REV. A
UNLESS OTHERWISE SPECIFIED		SHEET OF	SIZE CODE D I F D K A I 0 - 0 - N R F
DIMENSION IN INCHES		NUMBER	
TOLERANCES		REV.	
DECIMALS	FRACTIONS	A	
± .005	± 1/64		
ANGLES	± 0°30'		
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
FIRST USED ON			
DATE			
BY			
CHECKED			
DATE			
ENGINEER			
DATE			
DRAWN			
DATE			





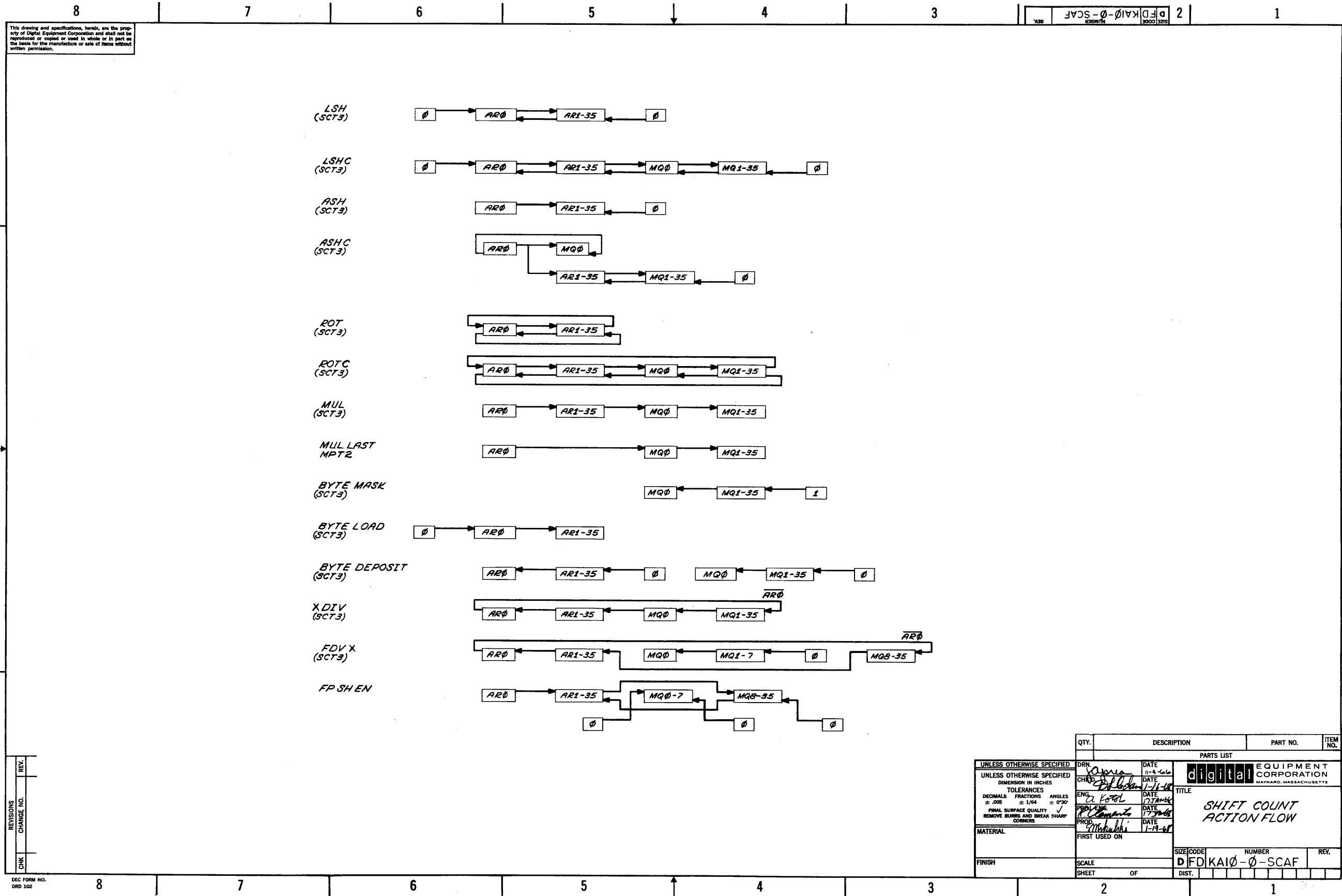
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REV.	CHANGE NO.	DESCRIPTION
1	1	INITIAL DESIGN
2	2	REVISED TO MATCH MECHANICAL DRAWING
3	3	REVISED TO MATCH MECHANICAL DRAWING
4	4	REVISED TO MATCH MECHANICAL DRAWING
5	5	REVISED TO MATCH MECHANICAL DRAWING
6	6	REVISED TO MATCH MECHANICAL DRAWING
7	7	REVISED TO MATCH MECHANICAL DRAWING
8	8	REVISED TO MATCH MECHANICAL DRAWING

DEC FORM NO. DRD 102A

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	UNLESS OTHERWISE SPECIFIED: DRN 1, DATE 12/1/68, DIMENSION IN INCHES, TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0'30", FINAL SURFACE QUALITY: REMOVE BURRS AND BREAK SHARP CORNERS, MATERIAL: 2, FINISH: 2		
	digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS		
	TITLE: KAIO REGISTER INTER-CONNECTIONS		
	SCALE: SHEET 1 OF 1	SIZE CODE: DFD	NUMBER: KAIO-0-REG
			REV. A





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SIZE CODE NUMBER REV. 2

SIZE CODE NUMBER REV. DFDKAI0-0-SCAF

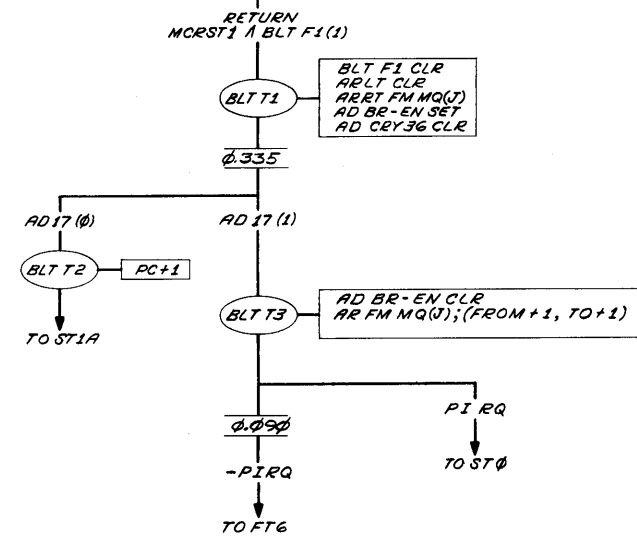
UNLESS OTHERWISE SPECIFIED		QTY.	DESCRIPTION	PARTS LIST	PART NO.	ITEM NO.
DRN	DATE			digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
CHKD	DATE			TITLE		
ENG	DATE			SHIFT COUNT ACTION FLOW		
PROB. ENG.	DATE			SIZE CODE NUMBER REV.		
PROD.	DATE			DFDKAI0-0-SCAF		
MATERIAL	FIRST USED ON			SHEET OF		
FINISH	SCALE			DIST.		

REVISIONS	REV.
CHANGE NO.	
CHK.	

DEC FORM NO. DRD 102

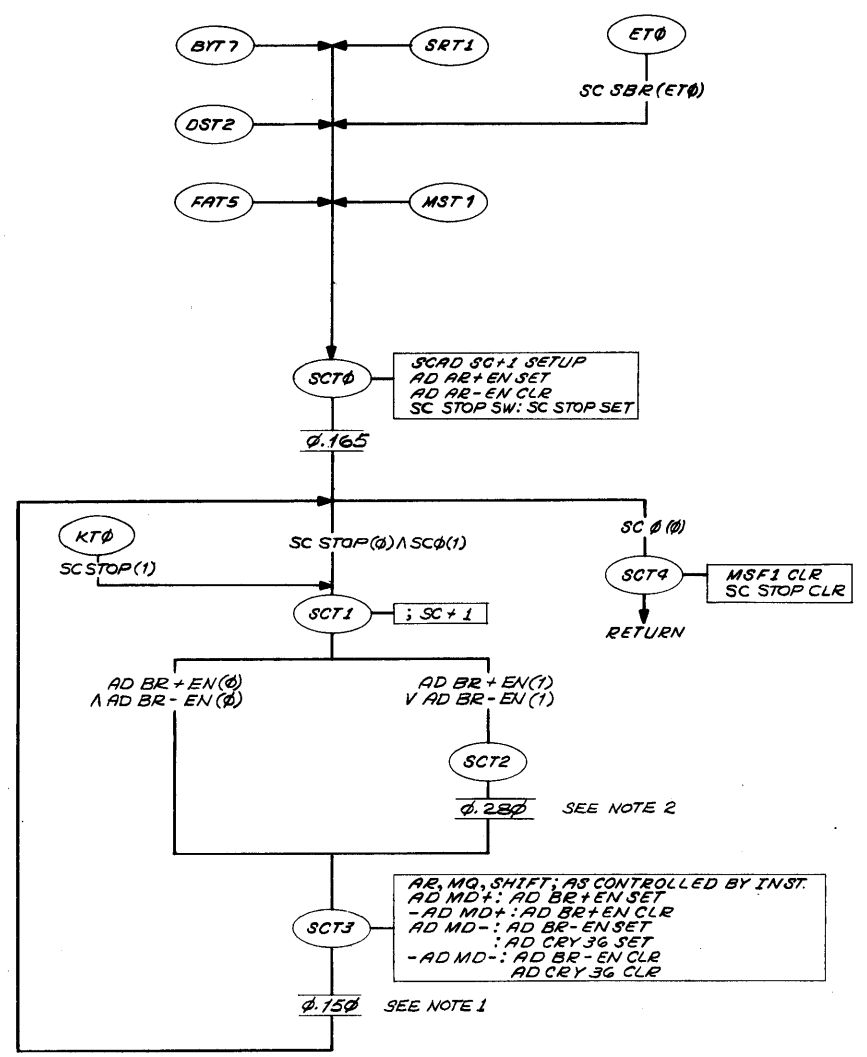
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INSTRUCTION	BLT
INITIAL SWITCHES	PC+1 INH FC C ACLK ST INH E LONG
INITIAL REGISTERS	AR; TO; FROM BR; 0; LAST MQ; DATA; C (FROM) MA; FROM PC; ADDRESS (BLT)
FT9	AD AR+EN SET AD+1 BOTH
ET0	AR SWAP; FROM, TO
ET1	MA FM AR(J); TO
ET2	AR FM MQ(J); DATA MQ FM AD(J); (FROM+1, TO+1) AD+1 LH CLR MC WR RQ BLT F1 SET



**SUMMARY**

BR; (0, FINAL)  
AR; (NEW FROM, TO)  
MA; (OLD, TO)  
MQ; (NEW FROM, TO)



$$AD MD += (MSF1(1) \wedge MQ34(0) \wedge MQ35(1))$$

$$V[DSF1(1) \wedge (AD0(1) \wedge BR0(0)) \wedge (AD0(0) \wedge BR0(1))]$$

$$AD MD -= (MSF1(1) \wedge MQ34(1) \wedge MQ35(0))$$

$$V[DSF1(1) \wedge (AD0(0) \wedge BR0(0)) \wedge (AD0(1) \wedge BR0(1))]$$

- NOTES:
- THIS IS THE SHIFT TIME LOOP DELAY. THE DELAY IS ADJUSTED FOR 150 NS BETWEEN SCT3 WHILE DOING ROTATES. THIS DELAY MUST BE SETUP BEFORE SCT2 DELAY
  - THIS IS THE ADD TIME LOOP DELAY FOR MUL & DIV. THE DELAY IS ADJUSTED FOR 280 NS BETWEEN SCT2 PULSES. THIS DELAY IS SET AFTER THE SCT3 DELAY.

REVISIONS	REV.
CHANGE NO.	
CHK	

DEC FORM NO. DHD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DRN	DATE	DIGITAL EQUIPMENT CORPORATION	
CHRD	DATE	MAYNARD, MASSACHUSETTS	
ENG	DATE	TITLE	
PROJ	DATE	SHIFT COUNT SUB-ROUTINE & BLT FLOW	
PROD	DATE	SCALE	
FIRST USED ON		SHEET OF	
FINISH		DIST.	



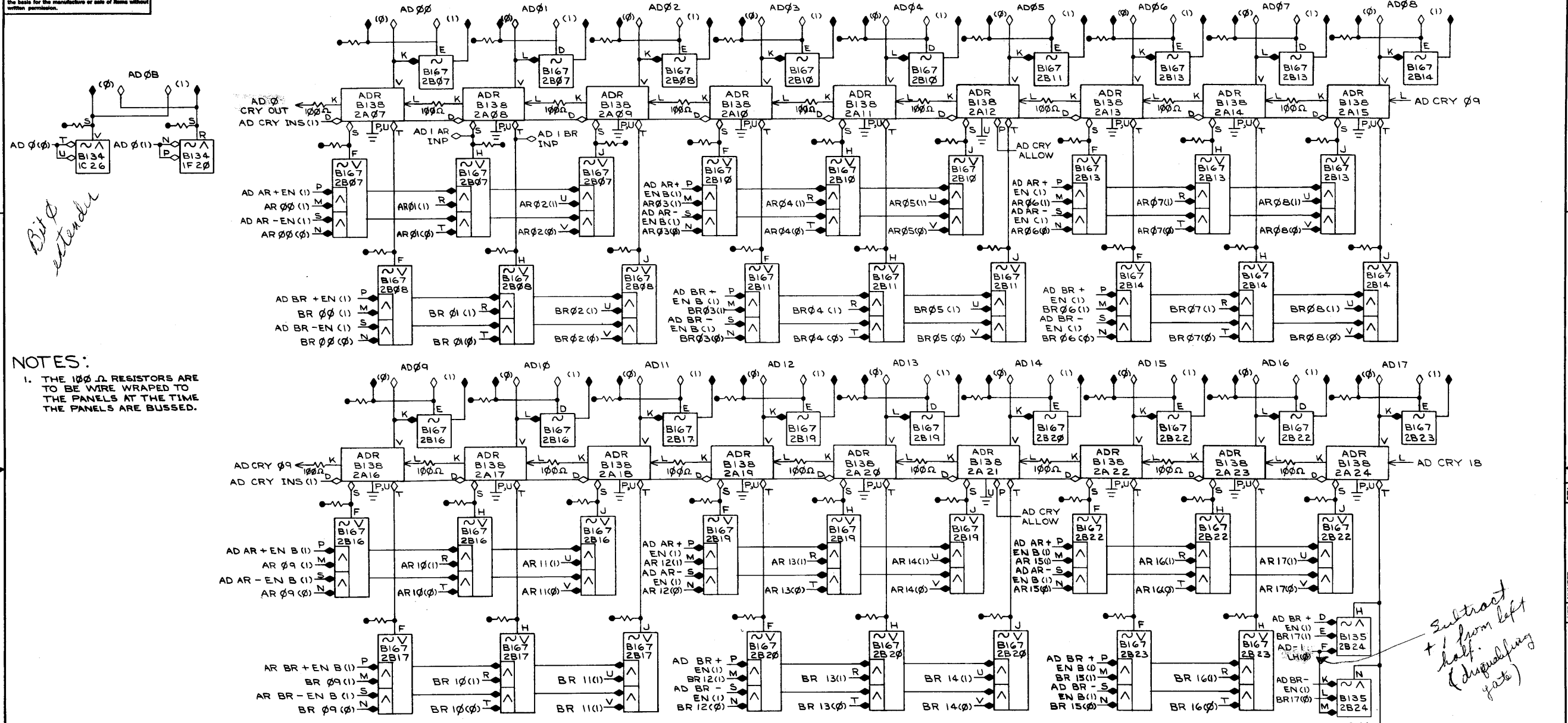






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REV. 1  
D-BS-KA10-0-AD3

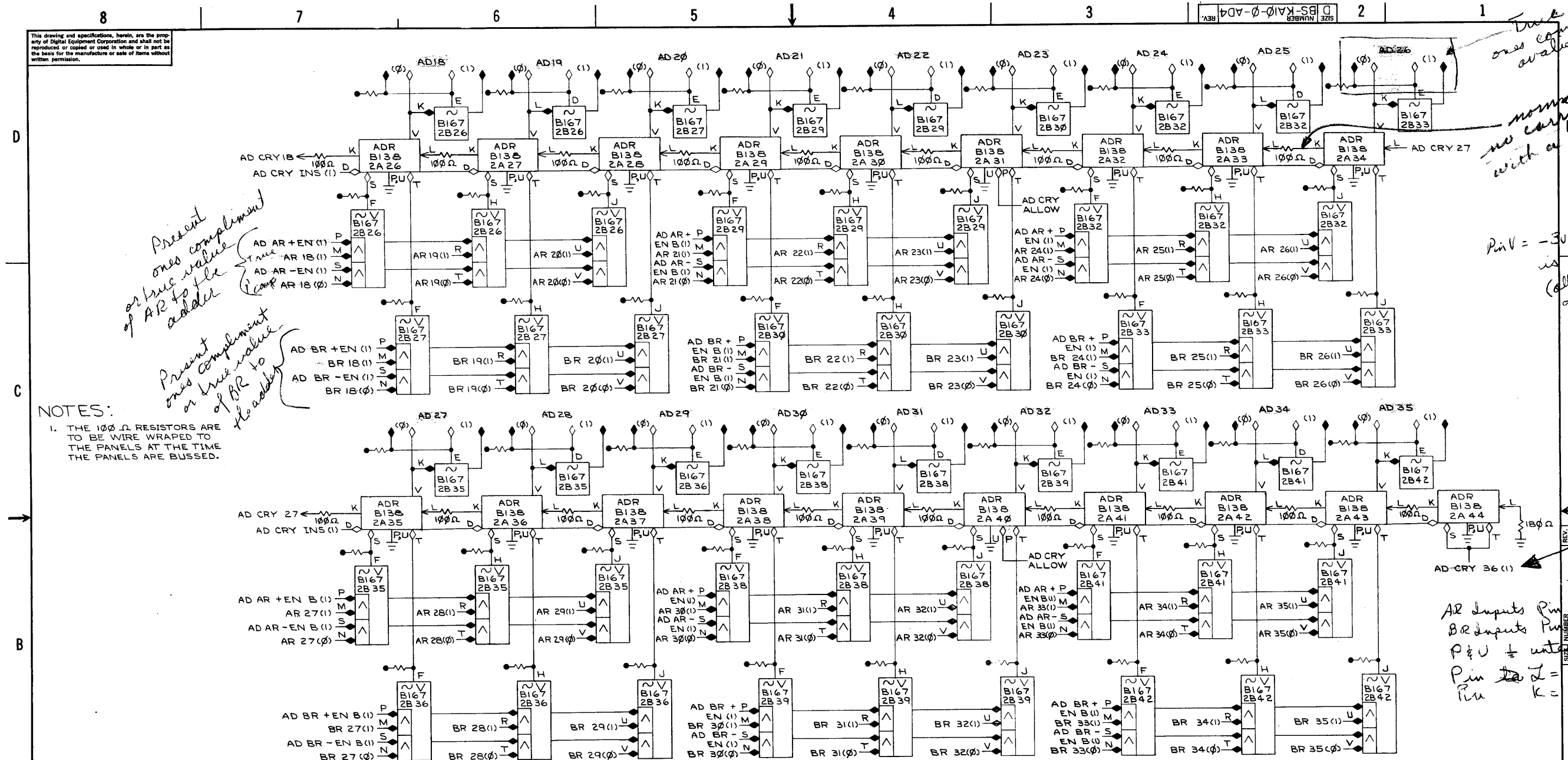


NOTES:  
1. THE 100Ω RESISTORS ARE TO BE WIRE WRAPPED TO THE PANELS AT THE TIME THE PANELS ARE BUSSED.

REV.	CHANGE NO.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
<small>DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ± .005 ± 1/64 ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS</small>			
<small>DRAWN BY: R. M. ...</small> <small>CHECKED BY: ...</small> <small>DATE: 10-25-68</small> <small>DATE: 7-16-68</small>		<small>DIGITAL EQUIPMENT CORPORATION</small> <small>MAYNARD, MASSACHUSETTS</small>	
<b>ADDER LEFT HALF</b>			
<small>FIRST USED ON</small> D-UA-KA10-0-0			<small>NUMBER</small> D-BS-KA10-0-AD3
<small>SCALE</small> 1 OF 1			<small>REV.</small> 

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NOTES:  
 1. THE 100Ω RESISTORS ARE TO BE WIRE WRAPPED TO THE PANELS AT THE TIME THE PANELS ARE BUSSED.

Present or true value of AR to the address  
 Present or true value of BR to the address  
 Present or true complement of AR to the address  
 Present or true complement of BR to the address

True value & ones complement available  
 normal volt for carry  $\approx 4.5V$   
 with a carry  $\approx 2V$

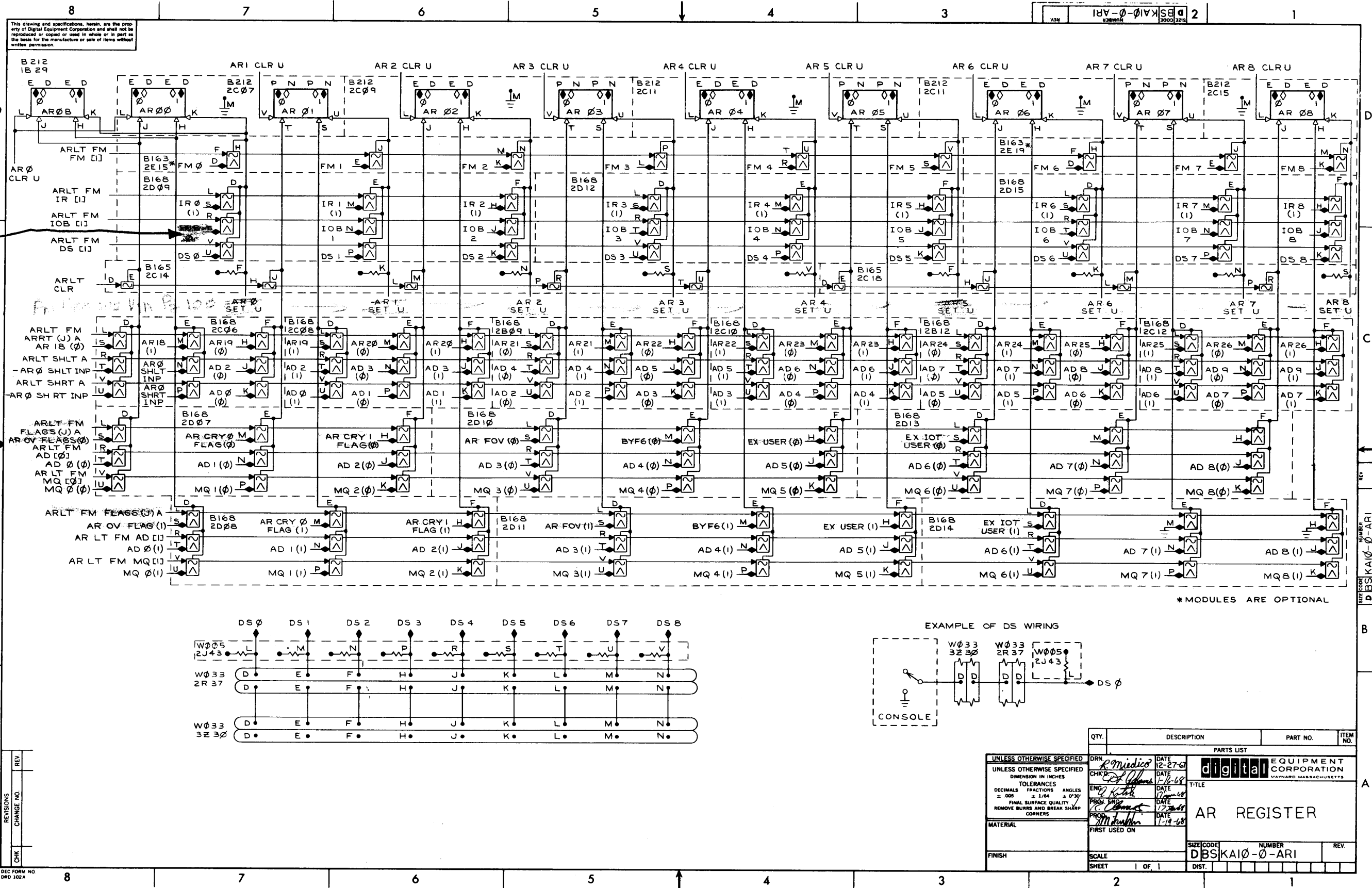
Pin V = -3V when address total is equal to a 1  
 (all 3 inputs add up to one:  $\begin{matrix} 010 \\ 011 \\ 011 \\ \hline 101 \end{matrix}$ )  
 when output = 0 (good) address = 0.

Set's two's complement

AR inputs Pin  
 BR inputs Pin  
 P & U  $\pm$  unattached to AD CRY all  
 Pin  $\alpha$  = carry into address  
 Pin  $\kappa$  = carry out

REV.	NO.
CHK	NO.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES: DECIMALS $\pm .005$ , FRACTIONS $\pm 1/64$ , ANGLES $\pm 0'30"$ FINAL SURFACE QUALITY: REMOVE BURRS AND BREAK SHARP CORNERS MATERIAL: FINISH: SCALE: SHEET 1 OF 1			
DRN: R. Mudio CHD: P. Adams ENG: J. Ketch PROJ. ENGR: PROD. ENGR: DATE: 10-25-67 DATE: 11-16-68 DATE: 12-20-68 DATE: 1-19-68		digital EQUIPMENT CORPORATION WATYARD, MASSACHUSETTS TITLE: <b>ADDER RIGHT HALF</b> NUMBER: D-BS-KA10-0-AD4 REV.	



From I/O Bus

FLAGS TO AR

REV

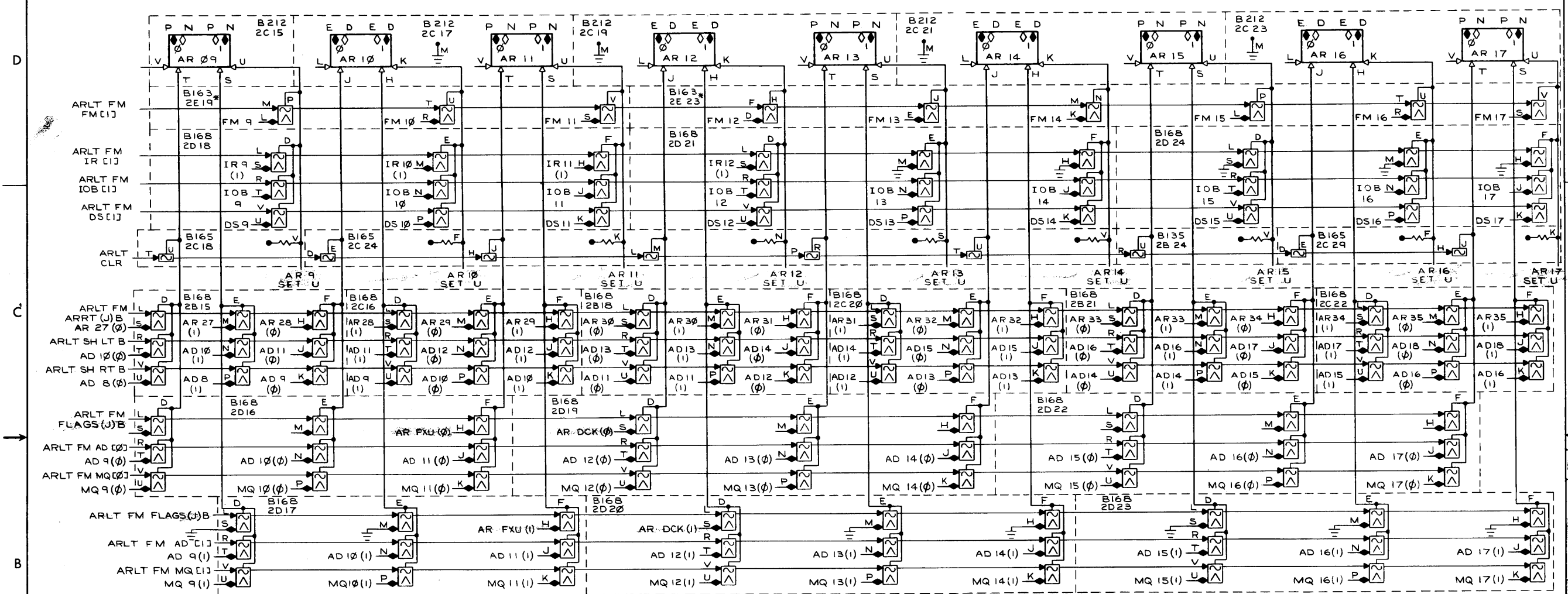
NUMBER DBSKAI0-0-ARI

A

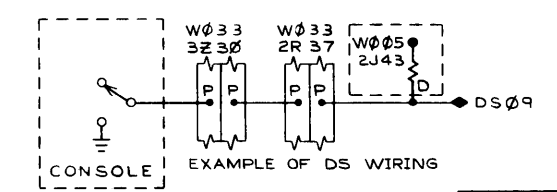
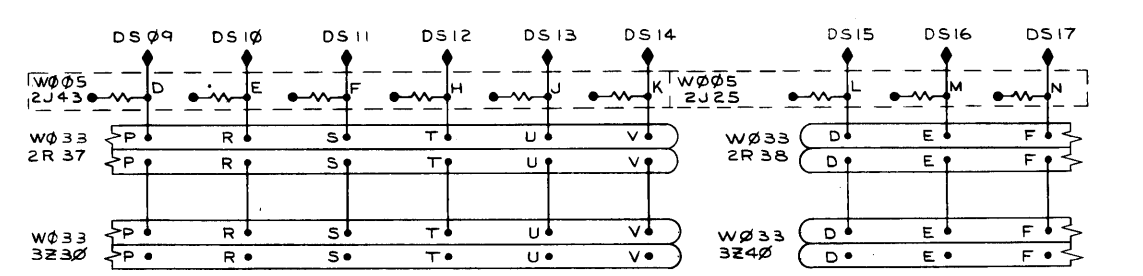
REV	
CHG	
NO.	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRY	
DIMENSION IN INCHES		DATE 12-27-68	
TOLERANCES		CHK'D	
DECIMALS	FRACTIONS	ANGLES	DATE 1/6-68
± .005	± 1/64	± 0°30'	DATE 1/22-68
FINAL SURFACE QUALITY		DATE 1-19-68	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE	
MATERIAL	FINISH	SCALE	SIZE CODE
		SHEET 1 OF 1	NUMBER DBSKAI0-0-ARI
			REV.

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\* MODULES ARE OPTIONAL



QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DRN	DATE 1-2-68	 <b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D	DATE 1-16-68		
ENG	DATE 1-26-68		
PROJ. ENG.	DATE 1-27-68		
TITLE		AR REGISTER	
MATERIAL		FIRST USED ON	
FINISH		SCALE	
		SHEET 1 OF 1	

REVISIONS	REV.
CHANGE NO.	
CHK	

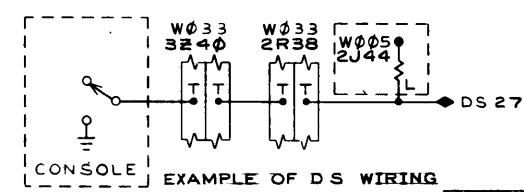
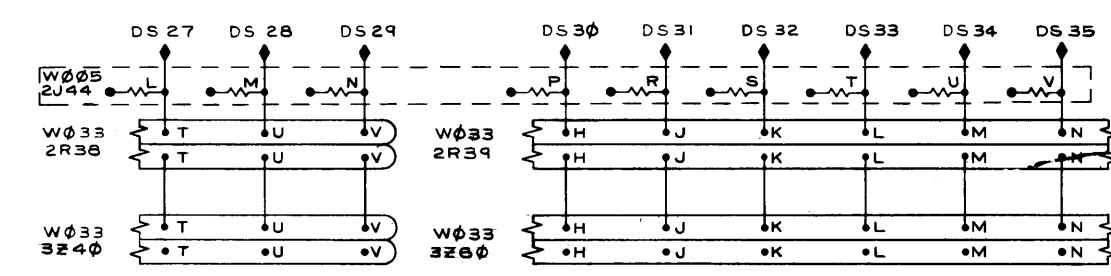
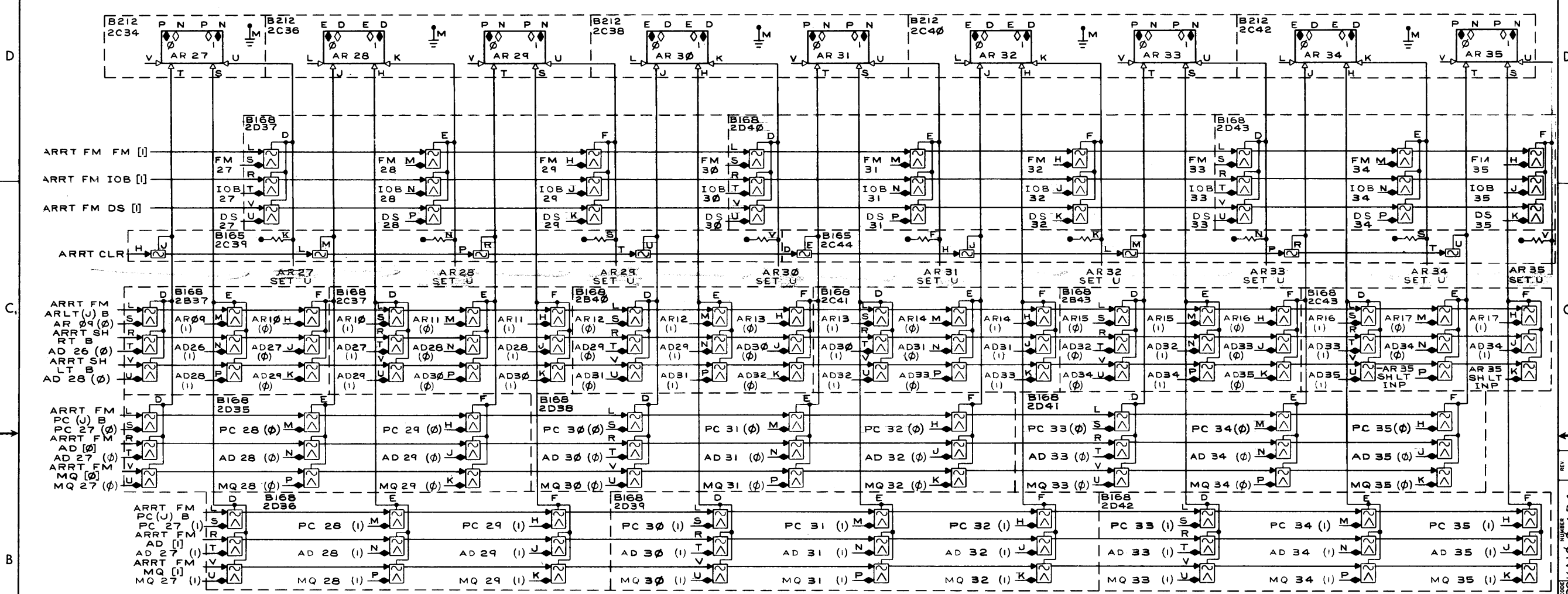
DEC FORM NO DRD 102A





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DBSKA10-0-AR4 2

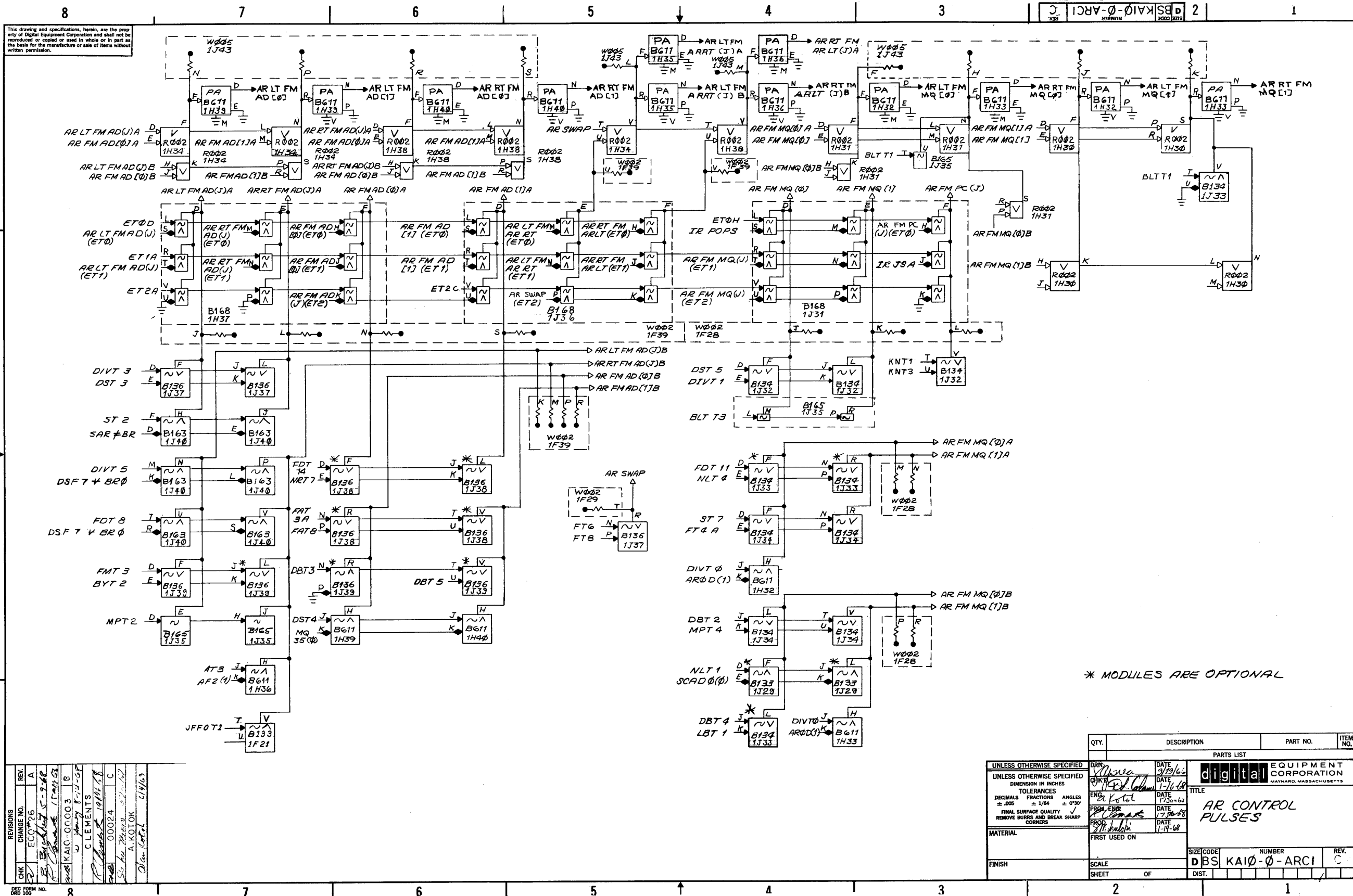


REV.	CHANGE NO.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN <i>E. Kelly</i> DATE 1-3-67	
UNLESS OTHERWISE SPECIFIED		CHK'D <i>D. O'Neil</i> DATE 1-10-67	
DIMENSION IN INCHES		ENC <i>E. Kelly</i> DATE 1-23-67	
TOLERANCES		PROB EN'D <i>P. O'Neil</i> DATE 1-23-67	
DECIMALS FRACTIONS ANGLES		PROD <i>M. O'Neil</i> DATE 1-14-68	
= .005 = 1/64 = 0°30'		TITLE	
FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS		AR REGISTER	
MATERIAL		FIRST USED ON	
FINISH		SCALE	
		SHEET OF	
		SIZE CODE NUMBER REV.	
		DBSKA10-0-AR4	
		DIST.	



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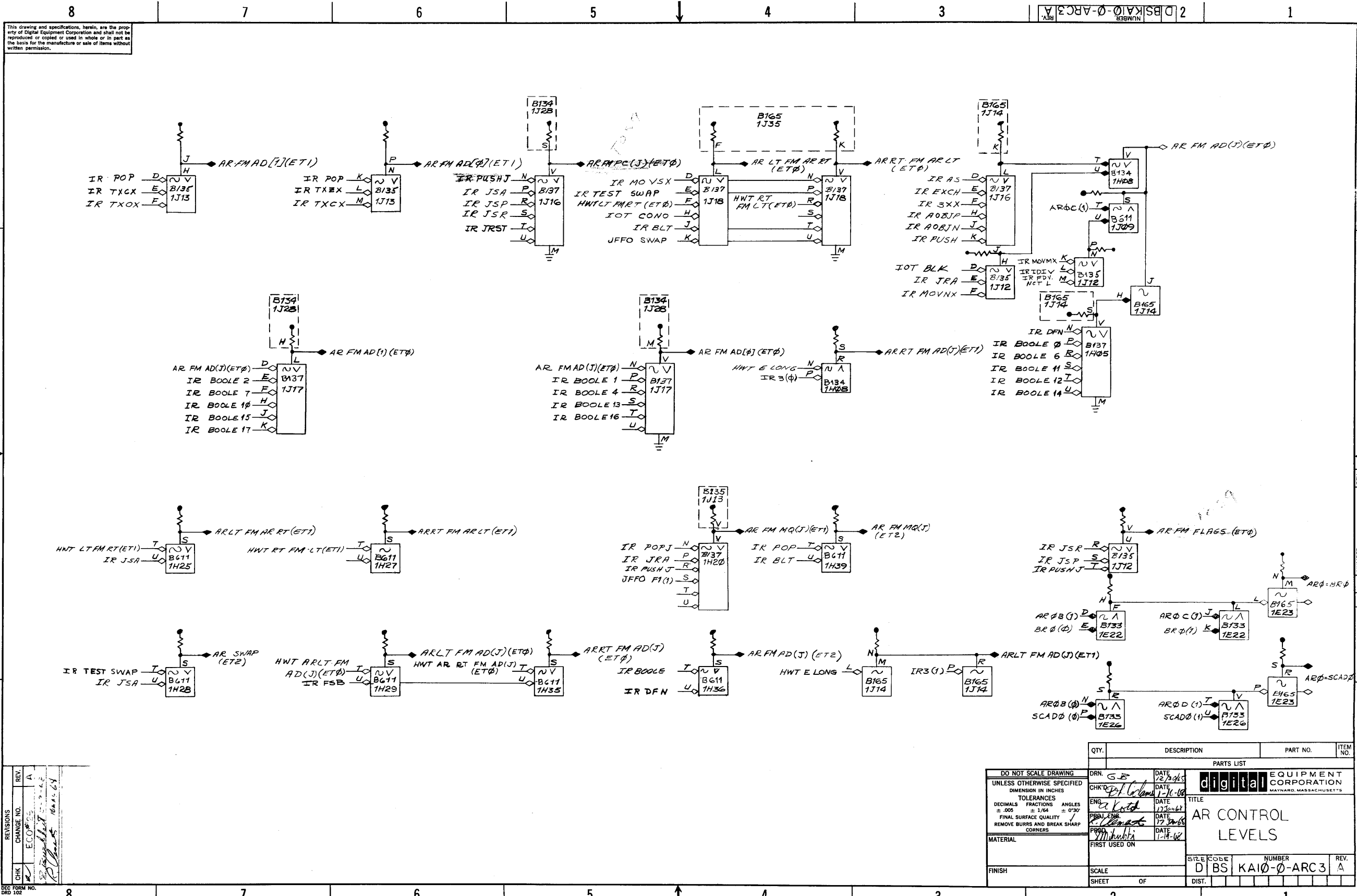
REV.	DATE	BY	CHKD.
1	1-16-68	W. J. ...	...
2	1-17-68	...	...
3	1-18-68	...	...
4	1-19-68	...	...

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS FRACTIONS ANGLES			
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE			
SHEET OF			
DATE		DATE	
3/19/68		1-16-68	
DATE		DATE	
1-17-68		1-17-68	
DATE		DATE	
1-19-68		1-19-68	
DATE		DATE	
1-19-68		1-19-68	

\* MODULES ARE OPTIONAL



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REV.	DATE	BY	CHKD.
1	1-16-68	...	...
2	...	...	...
3	...	...	...
4	...	...	...
5	...	...	...
6	...	...	...
7	...	...	...
8	...	...	...

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	ARΦ (1)	B133	
	BRΦ (1)	1E22	
	ARΦ (1)	B133	
	BRΦ (1)	1E22	
	ARΦ (1)	B133	
	BRΦ (1)	1E22	
	ARΦ (1)	B133	
	BRΦ (1)	1E22	
	ARΦ (1)	B133	
	BRΦ (1)	1E22	

DRN. G.B.	DATE 12/29/65	 <b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. J. ...	DATE 1-16-68	
ENG. ...	DATE 1-16-68	TITLE
PRJ. ENG. ...	DATE 1-16-68	AR CONTROL LEVELS
PROD. ...	DATE 1-16-68	SIZE CODE
FIRST USED ON		NUMBER
		D BS KA10-0-ARC3
		REV.
		A



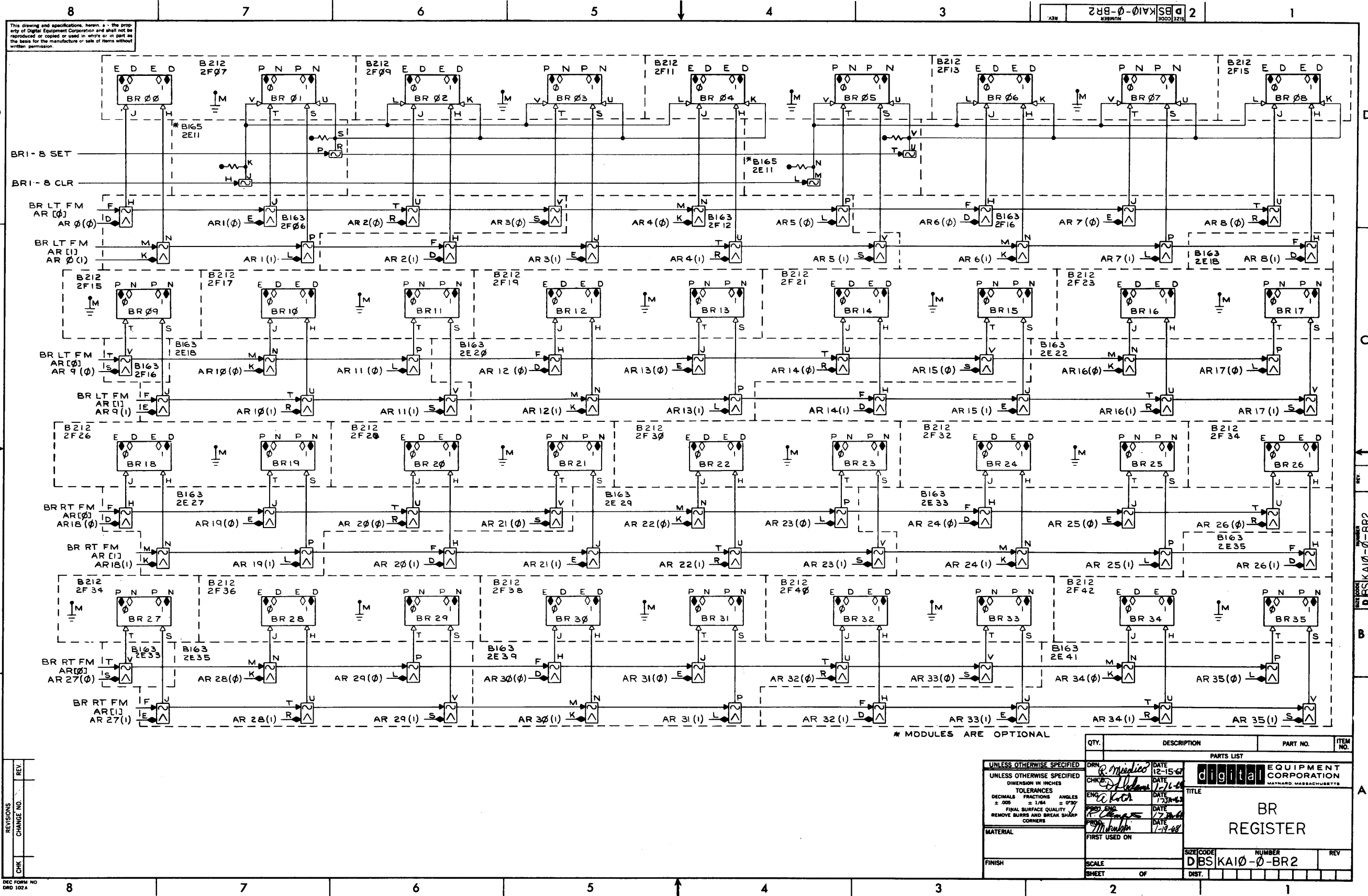








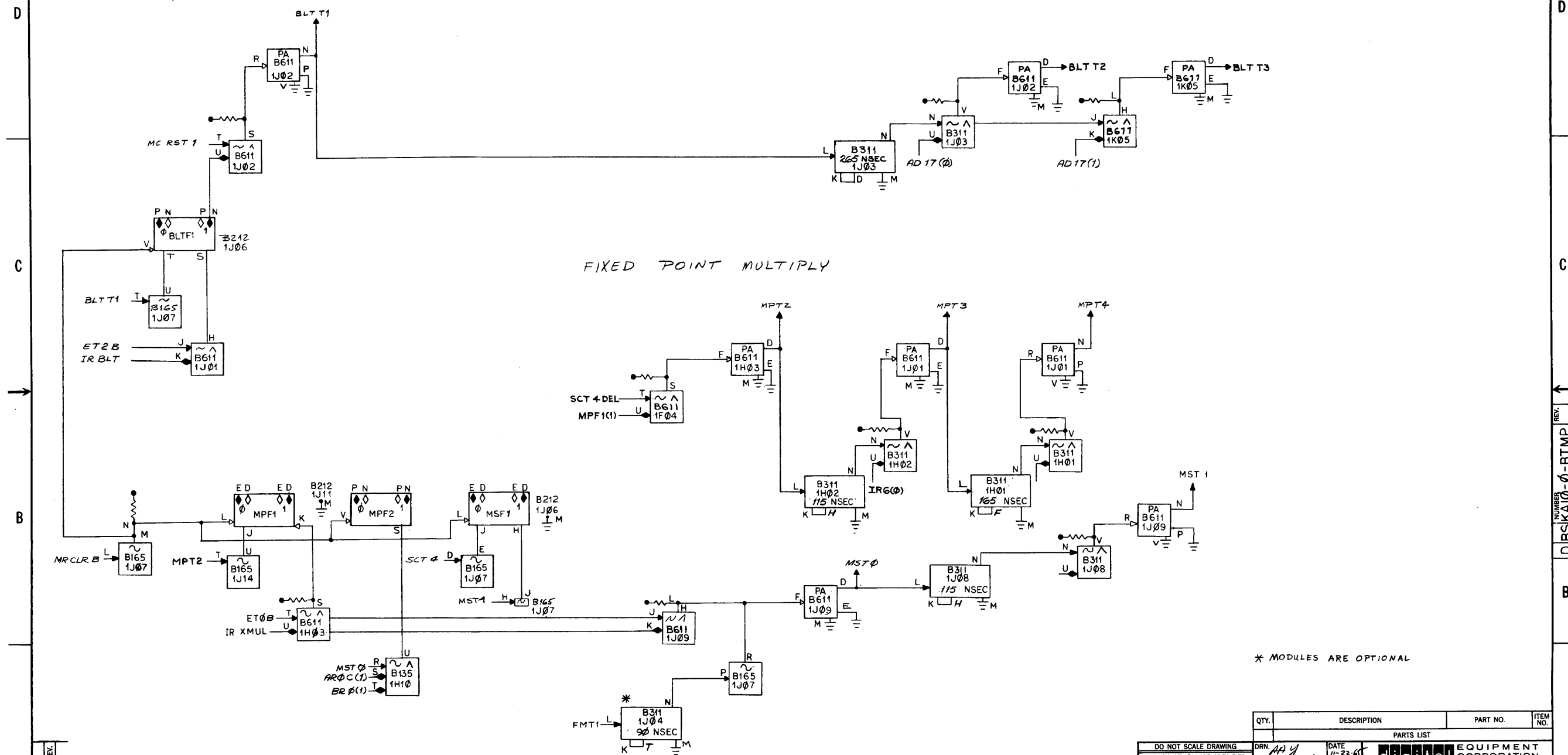




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BLOCK TRANSFER

FIXED POINT MULTIPLY



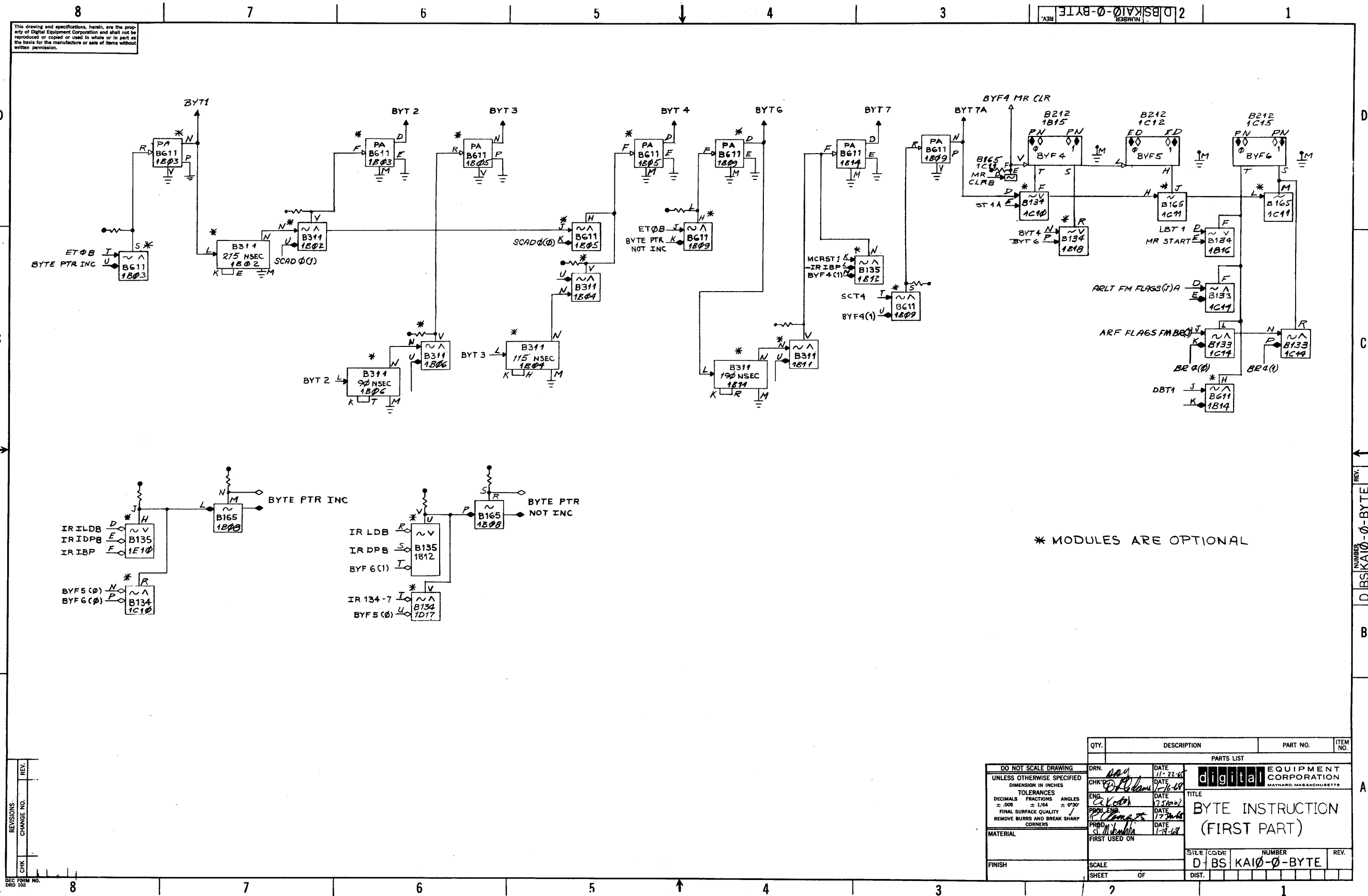
\* MODULES ARE OPTIONAL

REV.	CHANGE NO.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE <b>BLOCK TRANSFER AND MULTIPLY</b>			
MATERIAL		SIZE CODE	
FINISH		NUMBER	
SCALE		REV.	
SHEET		DIST.	

DO NOT SCALE DRAWING  
UNLESS OTHERWISE SPECIFIED  
DIMENSION IN INCHES  
TOLERANCES  
DECIMALS FRACTIONS ANGLES  
± .005 ± 1/64 ± 0°30'  
FINAL SURFACE QUALITY  
REMOVE BURRS AND BREAK SHARP CORNERS

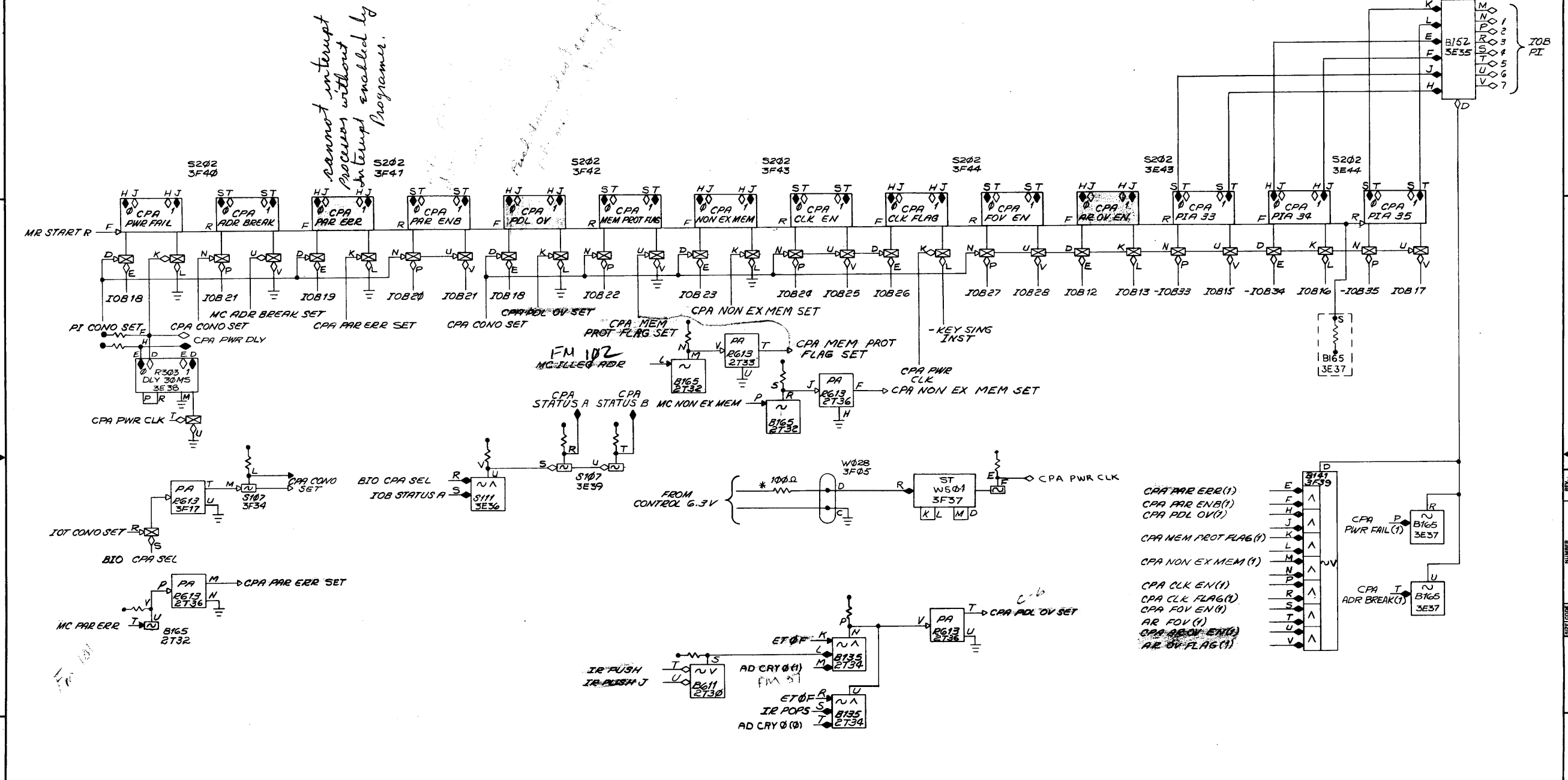
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REV.	
CHANGE NO.	
CHECK	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING			
DRN.	DATE	digital EQUIPMENT CORPORATION MAYFARL, MASSACHUSETTS	
CHK'D	DATE	TITLE	
ENG.	DATE	BYTE INSTRUCTION (FIRST PART)	
PROJ. ENG.	DATE	SIZE CODE NUMBER REV.	
PROD. MGR.	DATE	D BS KA10-0-BYTE	
MATERIAL		SHEET OF	
FINISH		DIST.	

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REV.	CHANGE NO.	BY	DATE
1	00033	ALLAN KENT	1/2/69
2	00035	KENT	2/1/69

\* NOTE:  
100Ω 1/2 WATT RESISTOR MOUNTED ON W028 MODULE

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	CPA PAR ERR (1)		
	CPA PAR ENB (1)		
	CPA PDL OV (1)		
	CPA MEM PROT FLAG (1)		
	CPA NON EX MEM (1)		
	CPA CLK EN (1)		
	CPA CLK FLAG (1)		
	CPA FOV EN (1)		
	AR FOV (1)		
	CPA ADR OV EN (1)		
	AR OV FLAG (1)		

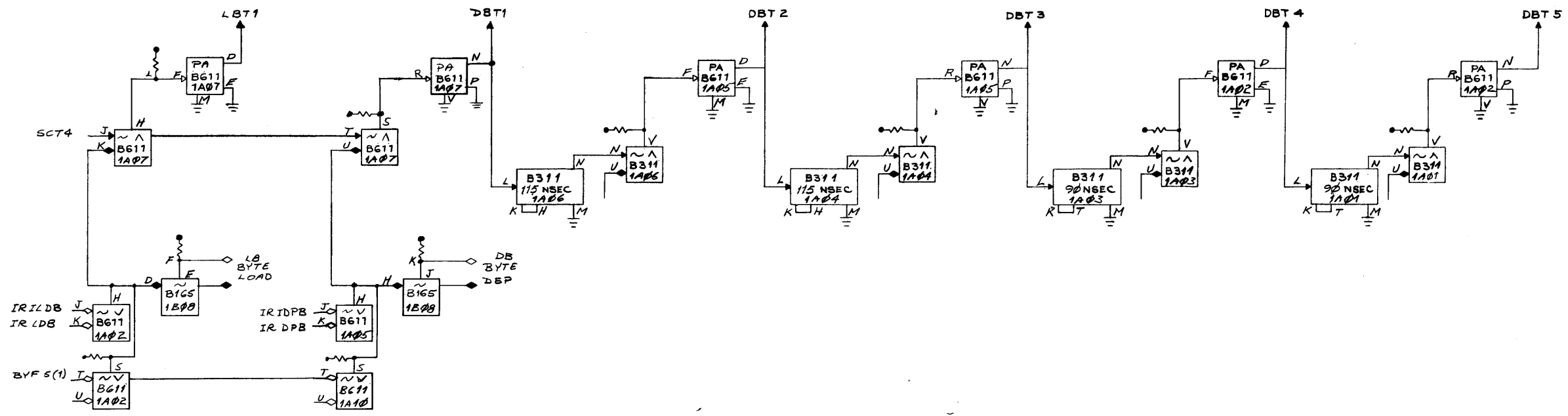
UNLESS OTHERWISE SPECIFIED	DRAWN BY	DATE
UNLESS OTHERWISE SPECIFIED	DATE	DATE
DIMENSION IN INCHES	DATE	DATE
TOLERANCES	DATE	DATE
DECIMALS FRACTIONS ANGLES	DATE	DATE
±.005 ± 1/64 ± 0°30'	DATE	DATE
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DATE	DATE
MATERIAL	DATE	DATE
FINISH	DATE	DATE

DRN	DATE	DATE
CHKD	DATE	DATE
ENG	DATE	DATE
PROJ	DATE	DATE
PRD	DATE	DATE
FIRST USED ON	DATE	DATE
SCALE	OF	OF
SHEET	OF	OF

PARTS LIST	
digital EQUIPMENT CORPORATION	MAYNARD, MASSACHUSETTS
TITLE	
ARITHMETIC PROCESS STATUS REGISTER	
SIZE CODE	NUMBER
D BS KA10-0-CPA	B
DIST.	

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REV. 1 2 3 4 5 6 7 8  
 SIZE CODE NUMBER  
 D BSKAI0-0-DBLB



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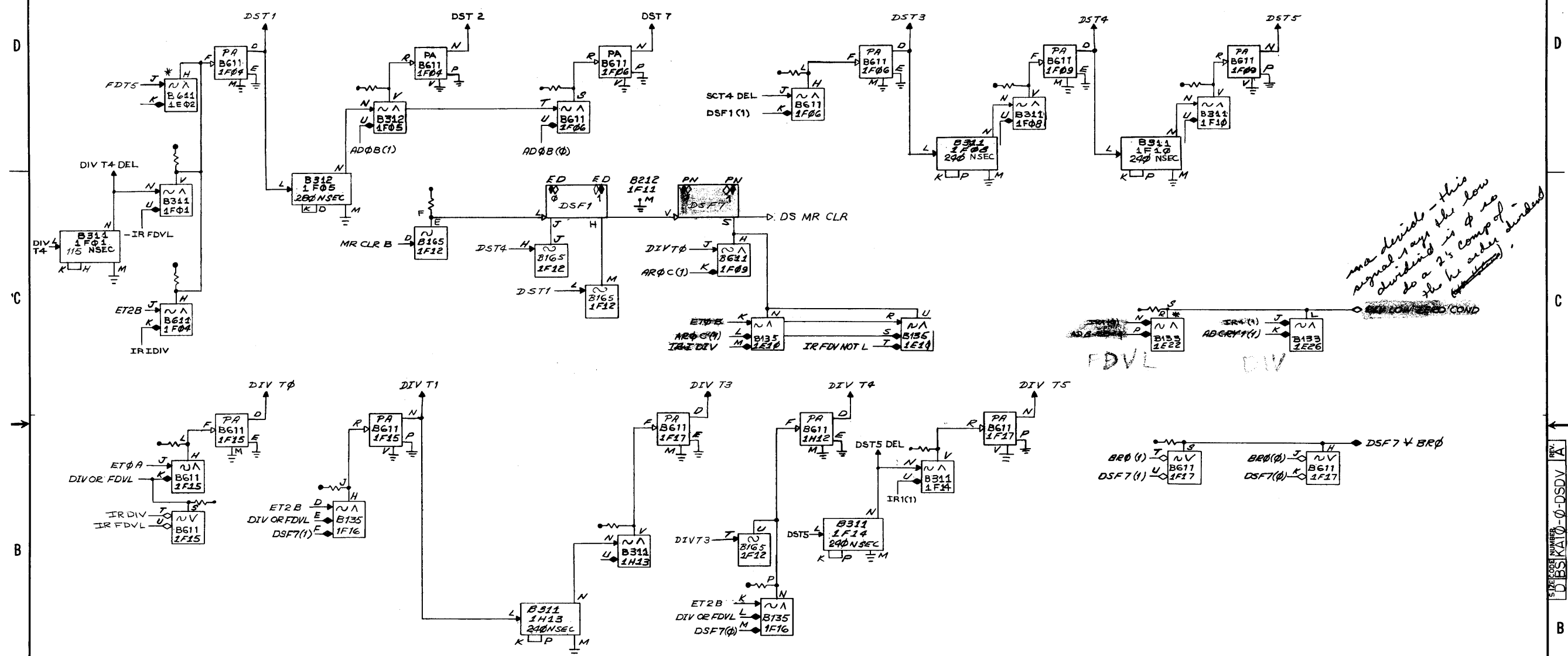
REV.	
CHG.	
NO.	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN. <i>11-22-68</i> DATE	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		CHK'D <i>[Signature]</i> DATE <i>1-6-68</i>	
TOLERANCES		ENG. <i>[Signature]</i> DATE <i>12-17-68</i>	
DECIMALS	FRACTIONS	ANGLES	DATE
± .005	± 1/64	± 0°30'	<i>12-30-68</i>
FINAL SURFACE QUALITY		PROB. ENG. <i>[Signature]</i> DATE <i>1-9-68</i>	
REMOVE BURRS AND BREAK SHARP CORNERS		PROD. <i>[Signature]</i> DATE	
MATERIAL		FIRST USED ON	
FINISH		SCALE	
SHEET		OF	
SIZE		CODE NUMBER	
D BSKAI0-0-DBLB		REV.	
DIST.			

**digital** EQUIPMENT CORPORATION  
 MAYNARD, MASSACHUSETTS

TITLE  
 BYTE INSTRUCTION DEPOSIT & LOAD (SECOND PART)

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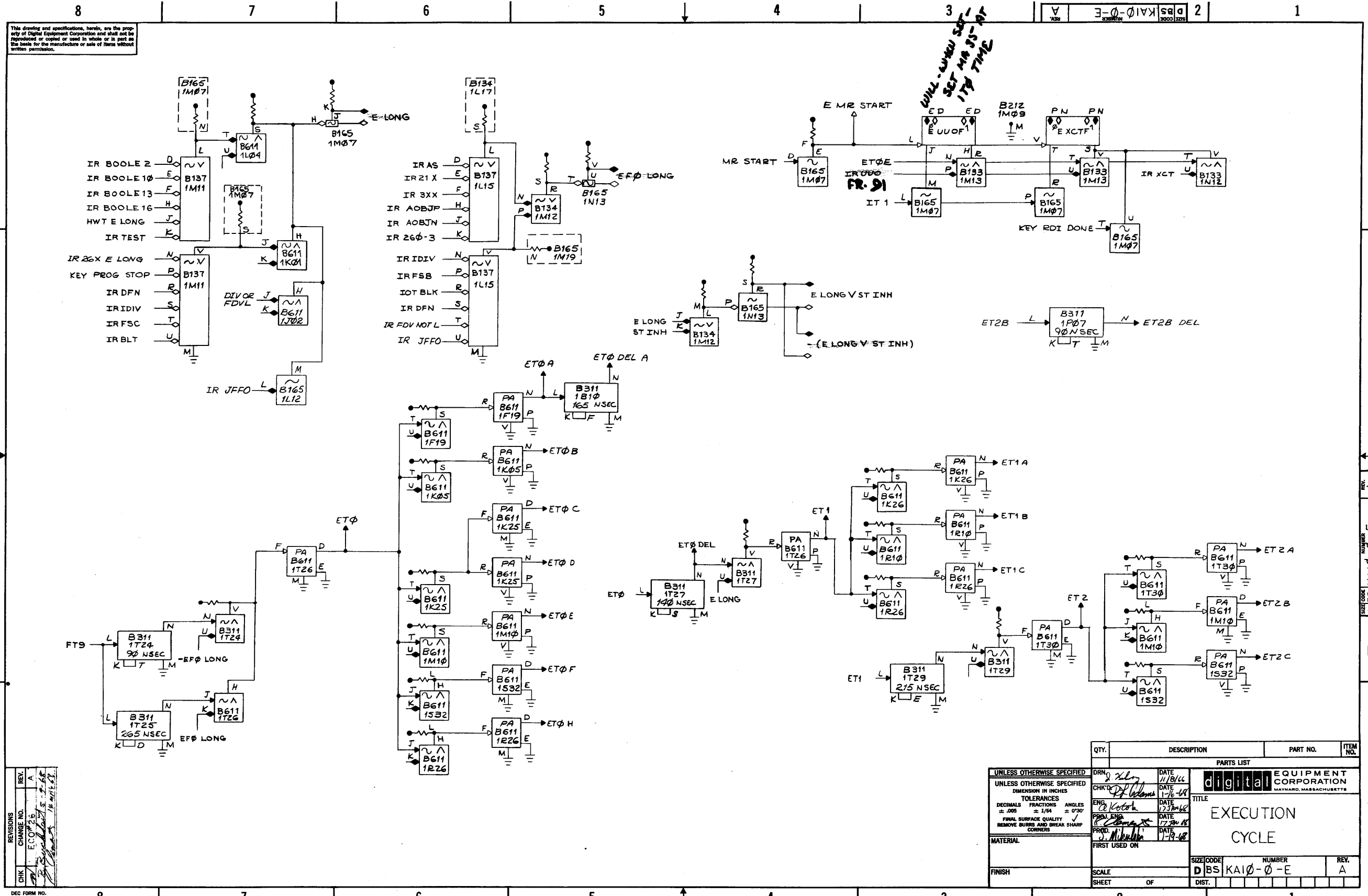


no divide - this signal says the low divided is 2's comp of the hi order dividend

\* MODULES ARE OPTIONAL

REV.	A
CHG.	FC 02/25
CHG.	FC 02/25
CHG.	FC 02/25

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE			
DIVIDE SUBROUTINE & FIXED DIVIDE			
SIZE CODE NUMBER REV.			
D. BS KA10-0-DSDV .A			
SCALE			
SHEET OF			
DIST.			

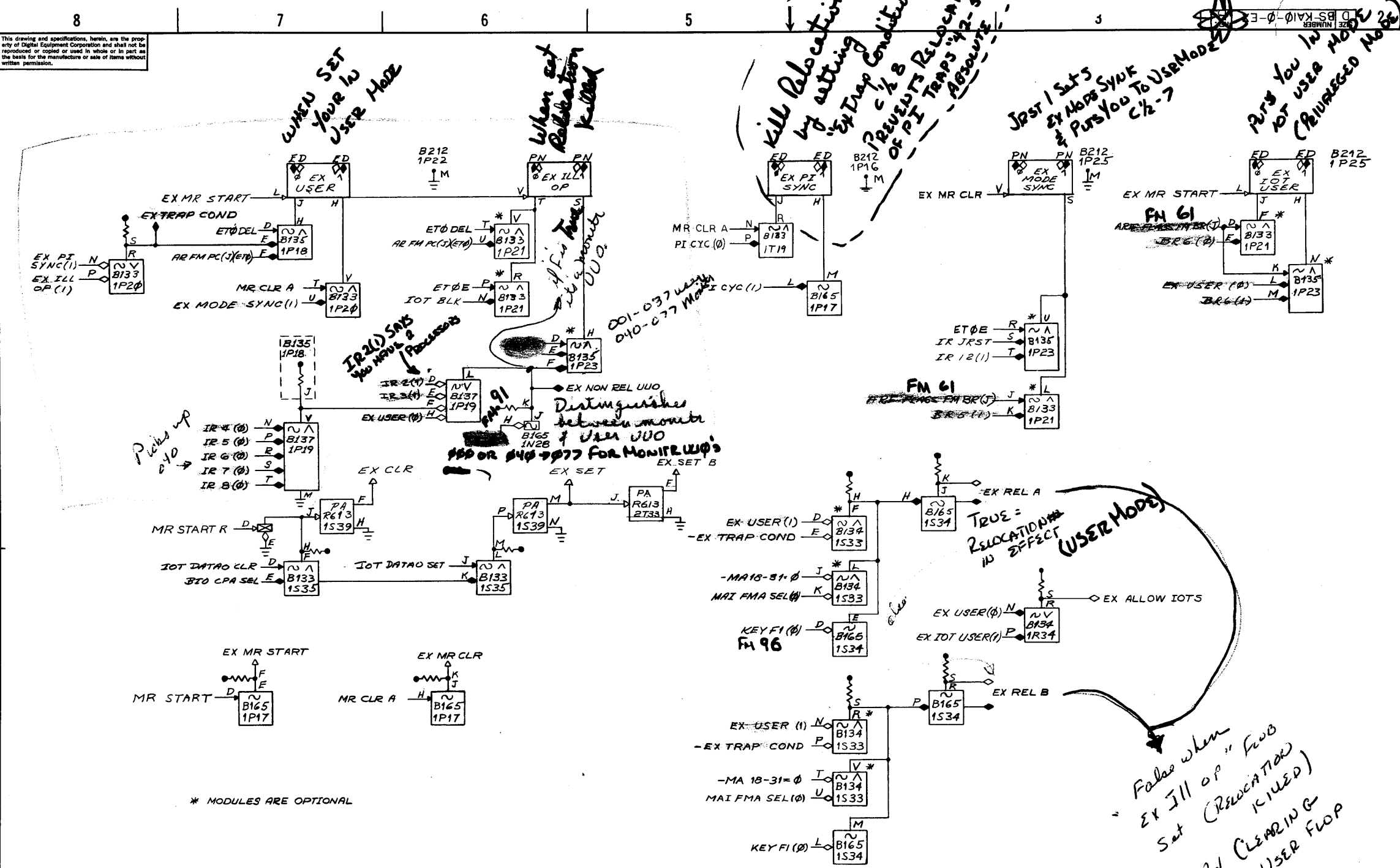


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REV.	CHG.	NO.	DATE
A	1	1	11/18/66
B	1	1	1-16-68
C	1	1	12/20/68
D	1	1	17/20/68
E	1	1	1-19-68

DEC FORM NO. DRD 102

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WHEN SET  
YOUR IN  
USER MODE

When set  
Relocation  
Killed

Kill Relocation  
by setting  
EX TRAP COND  
Prevents Relocation  
of PI TRAP 42-57  
Assuming

JRST / SETS  
EX MODE SYNC  
& Puts you in  
USER MODE  
CH-7

Puts you in  
USER MODE  
(MANAGED MODE)

IR 2(1) SAYS  
YOU HAVE 2  
PROCESSORS

001-037 WASH  
040-037 MONTE  
Distinguishes  
between monitor  
& user JUD  
100 or 140 977 FOR MONITOR

FM 61  
B133(1) = J  
B133(2) = K

TRUE =  
RELOCATION  
IN EFFECT  
(USER MODE)

False when  
EX ILL OP "FLOP"  
Set (RELOCATION  
KILLED)  
BY CLEARING  
USER FLOP

User Mode	EX USER	EX MODE SYNC
10 USER	EX IOT USER	EX MODE SYNC
	EX USER	

when in user mode you  
can only do a jrst 0,

\* MODULES ARE OPTIONAL

REV.	CHANGE NO.	DATE
A	ECO 29	5-20-68
B	ECO 29	5-20-68
C	ECO 29	5-20-68
D	ECO 29	5-20-68

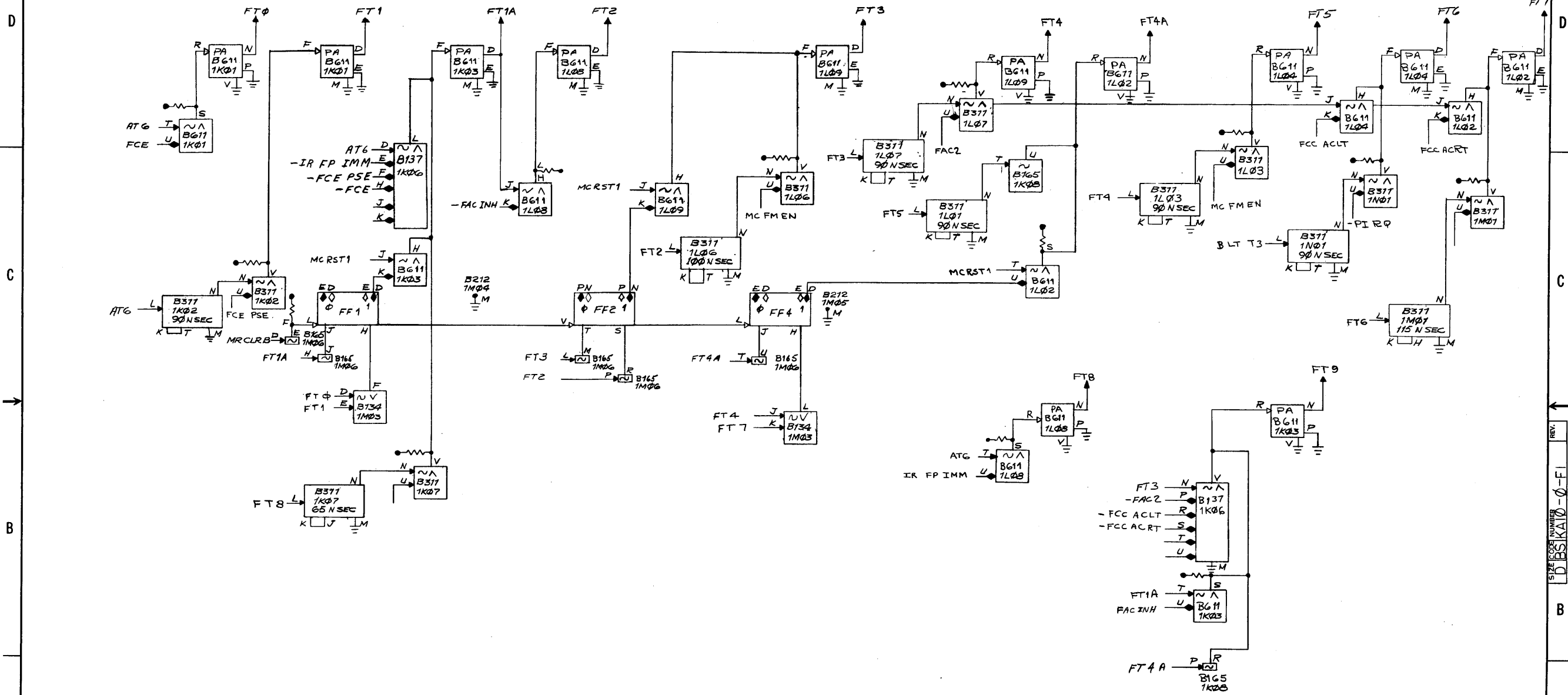
DO NOT SCALE DRAWING	DRN	DATE	1-16-68
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	CHK'D	DATE	1-16-68
TOLERANCES	ENG.	DATE	1-16-68
DECIMALS FRACTIONS ANGLES	PRBL. ENG.	DATE	1-16-68
± .005 ± 1/64 ± 0°30'	PROD.	DATE	1-16-68
FINAL SURFACE QUALITY	FIRST USED ON		
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE	SHEET	1 OF 1	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
EXECUTIVE CONTROL			
SCALE	SHEET	1 OF 1	



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REV. 13-0-010-01 2

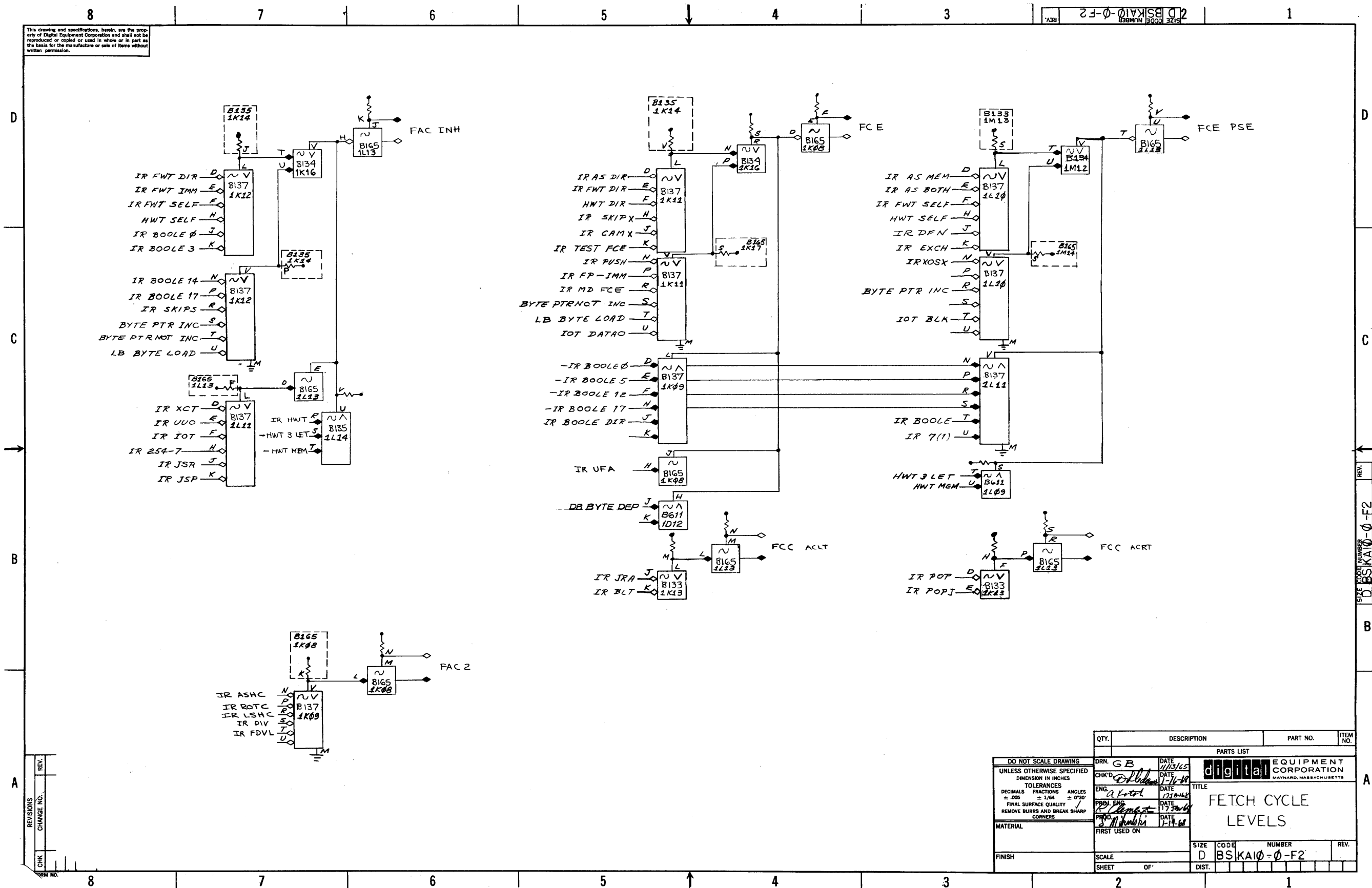


REV.	
CHANGE NO.	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ±.005 ± 1/64 ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS MATERIAL FIRST USED ON FINISH SCALE SHEET OF			
DRY DATE 11-15-68 CHK'D DATE 11-17-68 ENG. DATE 11-17-68 PRD. DATE 11-17-68 PROD. DATE 11-17-68		digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE FETCH CYCLE TIME PULSES SIZE CODE NUMBER D BS KAI0-0-F1 REV.	

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REV. 1  
D BSKA10-0-F2



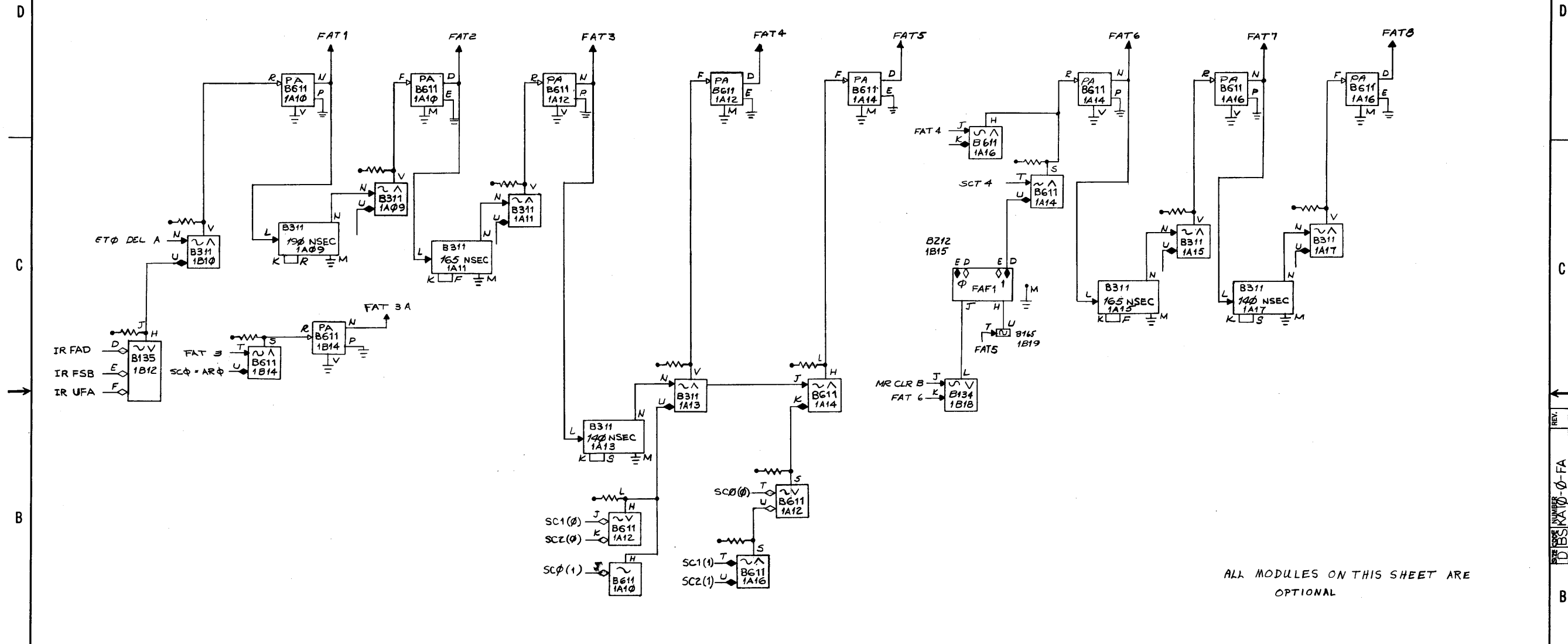
REV. 1  
D BSKA10-0-F2

REV.	CHANGE NO.	DESCRIPTION

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN. GB DATE 11/23/65	
UNLESS OTHERWISE SPECIFIED		CHK'D. [Signature] DATE 1-16-66	
DIMENSION IN INCHES		ENG. [Signature] DATE 1-16-66	
TOLERANCES		PROJ. ENG. [Signature] DATE 1-17-66	
DECIMALS FRACTIONS ANGLES		PROD. [Signature] DATE 1-19-66	
±.005 ±.004 ±.030		FIRST USED ON	
FINAL SURFACE QUALITY 1		MATERIAL	
REMOVE BURRS AND BREAK SHARP CORNERS		FINISH	
TITLE		SIZE CODE NUMBER REV.	
FETCH CYCLE LEVELS		D BSKA10-0-F2	
SCALE		SHEET OF	

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REV. 2 D BSKA10-0-FA



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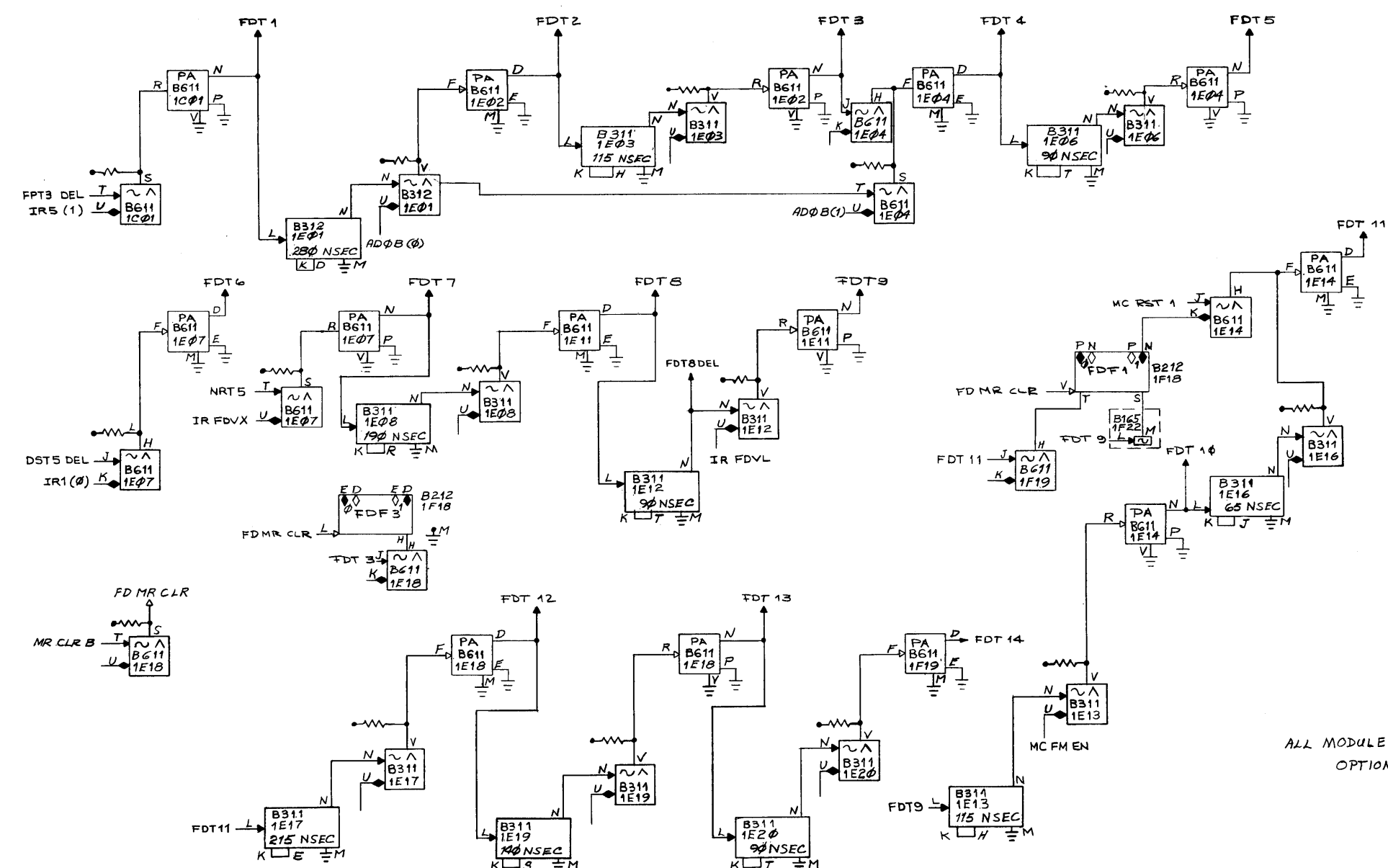
REV.	
CHANGE NO.	
CHK	
DEC FORM NO.	102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN: <i>[Signature]</i>	DATE: 11-16-68
UNLESS OTHERWISE SPECIFIED		CHK'D: <i>[Signature]</i>	DATE: 1-16-69
DIMENSION IN INCHES		ENG: <i>[Signature]</i>	DATE: 17 JAN 69
TOLERANCES		PROG. ENG: <i>[Signature]</i>	DATE: 17 JAN 69
DECIMALS FRACTIONS ANGLES		PRD: <i>[Signature]</i>	DATE: 1-19-69
= .005 = 1/64 = 0°30'		FIRST USED ON	
FINAL SURFACE QUALITY		SCALE	
REMOVE BURRS AND BREAK SHARP CORNERS		SHEET OF	
MATERIAL		SIZE CODE NUMBER REV.	
FINISH		D BSKA10-0-FA	

digital EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

TITLE  
FLOATING ADD INSTRUCTION

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REV.	
CHANGE NO.	
CHK	

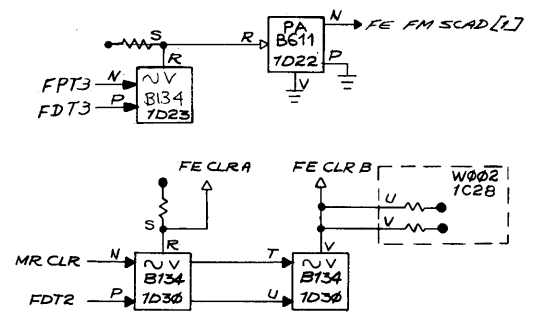
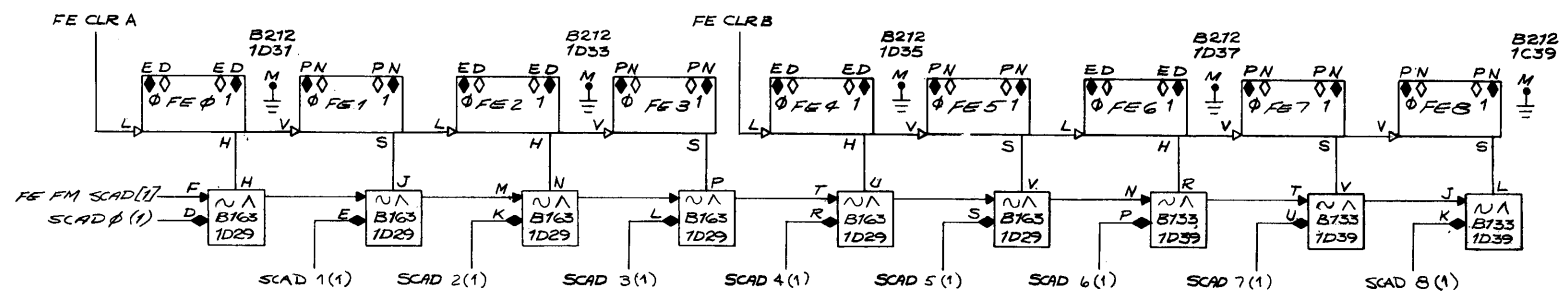
DEC FORM NO. DRD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN: <i>[Signature]</i> DATE: 8/11/68	
UNLESS OTHERWISE SPECIFIED		CHK: <i>[Signature]</i> DATE: 7/16/68	
DIMENSION IN INCHES		TITLES	
TOLERANCES		digital EQUIPMENT CORPORATION	
DECIMALS FRACTIONS ANGLES		MAYNARD, MASSACHUSETTS	
± .005 ± 1/64 ± 0°30'		TITLE	
FINAL SURFACE QUALITY		PROJ. ENG. DATE: 7/27/68	
REMOVE BURRS AND BREAK SHARP CORNERS		FRST. DATE: 7/27/68	
MATERIAL		FRST USED ON	
FINISH		SCALE	
SHEET		OF	
DIST.		NUMBER	
REV.		REV.	

REV. 1 D BSKAI0-0-FDV

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DBSKA10-0-FE 2



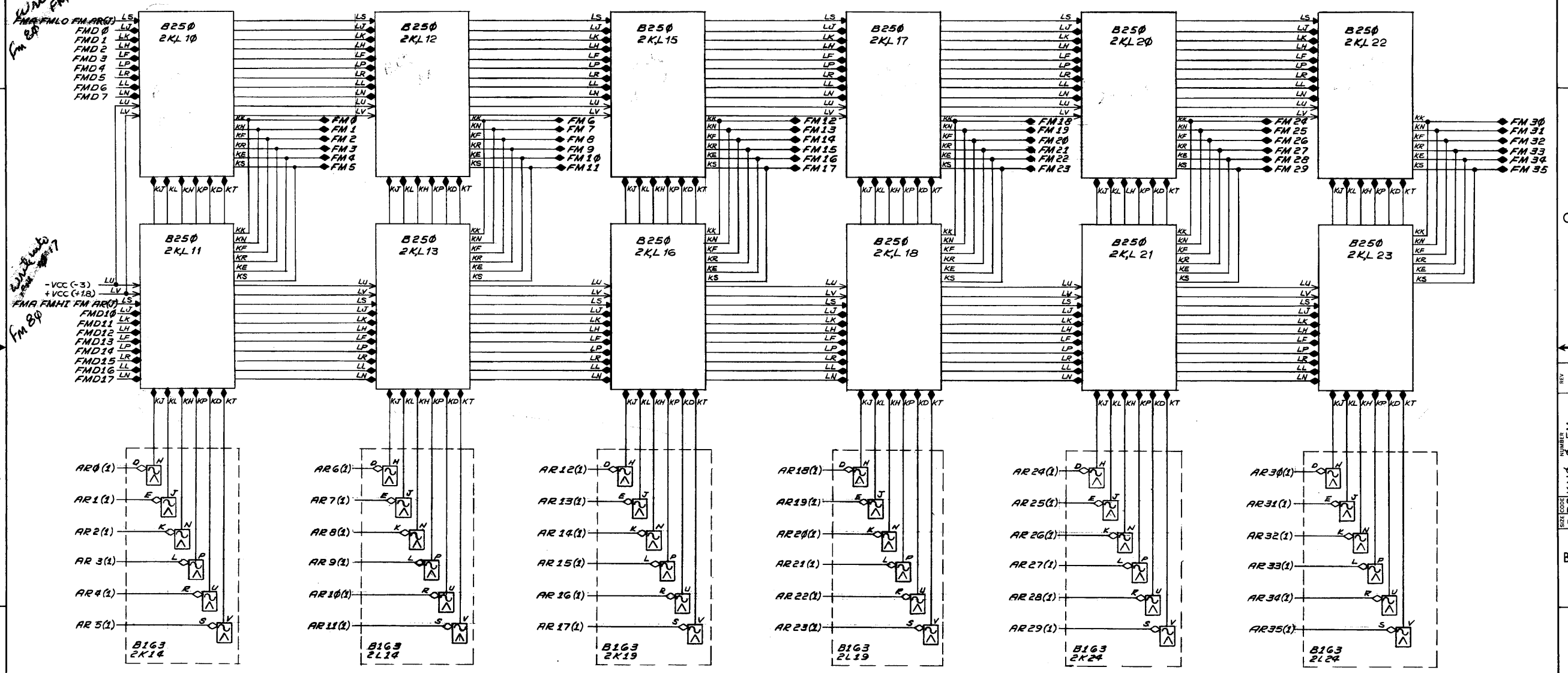
ALL MODULES ON THIS SHEET ARE OPTIONAL

REV.	
CHG	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		<b>digital</b> EQUIPMENT CORPORATION MATYARD, MASSACHUSETTS	
DRN.	DATE	TITLE	
CHK	DATE	FLOATING EXPONENT REG & CONTROL	
ENG	DATE	MATERIAL	
PRG	DATE	FINISH	
SCALE	SHEET OF	SIZE CODE	NUMBER
		DBSKA10-0-FE	REV.

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NOTE: B250 GNDS  
KC, KM, KV, LC, LM, LT



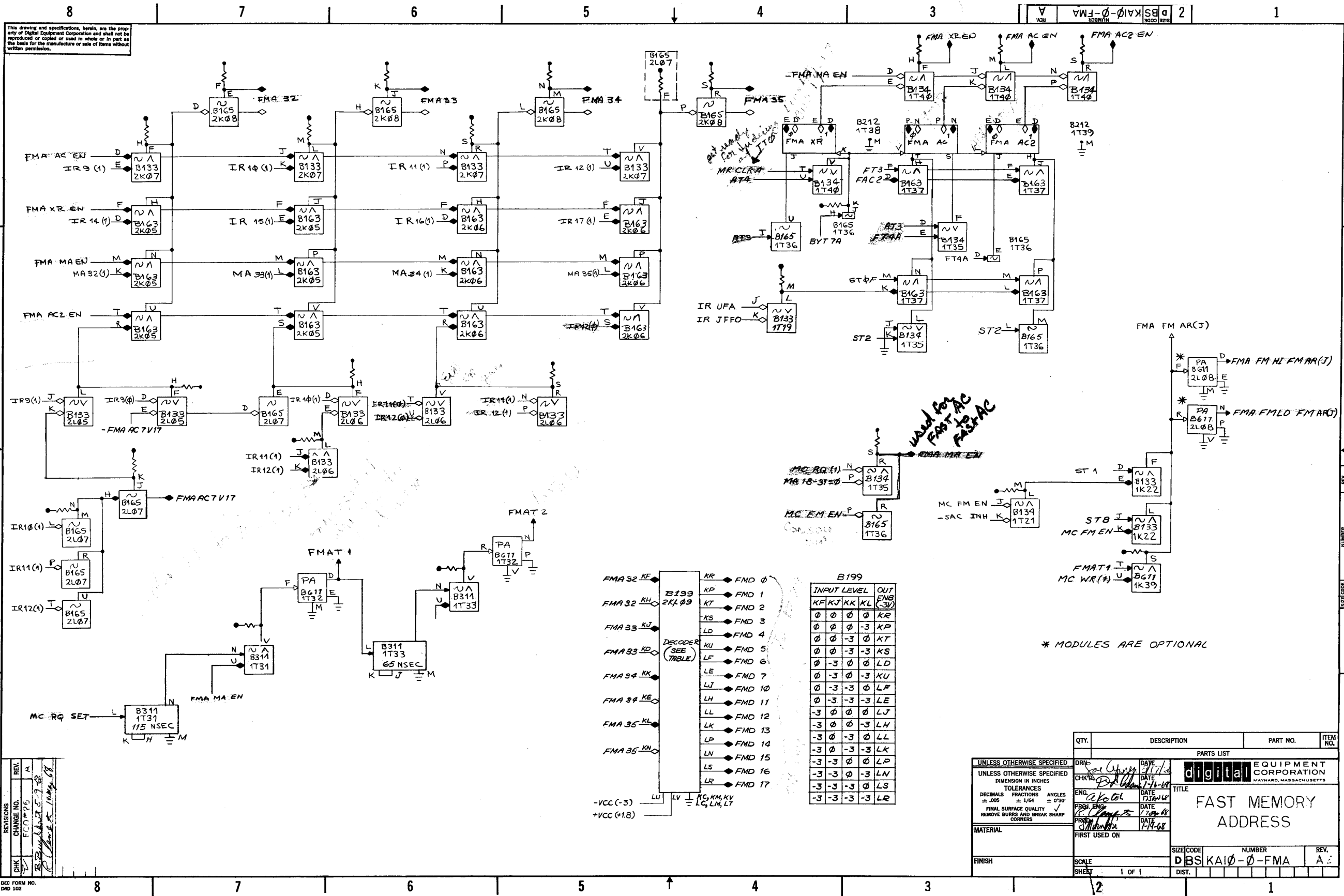
NOTE: ALL MODULES ON THIS SHEET ARE OPTIONAL

REV.	CHG.	NO.

DEC FORM NO. DRD 102

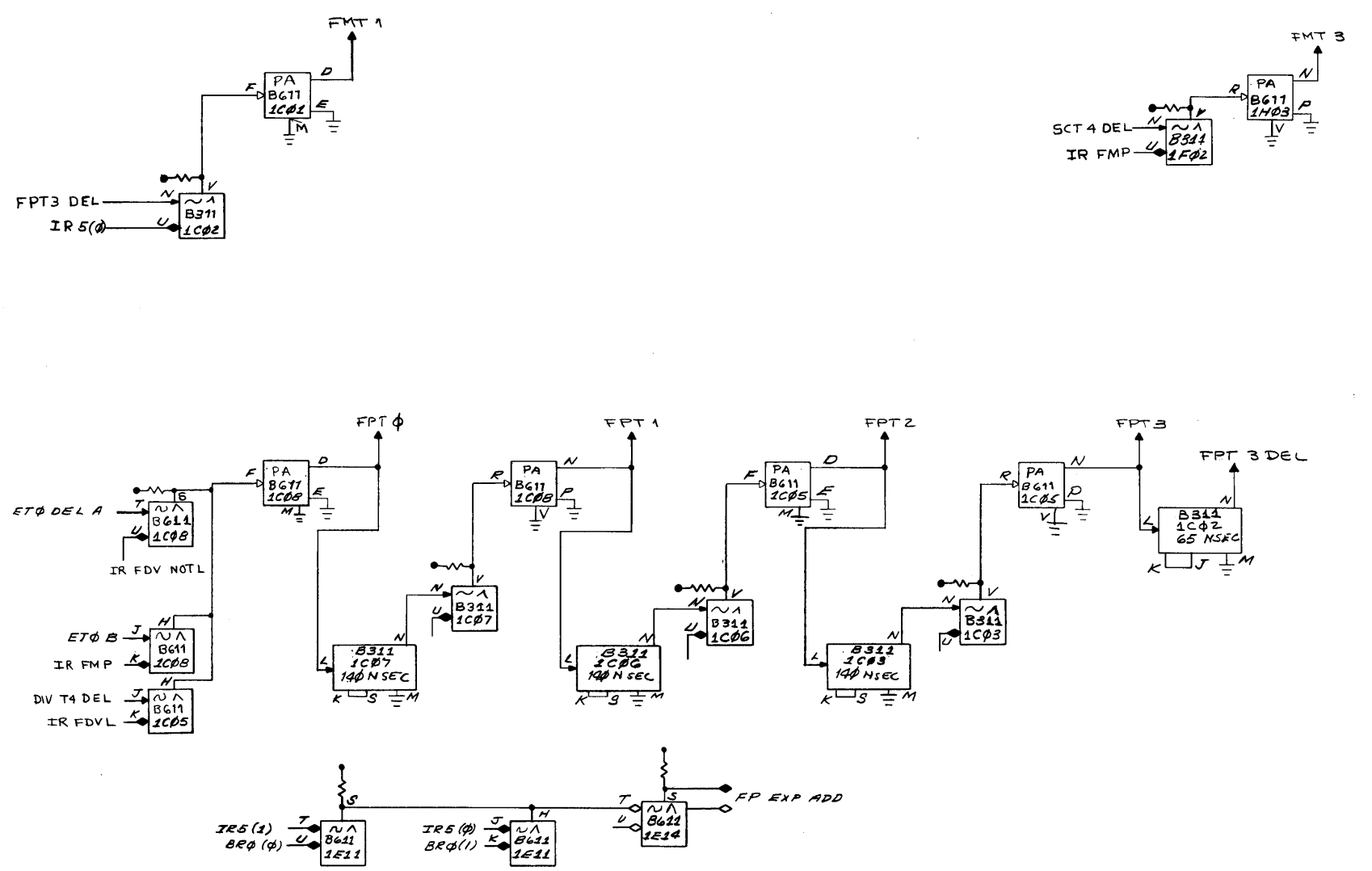
QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS FRACTIONS ANGLES			
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
FIRST USED ON			
SCALE			
SHEET OF			
DIST.			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE FAST MEMORY			
SIZE CODE NUMBER REV.			
DBSKAI0-0-FM			

REV. NUMBER DBSKAI0-0-FM



*FM = 0-17  
 Copying it doesn't  
 advance to Ad.*

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NOTE: ALL MODULES ON THIS SHEET ARE OPTIONAL

REV.	
CHANGE NO.	
CHK	

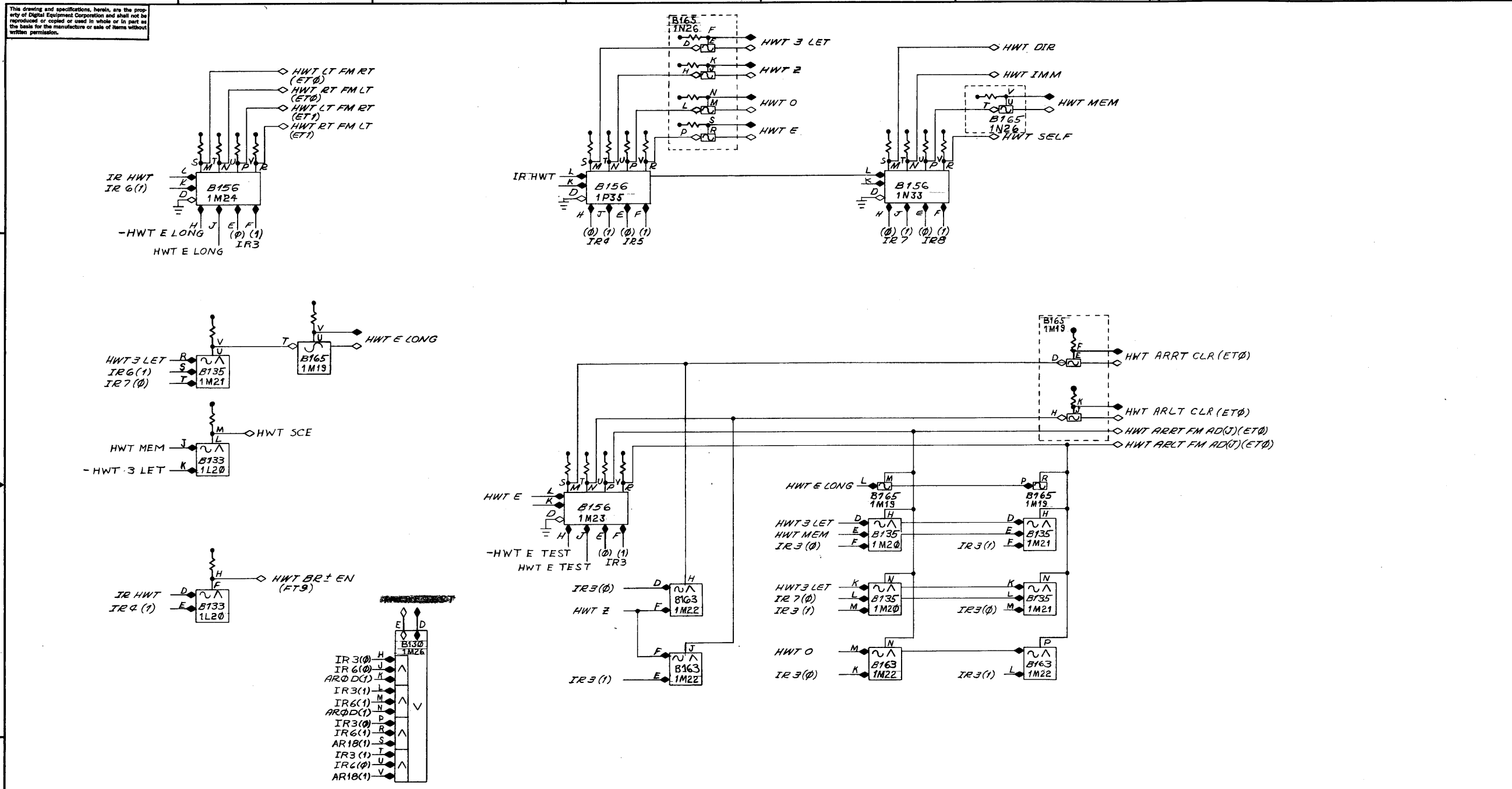
DEC FORM NO. 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DATE	
UNLESS OTHERWISE SPECIFIED		DATE	
DIMENSION IN INCHES		DATE	
TOLERANCES		DATE	
DECIMALS	FRACTIONS	ANGLES	DATE
±.005	± 1/64	± 0°30'	DATE
FINAL SURFACE QUALITY		DATE	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE	
MATERIAL		DATE	
FIRST USED ON		DATE	
FINISH		DATE	
SCALE		DATE	
SHEET OF		DATE	
DIST.		DATE	
TITLE		DATE	
FP EXP CALC.		DATE	
FLOATING MULTIPLY		DATE	
SIZE CODE		NUMBER	
D BSKAIΦ-Φ-FPFM		REV.	
DIST.		REV.	

REV. NUMBER D BSKAIΦ-Φ-FPFM



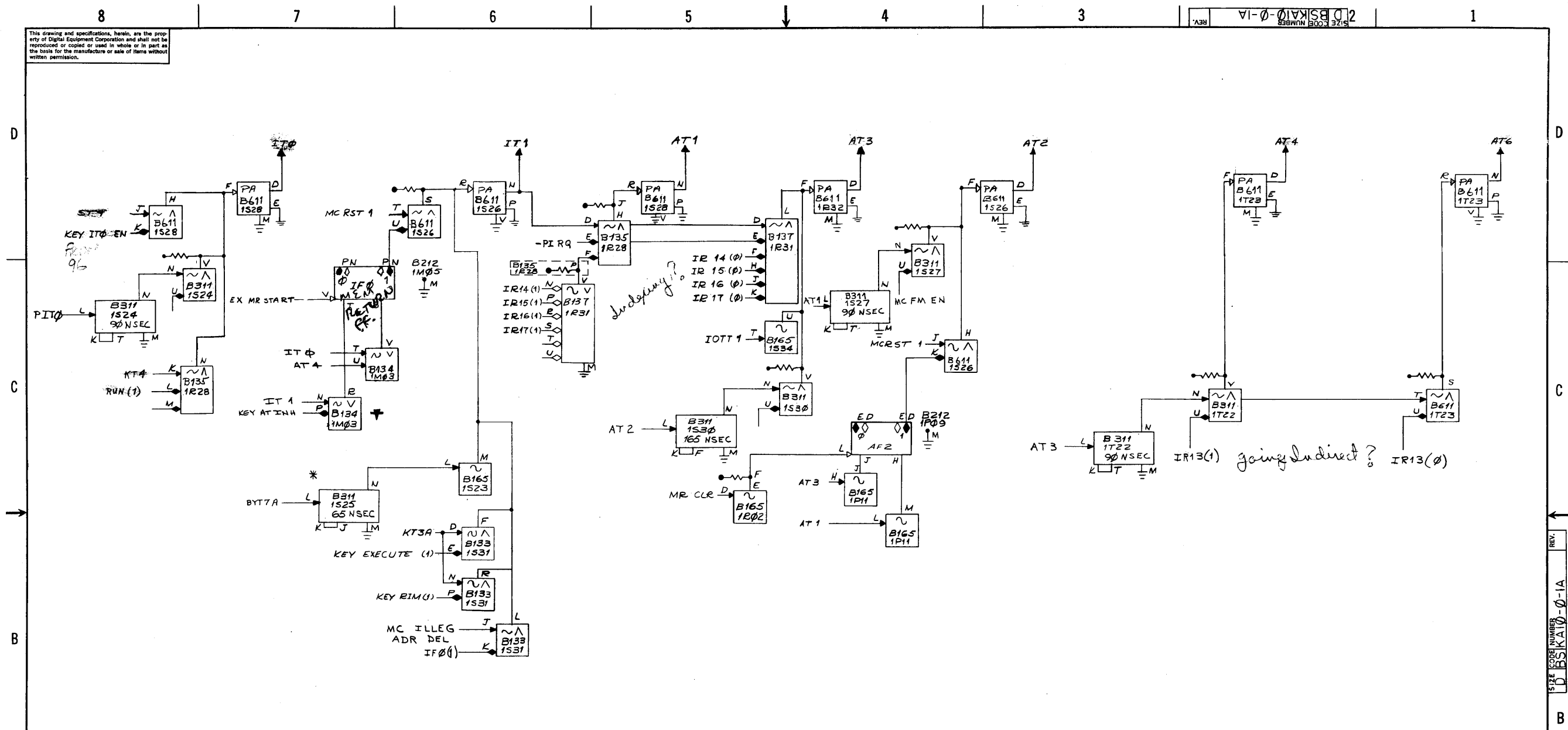
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REV.	CHANGE NO.
CHK	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DRN. <i>Lee Ayres</i>	DATE 7-28-66	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D <i>Debra</i>	DATE 7-16-66	TITLE <b>HALF WORD TRANSFER</b>	
ENG. <i>W. E. ...</i>	DATE 7-28-66	MATERIAL	
PROJ. ENG. <i>R. ...</i>	DATE 7-28-66	FINISH	
PROJ. MGR. <i>M. ...</i>	DATE 7-19-66	SCALE	
FIRST USED ON		SIZE CODE	NUMBER
SHEET 1 OF 1		DIST.	

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NOTE: 1. THIS IS A NOR (KEY AT INH STOPS THE TIME CHAIN)

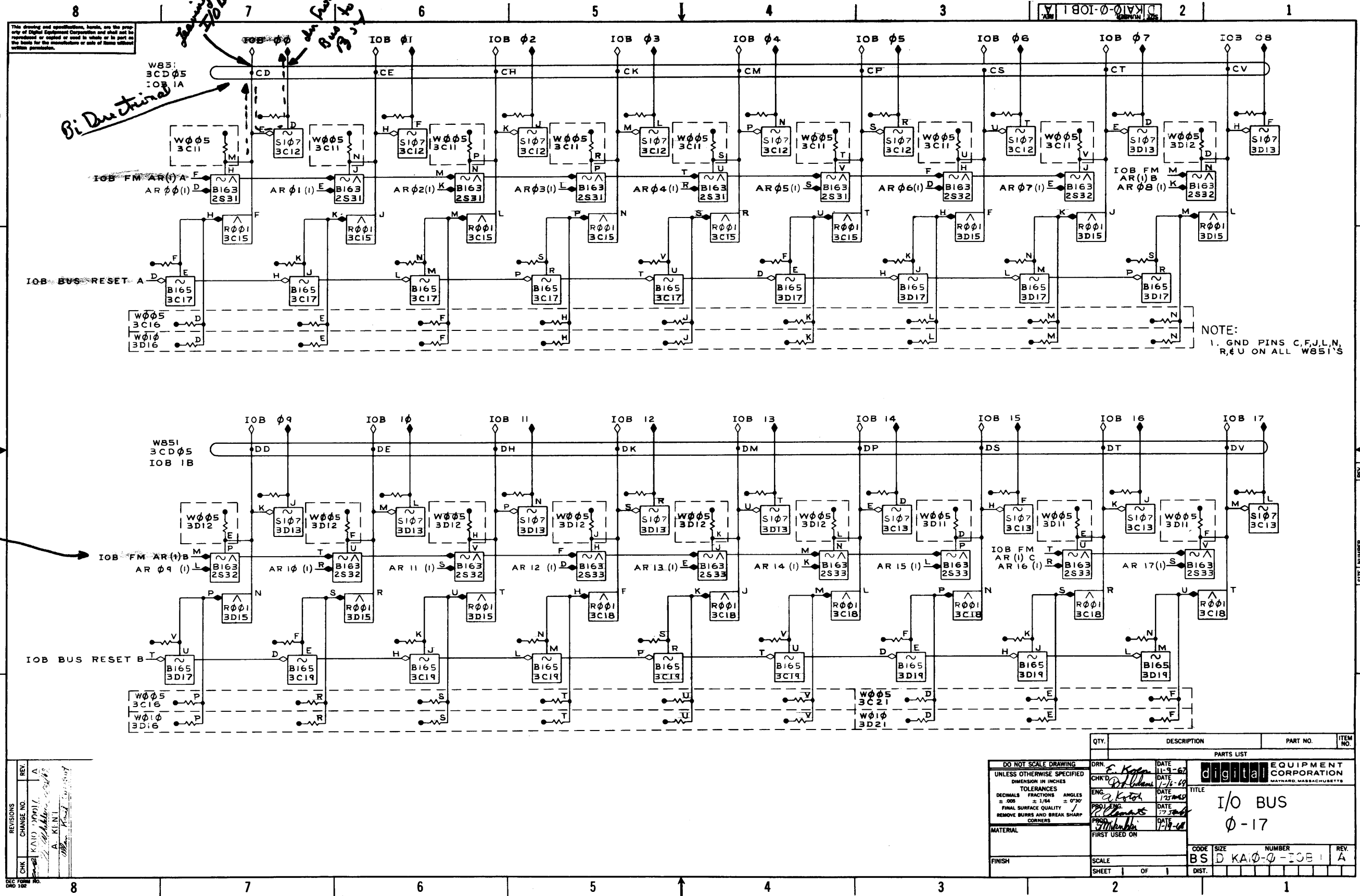
\* MODULES ARE OPTIONAL

REV.	
CHANGE NO.	
CHK	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN: <i>A. Yankovsky</i> DATE: <i>11-12-66</i>	
UNLESS OTHERWISE SPECIFIED		CHK: <i>D. B. Kato</i> DATE: <i>1-16-68</i>	
DIMENSION IN INCHES		ENG: <i>C. Kato</i> DATE: <i>17 Jan 68</i>	
TOLERANCES		PROJ. ENG: <i>D. B. Kato</i> DATE: <i>17 Jan 68</i>	
DECIMALS FRACTIONS ANGLES		PROD. <i>S. M. Kato</i> DATE: <i>2-19-68</i>	
± .005 ± 1/64 ± 0°30'		FIRST USED ON	
FINAL SURFACE QUALITY		SCALE	
REMOVE BURRS AND BREAK SHARP CORNERS		SHEET OF	
MATERIAL		SIZE CODE NUMBER REV.	
FINISH		D BS KA10-0-IA	

**digital** EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

TITLE  
**INSTRUCTION & ADDRESS CYCLES**



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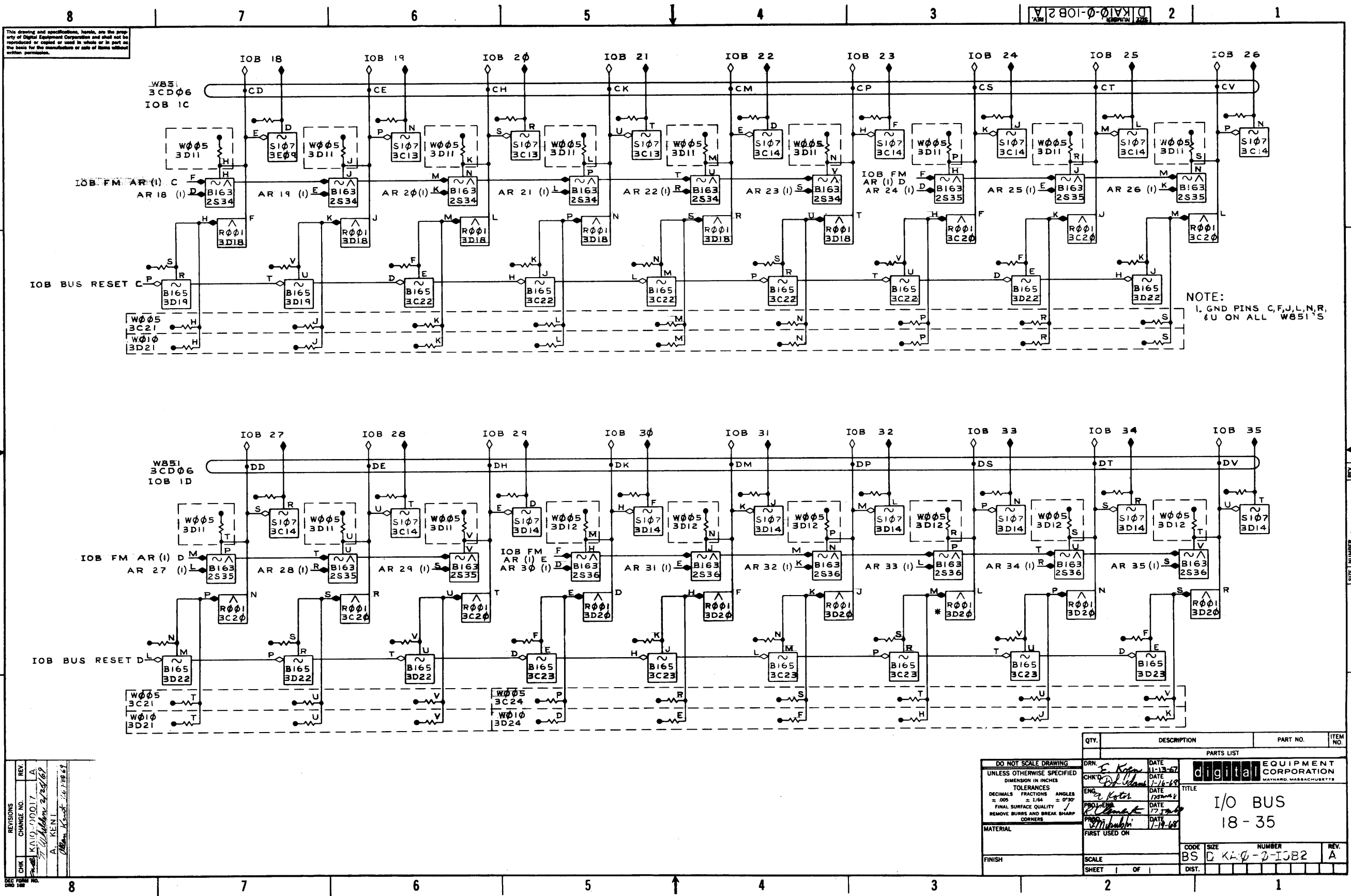
*Handwritten:* Bi Directional  
*Handwritten:* leading for I/O bus  
*Handwritten:* from I/O bus to AR

*Handwritten:* SAYS: INFORMATION OUT ON I/O BUS

NOTE:  
 1. GND PINS C,F,J,L,N,  
 R,&U ON ALL W851'S

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN: E. Kagan DATE: 11-9-67	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		CHK'D: [Signature] DATE: 1-16-68	
TOLERANCES		ENGR: [Signature] DATE: 1/27/67	
DECIMALS	FRACTIONS	ANGLES	PROJ. ENG: [Signature] DATE: 7/2/67
± .000	± 1/64	± 0°30'	PROD: [Signature] DATE: 1/19-68
FINAL SURFACE QUALITY /		FIRST USED ON:	
REMOVE BURRS AND BREAK SHARP CORNERS		TITLE: I/O BUS	
MATERIAL:		CODE: BS	
FINISH:		SIZE: D	
SCALE: SHEET 1 OF 1		NUMBER: KA.0-0-IOB 1	
		REV. A	
		DIST.	

REV.	CHANGE NO.	REVISIONS
1	A	KAGAN
2	B	KAGAN
3	C	KAGAN
4	D	KAGAN
5	E	KAGAN
6	F	KAGAN
7	G	KAGAN
8	H	KAGAN



REV.	CHANGE NO.	DATE
1	1	11-13-67
2	1	1-16-68
3	1	12-11-68
4	1	1-19-68

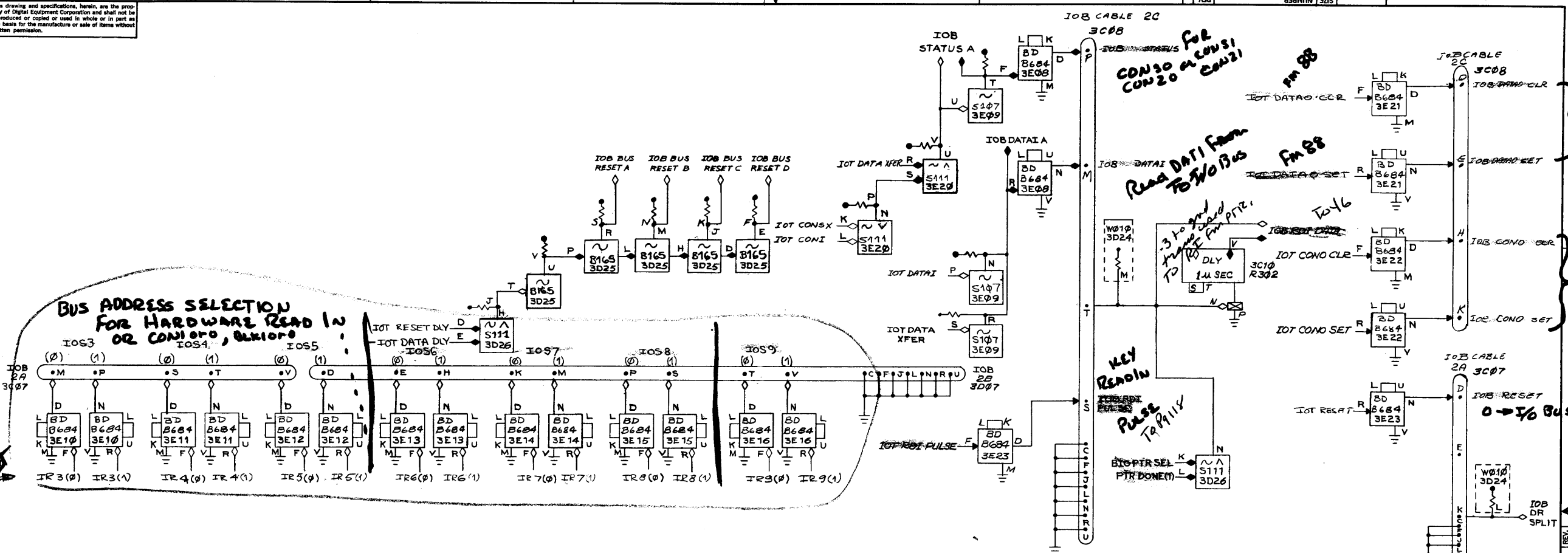
QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN: E. Kagan	DATE: 11-13-67
UNLESS OTHERWISE SPECIFIED		CHKD: D. J. Adams	DATE: 1-16-68
DIMENSION IN INCHES		ENG: E. Kagan	DATE: 12-11-68
TOLERANCES		PROV: R. Adams	DATE: 1-19-68
DECIMALS FRACTIONS ANGLES		PROD: M. Kagan	DATE: 1-19-68
± .005 ± 1/64 ± 0°30'		FIRST USED ON	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE		CODE	SIZE
SHEET 1 OF 1		BS	D
		NUMBER	REV.
		DIST.	A

digital EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

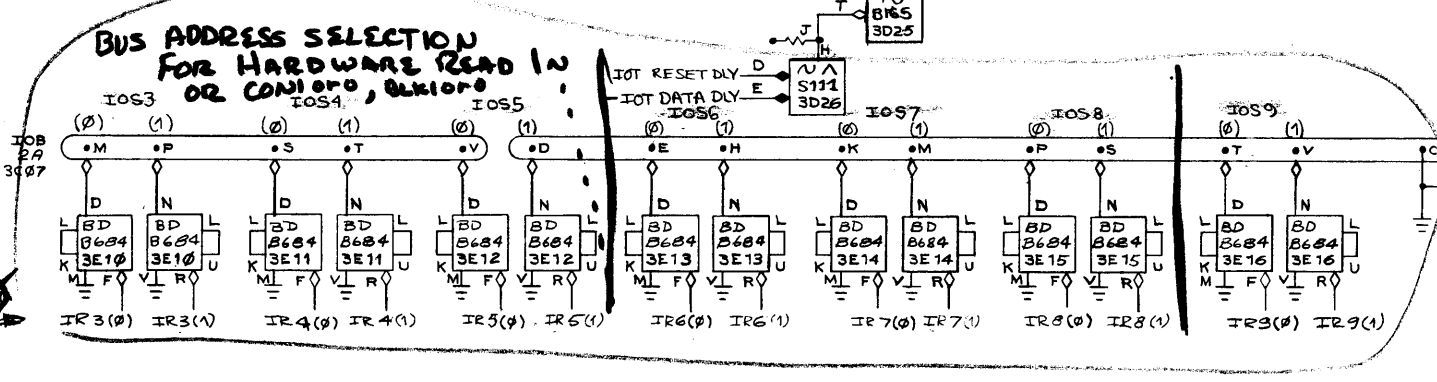
TITLE  
I/O BUS  
18-35

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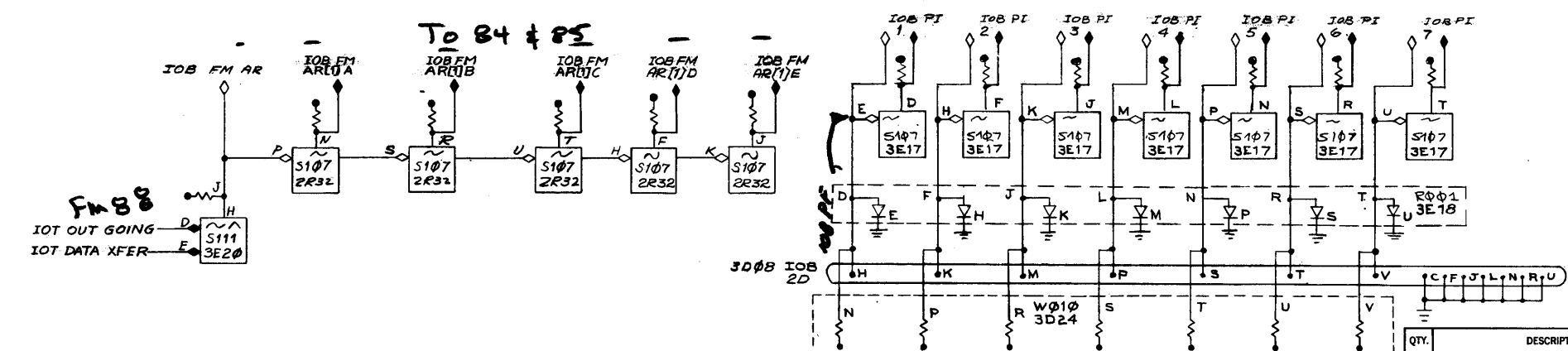
*TO BUS Drivers*



*OUT TO I/O BUS ON DATA*  
*OUT TO I/O BUS ON CONSO*



**FROM I/O DEVICES**



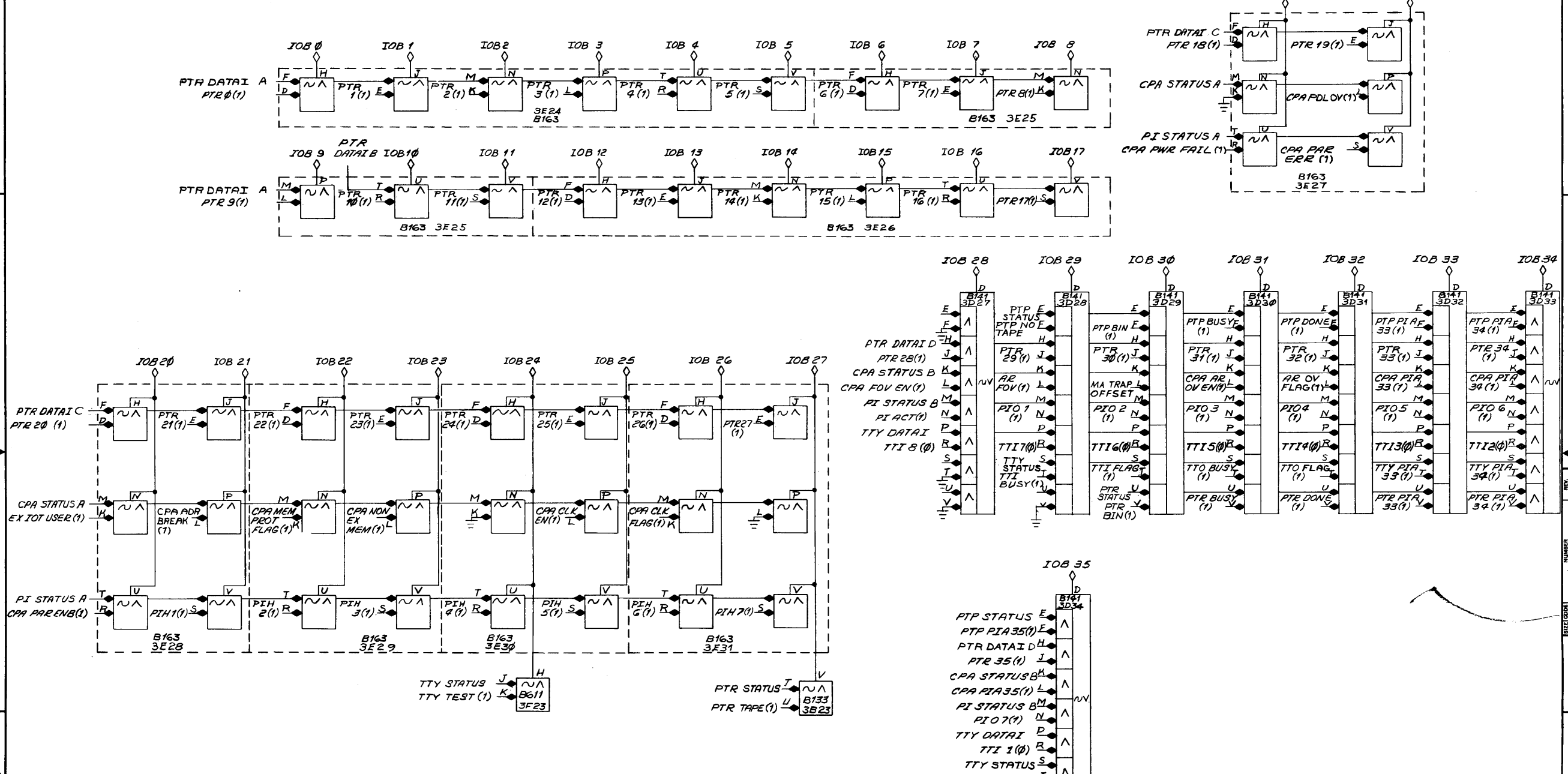
REV.	CHANGE NO.	DATE
A		

CHK	REV.	DATE

DO NOT SCALE DRAWING	DRN. <i>AAV</i>	DATE <i>2-65</i>
UNLESS OTHERWISE SPECIFIED	CHKD. <i>[Signature]</i>	DATE <i>1-16-68</i>
DIMENSION IN INCHES	ENG. <i>[Signature]</i>	DATE <i>7/20/65</i>
TOLERANCES	PROB. ENG. <i>[Signature]</i>	DATE <i>7-20-68</i>
DECIMALS FRACTIONS ANGLES	PROD. <i>[Signature]</i>	DATE <i>1-14-68</i>
± .005 ± 1/64 ± 0°30'	FIRST USED ON	
FINAL SURFACE QUALITY		
REMOVE BURRS AND BREAK SHARP CORNERS		
MATERIAL		
FINISH		



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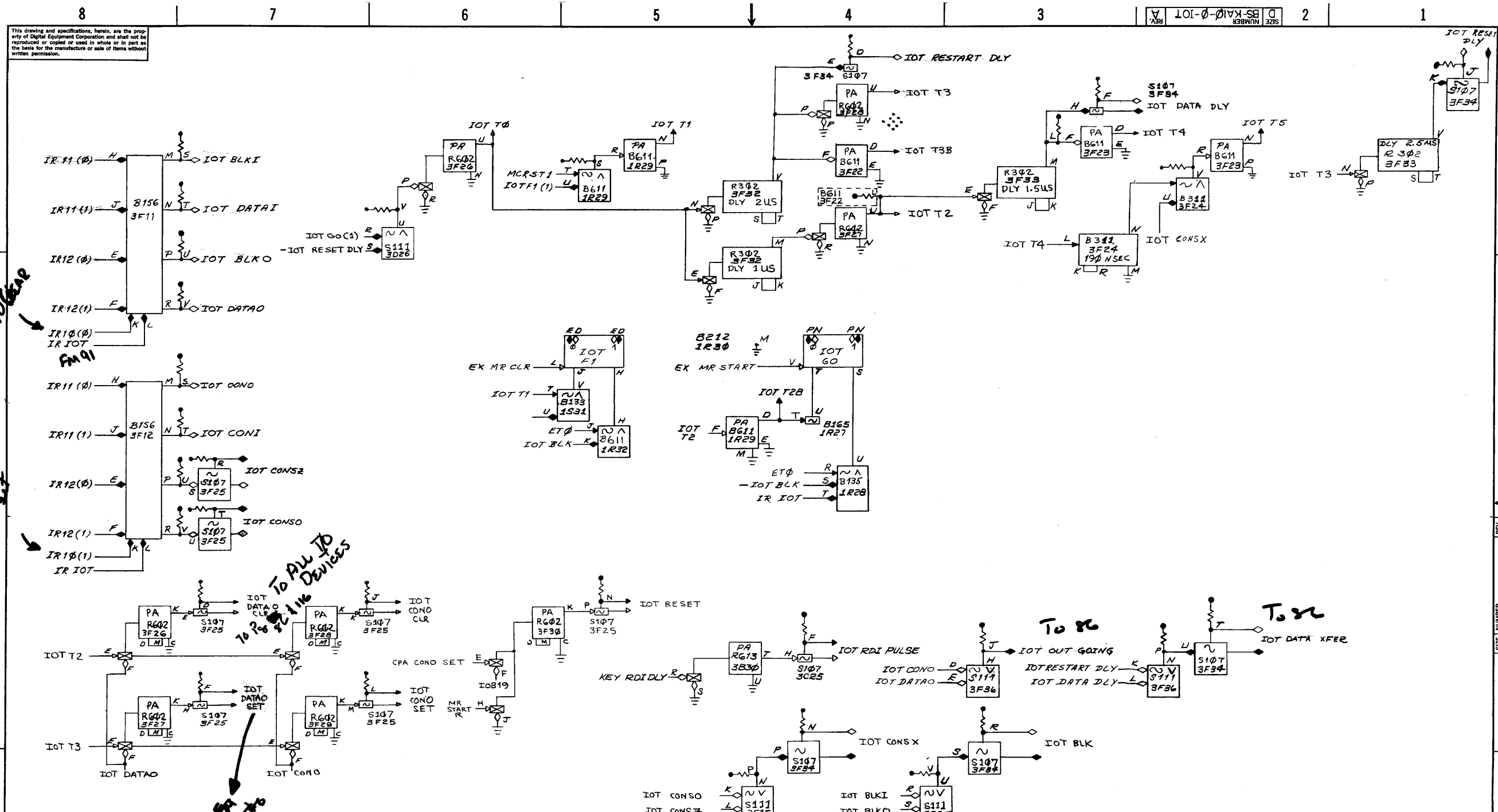


REV.	CHANGE NO.	DATE	BY	CHK
A	1	12/16/68	W.S.	
B	2	1/14/69	R. Clark	

DEC FORM NO. 8

- PTP STATUS E
- PTP PIA 35(1) E
- PTR DATA I D H
- PTR 35(1) J
- CPA STATUS B K
- CPA PIA 35(1) L
- PI STATUS B M
- PIO 7(1) N
- TTY DATA P
- TTI 1(0) R
- TTY STATUS S
- TTY PIA 35(1) I
- PTR STATUS U
- PTR PIA 35(1) V

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DATE 12/16/68	
DIMENSION IN INCHES		DATE 1/14/69	
TOLERANCES		TITLE	
DECIMALS	FRACTIONS	ANGLES	JOB INPUTS
± .005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL		DATE 1-14-69	
FINISH		FIRST USED ON	
SCALE		SIZE CODE	
SHEET OF		NUMBER	
		DIST.	



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REVISIONS		
CHK	CHANGE NO.	REV.
W.S.	32	A
<i>P. C. ...</i>		

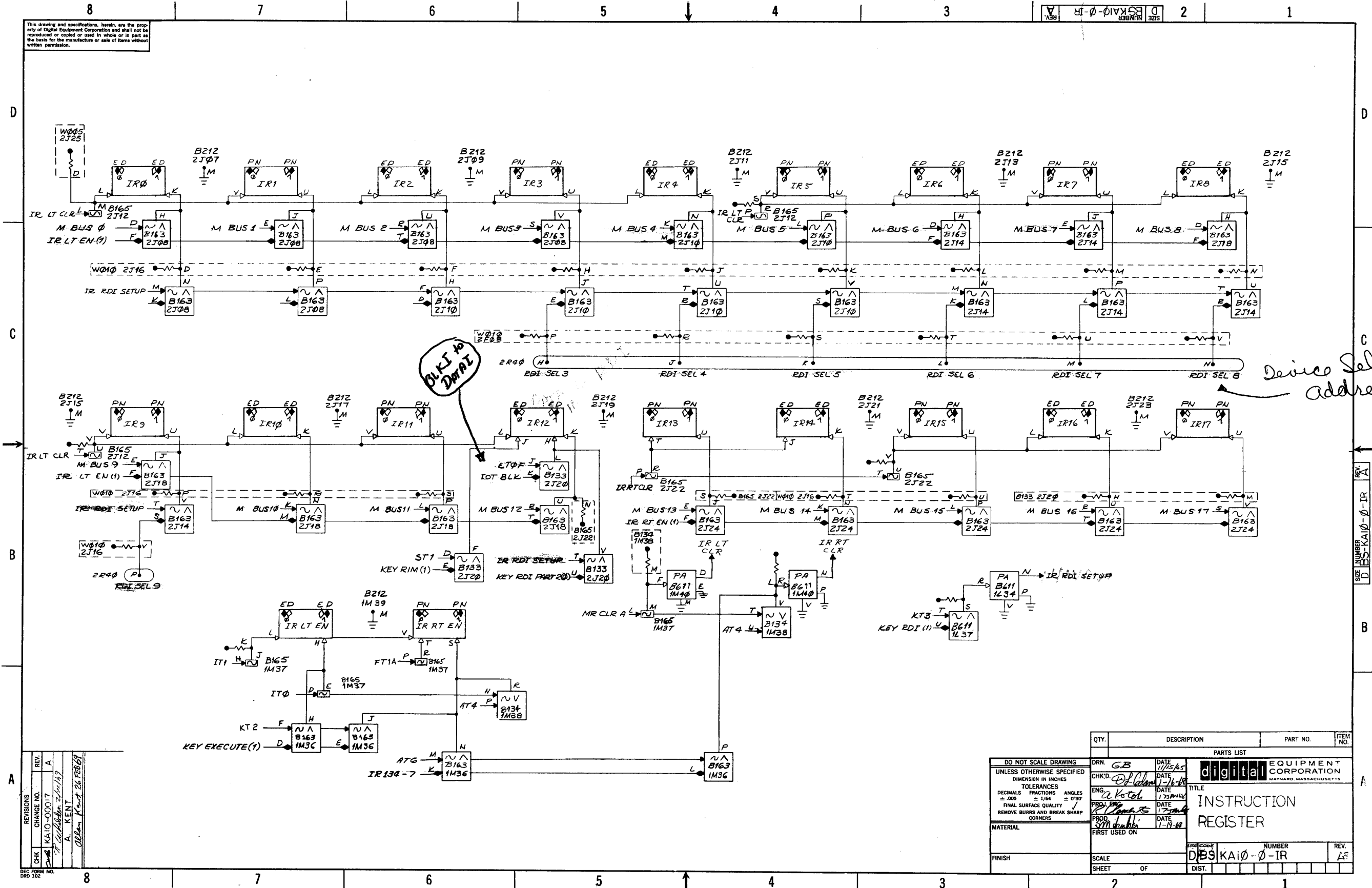
NOTE:  
ALL R602'S ON THIS DIAGRAM MUST BE TESTED FOR 400 NSEC PULSES (±50 NSEC)

*To All To The Devices*  
*To Bus to Reg's via 118 & 86*

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DRN	GB	DATE	1/30/68
CHK'D	<i>[Signature]</i>	DATE	1/16/68
ENG	<i>[Signature]</i>	DATE	1/27/68
PROD. ENG.	<i>[Signature]</i>	DATE	1/27/68
PROD.	<i>[Signature]</i>	DATE	1/19/68
FIRST USED ON			

digital	EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS	
TITLE	
IN-OUT TRANSFER CONTROL	
SCALE	NUMBER
5/8" = 1"	D18-KA10-0-IOT
SHEET	REV.
OF	A

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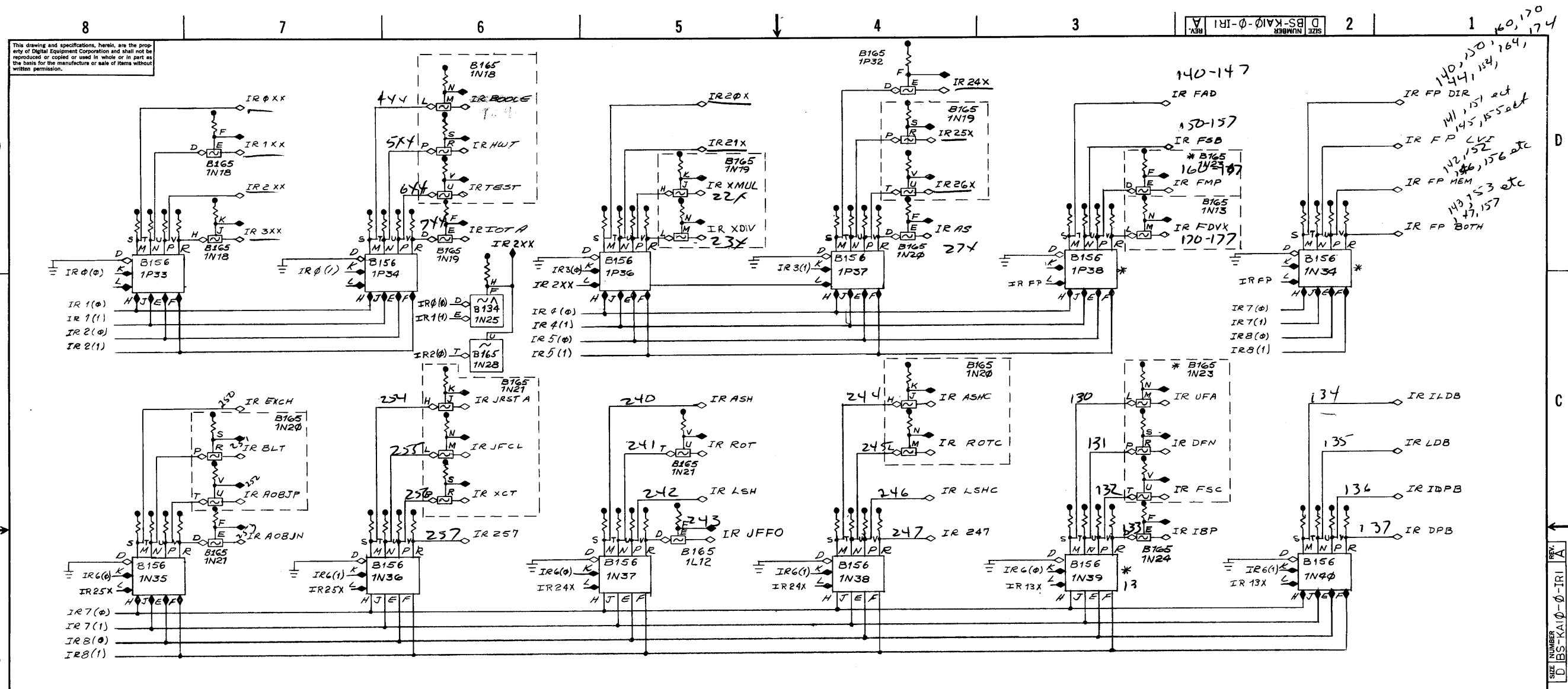
Device Select Address

BLK TO Digital

REV.	CHANGE NO.	DATE	BY	CHK
1				
2				
3				
4				
5				
6				
7				
8				

DO NOT SCALE DRAWING		PARTS LIST	
UNLESS OTHERWISE SPECIFIED	DRN. GB	DATE 1/15/65	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
DIMENSION IN INCHES	CHK'D. D. Allen	DATE 1-26-65	
TOLERANCES	ENG. G. Kotol	DATE 1-23-65	TITLE INSTRUCTION REGISTER
DECIMALS FRACTIONS ANGLES	PROD. ENR. G. Kotol	DATE 1-23-65	
± .005 ± 1/64 ± 0°30'	PROD. ENR. G. Kotol	DATE 1-23-65	NUMBER D85-KA10-0-IR
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	PROD. ENR. G. Kotol	DATE 1-23-65	
MATERIAL	PROD. ENR. G. Kotol	DATE 1-23-65	REV. A
FINISH	PROD. ENR. G. Kotol	DATE 1-23-65	
SCALE	SHEET	OF	
DIST.			





# & E = 0 M = True  
 H & F = 1 N = True  
 J & E = 2 P = True  
 J & F = 3 R = True

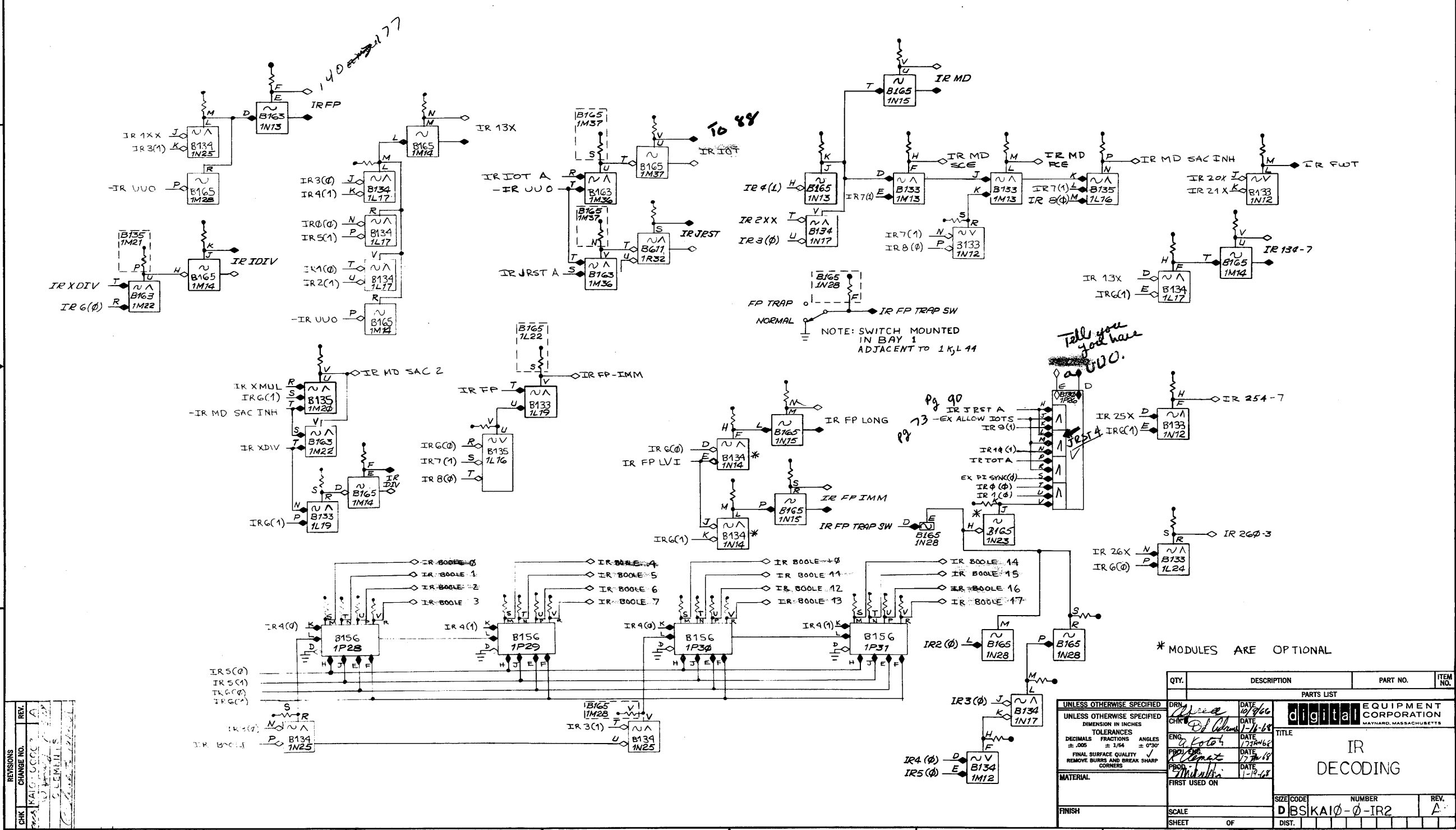
000  
 250

\* MODULES ARE OPTIONAL

REV.	CHANGE NO.	DATE
1	1	1-19-68
2	2	1-19-68
3	3	1-19-68

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
DO NOT SCALE DRAWING			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
±.005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE			
SHEET OF			
DRN. <i>RRY</i>		DATE <i>12-25-65</i>	<b>digital</b> EQUIPMENT CORPORATION WATUARD, MASSACHUSETTS
CHK'D <i>[Signature]</i>		DATE <i>1-18-69</i>	
ENG. <i>A. Kotoh</i>		DATE <i>12-28-68</i>	
PROD. <i>[Signature]</i>		DATE <i>1-19-68</i>	
TITLE			IR DECODING
FIRST USED ON			
PREPARED BY		NUMBER	REV.
D. BS-KAI0-0-IRI		A	A

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REV.	CHANGE NO.	CHK.
1	1	...
2	2	...
3	3	...
4	4	...
5	5	...
6	6	...
7	7	...
8	8	...

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS FRACTIONS ANGLES		
	±.005 ±.104 ±.930		
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET OF		
	SIZE CODE	NUMBER	REV.
	D BSKAI0-0-IR2		A
	DIST.		

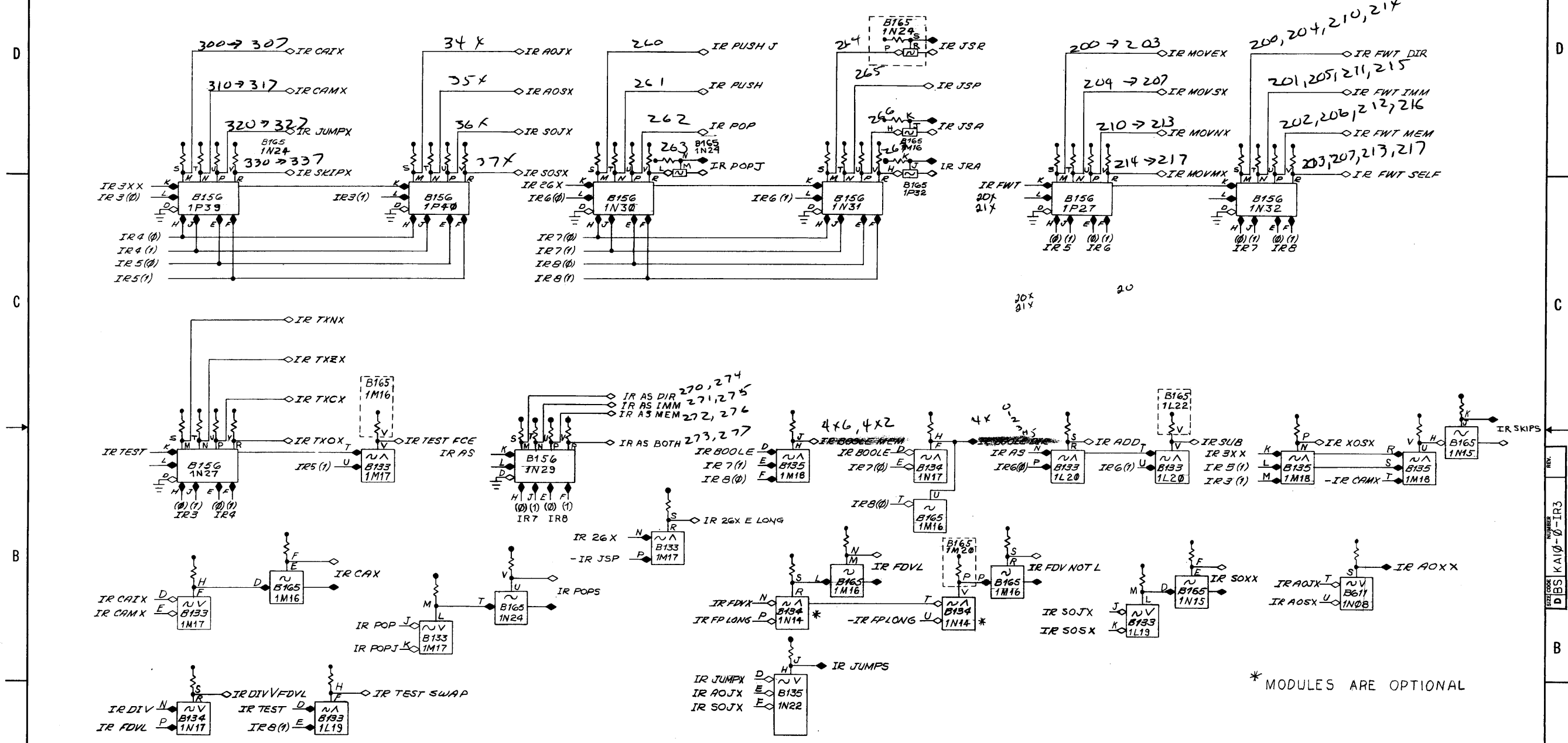
\* MODULES ARE OPTIONAL

Tell you  
you have  
a U.O.

NOTE: SWITCH MOUNTED  
IN BAY 1  
ADJACENT TO 1K, L 11

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8 7 6 5 4 3 2 1  
 DBS KA10-0-IR3  
 2



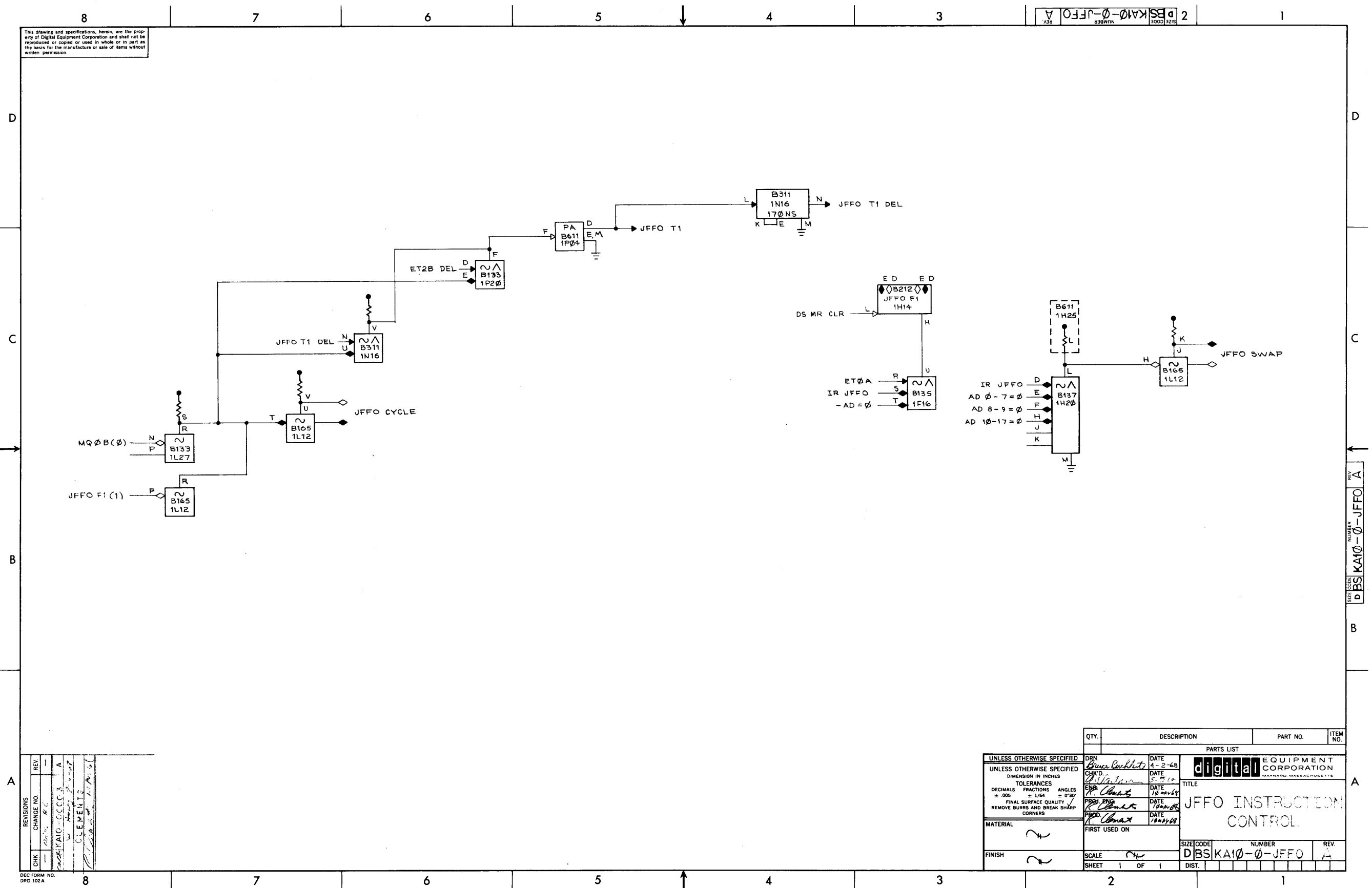
\* MODULES ARE OPTIONAL

REV.	
CHANGE NO.	
CHK.	

DEC FORM NO. DRD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
± .005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
DRN. DATE 10/1/66		DATE 1-16-68	
CHKD. DATE 1-16-68		DATE 1-16-68	
ENG. DATE 1-16-68		DATE 1-16-68	
PROJ. ENG. DATE 1-16-68		DATE 1-16-68	
PROD. DATE 1-16-68		DATE 1-16-68	
FIRST USED ON			
SCALE		SIZE CODE	NUMBER
SHEET OF		DBS KA10-0-IR3	REV.

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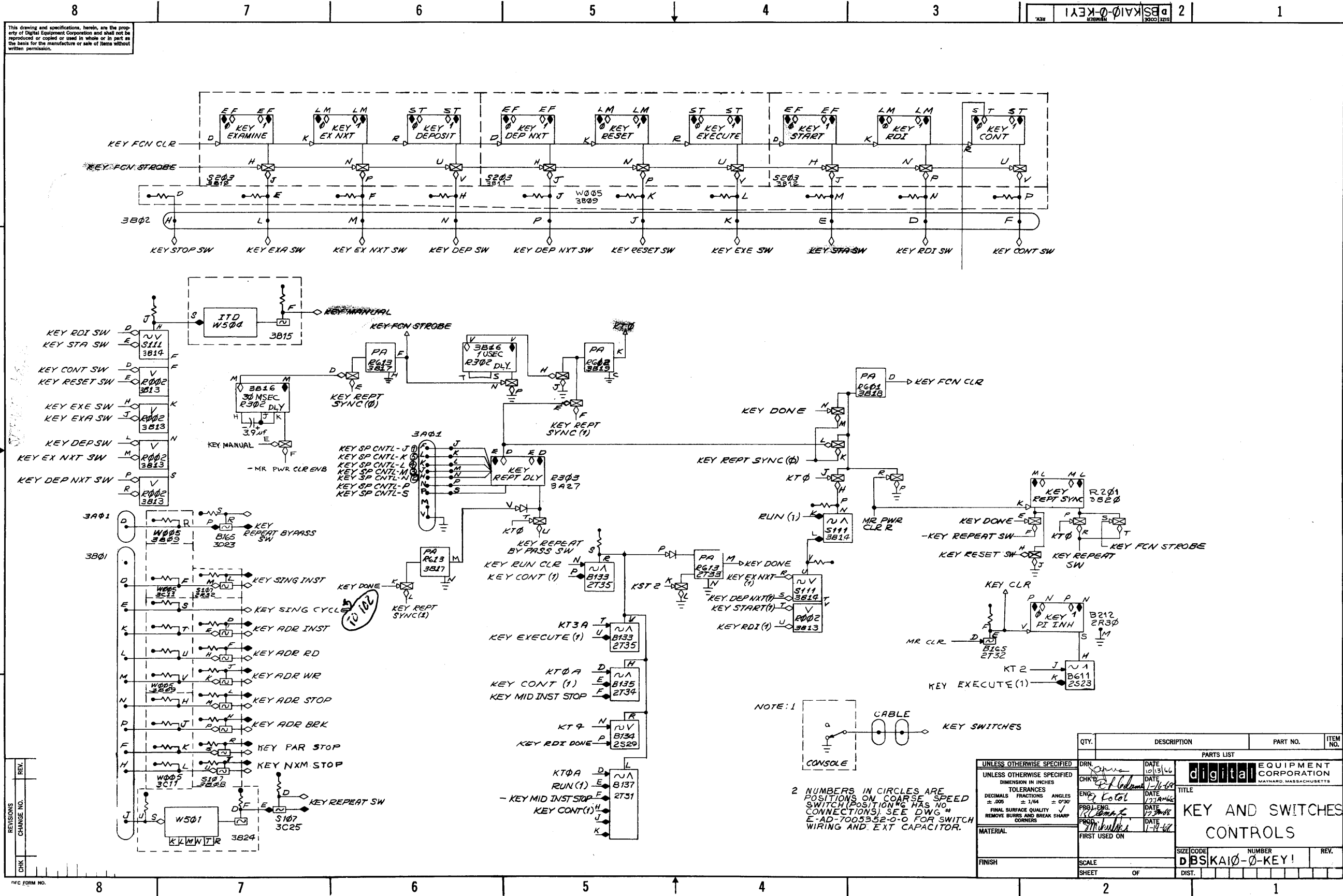


REV.	CHG.	NO.	DATE
1			

PAOLO CCCC  
 CLEMENTS  
 1/1/68

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN	DATE
UNLESS OTHERWISE SPECIFIED		CHK'D.	DATE
DIMENSION IN INCHES		ENR	DATE
TOLERANCES		PRD. ENR	DATE
DECIMALS FRACTIONS ANGLES		PRD.	DATE
= .005 ± 1/64 = 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL	FIRST USED ON		
FINISH	SCALE	SIZE CODE	NUMBER
	SHEET 1 OF 1	DIBS KA10-0-JFFO	REV. A

**digital** EQUIPMENT CORPORATION  
 MATTAPOISETT, MASSACHUSETTS  
 TITLE  
**JFFO INSTRUCTION CONTROL**



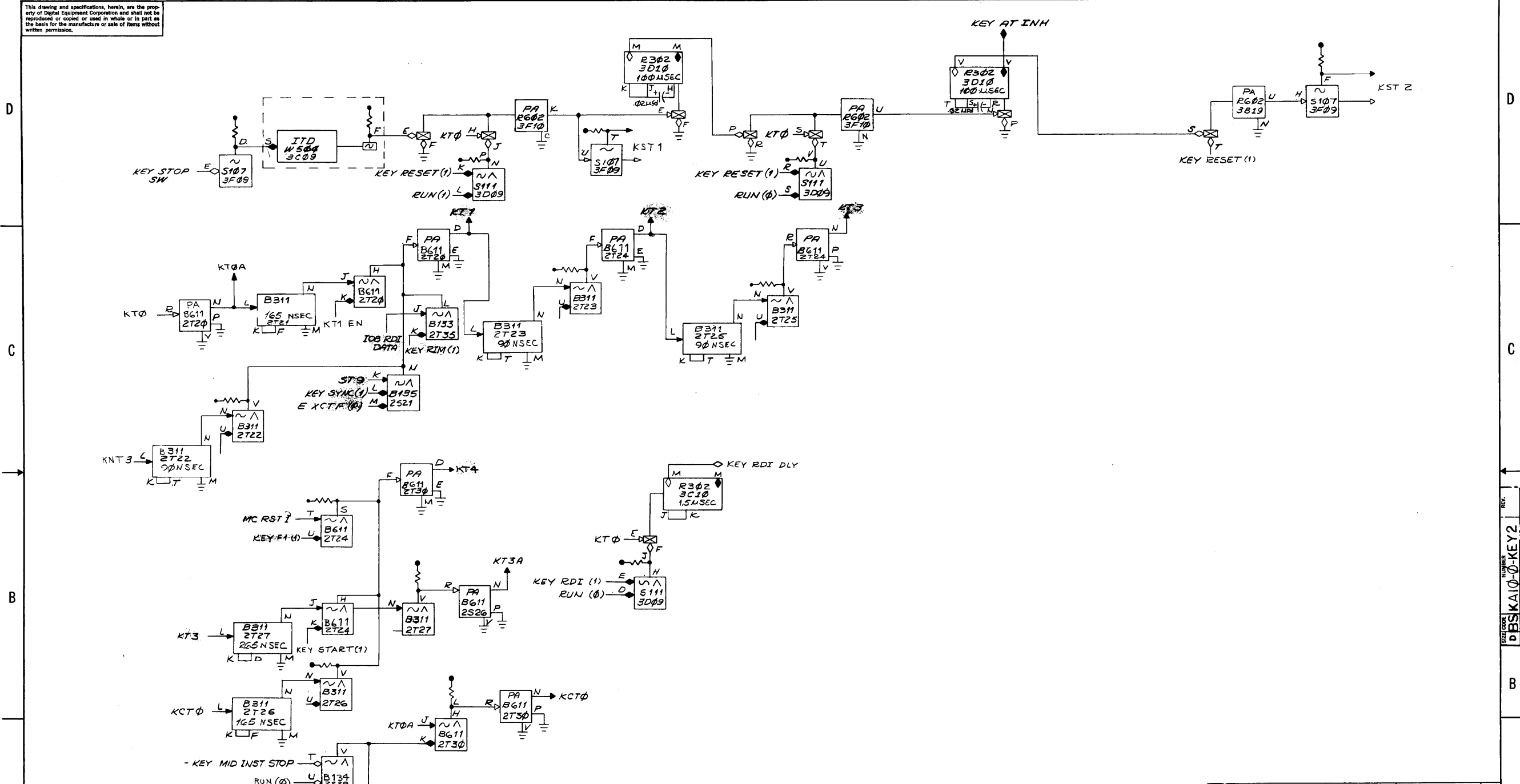
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REV.	CHANGE NO.
CHK	

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8 7 6 5 4 3 2 1

REV. NUMBER  
DBSKA10-0-KEY2



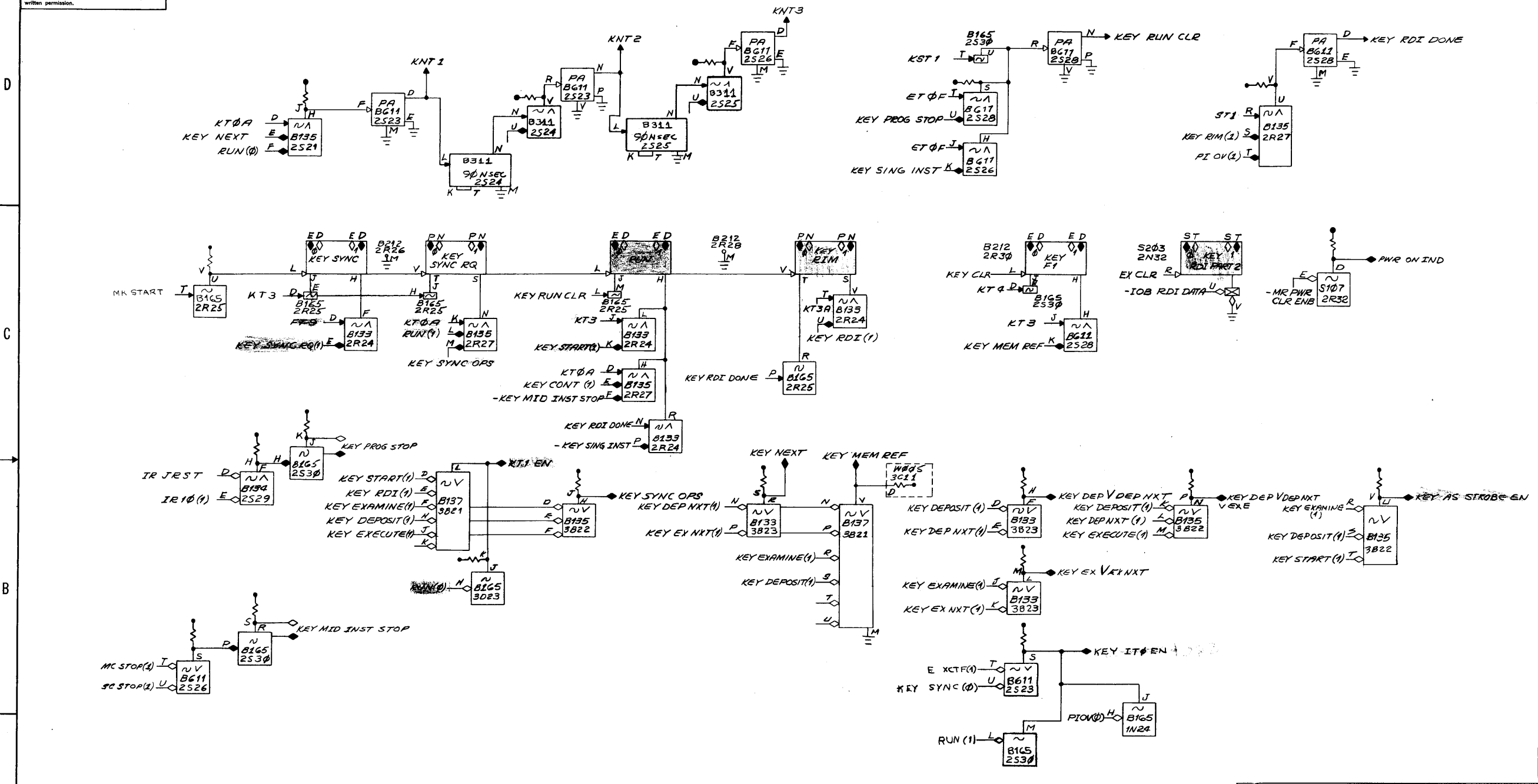
REV.	
CHG.	
NO.	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D	DATE	TITLE	
ENG.	DATE	KEYS & SWITCHES CONTROLS	
PROJ. ENGR.	DATE	SIZE CODE NUMBER	
PROJ. MGR.	DATE	DBSKA10-0-KEY2	
PROJ. SCHED.	DATE	REV.	
FIRST USED ON			
SCALE			
SHEET OF			
DIST.			

DEC FORM NO. DRD 102

8 7 6 5 4 3 2 1

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REV.	CHANGE NO.	DESCRIPTION

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			

UNLESS OTHERWISE SPECIFIED  
 DIMENSION IN INCHES  
 DECIMALS FRACTIONS ANGLES  
 ± .005 ± 1/64 ± 0°30'  
 FINAL SURFACE QUALITY  
 REMOVE BURRS AND BREAK SHARP CORNERS

DRN: *[Signature]* DATE: 12/14/60  
 CKD: *[Signature]* DATE: 1/16/61  
 ENG: *[Signature]* DATE: 1/16/61  
 PBL: *[Signature]* DATE: 1/16/61  
 PRD: *[Signature]* DATE: 1-19-61

TITLE  
**KEYS & SWITCHES CONTROL**

SHEET OF 1

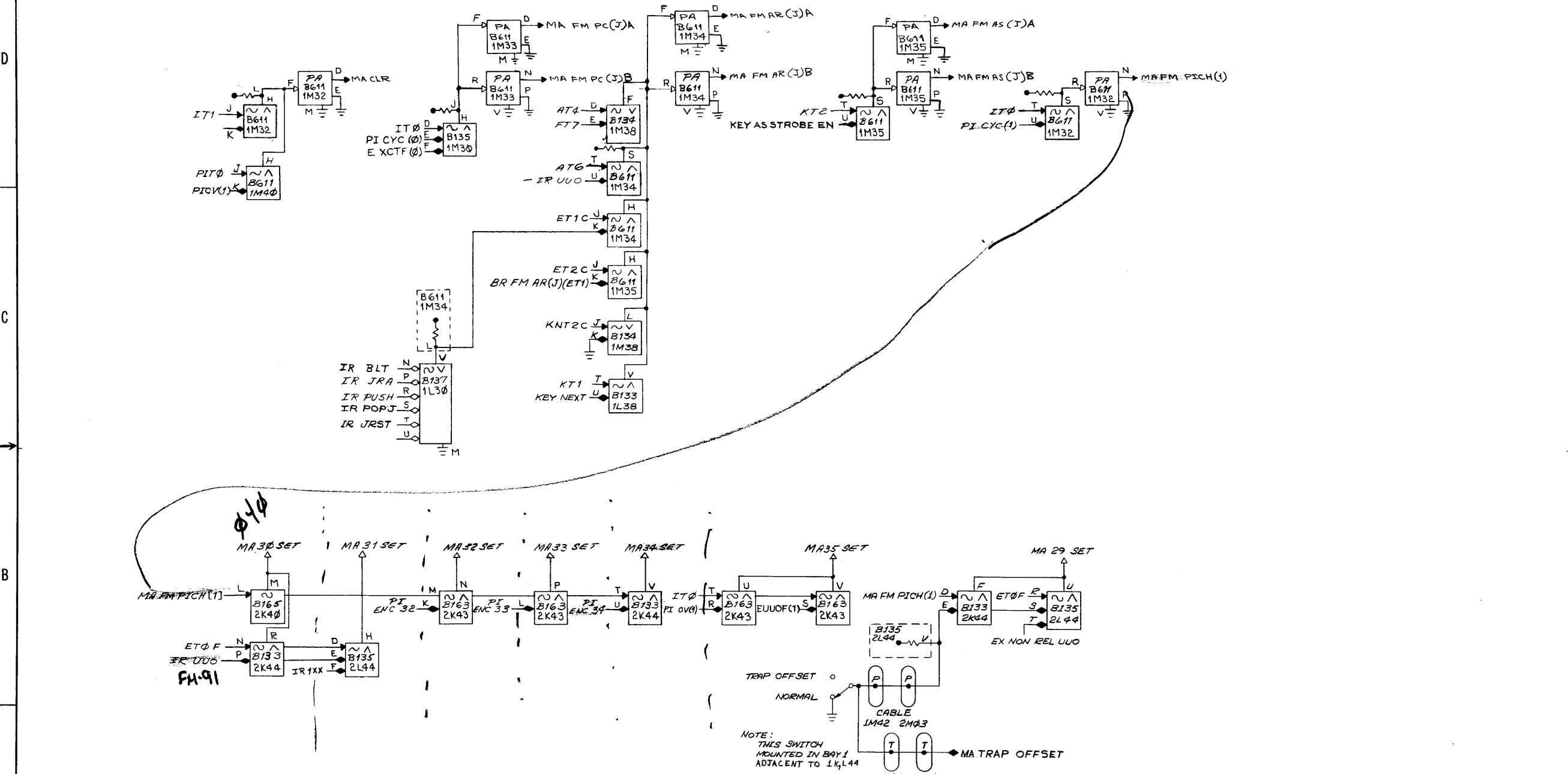
SCALE: DIST.

SIZE CODE: DBS KAI0-0-KEY3

NUMBER: 1

REV: 1

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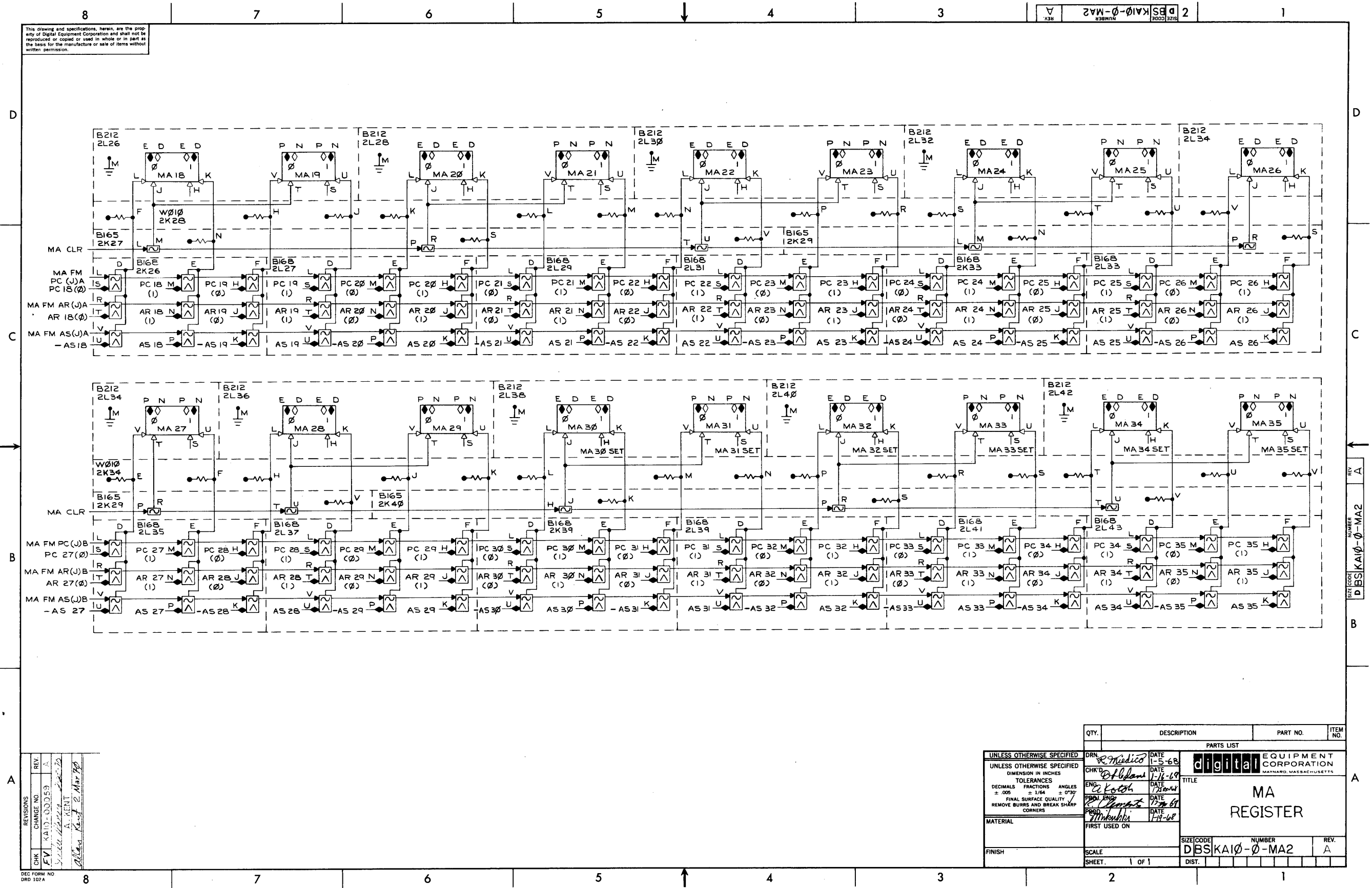
REV.	CHG.	NO.	DATE	BY
A				
B				
C				
D				

DESIGNED BY: A. KENT  
 CHECKED BY: J. W. KENT  
 DATE: FEB 67

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE <b>MA CONTROL</b>			
SCALE	SHEET OF	SIZE	CODE
		D	BS KAI 0 - 0 - MA I
FINISH		DIST.	



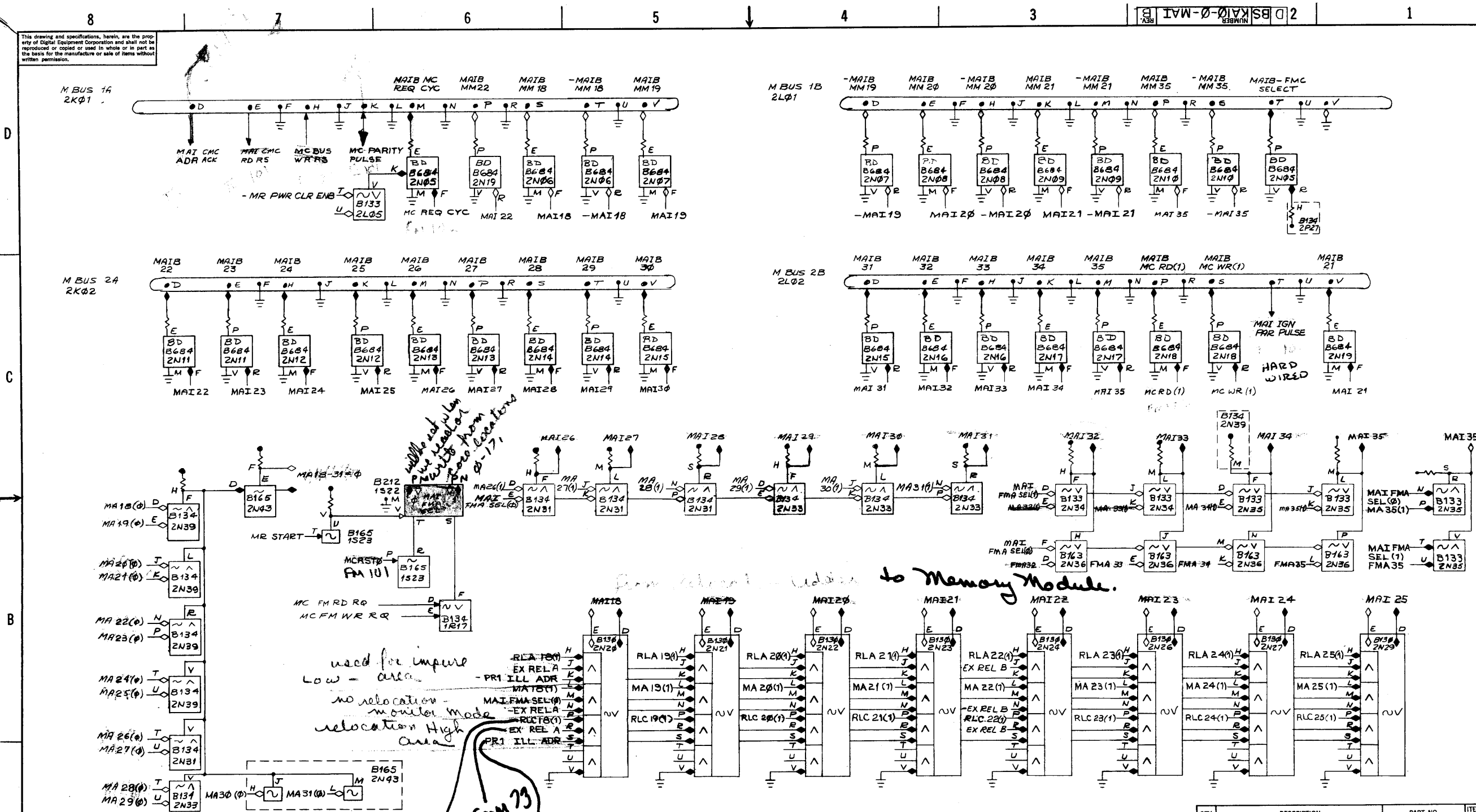
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REV.	CHANGE NO.	DATE
1	00053	1-11-68
2	00054	1-11-68
3	00055	1-11-68

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN: R. Medico	
UNLESS OTHERWISE SPECIFIED		DATE: 1-5-68	
DIMENSION IN INCHES		CHKD: D. Adams	
TOLERANCES		DATE: 1-11-68	
DECIMALS	FRACTIONS	ANGLES	DATE: 1-11-68
± .005	± 1/64	± 0°30'	DATE: 1-11-68
FINAL SURFACE QUALITY		DATE: 1-11-68	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE: 1-11-68	
MATERIAL		DATE: 1-11-68	
FINISH		DATE: 1-11-68	
FIRST USED ON		DATE: 1-11-68	
SCALE		SIZE/CODE	
SHEET 1 OF 1		DBS KAI0-0-MA2	
		NUMBER	
		REV. A	

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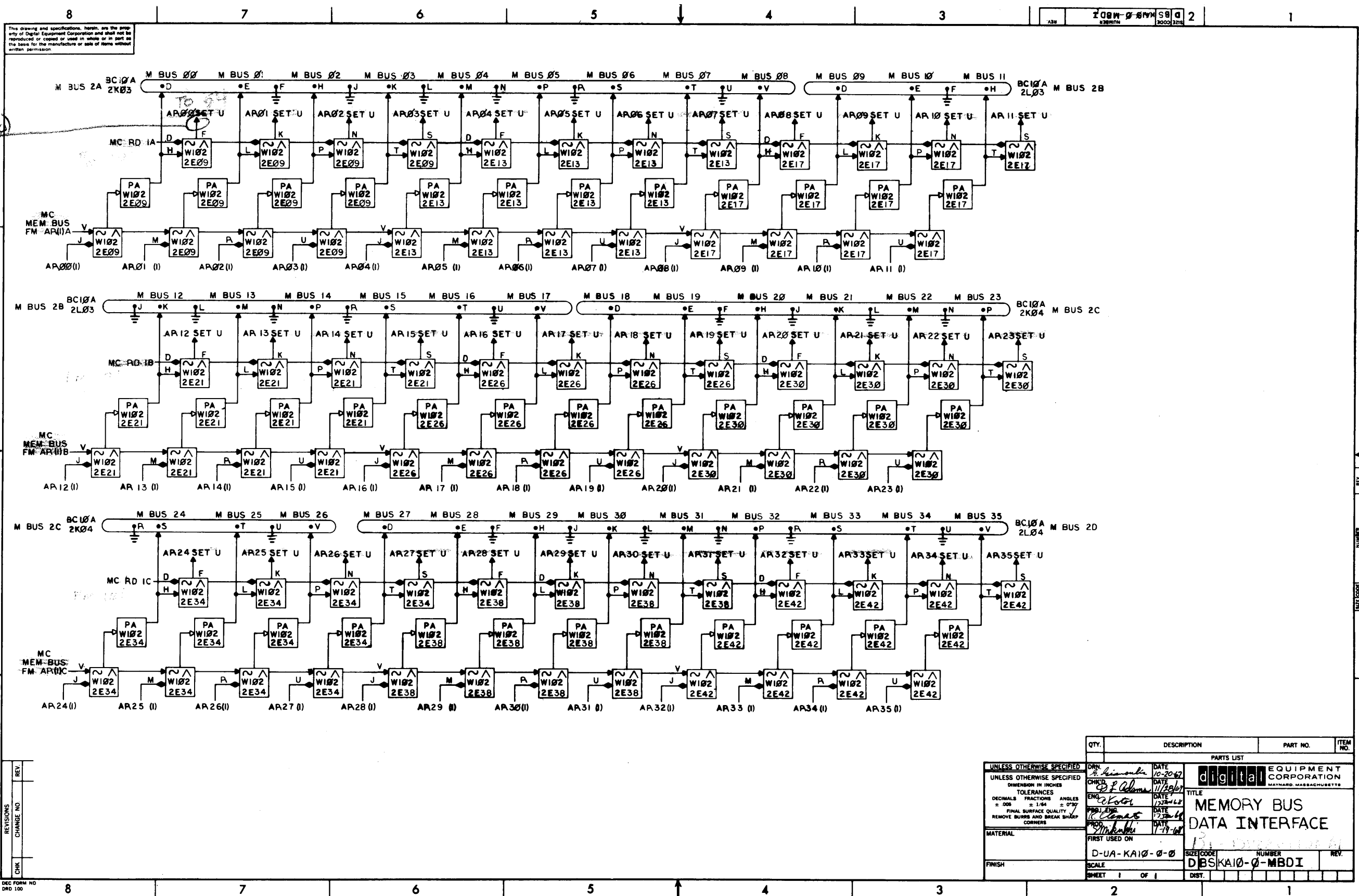


REV.	CHANGE NO.	DATE	BY	CHK'D
1	ECO # 20	12-7-65	A	
2	ECO # 20-21	1-17-66	A	
3	ECO # 20-21	1-17-66	A	
4	ECO # 20-21	1-17-66	A	
5	ECO # 20-21	1-17-66	A	
6	ECO # 20-21	1-17-66	A	
7	ECO # 20-21	1-17-66	A	
8	ECO # 20-21	1-17-66	A	

used for impulse  
Low - area  
no relocation -  
monitor mode  
relocation High  
area

from 121  
from 73  
from 115

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE MEMORY ADDRESS INTERFACE			
SIZE CODE NUMBER REV. D BS KA10-0-MAI B			
SCALE SHEET OF DIST.			

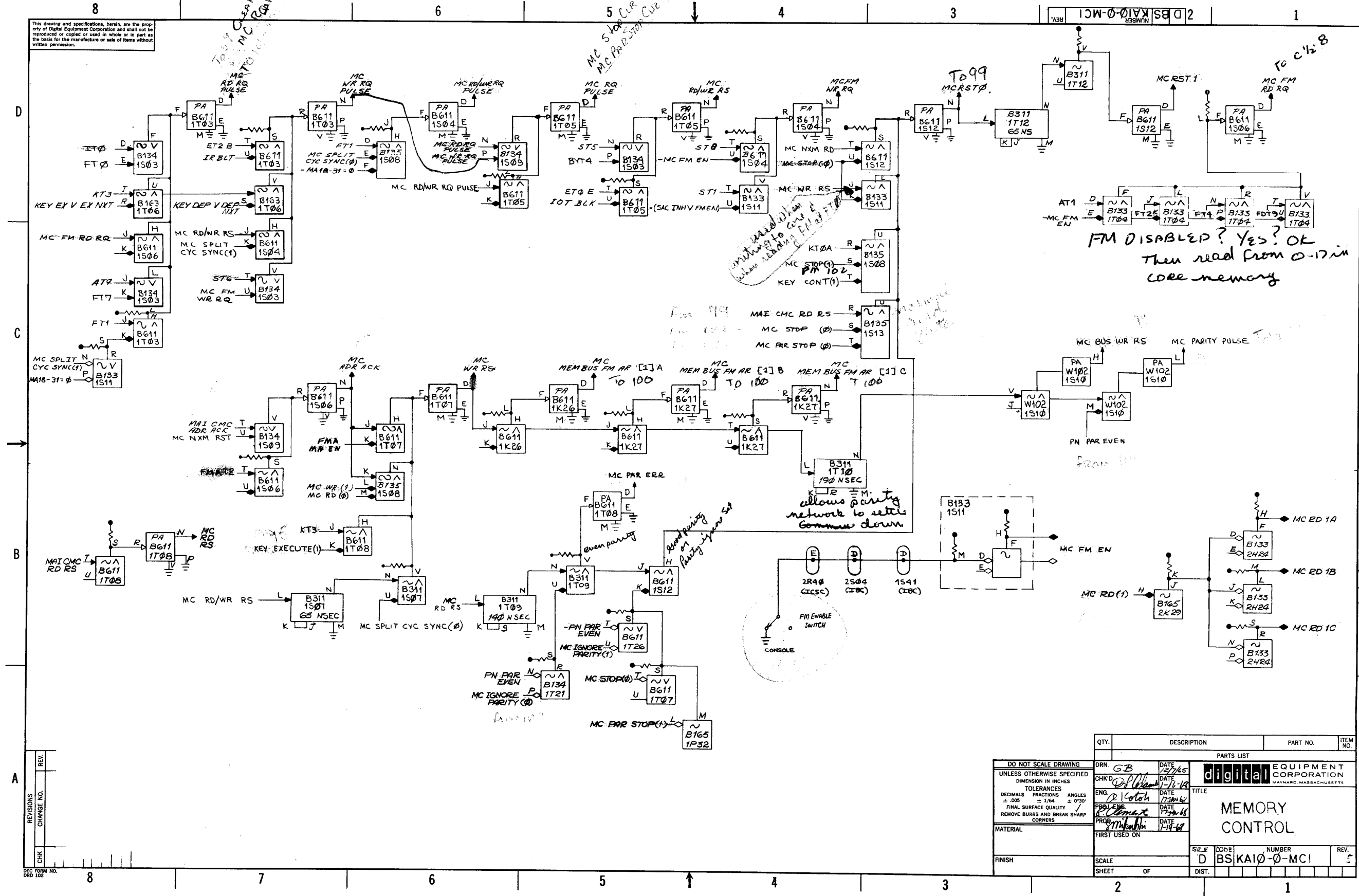


should be High going pulse (must be in print)

REV.	
CHANGE NO.	
CHK	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DATE 10-20-67	
DIMENSION IN INCHES		DRAWN <i>A. Simon</i>	
TOLERANCES		DATE 11/20/67	
DECIMALS	FRACTIONS	ANGLES	TITLE
± .005	± 1/64	± 0°30'	MEMORY BUS DATA INTERFACE
FINAL SURFACE QUALITY		DATE 12/20/67	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE 1/19/68	
MATERIAL		FIRST USED ON	
FINISH		D-UA-KA10-0-0	
SCALE		SIZE CODE	NUMBER
SHEET 1 OF 1		DIST.	REV.

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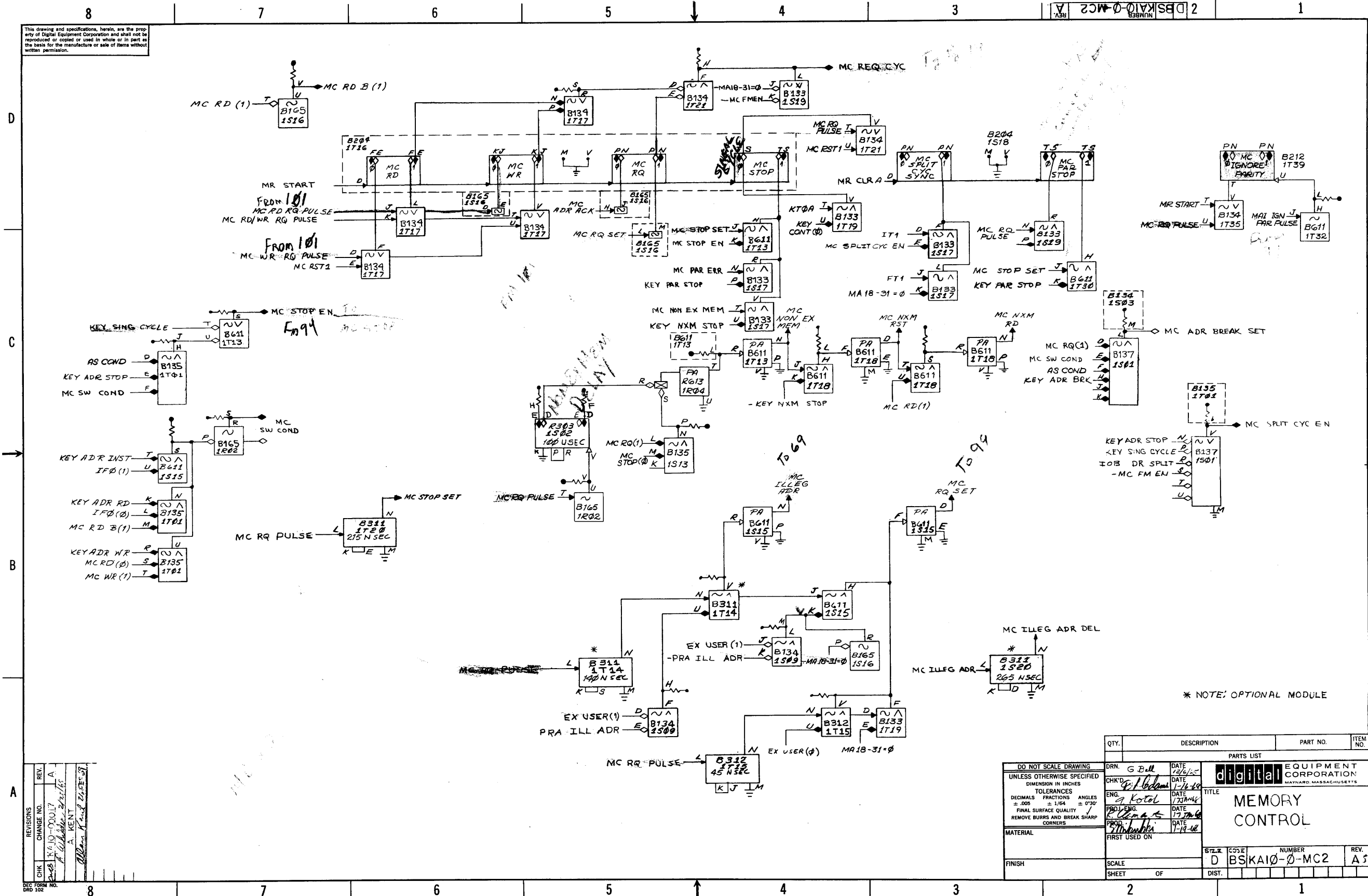


REV.	REVISIONS

SEC FORM NO. DRD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES = .005 = 1/64 = 90° FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS MATERIAL FINISH SCALE SHEET OF			
DRN.	GB	DATE	12/7/65
CHK'D	<i>[Signature]</i>	DATE	11-16-65
ENG.	<i>[Signature]</i>	DATE	11-18-65
PROB'G	<i>[Signature]</i>	DATE	11-19-65
FRST USED ON		DATE	11-19-65
TITLE		MEMORY CONTROL	
SIZ. E	D	NUMBER	BSKAI0-0-MC1
DIST.		REV.	5

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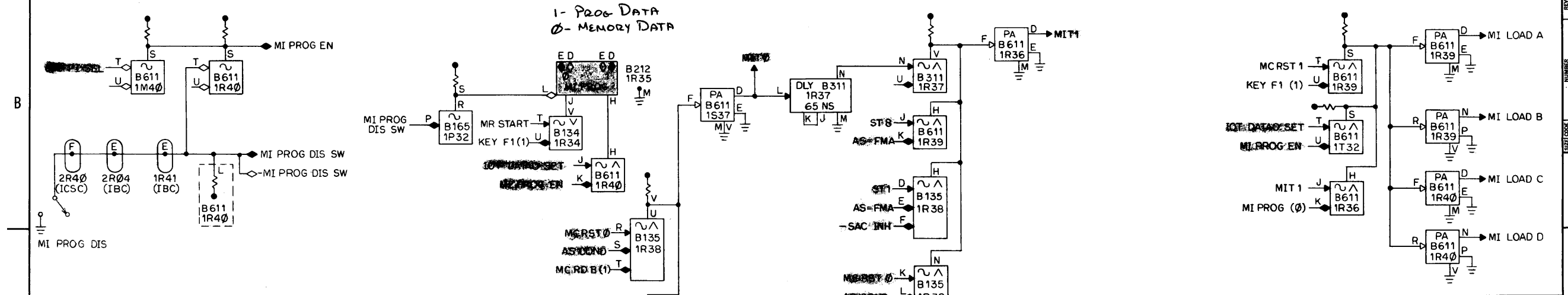
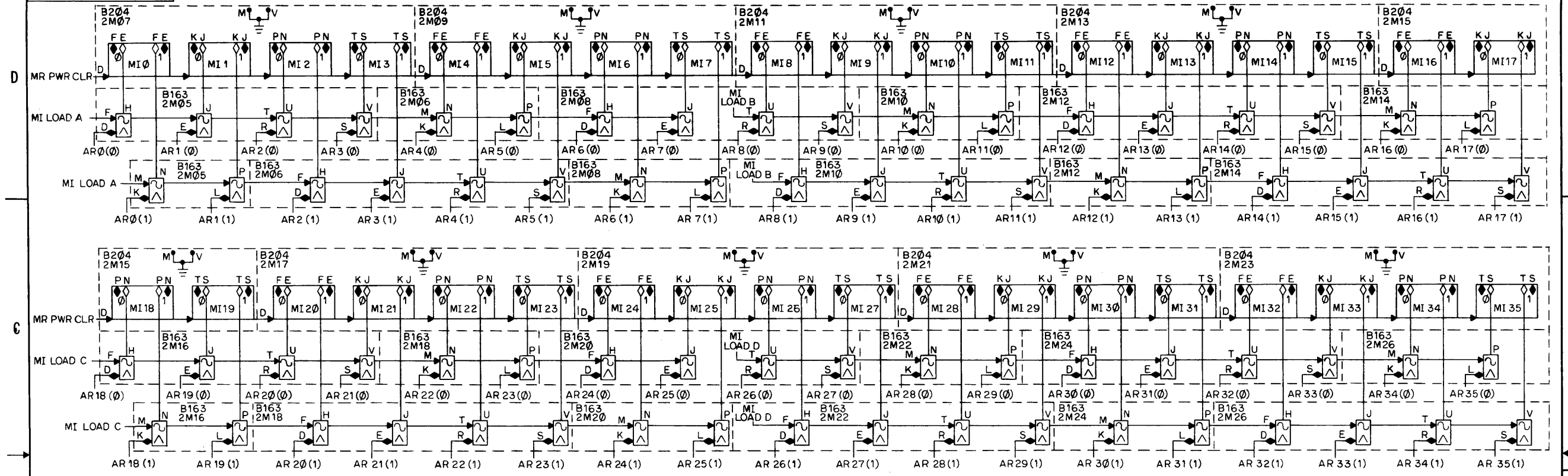


REV.	CHANGE NO.	DATE	BY	CHK'D
A	00017	1-16-60	G. Ball	G. Ball
B	00018	1-16-60	G. Ball	G. Ball
C	00019	1-16-60	G. Ball	G. Ball
D	00020	1-16-60	G. Ball	G. Ball

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING		DRN: G Ball	
UNLESS OTHERWISE SPECIFIED		DATE: 12/6/58	
DIMENSION IN INCHES		CHK'D: G. Ball	
TOLERANCES		DATE: 1-16-60	
DECIMALS FRACTIONS ANGLES		ENG: G. Kotel	
± .005 ± 1/64 ± 0°30'		DATE: 1-16-60	
FINAL SURFACE QUALITY		DATE: 1-16-60	
REMOVE BURRS AND BREAK SHARP CORNERS		DATE: 1-16-60	
MATERIAL		PROD. DATE: 1-19-60	
FINISH		FIRST USED ON	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
MEMORY CONTROL	
SCALE	NUMBER
SHEET OF	REV.
D BSKA10-0-MC2	A 5

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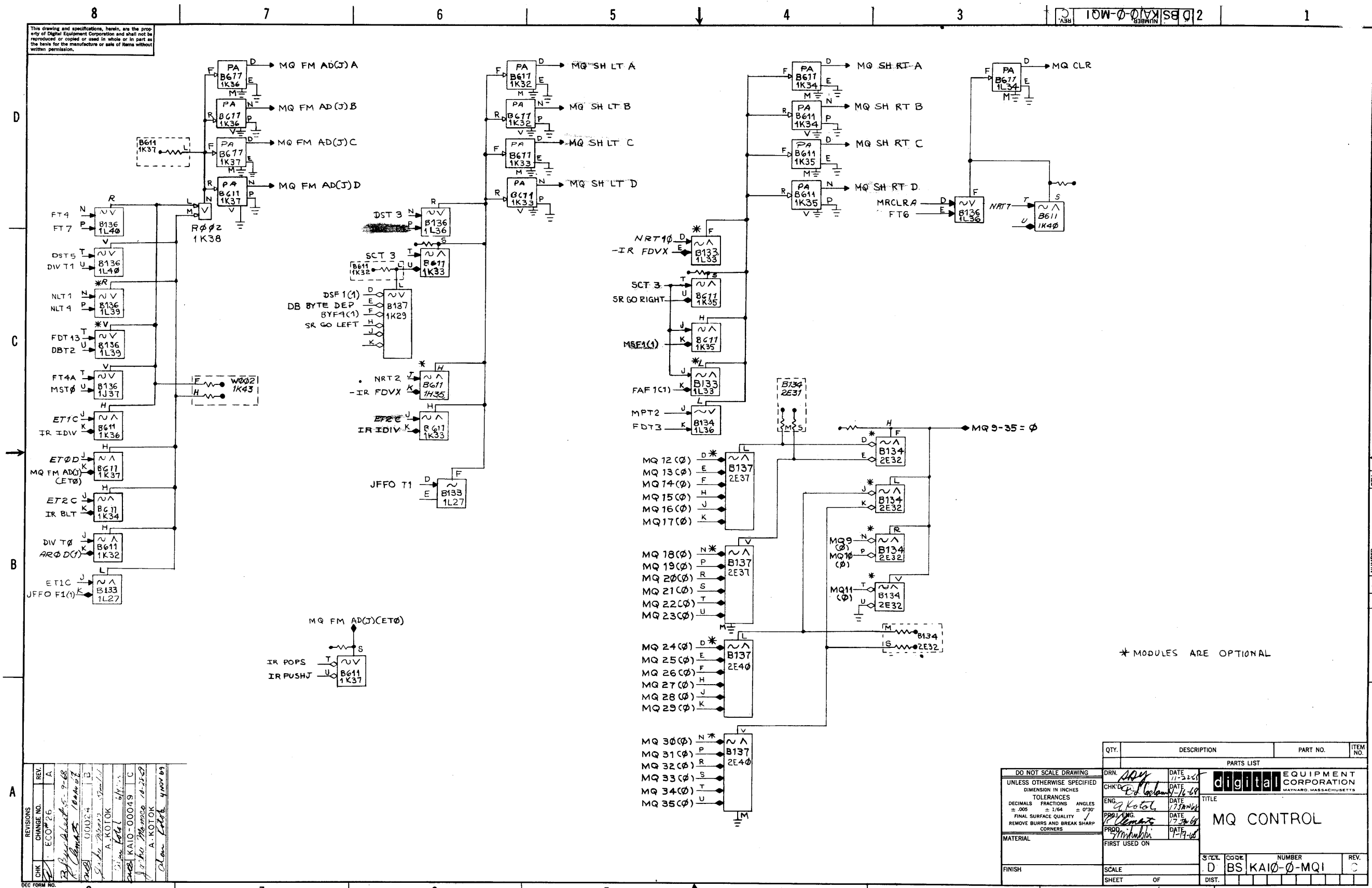
REV.	NO.	DESCRIPTION

QTY.	DESCRIPTION	PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED	DRN	DATE	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
UNLESS OTHERWISE SPECIFIED	CHKD	DATE	
TOLERANCES			
DECIMALS FRACTIONS ANGLES			
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			<b>MEMORY INDICATOR</b>
MATERIAL	FIRST USED ON		
FINISH	SCALE	SIZE CODE	NUMBER
	SHEET	DIST.	REV.

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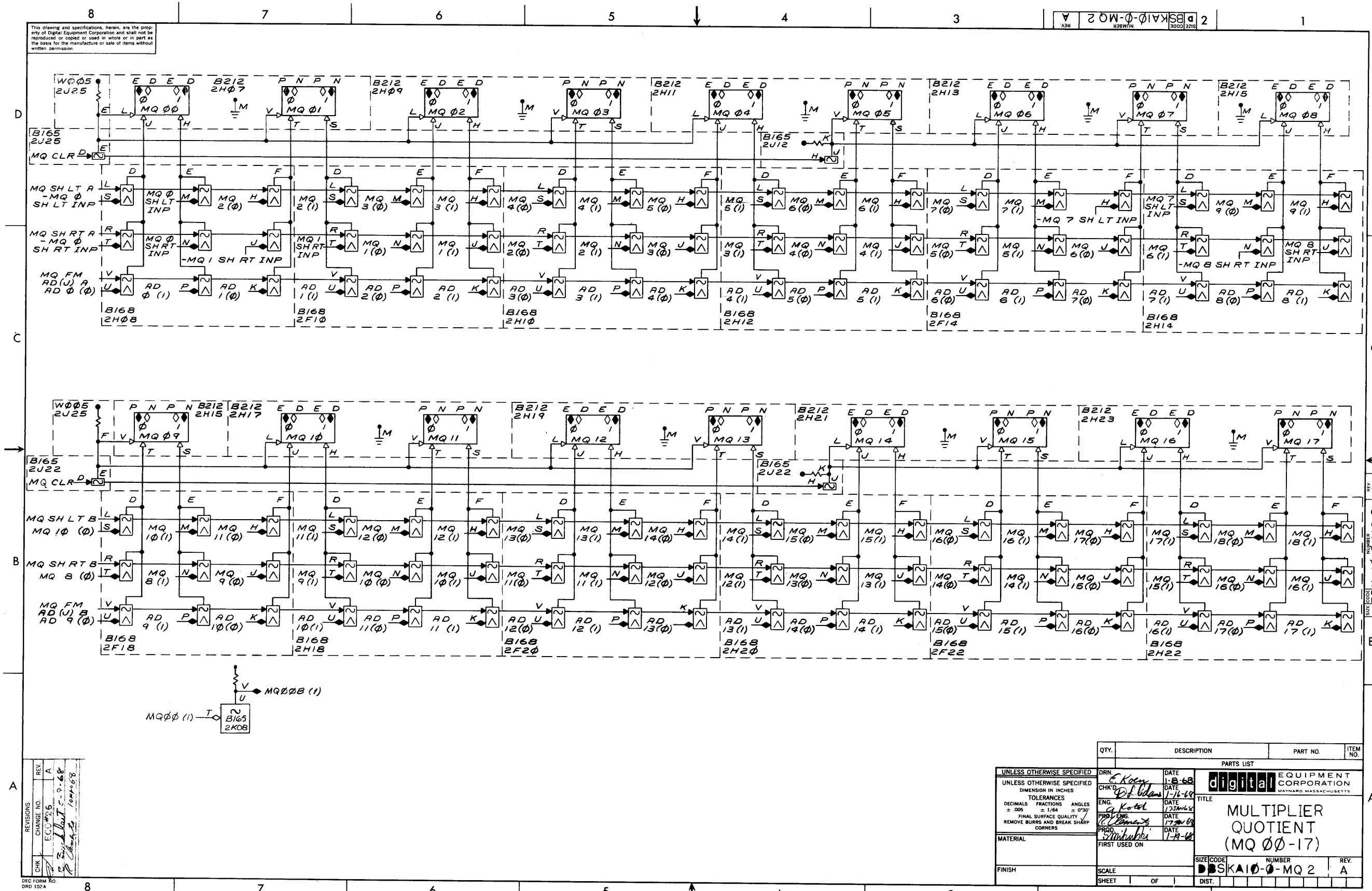
\* MODULES ARE OPTIONAL

REV	CHANGE NO.	DATE	BY	CHKD.
A	ECO# 26			
B				
C				
D				
E				
F				

DESKTOP  
 A. KOTOK  
 A. KOTOK  
 A. KOTOK  
 A. KOTOK  
 A. KOTOK

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	DO NOT SCALE DRAWING		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS FRACTIONS ANGLES		
	±.005 ±.1/64 ±.030'		
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET OF		
	DRAWN	DATE	
	CHK'D	DATE	
	ENG	DATE	
	PROJ ENG	DATE	
	PROD	DATE	
	FIRST USED ON		
	PARTS LIST		
	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
	TITLE MQ CONTROL		
	SHEET	CODE	NUMBER
	D	BS	KA10-0-MQ1
	DIST.		REV.
			C

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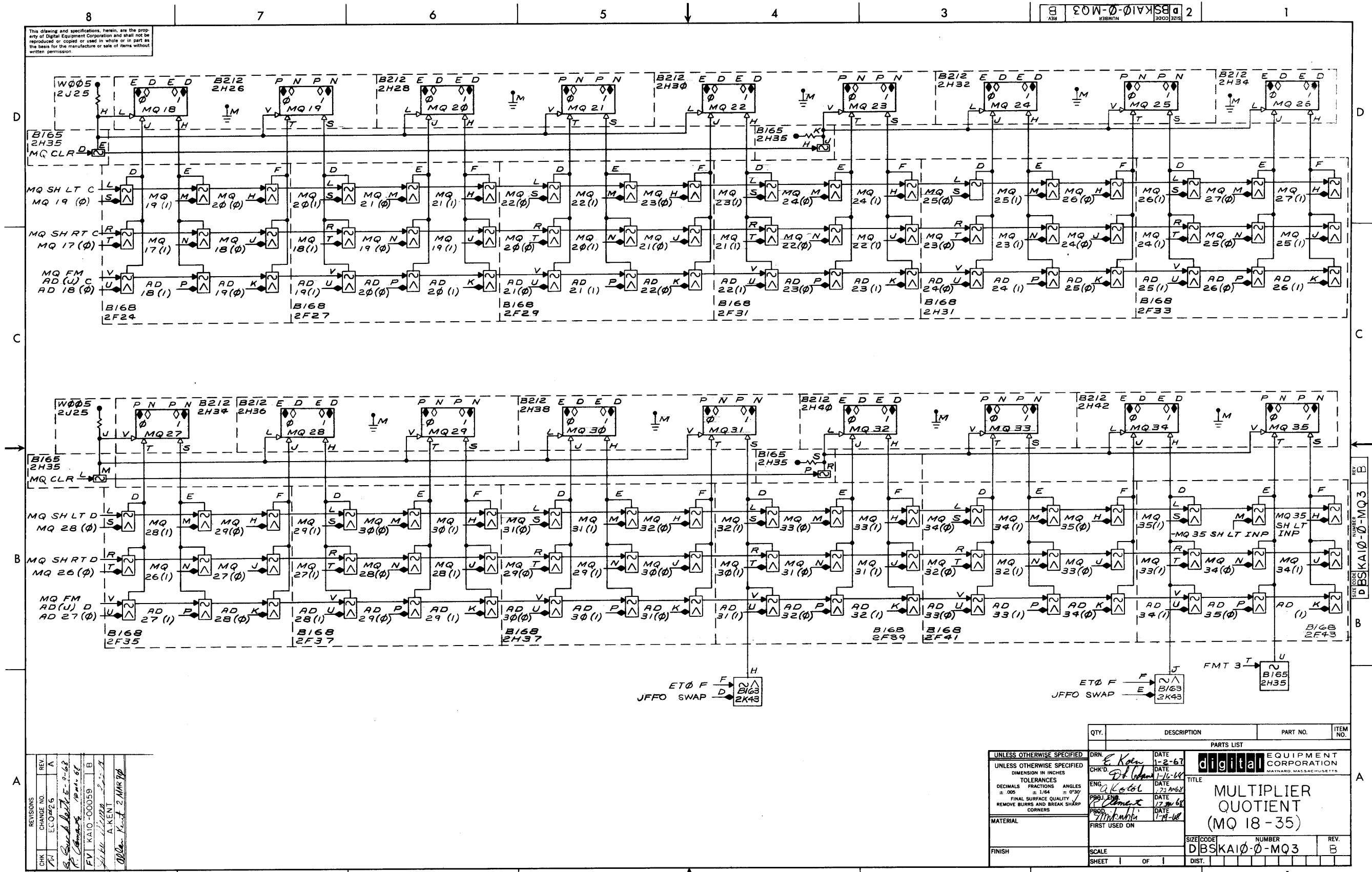
REV.	CHANGE NO.	DATE
A	1	10-1-68

DEC FORM NO. DRD 102A

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS FRACTIONS ANGLES			
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE			
SHEET OF			
DRN. E. Kocay		DATE 1-8-68	
CHK'D. D. Wilson		DATE 1-11-68	
ENG. G. Kotel		DATE 12-1-65	
PROV. ENG. G. Kotel		DATE 17-1-68	
FRONT. S. M. M. M.		DATE 1-9-68	
FIRST USED ON			
TITLE		MULTIPLIER QUOTIENT (MQ 00-17)	
SIZE CODE		BBSKA10-0-MQ 2	
NUMBER		A	
REV.		A	



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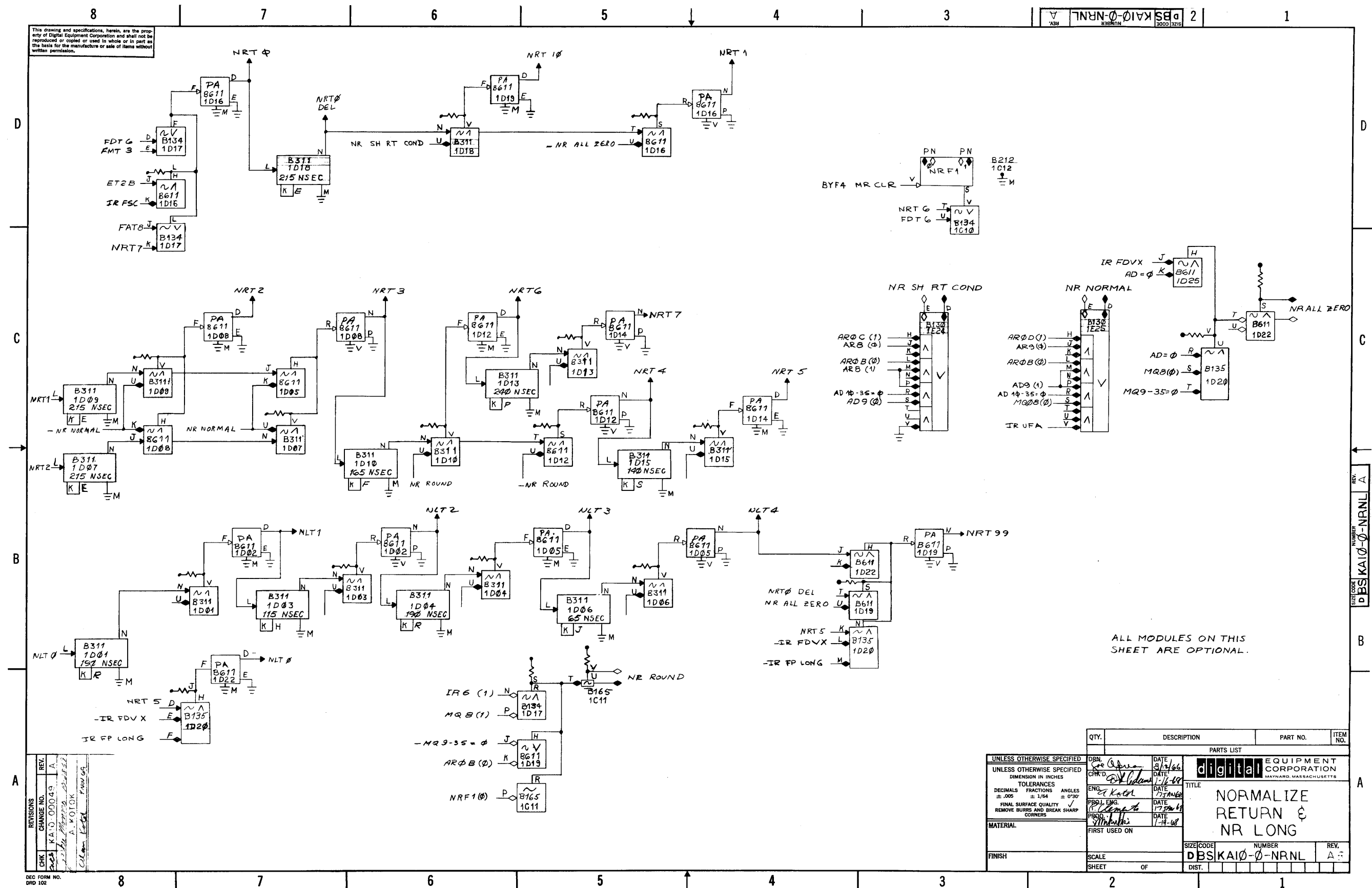


REV	CHANGE NO.	DESCRIPTION
A	ECO 25	
B	ECO 26	
C	ECO 27	
D	ECO 28	
E	ECO 29	
F	ECO 30	
G	ECO 31	
H	ECO 32	
I	ECO 33	
J	ECO 34	
K	ECO 35	
L	ECO 36	
M	ECO 37	
N	ECO 38	
O	ECO 39	
P	ECO 40	
Q	ECO 41	
R	ECO 42	
S	ECO 43	
T	ECO 44	
U	ECO 45	
V	ECO 46	
W	ECO 47	
X	ECO 48	
Y	ECO 49	
Z	ECO 50	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS	FRACTIONS	ANGLES
	± .005	± 1/64	± 0°30'
	FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET 1 OF 1		
	TITLE		
	MULTIPLIER QUOTIENT (MQ 18-35)		
	SIZE CODE NUMBER		
	DBSKAI0-0-MQ3		
	REV. B		

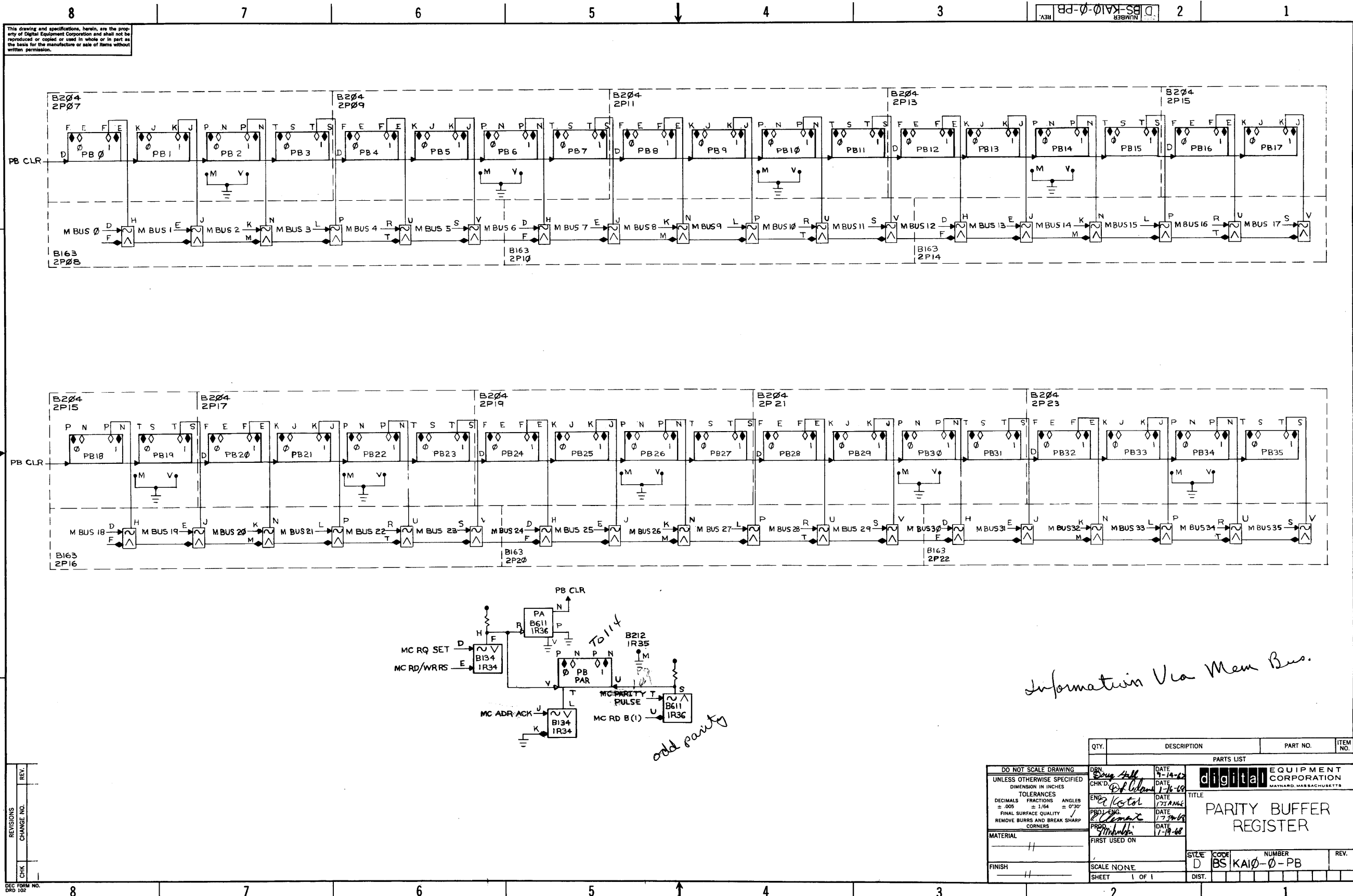


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REV.	CHG.	NO.	DATE	BY
A	1	00049	8/1/66	A. KOTOK
A	2	00050	11/16/69	A. KOTOK

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
± .005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY ✓			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
UNLESS OTHERWISE SPECIFIED		DATE	8/1/66
DWN. <i>[Signature]</i>		DATE	11/16/69
CHK'D. <i>[Signature]</i>		DATE	1/16/69
ENGR. <i>[Signature]</i>		DATE	1/16/69
PROJ. ENGR. <i>[Signature]</i>		DATE	1/16/69
PROD. <i>[Signature]</i>		DATE	1/14/68
FIRST USED ON			
TITLE		NORMALIZE RETURN & NR LONG	
SCALE		SIZE CODE NUMBER REV.	
SHEET OF		DBSKAI0-0-NRNL A-3	



*Information Via Mem Bus.*

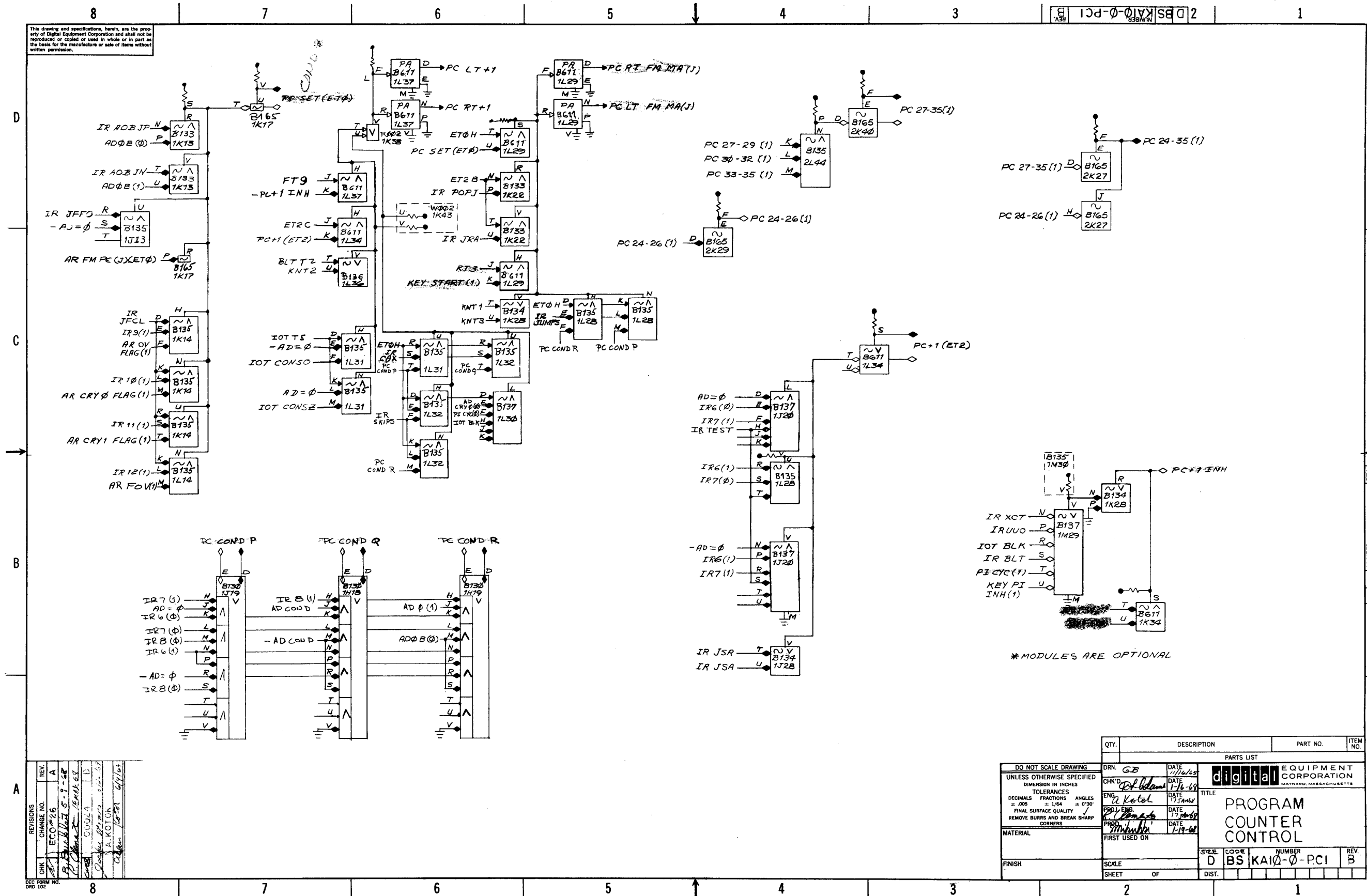
*odd parts*

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES = .005 = 1/64 = 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS		TITLE <b>PARITY BUFFER REGISTER</b>	
MATERIAL FINISH		FIRST USED ON SCALE NONE SHEET 1 OF 1	
REVISIONS CHANGE NO. 1		STYLE CODE NUMBER REV. D BS KA10-0-PB 1	

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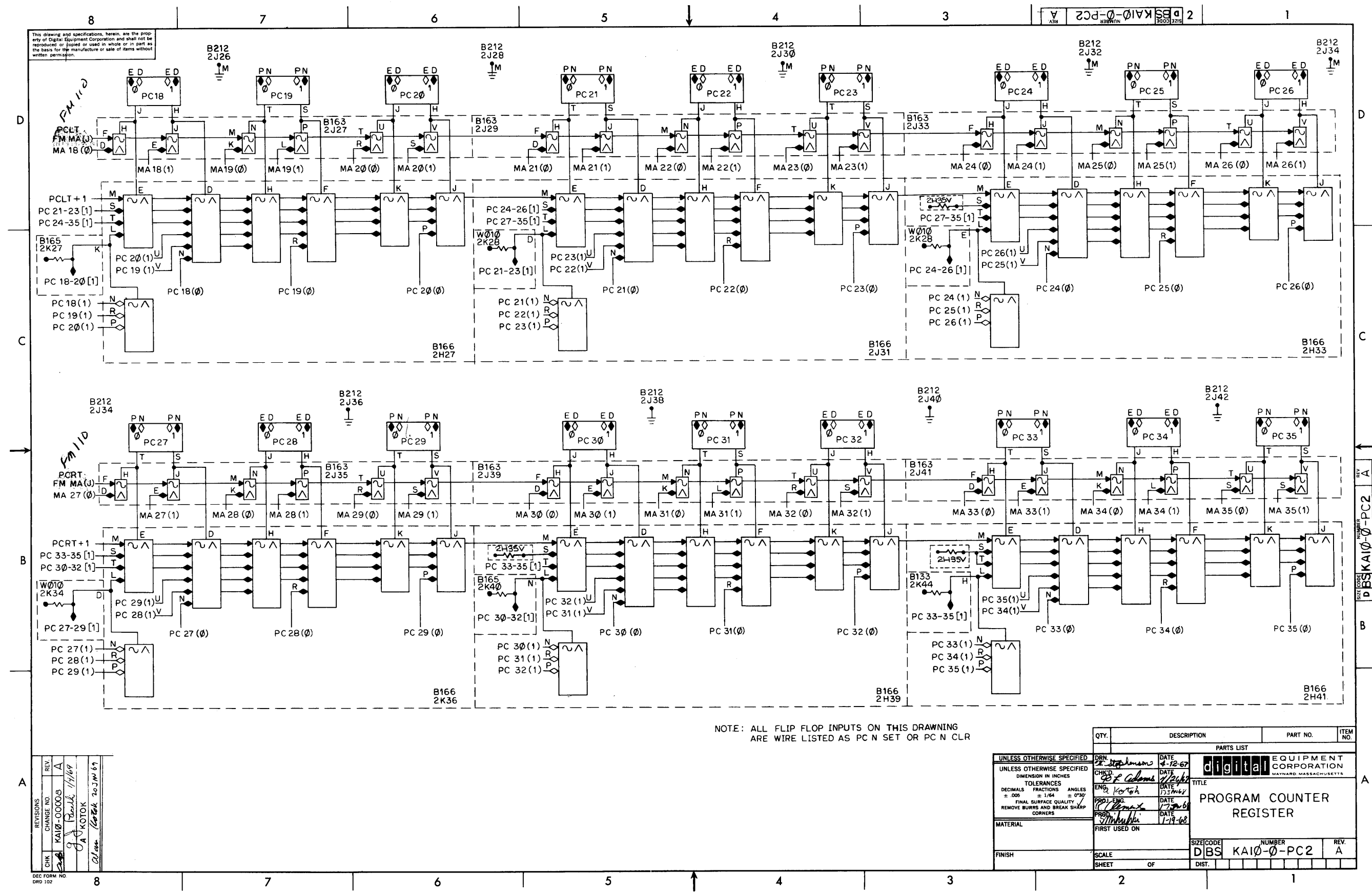
DEC FORM NO. DRD 102

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QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING	DRN. GB	DATE 11/16/65	<b>digital</b> EQUIPMENT CORPORATION MATINEAU, MASSACHUSETTS  <b>PROGRAM COUNTER CONTROL</b>
UNLESS OTHERWISE SPECIFIED	CHK'D <i>W. Kotal</i>	DATE 1-16-66	
DIMENSION IN INCHES	ENG. <i>W. Kotal</i>	DATE 1-16-66	
TOLERANCES	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
DECIMALS FRACTIONS ANGLES	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
± .005 ± .001 ± .030	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
FINAL SURFACE QUALITY	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
REMOVE BURRS AND BREAK SHARP CORNERS	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
MATERIAL	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
FINISH	PROV. ENG. <i>W. Kotal</i>	DATE 1-16-66	
SCALE	SHEET OF	SIZE CODE NUMBER	REV. B
		D BS KAI Q-0-PC I	

REV.	CHANGE NO.	DATE	BY	DESCRIPTION
A	26	1-16-66	W. Kotal	REVISED FOR...
B				
C				
D				
E				
F				
G				
H				
I				
J				
K				
L				
M				
N				
O				
P				
Q				
R				
S				
T				
U				
V				
W				
X				
Y				
Z				



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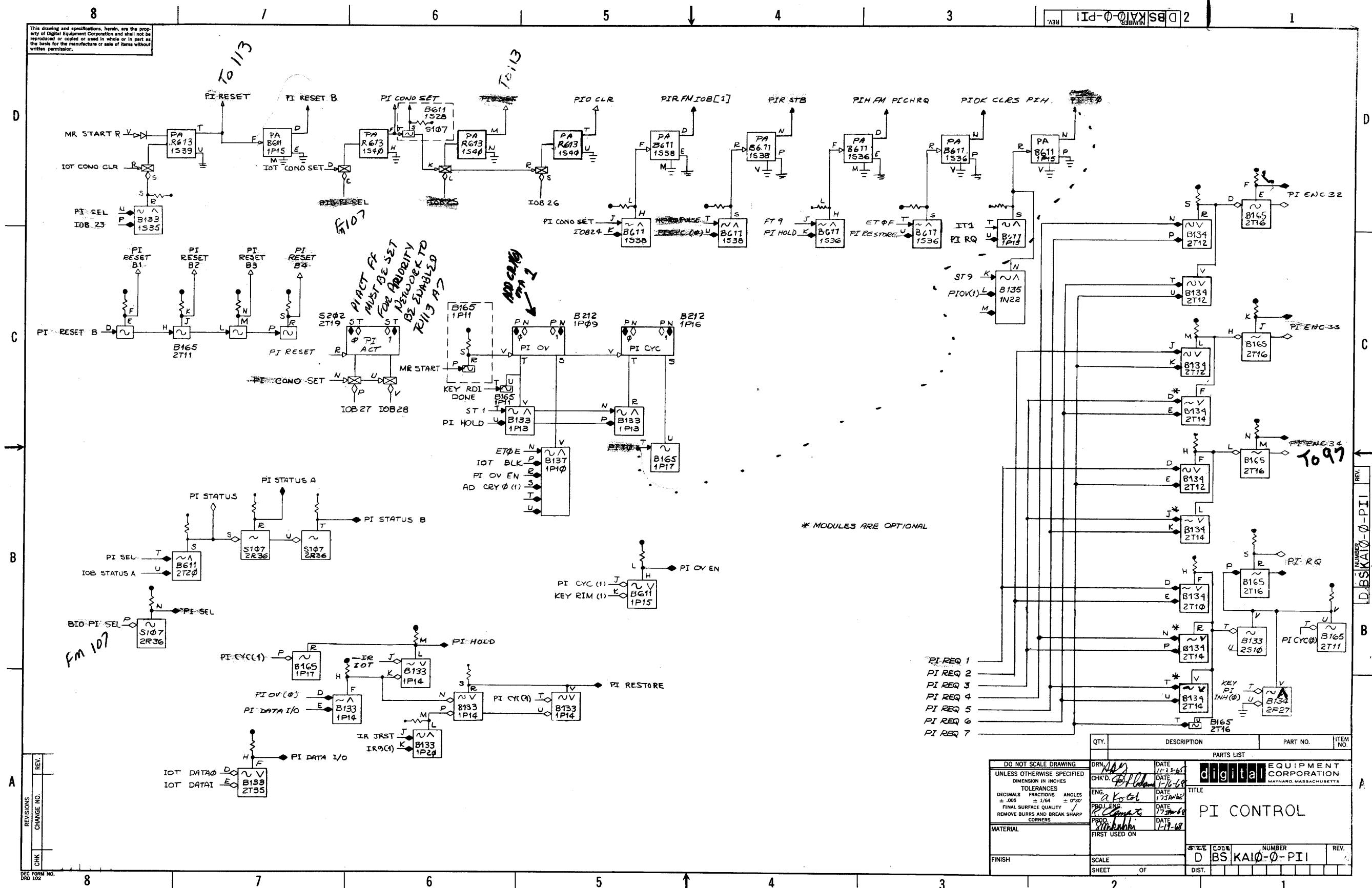
NOTE: ALL FLIP FLOP INPUTS ON THIS DRAWING ARE WIRE LISTED AS PC N SET OR PC N CLR

REV.	CHANGE NO.	REVISIONS
A	1	INITIAL DESIGN
B	2	REVISED FOR MANUFACTURE

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS	FRACTIONS	ANGLES
	± .005	± 1/64	± 0°30'
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	FIRST USED ON		
	SCALE	SHEET	OF
	DIST.		

DRN: *R. Stephenson* DATE: 4-12-67  
 CHKD: *B. Adams* DATE: 4/26/67  
 ENG: *K. Kottick* DATE: 7/31/67  
 PROD. ENG: *L. Kottick* DATE: 1/19/68  
 PROD. *M. Kottick* DATE: 1-19-68  
**digital** EQUIPMENT CORPORATION  
 MAYNARD, MASSACHUSETTS  
 TITLE: PROGRAM COUNTER REGISTER  
 SIZE CODE: DBS NUMBER: KA10-0-PC2 REV. A  
 SHEET OF DIST.

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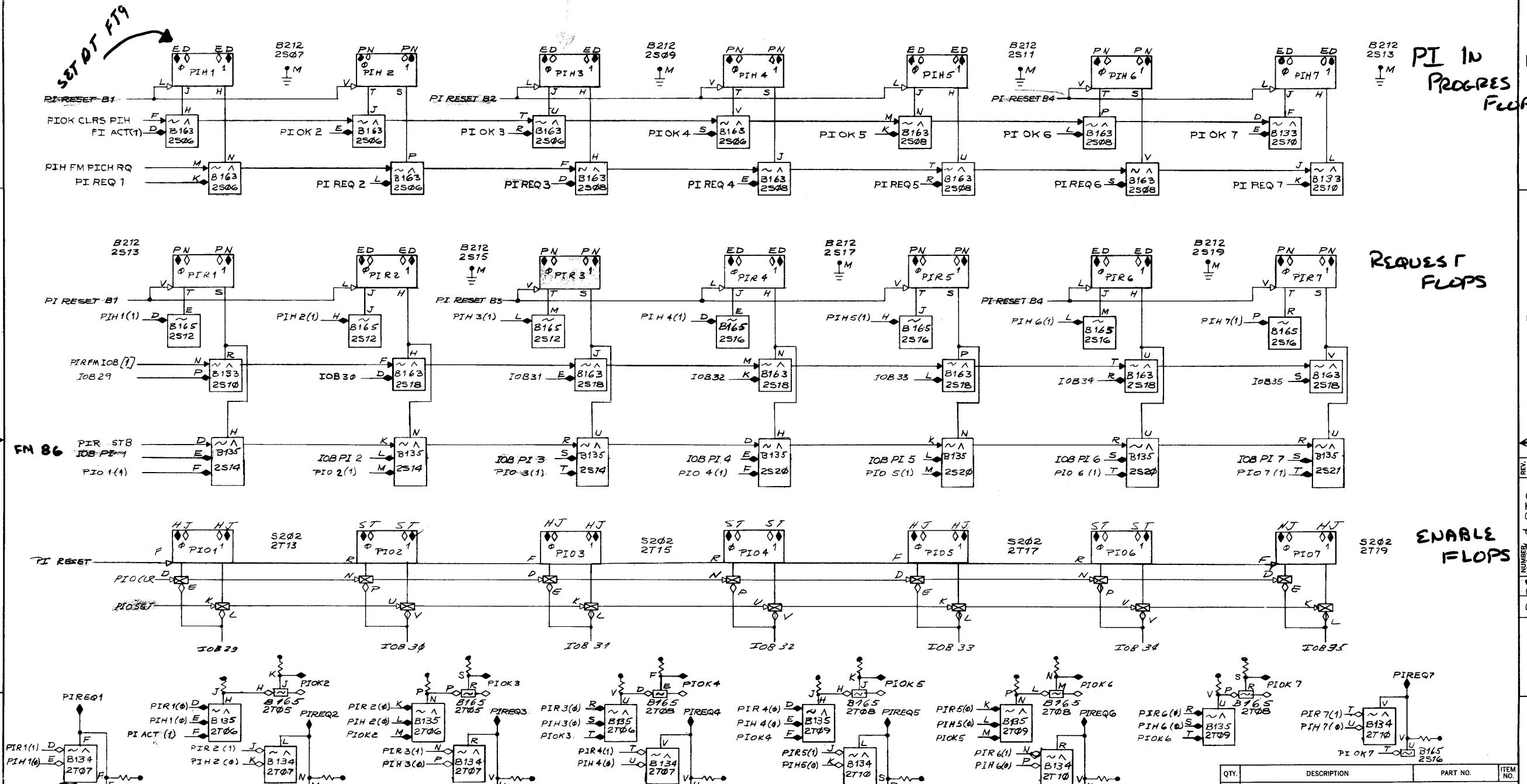
\* MODULES ARE OPTIONAL

- PI REQ 1
- PI REQ 2
- PI REQ 3
- PI REQ 4
- PI REQ 5
- PI REQ 6
- PI REQ 7

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
TITLE: PI CONTROL			
MATERIAL: _____			
FINISH: _____			
SCALE: D BS KA10-0-PII			
SHEET OF _____			
DATE: 11-23-61			
DATE: 1-12-68			
DATE: 1-25-68			
DATE: 1-29-68			
DATE: 1-19-68			
FIRST USED ON: _____			
SIZE	CODE	NUMBER	REV.
D	BS	KA10-0-PII	

REV.	CHANGE NO.

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REVISIONS

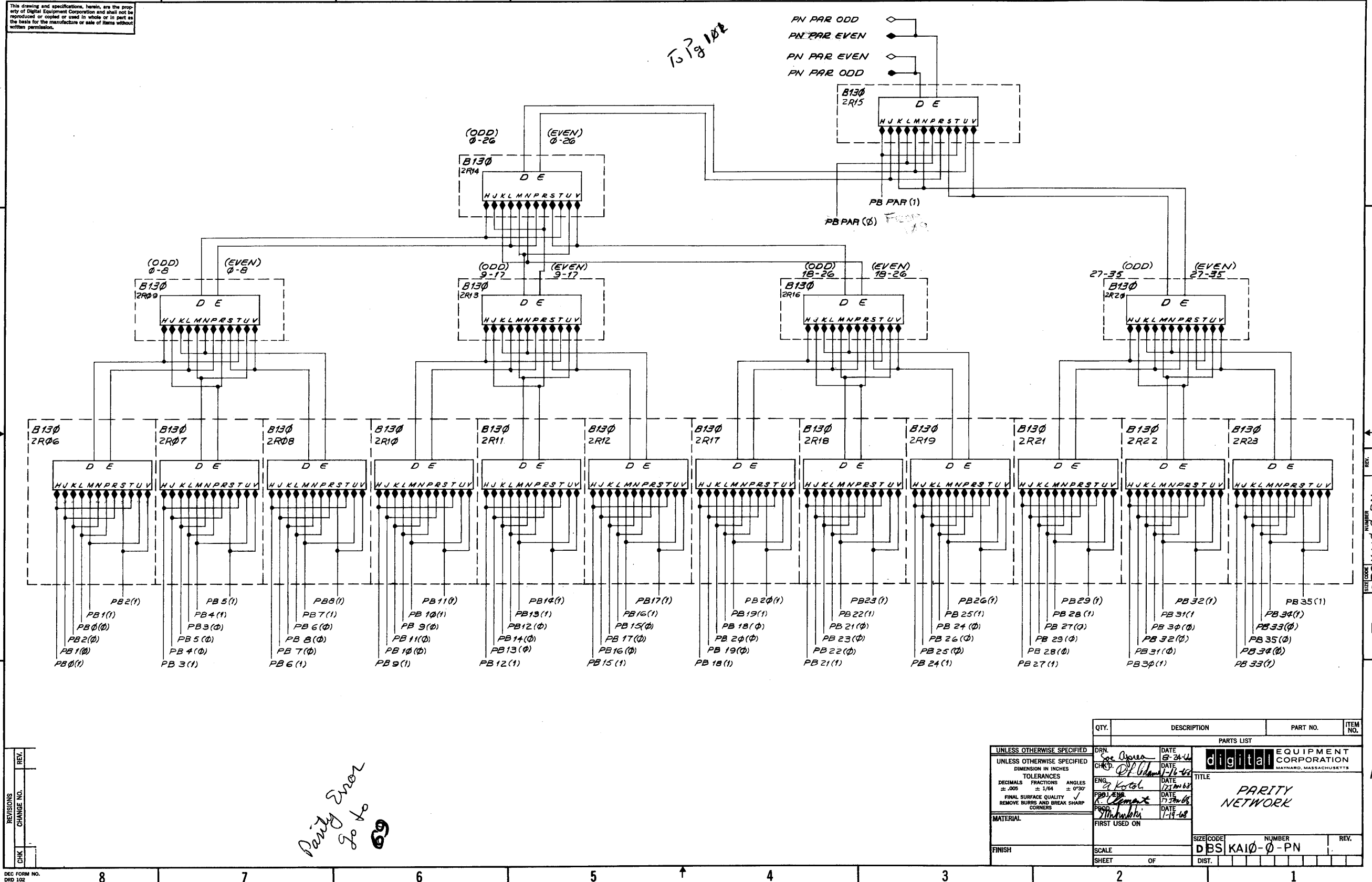
REV.	CHANGE NO.

DEC FORM NO. DRD 102

DO NOT SCALE DRAWING		UNLESS OTHERWISE SPECIFIED	
DIMENSION IN INCHES		TOLERANCES	
DECIMALS	FRACTIONS	ANGLES	= 0°30'
= .005		= 1/64	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
DRN.	DATE	CHKD.	DATE
ENG.	DATE	PRG.	DATE
FIRST USED ON		PARTS LIST	
		digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TITLE			
PRIORITY INTERRUPT PIH, PIR, PIO			
SIZE	CODE	NUMBER	REV.
D	BS1KA10-0-PI2		
SCALE	SHEET	OF	DIST.



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if # of true inputs is odd Pin D = -3v  
Pin Z = gnd

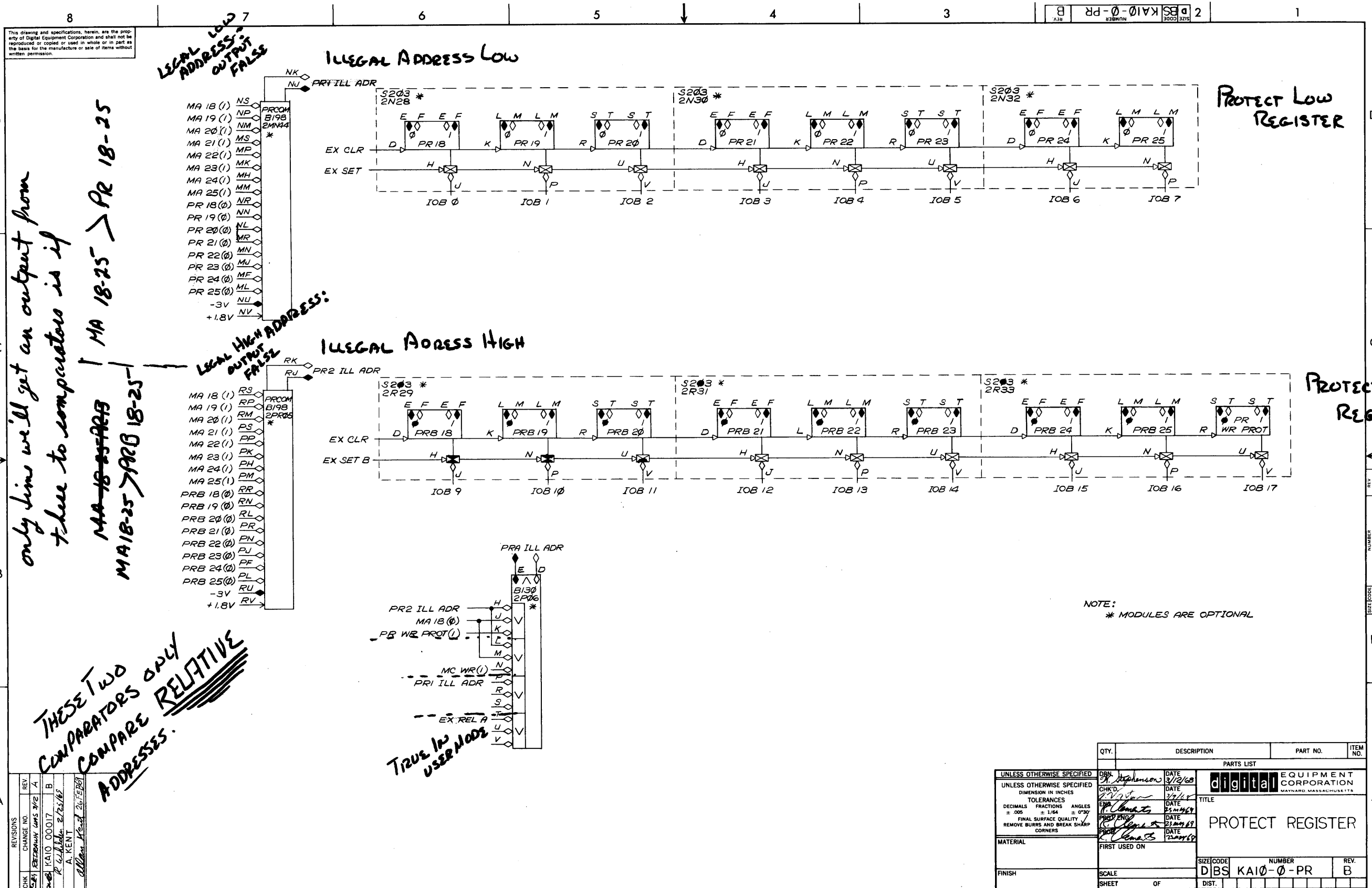
if # of true inputs is even Pin D = gnd  
Pin Z = -3v

Parity Error go to 69

REV.	CHANGE NO.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN. <i>See above</i>	DATE <i>8-24-68</i>
DIMENSION IN INCHES		CHK. <i>D. Williams</i>	DATE <i>1-16-68</i>
TOLERANCES		ENG. <i>A. Kotol</i>	DATE <i>12-10-67</i>
DECIMALS	FRACTIONS	ANGLES	DATE <i>12-10-67</i>
±.005	± 1/64	± 0°30'	DATE <i>12-10-67</i>
FINAL SURFACE QUALITY		PROD. <i>M. M. M.</i>	DATE <i>1-18-68</i>
REMOVE BURRS AND BREAK SHARP CORNERS		TITLE	
MATERIAL		PARITY NETWORK	
FINISH		SIZE CODE	NUMBER
SCALE		D B S	K A I 0 - 0 - P N
SHEET		DIST.	REV.

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only bin will get an output from these to comparators is if MA 18-25 > PR 18-25  
MA 18-25 > PR 18-25  
MA 18-25 > PR 18-25

THESE TWO COMPARATORS ONLY COMPARE RELATIVE ADDRESSES.

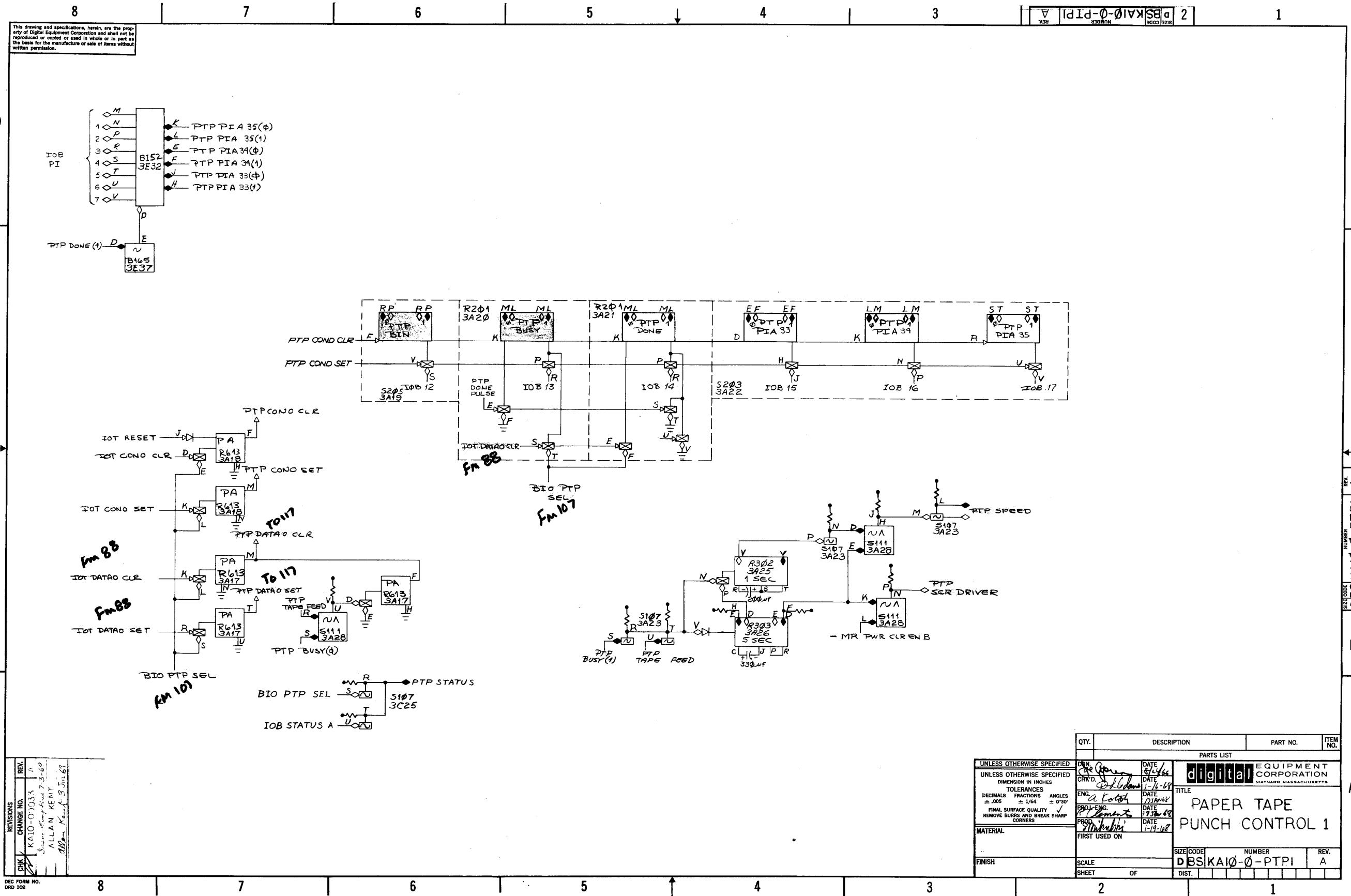
TRUE IN USER MODE

NOTE: \* MODULES ARE OPTIONAL

REV	DATE	BY	CHKD
1	3/12/68	A. KENT	R. STEPHENSON
2	3/14/68	A. KENT	R. STEPHENSON
3	3/14/68	A. KENT	R. STEPHENSON
4	3/14/68	A. KENT	R. STEPHENSON
5	3/14/68	A. KENT	R. STEPHENSON
6	3/14/68	A. KENT	R. STEPHENSON
7	3/14/68	A. KENT	R. STEPHENSON
8	3/14/68	A. KENT	R. STEPHENSON

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED	ORIGIN	DATE	
UNLESS OTHERWISE SPECIFIED	CHK'D	DATE	
TOLERANCES	DATE		
DECIMALS FRACTIONS ANGLES	DATE		
± .005 ± 1/64 ± 0°30'	DATE		
FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS	DATE		
MATERIAL	DATE		
FIRST USED ON			
FINISH	SCALE	SIZE CODE	NUMBER
SHEET	OF	DIBS KA10-0-PR	REV. B
		DIST.	

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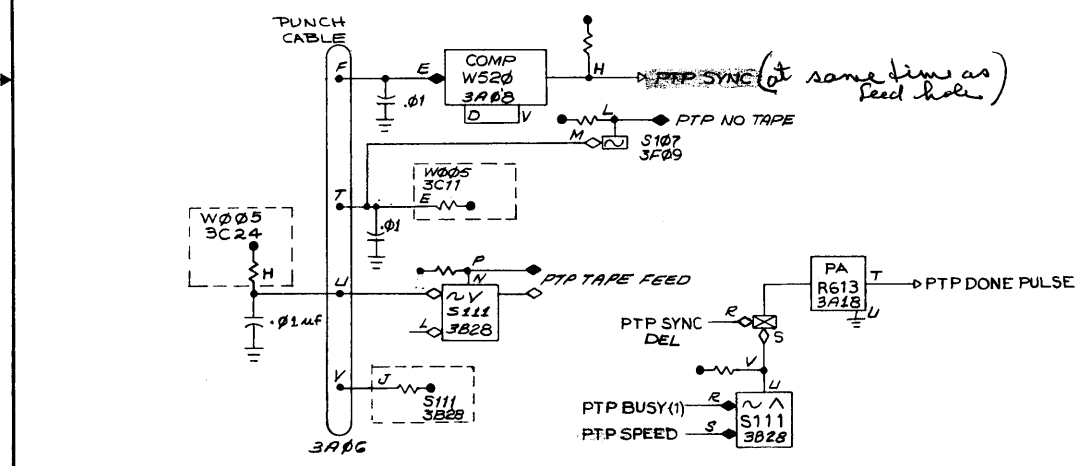
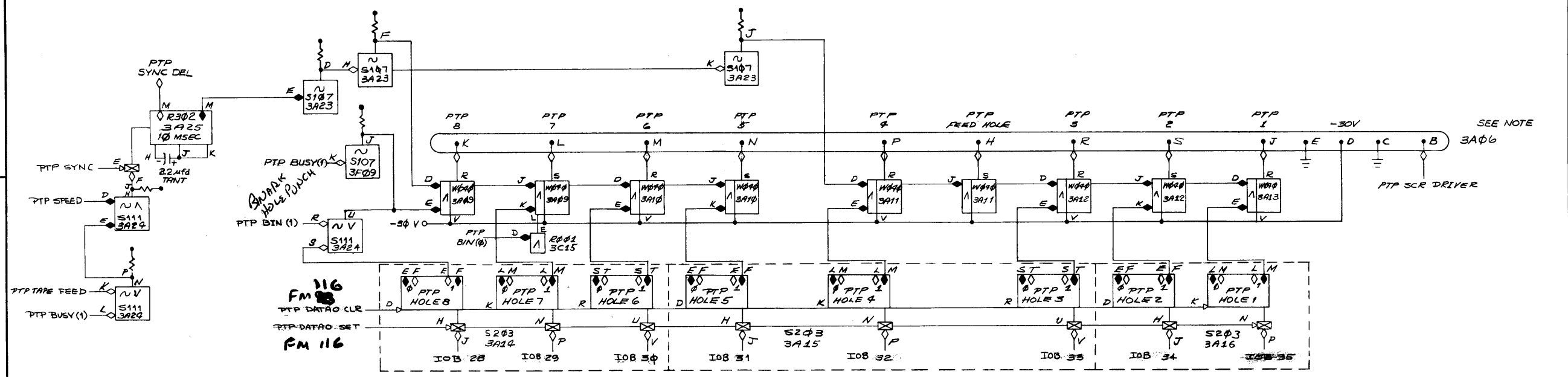


REV.	CHANGE NO.	DATE
1	01033	7-3-60
2	01033	7-3-60
3	01033	7-3-60
4	01033	7-3-60
5	01033	7-3-60
6	01033	7-3-60
7	01033	7-3-60
8	01033	7-3-60

DES FORM NO. ORD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
±.005	± 1/64	± 90°	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE			
SHEET OF			
TITLE		SIZE CODE	NUMBER
PAPER TAPE PUNCH CONTROL 1		DBSKAI0-0-PTPI	A
DATE		DATE	DATE
1-16-68	7-2-68	7-2-68	7-2-68
FIRST USED ON		REV.	
		A	

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*never punch hole  
'7' when in binary,  
always punch hole 8.*

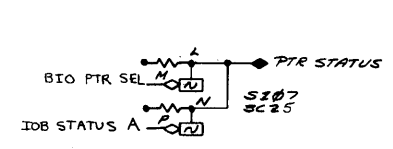
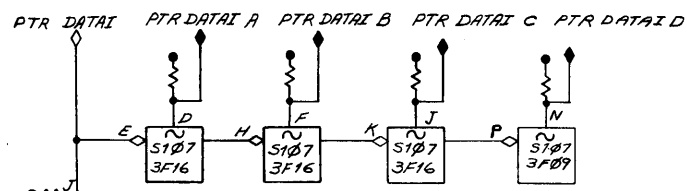
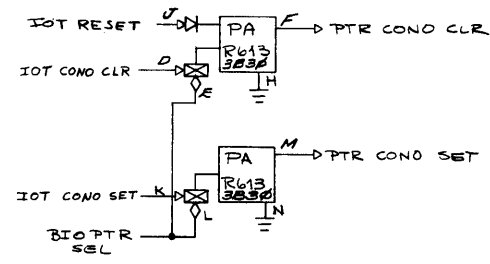
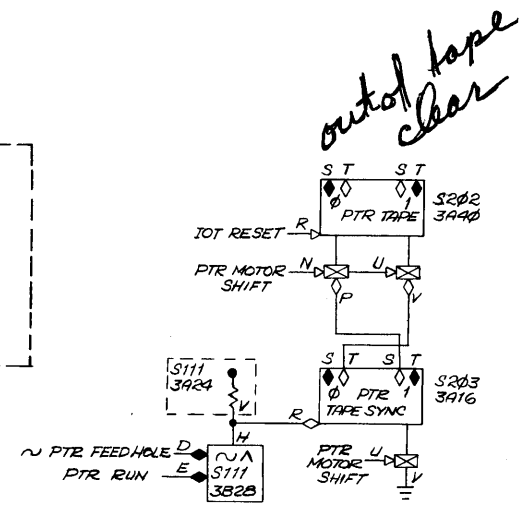
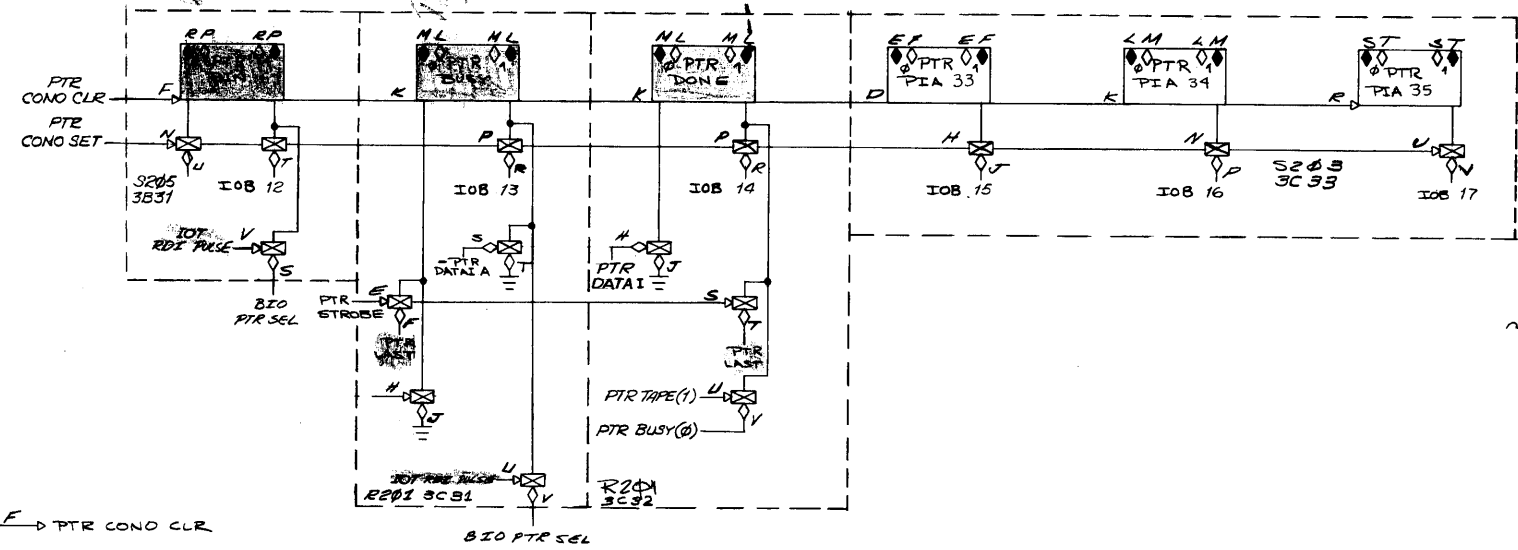
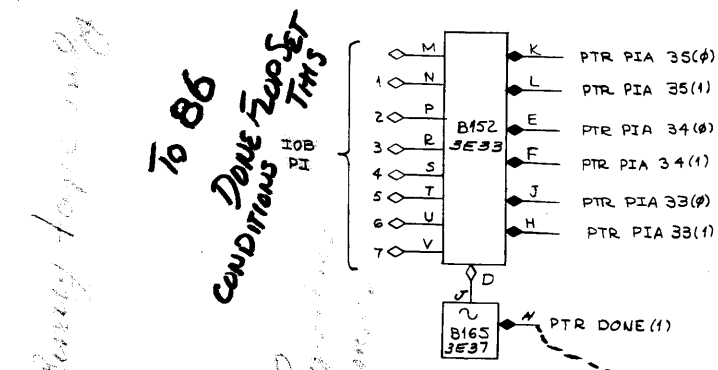
NOTE:  
THIS PUNCH CABLE MUST HAVE  
100 1/4 W RESISTORS IN  
PIN A+B

REV.	CHANGE NO.	DATE
A	3.2	1-16-68

DEC FORM NO. DRD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
± .005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
UNLESS OTHERWISE SPECIFIED			
DESIGN	DATE	digital EQUIPMENT CORPORATION	
ENG.	DATE	MAYNARD, MASSACHUSETTS	
PROD. ENG.	DATE	TITLE	
PROD.	DATE	PAPER TAPE	
FIRST USED ON		PUNCH CONTROL 2	
SCALE	SHEET	OF	DIST.
SIZE CODE		NUMBER	REV.
DBSKAI0-0-PTP2			A

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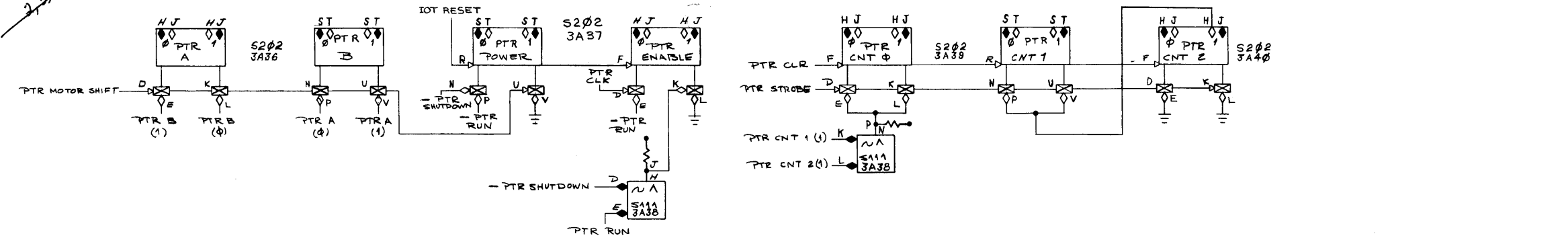
REV.	CHG.	NO.	DATE	BY	DESCRIPTION
1					
2					
3					
4					
5					
6					
7					
8					

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DWN. DATE 8/24/66			
CHD. DATE 11/16/68			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
±.005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FIRST USED ON			
FINISH			
SCALE			
SHEET OF			
TITLE		SIZE CODE	NUMBER
PAPER TAPE READER CONTROL		D BSKAI0-0-PTRI	B
REV.		REV.	
B		B	

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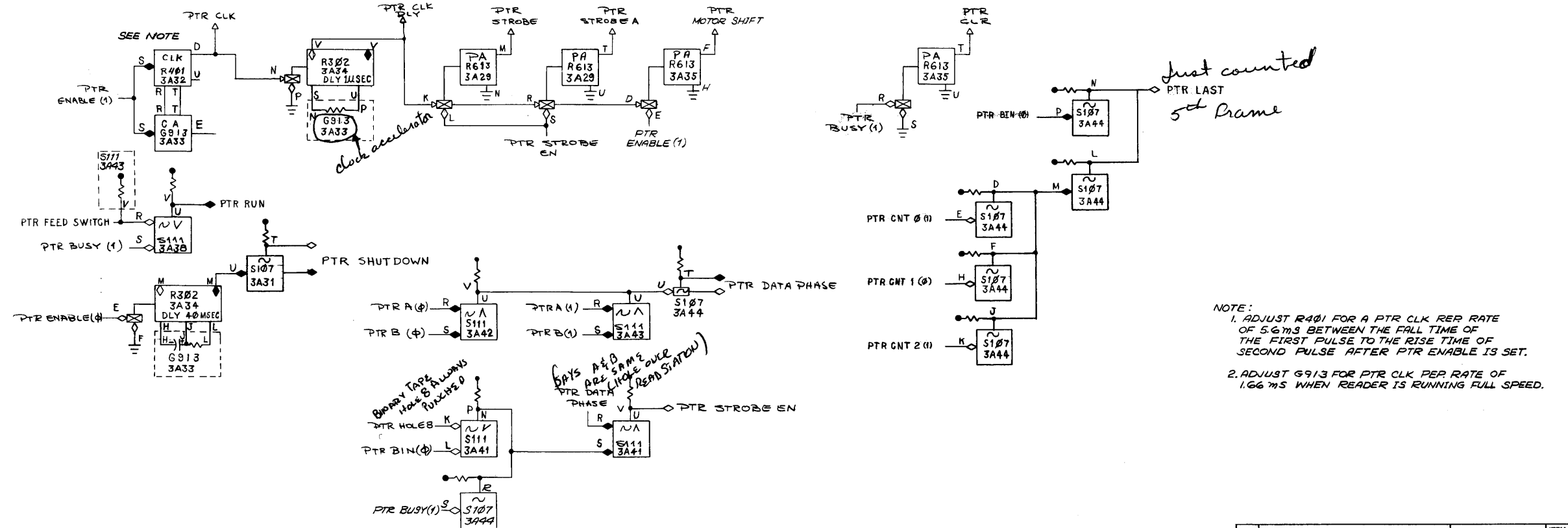
*Ring Counter  
Step counter for  
Steps to step 6  
motor in  
Reader*

*Every step  
= 1.8 degrees  
(200 pulses for  
1 rev)*



Parse

A	B
0	0
1	0
1	1
0	1



NOTE:  
1. ADJUST R401 FOR A PTR CLK REP RATE OF 5.6ms BETWEEN THE FALL TIME OF THE FIRST PULSE TO THE RISE TIME OF SECOND PULSE AFTER PTR ENABLE IS SET.  
2. ADJUST G913 FOR PTR CLK PER RATE OF 1.66ms WHEN READER IS RUNNING FULL SPEED.

REVISIONS

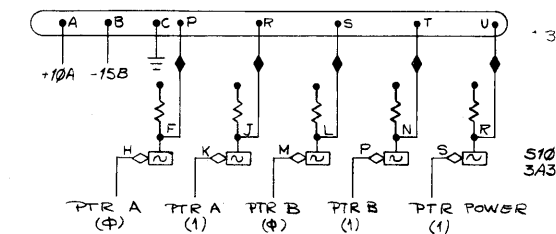
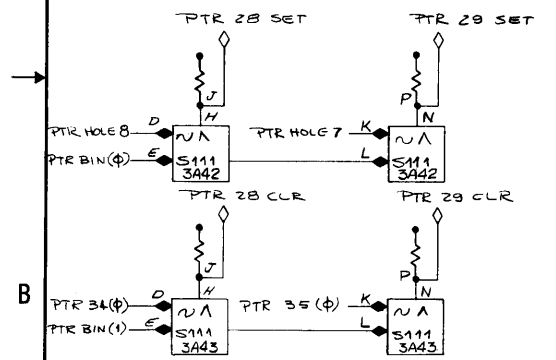
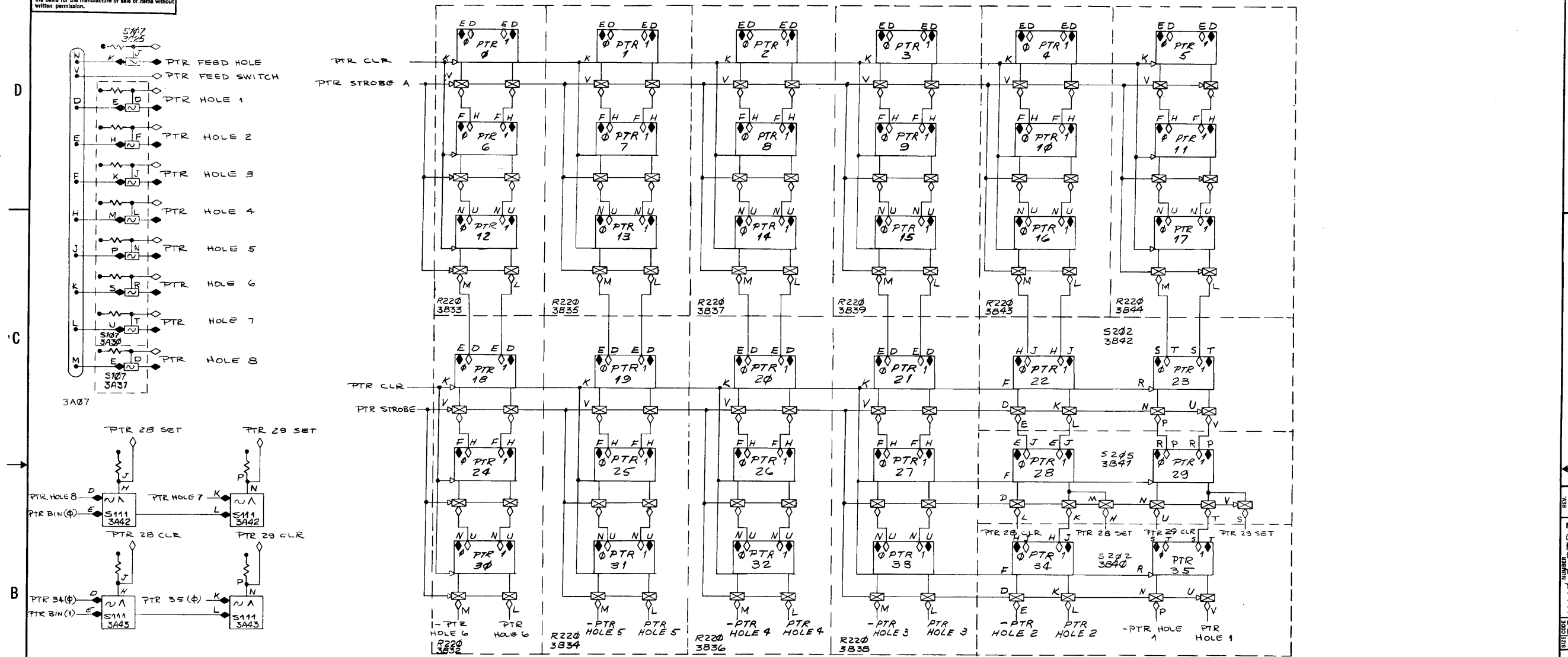
CHK	CHANGE NO.	REV.	DATE
		A	
		B	

8 7 6 5 4 3 2 1

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS FRACTIONS ANGLES			
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FIRST USED ON			
SCALE			
SHEET OF			
DISTRIBUTION			

DRN. <i>Green</i>	DATE <i>8/2/66</i>	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK. <i>John</i>	DATE <i>1/21/68</i>		
ENG. <i>W. J. ...</i>	DATE <i>1/17/68</i>	TITLE PAPER TAPE READER CONTROL	
PROJ. ENG. <i>...</i>	DATE <i>1/17/68</i>		
PROD. <i>M. ...</i>	DATE <i>1/17/68</i>		
SIZE CODE		NUMBER	REV.
D B S K A I 0 - 0 - P T R 2			B ?

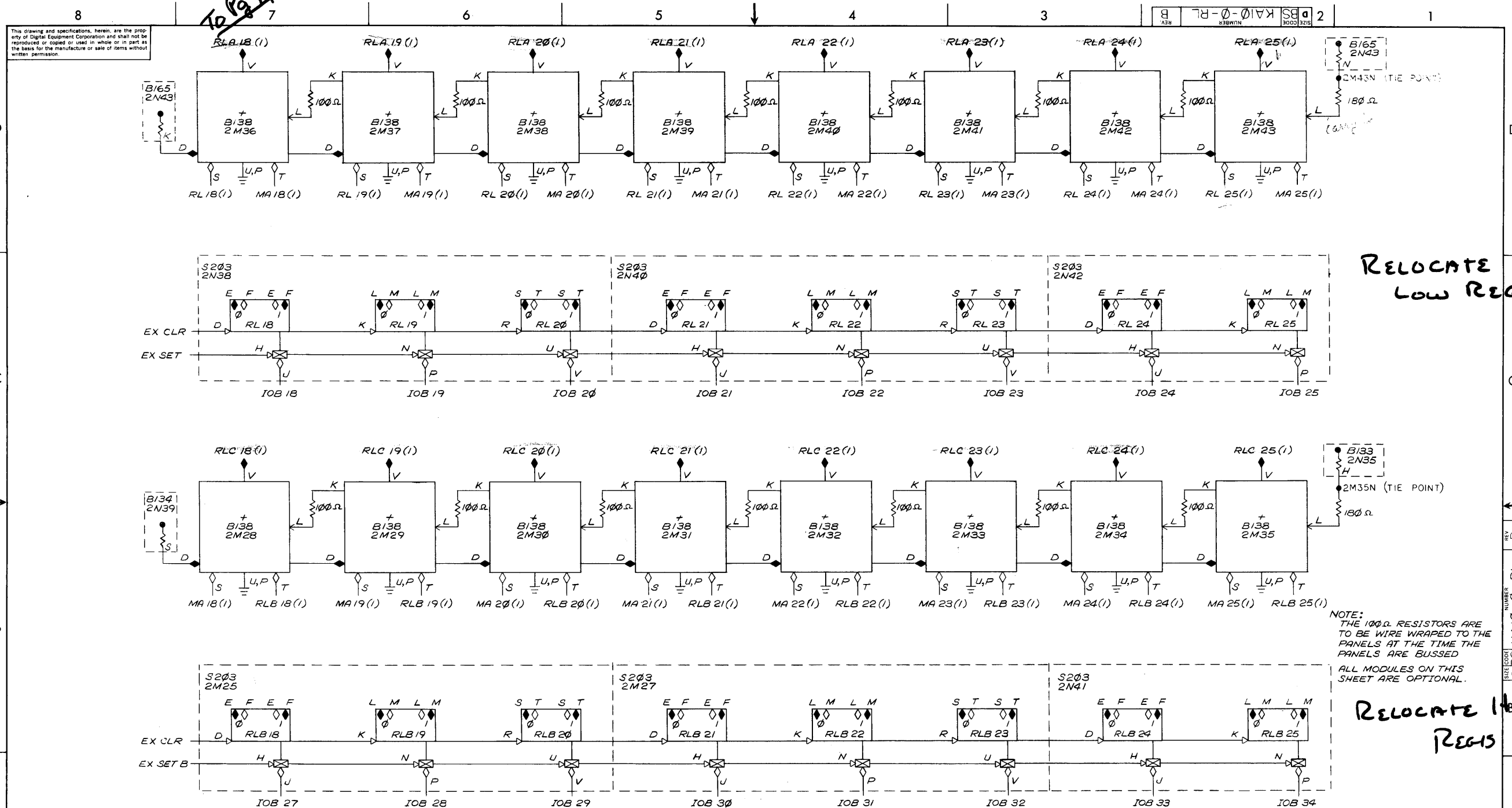
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NOTE: THIS CABLE MUST HAVE WIRE JUMPERS IN PINS A & B

REV.	CHANGE NO.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN. <i>Lee Capria</i> DATE <i>01/24/68</i> DESIGNED <i>P. Williams</i> DATE <i>1-16-68</i> ENGR. <i>W. J. ...</i> DATE <i>1/7/68</i> PROD. ENGR. <i>W. J. ...</i> DATE <i>1/7/68</i> PROD. <i>W. J. ...</i> DATE <i>1-14-68</i>	
UNLESS OTHERWISE SPECIFIED		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ±.005 ±.1/64 ±.030 FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS		TITLE <b>PAPER TAPE                  READER CONTROL</b>	
MATERIAL		SIZE CODE NUMBER	
FINISH		DBS KAI0-0-PTR3 SCALE OF DIST.	



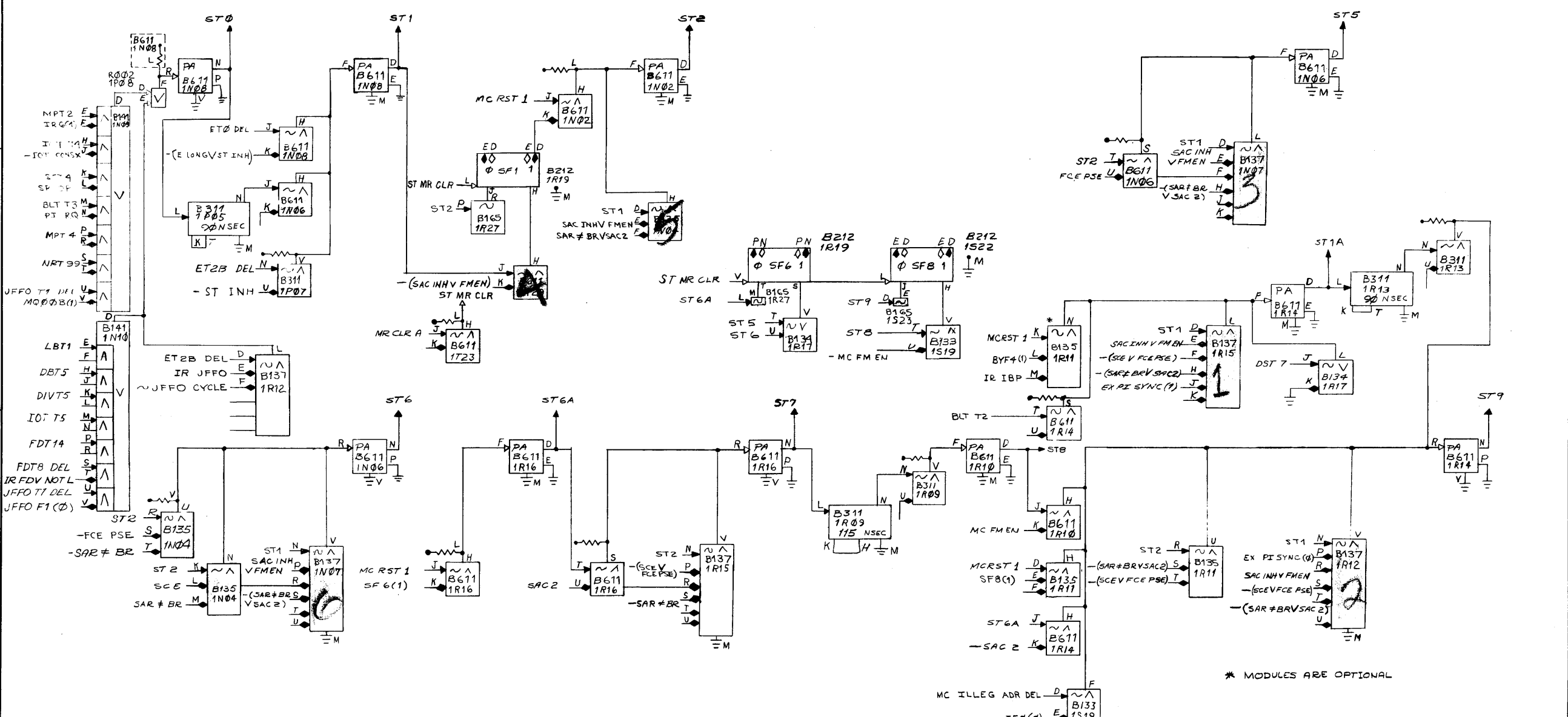
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REV	CHANGE NO	DATE
1	1	1/1/68
2	2	1/1/68
3	3	1/1/68
4	4	1/1/68
5	5	1/1/68
6	6	1/1/68
7	7	1/1/68
8	8	1/1/68

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
± .005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL	FIRST USED ON	SCALE	SHEET OF
FINISH	SCALE	SHEET OF	
TITLE		SIZE CODE	NUMBER
RELOCATE REGISTER		DBS	KA10-0-RL
DATE		REV.	
2/1/68		5	



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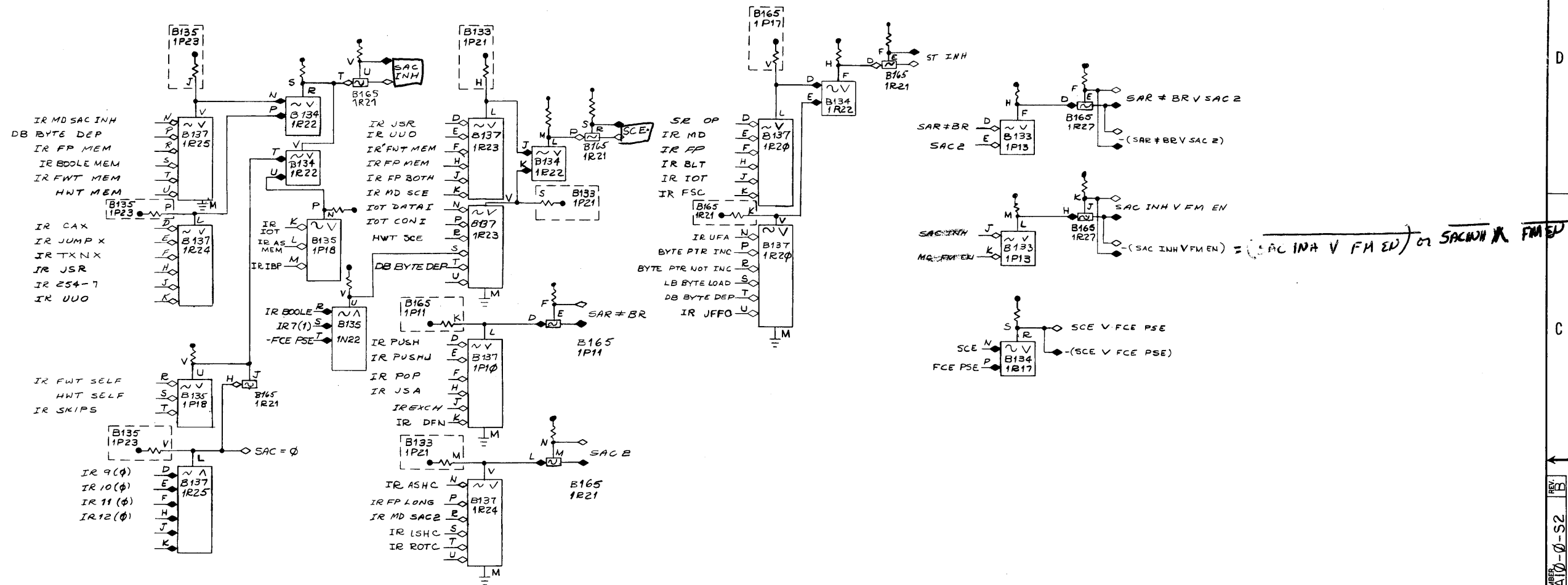
\* MODULES ARE OPTIONAL

REV	CHANGE NO.	DATE	BY	CHK
1	1	11-11-65	W. J. ...	...
2	2	1-11-68	...	...
3	3	7-21-68	...	...
4	4	7-21-68	...	...
5	5	1-19-68	...	...

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	DO NOT SCALE DRAWING		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS FRACTIONS ANGLES		
	± .005 ± 1/64 ± 0°30'		
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET OF		
	DATE		
	BY		
	CHKD		
	ENG		
	PROJ. ENG.		
	PROD.		
	FIRST USED ON		
	SIZE		
	CODE		
	NUMBER		
	DIST.		
	REV		

digital EQUIPMENT CORPORATION  
 MAYNARD, MASSACHUSETTS  
**STORE CYCLE TIME PULSES**  
 SIZE D CODE BS KA 10-0-SI NUMBER 2 REV 2

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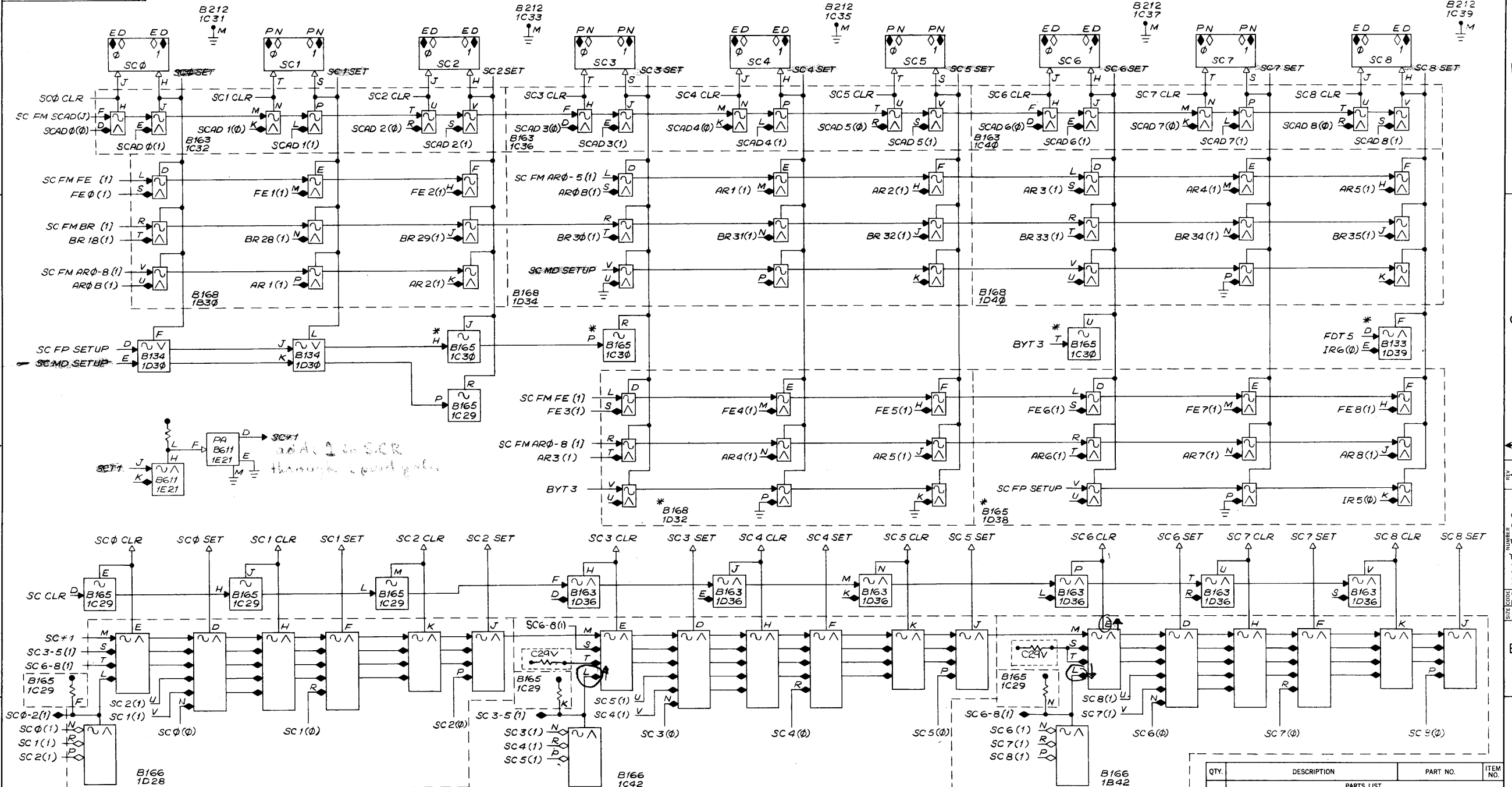
REV.	CHANGE NO.	REVISIONS
1		Initial
2		...
3		...
4		...
5		...
6		...
7		...
8		...

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ±.005 ± 1/64 ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS MATERIAL FINISH			
DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D	DATE	TITLE	
ENG.	DATE	STORE CYCLE LEVELS	
PROJ. ENGR.	DATE	SIZE	CODE
PROD. DATE	DATE	D	BS KA10-0-S2
FIRST USED ON	DATE	NUMBER	REV.
		3	2
SCALE	DIST.		
SHEET	OF		

Initial Switches  
&  
Final Switches

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DBSKAI0-0-SC 2



REV.	NO.	DATE	BY	CHKD.
1	1	1/19/68	W. C. ...	...
2	1	...	...	...

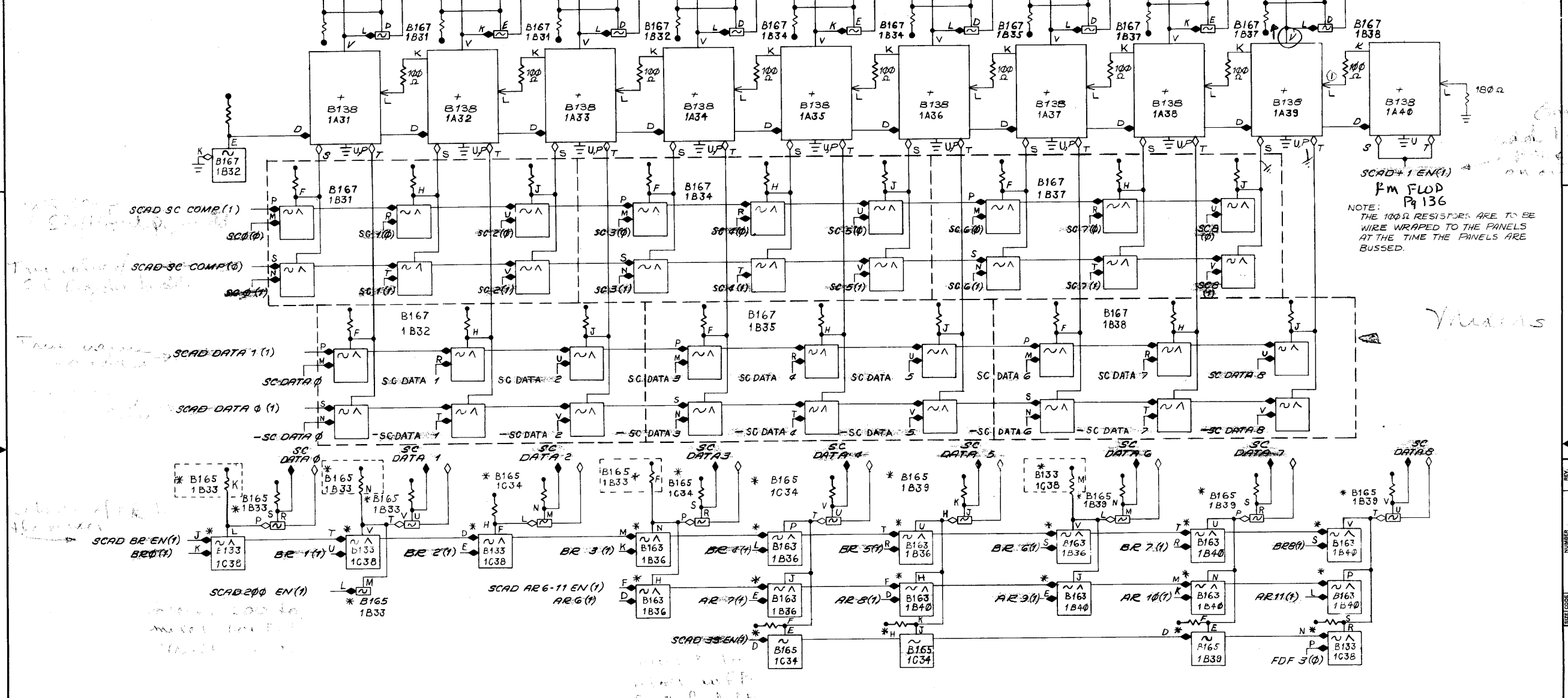
SEC FORM NO. DRD 102

\* MODULES ARE OPTIONAL

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS FRACTIONS ANGLES		
	± .005 ± 1/64 ± 0°30'		
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET OF		

PARTS LIST		TITLE	
DRN.	Dr. Stephenson	DATE	4/29/67
CHKD.	...	DATE	8/1/68
ENG.	...	DATE	1/31/68
PROD. ENG.	...	DATE	1/27/68
PROP.	...	DATE	1-19-68
FIRST USED ON			
SIZE CODE	DBSKAI0-0-SC	NUMBER	A
DIST.		REV.	

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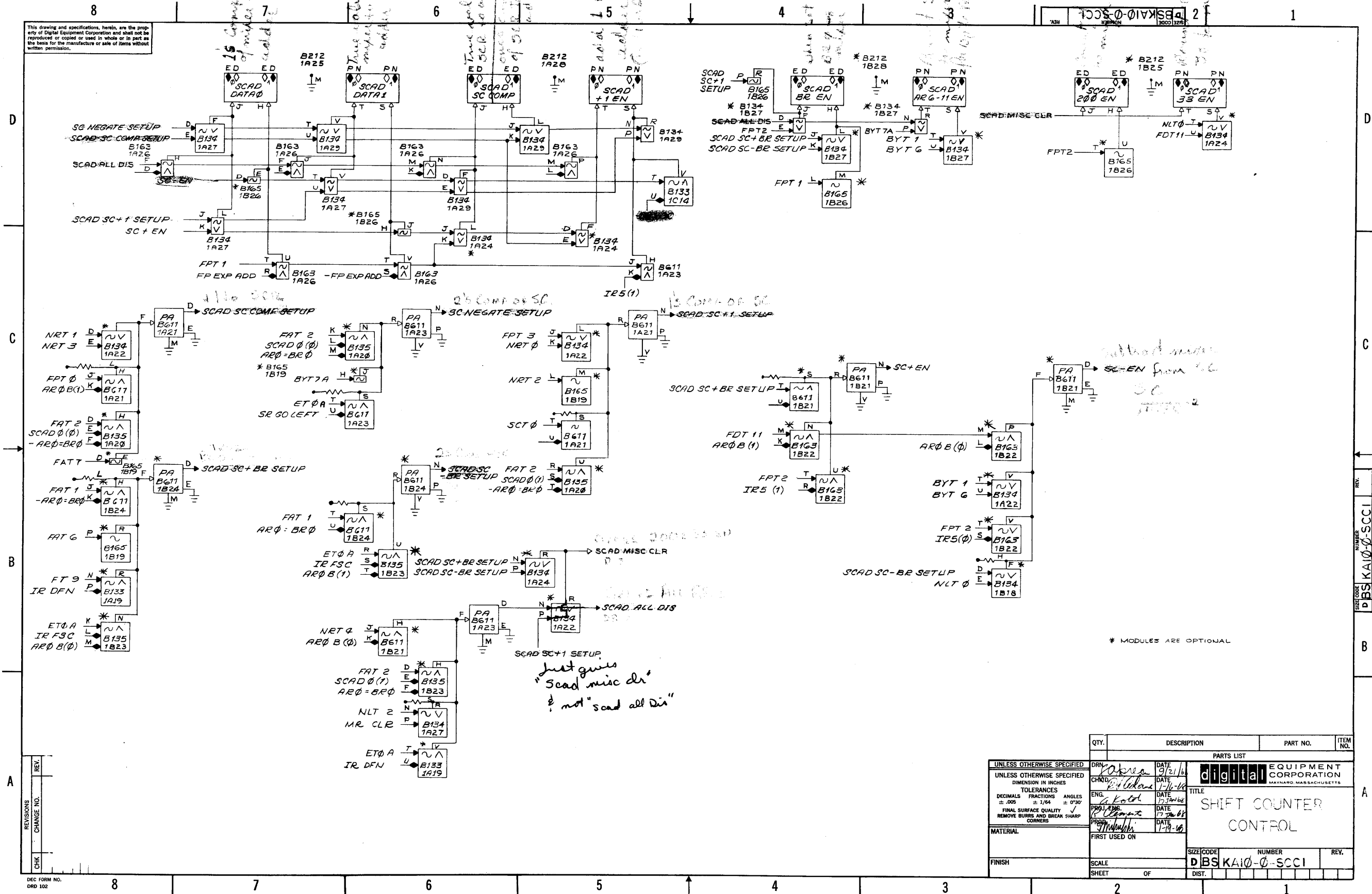
REV.	CHANGE NO.

DEC FORM NO. 100

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED	DRN	DATE	01/15/66
UNLESS OTHERWISE SPECIFIED	CHKD	DATE	1-16-68
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
±.005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY ✓			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FIRST USED ON			
FINISH			
SCALE		NUMBER	
SHEET OF		DBS KAI0-0-SCAD	
DIST.		REV.	

\* MODULES ARE OPTIONAL

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REV.	CHANGE NO.

DEC FORM NO. DRD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED	DRN: <i>John</i>	DATE: 9/21/66	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
UNLESS OTHERWISE SPECIFIED	CHKD: <i>John</i>	DATE: 1-16-66	
TOLERANCES	ENG: <i>John</i>	DATE: 12-1-66	
DECIMALS FRACTIONS ANGLES	PROJ. ENG: <i>John</i>	DATE: 12-2-66	
± .005 ± 1/64 ± 0°30'	PROD. <i>John</i>	DATE: 1-19-66	TITLE <b>SHIFT COUNTER CONTROL</b>
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	FIRST USED ON		SIZE CODE NUMBER <b>DBS KAI0-0-SCCI</b>
MATERIAL	SCALE	DIST.	REV.
FINISH	SHEET	OF	

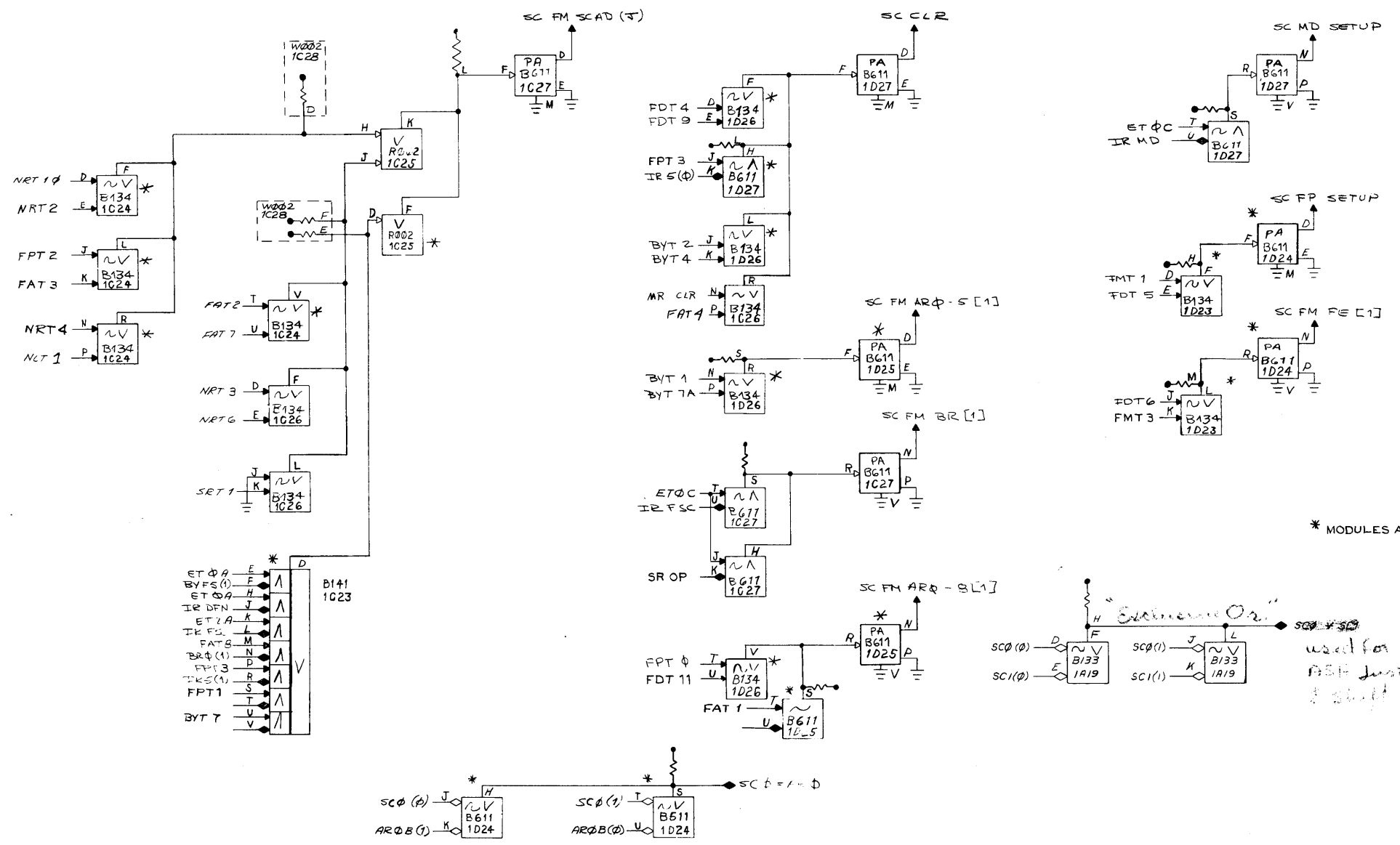
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REV. A  
 NUMBER  
 D B S K A I 0 - 0 - S C C 2  
 SIZE CODE

8 7 6 5 4 3 2 1

D  
 C  
 B  
 A

D  
 C  
 B  
 A



\* MODULES ARE OPTIONAL

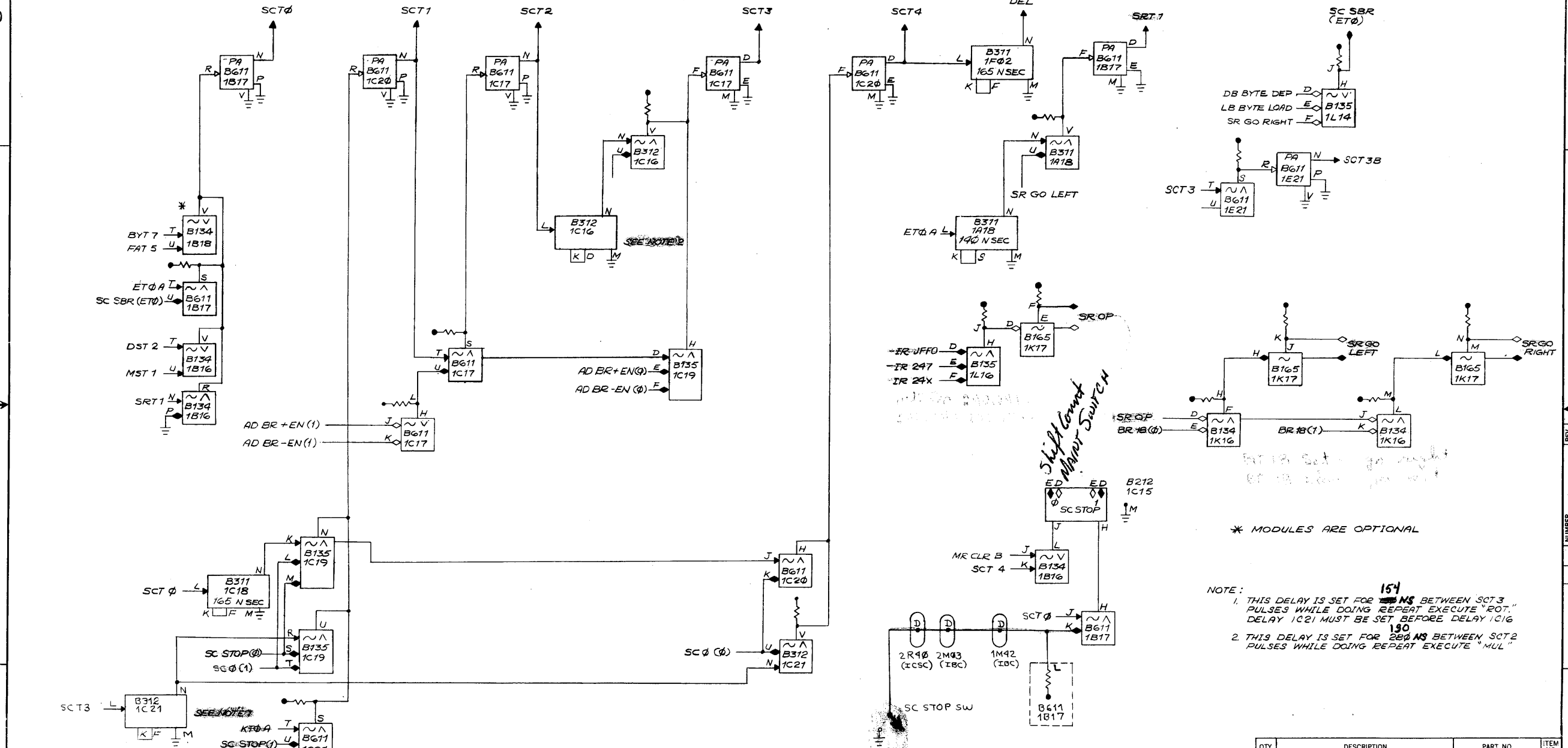
used for  
 ASE just  
 1 shift

REV.	CHANGE NO.	DATE
1		
2		
3		
4		
5		
6		
7		
8		

DEC FORM NO. DRD 102

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN: <i>John...</i> DATE: <i>1-3-66</i> CHRD: <i>John...</i> DATE: <i>1-16-66</i> ENG: <i>John...</i> DATE: <i>1-28-66</i> PROJ. ENG: <i>John...</i> DATE: <i>1-28-66</i> PROD: <i>John...</i> DATE: <i>1-28-66</i>	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ±.005 ± 3/64 ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS		TITLE <b>SHIFT COUNTER CONTROL</b>	
MATERIAL		FIRST USED ON	
FINISH		SCALE	
SHEET		OF	
SIZE CODE		NUMBER	
D B S K A I 0 - 0 - S C C 2		REV. A	

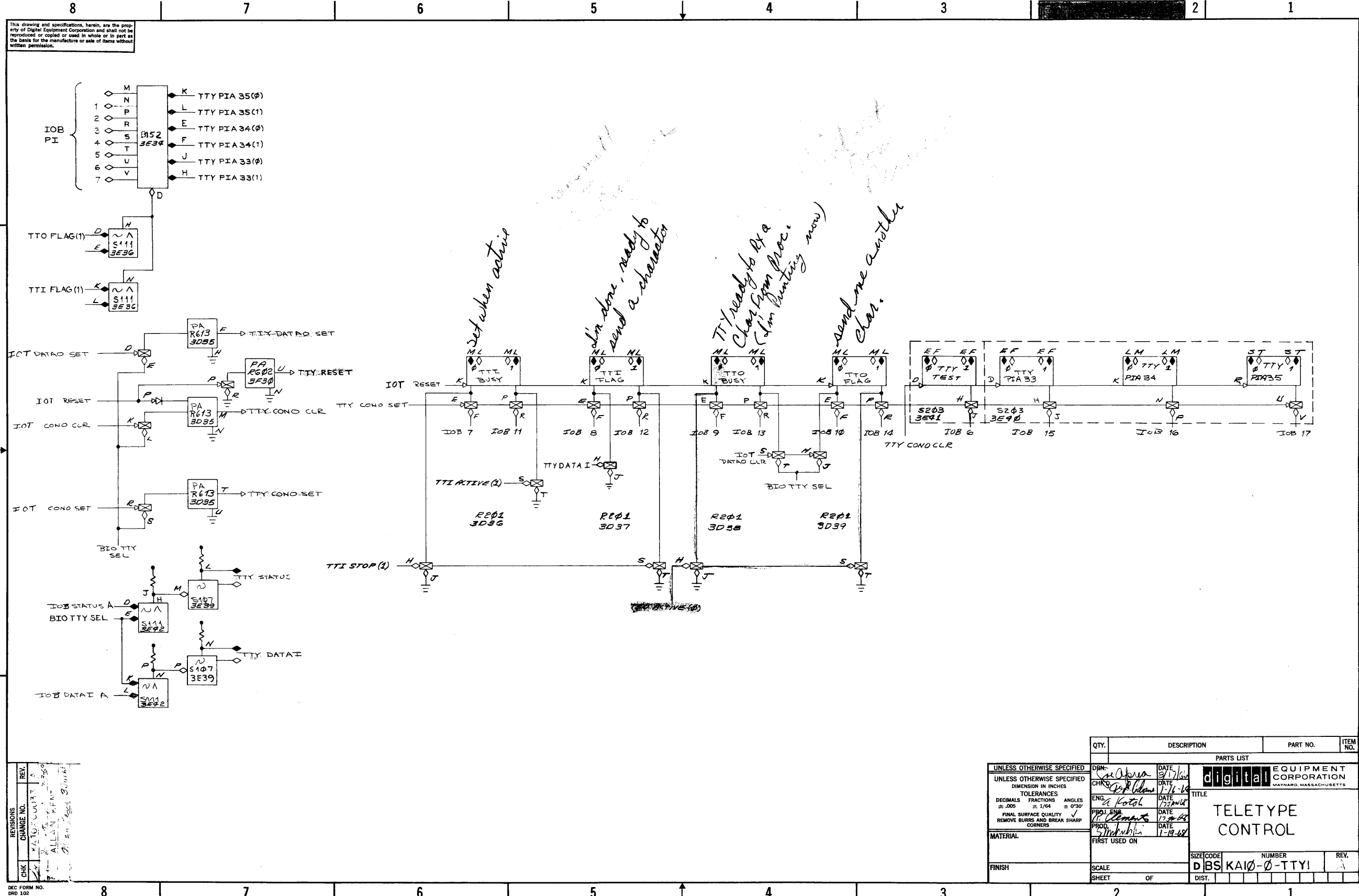
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NOTE:  
 1. THIS DELAY IS SET FOR 154 NS BETWEEN SCT3 PULSES WHILE DOING REPEAT EXECUTE "ROT." DELAY 1C21 MUST BE SET BEFORE DELAY 1C16  
 2. THIS DELAY IS SET FOR 280 NS BETWEEN SCT2 PULSES WHILE DOING REPEAT EXECUTE "MUL"

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
1	DO NOT SCALE DRAWING	DATE 11-23-66	
1	UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DATE 11-11-66	
1	TOLERANCES	DATE 12-14-66	
1	DECIMALS ± .005	DATE 12-14-66	
1	FRACTIONS ± 1/64	DATE 12-14-66	
1	ANGLES ± 0'30"	DATE 12-14-66	
1	FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DATE 12-14-66	
1	MATERIAL	DATE 12-14-66	
1	FINISH	DATE 12-14-66	
1	FIRST USED ON	DATE 12-14-66	
1	SCALE	DATE 12-14-66	
1	SHEET OF	DATE 12-14-66	
1	DIST.	DATE 12-14-66	
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE: SHIFT & CNT SUBRTN & SHIFT INST SIZE: D NUMBER: BS KA10-0-SCSR REV: A			

REV	CHG	NO	DATE	BY
1	1	1	11-23-66	WJ
2	1	1	11-11-66	E. J. Holden
3	1	1	12-14-66	E. J. Holden
4	1	1	12-14-66	E. J. Holden



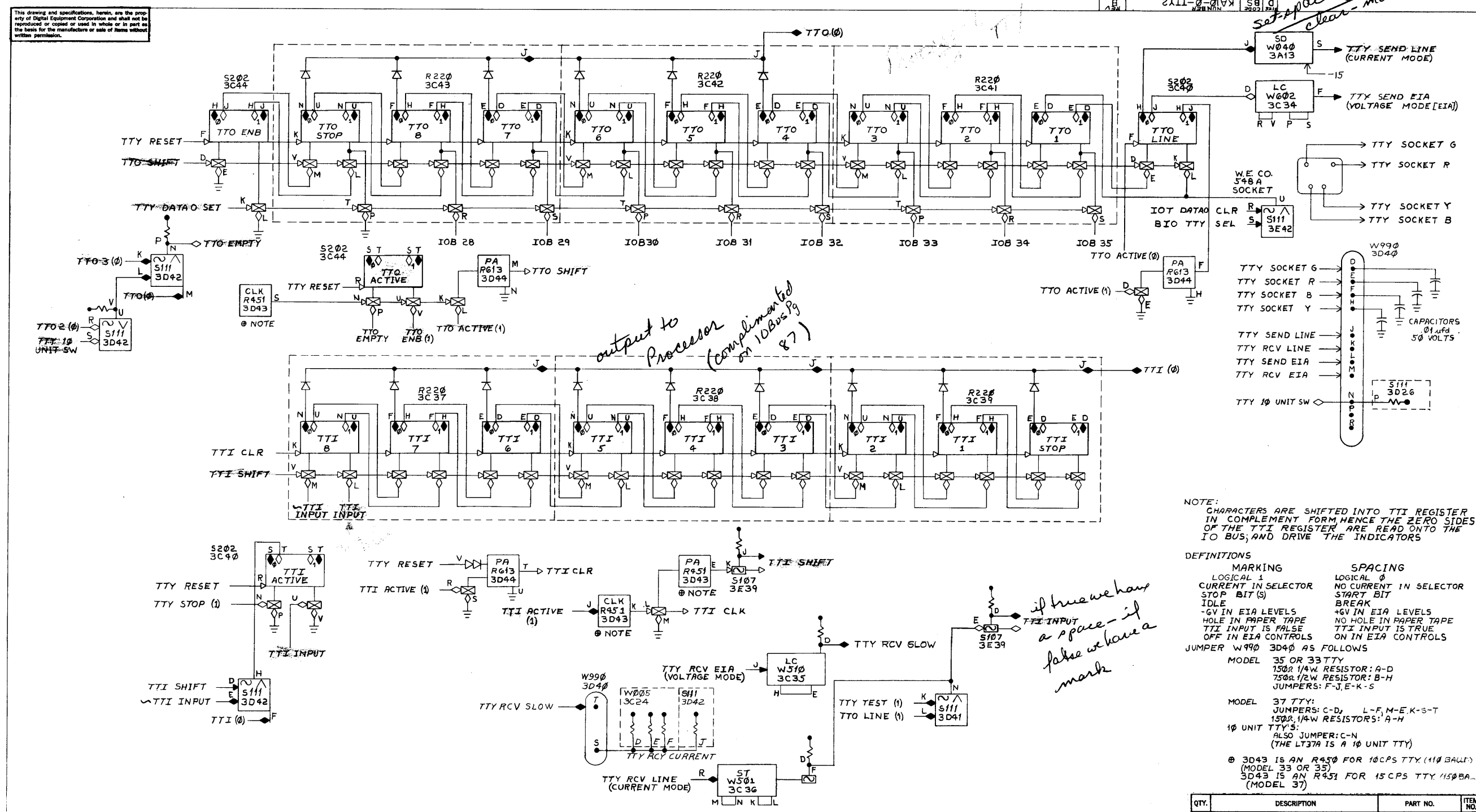
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REV.	CHANGE NO.	DATE	BY
1	1	1-16-68	W. J. COVAT
2	2	1-16-68	W. J. COVAT
3	3	1-16-68	W. J. COVAT
4	4	1-16-68	W. J. COVAT
5	5	1-16-68	W. J. COVAT
6	6	1-16-68	W. J. COVAT
7	7	1-16-68	W. J. COVAT
8	8	1-16-68	W. J. COVAT

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS	FRACTIONS	ANGLES	
±.005	± 1/64	± 0°30'	
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE			
SHEET OF			
TITLE		REV.	
TELETYPE CONTROL		A	
SIZE CODE		NUMBER	
D BS KA10-0-TTY1		A	
DIST.			



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NOTE: CHARACTERS ARE SHIFTED INTO TTI REGISTER IN COMPLEMENT FORM HENCE THE ZERO SIDES OF THE TTI REGISTER ARE READ ONTO THE IO BUS; AND DRIVE THE INDICATORS

DEFINITIONS

MARKING	SPACING
LOGICAL 1	LOGICAL 0
CURRENT IN SELECTOR	NO CURRENT IN SELECTOR
STOP BIT (S)	START BIT
IDLE	BREAK
-6V IN EIA LEVELS	+6V IN EIA LEVELS
HOLE IN PAPER TAPE	NO HOLE IN PAPER TAPE
TTI INPUT IS FALSE	TTI INPUT IS TRUE
OFF IN EIA CONTROLS	ON IN EIA CONTROLS

JUMPER W990 3D40 AS FOLLOWS

MODEL 35 OR 33 TTY:  
150R 1/4W RESISTOR: A-D  
750R 1/2W RESISTOR: B-H  
JUMPERS: F-J, E-K-S

MODEL 37 TTY:  
JUMPERS: C-D, L-F, M-E, K-S-T  
150R 1/4W RESISTORS: A-H

10 UNIT TTY'S:  
ALSO JUMPER: C-N  
(THE LT37A IS A 10 UNIT TTY)

3D43 IS AN R450 FOR 10CPS TTY (110 BAUD)  
(MODEL 33 OR 35)  
3D43 IS AN R451 FOR 15CPS TTY (150 BAUD)  
(MODEL 37)

REV.	CHG.	NO.	BY	DATE
1	WHELDEN	2/25/69	A. KENT	2/25/69
2	NO CHANGE	3/11/69	A. KENT	3/11/69
3	NO CHANGE	3/11/69	A. KENT	3/11/69
4	NO CHANGE	3/11/69	A. KENT	3/11/69
5	NO CHANGE	3/11/69	A. KENT	3/11/69
6	NO CHANGE	3/11/69	A. KENT	3/11/69
7	NO CHANGE	3/11/69	A. KENT	3/11/69
8	NO CHANGE	3/11/69	A. KENT	3/11/69
9	NO CHANGE	3/11/69	A. KENT	3/11/69
10	NO CHANGE	3/11/69	A. KENT	3/11/69

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	UNLESS OTHERWISE SPECIFIED		
	DIMENSION IN INCHES		
	TOLERANCES		
	DECIMALS FRACTIONS ANGLES		
	±.005 ±.002 ±.001 ±.0005 ±.0002 ±.0001		
	FINAL SURFACE QUALITY		
	REMOVE BURRS AND BREAK SHARP CORNERS		
	MATERIAL		
	FINISH		
	SCALE		
	SHEET 1 OF 1		
	DATE 11/24/66		
	CHK'D. D. ADAMS		
	DATE 1/16/67		
	ENG. A. KOTOK		
	DATE 1/17/67		
	PROJ. ENG. R. CLEMENTS		
	DATE 1/17/67		
	PROD. S. MIKULSKI		
	DATE 1/17/67		
	FIRST USED ON		
	TITLE		
	TELETYPE CONTROL		
	SIZE CODE		
	NUMBER		
	REV.		
	D.B.S. KA10-0-TTY2		
	DIST.		



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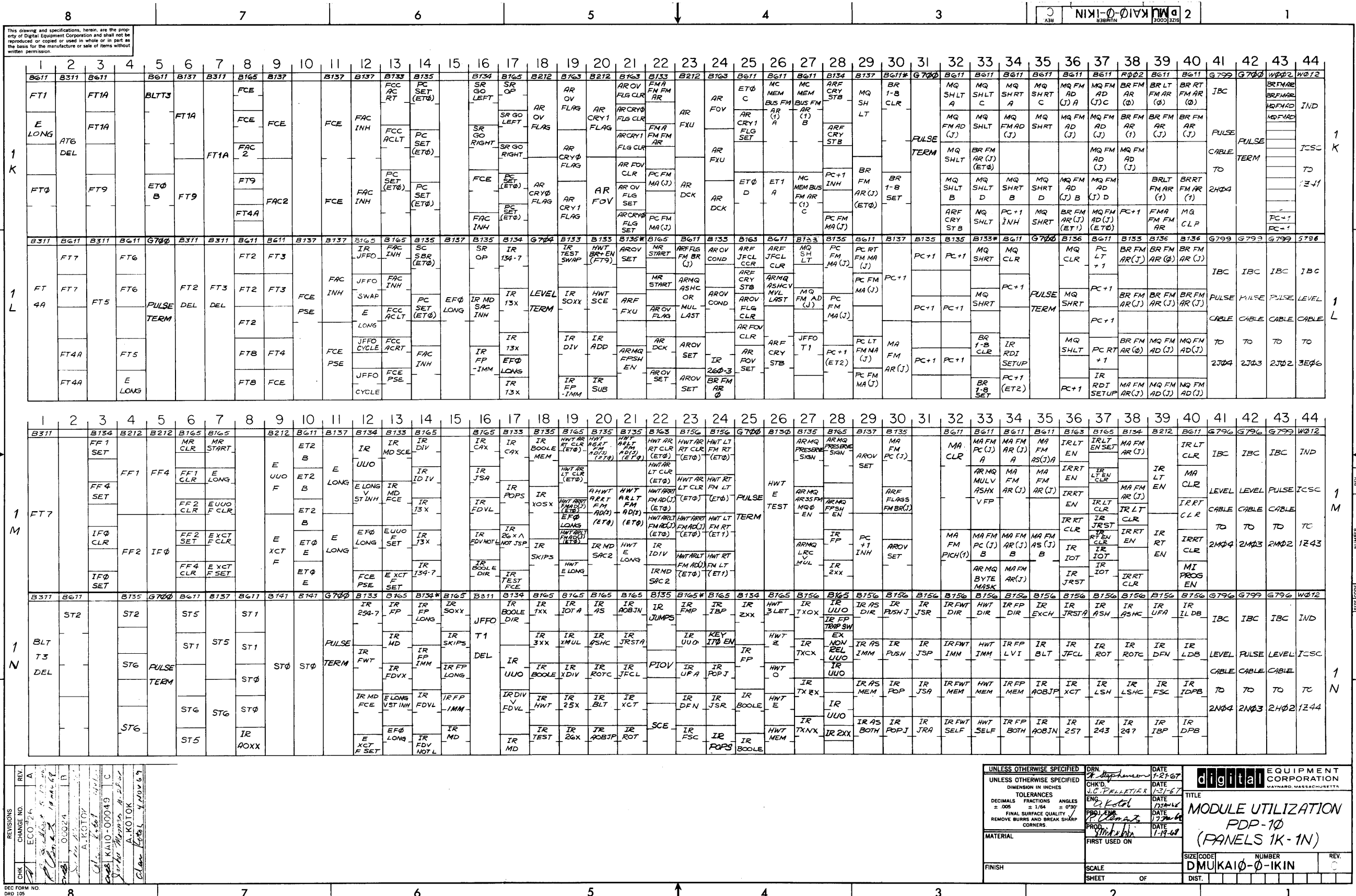
Table with columns 1-44 and rows D 1 E, D 1 F, C. Contains circuit logic descriptions such as FDT1 DE-LAYED, DST1, DIVT4 DEL, and various pulse and timing components.

Table with columns 1-44 and rows B, H, C. Contains circuit logic descriptions such as MPF2 DEL, AD BR+ EN, AR FM AD(J), and various timing and control logic components.

REVISIONS table listing change numbers, dates, and descriptions for the drawing.

DEC FORM NO. DRD 105

Technical specification block including tolerances (0.008, 0.0125, 0.025), surface quality, and equipment identification (DMUKAI0-0-IEI). Includes a title block with 'MODULE UTILIZATION PDP-10 (PANELS 1E - 1J)' and 'digital EQUIPMENT CORPORATION'.



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8 7 6 5 4 3 2 1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44				
R303	R302	R401	B611	B311	G700	B311	R002	B212	B137	B165	G700	B133	B133	B611	B212	B165	B135	B137	B133	B133	B133	B212	B135*		B212	B130	B156	B156	B156	B156	B156	B156	B156	B156	B156	B156	B156	B156*	B156	B156	G796	G796	G799	G796			
↑	MR PWR CLR ENB	MR PWR CLR R	JFFO T1				ST Ø	AF 2	SAR # BR	SAR # BR	SAR # BR	SAR # BR	SAR # BR	SAR # BR	EX PI HOLD	EX PI HOLD	EX PI HOLD	EX PI HOLD	EX PI HOLD	EX PI HOLD	EX PI HOLD	EX IOT USER	EX IOT USER		EX IOT USER		IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO	IR UVO		
1P	MR PWR CLR ENB	MR CLR R	MR CLR B	MR CLR B	ST Ø DEL	FULSE TERM		PI OV	PI OV SET	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	PI OV CLR	
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1C	MC SW COND	MC NON EX MEM	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR	MC ADDR

↑ NOTE: R303'S MUST BE REV. D OR LATER

REVISIONS

REV.	DATE	BY	DESCRIPTION
1	ECU 20	A	
2	5-9-66	R. K.	REVISED IN PANELS
3	5-11-66	A. K.	
4	5-12-66	A. K.	
5	12-20-69	A. K.	
6	12-20-69	A. K.	
7	12-20-69	A. K.	
8	12-20-69	A. K.	

DEC FORM NO. DRD 105

UNLESS OTHERWISE SPECIFIED

DRAWN: R. K. DATE: 1-20-67

CHKD: P. L. DATE: 1-26-67

ENG: A. K. DATE: 1-27-67

PROJ. ENG: C. K. DATE: 1-27-67

PRD: S. K. DATE: 1-19-67

FIRST USED ON:

FINISH: SCALE: SHEET OF: DIST.:

digital

MODULE UTILIZATION

PDP-10

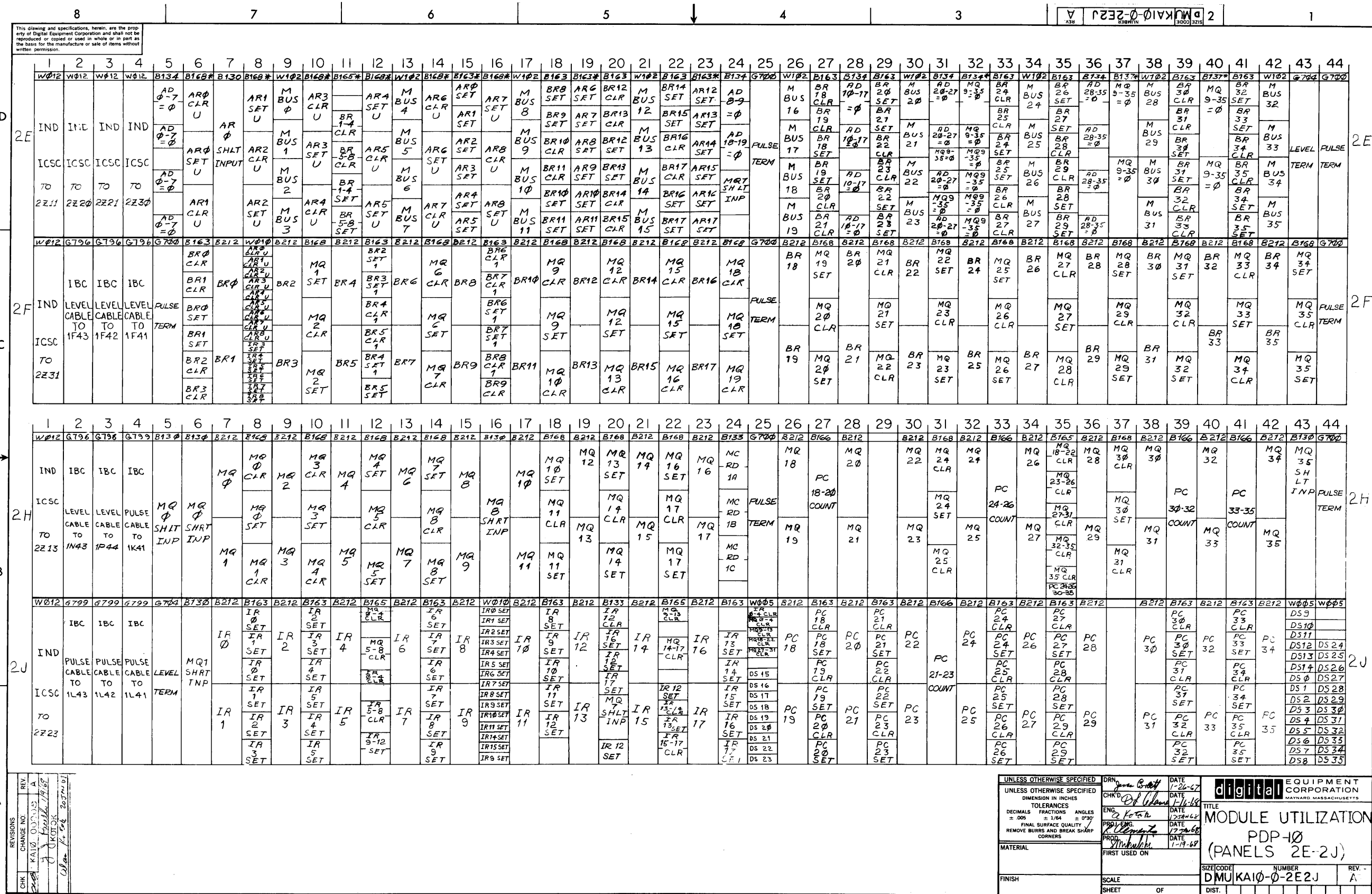
(PANELS 1P→1T)

DMUKAIØ-Ø-IPIT

REV. C

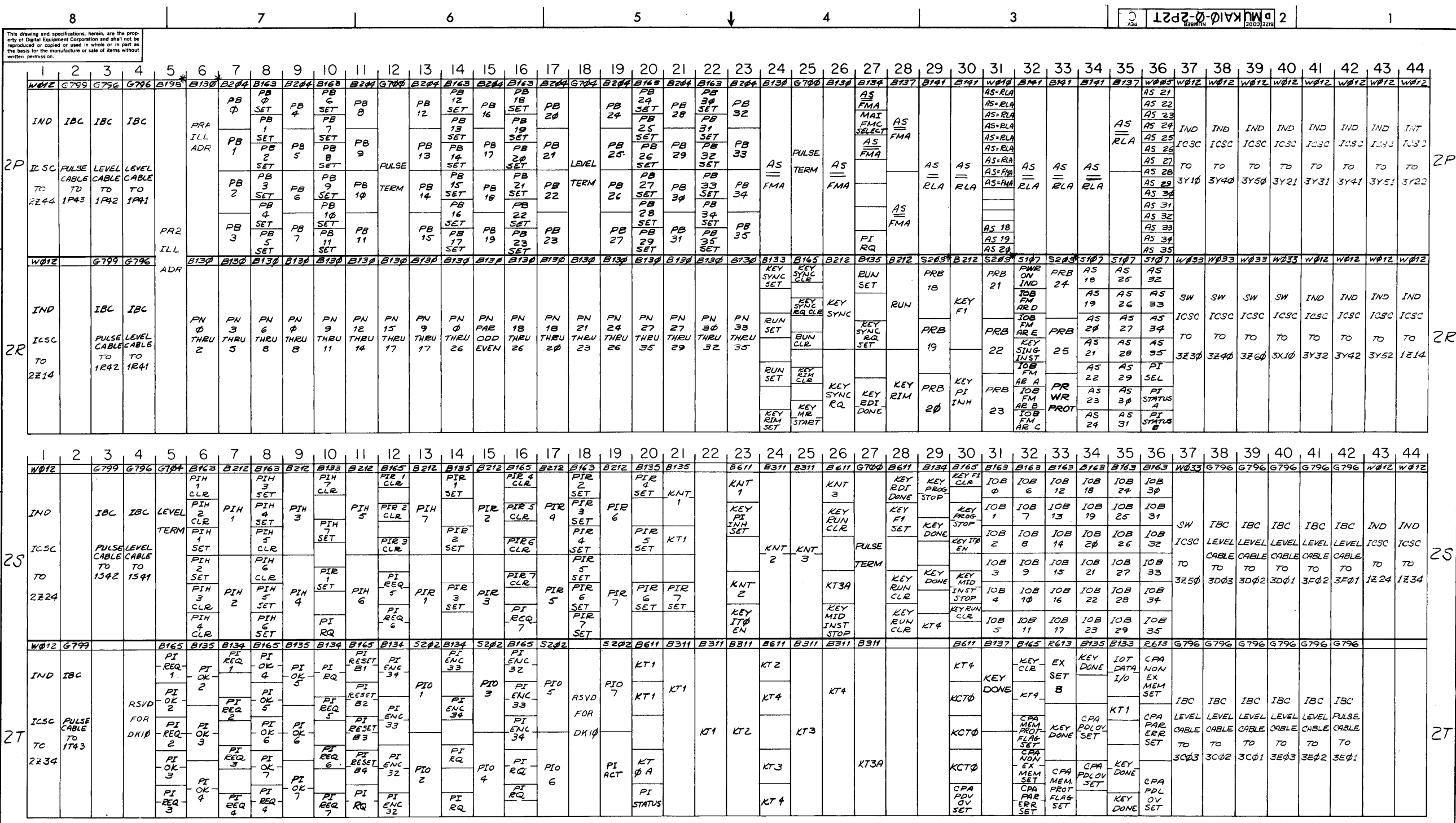












REVISIONS

REV.	CHANGE NO.	DATE
1	1-1	1-1-67
2	2	1-15-67
3	3	1-15-67
4	4	1-15-67
5	5	1-15-67
6	6	1-15-67
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41	41	1-15-67
42	42	1-15-67
43	43	1-15-67
44	44	1-15-67

NOTES:  
\* - MODULES ARE OPTIONAL

UNLESS OTHERWISE SPECIFIED	DRN	DATE	
UNLESS OTHERWISE SPECIFIED	CHK'D	DATE	
TOLERANCES	ENG.	DATE	
DECIMALS FRACTIONS ANGLES	PROJ. ENGR.	DATE	
± .005 ± .1/64 ± .010	PROD. MGR.	DATE	TITLE <b>MODULE UTILIZATION</b> <b>PDP-10</b> <b>(PANELS 2P-2T)</b>
FINAL SURFACE QUALITY	FIRST USED ON		
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL	FINISH	SCALE SHEET OF	SIZE/CODE NUMBER <b>DMUKA10-0-2P2T</b>
			REV C



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This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.																																																																																																																																																																																																																																																																																																																																																																																																						
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† NOTE: R303'S MUST BE REV. D OR LATER

REV. A	DATE	BY
1-1-68		
1-1-68		
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UNLESS OTHERWISE SPECIFIED		DRA. <i>A. Johnson</i>		DATE 1-1-68	
DIMENSION IN INCHES		CHKD. <i>P. Adams</i>		DATE 1-1-68	
TOLERANCES		ENG. <i>A. Johnson</i>		DATE 1-1-68	
DECIMALS FRACTIONS ANGLES		PROJ. ENG. <i>A. Johnson</i>		DATE 1-1-68	
± .005 ± 1/64 ± 0°30'		PROD. <i>A. Johnson</i>		DATE 1-1-68	
FINAL SURFACE QUALITY		FIRST USED ON		TITLE	
REMOVE BURRS AND BREAK SHARP CORNERS				MODULE UTILIZATION	
				PDP-10	
				PANELS 3E-3F	
MATERIAL		SCALE		SIZE CODE	
		SHEET OF		DMU KAI0-0-3E3F	
FINISH		DIST.		NUMBER	
				REV	

PARTS LIST			DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS	
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.	
		48	3 BIT PARITY CIRCUIT	B130 2	A-29	5-20-68	Rc	
		45	DIODE GATE	B133 2	00024	9/22/69	GK	
		60	DIODE GATE	B134 2				
		45	DIODE GATE	B135 2				
		40	DIODE GATE DIODE GATE	B136 B137 2				
		64	ADDER	B138 2				
		25	DIODE GATE	B141 2				
		4	BINARY TO OCTAL DECODER	B152				
		31	HALF BINARY TO OCTAL DECODER	B156 2				
		89	DIODE GATE	B163 2				
		85	DIODE INVERTER	B165 2				
		9	COUNTING GATE	B166				
		31	ADDER GATE	B167				
		113	DIODE GATE	B168 2				
		2	PROTECTION COMPARATOR	B198 2				
		1	FM ADDRESS DECODER	B199 2				
		20	FOUR FLIP FLOPS	B204				
MADE BY		DATE	TITLE	SIZE	CODE	NUMBER	REV.	
D.L.A. Adams		1/4/68	MODULE COUNT	A	PL	KAL0-0-MC	B	
CHECKED		DATE	FOR	ASSY. NO.				
P. Adams		1/17/68	KAL0	SHEET 1 OF 6				
ENG. Kotob		18 JAN 68						

DEC FORM NO.  
DRA 109

PARTS LIST			DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS	
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.	
		136	DUAL R-S FLIP FLOP	B212 2				
		12	FM MODULE	B250 2				
		91	TAPPED DELAY LINE	B311 2				
		5	VARIABLE DELAY LINE	B312 2				
		144	PULSE AMPLIFIER	B611 2				
		26	TWO BUS DRIVERS	B684				
		39	100-TERMINATOR	G700				
		15	2 MA LEVEL TERMINATOR	G704				
		1	CLOCK ACCELERATOR	G903				
		7	DIODE NETWORK	R001				
		10	DIODE CLUSTER	R002				
		9	2 MC FLIP FLOP	R201				
		16	3 BIT SHIFT REGISTER	R220				
		8	DELAY	R302				
		5	INTEGRATING ONE-SHOT	R303				
		2	CLOCK	R401				
MADE BY		DATE	TITLE	SIZE	CODE	NUMBER	REV.	
D.L.A. Adams		1/4/68	MODULE COUNT	A	PL	KAL0-0-MC	B	
CHECKED		DATE	FOR	ASSY. NO.				
P. Adams		1/19/68	KAL0	SHEET 2 OF 6				
ENG. Kotob		18 JAN 68						

DEC FORM NO.  
DRA 109

PARTS LIST		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS	
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		1	VARIABLE CLOCK	R450 1			
		1	PULSE AMPLIFIER	R601			
		7	PULSE AMPLIFIER	R602			
		14	PULSE AMPLIFIER	R613			
		22	INVERTER	S107			
		18	DIODE GATE	S111			
		19	DUAL FLIP FLOP	S202			
		22	TRIPLE FLIP FLOP	S203 2			
		3	DUAL FLIP FLOP	S205			
		4	CLAMP LOADS	W002			
		12	CLAMPED LOADS	W005			
		8	CLAMPED LOADS	W010			
		5	SOLENOID DRIVER	W040			
		10	PULSED BUS TRANSCIEVER	W102			
		3	SCHEMITT TRIGGER	W501			
		2	INITIAL TRANSIENT DETECTOR	W504			
MADE BY D.L.A. Adams		DATE 1/4/68	TITLE MODULE COUNT		SIZE A	CODE PL	REV. B
CHECKED D.L.A. Adams		DATE 1/18/68	FOR		NUMBER KAL0-0-MC		
ENG. C. Kotol		DATE 18 JAN 68	FOR		ASSY. NO.		SHEET 3 OF 6

DEC FORM NO.  
DRA 109

PARTS LIST		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS	
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		1	PULSE LEVEL CONVERTER	W510			
		1	COMPARATOR	W520			
		1	BIPOLAR LEVEL AMPLIFIER	W602			
		1	SPLIT LUG BOARD	W990			
NOTES:							
		1.	THE R450 IS USED WITH A MODEL 33 OR 35 TELETYPE A R451 IS USED WITH A MODEL 37 TELETYPE				
		2.	THE MODULE COUNT INDICATED FOR THESE MODULES INCLUDE THE MODULE COUNT FOR THE INTERNAL OPTIONS (KE10, KE10, KM10). THE FOLLOWING IS A BREAK DOWN OF THE MODULES IN THESE OPTIONS BUT THESE ARE NOT ADDITIONAL MODULES AS THEY ARE ALREADY INCLUDED IN THE ABOVE MODULE COUNT. KE10				
		2	3 BIT PARITY CIRCUIT	B130			
MADE BY D.L.A. Adams		DATE 1/4/68	TITLE MODULE COUNT		SIZE A	CODE PL	REV. B
CHECKED D.L.A. Adams		DATE 1/18/68	FOR		NUMBER KAL0-0-MC		
ENG. C. Kotol		DATE 18 JAN 68	FOR		ASSY. NO.		SHEET 4 OF 6

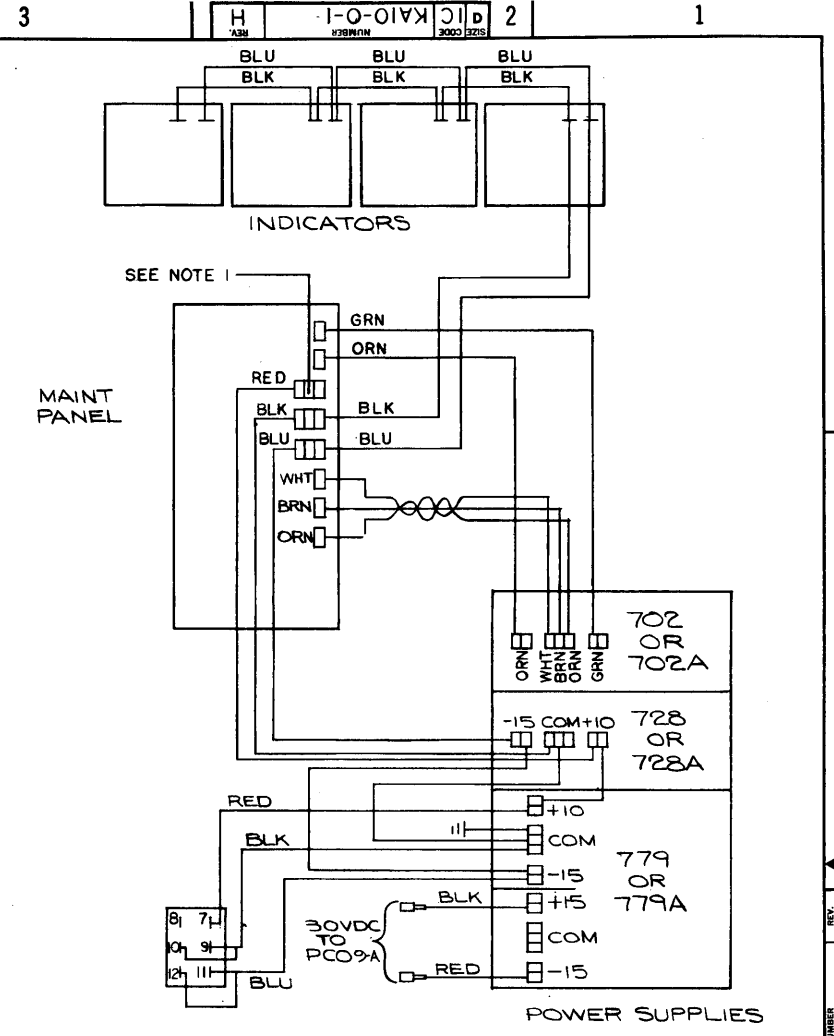
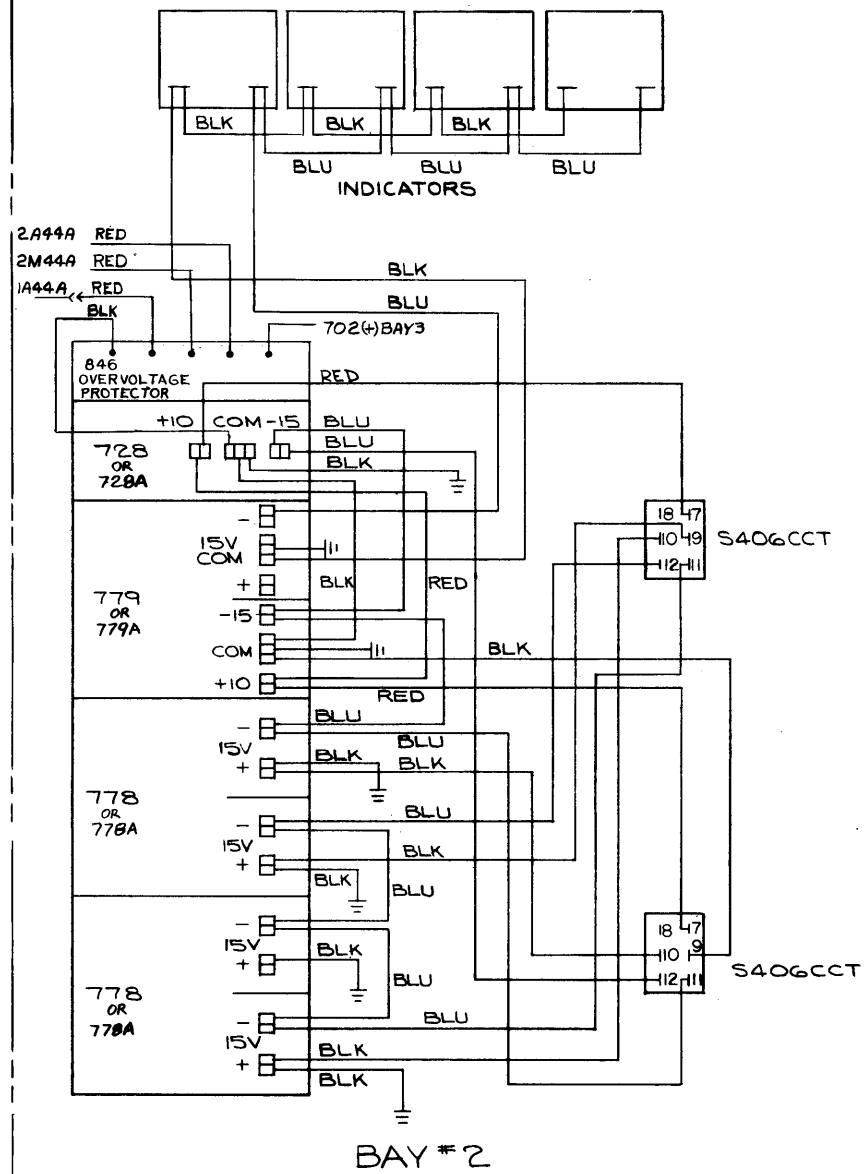
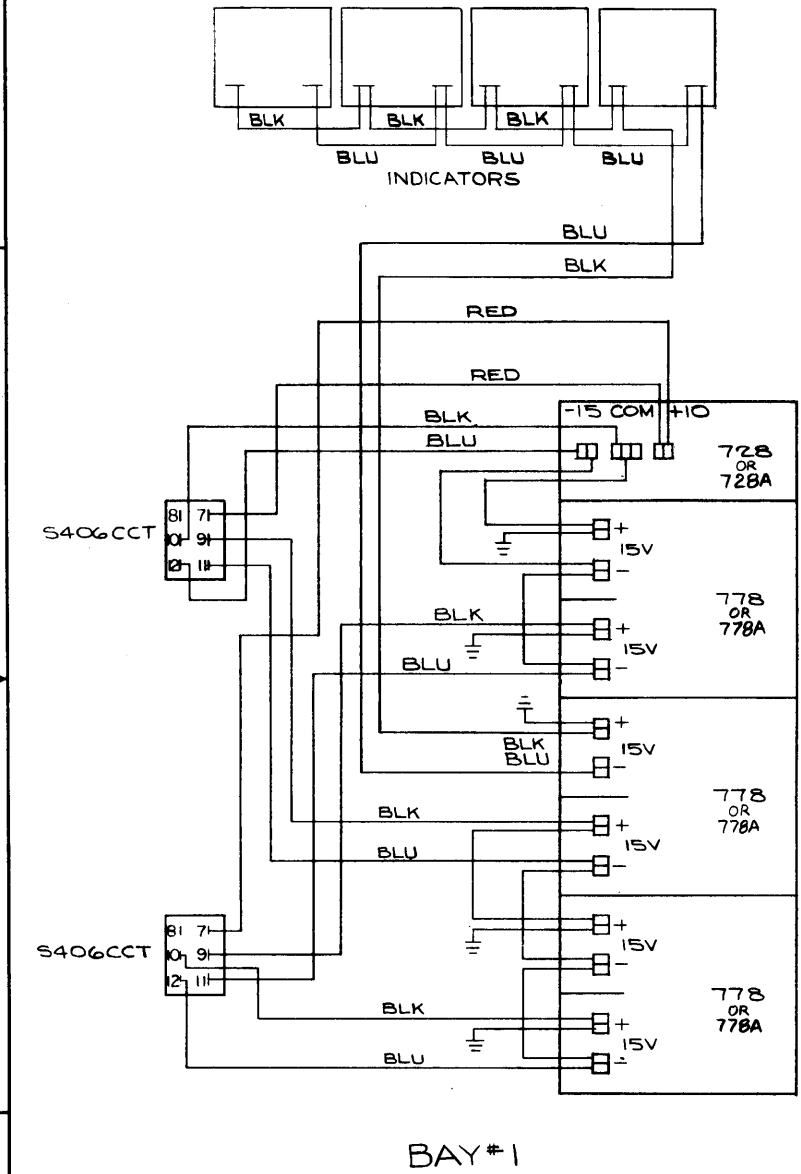
DEC FORM NO.  
DRA 109





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**NOTE:**  
ALL WIRE TO BE #14 AWG STRANDED UNLESS OTHERWISE SPECIFIED



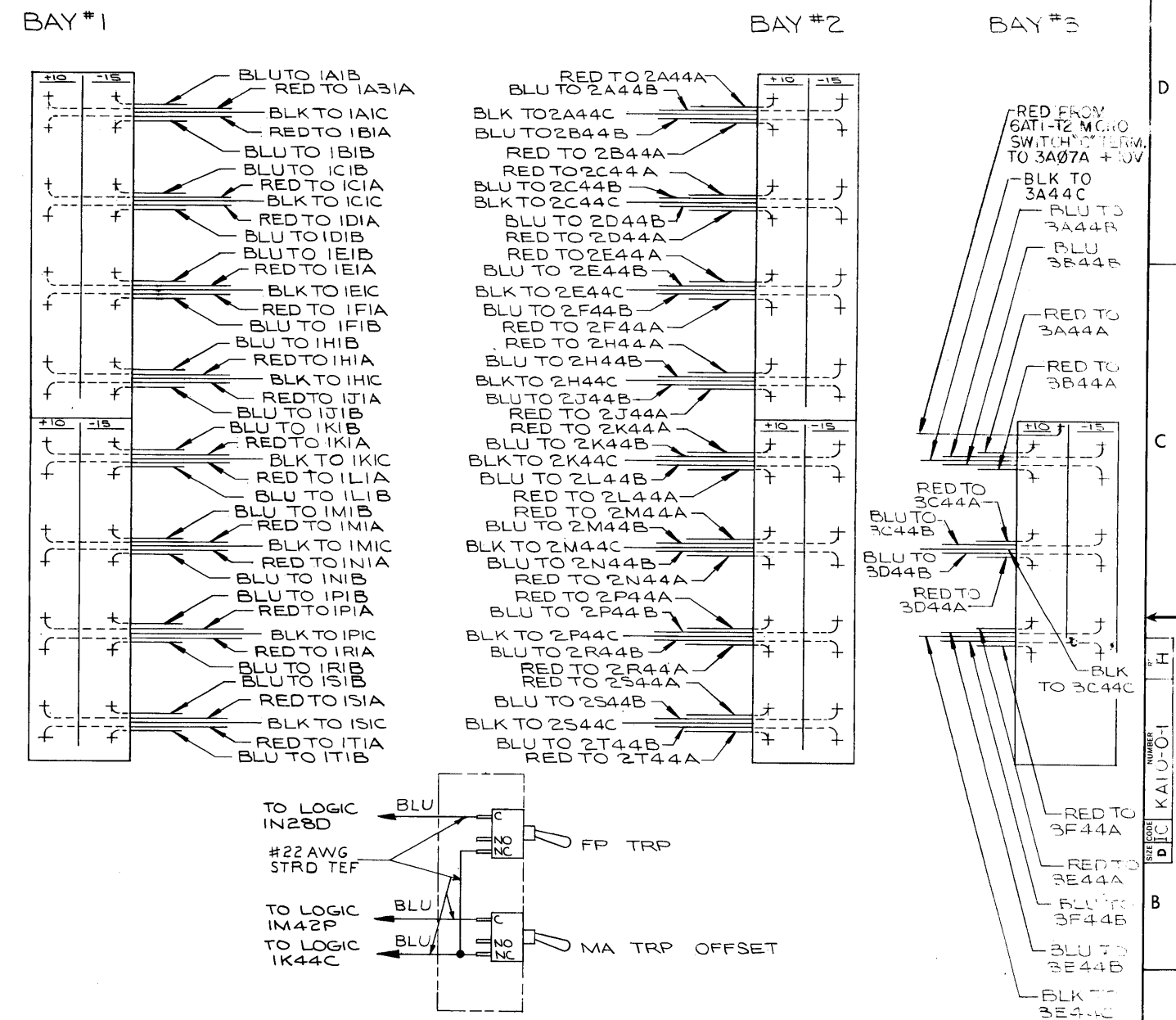
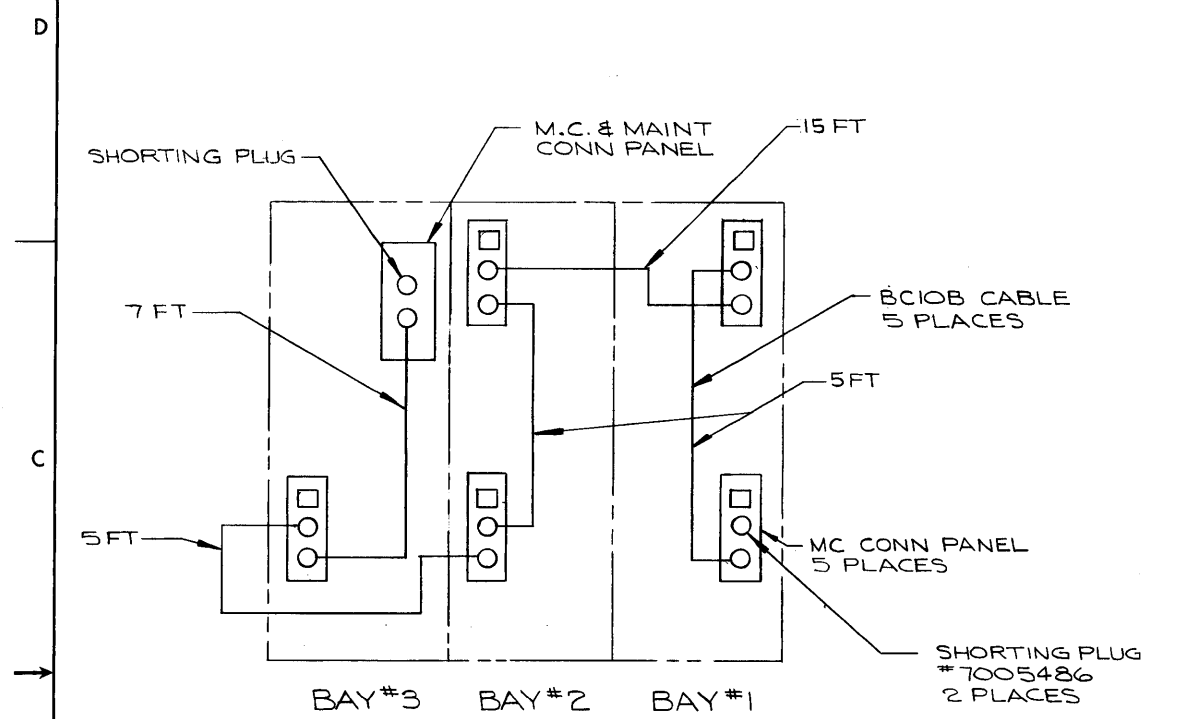
**NOTES:**  
1. +10 VOLTS FOR PC09 LAMP IS WIRED FROM HERE.

REV.	CHG.	DATE	BY
1	ECO #3131	11/15/67	M. Madden
2	ADDED SH SW TO & MAINT SW TO SH #2	11/15/67	M. Madden
3	ECO #330	12/2/67	M. Madden
4	ADDED MAR CHK SW WIRING ON SH #2 CHG LENGTH OF BC10B	12/2/67	M. Madden
5	ECO #3394	1/1/68	M. Madden
6	DEL MAR SW SWITCH & REVISED BAY #3 WIRING TO SUIT ON SH #2	1/1/68	M. Madden
7	ECO #29	1/2/68	M. Madden
8	ECO #29	1/2/68	M. Madden
9	ECO #29	1/2/68	M. Madden
10	ECO #29	1/2/68	M. Madden
11	ECO #29	1/2/68	M. Madden
12	ECO #29	1/2/68	M. Madden
13	ECO #29	1/2/68	M. Madden
14	ECO #29	1/2/68	M. Madden
15	ECO #29	1/2/68	M. Madden
16	ECO #29	1/2/68	M. Madden
17	ECO #29	1/2/68	M. Madden
18	ECO #29	1/2/68	M. Madden
19	ECO #29	1/2/68	M. Madden
20	ECO #29	1/2/68	M. Madden
21	ECO #29	1/2/68	M. Madden
22	ECO #29	1/2/68	M. Madden
23	ECO #29	1/2/68	M. Madden
24	ECO #29	1/2/68	M. Madden
25	ECO #29	1/2/68	M. Madden
26	ECO #29	1/2/68	M. Madden
27	ECO #29	1/2/68	M. Madden
28	ECO #29	1/2/68	M. Madden
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36	ECO #29	1/2/68	M. Madden
37	ECO #29	1/2/68	M. Madden
38	ECO #29	1/2/68	M. Madden
39	ECO #29	1/2/68	M. Madden
40	ECO #29	1/2/68	M. Madden
41	ECO #29	1/2/68	M. Madden
42	ECO #29	1/2/68	M. Madden
43	ECO #29	1/2/68	M. Madden
44	ECO #29	1/2/68	M. Madden
45	ECO #29	1/2/68	M. Madden
46	ECO #29	1/2/68	M. Madden
47	ECO #29	1/2/68	M. Madden
48	ECO #29	1/2/68	M. Madden
49	ECO #29	1/2/68	M. Madden
50	ECO #29	1/2/68	M. Madden

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE: <b>DC POWER WIRING</b>			
FIRST USED ON: <b>D-UA-KAIO-0-1</b>			
SCALE: <b>NONE</b>			
SHEET: <b>1</b> OF <b>4</b>			
DIST. <b>G</b>			



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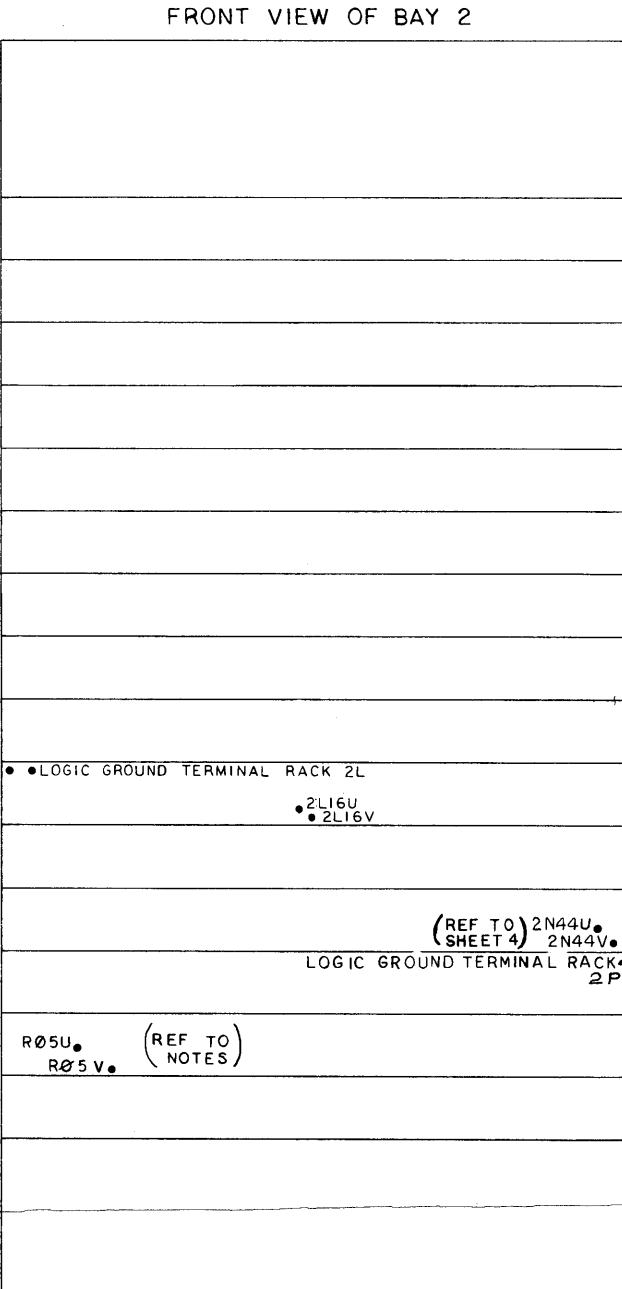
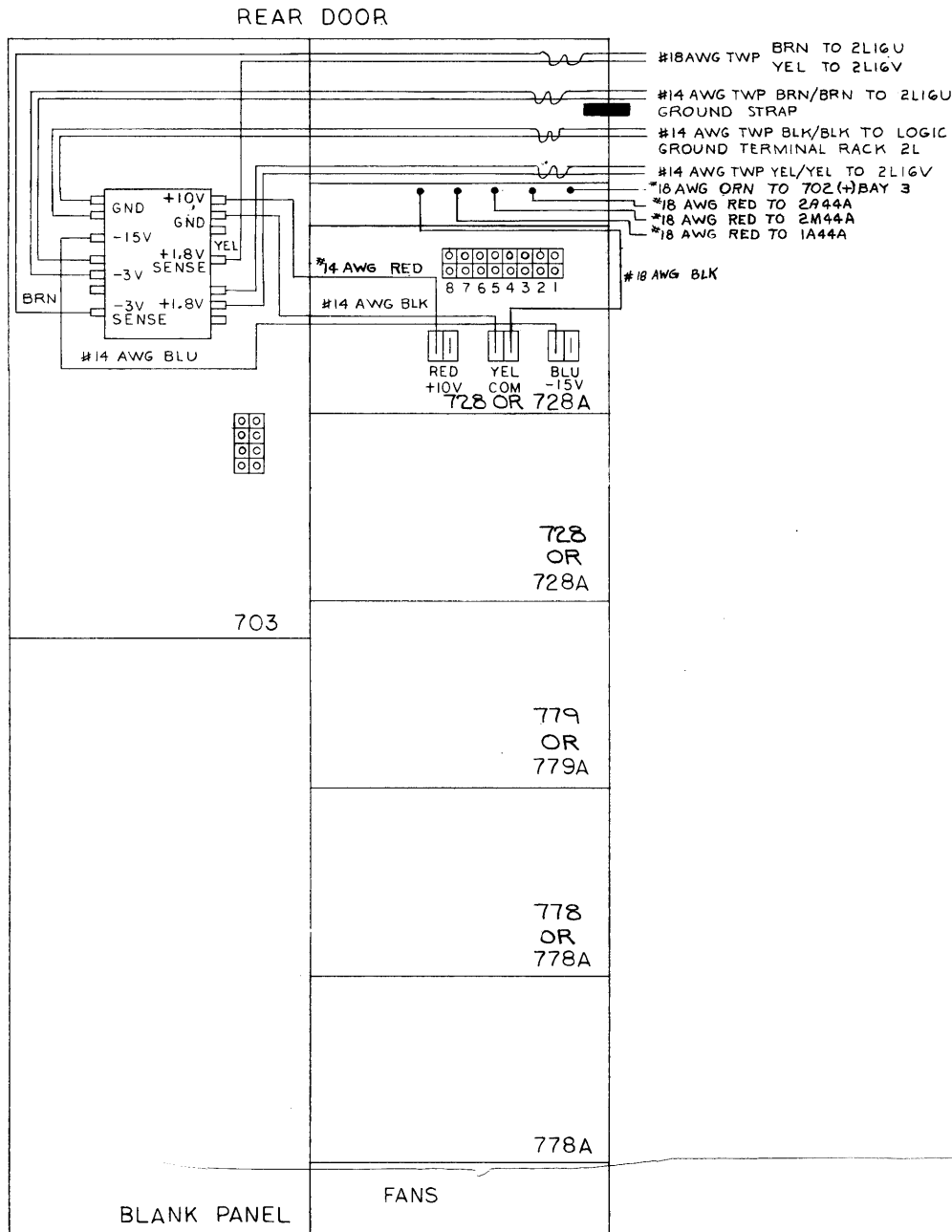


REV.	CHANGE NO.
CHK	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED	DRN <i>H. S. Conroy</i>	DATE <i>8/10/67</i>	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
UNLESS OTHERWISE SPECIFIED	CHK'D <i>H. S. Conroy</i>	DATE <i>7-11-67</i>	
TOLERANCES			TITLE <b>DC POWER WIRING</b>
DECIMALS	FRACTIONS	ANGLES	
= .005	= 1/64	= 0°30'	FIRST USED ON D-0A-KA10-0-0
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			SCALE NONE
FINISH			
SHEET 2 OF 4		SIZE CODE D I C	NUMBER KA10-0-1
		DIST. <i>6</i>	REV. H

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NOTES:  
 1. WIRE WITH #18 BRN 2N44U TO 2R05U  
 2. WIRE WITH #18 YEL 2N44V TO 2R05V



REV.	CHANGE NO.
CHK	

UNLESS OTHERWISE SPECIFIED		DRN	E.B	DATE	8/10/67
UNLESS OTHERWISE SPECIFIED		CHK'D	J. MADDEN	DATE	9/12/67
DIMENSION IN INCHES		ENG.	D. NEVALA	DATE	1/21/67
TOLERANCES		PROJ. ENG.	C. CLEMENTS	DATE	9/22/67
DECIMALS FRACTIONS ANGLES		PROD.	K. CAVOLET	DATE	9/29/67
± .005 ± 1/64 ± 0°30'		FIRST USED ON			
FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS		D-UA-KAIO-0-0			
MATERIAL	++	SCALE	NONE	SIZE CODE	NUMBER
FINISH	++	SHEET	3 OF 4	DIST.	

digital EQUIPMENT CORPORATION  
 MAINTARD, MASSACHUSETTS

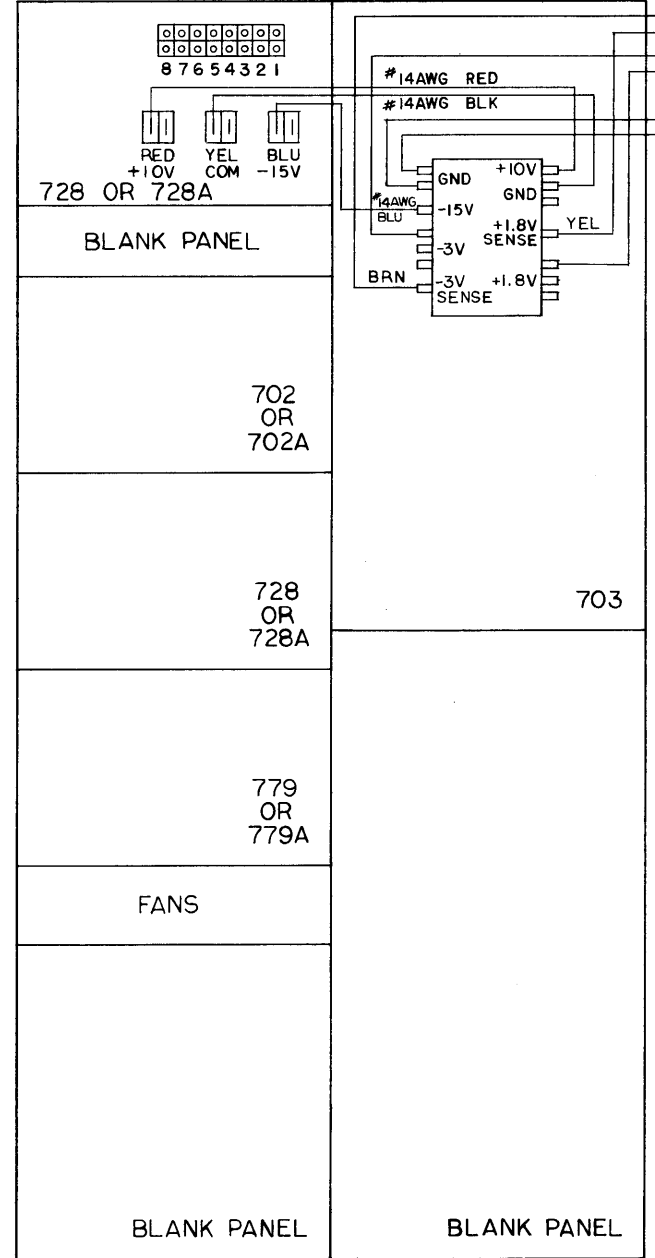
TITLE: DC POWER WIRING

SIZE CODE: D I C K A I O - 0 - 1  
 NUMBER: H  
 REV: H

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REV H  
1-0-01KX  
3000 3215  
2

#18AWG BRN TO 2N44U  
#18AWG YEL TO 2N44V  
#18AWG BRN TO 2N44U  
#18AWG YEL TO 2N44V  
#18AWG TWP BLK/BLK TO  
LOGIC GND TERMINAL RACK 2P



NOTE:  
REFER TO SHEET 3 FOR FRONT VIEW  
OF BAY 2

REAR DOOR BAY 3

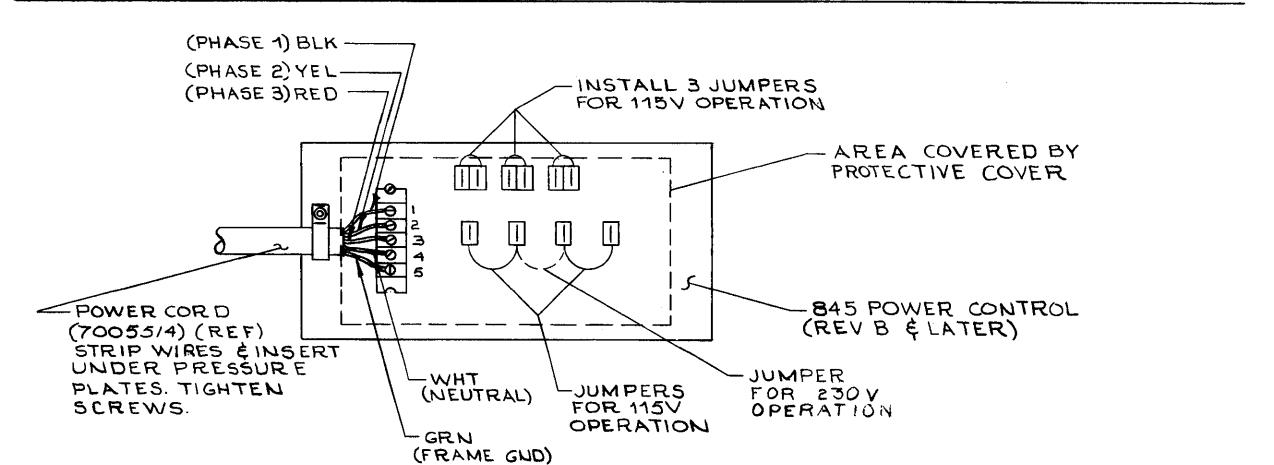
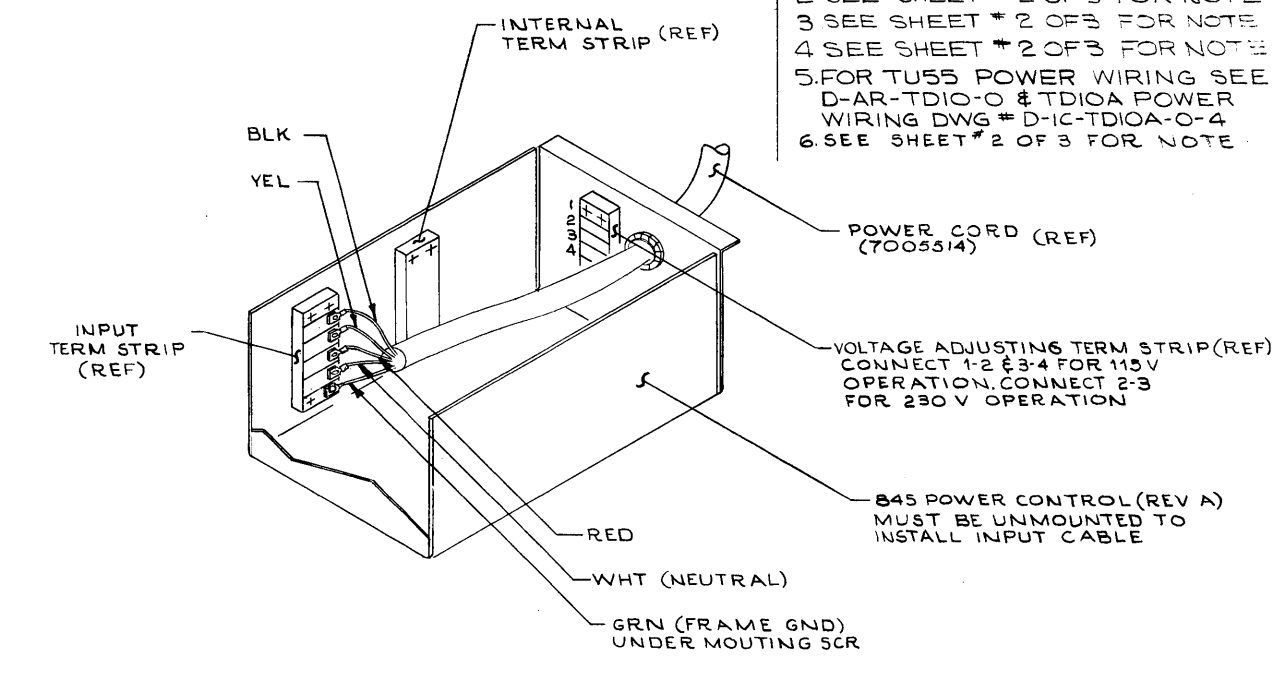
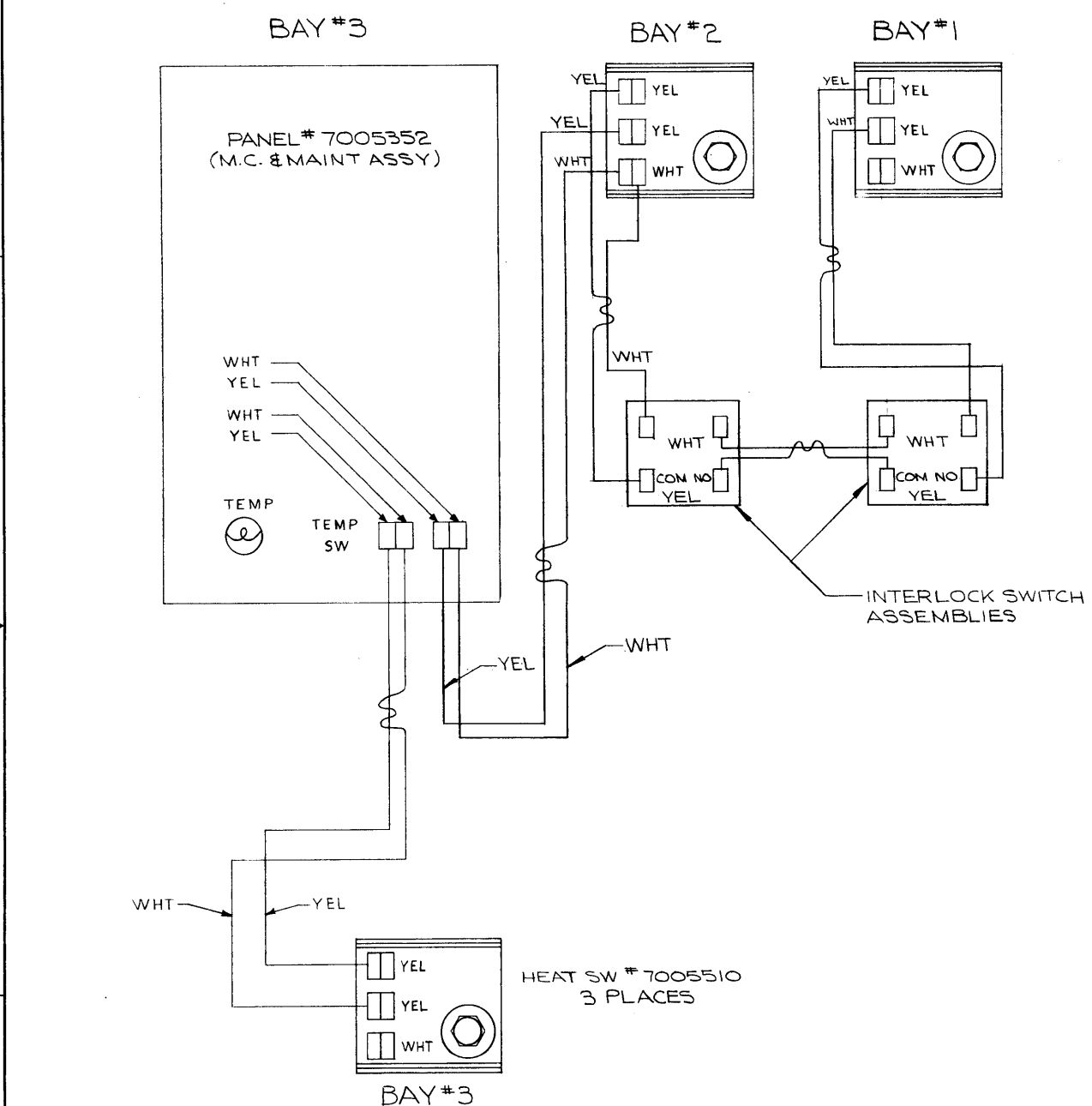
UNLESS OTHERWISE SPECIFIED		DRN	DATE	PARTS LIST	
UNLESS OTHERWISE SPECIFIED		<i>B. Buckleit</i>	5-22-68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
DIMENSION IN INCHES		CHK'D.	DATE	TITLE	
TOLERANCES		<i>R. Clout</i>	13 MAR 69	DC POWER WIRING	
DECIMALS FRACTIONS ANGLES		PRD. ENG.	DATE	SIZE CODE NUMBER REV.	
± .005 ± 1/64 ± 0°30'		<i>R. Clout</i>	13 MAR 69	D-UA-KA10-0-1 4	
FINAL SURFACE QUALITY		PRD.	DATE	DIST.	
REMOVE BURRS AND BREAK SHARP CORNERS		<i>R. Clout</i>	13 MAR 69	SHEET 4 OF 4	
MATERIAL		FIRST USED ON		D-UA-KA10-0-0	
++		SCALE		NONE	
FINISH		SHEET		4 OF 4	

REV.	
CHK.	
CHANGE NO.	
REVISIONS	

REV H  
1-0-01KX  
3000 3215  
2

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SIZE NUMBER  
D-IC-KA100-2

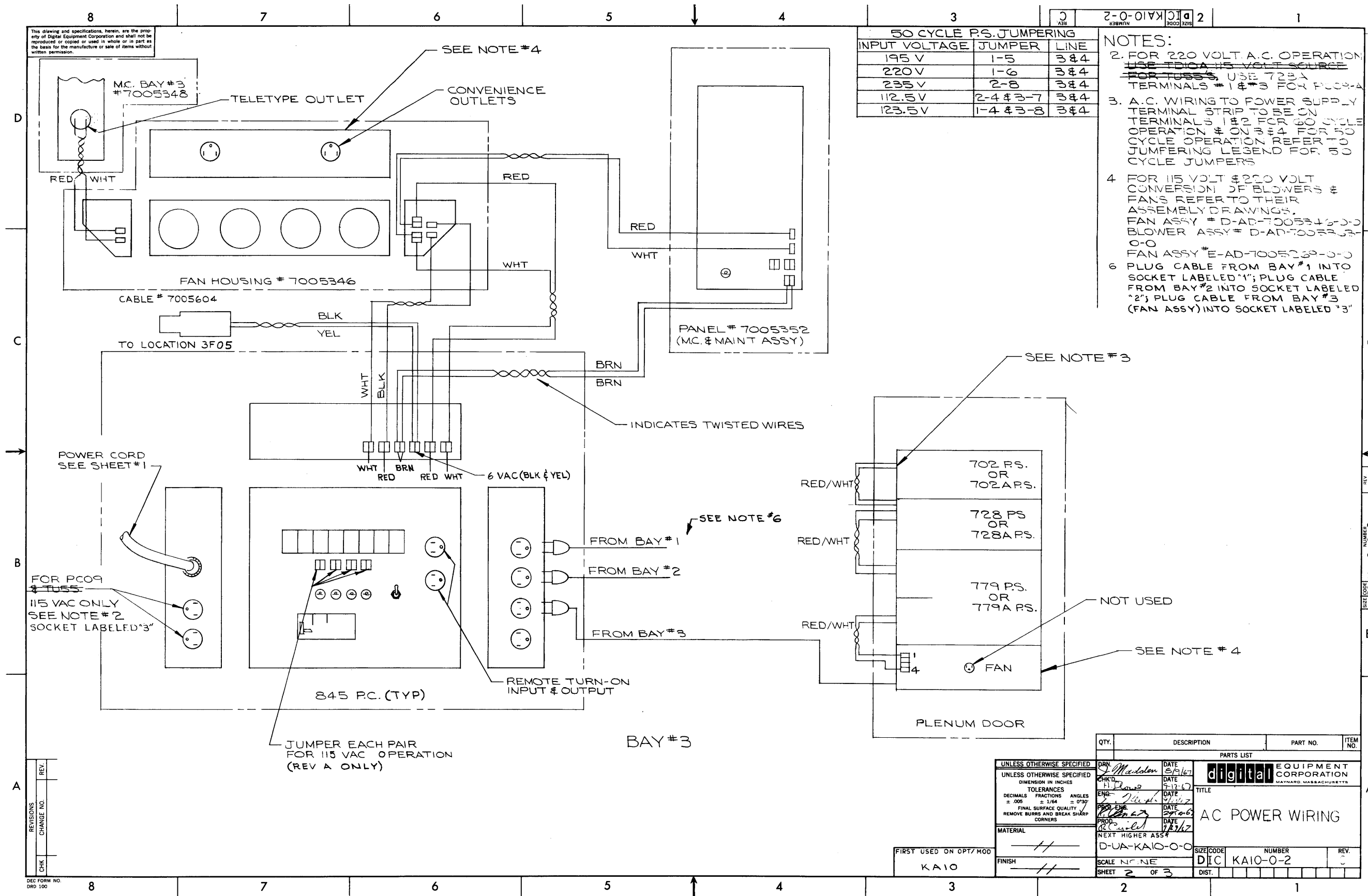


- NOTES
1. ALL WIRES TO BE #14AWG UNLESS OTHERWISE SPECIFIED
  2. SEE SHEET # 2 OF 3 FOR NOTE
  3. SEE SHEET # 2 OF 3 FOR NOTE
  4. SEE SHEET # 2 OF 3 FOR NOTE
  5. FOR TUBS POWER WIRING SEE D-AR-TDIO-0 & TDIOA POWER WIRING DWG # D-IC-TDIOA-0-4
  6. SEE SHEET # 2 OF 3 FOR NOTE

REV.	CHANGE NO.	DESCRIPTION
A	1	CHG TUBS WIRING NOTES & ADDED TUBS # 728P5 50 & 60 HZ
B	2	ECO # 29
C	3	ECO # 29
D	4	ECO # 29
E	5	ECO # 29
F	6	ECO # 29
G	7	ECO # 29
H	8	ECO # 29
I	9	ECO # 29
J	10	ECO # 29
K	11	ECO # 29
L	12	ECO # 29
M	13	ECO # 29
N	14	ECO # 29
O	15	ECO # 29
P	16	ECO # 29
Q	17	ECO # 29
R	18	ECO # 29
S	19	ECO # 29
T	20	ECO # 29
U	21	ECO # 29
V	22	ECO # 29
W	23	ECO # 29
X	24	ECO # 29
Y	25	ECO # 29
Z	26	ECO # 29

FIRST USED ON OPT/ MOD	QTY.	DESCRIPTION	PART NO.	ITEM NO.
KA10				
PARTS LIST				
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				
TITLE <b>AC POWER WIRING</b>				
NEXT HIGHER ASSY D-UA-KA10-0-0				
SCALE NONE				
SHEET 1 OF 3				
SIZE	CODE	NUMBER	REV.	
D	IC-KA100-2		C	

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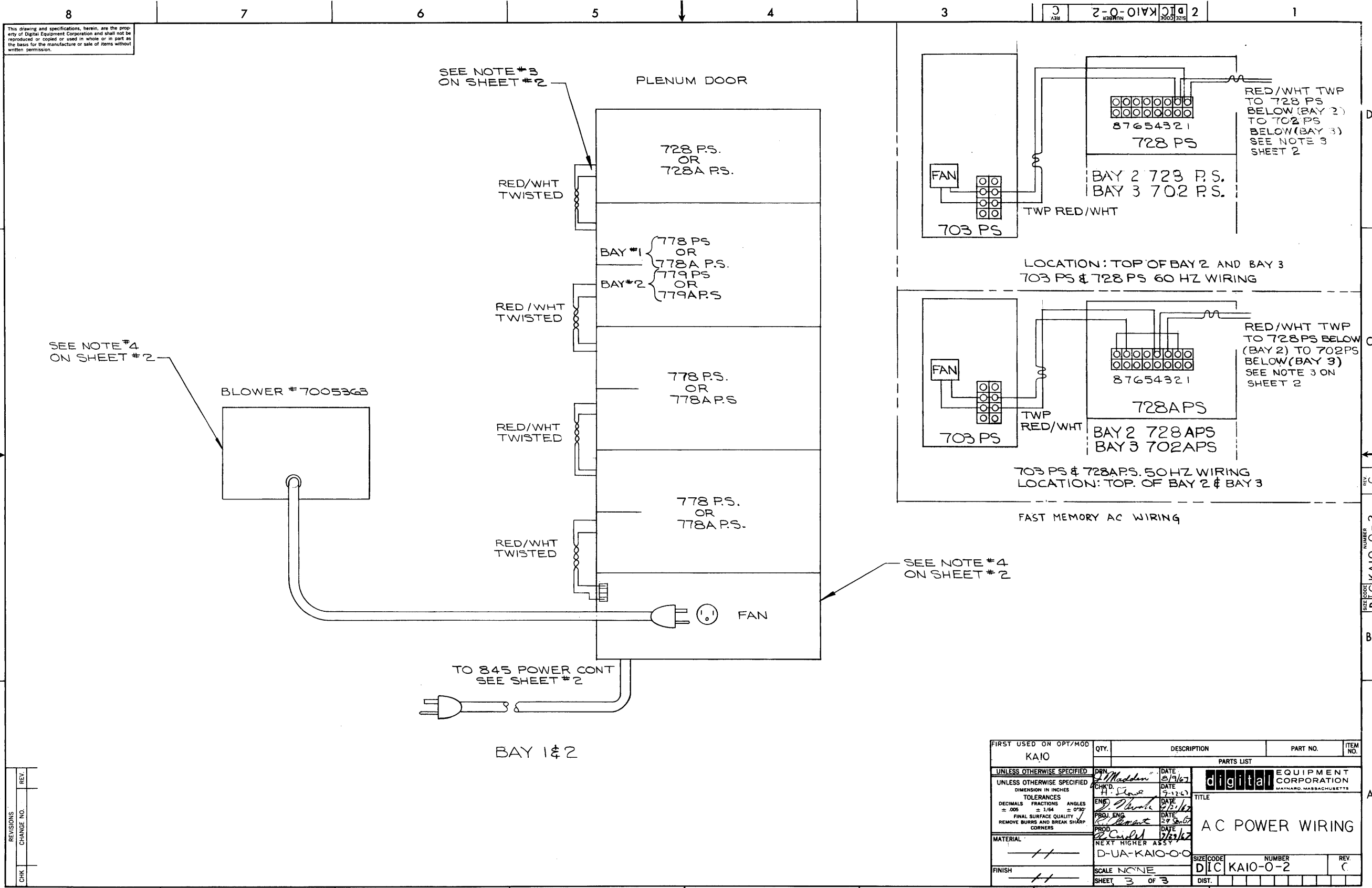
REV.	
CHANGE NO.	
CHK	

DEC FORM NO. DRG 100

UNLESS OTHERWISE SPECIFIED	DRN	DATE
DIMENSION IN INCHES	11/19/67	5/19/67
TOLERANCES	CHKD.	DATE
DECIMALS FRACTIONS ANGLES	11/19/67	5/17/67
= .005 = 1/64 = 0°30'	ENG.	DATE
FINAL SURFACE QUALITY	11/19/67	4/11/67
REMOVE BURRS AND BREAK SHARP CORNERS	PROJ. ENG.	DATE
	11/19/67	2/21/68
	PROJ. ENGR.	DATE
	11/19/67	12/16/67

FIRST USED ON OPT/MOD  
KA10


QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE AC POWER WIRING			
NEXT HIGHER ASSY D-UA-KA10-0-0		SIZE CODE D1C	NUMBER KA10-0-2
SCALE NONE		REV. C	
SHEET 2 OF 3		DIST.	



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COMPONENT NAME PART #	VALUE	POL.	FROM PIN	TO PIN	POL.
RES 74-4654	1500Ω 1/4W 5%		1A31R	1A31V	
			1A32R	1A32V	
			1A33R	1A33V	
			1A34R	1A34V	
			1A35R	1A35V	
			1A36R	1A36V	
			1A37R	1A37V	
			1A38R	1A38V	
			1A39R	1A39V	
			1A40R	1A40V	
			2A06R	2A06V	
			2A07R	2A07V	
			2A08R	2A08V	
			2A09R	2A09V	
			2A10R	2A10V	
			2A11R	2A11V	
			2A12R	2A12V	
			2A13R	2A13V	
			2A14R	2A14V	
			2A15R	2A15V	
			2A16R	2A16V	
			2A17R	2A17V	
			2A18R	2A18V	
			2A19R	2A19V	
			2A20R	2A20V	
RES 74-4654	1500Ω 1/4W 5%		2A21R	2A21V	


DEC FORM NO. DRA 106

REVISIONS				DRN. W. STEPHENS	DATE 4/4/67	 MAYNARD, MASSACHUSETTS
REV.	DATE	CHG. NO.	APP'D.	CHK'D.	DATE	
A	5-20-68	ECO#29	Rcc	<i>R. Adams</i>	1/17/68	TITLE <b>EXTERNAL COMPONENT LIST</b> FOR KA10 B138 EXTERNAL COMPONENTS
B	5-28-68	32	Rcc	<i>A. Kotok</i>	18 JAN 68	
C	8-14-68	00003	Rcc	<i>R. Adams</i>	19 JAN 68	
D	1/13/68	00010	AK	<i>S. M. ...</i>	1-22-68	
E	7/14/69	00034	AK			
F	7/30/69	KA10-00040	ARV			
				FIRST USED ON	KA10	SIZE CODE
				SCALE	A CP	NUMBER
				SHEET	1 OF 6	DIST.

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COMPONENT NAME PART #	VALUE	POL.	FROM PIN	TO PIN	POL.
RES 74-4654	1500Ω 1/4W 5%		2A22R	2A22V	
			2A23R	2A23V	
			2A24R	2A24V	
			2A26R	2A26V	
			2A27R	2A27V	
			2A28R	2A28V	
			2A29R	2A29V	
			2A30R	2A30V	
			2A31R	2A31V	
			2A32R	2A32V	
			2A33R	2A33V	
			2A34R	2A34V	
			2A35R	2A35V	
			2A36R	2A36V	
			2A37R	2A37V	
			2A38R	2A38V	
			2A39R	2A39V	
			2A40R	2A40V	
			2A41R	2A41V	
			2A42R	2A42V	
			2A43R	2A43V	
			2M36R	2M36V	
			2M37R	2M37V	
			2M38R	2M38V	
			2M39R	2M39V	
RES 74-4654	1500Ω 1/4W 5%		2M40R	2M40V	

DEC FORM NO. DRA 106

REVISIONS				DRN. W. STEPHENS	DATE 4/4/67	 MAYNARD, MASSACHUSETTS
REV.	DATE	CHG. NO.	APP'D.	CHK'D.	DATE	
				<i>R. Adams</i>	1/17/68	TITLE <b>EXTERNAL COMPONENT LIST</b> FOR KA10 B138 EXTERNAL COMPONENTS
				<i>A. Kotok</i>	18 JAN 68	
				<i>R. Adams</i>	19 JAN 68	
				<i>S. M. ...</i>	1-22-68	
				FIRST USED ON	KA10	SIZE CODE
				SCALE	A CP	NUMBER
				SHEET	2 OF 6	DIST.

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COMPONENT NAME PART#	VALUE	POL.	FROM PIN	TO PIN	POL.
CAP.	3.9 uf @ 10V	-	3B16H	3B16J	+
Cap.	0.027uf@ 100V	-	3D10 H	3D10J	+
Cap.	0.027uf @ 100V	-	3D10R	3D10S	+
Cap. 74-5962	2.2uf @ 20V	-	1P02H	1P02J	+
Cap.	330 uf @ 15V	-	1P01J	1P01C	+
Cap.	180 uf @ 6V	-	3A25R	3A25S	+
Cap.	330 uf @ 15V	-	3A26J	3A26C	+
Cap. 74-5962	2.2 uf @ 20V	-	3A25H	3A25J	+

REVISIONS				DRN.	DATE	 <b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	<b>EXTERNAL COMPONENT LIST</b> FOR KA10 R30X Delays
REV.	DATE	CHG. NO.	APP'D.	CHK'D.	DATE		

DEC FORM NO. DRA 106

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COMPONENT NAME PART#	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.- 74-4654	1500Ω 1/4W5%		2M41R	2M41V	
			2M42R	2M42V	
RES 74-4654	1500Ω 1/4W5%		2M43R	2M43V	
RES	180Ω 1/4W5%		2A44L	2A44C	
RES	180Ω 1/4W5%		2M35L	2M35N	
RES	180Ω 1/4W5%		2M43L	2M43N	
RES	180Ω 1/4W5%		1A40L	1A40C	

REVISIONS				DRN.	DATE	 <b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	<b>EXTERNAL COMPONENT LIST</b> FOR KA10 B138 EXTERNAL COMPONENTS
REV.	DATE	CHG. NO.	APP'D.	CHK'D.	DATE		

DEC FORM NO. DRA 106



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COMPONENT NAME PARTS#	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.-74-4644	100Ω 1/4W5%		1K21F	1K18C	
Res -74-4644	100Ω 1/4W5%		1R27T	1R27C	
Res -74-4644	100Ω 1/4W5%		2J20T	2K21C	
Diode-74-4914	D664		2D06L	2D06C	
Diode 74 4914	D664		2H16M	2H16C	
Diode-74-4914	D664		2J20E	2J21C	
Res-74-4644	100Ω 1/4W5%		2H41M	2H41C	
Res-74-4644	100Ω 1/4W5%		2D14L	2D14C	
Res-74-4644	100Ω 1/4W5%		2D33L	2D33C	
Cap-74-4657	.01ufd		3A06F	3A06C	
Cap	.01ufd		3A06T	3A07C	
Cap	.01ufd		3D40D	3D38C	
Cap	.01ufd		3D40E	3D39C	
Cap	.01ufd		3D40F	3D40C	
Cap-74-4657	.01ufd		3D40H	3D41C	
Res-74-4644	100Ω 1/4W5%		1K21T	1K21C	
Res	100Ω 1/4W5%		1C14J	1C14C	
Res	100Ω 1/4W5%		1B27U	1C27C	
Res	100Ω 1/4W5%		1S34T	1T34C	
Res	100Ω 1/4W5%		1R37L	1S37C	
Res	100Ω 1/4W5%		1R36J	1R36C	
Res 74 4644	100Ω 1/4W5%		1L22L	1L22C	
Res-Cap 74-05913	100Ω .01μF		1R29F	1R29C	

REVISIONS				DRN. D.L. Adams	DATE 1/27/67	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE EXTERNAL COMPONENT LIST FOR KA10 General EXTERNAL COMPONENTS	SIZE CODE A CP	NUMBER KA10-0-CP	REV. F
REV.	DATE	CHG. NO.	APP'D.	CHK'D. Adams	DATE 1/17/68					
				ENG. Kato	DATE 18 Jan 68					
				PROD. ENG. Adams	DATE 18 Jan 68					
				PROD. Minkwitz	DATE 1-26-68					
				FIRST USED ON		KA10				
				SCALE		A CP				
				SHEET 5 OF 6		DIST.				

DEC FORM NO. DRA 106

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COMPONENT NAME PART#	VALUE	POL.	FROM PIN	TO PIN	POL.
RES 74-4644	100Ω 1/4W5%		2J12T	2J12C	
	100Ω 1/4W5%		2J22T	2K22C	
	100Ω 1/4W5%		2E13V	2F13C	
	100Ω 1/4W5%		2E26V	2F25C	
	100Ω 1/4W5%		2E38V	2F39C	
	100Ω 1/4W5%		1J22R	1J23M	
	100Ω 1/4W5%		3F03E	3F03C	
RES 74-4644	100Ω 1/4W5%		3F03H	3F03F	
CAP 74-4657	.01MF		3A06U	3B06C	

REVISIONS				DRN. D.L. Adams	DATE 1/27/67	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE EXTERNAL COMPONENT LIST FOR KA10 General EXTERNAL COMPONENTS	SIZE CODE A CP	NUMBER KA10-0-CP	REV. F
REV.	DATE	CHG. NO.	APP'D.	CHK'D. Adams	DATE 1/17/68					
				ENG. Kato	DATE 18 Jan 68					
				PROD. ENG. Adams	DATE 18 Jan 68					
				PROD. Minkwitz	DATE 1-26-68					
				FIRST USED ON		KA10				
				SCALE		A CP				
				SHEET 6 OF 6		DIST.				

DEC FORM NO. DRA 106

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SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MR START R	3F30H	3F03V	WHT	} TWP
	3F30J	3F03U	BLK	

REVISIONS				DRN. T. QUILLIN	DATE 7/23/69	 <b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE <b>GENERAL WIRING SHEET</b> FOR TWP LIST KA10 BAY3
REV.	DATE	CHG. NO.	APP'D.	CHK'D. <i>W. Sutherland</i>	DATE 7/24/69		
ORIG	7/25/69	00035	----	ENG. <i>A Kotol</i>	DATE 7/25/69	SIZE CODE NUMBER REV. A WL KA10-0-TWP3	
				PROJ. ENG. <i>DM-M</i>	DATE 7/25/69		
				PROD. <i>W.M. - 141</i>	DATE 7/25/69	SCALE SHEET 1 OF 1	
				FIRST USED ON			

DEC FORM NO. DRA 104

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SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
TTY SOCKET B	3D40F	B of	WECO 548A	SOCKET
TTY SOCKET G	3D40D	G of	" "	"
TTY SOCKET R	3D40E	R of	" "	"
TTY SOCKET Y	3D40H	Y of	" "	"

REVISIONS				DRN. D.L.A. day	DATE 7/1/68	 <b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE <b>GENERAL WIRING SHEET</b> FOR TTY SOCKET WIRING OF KA10
REV.	DATE	CHG. NO.	APP'D.	CHK'D. <i>Phil Adams</i>	DATE 7/1/68		
A	2-26-69	KA10-00019	KLB	ENG. <i>A Kotol</i>	DATE 1/8 JAN 68	SIZE CODE NUMBER REV. A WL KA10-0-GW A	
				PROJ. ENG. <i>R. Cloutier</i>	DATE 1/8 JAN 68		
				PROD. <i>W. Sutherland</i>	DATE 1-19-68	SCALE SHEET 1 OF 1	
				FIRST USED ON			

DEC FORM NO. DRA 104

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CABLE PINS

FROM	TO	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V
1441	2002	ARRT FM AD (0)	ARRT FM MQ (0)	GND	ARRT FM AD (1)	GND	ARRT FM MQ (1)	GND	ARLT FM FM (1)	GND	AR0-5 FM SCAD 3-B(J)	GND	AR1-8 FM AR0(J)	AR1-8 FM SCAD 1-B(J)	GND	ARRT FM PC (J) B
1442	2003	ARLT FM IOB (1)	ARRT FM IOB (1)	GND	ARLT FM AD (0)	GND	ARLT FM MQ (0)	GND	ARLT FM AD (2)	GND	ARLT FM MQ (1)	GND	ARLT FM AR0(J)	ARRT FM PC (J) A	GND	ARLT FM FLAGS(J) B
1443	2002	ARRT SH RT A	ARRT SH RT B	GND	ARRT SH LT A	GND	ARRT SH LT B	GND	ARRT CLR	GND	ARRT FM FM (1)	GND	ARLT FM IR (1)	ARLT FM DS (1)	GND	ARRT FM DS (1)
1444	2803	ARLT CLR	ARLT FM ARRT(J) B	GND	ARLT SH LT B	GND	ARLT SH RT B	GND	ARLT FM ARRT(J) A	GND	ARLT SH LT A	GND	ARLT SH RT A	ARRT FM ARRT(J) A	GND	ARRT FM ARRT(J) B
1K41	2H04	MC MEM BUS FM AR(1) A	MC MEM BUS FM AR(1) B	GND	MC MEM BUS FM AR(1) C	GND	BR 1-8 CLR	GND	BR 1-8 CLR	GND	BRLT FM AR(0)	GND	BRLT FM AR(1)	BRRT FM AR(0)	GND	ARLT(J) B
1L41	2J04	MQ CLR	MQ SH LT A	GND	MQ SH LT B	GND	MQ SH RT A	GND	MQ SH RT B	GND	MQ FM AD(J) A	GND	MQ FM AD(J) B	MQ SH LT C	GND	MQ SH RT C
1L42	2J03	MQ SH LT D	MQ SH RT D	GND	MQ FM AD(J) C	GND	MQ FM AD(J) D	GND	FMT 3	GND	IR LT CLR	GND	IR RT CLR	IR RDI SETUP	GND	-
1L43	2J02	ET0F	ST 1	GND	PCLT FM MA (J)	GND	PCRT FM MA (J)	GND	PCLT +1	GND	PCRT +1	GND	MA FM PICH (1)	-	GND	-
1M43	2M02	MA CLR	MA FM PC(J) A	GND	MA FM PC(J) B	GND	MA FM AR(J) A	GND	MA FM AR(J) B	GND	MA FM AS(J) A	GND	MA FM AS(J) B	IT0	GND	MAI IGN PAR PULSE KT1
1N42	2N03	KNT 2	KEY RDI DONE	GND	ME PWR CLR	GND	MI LOAD A	GND	MI LOAD B	GND	MI LOAD C	GND	MI LOAD D	KT 2	GND	MI UO IND
1P43	2P02	FT 9	MAI CMC RD RS	GND	EX CLR	GND	EX SET	GND	PB CLR	GND	PI RESET B	GND	KNT 1	KNT 3	GND	*IR UO IND
1S42	2S03	MR START	ST 9	GND	PI OK CLRS PIH KT0A	GND	PIH FM PICH EQ	GND	PIR FM IOB (1)	GND	PIR STB	GND	PI RESET	PIO CLR	GND	PIO SET
1T43	2T02	KT 4	MR CLR	GND	PIH KT0A	GND	MC NON EX MEM	GND	MC ILLEG ADR	GND	MC PAR ERR	GND	MCRST 1	KT 3	GND	-
3E01	2T42	KEY DONE	KT0	GND	KST 1	GND	KST 2	GND	PI CONVO SET	GND	CPA MEM PROT FLAG SET	GND	CPA NON EX MEM SET	CPA PAR ERR SET	GND	CPA PDL OV SET
1A41	2A03	AD CRY 36(1)	AR 1(0)	AR 1(1)	AR 2(1)	AR 3(1)	AR 4(1)	AR 5(1)	AR 6(1)	AR 7(1)	AR 8(1)	AR 9(1)	AR 10(1)	AR 11(1)	AR 0 SET	GND
1B41	2B04	SCAD 1(0)	AD BR+EN(0)	AD BR-EN(0)	SCAD 2(1)	SCAD 3(0)	SCAD 3(1)	SCAD 4(0)	SCAD 4(1)	SCAD 5(0)	SCAD 5(1)	SCAD 6(0)	SCAD 6(1)	SCAD 7(0)	SCAD 7(1)	GND
1C41	2C04	AD AR+EN CLR	AD AR+EN SET	AD AR-EN CLR	AD AR-EN SET	AD BR+EN CLR	AD BR+EN SET	AD BR-EN CLR	AD BR-EN SET	AD -1 LH(0)	AD +1 LH(1)	AD CRY INS(0)	AD 20-27(0)	AD 28-35(0)	AD 0(0)	GND
1D41	2D04	MQ 5(0)	MQ 35(0)	MQ 35(1)	MQ 34(0)	MQ 34(1)	ARMQ PRESERVE SIGN	ARMQ PRESERVE SIGN	ARMQ MULV ASHXVFP	ARMQ AR35 FM MQ 0 EN	ARMQ FP SH EN	AD AR+EN(1)	AD AR-EN(1)	AD BR+EN(1)	AD BR-EN(1)	GND
1F41	2F04	BR 35(1)	EX USER(0)	EX USER(1)	EX IOT USER(0)	EX IOT USER(1)	ARI DFN CLR	ARI DFN SET	AR 8(0)	AR 9(0)	IR ROT	IR ROTC	ARMQ FDN NORM	IR ASHC	IR ASHC	GND
1G41	2G03	AR FXU(0)	AR FXU(1)	AR DCK(0)	AR DCK(1)	AR OV FLAG(0)	AR OV FLAG(1)	AR FOV(0)	AR 28(1)	AR 29(1)	BR 30(1)	BR 31(1)	BR 32(1)	BR 33(1)	BR 34(1)	GND
1H41	2H02	ARMQ LEC VMUL	ARMQ FP SH EN	ARMQ ASHC VMUL LAST	ARMQ BYTE MASK	DSF 1(1)	IR 7(0)	IR 7(1)	BR 3(1)	BR 4(0)	BR 4(1)	IR 9(0)	IR 9(1)	IR 10(0)	IR 10(1)	GND
1I41	2I03	IR 0(1)	IR 0(0)	IR 1(0)	IR 1(1)	IR 2(0)	IR 2(1)	IR 3(0)	BR 28(1)	BR 29(1)	BR 30(1)	BR 31(1)	IR 5(0)	IR 5(1)	IR 6(0)	GND
1J41	2M04	SC STOP SW	SC STOP(0)	FMA AC EN	FMA AC EN	FMA MA EN	FMA XR EN	FMA FM AR(J)	IR 16(0)	IR 17(0)	IR 17(1)	IR 18(0)	IR 18(1)	IR 19(0)	IR 19(1)	GND
1K41	2N04	KEY PROG STOP	KEY PI INH(0)	E XCT F(0)	EX REL A	EX REL A	EX REL B	EX REL B	AD 17(1)	AD 17(0)	MAI FMA SEL(1)	MAI FMA SEL(0)	EX NON REL UO	JFFO SWAP	MC REQ CYC	GND
1L41	2P03	PRAILLADR	PRAILLADR	KEY START(1)	IR PUSH	IR PUSHJ	IR POPS	IR JRST	MAI 18-31(0)	MAI 18-31(0)	MAI FMA SEL(1)	PB PAR(0)	MC REQ CYC	MC RD(1)	MC WR(1)	GND
1M41	2R04	KEY RIM(0)	MI PROG DIS SW	AS=RLA	AS=FMA	KEY F1(1)	RUN(1)	RUN(0)	PI RQ	PI RQ	PI OV(1)	PB PAR(0)	MC REQ CYC	MC RD(1)	MC WR(1)	GND
1N41	2S04	MC FM EN	PI SEL	KEY RIM(1)	KEY ITO EN	MC IGNORE PARITY(1)	-	BIO PI SEL	PI RQ	PI RQ	KEY RDI(1)	PN PAR ODD	MC REQ CYC	MC RD(1)	MC WR(1)	GND
3C01	2T39	IOB 0	IOB 1	IOB 2	IOB 3	IOB 4	IOB 5	IOB 6	KEY CONT(1)	KEY CONT(1)	KEY RDI(1)	PN PAR ODD	MC REQ CYC	MC RD(1)	MC WR(1)	GND
3C02	2T38	IOB 14	IOB 15	IOB 16	IOB 17	IOB 18	IOB 19	IOB 20	PI CYC(1)	PI CYC(1)	KEY RDI(1)	PN PAR ODD	MC REQ CYC	MC RD(1)	MC WR(1)	GND
3C03	2T37	RUN(1)	RUN(0)	IOB RDI DATA	KEY CONT(1)	KEY CONT(0)	KEY SING INST	IOB 28	KEY CONT(0)	KEY CONT(0)	KEY RDI(1)	PN PAR ODD	MC REQ CYC	MC RD(1)	MC WR(1)	GND

NOTES: 1.\*

NAME	ORIGIN
IR UO IND	1P26F
MC PAR STOP IND	1S18U
MC STOP IND	1T16U

REVISIONS

REV	CHANGE NO.	DATE	BY
1	1	1-11-68	...
2	2	1-19-68	...

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSION IN INCHES			
TOLERANCES			
DECIMALS FRACTIONS ANGLES			
± .005 ± 1/64 ± 0°30'			
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL			
FINISH			
SCALE			
SHEET OF			
DATE 2-1-67			
DATE 1-11-68			
DATE 1-19-68			
DATE 1-19-68			
FIRST USED ON			
TITLE			
INTER-BAY CABLES			
SIZE CODE			
NUMBER			
REV			
SCALE			
SHEET OF			

CABLE PINS

FROM	TO	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V
3001	2540	IOB 0	IOB 1	IOB 2	IOB 3	IOB 4	IOB 5	IOB 6	IOB 7	IOB 8	IOB 9	IOB 10	IOB 11	IOB 12	IOB 13	GND
3002	2539	IOB 14	IOB 15	IOB 16	IOB 17	IOB 18	IOB 19	IOB 20	IOB 21	IOB 22	IOB 23	IOB 24	IOB 25	IOB 26	IOB 27	GND
3003	2538	KEY SING INST	KEY START(W)	KEY EXECUTE (1)	KEY SYNC OPS	KT 1 EN	IOB STATUS A	IOB 28	IOB 29	IOB 30	IOB 31	IOB 32	IOB 33	IOB 34	IOB 35	GND
3F01	2542	IR 3 (0)	IR 3 (2)	IR 4 (0)	IR 4 (1)	IR 5 (0)	IR 5 (1)	IR 6 (0)	IR 6 (1)	IR 7 (0)	IR 7 (1)	IR 8 (0)	IR 8 (1)	IR 9 (0)	IR 9 (1)	GND
3F02	2541	IR 10 (0)	IR 10 (1)	IR 11 (0)	IR 11 (1)	IR 12 (0)	IR 12 (1)	IOB FM AR	AR FOV (1)	AR OV FLAG (1)	IOT DATAI	IOT DATAO	PI STATUS A	PI STATUS B	PI ACT (1)	GND
3E02	2T41	PIH 1 (1)	PIH 2 (1)	PIH 3 (1)	PIH 4 (1)	PIH 5 (1)	PIH 6 (1)	PIH 7 (1)	PIO 1 (1)	PIO 2 (1)	PIO 3 (1)	PIO 4 (1)	PIO 5 (1)	PIO 6 (1)	PIO 7 (1)	GND
3E03	2T40	KEY F1 (1)	KEY SYNC RQ (1)	KEY SYNC (1)	KEY MEM REF	KEY NEXT	KEY RDI (1)	IOB PI 1	IOB PI 2	IOB PI 3	IOB PI 4	IOB PI 5	IOB PI 6	IOB PI 7	IOB PI 8	GND
3E04	1S43	KEY ADR BEK	KEY ADR INST	KEY ADR RD	KEY ADR STOP	KEY ADR WR	KEY ADR WR	KEY AS STROBE EN	KEY SING CYCLE	KEY DEP V DEP NXT VEXE	KEY DEP V NXT	KEY EX V NXT	KEY NXM STOP	KEY NXM STOP	KEY PAR STOP	GND
3E05	1S44	MR PWR CLR ENB	MR PWR CLR ENB	IOT CONO SET	IOT CONO CLR	IOT DATAO SET	IOT DATAO CLR	IOB DATAI A	CPA PWR FAIL (0)	IOB DR SPILT	CPA CONO SET	IOT GO (1)	EX IOT USER (1)	CPA PWR DLY	BIO CPA SEL	BIO PI SEL
3E06	1L44	IOT BLK	IOT CONI	IOT CONO	IOT CONSO	IOT CONSX	IOT CONSX	IOT CONSZ	IOT T2	CPA CONO SET	IOT GO (1)	IR IOT	KEY AT INH	MA TRAP OFFSET	MC ADR BRK SET	GND
1P01	2P09	IOB 23	IOB 24	IOB 25	IOB 26	IOB 29	IOB 32	MI PROG (0)	MI PROG (1)	MR PWR CLR ENB	*MC STOP IND	GND	GND	GND	GND	PI CONO SET
1R02	2R03	MAI CMC ADR ACK	MC BUS WR RS	GND	MC PARIY PULSE	GND	KT 3A	GND	*MC PAR STOP IND	GND	GND	GND	GND	GND	GND	GND
W021	W021	IOT T3B	IOT T4	GND	IOT T5	GND	GND	GND	GND	GND	GND	GND	KST 2	MR PWR CLR R	GND	MR START R

REVISIONS

REV	CHANGE NO.	DATE	BY	CHK
32	A	1-16-68	W.S.	

PAID - 00035 1 P  
T. GUILLEN 7-23-67  
KENT  
O. Kotal 23 JUL 68

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
UNLESS OTHERWISE SPECIFIED	DATE	TITLE	
DIMENSION IN INCHES	1-16-68	INTER-BAY CABLES	
TOLERANCES	DATE	DATE	
DECIMALS FRACTIONS ANGLES	12/18/68	17/7/68	
± .005 ± 1/64 ± 0°30'	DATE	DATE	
FINAL SURFACE QUALITY	1-19-68	1-19-68	
REMOVE BURRS AND BREAK SHARP CORNERS	DATE	DATE	
MATERIAL	FIRST USED ON	SIZE CODE NUMBER REV.	
FINISH	SCALE	D1CL KA10-0-IBC2	
SHEET	OF	DIST.	

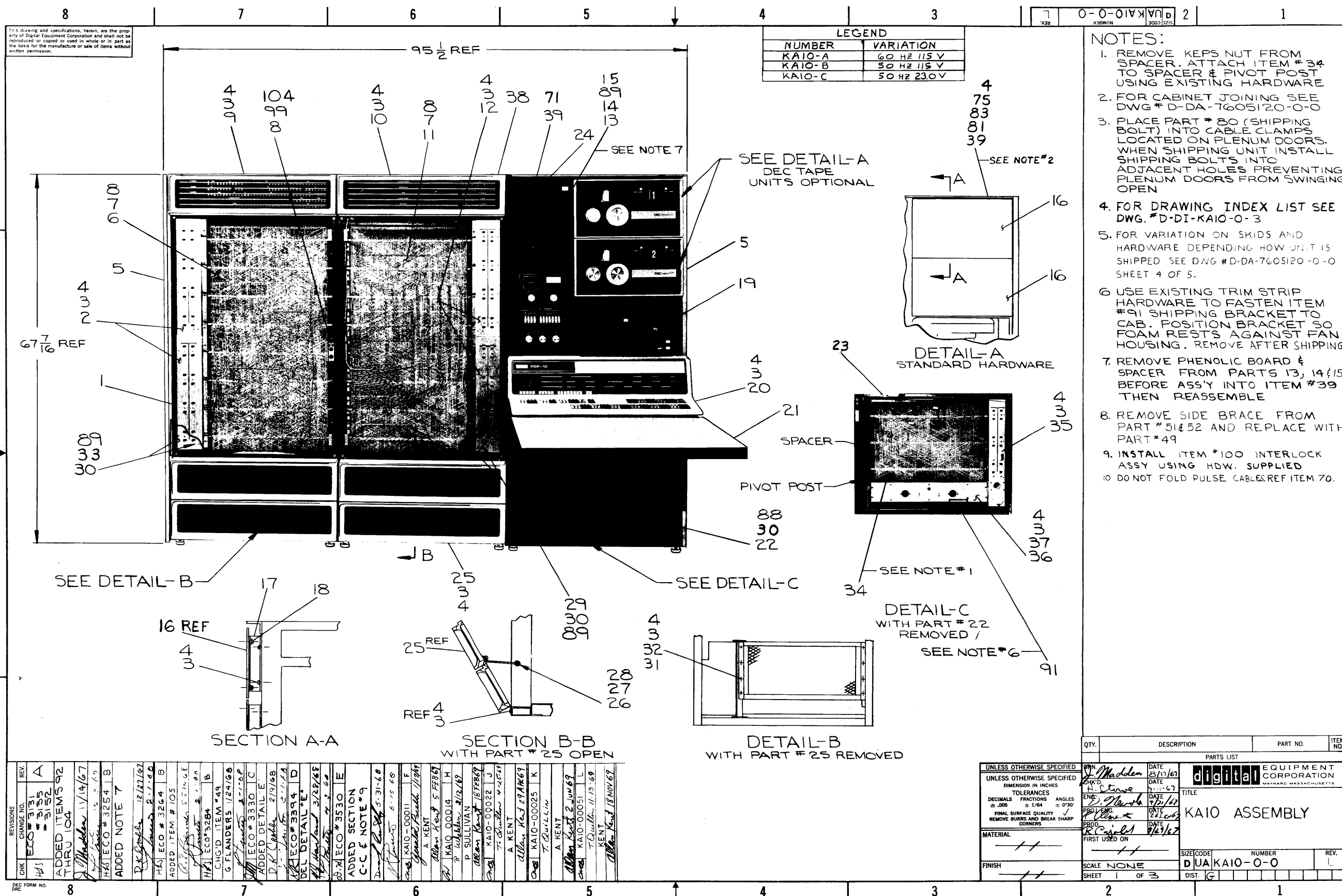
DEC FORM NO. DRD 102











LEGEND

NUMBER	VARIATION
KAIO-A	60 HZ 115 V
KAIO-B	50 HZ 115 V
KAIO-C	50 HZ 230V

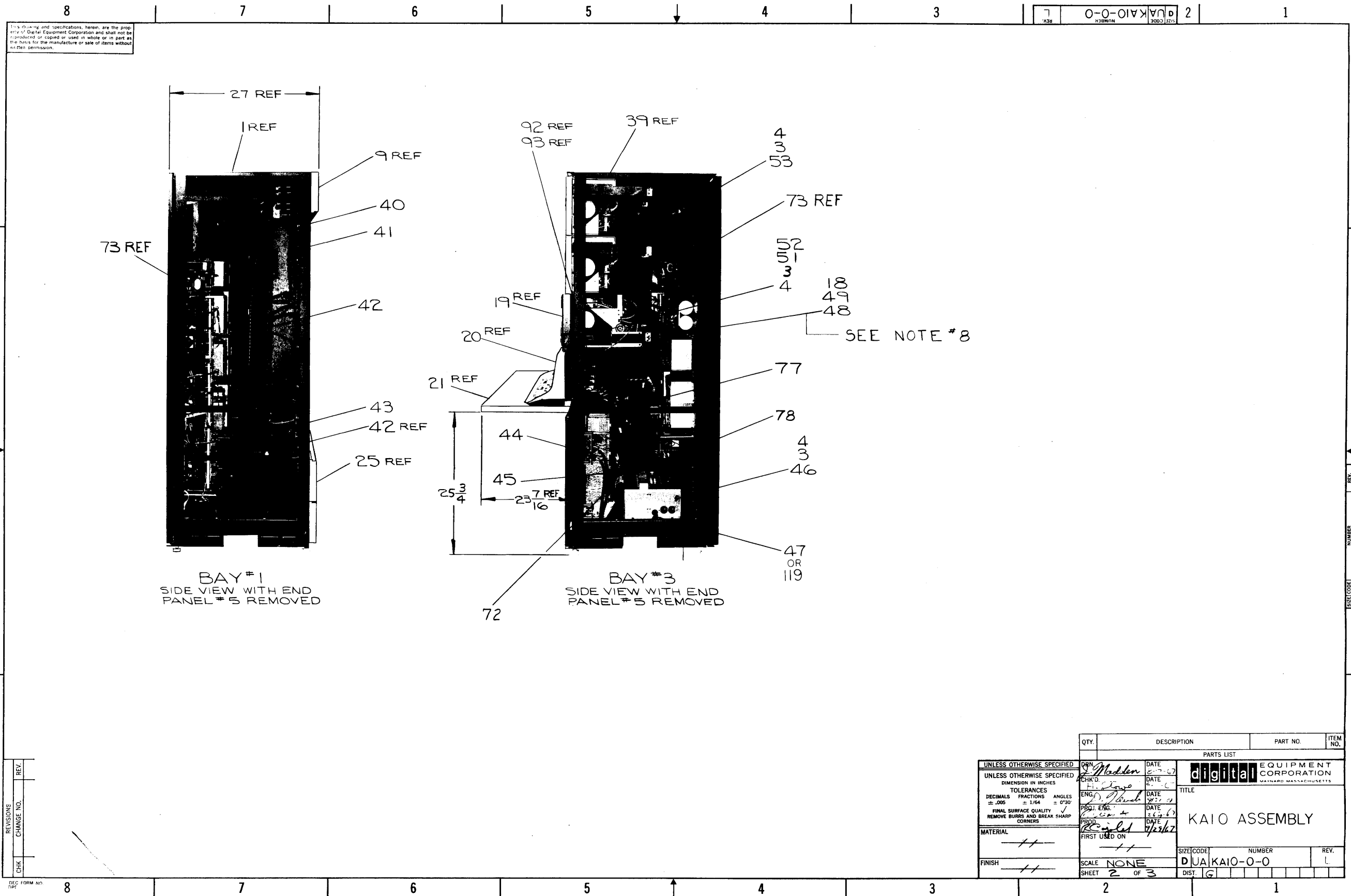
- NOTES:
1. REMOVE KEPS NUT FROM SPACER. ATTACH ITEM #34 TO SPACER & PIVOT POST USING EXISTING HARDWARE
  2. FOR CABINET JOINING SEE DWG #D-DA-7605120-0-0
  3. PLACE PART #80 (SHIPPING BOLT) INTO CABLE CLAMPS LOCATED ON PLENUM DOORS. WHEN SHIPPING UNIT INSTALL SHIPPING BOLTS INTO ADJACENT HOLES PREVENTING PLENUM DOORS FROM SWINGING OPEN
  4. FOR DRAWING INDEX LIST SEE DWG. #D-DI-KAIO-0-3
  5. FOR VARIATION ON SKIDS AND HARDWARE DEPENDING HOW UNIT IS SHIPPED SEE DWG #D-DA-7605120-0-0 SHEET 4 OF 5.
  6. USE EXISTING TRIM STRIP HARDWARE TO FASTEN ITEM #91 SHIPPING BRACKET TO CAB. POSITION BRACKET SO FOAM RESTS AGAINST FAN HOUSING. REMOVE AFTER SHIPPING
  7. REMOVE PHENOLIC BOARD & SPACER FROM PARTS 13, 14 & 15 BEFORE ASS'Y INTO ITEM #39 THEN REASSEMBLE
  8. REMOVE SIDE BRACE FROM PART #51 & 52 AND REPLACE WITH PART #49
  9. INSTALL ITEM #100 INTERLOCK ASSY USING HDW. SUPPLIED
  10. DO NOT FOLD PULSE CABLES REF ITEM 70.

UNLESS OTHERWISE SPECIFIED	UNLESS OTHERWISE SPECIFIED	DATE	BY
DIMENSION IN INCHES	TOLERANCES	8/11/67	Madden
DECIMALS ± .005	FRACTIONS ± 1/64	DATE	DATE
ANGLES ± 0°30'	FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	7/2/67	7/2/67
MATERIAL	PROBING	2/21/68	2/21/68
FINISH	PROD.	9/23/67	9/23/67

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
	digital EQUIPMENT CORPORATION		
	NORFOLK MASSACHUSETTS		
TITLE		KAIO ASSEMBLY	
SCALE NONE	SHEET 1 OF 3	DIST. (C)	REV. L

REV.	DESCRIPTION	DATE	BY
A	ECO #315	11/14/67	Madden
	ADDED ITEMS 92 THRU 104		
B	ECO #3254	11/14/67	Madden
	ADDED NOTE 7		
B	ECO #3264	12/21/67	D. K. Griffin
B	ECO #105	2/1/68	H.A. Flanders
B	ECO #3284	2/1/68	H.F. Griffin
C	ECO #3330	2/1/68	H.F. Griffin
D	ECO #3399	2/19/68	D. K. Griffin
E	ECO #3530	3/28/68	A. Kent
F	ECO #0011	6/15/68	A. Kent
F	ECO #0002	5/31/68	A. Kent
F	ECO #0014	5/31/68	A. Kent
H	ECO #0014	4/12/69	A. Kent
I	ECO #0022	4/12/69	P. Sullivan
J	ECO #0022	4/12/69	A. Kent
K	ECO #0025	4/12/69	A. Kent
L	ECO #0051	4/12/69	A. Kent
L	ECO #0051	11/13/69	T. Quinn
L	ECO #0051	11/13/69	A. Kent
L	ECO #0051	11/13/69	A. Kent





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BAY #1  
SIDE VIEW WITH END  
PANEL #5 REMOVED

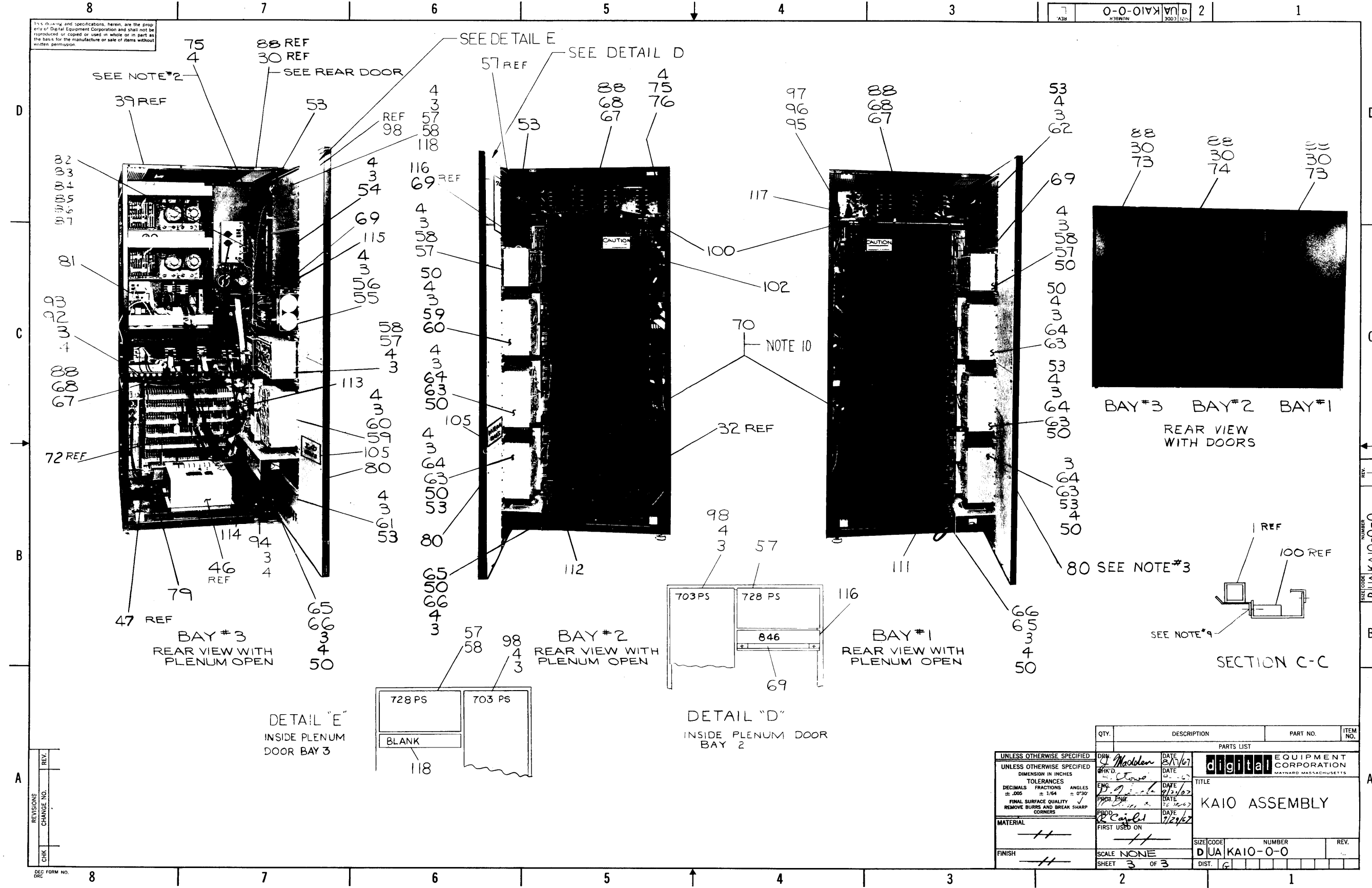
BAY #3  
SIDE VIEW WITH END  
PANEL #5 REMOVED

SEE NOTE #8

REV.	
CHG.	

UNLESS OTHERWISE SPECIFIED	DRN	DATE	PARTS LIST	
UNLESS OTHERWISE SPECIFIED	CHKD.	DATE	digital	EQUIPMENT CORPORATION
DIMENSION IN INCHES	ENG.	DATE	TITLE	
TOLERANCES	PROJ. ENG.	DATE	KAIO ASSEMBLY	
DECIMALS FRACTIONS ANGLES	PROD.	DATE	SIZE CODE	NUMBER
±.005 ±.0005 ±.1/64 ±.030	FIRST USED ON		DUA	KAIO-0-0
FINAL SURFACE QUALITY			DIST.	G
REMOVE BURRS AND BREAK SHARP CORNERS				
MATERIAL				
FINISH				
SCALE NONE				
SHEET 2 OF 3				

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**DIGITAL EQUIPMENT CORPORATION**  
MAYNARD, MASSACHUSETTS

**PARTS LIST**

ITEM NO.	DWG. NO.	DESCRIPTION	QUANTITY			REVISIONS		
			KAL0-A	KAL0-B	KAL0-C	CHANGE NO.	DATE	ENG.
1	E-AD-7005339-1-0	CABINET FRAME ASSEMBLY BAY #1	1	1	1	A-3131 3135	11/19/67	
2	E-AD-7005378-0-0	MARGINAL CHECK ASSEMBLY BAY #1	2	2	2	3152 EXT. CHG. SEE PREV REF.	19/67	
3		SCR PHL H TRUSS 10-32 x 1/2 SST	271271271			B3254 CHGD QTY	12/27/67	
4		WASH EXT TOOTH #10	286286286			ITEM #89 ADD ITEM #105	1/5	
5	E-IA-7405092-0-0	END PANEL ASSY	2	2	2	B-3284 CHG'D	1/24/68	
6	D-AD-7005354-0-0	LOGIC FRAME ASSEMBLY BAY #1	1	1	1	ITEM NO 49 & 41		
7		SCR HEX H CAP 1/20 x 1 SST	12	12	12	C-3330 CHG QTY	2/9/68	
8		WASH EXT TOOTH 1/4	7	7	7	ITEM #88 ADDED ITEMS		
9	D-AD-7005335-1-0	INDICATOR PANEL ASSEMBLY	1	1	1	#106,107 108,109,110		
10	D-AD-7005335-2-0	INDICATOR PANEL ASSEMBLY	1	1	1	D-3394 CHG QTY	3/27/68	
11	D-AD-7005350-0-0	LOGIC FRAME ASSEMBLY BAY #2	1	1	1	#88 DEL #'S		
12	E-AD-7005377-0-0	MARGINAL CHECK ASSEMBLY BAY #2	2	2	2	106,107, 108,109,		
13	E-AD-7005352-2-0	MARGINAL CHECK & MAINT PANEL ASSEMBLY	1			110.		
14	E-AD-7005352-1-0	MARGINAL CHECK & MAINT PANEL ASSEMBLY	1			E-3530 CHG ASSY	5/10/68	
MADE BY J. MADDEN			DRWG. NO. A-PL- KAL0-0-0			REV. LTR. L		
CHECKED H. Stone			ASSY NO D-UA-KAL0-0-0			SHEET 1 OF 9		
ENG D. Menden			FOR KAL0-A (60 HZ 115V) KAL0-B (50 HZ 115V) KAL0-C (50 HZ 220V)					

**DIGITAL EQUIPMENT CORPORATION**  
MAYNARD, MASSACHUSETTS

**PARTS LIST**

ITEM NO.	DWG. NO.	DESCRIPTION	QUANTITY			REVISIONS		
			KAL0-A	KAL0-B	KAL0-C	CHANGE NO.	DATE	ENG.
15	E-AD-7005352-3-0	MARGINAL CHECK & MAINT PANEL ASSEMBLY				E-3530	5/31/68	
16	C-IA-7406063-0-0	PANEL, BLANK FILLER	1			DEL NO 101		
17	C-WD-7406336-0-0	BRACKET, SUPPORT	2	2	2	F-KA10-00011	1/17/69	
18		NUT KEPS 8-32 SST	4	4	4	H-KA10-00014	2/14/69	
19	D-UA-PC09-A-0	PC09-A READER & PUNCH	12	12	12	J-KA10-00028	4-28/69	
20	D-AD-7005344-0-0	CONTROL PANEL ASSEMBLY	1	1	1	K-KA10-00025	2 JUN 69	
21	D-AD-7005090-0-0	TABLE	1	1	1	L-KA10-00051	1/13/69	
22	D-AD-7005347-0-0	FRONT DOOR BAY #3	1	1	1			
23		SCR PHL FLAT H 6-32 x 3/8 SST	2	2	2			
24	E-AD-7005355-0-0	FRONT DOOR ASSEMBLY BAY #3	1	1	1			
25	D-AD-7005270-0-0	AIR INTAKE ASSEMBLY	2	2	2			
26		SPACER 1/4D x 3/16 #6-32 AL	4	4	4			
27		WASH PLAIN 3/8D x 1/32 #6 SST	4	4	4			
28		SCR PHL HD PAN 6-32 x 5/8 SST	4	4	4			
MADE BY J. MADDEN			DRWG. NO. A-PL- KAL0-0-0			REV. LTR. L		
CHECKED H. Stone			ASSY NO D-UA-KAL0-0-0			SHEET 2 OF 9		
ENG D. Menden			FOR KAL0-A (60 HZ 115V) KAL0-B (50 HZ 115V) KAL0-C (50 HZ 220V)					