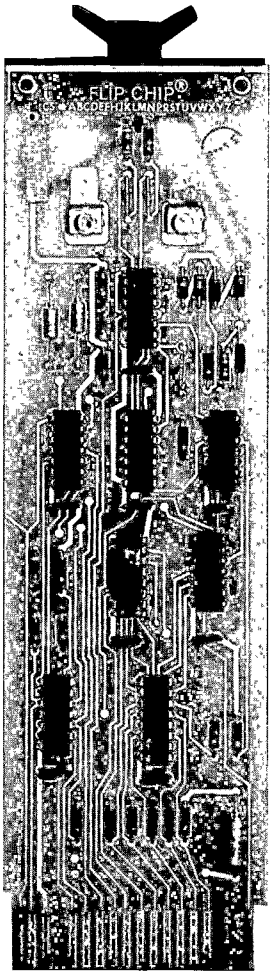
DIGITAL EQUIPMENT CORPORATION

MODULE DATA SHEET

LOGIC PRODUCTS

JULY 1974

M7346 External Event Detection Module



DESCRIPTION

The M7346 External Event Detection Module is a multipurpose unit manufactured by DIGITAL for use in conjunction with the M7341 Processor Module to implement interrupt priority schemes, power failure detection, and processor restart and halt control. This module is one of the Microprocessor Series (MPS) modules, a group of M Series modules designed to perform a range of industrial, laboratory, and commercial control and decision-making activities not previously considered as economic subjects for automation. These modules are:

- M7346 External Event Detection Module
- M7341 Processor Module
- M7344 Read/Write Memory Module
- M7345 Programmable Read-Only Memory Module

Used together, these modules can form low-cost digital control systems which exhibit characteristics normally attributed to more costly minicomputer-based systems. MPS systems can serve as dedicated controllers, operate as a CPU in intelligent terminals, perform data acquisition and analysis tasks in the laboratory, and automate a host of industrial processes.

The M7346 External Event Detection Module (EEDM) implements nine levels of priority arbitration. These include application-defined six-level priority interrupt schemes, an ac and dc power failure detection capability, and the processor control functions of Halt and Restart. The EEDM is completely contained on a single-height, extended-length PC board.

Separate input lines to the EEDM provide for encoding up to six levels of external application-defined event priority. Each of these lines, when asserted, initiates an attempt to jam a 1-byte unconditional call (RST) instruction into the M7341 Processor Module external event port.

The EEDM priority logic arbitrates all assertions and selects the highest level asserted, then jams the corresponding instruction into the Processor Module. The jammed RST instruction associated with each priority level (zero through five) constitutes an unconditional call on one of six 8-byte subroutines located in the first 48 words of an MPS system memory.

The eight output lines which propagate the instruction being jammed, are connected in common to the processor module external event port and the power-fail port.

To jam an RST instruction, the EEDM asserts a signal to enable multiplexing of the external event port and to initiate an external event interrupt. If interrupts are enabled at the Processor Module, the RST instruction is fetched and executed. If not, the RST instruction is ignored.

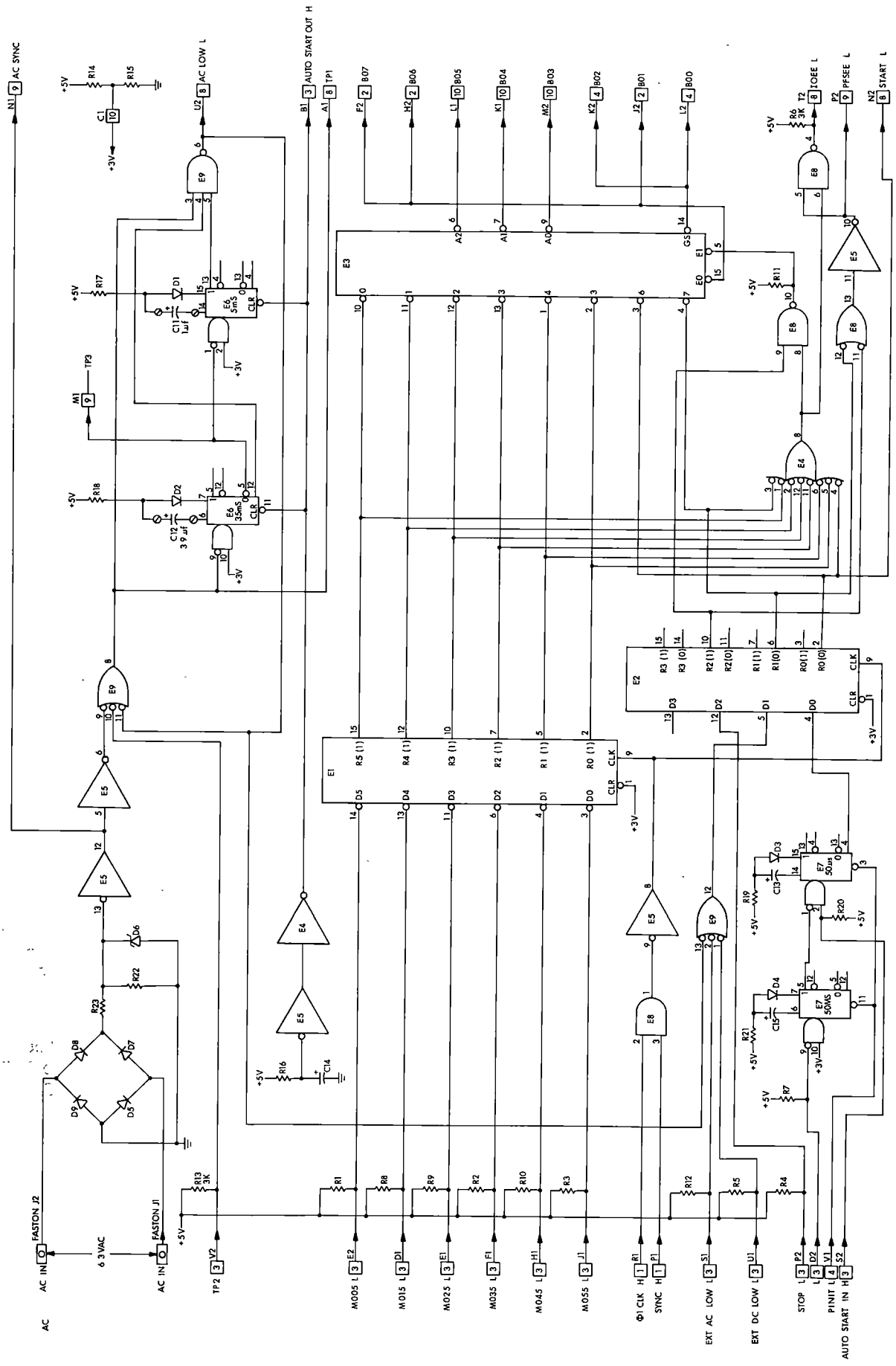


FIGURE 1. M7346 LOGIC BLOCK DIAGRAM

The seventh priority level is asserted by either a manually-initiated start signal or automatically as a consequence of power-up. In either of these cases, an RST instruction is generated which makes an unconditional call on eight reserved memory words headed by location 48 (60_8).

Priority level eight is asserted by the power failure detection circuit which monitors ac power inputs to an MPS system. When a power failure condition is detected, an RST instruction is automatically generated which makes an unconditional call on location 56 (70_8). Since level eight is the highest arbitrated priority, a power failure takes precedence over any of the six levels of application-defined event priorities as well as the seventh or start level.

Level nine implements the halt function for MPS systems. This function can be initiated manually or automatically, and overrides all other priorities. When initiated, a halt instruction is placed on the lines to the processor module, and the power fail/stop port is enabled for multiplexing. When fetched, this instruction forces the Processor Module into the stopped state.

FEATURES

- Eight interrupt priority request lines available to provide eight arbitrated priority levels.
- Power failure detection circuit continuously samples ac voltage levels.
- Inputs for optional external ac and/or dc power failure detection.
- Power failure detection is highest arbitrated priority.
- Halt function has precedent over all arbitrated priorities.
- Module senses power-up condition to initiate an automatic start.
- External event response time 12 to 44 μs.
- Power failure response time 35 ms from ac power loss to power fail interrupt request.
- Real-time clock signal (power line sync signal) available at module connector.
- Power fail indication signal (AC LOW) available at module connector.
- Except for ac sample input, all inputs and outputs are TTL-compatible.
- Module is contained on standard single-height extended-length board and plugs into standard DEC H863 and H803 wire-wrap connector block backplanes or equivalents.

SPECIFICATION SUMMARY

Performance

Number of Event Detection Input Lines: 8

Priority Encoded: 1—lowest
8—highest

External Event Response Time: 12 to 44 μs

Power Failure Response Time: 35 ms (from ac loss to power-fail interrupt request)

Input Polarity,
External Event Lines: +3V=True

Output Polarity,
Data Lines to Processor Module: +3V=True

Electrical

Power Supply: +5 Vdc,

Input Logic Levels
Logical Low: 0.8 Vdc maximum
Logical High: 2.0 Vdc minimum

Output Logic Levels
Logical Low: 0.4 Vdc maximum
Logical High: 2.4 Vdc minimum

Noise Immunity: 400 mV

Power Fail Sense Input: 6.3 V ac

Power Consumption: 250 mA @ +5 V
50 mA @ 6.3 V ac, 1.6 W

Mechanical

Board Type: Single height extended-length, single-width

Dimensions: 2.4375 X 8.50 X 0.50 inches
6.191 X 21.590 X 1.270 cm

Environmental

Ambient Temperature
Operating: 5 to 50°C; (41 to 122°F)
Nonoperating: —40 to 66°C (—40 to 150°F)

Humidity: 10 to 95% noncondensing

APPLICATIONS

In addition to the power failure detection capability, the External Event Detection Module can generate up to eight vectored priority requests in response to a service request from an associated input/output device.

Figure 2 is a simplified block diagram of a typical use of the M7346 External Event Detection module in arbitrating peripheral service requests. A printer is used to generate service requests only as an example. When the printer asserts its service request line, the READY flip-flop (which can be one of the six flip-flops in an M203 module) is set. As shown in the example of Figure 2, setting this flip-flop asserts the EED module input priority line M045 L which designates a level 5 priority. The EED module then generates an RST instruction with its address field set to octal 40. Simultaneously, the signal IOEEL is asserted.

If interrupts are enabled by the Processor Module, asserting this signal initiates multiplexing of the RST instruction generated by the printer into the I/O start port DIOST0 L to DIOST7 L for fetching by the processor. Execution of this RST instruction results in an unconditional transfer of program control to octal location 40. This location can be an entry into an external event-handling routine which would save the current state of the Processor Module, then service the printer in the same manner as with normal output-to-peripheral operations.

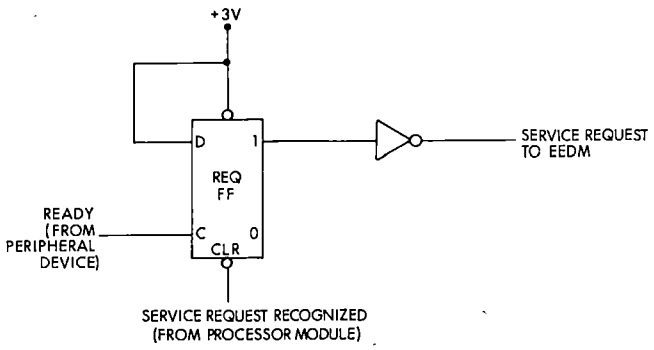


FIGURE 2. TYPICAL EXAMPLE OF PERIPHERAL SERVICE REQUEST ARBITRATION

FUNCTION

Priority Arbitration Logic

EEDM priority arbitration logic (see Figure 1) accepts nine levels of ascending priority. Eight of these levels result in a memory reference and the ninth, and highest, is executed by the Processor Module without referencing memory. Level 0 through 5, designated by the input signal lines M006 L, M015 L, M025 L, M035 L, M045 L, and M055 L, constitute the six lowest priority levels. These lines are reserved for implementing six levels of application-defined interrupt priority arbitration.

The seventh level is reserved for the automatic and manual restart function, and the eighth and highest arbitrated level, for power failure detection. The ninth, and highest absolute level, is reserved for the stop function which automatically jams a HLT instruction into the Processor Module to stop operation.

EEDM priority arbitration logic is formed by the nine-stage external event storage latch, E3 and E2, and the octal encoder, E4. Assertions of any of the nine levels are stored during the combined periods of the Processor Module synchronous timing signals SYNC H and Φ1CLCK H. These signals are ANDed to strobe the external event storage latch, E1 and E2, once during each processor state time (every 4 μs) to store asserted events. The outputs of the first eight stages of the external event storage latch are input to the octal priority encoder E3. These eight input lines are ORed by E4 to enable the encoder. The outputs of the encoder, E0 and GS, are wired to assert the code for an RST instruction on module output lines B00 to B02 and B06 and B07. The octal number corresponding to the external event input line asserted is simultaneously placed in the address field (B03 to B05) of the RST instruction generated by encoder E3.

In parallel with the generation of the RST instruction, the outputs of the first eight stages of latch E1, E2 are ORed by E4 to assert the signal IOEE L at the Processor Module. This signal, when asserted, generates an interrupt if interrupts are enabled, and initiates multiplexing of the RST instruction on EEDM output lines B00 to B07 at the Processor Module external event port DIOST0 L to DIOST7 L for fetching.

The octal number placed in the address field of the RST instruction generated is in the range of 0 to 7. Through decoding of this instruction, this value is mapped to address one of the eight locations 0, 8, 16, 24, 32, 40, 48, and 56 (octal 10, 20, 30, 40, 50, 60, and 70 respectively) in an MPS system memory. The result is a correspondence between a given external event input line and an unconditional call on a dedicated memory location. Through this mechanism, application-defined routines can be developed to implement priority interrupt schemes, start-up routines, and power-failure handling routines.

Start Circuit

The start function can be initiated in two ways: automatically by an integral EEDM circuit, or manually by an external switch. The automatic start output signal AUTO START OUT H is generated by the RC circuit R16, C14, and E5 when +5 V power is turned on and is maintained high as long as +5 V is maintained. The output of this circuit also clears the two monostable multivibrators, E6, in the power failure detection circuit. This automatically-generated start signal, when fed back to the EEDM, becomes the input signal AUTO START IN H. When asserted, this signal triggers the monostable multivibrator E7 to produce a 50 μs signal at pin 4. This signal is stored in the seventh stage of the external event latch, E1, E2, on the next assertion of Φ1CLK H and SYNC H from the Processor Module. As a consequence, an RST instruction making an unconditional call on memory location 48 (60_8) is generated and placed on output lines B00 to B07. Simultaneously, the signal START L is asserted at the Processor Module to initiate a demand interrupt and to multiplex the RST instruction into the external event port DIOST0 L to DIOST7 L for fetching. Manual restarts are implemented through the EEDM input signal START L which can be derived from an external switch. This signal is debounced by the monostable multivibrator E7 which produces a 50 ms negative-going debouncing level at pin 5 for input to E7 at pin 1. From this point, the circuit path is exactly the same as with an automatic restart. Both automatic and manual start signals take priority over all other external events except power failure detection and stop functions.

Power Failure Detection Circuit

The EEDM contains a complete ac power failure detection circuit (see Figure 1) which samples a 6.3 V, 50 or 60 Hz, ac input derived from the local line voltage by an external transformer. This sampled ac voltage, which is received through two FASTON tabs on the handle end of the module, is rectified by a full-wave diode bridge to produce a signal having a frequency twice that of the ac input frequency. This signal is input to the frequency integrator E5, E9, and E6 which detects the absence of line voltage for two complete cycles. The signal period triggered by a power failure is approximately 34 ms and is determined by the value of capacitor C12 which, together with R18, forms the RC for the monostable multivibrator E6 at pins 6 and 7. Note that C12 is connected to the circuit with split lugs. This manner of connection permits the value of C12 to be changed to accommodate different application requirements.

When an absence of two or more ac cycles is detected, the multivibrator E6 is triggered at pin 1 to assert a 5-ms signal to be gated out by E9 at pin 6. This period is determined by the RC circuit R17, C11, where capacitor C11 is connected to the circuit with split lugs to allow the value of C11 to be changed to accommodate different application requirements.

The 5-ms output signal from the frequency integrator is ORed with the externally generated signals AC LOW L and DC LOW L for input to level seven of the external event storage latch E2, E3. This input is stored in the latch on the assertion of the Processor Module signals SYNC H and Φ1CLK H. Since both of these signals are continuous irrespective of processor state, storage of a power failure detection signal for fetching by the processor is assured even when the processor is in the Wait state.

The external inputs AC LOW L and DC LOW L allow use of application-defined power failure detection circuitry whose outputs are TTL levels. Note: Many commercially-available power supplies provide such output signals. Power failure detection by the integral EEDM circuit or assertion of one of these external signals takes priority over all external events except assertion of the external signal STOP L.

A detection of power failure results in the automatic generation of an RST instruction which makes an unconditional call on memory location 56 (70_8). Simultaneously, the signal PFSEE L is asserted by E8, pin 13 of the priority arbitration logic to generate a mandatory interrupt at the Processor Module and to enable multiplexing of the RST instruction into the power-fail port DPFS0 L to DPFS7 L for fetching.

Stop Function

A halt instruction is generated by the EEDM when the input signal STOP L is asserted. When this occurs, the signal is stored in the ninth stage of the external event latch E1, E2 in the same manner as other external events. However, this stage is not input to the priority arbitration logic but rather directly disables encoder E3 to generate and place a halt instruction (HLT) on the lines B00 to B07.

As with detection of a power failure, the signal PFSEE L is asserted at the Processor Module power Fail/Stop port by the EEDM to initiate multiplexing and fetching of the halt instruction.

SIGNAL SPECIFICATIONS

Input Signals

Symbol	*Description*	*Pin*	*Function*
M005L	External Event Input Line Priority 1	E2	These external event detection lines provide for application-defined priority interrupt processing. These lines are arbitrated by the EEDM on the basis of ascending priority with line M005 L having the lowest possible priority (level 1) and line M055 L having the highest priority (level 6) within this group.
M015L	External Event Input Line Priority 2	D1	
M025L	External Event Input Line Priority 3	E1	
M035L	External Event Input Line Priority 4	F1	
M045L	External Event Input Line Priority 5	H1	
M055L	External Event Input Line Priority 6	J1	
EXT DC LOW L	External dc Power Failure Detection Signal	U1	This input signal is a TTL level generated by external equipment which when true designates a loss of dc power, This signal has a level-8 priority.
EXT AC LOW L	External ac Power Failure Detection Signal	S1	This input signal is a TTL level generated by external equipment which when true designates a loss of ac power. This signal has a level-8 priority.
START UP L	Manual Start Input Signal	D2	This input signal is a TTL level which can be derived from an external switch closure to initiate start-up of the Processor Module. This signal has a level-7 priority.
AUTO START IN H	Automatic Start Input Signal	S2	This input signal is the EEDM output signal AUTO START OUT H fed back to initiate an automatic start-up upon power-up. This signal has a level-7 priority.
STOP L	Signal to Halt Processor Module	P2	This input signal is a TTL level which can be derived from an external source to initiate halting of the Processor Module. This is the highest priority input to the EEDM (level nine).

Input Signals (continued)

Symbol	*Description*	*Pin*	*Function*
AC PLUS IN	Ac Sampling Voltage Positive Terminal	J1	This signal is the +6.3 Vac brought into FASTON tab J1 from an external transformer for sampling by the EEDM power failure detection circuit.
AC MINUS IN	Ac Sampling Voltage Negative Terminal	J2	This signal is the −6.3 Vac brought into FASTON tab J2 from an external transformer for sampling by the EEDM power failure detection circuit.
Φ1CLK H	Processor Module Clock Signal	R1	This is the first phase of the Processor Module two-phase clock and is used in conjunction with SYNC H to strobe external event signals into the EEDM for priority arbitration.
SYNC H	Processor Module Synchronization Signal	P1	This signal is the basic machine cycle synchronization signal for the Processor Module and is used in conjunction with ΦCLK H at the EEDM to control input timing of external event signals.
PINIT L	System Initialize Signal	V1	This is the 10-ms system initialize signal from the Processor Module and is used to reset condition-sensitive EEDM logic at start-up time.
TP2	Test Point 2	V2	This test point is used to check the operation of the EEDM power failure detection circuit.

Output Signals

Symbol	*Description*	*Pin*	*Function*
B00	External Event and Power Fail/Stop Output Line 0	L2	
B01	External Event and Power Fail/Stop Output Line 1	J2	
B02	External Event and Power Fail/Stop Output Line 2	K2	
B03	External Event and Power Fail/Stop Output Line 3	M2	These eight output lines serve to convey the RST instructions generated in response to specific application-defined events to the Processor Module for fetching.
B04	External Event and Power Fail/Stop Output Line 4	K1	These lines can be connected to both the PM external event and power fail/stop port.
B05	External Event and Power Fail/Stop Output Line 5	L1	
B06	External Event and Power Fail/Stop Output Line 6	H2	
B07	External Event and Power Fail/Stop Output Line 7	F2	

Output Signals (continued)

Symbol	*Description*	*Pin*	*Function*
IOEE L	External Event Enable Signal	T2	When program enabled at the PM, assertion of this line by the EEDM generates an interrupt of the Processor Module and enables multiplexing of an instruction from the EEDM into the PM for fetching.
PFSEE L	Power Fail/Stop Enable Signal	R2	When asserted by the occurrence of a power failure or the signal STOP L, this signal generates a mandatory interrupt of the Processor Module and enables the multiplexing of an RST or halt instruction from the EEDM into the PM.
START L	Start Processor Module	N2	This signal, when asserted at the Processor Module, generates a mandatory interrupt and enables the multiplexing of an RST instruction from the EEDM into the PM for fetching.
AUTO START OUT H	Automatic Start-up Circuit Output Signal	B1	This signal is generated automatically by the EEDM when power is applied to the module. This signal remains high as long as power is applied.
AC LOW L	Power Failure Indicator Signal	U2	When true, this output signal provides an external indication of an ac power failure.
TP1	Test Point 1	M1	These test points are used to check the operation of the EEDM power failure detection circuit.
TP3	Test Point 3	A1	
AC SYNC	Free-Running Real-Time Clock	N1	This free-running clock signal has a frequency of 120 Hz or 100 Hz depending on line voltage frequency (60 or 50 Hz respectively).
+3 V	+3 Vdc Logic Level	C1	A source of +3 Vdc for external use.

PROGRAMMING

The EEDM module arbitrates eight levels of priority and asserts a ninth level (halt) which is nonarbitrated. For each of the eight arbitrated levels, the EEDM generates an unconditional jump instruction (RST) whose jump address is one of eight dedicated locations in the first 64 words of an MPS system memory.

Each of these eight locations corresponds in relative magnitude to the specific priority level arbitrated and each is the first word of eight reserved memory locations. Table 1 lists the octal form of each RST instruction generated by the EEDM along with the octal form of the instruction, the jump address, and the related priority level. Note that the highest priority level implemented by the EEDM, level 9, results in the generation of a halt instruction.

TABLE 1

EEDM-Generated Instructions

Priority Level	Instruction Mnemonic	Octal Form	Jump Address		Comments
			Octal	Decimal	
1	RST	005	0	0	Application defined
2	RST	015	10	8	Application defined
3	RST	025	20	16	Application defined
4	RST	035	30	24	Application defined
5	RST	045	40	32	Application defined
6	RST	055	50	40	Application defined
7	RST	065	60	48	Reserved for Restart
8	RST	075	70	56	Reserved for Power Failure Detection
9	HLT	000	NA	NA	Halts the Processor Module

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 3).

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

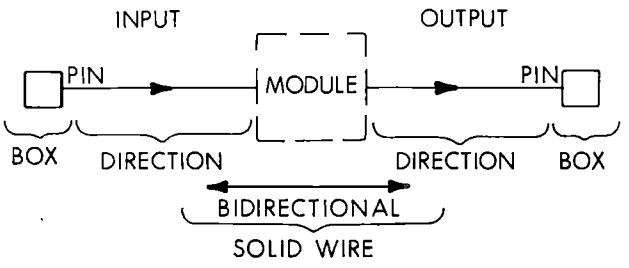


FIGURE 4. SIGNAL FLOW DIRECTION

POWER REQUIREMENTS

Volts	Power Consumption		Voltage Regulation	Ripple Regulation	Pins	
	mA	Watts			Power	Ground
+5Vdc	250	1.25	±5%	50mV	A2	C2,T1
6.3Vac	50	0.32			FASTON J2	FASTON J1

digital

DIGITAL EQUIPMENT CORPORATION

COMPONENTS GROUP HEADQUARTERS

ONE IRON WAY, MARLBOROUGH, MASSACHUSETTS 01752

(617) 481-7400 TWX 710-347-0348

For detailed information about products and policies, call 800-225-9480 toll-free (USA only), Massachusetts residents call (617) 481-7400.

DIGITAL EQUIPMENT CORPORATION, Maynard, Massachusetts, Telephone: (617) 897-5111 • ARIZONA, Phoenix • CALIFORNIA, Sunnyvale, Santa Ana, Los Angeles, Oakland, San Diego and San Francisco (Mountain View) • COLORADO, Englewood • CONNECTICUT, Meriden, Fairfield • DISTRICT OF COLUMBIA, Washington (Lanham, Md.) • FLORIDA, Orlando • GEORGIA, Atlanta • ILLINOIS, Northbrook • INDIANA, Indianapolis • LOUISIANA, Metairie • MASSACHUSETTS, Marlborough and Waltham • MICHIGAN, Ann Arbor and Detroit (Southfield) • MINNESOTA, Minneapolis • MISSOURI, Kansas City and Maryland Heights • NEW JERSEY, Fairfield, Metuchen and Princeton • NEW MEXICO, Albuquerque • NEW YORK, Huntington Station, Manhattan, New York, Syracuse and Rochester • NORTH CAROLINA, Durham/Chapel Hill • OHIO, Cleveland, Dayton and Euclid • OKLAHOMA, Tulsa • OREGON, Portland • PENNSYLVANIA, Bluebell and Pittsburgh • TENNESSEE, Knoxville • TEXAS, Dallas and Houston • UTAH, Salt Lake City • WASHINGTON, Bellevue • WISCONSIN, Milwaukee • ARGENTINA, Buenos Aires • AUSTRALIA, Adelaide, Brisbane, Canberra, Melbourne, Perth and Sydney • AUSTRIA, Vienna • BELGIUM, Brussels • BRAZIL, Rio de Janeiro, Sao Paulo and Porto Alegre • CANADA, Calgary, Montreal, Ottawa, Toronto and Vancouver • CHILE, Santiago • DENMARK, Copenhagen • FINLAND, Helsinki • FRANCE, Grenoble and Paris • GERMANY, Berlin, Cologne, Hannover, Frankfurt, Munich and Stuttgart • INDIA, Bombay • ISRAEL, Tel Aviv • ITALY, Milan and Turin • JAPAN, Tokyo • MEXICO, Mexico City • NETHERLANDS, The Hague • NEW ZEALAND, Auckland • NORWAY, Oslo • PHILIPPINES, Manila • PUERTO RICO, Santurce • SPAIN, Barcelona and Madrid • SWEDEN, Stockholm • SWITZERLAND, Geneva and Zurich • UNITED KINGDOM, Birmingham, Bristol, Edinburgh, London, Manchester and Reading • VENEZUELA, Caracas

PRINTED IN U.S.A. 5804 00874 3988/M 10 10