digital

**TU16/TM02
tape drive system
maintenance manual**

TU16/TM02
tape drive system
maintenance manual

EK-TU16-MM-002

digital equipment corporation • maynard, massachusetts

This document was set on DIGITAL's DECset-8000
computerized typesetting system.

CONTENTS

CONTENTS (CONT)

CONTENTS (CONT)

CONTENTS (CONT)

CONTENTS (CONT)

CONTENTS (CONT)

CONTENTS (CONT)

FIGURES

FIGURES (CONT)

FIGURES (CONT)

FIGURES (CONT)

TABLES

TABLES (CONT)

PREFACE

This manual is organized in a modular format to aid the user in finding information, at the level desired, in the shortest period of time. To accomplish this, the manual is broken down into five chapters, the contents of which are as follows:

Chapter 1, General Information — Contains general introductory information of interest to the operator, such as operating instructions, specifications, system configuration, and magnetic tape fundamentals.

Chapter 2, Theory of Operation — Presents an overview "Big Picture" of the theory of operation of the TU16/TM02 Tape Drive System. This chapter is intended to aid servicing personnel in understanding the basic principles of operation of the TU16/TM02. The final section of this chapter is a guide to the detailed servicing information in Chapter 3.

Chapter 3, Servicing — Consists of servicing pamphlets which describe various functional areas of the TU16/TM02. The first pamphlet, Maintenance Modes, describes on-line and off-line maintenance capabilities; the remaining pamphlets contain detailed theory of operation, performance checks, and adjustment and troubleshooting information.

Chapter 4, Removal and Replacement and Adjustment Procedures — Contains removal and replacement procedures, and the procedures required to adjust the TU16 Transport.

Chapter 5, Preventive Maintenance — Contains the preventive maintenance schedule and procedures.
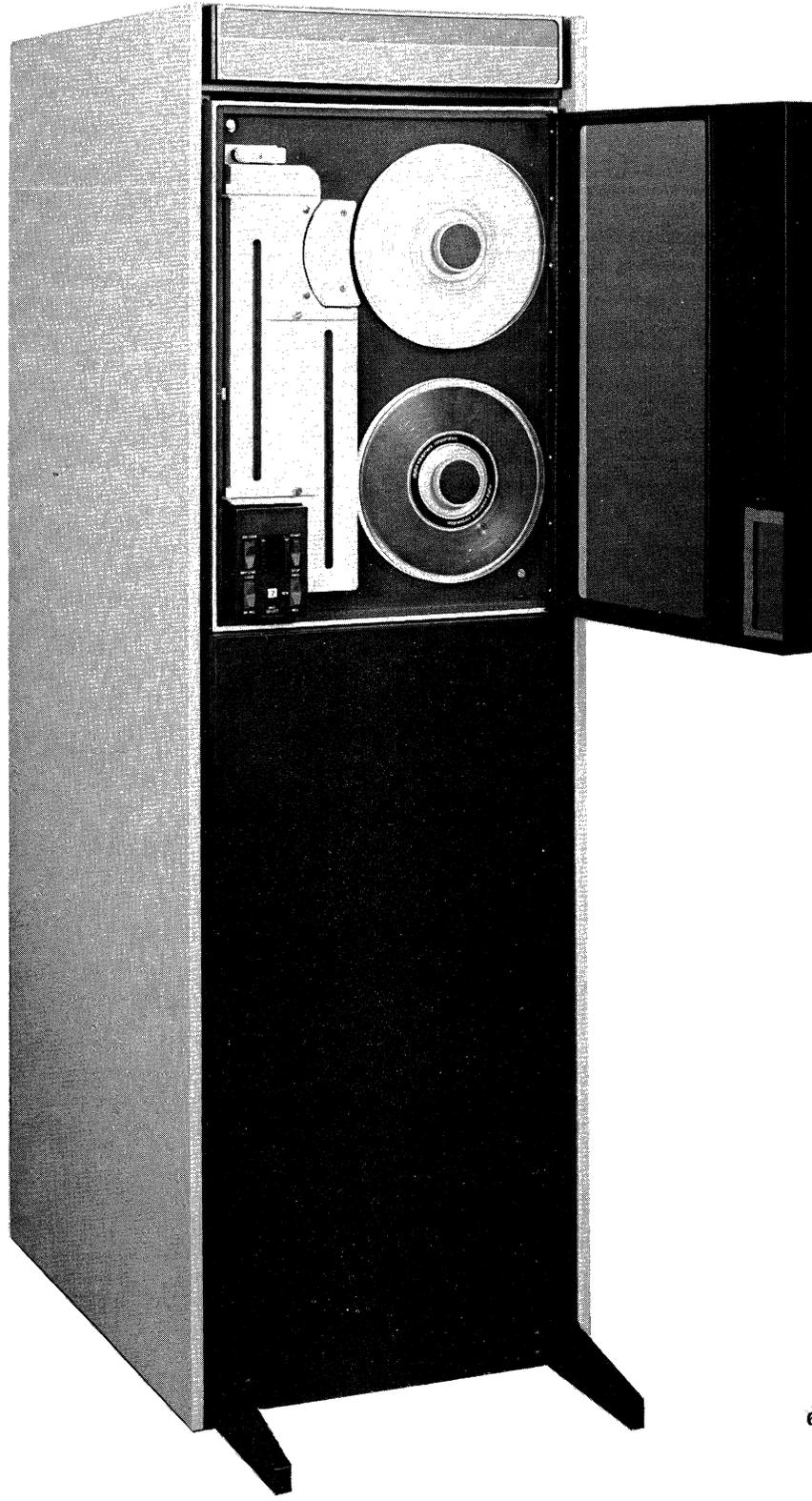
6999-2

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The TU16/TM02 is a Massbus-compatible, versatile tape drive system, consisting of a TM02 Tape Controller and TU16 Tape Transport(s). The TU16/TM02 records and reads digital data in industry standard PE or NRZ mode at a maximum data transfer rate of 72,000 tape characters per second. Tape density and tape character format are program selectable. Forward/reverse tape speed is 45 in./sec, while rewind is performed at 150 in./sec. The TU16/TM02 Tape Drive System also has forward and reverse read/space capability.

1.2 OPTIONS

Table 1-1 lists options available in the TU16 Tape Transport and the TM02 Tape Controller.

Table 1-1
TU16 and TM02 Options

Unit	Desig-nation	Data Features	Power Requirement
TU16	EE	9-track	115 Vac at 60 Hz
	EF	9-track	230 Vac at 60 Hz
	EH	9-track	115 Vac at 50 Hz
	EJ	9-track	230 Vac at 50 Hz
TM02	CA	18-bit/PE/NRZ	115 Vac at 50/60 Hz
	CB	18-bit/PE/NRZ	230 Vac at 50/60 Hz
	FA	16-bit/PE/NRZ	115 Vac at 50/60 Hz
	FB	16-bit/PE/NRZ	230 Vac at 50/60 Hz
	FC	16-bit/NRZ	115 Vac at 50/60 Hz
	FD	16-bit/NRZ	230 Vac at 50/60 Hz

1.3 SPECIFICATIONS

Table 1-2 contains operational, environmental, mechanical, and electrical specifications for the TU16/TM02 Tape Drive System.

1.4 REFERENCE DOCUMENTS

The following documents should be available to the user:

TU16/TM02 Engineering Drawing Set

Massbus Controller Maintenance Manual

861-A, B, C Power Controller Maintenance Manual (EK-861AB-MM-002)

H740D Power Supply Maintenance Manual (DEC-11-H740A-A-D)

Other useful documents include:

Recorded Magnetic Tape for Information Interchange (800 CPI, NRZI, ANSI Document No. X3.22-1973)

Recorded Magnetic Tape for Information Interchange (1600 CPI, PE, ANSI Document No. X3.39-1973)

1.5 MAJOR ASSEMBLIES

Figure 1-1a shows the location of the following major assemblies of the TU16/TM02 Tape Drive System:

- TU16 Tape Transport — Transfers digital data to and from magnetic tape, as commanded by the TM02 Tape Controller.

- TM02 Tape Controller Logic Assembly — The TM02 controls the tape motion and read/write operations of the TU16 Tape Transport. It also converts the Massbus data into tape characters, and vice versa, and provides formatting control for data written on and read from tape.

TU16 TAPE
TRANSPORT

TM02
LOGIC
ASSEMBLY

TM02 POWER
SUPPLY (H740D)

861 POWER
CONTROLLER

6999-9
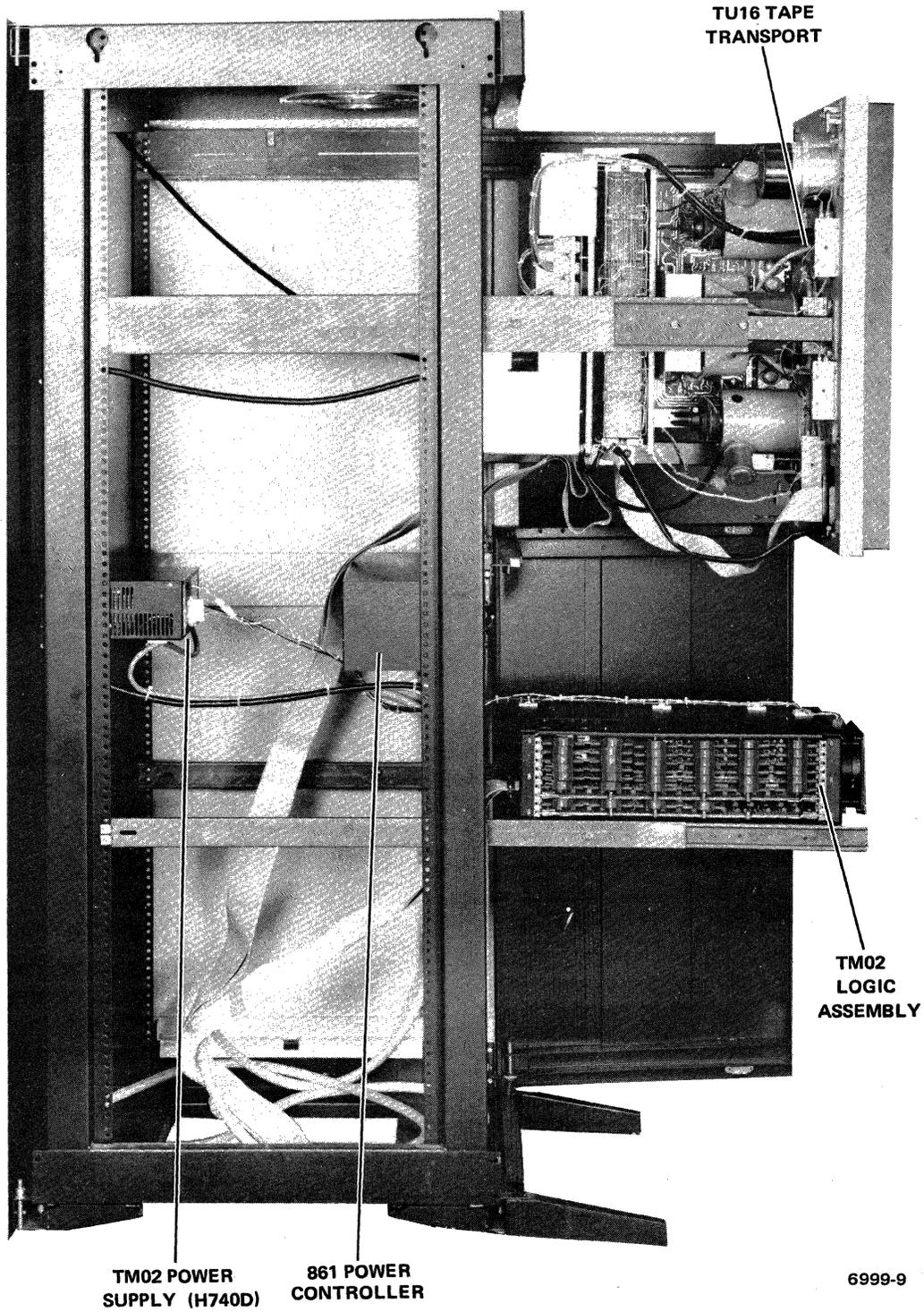
Figure 1-1a   Major Assemblies

Table 1-2
TU16/TM02 Specifications

Parameter	Specification
Packing Density	200, 556, 800, and 1600 bpi; program selectable.
Tape Speed	
Forward/Reverse	45 in./sec (1.14 m/sec)
Rewind	150 in./sec (3.8 m/sec)
Maximum Transfer Rate	72,000 characters/sec
Tape Motion Times	
Start	Normal operating speed is reached within 9 ms after initiation of forward or reverse command.
Stop	Motion stops in less than 8 ms after removal of forward or reverse command.
Electrical Skew	Write deskew only. Read skew mechanically aligned.
Recording Method	NRZI or PE recording; industry-compatible.
Transport Mechanism	Single capstan; vacuum columns.
Read/Write Heads	Dual gap, read after write.
BOT, EOT Detection	Photoelectric sensing of reflective strip.
Interrecord Gap	0.5 in. minimum, 0.65 in. nominal.
Tape	
Width	0.5 in.
Thickness	1.5 mils
Tape Reel	
Diameter	10½ in. (0.27 m)
Capacity	2400 ft
Power Control	861 Power Controller
Voltage Requirement	115/230 Vac ±10% at 50/60 Hz ± 2%
Power Dissipation	920 VA maximum
Physical Parameters	
TU16 Transport (without cabinet)	
Depth	25 in. (0.64 m)
Width	19 in. (0.48 m)
Height	26 in. (0.66 m)
Weight	150 lb (70 kg)
TM02 Tape Controller	
Depth	23 in. (0.58 m)
Width	19 in. (0.48 m)
Height	5¼ in. (0.13 m)
Weight	25 lb (11.25 kg)

Table 1-2 (Cont)
TU16/TM02 Specifications

Parameter	Specification
TM02 Power Supply	
Depth	8-1/8 in. (0.21 m)
Width	19 in. (0.48 m)
Height	5 in. (0.13 m)
Weight	20 lb (9 kg)
861 Power Controller	
Depth	8 in. (0.20 m)
Width	19 in. (0.48 m)
Height	5 in. (0.13 m)
Weight	10 lb (4.54 kg)
Environmental Limits	
Temperature	60° to 90° F (15° to 32° C)*
Relative Humidity	20 to 80% (no condensation)*

*Magnetic tape operation is more reliable if the temperature is limited to 65° to 75° F (18° to 24° C) and the relative humidity to 40 to 60%.

- TM02 Power Supply (H740D) — Provides the ac and dc power required by the TM02 logic assembly.

- 861 Power Controller — Controls power in the TU16/TM02 cabinet.

NOTE
Only TU16/TM02 master cabinets contain the TM02 logic assembly and power supply. TU16 slaves are controlled by the TM02 in the master cabinet.

Figure 1-1b depicts TU16 subassemblies referenced elsewhere in this chapter.

1.6 SYSTEM CONFIGURATION
Figure 1-2 illustrates a TU16/TM02 Tape Drive System configuration. Each TM02 can control up to eight slave TU16 Tape Transports. In turn, each Massbus Controller can control up to eight TM02 Tape Controllers. Thus, a maximum of 64 TU16 Tape Transports could be interfaced to a Massbus Controller.

1.7 TU16 OPERATING INSTRUCTIONS

1.7.1 Controls and Indicators
The operator control box (Figure 1-3) is located at the left of the file reel. The functions of the control box switches and indicators are listed in Tables 1-3 and 1-4.

1.7.2 Operating Procedures

1.7.2.1 Application of Power

1. If the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch is in the REMOTE ON position, TU16/TM02 power is controlled by the processor POWER key switch. This method is used in normal operation.

2. If the processor POWER key switch is not activated, TU16/TM02 power may be turned on locally by setting the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch to LOCAL ON. This method may be used during maintenance.

1.7.2.2 Loading and Threading Tape — Use the following procedure to mount and thread magnetic tape.

1. Apply power to the transport. Place LOAD/BR REL switch to center position.

2. Place a write enable ring in the tape reel groove if data is to be written on the tape. Ensure that there is no ring in the groove if data on the tape is *not* to be erased or written over.

3. Mount the file reel onto the lower hub, with the groove facing toward the back (away from the operator). Ensure that the reel is firmly seated against the flange of the hub and that the reel hub is securely tightened by hand. To tighten the reel hub, turn it clockwise. Do not grip reel by outer flanges. Ensure that brakes are on while tightening the hub.

1-4

CAPSTAN

VACUUM DOOR
(OPEN)

TAPE CLEANER

HEAD PLATE ASSEMBLY
(COVER REMOVED)

EOT/BOT
ASSEMBLY

CONTROL
PANEL

7660-22

H606 POWER BOARD

BRAKE ASSEMBLY

VACUUM ASSEMBLY

TU16 POWER SUPPLY
REGULATOR BOARD

BRAKE ASSEMBLY

LOGIC BACKPLANE
ASSEMBLY

TRANSFORMER-CAPACITOR
ASSEMBLY (P/O TU16
POWER SUPPLY)

TACHOMETER

AIR FILTER

CAPSTAN MOTOR

TAKE-UP REEL MOTOR

VACUUM SWITCHES

FILE REEL MOTOR

VACUUM SWITCHES

READ/WRITE
INTERLOCK

AIR FILTER

6999-8

Figure 1-1b   TU16 Tape Transport Subassemblies

1-5
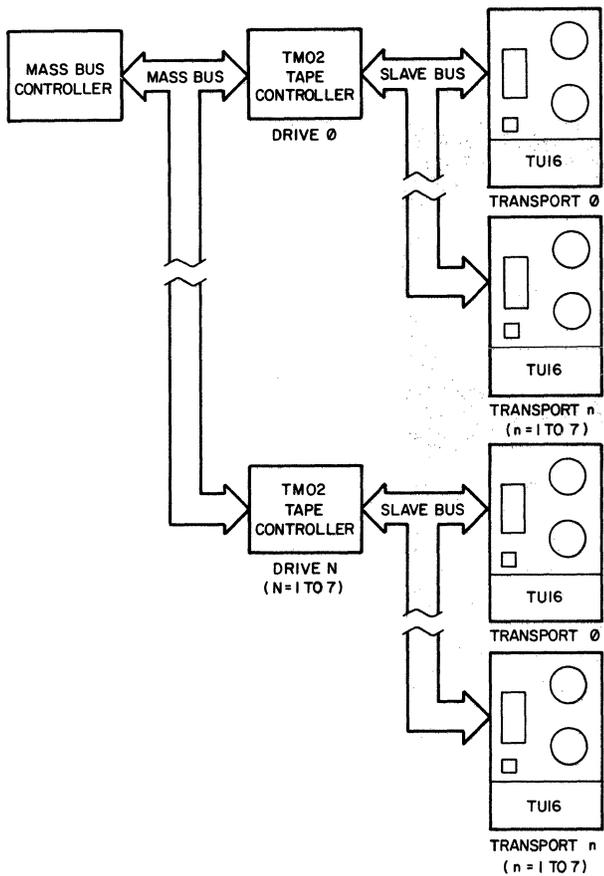
Figure 1-2   TU16/TM02 Tape Drive System
Configuration   10-1266
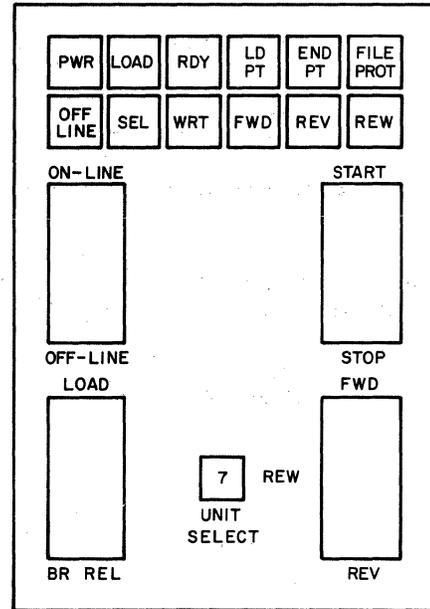
Figure 1-3   Operator Control Box

Table 1-3
TU16 Control Box Switches

Switch	Function
LOAD/BR REL	
LOAD position	Enables vacuum motor, which draws tape into the buffer columns.
Center position	Disables vacuum motor; brakes are full on.
BR REL position	Releases brakes.
ON-LINE/OFF-LINE	
ON-LINE position	Selects remote operation.
OFF-LINE position	Selects local operation.
FWD/REW/REV	
FWD position	Selects, but does not initiate, forward tape motion when transport is off-line.
REW position	Selects, but does not initiate, tape rewind when transport is off-line.
REV position	Selects, but does not initiate, reverse tape motion when transport is off-line.
START/STOP	
START position	Initiates tape motion selected by FWD/REW/REV switch when transport is off-line.
STOP position	Clears any motion commands when transport is off-line.
UNIT SELECT (plug activated)	Selects the tape transport unit by number (0 - 7); this number is used in the program to address the tape transport (slave address).

Table 1-4
Status Indicators

Indicator	Function
PWR	Indicates power has been applied to the transport.
LOAD	Indicates the vacuum is on and the tape is loaded into the buffer columns.
RDY	Indicates that the tape transport is ready (vacuum on and settle-down delay complete); no tape motion.
LD PT	Indicates that the tape is at load point (beginning of tape — BOT).
END PT	Indicates that the tape is at end point (end of tape — EOT).
FILE PROT	Indicates that write operations are inhibited because the write enable ring is not mounted on the file reel.
OFF-LINE	Indicates local operation by the control box.
SEL	Indicates the tape transport is selected by the controller (program).
WRT	Indicates that a write operation has been initiated.
FWD	Indicates that a forward command has been issued.
REV	Indicates that a reverse command has been issued.
REW	Indicates that a rewind command has been issued.

4. Install the take-up reel (at the top) using the same procedure used in step 3.

5. Place the LOAD/BR REL switch in the BR REL position.

6. Manually unwind tape from the file reel and thread the tape by the tape guides and head assembly as shown in Figure 1-4.

7. Wind about four turns of tape onto the take-up reel. Ensure that the tape is in the guides.

8. Place the LOAD/BR REL switch to the LOAD position to draw tape into the vacuum columns.

9. Select FWD and press START to advance the tape to the load point. When the BOT marker is sensed, tape motion stops, the FWD indicator goes out, and the LD PT indicator comes on.

NOTE
If tape motion continues for more than 10 sec, it is possible that originally too much tape was wound by hand onto the take-up reel, covering the BOT marker. If this happens, press STOP, select REV (reverse), and press START. The tape should move to the BOT marker (load point) and stop. Once BOT is sensed, you may continue.

1.7.2.3 Unloading Tape — Different procedures are used to unload tapes, depending on whether or not the tape is at BOT.

Unloading Tape at BOT — To unload a tape which is at the BOT marker, perform the following procedure:

1. Place the LOAD/BR REL switch in the BR REL position to release the brakes.

2. Gently hand wind the file reel (lower) in a counterclockwise direction until all of the tape is wound onto the reel.

CAUTION
When winding the tape by hand, do not jerk the reel. This can stretch or compress the tape, which could cause irreparable damage.

3. Remove the file reel from the hub assembly. Turn the hub counterclockwise to loosen it.

Unloading Tape Not At BOT — To unload a tape which is not at the BOT marker, perform the following procedure:

1. Place the ON-LINE/OFF-LINE switch in the OFF-LINE position.

2. Press STOP; select REW.

1-7

TAKE-UP REEL
(UPPER MOTOR)

TAPE GUIDES (2)

CAPSTAN

HEAD TAPE GUIDES (2)

R/W ERASE
HEAD ASSEMBLY

TAPE MOVES INTO BOTH
VACUUM COLUMNS
WHEN "LOAD" SWITCH
IS PRESSED

TAPE PATH
WHEN LOADING

FILE REEL
(LOWER MOTOR)

10-1308
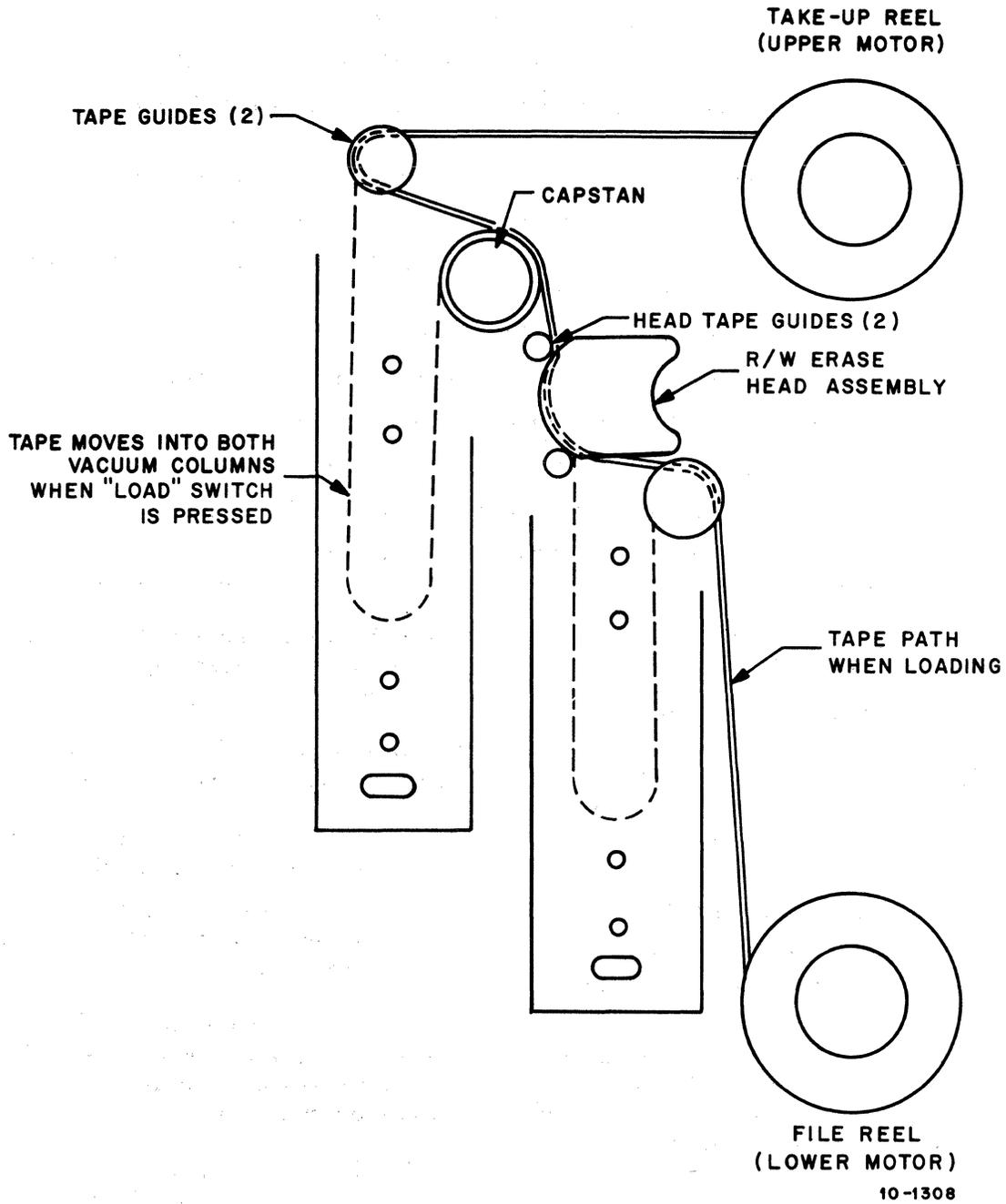
Figure 1-4   Tape Loading Path

3. Press START. The tape should rewind until the BOT marker is reached.

4. Place the LOAD/BR REL switch in the BR REL position to release the brakes.

5. Gently hand wind the file (lower) reel in a counterclockwise direction until all of the tape is wound onto the reel.

CAUTION
When winding the tape by hand, do not jerk the reel. This can stretch or compress the tape, which could cause irreparable damage.

6. Remove the file reel from the hub assembly. Turn the hub counterclockwise to loosen it.

1.7.2.4 Restart After Power Failure — In the event of a power failure, the TU16 automatically shuts down and tape motion stops without physical damage to the tape. However, if the TU16 was on-line and was either reading or writing at the time of the power failure, the last record was probably lost; refer to system recovery procedures documentation if this happens. To restart the transport, proceed as follows:

NOTE
Return of power is indicated when the PWR indicator lights.

1. Set the ON-LINE/OFF-LINE switch to OFF-LINE.

2. Place the LOAD/BR REL switch in the BR REL position to release the brakes.

3. Manually wind the reels to take up any slack in the tape.

4. Set the LOAD/BR REL switch to the LOAD position to draw tape back into vacuum columns.

5. Set the ON-LINE/OFF-LINE switch to the desired position.

1.7.2.5 Restart After Fail-Safe — If the tape loop in either buffer column exceeds the limit shown in Figure 1-5, the vacuum system automatically shuts down and tape motion stops without damage to the tape. When this fail-safe condition occurs, the TU16 does not respond to either on-line or off-line commands. To restart the transport, refer to Paragraph 1.7.2.4.
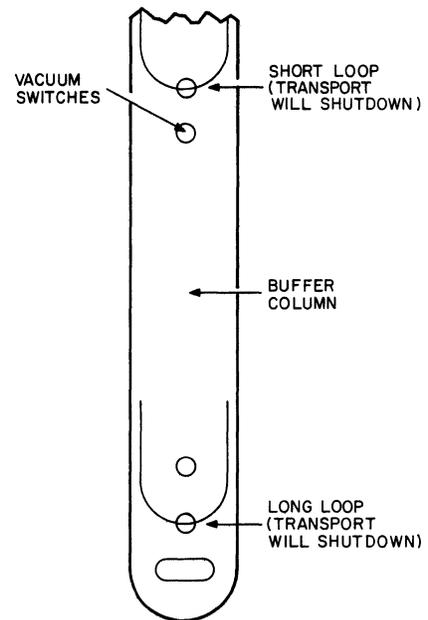
Figure 1-5   Fail-Safe Limits

1.7.3 Operator Troubleshooting
Before any maintenance personnel are called to correct a problem, the operator can make several checks with minimal effort. These precautions may isolate an easily correctable error:

1. Ensure that the vacuum door (Figure 1-1b) is closed and sealed properly.

2. If the tape does not stop at BOT, be certain the tape does have a BOT marker on it.

3. Ensure that the write enable ring is inserted in the tape reel if a write operation is to be performed.

4. Clean the tape path according to the daily (8-hour) preventive maintenance procedures (Paragraph 5.2).

1.7.4 Tape Handling

WARRANTY
Removable media involve use, handling, and maintenance which are beyond DEC's direct control. DEC disclaims responsibility for performance of the equipment when operated with media not meeting DEC specification/ or with media not maintained in accordance with procedures approved by DEC. DEC shall not be liable for damages to the equipment or to media resulting from such operation.

1-9

The operator should observe the following precautions when handling magnetic tape:

1. Always handle a tape reel by the hub hole; squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

2. Never touch the portion of tape between the BOT and EOT markers. Oil from fingers attracts dust and dirt. Do not allow a tape end to drag on the floor.

3. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and can affect tape transport operation.

4. Always store tape reels inside their respective containers. Keep empty containers closed so dust and dirt cannot get inside.

5. Inspect tapes, reels, and containers for dust and dirt. Replace damaged take-up reels.

6. Do not smoke near the transport or tape storage area. Tobacco smoke and ash are especially damaging to tape.

7. Do not place the TU16 Tape Transport near a line printer or other device that produces paper dust.

8. Clean the tape path frequently, as described in Paragraph 5.2.

1.8 MAGNETIC TAPE FUNDAMENTALS — DEFINITIONS

1. Reference Edge — The edge of the tape as defined by Figure 1-6. For tape loaded on a TU16, the reference edge is toward the observer.

2. BOT (Beginning Of Tape) Marker — A reflective strip placed on the nonoxide side of the tape, against the reference edge, 15 feet (± 1 ft) from the beginning of the tape.

3. EOT (End Of Tape) Marker — a reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 25 to 30 feet from the trailing edge of the tape.

4. Nine-Channel Recording — Eight tracks of data plus one track of vertical parity. Figure 1-7 shows the relationship between track and bit weight for a nine-channel transport.

5. Tape Character — A bit recorded in each of the nine channels.

6. Record — A series of consecutive tape characters.

7. File — An undefined number of records (minimum = zero, no maximum).

8. Interrecord Gap (IRG) — A length of erased tape used to separate records (0.5 in. minimum for nine-track; maximum IRG is 25 ft).

9. Extended IRG — A length of erased tape (3 in. minimum) optionally used to separate records. It must be used between BOT and the first record.

10. Tape Speed — The speed at which tape moves past the read/write heads; normally stated in inches per second.

11. Tape Density — The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi). This is equivalent to characters per inch (cpi), since 800 bpi means that there are 800 tape characters per inch of tape.

Figure 1-6 Reference Edge of Tape
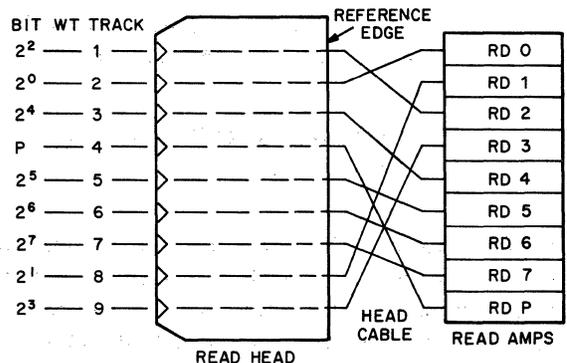
Figure 1-7 Track-Bit Weight Relationship for Nine-Channel Transport
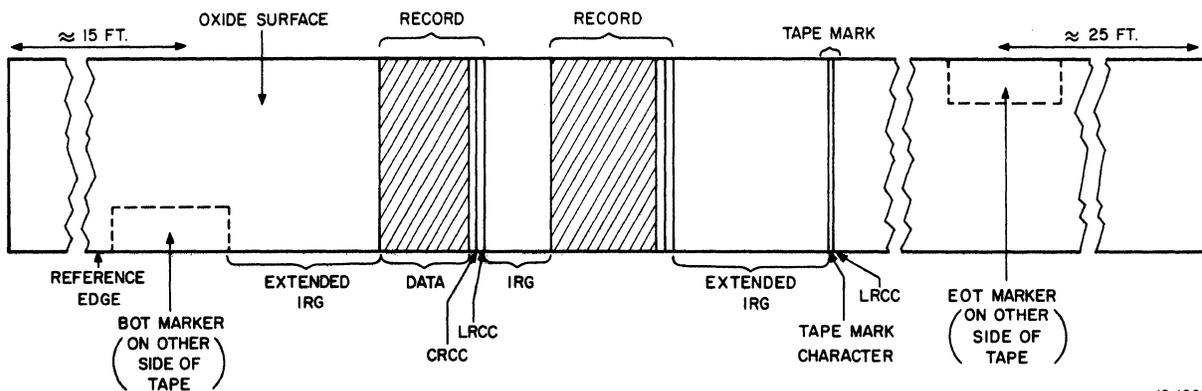
Figure 1-8   NRZ Format (Nine-Channel)

12. **Write Enable Ring** — A rubber ring which must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.

13. **Tape Mark (TM)** — A record written on the tape to designate the end of a file; sometimes referred to as a file mark (FMK). In the TU16/TM02, the tape mark is always preceded by an extended IRG.

1.9   TU16/TM02 RECORDING TECHNIQUES

1.9.1   NRZI (Non-return to Zero — Change on a 1)

1.9.1.1   Definition — NRZI is a recording technique which requires a change of state (flux change) to write a 1, and no change of state (no flux change) to write a 0.

1.9.1.2   Format —

Cyclic Redundance Check Character (CRCC) — A check character that is written four character spaces after the last character of a NRZ record (nine-channel only). CRCC is derived by a complex mathematical formula applied to the characters written in the record. The result of this manipulation (CRCC) can be used to recover a lost bit in a record read from tape.

Longitudinal Parity Check Character (LRCC) — A check character written four character spaces after CRCC (nine-channel). LRCC consists of one bit of even parity for each track of data. For example, if track 1 had an odd number of 1s written in a record, then a 1 must be written in the LRCC bit associated with track 1.

Tape Mark — A nine-channel NRZ tape mark consists of one tape character (23_8), followed by seven blank spaces, and then LRCC (23_8). (CRCC is not written.) Figure 1-8 illustrates nine-channel NRZ tape format.

1.9.2   PE (Phase Encoding)

1.9.2.1   Definition — Phase encoding is a recording technique in which a flux reversal occurs for each bit of information written on the tape. A 1 can be defined as a positive level followed by a negative transition, while a 0 can be defined as a negative level followed by a positive transition.

Sequential flux transitions on the tape are either at the data rate or at twice the data rate. Sequential 1s or sequential 0s will cause flux reversals to occur at twice the data rate:
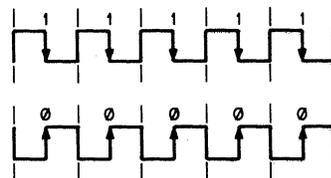
Waveform   10-1271

Alternate 1s and 0s cause flux reversals to occur at the data rate:

10-1269

Waveform

1-11
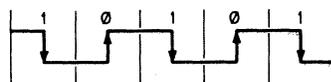
1.9.2.2 Format — To ensure proper extraction of PE data from the serial stream of transitions coming off the tape, PE data must be recorded in a precise format. A PE record consists of *preamble, data,* and *postamble.*

a. *Preamble* — Forty characters of 0s in all nine tracks, followed by a character of 1s in all nine tracks.

b. *Postamble* — One character of 1s in all nine tracks, followed by 40 characters of 0s in all nine tracks.

The PE read electronics uses a *data window* to isolate data transitions. For example,
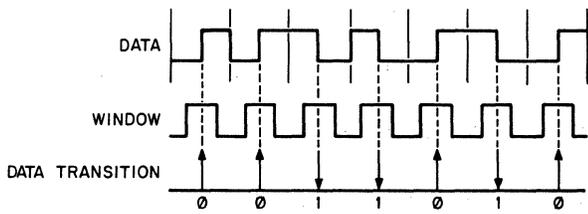
Waveform

Zeros in the preamble are used to set the window in position when reading in a forward direction, while 0s in the postamble perform this function when reading in the reverse direction. The all-1s character in the preamble and postamble is used to mark the beginning of data.

Tape Mark — A PE tape mark consists of forty 0s in tracks 2, 5, and 8 (bit positions 0, 5, and 1) with tracks 3, 6, and 9 (bit positions 4, 6, and 3) erased.

Identification Burst (IDB) — The IDB identifies the tape as being a PE tape. It consists of alternating 1s and 0s in the parity track (track 4) with all other tracks erased. The IDB is located at BOT, and has a minimum length of 1.7 in. Figure 1-9 illustrates PE tape format.
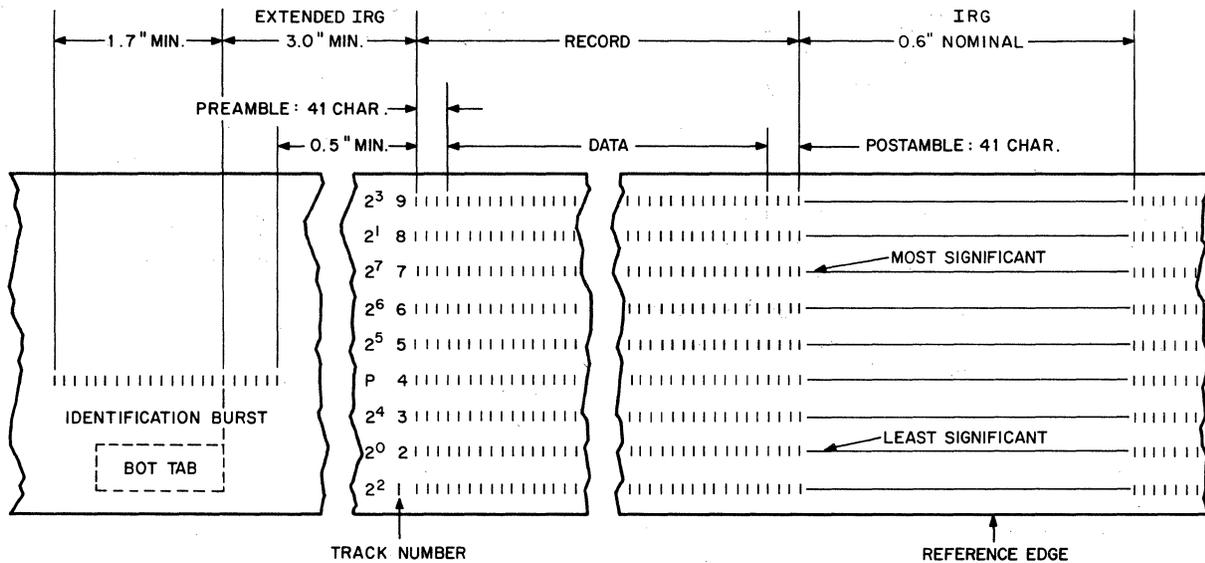
Figure 1-9   PE Recording Format

1-12

CHAPTER 2
THEORY OF OPERATION

2.1 INTRODUCTION

The TU16/TM02 Tape Drive System (Figure 2-1) interfaces with the central processor (CPU) via the Massbus Controller. However, the Massbus Controller is almost transparent to the CPU, and the CPU operates as though it were controlling the drive directly.

The TU16/TM02 interfaces with the Massbus Controller via the Massbus. The Massbus consists of an asynchronous control bus with its associated control lines, and a synchronous data bus with its associated control lines. Transactions on the control bus control the TU16/TM02 and determine its status, while transactions on the data bus transfer data to or from the TU16/TM02. Because the data and control buses operate independently, the Massbus Controller can monitor drive status while a data transfer operation is being performed. Table 2-1 lists the Massbus interface signals and their functions.

The TM02 can control up to eight TU16 Tape Transports via the slave bus. All TU16s controlled by a TM02 are "daisy-chained" on the slave bus (Figure 1-2). Essentially, this means that the TU16s are configured parallel to each other. The slave bus consists of slave (TU16) select lines, write data lines, read data lines, transport control lines, and various TU16 status lines. Table 2-2 lists the slave bus interface signals and their functions. Figure 2-2 shows the Massbus and slave bus signals connecting the TM02, TU16, and Massbus Controller.

2.2 SYSTEM OPERATION

Figure 2-3 is a block diagram of the TU16/TM02, and shows the major functional groups, control lines, and data paths. The following paragraphs describe these functional groups.
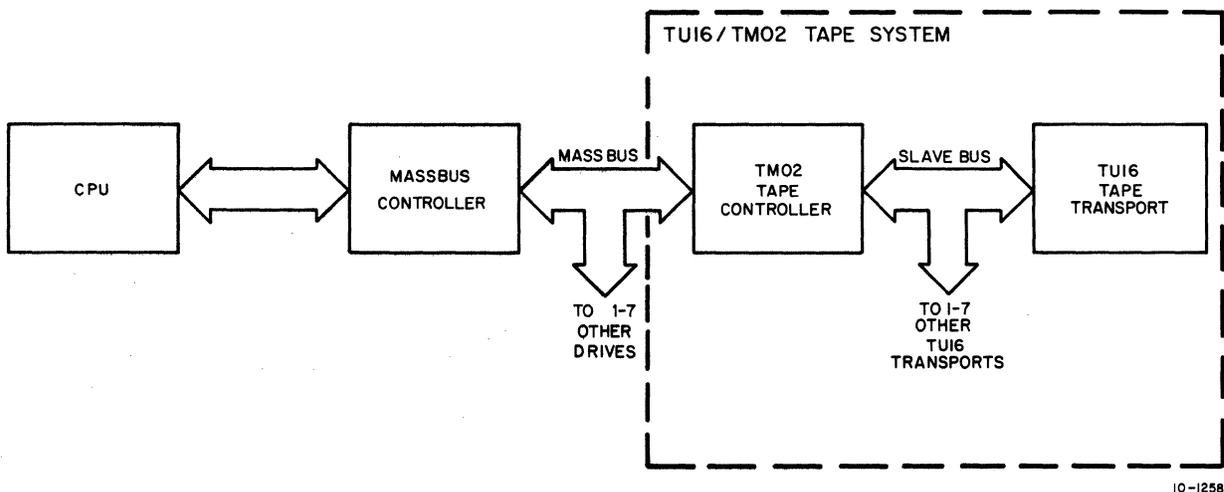
Figure 2-1   TU16/TM02 in a System Configuration

Table 2-1
Massbus Interface Signals

Signal	Function
Data Bus	
Data Lines [D(0:17)]	These bidirectional lines transmit 18 parallel data bits to or from the TM02.
Data Lines Parity (DPA)	This bidirectional line transmits the data parity bit (odd parity) to or from the TM02. Data parity is simultaneously transmitted with the bits on the Data lines.
Sync Clock (SCLK)	During a data write, this line transmits SCLK from the TM02 to request write data from the Massbus Controller. During a data read, this line transmits SCLK to the Massbus Controller to indicate that read data is present on the Data lines.
Write Clock (WCLK)	During a data write, this line transmits WCLK from the Massbus Controller to strobe write data into the TM02.
Run (RUN)	This line transmits RUN from the Massbus Controller to initiate data transfer execution.
End of Block (EBL)	Normally, this line transmits EBL from the TM02 at the end of each record. However, for certain abnormal conditions where it is necessary to terminate the transport operation immediately, EBL is transmitted prior to the end of the record.
Exception (EXC)	This bidirectional line transmits EXC from the TM02 to indicate that an error has occurred during data transfer. In some systems, EXC H can also be transmitted over this line from the controller to abort an in-progress data transfer.
Occupied (OCC)	During a data transfer (read/write), this bidirectional line transmits OCC from the TM02 to indicate that a transport has control of the data bus. Once asserted, this signal prevents any other transport from using the data bus.
Control Bus	
Control Lines [C(0:15)]	These bidirectional lines transmit 16 parallel control or status bits to or from the TM02.
Control Lines Parity (CPA)	This bidirectional line transmits control lines parity (odd parity) to or from the TM02. Control parity is simultaneously transmitted with the bits on the Control lines.
Drive Select [DS(0:2)]	These three lines transmit a three-bit binary code from the Massbus Controller to select a particular drive.
Register Select [RS(0:4)]	These five lines transmit a five-bit binary code from the Massbus Controller to select one of the ten TM02 registers.
Controller to Drive (CTOD)	This line transmits the CTOD signal from the Massbus Controller to indicate in which direction data is to be transferred on the Control lines. For a controller-to-drive transfer, the controller asserts CTOD. Conversely, for a drive-to-controller transfer, the controller negates CTOD.
Demand (DEM)	This line transmits DEM from the Massbus Controller to initiate a control bus transfer (initiate "handshake").
Transfer (TRA)	This line transmits TRA from the TM02 in response to DEM. The assertion of TRA indicates that data is available on the Control Bus.

Table 2-1 (Cont)
Massbus Interface Signals

Signal	Function
Attention (ATTN)	This line transmits ATTN from the TM02 to indicate that a nontransfer error or transport status change has occurred.
Initialize (INIT)	This line transmits INIT from the Massbus Controller to initialize all TM02s and transports on the daisy chain. INIT is transmitted at system start-up or whenever the Massbus Controller issues an Initialize command.
Massbus Fail (MASSFAIL)	This line transmits MASSFAIL L negated from the Massbus Controller to indicate that the controller power supply is operating properly. If the controller power supply fails, MASSFAIL L is asserted, thus initializing the TM02 logic as well as preventing it from accepting erroneous control bus information.

Table 2-2
Slave Bus Interface Signals

Slave Bus Signal	Function
Slave Select [SS(0:2)]	These lines select one out of eight possible TU16 Transports for command execution.
Forward (FWD) Reverse (REV) Rewind (RWND) Write Enable (WRITE)	These are the four command lines which determine TU16 operation.
Slave Set Pulse (SLAVE SET PLS)	This signal initiates TU16 response to the four command lines.
Stop (STOP)	This signal causes the TU16 to terminate motion. (Does not apply to rewind, which terminates independently.)
Enable Motion Delay (EMD)	This signal enables the TU16 to gate out a coded motion delay preset onto the read lines.
Accelerate (ACCL)	Asserted by the TM02 while the transport is getting up to speed or not moving tape. Not asserted while the IDB is being written.
Write Data [WD(0:7, P)]	These nine lines transmit data to be written by the TU16.
Record (REC)	A pulse that causes data to be written on tape.
Density Select [DEN(0:2)]	These three lines control the density at which data is written on tape. They must also represent the density of tape data during a read operation.
Clock (CLOCK)	A 144-kHz clock generated in the TU16, present at all times when the unit is on-line.
Write Clock (WRT CLK)	This clock is transmitted to the TM02 by a powered, on-line TU16 loaded with tape when it is running at speed (ACCL not asserted). The frequency of WRT CLK is a function of the DEN lines, and controls the write timing frequency.
LRC Strobe (LRC STRB)	Asserted by the TM02 prior to the REC pulse that writes the LRC character.
Read Data [RD(0:7, P)]	These nine lines transmit read data from the TU16 to the TM02. (They also transmit the motion delay preset.)

Table 2-2 (Cont)
Slave Bus Interface Signals

Slave Bus Signal	Function
Read Strobe Delay Over (RSDO)	A Read Strobe pulse generated by the transport at the end of the skew delay in NRZ mode.
Set Vertical Parity Error (SET VPE)	Asserted by the TU16 during a write or interchange read operation when data violates the skew window.
Beginning of Tape (BOT)	Asserted when the TU16 detects the beginning-of-tape marker.
End of Tape (EOT)	Asserted when the TU16 detects the end-of-tape marker.
Rewind Status (RWS)	Asserted while the selected TU16 is performing a rewind operation.
7-Channel (7 CH)	Always negated by a selected TU16.
Slave Present (SPR)	Asserted by a selected, powered TU16.
Medium On-Line (MOL)	Asserted by a selected, powered TU16 which is loaded with tape.
Tape Unit Ready (TUR)	Asserted by a selected TU16 to indicate that tape motion has stopped.
Settle Down (SDWN)	Asserted while the transport is decelerating, until it has stopped.
Phase Encoded Status (PES)	Asserted by a TU16 when instructed to operate in PE mode (DEN 2 asserted).
Slave Attention (SLA)	Asserted by a TU16 when it comes on-line.
Set Slave Status Change (SET SSC)	Asserted at the completion of a rewind or when the unit comes on-line. It is also pulsed when the transport goes off-line or when the TU16 power fails. This line may be asserted by any slave, selected or not.
Write Lock (WRL)	Asserted when the selected TU16 detects that the write enable ring has been removed from the tape reel.
Interchange Read (IRD)	A maintenance function. When asserted in NRZ mode, skew delays are tightened; in PE mode, on-the-fly error correction is inhibited.
Drive Type (DT)	In the TU16, these three bits are always asserted as follows: DT0 1 DT1 0 DT2 0
Serial Number [SN(0:15)]	These 16 lines contain the BCD code of the last four digits of the serial number of the selected TU16.
Drive Clear Pulse (DRV CLR PLS)	When asserted by the TM02, DRV CLR PLS clears SLA in the selected slave.
Initialize Pulse (INIT PLS)	When asserted by the controller, INIT PLS L clears SLA and terminates tape motion (except rewinds) in all on-line transports.
+5 V	The TM02 supplies this voltage to power the slave bus terminator networks.
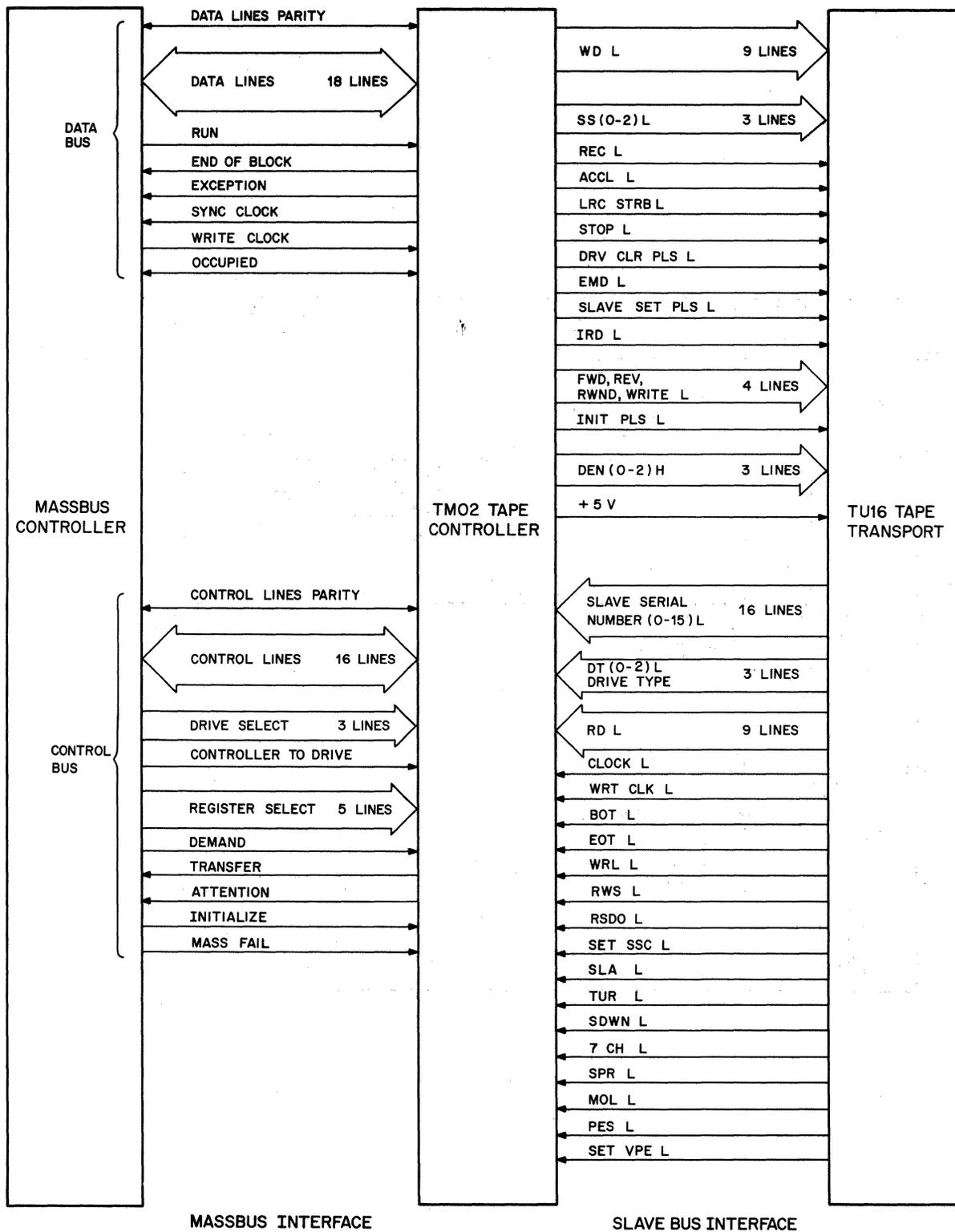
Figure 2-2   Interface Signals
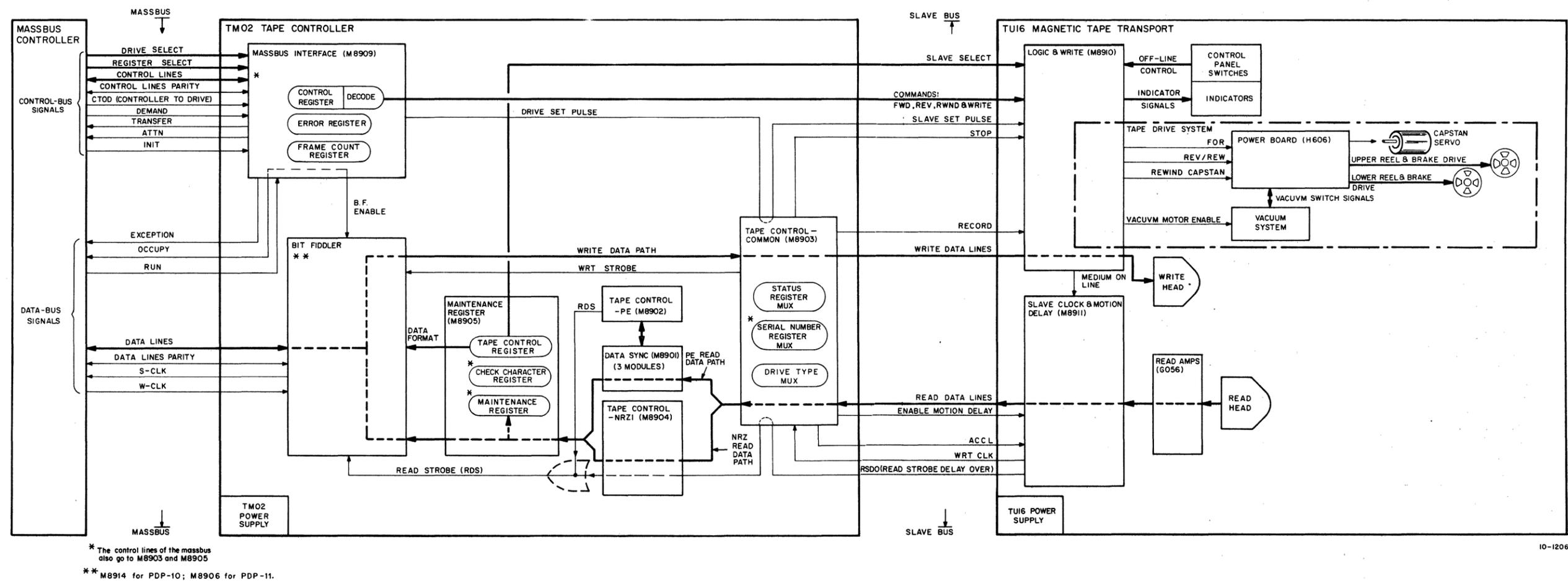
Figure 2-3 TU16/TM02 Block Diagram

2.2.1 Massbus Interface (M8909)

The Massbus Interface interfaces the TU16/TM02 with the Massbus Controller. It contains circuitry which decodes the Drive Select signals on the Massbus. If enabled by the proper Drive Select address code, the Massbus Interface can carry on the "handshake" operations with the Massbus Controller, which read and write TM02 registers. The most important of the TM02 registers (Control register) is located in the Massbus Interface. The Massbus Controller writes the function code of the next operation to be performed into the Control register. The Massbus Interface decodes this register and generates the appropriate control signals (FWD, REV, RWND, WRITE) to control the TU16 and various TM02 functions.

The Massbus Interface contains several other registers: the Error register and Attention Summary register can be read by the Massbus Controller to determine TU16/TM02 status; the Frame Count register may also be read by the Massbus Controller to determine TU16/TM02 status, and is critical for proper operation of the tape drive. The Frame Count register must be loaded prior to a space or write operation with the number (in 2s complement form) of records to be spaced or tape characters to be written. This register is incremented as the operation proceeds, and will terminate the operation with register overflow.

The Massbus Interface decodes the Control register to determine that a data transfer operation is to be performed. When this is the case, it generates OCC on the Massbus to notify the controller and other drives that it has occupied the data bus, and enables the Bit Fiddler.

2.2.2 Bit Fiddler

The Bit Fiddler interfaces the TU16/TM02 data paths to the Massbus Controller; it contains circuitry that performs synchronous data transfers on the data bus of the Massbus.

The Bit Fiddler is enabled for operation by the Massbus Interface with BF ENABLE H. The mode of Bit Fiddler operation is determined by control lines: FMT 0—3 (tape character format), WRITE H (direction of the transfer, i.e., read or write), and FWD H (direction of tape motion, i.e., forward or reverse). WRITE H and FWD H are decodes of the Control register function bits. FMT 0—3 are the Tape Control register format bits, and are decoded in the Bit Fiddler.

During a write operation, the Massbus Controller places an 18-bit data word on the data bus. When the Bit Fiddler is ready to accept this data word, it issues

SCLK (Sync Clock) to the controller, which replies with WCLK (Write Clock).

Upon receiving WCLK, the Bit Fiddler strobes in the word on the data bus, performs a data bus parity check, and begins disassembling the 18-bit data word into 8-bit characters. (Vertical parity bits are added at a later stage.) After generating WCLK, the controller places the next data word on the data bus. When the Bit Fiddler has finished disassembling the previous data word, it issues another SCLK, receives another WCLK, and strobes in the next data word for disassembly. The process continues until all the data has been transferred (precluding occurrence of data errors or other failures).

During a read operation, the Bit Fiddler assembles 8-bit characters into 18-bit data words. When the 18-bit data word has been assembled, it is placed on the data bus along with a parity bit (DPA), and the Bit Fiddler generates an SCLK pulse. When the Massbus Controller receives SCLK, it strobes in the data on the data bus. The Bit Fiddler continues to assemble data characters into 18-bit data words, and notifies the controller that a data word is available by generating SCLK. As in a write operation, the method of assembly is determined by the FMT 0—3, WRITE H, and FWD H signals input to the Bit Fiddler.

2.2.3 Maintenance Register Module (M8905)

The Maintenance Register module is part of the read data path; read data is multiplexed through the Maintenance Register module from the PE or NRZ read circuitry (M8901 or M8904) to the Bit Fiddler. The Maintenance Register module also contains the Tape Control register, the Check Character register, and the Maintenance register. The Tape Control register contains Slave Select bits, which are translated to slave bus signals (SS 0—2) and determine which slave TU16 will perform the operations specified by the Massbus Controller. This register also contains tape data format and density information. Therefore, the Tape Control register must be properly loaded by the Massbus Controller prior to the specification of a particular functional operation.

The Maintenance Register module plays an important role in maintenance mode operation. By writing into the Maintenance register (R03), the Massbus Controller can select one of several maintenance modes. These modes allow:

1. Testing of various TM02 circuits independently of the TU16

2. Testing of the TU16/TM02 under tighter operation criteria.

2.2.4 Tape Control-NRZI Module (M8904)

The Tape Control-NRZI module performs functions relating only to NRZ data storage and retrieval. During an NRZ read operation, the Tape Control-NRZI module is part of the read data path. When informed by the Slave Clock and Motion Delay module that a tape character is available [RSDO L (Read Strobe Delay Over) asserted], the Tape Control-NRZI generates RDS H (Read Strobe) and strobes the tape character from the Tape Control Common Mode module (M8903) into an NRZ Read Latch. The output of the latch, multiplexed through the Maintenance Register module, becomes available to the Bit Fiddler.

During an NRZ read operation, the Tape Control-NRZI module also generates and checks LRCC (Longitudinal Parity Check Character) and CRCC (Cyclic Redundancy Check Character), checks vertical parity, detects tape marks (file marks), and determines that the minimum criteria for normal termination have been met.

During an NRZ write operation, the Tape Control-NRZI module generates the CRCC.

2.2.5 Data Sync-PE Module (M8901)

The Data Sync module (one of three) is part of the PE read data path. It processes PE read data from the Tape Control Common Mode (TCCM) module (M8903), converting the PE information to binary and deskewing the data. It operates with the Tape Control-PE module (M8902) to detect preamble, data, postamble, and TM. It also performs on-the-fly error correction based on Vertical Parity Errors (VPE) detected by the Tape Control-PE module.

The Data Sync-PE module performs no write data path operations. However, it does do a read-after-write during PE write operations.

2.2.6 Tape Control-PE Module (M8902)

During a PE read operation, the Tape Control-PE module (M8902) operates with the Data Sync module to detect preamble, data, postamble, and TM. It also checks for vertical parity errors and PE format errors.

During a PE write operation, the Tape Control-PE module establishes the timing for writing preamble, data, and postamble.

2.2.7 Tape Control Common Mode Module (M8903)

The TCCM module (M8903) contains tape control functions that are used by both PE and NRZ modes. The TCCM module generates clock waveforms used throughout the TM02 from a base clock frequency it receives from the TU16 via the slave bus. It also plays a role in the control of TU16 tape motion and the synchronization of TU16 tape motion to TM02 operations.

When the Control register is loaded with a function code requiring tape motion, the function code is decoded by the Massbus Interface, and a FWD, REV, or RWND signal is applied to the TU16 via the slave bus. Soon after, a DRIVE SET Pulse is generated by the Massbus Interface to initialize TM02 circuitry. DRIVE SET Pulse enters the TCCM module and produces SLAVE SET Pulse and EMD (Enable Motion Delay) — both of which are transmitted to the TU16 Transport via the slave bus. SLAVE SET Pulse sets a motion flip-flop in the Logic and Write (LAW) module (M8910), and thereby initiates tape motion. EMD causes a preset to be applied on the Read Data lines of the slave bus by the Clock and Motion Delay module (M8911), and loads a Motion Delay Counter in the TCCM with the preset. The counter is then upcounted to 2^{14}, at which time ACCL H is negated; the TU16 is now assumed to be up to speed. ACCL negated is transmitted from the TCCM module to various TM02 circuitry, and even to the transport, as notification that the TU16 is at speed. A similar motion delay is generated upon termination of a motion command, in which ACCL H is asserted, and the TCCM issues STOP L to the TU16, causing the transport to cease tape motion.

During a read operation, read data is multiplexed from the slave bus Read Data lines (and the TM02 slave bus receivers), through the TCCM module, to the Data Sync module (for PE) or Tape Control-NRZI module (for NRZ).

During a write operation, data is input to the TCCM module from the Bit Fiddler. The TCCM generates vertical parity bits for the data characters to form nine-bit characters for transfer to tape. The TCCM controls the timing for writing the LRCC and CRCC. It also contains a Write Multiplex and Write Buffer, which:

1. Convert binary characters to PE mode

2. Multiplex 0s and 1s to write PE preambles and postambles

2-8

3. Multiplex the generated CRCC onto the write data path

4. Force IDB (identification burst) and TM (tape mark) character patterns onto the write data path.

Data in the TCCM Write Buffer is output via slave bus drivers to the TU16, along with REC L (SB). REC L (Record) is derived from WRT CLK (SB), generated in the TU16 Clock and Motion Delay module; its frequency depends on the mode (PE/NRZ) and density in which the write operation is performed.

2.2.8 Logic and Write (LAW) Module (M8910)

The LAW module (M8910) interfaces the TM02 Motion Control signals and write data path to the TU16.

Write Data Path — Input to the LAW circuitry of each track is the data line corresponding to that track and a delayed REC pulse. (The delay is prewired and corrects for static write skew errors in the write head itself.) PE write data has been converted from binary to PE mode in the TCCM module. NRZ write data is still in binary mode and is converted to NRZ mode (transition for 1s, no transition for 0s) in the LAW module. The Write Data signals are then applied to the write heads.

Tape Motion — The signals which control the Power Board (H606), which, in turn, controls capstan and tape reel motion, are generated on the LAW module. The LAW module contains motion control flip-flops and various sequencing circuits. The sequencing circuits provide smooth mechanical operation, which protects data and hardware. The flip-flops enable reel motion and vacuum operation, determine the direction and speed of capstan rotation, and light control panel indicators. These flip-flops are controlled by the TM02 via the slave bus when the TU16 is on-line, and by the TU16 control panel when the transport is off-line. When the TU16 is on-line and receives a motion/write command from the TM02, the flip-flop corresponding to that command will be set upon receipt of SLAVE SET Pulse, at which time the motion will commence/ the write amplifiers will be enabled. Receipt of STOP L from the TM02 causes the motion flip-flops to be reset, and the motion terminated.

2.2.9 Slave Clock and Motion Delay Module (M8911)

The Slave Clock and Motion Delay module (M8911) generates clock signals (CLOCK and WRT CLK) used by the TM02. CLOCK is a 144-kHz clock transmitted via the slave bus by a selected, on-line, and powered TU16 loaded with tape. CLOCK is used in the TM02 to generate other clock signals, which perform various housekeeping functions. The frequency of WRT CLK depends on the selected mode (PE/NRZ) and density. It is transitted to the TM02 by a selected, on-line TU16 loaded with tape when it is running at speed. WRT CLK plays a crucial role in the TM02 during read and write operations. The Slave Clock and Motion Delay module also generates presets for the Motion Delay Counter in the TCCM module. The presets are multiplexed onto the slave bus Read Data lines whenever the TU16 receives EMD (Enable Motion Delay) from the TM02.

2.2.10 Read Head and Read Amplifiers

The read head converts changes in magnetic flux on the tape into voltage signals which are then amplified by the Read Amplifiers (G056).

When reading in NRZ mode, the Read Amplifier of each track produces a high output level for each change of magnetic flux on its tape track (Figure 2-7). These levels will be strobed into the TM02 read logic. Zero bits are recognized by no change in flux on a track (i.e., no high level) when at least one other track has flux change. Because of parity conventions, each character on the tape will have at least one flux change on one of the tape tracks.

When reading in PE mode, the Read Amplifier output for each track will coincide with the direction of flux on its track (Figure 2-7). Because of the nature of phase encoding, each track of PE data contains all the information necessary to decode it.

2.2.11 TU16 Power Board

The TU16 Power Board (H606) contains circuits which control and drive the capstan and tape reels. The capstan motor is part of a servo loop, whose inputs are motion signals (FOR, REV/REW, and REWIND CAP) from the LAW module. These motion signals control the direction and speed of the capstan motor, which controls the direction and speed of the tape relative to the heads. The tape reel drives do *not* control tape direction or speed. Their function is to maintain the proper amount of tape in the vacuum columns.

There are two tape reel drive systems, each one operating independently of the other. The upper tape reel drive operates with the upper vacuum column vacuum switches as inputs. When the tape is too high in the column, the switches activate the tape reel motor to supply tape to the column. When the tape is too low in

the column, the tape reel motor is activated to take up tape. The lower tape reel drive operates with the lower vacuum column vacuum switches in an identical manner.

2.3 WRITE DATA PATH
The write data path, shown in the TU16/TM02 block diagram (Figure 2-3), is discussed in this section in greater detail (Figure 2-4)

To write data on tape, the Massbus Controller, after loading the Tape Control register and the Frame Count register, loads the write data function code into the Control register, places data on the data bus, and asserts RUN H to the TM02. When the TM02 is ready to accept a data word it asserts SCLK to the Massbus Controller, which responds by asserting WCLK to the TM02.

The data word, transmitted over the Massbus, is received in the TM02 by the Massbus Receivers (M5903) and applied to the Bit Fiddler Write Buffer. When WCLK is received by the TM02, the data word is strobed in this buffer. The Bit Fiddler Write Multiplex now disassembles the data word by multiplexing different portions of the word onto the eight Write Data Bit Fiddler Output (WDBFO) lines. Some of these lines may not contain true data, but may be forced high or low to conform to the format in which data is to be written on tape. The manner in which the Bit Fiddler operates will be determined by the format bits in the Tape Control register.

The outputs of the Bit Fiddler are input to the Tape Control Common Mode (TCCM) module (M8903) where they are used to generate a vertical parity bit for the tape character. The Bit Fiddler outputs, together with the vertical parity bit, are one set of inputs to the TCCM Write Multiplex.

The Bit Fiddler outputs, along with the vertical parity bit, are also input to the Write CRCC Generator on the Tape Control-NRZI module (M8904), where in NRZ mode they generate the CRCC that will be written on the tape (nine-track only) at the end of the record. The outputs of the CRCC Generator are another set of inputs to the TCCM Write Multiplex.

A third set of inputs to the TCCM Write Multiplex are the all 1s/0s. These inputs are controlled by the Tape Control-PE circuitry (M8902), and are selected by the TCCM Write Multiplex when the PE preamble or post-amble is written. They cause the all-1s and all-0s characters of the PE preamble and postamble to be written.

The fourth set of inputs to the TCCM Write Multiplex are the inverted contents of the multiplex that are fed back from the TCCM Write Buffer. These inverted inputs are used to convert binary inputs to the TCCM Write Multiplex into the Phase Encoded (PE) mode. The TCCM Write Multiplex and Write Buffer operate together to perform this function.

The output of the Write Multiplex is clocked into the Write Buffer. In NRZ mode, this clock occurs once for every character written on tape. In PE mode, the clock occurs twice for every character written: once when normal data is output from the Write Multiplex, and once again when inverted data is output from the Write Multiplex. It is this operation that produces phase encoding in PE mode. Figure 2-5 shows the timing of Write Multiplex-Write Buffer operation for PE and NRZ modes. Note that for NRZ mode the output of the Write Buffer is still in binary form. The output of the TCCM Write Buffer is then applied to signal drivers that transmit the data via the slave bus to the TU16.

In order to write tape mark (TM) characters or IDB, appropriate codes are obtained by clearing selected bits in the Write Buffer and forcing the data lines to their desired values.

The slave bus Write Data line signals are received by slave bus receivers on the Logic and Write (LAW) module (M8910), and then input to the LAW Write Data Multiplex, through which they pass to the LAW Write Deskew Buffer.

Timing for TCCM and Bit Fiddler write operations is derived from WRT CLK, which is generated in the TU16 and transmitted to the TM02. WRT CLK is also gated in the TM02 to produce REC pulses, which are transmitted back to the TU16. REC pulses are input to a delay, which is tapped (hardwired at manufacture), and connected to the clock inputs of the Write Deskew Buffer. This arrangement provides write deskew; it compensates for errors inherent in the manufacture of tape heads, which prevent the heads for all the tape tracks from lining up ideally.

The Write Deskew Buffer circuitry also converts the binary NRZ data to its NRZ form, i.e., transition for 1s, no transition for 0s. The Write Deskew Buffer output is then driven to the write heads.

2.4 READ DATA PATH
The read data path, shown in the TU16/TM02 block diagram (Figure 2-3), is discussed in this section in greater detail (Figure 2-6).
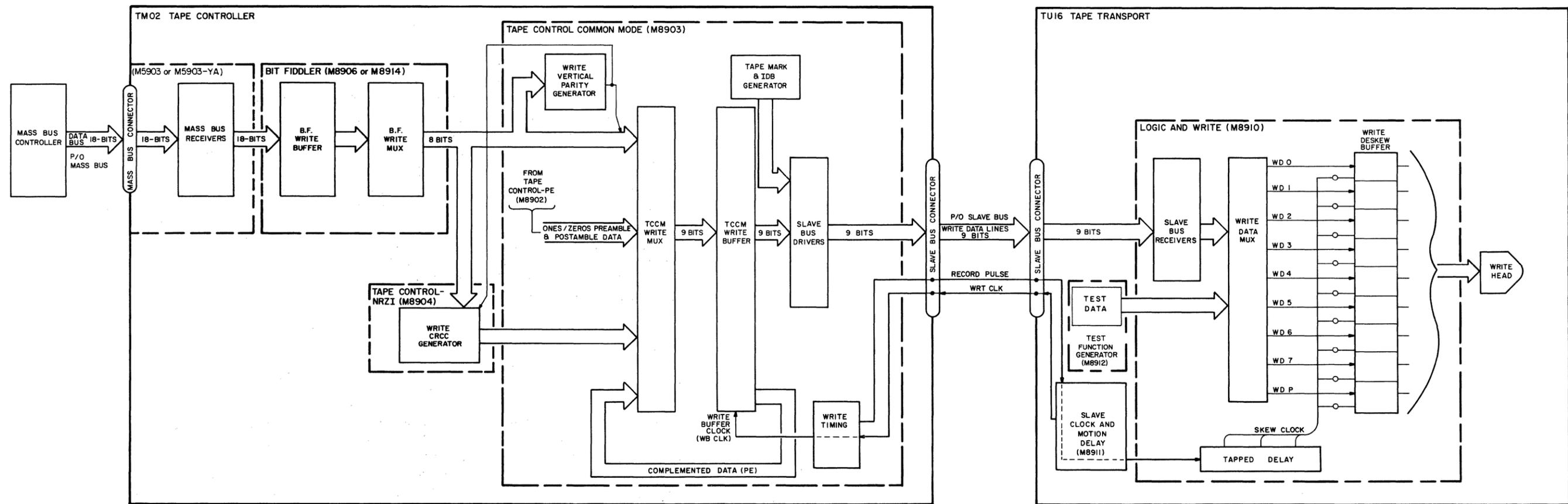
Figure 2-4 Write Data Path
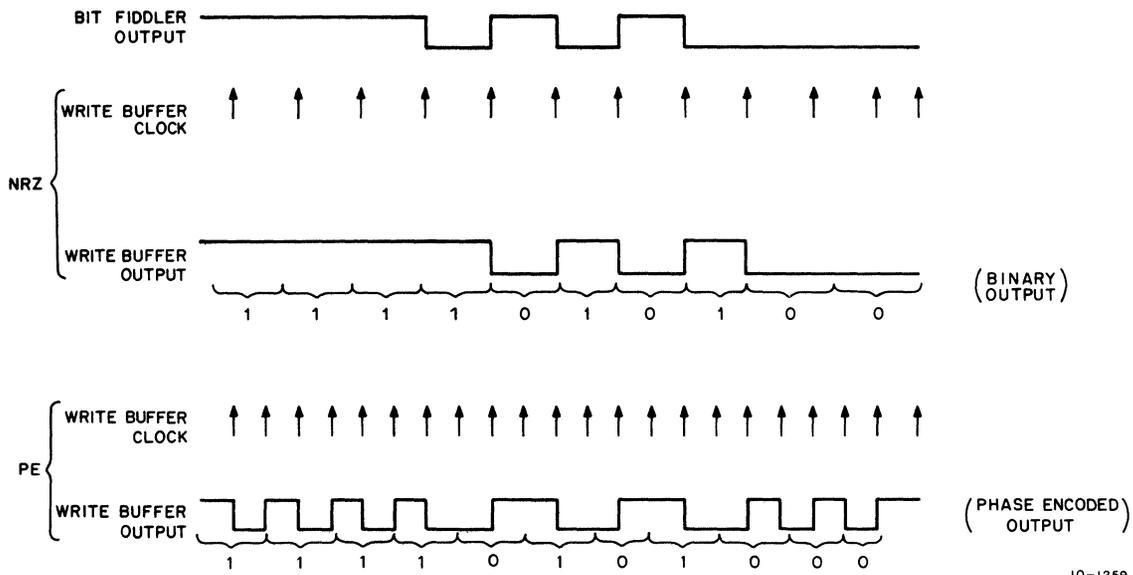
Figure 2-5 TCCM Write Timing

As tape moves past the read heads, flux transitions on the tape cause the read heads to produce positive and negative current pulse outputs. These current pulses are processed in the Read Amplifiers (G056) to yield voltage levels of the form shown in Figure 2-7. The voltage levels are transmitted by Line Drivers in the TU16 across the slave bus Read Data lines to the TM02 TCCM module. The read data is passed through the TCCM Read Multiplex to the three Data Sync (PE) modules and the Tape Control-NRZI module. However, the operation of one of these modules will be disabled, depending on whether the TU16/TM02 is operating in PE or NRZ mode.

In NRZ mode, the Tape Control-NRZI module is enabled, and data is strobed from the TCCM Read Multiplex into the Tape Control-NRZI Read Latch by RDS (Read Data Strobe). RDS, generated from RSDO (Read Strobe Delay Over) transmitted from the TU16, occurs when a valid tape character is known to be at the output of the TCCM Read Multiplex. RDS also clocks the CRCC and LRCC Generator, so that the data being read off the tape can be validated at the end of the read operation by comparing the generated CRCC/LRCC against the CRCC and LRCC read off the tape. The contents of the Tape Control-NRZI Read Latch are available to the Maintenance Register module (M8905) Multiplex.

In PE mode, the Tape Control-NRZI circuitry is disabled, while the Data Sync and Tape Control-PE

modules are enabled. The phase encoded data is input to the Data Sync modules (each module processes three data bits), which sync onto the frequency of the data during the preamble. The PE data on each track is then decoded and stored in the Deskew register. Only when all the bits of a character are available in the Deskew register is the character read from the register. Because the Deskew register has a capacity of 9 X 8 bits, a skew of 8 - 1 = 7 characters can be accommodated by the TU16/TM02.

The output of the Deskew register is input to error correction circuitry. If a vertical parity error occurs along with a single dead track error, the data on the dead track is corrected on the fly. The data (minus parity) is then output to the Maintenance Register module multiplex.

The Maintenance Register Multiplex passes the data character through to the Bit Fiddler, where it is loaded into position in the Bit Fiddler Read Data Buffer. When the Read Data Buffer is full (this will require two or more tape characters), the Bit Fiddler issues SCLK to the Massbus Controller.

Read data and SCLK are driven to the Massbus Controller by the Massbus Drivers (M5903 or M5903-YA). When the controller receives SCLK, it strobes in the word on the Data lines of the Massbus.

2-12
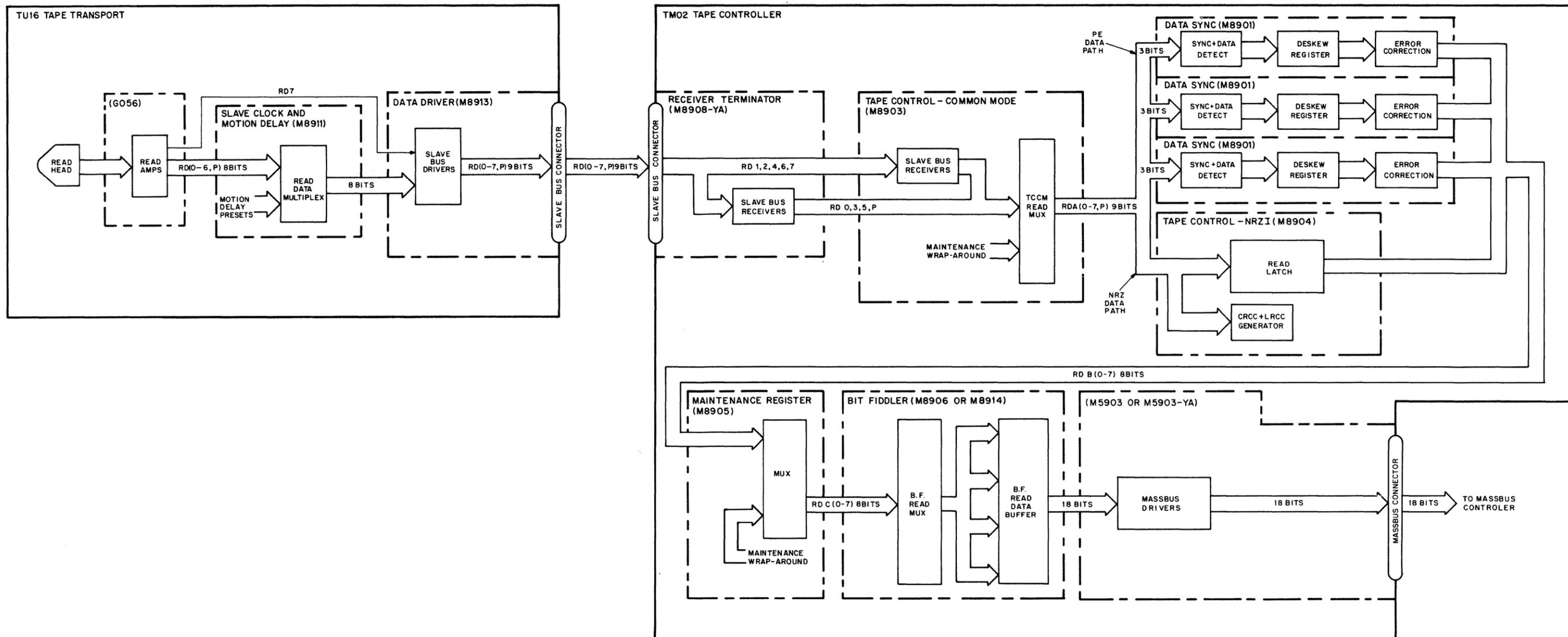
Figure 2-6   Read Data Path

2-13
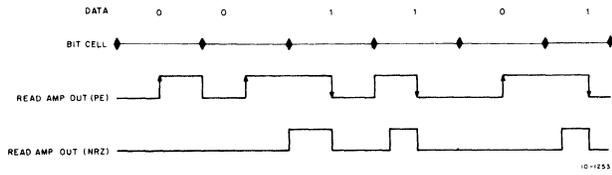
Figure 2-7 Read Amplifier Outputs

2.5 REGISTER FUNCTIONS AND FORMATS

The TM02 contains ten registers, some of which have been mentioned in previous discussions. A summary of the TM02 registers is provided in Table 2-3. Any of the TM02 registers may be read from to determine the status of the TU16/TM02 Tape Drive. Some of the registers may be written into, thereby controlling TU16/TM02 functions and operating parameters.

Table 2-3
TM02 Registers

Address Code (Octal)	Name	Type	Description
00	Control I (CS1)	Read/write	Contains the function code including the GO bit.
01	Status (DS)	Read only	Contains all nonerror status information plus the Error Summary bit.
02	Error (ER)	Read only	Contains all error indications.
03	Maintenance (MR)	Read/write	Controls diagnostic functions.
04	Attention Summary (AS)	Read/write	Indicates the Attention Active status of each TM02 (one bit/TM02).
05	Frame Count (FC)	Read/write	For a data transfer operation, contains the number of tape characters to be transferred. For a space operation, contains the number of records to be spaced.
06	Drive Type (DT)	Read only	Indicates the transport type and status (e.g., existing TU16 with power applied).
07	Check Character (CK)	Read only	For an NRZ operation, contains the CRC error character. For a PE operation, contains the dead track indications.
10	Serial Number (SN)	Read only	Contains the last four digits of the transport serial number.
11	Tape Control (TC)	Read/write	Contains the transport selection and configuration codes.

Control I (CS1) – Register 00

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				DVA*						F/5	F/4	F/3	F/2	F/1	F0/GO

DEFINED BY MASS BUS CONTROLLER · FUNCTION CODE
*DRIVE AVAILABLE, HARDWIRED SET 10-1274

Status (DS) – Register 01

ATA	ERR	PIP	MOL	WRL	EOT		DPR	DRY	SSC	PES	SDWN	IDB	TM	BOT	SLA

NOT USED 10-1275

Error (ER) – Register 02

COR/CRC	UNS	OPI	DTE	NEF	CS/ITM	FCE	NSG	PEF/LRC	INC/VPE	DPAR	FMT	CPAR	RMR	ILR	ILF

10-1276

Maintenance (MR) – Register 03

MDF8	MDF7	MDF6	MDF5	MDF4	MDF3	MDF2	MDF1	MDF0	SWC	MC	MOP3	MOP2	MOP1	MOP0	MM

MAINTENANCE DATA FIELD · SWC · MODE OF OPERATION 10-1277

Attention Summary (AS) – Register 04

								ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

NOT USED

Frame Count (FC) – Register 05

FC 15	FC 14	FC 13	FC 12	FC 11	FC 10	FC 9	FC 8	FC 7	FC 6	FC 5	FC 4	FC 3	FC 2	FC 1	FC 0

10-1307

Drive Type (DT) – Register 06

NSA	TAP	MOH	7CH	DRQ	SPR										

NOT USED · DRIVE TYPE (0-8) 10-1278

Check Character (CK) – Register 07

For an NRZ operation, contains the CRC error character.

							CRC PAR	CRC 7	CRC 6	CRC 5	CRC 4	CRC 3	CRC 2	CRC 1	CRC 0

NOT USED

For a PE operation, contains the dead track indications.

							DT4 PAR	DT7	DT6	DT5	DT3	DT9	DT1	DT8	DT2

NOT USED 10-1273

Serial Number (SN) – Register 10

SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0

4th DIGIT · 3rd DIGIT · 2nd DIGIT · 1st DIGIT 10-1272

Tape Control (TC) – Register 11

ACCL	FCS	TCW	EAO DTE		DEN 2	DEN 1	DEN 0	FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL 0	EV PAR	SS2	SS1	SS0

NOT USED 10-1279

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				DVA*						F/5	F/4	F/3	F/2	F/1	FØ/GO

DEFINED BY MASS BUS CONTROLLER   FUNCTION CODE

*DRIVE AVAILABLE, HARDWIRED SET

10-1274

Figure 2-8   Control Register Format

The TM02 registers are read and written into by performing "handshake" operations on the control bus of the Massbus. A register is loaded by the Massbus Controller in the following manner:

1. The controller places the select code of the desired TM02 on the Drive Select lines.

2. The controller places a register select code on the Register Select lines.

3. It asserts CTOD H (Controller To Drive).

4. It places data on the Control lines.

5. The controller then asserts DEM H.

The selected TM02 responds to DEM H and CTOD H asserted by loading the selected register with the data on the Control lines. It then asserts TRA H. The controller responds by negating DEM H, which causes the TM02 to negate TRA H; the write operation is thereby terminated.

A TM02 register is read in a similar manner except that CTOD H is negated (step 3) and step 4 is eliminated. The selected TM02 responds to DEM H asserted and

CTOD H negated by gating out the contents of the selected register onto the Control lines. It then asserts TRA H, which, when received by the controller, causes it to strobe in the data on the Control lines and negate DEM H. The TM02 responds by negating TRA H, thereby terminating the operation.

The remainder of Section 2-5 provides a more detailed description of the TM02 registers and their contents. It is primarily for reference, and may be skipped during a first reading.

2.5.1 Control Register (Register 00₈)

The Control register is a read/write register (Figure 2-8) which receives operational commands from the Massbus Controller via the control bus. This register operates in conjunction with the Tape Control register to control the operation of the selected transport.

The TU16/TM02 responds to the 14 function codes listed in Table 2-4. If the Control register is loaded with a function code (with GO bit set) that does not agree with those listed in the table, an Illegal Function Error (ILF) is generated. Thus, an ILF is generated for codes 05_8, 12_8, 37_8, but not for 00_8, 02_8, 06_8, 10_8, 20_8, 24_8, 30_8, etc.

Table 2-4
Command Function Codes

Function Code F (0—5) (octal)	Operation	Description
01	No Op	Performs no operation. Clears GO bit in Control register.

03	Rewind Off-line*	1. Initiates a rewind on selected transport and places it off-line.
		 2. Clears GO bit.
		 3. Sets the following bits in the Status register:
		     Drive Ready (DRY)
		     Slave Status Change (SSC)
		     Attention Active (ATA)

*Requires manual intervention to return transport on-line.

2-15

Table 2-4 (Cont)
Command Function Codes

Function Code F (0—5) (octal)	Operation	Description
07	Rewind	1. Initiates a rewind to BOT marker on selected transport and clears the GO bit. 2. Sets DRY, PIP, and ATA bits in the Status register during rewind. 3. When BOT is sensed, sets SSC and clears PIP.
11	Drive Clear	Similar to Initialize. Resets all TM02 and selected transport logic only. Does not affect unselected transports.
21	Read-In Preset	Presets the Tape Control register (R11) to select slave 0, odd parity, PDP-10 core dump format, and 800 bpi NRZI, then causes slave 0 to rewind.
25	Erase	Erases approximately 3 in. of tape. Clears GO bit and sets ATA on termination.
27	Write Tape Mark	Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination.
31	Space Forward	Moves tape forward (toward EOT) on the selected transport over the number of records specified by the Frame Count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
33	Space Reverse	Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the Frame Count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
51	Write Check Forward	Same as Read Forward.
57	Write Check Reverse	Same as Read Reverse.
61	Write Forward	Writes forward one tape record on the selected transport. Record length is determined by Frame Count register. Clears GO bit on command termination.
71	Read Forward	Reads forward one tape record on the selected transport. Clears GO bit on command termination.
77	Read Reverse	Reads reverse one tape record on the selected transport. Clears GO bit on command termination.

2.5.2 Status Register (Register 01_8)

The Status register is a 16-bit, read-only register which stores the tape system status information. Figure 2-9 illustrates the Status register format and Table 2-5 defines the bit positions. Although the Status register multiplexer is located in the TM02, inputs to this multiplexer may be generated either by a selected transport, any transport, or the TM02 logic itself. Because of this fact, each bit position in Table 2-5 is identified by one or more of the following designators to indicate the origin of the input signal.

(SS) = Selected transport
(S) = Any transport
(M) = TM02 logic

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	EOT		DPR	DRY	SSC	PES	SDWN	IDB	TM	BOT	SLA

NOT USED

10-1275
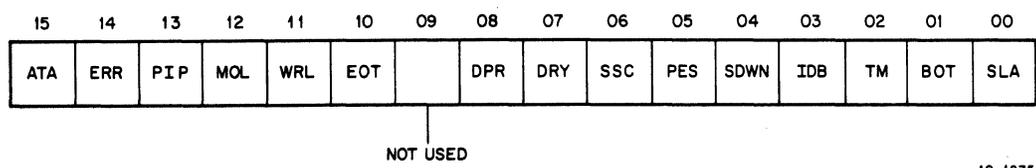
Figure 2-9 Status Register Format

Table 2-5
Status Register Bit Positions

Bit Position	Name	Description
00 (SS)	Slave Attention (SLA)	Indicates that a selected transport has come on-line.
01 (SS)	Beginning of Tape (BOT)	Indicates that a selected transport has detected the BOT marker.
02 (M)	Tape Mark (TM)	Indicates that a tape mark has been detected. Remains asserted until the next tape motion is initiated.
03 (M)	Identification Burst (IDB)	Indicates that a Phase Encoded (PE) identification burst has been detected. Asserted until a subsequent tape motion command is initiated.
04 (SS)	Settle Down (SDWN)	Indicates that tape motion on the selected transport is stopping.
05 (SS)	Phase Encoded Status (PES)	Indicates that the selected transport is configured for PE operation. Is negated during NRZ operation.
06 (S)	Slave Status Change (SSC)	Indicates that any transport has just gone on-line or off-line, or has completed a rewind operation.
07 (M)	Drive Ready (DRY)	Indicates that both the TM02 and the selected transport are ready to accept a command.
08 (M)	Drive Present (DPR)	Hardwired set.
09	Not used	
10 (SS)	End of Tape (EOT)	Indicates that the selected transport has detected the EOT marker during forward tape motion. Is negated when the EOT marker is detected during reverse tape motion.
11 (SS)	Write Lock (WRL)	Indicates that the selected transport is write protected.
12 (SS)	Medium On-Line (MOL)	Indicates that the selected transport has tape loaded and is on-line.
13 (M/SS)	Positioning in Progress (PIP)	Indicates that the selected transport is performing a tape motion operation. This bit is asserted by the TM02 (M) during a space or by the selected transport (SS) during a rewind.
14 (M)	Composite Error (ERR)	Indicates that an error condition has occurred. Is asserted whenever any bit in the Error register is set.

Table 2-5 (Cont)
Status Register Bit Returns

Bit Position	Name	Description
15 (M)	Attention Active (ATA)	Is asserted whenever the ATTN L interface signal is generated. Indicates one of the following: 1. The TM02 and the selected transport require servicing. 2. The TM02 and the selected transport have become ready after a nontransfer operation. 3. A transport status change has occurred.

2.5.3 Error Register (Register 02₈)

There are 16 different error conditions that can be detected in the TU16/TM02 Tape Drive System. The Error register is a 16-bit, read-only register which stores all of the tape system error indications.

TU16/TM02 errors are categorized as Class A and Class B. A Class B error will terminate an in-progress data transfer; a Class A error will not. However, the Massbus Controller is notified of *any* error during a data transfer by the immediate assertion of EXC H on the Massbus. If the TU16/TM02 is not performing any operation, or is performing a rewind (i.e., the GO bit is clear), the controller is immediately notified of an error condition by the assertion of ATTN H on the Massbus.

Figure 2-10 illustrates the Error register format and Table 2-6 lists the error bit indicators.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COR/CRC	UNS	OPI	DTE	NEF	CS/ITM	FCE	NSG	PEF/LRC	INC/VPE	DPAR	FMT	CPAR	RMR	ILR	ILF
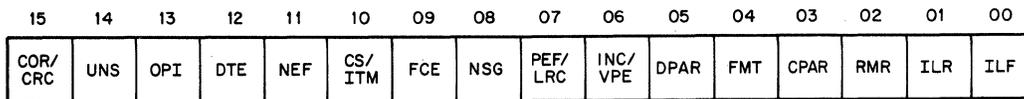
10-1276

Figure 2-10   Error Register Format

Table 2-6
Error Register Bit Indicators

Bit Position	Name	Description	Type
00	Illegal Function (ILF)	Indicates that an illegal function code has been transmitted.	Class B
01	Illegal Register (ILR)	Indicates that a read or write from a nonexistent register is attempted.	Class A
02	Register Modification Refuse (RMR)	Indicates that during a transport operation (GO = 1), a write into one of the registers is attempted. (Does not apply for the Maintenance or Attention Summary registers.)	Class A
03	Control Bus Parity (CPAR)	Indicates that incorrect control bus parity is detected.	Class A
04	Format (FMT)	Indicates that a data transfer with an incorrect format code is attempted.	Class B

Table 2-6 (Cont)
Error Register Bit Indicators

Bit Position	Name	Description	Type
05	Data Bus Parity Error (DPAR)	Indicates that incorrect data bus parity has occured.	Class A
06	Incorrectable Data Error or Vertical Parity Error (INC/VPE)	During a PE read operation, indicates that one of the following has occurred: 1. Multiple dead tracks 2. Dead tracks without parity errors 3. Parity errors without dead tracks 4. Skew overflow During an NRZ read operation, indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over.	Class A
07	Format Error or LRC (PEF/LRC)	During a PE read operation, indicates than an incorrect preamble or postamble is detected.	Class A
		During an NRZ write operation, indicates that the Read-after-write LRCC does not match the LRCC computed during the write.	Class A
08	Nonstandard Gap (NSG)	Indicates that a tape character is detected during the first half of the End of Record gap.	Class A
09	Frame Count Error (FCE)	Indicates that a space operation has terminated and the Frame Counter is not cleared. Also asserted when the Massbus Controller fails to negate RUN when the TM02 asserts EBL.	Class A
10	Correctable Skew or Illegal Tape Mark (CS/ITM)	During a PE read operation, indicates that excessive but correctable skew is detected. (This condition is only a warning and does not indicate bad data.)	Class A
		During an NRZ read, indicates that characters not legally a tape mark have been read and recognized as a tape mark.	
11	Nonexecutable Function (NEF)	Indicates one of the following: 1. A write operation is attempted on a write-protected transport. 2. A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT. 3. The DEN2 bit in the Tape Control register does not agree with the PES status bit. 4. A space or write operation is attempted when FCS = 0 in the Tape Control register. 5. A read or write operation is attempted with DEN-2 = 0 in the Tape Control register and the 2s complement of a number less than 13 is in the Frame Count register.	Class B

Table 2-6 (Cont)
Error Register Bit Indicators

Bit Position	Name	Description	Type
12	Drive Timing Error (DTE)	Indicates one of the following: 1. During a write operation, WCLK was not received from the Massbus Controller in time to provide a valid tape character. 2. A data transfer (read/write) was attempted when the data bus of the Massbus was already occupied.	Class B
13	Operation Incomplete (OPI)	During a read or space operation, indicates that a tape record has not been detected with 7 sec from command initiation. During a write operation, indicates that a read-after-write tape record has not been detected within 0.7 sec from command initiation.	Class B
14	Unsafe (UNS)	Indicates one of the following: 1. A program-controlled operation is attempted on a selected transport which is not on-line. 2. An imminent power failure is detected (AC LO L).	Class B
15	Correctable Data Error or CRC Error (COR/CRC)	During a PE read operation, indicates that a single dead track has occurred. During an NRZ operation, indicates that the CRCC read off the tape does not match the CRCC computed from the data read off the tape.	Class A

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MDF8	MDF7	MDF6	MDF5	MDF4	MDF3	MDF2	MDF1	MDF0	SWC2	MC	MOP3	MOP2	MOP1	MOP0	MM

MAINTENANCE DATA FIELD   SWC   MODE OF OPERATION
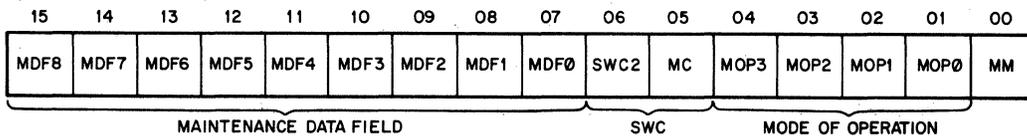
10-1277

Figure 2-11 Maintenance Register Format

2.5.4 Maintenance Register (Register 03$_8$)

The Maintenance register (M8905) is a 16-bit, read/write register (Figure 2-11) which allows complete diagnostic testing of the TM02 data paths and error detection circuitry. The Maintenance register can configure the data paths into four wrap-around loops, each loop testing certain TM02 circuits. The Maintenance register data field is part of these loops, and is used to read or write test data into the TM02. The wrap-around modes are discussed in more detail in the Maintenance Modes pamphlet (Section 3.1). Table 2-7 briefly describes the bits of the Maintenance register.

Table 2-7
Maintenance Register Bit Positions

Bit Position	Name	Description
00	Maintenance Mode (MM)	When set, configures the TM02 for maintenance mode operation.
01	Maintenance Operation Code (MOPO—3)	Controls command execution during the maintenance mode. (MM and MOP function together to alter normal command execution during maintenance mode operation.)
05	Maintenance Clock (MC)	Controls data sequencing through the TM02 data path in maintenance mode.
06	Selected Slave Clock (SWC2)	Is a clock signal generated by the selected slave at the frequency of 200 bpi data.
07—15	Maintenance Data Field (MDFO—8)	Buffers the Data generated during wrap-around operations.
		At the end of normal NRZ transfers, contains the LRC of the last record.

2.5.5 Attention Summary Register (Register 04₈)

The Attention Summary register (M8909, sheet 3) is a read/write "pseudo-register" which consists of from one to eight bits, depending on the number of TM02s in the system. The term "pseudo-register" refers to the fact that only one register bit position is physically contained in each TM02. This bit position reflects the state of the ATA status bit for that TM02. Hence, bit position 0 of the Attention Summary register is generated by the ATA bit of TM02 0, bit position 1 is generated by the ATA bit of TM02 1, and so on to bit 7. Bits 8 through 15 are not used.

Unlike the other drive registers, the Attention Summary register is directly selected by the controller without first addressing a particular TM02. Thus, for a single Attention Summary register read operation, every TM02 in the system responds by placing the state of its ATA bit in the appropriate bit position on the control bus and disabling its remaining 15 control bus transmitters. This control bus configuration appears as a single register output which collectively informs the controller of all TM02s that require attention (i.e., ATA = 1). The controller can then selectively examine the Error or Status registers of each of the affected TM02s to determine the cause of the individual attention conditions.

The controller can also write into the Attention Summary register; however, the significance of the bits being written is unusual. Writing a 1 into a bit position resets the ATA bit in the TM02 assigned to that bit position; however, writing a 0 has no effect. This unique writing scheme allows the controller to reset, after inspection, all summary bits that were set, without accidentally resetting those bits that may have become set in the meantime. The following table illustrates the effects of writing into an attention summary bit position:

ATA Bit Before	Summary Bit Written	ATA Bit After
0	0	0
1	0	1
0	1	0
1	1	0

2.5.6 Frame Count Register (Register 05₈)

The Frame Count register (M8909, sheet 8) is a 16-bit, read/write register that counts tape events. During a data transfer operation (read/write), this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time; but the controller can only write into this register when the transport is not performing a space or data transfer (GO negated).

For a write operation, the Frame Count register is loaded, prior to write initiation, with the 2s complement of the number of tape characters to be written. During the writing process, the Frame Count register is incremented each time a tape character is recorded. Normal write data transfer termination is accomplished when the Frame Count register overflows to zero. For a space operation, the Frame Count register functions similarly to a write, except it is loaded with the 2s complement of the number of records to be spaced and is then incremented each time a record is detected. Space termination is accomplished when the register overflows to zero. For a read operation, this register is automatically reset prior to read initiation. The register is then incremented each time a tape character is read. Thus, at the end of the read operation, the Frame Count register contains a count of the number of characters read.

2.5.7 Drive Type Register (Register 06$_8$)

The Drive Type register (M8903) is a 16-bit, read-only register, the content of which identifies the particular type of storage device (transport) being used. When a read from the Drive Type register is performed, the register output is applied to the appropriate multiplexer bit positions. The remaining bit positions are forced reset, and hence the 8-bit output of the Drive Type register presents a 16-bit format to the controller.

Bits 0 through 8 (DTO—8) of the Drive Type register identify the type and status of the selected transport. If a nonexistent transport is selected or if the selected transport is not powered up, DTO—8 will contain 010_8. If the selected transport is powered up, but is not a TU16, DTO—8 will contain 012_8 to 017_8, depending on the type of transport. If the selected transport is a TU16 and is powered up, these bit positions will contain 011_8.

Figure 2-12 illustrates the Drive Type register format and Table 2-8 briefly describes each bit position.

2.5.8 Check Character Register (Register 07$_8$)

The Check Character register (M8905) is a nine-bit, read-only register which permits the programmer to check the validity of a data transfer. At the end of an NRZ read operation, this register contains the CRCC for that operation. Hence, the programmer can determine if the CRCC generator logic is functioning properly. At the end of a PE read operation, however, this register contains a dead track indication (DT = 1) of any track which may have dropped one or more bits during the operation.

Figure 2-13 illustrates the Check Character register format for both NRZ and PE modes.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NSA	TAP	MOH	7CH	DRQ	SPR										

NOT USED

DRIVE TYPE (0-8)
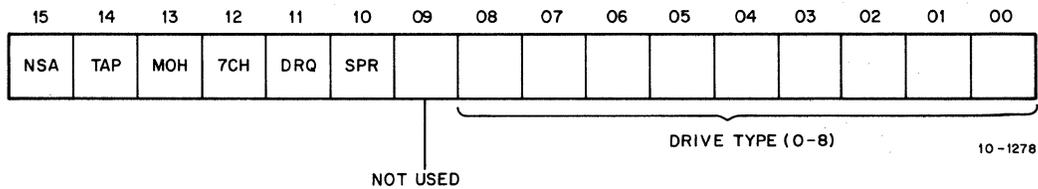
10-1278

Figure 2-12   Drive Type Register Format

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							CRC PAR	CRC 7	CRC 6	CRC 5	CRC 4	CRC 3	CRC 2	CRC 1	CRC 0

NOT USED

A. NRZ FORMAT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							DT4 PAR	DT7	DT6	DT5	DT3	DT9	DT1	DT8	DT2

NOT USED

B. PE FORMAT
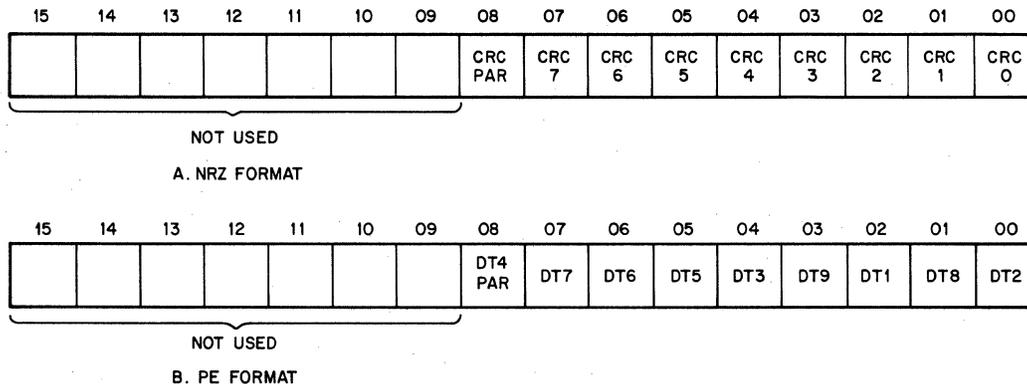
10-1273

Figure 2-13   Check Character Register Format

2-22

Table 2-8
Drive Type Register Bit Positions

Bit Position	Name	Description
00—08	Drive Type (DTO—8)	Specifies the drive type (011 = TU16).
10	Slave Present (SPR)	Asserted when a transport is powered up and has been assigned the selection code contained in the Tape Control register.
11	Drive Request Required (DRQ)	Always negated to indicate that the device is a single-port unit.
12	7-Channel (7CH)	Asserted if the selected transport is a 7-channel unit. Negated if the selected transport: 1. Is a 9-channel unit 2. Does not have power applied 3. Is disconnected from the slave bus.
13	Moving Head (MOH)	Always negated to indicate that the device is not a moving head unit.
14	Tape Drive (TAP)	Always asserted to indicate that the device is a tape transport.
15	Not Sector Addressed (NSA)	Always asserted to indicate that the device is not sector addressable.

2.5.9 Tape Control Register (Register 11$_8$)

The Tape Control register (M8905) is a 16-bit, read/write register which selects an existing transport and configures it to a particular operational mode.

Figure 2-14 illustrates the Tape Control register and Table 2-9 briefly describes each bit position.

2.5.10 Serial Number Register (Register 10$_8$)

The Serial Number register (M8912) is a 16-bit, read-only register which contains a BCD representation of the four least-significant digits of the transport serial number. This register is located on the Test Function Generator module and the register inputs are hardwired to the BCD configuration of the least-

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACCL	FCS	TCW	EAO DTE		DEN 2	DEN 1	DEN 0	FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL 0	EV PAR	SS2	SS1	SSO

NOT USED

10-1279
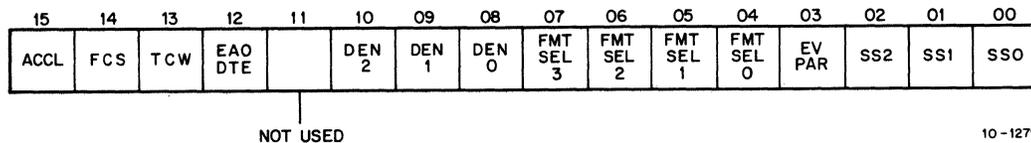
Figure 2-14   Tape Control Register Format

Table 2-9
Tape Control Register Bit Positions

Bit Position	Name	Description
00—02	Slave Select (SSO—2)	Specifies the unit number of the transport to be used.
03	Even Parity (EV PAR)	When set for NRZ operation, even parity is written or read from tape. Ignored during PE operation.
04—07	Format Select (FMT SEL0—3)	Specifies Massbus-to-tape character formatting during a write operation, or tape character-to-Massbus formatting during a read (Table 2-10).

Table 2-9 (Cont)
Tape Control Register Bit Positions

Bit Position	Name	Description
08—10	Density Select (DEN0—2)	Specifies the tape character density during read or write operations as follows: DEN2 DEN1 DEN0 Density (bpi) 0 0 0 200 0 0 1 556 } NRZ 0 1 0 800 0 1 1 800 1 0 0 1600 PE 1 0 1 1 1 0 } Reserved 1 1 1
11	Not used	
12	Enable Abort on Data Transfer Errors (EAODTE)	When set, immediately aborts a write or read operation for one of the following errors: 1. COR/CRC — Error register bit 15. 2. FMT/LRC — Error register bit 7. 3. INC/VPE — Error register bit 6. 4. DPAR — Error register bit 5.
13	Frame Count Status (FCS)	Is normally set at the end of a write into the Frame Count register. However, if FCS = 0, and a space or write command with GO = 1 is loaded, a nonexecutable function (NEF) error is generated and the command is not executed. Is reset when Frame Count register overflows.
14	Tape Control Write (TCW)	Is set when Tape Control register is written into. Is cleared with any tape motion command.
15	Acceleration (ACCL)	This read-only bit is asserted when the transport is not actively reading or writing data.

Table 2-10
Format Select Codes

System	Code	Description
PDP-10	0000	Core Dump
PDP-10	0001	7-Track (Not used)
PDP-10	0010	ASCII
PDP-10	0011	Compatible
PDP-11	1100	Normal
PDP-11	1101	Core Dump
PDP-11	1110	15 Normal

See Notes.

Notes

1. Codes 0000 — 0011 use an M8914 Data Formatting module.

2. Codes 1100 — 1110 use an M8906 Data Formatting module.

3. An invalid code causes a Format Error (FMT — Error register bit 4) when a data transfer command with GO = 1 is loaded.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0

4th DIGIT   3rd DIGIT   2nd DIGIT   1st DIGIT

10-1272
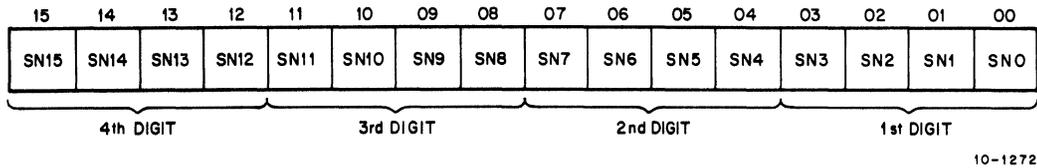
Figure 2-15   Serial Number Register Format

significant serial number digits. Since the Test Function Generator module must be switched from slot EF to slot AB of the logic assembly for off-line transport testing, the Serial Number register does not function during the test mode. If the generator module is inadvertently left in the test slot during on-line operations, the MOL (Medium On-Line) bit in the Status register is not asserted and thus the transport is unusable.

Figure 2-15 illustrates the Serial Number register format.

2.6 OPERATIONAL SEQUENCES

This section discusses the sequencing that occurs when the TU16/TM02 performs functional operations. Each operation is described separately to simplify the presentation. However, this does cause considerable redundancy, especially for similar operations. If the equipment is down and time is critical, it is recommended that only applicable portions of this section be read.

2.6.1 Rewind

A program-controlled rewind operation may be initiated by one of two commands from the processor. One of these commands (07_8) performs the rewind operation and retains the transport on-line. The other command (03_8) places the transport off-line immediately after command initiation. Following completion of the 03_8 command, the operator must use the ON-LINE/OFF-LINE switch on the transport to return it to the on-line status. With the exception of the status bit indicators (Table 2-5), both rewind commands function identically.

Figure 2-16 illustrates the major functional sequences of a rewind operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.1.1 Command Initiation — To initiate a program-controlled rewind operation, the Massbus Con-

troller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register (R10), selecting the slave TU16 desired to perform the rewind operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus. The Massbus Controller then writes the operational function code of the rewind command (03_8 or 07_8) into the Control register (R00). The TM02 decodes the function
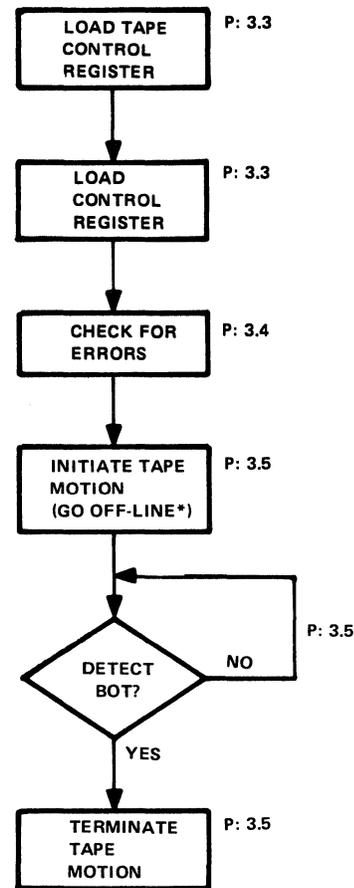
*03 COMMAND ONLY.

NOTE
P: REFERENCES
CHAPTER 3 PAMPHLET

10-1252

Figure 2-16   Rewind Operation Flowchart

2-25

code and asserts RWND L on the slave bus. (If a rewind/off-line operation has been specified, the TM02 also asserts WRITE L.) It then checks for errors, and, if there are none, issues SLAVE SET Pulse and STOP L to the TU16, and clears the GO bit in the Control register.

2.6.1.2 Command Execution — The TU16, enabled by its address code on the Slave Select lines (SS 0—2), responds to SLAVE SET Pulse by setting a Rewind Status flip-flop (if WRITE L is also asserted, it also places itself off-line), which activates the capstan drive for a high-speed (150 in./sec) rewind operation. The TU16 can now complete the rewind operation independently, and the Massbus Controller and TM02 may divert attention to other transports.

2.6.1.3 Command Termination — When the reflective beginning-of-tape (BOT) marker is detected, the TU16 terminates its high-speed reverse motion, but will overshoot the BOT marker. The TU16 then initiates forward tape motion at read/write speed (45 in./sec). When it encounters the BOT marker again, the Rewind Status flip-flop is reset, and the capstan motor is deactivated. When the TU16 has completed its rewind operation, it asserts SET SSC (Slave Status Change) on the slave bus. This causes the attention bit in the TM02 to be set, which results in ATTN H being asserted on the Massbus, thereby notifying the Massbus controller.

2.6.2 Space

Figure 2-17 illustrates the major functional sequences of a space operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.2.1 Command Initiation — To initiate a space operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, selecting the slave TU16 desired to perform the space operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus.

The Massbus Controller then loads the 2s complement of the number of tape records to be spaced into the TM02 Frame Count register. Following this, the controller loads the Control register with the operational function code of the space command (31 for space forward, 33 for space reverse). The TM02 decodes the
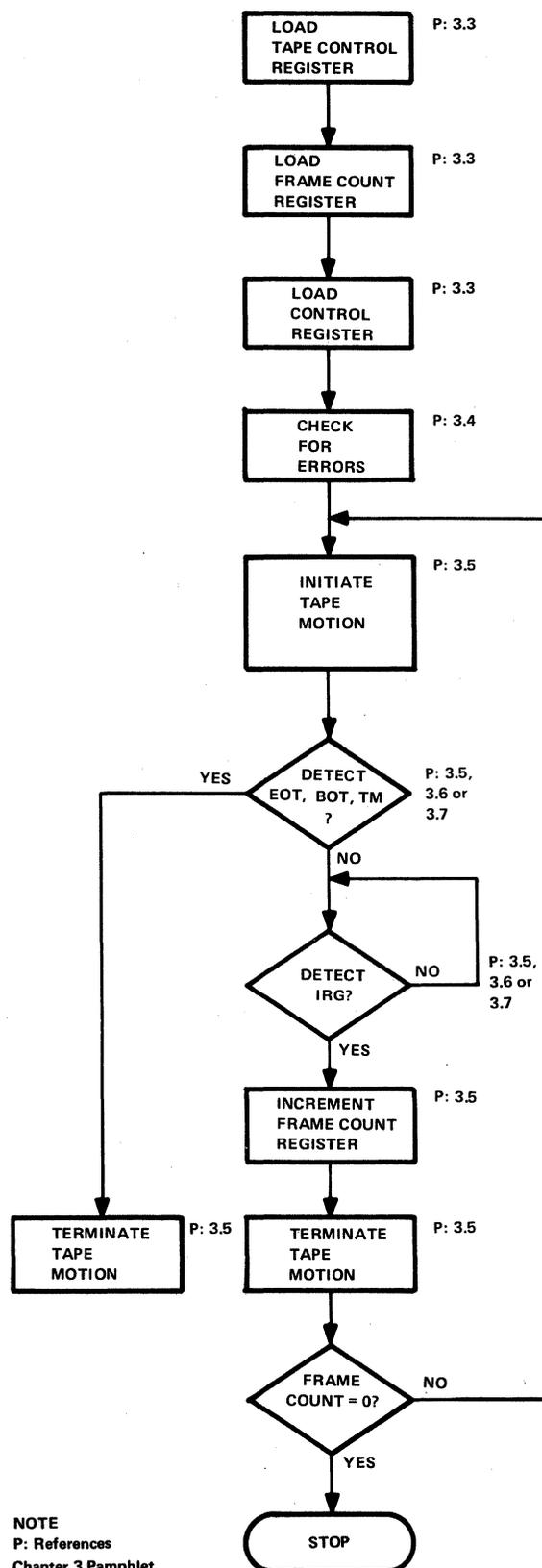
Figure 2-17   Space Operation Flowchart

2-26

function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET Pulse and EMD to the TU16.

2.6.2.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines (SS 0—2), responds to SLAVE SET Pulse by setting a motion control flip-flop (forward or reverse) in its LAW module (M8910), which activates the capstan drive for forward or reverse motion (45 in./sec).

The selected TU16 also responds to EMD, multiplexing motion delay presets onto the Read Data lines of the slave bus. The TM02 uses the presets to generate a motion delay, at the end of which the read heads will detect a record. (As the tape moves under the read heads, tape characters are detected exactly as they are during a read operation; however, Bit Fiddler operation is suppressed.)

When the end of the record, i.e., IRG (Interrecord Gap), is detected, a signal (RECORD H) from the TCCM module increments the Frame Count register, and another motion delay is generated. At the end of this motion delay, STOP L is asserted on the slave bus and causes the motion control flip-flop in the TU16 to be reset. Soon after, however, another SLAVE SET Pulse from the TM02 sets this flip-flop again, as another motion delay is generated. At the end of this motion delay, the read heads will detect the next record. At the end of this record, the Frame Count register is again incremented and another motion delay occurs. This sequence continues for all the records spaced. Because the resetting and setting of the TU16 motion control flip-flops takes place within approximately 1 μs, the space operation will be performed at a constant speed (45 in./sec).

2.6.2.3 Command Termination — After the last record has been spaced, the Frame Count register will overflow to zero. This will inhibit a SLAVE SET Pulse to the TU16; the motion control flip-flop will not be reset. The capstan will remain deactivated, and tape motion will be terminated. If BOT, EOT, or TM are detected before the Frame Count register overflows, tape motion will also be terminated. Upon detection of BOT, EOT, TM, or frame count overflow, the GO bit of the Control register is cleared.

2.6.3 Erase

Figure 2-18 illustrates the major functional sequences of an erase operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an ap-

plicable detailed logic description pamphlet in Chapter 3.

2.6.3.1 Command Initiation — To initiate an erase operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, selecting the slave TU16 desired to perform the erase operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus. The Massbus Controller then loads the

NOTE
P: REFERENCES
CHAPTER 3 PAMPHLET
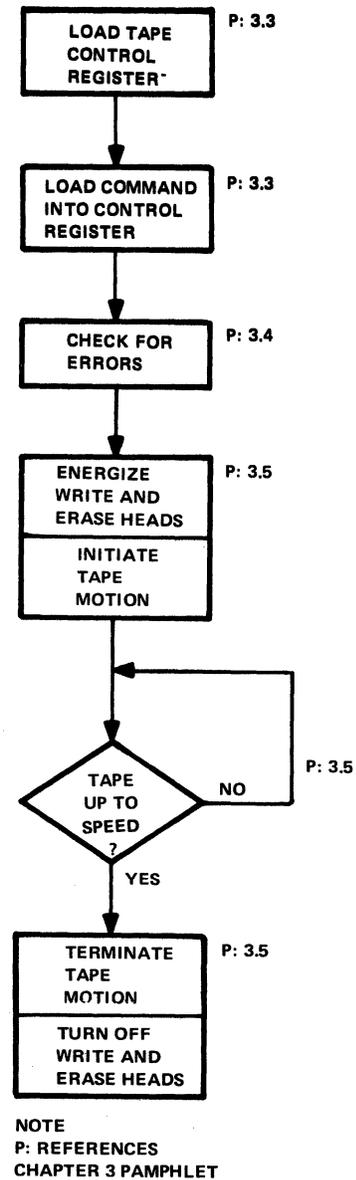
10-1251

Figure 2-18   Erase Operation Flowchart

TM02 Control register with the operational function code (25) of the erase command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET Pulse and EMD (Enable Motion Delay) to the TU16.

2.6.3.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines, responds to SLAVE SET Pulse by setting its Forward motion and Write Enable flips-flops, which activate the capstan drive (starting forward tape motion) and the write and erase heads. It also responds to EMD by gating out a motion delay preset onto the slave bus Read Data lines. The preset is loaded into a counter in the TCCM module, which is then counted up. When a count of 2 is reached, tape motion is considered to be up to speed.

Since the erase head is activated and the write heads receive no data input during an erase operation, all the tape moving past the erase head will be dc erased.

2.6.3.3 Command Termination — When the start motion delay is over, another motion delay is started. At the end of this second (stop) motion delay, the TM02 asserts STOP L on the slave bus. STOP L causes the Forward motion control flip-flop to be reset, thereby deactivating the capstan motor. STOP L also causes the GO bit of the Control register to be cleared. When tape motion has ceased, the Write Enable flip-flop is cleared, de-energizing the write and erase heads.

2.6.4 PE Data Read

Figure 2-19 illustrates the major functional sequences of a PE read operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.4.1 Command Initiation — To initiate a PE read operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU16, tape character format, and tape data density (1600 bpi for PE).

The TM02 places the slave select (SS 0—2) and density (DEN 0—2) bits of the Tape Control register on the slave bus. The Massbus Controller then loads the TM02 Control register with the operational function code of a read operation (71 read forward, 77 read re-
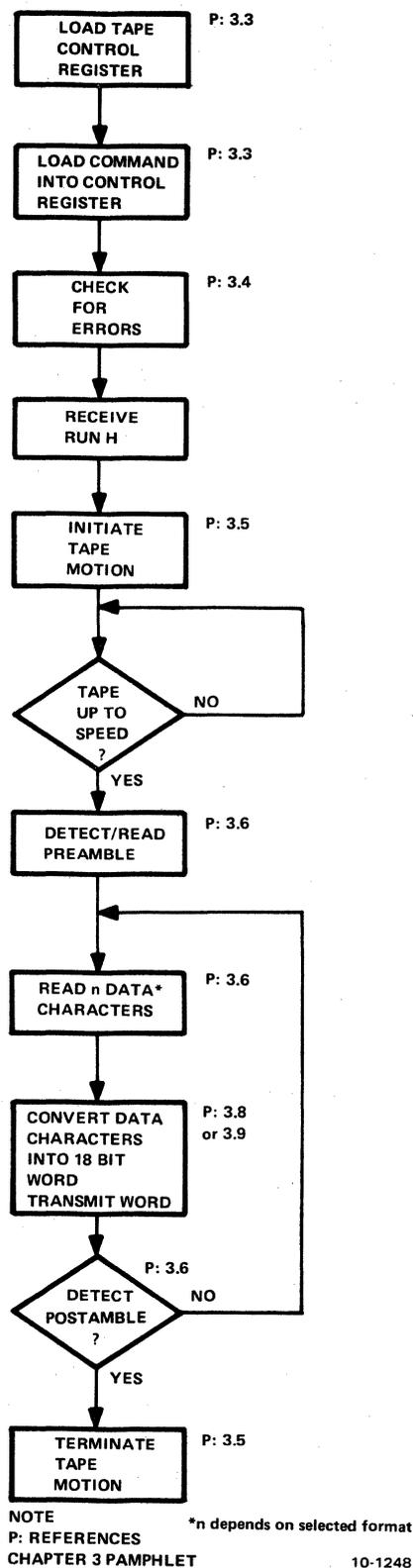
Figure 2-19   PE Read Operation Flowchart

2-28

verse, 51 write check forward, or 57 write check reverse) and asserts RUN on the Massbus. The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM02 then transmits SLAVE SET Pulse to the TU16 and initiates a motion delay.

2.6.4.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines (SS 0—2) of the slave bus, responds to SLAVE SET Pulse by setting a motion control flip-flop (forward or reverse), thereby activating the capstan drive motor and tape motion.

The TU16 Read Amplifiers are on continuously. Even as the tape accelerates, the TM02 PE read circuitry checks for a PE Identification Burst (IDB) and begins looking for a preamble. When the tape is at speed, the preamble will be detected and read; the tape characters immediately after the preamble all-1s character are data characters. These are deskewed in the Data Sync (M8901), and Tape Control-PE (M8902 logic), and sent to the Bit Fiddler (via the Maintenance Register module), which assembles the characters into 18-bit data words and places them on the data bus. When a data word is assembled, the Bit Fiddler notifies the Massbus Controller, which then strobes in the data on the data bus. The Bit Fiddler continues this assembly of data characters into 18-bit words until the first character of the postamble is detected.

2.6.4.3 Command Termination — The TM02 reads the postamble, which signifies the end of the record and asserts EBL H (End of Block) on the Massbus. When the postamble has been read, a motion delay sequence is initiated, at the end of which STOP L is asserted on the slave bus. STOP L resets the motion flip-flop in the TU16 and terminates tape motion. It also clears the GO bit in the Control register, which causes OCC to be negated on the Massbus.

2.6.5 NRZ Read

Figure 2-20 illustrates the major functional sequences of an NRZ read operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.5.1 Command Initiation — To initiate an NRZ read operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select
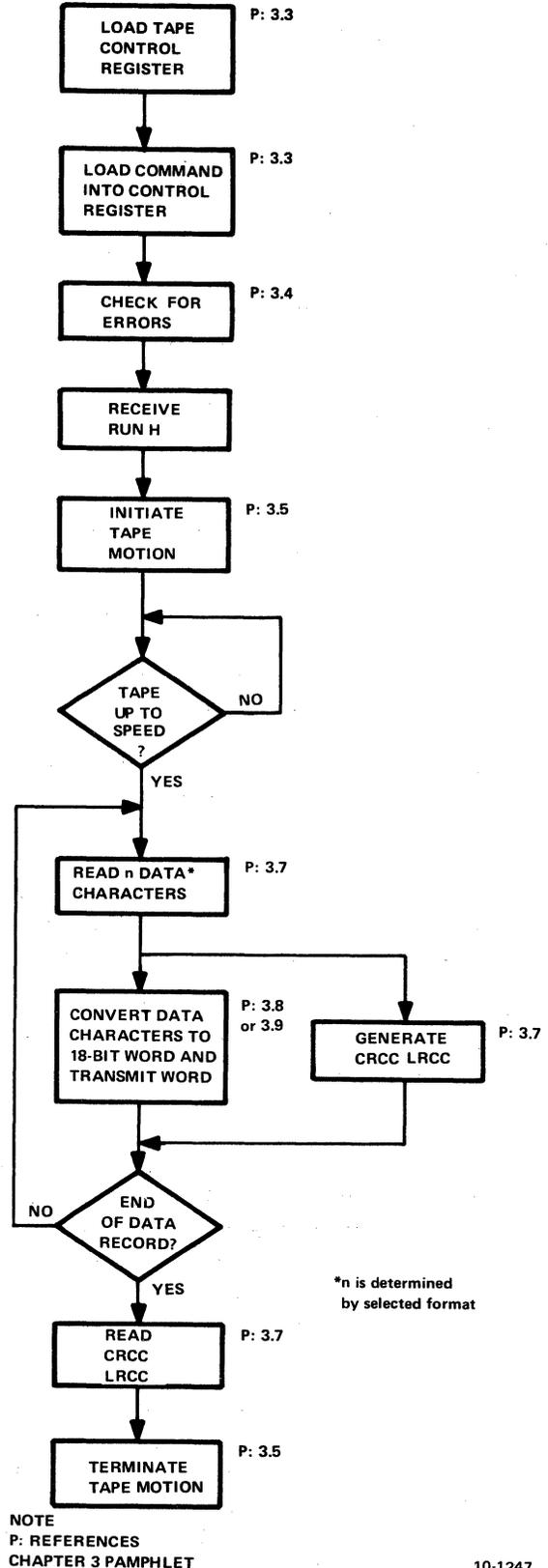
Figure 2-20   NRZ Read (Forward)
Operation Flowchart

2-29

lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU16, tape character format, and tape data density. The TM02 places the Slave Select (SS 0—2) and Density (DEN 0—2) bits of the Tape Control register on the slave bus. The Massbus Controller then loads the TM02 Control register with the operational function code of a read operation (71 read forward, 77 read reverse, 51 write check forward, or 57 write check reverse) and asserts RUN H on the Massbus. The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM02 then transmits SLAVE SET Pulse of the TU16, and initiates a motion delay.

2.6.5.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines (SS 0—2) of the slave bus, responds to SLAVE SET Pulse by setting a motion control flip-flop (forward or reverse), thereby activating the capstan drive motor and tape motion. When the motion delay has timed out, the TM02 negates ACCL L on the slave bus. This signal enables the TU16 NRZ read circuitry.

When a tape character is detected by the TU16, RSDO (Read Strobe Delay Over) is transmitted via the slave bus to the TM02 Tape Control-NRZ module, and the tape character is multiplexed onto the slave bus Read Data lines. RSDO causes the Tape Control-NRZ module to strobe in the tape character, via the TCCM module, from the slave bus. The character (minus the vertical parity bit) now becomes available to the Bit Fiddler. LRCC and CRCC are generated from the data as it passes through the Tape Control-NRZ module. These will later be used to check the validity of the data read.

The Bit Fiddler assembles the characters into 18-bit data words and places them on the data bus. When a data word is assembled, the Bit Fiddler notifies the Massbus Controller, which then strobes in the data word off the data bus. The Bit Fiddler continues this assembly of data characters into 18-bit words until the end of the data record.

During a forward read, the rest of the read circuitry continues its operation, reading the CRCC and strobing it into the Check Character register, and then reading the LRCC. Discrepancies between generated CRCC/LRCC and detected CRCC/LRCC cause their respective error bits to be set.

During a reverse read, the LRCC character is encountered first at the start of the read operation, but is ignored. The CRCC is encountered next, and strobed into the Check Character register, but otherwise it is ignored. No CRC or LRC error is generated. Then the data is read; assembly of characters into data words may differ when reading in the reverse direction, but this depends on the data format selected.

2.6.5.3 Command Termination — When the data and LRCC/CRCC have been read, the read heads will encounter the IRG. This absence of tape characters causes a motion delay, at the end of which STOP L is asserted on the slave bus and EBL (End of Block) is asserted on the Massbus. STOP L resets the motion flip-flop in the TU16 and terminates tape motion. It also clears the GO bit in the Control register, which causes OCC to be negated on the Massbus.

2.6.6 PE Data Write
Figure 2-21 illustrates the major functional sequences of a PE data write operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.6.1 Command Initiation — To initiate a PE write operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU16, tape character format, and tape data density (PE — 1600 bpi). The TM02 places the Slave Select (SS 0—2) and Density (DEN 0—2) bits of the Tape Control register on the slave bus. The Massbus Controller then loads the 2s complement of the number of tape characters to be written into the TM02 Frame Count register. Following this, the controller loads the Control register with the operational function code (61) of the data write command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM02 responds by asserting SLAVE SET Pulse on the slave bus and accepting the first data word from the controller.

2.6.6.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines (SS
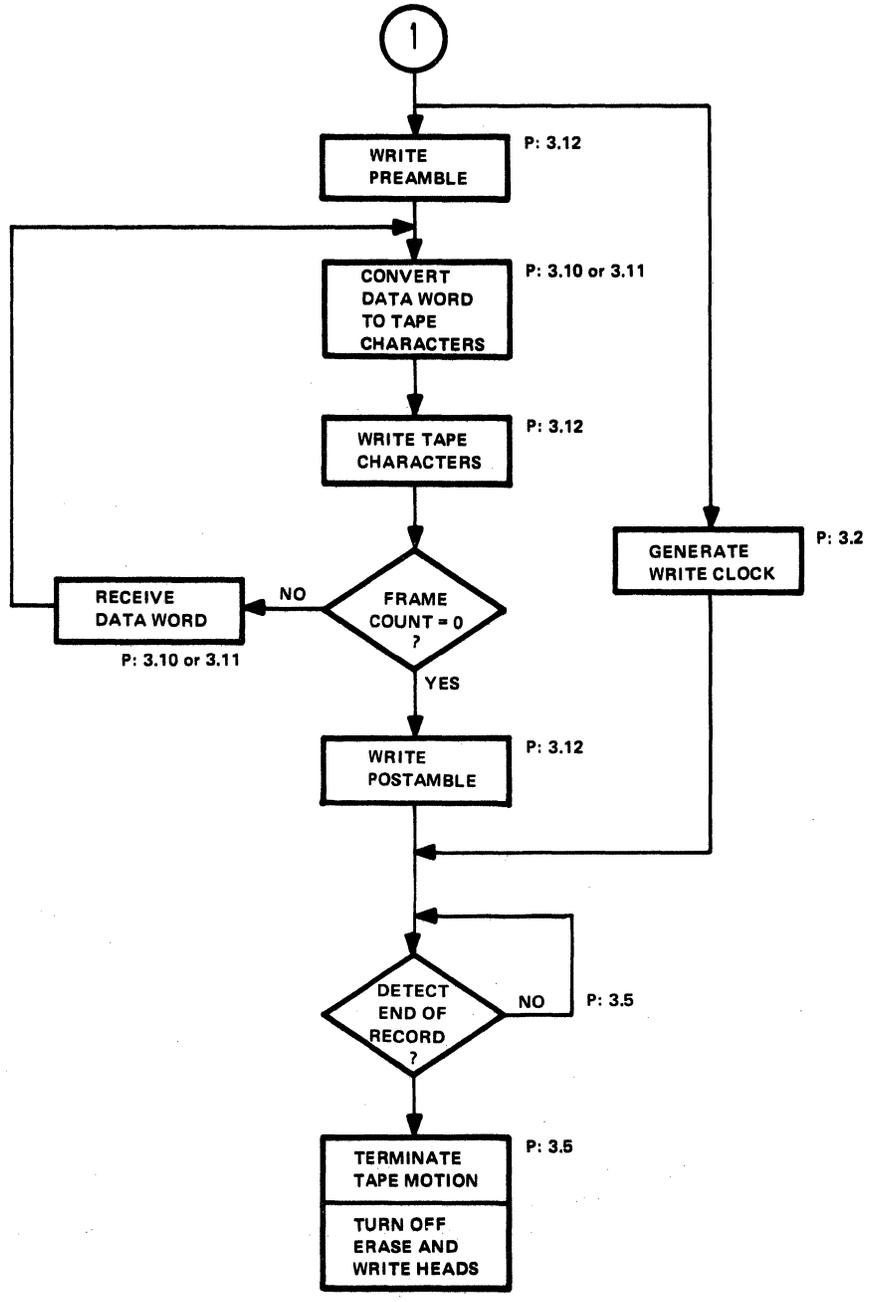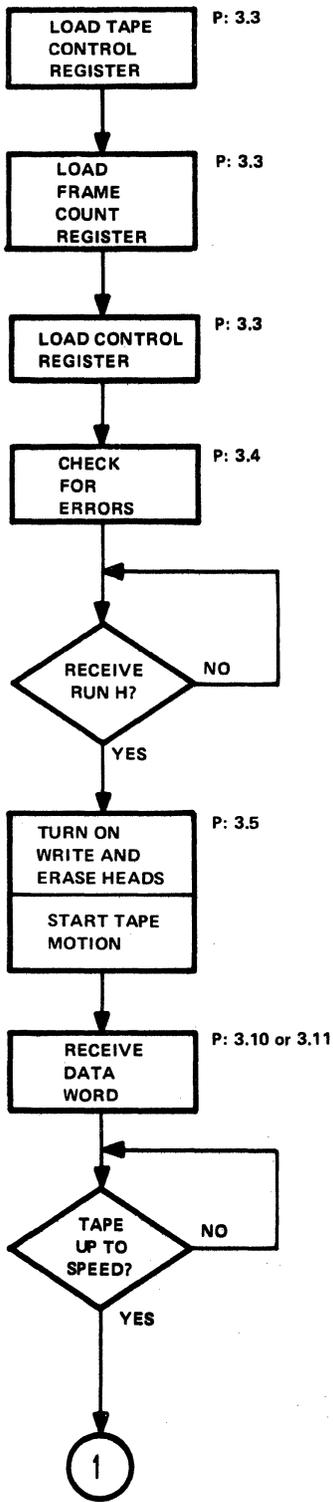
Figure 2-21 PE Data Write Operation Flowchart

0—2) of the slave bus, responds to SLAVE SET Pulse by setting its Forward motion control and Write Enable flip-flops. These flip-flops activate the capstan drive motor for forward tape motion and turn on the write and erase heads.

After a motion delay during which the TU16 erases tape while it comes up to speed, the TM02 negates ACCL L on the slave bus. This notifies the TU16 that it is at speed, and enables it to transmit WRT CLK to the TM02. Upon receipt of WRT CLK, the TM02 begins generating a preamble. When forty all-0 characters and one all-1s character have been written, the Bit Fiddler begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word from the Massbus Controller, and continues to do so until all the data words have been transferred. Each time the Bit Fiddler generates a character, the Frame Count register is incremented, a vertical parity bit is generated, and the tape character is converted to PE mode and transmitted to the write circuitry of the TU16. When the Frame Count register overflows to zero, the TM02 asserts EBL (End of Block) to the controller and generates a postamble which is written on a tape. During the entire operation, the TU16/TM02 read operation is active and reads the record being written.

2.6.6.3 Command Termination — When the TU16/ TM02 read circuitry detects the end of the record, a motion delay is generated at the end of which the TM02 asserts STOP L on the slave bus, resetting the TU16 Forward motion flip-flop, thereby terminating tape motion. STOP L also clears the GO bit of the Control register, which causes OCC to be negated. When tape motion ceases, the Write Enable flip-flop is cleared, and the write and erase heads are de-energized.

2.6.7 NRZ Data Write
Figure 2-22 illustrates the major functional sequences of an NRZ data write operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.7.1 Command Initiation — To initiate an NRZ write operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU16, tape character format, and tape data density. The TM02 places the Slave Select (SS 0—2) and Density (DEN 0—2) bits of the Tape Control register

on the slave bus. The Massbus Controller then loads the 2s complement of the number of tape characters to be written into the TM02 Frame Count register. Following this, the controller loads the Control register with the operational function code (61) of the data write command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM02 responds by asserting SLAVE SET Pulse on the slave bus and accepting the first data word from the controller.

2.6.7.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines (SS 0—2) of the slave bus, responds to SLAVE SET Pulse by setting its Forward motion control and Write Enable flip-flops. These flip-flops activate the capstan drive motor for forward tape motion and turn on the write and erase heads.

After a motion delay during which TU16 erases tape while it comes up to speed, the TM02 negates ACCL L on the slave bus. This notifies the TU16 that it is at speed, and enables it to transmit WRT CLK to the TM02.

Upon receipt of WRT CLK by the TM02, the Bit Fiddler begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word from the Massbus Controller, and continues to do so until all the data words have been transferred. Each time the Bit Fiddler generates a character, the Frame Count register is incremented. A vertical parity bit is generated, the CRCC is generated, and the tape character is transmitted to the write circuitry of the TU16 where it is converted from binary to NRZ mode (1s become transitions) and written on the tape. When the Frame Count register overflows to zero, the TM02 transmits EBL (End of Block) to the controller. It then generates the timing to write the generated CRCC and the LRCC.

During the time that the tape is moving at speed (ACCL L negated), the TU16/TM02 performs a read-after-write operation.

2.6.7.3 Command Termination — When the TU16/ TM02 read circuitry detects the end of the record, a motion delay is generated, at the end of which the TM02 asserts STOP L on the slave bus, resetting the

LOAD TAPE CONTROL REGISTER — P: 3.3

LOAD FRAME-COUNT REGISTER — P: 3.3

LOAD CONTROL REGISTER — P: 3.3

CHECK FOR ERRORS — P: 3.4

RECEIVE RUN H? — NO / YES

TURN ON WRITE AND ERASE HEADS / INITIATE TAPE MOTION — P: 3.5

RECEIVE DATA WORD — P: 3.10 or 3.11

TAPE UP TO SPEED? — NO

1

CONVERT DATA WORDS TO TAPE CHARACTERS — P: 3.10 or 3.11

WRITE TAPE CHARACTERS — P: 3.13

GENERATE CRC CHARACTER — P: 3.13

RECEIVE DATA WORD — P: 3.10 or 3.11

FRAME COUNT = 0 ? — NO / YES

SPACE 3 CHARACTERS AND WRITE CRCC — P: 3.13

SPACE 3 CHARACTERS AND WRITE LRCC — P: 3.13

TERMINATE TAPE MOTION / ERASE IRG / TURN OFF ERASE AND WRITE HEADS — P: 3.5
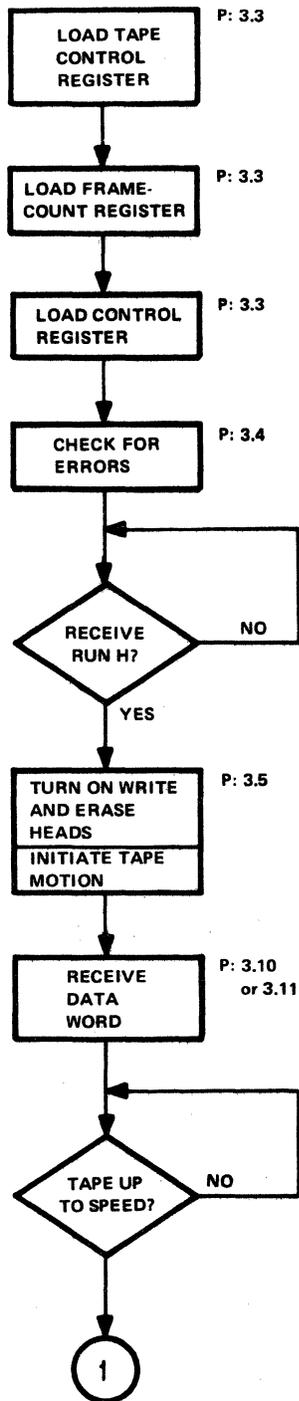
NOTE
P: REFERENCES
CHAPTER 3 PAMPHLET
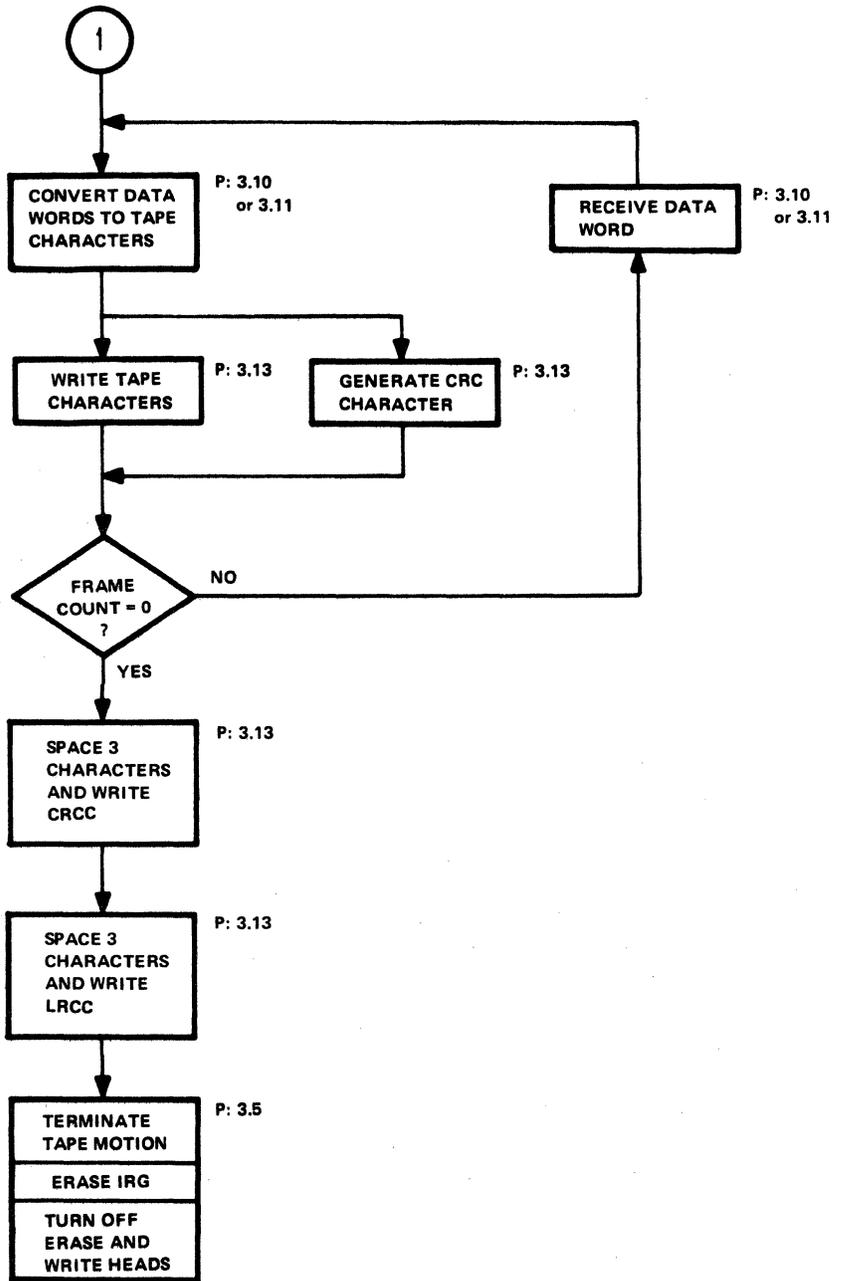
NRZ DATA WRITE

10-1245

Figure 2-22   NRZ Data Write Operation Flowchart

2-33

TU16 Forward motion flip-flop, thereby terminating tape motion. STOP L also clears the GO bit of the Control register, which causes OCC to be negated. When tape motion ceases, the Write Enable flip-flop is cleared and the write and erase heads are de-energized.

2.6.8 Write Tape Mark

The tape mark is a special tape record used to separate data on tape. Although a write tape mark command may be issued at any time, the most common use of this command is as a "software bookmark" to designate the end of a group of related records. It is possible to quickly locate the beginning of a group of related data records by searching the tape for written tape marks. This is accomplished by loading the Frame Count register with a record count larger than the number of records in any existing group of records, and then issuing a space command. The transport will space to the tape mark and terminate motion despite the fact that frame count overflow does not occur.

Figure 2-23 illustrates the major functional sequences of a write tape mark operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.8.1 Command Initiation — To initiate a write tape mark operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, selecting the slave TU16 desired to perform the write tape mark operation and the density at which the tape mark characters are to be written. The TM02 places the Slave Select (SS 0—3) and Density Select (DEN SEL 0—3) bits of the Tape Control register on the slave bus.

The Massbus Controller then loads the TM02 Control register with the operational function code (27) of the write tape mark command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET Pulse to the TU16 and generates a motion delay.

2.6.8.2 Command Execution — The TU16, which is enabled by its address code on the Slave Select lines, responds to SLAVE SET Pulse by setting its Forward motion and Write Enable flip-flops, which activate the capstan drive (starting tape motion) and the write and

NOTE
P: REFERENCES
CHAPTER 3 PAMPHLET
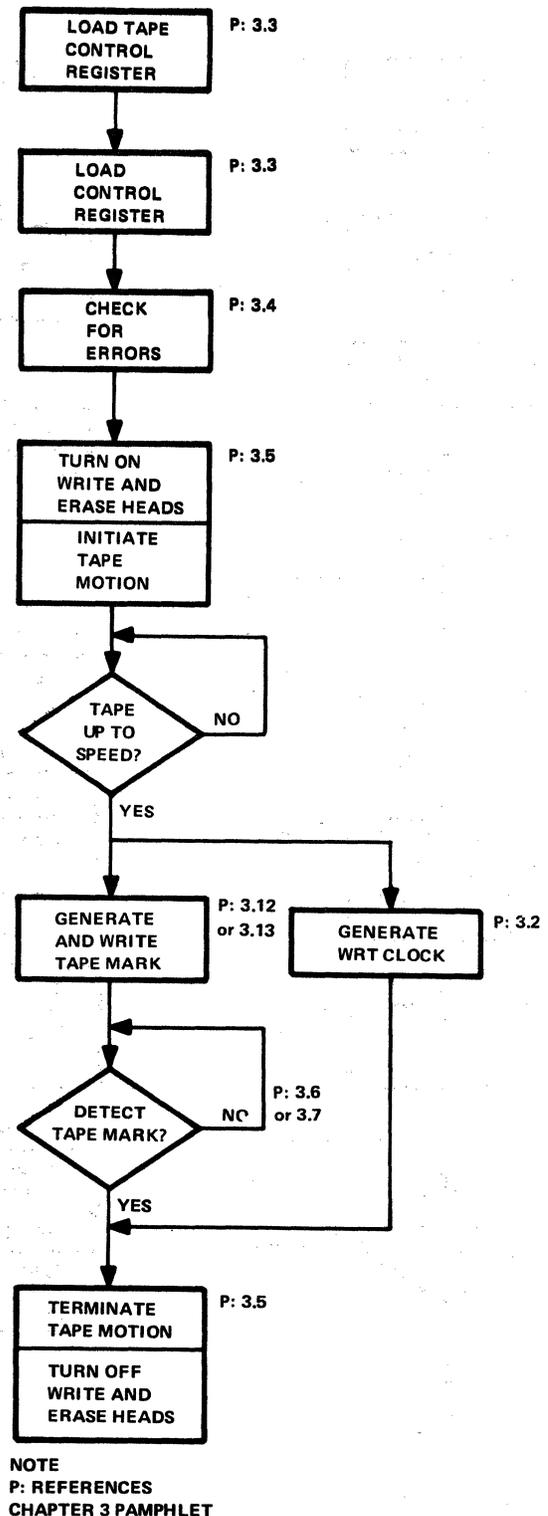
10-1250

Figure 2-23   Write Tape Mark Operation Flowchart

2-34

erase heads. As tape moves past the heads, it is erased. Then, when the motion delay is over, the TCCM module generates the tape mark.

If the TU16/TM02 is operating in PE mode, slave bus write lines WD 3, 4, 6, and 7 are forced low, while PE 0s are generated for WD 0, 1, 2, 5, and P. At the same time, Record pulses (40 X 2 = 80) are transmitted to the TU16. This results in forty 0s being written in tracks 1, 2, 4, 5, and 8, and erasure of the remaining tracks.

If the TU16/TM02 is operating in NRZ mode, the tape mark character is forced onto the slave bus WD lines, and a Record pulse is transmitted to the TU16. The TU16 is then allowed to erase seven character lengths of tape at which time it receives LRC STROBE on the slave bus, and writes an LRCC (which will be the same as the tape mark character).

After writing the NRZ or PE tape mark, the TU16/TM02 continues to erase tape. As the write tape mark operation is performed, the read circuitry performs a read-after-write.

2.6.8.3 Command Termination — When the read circuitry has detected the written tape mark, a motion delay is generated by the TM02, at the end of which STOP L is transmitted to the TU16. STOP L resets the TU16 Forward motion flip-flop, which deactivates the capstan motor, thereby terminating tape motion. When tape motion has ceased, the write and erase heads are de-energized. STOP L also resets the TM02 Control register GO bit.

CHAPTER 3
SERVICING

MAINTENANCE MODES

3.1 INTRODUCTION

This pamphlet discusses TU16/TM02 on-line testing capabilities (Paragraph 3.1.1), diagnostics (Paragraph 3.1.2), and TU16 off-line testing capabilities (Paragraph 3.1.3).

3.1.1 Maintenance Register

The Maintenance register (R3) facilitates on-line diagnostic testing of the TU16/TM02, and allows testing of the TM02 data paths and error discrimination circuitry. A discussion of the Maintenance register bits and their function follows.

1. Bit 0 — Maintenance Mode (MM) — Must be loaded set when any maintenance mode function is desired.

2. Bits 1 to 4 — Maintenance Op Code (MOP 0 to 3) — These four bits determine the maintenance function that will occur if the MM bit is set and the TM02 is loaded with the appropriate command. The op codes that are implemented are:

- 0000 — Null code

- 0001 — Interchange Read (IRD)
  In NRZI mode, this op code causes a more stringent skew check to be made on data during read or write check operations. In PE mode, this op code suppresses on-the-fly correction of data errors.

- 0010 — Even Parity
  Causes even parity to be used on the Control lines of the Massbus.

- 0011 — Global Data Wrap-Around (WRP 0)
  Configures the TM02 data paths as shown in Figure 3.1-1. This causes a write data command to be executed as follows. Data is brought in on the data lines, divided into bytes using the algorithm de-
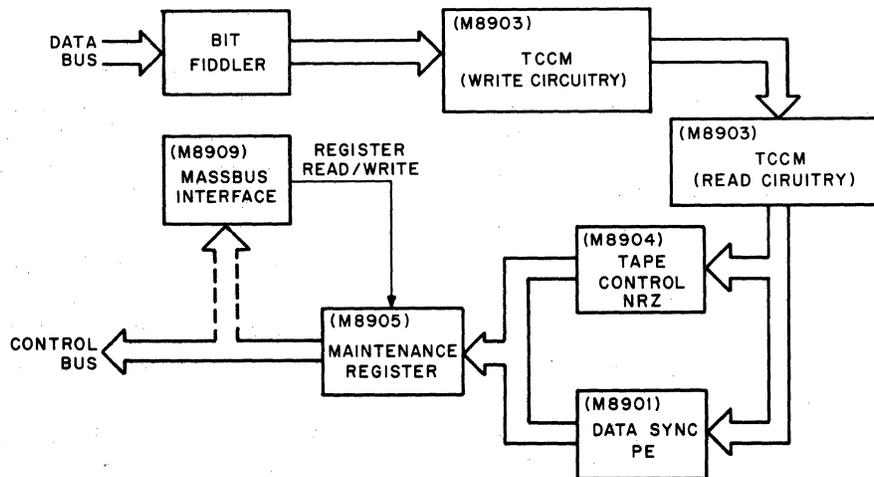
Figure 3.1-1   Global Wrap-Around (WRP 0)

fined by the format code resident in the Tape Control register, formatted as either NRZI or PE write data, multiplexed into the read circuitry, and deposited in the Maintenance Register Data Field.

- 0100 — Partial Data Wrap-Around (WRP 1)
  Configures the TM02 data path as shown in Figure 3.1-2. This causes a write data command to be executed as follows. Data is brought in on the data lines, divided into bytes using the algorithm defined by the format code resident in the Tape Control register, formatted as either NRZI or PE write data, and deposited in the Maintenance Register Data Field.

Figure 3.1-3   Formatter Wrap-Around (WRP 2)

Figure 3.1-2   Partial Wrap-Around (WRP 1)
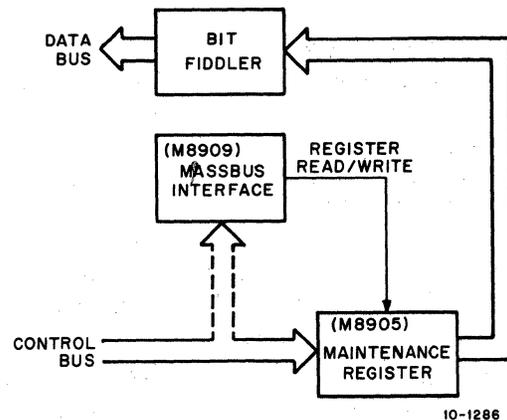
Figure 3.1-4   Formatter Read Wrap-Around (WRP 3)

- 0101 — Formatter Write Data Wrap-Around (WRP 2)
  Configures the TM02 data path as shown in Figure 3.1-3. This causes a write data command to be executed as follows. Data is brought in on the data lines, divided into bytes using the format code resident in the Tape Control register, and deposited in the Maintenance Register Data Field.

- 0110 — Formatter Read Data Wrap-Around (WRP 3)
  Configures the TM02 data path as shown in Figure 3.1-4. This causes a read data command to be executed as follows. Data is taken from the Maintenance Register Data Field, multiplexed into the for-

matting logic byte by byte, formed into data bus words using the algorithm defined by the format code resident in the Tape Control register, and transmitted to the controller.

In addition, the op code suppresses reception of the Massbus WCLK signal. Thus, an attempt to perform a write operation with this op code in the Maintenance register will result in detection of DTE.

- 0111 — Cripple Reception of OCC
  An attempt to perform any data transfer operation with this op code in the Maintenance register will result in detection of DTE.

3.1-2

- 1000 — Illegal Check Character (ILCC)
  In NRZI mode, this op code suppresses initialization of the CRC checking logic, resulting in CRC errors. In PE mode, this op code suppresses detection of data in logical track 1.

- 1001 — Incorrect Tape Mark
  This op code causes bit 5 of tape data bytes to remain in the negated state. In PE mode, this op code suppresses detection of data in logical tracks 1 and 2.

- 1010 — Maintenance Mode End of Record (MMEOR)
  This op code is used to signal the end of a maintenance mode operation, thus causing the GO bit to become negated.

- 1011 — Incorrect Preamble (INC PREAMBLE)
  This code causes logical bit 1 of a PE preamble and postamble to be inverted during a write data command, resulting in generation of invalid preambles and postambles.

3. Bit 5 — Maintenance Mode Clock (MC) — This bit controls the sequencing of data through the TM02 data paths when operating in a maintenance mode.

4. Bit 6 — Two-Hundred CPI Clock (SWC 2) — This bit displays a clock signal which is derived from the crystal oscillator in the selected slave. The frequency of this clock is dependent upon the read/write speed of the selected slave, and is equal to the frequency at which an unbroken chain of ones are written on tape when operating at a density of 200 characters per inch. Frequency of SWC2 (KHz) = (0.2) x (Drive speed in ips). This clock is displayed to aid in monitoring of drive functions during maintenance mode operations.

5. Bits 7 to 15 — Maintenance Data Field (MDF 0—8) — These bits act as buffers for data generated during checks of the TM02 data paths.

Proper operation of the Formatter Wrap-Around Tests is dependent upon three signals from the TU16: CLOCK (SB) L, MOL (SB) L and WRITE CLK (SB) L. Also, any fault (such as grounding data out of GO56) which causes incorrect RSDO pulses will interfere with wrap-around tests. *Verify the status of these signals before doing extensive toubleshotting in TM02.*

3.1.2 Diagnostics

This section introduces the diagnostics supplied with the TU16/TM02 Tape Drive System. For detailed information, refer to the documentation supplied with the diagnostics.

1. TM02/TU16 Control Logic Test, MAINDEC-11-DZTUC and MAINDEC-10-DLTUA

   a. Tests control logic; points to likely fault locations.

   b. Tests the data paths utilizing the maintenance wrap-arounds; points to likely fault locations.

2. TM02/TU16 Basic Function Test — MAINDEC-11-DZTUB and MAINDEC-10-DLTUA — Tests TU16/TM02 functions (read/write/space etc.)

3. TM02/TU16 Data Reliability Program, MAINDEC-11-DZTUA — Writes and reads user-determined data patterns, and thereby tests TU16 and TM02 circuitry. The program provides printouts whenever any errors occur.

4. TM02 Drive Function Timer, MAINDEC-11-DZTUD and MAINDEC-10-DLTUA — Tests for proper tape motion timing (speed, acceleration, deceleration) and data transfer rate.

5. TU16 Utility Driver, MAINDEC-11-DZTUE and MAINDEC-10-DLTUA — (BRUTUS — Brute Force Subroutine) — Performs up to 15 operational functions determined by the user.

6. Data Tape Create, MAINDEC-11-DZTUF-Utility Program Supplement to Random Data Exerciser. Creates a paper tape containing a desired data pattern for use as Pattern 0 of the Random Data Exerciser.

3.1.3 Test Function Generator

The Test Function Generator (TFG) module (M8912) is used for off-line testing of the TU16 Tape Transport. During normal, on-line operation of the TU16, the TFG is only used to transmit the Serial Number and certain Drive-Type bits to the TM02; to do so, it must be located in section EF of slot 3 of the TU16 backplane. The Serial Number and Drive-Type information required is wired on the backplane at this location. For use as an off-line tester, the TFG module must be moved to section AB of slot 3.

REMOVE POWER

REMOVE TFG
FROM SLOT EF3
EXTEND MODULE
IN SLOT AB3

PLACE WRT,
SS WRT, AND SS
RD SWITCHES
IN DOWN
POSITION

RESTORE POWER
AND LOAD TAPE

CONFIGURE S5-9
& S5-10 FOR
DENSITY

WRITE   READ

CONFIGURE DATA
PATTERN IN S5 &
S6

START
-STOP
READ

CONTINUOUS
READ

ENSURE THAT
TEST DATA OUT-
PUT OF TFG IS
PROPERLY
JUMPERED TO
M8910 MODULE
VIA BACKPLANE

INITIATE
FWD OR REV
TAPE MOTION
AT FRONT
PANEL

CONTINUOUS
WRITE

START-STOP WRITE

PLACE SS RD
SWITCH UP MO-
MENTARILY
THEN DOWN
(LOADS DATA
PATTERN)

LOAD FRAME
COUNT INTO
S4 1-8

LOAD FRAME
COUNT INTO
S4 1–8

PLACE WRT
SWITCH UP

SET FRONT
PANEL FWD/
REW/REV
SWITCH
TO FWD

SELECT FWD OR
REV TAPE MO-
TION AT FRONT
PANEL

INITIATE FWD
TAPE MOTION
FROM FRONT
PANEL

PLACE SS WRT
SWITCH UP

PLACE SS RD
SWITCH UP

SET S4-9 TO ON IF
LONG DELAY BE-
TWEEN START-
STOP OPERATIONS
IS DESIRED.
ADJUST R23 AS
DESIRED

*TU16's shipped prior to September 1975 do not
have the "TESTER WRITE DATA" function wired
on the backpanel. For these early units, it will be
necessary to install the following wiring to enable
this function.

FROM	TO
A3-K1	A2-C1
A2-C1	A2-E1
A2-E1	A2-F1
A2-F1	A2-J1
A2-J1	B2-H1
B2-H1	B2-J1
B2-J1	B2-P1
B2-P1	B2-R1
B2-R1	C2-M2

10-1337

Figure 3.1-5   TFG Operating Procedure Sequence

3.1-4

An operating procedure for the TFG is presented in flowchart form in Figure 3.1-5. Figure 3.1-6 provides additional information on TFG switch settings. The TFG module is illustrated in Figure 3.1-7.

As an off-line tester, The TFG module (Figure 3.1-7) controls tape motion, enables TU16 read and write circuitry, and generates test patterns to be written on tape. Three modes of operation are possible:

1. Start-Stop Read (SS RD) — When the SS RD switch (S3) is activated (raised), tape motion is initiated; a record of predetermined length is read; tape motion is then terminated. This cycle is repeated as long as the SS RD switch is up.

2. Start-Stop Write (SS WRT) — When the SS WRT switch (S2) is activated (raised), tape

MODE	S5-9 TEST PE	S5-10 TEST DEN
238 bpi NRZ	ON	ON
800 bpi NRZ	ON	OFF
1277 bpi PE	OFF	ON
1600 bpi PE	OFF	OFF
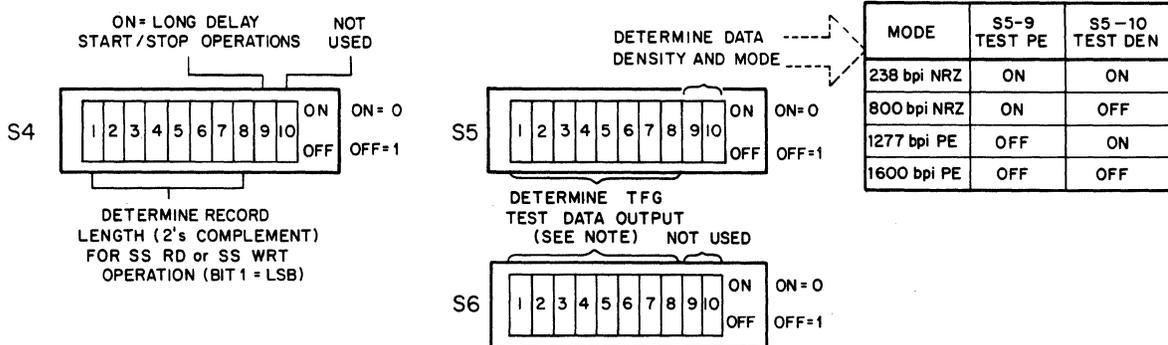
NOTE: If the data is to be written in PE mode, the phase encoding must be implemented by the switch configuration. Thus, while in NRZ mode an all 1s pattern is generated by setting the switches to OFF, in PE mode the same pattern is achieved by alternating the states of consecutive switches.

Figure 3.1-6 TFG Switch Settings

10-1341

SS RD
WRT
SS WRT
LED
R23*
S5
S6
S4
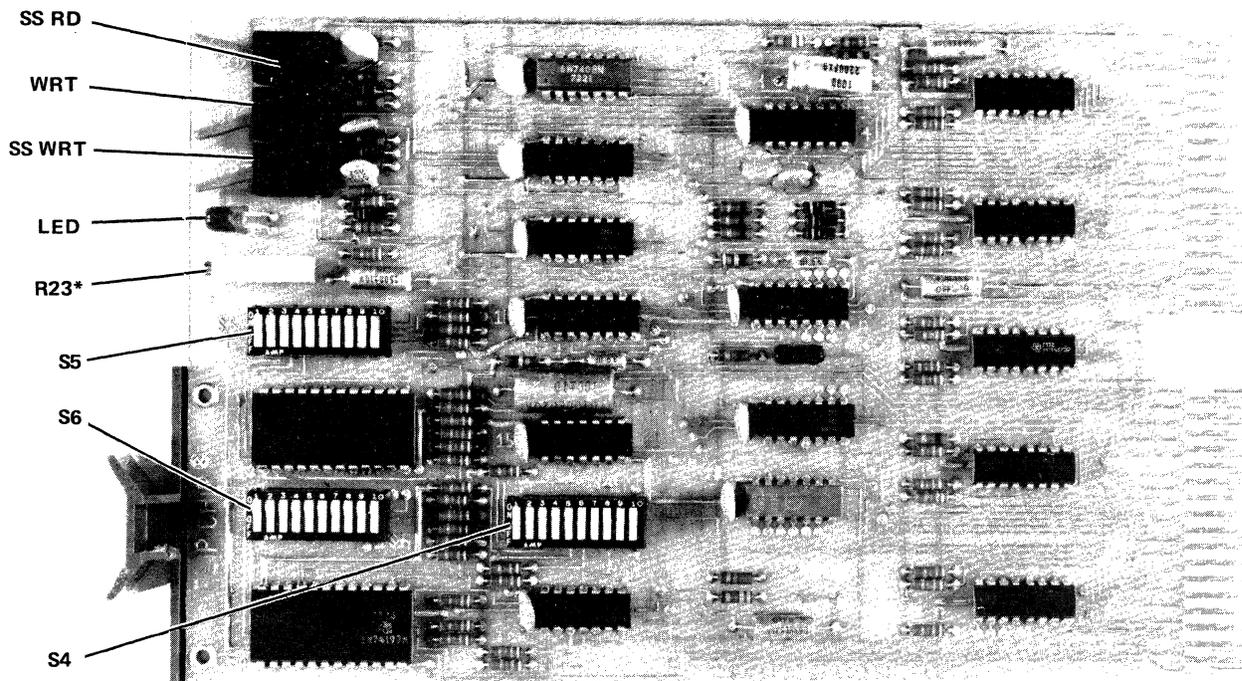
*Adjusts start-stop time.

6999-5

Figure 3.1-7 Test Function Generator Module

3.1-5

motion is initiated; a record of predetermined length, consisting of preselected characters, is written on tape; tape motion is then terminated. This cycle is repeated as long as the SS WRT switch is up.

3. Continuous Write (WRT) — When the WRT switch (S1) is activated (raised), power is supplied to the write drivers and they are continuously driven with a preselected pattern. Tape motion is controlled from the front panel.

When the tester card is located in the TU16 module, location AB, the pin labeled TESTER ENABLE L is at ground potential (drawing M8912, sheet 3). This enables the TEST PE H and TEST DEN H switches. With the LED on, the TEST PE H and TEST DEN H switches affect the recording density as controlled by the M8911 Slave Clock module. The TESTER ENABLE L level asserts LOCAL H, preventing the transport from going on-line.

An eight-bit counter, constructed from two 74197 up-counters, controls a preset record length. The preset count is entered from the S4 switches [S4 (1—8)]. Both the SS RD and SS WRT functions use the counter to control record length. The WRT function is continuous and does not use a preset panel.

A 16-bit shift register, constructed from two 74199 8-bit shift registers, allows various data test patterns to be generated. Switches on S5 and S6 select the data pattern to be loaded into the register. When shifted out, the test data patterns (TEST DATA A H and L and TEST DATA B H and L) are wired to the Data Multiplex on the LAW module (M8910) and written on tape.

The start-stop repetition rate during SS RD and SS WRT can be modified by adjusting R23. The range of adjustment is determined by switch S4, segment 9.

3.1.3.1 Theory of Operation — The following paragraphs describe the theory of operation of the TFG module in its three functional modes. The discussions reference the TFG schematic (TFG 3).

SS RD Function — Figure 3.1-8 illustrates SS RD timing. When the SS RD switch (S3) is closed, E1 - pin
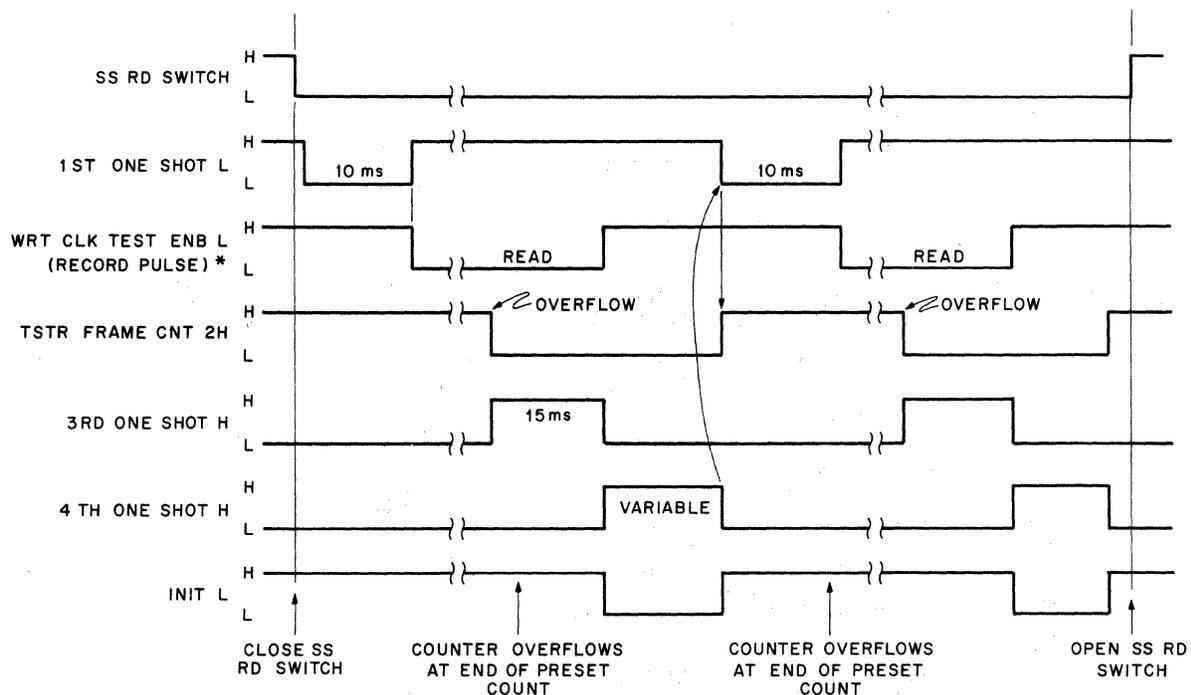
*RECORD PULSE L PULSES OCCUR DURING WRT CLK TEST ENB L.

10-1298

Figure 3.1-8 SS RD Function

10 goes low and triggers the First One Shot delay. FIRST ONE SHOT L, input to the LAW module (M8910), initiates tape motion; the direction of tape motion is determined by the direction switch on the TU16 control box. FIRST ONE SHOT also presets the 8-bit counter (E15 and E22) and loads the 16-bit shift register (E13 and E23).

When the First One Shot delay times out, flip-flop E8 is clocked set and asserts WRT CLK TEST ENB L. This signal is used in the Slave Clock and Motion Delay module (M8911) to enable WRT CLK and RECORD PULSE L pulses. The RECORD PULSE L pulses now clock the TFG 8-bit counter and 16-bit shift register. When the counter overflows, the Third One Shot delay is triggered and negates WRT CLK TEST ENB L, inhibiting further RECORD PULSE L pulses.

When the Third One Shot delay times out, FOURTH ONE SHOT H is generated, and causes tape motion to terminate. When the Fourth One Shot delay times, the First One Shot is again triggered; the cycle begins again. The start-read-stop cycle continues as long as the SS RD switch is depressed.

SS WRT Function — Figure 3.1-9 illustrates SS WRT timng. The Start-Stop Write function operates in a manner similar to the SS RD function, except that SET TEST WRE L is asserted along with WRT CLK TEST ENB L. SET TEST WRE L causes the write and erase heads to be energized. When RECORD PULSE L pulses clock the shift register (E13 and E23), the contents of the register are rotated. The shift register outputs (TEST DATA A H and L and TEST DATA B H and L) can be jumpered to the LAW Data Write Multiplex and written on tape.

Continuous Write Function — The continuous write function works differently than the SS WRT function in that in the continuous test mode, no starting and stopping occurs. One continuous write operation commences with the setting of the WRT switch and ends with the opening of the switch. Tape motion (starting and stopping) is controlled at the Control Panel.

As the WRT switch is closed, WRT CLK TEST ENB L and SET TEST WRE L are asserted. This enables RECORD PULSE L pulses and passes write current to the heads. The eight-bit counters are not used in the
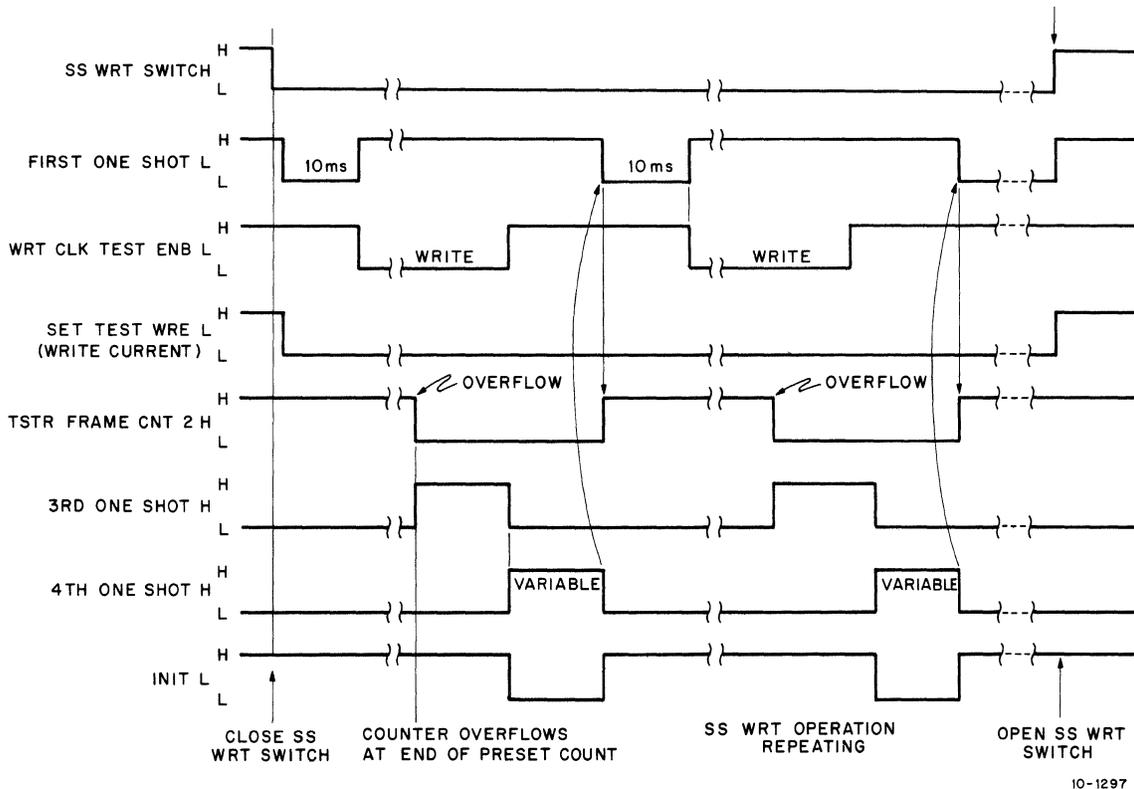
Figure 3.1-9   SS WRT Function

continuous write operation. Instead, the shift registers are clocked by inverted RECORD PULSE L pulses and whatever data pattern was in the shift register switches is shifted out on the TEST DATA lines to be written and observed. The THIRD ONE SHOT delay is inhibited which eliminates the start-stop operations.

If the operator desires a test data pattern other than the pattern presently in the shift register switches, he must first run a SS RD operation with the desired test data pattern. It is the only method for loading new information from the switches into the shift register.

The continuous write operation continues until the WRT switch is opened; this clears the WRT flip-flop and removes the write current and record pulses.

CLOCKS

CONTENTS

3.2.1 System Clocks

All free-running system clock waveforms used in the TU16/TM02 are generated from a 2.3-MHz, crystal controlled clock located on the TU16 Slave Clock and Motion Delay module (M8911). The 2.3-MHz clock is divided down to 144 kHz, and is transmitted to the TM02 via the slave bus [CLOCK (SB)] by an on-line, selected transport loaded with tape. On the Tape Control Common Mode (TCCM) module (M8903), this 144-kHz clock is further divided to provide:

DATA HALF	72 kHz
800 BPI CLK	36 kHz
200 BPI CLK	9 kHz

These clocks perform various housekeeping functions in the TM02. For example, 800 BPI CLK clocks the Motion Delay Counter (TCCM 3); 200 BPI CLK counts the IDB Counter, Write End Counter, and Shutdown Counter.

DATA HALF is essentially a 1600-bpi clock, and is used in functions pertaining to PE mode. For instance, it clocks the Character Counter on the Tape Control-PE module (TCPE 4).

3.2.2 Write Clock

The TU16/TM02 is capable of reading and writing data at several bit densities. To do this, a separate clock signal, whose frequency depends on the tape data density, must be developed; WRT CLK is this signal. WRT CLK is transmitted to the TM02 by a selected, powered TU16, loaded with tape and running at speed (except during a rewind). It is used in the TM02 to produce the following clock signals:

WB CLK	Clocks the TCCM Write Buffer (TCCM 2)
ST CLK	Used to generate PE write data states in the Tape Control-PE module (TCPE 2)

PE CLK   Used in PE mode to control TCCM Write Multiplex (TCCM 2).

WRT CLK is generated in the following manner. A number is preset into a 74161 (synchronously loaded) binary counter (SC 3), which is then upcounted at 575 kHz. When the counter overflows, WRT CLK H is asserted and causes the counter to be preset at the leading edge of the next 575-kHz clock pulse. With the counter preset, WRT CLK will be negated by the trailing edge of that same 575-kHz clock pulse. The counter will be clocked up as before, until overflow, and the cycle is repeated.

The presets of the 74161 counter are determined by various signals and conditions. These are listed in Table 3.2-1, along with the resulting counter presets, WRT CLK frequency, and density. Note that WRT CLK frequency for 1600 bpi is four times that of 800 bpi. This is because 1600 bpi is used only in PE mode, and PE mode requires a double frequency WRT CLK.

Obviously, the frequency of the cycle will vary with the magnitude of the preset. Figure 3.2-1 shows timing diagrams for presets of -1 (-n=2s complement of n), -2, and -3. Note that for a preset of -n, the frequency of WRT CLK, $f_{WRT\,CLK} = [575/(n+1)]$ kHz.

3.2.3 Performance Checks

Verification of the clock system is accomplished as follows:

1. With a TU16 selected, loaded and on line, observe with an oscilloscope, a 9 kHz square wave at F0651 of the TM02.

2. Completion of Drive Function Timer diagnostic without out-of-range errors. (The diagnostic may fail for reasons other than the clocks. Troubleshooting a failure should begin with the diagnostic printout.)

3.2.4 Adjustments
None.

3.2.5 Troubleshooting
Figure 3.2-2 provides a guide for analyzing particular troubles using the engineering drawing set. Careful evaluation of the trouble symptoms and good trouble-shooting judgement are necessary to successfully apply Figure 3.2-2 to practical troubleshooting situations.

Table 3.2-1
Write Clock Frequencies

	DEN 2	DEN 1	DEN 0	Test PE	Test DEN	WRT CLK Counter Presets		Frequency kHz (bpi)
						LSB	MSB	
On-Line	0	0	0	1	1	10000011		9 (200)
	0	0	1	1	1	01010111		28 (556)
	0	1	0	1	1	10001111		36 (800)
	0	1	1	1	1	10001111		36 (800)
	1	0	0	1	1	10111111		144 (1600)
	1	0	1	1	1	00111111		115 (1277)
	1	1	0	1	1	10111111		144 (1600) } Rese
	1	1	1	1	1	10111111		144 (1600)
Off-Line	x	x	x	0	0	01010011		10.7 (238)
	x	x	x	0	1	10001111		36 (800)
	x	x	x	1	0	00111111		115 (1277)
	x	x	x	1	1	10111111		144 (1600)

Figure 3.2-1   WRT CLK Generation Timing

A. STEADY STATE CLOCK SIGNALS

START

SC2
144 kHz SQUARE WAVE CLOCK (SB) L @ C03M2 OF TU16 — NO →

YES

TCCM4
CLOCK H @ A07M1 OF TM02 — NO →

YES

TCCM4
200 BPI CLOCK (9 kHz) @ E07H2 AND DATA HALF H (72 kHz) @ E07P2 OF TM02 — NO →

YES

STEADY STATE CLOCK SIGNALS OK

M8908YA M8913
REPAIR OR REPLACE CABLE OR CABLE MODULES

TCCM4
REPAIR OR REPLACE M8903

SC2
LAW6 MOL H ASSERTS @ C03P1 OF TU16 — NO →

YES

REPAIR OR REPLACE M8911 OR REPAIR CABLE SHORT

LAW6
DIAGNOSE REASON FOR NO MOL

B. WRITE CLOCK SIGNALS

START

SC3
DOES WRT CLK (SB) L SWITCH @ D03M2 OF TU16 — NO →

YES

DOES WRT CLK (SB) L FREQUENCY OBEY TABLE 3.2-1 — NO →

YES

TCCM4
DOES WRT CLK GET TO C07D2 OF TM02 — NO →

YES

THE CLOCKING SIGNALS DERIVED FROM WRT CLK ARE ON TCCM4

SC3
ACCL (SB) L NEGATED AFTER OPERATION IS INITIATED — NO →

YES

SC3
REAPIR OR REPLACE M8911 OR CABLE LINE

DIAGNOSE FAILURE OF ACCL(SB)L TO NEGATE. SEE TAPE MOTION, PARAGRAPH 3.5.

REPAIR SLAVE CABLE OR CABLE MODULE

10-2018

Figure 3.2-2   Clock Troubleshooting

REGISTER READING AND WRITING

CONTENTS

3.3   INTRODUCTION

The Massbus Controller performs register transfers to control and determine the status of the TU16/TM02. These register transfers are performed on the control bus of the Massbus.

3.3.1   Register Write

The Massbus Controller writes into TM02 registers to control TU16/TM02 operations. To accomplish a register write (Figures 3.3-1 and 3.3-2), the controller simultaneously:

- Places a three-bit address code on the Drive Select lines.

- Places the five-bit register select code of the desired register on the Register Select lines.

- Places the information to be written on the Control lines.

- Places a parity bit (odd parity) on the CPA line. This parity bit is associated with the data on the Control lines.

- Asserts CTOD H.

The controller now waits for these signals to settle (325 ns) and then asserts DEM H.

All drives daisy-chained on the Massbus examine the Drive Select lines (MBI 2), but only the drive whose unit select jumper block configuration corresponds to the signals on the Drive Select lines is conditioned to respond to DEM H. All drives decode the Register Select lines, but only the selected drive will utilize the information on these lines.

When DEM H is received by the selected TM02, a 200-ns PULSE H is generated, which produces ASYC WRT L (also of 200-ns duration).

In the meantime:

1. The TM02 has checked for control bus parity (MBI 4) (M8909, sheet 4) and, if detected, a parity error SET CMB PE L has been asserted.

2. The TM02 has decoded the Register Select lines and generated Rn L (MBI 2) (where n designates the selected register). If Rn is a nonexistent register, SET ILR (Set Illegal Register) is generated.

3. If Rn is not R3 (Maintenance register) or R4 (Attention Summary register) and GO L is asserted (i.e., an operation other than rewind is being executed), then the TM02 generates SET RMR (Set Register Modification Refused), (MBI 2).

If neither SET ILR or SET RMR has been asserted, ASYC WRT L generates REG WRT L. REG WRT L, along with Rn L, load the selected register with the data on the Control lines. If SET CMBPE, SET ILR, or SET RMR were asserted, the corresponding bits in the Error register are set (MBI 11).

The trailing edge of PULSE L triggers a 70-ns one-shot (MBI 2). When the 70-ns one-shot times out, TRA is asserted and transmitted to the Massbus Controller. This signal, when received by the Massbus Controller, notifies it that the write sequence in the TM02 is over. The controller therefore negates DEM H and this in turn negates TRA (MBI 1); the register transfer is over.
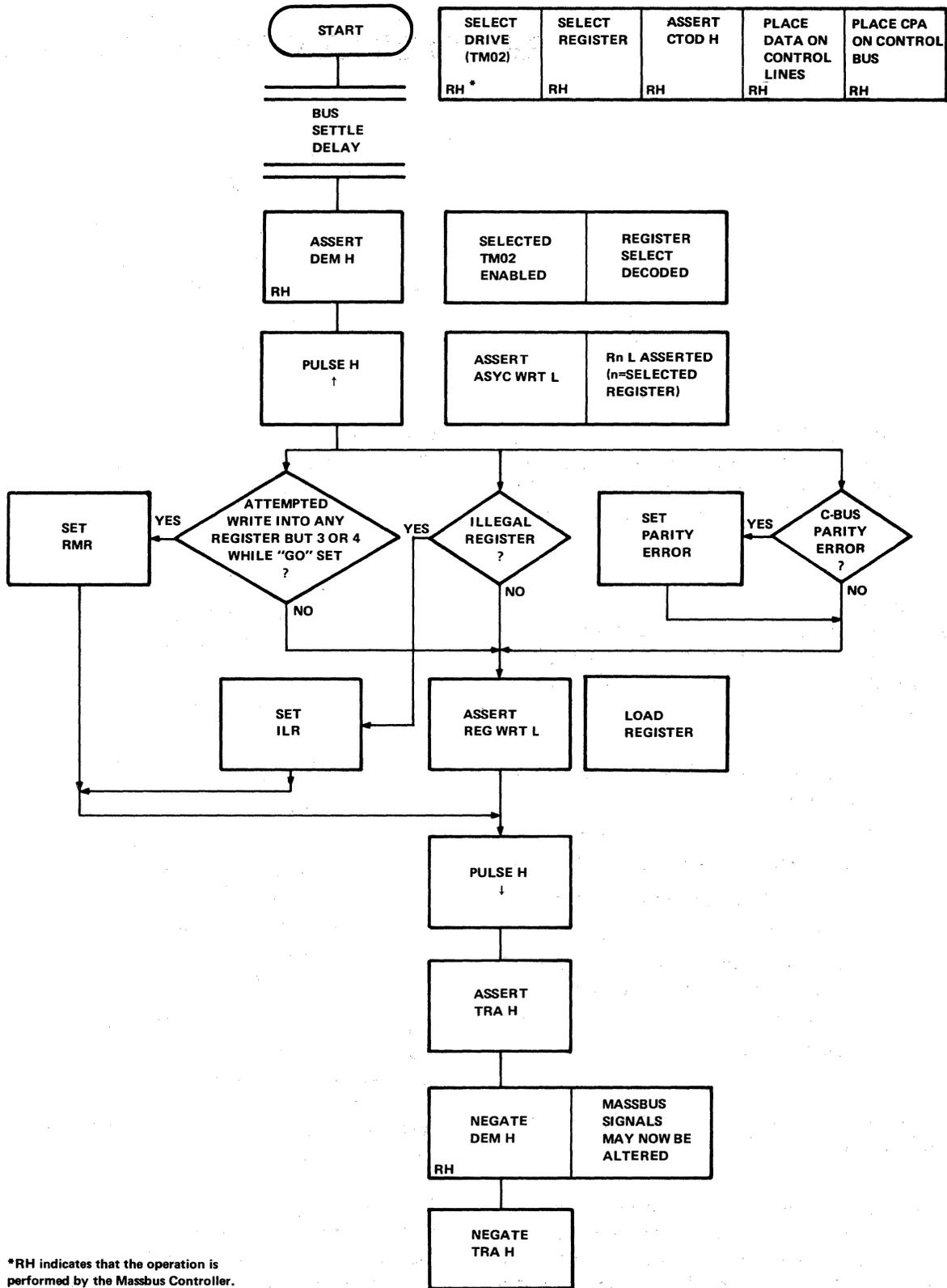
Figure 3.3-1   Register Write Flowchart
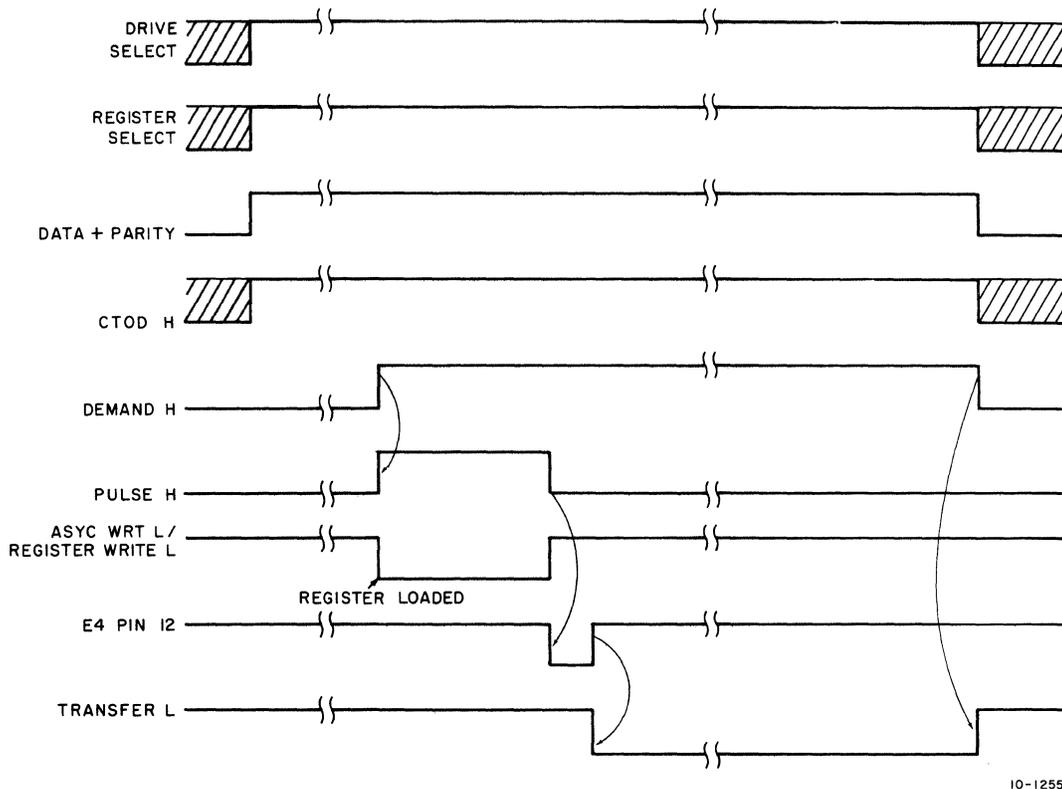
Figure 3.3-2   Register Write Timing Diagram

3.3.2 Register Read

The Massbus Controller can read any TM02 register to determine the status of the TU16/TM02. To do so (Figures 3.3-3 and 3.3-4), the controller simultaneously:

- Places a three-bit drive address code on the Drive Select lines.

- Places the five-bit register select code of the desired register on the Register Select lines.

- *Negates* CTOD H.

The controller now waits 325 ns for these signals to settle on the Massbus and then asserts DEM H.

Drive select recognition and register select recognition occur in the same way as for a register write (MBI 2); only the selected TM02 will respond.

When DEM H is received by the selected TM02, a 200-ns PULSE H is generated. If a nonexistent register is decoded on the Register Select lines, SET ILR H will be generated, and, on the leading edge of PULSE H, the ILR bit of the Error register will be set. If a legal

register has been addressed, Rn L (as decoded from the Register Select lines, where n is the selected register) will multiplex the bits of the selected register to the Control Line Latches (MR4 and Figure 3.3-5).

The register multiplexers are located on several of the TM02 logic modules, but their outputs are "common collectored." Table 3.3-1 lists the location in the engineering drawing set of the various multiplexers.

The trailing edge of PULSE L triggers a 70-ns one-shot, (MBI 2) which causes LCTOD L to be asserted. LCTOD loads the Control Line Latches with the multiplexed register contents and gates the register contents onto the Control lines.

When the 70-ns one-shot times out, TRA is asserted and transmitted to the Massbus Controller. Upon receipt of TRA H, the controller strobes in the data on the Control lines and negates DEM H. DEM H, a low, nehates TRA L in the TM02, and also negates LCTOD L. With LCTOD L negated, the type 74173 Control Line Latches produce high level (+5 V), *high impedance* outputs.

```
   ┌─────────────┐        ┌──────────────┬──────────────┬──────────────┐
   │    START    │        │  SELECT      │  NEGATE      │  SELECT      │
   └─────────────┘        │  DRIVE       │  CTOD H      │  REGISTER    │
          │               │  (TM02)      │              │              │
   ═══════╪═══════        │              │              │              │
          │               │  RH *        │  RH          │  RH          │
        BUS               └──────────────┴──────────────┴──────────────┘
       SETTLE
       DELAY
   ═══════╪═══════
          │
   ┌─────────────┐        ┌──────────────┬──────────────┐
   │   ASSERT    │        │  SELECTED    │  REGISTER    │
   │   DEM H     │        │  TM02        │  SELECT      │
   │             │        │  ENABLED     │  DECODED     │
   │  RH         │        │              │              │
   └─────────────┘        └──────────────┴──────────────┘
          │
   ┌─────────────┐        ┌──────────────┬──────────────┐
   │   PULSE H   │        │  Rn L ASSERTED│  MULTIPLEX   │
   │     ↑       │        │  (n=SELECTED │  SELECTED    │
   │             │        │  REGISTER)   │  REGISTER    │
   └─────────────┘        └──────────────┴──────────────┘
          │
┌────────┐     YES   ╱◇╲
│  SET   │◄───────  ╱ILLEGAL╲
│  ILR   │          ╲REGISTER╱
│        │           ╲  ?  ╱
└────────┘            ╲◇╱
    │                  │ NO
    │                  ▼
    │           ┌─────────────┐
    └──────────►│   PULSE H   │
                │     ↓       │
                └─────────────┘
                       │
                ┌─────────────┐        ┌──────────────┐
                │   ASSERT    │        │  LOAD C-LINES │
                │   LCTOD L   │        │  OUTPUT      │
                │             │        │  LATCH       │
                └─────────────┘        └──────────────┘
                       │
                ┌─────────────┐
                │   ASSERT    │
                │   TRA H     │
                │             │
                └─────────────┘
                       │
                ┌─────────────┐        ┌──────────────┐
                │   NEGATE    │        │  STROBE IN   │
                │   DEM H     │        │  C-LINES     │
                │             │        │  DATA        │
                │  RH         │        │  RH          │
                └─────────────┘        └──────────────┘
                       │
                ┌─────────────┐        ┌──────────────┐
                │   NEGATE    │        │  NEGATE      │
                │   TRA H     │        │  LCTOD L     │
                │             │        │              │
                └─────────────┘        └──────────────┘
```

*RH indicates that the operation is
performed by the Massbus Controller.

10-1261

Figure 3.3-3   Register Read Flowchart

3.3-4

Table 3.3-1
Register Locations

Register	Bit Source		Multiplexer	
	Drawing	**Sheet**	**Drawing**	**Sheet**
00 Control	M8909	5	M8905	6
01 Status			M8903	7
02 Error	M8909	11	M8909	10
03 Maintenance	M8905	2,3,5	M8905	4
04 Attention Summary	M8909	3		
05 Frame Count	M8909	8	M8909	10
06 Drive Type	M8912	2	M8903	7
07 Check Character	M8905 and M8901	3 3,5,7	M8905	4
10 Serial Number	M8912	2	M8903	7
11 Tape Control	M8905	6	M8903 and M8905	7 6
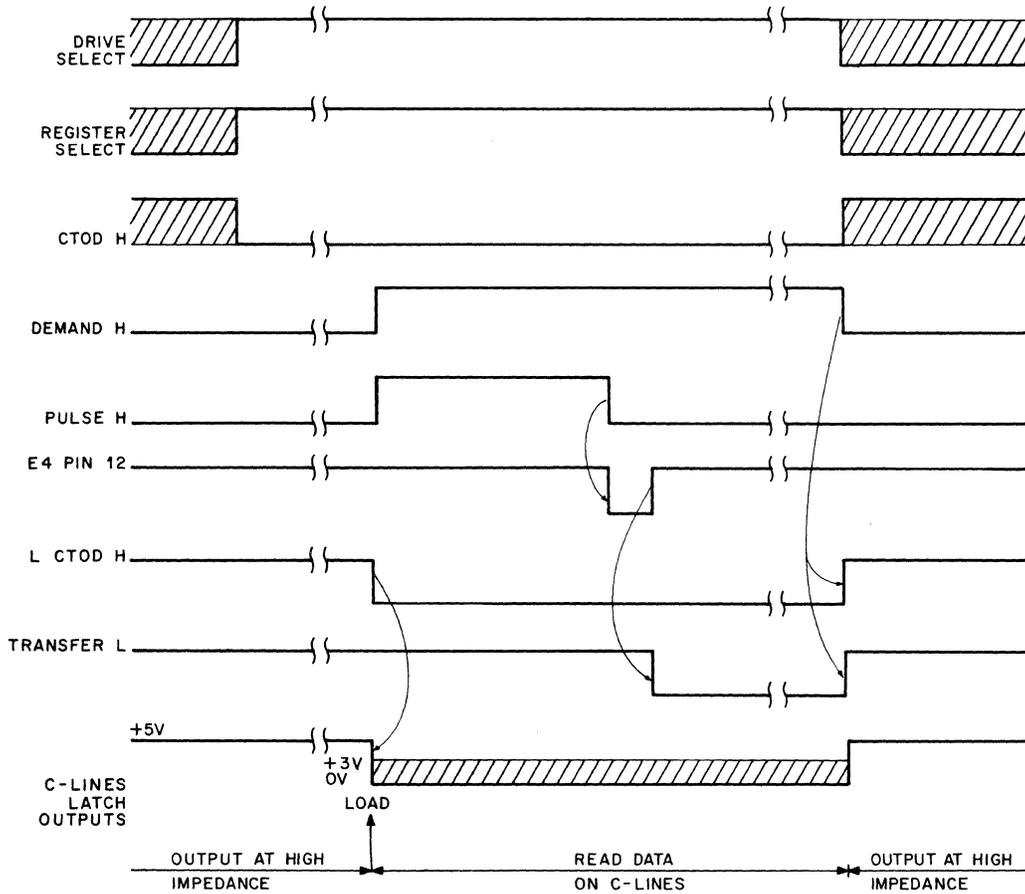
Figure 3.3-4   Register Read Timing Diagram
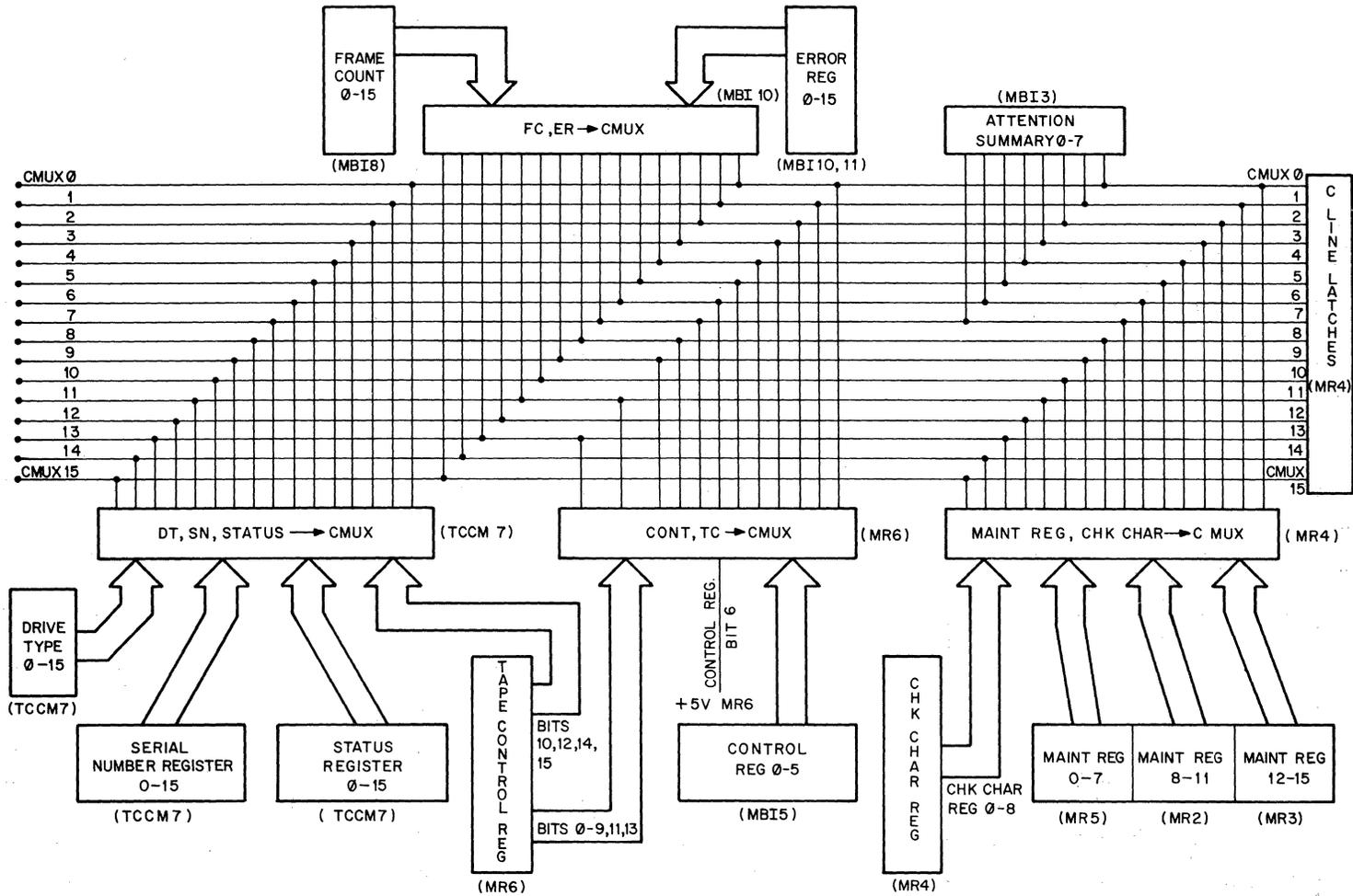
Figure 3.3-5   Register Read Multiplexing

10-1304

3.3.3 Attention Summary Register (R04)

The Attention Summary register is shared by all TM02s (and other drives) that are connected to a particular Massbus Controller. Therefore, when reading or writing this register, it is not required to place any address code on the Drive Select lines of the Massbus. Each TM02 is enabled to respond when it decodes R4 L from the Register Select lines. It should be noted, however, that the DEMAND-TRANSFER "handshake" is carried on in the normal manner by the TM02.

3.3.3.1 Register 04 Read

To read the Attention Summary register, the Massbus Controller performs its usual register read sequence; however, no particular TM02 address code need be placed on the Drive Select lines. When each TM02 decodes R4 L (MBI 2) from the Register Select lines, it places its ATA (Attention Active) status bit on one of the Control lines of the Massbus; which Control line is determined by the unit select plug configuration (unit number) of the particular TM02.

A type 74145 BCD decoder (MBI 3 and Figure 3.3-6) multiplexes the ATA bit onto the proper Control line. Inputs D0, D1, and D2 of the decoder are the unit select (US0—2) configuration of the TM02. If register 4 is being read and the ATA bit is asserted, input D3 is low (units 0 and 2 in Figure 3.3-6). The input to the BCD decoder is therefore the unit select configuration; the appropriate output is asserted low, but is later inverted by the Massbus Drivers.

If the ATA bit is not asserted (unit 1 in Figure 3.3-6), D3 is high and the decoder decodes 8 or higher (8 + n for unit n). Since only outputs 0—7 of the decoder are used, this condition will not produce a high on the Control lines.
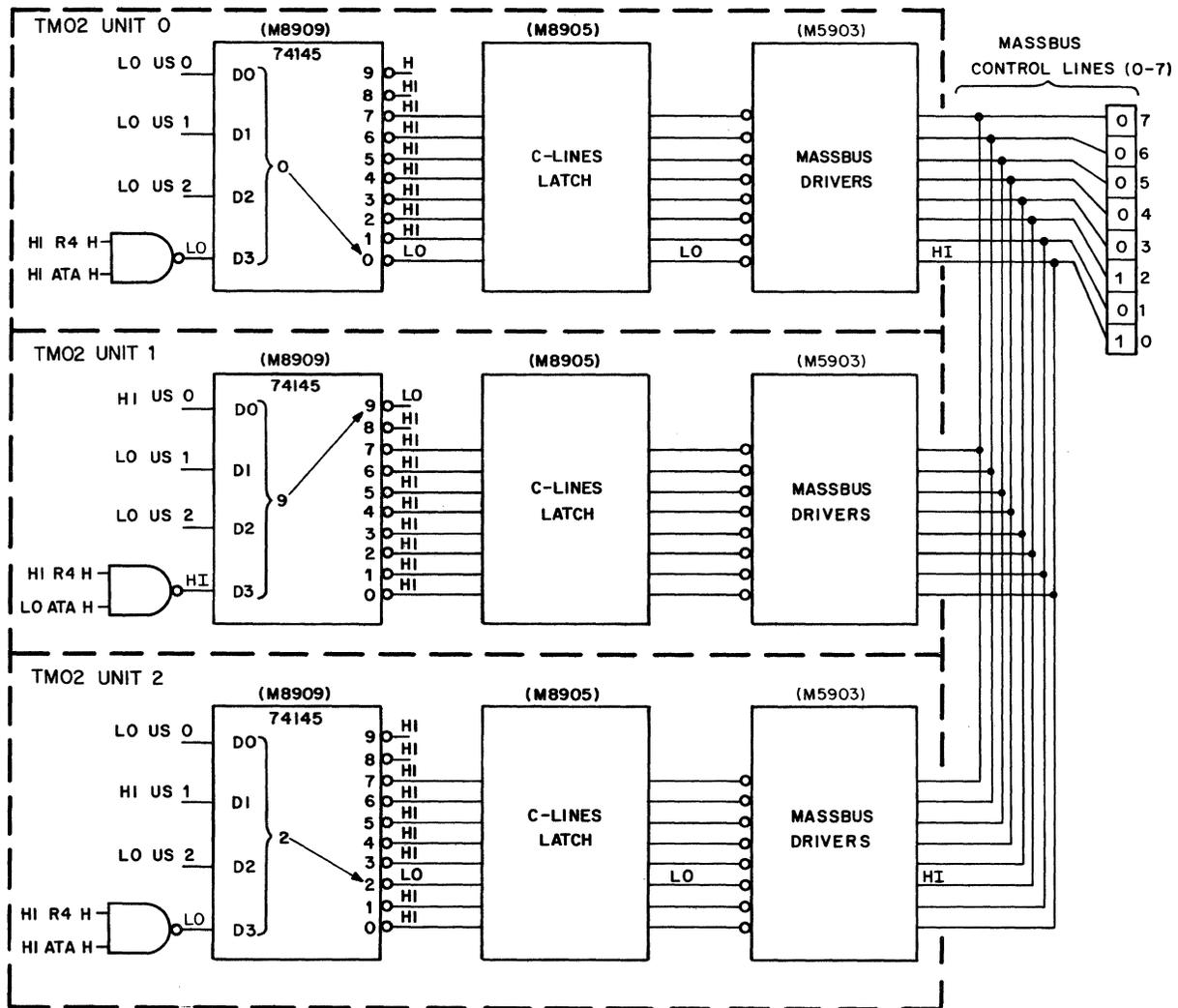
Figure 3.3-6 Attention Summary Register Read

10-1257

3.3-7

3.3.3.2 Register 04 Write — To write the Attention Summary register, the Massbus Controller performs the usual register write sequence. However, it need not specify a particular TM02 on the Drive Select lines. The DEMAND-TRANSFER handshake is carried out in the normal manner, but TM02 internal operation is slightly different.

When REG WRT L is generated, one of the Control lines is multiplexed (MBI 3) into the TM02. If the signal on the Control line is high, it resets the ATA flip-flop; if it is low, it has no effect. The Control line is selected by the unit select configuration (US 0—2) of the particular TM02, input to a type 74151 multiplexer.

3.3.4 Performance Checks
Most of the circuitry used to read and write registers is exercised by the TM02/TU16 Control Logic Test diagnostic (see Paragraph 3.1.2).

3.3.5 Adjustments
None.

3.3.6 Troubleshooting
For troubleshooting register read and register write operations, use the flowcharts in Figures 3.3-1 and 3.3-3; the information in Figures 3.3-2, 3.3-4, 3.3-5 and 3.3-6; and the data provided in the documentation with the TM02/TU16 Control Logic Test diagnostic (see Paragraph 3.1.2). Refer to Table 3.3-2 for more troubleshooting information.

Table 3.3-2
Register Reading and Writing Troubleshooting

Item	Symptoms:	Check For: —
1	Massbus controller sets NED, or constant MCPE.	• Software selecting proper TM02 address. • Proper TM02 address getting to TM02 and being acknowledged (Is E8-3 and MBI2 high?). • Is demand getting to TM02? ((Is DEM H asserted at MBI2?). • Is transfer generated and reaching Massbus controller? (MBI2, MB2).
2	ILR bit sets.	• Register select lines and register select decoder (MBI2).
3	Data in register read incorrectly without CPAR error.	• Problem with C mux lines, C-line latches or register flops (see Figure 3.3-5). • Problem on processor bus.
4	Data in register read incorrectly with CPAR error.	• Massbus cables or transceivers (MB1, MB2, MB3). • No -15 Vdc at controller.
5	Access to only every second register.	One bit high on RS lines (MBI2).

ERRORS

CONTENTS

3.4 INTRODUCTION

This pamphlet discusses the error check sequence performed by the TM02, as well as TM02 and system responses to error conditions (ATTN and EXC asserted). For a detailed discussion of the Error register bits, refer to Chapter 2, Paragraph 2.5.3.

3.4.1 Error Check

Whenever the Control register is loaded, setting the GO bit, an error check is performed. If an error condition exists, the operation specified by the function code in the Control register is inhibited.

If any bit in the Error register is asserted, COMPER H (Composite Error) is asserted (MBI 10). If the Control register is loaded while this signal is asserted, PREV ER H (Previous Error) is generated and prevents the assertion of OCC (Occupied) on the Massbus (MBI 7). This clears the Control register GO bit, which in turn sets the TM02 ATA bit and asserts ATTN on the Massbus.

3.4.2 Attention (ATTN)

Attention (ATTN) is asserted on the Massbus by any drive that requires servicing. ATTN is asserted (MBI 3) under the following conditions:

1. At the completion of an erase, space, or write tape mark operation

2. Upon initiation of rewind command

3. Upon loading a 1 into the GO bit of the Control register while an error condition exists

4. Upon termination of an operation during which an error occurred or SSC was asserted

5. Upon termination of any operation during which END POINT was asserted.

When the Massbus Controller senses that the ATTN line of the Massbus is asserted, it must read the Attention Summary register (R04) to determine which drive(s) require servicing. It will service each drive whose ATA bit is asserted, and will clear the ATA bit of the drive upon completion of servicing.

To service a TM02, the Massbus Controller first reads the Status register (R01) to determine why servicing is required. If the ERR (Composite Error) bit of the Status register is asserted, it will read the Error register (R02) to determine which error has occurred, and will then proceed accordingly. If the SSC (Slave Status Change) bit of the Status register is set, the Massbus Controller should poll all the slave TU16s controlled by the TM02 to determine which one requires servicing and why.

3.4.3 Exception (EXC)

The EXC line of the Massbus is immediately asserted (MBI 9) by the TM02 whenever any error occurs during a data transfer operation (OCC TM asserted).

If during a read data operation, an error which is serious enough to invalidate data occurs, then the TM02 asserts EBL (MBI 9) on the Massbus. This will cause the data transfer to be terminated; however, the read data operation of the TM02 continues and terminates in the normal manner.

If during a write data operation, an error which is serious enough to invalidate data occurs, then the TM02 asserts EBL on the Massbus. It also terminates the write operation (WRITE END L asserted), stopping tape motion after erasing IRG.

The following error conditions cause the TM02 to assert EBL:

1. A data transfer operation is attempted while an error condition exists in the TM02.

2. An error condition occurs while the data transfer is being initiated.

3. A Class B error (UNS, OPI, DTE) or an ILF error occurs while a data transfer command is being executed.

4. A data error (INC/VPE, DPAR, PEF/LRC, COR/CRC) occurs during the data transfer operation, while bit 12 (EAODTE) of the Tape Control register is set.

3.4.4 Performance Checks

The TM02/TU16 Control Logic Test diagnostic (see Paragraph 3.1.2) checks the operation of each error bit except UNS. The assertion of UNS may be caused by the TM02 power supply or the loss of MOL from the TU16.

3.4.5 Adjustments
None.

3.4.6 Troubleshooting

When troubleshooting the error detection circuitry of the TU16/TM02, it is preferable to start at the Error register itself. Most of the Error register flip-flops are located in the Massbus Interface (MBI-11). The rest are located as follows:

1. INC/VPE, PEF/LRC, and COR/CRC are on TCPE-2/CNRZ-2.

2. CS/ITM is on TCPE-2/CNRZ-4.

3. NSG is on TCCM-5.

Table 3.4-1 lists errors which could be detected during certain operations and remain asserted after the operation is completed. If errors other than those indicated occur, the TU16/TM02 error detection circuitry should be suspect. Use the TM02/TU16 Control Logic Test diagnostic (see Paragraph 3.1.2) to locate error circuitry which may be malfunctioning. Other errors along with some associated troubleshooting aids are given in Tables 3.4-2, 3.4-3 and 3.4-4.

Table 3.4-1
TU16/TM02 Operations and Possible Errors

Operations \ Errors	ILF	ILR	RMR	CPAR	FMT	DPAR	INC/VPE	PEF/LRC	NSG	FCE	CS/ITM	NEF	DTE	OPI	UNS	COR/CRC
Write to any register*		X	X	X												
Read fromm any register		X														
Load CS1 with "NO-OP"	X	X	X	X								X			X	
Load CS1 with "REWIND-OFF LINE"	X	X	X	X								X			X	
Load CS1 with "REWIND"	X	X	X	X								X			X	
Load CS1 with "DRIVE CLEAR"	X	X	X	X											X	
Load CS1 with "WRITE TAPE MARK"	X	X	X	X			X	X	X		X	X		X	X	
Load CS1 with "ERASE"	X	X	X	X					X		X	X			X	
Load CS1 with "SPACE FWD"	X	X	X	X						X		X		X	X	
Load CS1 with "SPACE REV"	X	X	X	X						X		X		X	X	
Load CS1 with "WRITE CHECK FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE CHECK REV"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ REV"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MASSBUS INIT															X	
Write into AS or MT register		X		X												

*Except AS or MT.

3.4-2

Table 3.4-2
Controller, Massbus Cable, Software and Power Supply Errors

Error	Bit	Mnemonic	Manual Reference Table No.	Print Reference	Diagnostic
Illegal Function	00	ILF	2-6	Set IFL Logic: (MBI5, MBI7); ILF Flop (MBI11); ILF Multiplexer (MBI10)	DZTUC, Test 20
Illegal Register	01	ILR	2-6	Register select lines (MB1, MB2); Register select logic (MBI2); ILR Flop (MBI11);	DZTUC, Test 27
Register Modification Refused	02	RMR	2-6	RMR Logic (MBI2); RMR Flop (MBI11) RMR Multiplexer (MBI10)	DZTUC, Test 21
Control Bus Parity	03	CPAR	2-6	C lines (MBI1, MBI2, MBI3); CPAR Flop (MBI11); C Bus Multiplexer (MBI3, MBI4, MBI5, MBI8, TCCM7, MR2 through MR6)	DZTUC, Test 3
Format Error	04	FMT	2-6	Format Bits (MR6); ILF Decode (BF3)	DZTUC, Test 23
Data Bus Parity	05	DPAR	2-6	Parity tree (BF3); DPAR Flop (MBI11); C lines (MBI1, MBI2, MBI3)	DZTUC, Test 24
Non-Executable Function	11	NEF	2-6	Analyze program to determine which of five causes are the most probable. Logic decoding of conditions is on MBI7.	----------
Drive Timing Error	12	DTE	2-6	Caused by failure in SYNC CLK/WCLK sequence (BF2) or Occupied Line (MBI7).	DZTUC, Test 30
Unsafe	14	UNS	2-6	MOL not present (MBI7); H740 ACLO is asserted	----------

Table 3.4-3
Tape Read/Write Errors

Error	Bit	Mnemonic	Symptom	Probable Cause
Operation Incomplete	13	OPI	_____	Go to Paragraph 3.5.10.3
Frame Count Error	09	FCE	During a Read Operation no other Error Register bits are set.	The RH11 was expecting a longer record. This is normal when tape format is unknown.
			In the NRZ mode, during a read or write operation, other data error bits are present.	Usually indicates the G056 output changed during the assertion of RSD0. Verify signal amplitudes and tape speed.
			During a write operation	Usually indicates tape error caused early detection of postamble.

Table 3.4-4
Analysis of Data Errors*

Mode of Operation	Symptom	Probable Cause
NRZ	PEF/LRC error only	The LRC character or the LRC checking logic is at fault.
	VPE with FCE error	Usually indicates G056 transistion during RSD0 causing SET VPE L on M8911. The trouble could be a badly damaged tape, poor velocity regulation, a worn head or a faulty G056.
	CRC and LRC errors without VPE while in the forward direction.	Problem is in the CRC character.
PE	CS/ITM error and NRZ runs.	Indicates a problem in detecting the end of the Preamble in one or more tracks.
	INC without any bits being set in the CC Register	Intermittent deskew channel in the TM02.

*Troubleshoot data errors (INC/VPE, PEF/LRC, COR/CRC, CS/ITM) using the appropriate read/write troubleshooting sections of Chapter 3 and the information contained in this table.

TAPE MOTION

CONTENTS

3.5 INTRODUCTION

TU16 tape motion can be controlled by the TM02 via the slave bus, or by the TU16 control panel switches (Figure 3.5-1), depending on whether the transport is on-line or off-line. The motion control logic in the LAW module (M8910) provides proper sequencing and control during TU16 operations. It enables the vacuum motor and provides the signals that control the capstan drive circuitry.

The H606 Power Board contains the capstan drive circuitry and the tape reel braking and motor control circuits. The direction and velocity of capstan rotation are determined by three signals (FOR H, REV/REW H, and REWIND CAP H) from the motion control logic. These signals, therefore, determine the direction and speed of tape motion. The tape reel braking and motor control circuits activated by the vacuum switches in the vacuum columns operate to maintain a reservoir of tape within the columns. The vacuum system operates to supply tape to the capstan at constant tension.

3.5.1 TU16 Power Board (H606)
The TU16 Power Board (H606) is divided into two
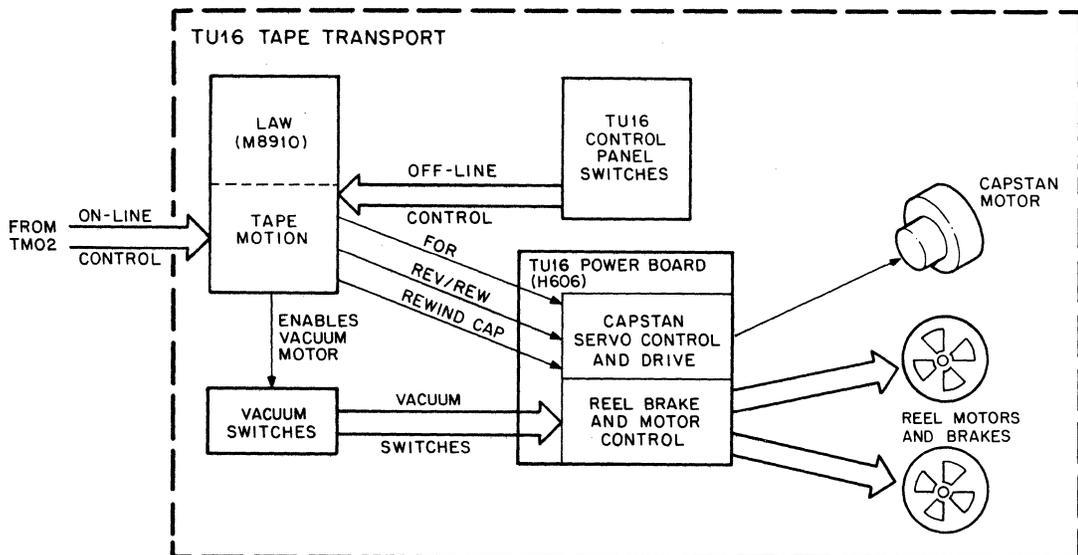
Figure 3.5-1   Tape Motion Control Block Diagram

3.5-1

main areas: Capstan Servo Control and Driver Circuits and the Tape Reel Braking and Motor Control Circuits; the discussions reference the H606-0-1 schematics.

3.5.1.1 Capstan Servo Control and Driver —

The heart of the transport mechanism is the capstan subsystem, which transports the tape across the read/write/erase head assembly at the desired speed. The capstan is controlled by a velocity-feedback servo loop, shown in Figure 3.5-2. Refer also to sheet 3 of the H606-0-1 schematics. As a forward command enters the logic (FOR H), Q1 is biased correctly to turn on. With Q1 turned on, the voltage present at the base of Q7 is higher than the -8 V at the emitter, resulting in Q7 being turned on. If either reverse or rewind is selected, signal REV/REW H becomes true and turns Q2 on, while forward selects Q7. Notice that the collectors of both Q2 and Q7 are tied together. That output line is the running speed line going to the "-" input of the operational amplifier. Diodes D7 and D10 detect the more positive and more negative levels from Q2 and Q7, respectively, when selected. Therefore, when Q2 is on (Q7 off), D7 conducts and when Q7 is on (Q2 off), D10 conducts. Resistors R12 and R13 are the reverse and forward speed adjustments. They are each adjusted to move tape at 45 in./sec. Refer to Paragraph 3.5.9 for more detailed information concerning adjustments.

Transistors Q8, Q9, and Q10 constitute a -8 V series regulator which biases the forward (Q7) logic. Transistors Q4, Q5, and Q6 make up a +8 V series regulator which supplies regulated +8 V to the reverse (Q2) logic. Circuit schematic DRVR 3 (H606, sheet 3) lists test points available for checking these supplies.

The tachometer feedback signal (TACH V) is filtered and applied to the "+" input of the operational amplifier (comparator). The tachometer produces an output voltage (TACH V) proportional to the velocity of the capstan. The capstan servo amplifier (72741 at E11) compares the tachometer output with a reference voltage that is proportional to the desired capstan velocity and generates an appropriate error voltage. The error voltage (SERVO SIGNAL) is further amplified by the capstan motor driver, which drives the capstan motor. Thus, if the capstan is running slower than the desired speed, the SERVO SIGNAL and, consequently, the voltage impressed on the capstan motor increase, speeding up the capstan. If the capstan is running too fast, the capstan velocity is similarly decreased.

When the capstan is at rest and a forward command is issued, the difference between TACH V (0 V) and the forward (Q7) circuitry is quite large. This causes the error voltage comparator to produce SERVO SIGNAL, which goes on to the driver circuitry to allow the capstan velocity to approach 45 in./sec forward velocity.

Resistor R21 is the balance adjustment resistor found in the comparator feedback loop. It is adjusted for zero
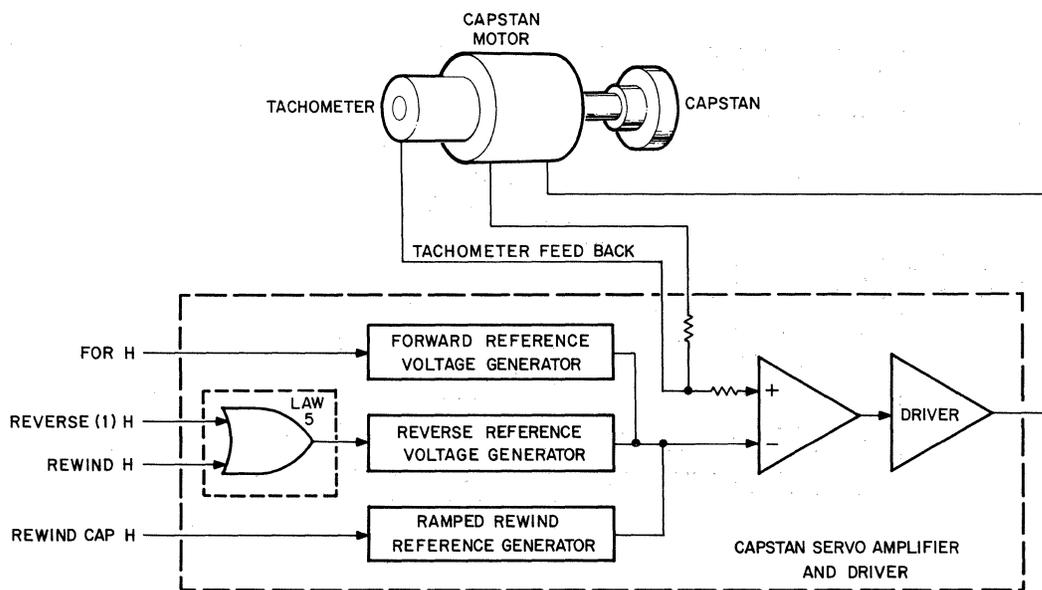
Figure 3.5-2   Servo Feedback Loop

IO-1299

3.5-2

capstan creep with no input. The procedure for adjustment may be found in Paragraph 4.19.1

Due to the danger of "spooking" (slippage between adjacent layers of tape on the reels), which can damage tape by stretching or buckling it, the tape reels cannot be accelerated as quickly as the capstan for high-speed (rewind) operation. For normal (45 in./sec forward and reverse) operation, the vacuum columns buffer enough tape to allow time for the reels to catch up with the rapid accelerations and decelerations of the capstan. However, the buffer columns cannot contain enough tape to allow the capstan to accelerate and decelerate at its normal high rates to and from the 150 in./sec rewind velocity. For this reason, the rewind command logic uses two signals (REV/REW H and REWIND CAP H) to control the rewind velocity of the capstan.

When a rewind command is issued, signal REV/REW H is asserted, causing the capstan to accelerate immediately to 45 in./sec just as in a normal reverse operation. Then REWIND CAP H is asserted; transistor Q3 is turned on, placing an increasing current on the running speed line. This causes a ramped rewind reference voltage generator (R10/C13 time constant) to gradually increase the rewind speed, exponentially approaching 150 in./sec at a rate at which the reels can be accelerated. Resistor R11 is used to fine-adjust the rewind speed. Refer to Paragraph 3.5.2 for further information.

Refer now to sheet 4 of schematic H606-0-1. This is the circuitry that drives the capstan motor. When SERVO SIGNAL enters, it splits and goes to both the right and left sides of the drawing. Transistors Q31 and Q32 sense the SERVO SIGNAL polarity for the forward (+) and reverse (-) directions, respectively. The circuitry involving transistors Q33, Q34, and Q35 provides current amplification for the forward direction, providing MOTOR with the current necessary to drive the motor. Transistors Q36, Q37, and Q38 operate in a similar manner for the reverse direction.

The SERVO SIGNAL line also goes to the left of the drawing; diode D38 shunts a positive SERVO SIGNAL for forward and diode 39 shunts negative levels for reverse. These two diodes are connected to the collectors of the two differential amplifiers (Q24 and Q26). The current (MOTOR) through the motor and, consequently, its acceleration rate, would be functions of such loosely controlled parameters as power supply voltage, motor armature resistance (a function of

temperature), and the back emf of the motor if some precautions were not taken. By current-limiting the output of the power current amplifier, the acceleration and deceleration rates of the capstan in normal (i.e., forward and reverse) operation become accurately controlled. The SERVO SIGNAL line is full of the large variations mentioned previously. Resistor R85 (0.1 ohm, 1%) in the MOTOR RETURN line senses current through the motor and supplies a respective signal (through R94) to the bases of the Q24 and Q26 differential amplifiers. The selected amplifier (Q24, forward; Q26 reverse) limits the current to the capstan motor and keeps the current between MOTOR and MOTOR RETURN constant.

Transistor Q24 is used in the forward line; Q26 operates in the reverse. Resistor R89 is the + current adjustment used to fine-tune the forward running current, eliminating large changes in the MOTOR RETURN line. Resistor R90 adjusts negative current for reverse direction, following a similar philosophy. Paragraph 4.19.3 explains the adjustment procedures involving these resistors.

3.5.1.2 Tape Reel Braking and Motor Control Circuits

— Sheets 5 and 6 of schematic H606-0-1 illustrate the braking and motor control circuits. As explained in the previous paragraphs, it is necessary to buffer a small amount of tape past the read/write/erase head assembly without "spooking" the tape on the file and take-up reels. For this purpose, vacuum-buffer columns are used. The capstan does not directly move tape from one reel to another; rather, it removes tape from one vacuum column and deposits it in another. Each reel motion servo system endeavors to keep its associated vacuum-buffer column half-filled with tape, ready either to supply or to take up tape, as might be required by a sudden acceleration of the capstan.

Figure 3.5-4 shows the tape transport vacuum-buffer columns and the respective tape-positioning-sensing vacuum switches; this figure is referred to again later in this section. A vacuum port at the bottom of each vacuum-buffer column provides the vacuum which draws the tape loop into the column with a constant tension, independent of the position or velocity of the tape loop. This assures a good, uniform wrap of the tape on the reel. In normal operation, the position of the tape loop in each vacuum column is sensed by a vacuum switch located near the top of each column, i.e., the upper motor upper vacuum switch (take-up reel column) and lower motor upper vacuum switch (the file reel column). These vacuum switches close when subject to a vacuum exceeding 10 in. of water and

EMPTY: A and B closed
        C and D open

FULL: A and B open
       C and D closed

NEITHER: all open

+17V

−17V

A

C

D

B

IO-1294
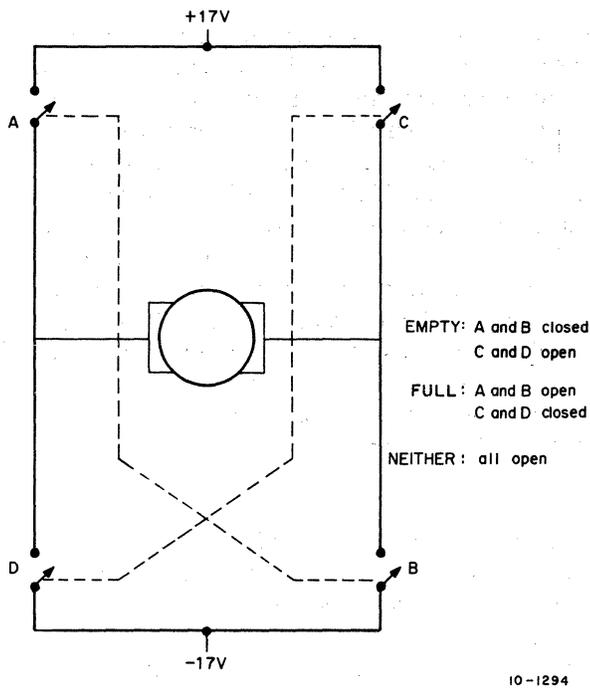
Figure 3.5-3 Reel Motor Amplifier Equivalent
             Circuit

open when exposed to ambient air pressure. Thus, if the tape loop is above the upper vacuum switch in the buffer column, the switch is exposed to vacuum; the switch is then closed and its corresponding signal (UVS for the upper vacuum switches and LVS for the two additional lower vacuum switches) is at ground. If, however, the tape loop is below a vacuum switch in either column, the switch is exposed to ambient air pressure; it opens and the corresponding signal is high.

The reel servo systems endeavor to keep the respective tape loops in the brake zones (i.e., between the UVS and LVS of each column). Thus, if the capstan stops, each reel comes to rest with the tape loop in its brake zone.

If, then, the capstan begins to put tape into a buffer, the loop moves down until it passes over the column LVS and enters the lower zone. At that point, braking is removed and a command is sent to the reel motor amplifier to accelerate the reel in order to empty tape from the buffer.

The tape loop continues to move down into the lower zone until the reel is emptying tape out of the buffer columns as fast as the capstan is putting it in. As the motor continues to accelerate the reel, the tape loop begins to move up again until is passes the LVS and enters the braking zone. The motor is then turned off and

braking is again applied. The tape loop continues to move up into the brake zone until the rate at which the reel motor is removing tape from the buffer column is again equal to the rate at which the capstan is putting tape in and, as the reel continues to decelerate, the cycle repeats. Thus, the tape loop oscillates about the position of the LVS. If the capstan instead removes tape from the buffer, the tape loop similarly oscillates about the UVS as the motor and brake alternately accelerate and decelerate the reel while supplying tape the buffer column at the average rate at which the capstan is removing it. Figure 3.5-4 also shows the additional fail-safe vacuum switches used. These switches, located above and below the UVS and LVS in each column, are used to detect a failure in the tape transport mechanism that threatens to damage the tape.

Figure 3.5-3 shows an equivalent circuit of the reel motor drive. Each reel motor is connected across a transistor bridge, which can connect the motor between the -17 V and +17 V INT power supplies in either direction. Under normal operating conditions, REEL MTR ENABLE L is asserted and the reel motor responds to control by the vacuum switch signals. When a UVS is low (closed), the reel motor is connected across the power supplies in the direction that drives tape into the buffer column. When a UVS is high (open) and an LVS is low, indicating that the tape is in the braking region, the reel motor is shut off. When both a UVS and LVS are high, the reel motor is connected across the power supply in the direction that removes tape from a buffer.

Each reel motor amplifier has an additional input, REEL MTR PLS H, which is used during the loading sequence to start tape into the vacuum column. The REEL MTR PLS signal is asserted during the tape loading sequence to cause the reel motor to feed a few inches of slack tape into the buffer column sealing the buffer column and allowing vacuum to build up in the column. The loading sequence is explained in more detail later.

When tape is not loaded, or when a failure is detected by the fail-safe switches, REEL MTR ENABLE L is negated, disabling the vacuum switch signals, and the +17 V INT is interrupted, removing power from the reel motors.

Tape Reel Motor Control Operation — The reel motors circuit operation still references sheets 5 and 6 of schematic H606-0-1 and Figure 3.5-4. Because the upper motor circuitry (take-up reel) functions identi-

TAKE-UP REEL
(UPPER MOTOR)

TAPE GUIDE

UPPER FAIL SAFE
TRANSPORT WILL
AUTOMATICALLY SHUT-DOWN
(FAIL-SAFE CONDITION)

UPR MOTOR UVS
TAPE WILL BE SUPPLIED TO
COLUMN (TAKE-UP REEL
TURNED OFF)

UPR MOTOR LVS
TAPE WILL BE EXTRACTED
FROM COLUMN
(TAKE-UP REEL TURNED ON)

LOWER FAIL SAFE
TRANSPORT WILL
AUTOMATICALLY SHUT DOWN
(FAIL-SAFE CONDITION)

VACUUM CHAMBER
PORT

LEFT VACUUM
COLUMN

CAPSTAN

HEAD TAPE GUIDES (2)

R/W ERASE
HEAD ASSEMBLY

TAPE GUIDE

FAIL SAFE
TAPE SUPPLIED
TO COLUMN

TAPE EXTRACTED
FROM COLUMN

FAIL SAFE

VACUUM CHAMBER
PORT

RIGHT VACUUM
COLUMN

FILE REEL
(LOWER MOTOR)

10-1293

Figure 3.5-4   Tape Transport Mechanism

cally to the lower motor circuitry (file reel), only the lower motor circuitry is detailed in this section.

Referring to Figure 3.5-4, notice that the file reel is associated with the right vacuum column. The column is numbered, 1, 2, and 3 with respect to what happens when tape is in one of those numbered areas. The three possibilities are described in the following paragraphs.

1. Supplying Tape to the Vacuum Column — Refer to the H606-0-1 schematic, sheet 5. When tape is in position 1, both the LWR MTR UVS and LWR MTR LVS are exposed to the vacuum and are, therefore, low. This places low levels at the bases of both Q11 and Q12, keeping them turned off and resulting in high level outputs from both collectors. With both LWR MTR UPR SW (LWR MTR UVS inverted) and E1-pin 11 high, signal LWR MTR UVS/LVS is low.

    Refer to H606, sheet 6. Signal LWR MTR UVS/LVS low puts a low level at the input (base) of Q28, keeping Q28 off. This indicates the column is empty. The LWR MTR UPR SW high level and REEL MTR ENABLE low make REEL MTR PLS high at the base of Q45, turning Q45 on. The base of transistor Q43 is clamped approximately three diode drops below +17 V. The base of Q43 is lower in potential than the emitter potential, so it turns on. This results in a voltage divider network from +17 V INT down through R141, R143, and R144 to -17 V, resulting in approximately +15 V on the collector of Q43 and -15 V at the junction of R143 and R144. The +15 V is also present on the base of Q42, turning it on; -15 V on the base of Q41 turns it on. Transistor Q42 places +17 V INT on the LWR MTR RT line. Transistor Q41 places -17 V on the LWR MTR line, resulting in 34 V across LWR MTR. The LWR MTR (file reel) turns in a clockwise direction, placing tape into the right vacuum column.

2. No Action — As soon as the tape enters the area marked 2 on Figure 3.5-4, the UVS is no longer exposed to vacuum pressure, but instead is exposed to open air. This makes the LWR MTR UVS line high, turning on Q11 and making LWR MTR UPR SW low. With LWR MTR UPR SW low and TP8 still high, signal LWR MTR UVS/LVS remains low.

Now both the LWR MTR UVS/LVS and LWR MTR UPR SW lines are low.

The LWR MTR UVS/LVS low level keeps Q28 off. The LWR MTR UPR SW low level keeps Q45 off. With both Q28 and Q45 off, no paths are connected to drive the LWR MTR, so nothing happens (motor does not turn).

3. Remove Tape from the Vacuum Column — If tape continues to go into the right vacuum column (i.e., the capstan may be putting it in), it passes point 3. Now both the UVS and LVS are exposed to air pressure, putting ground levels at the bases of Q11 and Q12, turning them on; LWR MTR UVS/LVS becomes high and LWR MTR UPR SW becomes low. The high level of LWR MTR UVS/LVS turns Q28 on and LWR MTR UPR SW low makes REEL MTR PLS low, turning Q45 off. Transistor Q28 turned on creates a voltage divider from +17 V INT, through R120 and R119 to ground. The base of Q40 is clamped in the same way Q43 was, placing about +15 V at its base; this turns Q40 on. The approximate voltage of +15 V at the base of Q39 turns Q39 on. The -15 V at the base of Q44 turns Q44 on. Transistors Q39 and Q44 operate in a manner similar to the Q41-Q42 combination (when the tape was in position 1). However, in this instance, the +17 V INT is connected to the LWR MTR line (through Q39) and the -17 V is connected to the LWR MTR RT line (through Q44). This puts +34 V across the LWR MTR with polarity opposite that of the supplying tape case, resulting in the reel motor turning in the opposite (counterclockwise) direction and removing tape from the right vacuum column.

Take-Up Reel Operation — The theory and logic operation for supplying and removing tape from the left vacuum column (take-up reel) is almost identical to the file reel operation. The exception is that when supplying tape to the column, the take-up reel turns counterclockwise (as opposed to clockwise for the file reel), and, when removing tape, it turns clockwise.

Transistors Q47 and Q50 create the network to place +17 V INT on the UPR MTR RT line and -17 V on the UPR MTR lines, turning the UPR MTR counterclockwise to supply tape to the left vacuum column.

Transistors Q46 and Q51 reverse the polarity of the voltage across the UPR MTR and turn it clockwise, removing tape from the left vacuum column.

Brake Control Operation — The brake control logic is illustrated on schematic H606-1, sheet 5. The brakes used on the TU16 are electromagnetically-operated friction brakes. In normal 45 in./sec operation, when UPR MTR UVS is high and UPR MTR LVS is low (i.e., when the tape loop is in the braking zone), approximately 310 mA of current is driven through the brake winding. With signal UPR MTR UVS high and signal UPR MTR LVS low, UPR MTR UVS/LVS becomes low. Tracing the AND of UPR MTR UVS/LVS and UPR MTR UPR SW through, it is noticed that UPPER BRK ON H is true. This high level turns Q19 on; this turns Q18 on, which, in turn allows the Q20 current driver to apply 310 mA of current to the brake winding (as UPPER BRK OUT). This produces enough torque to rapidly bring the take-up reel to a stop.

When the tape loop moves out of the brake zone, the current is shut off. Because the braking current tends to produce a significant residual magnetism in the brakes, a short (15 ms) pulse of about 150 mA current is applied in the reverse direction when the brakes are released to ensure complete demagnetization and release of braking. As the tape moves out of the brake zone, UPPER BRK ON goes away. This low transition is ac coupled through C25 to Q21 and Q22 (as UPPER BRK ON), resulting in the short pulse. Zener diode D25 and R71 (the collector resistor) cause the smaller (150 mA) current.

During high-speed rewind, the operation of the brake circuitry must be modified somewhat to avoid stopping the reel whenever the tape loop enters the braking zone. Without this modification, the reel motor could not accelerate the reel to 150 in./sec rapidly enough to prevent failure. For this reason, when REWIND CAP H is asserted and the tape loop enters the brake zone, only a short pulse of braking is applied to the reel to slow it down but not to bring it to a halt. In the case of the take-up reel servo, if the tape loop remains in the braking zone longer than about 50 ms, a low current of about 60 mA is applied to the brake, further decelerating the reel. As REWIND CAP H becomes asserted, signal LOW REWIND BRK L is asserted, placing a low level input to the base of Q23. This turns Q23 on and allows Q20 to pass an additional low current out UPPER BRK OUT. In the case of the lower (file) reel, this additional stop current is not necessary.

The file reel brake control logic operates otherwise identically to the take-up reel braking system. Signal LOWER BRK OUT is the line to the file reel brake coil. The path for normal braking (when LOWER BRK ON high is asserted) is through transistors Q15 and Q16 to drive 310 mA out of the LOWER BRK OUT line. To compensate for the residual magnetism in the brake coil, when LOWER BRK ON is negated, the LOWER BRK ON low transition is ac coupled through Q53, allowing Q17 to apply the necessary reverse current to LOWER BRK OUT.

The difference in braking of the two reel systems occurs because the upper reel is dumping tape into the buffer during rewind and is therefore accelerated by torque resulting from the tape tension produced by the vacuum column. The lower reel, however, is removing tape from its buffer and, therefore, the tape tension tends to decelerate the lower reel, making low drag braking unnecessary.

Figure 3.5-5 shows the brake current waveforms of each reel system during both 45 in./sec and rewind operations. Whenever tape is not loaded or the fail-safe switches detect a failure, and the LOAD/(OFF)/BRK REL switch is not in the BRK REL position, signal FORCE BRK ON low is asserted. This signal causes high (310 mA) braking to be applied to both reels, regardless of the signals from the vacuum switches.

3.5.2 Motion Control Logic
The motion control logic, shown on the M8910 (LAW) drawings, provides the necessary sequencing and control for loading tape, rewinding, brake release, and shutting down the TU16 if power or the tape unit itself should fail. Its main sections are listed and explained below.

Power Clear — The power clear circuitry consists of a power transient detector and one-shot. When the +5 V power supply is turned on, the circuit produces P CLR L, which produces LOCAL H; this produces a 20-ms clear pulse (DELAYED LOCAL L) that resets all of the various status flip-flops of the TU16 to the idle, unloaded, off-line condition, keeps all motors turned off, and asserts braking on the reels. Similarly, when the +5 V power supply drops to approximately 4.4 V, a PWR CLR pulse is produced that lasts for 20 ms or until the power supply drops too low to operate the power clear circuitry (approximately 3 V).

Servo System Failure Detection — As explained in previous text, two fail-safe switches, located in each

UPPER-REEL BRAKE
CURRENT WITH
REWIND CAP ASSERTED

310 mA
HIGH BRAKE
←22 ms→
15-40 ms
(See note)
60 mA
LOW BRAKE
-150 mA

LOWER-REEL BRAKE
CURRENT WITH
REWIND CAP ASSERTED

310 mA
HIGH BRK
(See note)
12 ms
-150 mA

EITHER BRAKE CURRENT
WITH REWIND CAP
NEGATED

310 mA
HIGH BRAKE
(See note)
-150 mA

BRAKE H

NOTE:
15 ms DEGAUSSING

CP-0215
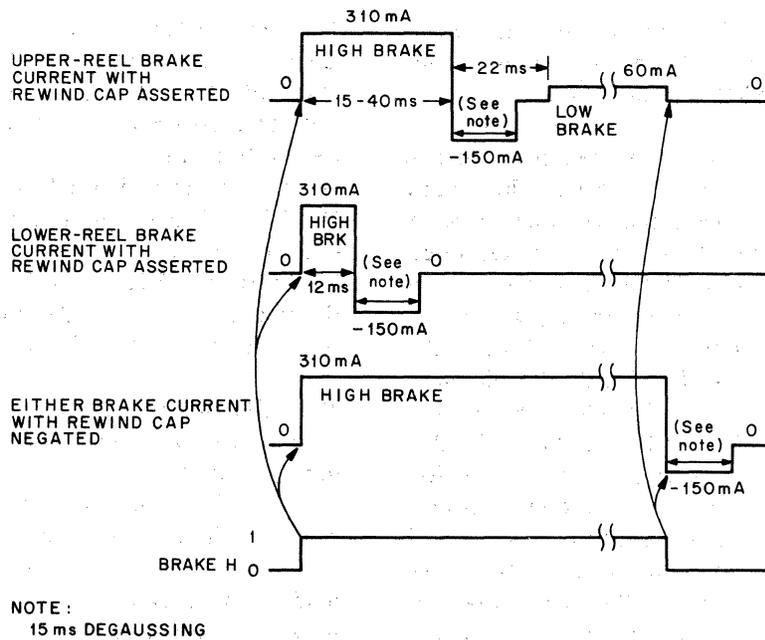
Figure 3.5-5   Brake Current Waveforms

vacuum-buffer column, define the permissible limits of excursion of the tape into those columns. If the tape loop in either buffer column goes below fail-safe switch, the switch opens and LFS H is asserted. If either tape loop is above its upper fail-safe switch, then UFS L is asserted. When VACUUM ON L is asserted, indicating that tape is loaded, and either LFS H goes to 1 or UFS L goes to 0, then the FAIL flip-flop (LAW 5) is set. The effect of FAIL (1) is essentially the same as that of the CLR PLS pulse, except that FAIL (1) is a level and remains asserted, preventing tape unit operation until manually reset by moving the LOAD/(OFF)/BRK REL switch to its central OFF position.

Loading Sequence Logic — Initiation and shutting down of the reel motors, brakes, and function control logic is controlled by the loading sequence logic. The loading sequence logic consists of the RELAY ENABLE flip-flop, the REEL MTR ENABLE L and VACUUM ON L one-shots, and their associated gating. The RELAY ENABLE flip-flop is reset by either FAIL (1) or the LOAD/(OFF)/BRK REL switch being in the OFF position. When RELAY ENABLE is reset, the vacuum motor is turned off. Also, the power supply interrupts PWR COM INT and +17 V INT, which turns off power to the reel and capstan motors. The REEL MTR ENABLE L one-shot is held to its 1 state, negating REEL MTR ENABLE L; the VACUUM ON L integrating one-shot is held to its 1 state, ne-

gating VACUUM ON L. These prevent the function control logic from responding to any command.

The RELAY ENABLE flip-flop is set by LOAD PULSE L, a pulse produced when the LOAD/(OFF)/BRK REL switch is brought to the LOAD position. When the RELAY ENABLE flip-flop is set, the vacuum motor is turned on; RELAY ENABLE L is asserted, clearing FORCE BRK ON and generating REEL MTR PLS (H606, sheet 6). Both PWR COM INT and +17 V INT are restored. Signal REEL MTR PLS causes each reel motor to dump a small amount of tape into the top of its buffer column, sealing it and allowing vacuum to build up in the column. When the lower fail-safe switches in both vacuum columns sense vacuum, the REEL MTR ENABLE L and VACUUM ON L delays are allowed to begin timing out. Approximately 100 ms is allowed for the vacuum to build up and stabilize before the REEL MTR ENABLE L one-shot times out, asserting REEL MTR ENABLE. When REEL MTR ENABLE is asserted, the reel servos can function normally, bringing the tape loops to the middle of the buffer columns. Approximately 3 sec later, the VACUUM ON L one-shot times out, asserting VACUUM ON. This allows the function control logic to accept commands and also enables failure detection. The tape loading sequence is then complete, and the transport remains loaded until the RELAY ENABLE flip-flop is reset.

Brake Release — When the FORCE BRK ON flip-flop is set, full braking is applied to both reels. It is set whenever the RELAY ENABLE flip-flop is reset, and is cleared whenever RELAY ENABLE is set. The FORCE BRK ON flip-flop can also be cleared by BRK REL SW L, the signal asserted when the LOAD/ (OFF)/BRK REL switch is in the BRK REL position, provided that LFS H is asserted. Thus, the lower vacuum switches prevent brake release until the vacuum has drained out of the buffer columns. Moving the LOAD/(OFF)/BRK REL switch from BRK REL to the center OFF position causes RELAY ENABLE L to be asserted, again setting the FORCE BRK ON flip-flop.

Rewind Control — Due to the limited rate at which the reels can be accelerated and decelerated, a special sequence of control signals must be generated to perform a high-speed rewind operation. The sequence is shown in Figure 3.5-6. When the function control logic accepts a rewind command, it asserts (see drawing LAW 7) signal SET RWD CMD L, which direct sets the RWS flip-flop.

A high level is presented to the pin 12 input of the 7400 gate in location E41 (LAW 5). This asserts signal REV/REW H, which accelerates the capstan servo to 45 in./sec in the reverse direction. At the same time, RWS H triggers a 300-ms delay, which allows the reels to stabilize at 45 in./sec. When the delay times out, it asserts signal REWIND CAP H. The REWIND CAP H signal causes the capstan servo to gradually accelerate to 150 in./sec in the reverse direction.

Normally, rewinding continues until the function control logic detects the Beginning of Tape (BOT) marker. When BOT is detected, the function control logic asserts FWD L (LAW 7) and removes REWIND CAP H. The assertion of FWD L triggers the 140-ms delay (enabled by RWS H). Normal braking is applied and the capstan servo gradually decelerates toward 45 in./sec, still traveling in the reverse direction past BOT.

When this delay times out, the forward command is passed on to the capstan servo as FOR H (LAW 5). The capstan accelerates from 45 in./sec in the reverse direction to 45 in./sec forward. The tape then moves forward until the BOT marker is again detected. At this point, the function control logic clears FWD L, FOR H, and RWS H, and the capstan comes to a stop, terminating the rewind.
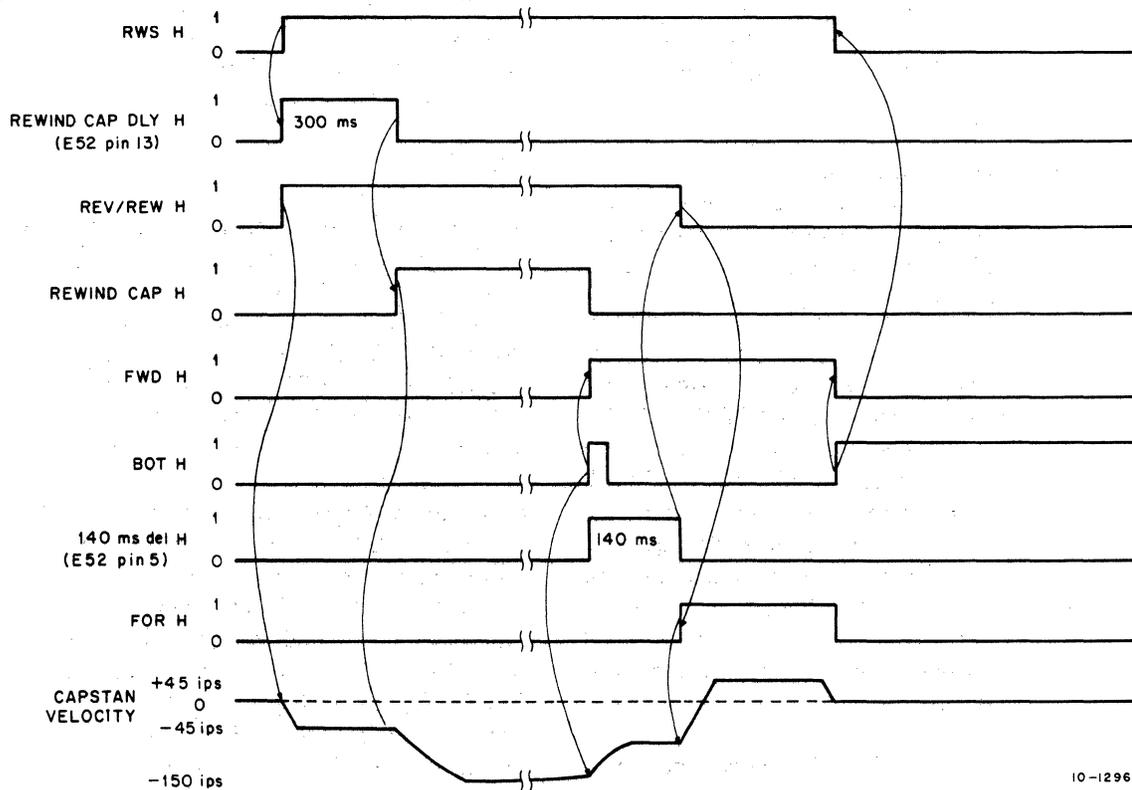
Figure 3.5-6   Rewind Sequence Timing

3.5-9

The rewind control logic is designed so that if the rewind is terminated at any point in the sequence, the operation stops without failure and without danger of "spooking" the tape.

Tape Unit Ready and Transport Settling Down — The RUNNING H and the transport settling down [SDWN (SB) L] signals indicate whether the transport is idle (ready to begin an operation) or settling down (coming to a halt after performing an operation). When the tape transport is on-line and selected by its controller, it transmits the signals to the controller to notify the controller when it is able to accept another command.

Whenever an operation is being performed, the function control logic asserts MOTION H. The OR of MOTION H (operation in progress) and LOCAL H (unit off line) sets the RUNNING H one-shot delay (LAW 5), thereby asserting RUNNING H and also inhibiting the settle-down signal, SDWN (SB) L. When both MOTION H and LOCAL H are negated, the RUNNING H one-shot begins to time out and SDWN (SB) L is asserted, indicating the transport is ready to accept a command to move tape in the same direction as the previous command. After approximately 13 ms, when the capstan has had time to come to a complete stop following any previous operation, the RUNNING H one-shot times out, negating SDWN (SB) L and, provided MOL H is asserted, asserting Tape Unit Ready [TUR (SB) L], thereby indicating that the unit is ready to accept any command.

3.5.3 Manual Control Operation
Manual operation of the TU16 Tape Transport is effected by the operator control box switches (Paragraph 1.7.1). The detailed operation of each of the switches is explained in this section.

LOAD/(OFF)/BR REL — This switch has three operations. In its center, or OFF position, signal OFF L is asserted to clear the FAIL and RELAY ENABLE flip-flops. When the switch is brought to the LOAD position, signal OFF L is negated and LOAD PULSE L is asserted for a few microseconds, setting RELAY ENABLE H and initiating the tape loading sequence. When the switch is brought to the BR REL position, OFF L is asserted again and the BRK REL SW signal is asserted low for brake release. For a more detailed explanation of these operations, see the relevant paragraphs of Section 3.5.2.

ON-LINE/OFF-LINE — When this switch is quiescent in either position, no output occurs to change the state of the transport. When it is moved from its ON-LINE to its OFF-LINE position, OFF LINE SW is momentarily asserted low, setting LOCAL H (LAW 6). When the ON-LINE/OFF-LINE switch is moved from its OFF-LINE to its ON-LINE position, ON LINE SW is asserted low momentarily, negating LOCAL H.

Unless a rewind operation is in progress, the assertion of either OFF LINE SW L or ON LINE SW L causes the assertion of INIT L (LAW 8). The assertion of INIT L clears the FWD, RWS and REV flip-flops and brings tape motion to a halt.

The LOCAL signal controls the operating mode of the TU16 Tape Transport. When LOCAL L is negated, the transport is on-line and all operations of the transport are directed by the TM02 Tape Controller via the Slave Bus (SB). When LOCAL H is asserted, the transport is off-line and is, effectively, isolated from the slave bus. In this mode, tape motion is controlled by the FWD/REW/REV and START/STOP switches, as discussed below.

FWD/REW/REV — This three-position switch selects the direction of tape motion for off-line operations (LAW 7). When it is in the FWD position, MANUAL FWD L is asserted; in the REW position, MANUAL REW L is asserted; and in the REV position, MANUAL REV L is asserted. These signals do not initiate tape motion, but are strobed by the START L pulse as explained below.

START/STOP — When this switch is moved from its START position to the STOP position, signal STOP L is asserted for a few microseconds. If the transport is off-line (LOCAL H asserted), this causes a corresponding pulse at INIT L, clearing the FWD, REW, and REV flip-flops and bringing tape motion to a halt. When the START/STOP switch is moved to the START position, START L is asserted, directly setting a flip-flop (at coordinates D-7 of drawing LAW 7). The high-going transition of this flip-flop is ANDed with LOCAL H (transport off-line) and MOTION L (no operation in progress) to produce a pulse that strobes the MANUAL FWD, REV, and REW lines in an 8266 multiplexer. The assertion of one of these lines causes the FWD, REV, or RWS flip-flop to be set, initiating tape motion in the indicated direction. Note, however, that if BOT H is asserted, the signal that sets the RWS flip-flop is gated off because the tape is already at BOT. Note also that if END PT H is asserted and FWD H is set, then INIT L is asserted to clear the FWD flip-flop and prevent running off the end of the tape.

3.5.4 Tape Unit Status Sensors

The tape status (EOT/BOT) and write lock sensor features are discussed in this section.

EOT/BOT Sensor — To locate the beginning and end of the recording area on the tape, the load and end points are marked by reflective strips mounted on the nonoxide side of the tape. The dimensions and placement of these strips are shown in Figure 3.5-7.

The strips are detected by the phototransistors of the EOT/BOT sensor assembly. The EOT/BOT assembly is located in the wall of the lower vacuum column. It consists of an EOT sensor phototransistor, located to detect light reflected from the EOT strip; a BOT sensor phototransistor, located to detect light reflected from the BOT strip; and two light-emitting diodes (LED) located opposite the center of the tape, which illuminate both the EOT and BOT strips. The LED operates in the infrared region and, therefore, produces no visible light. The outputs of the EOT and BOT signals are amplified, filtered, and converted to logic levels, as shown on drawing M8910 (LAW), sheet 6, producing signals BOT (SB) L, END PT H, and END PT (SB) L.

The assertion of END PT H sets a flip-flop, which remains set until either the tape is rewound or EOT is negated while the tape is traveling in the reverse direction. Thus, if the tape is moved forward past the EOT marker, the END PT flip-flop remains set even after the marker is passed and is cleared only by rewinding or reversing the tape back past the EOT marker. Setting the END PT flip-flop has the following effects:

1. If the TU16 is off-line (LOCAL H asserted), forward tape motion stops and the transport does not accept manual forward commands until the tape is rewound or reversed off the EOT marker.

2. The End Point indicator lamp is lit.

3. If the TU16 is on-line and selected by the TM02, the TU16 signal END PT (SB) L is asserted, indicating to the TM02 that is has passed the end point.

NOTE
Notice that if the TU16 is on-line, it does not stop automatically upon detecting EOT. It is permissible to write data up to 10 ft past the end point. It is up to the programmer to ensure that he does not run past this point.

NOTES:
(1) Photo reflective markers shall not protrude beyond edge of tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.2 ± 0.2 inch; width, 0.19 ± 0.02 inch; thickness, 0.0005 ± 0.0001 inch.
(2) Minimum for test area; maximum for recording.
(3) Tape shall not be attached to the hub.
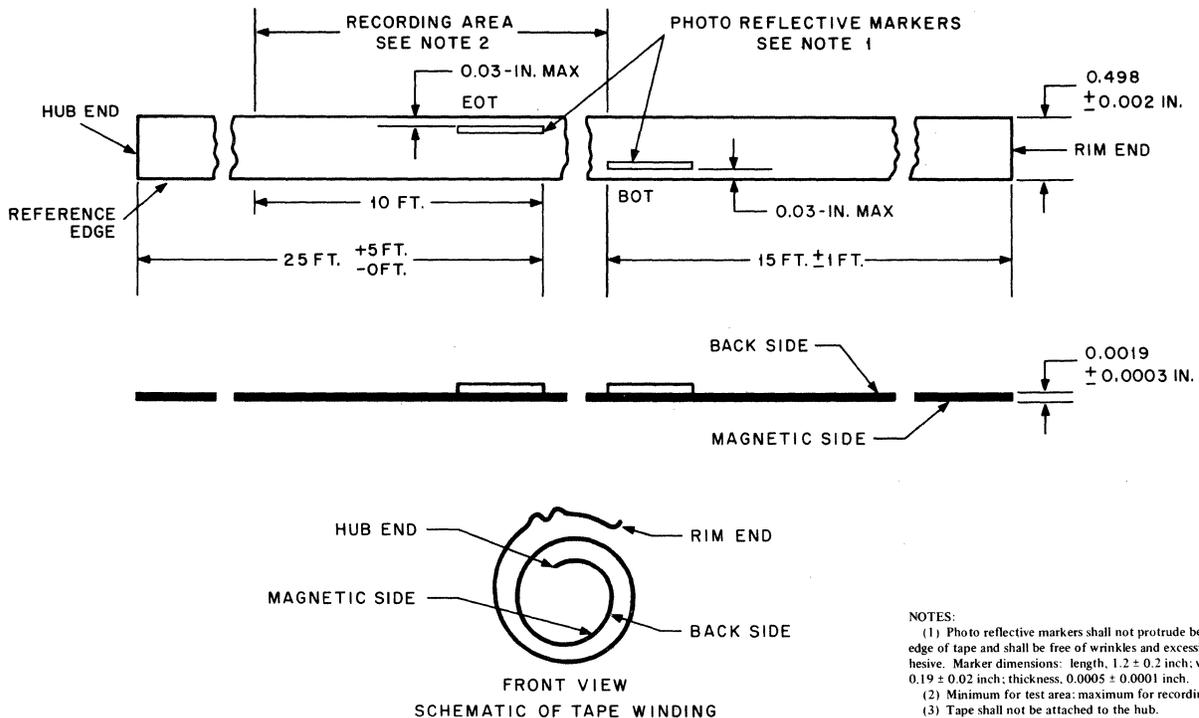
CP-0223

Figure 3.5-7   Tape Markers, Recording Area, and Tape Wind

The assertion of BOT H has the following effects:

1. The TU16 accepts no new rewind commands.

2. When the TU16 rewinds into BOT (i.e., RWS H is asserted, FWD L is asserted, and BOT H becomes asserted), the FWD flip-flop is set (drawing LAW 7); refer also to the description of rewind operation, Paragraph 3.5.2.

3. When the TU16 moves forward into BOT, the FWD flip-flop is cleared. (If the RWS flip-flop is set at this time, clearing FWD also clears RWS, terminating the rewind sequence.)

4. The LD PT indicator is lit.

5. If the TU16 is on-line (i.e., LOCAL L negated) and selected by the TM02, it asserts the transport bus signal BOT (SB) L, indicating to the TM02 that it is at BOT.

Write Lock — To protect tapes from inadvertent erasure, tape reels are provided with a write enable ring. If a reel of tape is mounted on the TU16 Tape Transport with its write enable ring removed, this condition is sensed and the transport refuses to honor any write commands. Further, if the transport is on-line and selected by its controller, it asserts WRL (SB) L to the TM02 Tape Controller, indicating to the TM02 that it is write-locked.

The physical write-lock assembly is shown in Figure 4-18. Principally, the assembly consists of the write-lock solenoid and the write-lock switch. When no write enable ring is inserted in the file reel, a feeler attached to the end of the solenoid shaft extends into the write-lock slot on the back of the reel. This feeler puts the write-lock switch in its normally closed position, asserting WR LOCK L (drawing LAW 8). When a write enable ring is inserted in the file reel, the ring pushes back the solenoid shaft, actuating the write-lock switch and negating WR LOCK L. If the write enable switch is actuated +17 V INT is turned on (i.e., when tape is loaded in the buffer columns) the write-lock solenoid is engaged to withdraw the write-lock feeler from contact with the ring. This keeps the write-lock switch actuated until the tape is unloaded and reduces wear of the write-lock assembly and write enable ring during tape unit operation.

3.5.5 On-Line Operation

When signal LOCAL L is negated, the TU16 is on-line. In this state, all transport operations are directed by the TM02 via the slave bus. The slave bus connects the TM02 Tape Controller to up to eight TU16 Tape Transports.

3.5.5.1 Transport Selection and Status Reporting —

All of the tape transports in a system are wired to the same slave bus, but only one transport can be logically connected to the bus at one time, i.e., only one transport can transmit its status to the TM02 Tape Controller and respond to commands, and only one transport can be reading or writing data at a given time.

To select the particular tape transport to converse with the tape controller, the controller transmits a binary code on bus lines B SEL 1 L, B SEL 2 L, and B SEL 4 L. As shown on drawing M8910 (LAW), sheet 6, each transport on the bus compares this code to the transport number determined by the unit select plug (signals SW1, SW2, and SW4). If the selection code transmitted by the TM02 Tape Controller matches the transport number, and the transport is on-line, the SELECT LAMP lights, and the transport logically connects itself to the slave bus. All other transports remain logically disconnected and neither transmit nor respond to bus signals.

When a particular transport is logically connected to the slave bus, it transmits status information to the tape control as follows:

7 CH (SB) L	Always negated in the TU16 Tape Transport.
BOT (SB) L	Asserted when the tape is positioned at load point (beginning of tape).
END PT (SB) L	Asserted when the End Point flip-flop is set.
WRL (SB) L	Asserted when the TU16 Tape Transport is write-locked.
RWS (SB) L	Asserted when the Rewind Status (RWS) flip-flop is set.
SDWN (SB) L	Asserted when the transport is settling down following an operation, i.e., asserted for about 13.5 ms following the command to terminate an operation while the capstan is coming to a halt.

TUR (SB) L   Asserted when the tape unit is ready to receive any command; i.e., when the transport is neither performing an operation nor settling down following an operation.

3.5.6 Tape Motion Initiation (On-Line)

When DRV SET PLS is generated by the Massbus Interface module (MBI 6), the TM02 negates STOP L (TCCM 3) and asserts SLAVE SET PLS L (TCCM 4) and EMD L (TCCM 3) on the slave bus (Figures 3.5-8 and 3.5-9). During a read or write data operation, this is a consequence of the assertion of RUN H by the Massbus Controller. During nondata transfer operations that require tape motion, this is a consequence of loading the corresponding function code (GO bit set) into the Control register (R00).

If a TU16 is selected, on-line, and loaded with tape (MOL H asserted), it responds to SLAVE SET PLS and the FWD, REV, and RWND command lines of the slave bus by setting the corresponding motion control flip-flops [i.e., FWD, REV, and RWS (Rewind Status) flip-flops on LAW 7]. If the WRITE command line is asserted, along with the RWND command line, SET OFFLINE L is generated, setting the LOCAL flip-flop (LAW 6). If WRITE is asserted but RWND is not,

SLAVE SET PLS produces SET WRE (Set Write Enable), which sets the WR ENAB flip-flop (LAW 8).

The outputs of the motion control flip-flops produce FOR H, REV/REW H, and REWIND CAP H (LAW 5) signals which control the capstan servo and drive circuits as described in Paragraph 3.5.1.1. At the same time, the WR ENAB flip-flop, if set, generates WRITE ENABLE H, which shunts WRITE voltage to the write and erase heads, thereby energizing the heads. This causes tape to be erased, generating IRG as the tape comes up to speed and the start motion delay times out. Simultaneously with motion initiation, EMD L gates the motion delay presets onto the Read Data lines of the slave bus (SC 2) and loads them into the Motion Delay Counter in the TM02 (TCCM 3). When EMD L is negated, the counter is upcounted by 800 BPI CLK until it reaches a count of 2^{14}, at which time ACCL H and READING L are asserted, and further clocking is inhibited. The presets of the counter determine the time interval necessary to reach a count of 2^{14}, and hence the duration of the motion delay. When an erase or write tape mark operation is performed, the presets to the motion delay may be modified. Modification occurs only when starting in the forward direction, not from BOT (E60 pins 3, 4, 5, and 6), and adds 80 ms to the start motion delay; this produces an extended IRG on tape. The presets depend on the
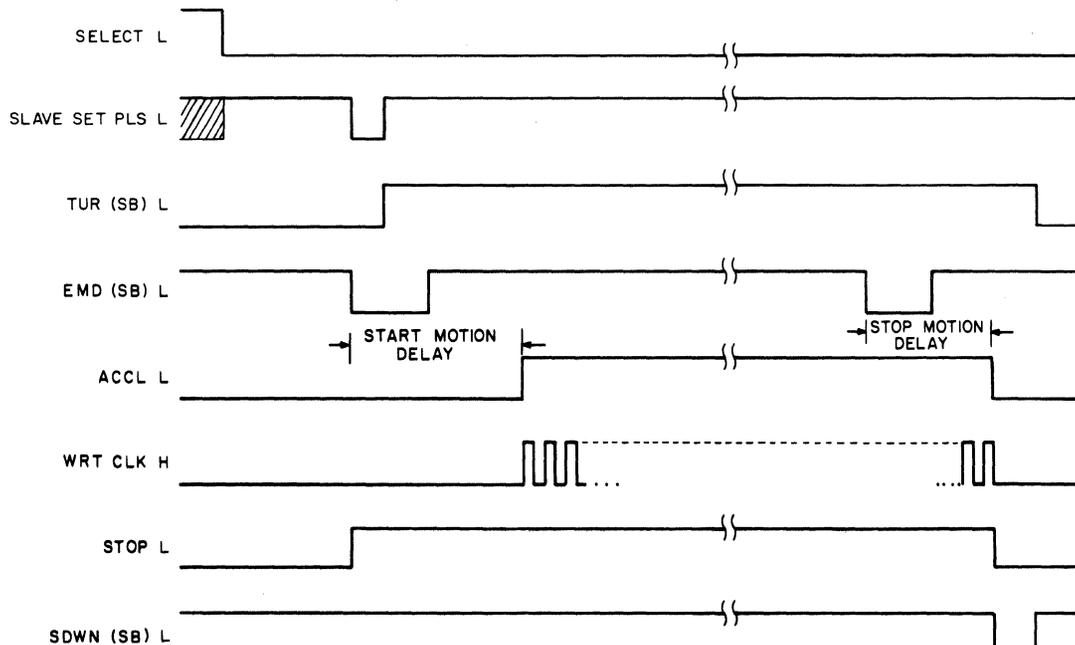
10-1295

Figure 3.5-8   Tape Motion Timing

3.5-13

TM02 | TU16

DATA-TRANSFER OPERATION

NON DATA-TRANSFER OPERATION

RECEIVE RUN H ASSERTED

CONTROL REGISTER LOADED (GO BIT SET)

DRIVE SET PULSE

SLAVE SET PULSE

ENABLE MOTION DELAY

LOAD MOTION DELAY COUNTER

COUNT UP TO 2^{14}

NEGATE ACCL L | ASSERT READING L

SB FWD ASSERTED ? — NO / YES

SB REV ASSERTED ? — NO / YES

SB RWND ASSERTED ? — NO / YES

SB WRITE ASSERTED ? — NO / YES

SB WRITE ASSERTED ? — NO / YES

SET FWD FF

SET REV FF

SET RWS FF

SET LOCAL FF

SET WR ENAB FF

GATE OUT MOTION DELAY PRESETS

GENERATE FOR, REV/REW & REWIND CAP

DRIVE CAPSTAN SERVO

PLACE TU16 OFF-LINE

ENERGIZE WRITE & ERASE HEADS

10-1291

Figure 3.5-9   Tape Motion Initiation Flowchart

type of operation performed (read/write), the direction of tape motion, and other parameters. Table 3.5-1 lists the motion delays generated under the various conditions. READING L enables the read circuitry in the TM02. ACCL L is transmitted to the TU16, where it enables generation of WRT CLOCK and other read and write functions.

Once forward or reverse tape motion is initiated, it continues (unless a TU16 mechanical or power failure is sensed) until the TM02 transmits STOP L asserted to the transport.

If a rewind operation is being performed, STOP L is asserted as soon as DRV SET PLS is negated. However, since the Rewind Status flip-flop is already set, this does *not* produce an INIT L pulse (LAW) and does not terminate motion. Once the Rewind Status flip-flop is set, the TU16 performs the rewind operation independently, as described in Paragraph 3.5.2. The TU16 notifies the TM02 that it is performing a rewind by asserting RWS L on the slave bus. When the rewind control sequence is over, motion terminates automatically and the TM02 is notified when the TU16 asserts SET SSC L (Slave Status Change) on the slave bus (LAW 8).

3.5.7 Tape Motion Termination (On-Line)

The TU16 terminates tape motion when an INIT L pulse (generated on LAW 8) clears the motion control flip-flops (LAW 7). Several sequences cause this to happen, depending on the type of operation being performed (Figure 3.5-10). The various sequences are discussed in the following paragraphs.

3.5.7.1 Read— During a read operation, the motion termination sequence begins when the read circuitry negates RST SHDN CNTR; this occurs when the read heads presumably encounter the IRG after reading a data record or tape mark.

When a tape mark or data record (24 preamble chara ters for PE, 10 data characters for NRZ) is encountere ENBL SHDN CNTR L is asserted (TCPE 5 and CNR 4). Because WRT CLK ENBL L is not asserted durir a read operation, the Gap Detection Timer (TCCM : will be inactive, and E35 pin 8 will be low. This allov ENBL SHDN CNTR L to gate 200 BPI CLK H to Shu down Counter (E51).

When no envelopes are detected in PE mode, (AN ENV H negated), or when no RSDO pulses are receive from TU16 in NRZ mode, RST SHDN CNTR L is n gated. This allows the Shutdown Counter to be uj counted. If the counter reaches a count of 15, EO PLS and EOR CLR L are produced. EOR CLR L a serts EMD L, (TCCM 3) and thereby initiates a sto motion delay. EMD L loads the motion delay count with presets gated by the TU16 onto the Read Da1 lines of the slave bus, just as occurred during motio initiation (Paragraph 3.5.6). The presets will, howeve be different during start and stop delays.

Note that because ACCL H was negated (E15, pin 2, high), the two most significant bits of the motion del counter are preset high, asserting DECL H and n gating READING L. The counter is upcounted unt overflow, at which time DECL H is negated and ACC H is asserted. The leading edge of ACCL H clocks th Stop flip-flop (E57), causing STOP L asserted to t transmitted to the TU16. STOP L produces the INIT pulse (LAW 8), which clears the FWD or REV motio control flip-flop, and thereby causes the capsta activating signal to be removed. As tape motion slov down, SDWN L is asserted by the TU16 and tran: mitted to the TM02. When tape motion stop RUNNING H is negated, while TUR L is asserted an transmitted to the TM02.

3.5.7.2 Write — Termination during a write is a most identical to that during a read. Note the two di ferences:

Table 3.5-1
Start and Stop Motion Delays

Start/Stop	Direction of Motion	Operation		
		Read/Space	Write Data	Erase/Write Tape Mark
Start Motion Delays	Reverse	2.7 ms	——	——
	Forward	2.7 ms	9 ms	89 ms
	Forward from BOT	9 ms	202 ms	202 ms
Stop Motion Delays	Reverse	1.8 ms	——	——
	Forward	1.8 ms	2.7 ms	2.7 ms
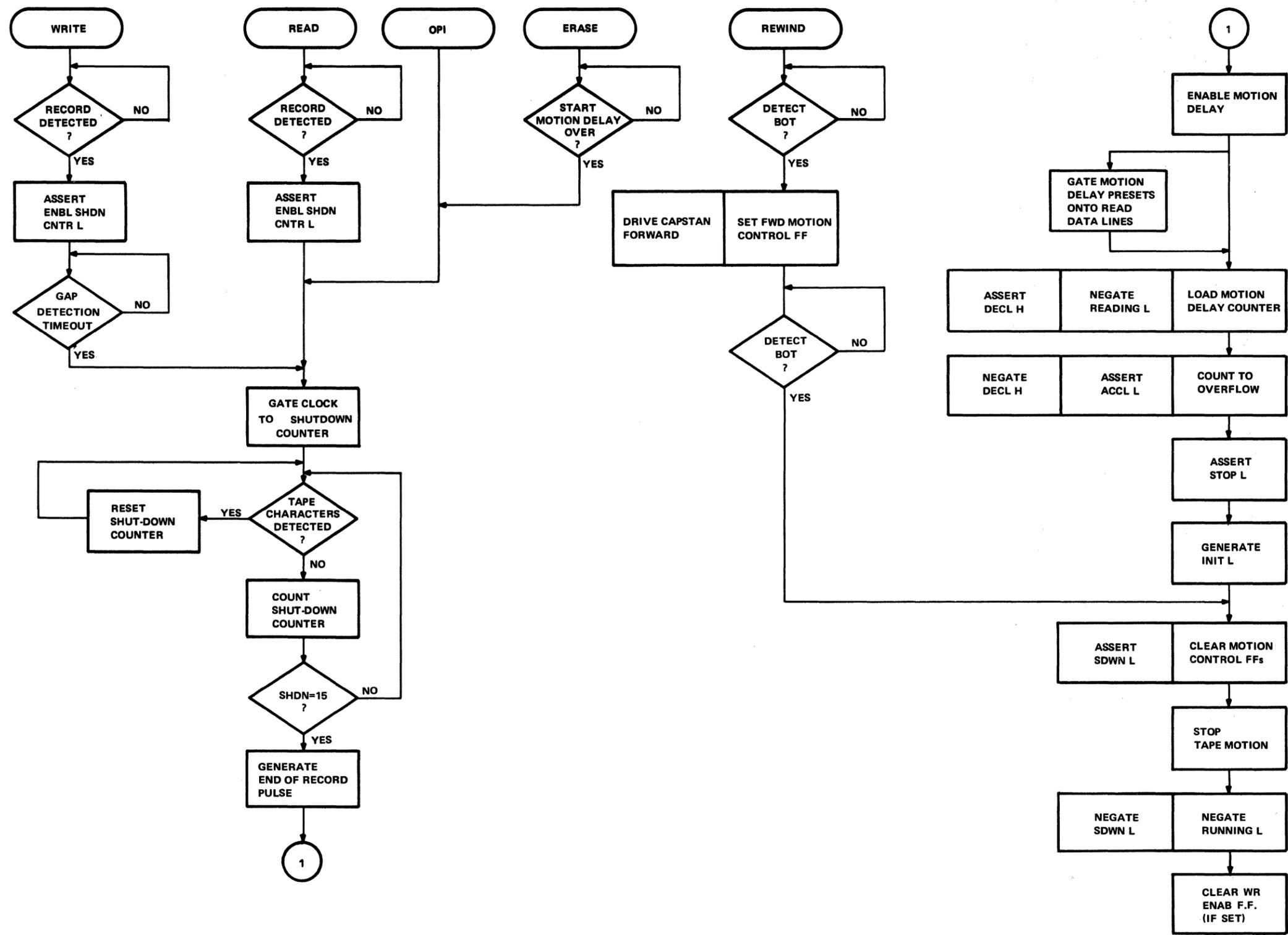
Figure 3.5-10   Tape Motion Termination Flowchart

10-1292

1. The Gap Detection Timer (TCCM 5) is active, because WRT CLK ENBL L is asserted during the write. Thus ENBL SHDN CNTR L cannot gate clock pulses to the Shutdown Counter until 2.7 ms (24 200 BPI CLK pulses) after the last character is written.

2. When tape motion ceases, RUNNING L is negated and clocks the WR ENAB flip-flop clear, thereby de-energizing the write and erase heads.

3.5.7.3 Erase — Termination during an erase follows a sequence similar to that of a write. The sequence starts as soon as the start motion delay is over (READING L asserted). This activates TCCM 5 E41 (pins 8, 9, and 10), and causes the Shutdown Counter to be upclocked immediately, because RST SHDN CNTR L remains unasserted. Thus the stop motion delay follows the start motion delay almost immediately, and tape (aproximately 3 in.) is erased throughout. As in a write operation, the write and erase heads are de-energized after tape motion ceases.

3.5.7.4 Space — Termination during a space is similar to that of a read. Each time an IRG is detected, a stop motion delay is generated, and STOP L is transmitted to the TU16 and clears the motion control flip-flop. However, as soon as SDWN L asserted is received by the TM02, a DRV SET PLS is generated, which produces a start motion delay and a SLAVE SET PLS. This causes the motion control flip-flop to be set once again. Thus, start motion delays and stop motion delays are produced as each record is spaced.

Each time a record is detected, the Frame Count register is incremented. When the Frame Count register overflows, or when a tape mark is detected, further DRV SET pulses are inhibited; the motion control flip-flop remains cleared, and tape motion ceases.

3.5.7.5 Rewind — Once the RWS flip-flop in the TU16 is set, the transport performs the rewind operation independently (Paragraph 3.5.2). The transport rewinds past the BOT marker, then spaces forward until it encounters the BOT marker again. This causes an INIT L to be generated (LAW 8), which clears the RWS and FWD motion control flip-flops, (LAW 7). When tape motion ceases, RUNNING L negated causes RWS L to be negated on the slave bus. It also causes the Set Slave Status Change flip-flop (E60 on LAW 8) to set and assert SET SSC L on the slave bus.

3.5.7.6 Operation Incomplete (OPI) — The OPI bit of the Error register is set when the end of a record is not detected within 7 sec of the initiation of a read or a space operation, or if the end of a record is not detected within 0.7 sec after the initiation of a write operation. If OPI H is asserted, 200 BPI CLK H is gated to the Shutdown Counter. The shutdown sequence begins if or when RST SHDN CNTR L is negated. Thus, if a record has not been detected, shutdown begins immediately. If a record is being detected, the shutdown sequence begins at the end of the record.

3.5.8 Performance Checks
Most failures in tape motion are located by off-line operation and checkout; or by use of the TM02/TU16 Control Logic Test, TM02/TU16 Basic Function Test or TM02 Drive Function Timer diagnostics (see Paragraph 3.1.2). Data reliability problems could also be caused by faulty brakes (Paragraph 4.19.4) or capstan jitter (4.19.2).

3.5.9 Adjustments
The following is a list of adjustments relating to material covered in this pamphlet, with referenced to Chapter 4 where these procedures are located.

Capstan Servo DC Balance	4.19.1
Capstan Speed	4.19.2
Capstan Acceleration and Deceleration Times	4.19.3
Brake Adjustment	4.19.4
Tape Guide Rollers	4.19.8
Read/Write Interlock Assembly	4.19.9
Vacuum Motor Belt Adjustment Procedure	4.19.10

The final three adjustments listed above are mechanical adjustments, and need only be performed when a failure is indicated. The remaining adjustments are electrical, and because of interaction among them should be performed in the sequence listed.

3.5.10 Troubleshooting

3.5.10.1 Tape Motion Troubleshooting Checks — Table 3.5-2 provides checks that can be made for specific trouble symptoms. If the trouble is not found go to Paragraph 3.5.10.2.

3.5.10.2 TM02/TU16 Data Reliability Program Diagnostic — Run the TM02/TU16 Data Reliability Program diagnostic using pattern 1, 800 BPI and 20 characters. Use Table 3.5-3 to analyze the results of the Data Reliability diagnostic.

Table 3.5-2
Tape Motion Troubleshooting Checks

Problem	Symptoms	Remedy
Tape unit will not load.	Vacuum motor does not turn on with load switch but relay on 5410451 energizes.	• Check fuse F1. • Check wiring from P1 on regulator to vacuum motor.
	Vacuum motor does not turn on with load switch and relay on 5410451 does not energize.	• Check harness connections from switch box to M8910. • Check harness connections from M8910 to H606. • Check harness connections from H606 to power supply. • If RELAY ENABLE does not go low (pin 8 of P2 on H606) when load switch is set, check with switch box or M8910.
	Vacuum motor turns on but reel motors do not dump tape into column.	• Check for +17 Vdc INT and -17 Vdc at H606 (DRVR2). • Check for presence of reel motor pulse at TP11 (DRVR6). • Check for assertion of REEL MOTOR ENABLE L on H606 (DRVR6). • Check that reel motors are plugged into H606.
Improper off-line operation.	Capstan does not respond to motion commands but motion indicators are on.	• Check for assertion of FOR and REV at H606 (DRVR6). • Check harness connections from capstan motor to H606. • Check for +16 Vdc, -16 Vdc and P COM INT from power supply (DRVR4).
	Motion flops do not respond to switches.	• Check that START L is setting E51 (LAW 7). • Check negative pulse from 8266 (LAW 7). • Check for assertion of INIT L (LAW 8).
	Capstan moves but tape leaves vacuum column.	• Check vacuum switches (DRVR5, DRVR6). • Check reel motor (DRVR5, DRVR6). • Check reel motor brake circuits (DRVR5, DRVR6).
	Improper EOT/BOT sensor operation.	• Check connections to the EOT/BOT sensor assembly (see Paragraph 4.5). • Check for -6 Vdc on C02B2 of TU16. • Check for appropriate markers on tape. • Check EOT/BOT sensor assembly (LAW6). • Check M8910 module (LAW6).
Improper on-line operation.	———————————	• Check that drive is selected. • Check that drive is on-line. • Check that drive is loaded. • Check cable installation. • Run TM02/TU16 Data Reliability Program.

Table 3.5-3
Trouble Analysis of Data Reliability Diagnostic

Problem	Symptom		Remedy
Runaway ⌈A runaway condition exists when the program starts and the WRT and FWD indicators light at a constant brightness (no flickering), the REV indicator does not light, and depressing the HALT key does not stop tape motion.⌋	No CLOCK (SB) L (144 KHz, 7 μs period) on wire wrap pin D01E1. (See sheet 2 of M8911 schematic)	Pin D01E1 stays at ground level.	Check for bad cable. Check for bad cable connector card. Check for bad M8911. Check for wire wrap pin short.
		Pin D01E1 stays at a logic level (approximately +0.3 to +3.4 Vdc).	Check that jumper is installed on M8911. Check M8911. Check M8913YA.
	No CLR READ BOARD L on pins C03V1 and C04J1. ⌈Approximately 12.5 msec after SET pulse, a series of 100 nsec negative going pulses should appear on pins C03V1 and C04J1. These pulses should be 28 msec apart and within 0.5 volts of ground.⌋		Check C03V1 and C04J1 for shorts. Check the following G056 output pins for shorts: A04B1 A04F1 B04F1 B04K1 C04P1 C04R1 D04V1 E04E1 F04K1 Replace or repair M8911
	G056 outputs stay low and will not reset.		Replace or repair G056
UNS (Unsafe) Error bit asserted in error register ⌈Unsafe error indicates that the TM02 attempted to execute a command with a TU16 that was not on-line or that the TM02 itself is faulty.⌋	———————————		Check that TU16 is on-line.
	Check MOL (SB) L at pin F01V2 for +0.2 to +0.4 Vdc. (See sheet 6 of M8910 schematic.)	MOL is low.	Check that cable connector cards are not loose. Check that cables are routed correctly.
		Set the TU16 to off-line mode. MOL does not go to +3 Vdc.	Check cables. Check cable cards. Check TM02.
	On-line mode is selected at the switch box but the TU16 goes off-line when the program is started.	REWIND (SB) L on pin C01P2 stays	Trouble is in TM02.
		REWIND (SB) L on pin C01P2 changes state.	Replace or repair M8910.
OPI (Operation Incomplete) Error	———————————		Run TU16 Utility Driver Diagnostic. Go to Paragraph 3.5.10.3.

3.5.10.3 TU16 Utility Driver Diagnostic — An OPI error occurring in the TM02/TU16 Data Reliability Program diagnostic of Paragraph 3.5.10.2 can be caused by any of the following:

- SET PULSE is not sent to the TU16.

- Write circuitry fails to write on tape.

- Read circuitry fails.

To troubleshoot an OPI error, run the TU16 Utility Driver Diagnostic by performing the following steps:

a.   Load the TU16 Utility Driver Diagnostic.

b.   Set up the following program parameters:
    Density   800 BPI
    Word Count 10_8
    Frame Count 20_8
    Data Pattern All ones
    Operation   Write

c.   Check that the TU16 is loaded, at BOT and is on-line.

d.   The tape should move forward and the WRT and FWD indicators should light.

Refer to Table 3.5-4 to analyze the results of the Utility Driver Diagnostic.

Table 3.5-4
Trouble Analysis of Utility Driver Diagnostic

Problem	Symptom	Remedy
Tape does not move.	Put HALT ON ERROR switch up to cause the program to pause. Wait for the RUN indicator to go out.	Check the TM02 error register for set-up errors. Check the SET PULSE line for shorts. Check for faulty M8910. Check for bad cable. Check for faulty M9001.
	Restart the program.	Check an A01S2 for SET PULSE (Figure 3.5-11A and sheet 7 of M8910 schematic.) Check FWD at pin C01V2 for a low (0 Volts). Check REV at pin C01V2 for a high (+3 Volts). Check WRITE at pin D01D2 for a low (0 Volts). Check REWIND at pin C01P2 for a high (+3 Volts). Check for bad cables. Check for bad cable card connectors. Check backplane wiring for errors. Check M8910.
	TU16 SEL indicator is not lit.	Check the following signals for a high level (+3 Vdc). SEL 0, Pin B01H2 SEL 1, Pin B01P2 SEL 2, Pin B01M2 STOP, Pin A01V2 (Figure 3.5-11B) INIT PLS, Pin A01U2 DRV CLR, Pin B01D2
Tape moves and REC pulses (pin B01R2) are present (Figures 3.5-11C, D and 3.5-12.)	————————	Check cable. Check cable card connector.
	Signal is low.	Check M8910.
	The 144 KHz pulse train CLOCK is not present on pin D01E1.	Check back panel wiring errors. Check M8911.
	ACC L (SB) L on pin A01H2 should go low (0 volts) for approximately 9.5 msec after SET PULSE and then go high (+3 Vdc). ACCL never goes high.	Check that data lines RD0, RD1, RD2, RD3, RD4, RD5, RD6, RD7 and RDP are between +3.5 and +4.5 Vdc. (Some RD lines may go low when the SET PULSE occurs but most of them should remain high.)
	————————	Check that EMD pulse on pin B01E2 goes low for 2.8 or 42 msec after SET PULSE, and then goes high.

Table 3.5-4 (Cont)
Trouble Analysis of Utility Driver Diagnostic

Problem	Symptom		Remedy
	WRITE CLOCK (SB) L on pin D01E2 is a 36 KHz (28 sec) square wave that starts when ACC L (SB) L goes high and continues until ACC L (SB) L goes low. WRITE CLOCK is missing.		Check back panel for wiring errors. Check M8911.

No analog signals on pin A04L1 (Figures 3.5-11E and ? 5-13).	Tape moves and REC pulses are present.		Check the writers.
			Check the write cable.
			Check M8910 (see Sheets 2 and 3 of M8910 schematic).
			Check that WRITE CLOCK jumpers are properly connected to back panel.
			Check that write buffer is being clocked.
			Check that write voltage (orange wire) is approximately +12 Vdc (+5.5 Vdc for PE or Off-line mode).
			Check that the following wires to G056 are at the specified voltages:
			    Red = +5 Vdc
			    Yellow = +12 Vdc
			    Green = -6 Vdc
			Check the read and write cables.
			Check that the WD lines (WD0, Wd1, ---) go low (0 volts) for approximately 400 μsec during the period when REC pulses occur.

No RSDO pulses on pin C01K2 (Figures 3.5-11F and 3.5-14).	Tape moves, REC occurs and analog signals are present.		Check that all RD lines on G056 go low.
			
			Check for 100 nsec CLEAR RD BRD L pulse on pin C03V1 (see Sheet 3 of M8911 schematic).
			Check for back panel wiring shorts.
			Check that there are no connections to the following back panel pins:
			    D03P1 D03E2 D03N2
			    D03N1 D03M1 D03T2

OPI error remains.	Tape moves, REC occurs, analog signals are present an0 RSDO pulses are present.		Replace or repair M8913 and cable B. Run the TU16 with another TM02.
		Less than 16 RSDO pulses are generated.	Check back panel wiring for errors.

3.5-21
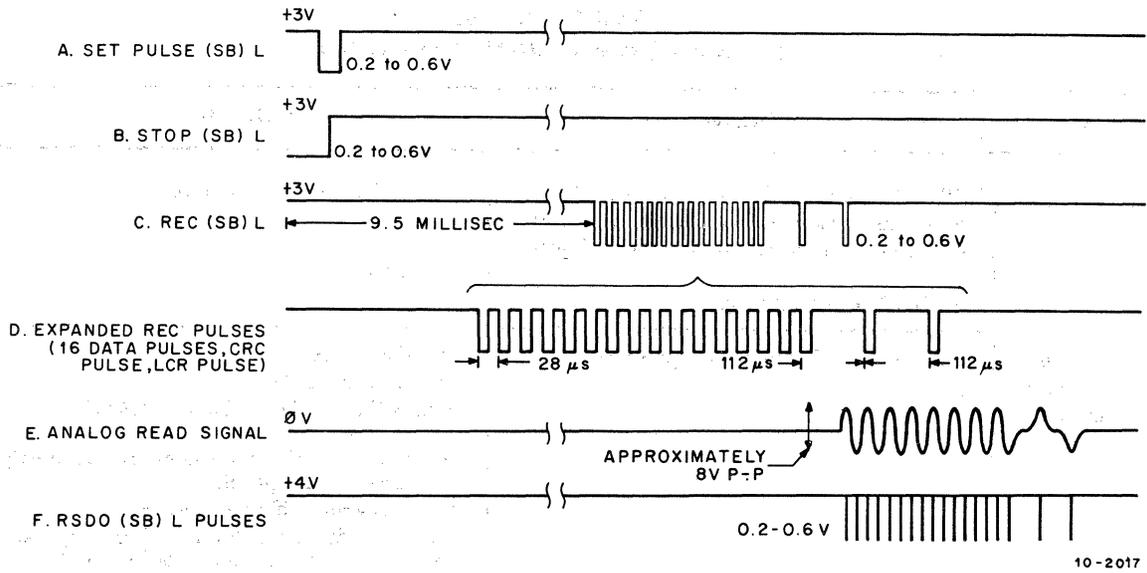
Figure 3.5-11   Time Relationships of Write Operation Signals
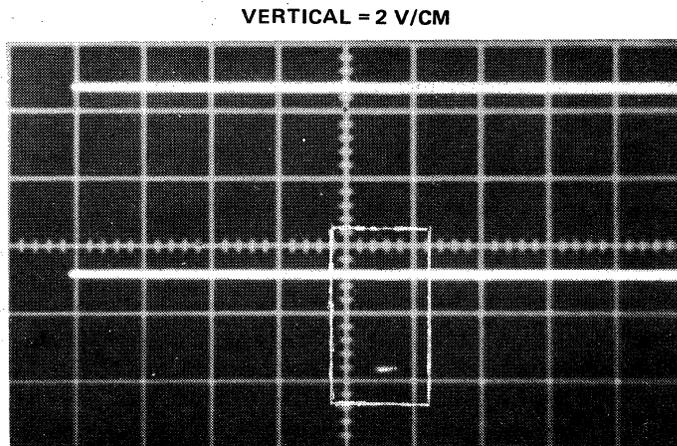
VERTICAL = 2 V/CM

Note: REC Pulses in box

A. SWEEP SPEED = 2 MS/CM
TRIGGER = SET PULSE
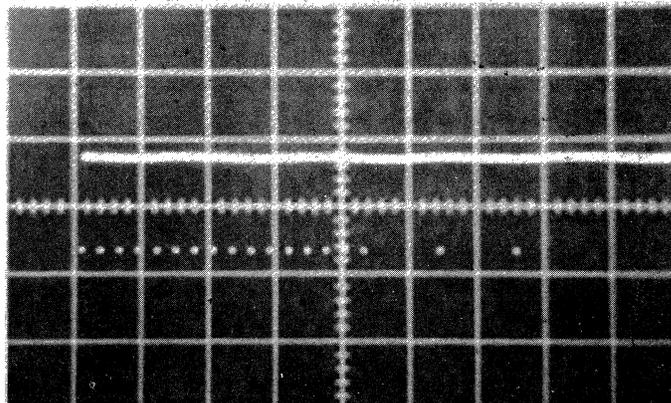
VERTICAL = 2 V/CM

B. SWEEP SPEED = 0.1 MS/CM
TRIGGER = FIRST REC PULSE

Figure 3.5-12   Waveforms of REC Pulses (16 data pulses, CRC pulse, LRC pulse)

3.5-22
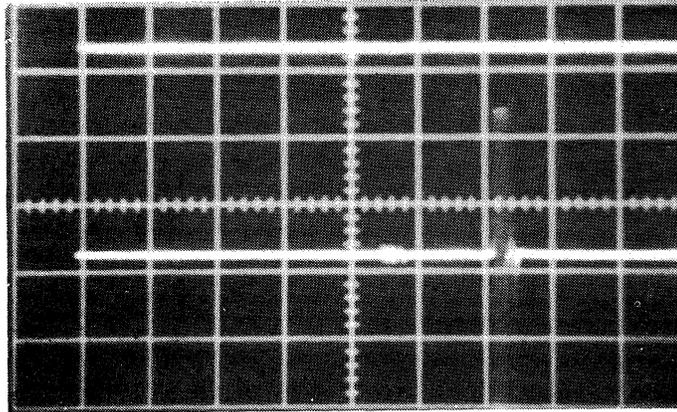
VERTICAL = 2 V/CM

Note write crosstalk 9 ms from start of trace.
A. SWEEP SPEED = 2 MS/CM
TRIGGER = SET PULSE
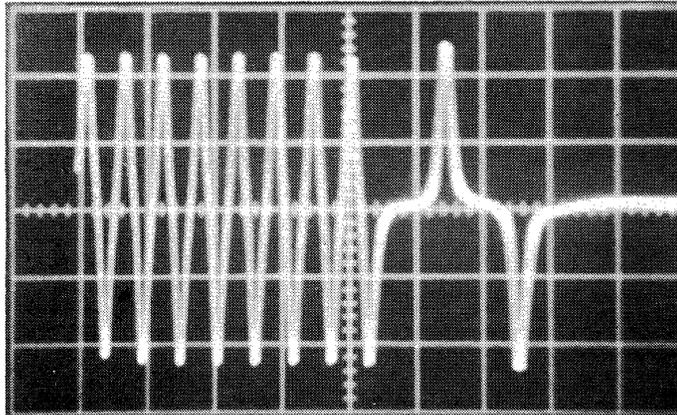
VERTICAL = 2 V/CM

B. SWEEP SPEED = 0.1 MS/CM
TRIGGER = FIRST ANALOG SIGNAL

Figure 3.5-13   Waveforms of Analog Read Signals

VERTICAL = 2 V/CM
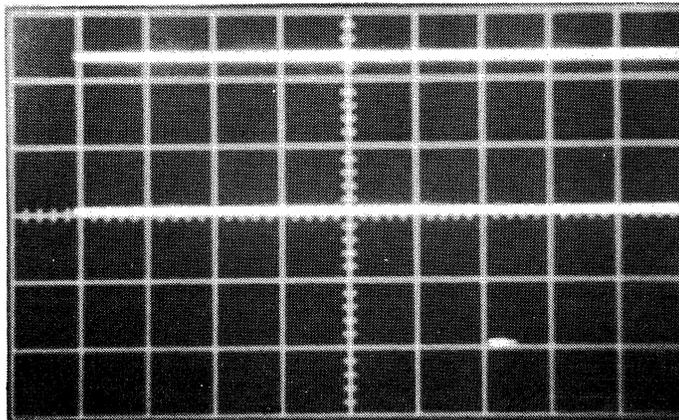
TRIGGER = SET PULSE
SWEEP SPEED = 2 MS/CM

Figure 3.5-14   Waveform of RSDO Pulses

3.5-23

CONTENTS

3.6 INTRODUCTION

This pamphlet discusses the operation of the TU16/TM02 read circuitry when operating in PE mode. The PE read data path (reference Figure 2-6) is covered from the read heads to the inputs of the Bit Fiddler. Bit Fiddler read operation is described in pamphlets 3.8 (M8906) and 3.9 (M8914).

3.6.1 Read Heads and Amplifiers

As tape moves past the read heads, flux transitions on the tape cause the read head to produce voltage pulses; the direction of flux transition determines the polarity of the output pulses. The read preamplifier (Figure 3.6-1 and G056 schematic), consisting of two type 72733 differential video amplifiers then inverts the read head signals. Each differential output of the read preamplifier is inverted and further amplified by a group of three transistors; the final two transistors operate in push-pull mode. The resulting amplified differential signals are then input to opposite sides of a delay lines. A phase shift of about 6 degrees (Figure 3.6-2) occurs across the delay line; this phase shift is utilized by the peak detector. The peak detector is a comparator circuit whose output changes state when the relative magnitude of its inputs changes (i.e., when one input becomes greater or less than the other); this occurs at the peaks of the read head signals.

Output transitions of the peak detector circuit are converted into pulses by the dual edge pulse amplifier; these pulses strobe the dual threshold gate. The dual threshold gate compares its input (amplifier output) to positive and negative threshold voltages (Figure 3.6-3). If the input is more positive that the POS RD THRESHOLD at strobe time, a negative pulse is produced at the + output. If the input is more negative than the NEG RD THRESHOLD, a negative pulse is produced at the - output.

The outputs of the G056 Read Amplifier are routed to the slave bus via a type 8266 multiplex on the Slave Clock and Motion Delay module (M8911, sheet 2) and drivers on the Data Driver module (M8913) (refer to Figure 2-6). The read data signals are then transmitted to the TCCM module in the TM02, where they are multiplexed to the three Data Sync modules (M9001).

Read threshold voltages are determined by the signals PES L and WRE H input to a 74156 data selector chip (Figure 3.6-3). Depending on these inputs, one of four transistors is turned on. Since each transistor has a different collector resistor, a programmable current (+ Threshold Voltage) is obtained. The + Threshold Voltage is fed to a 72741 O-Amp to produce an equal, but opposite polarity - Threshold Voltage. These threshold levels are used by the Read Amplifiers to establish the lowest acceptable signal level.

A pulse at the + output of the dual threshold gate sets the 7476 J-K Read Data flip-flop. A pulse at the - output will clear the flip-flop, because when reading in PE mode, the J input is low and the K input is high. The
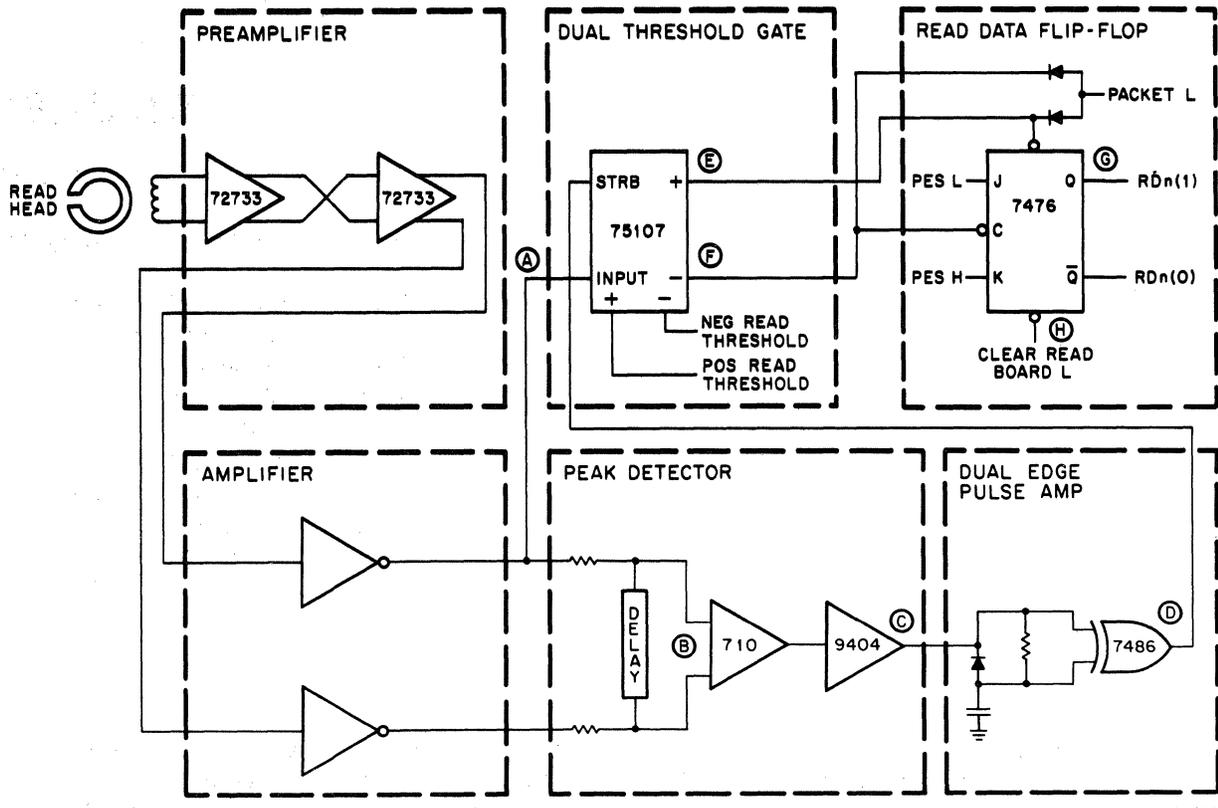
Figure 3.6-1   Equivalent Circuit of Read Circuitry for One Track
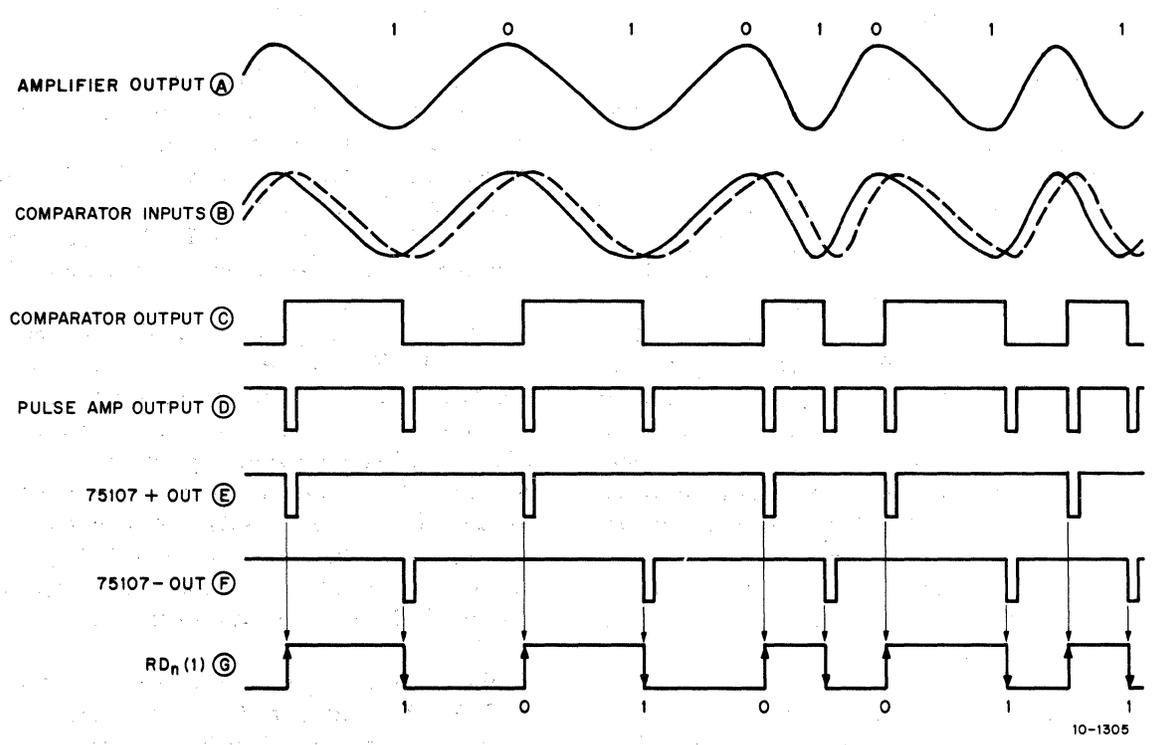
Figure 3.6-2   Read Amplifier Waveforms

3.6-2

	PES L B	WRE H A	Y_3	Y_2	Y_1	Y_0
PE·$\overline{WRE}$	0	0	1	1	1	0
PE·WRE	0	1	1	1	0	1
NRZ·$\overline{WRE}$	1	0	1	0	1	1
NRZ·WRE	1	1	0	1	1	1
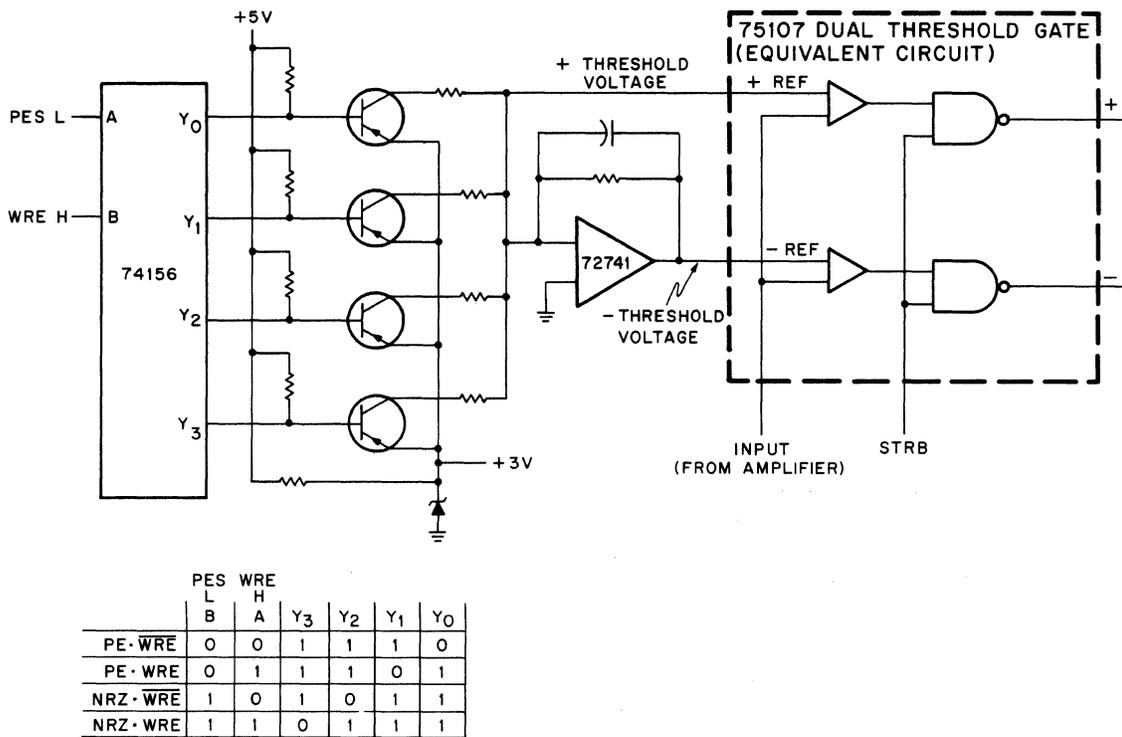
10-1288

Figure 3.6-3   Programmable Threshold

output of the Read Data flip-flop follows the polarity of the magnetic field on the tape; it contains the data in phase encoded form.

3.6.2   Data Sync

The Data Sync module (M8901) contains three sections, each of which processes a single track of read data (Figure 3.6-4). Each of these sections contains a data discriminator, a phase-locked clock, a Deskew Buffer, error detection circuitry, and error correction circuitry (Figure 3.6-5). To process nine tracks of data, three Data Sync modules are required.
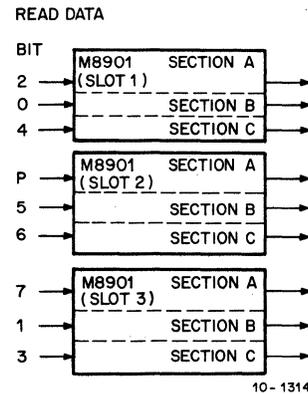
Figure 3.6-4   Data Sync Channels
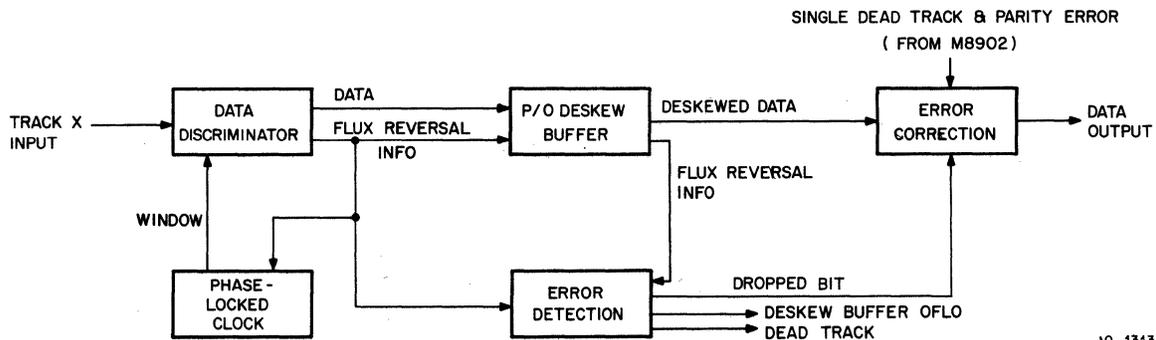
Figure 3.6-5   One Section of the Data Sync Module

NOTE
Operation of all sections of the M8901 Data Sync
module is identical. Therefore, all discussions of
Data Sync operation reference section A sche-
matics (DS 2 and 3), unless otherwise specified.

3.6.2.1 Phase-Locked Clock — Conversion of phase
encoded data into binary data requires generation of a
data window for each track in sync with the data transi-
tions in the track. The direction of the data transition
within the data window determines whether a 1 or a 0
bit is detected.

The phase-locked clock (DS 3) operates to generate the
data window and to keep it in sync with the incoming
data stream. The heart of the phase-locked clock is a
voltage controlled oscillator (VCO) and a phase detec-
tor (type 4044). The phase detector senses the phase re-
lationship between incoming data transitions (BIT
STRB) and the VCO output signal divided down to the
data frequency. If the frequency of data transitions
increases (decreases), BIT STRB begins to lead (lag)
TP3. This increases (decreases) the VCO output fre-
quency and brings the two signals back in phase. Thus,
the frequency of TP3 becomes the same as the fre-
quency of BIT STRB. The data window (WINDOW) is
generated 90 degrees out of phase with TP3 (DS3 and
Figure 3.6-6).
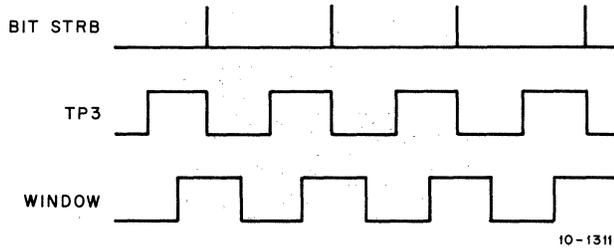
Figure 3.6-6 Data Window Generation

3.6.2.2 Data Discriminator — The data discrimi-
nator converts the phase encoded data on its track into
binary form: 1 = high, 0 = low. To do so, the data win-
dow must first be synchronized to the frequency of the
incoming data. It is for purposes of synchronization
that the preamble is used.

To understand the operation of the data discriminator,
it should be noted that the data discriminator operates
in three modes (Figure 3.6-7).
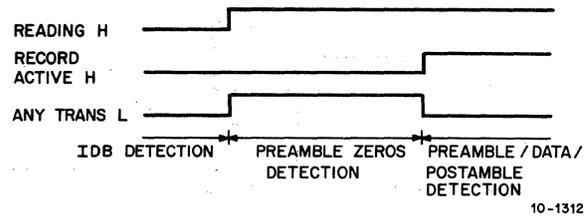
Figure 3.6-7 Data Discrimination Modes

1. During the start motion delay, READING H
    is negated, causing ANY TRANS L (Any
    Transition) to be asserted (TCPE 5). During
    this condition, IDB may be detected (Para-
    graph 3.6.7).

2. When the motion delay times out, ANY
    TRANS is negated. During this condition,
    preamble 0s may be detected (Paragraph
    3.6.3).

3. When 24 preamble 0s are detected,
    RECORD ACTIVE and ANY TRANS are
    asserted. During this condition, the pre-
    amble 1s character and data are detected
    (Paragraph 3.6.4).

3.6.2.3 Deskew Buffer — Each Deskew Buffer (DS3)
stores the binary data detected by the data
discriminator until a whole tape character becomes
available. Because eight bits of data can be stored for
each track, a skew of up to seven tape characters can be
accommodated.

The Deskew Buffer is implemented by nine type 74172
2 by 8 random access registers. Each register buffers
data (RD BUFFER I) and flux reversal information
(BIT STRB OCCURRED) for a single track. Each
register is loaded as data bits become available. The
output of the register depends on its RD ADDR input
(common to all the registers that make up the Deskew
Buffer), and is read when a whole tape character be-
comes available. The RD ADDR is then incremented,
and the read circuitry waits for the next tape character
to become available. Deskew Buffer operation is des-
cribed in more detail in Paragraph 3.6.4.1.

3.6.2.4 Error Detection — The error detection cir-
cuitry senses when a data transition fails to occur.
Error detection is described in more detail in Para-
graph 3.6.4.2.
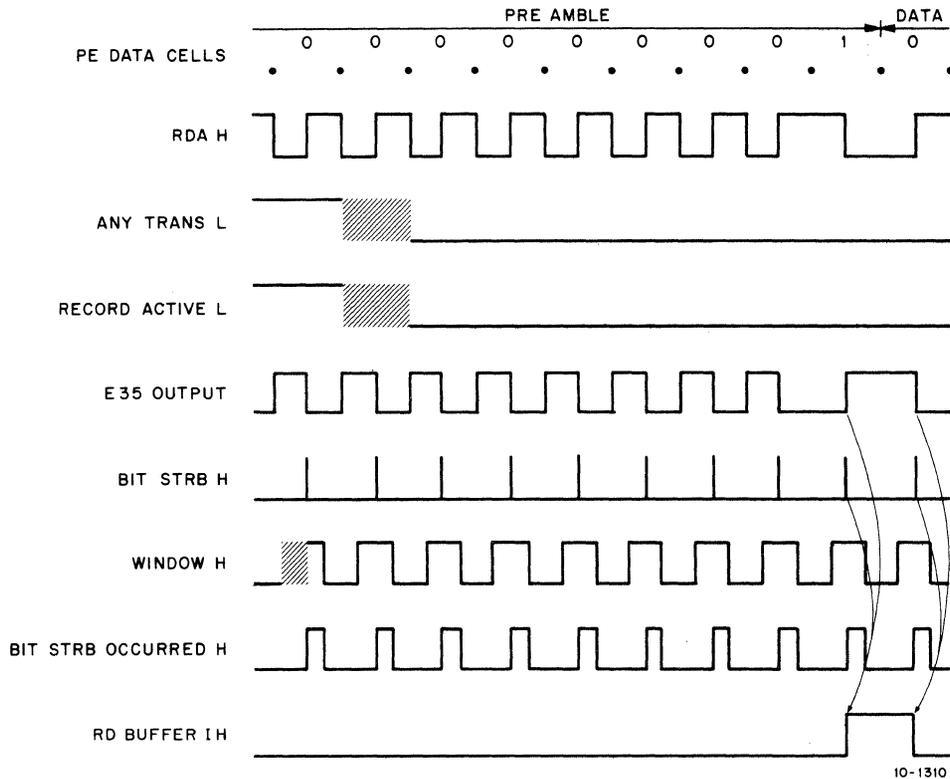
Figure 3.6-8 Data Discriminator Timing Diagram

3.6.2.5 Error Correction — The error correction circuitry performs on-the-fly error correction. Error correction is described in more detail in Paragraph 3.6.4.2.

3.6.3 Preamble Detection

Because all sections of the Data Sync modules operate in the same manner, this discussion describes the operation of one section: M8901, Section A, (DS 2 and 3). Reference Figures 3.6-8 and 3.6-9.

The preamble 0s (A RDA H) are input to an XOR gate which inverts A RDA H if tape motion is in the forward direction (REV L negated). The output of E35 is of proper polarity for both forward and reverse read operations. Another XOR gate together with an inverter and their associated circuitry, function to produce a positive pulse (BIT STRB H) each time the output of E35 (E31 for Rev. B circuit schematic) transitions. However, because ANY TRANS is negated and E14 and E24 (E15 and E35 for Rev. B circuit schematic) are "common collectored," BIT STRB H pulses are produced only on negative-going transitions. (The negative-going transition corresponds to the data transitions of preamble 0s.)

This operation synchronizes WINDOW H with the incoming data. On its trailing edge, BIT STRB H asserts BIT STRB OCCURRED. Since BIT STRB OCCURRED H is asserted when WINDOW H is negated, ENV H is generated (DS 3). Each time the output of E35 transitions low, BIT STRB H is asserted; ENV H remains asserted as long as BIT STRB occurs at the expected data rate.

When ENV H is detected on a sufficient number of tracks (TCPE 4), a clear input is removed from the character counter (E9 and E14), allowing it to be up-counted by DATA HALF H. Because DATA HALF occurs at the PE data rate, the outputs of the character counter represent the number of preamble 0s read. When the character counter reaches a count of eight (CT 3 H asserted), the Preamble flip-flop is set (TCPE 5). When the character counter reaches a count of 24 (CT 3 H and CT 4 H asserted), the Record Active flip-flop is set. With RECORD ACTIVE asserted, ANY TRANS L is asserted, and the data discriminator operates in its third mode. By this time, the phase-locked clock is synchronized to produce WINDOW H in sync with the Data being read.

3.6-5

As preamble 0s continue, WINDOW H is always asserted at the time E35's (E31 for Rev. B) output transitions low. This transition produces a BIT STRB H pulse which clocks the Read Buffer. But because E35's output is already low, the buffer remains reset.

3.6.4 Data Detection

When the preamble 1s character appears (Figure 3.6-8), BIT STRB H is produced at the positive transition of E35's (E31 for Rev. B) output (DS 2), thereby setting the Read Buffer flip-flop. Because WINDOW H has been synchronized to the PE data transition time, BIT STRB H occurs only during the data transition time, and will set or clear the Read Buffer depending on the direction of transition. Therefore, the binary output of the Read Buffer is a decode of the RDA phase encoded data.

3.6.4.1 Deskew Buffer — Whenever WINDOW H is negated, the Deskew Buffer (DS 3, 74172) is loaded with the contents of the Read Buffer and Bit Strobe Occurred flip-flops. However, during the preamble, only location 000 is loaded each time. When the preamble 1 bit is detected, ONE DETECTED (1) H is asserted (DS 3). ONE DETECTED (1) H enables the Write Address Generator to increment the Deskew Buffer write address. Thus, the preamble 1s bit is loaded into address 000. The next bit, i.e., the first data bit, is also loaded into address 000 (Figure 3.6-10). The address is now incremented on each leading edge of WINDOW H, so that the second data bit is loaded into 001, the third into 010, etc. After the eighth data bit, the write address becomes 000 again, and the cycle continues.

With ONE DETECTED asserted, counter E34 (E27 for Rev. B) (DS 2) is enabled to determine Deskew Buffer status. Each time a data bit is loaded into the Deskew Buffer, the count of E34 is decremented. Each time the Deskew Buffer is read, the count is incremented. Thus, the counter keeps track of how many unread data bits are in the Deskew Buffer.

When the Deskew Buffer contains an unread data bit in each track, BIT READY H (common collectored) is asserted. BIT READY H causes CHAR SHIFT H and ENB RDS L to be asserted (TCPE 3). CHAR SHIFT generates RD SYNC (0) H, which upcounts the Deskew Buffer Status Counters, thereby causing BIT READY H to be negated. CHAR SHIFT also increments the Deskew Buffer read address (TCPE 4). ENB RDS L enables generation of RDS L by succeeding BIT READY H pulses. RDS L causes the output of the Data Sync modules [i.e., the contents of Buffer B (Paragraph 3.6.4.2)] to be read and assembled by the Bit Fiddler.

If skew of more than seven characters occurs during the read operation, the Deskew Buffer Status Counter of the leading track will be downcounted to seven, causing OVERFLOW L to be asserted. This sets the INC/VPE error bit in the Error register. A skew of three or more characters causes the CS/ITM bit of the Error register to be set.

3.6.4.2 Error Detection and Correction — If BIT STRB does not occur during any data cell, ENV H is negated and the DD TRK (Dead Track) flip-flop (DS 3), E39 (E49 for Rev. B), is set. When the data of this data cell is read from the Deskew Buffer and loaded into Buffer A, E22 (E19 for Rev. B), DROPPED BIT H will be generated as well. The outputs of Buffer A of each track are input to a Parity Generator/Checker (TCPE 2). If there is only one dropped bit and a parity error is detected, PERR AND ONE DD TR H is generated; this means that the content of Buffer A of the dead track is of the wrong polarity. When the next CHAR SHIFT H is generated, this bit is corrected as it is clocked into Buffer B; thus, on-the-fly error correction is achieved.

The outputs of Buffer B are gated by PES B H (Phase Encoded Status Buffered), and become RD B (Read Data B). The RD B lines are multiplexed in the Maintenance Register module (MR 2) and become RD C (Read Data C), and are then transmitted to the Bit Fiddler.

3.6.5 Postamble Detection

If on any track, a 1 bit followed by a 0 bit is read, POST PAT L is asserted (DS 3 E28). If this occurs simultaneously on all tracks, POST DETECT A, B, C, H is asserted, and the Postamble flip-flop (TCPE 5) is set.

With the Postamble flip-flop set, the character counter is further upcounted, and, when a count of 32 is reached (CT 5 H asserted), MID POSTAMBLE (1) is asserted. This signal loads the Check Character register (R07) with dead track information (MR 4).

3.6.6 IRG Detection

If the read heads are passing over a portion of erased tape, no envelopes will be detected, and ANY ENV H will be negated. This also causes RS SHDN CNTR L (Reset Shutdown Counter) to be negated (TCPE 5), and allows the Shutdown Counter (E51 on TCCM 5) to be upcounted by 200 BPI CLK H. When a count of 15 is reached, EORS H and RECORD H are asserted. RECORD H indicates that an IRG is detected, while EORS H causes a stop motion delay to be generated.

3.6-6
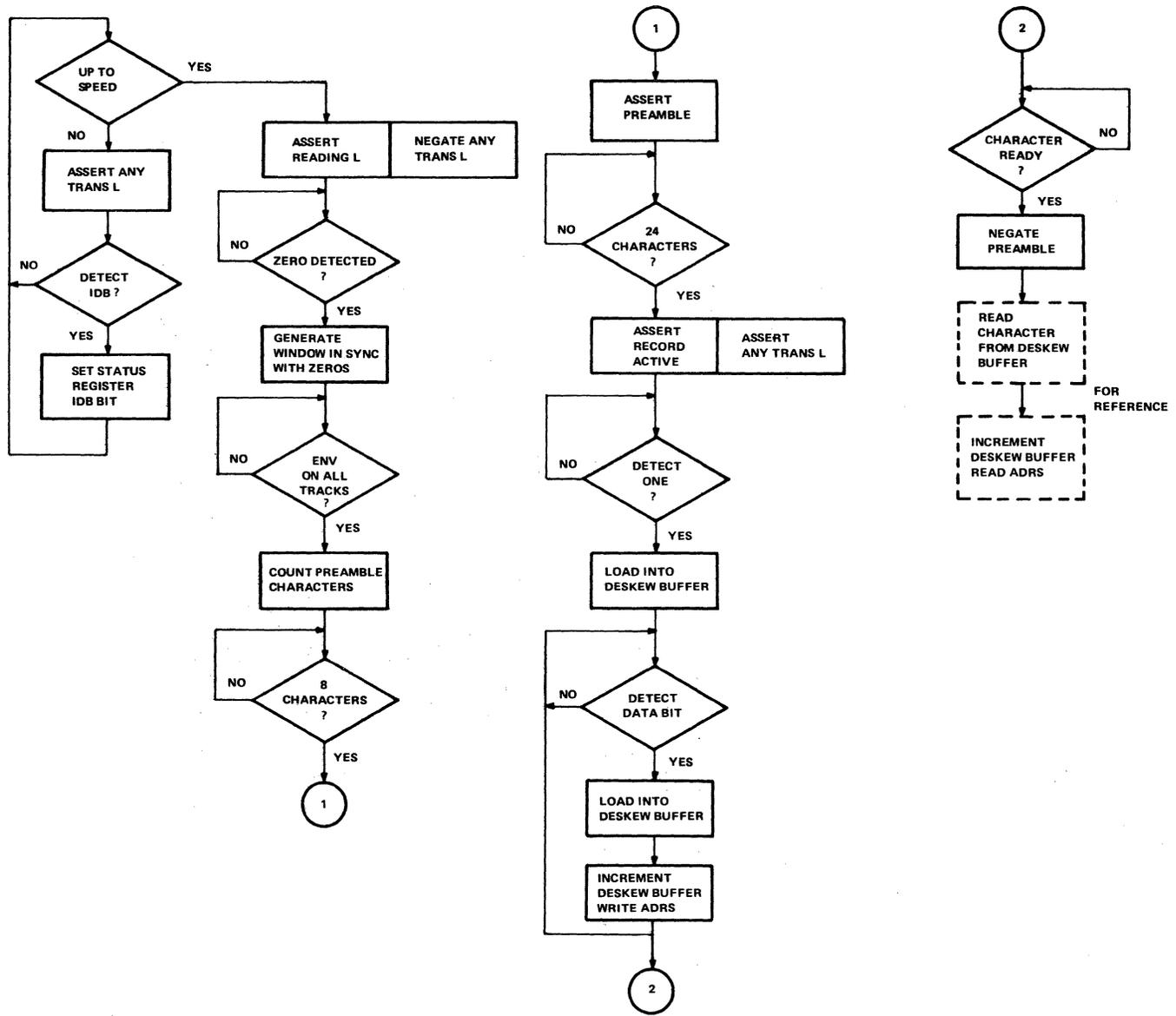
Figure 3.6-9   Preamble/IDB Detection Flowchart

3.6-7

10-1332

```
                    ┌──────────────┐
                    │   DETECT     │◄── NO
                    │   DATA BIT   │
                    └──────────────┘
                          │ YES
                    ┌──────────────┐
                    │ LOAD INTO    │
                    │ DESKEW BUFFER│
                    └──────────────┘
```
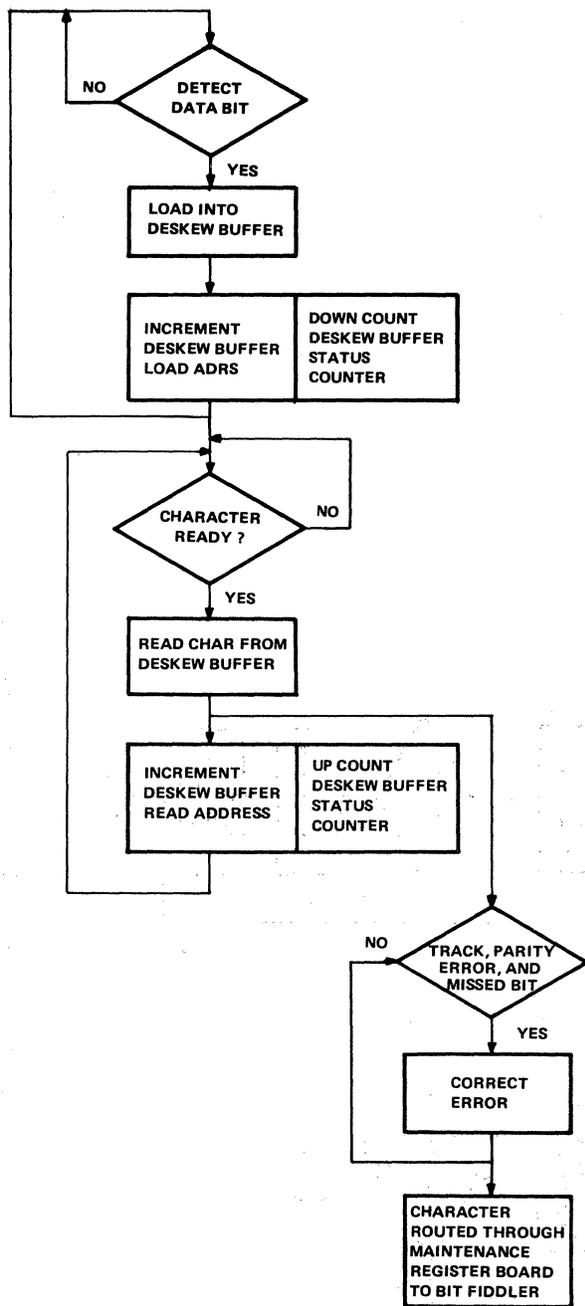
Figure 3.6-10   Data Sync Data Read Flowchart

IO-1333

3.6.7 IDB Detection

When the IDB is encountered, the parity read line contains alternate 1s and 0s; no other read lines transition.

The parity line (A RDA) is input to pin 9 of XOR gate E35 (DS 2 and Figure 3.6-11) on the Data Sync module in slot C02. If tape is moving in the forward direction (REV L negated), A RDA is inverted. Thus, the output of E35 is of proper polarity for both forward and reverse tape motion.

Gates E15 and E14 and their associated circuitry produce a narrow pulse BIT STRB H each time the output of gate E35 transitions. BIT STRB H sets ENV H. ENV H will remain asserted throughout the IDB.

During the IDB, the only track generating ENV H will be the parity track (track 4). This condition is recognized by circuitry on the Tape Control-PE module (TCPE 4), and allows the IDB Timer to be upcounted by 200 BPI CLK H. When the IDB Timer reaches a count of 8, IDB H is asserted; this prevents further counting of the IDB Timer, and asserts the IDB bit of the Status register (R01).

3.6.8 Tape Mark Detection

A PE tape mark is defined as 0s in tracks 2, 5, and 8, while tracks 3, 6, and 9 are erased. This pattern is recognized in the TM02 by the generation of ENV H in tracks 2, 5, and 8, while tracks 3, 6, and 9 do not generate ENV. When this condition is detected, (TCPE 4) FMK PATTERN is asserted, and the corresponding bit in the Status register (R01) is set.

3.6.9 Performance Checks

Use the TM02/TU16 Data Reliability Program diagnostic (see Paragraph 3.1.2) for a performance check on the Read (PE) circuitry.

3.6.10 Adjustments

The following adjustments directly affect proper operation of the TU16/TM02 read circuitry:

Read Amplitude Adjustment (Paragraph 4.19.5)
Read Skew Adjustment (Paragraph 4.19.6)

3.6.11 Troubleshooting

To troubleshoot the Read (PE) function, run the TM02/TU16 Data Reliability Diagnostic and use Table 3.6-1 to analyze the results.
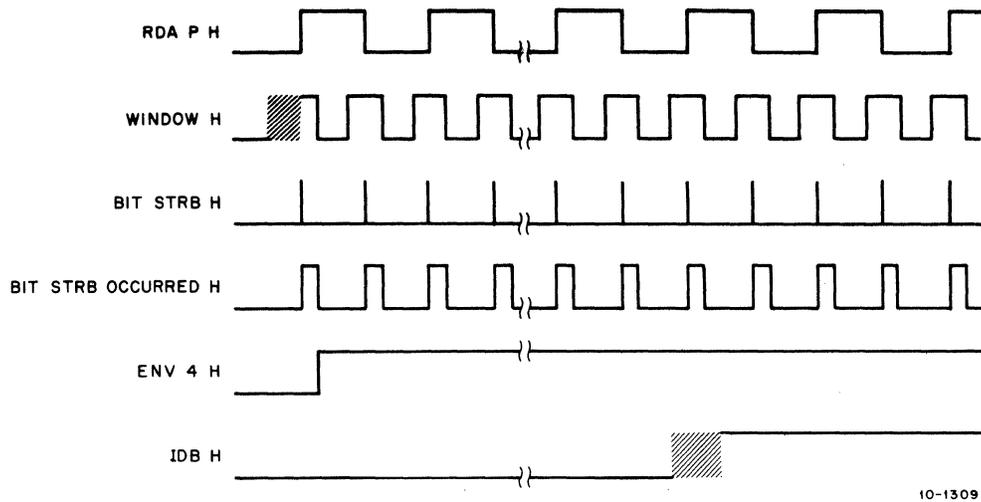
Figure 3.6-11   IDB Detection Timing Diagram

Table 3.6-1
Analysis of Data Reliability Diagnostic for Read (PE) Troubleshooting

Problem	Symptom	Remedy
FCE (Frame Count Error)	Postamble detected too soon.	Check postamble detect circuitry on M8901 (DS 3, 5, 7) Check postamble flip-flop on M8902 (dwng TCPE5)
	Error caused by certain data patterns.	Check for dead track.
		Check EBL on M8909 (dwng MBI9) Check RUN from RH controller and on MASSBUS.
CORR SKEW Error	One or more tracks using third stage of deskew buffer (M8901 - DS2, M8902; Dwng TCPE 2)	Problem is one track sensing end of preamble too soon or too late.
CORR SKEW Error and CORR DATA Error	One track is missing.	Check for damaged tape.
NSG Error	During a read operation one or more channels of read data completes a record in the wrong state. e.g. Overshoot on the last transition being recognized as an extra transition.	Check for poorly written tape. Check G056.
	Some unerased data left in the IRG.	Check for misaligned erase head.

Problem	Symptom		Remedy
PEF, CDE, INC Errors			Check tape for dirt and defects. Check for capstan jitter. Check operation of phase locked loop. Check deskew buffer. Check G056. Check read states circuits on M8902.
Incorrectable data error with all zeros in check character register and no CS/ITM error.	Parity error exists with no dead track.		Check for defective component in the deskew buffer (DS 3, 5, 7; Dwng TCPE 2).
Check Character Register repeatedly contains the same bit set.*	Trouble is in only one track. Swap the M8901 modules	Trouble is in same track.	Check for trouble in TU16. Check analog and digital outputs of G056.
		Trouble is in different track	Check M8901.
PEF Error	More than one dead track due to improper detection of preamble and postamble.		Check for poor quality tape. Check tape speed regulation.

*A 777 in the check character register may indicate a late detection of postamble which causes the check character register to be strobed at the wrong time.

READ (NRZ)

CONTENTS

3.7 INTRODUCTION

This pamphlet discusses the operation of the TU16/TM02 read circuitry when operating in NRZ mode. The NRZ read data path (reference Figure 2-6) is covered from the read heads to the inputs of the Bit Fiddler. Bit Fiddler read operation is described in pamphlets 3.8 (M8906) and 3.9 (M8914).

3.7.1 Read Heads and Amplifiers

As tape moves past the read heads, flux transitions on the tape cause the read head to produce voltage pulses; the direction of flux transition determines the polarity of the output pulses. The read preamplifier (Figure 3.7-1), consisting of two type 72733 differential video amplifiers, then inverts the read head signals. Each differential output of the read preamplifier is inverted and further amplified by a group of three transistors; the final two transistors operate in push-pull mode. The resulting amplified differential signals are then input to opposite sides of a delay lines. A phase shift of about 6 degress (Figure 3.7-2) occurs across the delay line; this phase shift is utilized by the peak detector. The peak detector is a comparator circuit whose output changes state when the relative magnitude of its inputs changes (i.e., when one input becomes greater or less than the other); this occurs at the peaks of the read head signals.

Output transitions of the peak detector circuit are converted into pulses by the dual edge pulse amplifier; these pulses strobe the dual threshold gate. The dual threshold gate compares its input (amplifier output) to positive and negative threshold voltages (Figure 3.7-3). If the input is more positive than the POS RD THRESHOLD at strobe time, a negative pulse is produced at the + output. If the input is more negative than the NEG RD THRESHOLD, a negative pulse is produced at the - output.

Read threshold voltages are determined by the signals PES L and WRE H input to a 74156 data selector chip (Figure 3.7-3). Depending on these inputs, one of four transistors is turned on. Since each transistor has a different collector resistor, a programmable current (+ Threshold Voltage) is obtained. The + Threshold Voltage is fed to a 72741 Op-Amp to produce an equal but opposite polarity - Threshold Voltage. These threshold levels are used by the Read Amplifiers to establish the lowest acceptable signal level.

Whenever the dual threshold gate produces an output pulse, PACKET L is asserted, and the Read Data flip-flop is set. This signifies that a one-bit has been detected on the tape track. Because of parity conventions, at least one of the TU16's Read Amplifiers will detect a flux transition (a one-bit) as a tape character is read. When the first one-bit of a tape character is read, and the corresponding Read Data flip-flop is set, START SKEW DELAY is asserted. This sets the Skew flip-flop and initiates a read deskew timing sequence, at the end of which SDO H (Skew Delay Over) and RSDO (Read Strobe Delay Over) are asserted.

SDO H generates CLEAR READ BOARD L, which clears the Read Data flip-flop in each Read Amplifier. RSDO L is transmitted via the slave bus to the TM02, where it is used to generate RDS H (Read Strobe).

3.7-1
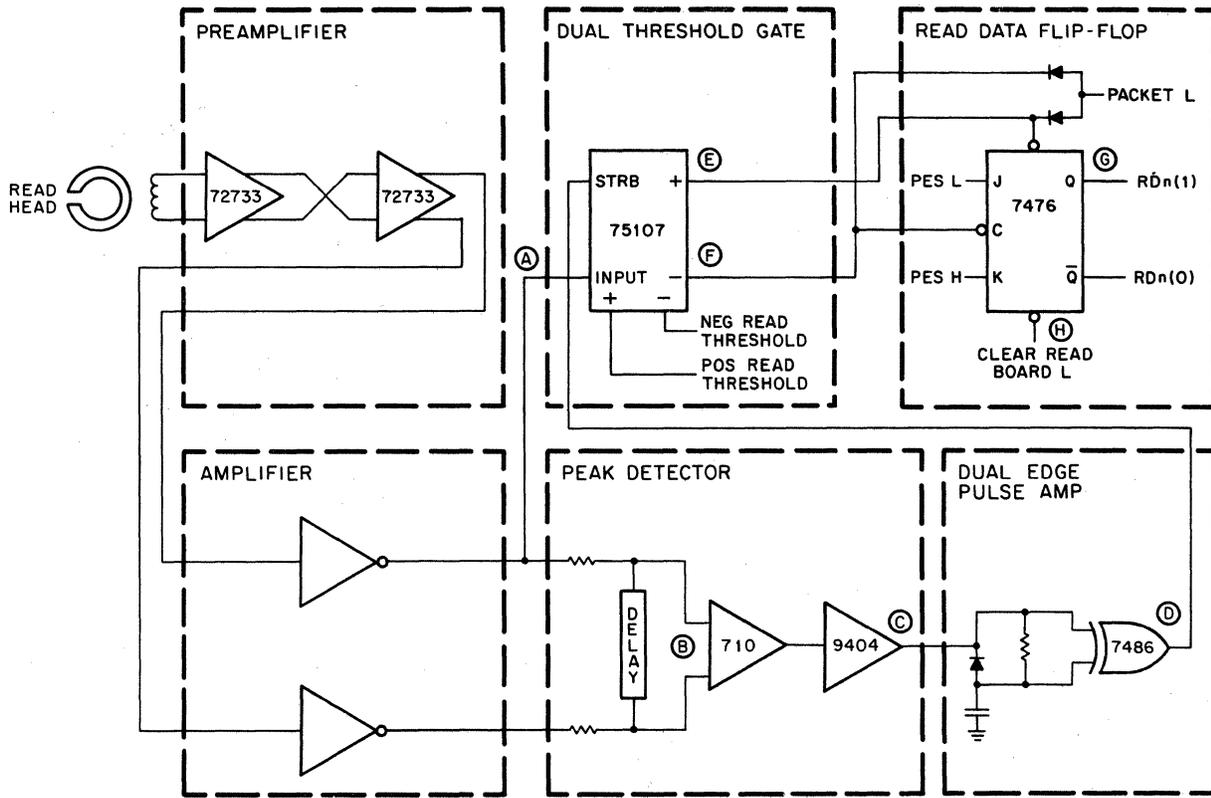
Figure 3.7-1 Equivalent Circuit of Read Circuitry for One Track

10-1290
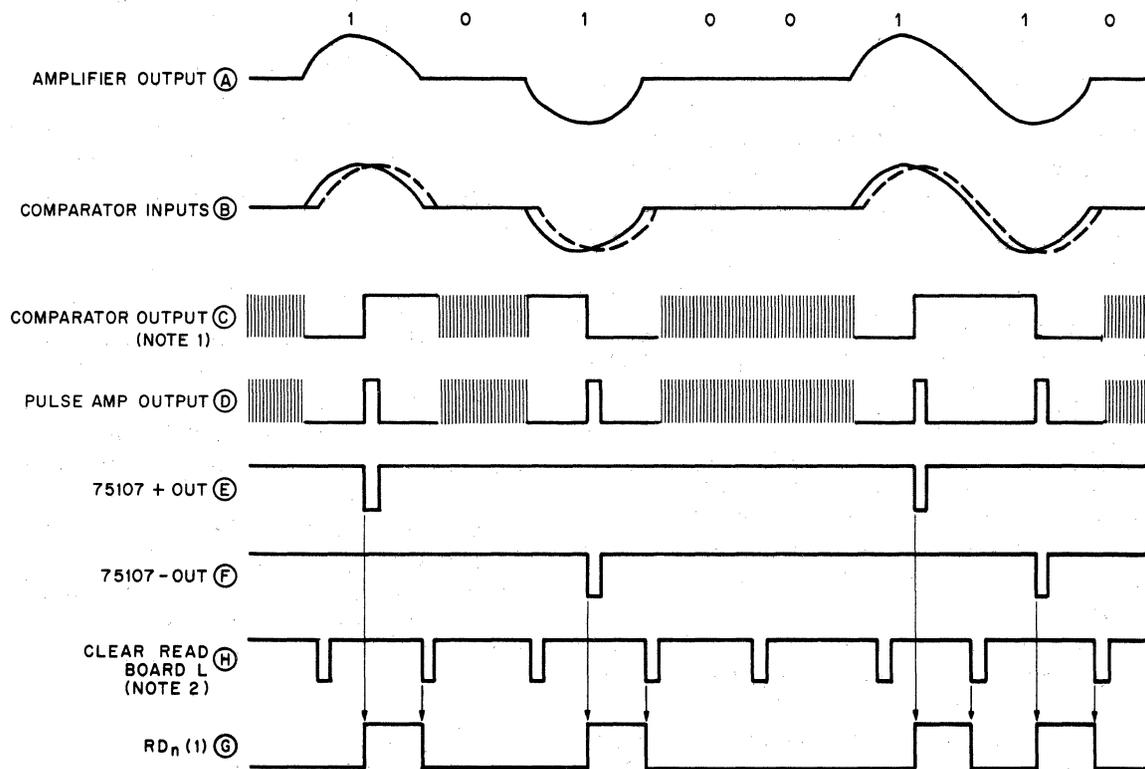
NOTES:
1. Oscillations occur at this output
   when input is at zero.
2. Generated on M8911

Figure 3.7-2 Read Amplifier Waveforms (NRZ)

10-1306

	PES L B	WRE H A	Y_3	Y_2	Y_1	Y_0
PE·$\overline{\text{WRE}}$	0	0	1	1	1	0
PE·WRE	0	1	1	1	0	1
NRZ·$\overline{\text{WRE}}$	1	0	1	0	1	1
NRZ·WRE	1	1	0	1	1	1
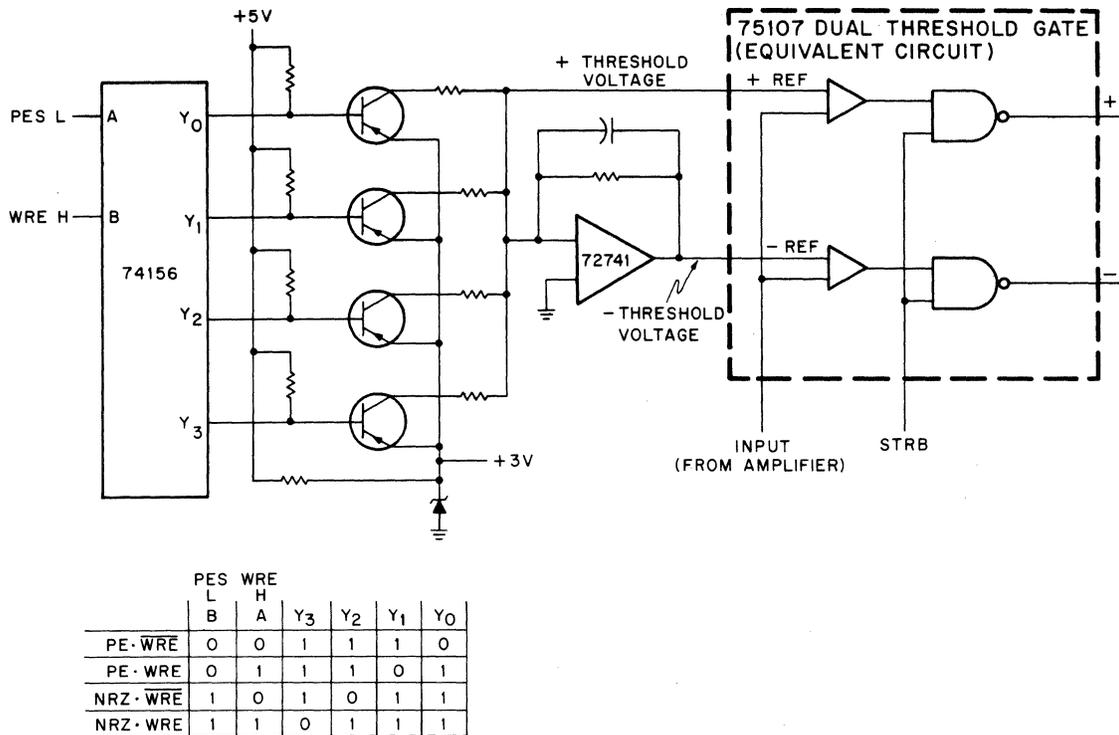
10-1288

Figure 3.7-3 Programmable Threshold

The read deskew timing sequence during a read data operation differs from that of an Interchange Read (IRD) or a write operation. During a read data operation, the Skew Delay Counter (two 74197s) loaded with a preset that depends on the tape data density is up-clocked at 1.15 MHz when the Skew flip-flop is set. When the counter reaches a count of 100 , SDO H is asserted; this occurs approximately 50 percent into the data cell.

With SDO H asserted, the Skew flip-flop is reset on the next negative-going clock edge. This causes the counter to be reloaded; SDO H is thereby negated. The deskew timing sequence will reoccur each time a tape character is read.

During a write or IRD operation, the counter presets are greater, and therefore SDO H is generated 35 percent sooner. When SDO H is generated, the counter is reloaded and upcounted until NTZO H (Non-Trespass Zone Over) is asserted. At this time, the Skew flip-flop is reset and the deskew timing sequence is over. If the Read Amplifiers detect a data transition (PACKET L asserted) while SDO H is asserted, SET VPE L is generated and transmitted to the TM02, where it sets the INC/VPE bit of the Error register.

The outputs of the G056 Read Amplifier are routed to the slave bus via a type 8266 multiplex on the Slave Clock and Motion Delay module (SC 2) and drivers on the Data Driver module (M8913) (refer to Figure 2-6). The read data signals are transmitted to the TCCM module in the TM02 where they are multiplexed to the Tape Control-NRZI module (M8904).

3.7.2 Tape Control-NRZI

When RSDO H is received in the TM02, it is used to generate (CNRZ 4) a 390-ns ERDS H pulse (Enable Read Strobe) and RDS L (Read Strobe). ERDS L loads the NRZ Read Latch (CNRZ 2) with the tape character data. The Read Latch outputs are then gated CNRZ 3) by PES B L (Phase Encoded Status Buffered) negated to the Maintenance Register module. The data inputs (RD B) to the Maintenance Register module are multi-

3.7-3

plexed to the Bit FIddler. ERDS L also clocks the Read LRCC register (CNRZ 3). Thus, a Longitudinal Parity Check Character and a Cycle Redundancy Check Character are developed as data is read. This is discussed in more detail in Sections 3.7.3 and 3.7.4.

3.7.3 CRCC Generation and Read

The Read CRCC Generator (CNRZ 3) is clocked at the start of an operation by DRV SET PLS H. The register is then clocked by ERDS H each time a tape character is read, and the Read CRCC is thus developed. Just before the CRCC is read from tape, the register should already contain the CRCC. It should therefore be cleared when the CRCC is read from tape; if not, a CRCC error has occurred. This is detected by E48 and E45 (CNRZ 3) and CRCE ENBL L is asserted. If the read is in the forward direction, COR/CRC L is asserted (CNRZ 2), and the corresponding bit is set in the Error register.

During a reverse read, when the second RDS H pulse is produced, REV CRCS L is asserted. During a forward read, FWD CRCS L is asserted when Binary Counter E16 (CNRZ 4) reaches a count of three; this occurs three character cells after the last data character has been read (i.e., when the CRCC is read).

REV CRCS L or FWD CRCS L generate CHK CHAR L. The negative-going edge of this signal clocks the Check Character register (R07) with the CRCC just read from tape.

3.7.4 LRCC Generation and Read

The read LRCC register (CNRZ 3) is cleared at the start of an operation by DRV SET PLS H. The register is then clocked by ERDS L each time a tape character is read. Each time a one-bit is read on a track, the corresponding bit in the register is toggled. Therefore, just before the LRC tape character is read, the register should contain the LRCC. When the LRC tape character is read, the register should contain all 0s; if it does not, an LRCC error has occurred. This is detected by E43, E49, E45, and E13, and LRCE ENBL H is generated. Note that during a reverse read (FWD L negated), LRCC error is inhibited. This is because the LRCC is ignored during a reverse read. LRCE ENBL H causes the PEF/LRC flip-flop (CNRZ 2) to be set, thereby setting the corresponding bit in the Error register.

Because the LRCC is the last character read in a record, it is preserved in the Data Field of the Maintenance register (R03). It can therefore be checked by performing a register read of R03.

3.7.5 IRG Detection

As data is read off the tape and RSDO is transmitted from the TU16 to the TM02, RST SHDWN CNTR L (CNRZ 4) constantly keeps resetting the Shutdown Counter (TCCM 5). If RSDO pulses terminate, the Shutdown Counter is enabled for counting by 200 BPI CLK H. [During a write operation, the Gap Detection Timer (TCCM 5) must first time-out before the Shutdown Counter is enabled.] When the Shutdown Counter reaches a count of 15, EORS H and RECORD H are asserted. EORS H causes a Stop tape motion delay to be generated. RECORD H signifies that IRG has been detected.

If data is again detected after a count of SHDN=8, and before the stop motion delay, a Nonstandard Gap error (NSG) is generated, and the corresponding bit in the Error register is set.

3.7.6 Tape Mark Detection

A set of two isolated characters, separated from each other by six to eight character lengths of erased tape is recognized as an NRZ (nine-channel) tape mark by the TU16/TM02.

Refer to the NRZ tape mark detection logic located on CNRZ 4. The Short Record flip-flops E17 were initially cleared by READING H negated, during the start motion delay. As the read heads pass over the IRG, no RSDO H pulse sets the Tape Mark Window flip-flop, because NO CHAR RD L is asserted. The same RSDO pulse also sets the Short Record 1 flip-flop, which negates NO CHAR RD L and enables the Binary Counter (E19) to be upcounted by WRT CLK.

If the next RSDO H pulse occurs while the Binary Counter is at a count of 12 through 15, TPMK WINDOW (1) L will remain asserted. At the same time, SHORT REC I (1) H will be negated, and SHORT REC II (0) L will be asserted.

These three conditions activate E13 (pins 1, 2, and 13), and generate ENBL SHDN CNTR L. If no other characters are soon detected, the Shutdown Counter will assert SHDN=8 H, which will cause the NRZ TMRK flip-flop to direct set.

In nine-track tape units, the Binary Counter is preset to 6. Therefore, the tape mark is valid if the second character arrives six to nine character lengths after the first.

3.7.7 Performance Checks

Use the TM02/TU16 Data Reliability Program diagnostic (see Paragraph 3.1.2) for a performance check on the Read (NRZ) circuitry.

3.7.8 Adjustments

The following adjustments directly affect proper operation of the TU16/TM02 read circuitry:

> Read Amplitude Adjustment (Paragraph 4.18.5)
> Read Skew Adjustment (Paragraphs 5.4.13 and 5.4.14)

3.7.9 Troubleshooting

3.7.9.1 TM02/TU16 Data Reliability Program Diagnostic — Run the TM02/TU16 Data Reliability

Program diagnostic using Pattern 1, 800 BPI and 20 characters. Use Table 3.7-1 to analyze the results of the Data Reliability diagnostic.

NOTE
If an OPI error occurs with a VPE errors, troubleshoot the OPI error first. (See Paragraph 3.5.10-.3.) This type of problem is usually caused by too few RSDO pulses.

If the trouble is not found, change the pattern to 3 (rippling 1s) and rerun the diagnostic. Use Table 3.7-2 to analyze the results of the Data Reliability diagnostic.

Table 3.7-1
Trouble Analysis of Data Reliability Diagnostic Using Pattern 1

Problem	Symptom			Remedy
CRC and LRC Errors				Check gain adjustment of G056.
	Look for a dead channel by letting the program run until some error printouts are obtained.			Check the WD line of the dead channel with an oscilloscope triggered from the REC line. The waveform of figure 3.7-4 should be obtained.
	If the error printout resembles CRC 377-777 LRC 377-777 the parity channel is dead. If the error printout resembles BN: 20 G 377 B 357 a dead channel exists. [1]	Analog signal for dead channel 2 is missing or distorted. Check analog signals (Fig. 3.5-7A) on pins A04L1, B04B1, B04M1, C04K1, C04L1, D04P1, D04R1, F04P1 and F04R1. Mount a skew tape and check the read channel (Fig. 3.5-7B) on pins A04B1, A04F1, B04F1, B04K1, C04P1, Co4R1, D04V1, E04E1 and F04K1.	Read channel is bad.	Check G056. Check read head cable. Check read head.
			Read channel is good.	Repair or replace M8910. Check for faulty back panel wiring. Check write head cable. Check write head. Check RD line. Check M8911 and cables. Check G056 and cables. Check M8913 and cables.
CRC, LRC and VPE Errors without data errors.				Check for "clean" analog signals (Fig. 3.7-5A). Check that the data pulses are approximately 9 volts peak-to-peak. Check that the CRC and LRC pulses are less than 5 volts above and below ground. Check pin E04K1 for the packet waveform shown in Figure 3.7-5C, D. Insure that each pulse is less than $2\,\mu sec$ wide and that pulses occur every $28\,\mu sec$. Check that logic "highs" are greater than $+2.4$ Vdc and all logic "lows" are less than $+0.8$ Vdc.
NEF (Non-Executable Function) Error.				Check that WRL (Write Lock) at pin F01K2 is at $+3$ Vdc. [3]
	The PESB (Phase Encoded Status Signal) signal is incorrect. The signal should be $+3$ Vdc for density 0, 1, 2, and 3; and 0 volts for density 4, 5, 6, and 7.			Check that DEN lines are in correct state. Check that 7 CH is not floating.
NSG (Non Standard Gap) Error.	Excessive number of RSDO pulses are being generated.			Check read circuitry.
FMT (Format) Error.	Format code in TM02 Control Register (bits 4, 5, 6, and 7 of location 172432) is not 14.			Stop and restart the program and retype the format code.
ITM (Illegal Tape Mark) Error.	When the program starts check the response to TM = 0.	Typed response is 0 or RETURN.		Check for system fault.
		Typed response is 1.		Check for bad tape.
		Typed response is 1 and ITM is printed more than once.		Check data channels 0, 1, and 4.
FCE (Frame Count) Error.	Error occurs at end of read operation.			Check for 18 RSDO pulses.
	Error occurs at end of write operation.			Trouble is in TM02 or RH11.
DTE (Drive Timing Error) DBPE (Data Bus Parity Error) CBPE (Control Bus Parity Error) RMR (Register Modification Refuse) ILR (Illegal Register) ILF (Illegal Function)				Trouble is in TM02, controller or processor.

[1] To determine which channel is dead, convert the G and B numbers, which are in octal, to binary.

			Channel 4	Channel 0
G	=	377	=	011 111 111
B	=	357	=	011 101 111

Channel 0 is the least significant (right-most) bit. In the above example, Channel 4 is dead.

[3] If WRL is at ground, a write lock condition will exist and it will be impossible to execute a write command. Refer to the M8910 circuit schematic.

2 Convert the data channel number to the physical track number as follows:

Data Channel Number	=	Physical Track Number
P		4
7		7
6		6
5		5
4		3
3		9
2		1
1		8
0		2

Figure 3.7-4   REC and WD Signal Waveforms
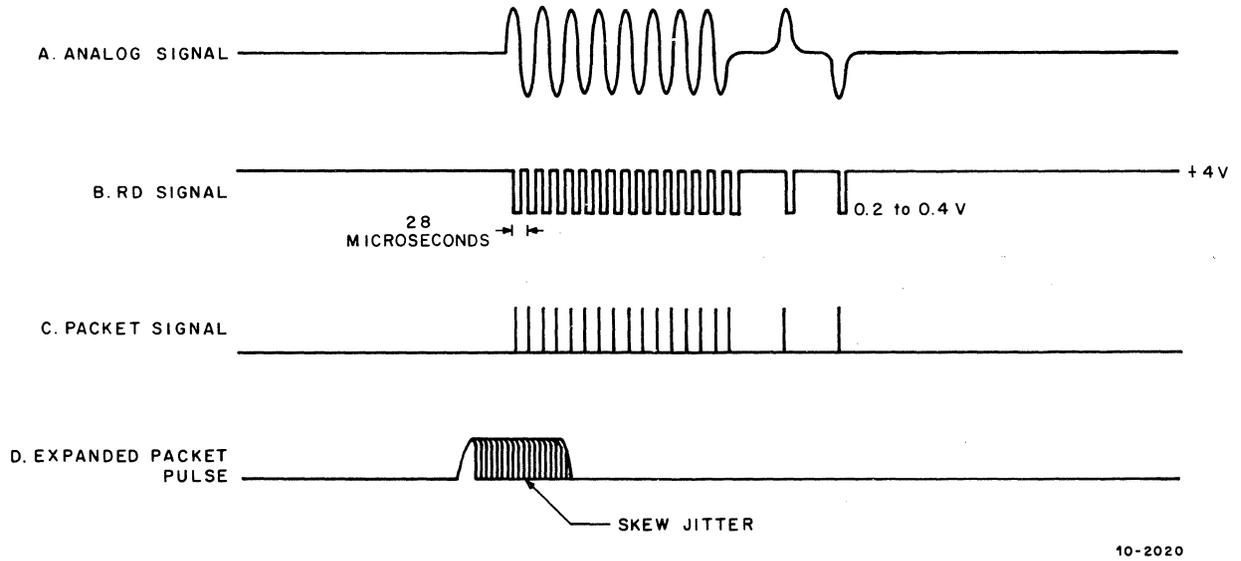
Figure 3.7-5   Read Signals

Table 3.7-2
Trouble Analysis of Data Reliability Diagnostic Using Pattern 3

Problem		Remedy

Grounded RD or WD line	Check printout as follows to locate bad channel.
	
	    BN: 1 Channel 0
	      G 0 0 0 0 0 0 1 0
	      B 0 0 0 0 0 0 1 1
	
	    BN: 2
	      G 0 0 0 0 0 1 0 0
	      B 0 0 0 0 0 1 0 1
	
	    BN: 3
	      G 0 0 0 0 1 0 0 0
	      B 0 0 0 0 1 0 0 1
	
	Note that for each B (bad data) printout, Channel 0 is a one (1). This indicates that either RD0 or WD0 is shorted to ground.
		Check RD and WD of faulty channel for short to ground.

Data lines tied together	Check printout as follows to locate connected data lines.
	
	    BN: 1 Channel 6 Channel 1
	      G 0 0 0 0 0 0 1 0
	      B 0 1 0 0 0 0 1 0
	
	    BN: 6
	      G 0 1 0 0 0 0 0 0
	      B 0 1 0 0 0 0 1 0
	
	    BN: 17
	      G 0 0 0 0 0 0 1 0
	      B 0 1 0 0 0 0 1 0
	
	Note that for each B (bad data) printout, Channels 1 and 6 are always the same. This indicates that WD1 and WD6 are tied to each other.
		Check on slave bus (cable A) for connection between two data lines indicated by printout.

Intermittent errors on data channel 0.	Error printout indicates that data channel 0 is intermittent.	Check that both ends of cables A and B are correctly installed. Using an oscilloscope, check for the wave shapes of Figure 3.7-6.

A. WRITE SIGNAL WAVEFORMS USING NEGATIVE EDGE
OF REC(SB) L FOR SCOPE TRIGGER
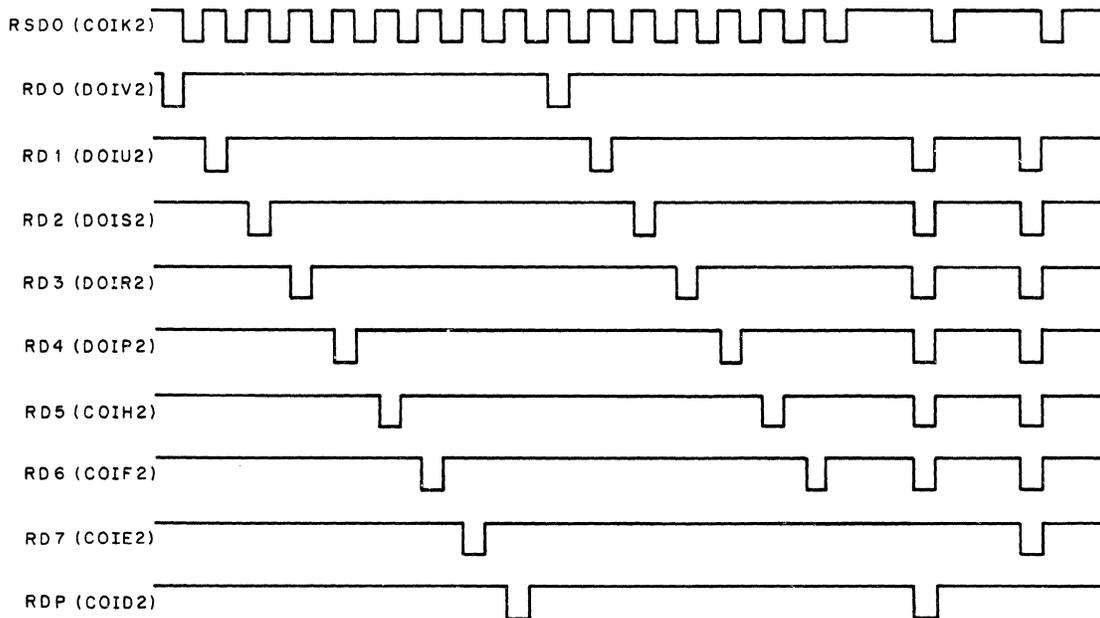
B. READ SIGNAL WAVEFORMS USING NEGATIVE EDGE
OF RSDO FOR SCOPE TRIGGER

NOTES:
1. When checking these waveforms, put PDP-11 keys 2,3,
   10,11,12, and 13 up. Keys 2 and 3 cause a foward write.
   Keys 10 through 13 inhibit error checking and printout.

2. Record count =1; character count = 20_8; switches 2 and 3 up.

3. Set oscilloscope for 0.1 ms/cm.

10-2021

Figure 3.7-6   NRZI Signal Waveforms Using Pattern 3 and 800 BPI

BIT FIDDLER READ (M8906)

3.8 INTRODUCTION

This pamphlet discusses the operation of the M8906 Bit Fiddler during a read data operation (reference Figure 2-6). The M8906 Bit Fiddler is used in PDP-11 systems. PDP-10 systems utilize an M8914 Bit Fiddler, which is described in other pamphlets (3.9 and 3.11).

3.8.1 M8906 Bit Fiddler Operating Modes

When OCC is asserted on the Massbus, the Bit Fiddler is enabled (BF ENABLE H asserted, MBI 9). [Reference the M8906 schematics and the M8906 Bit Fiddler Read Operation flowchart (Figure 3.8-D).] When DRIVE SET Pulse is generated, tape motion is started and the Bit Fddler is initialized by P BF RUN H (generated by the signal AEMD, BF 2). The initial state of the Bit Fiddler during a read operation is determined by the tape data format and the direction of tape motion. These parameters determine the initial states of the Select A and Select B flip-flops. The format also determines the manner in which these flip-flops will be toggles (see Table 3.8-1).

The Format Select bits (FMT 0—3) of the Tape Control register are decoded in the Bit Fddler (BF 3) as follows:

FMT (0—3)				Mode
3	**2**	**1**	**0**	
1	1	0	0	Normal Mode
1	1	0	1	Core Dump
1	1	1	0	15 Mode

Any other combination produces a Bit Fiddler Format Error (BFFMTE).

3.8.2 M8906 Bit Fiddler Read Operation

When a tape data character becomes available on the Read Data C lines (RDC 0—7, BF 5), the Bit Fiddler receives RDS (BF 2). This causes one or two of the Read Latches (E1, E2, E5, and E6 on BF 5) to be

Table 3.8-1
Bit Fiddler Initialization/Operation

	Format Mode	Select A		Select B	
		Initial	Toggled By	Initial	Toggled By
Forward	Normal Mode	Clear	Toggling inhibited	Clear	RDS
Tape	Core Dump	Clear	RDS	Clear	Alternate RDS
Motion	15 Mode	Clear	Toggling inhibited	Set	RDS
Reverse	Normal Mode	Clear	Toggling inhibited	Set	RDS
Tape	Core Dump	Clear	RDS	Set	Alternate RDS
Motion	15 Mode	Clear	Toggling inhibited	Clear	RDS

*Only normal mode and 15 mode provide proper reassembly in read reverse.

ASSERT OCC | **BIT FIDDLER ENABLED**

RECEIVE RUN H

DRIVE SET PULSE

GENERATE P BF RUN PULSE

NORMAL MODE ?

FORWARD ? — NO

CORE DUMP ? — NO

15 MODE NO

FORWARD ? — NO

YES

FORWARD ? — YES / NO

INITIALIZE SELECT A → 0 SELECT B → 1

INITIALIZE SELECT A → 0 SELECT B → 0

INITIALIZE SELECT A → 0 SELECT B → 1

INITIALIZE SELECT A → 0 SELECT B → 0

(1)

(2)

---

(1)

MUX CHARACTER	RECEIVE DATA CHARACTER
LOAD READ BUFFER	RECEIVE R D S
CLOCK FRAME-COUNT REGISTER	TOGGLE SELECT B
MUX CHARACTER	RECEIVE DATA CHARACTER
LOAD READ BUFFER	RECEIVE R D S
CLOCK FRAME-COUNT REGISTER	TOGGLE SELECT B
	GENERATE S CLK

(2)

---

(2)

MUX CHARACTER	RECEIVE DATA CHARACTER
LOAD READ BUFFER	RECEIVE R D S
CLOCK FRAME-COUNT REGISTER	TOGGLE SELECT A
MUX CHARACTER	RECEIVE DATA CHARACTER
LOAD READ BUFFER	RECEIVE R D S
CLOCK FRAME-COUNT REGISTER	TOGGLE SELECT A & SELECT B
MUX CHARACTER	RECEIVE DATA CHARACTER

(3)

---

(3)

LOAD READ BUFFER	RECEIVE R D S
CLOCK FRAME-COUNT REGISTER	TOGGLE SELECT A
MUX CHARACTER	RECEIVE DATA CHARACTER
LOAD READ BUFFER	RECEIVE R D S
CLOCK FRAME-COUNT REGISTER	TOGGLE SELECT A & SELECT B
	GENERATE S CLK

10-1331

Figure 3.8-1   M8906 Bit Fiddler Read Operation Flowchart

3.8-2

loaded by CLK Ⓐ and/or CLK Ⓑ , or by CLK Ⓒ and/or CLK Ⓓ , depending on the states of SELECT A, SELECT B, and CORE DUMP. The states of SELECT B and/or SELECT A are now altered, and, when the next tape data character becomes available and RDS is received, one or two other Read Latches are loaded. The Bit Fiddler thus assembles 18-bit data words (bits 16 and 17 forced set) for transfer to the Massbus Controller. Table 3.8-2 shows CLK Ⓐ Ⓑ Ⓒ Ⓓ sequences for the different formats and tape motion directions.

After each CLK Ⓐ Ⓑ Ⓒ Ⓓ cycle, an 18-bit data word, ready for transmission to the Massbus Controller, is sitting on the Data lines. The Bit Fiddler

(BF3) generates a parity bit DPA TM which will be transmitted with the data word.

When the data word is assembled, the Massbus Transfer (MB XFR, BF 2) flip-flop is clocked set. This produces a 1-μs pulse SCLK, which is transmitted to the Massbus Controller and causes it to strobe in the word on the Data lines. SCLK also resets the MB XFR flip-flop. Consecutive tape data characters are assembled in the same manner, and each time a data word is ready, SCLK is generated to the Massbus Controller.

Figure 3.8-2 is a timing diagram of Bit Fiddler operation in core dump mode during a read forward operation.
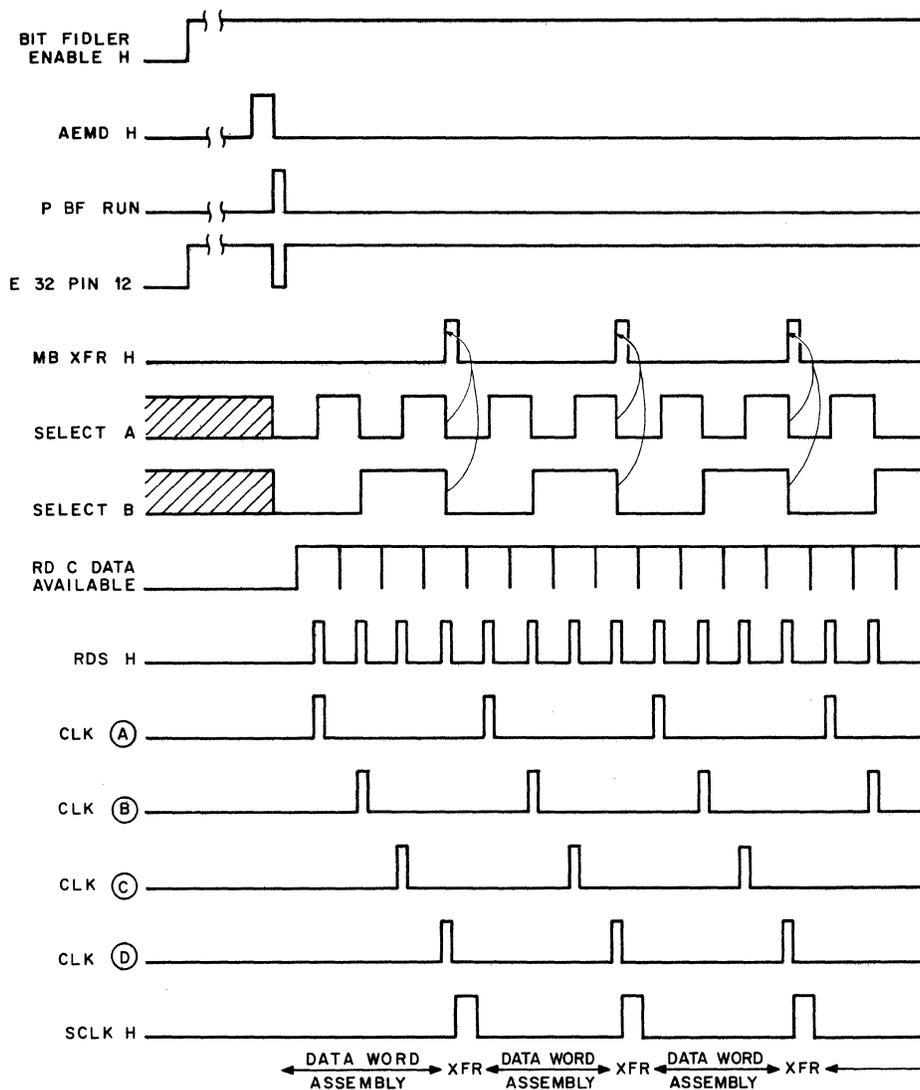
Figure 3.8-2   Bit Fiddler Read Forward Operation in Core Dump Mode

3.8.3 Performance Checks

Perform Wrap-Around tests of the TM02/TU16 Control Logic Test diagnostic (see Paragraph 3.1.2).

3.8.4 Adjustments

None.

3.8.5 Troubleshooting

Symptoms which point directly at Bit Fiddler malfunctions are:

1. Incorrect data without status errors.

2. Data late errors.

3. Data bus parity errors.

4. Format errors.

5. Drive timing errors.

If module swapping the M8906 does not correct the trouble, use Figure 3.8-1 to trace trouble to related circuits.

Table 3.8-2

CLK   (A)   (B)   (C)   (D)   Sequences

Mode	Direction of Tape Motion	Sequence
Normal Mode	Forward	A&B → C&D → A&B → C&D → etc.
	Reverse*	C&D → A&B → C&D → A&B → etc.
Core Dump	Forward	A → B → C → D → A → B → C → D → etc.
	Reverse	C → D → A → B → C → D → A → etc.
15 Mode	Forward	C&D → A&B → C&D → A&B etc.
	Reverse*	A&B → C&D → A&B → C&D etc.

*Only normal mode and 15 mode provide proper reassembly in read reverse.

BIT FIDDLER READ (M8914)

3.9 INTRODUCTION

This pamphlet discusses the operation of the M8914 Bit Fiddler during a read data operation (reference Figure 2-6). The M8914 Bit Fiddler is used in PDP-10 systems. PDP-11 systems utilize an M8906 Bit Fiddler, which is described in other pamphlets (3.8 and 3.10).

3.9.1 Bit Fiddler Initialization

Reference the M8914 Bit Fiddler schematics and the Bit Fiddler Read Operation flowchart (Figure 3.9-1).

When the TM02 decodes a data transfer function code in the Control Register, OCC TM is asserted (MBI 7); this enables the Bit Fiddler (BF ENABLE H). When BF ENABLE H and GO BUF H are asserted the status register is enabled.

When the TM02 receives RUN H, DRV SET PLS is generated in the Massbus Interface module (M8909). DRV SET PLS produces EMD H (TCCM 3), a pulse which, on its trailing edge, triggers a one shot (BFLR8, E10) which sets the status register. When the status register is set it assumes its initialized state of the SR1

H output being high, and the LD SEL H and SR3 H outputs being low. The status register remains in this state until the data output word has been assembled.

3.9.2 Bit Fiddler Formatting

The mode of Bit Fiddler operation during a data read is determined by the selected data format. The Format Select bits (FMT 0—3) of the Tape Control register are decoded in the Bit Fiddler (BF7) as shown in Table 3.9-1.

Figure 3.9-2 illustrates Bit Fiddler multiplexing. The figure shows the read operation in block diagram form. Figure 3.11-3 illustrates the tape frame format for the four modes of operation. In each case the tape frames are inputted into the Bit Fiddler from the drive unit. The tape frames are received in the Bit Fiddler Data Shift Register where they are assembled into the 36-bit PDP-10 core word. The number of tape frames required to assemble a complete word, and whether shifting is required in the data register, depends on the mode of operation.

Table 3.9-1
Bit Fiddler Format

Bits				Mode	Number of Tape Frames per Assembled Word
3	2	1	0		
0	0	0	0	10 Core Dump	5
0	0	0	1	10 Seven Track	6
0	0	1	0	10 ASCII	5
0	0	1	1	10 Compatibility	4

Any other combination produces a Bit Fiddler Format Error (BFFMTE).
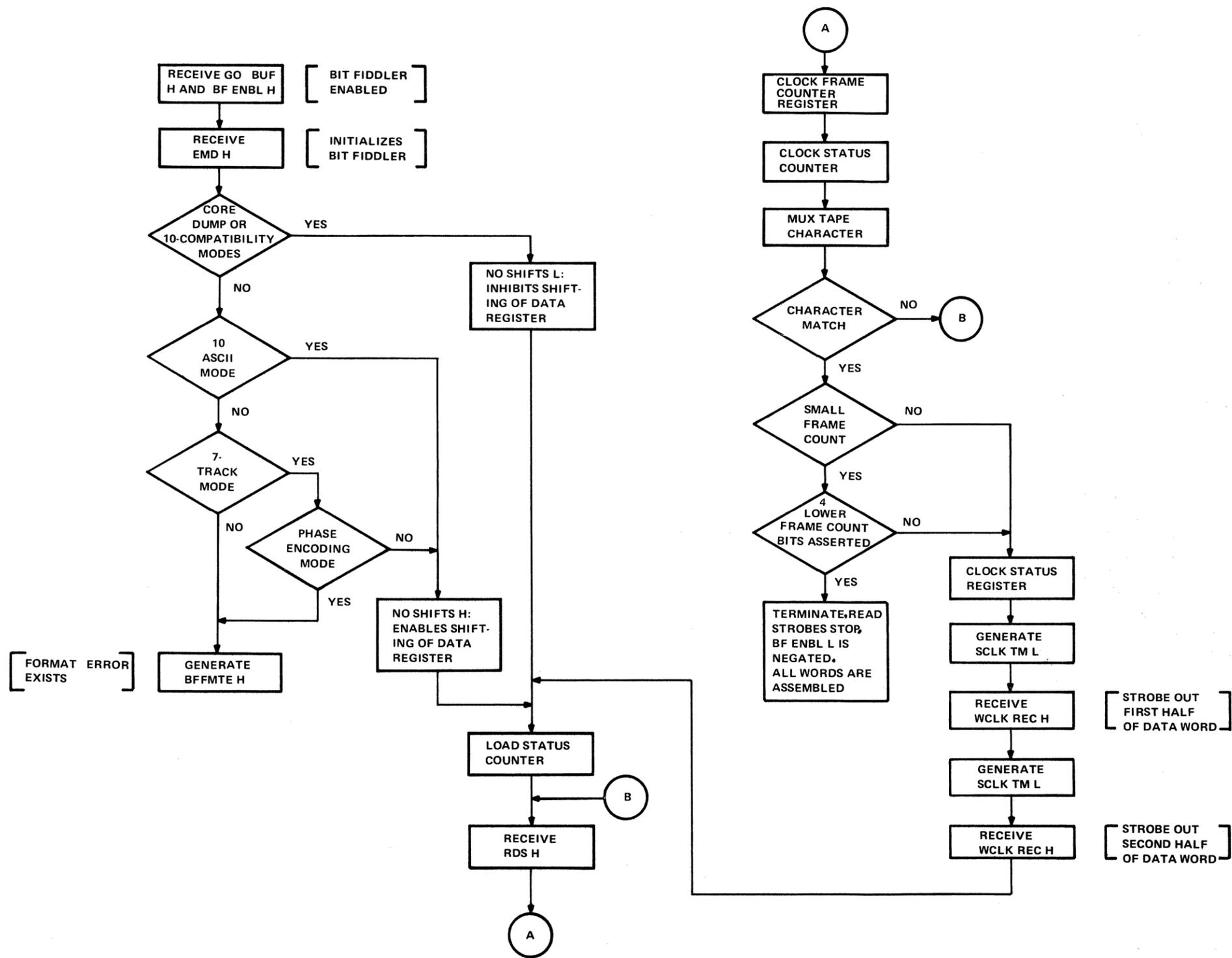
Figure 3.9-1   Bit Fiddler Read Operation Flowchart

10-2022

```
                          FROM TAPE
                           DRIVE
                             │ │ 8 DATA LINES
                             │ │ (READ OPERATION)
                             ▼
         18 DATA LINES    ┌───────┐              ┌──────────┐              ┌────────┐   18 DATA LINES
  FROM   ⎰(WRITE OPERATION)│ INPUT │ DATA LINES  │  48-BIT  │ DATA LINES  │ OUTPUT │   (READ OPERATION)   TO
MASSBUS ⎱                 │  MUX  │─────────────▶│   DATA   │────────────▶│  MUX   │─────────────────────▶ MASSBUS
         ─────────────────│       │              │ REGISTER │           │ │        │
                          └───────┘              └──────────┘           │ └────────┘
                                                                        │
                                                                        ▼
                                                                  ┌──────────┐
                                                                  │   TAPE   │
                                                                  │  FRAME   │
                                                                  │   MUX    │
                                                                  └──────────┘
                                                                        │
                                                                        │ 8 DATA LINES
                                                                        │ (WRITE OPERATION)
                                                                        ▼
                                                                    TO TAPE
                                                                     DRIVE
```
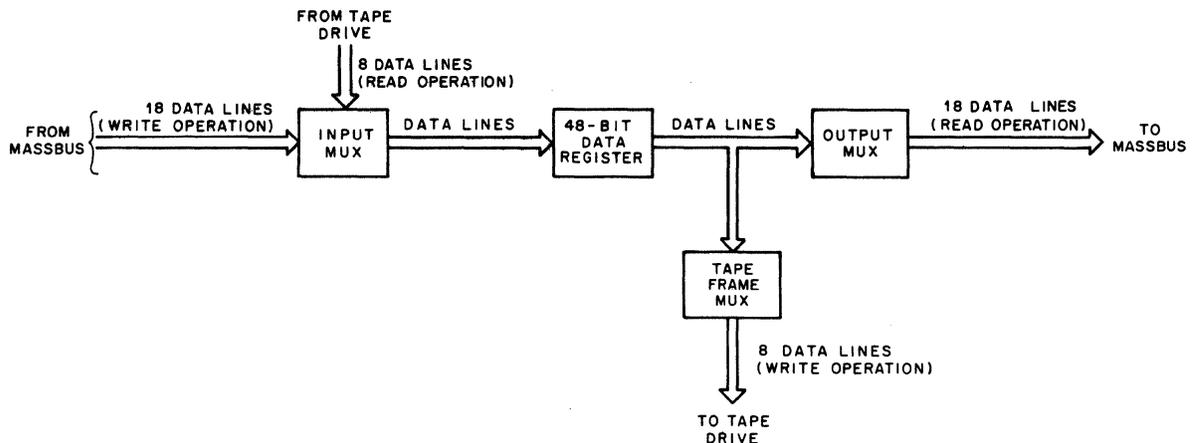
Figure 3.9-2 Bit Fiddler Multiplexing Block Diagram   10-2023

3.9.3 Bit Fiddler Read Operation

When a tape character becomes available on the Read Data C lines (RDO 0—7), the Bit Fiddler receives RDS H. RDS H clocks the status counter and the Frame Count Register on the Massbus Interface Module M8909. The status counter was already loaded prior to initialization and is counted up during the Read process. The output of the status counter addresses a PROM (E61) which clocks the data shift register causing the first character to be loaded. (See Figure 3.9-3).

When the next RDS pulse is received the status counter and frame count register are again clocked and the Prom outputs load each section of the data register except for the lower order 8 bits. The next RDS pulse again causes loading of the data register except for the lower order 16 bits, etc. until the data register is loaded with the correct number of tape frames (data characters). When the outputs of the status counter match a decoding of the format bits (FMT 0—3) a CHAR MTCH H signal is asserted indicating that the correct number of tape data characters have been loaded into the data register. CHAR MTCH H clocks the status register which asserts SHIFT LEFT H to the data register for assembling of the data word. When the word has been assembled according to the format, CLK SR H is asserted and clocks the status register which generates two SCLK pulses to the Massbus controller.

When the Controller receives the first SCLK it generates WCLK which strobes out the first half of the data word. When the Controller receives the second SCLK it sends another WCLK pulse to the Bit Fiddler causing the second half of the data word to be strobed out onto the data lines. The Bit FIddler then generates a parity bit for each data word placed onto the Massbus.

The status register now returns to its initial state until all of the tape data characters for the next word have been assembled and strobed onto the data lines.

Each SCLK generated by the Bit Fiddler preloads the status counter in preparation for a frame count of the next half of a data word.

When the frame count register overflows the BF ENBL H signal is negated and the Read operation is completed.

Figure 3.9-3 is a timing diagram of Bit Fiddler operation in the "10 core dump" mode during a Read operation.

3.9.4 Performance Checks

Perform Wrap-Around tests of PDP-10 Diagnostic MAINDEC-10-DLTUA to check performance of data paths, DPAR circuits and format error circuits (see Paragraph 3.1.2).

3.9.5 Adjustments

None.

3.9.6 Troubleshooting

Symptoms which point directly at Bit Fiddler malfunctions are:

1. Data late errors.

2. Data bus parity errors.

3. Format errors.

4. Drive timing errors.

If module swapping the M8914 does not correct the trouble, use Figure 3.9-1 to trace trouble to related circuits.
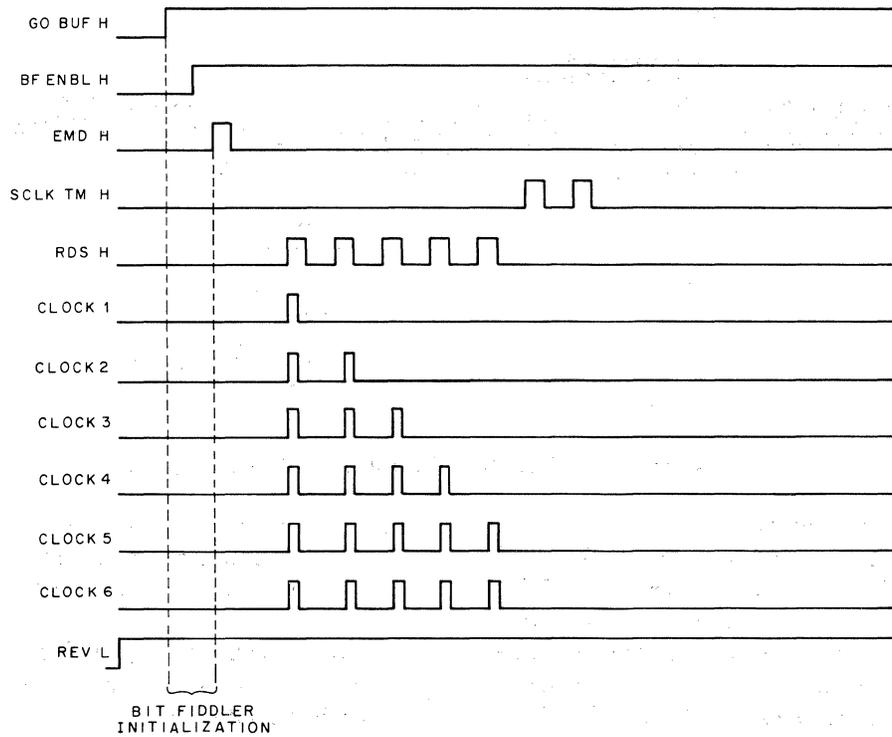
NOTE:
Clocks 1 through 6 are generated from prom outputs
(E67 pins 1,2,3,4,5,6).

10-2024

Figure 3.9-3   Timing Diagram of Bit Fiddler Read Forward Operation in Core Dump Mode

BIT FIDDLER WRITE (M8906

3.10 INTRODUCTION

This pamphlet discusses the operation of the M8906 Bit Fiddler during a write data operation (reference Figure 2-4). The M8906 Bit Fiddler is used in PDP-11 systems. PDP-10 systems utilize an M8914 Bit Fiddler, which is described in other pamphlets (3.9 and 3.11).

3.10.1 Bit Fiddler Initialization

Reference the M8906 Bit Fiddler schematics and the Bit Fiddler Write Operation flowchart (Figure 3.10-1).

When the TM02 decodes a data transfer function code in the Control register, OCC TM is asserted (MBI 7); this enables the Bit Fiddler (BF ENABLE H, MBI 9). When the Massbus Controller is ready to transmit data, it places an 18-bit data word on the Data lines of the data bus, places a parity bit associated with the Data lines on the DPA line, and then asserts RUN H.

When the TM02 receives RUN H, DRV SET PLS is generated in the Massbus Interface module (M8909). DRV SET PLS produces AEMD H (TCCM 3), a pulse which, on its trailing edge, triggers a one-shot (BF2, E29) and generates P BF RUN H. P BF RUN H initializes the Bit Fiddler by setting or clearing the Select A and Select B flip-flops. Because WRITE L is asserted during a write data operation, P BF RUN H is gated by E25 and also sets the MB XFR (Massbus Transfer) flip-flop. MB XFR H produces a 1- s SCLK pulse, which resets the MB XFR flip-flop and is transmitted to the Massbus Controller.

When the Massbus Controller receives SCLK, it transmits WCLK to the TM02 and then places the next data word and its corresponding parity bit on the data bus. WCLK, enabled by BF ENABLE, produces CLK WRT BUF H, which loads the Bit Fiddler Write Buffer

(BF 4). Thus, in a data write operation, the first dat word is transferred soon after, and as a consequence o the assertion of RUN H. Subsequent data words ar transferred only after the first data word has been cor verted to tape characters, i.e., after the motion delay over (and in PE Mode, after the preamble is written).

3.10.2 Bit Fiddler Formatting

The mode of Bit Fiddler operation during a data writ is determined by the selected data format. The Forma Select bits (FMT 0—3) of the Tape Control register ar decoded in the Bit Fiddler (BF 3) as follows:

	FMT (0—3)				
Bit	**3**	**2**	**1**	**0**	**Mode**
	1	1	0	0	Normal Mode
	1	1	0	1	Core Dump
	1	1	1	0	15 Mode

Any other combination produces a Bit Fiddler Forma Error (BFFMTE). The selected format determines th initial states of the Select A and Select B flip-flops, an also the manner in which the flip-flops are toggle (refer to Table 3.10-1). SLCT A and SLCT B are input to multiplexers E15, E16, and E19 (BF 4), and deter mine the manner in which a data word stored in th Write Buffer is disassembled. Note that in core dum mode, BFO 4—7 are forced low. As SLCT A and/c SLCT B toggle, the data word is multiplexed int characters as indicated in Figure 3.10-2.

3.10.3 Bit Fiddler Timing

When WRT STRB H pulses are received by the B Fiddler, it begins disassembling the data word store in the Write Buffer. In NRZ mode, this occurs imm diately after the start motion delay, when the TU16 at speed and transmits WRT CLK to the TM02. In P
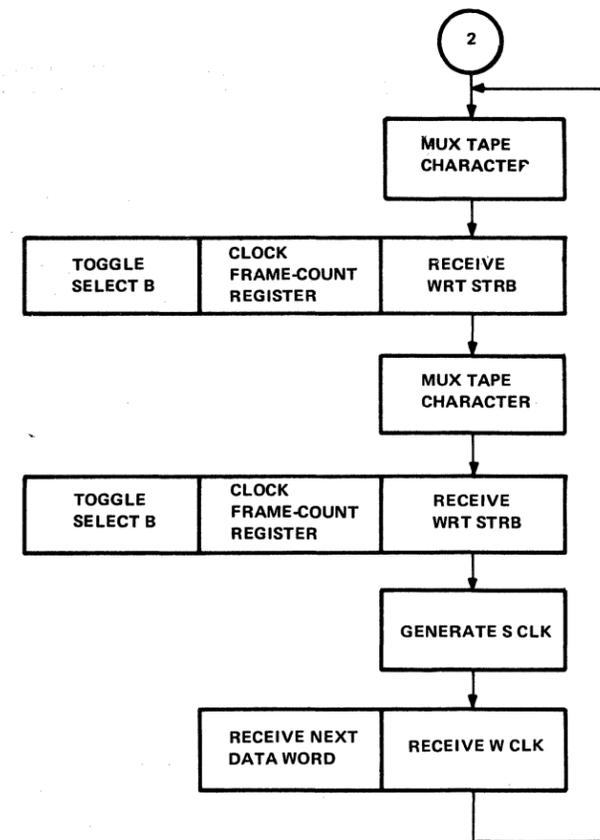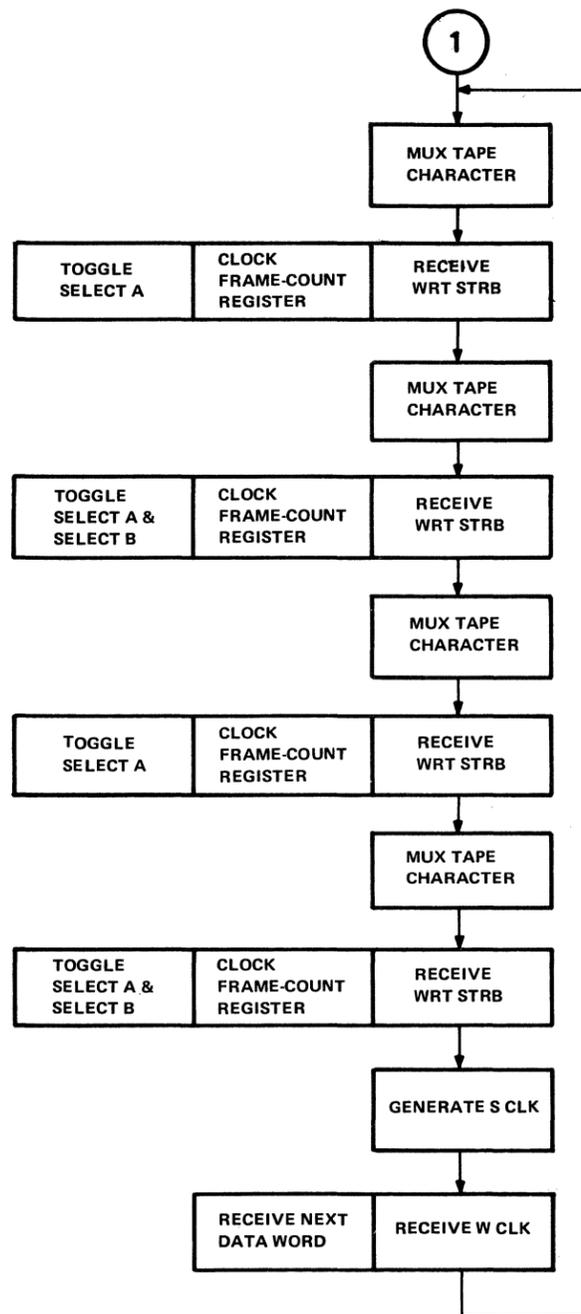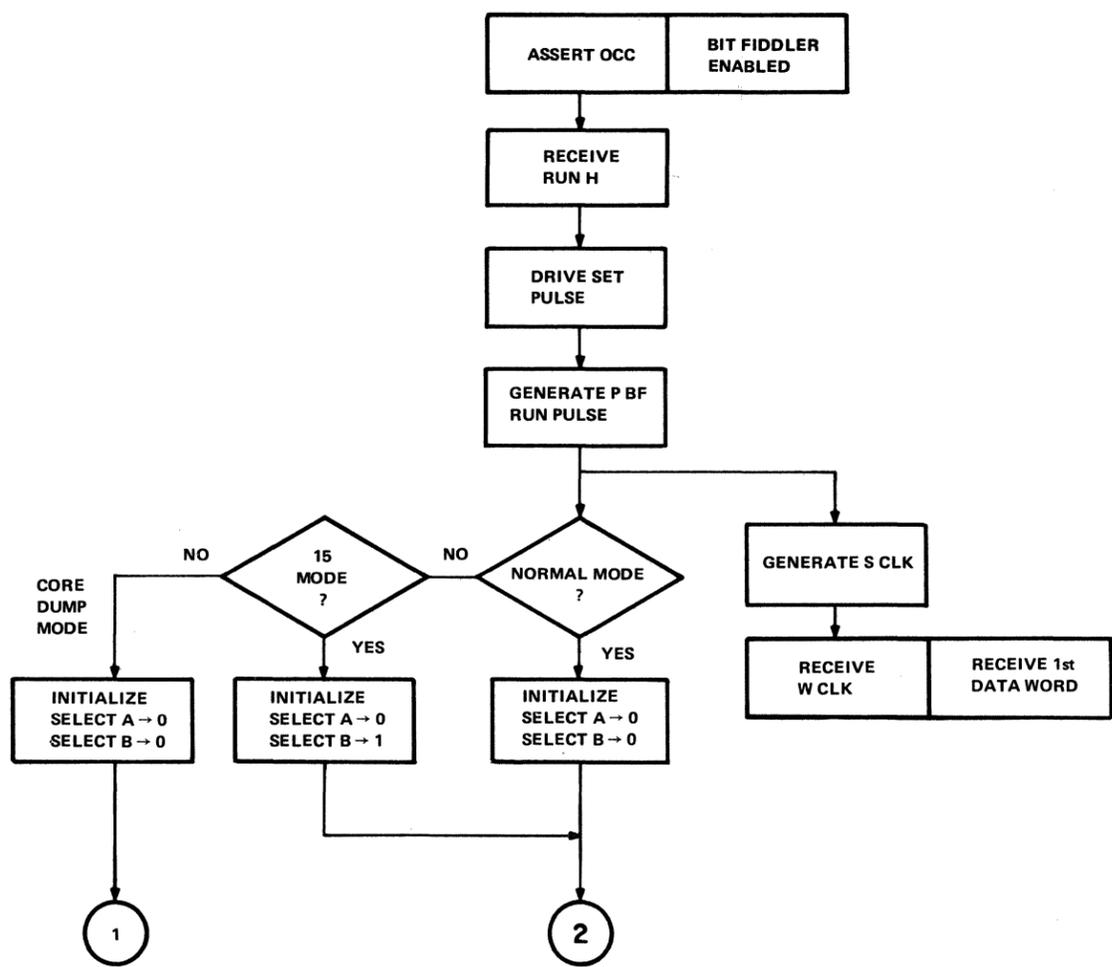
Figure 3.10-1   M8906 Bit Fiddler Write Operation Flowchart

Table 3.10-1
Bit Fiddler Initialization/Operation

Format Mode	Select A		Select B	
	Initial	Toggled By	Initial	Toggled By
Normal Mode	Clear	Toggling inhibited	Clear	WRT STRB
Core Dump	Clear	WRT STRB	Clear	Alternate WRT STRB
15 Mode	Clear	Toggling inhibited	Set	WRT STRB

a. Normal Mode

b. Core Dump Mode

c. 15 Mode
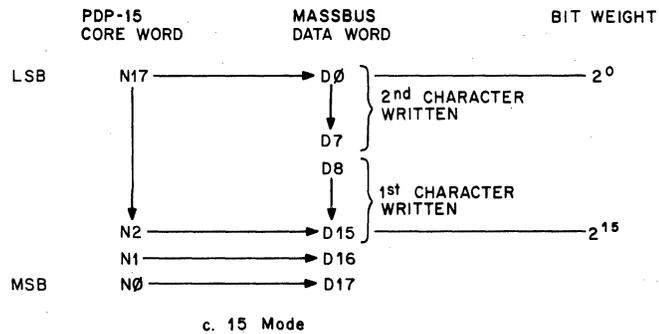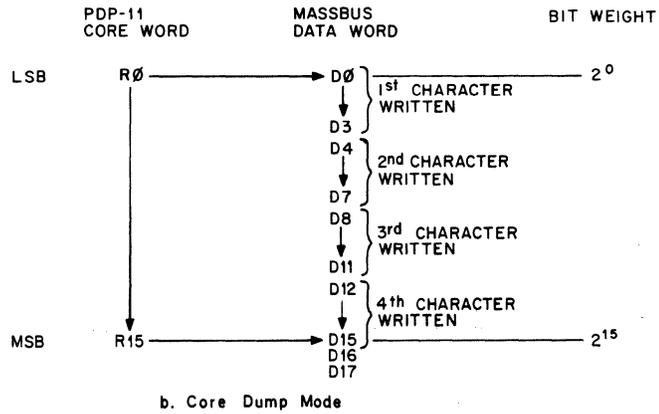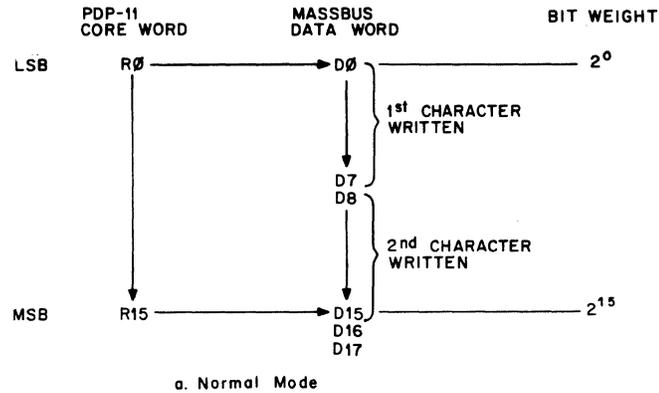
10-1326

Figure 3.10-2   M8906 Bit Fiddler Write Formats

mode, WRT STRB pulses are generated after the preamble has been written.

WRT STRB H is generated on the Tape Control Common Mode module (TCCM 4). When DRV SET PLS H is asserted during a write data operation, the Write Data Record flip-flop (E42) is set, generating WDR H. In NRZ mode, (PESB L negated), this produces a high at E25 pin 6 and E46 pin 8, and enables generation of WRT STRB H when WRT CLK is produced by the TU16. WRT STRB and WRT CLK will be at the same

frequency. In PE mode, WRT STRB H is also derived from WRT CLK; however, PE WRT ENABLE L and DATA CLK H must be asserted. This occurs when the data portion of a record is written. Because the frequency of DATA CLK H is half that of WRT CLK, WRT STRB H will also be at half the frequency of WRT CLK H (Figure 3.10-3).

Figure 3.10-4 is a timing diagram for Bit Fiddler write operation in core dump mode. Each time a WRT STRB H pulse is generated, the Select B and/or Select
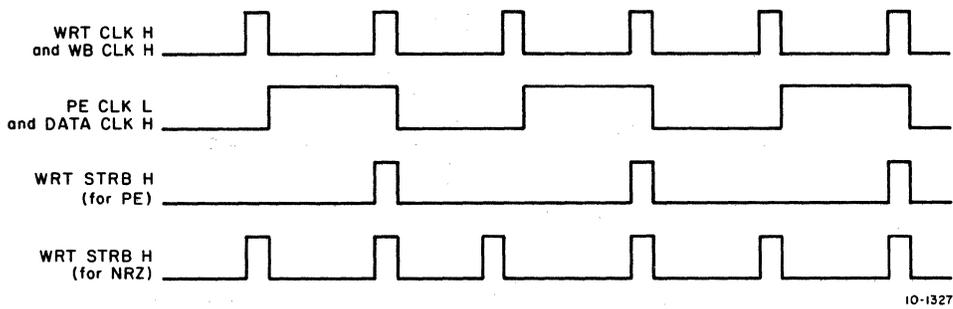
Figure 3.10-3   WRT STRB Timing
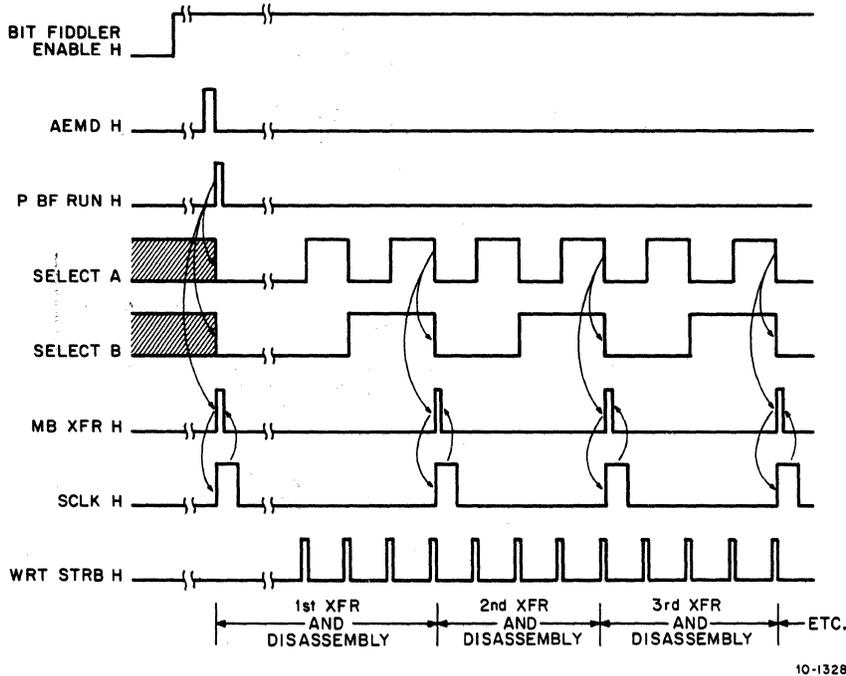
Figure 3.10-4   Bit Fiddler Write Operation in Core Dump Mode

A flip-flops are toggled. The Frame Count register is also incremented (FCCLK H, BF 2) at each WRT STRB H. For each combination of SLCT A and SLCT B, a separate character is multiplexed onto the Bit Fiddler output lines; this character becomes available to the write circuitry in the TCCM module.

In core dump (or normal) mode, completion of data word disassembly is detected by E21 (pins 3, 4, and 5) (in 15 mode, E21 pins 1, 2, and 13 detect this condition), and the MB XFR flip-flop is clocked set. MB XFR H generates a 1- s SCLK pulse, which clears the MB XFR flip-flop, and is transmitted to the Massbus Controller. The controller responds to SCLK with a WCLK pulse which loads the Bit Fiddler Write Buffer with the data word on the Data lines. The controller then places a new data word on the Data lines, places a data parity bit on the DPA lines, and waits for the next SCLK pulse. In the meantime, the Bit Fiddler performs its disassembly process on the new word in its Write Buffer. When this word is disassembled, another SCLK is transmitted to the controller; this cycle continues untill all the data has been transferred.

Each time the Write Buffer is loaded, a data bus parity check is performed. If there is a parity error, the Parity Error flip-flop (BF 3) is set and SET DPAR H is generated. This causes the DPAR bit in the Error register to be set.

If a WRT STRB H pulse occurs before the Bit Fiddler receives a WCLK response from the Massbus Controller, SET DTE L (Set Drive Timing Error) is asserted. This causes the DTE bit in the Error register to be set.

3.10.4 Performance Checks
Perform the TM02/TU16 Control Logic Test diagnostic to check performance of data paths, DPAR circuits and format error circuits (see Paragraph 3.1.2).

3.10.5 Adjustments
None.

3.10.6 Troubleshooting
Symptoms which point directly at Bit Fiddler malfunctions are:

1. Data late errors.

2. Data bus parity errors.

3. Format errors.

4. Drive timing errors.

If module swapping the M8906 does not correct the trouble, use Figure 3.10-1 to trace trouble to related circuits.

BIT FIDDLER WRITE (M8914)

CONTENTS

3.11 INTRODUCTION

This pamphlet discusses the operation of the M8914 Bit Fiddler during a write data operation (reference Figure 2-4). The M8914 Bit Fiddler is used in PDP-10 systems. PDP-11 systems utilize an M8906 Bit Fiddler, which is described in other pamphlets (3.8 and 3.10).

3.11.1 Bit Fiddler Initialization

Reference the M8914 Bit Fiddler schematics and the Bit Fiddler Write Operation flowchart (Figure 3.11-1).

When the TM02 decodes a data transfer function code in the Control register, OCC TM is asserted (MBI 7); and enables the Bit Fiddler (BF ENABLE H). When BF ENABLE H and GO BUF H are asserted, the status register is enabled.

When the Massbus Controller is ready to transmit data, it places an 18-bit data word on the Data lines of the data bus. The 18-bit data word is the first half of a PDP-10 36-bit data word.

When the TM02 receives RUN H, DRV SET PLS is generated in the Massbus Interface module (M8909). DRV SET PLS produces EMD H (TCCM 3), a pulse which, on its trailing edge, triggers a one-shot (BFLR9, E10) which presets status register E67 (BF8). When the status register is set its R2 output is asserted and generates two SCLK TM L pulses via multiplexer E75, exclusive OR E41 and one-shot E2. The RC time delay in the E41 input circuit results in the generation of the second SCLK TM L pulse.

When the Massbus Controller receives the first SCLK, it transmits WCLK to the TM02 and then places the first half of the 36-bit data word onto the data bus. When the Controller receives the second SCLK, it transmits the second WCLK to the TM02 and then places the second half of the data word and its corresponding parity bit on the data bus. The two halfs of the 36-bit data word are loaded into the 48-bit shift register via the input multiplexer (see Figure 3.9-2). Thus, in a data write operation, the first data word is transferred soon after, and as a consequence of, the assertion of RUN H. Subsequent data words are transferred only after the first data word has been converted to tape characters.

3.11.2 Bit Fiddler Formatting

The mode of Bit Fiddler operation during a data write is determined by the selected data format. The Format Select bits (FMT 0—3) of the Tape Control register are decoded in the Bit Fiddler (BF7) as shown in Table 3.11-1.

The mode of operation determines the number of frames required to disassemble one 36-bit word. Refer to Figure 3.11-2 and Table 3.11-2 for the tape frame formats. Figure 3.11-2 illustrates the tape frame format for the four modes of operation. In each case the 36-bit PDP-10 core word is inputted to the Bit Fiddler, via the Massbus, in two 18-bit segments. The two segments are received in the Bit Fiddler data register and then disassembled into tape frames according to the selected mode. Each tape frame corresponds to a character written onto the tape.

Table 3.11-2 illustrates the utilization of the tape tracks in the various modes of operation. Note in the 10 Compability mode all tracks of all tape frames are used, while in the 10 Core Dump mode four tracks of the 5th frame are not used. In 10 seven-track mode tracks 6 and 7 are never used while in the 10 ASCII Mode track 7 is not used except in frame 5. Thus shifting of the Bit Fiddler data register is necessary in the 10 seven-track and 10 ASCII modes of operation. The shift clock (CLK SR H) goes through a variable delay on BLFR7 to allow time for transfer of the word frames and for any shifting that may be required in the data register. The amount of delay varies according to the mode format.
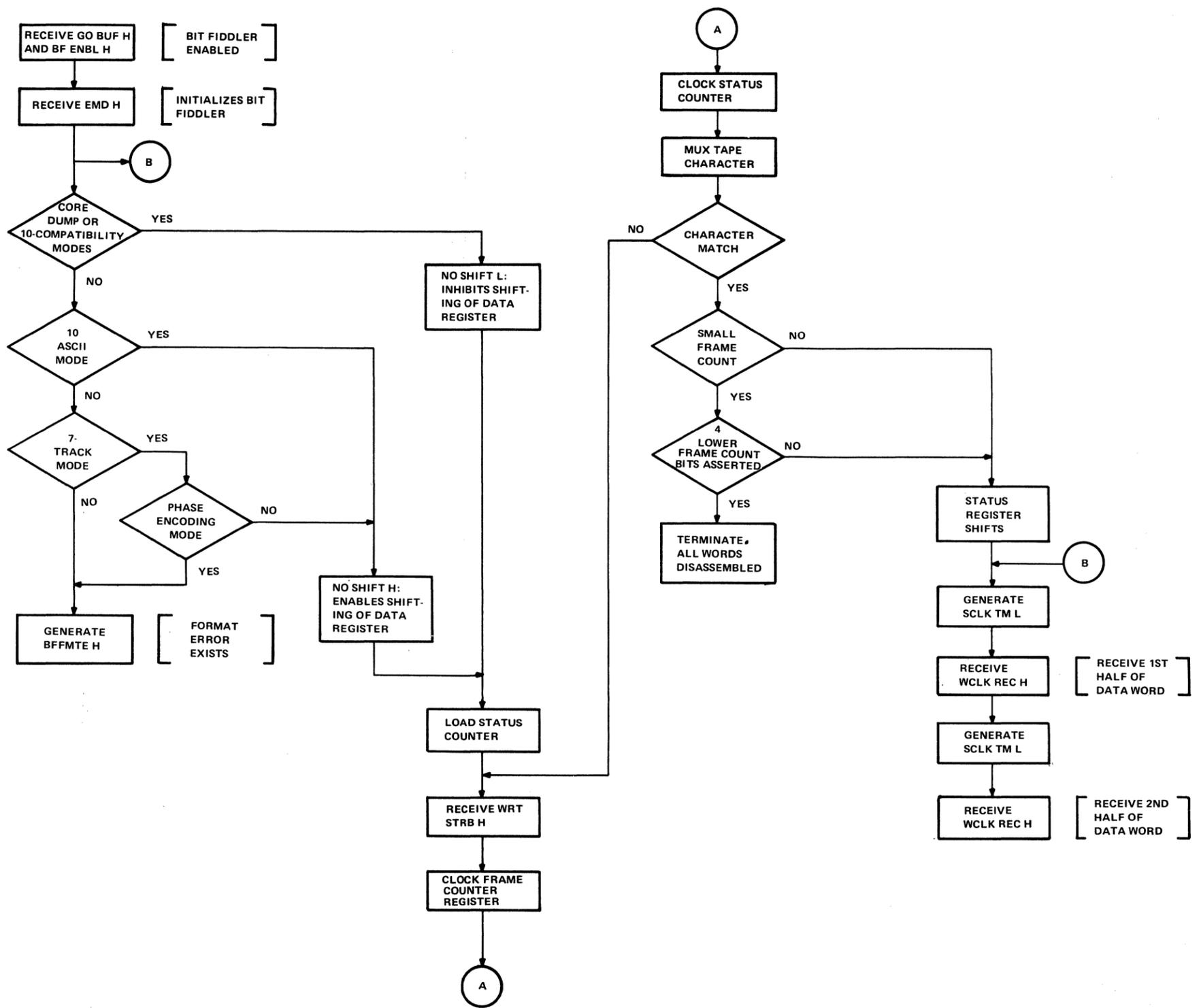
Figure 3.11-1   Bit Fiddler Write Operation Flowchart

Table 3.11-1
Bit Fiddler Format

	Bits			Mode	Number of Tape Frames per Disassembled Word
3	2	1	0		
0	0	0	0	10 Core Dump	5
0	0	0	1	10 Seven Track	6
0	0	1	0	10 ASCII	5
0	0	1	1	10 Compatibility	4

Any other combination produces a Bit Fiddler Format Error (FMTE).

Table 3.11-2
Tape Track Formats

Mode	Format Code	Frame No.	Trk. Par	Trk. 7	Trk. 6	Trk. 5	Trk. 4	Trk. 3	Trk. 2	Trk. 1	Trk 0
10—Compatibility	0011	1	P	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
		2	P	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}
		3	P	B_{16}	B_{17}	B_{18}	B_{19}	B_{20}	B_{21}	B_{22}	B_{23}
		4	P	B_{24}	B_{25}	B_{26}	B_{27}	B_{28}	B_{29}	B_{30}	B_{31}
10—Core Dump	0000	1	P	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
		2	P	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}
		3	P	B_{16}	B_{17}	B_{18}	B_{19}	B_{20}	B_{21}	B_{22}	B_{23}
		4	P	B_{24}	B_{25}	B_{26}	B_{27}	B_{28}	B_{29}	B_{30}	B_{31}
		5	P	*	*	*	*	B_{32}	B_{33}	B_{34}	B_{35}
10—ASCII	0010	1	P	*	B_0	B_1	B_2	B_3	B_4	B_5	B_6
		2	P	*	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}
		3	P	*	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	B_{20}
		4	P	*	B_{21}	B_{22}	B_{23}	B_{24}	B_{25}	B_{26}	B_{27}
		5	P	B_{35}	B_{28}	B_{29}	B_{30}	B_{31}	B_{32}	B_{33}	B_{34}
10—Seven Track	0001	1	P	*	*	B_0	B_1	B_2	B_3	B_4	B_5
		2	P	*	*	B_6	B_7	B_8	B_9	B_{10}	B_{11}
		3	P	*	*	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}
		4	P	*	*	B_{18}	B_{19}	B_{20}	B_{21}	B_{22}	B_{23}
		5	P	*	*	B_{24}	B_{25}	B_{26}	B_{27}	B_{28}	B_{29}
		6	P	*	*	B_{30}	B_{31}	B_{32}	B_{33}	B_{34}	B_{35}

*Blank

PDP-10 CORE WORD   **MASSBUS DATA WORD**   **BIT FIDDLER DISASSEMBLY**

R0 → D0 → B0
LSB

1st Character Written
B7
B8
1st Half of Core Word
2nd Character Written
B15
B16
One PDP-10 Core Word   D17   D0
3rd Character Written
B23
B24
2nd Half of Core Word
4th Character Written
B31
B32
5th Character Written
MSB
R35 → D17 → B35

A. 10 Core Dump Mode

PDP-10 CORE WORD   **MASSBUS DATA WORD**   **BIT FIDDLER DISASSEMBLY**

R0 → D0 → B0
LSB

1st Character Written
B5
B6
1st Half of Core Word
2nd Character Written
B11
B12
3rd Character Written
One PDP-10 Core Word   D17 → B17
D0 → B18
4th Character Written
B23
B24
2nd Half of Core Word
5th Character Written
B29
B30
6th Character Written
MSB
R35 → D17 → B35

B. 10 Seven-Track Mode

PDP-10 CORE WORD   **MASSBUS DATA WORD**   **BIT FIDDLER DISASSEMBLY**

R0 → D0 → B0
LSB

1st Character Written
B6
B7
1st Half of Core Word
2nd Character Written
B13
B14
3rd Character Written
One PDP-10 Core Word   D17   D0
B20
B21
4th Character Written
B27
B28
2nd Half of Core Word
*5th Character Written
MSB
R35 → D17 → B35

*One extra bit written in 5th character

C. PDP-10 ASCII Mode

PDP-10 CORE WORD   **MASSBUS DATA WORD**   **BIT FIDDLER DISASSEMBLY**

R0 → D0 → B0
LSB

1st Character Written
B7
B8
1st Half of Core Word
2nd Character Written
B15
B16
One PDP-10 Core Word   D17   D0
3rd Character Written
B23
B24
2nd Half of Core Word
4th Character Written
D13 → B31
D14
MSB
R35 → D17

D. 10-Compatibility Mode

10-2026

Figure 3.11-2 Tape Frame Formats

3.11-4

3.11.3 Bit Fiddler Timing

When WRT STRB H pulses are received by the Bit
Fiddler, it begins disassembling the data word stored
in the shift register. In NRZ mode, this occurs imme-
diately after the start motion delay, when the TU16 is
at speed and transmits WRT CLK to the TM02. In PE
mode, WRT STRB pulses are generated after the pre-
amble has been written.

WRT STRB H is generated on the Tape Control
Common Mode module (TCCM 4). When DRV SET
PLS H (MBI 6) is asserted during a write data opera-
tion, the Write Data Record flip-flop (E42) is set,
generating WDR H. In NRZ mode, (PESB L negated),

this produces a high at E25 pin 6 and E46 pin 8, and
enables generation of WRT STRB H when WRT CLK
is produced by the TU16. WRT STRB and WRT CLK
will be at the same frequency. In PE mode, WRT
STRB H is also derived from WRT CLK; however, PE
WRT ENABLE L and DATA CLK H must be asserted.
This occurs when the data portion of a record is
written. Because the frequency of DATA CLK H is
half that of WRT CLK, WRT STRB H will also be at
half the frequency of WRT CLK H (Figure 3.11-3).

Figure 3.11-4 is a timing diagram for the Bit Fiddler
during a Write operation in the Core Dump Mode.
Each time a WRT STRB H pulse is generated the

10-1327
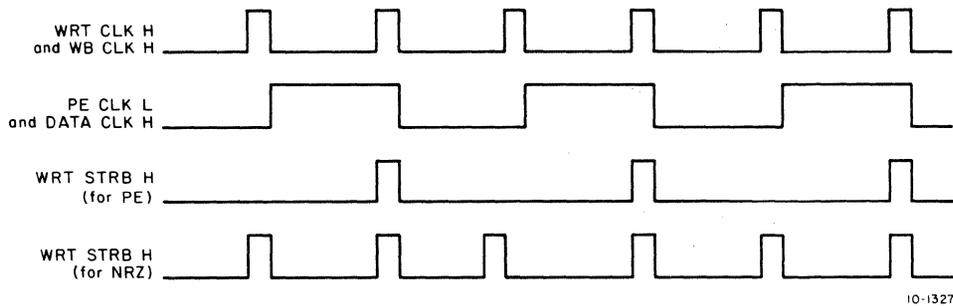
Figure 3.11-3   WRT STRB Timing

10-2027
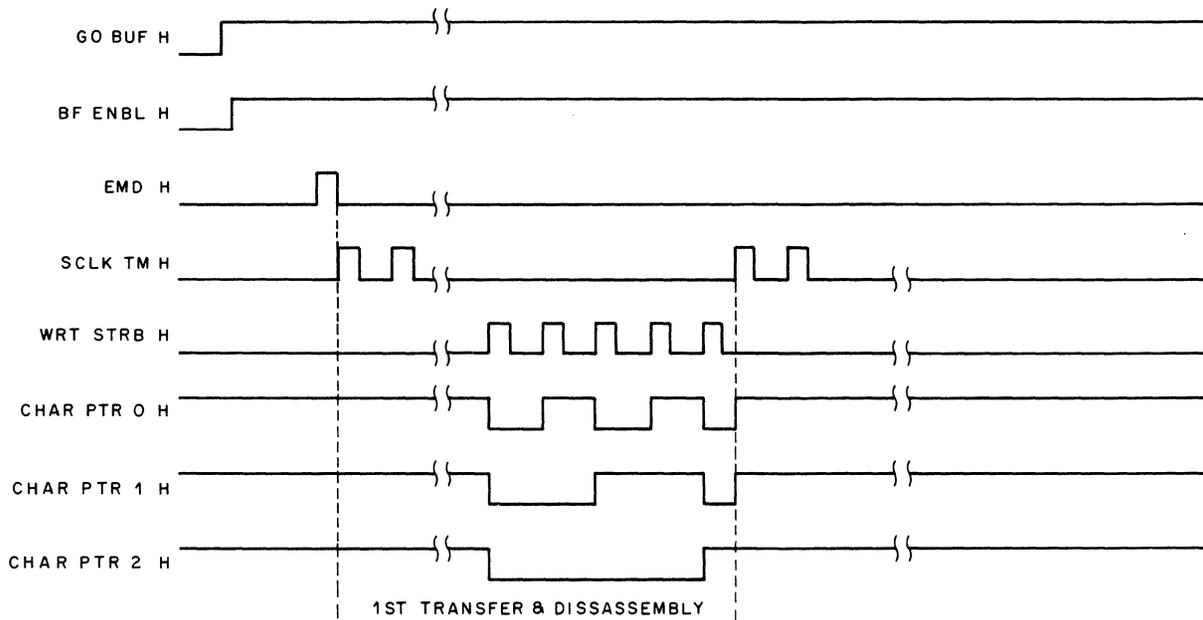
Figure 3.11-4   Bit Fiddler Write Operation in Core Dump Mode

3.11-5

frame count register in the Massbus Interface Module is incremented and the Bit Fiddler status counter (E70) is decremented. For each combination of the status counter output a separate character is multiplexed onto the Bit Fiddler output lines (WDBFO 0—4); this character becomes available to the write circuitry in the TCCM module.

Completion of a data word disassembly is detected by a comparison of the output of the status counter to a decoding of the format lines. When a match is detected CHAR MTCH H (E69-6) is asserted and shifts the status register thereby generating another pair of SCLK pulses to the Massbus. The Massbus RH11 Controller responds to the first SCLK with a WCLK pulse which loads the Bit Fiddler data register with the first half of the next data word. The second SCLK pulse causes the loading of the second half of the data word into the data register. If the format code indicates either 10-ASCII or 10-seven track, the shifting of the bits now takes place. The data register shift pulses are received from the status counter which generates the pulses in accordance with the particular mode of operation. The word is then disassembled and the cycle continues until all of the data has been transferred.

When the last data word has been disassembled and the CHAR MTCH H is asserted, the lower order four bits of the frame count register, gated with the Small Frame Count signal (SFC H) inhibits the CHAR MTCH signal from clocking the status shift register and generating a new SCLK pulse.

If a WRT STRB H pulse occurs before the Bit Fiddler has received a WCLK response from the Massbus Controller, SET DTE L (Set Data Timing Error) is asserted. This causes the DTE bit in the Error Register to be set.

If 10 Seven-track mode is requested while the board is operating in the PE mode, the BF FMTE (Bit Fiddler Format Error) is asserted.

3.11.4 Performance Checks
Perform Wrap-Around tests of PDP-10 Diagnostic MAINDEC-10-DLTUA to check performance of data paths, DPAR circuits and format error circuits (see Paragraph 3.1.2).

3.11.5 Adjustments
None.

3.11.6 Troubleshooting
Symptoms which point directly at Bit Fiddler malfunctions are:

1.   Data late errors.

2.   Data bus parity errors.

3.   Format errors.

4.   Drive timing errors.

If module swapping the M8914 does not correct the trouble, use Figure 3.11-1 to trace trouble to related circuits.

WRITE (PE)

3.12 INTRODUCTION

This pamphlet discusses the operation of the TU16/TM02 write circuitry when operating in PE mode. The write data path (reference Figure 2-4) is covered from the output of the Bit Fiddler to the write heads. Bit Fiddler write operation is described in pamphlets 3.10 (M8906) and 3.11 (M8914).

3.12.1 PE Data Write

The characters multiplexed by the Bit Fiddler onto the Write Data Bit Fiddler Output lines (WDBFO 0—7) are transmitted to the TCCM module. In the TCCM module, the WDBFO lines are input to a parity tree (TCCM 2 E44) and generate a vertical parity bit (PE parity is always odd). The character (parity bit included) is applied to the A inputs of the TCCM Write Multiplex (TCCM 2), and multiplexed to the TCCM Write Buffer.

When the Write Buffer receives WB CLK H, it is loaded with the output of the Write Multiplex. The complemented outputs of the Write Buffer are applied to the D inputs of the Write Multiplex, and loaded into the Write Buffer at alternate WB CLK H pulses. This operation phase encodes the binary data output of the Bit Fiddler.

The uncomplemented outputs of the TCCM Write Buffer are driven by type 75451 drivers across the slave bus to the TU16. The Write Data (WD) lines of the slave bus are received by receivers in the LAW module (M8910) of the TU16 (refer to LAW 3 and 4). The data is then gated by the Write Data Multiplex (E5, E13, and E19) to the Write Deskew Buffer and nine XOR gates. In PE mode (PE + LRC H asserted), the XOR gates cause the Write Deskew Buffer to "follow" its

voltage input. The Write Deskew Buffer is clocked by SK CLK (Skew Clock) pulses (LAW 4). These pulses are delayed REC L pulses, jumpered to compensate for static skew in the write head. The Write Deskew Buffer outputs are then driven to the write head.

3.12.2 PE Data Write Timing

When the TM02 decodes a Write Data function code, it places the WRITE and FWD commands on the slave bus. When the Massbus Controller asserts RUN, the TM02 generates DRV SET Pulse, which sets the WDR (Write Data Record) flip-flop (TCCM 4); this enables generation of WB CLK and REC L pulses when WRT CLK is received from the TU16. The TM02 also transmits SLAVE SET Pulse to the TU16. This initiates tape motion and sets the Write Enable flip-flop (LAW 8). WRITE ENABLE switches current to the write and erase heads (LAW 3). Since no flux reversals can be effected until WRT CLK pulses are produced, the tape is dc erased as it accelerates.

When the transport is up to speed (ACCL H negated), the PE Write Major States circuitry (TCPE 3) is enabled; at the same time, the TU16 begins to transmit WRT CLK to the TM02. The Write Major States circuitry enables the various segments of a PE data record (preamble 0s, preamble 1s, data, postamble 1s, and postamble 0s) to be written. While the preamble is being written, WRT CLK generates WB CLK and REC L pulses (TCCM 4). WB CLK is used in the TCCM write circuitry (TCCM 2) to phase encode the preamble (Figure 3.12-1). REC L is transmitted to the TU16 and causes the phase-encoded characters generated by the TCCM Write Buffer to be transferred to tape.
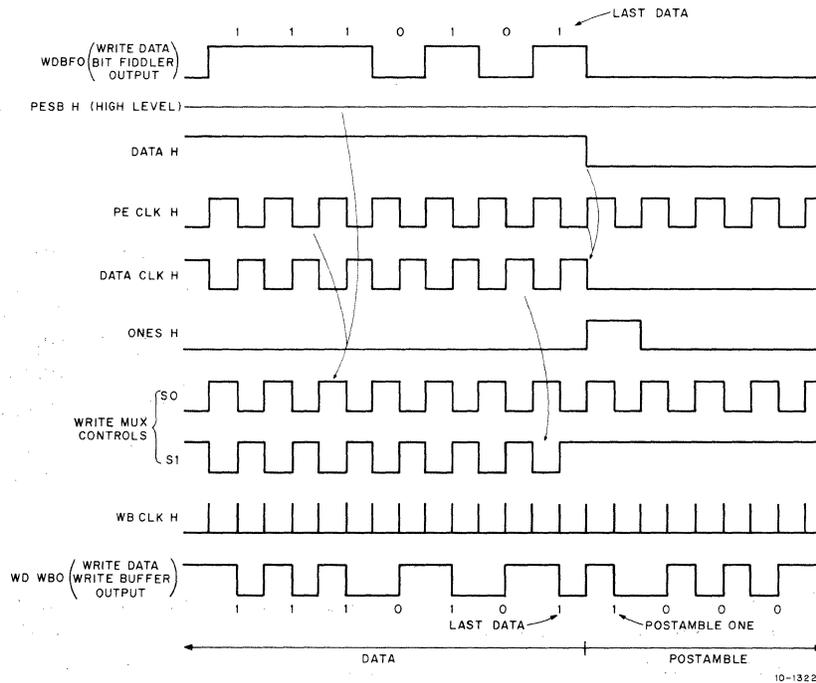
Figure 3.12-1   TCCM Write Operation Timing (PE)

When the preamble has been written, the Write Major States circuitry asserts DATA H. This enables the generation of WRT STRB in addition to WB CLK and REC L, and changes the mode of the TCCM Write Multiplex operation so that it gates data characters from the Bit Fiddler to the TCCM Write Buffer. The WRT STRB pulses cause the Bit Fiddler to generate tape characters from the data words it receives from the Massbus Controller. WB CLK pulses clock the TCCM Write Buffer and phase encode the Bit Fiddler outputs, while the REC L pulses, transmitted to the TU16, cause the data to be transferred to tape. The writing of the data portion of a PE record terminates with Frame Count register (R05) overflow.

3.12.3   Preamble Write Timing
The Write Major States circuitry on TCPE 3 controls various stages of a PE write data operation. At the beginning of a write data operation in PE mode, WDR H (TCCM 4) enables the PRE 0 flip-flop (TCPE 3) to be clocked set by ST CLK (State Clock). However, Write Major States circuitry operation is inhibited until the end of the start motion (acceleration) delay. When the start motion delay is over (ACCL negated), the PRE 0 flip-flop is set; PRE 0 asserts PE WRT ENB L. At the same time, WRT CLK pulses received by the TM02 produce PE CLK, WB CLK H, and REC L pulses (TCCM 4). PE CLK and PESB (Phase Encoded Status Buffered) cause the S0 and S1 inputs of the TCCM Write Multiplex (TCCM 2) to toggle as illustrated in Figure 3.12-1. Because ONES H is not asserted, phase-

encoded 0s are loaded into the TCCM Write Buffer by WB CLK. (The operation is identical to the manner in which postamble 0s are produced, illustrated in Figure 3.12-1.

The number of preamble 0s generated is counted by E5 and E6 on TCCM 3. (The motion delay counter, of which E5 and E6 are a part, thus serves a dual purpose.) When forty 0s have been generated, FORTY H causes the PRE 0 flip-flop to be cleared and the PRE 1 flip-flop to be set; this asserts ONES L, causing the TCCM Write Buffer to be loaded with a phase-encoded 1s character. REC L pulses are continuously transmitted to the TU16, and cause the forty 0s and the 1s character to be transferred to tape.

After the preamble 1s character is written, the PRE 1 flip-flop is cleared, and the Data flip-flop is set. DATA H asserted causes the data portion of the PE record to be written, as described in Paragraph 3.12.2.

3.12.4   Postamble Write Timing
When the Frame Count register overflows (indicating that the data has been written), WRITE END L is generated (MBI 9) and clears the Write Data Record flip-flop (TCCM 4). WDR H negated clears the Data flip-flop (TCPE 3) and causes the POS 1 flip-flop to set. This asserts ONES L, and changes the mode of TCCM Write Multiplex operation (Figure 3.12-1), so that a phase-encoded 1s character is generated and written on tape. The next ST CLK pulse clears the POS

3.12-2

1 flip-flop. This negates ONES L and enables the post-amble 0s to be written on tape. The ST CLK pulse that follows sets the POS 0 flip-flop. While POS 0 is asserted, E5 and E6 of the Binary Counter on TCCM 3 are upcounted from 40 to 80, during which time 40 postamble 0s are written on tape. When EIGHTY L is asserted, the POS 0 flip-flop is cleared; this completes the PE record.

3.12.5 PE Tape Mark Generation
When the DRV SET PLS is produced, the write and erase heads are energized and cause the tape to be erased throughout the start motion delay. DRV SET PLS also causes the TMWIP (Tape Mark Write In Progress) flip-flop (TCCM 4 E42) to be set.

When the start motion delay is over, the Write Major States circuitry (TCPE 3) is enabled, and TMWIP H allows the PRE 0 flip-flop to set. This cases the assertion of PE WRT ENB L, which enables generation of PE CLK, WB CLK, and REC L pulses (TCCM 4).

With PRE 0 asserted, almost the same situation exists as when preamble 0s are written (Paragraph 3.12.3). Forty tape characters will be written on tape, as determined by E5 and E6 on TCCM 3. However, because WFMK L is asserted and input to E33 pin 12 on TCCM 2, bits 3, 4, 6, and 7 of the TCCM Write Buffer are force cleared. Thus, instead of all-0 tape characters, only tracks 1, 2, 4, 5, and 8 will contain 0s; tracks 3, 6, 7, and 9 (corresponding to bits 3, 4, 6, and 7) will be erased.

When the 40 characters comprising the tape mark have been written, FORTY H (TCCM 3) causes the PRE 0 flip-flop (TCPE 3) to be cleared; this inhibits further WB CLK and REC L pulses.

3.12.6 IDB Generation
The IDB is written on tape automatically when a TU16, operating in PE mode, is commanded to perform a write operation while at BOT. The circuitry that detects this condition is located on TCCM 3. The count in the motion delay counter (E5, E6, E14, and E15) is used to activate the Write IDB circuitry. During a write from BOT operation, the start motion delay is 202 ms. Approximately 56 ms into the delay, the Write IDB flip-flop (E26) is forced set and asserts WRT ID BURST L. It remains set for 130 ms, during which time the identification burst is written.

WRT ID BURST L asserted negates ACCL (SB) L (TCCM 3); this enables the TU16 to transmit WRT CLK to the TM02. WRT ID BURST also generates PE WRT ENB L (TCPE 3), which enables generation of PE CLK, WB CLK, and REC (TCCM 4). At the same time, WRT ID BURST is input to E33 pin 13 on TCCM 2, and force clears all the bits of the TCCM Write Buffer except for the parity bit. WRT ID BURST H, input to E83 pin 13 on TCCM 2, enables PARITY DATA SET UP H, which causes the Write Buffer parity bit to produce alternate 1s and 0s. The net result is alternate 1s and 0s on the parity track (track 4) while all other tracks are erased.

3.12.7 Performance Checks
Perform TM02/TU16 Data Reliability Program diagnostic (see Paragraph 3.1.2).

3.12.8 Adjustments
The only adjustment directly affecting the proper operation of the TU16/TM02 write circuitry is the write skew adjustment (Paragraph 4.18.6). The adjustment should only be performed after replacing the head plate assembly, or when excessive wear in the head plate assembly is suspected. Note that before adjusting write skew, the read skew adjustment (Paragraphs 5.4.13 and 5.4.14) must be performed.

3.12.9 Troubleshooting
To troubleshoot the Write (PE) function, run the TM02/TU16 Data Reliability Diagnostic and use Table 3.12-1 to analyze the results.

Table 3.12-1
Analysis of Data Reliability Diagnostic For Write (PE) Troubleshooting

Problem	Symptom		Remedy
FCE (Frame Count Error)	Postamble detected too soon.		Check postamble detect circuitry on M8901 (DS 3, 5, 7) Check postamble flip-flop on M8902 (dwng TCPE5)
	Error caused by certain data patterns.		Check for dead track.
	————————————		Check EBL on M8909 (dwng MBI9) Check RUN from RH controller and on MASSBUS.
CORR SKEW Error	One or more tracks using third stage of deskew buffer (M8901 - DS2, M8902; Dwng TCPE 2)		Problem is one track sensing end of preamble too soon or too late.
CORR SKEW Error and CORR DATA Error	One track is missing.		Check for damaged tape.
NSG Error	During a read operation one or more channels of read data completes a record in the wrong state. e.g. Overshoot on the last transition being recognized as an extra transition.		Check for poorly written tape. Check G056.
	Some unerased data left in the IRG.		Check for misaligned erase head.
PEF, CDE, INC Errors	————————————		Check tape for dirt and defects. Check for capstan jitter. Check operation of phase locked loop. Check deskew buffer. Check G056. Check read states circuits on M8902.
Incorrectable data error with all zeros in check character register and no CS/ITM error.	Parity error exists with no dead track.		Check for defective component in the deskew buffer (DS 3, 5, 7; Dwng TCPE 2).
Check Character Register repeatedly contains the same bit set.*	Trouble is in only one track. Swap the M8901 modules	Trouble is in same track.	Check for trouble in TU16. Check analog and digital outputs of G056.
		Trouble is in different track	Check M8901.
PEF Error	More than one dead track due to improper detection of preamble and postamble.		Check for poor quality tape. Check tape speed regulation.
Records are being written improperly.	————————————		Check M8910 (head drivers). Check M8902 (Write major states). Check M8903 (Write buffer). Check PE Write voltages according to Table 3.15-3.

*A 777 in the check character register may indicate a late detection of postamble which causes the check character register to be strobed at the wrong time.

CONTENTS

3.13 INTRODUCTION

This pamphlet discusses the operation of the TU16/TM02 write circuitry when operating in NRZ mode. The write data path (reference Figure 2-4) is covered from the output of the Bit Fiddler to the write heads. Bit Fiddler write operation is described in pamphlets 3.10 (M8906) and 3.11 (M8914).

3.13.1 NRZ Data Write

The characters, multiplexed by the Bit Fiddler onto the Write Data Bit Fiddler Output lines (WDBFO 0—7), are transmitted to the TCCM module. In the TCCM module, the WDBFO lines are input to a parity tree (TCCM 2 E44), and generate a vertical parity bit (odd or even, as determined by the program). The character (parity bit included) is applied to the A inputs of the TCCM Write Multiplex (TCCM 2), and multiplexed to the TCCM Write Buffer.

When the Write Buffer receives WB CLK H, it is loaded with the outputs of the Write Multiplex. The outputs of the Write Buffer are then driven by type 75451 drivers across the slave bus to the TU16.

The Write Data (WD) lines of the slave bus are received by receivers in the LAW module (M8910) of the TU16 (refer to LAW 3 and 4). The data is then gated by the Write Data Multiplex (E5, E13, and E19) to the Write Deskew Buffer and nine XOR gates. In NRZ mode, the XOR gates cause the Write Deskew Buffer to be complemented for each 1 that is written. The Write Deskew Buffer is clocked by SK CLK (Skew Clock) pulses (LAW 4). These pulses are delayed REC L pulses, jumpered to compensate for static skew in the write head. The Write Deskew Buffer outputs are then driven to the write head.

3.13.2 NRZ Data Write Timing

When the TM02 decodes a Write Data function code, it places the WRITE and FWD commands on the slave bus. When the Massbus Controller asserts RUN, the TM02 generates DRV SET Pulse which sets the WDR (Write Data Record) flip-flop (TCCM 4); this enables generation of WB CLK and REC L pulses when WRT CLK is received from the TU16. The TM02 also transmits SLAVE SET Pulse to the TU16. This initiates tape motion and sets the Write Enable flip-flop (LAW 8). WRITE ENABLE switches current to the write and erase heads (LAW 3). Since no flux reversals can be effected until WRT CLK pulses are produced, the tape is dc erased as it accelerates.

When the transport is up to speed, WRT CLK pulses are transmitted to the TM02 and generate WRT STRB, WB CLK, and REC L pulses. WB CLK is used to load the TCCM Write Buffer with the outputs of the TCCM Write Multiplex (Figure 3.13-1). REC L is transmitted by the TM02 to the TU16, where it causes the tape character presently in the TCCM Write Buffer to be transferred to tape. WRT STRB activates the Bit Fiddler to generate the next character.

WB CLK, WRT STRB, and REC L pulses continue until the WDR flip-flop is cleared. This occurs when the Frame Count register overflows and generates WRITE END (MBI 9).

3.13.3 CRCC Generation

Data input to the TCCM is also input to the CRCC Generator (CNRZ 2). The generator, clocked by WB CLK, produces the CRCC by a series of shifts and XORs. The outputs of the CRCC Generator (CRC 1—7, P) are applied to the B inputs of the TCCM Write
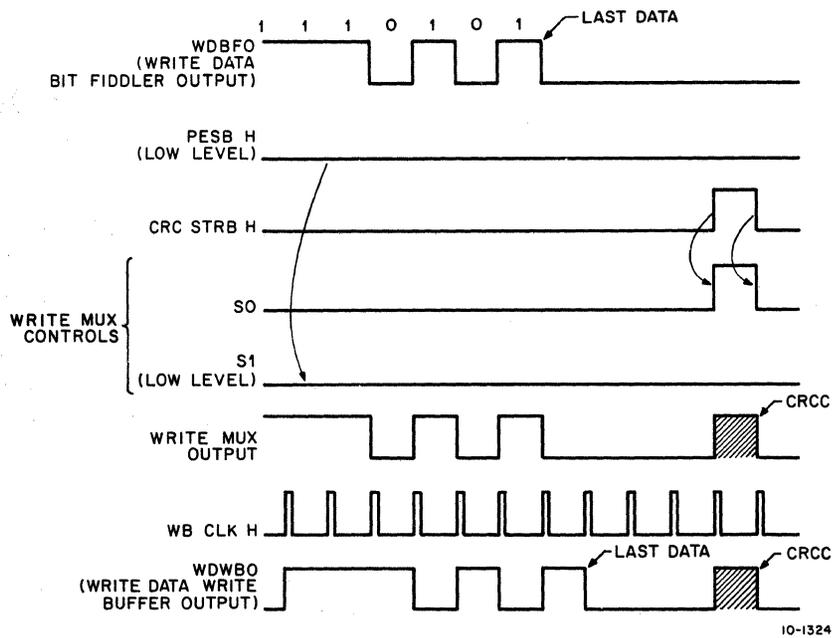
Figure 3.13-1 TCCM Write Operation Timing (NRZ, 1 of 9 Tracks)

Multiplex. After the data portion of the record is written, the CRCC is transmitted to the TU16 and written on tape.

3.13.4 CRCC and LRCC Write Timing
When the data portion of an NRZ record has been written, the WDR flip-flop is cleared; this enables Binary Counter E27 (TCCM 4) to be upcounted by WRT CLK. The counter, initially preset to a count of 8, generates CRC STRB H when it reaches a count of 11, and LRC STRB L when it reaches a count of 15. At a count of zero, further clocking is inhibited. Therefore, three clock pulses increment the counter to 11; another four clock pulses increment it to 15, so that CRC STRB H is produced three character spaces after the data, and LRC STRB L is generated seven character spaces after the data.

Whenever LRC STRB or CRC STRB occur, WRT CLK ENBL H is momentarily asserted, and gates out one WB CLK H pulse and one REC L pulse.

When CRC STRB H is asserted, the TCCM Write Multiplex (TCCM 2) gates the outputs of the CRCC Generator (CNRZ 2) to the TCCM Write Buffer (Figure 3.13-1). The WB CLK produced at CRC STRB time loads the buffer with the CRCC. The character is driven to the LAW module in the TU16, and applied to the Write Deskew Buffer. When REC L is received by

the TU16, the Write Deskew Buffer is clocked, and the CRCC is transferred to tape, three character lengths past the last date character (Figure 3.13-2).

LRC STRB L, input to E38 pin 2 on TCCM 2, clears the entire TCCM Write Buffer and causes 0s to be transmitted to the Write Deskew Buffer in the TU16. LRC STRB L is also transmitted to the TU16, where it causes PE + LRC H (LAW 4) to be asserted. This signal, input to the Write Deskew Buffer, causes it to follow the data at its inputs when clocked. Thus, when REC L causes SK CLK to clock the Deskew Buffer, the buffer is cleared. Because the bits of the Write Deskew Buffer, initially cleared by WRITE ENABLE H negated, are toggled only when 1s are written on tape, the buffer contains the LRCC. When the buffer is cleared by SK CLK, the LRCC is transferred to tape.

3.13.5 NRZ Tape Mark Generation
During a write tape mark operation, WFMK is asserted. WFMK L is input to E24 pin 12 on TCCM 2, and causes all the bits of the TCCM Write Buffer to be cleared, while at the same time NRZ WTMK L, 7 CH TM 1 and 7 CH TM 0 are generated. These signals are input to slave bus drivers E13 (pins 6 and 7), E21 (pins 2 and 6), and E12 (pin 6), thereby forcing the tape mark character onto the Write Data (WD) lines of the slave bus. The tape mark character forced on the WD lines is 23 (nine-channel NRZ format).
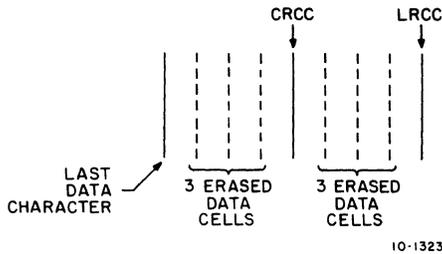
3.13-2

Figure 3.13-2   CCRC and LRCC Timing

3.13.6   Tape Mark Write Timing
When the DRV SET PLS is produced, the write and erase heads are energized, and cause tape to be erased throughout the start motion delay. DRV SET PLS also causes the TMWIP (Tape Mark Write In Progress) flip-flop (TCCM 4 E42) to set. This loads the type 74197 Binary Counter (E27) and also allows WRT CLK H to be gated by E49 (pins 8, 9, and 10) to produce WB CLK H and REC L.

When the start motion delay is over and the first WRT CLK pulse is received by the TM02, the first WB CLK H produced clears the TMWIP flip-flop; thus, further WB CLK and REC L pulses are temporarily inhibited. The REC L pulse produced, along with the WB CLK H pulse, cause the Write Deskew Buffer in the TU16 to be clocked, and transfer the tape mark character to tape.

With the TMWIP flip-flop now clear, the type 74197 Binary Counter is enabled. It operates in the same manner as during a CRCC and LRCC write, except that WFMK H asserted, input to E41 pin 3 on TCCM 4, inhibits the production of CRC STRB H. However, LRC STRB is produced in the normal manner, and occurs seven character spaces after the tape mark character.

LRC STRB L, input to pin 2 of AND gate E8 on TCCM 2, removes the tape mark character forced on the WD lines of the slave bus; this causes 0s to be input to the Write Deskew Buffer in the TU16. LRC STRB L, and the REC L pulse it produces, are also transmitted to the TU16, and cause the Write Deskew Buffer to clear, thereby transferring the LRCC of the tape mark character (which is *identical* to the tape mark character) to tape.

3.13.7   Performance Checks
Perform TM02/TU16 Data Reliability Program diagnostic (see Paragraph 3.1.2).

3.13.8   Adjustments
The only adjustment directly affecting the proper operation of the TU16/TM02 write circuitry is the write skew adjustment (Paragraph 4.18.6). The adjustment should only be performed after replacing the head plate assembly, or when excessive wear in the head plate assembly is suspected. Note that before adjusting write skew, the read skew adjustment (Paragraphs 5.4.13 and 5.4.14) must be performed.

3.13.9   Troubleshooting

3.13.9.1   TM02/TU16 Data Reliability Program Diagnostic — Run the TM02/TU16 Data Reliability Program diagnostic using Pattern 1, 800 BPI and 20 characters. Use Table 3.13-1 to analyze the results of the Data Reliability diagnostic.

NOTE
If an OPI error occurs with a VPE error, troubleshoot the OPI error first. (See Paragraph 3.5.10.-3.) This type of problem is usually caused by to few RSDO pulses.

If the trouble is not found, change the pattern to 3 (rippling 1s) and rerun the diagnostic. Use Table 3.13-2 to analyze the results of the Data Reliability diagnostic.

Problem	Symptom			Remedy
CRC and LRC Errors				Check gain adjustment of G056.
	Look for a dead channel by letting the program run until some error printouts are obtained.			Check the WD line of the dead channel with an oscilloscope triggered from the REC line. The waveform of figure 3.13-3 should be obtained.
	If the error printout resembles CRC 377-777 LRC 377-777 the parity channel is dead. If the error printout resembles BN: 20 G 377 B 357 a dead channel exists.[1]	Analog signal for dead channel [2] is missing or distorted. Check analog signals (Fig. 3.13-4A) on pins A04L1, B04B1, B04M1, CO4K1, C04L1, D04P1, D04R1, F04P1 and F04R1. Mount a skew tape and check the read channel (Fig. 3.13-4B) on pins A04B1, A04F1, B04F1, B04K1, C04P1, Co4R1, D04V1, E04E1 and F04K1.	Read channel is bad.	Check G056. Check read head cable. Check read head.
			Read channel is good.	Repair or replace M8910. Check for faulty back panel wiring. Check write head cable. Check write head. Check RD line. Check M8911 and cables. Check G056 and cables. Check M8913 and cables.
CRC, LRC and VPE Errors without data errors.				Check for "clean" analog signals (Fig. 3.13-4A). Check that the data pulses are approximately 9 volts peak-to-peak. Check that the CRC and LRC pulses are less than 5 volts above and below ground. Check pin E04K1 for the packet waveform shown in Figure 3.13-4C, D. Insure that each pulse is less than $2 \mu sec$ wide and that pulses occur every $28 \mu sec$. Check that logic "highs" are greater than $+2.4$ Vdc and all logic "lows" are less than $+0.8$ Vdc.
NEF (Non-Executable Function) Error.				Check that WRL (Write Lock) at pin F01K2 is at $+3$ Vdc. [3]
	The PESB (Phase Encoded Status Signal) signal is incorrect. The signal should be $+3$ Vdc for density 0, 1, 2, and 3; and 0 volts for density 4, 5, 6, and 7.			Check that DEN lines are in correct state. Check that 7 CH is not floating.
NSG (Non Standard Gap) Error.	Excessive number of RSDO pulses are being generated.			Check read circuitry.
FMT (Format) Error.	Format code in TM02 Control Register (bits 4, 5, 6, and 7 of location 172432) is not 14.			Stop and restart the program and retype the format code.
ITM (Illegal Tape Mark) Error.	When the program starts check the response to TM = 0.	Typed response is 0 or RETURN.		Check for system fault.
		Typed response is 1.		Check for bad tape.
		Typed response is 1 and ITM is printed more than once.		Check data channels 0, 1, and 4.
FCE (Frame Count) Error.	Error occurs at end of read operation.			Check for 18 RSDO pulses.
	Error occurs at end of write operation.			Trouble is in TM02 or RH11.
DTE (Drive Timing Error) DBPE (Data Bus Parity Error) CBPE (Control Bus Parity Error) RMR (Register Modification Refuse) ILR (Illegal Register) ILF (Illegal Function)				Trouble is in TM02, controller or processor.

[1] To determine which channel is dead, convert the G and B numbers, which are in octal, to binary.

			Channel 4	Channel 0
G	=	377	=	011 111 111
B	=	357	=	011 101 111

Channel 0 is the least significant (right-most) bit. In the above example, Channel 4 is dead.

[3] If WRL is at ground, a write lock condition will exist and it will be impossible to execute a write command. Refer to the M8910 circuit schematic.

[2] Convert the data channel number to the physical track number as follows:

Data Channel Number	=	Physical Track Number
P		4
7		7
6		6
5		5
4		3
3		9
2		1
1		8
0		2

REC ⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔ +3V / ØV

WD � +3V / ØV

10-2019

Figure 3.13-3   REC and WD Signal Waveforms

A. ANALOG SIGNAL

B. RD SIGNAL   + 4 V

28
MICROSECONDS   0.2 to 0.4 V

C. PACKET SIGNAL

D. EXPANDED PACKET
   PULSE

SKEW JITTER

10-2020

Figure 3.13-4   Read Signals

Problem		Remedy
Grounded RD or WD line	Check printout as follows to locate bad channel. BN: 1 Channel 0 G 0 0 0 0 0 0 1 0 B 0 0 0 0 0 0 1 1 BN: 2 G 0 0 0 0 0 1 0 0 B 0 0 0 0 0 1 0 1 BN: 3 G 0 0 0 0 1 0 0 0 B 0 0 0 0 1 0 0 1 Note that for each B (bad data) printout, Channel 0 is a one (1). This indicates that either RD0 or WD0 is shorted to ground.	Check RD and WD of faulty channel for short to ground.
Data lines tied together	Check printout as follows to locate connected data lines. BN: 1 Channel 6 Channel 1 G 0 0 0 0 0 0 1 0 B 0 1 0 0 0 0 1 0 BN: 6 G 0 1 0 0 0 0 0 0 B 0 1 0 0 0 0 1 0 BN: 17 G 0 0 0 0 0 0 1 0 B 0 1 0 0 0 0 1 0 Note that for each B (bad data) printout, Channels 1 and 6 are always the same. This indicates that WD1 and WD6 are tied to each other.	Check on slave bus (cable A) for connection between two data lines indicated by printout.
Intermittent errors on data channel 0.	Error printout indicates that data channel 0 is intermittent.	Check that both ends of cables A and B are correctly installed. Using an oscilloscope, check for the wave shapes of Figure 3.13-5.

A. WRITE SIGNAL WAVEFORMS USING NEGATIVE EDGE
OF REC(SB) L FOR SCOPE TRIGGER
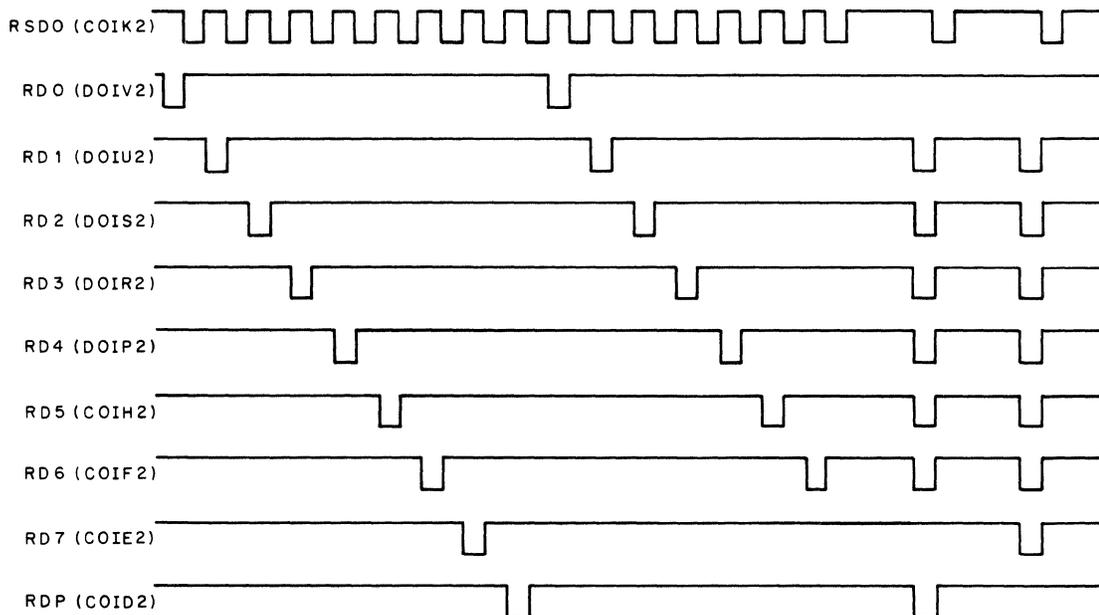
B. READ SIGNAL WAVEFORMS USING NEGATIVE EDGE
OF RSDO FOR SCOPE TRIGGER

NOTES:
1. When checking these waveforms, put PDP-11 keys 2, 3,
   10, 11, 12, and 13 up. Keys 2 and 3 cause a foward write.
   Keys 10 through 13 inhibit error checking and printout.

2. Record count =1; character count= 20_8; switches 2 and 3 up.

3. Set oscilloscope for 0.1ms/cm.

10-2021

Figure 3.13-5   NRZI Signal Waveforms Using Pattern 3 and 800 BPI

CONTENTS

3.14 INTRODUCTION

This pamphlet describes the routing of power to and within the TU16/TM02 cabinet.

3.14.1 TU16/TM02 Power System

Power to the TU16/TM02 cabinet is controlled by an 861 Power Controller, which is in turn controlled, via a remote cable, by a power controller in an adjacent cabinet. The power controllers in each cabinet are interconnected by remote cables. A ground (which originates at the processor POWER Key switch), transmitted via the remote cables, activates the interconnected controllers, and causes them to apply ac power to the power controller's switched outlets. Refer to the *861-A, B, C Power Controller Maintenance Manual* (DEC-00-H861A-A-D) for a complete description of the 861 Power Controller.

The TU16 power supply and the TM02 power supply (type H740D) plug into the switched outlets of the 861 Power Controller (Figure 3.14-1). The TU16 power supply supplies all power required by the TU16 Tape Transport, as well as 115 Vac to operate the cabinet fan. The TM02 power supply (H740D) provides power (and power fail logic signals AC LO and DC LO) to the TM02 logic assembly. The H740D Power Supply is discussed in detail in the *H740D Power Supply Maintenance Manual* (DEC-11-H740A-A-D). The H740D Power Supply has been modified slightly to provide 115 Vac to the TM02 logic assembly cooling fan. The H740D ac harness (Figures 1-1 and 1-5 in the H740D Power Supply Maintenance Manual) has been tapped, and 115 Vac is brought out through the side of the power supply mounting box.
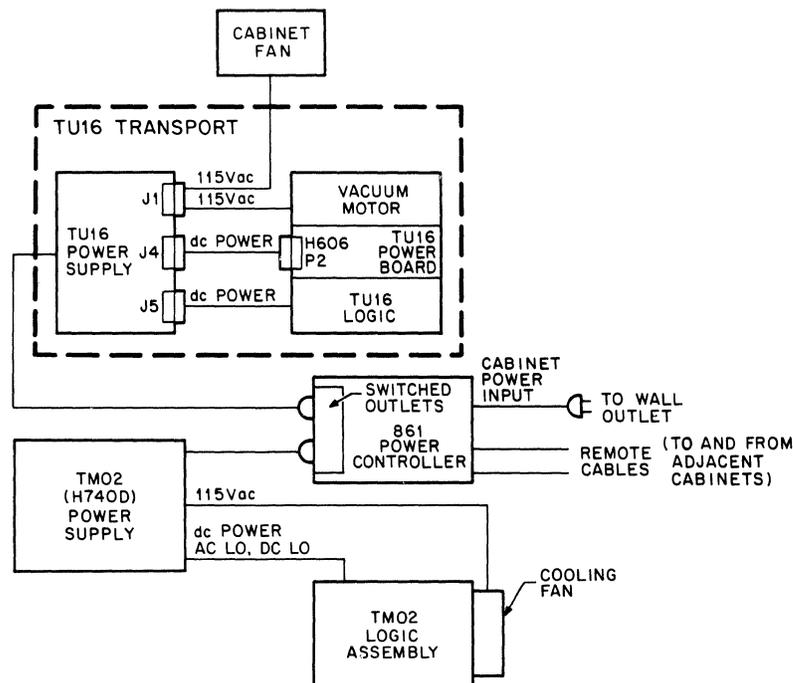
Figure 3.14-1   TU16/TM02 Power System

TU16 POWER SUPPLY

3.15   INTRODUCTION

The TU16 power supply is an air-cooled unit that converts single-phase, 115 V or 230 V nominal, 47—63 Hz line voltage to five regulated output dc voltages (+5 V, +12/+5 V, +12 V, and -6.4 V), and four unregulated voltages (± 16 V and ± 18 V). The power supply is controlled by the same 861 Power Control that controls the TM02 power supply. Each of the regulated voltages has short circuit (current foldback) protection. Overvoltage (crowbar) protection is incorporated in the +5 V, +12 V, and -6.4 V circuits.

The power supply is divided into two sections (Figure 4-1): the ac input circuitry, consisting of the transformer and large filter capacitors (transformer-capacitor assembly); and a regulator board, which contains the remaining circuitry. The power supply circuit description references schematic D-CS-5410451-0-1. The regulator board (Figure 3.15-1) contains all the circuitry between the transformer secondary winding and the power supply output cables. A four-pin Mate-N-Lok connector (J1) supplies voltage to the fan and vacuum motor. Connector J2 connects the transformer secondary winding outputs to the regulator board while J3 adds the large filter capacitors to the circuitry. Connector J4 connects the supply to the H606 Power Board servo circuitry and J5 supplies voltages to the TU16 backplane.

3.15.1   Generation of Raw ± DC

The ac power line cord, terminated with tab connectors, is brought to the lower left-hand area of the regulator board (as viewed from the rear of the TU16 cabinet) and connected to the input power tabs (AC HI, AC LO, and GND). Two wires (in the same area) connect to either the 230 V tab or the 115 V tabs, and configure the power supply for 115 V or 230 V

operation. The J2 Mate-N-Lok connector interconnects the regulator board and the main transformer.

A general block diagram of the TU16 power supply is shown in Figure 3.15-2. The center-tapped transformer voltage is fused, rectified, and filtered prior to being fed to the various voltage regulators and J4. The fuses do not normally blow when an output is shorted because of an overcurrent (current foldback) protection. Overvoltage protection (crowbar) is also used on all regulated outputs except the +12/+5 V (NRZ/PE) output. which does not require it.
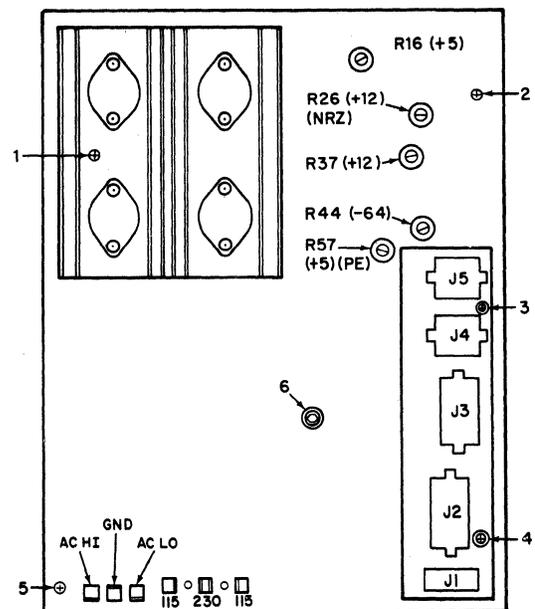
NOTES:
1) 1-5 represent 5 Phillips head screws.
2) 6 represent Allen screw-must be secured very tightly, or damage to the power supply may result.

IO-1317

Figure 3.15-1   TU16 Power Supply Regulator Board
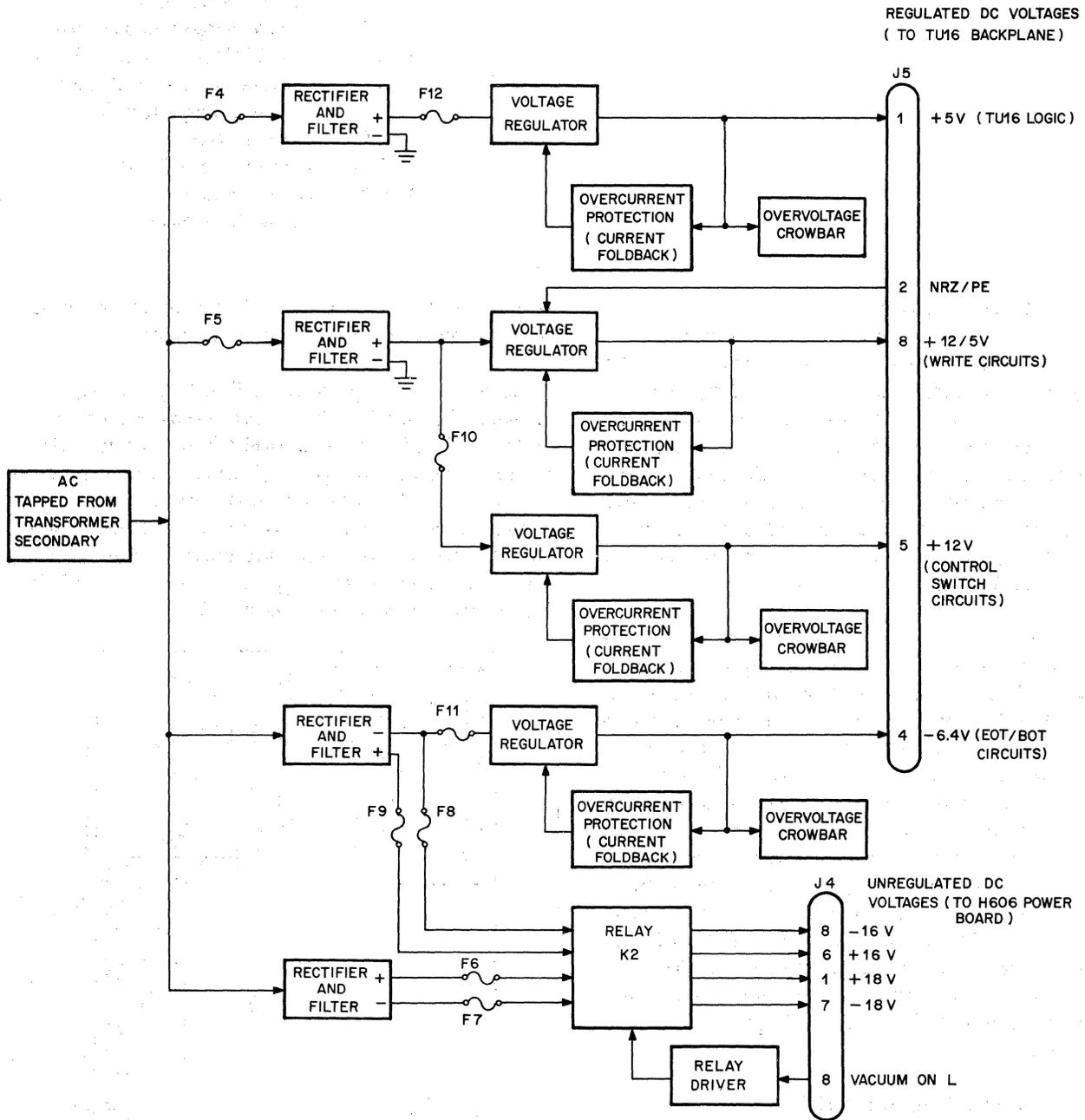
Figure 3.15-2   TU16 Power Supply Block Diagram

The J4 Mate-N-Lok plug connects the TU16 power supply's unregulated voltages to the TU16 Power Board (H606, plug P2). Once tape is loaded onto the transport, signal VACUUM ON L is asserted. This puts a low signal at the inputs of the 75451 gate (schematic D-CS-5410451-0-1, location A7) that enables the K2 relay. This relay passes required voltages on to the H606 module when tape is loaded.

3.15.2 +5 VDC Regulator Circuit

The +5Vdc regulator circuit is shown in Figure 3.15-3. Raw dc voltage in input to pin 3 of the LM300 voltage regulator. The output voltage from pin 2 is fed to transistors Q6 and Q5, which are series regulators used to increase the current output capabilities of the circuit. Resistors R20, R18, and R19 sense the output current. R19 is used as a current limit monitor by the LM300. As the current increases, the voltage across R19 increases. When a reference voltage is exceeded, the LM300 begins to turn off Q6 and Q5, impeding current flow. The current does not stop, but instead decreases to a safer level; this is called current foldback. It assures that the output current never goes over 4.8 A. Refer to Figure 3.15-4 which shows how the current foldback procedure works. As the current surpasses the limit of 4.8 A, the conduction of Q5 and Q6 slows down (toward being shut off) until no voltage is produced (at the short circuit current rating). The output voltage may be regulated. Resistors R15, R16, and R17 divide the actual output voltage. Pin 6 of the LM300 accepts the output feedback voltage through R16; the adjustment of R16 regulates the +5 V output.

In addition to the current foldback feature, a voltage crowbar circuit is used, offering overvoltage protec-

tion. If for some reason Q5 or Q6 become shorted, the overvoltage protection circuit protects any load connected to the power supply. When Q5 or Q6 short circuits, the output voltage starts increasing very rapidly. As the voltage across the D16 zener diode becomes greater than 6.8 V, it breaks down and begins conducting; it does not conduct during normal operation. Current now begins to flow through R22. When the voltage at the junction of D16 and R22 becomes greater than approximately 0.7 V (at the gate of D15), the SCR fires and begins conducting. This offers a path for current from the output to ground, shunting any load, thus protecting it. The SCR continues conducting until the power supply is turned off or the 5.0 A fuse is blown. Diodes D13 and D14 protect the LM300 from any kickback voltages that may occur.

3.15.3 +12/5 VDC Regulator Circuit

The +12/5 Vdc regulator circuit is shown in Figure 3.15-5. It operates in a manner similar, but not identical, to the +5Vdc regulator circuit discussed previously. In the case of the +12/5 Vdc regulator, a type 723 regulator is used (instead of the LM300) and two selectable voltages are available. If NRZ mode is se-

Figure 3.15-4 Current Foldback Operation

Figure 3.15-3 +5V Regulator Circuit

Figure 3.15-5 +12/+5V Regulator Circuit

lected, the +12 V output is used; if PE is selected, +5 V is developed instead. This is discussed in more detail later in this section.

The 723, like the LM300, is a precision voltage regulator. However, the 723 is a two-level regulator, in that it can output two selectable voltages. Raw dc from the bridge rectifier network enters pins 12 and 11 of the 723. The TU16 write driver circuits require +12 V and +5 V for NRZ and PE modes, respectively. If NRZ is selected, a high level is presented through J5, pin 2, to the inputs of the 75451, which outputs a high level through R57 by R23 and R24 and lets the full reference voltage from pin 6 of the 723 enter the noninverting input (pin 5). A +15 V output is produced.

When PE mode is selected, a low (ground) level is passed through the 75451, setting up the voltage

divider between R23 and R24 and offering a lower voltage to the noninverting input of the 723. The output becomes +5 V.

It is therefore observed that the correct write drive circuit voltages are produced by the same supply when the specific mode of operation is selected.

The output (from pin 10) of the 723 is sent to Q7, where higher current is produced for the output. The current foldback and sense circuits operate in a manner similar to those of the LM300. Output voltage is divided by R25, R26, and R27, and is adjusted by R26. Resistor R57 is also a voltage adjustment. It adjusts the reference line to the 723. When adjustments are made, R26 must be adjusted before R57, because the reference voltage is dependent on the actual output voltage.

As output current increases, the voltage across R30 and R31 also increases. As the voltage reaches the limit of the 723, it is sensed at pin 2. The output from the 723 starts reducing, starting to shut off Q7 and keeping the output current from reaching unsafe levels.

No overvoltage protection is provided in the +12/5 V power supply section because it is not necessary. The circuit that this supply feeds can stand voltage higher than this regulator can supply.

3.15.4 +12 VDC Regulator Circuit

The type 723 regulator used in the +12 V supply operates in exactly the same way as the previous 723 regulator. However, in the +12 V circuit, only one voltage is produced: +12 V (Figure 3.15-6).

Figure 3.15-6 +12V Regulator Circuit

In the +12 V regulator circuit, resistor R37 is the fine adjustment for the output voltage. Resistors R41, R39, R40, and R55 offer the sense for the current foldback network. The overvoltage network acts in the same way as the network in the +5 V supply, except the zener diode (D23) does not conduct until the voltage across it becomes greater than 15 V. Then the SCR fires and offers a path for output current, if Q8 becomes shorted for some reason.

3.15.5 -6.4 VDC Regulator Circuit

The TU16 power supply also furnishes a regulated -6.4 V (Figure 3.15-7). The LM304 is a complement of the LM300, intended for systems requiring regulated negative voltages. Rectified negative voltage is presented to the LM304 from the negative output of the D11 diode bridge.

The LM304 output from pin 7 goes to the base of transistor Q11. Transistor Q11, connected with Q10, looks and acts like a normal PNP device; the combination supplies high current to the output.

Transistor Q12 is used in the current foldback network. Output current is sensed by R50, the V_{eb} of Q11, R49, and R51. As the output increases (becomes more negative), the voltage at the base of Q12 also increases (becomes more negative). Transistor Q12 starts to turn on and, as it does, shunts LM304 output current away from Q11-Q12, limiting output current. Then, as the output decreases, Q12 begins to shut off and allows the output current to rise again.

The overvoltage protection works identically to the other networks. Zener diode D20 begins conduction at approximately -8.2 V, which fires the SCR (D26) and creates a path to ground if Q10 and/or Q11 should short out. Again, the supply must be turned off to allow C22 to discharge before D26 stops conducting. Diodes D24 and D25 protect the LM304 against any overvoltage surges.

3.15.6 Specifications

Tables 3.15-1 and 3.15-2 list the power supply specifications.

3.15.7 Performance Checks

Check the voltages at the J5 connector (under load) and ensure that they are within the tolerances indicated in Table 3.15-3.

Table 3.15-1
Power Supply Input Specifications

Parameter	Specification
Input Voltage (1 phase, 2 wires, and ground)	95—132/190—264 V
Input Frequency	47—63 Hz
Input Current	7 A nominal at 115 V, 60 Hz
Inrush	85 A at 115 V rms, 60 Hz
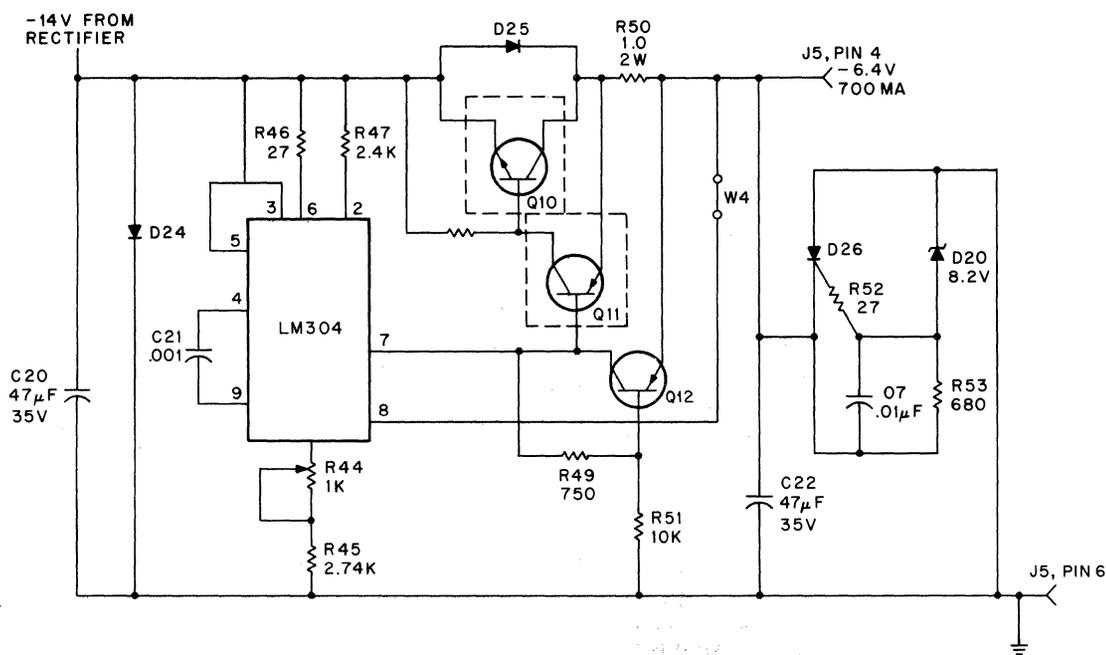
Figure 3.15-7   -6.4V Regulator Circuit

10-1321

Table 3.15-2
Power Supply Output Specifications

Parameter	Specification
+5 V Regulator Circuit	
Load Range	5 A maximum
Overvoltage Crowbar	6.4 V 10%
Current Foldback	
at 25° C	3 A nominal
Backup Fuse	5 A
Adjustment	5% minimum
Regulation	Less than 2%
+12/+5 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crowbar	None
Current Foldback	
at 25° C	0.5 A
Backup Fuse	1 A
Adjustment	35% min/ 30% min
Regulation	Less than 3%
+12 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crowbar	15.5 V 10%
Current Foldback	
at 25° C	0.75 A to 0.3 A
Backup Fuse	0.75 A
Adjustment	10% minimum
Regulation	Less than 3%
-6.4 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crowbar	8 V
Current Foldback	
at 25° C	0.75 A to 0.3 A
Backup Fuse	0.75 A
Adjustment	10% minimum
Regulation	Less than 3%

3.15.8 Adjustments

Five adjustments to the power supply adjust the five dc output voltages: +5 V, +12/+5 V, +12 V, and -6.4 V. A small screwdriver is all that is required. Clockwise adjustment of any of the potentiometers increases voltage. All potentiometers are located on top of the TU16 power supply board. Refer to Figure 3.15-1 for the respective locations and to Table 3.15-3 for adjustment values. Do not make adjustments if voltages are within tolerances of Table 3.15-3.

Use a calibrated voltmeter, preferably a digital voltmeter. Voltages should be adjusted to the values indicated in Table 3.15-3.

CAUTION
Do not adjust voltages beyond their 105 percent rating and adjust slowly to avoid overvoltage crowbar.

3.15.9 Troubleshooting

Troubleshooting information for the power supply consists of troubleshooting rules, hints, and a troubleshooting chart. This information provides a maintenance aid to isolating power supply (schematic D-CS-5410451-0-1) malfunctions.

3.15.9.1 Troubleshooting Rules — Troubleshooting rules for the power supply are as follows:

1. Ensure that power is turned off and the unit is unplugged before servicing the power supply.

2. The TU16 power supply may be accessed from the rear of the TU16 cabinet, or from the sides when the TU16 is moved forward on its slides.

3. Ensure that capacitors C8, C11, C15, and C20 are discharged before servicing the

Table 3.15-3
TU16 Power Supply Regulated Voltages

J5 Connector Pin Number	Adjustment Potentiometer	Voltage (Under Load) Volts	Wire Color Code
1	R16	5.2 to 5.3*	RED
4	R44	-6.3 to -6.4	YEL
5	R37	12.0 to 12.1	GRN
8	R26	12.0 to 12.4 (NRZ)	ORN
8	R57	5.3 to 5.4 (PE)*	ORN

*Note that the +5 volts is set to a value greater than 5 volts.

power supply. A 10- to 100-ohm, 10 W resistor can be used to hasten the discharge of the capacitors. (Be sure power is off.)

4. All fuses can be replaced without removing the module portion of the power supply.

5. For proper operation, all hardware must be secured tightly to about 12 in.-lb. All hardware should be replaced with identical hardware replacement parts.

6. The module portion of the power supply may be removed from its mounting area by removing five Phillips head screws (1—5 on Figure 3.15-1) and one Allen head screw (6 on Figure 3.15-1).

7. When replacing semiconductor components that are secured to the heat sink, apply a thin coat of Wakefield No. 128 compound or Dow silicon grease to the heat sink contact side (bottom) of the semiconductor. Insulating wafers are not required.

8. If a diode pack is replaced, it is imperative that the Allen head screw used to secure it is very tight. If the screw is not tightened securely, overheating of the diode pack can result.

3.15.9.2 Troubleshooting Hints

CAUTION
Unplug the TU16 before servicing

The most likely source of power supply malfunction is the module portion of the supply. A quick remedy for a malfunction may be to replace the entire module. The problem could, however, be a short circuit in the system unit or possibly a defective component or other problem in the ac input circuit.

The +5 V, +12 V, and -6.4 V regulators contain overvoltage detection circuitry. If any one of the potentiometers (used to adjust regulated output voltage) is adjusted too far clockwise, the corresponding crowbar circuit will trip. To avoid this, adjust the particular potentiometer fully counterclockwise and readjust per Paragraph 3.15.8.

Make a visual examination of the circuitry. Check for burnt resistors, cracked transistors, burnt printed circuit board etch, oil leakage from capacitors, and loose connections. A good visual check can prove to be a quick method of locating the cause of a malfunction.

3.15.9.3 Troubleshooting Charts — In checking the various areas of the power supply, the rules listed in Paragraph 3.15.9.1 should be followed. In addition to the main troubleshooting chart (Table 3.15-4), a separate fuse chart (Table 3.15-5) is included.

Table 3.15-4
Troubleshooting Chart

Problem	Cause
No +5 V (J5; 1,7)	F4 or F12 open D9 or transformer open +5 V adjusted too high
+5 V output too low	LM300 bad Q5 or Q6 shorted R20, R15, R16 opened
+5 V too high	D16 open R16 or R17 open
No +12/+5 V (J5; 8)	F5 open D10 or transformer open +12/+5 V adjusted too high
+12/+5 V output too low	723 bad 75451 shorted Q7 shorted R32, R25, R26 opened
+12/+5 V output too high	R26, R27 opened 75451 shorted
No +12 V (J5; 5)	F10 open D11 or transformer open
+12 V output too low	723 bad Q8 shorted R41, R36, R37 opened
+12 V output too high	D23 open R37, R38 open
No -6.4 V (J5; 4)	F11 open D11 or transformer open
-6.4 V output too low	LM304 bad Q10, Q11 shorted R50, R49, R51, R45 open
-6.4 V output too high	D20 open R44, R45 open

Table 3.15-5
Fuse Chart

Fuse	Type	Indication Fuse Is Open
F1	4 A	Vacuum motor not on
F2	4 A	No voltage outputs in 115 V configuration; low voltage outputs in 230 V configuration
F4	5 A	No +5 Vdc No power indicator No logic response
F5	1 A	No +12/+5 Vdc No +12 Vdc No write current No read data
F6	15 A	No +18 Vdc to H606 Power Board No reel motor No brake
F7	15 A	No -18 Vdc to H606 Power Board No reel motor
F8	8 A	No -16 Vdc to H606 Power Board No reverse capstan
F9	8 A	No +16 Vdc to H606 Power Board No forward capstan
F10	0.75A	No +12 Vdc
F11	0.75A	No -6.4 Vdc EOT and BOT sensed erroneously No read data out
F12	5 A	No +5 Vdc No power indicator No logic response

CHAPTER 4
REMOVAL AND REPLACEMENT
AND ADJUSTMENT PROCEDURES

4.1 INTRODUCTION
This chapter outlines the removal and replacement procedures and adjustment procedures for the TU16/TM02 Tape Drive System. The major TU16 assemblies referenced throughout this chapter are shown in Figure 4-1. Access to the interior components of the TU16 is gained by rotating the service locks on the upper left-hand side and lower right-hand side of the TU16 to release the unit from the cabinet (Figure 4-2).

4.2 TOOLS AND EQUIPMENT REQUIRED
Table 4-1 lists tools and equipment required to maintain the TU16/TM02.

4.3 OPERATOR CONTROL PANEL
To replace burnt-out bulbs in the operator control panel, proceed as follows:

1. Remove power from the TU16 Tape Transport.

2. Loosen the screw at the bottom-center of the control box and remove the panel.

3. Use a bulb extracting tool to remove and replace defective bulbs.

4. Mount the panel on the control box and tighten the screw.

The procedure for removing the control box is:

1. Remove power from the TU16 Tape Transport.

2. Disconnect the cable that runs from the rear of the control box to the M8910 module.

3. Remove the two cable clamp screws.

4. Loosen and remove the four nuts securing the control box to the casting.

5. Carefully remove the control box to ensure the connecting cable is not damaged.

CAUTION
This procedure should be done carefully, since the cable clamp bracket and control box can both fall and become damaged.

6. Reverse steps (in order) 5 through 2 to install the control box.

4.4 DOOR SEAL (FRONT CASTING PERIMETER)
Proceed as follows to replace the door seal along the casting perimeter (Figure 4-2):

1. Remove power from the TU16 Tape Transport.

2. Remove any tape reels to avoid possible contamination of the tape.

3. Pull the old foam stripping from the front casting.

4. Remove all adhesive residue from the casting with Freon or another suitable solvent.

5. Cut the new foam stripping to proper length before removing the protective backing.

6. Remove the protective backing from each strip and carefully press each strip into place around the casting perimeter.

7. Close the glass door to ensure correct latching and to ensure against binding the stripping.

4.5 EOT/BOT ASSEMBLY
To remove the EOT/BOT assembly, proceed as follows:

CAPSTAN

VACUUM DOOR
(OPEN)

HEAD PLATE ASSEMBLY
(COVER REMOVED)

EOT/BOT
ASSEMBLY

CONTROL PANEL

TAKE-UP REEL

FILE REEL

7660-22

VACUUM ASSEMBLY

TU16 POWER SUPPLY

LOGIC BACKPLANE
ASSEMBLY

CAPSTAN MOTOR

TAKE-UP REEL
MOTOR

FILE REEL MOTOR
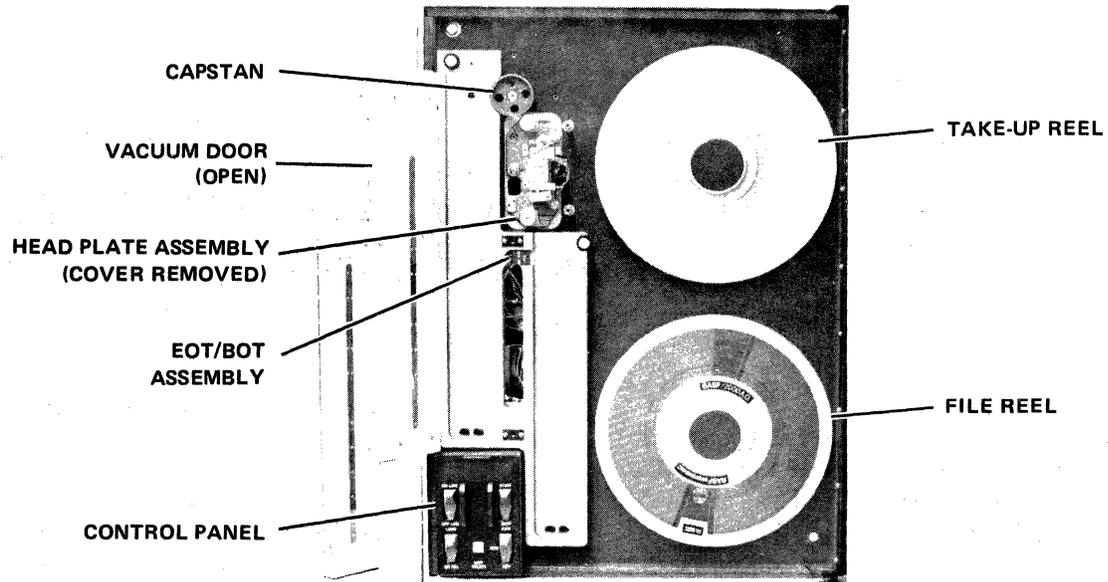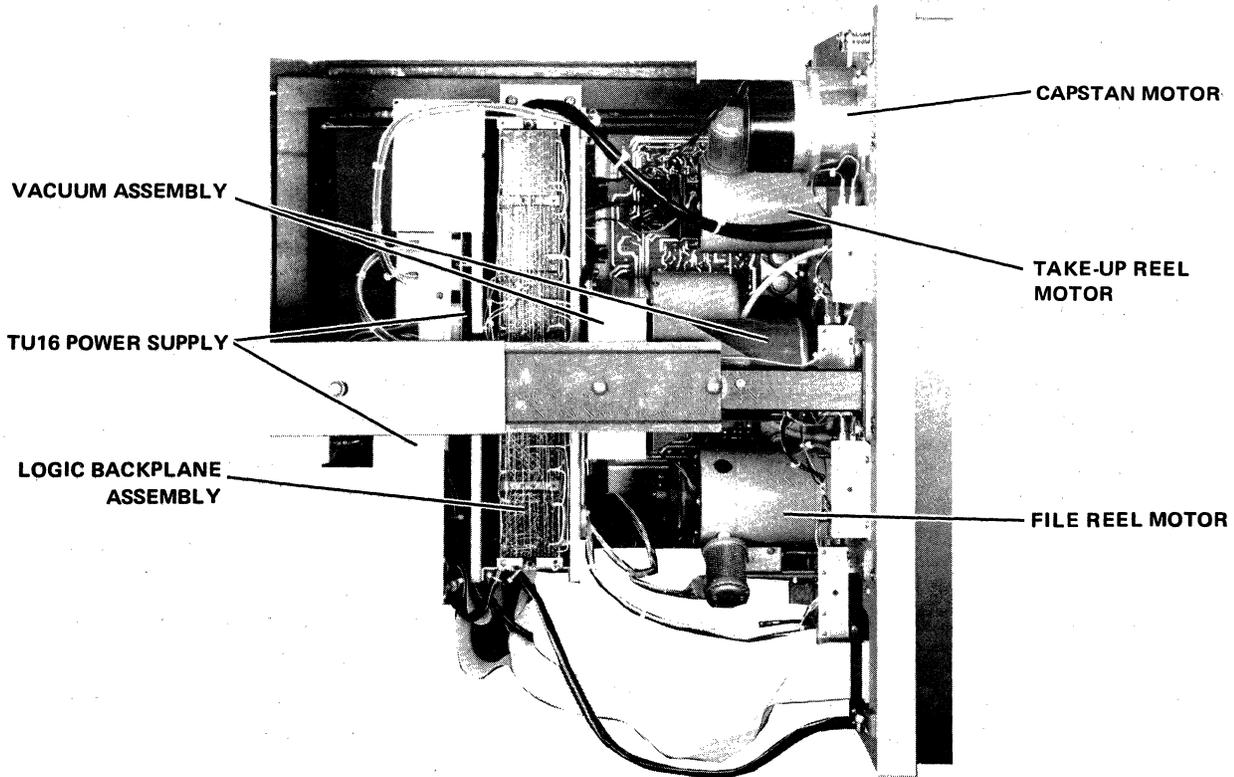
6999-9

Figure 4-1   TU16 Tape Transport Assemblies

4-2

1. Remove power from the TU16 Tape Transport.

2. Open the glass vacuum column door.

3. Use a small screwdriver to loosen the EOT/BOT assembly mounting screw.

4. Disconnect the wires from the back panel.

   Red   — C02A2
   Orange — C02D1
   Yellow — C02C1
   Brown   — C02D2

5. Carefully remove the assembly.

6. Replace the faulty assembly and install by reversing steps 3 through 5.

7. Check for proper alignment by ensuring that the EOT and BOT markers are sensed; adjust the assembly is necessary.

4.6 REEL MOTOR FILTER ELEMENTS

The procedure for replacing the reel motor filter elements (Figure 4-3) is:

1. Remove power from the TU16 Tape Transport.

2. Release the service locks and pull the transport out (forward) on the cabinet slides.

3. Reach in from the left side (as viewed from the front) of the transport and unscrew the filters from the reel motors (one filter from each motor).

Table 4-1
Required Tools and Equipment and Their Use

Item	Part No.	Usage* 1	2	3	4	5
1. Skew Tape (800BPI) 1200 ft.	29-19224	X				X
or 600 ft.	29-22020	X				X
2. Reel Hub Tool	29-18611					X
3. Roller Guide Tool	29-18607					X
4. Microscope	29-20273				X	X
5. Magna-see	29-16871				X	X
6. Penlight		X	X	X	X	X
7. Alignment Glass	74-13969					X
8. Depth Micrometer	29-22039					X
9. Shim stock .001	48-50023-01					X
.002 (red)	48-50023-03					X
.003 (green)	48-50023-04					X
.004 (tan)	48-50023-05					X
.005 (blue)	48-50023-06					X
.0075 (transparent)	48-50023-07					X
.010 (brown	48-50023-08					X
10. TU16/TM02 Module Swap Kit		X				
11. Oscilloscope (Techtronix 453 or equivalent)		X		X	X	X
12. Three Oscilloscope Probes		X		X	X	X
13. Feeler Gauge Set		X		X	X	X
14. Allen Wrench Set		X		X	X	X
15. EOT/BOT Markers (Reflective Strips)					X	X
16. Ground Isolation Plug (Scope Float)		X		X	X	X
17. Vacuum Belt Tension Gauge		X				

*Usage Legend

1. Routine Corrective Maintenance
2. Monthly P.M.
3. Quarterly P.M.
4. Semi-Annual P.M.
5. Major Tape Path Alignment (See Paragraph 4.17.1 for when required.)

SERVICE
LOCK

DOOR
SEAL

SERVICE
LOCK

6999-11
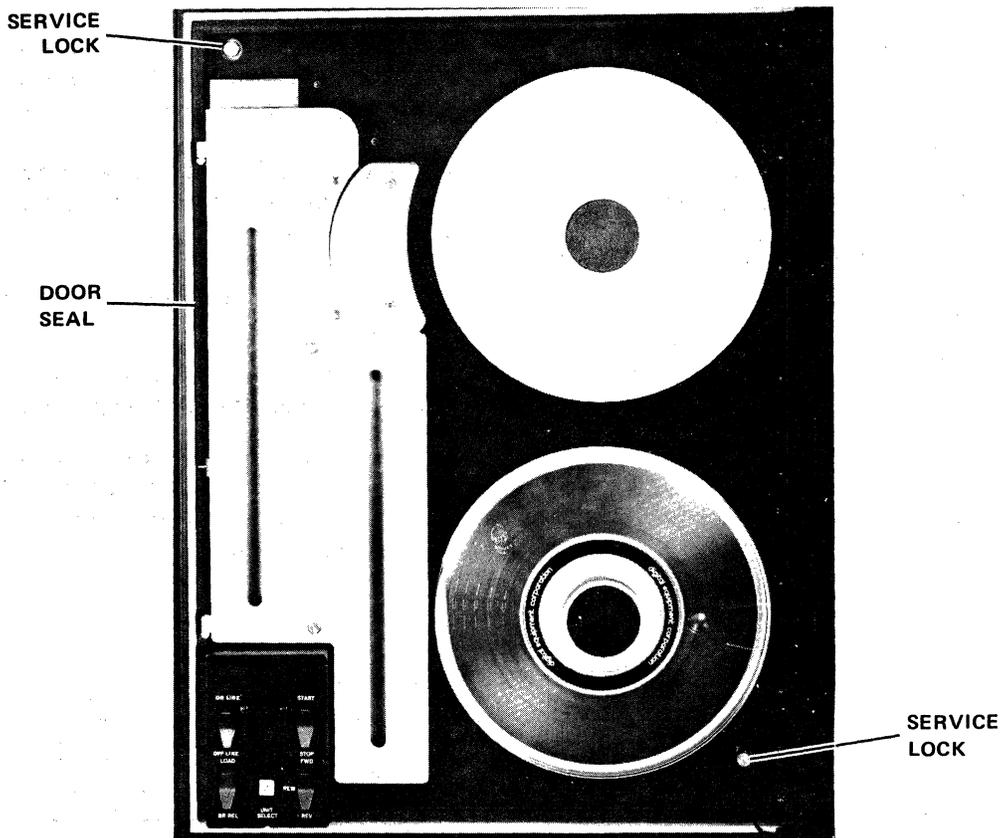
Figure 4-2   Transport Casting, Front View

4. Unscrew the two 4-40 Kep-nuts securing each filter body.

5. Remove and replace the filter elements within the filter bodies.

6. Reassemble each filter body and wrap one turn of Teflon tape on the mounting threads.

7. Screw each filter back into its servo motor mounting area and hand tighten.

4.7   REEL HUB COMPRESSION RING AND TEFLON WASHER

Proceed as follows to replace the reel hub compression ring and Teflon washer (Figure 4-4):

1. Remove power from the TU16 Tape Transport and remove the tape reel.

2. Carefully snap out the plastic disk from the reel hub.

3. Mark the position of the center roll pin in the hub guide.

4. Using a pair of heavy duty diagonal pliers, carefully remove the center roll pin.

5. Grasp the reel hub and unscrew the knob from the hub.

6. Remove (in order) the Teflon washer, pressure plate, and rubber compression ring.

7. Lightly lubricate the flat surfaces of a new compression ring with silicon grease. Wipe all excess grease from the ring with a lint-free cloth.

8. Install (in order) the new compression ring, pressure plate, and a new Teflon washer.

9. Lightly lubricate the knob on the hub until the compression ring is compressed and fully seated.

10. Loosen the knob until it is free of the Teflon washer. Then gently screw it in until it just touches the washer.

4-4
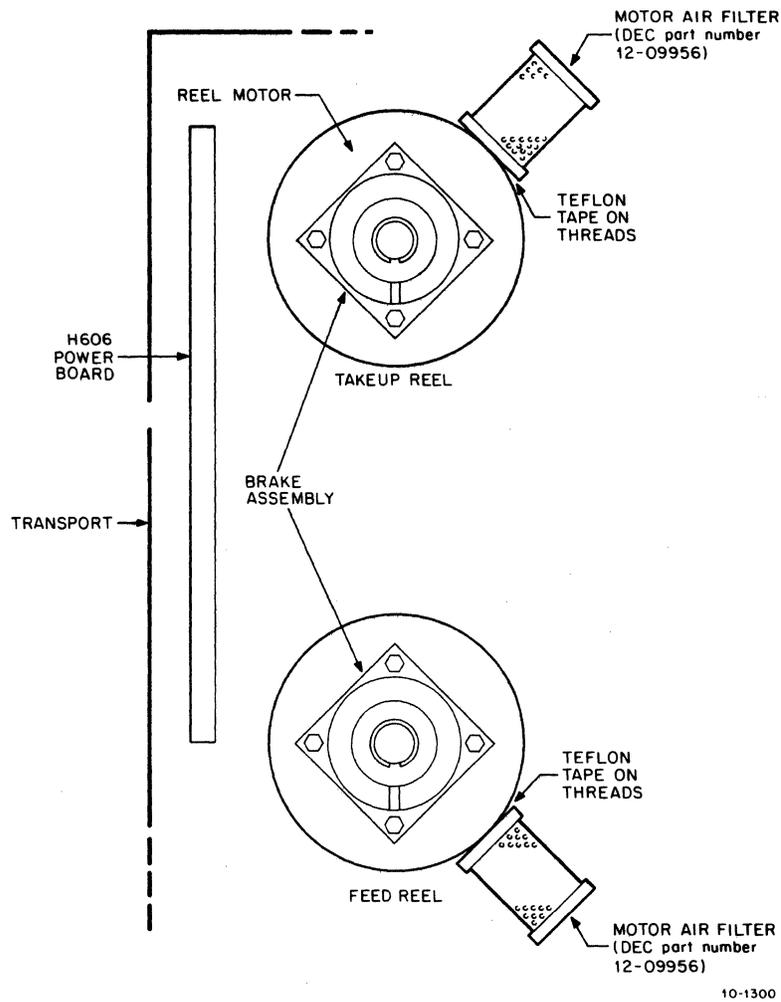
Figure 4-3   Reel Motors, Rear View

11. Reinstall the roll pin in the same hole from which it was removed (step 4).

12. Turn the knob counterclockwise until the roll pin makes contact with one of the two hub stop pins.

13. Try to install a tape reel on the hub. If the tape reel does not easily slip on the hub, move the stop pin back one hole at a time until the knob can be released far enough to permit the tape reel to slip on the hub.

14. With a tape reel installed, tighten the knob (clockwise) until the roll pin contacts the other hub stop pin. If the tape reel is not secure, the stop pin must be moved ahead until the knob can be tightened correctly.
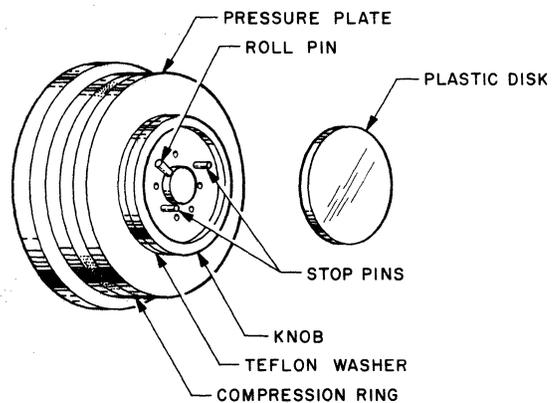
Figure 4-4   Hub Composition

4.8 REEL HUB ASSEMBLY

Proceed as follows to replace the reel hub assembly (Figure 4-5):

1. Remove power from the TU16 Tape Transport and remove the tape reel.

2. Loosen the two Allen locking screws that secure the reel hub to the reel motor drive shaft. (Access holes for the locking screws are located on the side of the hub.)

3. Remove the reel hub assembly, along with the 3/16-inch key (by pulling carefully) and carefully remove any burrs from the motor shaft.

4. Install a new reel hub assembly and the 3/16-inch key on the motor shaft and, using the reel hub alignment gauge, set the clearance between the back surface on the hub assembly and the machined boss on the main casting.

5. Tighten the two Allen locking screws.

4.9 REEL MOTOR

Proceed as follows to remove and replace a reel motor (Figure 4-1):

NOTE
The reel motor brushes are not field replaceable.

1. Remove power from the TU16 Tape Transport.

2. Remove the reel hub assembly. Refer to Paragraph 4.8.

3. Unplug the P3 connector from the rear of the H606 Power Board.

4. Remove the pins from the P3 plug and observe that the motor and brake wires are now disconnected from the connector.

5. Remove the four captivating screws that secure the motor to the deck casting. Remove the motor.

CAUTION
When removing these four screws, it is necessary to support the motor from the rear. If support is not supplied, the motor will fall when the screws are removed.

6. Remove the air filter(s) from the motor(s).

REEL HUB ALIGNMENT GAUGE #29-18611
(Should feel friction in vertical ($\updownarrow$) axis. Gauge should not move in horizontal ($\leftrightarrow$) axis.)

HUB LOCKING SCREW ACCESS OPENING

REEL HUB ALLEN LOCKING SCREWS (2)

TEFLON WASHER

3/16 INCH KEY

REEL HUB ASSEMBLY

FRONT OF TRANSPORT

TOP OF TRANSPORT

MACHINED ALIGNMENT BOSS

REEL MOTOR DRIVE SHAFT

CP-0104
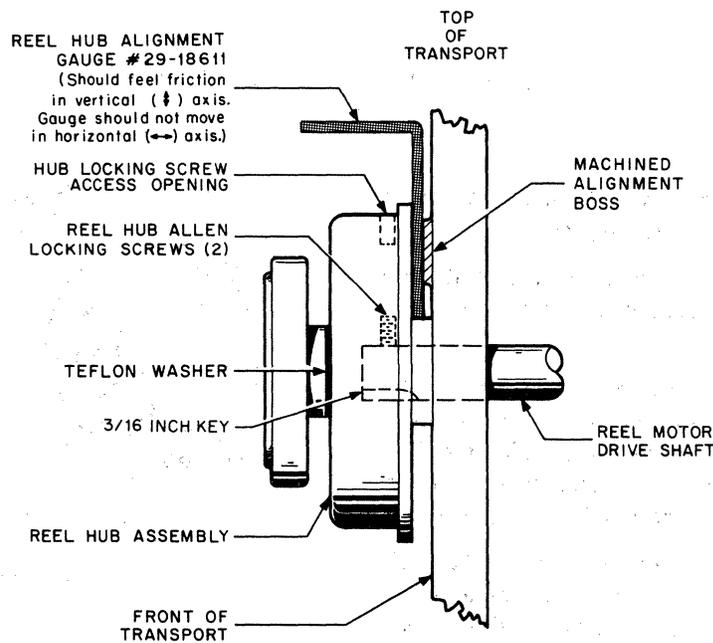
Figure 4-5   Reel Hub

7. Using the brake assembly removal procedure, remove the brake assembly.

8. Reinstall the brake assembly and air filter on the new reel motor.

9. Replace the reel motor and tighten the four captivating screws to a torque value of 10 in.-lb.

10. Reinstall the reel hub assembly and replace the pins in P3 plug. (Refer to Paragraph 4.8.)

4.10 REEL MOTOR BRAKES

If the stator slot is worn away, proceed as follows to remove and replace the reel motor brakes:

1. Remove power from the TU16 Tape Transport.

2. Unplug the brake (P3) connector from the rear of the H606 Power Board.

3. Remove the pins (from P3) holding the wires for the particular brake being removed. Observe that the wires for that particular brake are now disconnected from their respective P3 pin locations.

4. Loosen the hub clamp with an Allen wrench and withdraw the clamp, rotor, rotor disk, and spring (Figure 4-6).

5. Remove the four 10-32 screws securing the stator to the reel motor.

6. Replace the reel motor and secure the stator to the motor assembly using four 10-32 screws. Ensure that the stator slot is at the 6 o'clock position.

7. Slide the rotor disk, rotor and clamp onto the motor shaft. Insert a 0.010-inch feeler gauge between the stator and rotor disk face and rotate the disk face 360° to obtain the required clearance at all points between the stator and rotor disk face.

8. Position the hub clamp away from the rotor and over the slotted section of the sleeve as shown in Figure 4-6. The gap size is not critical so long as the entire clamp is gripping the slotted section of the sleeve.

9. Tighten the hub clamp.

10. Replace the spring as shown in Figure 4-6.

11. Reinsert the brake wires into the brake connector (P3). Insert the connector back in its correct location on the H606 Power Board.

NOTE
The armature is driven by three pins on the hub. It is important that the armature does not bind on the pins.

4.11 VACUUM SWITCHES AND RUBBER SLEEVES

Proceed as follows to replace the vacuum switches and/or rubber sleeves on the switches (Figure 4-7):

1. Remove power from the TU16 Tape Transport.

2. Release the service locks and pull the transport out on the cabinet slides.

3. Remove the two 8-32 screws securing the switch brackets to the casting; pull the brackets backward to disengage the assembly.

NOTE
One switch assembly is located directly in front of the vacuum system. It may be easier not to remove the switch bracket, but to instead go on directly to step 4.

4. Carefully detach the pair of fast-on connectors from each switch and note their respective positions for reassembly purposes.

5. Remove the switch from the bracket by removing the two 2-56 screws.

6. Replace the rubber sleeve on each switch with a 7/8-inch length of tubing. Replace the switch when necessary.

7. If a switch is replaced, it should be left untightened until the bracket is secured to the casting. This allows for any misalignment present in the mechanics.

CAUTION
Never overtighten the screws securing the vacuum switches to the bracket. Damage to the switch may result.

8. Reconnect the fast-on connectors to all switches.

STATOR MUST
BE MOUNTED
WITH SLOT IN
DOWNWARD
POSITION

REAR VIEW

REEL MOTOR
BRUSH RETAINER

.010"
CLEARANCE

SPRING

GAP SUCH THAT CLAMP
IS OVER SLOTTED
SECTION OF ROTOR
SLEEVE.

REEL MOTOR

MOTOR SHAFT

CLAMP

ROTOR

ROTOR DISC

STATOR SLOT

STATOR

REEL MOTOR
BRUSH RETAINER

MOTOR DRIVE
WIRES

10-1301

SIDE VIEW
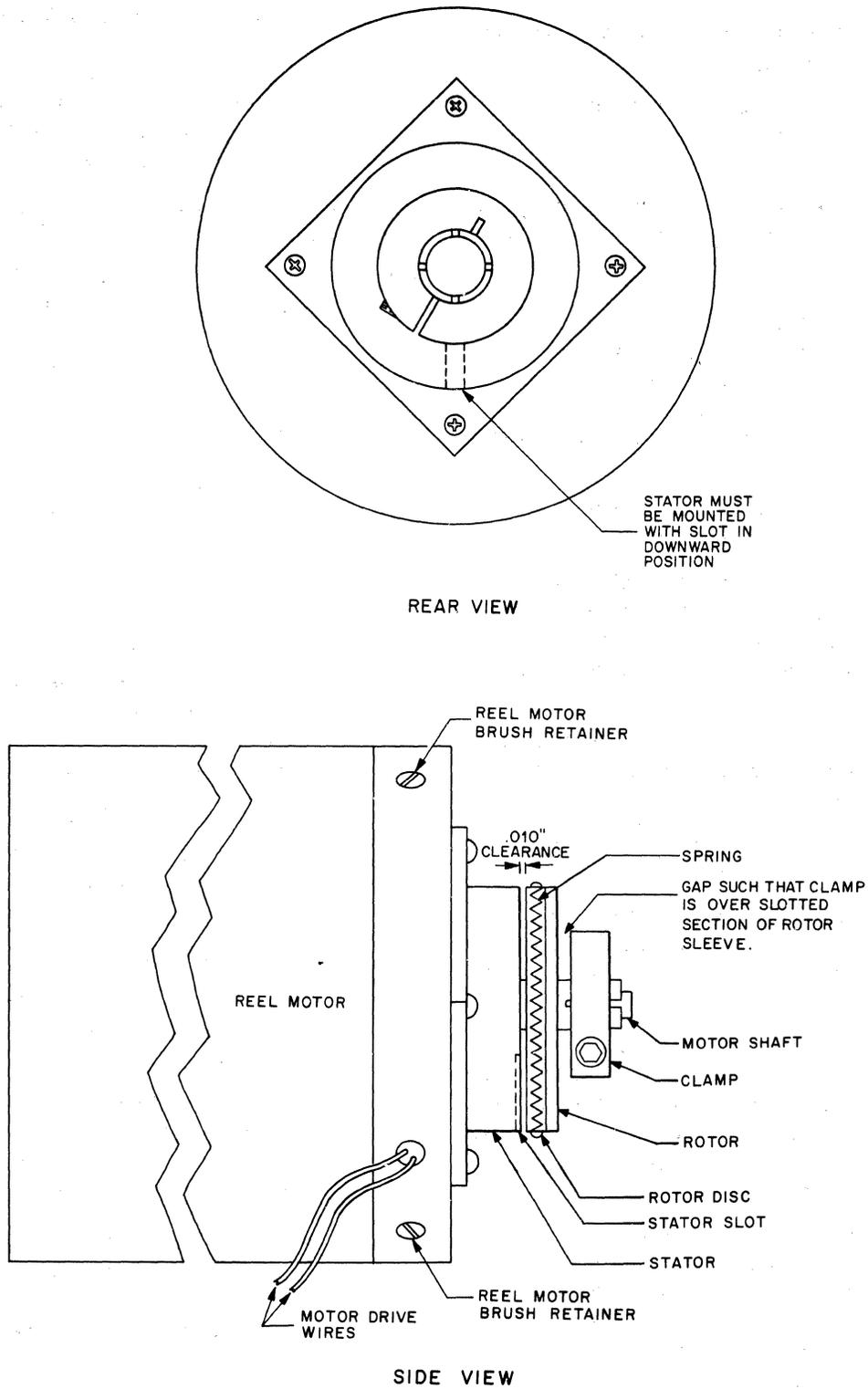
Figure 4-6   Reel Motor Brush Locations and Brake Assembly

4-8
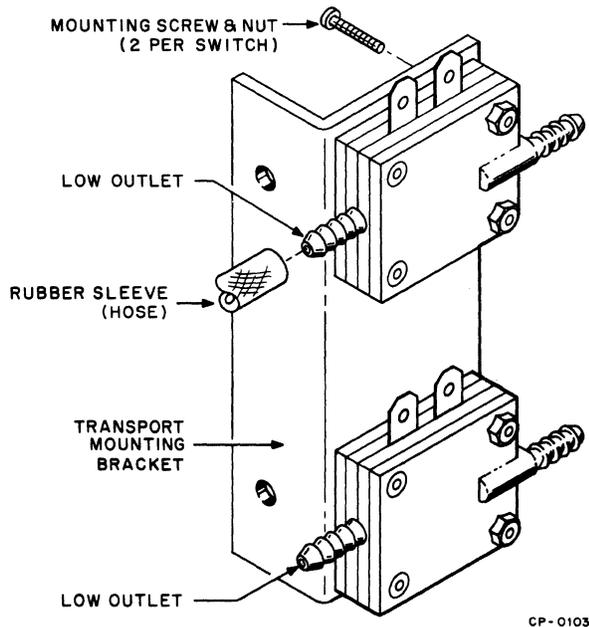
Figure 4-7 Vacuum Switches

Figure 4-8 Rear View of Vacuum Motor Assembly

9. Guide the switch assemblies so each switch sleeve fits snugly into its respective hole in the casting without any lateral strain.

10. Insert and tighten the bracket screws.

11. Operate the transport off-line to verify switch functions.

4.12 VACUUM MOTOR ASSEMBLY

Proceed as follows to remove and/or replace the vacuum motor assembly (Figure 4-8).

1. Remove power from the TU16 Tape Transport.

2. Slide the transport forward on its slides.

3. Unplug P1 through P5 from their sockets on the H606 Power Board.

4. Loosen the three Phillips head screws that secure the H606 Power Board to the framework and carefully remove the H606 Power Board.

5. Remove one screw and two nuts that secure the vacuum motor assembly to the framework.

6. Disconnect the 3-pin Mate-N-Lok jumper located just below the vacuum blower; this is the ac from the TU16 power supply.

7. Remove the entire vacuum motor assembly from the side from which the H606 was removed, being certain to take the short vacuum hose with it.

8. Place the vacuum motor assembly in a convenient location to work in. Remove the vacuum subassembly back cover to expose the belt and pulleys. Refer to Figure 4-9.

9. Remove the Allen set screw from the pulley.

10. Remove the belt, then the pulley.

11. Remove the four Allen screws exposed by removing the pulley, and remove the vacuum motor.

12. To replace the vacuum motor, reverse steps 2 through 11.

NOTE
Refer to the adjustments section (Paragraph 4.18.8) for belt adjusting procedures.

4.13 TU16 POWER SUPPLY REGULATOR BOARD

To remove and/or replace the TU16 power supply regulator board (Figure 4-1), proceed as follows:

4-9
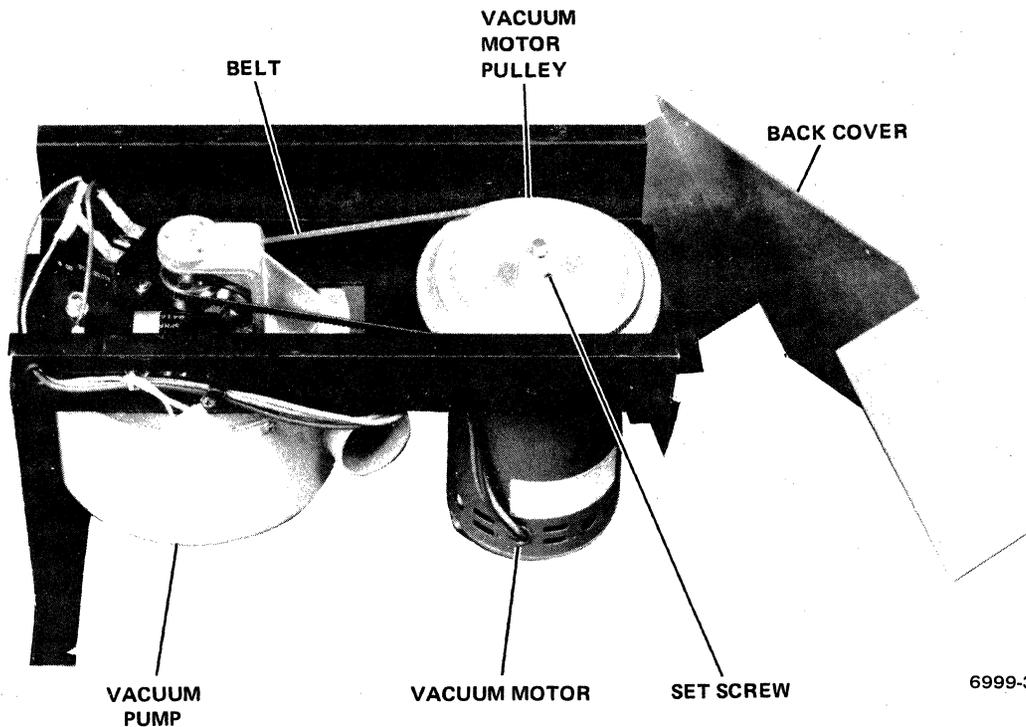
Figure 4-9   Vacuum Assembly

1. Ensure that power to the TU16 is turned off; then unplug the TU16 from its outlet.

2. Approach the TU16 power supply from the rear of the TU16 cabinet.

3. Remove all connectors (J1—J5) from the TU16 power supply board.

4. Remove the regulator board cover.

5. Unplug the three power connections (AC HI, AC LO, and GND) from the bottom left corner of the regulator board.

6. Remove the five Phillips head mounting screws and the single Allen head mounting screw (Figure 3.15-1).

7. Carefully lift the regulator board out of the cabinet.

8. To reinstall the regulator board, perform steps 1—7 in reverse.

CAUTION
When replacing a TU16 power supply regulator board, apply a thin coat of Wakefield No. 128 compound or Dow silicon grease to the diode pack heat sink, and ensure that the Allen head screw is secured very tightly. This provides adequate heat flow, and prevents the diode packs from overheating.

Next to the AC HI, AC LO, and GND connector tabs in the lower left corner of power supply regulator board are three additional tab connectors and two wires. Two of the tabs are marked "115;" the other (central) tab is marked "230." If you are operating from a 115 V source, the two wires are connected to the two outside tabs (marked 115); for 230 V operation, the wires are connected to the two tabs on the central connector (marked 230).

4.14   TU16 TRANSFORMER-CAPACITOR ASSEMBLY (7009636)
The procedure for removing and/or replacing the TU16 transformer-capacitor assembly (Figure 4-1) is:

1. Ensure that power to the TU16 is turned off; then unplug the TU16 from its outlet.

2. If possible, approach the TU16 transformer-capacitor assembly from the rear of the TU16 cabinet. If this is not possible, pull the transport forward on its slides and work from either side.

3. Remove connectors J2 and J3 from the TU16 power supply board.

4. Remove the regulator board cover.

5. Remove the transformer-capacitor assembly cover.

6. Unplug the three power connections (AC HI, AC LO, and GND) from the bottom left corner of the regulator board.

7. Remove the four Phillips head mounting screws that hold the transformer-capacitor assembly.

NOTE
Do not remove the two Phillips head screws that hold the transformer-capacitor assembly bracket.

8. Carefully lift the transformer-capacitor assembly out of the cabinet.

9. To reinstall the transformer-capacitor assembly reverse steps 1 through 8.

4.15 TM02 POWER SUPPLY (H740D)
To remove and/or replace the TM02 power supply, proceed as follows:

1. Ensure that the power to the TU16/TM02 unit is turned off; then unplug the unit from its wall outlet.

2. Disconnect the BC05H input box from the TM02 power supply.

3. Access to the TM02 power supply assembly is gained from the rear of the TU16/TM02 cabinet; the supply is positioned across the back of the cabinet.

4. Unplug the two Mate-N-Lok connectors.

5. Remove the four screws that secure the power supply assembly to the cabinet. Hold the supply so that it does not fall.

6. Move the power supply assembly to a convenient location to work.

7. Locate and remove the three screws that secure the cover to the power supply assembly.

8. Locate and remove the four screws on the bottom of the power supply assembly.

9. Unplug the internal ac harness, and then lift the power supply from the container.

10. To replace the power supply, reverse steps 2 through 9.

For instructions on removal and replacement of the TM02 power supply subassemblies, refer to the *H740D Power Supply Maintenance Manual* (DEC-11-H740A-A-D).

4.16 CAPSTAN, CAPSTAN MOTOR, ROLLER GUIDES, HEAD PLATE ASSEMBLY
The capstan, capstan motor, roller guides and head plate directly effect the path of the tape as it moves through the tape transport. If any one of these items requires replacement, an entire tape path alignment is necessary. Refer to Paragraph 4.17 for tape path alignment and for the conditions which require a tape path alignment.

4.17 TAPE PATH ALIGNMENT

4.17.1 When to Perform a Tape Path Alignment

A. When a capstan, capstan motor, roller guides or head plate is replaced.

B. When forward and/or reverse skew is found to exceed specifications (quarterly PM items 13 and 14 in Chapter 5).

C. When an amplitude difference of more than 10% is seen between forward and reverse read amp output.

D. When a visible change in the tape's path across the capstan is apparent when changing from forward to reverse tape motion.

E. When measurement of reference edge of Track 1 of a developed (with magna-see solution) tape shows a result different from 0.007" (±0.003"). See Semiannual PM items 3 and 4 in Chapter 5.

F. When TU16 Data Reliability diagnostic shows a "Read Reverse" error rate which exceeds specification in Monthly PM items 4 and 5 in Chapter 5.

G. When, after performing tape speed adjustment (items 9 and 10) and mechanical skew adjustment (items 13 and 14) under quarterly Preventive Maintenance; and performing capstan ramp adjustment (items 1 and 2) and read amplitude adjustment (item 6) under semiannual Preventive Main-

tenance, and running all TJU16 diagnostics, you are still suffering from incompatibility with other tape transports.

4.17.2 Objectives

A. To establish a single plane for tape to travel from supply reel to take-up reel, independent of the capstan and fixed guides (part of the head plate assembly). This is accomplished by aligning reel hubs and roller guides.

B. To mount the head plate in the plane established in A. This is accomplished by establishing the relationship between the reference surfaces used in A and the surface onto which the head plate is to be mounted. If this relationship is nominal, the head plate is simply mounted. If the relationship is not nominal, appropriate shims are placed underneath the head plate so as to bring the reference edges of the fixed guides into the proper plane.

C. To minimize the amount of distortion to the tape as it travels through the plane established in A and B. This is accomplished by shimming the capstan motor in such a way that the capstan motor shaft becomes perpendicular to the tape path.

NOTE

The effect of accomplishing A, B, and C is to minimize static skew, dynamic skew and tracking error in both forward and reverse directions. Skew is the total amount of non-perpendicularity of characters written on tape. Tracking is defined by ANSI standard as the measurements from the reference edge to each track center line. Improper tracking takes two forms:

(1) Read - **A tape transport that is tracking incorrectly will not have its read head elements centered over tracks correctly written by another tape transport.**

(2) Write - **A tape transport tracking incorrectly will write tracks of data that are not correctly spaced from the reference edge of the tape. Therefore, a transport with proper tracking alignment would not have its read head elements centered on the incorrectly written tracks.**

4.17.3 Tools Required for Tape Path Alignment

The following tools are required to perform a tape path alignment.

1.	Skew Tape (800BPI) 1200 ft.	29-19224
	or 600 ft.	29-22020
2.	Reel Hub Tool	29-18611
3.	Roller Guide Tool	29-18607
4.	Microscope	29-20273
5.	Magna-see	29-16871
6.	Penlight	
7.	Alignment Doors	74-13969
8.	Depth Micrometer	29-22039
9.	Shim stock .001	48-50023-01
	.002 (red)	-03
	.003 (green)	-04
	.004 (tan)	-05
	.005 (blue)	-06
	.0075 (transparent)	-07
	.010 (brown)	-08

4.17.4 Alignment Procedure

4.17.4.1 Establishing Basic Plane for Tape Path —
The following 8 steps will establish the basic tape path plane.

1. Remove supply reel and take-up reel.

2. Use Reel HUB Alignment tool to check alignment of both reel hubs. You should feel a small amount of friction when sliding tool in and out between alignment boss and reel hub. You should not be able to move tool back and forth between hub and alignment boss. (See Figure 4-10.) Loosen Allen screws and adjust hub if necessary.

3. Rotate hub, checking fit of alignment tool at several intervals. You will probably find some high and low spots but tool should not bind hard or become loose when moving tool toward and away from the casting. Replace hub and/or motor if either of these conditions exist.

4. Remove upper roller guide ramp. See Figure 4-11 for location of roller guides.

5. Slide roller guide alignment tool underneath upper roller guide (Figure 4-12A). You should feel a small amount of friction as you slide tool back and forth under roller

7660-3

Figure 4-10a   Reel Hub Adjustment, Front View

TOP
OF
TRANSPORT

REEL HUB ALIGNMENT
GAUGE #29-18611
(Should feel friction
in vertical (⬍) axis.
Gauge should not move
in horizontal (↔) axis.)

HUB LOCKING SCREW
ACCESS OPENING

REEL HUB ALLEN
LOCKING SCREWS (2)

MACHINED
ALIGNMENT
BOSS

TEFLON WASHER

3/16 INCH KEY

REEL MOTOR
DRIVE SHAFT

REEL HUB ASSEMBLY

FRONT OF
TRANSPORT

CP-0104

Figure 4-10b   Reel Hub Adjustment, Side View

4-13

guide. Loosen clamp on back side of casting and adjust roller guide if necessary. See Figure 4-12C.

6. Slide one side of roller guide alignment tool under lower roller guide (Figure 4-12B). You should feel slight amount of friction as you move tool back and forth. Adjust if necessary.

7. Load a scratch tape. Run tape forward for 5 seconds.

   a. Ensure that tape is not touching either side of supply or take-up reel while tape is moving.

   b. Look for tape puckering against either column floor or door glass at both upper and lower roller guides.

If either of these conditions exist, re-check the associated roller guide and reel hub adjustments.

8. Dismount tape. Re-install upper roller guide ramp.

CAUTION
When installing ramp, it is necessary to push down on right side of ramp while tightening screw. Otherwise, it is possible that the ramp will be touching tape.

4.17.4.2 Mounting Head Plate in Plane of Tape Path — The following six steps cover the removal of the head plate assembly and the replacement of the assembly into the plane of the tape path.

1. Remove head plate cover.

2. Disconnect Write, Read and Erase head cables from head.

3. Loosen the three shoulder screws and remove head assembly.
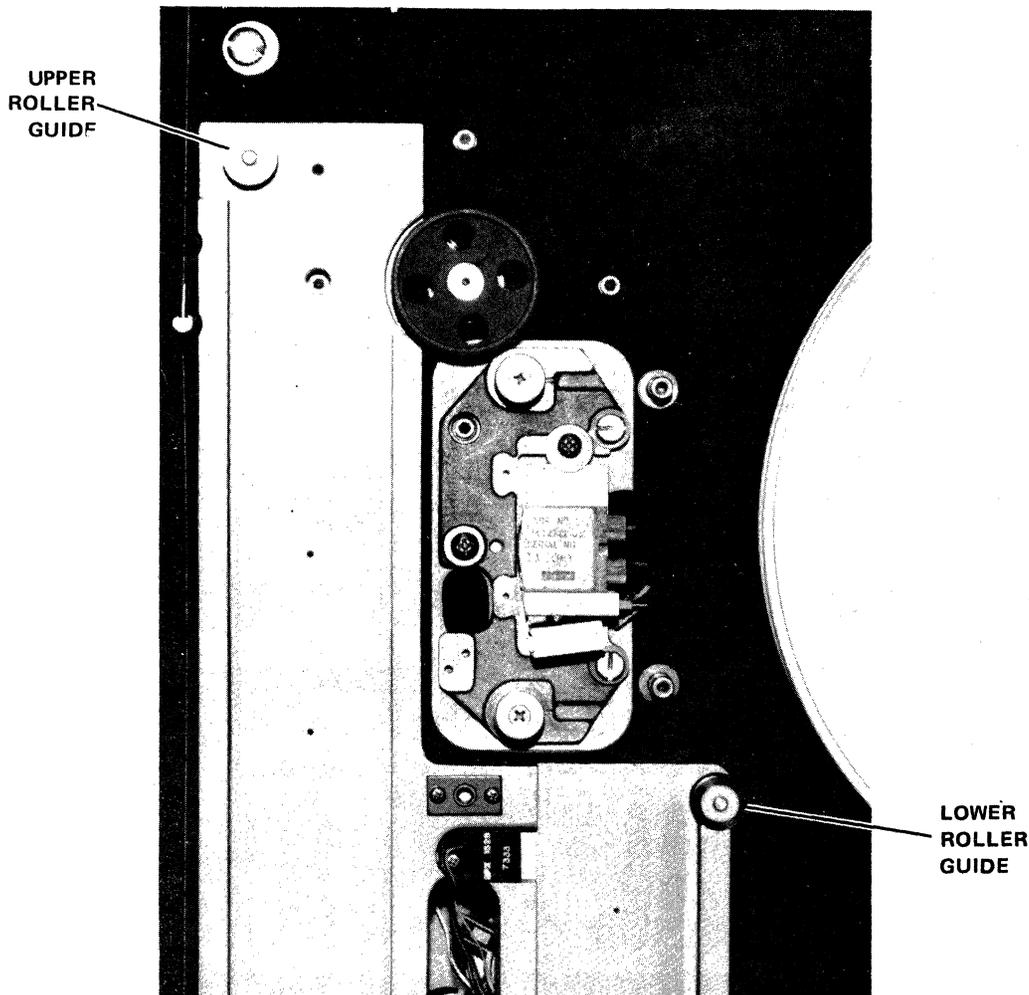
7660-12

Figure 4-11   Location of Upper and Lower Roller Guides

4-14
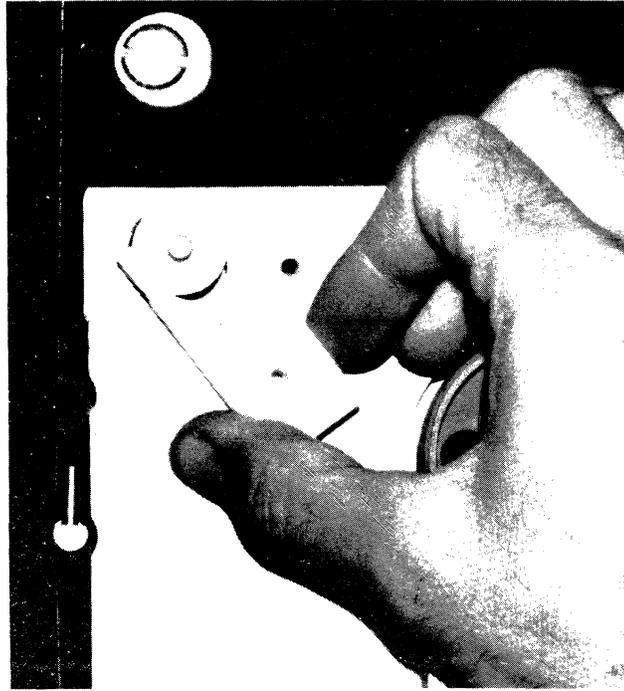
7660-1

Figure 4-12a   Roller Guide Adjustment, Upper Roller Guide Adjustment
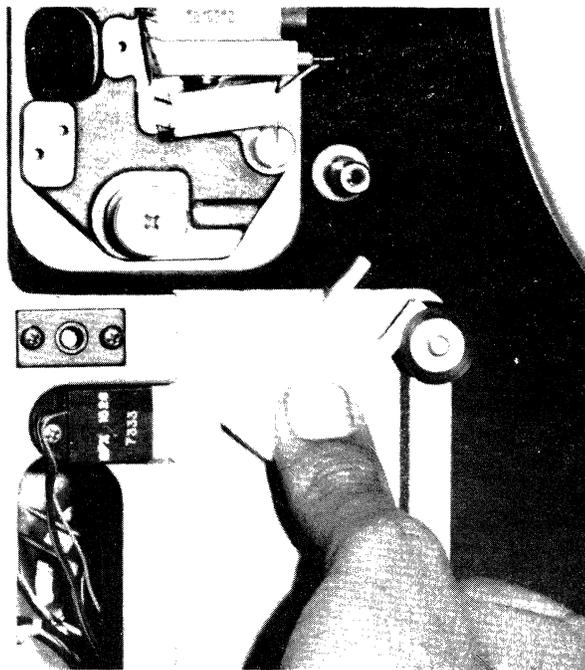
7660-5

Figure 4-12b   Roller Guide Adjustments, Lower Roller Guide Adjustment

FRONT OF
TRANSPORT

TAPE ROLLER
GUIDE ALIGNMENT
GAUGE # 29-18607

TAPE GUIDE ROLLER

ROLLER SHAFT
LOCK CLAMP

6 X 32 X 1/2" ALLEN
CLAMP LOCK SCREW

EXERT PRESSURE
AT THIS POINT
DURING ALIGNMENT

TAPE GUIDE
ROLLER SHAFT

CLAMP
MOUNTING
SCREW

CP-0105
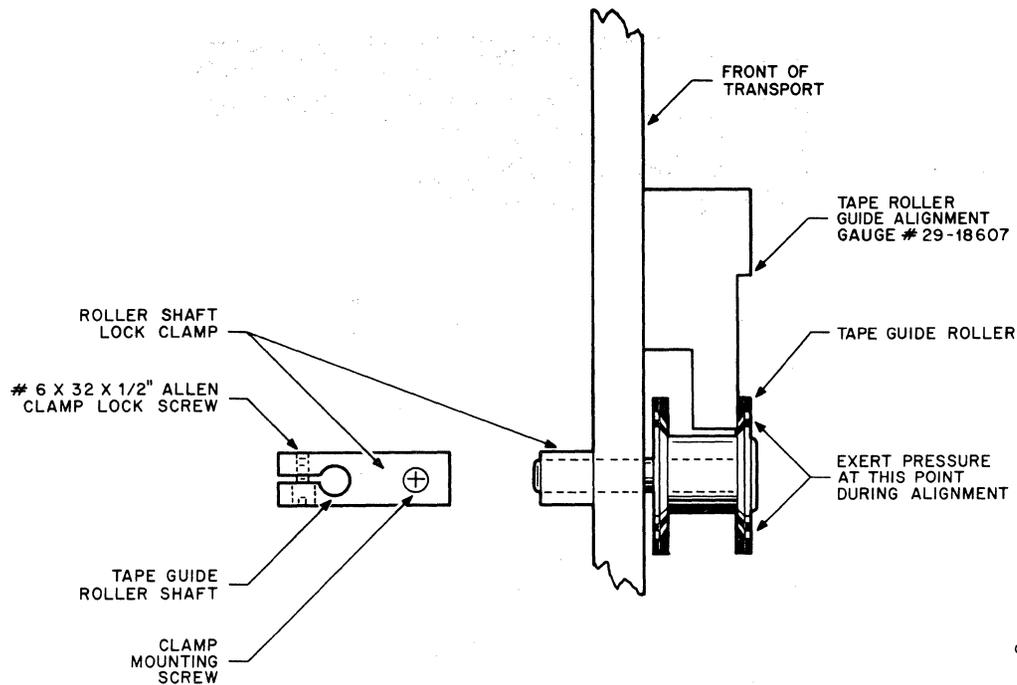
Figure 4-12c   Roller Guide Adjustments, Side View of Roller Guide
Tool Insertion

4. Using a depth micrometer, measure depth
from outer surface of left vacuum column
to surface onto which head plate was
mounted. (See Figure 4-13.) Nominal value
is 1.120 inches. Call this value "HMS".

NOTE
**You may find this measurement diffi-
cult to make since you can only seat one
side of the micrometer on the vacuum
column surface. It is, therefore, ad-
vised that you:**

(1) **Place the micrometer base at a 45
degree angle with the vacuum
column surface thereby giving
greater seating area for the micro-
meter (Figure 4-13A).**

(2) **Make the measurement with the
micrometer shaft as close as pos-
sible to the vacuum column wall
thereby giving greater leverage to
keep the micrometer base seated
and less distance to project errors.**

(3) **Repeat the measurement several
times to verify results.**

5. Subtract 1.120 from HMS (HMS-1.120).

6a* If result obtained in step 5 is zero or negative,
mount head plate without shims.

6b* If result obtained in step 5 is positive, cut 3
horseshoe-shaped shims** of the value ob-
tained in step 5 and place one around each of
the three mounting screws when mounting
head plate (shims go between head plate and
mounting surface). See Paragraph 4.17.3
for shim color code. Also, cut a shim of the
same value to surround the vacuum port
which goes to the tape cleaner to prevent air
leakage. (See Figure 4-14.)

*If a new head assembly is mounted, electrical write deskew will
have to be performed. This should be done after the read mechani-
cal skew adjustment (quarterly PM items 13 and 14 in Chapter 5).

**Another method is to paper punch some one-inch square shim
stock and use the punched holes for the mounting screws and the
vacuum port.

DEPTH
MICROMETER

HEAD PLATE
MOUNTING
SURFACE

LEFT VACUUM
COLUMN
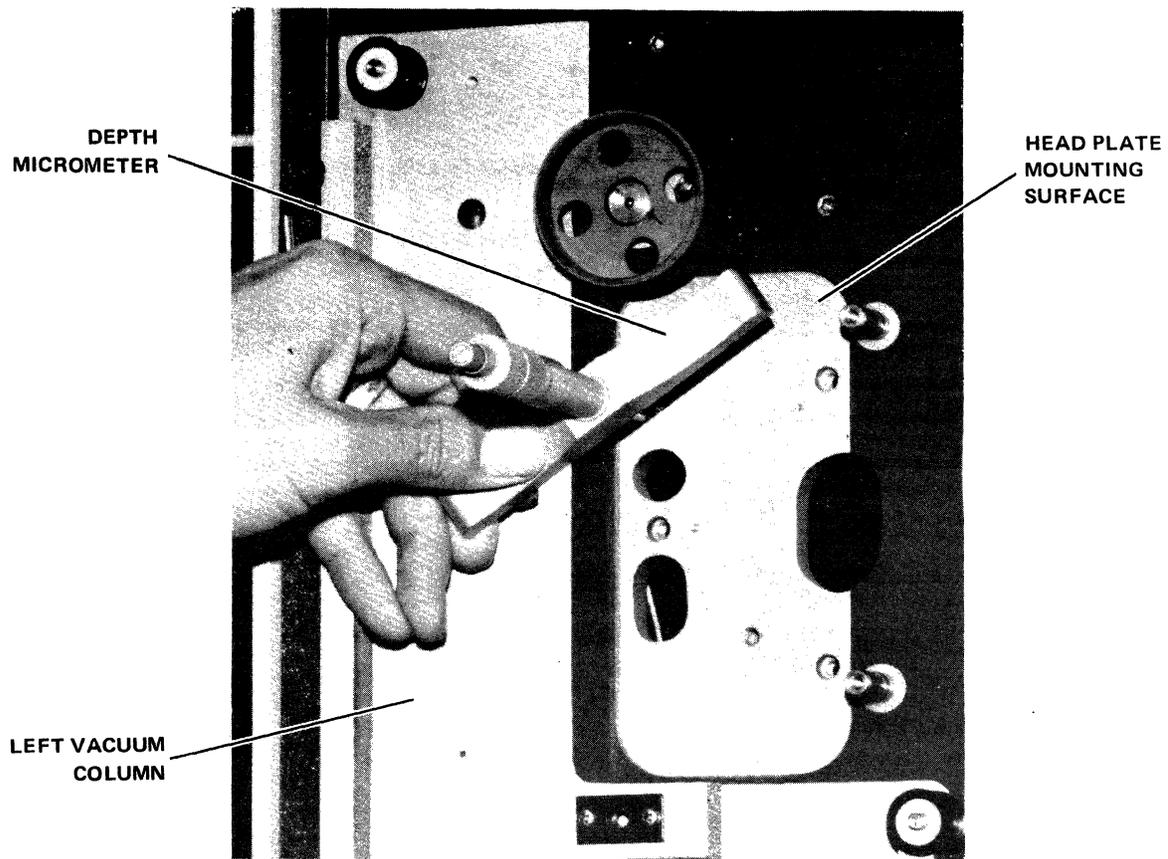
7660-18

Figure 4-13a   Measurement of Head Plate Mounting Surface (HMS), Placement of
Depth Micrometer

DEPTH
MICROMETER

LEFT
VACUUM
COLUMN

HMS

HEAD PLATE
MOUNTING
SURFACE
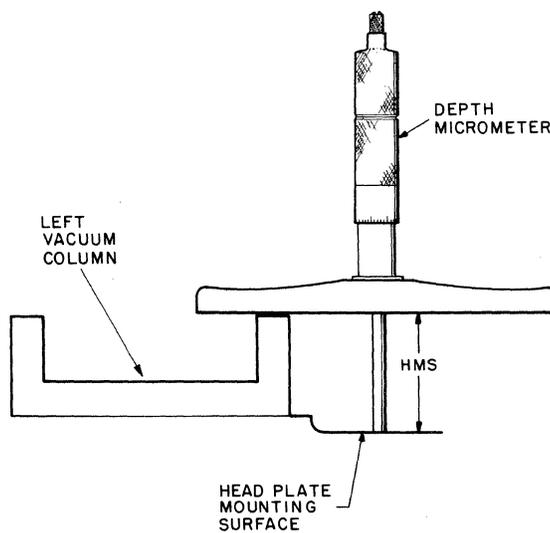
CP-1991

Figure 4-13b   Measurement of Head Plate Mounting Surface (HMS), Bottom View of
HMS Measurement

4-17

HOLES FOR MOUNTING
SCREWS (3)

VACUUM PORT
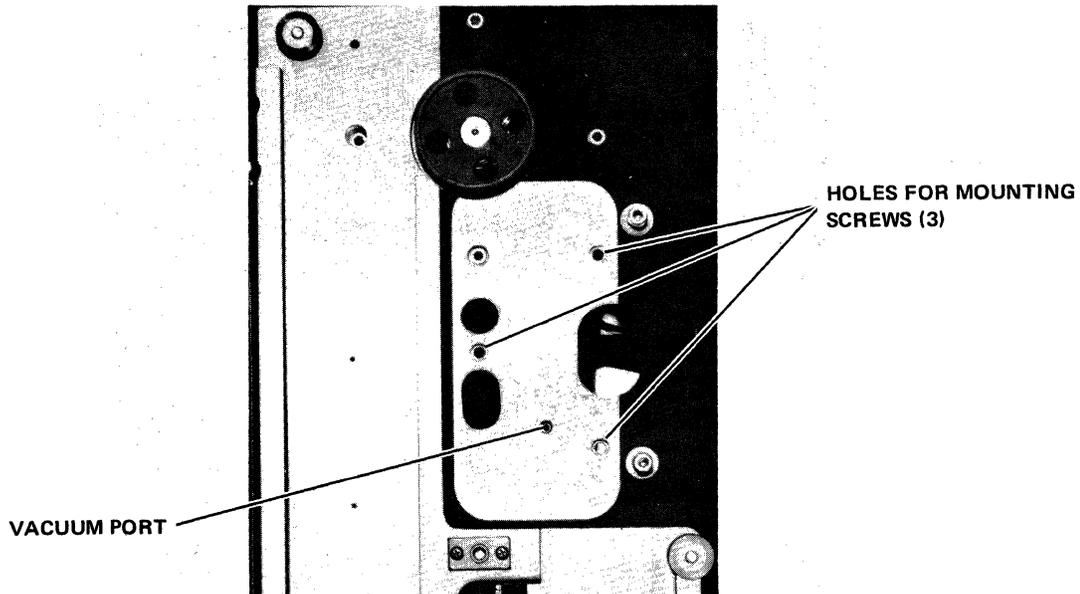
7660-20

Figure 4-14   Location of Shims Under Head Plate Assembly

SUPPLY REEL · LOWER ROLLER GUIDE · RIGHT VACUUM COLUMN · LEFT VACUUM COLUMN · UPPER ROLLER GUIDE · TAKE-UP REEL · MACHINED BOSS · MACHINED BOSS · MACHINED REFERENCE SURFACES
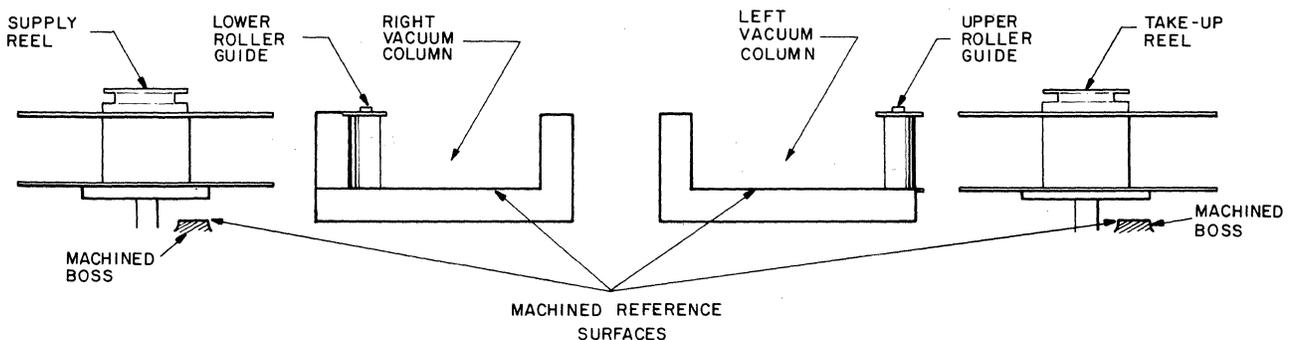
CP-1993

Figure 4-15   Machined References Used to Establish Tape Path Plane

4.17.4.3   Summary of Accomplishments Thus Far

A.   Paragraph 4.17.4.1 set reel hubs and roller guides in the same plane as the vacuum columns (Figure 4-15).

B.   Paragraph 4.17.4.2 set the reference edge of the fixed guides into the plane of the tape coming out of the vacuum columns (Figure 4-16).

C.   Paragraph 4.17.4.4 will set the shaft of the capstan motor perpendicular to the tape path so as to minimize distortion of the plane established in A & B above.

4.17.4.4   Making Capstan Motor Shaft Perpendicular to Tape Path — Steps 1 through 20 will insure that the capstan motor shaft is perpendicular to the tape path. There are two conditions that can cause non-perpendicularity of the motor shaft to the tape path. One is the capstan motor shaft not being perpendicular to the mounting face of the motor. Figures 4-17A and 4-17C are examples of this condition. (Specifications allow 0.005 inches of non-perpendicularity of the motor shaft.) The other condition is non-parallelism between the motor mounting surface on the back of the casting and the front surface of the casting. Figure 4-17B illustrates this situation. (Specifications allow 0.004 inches of non-parallelism between the machined surfaces on the front and back of the casting.

4-18
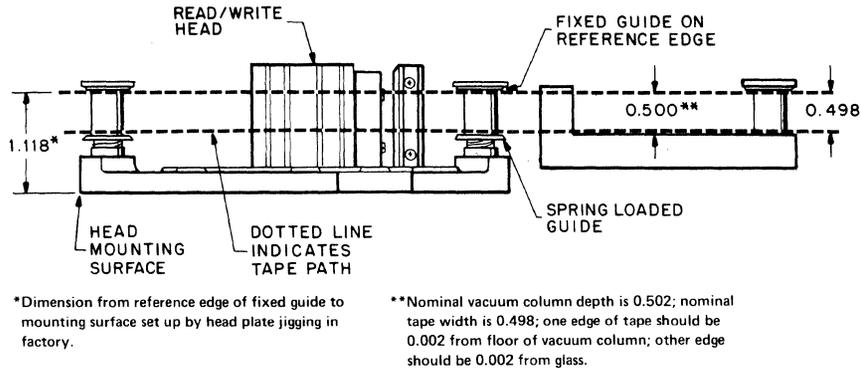
Figure 4-16   Head Plate Assembly Mounted in the Plane of the Tape Path

READ/WRITE HEAD

FIXED GUIDE ON REFERENCE EDGE

0.500**   0.498

1.118*

SPRING LOADED GUIDE

HEAD MOUNTING SURFACE

DOTTED LINE INDICATES TAPE PATH

*Dimension from reference edge of fixed guide to mounting surface set up by head plate jigging in factory.

**Nominal vacuum column depth is 0.502; nominal tape width is 0.498; one edge of tape should be 0.002 from floor of vacuum column; other edge should be 0.002 from glass.

CP-1983

CP-1994

Figure 4-17a   Examples of Capstan Non-Perpendicularity, Side View - Capstan Motor Shaft Pointing Down due to Non-Perpendicularity of Shaft
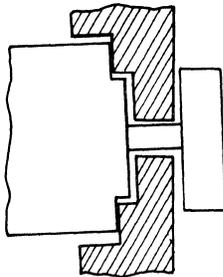
CP-1995

Figure 4-17b   Examples of Capstan Non-Perpendicularity, Side View - Capstan Motor Shaft Pointing Up due to Non-Parallelism of Machines Motor Mounting Surface
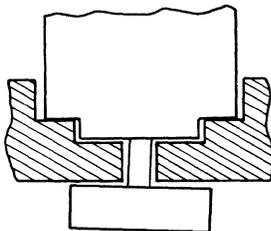
CP-1996

Figure 4-17c   Examples of Capstan Non-Perpendicularity, Top View - Capstan Tipped Toward Casting on Left Side and Away from Casting on Right Side due to Non-Perpendicularity of Motor Shaft

The effect of the capstan motor shaft not being perpendicular to the tape path will depend on the direction of the non-perpendicularity; i.e., whether the motor shaft is pointing up, down, toward the left or toward the right. When the shaft is pointing down (Figure 4-17A) the top of the capstan is away from the casting causing the tape to track away from the casting. Hard guiding will occur on the vacuum door glass and the fixed guides in both forward and reverse directions. When the shaft is pointing up (Figure 4-17B) the bottom of the capstan is away from the casting causing the tape to track toward the casting. Hard guiding will occur on the vacuum column floor and the spring loaded guides in both forward and reverse directions. When the shaft is pointing toward the left (Figure 4-17C) the tape will track away from the casting in the forward direction and toward the casting in the reverse direction. If the shaft were pointing toward the right the opposite would be true; i.e., the tape would track toward the casting in the forward direction and away from the casting in the reverse direction.

Figure 4-28 is a flowchart of capstan alignment and summarizes the twenty steps of the alignment procedure.

1.   Remove the capstan by loosening the capstan locking clamp with an Allen wrench and remove the capstan and clamp.

NOTE

If the capstan is hard to remove, it may be bent and should be replaced. The inside of the capstan should be checked for burrs in the area of the slots. The end of the capstan motor shaft should be checked for burrs also. See Figure 4-18.

4-19

CP-1987
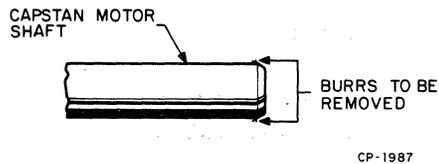
Figure 4-18   Location of Possible Capstan Burrs

2. Remove the capstan motor by unplugging P1 from the H606 Power Board and removing the 4 bolts holding the capstan motor on the casting.

CAUTION

Because the bolt heads are in front of the casting and the motor is on the rear, caution should be used so that the motor does not fall when the screws are removed.

DO NOT ATTEMPT to remove the tachometer portion of the motor; the two are replaced as an assembly.

3. Check the capstan motor and casting for the following:

   • The capstan motor specification template does not interfere with the motor mounting on the casting. If there is interference, remove the template.

   • The motor does not have any burrs on the mounting surface that would prevent it from mounting squarely on the casting.

   • Insure the mounting surface of both the motor and casting are free of dirt, gummy substances and burrs pushed up by machining operations.

4. Lift up and remove the vacuum column door.

5. Measure the depth from the outer surface of the left vacuum column to floor of left vacuum column. Nominal depth = 0.502 inches. Call this value "LVC". See Figure 4-19.

6. Subtract 0.500 from LVC and call the resulting value "X" (X=LVC-0.500). Record the value "X" as it will be used in Step 16.

NOTE

"X" should be the distance from the inside edge of the tape to the floor of the left vacuum column when the outside edge is 0.002 inches from the outer sur-

face of the left vacuum column. (See Figure 4-16). If the capstan motor shaft is perpendicular to the tape path and if Paragraphs 4.17.4.1 and 4.17.4.2 were performed correctly, "X" will be equal to this distance.

7. Remount the capstan motor on the casting (4 bolts). Tighten the mounting bolts.

8. Clean the capstan with a water-dampened Kim-wipe or lint-free cloth. Do not use any cleaner other than water on capstan.

9. Reposition the capstan on the capstan motor shaft. Tighten the clamp.

10. Load a good quality tape using the alignment glass (Figure 4-20). It will be necessary to hold the alignment glass with one hand while pressing the LOAD switch with the other (see Figure 4-21).
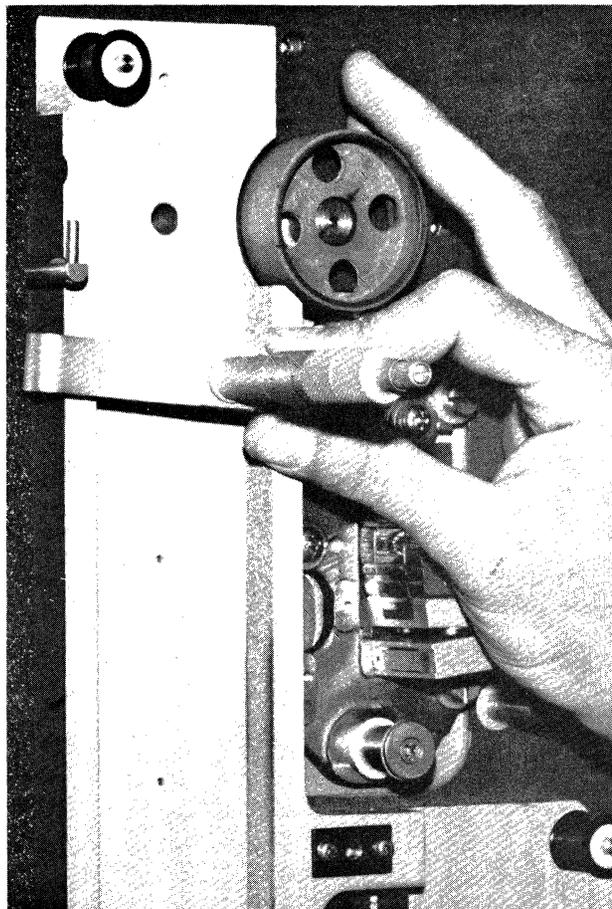
7660-11

Figure 4-19a   Measuring Depth of Left Vacuum Column (LVC), Placement of Depth Micrometer
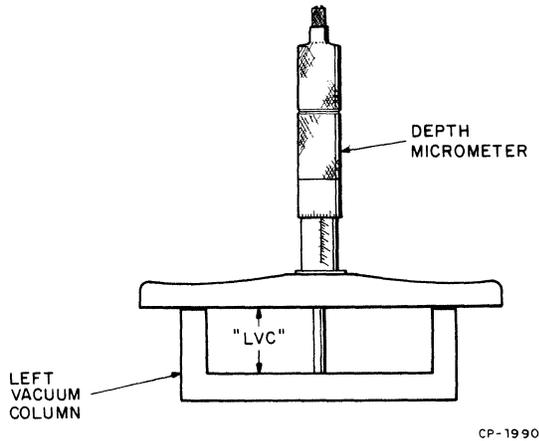
Figure 4-19b   Measuring Depth of Left Vacuum
Column (LVC), Top View of LVC
Measurement

11. Insure the tape rides in the center of the capstan. This can be done by running the tape forward several feet and eyeballing the tape position on the capstan. The capstan can be moved in or out to insure the tape is in the middle of the capstan. The capstan alignment tool 29-18609 can be used for course adjustment (Figure 4-22). Install the capstan clamp over the slotted portion of the capstan lock ring to insure that the capstan is clamped securely to the capstan motor shaft.

12. Alignment of the capstan motor shaft, making it perpendicular to the tape path, can now begin. The alignment is done by placing shims between the capstan motor mounting face and the casting surface onto which the capstan motor is mounted. Shims may be placed in one of two coordinates to correct for any mis-alignment which exists. They may be placed in quadrant II or in quadrant IV but not in both (see Figure 4-23).

A few notes of caution will assist in doing the procedure; in the shortest possible time.

a) The sequence of tightening the bolts on the capstan motor is important. Each time the bolts are tightened in a particular procedure they must be tightened in the same order. This allows the procedure to be repeated while keeping the motor in the exact same position.

b) The use of sharp scissors on the plastic shim stock is necessary to keep the edges from curling up. The plastic shim stock sizes are identifiable by the color coding as follows.

Red   -.002"
Green   -.003"
Tan   -.004"
Blue   -.005"
Transparent -.0075"
Brown   -.010"

c) The use of a good quality tape is necessary for correct capstan alignment. A
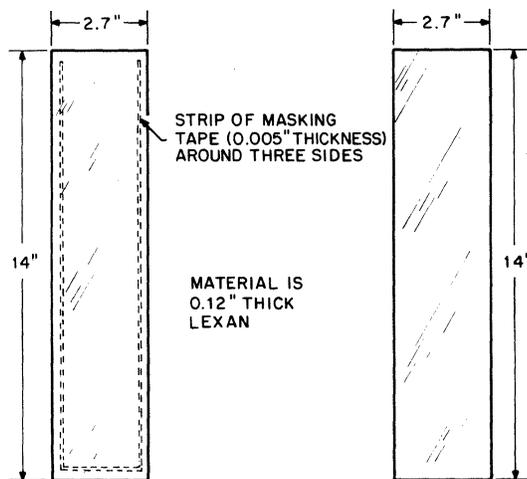
Figure 4-20a   Alignment Glass, Left Column Glass

Figure 4-20b   Alignment Glass, Right Column Glass

LEFT COLUMN GLASS

TAPE

RIGHT COLUMN GLASS
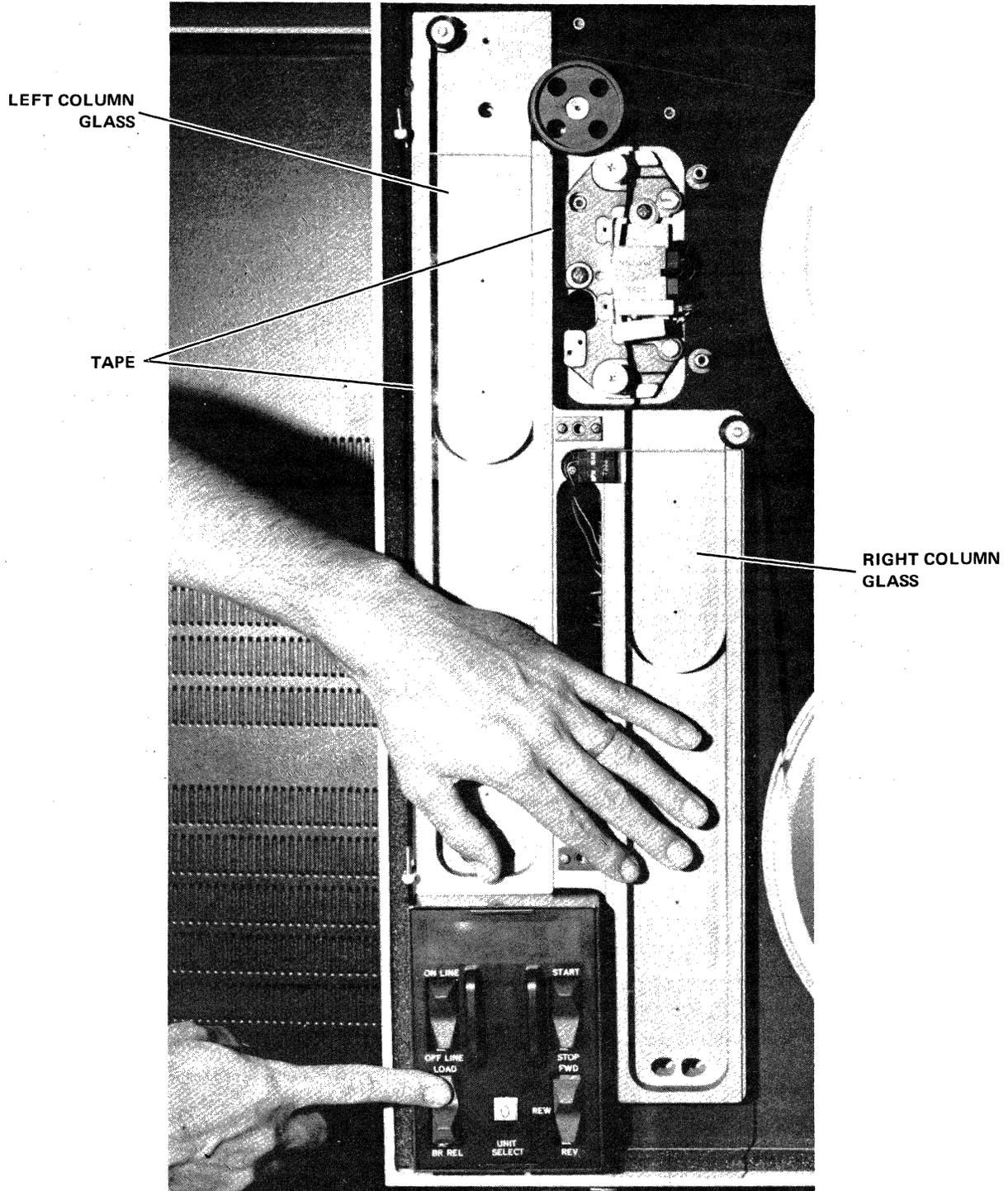
7660-17

Figure 4-21 Using Alignment Glass to Load Tape
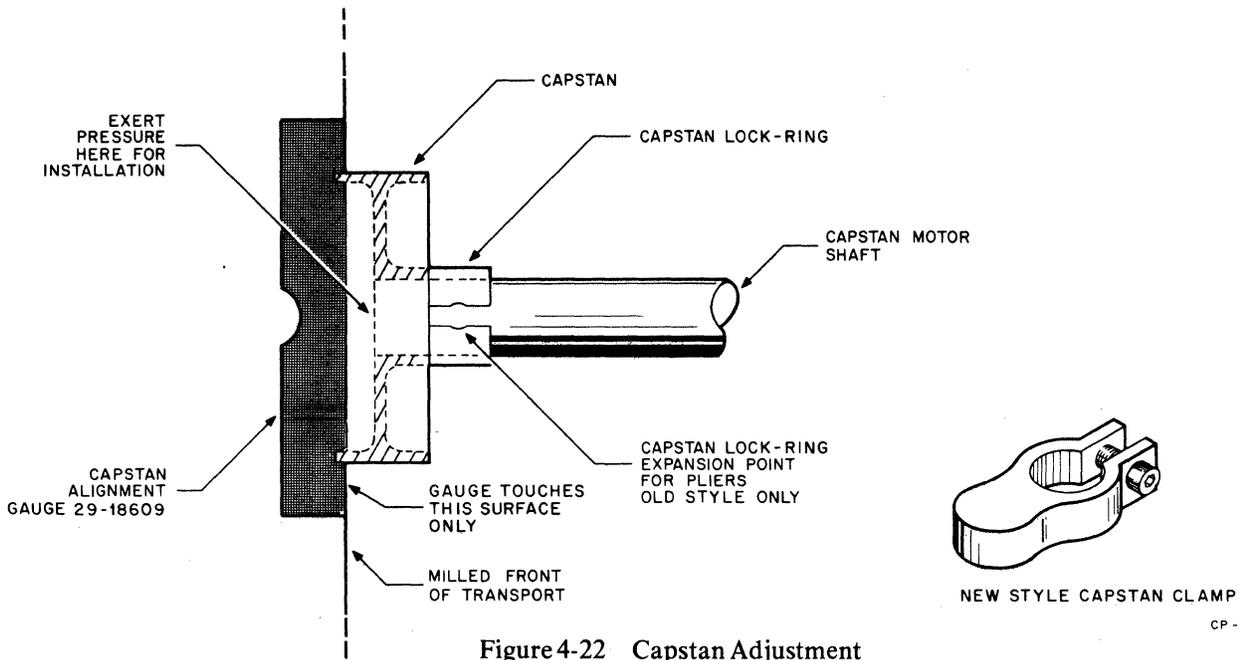
Figure 4-22   Capstan Adjustment

CAPSTAN

CAPSTAN LOCK-RING

CAPSTAN MOTOR
SHAFT

EXERT
PRESSURE
HERE FOR
INSTALLATION

CAPSTAN LOCK-RING
EXPANSION POINT
FOR PLIERS
OLD STYLE ONLY

CAPSTAN
ALIGNMENT
GAUGE 29-18609

GAUGE TOUCHES
THIS SURFACE
ONLY

MILLED FRONT
OF TRANSPORT

NEW STYLE CAPSTAN CLAMP

CP - 0108

SHIM

DECK
PLATE

CAPSTAN
MOTOR

CAPSTAN

NOTE:
Shim may be placed in quadrant II
or quadrant IV but not in both.

MOUNTING
SCREWS

45°

SHIM

0.5

II   I

A

B   D

III   IV

45°

C

CP-1992

Figure 4-23a   Capstan Motor Shim Placement, Side
View

Figure 4-23b   Capstan Motor Shim Placement, Front
View

used or abused tape will not run true
over the capstan causing false readings
during the capstan alignment pro-
cedure.

13.   Cut one piece of each type of shim stock as
indicated in Figure 4-24. The exact dimen-
sions of the shim stock aren't critical. The
main consideration is to have a manageable
size to use as a feeler gauge. The blunt point
shown in Figure 4-24 will minimize curling
of the end while making measurements.

14.   Run tape forward from BOT for 5 seconds.

15.   Using shim stock and penlight, determine
the spacing (Y) between the inside edge of
the tape and the floor of the left vacuum
column. See Figure 4-25. The method of
measuring space Y is shown in Figure 4-26
and described in a, b, and c below:

a)   Slide shim stock underneath inside
edge of tape at slot between top of left
column and capstan.

b)   Shine light onto full width of tape, while
moving shim stock back and forth; look
for puckering.

c) Measurement has been obtained when you select a piece of shim stock which causes small amount of friction when sliding back and forth; yet no visible pucker.

16. Value "Y" (obtained in step 15) must be equal to value "X" (obtained in step 6). Tolerances for value "Y" are plus one thousandth minus zero (Y = X, +0.001, -0.000).

a. If Y=X, +0.001, -.000; go to Step 18.

b. If Y is more than 0.006 greater than X, place a 0.0075 shim in Quadrant II, then go to Step 17.
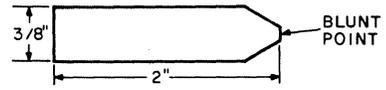
Figure 4-24   Capstan Motor Shim
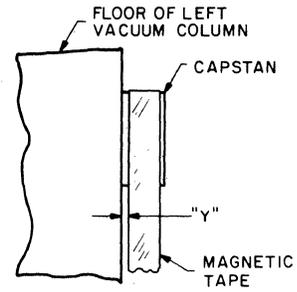
Figure 4-25   Gap (Y) from Tape to Floor of Left Column
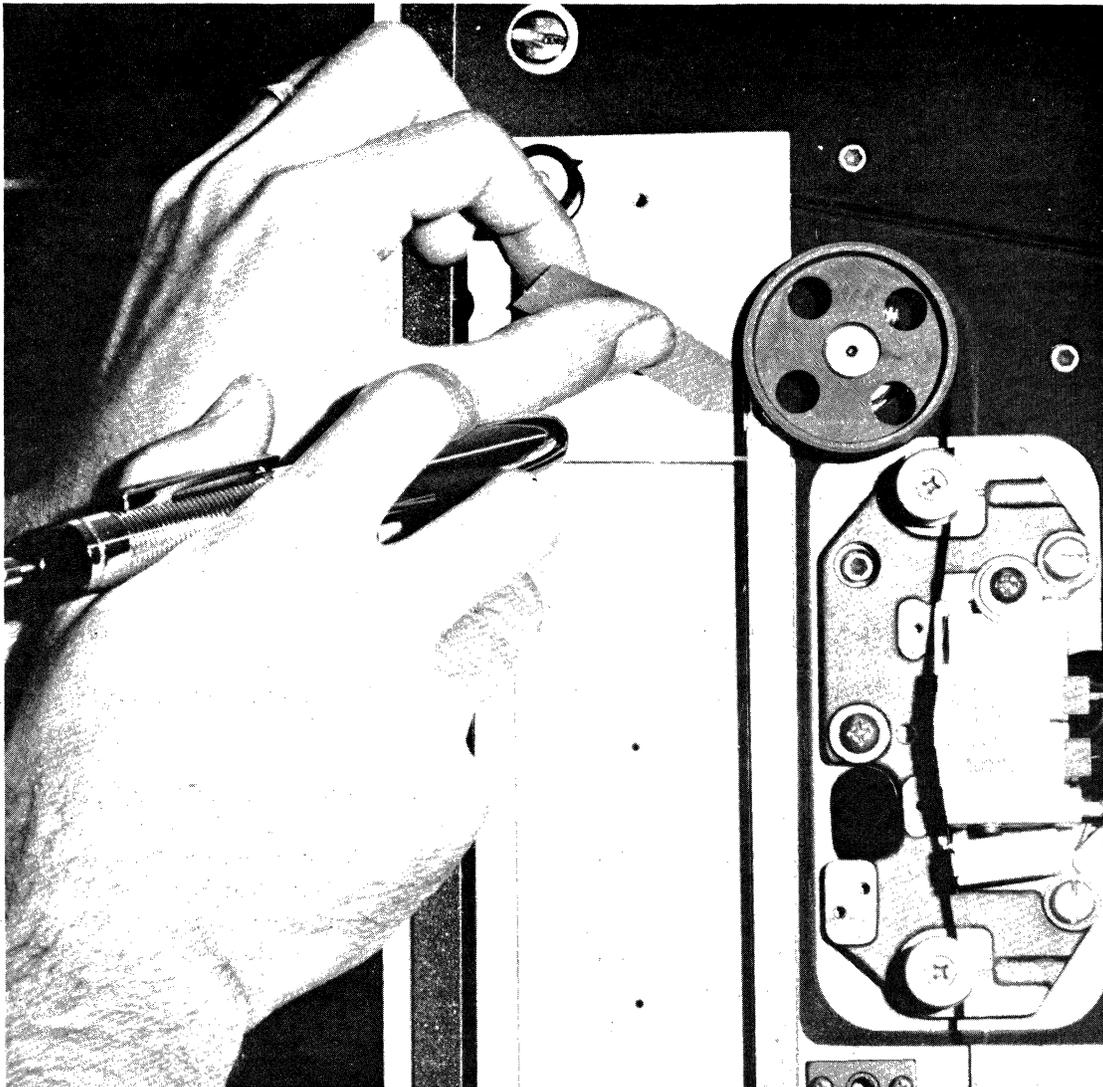
Figure 4-26   Measurement of Tape Gap (Y) with Penlight and Shim

4-24

c. If Y=0 (tape touching casting surface), place a 0.0075 in Quadrant IV, then go to step 17.

d. For any case not covered by step a, b, or c; go to Step 17.

17. Run tape forward for 5 seconds. Measure tape to column spacing to obtain value "Y".

a. If Y=X,+0.001, -0.000; go to Step 18.

b. If Y is more than 0.001 greater than X, with shim in Quadrant IV, decrease shim value in Quadrant IV to obtain Y = X, +0.001, -0.000 (amount of decrease should be approximately Y-X). Repeat Step 17.

c. If Y is more than 0.001 greater than X with 0.0075 shim in Quadrant II, rotate motor mounting 90° clockwise and go back to Step 14. (See note in Step 18.)

d. If Y is more than 0.001 greater than X with no shim installed, shim Quadrant II to obtain Y = X, +0.001, -0.000 (shim value should be approximately Y-X). Repeat Step 17.

e. If Y is more than 0.001 greater than X with a shim in Quadrant II less than 0.0075, increase shim value to obtain Y = X, +0.001, -0.000. The amount of increase should be approximately Y-X. Repeat Step 17 if the new shim value does not exceed 0.0075. If the new shim value exceeds 0.0075, rotate the motor mounting 90° clockwise and go back to Step 14. (See note in Step 18.)

f. If Y is less than X, with shim in Quadrant II, decrease shim value in Quadrant II to obtain Y = X, +0.001 -0.000 (Amount of decrease should be approximately X-Y). Repeat Step 17.

g. If Y is less than X, with 0.0075 shim in Quadrant IV, rotate motor mounting 90° clockwise and go back to Step 14. (See note in Step 18.)

h. If Y is less than X with no shim installed, shim Quadrant IV to obtain Y = X, +0.001 (Shim value should be approximately X-Y). Repeat Step 17.

i. If Y is less than X with a shim in Quadrant IV less than 0.0075, increase shim value to obtain Y = X, +0.001, -0.000. The amount of increase should be approximately X-Y. Repeat Step 17 if the new shim value does not exceed 0.0075.

If the new shim value exceeds 0.0075, rotate the motor mounting 90° clockwise and go back to Step 14. (See note in Step 18.)

18. Run Tape in reverse direction for 5 seconds, measure tape to column spacing to obtain value Y. If Y does not =X, +0.003, -0.000, rotate motor mounting 90° clockwise and go back to Step 14. (See note below.)

NOTE

Motor should be tried in each of four mounting configurations before giving up on procedure above. If procedure does not work with any of the above configurations, the problem is probably due to lack of parallelism between motor mounting surface and head plate mounting surface. In this case, repeat procedure substituting Quadrant I for Quadrant II and Quadrant III for Quadrant IV. If this does not correct problem, change capstan motor, try again. When a new capstan motor is installed the DC balance adjustment should be made prior to making a tape speed adjustment.

19. Run tape forward. Look in the slot between the inside tape edge and the left vacuum column floor while the tape is moving forward. If room light is not adequate, shine penlight through from inside of vacuum column. See Figure 4-27. A constant space
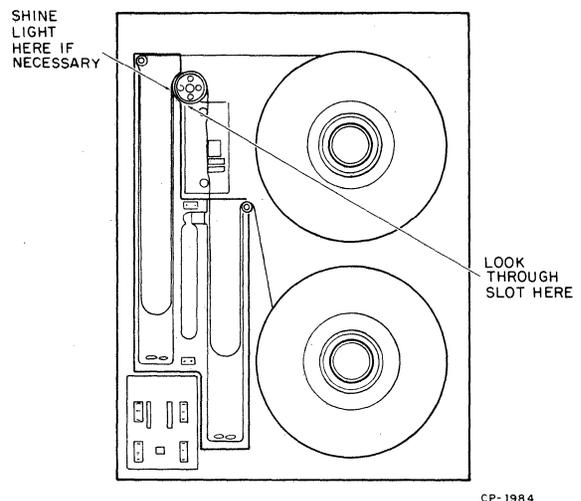
Figure 4-27a Capstan Wobble Check, Front View
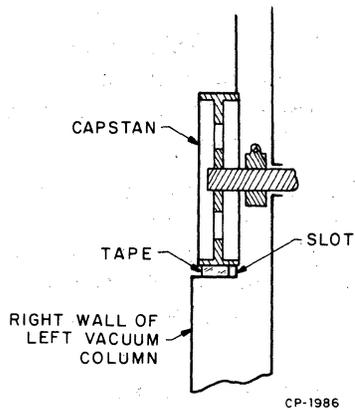
Figure 4-27b   Capstan Wobble Check, Right Side
View

(width of light) should be seen in this slot
as the tape moves forward. Periodic width
change at a very low frequency (less than
once per second) is probably due to tape de-
fects; these can be ignored unless they are
very repetitive and cause wide excursions.
Higher frequency changes (5 to 10 times per
second) are usually caused by a bent cap-
stan. If this occurs, it will be necessary to
replace the capstan and re-check tape to
column spacing with shim stock feeler
gauges.

20.   Run tape in reverse. Check slot width to
      same criteria as Step 19.

21.   Replace vacuum column door.

4.17.4.5   Final Adjustments and Equipment Evalua-
tion — Mechanical alignment of the tape path has now
been achieved. To complete the final electrical adjust-
ments, perform the operations in Chapter 5 (Preventive
Maintenance) starting from item 9 under Quarterly
(Tape Speed Adjustment) through the rest of the
quarterly items and all the semi-annual items. If any of
these adjustments cannot be satisfactorily accom-
plished, review Paragraph 4.17.1 to see if the problem
is one that requires doing a tape path alignment. If this
is the case, rotate the capstan motor and repeat the
tape path alignment. If the motor was already rotated
try shimming in quadrants I and III instead of II and
IV (see note under Step 18 of Paragraph 4.17.4.4).

4.18   ADJUSTMENT PROCEDURES
This section contains all the procedures required to ad-
just the TU16/TM02 Tape Drive System, except for
power supply adjustments. Adjustment procedures for
the TU16 power supply may be found in Paragraph

3.15.8; adjustment procedures for the TM02 power
supply may be found in the *H740D Power Supply
Maintenance Manual,* DEC-11-H740A-A-D.

4.18.1   Capstan Servo DC Balance
To perform the capstan servo dc balance adjustment,
proceed as follows:

1.   Pull the TU16 Tape Transport out on its
     slide mount.

2.   Apply power to the TU16, and place the unit
     off-line.

3.   Place the control panel START/STOP
     switch on STOP.

4.   Set up to measure the voltage at test point 2
     of the TU16's H606 Power Board.

5.   Slowly adjust R21 on the H606 Power Board
     to obtain 0.0 V ± 0.04 V at test point 2.

6.   Check capstan speed, Paragraph 4.18.2.

4.18.2   Capstan Speed
Potentiometers are located on the H606 to adjust the
FWD, REV, and REW speeds. To check and adjust
capstan speed, proceed as follows:

1.   Load a master skew tape (800 bpi).

2.   Place an oscilloscope probe on pin CU1 of
     the Read Amplifier (G056).

3.   Initiate FWD tape motion and measure a
     100 to 400 ns pulse with a period of 55.5 μs
     as shown in Figure 4-29.

4.   If necessary, adjust the FWD potentiometer,
     R13.

5.   Initiate REV tape motion; observe condi-
     tions identical to those in Step 3.

6.   If necessary, adjust the REV potentiometer,
     R12.

7.   Remove the master skew tape and load a
     scratch tape.

8.   With the TFG configured for 800 BPI, write
     an all 1's pattern on the tape.

9.   After ensuring that there is adequate tape on
     the take-up reel, run the TU16 in REW. Ob-
     serve a wave pattern similar to that shown in
     Figure 4-29, except that the period between
     pulses is approximately 16.6 ms.

10.   If necessary, adjust the REW potentiometer,
      R11.
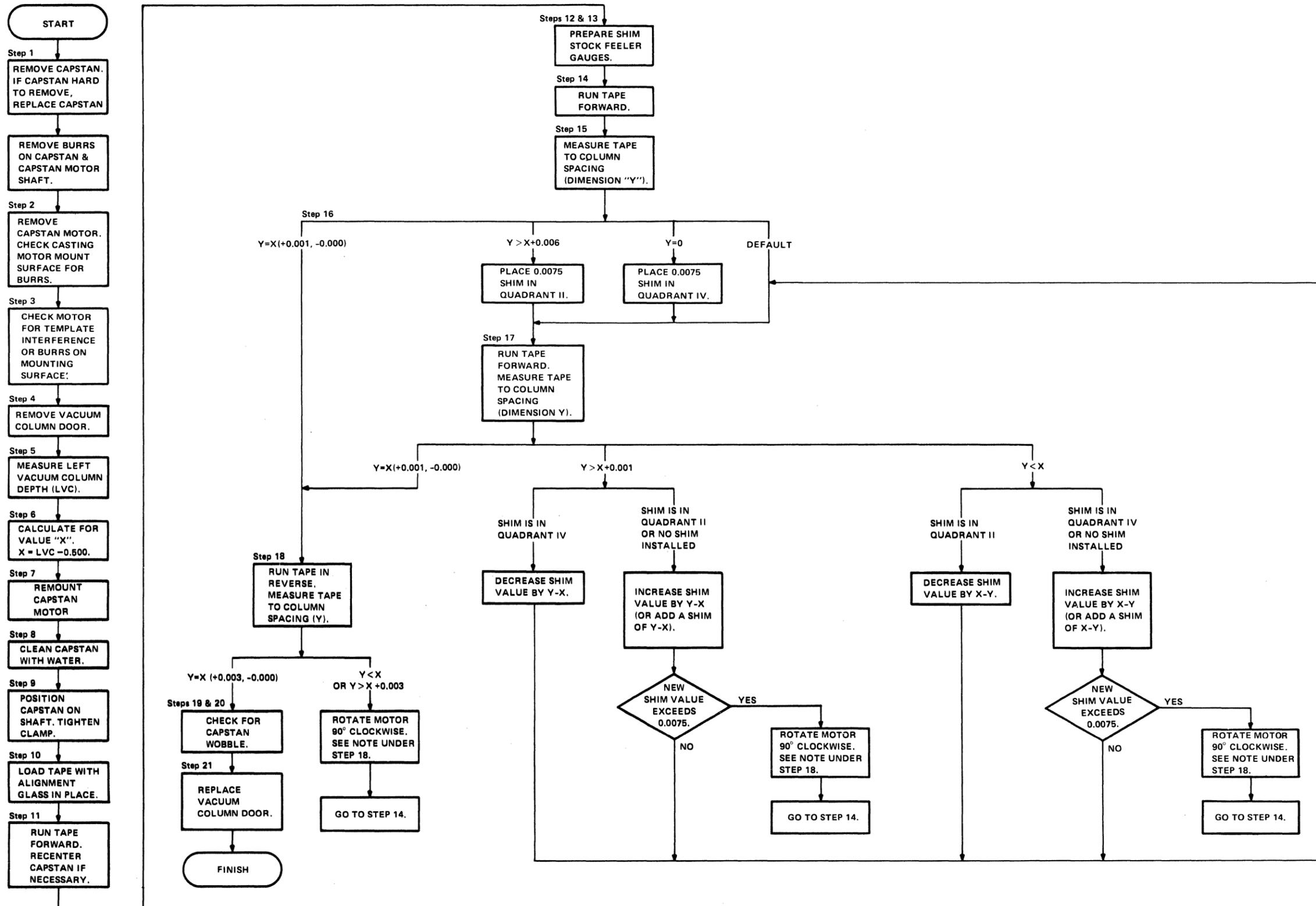
Figure 4-28   Capstan Alignment Flowchart

← 55.5 μs →

10-1340
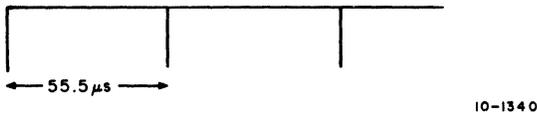
Figure 4-29   Capstan FWD and REV Speed Wave-
forms

11. Perform capstan acceleration and decelera-
tion adjustment, Paragraph 4.18.3.

4.18.3   Capstan Acceleration and Deceleration Times

Capstan acceleration and deceleration times are best
measured while running the SS RD test with the Test
Function Generator. To check the capstan accelera-
tion and deceleration times, proceed as follows:

1. Connect oscilloscope channel A to the
tachometer signal found on the H606 at P1
pin 7.

2. Connect the oscilloscope EXT TRIG to pin
A3S1 (FIRST ONE SHOT L) of the TU16
backplane.

3. Set the scope controls as follows:

Channel A	0.2 V/cm
Time/Div	2 ms/cm
A TRIG	EXT, negative slope

4. With the Test Function Generator (TFG)
module, initiate an SS RD function in the
FWD direction, and adjust R89 on the H606
to obtain a negative slope of 7—8 ms dura-
tion on the scope (Figure 4-30a).

5. With the TFG, initiate an SS RD function in
the REV direction, and adjust R90 on the
H606 to obtain a positive slope of 7—8 ms
duration on the scope (Figure 4-30b).

a. FWD TAPE MOTION   b. REV TAPE MOTION

CP-0124
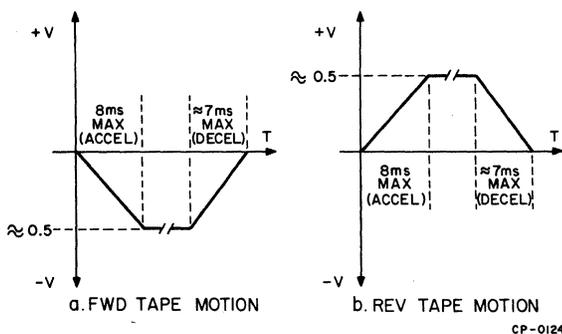
Figure 4-30   Acceleration and Deceleration Times
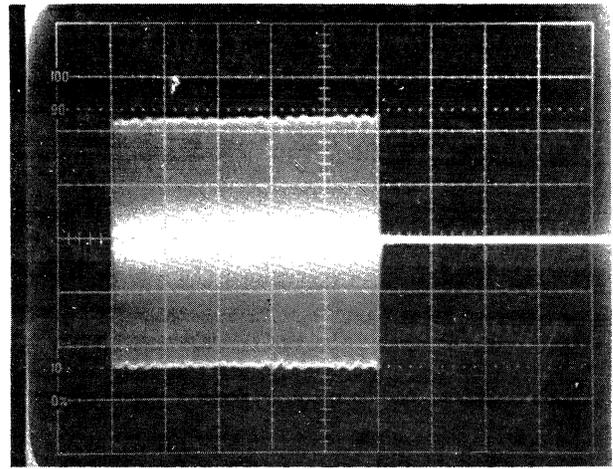
Figure 4-31   Read Amplifier Output

NOTE
**Deceleration times are not adjustable,
and will be somewhat shorter than the
acceleration times.**

6. Check Read amplitudes (Paragraph 4.18.5).

4.18.4   Brake Adjustment (Electrical)

To ensure proper operation of the TU16, an adjust-
ment to the brake circuit may be necessary after
normal wear or long periods of inactivity. In addition,
brake operation must be checked after cleaning the
brake armature. The TU16 brake circuitry has two ad-
justments that affect brake operation during
REWIND. Both adjustments affect only the upper
brake and upper vacuum column.

Proceed as follows to perform a visual check of the RE-
WIND operation:

1. Place the TU16 in the off-line mode and
move tape to EOT.

2. Initiate the REWIND operation from EOT
several times. Allow the operations to con-
tinue approximately 10 sec before returning
to EOT.

3. Initiate the REWIND operation and conti-
nue to the BOT marker. Check for an im-
properly adjusted brake circuit by watching
for any of the following symptoms during
the REWIND operation:

a. Any vacuum column failure.

b. More than two or three tape loop excur-
sions exceeding approximately one-
third of the distance into the brake zone.

4-28

During acceleration from EOT, two or three large excursions are normal.

c. Normal tape loop excursions during acceleration but a sluggish return of the tape loop from the reel motor zone to the brake zone.

d. Erratic tape loop excursions during the continuous REWIND operation exceeding 1¼ inches above the upper vacuum column upper vacuum switch. Tape motion will always be somewhat erratic, but the magnitude of the loop "jumps" should be less than 1¼ inches.

In almost every case, a tape loop failure can be diagnosed as an extreme example of symptoms b, c, or d.

Continuous large tape loop excursions (symptom b) are probably due to one of the following:

1. High current rewind time is too short. The high current rewind time is measured as a negative pulse at test point 14 of the H606 Power Board during a REWIND operation. Typical pulse width is 20—25 ms. It is adjusted using the REW PULSE potentiometer (R61) on the H606 Power Board.

2. Low current rewind amplitude is too low. The amplitude is adjusted using the LOW CURRENT ADJ potentiometer (R79) on the H606 Power Board. Clockwise rotation of the potentiometer increases the current to the brake. Adjustment should be made at intervals not greater than two turns of the potentiometer.

Symptom c is an indication that the low current rewind amplitude is too high. Counterclockwise adjustment of the LOW CURRENT ADJ potentiometer (R79) on the H606 Power Board will decrease the amplitude. The effects of the potentiometer adjustment should be observed at intervals of two turns of the potentiometer.

Symptom d is an indication that the high current rewind time is either above or below the ideal operating range. The 20—25 ms range is a helpful guideline, but is not absolute, and will depend on the operation of the brakes.

4.18.5 Read Amplitude Adjustment

1. Check capstan speed (Paragraph 4.18.2) and adjust if necessary.

2. Rewind tape and remove from transport.

3. Clean the read/write head, erase head, and tape cleaner.

4. Load a good quality tape, positioned at BOT; set up the scope as follows:

   Channel 1 = 2 V/cm
   Sweep speed = 2 ms/cm
   Trigger = normal, Channel 1 triggered.

5. Set the switches on the TFG as follows:

   S4: 1-8 ON
   S4: 9 & 10 OFF
   S5: 9 & 10 ON
   S5: 1-8 OFF
   S6: 1-8 OFF
   SSWRT, SSRD, and WRT: down.

6. Place the SSWRT switch in the TFG up, and place Channel 1 probe on A4-L1. The scope presentation should resemble the Figure 4-31.

7. Increase vertical sensitivity to 1 V/cm and place inter-record gap 1 cm down from top. Measure negative half of read amplifier output (using the inter-record gap as the baseline). The peak amplitude of the negative-going signal should be from -4.45 to -4.75 V. (See Figure 4-32.)

8. Repeat Step 7 for all 9 tracks. See Table 4-2.
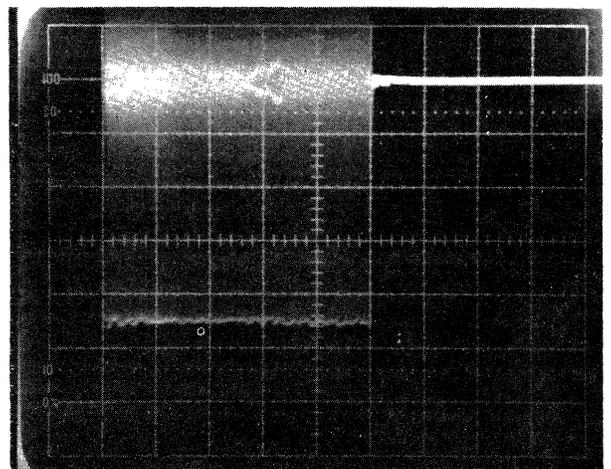
Figure 4-32   Negative Half of Read Amplifier Output

Table 4-2 Read Amplitude Test Points

Track	Pin
1	A4-L1
2	B4-B1
3	B4-M1
4	C4-K1
5	C4-L1
6	D4-P1
7	D4-R1
8	F4-P1
9	F4-R1

If any track is out of the acceptable range (-4.45 to -4.75 V), adjust all nine channels to -4.6 V. Such adjustment requires the following procedure:

a. Turn power OFF.
b. Take the TFG off the extender.
c. Place G056 on extenders.
d. Turn power ON.
e. Adjust all read amplifiers to -4.6 V. (Potentiometers are arranged sequentially from top to bottom, starting with Track 1.)

NOTE

If any channel cannot be adjusted within range, the TU16 input preamplifier resistors may have to be changed.

9. Place the SS WRT switch on the TFG down; rewind the tape.

4.18.6 Write Skew Adjustment

The procedure should be performed only after completing the read skew adjustment (Quarterly PM items 13 and 14 in Chapter 5). Write skew adjustment is only required upon replacement of the head plate assembly, or when excessive wear in the head plate assembly is suspected.

1. Slide the TU16 Tape Transport out of the cabinet.

2. With power removed from the transport, remove the Test Function Generator (TFG) module (M8912) from section EF of slot 3.

3. Set the TFG switches as follows:

S5 segments 1—8	OFF
S5 segment 9	ON
S5 segment 10	OFF
S6 segments 1—8	OFF

4. Insert the TFG into section AB of slot 3.

5. Ensure that the SS RD, WRT, and SS WRT switches at the upper portion of the module are in the lowered position.

6. Apply power to the TU16. The LED indicator on the TFG should light.

7. Load write-protected IBM skew tape (800 bpi) on the transport.

8. Initiate forward tape motion from the transport control panel.

9. Connect the channel A input of an oscilloscope to pin E4K1 (PACKET), using internal sync, negative slope. PACKET is a composite signal, comprised of Read Amplifier outputs of all nine tracks.

10. Monitor the pulses which comprise PACKET on Channel B of the scope, using chopped mode. Note and tabulate their positions, in microseconds, with respect to the leading edge of PACKET (Figure 4-33). Table 4-3 lists the pins to be monitored for each track; it also contains a column, left blank, for listing the position of the monitored pulses relative to PACKET, and can therefore serve as a model to the user.

Table 4-3
Write Deskew Parameters

Track No.	Pin	Measured Pulse Position (μs)
1	A4J1	
2	A4H1	
3	B4N1	
4	B4L1	
5	C4U1	
6	C4S1	
7	E4H1	
8	E4F1	
9	F4M1	
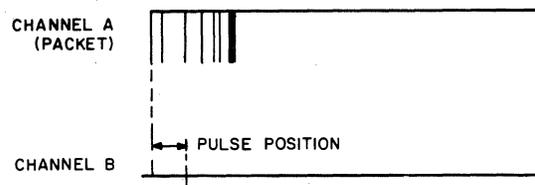
Figure 4-33 Measurement of Pulse Positions Relative to Packet

11. After tabulating the data for all 9 tracks, terminate tape motion.

12. Unload the skew tape and load a scratch tape on the transport.

13. Raise and lower the TFG SS RD switch; this loads the preselected data pattern.

14. Raise the TFG WRT switch. Now initiate forward tape motion from the transport control panel. The TU16 will perform a continuous write operation.

15. Monitor the pins that were monitored in step 10. Note the position of the displayed pulses relative to the leading edge of PACKET. If the position measured now differs from the position measured in step 10 by more than 2μs, alter the write deskew jumper configuration on the TU16 backplane. The jumpers connect the Write Deskew Buffer (refer to drawing M8910, sheets 3 and 4) to four record pulses (SK CLK A, SK CLK B, SK CLK C, and SK CLK D) which are shift delayed in increments of 0.9μs. These pulses are available at the following pins:

SK CLK A	A2R1 and A2R2
SK CLK B	A2N1 and A2N2
SK CLK C	A2L1 and A2L2
SK CLK D	A2B1 and A2B2

The jumper configuration must be modified so that the position of the monitored pulse with respect to the leading edge of PACKET does not vary by more than 2μs from that obtained in step 10.

16. After performing the write skew adjustment remove power from the transport and replace the TFG module in section EF of slot 3.

4.18.7 Read/Write Interlock Assembly

Proceed as follows to perform the Read/Write Interlock assembly adjustment (Figure 4-34):

1. Loosen the two screws securing the switch to the bracket just enough to allow the switch to be moved.

2. Loosen the locknut and adjusting screw several turns (see detail B, Figure 4-34).

3. Insert the small end of the setting gauge (29-18610) in front of the roll pin through the bottom of the bracket body edge. Tighten the adjusting screw until the switch just actuates.

4. Tighten the two screws securing the switch to the bracket and lock the adjusting screw using the locknut.

5. Loosen the two solenoid mounting screws (see detail A, Figure 4-34).

6. Insert the large end of the setting gauge in front of the roll pin as described in step 3. Push the solenoid body forward until the plunger bottoms out; then tighten the solenoid mounting screws, keeping the solenoid body parellel to the upper edge of the bracket.

7. Loosen the bottom screws securing the interlock assembly to the mounting bracket. (See detail C, Figure 4-34).

8. Insert the ring gauge (29-18608) on the reel, lock it, and spin the reel to check for even rotation.

9. Push the interlock assembly forward until the shaft bottoms in the solenoid and the small spring is fully depressed.

10. Tighten the screws securing the assembly to the bracket, remove the ring gauge, and check for free movement of the solenoid shaft in the casting.

4.18.8 Vacuum Motor Belt Adjustment Procedure

The vacuum motor subassembly should be removed from the main assembly framework before working on it. Refer to Paragraph 4.12 for the removal procedure.

Proceed as follows to adjust the vacuum motor belt:

1. Tighten the four motor plate mounting nuts.

2. Using gauge CMD-9606370 set pulley height to 0.520 or 0.820 inches.

NOTE
The pulley is positioned either 0.520 inch or 0.820 inch above the mounting assembly to accommodate 60 or 50 Hz operation, respectively (selects one of two pulley diameters). For further information, refer to the vacuum assembly drawing E-AD-7009638-0-0.

3. Place belt tension gauge on belt.

4. Pull belt tension gauge knob until surface "A" touches belt. (See Figure 4-35).

5. Tension should read 14-16 lbs.

SOLENOID WIRES

A

SOLENOID (ADJUSTABLE)

SOLENOID MOUNTING BRACKET

SOLENOID SHAFT

B   C

SWITCH (ADJUSTABLE)

SWITCH
CONNECTING
PINS (3)

C

INTERLOCK ASSEMBLY
ADJUSTMENT
SCREWS
(UNDERSIDE OF
MOUNTING BRACKET)

A

SOLENOID
ADJUSTMENT
SCREWS (LEFT OF
INTERLOCK ASSEMBLY
AS VIEWED FROM
FRONT OF TU16)

B

SWITCH
ADJUSTMENT
SCREW

CP-0096
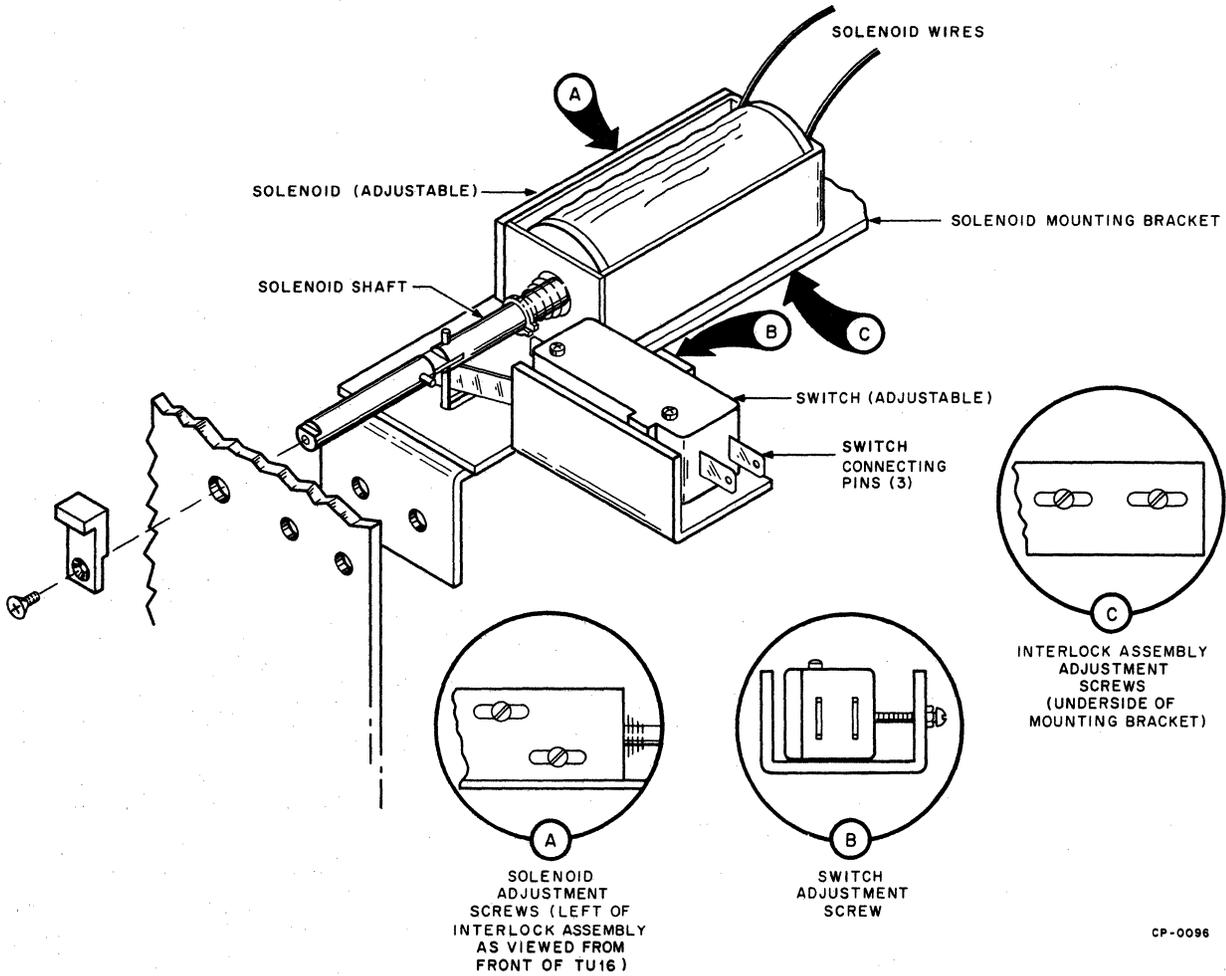
Figure 4-34   Read/Write Interlock Assembly

6. If tension is out of tolerance loosen the four motor plate mounting nuts and adjust the motor plate take up screw until the 14-16 lb. reading is obtained. Tighten the motor plate mounting nuts.

7. If a belt tension adjustment was made to the vacuum motor, the tension must be re-checked after the motor has been run for more than 30 minutes. Recheck the tension by performing steps 3, 4, and 5 of this procedure. If necessary readjust the belt tension by performing step 6.
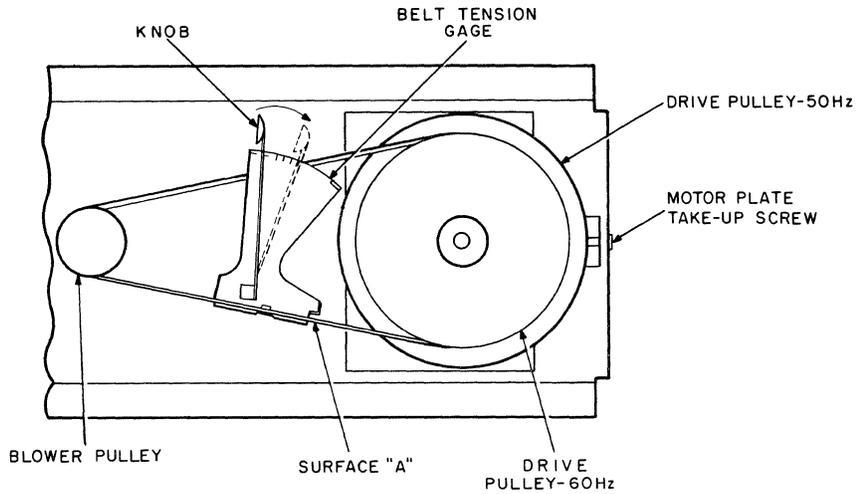
10-2075

Figure 4-35   Vacuum Motor Belt Adjustment

5.1 PREVENTIVE MAINTENANCE SCHEDULE

The recommended frequencies for performing the PM steps in this procedure are based on moderate usage of the equipment. In cases where usage is heavy, certain steps should be performed more frequently.

For example, items 1 and 9 through 16 of the quarterly procedure (Paragraphs 5.4.1 and 5.4.9 through 5.4.16) assume that tape motion will not exceed 150 hours/quarter; if tape motion exceeds that figure, the steps should be performed more often. (Tape motion = Time spent actually moving tape; this must be decreased by 1/2 if software is not double-buffered, or if two drives exist on the same controller.)

Item 2 of the quarterly procedure (Paragraph 5.4.2) assumes that vacuum on-time will not exceed 1000 hours/quarter; if vacuum on-time exceeds that figure, this step should be performed more frequently. (Vacuum on-time = Time that tape is loaded on a drive with vacuum on, whether or not the tape is actually moving.)

The semiannual procedure (Paragraph 5.5) assumes that tape motion will not exceed 300 hours during a 6-month period; if tape motion exceeds that figure, the procedure should be performed more frequently.

5.2 SPECIAL TOOLS AND EQUIPMENT

Table 5-1 lists the special tools and equipment required to perform Preventive Maintenance.

Table 5-1
Special Tools and Equipment Required for PM

Tools and Equipment	Part No.
Microscope	29-20273
Magna-see	29-16871
Penlight*	29-10780
Feeler Gauge Set*	29-13515

*Contained in standard tool kit.

5.3 MONTHLY

The five items listed under Paragraph 5.3 are to be performed on a monthly basis.

5.3.1 Tape Path Cleaning and Inspection

Clean the tape path and inspect it for wear as follows:

a. Turn power OFF in the 861 Power Controller. Remove and clean the take-up reel, using a Kimwipe dampened with water; inspect the take-up reel for cracks or loose center ring (hub interface). Replace if necessary.

b. Remove supply reel (if installed). Using water-dampened Kimwipes, clean the deckplate surfaces and front door.

CAUTION
Be careful not to saturate the Scotch-Lite lining on the vacuum column walls with fluid; this could cause damage to the lining.

c. Remove the head cover and open the vacuum door.

d. Using a penlight flashlight, inspect the read/write head and erase head for oxide accumulation. A worn head will normally show oxide accumulation on the worn spot. If the read/write head is unevenly worn or if the erase head shows any wear, replace the head plate assembly. (Refer to Figure 5-1; shiny spots indicate uneven wear.)

NOTE
Wear spots of any kind on erase head require head plate replacement.

e. Using DEC magtape cleaning fluid and cotton-tipped wooden swabs, clean any accumulatemulated oxide from the read/write head, erase head, tape cleaner, and fixed guides. (Pay particular attention to removing oxide buildup from ceramic surfaces of fixed guides.)
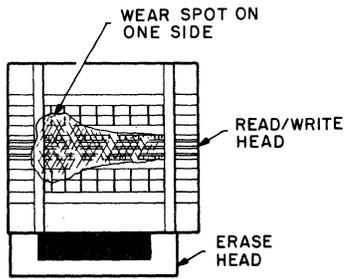
Figure 5-1a   Examples of Unacceptable Head Assembly Wear, Uneven Wear on Read/Write Head

Figure 5-1b   Examples of Unacceptable Head Assembly Wear, Wear on Erase Head

NOTE
Ensure that the inner (spring-loaded) guides move freely after cleaning and that they are not jammed under the fixed guides.

f.   Clean vacuum columns and vacuum column doors with DEC magtape cleaning fluid and Kimwipes. Clean roller guides with cotton swabs and DEC magtape cleaning fluid.

5.3.2   Reel Hub Inspection and Lubrication
Lubricate and inspect reel hubs as follows. (Refer to Figure 5-2.)
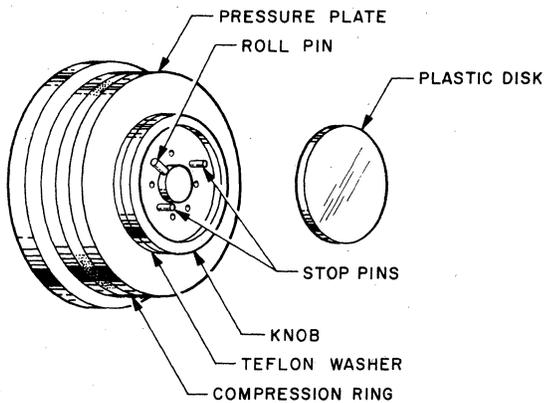
Figure 5-2   Hub Composition

a.   Lubricate the upper and lower reel hub compression rings by applying silicon grease generously by finger and rubbing it in. Wipe away excess with Kimwipe.

b.   Place the takeup reel on the lower hub. Turn the hub lock until it hits the stop pin. Hold the hub with one hand and attempt to turn the reel counterclockwise with the other hand.

c.   If the hub lock does not hit the step when tightened or if the reel turns while the hub is being held stationary, readjust the hub pin and replace the compression ring according to the following procedure.

   (1) Remove power from the TU16 Tape Transport and remove the tape reel.

   (2) Carefully snap out the plastic disk from the reel hub.

   (3) Mark the position of the center roll pin in the hub guide.

   (4) Using a pair of heavy duty diagonal pliers, carefully remove the center roll pin.

   (5) Grasp the reel hub and unscrew the knob from the hub.

   (6) Remove (in order) the Teflon washer, pressure plate, and rubber compression ring.

   (7) Lightly lubricate the flat surfaces of a new compression ring with silicon grease. Wipe all excess grease from the ring with a lint-free cloth.

   (8) Install (in order) the new compression ring, pressure plate, and Teflon washer.

   (9) Lightly tighten the knob on the hub until the compression ring is compressed and fully seated.

   (10) Loosen the knob until it is free of the Teflon washer. Then gently screw it in until it just touches the washer.

   (11) Reinstall the roll pin in the same hole from which it was removed [step (4), above].

   (12) Turn the knob counterclockwise until the roll pin makes contact with one of the two hub stop pins.

   (13) Try to install a tape reel on the hub. If the tape reel does not easily slip on the hub, move the stop pin back one hole at

a time until the knob can be released far enough to permit the tape reel to slip on the hub.

    (14) With the tape reel installed, tighten the knob (clockwise) until the roll pin contacts the other hub stop pin. If the tape reel is not secure, move the stop pin ahead until the knob can be tightened correctly.

d. Place the takeup reel on the upper hub. Repeat the procedure followed for the lower hub takeup reel in step b, above.

5.3.3 Operator Panel Check

Check the operator panel switches aud indicators as follows. (Replace switches and/or indicators as required.)

a. Apply power to the 861 Power Controller; ensure that the OFF-LINE and PWR indicators on the control panel are ON.

b. Place a scratch tape (with write ring) on the lower hub and secure the hub lock. Set the LOAD/BR REL switch to LOAD and then back to BR REL. Ensure that both reels turn freely and that the FILE PROT light does not light as the supply reel is rotated.

c. Thread the scratch tape through the tape path and take two wraps around the takeup reel. Set the LOAD/BR REL switch to LOAD; ensure that the LOAD indicator on the control panel comes ON.

d. Place the FWD/REW/REV switch to FWD; place the START/STOP switch to STOP and then back to START. Ensure that the FWD indicator is lit while the drive is moving the tape toward BOT, and that the LD PT indicator lights when the drive stops at BOT.

e. Run the tape forward for approximately 30 seconds; set the START/STOP switch to STOP.

f. Set the FWD/REW/REV switch to REV; press START. Allow the tape to run in reverse for approximately 10 seconds and ensure that the REV indicator is ON. Place the START/STOP switch in the STOP position.

g. Set the FWD/REW/REV switch to REW; press START. Ensure that the REW indicator is ON.

h. Set the ON-LINE/OFF-LINE switch to ON-LINE. When the drive has completed the re-wind operation in step g, above, check that the RDY indicator comes ON. Check that the SEL indicator also comes ON if the TM02 is currently selecting this TU16.

i. Set the ON-LINE/OFF-LINE switch to OFF-LINE and the LOAD/BR REL switch to BR REL. Dismount the tape and remove the write enable ring. Mount the tape and ensure that the FILE PROT indicator is ON. Rotate the reel; ensure that the FILE PROT indicator remains ON.

NOTE
If a quarterly PM procedure is scheduled, proceed to item 1 of that procedure (Paragraph 5.4.1); if not, continue with item 4 below.

5.3.4 NRZ Diagnostic

Position tape at BOT; place unit ON-LINE. Run the On-Line Diagnostic for 10 minutes of NRZ (800 bpi). If any soft errors occur, it will be necessary to run a complete pass to determine whether the frequency of soft errors is within specification; no hard read errors are allowed.

NOTE
Acceptable soft error rate for one 2400-foot reel of tape is:

    a. Forward read: 2
    b. Reverse read: 2
    c. Write: 2

Retries on the same spot do not increase the soft error tally; i.e., a read error on block #1, record #1, that required three retries to recover is recorded as one soft read error.

5.3.5 Phase Encoding Diagnostic

Rewind tape; run 10 minutes of Phase Encoding ON LINE. If any soft errors occur, it will be necessary to run a complete pass to determine whether the frequency of soft errors is within specification; no hard read errors are allowed.

NOTE
Acceptable soft error rate for one 2400-foot reel of tape is:

    a. Forward read: 3
    b. Reverse read: 5
    c. Write: 5

Retries on the same spot do not increase the soft error tally; i.e., a read error on block #1, record #1, that required three retries to recover is recorded as one soft read error.

5.4 QUARTERLY

The fifteen items listed under Paragraph 5.4 are to be performed on a quarterly basis.

5.4.1 Reel Motor Brakes

Disassemble, clean, and reassemble the reel motor brakes according to the following procedure:

a. With power OFF, pull the transport out on its slides. (Access brakes from the left side of the transport; operation is identical for both reel motors.)

b. Loosen the Allen-head screw located on the clamp. (See Figure 5-3.)

c. Remove the spring and brake assembly. Push a cotton swab through each of the inserts (locating holes) that hold the rotor disk and rotor to ensure that they are securely held in the rotor and that they do not protrude in such a way as to interfere with operation of the rotor disk. If inserts are loose, replace the brake assembly.

d. Using a clean, dry, lint-free cloth or wipe, clean the following:

   (1) The brake surface of the stator (stator is still on motor).

   (2) Both sides of the rotor disk, including location pins.

   (3) The face of the rotor next to the rotor disk.

NOTE
Avoid skin contact with brake surfaces; body oils are detrimental to brake function.

e. Install the rotor disk into the rotor; select the mating combination that allows for smoothest insertion and retraction of rotor disk pins into the rotor locating holes. Try each of the 120-degree intervals for best fit.

f. Replace the brake, leaving a clearance of 0.010 inch between the rotor disk and the stator and approximately 3/6 inch clearance
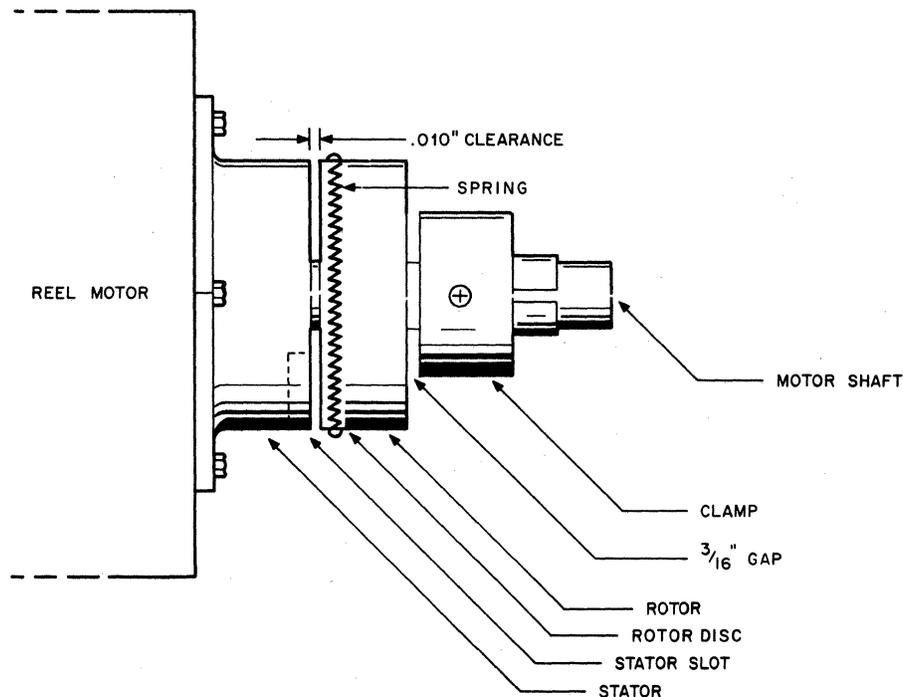
CP-1539

Figure 5-3   Reel Motor Brake Assembly

between the rotor and the clamp. In this position, the clamp should be clamping on the splits cut into the sleeve of the rotor, ensuring that the rotor is fastened securely to the reel motor shaft. When clearances are correct, tighten the Allen screw.

g. With the 0.010-inch feeler gauge inserted between the stator and the rotor, rotate the reel motor manually from the front of the unit to see that the brake is spaced uniformly all around. If necessary, rotate the brake at 120-degree intervals to determine best position for uniform separation. (An excessively high or low spot is cause for replacing brake assembly.)

h. Remount the rotor spring between the rotor disk and the rotor.

i. When the above steps have been completed for both reels, rotate both reels, feeling for free rotation and listening to ensure that there is no squealing from stator/ rotor disk contact.

5.4.2 Vacuum Motor Brushes*

With power OFF, replace the vacuum motor brushes as follows:

a. Disconnect the vacuum motor electrical connector by unplugging P9 from J9 (wires from plenum cover on vacuum motor).

b. Loosen three large Phillips head screws that fasten plenum chamber cover to the casting and remove plenum chamber cover.

c. Remove the brush assembly by removing the screws that hold the U-shaped bracket over the brush assembly, then pull out the connector that holds the coil wire of the brush assembly.

d. Using a cotton-tipped wooden swab, carefully clean the commutator. Apply a drop of light oil at the rear sleeve bearing, taking care not to get any oil on the commutator.

e. Install and connect the new brush assembly.

f. Reinstall cover and reconnect P9 to J9.

5.4.3 Voltage Check Setup

Set up as follows to check voltages:

a. Turn power OFF; remove M8912 [Test Function Generator (TFG)] from slot EF3 and place it on the module extender in slot AB3.

b. Place SSRD, SSWRT, and WRT switches down; turn power ON.

NOTE
In all voltage checks, refer to the figure 5-4 for the location of the potentiometers that control adjustments. If any voltages cannot be adjusted to meet specifications, repair or replace the regulator board.

5.4.4 +5 Vdc Check (drive logic)
Check the +5 Vdc drive logic voltage.

Reference Point = D01A2 (Red wire)
Nominal Value = +5.25 ± 0.05 V

If adjustment is necessary, adjust potentiometer R16.

5.4.5 +12 Vdc Check (drive voltage)
Check the +12 Vdc drive voltage.

Reference Point = A04V1 (Yellow wire)
Nominal Value = +12.05 Vdc ± 0.05 V

If adjustment is necessary, adjust potentiometer R37.
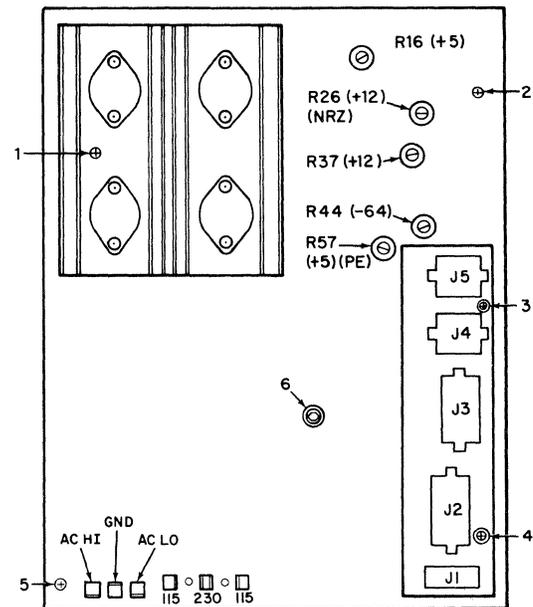
NOTES:
1) 1-5 represent 5 Phillips head screws.

2) 6 represent Allen screw—must be secured very tightly, or damage to the power supply may result.

IO-1317

Figure 5-4   TU16 Power Supply Regulator Board

*For TU10 vacuum systems only. For TU16 vacuum systems, skip Paragraph 5.4.2.

5.4.6 -6.4 Vdc Check

Check the -6.4 Vdc drive voltage.

Reference Point = C04N2 (Green wire)
Nominal Value = -6.35 Vdc ± 0.05 V

If adjustment is necessary, adjust potentiometer R44.

5.4.7 +12 Vdc Check (NRZ)

With S5-9 (M8912) ON, check the +12 Vdc (NRZ) drive voltage.

Reference Point = C02J2 (Orange wire)
Nominal Value = +11.875 Vdc ± 0.125 Vdc

If adjustment is necessary, adjust potentiometer R26.

NOTE
Paragraphs 5.4.7 and 5.4.8 are interactive, and must be performed in that sequence.

5.4.8 +5 Vdc Check (PE)

With S5-9 (M8912) OFF, check the +5 Vdc (PE) drive voltage.

Reference Point = C02J2 (Orange wire)
Nominal Value = +5.6 Vdc ± 0.1 V

If adjustment is necessary, adjust potentiometer R57.

NOTE
The remaining steps in this PM procedure require a well-calibrated oscilloscope. It is advisable to check the voltage and frequency calibration at this time, with the probes intended for use.

5.4.9 Forward Tape Speed and DC Balance Check

Check forward tape speed as follows:

a. Turn power OFF; disconnect the erase head cable (the 2-pin connector located just below the read/write head) and the write head cable (located directly above the erase head connector.

b. Turn power ON; load a master skew tape and position it at BOT.

c. Set scope vertical gain to 50 mv/cm.

d. Check the voltage at test point 2 of the TU16's H606 Power Board.

e. Slowly adjust R21 (BAL) on the H606 Power Board to obtain 0.0 V ± 0.04 V at test point 2.

NOTE
50 millivolts of ac ripple will be seen on the scope. Center the ac ripple on ground to obtain a 0 volt dc level.

f. Set oscilloscope as follows:

10 μs/cm
Channel 1: 2 V/cm
Triggering:
  Normal
  Negative slope
  Channel 1 triggered
Channel 1 probe to C4-U1.

g. Initiate FWD tape motion; check that negative pulses are 55—57 μs apart. (See Figure 5-5.) If not, adjust FWD potentiometer R13 on H606 for 56 μs.
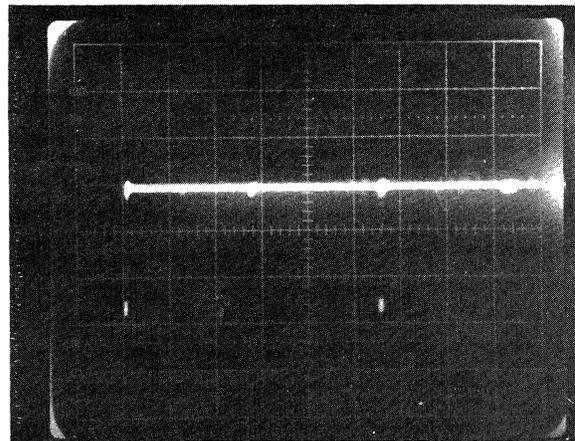
Figure 5-5 Tape Speed Check, 10 μs/cm Sweep Speed

5.4.10 Reverse Tape Speed Check

Initiate REV tape motion; check that negative pulses are 55—57 μs apart. If not, adjust REV potentiometer R12 on H606 for 56 μs.

5.4.11 Forward Jitter Check

Check forward jitter as follows:

a. Change sweep to 20 μs/cm; initiate FWD tape motion. Check that four negative pulses appear on the oscilloscope screen. (See Figure 5-6A.)

b. Use the horizontal X10 magnifier to increase the horizontal display. Using the horizontal
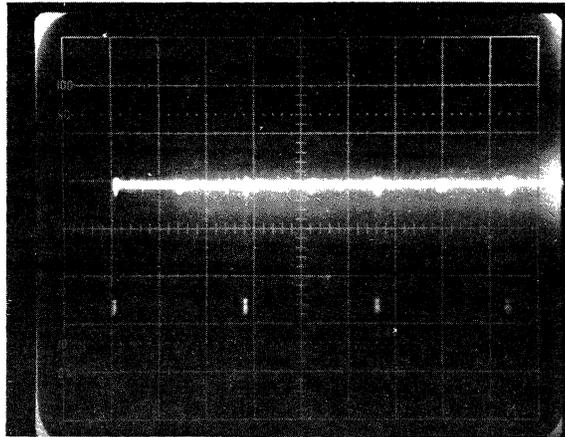
Figure 5-6a   Jitter Check, Scope Setup
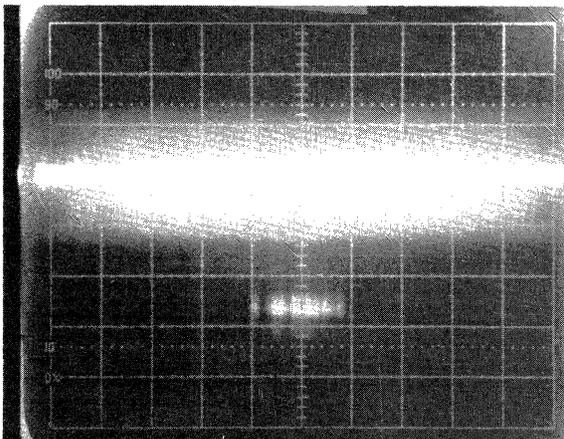
Figure 5-6b   Jitter Check, Capstan Motor Good
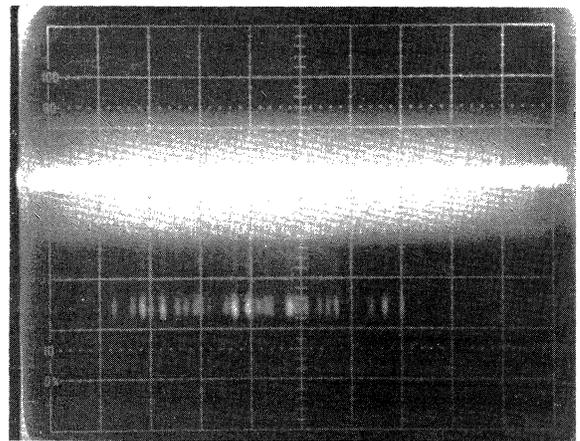
Figure 5-6c   Capstan Motor Bad

position knob, place the *third pulse* in the center of the screen. Check that the jitter is *less than 6 μs* (3 cm on the scope, as indicated in Figure 5-6B). If jitter exceeds 6 μs (as in Figure 5-6C). replace the capstan motor.

NOTE
If it is necessary to replace the capstan motor, tape path alignment must be performed at the same time. (See Paragraph 4.17.)

5.4.12 Reverse Jitter Check
Initiate REV tape motion; repeat Paragraph 5.4.11, above, to check reverse jitter. Remove the X10 horizontal magnification on the oscilloscope.

5.4.13 Forward Skew Check
Perform mechanical skew (head azimuth) adjustment as follows:

a. Set up the oscilloscope as follows:

   1 μs/cm
   Channel 1: 2 V/cm
   Triggering:
       Normal
       Positive slope
       Channel 1 triggered
   Channel 1 probe to E4K1 (Packet H).

b. Initiate FWD motion; synchronize the scope. Adjust the Phillips head screw on the head plate (Figure 5-7) for minimum packet width (must be less the 2.5 μs) as shown in Figure 5-8. If adjustment cannot be made, tape path alignment must be performed at this time. (See Paragraph 4.17.)

NOTE
An occasional jump in packet width of 1 μs is usually allowable in Paragraphs 5.4.13 and 5.4.14 (usually due to tape defect); however, this should not occur more often than once per second.

5.4.14 Reverse Skew Check
Initiate REV tape motion; ensure that packet width is less than 3.5 μs. No adjustment is possible; if packet width exceeds maximum, tape path alignment must be performed (see Paragraph 4.17). Allow skew tape to continue in REV mode to BOT. (Do not rewind.) Remove skew tape. Connect write and erase heads.
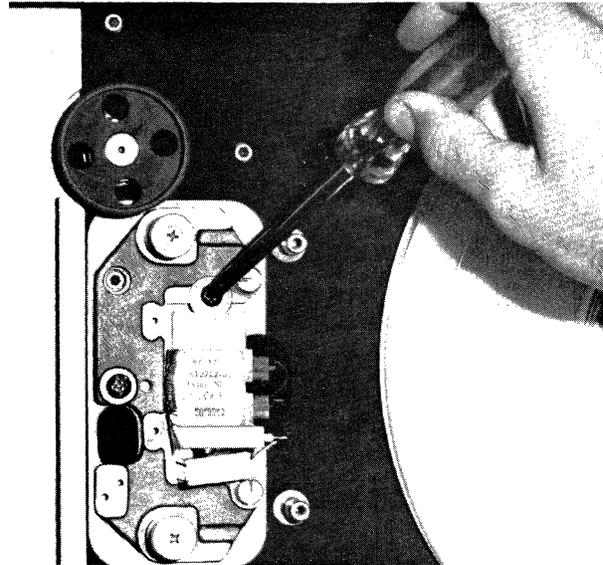
7660-9

Figure 5-7   Adjusting Mechanical Skew
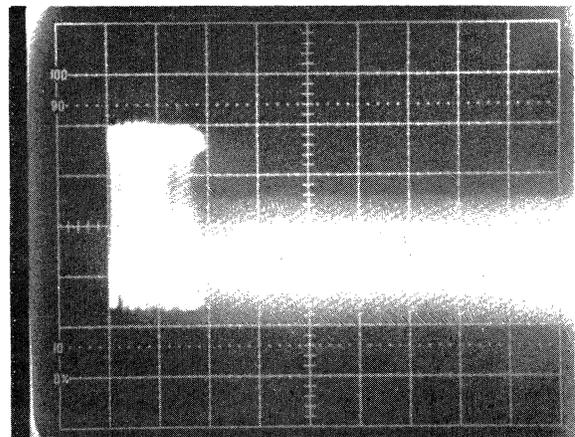
Figure 5-8   Packet Waveform

NOTE
If a semiannual PM procedure is scheduled, proceed to Paragraph 5.5; if not, continue with Paragraph 5.4.15 below.

5.4.15 Functional Test Diagnostic
Run the Basic Function Test (MAINDEC-11-DZTUB) as follows:

a. Turn power OFF.

b. Remove the TFG from slot AB03 and plug it into slot EF03.

c. Turn power ON.

NOTE
Perform Paragraphs 5.3.4 and 5.3.5 of the monthly PM procedure at this time.

5.5 SEMIANNUAL

The eight items listed under Paragraph 5.5 are to be performed on a semiannual basis.

5.5.1 Forward Ramp Check

Adjust forward acceleration ramp as follows:

a. Float the scope as shown in Figure 5-9.

WARNING
While the scope is floated, avoid contact with the case of the scope and the internal ground lead of the scope probe.

b. Set the switches of the Test Function Generator (TFG) module (M8912) as follows:

(1) SSRD, SSWRT, and WRT: Down.

(2) S4-9: OFF.

c. Load a scratch tape (with write ring installed) and position it at BOT.

(1) Place probe from external trigger to A3S1.

(2) Connect Channel 1 probe to P1-7 of the H606 module.

(3) Connect Channel 1 ground to GND test point on H606 (adjacent to P3-4).

(4) Set scope to external sync, negative slope, 2 ms/cm, with Channel 1 to 0.2 V/cm (20 mV/cm if X10 probe is used).

d. Set FWD/REV/REW switch to FWD. Place SSRD switch on TFG (M8912) up. Observe negative slope of 7—8 ms. (Refer to Figure 5-10.) Adjust -CUR potentiometer on H606, if necessary.

5.5.2 Reverse Ramp Check

Adjust reverse acceleration ramp as follows:

a. Set FWD/REV/REW switch to REV. Observe positive slope of 7—8 ms. (Refer to Figure 5-11.)

b. Adjust +CUR potentiometer on H606, if necessary.

5.5.3 Tracking Check Setup

Place SSRD switch on TFG (M8912) down. Rewind tape. Remove float from scope ground.

TO POWER

SCOPE GROUND
NOT CONNECTED
(ROUND PIN)

TO SCOPE

CP-0226
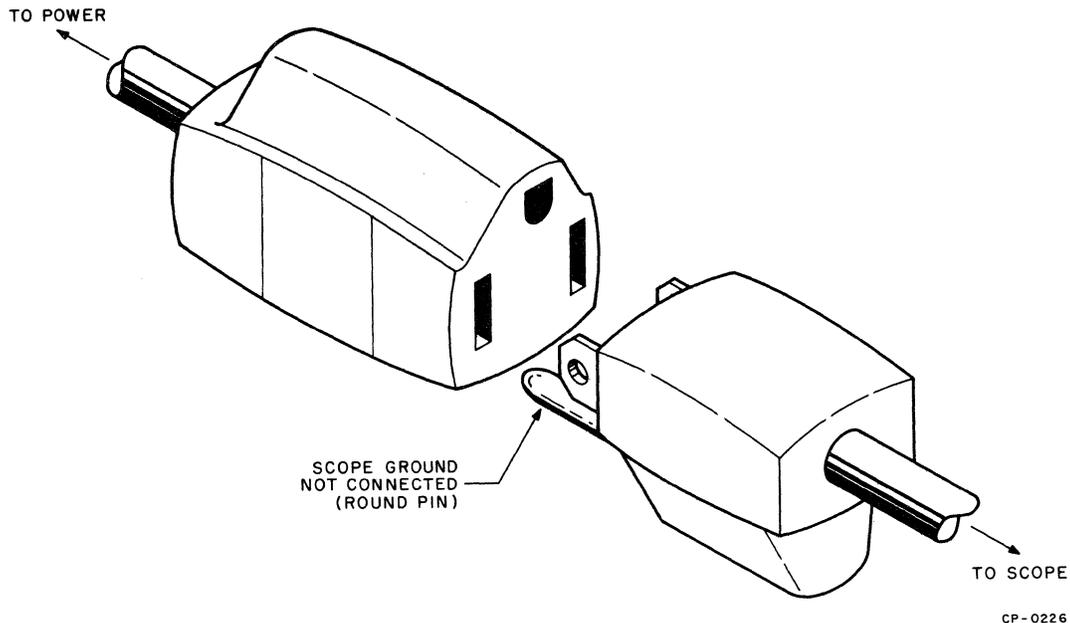
Figure 5-9   Floating Oscilloscope Connection
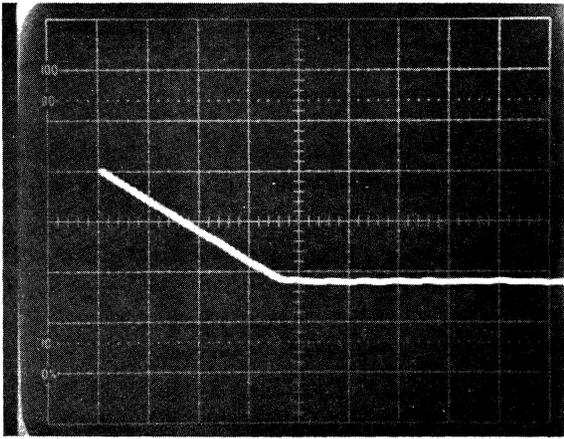
Figure 5-10   Forward Acceleration Ramp
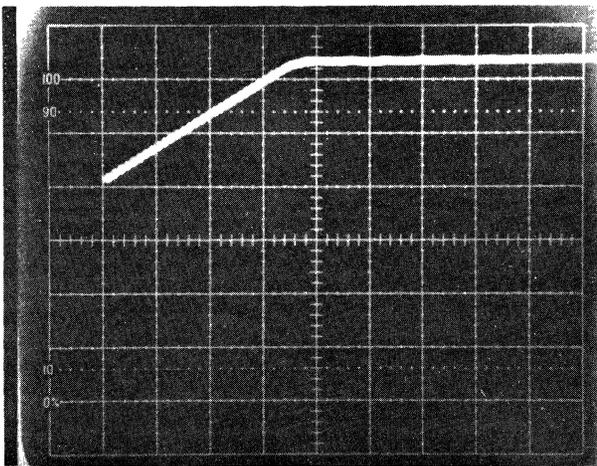
Figure 5-11   Reverse Acceleration Ramp

NOTE
TU16 ECO No. 10 must be installed in order to perform a write function with the TFG. Check against the following wire list, and install as necessary.

From	To
A3-K1	A2-C1
A2-C1	A2-E1
A2-E1	A2-F1
A2-F1	A2-J1
A2-J1	B2-H1
B2-H1	B2-J1
B2-J1	B2-P1
B2-P1	B2-R1
B2-R1	C2-M2

5.5.4 Tracking Check
Check industry-compatible tape tracking as follows:

a. Set up the TFG as follows:

   SSWRT, SSRD, and WRT: Down
   S5: 1-8 OFF
   S5: 9 and 10 ON
   S6: 1-10 OFF

b. Set the FWD/REV/REW switch to FWD. Place SSRD momentarily up, then down. (This loads data into the TFG write buffer.)

c. Position tape at BOT.

d. Place the WRT switch of the TFG up; press FWD and START on the control panel.

e. Allow the tape to be written for 10 seconds; ensure that the WRT indicator on the control panel is ON as the tape is being written.

f. Place the WRT switch down; rewind tape.

g. Remove the tape from the drive, take it to a work area, and proceed as follows:

   (1) Unwind tape until you reach the BOT marker; cut the tape with scissors.

   (2) Unwind 3 feet of tape beyond the BOT marker; cut the tape again.

   (3) Shake Magna-see solution vigorously.

   (4) Dip the 3-foot section of tape in Magna-see solution. (Refer to Figure 5-12.) Try to keep a loop of tape at the bottom of the can.

   (5) Work the tape back and forth until the entire 3-foot section (except for the ends being held) has been dipped into the solution.

   (6) Allow the tape to dry. Data written on the tape should appear as the solution dries. (See Figure 5-13.) If necessary, dip the tape again.

h. When the tape has been developed, proceed as follows:

   (1) Place the developed tape flat on a white background (e.g., white sheet of paper).

   (2) Make sure that the tape is flat, then place a weight on each end.

   (3) Check four points along the reference edge (edge with BOT marker) 1½ inches apart.

7660-24

Figure 5-12   Developing Magnetic Tape

RECORDED TRACKS (9)

INTERTRACK GAPS (8)
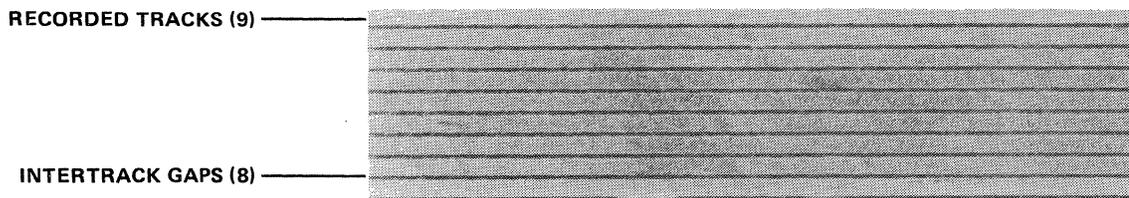
7660-27

Figure 5-13   Developed Magnetic Tape

(4) Set up microscope according to Figure 5-14; lay the penlight flat on the table, positioned so that it shines on the reflector.

(5) Ensure a distance of 0.007 ± 0.003 inches from the reference edge to track 1 (inset in Figure 5-14) at each of the four points mentioned in step (3), above.

NOTE
If the tracking check described above fails, tape path alignment must be performed at this time. (See Paragraph 4.17)

i. Install a new BOT marker 15 feet from the front of the tape on the non-oxide side, against the reference edge. (The reference edge faces the operator when the tape is installed on the transport.)

5.5.5   Erase Head Check
Check the erase head function as follows:

a. Load the tape and position it at BOT.

b. Set up TFG as follows:

   SSWRT, SSRD, and WRT: Down.
   S5: 1-8 OFF

5-11

RECORDED TRACK REFERENCE EDGE MICROSCOPE PENLIGHT

TRANSPARENT CASE REFLECTOR TAPE

7660-28

Figure 5-14   Track No. 1 to Reference Edge Measurement

S5: 9 and 10 ON
S6: 1-10 OFF

c.   Set the FWD/REV/REW switch to FWD. Place SSRD momentarily up, then down.

d.   Place the WRT switch on the TFG up; press FWD and START on the control panel. Allow tape to be written for 30 seconds.

NOTE

Steps a through d, above, are recording an all-1s tape at low density (full saturation). The steps below check the ability of the TU16 to erase a saturated tape.

e.   Press STOP on the control panel. Place the WRT switch down. Rewind tape.

f.   Set up the TFG as follows:

SSWRT, SSRD, and WRT: Down.
S5: 9 and 10 OFF
S4: 1-8 ON
S4: 9 and 10 OFF
S5: 1-8 ON
S6: 1-10 ON

g.   Press FWD on control panel and place SSWRT on the TFG up; allow tape to be written for 1 minute.

h.   Lower SSWRT switch; rewind tape.

i.   Set up oscilloscope as follows:

Channel 1 = 50 mV/cm
1 ms/cm
Triggering: Auto, Channel 1 triggered
Channel 1 probe on A4-L1
Channel 1 probe ground on B4-C2.

j.   Press FWD and START on control panel.

k.   Measure unerased signal level for maximum level. (Ensure good scope ground.) Maximum level must be less the 300 mV. Failure of this check will require replacement of the head plate assembly. (Tape path alignment under Paragraph 4.17 must be performed at this time.) Figure 5-15 is an example of acceptable erasure.

l.   Rewind tape. Place Channel 1 scope probe on C4-L1. (Ensure good ground.) Initiate forward motion. Check unerased signal level (max = 300 mV).

m. Rewind tape. Place Channel 1 scope probe on F4-R1. (Ensure good ground.) Initiate forward motion. Check unerased signal level (max = 300 mV).

5-12

Figure 5-15   Unerased Signal

5.5.6   Read Amplifier Check

NOTE

Paragraphs 5.5.6, 5.5.7 and 5.5.8 require comparison of read amplifier outputs under varied conditions. Photocopy table 5-2, or prepare a similar table.
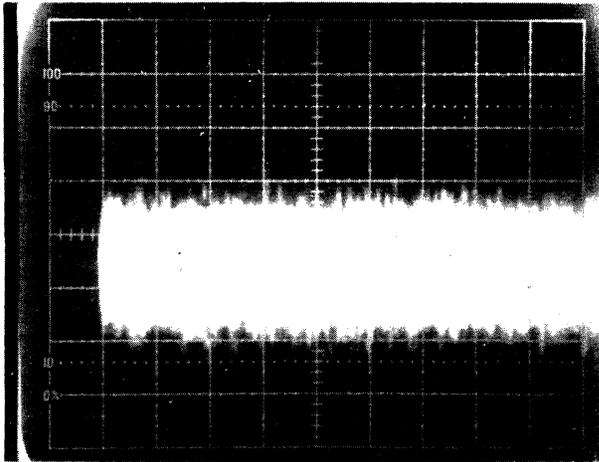
Check read amplifier outputs as follows:

a.   Rewind tape and remove from transport.

b.   Clean the read/write head, erase head, and tape cleaner.

c.   Load a good quality tape, positioned at BOT; set up the scope as follows:

   Channel 1 = 2 V/cm
   Sweep speed = 2 ms/cm
   Trigger = normal, Channel 1 triggered.

d.   Set the switches on the TFG as follows:

   S4: 1-8 ON
   S4: 9 and 10 OFF
   S5: 9 and 10 ON
   S5: 1-8 OFF
   S6: 1-8 OFF
   SSWRT, SSRD, and WRT: Down.

e.   Place the SSWRT switch in the TFG up and place Channel 1 probe on A4-L1. The scope presentation should resemble Figure 5-16.

f.   Increase vertical sensitivity to 1 V/cm and place interrecord gap 1 cm down from top. Measure negative half of read amplifier output (using the interrecord gap as the base-

Table 5-2
Read Amplitude, Residual Amplitude and Balance Checks

Track	Pin No.	Read Amplitude	Residual Amplitude	Reverse Balance Amplitude
1	A4-L1			
2	B4-B1		N/A	N/A
3	B4-M1		N/A	N/A
4	C4-K1		N/A	N/A
5	C4-L1			
6	D4-P1		N/A	N/A
7	D4-R1		N/A	N/A
8	F4-P1		N/A	N/A
9	F4-R1			

5-13

line). The peak amplitude of the negative-going signal should be from -4.45 to -4.75 V. (See Figure 5-17.) Record the results in the Read Amplitude column of Table 5-2, beside Track 1.

g. Repeat step f, above, for all nine tracks, recording the results in the same table. If any track is out of the acceptable range (-4.45 to -4.75 V), adjust all nine channels to -4.6 V. Such adjustment requires the following procedure:

(1) Turn power OFF.

(2) Take the TFG off the extender.

(3) Place G056 on extenders.

(4) Turn power ON.

(5) Adjust all read amplifiers to -4.6 V. (Potentiometers are arranged sequentially from top to bottom, starting with Track 1.)
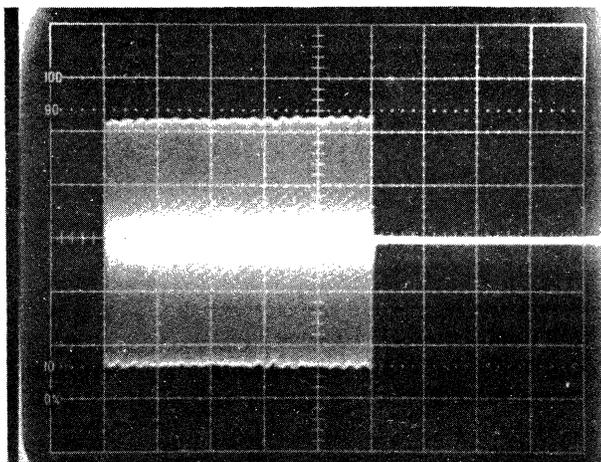
Figure 5-16   Read Amplifier Output

NOTE
If any channel cannot be adjusted within range, the TU16 input pre-amplifier resistors may have to be changed.

h. Place the SSWRT switch on the TFG down; rewind the tape.

5.5.7   Residual Amplitude Check
Perform residual amplitude check as follows: (Residual amplitude is the amplitude left on the tape after
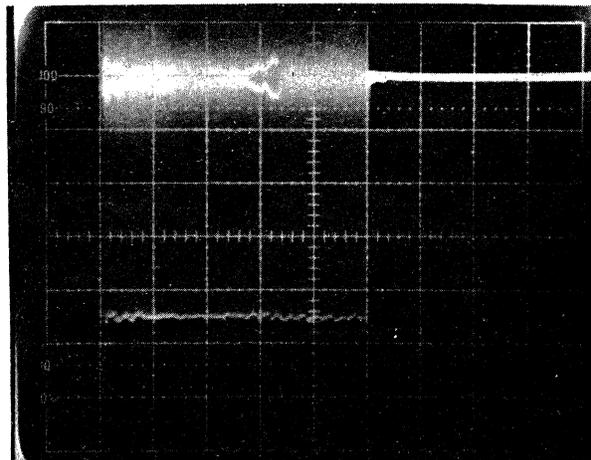
Figure 5-17   Negative Half of Read Amplifier Output

several read operations. Some amount of erasure can be expected during the first few read passes, due to residual magnetism in the write and erase heads.)

a. Press FWD; raise SSWRT. Allow start/stop data to be recorded for at least 20 seconds, then place SSWRT down and rewind tape.

b. Initiate FWD tape motion; allow the tape to run in forward direction for 10 seconds. Rewind tape. Repeat this operation ten times.

c. Leave scope setup as in Paragraph 5.5.6 above. Place the Channel 1 probe on A4-L1. Initiate FWD motion. Record the negative read amplifier output in the Residual Amplitude column of Table 5-2. Rewind tape.

d. Place the Channel 1 probe on C4-L1. Initiate FWD motion. Record the negative read amplifier output in the Residual Amplitude column of Table 5-2. Rewind tape.

e. Place the Channel 1 probe on F4-R1. Initiate FWD motion. Record the negative read amplifier output in the Residual Amplitude column of the table.

NOTE
It is assumed that tape did not run more than 10 seconds forward during steps c, d, and e, above. If there is any doubt of this, rewind tape and recheck forward residual amplitude.

f. Compare the entries in the Residual Amplitude column of the table with entries in the

5-14

Read Amplitude column. If the Residual Amplitude entries show a decrease of greater than 20 percent on any of the three tracks, replace the head plate assembly and perform a tape path alignment (Paragraph 4.17).

5.5.8 Reverse Balance Check

Perform the reverse balance check as follows:

a. Rewind tape.

b. Place Channel 1 probe on A4-L1; run tape FWD from BOT for 10 seconds. Initiate REV tape motion; record negative read amplifier output in the Reverse Amplitude column of Table 5-2.

c. Place Channel 1 probe on C4-L1; run tape FWD from BOT for 10 seconds. Initiate REV tape motion; record negative read am-

plifier output in the Reverse Balance Amplitude column of the table.

d. Place Channel 1 probe on F4-R1; run tape FWD from BOT for 10 seconds. Initiate REV tape motion; record negative read amplifier output in the Reverse Balance Amplitude column of the table.

e. Compare entries in the Reverse Balance Amplitude column of the table to the entries in the Residual Amplitude column. If the Reverse Amplitude entries show a decrease of greater than 10 percent, the tape path alignment must be performed (see Paragraph 4.17).

NOTE
Return to Paragraph 5.4.15 of the Quarterly PM Procedure.

DIGITAL EQUIPMENT CORPORATION **digital** WORLDWIDE SALES AND SERVICE

MAIN OFFICE AND PLANT

Maynard, Massachusetts, U.S.A. 01754 • Telephone: From Metropolitan Boston, 646-8600 • Elsewhere: (617)-897-5111
TWX: 710-347-0212 Cable: DIGITAL MAYN Telex: 94-8457

DOMESTIC

NORTHEAST

REGIONAL OFFICE:
235 Wyman Street, Waltham, Mass. 02154
Telephone: (617)-890-0330/0310   Dataphone: 617-890-3012 or 3013
CONNECTICUT
Meriden
240 Pomeroy Ave., Meriden, Conn. 06540
Telephone: (203)-237-8441/7466   Dataphone: 203-237-8205
Fairfield
1275 Post Road, Fairfield, Conn. 06430
Telephone: (203)-255-5991
NEW YORK
Rochester
130 Allens Creek Road, Rochester, New York
Telephone: (716)-461-1700   Dataphone: 716-244-1680
Syracuse
6700 Thompson Road, Syracuse, New York 13211
Telephone: (315)-437-1593/7085   Dataphone: 315-454-4152
MASSACHUSETTS
Marlborough
One Iron Way
Marlborough, Mass. 01752
Telephone: (617)-481-7400   Telex: 710-347-0348

MID-ATLANTIC

REGIONAL OFFICE:
U.S. Route 1, Princeton, New Jersey 08540
Telephone: (609)-452-2940
FLORIDA
Orlando
Suite 130, 7001 Lake Ellenor Drive, Orlando, Florida 32809
Telephone: (305)-851-4450   Dataphone: 305-859-2360
GEORGIA
Atlanta
2815 Clearview Place, Suite 100
Atlanta, Georgia 03040
Telephone: (404)-451-7411   Dataphone: 305-859-2360
NORTH CAROLINA
Durham/Chapel Hill
Executive Park
3700 Chapel Hill Blvd.
Durham, North Carolina 27707
Telephone: (919)-489-3347   Dataphone: 919-489-7832
NEW JERSEY
Fairfield
253 Passaic Ave., Fairfield, New Jersey 07006
Telephone: (201)-227-9280   Dataphone: 201-227-9280
Metuchen
95 Main Street, Metuchen, New Jersey 08840
Telephone: (201)-549-4100/2000   Dataphone: 201-548-0144

MID-ATLANTIC (cont.)

Princeton
U.S. Route 1, Princeton, New Jersey 08540
Telephone: (609)-452-2940   Dataphone: 609-452-2940
NEW YORK
Long Island
1 Huntington Quadrangle
Suite 1507 Huntington Station, New York 11746
Telephone: (516)-694-4131, (212)-895-8095
Dataphone: 516-293-5693
Manhattan
810 7th Ave., 22nd Floor
New York, N.Y. 10019
Telephone: (212)-582-1300
PENNSYLVANIA
Philadelphia
Digital Hall
1740 Walton Road, Blue Bell, Pennsylvania 19422
Telephone: (215)-825-4200
TENNESSEE
Knoxville
6311 Kingston Pike, Suite 21E
Knoxville, Tennessee 37919
Telephone: (615)-588-6571   Dataphone: 615-584-0571
WASHINGTON D.C.
Lanham 30 Office Building
4900 Princess Garden Parkway, Lanham, Maryland
Telephone: (301)-459-7900   Dataphone: 301-459-7900 X53

CENTRAL

REGIONAL OFFICE:
1850 Frontage Road, Northbrook, Illinois 60062
Telephone: (312)-498-2500   Dataphone: 312-498-2500
Ex. 78
INDIANA
Indianapolis
21 Beachway Drive, Suite G
Indianapolis, Indiana 46224
Telephone: (317)-243-8341   Dataphone: 317-247-1212
ILLINOIS
Chicago
1850 Frontage Road
Northbrook, Illinois 60062   Dataphone: 312-498-2500
LOUISIANA
New Orleans
3100 Ridgelake Drive, Suite 108
Metairie, Louisiana 70002
Telephone: (504)-837-0257   Dataphone: 504-833-2800

CENTRAL (cont.)

MICHIGAN
Ann Arbor
230 Huron View Boulevard, Ann Arbor, Michigan 48103
Telephone: (313)-761-1150   Dataphone: 313-769-9883
Detroit
23777 Greenfield Road
Suite 189
Southfield, Michigan 48075   Dataphone: 313-557-3063
MINNESOTA
Minneapolis
8030 Cedar Ave. South, Minneapolis, Minnesota 55420
Telephone: (612)-854-6562-3-4-5   Dataphone: 612-854-1410
MISSOURI
Kansas City
12401 East 43rd Street, Independence, Missouri 64055
Telephone: (816)-252-2300   Dataphone: 816-461-3100
St. Louis
Suite 110, 115 Progress Parkway
Maryland Heights, Missouri 63043
Telephone: (314)-878-4310   Dataphone: 816-461-3100
OHIO
Cleveland
2500 Euclid Avenue, Euclid, Ohio 44117
Telephone: (216)-946-8484   Dataphone: 216-946-8477
Dayton
3101 Kettering Boulevard
Dayton, Ohio 45439
Telephone: (513)-294-3323   Dataphone: 513-298-4724
OKLAHOMA
Tulsa
3140 S. Winston
Winston Sq. Bldg., Suite 4, Tulsa, Oklahoma 74135
Telephone: (918)-749-4476   Dataphone: 918-749-2714
PENNSYLVANIA
Pittsburgh
400 Penn. Center Boulevard, Pittsburgh, Pennsylvania 15235
Telephone: (412)-243-9404   Dataphone: 412-824-9730
TEXAS
Dallas
Plaza North, Suite 513
2880 LBJ Freeway, Dallas, Texas 75234
Telephone: (214)-620-2051   Dataphone: 214-620-2061
HOUSTON
6656 Hornwood Drive
Monterey Park, Houston, Texas 77036
Telephone: (713)-777-3471   Dataphone: 713-777-1071
WISCONSIN
Milwaukee
8531 West Capitol Drive, Milwaukee, Wisconsin 53222
Telephone: (414)-463-9110   Dataphone: 414-463-9115

WEST

REGIONAL OFFICE:
310 Soquel Way, Sunnyvale, California 94086
Telephone: (408)-735-9200   Dataphone: 408-735-1820
ARIZONA
Phoenix
4358 East Broadway Road, Phoenix, Arizona 85040
Telephone: (602)-268-3488   Dataphone: 602-268-7371
CALIFORNIA
Santa Ana
2110 S. Anne Street, Santa Ana, California 92704
Telephone: (714)-979-2460   Dataphone: 714-979-7850
San Diego
6154 Mission Gorge Road
Suite 110, San Diego, California
Telephone: (714)-280-7880/7970   Dataphone: 714-280-7825
San Francisco
1400 Terra Bella, Mountain View, California 94040
Telephone: (415)-964-6200   Dataphone: 415-964-1436
Oakland
7850 Edgewater Drive, Oakland, California 94621
Telephone: (415)-635-5453/7830   Dataphone: 415-562-2160
West Los Angeles
1510 Cotner Avenue, Los Angeles, California 90025
Telephone: (213)-479-3791/4318   Dataphone: 213-478-5626
COLORADO
7901 E. Bellevue Avenue
Suite 5, Englewood, Colorado 80110
Telephone: (303)-770-6150   Dataphone: 303-770-6628
NEW MEXICO
Albuquerque
10200 Menual N.E., Albuquerque, New Mexico 87112
Telephone: (505)-296-5411/5428   Dataphone: 505-294-2330
OREGON
Portland
Suite 168
5319 S.W. Westgate Drive, Portland, Oregon 97221
Telephone: (503)-297-3761/3765
UTAH
Salt Lake City
429 Lawn Dale Drive, Salt Lake City, Utah 84115
Telephone: (801)-487-4669   Dataphone: 801-467-0535
WASHINGTON
Bellevue
13401 N.E. Bellevue, Redmond Road, Suite 111
Bellevue, Washington 98005
Telephone: (206)-545-4058/455-5404   Dataphone: 206-747-3754

INTERNATIONAL

EUROPEAN HEADQUARTERS

Digital Equipment Corporation International Europe
81 route de l'Aire
1211 Geneva 26, Switzerland
Telephone: 42 79 50   Telex: 22 683

FRANCE

Digital Equipment France
Centre Silic — Cidex L 225
94533 Rungis, France
Telephone: 687-23-33   Telex: 26840
GRENOBLE
Digital Equipment France
Tour Mangin
16 Rue Du Gal Mangin
38100 Grenoble, France
Telephone: (76)-87-56-01   Telex: 212-32882

GERMAN FEDERAL REPUBLIC

Digital Equipment GmbH
MUNICH
8 Muenchen 13, Wallensteinplatz 2
Telephone: 0811-35031   Telex: 524-226
COLOGNE
5 Koeln 41, Aachener Strasse 311
Telephone: 0221-44-40-95   Telex: 888-2269
Telegram: Flip Chip Koeln
FRANKFURT
6078 Neu-Isenburg 2
Am Forstaus Gravebruch 5-7
Telephone: 06102-5526   Telex: 41-76-82
HANNOVER
3 Hannover, Podbielskistrasse 102
Telephone: 0511-69-70-95   Telex: 922-952
STUTTGART
D-7301 Kemnat, Stuttgart
Marco-Polo-Strasse 1
Telephone: (0771)-45-50-65   Telex: 841-722-393

AUSTRIA

Digital Equipment Corporation Ges.m.b.H.
VIENNA
Mariahilferstrasse 136, 1150 Vienna 15, Austria
Telephone: 85 51 86

UNITED KINGDOM

Digital Equipment Co. Ltd.
U.K. HEADQUARTERS
Fountain House, Butts Centre
Reading RG1 7QN, England
Telephone: (0734)-583555   Telex: 8483278
BIRMINGHAM
Maney Buildings
29/31 Birmingham Rd., Sutton Coldfield
Warwickshire, England
Telephone: 021-355-5501   Telex: 337-060
BRISTOL
Fish Ponds Road, Fish Ponds
Bristol, England BS163HQ
Telephone: Bristol 651-431
EALING
Bilton House, Uxbridge Road, Ealing, London W.5.
Telephone: 01-579-2334   Telex: 22371
EDINBURGH
Shiel House, Craigshill, Livingston,
West Lothian, Scotland
Telephone: 32705   Telex: 727113
LONDON
Management House
43 Parker St., Holborn, London
WC 2B 5PT, England
Telephone: 01-405-2614/4067   Telex: 27560
MANCHESTER
Arndale House
Chester Road, Stretford, Manchester M32 9BH
Telephone: (061)-865-7011   Telex: 668666

UNITED KINGDOM (cont.)

READING
Fountain House, Butts Centre
Reading RG1 7QN, England
Telephone: (0734)-583555   Telex: 8483278

NETHERLANDS

Digital Equipment N.V.
THE HAGUE
Sir Winston Churchillian 370
Rijswijk/The Hague, Netherlands
Telephone: 94 9220   Telex: 32533

BELGIUM

Digital Equipment N.V./S.A.
BRUSSELS
108 Rue D'Arlon
1040 Brussels, Belgium
Telephone: 02-139256   Telex: 25297

SWEDEN

Digital Equipment AB
STOCKHOLM
Englundavagen 7, 171 41 Solna, Sweden
Telephone: 98 13 90   Telex: 170 50
Cable: Digital Stockholm

NORWAY

Digital Equipment Corp. A/S
OSLO
Trondheimsveien 47
Oslo 5, Norway
Telephone: 02/68 34 40   Telex: 19079 DEC N

DENMARK

Digital Equipment Aktiebolag
COPENHAGEN
Hellerupveg 66
2900 Hellerup, Denmark

FINLAND

Digital Equipment AB
HELSINKI
Titismaantie 6
SF-00710 Helsinki 71
Telephone: (090) 370133
Cable: Digital Helsinki

SWITZERLAND

Digital Equipment Corporation S.A.
GENEVA
20, Quai Ernest Ansermet
Boite Postale 23, 1211 Geneva 8, Switzerland
Telephone No. 022 20 40 20 and 20 58 93 and 20 68 93
Telex: 28 92 01
ZURICH
Digital Equipment Corp. AG
Schaffhauserstr. 315
CH-8050 Zurich, Switzerland
Telephone 01-46-41-91   Telex: 56059

ITALY

Digital Equipment S.p.A.
MILAN
Corso Garibaldi 49, 20121 Milano, Italy
Telephone: (02)-879-051/2/3/4/5   Telex: 843-33615

SPAIN

Digital Equipment Corporation Ltd.
MADRID
Ataio Ingenieros S.A , Enrique Larreta 12, Madrid 16
Telephone: 215 35 43   Telex: 27249
BARCELONA
Ataio Ingenieros S.A., Granduxer 76, Barcelona 6
Telephone: 221 44 66

ISRAEL

DEC Systems Computers Ltd.
TEL AVIV
Suite 103, Southern Habakuk Street
Tel Aviv, Israel
Telephone: (03) 443114/440763   Telex: 922-33-3163

CANADA

Digital Equipment of Canada, Ltd.
CANADIAN HEADQUARTERS
P.O. Box 11500
Ottawa, Ontario, Canada
K2H 8K8
Telephone: (613)-592-5111   TWX: 610-562-8732
TORONTO
2550 Goldenridge Road, Mississauga, Ontario
Telephone: (416)-270-9400   TWX: 610-492-7118
MONTREAL
9045 Cote De Liesse
Dorval, Quebec, Canada H9P 2M9
Telephone: (514)-636-9393   Telex: 610-422-4124
CALGARY/Edmonton
Suite 140, 6940 Fisher Road S.E.
Calgary, Alberta, Canada
Telephone: (403) 435-4881   TWX: 403-255-7408
VANCOUVER
Suite 202
644 S.W. Marine Dr., Vancouver
British Columbia, Canada V6P 5Y1
Telephone: (604)-325-3231   Telex: 610-929-2006

GENERAL INTERNATIONAL SALES

REGIONAL OFFICE
146 Main Street, Maynard, Massachusetts 01754
Telephone: (617) 897-5111
From Metropolitan Boston, 646-8600
TWX: 710-347-0217/0212
Cable: DIGITAL MAYN
Telex: 94-8457

AUSTRALIA

Digital Equipment Australia Pty. Ltd.
ADELAIDE
6 Montrose Avenue
Norwood, South Australia 5067
Telephone: (08)-42-1339   Telex: 790-82825
BRISBANE
133 Leichhardt Street
Spring Hill
Brisbane, Queensland, Australia 4000
Telephone: (072)-293088   Telex: 790-40616
CANBERRA
27 Collie St.
Fyshwick, A.C.T. 2609 Australia
Telephone: (062)-959073
MELBOURNE
60 Park Street, South Melbourne, Victoria 3205
Australia
Telephone: (03)-699-2888   Telex: 790-30700
PERTH
643 Murray Street
West Perth, Western Australia 6005
Telephone: (092)-21-4993   Telex: 790-92140
SYDNEY
P.O. Box 491, Crows Nest
N.S.W. Australia 2065
Telephone: (02)-439-2566   Telex: 790-20740

NEW ZEALAND

Digital Equipment Corporation Ltd.
AUCKLAND
Hilton House, 430 Queen Street, Box 2471
Auckland, New Zealand
Telephone: 75533

JAPAN

Digital Equipment Corporation International
Kowa Building No. 16 — Annex, First Floor
9-20 Akasaka 1-Chome
Minato-Ku, Tokyo 107, Japan
Telephone: 586-2771   Telex: J-26428
Rikei Trading Co., Ltd. (sales only)
Kozato-Kaikan Bldg.
No. 18-14 Nishishimbashi 1-Chome
Minato-Ku, Tokyo, Japan
Telephone: 5915246   Telex: 781-4208

PUERTO RICO

Digital Equipment Corporation De Puerto Rico
407 del Parque Street
Santurce, Puerto Rico 00912
Telephone: (809)-723-8068/67   Telex: 385-9056

ARGENTINA

BUENOS AIRES
Coasin S.A.
Virrey del Pino, 4071, Buenos Aires
Telephone: 52-3185   Telex: 012-2284

BRAZIL

RIO DE JANEIRO — GB
Ambriex S.A.
Rua Ceará, 104, 2 e 3 andares ZC - 29
Rio De Janeiro — GB
Telephone: 264-7406/0461/7625
SAO PAULO
Ambriex S.A.
Rua Tupi, 535
Sao Paulo — SP
Telephone: 52-7806/1870, 51-0912
PORTO ALEGRE — RS
Rua Coronel Vicente 421/101
Porto Alegre — RS
Telephone: 24-7411

CHILE

SANTIAGO
Coasin Chile Ltda. (sales only)
Casilla 14588, Correo 15,
Telephone: 396713   Cable: COACHIL

INDIA

BOMBAY
Hinditron Computers Pvt. Ltd.
69/A, L. Jagmohandas Marg.
Bombay-6 (WB) India
Telephone: 38-1615: 36-5344   Telex: 011-2594 Plenty
Cable: TEKHIND

MEXICO

MEXICO CITY
Mexitek, S.A.
Eugenia 408 Deptos. 1
Apdo. Postal 12-1012
Mexico 12, D.F.
Telephone: (905) 536-09-10

PHILIPPINES

MANILA
Stanford Computer Corporation
P.O. Box 1608
416 Dasmarinas St., Manila
Telephone: 49-68-96   Telex: 742-0352

VENEZUELA

CARACAS
Coasin, C.A.
Apartado 50939
Sabana Grande No. 1, Caracas 105
Telephone: 72-8662; 72-9637
Cable: INSTRUVEN