RJS04/RJS03
fixed-head disk system
maintenance manual

pdp11

digital

DEC-11-HRJSA-B-D

RJS04/RJS03
fixed-head disk system
maintenance manual

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CONTENTS

		Page
CHAPTER 1	**SYSTEM AND PHYSICAL DESCRIPTION**	
1.1	GENERAL	1-1
1.1.1	Scope	1-1
1.1.2	Related Documentation	1-1
1.2	DISK FILE SYSTEM	1-1
1.2.1	Unibus	1-1
1.2.2	Massbus	1-3
1.3	RH11 CONTROLLER	1-3
1.3.1	Register and Control Path	1-4
1.3.2	DMA Data Path	1-4
1.3.2.1	Write Operation	1-4
1.3.2.2	Read Operation	1-6
1.3.2.3	Write-Check Data Transfer	1-6
1.3.2.4	Data Transfer Rates	1-6
1.4	RS04/RS03 DISK FILE	1-8
1.5	RJS04 and RJS03 SPECIFICATIONS	1-8
1.5.1	Unibus NPR Latency	1-8
1.5.2	Data Format	1-9
1.5.3	Error Detection and Signaling	1-9
1.5.4	RH11 Controller Specifications	1-9
1.5.5	RS04/RS03 Disk File Specifications	1-10
CHAPTER 2	**MASSBUS INTERFACE**	
2.1	GENERAL	2-1
2.2	DATA BUS	2-1
2.3	CONTROL BUS	2-1
2.4	COMMAND INITIATION	2-3
2.4.1	Non-Data Transfer Commands	2-3
2.4.2	Data Transfer Commands	2-4
2.5	MASSBUS PHYSICAL DESCRIPTION	2-4
CHAPTER 3	**OPERATION AND PROGRAMMING**	
3.1	GENERAL	3-1
3.2	DEFINITIONS	3-1
3.3	PROGRAMMING NOTES	3-3
3.4	INTERRUPT CONDITIONS	3-4
3.5	TERMINATION OF DATA TRANSFERS	3-4
3.6	CONTROL AND STATUS 1 (RSCS1) REGISTER (772040)	3-5
3.7	WORD COUNT (RSWC) REGISTER (772042)	3-7
3.8	UNIBUS ADDRESS (RSBA) REGISTER (772044)	3-8
3.9	DESIRED ADDRESS (RSDA) REGISTER (772046)	3-8
3.10	CONTROL AND STATUS 2 (RSCS2) REGISTER (772050)	3-9
3.11	DRIVE STATUS (RSDS) REGISTER (772052)	3-12
3.12	ERROR (RSER) REGISTER (772054)	3-14
3.13	ATTENTION SUMMARY (RSAS) REGISTER (772056)	3-16
3.14	LOOK-AHEAD (RSLA) REGISTER (772060)	3-17
3.15	DATA BUFFER (RSDB) REGISTER (772062)	3-17
3.16	MAINTENANCE (RSMR) REGISTER (772064)	3-18

CONTENTS

		Page
3.17	DRIVE TYPE (RSDT) REGISTER (772066)	3-21
3.18	RH11/RS04/RS03 REGISTER SUMMARY	3-22
3.19	FUNCTION CODES	3-22
3.19.1	No-Op, Function Code = 01_8	3-22
3.19.2	Drive Clear, Function Code = 11_8	3-22
3.19.3	Search, Function Code = 31_8	3-22
3.19.4	Write-Check, Function Code = 51_8	3-24
3.19.5	Write, Function Code = 61_8	3-24
3.19.6	Read, Function Code = 71_8	3-24
3.20	INTERRUPT VECTOR ADDRESS	3-24
3.21	INTERRUPT PRIORITY LEVEL	3-24
CHAPTER 4	**THEORY OF OPERATION**	
4.1	GENERAL	4-1
4.2	REGISTER CONTROL PATH	4-1
4.2.1	Writing a Local Register	4-1
4.2.2	Reading a Local Register	4-3
4.2.3	Writing a Remote Register	4-3
4.2.4	Reading a Remote Register	4-3
4.3	DMA DATA PATH	4-3
4.3.1	Write Block Transfer	4-7
4.3.2	Read Block Transfer	4-9
4.3.3	Write-Check Block Transfer	4-11
4.4	WRITE FLOW DIAGRAM DESCRIPTION	4-11
4.4.1	Unibus Flow Description	4-11
4.4.2	Massbus Flow Description	4-14
4.5	READ FLOW DIAGRAM DESCRIPTION	4-15
4.5.1	Massbus Flow	4-15
4.5.2	Unibus Flow	4-17
4.6	WRITE CHECK FLOW DIAGRAM DESCRIPTION	4-17
4.6.1	Massbus Flow Description	4-19
4.6.2	Unibus Flow Description	4-19
CHAPTER 5	**DETAILED LOGIC DESCRIPTION**	
5.1	GENERAL	5-1
5.2	BCTA LOGIC DIAGRAM	5-1
5.2.1	Local/Remote Register Selection	5-7
5.2.2	RSEL Signals	5-7
5.2.3	Decoder Inputs	5-7
5.2.4	Decoder Outputs	5-7
5.2.5	Word or Byte Addressing	5-8
5.2.6	Control Lines	5-8
5.2.7	ODD BYTE L Signal	5-8
5.2.8	Device Select (DEV SEL) Logic	5-8
5.2.9	Deskew Demand (DESK DEM)	5-8
5.2.10	Register Strobe (REG STR)	5-8
5.2.11	Control Out (CTRL OUT) Signal	5-8
5.2.12	Gate Control (GATE CNTL) Signal	5-8
5.3	LOGIC DIAGRAM BCTB	5-8

CONTENTS

		Page
5.3.1	Deskew Demand (DESK DEM) Logic	5-8
5.3.2	Response from Drive	5-8
5.3.3	SSYN Logic	5-9
5.3.4	Gating Address Onto Unibus	5-10
5.3.5	Data Buffer Out Clock	5-10
5.4	LOGIC DIAGRAM BCTC	5-10
5.4.1	Clocking Bus Address Register	5-11
5.4.2	Address Bit 00	5-11
5.4.3	Count Down (CNT DW) Flip-Flop	5-11
5.4.4	Bus Address Outputs	5-11
5.5	LOGIC DIAGRAM BCTD, BCTE	5-11
5.5.1	Word Count Registers	5-11
5.5.2	Word Count or Bus Address Selection	5-11
5.5.3	Clear Logic	5-12
5.5.4	Word Count Overflow	5-12
5.6	LOGIC DIAGRAM BCTF	5-12
5.6.1	Interrupt Request	5-12
5.6.2	Bus Request	5-12
5.6.3	Interrupt Done	5-13
5.7	LOGIC DIAGRAM BCTH	5-13
5.7.1	NPR Arbitration	5-13
5.7.2	Acquiring Bus Mastership	5-14
5.7.3	Completion of NPR Cycle	5-14
5.8	LOGIC DIAGRAM BCTJ	5-14
5.8.1	MB INIT Signal	5-14
5.8.2	Gating High Byte of CS1/CS2	5-14
5.8.3	MXF Error Flip-Flop	5-14
5.8.4	AC LO and DC LO	5-14
5.9	BCTK LOGIC DIAGRAM	5-15
5.10	LOGIC DIAGRAM CSRA	5-15
5.10.1	Data Transfer Command Logic	5-15
5.10.2	RUN Flip-Flop	5-16
5.10.3	BUSY Flip-Flop	5-16
5.10.4	Port Select Flip-Flop	5-17
5.10.5	CS1 Clocking Logic	5-17
5.10.6	Interrupt Requests	5-17
5.11	LOGIC DIAGRAM CSRB	5-17
5.11.1	CS2 Clocking Signals	5-17
5.11.2	Program Clear Bit	5-17
5.11.3	Bus Address Increment Inhibit	5-17
5.11.4	Unit Select Number	5-18
5.11.5	Parity Test Mode	5-18
5.11.6	Function Load	5-18
5.11.7	Non-Existent Device	5-18
5.11.8	Transfer Error	5-18
5.11.9	Program Error Flip-Flop	5-19
5.11.10	End of Sector (EOS) Flip-Flop	5-19
5.11.11	Unibus Parity Error (UPE) Flip-Flop	5-19
5.12	LOGIC DIAGRAM DBCA	5-19
5.12.1	NPC MASTER Signal	5-20

CONTENTS

		Page
5.12.2	ADDR TO BUS Signal	5-20
5.12.3	MSYN DESKEW	5-20
5.12.4	MSYN Inhibit Conditions	5-20
5.12.5	MSYN Timeout	5-21
5.12.6	DATA WAIT and MSYN WAIT One-Shot Multivibrators	5-21
5.12.7	CYCLE COUNT and NEXT CYCLE Flip-Flops	5-22
5.12.8	ERROR Conditions	5-22
5.12.9	1-Cycle Jumper	5-22
5.12.10	BUS HOG Mode	5-22
5.13	LOGIC DIAGRAM DBCB	5-23
5.13.1	Silo Input Logic	5-23
5.13.2	Silo Output Logic	5-24
5.13.3	Error Flip-Flop	5-26
5.13.4	Generation of INH CLK L	5-26
5.13.5	SILO CLR Generation	5-26
5.13.6	Write Clock	5-26
5.13.7	Gating Synchronous Data	5-26
5.13.8	Data Requests (Write Command)	5-26
5.13.9	Data Requests (Read or Write-Check)	5-26
5.13.10	NEXT SIGNAL (Write)	5-26
5.13.11	NEXT SIGNAL (Read or Write-Check)	5-27
5.13.12	Word Count Increment (Write Command)	5-27
5.13.13	Word Count Increment (Read or Write-Check)	5-27
5.13.14	EXCEPTION ERROR (Write Command)	5-27
5.13.15	EXCEPTION ERROR (Read or Write-Check)	5-27
5.14	LOGIC DIAGRAM DBCC	5-27
5.15	LOGIC DIAGRAM DBCD	5-28
5.16	LOGIC DIAGRAM DBCE	5-28
5.17	LOGIC DIAGRAM DBCF	5-28
5.18	LOGIC DIAGRAM DBCH	5-28
5.18.1	Parity Jumpers	5-29
5.18.2	74157 Parity Multiplexer	5-29
5.18.3	8234 Control Line/Data Buffer Multiplexing	5-29
5.19	LOGIC DIAGRAM DBCJ	5-29
5.19.1	Start Counter	5-29
5.19.2	CS1/CS2 Gating Onto BUSI	5-29
5.19.3	Voltage Regulator	5-29
5.20	M7297 PARITY CONTROL MODULE (PACA)	5-29
5.20.1	Synchronous Massbus Parity	5-29
5.20.2	Read or Write-Check Parity	5-30
5.20.3	Write Parity	5-30
5.20.4	Asynchronous Massbus Parity	5-30
5.21	M5904 MASSBUS TRANSCEIVER MBSA, MBSB, MBSC	5-31
5.22	UNIBUS A CABLE DIAGRAM	5-31
5.23	UNIBUS B CABLE DIAGRAM	5-32
5.24	M9300 UNIBUS B TERMINATOR	5-32
5.24.1	NPR Arbitration and Issuance of NPG	5-32
5.24.2	Prevention of NO-SACK TIMEOUT	5-33
5.25	G727 GRANT CONTINUITY MODULE	5-33
5.26	M688 POWER FAIL DRIVER	5-33

CONTENTS

		Page
5.27	M5904 MASSBUS TRANSCEIVER MODULE	5-35
5.27.1	75113 Dual Differential Driver Chip	5-35
5.27.2	75107B Dual Differential Line Receiver Chips	5-35
5.28	H870 TERMINATOR	5-37
5.29	M8838 UNIBUS TRANSCEIVER MODULE	5-37
5.30	UNIBUS TERMINATION	5-37
CHAPTER 6	**INSTALLATION AND MAINTENANCE**	
6.1	INTRODUCTION	6-1
6.2	INSTALLATION	6-1
6.2.1	Mechanical	6-1
6.2.2	Electrical	6-1
6.2.2.1	Power Cable Connections	6-1
6.2.2.2	Unibus Cable Connections	6-1
6.2.2.3	Massbus Cables	6-3
6.2.2.4	AC LO, DC LO	6-6
6.2.3	Small Peripheral Controller Slots	6-6
6.2.4	Jumper Configurations	6-6
6.2.4.1	BCT Module	6-6
6.2.4.2	DBC Module	6-10
6.2.4.3	CSR Module	6-10
6.3	VISUAL INSPECTION	6-10
6.4	RS04/RS03 ADD-ON INSTALLATION PROCEDURE	6-11
6.5	DIAGNOSTIC MAINTENANCE	6-12
6.5.1	Basic Function Test Diagnostic DZRSB	6-12
6.5.2	Data Reliability Diagnostic DZRSC	6-12
6.5.3	Diskless Diagnostic DZRSD	6-12
APPENDIX A	**INTEGRATED CIRCUIT DESCRIPTION**	

ILLUSTRATIONS

Figure No.	Title	Page
1-1	RH11 Simplified System Diagram	1-2
1-2	RH11 Multiport System	1-2
1-3	RH11 Combined With UNICHANNEL 15 System	1-3
1-4	RH11 Simplified Data Path Diagram	1-5
1-5	Effect of Sector Interleaving On UNIBUS Transfer Rate with Large Data Buffer	1-7
1-6	Read Data Transfer Sequence	1-7
1-7	Write Data Transfer Sequence	1-8
2-1	MASSBUS Interface Lines	2-2
3-1	Device Register Locations	3-2
3-2	Control & Status Register 1 Bit Usage	3-5
3-3	Word Count Register Bit Usage	3-7
3-4	UNIBUS Address Register Bit Usage	3-8
3-5	Desired Address Register Bit Usage	3-9
3-6	Control and Status Register 2 Bit Usage	3-9

ILLUSTRATIONS (Cont)

Figure No.	Title	Page
3-7	Drive Status Register Bit Usage	3-12
3-8	Error Register Bit Usage	3-14
3-9	Attention Summary Register Bit Usage	3-16
3-10	Look-Ahead Register Bit Usage	3-17
3-11	Data Buffer Bit Usage	3-18
3-12	Maintenance Register Bit Usage	3-18
3-13	Drive Type Register Bit Usage	3-21
3-14	RH11/RS04/RS03 Register Summary	3-23
4-1	Register Control Path	4-2
4-2	Writing Remote Register Interface	4-4
4-3	Reading Remote Register Interface	4-5
4-4	DMA Data Path Block Diagram	4-6
4-5	Write Cycle Interface Diagram	4-8
4-6	Read Cycle Interface Diagram	4-10
4-7	Write Check Cycle Interface Diagram	4-12
4-8	Write Command Flow Diagram	4-13
4-9	Read Command Flow Diagram	4-16
4-10	Write Check Command Flow Diagram	4-18
5-1	Write UNIBUS Timing Diagram	5-3
5-2	Read & Write Check UNIBUS Timing Diagram	5-4
5-3	Write MASSBUS Timing Diagram	5-5
5-4	Read & Write Check MASSBUS Timing Diagram	5-6
5-5	UNIBUS Power Fail Drivers Schematic	5-34
5-6	Typical Differential Driver/Receiver Connection	5-35
5-7	Driver Termination	5-35
5-8	Driver Chip Simplified Schematic	5-36
5-9	Dual Differential Driver Pin Connection Diagram	5-36
5-10	Simplified Line Receiver Logic Diagram	5-37
5-11	75107B Differential Receiver Pin Connection Diagram	5-37
5-12	M8838 UNIBUS Transceiver Pin Connection Diagram	5-38
6-1	RH11 Module Utilization	6-2
6-2	Single Port UNIBUS Configuration	6-4
6-3	Dual Port Configuration – Memory on UNIBUS B	6-4
6-4	Dual Port Configuration – Memory & Processor on UNIBUS B	6-5
6-5	MASSBUS Cable System Configuration	6-5
6-6	Typical Power Fail Configuration for RH11 & Options Mounted in Same Expander Box	6-7
6-7	Typical Power Fail Configuration for Two RH11s Mounted in Same Expander Box	6-8
6-8	Typical Power Fail Configuration for RH11 and CPU Mounted in Processor Box	6-9

TABLES

Table No.	Title	Page
1-1	Related Documentation	1-1
2-1	Massbus Signal Cable Designations	2-4
3-1	RH11 and RS04/RS03 Device Registers	3-1
3-2	Results of Program-Controlled Clearing	3-3
3-3	Control and Status 1 Register Bit Assignments	3-5
3-4	Word Count Register Bit Assignments	3-7
3-5	Unibus Address Register Bit Assignments	3-8
3-6	Desired Address Register Bit Assignments	3-9
3-7	Control and Status Register 2 Bit Assignments	3-10
3-8	Drive Status Register Bit Assignments	3-12
3-9	Error Register Bit Assignments	3-14
3-10	Attention Summary Register Bit Assignments	3-16
3-11	Look-Ahead Register Bit Assignments	3-17
3-12	Data Buffer Bit Assignments	3-18
3-13	Maintenance Register Bit Positions	3-19
3-14	Drive Type Register Bit Assignments	3-21
5-1	Listing of RH11 Logic Diagrams	5-2

CHAPTER 1
SYSTEM AND PHYSICAL DESCRIPTION

1.1 GENERAL

This manual describes the RJS04/RJS03 Fixed-Head Disk manufactured by Digital Equipment Corporation. The RJS04 system consists of an RH11 Device Controller and from one to eight RS04 disks. The RJS03 system consists of an RH11 Device Controller and from one to eight RS03 disks. The RH11 interfaces with any PDP-11 processor via the Unibus and controls one to eight RS04 or RS03 Fixed-Head Disk Files.

1.1.1 Scope

This manual is designed to provide Digital Field Service and customer maintenance personnel with sufficient installation, operation, and servicing information to install and maintain the RH11. Because the RH11 is used with the RS04 and the RS03 Fixed-Head Disk Files, a brief description of the RS04/RS03 is included in this manual. Detailed information on the RS04/RS03 can be found in the respective *RS04 and RS03 Maintenance Manuals.*

1.1.2 Related Documentation

Table 1-1 lists related documentation that supplements the information in this manual.

Table 1-1
Related Documentation

Title	Document Number
PDP-11 Peripherals Handbook	112.00973.2908
RS04 DECdisk Service Manual	DEC-00-HRS4A-A-D
RS03 DECdisk Service Manual	DEC-00-HRS3A-A-D
Digital Logic Handbook	058.00173.2505

1.2 DISK FILE SYSTEM

Figure 1-1 shows the major components of a PDP-11 system containing an RH11 Controller and one to eight disks. The processor and memory components can be any of several types in the PDP-11 family since all of these components are equipped with the standard Unibus interface. This manual describes the RH11 Device Controller as it interfaces with the RS04/RS03 disk drives.

1.2.1 Unibus

The Unibus provides the interface between the processor memory and the RH11 Controller. All data transfers between memory and the RH11 are accomplished via the NPR data transfer facilities of the Unibus.

The RH11 contains two Unibus ports: one designated as a control port and the second as a data port. Data may be transferred through either port using the NPR transfer facility. For normal operation, with memory connected to Unibus A as shown in Figure 1-1, the data port is not used, and the control port serves for both control and data transfers. When memory is connected to Unibus B, a programmable port select bit can cause data to be routed through the data port. Figure 1-2 shows a system configuration using multiport memory and both the control port and data port.

A third configuration which may be employed occurs in a multiprocessor environment. Figure 1-3 shows the RH11 system interfaced to a Unichannel 15 system and a remote processor. In this type of configuration, for example, the PDP-15 can direct the PDP-11 to transfer data from common memory to the disk. The data could then be transferred to another memory bank associated with the remote processor on Unibus B.

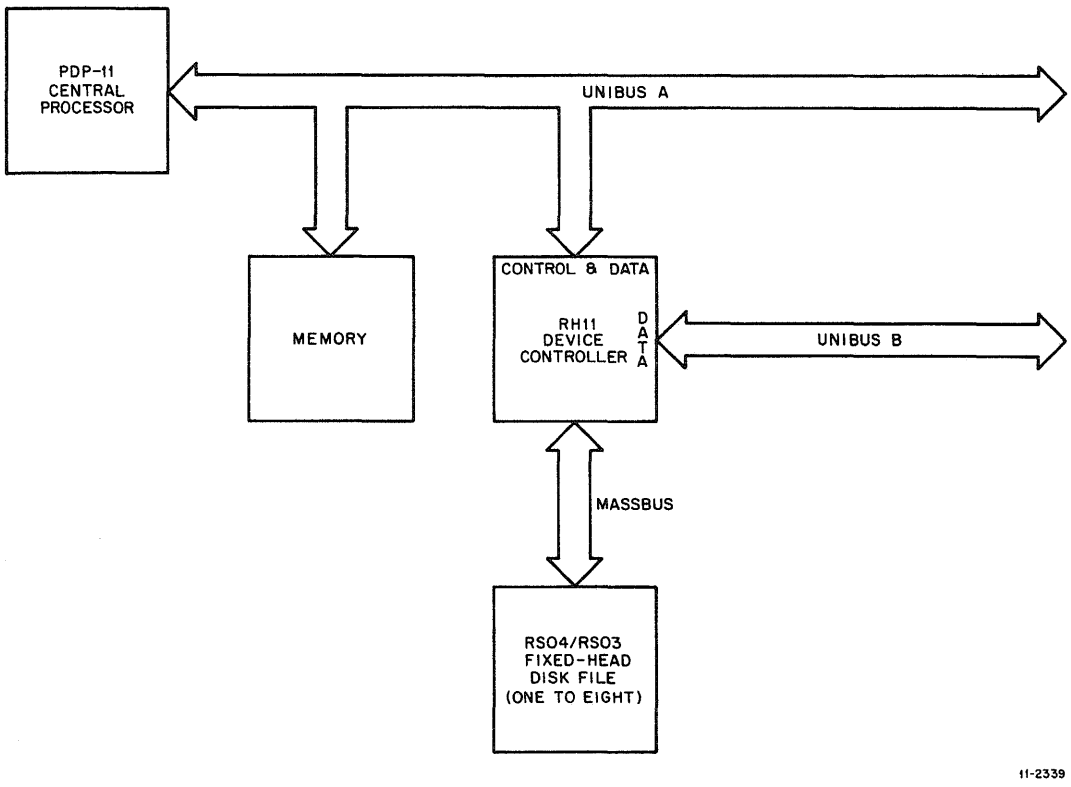


Figure 1-1 RH11 Simplified System Diagram

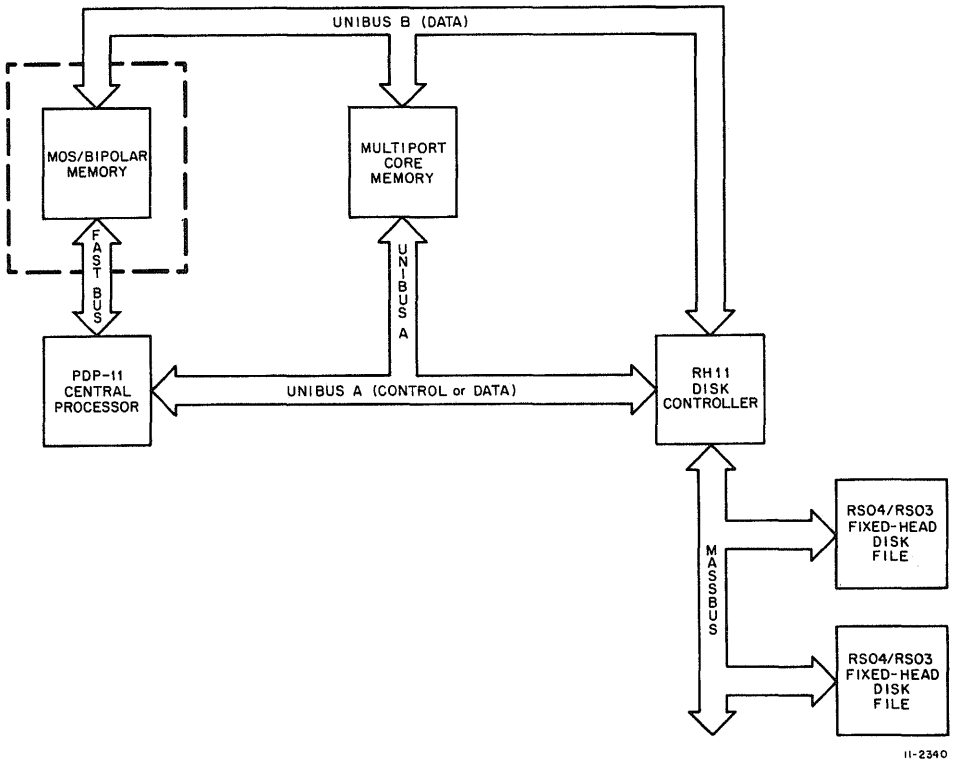


Figure 1-2 RH11 Multiport System

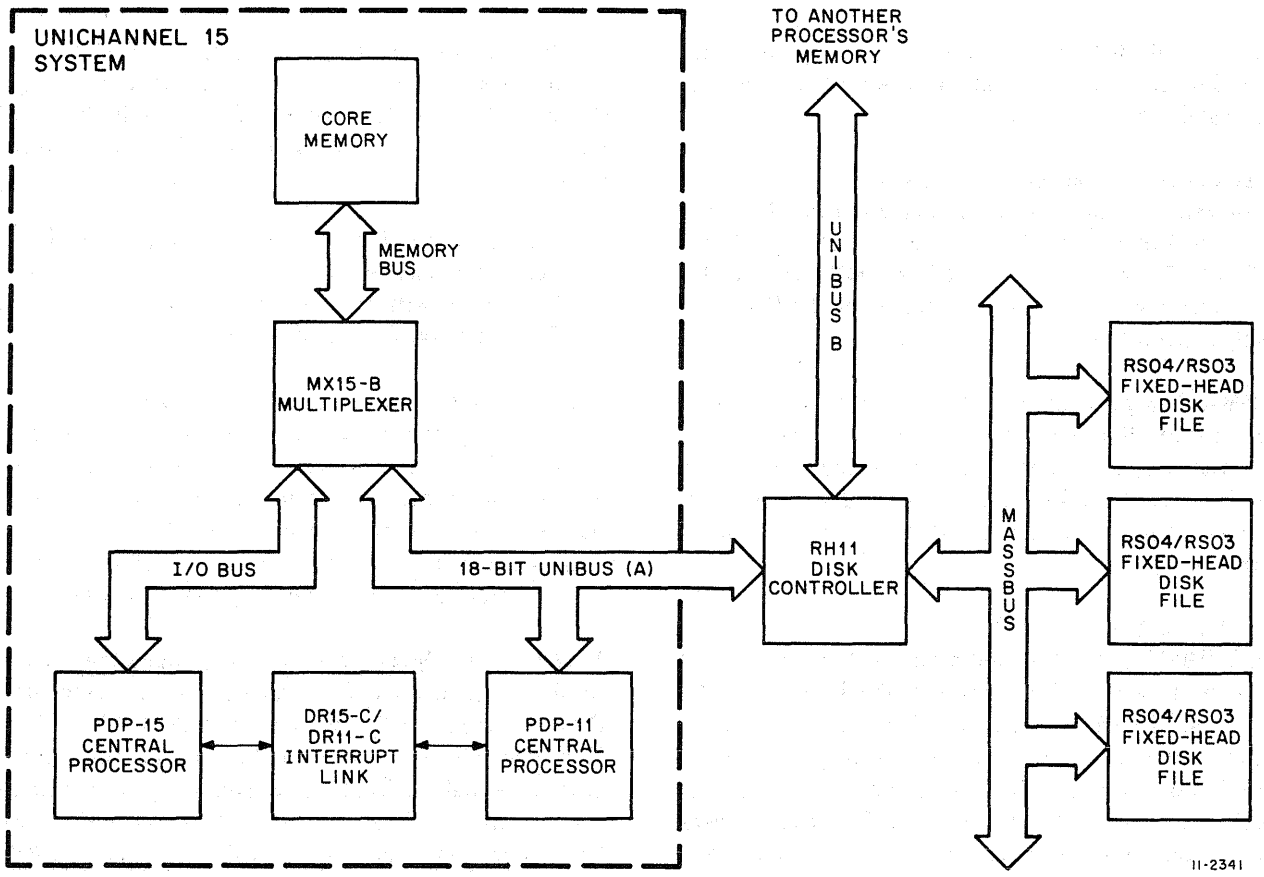


Figure 1-3 RH11 Combined With UNICHANNEL 15 System

1.2.2 Massbus

Massbus is the name of the interface between the RH11 Controller and the RS04/RS03 disk files. The Massbus provides a parallel data path between the RH11 and the disk devices, and has a maximum cable length of 120 ft, allowing 15 ft between drives if the daisy-chain configuration with a maximum of 8 disks is employed. The Massbus comprises two sections: an asynchronous control bus and a synchronous data bus for high-speed data transmission.

The purpose of the asynchronous control bus is to:

1. Transmit commands and information from the controller to the drive for the purpose of reading or writing drive registers
2. Notify the controller when an unusual (attention) condition exists in one or more drives
3. Transmit status information from the drive to the controller, and
4. Provide a master reset to all drives from the controller.

The purpose of the synchronous data bus is to transmit blocks of data at high speed between the controller and drives and to control the initiation and termination of block transmissions.

1.3 RH11 CONTROLLER

The RH11 Controller, in conjunction with the RS04/RS03, provides an extremely fast and reliable mass storage system that can be employed in timesharing or real-time data storage applications. The following major functions are performed by the RH11:

a. Interfaces with one or two Unibus cables and signals.

b. Communicates directly with the main memory in order to fetch and store data.

c. Communicates with the central processor in order to receive commands, provides error and status information, and generates interrupts.

d. Interfaces with one to eight drives.

The RH11 is divided into two major functional groups: the register and control path, and the DMA (direct memory access) data path (Figure 1-4).

The register access control path allows the program to read from or write into any register contained in the RH11 and the selected RS04/RS03. There are a total of 4 registers in the RH11, 7 registers in each RS04/RS03 drive, and 1 shared register which is partially contained in the RH11 and partially contained in the selected drive.

The DMA data path functionally consists of a 66-word X 18-bit first-in, first-out memory and associated control logic. The major function of this memory (hereafter referred to as the Silo) is to buffer data in order to compensate for fluctuations in NPR latency time on the Unibus.

1.3.1 Register and Control Path

When a PDP-11 instruction addresses the RH11 in order to read or write any device register in the RH11 or in the drive, a Unibus cycle is initiated and this data is routed to or from the RH11 (refer to Chapter 3 for a detailed description of the registers). If the register to be addressed is local (contained within the RH11), the register control logic immediately gates the data to or from the appropriate register. If the register to be accessed is remote (contained in one of the RS04/RS03 drives), the register control logic initiates a Massbus control bus cycle. Accesses to registers in a drive via the control bus do not interfere with DMA data transfers that may be going on at the same time. Local RH11 registers specify parameters such as bus address and word count while the drive registers specify parameters such as desired address, status information, etc.

1.3.2 DMA Data Path

The DMA data path functionally consists of the Massbus data bus, a Silo memory, and the Unibus NPR logic. The Silo memory compensates for fluctuations in NPR latency times by buffering data between the Unibus and Massbus data bus during DMA transfers.

Figure 1-4 shows a simplified block diagram of the DMA data path. A single Unibus configuration is shown with Unibus A serving as both the control port and the data port.

Three data transfer commands that can be performed by the RH11 and RS04/RS03 are Write, Read, and Write-check. Before these data transfers occur, the program specifies a memory address (MA), a desired address (DA), and a word count (WC). The memory address represents the starting memory location which the data will be written into or read from. This address occupies the 16 bits of the RSBA register and bits 9 and 8 of the RSCS1 register (Chapter 3). The state of the PSEL bit in the RSCS1 register determines over which Unibus the transfer will take place.

The desired address is the disk sector and track address and represents the starting location on the disk surface where the data is to be written or read from. This address occupies bits 11 through 00 in the RSDA register.

The word count is a count of the number of words to be transferred to or from the disk. The negative (2's complement) of this number is loaded in the word count (RSWC) register and is incremented toward 0 for each data word transferred into or from memory. At the normal completion of a transfer, the appropriate number of words have been transferred, and the RSWC register contains 0.

1.3.2.1 Write Operation – In a write operation, the data words are transferred from memory to the disk via the RH11. The data path functionally consists of the Unibus NPR logic, the Silo memory, and the Massbus data bus. The program initially selects a drive and loads the bus address, word count, and desired address. The program then loads a Write command code (with the GO bit set) into the RSCS1 Control and Status register. Unibus NPR cycles are initiated by the RH11, and the data words from memory are transferred to the input buffer (IBUF) of the Silo.

NOTE

The RH11 may perform either single cycle or back-to-back memory references per NPR request.

For each data word transferred, the word count is incremented by 1 and the bus address is incremented by 2. The data words are clocked into and "bubble" through the Silo. When the first data word reaches the top, it is automatically clocked into the Silo output buffer (OBUF). When the Silo is filled and a word is in OBUF, the RH11 asserts the RUN signal which signals the drive to begin writing data on the disk.

After the RUN signal is asserted, the disk begins searching for the rotational position corresponding to the value in the Desired Address (RSDA) register. When this rotational position is found, the disk begins sending SCLK pulses to the RH11 and starts receiving data words from the RH11 via the Massbus data bus.

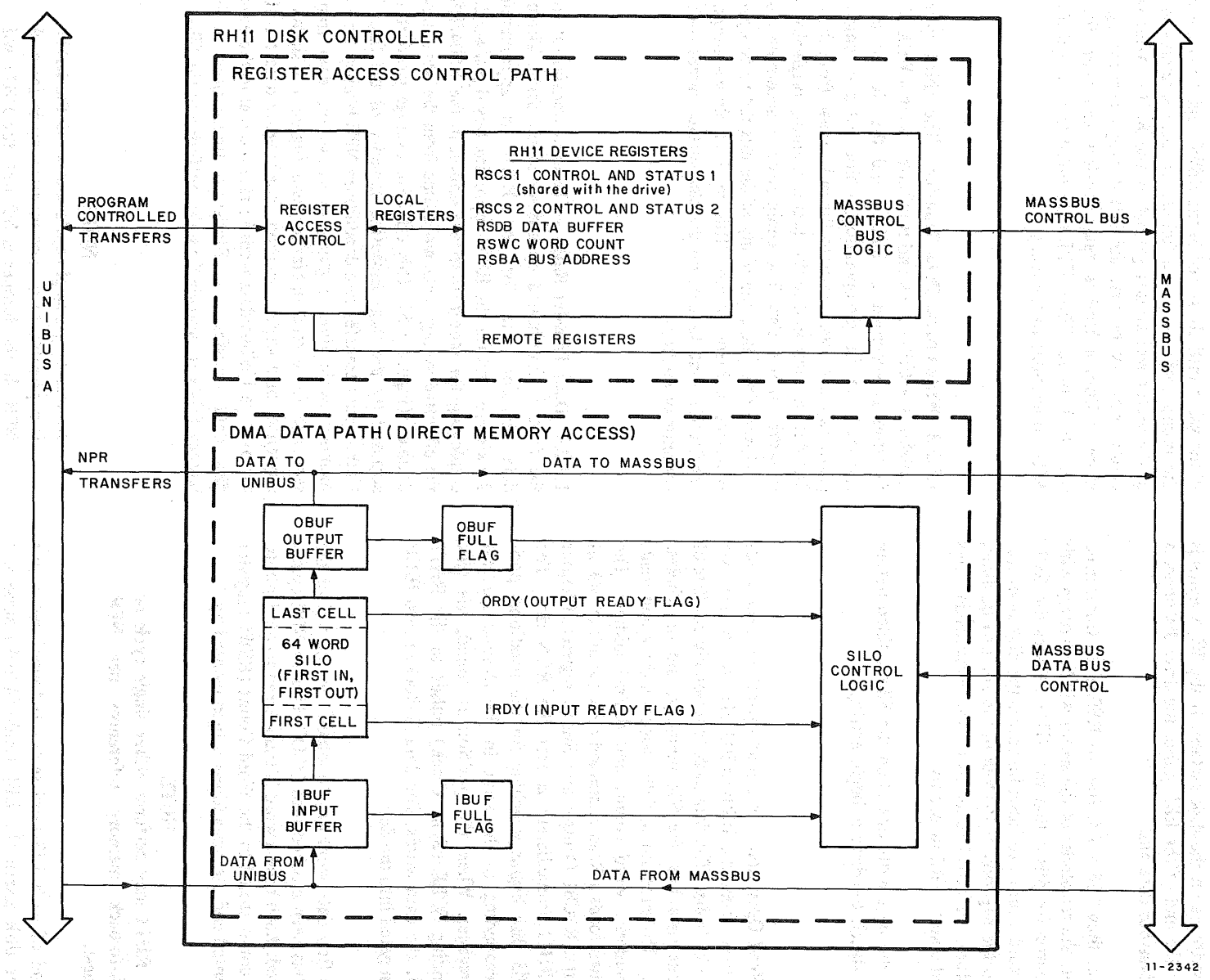


Figure 1-4 RH11 Simplified Data Path Diagram

At the end of each 128-word (64-word for the RS03) data block or sector, the disk asserts the EBL (end-of-block) pulse and looks at the RUN signal. If the RUN signal is still asserted, the disk continues to receive the next sector of data and writes it on the disk surface. If the RUN signal is negated at the end of the EBL pulse, the drive disconnects from the Massbus data bus.

When fewer than 128 words (64 for RS03) are transferred to a sector, the remainder of the sector will be written with 0s. The reason for this is that the RH11 negates the RUN signal at word count overflow; however, the disk does not respond to the negation of RUN until the end of EBL time, and therefore, the RH11 sends 0s on the Massbus data bus when word count overflow occurs.

Note that during a write operation the Silo is filled before the RH11 signals the drive to begin writing.

1.3.2.2 Read Operation – In a read operation, data words are transferred from the RS04/RS03 disk to memory via the RH11 Controller. The data path functionally consists of the Massbus data bus, the Silo memory, and the Unibus NPR logic. The program initially selects a drive and loads the bus address, word count, and desired address. The program then loads a Read command code (with the GO bit set) into the RSCS1 Control and Status register (Chapter 3). The RH11 immediately asserts the RUN line. The RS04/RS03 disk begins searching for the rotational position corresponding to the value in the Desired Address (RSDA) register. When the position is found, the disk begins sending SCLK (Sync Clock) pulses to the RH11 along with the data words. The data is clocked into IBUF and is then gated into the Silo.

When the first data word has "bubbled" to the top of the Silo and has been clocked into OBUF, Unibus NPR cycles are initiated. Each time a word is transferred to the Unibus, the word count stored in the Word Count (RSWC) register is incremented and the bus address is incremented by 2.

NOTE

The RH11 may perform either single cycle or back-to-back memory references per NPR request.

At the end of each 128-word sector (64-word sector for RS03), the disk asserts the EBL (end-of-block) pulse and looks at the RUN signal. If the RUN signal is still asserted, the disk continues sending the next sector of data to the RH11 via the Massbus data bus. If the RUN signal is negated at the end of the EBL pulse, the disk disconnects from the Massbus data bus and the transfer is terminated.

If the value initially stored in the RSWC register is less than the number of words in a full sector, the remaining words in the sector will be disregarded by the RH11. After word count overflow occurs, the RH11 stops performing any more additional Unibus data transfers and waits for the next EBL pulse. When EBL is received from the disk, the RH11 transitions to the ready state.

1.3.2.3 Write-Check Data Transfer – The third type of transfer is a Write-check and is initiated when a Write-check function is specified in RSCS1 and the GO bit in this register is set. In this operation, a block of data which has previously been written onto the disk is read from the disk. The data is compared to the data in memory originally used to write on the disk. The comparison is accomplished by Exclusive OR gates, and if any of the bits fail to compare, a Write-check Error occurs. This method allows automatic verification that the data on the disk surface agrees with the contents of memory.

1.3.2.4 Data Transfer Rates – The data transfer rate from the drive is determined by a clock in the drive. The basic data transfer rate for the RS04 is approximately 2 μ s/word, and for the RS03 approximately 4 μ s/word. By employing the sector interleave option in the RS04/RS03, the effective average data word time from the drive may be doubled (Figure 1-5). This effective average word time is achieved by the large buffering capacity of the Silo. The Unibus data transfer rate depends on NPR latency time and memory cycle time. Figure 1-6 shows the data transfer sequence for a read operation, and Figure 1-7 shows the sequence for a write operation. For lengthy data transfers, the average Unibus data transfer rate is equal to the average disk data transfer rate. Statistical fluctuations in NPR latency times are absorbed by the buffering in the Silo.

NOTE

By inserting a single-cycle jumper in the RH11, it is possible to do one memory cycle for each NPR. If the jumper is left out, the RH11 will perform either single or back-to-back memory cycles before releasing the Unibus.

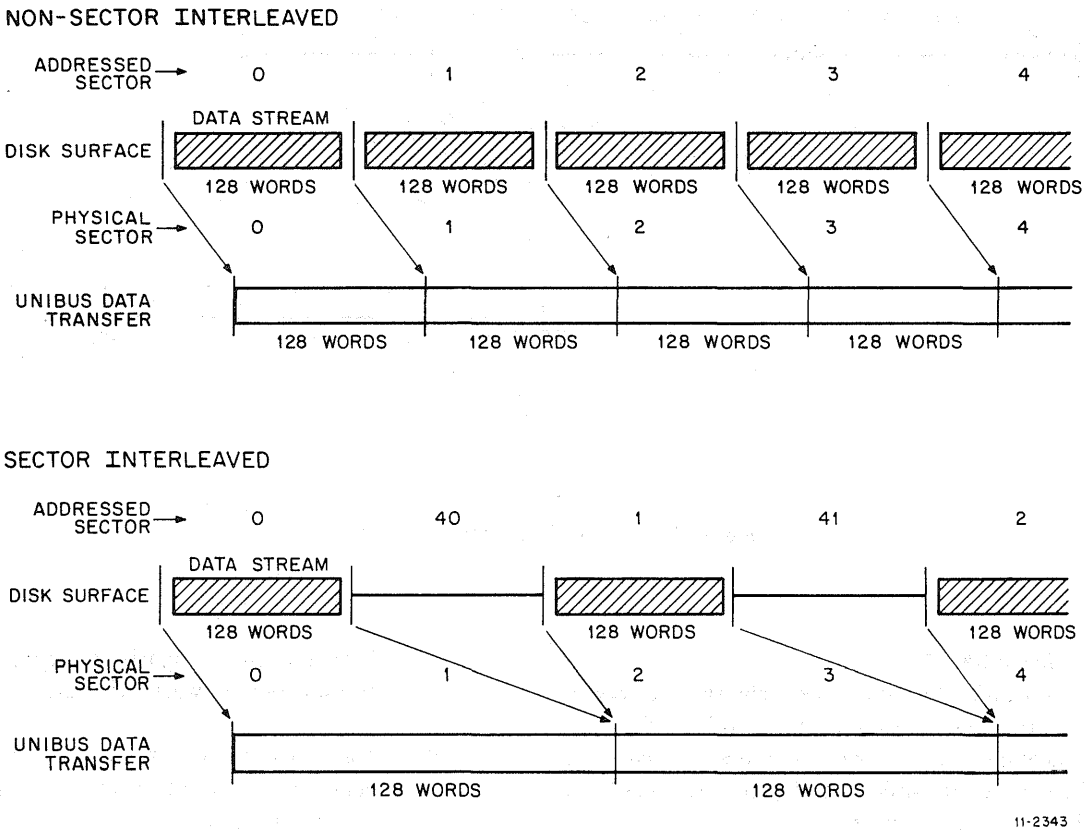
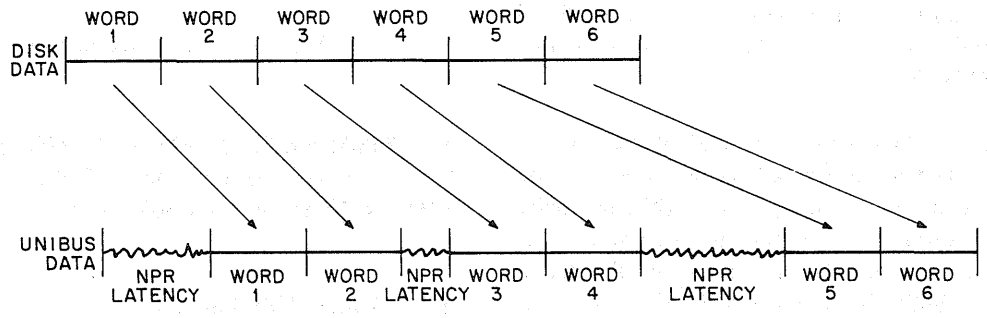


Figure 1-5 Effect of Sector Interleaving On UNIBUS Transfer Rate with Large Data Buffer



NOTE:
Data transfer rate is 4 μseconds/word for the RS03 and 2 μseconds/word for the RS04. With sector interleave option, the effective average word time increases to approximately 8 μseconds for the RS03 and 4 μseconds for the RS04.

Figure 1-6 Read Data Transfer Sequence

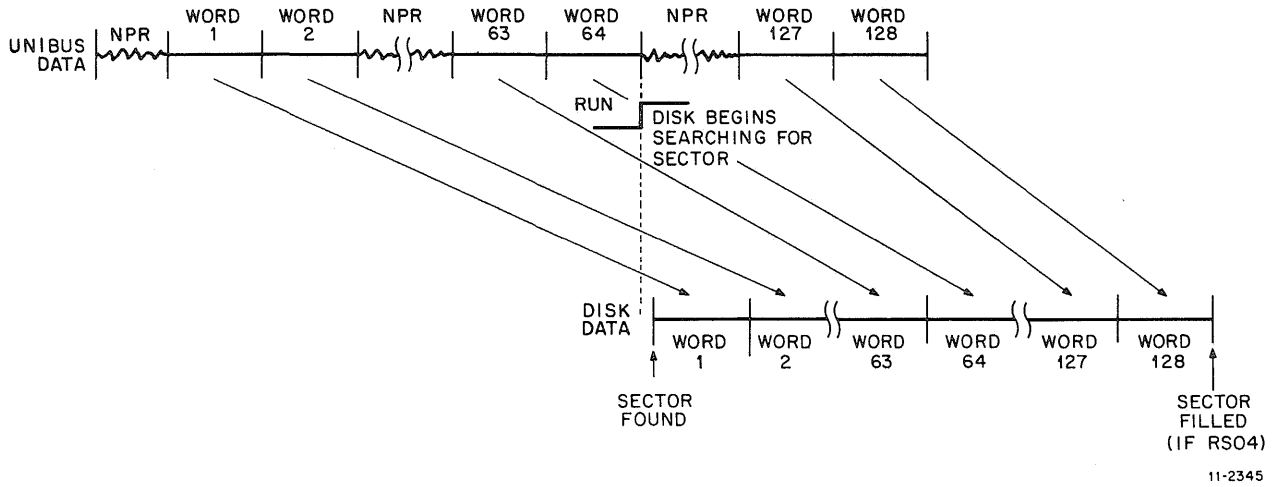


Figure 1-7 Write Data Transfer Sequence

1.4 RS04/RS03 DISK FILE

The RS04/RS03 disk files consist of a chassis assembly, a power supply assembly with power control, a disk and associated assembly, and a logic assembly housed in a 15-3/4 in. high by 19 in. wide rack. Up to three disks can be mounted in the standard cabinet.

The RS04/RS03 disks are 16 in. in diameter and are plated with nickel cobalt. Recording capacity is 512K words for the RS04 and 256K words for the RS03.

Information is recorded on the lower surface in the RS03 drive and on both the upper and lower surfaces simultaneously in the RS04 drive.

In other words, the RS04 records one half of the word on the lower surface and the other half on the upper surface. Therefore, for a constant recording density (bits per inch), recording on two surfaces rather than one doubles both the capacity and the transfer rate. The same angular sector length is used in both the RS04 and RS03, so that the RS04 contains twice as many words per sector as the RS03.

The RS04/RS03 drives perform the following functions:

a. Records and plays back data

b. Generates gaps and synchronization marks on the recording medium

c. Provides clock signals to synchronize data transmission between drive and controller

d. Maintains error and status indicators and generates an attention signal when exceptional conditions occur

e. Locates data by sector address

f. Provides mechanisms for maintenance and diagnostic testing

g. Performs error detection on the data.

1.5 RJS04 and RJS03 SPECIFICATIONS

This paragraph defines some of the parameters in the RH11/RS04 and RH11/RS03 systems.

1.5.1 Unibus NPR Latency

NPR latency time is from the assertion of a Unibus NPR by the RH11 until the RH11 takes control of the Unibus (asserts BBSY). The acceptable average NPR latency time is calculated as follows:

Average data word time of the disk minus time to transfer one word to or from memory plus the time for the RH11 to issue the next NPR.

If the jumper in the RH11 is cut for two memory cycles per NPR, average acceptable NPR latency time is doubled, and is calculated as follows:

> Twice the average data word time of the disk minus time to transfer two words to or from memory plus the time for the RH11 to issue the next NPR. Example: If the average data word time of the disk is 4 μs and the time to transfer two words to or from memory is 2 μs plus .2 μs to request the Unibus again, then the average acceptable NPR latency = $(2 \times 4)\ \mu s - (2 + .2)\ \mu s = 5.8\ \mu s$.

If the actual NPR latency consistently exceeds the acceptable average NPR latency during a lengthy read or write operation, the 66 words of data buffering in the RH11 will eventually fail to be sufficient. This condition is signaled by a Data Late Error (DLT) condition.

1.5.2 Data Format

Data words are recorded on the disk in 18-bit format. Normally, for the RH11/RS04 or RH11/RS03 system, only 16 bits are transmitted per word between the controller and memory. To accomplish an 18-bit transfer via the Unibus, the Bus PA and Bus PB lines may be used as data bits BUS D16 and BUS D17, respectively. Both Unibus A and Unibus B are jumper selectable in the RH11 for this 18-bit mode. When a Unibus is not selected for 18-bit mode, the RH11, when reading, sends logical 0s on the Unibus PA and Unibus PB lines, and when writing sends 0s to the disk in bits 16 and 17 of the Massbus data bus.

In addition, the RH11 checks parity error conditions on the Unibus in the normal 16-bit mode, when performing a write operation. A PDP-11 memory parity error is indicated when Unibus PA is negated and Unibus PB is asserted during an NPR data transfer from memory.

1.5.3 Error Detection and Signaling

The error detection method employed in the RS04/RS03 must detect burst errors as well as single bit errors. This is accomplished by the CRC logic in the drive. This logic calculates a block check word on writing the data and a second block check word on reading the data. If there are no errors, the block check word calculated during reading should contain all 0s.

During a read, write, or write-check operation, both data errors and unusual drive conditions signal the RH11 via the EXC line (Exception) which sets the TRE (Transfer Error) bit after the read/write operation is complete. During non-data transfer operations, the drive can signal unusual conditions or completion of non-data transfer operations by the Attention (ATTN) line. This line is shared by all drives connected to the RH11.

During a read, write, or write-check operation, errors in the RH11 (such as DLT, Unibus parity error, etc.) also set the TRE bit and cause the operation to be aborted.

Interrupts are generated as a result of the ATTN line being asserted or by completion of a read or write data transfer.

1.5.4 RH11 Controller Specifications

Mechanical

Consists of a double hex-height system unit, which will mount in a BA11-FA, BA11-FB, BA11-BA, or BA11-BB mounting box (not supplied). Module usage is as follows:

RH11 Logic –
2 hex-height, 2 double-height modules.
Massbus Controller Transceivers –
3 double-height modules.
Unibus Cable Slots –
4 double-height cable slots.
Power Fail –
2 single-height modules.
Small Peripheral Controller Slots (spares) –
3 quad-height module slots available.

Electrical

Power Requirements (RH11)
+5.0 ± 0.25 Vdc at 19.0 A max.
−15.0 ± 1.5 Vdc at 0.58 A max.

Logic Voltage
H ≈ +3 V, L ≈ 0 V

Power Requirements (Small Peripheral Controllers)
+5.0 ± 0.25 Vdc at up to 6.0 A max. for three small peripheral controllers

Also, −15 Vdc, LTC, & +15 Vdc are provided for SPC use.

Environmental
Temperature
32° – 122° F (0° – 50° C) Class C

Relative Humidity
Vibration Shock
8% to 90% RH, no condensation
1.89 G rms, 10–300 Hz
20 G, half sine, 30 ms duration, any plane

Data Transfers Memory/Controller
Accomplished via the NPR facility of the Unibus. Data can be transferred on either of two Unibuses (program selected). An 18-bit data path is optional (uses Unibus PA and Unibus PB lines as data).

Data Transfer Controller/Disk
All controller/disk transfers are accomplished as 18-bit parallel words over the synchronous section of the Massbus.

Data Rates
RS03
250 kHz 4 μs/word
RS03
(with sector interleave) 125 kHz 8 μs/word
RS04
500 kHz 2 μs/word
RS04
(with sector interleave) 250 kHz 4 μs/word

Number of Disks per Controller
Can handle up to 8 RS04 or RS03 disk files.

Maximum Controller/Drive Cable Length
120 ft max.

1.5.5 RS04/RS03 Disk File Specifications

The following specifications apply to both the RS04 and RS03 disk files. Differences in specifications between the drives are indicated.

Mechanical
Mounting – Mounted in a 19 in. rack. Each disk file requires 15-3/4 in. of panel height. Self contained power control and sequencing, dc power supply, and absolute air filter system. A total of three drives per cabinet is possible.

Electrical
Power Requirements
dc – None
ac 90 – 132 Vac at 50/60 Hz
180 – 264 Vac at 50/60 Hz
Starting current – 13 amps
Nominal current – 4 amps

Environmental
Temperature
32° – 122° F (0° – 50° C)

Humidity
20% to 80% RH, no condensation

Vibration
5–20 Hz 0.010 in. D.A.
20–500 Hz ± 1.5 G any plane.

Shock
5 G, half sine, 10 ms duration any plane.

Error Detection
16-bit CRC (cycle redundancy check) per sector

Error Rate
Recoverable error rate – less than one recoverable error in 1×10^{11} bit transfers.

Non-recoverable error rate – less than one error in 1×10^{12} bit transfers.

A recoverable error is defined as one in which the data is recovered correctly within three successive retries.

Recording Method
Three-frequency, Miller encoding, modified frequency modulation (mfm).

Maximum Access Time (3600 rpm)
17.0 ms for 60 Hz systems
20.4 ms for 50 Hz systems

Average Access Time
8.5 ms for 60 Hz systems
10.2 ms for 50 Hz systems

Minimum Access Time
(Disk Drive Only)
6.4 μs for 60 Hz systems
7.7 μs for 50 Hz systems

Data Transfer Rate

Jumper selectable at RS04 for 2 μs/word or 4 μs/word transfer rate. Jumper selectable at RS03 for 4 μs/word or 8 μs/word transfer rate. For slower transfer rates, sectors are interleaved. Read and write occur at the same data rate.

Disk Format

Logical tracks – 64

Spare tracks

RS04 – 16 (8 guaranteed good for read/write, 1 timing spare)

RS03 – 8 (4 guaranteed good for read/write, 1 timing spare)

Sector

64 per track (RS04 and RS03)

Words

64 per sector (RS04 = 128 per sector)

Bits

18 per word

Total Storage Capability per Drive

RS03

64 words/sector X 64 sectors/track X 64 tracks = 262, 144 words

RS04

128 words/sector X 64 sectors/track X 64 tracks = 524, 288 words

Total Storage Capability per Controller

(8 RS03 drives) – 262K X 8 = 2 Megawords

(8 RS04 drives) – 524K X 8 = 4 Megawords

RS04/RS03 Format Specifications

NOTE

The following specifications are applicable to both the RS04 and RS03 except as noted.

Clock Track

Recorded with 86,016 clock pulses at a nominal rate of 4.8 MHz (208 ns/bit). Gap of 250 ±50 μs duration recorded at 1/2 nominal rate (2.4 MHz).

Timing Signals Generated

Index Pulse – generated for duration of gap.

Resync – 512 bits following index to allow resynchronization of the phase-locked loop.

Sector Pulse – start after resync, 64 per revolution, duration 1 bit time, at 1334 bit time intervals.

Set sync – occurs 62 bit times after sector pulse to indicate sufficient preamble has been written or loop is locked and data may be read.

Data

A sector consists of 67 to 70 bits of "0s" preamble followed by a sync "1." For the RS04, this is followed by 128 9-bit half data words and an 8-bit half CRC word. For the RS03, this is followed by 64 18-bit data words plus a 16-bit CRC word. Dead band following data is 103 to 127 bits for the RS04 and 95 to 98 bits for the RS03. Total sector length = 1334 bits.

NOTE

Since data is recorded on two tracks in parallel, half of each data word is recorded on each track.

End of Track Dead Band

128 bits

Read/Write Timing

To read or write a sector, the address and command must be asserted and acknowledged prior to the trailing edge of the sector mark for that sector.

The first sync clock will be asserted greater than 6.4 μs after this edge. The End of Block (EBL) signal occurs during the "130th" word time. Duration is approximately 1.8 μs. The trailing edge is at least 11.6 μs prior to the next sector mark.

CHAPTER 2
MASSBUS INTERFACE

2.1 GENERAL

The Massbus provides the interface between the RH11 Controller and the RS04/RS03 disk files. The Massbus can be up to 120 ft in length and up to eight drives may be connected in a daisy-chain configuration. The Massbus consists of two sections – a data bus section and a control bus section. These buses are described in the following paragraphs.

2.2 DATA BUS

The data bus section of the Massbus consists of a 19-bit (18 data bits plus parity bit) parallel data path and six control lines (Figure 2-1).

Parallel Data Path – The parallel data path consists of an 18-bit data path designated D00 through D17 and an associated parity bit (DPA). The data path is bidirectional and employs odd parity. Data is transmitted synchronously, using a clock generated in the drive.

RUN – After a data transfer command has been written into the Control register of a drive, the drive connects to the data bus. The controller then asserts the RUN line to initiate the function. At the end of each sector on the trailing edge of the EBL (End-of-block) pulse, RUN is strobed by the drive. If it is still asserted, the function continues for the next sector; if it is negated, the function is terminated.

Occupied (OCC) – This signal is generated by the drive to indicate "data bus busy." As soon as a valid data transfer command is written into a drive, and the command is accepted, the drive asserts OCC. Various errors may cause a drive to be unable to execute a command. The controller will time out in these cases due to no assertion of OCC or of SCLK, and the MXF (Missed Transfer Error) will be set in the controller. OCC is negated at the trailing edge of the last EBL pulse of a transfer.

End-of-block (EBL) – This signal is asserted by the drive for one word time at the end of each sector (after the last SCLK pulse). For certain error conditions, where it is necessary to terminate operations immediately, EBL is asserted prior to the normal time for the last SCLK. The data transfer is terminated prior to the end of the sector in this case.

Exception (EXC) – This signal is asserted when an abnormal condition occurs in the drive. The drive asserts this signal to indicate an error during a data transfer command (Read, Write, or Write-check). Exception is asserted at or prior to assertion of EBL and is negated at the negation of EBL.

Sync CLK (SCLK), Write CLK (WCLK) – These signals are the timing signals used to strobe the data in the controller and/or in the drive. During a read operation, the RH11 strobes the data lines on the negation of SCLK and the drive changes the data on the assertion of SCLK. During a write operation, the controller receives SCLK and echoes it back to the drive as WCLK. On the assertion of WCLK, the drive strobes the data lines and on the negation of WCLK, the controller changes the data on the data lines.

2.3 CONTROL BUS

The control bus section of the Massbus consists of a 17-bit (16 bits plus parity) parallel control and status data path, and 14 control lines (Figure 2-1).

Parallel Control and Status Path – The parallel control and status path consists of a 16-bit parallel data path designated C00 through C15 and an associated parity bit (CPA). The control and status lines are bidirectional and employ odd parity.

Drive Select DS (2:0) – These three lines transmit a 3-bit binary code from the controller to select a particular drive. The drive responds when the (unit) select number in the drive corresponds to the transmitted binary code.

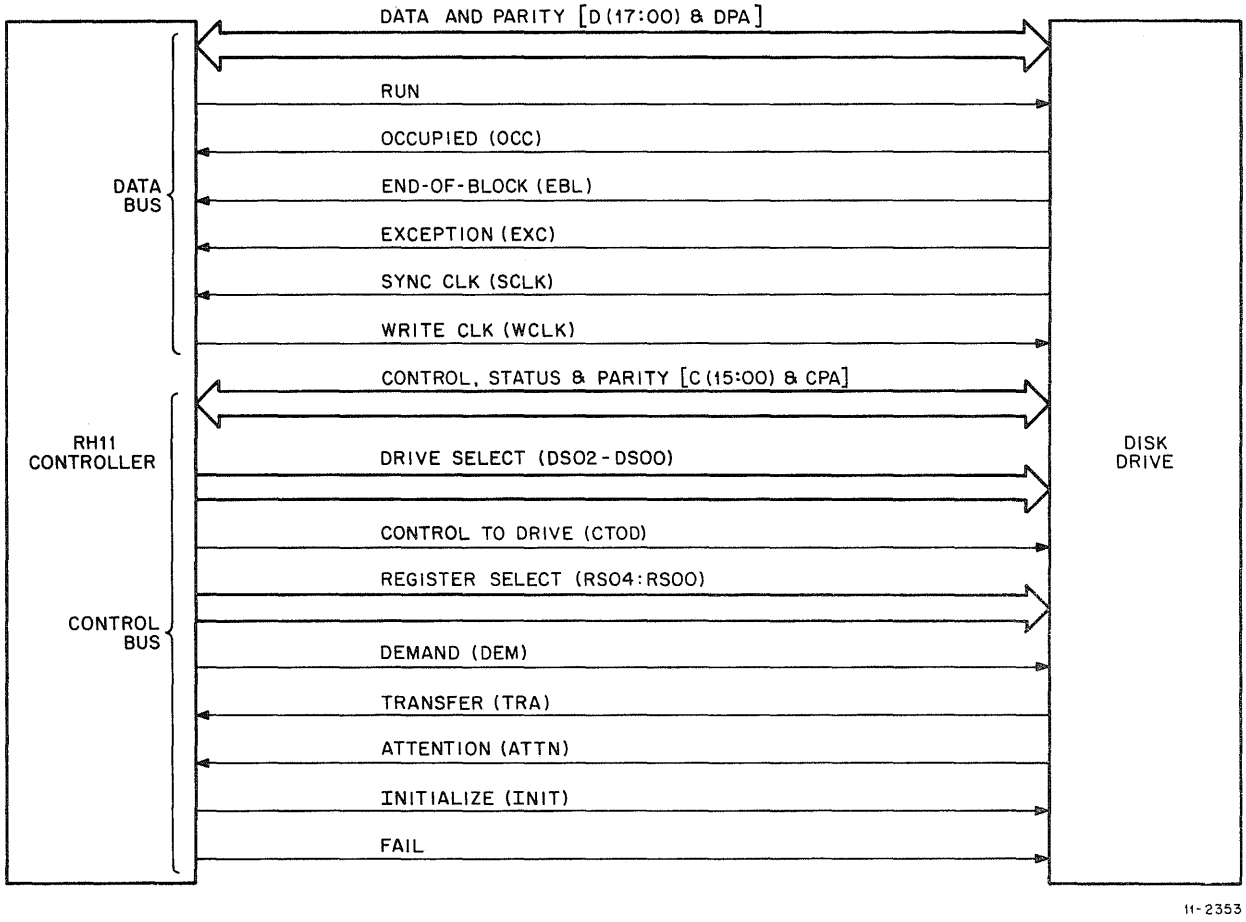


Figure 2-1 MASSBUS Interface Lines

Controller-to-Drive (CTOD) – This signal is generated by the controller and indicates the direction in which control and status information is to be transferred. For a controller-to-drive transfer, the controller asserts CTOD. For a drive-to-controller transfer, the controller negates this signal.

Register Select RS (4:0) – These five lines transmit a 5-bit binary code from the controller to the selected drive. The binary code selects one of the drive registers.

NOTE

Eight registers are present in the RS04/RS03 designated by codes 00 through 07. If a register code higher than 07 is selected, an Illegal Register (ILR) Error occurs.

	Corresponds To:	
	Register Mnemonic	Unibus Address (octal)
00 – Control Register	RSCS1	772040
01 – Drive Status Register	RSDS	772052
02 – Error Register	RSER	772054
03 – Maintenance Register	RSMR	772064
04 – Attention Summary Register	RSAS	772056
05 – Desired Block Address Register	RSDA	772046
06 – Drive Type Register	RSDT	772066
07 – Look-ahead Register	RSLA	772060

Demand (DEM) – This signal is asserted by the controller to indicate a transfer is to take place on the control bus. For a controller-to-drive transfer, Demand (DEM) is

asserted by the controller when data is present and settled on the control bus. For a drive-to-controller transfer, DEM is asserted by the controller to request data and is negated when the data has been strobed off the control bus. In both cases, the RS, DS, and CTOD lines are generated and allowed to settle before assertion of DEM.

Transfer (TRA) – This signal is asserted by the drive in response to DEM. For a controller-to-drive transfer, Transfer (TRA) is asserted when the data is strobed and is negated when DEM is negated. For a drive-to-controller transfer, TRA is asserted after the data is asserted on the bus and negated when the negation of DEM is received.

Attention (ATTN) – This line is shared by all eight drives attached to a controller; it may be asserted by any drive as a result of an abnormal condition or status change in the drive. An ATA status bit in each drive is set whenever that drive is asserting the ATTN line. ATTN may be asserted due to any of the following conditions:

a. An error while no data transfer is taking place (asserted immediately).

b. Completion of a data transfer command if an error occurred during a data transfer (asserted at the end of the transfer).

c. Completion of a non-data transfer command (such as a Search).

The ATA bit in a drive may be cleared by the following actions:

a. Asserting INIT on the Massbus (affects all eight drives).

b. Writing a 1 into the Attention Summary register (in the bit position for this drive). This clears the ATA bit; however, it does not clear the error.

c. Writing a valid command into the Control register (with the GO bit set). Note that clearing the ATA bit of one drive does not always cause the ATTN line to be negated, because other drives may also be asserting the line.

NOTE

There are three cases in which ATA is not reset when a command is written into the Control register (with the GO bit set). These are: (a) if there is a Control Bus Parity Error on the write, (b) if an error was previously set, or (c) if an illegal function code (ILF) is written.

Initialize (INIT) – This signal is asserted by the controller to perform a system reset of all the drives. It is asserted when a 1 is written into the CLR bit (bit 05 of RSCS2) and when Unibus INIT is asserted on Unibus A. When a drive receives the INIT pulse, it immediately aborts the execution of any current command and performs all actions described for the Drive Clear command.

Fail – When asserted, this signal indicates a power-fail condition has occurred in the controller. In particular, the drive inhibits reception of the INIT and DEM signals at the drive.

2.4 COMMAND INITIATION

To initiate a command in a drive via the Massbus, the controller (or the central processor via the controller) writes a word in the RSCS1 register which causes a word to be written into the drive's Control register (00). The word contains a command function code in bits 05 through 01 and a GO bit in bit 00. The GO bit is set when initiating a command. If the command specified is valid, the drive which has been addressed by the program executes the command.

Commands are of two types: non-data transfer commands (such as Drive Clear, Search) and data transfer commands (such as Read, Write, and Write-check). The command function code bits (05 through 00 including GO in RSCS1) are 01_8 through 47_8 for non-data transfer commands and are 51_8 through 77_8 for data transfer commands.

2.4.1 Non-Data Transfer Commands

Non-data transfer commands have effect only on the state of the drive. The controller merely writes the command word (with GO bit set) into the drive's Control register. At the completion of the command execution, the drive typically asserts the ATTN line in order to signal its completion.

If the non-data transfer command code written into the drive is not recognized by the drive as a valid command, the drive will immediately signal an error by asserting the ATTN line. The Illegal Function Error (ILF) is set.

2.4.2 Data Transfer Commands

When any data transfer command code (with the GO bit set) is written into the Drive's Control register, the controller expects data transfer on the data bus to begin soon thereafter. The controller resets its RDY (Controller Ready) bit as soon as the data transfer command code is written into a drive. The drive normally responds by asserting the OCC line. The controller asserts RUN and then data is transferred to or from the specified drive.

If an error occurs in a drive during a data transfer command, the drive asserts the EXC line. This line remains asserted until the trailing edge of the last EBL pulse. The RH11 Controller always negates the RUN line when it detects EXC asserted, so that data transfer is terminated at the end of the sector in which the error was signaled.

2.5 MASSBUS PHYSICAL DESCRIPTION

The Massbus consists of 56 signals including data, control, status, and parity. These signals are routed between the RH11 and the drives by three 40-conductor flat cables. Since Massbus signal transmission (with exception of the FAIL signal) is accomplished by differential transmitter/receiver pairs, each cable can accommodate 20 differential signals.

On the drive end, the cables are plugged into M5903 Massbus Drive Transceiver modules. The last drive has M5903-YA modules which terminate the buses. On the controller end, each cable plugs into a M5904 Massbus Controller Transceiver module (described in subsequent paragraphs). Each M5904 module, in turn, plugs into a slot (slots C, D-4, 5, 6) in the RH11 backplane to complete the signal path.

Table 2-1 shows the Massbus signals and their associated pin assignments.

Table 2-1
Massbus Signal Cable Designations

Cable	Pin*		Polarity	Designation
Massbus Cable A	A	1	-	MASS D00
	B	2	+	
	C	3	+	MASS D01
	D	4	-	
	E	5	-	MASS D02
	F	6	+	
	H	7	+	MASS D03
	J	8	-	
	K	9	-	MASS D04
	L	10	+	
	M	11	+	MASS D05
	N	12	-	
	P	13	-	MASS C00
	R	14	+	
	S	15	+	MASS C01
	T	16	-	
	U	17	-	MASS C02
	V	18	+	
	W	19	+	MASS C03
	X	20	-	
	Y	21	-	MASS C04
	Z	22	+	
	AA	23	+	MASS C05
	BB	24	-	
	CC	25	-	MASS SCLK
	DD	26	+	
	EE	27	+	MASS RS3
	FF	28	-	
	HH	29	+	MASS ATTN
	JJ	30	-	
	KK	31	-	MASS RS4
	LL	32	+	
	MM	33	-	MASS CTOD
	NN	34	+	
	PP	35	+	MASS WCLK
	RR	36	-	
	SS	37	+	MASS RUN
	TT	38	-	
	UU	39		SPARE
	VV	40		GND

*Alternate pin designation schemes

Table 2-1 (Cont)
Massbus Signal Cable Designations

Cable	Pin*		Polarity	Designation
Massbus Cable B	A	1	-	MASS D06
	B	2	+	
	C	3	+	MASS D07
	D	4	-	
	E	5	-	MASS D08
	F	6	+	
	H	7	+	MASS D09
	J	8	-	
	K	9	-	MASS D10
	L	10	+	
	M	11	+	MASS D11
	N	12	-	
	P	13	-	MASS C06
	R	14	+	
	S	15	+	MASS C07
	T	16	-	
	U	17	-	MASS C08
	V	18	+	
	W	19	+	MASS C09
	X	20	-	
	Y	21	-	MASS C10
	Z	22	+	
	AA	23	+	MASS C11
	BB	24	-	
	CC	25	-	MASS EXC
	DD	26	+	
	EE	27	+	MASS RS0
	FF	28	-	
	HH	29	+	MASS EBL
	JJ	30	-	
	KK	31	-	MASS RS1
	LL	32	+	
	MM	33	-	MASS RS2
	NN	34	+	
	PP	35	+	MASS INIT
	RR	36	-	
	SS	37	+	MASS SP1
	TT	38	-	
	UU	39		SPARE
	VV	40		GND

Table 2-1 (Cont)
Massbus Signal Cable Designations

Cable	Pin*		Polarity	Designation
Massbus Cable C	A	1	-	MASS D12
	B	2	+	
	C	3	+	MASS D13
	D	4	-	
	E	5	-	MASS D14
	F	6	+	
	H	7	+	MASS D15
	J	8	-	
	K	9	-	MASS D16
	L	10	+	
	M	11	+	MASS D17
	N	12	-	
	P	13	-	MASS DPA
	R	14	+	
	S	15	+	MASS C12
	T	16	-	
	U	17	-	MASS C13
	V	18	+	
	W	19	+	MASS C14
	X	20	-	
	Y	21	-	MASS C15
	Z	22	+	
	AA	23	+	MASS CPA
	BB	24	-	
	CC	25	-	MASS OCC
	DD	26	+	
	EE	27	+	MASS DS0
	FF	28	-	
	HH	29	+	MASS TRA
	JJ	30	-	
	KK	31	-	MASS DS1
	LL	32	+	
	MM	33	-	MASS DS2
	NN	34	+	
	PP	35	+	MASS DEM
	RR	36	-	
	SS	37	+	MASS SP2
	TT	38	-	
	UU	39	H	MASS FAIL
	VV	40		GND

*Alternate pin designation schemes

Note: Massbus cables are installed with the edge marking of the cable closest to the module handle.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 GENERAL

Twelve 16-bit registers are employed to interface the RH11 Device Controller to the RS04/RS03 disk. These registers are loaded and read under program control via Unibus A (the control port of the RH11). Data may sometimes be transferred over a second Unibus (Unibus B) called the 'data port' of the RH11. The disk system is monitored by status and error indicators in these registers. Figure 3-1 shows the various device registers and their locations. Four of the twelve registers are located entirely in the RH11 and seven are located entirely in the RS04 or RS03. The twelfth register (RSCS1 Control and Status register) is shared by both the RH11 and the RS04 or RS03 disk. Bits 15 through 13 and bits 10 through 6 of this register are stored in the RH11 while bits 12, 11, and 5 through 0 are generated by the RS04 or RS03. Table 3-1 shows the various subsystem registers and their respective addresses. The following paragraphs describe the registers and their bit usage in detail.

Table 3-1
RH11 and RS04/RS03 Device Registers

Mnemonic	Register Name	Unibus Address
RSCS1	Control and Status 1	772040
RSWC	Word Count	772042
RSBA	Unibus Address	772044
RSDA	Desired (Disk) Address	772046
RSCS2	Control and Status 2	772050
RSDS	Drive Status	772052
RSER	Error	772054
RSAS	Attention Summary	772056
RSLA	Look-Ahead	772060
RSDB	Data Buffer	772062
RSMR	Maintenance	772064
RSDT	Drive Type	772066

3.2 DEFINITIONS

This paragraph describes some of the Massbus signals which are used in generating status information.

- Attention (ATTN) – The ATTN line is a shared line which connects from all drives in common to the RH11 Controller. Each drive asserts ATTN (and sets its own ATA bit) whenever a) it has an error condition (ERR asserted) or b) it has just finished executing a search command.

  The logical expressions for these statements are:

  $ATTN \leftarrow ATA_0 + ATA_1 + \cdots\cdots + ATA_7$

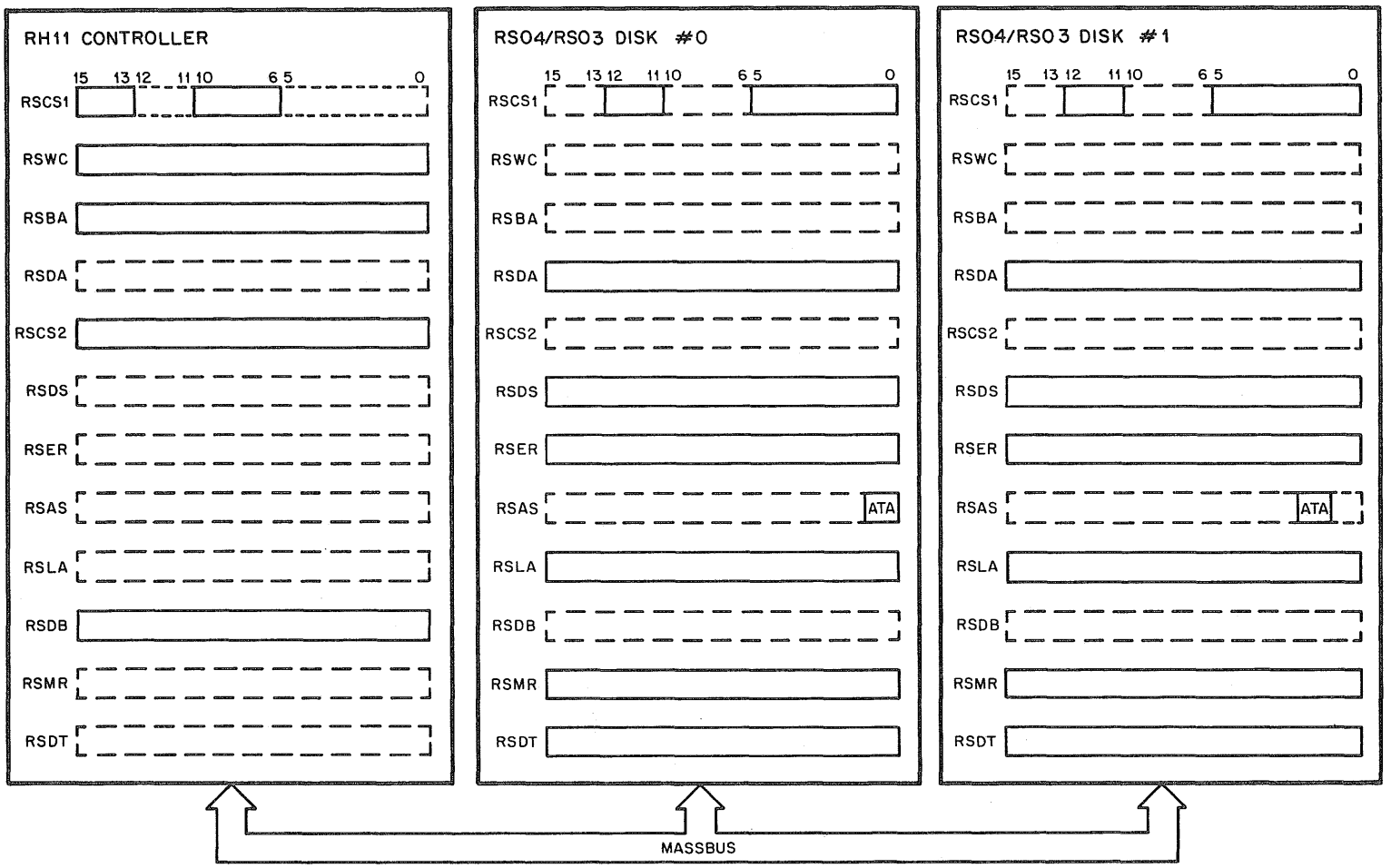
  $ATA_i \leftarrow ERR_i +$ completion of search command in drive

  $ERR_i \leftarrow$ any drive error asserted (RSER).

  (i represents the unit select code of a drive, 0 through 7).

- Exception (EXC) – The EXC line connects from the controllers to the drive which is doing a data transfer. It is asserted by the drive if an error occurs during the transfer. This line is used to distinguish errors in the drive doing a data transfer from errors signaled by the ATTN line. (A drive which is doing a data transfer never asserts ATTN while the data transfer is under way.)

- End-of-Block (EBL) – The EBL line is pulsed by the drive doing a data transfer at the end of each sector. The RH11 examines the EXC line only during the EBL pulse.



NOTES:

1. RSCS1 shared between RH11 and RS04/RS03 bits 15-13 & 10-6 are stored in RH11, bits 12,11, & 5-0 are generated by RS04/RS03
2. Each drive is assigned an attention summary bit in the bit location corresponding to it's unit no.
3. Location of registers denoted by solid lines; dashed lines are for reference only.

RSCS1, RSCS2 - CONTROL & STATUS
RSWC - WORD COUNT
RSBA - UNIBUS ADDRESS
RSDA - DESIRED (DISK) ADDRESS
RSER - ERROR
RSAS - ATTENTION SUMMARY
RSLA - LOOK-AHEAD
RSDB - DATA BUFFER
RSMR - MAINTENANCE
RSDT - DRIVE TYPE

11-2338

Figure 3-1 Device Register Locations

- Clearing Methods

  Controller Clear – Controller Clear is the action of writing a 1 into the CLR control bit (bit 5 of RSCS2). This causes the following to be cleared:

  a) All controller errors (RSCS2, bits 15 through 8, RSCS1, bits 15 through 13)

  b) Silo buffer

  c) RSBA Unibus Address register and A16, A17

  d) Unit select U(02:00), IE, PSEL, BAI and PAT bits

  e) Errors, function code, and DA register in all drives connected to the RH11 (by assertion of the Massbus INIT signal).

  RH11 Error Clear – RH11 Error Clear is the action of writing a 1 into the TRE bit (bit 14 of RSCS1). This causes all controller errors to be cleared (RSCS2, bits 15 through 8 and RSCS1 bits 14 and 13).

  Drive Clear – Drive Clear is a command code (11_8) which causes errors, the function code, and the DA register to be cleared in the drive selected by U(02:00).

Table 3-2 shows the various methods used to clear the disk system.

3.3 PROGRAMMING NOTES

This paragraph describes miscellaneous features of the RH11/RS04/RS03 subsystem not described in other sections of this manual.

The TRE (Transfer Error) bit is located in the RH11 and is associated only with error conditions during data transfers and error conditions in the controller. The ERR bit is a summary error bit which is located in each drive. Writing a

Table 3-2
Results of Program-Controlled Clearing

ACTION	Clear All RH11 Errors	Clear Silo	RESULTS			
			Clear BA, U(02:00), IE, PSEL, PAT, BAI A16, A17	Assert Massbus INIT	Clear ERR and errors in the drive	Clear RSDA and Function Code in the Drive
Unibus A INIT (Reset instruction execution or console reset)	X	X	X	X	X (all 8 drives)	X (all 8 drives)
Controller Clear (Bit 5 in RSCS2←1)	X	X	X	X	X (all 8 drives)	X (all 8 drives)
Issue a Data Transfer command (with GO = 1)	X	X				
RH11 Error Clear (Bit 14 in RSCS1←1)	X					
Drive Clear (Function code with GO = 11_8)					X (selected drive only)	X (selected drive only)

1 into TRE (RH11 Error Clear) does not affect ERR in any drive. Similarly, a Drive Clear command does not affect TRE in the RH11.

RDY is the "ready" indicator for the RH11 Controller. When RDY is asserted, the RH11 is ready to accept a data transfer command. DRY is the "ready" indicator for each drive. In order to successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data transfer command (e.g., Search, Drive Clear) may be issued to a drive any time DRY is asserted, regardless of the state of the RDY bit.

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command (such as Search) is successfully initiated, only the DRY bit becomes negated. Some non-data transfer commands (such as Drive Clear) take so little time to execute that the program will never see the negation of the DRY bit.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the controller (RH11) is done.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a data transfer command is issued to a drive which has ERR asserted, the drive does not execute the command, and the Missed Transfer Error (MXF, bit 9 in the CS2 register) occurs in the RH11.

3.4 INTERRUPT CONDITIONS

The RH11 generates an interrupt in the PDP-11 CPU due to the following conditions:

a. Upon termination of a data transfer (if Interrupt Enable is set when the RH11 becomes "ready").

   Interrupt = (RDY ← 1) · (IE)

b. Upon assertion of attention or occurrence of a controller error (while the controller is not busy and Interrupt Enable is set).

   Interrupt = (SC ← 1) · (RDY) · (IE)

c. When the program writes 1s into IE and RDY at the same time.

   Interrupt = (IE ← 1) · (RDY ← 1)

CAUTION

READ-MODIFY-WRITE instruction (BIS, BIC, etc.) with IE bit set will cause an immediate interrupt.

3.5 TERMINATION OF DATA TRANSFERS

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination – word count overflows to 0 and the RH11 becomes ready (RDY ← 1) at the end of the current sector.

b. Controller Error – An error occurs in the CS2 register as indicated below:

Bit		
	15	DLT (Data Late)
	14	WCE (Write Check Error)
	13	UPE (Unibus Parity Error)
	12	NED (Nonexistent Drive)
	11	NEM (Nonexistent Memory)
	10	PGE (Program Error)
	9	MXF (Missed Transfer Error)
	8	MDPE (Massbus Data Parity Error)

   Any of these errors sets TRE. The RH11 terminates the data transfer immediately, but waits for the EBL pulse at the end of the current sector before becoming Ready.

c. Drive Error – An error occurs in the drive. The drive sets ERR in the RSDS register and at least one bit in the RSER register. The drive also asserts EXC, which causes TRE to set when the next EBL pulse occurs. The RH11 becomes Ready after the EBL pulse.

   After the EBL pulse, the drive disconnects from the Massbus data bus and, because ERR is set, ATTN is then asserted.

   In some cases of severe drive errors, the EBL pulse may be artificially generated by the drive before the normal end of the sector.

d. Program-caused Abort – By performing a Controller Clear or a Reset instruction, the program can cause Massbus INIT to be asserted by the RH11, which aborts all operations on all drives attached to the Controller. Status and error information is lost when this is done. The RH11 and RS04/RS03 become Ready immediately.

3.6 CONTROL AND STATUS 1 (RSCS1) REGISTER (772040)

This register is utilized by the RH11/RS04/RS03 to store the disk commands and operational status. The function (command) code and GO bit, in this register, designate a function for the drive selected by bits 02 through 00 in the RSCS2 Control and Status 2 register.

Data transfer command codes are designated by 51_8 through 77_8 (always odd since the GO bit must be asserted to execute a data transfer command). Other command codes (01_8 through 47_8) are called non-data transfer commands. Only data transfer commands cause the RH11 to become busy (RDY bit negated). While the RH11 is busy, no further data transfer commands may be issued (see PGE bit 10 in RSCS2). Non-data transfer commands, however, may be issued at any time and to any drive which is not busy (DRY asserted).

While a data transfer is in progress, unit select bits U(02:00) in RSCS2 may be changed by the program in order to issue a non-data transfer command to another drive. This will not affect the data transfer.

When a non-data transfer command code is written into RSCS1 while a data transfer is taking place, only the even (low) byte of RSCS1 should be written. This will prevent the program from unintentionally changing RSCS1 status bits (A16, A17 and PSEL) if the transfer is completed just before the register is written. (While the RDY bit is negated, the RH11 prevents program modification of these control bits even when the write is done into the odd byte.)

Figure 3-2 shows the bit format, and Table 3-3 defines the bit usage for the RSCS1 register.

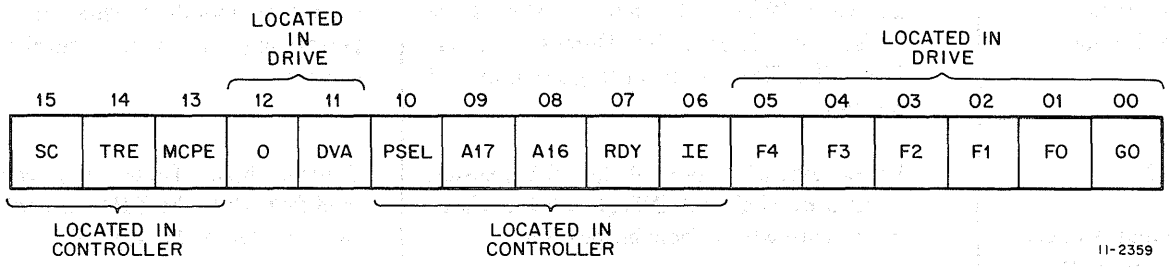


Figure 3-2 Control & Status Register 1 Bit Usage

Table 3-3
Control and Status 1 Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	SC Special Condition Read only	Set by TRE or ATTN or Massbus Control Parity Error. Cleared by Unibus A INIT, Controller Clear, or by removing the ATTN condition.	SC = TRE + ATTN + MCPE
14	TRE Transfer Error Read/write	Set by DLT or WCE or UPE or NED or NEM or PGE or MXF or MDPE or a drive error during a data transfer. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	TRE = (DLT + WCE + UPE + NED + NEM + PGE + MXF + MDPE + (EXC · EBL)

Table 3-3 (Cont)
Control and Status 1 Register Bit Assignments

Bit		Set By/Cleared By	Remarks
13	MCPE Massbus Control Bus Parity Error Read only	Set by parity error on Massbus control bus while reading a remote register (located in the drive). Cleared by Unibus A INIT, Controller Clear, or RH11 Error Clear or loading a data transfer command with the GO set.	Parity errors which occur on the Massbus control bus while writing a drive register are detected by the drive and cause the PAR error (RSER register, bit 03) to set.
12	Not used	Always read as a 0.	
11	DVA DriVe Available Read only	Always a 1 in the RS04/RS03 when read from an existing drive.	
10	PSEL Port SELect Read/write	When PSEL = 1, data transfer is via Unibus B; when PSEL = 0, data transfer is via Unibus A. Cleared by Unibus A INIT, Controller Clear, or by writing a 0 in this bit position.	A Unibus select control bit. This bit cannot be modified while the RH11 is performing a data transfer (RDY negated).
9 8	A17 A16 Unibus Address Extension Bits Read/write	Upper extension bits of the BA register. Cleared by Unibus A INIT, Controller Clear, or by writing 0s in these bit positions.	Control bits. These bits cannot be modified while the RH11 is performing a data transfer (RDY negated).
7	RDY ReaDY Read/only	RDY normally = 1. During data transfers, RDY = 0.	When a data transfer command code (51_8–77_8) is written into RSCS1, RDY is reset. At the termination of the data transfer, RDY is set (Paragraph 3.3).
6	IE Interrupt Enable Read/write	IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted (Paragraph 3.4). Cleared by Unibus A INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.	A program-controlled interrupt may occur by writing 1s into IE and RDY at the same time.

Table 3-3 (Cont)
Control and Status 1 Register Bit Assignments

Bit		Set By/Cleared By	Remarks
5–0	F4–F0 and GO bit Read/write	F4–F0 are function (command) code control bits which determine the action to be performed by the RH11 and RS04/RS03 as shown in chart. F4 F3 F2 F1 F0 Function 0 0 0 0 0 No operation 0 0 1 0 0 Drive Clear 0 1 0 0 0 Read In Preset 0 1 1 0 0 Search 1 0 1 0 0 Write Check 1 1 0 0 0 Write 1 1 1 0 0 Read The GO bit (RSCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution. Cleared by Unibus A INIT or Controller Clear (will abort command execution in all drives).	The function code bits are stored in the selected drive. Data transfer commands, defined as F4 · (F3 + F2), always cause the RH11 to become busy.

3.7 WORD COUNT (RSWC) REGISTER (772042)

This register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory.

Figure 3-3 shows the RSWC bit format, and Table 3-4 provides a description of each bit.

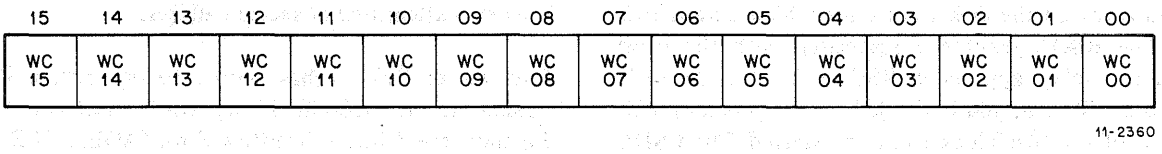


Figure 3-3 Word Count Register Bit Usage

Table 3-4
Word Count Register Bit Assignments

Bit		Set By/Cleared By	Remarks
WC	(15:00) Word Count Read/write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it.	Incremented for each data transfer.

3.8 UNIBUS ADDRESS (RSBA) REGISTER (772044)

This device register is used by the RH11 to address the memory location in which a transfer is to take place.

The RSBA register forms the lower 16 bits of address which combine with RSCS1 bits 09 and 08 to create the 18-bit memory address. This register should be loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (Bus Address Increment Inhibit) bit (bit 03 of RSCS2) is set, the incrementing of the RSBA register is inhibited and all transfers take place to or from the starting memory address. Figure 3-4 shows the RSBA bit usage, and Table 3-5 provides a description of each bit.

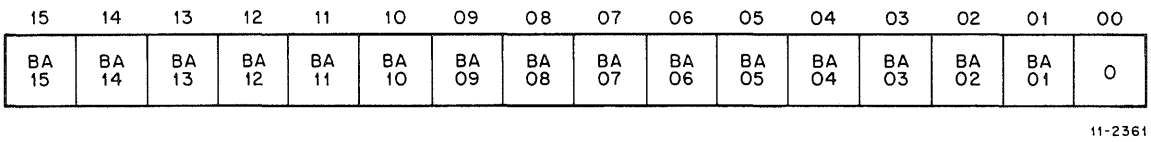


Figure 3-4 UNIBUS Address Register Bit Usage

Table 3-5
Unibus Address Register Bit Assignments

Bit		Set By/Cleared By	Remarks
00	Not used	Always read as a 0.	
01–15	BA(01:15) Unibus Address Read/write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus A INIT or by Controller Clear.	The BA register is incremented by 2 by the RH11 after each transfer of a word to or from memory.

3.9 DESIRED ADDRESS (RSDA) REGISTER (772046)

This device register is used by the drive to address the sector and track on the disk to or from which a transfer is desired. The RSDA register is associated with the drive whose unit number appears in RSCS2 (02:00). Before a transfer, the RSDA should be loaded by the program with the address of the first block to be transferred. The RSDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RSDA contains the address of the *next* block (not yet transferred).

The contents of RSDA are regarded as a 16-bit address, of which only the values 000000 through 007777 are valid. Other values may be loaded into RSDA, but the Invalid Address Error (IAE, RSER bit 10) will be set if a data transfer is attempted at such an address.

After sector 007777 has been read or written, RSDA is incremented to 010000. If the word count is not zero at this time, the Address Overflow Error (AOE, RSER bit 9) is set.

The RSDA register can only be loaded with a word. Any attempt to write a byte causes the entire word to be written. Any attempt to write in this register while the drive's GO bit is asserted will cause an RMR (Register Modify Refused) Error (RSER, bit 02) and the register is not modified. Figure 3-5 shows the Desired Address register bit usage, and Table 3-6 provides a description of each bit.

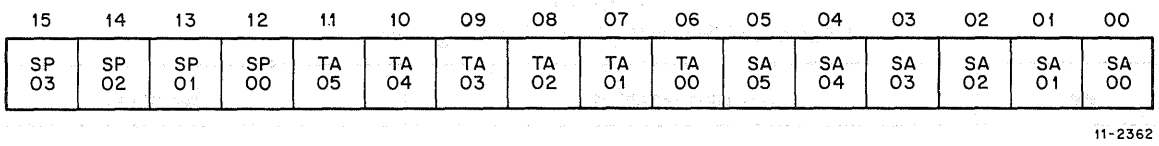


Figure 3-5 Desired Address Register Bit Usage

Table 3-6
Desired Address Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–12 SP(03:00) SPare Read/write	If set when an operation is begun by setting the GO bit, an IAE error (RSER bit 10) will be posted. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function.	Spare bits for future expansion. The bits are incremented by a carry from the track address.
11–06 TA Track Addr (05:00) Read/write	Set by the program to specify the track on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function.	Incremented by the drive when a carry out of SA (05) occurs.
05–00 SA Sector Addr (05:00) Read/write	Set by the program to specify the sector on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or performing a Drive Clear function.	Incremented by the drive after each sector has been transferred.

3.10 CONTROL AND STATUS 2 (RSCS2) REGISTER (772050)

This register indicates the status of the controller and contains the drive unit number U(02:00). The unit number specified in bits 02 through 00 of this register indicates which drive is responding when registers are addressed that are located in a drive.

These are:

RSCS1 (bits 5 through 0, 12 and 11)
RSDA RSLA
RSDS RSMR
RSER RSDT

Figure 3-6 shows the RSCS2 bit usage, and Table 3-7 provides a description of each bit.

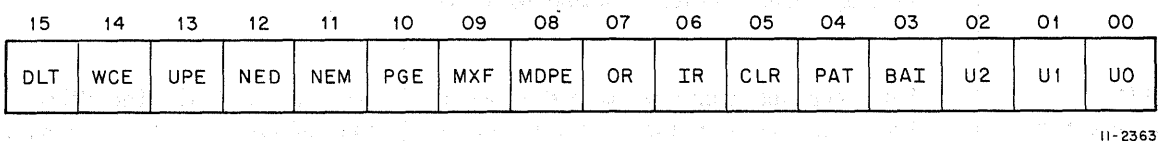


Figure 3-6 Control and Status Register 2 Bit Usage

Table 3-7
Control and Status Register 2 Bit Assignments

Bit		Set By/Cleared By	Remarks
15	DLT Data LaTe Read only	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second Unibus (PSEL = 1) and a Unibus B INIT is received on that port. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	DLT causes TRE. Buffering is 66_{10} words deep in the controller, and a DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the RSDB register (Paragraph 3.15).
14	WCE Write Check Error Read only	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	WCE causes TRE. If a mismatch is detected during a Write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RSBA [and extension is the address of the word following the one which did not match (if BAI is not set)]. The mismatched data word from the disk is displayed in the data buffer (RSDB).
13	UPE Unibus Parity Error Read/write	Set if the Unibus parity lines indicate a parity error while the controller is performing a Write or Write-check command. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	UPE causes TRE. When the Unibus is selected to do 18-bit data transfers, the UPE error is disabled. When a Unibus parity error occurs, the RSBA register contains the address +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes.
12	NED Non-Existent Drive Read only	Set when the program reads or writes a drive register (CS1, DA, DS, ER, LA, MR, or DT) in a drive [selected by U(02:00)] which does not exist or is powered down. (The drive fails to assert TRA within 1.5 μs after assertion of DEM.) Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	NED causes TRE.
11	NEM Non-Existent Memory Read only	Set when the controller is performing a DMA transfer and the memory address specified in RSBA is nonexistent (does not respond to MSYN within 10 μs. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	NEM causes TRE. The RSBA contains the address +2 of the memory location causing the error.

Table 3-7 (Cont)
Control and Status Register 2 Bit Assignments

Bit		Set By/Cleared By	Remarks
10	PGE ProGram Error Read only	Set when the program attempts to initiate a data transfer operation while the RH11 is currently performing one. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	PGE causes TRE. The data transfer command code is inhibited from being written.
09	MXF Missed Transfer Read/write	Set if the drive does not respond to a data transfer command within 250 ms. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error).
08	MDPE Massbus Data Bus Parity Error Read only	Set when a parity error occurs on the Massbus data bus while doing a read or write-check operation. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	MDPE causes TRE. Parity errors on the Massbus data bus during write operations are detected by the drive and cause the PAR error (RSER register, bit 03).
07	OR Output Ready Read only	Set when a word is present in RSDB and can be read by the program. Cleared by Unibus A INIT, Controller Clear, or by reading DB (Paragraph 3.15).	Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB register before OR is asserted will cause a DLT error.
06	IR Input Ready Read only	Set when a word may be written in the DB register by the program. Cleared by reading the DB (Paragraph 3.15).	Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB register before IR is asserted will cause a DLT error.
05	CLR Controller CLeaR Write only	When a 1 is written into this bit, the RH11 and all drives are initialized (Paragraph 3.2).	Unibus A INIT also causes Controller Clear to occur.
04	PAT PArity Test Read/write	While PAT is set, the RH11 generates even parity on both the control bus and data bus of the Massbus. When clear, odd parity is generated. Cleared by Unibus A INIT or Controller Clear.	While PAT is set, the RH11 checks for even parity received on the data bus but not on the control bus.

Table 3-7 (Cont)
Control and Status Register 2 Bit Assignments

Bit		Set By/Cleared By	Remarks
03	BAI UniBus Address Increment Inhibit Read/write	When BAI is set, the RH11 will not increment the BA register during a data transfer. This bit cannot be modified while the RH11 is doing a data transfer (RDY negated). Cleared by Unibus A INIT or Controller Clear.	When set during a data transfer, all data words are read from or written into the same memory location.
02–00	U(2:0) Unit Select (2:0) Read/write	These bits are written by the program to select a drive. Cleared by Unibus A INIT or Controller Clear.	The unit select bits can be changed by the program during data transfer operations without interferring with the transfer. The CS1, DA, DS, ER, LA, MR, and DT registers contain bits which come from the selected drive.

3.11 DRIVE STATUS (RSDS) REGISTER (772052)

This register contains the various status indicators for the selected drive. The status indicators displayed are those of the drive which is specified by the unit select bits (02:00) of the RSCS2 register. The register is a read-only register. Figure 3-7 shows the RSDS bit usage, and Table 3-8 provides a description of each bit. Writing into this register will not cause an error, and will not modify any of the status bits.

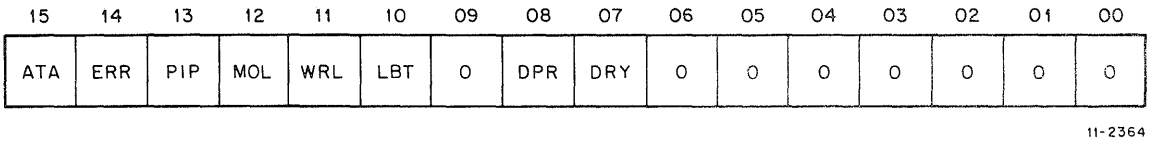


Figure 3-7 Drive Status Register Bit Usage

Table 3-8
Drive Status Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	ATA ATtention Active Read only	Set by the drive when there is an Attention condition in that drive. Cleared by Unibus A INIT, Controller Clear, loading a command with the GO bit set and ERR = 0, or loading a 1 in the RSAS register in the bit position corresponding to the drive's unit number. (The last two methods of clearing the ATA bit will not clear the error indicators in the drive.)	An Attention condition occurs 1) at the completion of a Search command, 2) at the completion of a data transfer in which the drive detected an error, 3) if an error condition occurs while the drive is not performing a command, and 4) if there is any change in status of MOL. When the ATA bit of any drive is set, the ATTN line is asserted.

Table 3-8 (Cont)
Drive Status Register Bit Assignments

Bit		Set By/Cleared By	Remarks
14	ERR (ERRor Summary) Read only	Set when one or more of the error bits is set in the RSER register of the selected drive. Cleared by Unibus A INIT Controller Clear, or by Drive Clear.	This bit is the logical OR of all the bits in the RSER register. This bit is not cleared by loading a command other than Drive Clear. While ERR is asserted, commands other than Drive Clear are not accepted by the drive.
13	PIP Positioning In Progress Read only	Set by the drive while a Search command is underway. Cleared at the completion of the search operation.	This bit helps to distinguish the case of a drive being busy (DRY negated) while no data transfer is underway (RDY asserted in the RH11).
12	MOL Medium On Line Read only	Set by the drive when the drive is up to speed and power is within limits. Cleared when the drive is powered down, and during power-up sequencing.	Any change in status of MOL will set ATA.
11	WRL WRite Locked Read only	Set by the drive when the address in the RSDA register is among those which are write protected (and the write lock switch is in the enable position). Cleared by loading RSDA with an address which is not write protected.	
10	LBT Last Block Transferred Read only	Set by the drive at the end of the data transfer to the highest address sector. Cleared by Unibus A INIT, Controller Clear, loading a new address in the RSDA register, or performing a Drive Clear function.	
09	Not Used	Always read as a 0.	
08	DPR Drive PResent Read only	Always read as a 1.	This bit is for use in dual-controller configurations.
07	DRY Drive ReadY Read only	Set whenever the drive is on-line and prepared to accept a command. Cleared whenever a valid command (with GO set) is loaded into RSCS1.	
06–00	Always read as 0. Not Used		

3.12 ERROR (RSER) REGISTER (772054)

This register contains the error status indicators for the drive whose unit number appears in bits 02 through 00 of RSCS2. Bit 14 of the RSDS register (ERR) is a composite error indicator which represents the logical OR of all the bits in the RSER register.

The RSER register is a read/write register; thus, diagnostic programs may test the functioning of the error indicators by counting a 1 into them.

Writing 0s into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

The RSER register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy (GO bit is asserted), an RMR (RSER register, bit 02) error is set, and the contents of the register are not modified. Figure 3-8 shows the RSER bit usage, and Table 3-9 provides a description of each bit.

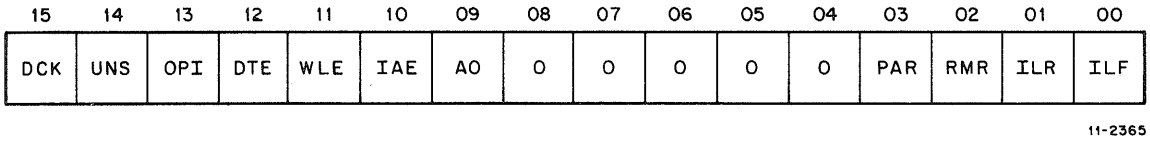


Figure 3-8 Error Register Bit Usage

Table 3-9
Error Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	DCK Data CheckK Read/write	Set by the drive when an error in the cyclic redundance check is detected during a read or write-check operation. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	
14	UNS UNSafe Read/write	Set by the drive upon detection of low power. Cleared upon restoration of power. Can be set or cleared by the program.	If a transfer is in progress when ac power loss occurs in the drive, the transfer is aborted. ATTN is asserted by this drive for as long as dc power lasts, whether or not a transfer was in progress.
13	OPI OPeration Incomplete Read/write	Set when the drive fails to complete an operation within the expected time. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	A data transfer operation is considered incomplete if the RUN line is not asserted by the RH11 within two disk revolutions after a data transfer command was loaded. This would indicate a failure in the RH11. A Search command is considered incomplete if not terminated within two disk revolutions. This would indicate a drive failure.
12	DTE Drive Timing Error Read/write	Set by the drive when it detects a timing fault (loss of clock or index pulse, dropping or picking up clock pulses). Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	

Table 3-9 (Cont)
Error Register Bit Assignments

Bit		Set By/Cleared By	Remarks
11	WLE Write Lock Error Read/write	Set by the drive when a write function is attempted at an address which is write protected. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	
10	IAE Invalid Address Error Read/write	Set by the drive when a data transfer or Search command is loaded while an invalid address is in the RSDA (desired address) register. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	In the RS04/RS03, an invalid address is one which is larger than the maximum address.
09	AOE Address Overflow Error Read/write	Set by the drive when the controller attempts to continue to transfer data after the last sector on the last track has been written or read. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	When this error occurs, no further data transfer occurs. The RSDA register contains an invalid address.
08–04	Not Used	Always read as 0.	
03	PAR Massbus PARity Error Read/write	Set when incorrect parity is detected by the drive during a register write operation or on a data transfer during a write operation. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	If a control bus parity error is detected when writing into the CS1 register, the GO bit is inhibited and no commands will be executed.
02	RMR Register Modify Refused Read/write	Set by the drive when an attempt is made by the program to write into the RSDA, RSER, or RSCS1 registers, while the drive is busy (DRY bit is negated). Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	Drive operation can be aborted by program control only by performing Controller Clear or Reset. These must be used with caution due to their effects on other devices.
01	ILR ILlegal Register Read/write	Set by the drive when the program attempts to read or write a drive register whose address is not recognized by the drive. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	Indicates a hardware failure in the controller or drives address logic.
00	ILF ILlegal Function Read/write	Set by the drive when the GO bit is set and the code in the Function register (RSCS1, bits 05–01) is not an implemented code. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Can be set or cleared by the program.	

3.13 ATTENTION SUMMARY (RSAS) REGISTER (772056)

This register allows the program to examine the state of the attention status of all drives with only one register read operation. It also provides means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in RSDS for the corresponding drive. When fewer than eight drives are attached to the RH11, the bits corresponding to the missing drives are always 0.

A drive's ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number (loading a 0 has no effect). This allows the program to inspect the RSAS register and later to reset the ATA bits which were set, without accidentally resetting other ATA bits which may have become set in the meantime.

For a program to use RSAS without losing status information, the program must use the MOV instruction for all reads and writes of this register. An instruction that does a read-restore (such as BIS) may cause bits that became asserted between the read and the restore to be lost.

This register can be read or written at any time, regardless of whether any particular drive is busy. Note that a drive never asserts ATA during the execution of a command. The RSAS register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. Figure 3-9 shows the RSAS bit usage and Table 3-10 provides a description of each bit.

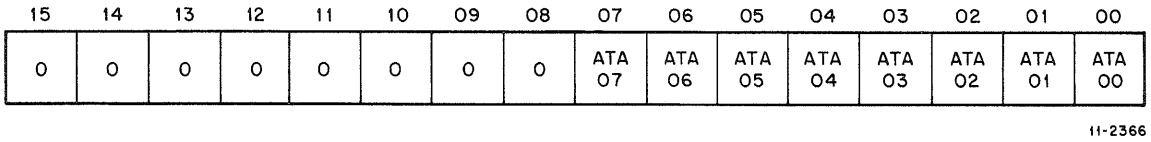


Figure 3-9 Attention Summary Register Bit Usage

Table 3-10
Attention Summary Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15:08 Not Used	Always read as a 0.	
07:00 ATA 07–00 ATtention Active (07:00) Read/write	Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by Unibus A INIT or Controller Clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive if ERR = 0, or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.	Each drive's ATA bit is displayed individually in bit 15 of RSDS. Each drive responds in the bit position which corresponds to its unit number; e.g., drive 02 responds in bit position 02.

3.14 LOOK-AHEAD (RSLA) REGISTER (772060)

This register presents the angular position of the disk relative to the read/write heads for the disk whose unit number appears in bits 02 through 00 of the RSCS2 register.

The purpose of this register is to provide the programmer with a means of optimizing disk access by minimizing rotational delays. The register contains a fractional sector counter providing fine resolution of angular position to 64ths of a sector. Figure 3-10 shows the RHLA bit usage, and Table 3-11 provides a description of each bit.

The RSLA is a read only register. Writing into it will not cause an error and will not modify any status bits.

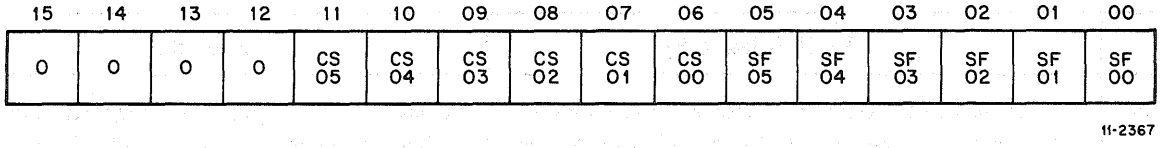


Figure 3-10 Look-Ahead Register Bit Usage

Table 3-11
Look-Ahead Register Bit Assignments

Bit	Set By/ Cleared By	Remarks
15–12 Not Used	Always read as a 0.	
11–06 CS(05:00 Current Sector Addr Read only		Indicates the sector address currently under the read/write heads of the drive whose unit number appears in RSCS2(2:0).
05–00 SF(05:00) Sector Fract Read only		Indicates the fraction of the current sector which has passed the read/write heads in 64ths of a sector.

3.15 DATA BUFFER (RSDB) REGISTER (772062)

This register provides a maintenance tool to check the Silo data buffer in the RH11. A total of 66_{10} words is accepted before the Silo data buffer becomes full. If the program attempts to write into the data buffer while it is full, a DLT (Data Late Error) is posted. If the program attempts to read the data buffer when it is empty, a DLT error will be posted. Successive reads from DB read out words in the same order in which they were entered into the Silo.

The IR (input ready) and OR (output ready) status indicators in the RSCS2 register are provided so that the programmer can determine when words can be read from or written into the RSDB. IR should be asserted before attempting a write into DB; OR should be asserted before attempting a read from DB.

The RSDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the DB register is a "destructive read-out" operation: the top data word in the Silo buffer is removed by the action of reading DB, and a new data word (if present) replaces it a short time later. Conversely, the action of writing the DB register does not destroy the "contents" of DB; it merely causes one more data word to be inserted into the Silo buffer (if it was not full). Figure 3-11 shows the RHDB bit usage, and Table 3-12 provides a description of each bit.

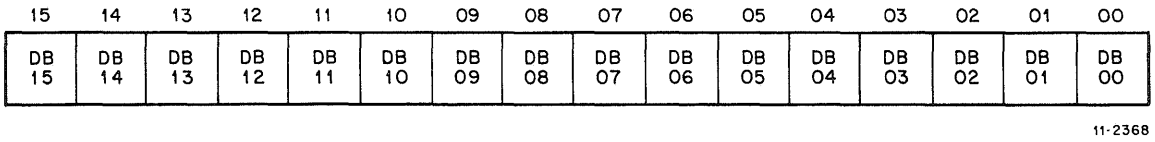


Figure 3-11 Data Buffer Bit Usage

Table 3-12
Data Buffer Bit Assignments

Bit	Set By/Cleared By	Remarks
15–00 DB(15:00) Data Buffer (15:00) Read/write	When read, the contents of OBUF (internal RH11 register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal RH11 register) and allowed to sequence into the Silo if space is available.	Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the DB is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data word read from the disk which did not compare with the corresponding word in memory is frozen in RSDB for examination by the program.

3.16 MAINTENANCE (RSMR) REGISTER (772064)

The Maintenance register is a 16-bit register which simulates various signals from the disk to allow diagnostic testing of the drive logic circuits. Read/write bits 00, 02, 03, 04, and 05 of this register control testing of functions in the RS04/RS03 disk control logic. The remaining bits display status of the RS04/RS03 disk format or encode/decode logic, and are read only bits. During diagnostic testing of the drive, the Clock signal from the disk is removed from the drive timing logic. Since Index pulses are derived from the Clock signal by the timing logic, the clock signal will no longer be generated and must be provided under program control. Read Data signals are also removed from the decode portion of the encode/decode logic. Signals generated by Maintenance register bits (MCLK, MIND, MRD) are then substituted in place of these disk signals. This allows a diagnostic program to step through the signal transitions which simulate a disk data transfer by writing repeatedly into this register. Figure 3-12 shows the RSMR bit usage, and Table 3-13 provides a description of each bit.

NOTE

When in diagnostic mode, data recorded on the disk surface is not destroyed during maintenance write operations.

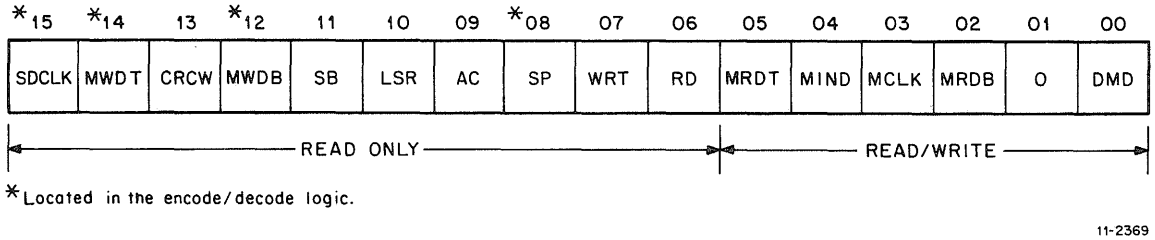


Figure 3-12 Maintenance Register Bit Usage

Table 3-13
Maintenance Register Bit Positions

Bit		Set By/Cleared By	Remarks
15	SDCLK Serial Data CLocK Read only		Displays the clock which clocks serial read data out of the data decoding logic during a read operation; or, clocks serial write data into the encoding logic during a write operation. In the RS03, one data bit is clocked for each SDCLK pulse; in the RS04, two data bits are clocked for each SDCLK pulse.
14	MWDT Maintenance Write DaTa (Top Surface) Read only		During a write operation, data received from the controller is displayed here in Miller encoded format bit by bit as MCLK pulses proceed. This data stream is normally written on the top surface in the RS04. Always read as a 0 in the RS03.
13	CRCW CRC Word Read only		When set, indicates that the CRC word is being read or written.
12	MWDB Maintenance Write Data (Bottom Surface) Read only		During a write operation, data received from the controller is displayed here in Miller encoded format bit by bit as MCLK pulses proceed. This data stream is normally written on the bottom surface.
11	SB Strobe Buffer Read only		Strobes data from the data bus into the drive's data buffer during a write operation; or, loads stored read data from the shift register into the drive's data buffer during a read operation.
10	LSR Load Shift Register Read only		Enables the shift register to accept parallel data from the drive's data buffer register during a write data transfer.
09	AC Address Confirmed Read only		Indicates that the current sector and the desired addresses are the same.
08	SP Sector Pulse Read only		Generated at the start of each sector and will be asserted for two MCLK cycles in the RS04 and one MCLK cycle in the RS03.

Table 3-13 (Cont)
Maintenance Register Bit Positions

Bit		Set By/Cleared By	Remarks
07	WRT WRiTe Read only		Indicates that the drive is performing a write operation.
06	RD ReaD Read only		Indicates that the drive is performing a read operation. This signal is not asserted for write-check operations.
05	MRDT Maintenance Read Data (Top Surface) Read/write	When DMD is set, this bit replaces the read data from the top surface read amplifier (data simulated by this bit will be transferred to the controller after 36 MCLK pulses in RS04).	The simulated data bit must be constant for two MCLK pulses in the RS04. This bit is not used in the RS03.
04	MIND Maintenance INDex Read/write	When DMD is set, this bit replaces the disk Index pulse.	An Index pulse is required to initialize the drive timing logic.
03	MCLK Maintenance CLocK Read/write	When DMD is set, this bit substitutes for the disk timing clock.	
02	MRDB Maintenance Read Data (Bottom Surface) Read/write)	When DMD is set, this bit replaces the read data from the bottom surface read amplifier (data simulated by this bit will be transferred to the controller after 18 MCLK pulses in RS03 and 36 MCLK pulses in RS04).	The simulated data bit must be constant for two MCLK pulses.
01	Not Used	Always read as a 0.	
00	DMD Maintenance Mode Read/write	When set, places the drive in the maintenance (diagnostic) mode. Cleared by Controller Clear or by writing a 0.	Drive clear does not clear any bits in the Maintenance register.

3.17 DRIVE TYPE (RSDT) REGISTER (772066)

This register allows the program to distinguish between different classes of drives. The register is located in the drive whose unit number appears in bits 02 through 00 of RSCS2. Figure 3-13 shows the RSDT register bit usage, and Table 3-14 provides a description of each bit.

The RSDT register is a read only register; writing into it will not cause an error and will not modify any of the status bits.

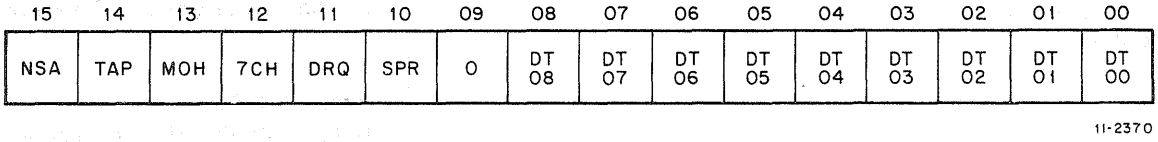


Figure 3-13 Drive Type Register Bit Usage

Table 3-14
Drive Type Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	NSA Not Sector Addressed Read only	This bit is 0 in drives which locate data by address.	Always 0 in RS04/RS03.
14	TAP TAPe drive Read only	Set in drives which are tape units.	Always 0 in RS04/RS03.
13	MOH MOving Head Read only	This bit is set in drives with moving head arms.	Always 0 in RS04/RS03.
12	7CH 7 CHannel tape Read only	Set in tape drives with 7-channel read heads.	Always 0 in RS04/RS03.
11	DRQ Drive ReQuest required Read only	Set when the drive may have dual controllers and use must be requested by the program.	Always 0 in RS04/RS03.
10	SPR Slave PResent Read only	In a drive which may have slave drives, this bit is 1 when the selected slave is present.	Always 0 in RS04/RS03.

Table 3-14 (Cont)
Drive Type Register Bit Assignments

Bit	Set By/Cleared By	Remarks
09 Not Used	Always read as a 0.	
08–00 DT(08:00) Drive Type Read only		These bits contain a unique number for each drive type. The following drive type numbers are assigned to RS04/RS03. 000_8 RS03 001_8 RS03 with sector interleave 002_8 RS04 003_8 RS04 with sector interleave

3.18 RH11/RS04/RS03 REGISTER SUMMARY

Figure 3-14 shows the bit assignments of the 12 registers in the RH11 and the RS04/RS03 disk drive, in a quick-look form for ease of reference. The registers are listed in sequential order by Unibus address.

3.19 FUNCTION CODES

The RS04/RS03 disk file is capable of executing the following function codes. (The Write-check, Write and Read function codes are designated data transfer commands.)

a. No Op – 01_8
b. Read In Preset – 21_8
c. Drive Clear – 11_8
d. Search – 31_8
e. Write-check – 51_8
f. Write – 61_8
g. Read – 71_8

These function codes are specified in bits 05 through 01 of the RSCS1 register and are described in the following paragraphs. (Function codes shown above include the GO bit, RSCS1 bit 00.)

3.19.1 No-Op, Function Code = 01_8 and Read In Preset, Function Code = 21_8

No operation is performed and the GO bit is immediately reset. No Attention condition will result from the command.

3.19.2 Drive Clear, Function Code = 11_8

Errors are cleared and the drive is initialized to the quiescent state. At the completion of the clear, the GO bit is reset by the drive. No Attention condition results from the command.

3.19.3 Search, Function Code = 31_8

The drive clears the drive ready bit (RSDS bit 07) and asserts the PIP bit (RSDS bit 13). When the current sector address (RSLA bits 11–06) matches the desired address (RSDA bits 05–00), the drive:

a. clears the GO and PIP bits.
b. sets DRY (drive ready) and ATA.
c. asserts Attention.

The RH11 will then interrupt the program if the IE bit is set and if the RH11 is not currently performing a data transfer operation with another drive. If the RH11 is busy at the time of the Attention, the interrupt does not occur until the data transfer operation has been completed.

The Search command does not clear the controller's RDY bit (RSCS1, bit 07).

RSCS1-772040

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	FO	GO

RSWC - 772042

WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

RSBA-772044

BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	0

RSDA-772046

SP 03	SP 02	SP 01	SP 00	TA 05	TA 04	TA 03	TA 02	TA 01	TA 00	SA 05	SA 04	SA 03	SA 02	SA 01	SA 00

RSCS2-772050

DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	UO

RSDS-772052

ATA	ERR	PIP	MOL	WRL	LBT	0	DPR	DRY	0	0	0	0	0	0	0

RSER-772054

DCK	UNS	OPI	DTE	WLE	IAE	AO	0	0	0	0	0	PAR	RMR	ILR	ILF

RSAS-772056

0	0	0	0	0	0	0	0	ATA 07	ATA 06	ATA 05	ATA 04	ATA 03	ATA 02	ATA 01	ATA 00

RSLA-772060

0	0	0	0	CS 05	CS 04	CS 03	CS 02	CS 01	CS 00	SF 05	SF 04	SF 03	SF 02	SF 01	SF 00

RSDB-772062

DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00

RSMR-772064

RWCLK	MWDT	CRCW	MWDB	SB	LSR	AC	SP	WRT	RD	MRDT	MIND	MCLK	MRDB	0	DMD

RSDT - 772066

NSA	TAP	MOH	7CH	DRQ	SPR	0	DT 08	DT 07	DT 06	DT 05	DT 04	DT 03	DT 02	DT 01	DT 00

11-2371

Figure 3-14 RH11/RS04/RS03 Register Summary

3.19.4 Write-Check, Function Code = 51_8

The RH11 clears the RDY bit (RSCS1 bit 07) and waits for the disk to rotate to the desired sector. When the drive has reached the correct sector, it will begin to transfer data words to the controller Silo buffer. As the first word reaches the output of the Silo, the RH11 requests a word from memory via the NPR facilities of the Unibus. Each time a word is present at the output of the Silo, the RH11 initiates an NPR sequence.

As each word is received from the memory, it is compared to the word at the output of the Silo. If the words do not compare, the WCE (Write-Check Error) bit is set and the word from the drive that did not compare is saved at the output of the Silo. If the words do compare, operation is continued until all the words have been read from the drive and checked at the output of the Silo. The RH11 then asserts the RDY bit and interrupts the program if the IE bit is set.

While the drive is performing the read operation, the GO bit is asserted. However, the drive may assert its DRY bit before the RH11 RDY bit is asserted since the RH11 must wait for all the words still contained in the Silo to be checked.

3.19.5 Write, Function Code = 61_8

The RH11 clears the RDY bit and starts filling the Silo buffer with data words read from memory on the Unibus. When there are 64_{10} words in the Silo or the RSWC register reaches zero (whichever occurs first), the RH11 signals the drive to begin searching for the desired address on the disk. When the drive reaches the correct sector, words are transferred from the Silo to the disk.

When the RSWC overflows to zero, the RH11 stops requesting data transfers on the Unibus. The RDY bit, however, will not be asserted until all the words in the Silo have been written and the drive reaches the end of the current sector. The RH11 then asserts the RDY bit and interrupts the program if the IE bit is set.

If the end of the transfer occurs other than on a sector boundary, the remainder of the last sector will be written as 0s.

3.19.6 Read, Function Code = 71_8

The RH11 clears its RDY bit and waits for the disk to rotate to the desired address. When the drive reaches the correct sector, it begins to transfer words to the controller Silo buffer. As the first word reaches the output of the Silo, the RH11 transfers it to memory via the NPR facilities of the Unibus. Each time a word is present at the output of the Silo, the RH11 initiates an NPR sequence. This operation is continued until all the words have been read from the drive and transferred to memory. The RH11 then asserts the RDY bit and interrupts the program if the IE bit is set.

While the drive is performing the read, its GO bit is asserted. However, the drive may assert its DRY bit before the RH11 RDY bit is asserted since the RH11 must wait for all the words still contained in the Silo to be transferred into memory.

3.20 INTERRUPT VECTOR ADDRESS

The interrupt vector address is set to 000204 and is jumper selectable. This is the same vector address as the RF11 and caution must be used in configuring systems with both RF11 and RH11 Controllers.

3.21 INTERRUPT PRIORITY LEVEL

The priority interrupt level for the RH11 is set at BR5. However, priority levels are plug selectable and may be changed to satisfy system operation.

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

This chapter describes the theory of operation of the RH11 Controller in two functional groupings – the register control path and the DMA path. These are described in detail in the following paragraphs.

4.2 REGISTER CONTROL PATH

The register control path provides the interface that enables the program to read from or write into any register in the RH11 or associated drive. Specific bits in these registers are designated as follows: 'read only' bits indicate that the program can read the status of these bits but cannot load them; 'write only' bits indicate that the program can load them but will read back a 0; 'read/write' bits indicate that the program may load them and read back the status.

The RH11 examines Unibus address bits 17 through 05 (17 through 06 if there are a total of more than 16 registers) to determine if the register being addressed is an RH11 register (Figure 4-1). The address field can be defined by a set of jumpers within the RH11. The Unibus address is compared with the set of jumpers and, if the two match, the addressed register is a valid RH11 register which enables the circuitry for a register function. If the Unibus address does not compare with the jumpers, the RH11 will not accept the address and will not initiate a data transfer with the processor.

4.2.1 Writing a Local Register

Unibus address bits 04 through 00 (05 through 00 if more than 16 registers are employed) select a cell in a read only memory (ROM) which specifies a unique register. The ROM outputs are register select signals (RSEL 04:00), two coded bits (M6 and M7), and a LOCAL/REM signal. Since this description involves accessing a local register (one contained in the RH11), LOCAL is generated at the output of the ROM as LOC/REM H. When this signal is unasserted or low and a register operation is being performed, a remote register is selected. Signals RSEL 01:00 and M6 and M7 are supplied to the register decoders to select one of the local registers. RSEL 04:00 is also supplied to the Massbus control logic, but is inhibited from the Massbus because a 'write local register' function is specified and REM remains unasserted.

Unibus control lines A0, C0, and C1 specify the direction of transfer and also specify byte or word addressing. When writing a register, the C0 and C1 lines are encoded for a DATO or DATOB (if byte addressing is specified). The A0, C0, and C1 control lines are supplied to a direction control network which generates IN, OUT, HI BYTE, or LO BYTE signals depending on the cycle desired. These signals are fed to the register decoder where they are used in decoding the various register enable signals.

The Unibus A data lines are connected to the RH11 and contain the data used to load the desired register.

When BUSA MSYN is received from the central processor (150 ns after the data, control and address are placed on the Unibus), a DEV SEL (device select) signal is generated which enables the register decoder to generate the appropriate enable signal for the register specified. Signal REG STR is created 85 ns later and is ANDed with the HI BYTE or LO BYTE signal and the specified register enable signal from the register decoder. The signals designated with IN are used for *writing* local registers; the signals designated OUT are used for *reading* local registers. For example, if it was desired to write into the WC (word count) register, the register decoders specify the WC IN L signal, which is ANDed with HI BYTE or LO BYTE and REG STR to generate a clock used to load the WC register. The data is clocked into the WC register at the time of REG STR. The trailing edge of this signal, which is 135 ns long, causes SSYN to be asserted. The central processor receives SSYN and lowers MSYN, which deselects the RH11 from the Unibus. The lowering of MSYN then causes SSYN to be lowered, and 75 ns after the lowering of MSYN, the address lines change and the cycle is completed.

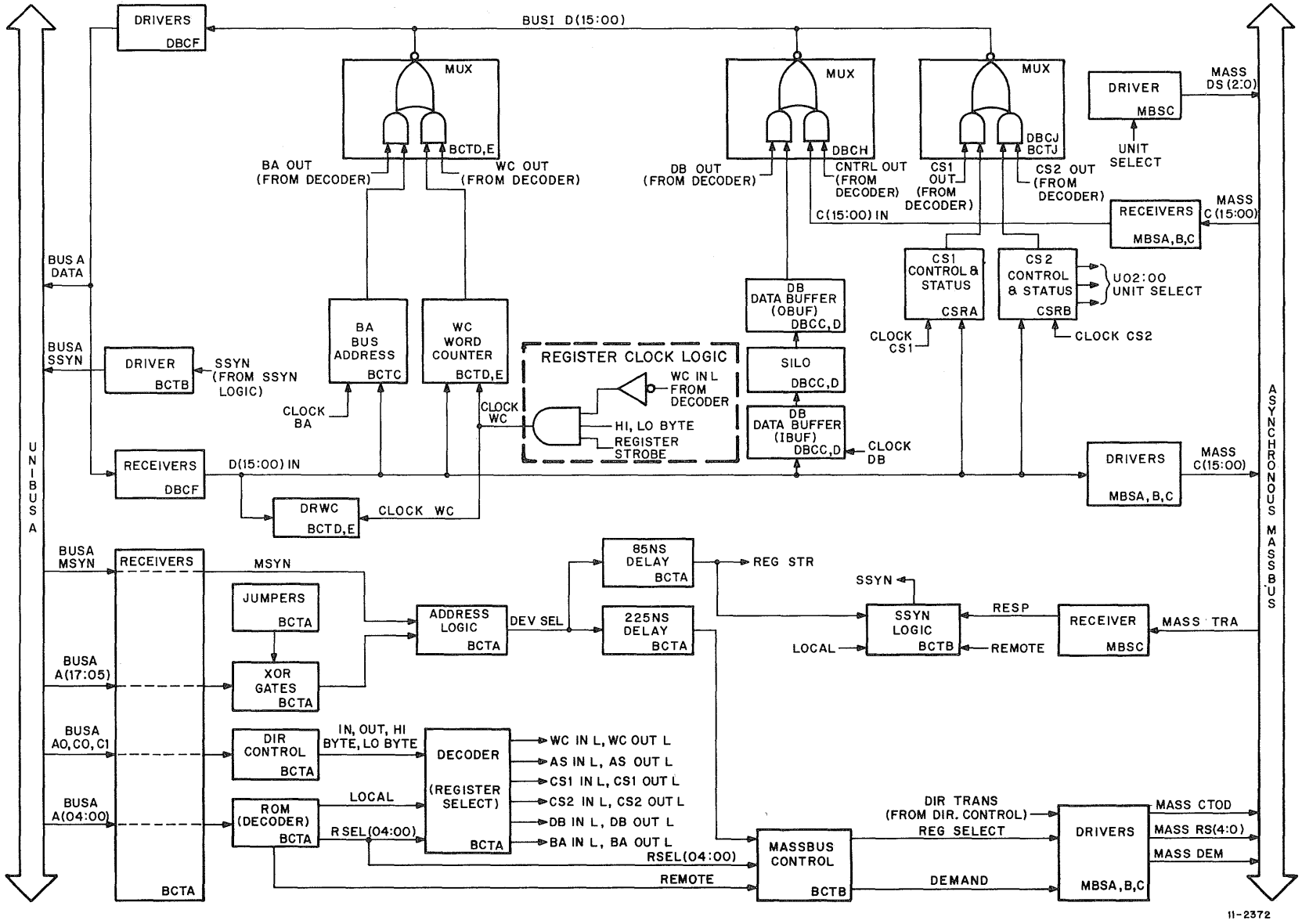


Figure 4-1 Register Control Path

4.2.2 Reading a Local Register

The process of reading a local register is the same as that described for writing a local register (Paragraph 4.2.1) with the following exceptions:

1. The C0 and C1 Unibus control lines are decoded for a DATI or DATIP operation.

2. When reading a local register, the register "OUT" signals of the register select decoders gate the contents of the register on the BUSI lines for transmission to the processor via Unibus A.

4.2.3 Writing a Remote Register (Figure 4-2)

A remote register is defined as a register located in the drive. The data path for writing a remote register is from Unibus A via data lines D00–D15 IN H on to the Massbus via control lines MASS C00–C15 H, where the data is received by the selected drive and loaded into the specified register in that drive. A CTOD (Controller to Drive) signal on the Massbus specifies the direction of transfer to the drive.

The upper address bits of the Unibus address are compared with a set of jumpers in the RH11 to enable the register selection logic, previously described. Unibus address bits 04 through 00 (05 through 00 if more than 16 registers are employed in the system) select a cell in the ROM (read only memory) which specifies a particular register. The outputs of the ROM are register select signals RSEL (04:00), two coded bits (M6 and M7), and the LOCAL/REM signal. The selected drive, whose unit number was preloaded by the programmer in the CS2 register, is specified by device select lines DS00 through DS02 on the Massbus.

When the MSYN signal is received over the Unibus by the RH11, the DEV SEL signal is enabled and a delay of 220 ns occurs before the RH11 issues DEM to the Massbus. This delay allows the select and data lines to settle and be decoded on the Massbus before the drive strobes the Massbus control lines. When the drive receives DEM and recognizes the unit address as its own and when the data has been clocked into the appropriate drive register, it issues transfer (TRA) to the RH11. When the RH11 receives TRA indicating that the drive has obtained the data, it issues SSYN to the processor. SSYN signals the processor that the slave (RH11) has finished the cycle, and the processor removes MSYN which, in turn, causes SSYN to go unasserted. Also MSYN going unasserted, removes the DEV SEL signal which causes DEM to drop. This action, in turn, causes TRA from the drive to go unasserted. The address and data is then removed from the Unibus and Massbus to complete the cycle.

4.2.4 Reading a Remote Register (Figure 4-3)

The process of reading a remote register is similar to that of writing a remote register with the following exceptions:

a. The data path for reading a remote register is from the drive to Massbus control lines C00 through C15 H, to the RH11 open-collector multiplexers (8234), to the BUSI lines, and then to the Unibus A data lines D00–D15.

b. Upon receipt of TRA when writing a remote register, SSYN is immediately sent to the CPU. When reading a remote register, however, SSYN is delayed 220 ns from transfer (TRA) to ensure that the data is present and settled on the Unibus.

4.3 DMA DATA PATH

Figure 4-4 is a block diagram of the DMA data path. The diagram shows three basic data flows – write, read, and write-check. These are briefly described below.

Write – Data is routed from the Unibus through two multiplexers (DMX and IMX) and into IBUF. The DMX multiplexer selects the data from Unibus A or Unibus B. If SEL BUS A is present, Unibus A is selected; if this signal is not asserted, Unibus B is selected. The IMX multiplexer selects the data from the DMX or from the Massbus depending on the function being performed. For a write function, the data at the output of IMX is from the Unibus and for a read or write-check function, the data is from the Massbus. The data words are gated into IBUF and bubble through the Silo to OBUF. For the write function, the data from OBUF is supplied to drivers and then to the Massbus data lines (MASS D00–D17).

Read – Data is routed from the Massbus data lines (MASS D00–D17) to IBUF through the IMX multiplexer. Just as in the write function, the data from IBUF bubbles through the Silo into OBUF. From OBUF, the data is gated onto Unibus A if SEL BUS A is present; otherwise, the data is gated onto Unibus B.

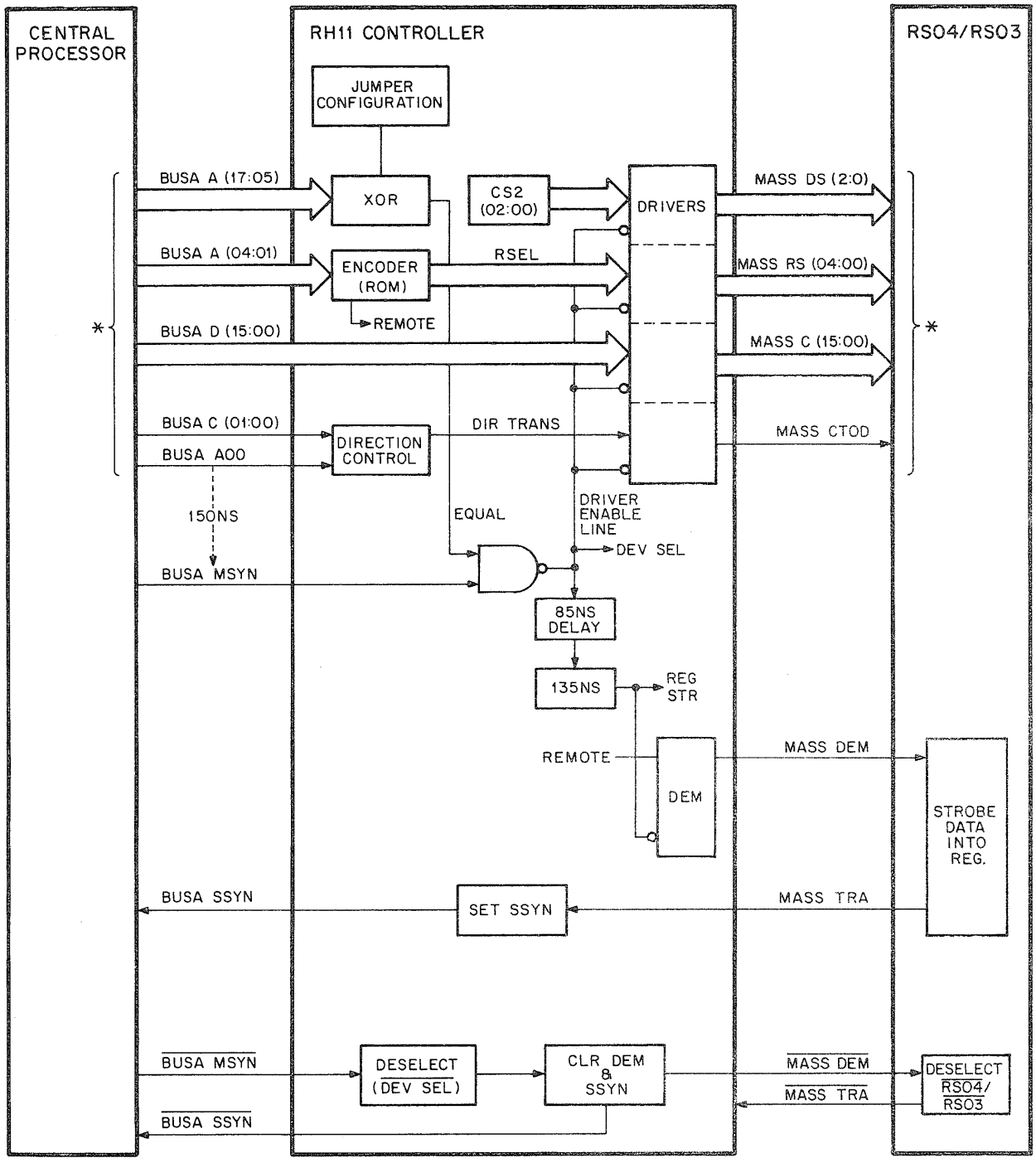
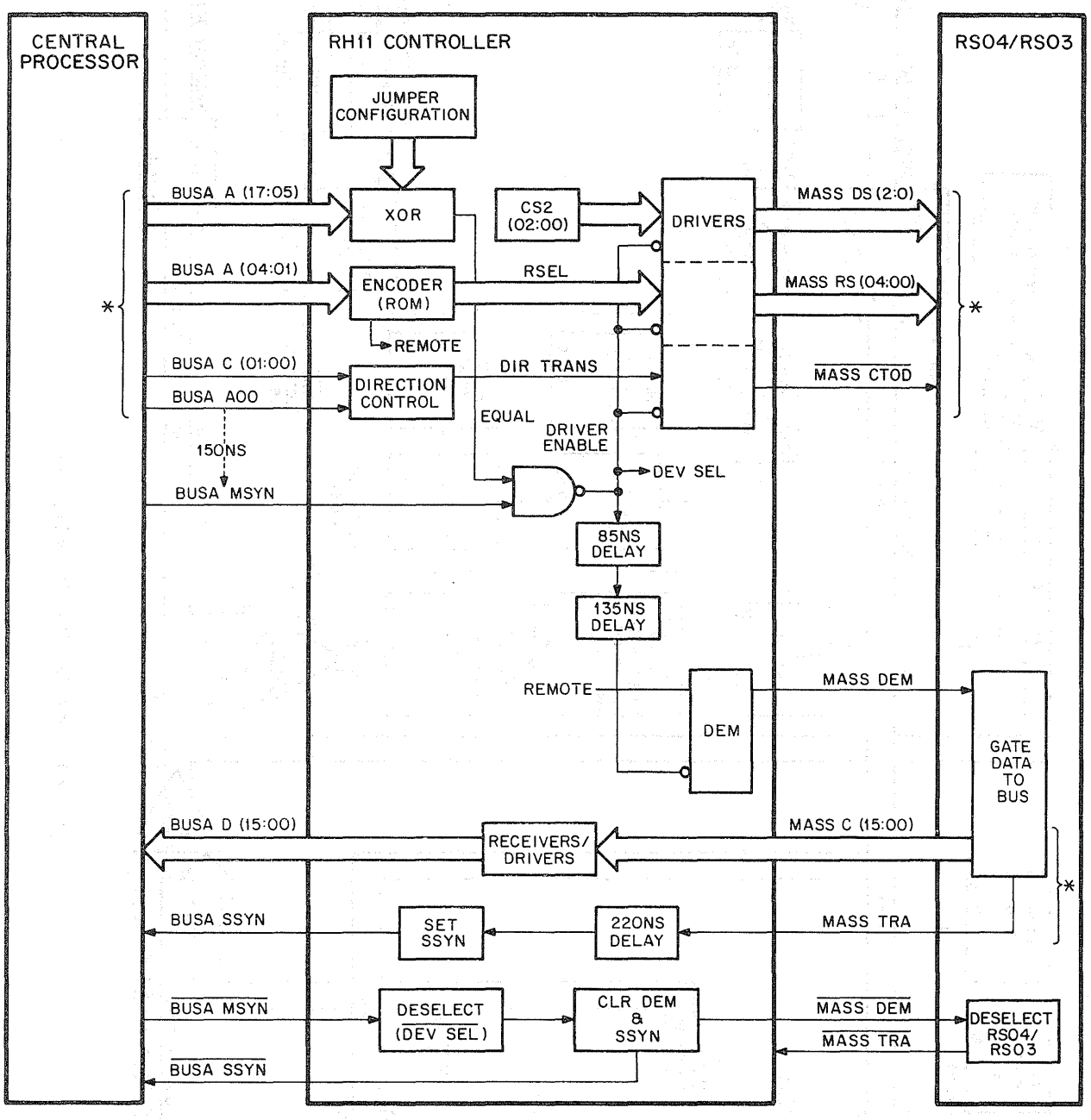


Figure 4-2 Writing Remote Register Interface



* ALL EVENTS WITHIN BRACKET OCCUR AT APPROXIMATELY SAME TIME.

11-2374

Figure 4-3 Reading Remote Register Interface

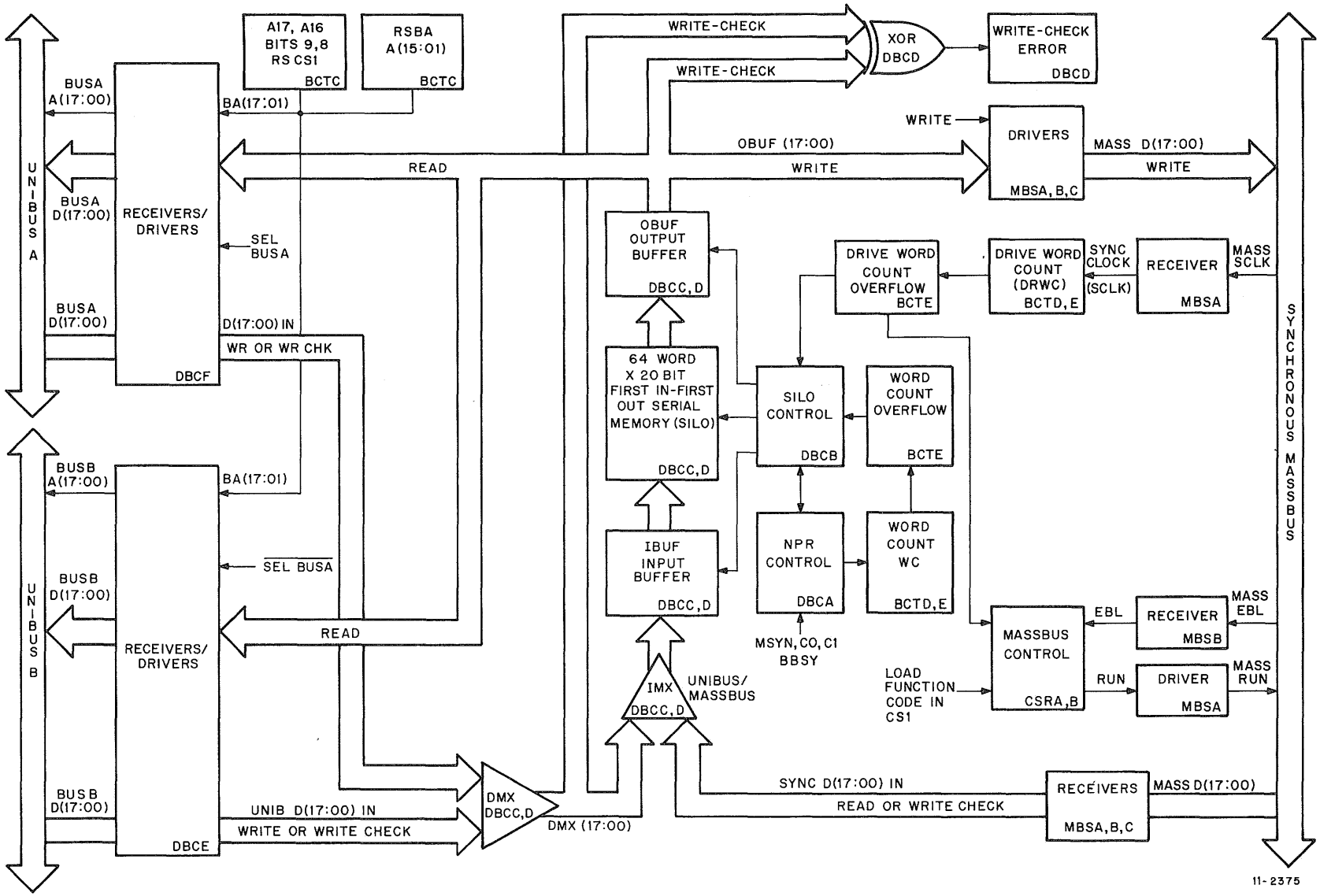


Figure 4-4 DMA Data Path Block Diagram

Write-Check – In the write-check function, the data that has previously been written onto the disk is compared with the contents of the memory locations that were the source of this data. In this way, errors in transmission can be easily detected. The data from the Massbus is fed through the IMX multiplexer into IBUF. From IBUF, the data bubbles through the Silo into OBUF and to a series of write-check Exclusive-OR gates. The second input to these gates is from the DMX multiplexer which contains data from the corresponding Unibus memory location. If the data from memory does not compare to the data read from the disk, a write-check error is flagged indicating a transmission error.

Figure 4-4 shows the bus address used to address memory on the Unibus. This is obtained from the BA register and from bits 9 and 8 of the CS1 register to form the 18 bit Unibus address. Both the word count (WC) and drive word count (DRWC) logic is shown. The word count keeps track of the number of words transferred between the Unibus memory and RH11 while the drive word count keeps track of the number of words transferred between the RH11 and the drive via the Massbus. When the WC register overflows, the RH11 ends the Unibus transfer; when the DRWC register overflows, the RH11 ends Massbus transfers.

In order to describe the data transfer operation of the RH11 in more detail, the following paragraphs present each function (read, write, write-check) as it interfaces between the Unibus and Massbus.

4.3.1 Write Block Transfer

Figure 4-5 is an interface diagram showing the action of the RH11 during a write data transfer. Initially, the desired address, bus address, selected unit, and word count are specified by the program. The desired address consists of the drive track and sector address desired to write on. This address is sent to the device and will be compared to the various sector addresses of the rotating disk. The bus address and word count are supplied to the RH11 and are monitored by circuitry in the RH11. The program, in this case, also specifies a write command code with the GO bit set (bits 5 through 0 of the CS1 register). The RH11 transfers the write command code and the GO bit to the selected drive and also examines the command code to enable the appropriate logic (memory reference, Silo control, data path, and Massbus control). The write command code and GO bit, which are sent to the drive, are stored in the drive's function register (bits 5 through 0 of CS1) and are decoded by the drive in order to determine the function to be performed.

NOTE

When a write command and the GO bit are loaded, the RH11 becomes busy and cannot accept another data transfer command.

The drive then waits for the RUN assertion from the Massbus before staring to search for the desired disk address where the data transfer will be initiated. The RUN signal is asserted by the RH11 when the Silo has been filled with a prescribed number of words, depending on the Silo capacity selected.

When the RH11 decoded the write command code from the program, it issued an NPR data request on the selected Unibus.

NOTE

The NPR request allows the RH11 to acquire bus mastership in order to transfer data directly to or from memory. This sequence is described in detail in Paragraph 5.7.

When bus mastership is granted to the RH11, the RH11 sends a memory address [stored in the bus address (BA) register and in bits 8 and 9 of the CS1 register] to memory via the Unibus. The RH11 asserts BUS MSYN 200 ns after the address is placed on the Unibus. The specified memory location responds with the data word in that location and the SSYN control signal. The data word is clocked into the IBUF register in the RH11, the WC register is incremented by 1, and the BA register is incremented by 2.

NOTE

The WC register is initially loaded with the 2's complement of the number of words to be transferred and is incremented toward 0 for each word transferred. The BA register is incremented by 2 since the RH11 is a word-oriented device and the PDP-11 memory system is byte-oriented.

If the first word of the Silo is empty at this time, the RH11 will initiate a second memory reference. If the first cell of the Silo is full or if this is the second memory reference of back-to-back NPRs, the RH11 will release control of the Unibus and will wait for IBUF to be empty before initiating another NPR request. When word count overflow occurs or an error is detected, the Unibus memory references are terminated.

NOTE

The RH11 can perform single-cycle or back-to-back memory references for each NPR request.

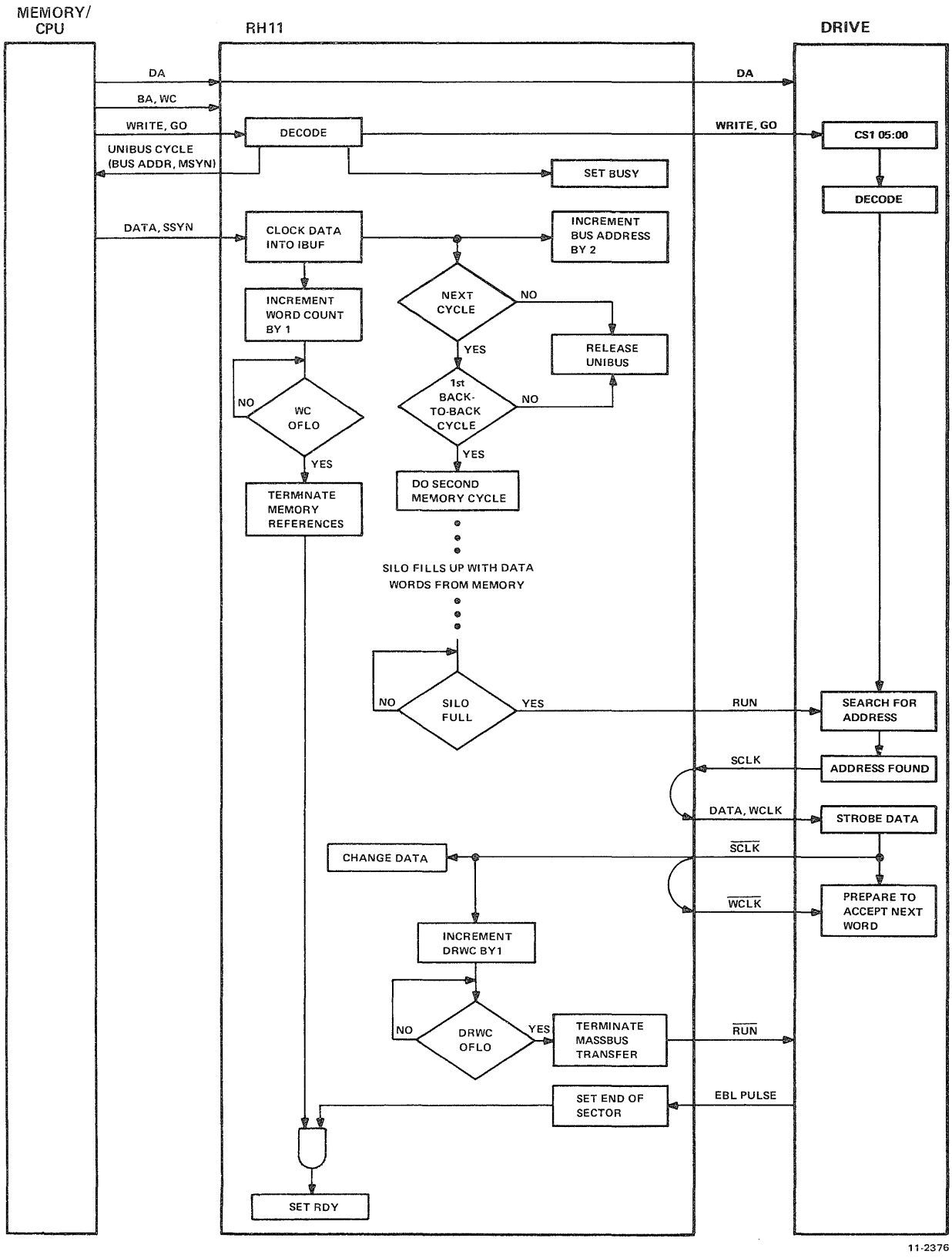


Figure 4-5 Write Cycle Interface Diagram

The data word which was clocked into IBUF from memory is automatically transferred to the bottom cell of the Silo if this cell is empty. If the cell is full, the data word in IBUF remains in IBUF until the data word in the bottom cell of the Silo has propagated to the next cell. Once a word is input to the Silo, it "bubbles" through the Silo to the last empty cell. Once a data word appears at the last cell of the Silo, it is clocked into the OBUF register, provided OBUF is empty. If OBUF is not empty, the data word remains in the last cell. Successive data words stack up in the Silo in a first in/first out (FIFO) sequence.

Each time a data word is input into IBUF, a start counter is incremented to determine how many words will be stacked in the Silo before the drive is signaled to begin the data transfer by the assertion of the RUN signal on the Massbus.

NOTE

There are four different Silo capacities which can be selected (Paragraph 5.19).

When the RUN signal is asserted on the Massbus and the drive has decoded a write command code, the drive starts to search for the desired address. When it has found the desired address, it issues synchronous clock (SCLK) signals on the Massbus. The SCLK is received by the RH11 and re-driven onto the Massbus as a write clock (WCLK) signal. The data word in OBUF is transferred to the drive on the leading edge of WCLK (leading edge of SCLK plus cable delay). The drive accepts the data word on the leading edge of WCLK. On the trailing edge of SCLK, the RH11 writes over the previous data word in OBUF with the word in the last cell of the Silo. A drive word count register (DRWC), which was initially loaded with the same value contained in the WC register, is incremented by 1 toward 0 for each word transferred. Successive words are transferred in this manner and when the required number of words are transferred, drive word count overflow occurs and the RUN line goes unasserted. If the number of words to be transferred is less than a complete sector, the drive is zero-filled in the remaining words in the sector. This action causes 0s to be loaded in the remainder of the sector by disabling the Massbus data drivers.

The drive signals completion of the sector with an EBL (End of Block) pulse. When the RUN signal is unasserted with the EBL pulse present, the data transfer is terminated and the RH11 transitions to the Ready state. If the number of words to be transferred is greater than a sector, the RUN line remains asserted at EBL time signaling the drive to continue transferring words to the next sector.

4.3.2 Read Block Transfer

Figure 4-6 is an interface diagram showing the action of the RH11 during a read data transfer. Initially, the desired address, bus address, selected unit, and word count are specified by the program as in the write block transfer. The program then loads a read command code with the GO bit set (bits 5 through 0 of the CS1 register). The RH11 transfers the read command code and the GO bit to the selected drive and also examines the command code to enable the appropriate logic (memory reference, Silo control, data path, and Massbus control). The read command and GO bit, which are sent to the drive, are stored in the drive's function register (bits 5 through 0 of CS1) and are decoded by the drive to determine the function to be performed.

NOTE

When a read command and the GO bit are loaded, the RH11 becomes busy and cannot accept another data transfer command.

The RH11 now asserts the RUN line on the Massbus to signal the drive to begin searching for the desired address specified. Once the drive has reached the desired address and begins to read the data, it presents a data word accompanied by SCLK on the Massbus. At the trailing edge of SCLK, the RH11 loads the data word into IBUF. In addition, the DRWC register is incremented. From IBUF, the data word automatically sequences through the Silo to the OBUF register. Successive words are transferred in this manner until the DRWC register overflows. When overflow occurs, the RUN line is negated and all remaining words in the sector are disregarded by the RH11. The drive indicates completion of the sector transfer by issuing an EBL (End of Block) pulse. If the RUN line is unasserted when EBL occurs, the data transfer is terminated and the RH11 becomes Ready as soon as the remaining Unibus memory references have been completed. If the number of words to be transferred is greater than the sector, the RUN line remains asserted at EBL time signaling the drive to continue transferring data words from the next sector.

The data words input to IBUF are propagated through the Silo. When the first data word reaches OBUF, an NPR request on the selected Unibus is issued and the WC register is incremented toward 0. This register is loaded with the 2's complement of the number of words to be transferred and incremented each time a word is loaded in OBUF.

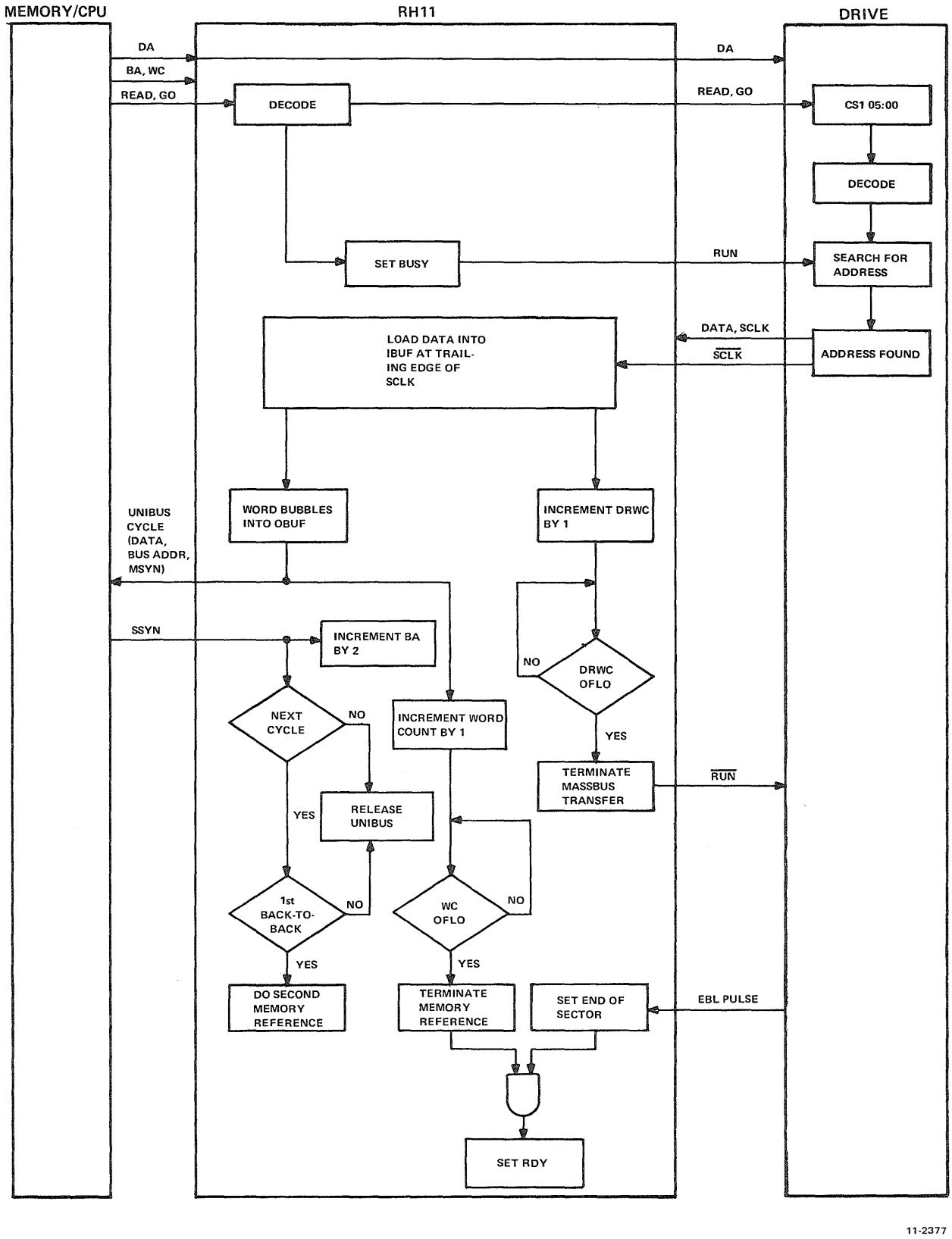


Figure 4-6 Read Cycle Interface Diagram

NOTE

The NPR request allows the RH11 to acquire bus mastership in order to transfer data directly to or from memory. This sequence is described in Paragraph 5.7.

When the RH11 acquires bus mastership, it sends a memory address (stored in the BA register and in bits 8 and 9 of CS1) and data (stored in OBUF) onto the Unibus. The RH11 issues BUS MSYN 200 ns after the data and address are placed on the Unibus. Memory acknowledges receipt of the data by asserting SSYN. The RH11 then removes MSYN and waits 75 ns before changing the data and address. After the data word has been transferred, the Bus Address register is incremented by 2 since the RH11 is word-oriented and the PDP-11 memory reference system is byte-oriented.

If there is a word in the top cell of the Silo when the data word is transferred from OBUF, the RH11 will maintain control of the Unibus for a second memory reference. If a word is not stored in the top cell of the Silo, or if this transfer is the second word of a back-to-back memory reference, the RH11 releases control of the Unibus and does not initiate a new NPR request until OBUF becomes full again.

NOTE

The RH11 can perform single-cycle or back-to-back memory references for each NPR request.

When word count overflow occurs or an error condition is present, the Unibus memory references are terminated. When the Unibus memory references are terminated and the drive reaches the end of the last sector, the RH11 transitions to the Ready state.

4.3.3 Write-Check Block Transfer

Figure 4-7 shows the interface diagram for a write-check operation. In a write-check operation, data written on the disk is validated by comparing it with the data in memory used to write it on the disk. This operation will reveal the addition or loss of any bits in the transmission process from memory to the disk via the RH11. This operation is similar to the read data transfer where the data is successively read from the disk, gated into IBUF (on the negation of SCLK), and propagated through the Silo. When the first data word reaches OBUF, an NPR request is initiated and a Unibus cycle allows the original data word from memory to be supplied to the RH11. The data word in OBUF is compared with its original counterpart from memory. If any bits do not compare, the WCE (Write-Check Error) bit is set and the word is 'frozen' in OBUF so that the program can examine the data word in error from the disk. If the bits do compare, the write-check operation continues until the final sector is checked or until an error is detected.

When the RH11 becomes bus master and requests a data word from memory, memory issues the data word on the Unibus accompanied by SSYN. When the RH11 receives SSYN, it waits 125 ns to deskew data on the Unibus and to allow the data to propagate through the XOR gates before MSYN is cleared.

4.4 WRITE FLOW DIAGRAM DESCRIPTION

Figure 4-8 is a detailed flow diagram of the write data transfer. Initially, the RH11 is in the Ready state and the program specifies the bus address, desired address, word count, and selected unit (specified in CS2). A Write command is loaded in bits 05 through 01 of CS1 and the GO bit is set in bit 00 of CS1. The Ready state in the RH11 is then cleared and the Silo is initialized. At this point the flow diagram divides into two asynchronous paths – one for the Unibus sequence of events and one for the Massbus sequence of events. The Unibus flow is discussed first inasmuch as a START signal, generated in this path, is necessary to initiate the Massbus flow.

4.4.1 Unibus Flow Description

When the Write command is loaded in CS1, DATA REQ is set. This signal asserts the BUS NPR line to request a Unibus cycle. The processor acknowledges the NPR by returning NPG (non-processor grant). The RH11, in turn, clears NPR and asserts SACK, indicating acknowledgment of the NPG. If a cycle is already in progress, the RH11 waits until BBSY and SSYN become negated. When this occurs, the RH11 asserts BBSY, indicating it is now bus master and negates BUS SACK. In addition, NPC MASTER is asserted which initiates the timing for the NPR cycles.

The Bus Address (BA) register and bits 9 and 8 of CS1 are then gated onto the Unibus in order to access the specified memory location. The C lines (C0 and C1) are encoded for a DATI cycle (data into the RH11, which is the master device). A delay of 200 ns is provided for deskewing on the Unibus. This deskew period allows the address and C lines on the Unibus to settle and also allows time for the memory to decode them.

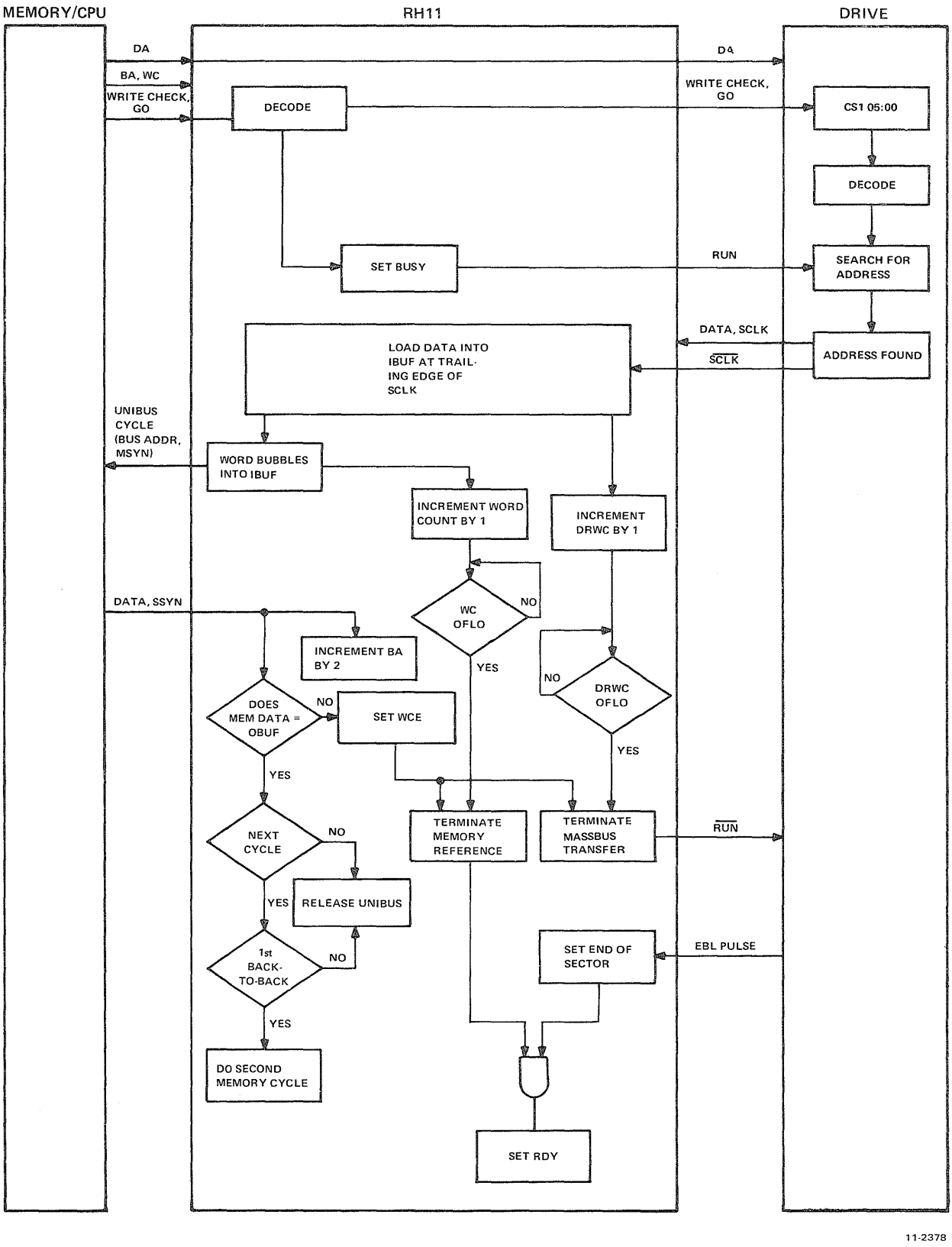


Figure 4-7 Write Check Cycle Interface Diagram

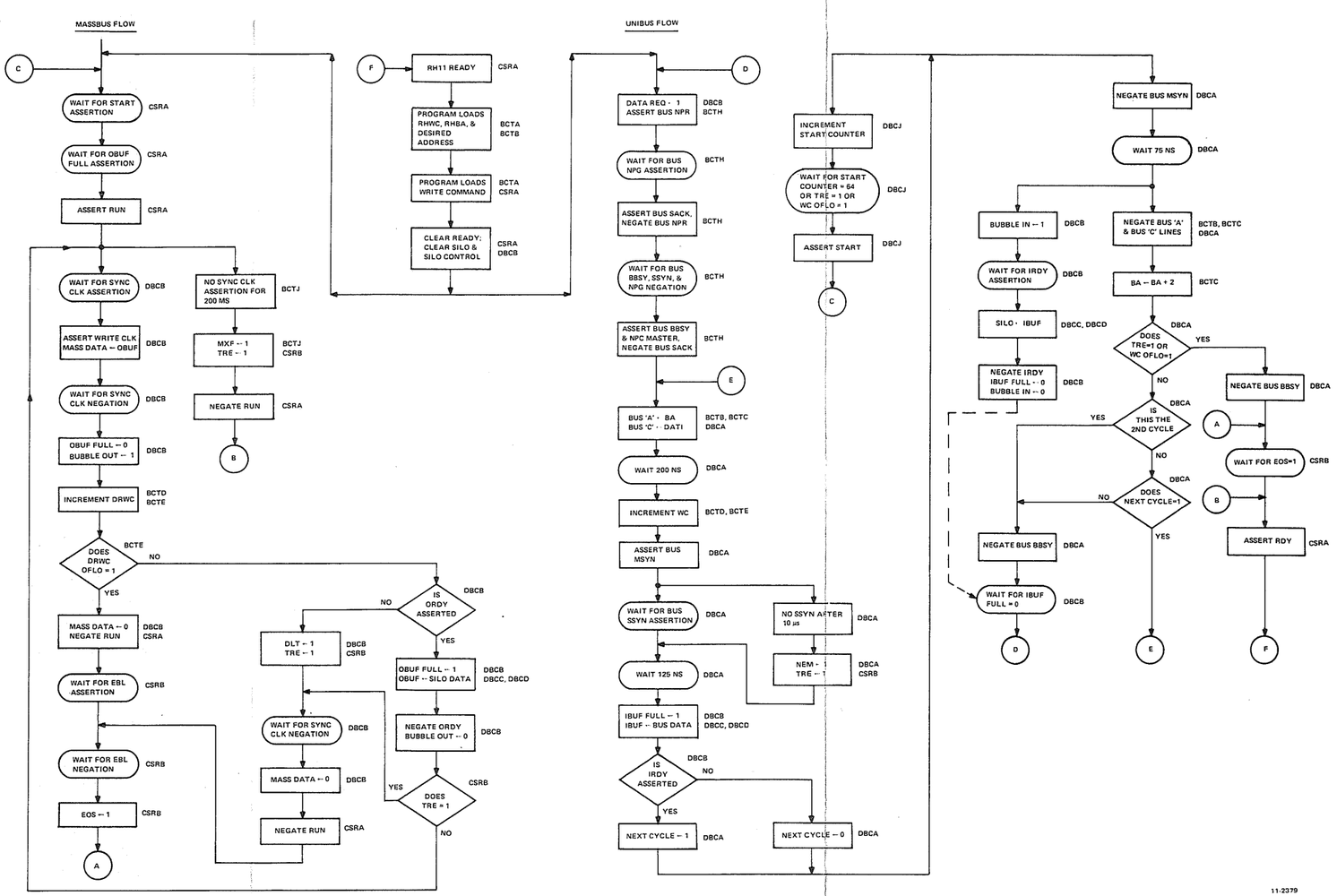


Figure 4-8 Write Command Flow Diagram

After the 200 ns deskew, the RH11 asserts BUS MSYN and increments the Word Count (WC) register. The RH11 then waits for SSYN to be returned from memory with the first data word. If SSYN does not occur within 10 μs of MSYN, the RH11 sets NEM (non-existent memory) error and TRE (transfer error). A 125 ns delay is provided for deskewing data on the Unibus and also provides time to allow the data to be internally gated to IBUF. After 125 ns, a DATA STR (data strobe) signal is generated. The leading edge of DATA STR clocks the data into IBUF and sets IBUF FULL. Also the status of the first cell in the Silo is checked (IRDY) and, if empty, NEXT CYCLE is set to allow back-to-back memory references.

The Unibus flow divides into two paths at this point. The first path checks to see if the START signal should be asserted; the second path provides the signals required to complete the present Unibus cycle and to start the new one. In addition, the second path allows the data from IBUF to be gated into the Silo and bubble up to the top; the second path will be described first, since the first path is used to initiate the Massbus flow when START is present.

MSYN is negated and a 75 ns delay is provided to allow the memory to deselect. This branch of the flow then divides into two simultaneously occurring operations. When BUBBLE IN is set, it triggers the logic to look for Input Ready (IRDY) at the input to the Silo. When IRDY is present, a SHIFT IN pulse is generated which clocks the data from IBUF into the Silo. If a word is in the first cell of the Silo, IRDY is inhibited until the word bubbles up to the next cell. When the Silo accepts the word from IBUF, it clears IRDY and the word begins to bubble up the Silo. When IRDY clears, BUBBLE IN and IBUF FULL clear. When the data reaches OBUF, it is ready to be transferred to the disk. However, the drive is not connected to the RH11 until the START signal is asserted.

This branch of the flow not only inputs data to the Silo but also shows the completion of the Unibus cycle. The Bus Address (BA) register is incremented by 2 to point to the next sequential memory word. The RH11 examines the WC for word counter overflow and also examines TRE. If word count has overflowed or if TRE is present, the second memory cycle is not performed, the address and C lines are removed from the Unibus, and BBSY is negated, which allows another device to become bus master. The RH11 waits for the drive to finish the transfer before going back to the Ready state. If TRE or word count overflow is not present, the status of NEXT CYCLE is checked and, if asserted during the first memory cycle of the back-to-back references, the flow then goes to point E to start the second memory cycle. If NEXT CYCLE is not asserted, or if it already is the second memory reference of a back-to-back cycle, BBSY is negated and the RH11 waits for IBUF FULL to clear before reinitiating an NPR sequence at point D in the flow diagram. The dotted input shown indicates that both parallel branches must complete before the flow can sequence to point D.

The first breakpoint in the flow previously described will now be discussed. It must be understood that this operation is occurring in parallel with what has just been described. DATA STR increments the START counter which counts up to 64. START is asserted when the counter reaches 64, or word count overflow occurs, or TRE sets.

NOTE

If TRE sets, START is asserted and generates the RUN signal which the drive is waiting for. On the first SYNC CLK from the drive, the RH11 sets an ERROR flip-flop. When ERROR is set, the synchronous bus data drivers are disabled, no more words are clocked out of OBUF, and RUN is negated at the next EBL pulse (which occurs at the end of the sector).

4.4.2 Massbus Flow Description

If the conditions causing the START assertion are not met, then this branch of the flow terminates until entered with the next Unibus memory cycle. When the START signal is asserted, the Massbus flow is initiated. With START asserted, the RH11 waits for OBUF FULL and then asserts the RUN line. By waiting for OBUF FULL, the RH11 ensures that a data word is available on the Massbus for the drive to accept.

When the RUN signal is set, the RH11 is connected to the drive and the RH11 now waits for the first SYNC CLK from the drive. If a SYNC CLK does not occur after 200 ms, the MXF (missed transfer) error is set which, in turn, sets TRE. This action clears the RUN line and returns the RH11 to the Ready state. When the SYNC CLK signal is received by the RH11, it is returned to the drive as a WRITE CLK signal. The data from OBUF has been gated on the synchronous bus data lines. On the trailing edge of SYNC CLK, OBUF FULL is cleared, BUBBLE OUT is set, and the Drive Word Count (DRWC) register is incremented. The DRWC register is checked for overflow. If there is overflow, the synchronous bus data drives are disabled which effectively writes 0s in the remaining word slots in the sector and the RUN signal is negated. The RH11 then waits for EBL. On the trailing edge of EBL, the RH11 sets the EOS (end of sector) and returns to the Ready state.

If drive word count overflow did not occur, the RH11 examines ORDY (output ready) at the trailing edge of SYNC CLK. This is done to ensure that a word is in OBUF in time for the next transfer. If ORDY is not asserted, a DLT (data late) error is raised which, in turn, causes TRE. The synchronous bus data drivers are disabled which causes 0s to be written in the remaining words in the sector. The RH11 then waits for the EBL signal from the drive, clears the RUN line, asserts the EOS signal, and returns to the Ready state.

If ORDY is asserted, the Silo data is clocked into OBUF and OBUF FULL is set. When the data word is gated from the Silo to OBUF, ORDY is cleared and BUBBLE OUT is cleared to prevent the next word in the Silo from being clocked into OBUF. When the next data word bubbles up to the top cell, ORDY is again asserted. If TRE is not present, the Massbus flow loops back and the RH11 waits for the next SYNC CLK from the drive, indicating the next word is to be transferred.

If TRE was set, the RH11 waits for the SYNC CLK negation before synchronizing the error condition. At this point the Massbus data drivers are disabled to cause a zero-fill in the rest of the sector. In addition, RUN is negated. At the trailing edge of EBL, End of Sector (EOS) is set and the RH11 returns to the Ready state.

4.5 READ FLOW DIAGRAM DESCRIPTION

Figure 4-9 is a detailed flow diagram of the read data transfer. Initially, the RH11 is in the Ready state and the program specifies the bus address, desired address, word count, and selected unit (specified in CS2). A read command is loaded in bits 05 through 01 of CS1 and the GO bit is set in bit 00 of CS1. The Ready state in the RH11 is then cleared, the RUN line is asserted which logically connects the RH11 to the drive, and the Silo and Silo control are initialized. At this point the flow divides into two asynchronous branches – the Massbus flow and the Unibus flow. The Massbus flow is described first because it is necessary to provide the first data word (ORDY assertion) to begin the Unibus flow.

4.5.1 Massbus Flow

The RH11 sits in a Wait state waiting to receive SYNC CLK signals from the drive.

NOTE

If there is no SYNC CLK after 200 ms, MXF error and TRE are set. The RUN line is cleared and the RH11 returns to the Ready state.

SYNC CLK is issued when the drive has found the address which matches the track and sector address set in the desired address register. The leading edge of SYNC CLK informs the RH11 that the drive has asserted a data word on the Massbus. On the trailing edge of SYNC CLK, the Drive Word Count (DRWC) register is incremented which indicates the number of words received from the synchronous bus. Also, the RH11 checks IBUF FULL.

If IBUF FULL is asserted indicating a word in IBUF, a DLT (data late) error is posted since there is no place to store the incoming data word. The RH11 then clears RUN. On the trailing edge of EBL, the EOS (End of Sector) is set and returns the RH11 to the Ready state.

If IBUF is not full, the data word from the Massbus is clocked into IBUF and the IBUF FULL flag is asserted. After a 150 ns delay (to allow the data in IBUF to be available to the Silo) the BUBBLE IN flip-flop is set. If Input Ready (IRDY) is not asserted (indicating the presence of a data word in the bottom cell of the Silo), the flow waits for IRDY to be asserted. As soon as IRDY is asserted, the BUBBLE IN flip-flop enables the data word to be clocked from IBUF into the Silo. When IRDY is negated, the IBUF FULL flag and BUBBLE IN are cleared, allowing a new word to be loaded into IBUF.

Each new data word from the drive is accompanied by SYNC CLK and on the trailing edge of each SYNC CLK, the drive word count is incremented indicating receipt of another word. The Drive Word Count register is loaded in parallel with the Word Count register. Both registers contain the 2's complement of the number of words to be transferred. DRWC register is now checked for overflow. If drive word count has not overflowed and there is no TRE, the flow loops back to point C and waits for the next SYNC CLK and the next data word. With TRE set or drive word count overflow, the RUN line is cleared. The RH11 waits for EBL, sets EOS on the trailing edge of EBL, and returns to the Ready state when the Unibus flow is completed.

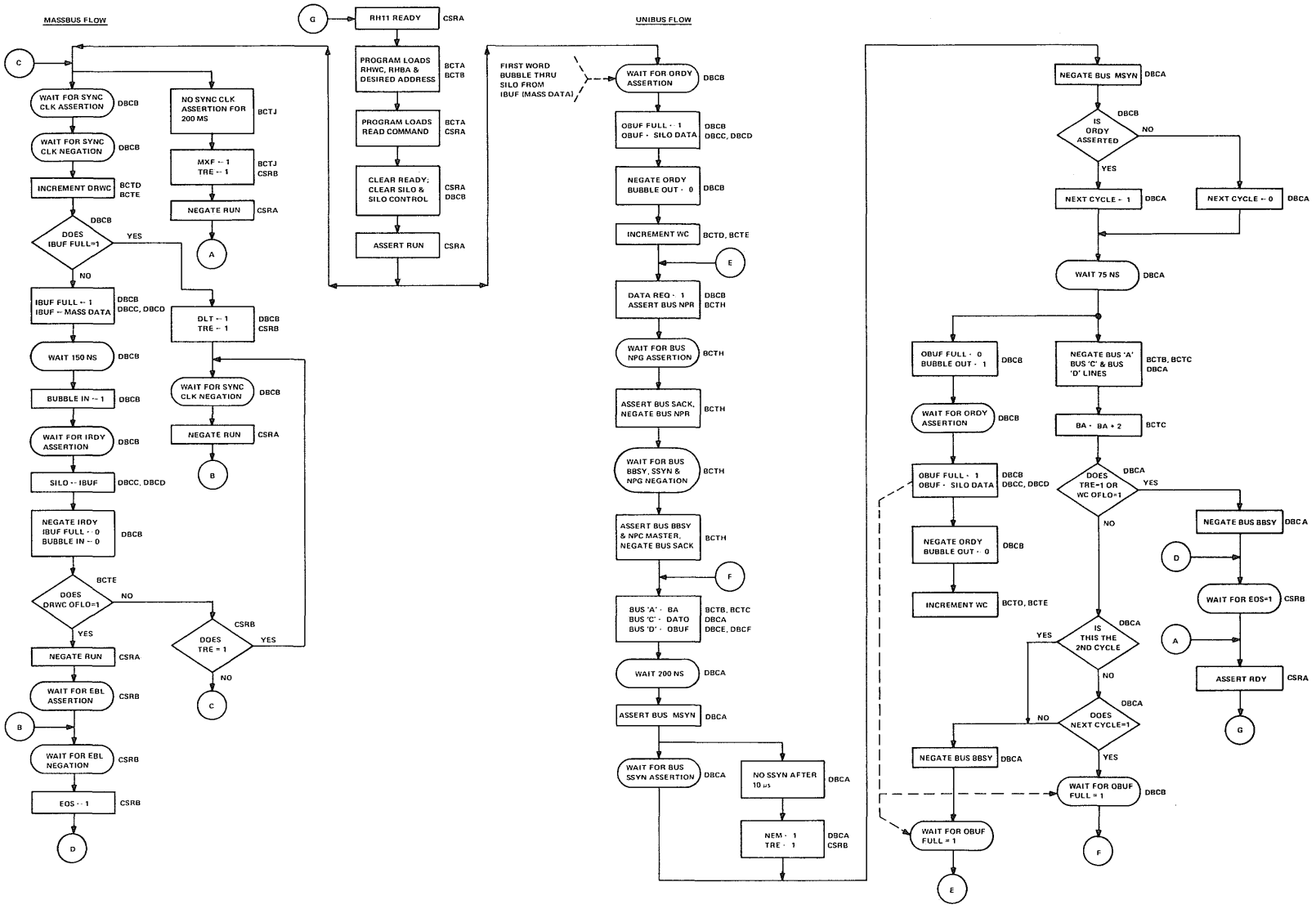


Figure 4-9 Read Command Flow Diagram

4.5.2 Unibus Flow

The Unibus flow is waiting for the first data word to be clocked to the top cell of the Silo. When this occurs, ORDY (output ready) is asserted. Since this is the first word, OBUF is not full and the data word is gated into OBUF, the OBUF FULL flag is asserted, BUBBLE OUT is cleared (previously initialized set), and ORDY is cleared. The word count is incremented. The condition of OBUF FULL being asserted causes DATA REQ to set, which enables the RH11 to assert BUS NPR. The RH11 waits for NPG (non-processor grant); upon receipt of NPG, the RH11 is the next device to gain control of the bus and asserts BUS SACK acknowledging receipt of NPG. BUS NPR is also cleared. The RH11 is waiting for BBSY and SSYN from the previous Unibus cycle to be removed. When this occurs, SACK is cleared and the RH11 asserts BBSY and becomes bus master.

The RH11 then asserts an NPC master signal, gates the bus address to the Unibus address lines, encodes the control lines (C0 and C1) for a DATO cycle, and gates the data from OBUF to the Unibus data lines. The RH11 now waits 200 ns to deskew the address, control, and data lines before BUS MSYN is asserted.

The RH11 asserts BUS MSYN and waits for memory to respond with SSYN. If the memory location specified by the bus address does not respond within 10 μs, the RH11 sets a NEM (non-existent memory) error, which causes TRE to set.

SSYN indicates that the memory has accepted the data word. At this time, MSYN is negated and the status of the Silo is checked (ORDY) to determine if another memory reference can be performed. If ORDY is asserted, NEXT CYCLE is set.

The RH11 then waits 75 ns after MSYN is negated before the address is removed or changed. The 75 ns deskew ensures that the memory is properly deselected. The flow now divides into two branches. The first branch finishes the Unibus cycle while the second branch allows data to bubble out of the Silo into the OBUF register. The first branch will now be described.

If a transfer error or word count overflow occurs, the address, control lines, and data are removed from the Unibus, the bus address is incremented by 2, BBSY is cleared, and the RH11 waits for the EOS produced by the trailing edge of EBL from the Massbus flow. If EOS is present with TRE or word count overflow, the RH11 goes to the Ready state. Both the Massbus and Unibus loops must complete before the RH11 goes to the Ready state. It is at this point that the two asynchronous loops merge in order to set Ready.

If there is no transfer error or word count overflow, the bus address is incremented, and if this is the second memory cycle or NEXT CYCLE is not set, BBSY is cleared. At this point, the flow stops and waits for OBUF FULL to set before looping back to point E and reinitiating an NPR cycle.

If the bus cycle was not the second one and the NEXT CYCLE flop is set, the RH11 waits for the next data word (OBUF FULL asserted) before starting the second back-to-back cycle. At this point, the flow loops back to point F.

The second branch, which begins after the 75 ns delay, allows data to be bubbled out of the Silo and into OBUF register. This is shown by OBUF FULL being cleared and BUBBLE OUT set to allow the data word in the top cell of the Silo to be transferred to OBUF. When ORDY is asserted, the Silo data is transferred to OBUF and OBUF FULL is set. The dotted lines indicate that this operation (OBUF FULL setting) allows the first branch to continue. When ORDY is negated, the BUBBLE OUT flip-flop is cleared and the WC register is incremented. The flow then ends until the next memory cycle causes this branch to be reentered.

4.6 WRITE CHECK FLOW DIAGRAM DESCRIPTION

Figure 4-10 is a detailed flow diagram of the write-check operation. This operation reads data from the device via the Massbus and stores the data in the Silo. When the data propagates through the Silo to OBUF, a Unibus cycle is performed to read the corresponding word in memory. This word is compared with the word from the drive which has propagated into OBUF. The comparison is accomplished by a series of Exclusive-OR gates. If the two words are equal (indicating no transmission errors), the OBUF FULL flag is cleared, and successive data words are compared until an error or until all words have been compared. If the two are not equal, the WCE (write-check error) bit is set which sets TRE, the word is frozen in OBUF, and the OBUF FULL flag remains asserted. Either the word read from the device and stored in OBUF or the word read from the Unibus could be in error. Since it is more difficult to access the word from the drive, this word is held in OBUF in the event of a WCE.

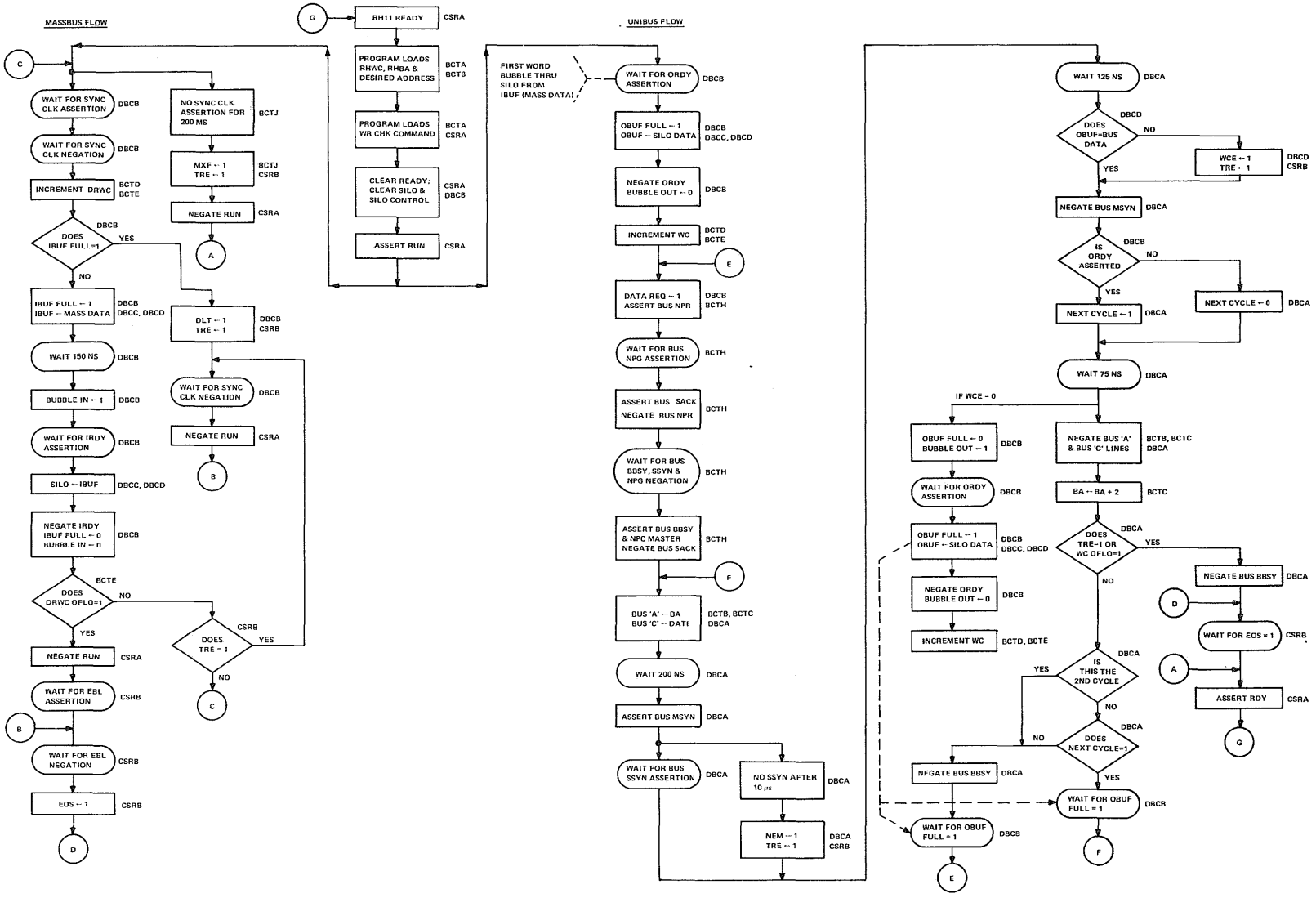


Figure 4-10 Write Check Command Flow Diagram

4.6.1 Massbus Flow Description

The description of the Massbus flow for the write-check operation is identical to the read operation (Paragraph 4.5.1).

4.6.2 Unibus Flow Description

The description of the Unibus flow for the write-check operation is similar to that for the read operation (Paragraph 4.5.2) with the following exceptions:

a. A DATI Unibus operation is performed to receive data from the specified memory location.

b. Upon receipt of SSYN from memory, the RH11 generates a 125 ns delay to deskew the data on the Unibus and to allow the data to propagate through the Exclusive-OR gates so that it may be compared with OBUF, and

c. If the data from memory and the data from the drive (stored in OBUF) do not compare, the WCE is posted and the parallel branch of the flow which transfers data from the Silo to OBUF is prevented from happening.

CHAPTER 5
DETAILED LOGIC DESCRIPTION

5.1 GENERAL

This chapter provides a detailed description of the RH11 logic diagrams. These descriptions should be used in conjunction with the flow diagrams in Chapter 4 to provide both an overall and detailed understanding of the RH11. The diagrams described in this chapter are tabulated in Table 5-1.

The M7295 module is designated BCT and is used for bus control; the M7296 module is designated CSR and is used for control and status; the M7294 module is designated DBC and is used for data path routing; and the M7297 module is designated PAC and is used for parity generation and checking.

Detailed timing diagrams (Figure 5-1, 5-2, 5-3, and 5-4) are also included in this chapter and may be used in conjunction with the detailed logic descriptions to show timing relationships between signals. Figure 5-1 is the Unibus timing diagram for a write operation; Figure 5-2 is the Unibus timing diagram for a read or write-check operation; Figure 5-3 is the Massbus timing diagram for a write operation; and Figure 5-4 is the Massbus timing diagram for a read or write-check operation.

5.2 BCTA LOGIC DIAGRAM

This diagram contains the register selection logic used by the program to select local RH11 registers or remote registers in the associated drive. The register address is supplied to 18 Unibus receivers (8838) via the Unibus. Bits 17 through 13 of the register address are asserted designating the I/O area. Bits 12 through 5 are fed to a series of jumper Exclusive-OR gates whose outputs are collector-ORed. If any of the output of these gates goes low, it forces the output line low as in the case where the Unibus address does not match the selected address of the RH11. The addresses to which the RH11 responds can be relocated by modifying the jumpers. If a jumper is left in, it represents a logic 0 and if it is cut, it represents a logic 1. The register address bits are asserted low on the Unibus. For example, address bit 12 is low at the input to the 8838 Unibus receiver. The output of this gate goes high. This is compared to the jumper intact which is low. The output of the Exclusive-OR gate, after inversion, is low and this drives the collector-ORed output line low to inhibit DEV SEL. On the other hand, if the jumper is out, (representing a 1), the Exclusive-OR gate compares two high inputs yielding a high output which enables the DEV SEL signal for that bit.

Bits 4 through 1 of the Unibus address are supplied to a 32-cell read only memory (ROM). A low logic level is supplied to the fifth address input to the ROM via the jumper selection at E3 and thereby allows 4 address bits to specify one of 16 cells in the ROM. The contents of the specified cell represents a specific pattern on the eight output signals (M0 through M7) of the ROM.

These outputs are used to provide the appropriate register signals. Each cell represents a different register address. If more than 16 registers are required for a particular RH11 system, the jumpers at E3 shown below the address jumpers are selected to feed bit 5 of the Unibus address to the ROM. As a result, one of 32 cells in the ROM can be specified, and Unibus address bit 5 is not compared at the Exclusive-OR gates which enable a DEV SEL signal.

Table 5-1
Listing of RH11 Logic Diagrams

Logic Print	Functions
BCTA	Register Selection
BCTB	Unibus A Address Drivers; SSYN; DEMAND
BCTC	Bus Address Register
BCTD	Word Count Register (07:00)
BCTE	Word Count Register (15:08)
BCTF	Interrupt Control
BCTH	NPR Control
BCTJ	MXF; Data Out MPX; MB INIT
BCTK	PROM Truth Table
CSRA	Control and Status Register CS1
CSRB	Control and Status Register CS2 and Error Status
DBCA	NPR Control Logic
DBCB	Silo Timing Control
DBCC	Silo Data Path (11:00)
DBCD	Silo Data Path (17:12)
DBCE	Unibus B Data Transceivers
DBCF	Unibus A Data Transceivers
DBCH	Unibus Parity Control and Data Out MPXs
DBCJ	Start Control and Data Out MPXs
PACA	Parity Control (Massbus Parity Detection and Generation)
MBSA	Massbus Transceiver (Massbus Cable A)
MBSB	Massbus Transceiver (Massbus Cable B)
MBSC	Massbus Transceiver (Massbus Cable C)
BUSA	Unibus A Cable Diagram
BUSB	Unibus B Cable Diagram
M9300	Unibus B Terminator
G727	Grant Continuity Module

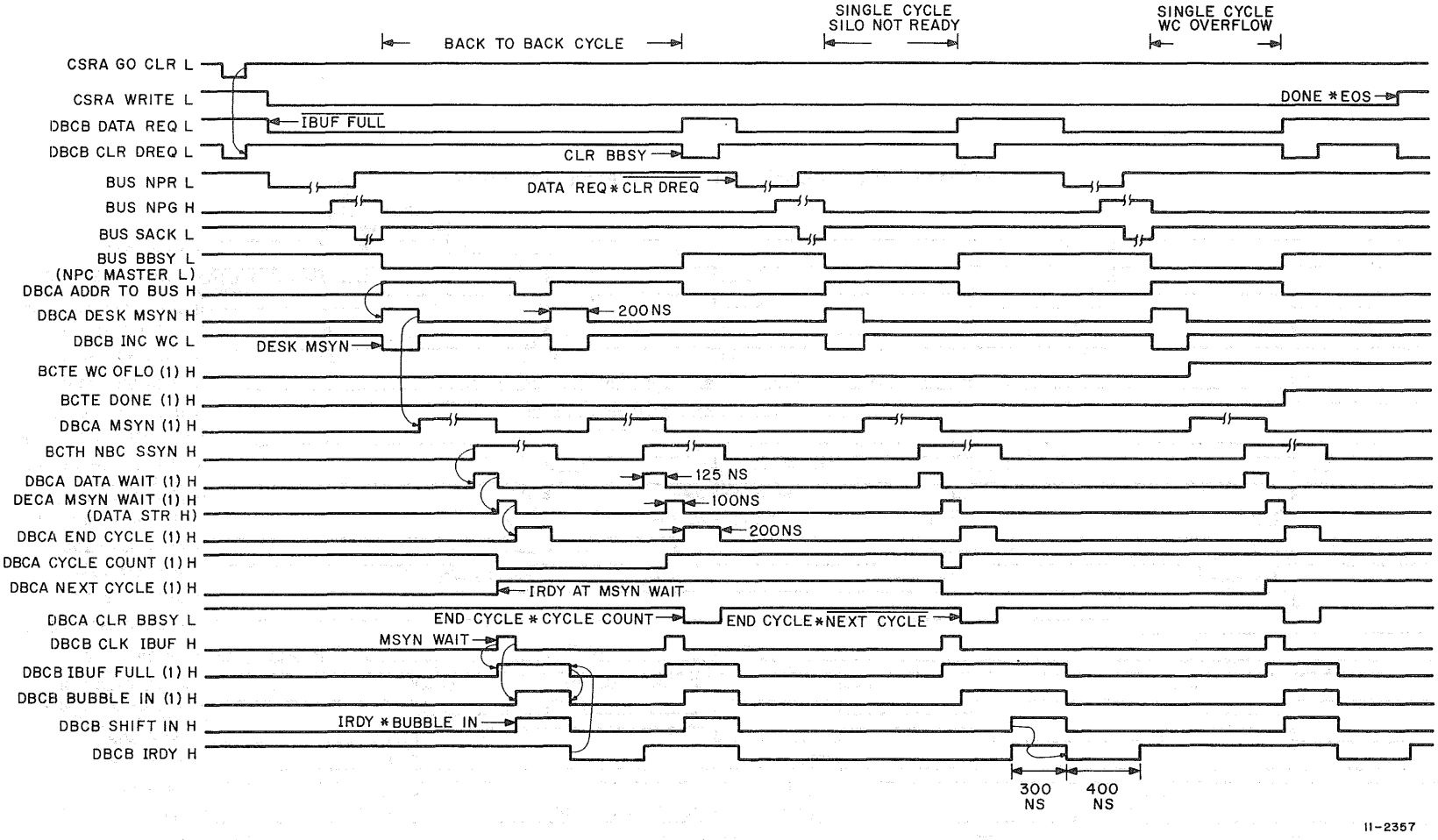


Figure 5-1 Write UNIBUS Timing Diagram

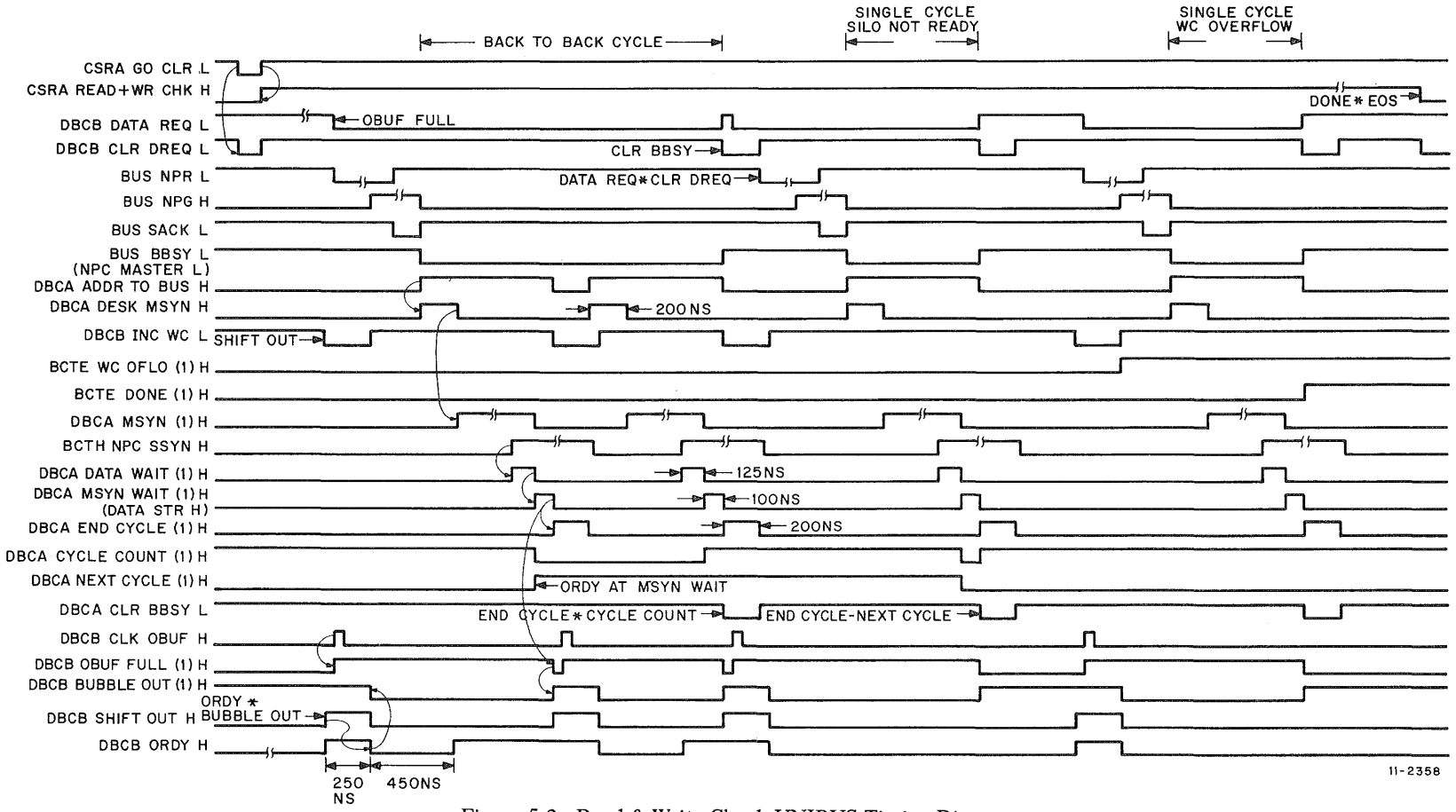


Figure 5-2 Read & Write Check UNIBUS Timing Diagram

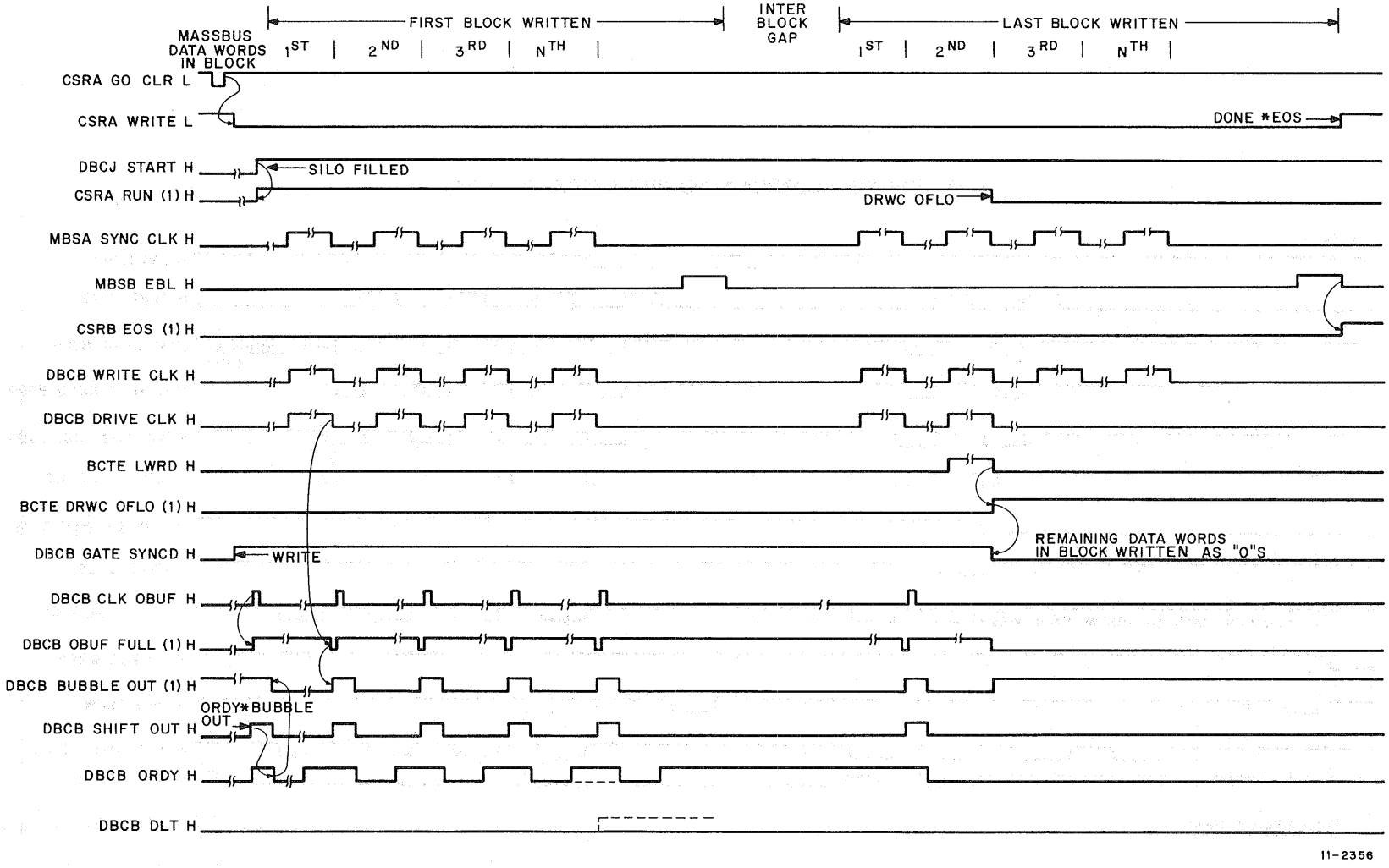


Figure 5-3 Write MASSBUS Timing Diagram

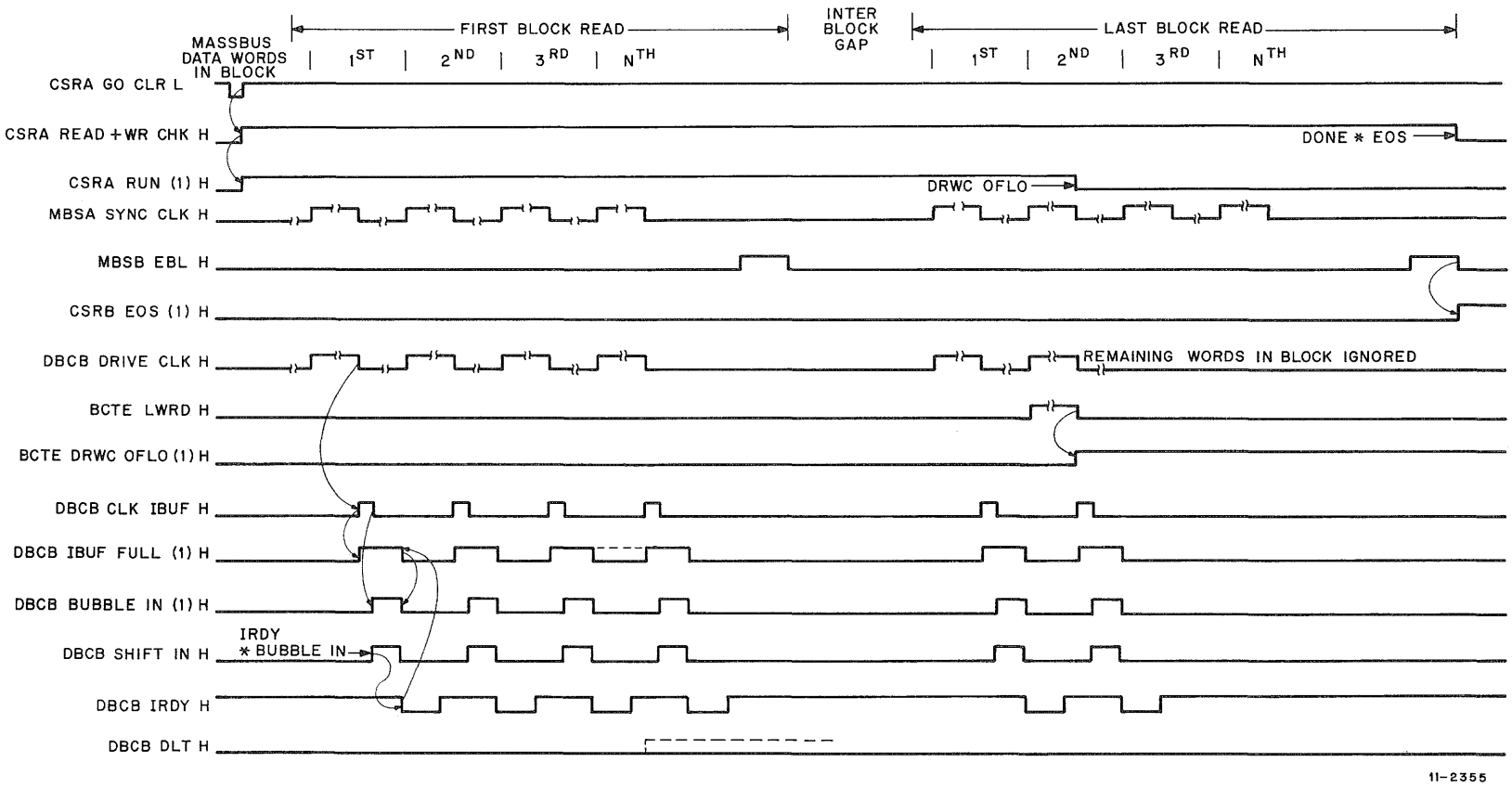


Figure 5-4 Read & Write Check MASSBUS Timing Diagram

In addition, the four most significant address bits which are applied to the ROM are compared against a jumper setting which define the exact number of registers used in the system. Each of these jumpers is weighted by the value assigned to it. If a jumper is removed, the RH11 will respond to the number of registers designated by the removed jumper. This number is added to the base address set by the address select jumpers on the Exclusive-OR gates. For example, if 12 registers are used in the system, the jumpers weighted 8 and 4 are removed. A Unibus address between the base address and the base address +11 words would be a valid register address. A Unibus address equal to or greater than the base address +12 words will cause the Logal REG output of the comparator to go unasserted, thus preventing the SSYN response.

NOTE

MSYN is delayed for 150 ns by the processor to allow the jumper Exclusive-OR gate decoder sufficient time to decode the address of the selected register. The MSYN signal then keys the DEV SEL signal which starts the register strobing sequence.

5.2.1 Local/Remote Register Selection

In addition to encoding the register address, the ROM asserts the LOC/REM H signal if a local register is being accessed. The Massbus handshaking sequence necessary to access a register located in a drive is inhibited in this case. If a remote register is being addressed, the LOC/REM H signal is not asserted (the Massbus handshaking sequence is enabled) and the DEMAND signal is initiated.

NOTE

The CS1 register is shared by the RH11 control and the associated drive. The LOCAL/REM H signal is not asserted to address this register. If LOC/REM H is asserted, the Massbus handshaking sequence is inhibited. This would prevent access to the portion of the CS1 register located in the drive.

5.2.2 RSEL Signals

The RSEL 04 through RSEL 00 signals from the output of the ROM are supplied to the Massbus which will be decoded in the drive to select a specific register. In addition, RSEL 00 and RSEL 01 are supplied to the lower of two 7442 BCD-to-decimal decoders and are used when the LOCAL/REM signal is asserted. The lower decoder decodes the CS2, DB, and BA registers and whether an input (from processor to RH11) or output (from RH11 to processor) function is to occur.

5.2.3 Decoder Inputs

Inputs D0, D1, and D2 to the decoder specify one of 8 outputs from 0 through 7 (outputs 3 and 7 are not used). RSEL 00 and RSEL 01 are applied to inputs D0 and D1 of the decoder, respectively, and specify one of the three above mentioned registers. BUSA C1 is applied to input D2 of the decoder and specifies an input or output function. When BUSA C1 L is asserted, the D2 input to the decoder is low enabling the register codes on outputs 0, 1, and 2. This indicates a DATO or DATOB where the data is transferred from the master (processor) to the slave (RH11). The register signal names incorporate the word "IN" denoting a 'write register' operation. When BUSA C1 L is not asserted, the D2 input to the decoder is high enabling the register codes on outputs 5, 6, and 7. This indicates a DATI or DATIP where the data is transferred from the slave (RH11) to the master (processor). The signal names are designated with the word "OUT" denoting a 'read register' operation. Input D3 is asserted low if the LOCAL REM H signal indicates a local register is addressed and DEV SEL H is asserted.

5.2.4 Decoder Outputs

With input D3 low, outputs 0 through 7 are enabled. If input D3 is not asserted, the outputs from 0 through 7 are inhibited and the decoder outputs are switched to 8 and 9 which are not used. Since the RSEL 04 through RSEL 00 signals are not used for selecting a drive register when the LOC/REM H signal is asserted, it is possible to redefine the two bottom bits of the ROM (RSEL 00 and RSEL 01) to be used as inputs to the decoder.

The upper decoder is similar to the lower one with a few exceptions noted below.

- Input D2 operates exactly the same as described for the lower decoder.
- ROM outputs M6 and M7 are used to decode the registers (WC, AS, CS1) associated with the upper decoder and are applied to inputs D0 and D1, respectively.
- Input D3 is enabled when DEV SEL L is asserted. LOC/REM H is not required since the M6 and M7 outputs of the ROM are not dual defined and may be used anytime.

5.2.5 Word or Byte Addressing

The logic network with the A0, C0, and C1 inputs determines whether word or byte addressing is required and whether an input or output function is occurring. The network implements the chart shown below.

C1	C0		
0	0	DATI	
0	1	DATIP	
1	0	DATO	
1	1	DATOB	if A00 = 0, low byte is specified. if A00 = 1, high byte is specified.

5.2.6 Control Lines

The C0 and C1 lines from the Unibus generate the DIR TRANS (direction of transfer) signal. When this signal is asserted, the direction of data transfer is from the RH11 to the drive register via the Massbus. When the signal is not asserted, the direction of data transfer is from the drive register to the RH11, and then to the Unibus to be made available to the program. The DIR TRANS signal is used to form the CTOD signal on the Massbus.

5.2.7 ODD BYTE L Signal

The ODD BYTE L signal is asserted when performing a DATOB to the high byte and is used to generate DIS DEM (disable demand). This is done to prevent the low (even) byte of the CS1 register from changing to the upper byte when the program is doing a byte operation (this is necessary since the Massbus does not implement byte operations and writeable bits in the low byte of CS1 are located in the drive).

5.2.8 Device Select (DEV SEL) Logic

The upper portion of BCTA shows the DEV SEL logic and the deskew demand logic. Bits 17 through 5 of the Unibus A address are used to generate DEV SEL L when MSYN occurs. MSYN is delayed from the address 150 ns to allow the address to be properly decoded by the jumper Exclusive-OR gates.

The negative-going edge of the DEV SEL L signal triggers one-shot multivibrator E63. The external components associated with this multivibrator are chosen to provide an 85 ns delay. Consequently, the negative-going edge of DEV SEL causes an 85 ns negative-going pulse at the 0 output of the one-shot. The positive-going trailing edge of this one-shot triggers a second one-shot with external components chosen for a delay of 135 ns. A positive-going pulse of 135 ns from the 1 output and a negative-going pulse of 135 ns from the 0 output are available.

5.2.9 Deskew Demand (DESK DEM)

The output of the second one-shot is designated DESK DEM (1) H or DESK DEM (0) H and provides a total delay of 220 ns before DEMAND is issued to the Massbus (see logic diagram BCTB).

5.2.10 Register Strobe (REG STR)

A REG STR signal is generated 85 ns after MSYN and is used for clocking the local registers.

5.2.11 Control Out (CTRL OUT) Signal

The CTRL OUT L signal is used when reading a remote register in the drive. CTRL OUT L is generated when the LOC/REM H signal is not asserted (remote mode), DEV SEL is asserted, and the BUSA C1 L signal is not asserted. This signal switches the multiplexer on logic diagram DBCH to gate the Massbus asynchronous data to the Unibus data lines making the register information available to the program.

5.2.12 Gate Control (GATE CNTL) Signal

The GATE CNTL H signal is used when writing into a remote register in the drive. GATE CNTL L is generated when DIR TRANS and DEV SEL signals are asserted and gate the Unibus data signals to the Massbus control lines.

5.3 LOGIC DIAGRAM BCTB

This sheet contains the DEMAND, SSYN, and NED logic and also contains the Unibus A address drivers used to gate the bus address to the Unibus.

5.3.1 Deskew Demand (DESK DEM) Logic

The DESK DEM (0) H signal from sheet BCTA is delayed 220 ns from MSYN and sets the SET DEM flip-flop. When set, this flip-flop causes DEMAND to be set, provided the TRANS (transfer) signal is not present on the Massbus. The TRANS signal is generated in the drive when the drive is ready to accept data or has data for transfer to the RH11.

5.3.2 Response from Drive

TRANS generates RESP L (response), indicating that the drive has responded to the controller. If no response occurs within 1.5 μs, a non-existent drive has been accessed. In this case, the NED (non-existent drive) flip-flop on BCTB is set.

5.3.3 SSYN Logic

The SSYN logic is used to determine when SSYN is sent to the Unibus. Each of the various methods of setting SSYN is described below.

Setting SSYN-Writing Remote Register (register electrically located in the drive) – When the program writes a remote register via the RH11, the unit select bits, the RSEL 04 through 00 signals, and the data are gated onto the Massbus. The unit select bits select the specified unit and the RSEL 04 through 00 signals select the appropriate register in that unit. If the RH11 is writing into a remote register, DIR TRANS H is asserted. After a 220 ns deskew period, the RH11 asserts DEMAND on the Massbus. When the drive sees DEMAND and recognizes its own unit select code and register address, it takes the data and issues TRANS which generates RESP in the RH11. Consequently, since DEMAND (1) H is asserted (accessing a remote register), DIR TRANS H is asserted (controller-to-drive transfer), and RESP L is asserted, gate E83 at zone D-6 generates SET SSYN L which is applied to the direct set input of the SSYN flip-flop.

NOTE

The Attention Summary register is a 1-bit pseudo register. When this register is accessed, more than one drive may respond. Therefore, the TRANS signal cannot be used to indicate the availability of data. In order to ensure that all drives have their respective Attention Summary bits loaded, a 1.5 μs delay is incorporated before the setting of SSYN.

Setting SSYN-Reading Remote Register – If the RH11 is reading a remote register (accepting data from the drive), the drive after recognizing its unit select code, register address, direction of transfer, and DEMAND, issues TRANS which generates RESP L in the RH11. Since DIR TRANS H is unasserted at this time (drive-to-controller transfer), a 200 ns one-shot multivibrator (E93) is fired. The external components are selected to provide the 200 ns pulse. This delay is designed to allow the data from the drive to propagate to the RH11 and onto the Unibus before SSYN is set. In other words, SSYN cannot be asserted on the Unibus until the data from the drive has been transferred to the Unibus and has stabilized. Consequently, when the one-shot fires, the 0 output goes low for 200 ns forcing the clock input to the SSYN flip-flop low for this period. At the end of 200 ns, the positive-going trailing edge of the 200 ns pulse sets SSYN which is asserted on the Unibus.

Setting SSYN-Access Local Registers – SSYN is set during the access of local registers as a result of REG STR H and DIS DEM H being asserted. REG STR H is generated 85 ns after MSYN on logic diagram BCTA and is used as a strobe input to the local register being accessed. Signal DIS DEM H indicates that the Massbus cycle is inhibited and a local register is being accessed. At the trailing edge of the REG STR signal, SSYN is set indicating that data has been accepted or is present on the Unibus when writing or reading a local register.

One-Shot Multivibrator (1.5 μs) – The 1.5 μs one-shot multivibrator (E93) shown in zone C-6 serves two purposes. First, it checks whether a non-existent drive has been accessed. The one-shot is fired when DEMAND is asserted. When the drive responds with TRANS which generates RESP L, the one-shot is cleared. As previously described, RESP L either generates SET SSYN L or DESK DATA L, depending on the state of the DIR TRANS H signal. Either of these signals direct clears the 1.5 μs one-shot, causing a positive-going edge at the output. This edge tries to clock the NED flip-flop set, but the same signal that direct clears the 1.5 μs one-shot also direct clears the NED flip-flop. When the RH11 issues DEMAND and receives TRANS from the drive, the 1.5 μs one-shot is cleared. In addition, the NED flip-flop is inhibited from setting. If the drive did not respond, the SET SSYN L and DESK DATA L signals are both inhibited from clearing the one-shot, causing the one-shot to time out. At this time, the positive-going edge clocks the SSYN flip-flop set. The NED flip-flop also sets if the register being accessed is not the Attention Summary register.

NOTE

The DEV SEL H signal is applied to the direct clear input of the one-shot and NED flip-flops. If set, the flip-flops are cleared after the Unibus cycle is completed and the addressed register has been deselected.

A second function of the one-shot is to provide a 1.5 μs waiting period to allow the Attention Summary register in the various drives to be properly read from or written into. In this case, the one-shot times out because the RESP signal is inhibited and at the end of 1.5 μs, SSYN is set. NED is not set since the flip-flop is set only when a register other than the Attention Summary register has been addressed and no RESP is received.

DIS DEM disables the DEMAND signal from being asserted on the Massbus and is generated under the following conditions:

1. If the LOC/REM H signal is asserted indicating local mode, DIS DEM is generated to inhibit the Massbus handshake sequence.

2. DIS DEM is generated if the access is to the odd byte (ODD BYTE L) in the CS1 register (CS1 IN L). The CS1 register is shared by the RH11 and the drive with the odd byte being in the RH11 and the even byte being in the drive. ODD BYTE L and CS1 IN L generate DIS DEM to inhibit the Massbus handshake sequence in order to prevent altering the even (low) byte of the CS1 register located in the drive when the program is doing a byte operation to the odd (high) byte in the RH11. This is necessary because the Massbus cannot differentiate byte from word operations.

3. The STOP DEM L signal is asserted when the processor tries to load a function code specifying a data transfer operation into the drive while the RH11 is already busy executing a data transfer function with that drive or some other drive. For example, if unit 0 is doing a read data transfer and the processor tries to do a read or write data transfer in unit 1, the STOP DEM L signal from CSRB prevents the function code from being transferred to unit 1; otherwise, there would be the OR condition of data from unit 0 and unit 1 on the synchronous Massbus and the program could not distinguish unit 0 data from unit 1 data.

In addition, the DEMAND signal is inhibited when the LEG REG (legal register) signal from BCTA is not asserted. This prevents a SSYN response by the RH11 which indicates to the processor that the Unibus address was not recognized by the RH11.

5.3.4 Gating Address Onto Unibus

The remainder of the sheet shows the Unibus drivers which gate the contents of the Bus Address (BA) register and A16 and A17 of CS1 onto the Unibus address lines. This is accomplished when the RH11 is bus master and doing NPR cycles. Signal ADDR TO BUS H is used to gate the address; signal SEL BUSA H from the CSR module (sheet A) is asserted when the PSEL bit in the CS1 register is cleared. At this time, the RH11 is connected to Unibus A. During NPR operations, if PSEL is asserted, the RH11 is connected to Unibus B. The RH11 is always powered up in the condition where PSEL is cleared indicating the RH11 is connected to Unibus A.

5.3.5 Data Buffer Out Clock

The DB OCLK H signal is used to release data at the output of the Silo when the DB register is read by the program. The BCTA CO L signal is used to inhibit the assertion of DB OCLK during Unibus DATIP operations. This is necessary so that a read-modify-write instruction does not falsely remove data from the Silo. DB register selection is used for maintenance purposes when verifying the operation of the 66-word Silo Buffer register. Signal DB OCLK is asserted when the RH11 responds with SSYN to the register operation (if not a DATIP) and is released when the processor removes MSYN.

5.4 LOGIC DIAGRAM BCTC

This sheet contains the logic for the 16-bit Bus Address register and the 2 extension address bits located in the CS1 register. The register functions as an up-down counter and consists of four 74193 chips, providing outputs labeled BUSB A01 L through BUSB A15 L. The inputs to the chips come from the Unibus A data receivers, shown on sheet DBCF. The register is loaded when the BA IN L signal, REG STR H, and HI BYTE or LO BYTE signal is available, depending on whether the high byte or low byte is to be loaded. If the register is to be loaded as a word, both HI BYTE H and LO BYTE H signals are asserted.

A fifth chip processes bits 9 and 8 of CS1 which are extension bits of the Bus Address register. These bits are designated A16 and A17. The chip is loaded when CS1 IN L, REG STR H, and HI BYTE H are asserted. The RDY signal must also be asserted to load this chip in order to prevent bits A16 and A17 from being changed unless the RH11 is in the Ready state, since other commands can be passed through the dynamic CS1 register to drives not doing transfers.

The 74193 chip has a load input. When this input goes low, the data on the input lines is loaded into the register. The chip also has a CLR input which clears the register to all 0s when CLR H is asserted. The register functions as an up-down counter which counts on the positive-going trailing edge of the ADDR TO BUS H strobe. If CNT DW (1) H is asserted, the register counts down; if CNT DW (0) H is asserted, the register counts up.

5.4.1 Clocking Bus Address Register

The ADDR TO BUS H clock can be inhibited by setting the bus address increment inhibit bit (BAI bit 08) in the CS2 register. When the BAI bit is set, it prevents the bus address from changing during transfers, and the transfers will always occur from that same memory location. This feature might be used when refreshing a display. Normally, BAI (0) H is asserted at the input to AND gate E88 in zone A-7 to enable the ADDR TO BUS H strobe used to increment or decrement the Bus Address register.

5.4.2 Address Bit 00

Address bit 00 is not implemented making the bus address always even (word addressing): This results in only three bits being implemented in the low-order 74193 chip. Since the carry and borrow lines are based on four bits in the chip, two external gates are employed as decoders – AND gate E21 in zone B-6 to detect a carry condition (all 1s) and NOR gate E20 in zone C-6 to detect a borrow condition (all 0s).

5.4.3 Count Down (CNT DW) Flip-Flop

A CNT DW flip-flop is shown in zone A-4 of the diagram and is employed for future capability when reverse write-check and reverse read operations may be implemented. When a reverse function code is loaded (defined by a combination of GO CLR and data bits D01 and D02), the CNT DW flip-flop sets, and reverse write-check and reverse read operations can be implemented. This function is not used with the RS04/RS03 disk.

5.4.4 Bus Address Outputs

The bus address outputs from the RSBA Bus Address register are multiplexed with the outputs of the RSWC Word Count register on logic diagrams BCTD and BCTE for transfer to the Unibus data lines when the register is read by the program.

The BA register and address extension bits (A16 and A17) are also driven onto the selected Unibus (A or B) when the RH11 is performing NPR transfers. This selects the memory location to be accessed by the transfer. The Unibus A address drivers are located on sheet BCTB, while the Unibus B address drivers are located on sheet BCTC.

5.5 LOGIC DIAGRAM BCTD, BCTE

Logic diagram BCTE contains the upper eight bits of the Drive Word Count register, the upper eight bits of the Word Count register and two quad-input multiplexer chips (8234) used to select the word count or bus address when the program reads these registers. Logic diagram BCTD contains a similar arrangement for the lower eight bits of the Drive Word Count and Word Count registers and contains an additional two quad-input multiplexer chips for selecting the lower bits of the Bus Address or Word Count register.

5.5.1 Word Count Registers

The Drive Word Count (DRWC) register counts words transferred between the RH11 and the Massbus and is invisible to the program. This register detects when the RUN line should be unasserted on the Massbus. The Word Count (WC) register is a programmable register which counts words transferred between the RH11 and memory on the Unibus. Both registers are loaded in parallel with the 2's complement of the number of words to be transferred and are incremented toward 0 for each transfer.

The load input to both registers is the logical AND of WC IN H (Word Count register specified), REG STR H and HI BYTE H and LO BYTE H. The Drive Word Count register is incremented by DRIVE CLK H on sheet BCTD. This signal is a synchronous clock and occurs if there is no word count overflow or no error condition. The Word Count register is clocked by the INC WC L signal from sheet DBCB. The registers count on the trailing edge (positive-going) of the DRIVE CLK signal and INC WC signal. A carry out of one chip of the Word Count register is rippled to the count input of the next successive chip. When a carry occurs out of the chip with the most significant bits, word count overflow occurs. The Drive Word Count register is configured in the same manner and when the carry occurs out of the chip with the most significant bits, drive word count overflow occurs. Note the absence of a clear input to both registers. Since the registers are preloaded at the start of a data transfer, a clear is not necessary.

5.5.2 Word Count or Bus Address Selection

The output from the Word Count register is applied to 8234 multiplexer chips. These chips switch either the contents of the Word Count register or Bus Address register to the output. When the S0 input is low, the B inputs (B0, B1, B2, etc.) are switched to the F outputs (F0, F1, F2, etc.). This condition occurs when the Bus Address register is selected from the register select logic on sheet BCTA. When the S1 input is low, the A inputs (A0, A1, A2, etc.) are gated to the F outputs. This condition occurs when the Word Count register has been selected by the register select logic on sheet BCTA. Since S0 and S1 are supplied from a decoder, both cannot be low at the same time. If both inputs are high, the output is disabled and floats high unless asserted by another chip wired in parallel. The multiplexer is open-collector and can be bused together with other

multiplexers. The output feeds an internal bus (BUSI) which is used to sum up data from all the registers and prepares it for input to the Unibus drivers which drive Unibus A.

5.5.3 Clear Logic

Zones D-3 and D-2 on BCTD contains the logic for both Unibuses which determine when a Clear signal is generated. BUSA INIT L or BUSA DC LO L, when asserted, generates INIT + DC LO L. The BUSA INIT L signal initializes the RH11 and the drive. The BUSA DC LO L indicates no power on the Unibus. INIT + DC LO L creates MB INIT H (Massbus initialize) which initializes the registers in the drive. Thus, a no-power condition on the Unibus is implemented to initialize the Massbus.

The three signals that follow generate CLR + GO CLR H and CLR. GO CLR is used to clear the NPR logic, and CLR is used to clear the RH11 and the associated drives.

1. INIT + DC LO L – This signal is the OR of BUSA initialize and DC LO L.

2. GO CLR L – This signal is asserted when a data transfer command is loaded with the GO bit in the CS1 register.

3. PG CLR L – This signal is asserted by setting the CLR bit in bit 05 of the CS2 register, and is used to clear the RH11 and the drive registers.

CLRB H is similar to the CLR H signal and is generated as a result of BUSB INIT or BUSB DC LO L. This signal does not clear the RH11 registers as they are not connected to Unibus B.

If data transfers are being performed on Unibus B when CLRB is asserted, a DLT (data late error) is posted to terminate the transfers.

On sheet BCTE the CLR + GO CLR H signal resets the WC, DRWC OFLO, and DONE flip-flops.

5.5.4 Word Count Overflow

When the Word Count register overflows, the carry output goes low and is applied to the WC OFLO flip-flop as a clock. The positive-going trailing edge of this signal clocks the WC OFLO flip-flop set.

When the WC OFLO flip-flop is set and the last data transfer is completed (trailing edge of DATA REQ), flip-flop E74 is set, causing the DONE assertion which indicates the completion of the data transfer on the Unibus. If an error occurs (TRE asserted), then the DONE signal will be asserted at the end of the DATA REQ. The RH11 waits for the EOS (end of sector) before going to the Ready state. The DRWC OFLO flip-flop and Drive Word Count register function the same as the WC OFLO flip-flop and Word Count register. The carry output of the Drive Word Count register generates a LWRD H (last word) signal, indicating that the RH11 is not to anticipate receipt of another word. When the RH11 does a write data transfer, it normally makes sure that a word is available for transfer before the next SYNC CLK from the drive. When LWRD is generated, this operation is bypassed. LWRD is checked at the trailing edge of DRIVE CLK and will disable DLT (data late error).

5.6 LOGIC DIAGRAM BCTF

This diagram contains the interrupt control logic to prepare the Unibus to do an interrupt. The logic contained herein is similar to that on the M7821 Interrupt Control module which can be found in the *PDP-11 Peripherals and Interfacing Handbook.*

5.6.1 Interrupt Request

The interrupt control logic is initiated by INTR REQ H (interrupt request) and IE (1) H. The IE (Interrupt Enable) bit is set by the programmer by loading a 1 in bit 6 of the CS1 register. This allows interrupts to occur upon completion of an operation or upon detecting an error condition when INTR REQ H is asserted.

5.6.2 Bus Request

With the above conditions satisfied, BUSA BR L is asserted at the output of gate E65 in zone C-4. The other input to this gate is enabled because the SACK and BBSY flip-flops are reset. The BUSA BR L signal is applied to a priority jumper plug (zone D-6) configured at priority level 5. This causes BUSA BR5 L to be asserted at the output of the plug. The other BR outputs from the plug are unasserted at this time. BUSA BR5 L causes a bus request on the Unibus. When the processor is ready to allow the RH11 to become bus master, it returns BG IN H (bus grant) shown in zone C-8. This signal performs the following functions.

1. It is applied as a clock to the GRANT flip-flop. The positive-going edge tries to clock GRANT set. However, the set input to GRANT is disabled by BBSY being reset and IE (1) H and INTR REQ H being asserted. These conditions hold the input to NAND gate E47, pin 2 low, forcing the output high. The other input (pin 1) to the gate is from the BUSA NPR logic. With no NPR request, pin 1 is held high. AND gate E16 and inverter E64 which feed NAND gate

1. (Cont) are designed to improve the Unibus latency. The jumper at the input to gate E16, when cut, disables the circuit.

2. The BG IN H signal is used to direct clear the GRANT flip-flop when GRANT is negated. However, at this time, note that the GRANT flip-flop is still reset.

3. BG IN H also sets SACK 100 ns after the GRANT is received. The 100 ns delay is provided by the external components at the input to the 7408 AND gate in zone B-6. The delay provides the required time for the GRANT flip-flop to decide whether to block the grant or pass it on to the next device. Note that the set input to SACK is enabled as a result of the Bus Grant signal and because the GRANT flip-flop is still reset.

4. When the BG IN H signal is unasserted and SSYN IN H and BBSY IN H are unasserted indicating completion of the current cycle, BBSY is set. Note that the set input to BBSY is enabled since SACK is set.

Consequently, the interrupt control logic is initiated, a bus request is sent to the processor, a bus grant is returned from the processor, and the SACK flip-flop is set after a 100 ns delay. When the SACK flip-flop sets, the BUSA BR5 L signal goes unasserted and when the processor completes its current cycle, BBSY is set indicating that the RH11 has control of the bus. When BBSY sets, the set input to the GRANT flip-flop is enabled and the GRANT flip-flop will be set by the next BG IN H signal. The grant will be passed to the next device on the bus. In addition, setting BBSY causes the SACK flip-flop to clear, and also generates INTR MASTER L. This signal causes the BUSA INTR L signal on Unibus A to be generated and also gates the 7-bit interrupt vector to the Unibus. The vector is jumper selectable. If the jumper is left in, the corresponding bit is a 1; if the jumper is cut, the corresponding bit is a 0.

5.6.3 Interrupt Done

When the processor has accepted the interrupt vector, it returns SSYN IN H which generates INTR DONE H. This signal clears the latch in zone C-7 which allows the interrupt sequence to terminate. Also, INTR DONE H clears BBSY to allow another device to gain control of the bus.

5.7 LOGIC DIAGRAM BCTH

This diagram contains the NPR control logic necessary to initiate NPR requests and to gain control of the Unibus in order to do NPR cycles. The logic on this sheet is similar to the logic contained on the M7821 Interrupt Control module described in the *PDP-11 Peripherals and Interfacing Handbook.*

5.7.1 NPR Arbitration

The logic is initiated by DATA REQ H being asserted at the input to AND gate E15 (zone D-5). This signal is held asserted during the entire cycle for single cycle NPRs or is held asserted for both cycles when performing back-to-back NPR cycles. The other input to the AND gate is CLR DREQ L, which is normally held high during the cycle and enables the gate. The output of this AND gate qualifies AND gate E25 (zone B-3). The other two inputs to this gate are enabled by the SACK and BBSY flip-flops being reset. The output of AND gate E25, pin 12 is supplied to two gates (E33), (zone D-2) to raise an NPR request on the Unibus which has been selected. This sheet will be described assuming that Unibus A has been selected. In this event, the BUSA NPR L signal is asserted on the Unibus. The processor arbitrates the NPR requests and returns a BUSA NPG IN H signal when it wishes to to grant the bus to the RH11. The BUSA NPG IN H signal clocks the GRANT A flip-flop, but the flip-flop does not set since the three inputs to gate E7 (zone D-3) are high causing the D-input to the flip-flop to remain low. Consequently, the GRANT signal is blocked and is not passed to the other devices. The BUSA NPG IN H signal is also applied to multiplexer E26. Since Unibus A has been selected, the multiplexer inputs at pins A3 through A0 are present at the output. If Unibus B is selected, the inputs at pins B3 through B0 are present at the output. The BUSA NPG IN H signal clocks the SACK flip-flop after 100 ns. Since GRANT L is not asserted, the other input (pin 11) to E7 is high and provides a low input to the SACK flip-flop causing it to set. The 100 ns delay network consisting of the resistor and capacitor network at the input to AND gate E15 (zone C-5) ensures that the SACK flip-flop will not be prematurely set until the GRANT signal has been blocked. Setting the SACK flip-flop causes the BUSA SACK L signal to be asserted on the Unibus and also causes the RH11 to drop the BUSA NPR L signal. This acknowledges the fact that the RH11 has received the BUSA NPG IN H signal from the processor. SACK prevents the processor from further arbitrating NPRs.

5.7.2 Acquiring Bus Mastership

Multiplexer E26 monitors BBSY and SSYN for the selected Unibus (BUSA, in this case). When both BBSY and SSYN from the device currently acting as bus master are unasserted, NOR gate E32 (zone B-6) is qualified. This enables AND gate E15 (zone B-5). The other input to this gate qualifies the gate when the processor drops BUSA NPG IN H. The output of this gate clocks the BBSY flip-flop set since SACK is still asserted. When BBSY sets, it asserts BUSA BBSY L via gate E40 (zone B-2) and also asserts NPC MASTER L, indicating that the RH11 is now bus master. This initiates the sequencing logic for an NPR cycle (see sheet DBCA). The 0 output of the BBSY flip-flop disqualifies AND gate E25 (zone B-3) which keeps the BUSA NPR L signal unasserted. Also, when SACK ENB H and BBSY (1) H are asserted, the SACK flip-flop is cleared.

If a device on Unibus B desires to become bus master prior to the RH11 acquiring bus mastership, the logic in the RH11 must pass the grant to the next device. The BUSB NPG IN H signal clocks the GRANT B flip-flop set. Since the SEL BUSB H signal is unasserted, the D-input to the flip-flop is high and the flip-flop is set allowing the GRANT signal to be passed to the next device. When the BUSB NPG IN H signal is dropped by the processor, the clear input of the GRANT B flip-flop is brought low, thus removing the BUS NPG OUT signal to the next device.

5.7.3 Completion of NPR Cycle

The NPR cycle(s) is completed when CLR DREQ L is asserted, causing AND gate E15 (zone D-5) to go low. This action causes the NPR cycle to end and BBSY flip-flop to reset, releasing the bus to the next device.

5.8 LOGIC DIAGRAM BCTJ

This diagram contains the MB INIT logic, the logic used to gate out the high byte of the CS1 or the CS2 registers, and the logic to set the (Missed Transfer Error) MXF flip-flop.

5.8.1 MB INIT Signal

When an initialize (INIT) signal or a power fail condition (DC LO L) occurs on Unibus A, a MB INIT H (Massbus initialize signal) is generated and initializes all the drives. Both INIT and DC LO are guaranteed to be a minimum of 400 ns, and the assertion of either signal qualifies gate E87 (zone D-4) to produce MB INIT H.

Signal MB INIT H is also generated if the CLR bit in CS2 is set by the program. This causes a PG CLR L signal to be generated which fires 400 ns one-shot multivibrator E85 (zone D-6). The output of the one-shot is a 400 ns negative pulse which is used to enable the other input to gate E87 in zone D-4.

5.8.2 Gating High Byte of CS1/CS2

The two 2-to-1 multiplexers (E59 and E60) in the center of sheet BCTJ are used to gate out the high byte of the CS1 or CS2 register. CS1 OUT L, when asserted, gates the high byte of the CS1 register through the multiplexer and CS2 OUT L, when asserted, gates the high byte of the CS2 register through the multiplexer. The output of the multiplexer is the internal data bus (BUSI) which feeds Unibus A.

5.8.3 MXF Error Flip-Flop

The lower portion of sheet BCTJ shows the SET MXF and MXF flip-flops and a 250 ms one-shot. When the RH11 goes into the busy state (RDY H not asserted), the 250 ms one-shot (E85 in zone B-7) fires indicating that the RH11 is attached to the synchronous bus. The 250 ms one-shot is retriggered on every SYNC CLK signal from the drive. If the RH11 is busy, and a SYNC CLK pulse does not occur within 250 ms, the trailing edge of the 250 ms pulse clocks SET MXF flip-flop E86 (zone B-5) set which, in turn, causes MXF flip-flop E86 (zone B-3) to be direct set. Normally, the D-input to the SET MXF flip-flop is at ground which allows the flip-flop to set. If jumper W19 is cut, however, the high input applied to the D-input prevents the flip-flop from setting. This jumper is used for maintenance purposes. The MXF flip-flop can be set under program control by setting bit 9 (MXF error) of the CS2 register and by generating the appropriate gating signals (HI BYTE H, REG STR H, and CS2 IN L).

The 250 ms one-shot and the SET MXF flip-flop are direct cleared by the CLR H signal, the BUSY flip-flop being in the Reset state, or the OCC (occupied) line on the Massbus being asserted. The MXF flip-flop is direct cleared by the CLR ERR L signal.

5.8.4 AC LO and DC LO

Power supply signals AC LO and DC LO are actively pulled up so that they may be used as inputs to the two M688 Power Fail Driver modules.

5.9 BCTK LOGIC DIAGRAM

The BCTK print provides the truth table for the register selection ROM shown on sheet BCTA.

5.10 LOGIC DIAGRAM CSRA

This logic diagram contains the data transfer command logic, the RUN flip-flop, the BUSY flip-flop, the PSEL (port select) flip-flop, the CS1 clocking logic, and the interrupt request logic.

5.10.1 Data Transfer Command Logic

The data transfer command logic consists of the Write, Read, and Write-Check flip-flops (E3 pin 6, E15 pin 6, and E15 pin 8, respectively). These flip-flops decode the Write, Read, or Write-check commands that are being passed through the controller into the drive. The commands are decoded in the RH11 to let the RH11 know what type of operation is to be implemented. In addition, these commands are also supplied to the drive where they are again decoded in the drive's function register. All other commands are not decoded in the RH11 but are merely decoded in the drive.

The D-input to the Write flip-flop represents the range of function codes that define the Write command. These codes range from 60 through 67. The D-input to the Read flip-flop represents the range of function codes that define a Read command. These codes range from 70 to 77. The D-input to the Write-check flip-flop represents the function codes that define a Write-check command. These codes range from 50 to 57. For example, the D-input to the Write flip-flop is enabled when D03 IN L is unasserted and D04 IN H and D05 IN H is asserted in gate E6 pin 12. This bit pattern corresponds to the digit 6, specifying function codes from 60 through 67. The other flip-flops are decoded in like manner.

The C-input to the flip-flop accepts the positive-going trailing edge of the GO CLR L signal to clock the flip-flop specified by the appropriate data bits which comprise the function code. Signal GO CLR L is used to initialize the Silo and NPR logic for a data transfer, and is also used to direct set the BUSY flip-flop in zone B-6, indicating a data transfer command is in progress. Signal GO CLR L is asserted at the output of NAND gate E17, pin 6 if CLK CS1 LO H, D00 IN H, and a data transfer command (Write, Read, or Write-check) has been decoded by NAND gates E6 pin 12, E14 pin 12, or E14 pin 6. Signal CLK CS1 LO H is asserted when the program is loading data into the low byte of the CS1 register, and D00 IN H is asserted when the GO bit is set by the program. As previously mentioned, the write block code is 60 through 67. Since D00 IN H is asserted to generate GO CLR L which, in turn, is used to clock the data transfer flip-flops, the function code for each data transfer command consists of only the odd function codes within the group. For example, the write function codes are 61, 63, 65 and 67. The even codes do not start a data transfer function since the GO bit (D00 IN H) must be asserted.

The outputs of the data transfer flip-flops are applied to various gates to generate signals for internal use. Gate E20, pin 4 generates the Ready signal when there is no Read, Write or Write-check command being processed, meaning that the RH11 is capable of accepting a data transfer command. This fact is reflected in bit 7 (RDY) of the CS1 register. NAND gate E1, pin 11 generates WRITE L after the function command has been loaded in the drive. This is done for the following reason: When the Write command is asserted, a DATA REQ signal is initiated, causing a memory access on the Unibus. To prevent this access from occurring when the RH11 is trying to access a non-existent drive, the WRITE flip-flop is ANDed with FCTN LOAD (1) L. Signal FCTN LOAD (1) L inhibits the Write command from initiating a memory access until the command has been loaded into the drive. In this way, the memory cycle is not performed for a non-existent drive. Should a non-existent drive be accessed, an NED (non-existent drive) error is raised which disables the DATA REQ signal from initiating an NPR cycle. Inverter E13, pin 10 merely provides a buffered output of the Read signal. Gate E5, pin 3 ORs the output of the Read and Write-check flip-flops to create the Read or Write-check signal. Inverter E13, pin 12 buffers the Write-check signal from the WR CHECK flip-flop. When the data transfer is complete for a particular operation, the appropriate data transfer flip-flop is cleared by gate E8, pin 3. This gate is asserted by BUSY (0) H and DEV SEL L not asserted or by CLR L being asserted. BUSY (0) H is asserted when the BUSY flip-flop is cleared, indicating that the RH11 is no longer busy. This flip-flop is described in subsequent paragraphs. The DEV SEL L signal is asserted when the program is reading or writing a register and prevents the program from looking at the ready bit during the time the bit might be changing. When the data transfer flip-flops are cleared, the RH11 goes to the RDY state.

5.10.2 RUN Flip-Flop

In a write operation, the RH11 transfers the Write command to the function register in the drive and then turns the drive on by setting the RUN flip-flop which asserts the RUN signal. The drive seeks the address specified by the program and starts accepting data words as a result of the SYNC CLK signals. Before the RUN signal is asserted, however, the RH11 prefills the Silo with data words so that data is available to the drive immediately. This logic is implemented by NAND gate E19, pin 6 which is enabled by WRITE H, START H, and OBUF FULL (1) H. The START H signal is asserted when the number of words specified by the start counter have been loaded in the Silo. If only one or just a few words are to be transferred, the RH11 ensures that a word is in OBUF as a result of OBUF FULL (1) H. In this case, the START H signal is asserted as a result of WC OFLO (1) H and not due to the start counter indication of words loaded in the Silo. Note that it takes from 0 to 32 μs for a word to propagate from the bottom cell of the Silo to the top cell with a typical time of 16 μs. Because of this time delay, the logic is designed to ensure that a word is in OBUF before the RH11 turns on the drive. The TRE (1) L input to gate E19, pin 8, if asserted, also sets the RUN flip-flop. This is necessary because the data transfer command has already been loaded for writes when errors occur before the signal START in the RH11 is asserted, and the only way to terminate the operation is to set the RUN flip-flop and wait for the end of the first block or sector (designated by EBL). At this time, the error condition clears the RUN signal. On the trailing-edge of the EBL (end-of-block) signal, the drive looks at the cleared RUN signal and terminates its operations.

In the case of a read or write-check operation, it is desired to set the RUN signal immediately in order that the drive can start filling up the Silo. This is accomplished by gate E19, pin 8.

The RUN line, when cleared, disconnects the RH11 from the drive. This line is cleared under the following conditions:

1. When drive word count overflow [DRWC OFLO (1) L] is asserted. This occurs when the desired number of words have been transferred.

2. If an error exists in the RH11 and the drive has asserted a SYNC CLOCK (SCLK). The logic is implemented by inverter gate E9, pin 6, which is enabled when an error occurs. In this situation, the RUN flip-flop is direct cleared and the drive looks at the RUN line on the trailing edge of EBL. If RUN is cleared or unasserted, the transfer is terminated. If RUN is asserted, the drive does the transfer for the next sector.

3. If an exception (EXCP L) occurs (see gate E27, pin 8). When the drive has an error, it raises the EXCP line which clears RUN upon receipt of the EBL signal. This indicates the end of the current sector. An exception is caused by any of the error conditions defined in the ER register.

4. If a data transfer command is to be loaded into a non-existent drive. This condition is implemented by FCTN LOAD (1) H and NED H via NAND gate E9, pin 3.

5. If a clear (CLR L) or missed transfer signal [MXF (1) L] occurs.

NOTE

The conditions described in 1, 2, 3 to clear the RUN flip-flop are synchronized to the drive. The conditions described in 4 and 5 are not synchronized to the drive since there is no guarantee that a valid drive has been accessed or that the drive will respond.

5.10.3 BUSY Flip-Flop

The BUSY flip-flop is set during a data transfer command and remains set until reset by one of the following situations:

1. When the RH11 is doing a data transfer command, the BUSY flip-flop cannot be cleared and the operation cannot be terminated until both the Unibus and Massbus cycles have been completed. This is indicated by DONE (1) and EOS (1) applied to NAND gate E1. When both signals are asserted, the BUSY flip-flop is cleared via gate E8, pin 8.

2. The CLR or MXF (1) signals which clear RUN are also used to clear BUSY.

3. The BUSY flip-flop can be clocked clear by a data transfer command being loaded into a non-existent drive. This is accomplished by NAND gate E9, pin 3, which is qualified by FCTN LOAD (1) H and NED H.

5.10.4 Port Select Flip-Flop

The Port Select (PSEL) flip-flop in zone B-6 is a programmable bit which selects Unibus A or Unibus B. If the flip-flop is set, Unibus B is selected; if the flip-flop is cleared, Unibus A is selected. The output of the PSEL flip-flop feeds driver E5, pin 6 which generates the SEL BUSA H signal used to control the data path for the Unibus.

A second input to E5, pin 6 is a jumper which overrides the PSEL bit. PSEL is set or cleared via CS1 IN H, REG STR H and HI BYTE H only when the RH11 is in the Ready state. This prevents changing of the data path during a data transfer. These signals are asserted when the program is loading the upper byte of the CS1 register. With these conditions asserted and the RH11 in the Ready state, AND gate E11, pin 3 is qualified and clocks the PSEL flip-flop set if D10 IN H is asserted.

5.10.5 CS1 Clocking Logic

The CLK CS1 HI H and CLK CS1 LO H signals are generated by AND gates E23, pin 6 and E23, pin 8, respectively. These signals are clocking signals for the high byte and the low byte of the CS1 register. Signals HI BYTE H, REG STR H, and CS1 H create CLK CS1 HI H. Signals LO BYTE H, REG STR H, and CS1 H create CLK CS1 LO H.

5.10.6 Interrupt Requests

Interrupt requests are allowed to occur if the interrupt facility is enabled. The facility is enabled by the program loading a 1 in bit position 6 (interrupt enable bit) of the CS1 register. This sets the IE (Interrupt Enable) flip-flop and generates IE (1) H. If an interrupt occurs (with the interrupt enable set), the IE bit is cleared by INTR DONE H which occurs when the processor has been interrupted, has acknowledged the interrupt, and is preparing to execute the interrupt service routine. Signal INTR DONE H is generated on sheet BCTF and clears the IE bit to prevent interrupts from occurring while the service routine is being executed. The IE bit can also be cleared by CLR L which may occur during a Unibus initialize sequence, a power fail assertion, or by setting program clear bit 5 on the CS2 register.

The interrupt facility is enabled by the IE bit. However, the interrupt occurs as a result of the INTR REQ signal being asserted. Interrupts can occur as a result of one of the following conditions:

1. If SC (special condition) and RDY H are asserted, the INTR REQ H signal is generated to initiate an interrupt. SC occurs as a result of TRE, an ATTN signal from the drive, or MCPE (Massbus Control Parity Error). The RDY H signal ensures that the RH11 is in the Ready state before it initiates an interrupt. For example, if a drive asserts ATTN while the RH11 is busy doing a data transfer with another drive, the interrupt would not be allowed to occur until the RH11 has completed the current data transfer and returned to the Ready state.

2. If the IE bit is set and the RH11 changes from the Busy to the Ready state, the INTR flip-flop sets and generates INTR REQ H, indicating completion of the data transfer and initiating the interrupt.

3. The program can force an interrupt by loading bits D06 H (IE) and D07 H (RDY) in the CS1 register which direct sets the INTR flip-flop.

5.11 LOGIC DIAGRAM CSRB

This diagram contains the logic associated with some of the error conditions and status indicators.

5.11.1 CS2 Clocking Signals

The program loads data into the CS2 register by the CLK CS2 HI H and CLK CS2 LO H signals. CLK CS2 HI H causes the program to load data into the high byte of the CS2 register, and CLK CS2 LO H causes the program to load data into the low byte of the register. REG STR H and CS2 IN H are enable signals to AND gates E27, pin 6 and E27, pin 12. Signal CLK CS2 HI H is qualified by the HI BYTE H signal, and CLK CS2 LO H is qualified by the LO BYTE H signal.

5.11.2 Program Clear Bit

The program clear bit (PG CLR L) is set when the program loads a 1 in bit 5 of the CS2 register and CLK CS2 LO H is asserted, indicating that the program is loading the low byte of the CS2 register. PG CLR L is an input which generates the CLR portion (see sheet BCTD) of the CLR + GO CLR L signal and also generates MB INIT (see BCTJ). The CLR signal initializes the RH11 and MB INIT initializes the drive.

5.11.3 Bus Address Increment Inhibit

The Bus Address Increment Inhibit (BAI) flip-flop, when set, prevents the Bus Address register on the BCT module from incrementing when doing NPR cycles. Consequently, all memory references are made to or from the same memory location. This feature is useful when refreshing a display from a disk, for example. The BAI bit can only be

changed if the RH11 is in the Ready state. The CLK CS2 LO H and RDY H are ANDed to clock the BAI flip-flop which represents bit 3 of the CS2 register.

5.11.4 Unit Select Number

The unit numbers are unit 0 through 2 of the CS2 register and are designated U00 through U02 H. These three bits are loaded by the program and used on the Massbus to select one of eight drives, and are generated by data bits D02 IN H through D00 IN H which are applied to three of four flip-flops contained on IC E21.

5.11.5 Parity Test Mode

A parity test mode is provided for maintenance purposes. This is implemented as PAT (bit 4 of the CS2 REG) and may be set or cleared by the program. When set, the parity logic associated with the Massbus in the RH11 is switched from odd parity to even parity generation.

5.11.6 Function Load

The use of the Function Load flip-flop is described on logic diagram CSRA. The flip-flop is set when a data transfer command (Read, Write or Write-check) is being loaded in the CS1 register. The C-input to the flip-flop is clocked by GO CLR L which is asserted when a data transfer command is specified, the clocking signal for the CS1 is asserted, and the GO bit is set. The flip-flop remains set until the bus cycle being used to load that command is completed. At this time, the master drops MSYN and the DEV SEL L signal goes unasserted to clear the Function Load flip-flop. The Function Load signal is used to delay the Write signal from being asserted until the function has been loaded in the drive (see sheet CSRA), and is also used to clear the RUN flip-flop when a function command is being loaded into a non-existent disk (see sheet CSRA).

5.11.7 Non-Existent Device

The Non-Existent Device (NED) error is generated at the output of a latch circuit consisting of gates E9, pin 8 and E9, pin 11. Signal NED H is asserted when SET NED L is asserted, and SET NED L is asserted 1.5 μs after DEMAND is asserted on the Massbus and no transfer response occurred. Thus, if no response was received from a drive 1.5 μs after the assertion of DEMAND and the register being addressed was not the Attention Summary register, then a non-existent device has been addressed. Signal NED H is cleared by CLR ERR L. This CLR ERR L signal clears all the error conditions, and is generated by CLR + GO CLR L. Signal CLR occurs as a result of power fail, Unibus initialize, or program clear. Signal GO CLR L is asserted by setting the GO bit during a data transfer command.

The errors are also cleared by loading a 1 in the TRE bit position in bit 14 of the CS1 register. This is accomplished by NAND gate E2, pin 3 in zone B-7. Consequently, loading a 1 in the TRE bit position clears out any error in the RH11. This is done so the error conditions in the RH11 can be cleared without having to clear the error conditions in the drive.

5.11.8 Transfer Error

The TRE (transfer error) flip-flop (zone B-6) is a summation of all the error conditions in the controller and the drive. These include Data Late Error (DLT), Massbus Data Parity Error (SYNC PE), Exception (summation of all error conditions in the ER register), Write-Check Error (WCE), Unibus Parity Error (UPE), Non-Existent Device (NED), Non-Existent Memory (NEM), Program Error (PGE), and Missed Transfer Error (MXF). Any one of these conditions enables gate E22, pin 8 and clocks the TRE flip-flop set. TRE is bit 14 of the CS1 register. TRE (0) H is ORed with ATTN and CNTL PE (MCPE) to create SC H, which is bit 15 of the CS1 register. Bits 14 and 15 are coded to inform the programmer of the type of error and where it occurred. Whenever the SC bit is set, this indicates that an error has occurred from some drive doing a data transfer command or that a drive has finished some movement command such as a Seek. By then examining the TRE bit, the programmer can determine additional information. If TRE is set, this indicates that a data transfer error has occurred. If TRE is not set, this indicates that:

1. an error has occurred in some drive not doing a data transfer command,
2. the drive has completed some operation which is not a data transfer command, or
3. a Massbus Control Parity Error was detected when the program read information from a drive register.

The programmer can then ascertain which drive has caused the SC H signal by referring to the Attention Summary register which shows the ATTN condition of each drive or if MCPE occurred (bit 13 of CS1). ATTN is raised by a drive when an error occurs or when it has finished some operation other than a data transfer command such as a Block Search. Completion of data transfer commands are indicated to the programmer by the condition of the RDY bit.

5.11.9 Program Error Flip-Flop

The Program Error (PGE) flip-flop in zone C-5 is set when the programmer tries to load a data transfer command while the RH11 is in process of doing a data transfer. Signal GO H is asserted indicating that a data transfer command is being loaded; if the RH11 is busy, RDY H is low which causes the PGE flip-flop to set creating PGE (1) H. This signal is applied to NAND gate E6, pin 6 and generates a STOP DEM L signal which is applied to the BCT module and prevents the DEMAND signal from going out on the Massbus and actually loading the data transfer command into a drive. The PGE (1) H signal also creates the TRE condition (zone B-6). The PGE flip-flop is direct cleared by CLR L or CLR TRE L.

5.11.10 End of Sector (EOS) Flip-Flop

An EBL pulse occurs at the end of every sector. The drive monitors the RUN line from the RH11 at the trailing edge of every EBL. If RUN is asserted, the drive continues to do another sector. If RUN is not asserted, this is the last sector and the drive stops since the data transfer is completed.

The RH11 also must monitor the RUN line in order to know when the drive has reached the end of the last sector. Otherwise, the RH11 might return to the Ready state before the drive has completed the operation. The EOS flip-flop in the RH11 monitors the RUN line at the trailing edge of EBL. Signal EOS (0) H prevents the BUSY flip-flop (sheet CSRA) from clearing. When the end of the last sector is reached at the trailing edge of EBL, the EOS flip-flop is set, thus allowing the BUSY flip-flop to clear and permitting the RH11 to return to the Ready state as long as the last word on the Unibus has been transferred (DONE is asserted). Remember that the Unibus transfer as well as the Massbus transfer must be complete to return the RH11 to the Ready state.

5.11.11 Unibus Parity Error (UPE) Flip-Flop

The Unibus Parity Error (UPE) flip-flop is direct set by a parity error on the Unibus as defined by the states of the PA (D16) and PB (D17) bits (see sheet DBCH). The UPE flip-flop can be set by the programmer by writing a 1 in bit position 13 of the CS2 and clocking the UPE flip-flop with CLK CS2 HI H which clocks the high byte of the CS2 register. Signal UPE (1) H causes TRE and the programmer can ensure proper operation of the UPE flip-flop by writing a 1 in bit 13 and checking to see if TRE occurs.

5.12 LOGIC DIAGRAM DBCA

This diagram contains the logic necessary to transfer data between the RH11 and memory over the PDP-11 Unibus. When the RH11 asserts a DATA REQ, the following events occur:

1. The RH11 asserts an NPR request (see sheet BCTH).
2. The processor arbitrates the NPR requests and issues NPG to the RH11. This indicates that the RH11 is the next device to become bus master.
3. The RH11 acknowledges receipt of the grant by issuing SACK (selection acknowledge), which drops the NPG signal.
4. The RH11 waits for BBSY and SSYN to clear, indicating that the device currently using the Unibus has finished its cycle.
5. When BBSY and SSYN clear, the RH11 asserts BBSY and NPC MASTER.
6. The RH11 places address and control information on the Unibus (and data if a Read command is specified).
7. After 200 ns, the RH11 issues MSYN since it is now bus master.
8. If a Read command is specified, the slave device returns SSYN upon receipt of the data. If a Write or Write-check command is specified, the data from the slave is deskewed 125 ns after SSYN is returned before it is used in the RH11.
9. MSYN is cleared which, in turn, causes the slave device to clear SSYN. If a single NPR cycle is being performed, BBSY is cleared 100 ns after MSYN is cleared. If a back-to-back NPR cycle is being performed, BBSY is cleared 75 ns after MSYN clears on the second cycle.
10. When BBSY is cleared, the NPR cycle is finished until a new DATA REQ is issued to initiate the next cycle.

The logic to accomplish the above events is contained on sheets BCTH (previously described) and DBCA. The following description covers sheet DBCA.

5.12.1 NPC MASTER Signal

When NPC MASTER is asserted, ADDR TO BUS H is asserted. In addition, the NPC MASTER signal enables gates E84 and E96 (zone D-6). When a Read command is specified, these gates are qualified to yield both polarities of the DATA TO BUS signal used to gate data onto the Unibus. The gates are connected in parallel to avoid the delay normally required in going through an inverter.

5.12.2 ADDR TO BUS Signal

The ADDR TO BUS signal, generated at the output of E89, pin 10, accomplishes the following functions:

1. ADDR TO BUS triggers one-shot multivibrator E92 (zone C-5). In the first memory cycle, END CYCLE (1) H is unasserted, thus enabling gate E89. The assertion of ADDR TO BUS triggers the one-shot (the function of the one-shot is described in subsequent paragraphs). At the end of the first memory cycle, END CYCLE (1) H is asserted disqualifying E89. When END CYCLE (1) H goes low, it produces a positive-going pulse at E89, pin 10 which triggers the one-shot for the second memory cycle. Consequently, the one-shot is triggered by NPC MASTER in the first memory cycle and by the assertion and subsequent unassertion of END CYCLE (1) H in the second memory cycle.

2. ADDR TO BUS H is the enable signal which gates the address onto the selected Unibus. The leading edge of END CYCLE (1) H causes the trailing edge of ADDR TO BUS H which increments the Bus Address register. During the width of the END CYCLE pulse, the address in the address register is stabilized. At the trailing edge of END CYCLE, one-shot E92 is again triggered.

3. ADDR TO BUS is also applied to gate E89 and gate E90 (zone D-2). The other input to those gates is SEL BUSA, which selects the appropriate Unibus. If SEL BUSA is asserted, Unibus A is selected; otherwise Unibus B is selected. E89 and E90 enable the drivers shown in zone C1 and D1 to generate MSYN and C1 signals for the appropriate Unibus (BUSA or BUSB). MSYN is asserted by ADDR TO BUS H when the MSYN flip-flop is set. The setting of this flip-flop is described in the paragraph entitled MSYN Deskew. C1 is asserted low by ADDR TO BUS H when a Read command is specified. This designates a DATO operation (data written into memory). If C1 is unasserted (no Read command specified), a DATI operation is performed.

NOTE

The C0 control line specifies a DATOB or DATIP operation. Since the RH11 does neither operation, the C0 line is not required and remains unasserted.

5.12.3 MSYN DESKEW

The ADDR TO BUS H signal triggers one-shot multivibrator E92 as previously mentioned. This one-shot provides a 200 ns deskew for MSYN to allow the address and control lines time to stabilize on the Unibus.

NOTE

Gate E90 (zone C-6) is used during a Read command to lock the Silo timing to the Unibus timing and ensures that data will be deskewed for the proper interval before MSYN is set on the second cycle of back-to-back NPR sequences.

The positive-going trailing edge of the 200 ns pulse from pin 4 of E92 clocks DESK COMPL flip-flop E93 (zone C-4), indicating that the deskew is completed. This enables one input to gate E69 (zone C-3). The other inputs to this gate represent inhibit conditions to prevent MSYN flip-flop E93 (zone C-3) from setting. These inhibit conditions are described in the paragraph entitled MSYN Inhibit Conditions. If none of the inhibit conditions are present, and the Silo and Unibus signals are in the proper state, MSYN is set, and is ANDed with the appropriate Unibus select signal (zone D-1) to generate BUSA MSYN L or BUSB MSYN L.

5.12.4 MSYN Inhibit Conditions

In the second cycle of back-to-back NPRs or in BUS HOG mode (described in subsequent paragraphs), there are several conditions used to inhibit MSYN. These conditions are ORed in gate E69 (zone C-3). The purpose of these inhibits is to lock the data transfer rate to the Silo data rate. The inhibit conditions are listed below:

1. The RH11 cannot assert MSYN for the current cycle until NPC SSYN from the previous cycle has been cleared.

2. In a write function, the RH11 does not assert MSYN until it is certain that IBUF is empty and available to receive the data from the Unibus. If IBUF is full, E69 gate is disabled and inhibits MSYN until IBUF is cleared.

3. In a write-check function, the RH11 does not fetch a word from memory until it is sure that the word from the drive is in OBUF. When OBUF is not full, OBUF FULL (0) H is asserted which disqualifies gate E69 and prevents MSYN from setting until OBUF is full.

4. The fourth inhibit condition occurs during a Read command when the RH11 is doing the second NPR cycle of back-to-back NPRs or is in BUS HOG mode. In this instance, the RH11 does not initiate MSYN deskew until it is assured that a data word is available in OBUF. At this time, then, the data and address can be deskewed from MSYN to allow time for the data and address to stabilize on the Unibus. This inhibit condition is implemented in AND gate E90 (zone C-6). If OBUF is full, OBUF FULL (0) H goes low and allows 200 ns one-shot E92 to be triggered. If OBUF is not full, this gate inhibits the one-shot from firing.

5.12.5 MSYN Timeout

The MSYN (1) H signal is applied to NEM flip-flop E85 (zone B-6) and to 10 μs one-shot multivibrator E83 (zone B-6). The 10 μs one-shot measures the time it takes for SSYN to respond. If SSYN does not respond within 10 μs, the positive-going trailing edge at pin 4 of E83 clocks the NEM flip-flop set, denoting a non-existent memory. This sets bit 11 in the CS2 register to flag the programmer and also raises the TRE bit in the CS1 register. If SSYN does respond within 10 μs after MSYN is issued, it direct clears the 10 μs one-shot and the NEM flip-flop via gate E80, pin 3. The CLR ERR signal is used by the programmer to clear the NEM flip-flop after it has been set by the timeout circuitry.

5.12.6 DATA WAIT and MSYN WAIT One-Shot Multivibrators

The DATA WAIT one-shot is shown in zone B-5, and the MSYN WAIT one-shot is shown in zone B-3. The DATA WAIT one-shot is used during a Write or Write-Check command (READ L unasserted) and provides a 125 ns pulse to deskew the data from SSYN. Of the 125 ns, 75 ns are in accordance with Unibus specifications and 50 ns is the propagation time for the data to be supplied to IBUF from the Unibus in a write cycle. In a write-check cycle, it provides the propagation time for this data to be compared with the device data in OBUF. The DATA WAIT one-shot is triggered by NPC SSYN, or in its absence, a non-existent memory error when the RH11 is bus master (NPC MASTER H asserted), MSYN has been issued, and a write or write-check operation has been designated. The negative-going trailing edge of the DATA WAIT one-shot triggers the MSYN WAIT one-shot which initiates a 75 ns pulse. At the end of 75 ns, the positive-going output from E95, pin 4 triggers 200 ns END CYCLE one-shot (zone B-2). END CYCLE (1) H inhibits the ADDR TO BUS signal and retriggers the NPR control logic if a second cycle is to be performed or clears BBSY if it is the last cycle of the NPR sequence. During the 75 ns interval between the firing of MSYN WAIT and the firing of the END CYCLE one-shot, the RH11 has cleared MSYN and must hold the address and BBSY asserted.

The MSYN WAIT one-shot accomplishes the following functions:

1. Clears the MSYN flip-flop via OR gate E80 (zone C-3).

2. Is fed to CYCLE COUNT flip-flop E85 (zone B-3) and NEXT CYCLE flip-flop E36 (zone B-2). The CYCLE COUNT flip-flop determines whether the cycle is the first or second cycle of back-to-back NPRs. The NEXT CYCLE flip-flop determines whether a second memory cycle is to be performed in the NPR sequence.

3. Generates DATA STR H which is used to clock data into IBUF or to change data in OBUF.

If a Read command is specified (writing a data word into memory), the data does not have to be deskewed when NPC SSYN is received. However, MSYN must be cleared. Prior to the receipt of NPC SSYN, all inputs to NAND gate E94 (zone B-4) are high, forcing the output low. Upon receipt of NPC SSYN, pin 9 of E94 is driven low, forcing the output high. The positive-going output triggers the MSYN WAIT one-shot which clears MSYN. Consequently, in the case of a Write or Write-check command, both the DATA WAIT and MSYN WAIT one-shots are fired. In the case of a Read command, the data does not need to be deskewed and the DATA WAIT one-shot is bypassed.

5.12.7 CYCLE COUNT and NEXT CYCLE Flip-Flops

The CYCLE COUNT flip-flop is shown in zone B-4 and determines whether the RH11 is doing the first or second cycle of back-to-back NPRs. Initially, NPC MASTER H is not asserted which causes CYCLE COUNT to direct set. Near the end of the first cycle, MSYN WAIT is triggered which toggles CYCLE COUNT. The low (0) output of the flip-flop is fed through gates E98 and E97. As a result of the double inversion, the D-input is low which causes the flip-flop to reset. Assume that the RH11 is not in BUS HOG mode (pin 10 of E98 asserted high), there is no TRE error (pin 5 of E97 asserted high), and word count overflow, exception stop, or non-existent memory is not holding the flip-flop direct set. The RH11 monitors the flip-flop at END CYCLE time. Since CYCLE COUNT is reset, it indicates the first NPR cycle is being performed. The second MSYN WAIT signal toggles the CYCLE COUNT flip-flop again. Since the flip-flop was reset, the high output from pin 6 is reflected as a high level at the D-input. This action causes the flip-flop to set, indicating the second NPR cycle is being performed.

Whenever the CYCLE COUNT flip-flop is set, gates E71 (zone A-1) and E97 (zone B-2) are enabled. At END CYCLE time, therefore, gate E96 (zone B-1) is enabled to assert CLR BBSY L. This indicates that the RH11 has completed the second cycle of back-to-back NPRs or desires to terminate after the first cycle.

If the RH11 is in BUS HOG mode or if a TRE (Transfer Error) occurs, the CYCLE COUNT is prevented from toggling because a high level is presented at the data input.

The NEXT CYCLE flip-flop determines whether a second memory cycle is to be performed in the NPR sequence. If the NEXT CYCLE signal is asserted, a second cycle is desired, and the reset output of the NEXT CYCLE flip-flop goes low which inhibits the clearing of BBSY. The NEXT signal indicates the availability of a data word in the Silo indicated by Input Ready or Output Ready (depending on the function performed). If the NEXT signal is not asserted, indicating a second cycle is not desired, the reset output of NEXT CYCLE goes high enabling gates E97 and E96 (zone B-2). At END CYCLE time, E96 is qualified and BBSY is cleared terminating the transfer.

5.12.8 ERROR Conditions

The error conditions in the RH11 can also cause a cycle to terminate. The UPE (Unibus Parity Error) and WCE (Write-Check Error), if asserted at END CYCLE time, cause BBSY to clear. NEM (Non-Existent Memory), if asserted, keeps the CYCLE COUNT flip-flop direct set so the flip-flop cannot toggle. A TRE error, if asserted, keeps the data input high to prevent the CYCLE COUNT flip-flop from toggling.

5.12.9 1-Cycle Jumper

If the RH11 is to do single NPR cycles, a jumper designated "1 CYCLE" and located in zone B-5 is inserted. This places a steady high level at the data input to the CYCLE COUNT flip-flop, causing single memory cycle NPR sequences to always be performed.

The SACK ENB H signal is always asserted at the output of gate E96, pin 8. This signal allows the SACK flip-flop to be cleared when the RH11 becomes bus master and allows NPR arbitration to occur on the Unibus.

5.12.10 BUS HOG Mode

In BUS HOG mode, the RH11 desires to hold onto the Unibus to transfer the total number of words indicated in the word counter. This feature is only employed on Unibus B if this bus is dedicated and no other devices are connected to it. Its purpose is to reduct the NPR latency time of the Unibus. The RH11 enters BUS HOG mode by doing the first NPR cycle and holding the Unibus by asserting BBSY until the required number of words have been transferred or an error condition occurs.

The MSYN inhibit conditions (Paragraph 5.12.4) locks the Unibus cycle timing with the Silo buffer word rate.

To implement BUS HOG mode, the jumper in zone D-2 is cut which enables gate E98. If Unibus B is selected, the gate is qualified, and BUS HOG L is asserted. This signal forces the NEXT CYCLE flip-flop set, indicating another cycle is to be performed. With this flip-flop set, CLR BBSY L is inhibited (except if a UPE or WCE error is raised at END CYCLE time). In addition, BUS HOG L is applied to gate E98, causing a low input to be applied to the D-input of the CYCLE COUNT flip-flop. This overrides the toggling action from pin 6 of the CYCLE COUNT flip-flop and prevents the flip-flop from counting cycles. However, it still allows errors (TRE) or word count overflow to terminate the cycle.

NOTE

The "1 CYCLE" jumper must not be inserted and BUSB must be selected to implement the BUS HOG mode of operation.

5.13 LOGIC DIAGRAM DBCB

This diagram contains the logic used to transfer data into IBUF and from IBUF into the Silo (Silo input logic). Also, the diagram contains the logic used to clock data out of the Silo and into OBUF (Silo output logic).

5.13.1 Silo Input Logic

Data is supplied to IBUF as a result of one of the following conditions:

a. During a Write command – In this case, WRITE H and MSYN WAIT (1) H are asserted which qualifies gate E72, and causes the output of E72, pin 11 to go high for 75 ns. The effect of this is described in subsequent paragraphs. Signal MSYN WAIT (1) H is a 75 ns pulse which occurs during every Unibus cycle. The positive-going leading edge of this pulse is used to clock data off the Unibus during a Write (WRITE H) command. The data is transferred to IBUF, bubbled through the Silo into OBUF, and is written on the drive.

b. During a read or write-check operation – In a read operation, the synchronous data from the Massbus is clocked into IBUF, bubbled through the Silo into OBUF, and then to the Unibus. In a write-check operation, the synchronous Massbus data is clocked into IBUF, bubbled through the Silo into OBUF, and then to a series of Exclusive-OR gates where it is compared to the corresponding memory location from which it was written. The READ + WR CHK H signal is asserted during a read or write-check operation and is ANDed with 150 ns pulse in gate E77 to initiate this action. The 150 ns pulse is produced by one-shot multivibrator E58 which is triggered by the positive-going trailing edge of DRIVE CLK H signal (zone D-7). Also, when an exception condition is detected (error condition in the device), a special stop word is inserted into the Silo to allow all previous data words in the buffer to be transferred before signaling the RDY state. The positive-going trailing edge of EXCP L, which is an exception condition at EBL time, will fire the 150 ns one-shot. Either of these two conditions mentioned above will cause E72, pin 11 to go high for 150 ns.

c. When the program is loading data in the Silo – This function is used during maintenance and allows the data buffer to be read from or written into by the program. To accomplish this, REG STR H and DB IN H are both asserted. When this occurs, both inputs to the lower AND gate of E77 are high which cause the output of gate E72, pin 11 to go high for 125 ns. The REG STR signal allows the RH11 or one of the device registers to be written into. In this case, the register specified is the data buffer as designated by the DB IN H signal.

Consequently, the three situations described above cause the output of E72, pin 11 to go high for 75 to 150 ns, depending on the condition causing the output. This pulse is designated CLK IBUF H and clocks the data from the data lines into IBUF. IBUF is shown on logic diagrams DBCC and DBCD. The output of E72, pin 11 also direct sets the IBUF FULL flip-flop via inverter E82, pin 10.

When the trailing edge from E82, pin 10 goes positive (75 to 150 ns after the negative-going leading edge), the BUBBLE IN flip-flop is set.

The width of the pulse at the output of E72 is sufficient to guarantee that the data is clocked into IBUF and has adequate time to be clocked into the Silo. In other words, the pulse width ensures that the data has time to be propagated through IBUF.

When the BUBBLE IN flip-flop sets and the Input Ready signals (IR5 through IR1) are asserted, a SHIFT IN H signal is generated which allows the data to be shifted into the Silo (see gate E78, pin 4). Signals IR5 through IR1 originate from the five parallel ICs which comprise the 18-bit data word. When IR5 through IR1 is asserted, it means that the Silo is ready to accept data from IBUF. The Input Ready signals are guaranteed to have a certain width to comply with the specification of the Silo.

When the Input Ready signals are no longer asserted, the output of E62, pin 8 goes high and clocks the IBUF FULL flip-flop clear since the data has been accepted by the Silo. The output of IBUF FULL, in turn, clears the BUBBLE IN flip-flop. The Input Ready signals, when not asserted,

indicate that the data need not be stored any longer in IBUF and sufficient time has ensued to strobe the data into the Silo. After the data has bubbled out of the first cell in the Silo, the Input Ready signals once again are asserted. Consequently, these signals are asserted when an empty data cell exists at the bottom of the Silo buffer. This timing sequence of INPUT RDY and the movement of data in the Silo is all accomplished in the 3341 Silo IC.

NOTE

The time required for a data word to propagate from the bottom cell to the top cell in the Silo is specified from 0 to 32 μs. For an empty Silo, the typical time is 16 μs but may vary between Silos due to internal characteristics.

DLT IN

When inputting data to the Silo, a DLT (data late) error can be raised in one of the following two instances:

a. If a word is stored in IBUF [IBUF FULL (1) H] and a second word is to be loaded from the Massbus into IBUF during a Read or Write-check command, the DLT IN flip-flop is set. The READ + WR CHK signal is ANDed with a 150 ns pulse derived from DRIVE CLK (or EXCP for the stop word case) and is applied to the clock input of DLT IN. The data input monitors the IBUF FULL flip-flop and, if IBUF is full, DLT IN is set. The 0 output of DLT IN causes DLT to be created at the output of E72, pin 8. This condition would occur if the Unibus latency time is increased to the point where the Unibus cannot accept data from the Silo at a fast enough rate.

b. A maintenance feature is provided in the DLT logic. The program can load 66 words in the DB register, thus filling IBUF, the Silo, and OBUF. The next word that is loaded in IBUF simulates a DLT error which is posted in bit 15 of CS2. This condition is implemented by DB IN H and REG STR H signals being asserted which cause the DLT IN flip-flop to be clocked to a 1 when IBUF FULL is asserted. As a result, a DLT error at E72, pin 8 is raised.

   A third condition causes the DLT IN flip-flop to set when performing any of the data transfer commands over BUSB. If NPR transfers are being done on Unibus B and the processor issues an initialize pulse or a power fail occurs on Unibus B, a CLRB H signal is asserted and is applied to gate E79. The other two inputs to NAND gate E79 are SEL BUS A L (which indicates BUS B is selected when unasserted) and RDY L (which indicates that the RH11 is busy when unasserted). If all three inputs are asserted, the DLT IN flip-flop is set, causing a DLT error to be asserted.

   The DLT error, in this case, does *not* mean that IBUF is full and cannot accept another word but *does* mean that additional transfers cannot be done due to the power fail or initialize condition.

5.13.2 Silo Output Logic

The Silo output logic clocks data words out of the Silo and loads them in OBUF, where they can be transferred to the Unibus (Read command), to the drive (Write command), or to the Exclusive-OR gates in the controller (Write-check).

The output ready signals from each of the five parallel Silo chips are asserted when a data word bubbles to the top cell in the Silo. The output of gate E59, pin 8 is driven low when the output ready signals are asserted. This action causes ORDY H to be asserted at the output of inverter E61, pin 8, indicating a word has bubbled to the top of the Silo. In addition, a SHIFT OUT H signal is asserted provided BUBBLE OUT flip-flop is set. When OBUF is empty, the OBUF FULL flip-flop is cleared which sets the BUBBLE OUT flip-flop which, in turn, qualifies gate E78, pin 1 to enable SHIFT OUT H to be developed. The SHIFT OUT H signal is applied to the Silo and causes the word in the top cell to be transferred out of the Silo. In addition, the SHIFT OUT signal fires one-shot multivibrator E58, pin 4 which creates a 45 ns negative-going pulse used to deskew the data at the output of the Silo before it is loaded into OBUF. The positive-going trailing edge of the SHIFT OUT signal fires one-shot multivibrator E70. The negative-going edge from E70, pin 4 creates a second 45 ns pulse which is used to generate CLK OBUF H. CLK OBUF H loads the data word from the Silo into OBUF. The positive-going pulse from the 1 side of E70 generates SET OFULL L if EXC STOP has not been asserted. The SET OFULL L signal direct sets the OBUF FULL flip-flop, indicating that OBUF is presently storing a valid data word.

NOTE

If OBUF is full, the OBUF FULL flip-flop is set and the BUBBLE OUT flip-flop is cleared. This condition inhibits the SHIFT OUT signal from clocking the top cell in the Silo.

When the Output Ready signal becomes unasserted due to one of the five parallel Silo chips responding to the SHIFT OUT signal, gate E59, pin 8 is driven high. As a result, the SHIFT OUT signal is terminated and the BUBBLE OUT signal is cleared because OBUF FULL has been set and has removed the direct set on the BUBBLE OUT flip-flop. The purpose of the BUBBLE OUT flip-flop is to enable the completion of the SHIFT OUT signal after data has been clocked into OBUF and OBUF FULL has been set. When the next word bubbles to the top of the Silo, the word will not be clocked into OBUF since the BUBBLE OUT flip-flop is clear which inhibits the SHIFT OUT signal from shifting the word out of the Silo.

Consequently, the OBUF FULL flip-flop must be cleared in order that the BUBBLE OUT flip-flop becomes set and allows SHIFT OUT pulses. When this occurs, the data in OBUF is automatically written over by the next data word bubbling out of the top of the Silo. The OBUF FULL flip-flop can be cleared under the following conditions:

a. When the program is reading the Data Buffer register. After the program reads the data buffer, the next data word is allowed to sequence to the top. This logic is shown in NAND gate E75, pin 6. The DB OUT H signal occurs when the data buffer is read, and the DB OCLK H signal occurs when the RH11 asserts SSYN for that register operation. When the master device removes MSYN and the RH11 is deselected, the DB OCLK signal is unasserted, causing a positive-going edge at the clock input to OBUF FULL. This indicates that the RH11 does not have to store the data any longer and OBUF FULL is clear.

b. When the RH11 is doing a write operation (memory-to-drive transfer). This condition is implemented by the WRITE H and DRIVE CLK H signals at the input to NAND gate E75, pin 3. Signal WRITE H denotes a write operation. Upon the assertion of DRIVE CLK H, NAND gate E74, pin 3 goes low and the drive clocks the data off the Massbus.

   On the trailing edge of DRIVE CLK, E75, pin 3 goes high to clock the OBUF FULL flip-flop clear, and allows the RH11 to change the data on the Massbus.

c. When the RH11 is doing a read (drive-to-memory transfer) or write-check operation where the output of OBUF is applied to the Exclusive-OR gates in the controller. In this instance, READ + WR CHK H and DATA STROBE are applied to gate E76. Signal READ + WR CHK H, when asserted, denotes a read or write-check operation; signal DATA STROBE H, when asserted, drives the output of E76, pin 6 low. When DATA STROBE H goes unasserted, E76, pin 6 is driven high, clocking the OBUF FULL flip-flop clear and allowing the RH11 to change the data on the Unibus. If WCE (Write-Check Error) is detected, the data word in OBUF is frozen by forcing gate E76, pin 6 low which keeps the clock input to OBUF FULL low.

DLT OUT Flip-Flop

DLT OUT flip-flop E73 is shown in zone D-2. This flip-flop is clocked by OUT CLK L which goes positive on the trailing edge of DRIVE CLK during a write operation (see gate E75, pin 3 in zone B-6). On the trailing edge of DRIVE CLK (SYNC CLK from the drive), the RH11 monitors the top cell in the Silo to determine if a word is there to output to OBUF. If a word is present, it is indicated on the trailing edge of DRIVE CLK by ORDY H being asserted, which inhibits DLT from being generated via gate E71. If ORDY is not asserted, indicating the absence of a word available for OBUF, and it is not the last word (LWRD asserted), the DLT OUT flip-flop is clocked to the Set state, thus enabling gate E72, pin 8 to post a DLT error.

The DLT OUT flip-flop can be direct set if DB OCLK H, DB OUT H, and OBUF FULL (0) H are asserted. Signal DB OCLK H is asserted at the time of MSYN; DB OUT H denotes a register select function is specified; and OBUF FULL (0) H indicates OBUF is empty. The setting of DLT OUT, in this manner, occurs when the program tries to read the Data Buffer register without a word available in it (OBUF). It allows the program to simulate the clocking of non-existent words out of OBUF in order to post DLT errors. This feature is used as a maintenance aid.

Generation of DRIVE CLK H

The DRIVE CLK H signal is asserted when the disk has rotated to the correct address and starts to transfer data to or from that address. At that time the drive issues SYNC CLK H, which is DRIVE CLK H if no error conditions are present (indicated by INH CLK L) and if the desired number of words have not been transferred as indicated by DRWC OFLO (0). As previously described, SYNC CLK signals originate at the drive. On the leading edge of SYNC CLK, the drive either accepts the data (Write) or prepares it for transfer to the RH11 Controller (Read or Write-Check).

On the trailing edge of SYNC CLK, the controller accepts the data (Read or Write-Check) or prepares the next word (Write). If word count overflow has not occurred (indicating more words are to be transferred) and if no error conditions are present, the SYNC CLK signal becomes DRIVE CLK in the RH11. This is accomplished through gate E68 in zone C-7.

5.13.3 Error Flip-Flop

If an error condition occurs in the controller or the drive, a TRE (Transfer Error) is posted. TRE (bit 14 of CS1) is applied to the data input of the ERROR flip-flop (zone B-7). The error condition sets the ERROR flip-flop when clocked by SYNC CLK which then causes an INH CLK assertion to prevent further DRIVE CLK signals. The purpose of synchronizing the TRE with SYNC CLK is to prevent spurious spikes from occurring on DRIVE CLK during detection of an error. The ERROR flip-flop is cleared by SILO CLR L which is derived from CLR + GO CLR.

5.13.4 Generation of INH CLK L

INH CLK L is asserted as a result of a TRE or DLT error. These error conditions are ORed in gate E71. INH CLK L prevents DRIVE CLK H from occurring and thus prevents the RH11 from accepting any more data words from the device.

5.13.5 SILO CLR Generation

The SILO CLR L signal is generated by CLR + GO CLR which triggers 400 ns one-shot multivibrator E92. The 400 ns provides the required pulse width to clear the Silo chip. The CLR signal occurs when the program sets the CLEAR bit (bit 5 in CS2) when a reset or Unibus initialize pulse is asserted, or when the power supply is failing which asserts the DC LO L signal on the Unibus. The GO CLR signal is asserted when a data transfer command is loaded with the GO bit asserted. There are two instances in which the pulse used to generate CLR + GO CLR L is too narrow (less than 400 ns) to clear the Silo: 1) when the program is loading the CLEAR bit and 2) when a data transfer command is loaded in CS1 with the GO bit asserted. In these cases, the CLR + GO CLR is applied to the one-shot which widens the pulse to 400 ns. The other conditions used to generate CLR + GO CLR L (reset, Unibus initialize, and DC LO) are applied to gate E98 to ensure full width of the clear condition. Signal SILO CLR is used to initialize the Silo and Silo control signals.

5.13.6 Write Clock

The WRITE CLK H signal at the output of AND gate E90, pin 6 is the SYNC CLK signal from the drive which is ANDed with the WRITE H signal. Signal WRITE CLK H is sent back to the drive over the Massbus and is used by the drive to clock data into its buffer during a write operation. The purpose of WRITE CLK is to ensure the proper deskew of data on the Massbus during write operations.

5.13.7 Gating Synchronous Data

The GATE SYNCD signal at the output of gate E63, pin 11 turns on the Massbus drivers, when asserted, and allows the data from OBUF to be gated on the Massbus synchronous data lines. This signal is asserted during a write operation if drive word count overflow has not occurred or an error condition has not been raised. If an error or drive word count overflow occurs before the end of a sector, GATE SYNCD H goes unasserted which disables the data drivers, causing 0s to be written in the remaining words in the sector by presenting all 0s on the synchronous Massbus data lines.

5.13.8 Data Requests (Write Command)

When requesting words from the Unibus during a write operation, the DATA REQ L signal must be asserted. This signal is transferred to the BCT module to initiate an NPR request on the Unibus. Signal DATA REQ L is asserted when IBUF is empty, provided there is no word count overflow or no TRE. This is shown in AND gate E68 (output pin 8) which feeds gate E67. The output of E82 is fed back to AND-OR gate E67 and serves to keep this circuit latched. The circuit will unlatch as a result of CLR BBSY L or RDY L. Signal CLR BBSY L occurs when the RH11 gives up the Unibus. After the first DATA REQ, subsequent DATA REQ signals are asserted by the SHIFT IN H signal fed to gate E67. The SHIFT IN signal anticipates the availability of IBUF to accept a data word from the Unibus.

5.13.9 Data Requests (Read or Write-Check)

The RH11 requests the Unibus by the DATA REQ signal which is used to initiate the NPR logic on diagram BCTH. The DATA REQ signal is asserted by the Silo output logic when OBUF FULL is set (indicating a word has bubbled up the Silo and into OBUF), there is no TRE (Transfer Error), and a READ + WR CHK command is specified. The logic is implemented in gate E68, pin 6. The output at pin 6 is applied to gate E67. The output of inverter E82, pin 6 latches gate E67 until unlatched by CLR BBSY L. Signal CLR BBSY L is generated at the end of the cycle in a single-cycle NPR or at the end of the second cycle when doing back-to-back NPR cycles.

5.13.10 NEXT SIGNAL (Write)

The NEXT signal shown in zone C-1, when asserted, causes back-to-back NPR cycles to occur. The DATA REQ L signal is keyed when the IBUF is empty or SHIFT IN

occurs. As soon as the RH11 gains control of the Unibus, it asserts BBSY, prepares to obtain the data word, and monitors Input Ready (IRDY). This is done at MSYN WAIT time. If IRDY is asserted, the NEXT signal is generated by AND-OR gate E76 (as a result of IRDY H and WRITE H both being asserted). This means that the bottom cell of the Silo is empty, and the RH11 will do a second NPR cycle before releasing the Unibus. If the NEXT signal is not asserted, it indicates that the bottom cell of the Silo is full. In this case, the single NPR cycle is completed, the bus is released, and the RH11 waits for SHIFT IN to be asserted to repeat the cycle.

5.13.11 NEXT SIGNAL (Read or Write-Check)

In order for the RH11 to initiate back-to-back NPR cycles, the NEXT L signal must be asserted. Signal NEXT L is asserted when OR5 through OR1 are asserted (indicating a data word in the top cell of the Silo) and READ + WR CHK H is asserted. Consequently, the RH11 monitors the leading edge of MSYN WAIT in the first memory cycle and determines whether there is a word in the top cell of the Silo (ORDY asserted). If there is, the NEXT CYCLE flip-flop is set on DBCA and back-to-back NPR cycles are done. If there is no word in the top cell of the Silo, NEXT L is unasserted to inhibit the next NPR cycle and CLR BBSY L is asserted which removes the latch keeping the DATA REQ signal asserted.

5.13.12 Word Count Increment (Write Command)

The INC WC gate below NEXT causes the word counter to be incremented if DESK MSYN is asserted. Consequently, each memory cycle causes the word counter to increment.

5.13.13 Word Count Increment (Read or Write-Check)

The INC WC L signal at the output of gate E77, pin 6 is asserted during a read or write-check operation when the SHIFT OUT signal is generated. This indicates a word is in OBUF ready to transfer and the word counter is thus incremented.

5.13.14 EXCEPTION ERROR (Write Command)

The EXCP ERR L signal indicates that an exception condition in the drive (any error set in the ER register) can be recognized and may cause TRE to set to end the operation. When performing a Write command, EXCP SAVE (1) H immediately causes EXCP ERR L to be asserted.

5.13.15 EXCEPTION ERROR (READ or WRITE-CHECK)

When performing a read or write-check operation and an exception condition is raised in the drive, it is desirable to finish transferring the data words which already exist in the Silo before returning to the Ready state. This is accomplished by inserting a stop word into the Silo upon detection of exception and waiting for the word to appear at the output of the Silo before raising the error condition as TRE and thus producing the return to RDY state.

The above operation is performed by causing a 150 ns pulse to be generated by one-shot E58 in zone D7 when the positive-going trailing edge of EXCP L occurs, which at the same time sets the EXCP SAVE flip-flop located on drawing DBCD. The 150 ns pulse creates an input clock to the Silo as previously described. The EXCP SAVE condition is then inserted in the 20th bit position of the Silo and begins to bubble to the top as does a normal data word. When this stop word reaches the top cell of the Silo, the EXCP STOP signal is asserted, indicating the last word in the Silo is or has been transferred on the Unibus. The Silo control then attempts to transfer this stop word into OBUF. However, the EXCP STOP signal diverts the 45 ns pulse from one-shot E70, pin 13 to cause EXCP ERR L and prevents the SET OFULL signal from setting OBUF FULL (an indication that means a valid data word exists in OBUF). If, however, the WC OFLO (1) condition is asserted when EXCP SAVE has been set, the EXCP ERR signal is immediately asserted, causing TRE to set as the RH11 returns to the Ready state.

NOTE

If another error occurs causing TRE to set, operations on the Unibus are halted and the RH11 will return to the Ready state with data words remaining in the Silo buffer.

5.14 LOGIC DIAGRAM DBCC

This diagram shows bits 11 through 0 of the DMX, IMX, IBUF, Silo and OBUF. For a Write command, the data is gated from the appropriate Unibus (DMX) to IMX, and then through IBUF, the Silo, and OBUF for transfer to the drive. For a Read command, the data from the drive is supplied to IMX from the Massbus and then to IBUF, the Silo, and OBUF for transfer onto the appropriate Unibus. For a Write-check command, the output of DMX (from the Unibus) is compared with the synchronous data at the output of OBUF (from the drive).

When the RH11 is bus master (NPC MASTER L asserted), the CSRA SEL BUSA signal is checked to determine which Unibus is selected. If CSRA SEL BUSA is asserted, Unibus A is selected; if the signal is not asserted, Unibus B is selected. If the RH11 is not master (NPC MASTER L unasserted), the DMX is selected to BUSA. If the RH11 is not performing a Read or Write-check command, IMX is selected to accept DMX rather than Massbus synchronous

data. In this case, the DMX and IMX are set up to only accept data from Unibus A regardless of the setting of the PORT SEL bit. Consequently, when the program is loading data into the Data Buffer register, the data originates from Unibus A. The clocking logic for the IBUF, Silo, and OBUF is shown on sheet DBCB.

5.15 LOGIC DIAGRAM DBCD

This diagram shows bits 17 through 12 of the DMX, IMX, IBUF, Silo, and OBUF. The description of these bits is similar to that described on sheet DBCC.

In addition to selecting the 18 data bits from the Unibus or Massbus, the IMX incorporates a parity bit. During a Write command, the parity bit is forced to 0 through the Silo and into OBUF. The parity bit generated by the drive during a Read or Write-check command is carried through the Silo, providing a parity check of the Silo logic as well as transmission over the Massbus. The parity logic associated with the Massbus is described in more detail on sheet PACA.

The EXCP SAVE flip-flop in zone A-5 stores the fact that an exception condition was received from the drive and is used as an input to the 20th bit position of the Silo. This input provides the stop word described previously on DBCA (EXCP ERR) which will appear as EXCP STOP when all data words in the Silo have been transmitted.

The top of sheet DBCD shows 18 Exclusive-OR gates used during a Write-check command. These gates compare the data in OBUF that was taken from the drive to the output of DMX which represents the corresponding memory word. The outputs of the Exclusive-OR gates are open-collector ORed such that if corresponding bits fail to compare, an error will be registered and is indicated by the setting of the WCE (Write-Check Error) flip-flop. This flip-flop checks the status of the open-collector Exclusive-OR gates at the time of the MSYN WAIT signal and is latched if an error is detected. The flip-flop remains in this state until the CLR ERR signal is asserted.

5.16 LOGIC DIAGRAM DBCE

This diagram contains the drivers and receivers (8838 transceivers) for the Unibus B data lines. The Unibus B drivers drive the data from OBUF onto the BUSB data lines. In order to enable the drivers, the RH11 must be bus master, Unibus B must be selected (SEL BUSA H not asserted), and a read function must be specified (DATA TO BUS L asserted).

The Unibus B receivers receive the data from the Unibus (BUSB D00 L through BUSB D17 L) and supply them to the RH11 where the signals are designated UNIB D00 H through UNIB D17 H.

Bits 16 and 17 of the Unibus B data which is normally the Unibus PA and PB lines are employed as data when the EN DATA BUSB L signal is asserted. This signal is asserted when Unibus B is selected (SEL BUSA H unasserted) and the 16 BIT BUSB jumper (W2) shown on sheet DBCH is cut.

5.17 LOGIC DIAGRAM DBCF

This logic diagram contains the drivers and receivers (8838 transceivers) for the Unibus A data lines. The pull-up resistors for the internal open-collector bus (BUSI) in the RH11 are also shown. This internal open-collector bus is used when the program is reading information from an RH11 register (or a drive register via the Massbus control lines) and is actually the output of the 8234 open-collector multiplexers which route information to the Unibus.

Data from BUSI (BUSI D00 OUT L through BUSI D15 OUT L) is supplied to the Unibus A drivers which drive these signals onto the Unibus where they are designated BUSA D00 L through BUSA D15 L.

Data from OBUF is applied to the Unibus via 8881 bus drivers. The 8881 drivers are enabled if the RH11 is bus master, if a read operation is specified (DATA TO BUS H asserted), and if Unibus A is selected (SEL BUSA H asserted).

Data from Unibus A (BUSA D00 L through BUSA D17 L) is supplied to the RH11 via the 8838 gates and is designated D00 IN H through D17 IN H in the RH11.

Bits 16 and 17 of Unibus A data which is normally the Unibus PA and PB lines are employed as data when EN DATA BUSA L is asserted. This signal is asserted when Unibus A is selected (SEL BUSA H asserted) and the 16 BIT BUSA jumper (W1) shown on sheet DBCH is cut.

5.18 LOGIC DIAGRAM DBCH

This diagram contains the parity jumpers for Unibus A and Unibus B multiplexer E21 to monitor parity, and four 8234 multiplexers to multiplex the Massbus control lines with the data buffer output.

5.18.1 Parity Jumpers

The lower portion of the diagram shows a parity jumper (16 BIT BUSA) for Unibus A and a parity jumper (16 BIT BUSB) for Unibus B. The operation of each is similar, so only the Unibus B parity jumper will be described. If the jumper is left in, gate E27, pin 8 is inhibited from generating EN DATA BUSB L, indicating that the upper two bits (D16 and D17) are to be used as parity bits (PA and PB). In addition, AND gate E28, pin 6 is qualified by the jumper for the selected bus being inserted which causes EN PAR H (enable parity) to be generated. When the 16 Bit BUSB jumper is cut, one input to E27, pin 9 is enabled. If Unibus B is selected, the output goes low, creates EN DATA BUSB L, and disables EN PAR which indicates that the upper two bits are used as data bits. The lower jumper and gate for Unibus A are the same except that the gate is qualified by selecting Unibus A and not Unibus B.

5.18.2 74157 Parity Multiplexer

Multiplexer E21 monitors the parity bits for Unibus A and Unibus B. The multiplexer is enabled by EN PAR H. A parity error is detected when parity bit PB is asserted and PA is unasserted. For example, if Unibus A is selected, D16 IN H (PA) is unasserted and D17 IN H (PB) is asserted, which causes pins 3 and 4 of gate E79 to be enabled. At DATA STR time, E79 is qualified generating SET UPE L (SET Unibus Parity Error).

5.18.3 8234 Control Line/Data Buffer Multiplexing

The 8234 multiplexers select the Massbus control lines or the outputs from OBUF for transfer to the RH11 internal open-collector bus (BUSI). When the program reads a remote register, the 8234 open-collector multiplexers gate the Massbus control lines (C00 IN H through C15 IN H) to the internal bus (BUSI). In this instance, the multiplexers are enabled by CNTL OUT L, which is the signal associated with reading a remote register. When the program is reading the data buffer for maintenance purposes, the data buffer outputs (OBUF 00 H through OBUF 15 H) are multiplexed onto the BUSI lines. The multiplexers are enabled by DB OUT L, in this case, which is the signal associated with reading the data buffer.

5.19 LOGIC DIAGRAM DBCJ

The logic diagram shows the START counter, two 8234 open-collector multiplexers which select the low byte of the CS1 or CS2 register onto BUSI, and a regulator circuit.

5.19.1 Start Counter

The Start Counter consists of two ICs (E64 and E65) connected in series. Each time a data transfer command is loaded in the RH11, the CLR + GO CLR signal resets the counter to 0. For a write operation, words are fetched from memory. Every word fetched is accompanied by DATA STR which clocks the counter and causes it to increment. A selectable count range may be selected to determine when the START signal is to be asserted which will cause the RUN assertion on the Massbus. This is done to prefill the Silo with data before requesting the drive to start to perform the write operation. A count of 64 is designated by the FULL jumper being connected. Other jumper configurations may be inserted. For example, if the HALF jumper is inserted, the START H signal will be asserted at a count of 32. If the QTR jumper is connected, the START H signal will be asserted at a count of 16. Only one jumper may be inserted at any given time and, with no jumper inserted, START will always be asserted allowing RUN to be asserted when the first word reaches OBUF (see CSRA). If a write operation is designated, the START signal generates RUN when the Silo is filled to the selected value. This connects the RH11 to the drive and signals the beginning of the data transfer on the synchronous Massbus.

5.19.2 CS1/CS2 Gating Onto BUSI

The two 8234 open-collector multiplexers select the low byte of the CS1 or CS2 register and gate the contents onto the internal bus (BUSI). Inputs from the CS1 register are gated onto BUSI when CS1 OUT is asserted and the inputs from the CS2 register are gated onto BUSI when CS2 OUT is asserted.

5.19.3 Voltage Regulator

This diagram shows a regulator circuit which converts -15 Vdc to -12 Vdc for use on the Silo chips. The 2N5639 FET is connected as a constant current generator to stabilize the bias current through Zener diode 1N759A. The 2N2409A transistor is used as the series pass element (regulator in series with the load current).

5.20 M7297 PARITY CONTROL MODULE (PACA)

The M7297 Parity Control module contains the parity logic for parity generation and checking both the synchronous and the asynchronous sections of the Massbus. Each drive contains associated parity generation and checking logic. Sheet PACA shows the Massbus parity logic, consisting of 74180 8-bit parity generator/checkers. The three 74180s on the left are used for parity on the synchronous Massbus and the remaining four 74180s are used for parity on the asynchronous Massbus. Parity on the Massbus is odd.

5.20.1 Synchronous Massbus Parity

The 74180 chips serve a dual function. During a write operation, the 74180 chips in the RH11 *generate* parity while the associated parity logic in the drive *check* parity. Conversely, during a read or write-check operation, the parity logic in the drive *generate* parity while the 74180s in

the RH11 *check* parity. This is possible with the same set of parity chips because in write, read or write-check operations the parity bit is rippled through the Silo along with the data word. This feature is useful because the parity bit also checks out the Silo logic as well as the Massbus.

The 18 data bits and the parity bit from OBUF are applied to the 3 74180 chips. This can be considered as a 19-bit data word. Each 74180 also has an ODD and EVEN input and a ΣEVEN and a ΣODD output. The EVEN input is normally low and the ODD input is normally high, selecting the 74180 for odd parity. The 19 data bits and the ODD input are summed to yield an asserted ΣEVEN or ΣODD output. For example, if all the data bits (18 data bits plus the parity bit) are asserted, the sum is odd. This is summed with the ODD input to yield an even number of 1s. Consequently, the ΣEVEN output is asserted and the disconnected ΣODD output is unasserted. As another example, if the 18 data bits are summed to yield an even number of 1s and the parity bit is unasserted, the result is even. This is summed with the ODD input to yield an odd number. In this case, the ΣEVEN output is unasserted.

5.20.2 Read or Write-Check Parity

Note that the ΣEVEN output is applied to the SYNC PE (Synchronous Parity Error) flip-flop and, if ΣEVEN is asserted, this disables the SYNC PE flip-flop from setting, indicating that there is no parity error. The SYNC PE flip-flop is used when checking parity during a read or write-check operation. The flip-flop is clocked during the trailing edge of DATA STR from the Unibus cycle if WRITE L is unasserted which occurs during a Read or Write-Check command. A third input to gate E5, which feeds the SYNC PE clock input, is the 0 output of the flip-flop which prevents the flip-flop from being clocked again. In this instance, the flip-flop is direct cleared by the CLR ERR L signal from sheet CSRB.

5.20.3 Write Parity

For a write operation, the 18 data bits and the parity bit are supplied to the drive to yield an odd number of 1s. To accomplish this, the 19th bit, designated OBUF PA H, is forced to a 0 so the 18 data bits (designated OBUF 00 through OBUF 17) determine whether the ΣEVEN output of the 74180 is asserted or unasserted. For example, assume that the sum of the 18 data bits is odd (the parity bit OBUF PA can be disregarded since it is a forced 0). These bits are summed with the ODD input to assert the ΣEVEN output. This inhibits gate E7, pin 8 from generating a sync parity bit (SYNC PA H), if the second input to this gate is temporarily disregarded. Since the data is an odd number of 1s, it is not necessary to generate a parity bit. If the data contains an even number of 1s, it yields an odd number when summed with the ODD input. As a result, the ΣEVEN output goes low generating a SYNC PA bit, which creates odd parity.

In the case where an error condition exists or word count overflow occurs prior to the end of a sector, the remaining words in the sector are filled with 0s. This is accomplished by disabling the data drivers on the Massbus with the signal GATE SYNCD (see sheet DBCB). As a result, the number of 1s is zero which is even. Consequently, a parity bit must be simulated to generate odd parity. This is accomplished by the GATE SYNCD input going unasserted. The situation just described only occurs for a write operation and, consequently, the driver that drives the SYNC PA signal on the Massbus is ANDed with the Write signal.

5.20.4 Asynchronous Massbus Parity

The two 74180 chips in the center of sheet PACA are employed for parity generation when writing into a register in the drive. The 16 data inputs to the chips are from the Unibus A data lines. Note that odd parity is normally selected.

Assume the data inputs contain an even number of 1s. This is summed with the ODD input to assert the ΣODD output which generates CNTL PA OUT H. This is the parity bit generation and is supplied to the Massbus driver for transfer to the drive. If the data inputs contain an odd number of 1s, the CNTL PA OUT H signal is not asserted and no parity bit is generated. When reading from a drive register, a different set of data lines is used and this necessitates two additional 74180 chips to check parity. The lines are the "C" IN lines which are the outputs of the receivers used to monitor the Massbus control information. The parity bit generated by the drive is supplied to the ODD input. The inverted polarity of the parity bit is applied to the EVEN input. The sum of the bits should be odd which means that ΣEVEN should be unasserted. For example, if the 16 data bits are all 1s and the parity bit generated in the drive is a 1, the sum of all bits is 17, which is odd. This causes ΣEVEN to go low, which inhibits NAND gate E5, pin 5 which, in turn, places a low at the D-input to the CNTL PE (control parity error) flip-flop. If the data inputs to the 74180 chips contain an odd number of 1s and the parity bit from the drive (CNTL PA IN H) is asserted (indicating a parity error), the ΣEVEN output is forced high which sets the CNTL PE flip-flop during the trailing edge of CNTL OUT L. This signal is the gating signal used to gate data from the Massbus control lines to the Unibus. When the CNTL PE flip-flop is set, it remains latched by the 0 output feeding the data input via gate E7, pin 3. The flip-flop is cleared in the same manner as the SYNC PE flip-flop by CLR ERR L.

NOTE

The second input to gate E5 is the AS REG signal. This signal inhibits checking parity when the Attention Summary (AS) register is being read. The reason that parity cannot be checked when reading the Attention Summary register is that the AS register in each drive provides only one bit of information and a parity check is meaningless.

The output of the SYNC PE flip-flop causes an MDPE (Massbus Data Parity Error) which appears in bit 8 of the CS2 register and also causes TRE (bit 15 of CS1) to be raised.

The output of the CNTL PE flip-flop causes an MCPE (Massbus Control Parity Error) which appears in bit 13 of the CS1 register and causes SC (bit 15 of CS1).

The PAT H signal can be asserted by the program (bit 4 in CS2) to generate even parity on the Massbus and to check for even parity on the synchronous data lines when performing Read or Write-check commands. This maintenance feature allows verification of the parity logic in the drive.

The M7297 Parity Control module contains two light-emitting diodes: one for control bus parity error and one for synchronous bus parity error. This allows the maintenance personnel to quickly detect whether the parity error occurred on the synchronous section of the Massbus or on the control (asynchronous) section of the Massbus.

5.21 M5904 MASSBUS TRANSCEIVER MBSA, MBSB, MBSC

The Massbus consists of three Massbus cables and associated Massbus transceiver modules. A 40-pin connector on each M5904 Massbus Transceiver module connects the Transceivers to the Massbus cables. The transceivers plug into slots C4-D4, C5-D5, and C6-D6 in the RH11 to connect the RH11 to the Massbus.

Each signal on the Massbus is applied to a differential circuit which transmits the true signal and an inversion of the signal along the bus. At the other end of the bus, the signals are received by differential receivers which output the true form of the signal. The differential circuitry serves to eliminate noise since any common mode noise will be cancelled at the differential receivers. For additional description, refer to M5904 Massbus Transceiver module in Appendix A.

The three Massbus cables are designated: Massbus Cable A (D-BS-RH11-0-02, MBSA) Massbus Cable B (D-BS-RH11-0-02, MBSB) Massbus Cable C (D-BS-RH11-0-02, MBSC).

The M5904 Massbus Transceiver is functionally shown within the dotted block on each drawing. The 40-pin connector is shown in the center of the dotted block. The differential transmitters which drive signals onto the Massbus from the RH11 are shown to the left of the connector. The differential receivers which receive signals from the Massbus are shown to the right of the connector. These signals originate at the drive and are routed to the RH11 via the differential receivers.

To minimize switching of signals on any transceiver module at a given time, the signals are grouped on different modules. For example, OBUF 00–05 H is contained on MBSA, OBUF 06–11 H is contained on MBSB and OBUF 12–17 H is contained on MBSC. The D00 IN H through D15 IN H signals from BUSA are also divided on the three modules in similar manner. The RSEL 0 H through RSEL 4 H signals are grouped on MBSA and MBSB.

The OBUF signals are gated by GATE SYNCD H which enables the output of OBUF to be gated onto the MASS 'D' lines of the Massbus. The D00 IN H through D15 IN H signals which form the MASS 'C' lines are enabled by GATE CNTL H which occurs when the RH11 is writing a remote register. GATE CNTL H is the assertion of DEV SEL and a DATO. The RSEL signals select a drive register and are enabled by the DEV SEL signal. Unit select signals U00 H through U02 H are also enabled by DEV SEL and specify one of eight possible drives. The remaining control signals which are supplied to the drive are also shown. These include WRITE CLK, RUN, DIR TRANS, MB INIT, DEMAND, CNTL PA OUT, SYNC PA, and SUPPLY AC LO.

The signals sent from the drive to the Massbus are SYNC D00 through SYNC D17 which represents synchronous data, and C00 H through C15 H which represents the contents of a drive register. Control signals which include EXCP, EBL, ATTN, SYNC CLK, CNTL PA IN, OCC and TRANS are also shown.

5.22 UNIBUS A CABLE DIAGRAM

The Unibus A cable diagram is shown on D-IC-RH11-0-03. Slots A1 and A9 are wired together as are slots B1 and B9. The slots are wired to provide UNIBUS A IN and UNIBUS A OUT signals, except for the GRANT signals. The GRANT signals are passed through the device before being supplied

to the Unibus out cable. The cable slots occupy slots A1, B1, and A9, B9 as shown in the Module Utilization Chart D-MU-RH11-0-01.

The three small peripheral controller devices are shown on the lower portion of the cable diagram. If the devices are inserted in the slots, the GRANT signals are passed from device to device. G727 Grant Continuity modules are inserted in any of these slots (D7, D8, or D9) not containing small peripheral controllers. The designated slots for the peripheral controllers are C7 through F7, C8 through F8, and C9 through F9 (see D-MU-RH11-0-01).

Also shown on the diagram is the M688 Power Fail driver which buffers the AC LO and DC LO signals and supplies them to Unibus A for power fail detection.

5.23 UNIBUS B CABLE DIAGRAM

The Unibus B cable diagram is shown in drawing D-IC-RH11-0-04. It is similar to the Unibus A cable diagram with the following exceptions:

1. The signals are prefixed by BUSB to denote Unibus B.

2. In Unibus A, the BUS GRANT signals are passed through the devices and are not directly wired from the UNIBUS A IN slot to the UNIBUS A OUT slot. In Unibus B, the BUS GRANT signals are directly wired from the UNIBUS B IN slot to the UNIBUS B OUT slot. The reason for this is that the RH11 cannot interrupt on Unibus B and, consequently, does not have to look at the BUS GRANT signals. Note that the NPG signal is not directly connected but is passed through the device on both Unibuses.

Unibus B has an M688 Power Fail driver similar to that on Unibus A. This is to assert BUSB AC LO or BUSB DC LO on Unibus B in the event of a power-fail condition.

5.24 M9300 UNIBUS B TERMINATOR

The M9300 Unibus B Terminator is shown in drawing D-CS-M9300-0-1. Three main functions performed by the M9300 are:

1. to properly terminate the Unibus cable
2. to arbitrate NPRs and issue NPGs
3. to prevent NO-SACK timeout.

5.24.1 NPR Arbitration and Issuance of NPG

In certain multiport memory configurations, Unibus B will be employed without a processor. In order for the RH11 to acquire bus mastership, it must issue an NPR and must receive an NPG signal. Since there is no processor to issue grants, the arbitration logic on the M9300 performs this function. The logic is shown on the left-hand side of the drawing. If the M9300 is connected at the beginning of the Unibus and no processor is connected to this Unibus, jumper W1 is cut. This enables the arbitration logic as described below.

The NPR requests are arbitrated by the M9300. If an NPR request is received (and BUS SACK is not present or has not been on the Unibus for 100 ns), the latch consisting of E2, pin 3 and E2, pin 6 is enabled. When the NPR request is received, pin 1 goes low forcing pin 3 high which, in turn, forces pin 6 low and enables signal BUS NPG H to be generated.

NOTE

If a BUS SACK signal and an NPR request are both received, pins 3 and 6 will both be high because the arbitration logic recognizes NPRs while SACK is asserted. In accordance with the Unibus specification, a GRANT signal cannot be issued until 100 ns after the SACK signal is removed. This logic is shown by gates E1, pin 14, E2 pin 11, E6 pin 3, 100 ns delay DL1, E5 pin 2, and E2 pin 6. When BUS SACK is asserted, E2 pin 6 is high and inhibits NPG H from occurring. After BUS SACK is unasserted for 100 ns, E2, pin 5 goes high to allow the grant to be asserted.

The NPR request, as previously described, generates the NPG H signal. In addition, however, it fires 10 μs one-shot multivibrator E4, pin 4 via gate E2, pin 6 If the BUS SACK signal is not returned within 10 μs, the one-shot times out and the positive-going trailing edge at E4, pin 4 clocks NO-SACK TIMEOUT flip-flop E3 set. The 0 output of this flip-flop goes low and simulates the BUS SACK signal since it is ORed with BUS SACK in gate E6, pin 3. The simulated BUS SACK signal performs two operations: 1) it clears the latch by causing E2, pin 5 to go low, and allows other NPRs to be arbitrated, and 2) after the 100 ns delay through DL1, it direct clears the 10 μs one-shot and the NO-SACK TIMEOUT flip-flop.

In addition to arbitrating NPRs, the M9300 must also simulate a processor when a power-fail condition is asserted. In this case, the device on the Unibus asserts BUS DC LO L. The M9300 receives this signal and returns BUS INIT L via gates E1, pin 2 and E8, pin 1. Note that BUS INIT L is only returned when jumper W1 is cut (no processor connected to Unibus). Consequently, the M9300 simulates the BUS INIT signal from the processor.

If the M9300 is connected at the beginning of the Unibus and there is a processor connected to the Unibus, jumper W1 is not cut. This places a low input at NOR gate E8, pin 5 which causes the output to go high. This output is open-collector ORed with the processor GRANT signal on the Unibus. In this instance, E8, pin 5 diables the arbitration logic in the M9300 from arbitrating NPRs. E8, pin 4 is effectively disconnected from the Unibus, and the processor does the necessary arbitration.

5.24.2 Prevention of NO-SACK TIMEOUT

The logic on the right-hand side of D-CS-M9300-0-01 is employed when the M9300 is connected at the end of the Unibus. The purpose of this logic is to monitor the BUS NPG and BUS GRANT signals and to issue BUS SACK which bypasses the 10 μs timeout logic used in the processor or in an M9300 module when employed as an arbitrator.

If a processor is connected to this Unibus, jumper W3 is cut. Since the M9300 is at the end of the Unibus, jumper W2 is also cut. With W3 cut, NAND gate E6, pin 8 is enabled to pass the BUS GRANT signals, and with jumper W2 cut, NAND gate E8, pin 13 is enabled to pass the BUS GRANT or the BUS NPG signal.

Consequently, any grant that reaches the end of the bus, and has bypassed the device requesting a grant, causes the BUS SACK L signal to be asserted. BUS SACK L is sent to the processor and causes the GRANT signal to drop which, in turn, causes BUS SACK to become unasserted.

The 10 μs timeout logic is overridden as follows. Assume a device issues a request and then suddenly clears it. The processor arbitrates the request and issues the grant, thinking it saw a valid request. The processor then times out for 10 μs waiting for BUS SACK. However, the logic just described causes BUS SACK to be asserted immediately, thus bypassing the timeout feature and improving interrupt response time of the Unibus.

If the M9300 is at the end of the Unibus and there is no processor connected to the bus, then only jumper W2 is cut. With jumper W3 in, the gate (E6, pin 8) which normally passes the BUS GRANT signals is inhibited. Since there is no processor to issue BUS GRANT signals, they have no meaning. These signals are open-collector signals asserted high and since there is nothing to assert them low, they appear as valid BUS GRANT signals on the Unibus. Therefore, jumper W3 is in which disconnects these signals from the Unibus by opening gate E6, pin 8. The BUS NPG signal can be asserted by a processor or another M9300 terminator at the beginning of the bus, thereby causing the SACK assertion. This is verified by the fact that NAND gate E8, pin 13 is enabled to allow the BUS NPG signal to assert BUS SACK.

If jumpers W1 and W2 are erroneously cut, the M9300 would function abnormally. To prevent this condition from occurring, both jumpers are applied to NAND gate E8, pin 10. If both jumpers are cut, E8, pin 10 is driven low causing a light-emitting diode to illuminate. This immediately indicates an illegal jumper configuration for maintenance purposes.

NOTE

If all three jumpers are in, the M9300 logic is bypassed and only the terminating resistors are utilized.

5.25 G727 GRANT CONTINUITY MODULE

If there are no small peripheral controllers installed in slots C7 through F7, C8 through F8, and C9 through F9, G727 Grant Continuity modules must be installed in slot D7, D8, or D9. These modules merely continue the BUS GRANT signals to the next device on the Unibus.

5.26 M688 POWER FAIL DRIVER

The M688 Power Fail driver is a single-height module which receives power fail signals from the power supply and asserts them on the Unibus. If Unibus B is utilized as a second bus, an additional M688 is required to assert power fail signals on this bus. Figure 5-5 is the M688 Power Fail module schematic. AND-NOR gates E1, pin 8 and E4, pin 8 and the associated inverters are not used in the RH11.

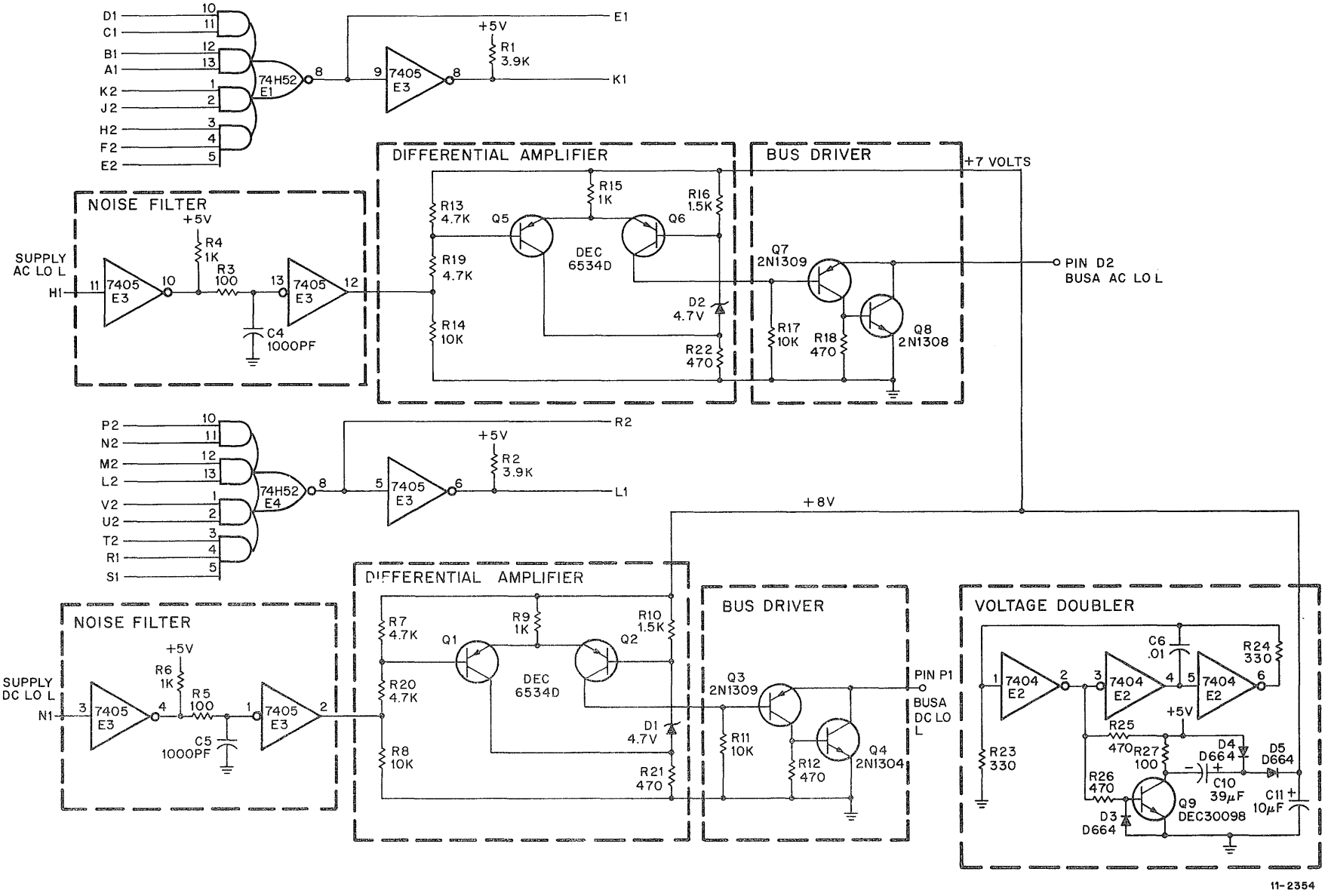


Figure 5-5 UNIBUS Power Fail Drivers Schematic

The schematic shows a noise filter, differential amplifier, and bus driver for two power fail input sources. Pin H1 is connected to the ac power fail line, and pin N1 is connected to the dc power line. When the input at pin H1 or N1 goes low, the output at pin D2 or P1, respectively, goes low. The input power fail signal is applied to a differential amplifier via the noise filter. The differential amplifier increases the voltage swing of 3 V (0 to 3 V) to 5 V (0 to 5 V), which is the voltage required to operate the bus driver. This circuit provides the drive necessary to supply the signal to the Unibus. The voltage doubler circuit increases the +5 V input to 8 V. This voltage is necessary to generate the +5 V required at the input to the bus driver circuit.

5.27 M5904 MASSBUS TRANSCEIVER MODULE

The M5904 Massbus Transceiver module contains nine differential driver chips (75113) and seven differential receiver chips (75107B). Each driver chip and each receiver chip is capable of carrying two signals. Thus, the chips can be designated dual drivers and dual differential receivers. The transmission line connected to the transceivers are bidirectional in that they can both receive and transmit information. This is illustrated for one signal line in Figure 5-6.

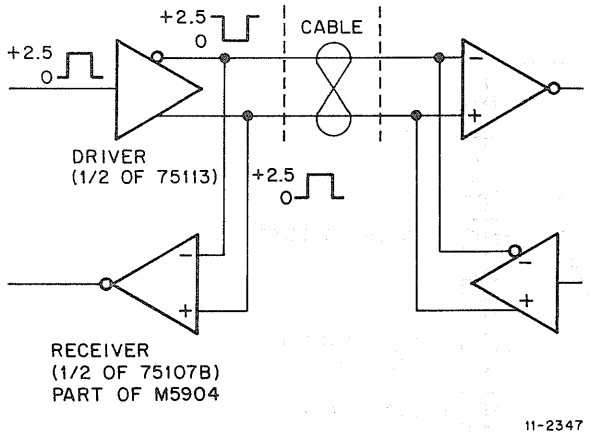


Figure 5-6 Typical Differential Driver/Receiver Connection

The advantage of differential circuitry is that any noise picked up is generally picked up on both the inverted and non-inverted signal lines. The differential receiver takes the difference between the signals regardless of the noise level, and the noise is effectively cancelled out.

Each driver on the M5904 must be terminated since the M5904 is used to drive transmission lines (Figure 5-7).

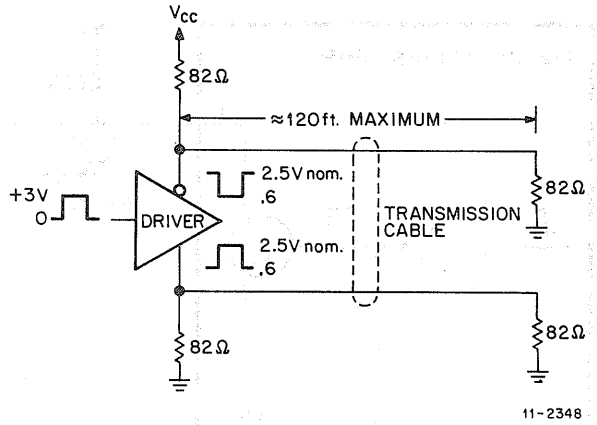


Figure 5-7 Driver Termination

The M5904 Massbus Transceiver requires input voltages of +5 Vdc and -15 Vdc. The dual drivers require +5 Vdc operating voltage while the dual differential receivers require +5 Vdc and -5 Vdc. The -5 Vdc is obtained from the -15 Vdc source via a resistor and Zener diode network.

5.27.1 75113 Dual Differential Driver Chip

The 75113 Tri-state Dual Differential Driver Chips provide differential outputs with high current capability in order to drive balanced lines. The chips feature a high output impedance making it possible to connect many drivers on the same transmission line. A simplified schematic of the 75113 is shown in Figure 5-8.

The inverting output of the driver chip is the transistor collector, while the non-inverting output is the transistor emitter shown at point B. When the input is low, neither transistor conducts and line A is biased to +2.5 V while line B is biased to 0 V by the terminator resistors (refer to diagram). When the input is high, the upper transistor collector is driven low (0 V) and the lower transistor emitter is driven high (+2.5 V). The pin connection diagram for the dual differential driver is shown in Figure 5-9.

5.27.2 75107B Dual Differential Line Receiver Chips

The 75107B Differential Receiver Chips feature dual independent channels with common voltage supply and ground terminals. The circuits operate as follows. If the voltage at pin 1 is positive with respect to the voltage at pin 2, the output at pin 4 goes positive (Figure 5-10).

If the voltage at pin 1 is negative with respect to pin 2, the output at pin 4 goes negative. The pin connection diagram for the receiver is shown in Figure 5-11.

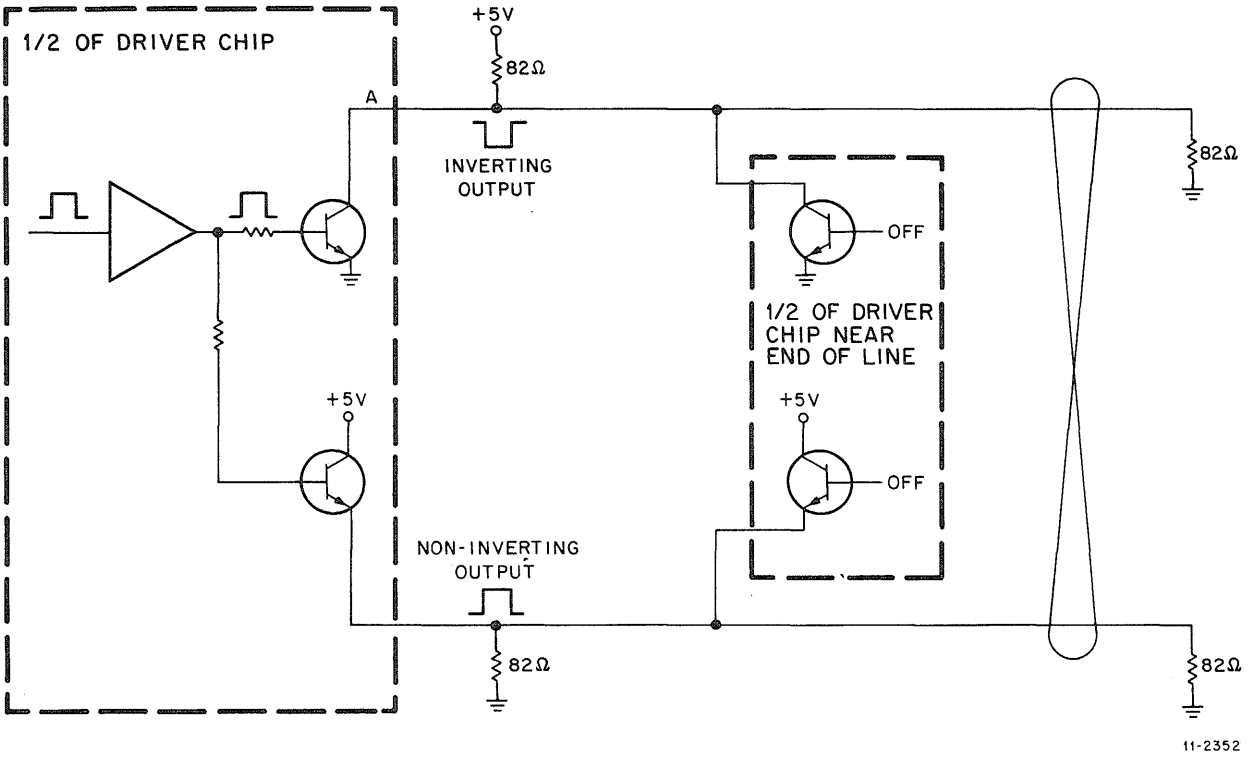


Figure 5-8 Driver Chip Simplified Schematic

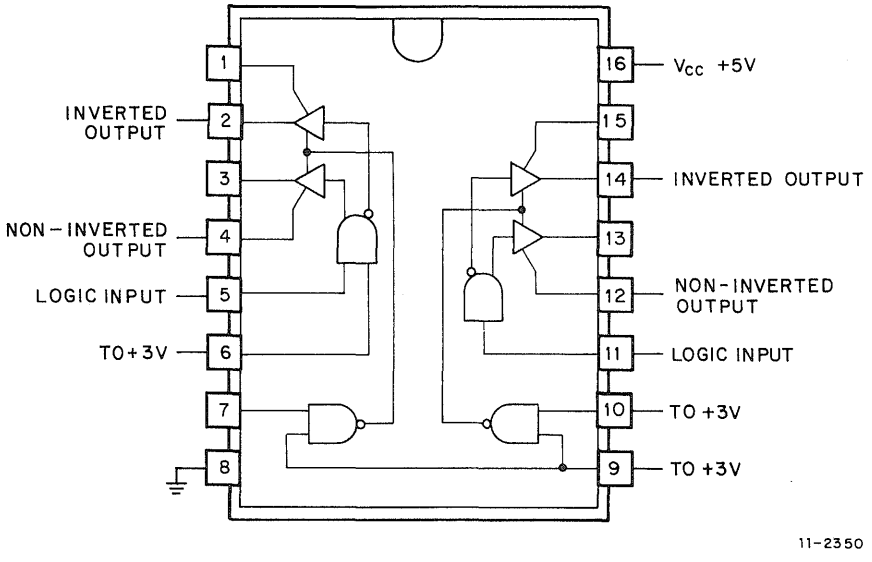


Figure 5-9 Dual Differential Driver Pin Connection Diagram

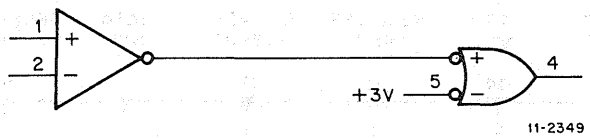


Figure 5-10 Simplified Line Receiver Logic Diagram

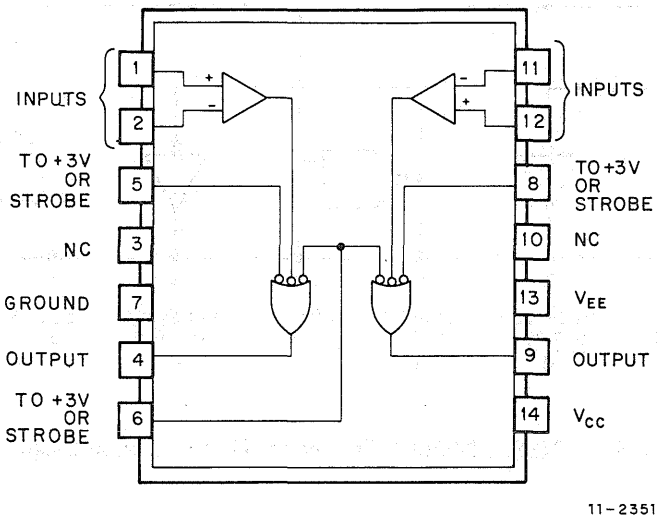


Figure 5-11 75107B Differential Receiver Pin Connection Diagram

5.28 H870 TERMINATOR

The H870 Bus Terminator provides a simple and reliable method of terminating the Massbus. The Massbus is terminated by plugging H870 terminators into each M5903 transceiver module in the last drive.

The H870 consists of 38 82Ω, 1/4 watt resistors wired between each Massbus line and a common ground connection.

NOTE

The H870 Terminators are to be installed on the M5903 transceiver module with the resistors facing up.

5.29 M8838 UNIBUS TRANSCEIVER MODULE

The M8838 Unibus Transceiver module drives and receives signals on the Unibus. The module is a quad chip consisting of four Unibus drivers with common enables on pins 7 and 9 and four receivers which are always enabled. The pin connection diagram is shown in Figure 5-12.

5.30 UNIBUS TERMINATION

The terminating resistors for the Unibus comprise voltage divider networks necessary to properly terminate the Unibus. These resistors are similar to the terminating resistors on the M930 standard Unibus Terminator module.

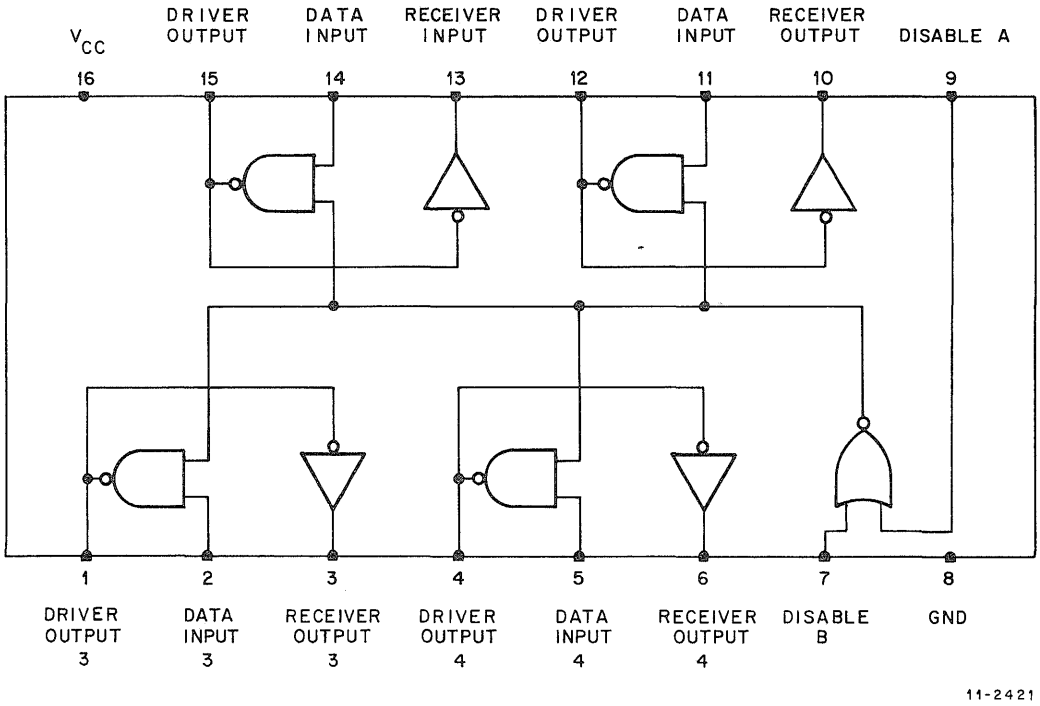


Figure 5-12 M8838 UNIBUS Transceiver Pin Connection Diagram

CHAPTER 6
INSTALLATION AND MAINTENANCE

6.1 INTRODUCTION

This chapter describes the necessary installation information required to install the RH11 as a Unibus device. The chapter also describes the preventive and corrective maintenance procedures that apply to the RH11 when connected to an RS04 or RS03 disk drive. A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the RH11.

This knowledge, plus the maintenance information contained in the *RS03 DECdisk Service Manual* and in the *RS04 DECdisk Service Manual*, will assist the maintenance personnel in isolating system malfunctions.

6.2 INSTALLATION

The following paragraphs describe the mechanical and electrical installation, power checks, jumper configurations, visual inspection, and diagnostics associated with the RH11.

6.2.1 Mechanical

The RH11 uses two hex-height modules and must be installed in a mounting box that accommodates hex-height modules. The modules are inserted in a double-system unit backplane which is installed in the mounting box with four thumbscrews. The double-system unit is oriented with the bus cable slots in line with the other options.

6.2.2 Electrical

Electrical installation describes the power cable connections, Unibus cable connections, and Massbus cable connections.

6.2.2.1 Power Cable Connections – Power is distributed to the RH11 modules via two power cables which attach to the printed circuit backplane assembly by quick-disconnect tabs (refer to RH11 Wired Assembly Drawing D-AD-7009397-0-0). The power cables have Mate-N-Lok connectors on one end, which connect to the Power Distribution Panel located above the backplane, and quick-disconnect tabs on the other end, which connect to the printed circuit backplane. The following chart shows the color codes associated with the power harness connections.

Red	+5 Vdc
Black	Gnd
Blue	-15 Vdc
Gray	+15 Vdc
Violet	DC LO (+3 V to +5 V)
Yellow	AC LO (+3 V to +5 V)
Brown	LTC 8 V pk-to-pk ac

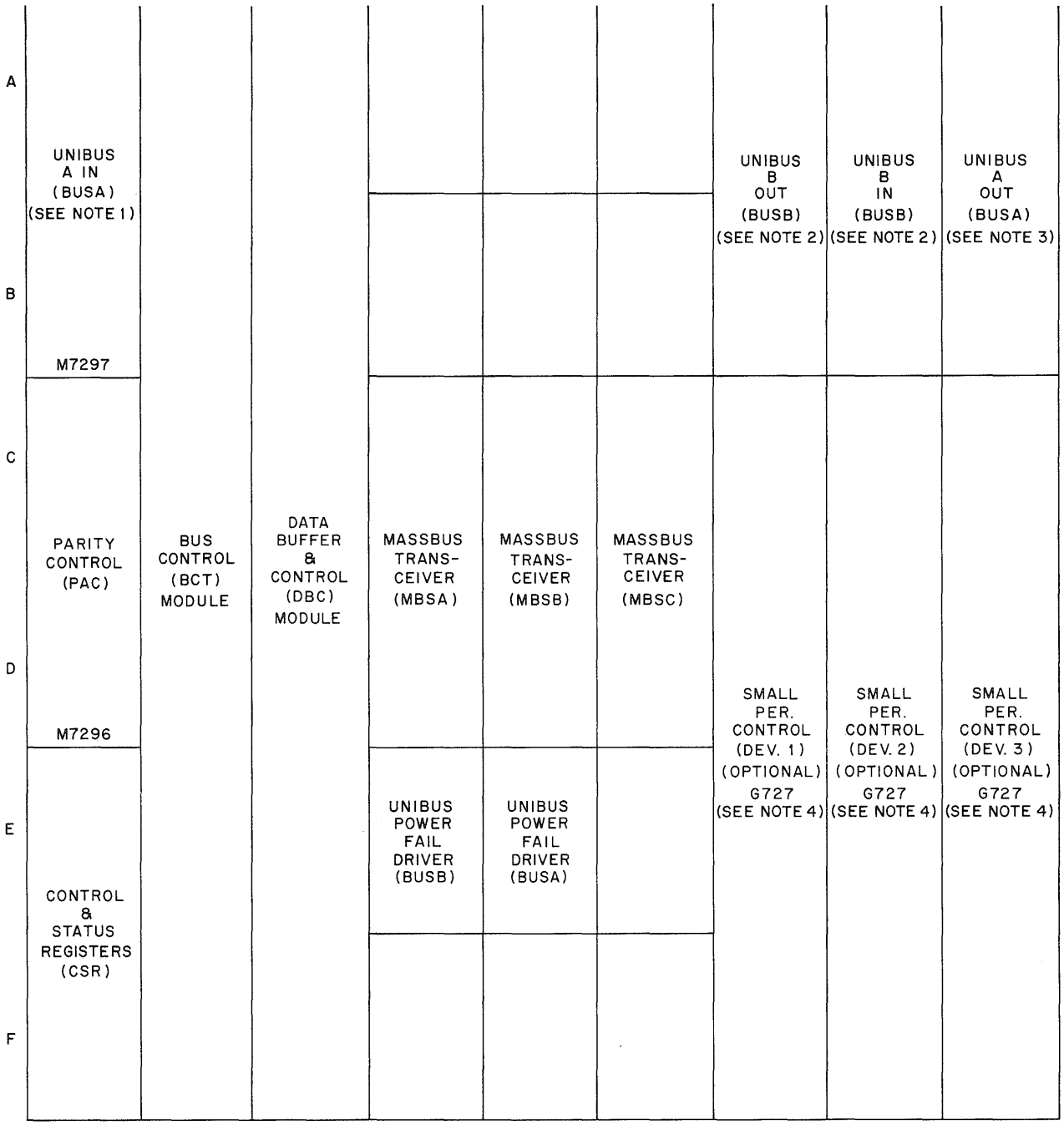
CAUTION

When connecting the power cables to the backplane, ensure that backplane wires are not damaged. Also, *do not cut* AC LO and DC LO wires out of the power harness as they are used for power fail conditions on the Massbus and on both Unibus A and Unibus B ports.

After power connections have been made, check for power shorts with an ohmmeter. Ensure that all modules are firmly seated in the proper slots (Figure 6-1). Power up the cabinet and measure voltages in accordance with values listed in color code chart for power connections. After this is accomplished, turn power off.

6.2.2.2 Unibus Cable Connections – The RH11 is a two-port Unibus device capable of accepting two Unibus cable systems, designated Unibus A and Unibus B.

Unibus A Connections – The Unibus A cable slots connect the RH11 to the processor controlling it. The Unibus A cable enters the RH11 via slot A1, B1 and connects to the next device via slot A9, B9 (refer to Module Utilization Drawing D-MU-RH11-0-01).



NOTES:

1. MAY BE EITHER M920 (CONNECTION FROM ADJACENT DEVICE) OR BC11A CABLE (CONNECTION FROM ANOTHER BOX OR NON-ADJACENT DEVICE).
2. MAY BE M9300 (TERMINATION AT BEGINNING OR END OF UNIBUS B) OR BC11A CABLE (CONNECTION TO OTHER BUS B DEVICES).
3. MAY BE M920 (CONNECTION TO ADJACENT DEVICE), M930 (TERMINATION AT END OF UNIBUS A), OR BC11A CABLE (CONNECTION TO NEXT BOX OR NON-ADJACENT DEVICE).
4. THE SMALL PERIPHERAL CONTROLLER SLOTS MAY CONTAIN A VARIETY OF PDP-11 OPTIONS. THE OPTION MAY CONSIST OF A SINGLE QUAD MODULE BOARD (SLOTS C, D, E, & F) OR A DOUBLE HEIGHT CONTROLLER BOARD (SLOTS C & D) WITH AN M105 ADDRESS SELECTOR MODULE (SLOT E) AND AN M7821 INTERRUPT CONTROL MODULE (SLOT F).
5. IF NO OPTION IS PRESENT IN THE SMALL PERIPHERAL CONTROLLER SLOTS, G727 GRANT CONTINUITY MODULE(S) MUST BE INSERTED IN SLOTS D.

11-2384

Figure 6-1 RH11 Module Utilization

Connections to slot A1, B1 are made via the BC11A Unibus cable if the RH11 is the first Unibus A device in the mounting box. Otherwise, connection to A1, B1 from the preceding device is made by an M920 Unibus Jumper module. Connection to the next adjacent device on the Unibus is made via the M920 Unibus Jumper module, or is made by BC11A cable if the device is not adjacent.

NOTE

If the RH11 is the last device on Unibus A, an M930 Terminator module is installed in slot A9, B9.

Unibus B Connections – Unibus B connections are generally made in systems with multiport memories. When the Unibus B port of the RH11 is not used, an M9300 Terminator module (with jumper W1 cut) should be installed in slot A8, B8 to terminate Unibus B signals into the RH11. The second M9300 Terminator module should *not* be used in order to conserve power consumption. If the Unibus B port of the RH11 is used, connections are determined on the basis of whether a processor is connected to Unibus B. These connections are described below.

a. Processor on Unibus B – If a processor is connected to Unibus B, it is electrically connected at the beginning of the bus. In this case, the M930 Terminator modules supplied with the processor are used for bus termination, and the two M9300 Unibus B Terminator modules supplied with the RH11 are not used.

NOTE

The M9300 Terminator may be used as a substitute for the M930 Terminator if the jumpers are selected correctly.

The Unibus B cable connection to the RH11 is made via slot A8, B8 with a BC11A cable. Connection from the RH11 to the next device is made via BC11A cable connected to slot A7, B7. If the RH11 is the last device on the bus, the M930 or M9300 Terminator is installed in slot A7, B7 instead of the BC11A cable.

b. No Processor on Unibus B – If no processor is connected to Unibus B, a M9300 Unibus B Terminator module must be selected as an NPR arbitrator. If one RH11 is connected to Unibus B, the RH11 is electrically connected at at the beginning of the bus with the M9300 selected to act as an NPR arbitrator. One M9300 Unibus B Terminator module is placed in slot A8, B8 of the RH11. Jumper W1 on this module must be cut to enable the arbitration logic. Connection to other devices on Unibus B, such as memory, are made via BC11A cable connected to slot A7, B7. The second M9300 Unibus B Terminator module is installed in the last device on Unibus B. Jumper W2 is removed for terminating the Unibus with no processor connected.

NOTE

In this case, an M930 Terminator module can be substituted for the M9300 Unibus B Terminator in the last device slot. If more than one RH11 is installed, the user may have extra M9300 modules as a result of a particular configuration. Figures 6-2, 6-3, and 6-4 show typical Unibus configurations.

6.2.2.3 **Massbus Cables** – Massbus connections to the RH11 are made via three 40-conductor ribbon cables. These cables plug into three M5904 Transceivers in the RH11 and are designated Massbus Cable A, Massbus Cable B, and Massbus Cable C. The connections are made as shown below:

Massbus Cable A – Install in M5904 module in slot C4, D4.

Massbus Cable B – Install in M5904 module in slot C5, D5.

Massbus Cable C – Install in M5904 module in slot C6, D6.

The Massbus cables are marked and should be inserted with the edge-marking facing the module handles. To terminate the Massbus, three H870 modules (Massbus Transceivers and Terminators) supplied with the RH11 should be plugged into the M5903 modules located in the last drive on the Massbus in place of the M5903 modules (Figure 6-5).

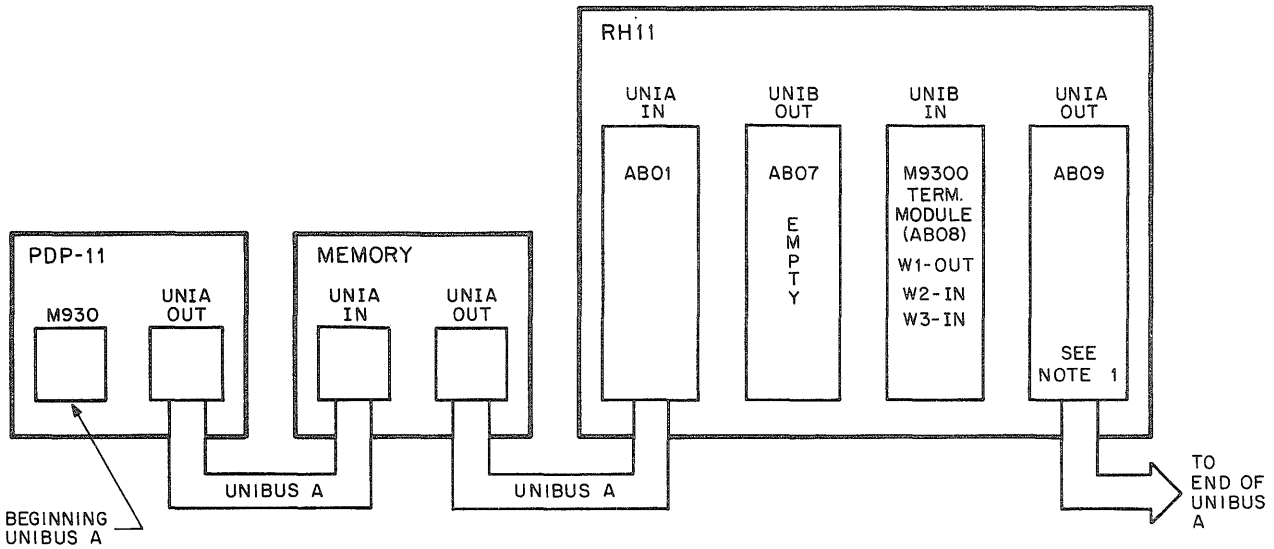


Figure 6-2 Single Port UNIBUS Configuration

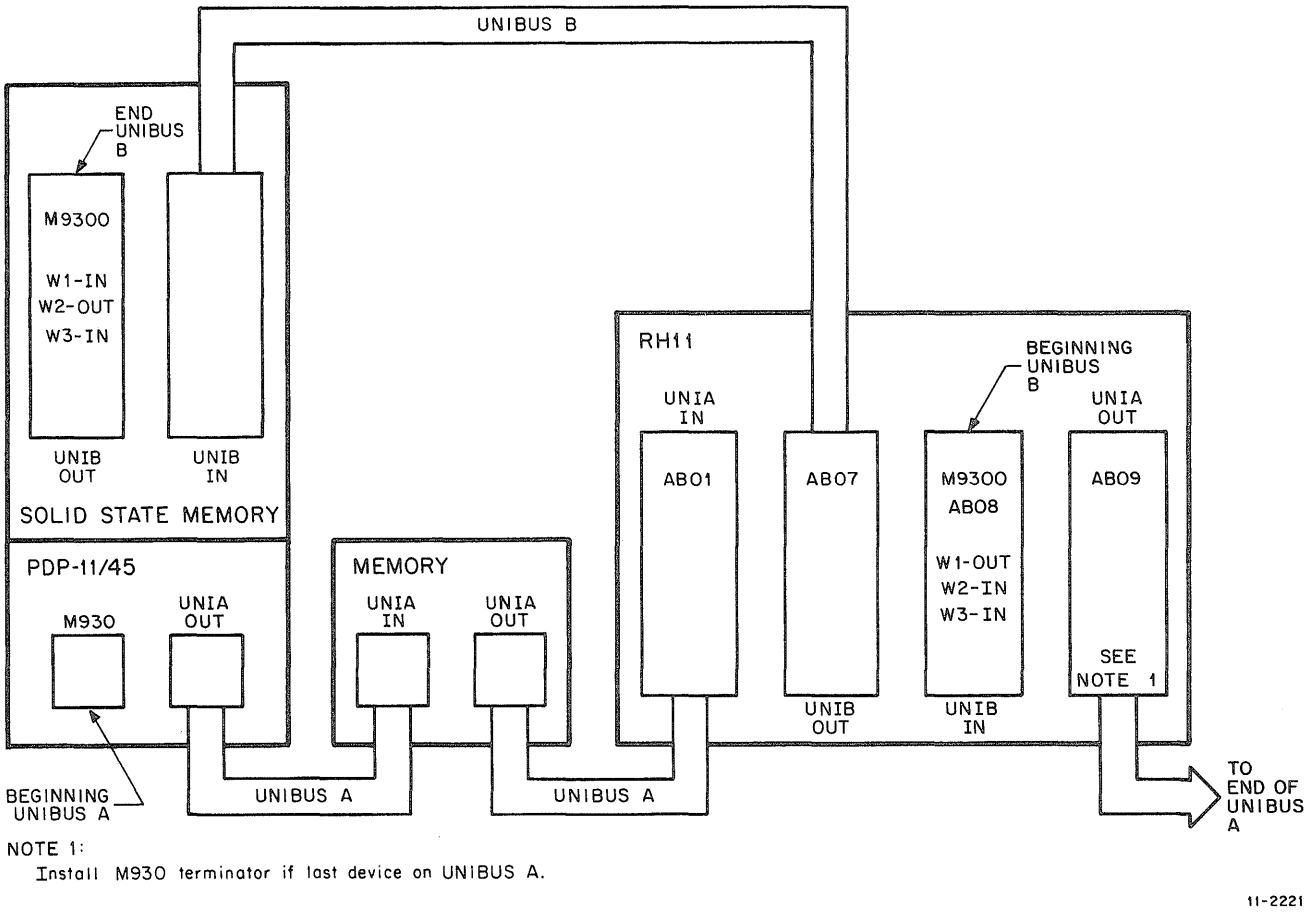


Figure 6-3 Dual Port Configuration – Memory on UNIBUS B

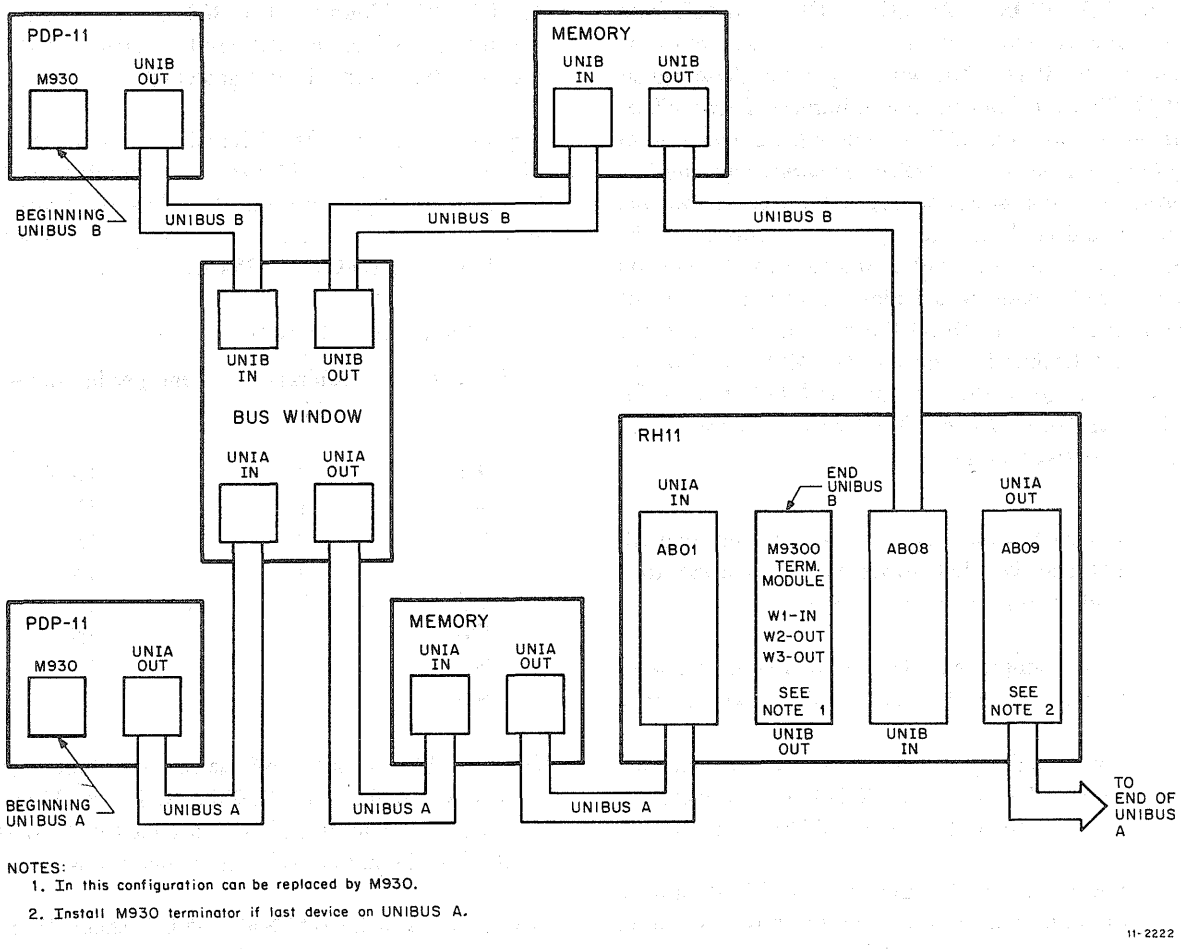


Figure 6-4 Dual Port Configuration – Memory & Processor on UNIBUS B

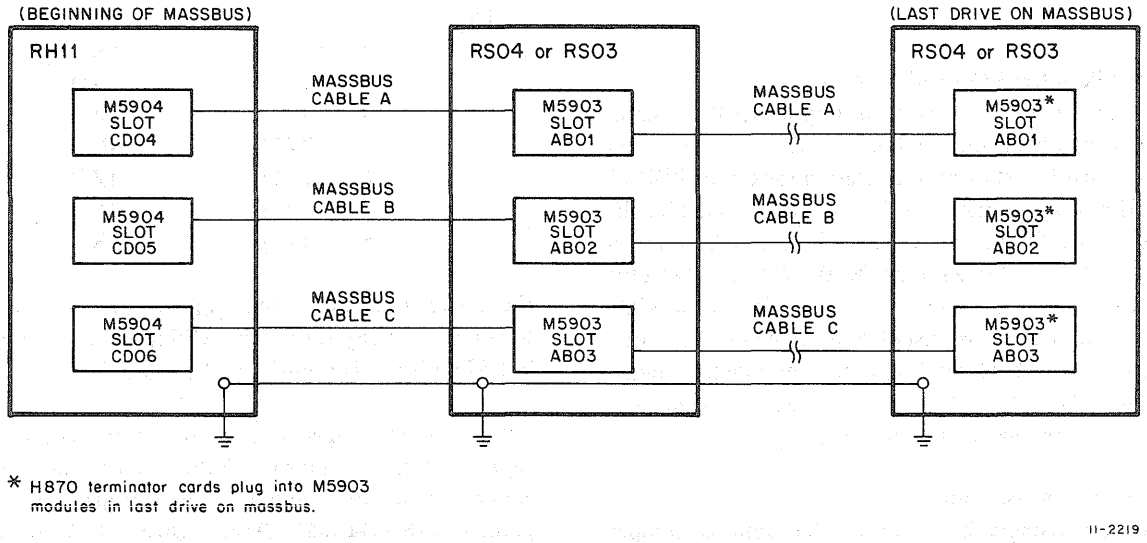


Figure 6-5 MASSBUS Cable System Configuration

6.2.2.4 **AC LO, DC LO** – AC LO and DC LO signals from the power supply which supplies RH11 power must be connected to the RH11. The wires supplying these signals WILL NOT BE CUT from the power harness. *There will be only one AC LO and one DC LO power fail connection to each Unibus for devices mounted in the same mounting box and sharing the same power supply.* Otherwise, power fail conditions would latch up due to positive feedback to the power fail logic. If a power fail connection for AC LO and DC LO is already made to a Unibus from a device in the same mounting box, the M688 Power Fail module in the RH11 for that Unibus is removed. The M688 module for Unibus A is located in slot E5 and the M688 module for Unibus B is located in slot E4. The following is a summary of power fail configuration rules.

1. For each mounting box, there is only one AC LO and DC LO power fail connection to a Unibus from the power supply.

2. Power supply AC LO and DC LO must always be wired to each RH11 via the power harness.

3. Power fail signals may only be disconnected from a Unibus in an RH11 by removing the appropriate M688 Power Fail Driver module.

4. Power supply AC LO and DC LO should be disconnected from all other options mounted in the same box as the RH11 if they do not need those signals for internal operation.

Figures 6-6, 6-7, and 6-8 show three typical power fail configurations which are configured in accordance with the above mentioned rules.

6.2.3 Small Peripheral Controller Slots

The RH11 provides space for mounting up to three small peripheral controllers on Unibus A. These three small peripheral controller slots may contain a variety of PDP-11 options. The option may consist of single quad-height boards (slots C, D, E, and F) or double-height control boards (slots C and D) with an M105 Address Selector module (slot E) and an M7821 Interrupt Control module (slot F). If no option is installed in a small peripheral controller slot, a G727 Grant Continuity module is installed in empty slots D7, D8 and/or D9 to jumper the Unibus A bus grant lines through the unused option space.

6.2.4 Jumper Configurations

The following paragraphs describe the various jumper configurations on the BCT (M7295), DBC (M7294) and the CSR (M7296) modules.

6.2.4.1 **BCT Module** – The BCT module contains jumpers for register selection, BR level interrupt, NPR latency, vector address, and missed transfer error.

Register Selection – The RH11 is capable of responding to 30 possible Unibus addresses. The number of addresses, however, is dependent on the Massbus device. For the RS04/RS03 drives, the following jumper configuration should be used (D-CS-M7295-0-1, sheet 2).

Jumper in = binary 0

Jumper	Address Bit	Jumper In/Jumper Out
W1	12	OUT
W2	11	IN
W3	10	OUT
W4	9	IN
W5	8	IN
W6	7	IN
W7	6	IN
W8	5	OUT

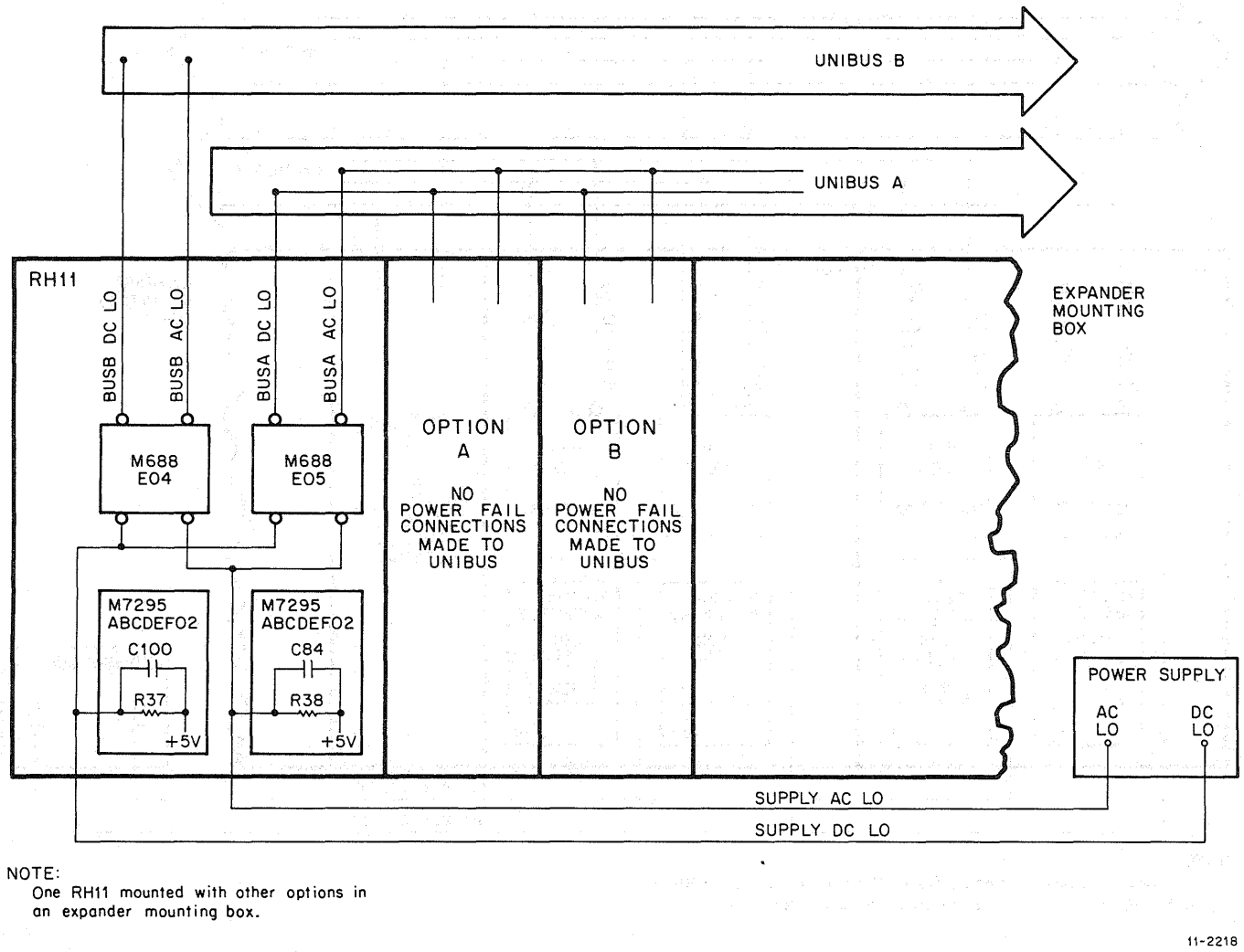
Jumpers W1 through W8 select the block of Unibus addresses that the RH11/RS04 or RH11/RS03 responds to. The standard addressing block assigned is 772040 through 772066. If the jumper is left in, a binary 0 is encoded.

The jumpers in E3 (D-CS-M7295-0-1, sheet 2) are selected for the appropriate number of registers (12) in the RH11/RS04 or RH11/RS03 system.

Slot	Jumper	Jumper In/Jumper Out
E3	1 – 16	IN
	2 – 15	IN
	3 – 14	OUT
	4 – 13	OUT
	5 – 12 (2)	IN
	6 – 11 (4)	OUT
	7 – 10 (8)	OUT
	8 – 9 (16)	IN

BR Level Interrupt – The priority jumper plug for the RH11 is normally set for the BR5 level. This plug is located in E57 (refer to D-CS-M7295-0-1, sheet 7).

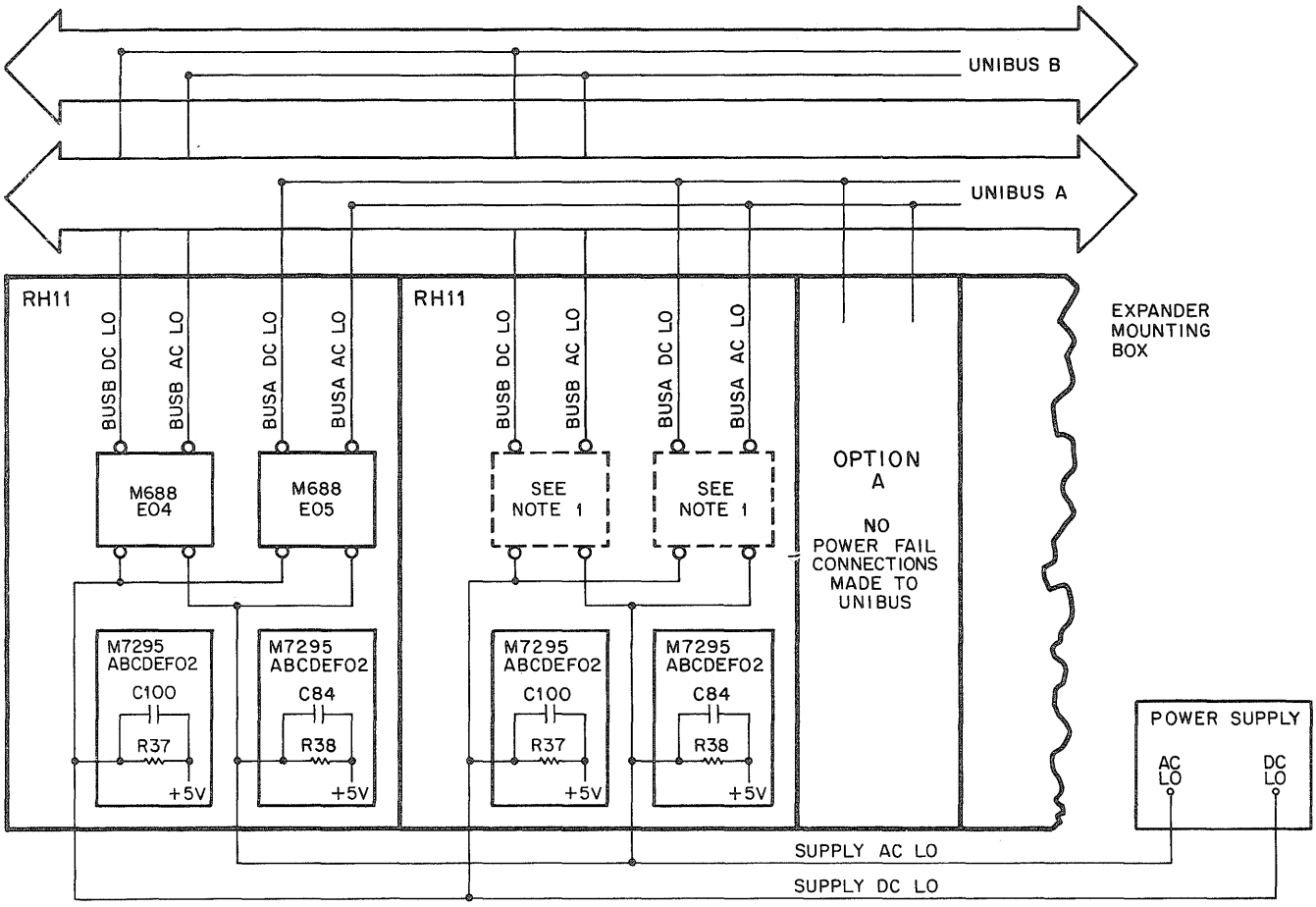
NPR Latency – Special circuitry is incorporated on the BCT module to improve NPR latency time for devices connected to the Unibus. This circuitry is enabled via jumper W18 (D-CS-M7295-0-1, sheet 7). When the jumper is left in, the NPR latency feature is enabled. Not all PDP-11 processors will work with this special feature.



NOTE:
One RH11 mounted with other options in an expander mounting box.

11-2218

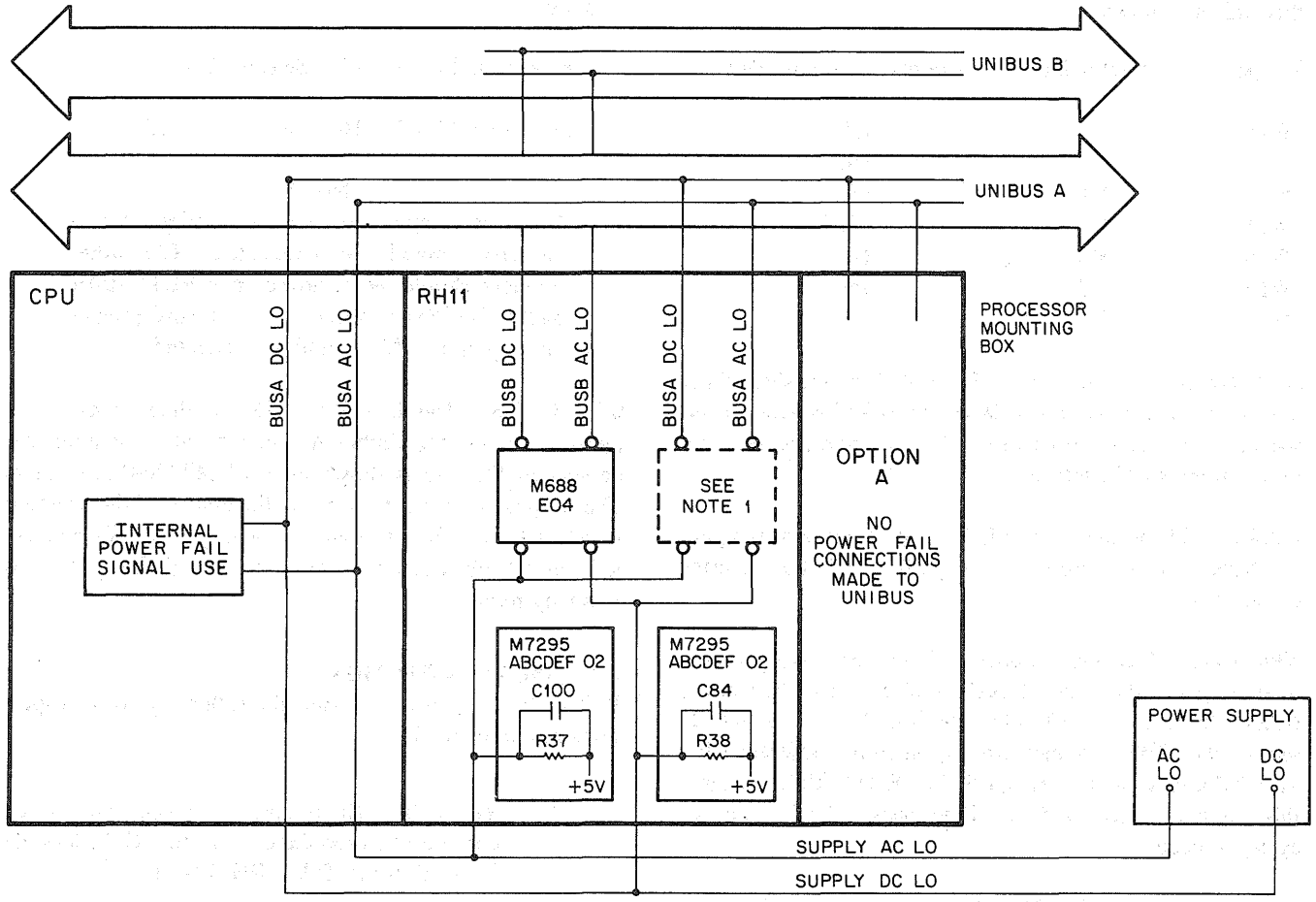
Figure 6-6 Typical Power Fail Configuration for RH11 & Options Mounted in Same Expander Box



NOTE 1:
Disconnect power fail signals from BUSA by removing M688 in slot E05 & from BUSB by removing M688 in slot E04.

11-2216

Figure 6-7 Typical Power Fail Configuration for Two RH11s Mounted in Same Expander Box



NOTE 1
Disconnect power fail signals from BUSA by removing M688 in slot E05.

11-2217

Figure 6-8 Typical Power Fail Configuration for RH11 and CPU Mounted in Processor Box

Vector Address Jumpers – The interrupt vector transferred to the processor is jumper selectable via jumpers W11 through W17, representing vector bits 2 through 8, respectively. When a jumper is left in, a binary 1 is encoded. The RH11/RS04 and RH11/RS03 systems have been assigned a vector address of 000204. The jumper configuration for this address follows:

Jumper	Vector Bits	Jumper In/Jumper Out
W11	V2	IN
W12	V3	OUT
W13	V4	OUT
W14	V5	OUT
W15	V6	OUT
W16	V7	IN
W17	V8	OUT

MXF Jumper – Jumper W19 (D-CS-M7295-0-1, sheet 9) is used to disable detection of MXF errors and is used during special maintenance procedures. Normal operation requires that jumper W19 be left in.

6.2.4.2 **DBC Module** – The DBC module contains jumpers for NPR cycle selection, Unibus parity, and start counter capacities.

NPR Cycle Selection Jumpers – There are two jumpers used to select the type of cycle implemented when doing NPRs. Jumper E66 (3–14) (D-CS-M7294-0-1, sheet 2) selects the RH11 to perform one memory reference for each NPR request. In RH11/RS04 or RH11/RS03 systems, this jumper is removed to allow back-to-back memory cycles to occur.

Jumper E66 (2–15) (D-CS-M7294-0-1, sheet 2) takes advantage of dedicated Unibus B systems by allowing the RH11 to transfer complete consecutive blocks of data without giving up the Unibus. A dedicated Unibus B system is one in which the RH11 is used exclusively as a Unibus B master. To implement this feature (called BUS HOG mode), the one-cycle jumper and E66 (2–15) must be cut.

Unibus Parity Jumpers – The RH11 option can be selected for 16 data-bit (plus two parity bits) transfers or 18 data-bit transfers. Unibus A and Unibus B can each be selected individually via jumpers W1 and W2 (D-CS-M7294-0-1, sheet 8). Jumper W1, if left in, allows parity error code detection on Unibus A when the RH11 is doing DATI operations. If jumper W1 is removed, the Unibus A PA and PB parity lines are used as data bits 16 and 17, respectively. Jumper W2 serves the same function for Unibus B as jumper W1 does for Unibus A. The jumpers are normally left in.

Start Counter Jumpers – Different Silo fill capacities are jumper selectable before starting a write operation onto the disk drive. The jumper selections are listed below (D-CS-M7294-0-1, sheet 9):

Jumper E66, Pins 1 – 16 – Selects full capacity of 64 words.

Jumper E66, Pins 5 – 12 – Selects 32 words.

Jumper E66, Pins 7 – 10 – Selects 16 words.

NOTE

Only the jumper representing the desired Silo capacity should be connected. The other jumpers should be removed. For RH11/RS04 and RH11/RS03 systems, the 64-word jumper (E66, pins 1 – 16) should be connected.

6.2.4.3 **CSR Module** – The CSR module contains a jumper to allow for Unibus A selection only. The jumper is designated W1 and is shown on D-CS-M7296-0-1, sheet 2. The purpose of W1 is to override the ability of the program to select Unibus B data transfers; with jumper W1 connected, only Unibus A operations are allowed. The jumper is normally removed.

6.3 VISUAL INSPECTION

Before the diagnostics are run, the following visual inspections should be made.

1. Verify that all modules have been configured correctly in accordance with the RH11 Module Utilization List D-MU-RH11-0-01.
2. Ensure that all modules are firmly seated in the system backplane assembly.
3. Inspect backplane wiring for broken wires or damaged pins. Repair or replace as required.
4. Ensure that the power cable is firmly attached to the Fast-on tabs on the system backplane assembly and that the Mate-N-Lok connector is seated firmly in the power distribution panel on the chassis.
5. Clean air filters at top of cabinet.
6. Ensure that all Unibus and Massbus cables are properly terminated and are firmly seated.
7. Check cabinet fans for proper operation.

6.4 RS04/RS03 ADD-ON INSTALLATION PROCEDURE

This paragraph provides Field Service with the proper installation procedure for the RS04/RS03 disk unit added to PDP-11 systems. If the installation is not a field add-on, this procedure may be used as a check list to validate the originally configured subsystem. The following steps outline the procedure for unpacking, inspecting, and mounting the drive.

1. Open the RS04/RS03 shipping container and examine the drive for shipping damage.

2. Remove the disk from the container and place it on a flat surface with the top surface up. The RS04/RS03 is designed to be slide mounted in a standard DEC 19-in. rack, containing an 861 Power Control and cabinet stabilizers.

3. Remove the rack slide sections from the side of the disk by sliding them completely forward. Do not unscrew the slide sections which are mounted to the disk cabinet sides.

4. Refer to the RS04/RS03 configuration drawings located in the RJS04 or RJS03 print set.

5. Insert the snap-on 10-32 Tinnerman nuts (90-07786) into the proper hole positions as indicated on the configuration drawing by "A" numbers and attach the rack slides.

   Upper drive – Holes 87–84 from bottom.
   Middle drive – Holes 60–57 from bottom.
   Bottom drive – Holes 33–30 from bottom.

   NOTE

   DO NOT attempt to lift the RS04/RS03 by yourself. Two persons are needed.

6. Pick up the RS04/RS03 and slide it into the chassis slides just mounted. Slide the unit fully to the rear, making sure that all slides seat properly and interlock.

7. Extend the unit to its full out position on the slides. A lock click should be heard when the unit is fully extended.

   NOTE

   DO NOT APPLY POWER to the unit. The motor lock must be removed before power is applied.

8. Motor Lock

   a. After repeating step 7 above, remove the bottom chassis cover.

   b. Remove the motor lock, turn it 180° around, and secure it back into position with the brushes around the spindle shaft. The metal protection plate should be covering the brushes so that the brushes cannot be seen when viewing from the bottom.

9. Massbus Cable Connections

   a. Steps 8 and 9 must be completed before connecting cables. Refer to the RS04/RS03 Massbus cabling diagram in the RJS04 or RJS03 print set.

   b. Remove the two Massbus cable restraints from the lower right rear corner of the drive.

   c. Route the three incoming Massbus ribbon cables marked Massbus A, B, and C through the right (viewed from the rear of the unit) cable clamp to the M5903 module area.

   d. Connect each cable to the proper module via the 3M connectors. Note that the connectors are keyed, and only can be plugged in one way. Use the following table to locate the correct transceiver board.

Module	Slot	Cable
M5903	AB01	Massbus A
M5903	AB02	Massbus B
M5903	AB03	Massbus C

   e. If there are no more drives to be added to the Massbus, the bus must be terminated here. Insert three H870 Miniterminators into the remaining 3M cable connectors, one per M5903 module. (Some systems may contain an M5903YA module as a combined terminator and transceiver for the last drive on the Massbus.)

f. If another drive is to follow, insert three output cables as in step c and dress them out through the rear of the drive via the left cable clamp (viewed from the rear).

g. Secure both cable clamps and replace both covers. Slide the drive into the rack.

10. Power

a. Insert the RS04 power plug into the unswitched side of the 861 Power Control.

b. Connect the incoming remote power cable (3-wire) into J1 of the drive and output remote cable into J2, if applicable.

c. Connect the power sequence jumper into J3 if this is the first drive; otherwise, connect the incoming 4-wire power sequence cable to J3.

d. If this is the last drive or the only drive, no connection is made to J4. Otherwise, a 4-wire sequence cable is output from J4 to J3 of the next drive. Part numbers:

J1, J2 Cable, 3-wire	70-08288
J3 Jumper Plug, 1st device	70-09490
J3, J4 Cable, 4-wire	70-09491

e. Turn SW1 to "REMOTE" and the circuit breaker on. When the CPU is turned on, all drives (if multidrive) will power sequence up, one at a time.

f. The RS04 is now physically mounted. Refer to the RJS04/RJS03 Customer Acceptance Procedures located in the RJS04 or RJS03 Print Set for on site acceptance procedures.

6.5 DIAGNOSTIC MAINTENANCE

The three diagnostic programs described herein are employed with the RH11/RS04 and RH11/RS03 systems. Refer to the applicable diagnostic operating procedures for detailed information. The diagnostic programs listed below may be run independent of the type of drive (RS04 or RS03) configured on the RH11.

6.5.1 Basic Function Test Diagnostic DZRSB

This diagnostic verifies that the RH11 Controller and the RS04 or RS03 drives are operating correctly. The diagnostic can test up to eight drives in any order or in any mixture of RS04 and RS03 drives. The diagnostics determine which type of drive each unit is before testing. The major tests in this diagnostic are:

1. Determining whether all registers can be read from or written into.

2. Checking error conditions by causing an error and observing the results on the associated error bit in the RSCS1 or RSCS2 and RSER registers, and

3. Checking that the Silo can accurately store and transfer data.

6.5.2 Data Reliability Diagnostic DZRSC

This diagnostic checks the ability of the drive to read or write large blocks of data. There are two basic tests – address test and data test.

Address Test – This test writes the sector address in each word in each sector. The diagnostic then reads the drive to ensure that the drive address correlates with the data in that address. This is used as a confidence test.

Data Test – This test completely writes a drive with a specific word pattern and write-checks the drive. The drive is then read, and the data is placed in a buffer where it is compared with the known data from memory. The write-check operation ensures that the data was written on the disk, and the read function ensures that the data can be read from the disk.

6.5.3 Diskless Diagnostic DZRSD

This diagnostic removes all inputs to the digital portion of the drive logic from the disk/analog logic and replaces these inputs with bits of the Maintenance register. This allows both the digital and analog portions of the drive to be checked out separately. In addition, ten important test points in the digital logic may be monitored through the Maintenance register. Since the controller merely passes Maintenance register information in and out of the drive and neither modifies nor monitors this data, all drive functions may be simulated in this mode with the controller in its standard operating configuration. All other drive registers perform exactly as in the normal operating mode.

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTION

A.1 INTRODUCTION

This appendix contains descriptions of some of the integrated circuits used in the RH11. Where applicable, logic diagrams, schematics, and pin connection diagrams are shown.

A.2 3341 64-WORD X 4-BIT SERIAL MEMORY (SILO)

The 3341 Silo Memory operates in a first in/first out mode (FIFO). The output rate is independent of the input rate and asynchronous or synchronous operation can be achieved.

The four data inputs (D0 through D3) are transferred to the first memory location if both the Input Ready (IR) and Shift In (SI) signals are asserted high (see Silo Memory Block Diagram). After 250 ns to allow the data to stabilize, IR goes low. However, data remains in the first memory location until both IR and SI are brought low. At this point, the data propagates to the next memory location, if the location is empty. When the data is transferred, IR goes high, indicating that the device is ready to accept new data. If the memory is full, the IR signal remains unasserted (low).

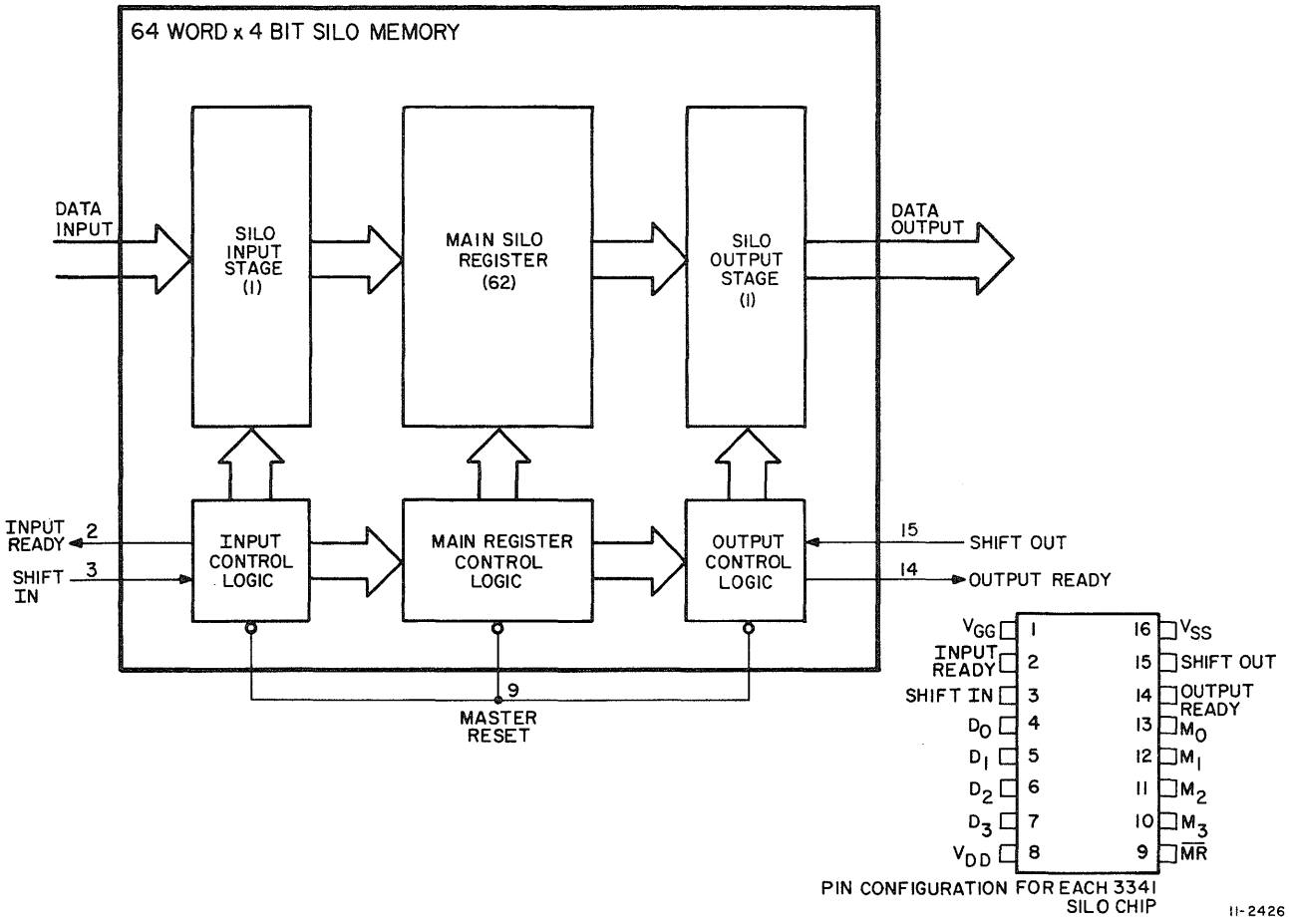
When data enters the second cell, the transfer of any data word from a full cell to the next empty cell is automatic and is activated by an on-chip control. Consequently, data stacks up at the output to the memory while empty locations "bubble" to the input of the memory. The throughput time from input to output of the Silo is from 0 to 32 μs (16 μs typical).

When data has transferred to the last cell in the Silo, OUTPUT READY (OR) is asserted high, indicating that valid data is present at the output pins (M0 through M3 on each chip). Data is not shifted out of the Silo, however, until the OUTPUT READY and SHIFT OUT signals to the Silo are both asserted high. When the data is shifted out, OUTPUT READY goes low. The output data is maintained until both OUTPUT READY and SHIFT OUT go low. At this point, the contents of the previous memory cell (if it is full) are transferred to the output cell, causing OUTPUT READY to be asserted high again. When the Silo memory is emptied, OUTPUT READY stays low.

Table A-1 lists the minimum, typical, and maximum times for the above mentioned signals at 0° C and at 70° C.

Table A-1
Control Signal Timing Specifications

Signal	0°			70°		
	MIN	TYP	MAX	MIN	TYP	MAX
Input Ready High Time	90	300	–	155	300	450
Input Ready Low Time	138	400	–	–	400	520
Data Input Stabilizing Time	–	250	–	–	250	400
Data Output Stabilizing Time	–	250	–	–	250	400
Output Ready High Time	90	250	–	155	250	350
Output Ready Low Time	170	450	–	–	450	650


64 WORD x 4 BIT SILO MEMORY
DATA INPUT
SILO INPUT STAGE (1)
MAIN SILO REGISTER (62)
SILO OUTPUT STAGE (1)
DATA OUTPUT
INPUT READY
2
SHIFT IN
3
INPUT CONTROL LOGIC
MAIN REGISTER CONTROL LOGIC
OUTPUT CONTROL LOGIC
15
SHIFT OUT
14
OUTPUT READY
9
MASTER RESET
VGG 1
INPUT READY 2
SHIFT IN 3
D0 4
D1 5
D2 6
D3 7
VDD 8
16 VSS
15 SHIFT OUT
14 OUTPUT READY
13 M0
12 M1
11 M2
10 M3
9 MR
PIN CONFIGURATION FOR EACH 3341 SILO CHIP
11-2426

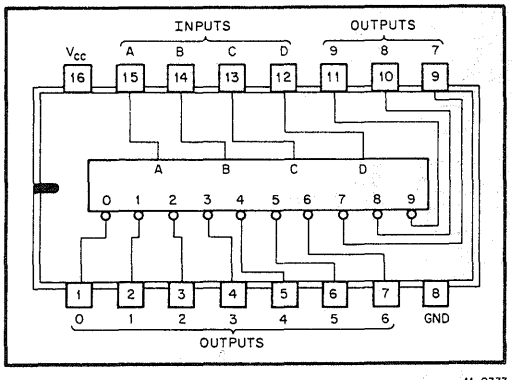
A.3 7442 4-LINE-TO-10-LINE DECODERS (1-of-10)

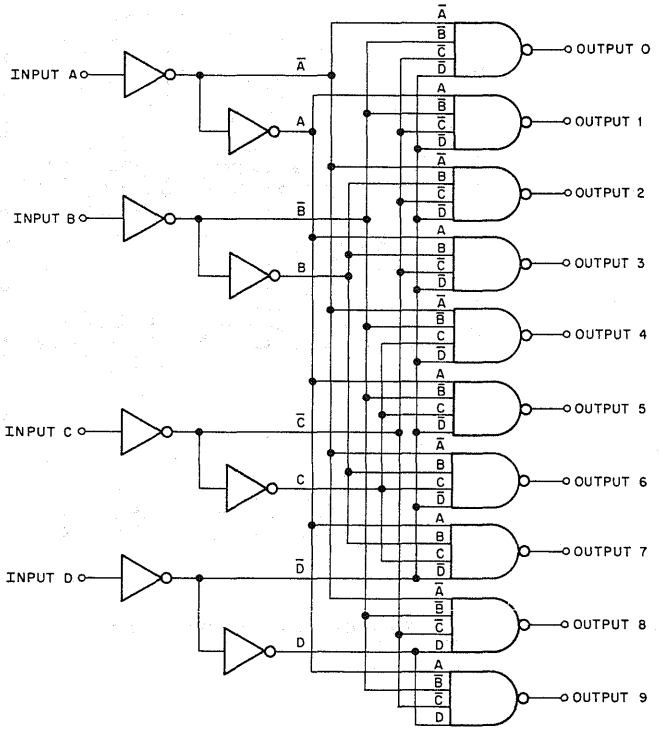
These monolithic decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The 7442 BCD-to-decimal decoder features familiar transistor-transistor-logic (TTL) circuits with inputs and outputs that are compatible for use with other TTL and DTL circuits.

TRUTH TABLES

BCD Input				Decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1





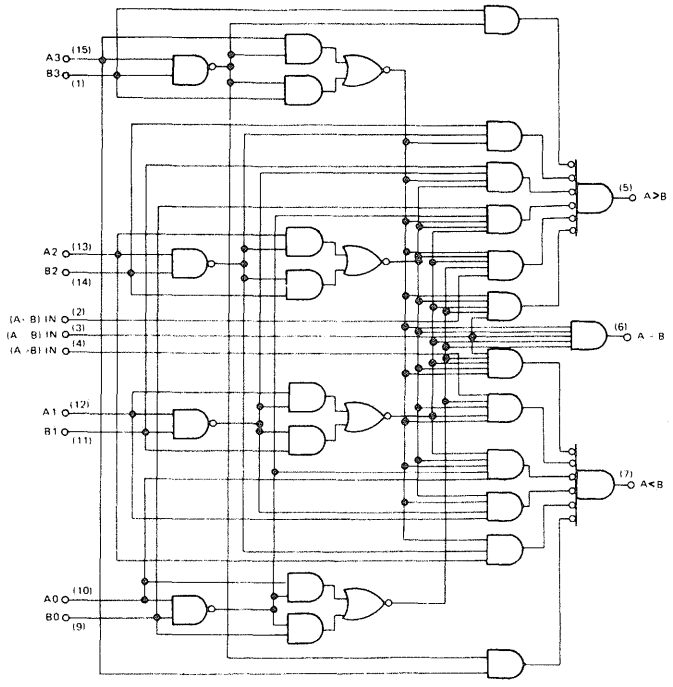
A.4 7485 4-BIT MAGNITUDE COMPARATORS

The 7485 performs magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

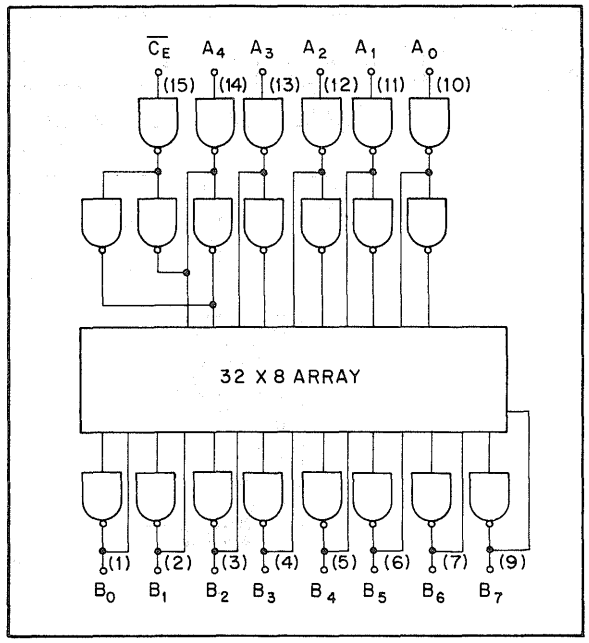
NOTE: H = high level, L = low level, X = irrelevant



Pin (16) = V_{CC}, Pin (8) = GND

A.5 8223 256-BIT BIPOLAR FIELD-PROGRAMMABLE ROM (32 X 8 PROM)

The 8223 is a TTL 256-bit read only memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

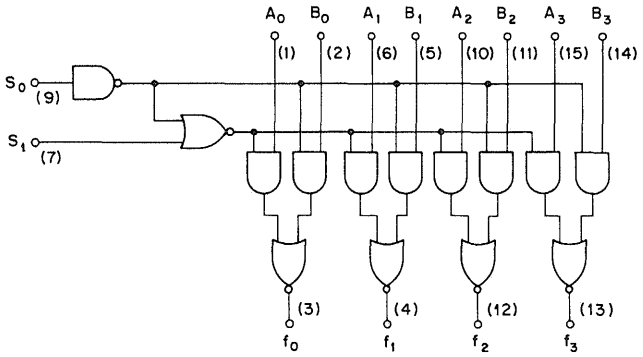


V_{CC} = (16)
GND=(8)
( ) = DENOTES PIN NUMBERS

11-2382

A.6 8234 2-INPUT 4-BIT DIGITAL MULTIPLEXER

This device is a 2-input, 4-bit digital multiplexer designed for general purpose, data selection applications. The 8234 features inverting data paths. The 8234 design has open-collector outputs which permit direct wiring to other open-collector outputs (collector logic).



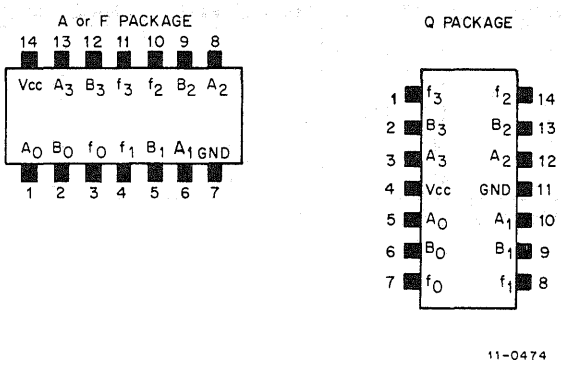
S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

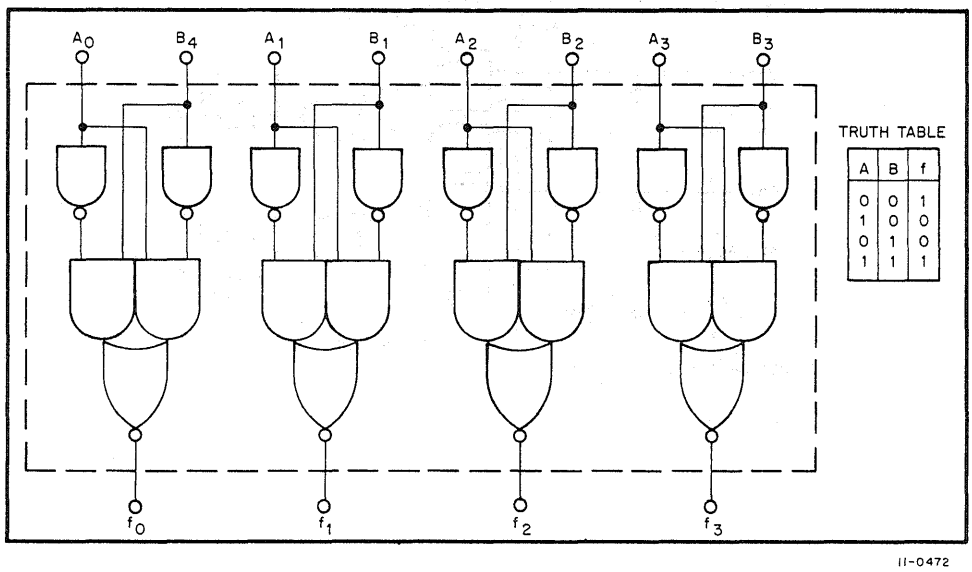
V_{CC} = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

11-2383

A.7 8242 EXCLUSIVE-NOR 4-BIT DIGITAL COMPARATOR

The 8242 digital comparator circuit consists of four independent Exclusive-NOR gates with each gate structure having an open-collector output to permit multiple bit comparisons. A 4-bit comparator network is formed by connecting the independent outputs; such a network is easily expanded by cascading the outputs.



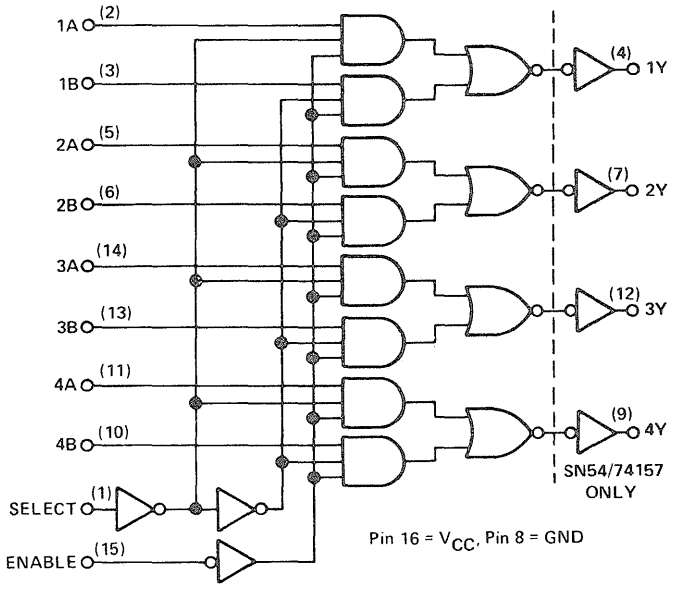


A.8 74157 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER

The 74157 quadruple 2-line to 1-line multiplexer features buffered inputs and outputs. All outputs are low when disabled (enable high). The truth table and logic diagram are shown below.

INPUTS			OUTPUT Y	OUTPUT W
ENABLE	SELECT	A B	SN54/74157, SN54S/74S157	SN54S/74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

H = high level, L = low level, X = irrelevant



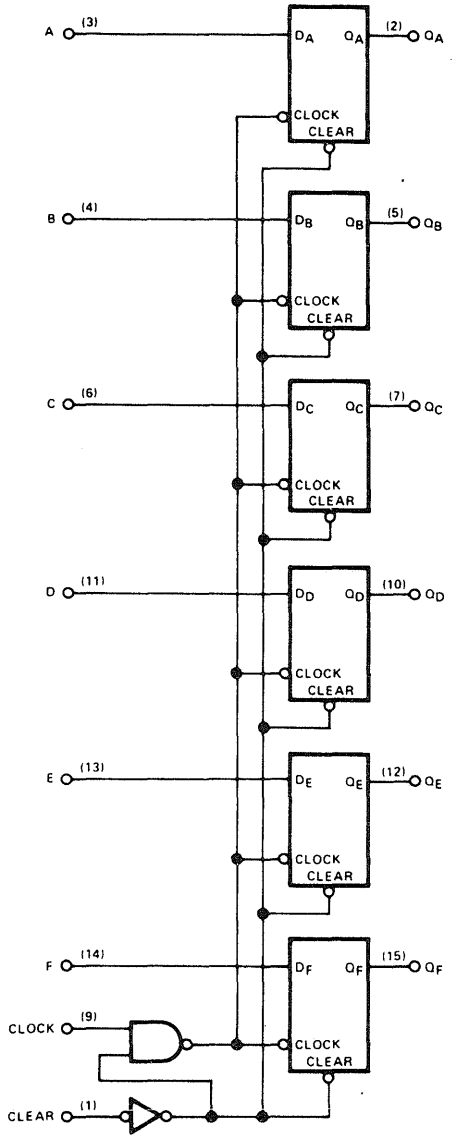
Pin (16) = V_{CC}, Pin (8) = GND

A.9 74174 HEX D-TYPE FLIP-FLOPS

The 74174 contains six flip-flops with single outputs. The flip-flops contain direct clear inputs and buffered clock inputs.

INPUT t_n	OUTPUTS t_n+1	
D	Q	Q
H	H	L
L	L	H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

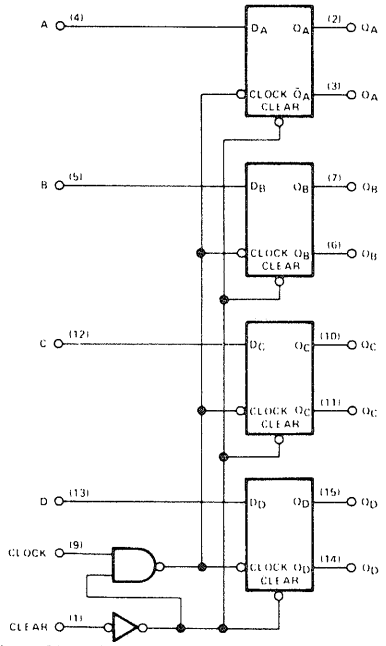
A.10 74175 QUAD D-TYPE FLIP-FLOPS

The 74175 contains four D-type flip-flops with dual outputs. Each flip-flop has direct clear and buffered clock inputs.

INPUT t_n	OUTPUTS $t_n + 1$	
D	Q	$\bar{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.

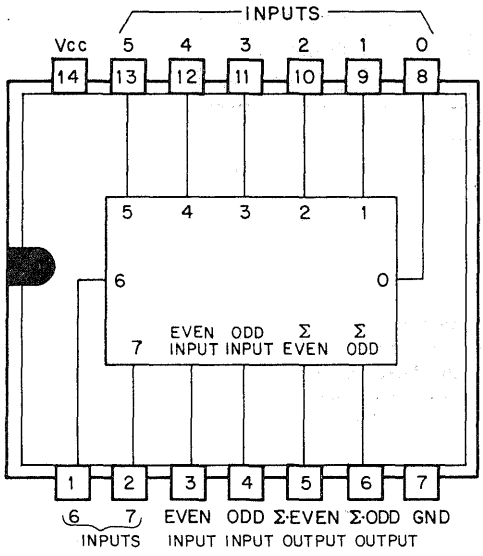
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

A.11 74180 PARITY CONTROL GENERATOR/ CHECKER

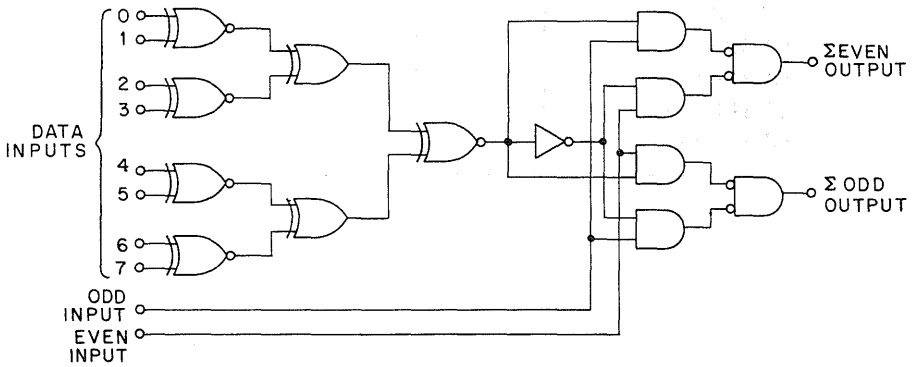
The 74180 is an 8-bit parity generator/checker featuring odd and even outputs and control inputs to provide odd or even parity operation. Word length is expandable by cascading. The truth table, pin connection diagram, and functional block diagram are shown below.



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= IRRELEVANT



11-2384

A.12 74193 4-BIT BINARY COUNTER

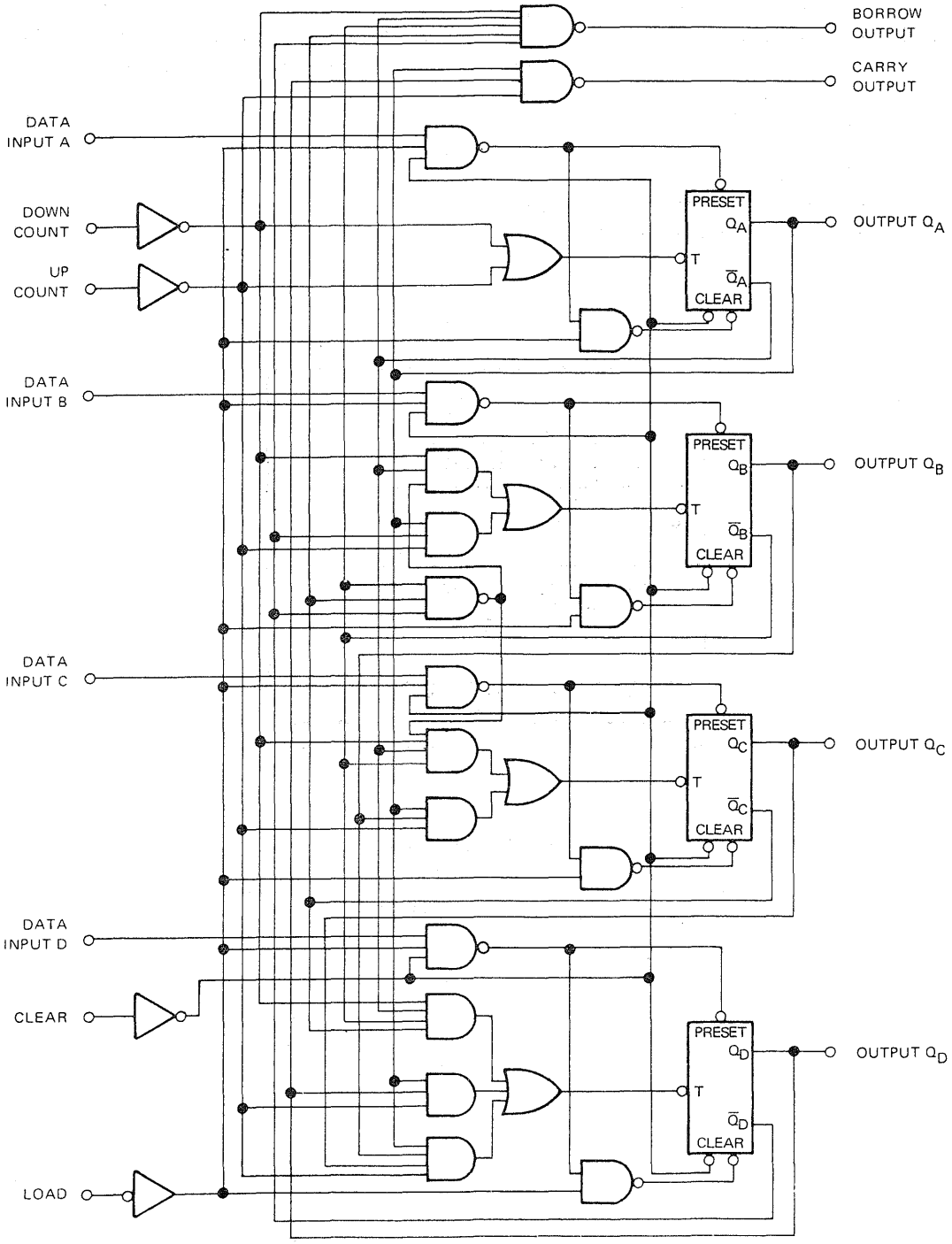
The 74193 binary counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.

COUNT UP	COUNT DOWN	LOAD	MODE
X	X	L	Parallel Load
CLOCK	H	H	Count Up
H	CLOCK	H	Count Down

H = high level, L = low level, X = irrelevant

Signal/Pin Designation

Signal Name	Pin Designation
DATA INPUT A	15
DATA INPUT B	1
DATA INPUT C	10
DATA INPUT D	9
CLEAR	14
LOAD	11
DOWN COUNT	4
BORROW OUTPUT	13
CARRY OUTPUT	12
UP COUNT	5
OUTPUT Q_A	3
OUTPUT Q_B	2
OUTPUT Q_C	6
OUTPUT Q_D	7


BORROW OUTPUT
CARRY OUTPUT
DATA INPUT A
DOWN COUNT
UP COUNT
DATA INPUT B
DATA INPUT C
DATA INPUT D
CLEAR
LOAD
PRESET
Q_A
T
$\overline{Q}_A$
CLEAR
OUTPUT Q_A
PRESET
Q_B
T
$\overline{Q}_B$
CLEAR
OUTPUT Q_B
PRESET
Q_C
T
$\overline{Q}_C$
CLEAR
OUTPUT Q_C
PRESET
Q_D
T
$\overline{Q}_D$
CLEAR
OUTPUT Q_D

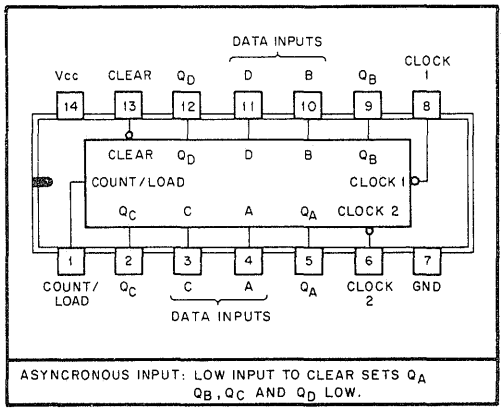
A.13 74197 50 MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

This high-speed monolithic counter consists of four dc coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter. The counter is fully programmable; i.e., the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. It features a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A Q_B, Q_C AND Q_D LOW.

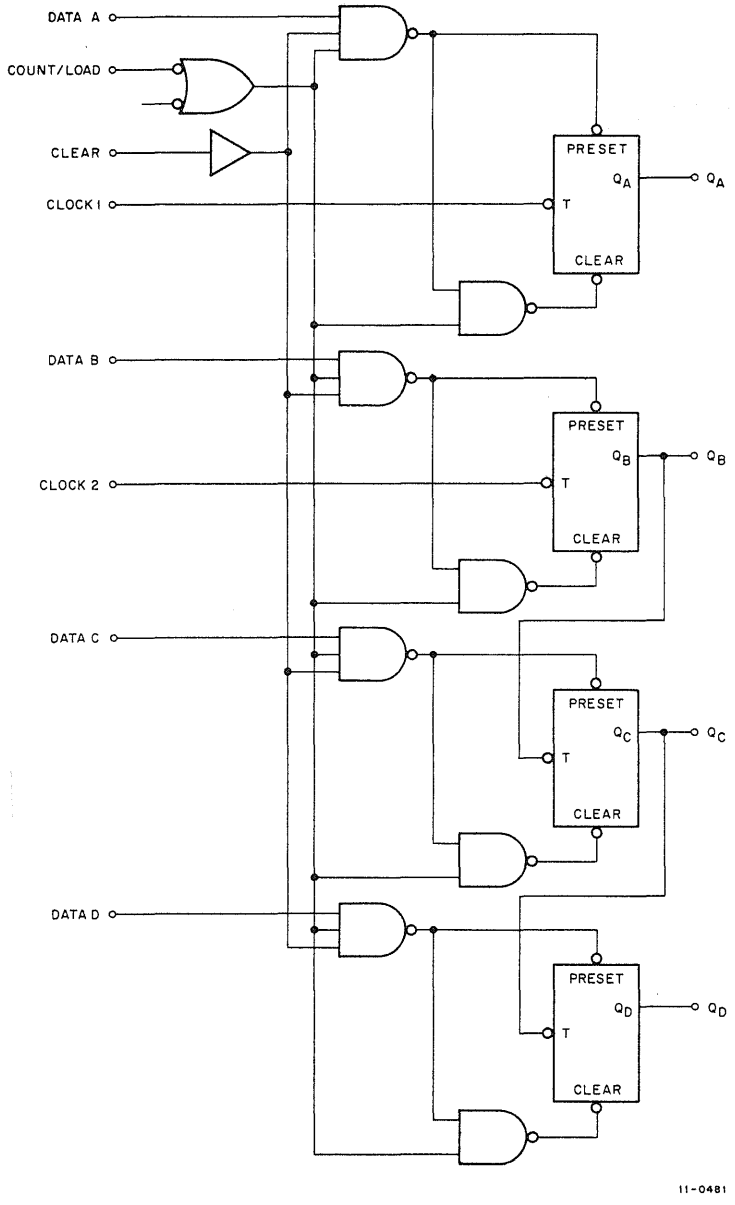
*Pin assignments for these circuits are the same for all packages.

11-0482

SN74197 TRUTH TABLE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.


DATA A
COUNT/LOAD
CLEAR
CLOCK 1
DATA B
CLOCK 2
DATA C
DATA D
PRESET
Q_A
T
CLEAR
Q_A
PRESET
Q_B
T
CLEAR
Q_B
PRESET
Q_C
T
CLEAR
Q_C
PRESET
Q_D
T
CLEAR
Q_D
11-0481

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