TECHNICAL MANUAL
MODEL S33/A
STORAGE MODULE DISK CONTROLLER

TABLE OF CONTENTS

1.0 INTRODUCTION

This manual defines the functional, electrical and mechanical characteristics of the Model S33/A Disk Controller produced by Dataram Corporation, Cranbury, New Jersey for the PDP*-11 series of computers.

*Registered trademark of Digital Equipment Corporation

2.0 GENERAL DESCRIPTION

The Model S33/A Disk Controller emulates the functions and operations of the DEC* RH11 MASSBUS* Controller and attached RM02 Disk Drives. Used with one to four 80MByte CDC Model 9762 (or equivalent) storage modules, the Model S33/A is functionally equivalent to a DEC RM02 Subsystem of the same configuration. See Figure 2.1 for a typical system configuration.

The S33/A controller also provides dual-port capability, enabling two controllers to access one or more common disks which are equipped with dual-port option. See Figure 2.2 for a typical system configuration. Refer to Tables 2.1 and 2.2 for a summary of performance characteristics.

The S33/A controller provides a formatted disk capacity of 67 megabytes per drive using the standard SMD 14-inch diameter removable disk pack with five platters. Data is recorded on the disk in a format identical to that of the RM02.

The S33/A controller provides several forms of redundancy and reliability enhancement with error detection and isolation operations performed on all information read from the disk.

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Standard features include:

1. The RM02 compatible header block with provisions for accepting manufacturer or user specified codes to indicate that the sector is unacceptable for data storage.

2. A 2048 byte RAM memory provides a four-sector data buffer which eliminates data late errors, enables multiple sector cross-track (spiral) read or write operations, and allows the controller to be operated at a low NPR priority level.

3. RM02 compatible, thirty-two bit ECC for data error detection allowing correction of a single 11-bit error burst.

4. RM02 compatible 16-bit CRC for header error detection.

5. Offset commands causing the heads to move off the track centerline to recover marginal data.

These features permit the software to detect and correct errors and recover data that would otherwise be lost. Since the pack type, reading format, redundancy, and recovery techniques are identical to those used by the DEC RM02, recorded packs can be easily interchanged between S33/A and RM02 disk subsystems.

The functional capability of the S33/A with the DEC RM02 provides a large body of existing software to be used without modifications or patches to the standard operating systems as written. The same compatibility provides extensive diagnostic programs for maintenance procedures.

Additionally, extensive micro-program self-test diagnostics check all major components of the controller micro-engine. The self-test program makes no attempt to transfer data to or from the disk or UNIBUS. The self-test operates on power up sequencing and will run with or without a drive connected.

FUNCTION	CHARACTERISTICS
Type	Storage Module Disk Controller
Application	Direct interface to PDP-11 standard UNIBUS* and to most SMD compatible disk drives.
Software Compatibility	DEC RH-11/RM02 System: Standard functional diagnostics, RSX-11M, RSTS, RT-11
Electrical:	
Power	9.4 amps @ + 5 VDC, 0.5 amps @ - 15 VDC
PDP-11 Bus Load	1 unit load, all lines
Physical:	
Dimensions	15.68" x 8.88" hex
Mounting	Plugs directly into PDP-11 Standard UNIBUS SPC slot via A,B,C,D,E,F Connectors
Drive Cable	60-Conductor flat cable, 100 ft. max. 26-Conductor flat cable, 50 ft. max.
PDP-11 Interface:	
Compatibility	Direct to PDP-11 standard UNIBUS
Addressing	Direct to 128K words (256K bytes)
UNIBUS Base Address	Standard: 776700_8 in etch. Selectable: 760000_8 - 777740_8 by jumpers.
UNIBUS Vector Address	Standard: 254_8 in etch. Selectable: 0 - 374_8 by jumpers.
UNIBUS Priority Level	Standard: BR5 in etch. Selectable: BR4 - BR7 by jumpers.
Physical Drives	1 - 4 per controller.
Disk Data Rates	Up to 10 mBit per second serial data.
Dual-Port Drives	Dual-port operations supported on drives suitably equipped.
Media	DEC RM02 media compatible
Register Compatibility	Separate registers for each disk allow emulation of overlapped seeks.
Buffer Memory	2048 byte (4 Sector) bipolar RAM buffer, to eliminate data late errors.

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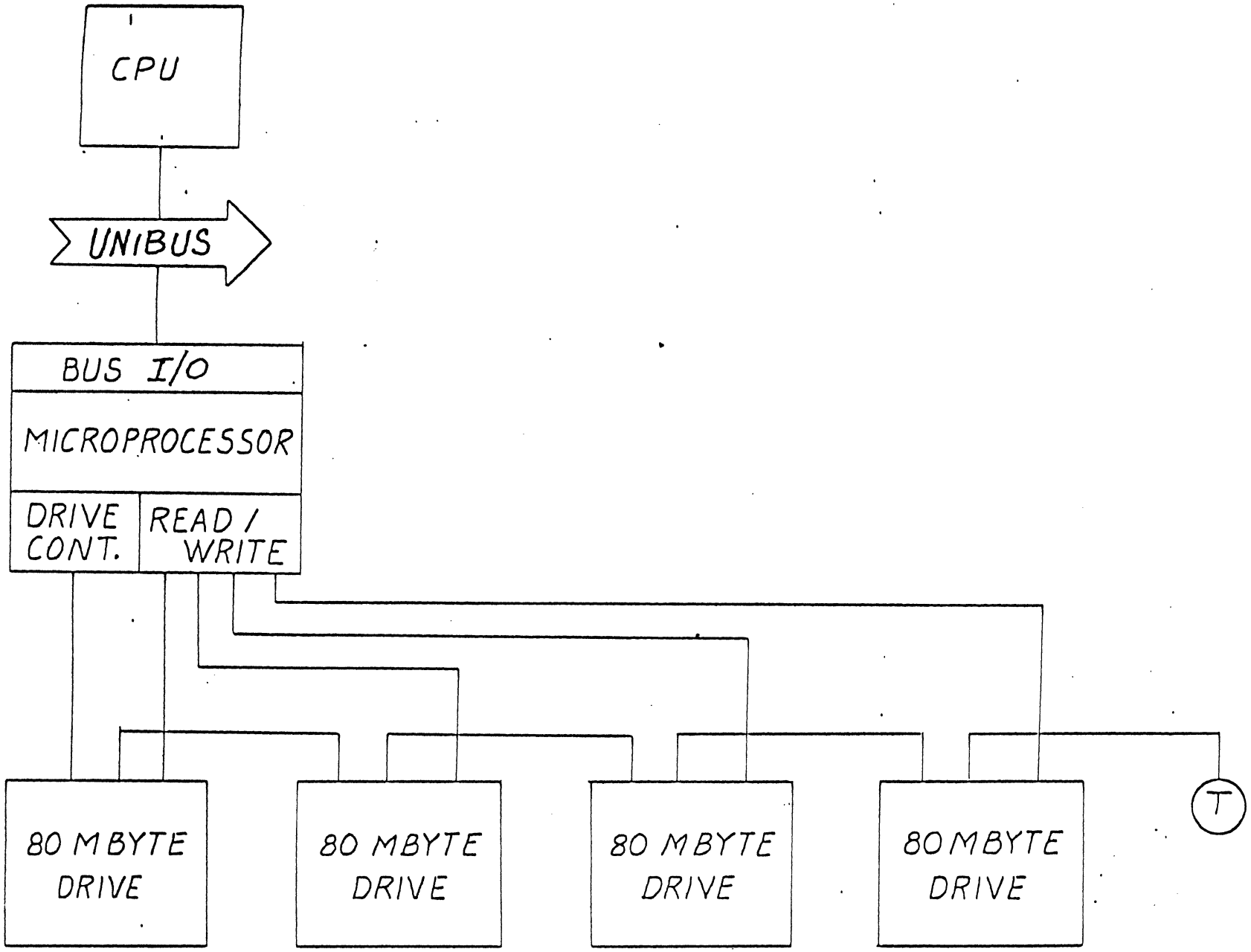
CONTROLLER AND PERFORMANCE CHARACTERISTIC SUMMARY

TABLE 2.1

SPECIFICATION	DRC S33
1. SEEK TIME	
Maximum Seek Time (822 Cylinders), mSec.	55.0
Average Seek Time, mSec.	30.0
1 Cylinder Seek Time, mSec.	6
Seek to Same Cylinder Time, micro-Sec.	37.5
2. LATENCY	
Speed, RPM	3600
Rotational Time, mSec.	16.7
Maximum Latency, mSec.	33.4
Average Latency, mSec.	16.7
3. START/STOP TIME	
Start (Maximum), Sec.	35
Start (Typical), Sec.	25
4. CAPACITY	
Platters/Drive	3
Tracks/Cylinder	5
Cylinders/Pack	823
Total Tracks/Pack	4115
Sectors/Track	32
Data Bytes/Sector	512
MBytes/Drive	67.4
Drives/System, Max	4
MBytes/System, Max	269.7
5. DATA RATES	
Bit Density, BPI	6060
Bit Cell Time, n Sec.	103.3
Disk Data Rate, K Bytes/Sec.	1209
Bus Data Rate, K Bytes/Sec.	810
6. ERROR DETECTION/CORRECTION	
Bits/Sector	32
Maximum Time for Correction, mSec.	4.47

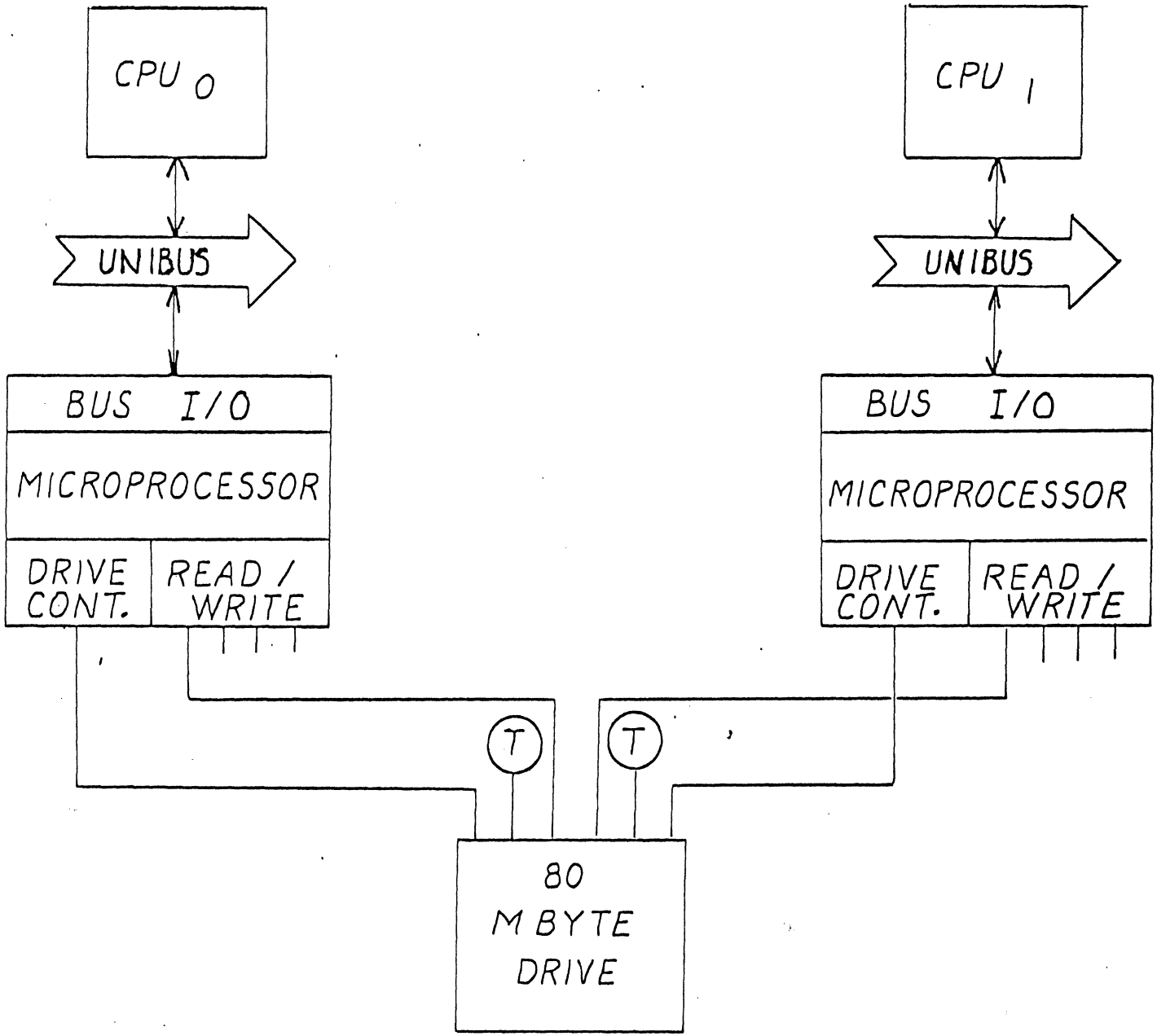
TABLE 2.2

SPECIFICATION COMPARISON



SINGLE PORTED CONFIGURATION
1-4 DRIVES

FIGURE 2-1



DUAL PORTED CONFIGURATION
1-4 DRIVES

FIGURE 2-2

3.0 FUNCTIONAL SPECIFICATIONS

3.1 UNIBUS Interface

The S33 controller interfaces directly to the standard UNIBUS of the PDP-11, plugs into any standard hex SPC slot, and completely conforms to UNIBUS protocol. The bus drivers and receivers used present one unit load on all signal lines and are compatible to those used by DEC.

The following types of I/O transfers occur between the controller and the processor and/or memory modules via the bus.

3.1.1 Programmed I/O Transfers

Transfers to the controller may be either an 8-bit byte of a full 16-bit word. Programmed transfers exchange control and status between the controller and the processor. The controller responds to DATI, DATO, and DATOB types of bus cycles.

3.1.2 DMA Transfers

All data read or write transfers are performed as full word DMA (or NPR) transfers between the controller and memory. To accommodate the high data rates required by the disk with minimum "bus hogging", the S33/A transfers two 16-bit words per NPR request-grant cycle.

Controller priority for NPR transfers is a function of its position on the bus with respect to other devices. Selection of priority is a system consideration. However, since the disk involves relatively high transfer rates, it is recommended that the controller be located at the highest priority position possible.

3.1.3 Interrupts

The controller generates interrupts to the processor to flag various events (end of transfer, error condition, etc.) using location 254_8 as a common interrupt vector. Controller priority for interrupt requests is a function of: (1) the priority level assigned the controller, and (2) its position on the bus with respect to other devices with the same priority level. Other interrupt vectors may be implemented by appropriate jumpers. See Section 4.6.

The PDP-11 has four interrupt request levels, BR4-BR7, with BR4 as the lowest level. The standard level assigned to the RH11 is BR5, and this connection is implemented in etch on the S33/A board (along with etch connection of the associated bus grant level, BG5). The unused bus request levels -- BR4, BR6, BR7 -- and bus grant levels -- BG4, BG6, BG7 -- have their respective in and out lines jumpered together in etch on the S33/A board to assure continuity of these lines to succeeding devices on the UNIBUS. Should it be desired to alter the standard BR priority, etch cuts and jumpers may be incorporated as required.

3.1.4 Bus Signals

The S33/A controller interfaces to the standard PDP-11 UNIBUS via the C, D, E and F connectors. The controller occupies any hex location designated as a Small Peripheral Controller (SPC) slot. Table 3.2 lists the UNIBUS signals used by the controller and their connector and pin assignments.

3.1.5 Initialization and Power Sequencing

Controller response to an Initialize (INIT) signal on the UNIBUS is immediate, terminating any fucntion being executed by any drive. The controller monitors the DC power status line on the UNIBUS, DCLO (DC Power Low). In the event that DCLO indicates that system DC power is unstable, the controller will terminate and clear the controller unconditionally When DC power is stabilized, the controller will perform an automatic initialization so that it is ready to execute the initial software commands received.

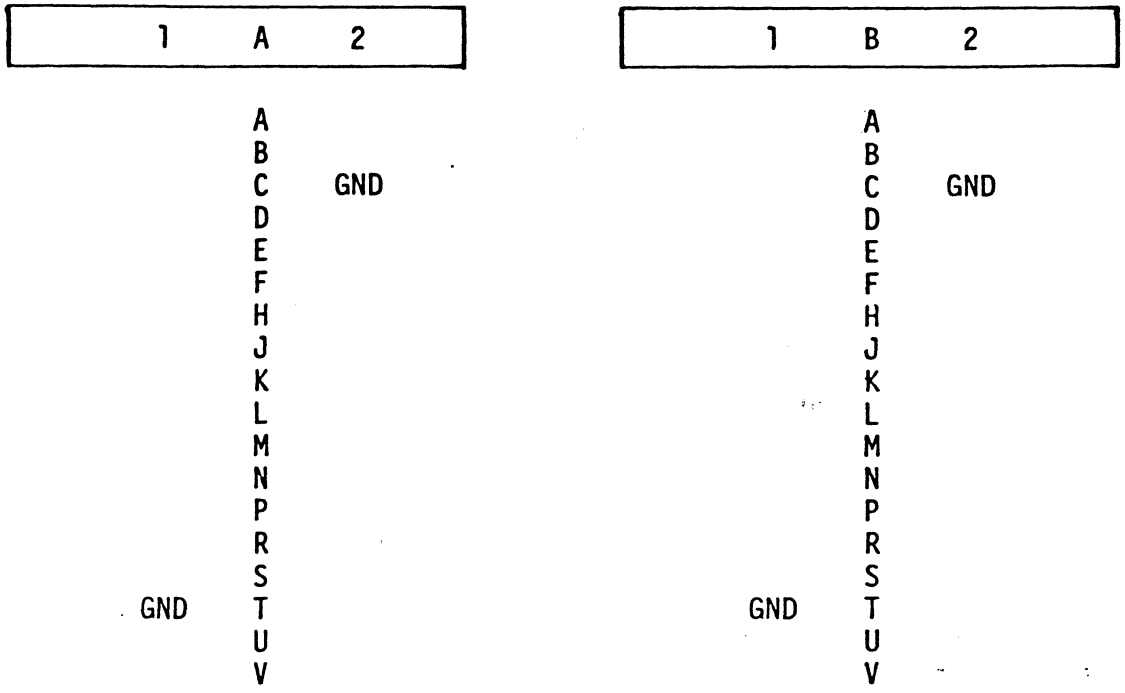
3.2 Controller Registers

Twenty registers are visible to software and emulated by the controller to communicate control commands, status, data, error conditions, and maintenance information. Table 3.2.1 defines these registers, their UNIBUS addresses, and their basic function.

3.3 Disk Interface (See Figures 3.3.1 through 3.3.3 for Flat Cable) (See Figures 3.3.4 through 3.3.5 for Round Cable)

The controller has an industry standard SMD interface utilizing Motorola 3450 and 3453 differential transmitters and receivers. These circuits provide a terminated, balanced transmission system and allow disk operation at radial distances up to 50 feet and daisychain distances up to 100 feet from the controller.

The "A" cable is a twisted pair, flat ribbon cable which allows mass termination to the "A" cable connector without stripping. The "B" cable is a flat ribbon cable with a ground plane and drain wire which allows mass termination without stripping.



1	A	2
	A	
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
	V	

1	B	2
	A	
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
	V	

1	C	2
BUSNPGIH	A	+5V
BUSNPGOH	B	
	C	GND
	D	BUSD15N
	E	BUSD14N
	F	BUSD13N
BUSD11N	H	BUSD12N
	J	BUSD10N
	K	BUSD09N
	L	BUSD08N
	M	BUSD07N
BUSDCLOL	N	BUSD04N
	P	BUSD05N
	R	BUSD01N
BUSPBL	S	BUSD00N
GND	T	BUSD03N
	U	BUSD02N
	V	BUSD06N

1	D	2
	A	+5V
	B	
	C	GND
	D	BUSBR7L
	E	BUSBR6L
	F	BUSBR5L
	H	BUSBR4L
	J	
	K	BUSBGIN7H
BUSINITL	L	BUSBGOUT7
	M	BUSBGIN6H
	N	BUSBGOUT6
	P	BUSBGIN5H
	R	BUSBGOUT5
	S	BUSBGIN4H
GND	T	BUSBGOUT4
	U	
	V	

TABLE 3.2

UNIBUS SIGNALS

1	E	2
	A	+5V
	B	
BUSA12L	C	GND
BUSA17L	D	BUSA15L
BUSMSYNCL	E	BUSA16L
BUSA07L	F	BUSC1L
BUSA01L	H	BUSA00L
BUSSSYNCL	J	BUSC0L
BUSA14L	K	BUSA13L
BUSA11L	L	
	M	
	N	BUSA08L
BUSA10L	P	BUSA07L
BUSA09L	R	
	S	
GND	T	
BUSA06L	U	BUSA04L
BUSA05L	V	BUSA03L

1	F	2
	A	+5V
	B	-15V
	C	GND
BUSBBSYL	D	
	E	
	F	
	H	
BUSNPRL	J	
	K	
	L	
BUSINTRL	M	
	N	
	P	
	R	
	S	
GND	T	BUSSACKL
	U	
	V	

TABLE 3.2

UNIBUS SIGNALS (Continued)

REGISTER	NAME	UNIBUS ADDRESS	MODE	FUNCTION
RMCS1	Control	776700	Read/Write	Function code, Go bit.
RMWC	Word Count	776702	Read/Write	2's complement of number of words to be transferred.
RMBA	Bus Address	776704	Read/Write	Memory address of location where data transfer is to begin.
RMDA	Desired Sector/ Track Address	776706	Read/Write	Disk sector and track address where transfer is to occur.
RMCS2	Status	776710	Read/Write	Controller status indication.
RMDS	Drive Status	776712	Read/Write	Non-error status plus error summary bit.
RMER1	Error No.1	776714	Read/Write	Individual error indication.
RMAS	Attention Summary	776716	Read/Write	1-bit per-drive attention summary status.
RMLA	Look Ahead (Sector Counter)	776720	Read Only	Current sector address under heads.
RMDB	Data Buffer	776722	Read Only	Input and output connection to silo (Buffer) for maintenance.

CONTROLLER REGISTERS

TABLE 3.2.1

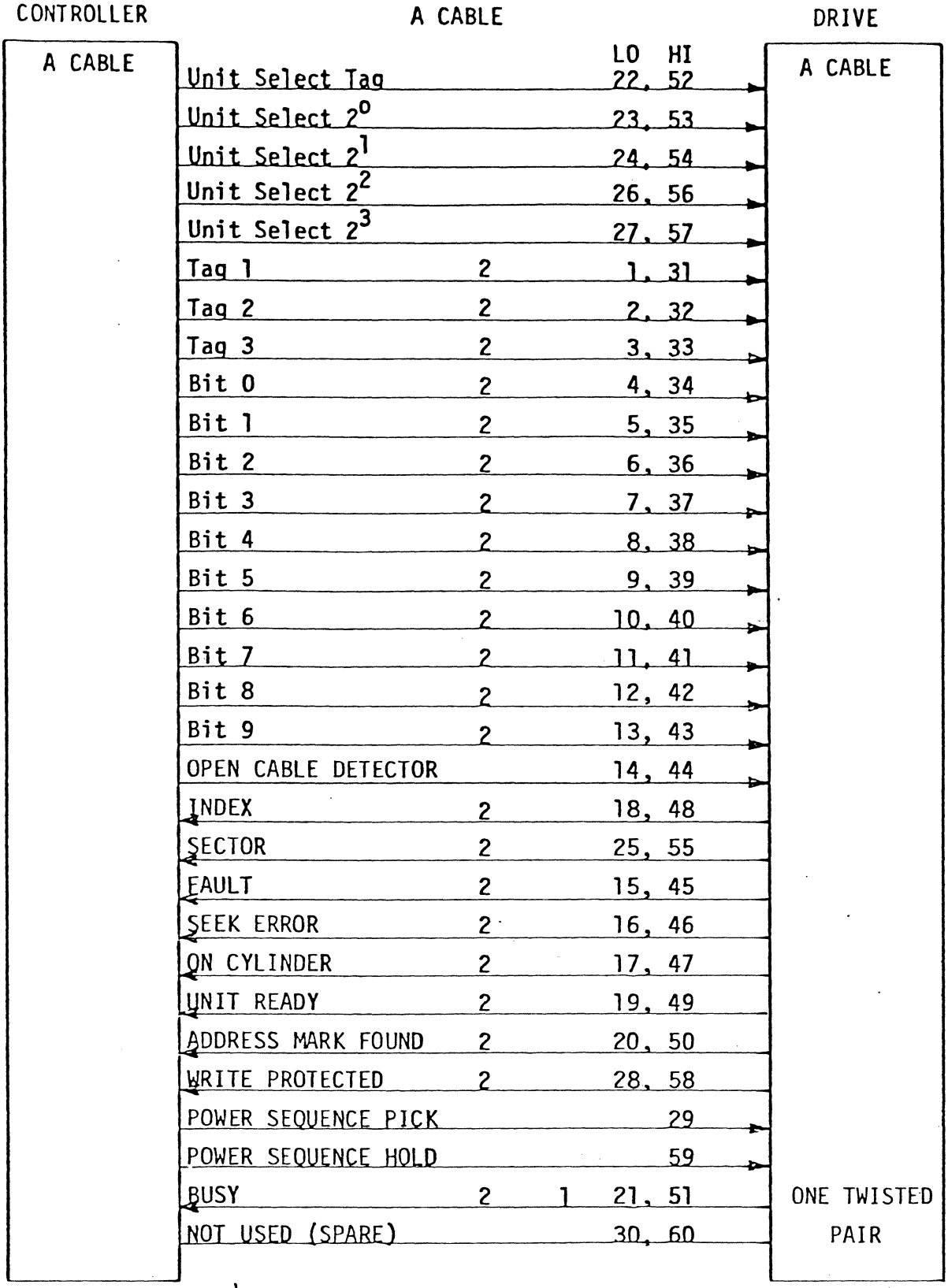
REGISTER	NAME	UNIBUS ADDRESS	MODE	FUNCTION
RMMR1[1]	Maintenance No. 1	776724	Read/Write	Diagnostic test functions.
RMDT	Drive Type	776726	Read Only	Drive Character indication.
RMSN	Serial Number	776730	Read Only	Serial Number Simulated by Logical Unit Selected.
RMOF	Offset	776732	Read/Write	Control bit for offset of drive heads.
RMDC	Desired Cylinder	776734	Read/Write	Address of cylinder for seek operation.
RMHR	Holding	776736	Read/ Write	Not used; contents always all zeros.
RMMR2[1]	Maintenance No. 2	776740	Read Only	Diagnostic test functions.
RMER2	Error No. 2	776742	Read/Write	Drive error bits.
RMEC1	ECC Position	776744	Read Only	Position of error burst.
RMEC2	ECC Pattern	776746	Read Only	Error burst.
RMBAE[2]	Bus Address Extension	776750		
RMCS3[2]	Control and Status	776752		

1. These registers are used by the DEC RH11 controller in Maintenance mode only to test specific logic functions implemented in hardware. No attempt at emulation is made by the S33.

2. No attempt at emulation. No response to these addresses, as they are RH70 registers.

CONTROLLER REGISTERS (Continued)

Table 3.2.1

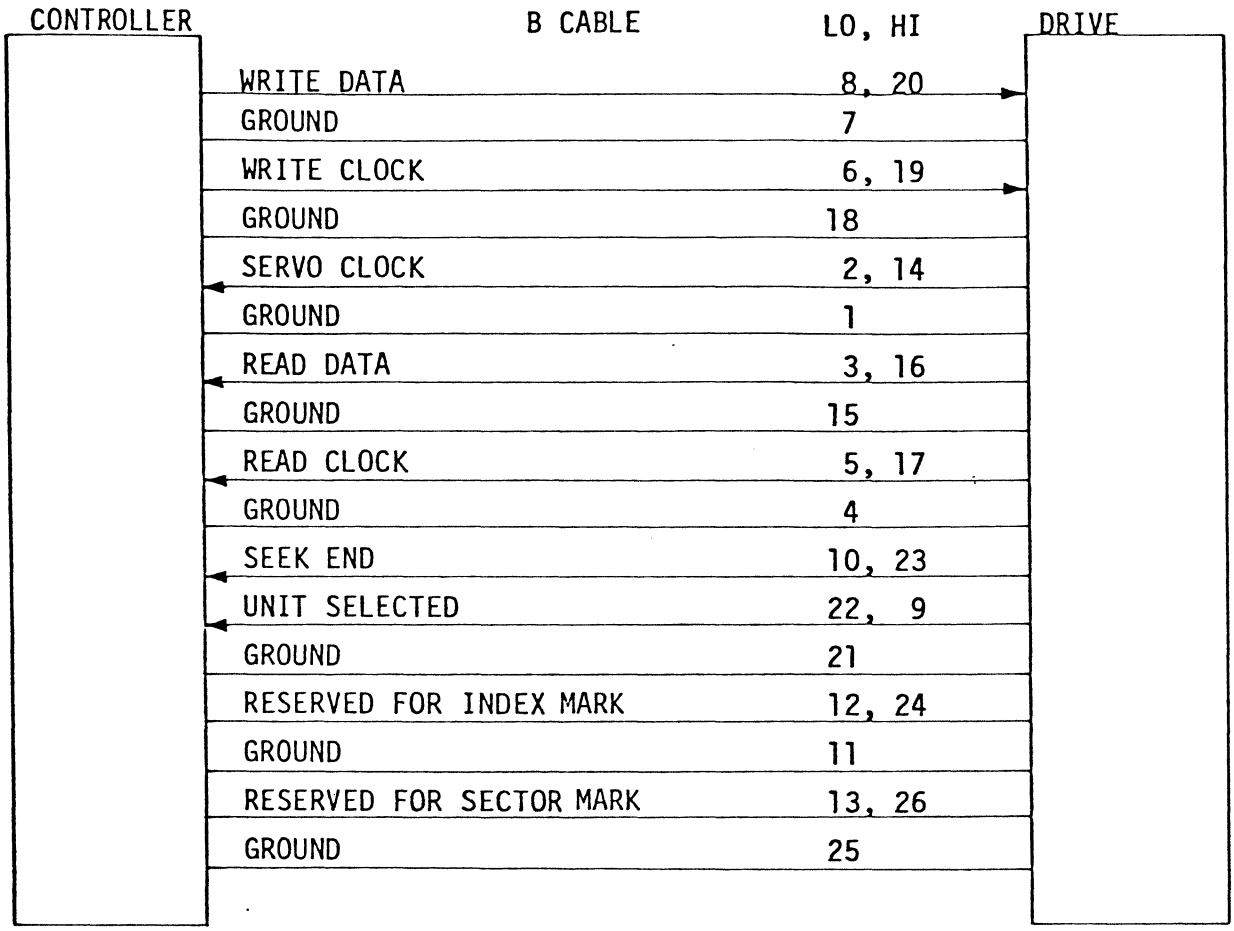


NOTE: 60 POSITION
28 AWG, 30 TWISTED PAIR - STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT.

1 DUAL CHANNEL UNITS ONLY.

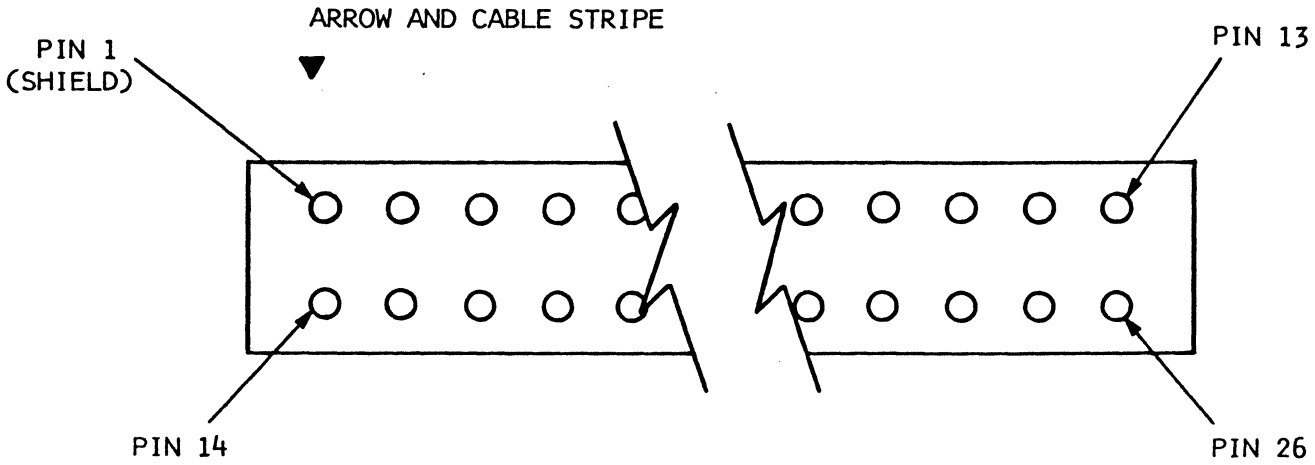
2 GATED BY UNIT SELECTED.

FIGURE 3.3.1 TAG BUS I/O INTERFACE

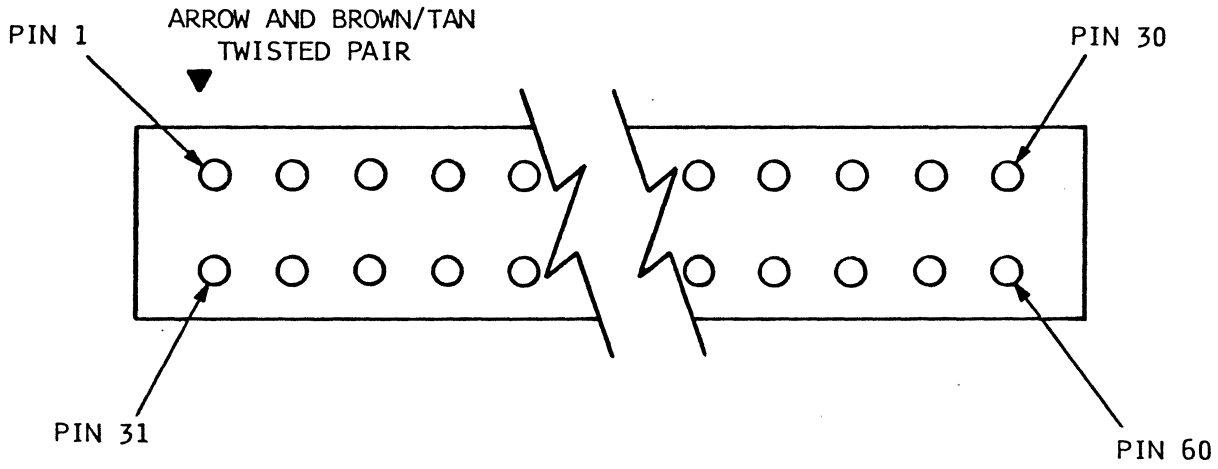


NOTES:
1. 26 CONDUCTOR, FLAT CABLE. MAXIMUM LENGTH - 50 FT.
2. NO SIGNALS GATED BY UNIT SELECTED.
3. SECTOR AND INDEX MUST BE ON "A" CABLE FOR OPERATION WITH S33.

FIGURE 3.3.2 "B" CABLE INTERFACE



26-PIN FLAT CABLE CONNECTOR
("B" CABLE AS VIEWED FROM EITHER END)

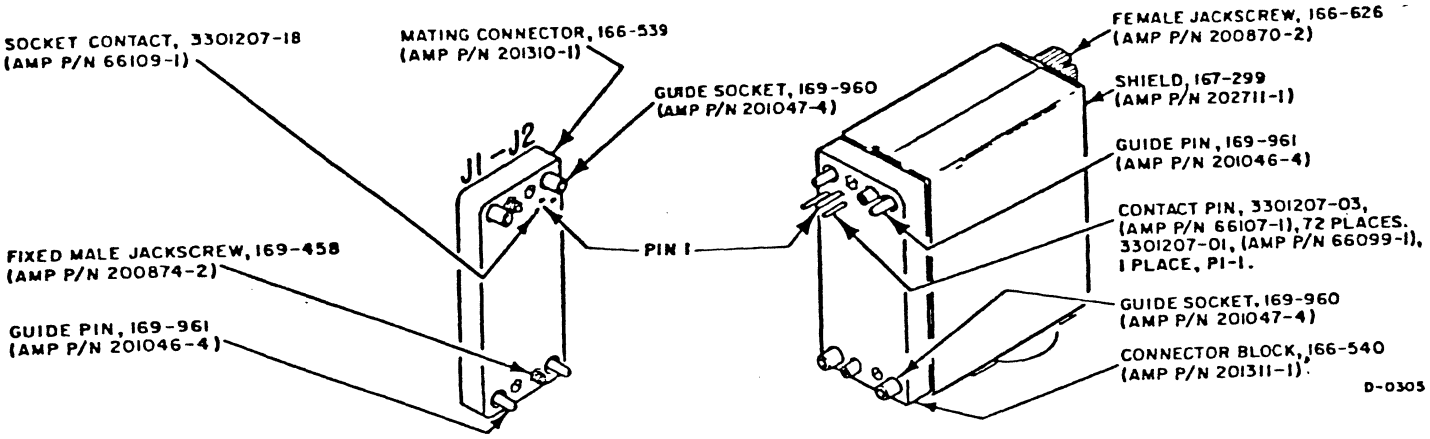


60-PIN FLAT CABLE CONNECTOR
("A" CABLE AS VIEWED FROM EITHER END)

PIN ORIENTATION, A AND B FLAT CABLE CONNECTORS

FIGURE 3.3.3

"A" CABLE DEFINITIONS
ROUND CABLE DRIVE CONNECTOR



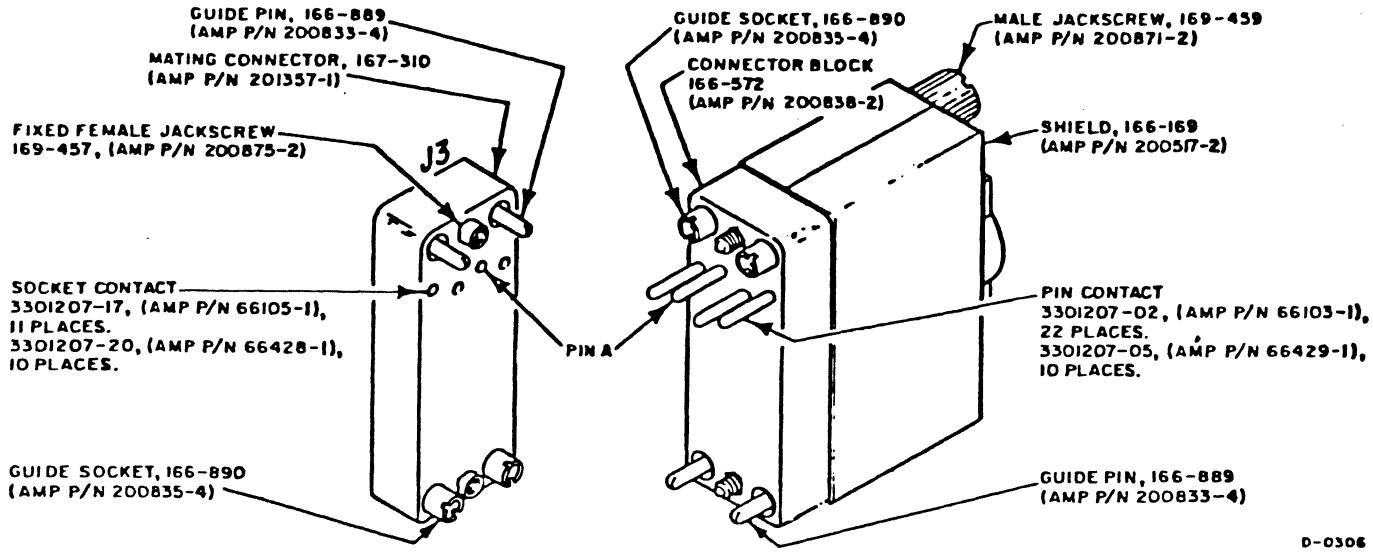
PIN IDENTIFICATIONS

SIGNAL NAME	J1/J2* PINS	FROM	TO
INIT SELECT BIT 0	1,4	CONTROL UNIT	DRIVE
INIT SELECT BIT 1	2,5	CONTROL UNIT	DRIVE
INIT SELECT BIT 2	3,7	CONTROL UNIT	DRIVE
INIT SELECT BIT 3	8,12	CONTROL UNIT	DRIVE
UNIT SELECT TAG	22,25	CONTROL UNIT	DRIVE
SET CYLINDER (TAG 1)	46,49	CONTROL UNIT	DRIVE
SET HEAD ADDRESS (TAG 2)	48,51	CONTROL UNIT	DRIVE
CONTROL TAG (TAG 3)	52,55	CONTROL UNIT	DRIVE
BIT 0	23,26	CONTROL UNIT	DRIVE
BIT 1	24,27	CONTROL UNIT	DRIVE
BIT 2	28,31	CONTROL UNIT	DRIVE
BIT 3	29,32	CONTROL UNIT	DRIVE
BIT 4	30,33	CONTROL UNIT	DRIVE
BIT 5	34,37	CONTROL UNIT	DRIVE
BIT 6	35,38	CONTROL UNIT	DRIVE
BIT 7	36,39	CONTROL UNIT	DRIVE
BIT 8	40,43	CONTROL UNIT	DRIVE
BIT 9	41,44	CONTROL UNIT	DRIVE
OPEN CABLE DETECTOR	16,20	CONTROL UNIT	DRIVE
INDEX	10,13	DRIVE	CONTROL UNIT
SECTOR	74,77	DRIVE	CONTROL UNIT
FAULT (UNSAFE)	11,14	DRIVE	CONTROL UNIT
SEEK ERROR (SEEK INCOMPLETE)	75,78	DRIVE	CONTROL UNIT
ON CYLINDER (ATTENTION)	15,18	DRIVE	CONTROL UNIT
UNIT READY (ON LINE)	17,21	DRIVE	CONTROL UNIT
WRITE PROTECT	53,56	DRIVE	CONTROL UNIT
ADDRESS MARK (NOT USED)	42,45	DRIVE	CONTROL UNIT
POWER SEQUENCE HOLD (-)	73	CONTROL UNIT	DRIVE
SEQUENCE PICK IN (-)	76	CONTROL UNIT	DRIVE

* FIRST PIN IN PAIR IS (-); SECOND IS (+)

FIGURE 3.3.4

"B" CABLE DEFINITIONS
ROUND CABLE DRIVE CONNECTOR



PIN IDENTIFICATIONS

SIGNAL NAME	J3 PINS	FROM	TO
WRITE DATA	A,B	CONTROL UNIT	DRIVE
SERVO CLOCK	M,N	DRIVE	CONTROL UNIT
READ DATA	U,V	DRIVE	CONTROL UNIT
READ CLOCK	W,X	DRIVE	CONTROL UNIT
WRITE CLOCK	H,J	CONTROL UNIT	DRIVE
UNIT SELECTED	BB	DRIVE	CONTROL UNIT
SEEK END (ATTENTION)	AA,CC	DRIVE	CONTROL UNIT
[1] INDEX	HH	DRIVE	CONTROL UNIT
[1] SECTOR	FF,JJ	DRIVE	CONTROL UNIT

NOTE 1: INDEX AND SECTOR APPEAR IN "B" CABLE IN SOME DRIVE OPTIONS. THEY MUST BE IN "A" CABLE (STD. DRIVE CONFIGURATION) FOR S33 CONTROLLER.

FIGURE 3.3.5

3.4 Power Requirements

+4.75 VDC to +5.25 VDC @ 9.4 amps
-13.5 VDC to -16.5 VDC @ 0.5 amps

3.5 Physical Description (Figure 3.5.1)

The S33/A controller is physically contained on a single hex height printed circuit board measuring 15.68 inches by 8.88 inches, identical to the hex card size of many DEC PDP-11 peripheral controllers. The card is a 4-layer printed wiring board having its power and ground distribution plane on the inner layers and signal lines on the outer layers.

The controller plugs into any standard hex SPC slot, minimizing mounting space requirements, system configuration changes, specially wired system units, and external boxes and cables. Permanently attached insertion/extraction handles are provided to facilitate insertion and removal from the computer.

Disk drives are connected to the S33/A via flat ribbon connectors located on the rear edge of the controller. One 60-conductor ribbon cable providing address, control and status between the controller and drives is connected to all drives in a daisychained fashion with a terminator at the end of the cable.

A 26-conductor ribbon cable providing clock and data between the controller and each drive is required for each attached disk and connected in a star configuration.

3.5.1 Weight

28 ounces (0.8 kg)

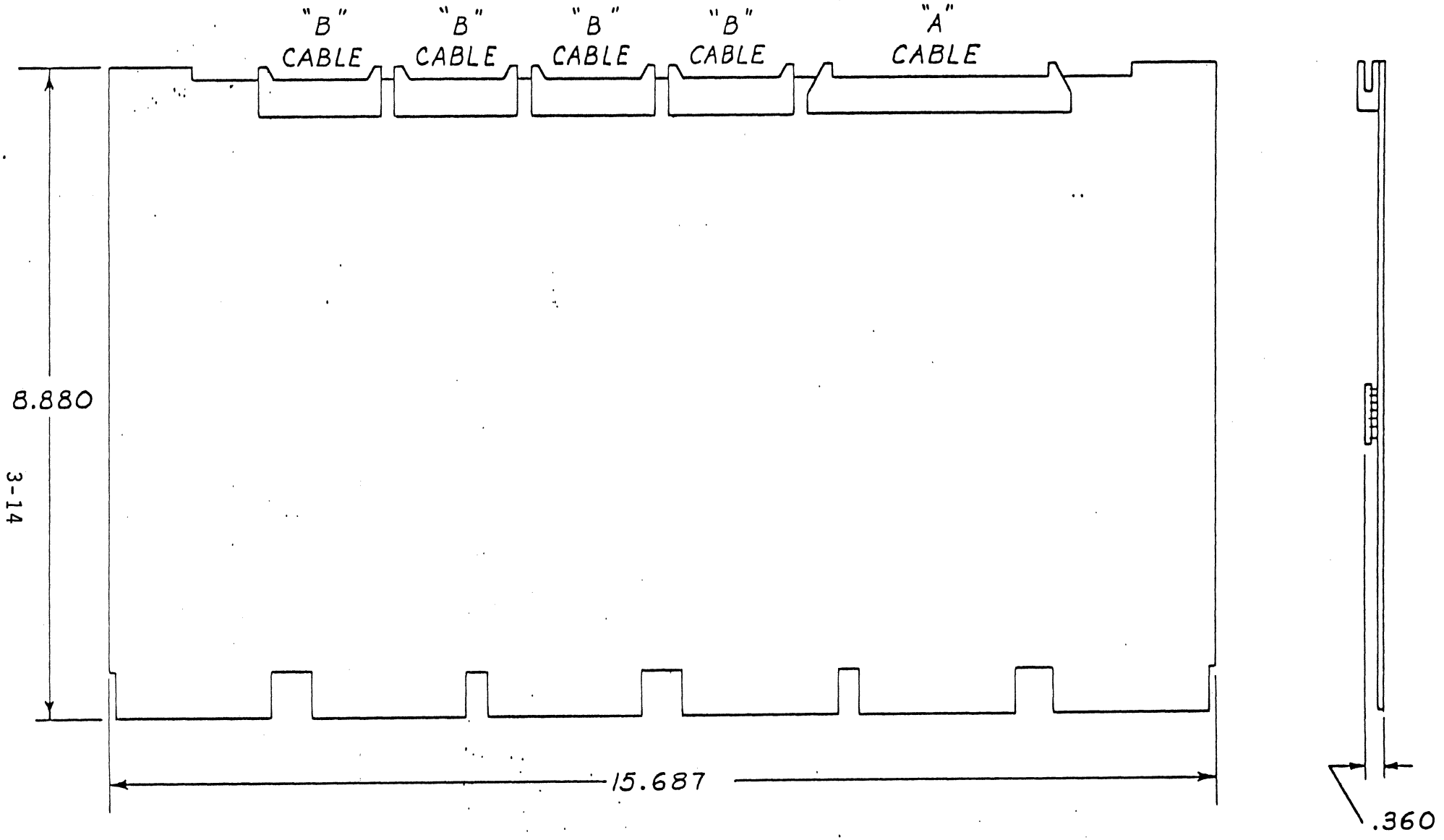


FIGURE 3.5.1

3.6 Environmental

The S33/A controller is designed to operate in or withstand the following environments.

3.6.1 Temperature

Operating	0^{o} to $+55^{o}C$
Non-Operating	-40^{o} to $+60^{o}C$

3.6.2 Relative Humidity

Up to 95% without condensation

3.6.3 Altitude

Operating	1000 ft. below sea level to 10,000 ft. above sea level
Non-Operating	1000 ft. below sea level to 20,000 ft. above sea level

3.6.4 Vibration

Will withstand normal stresses encountered in transport.

3.7 Ordering Information

The following part numbers have been assigned to the Model S33 and accessories:

65001	Model S33/A Storage Module Disk Controller
65013	SMD "A" Cable, 10-ft. (Control Cable)
65015	SMD "A" Cable, 25-ft. (Control Cable)
65014	SMD "B" Cable, 10-ft. (Data Cable)
65016	SMD "B" Cable, 25-ft. (Data Cable)
65028	SMD "A" Round Cable, 10-ft.
65029	SMD "B" Round Cable, 10-ft.
65030	SMD "A" Round Cable, 25-ft.
65031	SMD "B" Round Cable, 25-ft.
65032	SMD Ground Cable, 10-ft.
65033	SMD Ground Cable, 25-ft.

4.0 INSTALLATION AND OPERATION

4.1 General

A major advantage of the S33 is its ease of installation. Since it is completely contained on a single hex height board, it is physically installed the same as a standard PDP-11 hex interface board.

The user is referred to various DEC publications which may contain specific checklist items which should be observed in the installation of standard PDP-11 components as well as the S33 controller. Initial problems with the disk controller when imbedded in a system are, more often than not, the result of failure to observe all necessary installation procedures for all system elements, not just the disk controller. Often, various oversights will not be detected with some system elements connected and will appear only with the addition of new components. Some specific steps to avoid often-incurred problems of a general nature are noted below.

(1) Verify that the capacity of the power source is not exceeded, and that the source meets the tolerances specified for the minicomputer (and any other system elements of a special nature). An overloaded power source may produce intermittent failures which are difficult to detect.

(2) Insure that the bus interrupt and DMA grant daisychain lines are properly propagated. Unused option slots should have these lines (NPG and BRG) jumpered.

(3) Check to see that all boards in the processor are properly oriented and that boards and drive cables are properly seated in the connectors.*

(4) Insure that all necessary signals, including power and ground inputs, are connected as required to the backplane assembly.

*CAUTION: It is possible to plug S33 controller in backwards. If power is applied in this position, controller components will be destroyed.

(5) Check all option switches, option jumpers, and other variable items for proper settings/connections.

4.2 Inspection

A visual inspection of the unit is recommended after unpacking. Specific checks should be made for such items as bent or broken pins or component leads, damaged components, or any other visual evidence of physical damage. The cable and associated drive adapter unit (if included) should likewise be visually inspected prior to installation.

The simplicity of the controller board makes such visual inspection most worthwhile because physical damage incurred in shipment will usually be obvious. Should any damage be detected, you may wish to immediately return the unit to Dataram for repair prior to further handling.

4.3 Installation

4.3.1 Computer Installation

After visual inspection and prior to insertion in the computer, it is recommended that the S33 be checked for proper configuration. The optional selections on the board which control configuration are:

- o Proper Interrupt Vector Address Jumpers
- o Proper CSR Address Jumpers

The following points should be checked in the PDP-11 computer:
1) The S33 interfaces the UNIBUS via the C,D,E,F connectors only. Backplane slot must be compatible with QUAD or HEX Small Peripheral Controllers (SPC). DEC system unit backplane may be either UNIBUS or MUDBUS compatible.
2) Since the S33 is a HEX high module all six (A, B, C, D, E, F) connectors must be available.
3) The S33 controller has DMA capability and utilizes the BUSNPG line. Standard system units have the NPGINH and NPGOUTH lines wirewrap jumpered on the wiring side of the backplane.

This jumper (between CA1 and CB1) must be removed from the connector slot that accepts the S33. If the S33 is unplugged this jumper must be reinstalled for proper operation of the computer without the S33.

4) On some older system mounting units (SMU), The BUSACLOL and BUSDCLOL signals are not wired to the SPC connector pins. If the S33 is being installed in an old SMU verify that these connections are made.

4.3.2 Drive Installation

4.3.2.1 General

Prior to connecting the drive to the S33 confirm the following:

1) The drive is configured for the proper number of sectors. (32 sector format for S33/A, B, C)

2) Sector and Index are on the A cable. (CDC transmitter option FTVV)

3) Make sure the last physical drive is terminated per manufacturer's recommendation.

4) Ground cable must be installed between computer frame and Drive ground lug.

4.3.2.2 Cable Connections

The 60-position A cable connector is installed in the corresponding connector on the S33.

The 26 position B cable connector of each drive may be installed in any one of the four connectors on the S33. All four connectors are identical and no particular sequence of physical/logical drive number assignment is required. Arrows marked on connectors must line up.

CAUTION: Use care when inserting into and removing from the drive cable connectors because the connector material can be easily damaged. A connector tool is available from the manufacturer and is recommended.

4.4 Operation

4.4.1 Power UP

Upon power up, the S33 performs an extensive self-test. This can be noticed by observing the four LED's located along the edge of the S33. During power up, all four LED's will appear to flash on simultaneously and then go out. In actuality, the four LED's are displaying, in reverse sequence, a binary count representing the 16 self-test routines performed by the on-board microprocessor. This happens so fast that the appearance is that all LED's flash at once. If the LED's do not all go out but remain lit in some binary code, this will indicate a failure of some sub-test.

The power-up tests are to verify proper operation of internal controller circuits only and should run to completion (all lights go out) whether or not a drive is connected. If the board has +5 volts applied and the backplane signals BUS ACLO-L and BUS DCLO-L are both high (negated)*, the tests should run successfully on a good controller board. Successful running of the test does not guarantee that the NPG jumper has been removed from the back-plane, however.

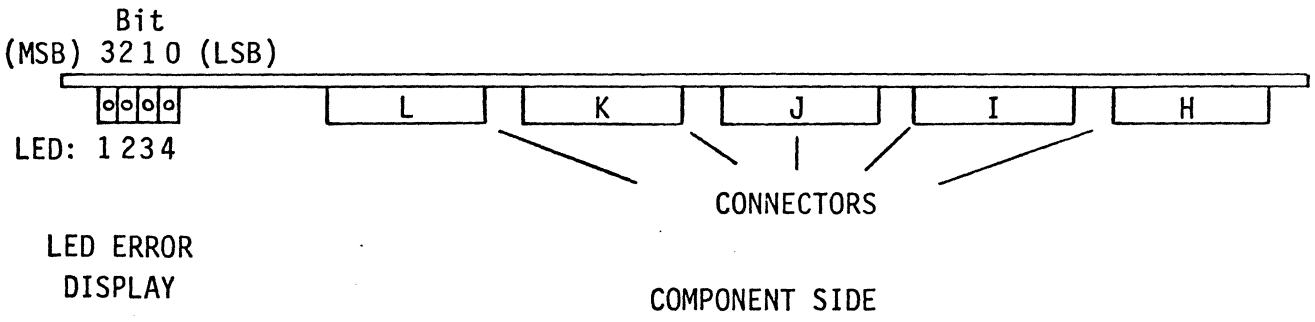
If an error condition is displayed by the LED's, the installation procedure should not be continued. Recheck all connections and options and retry the power-up self test. If there is still a failure, refer to Section 4.5. If the problem remains, contact the factory for assistance or return the S33 for repair as out-lined in Dataram's "Return Material Policy".

See also Table 4.4.1 and Section 4.5 for further information concerning the Self-Tests.

TABLE 4.4.1
SELF DIAGNOSTIC ERROR CODES

The tests below are listed in the order in which they execute.

TEST	FEATURE TESTED	RESULTING ERROR DISPLAY LED'S	
		Binary Bit: 3210	Hex
Priority Vector	Firmware Interrupts Bus DCLO, BUS INIT	1111	F
Timer	Interrupt Timer	1101	D
Data Sequencer	Data Sequencer	0101	5
FIFO	Disk FIFO (Storage)	0111	7
Disk 1	Disk Sequencer	0011	3
DBit	Conditional Branch-On-Bit	0001	1
2901	μ-Processor and its RAM	1001	9
XFile	PIO Register Files	1011	B
1K Buffer	UNIBUS 1K Word Buffer	1010	A
Disk 2	Disk FIFO (S/P, P/S Conversion)	0010	2
---	(Completion)	0000	0



4.4.2 Diagnostics

The S33/A will run all of the DEC RM02 diagnostics without patches with the exception of the Diskless Diagnostic Tests (DZRMJCØ and DZRMKBØ). These two diagnostics will not run at all due to the testing of the specific logic/hardware implementation of an RM02.

4.4.2.1 Formatting

Prior to running any of the diagnostics, the disk pack must be formatted. When formatting, the CZRMACØ RM03/RM02 Formatter program is used as supplied by DEC. If the pack has not been previously formatted as an RM02 Disk Pack, the bad block directory must first be initialized. The Formatter program can be run and it will report several errors. These are due to improper information in the bad track directory. The Formatter program will pause, waiting for an operator response to the prompt "SN:" (Serial Number). At this time, enter "1" and a Carriage Return. The Formatter will now write the bad block directory or format the pack. Few, if any, errors should be reported on this pass. Any errors on this or subsequent passes are probably due to marginal media. If there is difficulty in getting the Formatter program to operate successfully on a previously unformatted pack, the following program can be used to initialize the directory sufficiently to allow the Formatter to run.

```
ADR
1000     12737      40       MOV #40,@#176710          ;CNTRL CLR
1006     12737      23       MOV #23,@#176700          ;PACK ACKNOWLEDGE
1014     12737   10000       MOV #10000,@#176732       ;16 BIT FMT
1022     12737    1466       MOV #1466,@#176734        ;CYL ADR = 822
1030     12737    2000       MOV #2000,@#176706        ;TRK = 4,SCT = Ø
1036     12737    2000       MOV #2000,@#176704        ;BUS ADR = 2000
1044     12737  160000       MOV #160000,@#176702      ;WD CNT = 16K
1056     12737  151466       MOV #151466,@#2000        ;1ST HDR WRD
1060     12737    2000       MOV #2000,@#2002          ;2ND HDR WRD
1066     12737      63       MOV #63,@#176700          ;WRT HDR & DATA CMND
1074    105737  176700 NRDY:TSTB@#176700               ;TST RDY
1080    100375             BPL NRDY                  ;LOOP TIL RDY
1082         0             HALT                      ;RDY
```

A first pass of the format program, DZRMAC0, should then be run to fully initialize the bad block directory. Some errors should be expected. A second pass should then be run, resulting in few, if any, errors. Any errors on subsequent passes would probably be due to marginal areas on the pack.

4.4.2.2 Diagnostic Tests

After formatting, the following diagnostic tests may be run without modification:

1. Performance Exerciser CZRMBBØ -- Best overall single test. Verifies data and seek error rates while exercising the disk system by using all commands and data patterns. This test requires a fully formatted disk pack.

2. Functional Tests

   Part 1 CZRMCBØ -- Tests housekeeping and mechanical positioning.

   Part 2 CZRMDCØ -- Tests Write, Read, and Write Check operations using Header and Data

   Part 3 CZRMECØ -- Tests Write, Read, and Write Check operations using Data only.

3. Extended Drive Test CZRMFBØ -- Tests disk's ability to perform seeks and data storage and retrieval in the specified access times. Also tested are track and sector addressing. Disk pack must be formatted.

4. Drive Compatibility Test CZRMIBØ -- Tests pack interchange between RM02 drives.

NOTE: Diagnostic programs do not use the bad block directory and will report bad blocks as encountered.

4.4.2.3 Key-In Test Program

The following program may be used to perform a rough operational check on the disk system at sites which do not have the full disk diagnostic or the means to load it. The contents of buffers may be changed, then reads, writes and write checks may be done. Proper status following each transfer should be verified by examining location 776700 (CSR1). The pack must have previously been formatted.

```
                                        .TITLE RM02.MAC
                                        ;THIS ROUTINE WILL TRANSFER DATA FROM MEMORY TO THE
                                        ;RM02 DISK, READ THE DATA BACK AND COMPARE FOR ERRORS.
                                        ;TRANSFER PARAMETERS MAY BE ALTERED AS DESIRED.
                                        ;
 000000  012737  000040  176710  WRITE: MOV     #40,    @#176710        ;CLR CONTROLER
 000006  012737  000023  176700         MOV     #23,    @#176700        ;SET VOLUME VALID
 000014  012737  010000  176732         MOV     #10000, @#176732        ;SET 16 BIT FORMAT
 000022  005037  176710                 CLR     @#176710                ;SELECT UNIT 0
 000026  012737  000000  176734         MOV     #0,     @#176734        ;SELECT CYCLINDER 0
 000034  012737  000000  176706         MOV     #0,     @#176706        ;SELECT TRACK 0, SECTOR 0
 000042  012737  010000  176704         MOV     #10000, @#176704        ;SELECT BUS ADDRESS (WRITE)
 000050  012737  177770  176702         MOV     #177770,@#176702        ;SELECT WORD COUNT
 000056  012737  000061  176700         MOV     #61,    @#176700        ;SELECT FUNCTION & GO BIT
 000064  105737  176700                 TSTB    @#176700                ;TEST FOR WRITE XFER DONE
 000070  100375                         BPL     .-4                     ;
                                        ;
 000072  012737  000040  176710  READ:  MOV     #40,    @#176710        ;CLR CONTROLLER
 000100  012737  010000  176732         MOV     #10000, @#176732        ;SET 16 BIT FORMAT
 000106  012737  000000  176734         MOV     #0,     @#176734        ;SELECT CYCLINDER 0
 000114  012737  000000  176706         MOV     #0,     @#176706        ;SELECT TRACK 0 , SCETOR 0
 000122  012737  020000  176704         MOV     #20000, @#176704        ;SELECT BUS ADDRESS (READ)
 000130  012737  177770  176702         MOV     #177770,@#176702        ;SELECT WORD COUNT
 000136  012737  000071  176700         MOV     #71,    @#176700        ;SELECT FUNCTION & GO BIT
 000144  105737  176700                 TSTB    @#176700                ;TEST FOR READ XFER DONE
 000150  100375                         BPL     .-4                     ;
                                        ;
 000152  012700  010000         CMP:    MOV     #10000, R0              ;SET WRITE DATA POINTER
 000156  012701  020000                 MOV     #20000, R1              ;SET READ DATA POINTER
 000162  012702  177770                 MOV     #177770,R2              ;SET WORD COUNT FOR COMPARE
 000166  022021                 1$:     CMP     (R0)+,  (R1)+           ;COMPARE WRITE DATA WITH READ DATA
 000170  001005                         BNE     ERROR                   ;HALT ON ERROR
 000172  005202                         INC     R2                      ;INCREMENT WORD COUNT FOR COMPARE
 000174  005702                         TST     R2                      ;TEST WORD COUNT FOR COMPARE OVERFLOW
 000176  001373                         BNE     1$                      ;CONTINUE COMPARE IF NEGATIVE
 000200  000167  177574         DONE:   JMP     WRITE                   ;TRANSFER OK
 000204  000000                 ERROR:  HALT                            ;DATA COMPARE ERROR
         000000'                         .END WRITE
```

4.5 Disk System Troubleshooting Guide

4.5.1 Disk System failures usually fall into one of the following categories:

1) Internal S33 Controller Problems
2) Drive Cabling Problems (A, B, Ground)
3) SMD Drive Problems
4) Host Processor Chassis Problems (CPU, Memory, Backplane, Power Supply)

The solution of any system problem relies on the successful isolation of the fault to one of the above areas. Dataram controller support can be helpful only if the problem falls into the first category.

4.5.2 Fault Isolation Steps

4.5.2.1 Is it an Obvious S33 Board Problem?

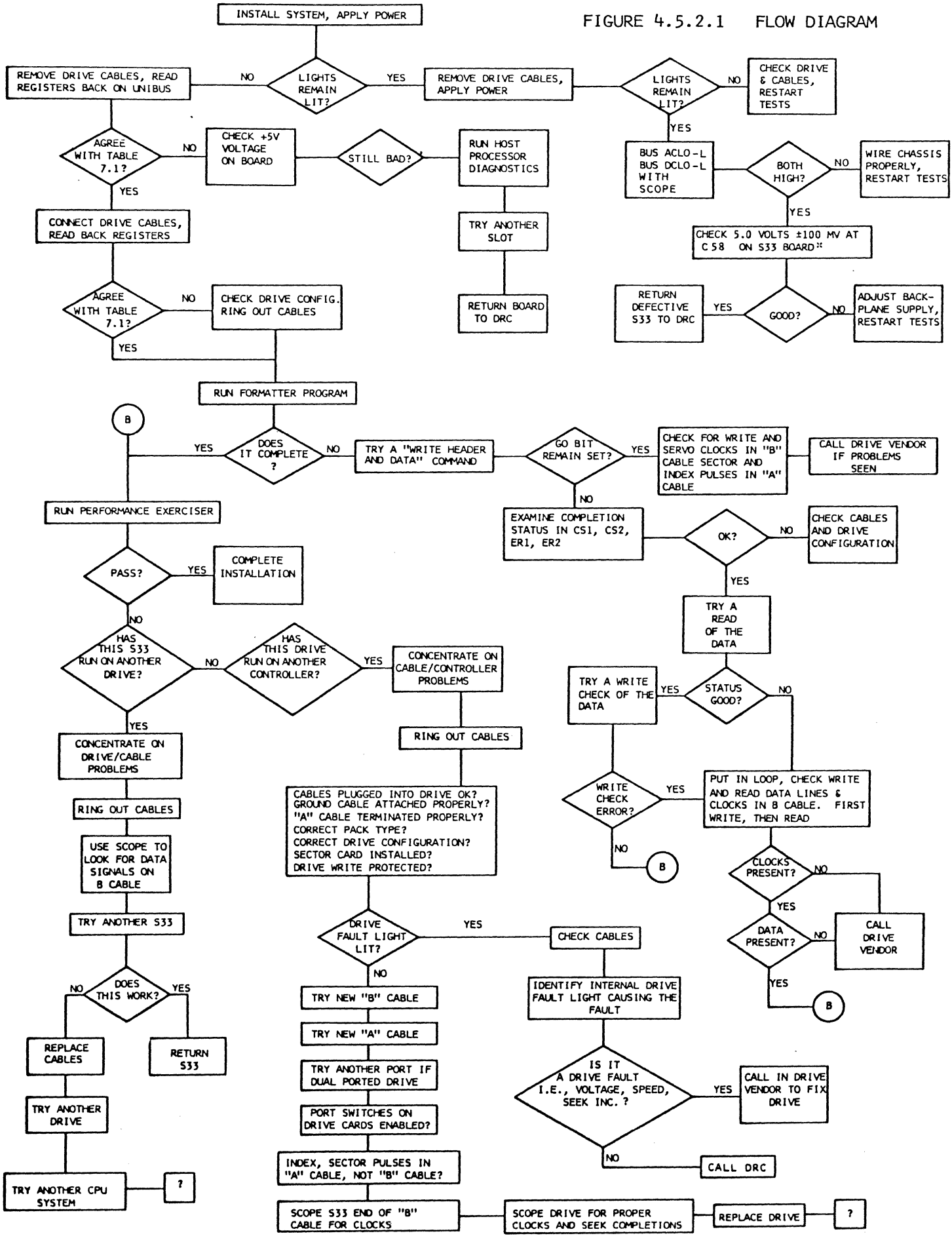
1) Remove the A and B cables from the S33 controller, then cycle the AC power to the computer off and on a few times. The self-test indicator lights should flash and then all go out (See Section 4 for description). If one or more LED's remain on, either the S33 is defective or the backplane wiring is improper. (If all 4 lights remain lit, see Section 4.3.1 for possible missing backplane signals.) When all 4 lights remain lit, the power-up sequence is aborted and the controller will not accept or respond to UNIBUS commands.

If the lights extinguish after 200 milliseconds or so as they should, the principal elements of the S33 will be functioning properly. If the lights remain on, see Figure 4.5.2.1 (the flow diagram) for remedial action.

4.5.2.2 Is the S33 Capable of Generating a Slave Response on the UNIBUS? Are the Emulated RM02 Registers Being Initialized Properly?

1) Do a "BUS INIT" (System Reset) by pressing the INIT button or by pressing START with the HALT switch down. Place a 776700 in the Memory Address Register, then read back each location up to and including 776746, comparing each register to the "no drive connected" data in Table 4.5.1. If the data comes back wrong or if bus timeouts occur, check for possible custom

FIGURE 4.5.2.1 FLOW DIAGRAM



*NEAR Z80 AND 60 PIN CABLE CONNECTOR

TABLE 4.5.1

S33/A REGISTER CONTENTS FOLLOWING POWER ON CONTROLLER RESET AS READ SEQUENTIALLY

Bus Address	Register Designation	Contents w/o Drive	Contents w/Drive Ø
776700	CS1	140200*	4200*
776702	WC	1000	1000
776704	BA	0	0
776706	DA	XXXXXX	XXXXXX
776710	CS2	10100*	100*
776712	DS	0*	10600*
776714	ER1	0	0
776716	AS	0	0
776720	LA	0	0
776722	DB	XXXXXX	XXXXXX
776724	MR1	XXXXXX	XXXXXX
776726	DT	0	020025*
776730	SN	0	0
776732	OF	0	0
776734	DC	0	0
776736	HR	XXXXXX	XXXXXX
776740	MR2	XXXXXX	XXXXXX
776742	ER2	0	0
776744	EC1	0	0
776746	EC2	0	0
776750	---	(Timeout)	(Timeout)

*-Significant Data

X-Indeterminate. Dependent upon emulation ROM revision level

For bit definition summary, see Table 3.2.1 and Section 5.2

address jumpering on the S33 board, faulty backplane wiring, broken backplane connector or dirty connector fingers.

2) Attempt to read all of the emulated RM02 registers from the front panel (or the system keyboard if the CPU has the On-Line Debugging Tool (ODT) feature). The drive cables should be disconnected.

4.5.2.3 Can the Emulated Registers be written into?

Attempt to write the Word Count Register by depositing into and then reading back from address 776702.

1) Deposit all 1's (177777) into WC, then read it back. Repeat with all zeros. Any missing bits or bus timeout could mean poor seating of board, dirty board fingers, faulty backplane connector

Only certain bits in certain registers may be written into, so that writing into registers other than WC may produce confusing results. Modification of some registers causes the contents of other registers not addressed to change also as a result of the emulation process.

4.5.2.4 Can the S33 Communicate with a Drive and Determine its Status?

1) Connect a single drive to the S33 controller via A and B cables. Make sure that pin orientation is correct and that the "A" cable is terminated at the drive end. Insert a "UNIT 0" button into the front of the drive. Install a scratch pack, bring drive up to speed; issue a system reset from the CPU front panel. The DRIVE PROTECT switch should be OFF.

Repeat the examination of RM02 emulated registers per 4.5.2.2, this time comparing the data with the "drive connected" data of Table 4.5.1. Data should be in agreement. If not, the differences should provide a clue to the trouble. Of particular interest is Drive Status (DS) Register, in which bit 7 set indicates that the drive is ready and bit 12 shows that the medium is on line. (See Section 5.2)

4.5.2.5 Is S33 Capable of Completing a Disk Operation (Does Controller Sense Index and Sector Pulses of Selected Disk? Can Controller Operate in the Backplane's NPR Facility?)

With a formatted pack loaded, perform the following test:

1) Write location 776710 with a 40 to clear controller (status and buffer address).

2) Zero main memory locations 0-20$_8$ to provide a buffer space.

3) Write location 776702 with a 177770 to produce a word count of 8 decimal.

4) Write location 776706 with a zero to clear the DISK ADDRESS.

5) Write location 776700 with a 23 to set the VOLUME VALID bit and allow disc transfers.

6) Write location 776732 with a 10000 to set "16 bit mode" header bit.

7) Key this program into memory starting at location 10000:

```
10000   12737      71     776700    ;MOVE 71 COMMAND (READ) TO CSR1
10006    777                         ;LOOP AT 10006
```

8) Start computer at location 10000.

9) Halt computer and examine CS1 at 776700. Status should read 4270 if no error occurred. A 1 in bit 15 indicates that an error was detected, while a 1 in bit 0 (XX71) means that the GO bit is still set and the command never executed. If bit 15 has set, the error bits in the other registers can be examined to better determine the nature of the failure.

10) If the Read was successful, the 8 words transferred should reside in locations 0-16 of main memory and may be examined from the front panel.

11) Writes and Write Checks can be performed by placing 61 or 51 at location 10002, respectively. If the pack is initially unformatted, a WRITE HEADER AND DATA command (63) will have to be performed first.

The buffer space will have to be set up as follows prior to issuing the command:

Location	Data	
000000	150000	;RM02 FORMAT BITS, HEADER WD 1
2	000000	;RM02 HEADER WD 2
4-14	000000	;DATA WORD 1-6

The use of format commands in this test may require that the pack be reformatted later. Pack Formats other than RM02 require different header words.

Failing of the GO bit to clear is usually caused by a missing servo clock (B Cable) or missing sector or index pulses on the A Cable. Cable or drive faults could cause this. UNIBUS timeout under NPR facility will cause bit 11 of CS2 (776710) to set.

4.5.2.6 If any of the tests of Section 4 fail, it may become necessary to employ an oscilloscope to find the fault. This is especially true if cable problems are suspect and there is only one set of cables at the site.

All signals in the SMD interface are current differential. When terminated with 100 ohms to ground the + side of an asserted signal will read 0 volts and the - side will read approximately -.8 volts. With a negated signal, the reverse is true. An unterminated line reads approximately -5 volts regardless of logic state.

If a "B Cable" is suspect, the cable may be disconnected at the controller end and scoped with a probe terminated to ground with 100 ohms. All of the B Cable lines are active whether their drive is selected or not and the signals, particularly the servo and read clocks, should be present all the time. The waveform should be sloped but not ragged and appear on both the + and - sides of the line, 180 degrees out of phase. The "selected" line should pulse periodically as the drive is selected and its status polled by the firmware.

The "A" cable lines are driven mostly by the controller and probing should be done at the drive end. Exceptions to this are the INDEX and the SECTOR signals, which are gated with UNIT SELECTED and come from the drive.

The most satisfactory method of proving the integrity of an A or B Cable is to "ring it out" with an ohmmeter or buzzer. Pin configuration tables appear as Figures 3.3.1 - 3.3.5. Continuity of the shield drain on pin 1 of the "B Cable" should also be verified.

It should be pointed out that a relatively high percentage of system failures have been attributed to defective flat cables, regardless of their source of manufacture. The user should have his cables checked thoroughly (or replaced) before calling the drive or controller manufacturer to task.

4.5.2.7 Functional Testing of the S33 System
Will the System Format a Pack?

1) Load DEC CZRMACØ RM03/RM02 Formatter Program into the computer memory and execute. Error reports may be somewhat ambiguous and do not readily substitute for the previous procedures. The operating procedure is a part of this program's listing.

4.5.2.8 Will the System Transfer Data?

1) Load DEC CZRMBBØ RM03/RM02 Performance Exerciser and run. If the program indicates that no drives are on line, be sure that a Unit Select button from 0 to 3 is installed in the drive. If diagnostic cannot find the drive, it will not proceed further.

As the program executes, errors of various types may be reported. Some of these may be caused by bad areas of the pack; others may be related to drive head alignment. Poor grounding of the drive chassis to the CPU chassis may cause various types of intermittent "soft" errors.

If errors are logged during this test, the frequency and nature of the errors will determine whether the system is operating at an acceptable performance level. Substitution of disk packs, drives and controllers is about the only method which will enable the user to isolate the trouble down to a particular assembly. Errors which appear at the same disk address on multiple passes of the diagnostic are typical of disk pack problems. A good system with an error-free pack can be expected to run overnight with zero errors detected by this program.

4.5.2.9 Troubleshooting Flow Chart

The flow diagram of Figure 4.5.2.1 summarizes the steps which should be used to try to isolate system problems before any vendors are contacted. Data collected during this procedure (essentially the same as previously described) will be important to the resolution of the difficulty.

4.6 Non-Standard Vector/UNIBUS Address Strapping

4.6.1 Vector Address

The standard RM02 UNIBUS Vector is in etch (254_8). The vector address may be altered with etch cuts and jumpers on "E" points.

150.
VECTOR = 254_8

CUT E36
ADD E38
ADD E42

DATA	0	1	0	1	0	1	1	0	0
DATA BIT #	8	7	6	5	4	3	2	1	0
	Fixed	E38 E39	E36 (E37	E32 E33	E34 (E35	E40 E41	E42 E43	Fixed	Fixed

JUMPERS IN ETCH

JUMPER INSTALLED = 0
JUMPER REMOVED = 1

The following is an optional vector address:

VECTOR = 320_8

DATA	0	1	1	0	1	0	0	0	0
DATA BIT #	8	7	6	5	4	3	2	1	0
	Fixed	E38 E39	E36 ≠E37	E32 (E33	E34 ≠E35	E40 (E41	E42 (E43	Fixed	Fixed

(= Install Jumper

≠ = Cut Etch/Remove Jumper

4.6.2 UNIBUS Address

The standard RM02 UNIBUS address is in etch (776700_8). This address may be altered by etch cuts and jumpers on "E" points. The following is an example of the standard and an optional address.

776300

BASE ADDRESS = 776700_8

ADDRESS	1	1	1	1	1	1	1	1	0	1	1	1	0	X	X	X	X	X
ADDRESS BIT #	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOT ALTERABLE (E3 E4 (E1 E2 (E9 E10 E5 E6 (E15 E16 (E7 E8 (E13 E14 E11 E12 REGISTER ADDRESS

776300 = CUT E15

THESE JUMPERS ARE NORMALLY IN ETCH FOR S33/A

JUMPER INSTALLED = 1
JUMPER REMOVED = 0

BASE ADDRESS = 761300_8

ADDRESS	1	1	1	1	1	0	0	0	1	0	1	1	0	X	X	X	X	X
ADDRESS BIT #	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

*E3 *E4 *E1 *E2 (E9 *E10 (E5 *E6 (E15 *E16 (E7 *E8 (E13 E14 E11 E12

(= ADD JUMPER

* = CUT ETCH/REMOVE JUMPER

UNIBUS ADDRESS OPTION

5.0 PROGRAMMING

5.1 Command Codes

Software initiates operations by selecting a drive, loading the control register with a function code and setting the GO bit. The function code specifies the command to be executed upon assertion of the GO bit. The commands can be divided into three categories: positioning commands, data transfers, and housekeeping operations. These commands and their corresponding octal functions are listed below.

Positioning Commands	Function Codes (Octal)
Seek	5
Recalibrate	7
Offset	15
Return to Centerline	17
Search	31

Data Transfer Commands	Function Codes (Octal)
Write Check Data	51
Write Check Header and Data	53
Write Data	61
Write Header and Data (Format)	63
Read Data	71
Read Header and Data	73

Housekeeping Operations	
No-Op	1
Drive Clear	11
Release	13
Read-In Preset	21
Pack Acknowledge	23

5.1.1 Positioning Commands

Positioning commands are used by the software to position the heads over the disk pack.

Seek* - Causes the heads to be moved to the cylinder address specified by the desired cylinder register (RMDC). The current cylinder equals the desired cylinder upon the completion of the command.

Recalibrate* - Positions the heads over cylinder zero.

Offset* - Allows the heads to be moved off the track centerline 200 microinches toward the spindle (positive offset) or away from the spindle (negative offset).

Return to Centerline* - Returns the heads to track centerline after an offset operation.

Search - A Seek command combined with a search for the desired sector address. Used to synchronize software with the desired disk address.

*Since the S33/A utilizes a daisychained control cable to the disk drives, positioning commands for one drive cannot be executed concurrently with data transfers to or from another drive. Therefore, the Seek, Recalibrate, Offset, and Return to Centerline commands are simulated logically with proper status for the software, but the physical positioning is deferred and completed with the next search or data transfer command. Recalibrate functions are completed automatically by the S33/A whenever a drive fault or seek error is encountered.

5.1.2 Data Transfer Commands

These commands transfer data to or from the disk and require the completion of a positioning command or an implied seek as part of the data command.

Read Header and Data - Transfers two words of header information and 256 data words per sector from the disk pack to the PDP-11. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred.

Read Data - Transfers 256 data words per sector from the disk pack to the PDP-11. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred.

Write Check Header and Data - Compares two words of the header and 256 words of data per sector from the disk to 258 words of data per sector from memory. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred or compared.

Write Check Data - Compares 256 words of data per sector from the disk to 256 words of data per sector from memory. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred or compared.

Write Data - Transfers 256 words of data per sector to the drive. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred.

Write Header and Data - Also referred to as a "format", this command writes all gaps, headers, and data for specified sector(s) including the sync byte, CRC, and ECC.

5.1.3 Housekeeping Commands

These commands are used to place the drive logic into a known or initial state.

No-Op - Resets the GO bit. Considered a filler command.

Drive Clear - Clears bits in the following registers:

Status (RMDS)	Bit 14 (ERR) Bit 15 (ATA)
Error No. 1 (RMER1)	All Bits
Error No. 2 (RMER2)	All Bits
Attention Summary (RMAS)	All Bits (for the selected drive)
Maintenance No. 1 (RMAS)	All Bits
ECC Pattern (RMEC2)	All Bits

The drive clear command also clears all error indications in the drive provided the error condition no longer exists.

Release - Logically releases the dual-ported drive for use by the other port. The S33/A physically releases the drive upon completion of each command which required a drive selection for execution. Therefore the Release command is a logical emulation of a function previously completed.

Read-In Preset - Sets the volume valid (VV) bit (06) in the status register (RMDS), clears all bits in the desired sector/track address register (RMDA) and all bits in the desired cylinder address register (RMDC); clears the offset

mode and the following bits in the offset register (RMOF):

OFD (Bit 07) - Offset Direction
HCI (Bit 10) - Header Compare Inhibit
ECI (Bit 11) - Error Correction Code Inhibit
FMT16 (Bit 12) - Format

Pack Acknowledge - Sets the volume valid (VV) bit (06) in the status register (RMDS). This command must be issued before any data transfer or positioning commands can be given if the drive has gone off-line and then on-line (i.e., if MOL changes state). It is primarily intended to avoid unknown pack changes.

5.2 Controller Registers

Twenty registers are visible to software and emulated by the controller to communicate control commands, status data, error conditions, and maintenance information. See Table 5.2.1.

Specific bit locations in these drive registers are designated as follows:

- Read Only indicates that software can read the bits, but cannot load them.
- Write Only indicates that software can load the bits, but will read back a zero.
- Read/Write indicates that software may load and read the bits back.

Table 5.2.1 and the paragraphs that follow define these registers their mnemonics, their UNIBUS addresses, whether they are Read Only or Read/Write, and their basic function.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMCS1 (776700) 00	SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO	R/W
RMWC (776702) RH	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 9	WC 8	WC 7	WC 6	WC 5	WC 4	WC 3	WC 2	WC 1	WC 0	R/W
RMBA (776704) RH	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 9	BA 8	BA 7	BA 6	BA 5	BA 4	BA 3	BA 2	BA 1	BA 0	R/W
RMDA (776706) 05	0	0	0	TA 16*	TA 8*	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1	R/W
RMCS2 (776710) RH	DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0	R/W
RMDS (776712) 01	ATA	ERP	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	0	OM	R
RMER1 (776714) 02	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF	R/W
RMAS (776716) 04	0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0	R/W
RMLA (776720) 07	0	0	0	0	0	SC 16	SC 8	SC 4	SC 2	SC 1	0	0	0	0	0	0	R
RMDB (776722) RH	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	R
RMMR1 (776724) 03	OCC	R/G	EBL	REX	ESRC	PLFS	ECRC	PDA	PHA	CONT	WC	EECC	WD	LS	LST	DMD	R
	DBCK	DBEM	DEBL	MSEN	MCLK	MRD	MUR	MOC	MSER	MDF	MS	DTG	MWP	MI	MSC	DMD	W

*RESERVED

REGISTER SUMMARY, RM02 EMULATION

TABLE 5.2.1

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMDT (776726) 06	0	0	MOH 1	0	DRQ	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	R
RMSN (776730) 10	SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	R
RMOF (776732) 11	0	0	0	FMT 16	ECI	HCI	0	0	OFF DIR	0	0	0	0	0	0	0	R/W
RMDC (776734) 12	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	R/W
RMHR (776736) 13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W
RMMR2 (776740) 14	RQA	RQB	TAG	TEST BIT	CIC	CIH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	R
RMER2 (776742) 15	BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0	R/W
RMEC1 (776744) 16	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	R
RMEC2 (776746) 17	0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	R

REGISTER SUMMARY (Continued)

TABLE 5.2.1

5.2.1 Control Register (RMCS1) (776700)

This register is utilized by the controller to store the disk commands and operational status. The function (command) code designates a function for the drive selected in bits 00 through 02 of the RMCS2 register. Setting the GO bit causes the controller to execute the function code in the control register.

Bits 00-05 GO and Function (GO, F0-04) - Read/Write

GO bit and F0-F4 establish the function (command) code control bits that determine the action performed by the controller as shown below.

F4	F3	F2	F1	F0	GO	Octal	
0	0	0	0	0	1	01	No Operation
0	0	0	1	0	1	05	Seek Command
0	0	0	1	1	1	07	Recalibrate
0	0	1	0	0	1	11	Drive Clear
0	0	1	0	1	1	13	Release (Dual-Port Operation)
0	0	1	1	0	1	15	Offset Command
0	0	1	1	1	1	17	Return to Centerline
0	1	0	0	0	1	21	Read-In Preset
0	1	0	0	1	1	23	Pack Acknowledge (Set V.V.)
0	1	1	0	0	1	31	Search Command
1	0	1	0	0	1	51	Write Check Data
1	0	1	0	1	1	53	Write Check Header and Data
1	1	0	0	0	1	61	Write Data
1	1	0	0	1	1	63	Write Header and Data
1	1	1	0	0	1	71	Read Data
1	1	1	0	1	1	73	Read Header and Data

The GO bit (bit 0) must be set to cause the controller to respond to a command. The GO bit is reset after command execution. All other commands are illegal (ILF).

Bit 06 Interrupt Enable (IE) - Read/Write

IE is a control bit that can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled. A program-controlled interrupt may occur by writing 1's into IE and RDY at the same time.

Bit 07 Ready (RDY) - Read Only

This bit is normally set except during data transfers when it is reset. When a data transfer command code (51-73) is written into RMCS1, RDY is reset. At the termination of the data transfer, RDY is set.

Bits 08-09 UNIBUS Address Extension (A16,A17) - Read/Write

Upper extension bits of the RMBA register. Cleared by INIT, controller clear, or by writing 0's in these bit positions. These control bits cannot be modified while the controller is performing a data transfer (RDY negated).

Bit 10 Port Select (PSEL) - Read/Write

When PSEL = 0, data transfer is via UNIBUS A. Cleared by UNIBUS INIT, controller clear, or by writing a 0 in this bit position. The controller only supports Port A operation; therefore, the bit must be 0 and, in addition, cannot be modified while the RH controller is performing a data transfer (RDY negated).

Bit 11 Drive Available (DVA) - Read Only

This bit is used in dual-port disk configurations and set when the drive is not busy on the other port.

Bit 12 Spare

Bit 13 MASSBUS Control Bus Parity Error (MCPE) - Read Only

Set when a simulated parity error is forced by a diagnostic while reading a register logically located in the drive. Cleared by UNIBUS INIT, controller clear, RH error clear, or by loading a data transfer command with the GO bit set.

Simulated parity errors while writing a register logically located in a drive cause the PAR error (RMER1 register, Bit 03) to set.

Bit 14 Transfer Error (TRE) - Read/Write

Set if any of the following conditions occur:

- o Data Late (RMCS2 Bit 15 is set)
- o Write Check Error (RMCS2 Bit 14 is set)
- o UNIBUS Parity Error (RMCS2 Bit 13 is set)
- o Non-Existent Drive (RMCS2 Bit 12 is set)
- o Non-Existent Memory (RMCS2 Bit 11 is set)
- o Program Error (RMCS2 Bit 10 is set)
- o Missed Transfer (RMCS2 Bit 9 is set)
- o Simulated MASSBUS Data Bus Parity Error (RMCS2 Bit 8 is set)
- o Drive Error occurs during a Data Transfer

Cleared by UNIBUS INIT, controller clear, or by loading a data transfer command with GO bit set.

Bit 15 Special Condition (SC) - Read Only

Set by TRE or ATTN or MCPE bits. Cleared by UNIBUS INIT, controller clear, or by removing the ATTN condition.

5.2.2 Word Count Register (RMWC) (776702)

The word count register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory. A maximum of 65,535 words can be transferred at one time. It is cleared only by writing zeros into it.

5.2.3 Address Register (RMBA) (776704)

This register is used by the controller to address the memory location in which a transfer is to take place. The register contains the lower 16 bits of address which combine with Bit 09 and 08 of the control register RMCS1 to create the 18-bit memory address. This register is loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (Bus Address Increment Inhibit) bit (bit 03 of RMCS2) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address. It is cleared by a UNIBUS INIT or by controller clear.

5.2.4 Sector/Track Address Register (RMDA) (776706)

This register is used to address the sector and track on the disk to or from which a transfer is desired. The RMDA register is associated with the drive whose unit number appears in bits 00:01 of the status register RMCS2. Before a transfer, the RMDA is loaded by the program with the address of the first block to be transferred. The RMDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred.

The RMDA register contains a 5-bit sector address providing for 32 sectors per data track. The register also contains a 3-bit track address providing for five data tracks. The sector and track addresses are non-contiguous. However, when the sector count fills up with a count of 31, the next word read or written will cause the track address to increment and the sector address to clear. When the sector address and track address reach their full counts, the next word will cause both sector and track addresses to increment to 0 and a mid-transfer seek to occur. The RMDA register can only be loaded with a 16-bit word. Any attempt

to write a byte causes the entire word to be written. Any attempt to write in this register while the drive's GO bit is asserted will cause an RMR (Register Modify Refused) error (RMER1, Bit 02) and the register is not modified.

Bits 00-04 Sector Address - Read/Write

Set by the program to specify the sector on which a transfer is to start. Cleared by read in preset command. Incremented after each sector has been transferred.

Bits 05-07 Spare

Bits 08-12 Track Address - Read/Write

Set by the program to specify the track on which a transfer is to start. Cleared by read in preset command. Incremented when sector 31 is reached.

Bits 13-15 Spare

5.2.5 Status Register (RMCS2) (776710)

This Read/Write register indicates the status of the controller and contains the drive unit number. The unit number specified in Bits 00 and 01 of this register indicates which of the possible four drives is selected.

Bits 00-01 Unit Select - Read/Write

These bits are written by the program to select a drive. Cleared by UNIBUS INIT or controller clear. The unit select bits can be changed by the program during data transfer operations without interfering with the transfer.

Bit 02 Not used by S33. Unit Select 2

Bit 03 Bus Address Inhibit (BAI) - Read/Write

When BAI is set, the controller will not increment the RMBA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by UNIBUS INIT or controller clear.

Bit 04 Parity Test (PAT) - Read/Write

This bit is used by the controller to simulate a MASSBUS Data Bus Parity Error (MDPE) to support diagnostic programs. Cleared by UNIBUS INIT or controller clear.

Bit 05 Controller Clear (CLR) - Write Only

When a 1 is written into this bit, the controller is initialized. UNIBUS INIT also causes controller clear to occur.

Bit 06 Input Ready (IR) - Read Only

Set when a word may be written in the RMDB register by the program. Cleared by reading RMDB register. Serves as a status indicator for diagnostic check of the silo buffer. An attempt to write the RMDB register before IR is asserted will cause a Data Late Error (DLT). Used for diagnostic mode only.

Bit 07 Output Ready (OR) - Read Only

Set when a word is present in RMDB and can be read by the program. Cleared by UNIBUS INIT, controller clear, or by reading the RMDB register. Serves as a status indicator for diagnostic check of the silo buffer. An attempt to read the RMDB register before OR is asserted will cause a Data Late Error (DLT). Used for diagnostic mode only.

Bit 08 MASSBUS Data Bus Parity Error (MDPE) - Read Only

Set When a simulated parity error is forced by a diagnostic while doing a read or write-check operation. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. MDPE causes a transfer error (Bit 14 of RMCS1 sets). Simulated parity errors during write operations are detected by the drive and cause the PAR error (RMER1 register, Bit 03).

Bit 09 Missed Transfer (MXF) - Read/Write

MXF causes a transfer error (Bit 14 of RMCS1 sets). This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive that has ERR (Bit 14 of RMDS set).

Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set.

Bit 10 Program Error (PGE)

Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. PGE causes a transfer error (Bit 14 of RMCS1 sets). The data transfer command code is inhibited from being written.

Bit 11 Non-Existent Memory (NEM) - Read Only

Set when the controller is performing a DMA transfer and the memory address specified in RMBA is non-existent (does not respond to MSYN within 20μs). Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. NEM causes a transfer error (Bit 14 of RMCS1 sets). The RMBA contains the address +2 of the memory location causing the error.

Bit 12 Non-Existent Drive (NED) - Read Only

Set when the program reads or writes a drive register in a drive that does not exist or is powered down. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. NED causes a transfer error (Bit 14 of RMCS1 sets).

Bit 13 UNIBUS Parity Error (UPE) - Read/Write

Set if the UNIBUS parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. UPE causes a transfer error (Bit 14 of RMCS1 sets). When a UNIBUS parity error occurs, the RMBA register contains the address +2 of the memory word with the parity error (if BAI (Bit 03 of this register) is not set). This bit may be set by program control for diagnostic purposes.

Bit 14 Write Check Error (WCE) - Read Only

Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. WCE causes a transfer error (Bit 14 of RMCS1 sets). If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RMBA (and extension) is the address of the word following the one that did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RMDB).

Bit 15 Data Late (DLT) - Read Only

Set only by the program reading or writing the RMDB register. DLT causes a transfer error (Bit 14 of RMCS1 sets). Cleared by UNIBUS INIT, controller clear, or loading a data transfer command GO set. Used for diagnostic mode only.

5.2.6 Drive Status Register (RMDS) (776712)

This Read-Only register contains the various status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bus (00:02) of the RMCS2 register. The register is a Read-Only register. Writing into this register will not cause an error and will not modify any of the status bits.

Bit 00 Offset Mode (OM) - Read Only

Set when an offset command is issued to the controller; reset by any of the following seven actions:

1) Power-Up
2) Mid-Transfer Seek
3) Read-In Preset
4) Write Data or Write Header and Data Command
5) Return to Centerline
6) Writing Desired Cylinder
7) Recalibrate Command

When set and a read command is received, the offset is performed prior to the execution of the read.

Bits 01-05 Spare

Bit 06 Volume Valid (VV) - Read Only

Set by the pack acknowledge or read-in preset commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed. Therefore, the program should not assume anything about the identity of the pack.

Bit 07 Drive Ready (RDY) - Read Only

Set at the completion of every command, data handling, or mechanical motion. Cleared at the initiation of a command. When set, this bit indicates the readiness of the controller to accept a new command involving data handling or mechanical motion of the drive. If a Read or Write command was issued, the setting of the DRY bit will indicate normal termination. If an error was made during the data transfer, the appropriate error bits and Bit 15 (ATA) of this register will also be set.

If a mechanical movement command was issued, the ATA bit will also be set when DRY is set. If an error occurs during the mechanical movement, the appropriate error bits will also be set.

The DRY bit is the complement of the GO bit. (DRY = GO negated) This is true except when the drive is non-existent; then the DRY bit is reset.

Bit 08 Drive Present (DPR) - Read Only

Always set to "one".

Bit 09 Programmable (PGM) - Read Only

In the S33/A controller, this bit will always be reset to "zero".

Bit 10 Last Block Transferred (LBT) - Read Only

After reading or writing sector 31 of cylinder 882 on track 4, the LBT bit is set. With this bit set, the desired cylinder address register contains 823 (illegal address), and the desired sector track address register contains 0. Cleared when a new track or sector address is received. Also cleared during power-up cycle.

Bit 11 Write Lock (WRL) - Read Only

The drive is placed in write protect mode through a manual switch on the drive control panel. When the drive is write protected, any attempt by the operating system to issue a write command to a write-locked device will cause the write lock error (WLE, Bit 11 of RMER1) bit to set. Cleared when the PROTECT switch is not depressed (PROTECT light extinguished).

Bit 12 Medium On-Line (MOL)

After the drive power-up cycle, the heads are positioned over cylinder zero and the MOL bit is set. Whenever the MOL bit changes state (set or reset), Bit 15 (ATA) of this register is also set, except when the heads are unloaded. MOL is cleared when the heads are unloaded.

Bit 13 Positioning in Progress (PIP) - Read Only

Set when a positioning command is accepted. These commands are seek, offset, return to centerline, recalibrate, and search. In addition, PIP is set whenever MOL is reset and drive is powered up. Cleared when the function is completed.

The following chart shows the state of the PIP bit in relation to the type of operation being performed.

Operation	DRY	PIP	ATA at End of Operation (No Error)
No Operation	0	0	NO
Recalibrate	0	1	YES
Drive Clear	0	0	NO
Search	0	0/1	YES
Seek	0	1	YES
Offset	0	0	YES
Write Check	0	0	NO
Write Data	0	0	NO
Write Header and Data	0	0	NO
Read Data	0	0	NO
Head Header and Data	0	0	NO
Implied Seek	0	1	NO
Mid-Transfer Seek	0	1	NO
Return to Centerline	0	0	YES
Pack Acknowledge	0	0	NO
Read-In Preset	0	0	NO
Offset During Read	0	1	NO

Bit 14 Error (ERR) - Read Only

A composite error bit that is the logical OR of all drive error conditions. While ERR is set, only clearing commands are accepted. Set when either of the error registers (RMER1 or RMER2) indicates a drive error. Cleared by drive clear, INIT, writing 0's in error registers or during a power-up cycle.

Bit 15 Attention Active (ATA) - Read Only

Set when a drive attention condition exists as follows:

1. Any error in the error register:
   a) If the GO bit is set; at the completion of the command.
   b) If the GO bit is reset; at the occurrence of the error.
2. At the completion of seek, search, recalibrate, offset, or return to centerline.
3. When the MOL bit changes state.

These conditions are cleared by the following:

1. Drive clear command
2. Writing a 1 into the attention summary register (RMAS)
3. INIT command
4. Writing a 1 into the GO bit if no error condition exists

5.2.7 Error Register No. (RMER1) (776714)

This register contains the error status indicators for the drive whose unit number appears in Bits 00 through 01 of RMCS2. The logical OR of all the error bits in the RMER1 and RMER2 registers will be written into Bit 14 of RMDS.

The RMER1 register is a read/write register and can only be writen as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy (GO bit is asserted), an RMR (RMER1 register, bit 02) error is set and the contents of the RMER1 register are not otherwise modified.

Errors can be classified into two categories: Class A and Class B.

- A Class A error is handled at the completion of a non-data transfer command or, in the case of a data transfer command, at a sector boundary.

- o A Class B error causes the command to terminate immediately or as soon as possible.

Bit 0 Illegal Function (ILF) - Read/Write

ILF is a Class B error set when the GO bit is set, there is no previous error, and the function code in the control register does not correspond to a valid drive command. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 01 Illegal Register (ILR) - Read/Write

ILR is a Class A error set when a read or write is attempted on a register address greater than 17. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 02 Register Modify Refused (RMR) - Read/Write

RMR is a Class A error set when a write is attempted into any register (exept RMAS or RMMR1) while the GO bit is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register. The following registers can be written into before or after an operation, but not during.

- o Control Register
- o Error Registers
- o Maintenance Register No. 1
- o Attention Summary Register
- o Desired Sector/Track
- o Address Register
- o Offset Register
- o Desired Cylinder Address Register

The remaining drive registers are read-only registers. When RMR is set, the drive continues to execute the command in progress.

Bit 03 Parity Error (PAR) - Read/Write

Depending when PAR occurs, it is either a Class A or B error.

- o Class A during a register write
- o Class B if DPE is set

Set when writing into a register if even parity is detected on the UNIBUS lines. Also set when Bit 03 (DPE) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 04 Format Error (FER) - Read/Write

FER is a Class A error during a read header and data command and a Class B error during all other commands.

Set when reading a sector header if Bit 10 (HC1) of RMOF register is reset and Bit 12 of the first header word does not match the state of Bit 12 (FMT) of RMOF register. Cleared by drive clear, INIT, power-up cycle, or writing 0's in this register.

Error usually indicates that pack and drive are incompatible in data word length (e.g., drive configured for 16-bit format and an 18-bit format pack installed). The S33/A controller will not accommodate 18 bit operations.

Bit 05 Write Clock Fail (WCF) - Read/Write

Always a zero.

Bit 06 ECC Hard Error (ECH) - Read/Write

ECH is a Class B error set at the conclusion of the error correction procedure (Bit 15 of this register is set), indicating that the error was an uncorrectable error. Cleared by drive clear, INIT, power-up cycle, or writing 0's into this register.

Bit 07 Header Compare Error (HCE) - Read/Write

HCE is a Class A error during a read header and data command and a Class B error during all other commands.

Set if Bit 10 (HC1) of RMOF register is reset and one or more of the following occurs while reading the header.

- Bits 0-9 of the first header word do not match bits 0-9 of the desired cylinder address register (RMDC).
- Bit 12 of the first header word does not match Bit 12 (FMT) of the offset register (RMOF).
- Bits 0-5 of the second header word do not match bits 0-5 of the desired track and sector (RMDA) register.
- Bits 8-10 of the second header word do not match Bits 8-10 of the desired track and sector (RMDA) register.

- o Bits 14 and 15 must be 1's; otherwise BSE is set.
- o Any bit other than those specified above that is not a zero in either the first or second word of the header.

Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 08 Header CRC Error (HCRC) - Read/Write

HCRC is a Class A error during a read header and data command and a Class B error during all other commands. Set if Bit 10 (HC1) of RMOF is reset and the CRC register in the controller is not zero after the complete header has been read. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 09 Address Overflow Error (AOE) - Read/Write

AOE is a Class B error set when the controller requests a data transfer (read or write) beyond the last sector of the last cylinder of the pack. This results in a cylinder address overflow condition. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 10 Invalid Address Error (IAE) - Read/Write

IAE is a Class B error which causes the command to terminate when the GO bit sets. Set if the contents of either desired cylinder register (RMDC) or desired sector/track address register (RMDA) are invalid and at the receipt of one of the following commands.

- o Seek
- o Search
- o Read Header and Data
- o Read Data
- o Write Check Header and Data
- o Write Check Data
- o Write Header and Data
- o Write Data

Invalid addresses are: desired cylinder greater than 822; desired track greater than 4; desired sector greater than 31. Cleared by drive clear, INIT, power-up cycle or by writing 0's into this register.

Bit 11 Write Lock Error (WLE) - Read/Write

WLE is a Class B error set if a write command is issued when the drive is in the write lock mode. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 12 Drive Timing Error (WTE) - Read/Write

DTE is a Class B error which is not fully emulated. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 13 Operation Incomplete (OPI) - Read/Write

OPI is a Class B error set if either of the following occurs:

1. During a Search command, the correct sector is not located within three revolutions of the disk.
2. If MOL is reset and a command is attempted, it will not execute.

Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 14 Unsafe Drive (UNS) - Read/Write

Set when Bit 07 (DVC) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 15 Data Check Error (DCK) - Read/Write

DCK is a Class A error if Bit 11 (ECI) of RMOF is set and a Class B error if ECI is reset. Set after reading the entire data field of the sector if the ECC register bits 11-31 are non-zero. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

5.2.8 Attention Summary Register (RMAS) (776716)

The Attention Summary Register allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention status for a selected group of drives. The bit displayed in each of the four low-order positions of this register is identical to the ATA bit displayed in RMDS for the corresponding drive. When

fewer drives are attached to the controller, the bits corresponding to the missing drives are always 0.

The ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. (Loading a 0 has no effect.) This allows the program to inspect the RMAS register and later to rest the ATA bits that were set without accidentally resetting other ATA bits that may have become set in the meantime.

This register can be read or written at any time, regardless of whether any particular drive is busy. Note that the controller never asserts ATA during the execution of a command.

Bits 00-07 Attention Active (ATA 00-03) - Read/Write

The ATA bit for each drive is displayed in Bit 15 of RMDS for that drive and in the bit position corresponding to the unit number, e.g., the ATA bit for drive 02 corresponds to bit position 02 in RMAS.

Each bit sets when the corresponding ATA in RMDS is asserted. All bits are cleared by INIT or drive clear. Individual bits are cleared by writing function code with the GO bit to the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.

Bits 04-15 Not Used.

5.2.9 Look-Ahead Register (RMLA) (776720)

This Read Only register contains a simulation of the sector number currently positioned under the heads. This value is represented as a binary number in bit locations 6-10, where bit 6 is the LSB. The maximum count is 31.

Bits 00-05 Not Used. Always read as 0's.

Always read as 0's.

Bits 06-10 Sector Count (SC1,2,4,8,16) - Read Only

Simulates the sector number currently under the heads.

Bits 11-15 Not Used.

Always read as zeros.

5.2.10 Data Buffer Register (RMDB) (776722)

This Read/Write register is used to monitor the data buffer in the controller. If the program attempts to write into the data buffer while it is full or read the data buffer when it is empty, a data late (DLT) error occurs (Bit 15 of RMCS2 is set). The RMCS2 register also provides status indicators showing whether the data buffer can be read or written. When RMCS2 Bit 6 (IR) is set, the data buffer can be written. When RMCS2 Bit 7 (OR) is set, the data buffer can be read.

The RMDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the RMDB register is a "destructive" readout operation: the top data word in the buffer is removed by the action of reading the RMDB and a new data word (if present) replaces it a short time later. The action of writing the RMDB register causes one more data word to be inserted into the buffer (if it was not full).

Bits 00-15 Data Buffer (DB) - Read/Write

Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the data buffer is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data word read from the disk that did not compare with the corresponding word in memory is frozen in RMDB for examination by the program.

5.2.11 Maintenance Register No. 1 (RMMR1) (776724)

The emulation of the RMMR1 register in the S33/A provides a subset of the maintenance and diagnostic functions of the RM02. The register has two distinct 16-bit sections: a Read Only section and a Write Only section.

The Write Only section can be written only after the controller is set in the maintenance mode of operation (bit 00 set). The Read Only section can be read in both normal and maintenance operational modes.

Bit 00 Diagnostic Mode (DMD) - Read/Write

Set by a diagnostic program to configure the controller in the maintenance mode. Must be set before any other RMMR1 bits can be written. Cleared by drive clear, INIT, or power-up cycle. Also, when cleared, resets Bits 01-15 of this register.

Bits 01-15 Not Emulated

5.2.12 Drive-Type Register (RMDT) (776726)

This Read Only register allows the program to distinguish between different classes of drives. The value returned (20024) by the S33/A controller defines the drive as a single-ported RM02. Implementation of the dual-port capability is transparent to the software.

Bits 00-08 Drive Type (DT) - Read Only

This 9-bit field contains a unique number assigned to each device type. This field contains a 024_8.

Bits 09,10 Not Used. Always zeros.

Always zeros.

Bit 11 Drive Request Required (DRQ) - Read Only

The status of this bit indicates the availability of the dual-port option. The S33/A returns a zero (single port). Dual por is handled by the drive. Controller will wait until the drive is not busy.

Bit 12 Not Used. Always zeros.

Bit 13 Moving Head (MOD) - Read Only

Since the RM02 is a moving head device, this bit is returned in the 1 state.

Bits 14,15 Not Used.
Always zeros.

5.2.13 Serial Number Register (RMSN) (776730)

This Read Only register permits the program to distinguish between drives connected to the same controller. This information is useful during error logging of on-line software diagnostics to allow errors to be associated with a particular drive.

The serial number register in the S33/A is actually the logical unit number selected by software.

Bits 00-01 Serial Number (SN) - Read Only

These bits reflect the logical unit number of the drive currently selected by software.

Bits 02-15 Not Used.

Always zeros.

5.2.14 Offset Register (RMOF) (776732)

The controller has the ability to offset the drive carriage approximately 200 microinches from the track centerline in either direction.

The positioner offsetting information is supplied to the controller directly from the software operating system prior to the issuance of the offset command.

Bits 00-06 Not Used.

Always zeros.

Bit 07 Offset Direction (OFD) - Read/Write

Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle. The offset direction bit is valid if the following three conditions are met:

1. Read command is loaded into control register (RMCS1) (Bits 0-5).
2. RMCS1 GO bit is set.
3. Offset mode bit (RMDS Bit 00) is set.

Cleared by Read-In Preset command or a software write to this register.

Bit 10 Header Compare Inhibit (HCI) - Read/Write

Set by the software program to inhibit the reporting of header compare errors FER, HCE, and HCRC (Bits 4, 7, and 8 respectively of RMER1). Cleared by a Read-In Preset command or by a software write to this register. The meaning of the HCI bit is valid in both the Read and Write commands. It is strongly recommended, however, that the HCI bit be reset during a Write operation.

Bit 11 Error Correction Inhibit (ECI) - Read/Write

Set by the software to prevent the isolation and correction of a data check error. Cleared by a Read-In Preset command or by a software write to this register.

If a data error is detected at the end of the data transmission in the Read mode with the ECI bit reset, the controller goes into the ECC correction process at the end of the sector. Prior to beginning the correction routine, the device will also set the data check (DCK) error bit RMER1 Bit 15, which will remain set until a drive clear command or an INIT pulse is received.

When the results of the error correction process are available, the device will place the error pattern and the location of the error pattern within the data field in the appropriate ECC registers.

If the error was non-ECC-correctable, the drive will also set the ECC hard error (ECH) bit. If the ECI bit is set, the error correction process will be inhibited. The termination procedure will be done normally as if no data error occurred. Only the DCK bit will be set as soon as a data error is detected. This bit will remain set until a Drive Clear or an INIT pulse is received.

Bit 12 Format (FMT) - Read/Write

Set to a 1 when 16-bit/word format is used (16 bits/word x 256 words/sector). Set to a 0 when 18-bit/word format is used (18 bits/word x 256 words/sector). Cleared by read-in preset command or by software write to this register. This bit is used by the S33/A only to achieve compatibility with diagnostic programs. All data operations to the disk are in 16 bit format.

Bits 13-15 Not Used.
Always zeros.

5.2.15 Desired Cylinder Register (RMDC) (776734)

The Read/Write register contains the address of the cylinder to which the drive carriage moves the heads for a Seek, Search or Data Handling command. Since the maximum number of cylinders in the RM02 is 823, only 10 bits are necessary to specify the desired cylinder address.

Bits 00-09 Desired Cylinder (DC) - Read/Write

Set by the program, the cylinder number to which the head will move. Bit DC1 is the least significant bit and bit DC512 is the most significant bit. Cleared by read-in preset. The invalid address error bit (RMER1 Bit 10) sets when, upon asserting the GO bit, the contents of the desired cylinder contain an address larger than 822.

Bits 10-15 Not Used.

Always zero.

5.2.16 Holding Register (RMHR) (776736)

This is an addressable register with no drive function. It is used only by diagnostic software. When writing into this register, all bits remain unchanged and new information is lost. When reading this register (or any illlegal register), the complement of the register contents is read. Whenever writing any legal register, this holding register is concurrently written.

5.2.17 Maintenance Register No. 2 (RMMR2) (776740)

The RMMR2 register operates in conjunction with the Maintenance Register No. 1. No bits of RMMR2 are emulated in the S33/A controller.

Bits 00-15 Not Used.

Always zeros.

5.2.18 Error Register No. 2 (RMER2) (776742)

This Read/Write register contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive. Whenever any of the bits in this register are set, the ERR bit (Bit 14) in the status register (RMDS) is set and the ATA bit in the RMAS register is set. All Error Register No. 2 errors are considered "catastrophic" errors.

All error bits reset when a drive clear command or an INIT pulse is received. If the heads are retracted from the disk pack upon receiving a drive clear or an initialize pulse, the drive attempts to reload the heads unless the error persists. Errors are classified into two categories: Class A and Class B.

- o A Class A error is handled at the completion of a non-data transfer command, or in the case of a data transfer command, at a sector boundary provided the Run line is inactive.
- o A Class B error is handled immediately and causes the immediate termination of a command or a termination as soon as possible.

Bits 00-02 Not Used.

Bit 03 Data Parity Error (DPE) - Read/Write

Set during either a Write data or Write Header and Data command if the UNIBUS data bus parity is even. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register. When DPE sets, it also causes bit 3 of RMER1 to set. DPE is a Class B error.

Bits 04-06 Not Used.

Always zeros.

Bit 07 Device Check (DVC) - Read/Write

Set to indicate either or both of the following drive errors occurred: DC power fault or head select fault. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this

register. DVC is a Class B error.

Bits 08,11 Not Used.
Always zeros.

Bit 12 Invalid Command (IVC) - Read/Write

Set when the volume valid (RMDS Bit 6) is reset or unit ready is not active and any command other than read-in preset or pack acknowledge is received. Also set if Drive Clear or NO-OP is received. Cleared by INIT, power-up cycle, or by writing 0's into this register. IVC is a Class B error.

Bit 13 Not Used
Always zeros.

Bit 14 Seek Incomplete (SKI) - Read/Write

Set by the controller upon a drive fault or a seek incomplete status from the drive. Cleared by either a drive clear or INIT, then a recalibrate command.

Due to a positioner malfunction, it is possible for the Seek not to complete. The controller will do the following:

- o Set the SKI bit (RMER2, Bit 14)
- o Set the ATA bit (RMDS, Bit 15)
- o Reset the PIP bit (RMDS, Bit 13)
- o Set the RDY bit (RMCS1, Bit 7)
- o Set the UNS bit (RMER1, Bit 14)

This indicates to the software that the Seek operation did not complete and the exact positioner location is unknown.

Bit 15 Bad Sector Error (BSE) - Read Only

Set whenever the controller detects a 0 in Bit 14 or 15 of the first header word. A bad sector is indicated when these bits are cleared. This is a Class B error which causes termination of a read command after checking the CRC word. In the case of a read header and data command, this is a Class A error. Cleared by a Drive Clear or INIT.

5.2.19 ECC Position Register (RMEC1) (776744)

The controller has Error Correction Code (ECC) capabilities that detect and correct errors by reconstructing a portion of the data. In the specified code word length, the ECC code corrects an error that falls within an 11-bit burst. Any errors outside the specified burst length are detected but not corrected. The ECC hardware, in this case, yields an ECC uncorrectable error (Bit 6 of RMER1 sets). The controller contains the hardware to find the burst in which the read error is included and to determine the exact location of the burst within the data field.

The ECC pattern register (RMEC2) contains the actual error burst and the ECC position register (RMEC1) contains the address that determines the actual location of the error burst within the data field.

NOTE: The actual correction of the data field is done by the software with the help of the ECC position and ECC pattern registers.

Bits 00-12 ECC Position (POS) - Read Only

Set by the ECC logic if a data check error occurred (Bit 15 of RMER1 is set) during a data transfer command and the error detected is determined to be correctable (Bit 6 of RMER1 is reset).

The 13 position bits establish the binary address of the first bit of the error burst within the data field. The maximum valid address is 4128. If the ECC logic determines that the error is a non-correctable hard error (Bit 6 of RMER1 is set) or if the ECI bit (RMOF Bit 11) is set, the contents of this register are irrelevant.

Bits 13-15 Spare

5.2.20 ECC Pattern Register (RMEC2) (776746)

This Read Only register is used in conjunction with the ECC position register (RMEC1) and contains the actual error burst available at the completion of the ECC process. The software

uses the contents of the ECC position register to find the actual location of the error burst in the data field. Then the error burst itself determines the bits in error within the 11-bit field.

Bits 00-10 ECC Pattern (PAT) - Read Only

Set by the ECC logic if the detected error is correctable. The 11 pattern bits establish the error burst. Cleared by drive clear or INIT. If the ECC logic determines that the error is a non-correctable hard error (Bit 6 of RMER1 is set) or the error correction inhibit bit (RMOF Bit 11) is set, the contents of this register are irrelevant.

Bits 11-15 Spare

5.3 Error Correcting Coce (ECC)

The S33/A contains ECC logic capable of detecting errors in the data read from disk and providing information to the software to permit data recovery. The ECC code employed locates an error that falls within an 11-bit burst. An uncorrectable error includes any error field larger than an 11-bit burst and isolated dropped bits (for example, one bit in word 0 and one bit in word 225). The S33/A indicates ECC uncorrectable errors to the software by setting the ECC hard error bit (ECH) in Error Register No. 1 (RMER1). The ECC logic performs the following functions:

1. Finds the 11-bit burst where the read error is located.
2. Determines exact location of the burst within the data field.

This error information is provided to software through 2 registers:

1. ECC Pattern Register (RMEC2) - Contains the actual 11-bit correction mask.
2. ECC Position Register (RMEC1) - Contains the location of the first bit of the error burst within the 4128 bit data field.

The actual correction of the error is done by operating system software using the data contained in these two registers. In the event of a hard ECC error, the contents of the ECC pattern and ECC position registers are of no significance.

6.0 THEORY OF OPERATION

The theory of operation of the S33 and its interface to the disk drive is explained in detail in the following paragraphs.

6.1 Disk Interface

The controller has a industry standard SMD interface utilizing Motorola 3450 and 3453 differential transmitters and receivers. These circuits provide a terminated, balanced transmission system and allow disk operation at radial distances up to 50 feet and daisychain distances up to 100 feet from the controller.

The "A" cable is twisted pair, flat ribbon cable which allows mass termination to the "A" cable connector without stripping. The "B" cable is a flat ribbon cable with a ground plane and drain wire which allows mass termination without stripping.

6.1.1 "A" Cable

1) Characteristics

Type: 30 twisted pair, flat cable
Impedance: 100 ±10 ohms
Wire Size: 28 AWG, 7 strands
Propagation Time: 1.6 to 1.8 ns/ft.
Maximum Cable Length: 100-ft. cumulative
Voltage Rating: 300V rms

2) Components

Item	CDC P/N	AMP P/N	3M P/N
Connector (60 Position)	94384514	88012-2	3334-6060
Flat Cable (Twisted Pair) 30 pair 28 AWG	95047400	---	SS-455-248-60

3) Mating Receptacle on Controller

Item	3M P/N
60 Pin, Right Angle Header	3372-1002

4) Termination

Termination of the differential signals is provided by the terminator assembly installed on the last disk in the daisy-chain. See Figure 2.1.

6.1.2 "B" Cable

1) Characteristics (with ground plane)

Type: 26 conductor flat cable with ground plane drain wire
Impedance: 130 ±15 ohms (3M P/N 3476/26)
Wire Size: 28 AWG - 7 strand
Propagation Time: 1.65 ns/ft. (nominal)
Maximum Cable Length: 50 ft.
Voltage Rating: 300V rms

2) Components

Item	CDC P/N	AMP P/N	3M P/N
Connector (26 position)	9438-507	86905-2	3399-3000
Flat Cable (26 position) w/ground plane & drain wire	95028509	---	3476/26

3) Mating Receptacle on Controller

Item	3M P/N
26 Pin, Right Angle Header	3493-1002

4) Termination

Termination of the differential signals is provided at the receiving end of the signal on either the controller or the SMD's logic receiver end as appropriate.

6.1.3 Signal Descriptions "A Cable"

6.1.3.1 Address and Control Bus

Address and Control functions are transferred on a 10-line bus labeled Bit 0 - Bit 9. See Figures 3.3.1 and 6.1.1.

6.1.3.2 Cylinder Address

The controller places the cylinder address on the bus lines and strobes the lines with Tag 1. The unit must be On Cylinder before Tag 1 is sent.

6.1.3.3 Head Select

The controller places head address on the bus lines and strobes the lines with Tag 2.

BUS	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD SELECT	TAG 3 CONTROL SELECT	UNIT SELECT
Bit 0	2^0	2^0	Write Gate	
1	2^1	2^1	Read Gate	
2	2^2	2^2	Servo Offset Plus	
3	2^3	2^3	Servo Offset Minus	
4	2^4		Fault Clear	
5	2^5		AM Enable 1	
6	2^6		RTZ	
7	2^7		Data Strobe Early 1	
8	2^8		Data Strobe Late 1	
9	2^9		Release	Priority Select 1

1 Not Used By The S33/A Controller

TAG BUS DECODE

FIGURE 6.1.1

6.1.3.4 Control Select

Tag 3 is used as an enable for the bus lines and must be true for the entire control operation. The functions of Bus Bits 0 - 9 are as follows:

Bit 0 Write Gate - The Write Gate line enables the write driver.

Bit 1 Read Gate - Setting the Read Gate enables read data from the disk to the transmission line. The leading edge of Read Gate triggers the disk's phase-lock oscillator to synchronize on an all zeros pattern.

Bit 2 Servo Offset Plus - Offsets the carriage from the nominal On Cylinder position towards the spindle.

Bit 3 Servo Offset Minus - Offsets the carriage from the nominal On Cylinder position away from the spindle.

Bit 4 Fault Clear - Clears the fault flip-flop in the disk if the faul condition no longer exists.

Bit 5 AM Enable - Not Used. Always a zero.

Bit 6 RTZ - Causes the actuator to seek Track 0; resets the Head Register; clears the Seek Error flip-flop in the disk.

Bit 7 Data Strobe Early - Not Used. Always a zero.

Bit 8 Data Strobe Late - Not Used. Always a zero.

Bit 9 Release - Enabling this line releases Channel Reserve and Channel Priority Select Reserve in the disk making alternate channel access possible after selection by the first channel ceases.

6.1.4 Individual Lines "A Cable"

1. Sector Mark

Derived from the servo track and occurs at the beginning of each sector.

2. Index Mark

Occurs once per revolution and its leading edge is considered the leading edge of Sector Zero.

3. Fault

Indicates one or more of the following fault conditions exist in the SMD: DC Power Fault, Head Select Fault, Write Fault, Write or Read while Off Cylinder, and Write Gate during a Read operation. A fault condition inhibits the writer to prevent

data destruction. The DC power fault indicates a below normal voltage from the positive or negative power supplies. The Head Select fault indicates that more than one head is selected. The Write Fault indicates low (or absence of) write current as well as the absence of write data.

4. Seek Error

Indicates a Seek Error has occurred (e.g., the disk was unable to complete a move within 500ms, the carriage has moved to a position outside the recording field or that a cylinder address greater than 822 has been selected).

5. On Cylinder

This status indicates the servo has positioned the heads over a cylinder. The status is cleared with any Seek instruction causing carriage movement or a zero-track Seek.

6. Unit Ready

This line indicates that the unit is selected; is up to speed; the heads are loaded; and no fault condition exists within the drive. If, after a load sequence, dibits are not sensed within 350ms, the heads will unload; the fault light will be illuminated; and Unit Ready will be dropped.

7. Open Cable Detector

The open cable detect circuit disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

8. Unit Select Tag

This signal gates the desired unit number into the disk's unit number compare circuit.

9. Unit Select (2 , 2)

These two lines are binary coded to select one of four SMD's. The unit number (0 through 4) is selectable by means of a logic plug on the operator panel in each individual disk.

10. Unit Select (2 , 2)

Always zero.

11. Address Mark Found

Not Used.

12. Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a front panel LED, and sends a write protected signal to the controller. Attempting to write while protected will cause a fault to be issued.

13. Power Sequencing

Power Sequencing requires AC and DC Power On, START indicator on, and the REMOTE/START switch in the SMD in the REMOTE position. Applying ground to the Pick and Hold lines will cause the first SMD in sequence to power up. Once this SMD is up to speed, the Pick signal is transferred to the next active SMD and is repeated until all active SMD's are powered up.

Individual SMD's may be started and stopped once the power sequencing is completed.

14. Busy (Dual Channel Only)

If the SMD is already reserved and/or selected, a Busy signal will be issued to the "A" cable and unit selected will be issued on the "B" cable to the channel attempting the select.

6.1.5 Signal Descriptions, "B" Cable

6.1.5.1 Individual Lines ("B" Cable)

The following signals are provided between the controller and each disk. See Figure 3.3.2.

1. Write Data

   This line carries data which is to be recorded on the disk pack from the controller to the disk.

2. Servo Clock

   The servo clock is a phase-locked 9.677 MHz clock generated from the servo track dibits. Servo clock is available at all times (not gated with Unit Select).

3. Read Data

   This line transmits the recovered data as NRZ form data from disk to the controller.

4. Read Clock

   The Read Clock defines the beginning of a data cell and is synchronous with the detected data.

5. Write Clock

   This line is synchronized to the NRZ data and is the Servo Clock retransmitted to the SMD by the controller.

6. Seek End

   Seek End is the combination of On Cylinder or Seek Error indicating that a Seek operation has terminated.

7. Unit Selected

   If the Unit Select bit lines match the logic plug in the disk when the leading edge of Unit Select tag is received, the Unit Selected signal is transmitted to the controller.

6.2 Pack Format

Each disk pack is divided into five individually addressable data surfaces as shown in Figure 6.2.1. The five Read/Write surfaces (designated 0 through 4) are sectioned into 823 (0 through 822) concentric cylinders. These cylinders consist of fixed-length sectors consecutively numbered 0 to 31 on each surface. Each sector is divided into two information fields separated by gaps or spaces. The header field contains two words of address information and two words of Header CRC. The data field contains 256 data words and two words of data CRC. The controller generates the sector gaps and the computer supplies the header and data information during a pack-formatting operation.

The read only servo surface is pre-recorded by the manufacturer with positioning signals used by the servo tracking circuits.

Each disk pack has a maximum formatted capacity of 663,667,200 bits. Table 6.2.1 shows how these bits are utilized.

6.2.1 Sector Format

The five major divisions of a sector are shown in Figure 6.2.2. Table 6.2.2 contains the overall bit/byte assignments for each sector.

1. Sector Gap - Contains 28 bytes of 0's and one sync byte. The sync byte, which marks the beginning of valid information, is shown in Figure 6.2.3.

2. Header Field - The header field is divided into three words as follows:

   a. Cylinder Address Word - Contains the address of the respective cylinder. The 16-bit format is shown in Figure 6.2.3 and described in Table 6.2.3.

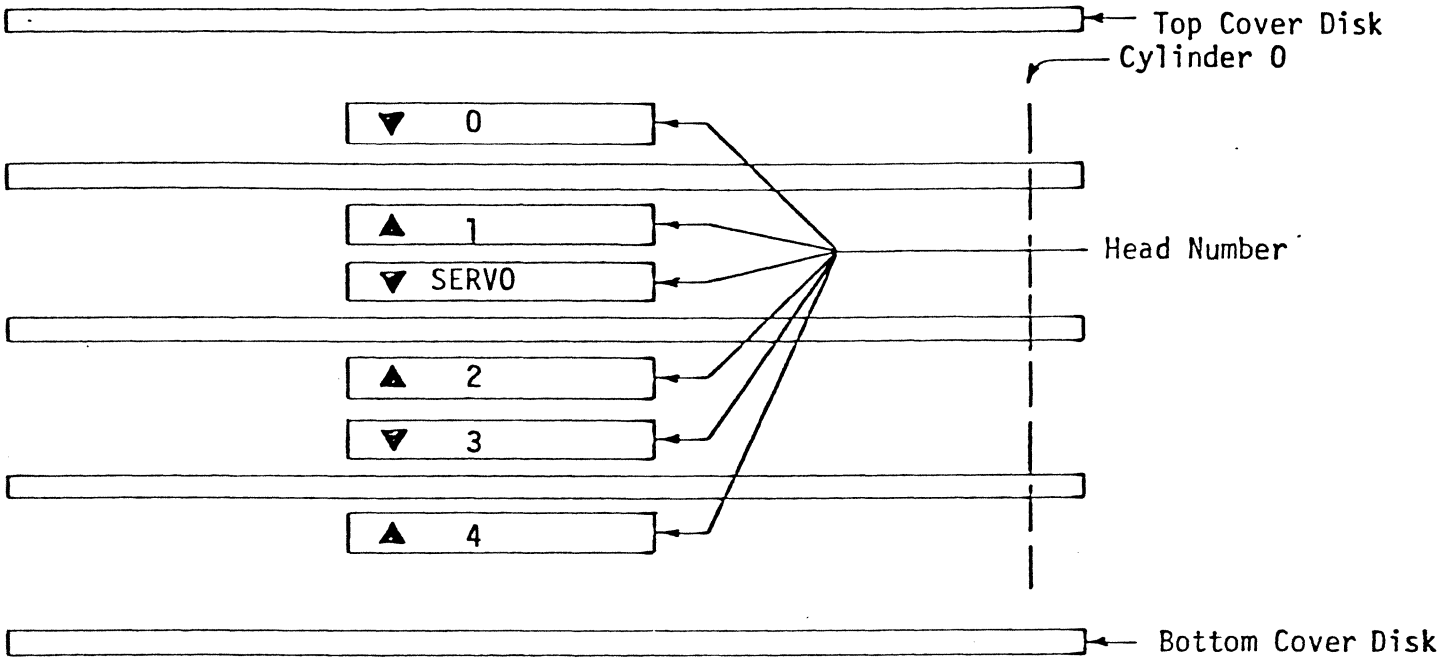
   b. Sector/Track Address Word - Contains the address of the respective track and sector. The 16-bit format is shown in Figure 6.2.3 and described in Table 6.2.4.

c. CRC Word - This 16-bit word is generated by the cycle redundancy check (CRC) circuits using the data in the first two header words. This CRC provides a method for error detection in reading the Header data.

3. Header Gap - Contains 17 bytes of 0's and one sync byte. The sync byte, which marks the beginning of valid information is shown in Figure 6.2.3.

4. Data Field - The data field is composed of 512 data bytes provided by software and 4 error correction code bytes generated by the ECC circuits of the controller. The 32-bit ECC word is considered part of the data field and used to detect errors in reading the data.

5. Data Gap - This gap consists of two 0 bytes which are generated by the drive followed by an indefined gap area which fills the remaining sector space.



80 mBYTE DISK PACK WITH HEAD LOCATION

FIGURE 6.2.1

TABLE 6.2.1 Pack Capacity Allocation

ITEM	FORMAT
No. of Sectors/Track	32
Bits/Sector	4,864
Total Formatted Capacity	640,491,520 bits
Formatted Data	539,361,280 bits
Total Number of Words	33,710,080

Table 6.2.2 Assignment of Bits/Bytes in Sectors

SECTOR LOCATION	BYTES	BITS
Sector Gap	29	232
Header Field	6	48
Header Gap	18	144
Data field	516	4128
Data Gap (fixed)	2	16
Undefined	59	472
Total per Sector	630	5040

NOTE: All byte descriptions in Table 6.2.2 are in terms of 8-bit bytes.

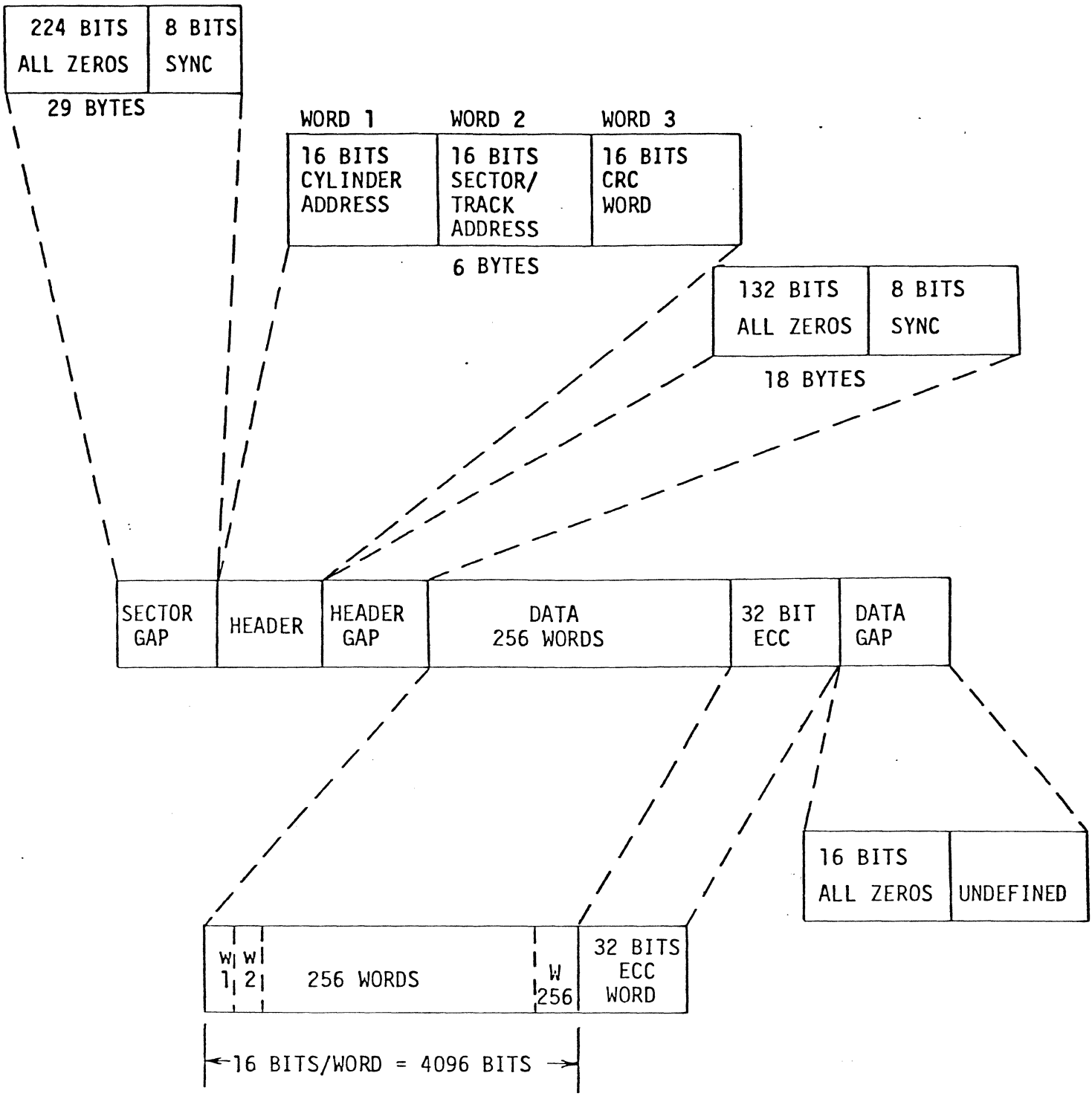


FIGURE 6.2.2

SECTOR FORMAT RM02

SYNC BYTE FORMAT

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1

CYLINDER ADDRESS FORMAT (First Header Word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MF	UF	0	FMT 1	0	0	CYL 512	CYL 256	CYL 128	CYL 64	CYL 32	CYL 16	CYL 8	CYL 4	CYL 2	CYL 1

SECTOR/TRACK ADDRESS FORMAT (Second Header Word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1

FIGURE 6.2.3

HEADER BITS AND SYNC BYTE FORMAT

TABLE 6.2.3 Cylinder Address Word-Bit Assignments

BIT	NAME	DESCRIPTION
0-9	CYL	Ten bit locations for the address of the cylinder. Any decimal number from 0 to 822 is valid. Bit 0 is least-significant bit.
10,11	Unused	Always 0s
12	FMT	The format bit is set to a 1 which establishes the sector is formatted using 16-bit words.
13	Unused	Always 0s
14	UF	The location where the user can identify this sector as being bad so that data is not recorded here. A 0 indicates a bad sector; 1 a good sector.
15	MF	The location used by the disk pack manufacturer to indicate a bad sector. A 0 indicates a bad sector; 1 a good sector.

TABLE 6.2.4 Sector/Track Address Word-Bit Assignments

BIT	NAME	DESCRIPTION
0-4	SA	These five bits contain the address of the sector. Valid decimal numbers are 0-31
5-7	Unused	Always 0s
8-10	TA	These three bits contain the track address. Valid numbers are 0-4.
11-12	Unused	Reserved for future use. (Set to zeros)
13-15	Unused	Always 0s

6.3 HARDWARE DESCRIPTION

The S33 controller is implemented using an advanced architecture whose unique structure and resulting capability provides exceptional features and performance. The heart of the system is a fast bi-polar microprocessor based on the 2901 family of components.

Three additional independent microprogrammed sequencers perform detail decision making and control for: 1) UNIBUS DMA operations, 2) UNIBUS programmed I/O operations, and 3) Disk Data movement operations. A block diagram of the controller is shown in Figure 6.3.1.

6.3.1 Microprocessor

Internal data path communication is via a tri-state, 16-bit bus (D Bus). Major elements in the data path include:

1. Disk Command Register

   This register is loaded by firmware with Bits 15, 14, 13 of the command word and directs the Disk Data Sequencer to execute one of the six following operations:

   - o Self-Test
   - o Read Header and Data
   - o Read Data
   - o Write Header and Data
   - o Write Data
   - o Idle

2. A Register

   Contains the Disk Address and Control Bus bits to direct disk operations. The data loaded into this register corresponds to the disk address and control bus defined in Section 6.1.3.

3. FIFO

   Performs serial-to-parallel and parallel-to serial data operations. Acts as the synchronization element between the disk and the controller for all data movements by buffering up to 16 words of data.

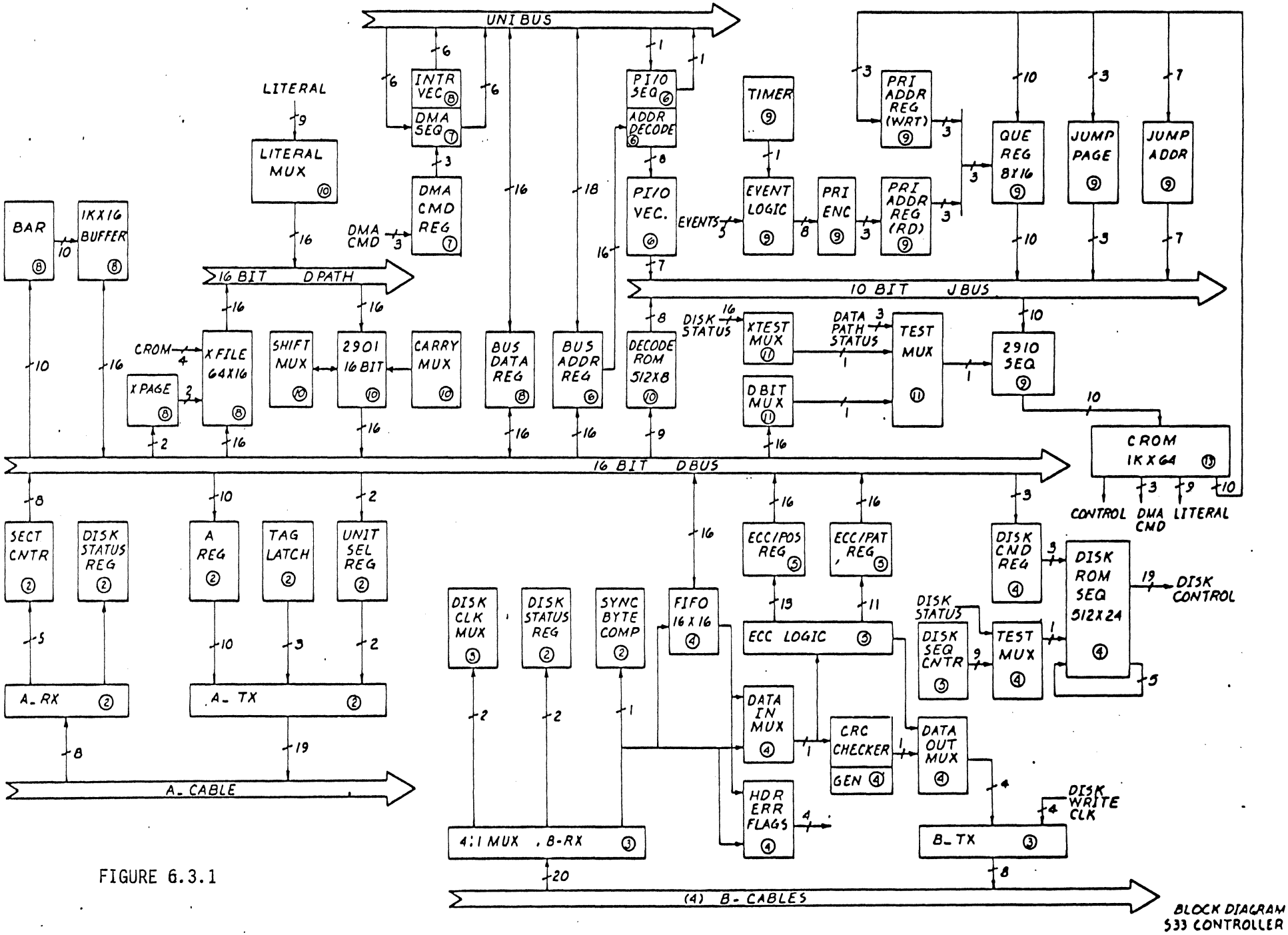


FIGURE 6.3.1

BLOCK DIAGRAM
533 CONTROLLER

4. Pattern Register

   Contains the actual data error correction mask after a successful data error-correction operation.

5. Position Register

   Contains the location of the first bit of the error burst after a successful data error-correction operation.

6. Sector Counter

   Provides rotational position (sector number) for the selected disk drive.

7. Buffer Address Register (BAR)

   Contains the address currently being used to read (Buffer Read Pointer) or Write (Buffer Write Pointer) data in the buffer.

8. Buffer (1K x 16)

   Provides storage of up to four sectors of data being transferred to or from the UNIBUS to eliminate data late errors and allow cross-track (spiral) read or write operation.

9. X-File (16 x 16)

   Provides 16 words of internal working storage for the software visible registers.

10. Microprocessor (2901)

    Provides the arithmetic/logical manipulation capability of the controller under firmware control. It also provides 16 words of storage for various pointers and temporary working registers. All standard 2901 functions are implemented including a set of 8 shift instructions.

11. Address/Data Registers

    Provides temporary storage for address or data movements between the controller and the UNIBUS.

Major elements in the control structure include:

1. Resume Address RAM and Event Logic

   Provides the primary task scheduling mechanism for the firmware by prioritizing the various events demanding attention by the controller. Provides the firmware address for resumption of a task temporarily suspended waiting the occurrence of some event.

2. Bus Vector ROM

   Provides a unique vector address for the firmware as a function of the register addressed by software and the operation required (Read/Write, Word/Byte).

3. 2910 Sequencer

   Provides the next micro-program address to be executed and resolves all conditional executions.

4. Test Logic

   Selects 1 of 45 firmware testable status flags or testable bits used to direct firmware execution.

5. Control ROM

   1024 words of 64-bit micro-program memory

6. Command Decode ROM

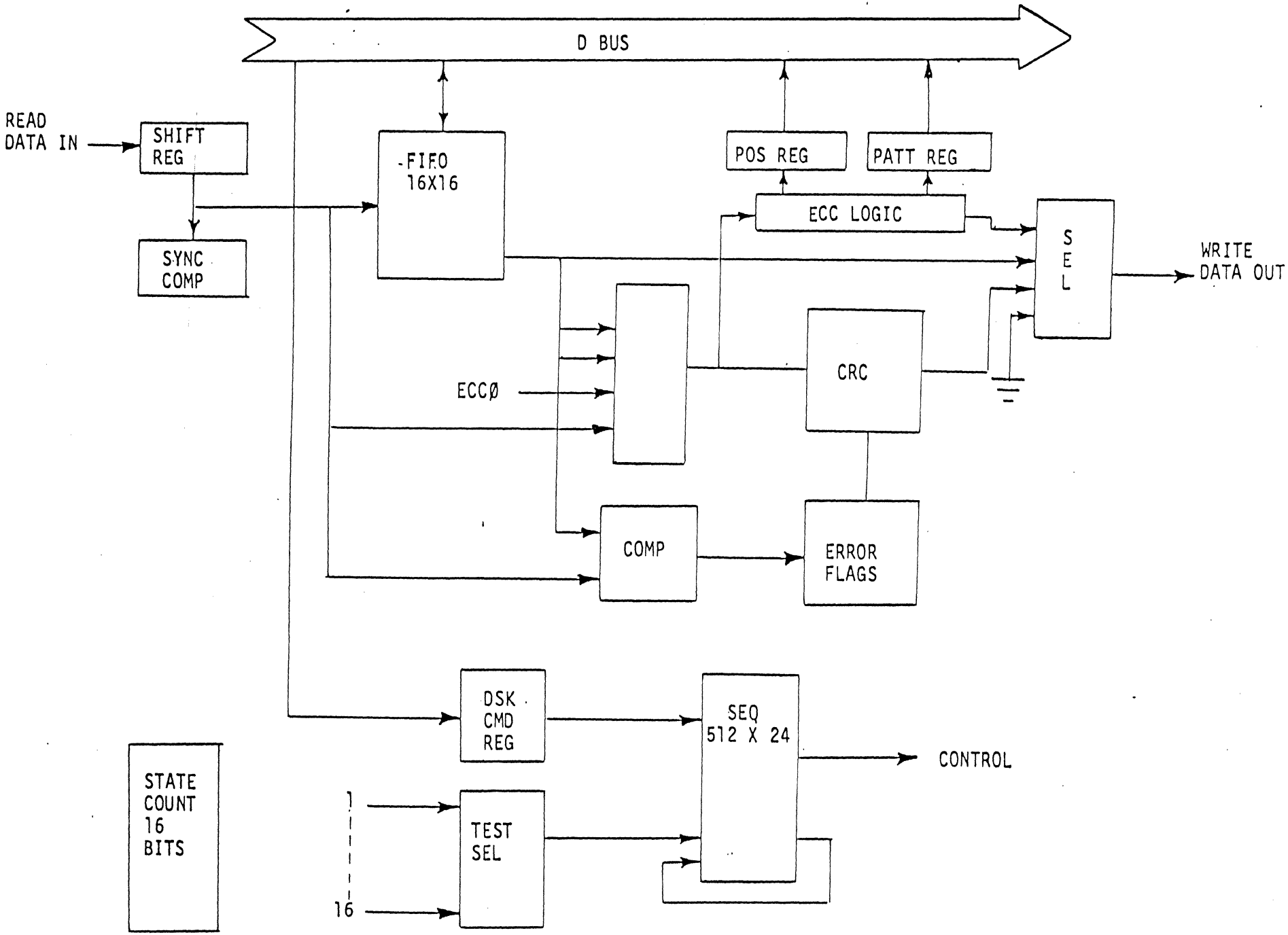
   Provides a unique vector address for the firmware as a function of the data on the D Bus. Used to decode the operation required as defined by the contents of CS1 loaded previously by software.

6.3.2 Disk Data Sequencer

A block diagram of the disk data sequencer and serial data path is shown in Figure 6.3.2.1. Data written to and read from the disk and the verification of data integrity is controlled by this logic. Major elements include:

1. Data Input Shift Register

   Synchronizes disk data with Read Clock and provides 8 bits of storage for Sync Byte comparison.



DISK DATA SEQUENCER BLOCK DIAGRAM
FIGURE 6.3.2.1

2. FIFO

   See Section 6.3.1.

3. Position Register/Pattern Register

   See Section 6.3.1.

4. ECC Logic

   Generates and checks ECC over the 512 data bytes and provides the proper values for the POS and PAT registers on an error.

5. CRC

   Generates and checks 16-bit CRC over the sector header.

6. Comparator

   Performs bit by bit comparison of the header read from disk with expected value read from the FIFO.

7. Error Flags

   Consists of the error flags associated with header and data.

   - o DCK - Disk Data Error
   - o ECH - Hard Data Error
   - o FMT - Improper Format
   - o CRC - Header CRC Error
   - o HCE - Header Compare Error
   - o BSE - Bad Sector Error

8. Disk Command Register

   See Section 6.3.1.

9. Sequencer

   Micro-program storage which provides decision making and direct control for disk data movements.

10. Test Mux

    Selects 1 of 16 testable status flags to direct sequencer execution.

11. State Counter

    A 16-bit counter, testable by the sequencer, used to count the data bits read from or written to disk.

6.3.3 UNIBUS Control Sequencers

A block diagram of the UNIBUS interface is shown in Figure 6.3.3.1. In addition to the normally used transceivers and registers, there are two ROM sequencers whose major elements include:

1. DMA Command Register

   Directs the DMA sequencer to execute one of eight operations:

   - o Bus Request (Interrupt)
   - o DMA Idle (Release Bus)
   - o NPR Request
   - o DMA Write (Write and Hold Bus)
   - o Write Release (Write and Release Bus)
   - o Request Read (Request Bus and Read Memory)
   - o DMA Read (Read Memory)
   - o Self-Test

2. DMA Sequencer

   Tests and asserts UNIBUS control lines to perform the required "handshake" and controls bus interface timing to complete the required bus operation.

3. Programmed I/O Sequencer

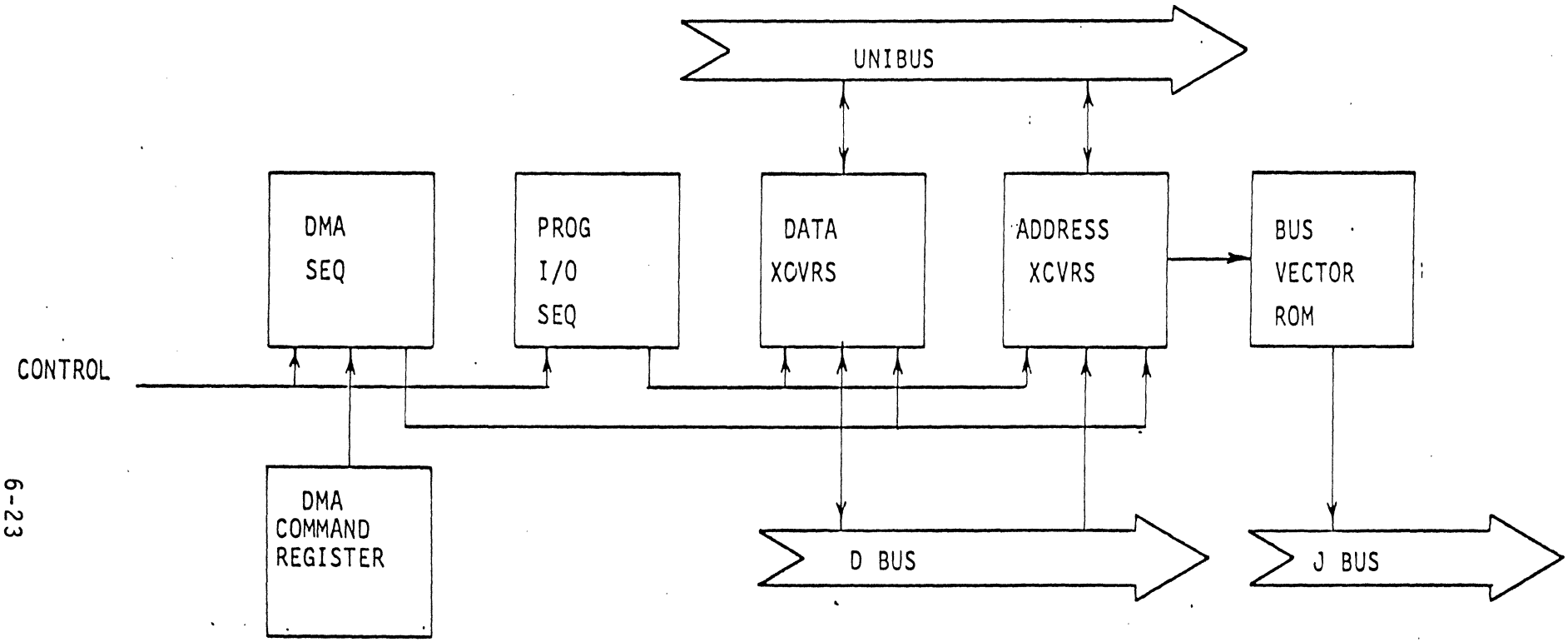
   Tests and asserts UNIBUS control lines to perform the required "handshake" and controls bus interface timing to complete "Bus Slave" operations.

6.3.4 Internal Self-Test

The S33 controller firmware contains an extensive automatic self-test feature enabled on power-on with errors/status displayed via four on-board LED's. Initially the LED's are illuminated with successive tests extinguishing LED's as appropriate giving a total of 16 possible status states. Major hardware tests of the self-test program include: (See Table 4.4.1 for Error Decode)

- o Buffer RAM
- o X File
- o 2901 Bit Slice
- o D Bus
- o FIFO (Parallel and Serial Operation)

- Priority Event Logic
- ECC Logic
- CRC Logic
- Disk Sequencer Sanity Test
- Sync Byte Comparator



UNIBUS INTERFACE
BLOCK DIAGRAM

FIGURE 6.3.3.1

6.4 Firmware Description

The firmware in the controller is contained in three independent micro-programmed sequencers to perform the required decision making and control functions. Each sequencer contains its own firmware set implemented in a language appropriate to the task. In addition, there are three ROM's used for translation or mapping functions.

6.4.1 Microprocessor

Primary control of the operations of the controller is provided by the firmware for the 2901/2910 microprocessor. This structure also provides supervisory control of the other sequencers, defining and initiating their functions and utilizing the results to complete its own activities.

The firmware is contained in a set of ROM's organized as 512 words by 64 bits which is addressed by the 2910 sequencer chip.

Figure 6.4.1.1 defines the micro-instruction format, the usage of the different fields, their respective bit assignments, field values, and labels used by the language translator.

6.4.1.1 Programmed I/O Map ROM

The PIO map is a 512 word by 8 bit ROM used to provide two functions. The contents of this map are shown in Figure 6.4.1.1.1.

- o Device Code Recognition

  For the normal RM02 device codes, the ROM is enabled for all UNIBUS addresses from 776700 to 776777. The six least significant bus address bits are used as ROM address bits directly which allows the controller to respond to addresses from 776700 to 776747 as valid RM02 locations. Unwanted addresses from 776748 to 776777 are thus excluded with a minimum of logic.

- o Selected Register/Function Mapping

  Addressing the ROM with the two bus control lines in addition to the six UNIBUS address lines provides a decode of the selected register, word, upper byte or lower byte manipulation, and read or write operation.

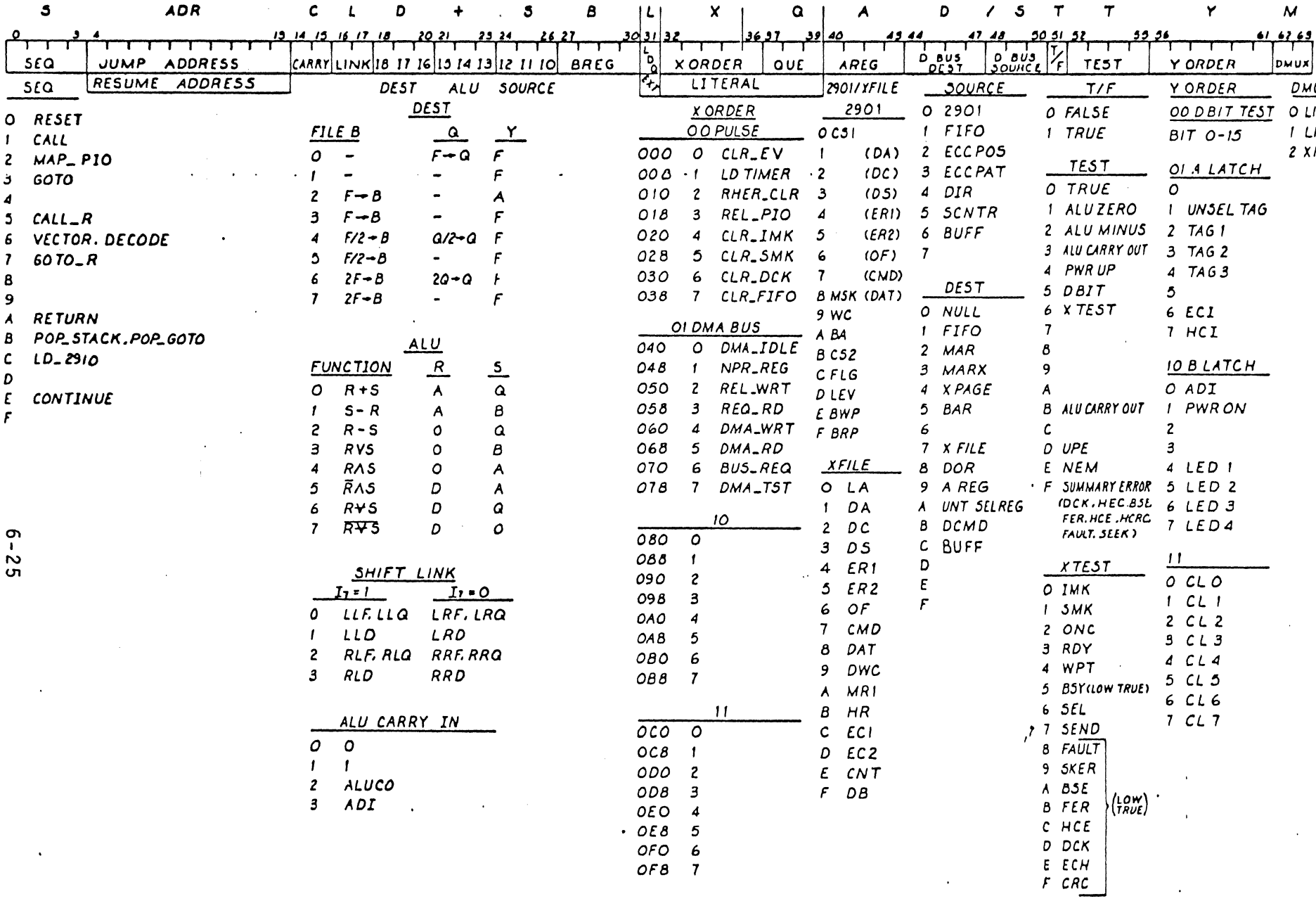


FIGURE 6.4.1.1

S33 CONTROLLER
MICRO WORD

PIO MAPPING PROM

ROM Address:

8	7	6	5	4	3	2	1	Ø
Ø	REG SEL					MODE		B

ROM Output:

7	6	5	4	3	2	1	Ø
SEL	VECTOR						

Field Definitions:

Register Select Field (Reg. Sel):

Selected Register	UNIBUS Address	Field Value
RMCS1	776700	00
RMWC	776702	01
RMBA	776704	02
RMDA	776706	03
RMCS2	776710	04
RMDS	776712	05
RMER1	776714	06
RMAS	776716	07
RMLA	776720	10
RMDB	776722	11
RMMR1	776724	12
RMDT	776726	13
RMSN	776730	14
RMOF	776732	15
RMDC	776734	16
RMHR	776736	17
RMMR2	776740	20
RMER2	776742	21
RMEC1	776744	22
RMEC2	776746	23

FIGURE 6.4.1.1.1

MODE, Byte Fields (MODE), (B):

Bus Function	MODE Field	Byte Field	Controller Interpretation
DATI	00	0	Word Read
Invalid	00	1	Word Read
DATIP	01	0	Word Read
Invalid	01	1	Word Read
DATO	10	0	Word Write
Invalid	10	1	Word Write
DATOB	11	0	Write Lower Byte
DATOB	11	1	Write Upper Byte

Device Selected (Sel):

Field Value	Controller Interpretation
Ø	Selected
1	Not Selected

Micro Instruction Address (Vector):

These seven bits provide an address for the micro-program as a function of the register selected and the operation requested by software.

PIO MAPPING PROM (Continued)

FIGURE 6.4.1.1.1

6.4.1.2 Command Decode ROM

Decode of the controller command word is done by a 512 word by 8 bit ROM using specific bits of the D Bus as an address with the ROM output providing a micro-instruction location (address) for the controller firmware. Although the implementation allows the appropriate bits of any D Bus transfer to be used as the ROM address, usage in the controller is restricted to specific control and status bits. The contents of the decode ROM are shown in Figure 6.4.1.2.1.

6.4.2 Disk Data Sequencer

The disk data sequencer is a set of ROM's organized as a "ROM-Register Sequencer" consisting of 512 words by 24 bits. Primary control of the sequencer's operation is provided by the Disk Command Register which is loaded from the microprocessor "D Bus". This register provides three bits of address for the ROM which may be viewed as defining a "page" of locations or an "OP-Code". Execution is by means of conditional two-way jumps or branches to adjacent location (address) "pairs". The address of the "pairs" is provided from the ROM's output with the decision between the two addresses made based on the test result.

Figures 6.4.2.1 through 6.4.2.3 define the instruction format, the usage of the different fields, their respective bit assignments, addresses, field values, and labels used by the language translator.

6.4.3 Bus Control Sequencers

Two independent micro-programmed sequencers provide the decision-making and control functions required by the protocol of the UNIBUS.

6.4.3.1 DMA Sequencer

The DMA Sequencer is a set of ROM's organized as 512 words by 16 bits which functions as a "ROM-register sequencer". Inputs provided as addresses consist of bits defining the desired function, the current state of the sequencer, and UNIBUS lines whose states determine subsequent actions. Figure 6.4.3.1.1 defines

COMMAND DECODE ROM FORMAT

ROM Address:	A8	A7	A6	A5	A4	A3	A2	A1	A0
D Bus Bit:	14	12	6	5	4	3	2	1	0
Specific Bit:	ERR	MOL	VV	FUNCTION					GO
Source:	RMDS			RMCS1					

ROM Output:	7	6	5	4	3	2	1	0
	VECTOR							

Individual Bit Definitions:

ERR: Composite Error Bit
MOL: Medium on Line
W : Volumn Valid
GO : Go or Execute Bit.

FIGURE 6.4.1.2.1

Valid Combinations:

ERR	MOL	VV	VALID FUNCTION FIELD VALUES	VALID FUNCTIONS
0	0	0	0	NOP
			4	Drive Clear
			8	Read in Preset
			9	Pack Acknowledge
0	0	1	0	NOP
			4	Drive Clear
			8	Read in Preset
			9	Pack Acknowledge
0	1	0	0	NOP
			4	Drive Clear
			8	Read In Preset
			9	Pack Acknowledge
0	1	1	1	NOP
			2	Seek
			3	Recalibrate
			4	Drive Clear
			5	Release
			6	Offset
			7	Return to Centerline
			8	Read In Preset
			9	Pack Acknowledge
			C	Search
			14	Write Check Data
			15	Write Check Header & Data
			18	Write Data
			19	Write Header & Data
			1C	Read Data
			1D	Read Header & Data
1	0	0	4	Drive Clear
1	0	1	4	Drive Clear
1	1	0	4	Drive Clear
1	1	1	4	Drive Clear

FIGURE 6.4.1.2.1 (Continued)

DISK SEQUENCER - MICRO INSTRUCTION FORMAT

ROM Address:

8	7	6	5	4	3	2	1	0
CMD			STATE					T

Micro Instruction Format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
STATE					TEST			MUX		ORDER				BIT ORDERS									
ST					T			M		O				Z	#	ECC		G	H	OFI		W	R

Field Definitions:

Command Field (CMD):

CMD	Name	Field Value	Origin HEX
Disk Idle	DI	0	000
Spare	-	1	040
Disk Test	DT	2	080
Spare	-	3	0C0
Write Data	WD	4	100
Write Header and Data	WH	5	140
Read Data	RD	6	180
Read Header and Data	RH	7	1C0

State Field (State):

Address Label	Field Value	Absolute Address
DIXX	00-1F	000-03F
-	00-1F	040-07F
DTXX	00-1F	080-0BF
-	00-1F	0C0-0FF
WDXX	00-1F	100-13F
WHXX	00-1F	140-17F
RDXX	00-1F	180-1BF
RHXX	00-1F	1C0-1FF

Test Results (T):

Condition	Field Value
Selected test state low	0
Selected test state high	1

FIGURE 6.4.2.1

TEST FIELD (Test):

Function	Name	Field Value
Unconditional Jump	True	0
Header Error Summary	Error	1
Index or Sector Mark	IOSMK	2
Sync Byte (Neg True)	-Sync	3
Data Check (ECC Error)	DCK	4
Error Check Inhibit	ECI	5
End of ECC Correction Cycle	END	6
State Counter = 4	C4	7
State Counter = 8	C8	8
State Counter = 16	C16	9
State Counter = 32	C32	A
State Counter = 64	C64	B
State Counter = 128	C128	C
State Counter = 256	C256	D
State Counter = 4096	C4096	E
State Counter = 65536	Carry	F

DATA SELECT FIELD (MUX):

Read Select Function	RMUX Name	Field Value	WMUX Name	Write Select Function
Zeros Fill	Zero	0	Zero	Zeros Fill
Data Input	DIN	1	CRCOUT	CRC Gen Output
ECC CKTS - Bit 0	ECC0	2	ECC0	ECC CKTS Bit 0
FIFO Output	FIFO	3	FIFO	FIFO Output

ORDER FIELD (Order):

Function	Name	Field Value
No Operation	NOP	000
Data Check Error Enable	DCKEN	001
CRC Error Enable	CRCEN	010
Bad Sector Error Enable	BSEN	011
Format Error Enable	FMTEN	100
Set Done Flag	DONE	101
Spare	--	110
Spare	--	111

BIT ORDER FIELD (Bit Order):

Function	Signal Name	Bit Position	Comments
Clear Cmd Register	CLR CMD	14	Default = 1
State Counter Enable	CNTEN	15	
ECC Correction Cycle Enable	ECCTN	16	
Clear ECC - CRC Circuits	ECC-CRC	17	Default = 1
Enable ECR	GENCRC	18	
Header Compare Enable	HCEN	19	
FIFO Output Enable	FIFOOUT	20	
FIFO Input Enable	FIFOIN	21	
Disk Write Gate	WRT - Gate	22	
Disk Read Gate	RD - Gate	23	

FIGURE 6.4.2.2

Language Form

```
Label (1):  IF [Test] THEN [Label (2)] ELSE [Label (3)],
            RMUX = Name (1), Order A,
            WMUX = Name (2),
            SET [Bit Order (1) &.....Bit Order (N)],
            Clear [Bit Order (1) &.....Bit Order (N)];
```

FIGURE 6.4.2.3

DMA SEQUENCER FORMAT

ROM Address:

8	7	6	5	4	3	2	1	Ø
SEQ BG	CMD			DONE	TEST	SEQ NPG	BBSYO	SSYNC

ROM Output:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
BR	NPR	SACK	INTR	MSYNCI	BBSYI	DMA OUT	BUS MASTER	X	DMA EVENT	TEST	DONE	HOLD DATA	DMA BAD	DMA OUT	X

Field Definitions - Address:

Command Field (CMD):

Disk Command	Field Value	Comment
DMA IDLE	000	No Operation
NPR REQ	001	Bus Request for DMA Transfer
REL-WRT	010	Write Operand to Memory and Release Bus
REQ-RD	011	Request Bus and Read Data From Memory
DMA WRT	100	Write Operand to Memory
DMA RD	101	Read Data From Memory
BUS REQ	110	Interrupt Request
DMA TEST	111	Self Test of DMA Sequencer

Individual Bits:

Mnemonic	Bit No.	Comment
SEQ-BG	8	BUS GRANT
DONE	4	Sequencer STATE - Internal Use
TEST	3	Sequencer STATE - Internal Use
SEQ-NPG	2	Non-Processor Grant
BBSYO	1	Bus Busy - Input from Bus
SSYNC	0	Slave Sync - Input from Bus

FIGURE 6.4.3.1.1

Bit Definitions - Output:

Mnemonic	Bit No.	Comment
BR	15	Bus Request
NPR	14	Non Processor Request'
SACK	13	Acknowledge
INTR	12	Interrupt Request
MSYNCI	11	Master Sync
BBSYI	10	Bus Busy
DMAOUT	9	Enable Data into UNIBUS
BUSMASTER	8	Enable Address and Control onto UNIBUS
-	7	Not Used
DMAEVENT	6	Priority Event For DMA
TEST	5	One of Two Sequencer Controls
DONE	4	One of Two Sequencer Controls
HOLDDATA	3	Latch Control for Data From UNIBUS
DMABAD	2	Filler for Unused Locations
DMAOUT	1	Gates Data onto UNIBUS
-	Ø	Not Used

FIGURE 6.4.3.1.1 (Continued)

the fields, bit assignments, and functions of the DMA sequencer.

6.4.3.2 Programmed I/O Sequencer

The PIO sequencer is a 32 word by 8 bit ROM which functions as a "ROM-register sequencer". Inputs are provided as addresses which consist of bits derived from UNIBUS lines whose state determines subsequent actions, two bits which define the current state of the sequencer, and a bit which signals the completion of the bus transaction. Figure 6.4.3.2.1 defines the fields, bit assignments and functions of the PIO sequencer.

PI/O SEQUENCER FORMAT

ROM Address:

4	3	2	1	0
REL PIO	DEV SEL	C1	OUT BIT	IN BIT

ROM Output:

7	6	5	4	3	2	1	Ø
	PIO BAD	PIO EVENT	OUT BIT	IN BIT	PIO DIN	SSYNC	

Bit Definitions - Address:

Mnemonic	Bit No.	Comment
In Bit	Ø	Sequence STATE - Internal Use
Out Bit	1	Sequence STATE - Internal Use
C1	2	Unibus Read/Write Control
DEV-SEL	3	Device Selected
REL-PI/O	4	Release PI/O Sequencer

Bit Definitions - Output:

Mnemonic	Bit No.	Comment
-	Ø	Not Used
SSYNCI	1	Slave Sync
PIODIN	2	Enables Data Onto Unibus
INBIT	3	One of Two Sequence Control Bits
OUTBIT	4	One of Two Sequence Control Bits
PIOEVENT	5	Priority Event for PI/O
PIOBAD	6	Filler For Unused Locations
-	7	Not Used

FIGURE 6.4.3.2.1

7.0 DOCUMENTATION

7.1 Schematic Diagram 03190

7.2 Assembly Drawing 65001/65034

7.3 Bill of Materials 65001

1	A,B	2
	A	
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
	V	

1	E	2	
	A	+5V	
	B		
BUSAI2L	C	GND	
BUSAI7L	D	BUSAI5L	
BUSMSYNCL	E	BUSAI6L	
BUSAO2L	F	BUSCIL	
BUSAO1L	H	BUSAOOL	
BUSSSYNCL	J	BUSCOL	
BUSAI4L	K	BUSAI3L	
BUSAIIL	L		
	M		
	N	BUSAO8L	
BUSAIOL	P	BUSAO7L	
BUSAO9L	R		
	S		
GND	T		
BUSAO6L	U	BUSAO4L	
BUSAO5L	V	BUSAO3L	

1	C	2	
BUSNPGH	A	+5V	
BUSBGOUTH	B		
	C	GND	
	D	BUSDI5N	
	E	BUSDI4N	
	F	BUSDI3N	
BUSDIIN	H	BUSDI2N	
	J	BUSDION	
	K	BUSDO9N	
	L	BUSDO8N	
	M	BUSDO7N	
BUSDCLOL	N	BUSDO4N	
	P	BUSDO5N	
	R	BUSDOIN	
BUSPBL	S	BUSDOON	
GND	T	BUSDO3N	
	U	BUSDO2N	
	V	BUSDO6N	

1	F	2	
	A	+5V	
	B	-15V	
	C	GND	
BUSBBSYL	D		
	E		
	F		
	H		
BUSNPRL	J		
	K		
	L		
BUSINTRL	M		
	N		
	P		
	R		
	S		
GND	T	BUSSACKL	
	U		
	V		

1	D	2	
	A	+5V	
	B		
	C	GND	
	D	BUSBR7L	
	E	BUSBR6L	
	F	BUSBR5L	
	H	BUSBR4L	
	J		
	K	BUSBGIN7H	
BUSINITL	L	BUSBGOUT7	
	M	BUSBGIN6H	
	N	BUSBGOUT6	
	P	BUSBGIN5H	
	R	BUSBGOUT5	
	S	BUSBGIN4H	
GND	T	BUSBGOUT4	
	U		
	V		

H			H
TAG 1	1	51	TAG 1
TAG 2	2	52	TAG 2
TAG 3	3	53	TAG 3
D BIT 0	4	54	D BIT 0
D BIT 1	5	55	D BIT 1
D BIT 2	6	56	D BIT 2
D BIT 3	7	57	D BIT 3
D BIT 4	8	58	D BIT 4
D BIT 5	9	59	D BIT 5
D BIT 6	10	60	D BIT 6
D BIT 7	11	61	D BIT 7
D BIT 8	12	62	D BIT 8
D BIT 9	13	63	D BIT 9
OPEN CABLE DET.	14	64	OPEN CABLE DET.
FAULT	15	65	FAULT
SEEK ERROR	16	66	SEEK ERROR
ON CYLINDER	17	67	ON CYLINDER
INDEX MARK	18	68	INDEX MARK
UNIT READY	19	69	UNIT READY
	20	70	
BUSY	21	71	BUSY
UNIT SELECT TAG	22	72	UNIT SELECT TAG
UNIT SELECT 2°	23	73	UNIT SELECT 2°
UNIT SELECT 2'	24	74	UNIT SELECT 2'
SECTOR MARK	25	75	SECTOR MARK
UNIT SELECT 2²	26	76	UNIT SELECT 2²
UNIT SELECT 2³	27	77	UNIT SELECT 2³
WRITE PROTECT	28	78	WRITE PROTECT
POWER PICK	29	79	POWER HOLD
	30	80	

J			J
GND	1	14	SI
SERVO CLK 1	2	15	GI
READ DATA 1	3	16	RI
GND	4	17	RE
READ CLK 1	5	18	GI
WRT CLK 1	6	19	W
GND	7	20	W
WRT DATA 1	8	21	GI
UNIT SELD 1	9	22	UI
SEEKEND 1	10	23	SE
GND	11	24	
	12	25	GI
	13	26	

K			K
GND	1	14	SE
SERVO CLK 2	2	15	GI
READ DATA 2	3	16	RE
GND	4	17	RE
READ CLK 2	5	18	GI
WRT CLK 2	6	19	WI
GND	7	20	W
WRT DATA 2	8	21	GI
UNIT SELD 2	9	22	UI
END SEEK 2	10	23	EN
GND	11	24	
	12	25	GI
	13	26	

L			L
GND	1	14	SE
SERVO CLK 3	2	15	GI
READ DATA 3	3	16	RI
GND	4	17	RE
READ CLK 3	5	18	GI
WRT CLK 3	6	19	WI
GND	7	20	W
WRT DATA 3	8	21	GI
UNIT SELD 3	9	22	UI
SEEK END 3	10	23	SE
GND	11	24	
	12	25	GI
	13	26	

M			M
GND	1	14	SE
SERVO CLK 4	2	15	GI
READ DATA 4	3	16	RE
GND	4	17	RE
READ CLK 4	5	18	GI
WRT CLK 4	6	19	WI
GND	7	20	W
WRT DATA 4	8	21	GI
UNIT SELD 4	9	22	UI
SEEK END 4	10	23	SE
GND	11	24	
	12	25	GI
	13	26	

REF. DESIG.	GATES USED PER TOTAL
Z21	5/6
Z32	3/4
Z61	3/4
Z132	3/4

8. ALL LIGHT EMITTING DIODES ARE DIALIGHT 555-2003.

4. ALL RESISTOR MODULE VALUES ARE IN OHMS.

3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W.

2. CAPACITANCE TOLERANCE AND VOLTAGES ARE AS FOLLOWS
   PICOFARADS = ±5% 100VOLTS
   0.1 MICROFARADS = ±20%, 50VOLTS
   4.7 MICROFARADS = ±20%, 10 VOLTS

1. ALL CAPACITOR VALUES ARE IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION	10-29-79	
	B	RE-RELEASE	9-27-80	

PRIORITY INTERRUPT LEVEL OPTION

	CUT ETCH BETWEEN CONN. PINS	CUT ETCH BETWEEN CONN. PINS	REMOVE JUMPERS	ADD BR+BG JUMPER	ADD BR-PROPAGATE JUMPER
PRIORITY 4	E17 AND E19 E22 AND E24 E28 AND E31	DS2 AND DT2	E17 E22, E23, E24 E25, E26	E17 TO E18 E31 TO E27 E22 TO E23	E24 TO E28 E25 TO E29 E26 TO E30
* PRIORITY 5			E17 E22 E23 E24 E25 E26	E17 TO E19 E31 TO E28 E22 TO E24	E23 TO E28 E25 TO E29 E26 TO E30
PRIORITY 6	E17 AND E19 E22 AND E24 E28 AND E31	DM2 AND DN2	E17 E22, E23, E24 E25, E26	E17 TO E20 E31 TO E29 E22 TO E25	E23 TO E27 E24 TO E28 E26 TO E30
PRIORITY 7	E17 AND E19 E22 AND E24 E28 AND E31	DK2 AND DL2	E17 E22, E25, E24 E23, E26	E17 TO E21 E31 TO E30 E22 TO E26	E23 TO E27 E24 TO E28 E25 TO E29

* = STANDARD IN ETCH

S33/A UNIBUS ADDRESS OPTION
7767XX (STANDARD IN ETCH)

1	1	1	1	1	1	1	Ø	1	1	1	Ø	X	X	X	X	X	X
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(E3 (E1 (E9 E5 (E15 (E7 (E13 (E11
E4 E2 E10 E6 E16 E8 E14 E12) NOTE 1
NOTE 2

NOTE 1 : JUMPER MUST BE INSTALLED FOR S33/A

NOTE 2 : JUMPERS ARE IN ETCH
JUMPER INSTALLED = 1
JUMPER REMOVED = Ø

S33/A UNIBUS VECTOR OPTION
254 (STANDARD IN ETCH)

Ø	1	Ø	1	Ø	1	1	Ø	Ø
8	7	6	5	4	3	2	1	0

E38 /E36 E35 /E34 E40 E42
E39 (E37 E32 (E35 E41 E43)
NOTE 3

NOTE 3 : JUMPERS ARE IN ETCH
JUMPER INSTALLED = Ø
JUMPER REMOVED = 1

S33 CONFIGURATION CHART

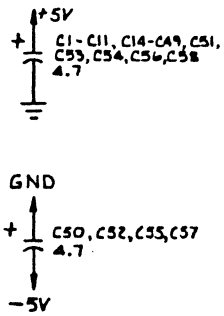
FUNCTION		S33/A REMOVE JUMPER	S33/A ADD JUMPER	S33/B REMOVE JUMPER OR CUT ETCH	S33/B ADD JUMPER
UNIBUS ADDRESS		E5 TO E6	E1 TO E2 (1)	E7 TO E8	E1 TO E2 (1)
			E3 TO E4 (1)	E11 TO E12	E3 TO E4 (1)
			E7 TO E8 (1)	E13 TO E14	E5 TO E6
			E9 TO E10 (1)		E9 TO E10 (1)
			E11 TO E12 (1)		E15 TO E16 (1)
			E13 TO E14 (1)		
			E15 TO E16 (1)		
UNIBUS VECTOR		E32 TO E33	E34 TO E35 (1)	E38 TO E39	E32 TO E33
		E38 TO E39	E36 TO E37 (1)	E40 TO E41	E34 TO E35 (1)
		E40 TO E41			E36 TO E37 (1)
		E42 TO E43			E42 TO E43
CRC/LRC OPTION		E61 TO E59	E60 TO E61 (1)	E60 TO E61	E61 TO E59
DRIVE CONFIG	80MB		E62 TO E63 (1)		E62 TO E63 (1)
	300MB			E62 TO E63	

(1) CONNECTION EXISTS IN ETCH. JUMPER NOT REQUIRED IF ETCH NOT PREVIOUSLY CUT

LAST DESIGNATION USED	
INTEGRATED CIRCUIT	E182
RESISTOR	R47
CAPACITOR	C62
LIGHT EMITTING DIODE	LED4
RESISTOR MODULE	RM21
OSCILLATOR	Y1
VOLTAGE REGULATOR	Q1
DIODE	CR1

REFERENCE DESIGNATIONS NOT USED
R38, R39

PART NUMBER
74504
74500
74508
74586



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± / .XXX ± / ANGLES ± /
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN R.A. McNULTY	9-18-79
CHECKED J. Ramsey	10-31-79
ENG.	
APPROVED	

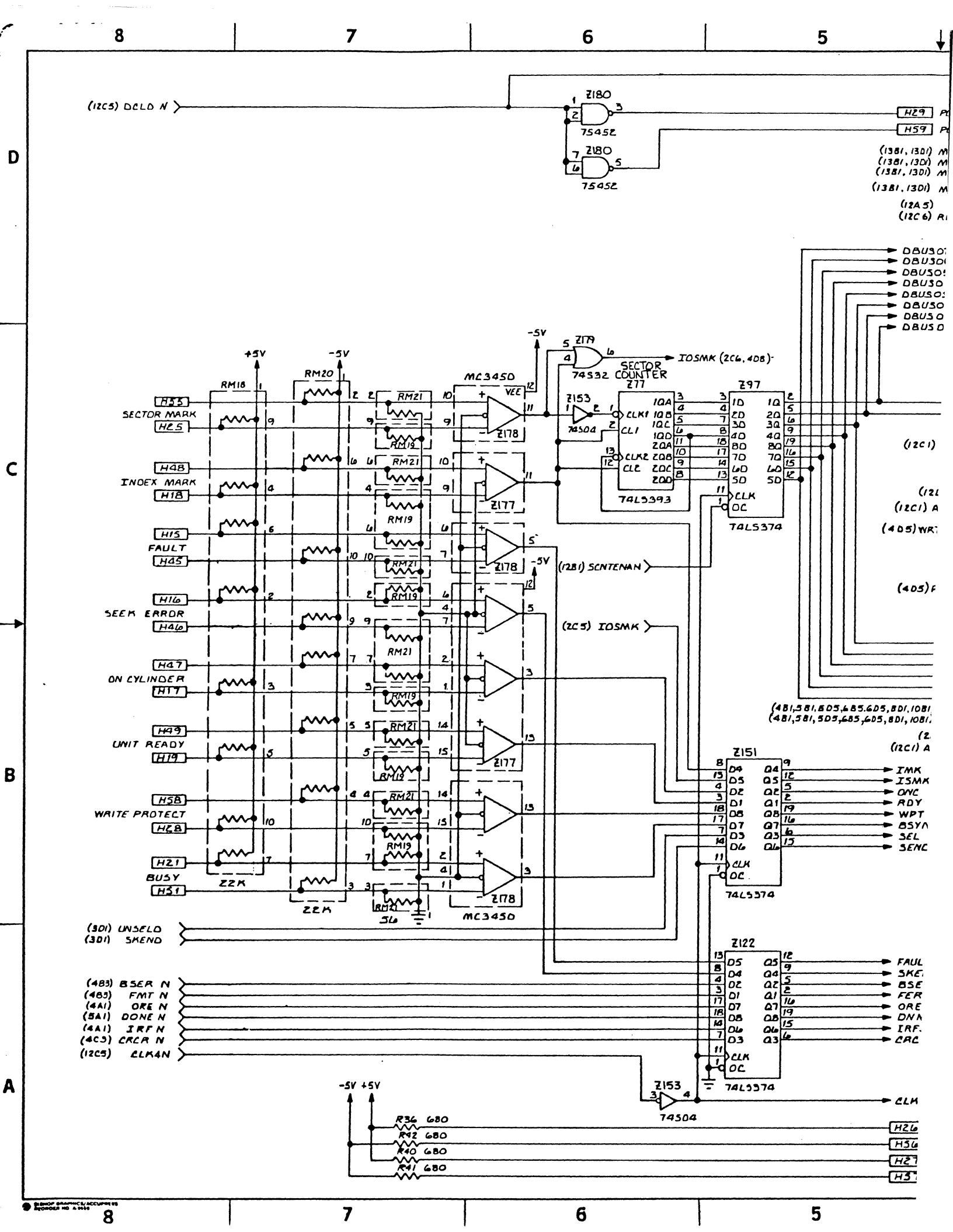
DATARAM CORPORATION
CRANBURY NEW JERSEY

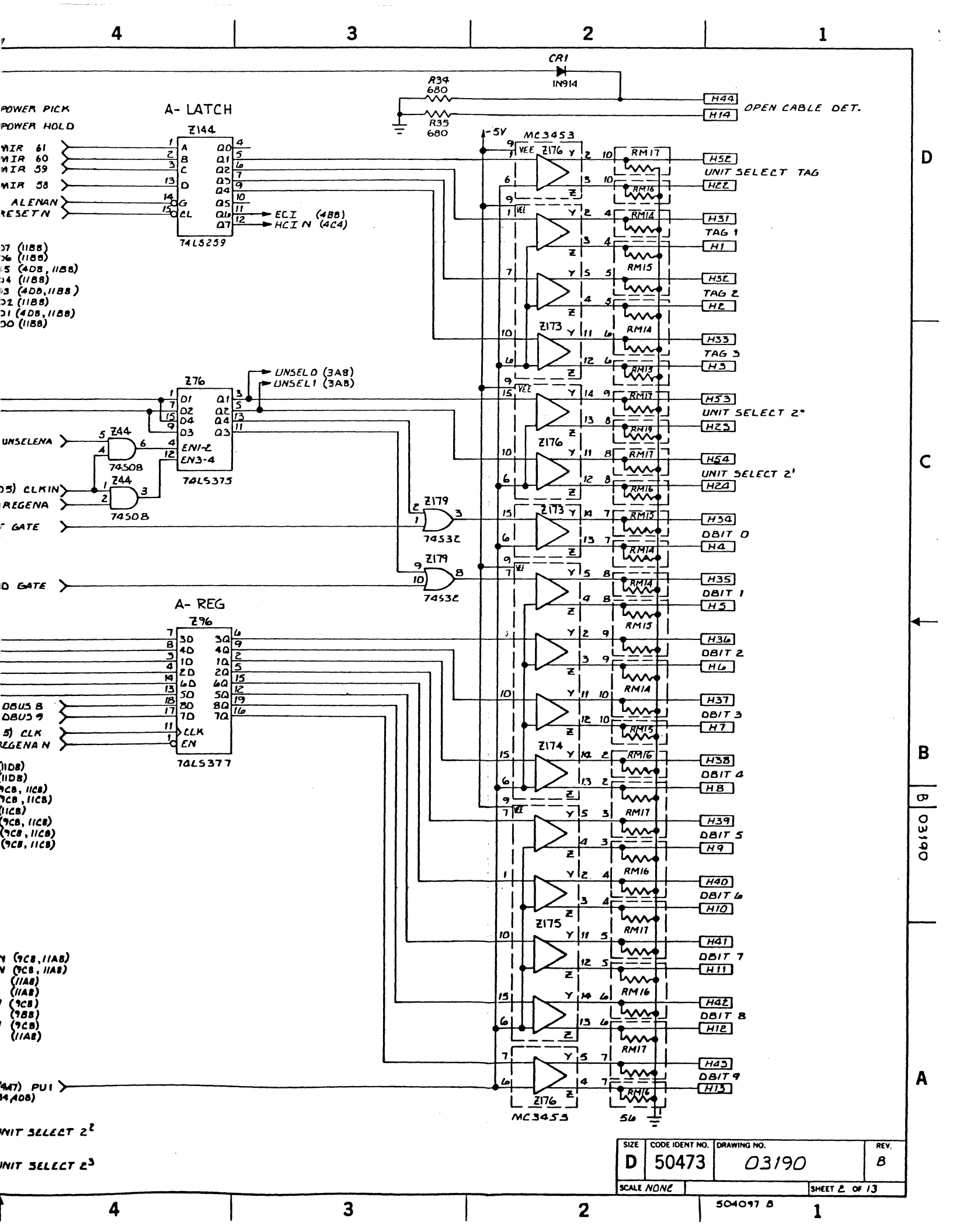
SCHEMATIC DIAGRAM
S33 SMD CONTROLLER

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B

SCALE NONE | SHEET 1 OF 13

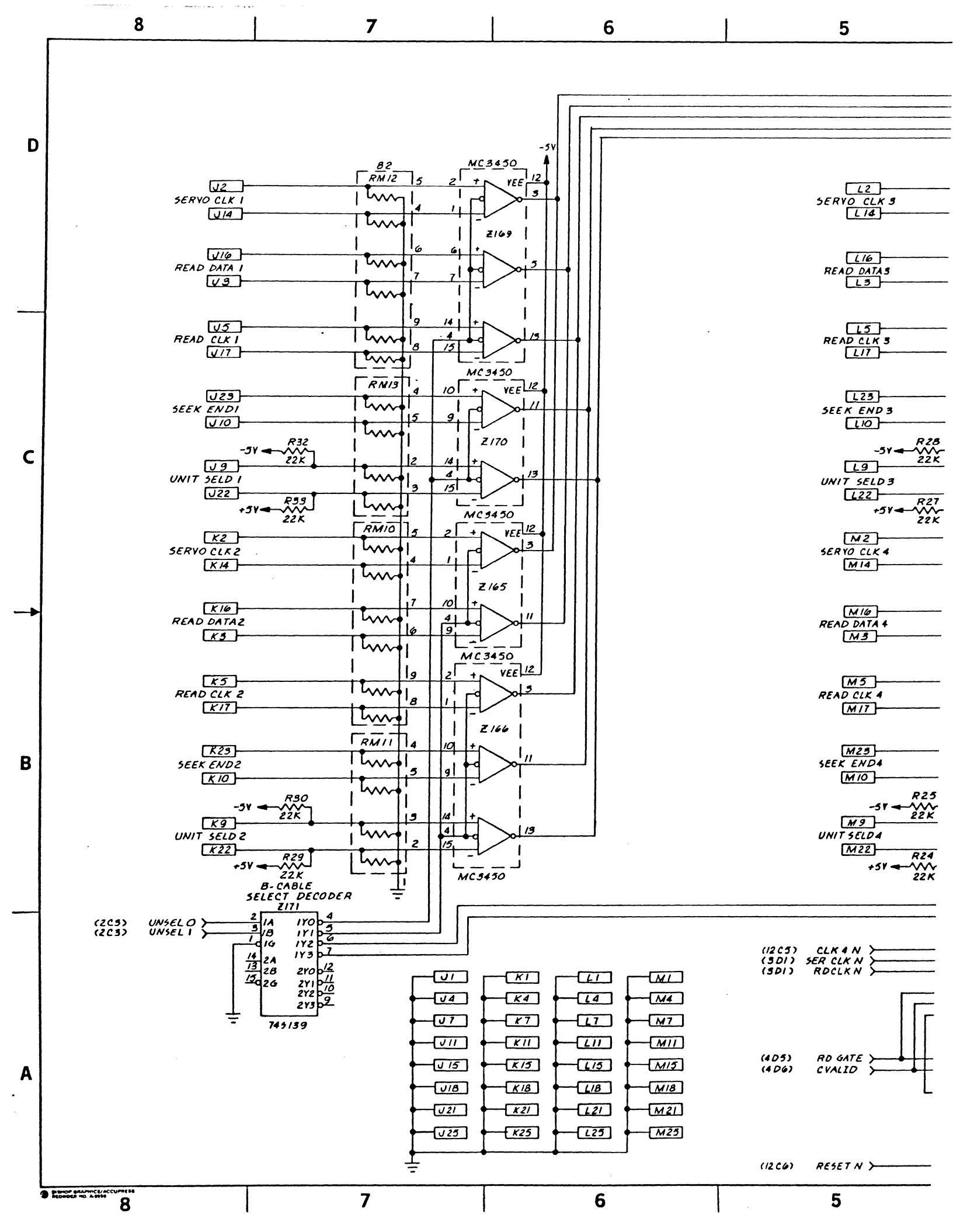
504097 B

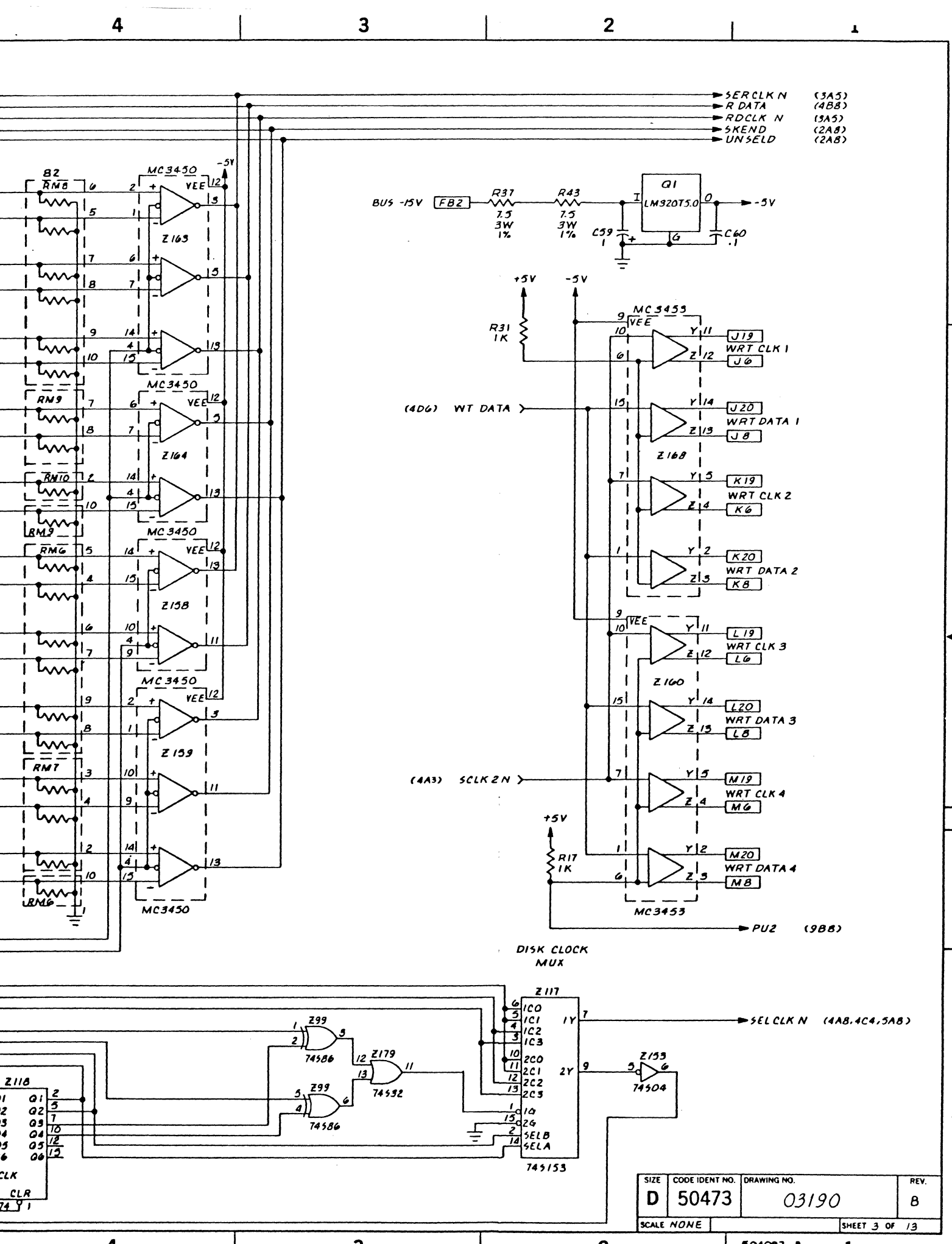

8
7
6
5
D
C
B
A
(12C5) DCLD N
Z180
75452
Z180
75452
H29
H59
(1381, 1301) M
(1381, 1301) M
(1381, 1301) M
(1381, 1301) M
(12A5)
(12C6) R
DBUS07
DBUS06
DBUS05
DBUS04
DBUS03
DBUS02
DBUS01
DBUS00
+5V
-5V
RM18
RM20
MC3450
VEE
-5V
Z179
74S32
IOSMK (2C6, 4D8)
SECTOR COUNTER
Z177
Z153
74S04
74LS393
Z97
74LS374
H55
SECTOR MARK
H25
H48
INDEX MARK
H18
H15
FAULT
H45
H16
SEEK ERROR
H46
H47
ON CYLINDER
H17
H49
UNIT READY
H19
H58
WRITE PROTECT
H28
H21
BUSY
H51
RM21
RM19
Z178
Z177
Z178
Z177
Z178
MC3450
22K
22K
56
(1281) SCNTENAN
(2C5) IOSMK
(12C1)
(405) WR
(405) F
(481,581,605,685,605,801,1081
(481,581,505,685,605,801,1081
(2
(12C1) A
Z151
74LS374
IMK
ISMK
ONC
RDY
WPT
BSYA
SEL
SENC
(301) UNSELD
(301) SKEND
Z122
74LS374
FAUL
SKE
BSE
FER
ORE
DNA
IRF
CRC
(483) BSER N
(483) FMT N
(4A1) ORE N
(5A1) DONE N
(4A1) IRF N
(4C3) CRCA N
(12C5) CLK4N
Z153
74S04
CLK
-5V +5V
R36 680
R42 680
R40 680
R41 680
H26
H56
H27
H57



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 2 OF 13

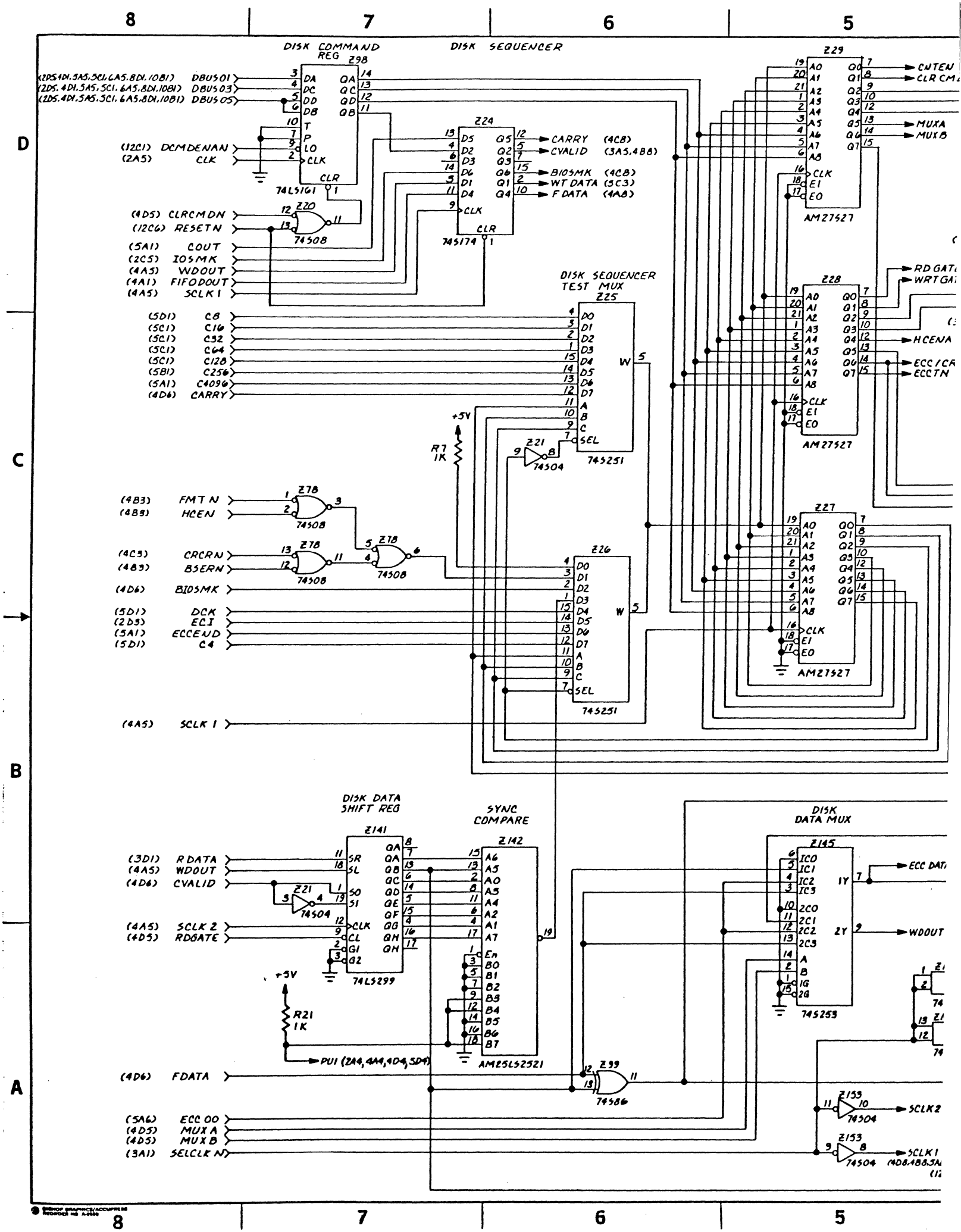
504097 B

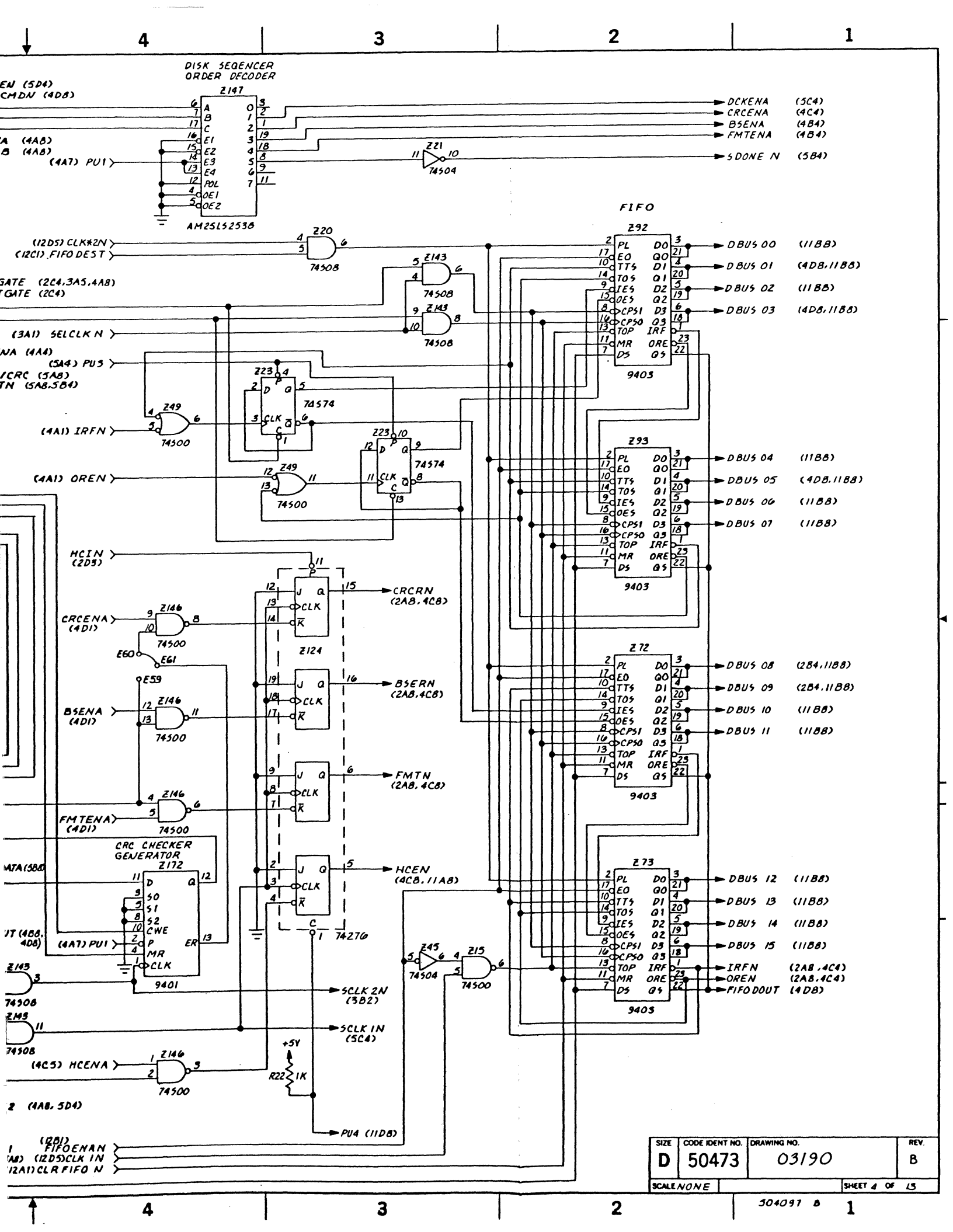

8
7
6
5
D
C
B
A
82
RM12
RM13
RM10
RM11
MC3450
Z169
Z170
Z165
Z166
VEE
-5V
+5V
J2
SERVO CLK 1
J14
J16
READ DATA 1
J3
J5
READ CLK 1
J17
J23
SEEK END1
J10
J9
UNIT SELD 1
J22
R32
22K
R33
22K
K2
SERVO CLK 2
K14
K16
READ DATA2
K3
K5
READ CLK 2
K17
K23
SEEK END2
K10
K9
UNIT SELD 2
K22
R30
R29
B-CABLE
SELECT DECODER
Z171
(2C3) UNSEL 0
(2C3) UNSEL 1
1A
1B
1G
2A
2B
2G
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
74S139
L2
SERVO CLK 3
L14
L16
READ DATA3
L3
L5
READ CLK 3
L17
L23
SEEK END 3
L10
L9
UNIT SELD 3
L22
R28
R27
M2
SERVO CLK 4
M14
M16
READ DATA 4
M3
M5
READ CLK 4
M17
M23
SEEK END4
M10
M9
UNIT SELD4
M22
R25
R24
J1
J4
J7
J11
J15
J18
J21
J25
K1
K4
K7
K11
K15
K18
K21
K25
L1
L4
L7
L11
L15
L18
L21
L25
M1
M4
M7
M11
M15
M18
M21
M25
(12C5) CLK 4 N
(3D1) SER CLK N
(3D1) RDCLK N
(4D5) RD GATE
(4D6) CVALID
(12C6) RESET N



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 3 OF 13

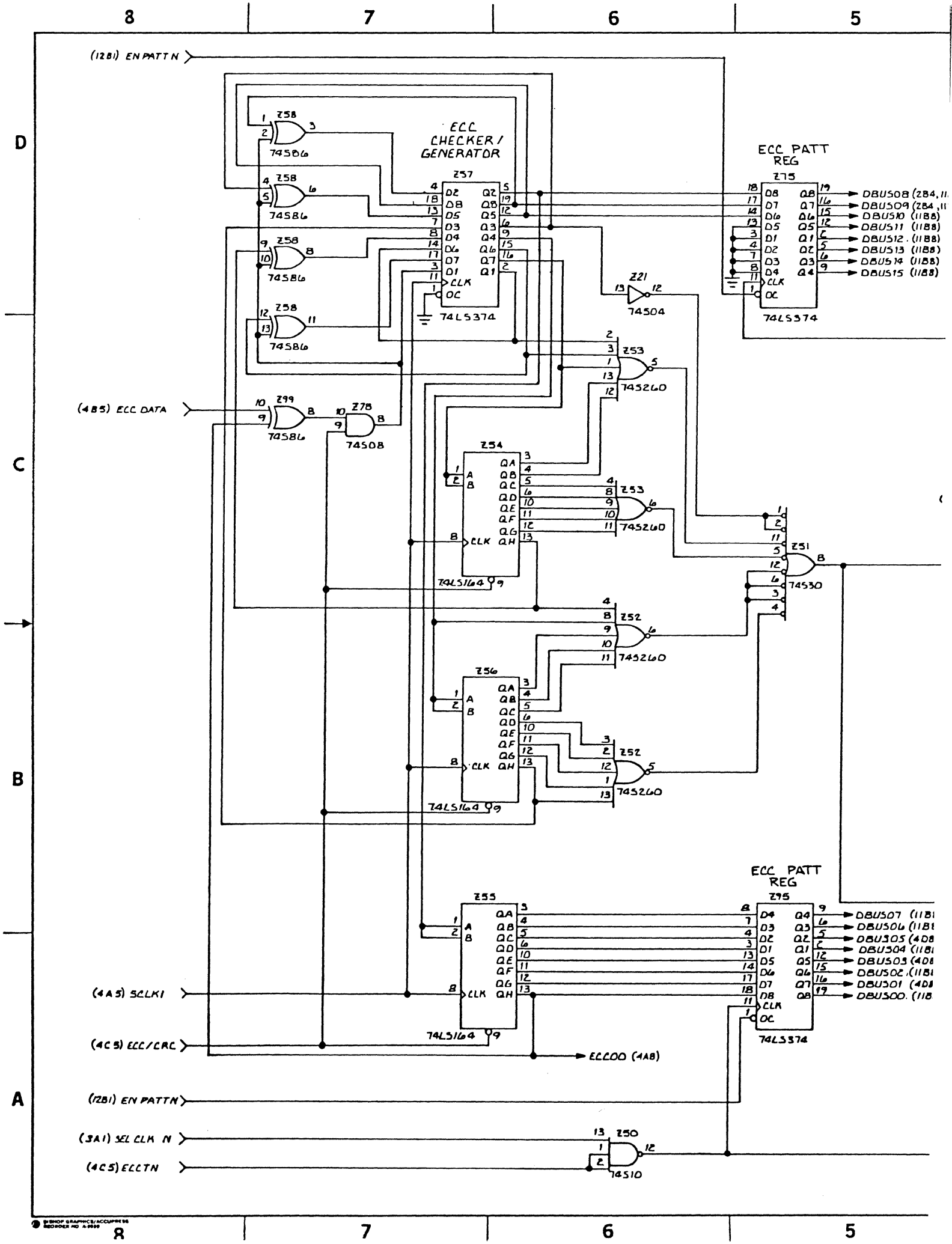
504097 B

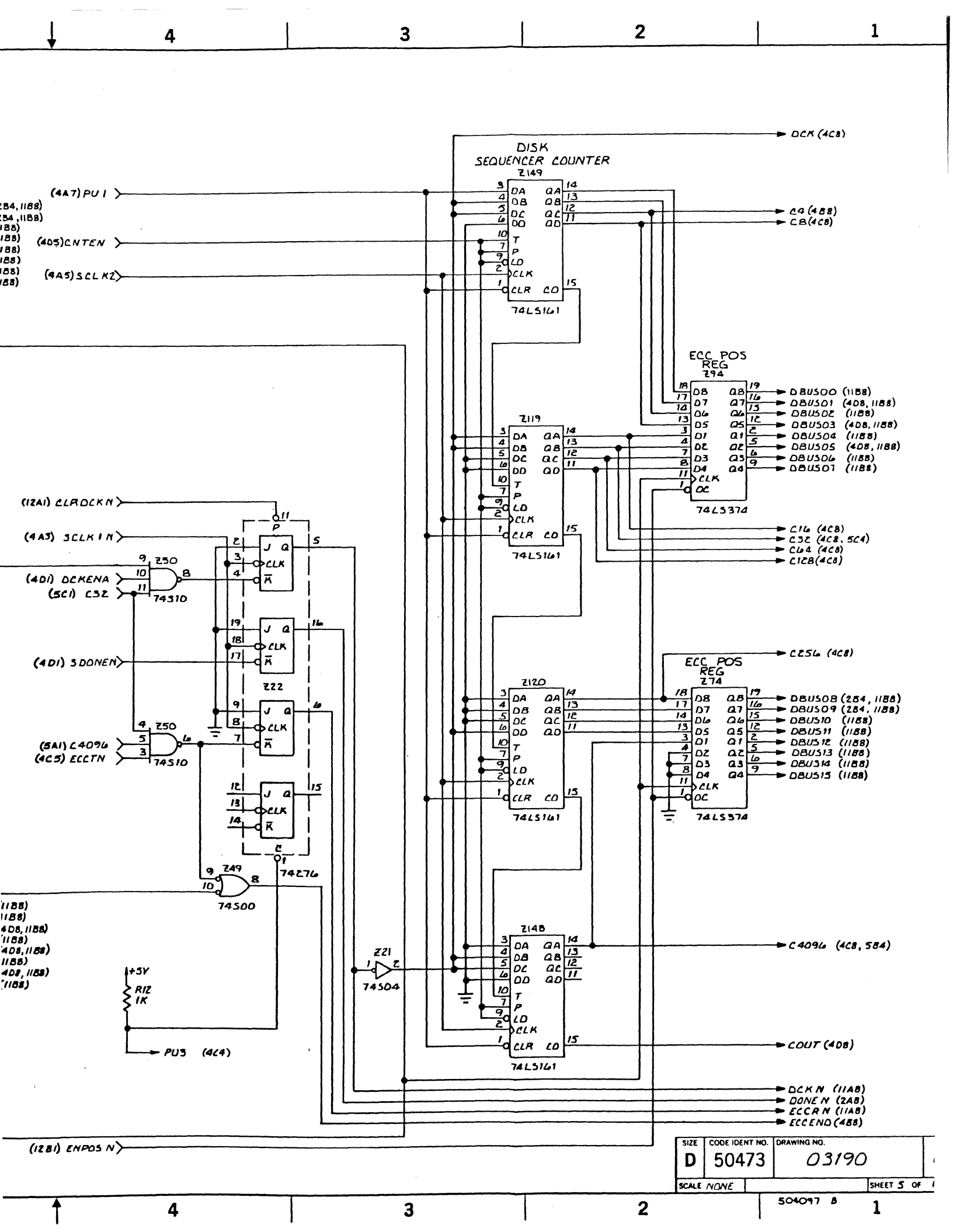

8
7
6
5
D
C
B
A
DISK COMMAND REG Z98
DISK SEQUENCER
DISK SEQUENCER TEST MUX Z225
DISK DATA SHIFT REG Z141
SYNC COMPARE Z142
DISK DATA MUX Z145
Z229
Z228
Z227
Z226
Z224
Z220
Z221
Z78
Z153
Z99
74LS161
74S174
74S08
74S04
74S251
74LS299
AM27S27
AM2SLS2521
74S86
74S253
R7 1K
R21 1K
+5V
(2D5,4D1,5A5,5C1,6A5,8D1,10B1) DBUS01
(2D5,4D1,5A5,5C1,6A5,8D1,10B1) DBUS03
(2D5,4D1,5A5,5C1,6A5,8D1,10B1) DBUS05
(12C1) DCMDENAN
(2A5) CLK
(4D5) CLRCMDN
(12C6) RESETN
(5A1) COUT
(2C5) IOSMK
(4A5) WDOUT
(4A1) FIFODOUT
(4A5) SCLK1
(5D1) C8
(5C1) C16
(5C1) C32
(5C1) C64
(5C1) C128
(5B1) C256
(5A1) C4096
(4D6) CARRY
(4B3) FMTN
(4B3) HCEN
(4C3) CRCRN
(4B3) BSERN
(4D6) BIOSMK
(5D1) DCK
(2D3) ECI
(5A1) ECCEND
(5D1) C4
(4A5) SCLK1
(3D1) RDATA
(4A5) WDOUT
(4D6) CVALID
(4A5) SCLK2
(4D5) RDGATE
(4D6) FDATA
(5A6) ECC00
(4D5) MUXA
(4D5) MUXB
(3A1) SELCLKN
CARRY (4C8)
CVALID (3A5,4B8)
BIOSMK (4C8)
WT DATA (3C3)
F DATA (4A8)
CNTEN
CLR CM
MUXA
MUXB
RD GAT
WRT GA
HCENA
ECC/CR
ECCTN
ECC DAT
WDOUT
SCLK2
SCLK1
PU1 (2A4,4A4,4D4,5D4)



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 4 OF 13

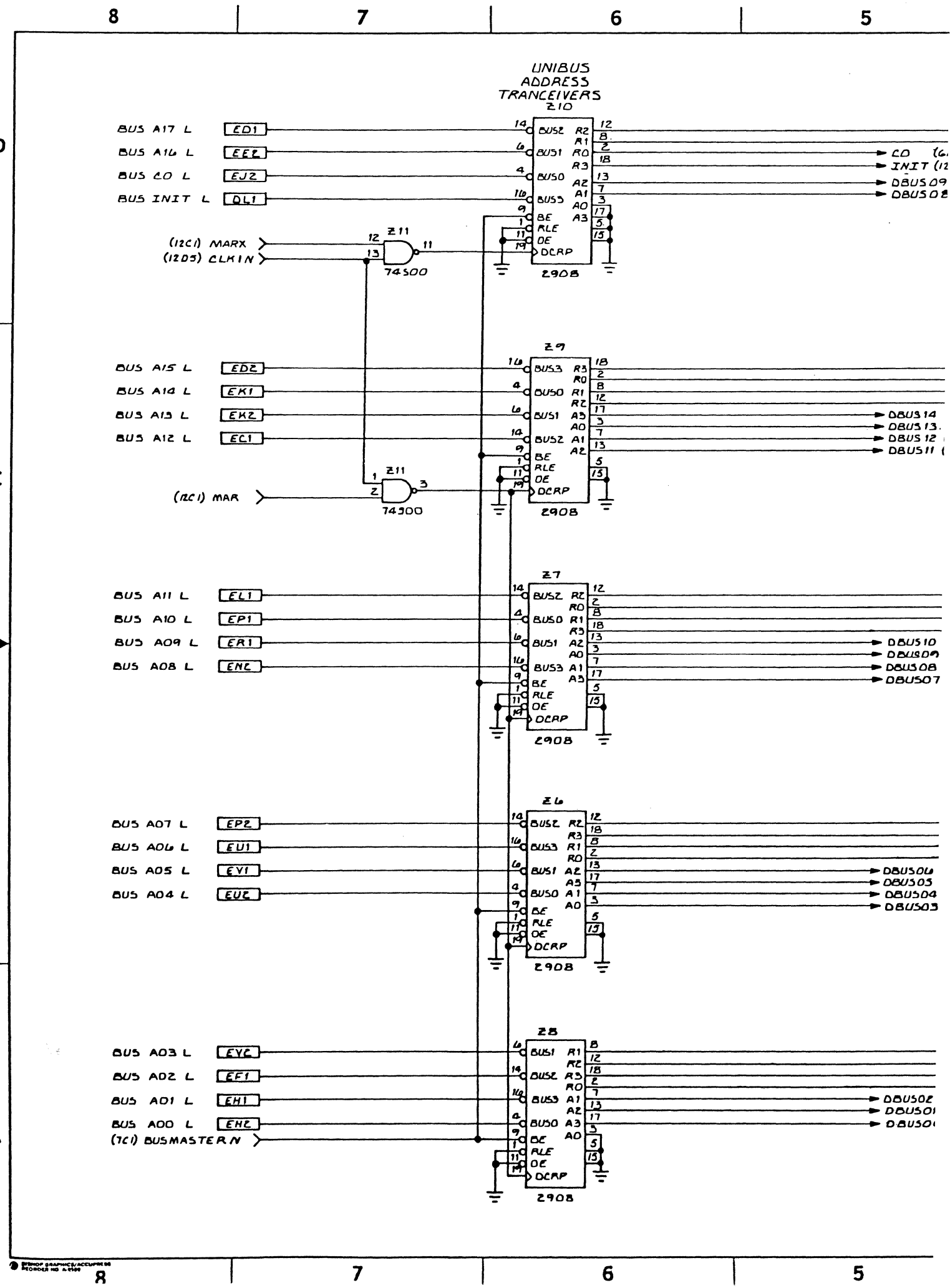
304097 B

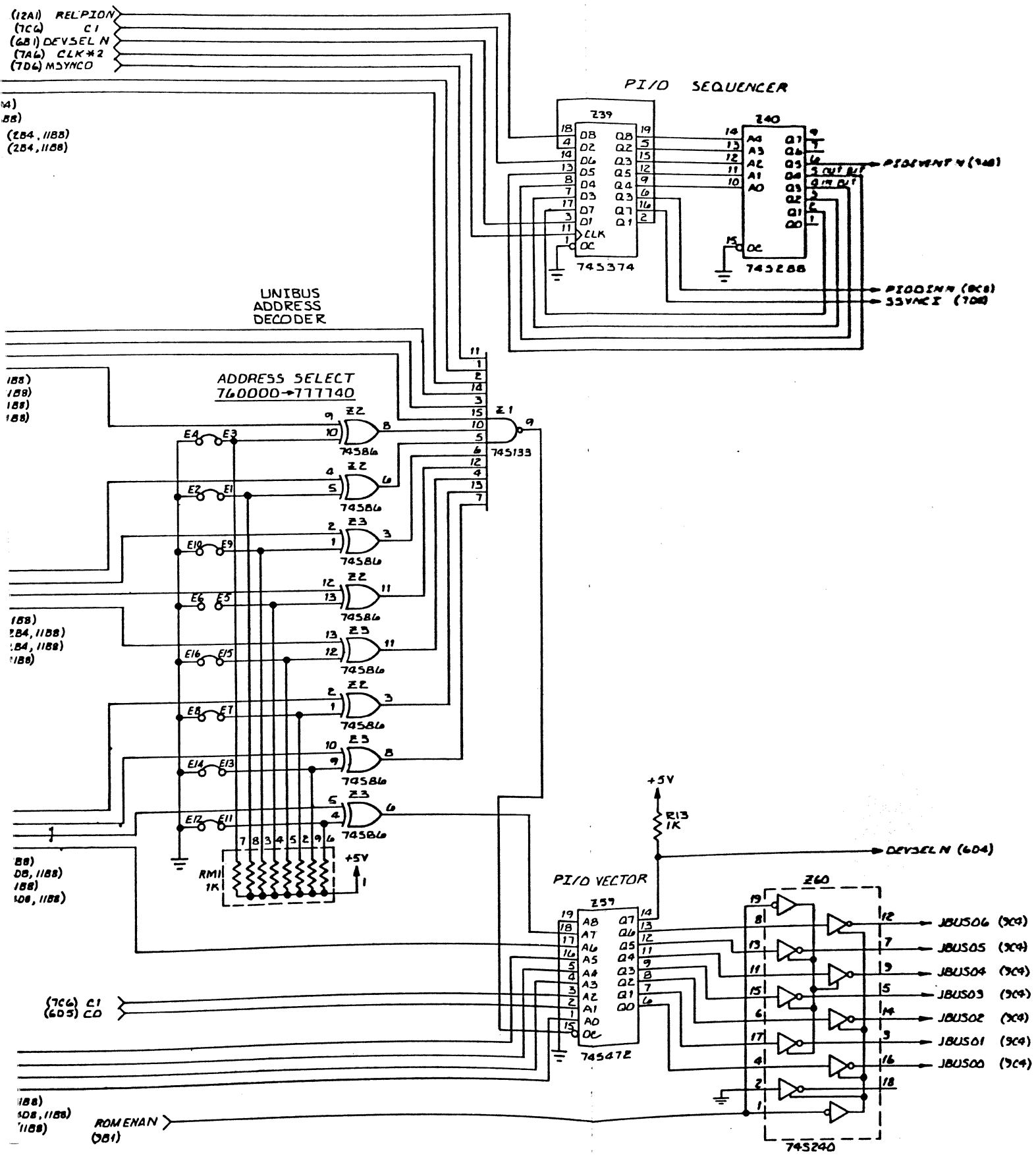

8
7
6
5
D
C
B
A
(128I) EN PATT N
ECC CHECKER / GENERATOR
Z57
74LS374
ECC PATT REG
Z75
74LS374
DBUS08 (Z84,11
DBUS09 (Z84,11
DBUS10 (1188)
DBUS11 (1188)
DBUS12 (1188)
DBUS13 (1188)
DBUS14 (1188)
DBUS15 (1188)
Z58
74S86
Z21
74S04
Z53
74S260
(48S) ECC DATA
Z99
74S86
Z78
74S08
Z54
74LS164
Z51
74S30
Z52
Z56
Z55
ECC PATT REG
Z95
74LS374
DBUS07 (118
DBUS06 (118
DBUS05 (408
DBUS04 (118
DBUS03 (408
DBUS02 (118
DBUS01 (408
DBUS00 (118
(4A5) SCLK1
(4C5) ECC/CRC
ECCOO (4AB)
(128I) EN PATT N
(3A1) SEL CLK N
(4C5) ECC TN
Z50
74S10



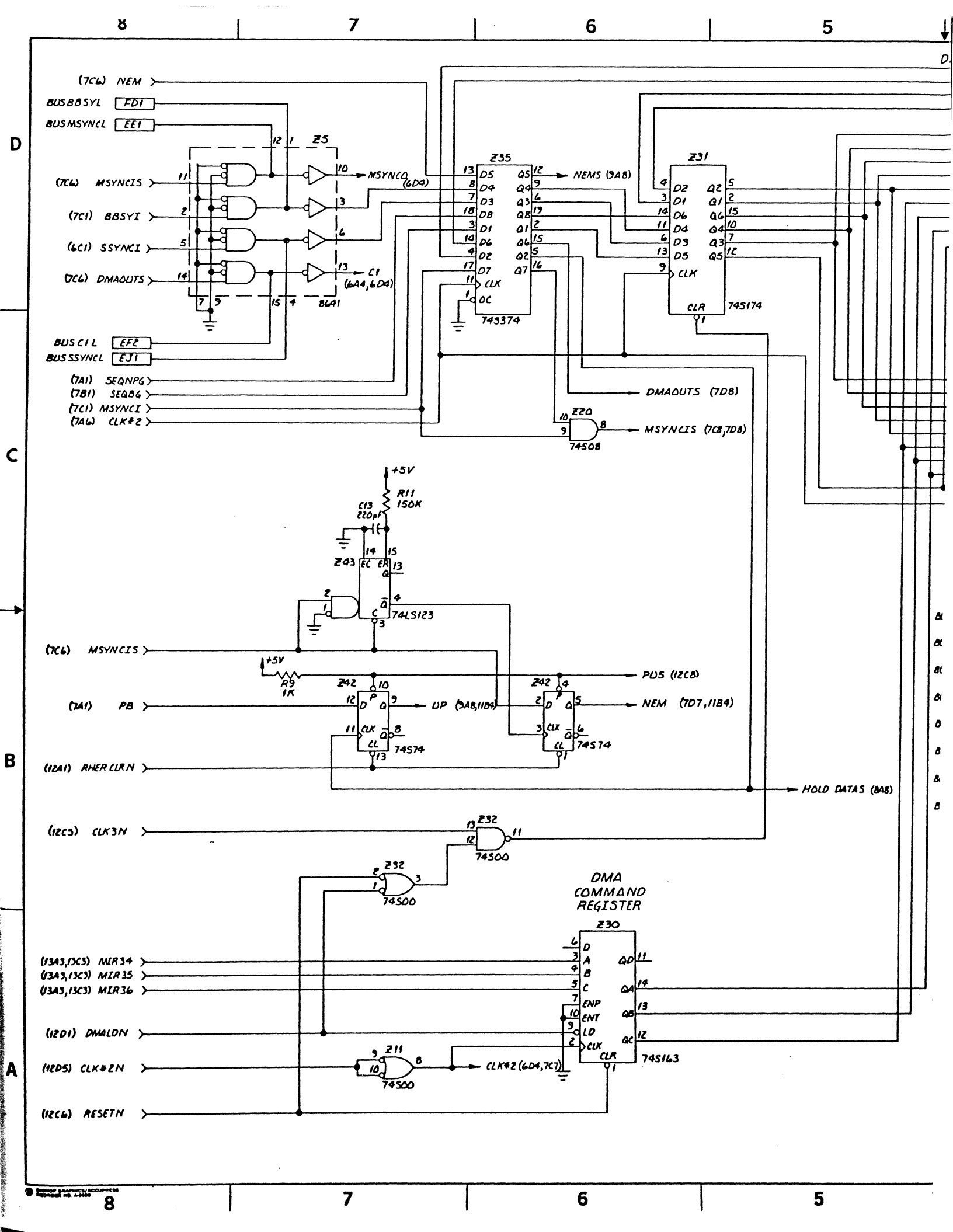
SIZE	CODE IDENT NO.	DRAWING NO.
D	50473	03190
SCALE NONE		SHEET 5 OF

504097 B

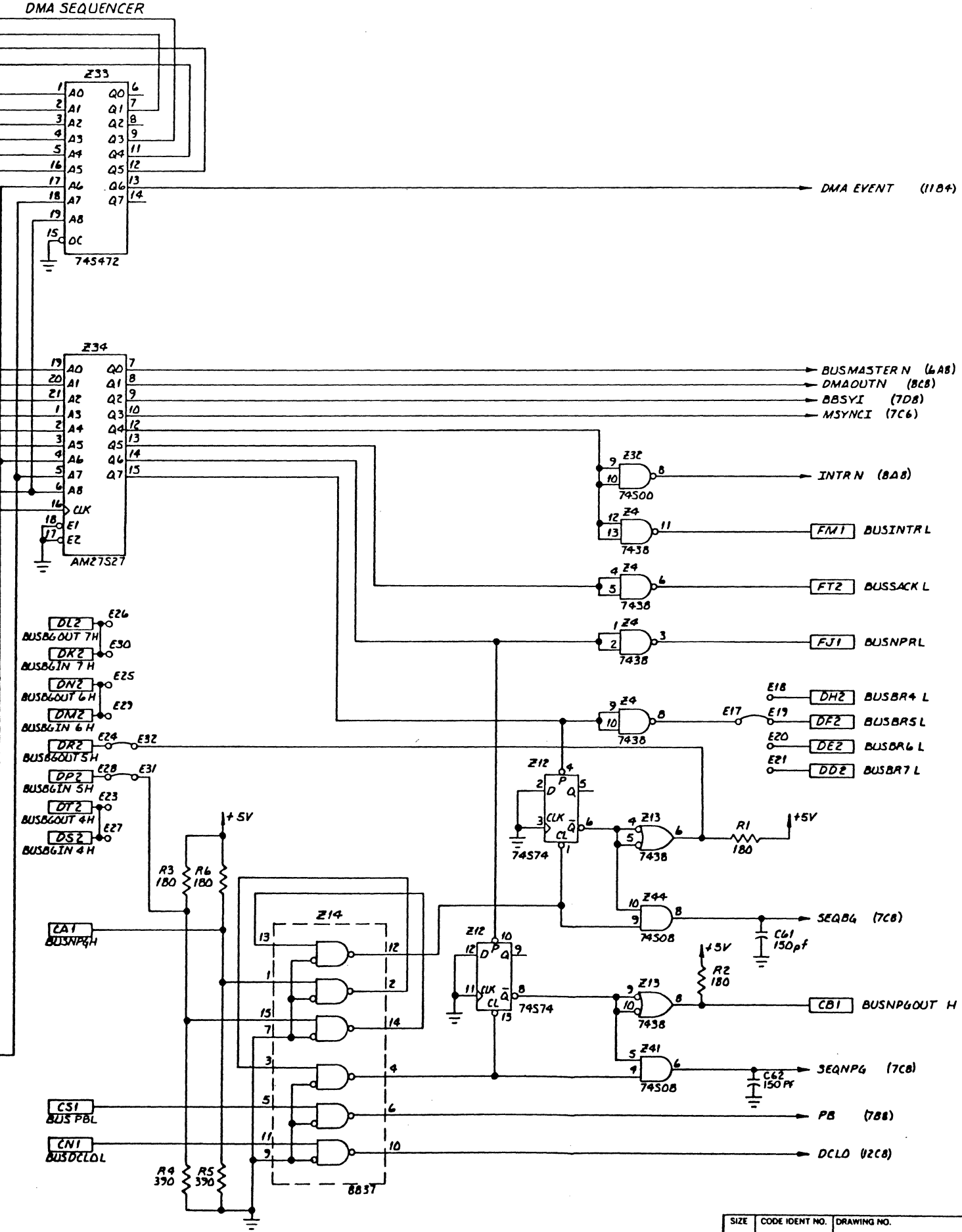

UNIBUS
ADDRESS
TRANCEIVERS
Z10
BUS A17 L
BUS A16 L
BUS A0 L
BUS INIT L
(12C1) MARX
(12D5) CLKIN
74S00
Z11
Z908
Z9
BUS A15 L
BUS A14 L
BUS A13 L
BUS A12 L
(7C1) MAR
Z7
BUS A11 L
BUS A10 L
BUS A09 L
BUS A08 L
Z6
BUS A07 L
BUS A06 L
BUS A05 L
BUS A04 L
Z8
BUS A03 L
BUS A02 L
BUS A01 L
BUS A00 L
(7C1) BUSMASTER N
DBUS14
DBUS13
DBUS12
DBUS11
DBUS10
DBUS09
DBUS08
DBUS07
DBUS06
DBUS05
DBUS04
DBUS03
DBUS02
DBUS01
DBUS00



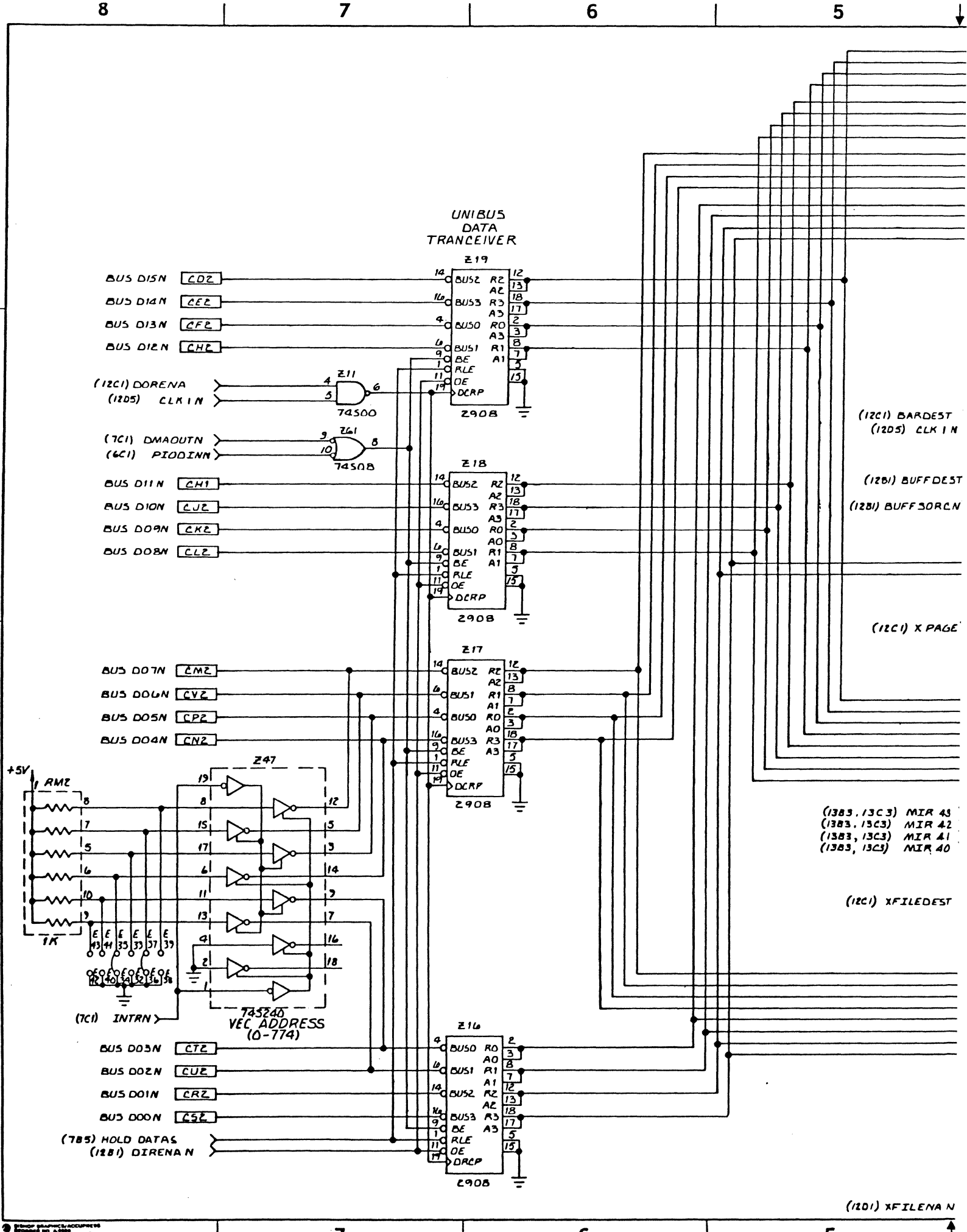
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 6 OF 13

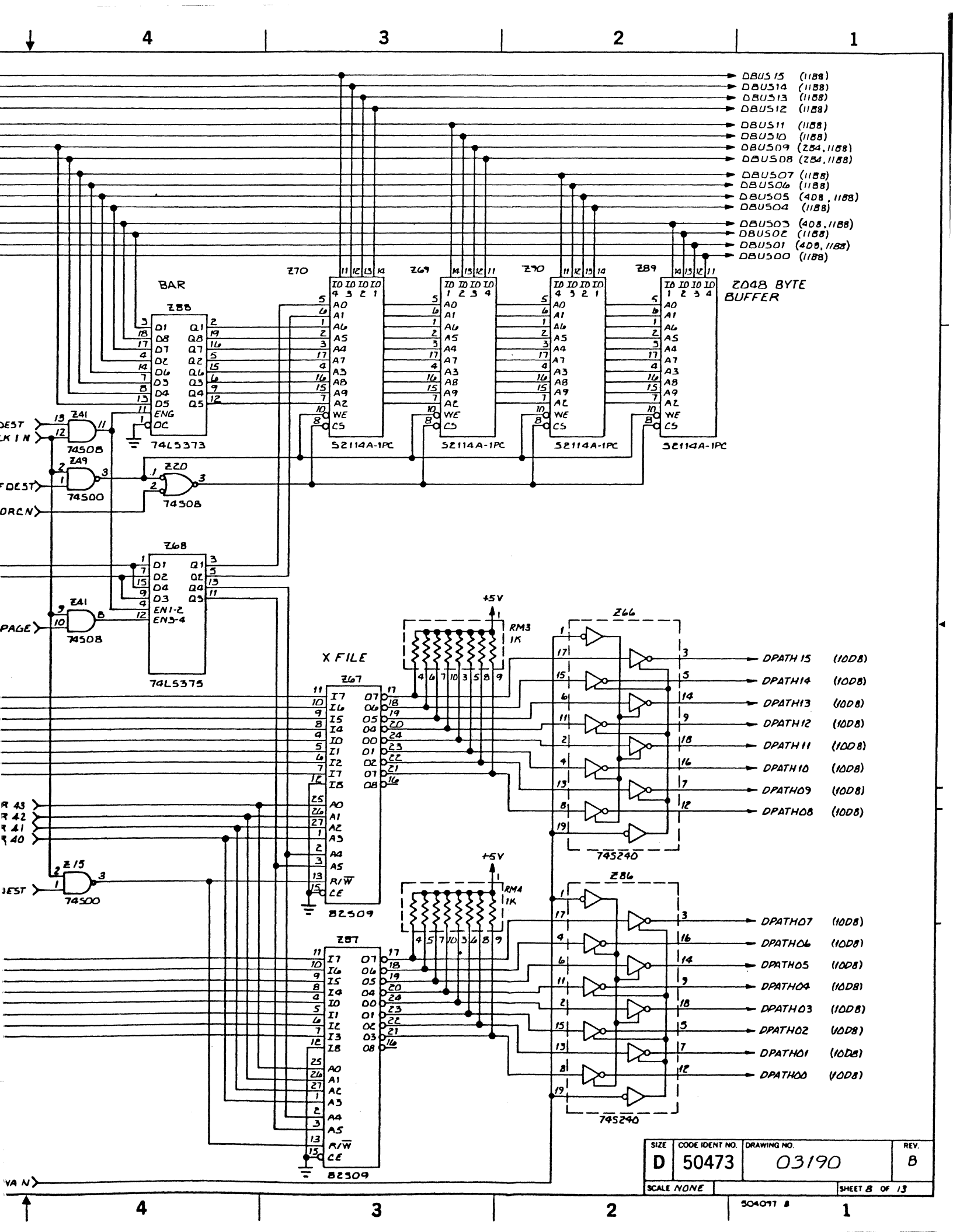

8
7
6
5
D
C
B
A
(7C4) NEM
BUSBBSYL FD1
BUSMSYNCL EE1
Z5
(7C4) MSYNCIS
(7C1) BBSYI
(6C1) SSYNCI
(7C4) DMAOUTS
MSYNCO (6D4)
C1 (6A4,6D4)
8641
BUSC1L EF2
BUSSSYNCL EJ1
(7A1) SEQNPG
(7B1) SEQBG
(7C1) MSYNCI
(7A4) CLK*2
Z35
74S374
NEMS (9A8)
Z31
74S174
DMAOUTS (7D8)
Z20
74S08
MSYNCIS (7C8,7D8)
+5V
R11 150K
C13 220pf
Z43
74LS123
(7C6) MSYNCIS
R9 1K
Z42
74S74
(7A1) PB
UP (9A8,11B4)
PUS (12C8)
NEM (7D7,11B4)
(12A1) RHERCLRN
HOLD DATAS (8A8)
(12C5) CLK3N
Z32
74S00
DMA COMMAND REGISTER
Z30
74S163
(13A3,13C3) MIR34
(13A3,13C3) MIR35
(13A3,13C3) MIR36
(12D1) DMALDN
(12D5) CLK*2N
Z11
CLK*2 (6D4,7C1)
(12C6) RESETN

DMA SEQUENCER



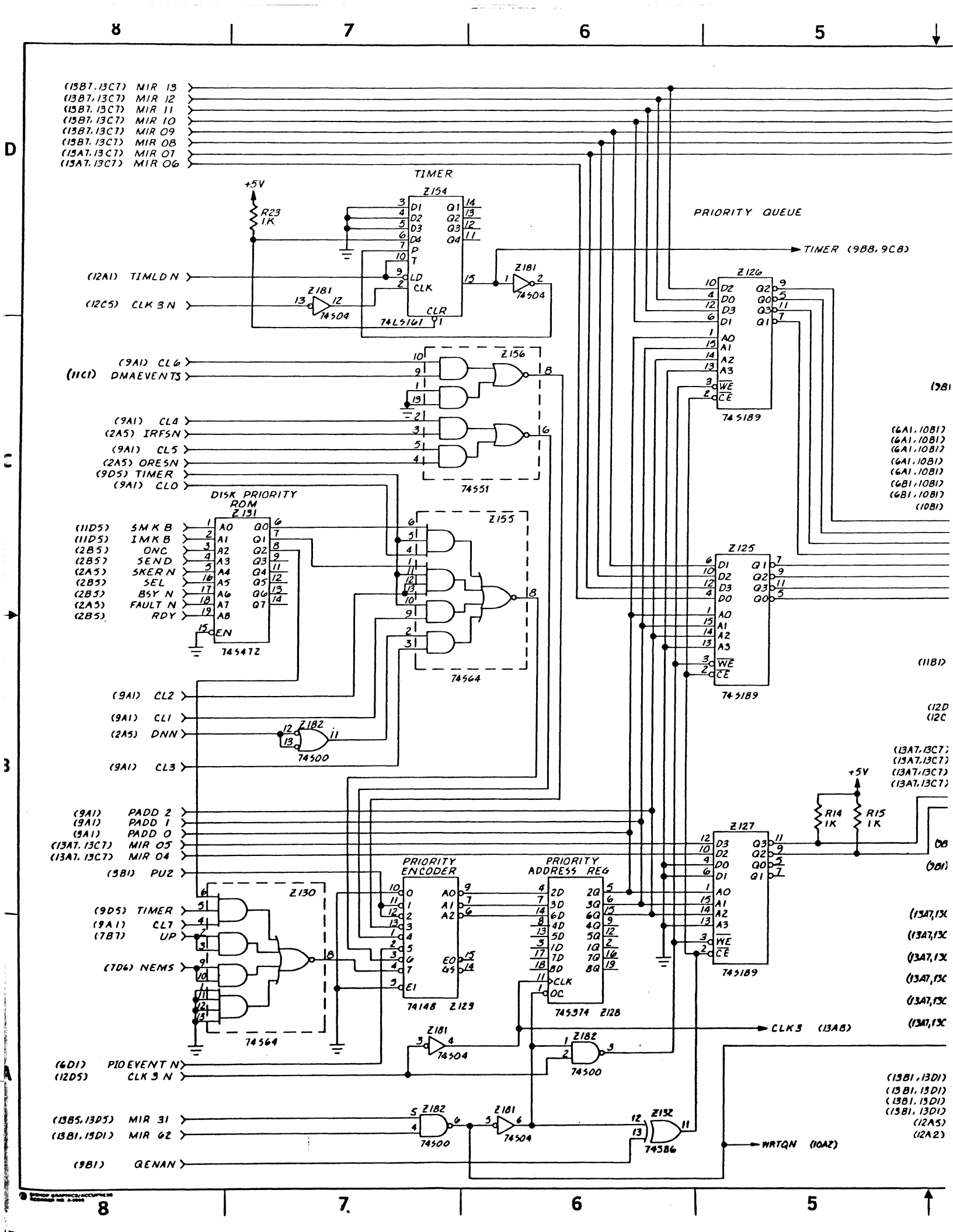
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 7 OF 13

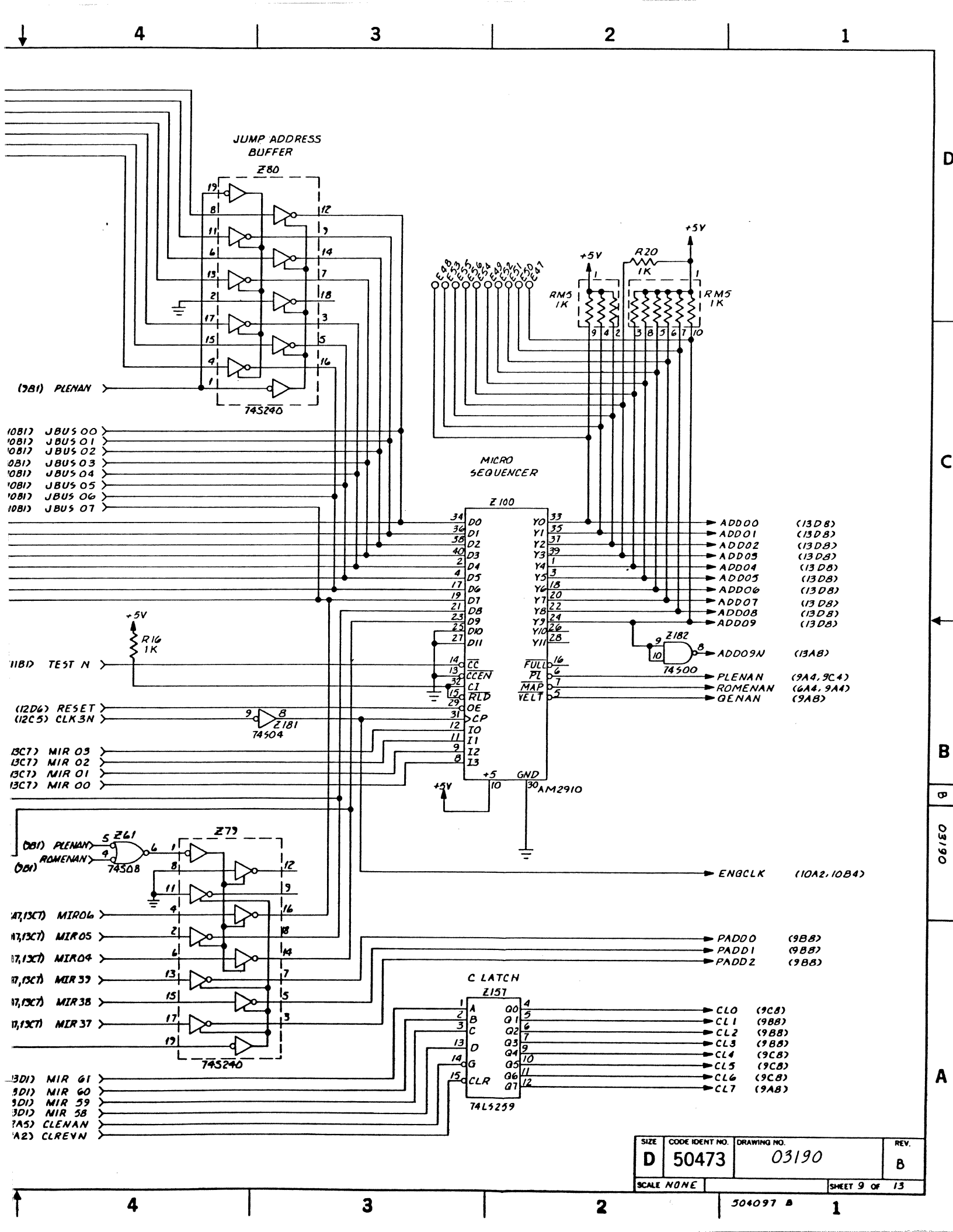

UNIBUS
DATA
TRANCEIVER
Z19
Z18
Z17
Z16
2908
Z11
74S00
Z61
74S08
Z47
74S240
VEC ADDRESS
(0-774)
BUS DI5N
BUS DI4N
BUS DI3N
BUS DI2N
BUS DI1N
BUS DI0N
BUS DO9N
BUS DO8N
BUS DO7N
BUS DO6N
BUS DO5N
BUS DO4N
BUS DO3N
BUS DO2N
BUS DO1N
BUS DO0N
(12C1) DORENA
(1205) CLK IN
(7C1) DMAOUTN
(6C1) PIODINN
(7C1) INTRN
(785) HOLD DATAS
(1281) DIRENA N
+5V
1K
(12C1) BARDEST
(1205) CLK IN
(12B1) BUFFDEST
(12B1) BUFFSORCN
(12C1) X PAGE
(1383, 13C3) MIR 43
(1383, 13C3) MIR 42
(1383, 13C3) MIR 41
(1383, 13C3) MIR 40
(12C1) XFILEDEST
(1201) XFILENA N



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 8 OF 13

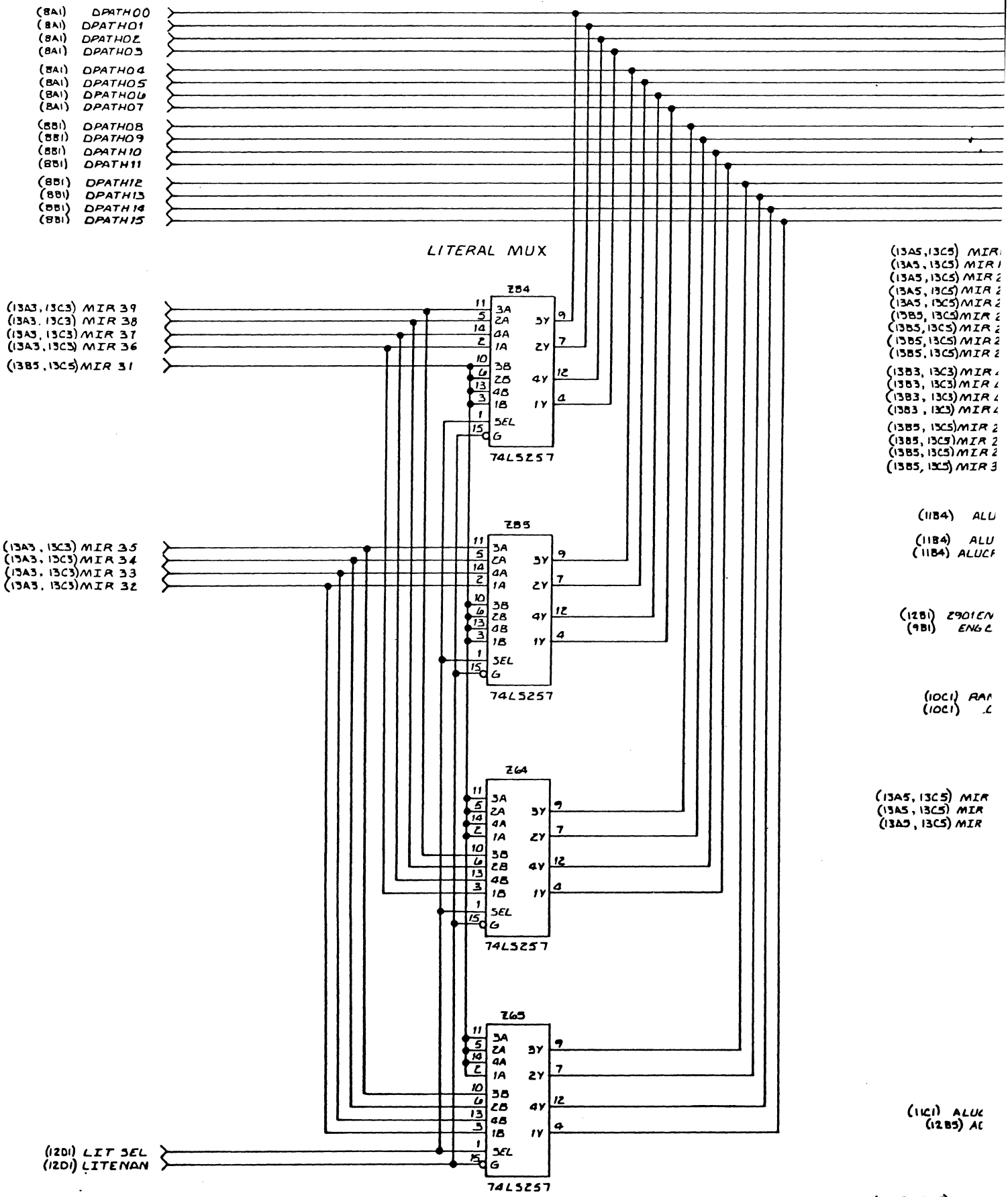
504097 8

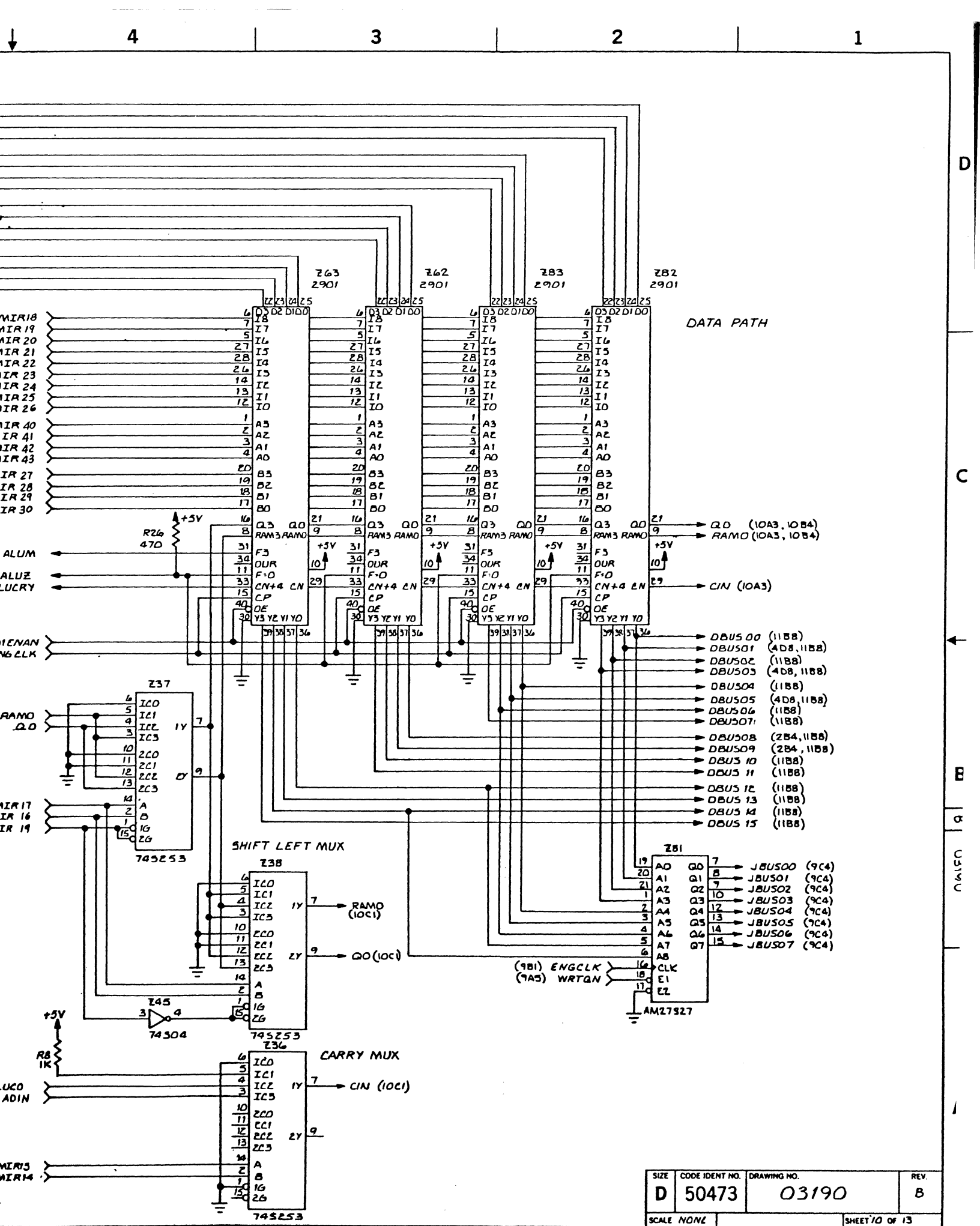

(13B7, 13C7) MIR 13
(13B7, 13C7) MIR 12
(13B7, 13C7) MIR 11
(13B7, 13C7) MIR 10
(13B7, 13C7) MIR 09
(13B7, 13C7) MIR 08
(13A7, 13C7) MIR 07
(13A7, 13C7) MIR 06
TIMER
+5V
R23 1K
Z154
74LS161
(12A1) TIMLD N
(12C5) CLK 3 N
Z181
74S04
PRIORITY QUEUE
TIMER (9B8, 9C8)
Z126
74S189
(9A1) CL6
(11C1) DMAEVENTS
(9A1) CL4
(2A5) IRFSN
(9A1) CL5
(2A5) ORESN
(9D5) TIMER
(9A1) CL0
Z156
74S51
DISK PRIORITY ROM
Z131
74S472
(11D5) SMK B
(11D5) IMK B
(2B5) ONC
(2B5) SEND
(2A5) SKERN
(2B5) SEL
(2B5) BSY N
(2A5) FAULT N
(2B5) RDY
Z155
74S64
Z125
74S189
(9A1) CL2
(9A1) CL1
(2A5) DNN
Z182
74S00
(9A1) CL3
(9A1) PADD 2
(9A1) PADD 1
(9A1) PADD 0
(13A7, 13C7) MIR 05
(13A7, 13C7) MIR 04
(9B1) PU2
PRIORITY ENCODER
74148
Z129
PRIORITY ADDRESS REG
74S374
Z128
Z127
74S189
R14 1K
R15 1K
Z130
74S64
(9D5) TIMER
(9A1) CL7
(7B7) UP
(7D6) NEMS
CLK 3 (13A8)
(6D1) PIOEVENT N
(12D5) CLK 3 N
(13B5, 13D5) MIR 31
(13B1, 13D1) MIR 02
Z132
74S86
WRTQN (10A2)
(9B1) QENAN



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 9 OF 13

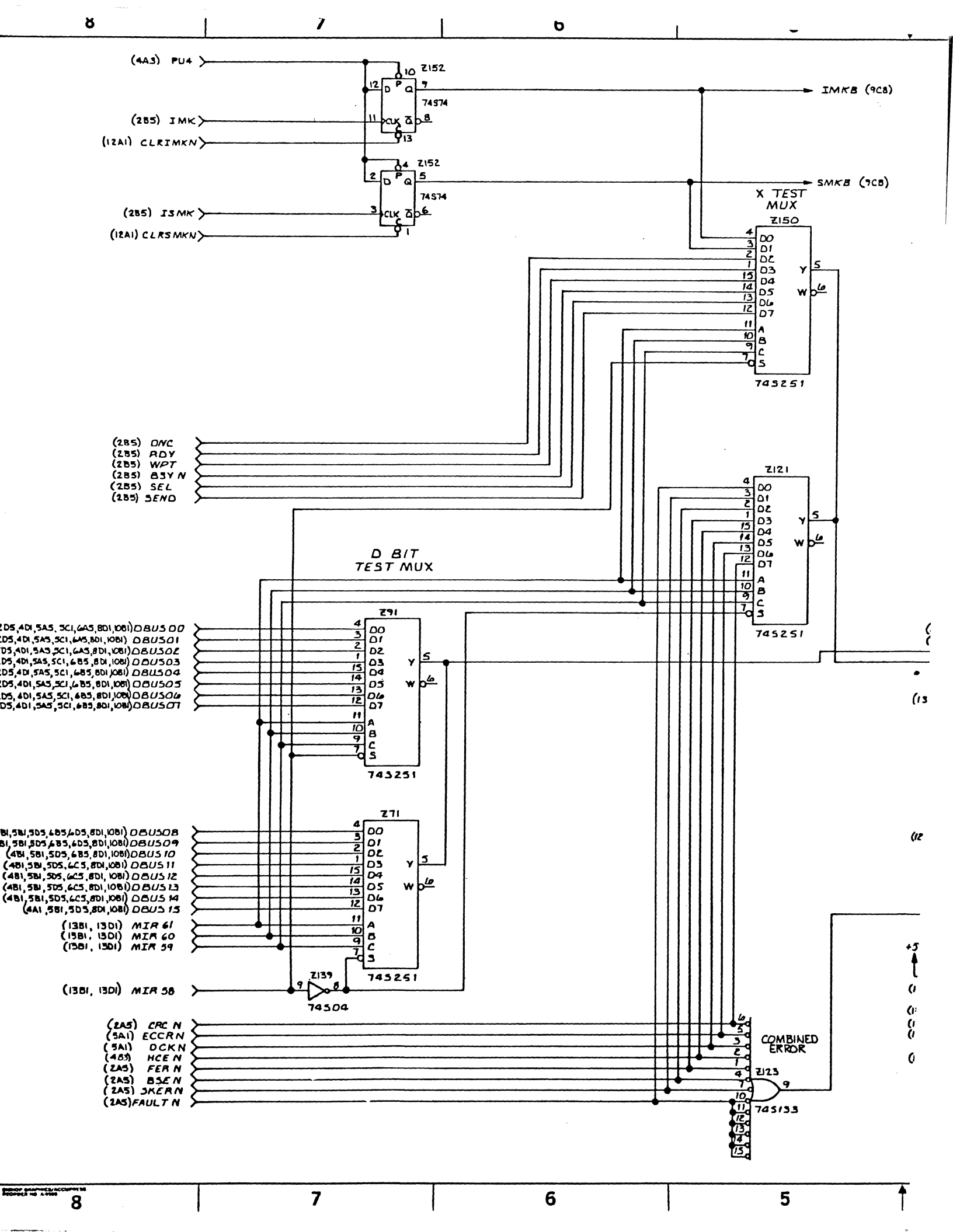
504097 B


(8A1) DPATH00
(8A1) DPATH01
(8A1) DPATH02
(8A1) DPATH03
(8A1) DPATH04
(8A1) DPATH05
(8A1) DPATH06
(8A1) DPATH07
(8B1) DPATH08
(8B1) DPATH09
(8B1) DPATH10
(8B1) DPATH11
(8B1) DPATH12
(8B1) DPATH13
(8B1) DPATH14
(8B1) DPATH15
LITERAL MUX
(13A3,13C3) MIR 39
(13A3, 13C3) MIR 38
(13A3, 13C3) MIR 37
(13A3, 13C3) MIR 36
(13B5, 13C5) MIR 31
Z84
74LS257
(13A3, 13C3) MIR 35
(13A3, 13C3) MIR 34
(13A3, 13C3) MIR 33
(13A3, 13C3) MIR 32
Z85
74LS257
Z64
74LS257
Z65
74LS257
(12D1) LIT SEL
(12D1) LITENAN
3A
2A
4A
1A
3B
2B
4B
1B
SEL
G
3Y
2Y
4Y
1Y



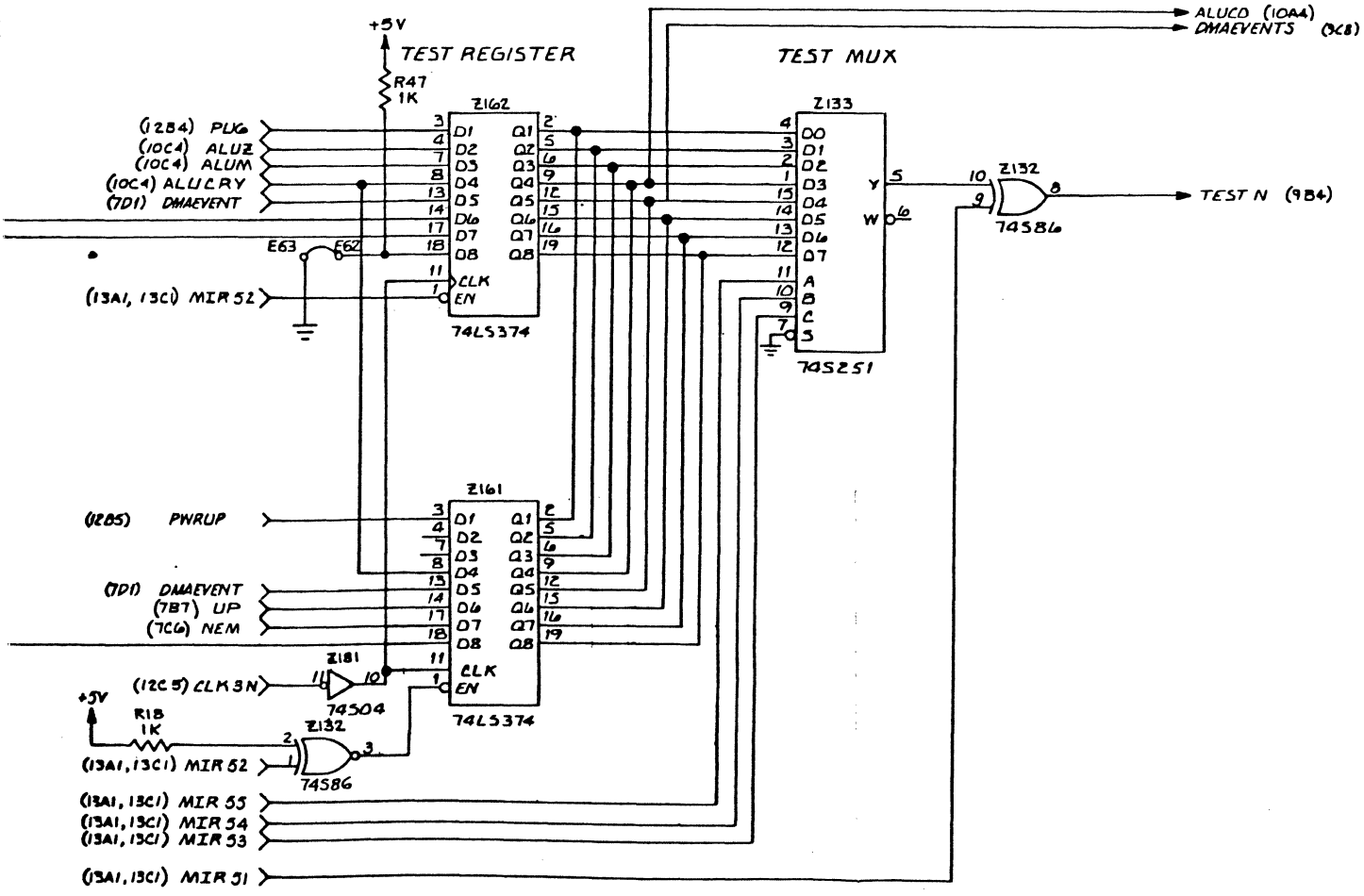
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 10 OF 13

504097 B

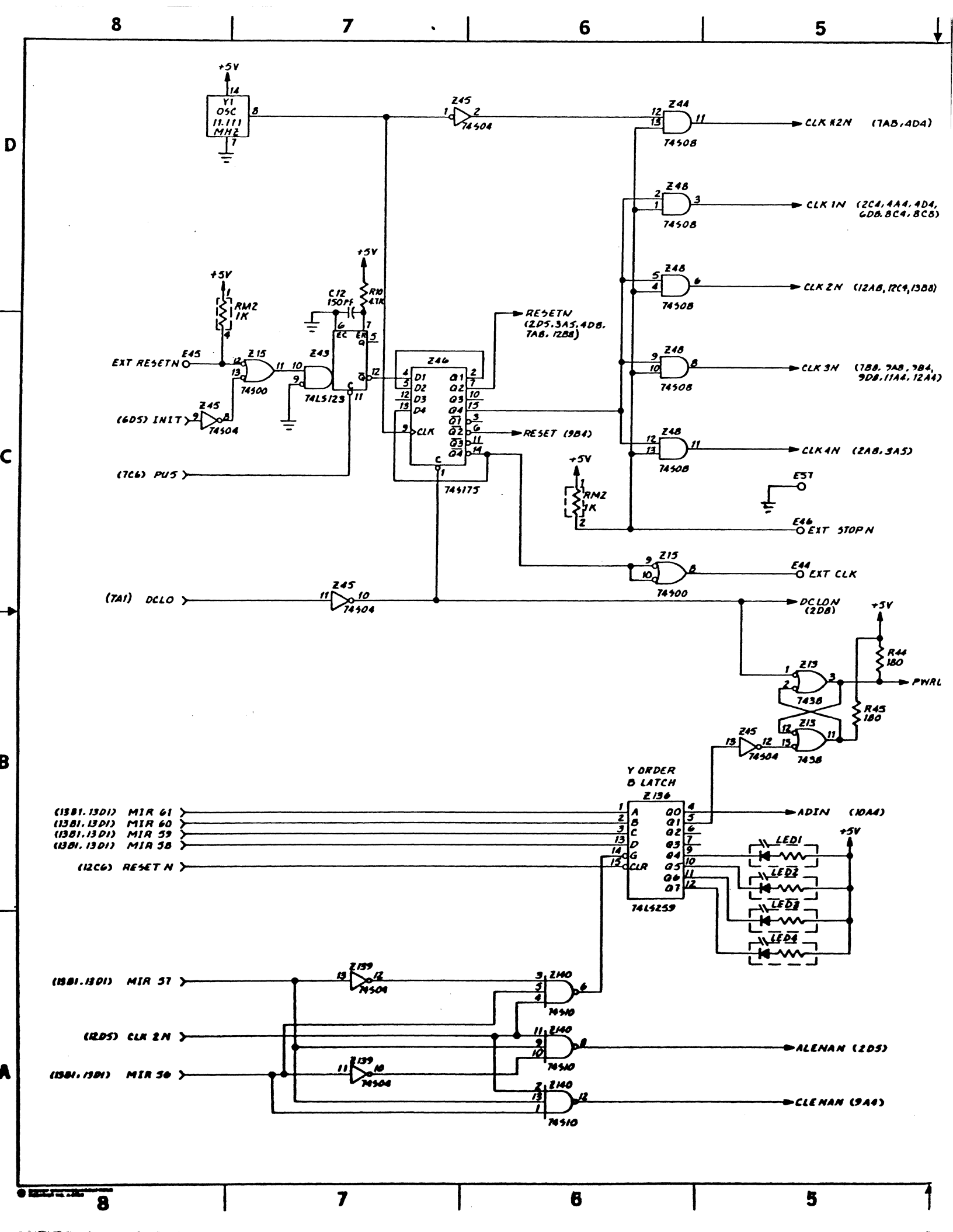

(4A3) PU4
(28S) IMK
(12A1) CLRIMKN
(28S) ISMK
(12A1) CLRSMKN
Z152
74S74
IMKB (9C8)
SMKB (9C8)
X TEST MUX
Z150
74S251
(28S) DNC
(28S) RDY
(28S) WPT
(28S) BSY N
(28S) SEL
(28S) SEND
Z121
D BIT TEST MUX
Z91
Z71
(13B1, 13D1) MIR 61
(13B1, 13D1) MIR 60
(13B1, 13D1) MIR 59
(13B1, 13D1) MIR 58
Z139
74S04
(2A5) CRC N
(5A1) ECCRN
(5A1) DCKN
(4B3) HCE N
(2A5) FER N
(2A5) BSE N
(2A5) SKERN
(2A5) FAULT N
COMBINED ERROR
Z123
74S133
+5

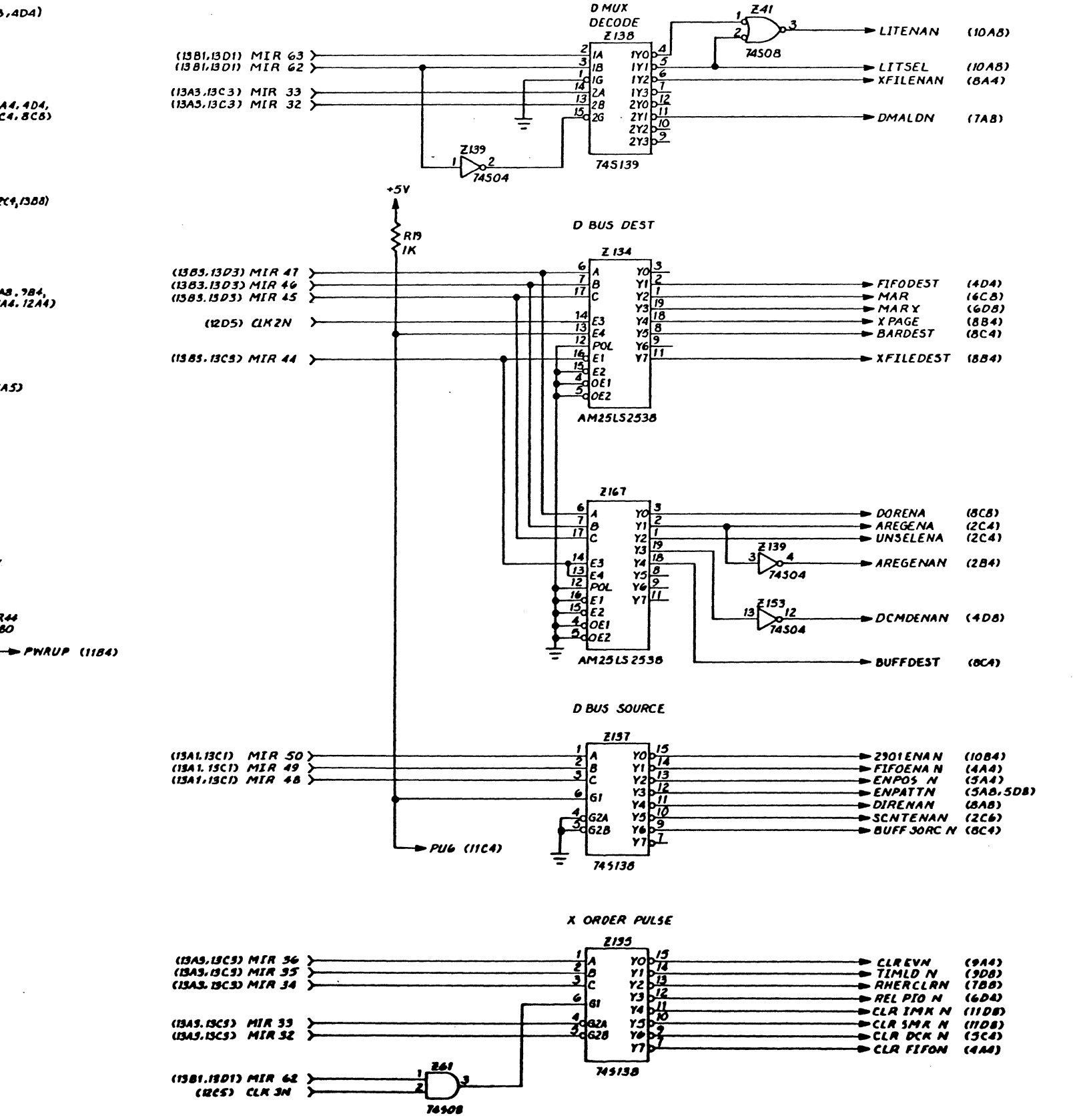
(9C8)

(9C8)



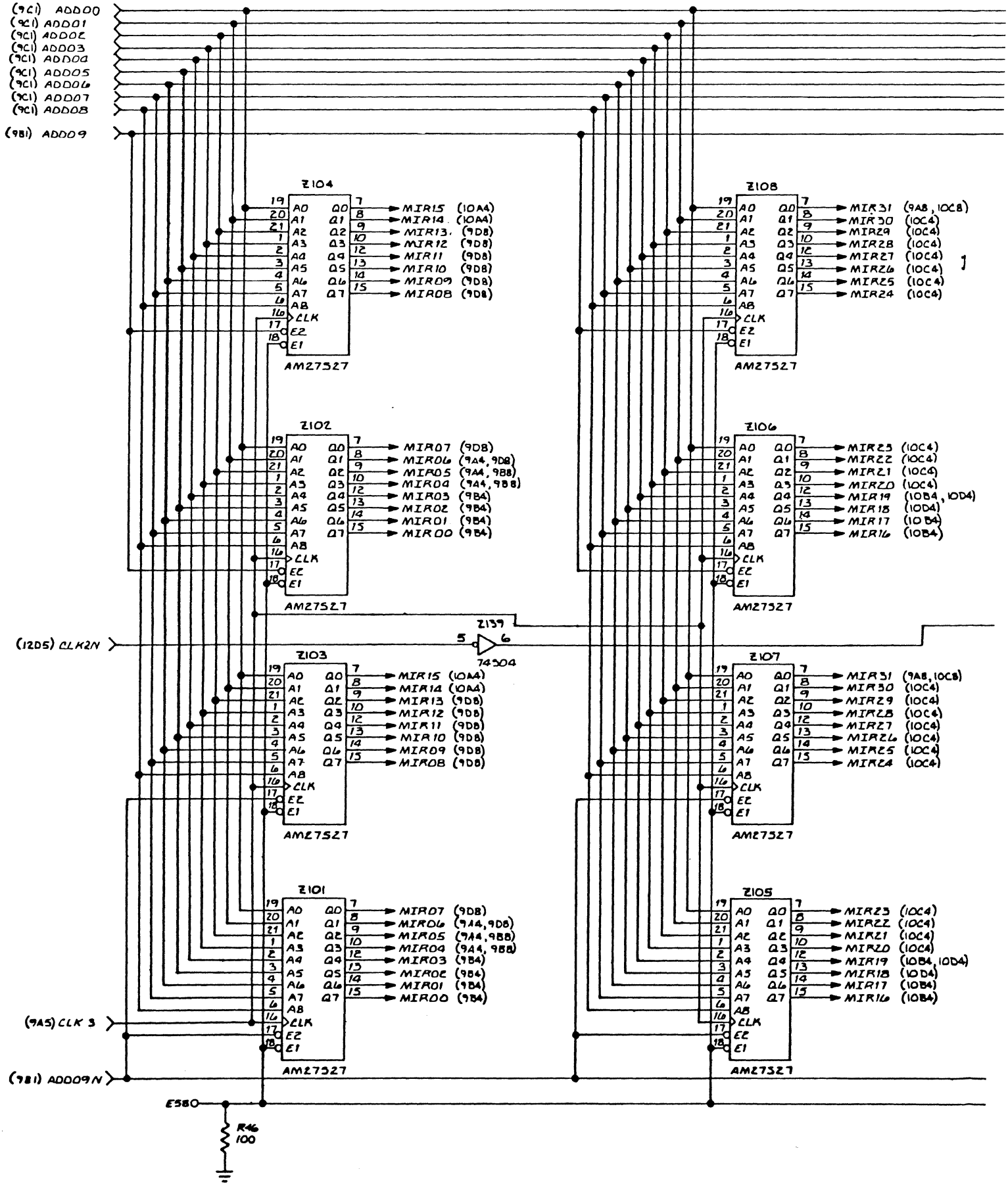
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 11 OF 13


+5V
Y1
OSC
11.111
MHZ
14
8
7
Z45
74S04
Z44
74S08
CLK K2N (7AB, 4D4)
Z48
CLK 1N (2C4, 4A4, 4D4, 6D8, 8C4, 8C8)
CLK 2N (12AB, 12C4, 13B8)
CLK 3N (7B8, 9AB, 9B4, 9D8, 11A4, 12A4)
CLK 4N (2AB, 9A5)
RM2
1K
C12
150pf
R10
4.7K
EC
ER
Q
Z43
74LS123
Z46
74S175
RESETN (2D5, 3A5, 4D8, 7A8, 12B8)
RESET (9B4)
EXT RESETN
E45
Z15
74S00
(6D5) INIT
(7C6) PU5
E57
E46
EXT STOPN
E44
EXT CLK
(7A1) DCLO
DCLON (2D8)
R44
180
Z13
7438
PWRL
R45
180
Y ORDER
B LATCH
Z136
74LS259
(13B1, 13D1) MIR 61
(13B1, 13D1) MIR 60
(13B1, 13D1) MIR 59
(13B1, 13D1) MIR 58
(12C6) RESET N
ADIN (10A4)
LED1
LED2
LED3
LED4
(13B1, 13D1) MIR 57
(12D5) CLK 2N
(13B1, 13D1) MIR 56
Z139
Z140
74S10
ALENAN (2D5)
CLENAN (9A4)

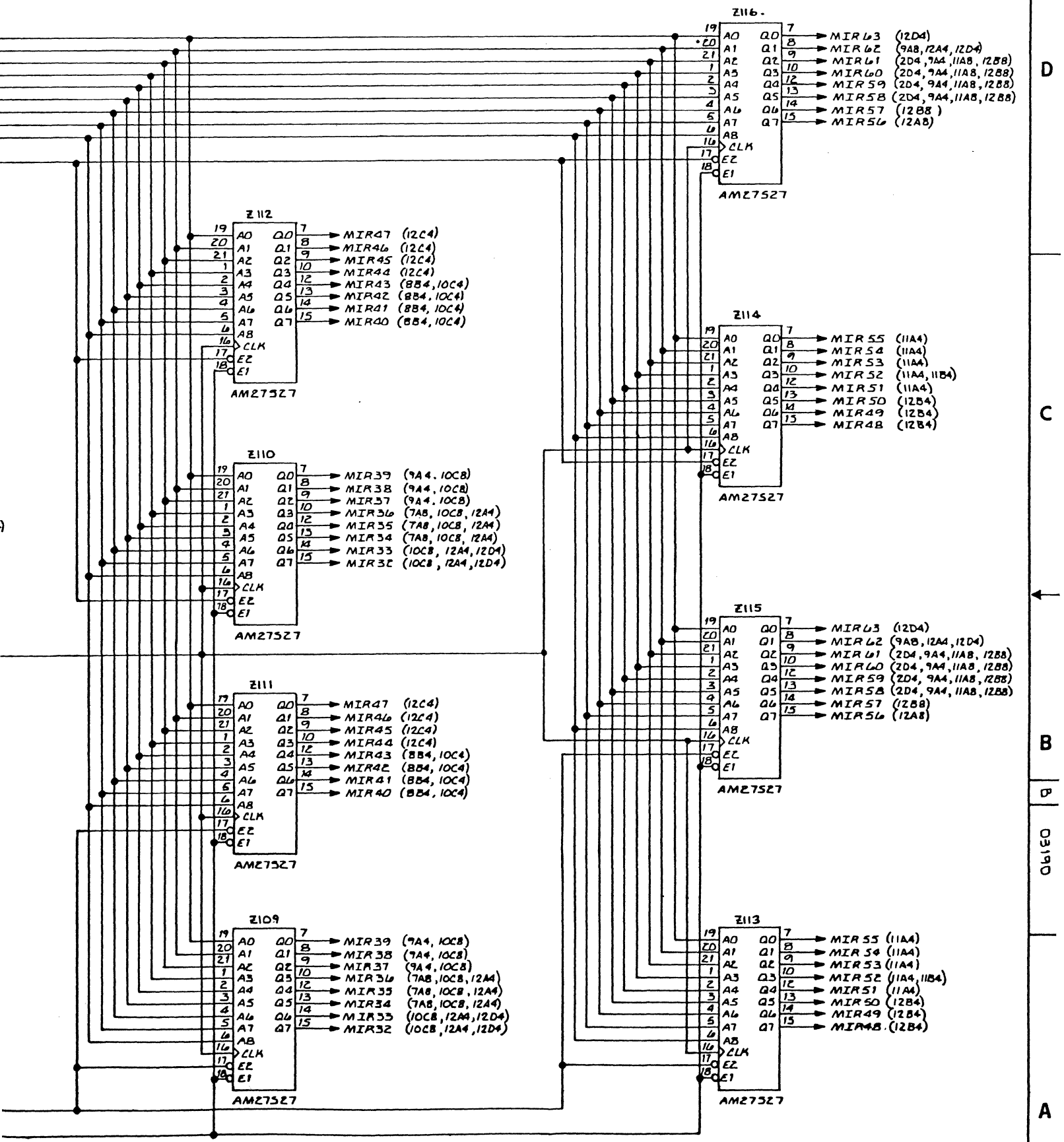


SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	50473	03190	B
SCALE NONE			SHEET 12 OF 13

CONTROL A
MICRO-INSTRUCTIO

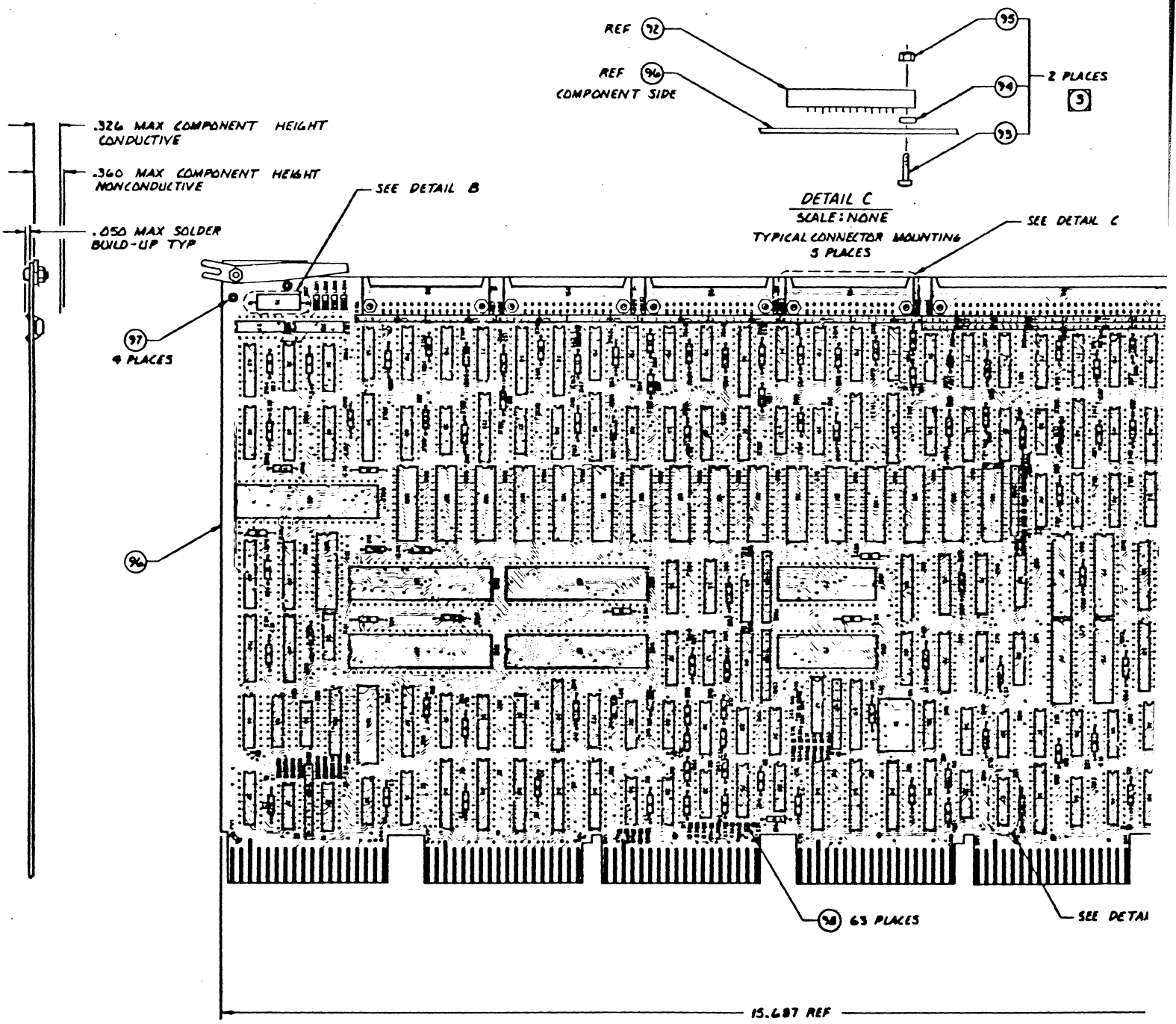


OL ROM
CTION REGISTER

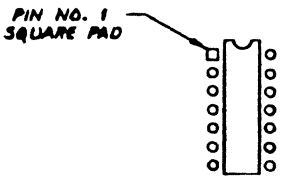


SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03190	B
SCALE NONE			SHEET 13 OF 13

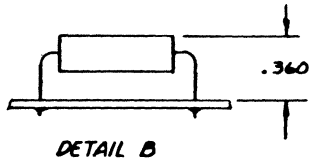
504097 B



DETAIL C
SCALE: NONE
TYPICAL CONNECTOR MOUNTING
5 PLACES

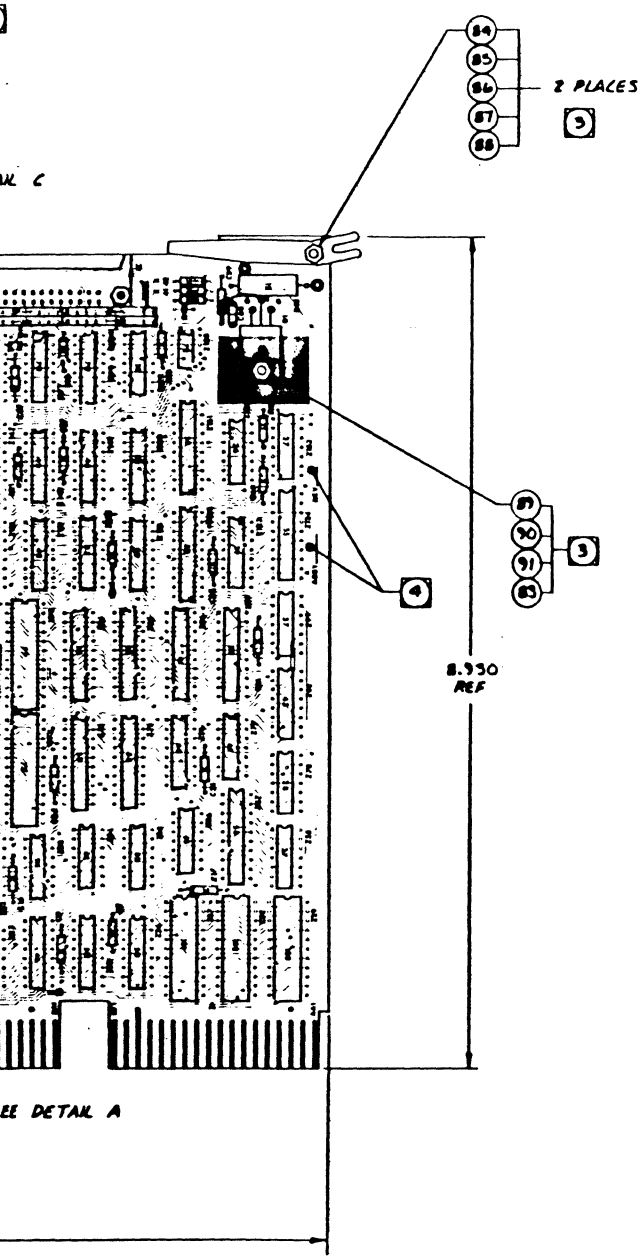


DETAIL A
SCALE 2:1
TYPICAL PIN ORIENTATION
FOR LOGIC IC'S



DETAIL B
SCALE 2:1
TYPICAL MOUNTING HEIGHT
FOR 3 WATT RESISTORS

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	RE-RELEASE	3-27-80	



NOTES: UNLESS OTHERWISE SPECIFIED.

1. FOR SCHEMATIC DIAGRAM SEE DRAWING NO. 03190.
2. COMPONENT DESIGNATIONS ARE FOR REFERENCE PURPOSES ONLY AND DO NOT APPEAR ON COMPONENT PART.
3. INSTALL AFTER FLOW SOLDER.
4. MARK ASSY NO., REVISION LETTER AND SERIAL NO. WITH .12 HIGH CHARACTERS USING BLACK INK PER MIL-M-13231, GROUP III. LOCATION APPROXIMATELY WHERE SHOWN.
5. ALL COMPONENTS TO BE MOUNTED IN ACCORDANCE WITH DATARAM QC SPEC #QC2000

S33 CONFIGURATION CHART

FUNCTION	S33/A REMOVE JUMPER	S33/A ADD JUMPER	S33/B REMOVE JUMPER OR CUT ETCH	S33/B ADD JUMPER
UNIBUS ADDRESS	E5 TO E6	E1 TO E2 (1)	E7 TO E8	E1 TO E2 (1)
		E3 TO E4 (1)	E11 TO E12	E3 TO E4 (1)
		E7 TO E8 (1)	E13 TO E14	E5 TO E6
		E9 TO E10 (1)		E9 TO E10 (1)
		E11 TO E12 (1)		E15 TO E16 (1)
		E13 TO E14 (1)		
		E15 TO E16 (1)		
UNIBUS VECTOR	E32 TO E33	E34 TO E35 (1)	E34 TO E39	E32 TO E33
	E38 TO E39	E36 TO E37 (1)	E40 TO E41	E34 TO E35 (1)
	E40 TO E41			E36 TO E37 (1)
	E42 TO E43			E42 TO E43
CRC/LAC OPTION	E61 TO E59	E60 TO E61 (1)	E60 TO E61	E61 TO E59
DRIVE CONFIG 80MB		E62 TO E63 (1)		E62 TO E63 (1)
DRIVE CONFIG 300MB			E62 TO E63	

(1) CONNECTION EXISTS IN ETCH. JUMPER NOT REQUIRED IF ETCH NOT PREVIOUSLY CUT.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS XX ±.02 XXX ±.010 / ANGLES ± /
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN H D KOGA	3-26-80
CHECKED [signature]	3-27-80
ENG.	
APPROVED	

DATARAM CORPORATION
CRANBURY NEW JERSEY

ASSEMBLY PRINTED WIRING BOARD
S33 SMD CONTROLLER

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	65001/65034	B

SCALE 1/1 SHEET 1 OF 1

500097

REV. B

DWG. NO. 65001 SHEET 1 OF 7

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		RELEASE TO PRODUCTION		1/28/80
B		RE-RELEASE		3/27/80

DRAWN JRK	DATE 1/28/80	TITLE BILL OF MATERIALS S33/A SMD CONTROLLER (RM02)		
CHECKED [signature]	DATE 3.28.80			
ENGR.	DATE	DATARAM CORPORATION CRANBURY NEW JERSEY	DWG. NO. 65001 SHEET 1 OF 7	REV. B
APPROVED	DATE			

PL500097-B

TITLE: S33/A SMD CONTROLLER

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	1	12329	CAP. CER. 0.1 UF. 20%	C60
2	56	12105	CAP. TANT. 4.7 MF 10V	C1-C11,C14-C58
3	1	12517	CAP. SIL MICA. 220 PF. 5%	C13
4	3	12503	CAP. SIL MICA. 150 PF. 5%	C12,C61,C62
5	1	12119	CAP. TANT. 1MF. 20V 150D105X9020A2 SPRAUGE	C59
6	4	18401	DIODE, LED, 555-2003 DIALIGHT	LED1-LED4
7	1	18108	DIODE 1N914	CR1
8	6	10155	RES, CC, 1/4 W, 180 OHM, 5%	R1,R2,R3,R6,R44,R45
9	2	10110	RES, CC, 1/4 W, 390 OHM, 5%	R4,R5
10	1	10111	RES, CC, 1/4 W, 470 OHM, 5%	R26
11	17	10113	RES, CC, 1/4 W, 1.0K OHM, 5%	R7-R9,R12-R23, R31,R47
12	6	10177	RES, CC, 1/4 W, 680 OHM, 5%	R34-R36,R40-R42
13	8	10145	RES, CC, 1/4 W, 22K OHM, 5%	R24,R25,R27-R30,R32,R33
14	1	10616	RES, CC, 1/4 W, 150K OHM, 5%	R11
15	2	10356	RES, 3 W, 7.5 OHM, 1% M-20 TYPE	R37,R43
16	1	10121	RES, CC, 1/4 W, 4.7K OHM, 5%	R10
17	1	10105	RES, CC, 1/4 W, 100 OHM, 5%	R46
18	6	11986	RES MDL, 56 OHM (10/P, 9/EL) 750-101-R56 CTS	RM14-RM17,RM19,RM21
19	8	11987	RES MDL, 82 OHM, (10/P, 9/EL) 750-101-R82 CTS	RM6-RM13
20	5	11988	RES MDL, 1.0K OHM, (10/P, 9/EL) 750-101-RIK CTS	RM1-RM5
21	2	11989	RES MDL, 22K OHM (10/P, 9/EL) 750-101-R22K CTS	RM18,RM20
22				
23				
24				
25				

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65001 B/M
SHEET 2 OF 7

REV. B

TITLE: S337A SMD CONTROLLER

ITEM NO	QTY	PART NUMBER	DESCRIPTION		REFERENCE NOTES
26	6	16513	IC, QUAD 2 I/P NAND 74S00		Z11,Z15,Z32,Z49,Z146,Z182
27	5	16501	IC, HEX INV 74S04		Z21,Z45,Z139,Z153,Z181
28	7	16525	IC, QUAD 2 I/P NAND 74S08		Z20,Z41,Z44,Z48,Z61,Z78,Z143
29	2	16515	IC, TRIPLE 3 I/P NAND 74S10		Z50,Z140
30					
31	1	16542	IC, 8 I/P NAND 74S30		Z51
32	1	16521	IC, QUAD 2 I/P POS-OR GATE 74S32		Z179
33	2	16309	IC, QUAD 2 I/P NAND GATE 7438		Z4,Z13
34	1	16512	IC, DUAL AND NOR 74S51		Z156
35	2	16519	IC, AND -OR-INVERT 74S64		Z130,Z155
36	4	16522	IC, DUAL D BINARY 74S74		Z12,Z23,Z42,Z152
37	5	16505	IC, QUAD EX OR 74S86		Z2,Z3,Z58,Z99,Z132
38	1	16214	IC, DUAL MONOSTABLE MV 74LS123		Z43
39	2	16537	IC,13 INPUT NAND 74S133		Z1,Z123
40	2	16520	IC, 3-TO-8 DCDR/DEMUX 74S138		Z135,Z137
41	2	16510	IC, DUAL DEC/DEMUX 74S139		Z138,Z171
42	1	16364	IC,	74148	Z129
43	6	16245	IC,	74LS161	Z98,Z119,Z120,Z148,Z149,Z154
44	1	16534	IC,	74S163	Z30
45	3	16246	IC,	74LS164	Z54,Z55,Z56
46	3	16524	IC, HEX D-TYPE FF W/CLR	74S174	Z24,Z31,Z118
47	1	16509	IC, QUAD D BIN	74S175	Z46
48	3	16744	IC, 64 BIT RNDM ACS MEM	74S189	Z125,Z126,Z127
49	6	16531	IC,	74S240	Z47,Z60,Z66,Z79,Z80,Z86
50	7		IC,	74S251	Z25,Z26,Z71,Z91,Z121,Z133,Z150
51	4	16538	IC, 4 TO 1 MUX 74S253		Z36,Z37,Z38,Z145

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

TITLE: S33/A SMD CONTROLLER

ITEM NO	QTY	PART NUMBER	DESCRIPTION		REFERENCE NOTES
52	4	16251	IC,	74LS257	Z64,Z65,Z84,Z85
53	3	16264	IC,	74LS259	Z136,Z144,Z157
54	2	16511	IC, DUAL 5 I/P NOR	74S260	Z52,Z53
55	2	16377	IC,	74276	Z22,Z124
56					
57	1	16261	IC,	74LS299	Z141
58	10	16260	IC,	74LS374	Z57,Z74,Z75,Z94,Z95,Z97,Z122
					Z151,Z161,Z162
59	3	16551	IC, OCT D-TYPE FLIP-FLOP	74S374	Z35,Z39,Z128
60	2	16235	IC, 4-B BISTABLE LCH	74LS375	Z68,Z76
61	1	16252	IC, OCTAL D TYPE FF	74LS377	Z96
62	1	16236	IC, DUAL 4-B BC	74LS393	Z77
63					
64	1	16268	IC,	AM25LS2521	Z142
65	3	16269	IC,	AM25LS2538	Z134,Z147,Z167
66					
67	4	16701	IC, MICROPROCESSOR	2901	Z62,Z63,Z82,Z83
68	9	16380	IC,	AM2908	Z6,Z7,Z8,Z9,Z10,Z16,Z17,Z18,Z19
69	1	16918	IC,	AM2910	Z100
70	10	16378	IC,	MC3450	Z158,Z159,Z163-Z166,Z169,Z170
					Z177,Z178
71	6	16379	IC,	MC3453	Z160,Z168,Z173-Z176
72	1	16604	IC, DUAL PERIPH DRIVE	75452	Z180
73	2	16919		82S09	Z67,Z87
74	1	16345	IC, QUAD UNI BUS XCVR	DS8641N	Z5
75	1	16334	IC, HEX UN BUS RCVR	8837/8T37	Z14

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

TITLE: S33/A SMD CONTROLLER

ITEM NO	QTY	PART NUMBER	DESCRIPTION		REFERENCE NOTES
76	1	16381	IC,	9401	Z172
77	4	16915	IC,	9403	Z72,Z73,Z92,Z93
78	4	16916	IC,	S2114A-1PC	Z69,Z70,Z89,Z90
79	1	16554	IC,	74S153	Z117
80	1	16217	IC,	74LS373	Z88
81	1	14112	OSC 11.111 MHZ		Y1
82	1	20314	VOLTAGE REGULATOR	LM320T 5.0	Q1
83	A/R		INSULGREASE - G641 G.E.		
84	2	42650	HANDLE - INSERTOR, EXTRACTOR DR-111		
85	2	26301	SCR, PNH PH, STL, 2-56 X 1/4		
86	2	26107	NUT, HEX, SELF-LOCK, STL, 2-56		
87	2	42651	SPACER, HANDLE MOUNT, DR-111		
88	2	26221	WASHER-BELVILLE SPRING S.P.E.C. B0281-103		
89	1	26322	SCR, PNH PH, STL, 4-40 X 1/4		
90	1	26206	WASHER INT. TOOTH STL #4		
91	1	26102	NUT, HEX, STL, 4-40		
92	4	3493-1002 3M	CONNECTOR 26PIN		
93	1	3372-1002 3M	CONNECTOR 60PIN		
93	10	26311	SCR, PNH PH, STL, 2-56 X 7/16		
94	10	2315-N089 AMATON	SPCR, RND NYL,		
95	10	26101	NUT, HEX, STL, 2-56		
96	1	40741	PC BOARD S33 SMD CONTROLLER		
97	4	22214	BEAD PIN		
98	63	22614	WIRE WRAP POST		
99	A/R		WIRE 30 AWG		
100	REF	03190	SCHEMATIC DIAGRAM S33 SMD CONTROLLER		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65001 B/M
SHEET 5 OF 7

REV. B

TITLE: S33/A SMD CONTROLLER

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
101	1	16747	IC, PROM PATTERN SPEC 1 (AM27S27)	Z27
102	1	16748	IC, PROM PATTERN SPEC 2 (AM27S27)	Z28
103	1	16749	IC, PROM PATTERN SPEC 3 (AM27S27)	Z29
104	1	16750	IC, PROM PATTERN SPEC 4 (AM27S27)	Z34
105	1	16751	IC, PROM PATTERN SPEC 5 (AM27S27)	Z81
106	1	16752	IC, PROM PATTERN SPEC 6 (AM27S27)	Z101
107	1	16753	IC, PROM PATTERN SPEC 7 (AM27S27)	Z102
108	1	16754	IC, PROM PATTERN SPEC 8 (AM27S27)	Z103
109	1	16755	IC, PROM PATTERN SPEC 9 (AM27S27)	Z104
110	1	16756	IC, PROM PATTERN SPEC 10 (AM27S27)	Z105
111	1	16757	IC, PROM PATTERN SPEC 11 (AM27S27)	Z106
112	1	16758	IC, PROM PATTERN SPEC 12 (AM27S27)	Z107
113	1	16759	IC, PROM PATTERN SPEC 13 (AM27S27)	Z108
114	1	16760	IC, PROM PATTERN SPEC 14 (AM27S27)	Z109
115	1	16761	IC, PROM PATTERN SPEC 15 (AM27S27)	Z110
116	1	16762	IC, PROM PATTERN SPEC 16 (AM27S27)	Z111
117	1	16763	IC, PROM PATTERN SPEC 17 (AM27S27)	Z112
118	1	16764	IC, PROM PATTERN SPEC 18 (AM27S27)	Z113
119	1	16765	IC, PROM PATTERN SPEC 19 (AM27S27)	Z114
120	1	16766	IC, PROM PATTERN SPEC 20 (AM27S27)	Z115
121	1	16767	IC, PROM PATTERN SPEC 21 (AM27S27)	Z116
122	1	16768	IC, PROM PATTERN SPEC 22 (74S288)	Z40
123	1	16769	IC, PROM PATTERN SPEC 23 (74S472)	Z33
124	1	16819	IC, PROM PATTERN SPEC 24 (74S472)	Z59
125	1	16820	IC, PROM PATTERN SPEC 25 (74S472)	Z131

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
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SHEET 6 OF 7

REV. B

TITLE: S33/A SMD CONTROLLER

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
126	REF	08506	RM02 S33/A EMULATION SET LISTING	Z101 Thru Z116
127	REF	08507	RM02 S33/A DISK SEQUENCER LISTING	Z27, Z28, Z29
128	REF	08508	RM02/RK07 S33/A/B DMA SEQUENCER LISTING	Z33, Z34
129	REF		RM02 S33/A PI/O VECTOR LISTING	Z59
130	REF		RM02/RK07 S33/A/B PI/O SEQUENCER LISTING	Z40

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

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SHEET 7 OF 7

REV. B

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