Harris Series 100 and 200

MANAGEMENT SUMMARY

Harris Corporation's Computer Systems Division (CSD) introduced the Series 100 and 200 families in November 1975. The Series 100 now consists of five systems based on the Slash 4 VMS central processor and three systems based on the Slash 6 central processor that Harris introduced in May 1976. The Series 200 is composed of four systems, all based on the Slash 7, an asynchronous CPU introduced in September 1975. The Series 100 is upward-compatible with the Series 200.

Harris Corporation entered the minicomputer business when it acquired the Datacraft Corporation in January 1974, renaming it the Harris Computer Systems Division in September 1974. The first Datacraft system (a Slash 1) was delivered in the spring of 1969. Less than a year later, Datacraft delivered its second model, the Slash 3. In February 1971, the company announced the Slash 5 as a software-compatible minicomputer version of the medium-scale Slash 1 and Slash 3. The next addition to the Datacraft family was the Slash 4, which has I/O and software compatible with all the other Datacraft models and was announced in August 1973.

In a series of product moves, the earlier Slash 1 and Slash 3 systems were de-emphasized in favor of the lower-priced Slash 4 and Slash 5 models. These moves established the Slash 4 as the more powerful, and more expensive, base system, with the Slash 5 becoming a cost-effective economy version. The newer Slash 7 is the highest-priced and most powerful processor in the current

The Harris Series 100 and 200 systems are packaged systems based on the company's Slash 4, Slash 6, and Slash 7 CPU's. The 24-bit systems feature virtual-memory processing and a COBOL compiler. Prices for the eight-member Series 100 start at $85,000, and the four-member Series 200 at $179,000.

CHARACTERISTICS

MANUFACTURER: Harris Corporation, Computer Systems Division, 1200 Gateway Drive, Fort Lauderdale, Florida 33309. Telephone (305) 974-1700.

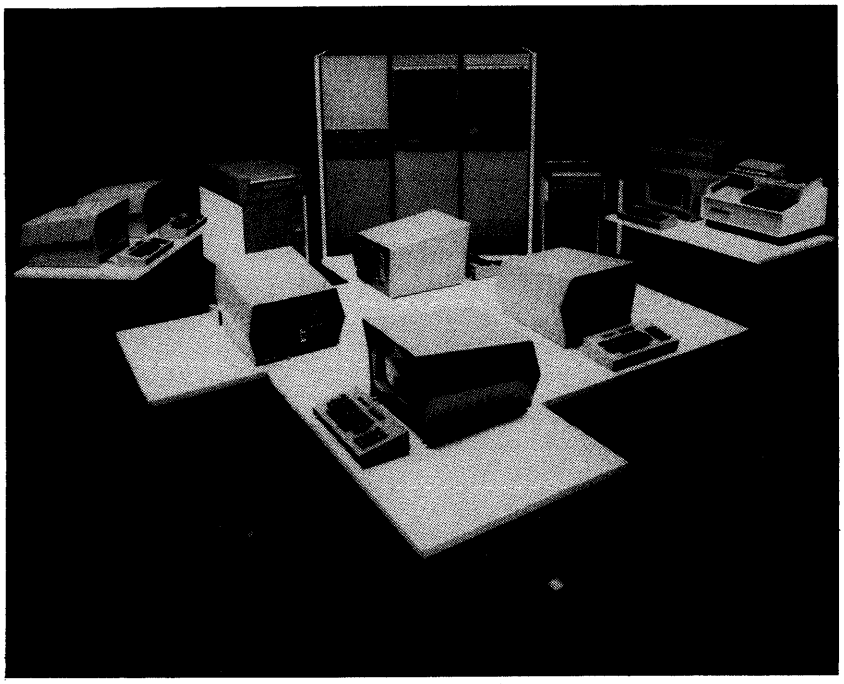
Founded in 1895 as a manufacturer of automatic printing presses, Harris Corporation is now a high-technology company supplying a board range of equipment and services for communications and information handling. The Computer Systems Division came into being in 1974, after Harris acquired the Datacraft Corporation, a minicomputer manufacturer.

MODELS: Series 100 Models 110, 120, 130, 140, and 150, which are based on the Slash 4 VMS; Series 100 Models 115, 125, and 135, which are based on the Slash 6 VMS; and Series 200 Models 210, 220, 230, and 240, which are based on the Slash 7 VMS.

DATA FORMATS

BASIC UNIT: 24-bit word.

FIXED-POINT OPERANDS: 24-bit words and 48-bit



This typical Harris System 125 configuration includes a Slash 6 CPU with 96K words of memory, six interactive CRT terminals and an operator's console, one 300-megabyte disc unit, one 40-megabyte disk unit, two magnetic tape units, a 600-lpm line printer, and a 600-cpm card reader. Prices for the basic Series 100 systems range from $85,000 to $290,000.

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Slash line. Although the Slash 4 in a virtual-memory model was marketed in non-packaged systems for a short time, that model was withdrawn when the Series 100 and 200 were announced.

As indicated before, the Series 100 and 200 systems are based on the Harris Slash 4, Slash 6, and Slash 7 processors (see Report M11-468-101). The enhancements made to these processors include virtual-memory hardware, a second parity bit in the Slash 4, all internal options (such as address trap) as standard features, and an increased number of external interrupts. On the software side, there is no choice of operating systems; VULCAN is the only operating system available for the Series 100 and 200, and it is not offered for the earlier Slash Series systems. Also, a new COBOL compiler is available for the Series 100 and 200 only.

The only way you may purchase a Series 100 or 200 system is through packaged configurations which come with a set of peripheral expansion restrictions and penalties. For full expansion capabilities and maximum flexibility, component-by-component build-up of a Slash 4, Slash 6, or Slash 7 system is required.

During its first seven years of minicomputer development, Datacraft encountered severe financial difficulties. Its acquisition by Harris Corporation has provided the necessary financial and marketing resources needed to move its products more aggressively. With its new backing, Datacraft received an active outlet for supplying computer systems to meet the needs of its senior partner, which is deeply involved in computerized communications and information systems.

At the low end of the Series 100 line, the Harris System 110, including a CPU with 32K words of core memory, 10.8-megabyte cartridge disc, 20-KBS magnetic tape unit, console CRT/keyboard, and DMA communications multiplexer, sells for $85,000.

The System 150, at the high end of the Series 100 line, includes a CPU with 160K words of core memory, three disc drives with a combined storage capacity of 640 megabytes, 20-KBS magnetic tape unit, console CRT/keyboard, 1000-cpm card reader, 900-lpm printer, and DMA communications multiplexer. The purchase price of this system is $290,000.

At the low end of the Series 200 line, the System 210 consists of a CPU with 64K words of memory (which is expandable to 256K words in 32K-word increments), 40-megabyte disc storage module, 20-KBS magnetic tape unit, console/keyboard, DMA communications multiplexer, Scientific Arithmetic Unit (SAU), 300-cpm card reader, and 300-lpm line printer. Its purchase price is $179,000.

The largest member of the Series 200 line is the System 240, priced at $436,000. This system includes a CPU with 192K words of memory (expandable to 256K words),

double words. Data is represented in two's-complement binary notation.

FLOATING-POINT OPERANDS: Hardware floating-point is standard on the Series 200, and optional on the Series 100 (except the Model 115) through the Scientific Arithmetic Unit (SAU). The SAU contains hardware for operating on double-precision numbers which have a 39-bit mantissa, an 8-bit exponent, and a sign bit. Sign, zero, or overflow status is determined after each operation.

INSTRUCTIONS: All instructions are one word in length. In the monitor mode, direct addressing to 32K words is provided in the majority of memory reference instructions, with additional instructions, such as Branch, that directly address up to 65K words. Formats of the instructions are complex, but in general they use a 6- or 12-bit op code and permit indirect addressing and/or indexing. Register-to-register instructions are included.

INTERNAL CODE: ASCII.

MAIN STORAGE

TYPE: Magnetic core or MOS memory for the Series 100; multiport magnetic core memory for the Series 200. Multiport semiconductor memory is optionally available for the Series 200.

CYCLE TIME: 750 or 450 nanoseconds for Series 100 models; 675 nanoseconds for Series 200 core memory, and 200 nanoseconds for semiconductor memory.

CAPACITY: The following table shows the minimum and maximum memory capacities of the various Harris Series 100 and Series 200 systems. Expansion in the Series 100 models may be in 8K- or 16K-word increments. The memory of the Series 200 processors is expandable in 32K-word increments. The optional Series 200 multiport semiconductor memory is expandable to 32K words in 8K-word increments.

Model Number	Basic System (words)	Max. Capacity (words)
110	32K	64K
115	48K	64K
120	64K	256K
125	48K	208K
130	96K	256K
135	128K	256K
140	128K	256K
150	160K	256K
210	64K	256K
220	96K	256K
230	160K	256K
240	192K	256K

The memory in the Series 200 processors is modulo-2 interleaved. Two segments exist, one odd and the other even, in separate chassis. When expansion occurs, the 32K-word increment is divided into two 16K-word modules, one added to each chassis. Memory interleaving gives the appearance of reduced memory access time.

CHECKING: A parity bit is associated with each 12 bits (one halfword) of core memory. MOS memory uses a 5-bit error correction code per word.

STORAGE PROTECTION: Memory limits are set by the virtual-memory hardware as described under Central Processors.

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION AND SPEED	MANUFACTURER
MAGNETIC TAPE		
6210, 6211	Seven-track, 556/800 bpi, 100 ips, 55.6/80 KC/sec, vacuum column	CDC 92103
6220, 6221	Seven-track, 556/800 bpi, 150 ips, 83.4/120 KC/sec, vacuum column	CDC 92153
6230, 6231	Seven-track, 556/800 bpi, 200 ips, 111.2/160 KC/sec, vacuum column	CDC 92203
6240, 6241	Nine-track, 800/1600 bpi, 100 ips, 80/160 KB/sec, vacuum column	CDC 92101
6250, 6251	Nine-track, 800/1600 bpi, 150 ips, 120/240 KB/sec, vacuum column	CDC 92151
6260, 6261	Nine-track, 800/1600 bpi, 200 ips, 160/320 KB/sec, vacuum column	CDC 92201
6630, 6631	Seven-track, 556/800 bpi, 45 ips, 25/36 KC/sec, tension arm	Wangco
6640, 6641	Nine-track, 800 bpi, 45 ips, 36 KB/sec, tension arm	Wangco
6650, 6651	Nine-track, 800/1600 bpi (PE), 45 ips, 36/22 KB/sec, tension arm	Wangco
6660, 6661	Nine-track, 800/1600 bpi, 45 ips, 36/72 KB/sec, vacuum column	Wangco
6680, 6681	Seven-track, 556/800 bpi, 75 ips, 41.7/60 KB/sec, vacuum column	Wangco
6690, 6691	Nine-track, 800/1600 bpi, 75 ips, 66/120 KB/sec, vacuum column	Wangco
LINE PRINTERS		
4110	300 lpm, drum type, 64-char. set, 136 positions	Dataproducts
4115	240 lpm, drum type, 96-char. set, 136 positions	Dataproducts
4120	600 lpm, drum type, 64-char. set, 136 positions	Dataproducts
4125	436 lpm, drum type, 96-char. set, 136 positions	Dataproducts
4130	900 lpm, drum type, 64-char. set, 136 positions	Dataproducts
4135	660 lpm, drum type, 96-char. set, 136 positions	Dataproducts
4710	500 lpm, 1.2 ips plot, 11-inch plot/123-col. print, 1024 nibs, 96-char. set	Versatec
4720	1000 lpm, 2.3 ips plot, 11-inch plot/123-col. print, 1024 nibs, 96-char. set	Versatec
4730	300 lpm, 75 ips plot, 20-inch plot/232-col. print, 96-char. set	Versatec
4740	1200 lpm, 3 ips plot, 20-inch plot/232-col. print, 96-char. set	Versatec
4750	1000 lpm, 1 ips plot, 11-inch plot/132-col. print, 96-char. set	Versatec
CARD EQUIPMENT		
3010	300 cpm reader, 1000 card I/O stackers, 80-column	Documation MXXXL
3020	600 cpm reader, 1000 card I/O stackers, 80-column	Documation MXXXL
3030	1000 cpm reader, 1000 card I/O stacker, 80-column	Documation MXXXL
3110	300 cpm reader, 550 card I/O stackers, 80-column	Documation MXXXL
3120	600 cpm reader, 1000 card I/O stacker, 80-column	Documation MXXXL
3130	1000 cpm reader, 1000 card I/O stacker, 80-column	Documation MXXXL
PAPER TAPE EQUIPMENT		
2030/2035	300 cps reader/75 cps punch (2035 is for fanfold tape)	Remex
2040	300 cps reader/spooler	Remex
2050	2040 with 7.25-inch reel	Remex
2060	75 cps punch/spooler	Remex
2095	Paper tape spooler	Remex
TELETYPEWRITERS		
2110, 2130	Modified ASR-33; 8530 is remote terminal; 10 cps	Teletype
2140	Modified KSR-33; 8540 is remote terminal; 10 cps	Teletype
2150	Modified ASR-35; 8550 is remote terminal; 10 cps	Teletype
2160	Modified ASR-35; 8560 is remote terminal; 10 cps	Teletype
CONSOLE DEVICES		
2210	ASR-733 TTY; 8710 is remote terminal	TI
2220	KSR-733 TTY; 8720 is remote terminal	TI
2310	Interactive CRT 24 lines x 80 char., 9600 bps; 2315 has hard-copy device; 8610 is a remote terminal; 8615 is a remote terminal with hard-copy device; 8630 has RS-232 interface; 8635 has RS-232 interface and hard-copy device	Tec
2320	733 replacement CRT, 24 lines x 80 char., 9600 bps; 2325 has hard-copy device; 8620 is a remote terminal; 8625 is a remote terminal with hard-copy device; 8640 with RS-232 interface; 8645 with RS-232 interface and hard-copy device	Tec
2350	Teletype replacement CRT; 24 x 80 with keyboard	Infoton

two 80-megabyte disc units, two 9-track 800/1600-bpi tape units at 150 ips, two DMA multiplexers, 600-lpm line printer, 1000-cpm card reader, system console CRT/keyboard, and Scientific Arithmetic Unit (SAU).

CENTRAL PROCESSORS

GENERAL: Series 100 models utilize the Harris Slash 4 or Slash 6 processor with virtual-memory hardware additions. Series 200 models utilize the Harris Slash 7 processor, also with virtual-memory hardware additions. The following

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Most of the Harris systems software is bundled. It includes the VULCAN core manager (virtual-memory operating system); an extended ANS FORTRAN IV compiler; an interactive extended BASIC interpreter; COBOL, RPG II, and SNOBOL 4 compilers; a FORGO (diagnostic FORTRAN) compiler; a macro assembler; a sort/merge; an indexed sequential file handler; an interactive text editor; and cross-reference, debug, and trace aids. An RJE (remote job entry) discipline to emulate an IBM 2780 or HASP II terminal with a System/360 or 370, a Control Data 200 User Terminal with the CDC 6000/7000 Series, or a Univac 1004 with the Univac 1100 Series is available at extra cost.

USER REACTION

Six users of Harris Corporation's computers responded to Datapro's 1977 survey of minicomputer users (see Report M07-100-401). Four of these users had either Slash Series systems or the Series 100 and Series 200 packaged versions installed. Datapro contacted Harris to obtain the names of additional users and was informed that it is against company policy to release this information.

The four survey respondents had a total of five systems installed, including one Slash 4-based Model 120, one Slash 7-based Model 220, two Slash 5 systems, and one Slash 7 system. Three of the users had purchased their systems outright, while one had been obtained through a lease-purchase arrangement. The earliest date of installation was May 1972, and the latest was December 1976. Memory sizes varied from 32K to 160K words, with an average of about 70K words.

Three of the users were doing all of their own programming, while the fourth had also purchased some proprietary software packages and had Harris develop some software to supplement what he was doing on his own. Programming languages used included COBOL, FORTRAN, BASIC, SNOBOL, JOVIAL, and Assembly. These users had an average of about 93 million bytes of disc storage on-line, and the number of interactive terminals connected on-line ranged from 2 to 27. Principal applications included scientific/engineering computing, data communications, program development, and education.

The table below summarizes the ratings of the four users. Since Harris does not offer application programs, this category has been omitted.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	1	2	1	0	3.0
Reliability of mainframe	2	1	0	1	3.0
Reliability of peripherals	2	1	0	1	3.0
Responsiveness of maintenance service	2	1	1	0	3.2
Effectiveness of maintenance service	2	1	0	1	3.0
Technical support	1	2	0	1	2.8
Operating systems	0	3	0	1	2.5
Compilers and assemblers	0	3	1	0	2.8
Ease of programming	0	2	2	0	2.5
Ease of conversion	0	3	0	0	3.0
Overall satisfaction	0	3	0	1	2.5

*Weighted Average on a scale of 4.0 for Excellent.

paragraphs describe the virtual-memory hardware additions. See the previous report, M11-468-101, for a detailed description of the Slash 4, Slash 6, and Slash 7 processors, including instruction execution times.

In the user mode, which is active in virtual-memory operation, an individual program can use up to 256K words, of which 64K words can be instruction space and the remaining 192K words data space for that program. Since the largest configuration offered can contain a maximum real memory of 256K words, a virtual-to-read storage ratio of 4 to 1 can be achieved, which is respectable. In the largest system announced, up to 16 users, each with a 256K-word program (instructions plus data), can be mapped into a 256K-word physical address space via 4096 1K-word virtual address pages. Virtual addressing is by means of a demand paging scheme with a least-recently-used (LRU) page-swapping algorithm.

Each Model 110, 120, 125, 130, 140, and 150 system contains 1024 virtual address register (VAR's) that are implemented in solid-state logic. The Model 115 system has 256 VAR's, while the Model 135 had 4096. A VAR has 10 bits, 8 for the page pointer address and 2 for indicating 3 states of memory protection or a page fault (page not in physical memory). Also, there are two 1-bit registers associated with each physical page to indicate usage of the page and whether the page has been modified (written to); a page is overwritten instead of being swapped out to save time if it hasn't been written to.

Mapping is through the 18-bit addresses generated in the demand page register. The scheme for generating these addresses begins with the addition to the virtual base register (VBR) of the most significant bits of the effective memory address. These will be five, six or eight bits in number dependent on the type of instruction. The resultant sum in the VBR selects one of the VAR's. Bits 0 through 7 of the VAR are then appended to the left of the 10 least significant bits of the effective memory address to form the address which is then transferred to the virtual demand page register. The program in current use abides by the range of address space between the contents of the single virtual-base register and virtual-limit register (VLR). VAR use is kept contiguous by automatic selection of contiguous VAR's as a program is loaded and by compression of VAR's in use as fragmentation naturally occurs. The virtual mapping process takes place without adding overhead to the memory cycle time.

Access to respective pages in monitored by the 256 one-bit virtual page registers (VNR's), which indicate whether a page has been written to since it was transferred to memory. The pointers to the VNR's that allow them to be tested are the 256 virtual usage base registers (VUR's). Two 10-bit registers are used for the storing and retrieval of data from the VAR's; they are the virtual source register (VSR) and the virtual destination register (VDR). Lastly, there is the 12-bit virtual demand page register, in which bits 0 to 9 contain the relative address of the VAR, which in turn contains the missing page that created a demand page or the address of the VAR that resulted in a limit violation.

INPUT/OUTPUT CONTROL

The same variety of I/O channels is provided for the Series 100 and Series 200 models as for the Harris Slash 4, Slash 6, and Slash 7 processors as described in the previous report, M11-468-101, subject to the limits imposed on the Series 100 and 200 packaged configurations. The configurations of the Series 100 and 200 models are shown in the Equipment Pricing section at the end of this report.

MASS STORAGE

See report M11-468-101 for a description of the available mass storage devices.

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In summary, the system hardware and Harris' maintenance service received the most favorable ratings, while programming and software aspects drew the least favorable user reactions. It should be noted that one user rated his system as poor in 6 of the 11 categories, fair in 4 categories, and good in only one, thereby accounting for all of the poor ratings and all except one of the fair ratings given to the Harris systems in this survey. Interestingly enough, this user had converted from a large system from a major mainframe vendor and cited as a principal strength of the Harris system its similarity to his previous system. As a disadvantage, he noted "poor software (OS) and hardware reliability." Positive comments from the other three users included "solid operating system" and "good I/O structure." On the negative side, these users cited "poor documentation" and "lack of extensive user libraries of programs."□

INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

SOFTWARE

The basic software package supplied as standard with each system depends on the particular system configuration chosen. The one operating system available is VULCAN.

Also supplied are a FORTRAN IV Compiler, Interactive BASIC Compiler, SNOBOL 4, RPG II, Harris MACRO Assembler, COBOL, Diagnostic FORTRAN Compiler (FORGO), Sort/Merge, Indexed Sequential File Handler, Interactive Text Editor (ACRONIM), Utility Package, Cross-Reference, DEBUG, Trace, Link Loader; and a complete set of diagnostics for the mainframe, memory, and peripherals.

OPERATING SYSTEM: The *Virtual Core Manager(VULCAN)* occupies 10,000 to 32,000 words. System size depends on several factors, including the number of concurrently active user programs, system table sizes, and the number of nonresident handlers loaded at a given time. According to Harris, the system will generally occupy less than 20,000 words of core. Absolute minimum VULCAN configurations require 32K words of core for real-time applications, and if interactive or batch environments are required, minimum memory sizes of 49K to 65K words will be needed.

VULCAN's features included disc file security on a multi-level basis, re-entrant processors and libraries which minimize the additional memory required by multiple users, re-entrant code generation (which implies separation of program space into code and data sections), spooling of input and output of either the data or jobstream type for local or remote terminals, interprogram communications either by message or parameter, integral systems accounting, and a Remote Job Entry (RJE) subsystem for emulation of several different terminal types.

The Remote Job Entry subsystem provides the capability for communication with certain host computers concurrently with other processing. All standard terminal features are supported for the communication with the following systems: as a Univac 1004 with the Univac 1100 Series computers; as a CDC 200 User Terminal with the CDC 6000/7000 Series; as an IBM 2780 with the IBM 360/370 series; and as an IBM HASP II workstation with the IBM 360/370 series. Any interactive terminal, either CRT or teletypewriter, may serve the RJE subsystem. Message transmission and reception use the host system's protocol.

LANGUAGES: Seven languages are currently being offered for use on the Series 100 and 200.

FORTRAN IV is based on but exceeds ANSI X3.9-1966. Harris-supported extensions include random-access I/O; indexed sequential file operations; memory-to-memory data conversion through encode/decode statements; double-buffered and overlapped I/O capabilities through asynchronous I/O statements, which include processing of variable-length and arbitrary-format records in both input and output; free-format I/O, allowing for basic I/O without using FORMAT statements; control functions for end-of-file and I/O or FORMAT errors in all I/O statements; a DATA statement extension for arrays; octal and literal constants; recursive subprograms; in-line assembly code for statements and variables or constants; implied DO loops in DATA statements; program-controlled loading of program overlay segments which have been separately compiled; pseudo-random number generations; services in real-time digital and analog I/O functions; and bit manipulation functions. A diagnostic FORTRAN compiler (FORGO) serves as a companion to Harris extended FORTRAN IV.

Interactive BASIC contains 54 statements and language enhancements for string manipulation, extended Boolean operators and IF statements, logical I/O and picture format facilities, and editing for input. Built-in real-time capabilities allow for use of external interrupts, initiation of programs, parameter passing from other programs regardless of language, and operator communications. Interactive use is enhanced because of the re-entrant code generated by the Basic compiler which itself is re-entrant.

RPG II as implemented by Harris allows for interchange of files between itself and FORTRAN IV or assembly-language programs, as well as creation of these files by programs coded in any of the three languages. Harris RPG II language extensions include array and table equivalencing, main program execution initiation, array element manipulation, source library use, and one- to six-byte binary numeric fields.

The *MACRO Assembler* is a two-pass system that supports over 700 mnemonic operation codes and a range of pseudo-operations which can, among other things, create 11 different constant types. The assembler features nested an recursive macro capabilities.

Also available is the character-string-oriented language, *SNOBOL,* which provides a means to manipulate strings of data by rule development. The language is free-format in character.

COBOL conforms to ANSI X3.23-1974. As with FORTRAN, the COBOL compiler generates re-entrant code. It features 44 verbs and modifications, 49 levels of qualification, arbitrary deeply nested conditional statements, 32-digit accuracy in intermediate calculations, facilities for using CORRESPONDING, and standard debugging tools.

TOTAL is a host-language data base management system implemented much along the same lines of the CODASYL Data Base Task Group Report, except that the user can use other host languages as well as COBOL. TOTAL provides an effective means for organizing and managing diverse data to make it both efficient and convenient for application programmers to maintain and retrieve the data for processing. It was developed by Cincom Systems, Inc. and is widely used with large computer systems. It has been well received and highly rated by users.

TOTAL can manage virtually an unlimited number of data sets on an "integrated, non-redundant" basis and provides for association of each of these data sets with other data sets to form an integrated data base. TOTAL allows the user to

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relate data across many functional and/or departmental boundaries, permitting the data processing applications to mirror the system of management within an organization.

TOTAL permits the establishment of two types of records: a single-entry or master record and a variable-entry record. Each group of records, of either type, forms a file (data set). Linkages can be set up that permit automatic retrieval of all variable-entry records associated with a particualr single-entry record based on the linkage. A variable-entry record can be part of many linkage paths or chains.

A TOTAL data base is composed of mulitple data sets or files. Linkages can exist between any master file and any variable-entry file. Multiple file data bases can be established. A particular master file or variable-entry file can be part of more than one data base. The multiple paths of access allowed by such a structure, called a network structure, simplify the logic of application programs using the data. In the case of TOTAL, they also reduce the amount of disc storage required to hold information by eliminating duplicate fields or records.

To one familiar with sequential and hierarchical sequential files, the benefits of a network structure are not immediately evident. It seems at first glance that the power of a network structure is limited because only one sublevel of linking is possible; i.e., master to variable-entry. The real power of this structure lies in the fact that multiple master files can be established, each for a particular relationship, and any number of variable files can be related to any number of these master files. Each variable file can handle up to 2500 different record types.

A randomizing algorithm is used by TOTAL to calculate master record physical addresses based on the value of the control field. If duplicate addresses are calculated, a pointer is used in that record to show where the "duplicate" or synonym record is stored. Thus, the complete disc space allocated can be used. Once all space is used up, the data file must be reloaded with new parameters. Cincom provides a utility to handle such occurrences.

Access to TOTAL files is provided through the Call statement for application programs written in COBOL, FORTRAN, or assembly language. The applications programmer cannot establish new data sets or alter existing linkages among data items; this function is accomplished separately through a generator program using a special data base definition language.

The TOTAL interactive QUERY language allows non-programmers to extract information that is stored in the TOTAL data base by means of a simple, English-like, non-procedural information retrieval language.

UTILITIES: Other software includes an indexed sequential disc access method callable by FORTRAN IV or assembly-language programs; a sort/merge package callable by FORTRAN IV, RPG II, or assmbly language; and a macro cross-assembler written in FORTRAN IV.

APPLICATIONS: Harris does not supply application packages.

PRICING

POLICY: Harris offers its systems primarily for purchase, although third-party leasing (one-year term) is available on a negotiated basis. Software costs are bundled in the system prices, except for the remote batch terminal emulation software, which is priced at $5,000; TOTAL Basic, priced at $10,000; TOTAL Control, priced at $12,000; and QUERY priced at $10,000.

Deletions from standard hardware configurations are not allowed; substitutions for standard hardware are permitted with a penalty of 20 percent of the deleted item's list price. The items to be substituted will be charged at full list price.

Supplementary hardware in addition to or in lieu of standard options is available subject to home office approval.

Special considerations apply for volume purchases of virtual-memory systems. When a new purchase of an S100/S200 system is made by an OEM or volume-purchase end user, no OEM, CPU, peripheral, or business volume discounts will apply to standard-configuration S100/S200 systems. Any additions or upgrades to a system, however, will be eligible for appropriate CPU/peripheral discounts. Downgrade substitutions are permitted with a penalty of 20 percent of the deleted item's list price; the items to be substituted will be charged at full list price. CPU's purchased in S100/S200 systems will count toward CPU and peripheral totals for other OEM purchases, and the final "dollar total" on the systems will apply to total business volume for other purchases.

SUPPORT: Maintenance is performed by service personnel working out of Harris CSD service offices in the U.S. Maintenance contracts are developed on the basis of local or remote service areas. A local service area is defined as the area within a 50-mile radius of a Harris CSD service office. All other areas are considered remote. For non-contract maintenance, prime-time hourly rates are $45 and $50 per man-hour; minimum billing for these customers is four hours for local service and eight hours for remote service. Remote service area customers, whether on contract or not, are billable at actual cost for tourist-class air travel or at $0.20 mile for automobile usage, and for meals and lodging.

Under contract, maintenance is available for 9 prime-shift hours from 7 am to 6 pm Monday through Friday. Additional maintenance hours are available by negotiation with Harris at prime monthly rates plus an extra charge.

Installation charges are made, but are negotiable depending on the size and quantity of systems sold. Programming and maintenance training are separately priced and are available either at the installation site or at Harris' Fort Lauderdale facility. Training courses are offered in maintenance for the processors, Scientific Arithmetic Unit, and peripherals. A software course on VULCAN is currently being offered.■

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PACKAGED SYSTEMS AND OPTIONS			
System 110	Series 100 CPU (Model 4) with 32K words (96K bytes) of memory, 10.8-megabyte cartridge disc, 9-track 800-bpi tape unit, communications multiplexer, system console CRT, and software package; expandable to 256K words (768K bytes)	$ 85,000	$ 730
System 115	Series 100 CPU (Model 6-5) with 48K words (144K bytes of MOS memory, 10.8-megabyte cartridge disc, 9-track 800-bpi tape unit, communications multiplexer, system console CRT, and software package; expandable to 64K words (192K bytes)	85,000	640
System 120	Series 100 CPU (Model 4) with 64K words (192K bytes) of memory, 10.8-megabyte cartridge disc, 9-track 800-bpi magnetic tape unit, communications multiplexer, 300-lpm printer, 300-cpm card reader, system console CRT, and software package; expandable to 256K words	125,000	1,065
System 125	Series 100 CPU (Model 6) with 48K words (144K bytes) of memory, 10.8-megabyte cartridge disc, 9-track 800 bpi tape unit, DMA communications processor with four asynchronous ports or one synchronous port, system console CRT, and software package; expandable to 208K words (624K bytes)	100,000	750
System 130	Series 100 CPU (Model 4) with 96K words (288K bytes) of memory, 40-megabyte disc storage module, 9-track 800-bpi tape unit, DMA communications multiplexer, 300-lpm printer, 300-cpm card reader, console CRT, and software package; expandable to 256K words (768K bytes)	155,000	
System 135	Series 100 CPU (Model 6-7) with 128K words (384K bytes) of memory, 40-megabyte disc storge module, 9-track 800-bpi tape unit, DMA communications processor, system console CRT, and software package; expandable to 256K words (768K bytes)	150,000	1,125
System 140	Series 100 CPU (Model 4) with 128K words (384K bytes) of memory, 40-megabyte disc storage module, 300-megabyte storage module disc drive, 9-track 800-bpi tape unit, DMA communications multiplexer, 600-cpm card reader, system console CRT, 600-lpm printer, and software package; expandable to 256K words (768 bytes)	225,000	2,030
System 150	Series 100 CPU (Model 4) with 160K words (480K bytes) of memory, two 300-megabyte storage module disc drives, 40-megabyte disc storage module, 9-track 800-bpi tape unit, DMA communications multiplexer, system console CRT, 1000-cpm card reader, 900-lpm printer, and software package; expandable to 256K words (768K bytes)	290,000	2,720
System 210	Series 200 CPU with 64K words (192K words) of interleaved core memory, 40-megabyte disc storage module, 9-track 800-bpi tape drive, DMA communications multiplexer, 300-lpm printer, 300-cpm card reader, system console CRT, scientific arithmetic unit, and software package; expandable to 256K words (768K bytes)	179,000	1,170
System 220	Series 200 CPU with 96K words (288K bytes) of interleaved core memory, two 40-megabyte disc storage modules, 9-track 800-bpi tape drive, DMA communications multiplexer, 600-lpm printer, 600-cpm card reader, system console CRT, scientific arithmetic unit, and software package; expandable to 256K words (768K bytes)	242,000	1,910
System 230	Series 200 CPU with 160K words (480K bytes) of interleaved core memory, 40-megabyte disc storage module, 80-megabyte disc storage module, two 9-track 800-bpi tape units (75 ips), DMA communications multiplexer, 600-lpm printer, 1000-cpm card reader, system console CRT, scientific arithmetic unit, and software package; expandable to 256K words (768K bytes)	339,000	2,445
System 240	Series 200 CPU with 192K words (576K bytes) of interleaved core memory, two 80-megabyte disc storage modules with controller, two 9-track 800-bpi tape units (150 ips) with controller, two DMA communications multiplexers, 600-lpm printer, 1000-cpm card reader, system console CRT, scientific arithmetic unit, and software package; expandable to 256K words (768K bytes)	436,000	3,045
Series 100 options:			
401	8K-word, 24K-byte memory increment	7,000	40
402	16K-word, 48K-byte memory increment	12,200	75
415	Scientific Arithmetic Unit	10,500	70
System 115/125/135 options:			
608	16K-word, 48K-byte MOS memory with error correction	5,500	35
615	Scientific Arithmetic Unit (not available with S115)	6,700	40
Series 200 options:			
703	32K-word memory increment	30,000	150
710	First 8K-word, 200-nanosecond semiconductor memory increment	26,750	160
711	Additional 8K-word, 24K-byte semiconductor memory increment (limit 3)	22,500	135
755	I/O processor (IOP) for multiport semiconductor memory (4 maximum); requires 784	3,500	20
784	I/O processor ports, multiport semiconductor memory	3,000	20
785	CPU port, multiport semiconductor	3,270	20

For prices of peripherals, consultation, and special software, see Report M11-468-101. Note that 5400 series, 4700 series, and 2000 series peripherals are supplementary and not standard options. Configurations including supplementary peripherals are subject to Harris approval.