Hewlett-Packard 3000 Series II

MANAGEMENT SUMMARY

With the announcement of the HP 3000 Series II, Hewlett-Packard has taken a major step toward improved performance for its top-of-the-line minicomputer. Great care has preceded this announcement; more than 40 systems were built and tested before public release.

Main memory has been enlarged four times over the capacity of the older 3000CX and improved by one-third in cycle time, using MOS instead of core. The resultant improvement in overall system performance promises to be highly impressive: HP states that workloads on the Series II systems can be two to six times greater than on the 3000CX. Instruction execution is at least 50 percent faster, and terminal capacity has been doubled.

The processor has been redesigned to take advantage of technical innovations, but in such a way as to be transparent to the user (with the exception of a new extended-precision floating-point format). Also new is a redesigned version of the MPE operating system, entitled MPE-II. Features involving dynamic resource allocation and management have been redesigned or enhanced. Enhancements to the instruction set are designed primarily to offer more privileged instructions to the operating system for increased efficiency.

The Series II release additionally means improvements in file management, in the Image/Query data base management system, and in diagnostics and utility functions.

The HP 3000 was originally introduced in November 1971, for initial delivery in November 1972. By

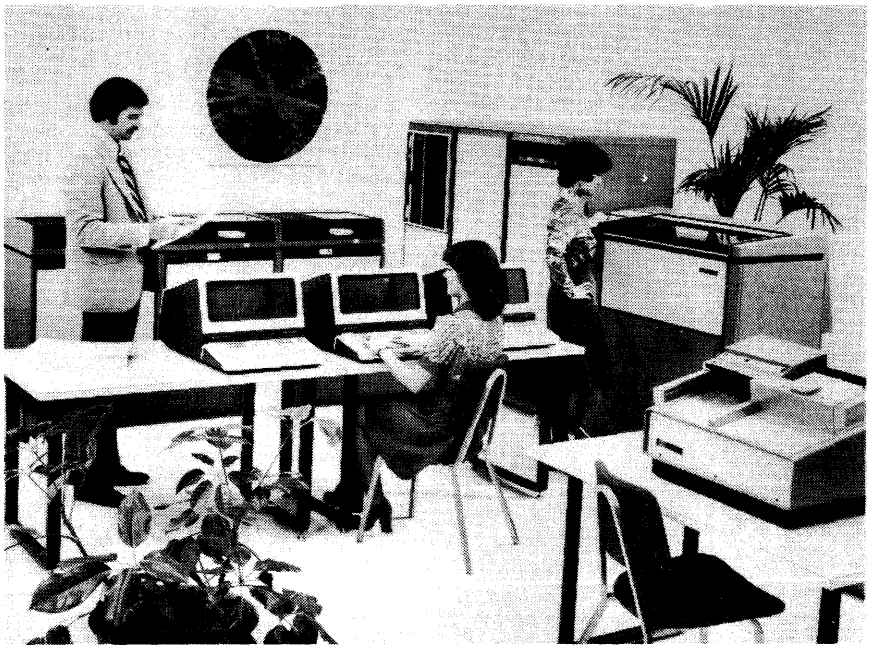
In this third release of the 3000, HP has gone all-out to improve the overall performance of its most powerful computer system. Highlights of the new Series II include MOS fault-control memories of larger capacity, a redesigned processor (transparent to users), an expanded instruction set, firmware-assisted software, a redesigned operating system, Image/Query enhancements, and a new Data Entry Library.

CHARACTERISTICS

MANUFACTURER: Hewlett-Packard Company, General Systems Division, 5303 Stevens Creek Blvd., Santa Clara, California 95050. Telephone (408) 249-7020.

Hewlett-Packard is one of the foremost manufacturers of sophisticated laboratory test equipment and specialized process control instrumentation. In addition to conventional laboratory equipment such as signal generators, oscilloscopes, and voltmeters, the company also manufactures more exotic instruments such as gas chromatographs, digital thermometers, network analyzers, and spectrum analyzers. Other related products include both digital and analog graphic recorders, analytic instrumentation, and medical electronic instrumentation systems. Other Hewlett-Packard Company divisions manufacture hand-held calculators and desk-top calculators.

The company also has two computer manufacturing divisions, the General Systems Division and the Data Systems Division. The former manufactures the HP 3000 Series II general-purpose computer, while the latter produces the 2100 and 21MX minicomputers along with disk drives. Other HP divisions manufacture line printers, magnetic tape transports, and the 2640 series CRT terminals.



The Model 9, largest of the three HP 3000 Series II systems, offers a broad range of expansion capabilities in both memory size and peripheral complement. Starting at 320K bytes, the memory can be increased to 512K bytes and still be housed, along with power supplies, processor, magnetic tape drive, and optional paper tape units, in the three cabinet bays shown here. Up to five additional 47-megabyte disc drives, up to 60 more terminals, and up to three additional printers can be configured with this system. The Model 9 starts at $190,000 for a minimum packaged system that includes the operating system and language processors.

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mid-1973, promised delivery schedules of key software elements had not been met and active marketing was suspended. In November 1973, the HP-3000 was reannounced with a modified version of the operating system. The HP-3000CX system was announced in November 1974, with first deliveries in the first quarter of 1975. Its chief competitors include the DEC PDP-11/70, the Burroughs B 1700, the Univac 90/30, the Data General Eclipse, and the once-ubiquitous IBM 1130.

To date there are over 350 HP 3000's installed, with 60 percent of them utilizing Image, a data base management software system. Image was announced in the summer of 1974 and delivered in the early fall of 1974.

Basically, the HP-3000 Series II is a multiprogramming, multilingual machine that uses either a moving-head disc or a high-speed fixed-head disc unit to provide a maximum swapping area of 4.4 million bytes of virtual storage. Spooling is a standard feature, enabling more efficient use of peripherals.

The smallest of the three models in the Series II line, the Model 5, provides a central processor with a 128K-byte fault-control memory, expandable to 256K bytes; a 14.75-megabyte cartridge disc drive; a 1600-bpi magnetic tape unit; a system console; and a 16-port asynchronous terminal controller. The Model 7 provides a central processor with a 192K-byte fault-control memory, expandable to 256K bytes; two 47-megabyte moving-head disc units; a 1600-bpi magnetic tape unit; a system console; and a 16-port asynchronous terminal controller. The top-of-the-line Model 9 provides a central processor with a 320K-byte fault-control memory, expandable to 512K bytes; two 47-megabyte moving-head disc units; a 1600-bpi magnetic tape unit; a system console; and a 16-port asynchronous terminal controller. Users have the option of selecting other peripherals, including paper tape units, punched card units, and printers ranging in speed from 200 to 1250 lpm. Also available is an asynchronous interface to handle remote job entry.

The central processor features MOS main memory with a cycle time of 700 nanoseconds for a 16-bit fetch, a 32-bit bipolar ROM-based microprocessor, a microprogrammed instruction set consisting of 209 instructions, firmware-assisted software, a 16-level external interrupt priority system, facilities for handling up to 125 peripherals, and an operating system (MPE-II) with virtual memory capabilities, I/O spooling, hardware stacks, and separation of data and program code (for user program sharing).

All language processors, except HP's ALGOL-like SPL, are optional on the Model 5. HP considers the Model 5 to be a general-purpose system with concurrent batch processing and terminal access for educational, commercial, and interactive scientific applications.

The Model 7 includes the SPL, COBOL, and RPG compilers. Data base management through the medium of Image and Query is also standard. HP has designed the

Hewlett-Packard products are sold by 135 sales offices in 37 countries, and are manufactured in facilities in the U.S., United Kingdom, Germany, France, Japan, and Malaysia. The company employs about 31,000 persons worldwide.

MODELS: Model 5, Model 7, and Model 9.

DATE ANNOUNCED: May 1976.

DATE OF FIRST DELIVERY: June 1976.

NUMBER INSTALLED TO DATE: 20 Series II systems. (Over 350 HP 3000 systems of all models have been installed since the product line was announced in November 1971.)

DATA FORMATS

BASIC UNIT: 16-bit word or eight-bit byte.

FIXED-POINT OPERANDS: 16-bit operands can be used by logical or fixed-point arithmetic instructions to represent unsigned 16-bit integers from 0 to 65,535 or signed 15-bit integers from -32,768 to +32,767. Double-integer fixed-point formats provide 32 bits for representation of values from -2 billion to +2 billion. Bit 0 of the most significant word is the sign bit. Logical operands are represented in positive integer format, while fixed-point operands are represented in two's-complement format. Also provided is 28-digit packed decimal arithmetic.

FLOATING-POINT OPERANDS: Single-precision 32-bit (2-word) operands with signed 9-bit exponent and 22-bit positive fraction. Extended-precision 64-bit (4-word) operands with signed 9-bit exponent and 55-bit positive fraction. In both single- and extended-precision formats, the exponent can range between -256 and +255, while an assumed "one" is placed to the left of the binary point in the fraction. (The "one" is disregarded for floating-point zero.) All floating-point numbers are by definition normalized. The binary point is assumed to be between the exponent and fraction. Bit 0 of the first word is the sign bit; the exponent in bits 1 through 9 is biased by +256.

INSTRUCTIONS: The HP-3000 Series II has an unusually rich and varied complement of instructions; all, except the stack operation instructions, are one-word types with 23 distinct formats for 13 different instruction groups. The 65 stack instructions can be packed two per word. In general, each instruction has a number of basic fields. Invariably, the first field is always four bits long and is used to define a specific operation code (for memory reference or loop control instructions) or one of four sub-opcode groups. All sub-opcode type instructions have an operation code extension field whose length and position in the instruction vary depending upon which of the four sub-opcode groups is specified. In some cases, a third operation code field (mini-opcode or special opcode) is used to extend the basic operation code. The rest of the 16-bit instruction is used for a variety of functions (count fields, bit positions, index specification, immediate operand, etc.) and is called the argument.

INTERNAL CODE: ASCII.

MAIN STORAGE

STORAGE TYPE: MOS, requiring 700 nanoseconds every 62 microseconds for memory refresh.

CYCLE TIME: Write, 700 nanoseconds minimum; read, 350 nanoseconds access time and 700 nanoseconds cycle time for a 16-bit fetch.

CAPACITY: 131,072 (128K) to 262,144 (256K) bytes in Model 5; 196,608 (192K) to 262,144 (256K) bytes in

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION & SPEED	MANUFACTURER
MAGNETIC TAPE EQUIPMENT		
30115A	9-track, 800-bpi NRZI/1600-bpi PE, 10.5-inch reels, 45 ips; 36/72 KBS	HP
PRINTERS		
30118A	Comb matrix, 132 positions, 64/128-character sets, 10 characters per inch, 6 or 8 lines per inch, 4 to 14.9-inch paper, 8-channel VFU; 200/165 lpm	HP, under license from Tally
30127A	Drum, 136 positions, 64/96-character sets, 10 characters per inch, 6 or 8 lines per inch, 4 to 16.8-inch paper, 12-channel VFU; 300/240 lpm	Dataproducts 2230
30133A	Drum, 132 positions, 64/96-character sets, 10 characters per inch, 6 or 8 lines per inch, 4 to 16.8-inch paper, 12-channel VFU; 600/436 lpm	Dataproducts 2260
30128A	Drum, 132 positions, 64/96-character sets, 10 characters per inch, 6 or 8 lines per inch, 4 to 19-inch paper, 12-channel VFU; 1250 lpm	Dataproducts 2440
PUNCHED CARD EQUIPMENT		
30106A	Reader, 80-column, 1000-card input hopper and output stacker, reads by column; 600 cpm	Documation M600L
30119A	Reader/Punch/Interpreter, 80-column, 600 & 400-card input hoppers, two 400-card output stackers, off-line data recorder opt.; 200/45 to 75 cpm	Decision Data 8000 Series
PAPER TAPE EQUIPMENT		
30104A	Reader, 8-level, 1-inch tape, rack-mounted; 500 cps	HP
30105A	Punch, 5 to 8-level, 11/16 to 1-inch tape, rack-mounted; 75 cps	Facit-Addo 4070
TERMINALS		
2762A	Type belt printer/keyboard, 75 positions, 96-character set, 10 characters per inch, 6 or 3 lines per inch, 8.5-inch paper, 128 ASCII character keyboard; 10, 15, or 30 cps	GE TermiNet 300
2762B	Type belt printer/keyboard, 120 positions, 96-character set, 10 characters per inch, 6 or 3 lines per inch, 3 to 12.9-inch paper, 128 ASCII character keyboard; 10, 30, or 120 cps	GE TermiNet 1200
2640A	CRT display/keyboard (console), 1920 characters, 24 lines by 80 characters, 64/128-character sets, up to 8K-byte memory; 110, 150, 300, 1200, or 2400 bps	HP
2644A	CRT display/keyboard, 1920 characters, 24 lines by 80 characters, 64/128-character sets, 4K-byte memory, dual minitape cartridges for up to 220K bytes; 110, 150, 300, 1200, or 2400 bps	HP
PLOTTER INTERFACE		
30126A	Interface for CalComp Series 500, 600, or 700 (excluding 745 & 748) plotters	HP

Model 7 for on-line medium-scale commercial and administrative applications.

The largest member of the family, the Model 9, comes with a full complement of language processors. The list includes FORTRAN, COBOL, RPG, SPL, and BASIC (both a compiler and interpreter). Also standard are the Scientific Library, a collection of procedures for the most common scientific functions; the Data Entry Library, a programming aid for forms creation, deletion, and updating designed to simplify terminal-oriented data

Model 7; 327,680 (320K) to 524,288 (512K) bytes in Model 9. Memory increments are 65,536 (64K) bytes.

CHECKING: Standard parity bit per 16-bit word is set with each write operation and checked with each read.

Fault-Control Memory is used in all Series II models. The system is composed of modules, each of which is made up of a memory and control logging board (MCL), fault correction array boards (FCA), and up to four 64K-byte memory array boards. The MCL, beside controlling memory module operation and interfacing it to the system, contains 256K bits of MOS for fault logging. The FCA

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collection; and the Image/Query subsystem for data base management. HP has designed the Model 9 to meet the needs of the larger commercial and scientific users who require a full-scale general-purpose system. The company's support of FORTRAN, SPL and BASIC indicate its scientific bent, while the Report Program Generator (RPG) and continued support of COBOL show renewed interest and strength in business applications.

Hewlett-Packard stresses flexible concurrent, multilingual environments where terminal-oriented scientific/engineering problem solving is likely to be combined with background batch business processing. The Models 5 and 7 can be configured to handle up to 31 terminals; the Model 9, up to 63 terminals. Terminals can be opened as files or used for program development with equal facility. Emulation of the IBM 2780/3780 batch terminals is available on all models. All models can also be configured with either the 30300B Programmable Controller or the 30301B Real-Time Programmable Controller.

At present, the Series II is available only in packaged configurations. Purchase prices range from $110,000 for a basic Model 5, to $150,000 for the minimum Model 7 configuration, to $190,000 for the top-of-the-line Model 9. HP will upgrade any 3000CX to a 256K-byte Series II Model 9 for $75,000. The 3000CX will continue to be supported, but it will not be actively marketed.

Customer services for the Series II are extensive. They include pre-installation site planning, installation, several levels of training given both at users' sites and at HP, several levels of on-site hardware and software service, program consultation both on-site and via toll-free telephone, reference manual updates, information newsletters, and an active users' group.

The Series II is being marketed to four general classes of prospective users: small manufacturers with sales in the 80 million dollar range; *Fortune* 500 or 1000 companies who wish to decentralize and have several applications in each location; educational institutions, both on the collage/university and secondary school levels; and OEM accounts and system houses with capabilities for high-level implementation of high-level languages. The main thrust of this marketing effort is toward distributed processing applications instead of the older batch processing market.

Maintenance is handled through 53 HP offices in the U.S., 9 in Canada, 18 in Central and South America, and 103 in Europe, Africa, Asia, and Australia. Both on-call and scheduled services are available. The basic monthly maintenance contract provides for typical four-hour response times within a 100-mile radius of a major metropolitan area. Prime-time coverage is provided Monday through Friday from 8 a.m. to 5 p.m.

USER REACTION

Detailed below are the results of Datapro's user interviews and surveys taken between the summer of 1975 and the present. The data which appears in this section is based on

boards expand each word of memory to 21 bits by appending 5 check bits. The check bits, called a Hamming code, and a special HP algorithm enable the system to automatically detect and correct a single-bit error and detect up to 30 percent of the multi-bit errors. The FCA boards also interface the fault-logging RAM (random-access memory) to the Series II I/O system. The operating system, MPE-II, periodically purges this RAM and stores it in a disc file for later access by the HP customer engineer.

STORAGE PROTECTION: Upper and lower address boundaries, provided by certain registers, define the limits of authorized program access in main memory. The microprogram routinely checks for bounds violation during execution (overlapped with operand fetch), and generates an interrupt if an unauthorized memory access attempt is made. Bounds violations may be classified under program transfer or reference, data reference, and stack overflow or underflow.

RESERVED STORAGE: The first 11 main memory locations are reserved for global system pointers used in the firmware implementation of virtual memory and variable-length program segmentation. Following this is a device reference table containing a set of forward entries (one per device, maximum 125 entries) containing device interrupt vectors and the identity of the drivers for each device.

CENTRAL PROCESSOR

GENERAL: The HP-3000 Series II is a complex system that includes a firmware-implemented instruction set; firmware-implemented repetitive functions such as subroutine linkage, string processing, and buffer transfers; firmware-assisted software; noninterleaved but concurrently operating 256K-byte fault-control memory modules; battery backup for 60 to 90 minutes, depending on memory size; power fail/auto restart; bus control clock; and crystal clock dedicated to process execution measurements. Firmware-assisted software includes the interrupt handler, cold-start loader, power-failure data-saving routines, automatic restart routines, and front panel-initiated diagnostics. The basic microprogramming architecture is asynchronous and designed to faciliate a multiprogrammed, variable-length, code-segmentation, virtual-memory mode of operation with extensive stack processing.

The system design emphasizes a modular structure, with the CPU, I/O processor (IOP), and its Module Control Unit (MCU) connected via a high-speed central data bus to other system modules such as the fault-control memory module. The MCU is shared by the CPU and IOP. The I/O processor executes I/O programs in parallel with CPU operations.

The CPU is divided into the instruction decoder, firmware storage and control, and hardware processor, is microprocessor-controlled, and uses a pipeline technique. It receives an instruction word from memory and translates it into a microprogram starting address. As this instruction word is being executed, another is received.

Program code and data are maintained in strictly separate domains and cannot be intermixed except for "immediate" type data present in program instructions. This design was chosen so that all program code would be protected from alteration, thus permitting the development of re-entrant programs for multi-thread operation.

CONTROL STORAGE: Bipolar ROM (read-only memory) consisting of 10,240 32-bit words. Control storage is not directly accessible to the end user; it has a cycle time of 175 nanoseconds and an average instruction execution time of 175 nanoseconds.

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the older HP 3000 and 3000CX. Thus, it provides an overall picture of company and product performance, but does not reflect any user experience with the new product, the Series II.

Represented were 8 companies with 10 installed systems. The earliest date of installation was March 1974, and the average time of installation was 18 months. The majority (8 out of 10) of the systems were operating with a memory size of 128K bytes. Seven of the 10 systems were purchased, and the remaining 3 were on third-party lease. There was an equal mix of scientific and business applications, including market research, general accounting, and data communications (RJE to an IBM 370/195). Systems replaced included the IBM 1130 and 360/20, and the HP 2100. The number of terminals per system varied from a low of 2 to a high of 16. Among the eight users, all of the programming languages offered by HP were being utilized. No one user, however, used more than three languages. The most popular combination appeared to be FORTRAN, BASIC, and SPL.

The table below shows how the users rated the HP 3000 and 3000CX, which preceded the present HP 3000 Series II product line.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	5	3	0	0	3.6
Reliability of mainframe	6	0	2	0	3.5
Reliability of peripherals	5	3	0	0	3.6
Maintenance service:					
Responsiveness	4	4	0	0	3.5
Effectiveness	5	2	1	0	3.5
Technical support	4	2	1	0	3.4
Manufacturer's software:					
Operating system	5	2	0	1	3.4
Compilers and assemblers	5	2	1	0	3.5
Application programs	3	1	3	0	3.0
Ease of programming	4	3	0	0	3.6
Ease of conversion	2	3	2	0	3.0
Overall satisfaction	6	1	1	0	3.6

*Weighted average on a scale of 4.0 for Excellent

These performance ratings make it clear that users of the HP 3000 and 3000CX systems are finding little to complain about—and the improved 3000 Series II should make them even happier. It appears that the problems that arose from the rather unfortunate entry of the original HP 3000 have now been solved. If any significant area of weakness still exists in the hardware, software, or vendor support, it certainly was not apparent from the responses of these generally well-satisfied users.□

REGISTERS: There are 38 hardware registers, 20 of which are accessible to the programmer. Those dedicated to system use are mostly 16-bit registers. These include the current and next instruction registers; nine registers for scratchpad, flag, and interrupt purposes; two I/O registers; three memory address registers; and two firmware address registers.

Registers accessible to the programmer include the code segment pointer group; the stack pointer group; top of stack group; and registers named Index, Status, Switch, and Program Clock. All registers are 16 bits in length except the bank registers, which are 2 bits, and the Program Clock register, which is 16 bits.

The code segment group consists of the Program Base regsiter (PB), which defines the program base of the code segment being executed; the Program Counter (P), which contains the 16-bit absolute address of the instruction being executed; the Program Limit register (PL), which defines the limit of the code segment being executed; and the Program Bank register (PB-Bank) which defines the bank of 64K words where the code segment resides.

The stack pointer group is divided into the data segment group and the stack pointers. The data segment group includes the Data Base register (DB), used to define the data base of the current user's stack; the Q register, utilized to define the current stack master in the current data segment; the Data Limit register (DL), where the data limit of the current data segment is defined; and the Data Base Bank register, which contains the location of the bank in which the stack or split stacks reside. The stack pointers include the SM register, which defines the number of top-of-stack elements that are in CPU Stack registers; the Z register, whose function is to define the stack limit of the current user's stack; and the Stack Bank register (S-Bank), used to define the 64K word bank in which the stack resides.

The Status register (STA) indicates the current status of the computer hardware, including whether the system is in user or privileged mode. The Program Clock register (PCLK) is a counter loaded and read by software. The Switch register (SWCH) is a 16-bit register representing front panel switches used for bootstrapping and fault diagnosis.

ADDRESSING: Only privileged instructions may use absolute addressing. All other addressing is performed using one of the six allowable relative techniques. Two techniques apply to code, while four apply to data. Except for privileged instructions (including I/O), all word addressing is indirect, indexed, or indirect indexed relative to the P-register (plus or minus), the Q-register (plus or minus), the DB-register (plus only), or the S-register, a logical addition of the contents of the SM and SR registers (minus only). Indirect addressing and indexing are both provided, individually or in combination. Up to 65K words (addresses) can be referenced by a memory reference instruction. For byte addressing, the left half of each word can be addressed, permitting a memory byte reference instruction to address up to 32K bytes. Byte addressing is direct, direct-indexed, indirect, and indirect-indexed relative to the DB register (plus only).

Double-word indexing is provided for two memory address instructions that automatically cause the index register contents to be incremented by two during development of the effective address.

INSTRUCTION REPERTOIRE: In total, there are 209 machine instructions in the HP-3000 Series II: 65 stack instructions, 16 memory address instructions, 13 branch instructions, 4 loop control instructions, 6 single-word shift instructions, 6 double-word shift instructions, 3 triple-word shift instructions, 1 field instruction, 10 I/O and interrupt instructions, 15 immediate instructions, 17 program control and special instructions, 7 register control instructions, 6 extended-precision floating-point instructions, 8 privileged memory reference instructions, 12 packed decimal instructions, and 12 move instructions. Approximately 19 percent of the instructions are privileged.

INSTRUCTION TIMINGS: All times are for full-word (16-bit) fixed-point operands and for single-precision (32-bit) floating-point operands, in microseconds:

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	Fixed Point	Floating Point
Load/Store	1.6/1.9	2.6/3.0
Add/Subtract	0.55	8.2 avg./8.4 avg.
Multiply/Divide	5.25/6.125	15.2/19.4
Compare and Branch	3.3	3.7

INTERRUPTS: The interrupt system provides for up to 125 external interrupts. There are 16 levels of interrupt masking, and each device is initially assigned to one of the 16 levels to fix priorities and permit masking under software control. Under microprogram control, context switching for an interrupt is performed in an average time of 21 microseconds (minimum 18; maximum 24.5). The interrupt routines operate on a common Interrupt Control Stack to permit nesting of interrupt routines for multiple interrupts; context switching time is reduced by about two microseconds should nested interrupts occur. Twenty-one internal interrupts for user errors, system violations, hardware faults, and power fail/restart are also provided, plus 14 traps for arithmetic errors and illegal use of instructions or privileged mode.

The priority assigned to external devices in determined by the device's logical proximity to the I/O processor (IOP) on the interrupt poll line. Masking is permissible through the 16-bit bit mask word, which will enable or disable an interrupt request according to the bit pattern of the word.

PHYSICAL SPECIFICATIONS: Models 5, 7, and 9 use cabinets measuring 64.5 inches high, 21 inches wide, and 33 inches deep. Models 5 and 7 require two of these cabinets, while Model 9 requires three for the processor, one magnetic tape drive, power supplies, and related gear.

The HP 3000 Series II operates at a temperature between 59 and 89 degrees F. with a relative humidity tolerance of 40 to 80 percent, noncondensing. The Model 5 outputs 14,450 BTU per hour; the Model 7, 19,800; and the Model 9, 22,900. Power requirements for all models are 208 volts +5 percent -10 percent, 3-phase, 60 Hz +0.5Hz, or 230 volts +5 percent -10 percent, single phase, 50 Hz +0.5Hz. Air conditioning requirements will exceed the average office installation by about two tons. A raised floor is not required, but is recommended.

INPUT/OUTPUT CONTROL

I/O PROCESSOR: The IOP operates in parallel with the CPU, and communicates with the CPU as well as other system modules over a high-speed central data bus. Data is transferred directly to or from memory over the central data bus (via a high-speed selector channel) or multiplexed via the IOP. Up to five system modules (CPU, IOP, Selector channel, and two memory modules) can be attached to the central data bus, and up to 125 I/O devices can be connected to the system via the IOP bus, the multiplexer channel, and the selector channel. Each of the modules in the system can operate independently at its own speed when not operating over the central bus.

The selector channel can transfer data at a maximum rate of 1.9 megabytes per second. The IOP bus has a maximum transmission rate of 952K bytes per second. The channel can accommodate one controller at present. The aggregate selector channel data rate cannot exceed the central data bus maximum data rate of 2.86 megabytes per second. The multiplexer channel can handle up to 16 device controllers, with an aggregate data rate of 1.038 (input) and 0.952 (output) megabytes per second. Data from the multiplexer channel is passed through the IOP for transfer to memory via the central data bus.

In addition to the multiplexer and selector modes of I/O data transfer, a direct I/O mode is also available that permits the CPU to transfer information directly to/from low-speed asynchronous peripheral devices without involving memory, the multiplexer, or the selector channels at rates of 4.5 megabytes per second. Four privileged I/O instructions are included to handle these one-word direct data transfers to/from the top of a stack in memory.

SIMULTANEOUS OPERATINGS: In addition to overlapped operations between the CPU and IOP, and the basically asynchronous nature of the architecture, a "microcode pipeline" and concurrent operation of the memory modules are also implemented on the HP 3000 Series II.

CONFIGURATION RULES

As is true with most minicomputers, the amount of peripheral equipment available is restricted only by the number of slots available in the CPU chassis or its extensions, by software restrictions, and by controller limitations.

The Model 5 comes with two 64K-byte memory increments, and two additional increments are allowable. One port controller and selector channel are standard; they are connected to the central data bus, allowing for up to four 15-megabyte cartridge disc drives (one is standard). Supplied as standard on the IOP bus are an asynchronous terminal controller (ATC) and a magnetic tape controller (MTC) with one tape drive. The ATC controls the system console and up to 15 other terminals. Optional support for 103 or 103/202 modems can be included. The MTC controls up to four magnetic tape drives, either 800 or 1600 bpi. The drives may be intermixed on the same controller. Up to 15 slots are available for connection of additional peripherals.

The Model 7 comes with three 64K-byte memory increments, and one additional increment is allowable. Model 9 comes standard with five 64K-byte memory increments, and three additional increments are optional. The port controller and selector channel for connection to the central data bus and up to four 15-megabyte cartridge disc drives are optional on both Models 7 and 9. Supplied as standard on Models 7 and 9 is the ATC configuration mentioned under the Model 5 above. The 103 modem control is standard, while 103/202 modem control remains optional. Also supplied as standard is the MTC discussed under the Model 5. Additionally, Models 7 and 9 include two 47-megabyte moving-head disc drives and a controller as standard equipment; up to six additional drives for connection to the same controller are optional. Up to 13 slots on the Model 7 and 14 slots on the Model 9 are available for connection of additional peripherals.

Additional peripherals, their slot requirements, and the maximum numbers of allowable units, if specified, are as follows. Models 5 and 7 can support one additional ATC, while the Model 9 can support up to three additional ATC's. Each ATC can support up to 16 terminals. The ATC and the 103 or 103/202 modem support option require one slot each. A plotter interface supporting CalComp Series 500, 600, or 700 plotters is optional and requires one slot. Both a programmable and a real-time programmable controller are optional. Each requires one slot, but both are not allowable on the same system at the same time. Up to three IBM 2780/3780 emulation subsystems are optional, each requiring one slot.

Punched card equipment includes up to two 600-cpm card readers, each requiring one slot, and a card reader/punch, requiring one slot. A paper tape reader and a paper tape punch each require one slot and are housed in a third cabinet, which is standard on Model 9 and optional on

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Models 5 and 7. A maximum of four line printers per system are allowed and may be selected from units with speeds of 200, 300, 600, and 1250 lpm. An additional magnetic tape controller requires two slots and can accommodate four 800-bpi or 1600-bpi drives in any combination.

The Model 5 can be configured with up to eight 47-megabyte moving-head disc drives as an option. As previously discussed, this drive is standard on Models 7 and 9. The controller for these drives requires three slots.

MPE-II, the operating system, will support the following terminals in addition to HP's own 2640A and 2644A: Teletype Model 33, 35, or 37 ASR Teleprinters, Execuport 300 Data Communications Transceiver Terminal, HP 2600A Keyboard Display Terminal, Datapoint 3300 Keyboard Display Terminal, Memorex 1240 Communications Terminal, and HP 2615A Terminal.

MASS STORAGE

30102A MOVING-HEAD DISC SUBSYSTEM: Consists of a controller for up to eight drives and one to eight 2316-type removable disc pack drives. Each drive has a capacity of 47,104,000 bytes recorded on an 11-platter pack with 20 usable surfaces. There are 400 data tracks per surface, plus 6 spares. Each track contains 23 sectors with 256 bytes per sector for a total of 5888 bytes. Average head movement time is 29 milliseconds; average rotational delay is 12.5 milliseconds. The drive has a rotational speed of 2400 prm and a data transfer rate of 312K bytes per second. The drive is manufactured by ISS/Univac as the ISS Model 715.

30129A CARTRIDGE DISC SUBSYSTEM: Consists of a controller and one cartridge drive that uses one fixed platter and one removable, front-loading, IBM 2315-type cartridge. Up to three additional Model 30329A drives may be added to the subsystem for a total of four. The drive data capacity is software-selectable as either 4,423,680 bytes, where 120 cylinders are utilized as a high-speed system disc, or 14,745,600 bytes, where all 400 cylinders are put to general use. In either mode, there are 256 bytes per sector, 48 sectors per track, and 12,288 bytes per track. There are three usable surfaces and three tracks per cylinder. In the 4.41-megabyte mode, there are 1,474,560 bytes per surface and 2,949,120 bytes per cartridge. In the 14.75-megabyte mode, there are 4,915,200 bytes per surface and 2,949,120 bytes per cartridge. In the 14.75-megabyte mode, there are 4,915,200 bytes per surface and 9,830,400 bytes per cartridge. The drive has a rotational speed of 3600 rpm. Average head movement time is 25 milliseconds; average rotational delay is 8.3 milliseconds. The data transfer rate is 937.5K bytes per second. The drive is manufactured by HP.

INPUT/OUTPUT UNITS

See Peripherals/Terminals Table.

COMMUNICATIONS CONTROL

30032B ASYNCHRONOUS TERMINAL CONTROLLER: Controls up to 16 additional Bell 103-type data sets. With Option 002, Bell 202-type data sets can be handled (for the HP 2640A only). Speeds of 110, 150, 300, 700, 1200, and 2400 bps are implemented. The 30032B is connected via a 16-bit parallel interface.

30300A PROGRAMMABLE CONTROLLER SUBSYSTEM: An HP-2100 minicomputer and interconnecting hardware for the attachment of foreign devices and on-line instrumentation applications; the controller makes available up to 42 (with extender) I/O channels. The 30300A utilizes a 16-bit parallel hard-wired interface between the HP-2100 and the HP-3000 Series II, with a transfer rate of up to 200K words per second.

30301A REAL-TIME PROGRAMMABLE CONTROLLER SUBSYSTEM: Provides dedicated real-time access to measurement and control devices simultaneously with general data processing. The controller makes 42 (with extender) I/O channels available. The 30301A offers hard-wired 16-bit parallel data transfer at up to 200K words/sec.

30055A SYNCHRONOUS SINGLE LINE CONTROLLER: Hardware portion of the 2780/3780 emulator subsystem; provides all IBM 2780 and 3780 capabilities plus 22 optional capabilities available from batch and interactive terminals under MPE-II. The controller uses public telephone or leased lines at speeds up to 4800 bps.

SOFTWARE

OPERATING SYSTEM: The Multiprogramming Executive II (MPE-II) operating system is the successor to the MPE/C system used on the HP 3000CX. It provides concurrent processing for multiprogrammed batch, time-sharing, real-time, and transaction processing. It is composed of a command interpreter, file management system, input/output system, virtual memory manager, segmenter, loader, job session scheduler, process dispatcher, user trap manager, spooling facility, disc space manager, utility intrinsics, backup/restore facility, initiator configurator, system console manager, power fail/auto restart, accounting facility, and logging facility. Support is provided for FORTRAN, ANSI COBOL, BASIC, RPG II, SPL, a program file edit subsystem (EDIT/3000), an interactive diagnostics generator (SLEUTH), a generalized sort and merge (SORT/3000), a compiler library, and general utilities.

Under virtual memory allocation, each program can be segmented into as many as 63 segments. Each code segment can be up to 32K bytes in length, and each data segment up to 64K bytes. The principle of memory allocation dictates that only the essential segments be in memory at any particular time. Program execution for a particular user (called a process by HP) then proceeds until additional segments are needed. The operating system remembers all segments brought into memory under a concept called segment trapping. The goal is to keep as much as possible of a program's working set—the code, data, and system data segments used most recently—in memory. This is accomplished by the use of an HP-developed algorithm called the segment trap frequency algorithm. The algorithm remembers the frequency of use of each segment of each working set and overlays only the least-used segment of a low-priority work set.

Features that have been redesigned or added to MPE include a local compression algorithm, memory allocation manager, and program dispatcher. The local compression algorithm functions to keep user segments tight together by executing large block moves within memory whenever necessary so that the need for frequent overlays is reduced. The memory allocation manager uses the segment trap frequency and local compression algorithms to optimize system throughput as much as possible. The program dispatcher schedules processes for execution by using an algorithm which handles three concurrently existing queues, the new crystal process clock, and instruction set enhancements for privileged operations. HP states that this dispatcher is three times faster than the one used on the 3000CX under MPE/C.

Other improvements to MPE include file control intrinsics that allow terminals to be opened as files; files that can

Hewlett-Packard 3000 Series II

cross physical volumes; better HP 2640A and 2644A terminal interfaces; up to 32 file extents; the ability to restore files to a previous volume; magnetic tape buffers of up to 32K bytes; and a power fail/auto restart that does not require human intervention.

Under MPE-II, all I/O is handled by the file system; thus, programs are essentially device-independent. The IOP allows for file manipulation without extensive JCL. In any access mode, whether sequential or direct, security is maintained for users, groups, accounts, and individual files.

Information such as CPU time, connect time, and disc file space is kept by user, group, and account. A Report command allows extraction of this information.

Other features of MPE-II include utilization of the machine's hardware-implemented stack architecture, recursive/re-entrant code, spooling from both terminal and batch devices, and remote processing via terminals.

Recommended disc space allocation for MPE-II, its subsystems, and virtual memory is somewhat over 2 million bytes. MPE-II is disc-resident, with about 8 percent (approximately 40K bytes) resident in memory at any one time.

LANGUAGES: The HP 3000 Series II is a multilingual system that supports five programming languages plus a data base management system.

SPL 3000 is the Systems Programming Language for the HP 3000 Series II. It is ALGOL-like, but is machine-dependent (direct register references, bit extraction, etc.). It supports one-dimensional arrays and CALL's from any other language available to the system. SPL is free-form in structure and includes other features such as recursive procedures, high-level statements with unlimited nesting, and arithmetic and logical expressions. A debugging aid, TRACE/3000, is provided. HP states that MPE-II and all compilers are written in SPL.

FORTRAN/3000 is based on American National Standard FORTRAN, X3.9-1966, and is a full implementation of that standard. As a programming aid, TRACE/3000 may be used for debugging.

Described below are the FORTRAN language extensions implemented by HP. Source programs may be written in a free-field as well as in a fixed-field format. Symbolic names may consist of up to 15 characters instead of the usual 6. Character type data may be used to facilitate string manipulation. Arrays may have up to 255 dimensions instead of the standard 3. A label may be used as an actual argument in a CALL statement to allow alternative return points following execution of the subroutine referenced by CALL. STOP or PAUSE statements use a decimal integer or character string for identification rather than an octal integer. Both 16-bit and 32-bit integers are supported. Subroutines and functions may have secondary entry points. A built-in cross-reference facility is available as a compile-time option. Undefined variables are detected at compute time, and generic functions are recognized.

COBOL/3000 is based on American National Standard COBOL, X3.23-1968, and includes these modules, all at high levels: Nucleus, Table Handling, Sequential Access, Random Access, Sort, Segmentation, and Library. At present, the Report Writer is not implemented.

Language extensions implemented by HP include interprogram communication, packed decimal (COMPUTATIONAL-3), note lines, current date in the form of MM/DD/YY, time of day in the form of HHMMSS, THEN optional, multiple REDEFINEs of a given location, Unary+, Go to MORE-LABELS EXIT, synchronized index data items, and forms message for special forms.

RPG/3000 is compatible to a high degree with RPG and RPG II as developed by IBM. Language extensions implemented by HP include parameters for external subroutine calls, an interface to the data base management system, three methods for run-time error options, a cross-reference error option, automatic program segmentation, EBCDIC/ASCII automatic translation, input/output terminal files, and no requirements for calculation indicator repetition for duplicate conditioning indicators.

BASIC/3000 is implemented as an interpreter and a compiler. The interpreter offers an effective way to debug programs interactively, while the compiler yields more efficient code with average program execution speeds 10 to 30 times faster for CPU-bound programs and one to four times faster for I/O-bound programs. Four numeric data types are possible: real, integer, complex, and extended precision.

BASIC/3000 also provides the following HP extensions. Mixed-mode arithmetic and program chaining with common storage are provided, along with a built-in debugging system. External routine calls, strings and string arrays, and multiple-line statements and functions are all permitted. Picture output formats can be implemented, and the programmer can use timed input by way of the ENTER statement. Both direct and sequential access to files are allowed. File creation and purging are under program control, while file security is user-definable with passwords.

All implemented languages have the ability to call a subroutine written in another language. Of equal importance is the facility provided by the MPE-II file system for all languages to utilize a common file structure, therefore providing uniform access to disc and tape.

COMMUNICATIONS: Software support for communications is available through the 30130C Emulation Subsystem, the 30300B Programmable Controller Subsystem, and the 30301B Real-Time Programmable Controller Subsystem.

In the Emulation Subsystem, the supplied software supports all significant IBM 2780/3780 capabilities on point-to-point lines, plus most optional capabilities such as EBCDIC and ASCII transparency, short-record truncation, and multi-record transmission.

In the 30300B Programmable Controller Subsystem, a Cross Assembler is supplied to develop programs on the HP-3000 Series II for use on the programmable controller. The assembler's support includes extended arithmetic and floating-point instructions.

In the 30301B Real-Time Programmable Controller Subsystem, HP has developed a program set including the RTE operating system, which allows running multiple instrumentation programs concurrently; the RTE scheduler, which orders program execution according to 99 user-supplied priority levels; and the ability to write applications, such as data acquisition and process monitoring, in FORTRAN.

IMAGE/3000: The data base management system for the HP 3000 Series II is oriented toward general-purpose data base management and operates in both terminal and batch environments.

IMAGE consists of three parts: a data base definition subsystem (DBDS), a data base management subsystem (DBMS), and a data base utility subsystem (DBUS). Typically, a data base manager would use DBDS to define