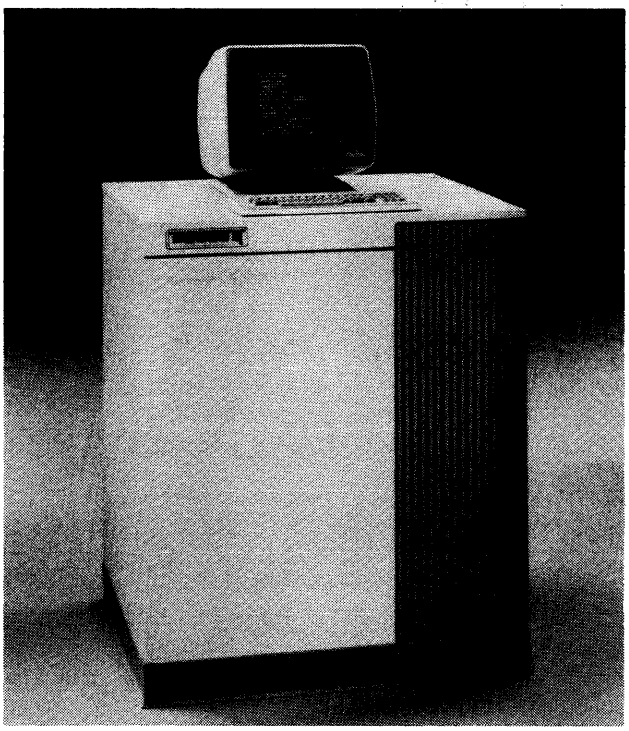
Burroughs A 5

PRODUCT DESCRIPTION

Burroughs has added a third system to the low end of its A Series of mainframes. The A 5 is a single-processor system targeted to offer a higher power alternative to the A 3 system users, and to fill a performance gap between the low-end A 3 and the medium-scale A 9 Series.

The basic cabinet and the architecture are the same for the A 2, A 3, and A 5, but the central processor of the A 5 has been enhanced, featuring an MC microprocessor with faster chip technology resulting in 2.3 times the performance of the A 3. The A 5 system provides an option for Burroughs customers who want more processing power than is available from the A 3, but do not require a larger mainframe. Users of the A 2 and A 3 systems looking for more processing power can upgrade their computers within the same cabinet by simply replacing the CPU and power supplies. The dual-processor A 3 K cannot be upgraded to an A 5.

The A 5 is a small-scale, general purpose computer designed to perform applications such as batch, on-line, and realtime processing. The A 5 can also serve as a distributed data processing system for Burroughs' large systems. With the identical operating system and code compatibility, the same programs can be run at a remote location. The use of Burroughs Network Architecture (BNA) allows the central site to control the A 5 at a remote location.



The Burroughs' A 5 Model F has a main memory range of 6 to 24 megabytes, and supports up to 16 Data Link Processors.

PRODUCT ANNOUNCED: The A 5 system brings the total number of A Systems up to seven. The A 5 is a single-processor system with a main memory of 6 megabytes, expandable to 24 megabytes in 3-megabyte increments. The A 5 is compatible with all the other A Systems and provides a field upgrade for A 3 users.

COMPETITION: Honeywell DPS 8/47, IBM 4381, and NCR 8600.

DATE ANNOUNCED: July 21, 1986.

SCHEDULED DELIVERY: September 1986.

BASIC SPECIFICATIONS

MANUFACTURER: Burroughs Corporation, 1 Burroughs Place, Detroit, Michigan 48232. Telephone (313) 972-7000. In Canada: Burroughs Canada, 801 York Mills Road, Don Mills, Ontario M3B 1X8. Telephone (416) 445-4030.

MODEL: Burroughs A 5 Model F.

CONFIGURATION: The distributed architecture of the A 5 system consists of five major subsystems: one Central Processor Unit (CPU), a Memory Subsystem, an Input/Output Subsystem, a Data Communications Subsystem and a Maintenance Subsystem. All subsystems and their components are housed in the same cabinet. The Central Processor Unit, the Memory Control Unit (MCU), the Memory Storage Boards, the Host Dependent Port (HDP), and the User Interface Processor (UIP) share the same housing with the Input/Output Subsystem containing the Data Link Processors (DLPs), the Data Link Interface (DLI), and the Message Level Interface (MLI). The processor cabinet also contains four integrated 8-inch Winchester disk drives with a capacity of 122.8 megabytes of formatted data per drive. The interface between the disk drives and the central processor is provided by the Storage Module Device (SMD) DLP.

CENTRAL PROCESSOR AND MEMORY: The Central Processor Unit is a microprogrammed processor that makes extensive use of Transistor-to-Transistor Logic (TTL) and Very Large Scale Integration (VLSI) gate arrays. The central processor is functionally subdivided into relatively independent submodules.

The storage element of the processor is organized as a Register File and made up of 32 words that are 48 bits wide. The Arithmetic/Logic Unit (ALU) located in the Data Section performs all mathematical and logic functions required by other modules in the system. The Condition Logic Module receives data and status inputs from the Data Section, MCU, and the HDP to accomplish condition checking. Tag storage and selection, counter and timer implementation, and address decoupling is also performed by the Condition Logic Module.

The A 5 system utilizes buses to transfer data between the various modules. The 52-bit wide Memory Bus transfers data between the MCU and the processor, and also between the HDP and the processor. The HDP transfers two bytes of data at a time, utilizing the upper 16 bits of the Memory Bus. The Logic supervising this transfer is contained in the central processor. The HDP ensures the integrity of the data by use of both vertical and longitudinal checking.

Burroughs A 5

The A 5 features Transistor-to-Transistor Logic (TTL), Very Large Scale Integration (VLSI) gate arrays, storage devices and drivers, and 256K-bit RAM chip high-density memory technology that results in higher machine throughput, increased memory reliability, lower costs for power and air conditioning and a smaller footprint.

RELATIONSHIP TO CURRENT PRODUCT LINE: The A 5 uses the Master Control Program/Advanced System (MCP/AS) operating system and the complete range of A Series software, including the InterPro software and the Logic and Information Network Compiler (Linc II). The A 5 will also run software based on the most recent versions of Burroughs' earlier MCP operating system without recompilation.

All peripheral equipment, including terminals and workstations, qualified for the other A Series systems are supported on the A 5.

COMPETITIVE POSITION: The approximate MIPS (Million Instructions Per Second) rating of the A 3 system is 0.7, which would give the A 5 a rating of about 1.6 MIPS and make it comparable with the IBM 4381 Model Group 11 with a rating of approximately 2.0 MIPS. The A 5 also competes with the Honeywell DPS 8/47 with a MIPS rating of 1.2, and the NCR 8635 with a rating of 1.0 MIPS. □

The Memory Subsystem consists of Memory Storage Boards, a Memory Control Unit, and a Memory Bus. The MCU serves as the interface between the processor and the main memory subsystem. Main memory is based on 256K-bit dynamic RAM chip technology and is expandable in 3-megabyte increments, from a base of 6 megabytes to a maximum of 24 megabytes. The MCU checks the integrity of data received from memory and logs hardware and software failures. Logic contained in the MCU performs single-bit error corrections and detects multiple-bit errors. The MCU also issues commands to the Memory Storage Boards to correct any soft errors in main memory. The A 5 uses a 60-bit memory word consisting of 48 data bits, four control bits, and eight error-correcting bits.

INPUT/OUTPUT SUBSYSTEM: The Host Dependent Port serves as the interface between the central processor and the I/O Subsystem through the Message Level Interface and the Data Link Interface. The I/O base subsystem contains a series of specialized Data Link Processors (DLPs) responsible for transferring data to and from the peripheral devices and the data communications subsystem, thereby relieving the burden on the central processor. There is a special DLP for each type of peripheral system. Some DLPs can service multiple peripherals of the same type through standard peripheral exchanges. Each DLP includes a microprocessor, a peripheral interface, and a quantity of local memory. The I/O subsystem can support up to 16 DLPs and an I/O bandpass of 3.4 megabytes per second.

The Data Communications DLPs are located in the I/O base in the A 5 processor cabinet and are designed for small to medium-size networks. A maximum of four Data Communications DLPs can be supported, with each DLP controlling up to four communication lines. For larger networks the Network Support Processor (NSP), the Line Support Processor (LSP), or the front-end processor CP 2000 are available as an option and are supported by the A 5 system.

The core of the Maintenance Subsystem is the User Interface Processor. The UIP performs system intialization and provides diagnostic testing for the components of the central processor, memory and I/O subsystems. The UIP also provides the interface for a remote diagnostic link that enables all diagnostic routines to be run and monitored at a remote location.

SOFTWARE: The Master Control Program/Advanced System (MCP/AS), designed to support the advanced architecture of the A Series family of computers, is the operating system used by the A 5. Under the MCP/AS, programs running on the A 5 can directly address the entire complement of main memory, up to 24 megabytes. The MCP/AS continually and automatically assigns resources, initiates jobs, and monitors their performance in a multiprogramming environment. The operating system is also responsible for assigning memory, managing input/output functions, communicating with the operator, logging system use, maintaining a library of all files, and supervising other functions.

The mainframe and workstation integration products Data Transfer System (DTS) and Host Link allow intelligent workstations such as the ET 2000, B 20, and B 50 to transfer information to and from the mainframe and utilize its resources.

Burroughs InterPro software modules can be implemented individually or as a complete package and include MARC (Menu Assisted Resource Control), IDC (Interactive Data Communications Configurator), SDF (Screen Design Facility), COMS (Communication Management System), ADDS (Advanced Data Dictionary System), and ERGO (Extended Retrieval with Graphic Output).

Among the other software products available for the A 5 are DMS II (Data Management System II), Data-Aid, WFL (Work Flow Language), On-line Reporter III, BNA (Burroughs Network Architecture), and Linc II (Logic and Information Network Compiler II).

A wide range of high-level and interpreter languages including APL, Algol, Cobol 74, Fortran 77, Pascal, PL/1, and RPG II are supported.

PRICING: The basic A 5 uniprocessor system with 6 megabytes of main memory is priced at $224,000. No other pricing information could be obtained from Burroughs by press date. ■