UNIVERSAL ASSEMBLER VERSION 3.1 FEBRUARY 29, 1980 (IN-HOUSE)


```
COMMAND LINE WAS: SNAP3 PROC14.MLTI,,,PROC144:GBQPLX

INCLUSION A: PROCINC/TXT:DR0
INCLUSION B: PROC14/LIB:DR0.PMACMIC
INCLUSION C: PROC14/LIB:DR0.GMACROZ
INCLUSION D: PROC14/LIB:DR0.PROCEQUS
INCLUSION E: PROC14/LIB:DR0.BDEF1800
INCLUSION F: PROC14/LIB:DR0.MDEF1800
INCLUSION G: PROC14/LIB:DR0.PORTEQUS
INCLUSION H: PROC14/LIB:DR0.PORTASGN
INCLUSION I: PROC14/LIB:DR0.PROCP4
D   20.A                        CAPIVS    EQU       0              INVERTED DISPLAY SCREEN VERSION **NEW**

*** ERRORS: D

PROGRAM NAME: MLTI

PROGRAM ADDRESS BLOCKS:     010000    /ABSOLUTE/  SIZE=000000  (ABS)
                            167400    /SYSIVR/    SIZE=000400  (ABS)
                            170000    /SYSROM/    SIZE=000047  (ABS)
                            006000    /CDOXL/     SIZE=001000  (ABS)
                            000000    /CDOXP/     SIZE=002000  (REL)

EXTERNAL DEFINITIONS:

COMMT     006000    COMMR     006114    RCVMRK    006202    INPUT     006462
PIN       006477    EXADR     006512    EXSTAT    006546    EXDATA    006563
OUTPUT    006600    EXWRITE   006600    EXMOUT    006610    EXCOM3    006634
EXCOM1    006665    EXCOM2    006724    EXCOM4    006724
```

EXTERNAL REFERENCES (UNDEFINED SYMBOLS):

SRVNXT FETCHI FETCH FETCHW SCLSTW IVIOL$ MEMPF$

UNUSED LABELS:

PSWND

```
1.
2.          . 2.14.I  HJS     82 AUG  7     CONVERSION TO NEW MULTI-PORT CODE
3.          . 2.14.G  HJS     80 FEB  26    LAST BUG FOUND (I HOPE) - SET RINGING
4.          . 2.14.F  HJS     80 JAN  16    CONVERT TO FINAL SYSTEM
5.          . 2.14.E  HJS     79 OCT  16    SETUP FOR FIRST TEST RUN
6.          . 2.14.D  HJS     79 AUG  30    START TO ADD USER INST. INTERFACE
7.          . 2.14.C  HJS     79 AUG  20    SELECT SECOND GENERATION CODE
8.          . 2.14.B  HJS     79 AUG  14    TRY SECOND GENERATION TRANSMITTER
9.          . 2.14.A  HJS     79 JULY 31    START GENERATION OF IMA
10.         .                               INTERNAL MULTIPORT ADAPTER
11.         .                               (INTERNAL RIM ALSO USES 2.14.A TO G)
12.         *
13.                   INC     PROCINC
```

```
14.A                    SNAPOPT   X
15.A                * TYPE  EQU       4              DEFINE VERSION OF MACHINE TO BE ASSEMBLED
16.A                    INC       PROC14.PORTASGN    PORT ASSIGNMENT DISPLAY
```

```
. THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS

*
.PORT
.    SUB   0       1       2       3       4       5       6       7
.
. 0     0 LIREG   LIMP            BASW    MODW    STW     LUF     LUCF
.     0 I MODIN                             INBUS   MIFIN   SDLCIN  ACUIN
.
. 0     0 IIMP    DIMP    COMF    CHUF    IMAR    DMAR
.    10 I
.
. 1     0 OTBUS   MDW     LSPKR   SDLCOT  ACUOT   SDLCMD  MIFADR  MIFDAT
.     0 I SRVREQ  STATUS          IDCODL  IDCODH  UCFLG   MDR     STEK
.
. 1     0 MIFSTB  MIFIAK  MIFSTB2 SINS    SIOD    CSRF    CSTF    SOTS
.    10 I
.
. 2     0 LDCH    LDMAP   SKCH    SDLM    KBSC    RDLM    CMPF    SMR
.     0 I KBDD    SNID
.
. 3     0 URFO
.       I
.
. 4     0 URO (MR2XXL)
.       I MARIL
.
. 5     0 URO (MR2XXH)
.       I MARIH
.
. 6     0 MAROL (XX2MRL)
.       I URI
.
. 7     0 MAROH (XX2MRH)
.       I URI
.
.
. USER IO PORTS 4-7
. REGS  0 URA     URB     URC     URD     URE     URH     URL     URX
.      10 PCH     PCL     SPH     SPL     PSW     I35     I02     IMP
*
.SUBITS    0       1       2       3       4       5       6       7
.
.SRVREQ:   SCPMEM  SCMBUS  SCSDLCR SCSDLCT SCDSPNL SCONMS  SCHUMS
.
.STATUS:   STUSCF  STIODR  STPFIN  STPFOU  STKBKC  STKBNS  STKBRDY STBOILN
.
.MODW:     SWINTE  SWBASD  SWUSER          SWSTDT  SWRPT           SWALBT
.
.STEK:     STLA                                                   STLW    STLSP
.
```

```
                        . THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS

 52.H                   *
 53.H                   . JUMP INPUT CONDITION CODES ARE:
 54.H                   .
 55.H                   .SELECT    0       1       2       3       4       5       6       7
 56.H                   .
 57.H                   .         CARRY   ZERO    MEMRDY  PARITY  IMPZERO IMPODD  BUSRDY  TRUE
 58.H                   .
 59.H                   *
 60.H                   . DOUBLY NAMED (SUB)PORTS ARE:
 61.H                   .
 62.H                   .         UR0     <>  MR2XXL
 63.H                   .         UR0     <>  MR2XXH
 64.H                   .         MAROL   <>  XX2MRL
 65.H                   .         MAROH   <>  XX2MRH
 66.H                   .
 17.A                     INC       PROC14.PROCP4     INDIRECT TO PARAMETER FILE
  1.I 000002            VER       EQU       2         1800 - INFO INSTRUCTION PROCESSOR NUMBER
  2.I 000014            REV       EQU       014       INFO INST. MICRO-CODE REVISION NUMBER
  3.I                   .
  4.I 000004            TYPE      EQU       4         =0 FOR 1800 PROCESSOR (DISK, ICA)
  5.I                   .                             =1 FOR 1871 PROCESSOR (DISK, ICA, APF/AML)
  6.I                   .                             =2 FOR 3800 PROCESSOR (ICA)
  7.I                   .                             =3 FOR 3802 PROCESSOR (RIM)
  8.I                   .                             =4 FOR 38MP PROCESSOR (IMA)
  9.I                   *
 10.I                     SNAPOPT   X
 11.I                   *
```

```
14.I                    *
15.I                    . CONDITION CODES
16.I                    .
17.I 020002             MO          EQU     F6+2            MEMORY READY
18.I 020003             MP          EQU     F6+3            MEMORY FAILURE (OF ANY SORT!)
19.I 020004             IZ          EQU     F6+4            IMPLICIT REGISTER ZERO
20.I 020005             IO          EQU     F6+5            IMPLICIT REGISTER ODD
21.I 020006             BR          EQU     F6+6            BUS READY (MICRO-BUS ONLY)
22.I                    *
23.I                    . REGISTER ALLOCATION
24.I                    .
25.I 010002             Q           EQU     F5+02           NOBODY SHOULD DO WRITE'S TO Q
26.I                    .
27.I 010000             PDLNP       EQU     F5+0            DISPLAY LINE POINTER
28.I 010001             KBSCNT      EQU     F5+01           KEYBOARD SCAN COUNTER
29.I 010002             SCANSV      EQU     F5+02           KEYBOARD SAVED SCAN NUMBER, REPEATED AI
30.I                    *
31.I                    . DISKETTE CONTROL REGISTERS
32.I                    .
33.I 010003             MADR        EQU     F5+03           DISKETTE DEVICE ADDRESS
34.I 010004             MBITS       EQU     F5+04           DISKETTE I/O CONTROL, FUNCTION & STATUS
35.I 010005             MBSTAT      EQU     F5+05           DISKETTE STATE CONTROL LINK REGISTER
36.I 010006             MCRCH       EQU     F5+06           DISKETTE CRC GENERATOR STORAGE REG.
37.I 010007             MCRCL       EQU     F5+07           DISKETTE CRC GENERATOR STORAGE REG.
38.I 010010             MDSKS       EQU     F5+010          DISKETTE HEADER READ SECTOR NUMBER
39.I 010011             MDSKT       EQU     F5+011          DISKETTE HEADER READ TRACK NUMBER
40.I 010012             MTRAK       EQU     F5+012          DISKETTE USER DESIRED TRACK NUMBER
41.I 010013             MSECT       EQU     F5+013          DISKETTE USER DESIRED SECTOR NUMBER
42.I                    .                                   * APF VERSION ABOVE 2 BYTES IN MEMORY *
43.I                    *
44.I                    . HONEYWELL-APF DMA CHANNEL CONTROL REGISTERS
45.I                    .
46.I 010013             APFRP       EQU     F5+013          APF RECEIVER POINTER LSB
47.I 010014             APFRK       EQU     F5+014          APF RECEIVER COUNTER LSB
48.I 010015             APFTP       EQU     F5+015          APF TRANSMITTER POINTER LSB
49.I 010016             APFTK       EQU     F5+016          APF TRANSMITTER COUNTER LSB
50.I                    *
51.I                    . AUDIO CHANNEL CONTROL REGISTER
52.I                    .
53.I 010015             ACD         EQU     F5+015          AUDIO CHANNEL ATTEN/VALUE
54.I 010016             ACPL        EQU     F5+016
55.I 010017             ACPH        EQU     F5+017          AUDIO CHANNEL CONTROL & MSB POINTER
56.I 010017             ACCTL       EQU     ACPH            APF - AUDIO CHANNEL 1 BYTE CONTROL
57.I                    .                                   (ACPH & ACCTL SHOULD BE SAME REG.)
```

```
58.I                    *
59.I                    . TEMPORARIES - AVAILABLE IN ANY ROUTINE, LOST BETWEEN ROUTINES
60.I                    .
61.I 030000             LINK      EQU     F5+F6+00          SUBROUTINE CALL AND RETURN LINKAGE REGS
62.I 030001             TEMP1     EQU     F5+F6+01          PROCESSOR EMULATION TEMPORARIES
63.I 030002             TEMP2     EQU     F5+F6+02
64.I 030001             TEMPH     EQU     TEMP1             H & L ONLY FOR DOUBLE H/L MACROS
65.I 030002             TEMPL     EQU     TEMP2
66.I                    *
67.I                    . COMMUNICATIONS CHANNEL CONTROL REGISTERS
68.I                    .
69.I 030003             RSTAT     EQU     F5+F6+03          COM RECEIVER STATUS
70.I 030004             RPNTR     EQU     F5+F6+04          COM RECEIVER MEMORY POINTER
71.I 030005             RDATA     EQU     F5+F6+05          COM RECEIVER DATA
72.I 030006             RCRCH     EQU     F5+F6+06          COM RECEIVER CRC GENERATOR STORAGE AREA
73.I 030007             RCRCL     EQU     F5+F6+07          COM RECEIVER CRC GENERATOR STORAGE AREA
74.I 030010             UXPNTR    EQU     F5+F6+010         USER TRANSMIT BUFFER POINTER
75.I 030011             COMMODE   EQU     F5+F6+011         COMMUNICATION MODE CONTROL REGISTER
76.I 030012             URPNTR    EQU     F5+F6+012         USER RECEIVE BUFFER POINTER
77.I 030013             XSTAT     EQU     F5+F6+013         COM TRANSMITTER STATUS
78.I 030014             XPNTR     EQU     F5+F6+014         COM TRANSMITTER MEMORY POINTER
79.I 030015             XDATA     EQU     F5+F6+015         COM TRANSMITTER DATA
80.I 030016             XCRCH     EQU     F5+F6+016         COM TRANSMITTER CRC GENERATOR STORAGE
81.I 030017             XCRCL     EQU     F5+F6+017         COM TRANSMITTER CRC GENERATOR STORAGE
82.I                    *
83.I                    . INTERNAL MULTI-PORT ADAPTER CONTROL REGISTER
84.I                    .
85.I                    .COMMODE  EQU     F5+F6+011!!!      COMMUNICATIONS MODE
86.I 010013             TRNFCN    EQU     F5+013            TX CONTROL LINE SHADOW
87.I 030003             TRNCHN    EQU     F5+F6+03          TRANSMITTING CHANNEL NUMBER
88.I 030004             TRNDTA    EQU     F5+F6+04          TRANSMITTING CHANNEL DATA
89.I 030005             TRNCTL    EQU     F5+F6+05          TRANSMITTING CHANNEL CONTROL
90.I 030006             TRNSEL    EQU     F5+F6+06          TRANSMITTING CHANNEL SELECTION
91.I 030007             RCVCTL    EQU     F5+F6+07          RECEIVER CONTROL REGISTER
92.I 030010             RCH0C     EQU     F5+F6+010
93.I 010014             RCH0D     EQU     F5+014            SWAP OUT WITH COMMODE
94.I 030012             RCH1C     EQU     F5+F6+012
95.I 030013             RCH1D     EQU     F5+F6+013
96.I 030014             RCH2C     EQU     F5+F6+014         RECEIVER CHANNEL & DATA REGISTERS
97.I 030015             RCH2D     EQU     F5+F6+015
98.I 030016             RCH3C     EQU     F5+F6+016
99.I 030017             RCH3D     EQU     F5+F6+017
```

. EXTENDED CONDITIONS, AND SYSTEM REGISTER DEFINITIONS

```
                *
                . CAPABILITY BITS:
                .    THESE BITS DEFINE THE VERSION OF THE 1800/3800 PROCESSOR THAT THIS IS FOR
                .
                .    XX XXX XXX
                .              0 --- MICRO I/O BUS AVAILABLE
                .             1 ---- 1500 SINGLE DENSITY DISKETTE DRIVE AVAILABLE
                .            2 ----- 1800 SINGLE/DOUBLE DISKETTE DRIVE AVAILABLE
                .          3 ------- APF SPECIAL MICRO-BUS INTERFACE AVAILABLE
                .         4 -------- INTERNAL MULTIPORT ADAPTER AVAILABLE
                .        5 --------- INBOARD RIM AVAILABLE
                .      6 ----------- 5500 I/O BUS AVALIABLE
                .    7 ------------ COMMUNICATIONS INTERFACE AVAILABLE (ASYNC, BISYNC, & SDLC)
                .
                . *PROCESSOR*                          1800 1871 3800 3802 38MP
000000          CAPMICR   EQU     0<0                   YES  YES
000002          CAPIMA    EQU     1<1                                      YES
000000          CAPBLUE   EQU     0<2                   YES  YES
000000          CAPAPF    EQU     0<3                        YES
000000          CAPDMPIO  EQU     0<4                                 YES
000000          CAPRIM    EQU     0<5                                 YES
000100          CAP55IO   EQU     1<6                   YES  YES  YES       YES
000000          CAPCOM    EQU     0<7                   YES  YES  YES
                . *TYPE*                               0    1    2    3    4
                .
000102          CAPABILI  EQU   CAPCOM+CAP55IO+CAPRIM+CAPDMPIO+CAPAPF+CAPBLUE+CAPIMA+CAPMICR
                *
                . LOCATION OF THE CODE IN ROMS IS A FOLLOWS   (MSB & LSB OF COURSE)
                .
000000          PROC      EQU     00<9          EMULATION SUPPORT CODE IN ROMS 0 & 1
002000          PROD      EQU     02<9          EMULATION SUPPORT CODE IN ROMS 2 & 3
004000          FLEX      EQU     04<9          MICRO-BUS CODE IN ROMS 4 & 5
006000          CDOX      EQU     06<9          COMM TRANSMIT CODE IN ROM 6
007000          CDOR      EQU     07<9          COMM RECEIVE CODE IN ROM 7
                .
000000          CAPIVS    EQU     0
000111          PRE       EQU     'I'           RELEASE LEVEL (FINAL IS BINARY ZERO)
                *
D 000000        CAPIVS    EQU     0             INVERTED DISPLAY SCREEN VERSION **NEW**
                *                               0 = NORMAL, 1 = INVERTED (PURE RASTER!)
```

```
                        . INTERNAL MULTI-PORT ADAPTER CONTROL DEFINITIONS

                        *
000151                  IMAADR    EQU     0151            ADDRESS OF THE 9462 BEING REPLACED
                        *
                        . CPU DATA          LOGICAL         "1"         "0"
                        . RS232C/RS363      DEFINES         MARK, -VE   SPACE, +VE
                        . TRANSMITTER       (4800 BAUD)     MARK        SPACE
                        . RECEIVER!!!!      ( 300 BAUD)     SPACE, TO   MARK, FC
                        . ** NOTE: RECEIVER INVERSION **    (ACUIN LINES INVERTED ON INPUT!)
                        *
                        . RECEIVER TRANSITION (x) & SAMPLE (V) POINTS
                        .      ...x= = = =V= = = =x= = = =V= = = =x= = = =V= = = =x= = = =V= = = =x...
                        . CLOCK:  0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
                        .         I-------I DELTA/2               I---DELTA = 8---I

000010                  DELTA     EQU     8               DELAY COUNT SAMPLE INTERVAL
000140                  TCOUNT    EQU     16-8-2<4        8 DATA & 2 STOP BITS IN THE 4 BIT COUNTER
                        *
                        . CONTROL REGISTERS INTERNAL DEFINITIONS:
                        . RCVCTL            3'2'1'0'3 2 1 0 0..3 RECEIVER READY (WIH DATA)
                        .                                   0'..3'  RECEIVER ERROR BITS (BREAK!)
                        . TRNCTL            Z Z Z Z 3 2 1 0 0..3 TRANSMITTER READY STATUS
                        .                                   ZZZZ ALWAYS ZERO
                        . TRNSEL            K K K K 3 2 1 0 0..3 TRANSMITTER PORT SELECTED FOR OUTPUT
                        .                                   KKKK COUNTER OF BITS GOING OUT
                        . TRNCHN            Z Z Z Z 3 2 1 0 0..3 TRANSMITTER CHANNEL DATA (SPACE/MARK)
                        . TRNDTA & RCHXD    D D D D D D D D DATA BEING SHIFTED OUT AND IN
                        . RCHXC               ^ U U U U U U U U MICRO-ADDRESS FOR RECEIVER CONTROL
                        .   ^X^  &   ^X^                    X VARIES FROM 0 TO 3 (PER CHANNEL REGS)
                        . TRNCTL & TRNCHN                   NOTE: ONLY 1 BIT MAY BE SET (1 CHANNEL)
                        . TRNFCN            A X X 2 3 X 1 0 0..3 TRANSMITTER DTR
                        .                                   A = 1 WHEN MULTIPORT COMES ALIVE

                        . COMMODE           Z Z E X 3 2 1 0 Z    ALWAYS ZERO  ** ONLY 1 BIT MAY BE 1**
000040                  COMMNPS   EQU       B5              E    DEVICE ADDRESSED NO PORT SELECTED YET
000020                  COMMNXP   EQU       B4              X    EXTRA (NON-PORT) 4-7 SELECTED
000017                  COMMPTS   EQU       B3+B2+B1+B0     3..0 EX ADR & EX COM3 SELECTED PORT
                        *
                        . INTERNAL MULTIPORT ALLOCATION OF COMMAND STROBES ON AVAILABLE CONTROL BITS
                        .
                        . ACUIN             0 0 5 4 3 2 1 0 3..0 RECEIVER DATA FOR CHANNEL 3..0
                        .                                   4    RECEIVER 2 CLEAR TO SEND (DSR/CD...)
                        .                                   5    RECEIVER 3 CLEAR TO SEND (DSR/CD...)
                        . MODIN             0 6 1 4 1 0 0 0 1'S  MASTER CD & CTS MUST BE ONE'S
                        .                                   4    RECEIVER 0 CLEAR TO SEND (DSR/CD...)
                        .                                   6    RECEIVER 1 CLEAR TO SEND (DSR/CD...)
                        . MODOUT            X X X 0 3 X 1 1 1'S  MASTER DTR & RTS MUST BE ONE'S
                        .                                   3    (NEW SYNC) CAN BE ANYTHING
                        .                                   0    MASTER SET BRAKE MUST BE ZERO
                        . ACUOT             X X 5 4 3 2 1 0 3..0 TRANSMITTER OUTPUT FOR CHANNEL 3..0
                        .                                   4    (DIGIT PRESENT = 0)
                        .                                   5    (CALL REQUEST = 0)
                        . SDLCIN            ? ? ? ? ? ? ? 0 0    MASTER RECEIVE DATA (IGNORED)
```

```
                        . INTERNAL MULTI-PORT ADAPTER CONTROL DEFINITIONS

                        . SDLCOT        X X X X X X X 0   0    MASTER TRANS. (MATCHES CHANNEL 0)
                        . SDLCMD        X X X 2 3 X 1 0   3..0 DTR FOR CHANNELS 3..0

000350                  IMASTS  EQU     B7+B6+B5+B3       DSR(7) & CD(6) & RD(5) & CTS(3) FOR 9462
                        *
                                MACRO                     1450 NSEC
                                RECEIVE CHN
                                BAL     LINK,RCHICHNIEND  SET RETURN ADDRESSS FOR ROUTINE CALL
                                LDRI    TEMP2,CHN         SET CHANNEL NUMBER FOR THE ROUTINE
                                LDRR    TEMP1,RCHICHNID,CC LOAD CHANNEL DATA FOR CHANNEL IN USE
                                DOTPI   ,ND,ACUIN,1<CHN   GET CHANNEL'S MARK/SPACE BIT
                                DOTI    ,AC,0377          SET CARRY ON MARK!
                                BRR     RCHICHNIC         GO TO THE CONTROL ROUTINE
                        RCHICHNIEND BAS RCHICHNIC         SAVE THE STATE FOR NEXT TIME
                                LDRR    RCHICHNID,TEMP1   SAVE THE NEW DATA TOO
                                MEND

                                MACRO                     850 NSEC WORST CASE
                                BIT2ADR ADDRESS
                                TSTIT   ,014
                                BRA     BITOK,TZ          WAS 0001(1) OR 0010(2) - LEAVE AS IS
                                DOTI    ,SB,1
                                TSTIT   ,014
                                BRA     BITOK,TZ          WAS 0100 - CHANGED TO 0011(3)
                                LDTI    4                 WAS 1000 - CHANGED TO 0100(4)
                        BITOK   DOPI    MAROL,AC,ADDRESS  NOW INDEX INTO MEMORY BY BIT POSITION
                                MEND
```

```
 98.                                    *
 99.  006000                            CDOXL   ORG     CDOX
100.  000000                            CDOXP   ORG     0
101.  006000                            CDOXL   USE     CDOXL
102.  000000                                    USE     CDOXP
103.  006000L                           CDOXP   LOC     CDOXL,2
104.                                    *
105.  006000L                           COMMT:                          !!ALL TIMINGS WORST CASE !!
106.                                    . 400
107.  006000L 01110001 10110110                 LDTR    TRNSEL,CC       CHANNELS ALIVE?
108.  006001L 11000011 11000101                BRA     SENANY,TZ       IF NONE, TRY SOME
109.  006002L 01000101 11110000                TSTIT   ,0360           AT THE START?
110.  006003L 11000010 11100000                BRA     SENDTA,FZ       NO, JUST DO NEXT DATA BIT
111.                                    . SENSTRT
112.                                    . 2400
113.  006004L 11000100 11111011                MWAIT   ,MEMPF6
      006005L 11010111 00010001
114.                                    .           LDTR    TRNSEL,CC       CONVERT BIT TO NUMBER
115.  006006L 01000101 00001100                BIT2ADR SVCTRN-1        GET TRANSMITTER DATA BYTE (ORIGIN 1 FIX)
      006007L 11000011 11110011
      006010L 01010100 00000001
      006011L 01000101 00001100
      006012L 11000011 11110011
      006013L 01010001 00000100
      006014L 01010010 01010111
      006015L 00110111 11000000
116.  006016L 01010001 11101111 LDPI    MAROH,SVCTRN>8   MSB OF DATA ADDRESS
      006017L 00110111 11100000
117.  006020L 00110001 11011100 DOPIP   MODW,ND,-1-SWUSER,PSWI
      006021L 01010101 11111011
      006022L 00110111 00000100
118.  006023L 00110111 01000111 STB     SMR
119.  006024L 01110001 10110110 DORIR   TRNSEL,OR,TCOUNT,TRNSEL,CC   INIT COUNTER WITH 2 STOP BITS
      006025L 01010011 01100000
      006026L 01101111 11110110
120.  006027L 01010101 00001111 DOTI    ,ND,017
121.  006030L 01010000 11111111 DOTI    ,XR,0377        HAVE 1 1 1 1 X X X X (ONLY ONE "X" IS A 0)
122.  006031L 01110101 11110101 DORR    TRNCTL,ND,TRNCTL TO TURN OFF BIT FOR CHANNEL TRANSMITTING
      006032L 01101111 11110101
123.  006033L 11000100 11100100 MWAIT   ,MEMPF6
      006034L 11010111 00010001
124.  006035L 00110001 00110110 LDRP    TRNDTA,MDR      GET DATA & OUTPUT ITS FIRST BIT
      006036L 01101111 11110100
```

```
                                . INTERNAL MULTI-PORT ADAPTER RECEIVER/TRANSMITTER CHANNEL OPERATING CODE

  125.                          *
  126.  006037L                 SENDTA
  127.                          . 800
  128.  006037L 01010001 00000001          LDTI    1                   SET LINK TO SHIFT IN 1
  129.  006040L 01110001 10110100          LDTR    TRNDTA,CC           FOR THE TWO STOP BITS
  130.  006041L 00010111 10010010          SHIFT   SR                  SHIFT NEXT DATA BIT TO LINK
  131.  006042L 01101111 11110100          LDRT    TRNDTA
  132.  006043L 00010111 10010010          SHIFT   SR
  133.  006044L 01010101 10000000          TSTIT   ,0200,,,TW          MARK OR SPACE?
  134.  006045L 11000010 110.11000          BRA     SENMARK,FZ          ON MARK: T-REG = 0200; ON SPACE: T = 0
  135.  006046L 01110001 11110110          LDTR    TRNSEL              SEND A SPACE (ONE CHANNEL ONLY!)
  136.  006047L                 SENMARK                                 SENDING A MARK (T MUST BE CORRECT, ZERO!)
  137.                          * *RE-DO SO THAT:
  138.                          . IF ANY "OTHER" CHANNEL IS AVAILABLE FOR TRANSMISSION, SWITCH
  139.                          . TO IT BEFORE SENDING STOP BITS ON PRESENT CHANNEL.
  140.                          . THIS WILL ENABLE HIGHER EFFECTIVE SPEED BY HIDING BOTH STOP BITS
  141.                          . BEHIND ANOTHER CHANNELS DATA TRANSMISSION.
  142.                          . 900
  143.  006047L 01010011 00110000          DOTI    ,OR,B5+B4           SET COMM ALIVE BITS
  144.  006050L 01010000 00001111          DORI    TRNCHN,XR,017       SAVE CHANNEL BITS FOR NEXT INTERRUPT
        006051L 01101111 11110011
  145.  006052L 01110001 10110110          DORIR   TRNSEL,AC,1<4,TRNSEL,CC
        006053L 01010010 00010000
        006054L 01101111 11110110
 >146. >006055L 01011001 11111111          BRAX    SRVNXT,FC           CONTINUE TILL COUNTER OVERFLOWS
       >006056L 11000000 11111111
  147.  006057L 01011001 11110011          BPGX    $                   REACHED THE END, DO THE NEXT
  148.                          *
  149.                          . SENEXT
  150.                          .
  151.                          . FIND NEXT FREE CHANNEL TO GET DATA FROM
  152.                          . SEARCH IS DONE IN A ROUND ROBIN FASHION
  153.                          . 400
  154.  006060L 01110001 11110110          LDRR    TEMP1,TRNSEL        SET STARTING TEST POINT
        006061L 01101111 11110001
  155.  006062L 01110001 11110101 SENTRY    LDTR    TRNCTL              (SPEEDUP IF NOTHING TO DO)
  156.  006063L 11000011 10111001          BRA     SENEND,TZ           YES, I HAVE NO BANANAS
  157.                          .
  158.                          . NOTE: IN THE FOLLOWING REPEATS THERE ARE ONLY "3" TOTAL NOT 4.
  159.                          . THIS IS SO THAT THE TRAILING MARK OF A CHANNEL JUST COMPLETED
  160.                          . CAN OVERLAP THE LEADING SPACE OF THE NEXT CHANNEL.
  161.                          . WHY THREE? BECAUSE IT CAN NOT OVERLAP ITSELF!
  162.                          . THIS WILL INSURE TWO FULL STOP BITS BEFORE THE START BIT OF
  163.                          . THE SAME CHANNEL BEING FINISHED & SELECTED AS NEXT.
  164.                          . TCOUNT MUST BE SET CORRECTLY TO DO THIS!  ** NOT SO AT PRESENT **
  165.                          . 2*1300+1300+600
  166.                                  RPT     (4-1)-1             4-1 PORTS IN ROUND ROBIN
  167.  006064L 01010001 11001001          BRC     CHKNXT
        006065L 11001111 11000010
  167.  006066L 01010001 11000111          BRC     CHKNXT
        006067L 11001111 11000010
  168.  006070L 01010001 10111001          BRC     CHKNXT,,SENEND      LEAVE MARKING IF NO AVALABLE DATA FOUND
```

```
        006071L 11001111 11000010
   169.
   170. 006072L 01010001 11001101   *
        006073L 01101111 11110000   SENANY   BRS     CHKANY,,SENTRY   DO FOUR STEPS IF QUIET BEFOREHAND
        006074L 11001111 10111101
   171.                             . 400+500
   172.                             *
   173. 006075L                     CHKNXT
   174.                             .
   175.                             . CHECK IF CHANNEL AS SPECIFIED BY TEMP1 CONTAINS DATA TO BE OUTPUT
   176.                             .
   177. 006075L 01101111 11110000           BAS     LINK             SAVE RETURN ADDRESS
   178. 006076L 01110001 11110001           LDTR    TEMP1
   179. 006077L 00010111 10100010           SHIFT   SL               CHECK THE NEXT CHANNEL IN SEQUENCE
   180. 006100L 01010101 00001110           DOTI    ,ND,07<1         HIGH BITS SHIFT IN ZERO
   181. 006101L 11000010 10111100           BRA     CHKCHN,FZ
   182. 006102L 01010001 00000001   CHKANY  LDTI    1<0              TRY CHANNEL 0 AFTER 3
   183. 006103L 01101111 11110001   CHKCHN  LDRT    TEMP1            SAVE CHANNEL MARKER
   184. 006104L 01110101 11110101           DOTR    ,ND,TRNCTL       IS THERE DATA? (T = 0 FOR LAST BRC)
   185. 006105L 11100011 00000000           BRR     LINK,TZ          NOT ON THIS ONE
   186. 006106L 01101111 11110110   SENEND  LDRT    TRNSEL           SAVE SELECTED CHANNEL'S BIT MARKER
   187. 006107L 01010011 00110000           DOTI    ,OR,B5+B4        SET COMM ALIVE BITS
   188. 006110L 01010000 00001111           DORI    TRNCHN,XR,017    SEND THE LEADING SPACE (OR MORE MARKS!)
        006111L 01101111 11110011
   189. >006112L 01011001 11111111          BRAX    SRVNXT
        >006113L 11001111 11111111
   190.                             .
   191.                             . TRANSMITTER TIMINGS RESULTS:
   192.                             .        NOTHING TO DO          1700
   193.                             .        AVERAGE PER BIT        2200
   194.                             .        FIRST BIT SPECIAL      5200
   195.                             .        LAST BIT WORST CASE    7200  (SAME CHANNEL READY BUT NO OTHERS)
```

. INTERNAL MULTI-PORT ADAPTER RECEIVER/TRANSMITTER CHANNEL OPERATING CODE

```
196.                                    +
197.  006114L                          COMMR:
198.                                    .
199.                                    . RECEIVER TIMINGS RESULTS:
200.                                    .       4*1450+300+4*3100 = 18500 NSEC
201.                                    .       4 CHANNELS TO BE EXAMINED
202.                                    .       300 NS RETRUN TO SERVICE REQUEST CONTROL
203.                                    .       4 CHANNELS WORST CASE (ALL FINISHED CHARACTER AT SAME TIME)
204.                                    .
205.                                    . AVERAGE CASE: 4*(1450+300)+300  ALL CHANNELS DOING BRRC DELAY COUNTING
206.                                    .
207.  006114L 01010001 10101001  LDTI  Φ251      RECEIVE  0          RECEIVE CHANNEL 0
      006115L 01101111 11110000  BAS   LINK
      006116L 01010001 00000000  LDTI  Φ                            LINK    Φ
      006117L 01101111 11110010  LDRT  TEMP2                        TEMP2   02
      006120L 00010001 10111100  LDTR  RCHΦD,3CC                    RCHΦD   14
      006121L 01101111 10110001  LDRT  TEMP1,CC                     TEMP1   1
      006122L 01010001 00000001  LDTI  1                            RCH0C   1Φ
      006123L 00110101 00010111  DOTP  ,ND, ACWIN                   RCH1D   13
      006124L 01010010 11111111  DOTI  ,AC, Φ377                    RCH1C   12
      006125L 11101111 00001000  BRR   ACHΦC
      006126L 01101111 11111000  LDRT  ACH ΦC
      006127L 01110001 11110001  LDTA  TEMP1
      006130L 00000111 11111100  LINK  RCHΦD
208.  006131L 01010001 10011100  LDTI  234        RECEIVE  1          RECEIVE CHANNEL 1
      006132L 01101111 11110000
      006133L 01010001 00000001  LDTI  1
      006134L 01101111 11110010
      006135L 01110001 10111011  LDTR  RCH1D
      006136L 01101111 10110001
      006137L 01010001 00000010  LDTI  2
      006140L 00110101 00010111
      006141L 01010010 11111111
      006142L 11101111 00001010  BRR   RCH1C
      006143L 01101111 11111010  LDRT  RCH1C
      006144L 01110001 11110001
      006145L 01101111 11111011  LDRT  RCHΦD
209.  006146L 01010001 10001111                RECEIVE  2          RECEIVE CHANNEL 2
      006147L 01101111 11110000
      006150L 01010001 00000010
      006151L 01101111 11110010
      006152L 01110001 10111101
      006153L 01101111 10110001
      006154L 01010001 00000100
      006155L 00110101 00010111
      006156L 01010010 11111111
      006157L 11101111 00001100
      006160L 01101111 11111100
      006161L 01110001 11110001
      006162L 01101111 11111101
210.  006163L 01010001 10000010                RECEIVE  3          RECEIVE CHANNEL 3
      006164L 01101111 11110000
```

. INTERNAL MULTI-PORT ADAPTER RECEIVER/TRANSMITTER CHANNEL OPERATING CODE

```
                006165L 01010001 00000011
                006166L 01101111 11110010
                006167L 01110001 10111111
                006170L 01101111 10110001
                006171L 01010001 00001000
                006172L 00110101 00010111
                006173L 01010010 11111111
                006174L 11101111 00001110
                006175L 01101111 11111110
                006176L 01110001 11110001
                006177L 01101111 11111111
211.  >006200L 01011001 11111111          BRAX    SRVNXT          AND DONE!
      >006201L 11001111 11111111
212.                                      *
213.  006202L                             RCVMRK:                 ** WAITING FOR START (SPACE)
214.  006202L 01010001 01111101 LDTI #175  BRRC    LINK,TC,RCVMRK  JUST WAIT UNTIL SPACE ENDS
      006203L 11100001 00000000 BRR LINK,TC
215.  006204L 01010001 01111011    RCVSPC  BRRC    LINK,FC,RCVSPC  JUST WAIT UNTIL SPACE RESTARTS
      006205L 11100000 00000000 BRR LINK,FC
216.                                      .                       THIS FORCES LEADING EDGE OF SPACE
217.                                      .                       AS CONDITION FOR START BIT
218.                                      .
219.                                          RPT     DELTA/2     ** DELAY TILL EARLY MID BIT WHILE SPACING
220.  006206L 01010001 01110111          0 BRRC    LINK,TC         NEXT STATE ONLY WHILE STILL SPACING
      006207L 11100001 00000000          1 BRRC    LINK,TC
220.  006210L 01010001 01110101          2 BRRC    LINK,TC         NEXT STATE ONLY WHILE STILL SPACING
      006211L 11100001 00000000
220.  006212L 01010001 01110011          3 BRRC    LINK,TC         NEXT STATE ONLY WHILE STILL SPACING
      006213L 11100001 00000000
221.  006214L 01010001 01111101          / BRRC    LINK,FC,RCVMRK  IF MARK, THEN START OVER AGAIN
      006215L 11100000 00000000
222.                                      .
223.                                      .       THE DELTA/2 CYCLE (MID START BIT)
224.  006216L 01010001 10000000              LDRI    TEMP1,0200      INIT REG TO RECEIVE DATA
      006217L 01101111 11110001
225.                                      .                       WHEN 0200 BIT SHIFTS OUT, GOT ALL DATA
226.                                  RCVDATA RPT     DELTA-1         DELAY TILL MID DATA BIT
227.  006220L 01010001 01101101          8 BRRC    LINK
      006221L 11101111 00000000
227.  006222L 01010001 01101011          9 BRRC    LINK
      006223L 11101111 00000000
227.  006224L 01010001 01101001          : BRRC    LINK
      006225L 11101111 00000000
227.  006226L 01010001 01100111          ; BRRC    LINK
      006227L 11101111 00000000
227.  006230L 01010001 01100101          < BRRC    LINK
      006231L 11101111 00000000
227.  006232L 01010001 01100011          = BRRC    LINK
      006233L 11101111 00000000
227.  006234L 01010001 01100001          > BRRC    LINK
      006235L 11101111 00000000
228.                                      .
```

```
                                . INTERNAL MULTI-PORT ADAPTER RECEIVER/TRANSMITTER CHANNEL OPERATING CODE

                                .       THE DELTA CYCLE TO MID DATA BIT
                                .                                       RECEIVED DATA (IN CARRY) PUT IN BIT 0
229.                                    DOTII   ,AC,0,1                 TC = SPACE = "0" -> B0 = 0
230.
231.  006236L 01010001 00000001
      006237L 01010010 00000000
232.                            .                                       FC = MARK  = "1" -> B0 = 1
233.  006240L 01110001 10110001      LDTR    TEMP1,CC                  GET OLD DATA & PUT NEW BIT INTO THE LINK
234.  006241L 00010111 10010010      SHIFT   SR,CC                     SHIFT THE DATA IN (DONE BIT TO LINK?)
235.  006242L 01101111 11110001      LDRT    TEMP1
236.  006243L 00010111 10010010      SHIFT   SR                        GET THE END MARKER BIT (MAYBE?)
237.  006244L 01000010 10000000      TSTIT   AC,0200                   SET CARRY IF REACHED THE END
238.  006245L 01010001 01101111      BRRC    LINK,FC,RCVDATA           NOT YET, KEEP GOING
      006246L 11100000 00000000
239.                            .
240.                                    RPT     DELTA#1                 ** DELAY TILL MID STOP BIT
241.  006247L 01010001 01010110        0 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006250L 11101111 00000000
241.  006251L 01010001 01010100        1 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006252L 11101111 00000000
241.  006253L 01010001 01010010        2 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006254L 11101111 00000000
241.  006255L 01010001 01010000        3 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006256L 11101111 00000000
241.  006257L 01010001 01001110        4 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006260L 11101111 00000000
241.  006261L 01010001 01001100        5 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006262L 11101111 00000000
241.  006263L 01010001 01001010        6 BRRC  LINK                    (RECEIVER ACCEPTS 1 STOP BIT!)
      006264L 11101111 00000000
242.                            *       BRAC    LINK
243.                            .       THE DELTA CYCLE TO MID FIRST STOP BIT
244.                            . 2050
245.  006265L 11000100 00100010        MWAIT   ,MEMPF6
      006266L 11010111 00010001
246.  006267L 00110001 11011100        DOPIP   MODW,ND,-1-SWUSER,PSWI
      006270L 01010101 11111011
      006271L 00110111 00000100
247.  006272L 01010001 11101111        LDPI    MAROH,SVCRCV>8          LOAD ADDRESS OF DATA SAVE AREA
      006273L 00110111 11100000
248.  006274L 01010001 01010100        DOPRI   MAROL,OR,TEMP2,SVCRCV   SELECT BUFFER LOC. (CARRY HELD!)
      006275L 01110011 11110010
      006276L 00110111 11000000
249.  006277L 01110001 11110001        LDPR    MDW,TEMP1               STORE DATA (TEMP1 FREE REG NOW!)
      006300L 00110111 00100001
250.
251.  006301L 01010001 00110100        LDTA    RCVSTB                  SETUP FOR SHIFTS TO BIT POSITION
252.  006302L 01110010 10110010        DORR    TEMP2,AC,TEMP2,,HC      BUT, DO NOT CHANGE CARRY!!
      006303L 01101111 11110010
253.  006304L 01010001 00000001        LDTI    1<0                     MARK = FC, ASSUMED DATA RECEIVED OK
254.  006305L 11000000 00111000        BRA     RCVBRK,FC               (CARRY MUST NOT BE DISTURBED TILL HERE)
255.  006306L 01010001 00010001        LDTI    (1<4)+(1<0)             SPACE = TC, DATA RECEIVED ERROR (BREAK?)
256.  006307L                     RCVBRK
257.                            . 200-500
```

. INTERNAL MULTI-PORT ADAPTER RECEIVER/TRANSMITTER CHANNEL OPERATING CODE

```
 258.  006307L 11101111 00000010          BRR     TEMP2              NOW SHIFT BITS TO CORRECT POSITION
 259.                                     RPT     4-1
 260.  006310L 00010111 10100010          SHIFT   SL
 260.  006311L 00010111 10100010          SHIFT   SL
 260.  006312L 00010111 10100010          SHIFT   SL
 261.  006313L                            RCVSTB                     FOR 0, IN CORRECT POSITION ALREADY
 262.                                     . 700
 263.                                     IFNE    $>8,COMMT>8
 265.                                     XIF
 266.  006313L 01110011 11110111          DORR    RCVCTL,OR,RCVCTL   SET STATUS BITS AS NEEED
       006314L 01101111 11110111
 267.  006315L 11000100 00110010          MWAIT   ,MEMPF6
       006316L 11010111 00010001
 268.  006317L 01010001 01111101          BRRC    LINK,,RCVMRK       ANYWAY, FINISHED A CHARACTER SO START OVER
       006320L 11101111 00000000
```

Noop

Noop

for future Diagnostics.

PAD 2

```
                                *
006321L 01010101 00010000 IMAIN   DOTI   ,ND,SWSTDT        WAS I IN STATUS OR DATA MODE?
006322L 11010010 11101011         BRA    IMARDTA,FZ       DATA INPUT
006323L 01101111 11110001         LDRT   TEMP1            INIT STATUS IS ZERO
006324L 01110001 11111001         TSTIR  ,COMMNPS+COMMNXP,COMMODE
006325L 01000101 00110000
006326L 11000010 00000001         BRA    IMASCOM,FZ       TESTING NON-SELECTED/EXISTANT PORT
006327L 01110101 11000101         TSTRT  ,TRNCTL
006330L 11000010 00100011         BRA    IMASB0,FZ
006331L 01010001 00000001         LDRI   TEMP1,B0         SET TRANSMITTER READY BIT
006332L 01101111 11110001
006333L 01110001 11111001         LDTR   COMMODE             RELOAD PORT SELECT BIT
006334L                   IMASB0
006334L 01110101 11000111         TSTRT  ,RCVCTL
006335L 11000011 00010110         BRA    IMASB1,TZ        RECEIVER NOT READY
                                  RPT    4                GET TO ERROR BIT POSITIONS
006336L 00010111 10100010         SHIFT  SL
006337L 00010111 10100010         SHIFT  SL
006340L 00010111 10100010         SHIFT  SL
006341L 00010111 10100010         SHIFT  SL
006342L 01110101 11110111         DOTR   ,ND,RCVCTL        SEE IF ERROR BIT SET
006343L 11000011 00011010         BRA    IMASB2,TZ
006344L 01010001 00000100         LDTI   B2               YES, INCLUDE IT IN BITS SET
006345L 01010011 00000010 IMASB2  DOTI   ,OR,B1           COMBINE READY WITH (MAYBE) THE ERROR BIT
006346L 01110011 11110001         DORR   TEMP1,OR,TEMP1    SET RECEIVER & BREAK DETECTED BITS AS NEED
006347L 01101111 11110001
006350L 01110001 11111001         LDTR   COMMODE             RELOAD PORT SELECT BIT
006351L                   IMASB1
006351L 01000101 00001100         TSTIT  ,B3+B2            WHICH PORT IS THIS FOR?
006352L 11000010 00001010         BRA    IMASBP32,FZ       PORTS 3 & 2
006353L 01000101 00000010         TSTIT  ,B1
006354L 11000010 00001110         BRA    IMASBP1,FZ
                                  *
006355L 01010001 00010000         TSTPI  ,MODIN,B4         PORT 0 DSR/CD/RD/CTS SET?
006356L 00110101 00010000
006357L 11000010 00000110         BRA    IMASBSTS,FZ       YES
006360L 11001111 00000101         BRA    IMASORZ           NO
006361L 01010001 01000000 IMASBP1 TSTPI  ,MODIN,B6         PORT 1 DSR/CD/RD/CTS SET?
006362L 00110101 00010000
006363L 11000010 00000110         BRA    IMASBSTS,FZ       YES
006364L 11001111 00000101         BRA    IMASORZ           NO
006365L 00010111 10100010 IMASBP32 SHIFT  SL
006366L 00010111 10100010         SHIFT  SL
006367L 00110101 00010111         TSTPT  ,ACUIN            P: 3,2 DSR/CD/RD/CTS SET?
006370L 11000011 00000101         BRA    IMASORZ,TZ        NO
                                  *
006371L 01010001 11101000 IMASBSTS LDTI  IMASTS
006372L 01110011 11110001 IMASORZ DOPR   IMPO,OR,TEMP1     RETURN THE GENERATED STATUS
006373L 00110111 10001111
>006374L 01011001 11111111        BRAX   FETCHI
>006375L 11001111 11111111
```

NOP in its place

```
 312.                                    *
 313.  006376L 01010101 00100000  IMASCOM  DOTI    ,ND,COMMNPS        NO PORT SELECTED?
 314.  006377L 11000011 00000101           BRA     IMASORZ,TZ         NO, WAS TO NON-EXISTANT PORT
 315.  006400L 01010001 00001111           TSTRI   XR,TRNCTL,COMMPTS  ANY AVAIL. PORT WILL BECOME A 1
       006401L 01110000 11000101
 316.  006402L 11010011 11111010           BRA     IMASC0,TZ          IF ANY TRANSMITTER AVAILABLE
 317.  006403L 01010001 00000001           LDRI    TEMP1,B0           SET TRANSMITTER READY BIT
       006404L 01101111 11110001
 318.  006405L                       IMASC0
 319.  006405L 01110001 11110111           LDTR    RCVCTL
 320.  006406L 11010011 11110010           BRA     IMASC1,TZ          NO RECEIVER IS READY
 321.  006407L 01010101 11110000           TSTIT   ,0360,,TW          SEE IF ANY ERROR BIT SET (ZERO T IF NO)
 322.  006410L 11010011 11110101           BRA     IMASC2,TZ
 323.  006411L 01010001 00000100           LDTI    B2                 YES, INCLUDE IT IN BITS SET
 324.  006412L 01010011 00000010  IMASC2    DOTI    ,OR,B1             COMBINE READY WITH (MAYBE) THE ERROR BIT
 325.  006413L 01110011 11110001           DORR    TEMP1,OR,TEMP1     SET RECEIVER & BREAK DETECTED BITS AS NEED
       006414L 01101111 11110001
 326.  006415L                       IMASC1
 327.  006415L 00110001 00010111           TSTIP   ,B5+B4,ACUIN       PORT 3 OR 2 DSR/CD/RD/CTS SET?
       006416L 01000101 00110000
 328.  006417L 11000010 00000110           BRA     IMASBSTS,FZ        YES
 329.  006420L 00110001 00010000           TSTIP   ,B6+B4,MODIN,TW    PORT 1 OR 0 DSR/CD/RD/CTS SET?
       006421L 01010101 01010000
 330.  006422L 11000010 00000110           BRA     IMASBSTS,FZ        YES
 331.  006423L 11001111 00000101           BRA     IMASORZ            NO
 332.                                    *
 333.  006424L                       IMARDTA
 334.                                    .
 335.  006424L 01010001 11101111           LDPI    MAROH,SVCRCV>8     ACCESS RECEIVER DATA (BUFFERED)
       006425L 00110111 11100000
 336.  006426L 01110001 10111001           TSTIR   ,COMMPTS,COMMODE,CC,TW
       006427L 01010101 00001111
 337.  006430L 11010011 11010000           BRA     IMRNXP,TZ          NOT A REAL PORT (SO ZERO)
 338.  006431L 01110001 11111001           LDTR    COMMODE
 339.  006432L 01000101 00001100           BIT2ADR SVCRCV-1
       006433L 11010011 11011111
       006434L 01010100 00000001
       006435L 01000101 00001100
       006436L 11010011 11011111
       006437L 01010001 00000100
       006440L 01010010 01010011
       006441L 00110111 11000000
 340.  006442L 00110111 01000111           STB     SMR
 341.  006443L 01110001 11111001           LDTR    COMMODE
 342.                                      RPT     4                  SELECT NECESSARY CONTROL BITS
 343.  006444L 00010111 10100010           SHIFT   SL
 343.  006445L 00010111 10100010           SHIFT   SL
 343.  006446L 00010111 10100010           SHIFT   SL
 343.  006447L 00010111 10100010           SHIFT   SL
 344.  006450L 01110011 11111001           DOTR    ,OR,COMMODE        THE RECEIVED & ERROR BITS
 345.  006451L 01010000 11111111           DOTI    ,XR,0377
 346.  006452L 01110101 11110111           DORR    RCVCTL,ND,RCVCTL   CLEAR PREVIOUS STATUS
```

```
        006453L 01101111 11110111
347.    006454L 11010100 11010011          MWAIT   ,MEMPF6
        006455L 11010111 00010001
348.    006456L 00110001 00110110          LDTP    MDR             AND GET THE RECEIVED DATA
349.    006457L 00110111 10001111  IMRNXP   LDPT    IMPO
350.  >006460L 01011001 11111111            BRAX    FETCH
      >006461L 11001111 11111111
351.                               *
```

```
                                *
                                INPUT:
                                . 3.70   (    101)  IN              INPUT FROM 5500 BUS
                                . 3.70   (IMP 101)  INR             (R) <- INBUS
                                . ******
                                . NOTE:  INSTRUCTION FETCH TIME (APPROX. 2 MICRO-SEC.) INCLUDED IN COUNT FOR
                                .        TOTAL OF 5 MICRO-SEC. I/O TIMING OF THE INSTRUCTION.
                                . ******

006462L 00110001 11011100                TSTIP   ,SWUSER,PSWI
006463L 01000101 00000100
006464L 11010010 00010011                BRA     IVIOL6,FZ          CONTINUE ONLY IF IN PRIVED MODE
006465L 01000101 00001000                TSTIT   ,SWIDEV
006466L 11000010 00101110                BRA     IMAIN,FZ
006467L 00110001 00010100  INPUTX        LDPP    SINS,INBUS,IMPO    GET INPUT DATA AND FAST ACKNOWLEDGE
006470L 00110111 00101011
006471L 00110111 10001111
006472L 00110001 00110001  INPW1        TSTIP   ,STIODR,STATUS
006473L 01000101 00000010
006474L 11010011 11000101                BRA     INPW1,TZ           WAIT FOR ACK. TO MAKE ITSELF KNOWN
>006475L 01011001 11111111  FTCHIO      BRAX    FETCHW             'W' BECAUSE I/O DELAY TIMING NEEDS IT
>006476L 11001111 11111111
                                .                                   AS WELL AS EX ADR AND MIN MEMORY WRITES
                                *
006477L                         PIN:
                                . 4.15   (    103)  PIN             PARITY CHECKING INPUT
                                . 4.15   (IMP 103)  PINR            (R) <- INBUS; PARITY CHECK
                                . ******
                                . NOTE:  INSTRUCTION FETCH TIME (APPROX. 2 MICRO-SEC. INCLUDED IN COUNT FOR
                                .        TOTAL OF 5 MICRO-SEC. I/O TIMING OF THE INSTRUCTION.
                                . ******

006477L 00110001 11011100                TSTIP   ,SWUSER,PSWI
006500L 01000101 00000100
006501L 11010010 00010011                BRA     IVIOL6,FZ          DON'T CONTINUE UNLESS PRIVED
006502L 01000101 00001000                TSTIT   ,SWIDEV
006503L 11010010 10111000                BRA     PINERR,FZ          PIN'S GIVE PARITY FAULT ON 9462
006504L 00110001 00110001                TSTIP   ,STPFIN,STATUS
006505L 01000101 00000100
006506L 11010011 11001000                BRA     INPUTX,TZ          NO PARITY FAULT, CONTINUE REGULAR INPUT
006507L 01010001 00000110  PINERR        LDTI    SVINP              USE PARITY INPUT ERROR VECTOR
>006510L 01011001 11111111               BRAX    SCLSTW             AND CALL SUPERVISOR ERROR ROUTINE
>006511L 11001111 11111111
                                .                                   PC CORRECT OR BACK UP IF IMP NON-ZERO
```

```
390.                                    +
391.  006512L                          EXADR:
392.
393.                                    . 9.40   (    121)  EX ADR          SELECT DEVICE (AND PUT IN STATUS MODE)
394.                                    . 9.40   (IMP 121)  EX ADR          (SEXADR) <- OUTBUS <- (R)
395.
396.  006512L 00110001 11011111                  LDPP     OTBUS,IMPI,SIOD  OUTPUT DATA AND START FIRST DELAY
      006513L 00110111 00100000
      006514L 00110111 00101100
397.  006515L 01010001 10101010                  DLDPI    MAR0,SEXADR
      006516L 00110111 11000000
      006517L 01010001 11101111
      006520L 00110111 11100000
398.  006521L 00110001 11011100                  TSTIP    ,SWUSER,PSWI     SHOULD I HAVE DONE THAT?
      006522L 01000101 00000100
399.  006523L 11010010 00010011                  BRA      IVIOL6,FZ
400.  006524L 01010101 11100111                  DOPI     PSW0,ND,-1-SWSTDT-SWIDEV   MARK IN STATUS & NON-IMA MODES
      006525L 00110111 10001100
401.  006526L 00110001 11011111                  LDPP     MDW,IMPI         OUTPUT ADDRESS TO ITS SAVE AREA
      006527L 00110111 00100001
402.  006530L 01000000 01101001                  TSTIT    XR,IMAADR        DID WE ADDRESS THE IMA?
403.  006531L 11010010 00100011                  BRA      OUTW0,FZ
404.  006532L 01010001 00100000                  LDRI     COMMODE,COMMNPS  SET ADDRESSED BUT NO PORT SELECTED
      006533L 01101111 11111001
405.                                    . **
406.                                    . SET THE REAL TRANSMITTER & RECEIVER'S MODEM CONTROLS SO THAT THE SYSTEM
407.                                    . WILL START INTERRUPTING CORRECTLY
408.  006534L 00010001 11111011                  TSTIR    ,B7,TRNFCN      TURNED ON FIRST TIME?
      006535L 01000101 10000000
409.  006536L 11010010 10011011                  BRA      EXADML,FZ       YES, JUST ANOTHER SELECT
410.  006537L 01010001 10000000                  LDRI     TRNFCN,B7       YES, REMEBER IT
      006540L 00000111 11111011
411.  006541L 01010001 00111111                  LDPI     ACUOT,077       MP IS NOW ON, LINE LEFT MARKING
      006542L 00110111 00100100
412.  006543L 01101111 11110011                  LDRT     TRNCHN          REMEMBER AS FIRST INTERRUPTS ARRIVE
413.  006544L 01010001 00001000    EXADML      LDTI     SWIDEV
414.  006545L 11011111 10000101                  BRA      PSWOR
415.                                    *
416.  006546L                          EXSTAT:
417.                                    . 9.05   (    123)  EX STATUS       PUT IN STATUS MODE
418.                                    . 9.05   (IMP 123)  EX STATUS       OUTBUS <- (R)
419.
420.  006546L 00110001 11011111                  LDPP     OTBUS,IMPI,SIOD  OUTPUT DATA AND START FIRST DELAY
      006547L 00110111 00100000
      006550L 00110111 00101100
421.  006551L 00110001 11011100                  TSTIP    ,SWUSER,PSWI     SHOULD I HAVE DONE THAT?
      006552L 01000101 00000100
422.  006553L 11010010 00010011                  BRA      IVIOL6,FZ
423.  006554L 01010001 11101111                  LDTI     -1-SWSTDT        MARK IN STATUS MODE
424.  006555L 00110101 11011100    PSWND       DOPP     PSW0,ND,PSWI     CLEAR TO CORRECT MODE
      006556L 00110111 10001100
425.  006557L 01000101 00001000                  TSTIT    ,SWIDEV
```

```
                                                BRA     OUTW0,TZ
>006561L 01011001 11111111                     BRAX    FETCHI
>006562L 11001111 11111111
*
EXDATA:
. 9.05   (    125)  EX DATA          PUT IN DATA MODE
. 9.05   (IMP 125)  EX DATA          OUTBUS <- (R)

006563L 00110001 11011111             LDPP    OTBUS,IMPI,SIOD  OUTPUT DATA AND START FIRST DELAY
006564L 00110111 00100000
006565L 00110111 00101100
006566L 00110001 11011100             TSTIP   ,SWUSER,PSWI     SHOULD I HAVE DONE THAT?
006567L 01000101 00000100
006570L 11010010 00010011             BRA     IVIOL6,FZ
006571L 01010001 00010000             LDTI    SWSTDT           MARK IN DATA MODE
006572L 00110011 10011100 PSWOR       DOPP    PSW0,OR,PSWI     SET CORRECT MODE STATE
006573L 00110111 10001100
006574L 01000101 00001000             TSTIT   ,SWIDEV
006575L 11010011 00100011             BRA     OUTW0,TZ
>006576L 01011001 11111111            BRAX    FETCHW           (FETCHW FOR EX ADR)
>006577L 11001111 11111111
```

```
                                        +
                                        OUTPUT:
                                        . 9.05   (1xy: x=2,3: y ODD)          EX COM OUTPUT TO 5500 BUS
                                        . 9.05   (IMP 1xy)  EXr COM           OUTBUS <- (R)

                                        EXWRITE:
                                        .        (    127)  EX WRITE          WRITE DATA TO THE DEVICE
                                        .        (IMP 127)  EXr WRITE
 450. 006600L 00110001 11011111          LDPP     OTBUS,IMPI,SIOD  OUTPUT DATA AND START ZEROTH DELAY
      006601L 00110111 00100000
      006602L 00110111 00101100
 451. 006603L 00110001 11011100          TSTIP    ,SWUSER,PSWI
      006604L 01000101 00000100
 452. 006605L 11010010 00010011          BRA      IVIOL6,FZ           ONLY CONTINUE IF PRIVED
 453. 006606L 01000101 00001000          TSTIT    ,SWIDEV
 454. 006607L 11010011 00100011          BRA      OUTW0,TZ            NOT SPECIAL, DO NORMAL I/O
 455. 006610L 01110001 10111001  EXMOUT:  TSTIR    ,COMMPTS,COMMODE,CC
      006611L 01000101 00001111
 456. 006612L 11010011 11000010          BRA      FTCHIO,TZ           DO NOTHING FOR PORTS 4-7 (NON-EXISTANT)
 457. 006613L 01000101 00001100          BIT2ADR  SVCTRN-1            POINT TO TRANSMITTER BUFFER POSITION
      006614L 11010011 01101110
      006615L 01010100 00000001
      006616L 01000101 00001100
      006617L 11010011 01101110
      006620L 01010001 00000100
      006621L 01010010 01010111
      006622L 00110111 11000000
 458. 006623L 01010001 11101111          LDPI     MAROH,SVCTRN>8
      006624L 00110111 11100000
 459. 006625L 00110001 11011111          LDPP     MDW,IMPI            OUTPUT NEW DATA BYTE TO BE TRANSMITTED
      006626L 00110111 00100001
 460. 006627L 01110001 11111001          DORRR    TRNCTL,OR,TRNCTL,COMMODE SET THE BIT THAT DATA AVAILABLE
      006630L 01110011 11110101
      006631L 01101111 11110101
 461. >006632L 01011001 11111111         BRAX     FETCHW
      >006633L 11001111 11111111
 462.                                   *
 463. 006634L                           EXCOM3:
 464.                                   .        (    135)  EX COM3          DO CONTROL STROBE 3
 465.                                   .        (IMP 135)  EXr COM3
 466.
 467. 006634L 00110001 11011111          LDPP     OTBUS,IMPI,SIOD  OUTPUT DATA AND START ZEROTH DELAY
      006635L 00110111 00100000
      006636L 00110111 00101100
 468. 006637L 00110001 11011100          TSTIP    ,SWUSER,PSWI
      006640L 01000101 00000100
 469. 006641L 11010010 00010011          BRA      IVIOL6,FZ           ONLY CONTINUE IF PRIVED
 470. 006642L 01000101 00001000          TSTIT    ,SWIDEV
 471. 006643L 11010011 00100011          BRA      OUTW0,TZ            NOT SPECIAL, DO NORMAL I/O
 472. 006644L 00010111 10110010          CCLR
 473. 006645L 00110001 11011111          DOTIP    ,ND,07,IMPI         SELECT LOWER 3 BITS
```

```
                006646L 01010101 00000111
   474.         006647L 01010010 01001101          DORA    LINK,AC,EXC3B
                006650L 01101111 11110000
   475.         006651L 01010001 00000001          LDTI    1                   SHIFT BIT INTO POSITION
   476.         006652L 11101111 00000000          BRR     LINK
   477.         006653L 11001110 11111111          NOOP                        SET BIT 4
   478.         006654L 11001110 11111111          NOOP                        SET BIT 4 (COMMNXP BIT)
   479.         006655L 11001110 11111111          NOOP                        SET BIT 4
   480.         006656L 00010111 10100010          SHIFT   SL                  SET BIT 4
   481.         006657L 00010111 10100010          SHIFT   SL                  SET BIT 3
   482.         006660L 00010111 10100010          SHIFT   SL                  SET BIT 2 (CIRCULAR SHIFT)
   483.         006661L 00010111 10100010          SHIFT   SL                  SET BIT 1
   484.         006662L 01101111 11111001  EXC3B   LDRT    COMMODE             STORE BIT IN CORRECT POSITION
   485. >       006663L 01011001 11111111          BRAX    FETCH
        >       006664L 11001111 11111111
   486.                                    *
   487.         006665L                    EXCOM1:
   488.                                    .       (    131)  EX COM1          DO CONTROL STROBE 1
   489.                                    .       (IMP 131)  EXr COM1
   490.
   491.         006665L 00110001 11011111          LDPP    OTBUS,IMPI,SIOD     OUTPUT DATA AND START ZEROTH DELAY
                006666L 00110111 00100000
                006667L 00110111 00101100
   492.         006670L 00110001 11011100          TSTIP   ,SWUSER,PSWI
                006671L 01000101 00000100
   493.         006672L 11010010 00010011          BRA     IVIOL6,FZ           ONLY CONTINUE IF PRIVED
   494.         006673L 01000101 00001000          TSTIT   ,SWIDEV
   495.         006674L 11010011 00100011          BRA     OUTW0,TZ            DO NORMAL I/O
   496.         006675L 01110001 11111001          TSTIR   ,COMMPTS,COMMODE
                006676L 01000101 00001111
   497.         006677L 11010011 11000010          BRA     FTCHIO,TZ           DO NOTHING UNLESS PORTS 0..3 SELECTED
   498.         006700L 01010001 00110011          BAL     LINK,EXC1MCLR       ASSUME DTR NOT SET
                006701L 01101111 11110000
   499.         006702L 00110001 11011111          TSTIP   ,B4,IMPI            WAS THAT BIT SET?
                006703L 01000101 00010000
   500.         006704L 11010011 00111000          BRA     EXC1CHN,TZ          NO, WASN'T
   501.         006705L 01010001 00110000          BAL     LINK,EXC1MSET       YES, IT WAS
                006706L 01101111 11110000
   502.                                    .
   503.         006707L 01110001 11111001  EXC1CHN  TSTIR   ,B2,COMMODE         CONVERT CHANNEL NO. TO BIT POSITION
                006710L 01000101 00000100
   504.         006711L 11010011 00110100          BRA     EXC1NT2,TZ          NOT CHANNEL 2 (ITS POSITION IS OK)
   505.         006712L 01010001 00010000          LDTI    B4                  CH. 2'S BIT IN SPECIAL POSITION
   506.         006713L 11101111 00000000  EXC1NT2  BRR     LINK                NOW, SET OR CLEAR THAT BIT
   507.                                    .
   508.         006714L 01010000 11111111  EXC1MCLR DOTI    ,XR,0377            CLEAR, INVERT BITS
   509.         006715L 00010101 11111011          DOTR    ,ND,TRNFCN          SO CAN 'AND' THE BIT OUT
   510.         006716L 11011111 00101111          BRA     EXC1MDO             SHOW THE RESULTS
   511.                                    .
   512.         006717L 00010011 11111011  EXC1MSET DOTR    ,OR,TRNFCN          SET, SO SET THE BIT
   513.         006720L 00000111 11111011  EXC1MDO  LDRT    TRNFCN              REMEMBER THE NEW STATE
   514.         006721L 00110111 00100101          LDPT    SDLCMD              SHOW IT TO THE WORLD
```

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   515. >006722L 01011001 11111111          BRAX    FETCH           AND DONE
        >006723L 11001111 11111111
   516.                                   *
   517.  006724L                          EXCOM2:
   518.                                   .       (    133)  EX COM2      DO CONTROL STROBE 2
   519.                                   .       (IMP 133)  EXr COM2
   520.  006724L                          EXCOM4:
   521.                                   .       (    137)  EX COM4      DO CONTROL STROBE 4
   522.                                   .       (IMP 137)  EXr COM4
   523.
   524.  006724L 00110001 11011111          LDPP    OTBUS,IMPI,SIOD OUTPUT DATA AND START ZEROTH DELAY
         006725L 00110111 00100000
         006726L 00110111 00101100
   525.  006727L 00110001 11011100          TSTIP   ,SWUSER,PSWI
         006730L 01000101 00000100
   526.  006731L 11010010 00010011          BRA     IVIOL6,FZ       ONLY CONTINUE IF PRIVED
   527.  006732L 01000101 00001000          TSTIT   ,SWIDEV
   528.  006733L 11010010 11000010          BRA     FTCHIO,FZ       ** DO NOTHING WHERE NOTHING TO DO **
   529.  006734L 00110001 00110001  OUTW0    TSTIP   ,STIODR,STATUS
         006735L 01000101 00000010
   530.  006736L 11010011 00100011          BRA     OUTW0,TZ        DELAY 0 WAITING FOR DATA TO REACH DEVICE
   531.  006737L 00110111 00101111          STB     SOTS            GIVE COMMAND
   532.  006740L 00110001 00110001  OUTW1    TSTIP   ,STIODR,STATUS
         006741L 01000101 00000010
   533.  006742L 11010011 00011111          BRA     OUTW1,TZ        DELAY 1 WAITING FOR COMMAND TO GET THERE
   534.  006743L 00110111 00101100          STB     SIOD            EXTEND THE COMMAND DELAY FOR FINAL STEP
   535.  006744L 00110001 00110001  OUTW2    TSTIP   ,STIODR,STATUS
         006745L 01000101 00000010
   536.  006746L 11010011 00011011          BRA     OUTW2,TZ        DELAY 2 WAITING FOR PARITY TO RETURN
   537.  006747L 01000101 00001000          TSTIT   ,STPFOU         WAS THERE AN OUTPUT PARITY FAULT?
   538.  006750L 11010011 11000010          BRA     FTCHIO,TZ       NO!
   539.  006751L 01010001 00001100          LDTI    SVOUTP          YES, TELL SUPERVISOR THAT THERE WAS
   540. >006752L 01011001 11111111          BRAX    SCLSTW
        >006753L 11001111 11111111
   541.                                   *
   542. >006754L 01011001 11111111  IVIOL6  BRAX    IVIOLs
        >006755L 11001111 11111111
   543. >006756L 01011001 11111111  MEMPF6  BRAX    MEMPFs
        >006757L 11001111 11111111
   544.
   545.                                           LIST    -G
   546.  006760L 11111111 11111111               TABPAGE CDOXL
   547.                                           LIST    G
   548.  001000                     CDOXLEN       EQU     $-CDOXP         "X"'S WERE "R"'S
   549.  006000                                   USE     CDOXL
   550.  006000                                   SKIP    CDOXLEN
   551.                                           END
```

*** ERRORS: D

IMASBPI
TSTPI ,MCSIN, B'6'
BRA IMAISTS, FZ
BRA IMA SCAZ

```
        AC              115     145     207     208     209     210     231     237     252     339     457     474
010017  ACCTL           *56:I
010015  ACD             *53:I
010017  ACPH            *55:I    56:I
010016  ACPL            *54:I
        ACUIN           207     208     209     210     306     327
        ACUOT           411
010014  APFRK           *47:I
010013  APFRP           *46:I
010016  APFTK           *49:I
010015  APFTP           *48:I
        B0               51     279     317
        B1               51     289     295     324
        B2               51     288     293     323     503
        B3               51      71     293
        B4               50     143     187     298     327     329     499     505
        B5               49      71     143     187     327
        B6               71     301     329
        B7               71     408     410
006014  BITOK    (M)    *115     115
006440  BITOK    (M)    *339     339
006621  BITOK    (M)    *457     457
020006  BR              *21:I
000100  CAP55IO         *121:I   125:I
000102  CAPABILI        *125:I
000000  CAPAPF          *118:I   125:I
000000  CAPBLUE         *117:I   125:I
000000  CAPCOM          *122:I   125:I
000000  CAPDMPIO        *119:I   125:I
000002  CAPIMA          *116:I   125:I
000000  CAPIVS          *135:I   *20:A
000000  CAPMICR         *115:I   125:I
000000  CAPRIM          *120:I   125:I
        CC               107     119     129     130     132     145     179     207     208     209     210     233
                         234     236     260     285     304     305     336     343     455     472     480     481
                         482     483
007000  CDOR            *133:I
006000  CDOX            *132:I    99
006000  CDOXL           *101     103     546
001000  CDOXLEN         *548     550
006000  CDOXP           *103     548
        CF               119     122     124     131     135     144     145     154     155     170     177     178
                         183     184     186     188     207     208     209     210     224     235     248     249
                         252     266     274     275     277     279     280     282     286     290     291     310
                         315     317     319     325     338     341     344     346     404     408     410     412
                         460     474     484     496     498     501     503     509     512     513
006102  CHKANY          *182     170
006103  CHKCHN          *183     181
006075  CHKNXT          *173     167     168
000040  COMMNPS          *49     275     313     404
000020  COMMNXP          *50     275
030011  COMMODE         *75:I    275     280     291     336     338     341     344     404     455     460     484
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006754  IVIOL6      *542    364   382   399   422   435   452   469   493   526
020004  IZ           *19:I
010001  KBSCNT       *28:I
030000  LINK         *61:I  170   177   185   207   208   209   210   214   215   220   221
                      227   238   241   268   474   476   498   501   506
010003  MADR         *33:I
        MAROH         116   247   335   397   458
        MAROL         115   248   339   397   457
010004  MBITS        *34:I
010005  MBSTAT       *35:I
010006  MCRCH        *36:I
010007  MCRCL        *37:I
        MDR           124   348
010010  MDSKS        *38:I
010011  MDSKT        *39:I
        MDW           249   401   459
        MEMPF$        543
006756  MEMPF6      *543    113   123   245   267   347
020002  MO           *17:I  113   123   245   267   347
        MODIN         298   301   329
        MODW          117   246
020003  MP           *18:I  113   123   245   267   347
010013  MSECT        *41:I
010012  MTRAK        *40:I
        OTBUS         396   420   433   450   467   491   524
006600  OUTPUT      *442
006734  OUTW0       *529    403   426   439   454   471   495   530
006740  OUTW1       *532    533
006744  OUTW2       *535    536
010000  PDLNP        *27:I
006477  PIN         *373
006507  PINERR      *387    384
000111  PRE          *18:A
000000  PROC        *129:I
002000  PROD        *130:I
        PSWI          117   246   363   381   398   421   424   434   437   451   468   492
                      525
006555  PSWND       *424
        PSWO          400   424   437
006572  PSWOR       *437    414
010002  Q            *25:I  130   132   179   234   236   260   285   304   305   343   472
                      480   481   482   483
030010  RCH0C        *92:I  207
010014  RCH0D        *93:I  207
006126  RCH0END     *207    207
030012  RCH1C        *94:I  208
030013  RCH1D        *95:I  208
006143  RCH1END     *208    208
030014  RCH2C        *96:I  209
030015  RCH2D        *97:I  209
006160  RCH2END     *209    209
030016  RCH3C        *98:I  210
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030017	RCH3D	*99:I	210									
006175	RCH3END	*210	210									
030006	RCRCH	*72:I										
030007	RCRCL	*73:I										
006307	RCVBRK	*256	254									
030007	RCVCTL	*91:I	266	282	286	319	346					
006220	RCVDATA	*226	238									
006202	RCVMRK	*213	214	221	268							
006204	RCVSPC	*215	215									
006313	RCVSTB	*261	251									
030005	RDATA	*71:I										
000014	REV	*2:I										
030004	RPNTR	*70:I										
030003	RSTAT	*69:I										
	SB	115	339	457								
010002	SCANSV	*29:I										
	SCLSTW	388	540									
	SDLCMD	514										
006072	SENANY	*170	108									
006037	SENDTA	*126	110									
006106	SENEND	*186	156	168								
006047	SENMARK	*136	134									
006062	SENTRY	*155	170									
	SEXADR	397										
	SINS	367										
	SIOD	396	420	433	450	467	491	524	534			
	SL	179	260	285	304	305	343	480	481	482	483	
	SMR	118	340									
	SOTS	531										
	SR	130	132	234	236							
	SRVNXT	146	189	211								
	STATUS	368	385	529	532	535						
	STIODR	368	529	532	535							
	STPFIN	385										
	STPFOU	537										
	SVCRCV	247	248	335	339							
	SVCTRN	115	116	457	458							
	SVINP	387										
	SVOUTP	539										
	SWIDEV	365	383	400	413	425	438	453	470	494	527	
	SWSTDT	272	400	423	436							
	SWUSER	117	246	363	381	398	421	434	451	468	492	525
000140	TCOUNT	*31	119									
030001	TEMP1	*62:I	64:I	154	178	183	207	208	209	210	224	233	235
		249	274	279	290	310	317	325					
030002	TEMP2	*63:I	65:I	207	208	209	210	248	252	258			
030001	TEMPH	*64:I											
030002	TEMPL	*65:I											
030003	TRNCHN	*87:I	144	188	412								
030005	TRNCTL	*89:I	122	155	184	277	315	460					
030004	TRNDTA	*88:I	124	129	131								
010013	TRNFCN	*86:I	408	410	509	512	513						

030006	TRNSEL	*90:I	107	119	135	145	154	186	
000004	TYPE	*4:I							
030012	URPNTR	*76:I							
030010	UXPNTR	*74:I							
000002	VER	*1:I							
030016	XCRCH	*80:I							
030017	XCRCL	*81:I							
030015	XDATA	*79:I							
030014	XPNTR	*78:I							
030013	XSTAT	*77:I							