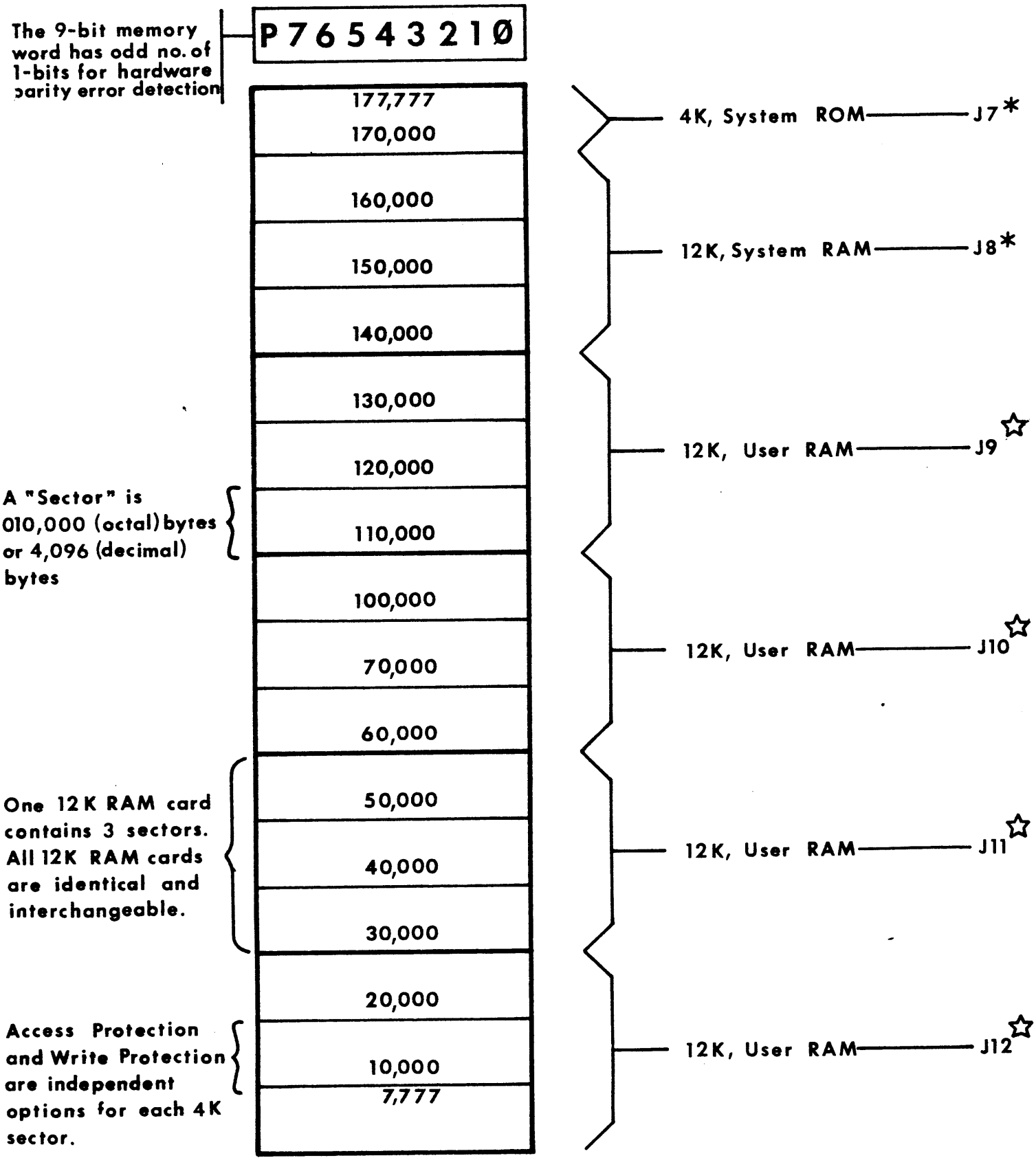
DATAPOINT 1800
MAINTENANCE COURSE
FOR

PARIS

SEPTEMBER 1977

INSTRUCTOR: LEN CONRAD

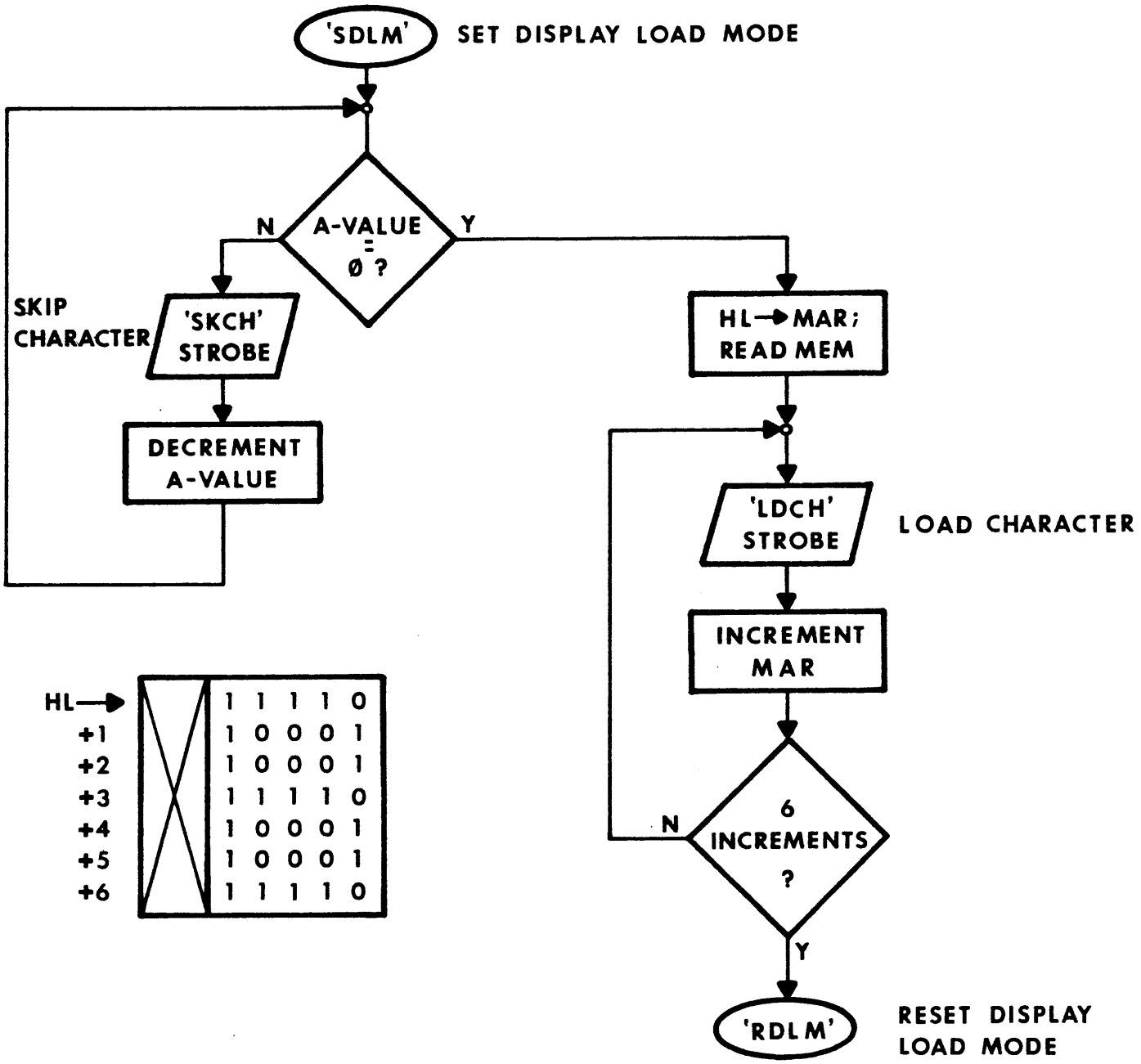


1800/3800 MEMORY ORGANIZATION MAP

[For a memory of 28K to 64K, using 12K RAM cards]

*Cards in these locations are necessary for operation.

☆Cards in these locations are optional for operation.

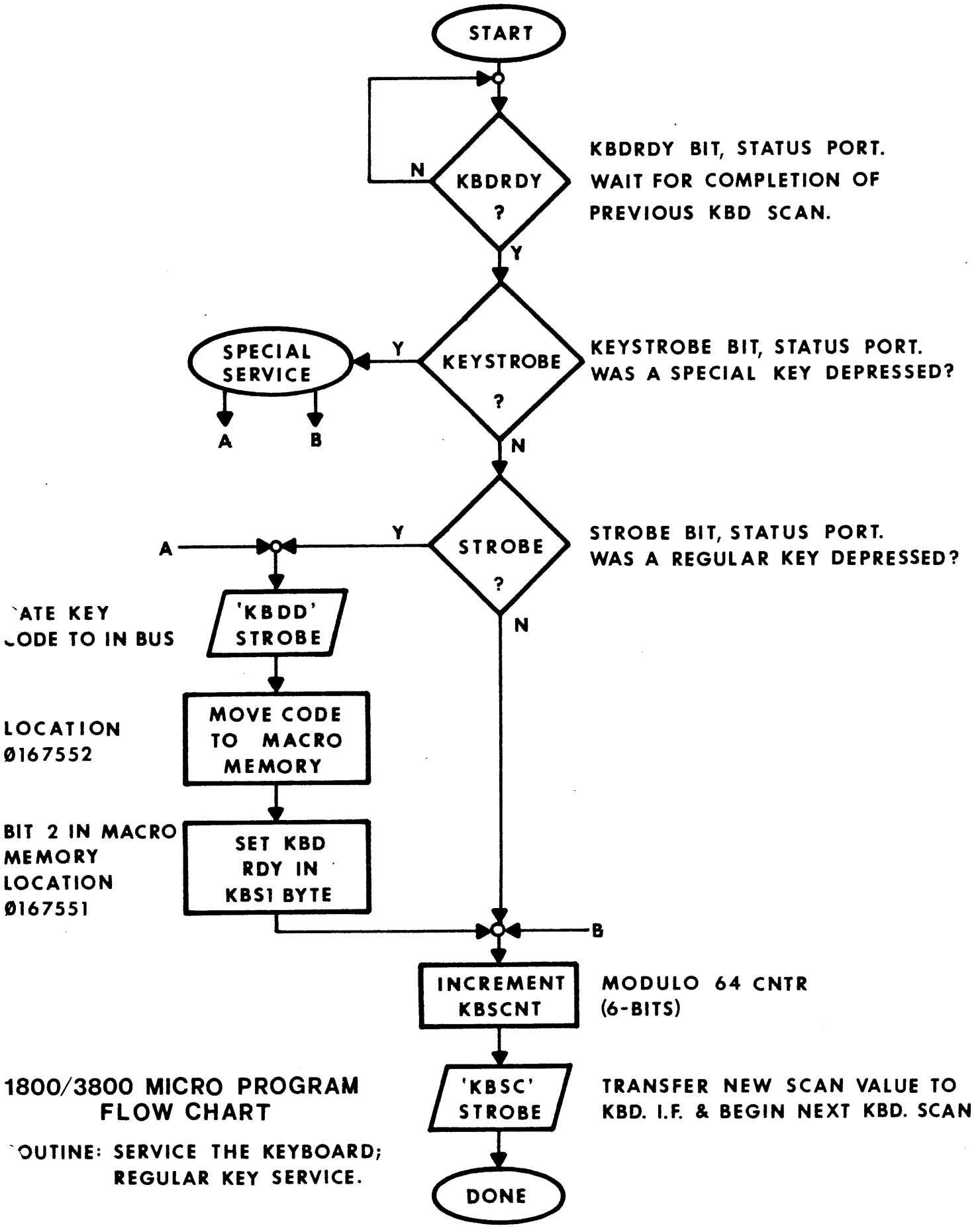


1800/3800 MICRO PROGRAM FLOW CHART

ROUTINE: TRANSFER THE 5 x 7 MATRIX DATA FOR ONE CHARACTER FROM THE MACRO MEMORY TO THE DISPLAY CONTROLLER

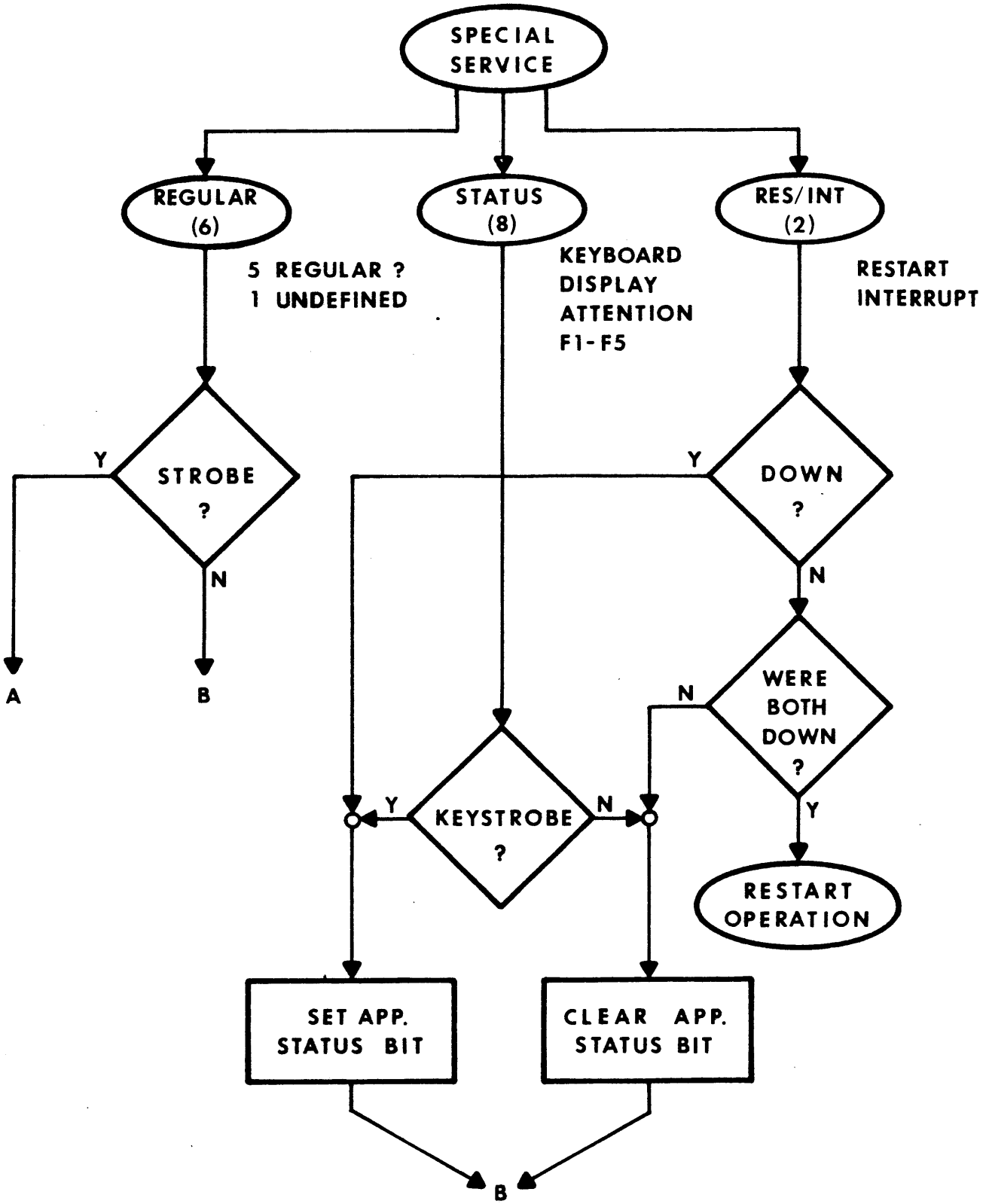
ENTRY CONDITIONS: 1.A-REG CONTAINS THE CHARACTER CODE
EXAMPLE: Ø1Ø2 FOR "B" IN ASCII.

2.HL CONTAINS THE ADDRESS OF THE MACRO MEMORY LOCATION OF THE FIRST BYTE OF A 7-BYTE STRING.



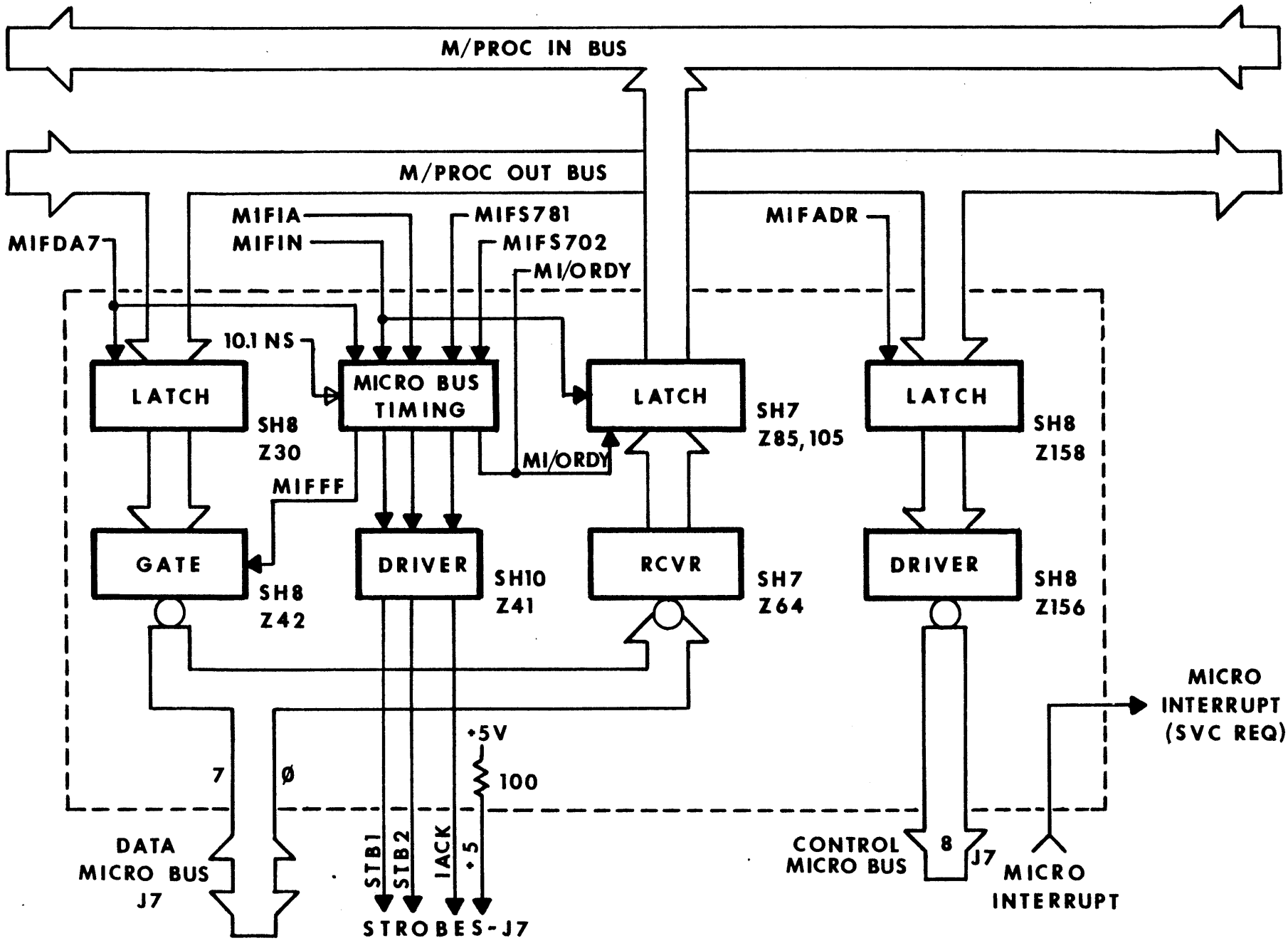
1800/3800 MICRO PROGRAM FLOW CHART

OUTINE: SERVICE THE KEYBOARD;
REGULAR KEY SERVICE.

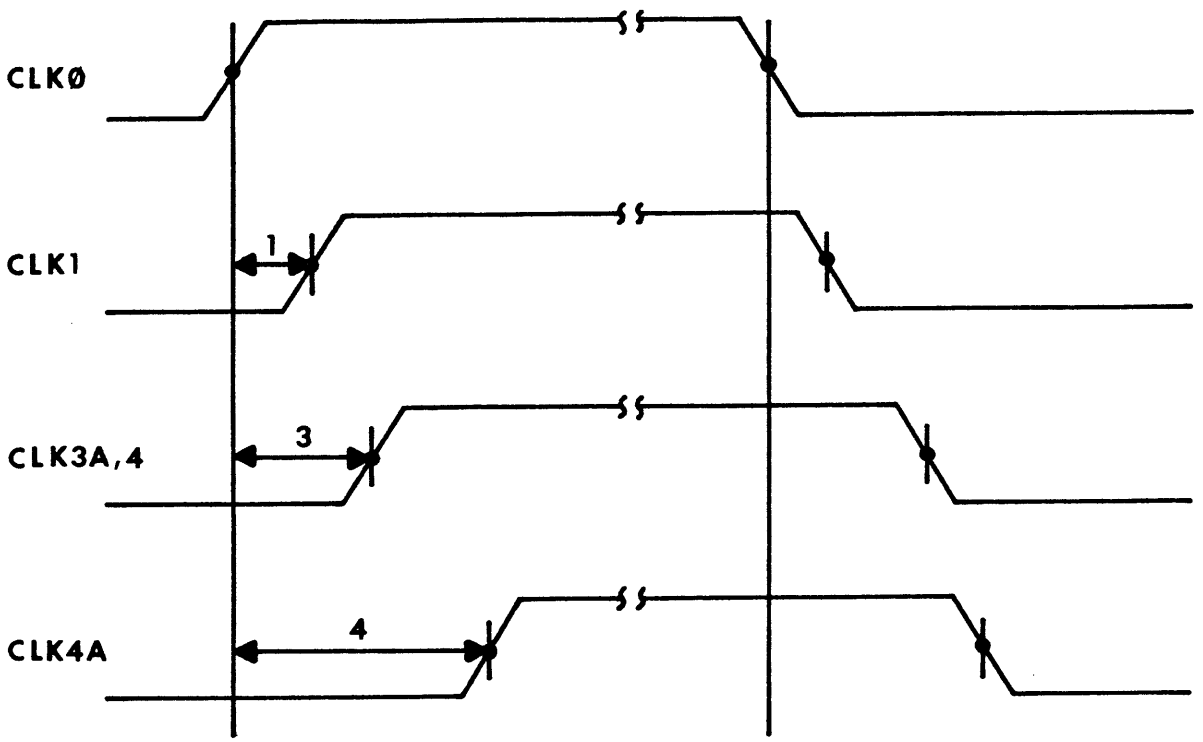


1800/3800 MICRO PROGRAM FLOW CHART

ROUTINE: SERVICE THE KEYBOARD;
SPECIAL KEY SERVICE

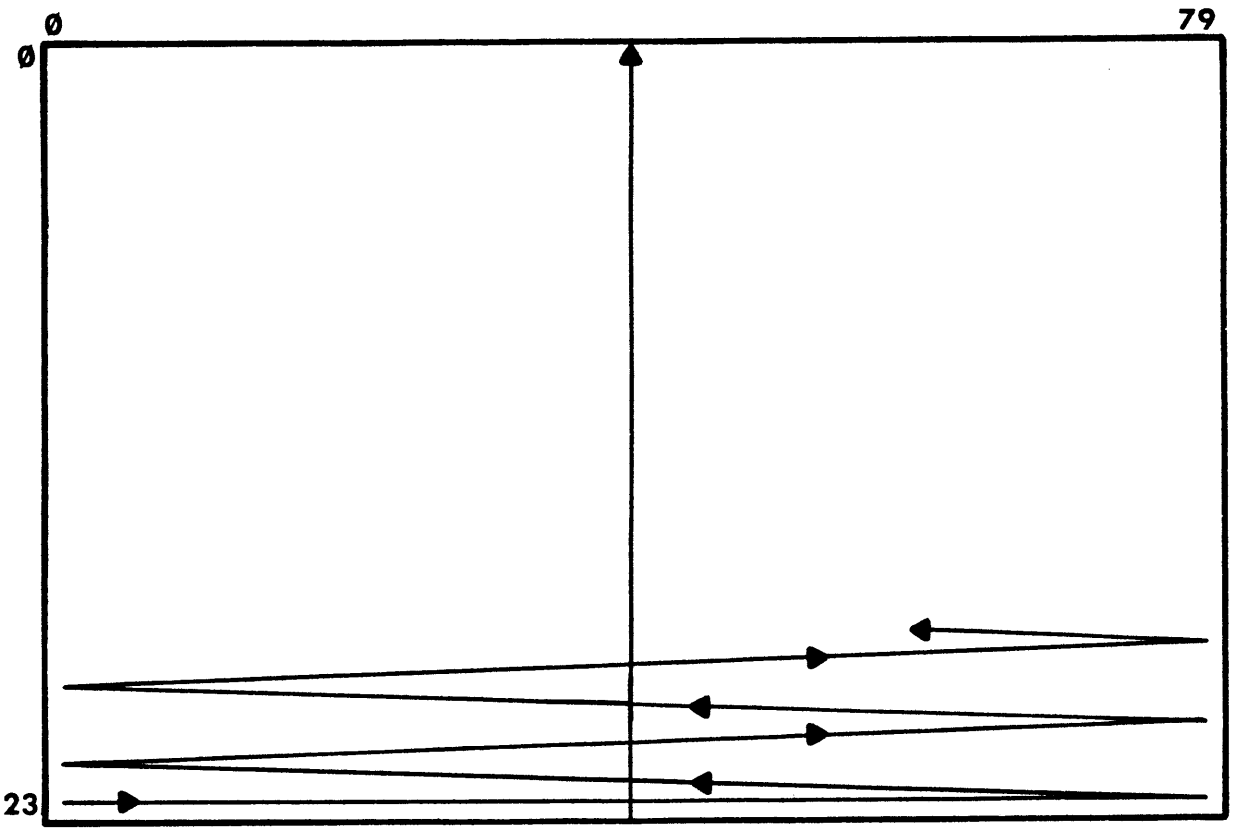


1800 MICRO BUS INTERFACE BLOCK DIAGRAM
(DISPLAY I/O BOARD)



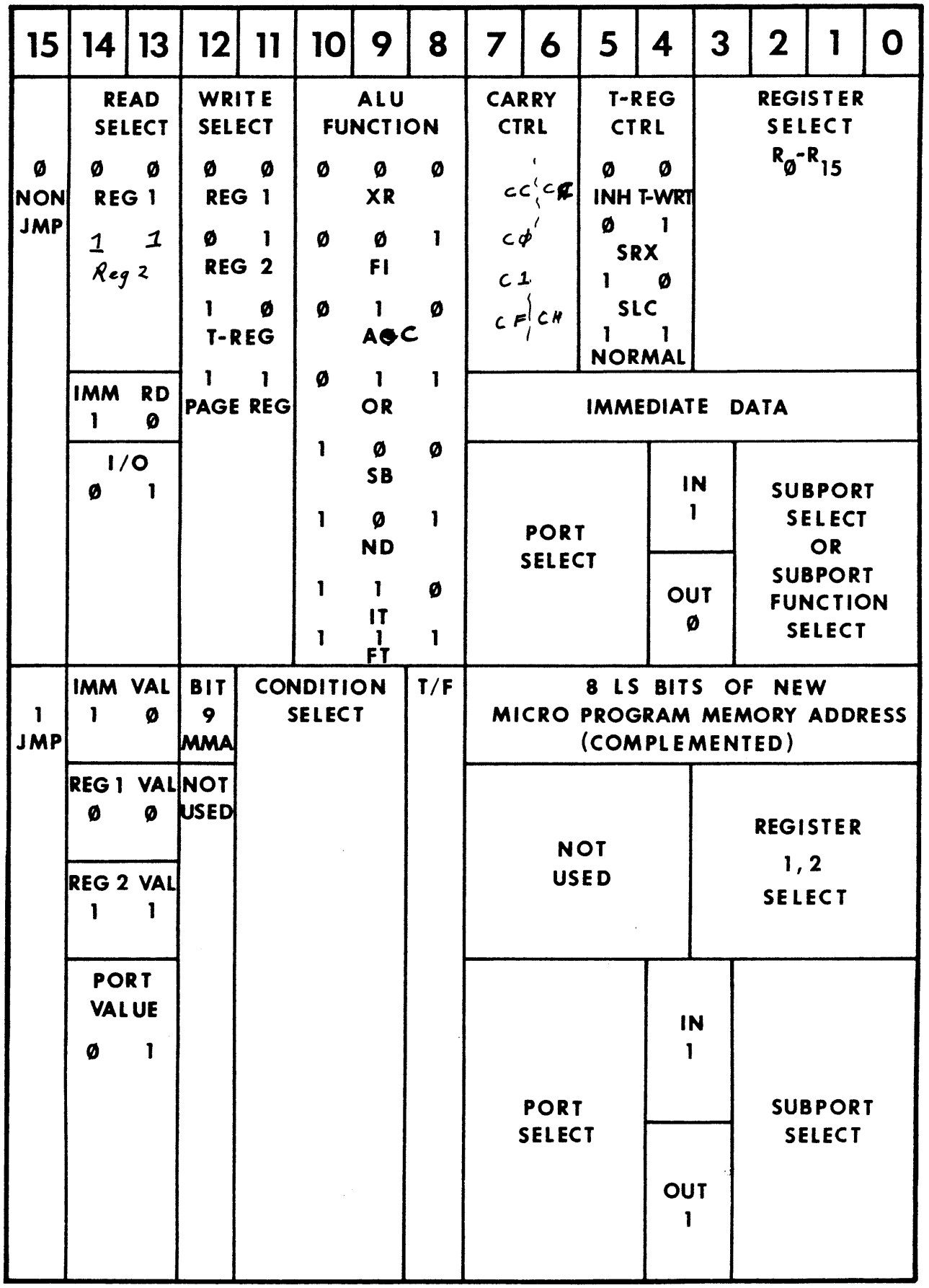
DATAPOINT 1800 MICRO PROCESSOR TIME BASE

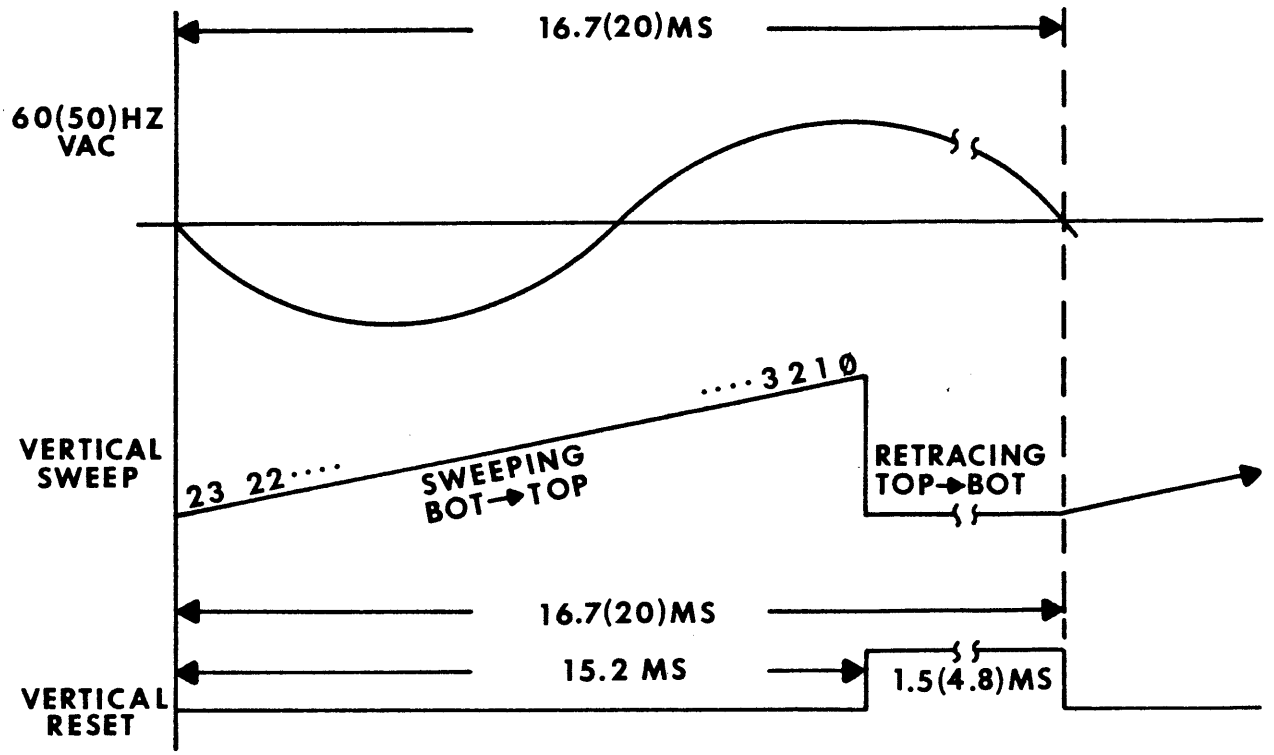
TIMING DIAGRAM SHOWING RELATIVE
SCHOTTKY-GATE DELAYS



1800/3800 DISPLAY DEFLECTION SCHEME MACRO VIEW

1. DOT ROW SCAN TECHNIQUE.
2. 10 ROWS/CHAR x 24 LINES = 240 HORIZONAL SWEEPS/FRAME.

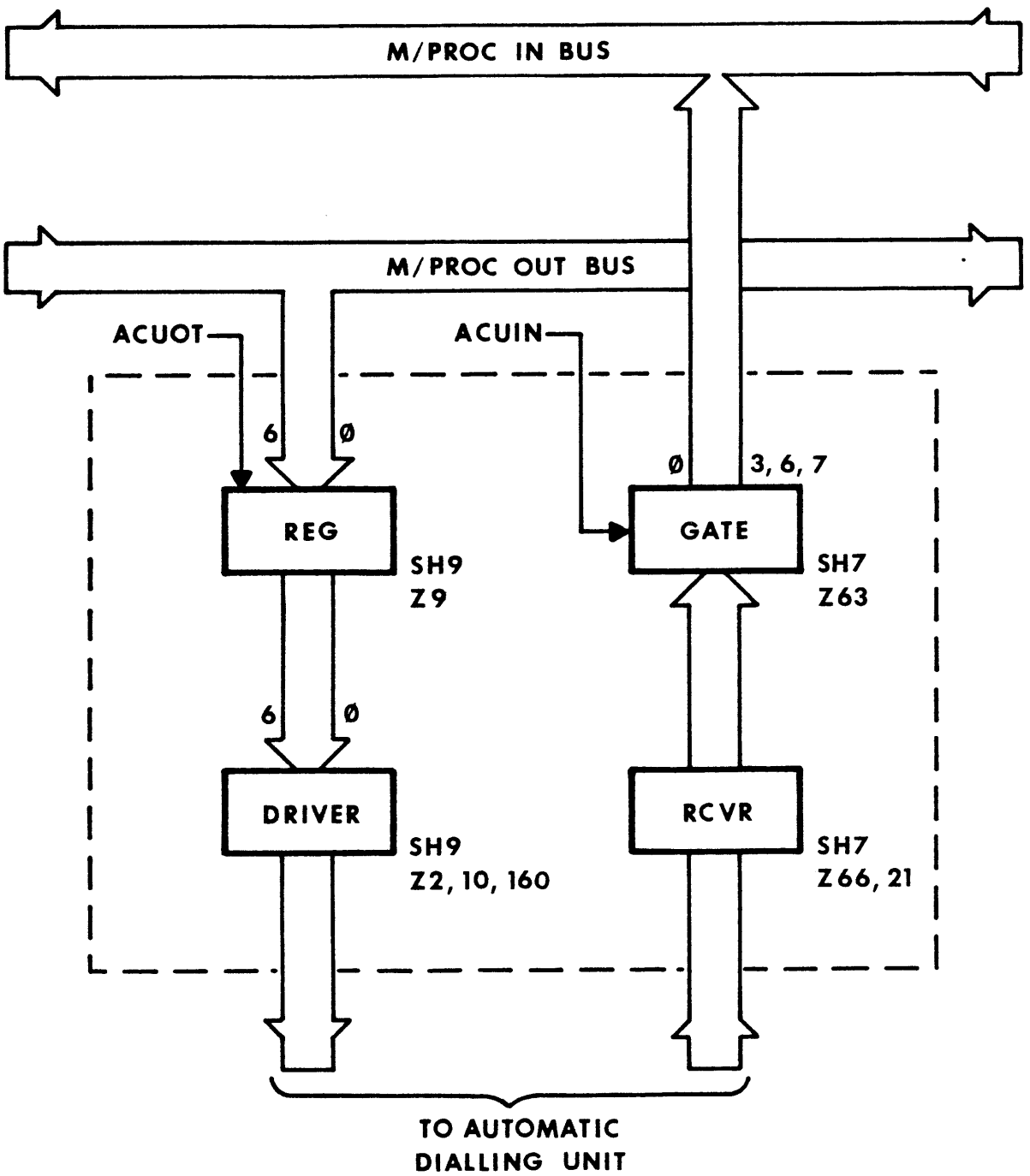

15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
0 NON JMP
READ SELECT
0 0 REG 1
1 1 Reg 2
0 1 REG 2
1 0 T-REG
1 1 PAGE REG
WRITE SELECT
0 0 REG 1
0 1 REG 2
1 0 T-REG
1 1 PAGE REG
ALU FUNCTION
0 0 0 XR
0 0 1 FI
0 1 0 A⊕C
0 1 1 OR
1 0 0 SB
1 0 1 ND
1 1 0 IT
1 1 1 FT
CARRY CTRL
CC CC
CΦ
C1
CF CH
T-REG CTRL
0 0 INH T-WRT
0 1 SRX
1 0 SLC
1 1 NORMAL
REGISTER SELECT
R0-R15
IMM RD
1 0
I/O
0 1
IMMEDIATE DATA
PORT SELECT
IN 1
OUT 0
SUBPORT SELECT OR SUBPORT FUNCTION SELECT
1 JMP
IMM VAL
1 0
REG 1 VAL
0 0
REG 2 VAL
1 1
PORT VALUE
0 1
BIT 9
MMA
NOT USED
CONDITION SELECT
T/F
8 LS BITS OF NEW MICRO PROGRAM MEMORY ADDRESS (COMPLEMENTED)
NOT USED
REGISTER 1, 2 SELECT
PORT SELECT
IN 1
OUT 1
SUBPORT SELECT



1800/3800 CRT DISPLAY SYSTEM

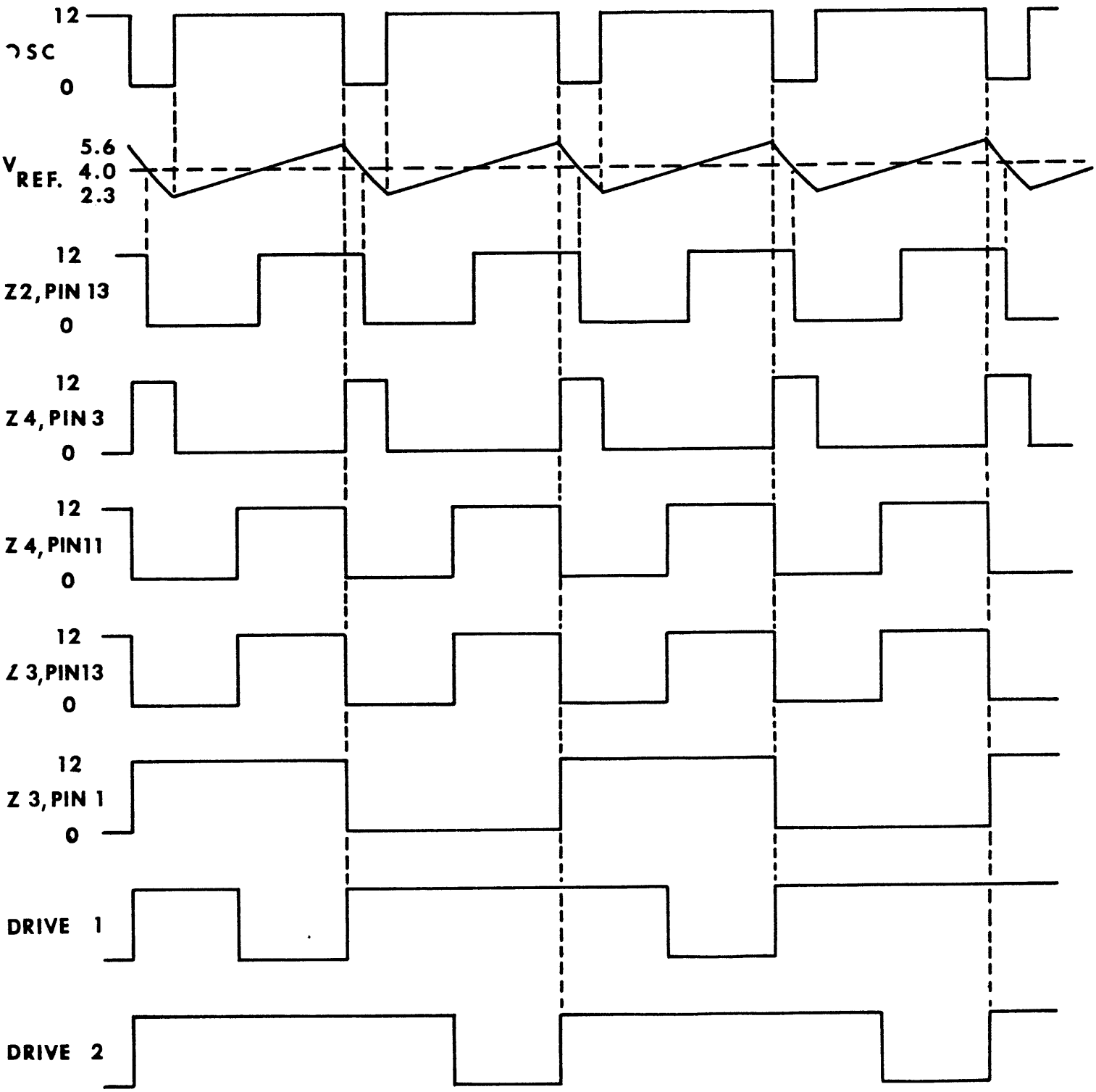
11.0592 MHZ ⟶ 90.4 NS/DOT
× 7 DOTS/CHAR = 633 NS/CHAR (INCLUDING HORIZONTAL SPACING)
×100 CHAR/ROW = 63.3 US/ROW (INCLUDING HORIZONTAL RETRACE)
× 10 ROWS/LINE = 633 US/LINE (INCLUDING VERTICAL SPACING)
× 24 LINES/FRAME = 15.2 MS/FRAME

TIMING: 1) AC LINE SYNC
2) FRAME TIMING

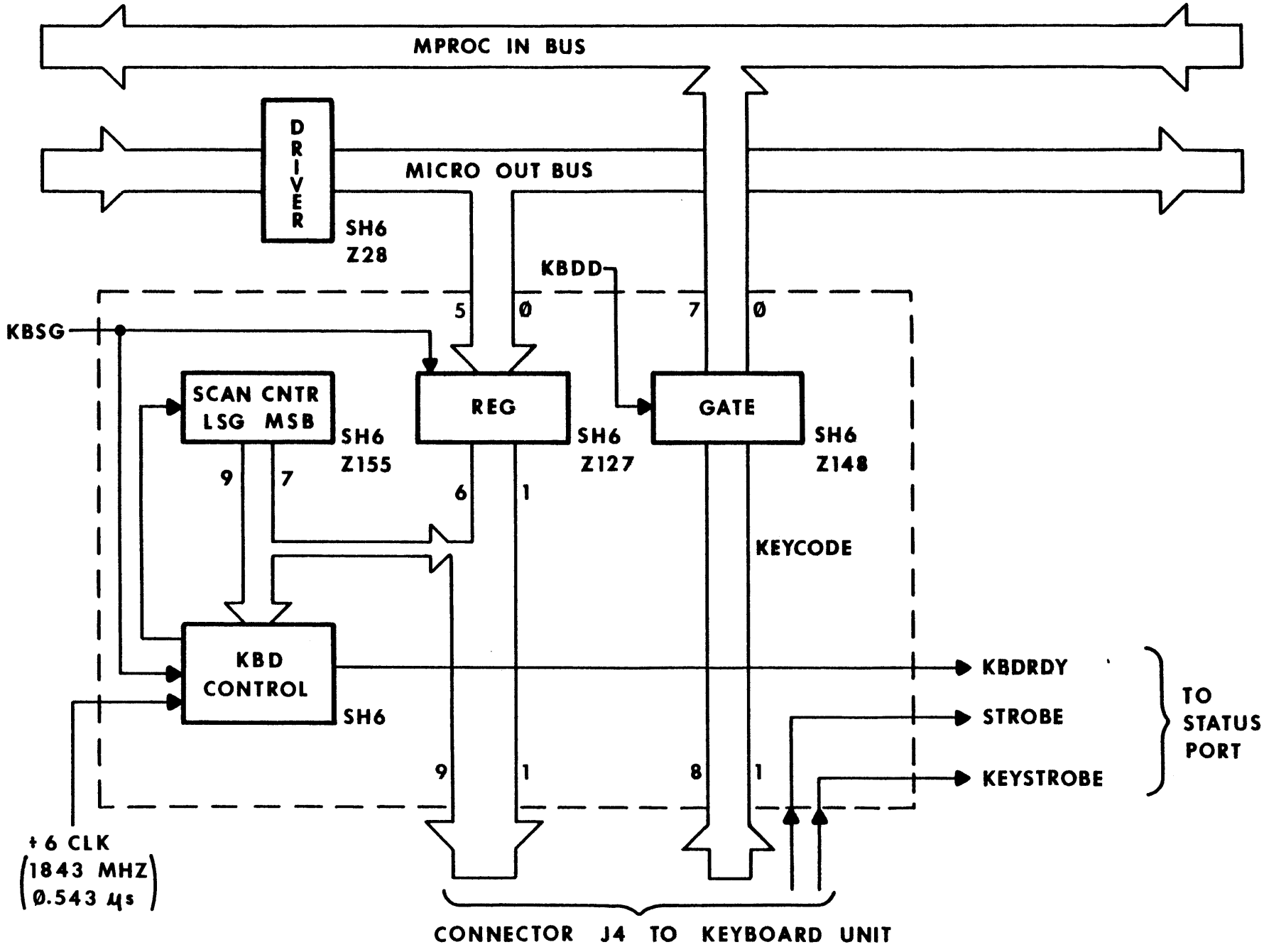


1800/3800 ACU INTERFACE BLOCK DIAGRAM

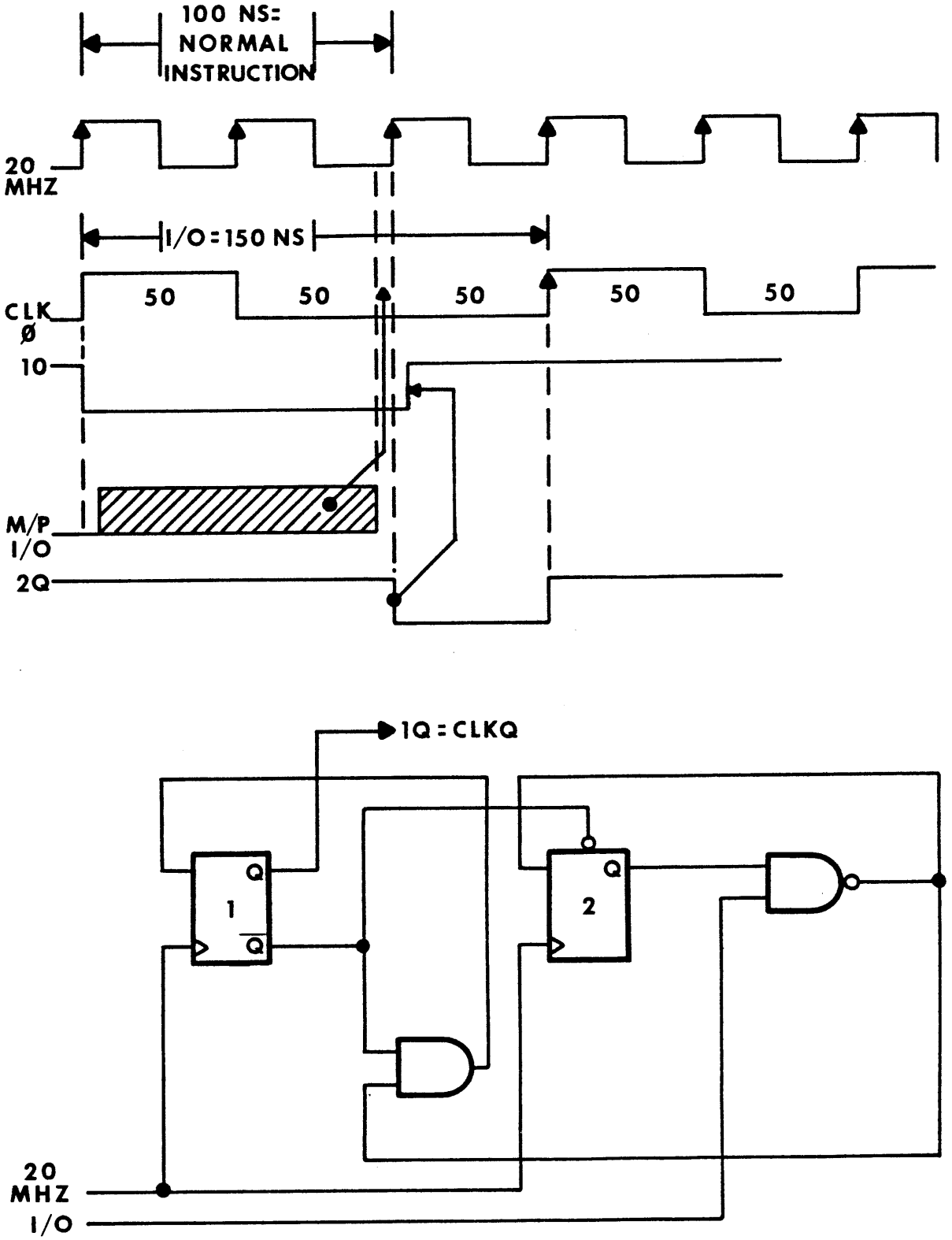
(DISPLAY I/O BOARD)



1800/3800 POWER SUPPLY
TIMING DIAGRAM
POWER SUPPLY CONTROL BOARD

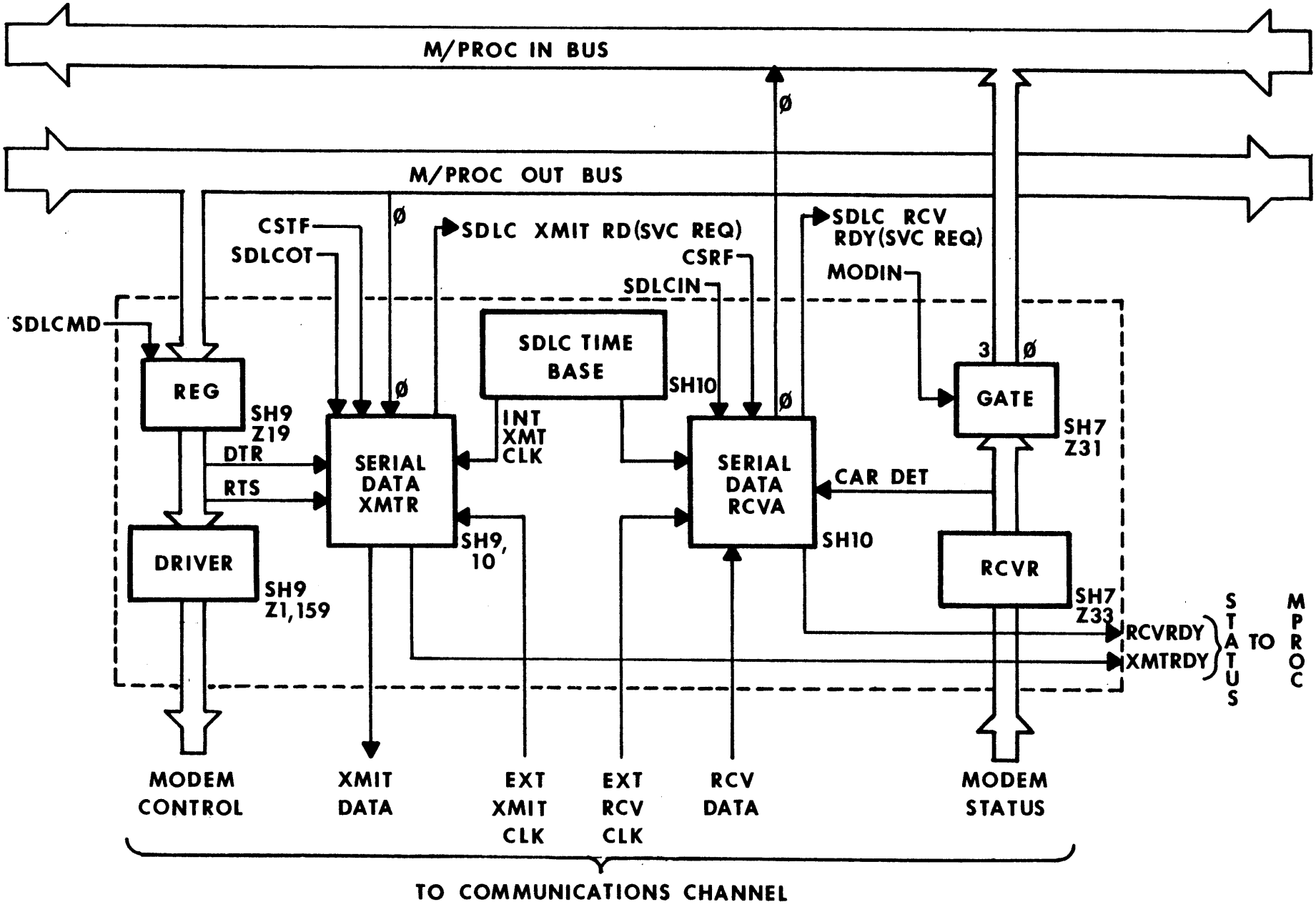


1800/3800 KEYBOARD INTERFACE BLOCK DIAGRAM
(DISPLAY I/O BOARD)



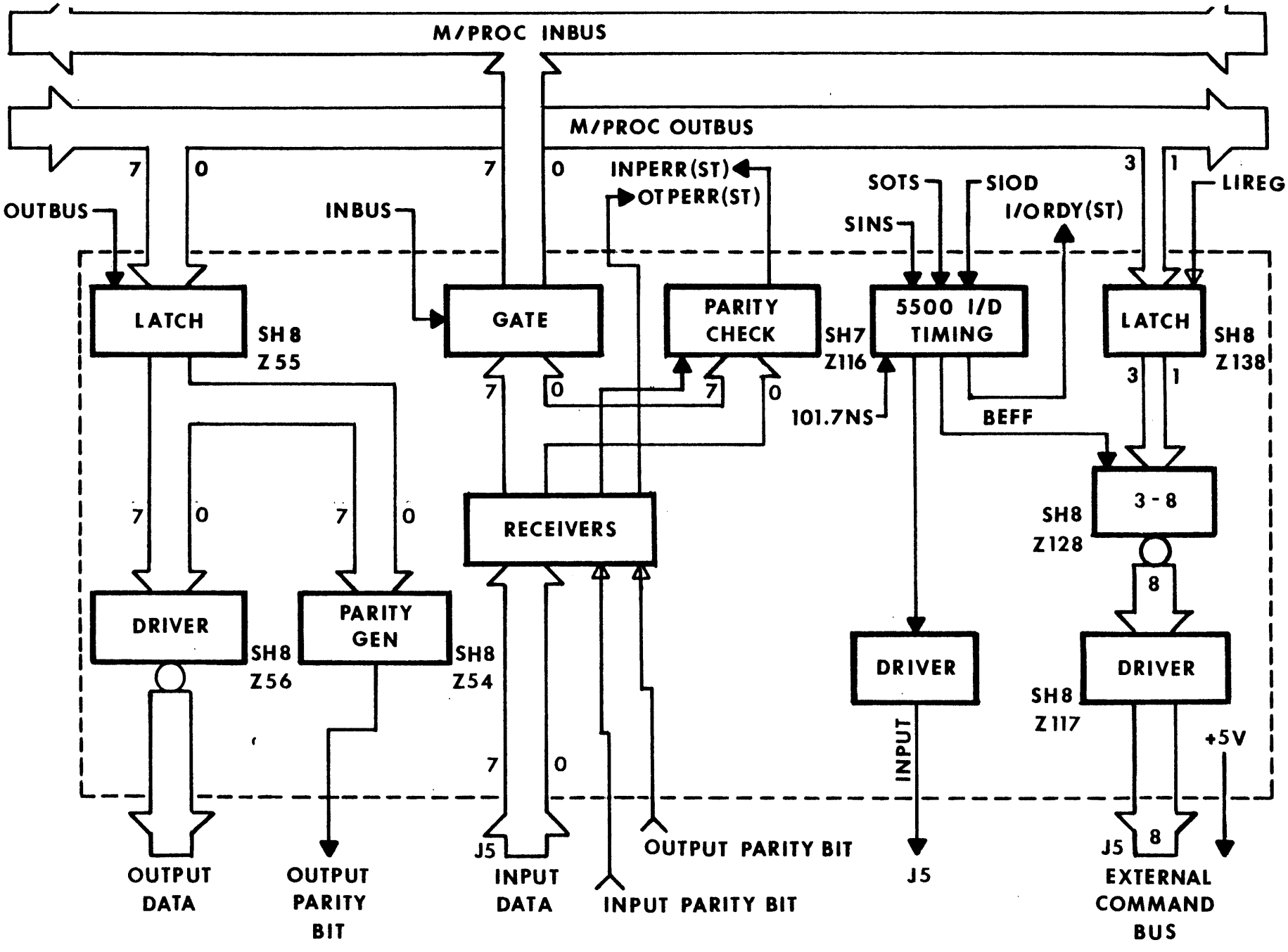
DATAPOINT 1800 MICRO PROCESSOR TIME BASE

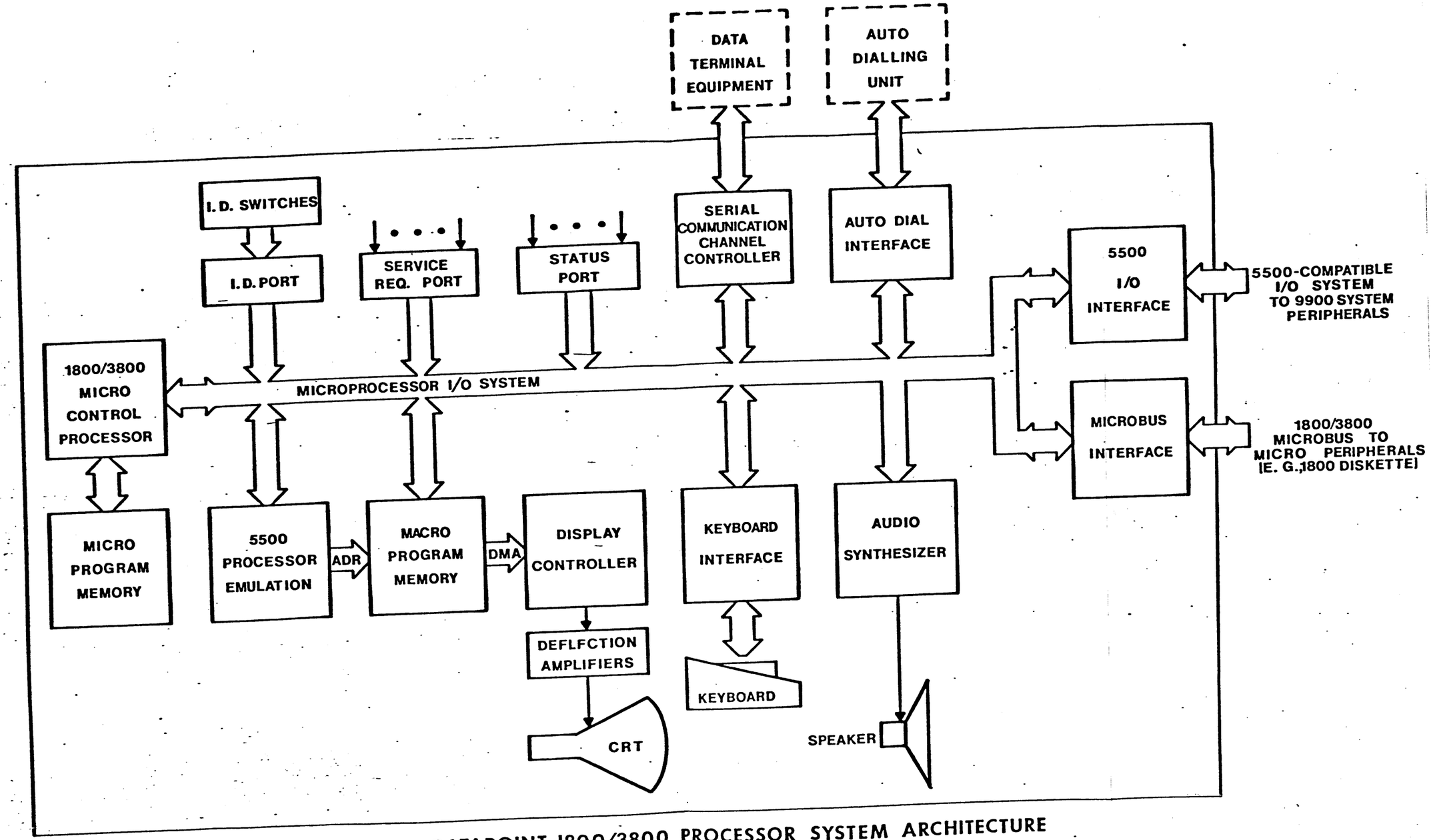
SIMPLIFIED SCHEMATIC, TIMING DIAGRAM



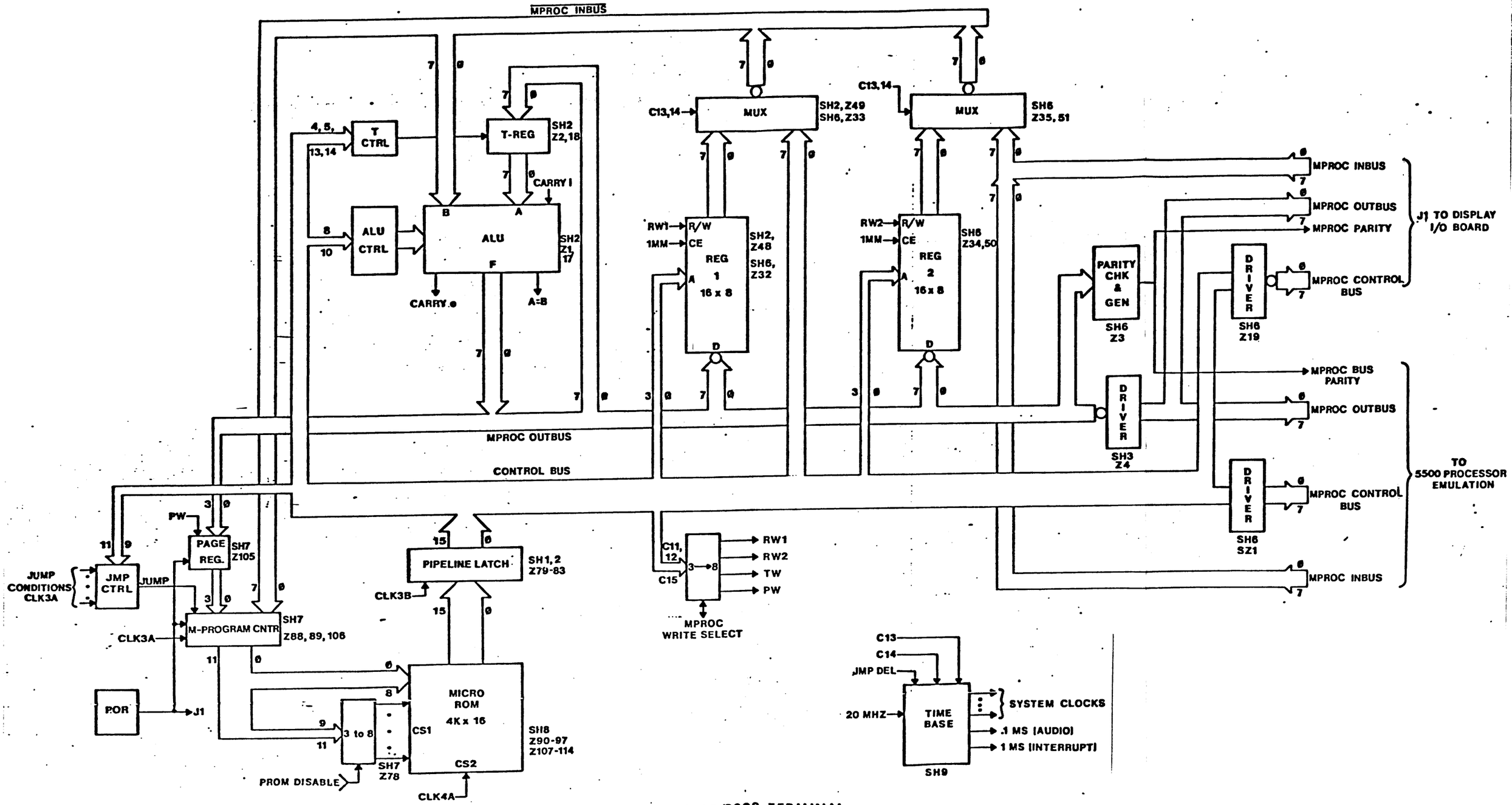
1800/3800 MODEM INTERFACE BLOCK DIAGRAM
(DISPLAY I/O BOARD)

14

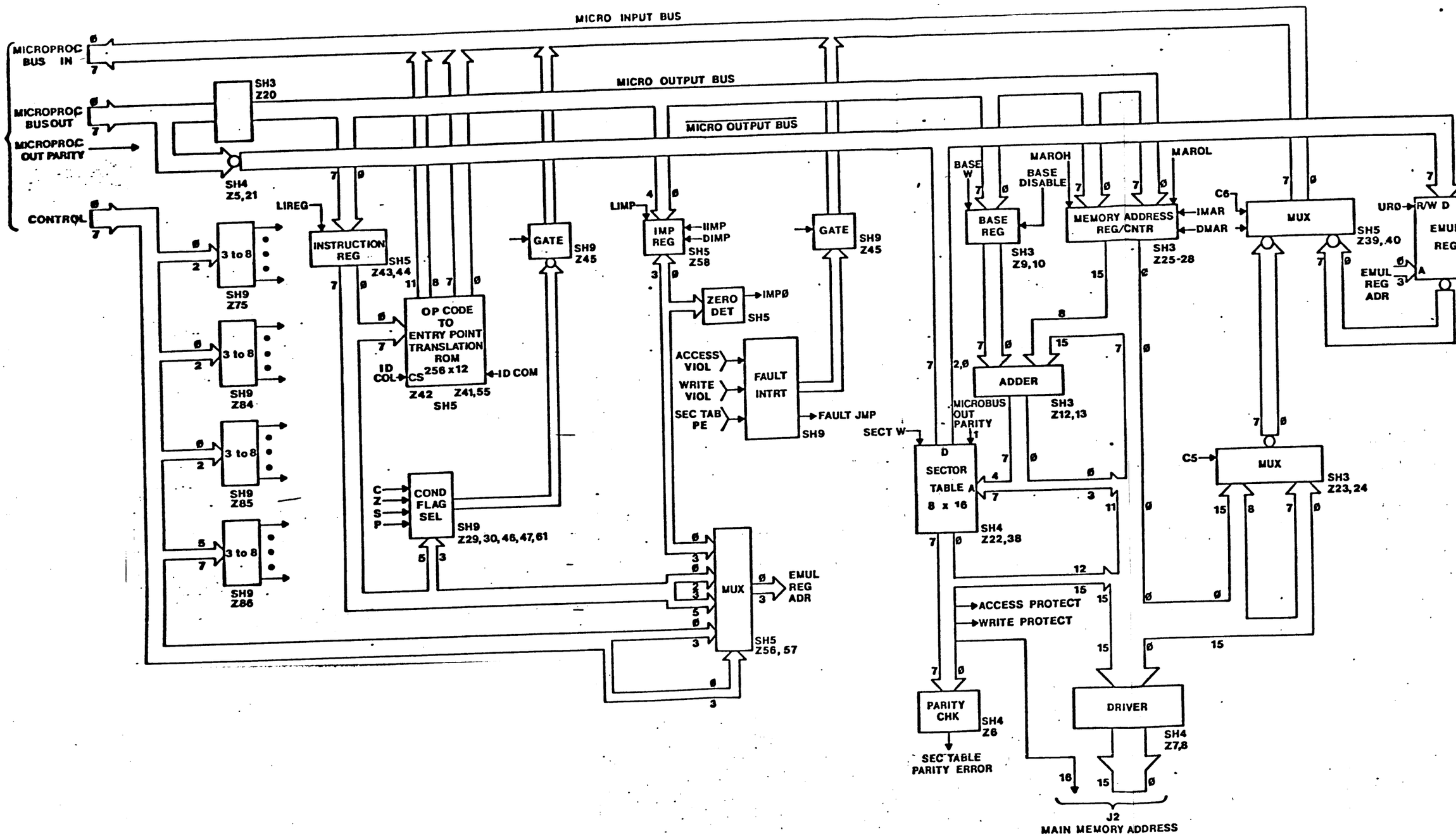

M/PROC INBUS
M/PROC OUTBUS
OUTBUS
INBUS
INPERR(ST)
OTPERR(ST)
SOTS
SIOD
I/ORDY(ST)
SINS
LIREG
LATCH
SH8
Z55
GATE
PARITY
CHECK
SH7
Z116
5500 I/D
TIMING
LATCH
SH8
Z138
101.7NS
BEFF
3 - 8
SH8
Z128
RECEIVERS
DRIVER
SH8
Z56
PARITY
GEN
SH8
Z54
DRIVER
DRIVER
SH8
Z117
INPUT
+5V
J5
OUTPUT PARITY BIT
OUTPUT
DATA
OUTPUT
PARITY
BIT
INPUT
DATA
INPUT PARITY BIT
J5
J5
EXTERNAL
COMMAND
BUS



DATAPOINT 1800/3800 PROCESSOR SYSTEM ARCHITECTURE

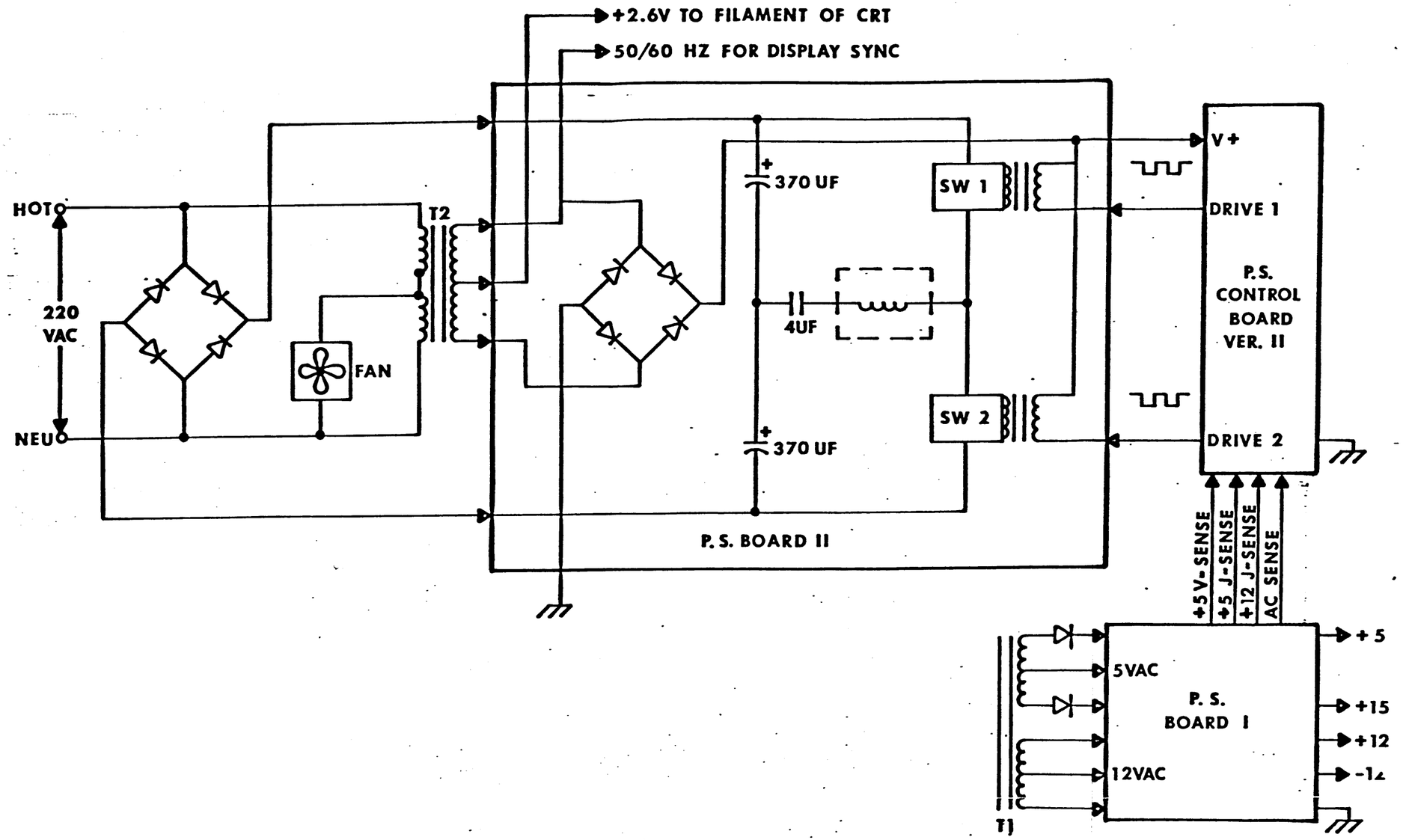


1800/3800 TERMINAL
MICROPROCESSOR BLOCK DIAGRAM
(PROCESSOR/EMULATION BOARD)



1800/3800 TERMINAL

5500 PROCESSOR EMULATION BLOCK DIAGRAM



1800/3800 PROCESSOR POWER SUPPLY BLOCK DIAGRAM