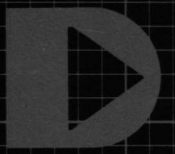
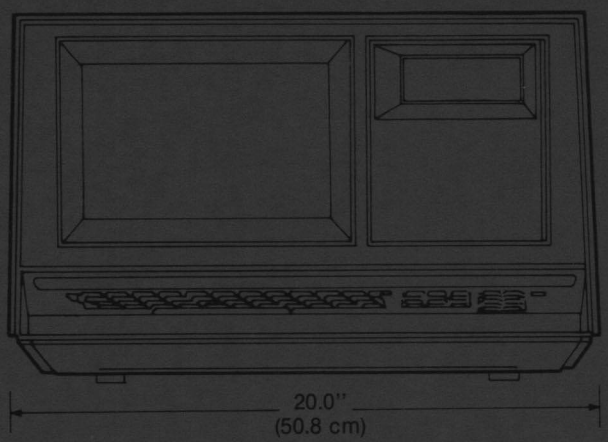


Product specification and
hardware reference manual

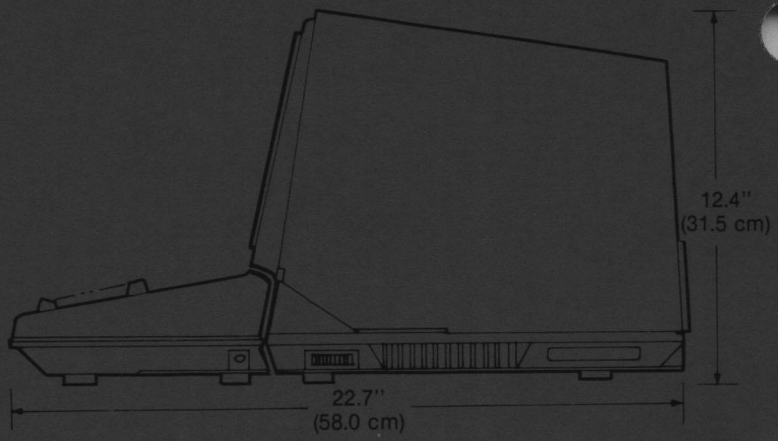
Datapoint 1560

1560 PROCESSOR

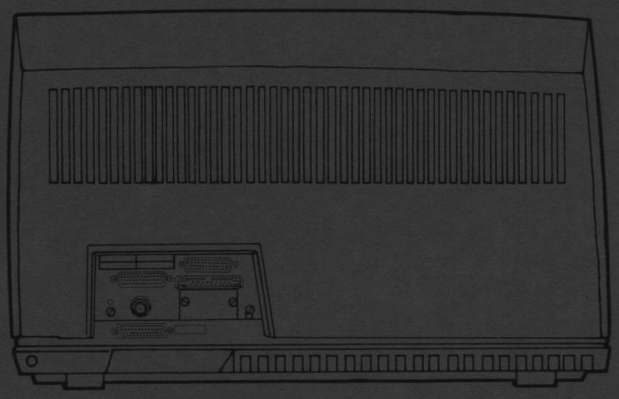
FRONT



SIDE



BACK



PREFACE

The computer-oriented user will find this manual useful for evaluation of the Datapoint 1560 processor capabilities. However, only the hardware considerations are covered in this manual. The full utility of the Datapoint 1560 cannot be appreciated until the available software support for the machine has been reviewed.

Software available for the 1560 processor includes high level languages, operating systems, text editors, communications programs, utility programs, etc. Reference should be made to the latest issue of the Datapoint Software Catalog for more information.

Table of Contents

PART 1
GENERAL FEATURES

1.1 Introduction

The Datapoint® 1560 Processor is intended for use in data entry, data processing, word processing, electronic message service, and data communications applications. The basic processor consists of a Z80A microprocessor, 12K of system ROM, 64K of RAM (expandable to 128K), typewriter-style keyboard, video display screen, communications interface, and printer interface.

1.2 System Elements

There are four basic elements in the 1560 processor. This chapter introduces the basic elements: CRT display, keyboard, processor, and memory. The 1560 may be interfaced to a variety of peripheral devices.

1.3 CRT Display

The CRT display provides the following features:

- 1920 characters
- 80-character by 24-line format
- Program-defined 128-character font
- 60 frames/second refresh rate (50 frames/second when using 50 Hz power)
- 5x7 matrix character generation
- 5x7 solid blinking cursor, alternates with characters, nondestructive
- Direct processor control of CRT display line-by-line
- Inverse video, character-by-character
- Amber screen
- Operator adjustable screen intensity

1.4 Keyboard

The keyboard provides a basic 55-key alphanumeric group, an 11-key numeric group and 10 programmable system control keys.

The keyboard provides a unique multikey roll-over characteristic giving maximum ease of typing. The control processor itself performs key scanning. An audible click and a "beep" for acoustic cues to the operator are available under software control.

1.5 Processor

The integral processor provides all control functions and includes:

- 8-bit memory word length (plus parity)
- 64 or 128K RAM memory
- 12K ROM for system functions
- Internal communications interface
- Supports Datapoint's Disk Operating System (DOS), DATABUS® language, FORTRAN, and BASICPLS and CP/M* operating system
- Microbus for direct control of disk or diskette

1.6 Memory

The memory contains both random access memory (RAM) for program storage, and read only memory (ROM) for system functions such as initialization, Boot Block, memory test, keyboard and display routines, diskette routines, a debug program, and various test routines.

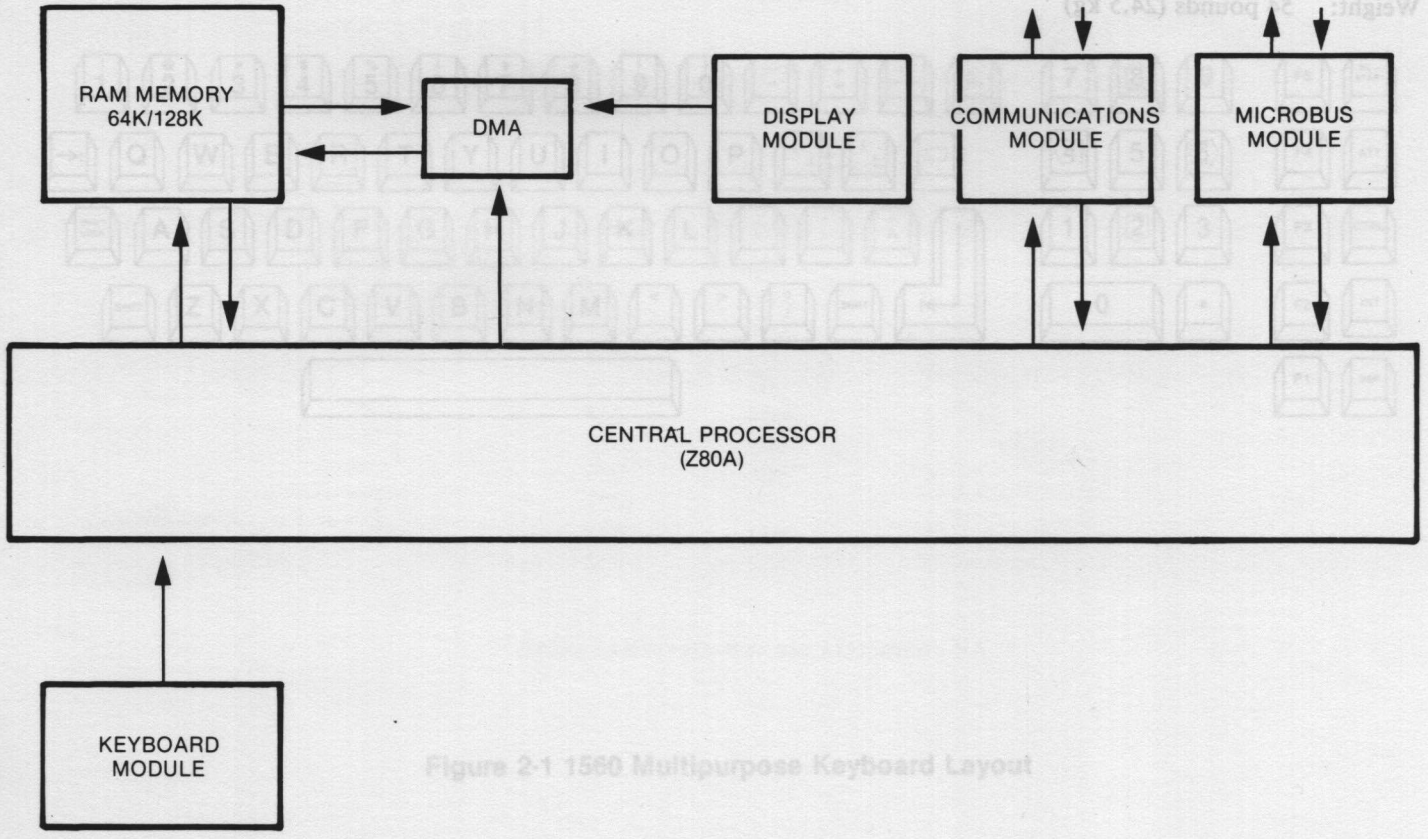


Figure 1-1 1560 Processor Schematic

1.7 Communications Channels

There are two serial communications channels provided in the basic unit. One channel is either Synchronous or Asynchronous and is provided for communication with a host system. Baud rates are programmable from 50 to 9600 baud when operating in asynchronous mode or external clock only for synchronous operation. The second channel is provided for local printer support under processor control but can be used as a second communications channel.

The Multifunction Communications interface option provides two serial communication channels. Channel A is either synchronous or asynchronous and allows bit-level protocols including SDLC, CCITT X.25, and ISO HDLC. Channel B is asynchronous only and provides communication with a DATASHARE® workstation.

1.8 Local Network Interface

The local network interface option provides a means of communication with other processors or workstations over an ARCNET™ local network. The interface provides all error detection, message protocol, and ARCNET protocol.

1.9 General Specifications

Power Requirements:
120/220/230/240 VAC (+/- 10%), 60 or 50 Hz
(+/- 1 Hz) 150 Watts, 512 Btu/Hour

Equipment Dimensions:
1560 with Removable Keyboard
Height: 12.4 inches (31.5 cm)
Width: 20.0 inches (50.8 cm)
Depth: 22.7 inches (58.0 cm)
Weight: 54 pounds (24.5 kg)

1560 with Fixed Keyboard
Height: 11.5 inches (29.2 cm)
Width: 18.5 inches (47 cm)
Depth: 19.3 inches (48.9 cm)
Weight: 50 pounds (22.7 kg)

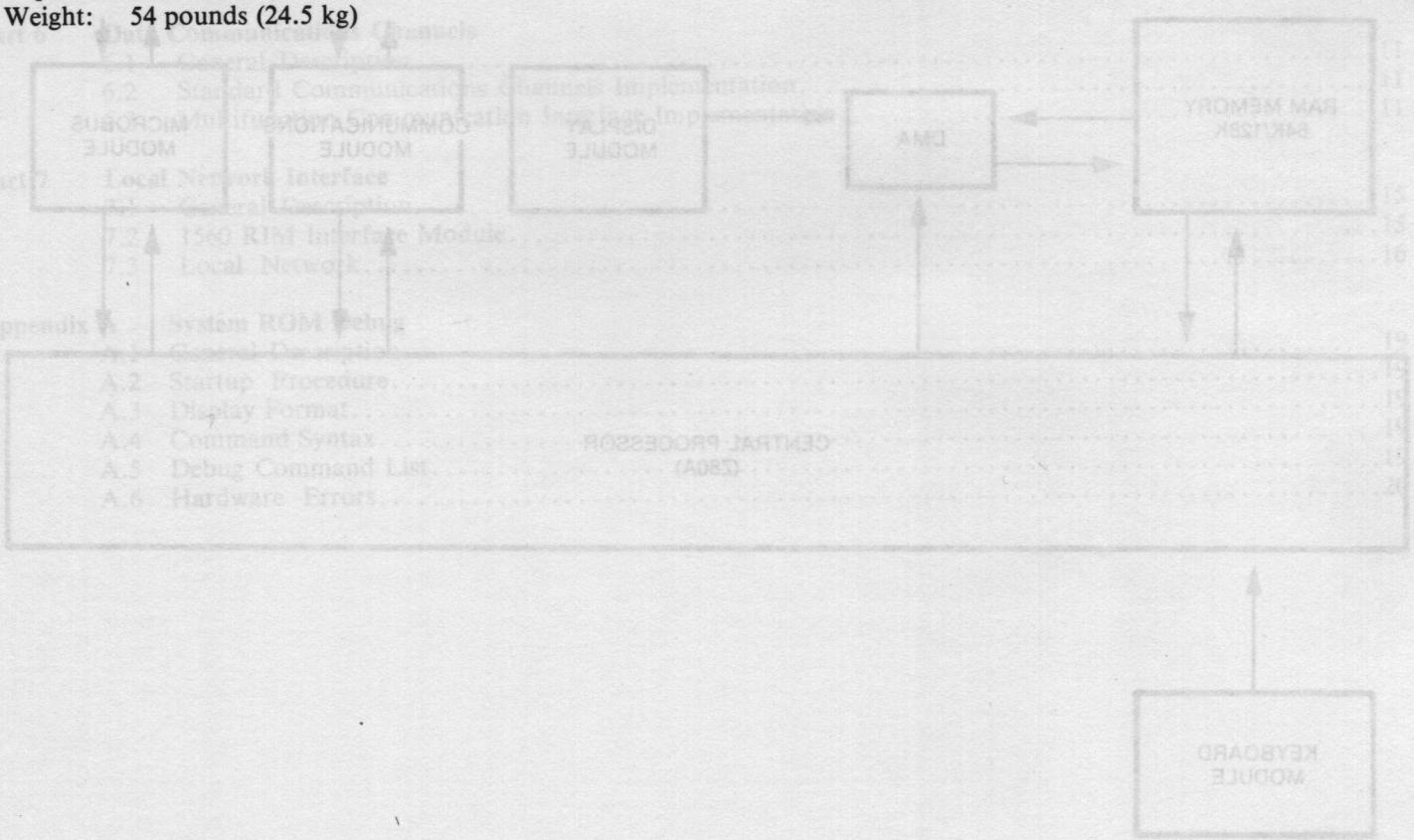
Operating Environment:
50 to 100 degrees F (10 to 38 degrees C)
20 to 90% relative humidity, noncondensing

WARNING:

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to correct the interference.

1.10 Peripherals

The 1560 will accommodate a wide variety of external peripherals such as printers, disks, and diskettes. Refer to the Datapoint Equipment Catalog (Document No. 60001) for a complete description of peripherals.



PART 2
KEYBOARD

2.1 General Description

The multipurpose keyboard on the Datapoint 1560 processor (see Figure 2-1) performs the functions of data entry, processor control, and word processing. This keyboard provides for 76 key positions including a 11-key numeric pad, shift/shift-lock functions and the standard ASCII alphanumeric set, and features a unique multi-key roll-over characteristic to allow for maximum ease of typing. In addition to the standard ASCII alphanumeric set, the multipurpose keyboard includes word processing keycaps.

Key coding is done in Programmable Read Only Memory (PROMs). On processors equipped with a removable keyboard, the keyboard can be detached up to one meter from the processor. Status is provided to allow macro-programs to generate "repeat" functions if desired.

Ten function keys are located on the right side of the keyboard. Five of these keys are reserved for control over the processor as follows:

RESTART
Momentary contact switch which sets a status bit that may be tested at any time by the processor. When pressed together with the INTERRUPT key, RESTART causes a jump to a bootstrap routine in the ROM. Both keys must be pressed to cause a restart. The order is not significant since the restart occurs when either key is released.

ATTENTION
Momentary contact switch which controls a status bit that may be tested by the processor.

INTERRUPT
Momentary contact switch which controls a status bit that may be tested by the processor. Used in conjunction with the RESTART key to effect a processor initialization.

KEYBOARD
Momentary contact switch which controls a status bit that may be tested by the processor.

DISPLAY
Momentary contact switch which controls a status bit that may be tested by the processor.

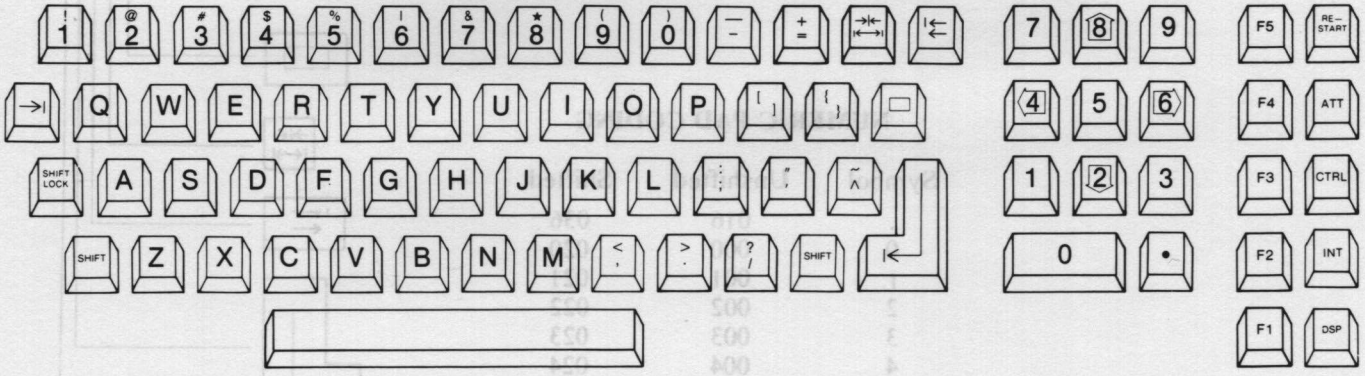
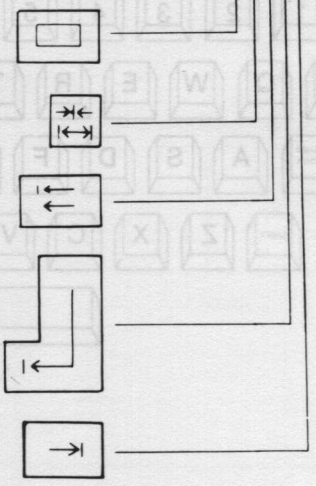


Figure 2-1 1560 Multipurpose Keyboard Layout

Table 2-1
Multipurpose Keyboard Coding (ASCII and Word Processing)

A - 101	a - 141	0 - 060	: - 072
B - 102	b - 142	1 - 061	; - 073
C - 103	c - 143	2 - 062	< - 074
D - 104	d - 144	3 - 063	= - 075
E - 105	e - 145	4 - 064	> - 076
F - 106	f - 146	5 - 065	? - 077
G - 107	g - 147	6 - 066	@ - 100
H - 110	h - 150	7 - 067	[- 133
I - 111	i - 151	8 - 070	] - 135
J - 112	j - 152	9 - 071	^ - 136
K - 113	k - 153	Space Bar - 040	_ - 137
L - 114	l - 154	! - 041	{ - 173
M - 115	m - 155	" - 042	| - 174
N - 116	n - 156	# - 043	} - 175
O - 117	o - 157	$ - 044	~ - 176
P - 120	p - 160	% - 045	
Q - 121	q - 161	& - 046	
R - 122	r - 162	' - 047	
S - 123	s - 163	(- 050	
T - 124	t - 164	) - 051	
U - 125	u - 165	* - 052	
V - 126	v - 166	+ - 053	
W - 127	w - 167	, - 054	
X - 130	x - 170	— - 055	
Y - 131	y - 171	. - 056	
Z - 132	z - 172	/ - 057	

Tab - 033 (030 shifted)
Return - 015 (035 shifted)
Backspace - 010 (013 shifted)
Insert - 037
Delete - 177
Command - 134 (140 shifted)
F5 - 200 (212 shifted)
F4 - 214 (202 shifted)
F3 - 216 (204 shifted)
F2 - 220 (206 shifted)
F1 - 222 (210 shifted)



NUMERIC PAD CODING

Symbol	Unshifted	Shifted
.	016	036
0	000	020
1	001	021
2	002	022
3	003	023
4	004	024
5	005	025
6	006	026
7	007	027
8	011	031
9	012	032

*** All characters are represented in octal.**

PART 3
DISPLAY

3.1 General Description

The Datapoint 1560 uses a magnetically deflected CRT. It provides for the display of 1920 characters organized as 24 lines of 80 characters each. It is refreshed from the processor memory through a direct memory access (DMA) channel under processor control. The display character generator is loadable, allowing software definition of the character set; it also incorporates an inverse video feature that displays characters as dark dots on a light background on a character by character basis (see Figure 3-1), under program control. Up to 128 different individual 5x7 dot matrix characters may be produced.

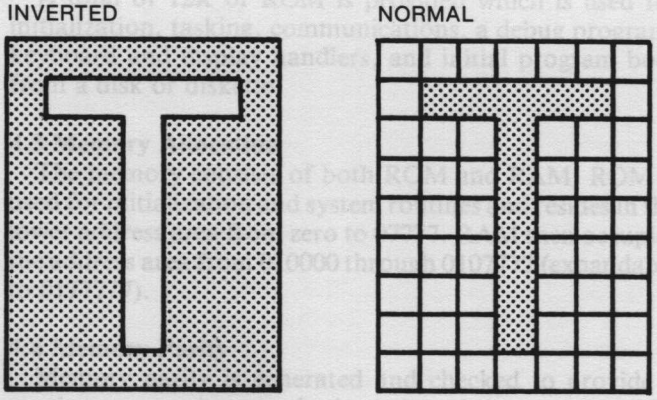
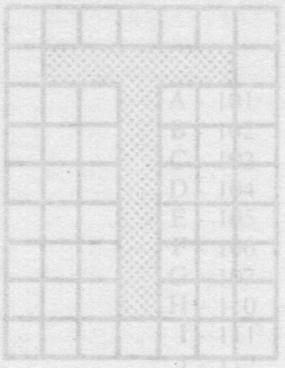
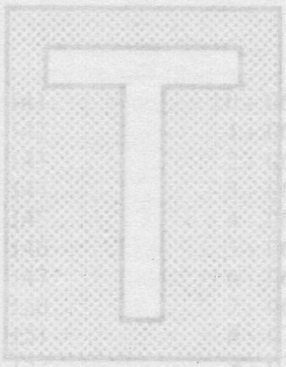


Figure 3-1 Inverted and Normal Characters





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PART 4
MEMORY

4.1 General Description

The 1560 contains 64K bytes of RAM memory, expandable to 128K. This memory is organized in 9 bit words (8 data + parity) and is composed of N channel MOS random access memory (RAM) and MOS read only memory (ROM). Due to the dynamic nature of the RAM used, it is necessary to periodically refresh the data in memory. This is performed automatically by the CPU, eliminating any additional overhead for refresh. The parity track allows for automatic detection of memory errors to prevent inadvertant operation with faulty memory. Parity is not checked during the DMA function, or when reading from ROM. When reading from non-existent memory, data will be all ones with correct parity.

4.2 Memory Specifications

RAM memory is provided on 64K cards. These cards provide a memory system with the following characteristics:

Memory type	MOS random access
Memory cycle time	630 nanoseconds
Memory access time	300 nanoseconds

A total of 12K of ROM is provided which is used for initialization, tasking, communications, a debug program, keyboard and display handlers, and initial program boot from a disk or diskette.

4.3 Memory Allocation

The memory consists of both ROM and RAM. ROM is used for initialization and system routines and resides in the lower address area from zero to 07777. RAM then occupies the address area from 010000 through 0107777 (expandable to 0177777).

4.4 Memory Parity

Memory parity is generated and checked to provide a continuous monitor on the integrity of the memory. If a memory parity error is detected, the processor is interrupted via a non-maskable interrupt which will normally post the error condition on the display and jump to the debug program. The particular action taken can be changed by the user program. Parity is not checked when reading data for the display, or from ROM.

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PART 5
MICROBUS INTERFACE

5.1 General Description

The microbus is an external bus that provides interface between the processor and as many as ten peripheral devices. The microbus handles block data transfer rates of 175K bytes per second. Maximum block length is 256.

The microbus is composed of an eight-bit command and address bus, an eight-bit bi-directional data bus, two command strobes, an interrupt acknowledge strobe, an interrupt request line, and a +5 volt power indication.

5.2 Microbus Signals

The microbus provides four bits of peripheral device address (A0-A3). Four command lines provide unique commands for each of two transfer strobes (USTB 1 & 2). A third strobe (IACK) is used to acknowledge an interrupt request. The content of the command and address lines is not defined during the IACK strobe. Decoding of the peripheral device address lines is determined by jumpers in each device. No two devices may have the same address on the same microbus.

The eight bi-directional lines are used to transfer data to and from the peripheral device under control of the processor. The drivers are open collector type and are enabled only during a write cycle. The data drivers in the peripheral device are active only when commanded to be by the processor.

5.3 Microbus Timing

The address, command, and data lines are stable for at least 100 ns before the leading edge of the transfer strobe, and remain so for at least 100 ns after the trailing edge. The transfer strobes are a minimum of 400 ns wide. During a microbus input cycle, the peripheral device will put stable data on the data lines at least 100 ns prior to the end of the transfer strobe and hold it for 100 ns after the end of the transfer strobe.

Interrupt ACKnowledge (IACK) strobe is propagated through each peripheral in a daisy chain fashion.

5.4 Microbus Input/Output Cycles

During an output cycle the address, command register, and data lines are loaded with the appropriate information and the bus drivers enabled. A transfer strobe is then generated. The peripheral device, by decoding the address lines, determines if the command and data information is to be latched, and completes the transfer on the trailing edge of the transfer strobe.

During an input cycle the command and address register is loaded with the appropriate information and a transfer strobe generated. The peripheral device, by decoding the address and command information, determines what information to place on the data bus. The peripheral device disables its bus drivers after detecting the trailing edge of the transfer strobe.

The peripheral device completes the specified command and is ready to accept additional commands at the rate of one every two microseconds. Commands requiring longer than this are associated with a busy status bit.

5.5 Microbus Interrupt Cycle

An interrupt cycle is initiated whenever a peripheral device pulls the microbus Interrupt REQuest (IREQ) line low. The processor may respond at any time to the IREQ by initiating the microbus IACK strobe. The IREQ line is independent of all other activity on the microbus.

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PART 6
DATA COMMUNICATIONS CHANNELS

6.1 General Description

The basic 1560 provides two serial communications channels. One channel (Channel I) is either synchronous or asynchronous and is provided for communication with a host system. Baud rates are programmable from 50 to 9600 baud when operating in asynchronous mode or external clock only for synchronous operation. The second channel (Channel II) is provided for local printer support under processor control but can be used as a second communications channel.

The Multifunction Communications Interface (MFC) provides an RS-232C-compatible serial Channel A that has the capability of extending the existing byte-oriented communication protocol support to handle bit-level protocols (SDLC, CCITT X.25, ISO HDLC). Support is also included for a second serial Channel B that supports asynchronous communication. Both channels will be brought out to one connector. Utilization of Channel B will require a special external "Y" cable adaptor (shown in Figure 6-1). The Multifunction Communications Interface is optional.

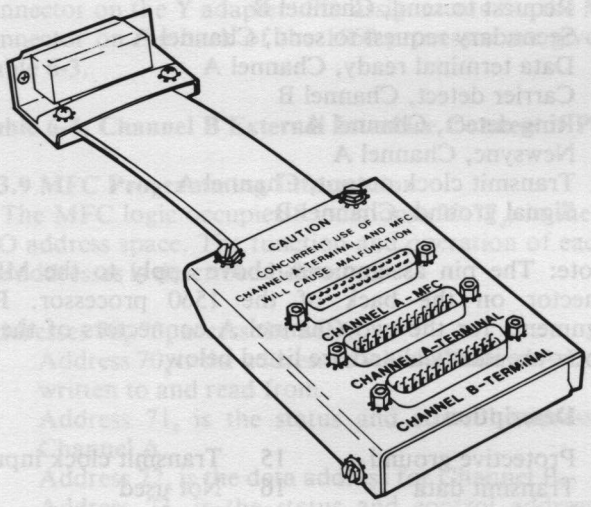

Figure 6-1 "Y" Connector

6.2 Standard Communication Channel Implementation

The serial communications channels are implemented with type 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chips which are capable of operating with a wide variety of serial communications formats. The 8251 supports basic data set control signals, and all but the supervisory channel command signals of the signalling described in EIA specification RS-232C. Therefore, one input and two output ports are assigned for auxiliary modem control signals in the 1560. One communications channel carrier can detect carrier, ringing, and secondary channel carrier while the other can only detect carrier. One channel can control Newsync and the Secondary Channel Request To Send while the other can control neither.

The main channel carrier detect, ring detect, and secondary channel carrier detect status bits are assigned to bits 0, 1, and 2 of port 016, respectively. The printer channel carrier detect status is assigned to bit 4 of the same port. The capability to detect Newsync and secondary channel request to send are assigned to bit 0 of ports 016 and 017, respectively.

6.3 Multifunction Communication Interface Implementation

6.3.1 Dual Channel Communication Controller

The MFC device functions as the communication controller for both channels. Channel A occupies I/O addresses 70_8 (Data) and 71_8 (Control and Status). Channel B (Async only) occupies I/O addresses 72_8 (Data) and 73_8 (Control and Status).

6.3.2 Baud Rate Generator

A counter/timer/controller (CTC) device functions as a baud rate generator when internal clocking is required for the communication controller. Refer to Table 6-1 for detailed information.

Nominal Baud Rate	Synchronous Divisor	(X1 Clock) Actual Baud Rate	Asynchronous Divisor	(X16 Clock) Actual Baud Rate
9600	16	9600	1	9600
4800	32	4800	2	4800
2400	64	2400	4	2400
2000	77	1994.8	5	1920
1800	85	1807	8	1200
1200	128	1200	11	872.2
880			16	600
600			22	435.4
440			32	300
300			44	218.2
220			64	150
150			71	135.2
134.5			87	110.3
110			128	75
75			145	66.2
66			160	60
60			192	50
50				

Table 6-1. Available Baud Rates for Communications Channels

6.3.3 Extended Communication Control and Status Logic

This logic adds software controlled outputs and software readable inputs to extend the capability of Channel A beyond that of the MFC communication controller. This logic also allows programmable selection of transmit and receive clock sources for each channel. The combinations are defined in Table 6-2.

BIT5	BIT6	
0	0	CHAN B TRANSMIT CLOCK
0	1	CHAN A TRANSMIT CLOCK
1	0	CHAN A RECEIVE CLOCK
1	1	CHAN B TRANSMIT CLOCK DIVIDED BY 8

Table 6-2. Source of Channel B Receive Clock

6.3.4 External Interface Logic

This circuitry provides the RS-232C to TTL conversion for inputs and TTL to RS-232C conversion for outputs.

6.3.5 Data Encode/Decode Logic

This circuitry provides the capability of transmitting and receiving data in either an NRZ or NRZI format. The NRZ/NRZI selection is performed under software control.

6.3.6 Diagnostic Loopback Logic

Provision has been made for a software controllable loopback of transmit signals to receive signals for diagnostic purposes. This same loopback function may also be provided by an external loopback plug. An LED indicator is illuminated when the board is in a diagnostic loopback mode to provide visible feedback during burn-in or field troubleshooting.

6.3.7 Channel A External Interface

All external drivers and receivers are electrically compatible with the two existing communication ports on the processor PCB as well as EIA Standard RS-232C. The basic functions of the interface signals are described for an SDLC mode of operation. Since most are under software control, their exact function for various applications may vary.

TxD-A (Transmit Data Channel A)-Serial output data in the selected NRZ/NRZI format.

RxD-A (Receive Data Channel A)-Serial input data that is processed according to the selected NRZ/NRZI format.

RTS-A (Request to Send Channel A)-Control output to the data communication equipment (DCE) indicating that the 1560 desires to initiate transmission.

CTS-A (Clear to Send Channel A)-Status input from the DCE in response to RTS indicating to the 1560 that communication may begin.

DTR-A (Data Terminal Ready Channel A)-Control output to the DCE indicating that the 1560 is in a ready state. Bringing this line false on a dialup line hangs up the phone.

DSR-A (Data Set Ready Channel A)-Status input from the DCE indicating that it is powered up and ready.

CD-A (Carrier Detect Channel A)-Status from the DCE indicating that a carrier has been detected on the telephone line.

RI-A (Ring Indicator Channel A)-Status from the DCE indicating that a ring has been detected (used for auto answer applications).

TXCI-A (Transmit Clock Input Channel A)-A clocking signal from the DCE to output transmit data when external clocking has been selected.

RXCI-A (Receive Clock Input Channel A)-A clocking signal from the DCE to input receive data.

TXCO-A (Transmit Clock Output Channel A)-A clocking signal from the 1560 to the DCE. If internal clocking is selected the source is the internal CTC and if external clocking is selected this is just the transmit clock input turned around.

SEC CD-A (Secondary Carrier Detect Channel A), SEC RTS-A (Secondary Request to Send Channel A)-These signals provide the same functions as CD and RTS except on a second channel of the DCE.

New Sync-A (Channel A)-This signal is not required for most configurations but is available for IBM compatibility.

Pin	Description
1	Protective ground
2	Transmit data, Channel A
3	Receive data, Channel A
4	Request to send, Channel A
5	Clear to send, Channel A
6	Data set ready, Channel A
7	Signal ground, Channel A
8	Carrier detect, Channel A
9	Not used
10	Not used
11	Data terminal ready, Channel B
12	Secondary carrier detect, Channel A
13	Clear to send, Channel B
14	Transmit data, Channel B
15	Transmit clock input, Channel A
16	Receive data, Channel B
17	Receive clock input, Channel A
18	Request to send, Channel B
19	Secondary request to send, Channel A
20	Data terminal ready, Channel A
21	Carrier detect, Channel B
22	Ring detect, Channel A
23	Newsync, Channel A
24	Transmit clock output, Channel A
25	Signal ground, Channel B

Note: The pin assignments above apply to the MFC connector on the back of the 1560 processor. Pin assignments for the two Channel A connectors of the Y adapter are identical and are listed below.

Pin	Description	Pin	Description
1	Protective ground	15	Transmit clock input
2	Transmit data	16	Not used
3	Receive data	17	Receive clock input
4	Request to send	18	Not used
5	Clear to send	19	Secondary request to send
6	Data set ready	20	Data terminal ready
7	Signal ground	21	Not used
8	Carrier detect	22	Ring detect
9	Not used	23	Newsync
10	Not used	24	Transmit clock output
11	Not used	25	Not used
12	Secondary carrier detect		
13	Not used		
14	Not used		

Table 6-3. Channel A External Interface Connector Pins

6.3.8 Channel B External Interface

The Channel B signals that are utilized have the same functions as their Channel A counterparts. The signals implemented are listed below:

TxD-B	(Transmit Data Channel B)
RxD-B	(Receive Data Channel B)
RTS-B	(Request to Send Channel B)
CTS-B	(Clear to Send Channel B)
DTR-B	(Data Terminal Ready Channel B)
CD-B	(Carrier Detect Channel B)

Pin	Description
1	Protective ground
2	Transmit data
3	Receive data
4	Request to send
5	Clear to send
6	Not used
7	Signal ground
8	Carrier detect
9-19	Not used
20	Data terminal ready
21-25	Not used

Note: The pin assignments above are for the Channel B connector on the Y adapter. Pin assignments for the MFC connector on the back of the 1560 processor are given in Table 6-3.

Table 6-4. Channel B External Interface Connector Pins

6.3.9 MFC Programming Information

The MFC logic occupies 8 locations (70-77$_8$) in the Z80 I/O address space. The function and operation of each of the addresses is described below.

Addresses 70$_8$-73$_8$ access the MFC.

Address 70$_8$ is the address to which Channel A Data is written to and read from.

Address 71$_8$ is the status and control address for Channel A.

Address 72$_8$ is the data address for Channel B.

Address 73$_8$ is the status and control address for Channel B.

Address 74$_8$ is used to access CTC Channels 0 and 2. If address 76$_8$ BIT 7 is a 0, CTC Channel 0 will be accessed and if address 76$_8$ BIT 7 is a 1, then CTC Channel 2 is addressed. Address 75$_8$ is used to access CTC Channels 1 and 3. The Channel selected will depend upon the state of Address 76$_8$ BIT 7.

Address 76$_8$ is an extension port to handle communication functions not handled by the MFC. The functions of each bit are described below:

Bit	Functions
0	Secondary Request to Send (Channel A)
1	New Sync (Channel A)
2	Select NRZ Transmit/Receive Mode when Set (Channel A) Select NRZI Transmit/Receive Mode when Clear
3	Select Internal Receive Clock when Set (Channel A) Select External Receive Clock when Clear
4	Select Internal Transmit Clock when Set (Channel A) Select External Transmit Clock when Clear
5	Channel B Baud Rate Select 0
6	Channel B Baud Rate Select 1 (see Table 6-2 for Baud Rate combinations)
7	Select CTC Channels 2 and 3 when Set Select CTC Channels 0 and 1 when Clear (see address 74$_8$ and 75$_8$ and vendor data sheet)

There is a restriction on the baud rates that may be used with channel B (Bits 5 and 6). The transmit clock for channel B may be any of those shown in Table 6-2. However, the receive baud rate may have only one of four possibilities:

- it may be the Channel B transmit baud rate
- it may be the Channel B transmit baud rate divided by 8
- it may be the Channel A transmit baud rate
- it may be the Channel A receive baud rate

Address 77$_8$ is a diagnostic control and status port with the bit definitions used below:

Write Function
Bit 0-1 = Loopback
-0 = Normal
Bit 1-7-Not Used

Read Function
Bit 0-State of Loopback/Normal
Bit 1—4 Not Used
Bit 5-State of Secondary Carrier Detect
Bit 6-State of Ring Indicator
Bit 7-State of Data Set Ready

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PART 7
LOCAL NETWORK INTERFACE OPTION

7.1 General Description

The 1560 RIM interfaces with the 1560 processor and the ARCNET local network. Functional descriptions of each are given below to promote a better understanding of the operation of the 1560 RIM.

7.2 1560 RIM

The integrated RIM circuit, memory interface, local network link interface, and buffer memory are described in the following sections.

7.2.1 Integrated RIM Circuit

The integrated RIM circuit is a custom integrated circuit chip that embodies the intelligence of the 1560 RIM. It is a special purpose communications circuit designed to provide a high speed communication link between computers tied together in a local network. The integrated RIM circuit responds to processor commands, handles the transmission and reception of messages over the network, and manages the communications protocol on the network.

7.2.1.1 Sequencer

The integrated RIM circuit is driven by an internal ROM based sequencer that causes the circuit to execute the internal microcode. Instructions are either one or two bytes long, and execute in 400 ns. The sequencer is reset to zero when 1560 Power On Restart (POR) is active.

7.2.1.2 Controller Bus and Registers

The integrated RIM circuit has two 8-bit internal buses. Data sources for the buses are the buffer memory, the microcode, the CRC logic, and internal registers. Selectable destinations are the buffer memory and internal registers. The registers are used to latch memory address and data, the 1560 RIM ID number, the NID, and to shift data to and from the local bus.

7.2.1.3 Network Data Transmission and Reception

The transmitter bit rate is synchronized to the clock frequency; i.e., one bit is transmitted during each 400 ns microinstruction. Data to be transmitted are loaded into the 8-bit shift register and shifted out to the transmit/receive module. Since there is no buffering, the shift register is loaded every 3.2 usec to assure that valid data is always present in the shift register. Data received from the transmit/receive module are synchronized with the clock and shifted into the shift register. When 8 bits have been received, the byte is transferred through the holding register to the buffer memory.

7.2.2 Memory Interface

The memory interface consists of address and data buses, control signals, and power supply lines.

7.2.2.1 Address Bus

The 1560 memory address bus (M0 to M17) is an 18-bit bus that is created from the 16 bit Z80A address bus and a 16 byte sector table. The sector table allows segmenting of the 256K byte address space into 4K byte sectors. Sixteen sectors are available to the processor at any one time as determined by the data loaded into the sector table. The top 4K bytes of address space (3F000H to 3FFFFH) have been allocated for use by the 1560 RIM.

7.2.2.2 Data Buses

The Z80A bi-directional data bus is separated into an output data bus and an input data bus at the memory interface in the 1560 processor. The output data bus (D0 to D7) is active low. The input data bus (MD0 to MD7) is active high. A vertical parity bit is generated on the output data bus for each byte of data transferred. A vertical parity bit is expected with each byte of input data. Parity on input is tested and a nonmaskable interrupt is initiated if an error is detected.

7.2.3 Local Network Link Interface

The link interface contains the logic necessary to connect the integrated RIM circuit to the local network. This logic consists of three major functional groups: the transmitter, the receiver, and the clock generation.

7.2.3.1 Link Interface-Transmitter Function

The input to the transmitter logic is the TX signal from the integrated RIM circuit which consists of a series of 200 ns negative pulses, to represent ONE bits, at a 2.5 Megabaud rate. A ZERO bit is represented by the absence of a pulse. When no data is being transmitted, the TX line is held at a high level. The transmitter logic converts each TX pulse to a bipolar pulse and a transformer couples these pulses to the local network coaxial cable.

7.2.3.2 Link Interface-Receiver Function

The same transformer which couples the transmitter to the local network also couples any bipolar pulse signals from other processors to the receiver section. This function consists of a special filter, a line receiver, and synchronizing logic. The filter is tuned to the characteristics of the bipolar pulse to provide a maximum signal to noise ratio. The signal is processed and sent to the integrated RIM circuit as the RX signal.

7.2.3.3 Link Interface-Clock Generation

The clock generation logic contains a 20 Megahertz crystal oscillator which produces two separate clock signals to the integrated RIM circuit: CLK and CA. The CA clock signal also drives the transmitter portion of the link interface. The 20 Megahertz signal clocks the receiver logic in the link interface.

7.2.3.4 RIM Transceiver Circuit

Much of the logic described in paragraphs 7.2.3.1 to 7.2.3.3 above is implemented in a gate array circuit called a RIM Transceiver.

7.2.4 Buffer Memory

The 1560 RIM interface module contains a 1024-byte random access buffer memory. Read/write control to the buffer memory is provided by the integrated RIM circuit. Data transfer is to/from the 1560 over the processor bus or to/from the local network.

7.2.4.1 Buffer Memory Organization

The buffer memory is segmented into four 256-byte segments. This provides full double buffering for both the transmitter and receiver. When transferring data to/from the local network, memory addresses are provided by the integrated RIM circuit. When transferring data to/from the 1560, memory addresses are obtained from the processor address bus. The buffer memory control signals come from the integrated RIM circuit in either case.

7.2.4.2 Buffer Memory Arbitration

Since access to the buffer memory by the integrated RIM circuit and the 1560 processor is asynchronous, arbitration is required. Access to the memory is on a first-come, first-served basis unless access requests occur simultaneously in which case the 1560 processor receives priority. The RIM generates a WAIT signal back to the 1560 processor in order to obtain the time necessary to access the buffer memory. All memory access requests are serviced within 2.2 usec.

7.3 Local Network

The local network is a high speed, special purpose, inter-processor communication link. Data is transmitted over a coaxial cable at 2.5 Megabaud in a unique format. Each processor on the network has a unique identification code. The network is self-polling, and packets of data are moved between processors using the identification codes for addresses. A single network will support up to 255 processors.

7.3.1 System Configuration

A minimum network consists of two processors connected with one coaxial cable up to 2000 feet apart. Up to four processors may be interconnected as one network with the use of a four-port passive hub. However, the use of the passive hub reduces the maximum permissable cable length between any two processors to 200 feet. For networks with more than four processors or separations greater than 200 feet, active hubs are used. Any number of active hubs may be used in the network with the following restrictions: maximum cable length between active hubs or active hubs and processors is 2000 feet, there may be no more than ten active hubs between any two processors and active and passive hubs may not be intermixed. Active hubs are available in 8-port and 16-port versions.

7.3.2 Network Connection

Each processor has a BNC receptacle for attachment to the local network. Interconnection is by means of RG62/U coaxial cable with BNC cable plugs. Transmission line impedance is 93 ohms nominal. Any number of processors may be powered down while still connected to the network without affecting the network integrity or communication between processors that are powered up. All active hubs must be powered up for full network operation. An active hub that is powered down or has failed typically affects only a portion of the network, allowing the remainder of the network to continue normal operation.

7.3.3 Network Transmission

Transmission of data on the network is by means of on/off keyed bipolar pulses. ONE bits are represented as a bipolar pulse and ZERO bits by the absence of a bipolar pulse. Pulses occur at a uniform rate of 2.5 Megabaud. Data transmissions are coded as eleven-bit characters consisting of two ONE bits, a ZERO bit, and 8 bits of ASCII (or binary) data. Characters are formatted into packets of variable length, 253 data characters maximum, for transmission. Each packet starts with an ALERT burst consisting of six ONE bits. The only other type of transmission allowed is the reconfiguration burst, which consists of a sequence of 8 ONE bits and one ZERO bit repeated 765 times.

7.3.4 Network Protocol

The network protocol is made up of five types of packets. Included in the various packets are data characters or special characters. There are seven special characters: End of Transmission (EOT), Enquiry (ENQ), Start of Header (SOH), Acknowledgement (ACK), Negative Acknowledgement (NAK), Source Identification Code (SID), and Destination Identification Code (DID). The packet types are described below.

Invitation to Transmit-An ALERT burst followed by three characters; an EOT and two DID characters. The Invitation to Transmit is used to pass control of the line from one processor to another.

Free Buffer Enquiry-An ALERT burst followed by three characters; an ENQ and two DID characters. The Free Buffer Enquiry is used to ask a processor if it is able to accept a data packet.

Data Packet-Data packets can have from one to 253 data characters. The beginning of a data packet has an ALERT burst followed by an SOH character, an SID character and two DID characters. The four header characters are followed by the COUNT character then the data characters. The last two bytes of a data packet are two Cyclic Redundancy Check Characters (CRCC). The COUNT is the two's complement of the number of data characters.

Acknowledgement-An ALERT burst followed by one character, the ACK. The Acknowledgement is used to confirm reception of a data packet and as an affirmative response to a Free Buffer Enquiry.

Negative Acknowledgement-An ALERT burst followed by one character, the NAK. The Negative Acknowledgement is used as a negative response to the Free Buffer Enquiry.

7.3.5 Data Exchange

When a processor receives an Invitation to Transmit it checks to see if a packet is ready for transmission. If not, it forwards an Invitation to Transmit to the processor with the next higher identification code. Otherwise, it sends a Free Buffer Enquiry to the processor whose ID equals the DID of the data packet it wants to transmit. If the response is an ACK, the packet is transmitted. If the response is a NAK, it then sends an Invitation to Transmit to the next processor, and waits until it receives another Invitation to Transmit before attempting to send its data packet. When a processor receives a Free Buffer Enquiry, it responds with an ACK or a NAK depending on whether its buffer is available to receive a packet. Upon receipt of a data packet, the receiving processor will check the length and CRC. If

both are correct, an ACK is sent; otherwise, the packet is ignored. If a transmitting processor does not receive an ACK to a data packet transmission, it sends an Invitation to Transmit to the next processor. It tries again to transmit the packet next time it gains control of the bus.

7.3.6 Broadcasts

In addition to data packet exchanges between two processors, the network protocol allows a processor to broadcast a data packet to all other processors that are enabled for broadcast reception. A data packet is converted to a broadcast data packet by setting the DID characters to null (all bits zero). No ACK packets are sent in response to a Broadcast data packet.

7.3.7 Reconfiguration

When a processor is first powered up on the network or when it has not received an Invitation to Transmit for 0.84 seconds, it will initiate a system reconfiguration by sending a RECON burst. This burst will terminate all activity on the network. Each processor on the network will go into a time-out state following the RECON burst. The duration of time-out for each processor is a function of its identification code. The processor with the largest code will time-out first, and begin sending Invitations to Transmit. This activity will prevent other processors from timing out. The first Invitation to Transmit is sent to the next higher address (modulo 256), and if line activity is not detected, the DID is incremented and the process is repeated until line activity is detected. That DID becomes the NID (next ID) for the first processor, the next processor repeats the process, and so on until all processors have received an Invitation to Transmit and had an opportunity to determine their NID. The NID is different for each processor and remains constant until the next network reconfiguration.

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APPENDIX A
SYSTEM ROM DEBUG

A.1 General Description

The Datapoint 1560 contains diagnostic programs which reside in the ROM memory. These programs are designed to provide the user with a method of determining the nature of basic faults in the processor.

A.2 Startup Procedure

The following conditions may cause entry to the diagnostic programs:

- Manual intervention
- Breakpoint embedded in the user's program
- Breakpoint set by the diagnostic system
- Certain hardware errors

To force entry into the diagnostic system, depress in sequence DSP, INT, and RESTART, keeping each key depressed until all three are down. Then release INT or RESTART. This will bring up the diagnostic system display and commands may be entered.

The diagnostic system operates as a task, just as all the other tasks in the system, although of higher priority. Thus while the diagnostic program is in the wait state, other tasks may be running.

A.3 Display Format

The diagnostic display consists of four lines and occupies the lower right corner of the screen.

AAAAAA	:CURADR (Current Address)
* NNN	:ASCII, 8-bit octal value at CURADR
MMMMMM	:LSB,MSB address formed at CURADR
nnnnnnn*	:Command interpreter

The top line shows the current sixteen-bit address.

The second line contains both an ASCII (one character shown as *) and an 8-bit octal (three characters shown as NNN) representation of the contents of the current address byte.

The third line contains an octal representation of the 16-bit value whose LSB is at CURADR and whose MSB is at CURADR + 1.

The bottom line of the display is an interpreter used to input commands to the diagnostic program. The blinking cursor signifies that the Command Interpreter is awaiting user input.

Data is entered serially into the input display buffer. The cursor is displaced to the right successively as data is entered. The backspace key erases the character most recently entered, shifting the entry cursor to the left one space. The cancel key deletes the entry. All commands are terminated by the enter key.

All commands are single characters. Commands which accept input arguments are preceded by the argument, which is entered in octal. Not all commands require an input argument. Illegal input is ignored, evoking a beep. Commands are executed when the enter key is depressed, after the entire command has been entered.

A.4 Command Syntax

Diagnostic commands use the following notation:

nnnnn...	Indicates an optional sequence of octal digits not to exceed the number of n's given. If input argument contains more than eight bits of significance, special results will occur. Usually two bytes of memory will be affected by the command, either a register pair or a memory address in LSB,MSB format.
12345	There are several special commands whose accidental execution is inhibited by the requirement that they contain this unique argument.

A.5 Debug Command List

Note: If a debug diagnostic routine is entered before the 1560 has booted, the "12345R" command must be executed before a "J" or "C" command is executed.

n A	Align the diskette head
nnnnnn B	Set a breakpoint at the given or current address
nnnnnn C	Call the given or current address
nnnnnn D	Decrement the current address
E	Continue execution
nnn F	Fill the screen with the given value
G	Display general communications channel status
H	MFC loopback test
nnnnnn I	Increment the given or current address
nnnnnn J	Jump to the given or current address
K	Key in on top line of screen
nnnnnn L	Link to the given address or the address pointed to by the current address
(nnn)nnn M	Modify the contents of the location pointed to by the current address
N	Sets the current address to that of a two-byte area containing the number assigned to the interrupted task
12345 O	Initiate a loopback test
P	Display the printer channel status
12345 R	System reset command
nnn S	Display the specified stack item
12345 T	Start memory test
n V	Diskette verification
n X	Start continuous diskette controller buffer test
n Z	Diskette track 0 sensor alignment
(nnn)nnn a	Display or update the contents of the A register
nnn b	Display or update the contents of the B register
(nnn)nnn c	Display or update the contents of the C register
nnn d	Display or update the contents of the D register
(nnn)nnn e	Display or update the contents of the E register
nnn f	Display or update the contents of the flag register

(nnn)nnn g	Write given command to general communications channel
nnn h	Display or update the contents of the H register
(nnn)nnn l	Display or update the contents of the L register
(nnn)nnn p	Write given command to printer channel
nnnnnn x	Display or update the contents of the IX register
nnnnnn y	Display or update the contents of the IY register
(nnn)nnn .	The equivalent of an M followed by an I
nnnnnn <enter>	Change the current address
#	Clear breakpoint
<	Input a character from the channel last selected by a P/G or p/g command
nnn >	Output a character from the channel last selected by a P/G or p/g command
?	Identify the firmware version number

A.6 Hardware Errors

There are certain error conditions which are detected in the hardware which may cause the diagnostic display to come up. If these occur, a line appears above the diagnostic display indicating the type of error. Some of these are caused by software conditions but are indicated as hardware errors. These errors are indicated as follows:

LRA ERR	This is caused by an internal error in a system program and is generated by an attempt to load the refresh register in the processor. The firmware traps and generates this error.
MEM ERR	This indicates that the system detected a parity error in the memory. This is a true hardware error. To attempt to clear it, the machine should be powered off and back on. Run the memory test (12345T), and place a service call.
KBD ERR	This is another error which is generally caused by an error in a system program. It is caused by the firmware not being able to service the keyboard often enough, generally because of an interlock situation.
NMI ERR	No source could be identified for the non-maskable interrupt. This only happens when a program accidentally transfers control to the interrupt handler.
CHAN X MFC ERR	Any error detected by the firmware MFC test will display this message. The "X" indicates failing channel A or B.

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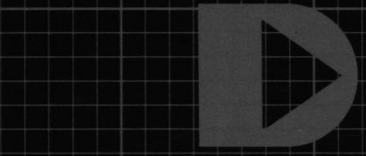
DATAPOINT