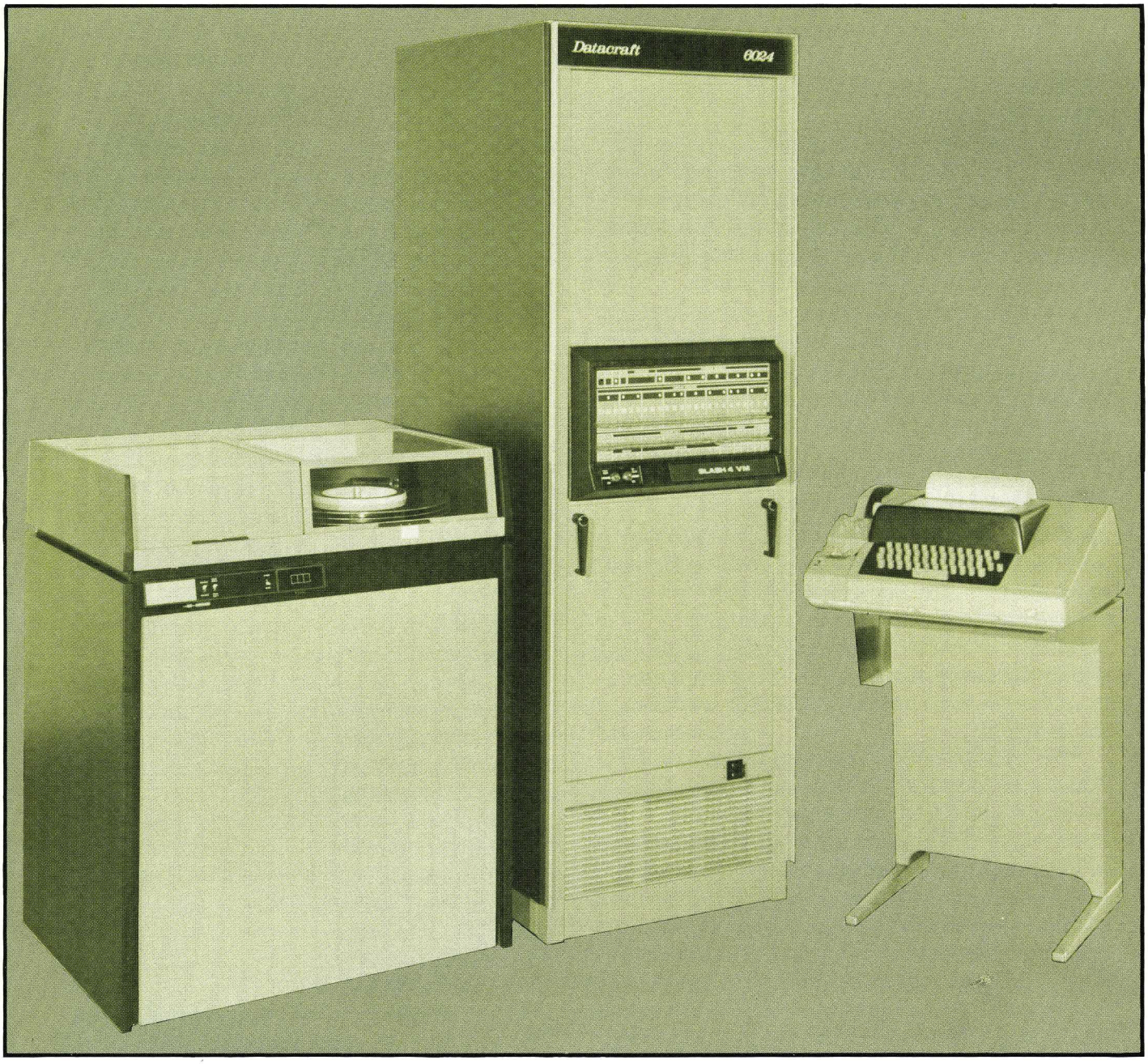

THE SLASH 4VMS

VIRTUAL MEMORY SYSTEM

PRODUCT BULLETIN

FEATURES

- Demand Paging
- Main Memory Segmentation
- Optimal Memory Allocation
- High-Speed Program Relocation
- Addressing to 263,144 words
- Execution of Programs Larger than Available Storage

Datacraft®

The SLASH 4VMS combines the most powerful member of Datacraft's family of real-time computers, the SLASH 4, with the flexibility of a highly efficient and effective Virtual Memory System.

The versatility of the SLASH 4 high-speed processor to handle real-time, time-sharing and batch scientific applications is now enhanced by the addition of the VMS capability. The new addition allows for the transfer of user programs and data in 1K (1024 words) segments — called pages — between main memory and an external mass storage device under system control. This operation, termed "demand-paging," is of necessity to meet the increasing demands of real storage space required by applications programs being run.

The demand-paging technique utilized by the SLASH 4 VMS allows a program's memory area to be discontiguous in main memory core and, in fact, to permit portions of the program to be absent from main core while the program is running. This permits the maximum utilization of available memory at any time and allows the computer to run a program larger than the physical memory available within the machine.

The SLASH 4VMS operates in two modes: "User and Monitor". In the User Mode, all memory references are mapped and the mapping algorithm produces an 18-bit address of 256 pages. In the Monitor Mode, all memory references are direct, i.e., the mapping function is disabled and the paging address registers are not used. Operation in this mode is identical to that of all Datacraft computers. A program may reference data to a maximum of 263,144 words due to the 18-bit indirect addressing capability, although limited to 65,536 words of executable code.

A minimum SLASH 4VMS system includes: 96K bytes of core memory, hardware paging, parity, hardware multiply/divide/square root, bit processor, priority interrupt control system, eight external priority interrupts, five registers (three index), stall alarm, 120 Hz clock, 8-bit integrated controller channel, 24-bit I/O channel, chain block controller, CRT, 200 LPM line printer, 300 CPM card reader, and a 10.8M byte disc with bootstrap.

Available as optional features are enhancements that configure the SLASH 4VMS to your requirements. Features such as the Scientific Arithmetic Unit providing floating point hardware, for the rapid execution of double-precision floating-point arithmetic (39-bit mantissa plus 8-bit exponent). Also an incremental memory system of high-speed semiconductors and magnetic core further augments the basic SLASH 4. The semi-conductor memory is available as a 24K or a 96K byte, multi-port unit featuring a cycle time of less than 150 nanoseconds. For critical real-time requirements, the semiconductor memory with I/O processor serves to further increase throughput.

Featured with the SLASH 4VMS software is a Virtual Core Management Operating System (VULCAN). A demand paging, priority structured multi-programming system. VULCAN can be configurable as a multi-level batch processing system, an interactive terminal time-sharing system, and a real-time operating system all supported concurrently in a normal configuration.

Completely compatible with the entire family of Datacraft computers, our additional field proven software library includes five languages, five operating systems and six support packages. The facility for concurrent real-time, time-sharing and batch processing is a unique, Datacraft, software plus.

Compatability is again underscored in the input/output structure. Because Datacraft I/O design is consistent with the entire computer family, a fully developed, comprehensive peripheral product line is available immediately.

A wide variety of optional features are available with the Virtual Memory System. Factory installed or ready for field-installation, the SLASH 4VMS capabilities can be extended to satisfy individual requirements.

OPTIONS

Chain Block Controllers (CBC) and External Block Controllers (XBC).
Up to 48 Vectored External Interrupts (can also be triggered under Software Control).
Up to four Hardware Bootstraps.
Interval Timer. (Real-time clock).
Power Failure Shutdown and Restart.
Address Trap.
Up to 768K bytes of memory.
Scientific Arithmetic Unit (Hardware Floating Point Processor).
Semiconductor Memory, in 24K or 96K bytes, multi-port.
I/O Processor interface to semiconductor memory with up to 4 I/O Processors.

TECHNICAL SPECIFICATIONS

Instruction Timing (In Microseconds)	Fixed Point Register-to-Register	Memory Access	Floating Point Double-Precision (Optional Hardware)
Add	0.75	1.5	2.25
Substract	0.75	1.5	2.25
Multiply	6.0	6.0	5.25
Divide	11.25	11.25	12.00
Square Root	5.25	—	9.75

Word Length: 24 bits + Parity.
Cycle Time: 750 nanoseconds (core), 150 nanoseconds (SCM).
Memory Addressing: Direct to 768K bytes via paging system.
Memory Size: 96K bytes basic, expandable in 24K increments to 768K bytes.
Input/Output: Maximum of 24 channels (only 12 of which may be CBC's or XBC's), 16 units per channel.

Programmed Data Transfer	External Control Lines. External Sense Lines. Single word to/from A register, 8 or 24 bits.
Automatic Transfer Data	Maximum of 12 CBC's or XBC's for automatic memory access. Rates up to 444K words per second on Single CBC, 1.3 Mwords per second, Multiple CBC's.
I/O Processor	Connects to the semiconductor memory option — can have up to 4 interfaces. Single-channel rates up to 4M bytes per second.
Priority Interrupt	Maximum of 8 executive traps and 48 vectored external interrupts available. All external interrupt levels may be individually enabled, disabled, armed, disarmed, or triggered.

Registers:

A Register	Main Arithmetic Register.
E Register	Main Arithmetic Register Extension.
I Register	24-bit General Purpose or Index Register.
J Register	24-bit General Purpose or Index Register.
K Register	24-bit General Purpose or Index Register.
Instruction Register	24-bit Register holds instructions while they are being executed.
Operand Register	24-bit Register used for holding operands in arithmetic execution and for entry from the control panel.
Program Address Register	16-bit Register for storage of the current instruction address.
Shift Control Register	8-bit Register used for arithmetic and shift operations.
Condition Register	4-bit Register used to indicate the status of arithmetic operations and data transfers.
Memory Address Register	18-bit Register used to hold memory address.
Memory Data Register	26-bit Register used to hold memory data and parity.
Time Register	24-bit Optional General Purpose Register usable as an interval timer.
Virtual Address Register (VAR)	512, 10-bit paging registers allowing an 8-bit memory address and a 2-bit page control.
Virtual Base Register (VBR)	A 12-bit Register of which 10 bits contain the lower page limits of the program.
Virtual Limit Register (VLR)	An 8-bit Register containing the upper page limit of the program.
Virtual Usage Register (VUR)	256, 1-bit Registers signifying access to a given memory page.
Virtual Not-Modified Register (VNR)	256, 1-bit storage registers signifying a write into a given memory page.
Virtual Usage Base Register (VUB)	An 8-bit Register used as a pointer to test the contents of the Virtual Usage Register and the Virtual Not-modified Register.
Virtual Source Register (VSR)	Contains the 10 bits of the Virtual Address Register and used as a base register for storing of data in the Virtual Address Register.
Virtual Destination Register (VDR)	Contains the 10 bits of the Virtual Address Register and used as a base register for retrieval of data from the Virtual Address Register.
Virtual Demand Page Register (VPR)	A 12-bit Register containing demand page and limit register violation information.

H Register	A 1-bit Register containing a memory bit to be tested or changed by the bit processor or the resultant tested or changed bit.
V Register	An 18-bit base address register used for operation with the bit processor.

Console:

Display	Program Address Register. Condition Register. Parity Error Bypass. Auto. Halt. H Register. Display Register (for memory and all working registers individually selected, including VBR and VLR).
Controls	4 Sense Switches. Run/Halt. Execute Instruction Register. Advance Program Counter. Manual/Auto. Register Entry and Clear Switches. 24-bit Entry Switches (includes 16-bit P-Stop). 24-bit Switch Register.
Operating Environment	10° to 45°C (50° to 113°F). (0°C to 50°C, optional) 20-90% relative humidity (non-condensing).
Power Requirements	117 VAC + 10% 48 — 62 Hz. 20 Amperes (Basic Configuration). Data Save in Memory System. Power Failure, Shutdown & Restart (optionally).

Specifications subject to change without written notice.

Datacraft®

a subsidiary of Harris-Intertype Corporation
1200 Gateway Drive
Fort Lauderdale, Florida 33309

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