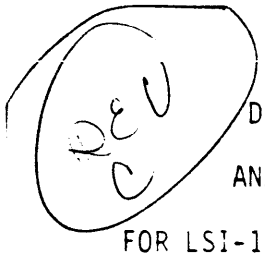
USER MANUAL FOR DATA TRANSLATION, INC.



DT2781

DEC DUAL HEIGHT

ANALOG I/O SYSTEM

FOR LSI-11, LSI-11/2, LSI-11/23

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CHAPTER 1

1.0 Product Description

DTI has designed a series of DEC dual height LSI Q-Bus compatible analog I/O boards. All models come standard with two independant D/A converters as well as a 16 single ended (8 differential) input A/D converter system. For clarity, the products have been broken up into two categories.

High Level Inputs

DT2781 - 12 bit resolution ADC with field selectable ranges of 0-10V (unipolar) or ±10V (bipolar). Has 16 single-ended or 8 differential input channels. SE/DI is field selectable.

DT2781/57xx - Same as above except with higher resolution on ADC. Configuration is not field selectable. Can be ordered as follows:

DT2781-xx/57xx-x-PGH

- PGH allows software control over gain of the instrumentation. Amp gains = 1,2,4,8. Alternative is gain selection by external resistor.
- B = Bipolar (range = ±10V)
  U = Unipolar (range = 0-10V)
- 14 = 14 bit resolution ADC
  16 = 16 bit resolution ADC
- SE = 16 single ended input channels
  DI = 8 differential input channels

Note: None of these options are field selectable.

Wide Range Inputs

DT2785 - 12 bit resolution ADC with field selectable unipolar or bipolar operation. Ranges are resistor selectable from 0-10mV unipolar (±10mV bipolar) to 0-10V unipolar (±10V bipolar). Has 16 single-ended or 8 dirrerential input channels. SE/DI is field selectable.

DT2785/57xx - Same as above except with higher resolution on ADC. Configuration is not field selectable. Can be ordered as follows:

DT2785-xx/57xx-x-PGL

PGL allows software control over gain of the instrumentation amp. gains = 1, 10, 100, 500. Alternative is gain selection by external resistor.

B = Bipolar (range = ±10V max)
U = Unipolar (range = 0-10V max)

14 = 14 bit resolution ADC
16 = 16 bit resolution ADC

SE = 16 single-ended input channels
DI = 8 differential input channels

Note: None of these options are field selectable.

CHAPTER 2

2.0 DT2781 High Level Input System Specifications

2.1 Analog Inputs

The DT2781 utilizes the DT57L02 data acquisition module. This module will accept up to 16 single-ended or 8 differential input channels. SE/DI selection is accomplished by wire wrap jumpers. This board has no expansion capability.

2.2 Number of Analog Inputs

The DT2781 will accept up to 16 single-ended or 8 differential input channels.

2.2.1 Selection of SE/DI

The configuration is field selectable simply by altering wire wrap jumpers.

2.3 Input Range

0-10V F.S. straight binary (unipolar)
±10V F.S. 2's complement offset (bipolar)

2.3.1 Input Protection

Inputs are current limited and protected to an ± 30V overvoltage condition without damage.

2.3.2 Input Impedance

100 Megohm, 10pf - "off" channels
100 Megohm, 100pf - "on" channels

2.3.4 Input Bias Current

15nA @ 25°C

2.3.5 Maximum Input Signal

10.5 Volts (signal + common mode voltage)

2.3.6 Common Mode Rejection Ratio

80 dB at full scale

2.4 A/D Specifications

2.4.1 Resolution

12 bits - unipolar
11 bits + sign bit - bipolar

2.4.2 Linearity

±½LSB

2.4.3 Inherrent Quantisizing Error

±½LSB

2.4.4 Stability

±25ppm/°C FSR

2.4.5 Sample and Hold Aperture Uncertainty

<10nSEC.

2.5 System Specifications

2.5.1 System Accuracy

±.03% (Bipolar)

2.5.2 Throughput Rate

25KHz

2.5.3 Input Noise

2mV RMS

CHAPTER 3

3.0 DT2781/57xx High Resolution, High Level Input System Specifications

3.1 Analog Inputs

The DT2781/57xx uses the DT5714/DT5716 modules for higher ADC resolution. This option will also accept 16 single-ended or 8 differential input channels. The SE/DI configuration is not jumper selectable and there is no expansion capability.

3.2 Input Specifications

3.2.1 Input Range

0-10V F.S. straight binary (unipolar)
±10V F.S. 2's complement offset (bipolar)

The input range can be changed under software control by the PGH option or hardware control via an external resistor. See table 1 and product description. The gains possible are 1,2,4,8.

3.2.2 Input Protection

Inputs are current limited and protected to ± 16V.

3.2.3 Input Impedance

100 Megohm, 10pf "off" channel
100 Megohm, 100pf "on" channel

3.2.4 Input Bias Current

15nA @ 25°C

3.2.5 Maximum Input Signal

10.5V (signal + common mode voltage)

3.2.6 Common Mode Rejection Ratio

80 dB at F.S.

3.3 5714 A/D Specifications

3.3.1 Resolution

14 bits

3.3.2 Linearity

±½LSB

3.3.3 Inherent Quantisizing Error

±½LSB

3.3.4 Offset Error

Adjustable to zero

3.3.5 Gain Error

Adjustable to zero

3.3.6 Stability

± 10ppm/°C FSR

3.3.7 Accuracy

±.01%

3.3.8 Throughput

10KHz

3.3.9 Input Noise

1uV RMS

3.4 5716 A/D Specifications

3.4.1 Resolution

16 bits

3.4.2 Linearity

± 1 LSB

3.4.3 Inherent Quantisizing Error

± 1 LSB

3.4.4 Stability

±10ppm/°C FSR

3.4.5 Accuracy

±.0075% at gain = 1. If PGH option is used, see table 1.

3.4.6 Throughput

2.4KHz at gain = 1. If PGH option is used, see table 1.

3.3.7 Input Noise

1uV RMS

CHART OF INPUT RANGE PARAMETERS

INPUT RANGE				Cext (in uF)			AMPLIFIER SETTLING TIME (in Millisec)			SYSTEM ACCURACY			THROUGHPUT RATE (in Hz)		
Unipolar	Bipolar	GAIN	Rext (in Ohms)	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712
0 to +5mV	±5mV	2000	50.02	0.470	0.100	0.056	24.0	6.0	3.0	±.13%	±.14%	±.18%	40	166	333
0 to +10mV	±10mV	1000	100.10*	0.220	0.056	0.022	12.0	3.0	1.5	±.06%	±.08%	±.10%	80	333	666
0 to +25mV	±25mV	400	250.62*	0.082	0.022	0.010	4.8	1.2	.6	±.035%	±.040%	±.08%	200	833	1600
0 to +50mV	±50mV	200	502.51*	0.039	0.010	0.0047	2.4	.6	.3	±.020%	±.022%	±.07%	400	1600	3200
0 to 100mV	±100mV	100	1,010.1*	.022	0.0047	0.0022	1.2	.3	.15	±.010%	±.020%	±.05%	800	3300	6600
0 to +1V	±1V	10	11,111*	None	None	None	.3	.07	.025	±.010%	±.015%	±.03%	2500	10,000	20,000
0 to +2.5V	±2.5V	4	33,333*	None	None	None	.3	.07	.025	±.010%	±.012%	±.03%	2500	10,000	20,000
0 to +5V	±5V	2	100,000*	None	None	None	.3	.07	.025	±.009%	±.01%	±.03%	2500	10,000	20,000
0 to +10V	±10V	1	NONE	None	None	None	.3	.07	.025	±.0075%	±.01%	±.03%	2500	10,000	20,000

* These resistors are offered as aPrecision Resistor Gain Selection Kit, Model number DT13-10501-4, for high accuracy gain setting.

REXT = 100,000 / (G-1)

$$\text{Throughput Time} = \frac{1}{\text{Amplifier Settling Time} + \text{A/D Conversion Time}}$$

TABLE 1

CHAPTER 4

4.0 2785 Wide Range Input Specifications

4.1 Analog Inputs

The DT2785 utilizes the 57L02 wide range data acquisition module. This module will accept up to 16 single-ended or 8 differential input channels. SE/DI selection is accomplished by wire wrap jumpers. There is no expansion capability.

4.2 Number of Analog Inputs

The DT2785 will accept upto 16 single-ended or 8 differential input channels.

4.2.1 Selection of SE/DI

The configuration is field selectable simply by altering wire wrap jumpers.

4.3 Input Range

The input range is variable by changing Rg and Ct (see Figure 8 for location). Full scale extends from 10mV to 10V in either the unipolar or bipolar mode. See table 2 for details.

4.3.1 Input Protection

Inputs are current limited and protected to ± 30V overvoltage without damage.

4.3.2 Input Impedance

100 Megohm, 10pF - "OFF" channel
100 Megohm, 100pF - "ON" channel

4.3.3 Input Bias Current

15nA @ 25°C

4.3.4 Maximum Input Signal

±10.5V (signal + common mode_

4.3.5 Common Mode Rejection Ratio

80dB at full scale

4.4 A/D Specifications

4.4.1 Resolution

12 bits - unipolar
11 bits + sign bit - bipolar

4.4.2 Linearity

±½LSB

4.4.3 Inherent Quantisizing Error

±½LSB

4.4.4 Stability

±25ppm/°C FSR

4.4.5 Sample and Hold Aperture Uncertainty

10nSEC

4.5 System Specification

4.5.1 System Accuracy and Throughput

System accuracy and throughput depend upon the range setting of the A/D system. Table 2 shows how these quantaties inter-relate.

4.5.2 Input Noise

2uV RMS

TABLE 2.

57L02 12 bit ADC

GAIN	ACCURACY (BIPOLAR)	THROUGHPUT (KHz)
1	±0.03%	25
2	±0.03%	25
4	±0.03%	25
10	±0.03%	25
100	±0.05%	16.75
200	±0.07%	11.1
400	±0.08%	7.1
1000	±0.1%	3.7

CHAPTER 5

5.0 DT2785/57xx High Resolution, High Level Input System Specifications

5.1 Analog Inputs

The DT2785/57xx uses the 57xx wide range modules for higher resolution as well as variable gain setting. This option will also accept 16 single-ended or 8 differential input channels. Configuration is not jumper selectable. There is no expansion capability.

5.2.1 Input Range

Input range is variable by either changing Ct/Rg or by using the PGL option. PGL gives gains of 1,10,100, and 500. See table 1 for details.

5.2.2 Input Protection

Inputs are current limited and protected to ±16V overvoltage without damage.

5.2.3 Input Impedance

100 Megohm, 10pF "off channel"
100 Megohm, 100pF "On channel"

5.2.4 Input Bias Current

15mA @ 25°C

5.2.5 Maximum Input Signal

±10.5Vs (signal + commode mode voltage)

5.2.6 Commode Mode Rejection

80 dB

5.3 5714 A/D Specifications

5.3.1 Resolution

14 bits

5.3.2 Linearity

±1 LSB

5.3.3 Inherent Quantisizing Error

±1 LSB

5.3.4 Offset Error

Adjustable to zero

5.3.5 Gain Error

Adjustable to zero

5.3.6 Stability

±10ppm/°C FSR

5.3.7 System Accuracy and Throughput

System accuracy and throughput depend upon the range setting of the A/D system. Table 2 shows how these quatities inter-relate.

5.3.8 Input Noise

1uV RMS

5.4 5716 A/D Specifications

5.4.1 Resolution

16 bits

5.4.2 Linearity

±1LSB

5.4.3 Inherent Quantisizing Error

±1LSB

5.4.4 Stability

±10ppm/°C FSR

5.4.5 Accuracy and Throughput

System accuracy and throughput depend upon the range setting of the A/D system. Table 2 shows how these quantities inter-relate.

5.4.6 Input Noise

1uV RMS

CHAPTER 6

6.0	External Trigger Specifications for All Models (EXT Trig L, Pin 19-J1)	
6.0.1	Signal Compatibility	TTL
6.0.2	Origin	User device (i.e. DT2769 Real Time Clock, or Signal Generator.)
6.03	Usage	To initiate A/D Conversion (Note: trigger occurs on high to low edge only.)
6.0.4	Loading	1 TTL Load.
6.1	D/A Specifications (both Channels) on all Models	
6.1.1	Resolution	12 bits
6.1.2	Non-Linearity	.02%
6.1.3	Differential Linearity	+/- ½ LSB
6.1.4	Gain Error	adjustable to zero
6.1.5	Zero Error	adjustable to zero
6.1.6	Offset drift unipolar	+/- 3ppm/ C
6.1.7	Offset drift bipolar	+/- 30ppm/ C
6.1.8	Gain drift	+/- 30ppm/ C
6.1.9	Settling Time	
6.1.10	to 0.01% FSR	35uS (10 Volt step)
6.1.11	Settling Time	
6.1.12	to 0.01% FSR	10uS (0.1 volt step)
6.1.13	Slew Rate	0.33 V/USEC
6.1.14	Range	0-10V, ±10V, ±5V (jumper selectable)
6.1.15	Current Output Impedance (DC)	±5mA Max. 0.1 ohms.
6.1.16	Noise	0.1% FSR
6.1.17	Capacitive Load Capability	0.5 MFD
6.1.18	Protection	Short Circuit Protected to Common

6.2 Physical Specifications

All models are contained on a standard DEC dual height card with LSI-11 compatability.

6.3 Power Requirements

All models - +5V @ 1.5A 5%

6.4 Q-Bus Loading

Each card represents 1 Q-Bus load.

CHAPTER 7

7.0 Programming Specifications For All Models

Data Translation interfaces are designed to meet the requirements of standard DEC interfaces. As such they are structured around a Control and Status register for complete software control of the interface.

7.1 DT2781/DT2785

7.1.1 Modes of Operation

This series can operate in a number of operating modes, as follows:

Program I/O - In this mode standard LSI-11 instructions can access and control the A/D components on the interface. A start A/D conversion can be accomplished by two ways:

1. Set A/D Start Bit (Bit Ø) ADCSR

2. External Triggers or Real Time Clock input.

Interrupt - In many real time applications the program does not want to dedicate itself to taking analog measurements. In this case the interface can be enabled to produce a program interrupt on the condition A/D Done. An interrupt may also be produced on the Error bit (Bit 15 ADCSR).

7.1.2 Device Address

The DT2781/DT2785 device address is selectable via wire wrap jumpers. Device address may be assigned between 170000_8 and 277774_8. The order of address is as follows, once a base address has been set in the jumpers:

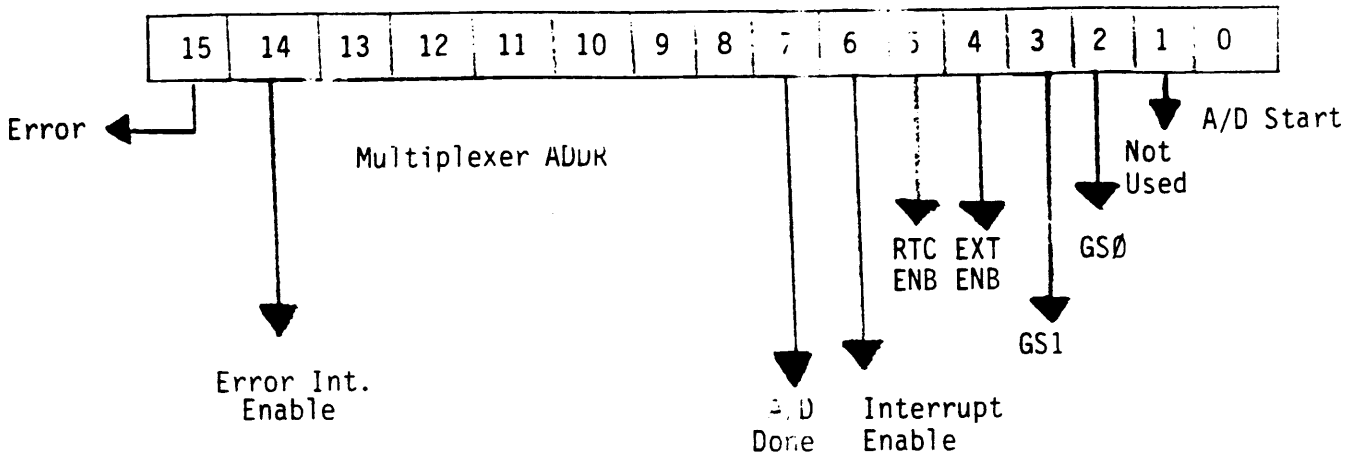
A/D Control and Status Register (ADCSR) - Base (R/W)
A/D Data Buffer Register (ADDBR) - Base + 2 (Read Only)
DAC A Register - Base + 4 (Write Only)
DAC B Register - Base + 6 (Write Only)

7.1.3 Interrupt Vector Address

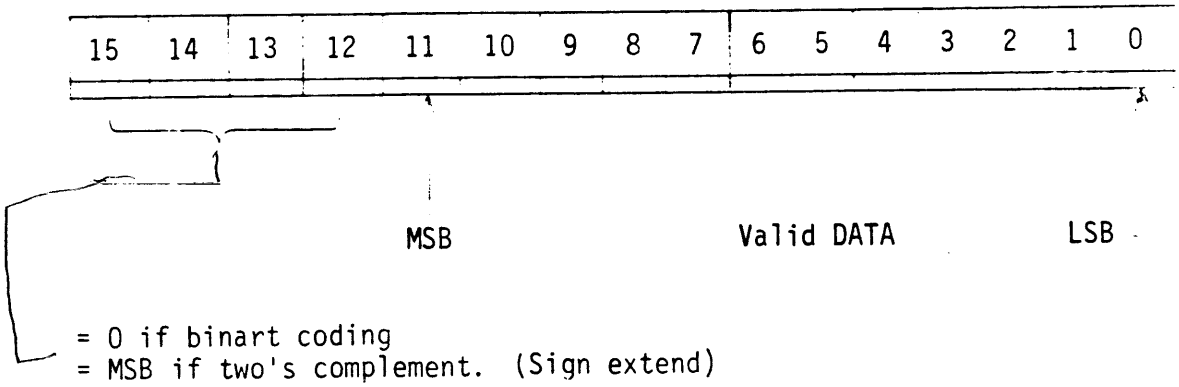
The vector address is set via wire wrap jumpers, they are selectable in increments of 10_8. There are two Interrupts A/D DONE, and ERROR. (See 7.1.4 CSR descriptions).

A/D DONE = BASE VECTOR
ERROR = BASE VECTOR + 4

7.1.4 Control and Status Register



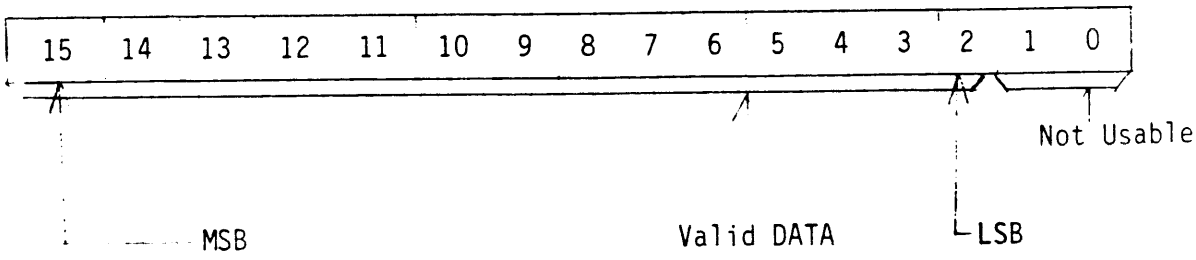
7.1.5 DT2781/2785 A/D Data Buffer Register (ADDBR) (Read Only)



The user has the option of using bits 12-15 in either sign extend mode or hard wiring to logic Ø or 1.

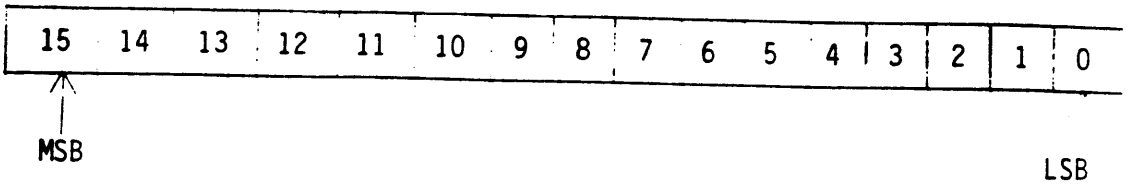
7.1.6 DT2781/5714 A/D Buffer Register (Read Only)

For 14 bit resolution, the two least significant digits are ignored.



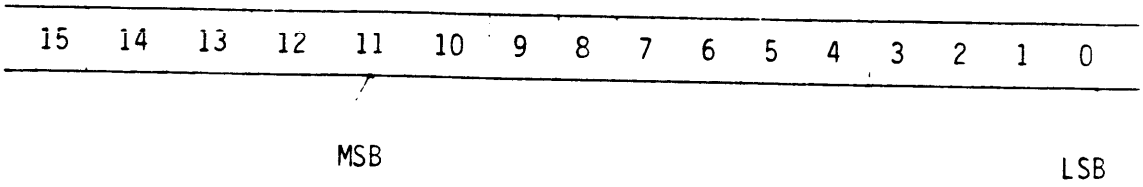
7.1.7 DT2781/5716 A/D Buffer Register (Read Only)

The format for 16 bit resolution is as follows:



7.1.8 D/A Data Registers (Write only)

The 12 bit D/A Registers are loaded in the following format:



The conversion is started immediately upon loading.

CSR BIT DESCRIPTIONS: Note:

BIT #	NAME	DESCRIPTION
15	ERROR	READ/WRITE - Indicates an error set by one of the following conditions. 1. Attempting an external start or clock start during MUX settling. 2. Attempting a start while conversion in process. 3. Attempting any start while the A/D Done bit is set. Cleared by Processor and Init.
14	ERROR INT. ENABLE	READ/WRITE - When set enables an Interrupt on Error Bit. Cleared by INIT.
13-8	MULTIPLEXER ADDRESS	READ/WRITE - Six MUX channel address bits (only 4 Bits are used.
7	A/D DONE	READ ONLY - Set by end of conversion reset by read A/D data. Cleared by INIT.
6	DONE INT. ENABLE	READ/WRITE - When set will enable interrupts from A/D done. Cleared by INIT.
5	RTC ENB	READ/WRITE - Real time clock enable when set this bit allows start conversion from the real time clock.
4	EXT TRIG ENB	READ/WRITE - When set this bit allows start conversion from an external trigger source.
3-2	GAIN SELECT (USED ON 14 & 16 BIT MODELS ONLY)	READ/WRITE - These bits provide the gain select information for PGX option on high resolution models.
Ø	A/D START	WRITE ONLY - Initiates a conversion when set, cleared by internal logic after start conversion, will always read back as a Ø.

BIT 3 (GS1)	2 (GSØ)	PGH	PGL
0	0	1	1
0	1	2	10
1	0	4	100
1	1	8	500

CHAPTER 8

8.0 User Configuration

8.1 Base Address Selection For All Models

The Base Address which is the I/O address assigned to the Control-Status Register (CSR) is user selectable by means of wire wrap jumpers located near the bus interface logic as shown in Figure 8. The A/D Data Buffer Register address is then two locations greater than the CSR (Base) address. The DIP switches allow the user to set the base address anywhere in the 170000_8 - 177774_8 address space in increments of 10_8. The recommended base address for the DT2781 series is 170400_8 and is the address set at the factory. Figure 8.1 shows how the wire wrap jumpers must be set to generate this base address.

1		7			0		4			0					0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0

Jumper Installed Decodes Address Bit "1" →

0	0	0	0	0	0	0	0	0	0
0 A12	0 A11	0 A10	0 A9	0 A8	0 A7	0 A6	0 A5	0 A4	0 A3

Figure 8.1

Jumper Configurations for Base Address of 170400_8

As shown in Figure 8.1, a wire wrap jumper in place represents a "1" in the corresponding bit location and no wire wrap jumper represents a "0" in the corresponding bit location.

8.2 Vector Address Selection for All Models

The DT2781 series systems are capable of generating two distinct interrupt vectors to the LSI-11 processor. These interrupts can occur when:

1. A/D Done is set
2. Error is set

Each of these two events can generate a unique interrupt to the processor with the internal priority being arranged such that the A/D Done interrupt has the higher priority of the two if both occur simultaneously and are both enabled. The interrupt vector address of the A/D Done interrupt can be assigned any address in the 000_8 - 770_8 vector address space in 10_8 increments. The interrupt vector of the Error Interrupt is then always 4_8 locations higher than the A/D Done interrupt vector address. The recommended interrupt vector address for the DT2781

series is 400_8 and is set to that value at the factory. Figure 8.2 shows how the wire wrap jumpers must be set to generate this address.

	0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Jumper Installed	0	0	0	0	0	0
Decodes Vector address	0	0	0	0	0	0
Bit "1"	V8	V7	V6	V5	V4	V3

Figure 8.2

Jumper Configuration for Vector Address of 400

8.3 Analog Configuration for DT2781/DT2785

The input range, polarity, and data coding for 12-bit models are user selectable. High resolution models (14,16-bits) are not user configurable and must be ordered from the factory as required.

All user configuration is accomplished by the insertion or removal of a wire wrap jumper between a pair of posts. Most factory default jumpers are implemented by connecting the wire wrap post via an etch run. To remove such a factory default jumper, the user must cut the etch run between the posts using a sharp knife or blade.

The location of most of the posts have been lettered right on the P.C. board, however, for ease of location, figure 8.3 at the end of this chapter also shows the location of all the jumpers.

Please note that there are two types of jumpers on the board. Some of the jumpers are point-to-point in which case each wire wrap post has a unique number and jumpering is done from a certain wire wrap post to another numbered wire wrap post. The other jumpers are a labelled pair of wire wrap posts. With this type of designation a jumper is installed across a pair of wire wrap posts as identified in the configuration chart.

8.3.1 Ranges

The DT2781/85 have the following ranges:

DT2781 (High Level)	0-10V Unipolar ±10V Bipolar
DT2785 (Wide Range)	From 0-10mV F.S. to 0-10V F.S. From ±10mV F.S. to ±10V F.S. Resistor selectable, Unipolar or Bipolar

8.3.2 DT2781/DT2785 Analog Input Configuration

Models DT2781/DT2785 can be user configured for SE or DI operation in the field. To change the DT2781/2785 from 16 SE to 8 DI or from 8 DI to 16 SE the following jumpers are required.

INPUT TYPE	JUMPERS
SE (16 Channels)	P1 to P2
DI (8 Channels)	P2 to P3 and P4 to P5

Note: Factory default is DI.

8.3.3 DT2781/DT2785 Range and Code Selection

The DT2781/DT2785 can be configured for any full scale range in the 10mV-10V range or ±10mV - ±10V by means of a single gain resistor. The gain resistor is used to program the gain of the instrumentation amplifier from 1 to 1000. Then as the A/D has a fullscale range of 10V or ±10V, the gain of the instrumentation amplifier will determine the full scale input signal required to produce a 10V or ±10V output. At a gain of 1000, the input signal voltage will be 10mV full scale. For a gain of 1, no resistor is required as the instrumentation amplifier is defaulted to this value internally. The gain of the instrumentation amplifier in terms of the gain selection resistor Rg is:

$$G = 1 + \frac{2 \times 10^4}{Rg}$$

or

$$Rg = \frac{2 \times 10^4}{G-1}$$

As the gain of the instrumentation amplifier is increased, the time allowed for the amplifier to settle must also be increased. This is accomplished by the addition of a single timing capacitor Ct. The location of the Rg resistor and Ct capacitor is printed on the interface board. The table below shows the resistors and capacitors required for some standard ranges.

CHART OF INPUT RANGE PARAMETERS

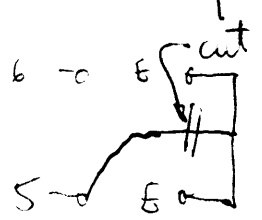
Input Range	Gain	RG (ohms)	Ct	System Accuracy	Amplifier Settling	Throughput
10mV, ±10mv	1000	20.02	0.015uf	±0.1%	250uS	3.7KHz
15mV, ±25mV	400	50.13	6800pf	±0.08%	120uS	7.1KHz
50mV, ±50mV	200	100.5	3300pf	±.07%	70uS	11.1KHz
100mV, ±100mV	100	202.0	150pf	±.05%	40uS	16.75KHz
1.0V, ±1.0V	10	2222	None	±.03%	12uS	31KHz
2.5V, ±2.5V	4	6667	None	±.03%	12uS	31KHz
5.0V, ±5.0V	2	20.0K	None	±0.03%	12uS	31KHz
10.0V, ±10.0V	1	None	None	±0.03%	12uS	31KHz

Note: $\text{Throughput} = \frac{1}{\text{Amp Settling} + 20\text{uS}}$

8.3.4 DT2781/DT2785 Input Polarity Selection

By using an appropriate Rg and Ct the user can configure the range of operations as required, the polarity of the input and data coding is then selected via jumpers as outlined below:
Note: These jumpers are configured as pairs thus installing jumper ID means put a wire across the pair of posts labelled ID.

POLARITY	JUMPERS		
	TWO's COMPLEMENT DATA	OFFSET BINARY DATA	BINARY DATA
Unipolar	Not applicable	Not applicable	1D, 6D, 6E
Bipolar	4D, 5D, 5E	4D, 6D, 6E	Not applicable



8.4 Analog Configuration for DT2781/57xx and DT2785/57xx

8.4.1 Ranges

Both models have the capability of user selectable gain of the input amplifier. This can be done using the PGX option or by adding an external resistor. See table 8.4 and sections 8.4.2, 8.4.3.

2781/xx	from 1.25 F.S. to 10V F.S.
2785/57xx	from 5mV F.S. to 10V F.S.
	either unipolar or bipolar.

8.4.2. PGS Option

The PGX option can be ordered with high resolution A/D modules. It allows software control over the F.S. input range. Note that a timing cap of .022uF (14 bit) or .062uF (16 bit) must be installed for proper PGH operation. Also, install jumpers P6 and P7.

PGH (2781/57xx)

GAIN	RANGE
1	0-10V, ±10V
2	0-5V, ±5V
4	0-2.5V, ±2.5V
8	0-1.25V, ±1.25V

PGL (2785/57xx only)

GAIN	RANGE
1	1-10V, ±10V
10	0-1V, ±1V
100	0-100mV, ±100mV
1600	0-20mV, ±20mV

8.4.3 Gain Selection with PGX

If no PGX option is present, then gain can be selected by an external resistor (Rg) and external capacitor (Ct). The gain equation for the instrumentation amp. is

$$G = \frac{1 + 100{,}000}{Rg} \quad \text{or} \quad Rg = \frac{100{,}000}{G-1}$$

See chart of Input Parameters (table 8.4)

2781/57xx max gain = 10

2785/57xx max gain = 2000

8.4.4 Selection of SE/DI and U/B

None of the higher resolution models are field selectable in these parameters. They must be factory ordered. (See product description.)

8.4.5 Data Notation for 14 Bit Resolution

Parallel digital outputs are provided in binary code. A unipolar input (0 to F.S.) should be jumpered to produce a straight binary output. A bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding. The two least significant bits are ignored.

CODE	RANGE	16 BIT BINARY CODE
Binary	+F.S.	177774 - 177777
	0	000000 - 000003
Offset	+F.S.	
	0	
	-F.S.	000000 - 000003
2's	+F.S.	077774 - 077777
Complement	0	000000 - 000003
	F.S.	100000 - 100003

8.4.6 Data Notation for 16 Bits

Parallel digital outputs are provided in binary code. A unipolar input (0 to F.S.) should be jumpered to produce a straight binary output. A Bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding.

CODE	RANGE	16 BIT BINARY CODE
Binary	+F.S.	177777
	0	000000
Offset	+F.S.	177777
Binary	0	100000
	-F.S.	000000
2's	+F.S.	077777
Complement	0	000000
	-F.S.	100000

CHART OF INPUT RANGE PARAMETERS

INPUT RANGE				Cext (in uF)			AMPLIFIER SETTLING TIME (in Millisec)			SYSTEM ACCURACY			THROUGHPUT RATE (in Hz)		
Unipolar	Bipolar	GAIN	Rext (in Ohms)	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712
0 to +5mV	±5mV	2000	50.02	0.470	0.100	0.056	24.0	6.0	3.0	±.13%	±.14%	±.18%	40	166	233
0 to +10mV	±10mV	1000	100.10*	0.220	0.056	0.022	12.0	3.0	1.5	±.06%	±.08%	±.10%	80	333	666
0 to +25mV	±25mV	400	250.62*	0.082	0.022	0.010	4.8	1.2	.6	±.035%	±.040%	±.08%	200	833	1600
0 to +50mV	±50mV	200	502.51*	0.039	0.010	0.0047	2.4	.6	.3	±.020%	±.022%	±.07%	400	1600	3200
0 to +100mV	±100mV	100	1,010.1*	.022	0.0047	0.0022	1.2	.3	.15	±.010%	±.020%	±.05%	800	3300	6600
0 to +1V	±1V	10	11,111*	None	None	None	.3	.07	.025	±.010%	±.015%	±.03%	2500	10,000	20,000
0 to +2.5V	±2.5V	4	33,333*	None	None	None	.3	.07	.025	±.010%	±.012%	±.03%	2500	10,000	20,000
0 to +5V	±5V	2	100,000*	None	None	None	.3	.07	.025	±.009%	±.01%	±.03%	2500	10,000	20,000
0 to +10V	±10V	1	NONE	None	None	None	.3	.07	.025	±.0075%	±.01%	±.03%	2500	10,000	20,000

* These resistors are offered as aPrecision Resistor Gain Selection Kit, Model number DT13-10501-4, for high accuracy gain settin

$$REXT = \frac{100{,}000}{(G-1)}$$

$$\text{Throughput Time} = \frac{1}{\text{Amplifier Settling Time} + \text{A/D Conversion Time}}$$

8.5 External Trigger Configuration

The DT2781 series allows the user to synchronize A/D conversions from two external sources. Each of the two sources may be enabled or disabled individually by software by setting or clearing certain bits of the control and status register. The source designated as RTCINL is applied to the board via user connector J1 pin 21. The source designated as EXT TRIG. may be selected by the user to the signal applied at user connector J1 pin 19 or the BUS EVENT line (BEVENT L) which is a 50/60 cycle signal appearing on the computer bus. To select the source for the EXT TRIG signal jumper pairs F1 and F2 are used as outlined below.

EXT TRIG source comes from J1 pin 19 - Install F1

EXT TRIG source comes from BUS EVENT line - Install F2.

8.6 D/A Configuration (All Models)

The output range, data, polarity and the format of the digital data presented to the DACs are user selectable as outlined in the tables below. Note that both DAC A and DAC B must operate with the same data coding and output polarity configuration. However, they need not both operate at the same range (i.e. DAC A may be strapped for ±10V full scale while DAC B may be strapped for ±5V full scale, and both must operate with the same data format, either two's complement or offset binary).

Range & Polarity	Binary Data Format	Offset Binary Data Format	Two's Complement Data Format
±10V	Not applicable (N.A.)	3A to 5A D2 to D3	3A to 5A D1 to D3
±5V	N.A.	1A to 2A, 3A to 5A, D2 to D3	1A to 2A, 3A to 5A, D1 to D3
0-10V	1A to 2A D2 to D3	N.A	N.A
0-5V	1A to 2A, 3A to 4A, D2 to D3	N.A	N.A

JUMPER TABLE DAC A

Range & Polarity	Binary Data Format	Offset Binary Data Format	Two's Complement Data Format
±10V	N.A.	1B to 5B D2 to D3	1B to 5B D1 to D3
±5V	N.A.	2B to 3B, 1B to 5B, D2 to D3	2B to 3B, 1B to 5B D1 to D3
0-10V	2B to 3B D2 to D3	N.A.	N.A.
0-5V	2B to 3B, 1B to 4B, D2 to D3	N.A.	N.A.

JUMPER TABLE DAC B

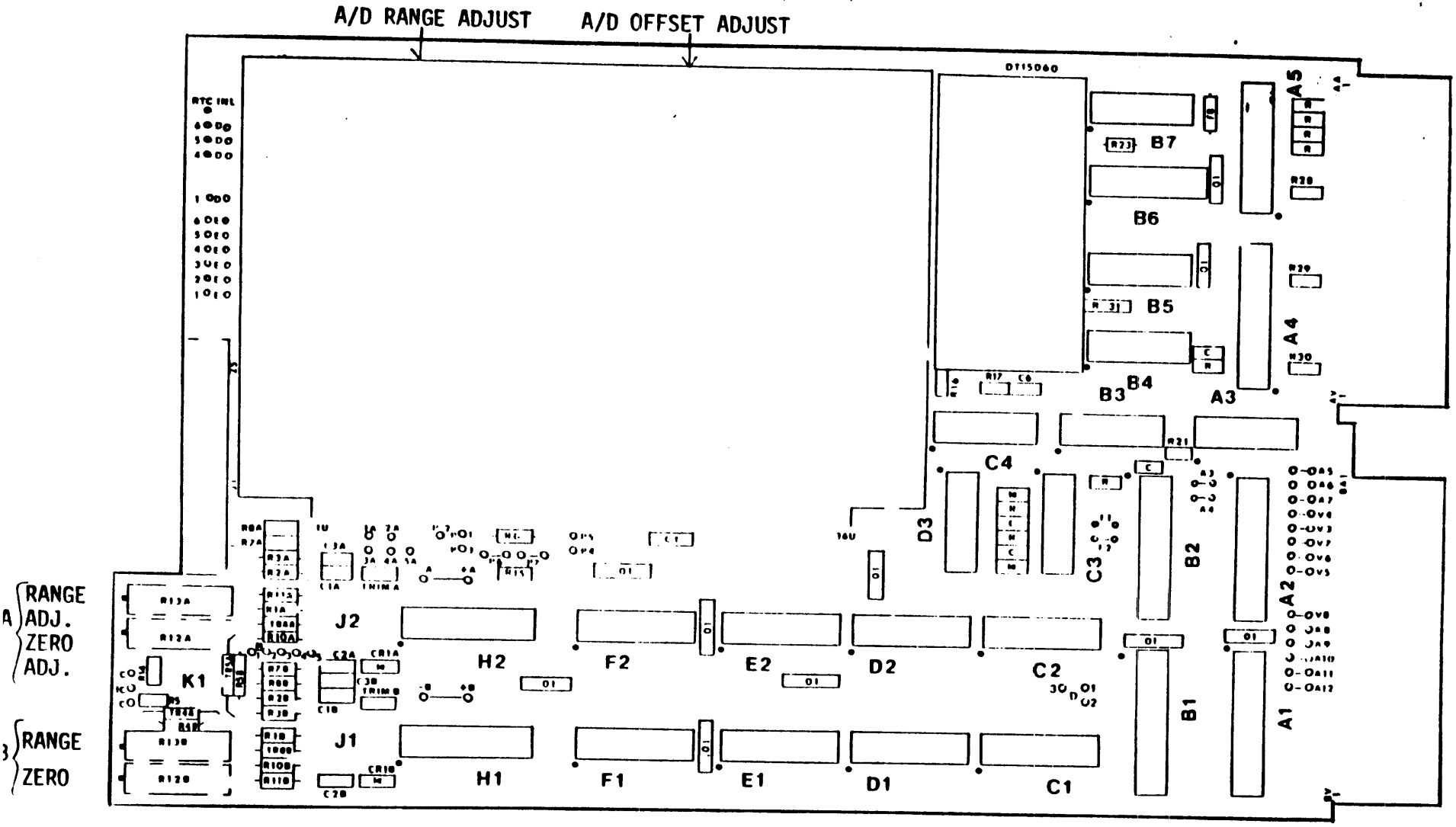


Figure 8.3

COMPONENT DESIGNATIONS

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
A	EP074	11070074	C
SCALE			SHEET 1 OF 1

CHAPTER 9

9.0

Table 9.1 shows the various models and the connection schemes available.

MODEL	SE/DI JUMPER SELECTABLE	NUMBER OF INPUTS
DT2781	Yes	16SE/8DI
DT2781/57xx	No	16SE/8DI
DT2785	Yes	16SE/8DI
DT2785/57xx	No	16SE/8DI

Please note that there is no expansion capabilities on any of these models.

9.1 Single-Ended Inputs - 16 Channels

Single-ended analog inputs - Single-ended connections are those which have a common side that is referenced back to analog common of the system. The advantage of this scheme is that the user gets twice the number of channels in the same space. The major disadvantage is that the user gives up any common mode rejection he might obtain from a differential system.

Recommendations:

High level inputs, greater than 1V.
Short lead lengths, less than 15 ft.

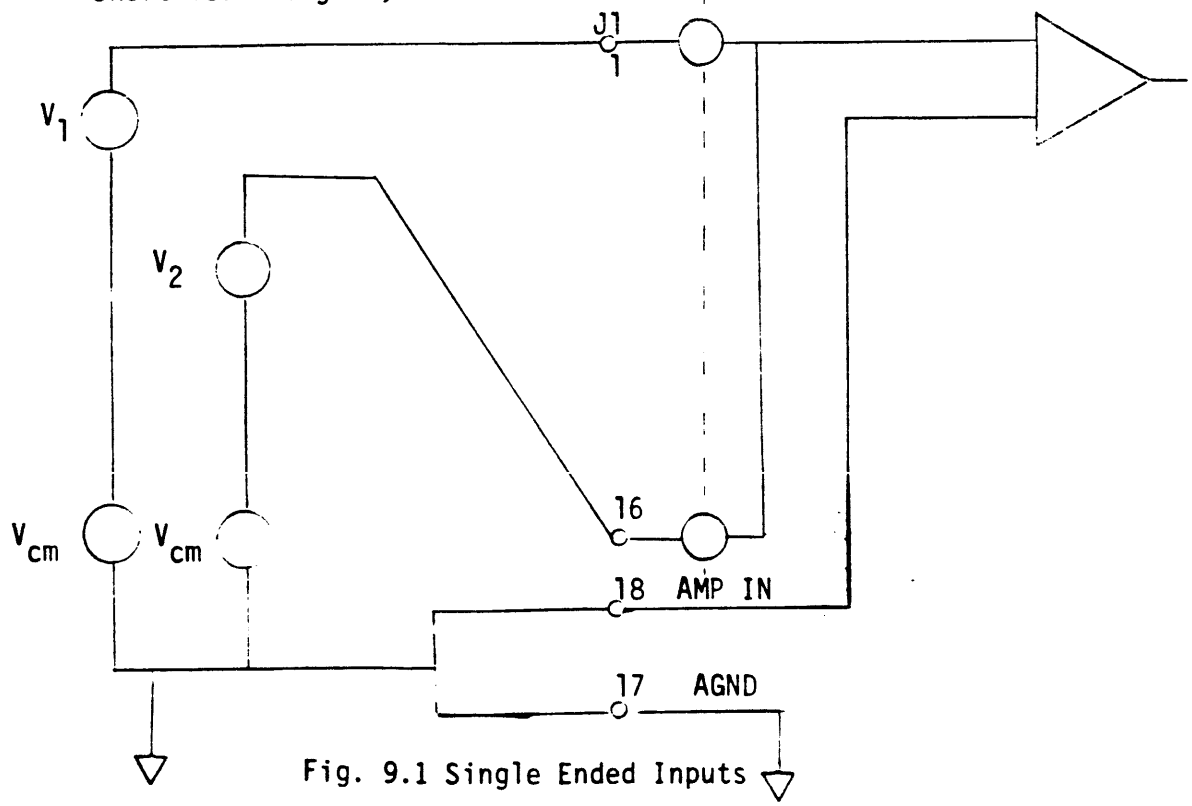


Fig. 9.1 Single Ended Inputs

Fig. 9.1 Single Ended Inputs (continued)

Where VCM = Common Mode Voltage

9.2 Pseudo - Differential Inputs - 16 Channels

Pseude - Differential mode can be utilized with a single ended system if the user has all input sensors referneced to a common ground point. In this manner the input instrumentation amplifier can reject common mode noise. This is possible since the AMP LO input is brought out to connector J1 for user connection. The following diagram illustrates -

Recommendation:

Input Ranges: 100mV to 10V
Lead Lengths - less than 25 ft.

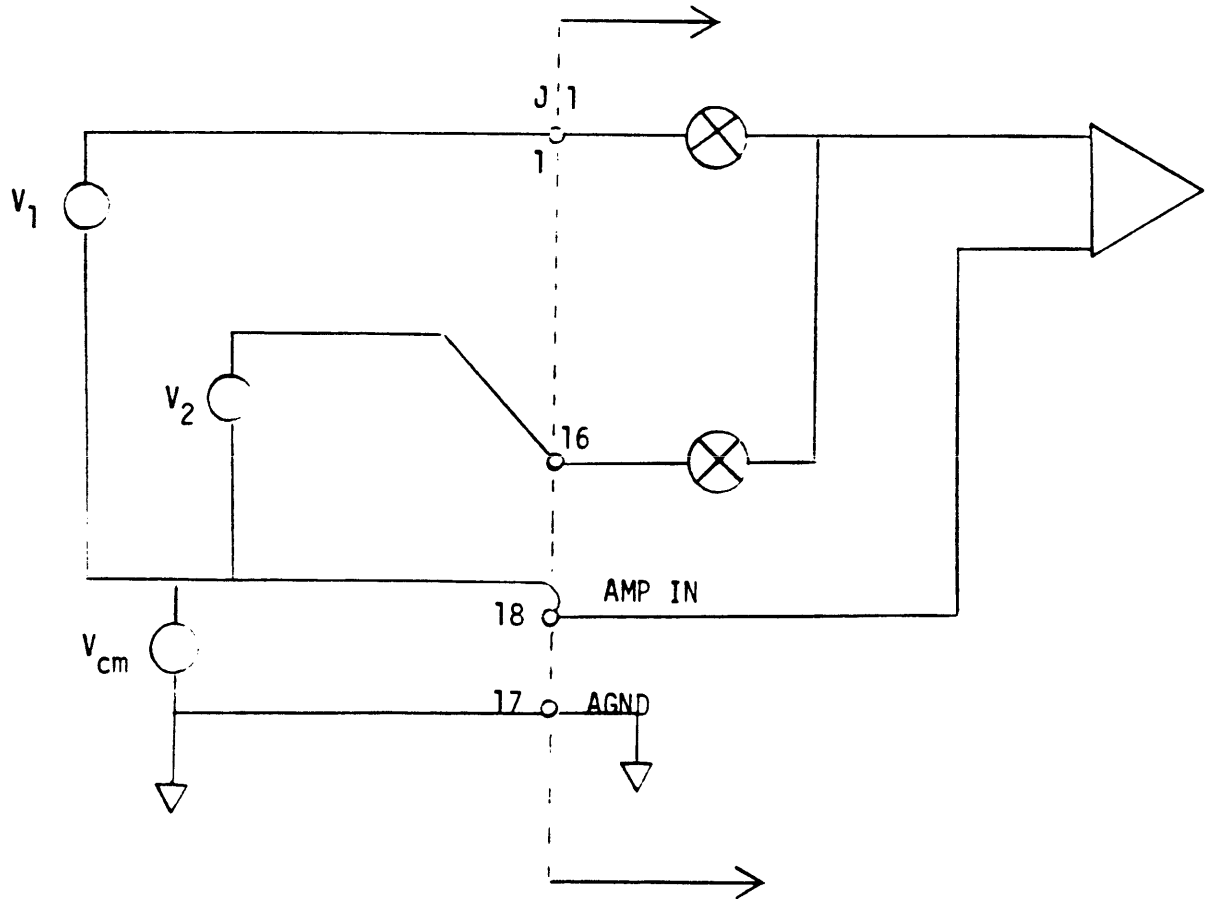


Fig. 9.2 PSEUDO-DIFFERENTIAL

9.3 Differential Inputs - 8 Channels

Differential Inputs - when the differential input scheme is utilized, there are two switches per channel, thus the number of channels are cut in half. The benefits are that common mode voltages, i.e. voltages appearing on both sides of the source simultaneously can be rejected by the differential input instrumentation amplifier. This CMR accounts for a much quieter system. The amount of CMRR depends on how well balanced the instrumentation amplifier is.

Recommendations:

Input Ranges:	10mV to 10V
Lead Lengths:	As required by user
Lead Type:	Twisted Pair (Low Level) Shielded Input line.

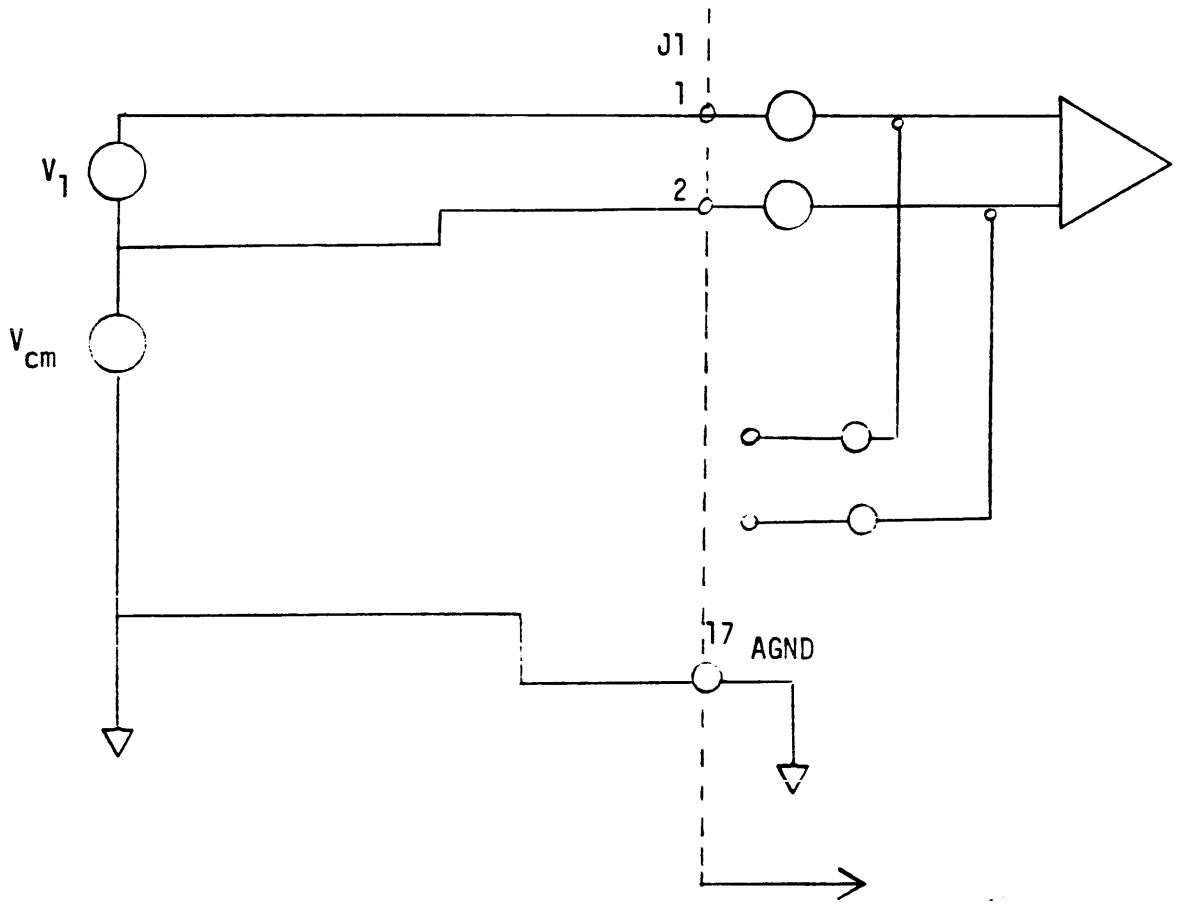


Fig. 9.3 DIFFERENTIAL INPUT CONNECTION

9.5 Avoiding Spurious Signals

In order to obtain the best performance from a system, certain guidelines in connecting analog signals to the system should be utilized. These guidelines and precautions will minimize the pickup of electrical noise by measuring circuits.

9.5.1 Twisted Pair Input Lines

The effects of magnetic coupling on the input signals may be reduced for differential input configuration by twisting the signal and return lines. This is effective since the inductive pickup voltages on the two lines tend to match, thus not having an effect on the measurement. This is not the case for a ground referenced single ended system.

9.5.2 Shielded Input Lines

The effects of electrostatic coupling may be reduced by shielding the input lines. This becomes important if the source has a high impedance. The shield should only be tied to ground at the instrument end. This will prevent ground loop currents.

9.5.3 Input Settling with High Source Impedance

Solid state multiplexers inject a small amount of charge into the input lines when channels are switched. This can cause a transient error due to the input source impedance time constants. All Data Translation systems allow for input settling upon new channel selection. The settling time varies for the different input systems available.

Normally, the control logic allows sufficient time for this charge to settle to less than ½LSB of error (nine time constants to .012 percent). However, more time may be needed when the multiplexer is switching an input channel with high source impedance, particularly when large amounts of shunt capacitance exists in the interconnecting cables. Source impedance/cable shunt capacitance products greater than 1 uSec (1K-1000PF) on 25KHz units should be avoided for less than 50PF/foot and 1K ohm source impedance.This translates into a maximum run of twenty feet on 25KHz models. Note also that settling errors can be minimized by increasing the internal time out with an external capacitor C_t ($\sim$60PF per uSec).

9.6 Common Mode Rejection Ratio - (CMRR)

The CMRR of a system is defined as the ratio of output voltage from the instrumentation amplifier to the voltage which is common to both sides of the differential input amplifier. This ratio is given in units of decibels.

9.6
(Cont.)

For example, the specification for CMRR on Data Translation's wide range interface is 100db at 60HZ at a gain of 1000. Thus with a CMV of 10 volts, the V out of the amplifier at a gain of 1000 should be:

$$CMRR = 20\log_{10} \left(\frac{CMV}{VOUT/A}\right)$$

Where CMRR = common mode rejection in db
CMV = common mode voltage
VOUT = The change in the amplifier output voltage due to the CMV.
A = Amplifier gain

$$100 = 20\log_{10} \left(\frac{CMV}{VOUT/A}\right)$$

$$\text{Antilog } \left(\frac{100}{20}\right) = \frac{10^4}{VOUT/1000}$$

$$10^5 = \frac{10^4}{VOUT}$$

$$VOUT = 10^{-1} \text{ V.}$$

Thus with a CMV of 10 volts, the output of the instrumentation amplifier is 100 millivolts.

9.7 User Connections

User connections are made via a 26 pin 3M type connector. This connector contains all analog input lines, D/A output lines, and external trigger inputs.

CONNECTOR

J1 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CHØ	2	CH8/RETØ
3	CH1	4	CH9/RET1
5	CH2	6	CH10/RET2
7	CH3	8	CH11/RET3
9	CH4	10	CH12/RET4
11	CH5	12	CH13/RET5
13	CH6	14	CH14/RET6
15	CH7	16	CH15/RET7
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND
21	RTCINL	22	D GND
23	DAC B RET	24	DAC B OUT
25	DAC A RET	26	DAC A OUT

RTCINL on Wire Post

9.8 External Trigger and RTC Inputs

This series of analog interfaces allow the user to externally trigger the conversion. Thus allowing sychronization of conversion to real word or a real time clock input. Data Translation can supply the user with a KVV11-A equivalent module, the DT2769 real time clock module. The two trigger inputs are only edge sensitive and initiate a conversion on the negative (high to low) transition of the input signal only.

CHAPTER 10

10.0 Calibration and Testing

10.1 Equipment and System Requirements

In order to assist the user in testing the operation of the DT2780 series interfaces, Data Translation has developed a comprehensive software diagnostic aid designated SP0031. This software is provided in either of the two media: Paper pape for minimum, paper tape based LSI-11 Systems, or Floppy Disks for more sophisticated RT-11 Systems. The system and test equipment requirements for this software are given below:

SP0031 - All models

SP0031 System Requirements
Paper Tape:

KD11-F (LSI-11) processor, ECO #10 or greater

or

KD11-HA (LSI-11/2) processor

Minimum of 4K words RAM
Serial Interface at Standard DEC console address
Paper tape reader
Data Translation DT2780 series interface.

Floppy Disk

KD11-F (LSI-11) processor, EC) #10 or greater

or

KD11-HA (LSI-11/2) processor

Minimum of 8K words RAM
System console terminal at standard DEC console address
DEC compatible dual floppy disc drive system
RT-11 operating system (Version 2 or Version 3)
Data Translation DT2780 series interface

Test Equipment Requirements

10MHz or greater bandwidth oscilloscope
Laboratory quality voltage standard

10.2 Loading SP0031 from Paper Tape

This software is supplied in PDP-11 absolute loader format. To load this release into memory the following steps must be taken:

1. Load the LSI-11 absolute loader (see DEC documentation for information on this.)

10.2
(Cont.)

2. Place the paper tape in the paper tape reader.

3. Start the absolute loader at location XXX500 where XXX is determined by the following table: (See 10-2)

System Memory Size	XXX
4K	017
8K	037
12K	057
16K	077
20K	017
24K	137
28K or greater	157

Following this procedure will cause SP0023 to be loaded into memory and executed.

10.2.1 Loading Floppy Disk

The SP0031 diskette contain an RT-11 memory image file called SP0031 SAV. This is a linked and executable version of SP0023. To load and execute SP0031, the user should boot up RT-11 in the usual way with the system disk in drive Ø. When RT-11 comes up the user should insert the SP0031 disk into drive 1 and type the following command string to the RT-11 monitor;

RUN DX1:SP0031 (Return)

This will cause SP0031 to be loaded and executed, at this time the SP0031 monitor will have control of the system and RT-11 will be prevented from interfacing.

10.3 Using SP0031

SP0031 is a stand-alone software diagnostic package that allows the user to test Data Translation's dual-height series of LSI-11 interface cards. The test program does not need RT-11 once it has been loaded and in fact it flushes RT-11 from the system after it has loaded. To allow the user to control the testing procedure a monitor has been included that interfaces to the user. When SP0031 is brought up this monitor is automatically entered. On start up the resident monitor prints out the directory of the various Data Translation interface boards that can be tested followed by the monitor prompt character ">" (a right angle-bracket). At this point the user should set the desired model number to be tested using the MODEL command.

10.3
(Cont.) for example:

Model (Space) DT2781 (Return)

would set up the program to test the DT2781 Analog Input Board. The monitor would then invoke all the necessary initialization routines to test this board and confirm the board model by printing out a confirmation message followed by the default base and vector addresses that will be used. These base and vector addresses have been preset at the factory and need not be changed. If for some reason, however, a change in the base or vector address is required, the user can modify locations 542 (base address) and 544 (Vector address) to the new address. In order to easily facilitate this change the SP0031 monitor also has some subset capabilities of ODT. In particular, the user can use the slash and back-slash characters to open and modify memory locations just as in ODT. Therefore, if the user needs to change any location, he should type the address followed by a slash (/) or back-slash ( ), the monitor will then open that location just as in ODt. The user can roll up or down sequentially in memory by using the line feed or carat ( ) keys. The SP0031 monitor is reentered from the ODT mode by typing a carriage return. Like ODT a memory location will only be modified if a valid octal number is typed before any of the ODT terminator characters. For example, to change the base and vector address of the DT2762 tests one would type:

542/177700 170400 (line-feed)

000544/000300 400 (return)

to change the base address to 170400 and vector address to 400. Note that this change is only temporary and the default addresses will be reloaded if the model number is retyped or if SP0031 is reloaded. In addition to these commands the SP0031 test executive allows the user to ask for the model directory, to start tests, to loop or halt on tests or even to reboot RT-11. The commands available to the user under the SP0031 test executive are listed on the following page.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

IL TEST (Space) 2

In this case the program will loop on Test 2 and inhibit error printouts.

If a test is run and no errors occur, the test will return to the SP0031 command level without any other messages. If however, an error does occur, then the test will print out the test number and error code. The user may look up the meaning of each error code in the program listings given in Appendix A.

10.4 Test Descriptions

All descriptions of the tests and the set up requirements needed for any particular test are described in detail in the program listings at the beginning of each test.

10.5 SP0031 Program Description

SP0031 consists of two groups of tests. The first group contains a series of tests which test all the logic of the interface board. These tests contain scope loops for debug purposes and will provide an error message if a problem exists. The second set of tests test the analog operation and calibration of the boards.

A listing of all the tests for testing DT2780 series boards can be found at the beginning of the program listings.

Note that the user can run all the logic tests by using the monitor ALL-command. Calibration tests, however, must be run individually.

COMMAND	FUNCTION
ALL	Runs all logic tests that are present for current device. Generates an error if there is no current device.
BOOT	Jumps to the standard hardware bootstrap (173000). Generates an error if there is no bootstrap present.
DIRECTORY	Displays the contents of the current directory.
EXIT	Halts the processor
MODEL	Displays the parameters associated with the current device. Generates an error if there is no current device.
MODEL (Space) DTXXXX	Searches the current directory for the given model number. If found, makes that model the current device. Generates an error if there is no current directory or if the model number cannot be found.
TEST	Runs the last test executed.
TEST (Space) Octal number	Runs the indicated test.

Test Command prefixes - The following command prefixes are to be

used with the TEST command to control the execution of the various tests.

COMMAND PREFIXES TO TEST EXECUTION COMMANDS

R	(TEST command only)	repeat this test continuously
L	(both TEST and ALL)	Loop on this test if an error is detected.
H	(both TEST and ALL)	halt test stream if an error is detected.
I	(both TEST and ALL)	inhibit error printout

Control-C will terminate any test.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

ILTEST (space) 2

In this case the program will loop on test 2 and inhibit error printouts.

SP0031 Error Codes - SP0031 will print an error code when a specific error is encountered. All codes are in the program listing and show the error and what test the program was in when a failure occured. Use the table of contents printed at the front of the listing to quickly find the lpages in the listing associated with the test that generates the error.

10.6 SP0031 Tests

Logic Tests:

Test 1: BRPLY from all registers
Test 2: Check ADCSR bits
Test 3: BINITL action
Test 4: Byte operation of ADCSR
Test 5: A/D Done bit and interrupt
Test 6: Error bit and interrupt
Test 7: End of logic tests
Calibration Initialization
Displays A/D Data
Test 10: A/D Calibration
Test 11: A/D Input channel scan
Test 12: A/D Input gain/channel scan
DAC Initialization
Test 13: A/D in to D/A out
Test 14: D/A ramps
Test 15: D/A calibration
Test 16: D/A square waves
Test 17: D/A out to A/D In

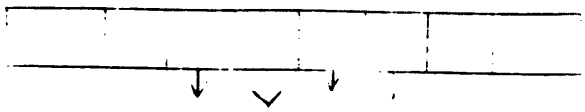
10.6.1 Test Description

All description of tests are located in the program listing at the beginning of each test.

10.6.2 Modes of Operation

Test 10, 11 and 12 will ask for a MODE input when they are called. This MODE input is the lower byte of the CSR.

When a user wants to run an interface under RTC control or EXT TRIG he can set these bits when the program asks for MODES. If a user wants to run under EXT TRIG he will set the MODES as 20_8. The GS0 and GS1 are bits to set the range for the PGX option.



MODE BITS FOR USE IN TEST 10, 11 AND 12.

10.6.3 Calibration

Calibration of the system requires a voltage standard for highly accurate analog inputs and a DVM for calibration of analog inputs. Note: User must calibrate ADC first, followed by the two D/A converters.

Equipment Required:

Voltage standard - EDC Model MV-100 or equivalent
- Data Technology Model 40 or equivalent.

10.6.3.1 Calibration of A/D Converter for DT2781/DT2785

Configuration ±10V FS, 2's complement notation:

1. Connect a Voltage Standard to CHØ input
2. Set standard to -2.4mV
3. Start A/D Calibration test at CHØ, Mode Ø.
4. Adjust A/D offset for the printout between 177777 and ØØØØØ.
5. Set voltage standard to +9.9927V
6. Adjust A/D range control for printout between 003776 and 003777

Note: For ±10mV systems (DT2785) divide above voltage values by 1000. (Octal values remain the same.)

10.6.3.2 27xx/5714 A/D Calibration

Configuration ±10V FS, 2's Complement

1. Connect a voltage standard to CHØ
2. Set standard to -9.99939V
3. Start A/D calibration test (test 19) CHØ, mode Ø.
4. Adjust A/D offset for printout between 173774 and 174003 The two least significant bits are ignored.
5. Reset standard to +9.9982V
6. Adjust A/D range for printout between 3777 and 3774 (2 least significant bits ignored)

10.6.3.3 27xx/5716 A/D Calibration

1. Connect a voltage standard to CHØ.
2. Set standard to -9.99985V
3. Start A/D calibration test (test 10) CHØ, Mode Ø.
4. Adjust A/D offset for printout between 173777 and 174000
5. Reset standard to +9.9991
6. Adjust A/D range for printout between 3777 and 3776.

10.6.3.4 D/A Calibration (Both Channels) Configuration 2's Complement Input

1. Connect lab quality DVM to DAC A out (pin 26). Ground DVM on DAC ret. (pin 25)
2. Start D/A calibration. (test 15)
3. Press space bar on terminal until approximately -10V is read on DVM.
4. Adjust zero put until exactly -10.0000V is read
5. Press space bar until +10V is read
6. Adjust range pot until +9.9951V is read
7. Repeat for DAC B
8. Repeat for DAC A

10.7 Adjustment Values

10.7.1 Notes on Full Scale (FS)

Full Scale (FS) is the amount of input voltage required to turn on all the bits of the A/D converter. For a D/A converter, the inverse is true: Full Scale is the voltage that results when all bits of the converter are turned on.

In a 12 bit converter there are 4096 possible states (2^{12}). Because one of these states is given to zero, the converter lacks one state at its high or positive FS end. Hence even though the converter is rated at 10 volts Full Scale, the positive Full Scale value will actually be 1 state (1 least significant bit value) below 10 volts. For example, a 0-10 volt range converter has a least significant bit value of 2.44V (10 volts / 4096 states). The positive Full Scale will be reached at 10 volts -2.44 mV or 9.99756 volts. The negative full scale (in this instance taken to mean the voltage associated with all converter bits OFF) will be 0 volts.

The Full Scale Range is the difference in voltage between positive Full Scale (all converter bits ON) and negative full scale (all converter bits OFF). Thus a 0-10 volt converter has a Full Scale Range of 10 volts while a ±10 volt converter has a FSR of 20 volts.

10.7.2 Computing Calibration Values for 12 bit ADC

(Note: LSB (least significant bit) = FSR ÷ 4096

10.7.3 A/D Offset Adjustment Values for 12 bit ADC

Unipolar Ranges 0-n Volts, $n \leq 10$

		Adjust for Printout Between	
Input Range	Input Voltage	Low Value	High Value
any	±½LSB	0	1 LSB
any,Octal output	±½LSB	0000	0001
0-10	+1.2207mV	0000	0001
0-5V	+0.6104mV	0000	0001
0-10mV	+1.220uV	0000	0001

Bipolar Ranges (+n Volts, n≤10)

		Adjust for Printout Between	
Input Range	Input Voltage	Low Value	High Value
any	0 volts -½LSB	0 volts -1LSB	0 volts
any, OCTAL output	0 volts -½LSB	177777	000000(2's complement)
±10V	-2.4414mV	008777	004000(offset binary)
±5V	-1.2207mV		
±10mV	-2.4414uV		

10.7.4 A/D Range Adjustment Valves for 12 bit ADC

Unipolar Ranges (0-n Volts, n≤10)

		Adjust for Printout Between	
Input Range	Input Voltage	Low Value	High Value
any	+FS-1½LSB	+FS-2LSB 007776	+FS-1 LSB 007777
any, OCTAL output	+FS-1½LSB		
0-10	+9.9963V		
0-5V	+4.9982V		
0-10mV	+9.9963mV		

Bipolar Ranges (±n Volts, N≤ 10)

		Adjust for Printout between	
Input Range	Input Voltage	Low Value	High Value
any	+FS - 1½LSB	+FS-2LSB	+FS - 1LSB
any, octal output	+FS - 1½LSB	003776	003777(2's complement)
±10V	+9.9927	007776	007777(offset binary)
±5V	+4.9964		
±10mV	+9.9927mV		

10.8 Computing Calibration Values

(Note: LSB (least significant bit) = FSR 16384
Ignore 2 LSB

10.8.1 A/D Offset Adjustment Values

Unipolar Ranges 0-n Volts, n ≤ 10

		Adjust for Printout between	
Input Range	Input Voltage	Low Value	High Value
any	+½LSB	0	1 LSB
any, Octal output	+½LSB	177774	000003
0-10	+.3052mV	177774	000003
0-5V	+1.526mV	177774	000003
0-10mV	+.3052uV	177774	000003

Bipolar Ranges (+n Volts, n ≤ 10)

		Adjust for printout between	
Input Range	Input Voltage	Low Value	High Value
any	0 volts -½LSB	0 volts -1LSB	0 volts
any,OCTAL output	0 volts -½LSB	177777	000000(2's complement)
±10V	-.6104mV	037774	040003(offset binary)
±5V	-1.2207mV-.3052mV		
±10mV	-.6104uV		

10.8.2 A/D Range Adjustment Valves

Unipolar Ranges (0-n Volts, n ≤ 10)

		Adjust for printout between	
Input Range	Input Voltage	Low Value	High Value
any	+FS-1½LSB	+FS-2LSB	+FS-1LSB
any,Octal output	+FS-1½LSB	077774	100003
0-10	+9.99908V		
0-5V	+4.99954V		
0-10mV	+9.99908mV		

Bipolar Ranges		(±nVolts, n 10)	
		Adjust for Printout between	
Input Range	Input Voltage	Low Value	High Value
any	+FS - 1½LSB	+FS-2LSB	+FS-1LSB
any,octal output	+FS-1½LSB	037774	040003(2's complement)
±10V	+9.9927+9.99817V	077774	100003(offset binary)
±5V	+4.9964+4.99908V		
±10mV	+9.9927mV+9.99817mV		

10.9 Adjustment Values

10.9.1 Notes on Full Scale (FS)

Full Scale (FS) is the amount of input voltage required to turn on all the bits of the A/D converter. For a D/A converter, the inverse is true: Full Scale is the voltage that results when all bits of the converter are turned on.

In a 12 bit converter there are 4096 possible states (2^{12}). Because one of these states is given to zero, the converter lacks one state at its high or positive FS end. Hence even though the converter is rated at 10 volts Full Scale, the positive Full Scale value will actually be 1 state (1 least significant bit value) below 10 volts. For example, a 0-10 volt range converter has a least significant bit value of 2.44V (10 volts / 4069 states). The positive Full Scale will be reached at 10 volts -2.44mV or 9.99756 volts. The negative full scale (in this instance taken to mean the voltage associated with all converter bits OFF) will be 0 volts.

The Full Scale Range is the difference in voltage between positive Full Scale (all converter bits ON) and negative full scale (all converter bits OFF). Thus a 0-10 volt converter has a Full Scale Range of 10 volts while a ±10 volt converter has a FSR of 20 volts.

10.9.2 Computing Calibration Values for 16 bit ADC

(Note: LSB 9least significant bit) = FSR 65536

10.9.3 A/D Offset Adjustment Valves

Unipolar Ranges (0-n Volts, n 10)

		Adjust for printout between	
Input Range	Input Voltage	Low Value	High Value
any	+½LSB	0	1LSB
any,Octal output	+½LSB	000000	000001
0-10	+.1526mV	000000	000001
0-5V	+.076294mV	000000	000001
0-10mV	+.1526uV	000000	000001

10.9.4 A/D Range Adjustment Valves for 16 bit ADC

Unipolar Ranges (0-n Volts, n 10)

		Adjust for Printout between	
Input Range	Input Voltage	Low Value	High Value
any	+FS-½LSB	+FS-2LSB	+FS-1LSB
any,Octal output	+FS-1½LSB	177776	177777
0-10	+9.99977V		
0-5V	+4.99988V		
0-10mV	+9.99977mV		

Bipolar Ranges (±n Volts, N 10)

		Adjust for printout between	
Input Range	Input Voltage	Low Value	High Value
any	+FS -1½LSB	+FS-2LSB	+FS-1LSB
Any,Octal output	+FS-1½LSB	077776	077777(2's complement)
±10V	+9.99969V	177776	177777(offset binary)
±5V	+4.99985V		
±10mV	+9.99969mV		

CHART OF INPUT RANGE PARAMETERS

INPUT RANGE				Cext (in uF)			AMPLIFIER SETTLING TIME (in Millisec)			SYSTEM ACCURACY			THROUGHPUT RATE (in Hz)		
Unipolar	Bipolar	GAIN	Rext (in Ohms)	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712	DT5716	DT5714	DT5712
0 to +5mV	±5mV	2000	50.02	0.470	0.100	0.056	24.0	6.0	3.0	±.13%	±.14%	±.18%	40	166	333
0 to +10mV	±10mV	1000	100.10*	0.220	0.056	0.022	12.0	3.0	1.5	±.06%	±.08%	±.10%	80	333	666
0 to +25mV	±25mV	400	250.62*	0.082	0.022	0.010	4.8	1.2	.6	±.035%	±.040%	±.08%	200	833	1600
0 to +50mV	±50mV	200	502.51*	0.039	0.010	0.0047	2.4	.6	.3	±.020%	±.022%	±.07%	400	1600	3200
0 to 100mV	±100mV	100	1,010.1*	.022	0.0047	0.0022	1.2	.3	.15	±.010%	±.020%	±.05%	800	3300	6600
0 to +1V	±1V	10	11,111*	None	None	None	.3	.07	.025	±.010%	±.015%	±.03%	2500	10,000	20,000
0 to +2.5V	±2.5V	4	33,333*	None	None	None	.3	.07	.025	±.010%	±.012%	±.03%	2500	10,000	20,000
0 to +5V	±5V	2	100,000*	None	None	None	.3	.07	.025	±.009%	±.01%	±.03%	2500	10,000	20,000
0 to +10V	±10V	1	NONE	None	None	None	.3	.07	.025	±.0075%	±.01%	±.03%	2500	10,000	20,000

* These resistors are offered as aPrecision Resistor Gain Selection Kit, Model number DT13-10501-4, for high accuracy gain setting.

REXT = 100,000 / (G-1)

$$\text{Throughput Time} = \frac{1}{\text{Amplifier Settling Time} + \text{A/D Conversion Time}}$$

APPENDIX A

DIAGNOSTIC LISTINGS

```
RT-11 LINK  V05.04A      LOAD MAP          FRI 28-DEC-79 08:45:32
SP0031.LDA       TITLE:  SP0031  IDENT:  V01.01

SECTION  ADDR    SIZE     GLOBAL  VALUE    GLOBAL  VALUE    GLOBAL  VALUE

. ABS.   000000  001000    (RW,I,GBL,ABS,OVR)
SP0031   001000  000050    (RW,I,LCL,REL,CON)
                          DIRECT  001000
DT2781   001050  003460    (RW,I,LCL,REL,CON)
                          T2781   001050  T2785   001050  I2781   001150
                          I2785   001150
TST11    004530  006434    (RW,I,LCL,REL,CON)
                          START   004530

TRANSFER ADDRESS = 004530, HIGH LIMIT = 013164 =  2874  WORDS
```

TABLE OF CONTENTS

```
                        .LIST   TTM
                        .ENABL  LC
                        .TITLE  DT2781  TST-11 MODULE
                        .IDENT  /V01.02/
000000                  .PSECT  DT2781
                .NLIST  BIN
        ;
        ;
                .SBTTL  GENERAL INFORMATION
        ;
        ;
        ; COPYRIGHT (C) 1979, DATA TRANSLATION INCORPORATED.  ALL
        ; RIGHTS RESERVED. NO PART OF THIS PROGRAM OR PUBLICATION
        ; MAY BE REPRODUCED WITHOUT THE PRIOR WRITTEN PERMISSION
        ; OF  DATA TRANSLATION INCORPORATED.  4 STRATHMORE ROAD.
        ; NATICK, MASS. 01760.
        ;
        ;
        ; THE INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE
        ; WITHOUT  NOTICE  AND  SHOULD  NOT  BE  CONSTRUED AS A
        ; COMMITMENT BY DATA TRANSLATION INCORPORATED
        ;
        ;
        ; DATA TRANSLATION CANNOT ASSUME ANY RESPONSIBILITY FOR
        ; THE USE OF ANY PORTION OF THIS SOFTWARE FOR OTHER THAN
        ; ITS INTENDED  DIAGNOSTIC  PURPOSE  IN CALIBRATING AND
        ; TESTING  DATA  TRANSLATION  MANUFACTURED  ANALOG  AND
        ; DIGITAL INTERFACE BOARDS.
        ;
        ;
        ;
        ; VERSION 01-02
        ;
        ; PHILLIP MARTINEZ 27-JUL-79
        ; PHILLIP MARTINEZ 28-DEC-79
        ;
        ;
        ; THIS PROGRAM MODULE CONTAINS ROUTINES TO TEST AND
        ; CALIBRATE DTI DT2781 AND DT2785  SERIES ANALOG
        ; INTERFACE SYSTEMS FOR THE LSI-11  A COMPLETE LISTING
        ; OF THE MODELS TESTED BY THIS CODE MODULE WILL BE FOUND
        ; ON THE FOLLOWING PAGES.  THIS MODULE IS DESIGNED TO
        ; OPERATE UNDER TST-11 SUPERVISION
        ;
                        .LIST   BIN
```

```
                ;
                ;
                ;
                ;       THE DIFFERENCES BETWEEN V01-02 AND V01-01 ARE
                ;       1).  THE TIMING IN TEST 3 HAS BEEN CHANGED TO
                ;            WAIT A FULL CONVERSION TIME BETWEEN TRIGGERS
                ;            BEFOR THE BINIT SIGNAL IS CYCLED
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
                ;
```

```
                        .SBTTL  TEST PARAMETER BLOCK (TPB)
                ;
                ; TEST-11 DECLARATION
                ;
                        .MCALL  TST11
000000                  TST11
                ;
                ;
                ; ADDITIONAL PARAMETERS USED BY THIS DIAGNOSTIC
                ;
                ;
        000546  DELAY   =546            ; A/D DELAY COUNT STORAGE
                ;
        000522  ERRCNT  =522            ; ERROR COUNTER
                ;
                ;
                ; TEST PARAMETER BLOCK
                ;
                .NLIST  BIN
        ;
000000  TPB:    .WORD   PARAM           ; ADDRESS OF PARAMETER
                                        ; PRINT-OUT ROUTINE
000002          .BYTE   377             ; RESERVED
000003          .BYTE   17              ; # OF TESTS
        ;
        ; TEST ADDRESS TABLE FOR USE BY TST-11
        ;
000004          .WORD   TEST1,PR7
000010          .WORD   TEST2,PR7
000014          .WORD   TEST3,PR7
000020          .WORD   TEST4,PR7
000024          .WORD   TEST5,PR7
000030          .WORD   TEST6,PR7
000034          .WORD   TEST7,PR7
000040          .WORD   TEST10,0
000044          .WORD   TEST11,0
000050          .WORD   TEST12,0
000054          .WORD   TEST13,0
000060          .WORD   TEST14,0
000064          .WORD   TEST15,0
000070          .WORD   TEST16,0
000074          .WORD   TEST17,0
        ;
                        .LIST   BIN
```

```
                                        .SBTTL  INITIALIZATION
                                ;
000100  005037  000540  INIT81:  CLR     @#SWR                   ; INPUT ONLY MODE!
000104  012737  000310          MOV     #200.,@#DELAY           ; SET WORST CASE DELAY
        000546
000112                  INIT:   RELMOV  #CHNL,R1                ; CHECK SE OR DI
000120  004767  000074          CALL    QUERY
000124  103407                  BCS     1$                      ; IS SE
000126                          SET     BIT6,SWR                ; IS DI
000134  012737  000020          MOV     #20.,@#ODTACC           ; SET CHANNEL NUMBER
        000514
000142  000403                  BR      2$
                                ;
000144  012737  000010  1$:     MOV     #10.,@#ODTACC           ; SET CHANNEL NUMBER
        000514
000152                  2$:     RELMOV  #DACTYP,R1              ; CHECK DAC TYPE
000160  004767  000034          CALL    QUERY
000164  103403                  BCS     3$                      ; DAC IS OFFSET BINARY
000166                          SET     BIT7,SWR                ; DAC IS 2'S COMPLEMENT
000174  113737  000514  3$:     MOVB    @#ODTACC,@#SWR+1
        000541
000202  012737  170400          MOV     #170400.,@#BASE         ; SET DEFAULT ADDRESS
        000542
000210  012737  000400          MOV     #400.,@#VECTOR          ; SET DEFAULT VECTOR
        000544
000216  000207                  RETURN                          ; ALL DONE
```

```
                        QUERY:  PUSH    R1                      ; SAVE POINTER
                                PRINTS                          ; PRINT PROMPT
                                PRINT   < (Y OR N)? >
                                TTYIN
000244  122700                  CMPB    #'Y,R0                  ; A "Y"?
        000131
000250  001427                  BEQ     2$
000252  122700                  CMPB    #'N,R0                  ; A "N"?
        000116
000256  001422                  BEQ     1$                      ; YES
000260                          CRLF
000262                          PRINTC  <SEE MANUAL FOR ASSISTANCE >
000320                          POP     R1                      ; RESTORE POINTER
000322  000736                  BR      QUERY
                        ;
000324  000261          1$:     SEC                             ; SET CARRY FLAG
000326  000401                  BR      3$
000330  000241          2$:     CLC                             ; CLEAR CARRY FLAG
000332                  3$:     TTYOUT                          ; ECHO CHARACTER
000334                          CRLF
000336                          POP     R1                      ; RESTORE R1
000340  000207                  RETURN
                        ;
                        ;
                        .NLIST  BIN
000342  SPEED:           .ASCIZ  "100 KHZ A/D MODULE"
000365  DACTYP:         .ASCIZ  "2'S COMPLEMENT "
000405  CHNL:           .ASCIZ  "IS BOARD SE "
                        .EVEN
                                .LIST   BIN
                        ;
                        ;
                        ;
                                .SBTTL  DISPLAY PARAMETERS
                        ;
                        ;       THIS ROUTINE DISPLAYS THE CURRENT SETTING
                        ;       OF 'BASE' AND 'VECTOR' ON THE SYSTEM CONSOLE
                        ;       TERMINAL.
                        ;
000422                  PARAM:  PRINT   <BASE ADDRESS = >
000444  013700                  MOV     @#BASE,R0               ; GET BASE ADDRESS
        000542
000450                          OCT16                           ; DISPLAY
000452                          CRLF
000454                          PRINT   <VECTOR ADDRESS = >
000500  013700                  MOV     @#VECTOR,R0             ; GET VECTOR ADDRESS
        000544
000504                          OCT16                           ; DISPLAY
000506                          CRLF
000510  000207                  RETURN                          ; ALL DONE
```

```
                        .SBTTL  ERROR REPORTERS
                ;
                ;
                ; THIS ROUTINE PROVIDES ERROR REPORTING FOR BUS
                ; TIME-OUT ERRORS (NO BRPLY FROM INTERFACE)
                ;
000512          NORPLY: PRINT   <NO BRPLY WHEN ACCESSING LOCATION >
000556  010100          MOV     R1,R0
000560                  OCT16                   ; DISPLAY ADDRESS
000562                  CRLF
000564  000207          RETURN                  ; DONE
                ;
                ;
                ; THIS ROUTINE PROVIDES ERROR REPORTING FOR REGISTER
                ; BIT ERRORS (ONE OR MORE INCORRECT BITS IN A REGISTER)
                ;
000566          REG:    PRINTC  <REGISTER ERROR>
000610                  PRINT   <ADDRESS: >
000624                  PUSH    R0              ; SAVE R0
000626  010100          MOV     R1,R0           ; GET ADDRESS
000630                  OCT16
000632                  CRLF
000634                  PRINT   <EXPECTED:>
000650  010200          MOV     R2,R0           ; GET EXPECTED VALUE
000652                  OCT16                   ; DISPLAY
000654                  CRLF
000656                  PRINT   <FOUND:    >
000672  011600          MOV     (SP),R0         ; GET BAD BITS
000674  074200          XOR     R2,R0           ; GENERATE SNAPSHOT
000676                  OCT16                   ; DISPLAY
000700                  CRLF                    ; FORMATTING
000702                  PRINT   <BITS:     >
000716                  POP     R0              ; GET ERROR BITS
000720                  OCT16                   ; DISPLAY
000722                  CRLF
000724  000207          RETURN                  ; DONE
```

```
                        .SBTTL  MODEL TESTING INFORMATION
                .NLIST  BIN
        ;
        ; THIS CODE MODULE CONTAINS THE ROUTINES NECESSARY
        ; TO TEST THE FOLLOWING DTI INTERFACE MODELS:
        ;
        ;
        ;
        ;
        ;       DT2781  HIGH LEVEL ANALOG INPUT
        I2781   ==INIT81
        T2781   ==TPB
        ;
        ;
        ;       DT2785  WIDE RANGE ANALOG INPUT
        I2785   ==INIT81
        T2785   ==TPB
        ;
        ;
        ;
                        .LIST   BIN
                ;
                ;
                ; SOFTWARE SWITCH REGISTER BIT RESERVATIONS
                ;
                ; BITS 14-15:   NOT USED
                ; BITS 13-8:    # OF A/D CHANNELS
                ; BIT 7:        2'S COMPLEMENT
                ; BIT 6:        DI MODULE PRESENT
                ; BITS 3-5:     NOT USED
                ; BITS 2-0:     RESERVED
```

```
                        .SBTTL  LOGIC TESTS
                        .SBTTL  TEST 1:  BRPLY FROM ALL REGISTERS
                ;
                ; THIS TEST VERIFIES THAT THE INTERFACE SYSTEM RESPONDS
                ; WITH A BUS REPLY SIGNAL DURING A BUS DATIO BUS CYCLE
                ; ALL REGISTERS AVAILABLE ON THE BOARD ARE CHECKED
                ;
                ;
000726  010602  TEST1:  MOV     SP,R2           ; SAVE SP
000730
000736  010037          RELMOV  #2$,R0          ; SET UP TRAP TO 4
        000004          MOV     R0,@#4
000742  013701  1$:     MOV     @#BASE,R1       ; GET ADDRESS
        000542
000746                  SCOPE                   ; DECLARE LOOP POINT
000750  005011          CLR     (R1)            ; DATIO BUS CYCLE
000752                  SCOPE                   ; DECLARE LOOP POINT
000754  062701          ADD     #2,R1           ; NEXT REGISTER
        000002
000760                  SCOPE                   ; DECLARE LOOP POINT
000762  005011          CLR     (R1)            ; DATIO BUS CYCLE
000764                  SCOPE                   ; DECLARE LOOP POINT
000766  062701          ADD     #2,R1           ; NEXT REGISTER
        000002
000772                  SCOPE                   ; DECLARE LOOP POINT
000774  005011          CLR     (R1)            ; DATIO BUS CYCLE
000776                  SCOPE                   ; DECLARE LOOP POINT
001000  062701          ADD     #2,R1           ; NEXT REGISTER
        000002
001004                  SCOPE                   ; DECLARE LOOP POINT
001006  005011          CLR     (R1)            ; DATIO BUS CYCLE
001010                  EXIT
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 1 - BUS TIMEOUT
                ;
                ; ********************************************************
                ;
001012  011603  2$:     MOV     (SP),R3         ; GET OFFENDING PC
001014  010206          MOV     R2,SP           ; RESTORE STACK
001016                  ERROR   1,NORPLY        ; REPORT ERROR
001022  000113          JMP     (R3)            ; CONTINUE TEST
```

```
                        .SBTTL  TEST 2:  CHECK ADCSR BITS
                ;
                ; THIS TEST CHECKS MOST OF THE BITS IN ADCSR.
                ; BITS ARE CHECKED FOR BOTH SET AND RESET CAPABILITY
                ; THE BIT THAT IS NOT CHECKED IS THE A/D DONE BIT
                ; IT IS CHECKED IN OTHER TESTS.
                ;
001024  013701  TEST2:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001030  005002          CLR     R2              ; INIT TEST REG.
001032  012703          MOV     #40,R3          ; SET # OF STATES
        000040
001036                  SCOPE                   ; DECLARE LOOP POINT
001040  010211  1$:     MOV     R2,(R1)         ; SET BITS
001042  013704          MOV     @#DELAY,R4      ; SET COUNTER
        000546
001046  077401  2$:     SOB     R4,2$           ; DELAY FOR SETTELING
001050  011100          MOV     (R1),R0         ; GET BITS
001052  042700          BIC     #177600,R0      ; IGNORE HIGH BYTE
        177600
001056  074200          XOR     R2,R0           ; TEST BITS
001060  001402          BEQ     3$              ; NO ERROR - SKIP
                ;
                ; ***************************************************
                ;
                ;       ERROR CODE 2 - BIT ERROR, ADCSR
                ;                       BITS 0-6
                ;
                ; ***************************************************
                ;
001062                  ERROR   2,REG           ; REPORT ERROR
                ;
001066  062702  3$:     ADD     #4,R2           ; NEXT STATE
        000004
001072  077316          SOB     R3,1$           ; LOOP UNTIL DONE
001074  005002          CLR     R2              ; INIT TEST REG
001076  012703          MOV     #16,R3          ; SET # OF STATES
        000016
001102                  SCOPE                   ; DECLARE LOOP POINT
001104  010211  4$:     MOV     R2,(R1)         ; SET BITS
001106  013704          MOV     @#DELAY,R4      ; SET COUNTER
        000546
001112  077401  5$:     SOB     R4,5$           ; DELAY
001114  011100          MOV     (R1),R0         ; GET BITS
001116  042700          BIC     #170377,R0      ; IGNORE LOW BYTE
        170377
001122  074200          XOR     R2,R0           ; TEST BITS
001124  001402          BEQ     6$              ; NO ERROR - SKIP
                ;
                ; ***************************************************
                ;
                ;       ERROR CODE 3 - BIT ERROR, ADCSR
                ;                       BITS 8-11
                ;
                ; ***************************************************
                ;
001126                  ERROR   3,REG           ; REPORT ERROR
```

```
 1
 2                              ;
 3 001132  062702  6$:     ADD     #400,R2          ; NEXT STATE
           000400
 4 001136  077316          SOB     R3,4$            ; LOOP UNTIL DONE
 5 001140  005002          CLR     R2
 6 001142  012703          MOV     #4,R3            ; SET NUMBER OF STATES
           000004
 7 001146                  SCOPE
 8 001150  010211  7$:     MOV     R2,(R1)          ; SET BITS
 9 001152  013704          MOV     @#DELAY,R4       ; SET COUNTER
           000546
10 001156  077401  8$:     SOB     R4,8$            ; WAIT TO FINISH
11 001160  011100          MOV     (R1),R0          ; GET BITS
12 001162  042700          BIC     #37777,R0        ; IGNORE SOME BITS
           037777
13 001166  074200          XOR     R2,R0            ; TEST BITS
14 001170  001402          BEQ     9$               ; NO ERROR SKIP
15                         ;
16                         ; ***************************************************
17                         ;
18                         ;       ERROR CODE 4 - BIT ERROR ADCSR
19                         ;                      BITS 14 AND 15
20                         ;
21                         ; ***************************************************
22                         ;
23 001172                  ERROR   4,REG            ; REPORT ERROR
24                         ;
25 001176  062702  9$:     ADD     #40000,R2        ; NEXT STATE
           040000
26 001202  077316          SOB     R3,7$            ; LOOP TILL DONE
27 001204                  EXIT
```

```
                        .SBTTL  TEST 3:  BINITL ACTION
                ;
                ; THIS TEST VERIFIES THAT THE BINITL SIGNAL CLEARS
                ; THE PROPER ADCSR BITS.
                ;
                ;
001206  013701  TEST3:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001212  012711          MOV     #40101,(R1)     ; SET BITS
        040101
001216  013700          MOV     @#DELAY,R0      ; WAIT FOR A/D DONE
        000546
001222  077001  1$:     SOB     R0,1$
001224  105211          INCB    (R1)            ; SET ERROR BIT
001226  005002          CLR     R2              ; CLR TEST REG
001230                  SCOPE                   ; DECLARE LOOP POINT
001232  013700          MOV     @#DELAY,R0      ; WAIT FOR A/D DONE
        000546
001236  077001  2$:     SOB     R0,2$
001240  000005          RESET                   ; ISSUE BINITL
001242  011100          MOV     (R1),R0         ; GET BITS
001244  042700          BIC     #37476,R0       ; IGNORE SOME BITS
        037476
001250  074200          XOR     R2,R0           ; TEST BITS
001252  001402          BEQ     3$              ; OK - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 5 - PROPER BIT(S) NOT CLEARED
                ;                       BY BINITL
                ;
                ; ********************************************************
                ;
001254                  ERROR   5,REG           ; REPORT ERROR
                ;
001260          3$:     EXIT                    ; ALL DONE
```

```
                        .SBTTL  TEST 4:  BYTE OPERATION OF ADCSR
                ;
                ; THIS TEST VERIFIES HIGH AND LOW BYTE OPERATIONS
                ; INVOLVING THE ADCSR.
                ;
                ;
001262  013701  TEST4:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001266  005011          CLR     (R1)            ; CLEAR ADCSR
001270  005002          CLR     R2              ; INIT. TEST REGISTER
001272                  SCOPE                   ; DECLARE LOOP POINT
001274  112711          MOVB    #-1,(R1)        ; SET R/W BITS
        177777
001300  013705          MOV     @#DELAY,R5      ; WAIT TO SETTLE
        000546
001304  077501  1$:     SOB     R5,1$
001306  011100          MOV     (R1),R0         ; GET ADCSR AS WORD
001310  042700          BIC     #100377,R0      ; IGNORE LOW BYTE
        100377
001314  074200          XOR     R2,R0           ; TEST BITS
001316  001402          BEQ     2$              ; OK - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 6 - HIGH BYTE LOADED DURING
                ;                       A LOW BYTE OPERATION
                ;
                ; ********************************************************
                ;
001320                  ERROR   6,REG           ; REPORT ERROR
                ;
001324  005011  2$:     CLR     (R1)            ; CLEAR ADCSR
001326  005002          CLR     R2              ; INIT. TEST REGISTER
001330  005201          INC     R1              ; POINT TO HIGH BYTE
001332                  SCOPE                   ; DECLARE LOOP POINT
001334  013705          MOV     @#DELAY,R5      ; WAIT TO SETTLE
        000546
001340  077501  3$:     SOB     R5,3$
001342  112711          MOVB    #-1,(R1)        ; SET R/W BITS
        177777
001346  016100          MOV     -1(R1),R0       ; GET ADCSR AS WORD
        177777
001352  042700          BIC     #177600,R0      ; IGNORE HIGH BYTE
        177600
001356  074200          XOR     R2,R0           ; TEST BITS
001360  001402          BEQ     4$              ; OK - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 7 - LOW BYTE LOADED DURING
                ;                       A HIGH BYTE OPERATION
                ;
                ; ********************************************************
                ;
001362                  ERROR   7,REG           ; REPORT ERROR
                ;
001366          4$:     EXIT
```

```
                        .SBTTL  TEST 5:  A/D DONE BIT AND INTERRUPT
                ;
                ; THIS TEST VERIFIES THAT THE A/D DONE BIT CAN
                ; BE SET PROPERLY AND THAT THE INT ENB BIT
                ; FUNCTIONS PROPERLY.
                ;
                ;
001370  013701  TEST5:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001374  013702          MOV     @#VECTOR,R2     ; GET VECTOR ADDRESS
        000544
001400  005761          TST     2(R1)           ; CLEAR A/D DONE BIT
        000002
001404  005011          CLR     (R1)            ; CLEAR ADCSR
001406                  SCOPE                   ; DECLARE LOOP POINT
001410  105211          INCB    (R1)            ; SET A/D DONE BIT
001412  013700          MOV     @#DELAY,R0      ; WAIT FOR A/D DONE
        000546
001416  077001  1$:      SOB     R0,1$
001420  105711          TSTB    (R1)            ; IS BIT SET?
001422  100402          BMI     2$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 10 - A/D DONE BIT NOT SET
                ;
                ; ********************************************************
                ;
001424                  ERROR   10              ; REPORT ERROR
001426  000457          BR      8$              ; CAN'T CONTINUE
                ;
001430          2$:     SCOPE                   ; DECLARE LOOP POINT
001432  005761          TST     2(R1)           ; READ ADDBR
        000002
001436  105711          TSTB    (R1)            ; DONE BIT CLEAR?
001440  100002          BPL     3$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 11 - A/D DONE BIT NOT CLEARED
                ;                       AFTER A/D DATA WAS READ
                ;
                ; ********************************************************
                ;
001442                  ERROR   11              ; REPORT ERROR
001444  000450          BR      8$              ; CAN'T CONTINUE
```

```
    1 001446  005003  3$:     CLR     R3                  ; PREPARE STATUS WORDS
    2 001450  012704          MOV     #PR7,R4
              000340
    3 001454                  RELMOV  #5$,R0              ; GET ISR ADDRESS
    4 001462  010012          MOV     R0,(R2)             ; STORE
    5 001464  010462          MOV     R4,2(R2)            ; STORE STATUS TOO
              000002
    6 001470                  SCOPE                       ; DECLARE LOOP POINT
    7 001472  105211          INCB    (R1)                ; SET A/D DONE
    8 001474  013700          MOV     @#DELAY,R0          ; WAIT FOR DONE
              000546
    9 001500  077001  4$:     SOB     R0,4$
   10 001502  052711          BIS     #100,(R1)           ; ENABLE INTERRUPTS
              000100
   11 001506  106403          MTPS    R3                  ; ENABLE CPU INTERRUPTS
   12 001510  000240          NOP                         ; STALL TIME
   13 001512  106404          MTPS    R4                  ; TURN OFF CPU
   14                 ;
   15                 ; ***************************************************
   16                 ;
   17                 ;       ERROR CODE 12 - NO INTERRUPT ON A/D DONE
   18                 ;
   19                 ; ***************************************************
   20                 ;
   21 001514                  ERROR   12                  ; REPORT ERROR
   22 001516  000423          BR      8$                  ; CAN'T CONTINUE
   23                 ;
   24 001520  062706  5$:     ADD     #4,SP               ; ADJUST STACK
              000004
   25 001524                  SCOPE                       ; DECLARE LOOP POINT
   26 001526  005761          TST     2(R1)               ; READ ADDRR
              000002
   27 001532  105711          TSTB    (R1)                ; A/D DONE CLEAR?
   28 001534  100002          BPL     6$                  ; YES - EXIT
   29                 ;
   30                 ; ***************************************************
   31                 ;
   32                 ;       ERROR CODE 13 - A/D DONE BIT NOT CLEARED
   33                 ;                       AFTER A/D DATA WAS READ
   34                 ;
   35                 ; ***************************************************
   36                 ;
   37 001536                  ERROR   13                  ; REPORT ERROR
   38 001540  000412          BR      8$                  ; CAN'T CONTINUE
```

TEST 5: A/D DONE BIT AND INTERRUPT

```
     1 001542           6$:     SCOPE                   ; DECLARE LOOP POINT
     2 001544  005761           TST     2(R1)           ; CLEAR DONE
               000002
     3 001550  005011           CLR     (R1)            ; CLEAR ADCSR
     4 001552  005211           INC     (R1)            ; START CONVERSION
     5 001554  105711   7$:     TSTB    (R1)            ; WAIT FOR DONE
     6 001556  100376           BPL     7$
     7 001560  005711           TST     (R1)            ; ERROR BIT SET?
     8 001562  100001           BPL     8$              ; NO - EXIT
     9                  ;
    10                  ; ********************************************************
    11                  ;
    12                  ;       ERROR CODE 14 - ERROR BIT SET AFTER NORMAL
    13                  ;                       A/D TRIGGERING SEQUENCE
    14                  ;
    15                  ; ********************************************************
    16                  ;
    17 001564                   ERROR   14              ; REPORT ERROR
    18                  ;
    19 001566  005761   8$:     TST     2(R1)           ; CLEAR DONE
               000002
    20 001572  005011           CLR     (R1)
    21 001574                   EXIT
```

```
                        .SBTTL  TEST 6:  ERROR BIT AND INTERRUPT
                ;
                ; THIS TEST VERIFIES THAT THE ERROR BIT CAN BE SET
                ; PROPERLY AND THAT THE ERR INT ENB BIT FUNCTIONS
                ; CORRECTLY.
                ;
                ;
001576  013701  TEST6:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001602  013702          MOV     @#VECTOR,R2     ; GET VECTOR ADDRESS
        000544
001606  062702          ADD     #4,R2           ; ADJUST VECTOR
        000004
001612  005761          TST     2(R1)           ; CLEAR A/D DONE BIT
        000002
001616                  SCOPE                   ; DECLARE LOOP POINT
001620  005011          CLR     (R1)            ; CLEAR ADDER
001622  005711          TST     (R1)            ; ERROR CLEAR?
001624  100002          BPL     1$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 15 - ERROR BIT NOT CLEAR
                ;
                ; ********************************************************
                ;
001626                  ERROR   15              ; REPORT ERROR
001630  000441          BR      5$              ; CAN'T CONTINUE
                ;
001632          1$:     SCOPE                   ; DECLARE LOOP POINT
001634  105211          INCB    (R1)            ; SET A/D DONE BIT
001636  105711  2$:     TSTB    (R1)            ; TEST FOR DONE
001640  100376          BPL     2$              ; WAIT FOR DONE
001642  105211          INCB    (R1)            ; SET ERROR BIT
001644  005711          TST     (R1)            ; IS BIT SET?
001646  100402          BMI     3$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 16 - ERROR BIT NOT SET
                ;
                ; ********************************************************
                ;
001650                  ERROR   16              ; REPORT ERROR
001652  000430          BR      5$              ; CAN'T CONTINUE
```

```
 1 001654  005003  3$:     CLR     R3              ; PREPARE STATUS WORDS
 2 001656  012704          MOV     #PR7,R4
           000340
 3 001662                  RELMOV  #4$,R0          ; GET ISR ADDRESS
 4 001670  010012          MOV     R0,(R2)         ; STORE
 5 001672  010462          MOV     R4,2(R2)        ; STORE STATUS TOO
           000002
 6 001676                  SCOPE                   ; DECLARE LOOP POINT
 7 001700  052711          BIS     #40000,(R1)     ; ENABLE INTERRUPTS
           040000
 8 001704  106403          MTPS    R3              ; ENABLE CPU INTERRUPTS
 9 001706  000240          NOP                     ; STALL TIME
10 001710  106404          MTPS    R4              ; TURN OFF CPU
11                  ;
12                  ; ******************************************************
13                  ;
14                  ;       ERROR CODE 17 - NO INTERRUPT ON ERROR
15                  ;
16                  ; ******************************************************
17                  ;
18 001712                  ERROR   17              ; REPORT ERROR
19 001714  000407          BR      5$              ; CAN'T CONTINUE
20                  ;
21 001716  062706  4$:     ADD     #4,SP           ; ADJUST STACK
           000004
22 001722                  SCOPE                   ; DECLARE LOOP POINT
23 001724  005011          CLR     (R1)            ; CLEAR ERROR BIT
24 001726  005711          TST     (R1)            ; CHECK BIT
25 001730  100001          BPL     5$              ; CLEAR - SKIP ERROR
26                  ;
27                  ; ******************************************************
28                  ;
29                  ;       ERROR CODE 20 - ERROR BIT NOT CLEAR
30                  ;
31                  ; ******************************************************
32                  ;
33 001732                  ERROR   20              ; REPORT ERROR
34                  ;
35 001734  005761  5$:     TST     2(R1)           ; CLEAR DONE
           000002
36 001740  005011          CLR     (R1)            ; CLEAR ADCSR
37 001742                  EXIT
```

```
                        .SBTTL  TEST 7:  END OF LOGIC TESTS
                ;
                ; THIS TEST IS PRESENT TO INFORM THE TST-11 MONITOR
                ; THAT THERE ARE NO MORE ADDITIONAL LOGIC TESTS
                ; TO BE EXECUTED.  WHEN THE "ALL" COMMAND IS USED.
                ; THIS TEST WILL FORCE A RETURN TO THE COMMAND
                ; LEVEL OF TST-11 WHEN THE TEST SEQUENCER REACHES
                ; THIS TEST.
                ;
                ;
001744          TEST7:  ESCAPE
                ;
                ;
                        .SBTTL  CALIBRATION INITIALIZATION
                ;
                ; THIS ROUTINE PERFORMS INITIALIZATION FUNCTIONS
                ; FOR SOME OF THE CALIBRATION TESTS.
                ;
                ;
001746          GETCH:  PRINT   <CHANNEL? >             ; OUTPUT PROMPT
001762                  GETOCT                          ; GET VALUE
001764  103422          BCS     1$                      ; CR AT END - CONT
001766                  PRINTC  <ENTER AN OCTAL CHANNEL ADDRESS >
002030  000746          BR      GETCH                   ; TRY AGAIN
                ;
002032  013701  1$:     MOV     @#BASE,R1               ; GET ADDRESS
        000542
002036  013702          MOV     @#ODTACC,R2             ; GET VALUE
        000514
002042  000302          SWAB    R2                      ; ADJUST
002044          2$:     PRINT   <MODE BITS? >           ; OUTPUT PROMPT
002062                  GETOCT                          ; GET VALUE
002064  103420          BCS     3$                      ; CR AT END - CONT
002066                  PRINTC  <ENTER AN OCTAL BYTE VALUE >
002124  000747          BR      2$
                ;
002126  042702  3$:     BIC     #377,R2                 ; CLEAR LOW BYTE R2
        000377
002132  013700          MOV     @#ODTACC,R0             ; GET VALUE
        000514
002136  042700          BIC     #177400,R0              ; CLEAR HIGH BYTE,R0
        177400
002142  060002          ADD     R0,R2                   ; ADD IN MODE BYTE
002144  005761          TST     2(R1)                   ; CLEAR DONE
        000002
002150  005011          CLR     (R1)                    ; CLEAR BOARD
002152  000207          RETURN
```

```
                        .SBTTL  DISPLAY A/D DATA
                ;
                ; THIS ROUTINE TAKES THE DATA FROM ADDBR AND DISPLAYS
                ; IT FOR THE USER AS A 16 BIT OCTAL VALUE.
                ;
002154  016100 DISPLY: MOV     2(R1),R0        ; GET DATA
        000002
002160                 OCT16                    ; PRINT
002162  005711         TST     (R1)             ; ERROR BIT SET?
002164  100015         BPL     1$               ; NO - RETURN
002166  112700         MOVB    #'E,R0           ; PRINT 'E'
        000105
002172                 TTYOUT
002174  042711         BIC     #40000,(R1)      ; CLEAR ERROR BIT
        040000
002200  005237         INC     @#ERRCNT         ; INC  COUNT
        000522
002204  005737         TST     @#ERRCNT         ; OVERFLOW?
        000522
002210  001003         BNE     1$               ; NO - SKIP
002212  012737         MOV     #-1,@#ERRCNT     ; YES - FORCE VALUE
        177777
        000522
002220  000207 1$:     RETURN
                ;
                ;
                        .SBTTL  TEST 10: A/D CALIBRATION
                ;
                ; THIS TEST ACCEPTS A CHANNEL ADDRESS FROM THE USER
                ; AND DISPLAYS THE DATA FROM THAT CHANNEL CONTINUOUSLY
                ;
                ;
002222  TEST10: PRINTC  <A/D CALIBRATION>
002244  004767         CALL    GETCH            ; GET CHANNEL ADDRESS
        177476
002250                 KBEXIT                   ; SET UP KEYBOARD
002252  042702         BIC     #140703,R2       ; CLEAR SOME BITS
        140703
002256  032702         BIT     #60,R2           ; EXTERNAL?
        000060
002262  001002         BNE     1$               ; YES - NO START BIT
002264  052702         BIS     #1,R2            ; SET START BIT
        000001
002270  112704 1$:     MOVB    #10,R4           ; LINE COUNTER
        000010
002274                 CRLF
002276  010211 2$:     MOV     R2,(R1)          ; START CONVERSION
002300  105711 3$:     TSTB    (R1)             ; WAIT FOR DONE
002302  100376         BPL     3$
002304  004767         CALL    DISPLY           ; DISPLAY DATA
        177644
002310  105304         DECB    R4               ; LINE OVER?
002312  001766         BEQ     1$               ; YES - NEW LINE
002314                 TAB
002316  000767         BR      2$               ; NEXT CONVERSION
```

```
                        .SBTTL  TEST 11: A/D INPUT CHANNEL SCAN
                ;
                ; THIS TEST SCANS THE INPUT CHANNELS WHILE
                ; DISPLAYING THE A/D DATA ON THE TERMINAL.
                ;
                ;
002320          TEST11: PRINTC  <A/D INPUT CHANNEL SCAN>
002352                  KBEXIT                          ; SET UP KEYBOARD
002354  013701          MOV     @#BASE,R1               ; GET ADDRESS
        000542
002360  005761          TST     2(R1)                   ; CLEAR DONE
        000002
002364  005011          CLR     (R1)                    ; CLEAR CSR
002366  005002          CLR     R2                      ; INIT  CHANNEL COUNT
002370                  1$:     CRLF
002372  112703          MOVB    #10,R3                  ; LINE COUNTER
        000010
002376                  PRINT   <CH=>                   ; DISPLAY ADDRESS
002404  010200          MOV     R2,R0
002406                  OCT8
002410  010200          MOV     R2,R0                   ; GET CHANNEL ADDRESS
002412  000300          SWAB    R0                      ; PUT IN HIGH BYTE
002414  010011          MOV     R0,(R1)                 ; SET UP CHANNEL
002416  013700          MOV     @#DELAY,R0              ; WAIT TO SETTLE
        000546
002422  077001          2$:     SOB     R0,2$
002424  105211          3$:     INCB    (R1)            ; TRIGGER CONVERTER
002426  105711          4$:     TSTB    (R1)            ; WAIT FOR DONE
002430  100376                  BPL     4$
002432                          TAB
002434  004767          CALL    DISPLY                  ; DISPLAY DATA
        177514
002440  105303          DECB    R3                      ; LINE DONE?
002442  001370          BNE     3$                      ; NO - CONTINUE
002444  005202          INC     R2                      ; INC  CHANNEL
002446  123702          CMPB    @#SWR+1,R2              ; END OF RANGE?
        000541
002452  001346          BNE     1$                      ; NO - CONTINUE
002454  005002          CLR     R2                      ; YES
002456                  CRLF
002460  000743          BR      1$
```

```
                        .SBTTL  TEST 12: A/D INPUT GAIN/CHANNEL SCAN
                ;
                ; THIS TEST SCANS THE INPUT CHANNELS WHILE
                ; CHANGING THE GAIN OF THE CONVERTER.  THE
                ; A/D DATA IS DISPLAYED ON THE TERMINAL.
                ;
                ;
002462          TEST12: PRINTC  <A/D INPUT GAIN/CHANNEL SCAN>
002520                  KBEXIT                          ; SET UP KEYBOARD
002522  013701          MOV     @#BASE,R1               ; GET ADDRESS
        000542
002526  005761          TST     2(R1)                   ; CLEAR DONE
        000002
002532  005011          CLR     (R1)                    ; CLEAR CSR
002534  005002          CLR     R2                      ; INIT. CHANNEL COUNT
002536  005003          CLR     R3                      ; INIT. GAIN
002540          1$:     CRLF
002542  112704          MOVB    #7,R4                   ; LINE COUNTER
        000007
002546                  PRINT   <CH=>                   ; DISPLAY ADDRESS
002554  010200          MOV     R2,R0
002556                  OCT8
002560  112700          MOVB    #',,R0                  ; DISPLAY GAIN
        000054
002564                  TTYOUT
002566  112700          MOVB    #'0,R0
        000060
002572  032703          BIT     #10,R3                  ; GS1 SET?
        000010
002576  001401          BEQ     2$                      ; NO - SKIP
002600  105200          INCB    R0
002602          2$:     TTYOUT                          ; DISPLAY BIT
002604  112700          MOVB    #'0,R0
        000060
002610  032703          BIT     #4,R3                   ; GS0 SET?
        000004
002614  001401          BEQ     3$                      ; NO - SKIP
002616  105200          INCB    R0
002620          3$:     TTYOUT                          ; DISPLAY BIT
```

```
    1 002622  010200          MOV     R2,R0           ; GET CHANNEL ADDRESS
    2 002624  000300          SWAB    R0              ; PUT IN HIGH BYTE
    3 002626  050300          BIS     R3,R0           ; SET GAIN BITS
    4 002630  010011          MOV     R0,(R1)         ; SET UP CHANNEL
    5 002632  105211  4$:     INCB    (R1)            ; TRIGGER CONVERTER
    6 002634  105711  5$:     TSTB    (R1)            ; WAIT FOR DONE
    7 002636  100376          BPL     5$
    8 002640                  TAB
    9 002642  004767          CALL    DISPLY          ; DISPLAY DATA
              177306
   10 002646  105304          DECB    R4              ; LINE DONE?
   11 002650  001370          BNE     4$              ; NO - CONTINUE
   12 002652  005202          INC     R2              ; INC. CHANNEL
   13 002654  062703          ADD     #4,R3           ; INCREMENT GAIN
              000004
   14 002660  042703          BIC     #177763,R3      ; CLEAR EXTRA BITS
              177763
   15 002664  123702          CMPB    @#SWR+1,R2      ; END OF RANGE?
              000541
   16 002670  001323          BNE     1$              ; NO - CONTINUE
   17 002672  005002          CLR     R2              ; YES
   18 002674                  CRLF
   19 002676  000720          BR      1$
   20                 ;
```

```
 1
 2                              .SBTTL  DAC INITIALIZATION
 3                      ;
 4                      ; THIS ROUTINE PROVIDES INITIALIZATION FUNCTIONS
 5                      ; FOR SOME OF THE TESTS THAT EXERCISE THE DACS
 6                      ;
 7                      ;
 8 002700  012703  DAC:  MOV     #4000,R3        ; SET FOR TWO'S COMP
           004000
 9 002704  074505        XOR     R5,R5
10 002706  012704        MOV     #3777,R4
           003777
11 002712                TEST    BIT7,SWR        ; OFFSET BINARY?
12 002720  001005        BNE     1$              ; NO - SKIP
13 002722  010305        MOV     R3,R5           ; MODIFY ZERO
14 002724  042703        BIC     #4000,R3        ; MODIFY
           004000
15 002730  052704        BIS     #4000,R4
           004000
16 002734  013701  1$:   MOV     @#BASE,R1       ; GET BASE ADDRESS
           000542
17 002740  062701        ADD     #4,R1           ; FORM DAC A ADDRESS
           000004
18 002744  010102        MOV     R1,R2
19 002746  062702        ADD     #2,R2           ; FORM DAC B ADDRESS
           000002
20 002752  000207        RETURN
21                      ;
22                      ;
23                      ;       THIS ROUTINE ALLOWS TIME FOR DACS A AND B
24                      ;       TO SETTLE
25                      ;
26 002754          TIME: PUSH    R0              ; SAVE R0 FOR LATER
27 002756  012700        MOV     #20,R0          ; SET DELAY
           000020
28 002762  077001  1$:   SOB     R0,1$           ; WAIT
29 002764                POP     R0              ; RESTORE R0
30 002766  000207        RETURN
31                      ;
32                      ;
```

```
                        .SBTTL  TEST 13: A/D IN TO D/A OUT
                ;
                ; THIS TEST ALLOWS A USER TO CONNECT A SIGNAL SOURCE
                ; TO INPUT CHANNEL 0 AND SEE WHAT SHOULD BE THE
                ; SAME SIGNAL APPEARING ON THE A DAC OUTPUT
                ;
                ;
002770  004767  TEST13: CALL    DAC
        177704
                        PRINTC  <CONNECT SIGNAL SOURCE TO CHANNEL 0>
003042                  KBEXIT                  ; SET UP KEYBOARD
003044  013701          MOV     @#BASE,R1       ; GET ADDRESS
        000542
003050  005761          TST     2(R1)           ; CLEAR DONE
        000002
003054  005011          CLR     (R1)            ; START LOOP
003056  105211          INCB    (R1)
003060  105711  1$:     TSTB    (R1)            ; WAIT FOR DONE
003062  100376          BPL     1$
003064  016100          MOV     2(R1),R0        ; GET DATA
        000002
003070  105211          INCB    (R1)            ; START NEXT CONVERSION
003072  042700          BIC     #170000,R0      ; PREPARE A DAC DATA
        170000
003076  010061          MOV     R0,4(R1)        ; LOAD DAC DATA
        000004
003102  004767          CALL    TIME            ; WAIT FOR DAC TO SETTLE
        177646
003106  000764          BR      1$
```

```
                        .SBTTL  TEST 14: D/A RAMPS
                ;
                ; THIS TEST GENERATES RISING AND FALLING
                ; RAMPS ON THE DAC OUTPUTS.
                ;
                ;
003110  004767  TEST14: CALL    DAC             ; INIT. DACS
        177564
003114                  PRINTC  <D/A RAMPS>
003130                  KBEXIT                  ; SET UP KEYBOARD
003132  012705  1$:     MOV     #010000,R5      ; SET COUNTER
        010000
003136  010311  2$:     MOV     R3,(R1)         ; OUTPUT DAC A
003140  010412          MOV     R4,(R2)         ; OUTPUT DAC B
003142  005305          DEC     R5              ; DECREMENT COUNTER
003144  001403          BEQ     3$              ; START DOWN RAMP
003146  005304          DEC     R4              ; DECREMENT RAMP B
003150  005203          INC     R3              ; BUMP RAMP A
003152  000771          BR      2$              ; REPEAT
                ;
003154  012705  3$:     MOV     #010000,R5      ; INITIALIZE COUNTER
        010000
003160  010311  4$:     MOV     R3,(R1)         ; OUTPUT DAC A
003162  010412          MOV     R4,(R2)         ; OUTPUT DAC B
003164  005305          DEC     R5              ; DECREMENT COUNTER
003166  001761          BEQ     1$              ; START OVER AGAIN
003170  005303          DEC     R3              ; DECREMENT RAMP A
003172  005204          INC     R4              ; BUMP RAMP B
003174  000771          BR      4$              ; REPEAT
                ;
```

```
                                .SBTTL  TEST 15: D/A CALIBRATION
                        ;
                        ; THIS TEST STEPS BETWEEN POSITIVE FULL SCALE
                        ; NEGATIVE FULL SCALE AND ZERO OUTPUTS ON THE
                        ; TWO DAC CHANNELS TO ALLOW THE USER TO
                        ; CALIBRATE THE DACS.
                        ;
                        ;
003176  004767  TEST15: CALL    DAC                     ; INIT. DACS
        177476
003202                  PRINTC  <D/A CALIBRATION>
003224  010312  1$:     MOV     R3,(R2)                 ; -FS. B
003226  010311          MOV     R3,(R1)                 ; -FS. A
003230                  TTYIN
003232  010412          MOV     R4,(R2)                 ; +FS. B
003234  010411          MOV     R4,(R1)                 ; +FS. A
003236                  TTYIN
003240  010512          MOV     R5,(R2)                 ; ZERO. B
003242  010511          MOV     R5,(R1)                 ; ZERO. A
003244                  TTYIN
003246  000766          BR      1$                      ; REPEAT
                        ;
                        ;
                        ;
                        ;
                        ;
                                .SBTTL  TEST 16: D/A SQUARE WAVES
                        ;
                        ; THIS TEST OUTPUTS HIGH SPEED FULL SCALE
                        ; SQUARE WAVES TO BOTH DACS.
                        ;
                        ;
003250  004767  TEST16: CALL    DAC                     ; INIT. DACS
        177424
003254                  PRINTC  <D/A SQUARE WAVES>
003300                  KBEXIT                          ; SET UP KEYBOARD
003302  010311  1$:     MOV     R3,(R1)                 ; OUTPUT TO DACS
003304  010312          MOV     R3,(R2)
003306  004767          CALL    TIME                    ; WAIT TO SETTLE
        177442
003312  000400          BR      2$                      ; FOR TIMING PURPOSES
003314  010411  2$:     MOV     R4,(R1)                 ; OUTPUT FULL SCALE
003316  010412          MOV     R4,(R2)                 ; CHANGE
003320  004767          CALL    TIME                    ; WAIT TO SETTLE
        177430
003324  000766          BR      1$                      ; REPEAT
```

```
 1
 2                              .SBTTL  TEST 17: D/A OUT TO A/D IN
 3                      ;
 4                      ; THIS TEST OUTPUTS A RAMP ON THE A DAC WHILE
 5                      ; DISPLAYING A/D INPUT DATA FROM CHANNEL 0.  IF THE
 6                      ; A DAC IS CONNECTED TO THE CHANNEL 0 INPUT, THE
 7                      ; USER CAN VERIFY THAT THE ANALOG SUBSYSTEMS ARE
 8                      ; FUNCTIONING (ALTHOUGH NOT CALIBRATED).
 9                      ;
10                      ;
11 003326  004767  TEST17: CALL    DAC                  ; INIT. DACS
           177346
12 003332                  PRINTC  <CONNECT THE A DAC TO CHANNEL 0>
13 003374                  KBEXIT                       ; SET UP KEYBOARD
14 003376  013701          MOV     @#BASE,R1            ; GET BASE ADDRESS
           000542
15 003402  005761          TST     2(R1)                ; CLEAR DONE
           000002
16 003406  005011          CLR     (R1)                 ; CLEAR CSR
17 003410          1$:     CRLF
18 003412  112705          MOVB    #10,R5               ; LINE COUNTER
           000010
19 003416  105211  2$:     INCB    (R1)                 ; TRIGGER CONVERTER
20 003420  105711  3$:     TSTB    (R1)                 ; WAIT FOR DONE
21 003422  100376          BPL     3$
22 003424  010361          MOV     R3,4(R1)             ; SET UP NEXT STATE
           000004
23 003430  004767          CALL    TIME                 ; WAIT FOR DAC TO SETTLE
           177320
24 003434  016100          MOV     2(R1),R0             ; GET A/D DATA
           000002
25 003440                  OCT16                        ; DISPLAY
26 003442  005203          INC     R3                   ; NEXT DAC STATE
27 003444  042703          BIC     #70000,R3            ; 12 BITS ONLY
           070000
28 003450  105305          DECB    R5                   ; LINE OVER?
29 003452  001756          BEQ     1$                   ; YES - NEXT LINE
30 003454                  TAB                          ; NEXT DATA
31 003456  000757          BR      2$
32                      ;
33                      ;
34         000001          .END
```

```
T2781  TST-11 MODULE   MACRO V03.0B    28-DEC-79 08:43:24 PAGE 27-1
SYMBOL TABLE

PASE  = 000542          ERRNUM= 000521          TEST11  002320R     002
BIT0  = 000001          FF    = 000014          TEST12  002462R     002
BIT1  = 000002          GETCH   001746R     002 TEST13  002770R     002
BIT10 = 002000          HLTERR= 000004          TEST14  003110R     002
BIT11 = 004000          INHERR= 000100          TEST15  003176R     002
BIT12 = 010000          INIT    000112R     002 TEST16  003250R     002
BIT13 = 020000          INIT81  000100R     002 TEST17  003326R     002
BIT14 = 040000          I2781 = 000100RG    002 TEST2   001024R     002
BIT15 = 100000          I2785 = 000100RG    002 TEST3   001206R     002
BIT2  = 000004          LF    = 000012          TEST4   001262R     002
BIT3  = 000010          LPERR = 000002          TEST5   001370R     002
BIT4  = 000020          LPTST = 000001          TEST6   001576R     002
BIT5  = 000040          NEWFLG= 010000          TEST7   001744R     002
BIT6  = 000100          NORPLY  000512R     002 TIME    002754R     002
BIT7  = 000200          ODTACC= 000514          TPB     000000R     002
BIT8  = 000400          PARAM   000422R     002 TSTALL= 000010
BIT9  = 001000          PR7   = 000340          TSTCSR= 000500
CHNL    000405R     002 QUERY   000220R     002 TSTNUM= 000520
CR    = 000015          RBUF  = 177562          TSTONE= 000040
CTRLC = 000003          RCSR  = 177560          TSTSEQ= 000020
CTRLI = 000011          REG     000566R     002 T2781 = 000000RG    002
DAC     002700R     002 SPACE = 000040          T2785 = 000000RG    002
DACTYP  000365R     002 SPEED   000342R     002 VECTOR= 000544
DELAY = 000546          SWR   = 000540          XBUF  = 177566
DISPLY  002154R     002 TEST1   000726R     002 XCSR  = 177564
ERRCNT= 000522          TEST10  002222R     002

  ABS.  000000    000
        000000    001
T2781   003460    002
ERRORS DETECTED:  0

VIRTUAL MEMORY USED:  2116 WORDS  ( 9 PAGES)
DYNAMIC MEMORY AVAILABLE FOR  65 PAGES
>DX1:2781,=DX1:TST11.ML/M,DX1:2781.V01
```

APPENDIX B

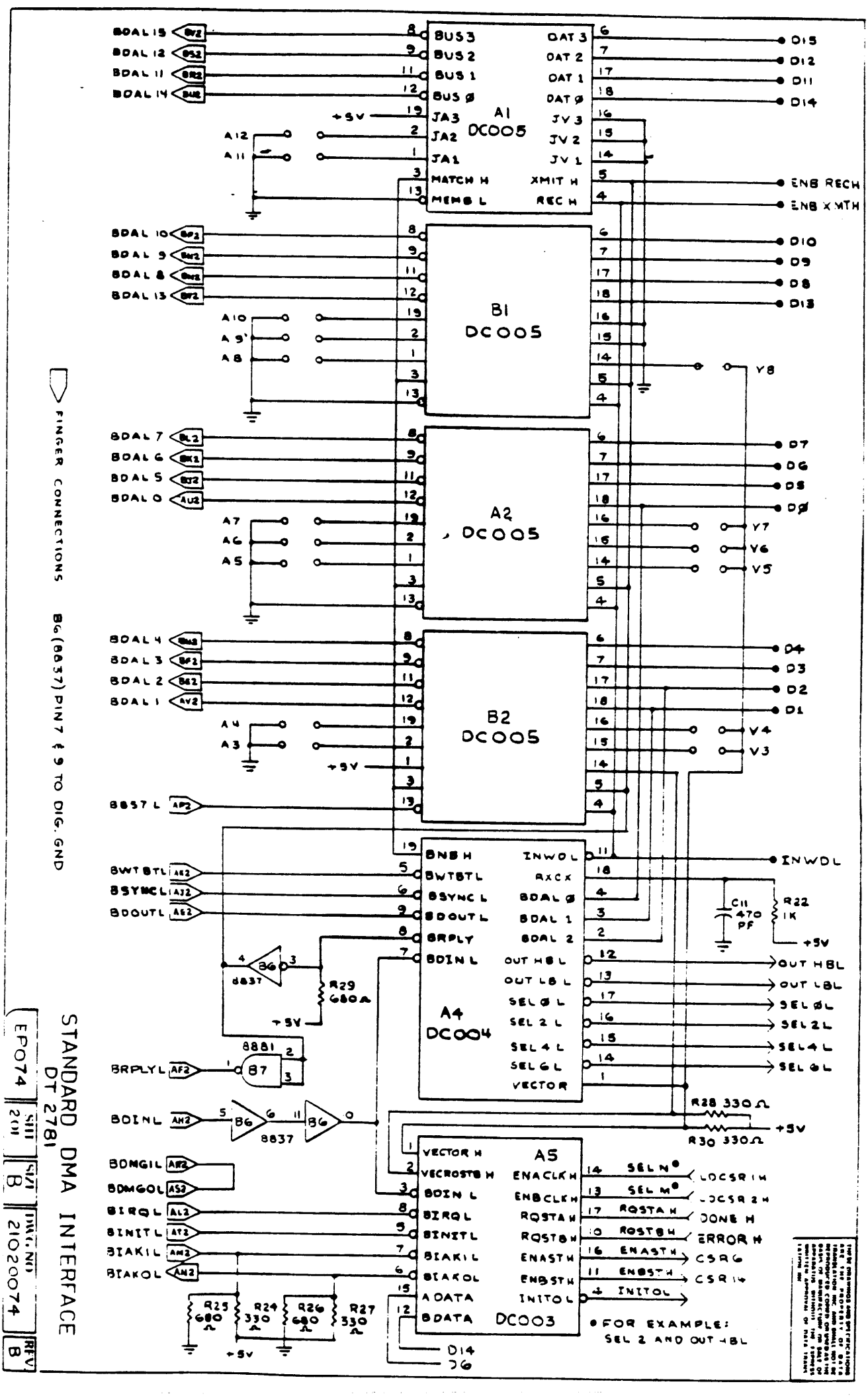
CIRCUIT SCHEMATICS

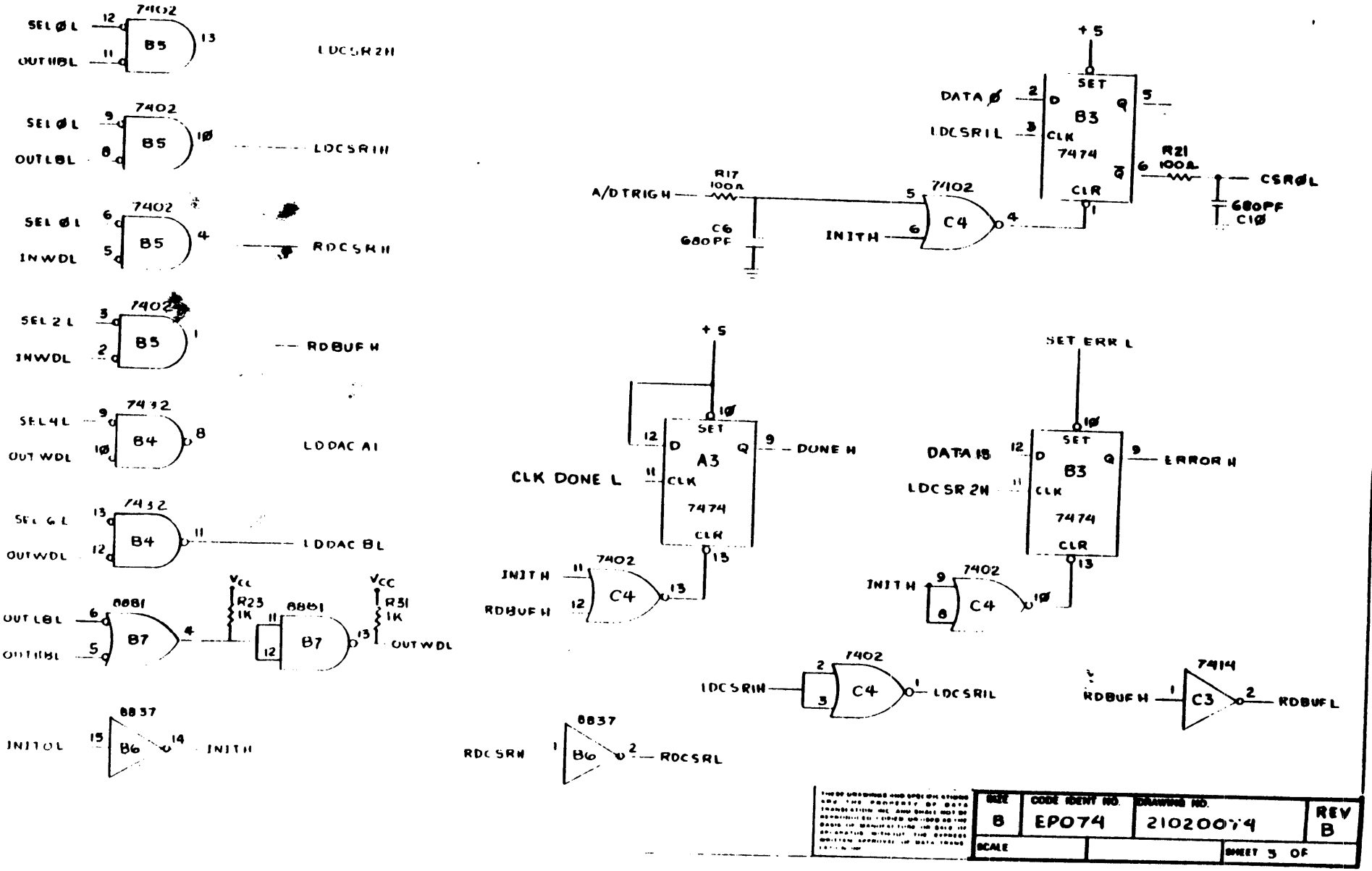
REVISION	ECO NO.	DATE	DWN	ENG
B	184	8-6-79	K.T.C.	K.E.D.

DATA TRANSLATION INC

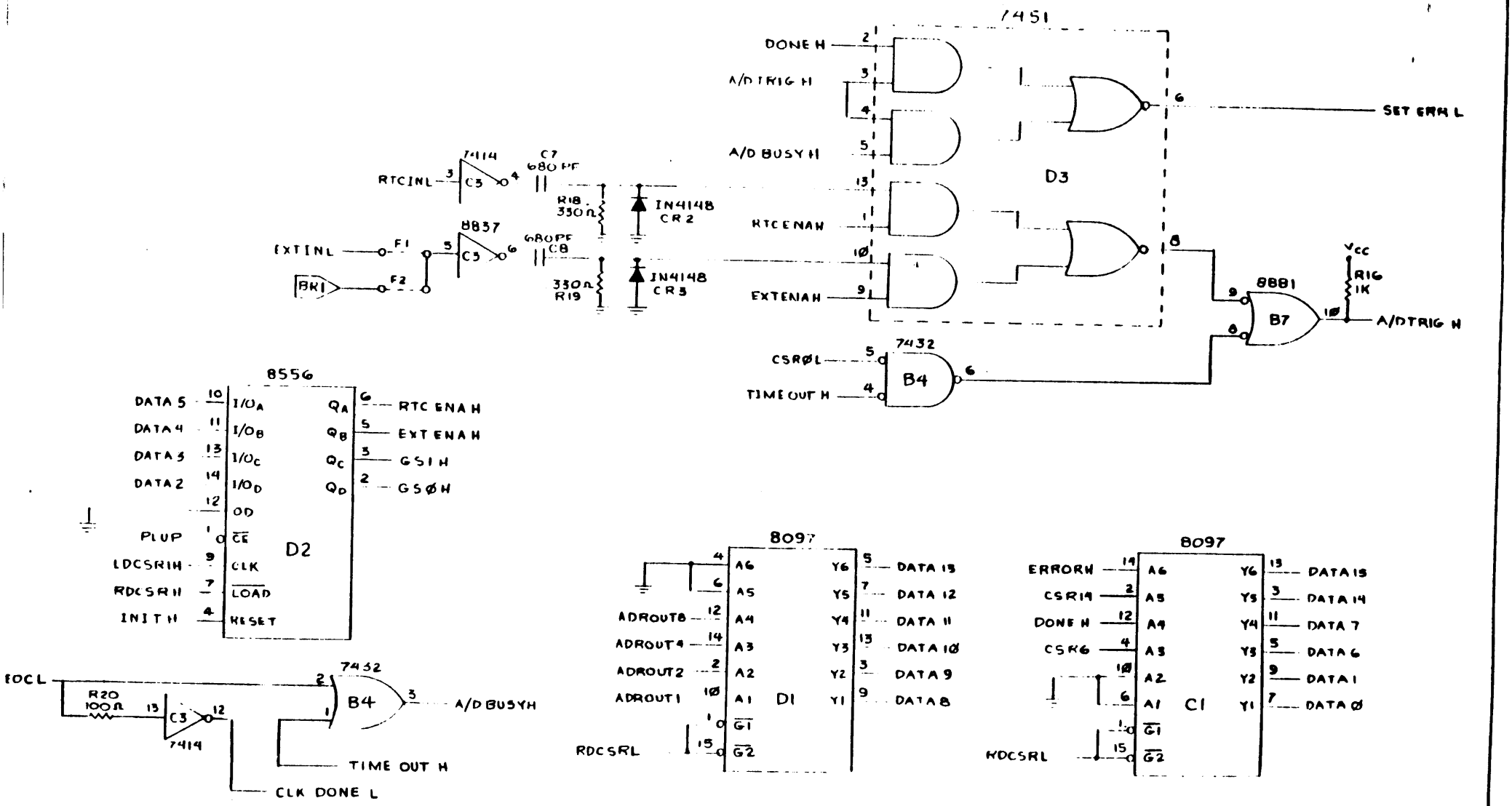
DRAWN: K.T.C.	DATE: 6-19-79	TITLE: SCHEMATIC DT 2781
CHECKED: K.E.D.	DATE: 6-19-79	
ENG:	DATE: 7-10-79	

EP074	SHT. 1 OF 9	SIZE: B	DWG.NO. 21020074	REV. B


STANDARD DMA INTERFACE
DT 2781
EPO74
SIZE B
DWG. NO. 21020074
REV B
FINGER CONNECTIONS
B6 (8837) PIN 7 & 9 TO DIG. GND
A1 DC005
A2 DC005
B1 DC005
B2 DC005
A4 DC004
A5
B3 DC003
BUS3
BUS2
BUS1
BUS0
JA3
JA2
JA1
MATCH H
MEMB L
DAT 3
DAT 2
DAT 1
DAT 0
JV 3
JV 2
JV 1
XMIT H
REC H
+5V
BDAL 15
BDAL 12
BDAL 11
BDAL 14
BDAL 10
BDAL 9
BDAL 8
BDAL 13
BDAL 7
BDAL 6
BDAL 5
BDAL 0
BDAL 4
BDAL 3
BDAL 2
BDAL 1
BBS7 L
BWTBTL
BSYNCL
BDOUTL
BRPLYL
BDINL
BDMGIL
BDMGOL
BIRQL
BINITL
BIAKIL
BIAKOL
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
D15
D12
D11
D14
ENB RECH
ENB XMTH
D10
D9
D8
D13
V8
D7
D6
D5
D0
V7
V6
V5
D4
D3
D2
D1
V4
V3
INWDL
OUT HBL
OUT LBL
SEL 0 L
SEL 2 L
SEL 4 L
SEL 6 L
BNBH
BWTBTL
BSYNC L
BDOUT L
BRPLY
BDIN L
INWD L
RXCX
BDAL 0
BDAL 1
BDAL 2
OUT HB L
OUT LB L
SEL 0 L
SEL 2 L
SEL 4 L
SEL 6 L
VECTOR
C11 470 PF
R22 1K
R28 330Ω
R30 330Ω
R29 680Ω
R25 680Ω
R24 330Ω
R26 680Ω
R27 330Ω
8837
8881
B6
B7
VECTOR H
VECROSTB H
BDIN L
BIRQL
BINITL
BIAKIL
BIAKOL
ADATA
BDATA
ENACLK H
ENBCLK H
RQSTA H
RQSTB H
ENASTH
ENBSTH
INITOL
SEL N*
SEL M*
LOCSR1 H
LOCSR2 H
DONE H
ERROR H
CSR6
CSR14
INITOL
* FOR EXAMPLE:
SEL 2 AND OUT HBL
D14
D6

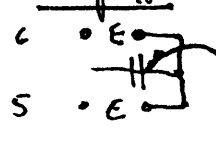


SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	2102007-4	B
SCALE		SHEET 3 OF	



SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	B
SCALE		SHEET 4 OF	

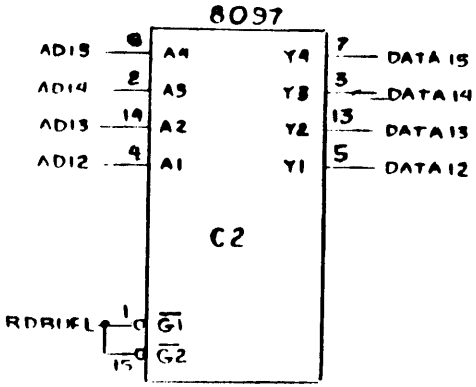
Unipolar: cut 4D

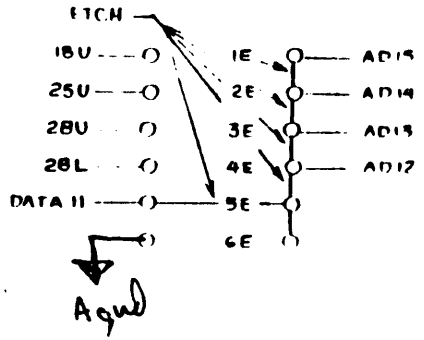


cut 5D

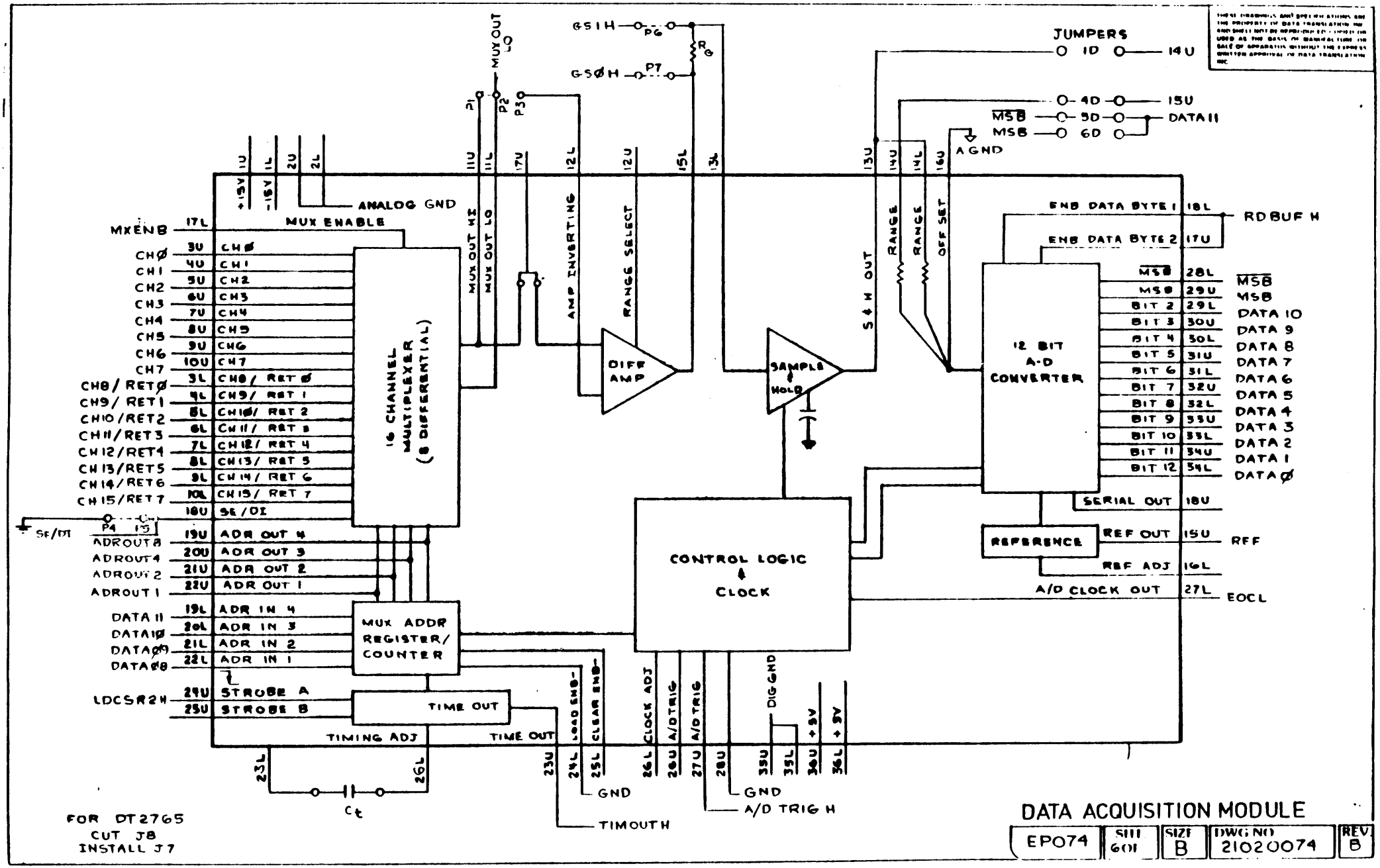
and cut here at 5E

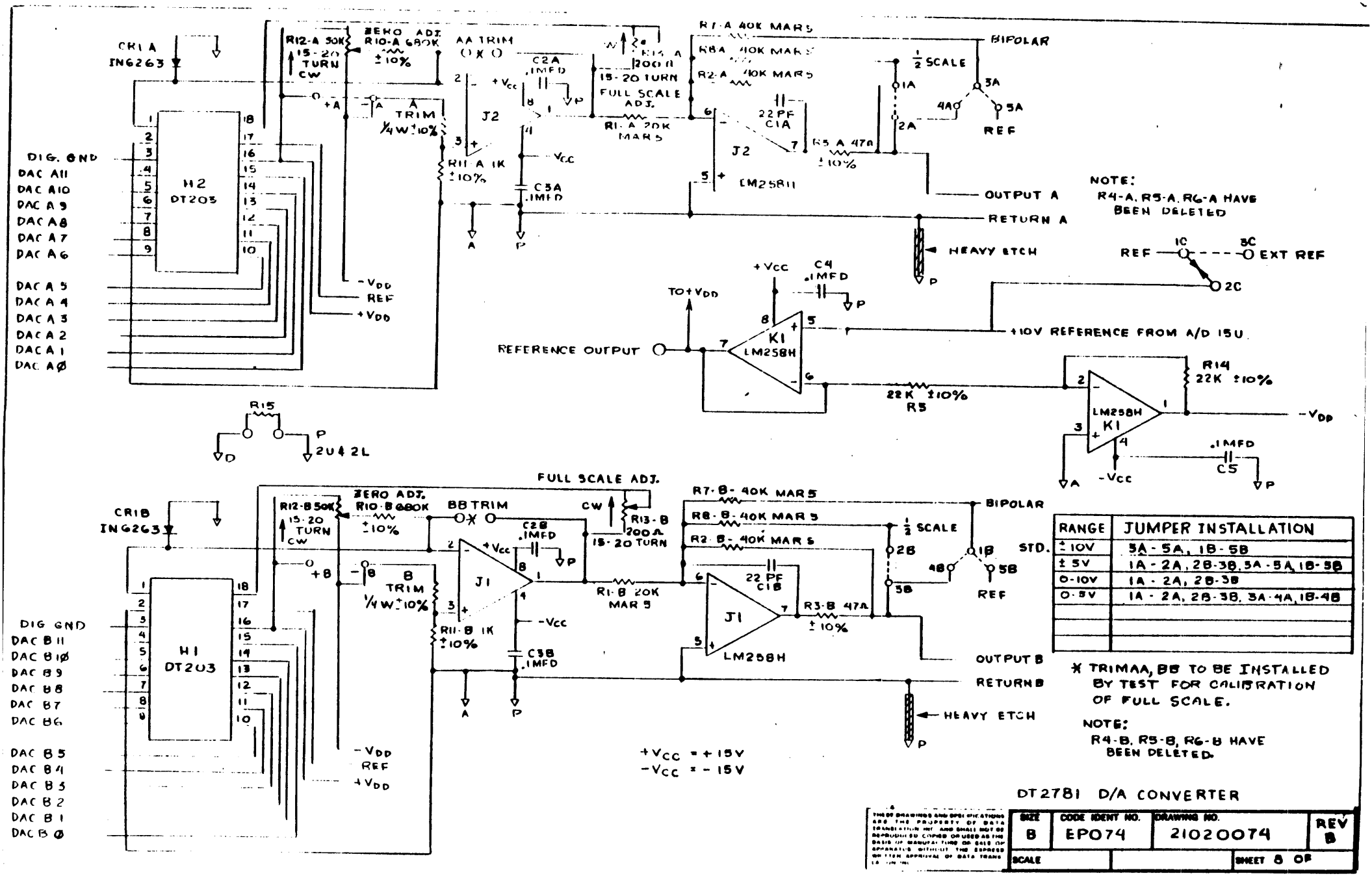
Jumper 1D, 6D + 6E





	SIZE B	CODE IDENT NO EP074	DRAWING NO 21020074	REV B
	SCALE		SHEET 1 OF	

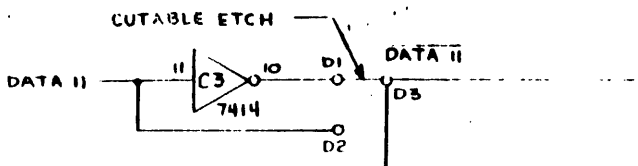

JUMPERS
1D
14U
4D
15U
MSB
5D
DATA 11
MSB
6D
AGND
GS1H
GSØH
MUXOUT LO
R_G
P1
P2
P3
P6
P7
+15V
-15V
ANALOG GND
MUX ENABLE
MUX OUT HI
MUX OUT LO
AMP INVERTING
RANGE SELECT
S & H OUT
RANGE
RANGE
OFF SET
MXENB
CHØ
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8/ RETØ
CH9/ RET 1
CH10/RET2
CH11/RET3
CH12/RET4
CH13/RET5
CH14/RET6
CH15/RET7
SE/DI
16 CHANNEL MULTIPLEXER (8 DIFFERENTIAL)
DIFF AMP
SAMPLE & HOLD
12 BIT A-D CONVERTER
ENB DATA BYTE 1
ENB DATA BYTE 2
RDBUF H
MSB
MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
DATA 10
DATA 9
DATA 8
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA Ø
SERIAL OUT
REFERENCE
REF OUT
REF
REF ADJ
A/D CLOCK OUT
EOCL
CONTROL LOGIC
CLOCK
ADROUT4
ADROUT3
ADROUT2
ADROUT1
ADR OUT 4
ADR OUT 3
ADR OUT 2
ADR OUT 1
DATA 11
DATA10
DATA9
DATA8
ADR IN 4
ADR IN 3
ADR IN 2
ADR IN 1
MUX ADDR REGISTER/ COUNTER
LDCSR2H
STROBE A
STROBE B
TIME OUT
TIMING ADJ
TIME OUT
LOAD ENB
CLEAR ENB
CLOCK ADJ
A/D TRIG
A/D TRIG
DIG GND
+5V
+5V
GND
GND
A/D TRIG H
TIMOUT H
Ct
FOR DT2765
CUT J8
INSTALL J7
DATA ACQUISITION MODULE
EP074
SHT 001
SIZE B
DWG NO 21020074
REV B

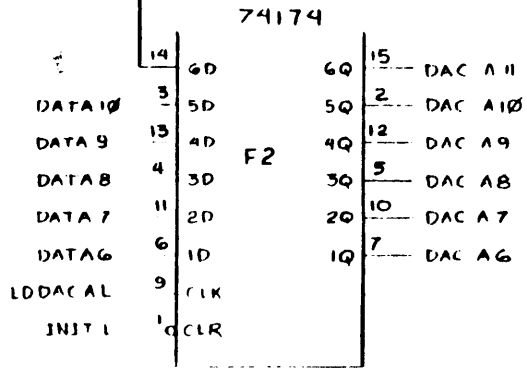


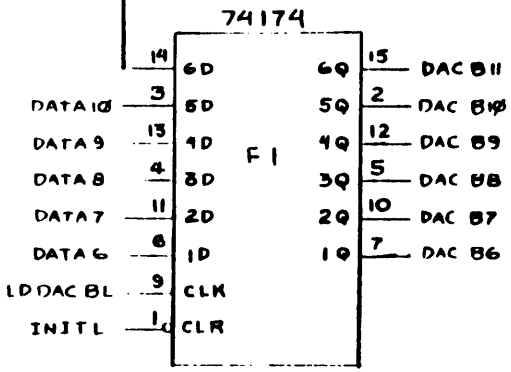
RANGE	JUMPER INSTALLATION
±10V	5A - 5A, 1B - 5B
±5V	1A - 2A, 2B - 3B, 3A - 5A, 1B - 5B
0-10V	1A - 2A, 2B - 3B
0-5V	1A - 2A, 2B - 3B, 3A - 4A, 1B - 4B

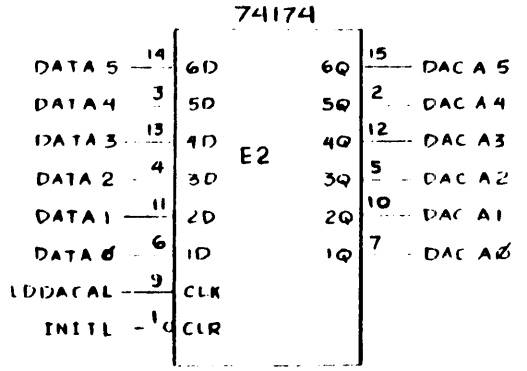
DT2781 D/A CONVERTER

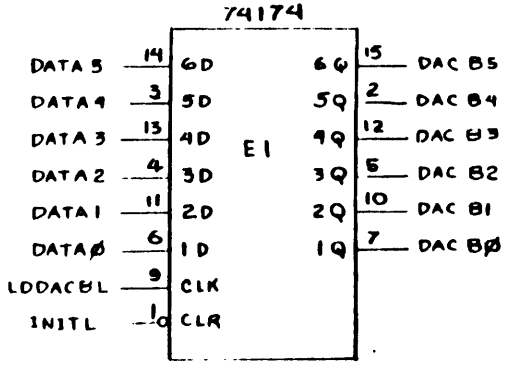
SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	B
SCALE			SHEET 8 OF



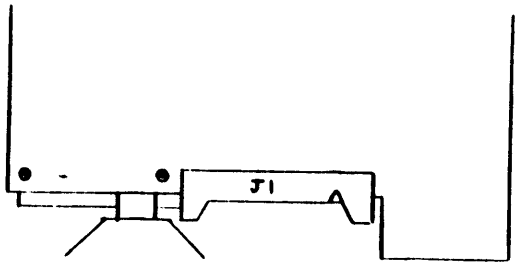






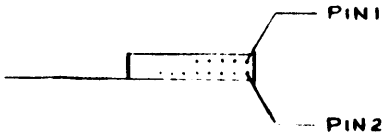


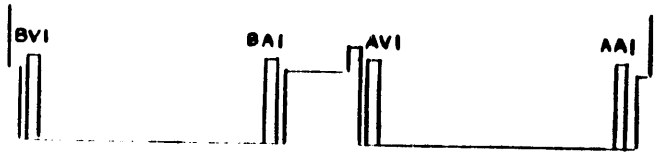
SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	B
SCALE		SHEET 7 OF	



J1 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CH Ø	2	CH 8 / RET Ø
3	CH 1	4	CH 9 / RET 1
5	CH 2	6	CH 10 / RET 2
7	CH 3	8	CH 11 / RET 3
9	CH 4	10	CH 12 / RET 4
11	CH 5	12	CH 13 / RET 5
13	CH 6	14	CH 14 / RET 6
15	CH 7	16	CH 15 / RET 7
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND
21	RTCINL	22	D GND
23	DAC B RET	24	DAC B OUT
25	DAC A RET	26	DAC A OUT

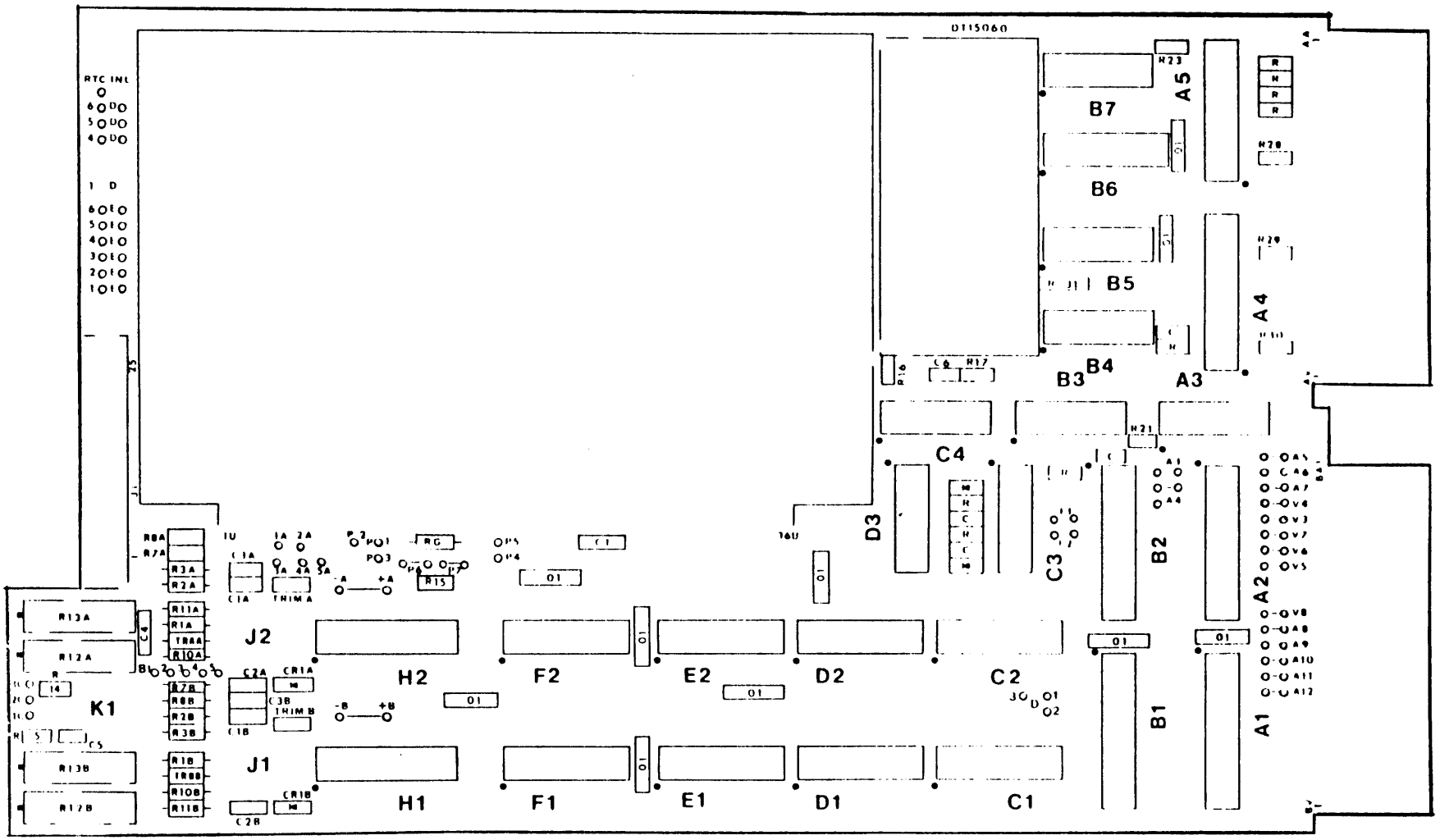
RTCINL ON WIRE POST





BOTTOM EDGE CONNECTOR							
COMPONENT SIDE		SOLDER SIDE		COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
BA1		BA2	+ 5V	AA1		AA2	+ 5V
BB1		BB2		AB1		AB2	
BC1		BC2	D GND	AC1		AC2	D GND
BD1		BD2		AD1		AD2	
BE1		BE2	BDAL 2L	AE1		AE2	BD OUT L
BF1		BF2	BDAL 3L	AF1		AF2	BRPLY L
BH1		BH2	BDAL 4L	AH1		AH2	BDIN L
BJ1	D GND	BJ2	BDAL 5L	AJ1	D GND	AJ2	BSYNC L
BK1		BK2	BDAL 6L	AK1		AK2	BWT BTL
BL1		BL2	BDAL 7L	AL1		AL2	BIRQ L
BM1	D GND	BM2	BDAL 8L	AM1	D GND	AM2	BIAK IL
BN1		BN2	BDAL 9L	AN1		AN2	BIAK OL
BP1		BP2	BDAL 10L	AP1		AP2	BBS 7L
BR1		BR2	BDAL 11L	AR1		AR2	BDMG IL
BS1		BS2	BDAL 12L	AS1		AS2	BDMG OL
BT1	D GND	BT2	BDAL 13L	AT1	D GND	AT2	BINIT L
BU1		BU2	BDAL 14L	AU1		AU2	BDAL OL
BV1	+ 5V	BV2	BDAL 15L	AV1		AV2	BDAL IL

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	B
SCALE		SHEET 9 OF 9	



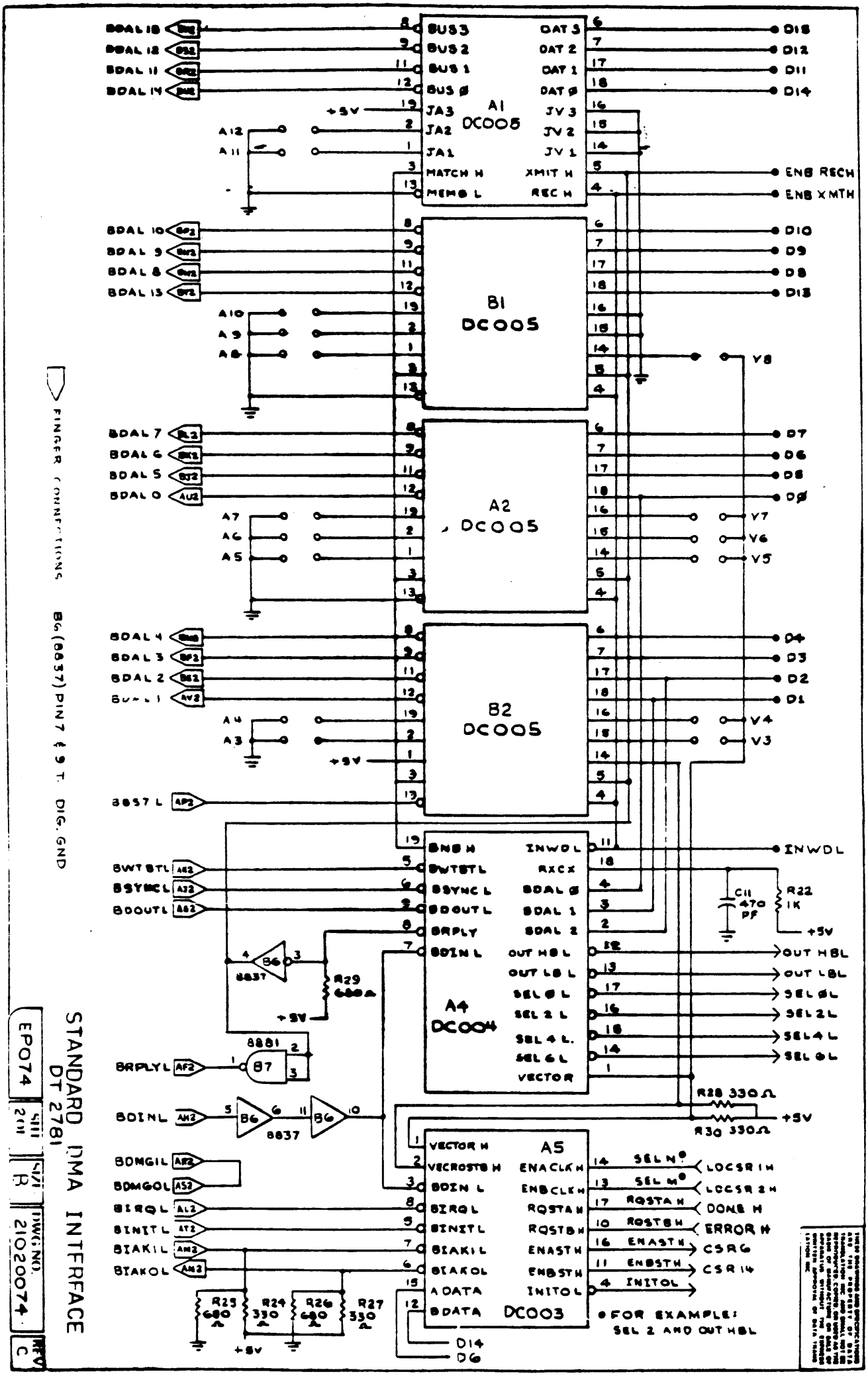
COMPONENT DESIGNATIONS

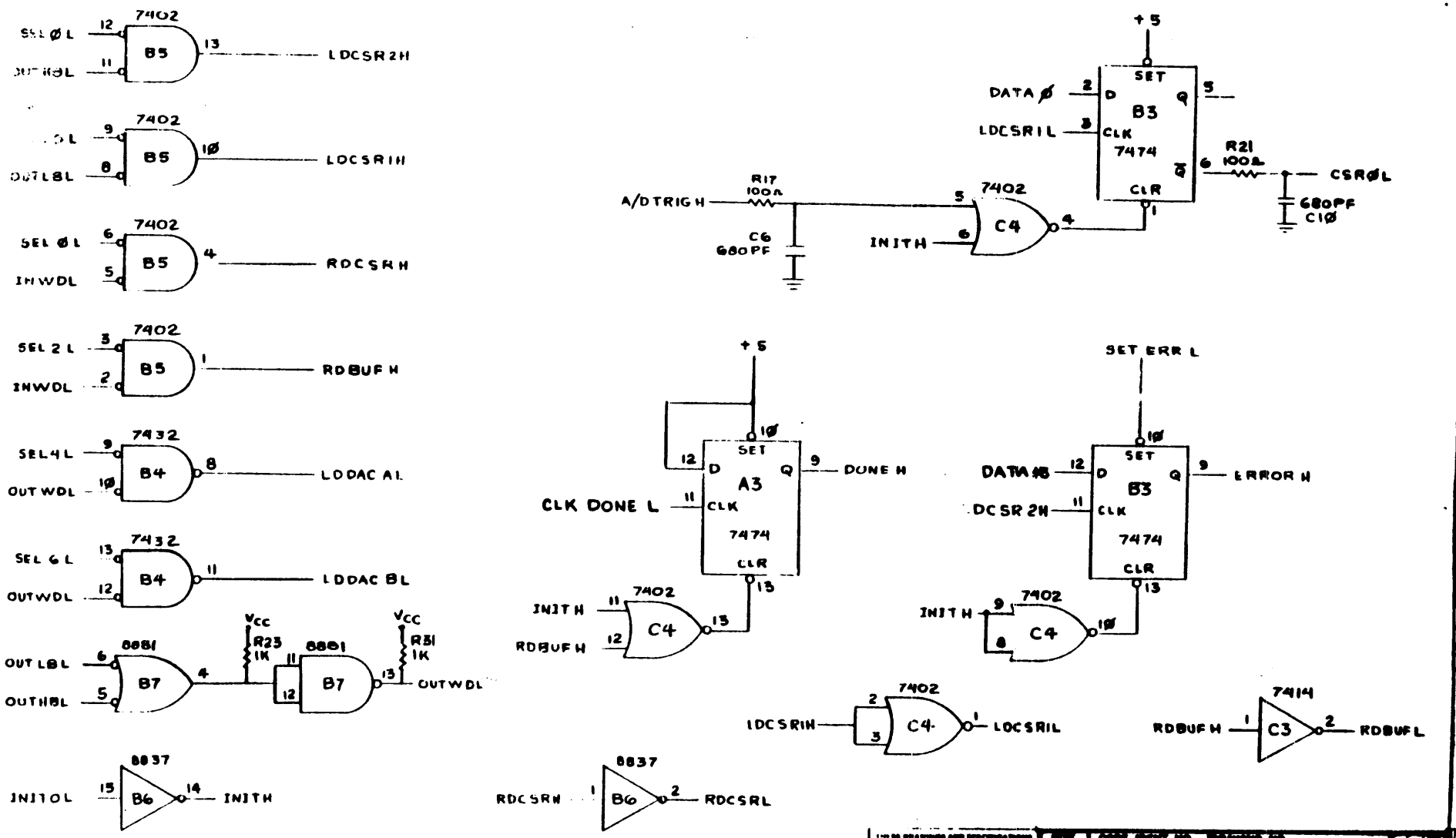
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
A	EP074	11070074	B
SCALE			SHEET 1 OF 1

REVISION	ECO NO.	DATE	DWN	ENG
C	203	10-16-79	K.T.C.	K.E.D.
B	184	8-6-79	K.T.C.	K.E.D.

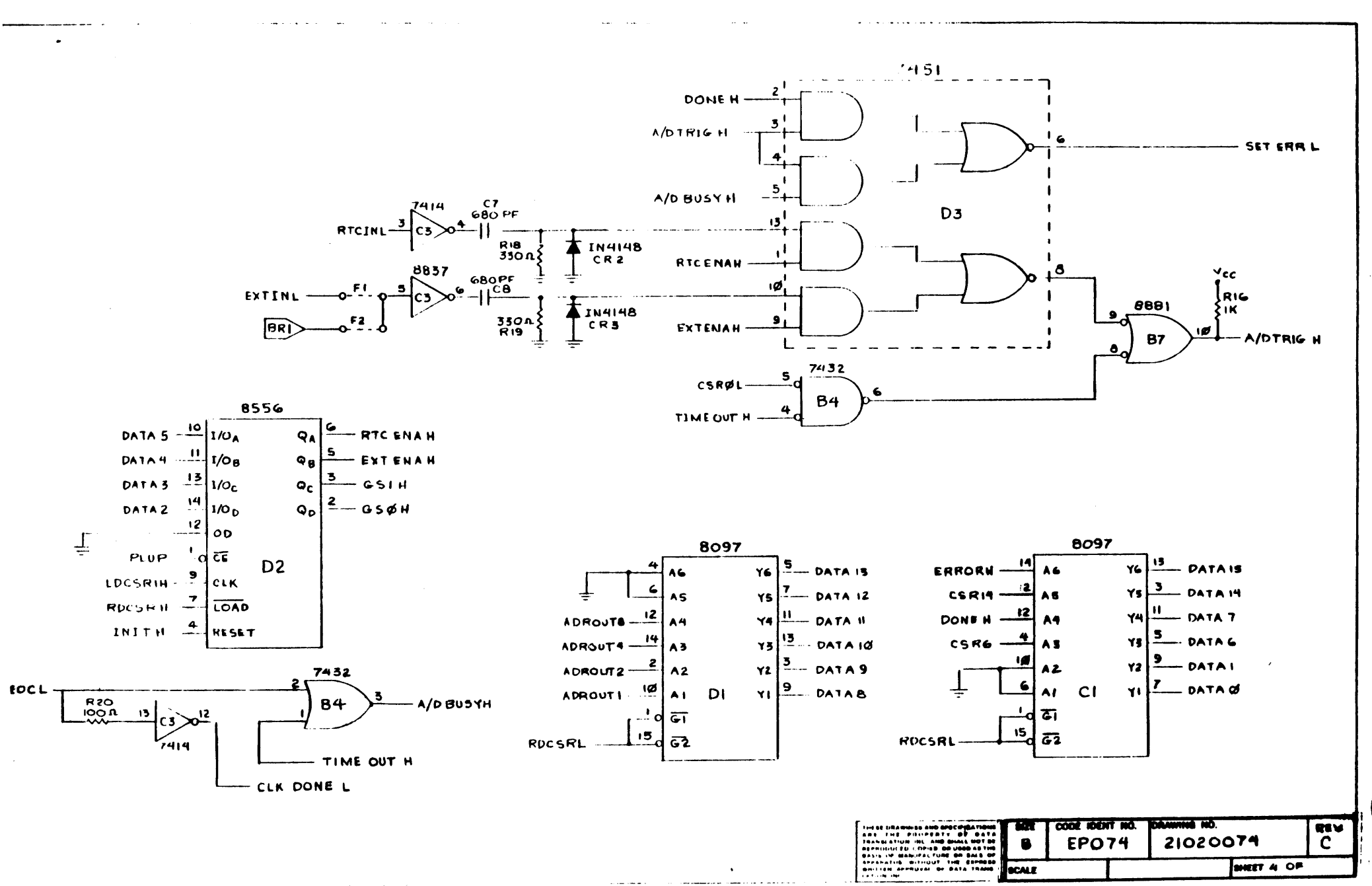
DATA TRANSLATION INC

DRAWN: K.T.C.	DATE: 6-19-79	TITLE: SCHEMATIC DT 2781
CHECKED: K.E.D.	DATE: 6-19-79	
ENG:	DATE: 9-10-79	
EP074	SHT. 1 OF 9	SIZE B
DWG.NO. 21020074	REV. C	

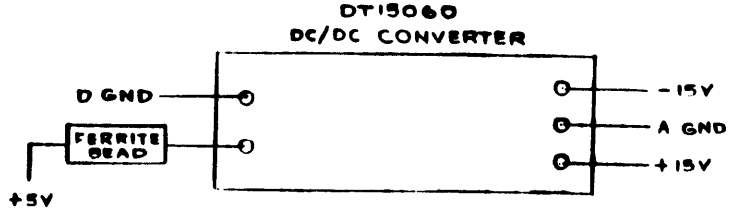

STANDARD DMA INTERFACE
DT 2781
EP074
SIZE B
DWG NO. 2102074
REV C
FINGER CONNECTIONS B6 (8837) PIN 7 & 9 TO DIG. GND
A1 DC005
B1 DC005
A2 DC005
B2 DC005
A4 DC004
A5
DC003
B6 8837
B7 8881
BDAL 15
BDAL 12
BDAL 11
BDAL 14
BDAL 10
BDAL 9
BDAL 8
BDAL 13
BDAL 7
BDAL 6
BDAL 5
BDAL 0
BDAL 4
BDAL 3
BDAL 2
BDAL 1
BBS7 L
BWTBTL
BSYNCL
BDOUTL
BRPLYL
BDINL
BDMGIL
BDMGOL
BIRQL
BINITL
BIAKIL
BIAKOL
+5V
R29 680Ω
R28 330Ω
R30 330Ω
R23 680Ω
R24 330Ω
R26 680Ω
R27 330Ω
C11 470 pf
R22 1K
D15
D12
D11
D14
D10
D9
D8
D13
D7
D6
D5
D0
D4
D3
D2
D1
V8
V7
V6
V5
V4
V3
INWDL
OUT HBL
OUT LBL
SEL 0 L
SEL 2 L
SEL 4 L
SEL 6 L
ENB RECH
ENB XMTH
LOCSR 1 H
LOCSR 2 H
DONE H
ERROR H
CSR 6
CSR 14
* FOR EXAMPLE: SEL 2 AND OUT HBL

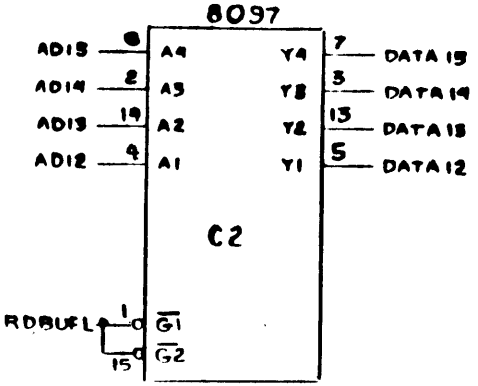


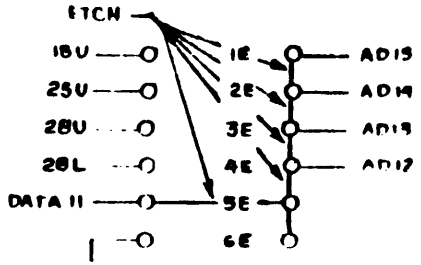
SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	C
SCALE			SHEET 3 OF



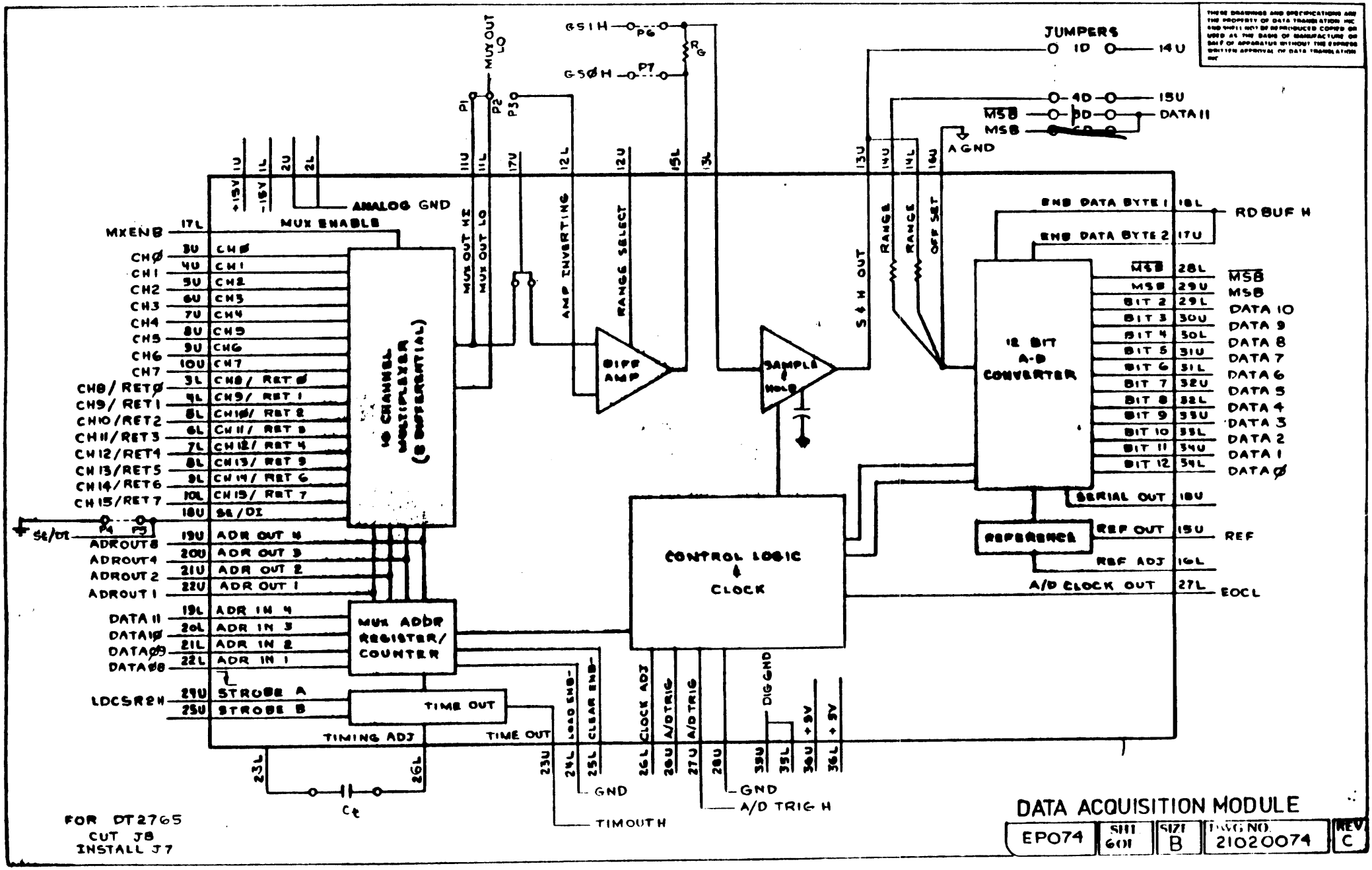
SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	C
SCALE		SHEET 4 OF	

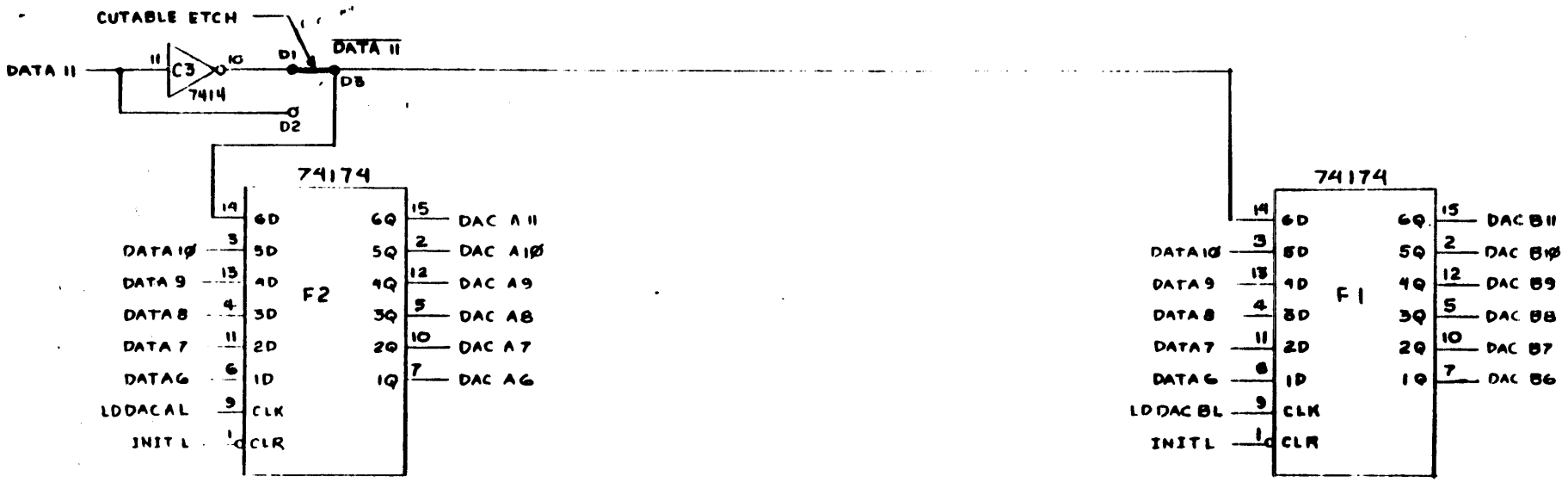




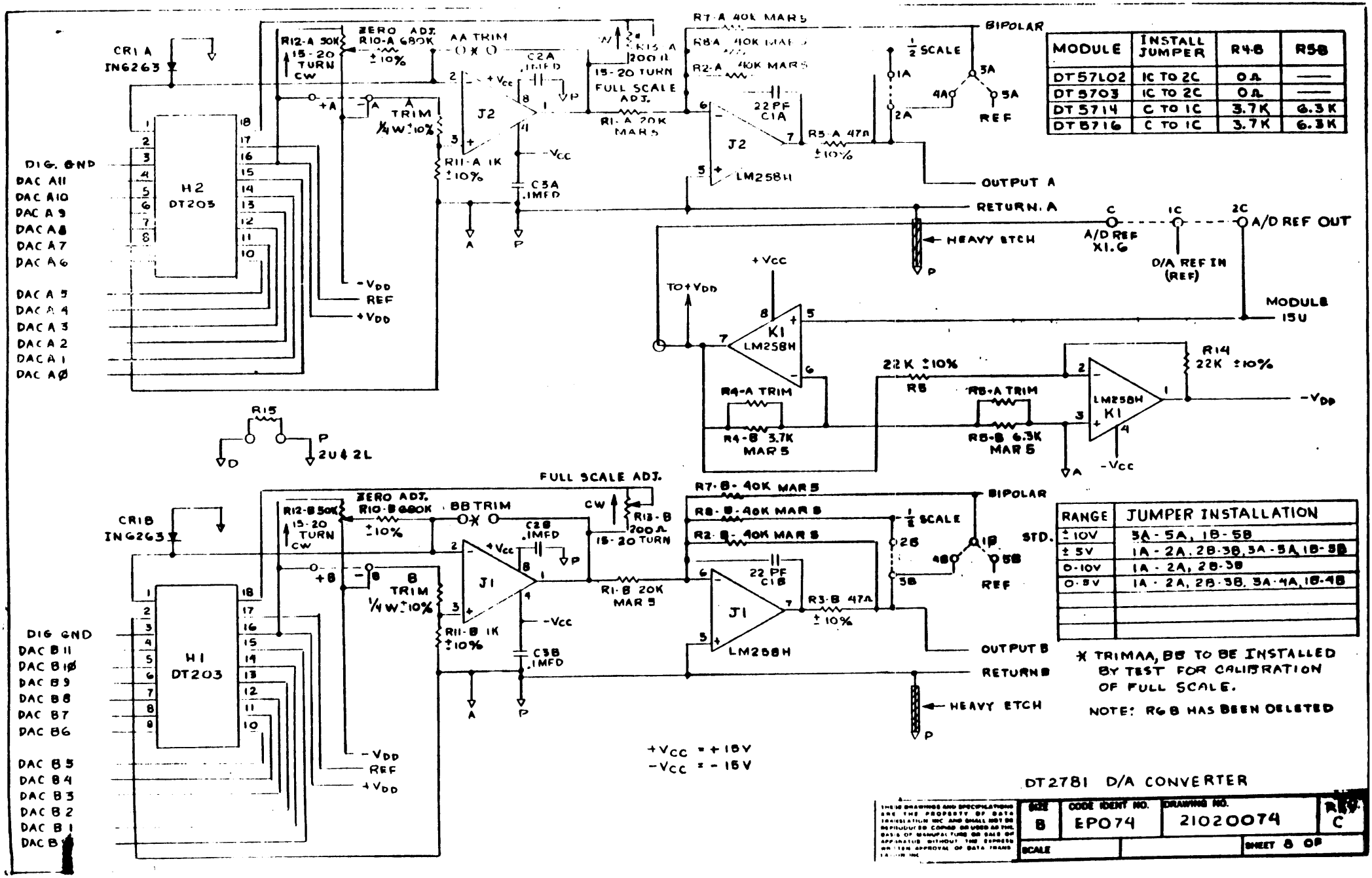


SIZE	CODE IDENT NO	DRAWING NO	REV
B	EP074	21020074	C
SCALE		SHEET 5 OF	


JUMPERS
1D
14U
4D
15U
MSB
3D
DATA 11
MSB
AGND
ANALOG GND
MUX ENABLE
MXENB
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8/RET0
CH9/RET1
CH10/RET2
CH11/RET3
CH12/RET4
CH13/RET5
CH14/RET6
CH15/RET7
SE/DI
16 CHANNEL MULTIPLEXER (8 DIFFERENTIAL)
MUX OUT HI
MUX OUT LO
AMP INVERTING
RANGE SELECT
DIFF AMP
SAMPLE HOLD
S & H OUT
RANGE
RANGE
OFF SET
12 BIT A-D CONVERTER
ENB DATA BYTE 1
ENB DATA BYTE 2
RDBUF H
MSB
MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
DATA 10
DATA 9
DATA 8
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA 0
SERIAL OUT
REFERENCE
REF OUT
REF
REF ADJ
A/D CLOCK OUT
EOCL
CONTROL LOGIC
CLOCK
ADROUT8
ADROUT4
ADROUT2
ADROUT1
DATA 11
DATA 10
DATA 09
DATA 08
MUX ADDR REGISTER/ COUNTER
LDCSR2H
STROBE A
STROBE B
TIME OUT
TIMING ADJ
TIME OUT
LOAD ENB-
CLEAR ENB-
CLOCK ADJ
A/D TRIG
A/D TRIG
DIG GND
+5V
+5V
GND
GND
A/D TRIG H
TIMOUT H
Ct
FOR DT2765
CUT J8
INSTALL J7
DATA ACQUISITION MODULE
EP074
SHT 001
SIZE B
DWG NO. 21020074
REV C



SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	C
SCALE			SHEET 7 OF



MODULE	INSTALL JUMPER	R4-B	R5B
DT57L02	IC TO 2C	0Ω	——
DT5703	IC TO 2C	0Ω	——
DT5714	C TO 1C	3.7K	6.3K
DT5716	C TO 1C	3.7K	6.3K

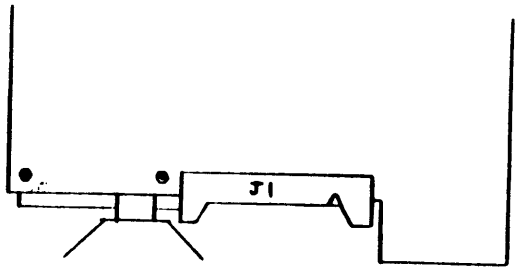
RANGE	JUMPER INSTALLATION
±10V	5A - 5A, 1B - 5B
±5V	1A - 2A, 2B - 3B, 3A - 5A, 1B - 5B
0-10V	1A - 2A, 2B - 3B
0-5V	1A - 2A, 2B - 3B, 5A - 4A, 1B - 4B

* TRIMAA, BB TO BE INSTALLED BY TEST FOR CALIBRATION OF FULL SCALE.

NOTE: R6 B HAS BEEN DELETED

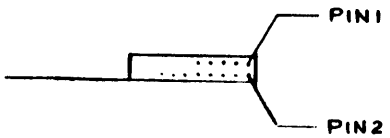
DT2781 D/A CONVERTER

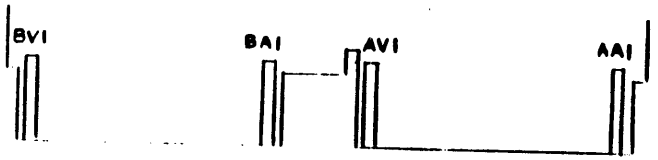
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
B	EPO74	21020074	C
SCALE		SHEET 8 OF	



J1 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CH 8	2	CH 8/ RET 0
3	CH 1	4	CH 9/ RET 1
5	CH 2	6	CH 10/ RET 2
7	CH 3	8	CH 11/ RET 3
9	CH 4	10	CH 12/ RET 4
11	CH 5	12	CH 13/ RET 5
13	CH 6	14	CH 14/ RET 6
15	CH 7	16	CH 15/ RET 7
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND
21	RTCINL	22	D GND
23	DAC B RET	24	DAC B OUT
25	DAC A RET	26	DAC A OUT

RTCINL ON WIRE POST





BOTTOM EDGE CONNECTOR							
COMPONENT SIDE		SOLDER SIDE		COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
BA1		BA2	+ 5V	AA1		AA2	+ 5V
BB1		BB2		AB1		AB2	
BC1		BC2	D GND	AC1		AC2	D GND
BD1		BD2		AD1		AD2	
BE1		BE2	BDAL 2L	AE1		AE2	BDOUT L
BF1		BF2	BDAL 3L	AF1		AF2	BRPLY L
BH1		BH2	BDAL 4L	AH1		AH2	BDIN L
BJ1	D GND	BJ2	BDAL 5L	AJ1	D GND	AJ2	BSYNC L
BK1		BK2	BDAL 6L	AK1		AK2	BWT BTL
BL1		BL2	BDAL 7L	AL1		AL2	BIRQ L
BM1	D GND	BM2	BDAL 8L	AM1	D GND	AM2	BIAK IL
BN1		BN2	BDAL 9L	AN1		AN2	BIAK OL
BP1		BP2	BDAL 10L	AP1		AP2	BBS 7L
BR1		BR2	BDAL 11L	AR1		AR2	BDMG IL
BS1		BS2	BDAL 12L	AS1		AS2	BDMG OL
BT1	D GND	BT2	BDAL 13L	AT1	D GND	AT2	BINITL
BU1		BU2	BDAL 14L	AU1		AU2	BDALOL
BV1	+ 5V	BV2	BDAL 15L	AV1		AV2	BDALIL

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	0
SCALE			SHEET 8 OF 8

DATA TRANSLATION INC
4 Strathmore Rd., Natick MA 01760
(617) 655-5300 Telex 948474