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PRELIMINARY DESCRIPTION
DATA DISC MODEL 1764 DISC MEMORY SYSTEM FOR DEC PDP-11 COMPUTERS

1.0 INTRODUCTION

The Model 1764 Disc Memory System consists of a Model 1264 controller coupled with a Data Disc 7200H Series Disc. The 1764 Disc Memory system is a hardware emulator of the DEC RC11/RS64 Disc Memory system. The 1764 is not only a hardware replacement for the DEC RC11/RS64, but in addition, has higher capacity (up to a million words at 1800 rpm) and faster transfer rate.

Other features are:

- 8.5 milliseconds or 16.7 milliseconds average access time
- CRC error detection for data validity.
- Real-time look ahead for reducing latency time.
- Compact packaging: Disc with power supply occupies only 14 inches of rack space; controller mounts in PDP-11 mainframe or expansion cabinet.

2.0 REFERENCE DOCUMENTS

2.1 PDP-11, Processor Handbook

2.2 PDP-11, Peripherals and Interfacing Handbook

2.3 7200 Series Disc Memory Operation and Maintenance Manual, 1973 Data Disc, Part no. 3016000-00.

3.0 SPECIFICATIONS

3.1 See Attachment 1

3.2 Disc Format:

	7200H	7230L
. Bits/Track	139,200 (+500, -0)	70,000
. Bits/Sector	538	538
. Sector Marks/Track	256	128

With first Sector Mark starting 40μs (min.) after Track Origin, the gap between the last Sector Mark and the first Sector Mark is 400μs minimum (600μs maximum).

Other:

. Words/Sector	32
. No. of Tracks/Disc Memory	8 to 128

3.3 Timing:

	7200H	7230L
. Disc Speed	1800 rpm	3600 rpm
. Average Access Time	16.7 ms	8.5 ms
. Worst Access Time	33.3 ms	16.7 ms

. Data Tx rate between the Controller and the Disc 4μs/word maximum

. Peak Tx rate between the Computer Memory, Controller and the Disc 260μs/32 words

3.4 Priority Interrupt:

Priority Level:	BR5 (selectable by plug-in circuit chip)
Interrupt Vector Address:	210
Interrupt Caused by:	Function Complete - Error Condition

4.0 FUNCTIONAL DESCRIPTION

The Model 1264 Controller and the 7200H Series Fixed-Head Disc File form a fast, low-cost, random-access, bulk-storage disc memory system (Model 1764) for the PDP-11 computer. This memory system provides from 32,768 to 1,048,596 16 bit words of storage. Data transfer to or from memory is via the DEC UNIBUS

with the 1264 controller acting as bus master (DMA) without processor intervention.

The disc memory stores data in a 32 x 16-bit word sector format. Cyclic Redundancy Check (CRC) error detection is performed on a sector basis, the sectors being randomly addressable.

Fast track switching time permits spiral read and write. Data may be read or written in blocks from any length up to 65,536 words. When the last sector address on a track has been used, the addressing will automatically advance to the next track.

Real-time look ahead is provided. This feature lets the processor continuously monitor the current position of the disc and minimize disc latency time.

5.0 CONTROLLER REGISTERS

The 1264 Controller has six main registers that are accessible to the programmer. They are:

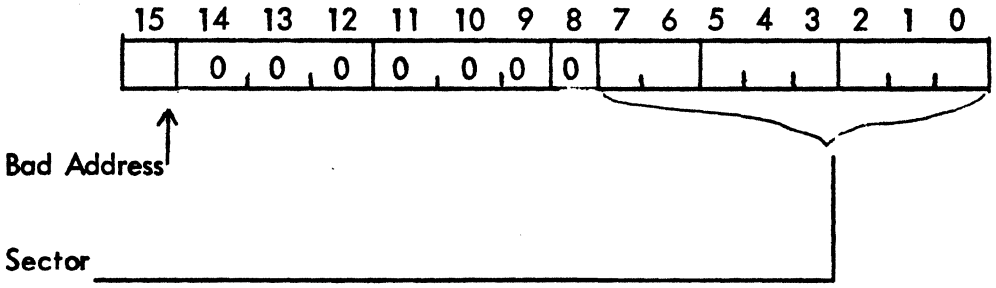
		Address
. Look Ahead Register	RCLA	777440
. Disc Address Register	RCDA	777442
. Disc Error Status Register	RCER	777444
. Command & Status Register	RCCS	777446
. Word Count Register	RCWC	777450
. Current Address Register	RCCA	777452

Note: All unused bits of these registers will appear as zeroes when read, and will be ignored if attempted to be written.

If registers 777454 (Maintenance Register) or 777456 (Data Buffer) are addressed, the 1264 Controller responds with zeroes on Data lines if read. If writing is attempted, the Data line contents will be ignored.

5.1 Look Ahead Register (RCLA = 777440)

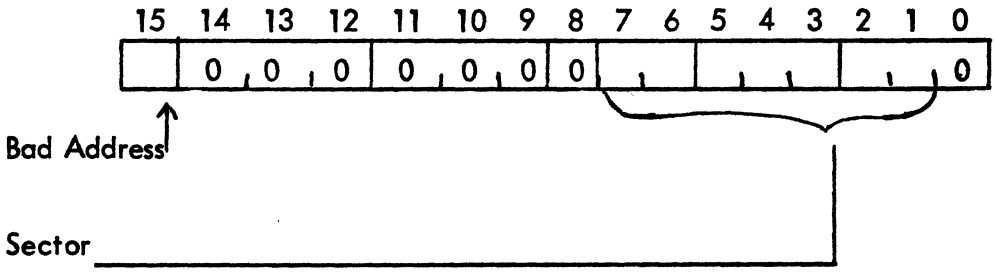
Format for 1800 RPM 7200 Series Disc:



Bit 0 - 7: Current Sector Position

- 15:Bad Address - if "1" indicates that the address is just changing and therefore may or may not be just valid. In such case, inquiry should be repeated.

Format for 3600 RPM 7230 Series Disc:



Bit 1 - 7: Current Sector Position

15: Bad Address - if "1" indicates that the address is just changing and therefore may or may not be just valid. In such case, inquiry should be repeated.

The sector addresses for the disc are not a sequence of consecutive numbers, the sector addresses are interlaced to provide processing time between sectors. For the 7200 Series Disc the sector address sequence is as follows:

0, 128, 1, 129, ...126, 254, 127, 255, 0, 128.....

For the 7230 Series Disc, the sector address sequence is as follows:

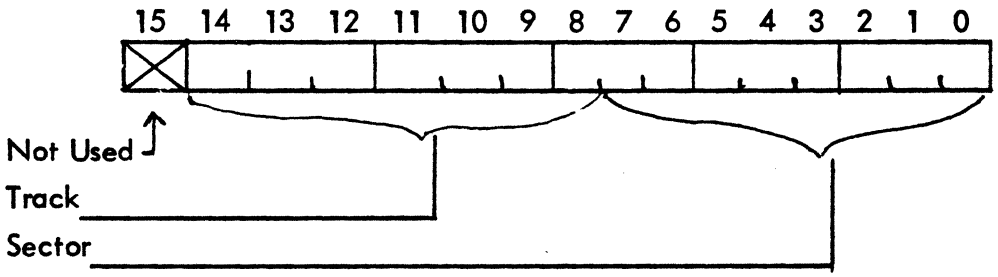
0, 64, 1, 65....., 62, 127, 63, 128, 0, 64.....

The RCLA Register always contains the address of Sector currently under the read/write head. RCLA is a real time register which gets updated on every sector mark. The RCLA Register is Read Only.

The RCLA Register is Read Only.

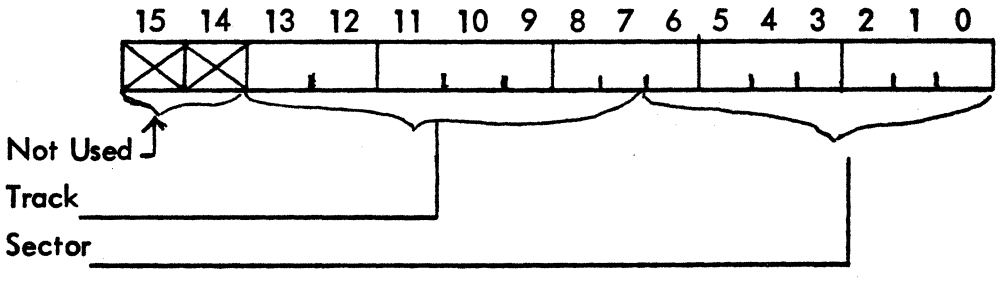
5.2 Disc Address Register (RCDA = 777442)

Format for 1800 RPM 7200 Series Disc:



Bit: 0 - 7: Sector
4 - 14: Track
15: Not Used

Format for 3600 RPM 7230 Series Disc:



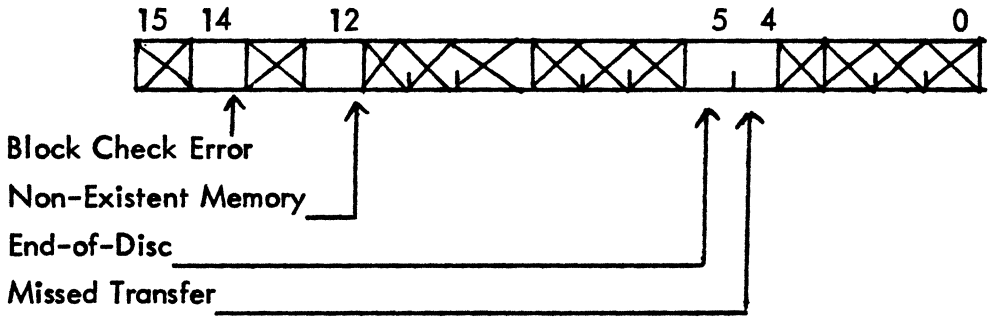
Bit: 0 - 6: Sector
7 - 13: Track
14 - 15: Not Used

Before any transfer between the 1264 Controller and disc memory, the controller must locate the addressed Sector. The Disc Address Register is loaded with a number that selects one specific Sector of one Track. If multiple sector operation is required (word count is more than 32) the RCDA is automatically incremented.

The RCDA is read/write register, all bits initialized to zero.

5.3 Disc Error Status Register (RCER = 777444)

Format:

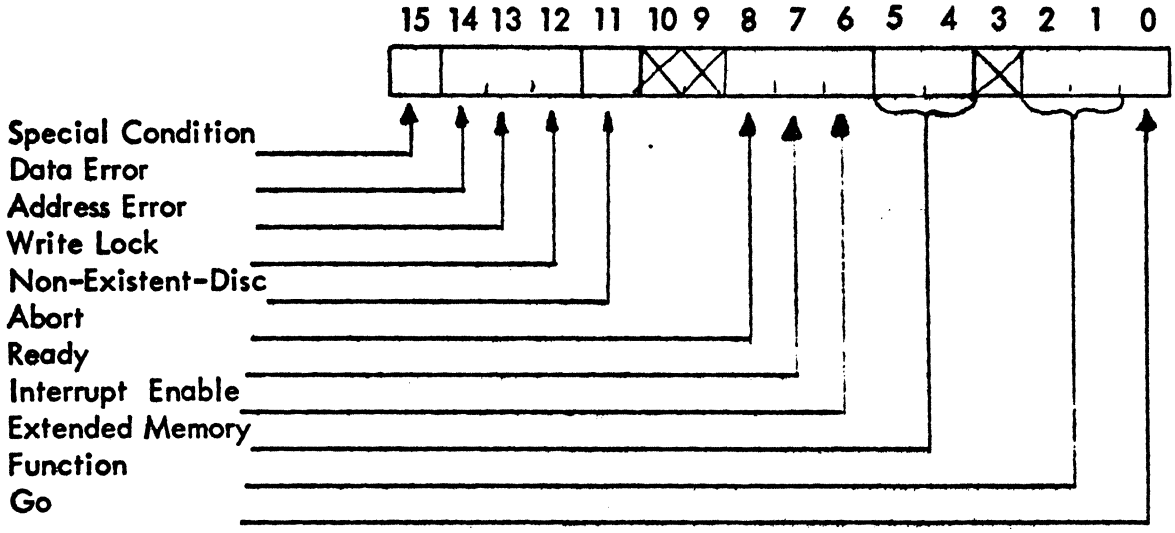


Bit	4:	MT	Missed Transfer - Sets to indicate that the 1264 Controller did not make a NPR for date transfer since initiating a function and the disc revolved more than once.
	5:	EOD	End-of-Disc - Sets after the very last word of the disc is written, or after this very last word is transferred from the 1264 Controller (after it had been read from the disc). This is not an error condition. If at this time the Word Count Register did not overflow, bit 11 ("Non-Existent - Disc") of the Disc Command and Status Register will be set also.
	12:	NEM	Non-Existent Memory - Sets if 1264 Controller initiates an UNIBUS data transfer and does not receive a slave sync signal (SSYN) within 20 microseconds after it asserted Master Sync (MSYN). This condition usually indicates that no register or memory has been assigned to that address.
	14:	BCER	Block-Check-Error - Sets if the Cyclic Redundancy Check (CRC) that is read back from the disc does not agree with the computed check on the data just read. The current operation will not be aborted if BCER sets.

The RCER is read only. All bits are initialized to zero.

5.4 Disc Command and Status Register (RCCS = 777446)

Format:



Bit 0: GO - Setting initiates the function specified.
Write only and initialized to zero.

1,2: Function - Specify the desired operation.
Controller decodes these bits as follows:

Bit 2	Bit 1	Function
0	0	No operation
0	1	Write
1	0	Read
1	1	No operation

These bits are read/write and initialized to zero.

4,5 Extended Memory - Two most significant bits when 18 bit address is in effect. These two bits are logical extension of the Current Address Register (RCCA).
These are read/write and initialized to zero.

6: Interrupt Enable - Program Interrupt will be allowed to occur only when this bit is "1".
This bit is read/write and initialized to zero.

7: READY - Controller sets this bit to indicate completion (or abortion) of an operation and is ready for the next operation.
This bit is read only and initialized to "1".

8: **ABORT** - If declared as "1" any operation in progress is aborted, and Interrupt generated (if Enabled) This bit is write only and initialized to zero.

11: Non-Existent-Disc - Set to indicate that Disc Address Register (RCDA) overflowed, and the word transfer did not finish yet.

Note that this bit will be "1" only when the Word Count Register did not overflow so that last Sector of the last Track can be operated on without getting an error status.

This bit is read only and initialized to zero.

12: Write Lock - Set to indicate that a write attempt was made on a write-protected area of the disc.

This bit is read only and initialized to zero.

13: Address Error - logical OR of Error Status bits NEM (bit 12) and MT (bit 4) of RCER register.

This bit is read only and initialized to zero.

14: Data Error - Identical with bit 14 of RCER register.

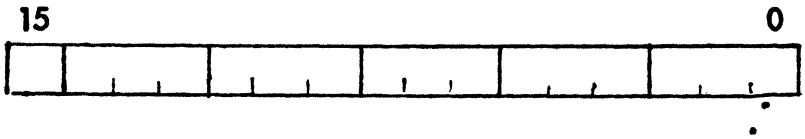
This bit is read only and initialized to zero.

15: Special Condition - Set to indicate that the Controller sensed an error condition. It is logical OR of bits 11 - 14 of this register and RCER register.

This bit is read only and initialized to zero.

5.5 Word Count Register (RCWC = 777450)

Format:

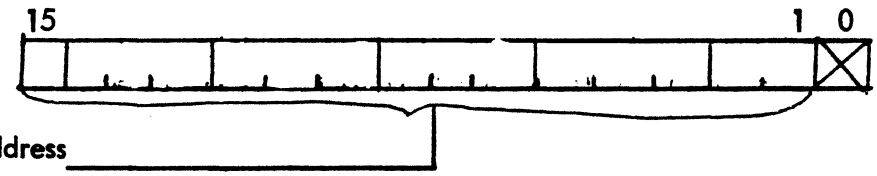


Bits 0-15 Word Count - This register is loaded with the 2's complement of the block length and incremented by one after each transfer. When the content of this register has been incremented to zero an overflow signal will end the operation. By definition the block size is limited to 65,536 (2^{16}) words.

This register is read/write.

5.6 Current Address Register (RCCA = 777452)

Format:



Before initiating any transfer operation the program declares the address of the UNIBUS location with which the controller should start data transaction. All data transfers take place at even address boundaries (no byte capability). After each data transfer this register is incremented by two. When this register overflows, extended memory bits in RCCS are incremented. Bit 0 of this register is always zero, and remaining bits are read/write. Initialization clears this registers.

6.0 DATA BUFFER

To remove the necessity of the UNIBUS to respond to a NPR request at a certain minimum rate, a 32 word Data Buffer has been designed into the 1264 Controller. Data is always transferred directly between the 1264 Controller Memory on the NPR level, without processor supervision. The Data Buffer is not accessible to the programmer.

7.0 WRITE PROTECT

Through a switch and 7 diodes in a 1264 Controller, writing can be inhibited on consecutive binary groups of Tracks starting from Track 0. The 3-position switch can be set to inhibit writing on no Tracks, all tracks or selected Tracks, With the switch set to protect selected Tracks, the protection can be set as shown on the following table: (Fig. 1).

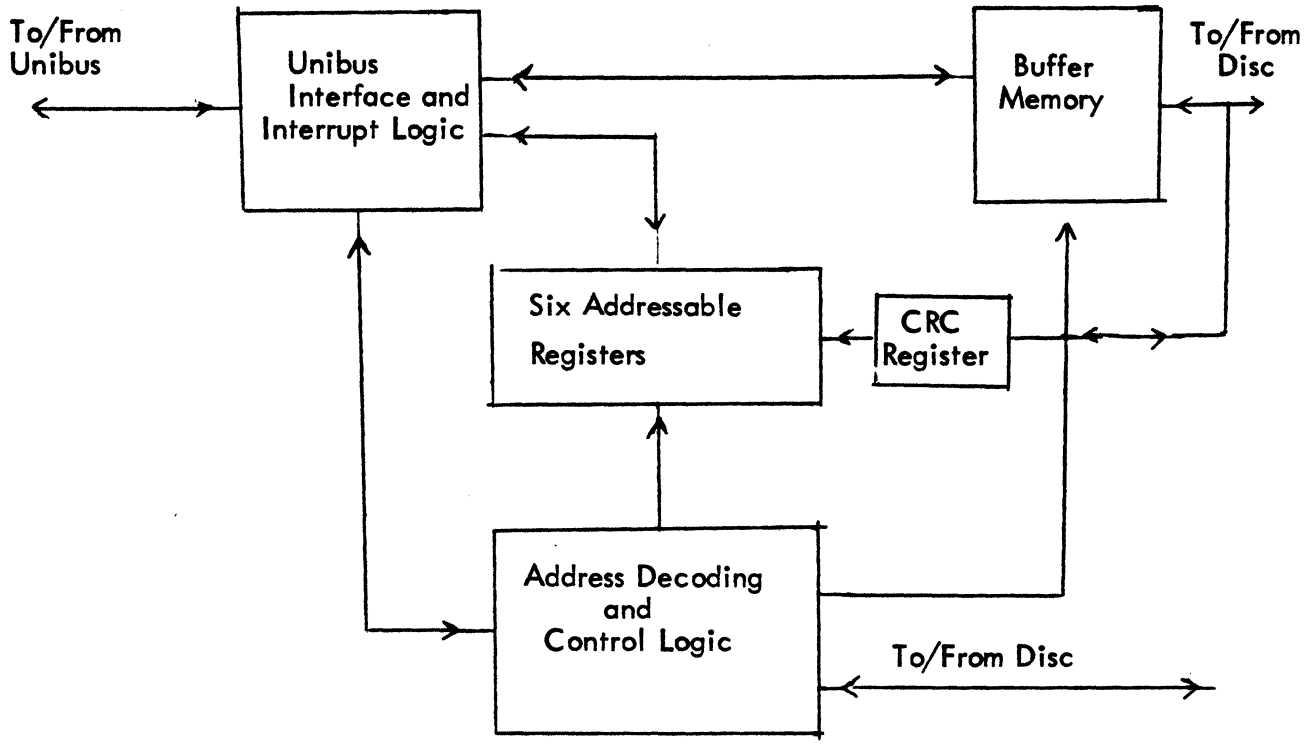


FIGURE 2
Controller's Basic Block Diagram

10.0 PHYSICAL

The 1764 Memory System consists of two parts: the 1264 Controller and the 7200H/7230L Series disc unit.

The disc memory consists of two rack-mounted packages 5-1/4" (power supply) and 8-3/4" (disc); therefore taking a total of 14.0" of rack space.

The 1264 controller is designed to be contained on a single DEC BB11 system module which mounts within the PDP-11 chassis. Since the maximum word capacity is contained on a single disc, this is all the space ever needed for a fully expanded system.

Weight is: Disc Memory: 62 pounds; Power Supply: 22 pounds.

11.0 POWER

The disc memory operates on either 115V, 50 or 60 Hz power. At 115V ac, 60 Hz, the memory requires 12 amps starting current and 2.6 amps operating current. The 1264 Controller requires +5V at 3.5 amps, supplied from the PDP-11.

12.0 INSTALLATION

12.1 Mounting:

The Data Disc 1264 Disc Controller consists of P. C. boards plugged into DEC BB11-A System Unit. The cable from the Disc Memory Unit is also connected to this module. The module itself is mounted in the CPU mainframe or expansion chassis and connected to the Unibus with a M920 jumper. Two UNIBUS connectors are provided for daisy chaining or accepting the DEC M930 Terminator. The Power (+5V) connectors, provided in the computer plugs into slot A3.

12.2 Environmental Conditions:

No special environmental conditions are required for proper operation of the 1264 Controller. Ambient temperature may vary between 0°C to 70°C.

12.3 Power Requirements:

The 1264 controller obtaining its primary power +5V/3.5 A from the PDP-11 power supply.

ATTACHMENT 1

DATA STORAGE CAPACITY

Disc Model	7203	7233	7204	7234	7205	7235	7206	7236	7207	7237
Number of Tracks	8	8	16	16	32	32	64	64	128	128
Sectors/Track	256	128	256	128	256	128	256	128	256	128
Words/Sector	32	32	32	32	32	32	32	32	32	32
Total Words	65536	32768	131072	65536	262144	131072	524288	262144	1048576	524288