COMMUNICATION MACHINERY CORPORATION (CMC)

Ethernet Node Processor

ENP-30

Reference Guide

Communication Machinery Corporation
125 Cremona Drive
Santa Barbara, California 93117

(805) 968-4262

Document No. 6213000-05B November 15, 1988

ENP-30 Reference Guide

The information in this manual belongs to Communication Machinery Corporation (CMC) and is subject to change without notice. CMC makes no warranty of any kind regarding this manual, including, but not limited to, implied warranties of merchantability and fitness for a particular purpose. CMC assumes no responsibility for errors in this manual, nor liability for any damages arising from the furnishing, performance, or use of this manual. Reproduction of any part of this manual without the express written permission of CMC is prohibited.

CMC does not recommend the use of its products in any life support device or system where a malfunction of the product may directly threaten life or injury. The user of any CMC product in a life support device or system assumes all risk and liability for such use.

CMC Customer Support
(805) 685-6605

Table of Contents

List of Figures

List of Tables

Section 1
General Information

1.1 Introduction

This manual provides general information, hardware preparation and installation instructions, software preparation and loading instructions, functional description, and support information for the ENP-30 Ethernet Node Processor. The ENP-30 is manufactured by Communication Machinery Corporation (CMC). The terms ENP-30 and ENP are used interchangeably in this manual. Refer to the Appendices for a glossary of other abbreviations and acronyms used in this manual. See Section 1.4 for related documentation.

1.2 Product Description

The ENP-30 is a high performance communications processor on a MULTIBUS form-factor, multi-layer printed circuit (PC) board. It provides the physical interface and intelligence necessary to attach information processing devices to the Ethernet, a Local Area Network (LAN), to allow a high speed exchange of information. Each ENP contains node-specific software, as well as industry-standard protocol software for exchanging information throughout the network.

1.3 Features

Features of the ENP-30 include:

- 10MHz MC68000 MPU (MC68010 optional).
- 128KB or 512KB dual-access DRAM with parity and no wait states.
- Up to 64KB PROM (2 sockets).
- MULTIBUS (IEEE 796) A24:D16 master and slave interface for host to ENP communications.

- Node address PROM contains a world-wide unique Ethernet address issued by the Xerox Corporation.
- A programmable interrupt for protocol software timing.
- Local Area Network Controller for Ethernet (LANCE), with
  - — Buffer management structures in shared local RAM,
  - — DMA to shared local RAM,
  - — Line access protocol (CSMA/CD), and
  - — Extensive diagnostics and error reporting.
- Serial Interface Adapter (SIA), with
  - — Manchester encoding/decoding, and
  - — Transceiver cable interface.
- Dual, RS-232, Asynchronous, Serial, Receiver-Transmitter, Communication Ports (DUART).
- MULTIBUS interrupt (NBVI).
- MULTIBUS to onboard processor interrupts.

1.4 Related Documentation

The *MULTIBUS Specification Manual*, the *K1 Kernel Software User's Guide* and the *ENP Debugger User's Guide* are all applicable to the ENP. Other documents referenced in the Appendices can provide additional information on Local Area Networks, communications protocols, and Node Processors.

Section 2
Specifications

2.1 Operational Specifications

The ENP-30 requires 5A at +5Vdc, 0.5A at +12Vdc, and 0.1A at -12Vdc. These voltages may vary a maximum of 5% without impacting the performance of the module. MULTIBUS signals conform to the IEEE-796 standard.

2.1.1 Mechanical

The ENP-30 conforms to the MULTIBUS IEEE 796 standard form factor. The printed circuit (PC) board has eight layers, conforming to MIL-P-55110.

2.1.2 Environmental

The ENP-30 is designed for operation or storage in the following environment:

Table 2-1. Environmental Conditions

Condition	Operation	Storage
Temperature	5 to 50 degrees C	−40 to 85 degrees C
Humidity	5% to 95% non-condensing	Same
Elevation	0 to 10,000 ft.	0 to 10,000 ft.

2.1.3 MULTIBUS Compliance

Table 2-2. MULTIBUS Compliance

MASTER DATA TRANSFER

M24 or M20
D16

SLAVE DATA TRANSFER

M24 or M20
D16

INTERRUPTER OPTIONS

VO L to MULTIBUS

Section 3

Functional Description

3.1 Introduction

This section provides overall block diagram level and operational descriptions for the ENP-30.

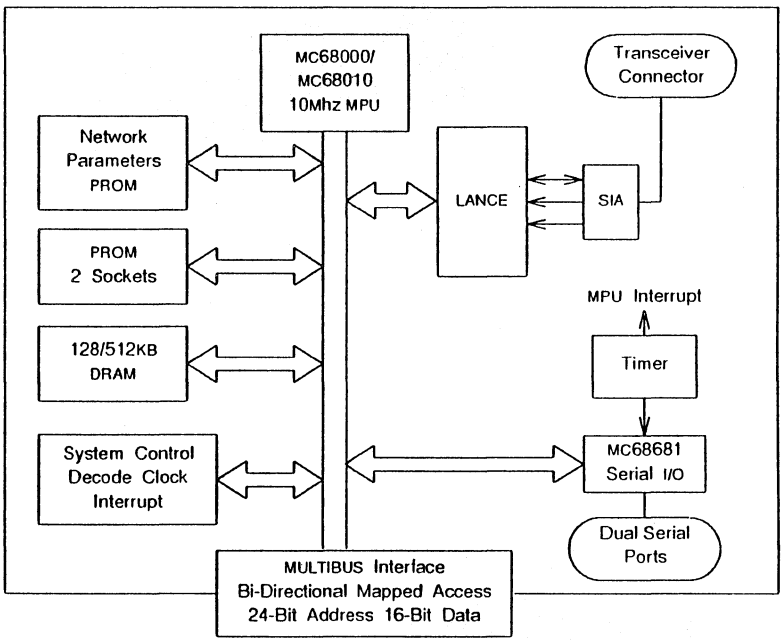


Figure 3-1. Block Diagram

3.2 Description

The ENP-30 is installed directly into the user's MULTIBUS backplane. Ethernet interfacing is accomplished by cable interconnections between the ENP transceiver connector and the associated Ethernet transceiver equipment.

The ENP-30 architecture includes: (1) an microprocessor unit (MPU), that performs supervisory functions over a VLSI local area network controller for Ethernet (LANCE), (2) closely coupled DRAM, (3) PROM for protocol processing code, (4) a bus interface to a host system, and (5) The signaling and timing utilities required to maintain a communication environment.

3.2.1 Microprocessor Unit

The on-board Microprocessor Unit (MPU) is the 10MHz MC68000 or MC68010 MPU. The MPU responsibilities include: (1) command and data transfer to and from system-visible memory, (2) response to and generation of bus interrupts, (3) execution of the network communications protocol upper layers, (4) running the K1 Kernel firmware, (5) implementing Layer 2 of ISO protocol, (6) software refresh for the DRAM, (7) timer functions, and (8) running self-diagnostics on power up or initialization.

Refer to the Memory Map in Section 6. The MPU runs at a 10MHz clock rate, synchronous with the LANCE clock.

3.2.2 Node Address PROM

Every Ethernet station (host and ENP) has been assigned a world-wide unique 48-bit address by the Ethernet Address Administration Office, XEROX. The address is used for station identification on all data transmissions. This address resides in the node address PROM and is read by the application protocol software during the start-up procedure. It is stored in a 512 X 4 bit PROM.

3.2.3 PROM Sockets

The ENP-30 has two 28-pin sockets for PROM. These sockets accept 32 Kilo (K) bits x 8, 16K bits x 8, 8K bits x 8, and 4K bits x 8 PROMS of various access times.

3.2.4 DRAM

The ENP-30 board, in the standard configuration, includes 128KB of Dynamic Random Access Memory (DRAM) with parity. Memory can be factory upgraded to a maximum of 512KB on board. The memory causes no wait states when accessed from the on-board MPU. Software refresh occupies about 5.0% of the MPU bandwidth.

Parity errors are reported to the MPU as Level 7 interrupts. The dynamic memory is accessible from the system bus, from LANCE, and from the MPU. The MULTIBUS has highest access priority, followed by the LANCE, and the MPU has lowest priority.

There are memory usage considerations due to the LANCE device on the ENP. CMC requires that the memory buffers accessed by LANCE reside on the ENP. LANCE performs eight-word bursts when writing received Ethernet data to memory or reading data from memory to send on the Ethernet. If this data were passing on the system bus, significant bus bandwidth would be consumed, impacting the access of other devices to the bus. It is possible that data could not be supplied or accepted fast enough to maintain the Ethernet 10Mb data rate, using this direct system bus approach. Because of these factors, all Ethernet data should be staged in the ENP memory between the Ethernet transfer and the system bus transfer. Either the ENP or the host processor can manage the transfer of the data between ENP memory and user memory.

During LANCE activity, each host access to ENP memory can incur up to a maximum 9µs wait before being granted access to the memory. This is because the LANCE performs transfers in eight-word bursts (it acquires the local data bus and holds onto it for the entire eight-word transfer. Therefore, if the host's system bus time out interval is less than 12µs, the host driver should be designed so that the data areas used for controlling data transfers reside in host memory and that the

ENP performs all data transfers between memory and system bus memory. If, due to UNIBUS acquisition latency, MPU to UNIBUS transfers average greater than 4µs or exceed about 12µs (worse case), the LANCE SILO (see 3.2.5) may overflow or underflow.

3.2.5 Local Bus Interface

The ENP can act as both master and slave on the MULTIBUS. This means that the MPU can read and write into bus memory, and the ENP memory may be accessed by other masters on the bus.

A single on-board address and data bus is shared between LANCE, RAM and ROM, system bus interface, and MPU. Bus requests to the MPU cause it to yield this local bus to the MULTIBUS master during slave access to the ENP, or to the LANCE during LANCE DMA access to on-board memory.

The local bus interface is structured so that all other resources are inactive while one resource is using the local bus. For example, a MULTIBUS access to on-board memory could be held off for up to 9µs, while the LANCE completes 8 DMA cycles. Similarly, the MPU can complete no work during LANCE DMA or host access to ENP resources. At 120 packets per second with 1500 bytes per packet and an average of 800ns per word DMA access, the LANCE DMA will take approximately 7.4% of the local bus bandwidth. With 5% of the bus used for software refresh (and negligible MULTIBUS access) this leaves approximately 88% of the local bus for the MPU. LANCE DMA use of the local bus is sporadic, occupying a large percentage of the bus when in use. During the active reception or transmission of data packets on the 10Megabit (Mb) Ethernet, LANCE alone uses more than 50% of the local bus bandwidth.

The peak throughput of the ENP is nearly 10Mb with the LANCE receiving/transmitting Ethernet back-to-back packets, without loss of status or data. The maximum number of back-to-back packets is limited only by the available buffer space. The best average throughput of the ENP will be dictated by network conditions, host performance, and available on-board MPU processing power.

The local bus architecture allows either the ENP MPU or the host to move data between the host system and the ENP DRAM. If the ENP MPU moves moves data via UNIBUS Master Operations, bus latency should average 4µs with a peak of 12µs. If the host moves data, it must have a bus time-out of at least 12µs.

Communication between the ENP and the network's physical medium (the coaxial cable) is handled by the ENP Kernel software and the LANCE device. The *K1 Kernel Software User's Guide* describes the related start up protocols that are required for ENP operation with the Kernel. All protocols are compatible with the *Ethernet 2.0 Specification*, as defined by Xerox, DEC, and Intel.

3.2.6 Clock Timer

A programmable timer causes a periodic interrupt to the MPU for protocol software timers. The K1 Kernel uses this timer to generate an interrupt every 2ms.

3.2.7 Local Area Network Controller for Ethernet (LANCE)

The Local Area Network Controller for Ethernet (LANCE) chip set consists of a DMA-oriented link-layer controller (Am7990) and a Serial Interface Adapter (SIA), the Am7992. The SIA provides proper IEEE 802.3 or Ethernet 1.0 transceiver interface levels and signaling and the TTL signals to the LANCE.

The LANCE features the Ethernet 10Mb data rate, an MPU compatible interface, a 16-bit data bus, multiplexed address/data bus, a DMA controller with 24-bit addressing, a sophisticated buffer management structure, a 48-byte SILO data buffer, diagnostic aids, three modes of receive addressing comparisons, CSMA/CD network access algorithm, and extensive error reporting.

The Am7990 deals directly with control structures and data in the ENP memory. The control structures (descriptor rings) supplies the LANCE with address and length information on data buffers and command and status information on each buffer or message.

Buffer management features include a defined circular queue of buffer descriptors called descriptor rings. Up to 128 buffers may be queued awaiting processing by LANCE at any one time. Data buffers may be chained to handle long packets in multiple data buffer areas. LANCE controls an *own* bit for each buffer that signals when the buffer has been filled or emptied and is available for action by the processor.

The 48-byte SILO buffer considerably relaxes the initial response time required for a DMA transfer request. LANCE services the SILO with DMA bursts of 8 words for each system bus acquisition. A burst takes 6.4µs or less (0.8µs/word) to complete.

There are three modes of network receive address comparison:

- The physical mode, which is a full comparison of all 48 destination address bits.
- The multicast mode, which is a logical mode that puts the 48 bits through a hash filter to determine one of 64 logical types.
- The promiscuous mode where all packets are received, regardless of address.

LANCE implements the full CSMA/CD network access algorithm. Upon detection of a collision, it sends a jam signal, followed by a backoff algorithm, before attempting to transmit again. After 16 successive collisions, it reports an error. Other reported errors include babbling transmitter (transmission of more than 1518 bytes), collision detection circuitry nonfunctional, missed packet due to insufficient buffer space, and a memory time-out (DMA memory access not complete in a reasonable amount of time). These errors cause an interrupt to be generated. Individual packet errors include CRC error, framing error, and SILO overflow or underflow error.

Refer to Section 10 for additional information about the LANCE.

3.2.8 Serial Interface Adapter

The Serial Interface Adapter (SIA) performs the Manchester encoding/decoding necessary for interfacing LANCE to Ethernet. It is compatible with standard Ethernet bus transceivers operating at

10Mb/s. The decoder acquires the clock and data within six bit times (600ns). It features guaranteed carrier detection and collision detection threshold limits and transient noise rejection. The receiver decodes Manchester data with up to plus or minus 20ns clock jitter, which represents 1/5-bit time.

3.2.9 Transceiver Connector

The Transceiver (XCVR) connector on the ENP is a 15-pin, MIL-C-24308, D-type connector that couples the ENP to the transceiver cable. The connector is female, with a slide latch assembly. Applicable IEEE Standard 802.3 electrical interface requirements are met.

3.2.10 MULTIBUS Slave Address

The MULTIBUS slave interface responds as a block of 128KB of word-wide standard data space on a modulo 128KB boundary (see Figure 19). The first 4KB of this window is non-responsive after the RAM/ROM swap control is set. The next 116KB maps to ENP DRAM at $F01000–$F1FE00. The first 4KB of ENP DRAM is used for vectors and debugger stack.

As bus master, the ENP-30 may access the entire bus address space, although some limitation may have to be accepted by system considerations.

3.2.11 Serial I/O

A dual RS-232 interface is driven by an SCN68681 controller. Baud rates are programmable from 50 to 38.4K baud. Connection is through two 26-pin box connectors located on the PC board top edge. These ports provide the capability for a remote diagnostic link, local monitoring and debugging, or a printer interface for logging of network statistics.

The SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-VLSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The DUART can be

used in polled or interrupt-driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of 18 fixed baud rates, a 16x clock derived from a programmable counter/timer, or an external 1x or 16x clock. The baud rate generator and counter/timer operate directly from a crystal.

Each receiver is buffered in quadruplicate to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt-driven systems.

3.3 ENP-30 Firmware

There are two PROM firmware packages available for the ENP-30. They are the K1 Kernel, or the K1 Kernel and CMC Debugger together. The standard ENP configuration includes the K1 Kernel PROM. A PROM that includes the K1 Kernel with the CMC Debugger is available separately.

3.3.1 K1 Kernel Firmware

The K1 Kernel supplies functions that control and monitor the hardware features of the ENP-30. The K1 Kernel allows downloading directly over the MULTIBUS from the host and gathers running statistics on all conditions reported by LANCE.

The K1 Kernel manages LANCE status registers and descriptor rings, performs software refresh and timer functions, and manages interrupts, allowing protocol software to be written in a high-level language such as Pascal or C. The use of user-developed protocol software is encouraged, but the software refresh must always be present. Without a non-maskable interrupt every 1.6384ms, the DRAM contents disintegrates. For more information, refer to the *K1 Kernel Software User's Guide*.

3.3.2 ENP Debugger

The ENP debugger is a ROM-based debugger for new program development and debugging. It is a full debugger with multiple breakpoints, memory examine, modify, test and move, an assembler, disassembler, download capabilities, and includes software memory refresh. Refer to the *ENP Debugger User's Guide* for more information on the Debugger.

Section 4

Preparation and Installation

4.1 Introduction

This section provides hardware preparation and installation instructions for the ENP-30.

4.2 Unpacking Information

Note

If shipping container is damaged upon receipt, request carrier's agent to be present during unpacking and inspection of equipment.

Unpack equipment from shipping container. Refer to packing list and verify that all items are present. Save packing material for storage or reshipping.

4.2.1 Hardware Preparation

The following paragraphs describe the hardware configuration options that are available, in the event that the factory configuration, as shipped, needs to be changed.

4.2.2 Standard Jumper Configuration

Each ENP is shipped with the jumpers properly configured for standard operation. The standard settings for the principal user-configurable options are:

- IEEE 802.3 Ethernet type selection.
- 20-bit MULTIBUS address mode.
- MULTIBUS memory address $A0000
- MULTIBUS interrupt level four.
- MULTIBUS parallel arbitration.

In the event that jumper configurations need to be changed, the jumper platforms are labeled on the PC board and shown in Figure 4-1 for easy location. Table 4-1 provides a list of all jumper platforms and their functions.

Table 4-1. Jumper Platforms

No.	Description
JP01	Slew Rate Capacitors (Not installed at factory.)
JP02	External Reset and Abort Header
JP03	Ethernet 1.0 or Ethernet 2.0/IEEE 802.3 Option
JP04	PROM Wait-State Options
JP06	PROM Control
JP07	DRAM Column/Row Address Strobe Delay Select
JP08	MBI Window Decode Address Select A17:23
JP09	MULTIBUS Master and Acquisition Options
JP10	MULTIBUS Interrupt Level Select
JP11	MULTIBUS Address Path Width Select AC 20:23

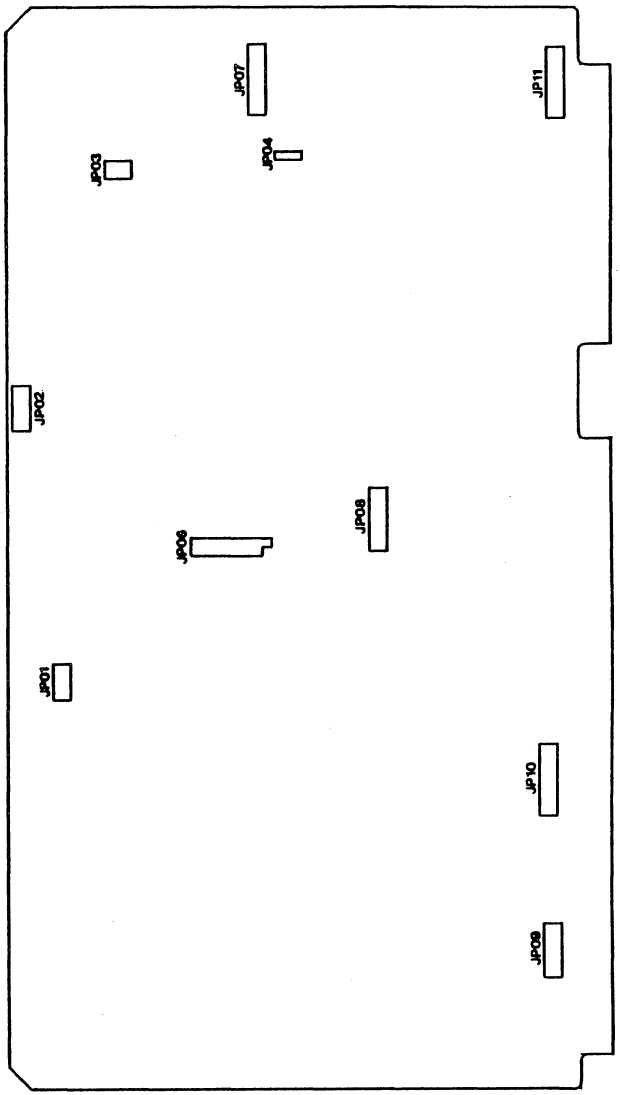


Figure 4-1. Jumper Platform Locations

4.2.3 Jumper Platform Description

The following paragraphs describe the jumper platforms and the configuration options available. The jumper platform locations on the PC board are shown Figure 4-1. If this is a standard installation and the jumpers are properly configured, proceed to the installation instructions.

4.2.3.1 Slew Rate Capacitors (JP01)

Installing capacitors affords noise attenuation on these RS-232 lines. For details on capacitor specifications, consult Motorola document *Linear Interface ICs* (1979), under 1489A. No capacitors are installed at the factory (they are only necessary in electrically noisy environments).

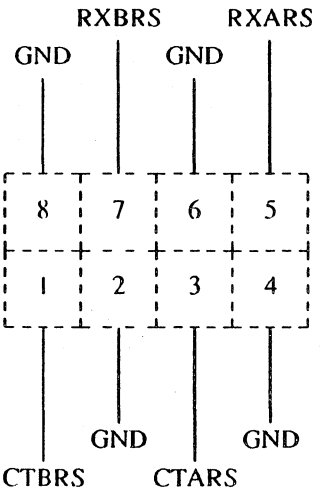


Figure 4-2. Slew Rate Capacitors (JP01)

4.2.3.2 External Reset and Abort Header (JP02)

The External Reset and Abort Header (JP02) is provided for connecting the optional Reset Box available from CMC, and included with the CMC *Software Development Kit.*

XRES – When asserted (pulled low) by an external device, the on-board reset logic is set in motion. The MPU (MC68000) is reset, behaving as described in the *MC68000 User's Guide*. All other on-board resources are reset simultaneously.

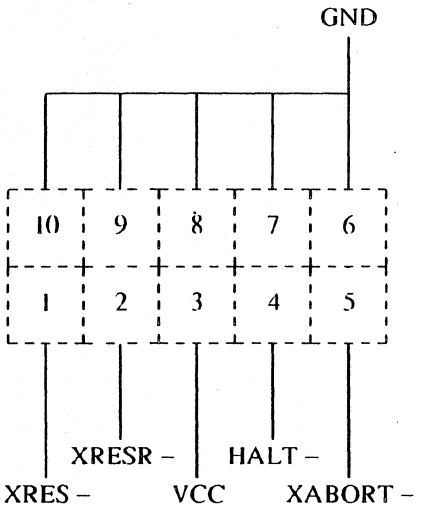
XRESR – Reserved for future use.

HALT – When asserted, the MPU is halted as described in the *MC68000 User's Guide.*

ABORT – When asserted (low), Bit 2 (ABORT) in the Lock Register (LOCKR) is set.[1] Concurrently a Level 7 interrupt is generated. A PROM-based debugger may then service the interrupt with the following:

- Halt program execution
- Dump address and data register, PC, SR, etc.

1. Programming Guide, Section 5.4.



To be used for connection
to external RESET and
software ABORT device.

Figure 4-3. External Reset and Abort Header

4.2.3.3 Ethernet Type Selection (JP03)

Ethernet type selection for Ethernet 1.0 or Ethernet 2.0/IEEE 802.3 is provided by JP03. The factory default configuration is for Ethernet 2.0/IEEE 802.3.

For ENP-30, Rev. B, the jumper between JP03 pins 4 – 5 should always be in place, as shown in Figure 4-4. In the event that the ENP-30, Rev. B, is to run with Ethernet 1.0 transceivers, place an additional jumper between JP03 pins 1 and 6. Also, replace U115 (PE8302) with a 16-pin DIP jumper platform and connect the pins as described in Section 9.

For ENP-30, Rev. C, JP03 is used to configure for IEEE 802.3/Ethernet 2.0 or Ethernet 1.0. For IEEE 802.3 or Ethernet 2.0 configuration, use the factory default of no jumpers, as shown in figure 4-4B. For ethernet 1.0, jumper settings depend on the device into which the ENP-30 is inserted. For a device such as CMC's DRN 3200 that has an isolated DC ground, jumpers should be placed between pins 1-4 and 2-3 as shown in figure 4-4C. For generic devices with DC ground connected to the chassis, a jumper should be placed between pins 1-4 as shown in figure 4-4D. All cases assume an intermediate internal cable with a chassis mounted metallic "D" connector ensuring an ethernet shell to chassis electrical connection.

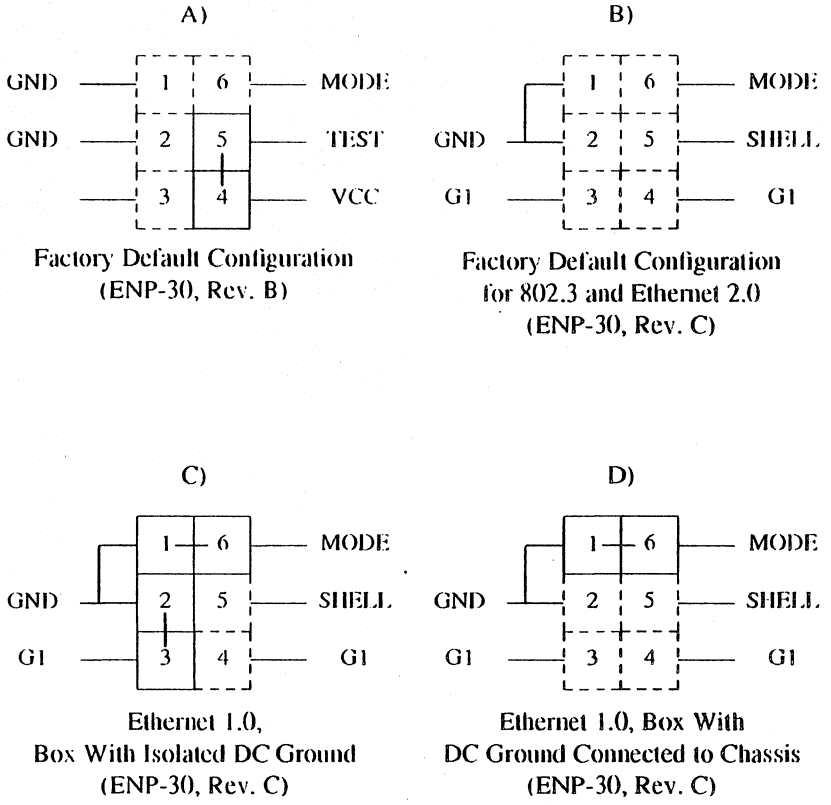


Figure 4-4. Ethernet Type Selection (JP03)

4.2.3.4 PROM Wait State Selection (JP04)

Selection of DTACK response for PROMs U28 AND U44 is provided by JP04. For a 3 to 4 wait state response, jumper pins 2 – 3 on JP04 (this corresponds to PROM access times of better than 550µs). If PROMs with 200ns or better response are used, 0 wait state jumpering is suggested; in this case, jumper JP04 pins 1 – 2. Best performance is obtained with 0 wait state jumpering.

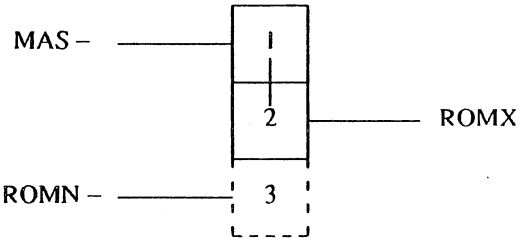


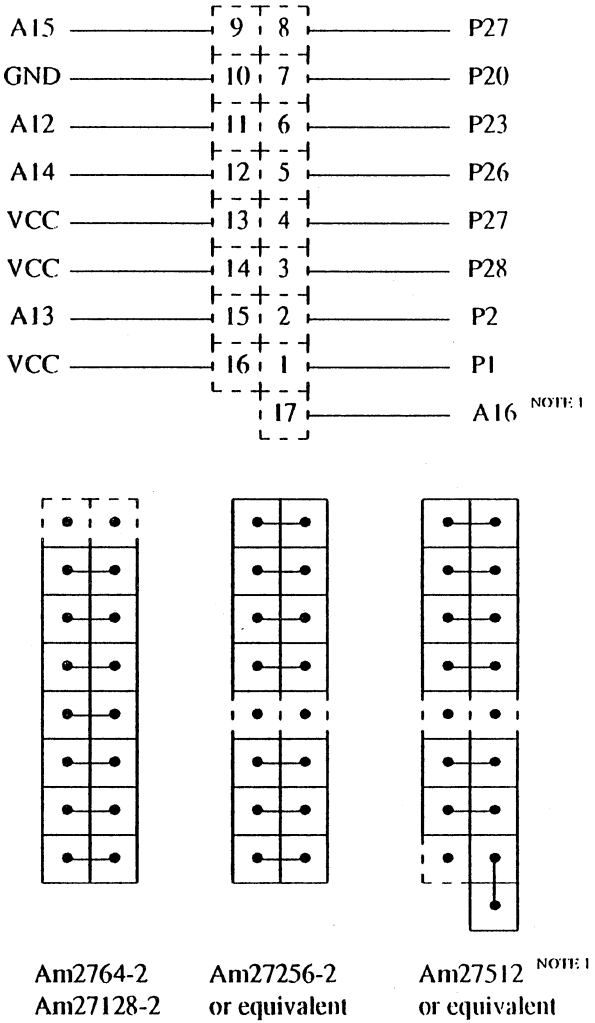
Figure 4-5. PROM Wait-State Selection (JP04)

4.2.3.5 PROM Control (JP06)

JP06 allows adaptation to a variety of 24- or 28-pin PROMs. The factory configuration is for Am27128 or Am2764 PROMs (Table 4-2). (See the PROM specification for descriptions of these signals).

Table 4-2. PROM Control Signal Table

Jumper Output Pin	PROM Control Signal Name
P1	VCC
P2	A13
P28	VCC
P27	PGM (Program Enable)
P26	A14
P23	A12
P20	CE (Chip Enable)



NOTE 1: JP06 pin 17 (A16) is only present on ENP-30, Rev. C. It allows a configuration for 512K PROMs.

Figure 4-6. PROM Control (JP06)

4.2.3.6 DRAM Column/Row Strobe and Address Multiplexer Delay Select and Cycle Timing (JP07)

This arrangement of jumpers allows adaptation to various types of DRAM timings. User reconfiguration is not recommended.

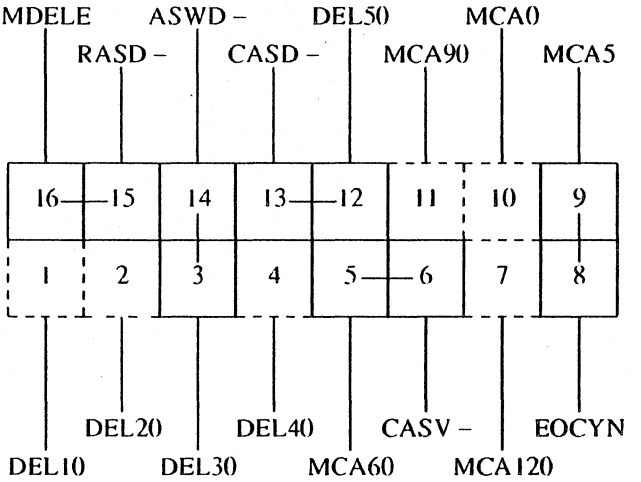


Figure 4-7. DRAM Column/Row Strobe and Address Delay Select and Cycle Timing (JP07)

4.2.3.7 MULTIBUS Window Decode Address Select (JP08)

These jumpers are used to select the MULTIBUS slave window address, which is either 20 or 24 bits long. The ENP-30 is configured at the factory for 20-bit addressing. The presence of a jumper means the bit is one, absence means the bit is zero.

The MULTIBUS slave window address default value set at the factory is $A0000. This address is also used in the 20-bit address example as an illustration of how to configure a 20-bit address, but if the default $A0000 slave window address is to be used, nothing needs to be done.

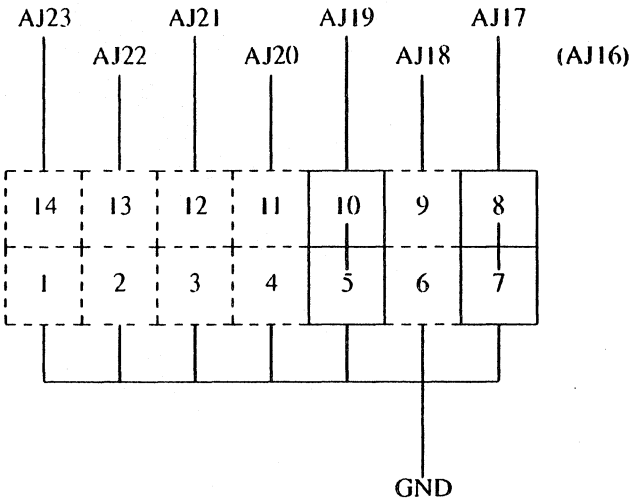
Of the five (20-bit) or six (24-bit) hexadecimal digits contained in the address, the most significant two are jumperable. The trailing four digits are set at 0; i.e., $*x*0000 or $*xx*0000.

Jumpers AJ23 to AJ20 constitute one hex digit. This is used Exclusively as the most significant digit in 24-bit addressing. This digit is NOT used in 20-bit addressing.

Jumpers AJ19 to AJ16 constitute the other hex digit, with AJ16 an implied 0 and not visible on the board. It is the most significant digit in a 20-bit address, and the second most significant digit in a 24-bit address.

The value of AJ16 is always 0 and must remain so, because it represents a 64KB boundary of MULTIBUS address space. When on, AJ16 represents an odd 64KB address. With either 128KB or 512KB of DRAM on the ENP, the MULTIBUS address boundary must be on a 128KB boundary, which requires an even 64KB boundary. AJ16 is omitted from the platform. AJ17 is the rightmost jumper pair on the platform.

20-BIT ADDRESS EXAMPLE: To select address $A0000 (the default value), begin by disregarding the trailing four zeros. Jumpers AJ23 to AJ20 are not used in 20-bit addresses. Jumpers AJ19 to AJ16 form the most significant digit, and the absent AJ16 is always 0. AJ19 (binary 8) and AJ17 (binary 2), in the first and third positions from the right, are shunted as shown in Figure 4-9.

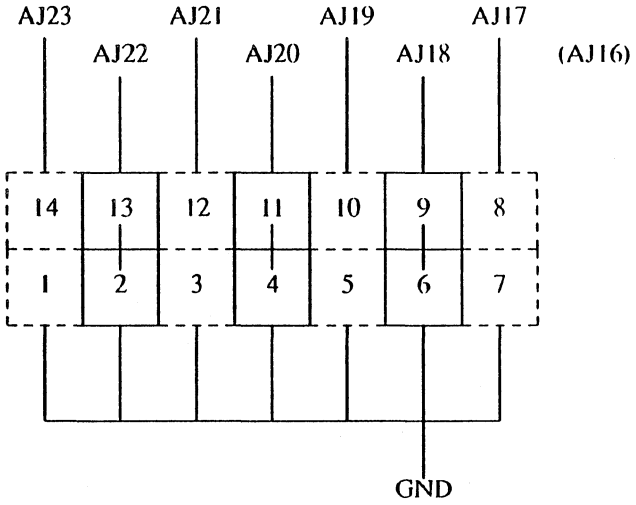


[xxxx] [101(0)] [0] [0] [0] [0]
A 0 0 0 0 = $A0000

The unused AJ23–AJ20 digit is represented by [xxxx], and AJ16 is represented by (0).

Figure 4-8. 20-Bit MULTIBUS Window Decode Address Select (JP08)

24-BIT ADDRESS EXAMPLE: To select address $540000, begin by disregarding the trailing four zeros. All jumpers are used in 24-bit addressing. The digit formed by AJ19 – AJ16 is the second most significant, and the absent AJ16 is always 0. Jumpers AJ22, AJ20 and AJ18, in the sixth, fourth, and second positions from the right are shunted as shown in Figure 4-10.



[0101] [010(0)] [0] [0] [0] [0]
5 4 0 0 0 0 = $540000

Again, AJ16 is represented by (0). Also, any jumpers on AJ23 – AJ20 will be ignored if JP11 is not appropriately jumpered for 24-bit addressing.

Figure 4-9. 24-Bit MULTIBUS Window Decode Address Select (JP08)

Table 4-3. JP08 Signal Names

Pins	Name	MULTIBUS Address Bit
JP08–1, 14	AJ23	A23*
JP08–2, 13	AJ22	A22*
JP08–3, 12	AJ21	A21*
JP08–4, 11	AJ20	A20*
JP08–5, 10	AJ19	A19
JP08–6, 9	AJ18	A18
JP08–7, 8	AJ17	A17

*Ignored in 20-bit mode. Leave jumpers off.

4.2.3.8 MULTIBUS Master and Acquisition Control Options (JP09)

This jumper platform allows the ENP-30 to be configured for various master types or as the system controller. These configurations are listed below.

- A jumper between pins 1 – 12 allows the ENP-30 to sense CBRQ* (factory configuration).
- A jumper between pins 2 – 3 allows the ENP-30 to assert CBRQ* (factory configuration).
- A jumper between pins 2 – 11 allows the ENP-30 to see CBRQ* always asserted.
- A jumper between pins 4 – 9 allows the ENP-30 to drive BCLK* for system controller applications.
- A jumper between pins 5 – 8 configures the ENP-30 for parallel arbitration (factory configuration).
- If a jumper is used between pins 5 – 8, there should be no jumper placed between pins 6 – 7.

- A jumper between pins 6 – 7 configures the ENP-30 for serial arbitration.

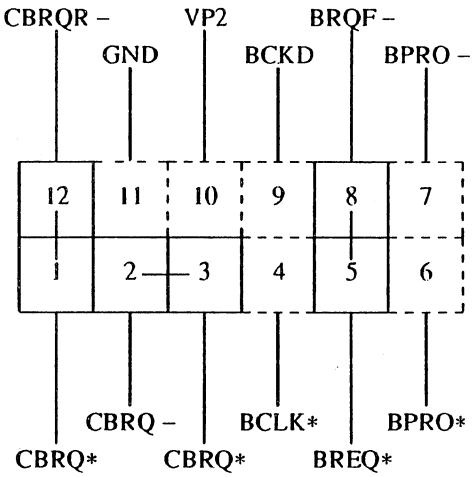
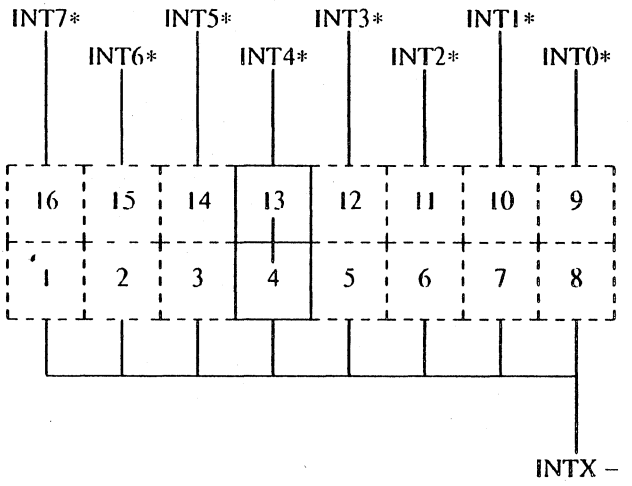


Figure 4-10. MULTIBUS Master and Acquisition Control Options (JP09)

4.2.3.9 MULTIBUS Interrupt Level Select (JP10)

This jumper selects the interrupt level, from 0 to 7, of MULTIBUS Non-Bus Vectored Interrupts (NBVI) generated by the ENP-30. Only one interrupt level may be selected, so only one jumper should be installed. Level 4 is shown below.



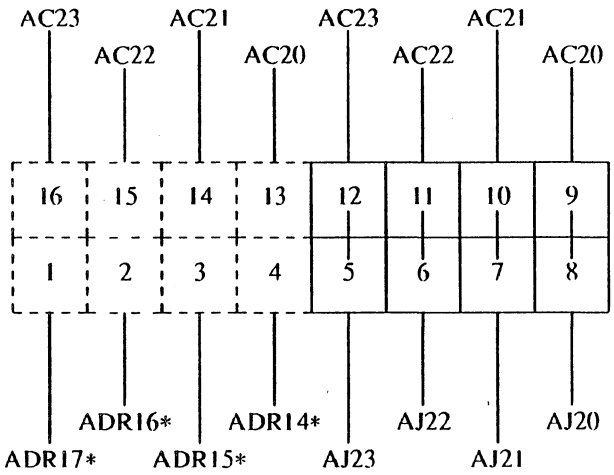
Note: Level 4 is shown.

Figure 4-11. MULTIBUS Interrupt Level Select (JP10)

4.2.3.10 MULTIBUS Address Path Width Select (JP11)

For a 24-bit address bus, jumpers on pins 1 – 16, 2 – 15, 3 – 14, and 4 – 13 must be installed.

For a 20-bit address bus, jumpers on pins 5 – 12, 6 – 11, 7 – 10, and 8 – 9 are installed.



20-bit addressing is shown.

Figure 4-12. MULTIBUS Address Path (Width Select JP11)

4.3 Installation Instructions

This section includes instructions for installing the Ethernet coaxial cable, transceiver installation, transceiver removal/relocation, and installing the ENP.

4.3.1 Installing the Ethernet Cable

The following are general instructions for installing an Ethernet cable on site. Specific tools needed are:

Ethernet cable
barrel connectors to join sections of cable
2 terminators
1 cable ground clamp
1 ground wire of appropriate length (AWG rating 2 – 8, insulated)
wire strippers
electrical tape

1. Plan the network layout and locations of node taps on the Ethernet cable. Proper preparation in this area is necessary for a successful installation. See *The Ethernet*, Version 2.0, November 1982, for acceptable network layouts.

Note

The distance between node taps on the Ethernet cable must be an integral multiple of 2-1/2 meters (8.2 feet). For handy reference, the bulk cable is marked with a heavy black bar each 2 1/2 meters.

2. Build your cable, using barrel connectors as necessary. Each of the cable sections is terminated by a male terminator. Remove the terminator cap to accept the barrel connector. You can join two sections of cable using a barrel connector.

Note

Total cable length may not exceed 500 meters (1640 feet).

3. Each free end of the cable must be capped with a terminator.
4. Route the cable, per your network design.
5. Ground the cable. THE CABLE MAY BE GROUNDED AT ONLY ONE POINT. One of the terminators is an easily accessible grounding point. Terminate the ground at any existing ground termination point, or at a separately driven ground rod. Clamp a cable ground clamp around the connector you have chosen as the ground origin. Be careful not to overtighten the screws securing the clamp, or damage to the connector may result.
6. Cut the ground wire to the appropriate length. Strip the insulation from 1/2-inch of each end of the ground wire; insert one end into the receptacle in the ground clamp. Tighten the screw holding the ground wire in place. Attach the free end of the ground wire to the ground termination point.
7. Wrap all connector junctions and terminators with electrical tape to insulate them.

4.3.2 Transceiver Installation

Attaching the transceiver(s) is the second phase of network installation. Specific manufacturer's installation instructions are packaged with each individual transceiver. Some brands of transceivers require special tools for installation. For transceivers supplied by CMC, any required special installation tools may be obtained from CMC. Observe the following transceiver installation considerations and precautions:

1. Do not install the transceiver tap block where it can touch grounded objects (conduit, piping, etc.).

2. Ensure that no shielding material fragments remain in the Ethernet cable tap hole. Such fragments could short the coaxial cable when the transceiver is installed and disable the network.

3. Securely connect the transceiver cable to the transceiver with the slide lock.

4. Position and secure the Ethernet cable and transceiver per the network layout plan. Ensure that the transceiver cable is strain relieved.

4.3.3 Transceiver Removal/Relocation

When removing or relocating transceivers, be sure to follow the transceiver manufacturer's instructions, precisely. Otherwise, ENP or Ethernet performance may be impaired.

4.3.4 ENP Installation

The following are general instructions for installing the ENP-30 in the user's system PC board rack. Refer to the applicable user's system instructions for specific procedures relating to the host system.

1. Power down the host system.

2. Remove any of the covers necessary to provide access to the backplane.

3. Slide the ENP PCB into the proper slot on the chassis. Make sure it is properly seated in the slot and to the connectors on the MULTIBUS backplane.

4. Power up the host system and verify that the ENP green *run* LED indicator light illuminates and that the host system is operating.

5. Boot the host system and verify that it can address the MULTIBUS.

6. Perform a memory test on the ENP by writing to ENP memory using ENP Debugger. Review the data. If the data is not being

stored or refreshed, examine the ENP connection to the bus, emulator, and power supply.

Upon power up, the ENP performs a series of self-diagnostic tests, that take about 3 to 12 seconds. Upon successful completion of these tests, the green *run* LED illuminates. If the green *run* LED does not illuminate, check the electrical connections between the ENP and the MULTIBUS.

If unable to identify the reason for a diagnostic test failure, contact CMC Technical Support at (805) 564-3355.

Section 5

Operations Procedure

5.1 Introduction

This section provides an overview of hardware operation, including initialization and diagnostic operation. A programming guide is included also, in the event that communications protocol software development is needed.

5.2 Initialization Procedure

Upon power up or system reset, the ENP-30 will execute a series of ROM-based tests to verify proper function of the PC board. The red *fail* LED illuminates while the tests are in progress.

Upon successful completion of the tests, the red *fail* LED is turned off and the green *run* LED illuminates. These tests include a LANCE register and loopback test, an MPU test, a memory test for the 128KB DRAM, and a control and status register test.

5.3 Diagnostic Description

A description of the diagnostic routines included in the power up self test are provided in the Appendices.

5.4 Programming Guide

For standard implementations of the ENP, the user can ignore this section, since the necessary programming is included in the K1 Kernel firmware and the selected CMC higher level protocol software. For non-standard implementations, the ENP can be custom programmed through specific control and status registers.

Programming the ENP requires an understanding of the MPU and how it interacts with the rest of the elements in a system of processors in a

MULTIBUS backplane. As a microprocessor, the ENP-30 has an array of on-board resources and MULTIBUS resources which respond according to the ENP Memory Map (Figure 6-4). These resources are the MPU, DRAM, PROM, the LANCE, the DUART, local control status registers, and the MULTIBUS interface, as shown in Figure 3-1.

The ENP-30 as a MULTIBUS device can perform as a master or interrupter, or respond as a slave. As a master, MPU access to the MULTIBUS window causes master operations on the MULTIBUS. As a slave, the ENP-30 responds as MULTIBUS memory with a selectable address base which maps to ENP-30 DRAM and local I/O space (Figure 6-4).

Note

Address numbers are expressed throughout this manual with a $ prefix, indicating hexadecimal format.

5.4.1 The Microprocessor Unit

The Microprocessor Unit (MPU) (see MC68000 or MC68010 Specification) runs at a 10MHz clock rate and is the default master of the ENP internal bus. Other potential masters are the LANCE or any MULTIBUS master accessing the slave access window of the ENP. Arbitration of the internal bus is via the MPU BR, BG, and BGACK controls. The MPU (along with all other ENP resources) is reset by a bus reset (INIT*), an external reset switch closure, or by setting a bit (bit 0 at $FFF001). The MPU can also issue a reset to ENP internal resources via the reset instruction.

System address decoding, with the exception of DRAM and PROM, is non-unique. The basic address decode granularity is modulo 32K. Data types are not differentiated with system decode; there is no difference between supervisory and user mode or between data and program modes.

Interrupts to the MPU are all autovectored. All seven levels are supported and used.

MPU bus error and halt lines are used to resolve deadlocks with other bus masters attempting to access the ENP or to trap the MPU if a resource does not return a DTACK within the 8µs resource time-out period.

5.4.2 Dynamic Memory

The 128KB ENP has dynamic random access memory (DRAM) consisting of eighteen 64K x 1 bit, 4164-type devices with 150ns access time. The 512KB version has eighteen 256K x 1 bit 4256-type devices with 120ns access time. DRAM responds at $F00000 – $F20000 ($F80000 for 512KB version) after a reset and at $F01000 – $F20000 ($F80000 for 512KB version) and $0 – $1000 after the MAPS bit (bit 1 at $FFF01) is set. This allows PROM to provide the start up vector after a reset. The DRAM causes no MPU wait states on reads or writes. (ENP-30 Rev. A has one wait state on writes.)

Byte parity is generated on writes to the memory and checked on reads. A parity error causes a Level 7 autovectored interrupt to the MPU. A parity error during host or LANCE access to the DRAM results in non-acknowledgment and a host or LANCE time-out. Parity errors are flagged in the LOCK register (bit 3 at $FFF061).

The DRAM must be refreshed by a software routine, since there is no hardware-supported refresh. A refresh timer causes a Level 7 autovector interrupt to occur about every 1.6384ms. The refresh routine must refresh alternate halves of DRAM by accessing 128 sequential words, starting at a location *n* or *n* + $100 on alternate interrupts.

DRAM must be initialized by reading after power up or reset, checked for proper parity, and written if necessary. The K1 Kernel and Debugger provide refresh and start up initialization for the DRAM and set the MAPS bit, which causes the swapping of memory address space from PROM to DRAM.

5.4.3 PROM

The ENP PROM responds at locations $0 – $1000 and $F81000 – $F90000 after a reset. After the MAPS bit is set, DRAM from $F00000 replaces the 4KB PROM segment at $0 – $1000, and that segment of PROM will then respond at $F80000 – $F81000. This mechanism provides PROM at the MPU reset vector. PROM is organized as words, with the upper byte in position U44 and the lower byte in position U28. A DTACK response jumper allows use of PROMs with access times of up to 500ns but fast PROMs (access time < 200ns) and no wait state jumpering provide the best performance.[2]

PROM pin-out selection jumpering allows PROMs from various manufacturers to be used, but the factory configuration is set for AMD Am2764-2 or Am27128-2, or equivalent parts. PROM response will be non-unique modulo the PROM size in words. Thus, for 8K bit x 8 PROMs, identical data is read at $F80000, $F84000, $F88000, ... $F9C000.

5.4.4 The LANCE

The LANCE (Am7990) and its companion device, the SIA (Am7991/7992), provide the link and physical layer interface to Ethernet. The details of LANCE programming and usage appear in the AMD Am7990 specification. The following details assume an understanding of the LANCE programming specification.

The LANCE is programmed by the MPU as a slave type device. Control is accomplished through the four LANCE CSRs, accessible as words only through the Data Buffer Register (DBR at $FFF200) and indexed by the Address Register (ADR at $FFF202).

In order to insure proper LANCE operation, some rules must be followed. First, the LANCE must not be given buffer or control

2. The ENP-30 Rev. A has no option jumpers for wait state selection. Factory setting is one wait state.

structure addresses outside ENP on-board memory space. Second, the bus interface characteristics, as selected by CSR3, must be set for the ENP/LANCE interface: CSR3 = $4. LANCE interrupts occur on autovector Level 6.

The primary function of the K1 Kernel is control of the LANCE for a friendly software interface. Because of its complex behavior, the LANCE should be programmed through the K1 Kernel.

5.4.5 MULTIBUS Interface

The ENP/MULTIBUS interface is a dual-purpose, master/slave interface. Master access is initiated by the MPU. Slave access can be made to ENP internal DRAM by other masters on the MULTIBUS.

5.4.5.1 MULTIBUS Master Access by the ENP

The ENP can access the MULTIBUS as a master as if the MULTIBUS were memory or I/O space by accessing the appropriate address ranges in MPU address space (Figure 6-4). MPU addresses $001000 – $EF0000 are mapped directly to MULTIBUS memory space. Since either 20-bit or 24-bit address MULTIBUS options are allowed, accesses above $100000 access duplicate 1MB spaces modulo $100000 on a 20-bit address MULTIBUS. MPU addresses $EF0000 – $F00000 map to the 64KB MULTIBUS I/O space. (A23 – A16 are driven, but not decoded, by I/O devices.)

The MULTIBUS is acquired by the bus exchange logic at the beginning and released at the end of each cycle (earlier versions of the ENP-30 Rev. A maintain control of the MULTIBUS until CBRQ is asserted). The resource time-out timer will not be started until the MULTIBUS is acquired during an MPU master access. For this reason, it is required that the acquisition of the MULTIBUS not take more than 200µs worst case or ENP operation may be adversely affected by the loss of DRAM contents. Best performance requires less than 2µs average acquisition time.

5.4.5.2 MULTIBUS Slave Access to ENP

Note

The information in this section is extremely important for writing programs.

Slave access to the ENP results in arbitration and acquisition of the ENP internal bus. The usual wait for acquisition is less than 0.6µs with a resulting cycle time of 1.1µs when accessing DRAM through the window. When the LANCE is doing DMA, slave access to the ENP can result in acquisition waits of up to 9µs with cycle times (XACK response) of 9µs.

As a slave, the ENP responds as MULTIBUS memory at a jumper-selectable, modulo 128KB address (Figure 6-4) on 20- or 24-bit address bus options (see Section 4.3.2.7, 4.3.2.8). Addresses from the host are mapped to MPU internal addresses by field substitution of the most significant address bits.

The segment between window addresses $XX1000 and $X[xxx1]E000 is accessed by substituting MULTIBUS address bits 23 – 17 (AD17 – AD10) with a constant 1111000 (binary), which maps the access into MPU addresses $F01000 – $F1E000. The segment between window addresses $X[xxx1]E000 and $X[xxx1]F000 is accessed by substitution of A23 – A20 with a constant 1111 (binary) and substitution of A19 – A12 with the contents of a page register (BPR at $FFF041). This allows the resulting 4KB page address to fall between $F00000 and $F80000. The segment between $X[xxx1]F000 and $X[xxx1]FFFF = 1 is accessed by substitution of A23 – A17 with a constant, 111 1111 1111 (binary), mapping the address to $FFF000 – $FFFFFF, which is the local I/O space of the ENP.

The host processor (or any other master) should not execute code resident in ENP slave-accessible DRAM, since this would use a large amount of available ENP internal bus bandwidth. Such a use of ENP DRAM would severely limit its performance and may result in insufficient MPU time for such essential tasks as DRAM refresh.

5.4.5.3 MULTIBUS Byte Order Control

Because the MPU byte order and byte access mechanism is different from the MULTIBUS, byte swapping and routing is provided in the ENP-30 to MULTIBUS data path. Byte order within words on the MPU (even-odd = high-low) is opposite the MULTIBUS (even-odd = low-high). All byte accesses are routed on the least significant byte path on the MULTIBUS, while the MPU routes even bytes on the most significant path and odd bytes on the least significant path.

Byte swapping within words can be selected for full word read or write on master or slave accesses with four separate control bits in local I/O space. These four control bits are:

1. Host read.
2. Host write.
3. MPU read.
4. MPU write.

Byte routing on byte accesses (master or slave) is positionally normalized to MULTIBUS byte order within words and is not selectable (the even byte on the MULTIBUS is the odd byte to the MPU). The routing/swapping logic data path flow is illustrated in Figure 5-1.

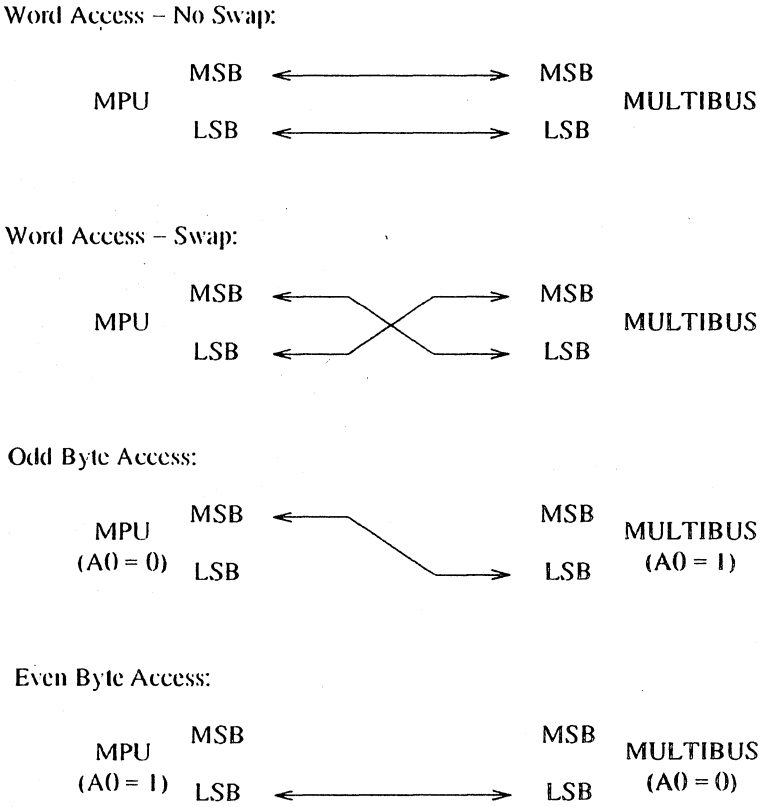


Figure 5-1. Routing/Swapping Logic Path

5.4.6 Programmable Registers

The programmable registers provide status and control functions for various features of the ENP. Although these registers are available for access to MULTIBUS masters, in general the ENP MPU controls their use.

To access the programmable registers from the MULTIBUS, the following algorithm is used to compute the register address: if $YY represents the least significant two hex digits of the register address given in the description and $XX0000 is the MULTIBUS window address of the ENP, the register address is computed by adding $XX0000, $1F000, and ($YY–1).

For example, to access from the MULTIBUS the Bus Interrupt Register (address $FFF027) on an ENP whose MULTIBUS window address is $1C0000, the MULTIBUS address is $1DF026 ($1C0000+$1F000+$26).

Note that the access address calculation above assumes that a byte access is performed. Note also that most MPUs follow the byte access rules outlined in section 5.4.5.3 above. Therefore, to access MULTIBUS address $1DF026 from a MC68000 or MC68010 MPU, address $1DF027 would be used. These rules may or may not apply to the processor in use, so consult the system-level documentation, regarding the processor-to-MULTIBUS address translation scheme used for byte accesses.

5.4.6.1 MPU Control/Status Register

The MPU Control/Status Register (MPUCSR) contains control and status bits relevant to the MPU and its activities.

MPUCSR:$FFF001

Table 5-1. MPU Control/Status Register

7	6	5	4	3	2	1	0
RTO	ALIVE	RRUN	IEN	MWSW	MRSW	MAPS	MRST
RW	W	RW	RW	RW	RW	RW	W

Bit	Name	RW	Function
7	RTO	R	**Resource Time Out**. Set if MPU accesses an address which does not reply with DTACK for longer than 8µs. A resource time-out condition will cause a bus error trap to occur. Cleared/set by MPU.
6	ALIVE	W	**System Alive**. Writing this bit with a 1 re-triggers a timer which drives the ALIVE indicator light. The time out value is about 10ms. ALIVE reads as 0.
5	RRUN	RW	**Rerun**. Indicates that a MULTIBUS access cycle was aborted and rerun by the MPU. Cleared by reset. Cleared/set by MPU.
4	IEN	RW	**Interrupt Enable**. When set allows interrupt to the MPU. When cleared, disables all interrupts to the MPU (including software refresh). Cleared by the MPU reset. Cleared/set by MPU.

Bit	Name	RW	Function
3	MWSW	RW	**MPU Write Swap.** This control bit determines what byte order is used during MPU word write accesses to the MULTIBUS. If MWSW=0, bytes are not swapped for word writes. If MWSW=1, MPU to MULTIBUS word writes are byte swapped. The order of MULTIBUS byte writes are not affected by MWSW. Cleared by reset. Cleared/set by MPU.
2	MRSW	RW	**MPU Read Swap.** This control bit controls the swapping of bytes during word reads of MULTIBUS data by the MPU (see MWSW). The order of MULTIBUS byte reads are not affected by MRSW. Cleared by reset. Cleared/set by MPU.
1	MAPS	RW	**Map Swap.** When MAPS=1, the RAM located at $F00000–$F01000 is relocated to $000000–$001000 and the PROM located at $000000–$001000 is relocated to $F80000–$F81000 (see Memory Map, Figure 6-4). Cleared by reset. Set/cleared by current MPU bus master.
0	MRST	W	**MPU Reset.** Writing a 1 in this position resets the MPU and the LANCE. Reads as a 0.

5.4.6.2 MULTIBUS Lock Control Register

LOCKR:$FFF061

Table 5-2. MULTIBUS Lock Control Register

7	6	5	4	3	2	1	0
UNUSED				MPAR RW	ABORT RW	REFT/ PUP W	LOCK W

Bit	Name	RW	Function
7-4			Unused.
3	MPAR	R	**Memory Parity error.** When clear, indicates a parity error in reading DRAM. Causes Level 7 autovectored interrupt. Set by reset. Cleared/set by MPU.
2	ABORT	RW	**Abort.** Indicates the external abort control line was pulled. Causes a Level 7 autovectored interrupt. Cleared by reset. Cleared/set by MPU.
1	REFT	W	**Refresh Time-out trigger.** Writing a 1 to this position retriggers the DRAM refresh timer. A time-out causes a Level 7 autovectored interrupt. Reading a 1 at this bit position indicates a power up just occurred. Any LOCKR write will clear the power up flag.

Bit	Name	RW	Function
0	LOCK	W	**MULTIBUS Lock.** When written with a 1, this bit causes the MULTIBUS to be held after the next bus acquisition until a subsequent bus cycle has ended. The MULTIBUS LOCK is asserted during this time. Do not use this control bit with any MPU instruction other than TAS. (Not on EN-30, Rev. A.)

5.4.6.3 DUART Registers

The SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) registers are detailed in the Signetics device specification. The DUART is programmed by the K1 Kernel to pulse a CINT signal, which causes a level 5 autovectored interrupt for ENP timer functions. These registers are located at $FFF081 through $FFF09F at the odd byte addresses (see Appendices).

Table 5-3. DUART Registers

Address	Read	Write
$FFF081	Mode Register A (MR1A,MR2A)	Mode Register A (MR1A,MR2A)
$FFF083	Status Register A (SRA)	Clock Select Reg. A (CSRA
$FFF085	*Reserved*	Command Register A (CRA)
$FFF087	RX Holding Register A (RHRA)	TX Holding Register A (THRA)
$FFF089	Input Port Change Reg. (IPCR)	Aux. Control Register (ACR)
$FFF08B	Interrupt Status Reg. (ISR)	Interrupt Mask Reg. (IMR)
$FFF08D	Counter/Timer Upper (CTU)	C/T Upper Register (CTUR)
$FFF08F	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
$FFF091	Mode Register B (MR1B,MR2B)	Mode Register V (MR1B,MR2B)
$FFF093	Status Register B (SRB)	Clock Select Reg. B (CSRB)
$FFF095	*Reserved*	Command Register B (CRB)
$FFF097	RX Holding Register B (RHRB)	TX Holding Register B (THRB)
$FFF099	Interrupt Vector Reg. (IVR)	Interrupt Vector Reg. (IVR)
$FFF09B	Input Port	Output Port Conf. Reg. (OPCR)
$FFF09D	Start Counter Command	Set Output Port Bits Command
$FFF09F	Stop Counter Command	Reset Output Port Bits Command

5.4.6.4 Window Setting Register

Reading the Window Setting Register (WINDR) reflects the state of the MULTIBUS Modulo 128KB window decoder jumpers JP08, which determine the ADR17:14* and ADR13:10* response address selection.

WINDR:$FFF0C1

7	6	5	4	3	2	1	0
W7	W6	W5	W4	W3	W2	W1	–
R	R	R	R	R	R	R	(0)

5.4.6.5 Single-Bit Registers

These read/write registers have only one valid bit in position 7. All other positions are undefined. They can be cleared/set by the MPU or current MPU bus master and are cleared by reset.

5.4.6.5.1 Bus Interrupt Register

The Bus Interrupt Register (BIR at $FFF027) is a single-bit (bit 7) register which causes assertion of the MULTIBUS interrupt request level selected by JP10. This is a Non-Bus-Vectored Interrupt (NBVI) to the host. This bit can be set or cleared by the MPU or the host, but it is generally set by the MPU to signal the host and cleared by the host interrupt service routine. The BIR is cleared by reset. The BIR responds at MPU addresses $FFF027 or $FFF037.

5.4.6.5.2 Receive Interrupt Register

The Receive Interrupt Register (RIR at $FFF029) is a single-bit register (bit 7) which causes a Level 4 autovectored interrupt request to the ENP-30 interrupt logic. The Level 4 request remains active until the

bit is cleared by the MPU or a reset occurs. The RIR can be set or cleared by the MPU or host. The RIR responds at MPU addresses $FFF029 and $FFF039.

5.4.6.5.3 Utility Interrupt Register

The Utility Interrupt Register (UIR at $FFF021) is a single-bit register (bit 7) which causes a Level 1 autovectored interrupt request to the interrupt logic. The Level 1 remains active until the bit is cleared by the MPU or host, or a reset occurs. The UIR responds at MPU addresses $FFF021 or $FFF031.

5.4.6.5.4 Slave Write Swap Register

The Slave Write Swap Register (SWSR at $FFF023) is a single-bit register (bit 7) which controls whether bytes are swapped (bit = 1) or unswapped (bit = 0) when the host makes word-write accesses to ENP-30 RAM. This bit can be set or cleared by the MPU or host, since it does not affect the data path logic until the end of the current cycle. The SWSR is cleared by reset. The SWSR responds to MPU addresses $FFF023 or $FFF033.

5.4.6.5.5 Slave Read Swap Register

The Slave Read Swap Register (SRSR at $FFF025) is a single-bit register (bit 7) which controls whether bytes are swapped (bit = 1) or unswapped (bit = 0) when the host makes word-read accesses to ENP DRAM. This bit can be set or cleared by by the MPU host. The SRSR is cleared by reset. The SRSR responds to MPU addresses $FFF025 or $FFF035.

5.4.6.5.6 Transmit Interrupt Register

The Transmit Interrupt Register (TIR at $FFF02B) is a single-bit (bit 7) register, which causes a level 3 autovectored interrupt request to the ENP interrupt logic. The level 3 request remains active until the bit is cleared by the MPU or a reset occurs. The TIR can be set or cleared by

the MPU or host. This register is generally used by the host to request an interrupt to the ENP. The TIR responds at MPU addresses $FFF02B or $FFF03B.

5.4.6.5.7 Extra Interrupt Register

The Extra Interrupt Register (XIR at $FFF02D) is a single-bit (bit 7) register which causes a Level 2 autovectored interrupt request to the ENP-30 interrupt logic. The Level 2 request remains active until the bus is cleared by the MPU or a reset occurs. The XIR can be set or cleared by the MPU or the host. This register is generally used by the host to request an interrupt to the ENP. The XIR responds to MPU addresses $FFF02D or $FFF03D.

5.4.6.6 Bus Page Register

The Bus Page Register (BPR) is an 8-bit, write only register. The value in this register is substituted for MPU bus address lines 19 – 12 when the MULTIBUS accesses the ENP in the 4KB paged-access window at $X[xxxx1]E000. See the Memory Map (Figure 6-4) for details. Also see section 5.4.5.

BPR:$FFF041

7	6	5	4	3	2	1	0
PA19	PA18	PA17	PA16	PA15	PA14	PA13	PA12
W	W	W	W	W	W	W	W

Section 6

Support Information

6.1 Introduction

This section provides interface connector information and supporting illustrations and diagrams for the ENP-30.

6.2 MULTIBUS Pin Assignments

The ENP is inserted directly into the MULTIBUS P1 and P2 backplane sockets. The P1 connector signals are identified in Table 6-1 by pin number, signal mnemonic, and signal name and description. Table 6-2 identifies the P2 connector signals.

Table 6-1. Connector P1 MULTIBUS Pin Assignments

Pin Number	Signal Mnemonic	Signal Name and Description
1, 2, 11, 12, 75, 76, 85, 86	GND	**Signal GND**
3-6, 81–84	+5V	+5Vdc power used by the ENP
7, 8	+12V	+12Vdc power used by LANCE devices
9, 10, 77, 78	NA	
13	BCLK*	**Bus Clock.** Used to synchronize the bus contention logic on all bus masters.
14	INIT*	**Initialize.** Reset the entire system to a known internal state.

Pin Number	Signal Mnemonic	Signal Name and Description
15	BPRN*	**Bus Priority In.** When low indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN* is synchronized with BCLK*.
16	BPRO*	**Bus Priority Out.** In serial (daisy chain) priority resolution schemes, BPRO* must be connected to the BPRN* input of the bus master with the next lower bus priority.
17	BUSY*	**Bus Busy.** Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus for one or more data transfers. BREQ* is synchronized with BCLK*.
18	BREQ*	**Bus Request.** In parallel priority resolution schemes, BREQ* indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ* is synchronized with BCLK*.
19	MRDC*	**Memory Read Command.** Indicates that the address of a memory location is on the MULTIBUS address lines and that the contents of that location are to be read (placed) on the MULTIBUS data lines.
20	MWTC*	**Memory Write Command.** Indicates that the address of a memory location is on the MULTIBUS address lines and that the contents on the MULTIBUS data lines are to be written into that location.
21	IORC*	**I/O Read Command.** Indicates that the address of an I/O port is on the MULTIBUS address lines and that the output of that port is to be read (placed) onto the MULTIBUS data lines.

Pin Number	Signal Mnemonic	Signal Name and Description
22	IOWC*	**I/O Write Command.** Indicates that the address of an I/O port is on the MULTIBUS address lines and that the contents on the MULTIBUS data lines are to be accepted by the addressed port.
23	XACK*	**Transfer Acknowledge.** Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the MULTIBUS data lines.
24	INH1*	**Inhibit RAM.** For system applications, allows ISBC dual port RAM addresses to be overlayed by ROM/PROM or memory mapped I/O devices. This signal has no effect on local CPU access of its dual port RAM.
25	LOCK*	**Lock.** Indicates a locked access is being performed on the MULTIBUS.
26	INH2*	**Inhibit ROM.** For system applications, allows ROM/PROM addresses to be overlayed by auxiliary ROM devices (e.g., a bootstrap program).
27	BHEN*	**Byte High Enable.** When active low, enables the odd byte bank (DAT8*–DATF*) onto the MULTIBUS.

Pin Number	Signal Mnemonic	Signal Name and Description
28 30 32 34 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58	AD10* AD11* AD12* AD13* ADRE* ADRF* ADRC* ADRD* ADRA* ADRB* ADR8* ADR9* ADR6* ADR7* ADR4* ADR5* ADR2* ADR3* ADR0* ADR1*	**Address.** These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0* (when active) enables the even byte bank (DAT0*–DAT7*) on the MULTIBUS; i.e., ADR0* is active all even addresses. ADR13* is the significant address bit for 20-bit addressing.
35 36 37 38 39 40 41 42	INT6* INT7* INT4* INT5* INT2* INT3* INT0* INT1*	**Interrupt.** These lines are the interrupt lines for MULTIBUS interrupt levels 0–7. When the ENP wishes to generate a MULTIBUS interrupt, one of these lines is asserted as selected by jumper JP10.

Pin Number	Signal Mnemonic	Signal Name and Description
59	DATE*	**Data.** These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF* is the most significant bit. For data byte operations, DAT0*–DAT7* is the even byte, DAT8*–DATF* is the odd byte.
60	DATF*	
61	DATC*	
62	DATD*	
63	DATA*	
64	DATB*	
65	DAT8*	
66	DAT9*	
67	DAT6*	
68	DAT7*	
69	DAT4*	
70	DAT5*	
71	DAT2*	
72	DAT3*	
73	DAT0*	
74	DAT1*	

*Notes:

1. All signal directions are with respect to the ENP-30.
2. The bus master is the device on the MULTIBUS that is in control of the transaction at the present time.
3. NA denotes signal pins not applicable to the ENP.

Table 6-2. Connector P2 MULTIBUS Pin Assignments

Pin Number	Signal Mnemonic	Signal Name and Description
1 – 4	NA	
55	AD16*	**Address.** These 4 lines are the 4 most significant address bits in 24-bit addressing.
56	AD17*	
57	AD14*	
58	AD15*	

The notes for Table 6-1 also apply to Table 6-2.

6.3 Transceiver Cable Pin Assignment

By specification, the ENP has a 15-pin female transceiver connector (MIL-C-24308 or commercial equal) with a connector slide latch assembly. The connector pin identification is shown in Table 6-3.

Table 6-3. Transceiver Pin Assignments (J3)

Pin Number	Signal Name
1	Shield (Ethernet 1.0, 2.0) (Ground)
2	Collision Presence +
3	Transmit +
4	Ground
5	Receive +
6	Power Return (Ground)
7	Reserved
8	Ground
9	Collision Presence –
10	Transmit –
11	Reserve –
12	Receive –
13	Power (+12Vdc Fused)
14	Ground
15	Reserved

Note

Cable shield must be terminated to connector shell and to Pin 1. Do not connect shield to any other pin. No connections are allowed on reserved pins.

6.4 RS-232 Serial Communications Pin Assignment

The ENP-30 has two full duplex asynchronous serial communication ports (ENP-30, Rev. B) with modem controls. These ports are accessed through two 26-pin, dual-in-line flat cable connectors at the top edge of the ENP-30 PC board. Port A (J5) is configured DTE for connection to a terminal. Port B (J4) is configured DCE. The pin identifications for these connectors are shown in Tables 6-4 and 6-5. Figure 6-3 shows the geometric arrangement of pins in the connectors.

Extender cables (Figure 6-2) are available for ENP-30 connectors J4 and J5 to provide true RS-232 interfaces at the host system connector panel. When mating an extender cable connector with either J4 or J5, use care to ensure that the connector markers designating pin 1 are in alignment.

Table 6-4. J5 Pin Assignment

Pin Number	Signal Name
1	GND
3	RXDA
5	TXDA
7	RTSA
9	CTSA
13	GND

Table 6-5. J4 Pin Assignment

Pin Number	Signal Name
1	GND
3	TXDB
5	RXDB
9	CTSB
13	GND
15	DCDB

6.5 Reset Box Connector Pin Assignments

A Reset and Software Abort Control Box (available from CMC or may user fabricated) can be connected to the ENP-30 for debugger operation and program development. The CMC Reset box includes a connector for mating with ENP-30 jumper block, JP02 (see section 4.3.2.2). The pin identification for JP02 is shown in Figure 4-3 and Table 6-6.

Table 6-6. Reset Box Connector Pin Assignment

Pin Number	Signal Name
1	GND
2	XRES–
3	GND
4	XRESR–
5	GND
6	VCC
7	GND
8	HALT–
9	GND
10	XABORT–

6.6 Associated Cable for Transceiver Connection

The cable required for the transceiver connection is comprised of two connectors and a cable length as follows:

1. 1 Male, 15-Pin, Subminiature, D-Type (MIL-C-24308 or equivalent) connector, with locking posts.
2. 1 Female, 15-Pin, Subminiature D-type (MIL-C-24308 or equivalent) connector, with a slide latch assembly.
3. 1 Standard Transceiver Cable with four stranded, shielded, twisted-pair conductors, plus an overall shield and insulating jacket.

Maximum length is 50 meters (approximately 164 feet).

6.7 Supporting Drawings

The supporting drawings and diagrams are included following pages:

Figure 6-1. ENP-30 Block Structure

Figure 6-2. RS-232 Cable Assembly Drawing

Figure 6-3. RS-232 Connections

Figure 6-4. ENP-30 Memory Map

Figure 6-5. Local I/O Map Detail

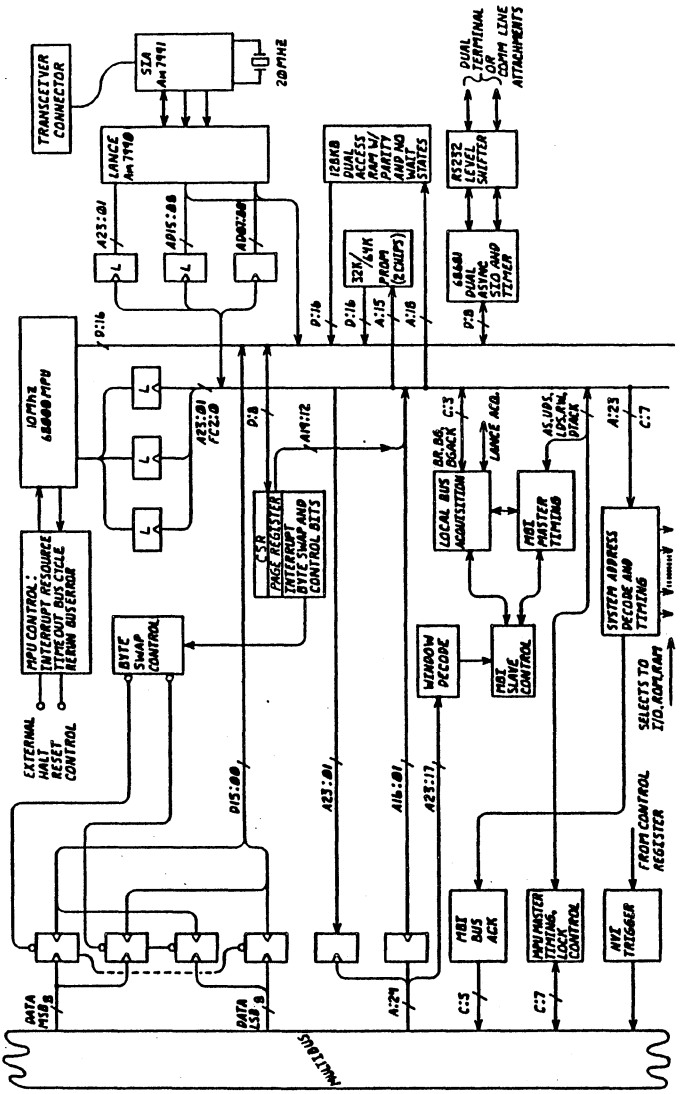


Figure 6-1. ENP-30 Block Structure

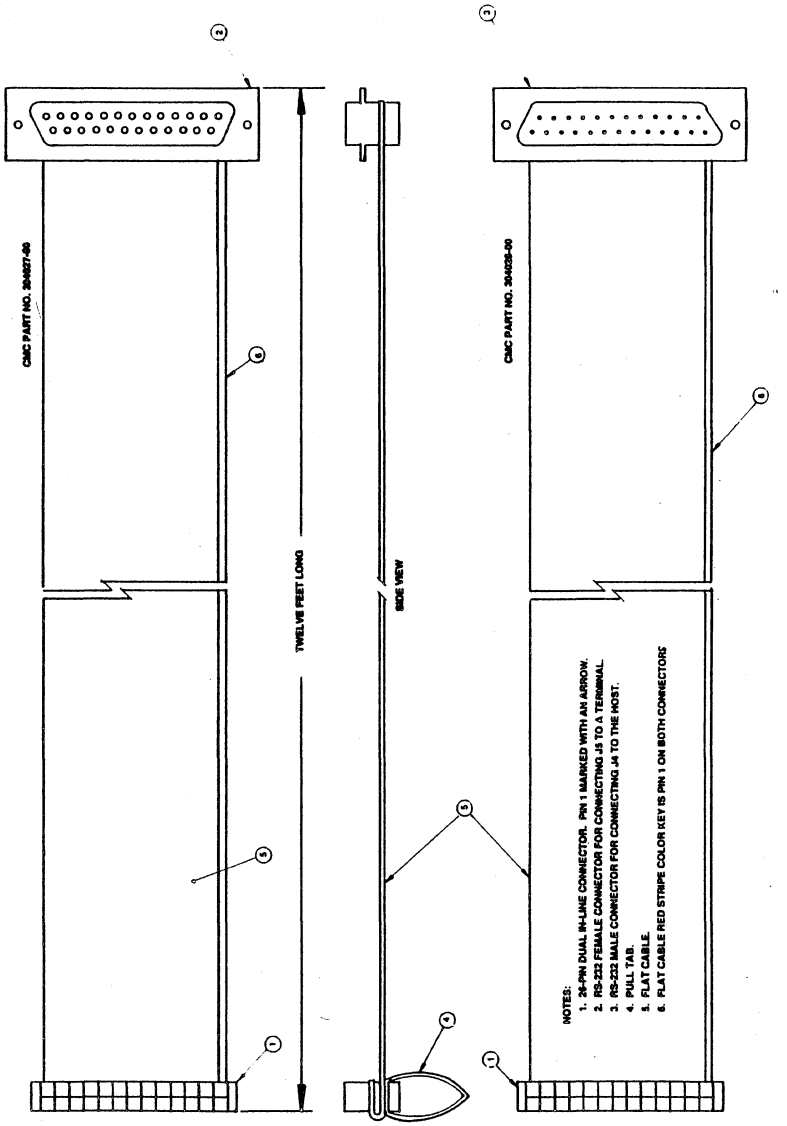
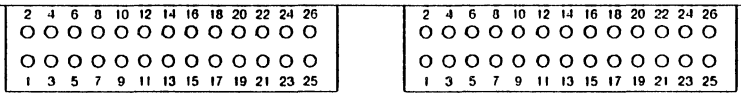


Figure 6-2. RS-232 Cable Assembly Drawing

VIEW FROM TOP EDGE OF PC BOARD



J5:DTE (Port A) Terminal J4:DCE (Port B) Host

NOTE: PC board connectors J4 and J5 for the serial ports are 26-pin, dual in-line receptacles for mating flat cable connectors. The above view provides connector and pin number locations. Pin 1 is marked with an arrow marker on the connector body and should always be matched with the arrow marker on the mating connector. Tables 6-4 and 6-5 provide signal identification for each serial port.

Figure 6-3. Serial Communication Ports

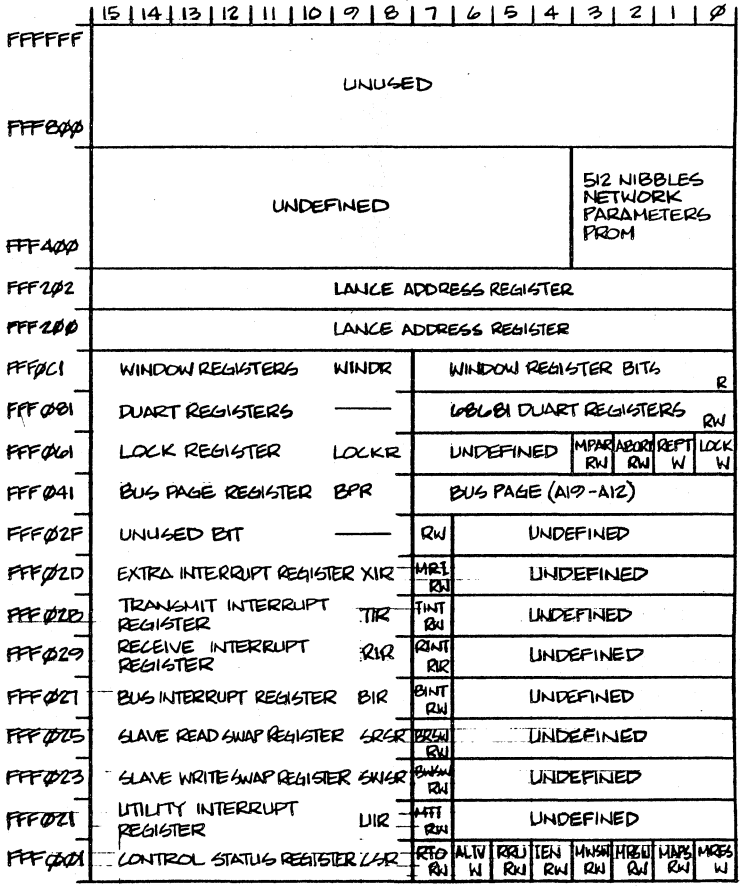


Figure 6-4. ENP-30 Memory Map

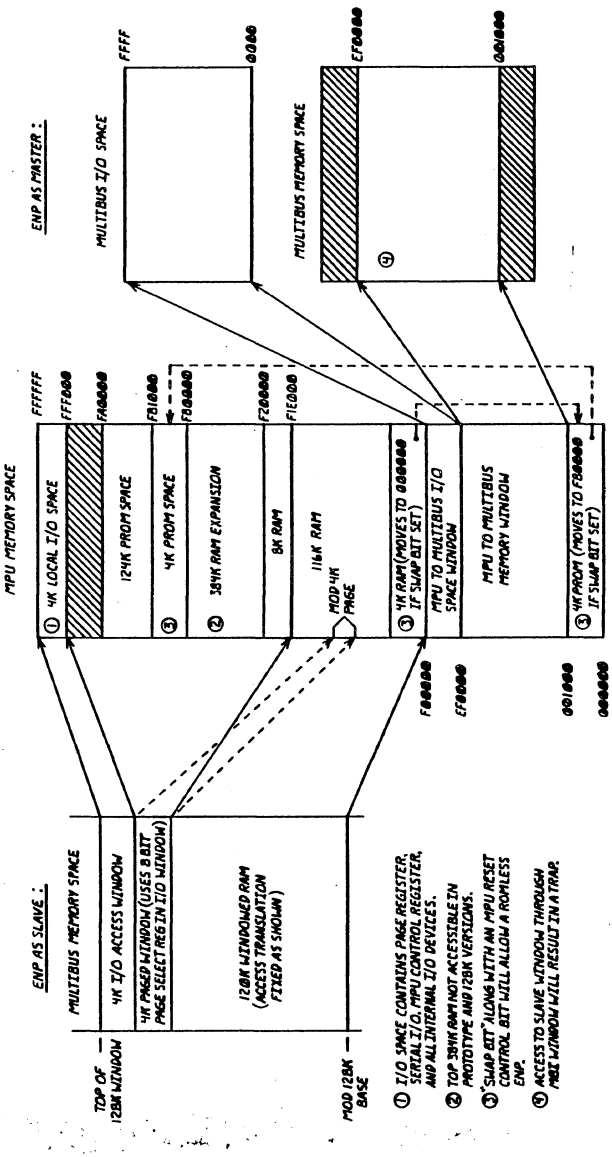


Figure 6-5. Local I/O Map Detail

Section 7

Debugger Installation

Included with the CMC Software Development Kit for the ENP-30 Series board are two debugger ROMs, a Reset Box, and cabling.

- The debugger ROMs replace the ROMs already on the board.
- The Reset Box controls debugger operation through use of reset and abort switches:

  RESET – When asserted (connected to ground) by an external device, the onboard reset logic is set in motion. The MPU (MC68000) is reset, behaving as described in the MC68000 Specification. All other onboard resources are reset simultaneously.

  ABORT – A Level 7 interrupt is generated. The PROM-based debugger may then service the interrupt with either halt program execution or dump address and data register, PC, SR, etc., to the CRT.

  The Reset Box includes a cable with a connector to attach to the ENP.

- Two ribbon cables with standard 25-pin RS 232 serial interface connectors are included. The female connector is configured DTE for use with a terminal. The male connector is configured DCE for downloading from the host system.

The following describes how to install the debugger:

1. Shut down your system and turn off the power.
2. Remove the ENP from the host system backplane.
3. Replace the ROMs with the Debugger ROMs. Use a small screwdriver to pry out the old ones if you have no PROM remover. The ROMs are marked as *H* (high) and *L* (low) and are

notched at one end. Be sure the notched end faces down when the board is oriented as shown in Figure 4-1 (board edge connector on the right and transceiver and cable connection on the left). Notches are also shown traced in white on the circuit board. The ROM marked *L* must go into the left socket, labelled U28 on the circuit board. The ROM marked *H* must go into the right socket, labelled U44 on the circuit board.

4. Attach the Reset Box cable to the ENP-30 at JP2.

   Note: Pin 1 on the cable must go to pin 1 on JP5. Normally, pin 1 is marked with a small triangle on the box connector on the end of the cable. Figure 4-3 shows the location of pin 1 on JP2.

5. Re-insert the ENP-30 into your system.

6. Connect the 26 pin connector at J5 to a video display terminal using the female ribbon cable supplied. Be sure pin 1 on the cable (marked with a red stripe) matches pin 1 on J5 (marked with a triangle).

7. Connect the 26 pin connector at J4 to a host serial port using the male ribbon cable supplied. As above, ensure that pin 1 on the cable matches pin 1 on J4.

For information on how to use the Debugger, refer to the *ENP Debugger User's Guide*.

Section 8

Powerup Diagnostics

8.1 Powerup Initialization

The K1 Kernel supplied with each ENP retrieves its stack pointer and initial program counter from locations $0 and $4, respectively, on system powerup. The map swap bit is immediately set in the MPU control status register, moving 4KB of DRAM located at $F00000 to location $0 and 4KB of K1 Kernel program code from $0 to $F80000.

A test of DRAM is performed after the swap bit is set followed by zeroing the entire DRAM area. Vector, stack, and variable initialization occurs next, followed by initiation of the DRAM refresh interrupt service routine.

The ENP then executes a series of diagnostic self tests which exercise the internal DRAM, registers, serial controller, and Ethernet controller on board.

The green *alive* LED on the ENP is turned on as an indication that all self tests have passed before jumping to the K1 Kernel executive.

The autovector 7 interrupt service routine handles three ENP exceptions: DRAM refresh, external abort, and parity error. DRAM refresh interrupts occur approximately every 2ms. Refresh is achieved by reading DRAM locations between $400 and $600. When a parity error interrupt occurs, the green *alive* light is turned off on the ENP (and on some models the red *fail* light will be turned on) and processing continues. The green LED will remain off until the ENP is reset or restarted.

ENP K1 Kernels use DRAM between $0 and $1000, and the upper 8KB of memory which is used for data and stack. The remaining DRAM is available for user applications.

8.2 Self Diagnostics

The ENP powerup and self diagnostic sequence is as follows:

On powerup, the ENP executes a series of self tests before initiating K I Kernel operation. Two internal DRAM pattern tests are performed, followed by an internal loopback test on the DUART (if present), an internal register interrupt test, and an internal loopback test on the Ethernet controller. If any single test fails, the green *alive* LED remains off, but program execution continues in the K I Kernel. Error status information is stored in a control block accessible by the bus host.

1. On startup, the presence of a parity error tells the ENP that a powerup has occurred and initiates self diagnostics.
2. A warm restart does not cause the ENP to perform self diagnostics, unless there is application code (e.g. TCP) in ROM.
3. If any single test fails (other than parity errors), ENP self diagnostics ceases and the failed test result is logged into the error control block.
4. ENP self diagnostics are performed in the following order:
   - Parity
   - Random Number RAM Pattern
   - Walking Bit RAM Pattern
   - DUART Internal Loopback
   - LANCE

The error control block contains specifics on the test that failed, the nature of the error, and related diagnostic information:

Offset From Base Error Control Block (Bytes)	Description
0	Reserved (word)
2	Test number (word)
4	Result code (long word)
8	Reserved (long word)
12	Reserved (long word)
1	Error address (long word)
20	Expected result (word)
22	Received result (word)

The control block may be viewed locally at $10 (relative to the start of ENP DRAM) using the debugger, or from the bus at $1010 bytes from the ENP, slave address.

Users are encouraged to attempt self diagnosis of a problem with an ENP, at least to the extent of reporting the contents of the error control block to CMC Technical Support.

Six powerup tests are currently being performed on the ENP. A short description of each test and the possible errors encountered follows:

8.2.1 Parity Check

The process of writing and reading memory on powerup will generate DRAM parity. If a parity error is detected, the error will be reported as follows:

Result Code	Error Address	Description
$1001		Parity error

8.2.2 Random Number DRAM Pattern Test

A pseudo random number pattern is written between memory locations $F01080 and the top of dynamic memory then read back and compared with the original pattern. Buffer comparison errors, error addresses and expected and received values are reported.

Result Code	Error Address	Description
$FFFFFFF4	(given)	Bus trap during memory write
$FFFFFFF5	(given)	Bus trap during memory read
$2001	(given)	Pattern comparison error

8.2.3 Walking Bit DRAM Pattern Test

A single bit is rotated through a 16-bit word and written to memory locations between $F01080 and top of dynamic memory. The data is read and verified with the original pattern. Any comparison error is reported as well as the address at which the comparison failure occurred and the expected and received values.

Result Code	Error Address	Description
$FFFFFFF4	(given)	Bus trap during memory access
$3002	(given)	Buffer comparison error

8.2.4 DUART Internal Loopback

The SC68681 DUART on board is initialized to internal loopback mode and a pattern transmitted from channels a and b. Each byte received is compared with the transmitted byte and any discrepancies reported.

Result Code	Error Address	Description
$FFFFFFFF	SC68681 address	Bus trap error
$4001		Transmit and receive bytes do not compare

8.2.5 Control/Status Register Test

The ENP Control/Status registers which generate autovectored interrupts 1 through 4, are written. A counter is ticked when the corresponding interrupt occurs and compared with the expected value. Interrupt generation is repeated twice. The timer is then initialized on the SC68681 and the interrupt at autovector Level 5 is verified. The Ethernet controller is then initialized and its ability to interrupt at autovector Level 6 is verified. Result codes appear as follows:

Result Code	Error Address	Description
$FFFFFFFF	(given)	Bus trap error
$FFFFFFFD		Bus trap during receive register access
$FFFFFFFC		Bus trap during transmit register access
$FFFFFFF3		Bus trap during Ethernet controller access
$5002	$FDA	Level 1 interrupt did not compare
$5003	$FDC	Level 2 interrupt did not compare
$5004	$FDE	Level 3 interrupt did not compare
$5005	$FE0	Level 4 interrupt did not compare
$5006	$FE2	Improper timer interrupt count
$5007	$FE4	Improper Ethernet controller interrupt count

8.2.6 Ethernet Controller Test

The Ethernet Controller Test includes a LANCE diagnostic, and the Control Transfer to the K I Kernel. These are detailed in the following subparagraphs.

8.2.6.1 LANCE

This diagnostic performs a series of tests on the LANCE device (if present) in internal loopback mode. Transmit and receive ring buffer sizes are varied in order to test the buffer chaining capabilities of the

device. In the first subtest, two receive buffers, 16 and 4 bytes long, are chained together for a 20-byte transmitted packet (including CRC). In the second subtest two 16 and 4 byte receive buffers are chained for a 24-byte transmitted packet. LANCE buffer error status is verified.

In subtest three, four (16, 2, 2, and 4 byte) buffers are placed in the receive ring. The four byte buffer is assigned host ownership, thereby disallowing LANCE use of the buffer. A 24-byte packet is transmitted, and buffer error status is verified. In subtest four, three (16, 2, and 2 byte) receive buffers are chained to accept a 24-byte transmitted packet. Transmit and receive buffers are compared to validate data transmission.

Specific addresses used by the LANCE loopback test are as follows:

Initialization Block – $600
Receive Message Descriptor – $680
Transmit Message Descriptor – $690
Transmit Buffer – $700
Receive Buffer – $800

Result codes appear as follows:

Result Code	Error Address	Description
$FFFFFFF3	$6X07	Bus trap during LANCE access.
No packet received.	$6X08	Transmit and receive packets do not compare.

An X in the result code represents the subtest number (1–4).

8.2.6.2 Control Transfer to K1 Kernel

Powerup tests are performed sequentially on the ENP. On successful completion of the tests, the result code in the error control block is zeroed, the green light emitting diode on the board is turned on, and control is passed immediately to the K1 Kernel. If any single test fails, the green LED remains off and control is passed to the K1 Kernel with the pertinent test information logged in the error control block. The host processor may at this time interpret the error control block results prior to downloading protocol software into the ENP and starting program execution in the ENP.

Section 9

Transceivers

9.1 Introduction

There are three different *Ethernet* transceiver interface specifications used by the industry. Ethernet 1.0 is the earliest version. It has a dc voltage offset of 0 to 5Vdc and differential voltage of 700mVdc, at quiescence on any signal line. Ethernet 2.0 has a dc voltage offset of 0 to 5Vdc and no dc voltage differential at quiescence. IEEE 802.3 has no dc voltage offset and no dc differential voltage at quiescence. Ethernet 2.0 and IEEE 802.3 are similar enough that interoperability should cause no problems.

The ENP-30, Rev. A is designed only for Ethernet 1.0. The ENP-30, Rev. B, is factory configured for IEEE 802.3; but can be reconfigured for Ethernet 1.0, when needed.

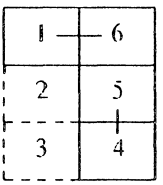
Transceiver interfaces should match transceiver interface types. The consequences of a mismatch will vary but will usually result in a dramatic reduction in performance of a node due to an increase in the number of CRC and alignment errors. Other possible manifestations include: (1) network lockup due to a babbling transceiver (802.3 interface hooked to a 1.0 transceiver), (2) failure of other link layer hardware that cannot tolerate spurious bits at end of transmission (transceiver type matches interface but non-CMC equipment is old 1.0 type), and (3) transceiver lockup due to intolerable transients during the onset of transmission. The latter error results in the transceiver light going out (802.3 interface driving 1.0 transceiver or visa versa, or ENP jumpering not proper for 802.3). All of these failures have been observed at customer sites and/or at CMC.

Modification of the ENP-30 for Ethernet 1.0 requires replacement of the PE8302 pulse transformer U115 with a 16-pin DIP jumper platform. On the jumper platform, connect pins 1–16, 2–15, 3–14, 4–13, 5–12, 6–11, 7–10, 8–9. In addition, place a jumper between

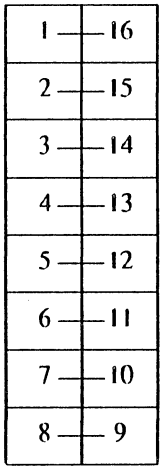
JP03 pins 1–6.

The following table shows the changes required to convert an ENP-30, Rev. B, from IEEE 802.3 to Ethernet 1.0:

ENP Rev.	Substitute 16-Pin DIP Jumper Platform For:	Add Shunt To:	Notes:
Rev. A	N.A.	N.A.	Already Ethernet 1.0; it has no PE8302 pulse transformer.
Rev. B	U115	JP03 pins 1–6	Setup jumper platform JP03 as shown below:



The pulse transformer and shunt positions on the ENP are located near the LANCE (Am7991). The jumper platform that is substituted for the PE8302 is diagramed below:



9.2 Common Transceivers and Their Type

The following is a list of commonly-used transceivers showing their interface type: Ethernet version 1.0 or IEEE 802.3 (Ethernet version 2.0 is identical to IEEE 802.3). Before installing the ENP, determine the transceiver type to which it will be connected. If the transceiver type differs from the ENP's default configuration (IEEE 802.3), you will need to rejumper the PC board as described above.

The following is a reference list of common transceiver types, known to be compatible with the ENP. Please note that this list is not intended to be complete nor does it intend to make recommendations.

Table 9-1. Common Transceiver Types

Model	IEEE 802.3	Ethernet 1.0
3COM	No	Yes
Cabletron MT800 (Multiport)	Yes	Yes
Cabletron ST500	Yes	Yes
DEC DELNI (Multiport)	Yes	Yes
DEC DESTA	No	Yes
DEC H4000	No	Yes
DEC H4005	Yes	Yes
Intel (Multiport)	No	Yes
Interlan NT100	Yes	No
Interlan NT10	No	Yes
TCL 2010 I series	Yes	No
TCL 2010 E series	No	Yes
TCL 2010 EB (with heartbeat)	No	Yes
EXOS 1110	No	Yes
EXOS 1111	Yes	No
BICC ISOLAN 1112	Yes	No
BICC ISOLAN 1113	No	Yes

Section 10

LANCE Programming Specification

10.1 Introduction

This section defines the control and status registers and the memory data structures required to program the LANCE. For the discussions herein, the referenced host is the MC68000 microprocessor on the ENP.

10.2 Programming the Am7990 LANCE

The Am7990 LANCE is designed to operate in an environment that includes close coupling with a local memory and a microprocessor (host). The Am7990 LANCE is programmed by a combination of registers and data structures resident within the chip and in memory. There are four control and status registers (CSRs) within the chip, which are programmed by the host device. Once enabled, the chip has the ability to access memory locations to acquire additional operating parameters.

The Am7990 has the ability to do independent buffer management and to transfer data packets to and from the Ethernet. There are three memory structures accessed by the chip:

1. Initialization Block — 12 words in contiguous memory starting on a word boundary. It also contains the operating parameters necessary for device operation. The initialization block contains:
   - Mode of operation
   - Physical address
   - Logical address mask
   - Location of receive and transmit descriptor rings

- Number of entries in receive and transmit descriptor rings

2. Receive and Transmit Descriptor Rings — Two ring structures, one each for incoming and outgoing packets. Each entry in the rings is 4 words long and each entry must start on a quadword boundary. The descriptor rings contain:

   - The address of a data buffer
   - The length of that buffer
   - Status information associated with the buffer

3. Data Buffers — Contiguous portions of memory reserved for packet buffering. Data buffers may begin on arbitrary byte boundaries.

In general, the programming sequence of the chip may be summarized as:

1. Programming the chip's CSRs by a host device to locate an initialization block in memory. The byte control, byte addressing and address latch enable modes are defined here, also.
2. The chip loading itself with information contained within the initialization block.
3. The chip accessing the descriptor rings for packet handling.

10.3 Control and Status Registers

There are four control and status registers (CSRs) resident within the chip. The CSRs are accessed through two bus addressable ports, an address port (RAP) and a data port (RDP).

10.3.1 Accessing the Control and Status Registers

The CSRs are read (or written) in a two-step operation. The address of the CSR to be accessed is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten.

To distinguish the data port from the address port, a discrete I/O pin is provided as follows:

ADR I/O Pin	Port
L	Register data (RDP)
H	Register address port (RAP)

10.3.1.1 Register Data Port (RDP)

The Register Data Port (RDP) is illustrated in Figure 10-1 and detailed in Table 10-1.

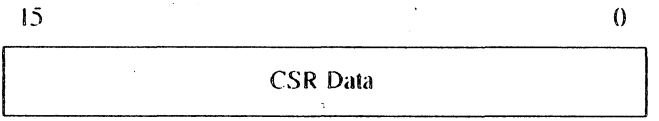


Figure 10-1. Register Data Port

Table 10-1. Register Data Port

Bit	Name	Description
15:00	CSR Data	Writing data into RDP writes the data into the CSR selected in RAP. Reading the data from the RDP reads the data from the CSR selected in RAP. CSR_1, CSR_2 and CSR_3 are accessible only when the STOP bit of CSR_0 is set. If the STOP bit is not set while attempting to access CSR_1, CSR_2 or CSR_3, the chip will not respond to the bus transfer.

10.3.1.2 Register Address Port (RAP)

The Address Register Port (RAP) is illustrated in Figure 10-2 and detailed in Table 10-2.

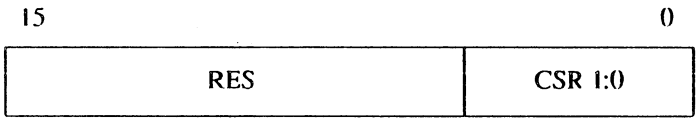


Figure 10-2. Register Address Port

Table 10-2. Register Address Port

Bit	Name	Description
15:02	RES	Reserved and read as zeroes.
01:00	CSR(1:0)	CSR address select. Read/Write. Selects the CSR to be accessed through the RDP. RAP is cleared by bus RESET. CSR(1:0) — CSR 00 — CSR_0 01 — CSR_1 10 — CSR_2 11 — CSR_3

10.3.2 Control and Status Register Definition

Control and Status Definition is detailed in the following subparagraphs.

10.3.2.1 Control and Status Register 0 (CSR_0)

The Control and status Register 0 (CSR_0) is illustrated in Figure 10-3 and detailed in Table 10-3.

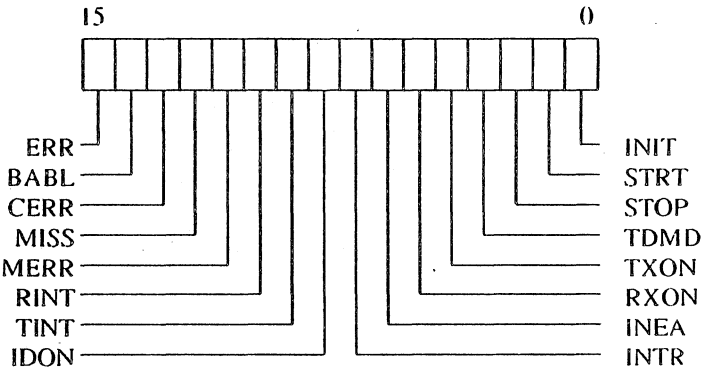


Figure 10-3. Control and Status Register 0 (CSR_0)

Table 10-3. Control and Status Register 0

Bit	Name	Description
15	ERR	ERROR summary is set by the "OR" of BABL, CERR, MISS and MERR. ERR remains set as long as any of the error flags are true. ERR is read only; writing it has no effect. It is cleared by bus RESET or by setting the STOP bit.
14	BABL	BABBLE is a transmitter time-out error. It indicates that the transmitter has been on the channel longer than the time required to send the maximum length packet. BABL will be set after 1519 bytes have been transmitted. When BABL is set, an interrupt will be generated if INEA = 1. BABL is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.
13	CERR	COLLISION ERROR. The collision input to the chip failed to activate within 2µs after a chip-initiated transmission was completed. The collision after transmission is a transceiver test feature. CERR is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.

Bit	Name	Description
12	MISS	MISSED PACKET is set when the receiver loses a packet because it does not own a receive buffer and the SILO has overflowed, indicating loss of data. When MISS is set, an interrupt will be generated if INEA = 1. MISS is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.
11	MERR	MEMORY ERROR is set when the chip is the bus master and has not received READY within 25.6μ after asserting the address on the DAL lines. When a MERR is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.

Bit	Name	Description
10	RINT	RECEIVER INTERRUPT is set after the chip updates an entry in the Receive Descriptor Ring. When RINT is set, an interrupt is generated if INEA = 1. RINT is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.
09	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the transmit descriptor ring. When TINT is set, an interrupt is generated if INEA = 1. TINT is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.
08	IDON	INITIALIZATION DONE indicates that the chip completed the initialization procedure started by setting the INIT bit. When IDON is set, the chip has read the Initialization Block from memory and stored the new parameters. When IDON is set, an interrupt is generated if INEA = 1. IDON is Read/Clear Only and is set by the chip and cleared by writing a 1 into the bit. Writing a 0 has no effect. It is cleared by RESET or by setting the STOP bit.

Bit	Name	Description
07	INTR	INTERRUPT FLAG. One or more of the following interrupt-causing conditions has occurred: BABL, MISS, MERR, RINT, TINT, IDON. If INEA = 1 and INTR = 1, the INTR I/O pin will be low. INTR is Read Only; writing this bit has no effect. INTR is cleared by RESET or by setting the STOP bit.
06	INEA	INTERRUPT ENABLE allows the INTR I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1, the INTR I/O pin will be low. If INEA = 0, the INTR I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is Read/Write and cleared by RESET or by setting the STOP bit.
05	RXON	RECEIVER ON indicates that the receiver is enabled. RXON is set when STRT is set if DRX = 0 in the MODE register in the initialization block and the initialization block has been read by the chip by setting the INIT bit. RXON is cleared when IDON is set from setting the INIT bit and DRX = 1 in the MODE register or a memory error (MERR) has occurred. RXON is Read Only; writing this bit has no effect. RXON is cleared by RESET or by setting the STOP bit.

Bit	Name	Description
04	TXON	TRANSMITTER ON indicates that the transmitter is enabled. TXON is set when STRT is set if DTX = 0 in the MODE register in the initialization block and the INIT bit has been set. TXON is cleared when IDON is set and DTX = 1 in the MODE register, or an error has occurred during transmission, or a memory error (MERR) has occurred. TXON is Read Only; writing this bit has no effect. TXON is cleared by RESET or by setting the STOP bit.
03	TDMD	TRANSMIT DEMAND, when set, causes the chip to access the transmit descriptor ring without waiting for the polltime interval to elapse. TDMD need not be set to transmit a packet; it merely hastens the chip's response to a transmit descriptor ring entry insertion by the host. TDMD is Write With 1 Only and cleared by the microcode after it is used. It may read as a 1 for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by RESET or by setting the STOP bit. Writing a 0 in this bit has no effect.

Bit	Name	Description
02	STOP	STOP disables the chip from all external activity when set and clears the internal logic. Setting STOP is the equivalent of asserting RESET. The chip remains inactive and STOP remains set until the STRT or INIT bit is set. If STRT, INIT and STOP are all set together, STOP will override the other bits and only STOP will be set. STOP is Read/Write With 1 Only and set by RESET. Writing a 0 to this bit has no effect.
01	STRT	START enables the chip to send and receive packets, perform direct memory access, and do buffer management. If STRT and INIT are set together, the INIT function will be executed first. STRT is Read/Write With 1 Only. Writing a 0 into this bit has no effect. STRT is cleared by RESET or by setting the STOP bit.
00	INIT	INITIALIZE, when set, causes the chip to begin the initialization procedure and access the initialization block. If STRT and INIT are set together, the INIT function will be executed first. INIT is Read/Write With 1 Only. Writing a 0 into this bit has no effect. INIT is cleared by RESET or by setting the STOP bit.

10.3.2.2 Control and Status Register 1 (CSR_1)

RAP = 1

Read/Write: Accessible only when the STOP bit of CSR_0 is a 1. CSR_1 is unaffected by RESET.

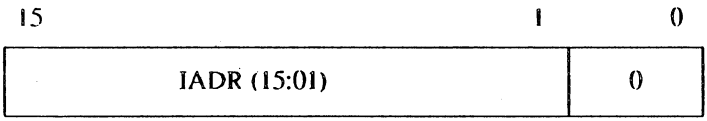


Figure 10-4. Control and Status Register 1

Table 10-4. Control and Status Register 1

Bit	Name	Description
15:01	IADR	The low-order 16 bits of the address of the first word (lowest address) in the initialization block.
00		Must be zero.

10.3.2.3 Control and Status Register 2 (CSR_2)

RAP = 2

Read/Write: Accessible only when the STOP bit of CSR_0 is a 1. CSR_2 is unaffected by RESET.

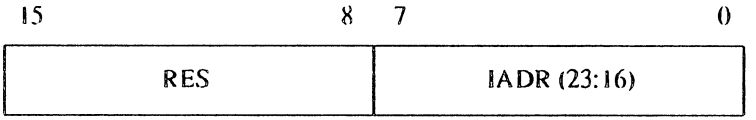


Figure 10-5. Control and Status Register 2

Table 10-5. Control and Status Register 2

Bit	Name	Description
15:08	RES	Reserved
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the initialization block.

10.3.2.4 Control and Status Register 3 (CSR_3)

CSR_3 allows redefinition of the bus master interface.

RAP = 3

Read/Write: Accessible only when the STOP bit of CSR_0 is 1. CSR_3 is cleared by RESET or by setting the STOP bit in CSR_0.

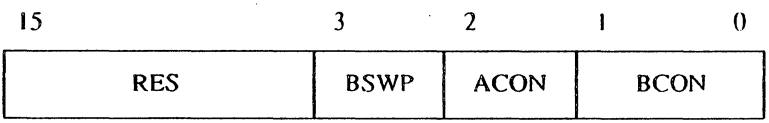


Figure 10-6. Control and Status Register 3

Table 10-6. Control and Status Register 3

Bit	Name	Description
15:03	RES	Reserved and read as 0.
02	BSWP	BYTE SWAP allows the chip to operate in systems that consider bits (15:08) to be the least significant byte and bits (07:00) to be the most significant byte. When BSWP = 1, the chip will swap the high and low bytes on DMA data transfers between the SILO and bus memory. Only data from SILO transfers are swapped; the initialization block data and the descriptor ring entries are NOT swapped. BSWP is Read/Write and cleared by RESET or by setting the STOP bit in CSR_0.
01	ACON	ALE CONTROL defines the assertive state of ALE when the chip is a bus master. ACON is Read/Write and cleared by RESET and by setting the STOP bit in CSR_0. ACON — ALE 0 — Asserted High 1 — Asserted Low

Bit	Name	Description
00	BCON	BYTE CONTROL redefines the byte mask and Hold I/O pins. BCON is Read/Write and cleared by RESET or by setting the STOP bit in CSR_0.

	I/O Pin	I/O Pin	I/O Pin
	---	---	---
BCON	16	15	17
0	BM1	BM0	HOLD
1	BUSAKO	BYTE	BUSRQ

10.4 Initialization

Initialization details are provided in the following paragraphs.

10.4.1 Initialization Block

Chip initialization includes the reading of the initialization block in memory to obtain the operating parameters. The following is a definition of the initialization block.

The initialization block is read by the chip when the INIT bit in CSR_0 is set. The INIT bit should be set before or concurrent with the STRT bit to insure proper parameter initialization and chip operation. After the chip has read the initialization block, IDON is set in CSR_0 and an interrupt is generated if INEA = 1.

Table 10-7. Initialization Block

Higher Addresses	TLEN-TDRA (23:16)	IADR +22
	TDRA (15:00)	IADR +20
	RLEN-RDRA (23:16)	IADR +18
	RDRA (15:00)	IADR +16
	LADRF (63:48)	IADR +14
	LADRF (47:32)	IADR +12
	LADRF (31:16)	IADR +10
	LADRF (15:00)	IADR +08
	PADR (47:32)	IADR +06
	PADR (31:16)	IADR +04
	PADR (15:00)	IADR +02
Base Address of Block	MODE	IADR +00

10.4.2 Mode

The mode register allows alteration of chip's operating parameters. Normal operation is with the mode register clear.

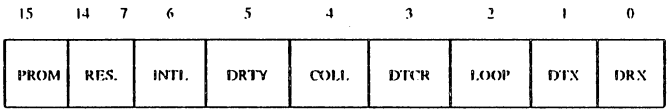


Figure 10-7. Mode Register

Table 10-8. Mode Register

Bit	Name	Description
15	PROM	PROMISCUOUS mode. When PROM = 1, all incoming packets are accepted.
14:07	RES	RESERVED
06	INTL	INTERNAL LOOPBACK is used with the LOOP bit to determine where the loopback is to be done. Internal loopback allows the chip to receive its own transmitted packet. Since this represents full duplex operation, the packet size is limited to 32 bytes. INTL is valid only if LOOP = 1; it is ignored otherwise. LOOP INTL LOOPBACK 0 X No loopback, normal 1 0 External 1 1 Internal
05	DRTY	DISABLE RETRY. When DRTY = 1, the chip will attempt only one transmission of a packet. If there is a collision on the first transmission attempt, a Retry Error (RTRY) will be reported in Transmit Message Descriptor 3 (TMD_3).
04	COLL	FORCE COLLISION. This bit allows the collision logic to be tested. The chip must be in internal loopback mode for COLL to be valid. If COLL = 1, a collision will be forced during the subsequent transmission attempt. This will result in 16 total transmission attempts with a retry error reported in TMD_3.

Bit	Name	Description
03	DTCR	DISABLE TRANSMIT CRC. When DTCR = 0, the transmitter will generate and append a CRC to the transmitted packet. When DTCR = 0, the CRC logic is allocated to the receiver and no CRC is generated and sent with the transmitted packet. During loopback, DTCR = 0 will cause a CRC to be generated on the transmitted packet, but no CRC check will be done by the receiver since the CRC logic is shared and cannot generate the check CRC at the same time. The generated CRC will be written into memory with the data and can be checked by the host software. If DTCR = 1 during loopback, the host software must append a CRC value to the transmit data. The receiver will check the CRC on the received data and report any errors.

Bit	Name	Description
02	LOOP	LOOPBACK allows the chip to operate in full duplex mode for test purposes. The maximum packet size is limited to 32 bytes. During loopback, the runt packet filter is disabled because the maximum packet is forced to be smaller than the minimum size Ethernet packet (64 bytes). LOOP = 1 allows simultaneous transmission and reception for a message constrained to fit within the SILO. The chip waits until the entire message is in the SILO before serial transmission begins. The incoming data stream fills the SILO from behind as it is being emptied. Moving the received message out of the SILO to memory does not begin until reception has ceased. In loopback mode, transmit data chaining is not possible. Receive data chaining is possible.
01	DTX	DISABLE THE TRANSMITTER causes the chip to not access the transmit descriptor ring; therefore no transmissions are attempted. DTX will clear the TXON bit in CSR_0 when initialization is complete.
00	DRX	DISABLE THE RECEIVER causes the chip to reject all incoming packets and not access the Receive Descriptor Ring. DRX clears the RXON bit in CSR_0 when initialization is complete.

10.4.3 Physical Address

The Physical Address is illustrated in Figure 10-8 and detailed in Table 10-9.

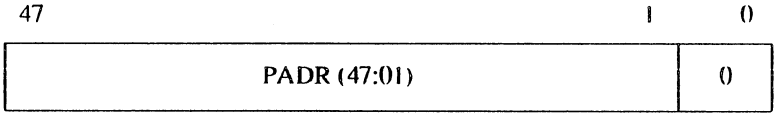


Figure 10-8. Physical Address

Table 10-9. Physical Address

Bit	Name	Description
47:00	PADR	PHYSICAL ADDRESS is the unique 48-bit physical address assigned to the chip. PADR (0) must be 0.

10.4.4 Logical Address Filter

The logical address filter is a 64-bit mask that is used to accept incoming logical addresses. The incoming address is sent through the CRC circuit. After all 48 bits of the address have gone through the CRC circuit, the high order 6 bits of the resultant CRC are strobed into a register. This register is used to select one of the 64-bit positions in the logical address filter. If the selected filter bit is a 1, the address is accepted and the packet will be put in memory. The first bit of the incoming address must be a 1 for a logical address. If the first bit is a 0, it is a physical address and is compared against the physical address that was loaded through the initialization block.

The broadcast address, which is all ones, does not go through the logical address filter and is always enabled. If the logical address filter is loaded with all zeroes, all incoming logical addresses except broadcast will be rejected.

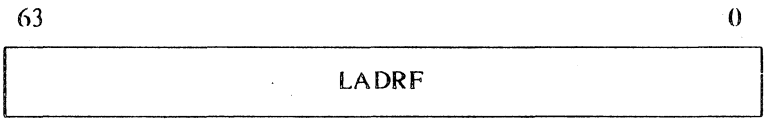


Figure 10-9. Logical Address Filter

Table 10-10. Logical Address Filter

Bit	Name	Description
63:00	LADRF	The 64-bit mask used by the chip to accept logical addresses.

10.4.5 Receive Descriptor Ring Pointer

The Receive Descriptor Ring Pointer is illustrated in the following Figure 10-10 and detailed in Table 10-11.

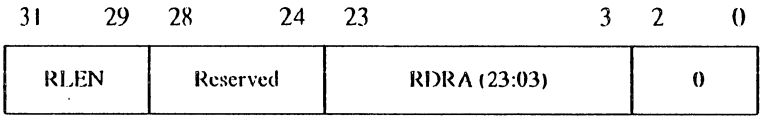


Figure 10-10. Receive Descriptor Ring Pointer

Table 10-11. Receive Descriptor Ring Pointer

Bit	Name	Description
15:13	RLEN	RECEIVE RING LENGTH is the number of entries in the receive ring expressed as a power of 2. RLEN — Number of Entries 0 — 1 1 — 2 2 — 4 3 — 8 4 — 16 5 — 32 6 — 64 7 — 128
12:00	RES	RESERVED

Bit	Name	Description
07:00 15:03	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address (lowest address) of the receive descriptor ring.
02:00		MUST BE ZEROES. These bits are RDRA (02:00) and must be zeroes because the receive rings are aligned on quadword boundaries.

10.4.6 Transmit Descriptor Ring Pointer

The Transmit Descriptor Ring Pointer is illustrated in Figure 10-11 and detailed in Table 10-12.

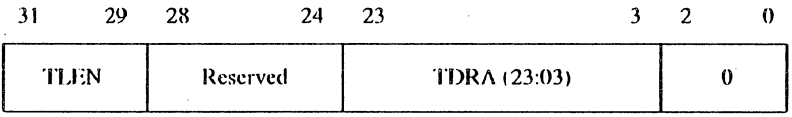


Figure 10-11. Transmit Descriptor Ring Pointer

Table 10-12. Transmit Descriptor Ring Pointer

Bit	Name	Description
15:13	TLEN	TRANSMIT RING LENGTH is the number of entries in the transmit ring expressed as a power of 2 TLEN — Number of Entries 0 — 1 1 — 2 2 — 4 3 — 8 4 — 16 5 — 32 6 — 64 7 — 128
12:08	RES	RESERVED

Bit	Name	Description
07:00 15:03	TDRA	TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the transmit descriptor ring.
02:00		MUST BE ZEROES. These bits are TDRA (02:00) and must be zeroes because the transmit rings are aligned on quadword boundaries.

10.5 Buffer Management

Buffer management is accomplished through message descriptors organized in ring structures in memory. Each message descriptor entry is four words long. There are two rings allocated for the device: a receive ring and a transmit ring. The device is capable of polling each ring for buffers to either empty or fill with packets to or from the channel. The device is also capable of entering status information in the descriptor entry. Chip polling is limited to looking one ahead of the descriptor entry with which the chip is currently working.

The location of the descriptor rings and their length are found in the initialization block, accessed during the initialization procedure by the chip. Writing a 1 into the STRT bit of CSR_0 will cause the chip to start accessing the descriptor rings and enable it to send and receive packets.

The chip communicates with a host device (probably a microprocessor) through the ring structures in memory. Each entry in the ring is "owned" either by the chip or the host. There is an ownership bit (OWN) in the message descriptor entry. Mutual exclusion is accomplished by a protocol which states that each device can only relinquish ownership of the descriptor entry to the other device; it can never take ownership, and each device cannot change the state of any field in any entry after it has relinquished ownership.

10.6 Descriptor Rings

Each descriptor in a ring in memory is a four-word entry. The following is the format of the receive and the transmit descriptors.

10.6.1 Receive Message Descriptor Entry

The following subparagraphs define each of the Receive Message Descriptor Entries.

10.6.1.1 Receive Message Descriptor 0 (RMD_0)

The Receive Message Descriptor 0 (RMD_0) is illustrated in Figure 10-12 and defined in Table 10-13.

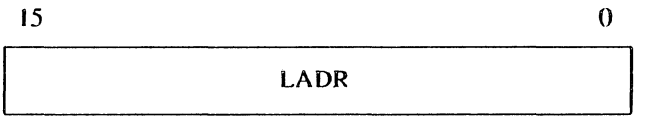


Figure 10-12. Receive Message Descriptor 0

Table 10-13. Receive Message Descriptor 0

Bit	Name	Description
15:00	LADR	The LOW ORDER 16 address bits of the buffer pointed to by this descriptor. LADR is written by the host and unchanged by the chip.

10.6.1.2 Receive Message Descriptor 1 (RMD_1)

The Receive Message Descriptor 1 (RMD_1) is illustrated in Figure 9-13 and detailed in Table 10-14.

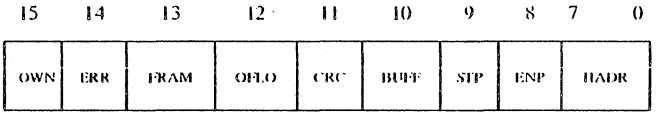


Figure 10-13. Receive Message Descriptor 1

Table 10-14. Receive Message Descriptor 1

Bit	Name	Description
15	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the chip (OWN = 1). The chip clears the OWN bit after filling the buffer pointed to by the descriptor entry. The host sets the OWN bit after emptying the buffer. Once the chip or host has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	ERR	ERROR summary is the "OR" of FRAM, OFLO, CRC, or BUFF. ERR is set by the chip and cleared by the host.
13	FRAM	FRAMING ERROR indicates that the incoming packet contained a noninteger multiple of 8 bits and there was a CRC error. If there was not a CRC error on the incoming packet, then FRAM will not be set, even if there was a non-integer multiple of 8 bits in the packet. FRAM is set by the chip and cleared by the host.
12	OFLO	OVERFLOW error indicates the receiver has lost all or part of the incoming packet due to an inability to store the packet in a memory buffer before the internal SILO overflowed. OFLO is set by the chip and cleared by the host.
11	CRC	CRC indicates that the receiver has detected a CRC error on the incoming packet. CRC is set by the chip and cleared by the host.

Bit	Name	Description
10	BUFF	BUFFER ERROR is set when the chip runs out of available buffers while data chaining a received packet. BUFF is set by the chip and cleared by the host. If a BUFF occurs, an OFLO will also occur, because the chip tries to acquire the next buffer until the SILO overflows.
09	STP	START OF PACKET indicates that this is the first buffer used by the chip for this packet. It is used for data chaining buffers. STP is set by the chip and cleared by the host.
08	ENP	END OF PACKET indicates that this is the last buffer used by the chip for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fit into one buffer and there was no data chaining. ENP is set by the chip and cleared by the host.
07:00	HADR	The HIGH ORDER 8 address bits of the buffer pointed to by this descriptor. This field is written by the host and unchanged by the chip.

10.6.1.3 Receive Message Descriptor 2 (RMD_2)

The Receive Message Descriptor 2 (RMD_2) is illustrated in Figure 10-14 and detailed in Table 10-15.

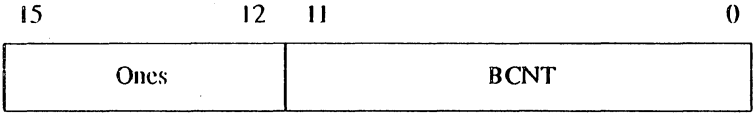


Figure 10-14. Receive Message Descriptor 2

Table 10-15. Receive Message Descriptor 2

Bit	Name	Description
15:12		MUST BE ONES. This field is written by the host and unchanged by the chip.
11:00	BCNT	BUFFER BYTE COUNT is the length of the buffer pointed to by this descriptor expressed as a two's complement number. The field is written by the host and unchanged by the chip.

10.6.1.4 Receive Message Descriptor 3 (RMD_3)

The Receive Message Descriptor 3 (RMD_3) is illustrated in Figure 10-15 and detailed in Table 10-16.

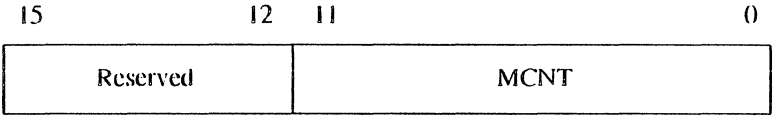


Figure 10-15. Receive Message Descriptor 3

Table 10-16. Receive Message Descriptor 3

Bit	Name	Description
15:12	RES	RESERVED and read as zeroes.
11:00	MCNT	MESSAGE BYTE COUNT is the length in bytes of the received message. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by the chip and cleared by the host.

10.6.2 Transmit Message Descriptor Entry

The Transmit Message Descriptor Entries are described in the following subparagraphs.

10.6.2.1 Transmit Message Descriptor 0 (TMD_0)

The Transmit Message Descriptor 0 (TMD_0) is illustrated in Figure 10-16 and detailed in Table 10-17.

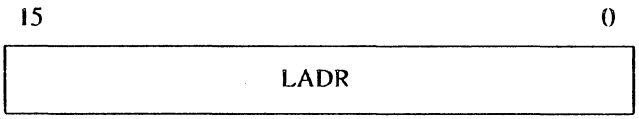


Figure 10-16. Transmit Message Descriptor 0

Table 10-17. Transmit Message Descriptor 0

Bit	Name	Description
15:00	LADR	The LOW ORDER 16 address bits of the buffer pointed to by this descriptor. LADR is written by the host and unchanged by the chip.

10.6.2.2 Transmit Message Descriptor 1 (TMD_1)

The Transmit Message Descriptor 1 (TMD_1) is illustrated in Figure 10-17 and detailed in Table 10-18.

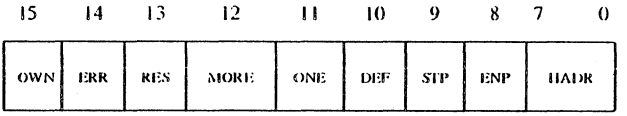


Figure 10-17. Transmit Message Descriptor 1

Table 10-18. Transmit Message Descriptor 1

Bit	Name	Description
15	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the chip (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by this descriptor. The chip clears the OWN bit after transmitting the contents of the buffer. Neither may alter a descriptor entry after it has relinquished ownership.
14	ERR	ERROR summary is the "OR" of LCOL, LCAR, UFLO or RTRY. ERR is set by the chip and cleared by the host.
13	RES	RESERVED bit. The chip will write this bit with a 0.

Bit	Name	Description
12	MORE	MORE indicates that more than one retry was needed to transmit a packet. MORE is set by the chip and cleared by the host.
11	ONE	ONE indicates that exactly one retry was needed to transmit a packet. ONE is set by the chip and cleared by the host.
10	DEF	DEFERRED indicates that the chip had to defer while trying to transmit a packet. This condition occurs if the channel is busy when the chip is ready to transmit. DEFER is set by the chip and cleared by the host.
09	STP	START OF PACKET indicates this is the first buffer to be used by the chip for this packet. It is used for data chaining buffers. STP is set by the host and unchanged by the chip.
08	ENP	END OF PACKET indicates this is the last buffer to be used by the chip for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fit into one buffer and there was no data chaining. ENP is set by the host and unchanged by the chip.
07:00	HADR	The HIGH ORDER 8 address bits of the buffer pointed to by this descriptor. This field is written by the host and unchanged by the chip.

10.6.2.3 Transmit Message Descriptor 2 (TMD_2)

The Transmit Message Descriptor 2 (TMD_2) is illustrated in Figure 10-18 and detailed in Table 10-19.

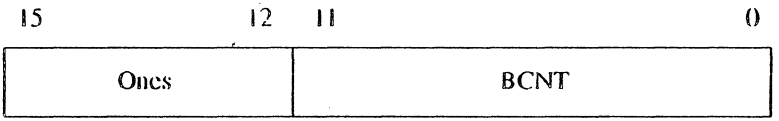


Figure 10-18. Transmit Message Descriptor 2

Table 10-19. Transmit Message Descriptor 2

Bit	Name	Description
15:12	ONES	Must be ones. This field is set by the host and unchanged by the chip.
11:00	BCNT	BUFFER BYTE COUNT is the usable length in bytes of the buffer pointed to by this descriptor expressed as a two's complement number. This is the number of bytes from this buffer that will be transmitted by the chip. This field is written by the host and unchanged by the chip.

10.6.2.4 Transmit Message Descriptor 3 (TMD_3)

The Transmit Message Descriptor 3 (TMD_3) is illustrated in Figure 10-19 and detailed in Table 10-20.

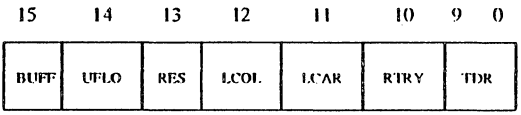


Figure 10-19. Transmit Message Descriptor 3

Table 10-20. Transmit Message Descriptor 3

Bit	Name	Description
15	BUFF	BUFFER ERROR is set by the chip during transmission when the chip does not find the ENP flag in the current buffer and does not own the next buffer. BUFF is set by the chip and cleared by the host. If a BUFF occurs, a UFLO will also occur because the chip tries to read memory data until the SILO is empty.
14	UFLO	UNDERFLOW ERROR indicates that the transmitter has truncated a message due to data late from memory. UFLO indicates that the SILO has emptied before the end of the packet was reached. UFLO is set by the chip, cleared by the host.

Bit	Name	Description
13	RES	RESERVED bit. The chip will write this bit with a 0.
12	LCOL	LATE COLLISION indicates that a collision has occurred after the slot time of the channel has elapsed. The chip does not retry on late collisions. LCOL is set by the chip and cleared by the host.
11	LCAR	LOSS OF CARRIER indicates that the carrier signal was not detected for some period during the transmission of the packet. LCAR is set by the chip and cleared by the host.
10	RTRY	RETRY ERROR indicates that the transmitter has failed in 16 attempts to successfully transmit a message due to repeated collisions on the medium. If DTRY = 1 in the MODE register, RTRY will set after one failed transmission attempt. RTRY is set by the chip and cleared by the host.
09:00	TDR	TIME DOMAIN REFLECTOMETRY reflects the state of an internal chip counter that counts from the start of a transmission to the occurrence of a collision. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by the chip and is valid only if RTRY or LCOL is set.