Multibus™ I

CDSBC™ 21/8635-E

Reference Manual

Central Data

Multibus™ I

CDSBC™ 21/8635-E

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Manual Order Number: CD91/8635-EMAN
Internal Part Number: 180053

This version of the *Multibus I* cDSBC 21/8635-E *Reference Manual* was published on March 13, 1990.

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1. General Information

Distinctive Characteristics

* Fully software compatible with the Intel 86/12A, 86/14, 86/30, and 86/35
* Can be configured for complete hardware compatibility with the Intel 86/30 or 86/35
* 5, 8, or 10MHz 8086 (or NEC V30™) CPU operation (strap-selectable)
* Two JEDEC-compatible 28-pin sockets for up to 128K of EPROM (2732-27512); can have either 16K or 64K of RAM or EEPROM
* Two additional JEDEC-compatible 32-pin sockets for up to 512K of EPROM (2732-27020); can have either 16K, 64K, or 128K of RAM
* 128K, 256K, 512K, or 1 megabyte of dual-port RAM with zero-wait-state access from the on-board 8086 (at 10MHz)
* Standard parity checking for dynamic RAM
* On-board socket for the 8087 numeric data coprocessor
* Two SBX connectors
* One serial I/O port (8251A)
* 24 programmable parallel I/O lines (8255A-5)
* Nine levels of interrupt priority, expandable to 65 levels (8259A)
* Three programmable timers (8253-5)
* Supports 20- and 24-bit addressing
* Full Multibus™ multi-master capabilities

The CDSBC™ 21/8635-E is an 8086-based single-board computer that is both hardware and software compatible with Intel 86/30 and 86/35 boards. It offers improved performance over Intel boards via its zero-wait-state dynamic RAM access at the 10MHz 8086 clock rate, as well as up to 1 megabyte of on-board RAM. Also, an on-board socket for the 8087 numeric data coprocessor reduces cost for applications requiring such a coprocessor.

Optionally, an NEC V30 microprocessor can be substituted for the 8086 microprocessor. Depending upon the application, the V30 reportedly provides a 5-

30% performance increase over the 8086. Central Data provides this option as a service to our customers, but we make no guarantee for increased performance or software compatibility of the V30 versus the 8086. In this manual the general term "8086" is used to refer to the microprocessor where, in fact, either processor can be installed. The Functional Description chapter lists the differences between the two versions of the board.

Four JEDEC sockets permit up to 640K of EPROM or a combination of up to 512K of EPROM and 64K of RAM/EEPROM to be inserted on the board.

The processors on the CDSBC 21/8635-E are socketed, and the processor clock frequency is jumper selectable for 5, 8, or 10MHz operation. The optional 8087 numeric data coprocessor may be added at any time. The 8086 has access to all on-board memory and peripherals as well as all Multibus memory and peripherals through a full multi-master interface. The Multibus interface may use either 20- or 24-bit memory addressing.

On-board I/O includes 2 SBX connectors, 24 programmable parallel I/O lines, a serial port, 3 programmable timers, and 9 to 65 levels of priority interrupt.

2. Functional Description

This chapter provides an overview of the CDSBC 21/8635-E Single-Board Computer. In this manual, both active-high and active-low signals appear in the text. Whenever a signal is active-low, its mnemonic is followed by a slash (/).

Architecture

The board has a three-level bus structure: 1) local bus, 2) dual-port RAM bus, and 3) Multibus interface bus. The CPU uses the local bus (A0-A19 and D0-D15) to access all on-board devices (EPROM, SBX modules, and I/O devices) and to access the dual-port RAM bus. The local bus cannot be accessed from the Multibus, so the use of this internal bus is contention-free.

The dual-port RAM bus (AB0-AB19 and DB0-DB15) resides between the local bus and the Multibus interface and connects to the dual-port RAM array. It is used whenever the on-board CPU or a Multibus master wishes to gain access to the dual-port RAM, or as a transfer bus between the local bus and the Multibus interface when the on-board CPU makes Multibus accesses. Since it is a shared bus, its use must be requested and a grant received, before either the on-board CPU or Multibus master can gain access to the bus.

The Multibus interface bus allows the on-board CPU to access Multibus resources and allows other Multibus masters to access the on-board dual-port RAM.

Functional Blocks

The 8086 (a 16-bit microprocessor) or the NEC V30 processor and optional 8087 (a 16-bit numeric data coprocessor) provide the computational power of the CDSBC 21/8635-E. A 10MHz 8086 is shipped with all boards; however, the 5, 8, or 10MHz processor clock selection must be chosen to support both the 8086 and 8087, if the 8087 is installed.

One known problem exists with the use of the V30 and the 8087 numeric data coprocessor. The 8087 requires a 33% duty cycle clock, while the V30 requires a 50% duty cycle clock. Since a single clock signal drives both devices, its frequency must be selected to meet the requirements of both devices. Unfortunately, this means that to operate with an 8087 both devices must be 10MHz, but can only operate at 8MHz. The 8MHz square wave clock input to the 8087 has time periods which satisfy the 33% duty cycle.

The V30 microprocessor version of the 8086 board is identical to the standard 8086 version with the exception of the following parts:

Location	8086 Version	V30 Version
U79	8086 microprocessor	V30 microprocessor
U11	8284A clock generator	UPD71011C clock generator
U21	30MHz crystal oscillator	20MHz crystal oscillator
U22	24MHz crystal oscillator	16MHz crystal oscillator

The Multibus interface circuitry supports both 20- and 24-bit addressing and includes full multi-master capabilities to allow the user to have several processor boards and DMA devices on the bus at one time. The circuitry also allows other Multibus masters to access the on-board dual-port RAM in the slave mode, requiring arbitration for both local and external accesses to the dual-port RAM. The on-board JEDEC sockets and I/O devices are not accessible through the Multibus interface, and therefore, on-board accesses to these resources do not require bus arbitration.

Four JEDEC sockets (referred to as EPROM sockets), allow EPROM, static RAM, and EEPROM devices to be installed. The sockets must be used in pairs because the 8086 processor has a 16-bit data bus. For normal operation, one pair of sockets must contain EPROM to support the initialization of the 8086 and optional 8087 after reset. The 32-pin sockets accept 2732, 2764, 27128, 27256, 27512, 27010, 27020 EPROM devices or 8Kx8, 32Kx8, or 128Kx8 static RAM and EEPROM devices. However, the 28-pin sockets will accept only 2732, 2764, 27128, 27256, and 27512 EPROM devices or 8Kx8 or 32Kx8 static RAM and EEPROM devices.

The sockets are mapped into the upper region of each of the 16 possible 1-megabyte pages or can be mapped into page 0 only, causing accesses to all areas in megabyte pages 1 through 15 to be routed to the Multibus.

The serial port consists of an 8251A USART and 1488/1489 RS-232 compatible drivers and receivers. Counter 2 of the 8253-5 can be jumper selected to drive the receive and transmit clocks for 8251A. Otherwise, the clock inputs are driven by the RS-232 SEC TxC signal. The RTS input may be connected to the CTS output of the 8251A if the external device does not support RTS. This ensures that CTS is active when data is ready to be transmitted by the 8251A.

The remaining two counters in the 8253-5 are jumper selectable as interrupt inputs to the 8259A Programmable Interrupt Controller, or they can be software polled. These counters are effective for providing timeouts that are independent of processor speed.

The 8259A has 27 jumper-selectable inputs, including the 8 Multibus interrupt-request signals. You can use the 8259A in either a direct 8-interrupt input scheme or a master/slave bus-vectored mode, which can provide up to 64 different interrupt inputs. In bus-vectored mode, the on-board 8259A is the master and other 8259As or compatible devices act as slave controllers on other Multibus boards in the system.

The 8255A-5 Programmable Parallel Interface (PPI) provides 24 programmable parallel I/O lines, grouped into three software-programmable 8-bit I/O ports. The exact usage and direction of each port depends on the configuration commands issued to the PPI and the hardware implementation installed by the user. Four sockets and a jumper array are provided to allow the user to customize the interface between the PPI and the external connector.

The dynamic RAM array is composed of 256K memory chips. The array can be either half filled to provide the 128K, 256K, and 512K configurations or completely filled to provide the 1-megabyte configuration of the CDSBC 21/8635-E board. Every location of the dynamic RAM array is protected by a parity detection circuit. A parity error signal can be jumper selected to drive the 8259A interrupt controller or the Non-Maskable Interrupt input of the 8086. Two LEDs display the parity error location by giving a high-byte and low-byte identification.

The RAM array has a PROM-based memory address selection circuit for Multibus (slave) accesses, which accommodates the different memory sizes and addressing schemes available on the CDSBC 21/8635-E. This PROM simplifies address selection for Multibus accesses and allows the mapping of none, a portion, or all of the on-board memory to the Multibus interface. The circuit supports both 20- and 24-bit addressing and the INH1 function.

For local accesses, the RAM is mapped from 0 to the top of RAM in each of the 16 possible 1-megabyte pages or can be mapped in page 0 only, causing accesses to all of megabyte pages 1 through 15 to be routed to the Multibus. In addition, a Status register bit can be written to temporarily disable internal access to a portion or all of the dual-port RAM, forcing Multibus accesses.

A Status register provides eight control outputs, five of which are configurable, while the other three are dedicated. The Status register outputs drive two user-definable status LEDs and allow the user to enable or disable seven different hardware features under software control. One of these is the Megabyte Page register, which drives the upper four Multibus address lines and selects one of the 16 possible megabyte pages. The register can be preset and either enabled or disabled by issuing I/O writes to the Status register.

3. Programming

The CDSBC 21/8635-E contains four programmable peripheral devices, a Status register, a Megabyte Page register, an Edge-Triggered Interrupt latch, and up to two SBX modules. These devices are I/O mapped as follows:

Address	Device
C0H or C4H	8259A Register 1
C2H or C6H	8259A Register 2
C8H	8255A-5 Port A
CAH	8255A-5 Port B
CCH	8255A-5 Port C
CEH	8255A-5 Control (Write Only)
D0H	8253-5 Counter 0
D2H	8253-5 Counter 1
D4H	8253-5 Counter 2
D6H	8253-5 Control (Write Only)
D8H or DCH	8251A Data
DAH or DEH	8251A Status/Control
C0H-C6H (even)	Edge-Triggered Interrupt Reset and Parity Error LED Clear (Word Write)
C9H-DFH (odd)	Status/Megabyte Page Register
80H-8EH (even)	SBX1 low-byte transfer (both 8- and 16-bit modules) or word transfer (16-bit modules); activates SBX1CS0 (and SBX1CS1 for 16-bit modules).
81H-8FH (odd)	SBX1 high-byte transfer (16-bit modules only); activates SBX1CS1.
90H-9EH (even)	SBX1 high-byte transfer (8-bit modules only); activates SBX1CS1.

Address	Device
A0H-AEH (even)	SBX2 low-byte transfer (both 8- and 16-bit modules) or word transfer (16-bit modules); activates SBX2CS0 (and SBX2CS1 for 16-bit modules).
A1H-AFH (odd)	SBX2 high-byte transfer (16-bit modules only); activates SBX2CS1.
B0H-BEH (even)	SBX2 high-byte transfer (8-bit modules only); activates SBX2CS1.

Status/Megabyte Page Register

The Status register is changed by performing an I/O byte write to any of the listed addresses. Data bit 11 is written to the Status register output selected by the binary value of data bits 8-10. The Megabyte Page register is enabled when output 7 of the Status register is low. When it is enabled, data bits 12-15 are latched (inverted) into the Megabyte Page register.

All Status and Megabyte Page register bits are cleared when the board is reset. The following chart lists the data values required to perform the various tasks as indicated:

Value	Description
X0H	With jumper at J11-1&2, 8253 GATE0=0 or STQ0=0 (for RAM disable control)
X1H	With jumper at J12-1&2, 8253 GATE1=0
X2H	With jumper at J14, 8086 NMI input disabled
X3H	With jumper at J58, dual-port RAM not overridden (Multibus accesses to it are allowed unless LOCK/ is active.)
X4H	With jumper at J15, BIO1 output inactive
X5H	BIO2 output inactive and LED DS1 off
X6H	LED DS2 off
X7H	Megabyte Page register enabled; data bits 4-7 are written to Megabyte Page register until turned off.
X8H	With jumper at J11-1&2, 8253 GATE0=1 or STQ0=1 (for RAM disable control)

Value	Description
X9H	With jumper at J12-1&2, 8253 GATE1=1
XAH	With jumper at J14, 8086 NMI input is enabled.
XBH	With jumper at J58, dual-port RAM is overridden (Multibus accesses to it are not allowed).
XCH	With jumper at J15, BIO1 output active
XDH	BIO2 output active and LED DS1 on
XEH	LED DS2 on
XFH	Megabyte Page register disabled

Programmable Devices

Information on the 8251A, 8253-5, 8255A-5, and 8259A can be obtained from their data sheets, which are available from the manufacturers of the devices.

4. Installation

Unpacking the Product

Immediately upon receipt, inspect the shipping carton for evidence of mishandling during transit. If the carton or its contents are damaged, report this as soon as possible to the carrier, who should instruct you further about how to file a damage claim. Some carriers, for instance, must receive a written notice of damage within 15 days after delivery.

It is always wise to save shipping cartons and all packing materials, in case of carrier inspection or future reshipment.

Service and Repair Assistance

For service and repair assistance, call Central Data at (217) 359-8010.

Always contact Central Data and request a Returned Materials Authorization (RMA) before returning a product for service or repair. When you call, have the following information ready:

1. Part and serial number of the board
2. Purchase order number for repair and shipping charges
3. Your shipping and billing address
4. Your contact name and telephone number

If the product is being returned due to damage during shipment or the product is out of warranty, a purchase order is required before repairs can be initiated. Before shipping, remove all user modifications. Be sure to protect the equipment adequately from any damage in transit. Remember the following:

1. Boards should be placed in anti-static bags.
2. Allow room in the box for protective padding.
3. Forward the product and all correspondence to:

Central Data Corporation
RMA # _____
1602 Newton Drive
Champaign, IL 61821-1098

Damage sustained due to improper packaging could result in extra repair charges.

Heat Dissipation

32W of heat (maximum) are dissipated by the CDSBC 21/8635-E Single-Board Computer. Sufficient air circulation must be provided to dissipate this heat and to help avoid heat damage to the board. The air surrounding the board must not rise above 55°C (131°F). Air flow of 200 linear feet per minute (minimum) adequately removes the heat generated by the board and keeps the air surrounding the board at a temperature less than the 55°C maximum.

Jumper Selections

This section of the manual provides a detailed description of each jumper on a circuit-by-circuit basis. Following these descriptions is a jumper cross-reference list, which compares the CDSBC 21/8635-E board with Intel 86/3X boards.

NOTE: In all charts showing jumper configuration options, a 1 indicates an installed jumper, while a 0 indicates a removed jumper.

For the CDSBC 21/8635-E jumper drawing, see Appendix C.

8086 TEST/ Input

The 8086 TEST/ input is connected to pin 2 of J55, as well as the TEST/ pin in the parallel I/O jumper array (J56-1). If the 8087 numeric data processor is installed, a jumper should be installed at J55-2&3. If the 8087 is not installed, the TEST/ input to the 8086 can be permanently enabled by installing jumper J55-1&2 (default), or it can be connected to another signal in the parallel I/O jumper array with J56 pin 1.

8086/8087 Clock and Reset Generation

The processor for the CDSBC 21/8635-E is the 8086-1 10MHz CPU; a socket is provided for an optional 8087 math coprocessor (U58). The 8086/8087 clock generator circuit generates the 5, 8, or 10MHz clock signals, as well as the various reset signals required by the CPUs and other on-board devices for initialization.

To select the 5MHz, 10MHz, or 8MHz CPU clock frequency, you must install a jumper at J60 pins 1&2, 3&4 (default), or 5&6, respectively. If the 8087 coprocessor is installed, it will be necessary to select a clock frequency within its specified operating range since this circuit provides the clock input for both devices.

For normal operations, you must install a jumper at J57-1&2, connecting the selected clock frequency from the 8284A clock generator to the CPU clock inputs. If you wish to operate from an external clock source, remove the jumper and connect the signal to pin 1 of J57.

The RESET output (pin 10) of the 8284A clock generator chip is produced at power-up due to the RC network (R3 and C87). RESET output can also be produced by installing a jumper at J89 (default) and providing an external AUX

RESET/ signal at P2 pin 38. When the AUX RESET/ input is used, a diode (D1) and a capacitor (C66) provide transient suppression and noise filtering for the external input.

JEDEC Device Selection

The JEDEC socket array allows you to install static RAM, EEPROM, IRAM, or EPROM memories. To accommodate the 16-bit data path required by the 8086, use the sockets in pairs (called banks). Sockets U45 and U47 form the lower addressed bank (Bank 0), while sockets U46 and U48 form the upper addressed bank (Bank 1). Within each bank of sockets, one socket contains the even data-byte (U45 and U46 contain D0-D7), while the other socket contains the odd data-byte (U47 and U48 contain D8-D15).

For normal operation, Bank 1 must contain EPROM to support the initialization of the 8086 processor, which jumps to address FFFF0H on reset.

A separate set of jumpers is provided to set the device type for each bank, which can be independently configured to accept 2732-27020 EPROMs or 8Kx8, 32Kx8, or 128Kx8 static RAMs/IRAMs/EEPROMs in the two 32-pin sockets. The 28-pin sockets, however, will accept only 2732-27512 EPROM devices or 8Kx8 or 32Kx8 static RAM/IRAM/EEPROM devices. The following chart illustrates the proper jumpers for each possible type and size of device:

Device Type	J64 J79	J66 J82	J76 J85	J75 J84	J83	J67	(Bank 0) (Bank 1)
2732 EPROM	N/C	N/C	1&2	N/C	3&4	N/C	
2764 EPROM	1&2	1&2	1&2	N/C	3&4	N/C	(default)
27128 EPROM	1&2	1&2	2&3	N/C	3&4	N/C	
27256 EPROM	1&2	1&2	2&3	1&2	3&4	N/C	
27512 EPROM	2&3	1&2	2&3	1&2	3&4	N/C	
27010 EPROM**	2&3	1&2	2&3	1&2	2&4	3&4	
27020 EPROM**	2&3	1&2	2&3	1&2	2&4	3&4	
8Kx8 SRAM	1&2	1&2	1&2	2&3	3&4	N/C	
32Kx8 SRAM	*	1&2	2&3	2&3	3&4	N/C	
128Kx8 SRAM**	2&3	1&2	2&3	2&3	2&4	2&4	
8Kx8 IRAM	1&2	2&3	1&2	2&3	3&4	N/C	

Notes: N/C = No Connection. Table lists pin numbers that should be shorted by adding a jumper or wire. J83 and J67 are for Bank 1 reference only. EEPROMs are configured like SRAMs of equal size.

* Add wire from J64-2 to J75-1 for Bank 0 or J79-2 to J84-1 for Bank 1.
** Bank 1 only

If IRAM devices are installed, you must remove J103; otherwise, leave J103 installed (default). If 2732 EPROMs are used, the data will appear twice within the range of F8000H-FBFFFH in Bank 0 or FC000H-FFFFFH in Bank 1.

JEDEC Address Decode

The JEDEC decode circuit consists of a 74F08 AND gate, a 16L8B PAL™, and four sets of jumpers (J32-J35). It generates the four chip-enable lines for the JEDEC sockets and maps the devices in each 1-megabyte page from the upper limit of the address space downward.

With a jumper installed at J35-2&3 (default), the JEDEC sockets will be mapped into each of the 16 possible 1-megabyte pages. If the jumper is moved to J35-1&2, the sockets will only be mapped into page 0.

Three JEDEC Size Select jumpers are provided to allow the circuit to correctly map devices ranging from 4Kx8 to 256Kx8. If different size devices are used in Banks 0 and 1, you must set the JEDEC Size Select jumpers according to the size of the largest device used (either Bank 0 or Bank 1). The circuit will then map an area as indicated below. Therefore, if 16Kx8 devices are installed in Bank 1 and 8Kx8 devices are installed in Bank 0, a total of 64K will be mapped (F0000H-FFFFFH), with the devices in Bank 0 repeating two times in the address range of F0000H-F7FFFH, while the devices in Bank 1 appear once in the address range of F8000H-FFFFFH.

The circuit always maps all four sockets (whether they are used or not) based on the device size, as indicated by the EPROM Size Select jumpers as follows:

J34	J33	J32	Size of Device	Memory Mapped	U45 PRM0L	U47 PRM0H	U46 PRM1L	U48 PRM1H
0	1	1	8Kx8 (Default)	32K	F8000H-FBFFEH	F8001H-FBFFFH	FC000H-FFFFEH	FC001H-FFFFFH
0	1	0	16Kx8	64K	F0000H-F7FFEH	F0001H-F7FFFH	F8000H-FFFFEH	F8001H-FFFFFH
0	0	1	32Kx8	128K	E0000H-EFFFEH	E0001H-EFFFFH	F0000H-FFFFEH	F0001H-FFFFFH
0	0	0	64Kx8	256K	C0000H-DFFFEH	C0001H-DFFFFH	E0000H-FFFFEH	E0001H-FFFFFH
1	0	0	128Kx8* 64Kx8**	384K	A0000H-BFFFEH	A0001H-BFFFFH	C0000H-FFFFEH	C0001H-FFFFFH
1	1	1	256Kx8* 64Kx8**	640K	60000H-7FFFEH	60001H-7FFFFH	80000H-FFFFEH	80001H-FFFFFH
1	1	0	256Kx8*	512K	----- -----	----- -----	80000H-FFFFEH	80001H-FFFFFH

* Bank 1
** Bank 0

On-Board Dual-Port Address Decode
This circuit decodes the on-board (local) accesses to the dual-port RAM, then maps the RAM from 0 to its maximum address (as defined by the RAM Size Select jumpers J25-J26) or the bottom of the JEDEC addressing space, whichever is lower. The circuit consists of a 16L8B PAL, a 74F11 AND gate, and five sets of jumper pins (J25-J28 and J30).

Since the total on-board address space is limited to 1 megabyte by the 8086 CPU and up to 1 megabyte of dual-port RAM can be installed in the board, it is possible for the JEDEC space to overlap the dual-port RAM. If this condition exists, the PRMACC/ signal serves to deselect on-board accesses to the dual-port RAM, thus preventing device contention. This makes the portion of the dual-port RAM that overlaps the JEDEC space inaccessible to the on-board CPU. Note that since Multibus masters cannot access the on-board JEDEC devices, there is no conflict for Multibus accesses; therefore, they are not restricted.

The RAM Size Select jumpers configure the board for one of seven possible amounts of dual-port RAM as follows:

For 128K, 256K, or 512K Boards:

J26	J25	RAM Size	Range
1	1	128K	0-1FFFFH
1	0	256K	0-3FFFFH
0	1	512K	0-7FFFFH

For 1-Megabyte Boards:

J26	J25	RAM Size	Range
1	1	640K	0-9FFFFH
1	0	768K	0-BFFFFH
0	1	896K	0-DFFFFH
0	0	1M	0-FFFFFH

With a jumper installed at J30-2&3 (default), the dual-port RAM will be mapped into the lower portion of each of the 16 possible 1-megabyte pages (for local accesses). If the jumper is installed at J30-1&2, the dual-port RAM will only be mapped into page 0.

The RAMDIS signal can be set or cleared by issuing I/O writes to Status register bit 0. In conjunction with jumper J28, this signal serves to disable local accesses to portions of the on-board dual-port RAM as shown below. (J28 is removed in the default configuration.)

RAMDIS Signal	J28	0H-1FFFFH	20000H to Top of RAM	Top of RAM to Start of JEDEC
0	X	On-board	On-board	Off-board
1	1	Off-board	Off-board	Off-board
1	0	On-board	Off-board	Off-board

Status Register Enable Jumper
If the Status register and/or the Edge-Triggered Interrupt flip-flop are required, you must install a jumper at J44. The SREGEN/ signal enables data transfers to the Status/Megabyte Page registers, while the LVCLR/ signal clears the Edge-Triggered Interrupt flip-flop, the parity error LEDs, and the DPERR signal.

Status Register and Megabyte Page Register Options
The Status register is a 74LS259 8-bit addressable latch that provides seven general-purpose control outputs and one additional output, which controls the loading of the Megabyte Page register.

The seven control outputs of the Status register each have one or more possible functions (as described in the following paragraphs), or each can be configured as a user-specified control line (with the addition of a discrete wire).

Outputs 0 and 1 connect to the 3-pin jumper arrays J11 and J12, which provide the GATE0 and GATE1 control signals for counters 0 and 1 of the 8253-5 timer. In each case, if the timers are to be permanently enabled, install a jumper at pins 2 and 3. If the respective Status register output is to control the GATE input to the timer, install a jumper at pins 1 and 2.

Output 0 can also be used to generate the RAMDIS signal, which redirects local accesses from portions of the dual-port RAM to the Multibus when active. If output 0 is not to control the RAMDIS line, you should remove the jumper at J91 and install a jumper at J92, enabling local accesses to the dual-port RAM (default). If you want the RAMDIS line to be controlled by output 0, remove the jumper at J92 and install a jumper at J91. Jumper J93 then determines which polarity of output 0 enables or disables the RAM. With J93 installed, output 0 must be low for RAMDIS to be true, while with J93 removed, output 0 must be high for RAMDIS to be true. If you want the on-board RAM to be permanently disabled, remove both J91 and J92.

Output 2 of the Status register connects to jumper J14 and enables or disables the NMI MASK signal, as described later.

Output 3 of the Status register is inverted by a 74F240 inverter and connects to J58-1. If jumper J58 is installed, the OVERRIDE/ signal will be true when output 3 is high, locking the dual-port RAM to the local port and therefore preventing Multibus accesses.

Output 4 of the Status register connects to jumper J15. With this jumper installed, output 4 is inverted by a 7406 open collector inverter and is available in the interrupt matrix at J13-1. Pins 1 and 2 of J13 are user-definable outputs that can be hardwired to one of the Multibus interrupt lines (J1-J8) (allowing the user to generate Multibus interrupts under software control) or to other sections of the board as general-purpose control outputs.

Output 5 of the Status register is inverted by two 7406 drivers, one of which drives J13-2 in the interrupt matrix, with the other driving a user-definable LED (0=off, 1=on).

Output 6 of the Status register is inverted by a 7406 that drives a user-definable LED (0=off, 1=on).

Output 7 controls the loading of the Megabyte Page register. When output 7 is low, the Megabyte Page register will be updated during any I/O write to the Status register, including the cycle that sets output 7 low. When output 7 is high, the Megabyte Page register will not be updated when the Status register is updated, including the write operation that sets output 7 high.

The Megabyte Page register holds the upper four Multibus address lines (A20-A23). J94 selects between 20- and 24-bit addressing for Multibus accesses from the local 8086 CPU. With jumper J94 removed, 24-bit addressing is selected; if installed, 20-bit addressing is selected.

Timebase Enable Jumper

Five of the clock frequencies used on the CDSBC 21/8635-E boards are produced by a timing circuit consisting of a 19.6608MHz crystal oscillator and a 74LS393 8-bit binary counter. For normal operation, the jumper must be installed at J86-1&2 to

connect the crystal oscillator output to the counter input. The circuit produces the following clock outputs:

Output Frequency	Timebase Output Function
9.8304MHz	Multibus BCLK, CCLK Source
2.4576MHz	8251A USART Clock
1.23MHz	8253-5 Timer Clock
153.6KHz	8253-5 Timer Clock
76.8KHz	Refresh Timer

Programmable Timer Options

The programmable timer circuit consists of an 8253-5 programmable timer and two jumper arrays (J59 and J61). The circuit provides three independent 16-bit counters, one of which provides the clock input to the 8251A USART, while the other two are intended as hardware timers for interrupt generation, producing the T0INT and T1INT signals.

Each counter is a 16-bit down-counter that can be preset and can operate in either binary or BCD mode. Each counter has a CLK input, a GATE input, and an OUT signal, all of which can be independently software and hardware configured for one of five modes of operation described in the databook for this component.

Although the clock input to each counter can be hardwired to any available on-board frequency source less than 2.6MHz, jumper array J59 allows jumper selection of the default clock frequencies for each counter as follows:

Counter	Jumper Pins	Frequency Input
0	J59-1&2	1.23MHz
1	J59-3&4	153.6KHz
2	J59-5&6	1.23MHz

As previously described, the GATE inputs for counters 0 and 1 connect to the GATE0 and GATE1 jumper arrays (J11 & J12), which allow the inputs for these counters either to be tied high (enabled) or to be dynamically controlled by status register outputs. For normal operation, the GATE input for counter 2 is tied high through a pull-up resistor, but if desired, it can be hardwired to any on-board control output.

For timer interrupt operations, the outputs of counters 0 and 1 connect to pins 3 and 4 of J42 in the interrupt jumper matrix. Either output can also provide the EXTCLK signal for the parallel I/O jumper array (J56-16). The output from counter 2 connects to the 8251A Clock Select jumper array, which configures the Transmit and Receive Clock inputs for the 8251A USART.

Serial Interface Options
The serial interface circuit consists of an 8251A USART, six jumper arrays for hardware configuration (J63 and J70-J74), a 1488 line driver, and a 1489 line receiver.

On-board jumper arrays are provided for configuration of the Transmit Clock, Receive Clock, and Data Set Ready inputs. Jumper array J74 connects the 8251A TxC and RxC inputs to either the 8253-5 OUT2 signal (TxC=pins 3-5, RxC=pins 4-6) or the SEC TxC signal from the RS-232 interface (TxC=pins 1-3, RxC=pins 2-4).

When installed, jumper J70 connects the Data Terminal Ready signal from the RS-232 interface to the Data Set Ready input of the 8251A.

With J73 installed, the 2.4576MHz clock signal drives the STXD line in the parallel port jumper array (J56-19) and J72-1. If J73 is not installed, an external clock signal from the parallel port jumper array can be connected to STXD.

J72 selects either the STXD signal (J72-1&2) or the RxC signal (J72-2&3) as an input to the line driver whose output drives pin 1 of J71. This output can be connected to either the Secondary Receive output (J71-1&2), the Secondary Clear To Send output (J71-1&3), or the Transmit Signal Element Timing output (J71-1&4).

Finally, you can connect the RS-232 CTS signal to the RS-232 RTS signal by jumpering J63. This is useful for connection with devices that do not drive RTS.

Parallel I/O Interface Options
The parallel I/O interface consists of an 8255A-5 Programmable Peripheral Interface, a 74AS640 8-bit bidirectional transceiver, four 14-pin IC sockets, and two jumper arrays for configuration (J54 and J56). These sockets correlate exactly to the sockets on the Intel 86/3X boards as follows:

21/8635-E Location	Intel 86/3X Location	Signals
U12	U19	PC0-PC3
U13	U18	PC4-PC7
U14	U20	PB0-PB3
U15	U21	PB4-PB7

The 8255A-5 PPI provides 24 programmable parallel I/O lines, grouped into three software-programmable 8-bit I/O ports. The exact usage and direction of each port depends on the configuration commands issued to the device, the external devices installed in the sockets, and the configuration jumpers/wires installed at J54 and J56.

A 74AS640 transceiver provides buffering for Port A, which is a bidirectional I/O port. You can control the direction of data flow through the transceiver by connecting J56-25&26 for Receive, leaving it open for Transmit, or connecting it to another control signal for dynamic direction control.

Sockets U14 and U15 buffer Port B, while U12 and U13 buffer Port C. The 14-pin sockets can be bypassed with shorting plugs if desired and are configured to accept the following line drivers (for output) or terminating resistor packs (for input):

Device	Type	Output Configuration	Output Current
7400	Inverting	Totem Pole	16mA
7403	Inverting	Open Collector	16mA
7408	Non-inverting	Totem Pole	16mA
7409	Non-inverting	Open Collector	16mA
7437	Inverting	Totem Pole	48mA
7438	Inverting	Open Collector	48mA
SBC901	220 ohm pullup/ 330 ohm pulldown	---	---
SBC902	1K pullup	---	---

Jumper array J56 and two spare wire-wrap pins (J54) are provided to configure Port C as required by the user and to configure the direction control mechanism for Port A as previously described. The jumper array is configured as follows:

Pin	Description
J56-1	8086 TEST/ Input
J56-2	8255A-5 PC7 Output
J56-3	PC7 Driver/Terminator Socket
J56-4	PA Interrupt Source
J56-5	8255A-5 PC6 Output
J56-6	PC6 Driver/Terminator Socket
J56-7	PB Interrupt Source
J56-8	8255A-5 PC5 Output
J56-9	PC5 Driver/Terminator Socket
J56-10	Spare Wire-Wrap Post J54-1
J56-11	8255A-5 PC4 Output
J56-12	PC4 Driver/Terminator Socket
J56-13	Spare Wire-Wrap Post J54-2
J56-14	8255A-5 PC0 Output
J56-15	PC0 Driver/Terminator Socket
J56-16	EXTCLK
J56-17	8255A-5 PC1 Output
J56-18	PC1 Driver/Terminator Socket
J56-19	STXD
J56-20	8255A-5 PC2 Output
J56-21	PC2 Driver/Terminator Socket
J56-22	PFSN/
J56-23	8255A-5 PC3 Output
J56-24	PC3 Driver/Terminator Socket

NMI Enable/Disable Jumpers

The NMI signal ties to a pin in the interrupt matrix (J43-13). If desired, you can connect J43-13 to a positive true signal on the board, which will cause a non-maskable interrupt whenever the signal switches high. If the non-maskable interrupt is not used, J43-13 should be connected to J43-14 (ground), preventing spurious interrupts (default).

The NMIMSK/ signal allows the user to enable or disable the NMI function from software. If jumper J14 is removed, the NMIMSK/ line will always be high and the NMI interrupt will be enabled. If J14 is installed, the NMI function will be controlled by output 2 of the Status register (0=disabled, 1=enabled).

8086 Interrupts

The interrupt circuitry consists of an 8259A Programmable Interrupt Controller, an interrupt jumper matrix (J40-J43), a 74LS240 octal inverting buffer, and some miscellaneous support circuitry. The 8259A handles up to eight bus-vectored or non-bus-vectored interrupts, and the circuit supports up to 27 interrupt sources without external hardware.

The circuit supports non-maskable interrupts by allowing any of the 27 possible inputs to be connected to the NMI signal (J43-13).

The 8259A provides the vectored interrupt input to the 8086 CPU and supports on- or off-board non-bus-vectored interrupts, as well as off-board bus-vectored interrupts. Bus-vectored interrupts are cascaded from Multibus slave devices and require the CDSBC 21/8635-E board to gain control of the Multibus interface for each interrupt (which requires additional response time as compared to non-bus-vectored interrupts). If only non-bus-vectored interrupt operation is acceptable, remove jumper J27; if bus-vectored interrupts are desired, install J27.

The interrupt inputs 0-7 for the 8259A connect to J41 pins 1-8, respectively, and can be jumpered to any of the 27 possible interrupt sources in the array, as follows:

Signal Name	Jumper Pin	Description
MBINT0	J40-1	Buffered Multibus Interrupt 0
MBINT1	J40-2	Buffered Multibus Interrupt 1
MBINT2	J40-3	Buffered Multibus Interrupt 2
MBINT3	J40-4	Buffered Multibus Interrupt 3
MBINT4	J40-5	Buffered Multibus Interrupt 4
MBINT5	J40-6	Buffered Multibus Interrupt 5
MBINT6	J40-7	Buffered Multibus Interrupt 6
MBINT7	J40-8	Buffered Multibus Interrupt 7
PFI	J42-1	Power Fail Input from P2-19
MINT	J42-2	8087 Interrupt Output
T0INT	J42-3	Timer 0 Interrupt
T1INT	J42-4	Timer 1 Interrupt
PAINT	J42-5	PA Interrupt from 8255A-5 Matrix
PBINT	J42-6	PB Interrupt from 8255A-5 Matrix
RXINT	J42-7	8251A Receive Interrupt
TXINT	J42-8	8251A Transmit Interrupt
SBX2I0	J42-9	SBX2 Interrupt 0
SBX2I1	J42-10	SBX2 Interrupt 1
SBX1I0	J42-11	SBX1 Interrupt 0
SBX1I1	J42-12	SBX1 Interrupt 1
EXTIN	J42-13	External Interrupt from P4-49
DPERR	J42-14	Dual-Port Parity Error Interrupt
PLC	J43-1	PLC Input from P2-31
TIMEOUT/	J43-2	Timeout Interrupt
LVINT	J43-4	Edge-Triggered Interrupt
ORINT1	J43-5	4-Level OR Function Interrupt
ORINT2	J43-6	2-Level OR Function Interrupt

A 74F74 flip-flop is provided to convert positive edge interrupts into level interrupts. The clock input is connected to J43-3, while the output connects to J43-4. The flip-flop will be set by a positive transition on the clock input. If the flip-flop is used, install jumper J44 so that an I/O word write to addresses C0H-C6H will reset the interrupt.

If the 8259A is not initialized to operate in the edge-triggered mode, the TIMEOUT/ signal available at J43-2 must be routed through the Edge-Triggered flip-flop if the signal is to interrupt the 8086. TIMEOUT/ and AEN/ (at J53) can be ORed (as described below) before driving the flip-flop in order to prevent an interrupt when the 8086 executes a HALT instruction. To correctly OR the TIMEOUT/ and AEN/ signals:

1) Add a wire from J43-2 to J43-7.
2) Add a wire from J43-8 to J53-1.
3) Add a wire from J43-6 to J43-3.
4) Add a wire from J43-4 to the desired interrupt level.

A 74LS32 provides a 2-input OR function and a 4-input OR function to expand the interrupt capabilities of the board, as follows:

Jumper Pin	Description
J43-7	2-Input OR Function Input
J43-8	2-Input OR Function Input
J43-9	4-Input OR Function Input
J43-10	4-Input OR Function Input
J43-11	4-Input OR Function Input
J43-12	4-Input OR Function Input

Jumpers J9 and J10 connect the PFI and EXTIN signals, respectively, to the buffers that drive the interrupt matrix array.

SBX Bus Interface Options
Two SBX connectors (P5 and P6) are provided for optional system expansion using SBX add-on products. All required power lines, address lines, data lines, and control lines are provided through the two SBX connectors, which are treated as on-board I/O locations.

The SBX1 and SBX2 16-bit jumpers (J80 and J81, respectively) in the I/O address decode circuit choose either 16-bit (installed) or 8-bit (removed) operation for each SBX connector.

Two general-purpose control outputs from each SBX connector connect to wire-wrap pins on the CDSBC 21/8635-E board as follows:

SBX Connector	Signal Name	Wire-Wrap Pins
SBX1	SBX1O0	J62-2
SBX1	SBX1O1	J62-1
SBX2	SBX2O0	J29-2
SBX2	SBX2O1	J29-1

Wait-State Generator
The ready circuit provides the synchronized Ready input to the 8086/8087 CPUs. The circuit determines which resource is being accessed, and then generates the correct number of wait-states to guarantee accurate data transfers. The circuit supports transfers to four types of resources: JEDEC, I/O, dual-port RAM, and the Multibus. A bus timeout circuit is also provided.

For on-board JEDEC and I/O cycles, a wait-state generator is enabled and used to generate the PRMRDY and IORDY signals, which signify the end of their respective cycles. To select the number of wait-states for each type of cycle, install only one JEDEC jumper at J16-J19 and one I/O jumper at J20-J23 as follows:

Number of Wait-States	JEDEC Jumper	Maximum Device Access Time 5MHz	8MHz	10MHz
0	J16	515	290	215
1	J17	715	415	315
2	J18	915	540	415
3	J19	1115	665	515

Number of Wait-States	I/O Jumper	Maximum Device Access Time 5MHz	8MHz	10MHz
0	J20	350	200	150
1	J21	550	325	250
2	J22	750	450	350
3	J23	950	575	450

Note that the board is configured for 250ns JEDEC devices (J17) and 350ns I/O devices (J22) for use at 10MHz when shipped.

For local accesses to the dual-port RAM, a 3-pin jumper array (J36) selects the number of wait-states inserted. For normal operation, a jumper should be installed at J36-1&2, which will select zero-wait-state operation for uncontested dual-port RAM cycles. If the jumper is installed at J36-2&3, one wait-state will be inserted. For any contested accesses (due to refresh or Multibus cycles to the dual-port RAM), wait-states are automatically inserted until control of the RAM is gained by the 8086.

Multibus Dual-Port Address Decode
This circuit allows the user to select the amount of on-board dual-port RAM accessible by the Multibus and the Multibus address range in which it will reside.

The circuit supports two different addressing schemes, depending on the amount of on-board RAM installed. When 128K or 256K of on-board RAM is installed, an addressing scheme emulating the Intel 86/30 board is used. When 512K or 1 megabyte of on-board RAM is installed, an addressing scheme emulating the Intel 86/35 is used.

Both approaches support 20- or 24-bit addressing and allow you to restrict portions of the on-board RAM from Multibus use.

The circuit consists of a 16L2A PAL, a 27S281A 1Kx8 PROM, an 8-bit tri-state buffer, and 14 user-selectable jumpers.

Jumpers J96-J99 correlate to the upper four Multibus address lines (A20-A23) and determine the 1-megabyte page (of 16 possible) that the on-board memory will reside in for Multibus accesses. For systems requiring only 20-bit addressing, you must remove J101 (default), which causes the upper four address lines to be

ignored. Installing jumpers at J96-J99 selects the active state for the specific address line as follows:

J96	J97	J98	J99	Selected 1-Megabyte Page
0	0	0	0	0 (default)
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Jumpers J100 and J102 allow Multibus accesses to be disabled and determine the desired 512K boundary memory area for the CDSBC 21/8635-E, as shown below:

J100	J102	128K-256K Versions	512K-1M Versions
1	1	Select upper 512K boundary	Illegal
1	0	Disable Multibus requests	Disable Multibus requests
0	1	Select lower 512K boundary (default)	Illegal
0	0	Illegal	Enable Multibus requests (default)

J90 is a 3-pin jumper array that allows Multibus address line 18 to be included or ignored in the address selection process, as follows:

J90-1&2	J90-2&3	128K-256K Versions	512K-1M Versions
1	1	Illegal	Illegal
0	1	A18 is ignored	A18 is ignored (default)
1	0	Selects Upper 256K	Illegal
0	0	Selects Lower 256K (default)	Illegal

The Intel 86/30 includes A18 in the Multibus address decode circuit and therefore does not allow the selected address range to cross a 256K boundary. If J90-2&3 is not installed, J90-1&2 determines the 256K boundary, as indicated. With J90-2&3

installed, A18 is ignored, allowing the selected Multibus range to fall anywhere within the selected 512K address range.

The translation PROM determines the amount of on-board RAM available to the Multibus and the specific Multibus address range in which it will reside. When emulating the Intel 86/30, the PROM also performs address translation (as explained in a later section of this chapter).

Depending on the amount of dual-port memory installed, three different translation PROMs and two different DP Decode PALs are used as shown below:

Amount of Memory	Translation PROM Part Number	DP Decode PAL Part Number
128K	240612	240191
256K	240611	240191
512K	240610	240191
1M	240610	240265

Intel 86/30 Emulation

When either 128K or 256K of on-board dual-port RAM is installed, the translation PROM emulates the addressing scheme used by the Intel 86/30 board.

As previously explained, the PAL selects one of sixteen possible 1-megabyte pages (24-bit addressing) and/or one of two 512K segments within that page. The PAL can also select one of two 256K segments within the 512K segment. The translation PROM and user configurable jumpers determine where in the selected 512K (or 256K) address range the on-board RAM will reside.

This is accomplished by specifying both the amount (or size) of the total on-board memory to be mapped in the Multibus address range, as well as the ending address within the selected 512K (or 256K) address range.

The amount of on-board memory available to the Multibus is selected by jumpers J45 and J47 as follows:

J45-1&2	J47	Amount of On-Board RAM Available to Multibus
1	1	Top 1/4 of on-board RAM
1	0	Top 1/2 of on-board RAM
0	1	Top 3/4 of on-board RAM
0	0	All of on-board RAM (default)

If less than the full amount of on-board RAM is available to the Multibus, the PROM provides the address translation required to map the uppermost sections of the on-board memory to the selected Multibus address range. Jumpers J48-J51

select 1 of 16 possible 32K ending addresses within the 512K (or 256K) range as follows:

J48	J49	J50	J51	Selected Multibus Ending Address
1	1	1	1	07FFFH
1	1	1	0	0FFFFH
1	1	0	1	17FFFH
1	1	0	0	1FFFFH (default for 128K board)
1	0	1	1	27FFFH
1	0	1	0	2FFFFH
1	0	0	1	37FFFH
1	0	0	0	3FFFFH (default for 256K board)
0	1	1	1	47FFFH
0	1	1	0	4FFFFH
0	1	0	1	57FFFH
0	1	0	0	5FFFFH
0	0	1	1	67FFFH
0	0	1	0	6FFFFH
0	0	0	1	77FFFH
0	0	0	0	7FFFFH

Note that the ending address selected must be greater than the amount of memory selected, if all of the selected memory is to be available to the Multibus. For example, if a size of 64K (e.g., top 1/4 of a 256K board) is selected with an ending address of 07FFFH, only 32K will be mapped.

You can determine the starting Multibus address (within the 512K or 256K segment) by subtracting the selected size from the ending address, as shown in the examples below.

Selected Size	Selected Multibus Ending Address	Resulting Multibus Starting Address	Amount of Memory Mapped
32K	37FFFH	30000H	32K
64K	2FFFFH	20000H	64K
96K	07FFFH	00000H	32K*

* Cannot cross 512K boundary

Intel 86/35 Emulation

When either 512K or 1 megabyte of on-board dual-port RAM is installed, the translation PROM emulates the addressing scheme used by the Intel 86/35 board.

As previously explained, the PAL selects 1 of 16 possible 1- megabyte pages (24-bit addressing), while the translation PROM determines where in the selected 1-megabyte page the on-board RAM will reside. With either 512K or 1 megabyte of RAM installed, you must install jumper J45-2&3 to connect Multibus address line A19 to the translation PROM. Addresses are selected with jumpers J47-J51 as follows:

J47	J48	Multibus Starting Address Within Page
1	1	40000H
1	0	20000H
0	1	10000H
0	0	0H (default)

J49	J50	J51	Multibus Ending Address Within Page
1	1	1	FFFFFH (default for 1M board)
1	1	0	EFFFFH
1	0	1	DFFFFH
1	0	0	CFFFFH
0	1	1	BFFFFH
0	1	0	AFFFFH
0	0	1	9FFFFH
0	0	0	7FFFFH (default for 512K board)

When emulating the Intel 86/35, the board performs no addressing translation. If only 512K of on-board RAM is installed, you must select an ending address of 7FFFFH.

Multibus Interface Jumpers

The Multibus Interface and Control circuitry allows the on-board 8086 CPU to access off-board system resources through the Multibus interface.

The following five jumpers determine the arbitration technique used by the 8289 Bus Arbiter:

* BPRO (J38)
* HPRQ ONLY (J37)
* CBRQ (J46)
* BCLK (J39)
* CCLK (J52)

The BPRO jumper (J38) must be installed if a serial bus priority resolution scheme is used (default), but removed if a parallel priority scheme is used. If installed, the Multibus BPRO (bus priority out) line is driven by the 8289 Bus Arbiter.

The HPRQ Only jumper (J37) and the CBRQ jumper (J46) work together to determine the exact priority technique employed. If J37 is installed, the CBRQ input is ignored and the bus will only be relinquished to a higher priority device. If the HPRQ Only jumper is removed and a jumper is installed at J46-1&2 (default), bus control will be relinquished each time the CBRQ line is activated, allowing lower priority devices to be serviced. If a jumper is installed at J46-2&3 (with J37 removed), the CDSBC 21/8635-E will be forced to surrender the bus after each bus cycle.

If installed (default), the BCLK (J39) and CCLK (J52) jumpers cause the board to provide the Multibus bus clock and constant clock signals.

With jumper J88 installed, the ALE signal is routed to pin 32 of the P2 connector (default).

The timeout circuit consists of a 74LS123 re-triggerable one-shot with an R/C network setting its nominal output pulse width to 2ms. The output (TIMEOUT/) connects to J43-2 in the interrupt matrix and can also be used to generate an 8086 interrupt. If J24 is installed (default), the TIMEOUT/ signal will be driven low during a timeout condition, activating the READY signal and thus terminating the cycle.

J104 should be installed to enable LOCK/ to be routed to the Multibus (default is not to route LOCK/ to Multibus). To bypass the inductor and diode in the LOCK/ signal path, install jumper J107.

Power Supply Voltage Jumpers
Jumpers J77 and J78 connect the battery power-plane to the +5V power-plane. If external battery backup is not provided, a jumper must be installed at both J77 and J78. If battery backup operation is desired, remove jumpers J77 and J78, wire the feed-through at J106-1 to the feed-through at J106-2, and provide battery backup voltage at pins 3 and 4 of P2.

If installed, jumpers J65, J68, and J69 connect -12V, +12V, and +5V to pins 20, 21, and 24, respectively, of the P3 serial interface connector.

MPRO/ Jumper
If battery backup operation is desired, install jumper J87, which connects the MPRO/ signal from P2-20 to the PWRDWN/ line and prevents dual-port RAM read/write operations when active.

I/O Offset Jumper
Installing jumper J105 will cause all on-board I/O addresses to be offset (increased) by 400H. With J105 removed (default), the I/O addresses are as detailed in this manual.

CDSBC 21/8635-E to Intel 86/3X Cross-Reference

Default jumpers are factory-installed and are marked with an asterisk (*) below. If asterisks appear on two consecutive lines that represent individual pins, then those pins are connected when shipped (e.g., J11-2 and J11-3). Defaults for jumpers not listed in these tables are given in the written description of the jumpers.

Status/Megabyte Page Register Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J11-1	E29	Status Register Output 0
J11-2*	E28	8253-5 GATE0 Input
J11-3*	E32	Pullup for GATE0
J12-1	E35	Status Register Output 1
J12-2*	E31	8253-5 GATE1 Input
J12-3*	E30	Pullup for GATE1
J14-1&2*	E27-E26	Enable NMI MASK/ Signal from Output 2
J15-1&2	E25-E24	Enable Multibus Interrupt Driver Input from Output 4
J44-1&2*	E43-E42	Enable Status Register and Edge-Triggered Interrupt
J58-1&2*	E22-E23	Enable Dual-port Override
J91-1&2	E298-E297	Enable RAM Disable Control Output
J92-1&2*	E239-E238	Disable RAM Disable Control Output
J93-1&2	E227-E219	RAM Disable Polarity Select
J94-1&2*	N/A	20-bit Master Select

8253-5 Timer Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J59-1*	E175	8253-5 CLK0 Input
J59-2*	E176	1.23MHz (for CLK0)
J59-3*	E185	8253-5 CLK1 Input
J59-4*	E184	153.6KHz (for CLK1)
J59-5*	E179	8253-5 CLK2 Input
J59-6*	E178	1.23MHz (for CLK2)
J61-1	E181	8253-5 OUT0 for EXTCLK
J61-2	E182	EXTCLK Output
J61-3	E180	8253-5 OUT1 for EXTCLK
J86-1&2*	E84-E85	Timebase Enable

Serial Interface Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J63-1	E77	RS-232 CTS signal
J63-2	E76	RS-232 RTS signal
J70-1&2*	E193-E189	RS-232 DTR to 8251A DSR
J71-1	E79	Spare Line Driver Output
J71-2	E78	Secondary Receive Output Pin
J71-3	E81	Secondary CTS Output Pin
J71-4	E80	Transfer Signal Element Timing Output Pin
J72-1	E196	STXD Signal
J72-2	E192	Spare Line Driver Input
J72-3	E188	8251 RxC Clock
J73-1&2	E183-E177	2.4576MHz Clock drives STXD
J74-1	E186	Secondary Transmit Clock (for 8251A TxC)
J74-2	E187	Secondary Transmit Clock (for 8251A RxC)
J74-3*	E190	8251A TxC Input
J74-5*	E194	8253-5 OUT2
J74-4*	E191	8251A RxC Input
J74-6*	E195	8253-5 OUT2

Parallel Interface Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J56-1	E62	8086 TEST/ Input
J56-2*	E53	8255A-5 PC7 Output
J56-3*	E44	PC7 Driver/Terminator Socket
J56-4	E63	PA Interrupt Source
J56-5*	E54	8255A-5 PC6 Output
J56-6*	E45	PC6 Driver/Terminator Socket
J56-7	E64	PB Interrupt Source
J56-8*	E55	8255A-5 PC5 Output
J56-9*	E46	PC5 Driver/Terminator Socket
J56-10	E65	Spare Wire-wrap Post J54-1
J56-11*	E56	8255A-5 PC4 Output
J56-12*	E47	PC4 Driver/Terminator Socket
J56-13	E66	Spare Wire-wrap Post J54-2
J56-14*	E57	8255A-5 PC0 Output
J56-15*	E48	PC0 Driver/Terminator Socket

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J56-16	E67	EXTCLK
J56-17*	E58	8255A-5 PC1 Output
J56-18*	E49	PC1 Driver/Terminator Socket
J56-19	E68	STXD
J56-20*	E59	8255A-5 PC2 Output
J56-21*	E50	PC2 Driver/Terminator Socket
J56-22	E69	PFSN/
J56-23*	E60	8255A-5 PC3 Output
J56-24*	E51	PC3 Driver/Terminator Socket
J56-25*	E61	Ground (for Direction Control)
J56-26*	E52	Transceiver Direction Control Input

Interrupt Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J1	E246	Multibus Interrupt 7 Line
J2	E247	Multibus Interrupt 6 Line
J3	E248	Multibus Interrupt 5 Line
J4	E249	Multibus Interrupt 4 Line
J5	E250	Multibus Interrupt 3 Line
J6	E251	Multibus Interrupt 2 Line
J7	E252	Multibus Interrupt 1 Line
J8	E253	Multibus Interrupt 0 Line
J9-1&2*	N/A	Enable PFI Input
J10-1&2	E19-E20	Enable EXTIN Input
J13-1	E244	Multibus Interrupt Out 1 Buffer Output
J13-2	E245	Multibus Interrupt Out 2 Buffer Output
J27-1&2*	E34-E33	Enable Bus-vectored Interrupts
J40-1	E160	Buffered Multibus Interrupt 0
J40-2	E149	Buffered Multibus Interrupt 1
J40-3	E148	Buffered Multibus Interrupt 2
J40-4	E159	Buffered Multibus Interrupt 3
J40-5	E162	Buffered Multibus Interrupt 4
J40-6	E151	Buffered Multibus Interrupt 5
J40-7	E150	Buffered Multibus Interrupt 6
J40-8	E161	Buffered Multibus Interrupt 7
J41-1	E165	8259A Interrupt 0 Input
J41-2	E164	8259A Interrupt 1 Input
J41-3	E147	8259A Interrupt 2 Input
J41-4	E136	8259A Interrupt 3 Input
J41-5	E157	8259A Interrupt 4 Input
J41-6	E152	8259A Interrupt 5 Input
J41-7	E155	8259A Interrupt 6 Input

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J41-8	E134	8259A Interrupt 7 Input
J42-1	E168	Power Fail Input from P2-19
J42-2	E166	8087 Interrupt Output
J42-3	E158	Timer 0 Interrupt
J42-4	E141	Timer 1 Interrupt
J42-5	E132	PA Interrupt from 8255-A Matrix
J42-6	E143	PB Interrupt from 8255-A Matrix
J42-7	E153	8251A Receive Interrupt
J42-8	E154	8251A Transmit Interrupt
J42-9	E137	SBX2 Interrupt 0
J42-10	E126	SBX2 Interrupt 1
J42-11	E156	SBX1 Interrupt 0
J42-12	E169	SBX1 Interrupt 1
J42-13	E129	External Interrupt from P4-49
J42-14	E167	Dual-port Parity Error Interrupt
J43-1	E163	PLC Input from P2-31
J43-2	E133	Timeout Error Interrupt
J43-3	E135	Edge-triggered Flip-flop Input
J43-4	E146	Edge-triggered Interrupt
J43-5	E130	4-Level OR Function Interrupt
J43-6	E128	2-Level OR Function Interrupt
J43-7	E138	2-Input OR Function Input
J43-8	E140	2-Input OR Function Input
J43-9	E131	4-Input OR Function Input
J43-10	E142	4-Input OR Function Input
J43-11	E139	4-Input OR Function Input
J43-12	E127	4-Input OR Function Input
J43-13*	E145	NMI Signal
J43-14*	E144	NMI Disable (Ground)

* J41-3 is jumpered to J42-3, and J40-6 is jumpered to J41-6 in the default configuration.

SBX Connector Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J29-1	E171	SBX2 Option 1 Wire-wrap Post
J29-2	E170	SBX2 Option 0 Wire-wrap Post
J62-1	E122	SBX1 Option 1 Wire-wrap Post
J62-2	E121	SBX1 Option 0 Wire-wrap Post
J80-1&2	E174-E173	SBX1 16-bit Select
J81-1&2	E172-E173	SBX2 16-bit Select

Wait-State Generator Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J16-1&2	E8-E4	JEDEC 0-Wait-state Select
J17-1&2*	E9-E5	JEDEC 1-Wait-state Select
J18-1&2	E11-E7	JEDEC 2-Wait-state Select
J19-1&2	E10-E6	JEDEC 3-Wait-state Select
J20-1&2	N/A	I/O 0-Wait-state Select
J21-1&2	E13-E12	I/O 1-Wait-state Select
J22-1&2*	E13-E14	I/O 2-Wait-state Select
J23-1&2	E280-E281	I/O 3-Wait-state Select
J36-1&2*	N/A	Dual-port RAM 0-Wait-state Select
J36-2&3	N/A	Dual-port RAM 1-Wait-state Select

NOTE: Jumper E280-E281 is found only on the Intel 86/35.

Multibus Interface Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J24-1&2*	E38-E39	Timeout Enable
J37-1&2	E202-E201	Release Bus (only for higher priority requests)
J38-1&2*	E210-E211	8289 BPRO/ drives Multibus
J39-1&2*	E205-E207	BCLK Driver Enable
J46-1*	E214	Multibus CBRQ Signal
J46-2*	E213	8289 CBRQ Input
J46-3	E212	Ground for CBRQ
J52-1&2*	E208-E209	CCLK Driver Enable
J53	E279	AEN/ Signal Test Point
J87-1&2*	N/A	Enable MPRO/ from P2-20
J88-1&2*	N/A	Enable ALE to P2-32
J94-1&2	E238-E239	Disable Driving 24-bit Multibus Address
J104	E204-E206	Enable LOCK/ to Multibus

Miscellaneous Jumpers

21/8635-E Jumper Pin	Intel 86/3X Jumper	21/8635-E Jumper Description
J57-1&2*	E17-E18	8086/8087 Clock Enable
J65-1&2	E74-E72	-12V to P3-20
J68-1&2	E75-E73	+12V to P3-21
J69-1&2	E71-E70	+5V to P3-24
J77-1&2*	E115-E114	Vbb from P1
J78-1&2*	E277-E278	Vbb from P1

The following sections of the board have been expanded or implemented in such a way that there is no direct correlation between the jumpers on the CDSBC 21/8635-E board and the Intel 863X boards. For information on jumper selection, see the appropriate section of this chapter.

1. 8086 TEST/ Input
2. 8086/8087 Clock and Reset Generation
3. JEDEC Device Selection and Address Decode
4. Dual-port RAM Size Select Jumper
5. On-board Dual-port Address Decode
6. Multibus Dual-port Address Decode

5. Specifications

Word Size
Instruction: 8, 16, 24, or 32 bits
Data: 8 or 16 bits

CPU Clock
The CDSBC 21/8635-E can be configured for 5MHz, 8MHz, or 10MHz operation.

Processor
8086 CPU
8087 Numeric Coprocessor (optional)

Cycle Time (Fastest Instruction)
10MHz: 400ns
8MHz: 500ns
5MHz: 800ns

Memory Capacity
Dynamic RAM: 128K, 256K, 512K, or 1 megabyte

EPROM: 32K to 2MB

I/O Capacity
Serial Interface: One RS-232 serial port is provided using an 8251A.
Parallel Interface: 24 programmable lines are provided using an 8255A-5.

Counters/Timers
Three independent, fully programmable, 16-bit timers/event counters are provided using an 8253-5. Two timers/counters are available for general use, while the third is dedicated for baud rate generation.

Interfaces
All signals meet the IEEE Multibus proposed specification.
IEEE 796 Bus Compliance: Slave D16 M24 VOL Master D16 M24 I16 V023L

SBX modules meet the Intel SBX specification.
SBX Bus Compliance: D16/16

Physical Characteristics
Width: 12.0 in (30.48 cm)
Height: 6.75 in (17.15 cm)
Depth: 0.50 in (1.26 cm)
Weight (1M): 19 oz (539 gm)

DC Power Requirements
Vcc = +5V ± 5%
Vdd = +12V ± 5%
Vbb = -12V ± 5%
Icc = 5.0A typical, 6.5A maximum
Idd = 0.02A typical, 0.03A maximum
Ibb = 0.02A typical, 0.03A maximum
plus requirements of SBX modules and 8087

Environmental Characteristics
Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 90% (non-condensing)

Ordering Information

CD21/8635-E000	Multibus I 8086 CDSBC 21/8635-E with no RAM
CD21/8635-E128	Multibus I 8086 CDSBC 21/8635-E with 128K RAM
CD21/8635-E256	Multibus I 8086 CDSBC 21/8635-E with 256K RAM
CD21/8635-E512	Multibus I 8086 CDSBC 21/8635-E with 512K RAM
CD21/8635-E024	Multibus I 8086 CDSBC 21/8635-E with 1 megabyte of RAM
CD21/8635-V512	Multibus I 8086 CDSBC 21/8635-E with 512K RAM, V30 processor
CD21/8635-V024	Multibus I 8086 CDSBC 21/8635-E with 1 megabyte of RAM, V30 processor
CD81/8635-MONS	Monitor Firmware for CDSBC 21/8635-E
CD91/8635-EMAN	*Multibus I CDSBC 21/8635-E Reference Manual*
CD91/8635-MONS	*80X86 Monitor Firmware Reference Manual*

Appendix A - PAL Equations

An equation is used to define each PAL (Programmable Array Logic) device output. All PAL equations are done in logical form, without regard to the active state (high/low) of each referenced signal. Thus, PAL equations use a trailing slash to indicate an inactive signal, and the absence of the slash indicates the signal must be active. The determination of whether the actual signals are active-high or active-low does not need to be made until the device is programmed, and is not described in this manual. Also, the "*" symbol represents the AND condition, while the "+" symbol represents the OR condition.

I/O PAL Equations

```
  IOACC = A5/ * A6 * A7 * EN1 * EN2 * ENBL
        + A4/ * A5/ * A6/ * A7 * SBX1P * EN1 * EN2 * ENBL
        + A4/ * A5 * A6/ * A7 * SBX2P * EN1 * EN2 * ENBL
        + A4 * A5/ * A6/ * A7 * SBX1P * 16BS1/ * EN1 * EN2 * ENBL
        + A4 * A5 * A6/ * A7 * SBX2P * 16BS2/ * EN1 * EN2 * ENBL

SBX2CS0 = A0/ * A4/ * A5 * A6/ * A7 * SBX2P * EN1 * EN2 * ENBL

SBX2CS1 = A4/ * A5 * A6/ * A7 * PBHE * SBX2P * 16BS2 * EN1 * EN2 * ENBL
        + A0/ * A4 * A5 * A6/ * A7 * SBX2P * 16BS2/ * EN1 * EN2 * ENBL

SBX1CS0 = A0/ * A4/ * A5/ * A6/ * A7 * SBX1P * EN1 * EN2 * ENBL

SBX1CS1 = A4/ * A5/ * A6/ * A7 * PBHE * SBX1P * 16BS1 * EN1 * EN2
          * ENBL
        + A0/ * A4 * A5/ * A6/ * A7 * SBX1P * 16BS1/ * EN1 * EN2 * ENBL

 EN51-59 = A0/ * A5/ * A6 * A7 * EN1 * EN2 * ENBL

   STTCS = A5/ * A6 * A7 * WT3 * PIOWC * EN1 * EN2 * ENBL
```

Unlabeled Signals:

Name	Pin
EN1	1
EN2	2
16BS2/	13
16BS1/	14

DP Decode PAL Equations

```
OBRDIS = MEM/
       + RAMDIS * DISALL
       + RAMDIS * A17
       + RAMDIS * A18
       + RAMDIS * A19

OBRAM = OBRANGE * OBRDIS/ * PRMACC/

OBADR = PRMACC
      + INTACY * OFBDINTA/
      + OBRANGE * OBRDIS/

PNMI/ = NMI/
      + NMIMSK
```

For 128K, 256K, and 512K Boards:

```
OBRANGE = A19/ * A18/ * A17/ * MEM
        + A19/ * A18/ * RS0 * MEM
        + A19/ * RS1 * MEM
        + RS1 * RS0 * MEM
```

For 1-Megabyte Boards:

```
OBRANGE = A19/ * MEM
        + A18/ * A17/ * MEM
        + A18/ * RS0 * MEM
        + A18/ * RS1 * MEM
        + A18 * A17/ * RS1 * MEM
        + RS1 * RS0 * MEM
```

JEDEC Decode PAL Equations

```
PRMACC = PS2 * PS1/ * PS0/ * A19 * A18 * A17 * A16 * A15 * MEM
       + PS2 * PS1/ * PS0 * A19 * A18 * A17 * A16 * MEM
       + PS2 * PS1 * PS0/ * A19 * A18 * A17 * MEM
       + PS1 * PS0 * A19 * A18 * MEM
       + PS2/ * PS1/ * A19 * MEM
       + PS2/ * PS1 * PS0 * A19 * A17 * MEM
       + PS2/ * PS1/ * PS0/ * A18 * A17 * MEM

 PRM0L = PS2 * PS1/ * PS0/ * A19 * A18 * A17 * A16 * A15 * A14/ * A0/ *
         MEM
       + PS2 * PS1/ * PS0 * A19 * A18 * A17 * A16 * A15/ *  A0/ * MEM
       + PS2 * PS1 * PS0/ * A19 * A18 * A17 * A16/ * A0/ * MEM
       + PS2 * PS1 * PS0 * A19 * A18 * A17/ * A0/ * MEM
       + PS2/ * PS1 * PS0 * A19 * A18/ * A17 * A0/ * MEM
       + PS2/ * PS1/ * PS0/ * A19/ * A18 * A17 * A0/ * MEM

 PRM0H = PS2 * PS1/ * PS0/ * A19 * A18 * A17 * A16 * A15 * A14/ * PBHE *
         MEM
       + PS2 * PS1/ * PS0 * A19 * A18 * A17 * A16 * A15/ * PBHE * MEM
       + PS2 * PS1 * PS0/ * A19 * A18 * A17 * A16/ * PBHE * MEM
       + PS2 * PS1 * PS0 * A19 * A18 * A17/ * PBHE * MEM
       + PS2/ * PS1 * PS0 * A19 * A18/ * A17 * PBHE * MEM
       + PS2/ * PS1/ * PS0/ * A19/ * A18 * A17 * PBHE * MEM

 PRM1L = PS2 * PS1/ * PS0/ * A19 * A18 * A17 * A16 * A15 * A14 * A0/ *
         MEM
       + PS2 * PS1/ * PS0 * A19 * A18 * A17 * A16 * A15 * A0/ * MEM
       + PS2 * PS1 * PS0/ * A19 * A18 * A17 * A16 * A0/ * MEM
       + PS2 * PS1 * PS0 * A19 * A18 * A17 * A0/ * MEM
       + PS2/ * PS1 * PS0 * A19 * A18 * A0/ * MEM
       + PS2/ * PS1/ * A19 * A0/ * MEM

 PRM1H = PS2 * PS1/ * PS0/ * A19 * A18 * A17 * A16 * A15 * A14 * PBHE *
         MEM
       + PS2 * PS1/ * PS0 * A19 * A18 * A17 * A16 * A15 * PBHE * MEM
       + PS2 * PS1 * PS0/ * A19 * A18 * A17 * A16 * PBHE * MEM
       + PS2 * PS1 * PS0 * A19 * A18 * A17 * PBHE * MEM
       + PS2/ * PS1 * PS0 * A19 * A18 * PBHE * MEM
       + PS2/ * PS1/ * A19 * PBHE * MEM
```

Appendix B - PROM Listings

This appendix gives a listing of each PROM used on the board. All values are listed in hexadecimal, with the starting address for a line listed at the left side.

Translation PROM for 128K Boards

0000	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06
0010	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06
0020	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06
0030	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06
0040	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06	01
0050	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06	04
0060	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06	04
0070	01	01	01	01	01	01	01	01	01	01	01	01	01	01	06	04
0080	01	01	01	01	01	01	01	01	01	01	01	01	01	06	01	01
0090	01	01	01	01	01	01	01	01	01	01	01	01	01	06	04	01
00A0	01	01	01	01	01	01	01	01	01	01	01	01	01	06	04	02
00B0	01	01	01	01	01	01	01	01	01	01	01	01	01	06	04	02
00C0	01	01	01	01	01	01	01	01	01	01	01	01	06	01	01	01
00D0	01	01	01	01	01	01	01	01	01	01	01	01	06	04	01	01
00E0	01	01	01	01	01	01	01	01	01	01	01	01	06	04	02	01
00F0	01	01	01	01	01	01	01	01	01	01	01	01	06	04	02	00
0100	01	01	01	01	01	01	01	01	01	01	01	06	01	01	01	01
0110	01	01	01	01	01	01	01	01	01	01	01	06	04	01	01	01
0120	01	01	01	01	01	01	01	01	01	01	01	06	04	02	01	01
0130	01	01	01	01	01	01	01	01	01	01	01	06	04	02	00	01
0140	01	01	01	01	01	01	01	01	01	01	06	01	01	01	01	01
0150	01	01	01	01	01	01	01	01	01	01	06	04	01	01	01	01
0160	01	01	01	01	01	01	01	01	01	01	06	04	02	01	01	01
0170	01	01	01	01	01	01	01	01	01	01	06	04	02	00	01	01
0180	01	01	01	01	01	01	01	01	01	06	01	01	01	01	01	01
0190	01	01	01	01	01	01	01	01	01	06	04	01	01	01	01	01
01A0	01	01	01	01	01	01	01	01	01	06	04	02	01	01	01	01
01B0	01	01	01	01	01	01	01	01	01	06	04	02	00	01	01	01
01C0	01	01	01	01	01	01	01	01	06	01	01	01	01	01	01	01
01D0	01	01	01	01	01	01	01	01	06	04	01	01	01	01	01	01
01E0	01	01	01	01	01	01	01	01	06	04	02	01	01	01	01	01
01F0	01	01	01	01	01	01	01	01	06	04	02	00	01	01	01	01
0200	01	01	01	01	01	01	01	06	01	01	01	01	01	01	01	01
0210	01	01	01	01	01	01	01	06	04	01	01	01	01	01	01	01
0220	01	01	01	01	01	01	01	06	04	02	01	01	01	01	01	01
0230	01	01	01	01	01	01	01	06	04	02	00	01	01	01	01	01
0240	01	01	01	01	01	01	06	01	01	01	01	01	01	01	01	01
0250	01	01	01	01	01	01	06	04	01	01	01	01	01	01	01	01
0260	01	01	01	01	01	01	06	04	02	01	01	01	01	01	01	01
0270	01	01	01	01	01	01	06	04	02	00	01	01	01	01	01	01
0280	01	01	01	01	01	06	01	01	01	01	01	01	01	01	01	01
0290	01	01	01	01	01	06	04	01	01	01	01	01	01	01	01	01
02A0	01	01	01	01	01	06	04	02	01	01	01	01	01	01	01	01
02B0	01	01	01	01	01	06	04	02	00	01	01	01	01	01	01	01

Translation PROM for 128K Boards, continued

02C0	01	01	01	01	06	01	01	01	01	01	01	01	01	01	01	01
02D0	01	01	01	01	06	04	01	01	01	01	01	01	01	01	01	01
02E0	01	01	01	01	06	04	02	01	01	01	01	01	01	01	01	01
02F0	01	01	01	01	06	04	02	00	01	01	01	01	01	01	01	01
0300	01	01	01	06	01	01	01	01	01	01	01	01	01	01	01	01
0310	01	01	01	06	04	01	01	01	01	01	01	01	01	01	01	01
0320	01	01	01	06	04	02	01	01	01	01	01	01	01	01	01	01
0330	01	01	01	06	04	02	00	01	01	01	01	01	01	01	01	01
0340	01	01	06	01	01	01	01	01	01	01	01	01	01	01	01	01
0350	01	01	06	04	01	01	01	01	01	01	01	01	01	01	01	01
0360	01	01	06	04	02	01	01	01	01	01	01	01	01	01	01	01
0370	01	01	06	04	02	00	01	01	01	01	01	01	01	01	01	01
0380	01	06	01	01	01	01	01	01	01	01	01	01	01	01	01	01
0390	01	06	04	01	01	01	01	01	01	01	01	01	01	01	01	01
03A0	01	06	04	02	01	01	01	01	01	01	01	01	01	01	01	01
03B0	01	06	04	02	00	01	01	01	01	01	01	01	01	01	01	01
03C0	06	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
03D0	06	04	01	01	01	01	01	01	01	01	01	01	01	01	01	01
03E0	06	04	02	01	01	01	01	01	01	01	01	01	01	01	01	01
03F0	06	04	02	00	01	01	01	01	01	01	01	01	01	01	01	01

Translation PROM for 256K Boards

0000	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E
0010	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E
0020	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E
0030	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E
0040	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C
0050	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C
0060	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C
0070	01	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C
0080	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	01
0090	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A
00A0	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A
00B0	01	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A
00C0	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	01	01
00D0	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08
00E0	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08
00F0	01	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08
0100	01	01	01	01	01	01	01	01	01	01	01	0E	0C	01	01	01
0110	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	01
0120	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	06
0130	01	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	06
0140	01	01	01	01	01	01	01	01	01	01	0E	0C	01	01	01	01
0150	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	01	01
0160	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	06	04
0170	01	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	06	04
0180	01	01	01	01	01	01	01	01	01	0E	0C	01	01	01	01	01
0190	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	01	01	01
01A0	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	06	04	01
01B0	01	01	01	01	01	01	01	01	01	0E	0C	0A	08	06	04	02
01C0	01	01	01	01	01	01	01	01	0E	0C	01	01	01	01	01	01
01D0	01	01	01	01	01	01	01	01	0E	0C	0A	08	01	01	01	01
01E0	01	01	01	01	01	01	01	01	0E	0C	0A	08	06	04	01	01
01F0	01	01	01	01	01	01	01	01	0E	0C	0A	08	06	04	02	00
0200	01	01	01	01	01	01	01	0E	0C	01	01	01	01	01	01	01
0210	01	01	01	01	01	01	01	0E	0C	0A	08	01	01	01	01	01
0220	01	01	01	01	01	01	01	0E	0C	0A	08	06	04	01	01	01
0230	01	01	01	01	01	01	01	0E	0C	0A	08	06	04	02	00	01
0240	01	01	01	01	01	01	0E	0C	01	01	01	01	01	01	01	01
0250	01	01	01	01	01	01	0E	0C	0A	08	01	01	01	01	01	01
0260	01	01	01	01	01	01	0E	0C	0A	08	06	04	01	01	01	01
0270	01	01	01	01	01	01	0E	0C	0A	08	06	04	02	00	01	01
0280	01	01	01	01	01	0E	0C	01	01	01	01	01	01	01	01	01
0290	01	01	01	01	01	0E	0C	0A	08	01	01	01	01	01	01	01
02A0	01	01	01	01	01	0E	0C	0A	08	06	04	01	01	01	01	01
02B0	01	01	01	01	01	0E	0C	0A	08	06	04	02	00	01	01	01

Translation PROM for 256K Boards, continued

02C0	01	01	01	01	0E	0C	01	01	01	01	01	01	01	01	01	01
02D0	01	01	01	01	0E	0C	0A	08	01	01	01	01	01	01	01	01
02E0	01	01	01	01	0E	0C	0A	08	06	04	01	01	01	01	01	01
02F0	01	01	01	01	0E	0C	0A	08	06	04	02	00	01	01	01	01
0300	01	01	01	0E	0C	01	01	01	01	01	01	01	01	01	01	01
0310	01	01	01	0E	0C	0A	08	01	01	01	01	01	01	01	01	01
0320	01	01	01	0E	0C	0A	08	06	04	01	01	01	01	01	01	01
0330	01	01	01	0E	0C	0A	08	06	04	02	00	01	01	01	01	01
0340	01	01	0E	0C	01	01	01	01	01	01	01	01	01	01	01	01
0350	01	01	0E	0C	0A	08	01	01	01	01	01	01	01	01	01	01
0360	01	01	0E	0C	0A	08	06	04	01	01	01	01	01	01	01	01
0370	01	01	0E	0C	0A	08	06	04	02	00	01	01	01	01	01	01
0380	01	0E	0C	01	01	01	01	01	01	01	01	01	01	01	01	01
0390	01	0E	0C	0A	08	01	01	01	01	01	01	01	01	01	01	01
03A0	01	0E	0C	0A	08	06	04	01	01	01	01	01	01	01	01	01
03B0	01	0E	0C	0A	08	06	04	02	00	01	01	01	01	01	01	01
03C0	0E	0C	01	01	01	01	01	01	01	01	01	01	01	01	01	01
03D0	0E	0C	0A	08	01	01	01	01	01	01	01	01	01	01	01	01
03E0	0E	0C	0A	08	06	04	01	01	01	01	01	01	01	01	01	01
03F0	0E	0C	0A	08	06	04	02	00	01	01	01	01	01	01	01	01

Translation PROM for 512K or 1-Megabyte Boards

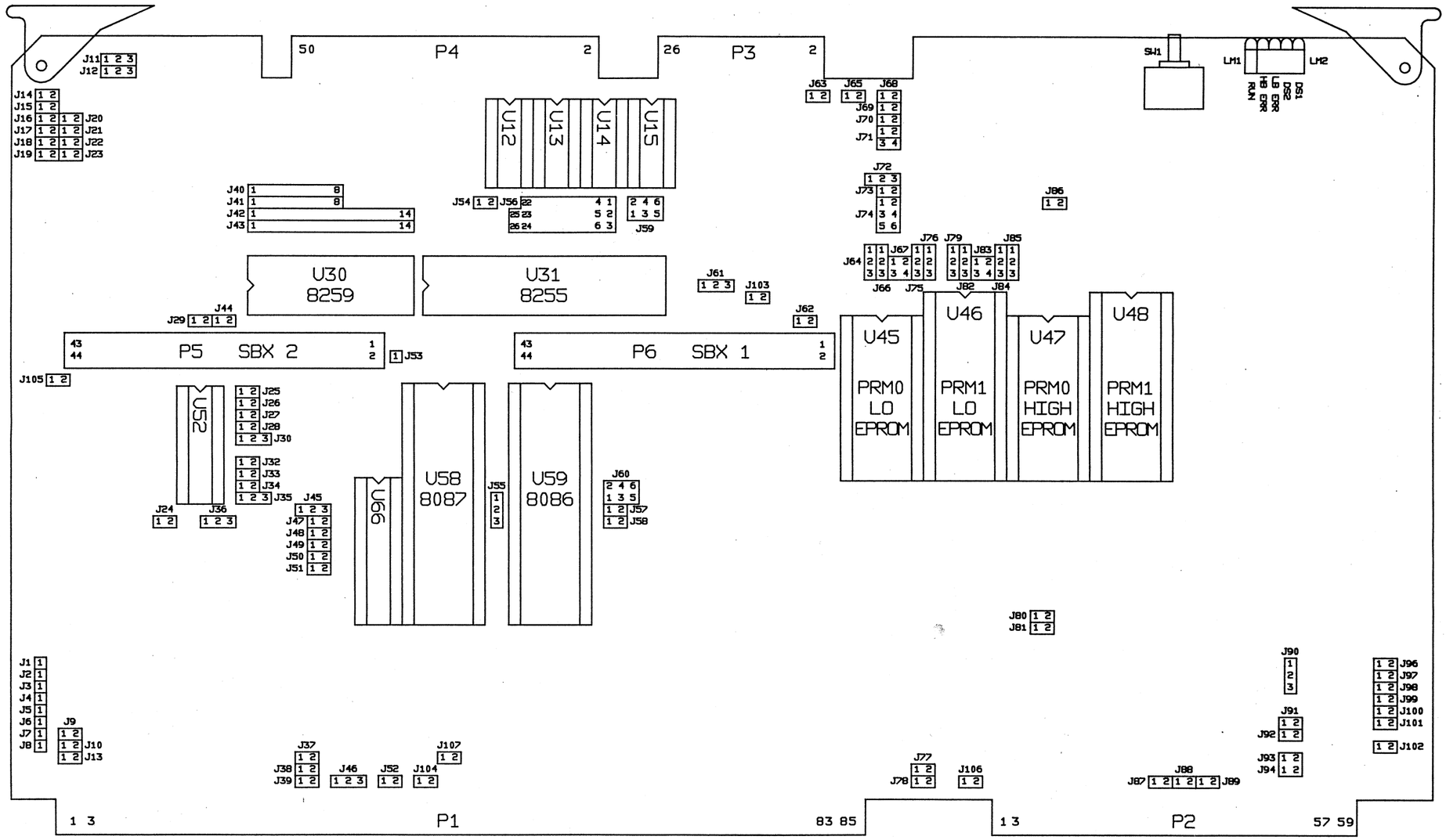
0000	3E	3C	3A	38	01	01	01	01	3E	3C	3A	38	01	01	01	01
0010	3E	3C	3A	38	01	01	01	01	3E	3C	3A	38	01	01	01	01
0020	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
0030	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
0040	01	01	3A	38	01	01	01	01	01	01	3A	38	01	01	01	01
0050	01	01	3A	38	01	01	01	01	01	01	3A	38	01	01	01	01
0060	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
0070	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
0080	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
0090	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
00A0	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
00B0	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
00C0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
00D0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
00E0	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
00F0	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18	1E	1C	1A	18
0100	36	34	32	30	01	01	01	01	36	34	32	30	01	01	01	01
0110	36	34	32	30	01	01	01	01	36	34	32	30	01	01	01	01
0120	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
0130	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
0140	36	34	32	30	01	01	01	01	36	34	32	30	01	01	01	01
0150	36	34	32	30	01	01	01	01	36	34	32	30	01	01	01	01
0160	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
0170	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
0180	36	34	32	30	01	01	01	01	36	34	32	30	01	01	01	01
0190	36	34	32	30	01	01	01	01	36	34	32	30	01	01	01	01
01A0	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
01B0	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
01C0	01	01	32	30	01	01	01	01	01	01	32	30	01	01	01	01
01D0	01	01	32	30	01	01	01	01	01	01	32	30	01	01	01	01
01E0	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
01F0	16	14	12	10	16	14	12	10	16	14	12	10	16	14	12	10
0200	2E	2C	2A	28	2E	2C	2A	28	2E	2C	2A	28	2E	2C	2A	28
0210	2E	2C	2A	28	2E	2C	2A	28	2E	2C	2A	28	2E	2C	2A	28
0220	01	01	01	01	01	01	01	01	0E	0C	0A	08	0E	0C	0A	08
0230	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08
0240	2E	2C	2A	28	01	01	2A	28	2E	2C	2A	28	01	01	2A	28
0250	2E	2C	2A	28	01	01	2A	28	2E	2C	2A	28	01	01	2A	28
0260	01	01	01	01	01	01	01	01	0E	0C	0A	08	0E	0C	0A	08
0270	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08
0280	2E	2C	2A	28	01	01	01	01	2E	2C	2A	28	01	01	01	01
0290	2E	2C	2A	28	01	01	01	01	2E	2C	2A	28	01	01	01	01
02A0	01	01	01	01	01	01	01	01	0E	0C	0A	08	0E	0C	0A	08
02B0	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08

Translation PROM for 512K or 1-Megabyte Boards, continued

02C0	2E	2C	2A	28	01	01	01	01	2E	2C	2A	28	01	01	01	01
02D0	2E	2C	2A	28	01	01	01	01	2E	2C	2A	28	01	01	01	01
02E0	01	01	01	01	01	01	01	01	0E	0C	0A	08	0E	0C	0A	08
02F0	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08	0E	0C	0A	08
0300	26	24	22	20	26	24	22	20	26	24	22	20	26	24	22	20
0310	26	24	22	20	26	24	22	20	26	24	22	20	26	24	22	20
0320	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
0330	06	04	01	01	06	04	01	01	06	04	02	00	06	04	02	00
0340	26	24	22	20	26	24	22	20	26	24	22	20	26	24	22	20
0350	26	24	22	20	26	24	22	20	26	24	22	20	26	24	22	20
0360	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
0370	06	04	01	01	06	04	01	01	06	04	02	00	06	04	02	00
0380	26	24	22	20	26	24	22	20	26	24	22	20	26	24	22	20
0390	26	24	22	20	26	24	22	20	26	24	22	20	26	24	22	20
03A0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
03B0	06	04	01	01	06	04	01	01	06	04	02	00	06	04	02	00
03C0	26	24	22	20	01	01	01	01	26	24	22	20	01	01	01	01
03D0	26	24	22	20	01	01	01	01	26	24	22	20	01	01	01	01
03E0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
03F0	06	04	01	01	06	04	01	01	06	04	02	00	06	04	02	00

Appendix C - Jumper Locations

The following drawing illustrates where jumpers are located on the Central Data CDSBC 21/8635-E Single-Board Computer. See Chapter 4, "Installation," for a complete description of jumpers and their functions.

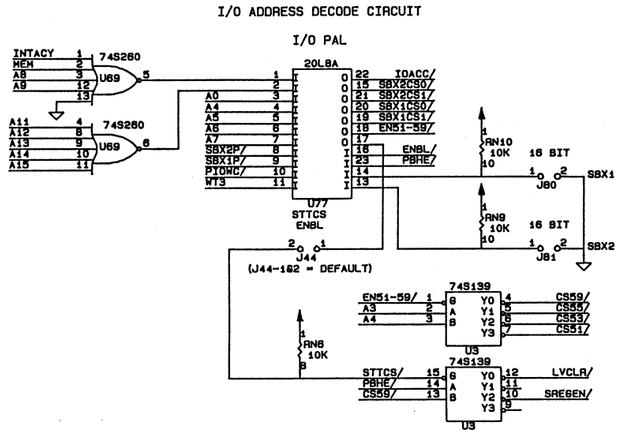


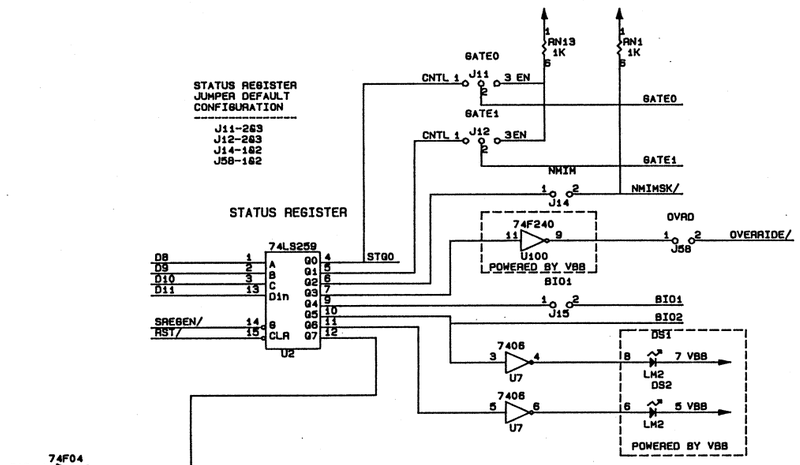
Central Data		8086 SINGLE BOARD COMPUTER	
		JUMPER LOCATIONS	
DRAWING NO. A1592	REV. A	SHEET 1 OF 1	

Appendix D - Schematics

The following pages contain the schematics for the CDSBC 21/8635-E Single-Board Computer. A brief description of the circuitry is given in the Functional Description chapter (Chapter 2) of this manual.

Following the schematics is a signal cross-reference table that lists signal locations on the schematics.

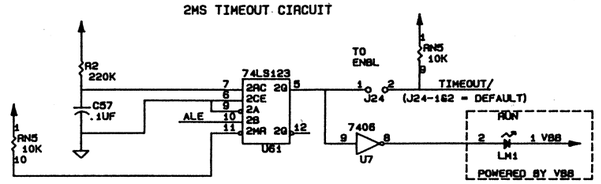


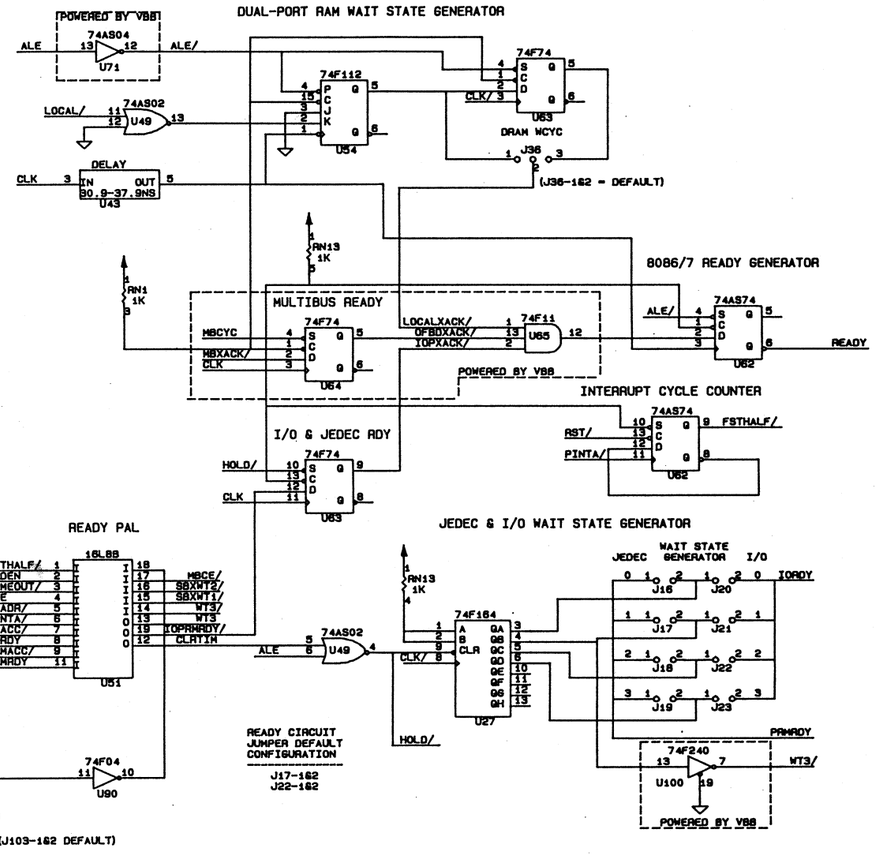


LOCAL DUAL-PORT RAM DISABLE FEATURE

J91	J92	J93	STQ0	RAMDIS	LOCAL ACCESSES
0	1	X	X	0	ENABLED
1	0	1	0	1	DISABLED
1	0	1	1	0	ENABLED
1	0	0	0	0	ENABLED
1	0	0	1	0	DISABLED

NOTE: FOR J91-J93, 1 = JUMPER INSTALLED
0 = JUMPER REMOVED





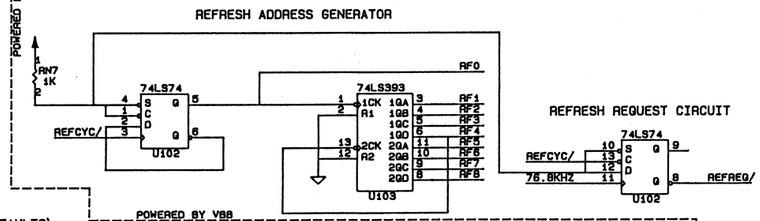
Central Data

8086 SINGLE BOARD COMPUTER

I/O DECODE, STATUS REGISTER AND READY CIRCUITRY

DRAWING NO.	REV.	SHEET 1 OF 5	
A1360			

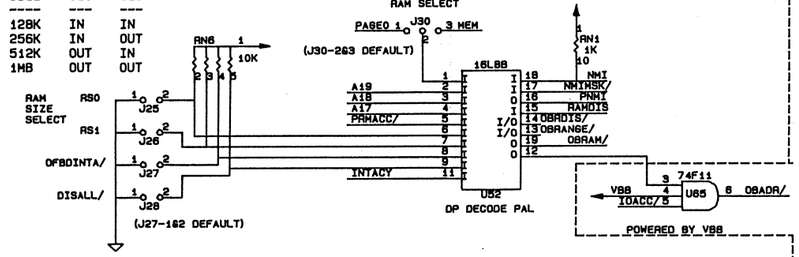
REFRESH ADDRESS GENERATOR



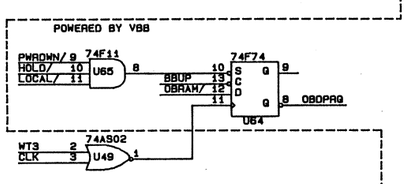
REFRESH REQUEST CIRCUIT

ON-BOARD (LOCAL) DUAL-PORT RAM DECODE CIRCUIT

RAM SIZE	J26	J25
128K	IN	IN
256K	IN	OUT
512K	OUT	IN
1MB	OUT	OUT

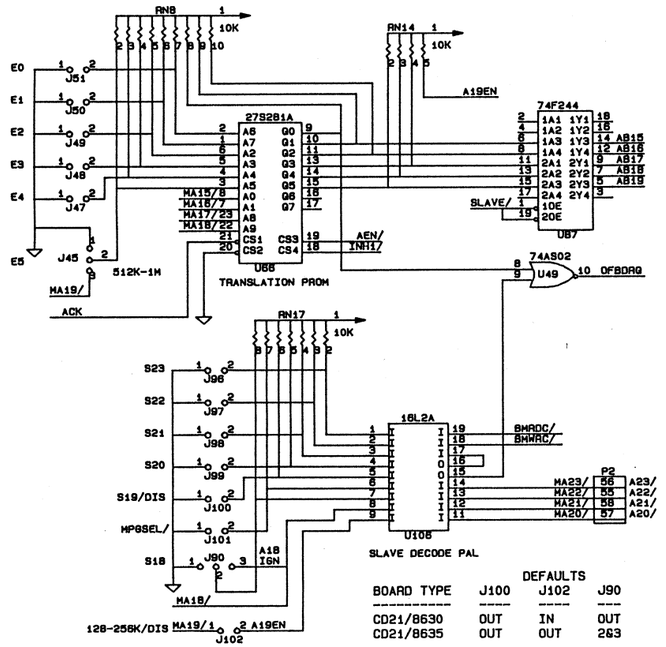


ON-BOARD (LOCAL) DUAL-PORT RAM REQUEST CIRCUIT



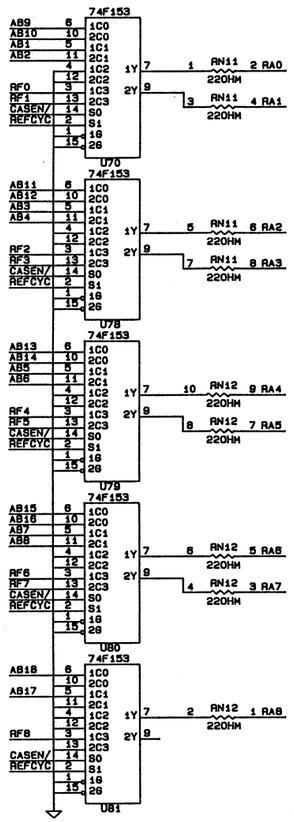
MULTIBUS (SLAVE) DUAL-PORT RAM DECODE/REQUEST CIRCUIT

RAM SIZE	J45	J47	J48	J49	J50	J51
128K	OUT	0	1	1	0	0
256K	OUT	0	1	0	0	0
512K	2-3	0	0	0	0	0
1MB	2-3	0	0	1	1	1



BOARD TYPE	DEFAULTS J100	J102	J90
CD21/8630	OUT	IN	OUT
CD21/8635	OUT	OUT	263

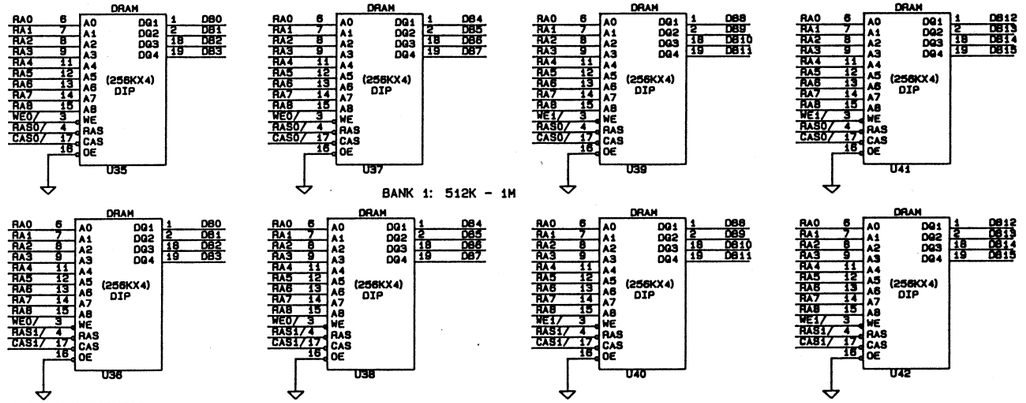
DUAL-PORT RAM ADDRESS MULTIPLEXERS



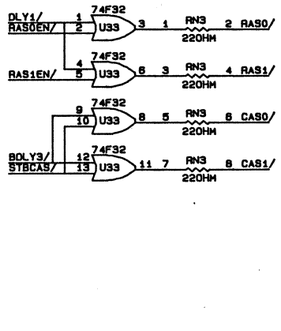
DUAL-PORT RAM ARRAY

BANK 0: 0 - 512K

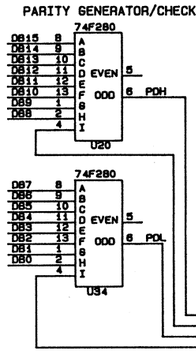
BANK 1: 512K - 1M



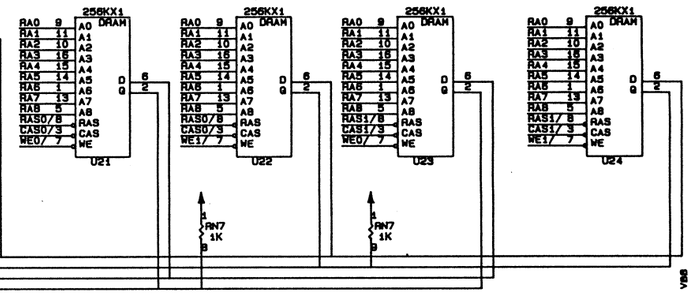
RAS & CAS DRIVERS



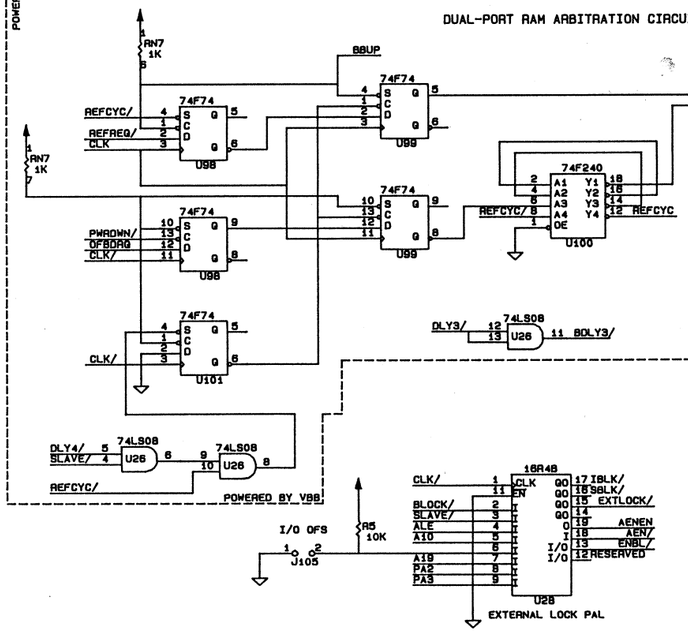
PARITY GENERATOR/CHECKERS



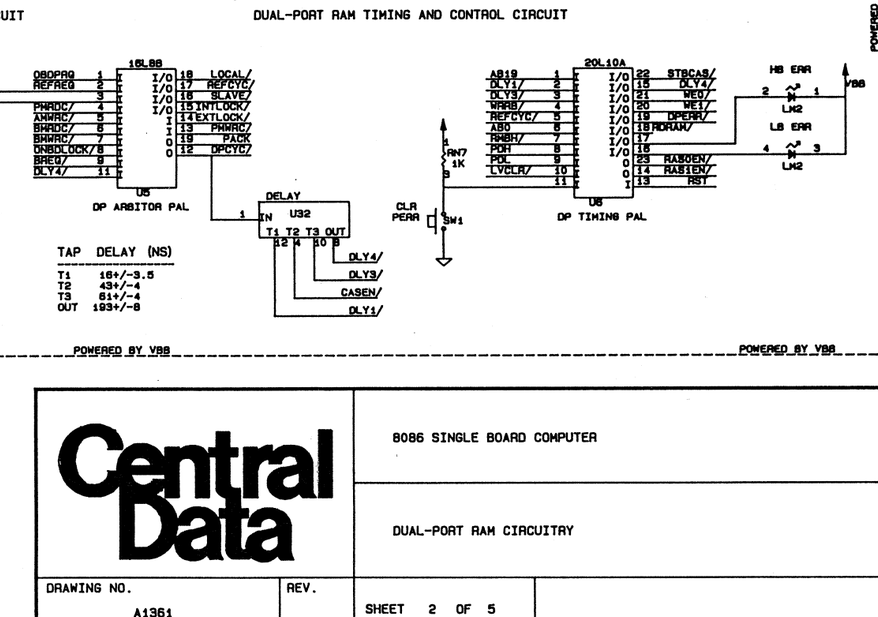
PARITY RAMS: 41256 (512K-1M)



DUAL-PORT RAM ARBITRATION CIRCUIT

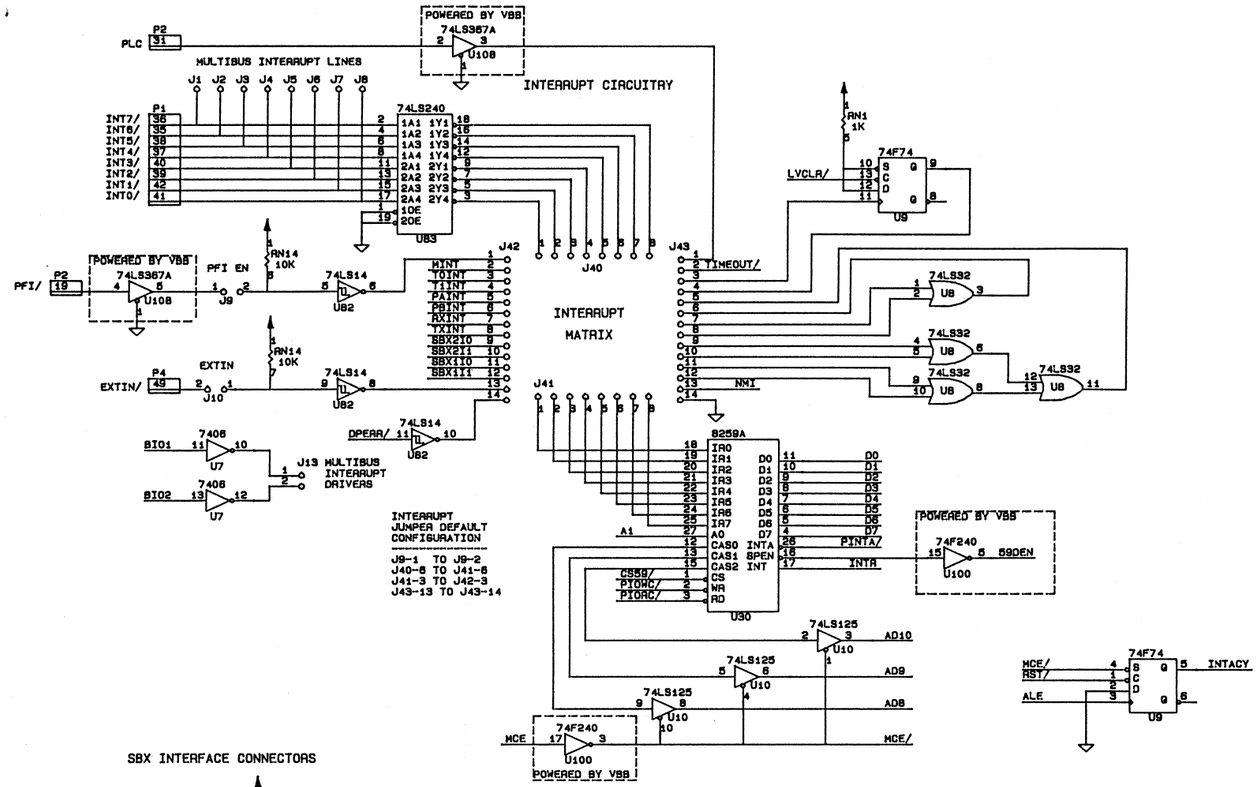


DUAL-PORT RAM TIMING AND CONTROL CIRCUIT



EXTERNAL LOCK PAL

POWERED BY VBB

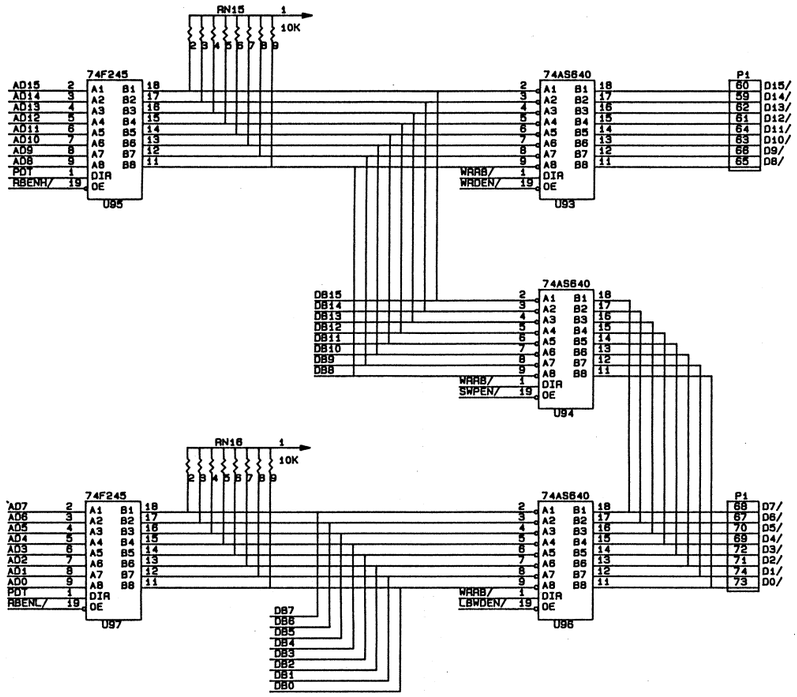


Central Data	8086 SINGLE BOARD COMPUTER	
	ON-BOARD I/O DEVICES	
DRAWING NO. A1362	REV. B	SHEET 3 OF 5

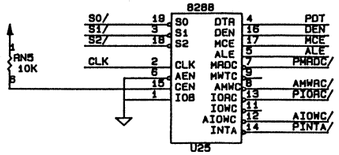
LOCAL DATA BUS

DUAL-PORT RAM DATA BUS

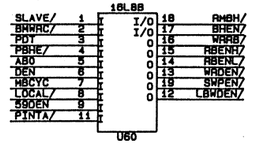
MULTIBUS DATA BUS



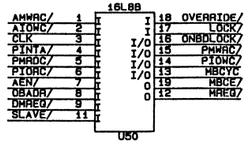
BUS CONTROLLER

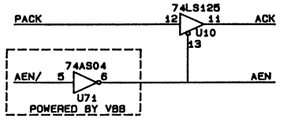


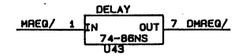
BUFFER CONTROL PAL

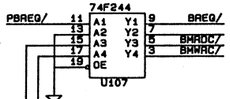


BUS COMMAND PAL

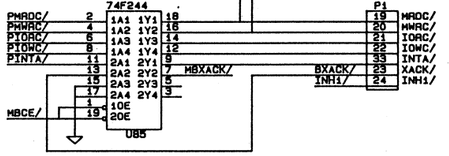


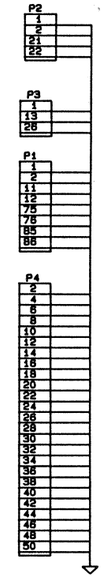


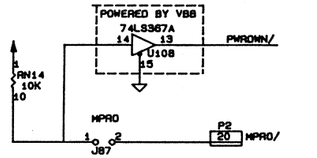


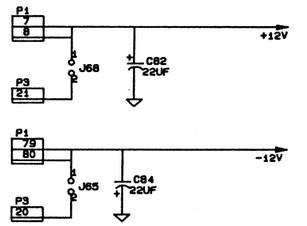


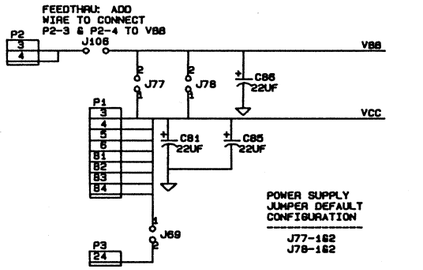
MULTIBUS COMMAND BUFFER











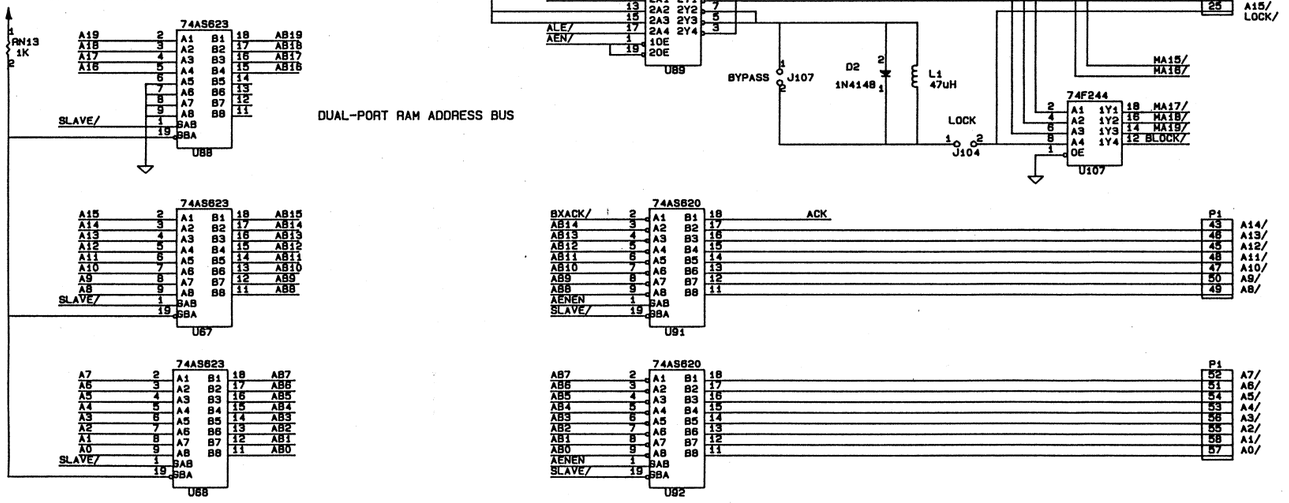
POWER SUPPLY JUMPER DEFAULT CONFIGURATION

J77-1&2
J78-1&2

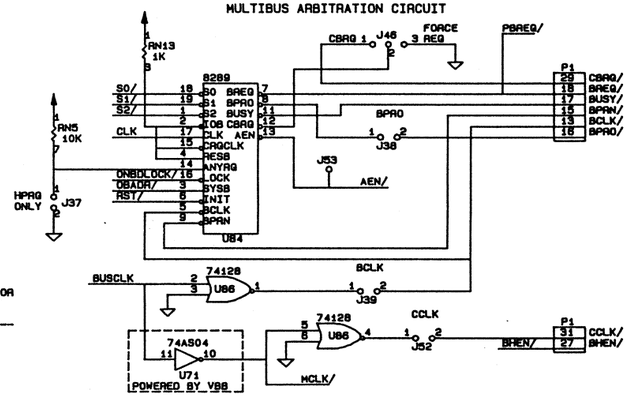
LOCAL ADDRESS BUS

DUAL-PORT RAM ADDRESS BUS

MULTIBUS ADDRESS BUS



MULTIBUS ARBITRATION CIRCUIT



MULTIBUS ARBITOR JUMPER DEFAULT CONFIGURATION

J38-1&2
J39-1&2
J46-1&2
J52-1&2

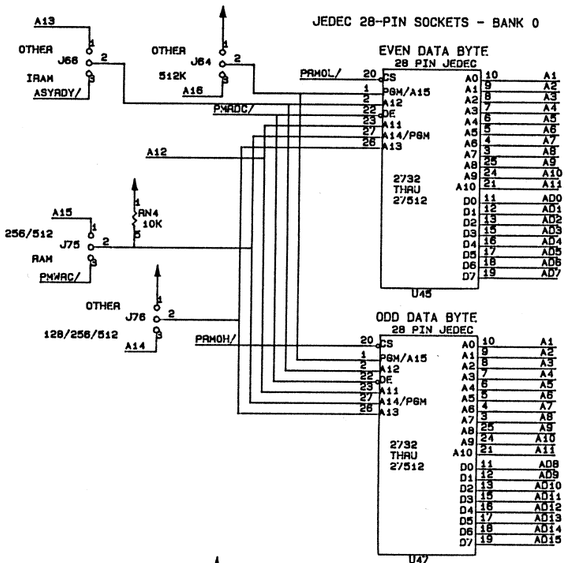
Central Data

8086 SINGLE BOARD COMPUTER

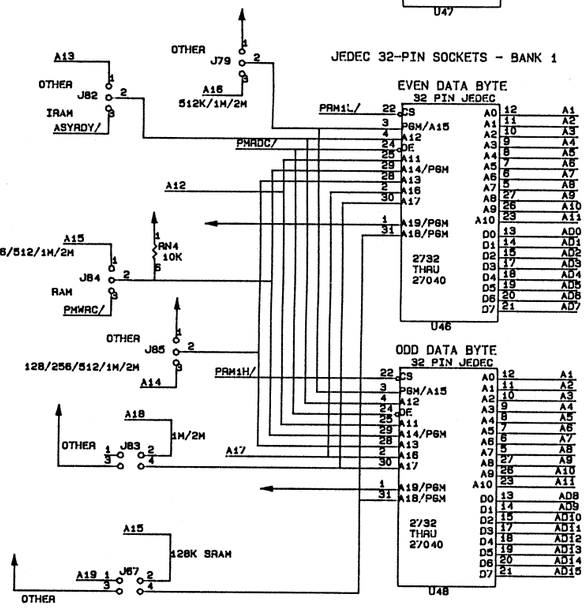
MULTIBUS INTERFACE CIRCUITRY

DRAWING NO.	REV.	SHEET 4 OF 5	
A1363			

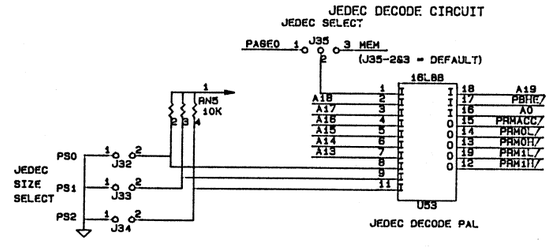
JEDEC 28-PIN SOCKETS - BANK 0



JEDEC 32-PIN SOCKETS - BANK 1



JEDEC DECODE CIRCUIT



CONFIGURATION JUMPERS FOR BANK 0:

DEVICE TYPE	J64 PIN1	J66 PIN2	J76 PIN26	J75 PIN27
2732 EPROM	N/C	N/C	1-2	N/C
2764 EPROM*	1-2	1-2	1-2	N/C
27128 EPROM	1-2	1-2	2-3	N/C
27256 EPROM	1-2	1-2	2-3	1-2
27512 EPROM	2-3	1-2	2-3	1-2
8Kx8 SRAM**	1-2	1-2	1-2	2-3
32Kx8 SRAM	***	1-2	2-3	2-3
8Kx8 IRAM	1-2	2-3	1-2	2-3

NOTES: * DEFAULT CONFIGURATION
** OR EEPROM OF SAME SIZE
*** ADD WIRE FROM J64 PIN 2 TO J75 PIN 1

CONFIGURATION JUMPERS FOR BANK 1:

DEVICE TYPE	J79 PIN3	J82 PIN4	J83 PIN30	J85 PIN28	J84 PIN29	J67 PIN31
2732 EPROM	N/C	N/C	3-4	1-2	N/C	N/C
2764 EPROM*	1-2	1-2	3-4	1-2	N/C	N/C
27128 EPROM	1-2	1-2	3-4	2-3	N/C	N/C
27256 EPROM	1-2	1-2	3-4	2-3	1-2	N/C
27512 EPROM	2-3	1-2	3-4	2-3	1-2	N/C
27010 EPROM	2-3	1-2	2-4	2-3	1-2	3-4
27020 EPROM	2-3	1-2	2-4	2-3	1-2	3-4
8Kx8 SRAM**	1-2	1-2	3-4	1-2	2-3	N/C
32Kx8 SRAM	***	1-2	3-4	2-3	2-3	N/C
128Kx8 SRAM	2-3	1-2	2-4	2-3	2-3	2-4
8Kx8 IRAM	1-2	2-3	3-4	1-2	2-3	N/C

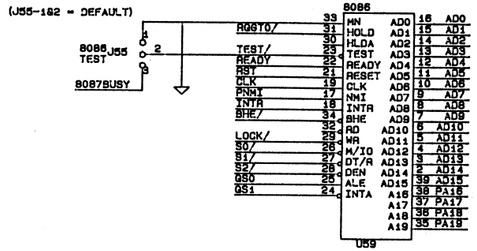
NOTES: * DEFAULT CONFIGURATION
** OR EEPROM OF SAME SIZE
*** ADD WIRE FROM J79 PIN 2 TO J84 PIN 1

JEDEC DECODE CIRCUIT SIZE SELECT CONFIGURATION JUMPERS:

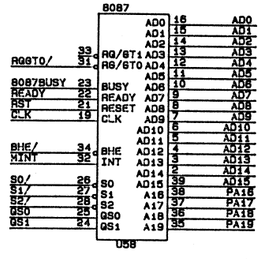
SIZE SELECT J34 PS2	J33 PS1	J32 PS0	SIZE OF DEVICE	TOTAL MEMORY MAPPED	(U45) PRM0L	(U47) PRM0H	(U46) PRM1L	(U48) PRM1H
*0	1	1	8Kx8	32K	F8000	F8001	FC000	FC001
					FBFFE	FBFFF	FFFFE	FFFFF
0	1	0	16Kx8	64K	F0000	F0001	F8000	F8001
					F7FFE	F7FFF	FFFFE	FFFFF
0	0	1	32Kx8	128K	E0000	E0001	F0000	F0001
					EFFFE	EFFFF	FFFFE	FFFFF
0	0	0	64Kx8	256K	C0000	C0001	E0000	E0001
					DFFFE	DFFFF	FFFFE	FFFFF
1	0	0	128Kx8	384K	A0000	A0001	C0000	C0001
			&64Kx8		BFFFE	BFFFF	FFFFE	FFFFF
1	1	1	256Kx8	640K	60000	60001	80000	80001
			&64Kx8		7FFFE	7FFFF	FFFFE	FFFFF
1	1	0	256Kx8	512K	-------	-------	80000	80001
					-------	-------	FFFFE	FFFFF

* DEFAULT CONFIGURATION

10MHZ 8086 MICROPROCESSOR

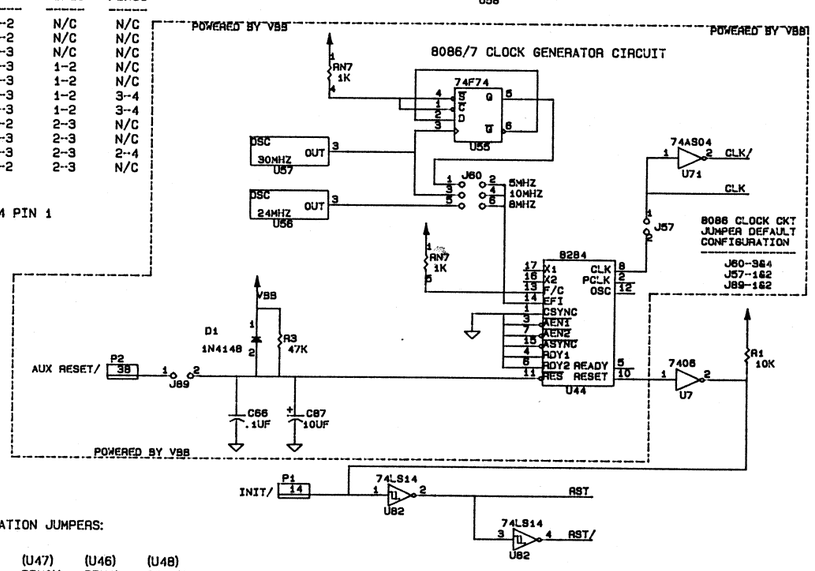


8087 MATH CO-PROCESSOR

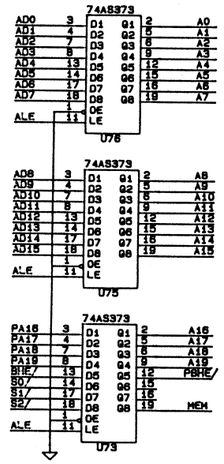


C40 22UF — LOCATED BETWEEN CHIPS

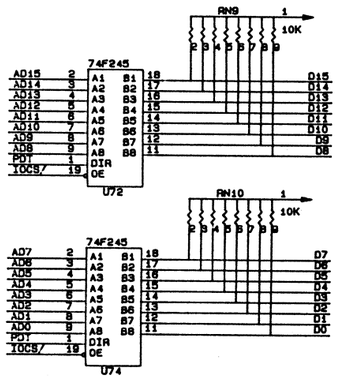
8086/7 CLOCK GENERATOR CIRCUIT



LOCAL BUS ADDRESS LATCHES



LOCAL BUS DATA TRANSCEIVERS



Central Data	8086 SINGLE BOARD COMPUTER
	8086/7 CPU'S, CLOCK CIRCUIT AND JEDEC SOCKETS
DRAWING NO. A1364-1	REV.
SHEET 5 OF 5	

Signal Name	Location on Schematics
1.23MHZ	3-A2 3-B5
153.6KHZ	3-A2 3-B5
2.4576MHZ	3-A6 3-B2 3-B5
59DEN	1-A6 1-B4 3-C5 4-D4
76.8KHZ	2-D6 3-A2
8087BUSY	5-C4 5-D4
A0	1-D7 4-A8 5-A7 5-D1
A1	3-A6 3-A8 3-B6 3-B8 3-C6 3-D3 4-A8 5-B6 5-C6 5-D1 5-D6
A10	2-A4 4-A8 5-B6 5-C6 5-D1 5-D6
A11	1-D8 4-A8 5-B6 5-C6 5-D1 5-D6
A12	1-D8 4-A8 5-C8 5-D1 5-D8
A13	1-D8 4-A8 5-A7 5-C1 5-C8 5-D8
A14	1-D8 4-A8 5-A7 5-B8 5-C1 5-D8
A15	1-D8 4-A8 5-A7 5-B8 5-C1 5-D8
A16	4-B8 5-A7 5-C1 5-C8 5-D8
A17	2-C7 4-B8 5-A7 5-B8 5-C1
A18	2-D7 4-B8 5-A7 5-B8 5-C1
A19	2-A4 2-D7 4-B8 5-A7 5-A8 5-C1
A19EN	2-A7 2-B7
A2	3-A8 3-B6 3-B8 3-D3 4-A8 5-B6 5-C6 5-D1 5-D6
A3	1-C6 3-A8 3-B8 4-A8 5-B6 5-C6 5-D1 5-D6
A4	1-C6 1-D7 4-A8 5-B6 5-C6 5-D1 5-D6
A5	1-D7 4-A8 5-B6 5-C6 5-D1 5-D6
A6	1-D7 4-A8 5-B6 5-C6 5-D1 5-D6
A7	1-D7 4-A8 5-B6 5-C6 5-D1 5-D6
A8	1-D8 4-A8 5-B6 5-C6 5-D1 5-D6
A9	1-D8 4-A8 5-B6 5-C6 5-D1 5-D6
AB0	2-B2 4-A6 4-A7 4-D4
AB1	2-D5 4-A6 4-A7
AB10	2-D5 4-A6 4-A7
AB11	2-D5 4-A6 4-A7
AB12	2-D5 4-A6 4-A7
AB13	2-C5 4-A6 4-A7
AB14	2-C5 4-A6 4-A7
AB15	2-B6 2-C5 4-A7 4-B6
AB16	2-B6 2-C5 4-B6 4-B7
AB17	2-B6 2-C5 4-B6 4-B7
AB18	2-B6 2-C5 4-B6 4-B7
AB19	2-B2 2-B6 4-B6 4-B7
AB2	2-D5 4-A6 4-A7
AB3	2-D5 4-A6 4-A7
AB4	2-D5 4-A6 4-A7
AB5	2-C5 4-A6 4-A7

Signal Name	Location on Schematics
AB6	2-C5 4-A6 4-A7
AB7	2-C5 4-A6 4-A7
AB8	2-C5 4-A6 4-A7
AB9	2-D5 4-A6 4-A7
ACK	2-B8 4-A6 4-D3
AD0	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD1	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD10	3-C5 4-D8 5-B2 5-B6 5-C3 5-C6 5-D2 5-D3
AD11	4-D8 5-B2 5-B6 5-C3 5-C6 5-D2 5-D3
AD12	4-D8 5-B2 5-B6 5-C3 5-C6 5-D2 5-D3
AD13	4-D8 5-B2 5-B6 5-C2 5-C3 5-C6 5-D3
AD14	4-D8 5-B2 5-B6 5-C2 5-C3 5-C6 5-D3
AD15	4-D8 5-B2 5-B6 5-C2 5-C3 5-C6 5-D3
AD2	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD3	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD4	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD5	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD6	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD7	4-C8 5-B2 5-B6 5-C3 5-D2 5-D3 5-D6
AD8	3-C5 4-D8 5-B2 5-B6 5-C3 5-C6 5-D2 5-D3
AD9	3-C5 4-D8 5-B2 5-B6 5-C3 5-C6 5-D2 5-D3
AEN	4-D3
AEN/	1-A6 2-A4 2-B7 4-B2 4-B6 4-D4 4-D5
AENEN	2-A4 4-A6
AIOWC/	3-A8 3-B8 4-D4 4-D5
ALE	1-B3 1-B4 1-C4 1-D3 2-A4 3-C5 4-D4 5-C2 5-D2
ALE/	1-C1 1-C3 4-B6
AMWRC/	2-B3 4-D4 4-D5
ASYRDY/	1-A4 5-C8 5-D8
BBUP	2-B5 2-C6
BDLY3/	2-A4 2-C4
BHE/	5-C2 5-C4 5-D4
BHEN/	4-A1 4-D3
BIO1	1-B6 3-C8
BIO2	1-B6 3-C8
BLOCK/	2-A4 4-B4
BMRDC/	2-A6 2-B3 4-C3
BMWRC/	2-A6 2-B3 4-C3 4-D4
BREQ/	2-B3 4-C3
BUSCLK	3-B2 4-B3
BXACK/	4-A6 4-C3
CAS0/	2-C2 2-C3 2-C4 2-D1 2-D2 2-D3 2-D4
CAS1/	2-C1 2-C2 2-C3 2-C4
CASEN/	2-A2 2-B5 2-C5 2-D5
CLK	1-B3 1-C3 1-C4 2-B5 2-C7 4-B3 4-D5 5-B3 5-C4 5-D4

Signal Name	Location on Schematics
CLK/	1-B2 1-C2 2-A4 2-A5 2-B5 5-B3
CLRTIM	1-B3
CS51/	1-C6 3-A6
CS53/	1-C6 3-B6
CS55/	1-C6 3-D3
CS59/	1-C6 3-C6
D0	3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D1	3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D10	1-B7 3-A8 3-B8 5-B1
D11	1-B7 3-A7 3-B7 5-B1
D12	1-A8 3-A8 3-B8 5-B1
D13	1-A8 3-A7 3-B7 5-B1
D14	1-A8 3-A8 3-B8 5-B1
D15	1-A8 3-A7 3-B7 5-B1
D2	3-A6 3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D3	3-A6 3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D4	3-A6 3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D5	3-A6 3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D6	3-A6 3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D7	3-A6 3-A8 3-B6 3-B8 3-C5 3-D3 5-B1
D8	1-B7 3-A8 3-B8 5-B1
D9	1-B7 3-A7 3-B7 5-B1
DB0	2-B3 2-D4 4-C7
DB1	2-B3 2-D4 4-C7
DB10	2-C3 2-D2 4-C7
DB11	2-C3 2-D2 4-C7
DB12	2-C3 2-D1 4-C7
DB13	2-C3 2-D1 4-D7
DB14	2-C3 2-D1 4-D7
DB15	2-C3 2-D1 4-D7
DB2	2-C3 2-D4 4-C7
DB3	2-C3 2-D4 4-C7
DB4	2-C3 2-D3 4-C7
DB5	2-C3 2-D3 4-C7
DB6	2-C3 2-D3 4-C7
DB7	2-C3 2-D3 4-C7
DB8	2-C3 2-D2 4-C7
DB9	2-C3 2-D2 4-C7
DEN	1-A6 4-D4
DLY1/	2-A2 2-B2 2-C4
DLY3/	2-A2 2-A4 2-B2
DLY4/	2-A2 2-A6 2-B1 2-B3
DMREQ/	4-C5 4-D5
DPCYC/	2-B3
DPERR/	2-B1 3-C7
EN51-59/	1-C6 1-D6

Signal Name	Location on Schematics
ENBL/	1-D6 2-A4
EXTCLK	3-B3 3-B5
EXTLOCK/	2-A4 2-B3
FSTHALF/	1-B1 1-B4
GATE0	1-B6 3-B6
GATE1	1-B6 3-B6
HOLD/	1-B2 1-B3 2-C7
INH1/	2-B7 4-C3
INTACY	1-D8 2-C7 3-C4
INTR	3-C5 5-D4
IOACC/	1-A6 1-B4 1-D6 2-C6
IOCS/	1-A6 5-B2
IOPRMRDY/	1-B3
IOPXACK/	1-C2
IORDY	1-B1 1-B4
LBWDEN/	4-C7 4-D3
LOCAL/	1-C3 2-B3 2-C7 4-D4
LOCALXACK/	1-C2
LOCK/	4-D5 5-D4
LVCLR/	1-C6 2-B2 3-D6
MA15/	2-B8 4-B4
MA16/	2-B8 4-B4
MA17/	2-B8 4-B4
MA18/	2-A8 2-B8 4-B4
MA19/	2-A8 2-B8 4-B4
MA20/	1-A6 2-A6
MA21/	1-A6 2-A6
MA22/	1-A6 2-A6
MA23/	1-A6 2-A6
MBCE/	1-B3 4-C5 4-D5
MBCYC	1-C3 4-D4 4-D5
MBXACK/	1-C3 4-C4
MCE	3-C7 4-D4
MCE/	3-C5
MCLK/	3-A7 3-B7 4-A2
MEM	1-A8 1-D8 2-D7 5-A7 5-C1
MINT	3-D7 5-C4
MREQ/	4-C5 4-D5
NMI	2-D6 3-C6
NMIMSK/	1-B6 2-D6
OBADR/	1-B4 2-C6 4-B2 4-D5
OBDPRQ	2-B3 2-C6
OBRAM/	2-C6
OFBDRQ	2-B5 2-B6
ONBDLOCK/	2-B3 4-B2 4-B7 4-D5
OUT2	3-A5 3-B6

Signal Name	Location on Schematics
OVERRIDE/	1-B5 4-D5
PA16	5-C2 5-C3 5-D3
PA17	5-C2 5-C3 5-D3
PA18	5-C2 5-C3 5-D3
PA19	5-C2 5-C3 5-D3
PA2	2-A4 3-D2
PA3	2-A4 3-D2
PACK	2-B3 4-D4
PAGE0	1-A7 2-D7 5-A7
PAINT	3-C3 3-D7
PBHE/	1-C6 1-D6 4-D4 5-A7 5-C1
PBINT	3-C3 3-D7
PBREQ/	4-B1 4-C4
PDH	2-B2 2-C3
PDL	2-B2 2-C3
PDT	4-C8 4-D4 4-D8 5-B2
PG0	1-A6 1-A8
PINTA/	1-B2 1-B4 3-C5 4-C5 4-D4 4-D5
PIORC/	3-A6 3-A8 3-B6 3-B8 3-C6 3-D3 4-C5 4-D4 4-D5
PIOWC/	1-D7 3-A6 3-B6 3-C6 3-D3 4-C5 4-D5
PMRDC/	2-B3 4-C5 4-D4 4-D5 5-C8 5-D8
PMWRC/	2-B3 4-C5 4-D5 5-B8 5-D8
PNMI	2-D6 5-D4
PRM0H/	5-A7 5-D8
PRM0L/	5-A7 5-D7
PRM1H/	5-A7 5-B8
PRM1L/	5-A7 5-C7
PRMACC/	1-B4 2-C7 5-A7
PRMRDY	1-B1 1-B4
PWRDWN/	2-B5 2-C7 4-D1
QS0	5-C4 5-D4
QS1	5-C4 5-D4
RA0	2-C1 2-C2 2-C3 2-D1 2-D2 2-D3 2-D4 2-D5
RA1	2-C1 2-C2 2-C3 2-D1 2-D2 2-D3 2-D4 2-D5
RA2	2-C1 2-C2 2-C3 2-D1 2-D2 2-D3 2-D4 2-D5
RA3	2-C1 2-C2 2-C3 2-D1 2-D2 2-D3 2-D4 2-D5
RA4	2-C1 2-C2 2-C3 2-C5 2-D1 2-D2 2-D3 2-D4
RA5	2-C1 2-C2 2-C3 2-C5 2-D1 2-D2 2-D3 2-D4
RA6	2-C1 2-C2 2-C3 2-C5 2-D1 2-D2 2-D3 2-D4
RA7	2-C1 2-C2 2-C3 2-C5 2-D1 2-D2 2-D3 2-D4
RA8	2-C1 2-C2 2-C3 2-C5 2-D1 2-D2 2-D3 2-D4
RAMDIS	1-A5 2-C6
RAS0/	2-C2 2-C3 2-C4 2-D1 2-D2 2-D3 2-D4
RAS0EN/	2-B1 2-C4
RAS1/	2-C1 2-C2 2-C3 2-C4
RAS1EN/	2-B1 2-C4

Signal Name	Location on Schematics
RBENH/	4-D3 4-D8
RBENL/	4-C8 4-D3
READY	1-C1 5-C4 5-D4
REFCYC	2-B4 2-B5 2-C5 2-D5
REFCYC/	2-A6 2-B2 2-B3 2-B4 2-B5 2-D6 2-D8
REFREQ	2-B3
REFREQ/	2-B5 2-D6
RF0	2-D5 2-D6
RF1	2-D5 2-D6
RF2	2-D5 2-D6
RF3	2-D5 2-D6
RF4	2-C5 2-D6
RF5	2-C5 2-D6
RF6	2-C5 2-D6
RF7	2-C5 2-D6
RF8	2-B5 2-D6
RMBH/	2-B2 4-D3
RQGT0/	5-C4 5-D4
RST	1-A7 2-B1 3-A6 3-A8 3-B8 3-D3 5-A3 5-C4 5-D4
RST/	1-B2 1-B7 3-C5 4-B3 5-A3
RXINT	3-A5 3-D7
S0/	4-B3 4-D5 5-C2 5-C4 5-D4
S1/	4-B3 4-D5 5-C2 5-C4 5-D4
S2/	4-B3 4-D5 5-C2 5-C4 5-D4
SBX1CS0/	1-D6 3-B7
SBX1CS1/	1-D6 3-B7
SBX1I0	3-B7 3-D7
SBX1I1	3-B7 3-D7
SBX1O0	3-B7
SBX1O1	3-B7
SBX1P/	1-D7 3-B7
SBX2CS0/	1-D6 3-A7
SBX2CS1/	1-D6 3-A7
SBX2I0	3-A7 3-D7
SBX2I1	3-A7 3-D7
SBX2O0	3-A7
SBX2O1	3-A7
SBX2P/	1-D7 3-A7
SBXWT1/	1-B3 3-B7
SBXWT2/	1-B3 3-A7
SLAVE/	2-A4 2-A6 2-B3 2-B7 4-A6 4-A8 4-B8 4-D4 4-D5
SREGEN/	1-A7 1-B7 1-C6
STBCAS/	2-B1 2-C4
STQ0	1-A6 1-B7
STTCS/	1-C6
STXD	3-B3 3-B5

Signal Name	Location on Schematics
SWPEN/	4-C7 4-D3
T0INT	3-B5 3-D7
T1INT	3-B5 3-D7
TEST/	3-C3 5-D4
TIMEOUT/	1-B4 1-D2 3-D6
TXINT	3-B5 3-D7
VBB	1-B6 1-D2 2-B1 2-C6 4-C1 5-B4
WE0/	2-B1 2-C2 2-C3 2-C4 2-D3 2-D4
WE1/	2-B1 2-C1 2-C2 2-D1 2-D2
WRDEN/	4-D3 4-D7
WRRB/	2-B2 4-C7 4-D3 4-D7
WT3	1-B3 1-C7 2-C7
WT3/	1-B1 1-B3

Central Data

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