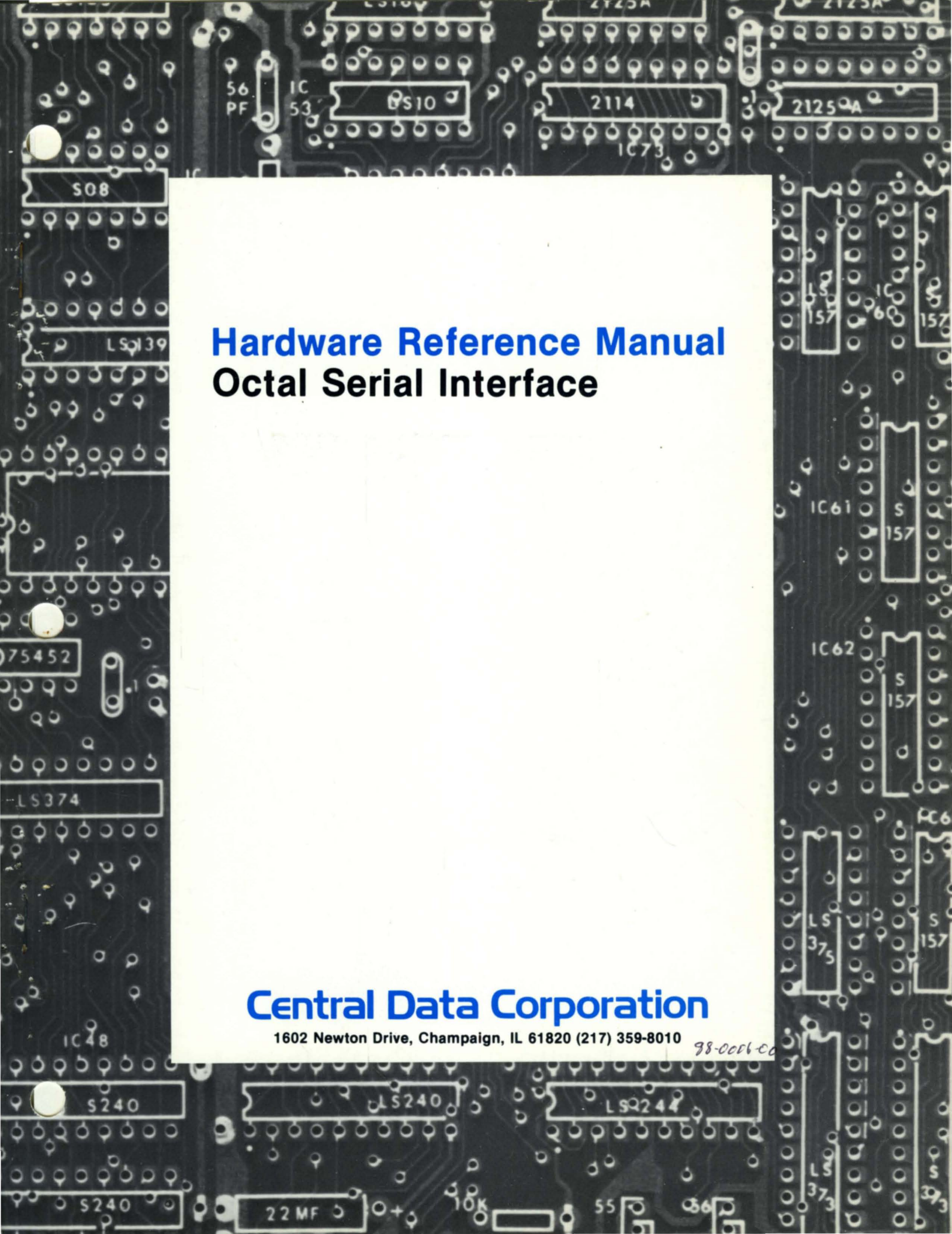

Hardware Reference Manual
Octal Serial Interface

Central Data Corporation
1602 Newton Drive, Champaign, IL 61820 (217) 359-8010

98-0006-00

Octal Serial Interface

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1. General Information

The Central Data Octal Serial Interface board is designed to expand the serial I/O capacity of any Multibus[1] system. The board uses the Signetics 2651 USART (Universal Synchronous/ Asynchronous Receiver/Transmitter) as the parallel to serial converter, and allows independent baud rates (transmission speeds) to be set for each of the board's eight channels.

The board supports standard EIA RS-232 interfaces, with the following pins used: TxD, RxD, DSR, CTS, DTR, and RTS. The board is capable of operating at baud rates ranging from 50 to 19,200 baud, and can be interrupt driven if so desired. Also, the board supports 16-bit I/O addressing as called for in the Multibus specification, with an option to use only 8-bit I/O addresses.

The board drives both the XACK and AACK lines of the Multibus to allow for the greatest flexibility. It can return either signal from 0-800ns after the receipt of a command, in 100ns increments. It is suggested that XACK be strapped to be equal to the access time of the board, while AACK can be strapped to allow the fastest possible system operation.

[1] Multibus is a trademark of Intel Corporation and is used throughout this manual.

2. Functional Description

The Octal Serial Interface board is divided into several major sections, which are described briefly below. For more detailed information, refer to the Principles of Operation section of this manual.

The addressing section of the board consists of the I/O address comparator and the chip-select generation circuitry for the USARTs. The board requires 32 I/O ports, which can be located on any 32-port boundary. Dip-switch I/O addressing allows the user to select the address of the board using either an 8- or 16-bit I/O address. With this ability, the board can work equally well in systems which generate a full 16-bit I/O address as well as in older 8-bit systems.

The bus interface of the board consists of the data bus buffers, interrupt circuitry, and the XACK/AACK generation logic. The data bus is buffered into and out of the board, and interrupts can be generated on the occurrence of any receiver full or transmitter empty condition. Finally, the XACK/AACK generation circuitry acknowledges all commands to the board and allows the system to run at the maximum possible speed.

Finally, the USART section is the actual interface to the external devices. This section is repeated on the board eight times, which gives eight totally independent channels. The interface between the on-board circuitry and the external connector is made through industry standard drivers and receivers, which guarantee proper RS-232 specifications.

3. Principles of Operation

This chapter details the operation of the entire interface board. Any signal names in this text followed by a slash (/) indicate that the signal is active-low.

As is all Central Data schematics, a grid system is provided to help locate sources and destinations of signals. The source of any named signal will have references to all locations on the schematics where the signal is used. At each location where a signal is used, a reference is given to where it was generated.

If the location is on the same sheet as it is being referenced, it will show only a grid location (i.e. D2). If, however, the referenced signal appears on a separate page, it will have the grid location preceded by the sheet number (i.e. 2-B5).

Addressing

Sheet 1 of the schematics includes the addressing circuitry for the board. The addressing function consists of determining when the board should be enabled as well as which USART is being accessed.

The board requires the use of 32 of the system's I/O ports. These ports can be started on any 32-port boundary, using either 8- or 16-bit addresses.

All of the address lines from the Multibus are buffered through 74LS04 gates. The buffered address lines are then routed to address decoding circuitry (A5-A15) and to chip selection circuitry (A0-A4).

The address decoding circuit consists of eleven 74LS266 open collector exclusive-NOR gates. All of the outputs of the gates are tied together, allowing any of the gates to pull the output low if its inputs do not match. If all of the pairs of inputs match, the common output is pulled high by a resistor to +5V.

One input from each of the gates goes to a buffered address line, with the other going to a dip-switch. This dip-switch, when closed, causes the corresponding gate input to become grounded. Under this circumstance, the address line leading to the same gate must also be low for the board to be addressed. If the switch position is left open, the input to the gate goes to a high state, thus comparing for a high address line.

To allow the selection between 8- and 16-bit I/O addressing, the outputs of the gates related to A8-A15 are connected through a shorting plug to the outputs of the gates related to A5-A7. If the shorting plug is installed, then the board decodes the full 16-bit address bus. If the shorting plug is removed, then the upper eight gates will not drive the common output, and thus only the lower three (A5-A7) are used for addressing.

When the address comparator is equal, pin 6 of IC39 will go high. This line is used in conjunction with pin 5 to enable the 74LS138 decoder. Pin 5 is low whenever an I/O command is currently on the bus.

When the 74LS138 is enabled, it uses the next lower three address lines (A4, A3, and A2) to select which USART should be enabled. In this manner, each USART has four consecutive addresses, for both reading and writing. The output of the decoder drives the chip-select pins of the USARTs. The R/W/ line of the USART is used to determine if a read or write operation is to occur when the chip is selected. When this line is high, a write will occur, while in read mode the line will be low.

In summary, the board uses 32 of the I/O ports on the system. The base address for these ports is selected with dip-switches, and the 32 ports are divided equally among the USARTs.

Bus Interface

The bus interface consists of the buffering circuits required from the Multibus, the interrupt driver, and the XACK/AACK generation logic. The bus interface circuitry is also found on sheet 1 of the schematics.

The data bus buffers consist of two 74LS242s, each one buffering four data lines. These are inverting buffers, thus immediately correcting for the inverted data on the bus. Since the directional enable pins of the buffers are of opposite polarity, they can be tied together, and are driven by a signal (pin 8 of IC28) which goes high whenever the board is addressed and an I/O read command is in progress. During all other conditions, this signal is low, thus sending data from the Multibus into the board.

The IORC/ and IOWC/ signals from the Multibus are also buffered (through 74LS08 gates) and used to set the level of the R/W/ line on the USARTs.

The interrupt circuitry takes the two bussed interrupt outputs from the USARTs (explained later) and allows them to be gated to

form an interrupt signal to the processor. If either the TINT/ or the RINT/ signal goes low, and it is jumpered into pin 8 of IC29 (with shorting plugs), it will cause a vectored interrupt to be generated on the selected line.

The board generates two command acknowledge signals. The first, XACK, indicates when a data transfer is complete and the processor can go to the next cycle. The other, AACK, gives the processor advance information related to when a transfer will be complete.

The circuit which generates the acknowledge signals consists of a shift register (74LS164, IC25) which is kept cleared when the board is not active. When an I/O command occurs, the clear input goes high, allowing the register to shift 1's through at the CCLK rate. The eight outputs of the shift register, which go high from 100-800ns after the time a command starts, can be jumpered to the SACK and AACK drivers (IC26). Note that since the command is asyncrhronous with respect to the bus clock the outputs may vary up to one clock cycle (i.e. the second output can occur anywhere from 100-200ns after command initiation).

The user can also select either acknowledge signal to be returned as soon as the board is selected by tying the driver's input high. The drivers are enabled whenever a command is occurring to this board, thus gating the proper timing onto the bus.

Sheet 1 of also contains the crystal oscillator which is used as a time-base for the USARTs. The oscillator is a simple feedback network, with the resistors used to bias the 7404 gates into their linear region, and the 100pf capacitor used to block any DC voltage to the crystal and to stablize operation. After buffering, this 5.0688MHz signal is sent to the eight USARTs, whose internal dividers generate baud rate clocks from it.

USART Section

Sheet 2 of the schematics shows the actual interface to the external devices. Note that this sheet is repeated eight times on the board, with the IC numbers listed for ports 0-7, in that order. Also, the signal CSX is referenced with the number 0-7 instead of the trailing "X" to indicate which USART is being used.

The format of the characters being sent and received is determined entirely by the USART and how it is programmed. Details on the programming of the 2651 are provided in the Signetics 2651 data sheet.

Note that there is one strap selection available for each USART. This strap, for CTS selection, is required because the USART will not transmit any characters unless its CTS/ pin is low. Since many serial devices do not drive this line, the strap labeled CTS INT allows the user to drive it from the RTS/ output of the USART. With this arrangement, whenever the RTS/ signal from a USART is low, it will be allowed to transmit. In the other mode, with the CTS EXT strap in place, the external device must drive CTS in order for the board to operate properly.

The USARTs can generate an interrupt on the occurrence of any transmitter empty or receiver full condition. All of these interrupt outputs are wire-ORed together to form a common transmitter interrupt and receiver interrupt signal. These two signals can be gated to any of the eight Multibus vectored interrupt lines (see the Bus Interface section).

All of the RS-232 signals from the external connector are buffered by 1489s. Note that capacitors can be added to slow the rise and fall times on all of the inputs to the USART. Normally, however, these additional capacitors are not needed.

4. Installation/User Selectable Options

The Octal Serial Interface is designed to operate in any standard Multlibus system. The board can occupy any card position of the system, since it does not operate as a bus master.

Addressing

The board has a 12-position dip-switch to select the port addresses it will respond to. Each position of the switch corresponds to one address line, from A5 to A15, with the right-most position not used. As marked on the board, A15 is selected by the left-most switch, while A5 is selected by the second from the right. An address line is compared for "0" if the switch is closed (up), as printed on the board. With the switch left open (down), the corresponding address line is compared for "1".

If 16-bit I/O addressing is to be used, a shorting plug must be placed over the two wire-wrap pins marked EXTENDED I/O. For systems where only 8-bit I/O addressing is used, this shorting plug should be left off. Also, for 8-bit systems, the upper eight address switches are not used.

CTS Selection

Since the USART will not transmit any data unless the CTS signal is active, the board allows the user to jumper it to a known state. This option can be used when the board is being connected to a simple device which does not generate this signal.

When the user wants the USART's RTS output to drive its CTS input, then a shorting plug should be placed in the USART's CTS INT position. This will allow the USART to transmit regardless of the state of the CTS signal from the external connector. If the user wishes CTS to be monitored from the device, then the CTS EXT position should be shorted. This will cause the output of the CTS buffer from the external connector to be run to the USART's CTS input.

Interrupt Selections

Each USART has its transmitter and receiver interrupt outputs tied to the others. The resulting two signals can be strapped to one of the vectored interrupt lines of the Multibus.

To allow transmitter interrupts, a shorting plug must be placed over the wire-wrap pins marked T INT. This plug should be left off to disable all transmitter interrupts for the board. Likewise, receiver interrupts are enabled by placing a shorting plug over the pins marked R INT.

Once the proper interrupt types are allowed, a vectored interrupt level must be established. The user can pick any level (0-7) to receive the interrupt by placing a shorting plug on the appropriately marked pins on the board.

XACK and AACK Generation

In order for the board to acknowledge processor commands, two lines are provided to indicate when a data transfer is complete. The XACK (transfer acknowledge) line is driven by the board when the transfer is completely finished, and the processor is allowed to complete the cycle. The AACK (advance acknowledge) is provided to allow systems to operate at their full speed potential (by preventing wait states), since it can be returned before XACK. Only XACK is used to indicate when a cycle can end, with the function of AACK to give advance information concerning the timing of the board.

Both of the lines can be strap selectable to return to the processor from 0-800ns after a command is received, in 100ns increments. The selection of timing for each line is done with shorting plugs placed over wire-wrap pins on the board.

The board has two rows of wire-wrap pins which are used for XACK/AACK generation. The top row is used for XACK, while the bottom row is for AACK. Each row consists of 9 pairs of pins, with each pair being one timing combination. To setup the board, the user needs to place a shorting plug in each row, under the timing number which he desires.

The timing numbers are marked to be the maximum return time for the signal involved (multiplied by 100ns). The minimum time is 100ns below the maximum time. For example, the pins marked "4" will return their signals from 300-400ns after a command is received. The pins marked "0" always return the signal immediately.

Since the XACK timing is tied to the access time of the board, the setting of that plug is suggested to be "3". The setting of the AACK strap will have to be determined by the system designer, using the information presented here.

If pin 25 of your system is being used for LOCK/ (as specified in the IEEE Multibus specifications), then the AACK driver must be disconnected by removing the shorting plug on the pins marked AACK ENBL. Leaving this on causes the board to drive pin 25 with the AACK signal when it is selected. This strap is available only on boards with revision A or greater.

One note--the timing for both acknowledge lines is dependent on the CCLK (constant clock) signal from the Multibus. It is assumed here that this clock is running at 10MHz, so if any other frequency is used on the system, the spacing between strap positions will be the period of the actual clock rather than 100ns. For example, a system with a 9.5MHz CCLK signal will have 105ns strap selection spacing.

5. Specifications

Word Size

8 bits

Addressing

This board requires 32 I/O ports. The base address for these ports can be on any 32 port boundary. Normally, 16-bit addressing is used for port selection. By changing a strap, however, 8-bit addressing can be selected.

Each USART requires four consecutively addressed ports, and their function is described below.

Address	Input Function	Output Function
0	Receiver data reg.	Transmitter data reg.
1	Status register	SYN1/SYN2/DLE regs
2	Mode register	Mode register
3	Command register	Command register

Access Time

350ns maximum

Baud Rates Available

50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200.

Interrupt Sources

Any transmitter empty or receiver full condition can trigger an interrupt on any of the eight vectored interrupt lines of the Multibus. Independent straps allow all transmitter interrupts or all receiver interrupts to be disabled.

RS-232 Specifications

The drivers and receivers used on the board are the 1488 and 1489 type. This provides a standard interface for the following lines: TxD, RxD, DTR, RTS, CTS, and DSR.

Interface

All signals meet the IEEE Multibus proposed specification.

12 Pin Edge Connector

Part Number: 345-012-500-201
Manufacturer: EDAC, 20 Railside Road, Don Mills, Ont. M3A1A4

Electrical Characteristics

Vcc= +5V ±5%
Vdd= +12V ±5%
Vbb= -12V ±5%
Icc= 1.2A typ, 2.0A max
Idd= 0.1A typ, 0.2A max
Ibb= 0.1A typ, 0.1A max

Environmental Characteristics

Operating Temperature: 0 C to +55 C
Relative Humidity: 0 to 90% (non-condensing)

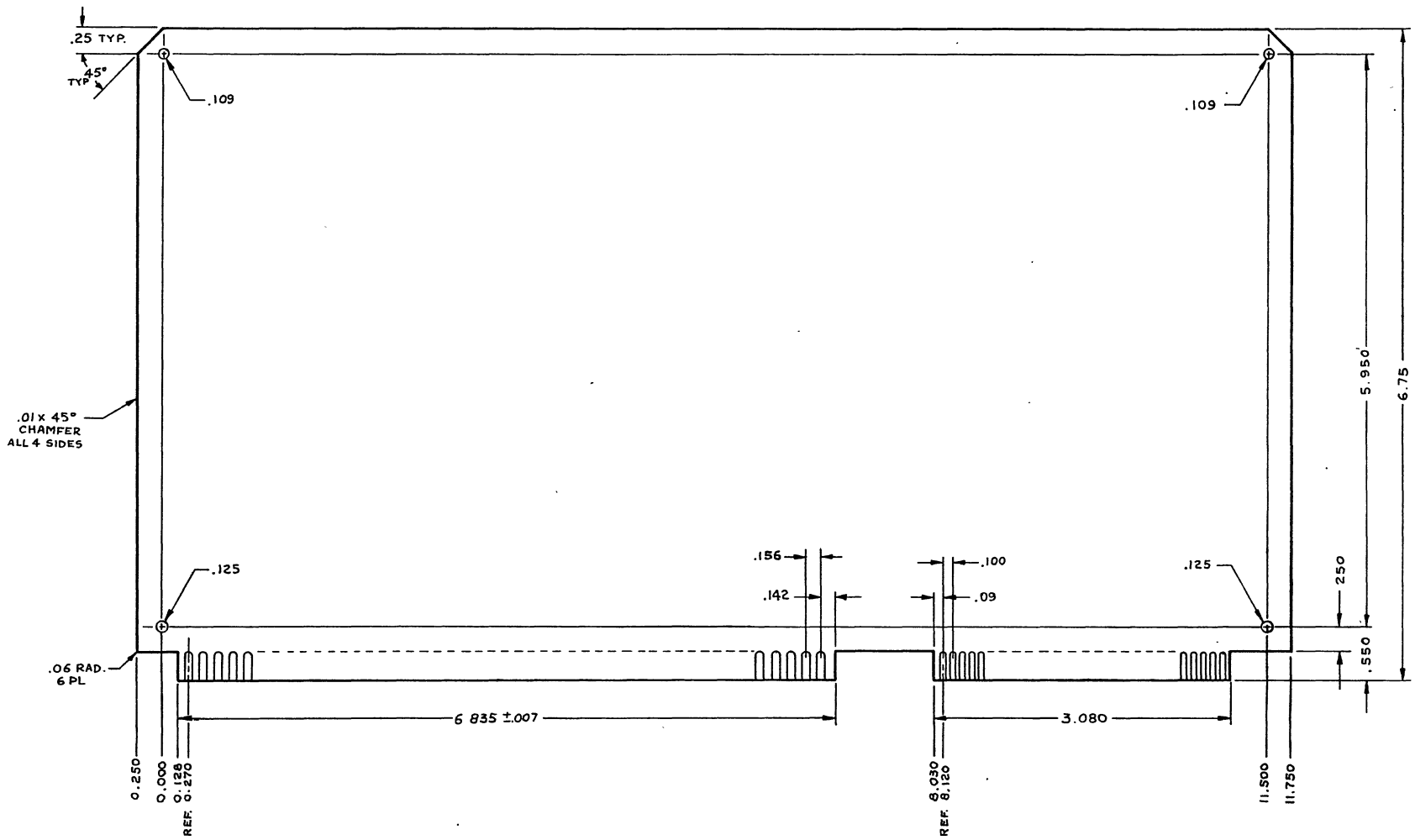
Physical Characteristics

Dimensions: see the basic Multibus dimensions on the following page. Each edge connector is 0.680" wide, with the right edge of each connector being 1.135", 2.360", 3.585", 4.810", 6.010", 7.235", 8.460", and 9.685" from the right-hand reference hole.

Weight: 9oz (255gm)

Ordering Information

Part Number: B1018
Description: Multibus Octal Serial Interface Board



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NO.

SHEET OF

MULTIBUS BOARD DIMENSIONS

6. **Schematics**

The following pages contain the schematics for the Octal Serial Interface board. A full description of the circuitry is given in the Principles of Operation section of this manual.

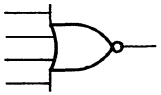
3 - INPUT 'AND' GATE

2 - INPUT 'OR' GATE

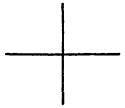
INVERTER

2 - INPUT 'NAND' GATE

4 - INPUT 'NOR' GATE

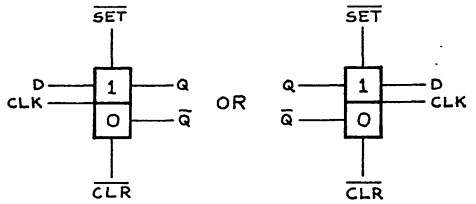


TWO LINES - NO CONNECTION

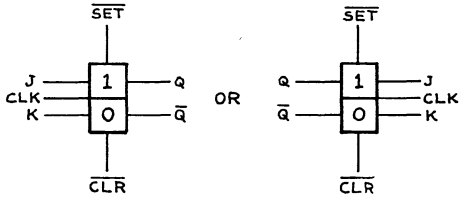


3 LINES - ALL CONNECTED

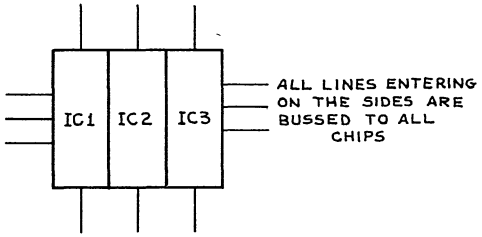
D-TYPE FLIP-FLOP



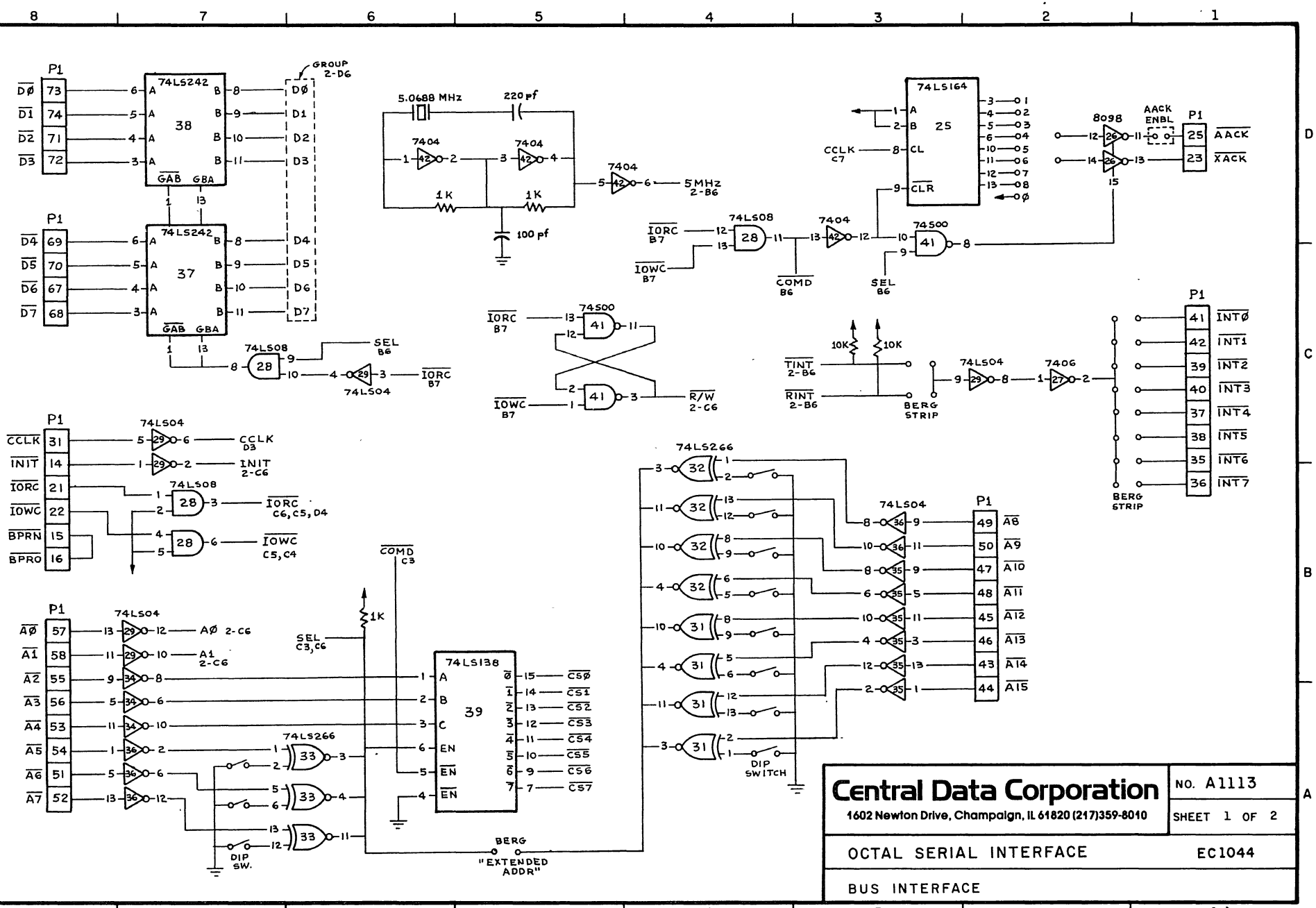
J/K FLIP-FLOP



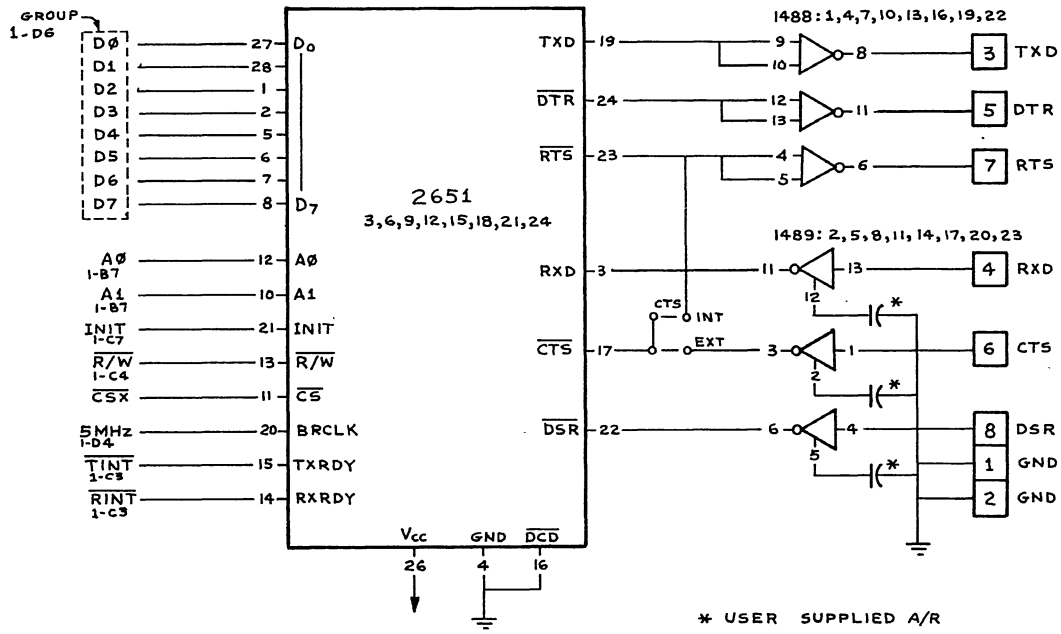
GROUP OF SIMILAR PARTS



Central Data Corporation 1602 Newton Drive, Champaign, IL 61820 (217)359-8010	NO. SHEET OF
DRAWING CONVENTIONS	



Central Data Corporation	NO. A1113
1602 Newton Drive, Champaign, IL 61820 (217)359-8010	SHEET 1 OF 2
OCTAL SERIAL INTERFACE	EC1044
BUS INTERFACE	



Central Data Corporation 1602 Newton Drive, Champaign, IL 61820 (217)359-8010	NO. A1112 SHEET 2 OF 2
OCTAL SERIAL INTERFACE	EC1044
UART SECTION – REPEAT 8 TIMES	

7. 2651 Data Sheets

The following pages contain the data sheets for the Signetics 2651 USART. This data sheet is reproduced with the permission and courtesy of Signetics Corporation.

DESCRIPTION

The Signetics 2651 PCI is a universal synchronous/asychronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- **Synchronous operation**
  - **5 to 8-bit characters**
  - **Single or double SYN operation**
  - **Internal character synchronization**
  - **Transparent or non-transparent mode**
  - **Automatic SYN or DLE-SYN insertion**
  - **SYN or DLE stripping**
  - **Odd, even, or no parity**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 0.8M baud (1X clock)**
- **Asynchronous operation**
  - **5 to 8-bit characters**
  - **1, 1 1/2 or 2 stop bits**
  - **Odd, even, or no parity**
  - **Parity, overrun and framing error detection**
  - **Line break detection and generation**
  - **False start bit detection**
  - **Automatic serial echo mode**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 0.8M baud (1X clock)**
    - **dc to 50k baud (16X clock)**
    - **dc to 12.5k baud (64X clock)**

OTHER FEATURES

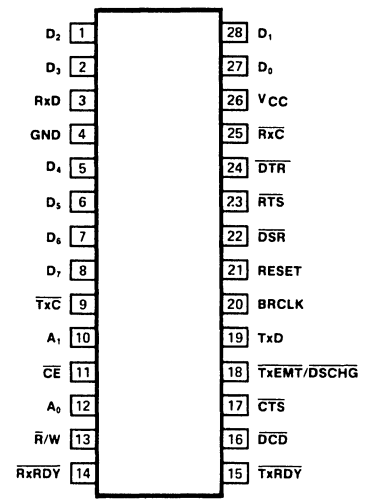
- **Internal or external baud rate clock**
- **16 internal rates-50 to 19,200 baud**
- **Double buffered transmitter and receiver**
- **Full or half duplex operation**
- **Fully compatible with 2650 CPU**
- **TTL compatible inputs and outputs**
- **Single 5V power supply**
- **No system clock required**
- **28-pin dual in-line package**

APPLICATIONS

- **Intelligent terminals**
- **Network processors**
- **Front end processors**
- **Remote data concentrators**
- **Computer to computer links**
- **Serial peripherals**

PIN CONFIGURATION

IQA PACKAGE



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1,2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	$\overline{R}/W$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

BAUD RATE	THEORETICAL FREQUENCY 16X CLOCK	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
50	0.8 KHz	0.8 KHz	--	6336
75	1.2	1.2	--	4224
110	1.76	1.76	--	2880
134.5	2.152	2.1523	0.016	2355
150	2.4	2.4	--	2112
300	4.8	4.8	--	1056
600	9.6	9.6	--	528
1200	19.2	19.2	--	264
1800	28.8	28.8	--	176
2000	32.0	32.081	0.253	158
2400	38.4	38.4	--	132
3600	57.6	57.6	--	88
4800	76.8	76.8	--	66
7200	115.2	115.2	--	44
9600	153.6	153.6	--	33
19200	307.2	316.8	3.125	16

NOTE

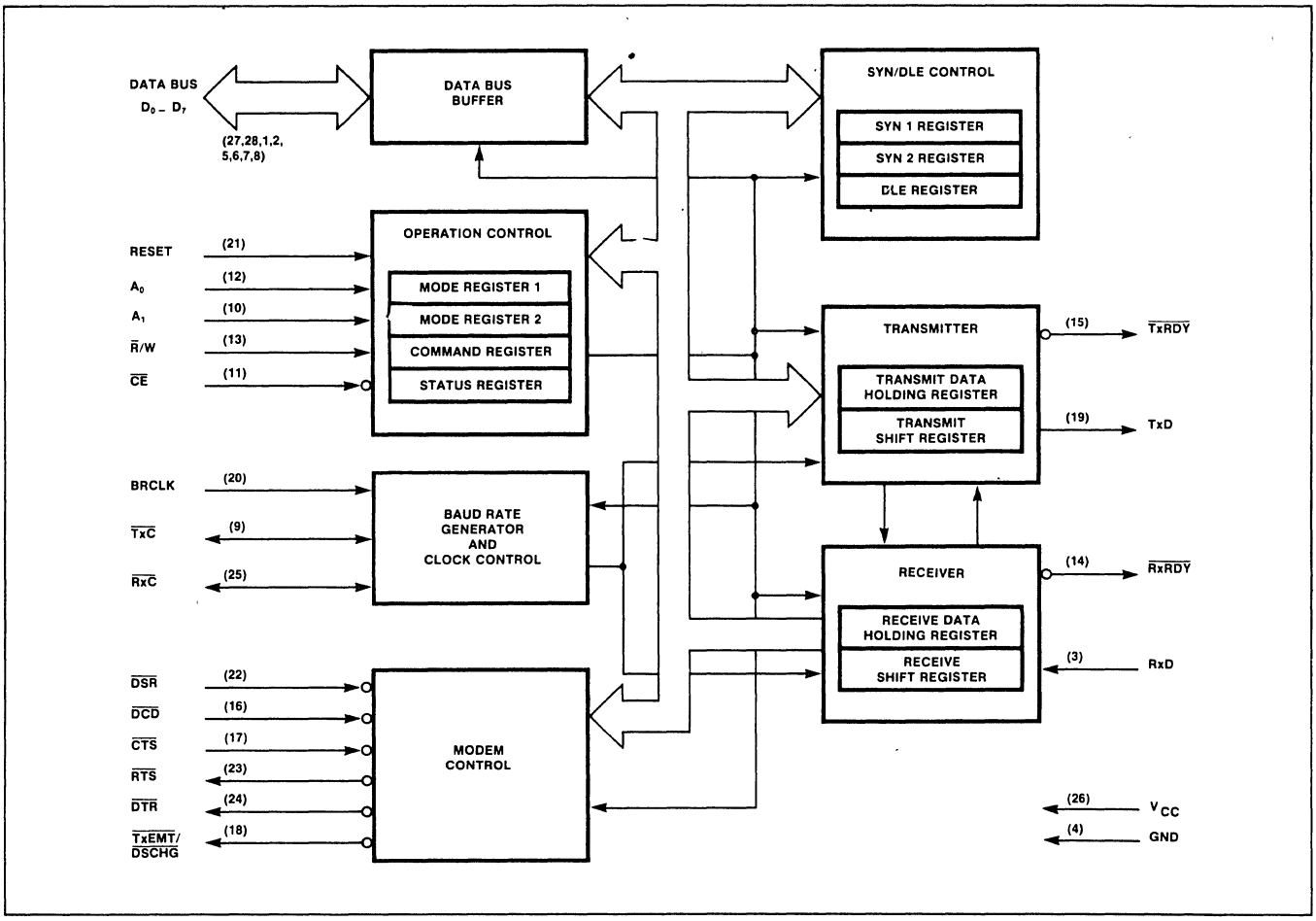
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.

Table 1 BAUD RATE GENERATOR CHARACTERISTICS
Crystal Frequency = 5.0688MHz

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10,12	I	Address lines used to select internal PCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the tri-state condition.
D_7-D_0	8,7,6,5, 2,1,28,27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of Status Register bit SR0. When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of Status Register bit SR1. When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}/\overline{DSCHG}$	18	O	This output is the complement of Status Register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Table 2 CPU-RELATED SIGNALS

BLOCK DIAGRAM



BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the PCI Programming section of this data sheet.

Timing

The PCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See Table 1.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The Transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the 2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin becomes an output at 1X the programmed baud rate.
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "Space" is low. Held in Mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data Carrier Detect input. Must be low in order for the receiver to operate. Its complement appears as Status Register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to Send input. Must be low in order for the transmitter to operate.
$\overline{DTR}$	24	O	General purpose output which is the complement of Command Register bit CR1. Normally used to indicate Data Terminal Ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of Command Register bit CR5. Normally used to indicate Request to Send.

Table 3 DEVICE-RELATED SIGNALS

OPERATION

The functional operation of the 2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI Programming section of this data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and the stop bit(s) have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are set if required. If a break condition is detected (RxD is low for the entire character as well as the stop bit (s)), only one character consisting of all zeros (with the FE status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode. In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the Holding Register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The 2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the Transmit Data Holding Register, these conditions are negated. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDI conditions are then asserted

again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the stop bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{\text{TxEMT/DSCHG}}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the 2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character. Since synchronous communications does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the command mode. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character.

PCI PROGRAMMING

Prior to initiating data communications, the 2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, the receiver and transmitter should be disabled if the change has an effect on the reception or transmission of a character. A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the $\overline{\text{CE}}$, $\overline{\text{R}}/\text{W}$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in Table 4.

2651 INITIALIZATION FLOW CHART

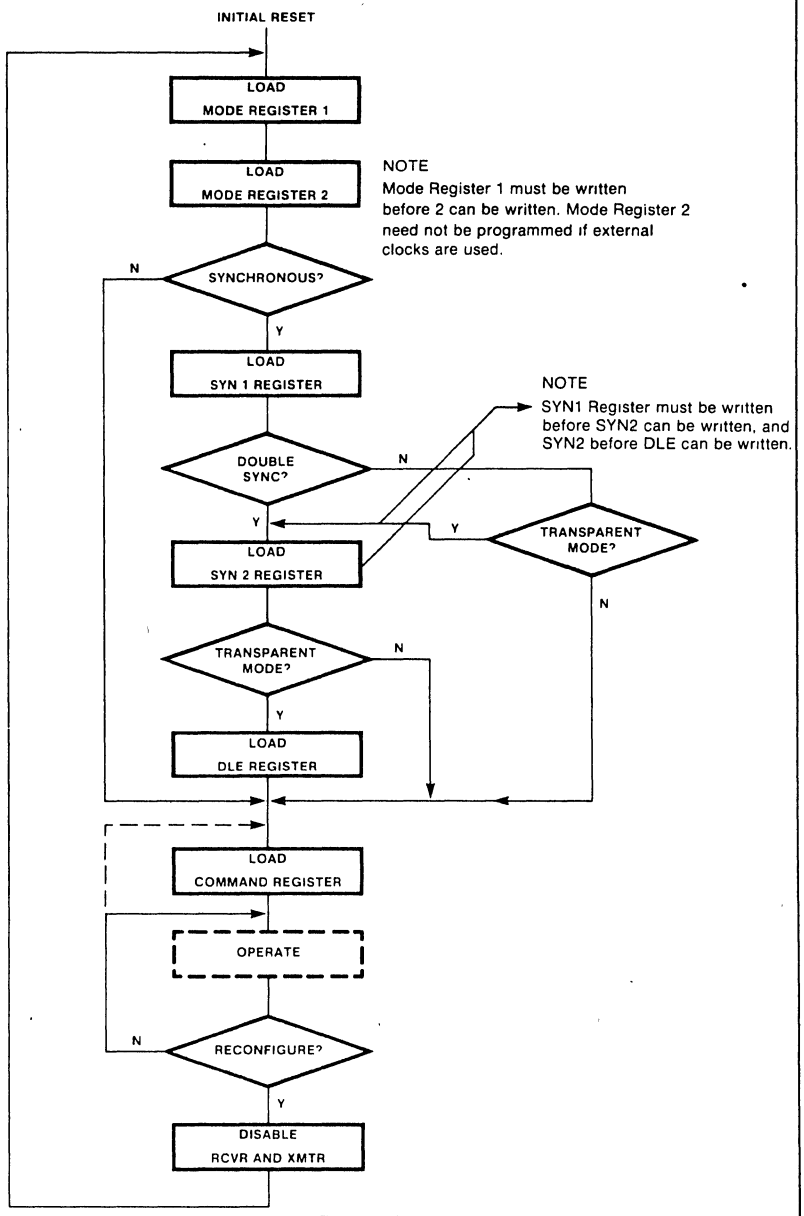


Figure 1

$\overline{\text{CE}}$	A_1	A_0	$\overline{\text{R}}/\text{W}$	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

Table 4 2651 REGISTER ADDRESSING

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and $\overline{R}/W = 1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The 2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode Registers 1 and 2 define the general operational characteristics of the PCI, while the Command Register controls the operation within this basic frame-work. The PCI indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asychronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1-SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill, but the normal synchronization sequence is used.

Mode Register 2 (MR2)

Table 6 illustrates Mode Register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688 MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5, 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the external inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00 = INVALID 01 = 1 STOP BIT 10 = 1 1/2 STOP BITS 11 = 2 STOP BITS		0 = ODD 1 = EVEN	0 = DISABLED 1 = ENABLED	00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		00 = SYNCHRONOUS 1X RATE 01 = ASYNCHRONOUS 1X RATE 10 = ASYNCHRONOUS 16X RATE 11 = ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0 = DOUBLE SYN 1 = SINGLE SYN	SYNCH: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT						

NOTE
Baud rate factor in asynchronous applies only if external clock is selected Factor is 16X if internal clock is selected.

Table 5 MODE REGISTER 1 (MR1)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	Receiver Clock	Baud Rate Selection			
NOT USED		0 = EXTERNAL 1 = INTERNAL	0 = EXTERNAL 1 = INTERNAL	0000 = 50 BAUD 0001 = 75 0010 = 110 0011 = 134.5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 BAUD 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 6 MODE REGISTER 2 (MR2)

Command Register (CR)

Table 7 illustrates Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for a least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared. This bit resets automatically.

The PCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6 = 01 places the PCI in the Automatic Echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6 = 01 places the PCI in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR. However, only the first SYN1 of an SYN1-SYN1 pair is stripped.
3. In transparent mode (MR16 =1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. Receive clock = transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6 = 11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the Status Register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the CPU and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error		Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = NORMAL OPERATION 01 = ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		0 = FORCE $\overline{RTS}$ OUTPUT HIGH 1 = FORCE $\overline{RTS}$ OUTPUT LOW	0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REG (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0 = NORMAL 1 = FORCE BREAK **SYNCH: SEND DLE** 0 = NORMAL 1 = SEND DLE	0 = DISABLE 1 = ENABLE	0 = FORCE $\overline{DTR}$ OUTPUT HIGH 1 = FORCE $\overline{DTR}$ OUTPUT LOW	0 = DISABLE 1 = ENABLE

Table 7 COMMAND REGISTER (CR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ INPUT IS HIGH 1 = $\overline{DSR}$ INPUT IS LOW	0 = $\overline{DCD}$ INPUT IS HIGH 1 = $\overline{DCD}$ INPUT IS LOW	**ASYNCH:** 0 = NORMAL 1 = FRAMING ERROR **SYNCH:** 0 = NORMAL 1 = SYN CHAR DETECTED	0 = NORMAL 1 = OVERRUN ERROR	**ASYNCH:** 0 = NORMAL 1 = PARITY ERROR **SYNCH:** 0 = NORMAL 1 = PARITY ERROR OR DLE CHAR RECEIVED	0 = NORMAL 1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0 = RECEIVE HOLDING REG EMPTY 1 = RECEIVE HOLDING REG HAS DATA	0 = TRANSMIT HOLDING REG BUSY 1 = TRANSMIT HOLDING REG EMPTY

Table 8 STATUS REGISTER (SR)

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the CPU. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the CPU reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. It is cleared when the transmitter is enabled by CR0 and does not indicate transmitter condition until at least one character is transmitted. It is also cleared when the Status Register is read by the CPU. When SR2 is set, the $\overline{TxEMT}$/$\overline{DSCHG}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE Register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character is single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, and when the Status Register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% [4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low			0.8		
V_{IH}	High			2.0		
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA		0.25		
V_{OH}	High	I_{OH} = -100uA		2.8		
I_{IL}	Input load current	V_{IN} = 0 to 5.5V		10		μA
Tristate	Output leakage current					μA
I_{LH}	Data bus high	V_O = 4.0V		10		
I_{LL}	Data bus low	V_O = 0.45V		10		
I_{CC}	Power supply current			90		mA

CAPACITANCE $T_A = 25°C$, $V_{CC} = 0V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Capacitance					pF
C_{IN}	Input	fc = 1MHz			20	
C_{OUT}	Output	Unmeasured pins tied to ground			20	
$C_{I/O}$	Input/Output				20	

PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Pulse width					ns
t_{RES}	Reset			1000		
t_{CE}	Chip enable			200		
	Setup and hold time					ns
t_{AS}	Address setup			10		
t_{AH}	Address hold			10		
t_{CS}	$\overline{R}$/W control setup			10		
t_{CH}	$\overline{R}$/W control hold			10		
t_{DS}	Data setup for write			150		
t_{DH}	Data hold for write			80		
t_{RXS}	Rx data setup			150		
t_{RXH}	Rx data hold			280		
t_{DD}	Data delay time for read	$C_L = 100pF$		180		ns
t_{DF}	Data bus floating time for read	$C_L = 100pF$		70		ns
	Input clock frequency					MHz
f_{BRG}	Baud rate generator		5.0637	5.0688	5.0738	
$f_{R/T}$	$\overline{TxC}$ or $\overline{RxC}$		dc	1.0		
	Clock state					ns
t_{BRH}	Baud rate high			90		
t_{BRL}	Baud rate low			90		
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high (duty cycle)		44%	50%	56%	
$t_{R/TL}$	$\overline{TxC}$ or $\overline{RxC}$ low (duty cycle)		44%	50%	56%	
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	$C_L = 100pF$		300		ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[8]	$C_L = 100pF$		0		ns

NOTES

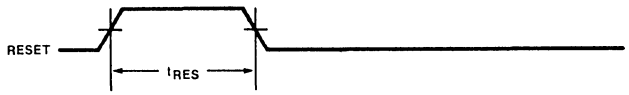
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified
5. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IH}, V_{IL} levels as appropriate
6. Typical values are at +25°C, typical supply voltages and typical processing parameters
7. $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open drain.
8. Parameter applies when internal transmitter clock is used.

PRELIMINARY SPECIFICATION

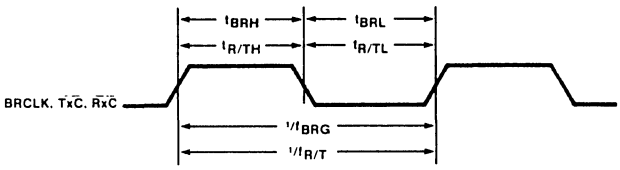
Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS

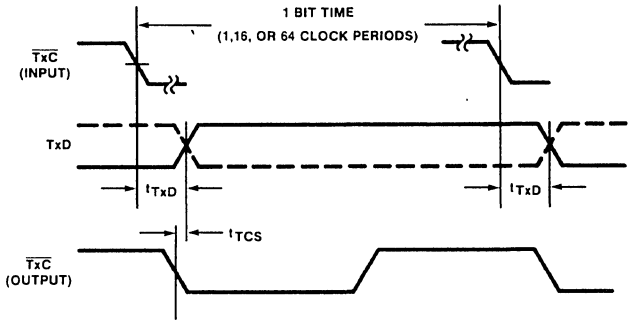
RESET



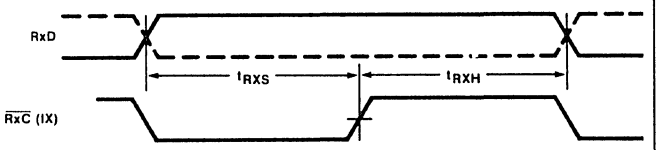
CLOCK



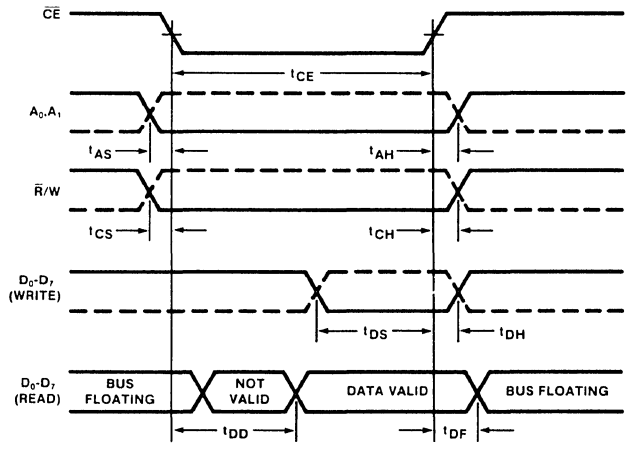
TRANSMIT



RECEIVE

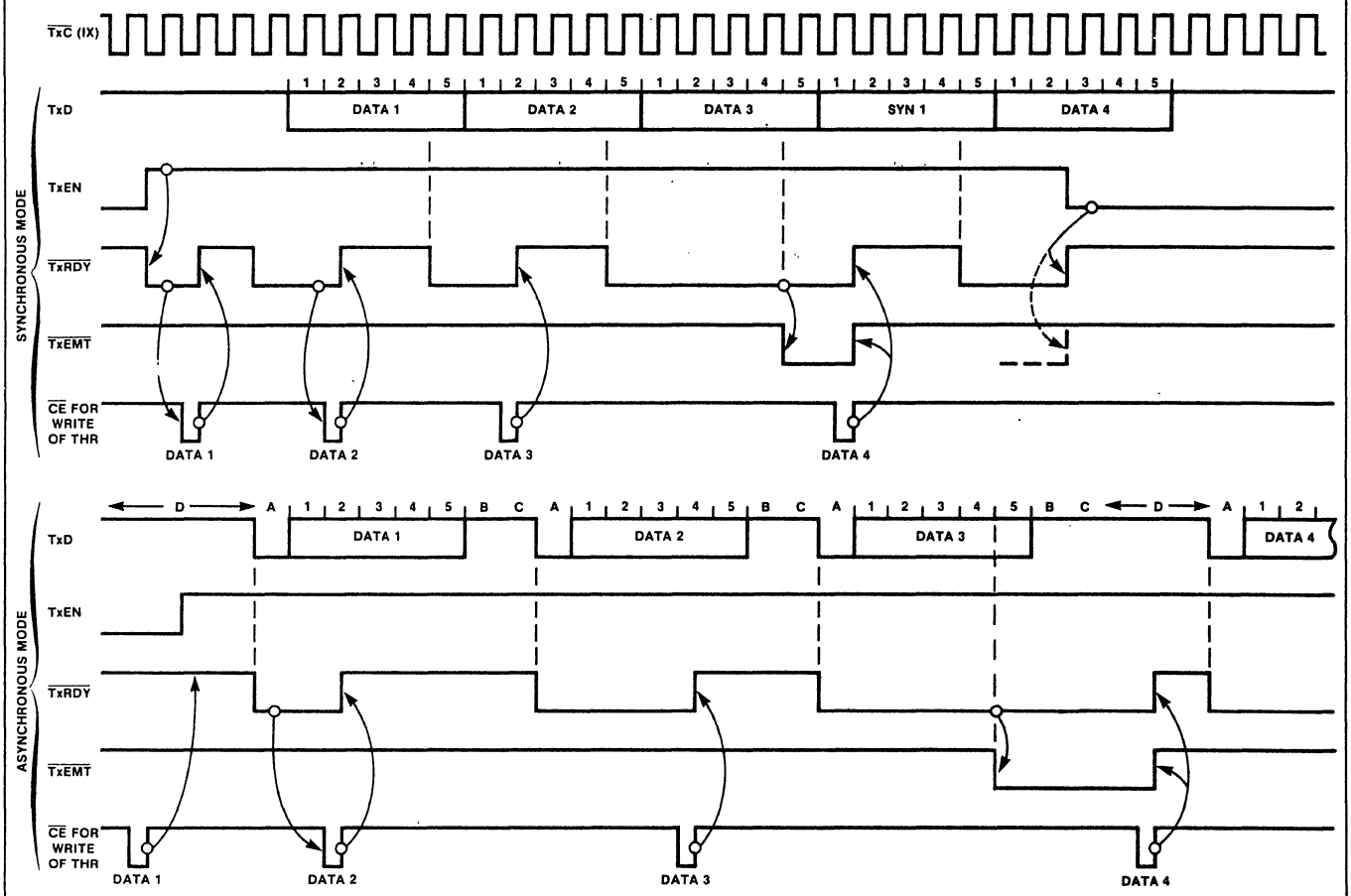


READ AND WRITE



TIMING DIAGRAMS (Cont'd)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



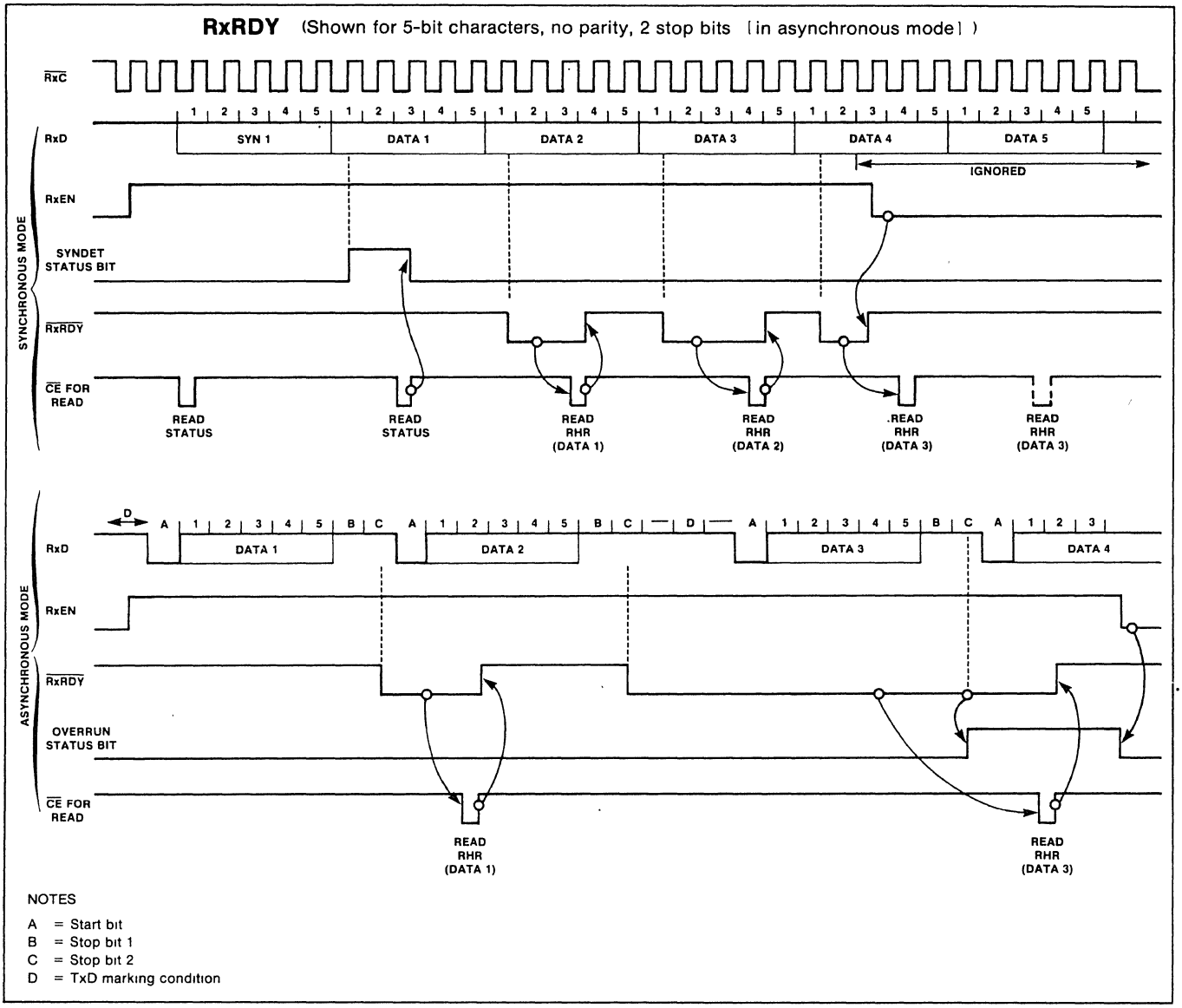
NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Cont'd)

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

Central Data Corporation
1602 Newton Drive, Champaign, IL 61821-1098 (217)359-8010

June 21, 1983

TO: All Edge Connector Customers

FROM: Engineering

It should be noted that all EC12/EC26 connectors which are manufactured by EDAC Corporation (which Central Data sells) are stamped with the odd and even pin numbers reversed.

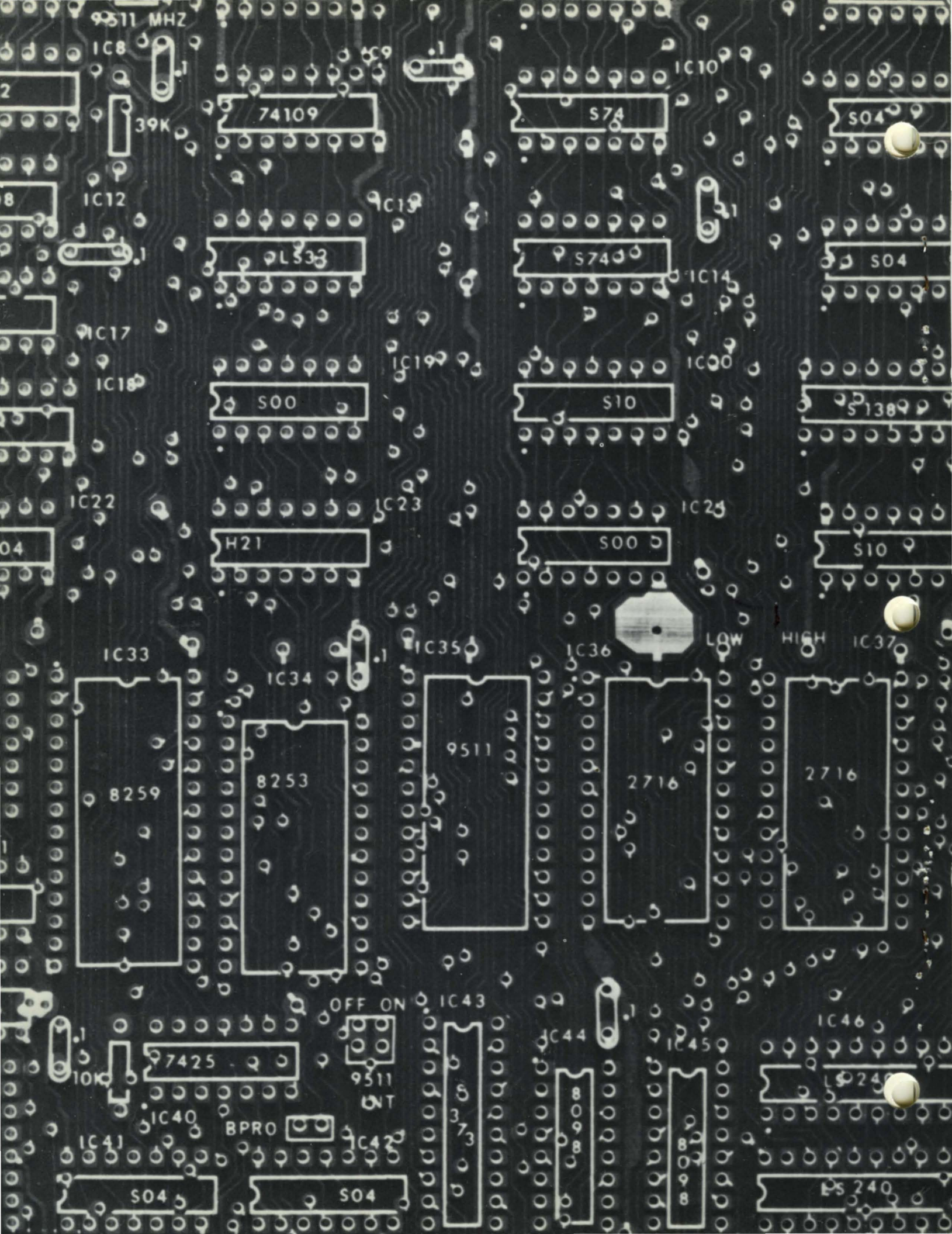
The pin numbers for the edge connectors that correspond to the schematic diagrams in our manuals are those numbers silkscreened on our board. Therefore, when wiring cables, you should be careful to use the pins corresponding to our silkscreened numbers, rather than the pins corresponding to the numbers stamped on the connectors themselves.

JJR/slb

Central Data Corporation
1602 Newton Drive, Champaign, IL 61820 (217)359-8010

NOTICE TO CUSTOMERS
(Effective March 10, 1983)

Due to a recent Engineering change, Central Data's Octal Interface boards (both Serial and Intelligent) will now have 2661 integrated circuits in place of the 2651 chips formerly used. This change has no detrimental effect on the board's performance whatsoever.


9.511 MHZ
IC8
.1
39K
74109
IC10
S74
S04
IC12
.1
IC13
LS33
S74
IC14
S04
IC17
IC18
IC19
S00
IC20
S10
S138
IC22
IC23
H21
IC24
S00
S10
IC33
IC34
IC35
IC36
LOW
HIGH
IC37
8259
8253
9511
2716
2716
OFF ON
IC43
IC44
IC45
IC46
7425
10K
9511
INT
IC40
BPRO
IC41
IC42
S04
S04
373
8098
8098
LS240
LS240