MAGNETIC PERIPHERALS, INC.
a Control Data Company

INTERFACE SPECIFICATION

FOR

IPI PHYSICAL LEVEL

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TWIN CITIES DISK DIVISION

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ILLUSTRATIONS

1.0 SCOPE

This Specification covers the physical aspects of the IPI I/Os (IPI-0, IPI-1, IPI-2, IPI-3); i.e., the hardware involved, the system configurations, the control sequences, and the timing, without regard to the content of the information being processsed.

The purpose is to help in the development and use of computer systems by providing a common IPI physical interface for connecting a variety of peripheral devices (disk and tape drives, printers, terminals, etc.).

2.0 APPLICABLE DOCUMENTS

SPEC 64731600	- Interface Specification for IPI-2
ANSC X3.129-1986	- IPI Physical Level Standard
ANSC X3T9.3/83-4	- IPI Device Generic - Disk Specification
EIA Standard RS-485	- Electrical Characteristics of Generators and Receivers

3.0 EDITORIAL CONVENTIONS

Certain terms used in this document which are proper names of signals, state mnemonics, or similar terms are printed in uppercase to avoid possible confusion with other uses of the same words. Any lowercase uses of these words have the normal English meaning. Examples printed in uppercase are BUS A, SLAVE IN, SYNC OUT, DESEL, SLAVEND.

A number of conditions, sequence parameters, events, English text, states or similiar terms are printed with the first letter of each word in uppercase and the rest lowercase. Any lowercase uses of these words have the normal English meaning. Examples printed with the first letter uppercase are In, Out, Selective Reset, Bidirectional, Bus Control, Operation Response.

4.0 GLOSSARY OF TERMS

Bidirectional - This term refers to the use of signal lines which may be asserted by either the master or a slave, but not concurrently.

Bus Acknowledge - In the optional configuration where the master permits the slave to define the type of Information Transfer to be executed, Bus Acknowledge is the BUS B equivalent of Bus Control.

Bus Control - This term refers to the Physical Interface Bus Control octet asserted on BUS A by the master during the Bus Control sequence. It is used to define the bus configuration for the subsequent Information Transfer.

Bus Exchange - This term refers to the Bus Control sequence (initiated by the master) and the Ending Status sequence (initiated by the slave), which are used to frame an Information Transfer (which may or may not have occurred). For every Bus Control sequence there shall be an Ending Status sequence.

Busy - A slave is Busy when it is currently unable to process Bus Exchanges or Information Transfers.

Data - This term refers to information transferred over the Physical Interface, other than that defined as Operation Commands and Operation Responses by the Logical Interface.

Data Streaming - This term refers to the transfer of information in a non-interlocked manner in order to achieve faster transfer rates.

Dominant Slave - A slave capable of assuming the role of the master for slave to slave Information Transfers.

DOM (Double Octet Mode) - This term refers to a mode of Information Transfer which uses BUS A and BUS B in parallel in a bidirectional manner to transfer 16 bits concurrently.

Ending Status - This term refers to the Physical Interface status octets presented by the master (optional) and the slave (mandatory), immediately following an Information Transfer.

Facility - This term refers to the entity addressable by the master through the slave.

Housekeeping - This is a function made available at the Logical Interface which permits the master to ascertain the attributes of the attached slaves.

Information Transfer - This term refers to interchanges on the interface associated with the Logical Interface; i.e., Operation Commands, Operation Responses and Data)

Interlocked - This term refers to the handshake between master and slave of signals on the interface.

Level 0 - This term refers to the electrical and mechanical characteristics of the Physical Interface.

Level 1 - This term refers to the bus states, sequences and other rules (excepting electrical and mechanical characteristics of Level 0) that govern the use of the Physical Interface.

Logical Interface - This term refers collectively to all protocols higher than the Physical Interface specified in this document.

Maintenance Mode - This term refers to the capability for a master to initiate analysis of the interface, and restore operation after a failure condition.

Mandatory - Unless otherwise described as Optional or MPI Unique, the definition of the Physical Interface as described is mandatory for all masters and slaves. The functions must be implemented as defined in this document.

Master - This term refers to the entity in control of the interface.

Master Status - In the optional configuration where the master permits the slave to define the type of Information Transfer to be executed, Master Status is the BUS A equivalent of Slave Status.

Operation Command - This term refers to a command issued by the master to initiate some specific operation which is outside the Physical Interface and is associated with a Logical Interface function.

Operation Response - This term refers to the response of a slave to an Operation Command. It is associated with the Logical Interface.

Optional - This term describes features which are not required by this document. However, if any feature defined by this document is implemented, it must be done as defined herein.

Physical Interface - This term denotes the mechanical, electrical, and interface protocols specified in this document. In use this term contrasts with the term Logical Interface.

Sequence - This term refers to a series of states which follow each other in a definite order to accomplish a function.

SOM (Single Octet Mode) - This term refers to a mode of Information Transfer which uses BUS A in a unidirectional manner to transfer 8 bits of information from master to slave, and BUS B in a unidirectional manner to transfer 8 bits of information from slave to master.

Slave - This term refers to the addressable entity under control of, and directly connected to, the master.

Slave Status - This is the status asserted on BUS B by the slave at the completion of an Information Transfer (which may or may not have occurred).

State - This term is used to define the immediate condition of the interface, excluding transitions, as indicated by the control signals.

Unidirectional - This term refers to the use of signal lines which are not asserted by both the master and slave (either concurrently or successively).

5.0 PHYSICAL CHARACTERISTICS OF THE HARDWARE

5.1 Cable-Connector Assemblies (See Figure 1)

Each cable shall be assembled with a male cable connector on one end and a female connector on the other end.

The outer shield of the 50 conductor shielded cable is terminated at the connector shell.

Cable assembly pin assignments are shown in Table 1.

5.2 Cables

The following cables are representative of the types used for the IPI. Cables may have an overall shield, suitable for terminating in a metal shielded connector. This overall shield serves the purpose of a signal shield.

5.2.1 28 AWG Internal Round Cable

This type cable may be used to interconnect several devices inside a common cabinet.

Cable shall consist of 50 conductors (25 twisted pair) of 28 AWG. The following characteristics apply to the twisted pairs within the bulk cable assembly.

CHARACTERISTIC IMPEDANCE:	120 ±12 Ω
DC RESISTANCE:	70 Ω max/1000 feet at 20°C
SIGNAL ATTENUATION:	0.029 db max/foot at 5 MHz
VELOCITY OF PROPAGATION:	60% ±10% C
PAIR TO PAIR PROPAGATION DELAY DELTA:	0.15 ns max/foot

5.2.2 28 AWG External Round Cable

This type of cable may be used to interconnect several devices cabinet to cabinet.

Cable shall consist of 50 conductors (25 twisted pair) of 28 AWG. The following characteristics apply to the twisted pairs within the bulk cable assembly.

CHARACTERISTIC IMPEDANCE:	120 ±12 Ω
DC RESISTANCE:	65 Ω max/1000 feet at 20°C
SIGNAL ATTENUATION:	0.029 db max/foot at 5 MHz
VELOCITY OF PROPAGATION:	77% ±05% C
PAIR TO PAIR PROPAGATION DELAY DELTA:	0.10 ns max/foot

5.3 Connectors

The connectors used shall be the industry standard 50 Pin Subminiature D, plug and receptacle.

The shells of shielded connectors shall be plated with conductive material to ensure the integrity of the cable shield to chassis current path. The resistance of the cable shield to equipment chassis shall not exceed 5 mΩ, after a minimum of 500 connect and disconnect cycles.

5.4 Terminators

The terminators shall fit within the same dimensions as the cable end connectors, and shall be secured by the same retention method as the cable connectors.

5.5 Differential Drivers/Receivers

The differential driver and receiver shall meet the requirements of the EIA Standard RS-485, which specifies the electrical characteristics of generators (drivers) and receivers for use in a balanced digital multipoint system.

Transceiver pin assignments are shown in Table 1.

6.0 SYSTEM CONFIGURATIONS

The IPI has been designed to operate with three defined elements of a computer system; master, slave, and facility.

6.1 Master

The master manages the slave(s) and is responsible for control of the interface. It is the master's responsibility to operate the slaves according to their capabilities.

6.2 Slave

The slave is managed by the master and may or may not have intelligence, depending on the command set it is capable of executing. In an intelligent configuration it can support a master which is oriented to generic device characteristics such as a disk with 22,000 blocks of data, each 512 bytes long. In a device-oriented configuration it can support a master oriented to specific device characteristics; e.g., a disk with 10,000 bytes/track, 7 tracks/cylinder, 500 cylinders/actuator.

6.3 Facility

The facility is addressable through the slave. It is the responsibility of the slave to manage the facility. A facility may or may not have generic functionality and may or may not be a device.

6.4 Multi-Tier Structure

Figure 2 (A) illustrates a mainframe configuration and in a parallel manner shows that the Storage Director can be both slave to the CPU and master to the String Control. The CPU can directly address the String Control through the Storage Director.

The figure also shows the String Control can be both slave to the Storage Director and master to the Device. The Storage Director can directly address devices through the String Control.

Figure 2 (B) illustrates a minicomputer configuration and in a parallel manner shows that the Controller can be both slave to the CPU and master to the Device. The CPU can directly address devices through the Controller.

Figure 3 illustrates cabling alternatives for configurations that have a master at one end of the cable, a slave at the other, with intermediate slave(s). Other electrically valid configurations may be used, even if they are not shown.

6.5 Cable Configuration

A maximum of 8 slaves may be connected to the master. Typically, this would be by a daisy chain signal cable configuration, but radial connection is permitted. Some precautions must be taken to properly handle interface features such as dominant slaves if radial connections are used.

Flat and round cable assemblies may be interconnected. Cables with 50-pin connectors allow cables to be joined if a slave has to be removed from the interface for any reason (this is the rationale for requiring alternating retention hardware on opposite ends of the cable). It is also possible to use a single connector with both an in and an out cable such that the daisy chain is not broken by the removal of a slave or facility.

When using the shielded connector in a daisy chain configuration, the master shall have a female panel connector per channel, and each slave shall have both a female and a male panel connector per channel. Line termination shall be provided at both ends of the daisy chain.

The maximum cumulative cable length in a daisy chain is 213 feet.

The minimum cable configuration dependent time period is 200 ns

The maximum streaming transfer rates are:

Single octet mode - 5 MB/s
Double octet mode - 10 MB/s

Interlocked transfer rates may exceed these rates over short distances.

7.0 INTERFACE

The purpose of the interface is to exchange information between connected devices and meet the criteria of:

1. Content Independence - The operation of the interface is not affected by the contents of Information Transfers.

2. Speed Independence - The control of the interface is not timing critical in handling of the interface protocol.

3. Protocol Integrity - The integrity of the protocol sequences is ensured by requiring that each signal change be handshaked. No more than one signal is permitted to change at any time, except during optional Data Streaming transfers.

The characteristics of the physical interface are:

1. A daisy chained cable consisting of 24 signal pairs.

2. Master/Slave mode of execution.

3. One master only.

4. Up to 8 slaves allowed, with up to 16 facilities per slave.

5. Master selection of slave.

6. Except for Selection, a master can allocate control of interface functions to a dominant slave.

7. Bus Exchanges are used to frame Information Transfers and are executed only as interlocked and unidirectional.

8. Information Transfers occur using either the unidirectional configuration or in a 16 bit bidirectional configuration. The two can co-exist on the same cable.

9. Information Transfers are asynchronous and interlocked except during Data Streaming.

10. Information Transfers can be terminated in either direction by either the master or the slave.

11. The terms In and Out are always used in reference to the master.

The following apply to the use of BUS A and BUS B.

1. The uses of BUS A and BUS B are structured to optimize operations between Bus Exchanges and Information Transfers.

2. The Bus Control sequence is initiated by the master and is associated with control of the Physical Interface. The Ending Status sequence is initiated by the slave and is associated with reporting the status of the Bus Exchange or the preceding Information Transfer.

3. During Bus Exchanges BUS A is unidirectional Out from the master for Bus Control and Master Status (optional), and BUS B is unidirectional In to the master for Bus Acknowledge (optional) and Slave Status.

4. Information Transfer is the term used to indicate the various types of information (Data, Operation Command, or Operation Response) that are transparently transferred across the Physical Interface.

5. Bus Exchanges are defined as framing (bracketing) Information Transfers. The differentiation between Bus Exchanges and Information Transfers allows a simple state machine to control Bus Exchanges e.g. the timing independent Bus Exchanges can be interpreted by a general purpose microprocessor.

6. Only one control signal shall change at a time between master and slave, and an In control signal change shall be interleaved with an Out control signal change such that the source of control signal changes is alternated between them, thus effectively interlocking all control functions. Optional Data Streaming transfers need not comply with this requirement.

7. Operation Commands are issued by the master and are associated with operation of the Logical Interface. Operation Responses are returned by the slave. Both occur as Information Transfers.

8. During Information Transfers there can be two modes:

   a. In Single Octet Mode, Information Transfers are 8 bit unidirectional; i.e., BUS A Out, BUS B In.

   b. In Double Octet Mode BUS A and BUS B are used to transfer 16 bits in parallel either In or Out as required.

9. If unused bits are listed as "Reserved" they shall be set to zero. The sender is responsible for ensuring zeros. The receiver may choose whether or not to verify that the zeros are present.

10. If unused bits are listed as undefined then there is no requirement for either sender or receiver to care about content. Octet parity must still be maintained.

11. In states where the Bus contents are bit significant addresses, octet parity need not be correct.

12. Parity shall be generated by the originator and checked by the receiver, except where noted.

7.1 Signals

The interface signals are summarized in Figure 4.

7.1.1 Signal Nomenclature

The nomenclature used to define voltage levels, signal states, logical states, and their correlation to each other is defined in Table 2.

7.1.2 Signal Usage

7.1.2.1 Select Out

SELECT OUT is sent from the master to the slave(s) to select a slave and maintain selection. When SELECT OUT is inactive all slaves shall release BUS A. Dominant slaves shall release MASTER OUT and SYNC OUT drivers upon sensing the negation of SELECT OUT by the master.

7.1.2.2 Slave In

SLAVE IN is used by the slave to either indicate acknowledgement of master initiated control sequences, or to terminate Information Transfers.

7.1.2.3 Master Out

MASTER OUT is used by the master to initiate or terminate Information Transfers, Request Interrupts, Request Transfer Mode, or Reset slave(s).

7.1.2.4 Sync In

When SYNC IN is asserted during transfers In, information is valid on the Bus(es). When SYNC IN is asserted during transfers Out the slave is ready to accept information.

NOTE: To deskew, the information In is asserted on the bus(es) a minimum time before SYNC IN is asserted. SYNC IN is asserted to acknowledge the Bus Control octet during the Bus Control sequence.

7.1.2.5 Sync Out

When SYNC OUT is asserted during transfers In the information has been accepted by the master. When SYNC OUT is asserted during transfers Out information is valid on the bus(es).

NOTE: To deskew, the information Out is asserted on the bus(es) a minimum time before SYNC OUT is asserted. SYNC OUT is asserted to initiate the Bus Control sequence.

During reset, SYNC OUT is asserted without response for a minimum time (see Figures 12 and 16).

7.1.2.6 Bus A

BUS A consists of nine lines (Bits 7 - 0 plus parity). Bit 7 is the most significant bit. Parity is odd.

BUS A is used by the master for all control sequences. For Information Transfers in Single Octet Mode, all information is passed from the master to the slave on BUS A. In Double Octet Mode information is passed from the master to the slave or from the slave to the master on BUS A. BUS A is considered to be the first octet of double octet information. BUS A shall be released by all slaves when SELECT OUT is negated.

7.1.2.7 Bus B

BUS B consists of nine lines (Bits 7 - 0 plus parity). Bit 7 is the most significant bit. Parity is odd.

BUS B is used by the slave for all control sequences. For Information Transfers in Single Octet Mode, all information is passed from the slave to the master on BUS B. In Double Octet Mode information is passed from the slave to the master or from the master to the slave on BUS B. BUS B is the other octet in a double octet of information.

7.1.2.8 Attention In

ATTENTION IN is not considered a control signal.

ATTENTION IN is a wired-OR signal for all slaves to inform the master that service is requested. The master has the responsibility to service the interrupts (or class of interrupts) as required.

This signal does not contribute to determining the state of the interface. It can be asserted regardless of whether a slave is selected or not.

The ATTENTION IN signal shall not be driven to inactive.

7.2 States

The states of the interface are defined by the condition of the control signals: SELECT OUT, SLAVE IN, MASTER OUT, SYNC IN, and SYNC OUT. With the exception of Data Streaming transfers (optional), these signals are interlocked between the master and the slave.

7.2.1 Idle

When all the control signals are inactive the interface is in the IDLE state. Abnormal entries to this state shall occur whenever the master and slave(s) recognize an undefined state or state transition. The buses are released prior to entering the IDLE state except during the Request Interrupts and Master Reset sequences.

7.2.2 Maintenance

The master negates MASTER OUT, SYNC OUT and then SELECT OUT. The master then releases BUS B, negates BUS A, and then asserts SYNC OUT to enter the MAINT (Maintenance Mode) state.

This state initiates Maintenence Mode on all slaves.

7.2.3 Request

While in IDLE the master sets the Request Modifier octet on BUS A, then asserts MASTER OUT to enter the REQUEST state.

This state causes the slave(s) to respond with either the Address octet, the Transfer Settings octet, or to initiate Selective Reset.

7.2.4 Selective Reset 1 - RESETSEL1

While in REQUEST the master asserts SYNC OUT to enter the RESETSEL1 state.

This state initiates a reset of the slave identified by the Selective Reset Control octet on BUS A, and terminates Maintenance Mode.

7.2.5 Selective Reset 2 - RESETSEL2

The slave entered REQUACK (Request Acknowledge) state in response to REQUEST. While in the REQUACK state the master asserts SYNC OUT to enter the RESETSEL2 state. The slave shall release or negate all interface lines upon recognition of this state, which then causes an entry to RESETSEL1.

While in REQUEST, the slave sets the requested response on BUS B, then asserts SLAVE IN to enter the REQUACK state.

7.2.6 Deselected - DESEL

While in REQUACK the master negates MASTER OUT to enter the DESEL state. While in SLAVACK the master negates SELECT OUT to enter the DESEL state.

This state initiates the deselection of the slave by the master.

7.2.7 Select - SELECT

While in IDLE the master sets the Selection octet on BUS A then asserts SELECT OUT to enter the SELECT state. This state initiates the Selection Sequence.

While in SLAVEND the master sets the Master Status octet on BUS A, and negates MASTER OUT to enter the SELECT state.

NOTE: In the SELECT state it is necessary to know the previous transition in order to respond correctly. When entered from IDLE, it is a true Selection (and the slave responds with Select Status on BUS B). When entered from SLAVEND, SELECT is an intermediate state following an Information Transfer between the master and the selected slave.

7.2.8 Slave Acknowledge - SLAVACK

While in SELECT following IDLE the addressed slave sets its Select Status on BUS B, then asserts SLAVE IN to enter the SLAVACK state.

While in SELECT following SLAVEND the selected slave sets the Slave Status octet on BUS B, then asserts SLAVE IN to enter the SLAVACK state.

While in MASTEND the selected slave negates SYNC IN to enter the SLAVACK state. BUS B is not valid during this transition.

This state acknowledges either selection, the end of a Bus Control sequence, or the end of an Information Transfer.

NOTE: In the SLAVACK state it is necessary to know the previous transition because BUS B contains different contents depending upon the state from which SLAVACK was entered.

While in SLAVACK the master sets the Bus Control octet on BUS A then asserts SYNC OUT to enter the BUSCTL (Bus Control) state.

This state initiates control of the subsequent Information Transfer.

7.2.9 Bus Acknowledge - BUSACK

While in BUSCTL the slave sets the Bus Acknowledge octet on BUS B, then asserts SYNC IN to enter the BUSACK state.

This state is complementary to BUSCTL to acknowledge that the Bus Control octet has been accepted.

7.2.10 Master End - MASTEND

While in BUSACK the master negates SYNC OUT to enter the MASTEND state.

While in XFRST the master negates MASTER OUT to enter the MASTEND state.

This state either acknowledges that the Bus Acknowledge octet has been accepted, or it initiates termination of an Information Transfer by the master.

7.2.11 Ready To Transfer - XFRRDY

While in SLAVACK the master asserts MASTER OUT to enter XFRRDY state.

When beginning transfers In, the assertion of MASTER OUT indicates to a slave operating in Double Octet Mode that the master has released BUS A.

When beginning transfers Out, the assertion of MASTER OUT directs a slave operating in Double Octet Mode to release BUS B.

While in XFREND the master negates SYNC OUT to enter the XFRRDY state.

This state is initiated by the master to transfer each octet (or double octet) of an Information Transfer.

While in XFRRDY for transfers In the slave sets information on the bus(es), then asserts SYNC IN to enter the XFRST (Start To Transfer) state.

While in XFRRDY for Transfers Out, the slave asserts SYNC IN to enter the Start To Transfer state. The master maintains control of the Bus(es).

This state is initiated by the slave to acknowledge the start of Information Transfer. For transfers Out it indicates that the slave is ready to accept information and for transfers In it is used to validate that the Bus(es) have stable information.

7.2.12 Respond To Transfer - XFRRES

While in XFRST for transfers Out the master sets information on the Bus(es) then asserts SYNC OUT to enter the XFRRES state.

While in XFRST for transfers In, the master accepts information on the Bus(es), then asserts SYNC OUT to enter the Respond To Transfer state. The slave maintains control of the Bus(es).

This state is initiated by the master to acknowledge the acceptance of information on the Bus(es) for transfers In, or to validate that the Bus(es) have stable information on transfers Out.

7.2.13 End Of Transfer - XFREND

While in XFRRES the slave negates SYNC IN to enter the XFREND state. For transfers Out the master maintains control of the Bus(es). For transfers In the slave maintains control of the Bus(es).

This state is initiated by the slave to acknowledge the acceptance of information on transfers Out, and to complete the transferring of each octet (or double octet) of an Information Transfer.

7.2.14 Slave End - SLAVEND

While in XFRRDY the slave negates SLAVE IN to enter the SLAVEND state. When in Double Octet Mode for transfers Out the master releases control of BUS B; for transfers In during Double Octet Mode, this acknowledges the release of BUS A by the slave.

This state is initiated by the slave to terminate an Information Transfer.

7.2.15 State Summary

The determination of bus contents requires remembering the previous state transition in two states. The two states which have defined bus contents only when entered from a particular previous state are SLAVACK when entered from SELECT or MASTEND, and SELECT when entered from IDLE or SLAVEND.

The states are summarized in Table 3 and are schematically shown in Figure 5.

Table 4 defines BUS A and BUS B for every valid state transition for both input and output. It also notes the interface signals.

The table supplements the timing diagrams. Its purpose is to provide a snapshot at two different times, from the perspective of the initiator and the respondee:

Initiator - the table identifies the responsibility of the initiator for bus contents at the time it changes a signal to begin transition to a new state.

Respondee - the table identifies the bus contents at the time that the respondee recognizes the state signalled by the initiator.

Wherever DOM is referenced it identifies that there is a special requirement to release the bus other than that used in SOM and control functions. It is also implied that the bus is undefined in SOM. In SOM configurations it is not necessary for the master or selected slave to release the buses.

7.2.16 Undefined State Recovery

An undefined state or state transition induced by a slave shall cause the master to begin abnormal deselection by releasing the Bus(es) and negating all OUT signals. SELECT OUT shall be the last signal line negated, unless Slave to Slave Informations Transfers are in progress (see 7.3.9.2). When the slave is deselected it releases the Bus(es) it may be driving, then negates SYNC IN and SLAVE IN. The interface is thus returned to the IDLE state, and the master can resume operations.

An undefined state or state transition induced by a master shall cause the slave to release the Bus(es) it may be driving, then negate SYNC IN and SLAVE IN. When the master recognizes the negation of SLAVE IN outside of a valid sequence it releases the Bus(es) and negates all OUT signals. SELECT OUT shall be the last signal line negated. The interface is thus returned to the IDLE state, and the master can resume operations.

NOTE: The negation of SLAVE IN and SYNC IN is valid during defined sequences such as SLAVEND from XFRRDY. SLAVE IN and SYNC IN are not active during REQUEST, SELECT and SLAVEND.

7.2.17 Slave End Without Information Transfer

There is no requirement that an Information Transfer has to occur between Bus Control and Slave Status. The following refers to sequences when an Information Transfer is expected to occur.

If a slave senses a parity error or illegal Bus Control octet on BUS A during a Bus Control Sequence, it shall terminate the sequence normally. When the master attempts the subsequent information transfer, the slave shall negate SLAVE IN upon sensing the assertion of MASTER OUT, and enter SLAVEND from XFRRDY.

Entering SLAVEND without an Information Transfer indicates to the master that the slave did not accept the Bus Control octet. The cause of the slave rejection of the Bus Control shall be reported to the master in the Slave Status Octet during the SLAVACK state.

7.2.18 Master End Without Information Transfer

During a slave-controlled Information Transfer (optional), if the master detects a parity error or an illegal Bus Acknowledge octet on BUS B during the Bus Control sequence, it shall terminate the sequence normally. The sequence shall proceed normally from BUSACK through MASTEND to SLAVACK. While in SLAVACK the master can either assert SYNC OUT to enter BUSCTL and restart the Bus Control sequence, or negate SELECT OUT to enter DESEL and deselect the slave.

The deselection sequence, or the restarting of the Bus Control sequence indicates to the slave that the master did not accept the Bus Acknowledge octet.

7.2.19 Slave Action on Bus A Parity Errors

7.2.19.1 Selection Octet

If the slave detects a parity error on BUS A during SELECT, it shall not respond to the contents of the octet for selection purposes. If the master fails to receive a response from the selected slave within a time-out period, it shall retry the SELECT sequence.

7.2.19.2 Request Modifier Octet

If the slave detects a parity error on BUS A during REQUEST, it shall not respond to the contents of the octet. If the master fails to receive a response from at least one slave within a time-out period, it shall retry the REQUEST sequence.

7.2.19.3 Master Status Octet

If the slave detects a parity error on BUS A during the SELECT state, it shall not interpret the contents of the octet. It shall assume the Information Transfer, if any, was unsuccessful and post accordingly in the Slave Status octet.

7.2.19.4 Bus Control Octet

If the slave detects a parity error on BUS A during BUSCTL, it shall not interpret the octet and shall post the parity error in Slave Status octet.

7.3 Sequences

The Bus State diagram of Figure 5 summarizes the possible state transitions. The condition of the buses during all of the states and transitions is shown in Table 4.

7.3.1 Request Sequences

7.3.1.1 Request Interrupts Sequence (See Figure 6)

This sequence allows the master to interrogate the slaves to determine the service (or class of service) desired.

The master initiates the sequence by setting the Request Modifier on BUS A and asserting MASTER OUT. Slave(s) with interrupts meeting the required Request Modifier conditions (See 7.4.7) place their bit significant address in the Address octet on BUS B. Appropriate latching may be required at the master because interrupts from the slaves can change dynamically. Parity on BUS B shall not be checked by the master. The master negates MASTER OUT to return to IDLE state.

NOTE: The response of the slaves is not synchronous, and the master must wait a time equal to that of the slowest and/or furthest slave to respond before latching or sampling BUS B. In addition, the master must wait for a time equal to that of the slowest and/or furthest slave to detect the IDLE state, and release its bit significant address on BUS B before starting another sequence.

See Figure 7 for timing details.

7.3.1.2 Request Transfer Settings Sequence (See Figure 8)

This sequence allows the master to interrogate the specified slave as to its Information Transfer characteristics.

The master initiates the sequence by placing the Request Transfer Settings octet on BUS A (See 7.4.7.3) and asserting MASTER OUT. The addressed slave responds by setting the Transfer Settings Response octet on BUS B, and asserting SLAVE IN. The master then negates MASTER OUT to reach the Deselection State and SLAVE IN is negated to return to IDLE State.

See Figure 9 for timing details.

7.3.1.3 Request Facility Interrupts Sequence (Optional)

This sequence allows the master to interrogate the facilities of the specified slave to determine the service (or class of service) desired. The sequence is the same as that for Request Transfer Settings. The contents of the Request Modifier octet affect the slave's octet response.

The master initiates the sequence by placing the Request Facility Interrupts octet on BUS A (See 7.4.7.2) and asserting MASTER OUT. Facilities on the specified slave which have interrupts meeting the required Request Modifiers conditions set the Address octet on BUS B, and the slave asserts SLAVE IN. Appropriate latching may be required at the master because interrupts from the facilities can change dynamically. Parity shall not be checked on BUS B by the master. The master then negates MASTER OUT to reach the DESEL state, and SLAVE IN is negated to return to IDLE state.

See Figure 9 for timing details.

7.3.2 Selection Sequence (See Figure 10)

The Selection sequence occurs when the master addresses a slave (or a slave and its facilities). The selection sequence is as follows:

The master places the Selection octet containing the slave address, andoptionally the facility address on BUS A, then asserts SELECT OUT to enter the SELECT state.

If the slave can process Bus Exchanges or Information Transfers, the slave places its (the slave's) bit significant address in the Address octet on BUS B and then asserts SLAVE IN to enter the SLAVACK state.

If the slave cannot process Bus Exchanges or Information Transfers, but is otherwise functioning normally, the slave asserts only SLAVE IN to report the Busy condition by entering the SLAVACK state. This Busy condition reflects only the current condition of the slave and does not necessarily reflect the current condition of the addressed facility when the facility address is optionally placed on BUS A.

If there is a parity error on BUS A, none of the slaves are selected, and SLAVE IN is not asserted.

See Figure 11 for timing details.

7.3.3 Normal Deselection Sequence (See Figure 12)

Selection is maintained while SELECT OUT remains active. When SELECT OUT is negated, the addressee is deselected. The sequence is as follows:

See Figure 13 for timing details.

7.3.4 Master Reset Sequence (See Figure 14)

The Master Reset sequence allows the master to initiate Maintenance Mode.

The master initiates the sequence by ensuring that SELECT OUT and MASTER OUT are not active, and then asserting SYNC OUT for a minimum of 10 µs.

Recognition of the MAINT state shall be independent of normal state processing logic. The slave shall not enter Maintenance Mode until the MAINT state has been active for at least 2 µs.

See Figure 15 for timing details.

See 7.5 for details on Maintenance Mode.

7.3.5 Selective Reset Sequence (See Figure 16)

The Selective Reset sequence allows the master to reset a single slave and terminate the Maintenance Mode. The sequence is as follows:

The master initiates the sequence by placing the Selective Reset Control octet on BUS A and asserting MASTER OUT. The master shall then allow the slave time to respond by asserting SLAVE IN but will disregard SLAVE IN and the contents of BUS B if asserted by the slave. The master shall then assert SYNC OUT for a minimum of 10 µs, before negating SYNC OUT and returning to the REQUEST state.

The slave shall neither initiate its reset action nor release its interface lines until RESETSEL1 has been active for at least 2 µs. The master shall then allow the slave time to respond by asserting SLAVE IN. Whether the slave responds or not the master completes the sequence by negating MASTER OUT and monitoring the interface to ensure that the slave completes the sequence by negating SLAVE IN.

Recognition of Selective Reset shall be independent of normal state processing logic.

See Figure 17 for timing details.

7.3.6 Bus Exchange

The Bus Exchange is started by the master with a Bus Control sequence to set up an Information Transfer, and completed by the slave with an Ending Status sequence when the transfer is ended.

7.3.6.1 Bus Control Sequence (See Figure 18)

The Bus Control sequence allows the master (or optionally the slave), to establish the bus configuration for the subsequent Information Transfer.

The Bus Control sequence is initiated by the master after either Select Status (following selection) or Slave Status (following an Information Transfer) has been accepted. The master sets the Bus Control octet on BUS A and asserts SYNC OUT. The slave responds by setting the Bus Acknowledge octet on BUS B, and asserting SYNC IN. The master ends the sequence by negating SYNC OUT. Note that although the interface returns to SLAVACK when the slave responds by negating SYNC IN that there is no Slave Status octet on BUS B because it is simply an intermediate state on the way to beginning an Information Transfer.

See Figure 19 for timing details.

7.3.6.2 Ending Status Sequence (See Figure 20)

The Ending Status sequence allows the slave (or optionally the master and the slave), to present the status of the previous Information Transfer (if any).

To enter SLAVEND, the slave terminates the Information Transfer by releasing BUS B (Double Octet Mode, transfers In) and negating SLAVE IN. The master responds by releasing BUS B (Double Octet Mode, transfers Out), setting the Master Status octet on BUS A and negating MASTER OUT. The slave then sets the Slave Status octet on BUS B and re-asserts SLAVE IN to enter the SLAVACK state.

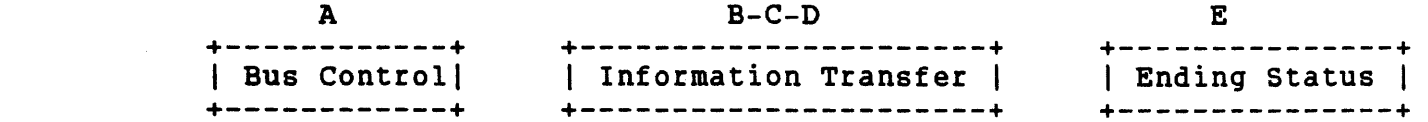
See Figures 21A through 21E for timing details.

7.3.7 Information Transfer Sequence

Information Transfer sequences differ depending on whether the ending of a transfer is initiated by the master or by the slave. The slave may terminate a sequence without the transfer of information.

Figures 22, 23, and 25 represent the sequence of states necessary for Information Transfers. In the following paragraphs (7.3.7.1 through 7.3.7.4) each line is labelled A-E, corresponding to the description below, to illustrate the separate parts of the sequence. An Information Transfer is framed by a Bus Exchange:

See Figures 24 and 26 for timing details.



7.3.7.1 Operation Command Transfer

A	Condition Bus for transfers Out	Bus Control sequence
B	Request transfer Out	
C	Transfers Out	Information Transfer sequence
D	Master initiated termination (if any)	
E	Ending Status	Ending Status sequence

7.3.7.2 Operation Response Transfer

A	Condition Bus for transfers In	Bus Control sequence
B	First transfer In	Information Transfer sequence
C	Additional transfers In	
E	Ending Status	Ending Status sequence

7.3.7.3 Data Transfer Out

A	Condition Bus for transfers	Out Bus Control sequence
B	Request transfer Out	
C	Transfers Out	Information Transfer sequence
D	Master initiated termination (if any)	
E	Ending Status	Ending Status sequence

7.3.7.4 Data Transfer In

A	Condition Bus for transfers In	Bus Control sequence
B	First transfer In	
C	Additional transfers In	Information Transfer sequence
D	Master initiated termination (if any)	
E	Ending Status	Ending Status sequence

7.3.7.5 Termination Of Information Transfer

The slave terminates an Information Transfer sequence with the Ending Status Sequence. The master initiates the end of the Information Transfer, and the slave terminates with the Ending Status sequence.

7.3.8 Data Streaming (Optional)

Data streaming is the technique that allows high transfer rates over long cable lengths. This is accomplished by not interlocking SYNC IN and SYNC OUT, which eliminates a round trip cable delay. This allows cable delay to be eliminated in determining transfer rate. Data streaming shall only be used during Information Transfers. All control and status sequences shall be interlocked.

Note: Normal state sequences do not apply during Data Streaming, since fully interlocked operation is not required.

The Request Transfer Settings sequence is used to ascertain what modes of transfer are possible. Slave attributes may be: interlocked only, Data Streaming only, or both. In the latter case, the master will select the mode to be used during slave selection.

7.3.8.1 Transfer Technique (See Figure 22)

The transfer begins with the slave asserting SYNC IN and then negating it to generate a pulse. The period between succesive pulses is defined by the transfer rate. Upon recognizing the SYNC IN pulse, the master generates a complementary SYNC OUT pulse. The master must "answer" every SYNC IN pulse with a complementary SYNC OUT pulse.

The period between successive SYNC IN pulses is determined by the transfer rate. Upon recognizing the SYNC IN pulse, the master generates a SYNC OUT pulse in response. The SYNC OUT pulse may be generated by the master in two ways:

1. Mirror the SYNC IN pulse by detection of leading and trailing edges.

2. Use a clock value to create a pulse which is at least 40% of CCD.

NOTE: The CCD (Cable Configuration Dependent) value that a slave can recognize at the interface is at least equal to, but may be faster than, the rate at which it can transfer data.

The transmitter must insure the proper set-up and hold times with respect to the active edge of its sync pulse.

If the hold time is greater than the one-way cable delay plus set up times the effect is to cause the transfers to appear interlocked.

7.3.8.2 Throttling Transfers (Optional)

A slave transferring from a buffer may be able to permit the master to stop and start the transfer stream.

If at any point in the transfer the slave has transmitted X unanswered SYNC IN pulses where X = 8 (unless X is specified by the master during housekeeping), it shall wait a minimum of 25 ms for a complementary SYNC OUT pulse. If a SYNC OUT pulse is received, operations shall continue normally. If a SYNC OUT pulse is not received, the slave shall end the transfer sequence.

The effect of this is that after the first X SYNC IN pulses are transmitted by the slave at its chosen transfer rate, all successive SYNC IN pulses shall only be generated upon receipt of a SYNC OUT pulse, thus allowing the master to dictate the period between SYNC IN pulses and throttling the speed at which the slave can transfer.

It is the responsibility of the master to ensure that the SYNC OUT pulses provided to the slave exceed 40% of the CCD (Cable Configuration Dependent) value.

7.3.8.3 Slave Termination of Data Streaming (See Figure 22)

To terminate a Data Streaming transfer, the slave first stops transmitting SYNC IN pulses. It then waits until it has received an equal number of SYNC OUT pulses from the master, or a minimum of 25 milliseconds has expired without pulses, after which it terminates the transfer by negating SLAVE IN and following the normal interlocked Ending Status Sequence.

7.3.8.4 Master Initiated Termination of Data Streaming (See Figure 22)

To terminate a Data Streaming transfer, the master substitutes a SYNC OUT pulse with an inactive pulse on the MASTER OUT line having the same pulse width and period requirements of the SYNC OUT pulse. The master then continues to "answer" every SYNC IN pulse with complementary SYNC OUT pulses.

For transfers Out, the master shall not transmit information with the MASTER OUT pulse or subsequent SYNC OUT pulses.

For transfers In, the master shall accept information with up to 8 SYNC IN pulses, following generation of the MASTER OUT pulse. This allows all information transmitted by the slave before its recognition of the MASTER OUT pulse, to be received by the master, thus maintaining the capability for data integrity.

NOTE: If master initiated termination of Data Streaming is used when the master does not require a precise match between the number of octets transferred by the master and the slave, the master is not required to accept information after generation of the MASTER OUT pulse.

When the slave senses the MASTER OUT pulse, it stops transmitting SYNC IN pulses and waits until it has received an equal number of SYNC OUT pulses, including the MASTER OUT pulse. For transfers Out, the slave shall not latch any information on the MASTER OUT pulse and subsequent SYNC OUT pulses.

After the slave detects the number of SYNC IN pulses equalling the number of SYNC OUT pulses, including the MASTER OUT pulse, or a minimum of 25 milliseconds has expired without pulses, it negates SLAVE IN and the normal interlocked Ending Status Sequence is followed.

7.3.9 Slave-to-Slave Information Transfers (Optional)

The master can permit transfers to occur between any two slaves on the interface by defining a dominant slave that shall control MASTER OUT and SYNC OUT. The master remains master of the interface because it retains control of SELECT OUT.

7.3.9.1 Information Transfers

It is possible to set up transfers between slaves so that data movement can be accomplished external to the master. This requires the designation of a dominant slave and a subservient slave. The following is a description of how the two are required to operate:

The master first selects the slave that shall be designated the dominant Slave.

Using Operation Commands/Operation Responses the master supplies the identity of the subservient slave to the dominant slave. The dominant slave shall monitor the interface and be prepared to assume control after the master selects the subservient slave. The subservient slave shall have its Select Status octet on BUS B during the SLAVACK state.

If the subservient slave is not busy, the master shall release BUS A and the dominant slave shall assume control of MASTER OUT and SYNC OUT (thus assuming the role of the master on the interface). The master thus permits the dominant slave to initiate Information Transfers with the subservient slave (which is operating normally), but retains through SELECT OUT the ability to abort the operation.

Each time the intermediate SELECT state is entered the dominant slave sets Master Status octet on BUS A. The master monitors this octet to detect the Slave-Slave Operation Completed bit.

The dominant slave relinquishes control to the master by posting the Slave-Slave Operation Completed bit in the Master Status octet. The subservient slave shall proceed normally to enter SLAVACK.

The master terminates the Slave-to-Slave Information Transfer by deselecting the subservient slave. The master shall reselect the dominant slave to obtain the Operation Response.

7.3.9.2 Error Recovery Considerations

If the subservient slave is busy during initial selection the master can continue to retry until successful, or re-select the dominant slave to terminate the process.

If the master must regain control of the bus during the process it does so by de-selecting the subservient slave. The dominant slave shall detect the de-selection as an abnormal termination, and prepare Operation Response for presentation to the master when it is next selected. The subservient Slave shall proceed through normal deselection, if it was in the SLAVACK state when SELECT OUT was negated.

NOTE: The implementation described in 7.3.9 requires the use of features in the interface which are defined as Optional. In addition, a master which intends to support Slave-Slave Information Transfers must be able to monitor the MASTER OUT and SYNC OUT lines which are under control of the dominant slave.

7.4 Bus Octet Definitions

Table 4 defines the usage of bus octets for each state and transition. 7.4.1 specifies the BUS A octet(s), 7.4.2 the associated BUS B response octet(s).

NOTE: The optional functions defined within each each octet are identified by the bits being enclosed in parentheses.

If the octet itself is optional, required bits within it do not have parentheses, only optional bits in an optional octet have parentheses.

7.4.1 BUS A Selection Octet Bit Definitions
Presented during the SELECT state.

During the selection sequence, BUS A contains the addressing information for the selection.

7.4.1.1 BUS A Selection Octet

7	6 | 5 | 4	3	2	1	0
0	SLAVE ADDRESS	CHANGE TRANS-FER MODE	CHANGE OCTET MODE	PRIOR-ITY HOLD	PRIOR-ITY SELECT

When Bit 7=0 the addressed slave shall respond on BUS B to the Selection octet on BUS A (See 7.4.2).

- Slave Address

  Bit 4 is the least significant bit (LSB) of the slave address.

- Change Transfer Mode

  When Bit 3=1 the addressed slave shall change its current mode of transfer (Interlocked or Data Streaming). See 7.4.8.3

- Change Octet Mode

  When Bit 2=1 the addressed slave shall change its current mode of octet operation (SOM or DOM). See 7.4.8.3

- Priority Hold

  When Bit 1=1 and a selection is established, the slave shall maintain an explicit allegiance after deselection to this port until:

  - a subsequent selection is established without the Priority Hold bit set in the Selection octet or
  - a selection by another port is established with both the Priority Hold and Priority Select bits set in the Selection octet or
  - an appropriate Reset is executed by the slave.

- Priority Select

  When Bit 0=1 the specified slave shall release the current port to which it is dedicated provided that an alternate port does not have a Priority Hold in effect, and shall respond to the requesting master.

  If two or more channels of a given slave are in the SELECT state at the same time with the Priority Select bit set in the Selection octet and the slave does not have a Priority Hold in effect for any port not attempting a selection, the slave will connect to one and only one of the channels. The other port(s) shall receive a Busy indication.

  A successful selection with the Priority Select bit set in the Selection octet shall cause any other channel with a selection established and not in the SELECT state to terminate its selection. The termination may be orderly or abrupt depending on the slave's implementation.

- Priority Hold and Priority Select

  When both Bit 1=1 and Bit 0=1 the specified slave shall release the current channel to which it is dedicated regardless of its previous condition providing another channel had not previously established selection with both of the bits set.

  The specified slave shall maintain allegiance to the selected post after deselection until:

  - a subsequent selection is established without the Priority Hold and Priority Select bits set or

  - an appropriate reset is executed by the slave.

  The Truth table provides a definition of the interaction of two channels given that Channel A action occurs prior to Channel B action. For the conditions under Channel A Not Selected, the slave was last selected by Channel A with the given value of PH (Priority Hold) and PS (Priority Select). For the conditions under Channel A Selected, the slave is currently selected on Channel A when Channel B attempts selection.

		Channel B			
	PH PS	PH PS	PH PS	PH PS	PH PS
		0 0	0 1	1 0	1 1
Channel A Not Selected	0 0	B	B	B	B
	0 1	B	B	B	B
	1 0	A	A	A	B
	1 1	A	A	A	A
Channel A Selected	0 0	A	B	A	B
	0 1	A	B	A	B
	1 0	A	A	A	B
	1 1	A	A	A	A

If any of the optional bits (bits 0-3) set are not supported by the slave, the addressed slave shall not acknowledge selection; i.e., the slave shall not assert SLAVE IN.

7.4.1.2 BUS A Facility Selection Octet (Optional)

The master has the ability to select any of 8 slaves and indirectly address up to 16 facilities. The slave is responsible for facility selection on behalf of the master.

7	6	5	4	3	2	1	0
1	SLAVE ADDRESS			FACILITY ADDRESS			

When Bit 7=1 the addressed slave shall respond to the selection request for the facility with the Select Status octet (See 7.4.2).

- Slave Address

  Bit 4 is the least significant bit (LSB) of the slave address.

- Facility Address

  Bit 0 is the least significant bit of the facility address.

  If this option is not supported the slave identified in Bits 4-6 shall not acknowledge selection; i.e., the slave shall not assert SLAVE IN.

  If it is supported, and the facility address is not valid then the Slave Status octet shall be used to indicate an invalid selection address.

7.4.2 Bus B Select Status Octet
Presented during the SLAVACK state.

The slave responds to selection by driving its (the slave's) bit significant address and releasing all other bus bits to provide Select Status, which is defined as follows:

7	6	5	4	3	2	1	0
SLAVE 7	SLAVE 6	SLAVE 5	SLAVE 4	SLAVE 3	SLAVE 2	SLAVE 1	SLAVE 0

NOTE: The parity line shall be released by the slave and parity shall not be checked by the master.

If the addressed slave is not present on the interface, or does not recognize its address, SLAVE IN will not be asserted and no address bits shall be asserted.

The master can detect invalid selection conditions by analysis of Select Status e.g. incorrect selection will have the wrong address bit posted, multiple selection will have more than one address bit posted. To detect multiple selection, the master must wait until all slaves have had enough time to respond.

7.4.3 Bus A Bus Control Octet
Presented during the BUSCTL state.

The Bus Control octet describes the subsequent Information Transfer and bus configuration. If the master sets up a Bus Control that is not recognizable at the slave, the slave shall end the subsequent Information Transfer sequence without an Information Transfer (See Figure 24).

The Bus Control octet is defined as follows:

7	6	5	4	3	2	1	0
0 * 1	0 ** 1	DEFINED BY LOGICAL INTERFACE					

* 0 = OPERATION COMMAND/OPERATION RESPONSE
1 = DATA

** 0 = INFORMATION OUT
1 = INFORMATION IN

The use of Bits 0-5 is is established by the master and the slave at the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

7.4.4 Bus B Bus Acknowledge Octet

Presented during the BUSACK state.

The contents of this octet are optional, and if none are supported it is the responsibility of the slave to ensure that the bus contents are stable with correct parity during the BUSACK state, and that zero is posted.

In an intelligent subsystem there may be a need for the master to receive responses from the slave immediately after Bus Control.

7	6	5	4	3	2	1	0
0 * 1	0 ** 1	DEFINED BY LOGICAL INTERFACE					

* 0 = OPERATION COMMAND/OPERATION RESPONSE
1 = DATA

** 0 = INFORMATION OUT
1 = INFORMATION IN

The use of Bits 0-5 is is established by the master and the slave at the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

7.4.5 Bus A Master Status Octet
Presented during the SELECT state.

The Master Status octet is used by the master to inform the slave whether or not the previous Information Transfer was successful, and if a bus parity error had been detected.

7	6	5	4	3	2	1	0
SUCCESSFUL INFORMATION TRANSFER	BUS PARITY ERROR	DEFINED BY LOGICAL INTERFACE					

- Successful Information Transfer

  When Bit 7=1 the previous Information Transfer as viewed by the master completed successfully.

- Bus Parity Error

  When Bit 6=1 the master detected a bus parity error on the Bus Acknowledge octet or the Information Transfer In.

  The use of Bits 0-5 is is established by the master and the slave at the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

7.4.6 Bus B Slave Status Octet
Presented during the SLAVACK state.

The Slave Status octet describes the slave-determined ending status of the previous Information Transfer, if any.

7	6	5	4	3	2	1	0
SUCCESSFUL INFORMATION TRANSFER	BUS PARITY ERROR	DEFINED BY LOGICAL INTERFACE					

- Successful Information Transfer

  When Bit 7=1 the previous Information Transfer completed successfully.

- Bus Parity Error

  When Bit 6=1 the slave detected a parity error in the Bus Control octet, the Information Transfer Out, or the Master Status octet.

  The use of Bits 0-5 is is established by the master and the slave at the Logical Interface or may be Vendor Unique. The use of these bits shall not affect the Physical Interface hardware.

7.4.7 Bus A Request Modifier Octet
Presented during the REQUEST state.

The Request Modifier octet is presented during the REQUEST state and is used by the master in various forms to request interrupt class(es), status, or transfer settings, and is also used to initiate Selective Reset.

7.4.7.1 Request Interrupts Octet

7	6	5	4	3	2	1	0
0	REPORT BUSY STATUS	REPORT READY STATUS	POWER FAIL ALERT	POWER ON STATUS REQUEST	CLASS 3 INTER-RUPT	CLASS 2 INTER-RUPT	CLASS 1 INTER-RUPT

When Bit 7=0, all slaves on the interface shall respond on BUS B (see 7.4.8.1) based on the settings of bits 0-6.

- Report Busy

  When Bit 6=1 all slaves that are Busy shall place their bit significant address on BUS B.

- Report Ready Status

  When Bit 5=1 all slaves that are Ready for use shall place their bit significant address on BUS B.

- Power Fail Alert

  When Bit 4=1 the master is informing the slaves that it has detected that power is failing. The slaves shall acknowledge by placing their address on BUS B after they have taken the appropriate action to permit a graceful termination of activity.

- Power On Status Request

  When Bit 3=1 the master is requesting that all slaves with power on (but not necessarily ready) place their bit significant address on BUS B.

- Interrupt Class

  Slaves with interrupts pending shall respond by placing their bit significant address on BUS B. The definition of interrupts within a class may vary between different implementations of the interface, however, they shall always be ranked with Class 3 considered most important, and Class 1 as least important.

  It is the responsibility of the vendor to define the type of interrupts within each class.

  When Bit 2=1 slaves with Class 3 Interrupts pending shall respond. Class 3 Interrupts would typically be asynchronous and critical, and deserving of immediate attention from the master.

  When Bit 1=1 slaves with Class 2 Interrupts pending shall respond. Class 2 Interrupts would typically be associated with a data transfer.

  When Bit 0=1 slaves with Class 1 Interrupts pending shall respond. Class 1 Interrupts would typically be status associated with the completion of operations, but may also be asynchronous and non-critical.

  NOTE: If more than one status or interrupt request is set by the master, the slaves shall respond to the logical OR of the conditions.

7.4.7.2 Request Facility Interrupts Octet (Optional)

If all the Interrupt Class bits are zero, this octet is interpreted as either Request Transfer Settings (see7.4.7.3) or Request Slave Interrupts (see7.4.7.4).

7	6 | 5 | 4	3	2	1	0
1	SLAVE ADDRESS	FACIL-ITY RANGE	CLASS 3 INTER-RUPT	CLASS 2 INTER-RUPT	CLASS 1 INTER-RUPT

When Bit 7=1, the slave specified by the address in Bits 6-4 shall decode the Request Facility Interrupts octet.

- Slave Address

  Bit 4 is the least significant bit (LSB) of the slave address.

- Facility Range

  Bit 3 is used to identify the range of addresses to respond on BUS B.

  Bit 3 = 0 - addresses 0-7 respond
  Bit 3 = 1 - addresses 8-F respond

- Interrupt Class

  See 7.4.7.1

  NOTE: If more than one interrupt request is set by the master, the facilities shall respond to the logical OR of the conditions.

7.4.7.3 Request Transfer Settings Octet

7	6	5	4	3	2	1	0
SLAVE ADDRESS				REQUEST TRANSFER SETTINGS			
				0	0	0	0

- Slave Address

  Bit 4 is the least significant bit (LSB) of the slave address.

- Request Transfer Settings

  When Bits 0-3 are set to zero, the selected slave shall respond with the Transfer Settings octet (See 7.4.8.3).

7.4.7.4 Request Slave Interrupts Octet (Optional)

This request allows the master to obtain status and all the interrupts from the slave.

7	6	5	4	3	2	1	0
SLAVE ADDRESS				REQUEST SLAVE INTERRUPTS			
				1	0	0	0

- Slave Address

  Bit 4 is the least significant bit (LSB) of the slave address.

- Request Slave Interrupts

  When Bit 3 is set to 1 and Bits 2-0 are set to zero, the selected slave shall respond with the Slave Interrupts octet (See 7.4.8.4).

7.4.7.5 Selective Reset Control Octet
(Interpreted during the RESETSEL1 and RESETSEL2 states)

The Selective Reset Control octet is used to perform Selective Reset (see 3.4.5) of the addressed slave. This octet is first presented during the REQUEST state, and acquires its specific meaning when in RESETSEL1 or RESETSEL2.

7	6	5	4	3	2	1	0
SLAVE ADDRESS				RESET CONTROL (DEFINED BY LOGICAL INTERFACE)			

- Slave Address

  Bit 4 is the least significant bit (LSB) of the slave address.

- Reset Control

  Bits 0-3 are used to define the type of Selective Reset to be executed by the slave. The use of Bits 0-3 is is established by the master and the slave at the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

  NOTE: There is no BUS B response to Selective Reset. If a slave interprets the octet and responds during a Selective Reset sequence the response is ignored by the master. The slave shall interpret this octet as a Selective Reset octet during the RESETSEL1 and RESETSEL2 states.

7.4.8 Bus B Responds to Request Modifier Octet
(Presented during the REQUEST or REQUACK states)

7.4.8.1 Address Octet Response to Request Interrupts
(Presented during the REQUEST state)

If there is an interrupt or status that satisfies the requirements of the Request Interrupts octet on BUS A the slave responds by driving only its address bit (and shall ensure that all other bits are released) to provide the Address octet, which is defined as follows:

7	6	5	4	3	2	1	0
SLAVE 7	SLAVE 6	SLAVE 5	SLAVE 4	SLAVE 3	SLAVE 2	SLAVE 1	SLAVE 0

NOTE: The parity line shall be released by the slave and parity shall not be checked by the master.

There is no control signal response made by the slave to the "polling" of interrupts. This octet is presented by the slave on BUS B during the REQUEST state, and the master is responsible to ensure that sufficient time has elapsed for all slaves to respond.

7.4.8.2 Address Octet Response to Request Facility Interrupts
(Presented during the REQUACK state)

The address bits are set on BUS B by the slave if there are any interrupts that satisfy the requirements in the facility range specified. Table 5 summarizes the bit significant address mapping.

NOTE: Parity may or may not be valid. Parity shall not be checked by the master.

7.4.8.3 Transfer Settings Octet
(Presented during the REQUACK state)

7	6	5 | 4	3 | 2	1 | 0
0	MAINT-ENANCE MODE	CURRENT SETTING	TRANSFER MODE CAPABILITY	OCTET MODE

- Maintenance Mode

  Used by the slave to indicate its Maintenance Mode setting to the master:

  Bit 6: 0 = Maintenance Mode 1 capability only
  1 = Maintenance Modes 1 and 2 capability

- Current Setting

  Used by the slave to identify to the master which modes are currently set:

  Bit 5: 0 = Single Octet Mode
  1 = Double Octet Mode

  Bit 4: 0 = Interlocked Transfer
  1 = Data Streaming Transfer

- Transfer Mode Capability

  Bit 3=1 the slave can transfer in Data Streaming Mode.
  Bit 2=1 the slave can transfer in Interlocked Mode.

  When both bits are set the slave is capable of operating in either mode.

- Octet Capability

  Bit 1=1 the slave is capable of operating in Double Octet Mode.
  Bit 0=1 the slave is capable of operating in Single Octet Mode.

  When both bits are set the slave is capable of operating in either mode.

If a slave is capable of supporting more than one type of octet mode, or more than one type of transfer mode, it shall be able to change the current mode under control of the master (See 7.4.1.1).

7.4.8.4 Slave Interrupts Octet (Optional)
(Presented during the REQUACK state)

7	6	5	4	3	2	1	0
DEFINED BY LOGICAL INTER-FACE	BUSY STATUS	READY STATUS	PRIOR-ITY HOLD STATUS	PRIOR-ITY SELECT STATUS	CLASS 3 INTER-RUPT	CLASS 2 INTER-RUPT	CLASS 1 INTER-RUPT

- Busy Status

  When Bit 6=1 the slave is Busy.

- Ready Status

  When Bit 5=1 the slave is Ready for use.

- Priority Hold Status

  When Bit 4=1 the slave has a Priority Hold established at one of its channels.

- Priority Select Status

  When Bit 3=1 the slave is Priority Selected at another channel.

- Interrupt Class

  When Bit 2=1 the slave has a Class 3 Interrupt pending.

  When Bit 1=1 the slave has a Class 2 Interrupt pending.

  When Bit 0=1 the slave has a Class 1 Interrupt pending.

The use of Bit 7 is established by the master and the slave at the Logical Interface. The use of this bit shall not affect the Physical Interface hardware.

7.5 Maintenance Mode

Maintenance Mode provides a communication path for error recovery and fault isolation when a failure exists in the interface or within an attached slave.

Utilizing the Master Reset sequence, the master forces the interface into a mode that allows various levels of communication and control while normal functional usage of the interface is blocked.

Normal interface function is blocked as a result of failure modes such as:

- An interface line being open
- An interface line being stuck-on; e.g., a slave's driver continually asserting SYNC IN)
- An attached slave malfunctioning in a manner that results in improper and irrational interface usage; e.g., microprocessor in a slave not recognizing or responding correctly to master sequences).

Such failure modes prevent the master/slave communication necessary to collect fault isolation information and/or to implement real-time error recovery procedures.

The Maintenance Mode permits using the interface for some basic functions during most failure modes that have been predicted (except for those that block the master from asserting SYNC OUT and negating SELECT OUT and MASTER OUT in order to enter the MAINT state).

To enter Maintenance Mode it is necessary for the master to initiate the Master Reset sequence (see 7.3.4). When in MAINT state the master can select Maintenance Mode 1 (MM1). Maintenance Mode offers capabilities to the master when normal methods of interface communications are not operational (failure) or may be inappropriate (diagnostics). The maintenance logic shall have the ability to take over the interface drivers in the slave and optionally to communicate with the master.

MM1 is a simple technique to provide a degree of isolation that improves the serviceability and availability of the interface.

Figure 25 illustrates a slave implementation including the maintenance logic. Normal operations are directed from the drivers and receivers into the functional circuits. When communication with the maintenance logic is required, the signals are disconnected from the functional circuits and diverted to the maintenance circuits.

Maintenance mode requires that the slave provide logic which is independent (as far as is practical) of the logic associated with normal functions.

MM control signals are developed by voting on triplicated lines. This technique provides fault tolerance. Voting shall be done on the static condition of the triplicated lines; i.e., the condition of the lines is not edge sensitive).

7.5.1 Maintenance Mode 1 - MM1

7.5.1.1 MM1 capabilities

MM1 enables releasing the slave's drivers from the interface. This capability, in conjunction with the Selective Reset state, can be used to isolate a slave which is holding a driver active on the interface. This may allow the master to continue using the remaining operational slaves on the interface when otherwise this would be impossible.

MM1 provides a reset capability.

The master may invoke MM1 at any time by placing the control Out lines into the MAINT state. The MM logic associated with each slave shall release the drivers from the interface whenever it is recognized that master has placed the Control Out lines into the MAINT state.

7.5.1.2 MM1 Scenario

Table 6 outlines the MM1 scenario. As can be seen the MM1 scenario is separated into three phases. The sections following the table describe each of these phases more fully. Table 7 provides the signal line assignments during the first two phases of the MM1 scenario.

FIRST PHASE (MM1) - Assert Master Reset sequence

The MM1 circuits shall release all the drivers from the interface whenever the master places the control out lines into the MAINT state.

SECOND PHASE (MM1) - Enter IDLE State, Begin Reset

Whether or not a reset and permanent releasing of the interface drivers occurs depends upon the state of three BUS A lines, referred hereafter as the DATA OUT lines, at the time SYNC OUT is negated. If at least two of these three lines are active at the trailing edge of SYNC OUT the slave shall be reset and the drivers shall remain released until a Selective Reset sequence is issued. The reset will persist as long as DATA OUT remains active. If at least two of the DATA OUT lines are not active at the trailing edge of SYNC OUT the drivers will be restored and no reset shall be issued.

THIRD PHASE (MM1) - Selective Reset of Slaves

The master may selectively restore a slave's interface drivers by use of the Selective Reset sequence. The response to the Selective Reset sequence is delayed until the MM1 circuits release the control In line drivers during RESETSEL1.

7.5.2 Other Maintenance Considerations

The MM circuits may release the slave's drivers from the interface outside of MAINT if a fault is detected by the slave which may prevent normal communications. Once the master recognizes that a slave has isolated itself from the interface it can attempt to restore communications via the Selective Reset sequence.

If the MM circuits release the slave's drivers from the interface, undefined states may result. When the Selective Reset sequence is initiated to restore the slave, the normal response to the Selective Reset state shall be delayed until the drivers are restored.

Multi-ported slaves are required to react to the Maintenance Mode considerations on the channel over which the MAINT state was recognized. The slave shall not induce error conditions on the other channels which are attached to the slave. However, during Maintenance Mode, the slave may be dedicated to the channel initiating the reset, and be Busy to all others.

7.6 Timing

7.6.1 Terms

The master must provide for cable deskewing for all signals originating from the master. The slave must provide for cable deskewing for all signals originating in the slave. The following terms are used in place of actual numbers so that timing may be determined separately for different slaves and their supported cable types.

SDE (Slave Dependent Exchange) - This term, the value of which is supplied by the slave manufacturer, specifies both the maximum slave BUS B setup time and the maximum slave response delay during a Bus Exchange when the slave is functioning properly.

SYD (System Dependent) - This term, the value of which is supplied by the slave manufacturer, specifies the time the master must wait during a Bus Exchange until it can conclude that the slave is not functioning properly. It is intended that this value be used by the master as a time-out for interlocked slave responses during a Bus Exchange.

IRT (Interrupt Response Time) - This term, the value of which is supplied by the slave manufacturer, specifies the maximum slave response time to a Request Interrupts Sequence.

SDR (Slave Dependent-Reset) - This term, the value of which is supplied by the slave manufacturer, specifies the maximum time the master must wait for the slave to recover from a reset sequence (which may include a reset of the slave microprocessor if specified by Bits 0-3 of the Selective Reset octet).

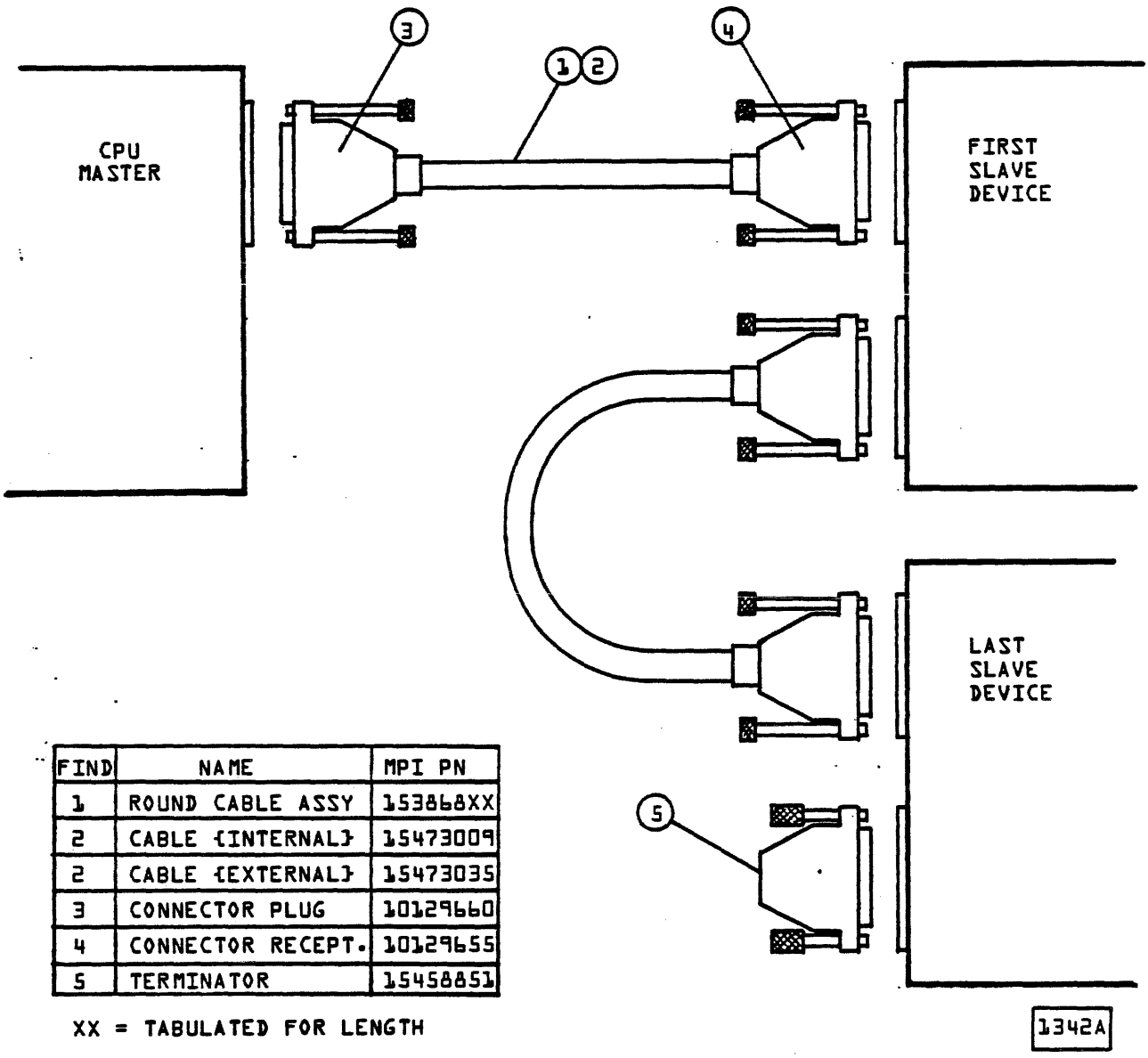
CCD (Cable Configuration Dependent) - This term, the value of which is limited by the electrical class, is defined in 6.5. It is used to establish minimum values such as set up times and pulse widths as shown in the timing diagrams. The actual CCD value is defined by an individual product. The actual value is determined by the product's implementation, and defines the minimum timings (maximum rates) that can be utilized.

CMX (Cable Delay Maximum) - The cable propagation delay based on the maximum length of cable in the configuration in which this interface is used.

7.6.2 Data Streaming Sync Out Pulse Width

When the slave is executing transfers which cannot be throttled, as for direct data transmittal between master and a disc drive, the values 1.1(tH), tH' Max and tY' Min and Max are applicable.

The value of tH' shall always be met by the master.

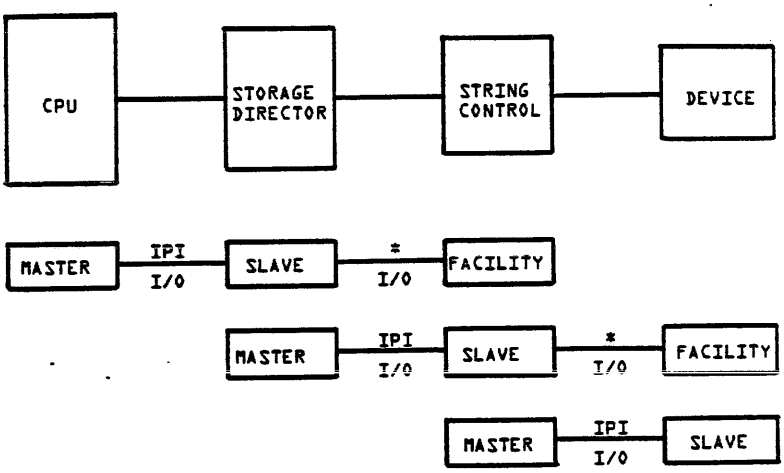


FIND	NAME	MPI PN
1	ROUND CABLE ASSY	153868XX
2	CABLE (INTERNAL)	15473009
2	CABLE (EXTERNAL)	15473035
3	CONNECTOR PLUG	10129660
4	CONNECTOR RECEPT.	10129655
5	TERMINATOR	15458851

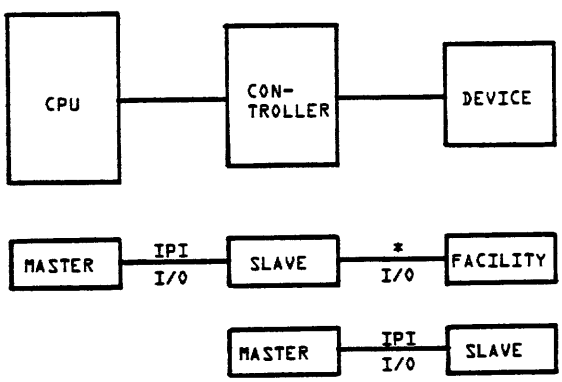
XX = TABULATED FOR LENGTH

FIGURE 1. SCHEMATIC OF IPI CABLING

(A) MAINFRAME CONFIGURATION EXAMPLE



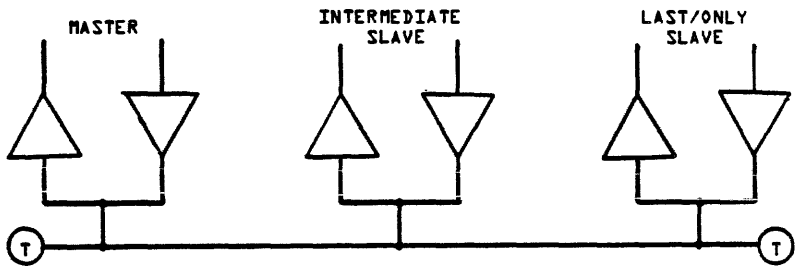
(B) MINICOMPUTER CONFIGURATION EXAMPLE



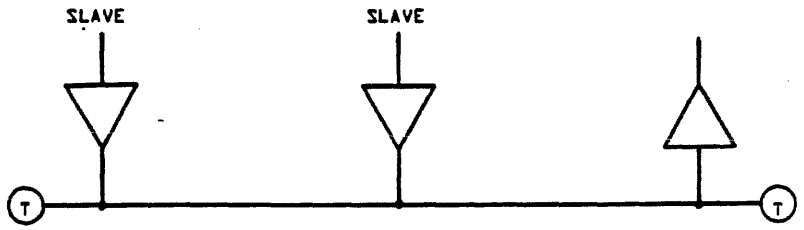
* IPI I/O IS ALWAYS BETWEEN THE MASTER AND THE SLAVE. THE I/O BETWEEN THE SLAVE AND THE FACILITY MAY OR MAY NOT BE IPI, BUT IF IT IS, THE MASTER/SLAVE RELATIONSHIP IS VALID BETWEEN THEM.

FIGURE 2. MULTI-TIER STRUCTURE

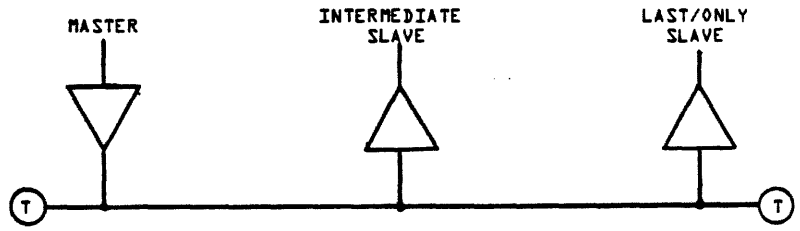
(A) CONFIGURATION FOR BIDIRECTIONAL BUS SIGNALS



(B) CONFIGURATION FOR UNIDIRECTIONAL SINGLE ENDED LINES FROM SLAVE



(C) CONFIGURATION FOR UNIDIRECTIONAL SINGLE ENDED LINES FROM MASTER



NOTE: CABLE TERMINATORS MUST BE AT EXTREME ENDS OF CABLE

FIGURE 3. CABELING ALTERNATIVES

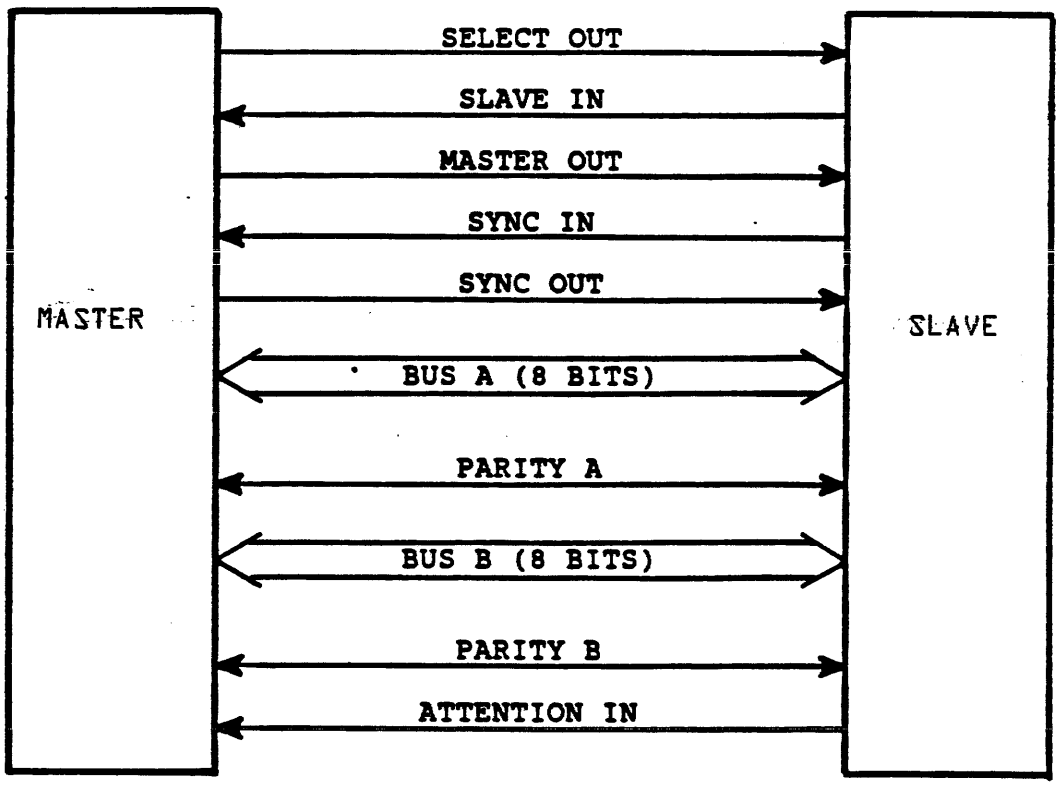
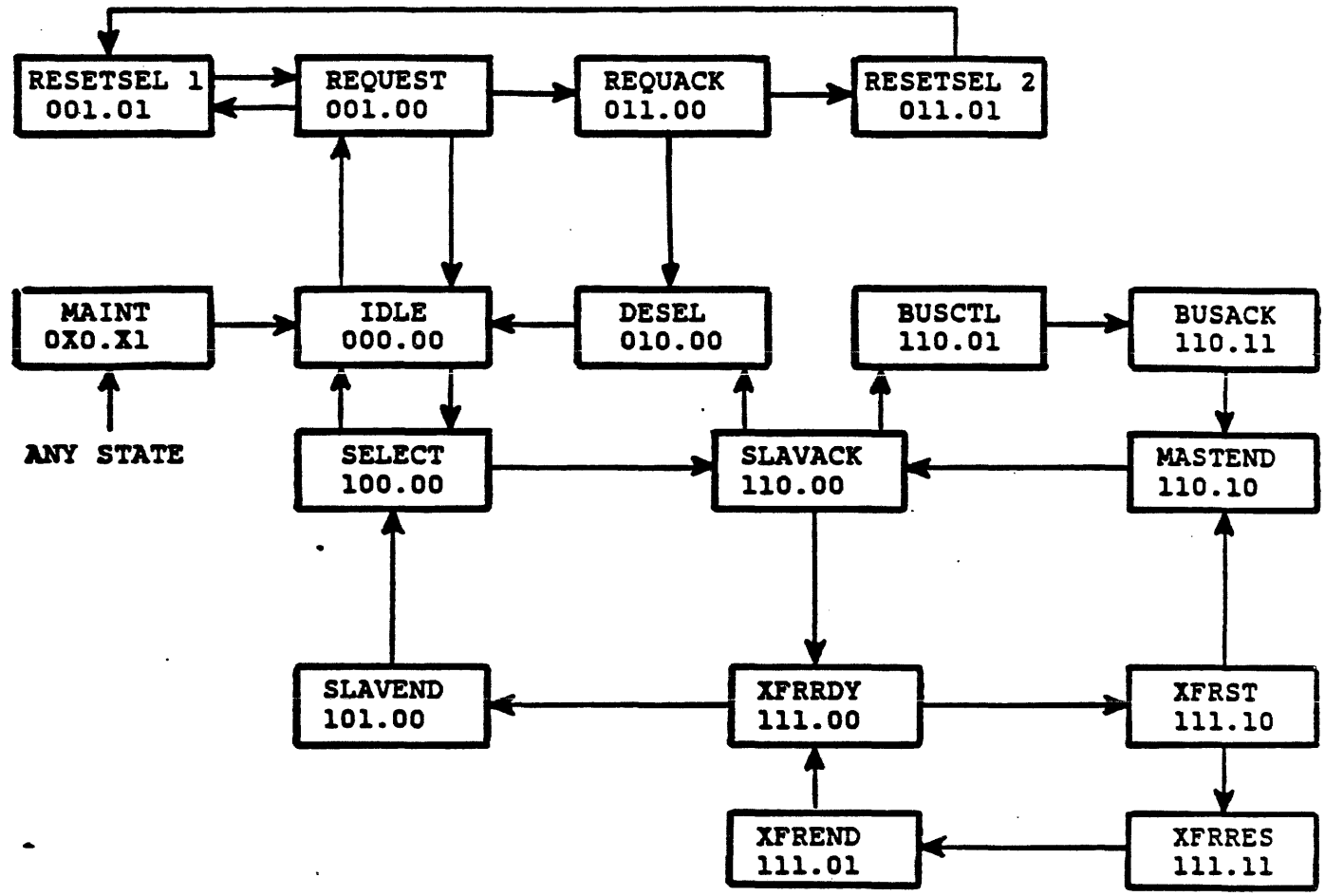


FIGURE 4. IPI INTERFACE SIGNALS

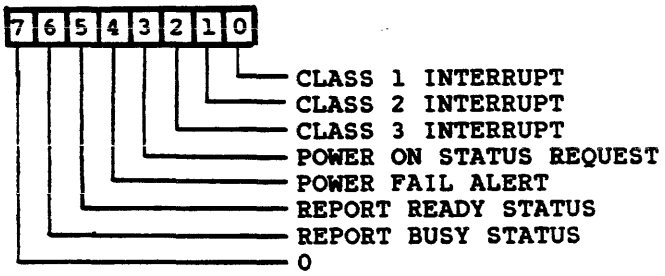


DEFINITION: XXX.XX

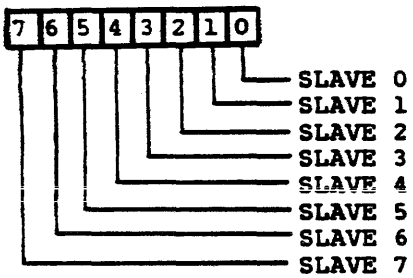
- XXX.XX
  - SYNC OUT
  - SYNC IN
  - MASTER OUT
  - SLAVE IN
  - SELECT OUT

FIGURE 5. BUS STATE DIAGRAM

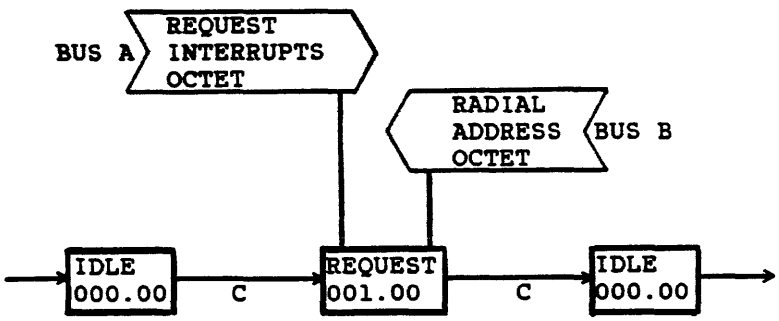
REQUEST INTERRUPTS OCTET (MASTER)



SELECT STATUS OCTET (SLAVE)



REQUEST INTERRUPTS SEQUENCE



DEFINITION: XXX.XX

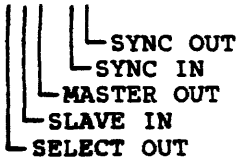
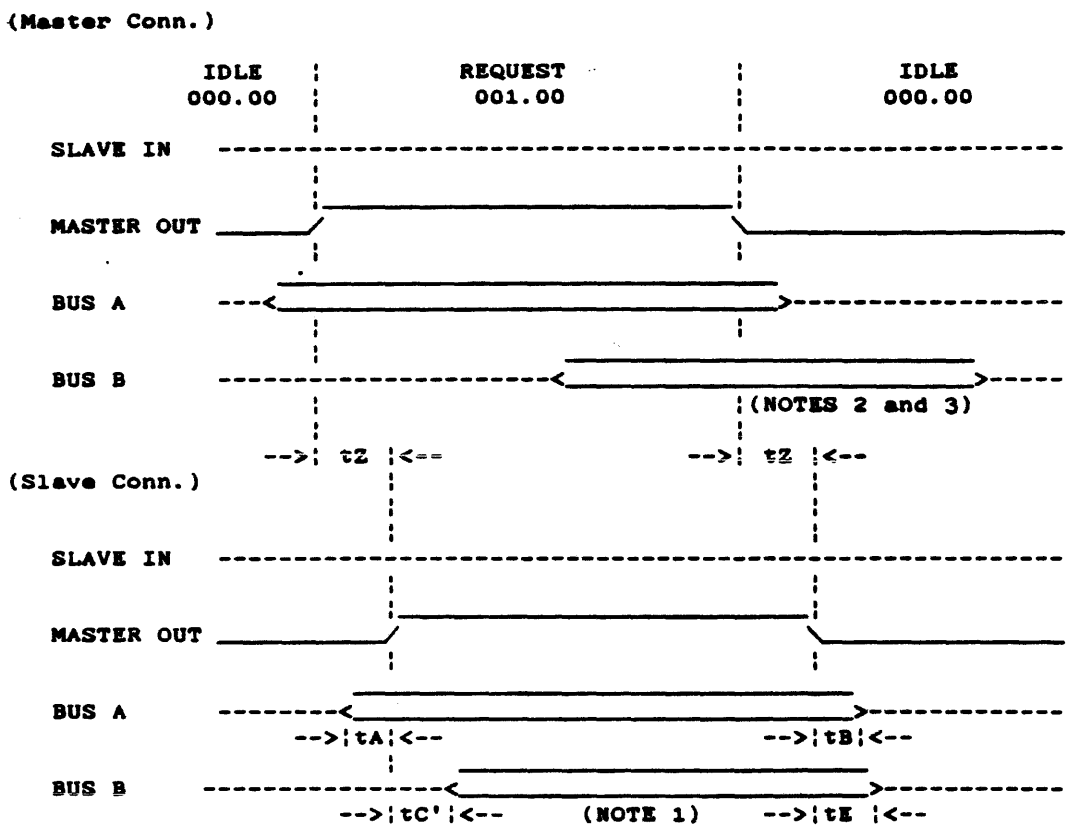


FIGURE 6. REQUEST INTERRUPTS SEQUENCE



SELECT OUT, SYNC OUT = Inactive
(Master and Slave Conn.)

SYNC IN = Released
(Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tB	Master bus release from MASTER OUT	0.025	-	µs
tC'	Slave Interrupt Response Delay	0	IRT	µs
tE	Slave bus release	0	SDE	µs
tZ	Cable delay	0	CMX	µs

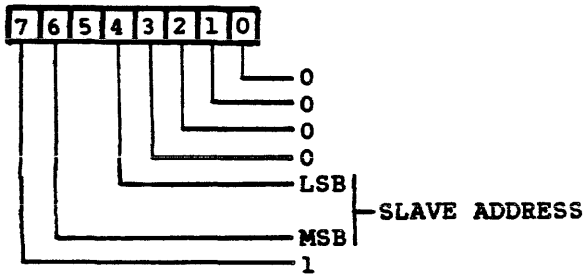
NOTE 1. The slave sets only the line corresponding to its bit significant address.

NOTE 2. The master receives valid interrupts only for the bit positions corresponding to the responding slaves on the bus.

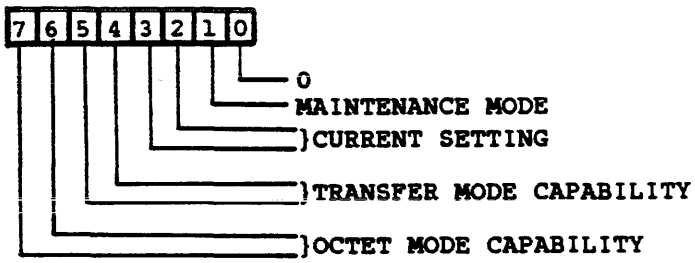
NOTE 3. The response of the slaves is not synchronous, and the master must wait a time equal to that of the slowest and/or furthest slave to respond before latching or sampling BUS B. In addition, the master must wait for a time equal to that of the slowest and/or furthest slave to detect the IDLE state, and release its bit significant address on BUS B before starting another sequence.

FIGURE 7. REQUEST INTERRUPTS TIMING

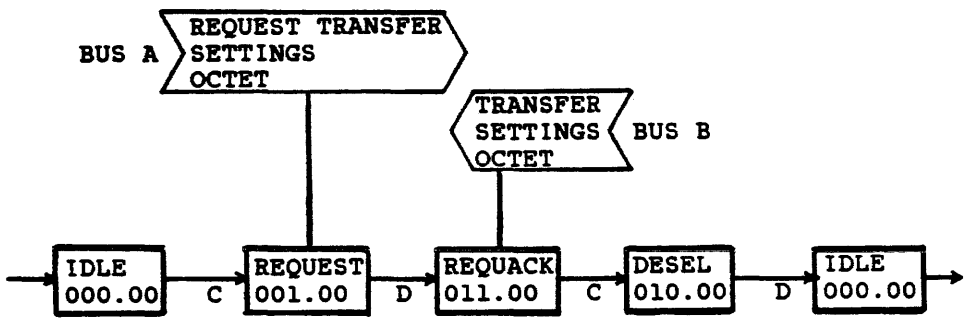
REQUEST TRANSFER SETTINGS OCTET (MASTER)



TRANSFER SETTINGS OCTET (SLAVE)



REQUEST TRANSFER SETTINGS SEQUENCE



DEFINITION: XXX.XX

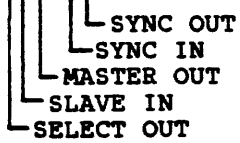
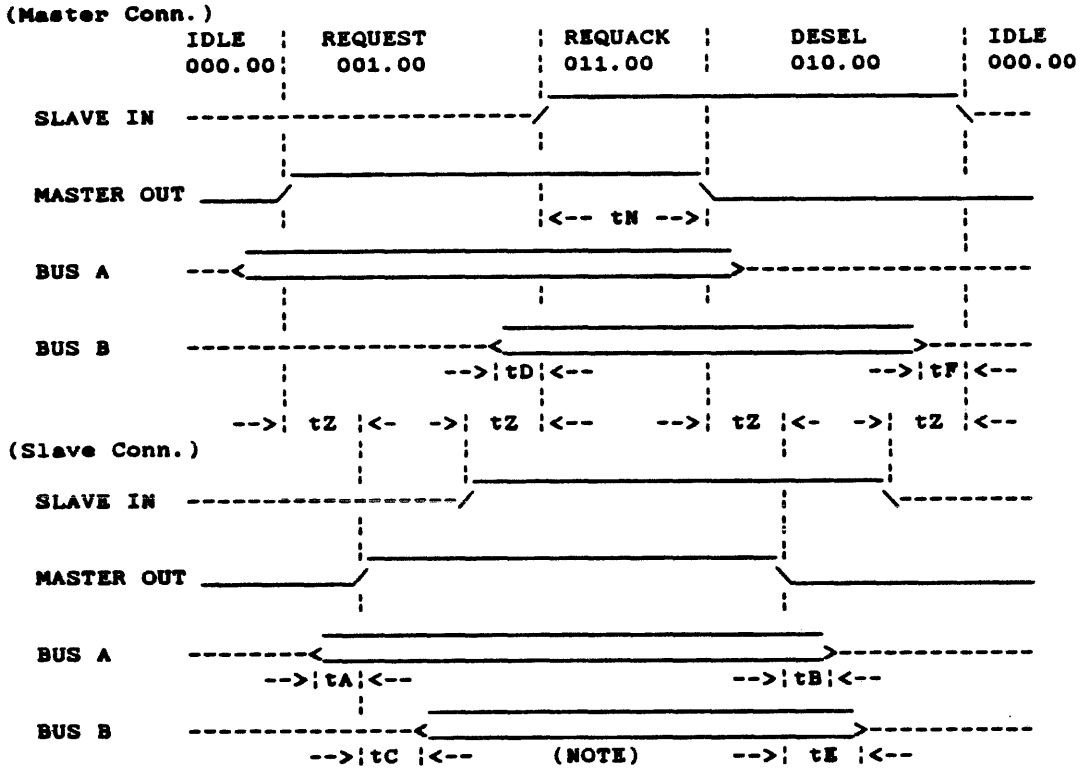


FIGURE 8. REQUEST TRANSFER SETTINGS SEQUENCE



SELECT OUT, SYNC OUT = Inactive
(Master and Slave Conn.)

SYNC IN = Released
(Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tB	Master bus release from MASTER OUT	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tE	Slave bus release	0	SDE	µs
tF	Slave bus release set-up	0.025	SDE	µs
tN	Master interlock delay	0	-	µs
tZ	Cable delay	0	CMX	µs

NOTE: For a Request Transfer Settings sequence, the addressed slave sets its Transfer Settings octet on BUS B.

For a Request Facility Interrupts sequence, the addressed slave sets only the line(s) corresponding to the facility(ies) under its control requesting attention, subject to the Request Modifier on Bus A. Note that the contents of BUS B may change after the assertion of SLAVE IN due to interrupts changing dynamically at the facility(ies).

For a Request Slave Interrupts sequence, the addressed slave sets its Slave Interrupts octet on BUS B. Note that the contents of BUS B may change after the assertion of SLAVE IN due to interrupts changing dynamically at the slave.

FIGURE 9. REQUEST TRANSFER SETTINGS TIMING

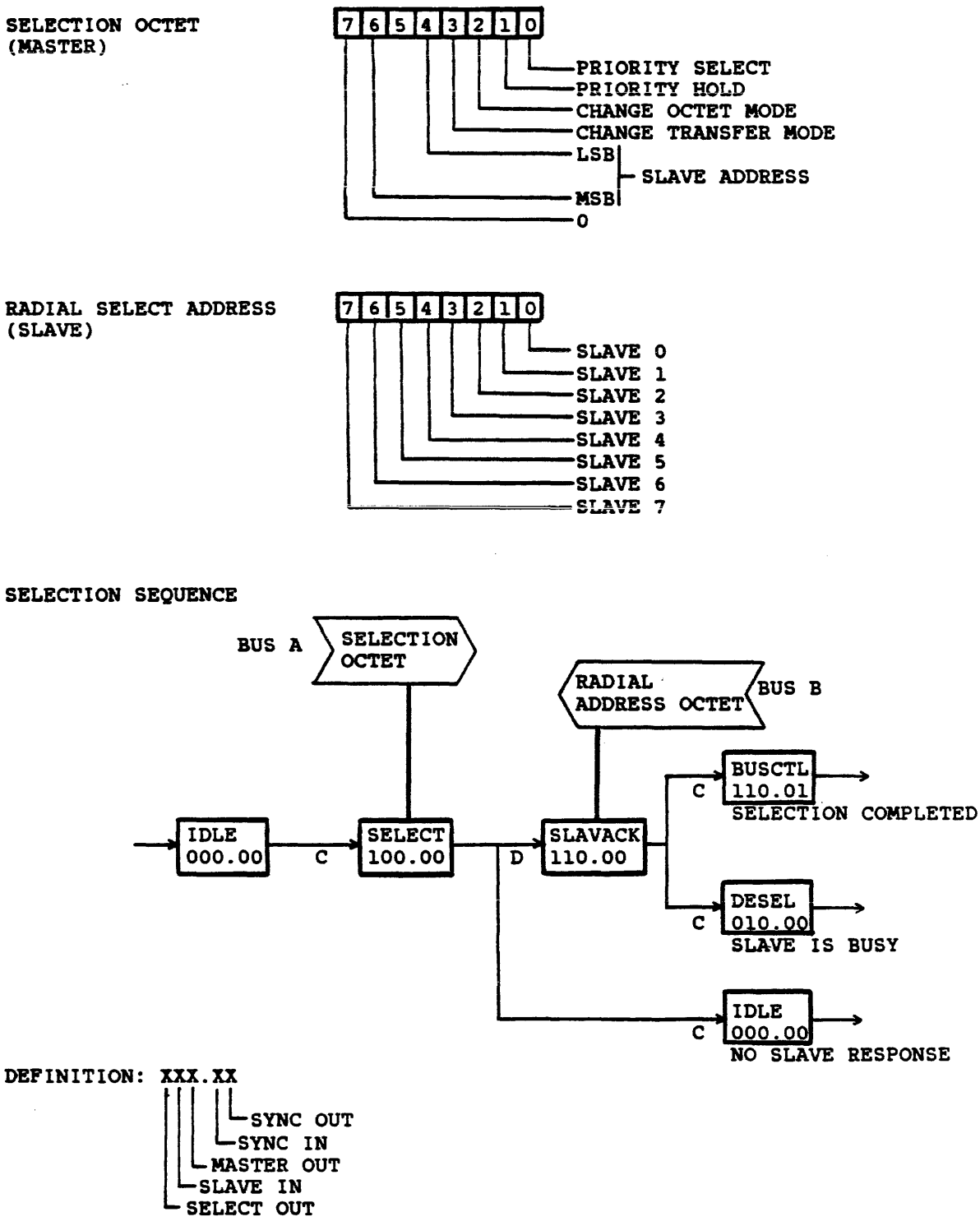
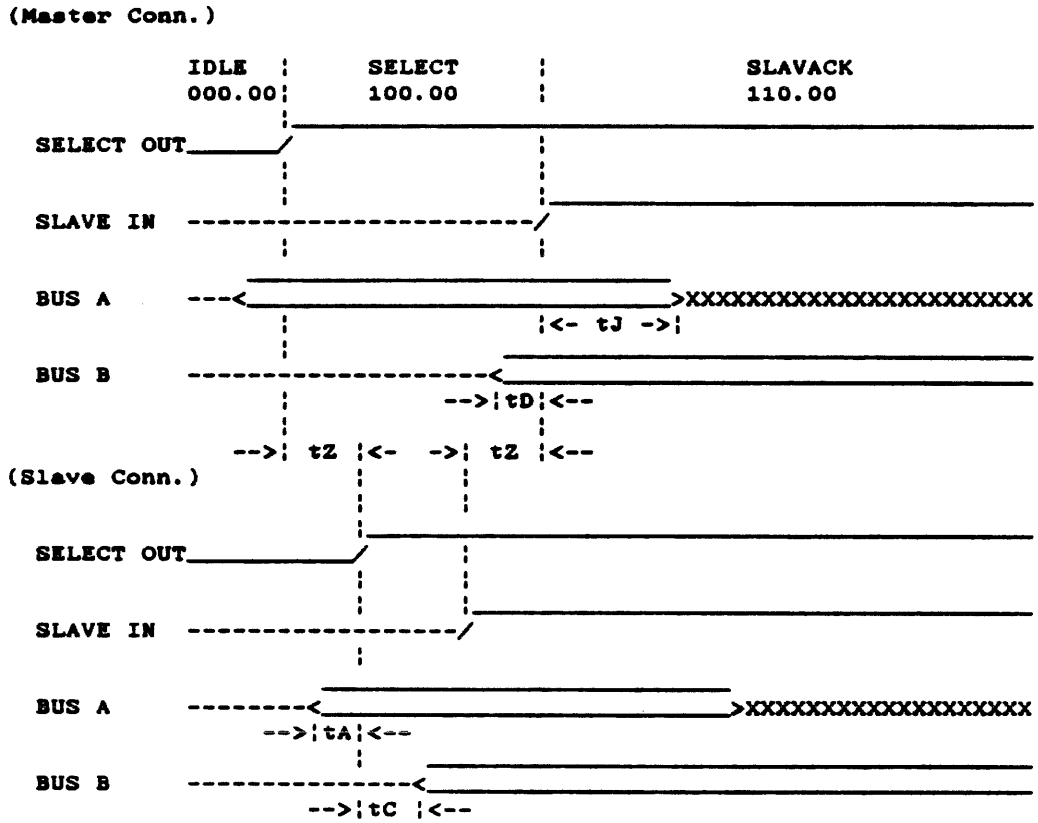


FIGURE 10. SELECTION SEQUENCE



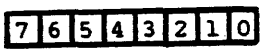
MASTER OUT,SYNC OUT = Inactive
(Master and Slave Conn.)

SYNC IN = Released
(Master and Slave Conn.)

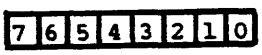
Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tJ	Master bus hold	0	-	µs
tZ	Cable delay	0	CMX	µs

FIGURE 11. SELECTION TIMING

BUS A
(BUS A IS NOT DEFINED FOR THE DESELECTION SEQUENCE)



BUS B
(BUS B IS NOT DEFINED FOR THE DESELECTION SEQUENCE)

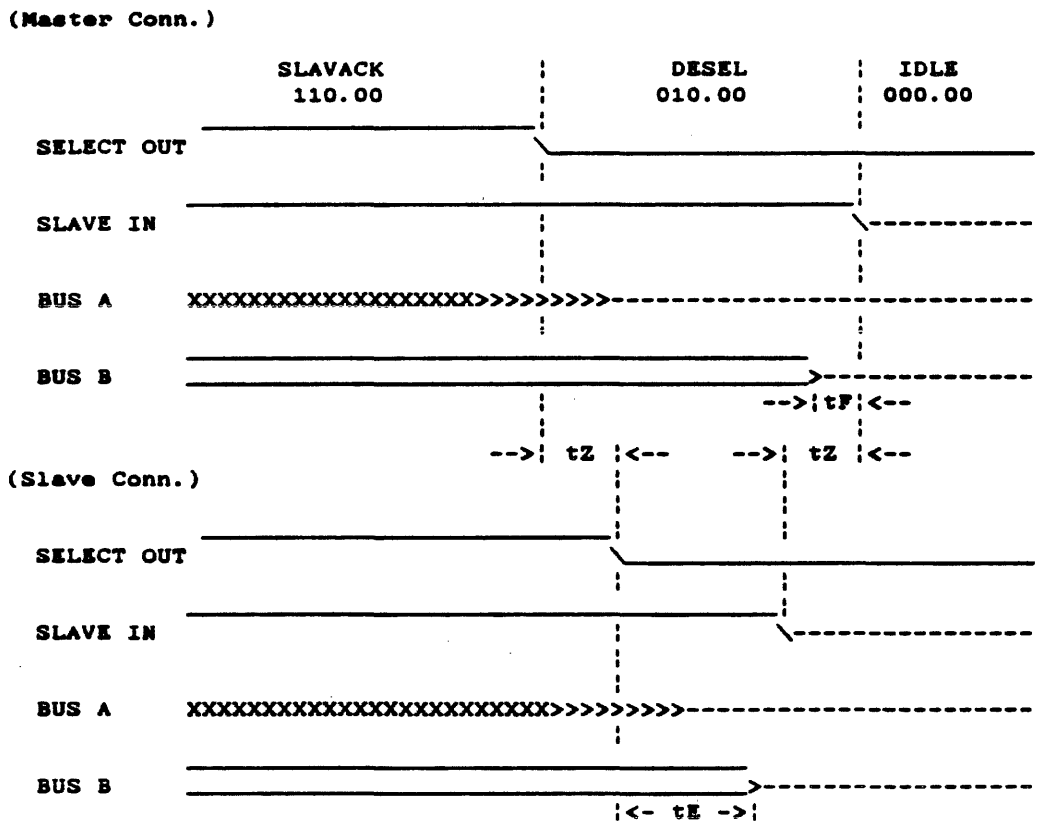


DESELECTION SEQUENCE

DEFINITION: XXX.XX

- SYNC OUT
- SYNC IN
- MASTER OUT
- SLAVE IN
- SELECT OUT

FIGURE 12. DESELECTION SEQUENCE



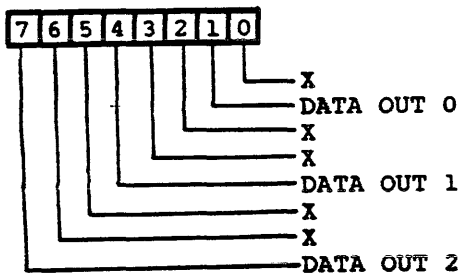
MASTER OUT,SYNC OUT = Inactive (Master and Slave Conn.)

SYNC IN = Released (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tE	Slave bus release	0	SDE	µs
tF	Slave bus release set-up	0.025	SDE	µs
tZ	Cable delay	0	CMX	µs

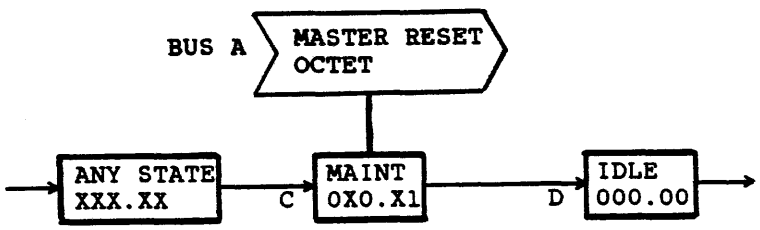
FIGURE 13. DESELECTION TIMING

BUS A



BUS B
(THERE IS NO BUS B
RESPONSE TO A
MASTER RESET)

MASTER RESET SEQUENCE



DEFINITION: XXX.XX

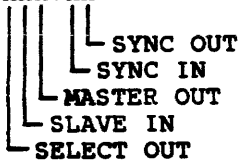
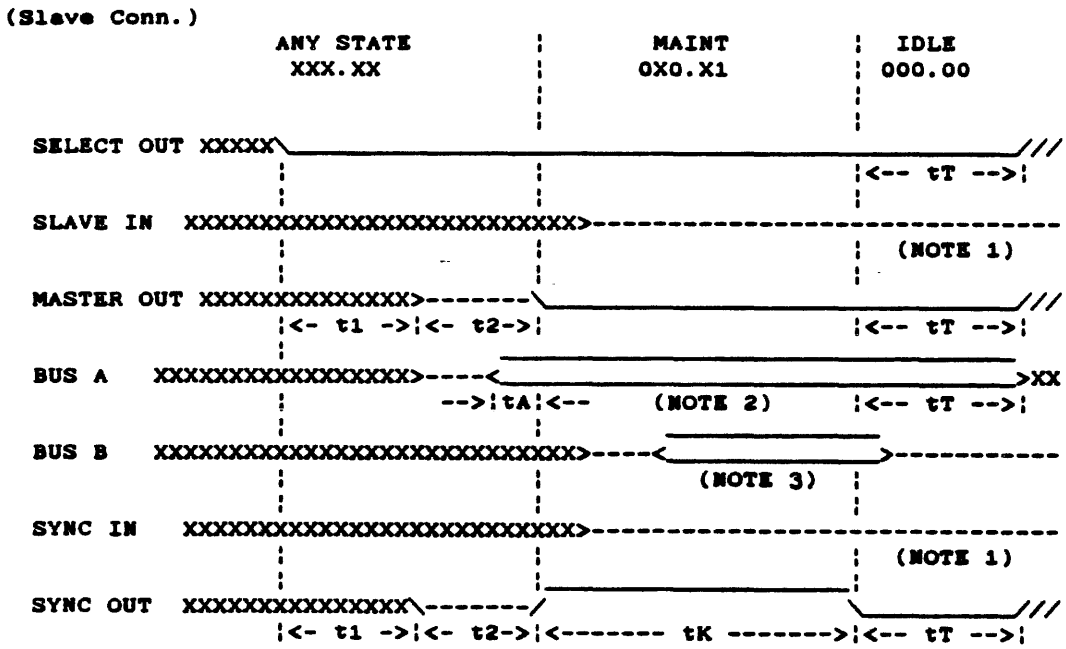


FIGURE 14. MASTER RESET SEQUENCE



Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tK	SYNC OUT pulse width for MAINT (see NOTE 4)	10	-	µs
tT	IDLE following MAINT (see NOTE 5)	6	-	µs
t1	Dominant Slave MASTER OUT, SYNC OUT and BUS A release from SELECT OUT negation (see NOTE 6)	0	1	µs
t2	Master SYNC OUT assertion, MASTER OUT negation from MASTER OUT, SYNC OUT release (see NOTE 6)	1	-	µs

NOTE 1. Signal In lines may or may not be released after MAINT (see section 3.6).
NOTE 2. BUS A is used for maintenance actions (see section 7.5).
NOTE 3. BUS B is optionally used for maintenance actions (see section 7.5).
NOTE 4. The slave shall not enter Maintenance Mode until the MAINT state has been active for at least two microseconds.
NOTE 5. The slave shall not reset until IDLE has been active after MAINT for at least two microseconds.
NOTE 6. If there are no slaves on the cable that implement slave to slave information transfers, the master shall hold all control Out signals inactive for a period of at least one microsecond (t2) before asserting SYNC OUT to enter the MAINT state.

FIGURE 15. MASTER RESET TIMING

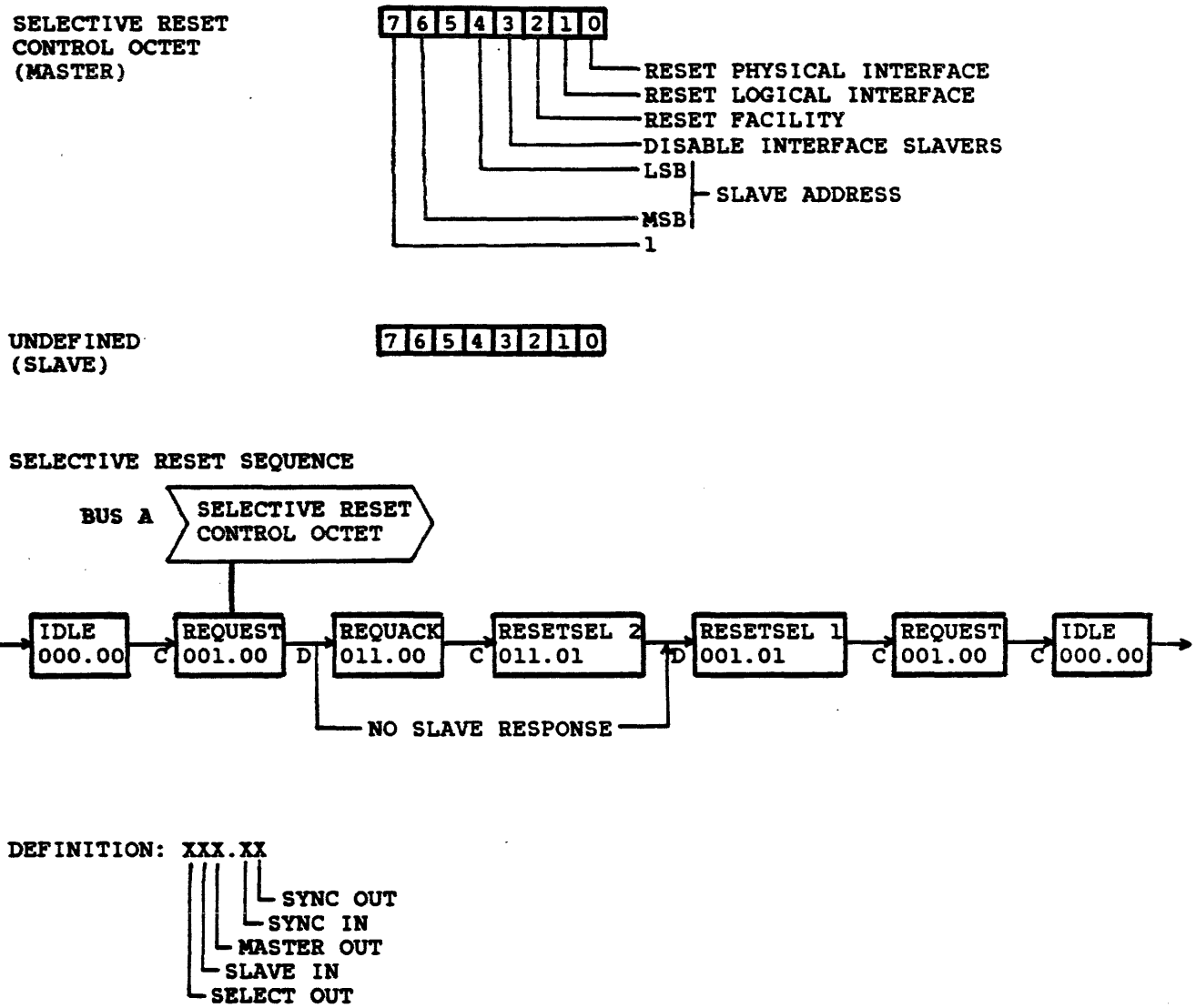
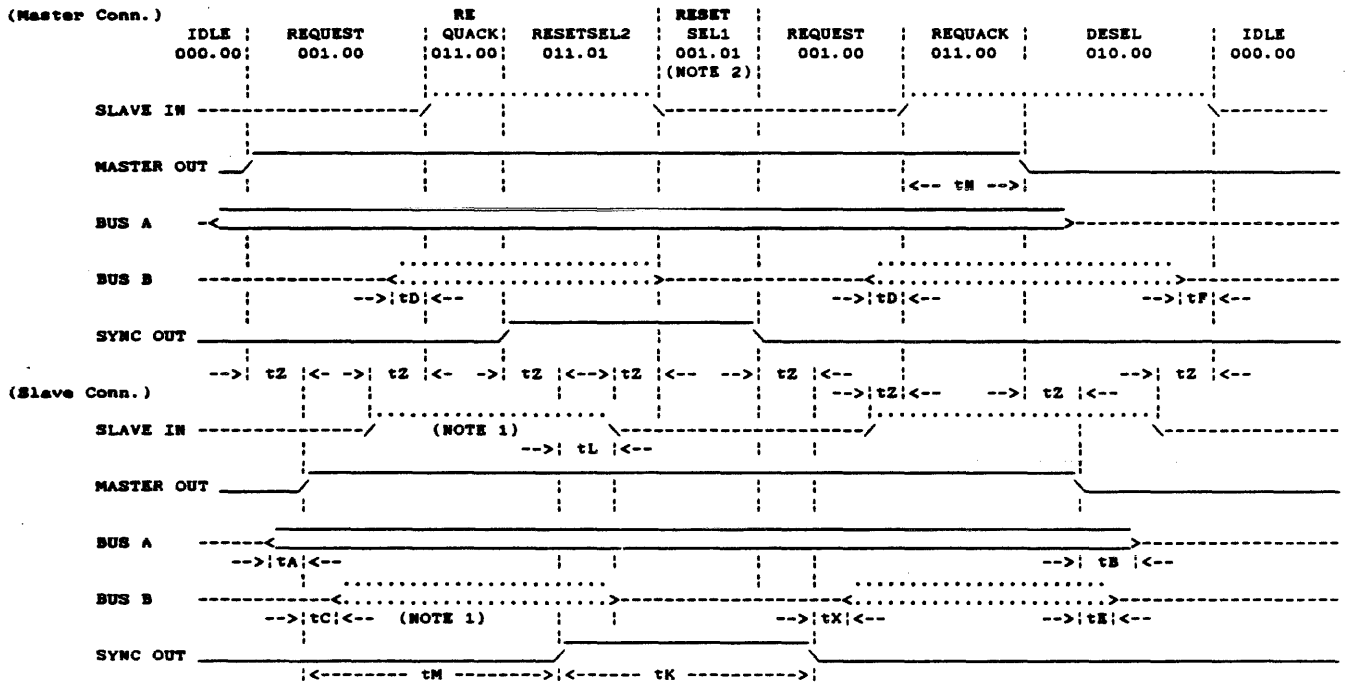


FIGURE 16. SELECTIVE RESET SEQUENCE

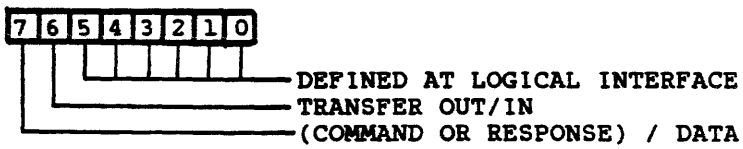


Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tK	SYNC OUT pulse width for reset	10	-	µs
tB	Master bus release from MASTER OUT	0.025	-	usecs.	tL	Slave reset response	0	SDE	µs
tC	Slave turnaround	0	SDE	usecs.	tM	MASTER OUT to SYNC OUT set-up	SDE	-	µs
tD	Slave bus set-up	0.025	SDE	usecs.	tN	Master interlock delay	0	-	µs
tE	Slave bus release	0	SDE	usecs.	tX	Slave reset delay	0	SDR	µs
tF	Slave bus release set-up	0.25	SDE	usecs.	tZ	Cable delay	0	CMX	µs

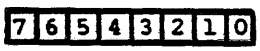
NOTE 1. The slave may or may not respond at this point e.g. a slave which does not support Request Facilities Interrrupts.
NOTE 2. The slave shall not reset unless the RESETSEL1 state has been active for at least two microseconds.

FIGURE 17. SELECTIVE RESET TIMING

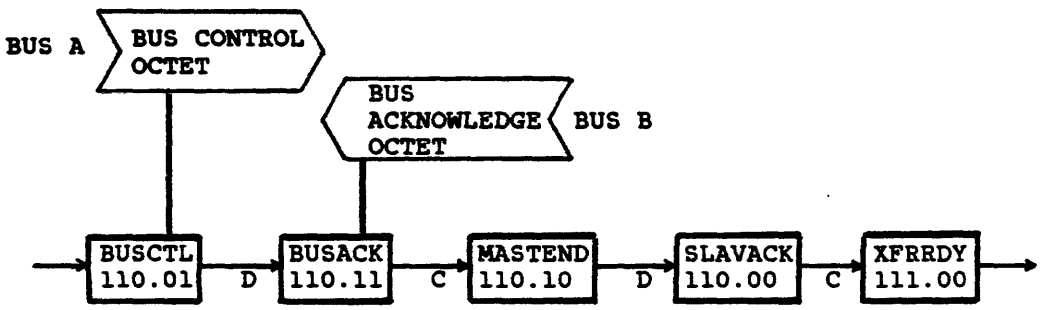
BUS CONTROL OCTET
(MASTER)



BUS ACKNOWLEDGE OCTET
(SLAVE)
BUS B IS NOT DEFINED
ZEROS WILL BE RETURNED



BUS CONTROL SEQUENCE



DEFINITION: XXX.XX

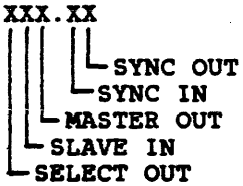
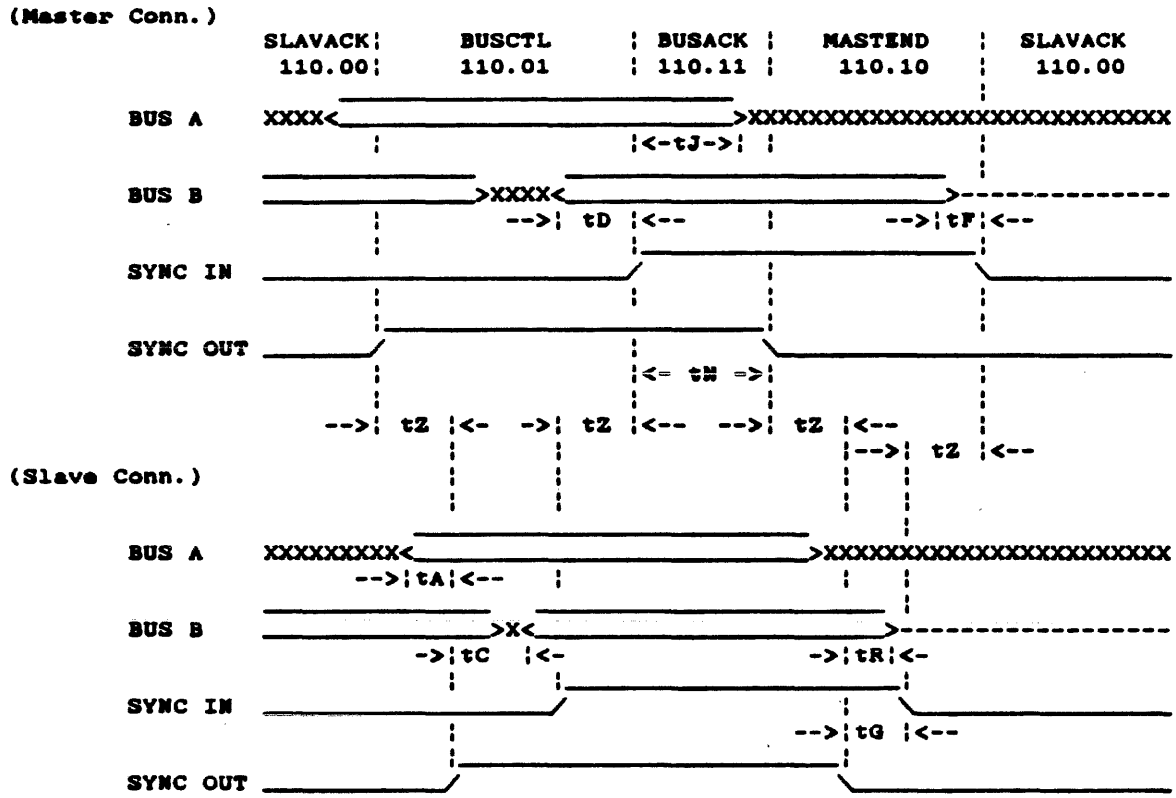


FIGURE 18. BUS CONTROL SEQUENCE

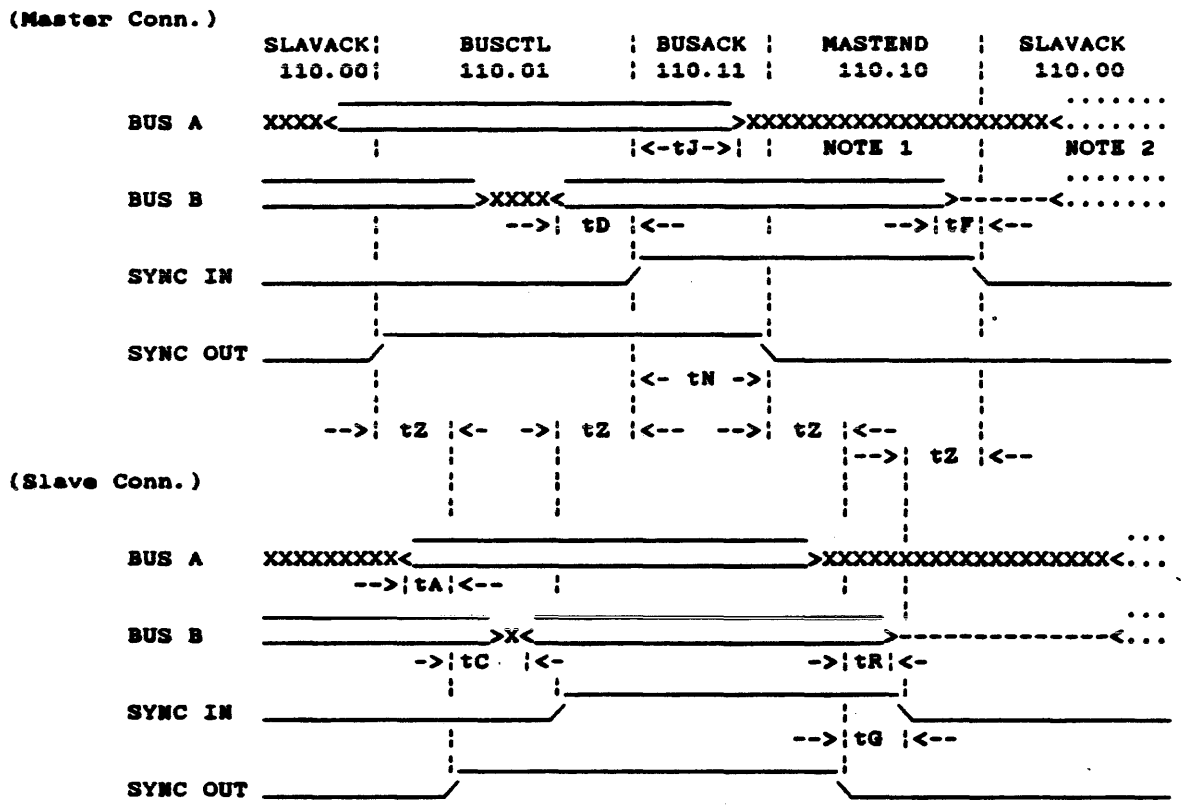


SELECT OUT, SLAVE IN = Active (Master and Slave Conn.)

MASTER OUT = Inactive (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tJ	Master bus hold	0	-	µs
tN	Master interlock delay	0	-	µs
tR	Slave bus hold	0	-	µs
tZ	Cable delay	0	CMX	µs

FIGURE 19A. BUS CONTROL TIMING PRECEDING TRANSFERS IN



SELECT OUT, SLAVE IN = Active (Master and Slave Conn.)

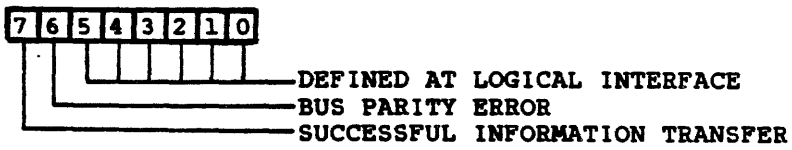
MASTER OUT = Inactive (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tF	Slave bus release set-up	0.25	SDE	µs
tZ	Cable delay	0	CMX	µs
tG	Slave interlock delay	0	SDE	µs
tJ	Master bus hold	0	-	µs
tN	Master interlock delay	0	-	µs
tR	Slave bus hold	0	-	µs

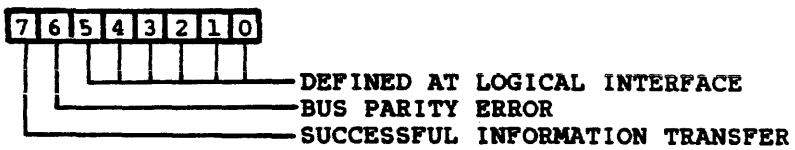
NOTE 1. The Slave shall release BUS B prior to entry to the SLAVACK state so that a Master implementation that wraps SYNC IN to produce SYNC OUT may meet the setup time requirements for the first SYNC IN pulse during DOM streaming.
NOTE 2. The master may or may not be driving the buses.

FIGURE 19B. BUS CONTROL TIMING PRECEDING TRANSFERS OUT

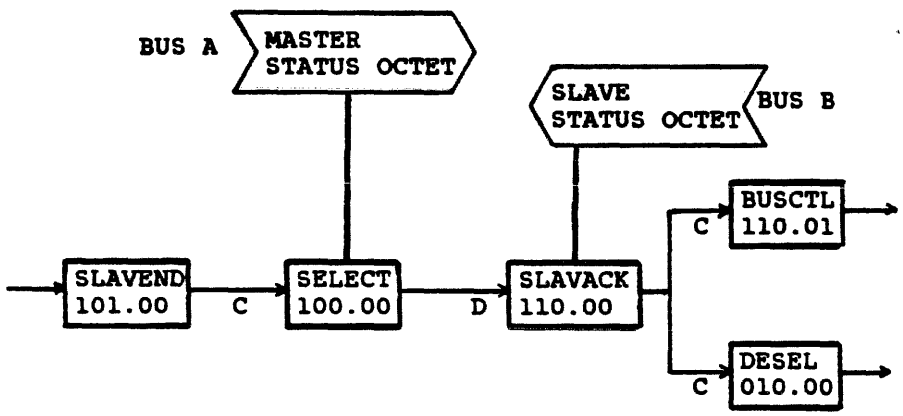
MASTER STATUS OCTET
(MASTER)



SLAVE STATUS OCTET
(SLAVE)



ENDING STATUS SEQUENCE



DEFINITION: XXX.XX

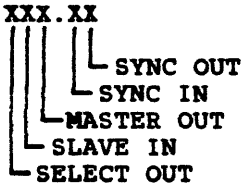
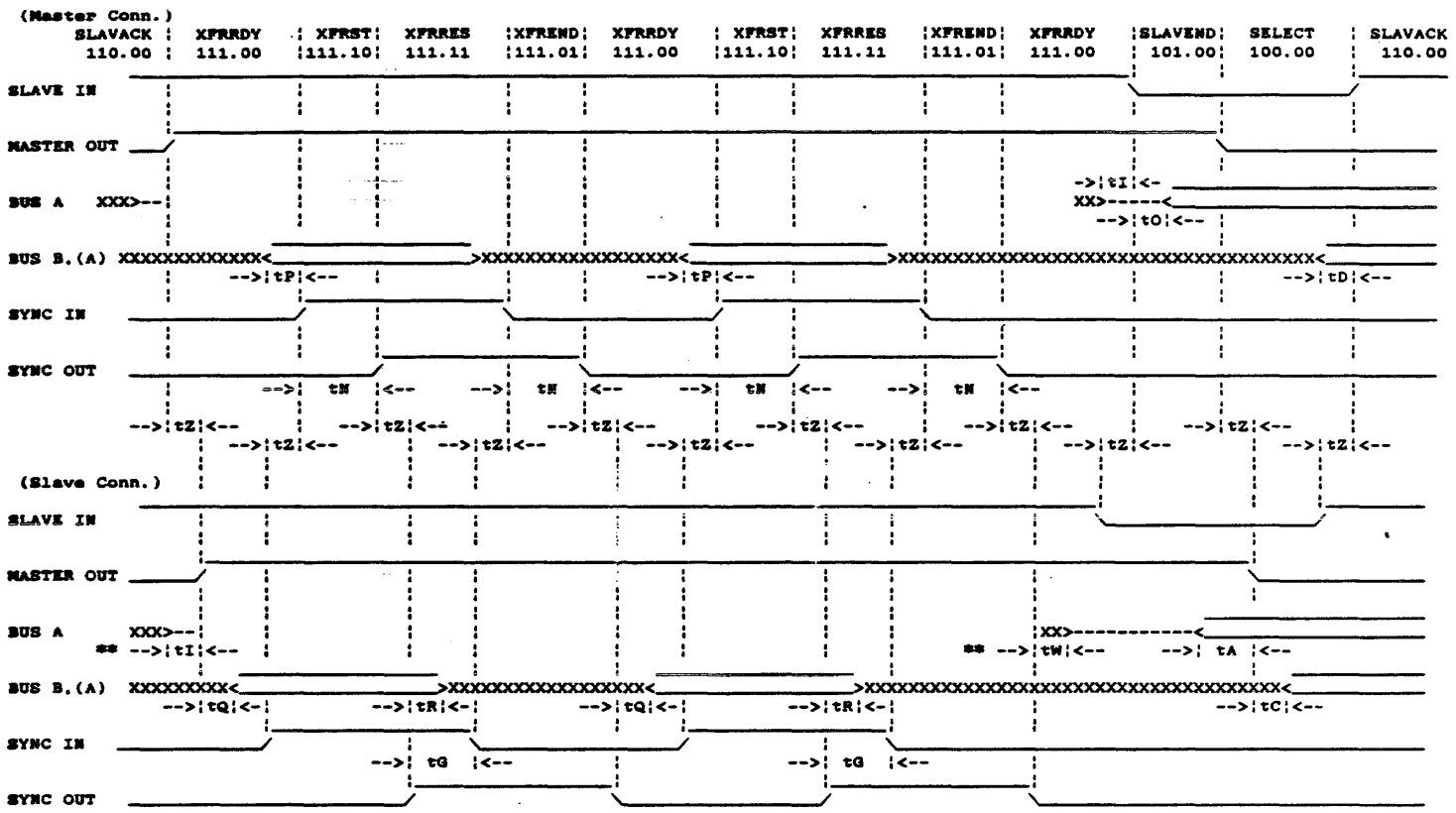
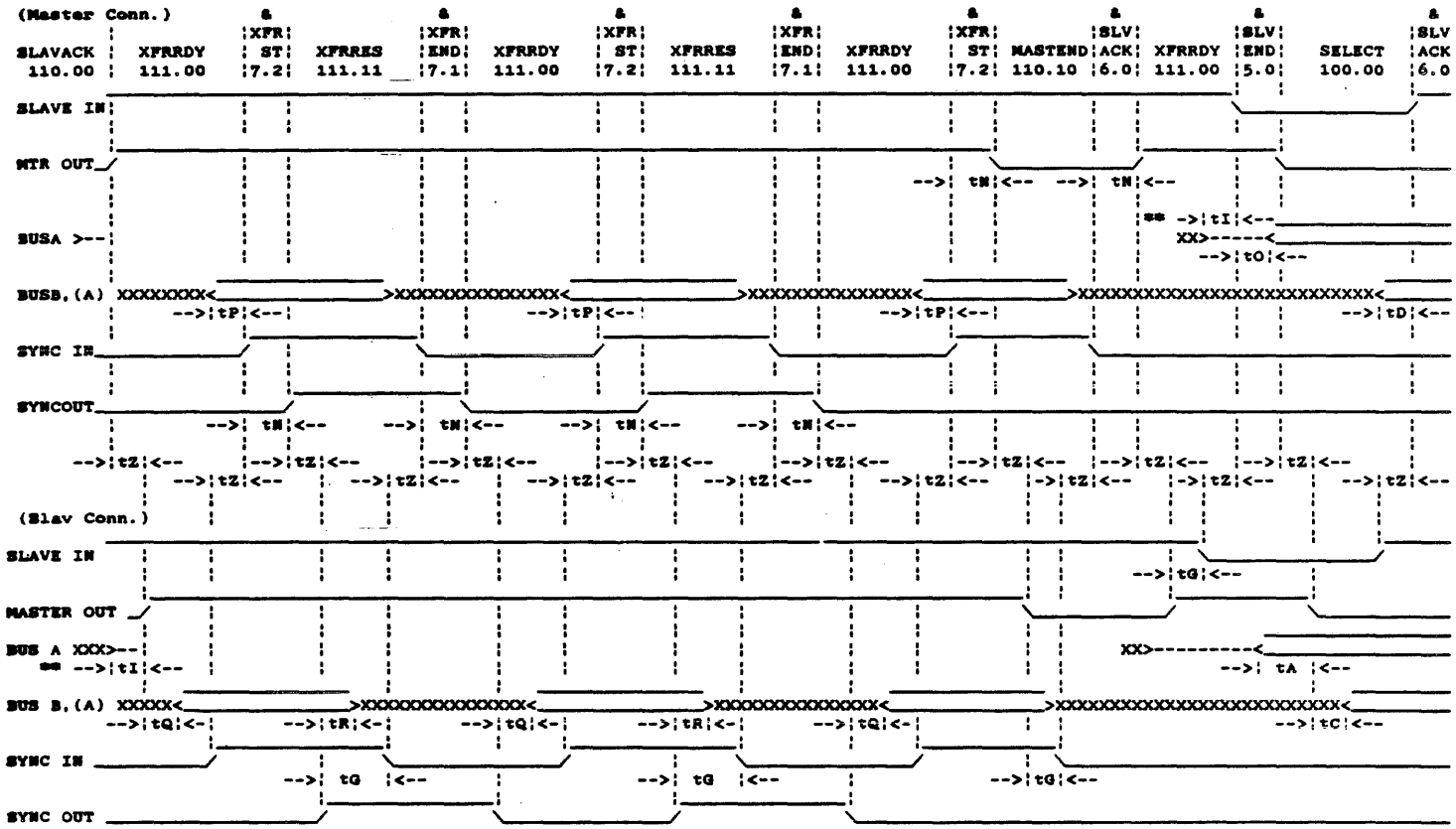


FIGURE 20. ENDING STATUS SEQUENCE



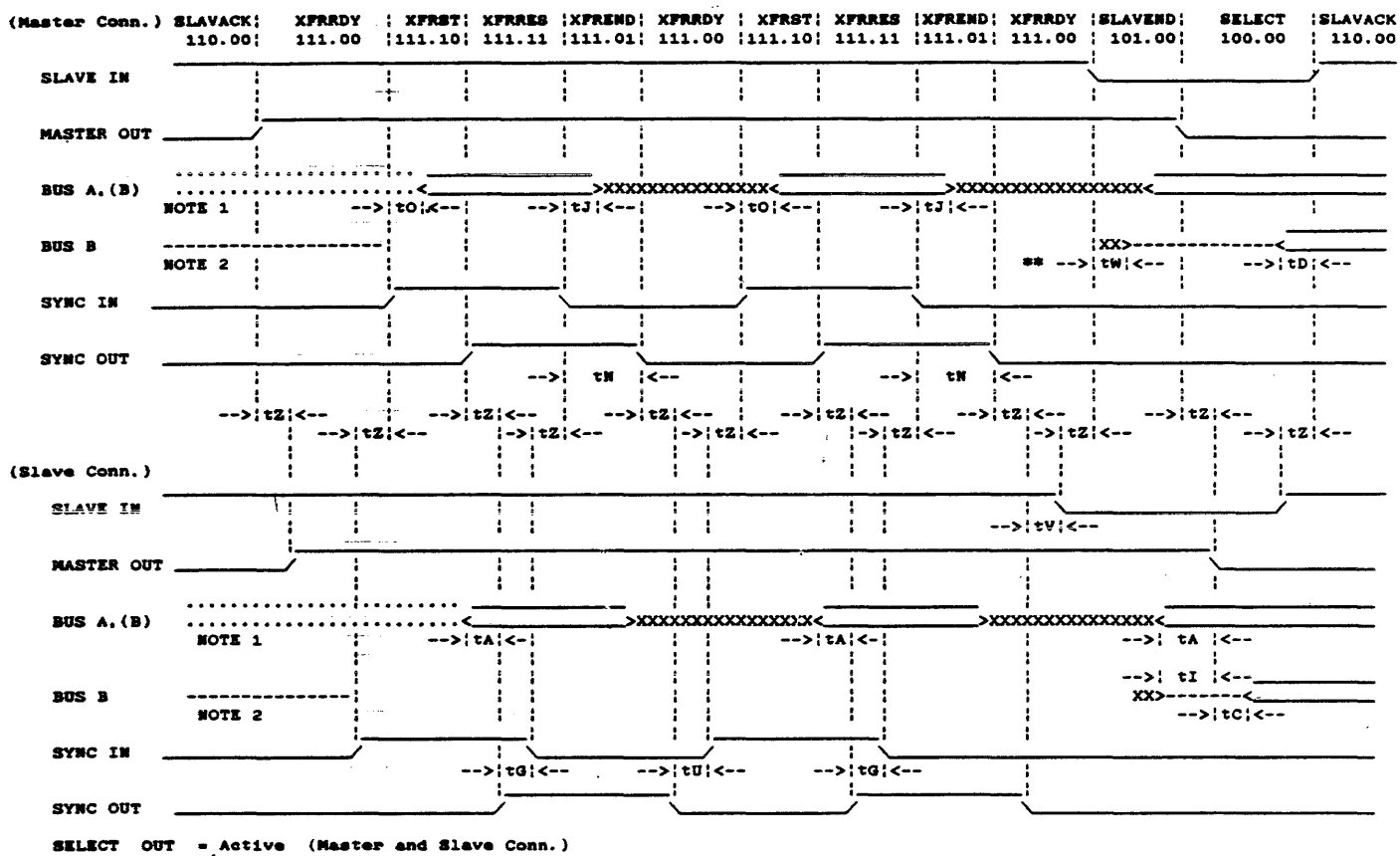
Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tD	Slave bus set-up	0.025	SDE	µs
tI	Bus release set-up	0.025	-	µs
tO	Master turnaround	0	-	µs
tQ	Slave data turnaround	0	-	µs
tW	Transfer Bus Release	0	-	µs
tC	Slave turnaround	0	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tN	Master interlock delay	0	-	µs
tP	Slave data set-up	0.025	-	µs
tR	Slave bus hold	0	-	µs
tZ	Cable delay	0	CMX	µs

FIGURE 21A. ENDING STATUS TIMING (INPUT, SLAVE TERMINATED)



Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tD	Slave bus set-up	0.025	SDE	µs
tI	Bus release set-up	0.025	-	µs
tO	Master turnaround	0	-	µs
tQ	Slave data turnaround	0	-	µs
tZ	Cable delay	0	CMX	µs
tC	Slave turnaround	0	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tN	Master interlock delay	0	-	µs
tP	Slave data set-up	0.025	-	µs
tR	Slave bus hold	0	-	µs

FIGURE 21B. ENDING STATUS TIMING (INPUT, MASTER TERMINATED)

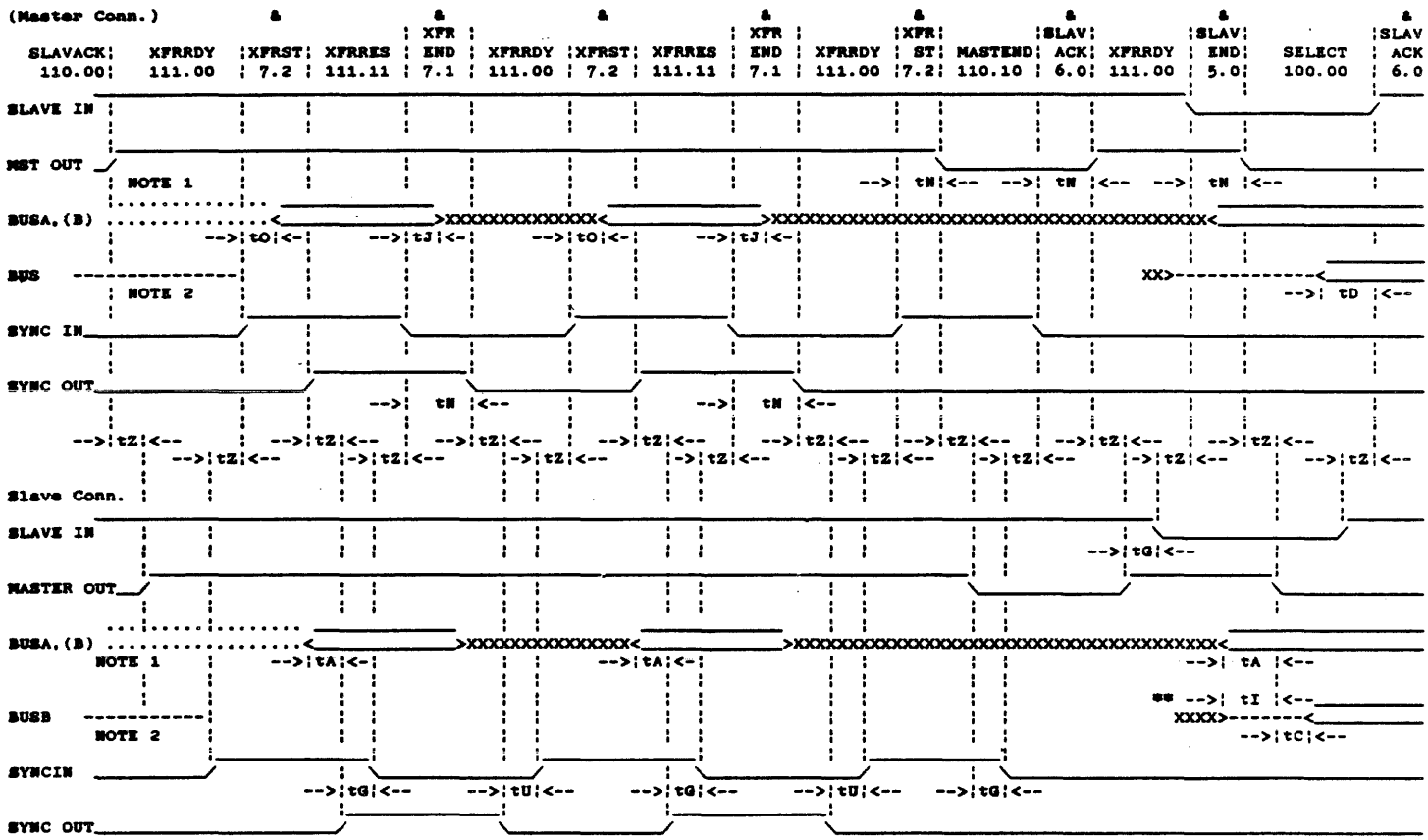


Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tD	Slave bus set-up	0.025	SDE	µs
tI	Bus release set-up	0.025	-	µs
tN	Master interlock delay	0	-	µs
tU	Slave SYNC IN delay	0	-	µs
tW	Transfer bus release	0	-	µs
tC	Slave turnaround	0	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tJ	Master bus hold	0	-	µs
tO	Master turnaround	0	-	µs
tV	Slave end delay	0	-	µs
tZ	Cable delay	0	CMX	µs

NOTE 1. The master may or may not be driving the buses.

NOTE 2. This represents the slave's drivers in DOM only.

FIGURE 21C. ENDING STATUS TIMING (OUTPUT, SLAVE TERMINATED)

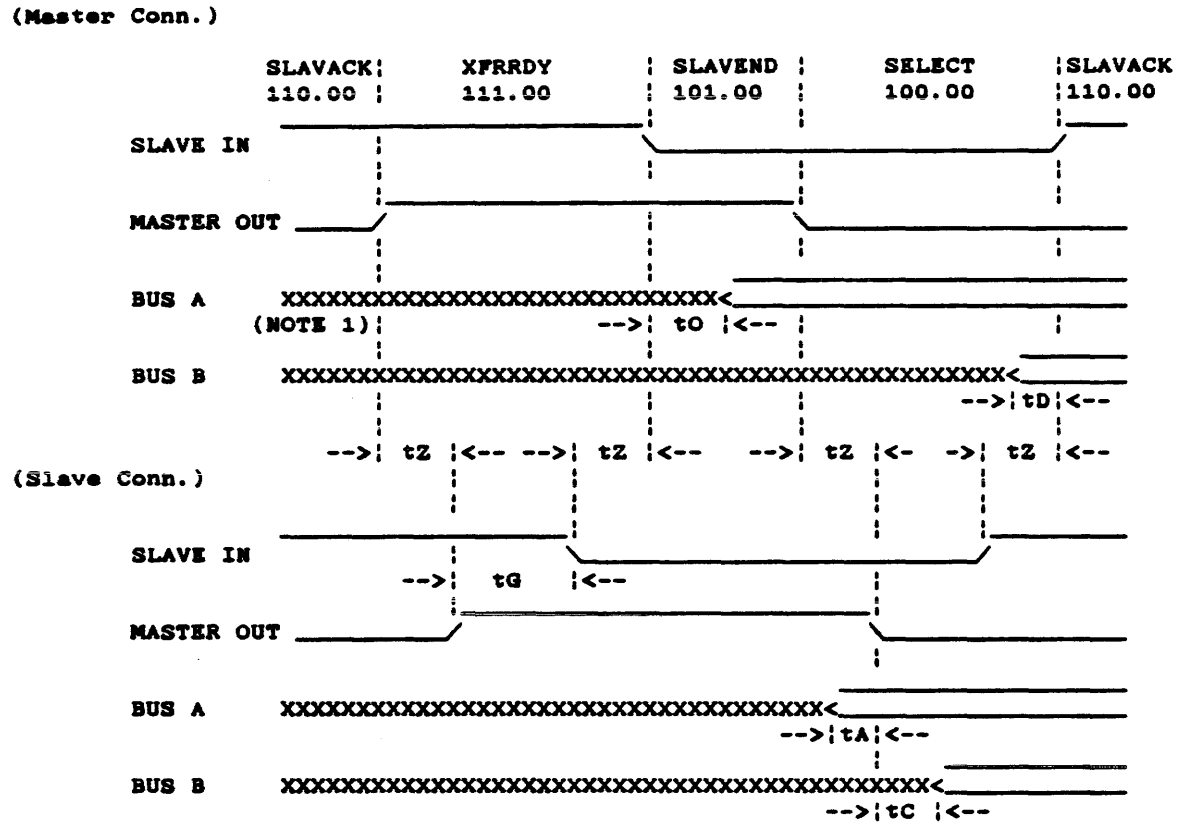


Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tD	Slave bus set-up	0.025	SDE	µs
tI	Bus release set-up	0.025	-	µs
tN	Master interlock delay	0	-	µs
tU	Slave SYNC IN delay	0	-	µs
tZ	Cable delay	0	CMX	µs
tC	Slave turnaround	0	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tJ	Master bus hold	0	-	µs
tO	Master turnaround	0	-	µs
tW	Transfer bus release	0	-	µs

NOTE 1. The master may or may not be driving the buses.

NOTE 2. This represents the slaves drivers in DOM only.

FIGURE 21D. ENDING STATUS TIMING (OUTPUT, MASTER TERMINATED)



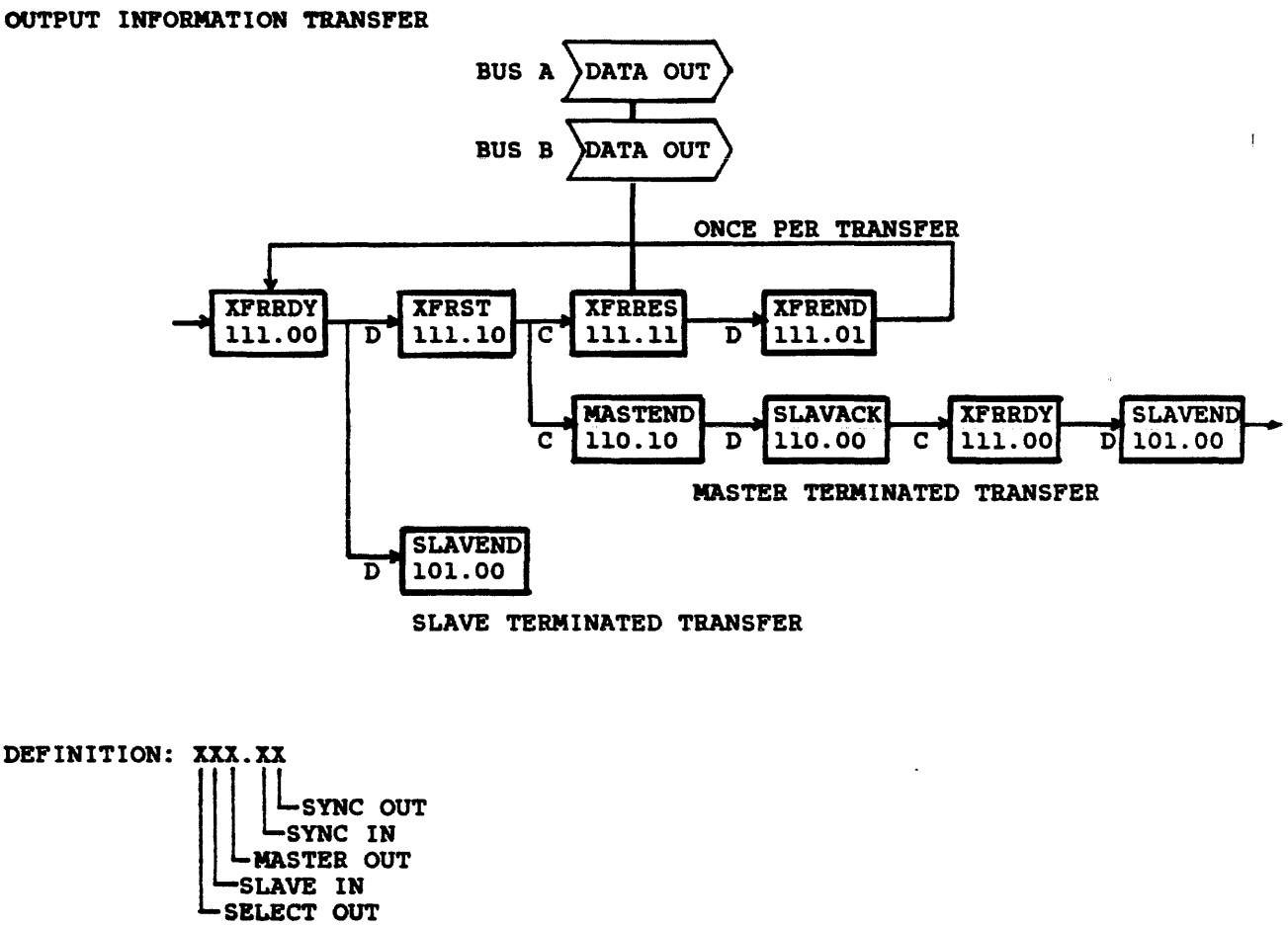
SELECT OUT = Active
(Master and Slave Conn.)

SYNC IN, SYNC OUT = Inactive
(Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tO	Master turnaround	0	-	µs
tZ	Cable delay	0	CMX	µs

NOTE 1. For DOM transfers In, BUS A shall be released before the XFRRDY state is entered (See Figure 5-9).
NOTE 2. This sequence is used if an unrecognizable Bus Control Octet is received at the slave (possibly due to a parity error).
NOTE 3. This sequence is used if there is no required Information Transfer during a Bus Exchange.

FIGURE 21E. ENDING STATUS TIMING (WITHOUT INFORMATION TRANSFER)



DEFINITION: XXX.XX

- SYNC OUT
- SYNC IN
- MASTER OUT
- SLAVE IN
- SELECT OUT

FIGURE 22. OUTPUT INFORMATION TRANSFER SEQUENCE

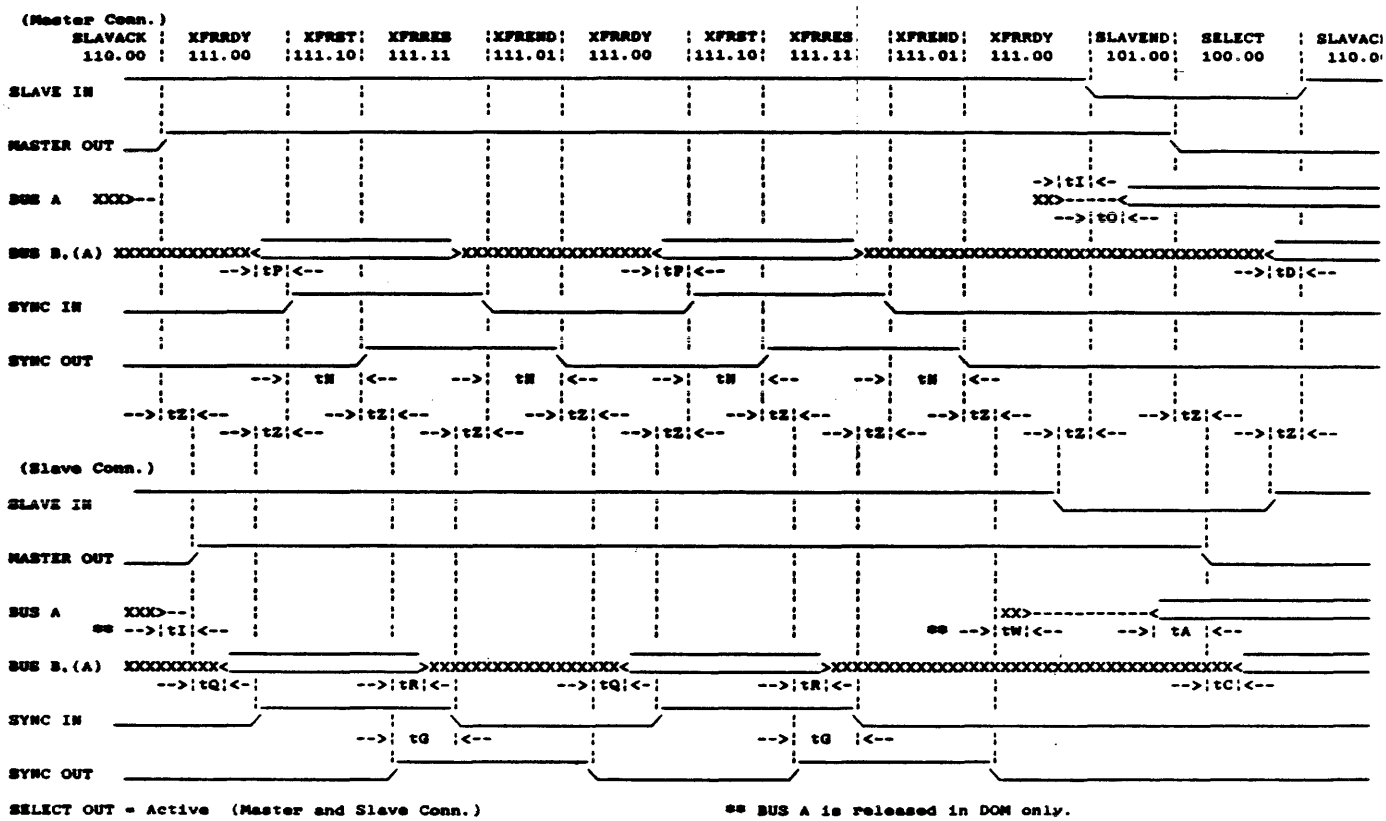


FIGURE 23A. INTERLOCKED INPUT TIMING SLAVE END

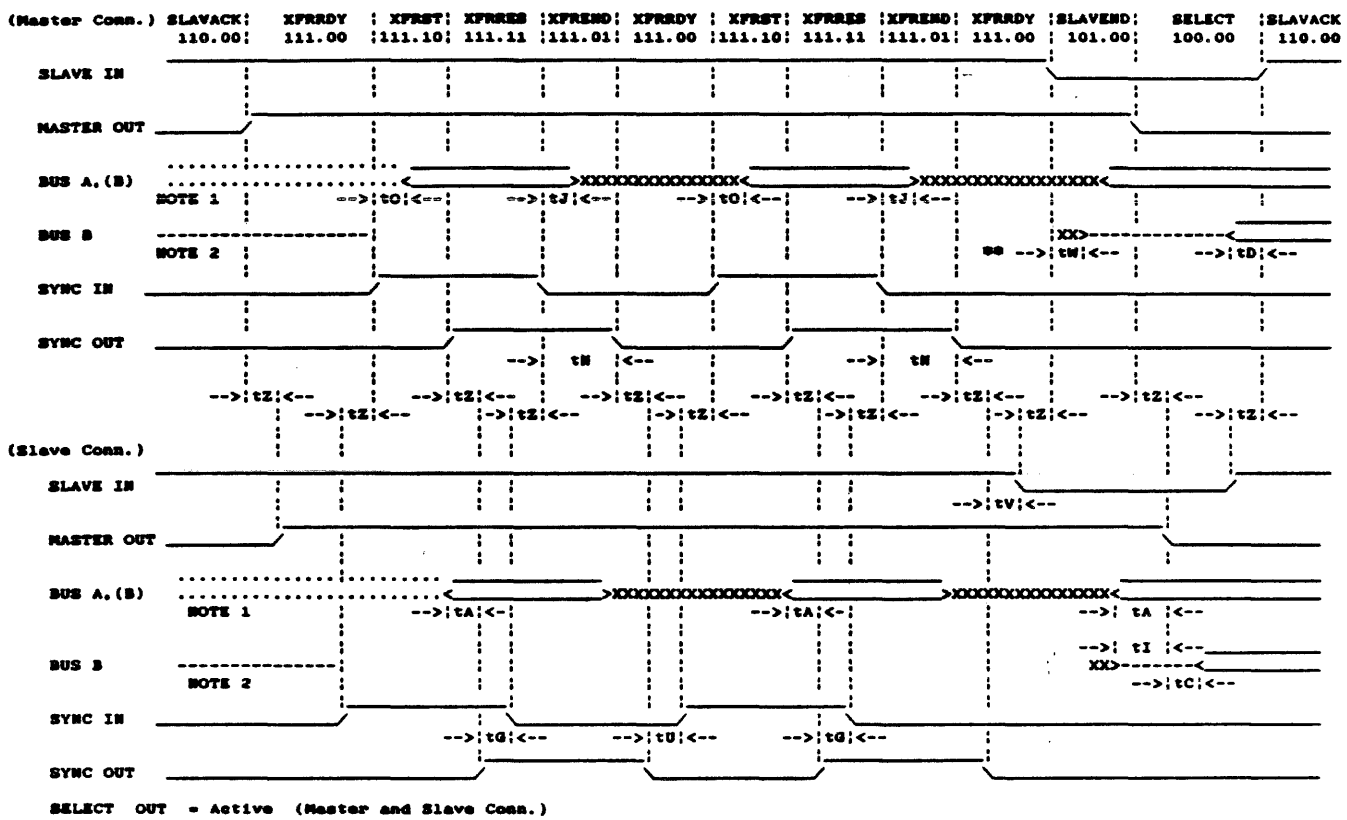


FIGURE 23B. INTERLOCKED OUTPUT TIMING SLAVE END

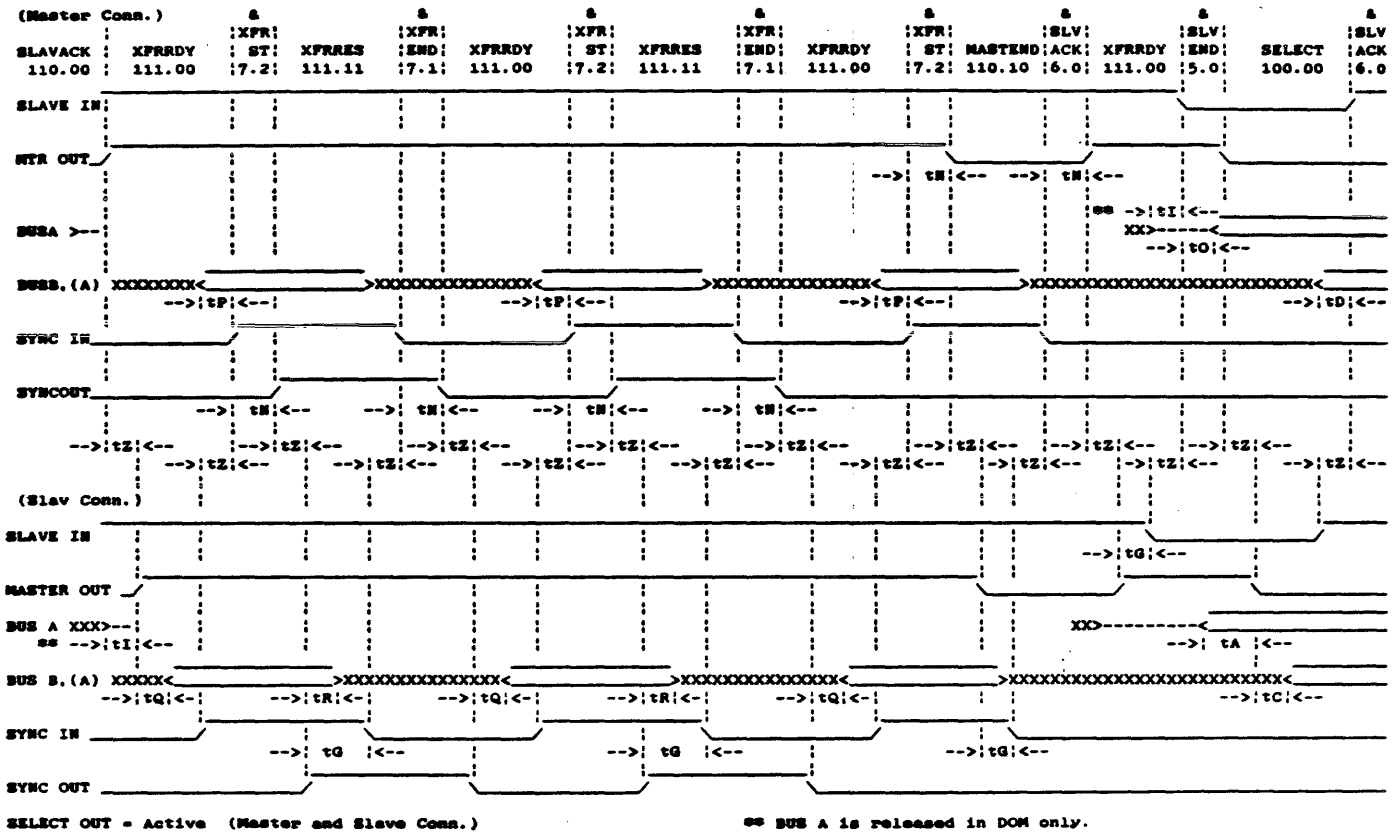


FIGURE 23C. INTERLOCKED INPUT TIMING MASTER END

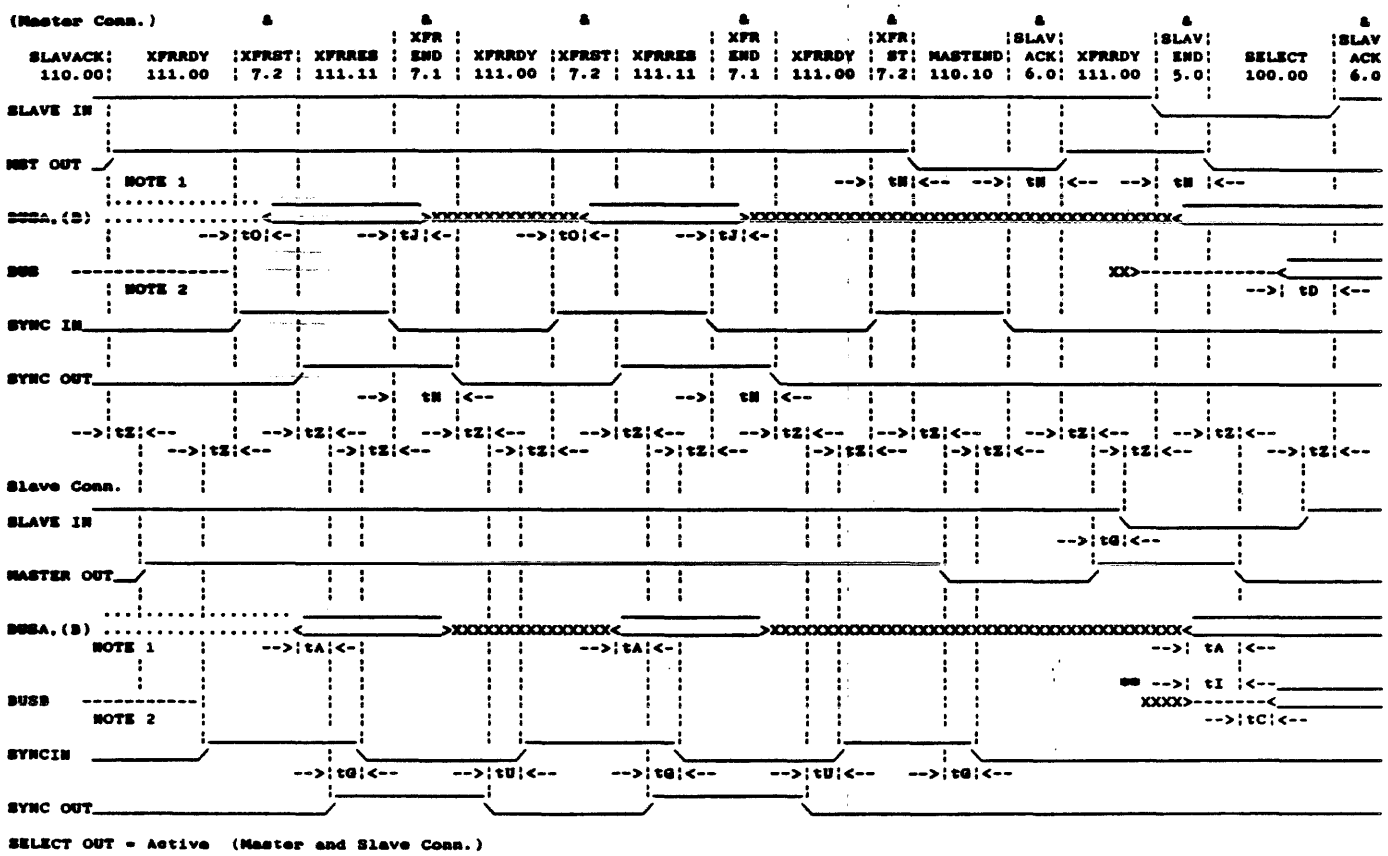
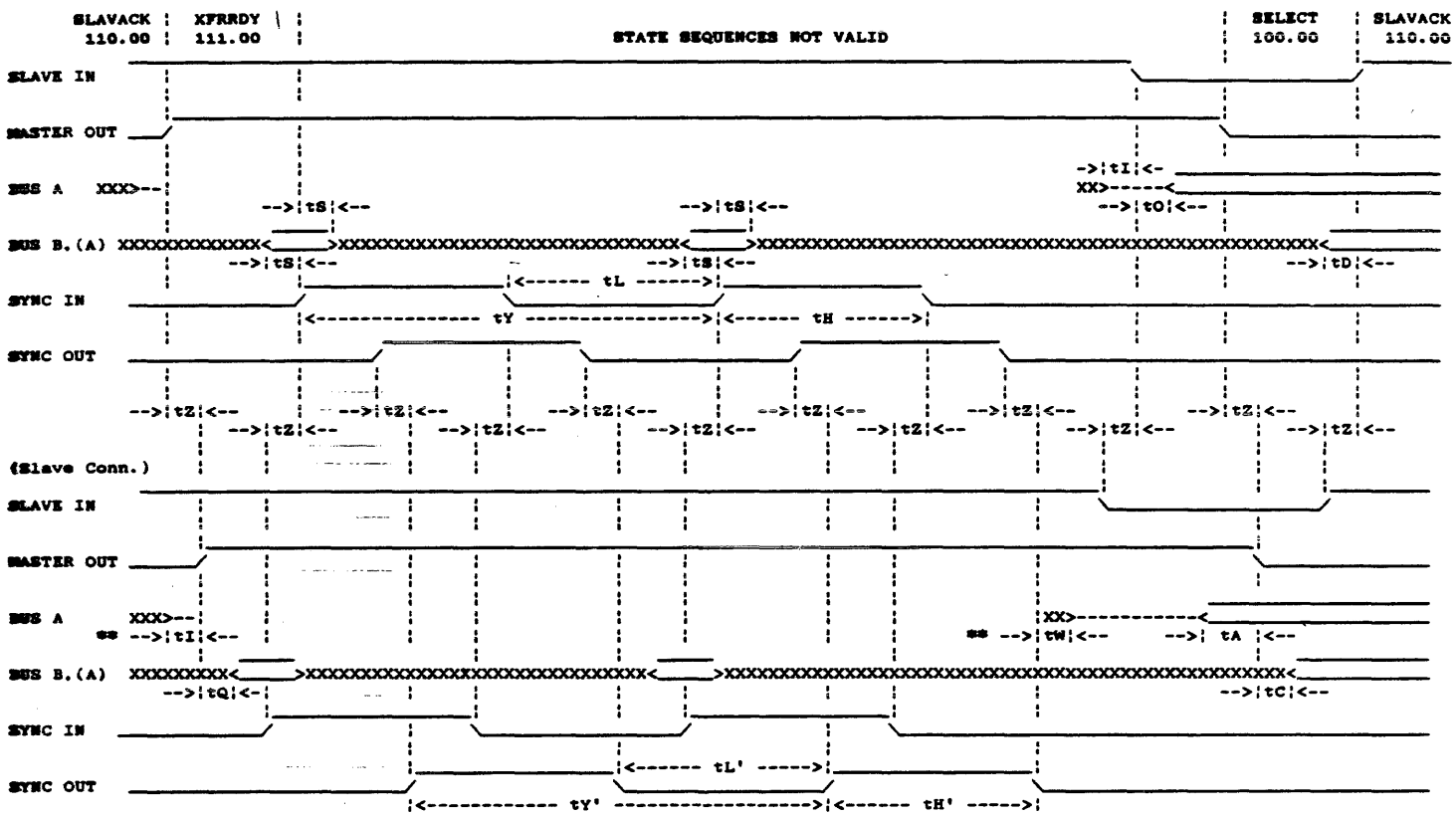
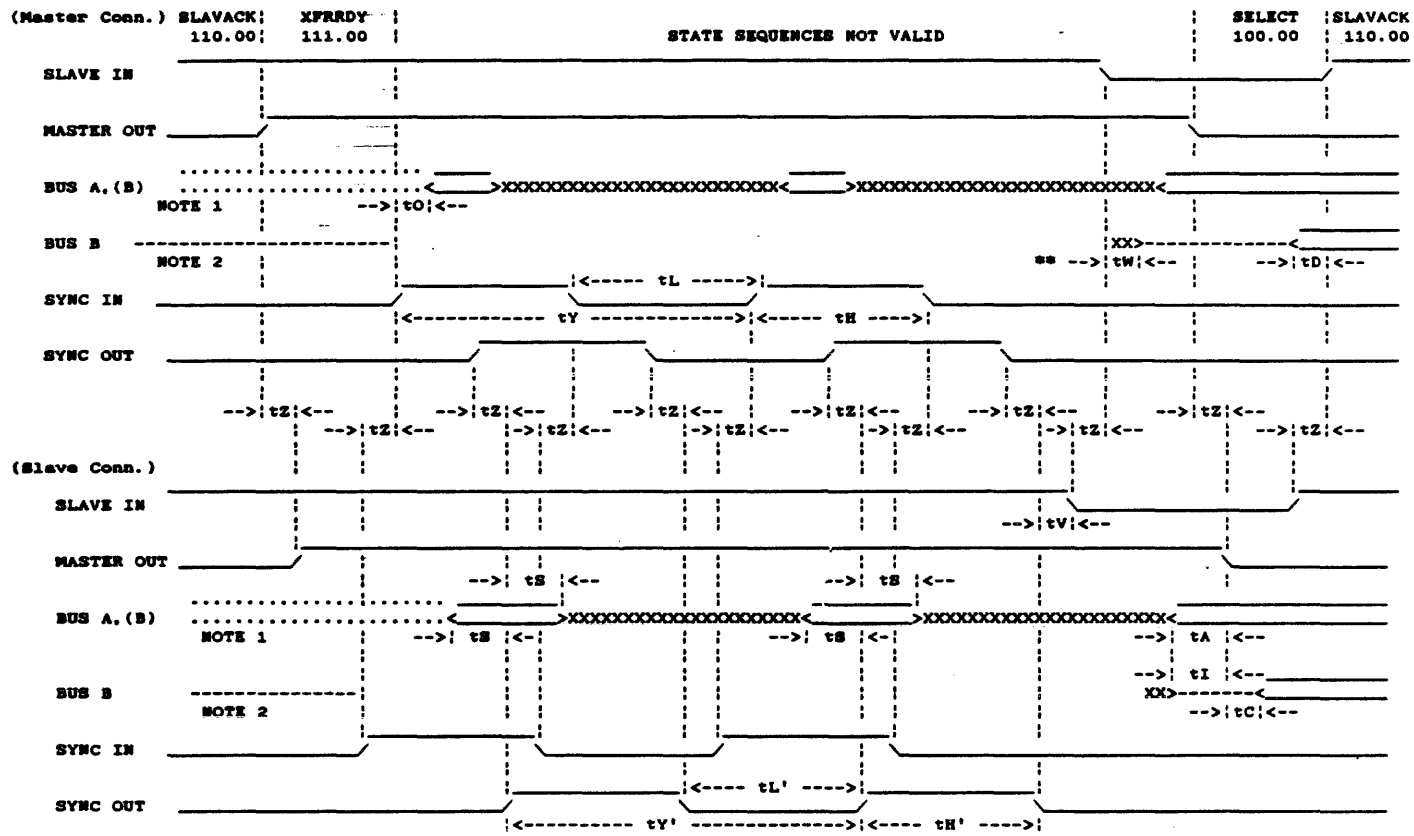


FIGURE 23D. INTERLOCKED OUTPUT TIMING MASTER END



Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tH	SYNC IN pulse active	0.080	-	µs
tH'	SYNC OUT pulse active	0.064	-	µs
tI	Bus release set-up	0.025	-	µs
tL	SYNC IN pulse inactive	0.080	-	µs
tL'	SYNC OUT pulse inactive	0.064	-	µs
tO	Master turnaround	0	-	µs
tQ	Slave data turnaround	0	-	µs
tS	Stream. set-up/hold	0.030	-	µs
tW	Transfer bus release	0	-	µs
tY	SYNC IN period	0.200	-	µs
tY'	SYNC OUT period	0.200	-	µs
tZ	Cable delay	0	CMX	µs

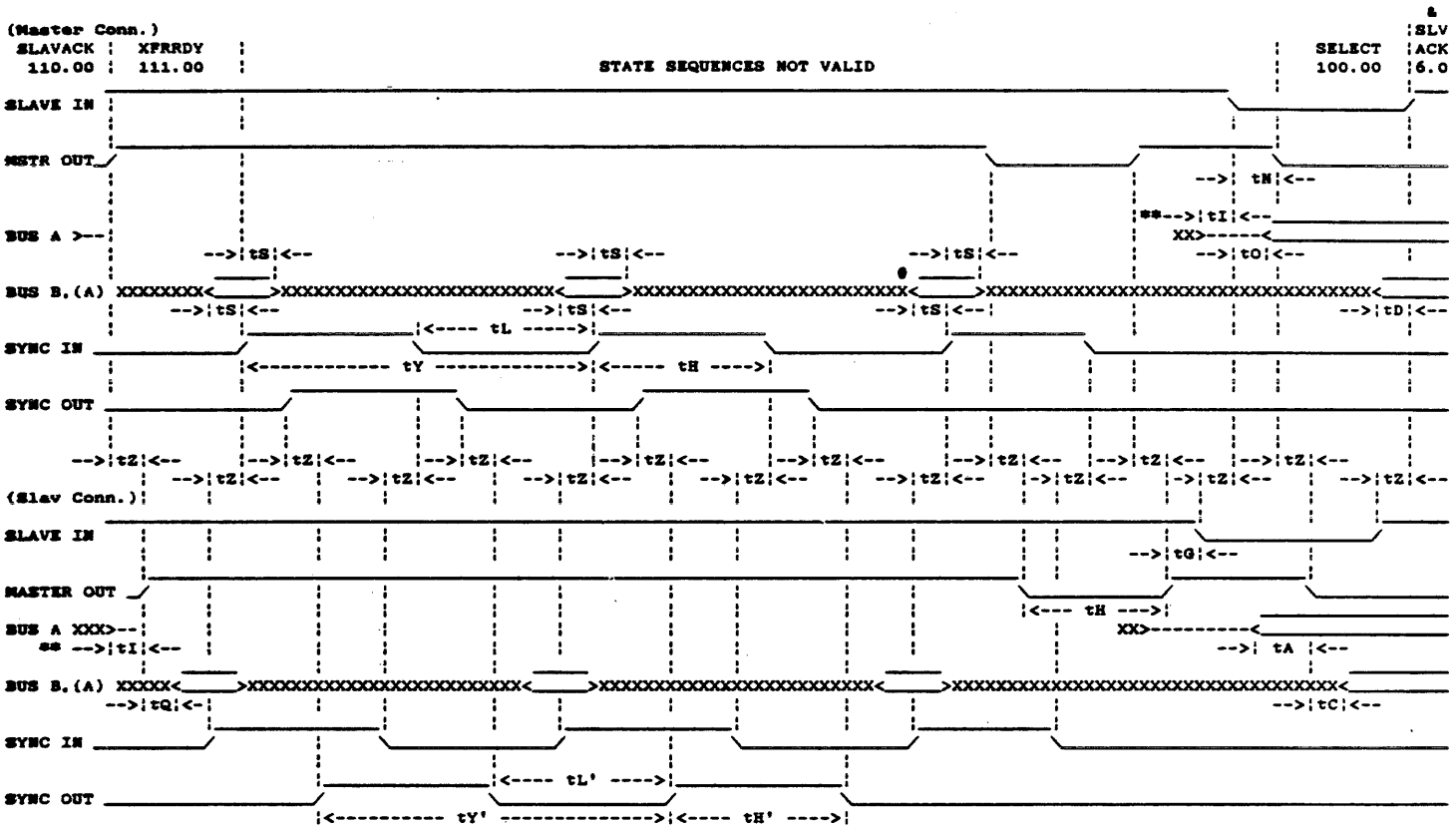
FIGURE 24A. DATA STREAMING INPUT TIMING SLAVE END



SELECT OUT = Active (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tH	SYNC IN pulse active	0.080	-	µs
tH'	SYNC OUT pulse active	0.064	-	µs
tI	Bus release set-up	0.025	-	µs
tL	SYNC IN pulse inactive	0.080	-	µs
tL'	SYNC OUT pulse inactive	0.064	-	µs
tO	Master turnaround	0	-	µs
tQ	Slave data turnaround	0	-	µs
tS	Stream. set-up/hold	0.030	-	µs
tW	Transfer bus release	0	-	µs
tY	SYNC IN period	0.200	-	µs
tY'	SYNC OUT period	0.200	-	µs
tZ	Cable delay	0	CMX	µs

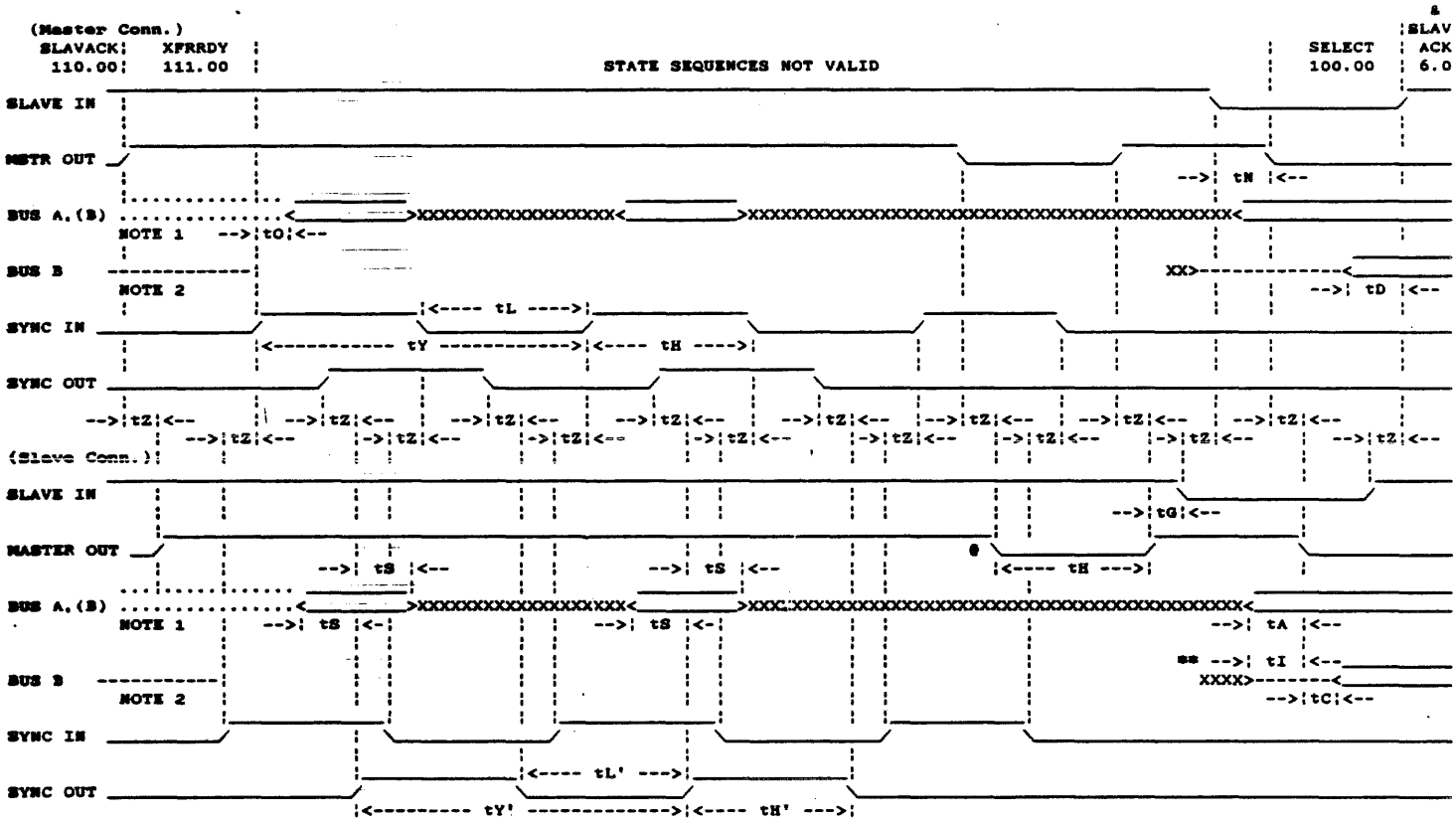
FIGURE 24B. DATA STREAMING OUTPUT TIMING SLAVE END



SELECT OUT = Active (Master and Slave Conn.) ** BUS A released in DOM only. @ The master latches the bus contents here.

Label	Description	Min.	Max.	Unit
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tH	SYNC IN pulse active	0.080	-	µs
tH'	SYNC OUT pulse active	0.064	-	µs
tL	SYNC IN pulse inactive	0.080	-	µs
tL'	SYNC OUT pulse inactive	0.064	-	µs
tI	Bus release set-up	0.025	-	µs
tN	Master interlock delay	0	-	µs
tO	Master turnaround	0	-	µs
tQ	Slave data turnaround	0	-	µs
tS	Stream. set-up/hold	0.030	-	µs
tY	SYNC IN period	0.200	-	µs
tY'	SYNC OUT period	0.200	-	µs
tZ	Cable delay	0	CMX	µs

FIGURE 24C. DATA STREAMING INPUT TIMING MASTER END



SELECT OUT = Active (Master and Slave Conn.) ** BUS B released in DOM only @ The slave does not latch the bus contents here.

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	µs
tC	Slave turnaround	0	SDE	µs
tD	Slave bus set-up	0.025	SDE	µs
tG	Slave interlock delay	0	SDE	µs
tH	SYNC IN pulse active	0.080	-	µs
tH'	SYNC OUT pulse active	0.064	-	µs
tI	Bus release set-up	0.025	-	µs
tL	SYNC IN pulse inactive	0.080	-	µs
tL	SYNC OUT pulse inactive	0.080	-	µs
tN	Master interlock delay	0	-	µs
tO	Master turnaround	0	-	µs
tS	Stream. set-up/hold	0.030	-	µs
tW	Transfer bus release	0	-	µs
tY	SYNC IN period	0.200	-	µs
tY'	SYNC OUT period	0.200	-	µs
tZ	Cable delay	0	CMX	µs

NOTE 1. The master may or may or may not be driving the buses.

NOTE 2. This represents the slaves drivers in DOM only.

FIGURE 24D. DATA STREAMING OUTPUT TIMING MASTER END

IPI CABLES AND CONNECTORS

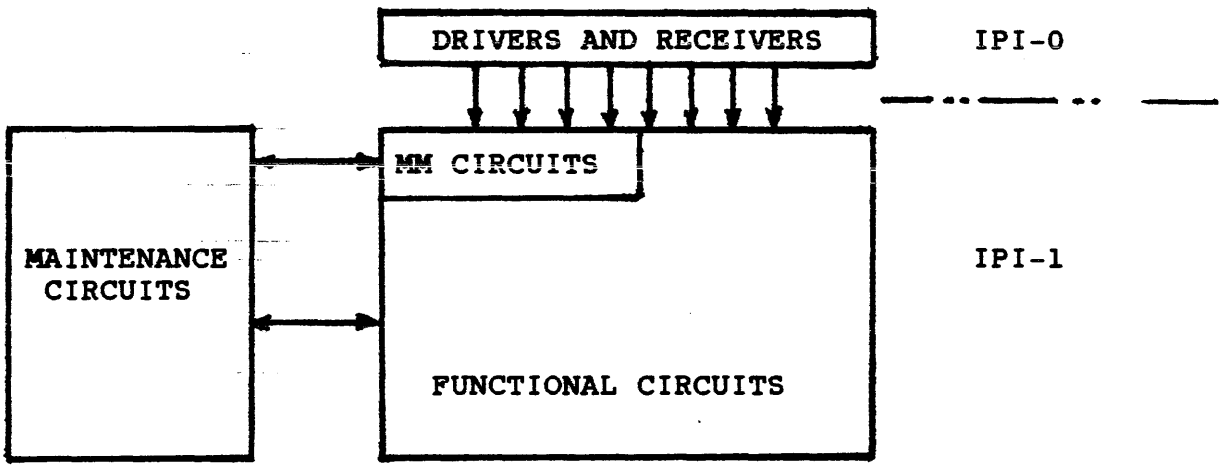
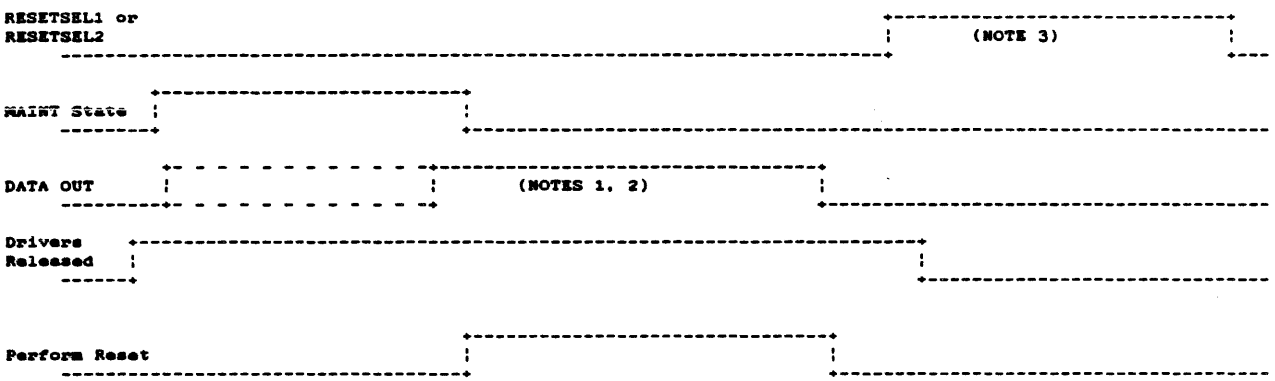


FIGURE 25. BLOCK DIAGRAM OF MAINTENANCE MODE



NOTE 1: For MM1 slaves if DATA OUT is active when the MAINT state is negated, a reset shall be generated that shall persist until DATA OUT is negated for a minimum of 10 microseconds. The drivers shall be left released if this situation occurs.

NOTE 2: For MM2 slaves, If DATA OUT and ENABLE OUT are active when the MAINT state is negated a reset shall be generated that shall persist until DATA OUT is negated. The Reset shall persist for a minimum of 10 microseconds. The drivers shall be left released if this situation occurred.

NOTE 3: The BUS A Selective Reset Control octet is assumed to contain the slave's address while the RESETSEL1 or RESETSEL2 state is active.

FIGURE 26. MAINTENAMCE MODE 1

TABLE 1. PIN ASSIGNMENTS

DIFFERENTIAL DRIVERS/RECEIVERS		CABLE TWISTED PAIR		CONNECTOR SUBMINIATURE D	
SIGNAL SOURCE	SIGNAL NAME	+	-	+	-
--	DC GND (SHIELD)	1	2	1	34
SLAVE	ATTENTION IN	9	10	20	4
MASTER	SYNC OUT	23	24	41	25
SLAVE	SLAVE IN	17	18	39	23
SLAVE	SYNC IN	43	44	15	48
MASTER	MASTER OUT	35	36	45	29
MASTER	SELECT OUT	29	30	43	27
SLAVE(MASTER)	BUS B - BIT 0	45	46	32	16
SLAVE(MASTER)	BUS B - BIT 1	47	48	49	33
SLAVE(MASTER)	BUS B - BIT 2	7	8	3	36
SLAVE(MASTER)	BUS B - BIT 3	19	20	7	40
SLAVE(MASTER)	BUS B - BIT 4	21	22	24	8
SLAVE(MASTER)	BUS B - BIT 5	25	26	9	42
SLAVE(MASTER)	BUS B - BIT 6	3	4	18	2
SLAVE(MASTER)	BUS B - BIT 7	5	6	35	19
SLAVE(MASTER)	BUS B - PARITY	49	50	17	50
MASTER(SLAVE)	BUS A - BIT 0	37	38	13	46
MASTER(SLAVE)	BUS A - BIT 1	39	40	30	14
MASTER(SLAVE)	BUS A - BIT 2	15	16	22	6
MASTER(SLAVE)	BUS A - BIT 3	27	28	26	10
MASTER(SLAVE)	BUS A - BIT 4	31	32	11	44
MASTER(SLAVE)	BUS A - BIT 5	33	34	28	12
MASTER(SLAVE)	BUS A - BIT 6	11	12	37	21
MASTER(SLAVE)	BUS A - BIT 7	13	14	5	38
MASTER(SLAVE)	BUS A - PARITY	41	42	47	31

TABLE 2. SIGNAL NOMENCLATURE

DEVICE LOGIC		INTERFACE		
TYPE OF DRIVER	VOLTAGE LEVEL	SIGNAL STATES	LOGICAL STATES	
			LOGICAL TRANSITION	LOGICAL CONDITION
DIFFERENTIAL	HIGH *	ACTIVE	ASSERT	1
	LOW *	INACTIVE	NEGATE	0
	RELEASED **	INACTIVE	DEGATE	0

* Odd pin relative to even pin
** Tri-state condition

TABLE 3. STATE DEFINITIONS

STATE OF SIGNAL						MNEMONIC
-0.0	0	0	0.0	0		IDLE
-0.1			.0	1		MAINT
-0.2			.1	0		*
-0.3			.1	1		MAINT
-1.0	0	0	1.0	0		REQUEST
-1.1			.0	1		RESETSEL1
-1.2			.1	0		*
-1.3			.1	1		*
-2.0	0	1	0.0	0		DESEL
-2.1			.0	1		MAINT
-2.2			.1	0		*
-2.3			.1	1		MAINT
-3.0	0	1	1.0	0		REQUACK
-3.1			.0	1		RESETSEL2
-3.2			.1	0		*
-3.3			.1	1		*
-4.0	1	0	0.0	0		SELECT
-4.1			.0	1		*
-4.2			.1	0		*
-4.3			.1	1		*
-5.0	1	0	1.0	0		SLAVEND
-5.1			.0	1		*
-5.2			.1	0		*
-5.3			.1	1		*
-6.0	1	1	0.0	0		SLAVACK
-6.1			.0	1		BUSCTL
-6.2			.1	0		MASTEND
-6.3			.1	1		BUSACK
-7.0	1	1	1.0	0		XFRRDY
-7.1			.0	1		XFREND
-7.2			.1	0		XFRST
-7.3			.1	1		XFRRES
	|	|	|	|	|		
	|	|	|	|	|		
	|	|	|	|	SYNC OUT		
	|	|	SYNC IN				
	|	MASTER OUT					
	SLAVE IN						
SELECT OUT							

* Undefined states which shall initiate exception handling

TABLE 4A. INTERFACE STATES

The following abbreviations and those of 7.2 are used in this table:

*	Bus Undefined (not necessarily released)
/	or
BUSACK	Bus Acknowledge Octet
BUSCTL	Bus Control Octet
DOM	Double Octet Mode
MASTER REL	Master releases bus
MSTR STATUS	Master Status Octet
ADDRESS	Address Octet (bit significant)
SELECT STAT	Select Status Octet (bit significant)
REQ/SEL/SET	Request Modifier Octet or Selective Reset Control Octet or Request Transfer Settings Octet
SAME PREC	Same contents as in preceding transition
SELECT OCT	BUS A Selection Octet
SEL RESET	Selective Reset Control Octet
SLAVE REL	Slave releases bus
SLAVE STAT	Slave Status Octet
SOM	Single Octet Mode
XFR SET	Transfer Settings Octet

FROM STATE	TO STATE	XFR	BUS A	BUS B	ASSERT	NEGATE
IDLE	IDLE		RELEASED/ MASTER REL	RELEASED/ SLAVE REL		
SELECT	IDLE		SELECT OCT	RELEASED		
DESEL	IDLE		RELEASED	RELEASED		SLAVE IN
REQUEST	IDLE		REQ/SEL/SET	ADDRESS		MASTER OUT
MAINT	IDLE		RELEASED	RELEASED		SYNC OUT
MAINT	MAIN		RELEASED	SLAVE REL		
ANY STATE	MAIN		RELEASED	*	SYNC OUT	
						SELECT OUT
						MASTER OUT
REQUEST	REQUEST		REQ/SEL/SET	ADDRESS/*		
IDLE	REQUEST		REQ/SEL/SET	RELEASED	MASTER OUT	
RESETSEL1	REQUEST		SEL RESET	*		SYNC OUT

(CONT.)

TABLE 4B. INTERFACE STATES

FROM STATE	TO STATE	XFR	BUS A	BUS B	ASSERT	NEGATE
RESETSEL1	RESETSEL1		SEL RESET	*		
REQUEST	RESETSEL1		SEL RESET	*	SYNC OUT	
RESETSEL2	RESETSEL1		SEL RESET	*		SLAVE IN
REQUACK	REQUACK		REQ/SEL/SET	ADDRESS/ XFR SET		
REQUEST	REQUACK		REQ/SEL/SET	ADDRESS/ XFR SET	SLAVE IN	
RESETSEL2	RESETSEL2		SEL RESET	*		
REQUACK	RESETSEL2		SEL RESET	ADDRESS/ XFR SET	SYNC OUT	
DESEL	DESEL		MASTER REL	SLAVE REL		
REQUACK	DESEL		REQ/SEL/SET	ADDRESS/ XFR SET		MASTER OUT
SLAVACK	DESEL		*	SAME PREC		SELECT OUT
SELECT	SELECT		SAME PREC	*		
IDLE	SELECT		SELECT OCT	RELEASED	SELECT OUT	
SLAVEND	SELECT	IN	MSTR STATUS	*		MASTER OUT
SLAVEND	SELECT	OUT	MSTR STATUS	MASTER REL DOM		MASTER OUT
SLAVEND	SLAVEND	IN	RELEASED DOM	*		
SLAVEND	SLAVEND	OUT	*	*		
XFRRDY	SLAVEND	IN	SLAVE REL DOM	*		SLAVE IN
XFRRDY	SLAVEND	OUT	*	*		SLAVE IN
SLAVACK	SLAVACK		SAME PREC/*	SAME PREC		

(CONT.)

TABLE 4C. INTERFACE STATES

FROM STATE	TO STATE	XFR	BUS A	BUS B	ASSERT	NEGATE
SELECT	SLAVACK		SAME PREC	SELECT STAT /SLAVE STAT	SLAVE IN	
MASTEND	SLAVACK		*	SLAVE REL DOM/*		SYNC IN
BUSCTL	BUSCTL		BUSCTL	*		
SLAVACK	BUSCTL		BUSCTL	SAME PREC	SYNC OUT	
BUSACK	BUSACK		*	BUSACK		
BUSCTL	BUSACK		BUSCTL	BUSACK	SYNC IN	
XFRRDY	XFRRDY		*	*		
SLAVACK	XFRRDY	IN	MASTER REL DOM/*	*	MASTER OUT	
SLAVACK	XFRRDY	OUT	*	*	MASTER OUT	
XFREND	XFRRDY		*	*		SYNC OUT
XFRST	XFRST	IN	IN DOM	IN SOM		
XFRST	XFRST	OUT	*	*		
XFRRDY	XFRST	IN	IN DOM	IN SOM	SYNC IN	
XFRRDY	XFRST	OUT	*	*	SYNC IN	
XFRRES	XFRRES	IN	*	*		
XFRRES	XFRRES	OUT	OUT SOM	OUT DOM		
XFRST	XFRRES	IN	IN DOM	IN SOM	SYNC OUT	
XFRST	XFRRES	OUT	OUT SOM	OUT DOM	SYNC OUT	
XFREND	XFREND		*	*		
XFRRES	XFREND	IN	*	*		SYNC IN
XFRRES	XFREND	OUT	OUT SOM	OUT DOM		SYNC IN
MASTEND	MASTEND		*	*		
BUSACK	MASTEND		*	BUSACK		SYNC OUT
XFRST	MASTEND	IN	IN DOM	IN SOM		MASTER OUT
XFRST	MASTEND	OUT	*	*		MASTER OUT

TABLE 5. FACILITY ADDRESS MAPPING

BUS B BIT	RANGE 0-7 ADDRESSES	RANGE 8-F ADDRESSES
7	ADDRESS 7	ADDRESS F
6	" 6	" E
5	" 5	" D
4	" 4	" C
3	" 3	" B
2	" 2	" A
1	" 1	" 9
0	" 0	" 8

TABLE 6. MM1 SCENARIO SUMMARY

MAINTENANCE MODE 1	MASTER ACTION	SLAVE ACTION
FIRST PHASE	Enter MAINT State	Upon recognition of MAINT state the MM1 slave shall release the interface drivers
SECOND PHASE	Assert the DATA OUT (and ENABLE OUT) signals and then enter IDLE state	If DATA OUT is active when SYNC OUT is negated a reset shall be activated
THIRD PHASE	Negate the DATA OUT (and ENABLE OUT) to enter RESETSEL1 and attempt communication with a specific slave	When the DATA OUT signal is negated the reset shall be deactivated. The interface drivers shall be left released until RESETSEL1 is entered. Upon recognition of RESETSEL1 the slave shall re-activate its drivers

TABLE 7. MM SIGNAL LINE ASSIGNMENTS

LINE NAME	MM1 USAGE
SELECT OUT (0) SLAVE IN (x) MASTER OUT (0) SYNC IN (x) SYNC OUT (1)	MAINT state (0x0.x1) invokes MM circuits
BUS B (bit 7) BUS B (bit 6) BUS B (bit 5) BUS B (bit 4) BUS B (bit 3) BUS B (bit 2) BUS B (bit 1) BUS B (bit 0) BUS B Parity	not used not used not used not used not used not used not used not used not used
BUS A (bit 7) BUS A (bit 6) BUS A (bit 5) BUS A (bit 4) BUS A (bit 3) BUS A (bit 2) BUS A (bit 1) BUS A (bit 0) BUS A Parity	DATA OUT (bit 2) ENABLE OUT (bit 2)* not used DATA OUT (bit 1) ENABLE OUT (bit 1)* not used DATA OUT (bit 0) ENABLE OUT (bit 0)* not used

* An MM1 Master must use both ENABLE OUT and DATA OUT to reset and release any attached MM2 slaves.