CONTROL DATA® 6638
DISK FILE SYSTEM

6639 DISK FILE CONTROLLER

DIAGRAMS &
CIRCUIT DESCRIPTIONS
MAINTENANCE
PARTS LIST
CARD PLACEMENT
WIRE LISTS
CHASSIS TABS

CONTROL DATA CORPORATION

CUSTOMER ENGINEERING MANUAL

60196300

RECORD of REVISIONS

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FOREWORD

Logic diagrams contained in this manual do not attempt to show the entire device. The purpose of the diagrams is to show the logical significance of circuits that may involve parts of many modules. The logic diagrams do not replace the chassis tabs, but they are a valuable tool in understanding the tabs and the overall operation of the controller.

PART 1

DIAGRAMS AND CIRCUIT DESCRIPTION

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA* logic, two signals, a logical "0" and a logical "1" are the possible input or output conditions of a circuit. For example, "1" is considered "up" and "0" is considered "down" on a timing chart. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for Control Data equipment using 6000 Series card types are inverters, test points, flip-flops, twisted pair line drivers, and coaxial cable line drivers.

Inverters

An inverter is a logic element which provides an output that is a negation of its input. When more than one input is provided to an inverter, "0's" take precedence over "1's" and therefore drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. The basic inverter is shown in the logic diagrams as an arrow into either a circle or a square (Figure 1). Both symbols represent the same electronic circuit and have the same logic interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain.

Figure 1. Inverter Symbols

Certain card types employ variations of the standard inverter building block. These differences are indicated in the logic diagrams by a dot or a cross in the circle or square (Figure 2). Both the chassis tabs containing the card in question and the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700) contain electronic schematics of these special variations.

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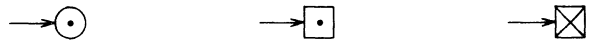


Figure 2. Special Inverters

Acceptable conventions for showing multiple inputs and outputs are given in Figure 3. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.

Figure 3. Multiple Inputs/Outputs

Acceptable conventions for showing inverter networks are illustrated in Figure 4. As a general rule, circle inverters alternate with square inverters wherever possible. Because multiple outputs are identical, only one arrow is shown in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D; in this case because B is not the only input to C or D).

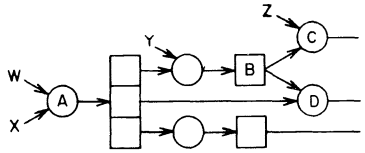


Figure 4. Inverter Networks

Test Points

A test point has no logic function, but is shown in the logic diagrams as a triangle (Figure 5). They are numbered from 1 to 6.

Figure 5. Test Point Symbols

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states--designated as Set and Clear--and is composed of two inverters (Figure 6). The flip-flop is said to be set when the set output (B) is a "1", and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop and (C) must be "0" to clear it.

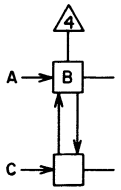


Figure 6. Flip-Flop Symbol

Logic signals are transmitted from one module to another by means of a line driver. Modules on the same chassis are connected with twisted pair lines, and those on separate chassis are connected by coaxial cable.

Twisted Pair Drivers

The twisted pair driver is represented by the standard square or circle. The output of the square or circle, however, is connected to a pin of the module in question and wired from there to a pin on another module (Figure 7). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28 (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams). The module location is shown above the card, and the module type is denoted in the upper right corner.

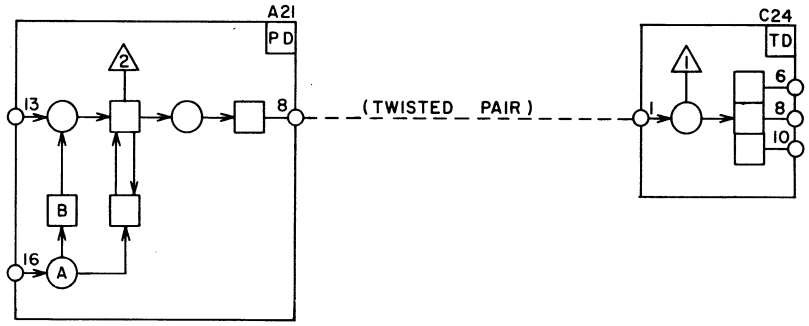


Figure 7. Twisted Pair Line Driver

Coaxial Cable Drivers

The coaxial cable driver is a 25 nsec pulse circuit, and is represented as shown in Figure 8. The pins used are represented by a small double circle.

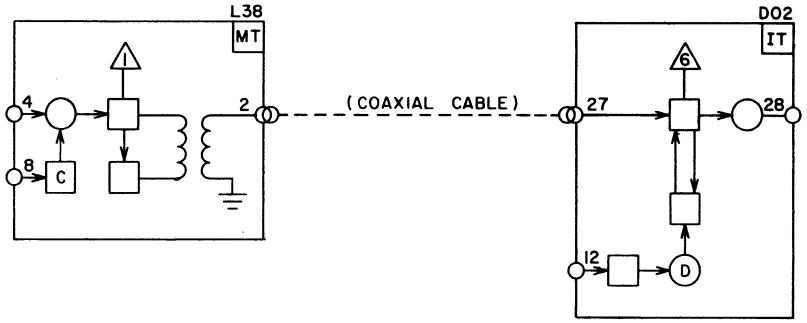


Figure 8. Coaxial Cable Driver

3000 Series Interface Modules

These modules convert 3000 Series logic voltage levels to cordwood module logic levels. In Figure 9, the crossed wire representation shows that both wires in a twisted pair line are used. The transmitter/receiver modules are used for bidirectional signals. The others are for unidirectional signals. Electrical schematics appear in the chassis tabs.

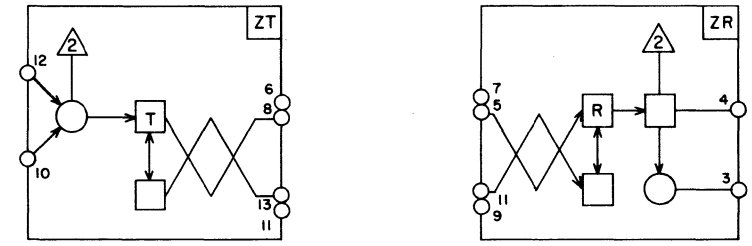


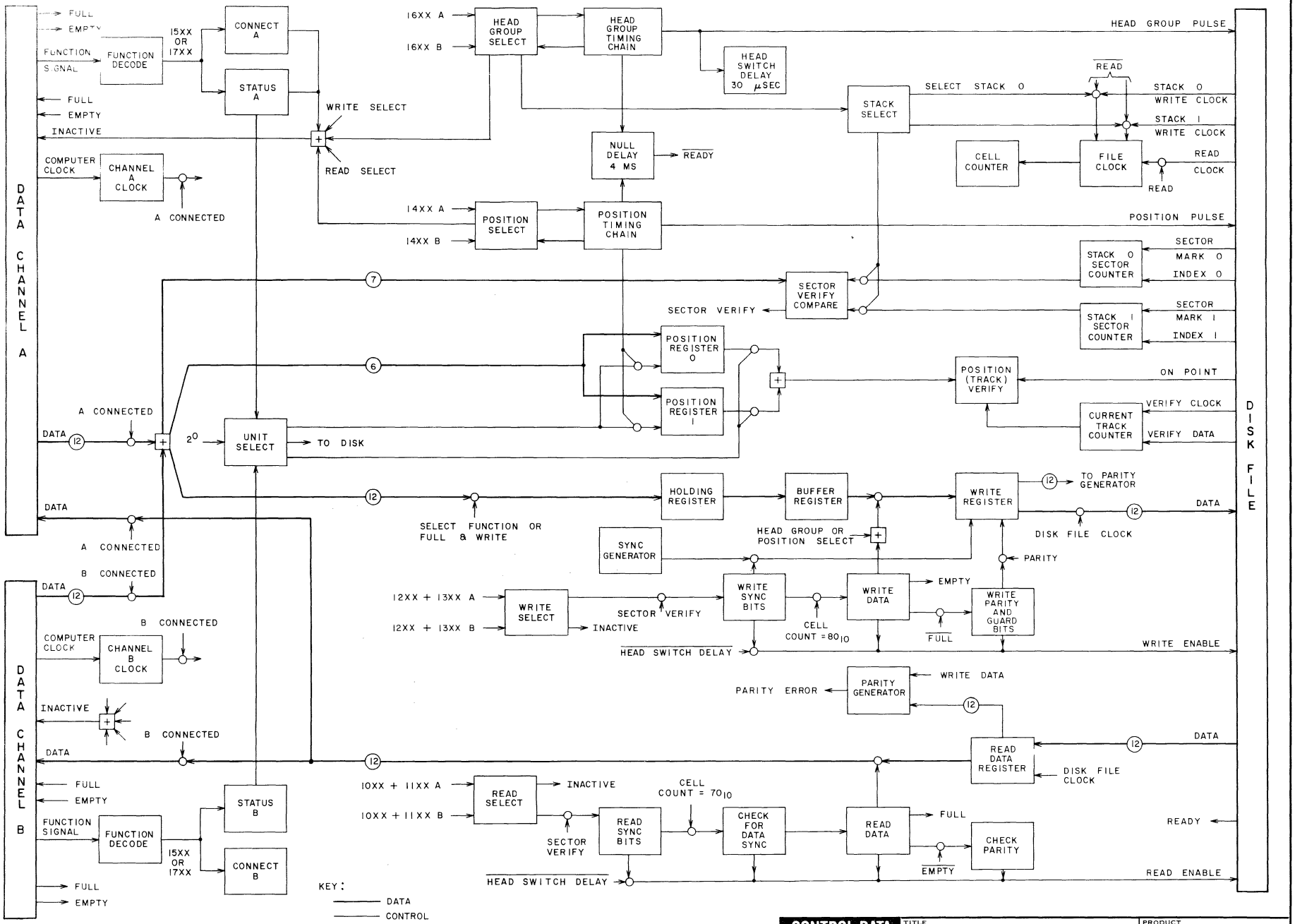
Figure 9. 3000 Series Interface Modules

The controller buffers data in a 12-bit parallel format between the computer and disk file via the Data Channel. A 12-bit function code conditions the controller to connect to the disk file and designates a location on the disk from which data is to be transferred thus initiating an I/O operation.

The Data Channel issues an output word to the controller. If the output word is accompanied by a function signal, the controller defines it as a function code. Otherwise, the controller recognizes it as a data word. When the controller accepts a function word, it returns an Inactive signal to the Data Channel. The five function codes are 1) Connect and Status, 2) Position Select, 3) Head Group Select, 4) Read, and 5) Write. The Connect code designates a disk file unit in which an I/O operation will be performed. A status response check can be performed to determine the state of conditions within the controller. The Position Select function causes the disk file access mechanism (positioner) to move to one of 32 positions. The Position Select function provides a position address which the controller compares against a Position code from the disk file to verify that the access mechanism is positioned correctly. The Head Group Select function selects one of 32 head groups to correspond with the position selected.

If the function is a Read, the Active signal, sent with the Read code, requests the controller to send data. The controller sends a data word and a Full signal. The Data Channel then returns an Empty signal, causing the controller to send the next word. Operations continue in this way until the end of the read buffer.

On a Write operation, the Full signal, sent with the Write code, signals the controller that the Data Channel is ready to start sending data. The controller acknowledges the data word by returning an Empty signal, causing the Data Channel to send the next data word. Operation continues in this way until the end of the write buffer.

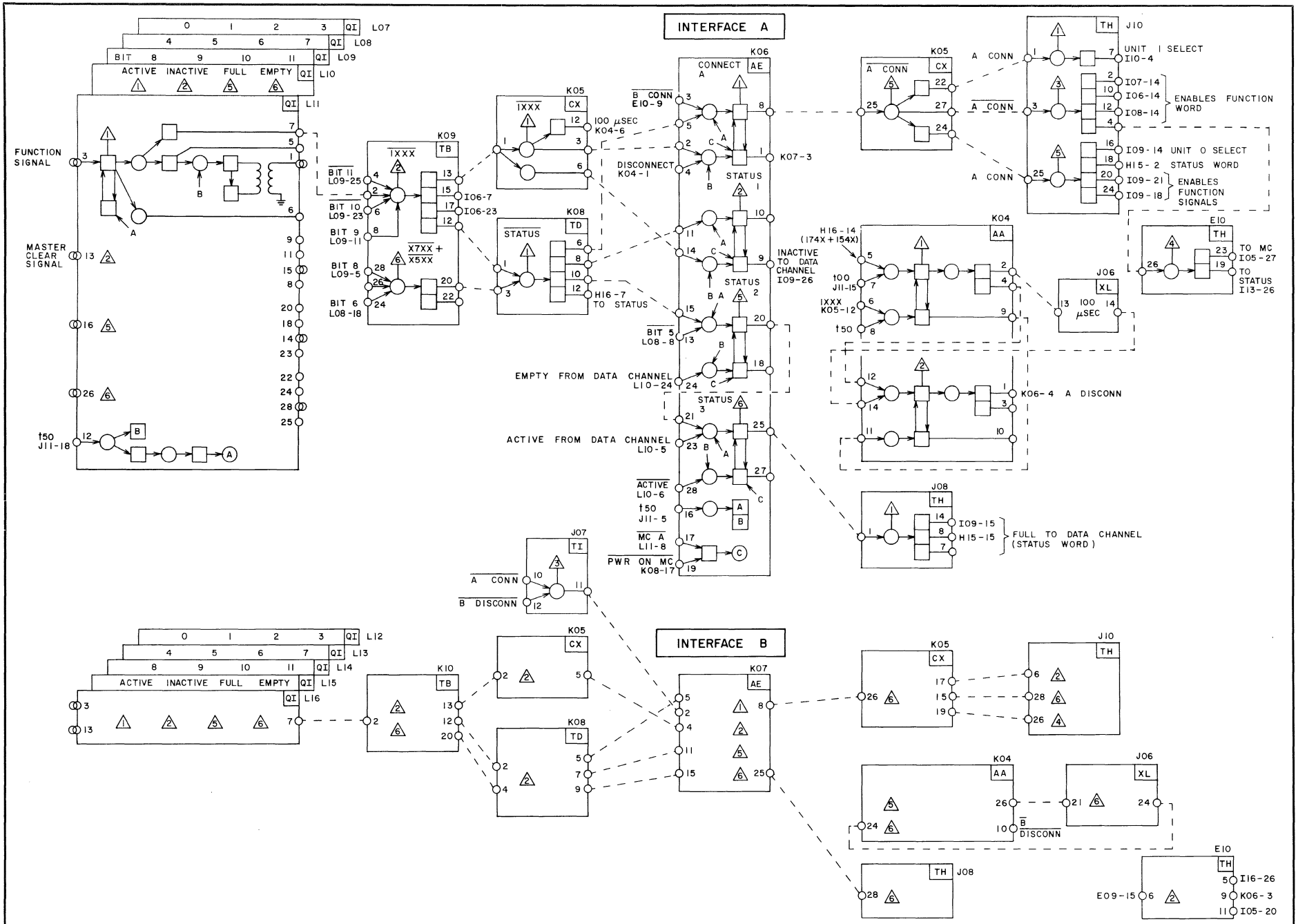


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER BLOCK DIAGRAM	PRODUCT 6639	
		SIZE C	DRAWING NO 60196300
		REV. A	
		SHEET	PAGE 1-1

This logic provides for receiving signals and data from the Data Channel for transmission to the disk file. Interfaces A and B provide for connecting the controller to Data Channels A and B, respectively. If the Connect and Status function word is received through Interface A, it sets the Connect A FF which provides various enables for transmitting the status word, data, and function signals through the controller during operation. The controller connects to Data Channel A if Channel B is not connected and vice versa. If Channels A and B attempt to connect simultaneously, the controller gives priority to Channel A.

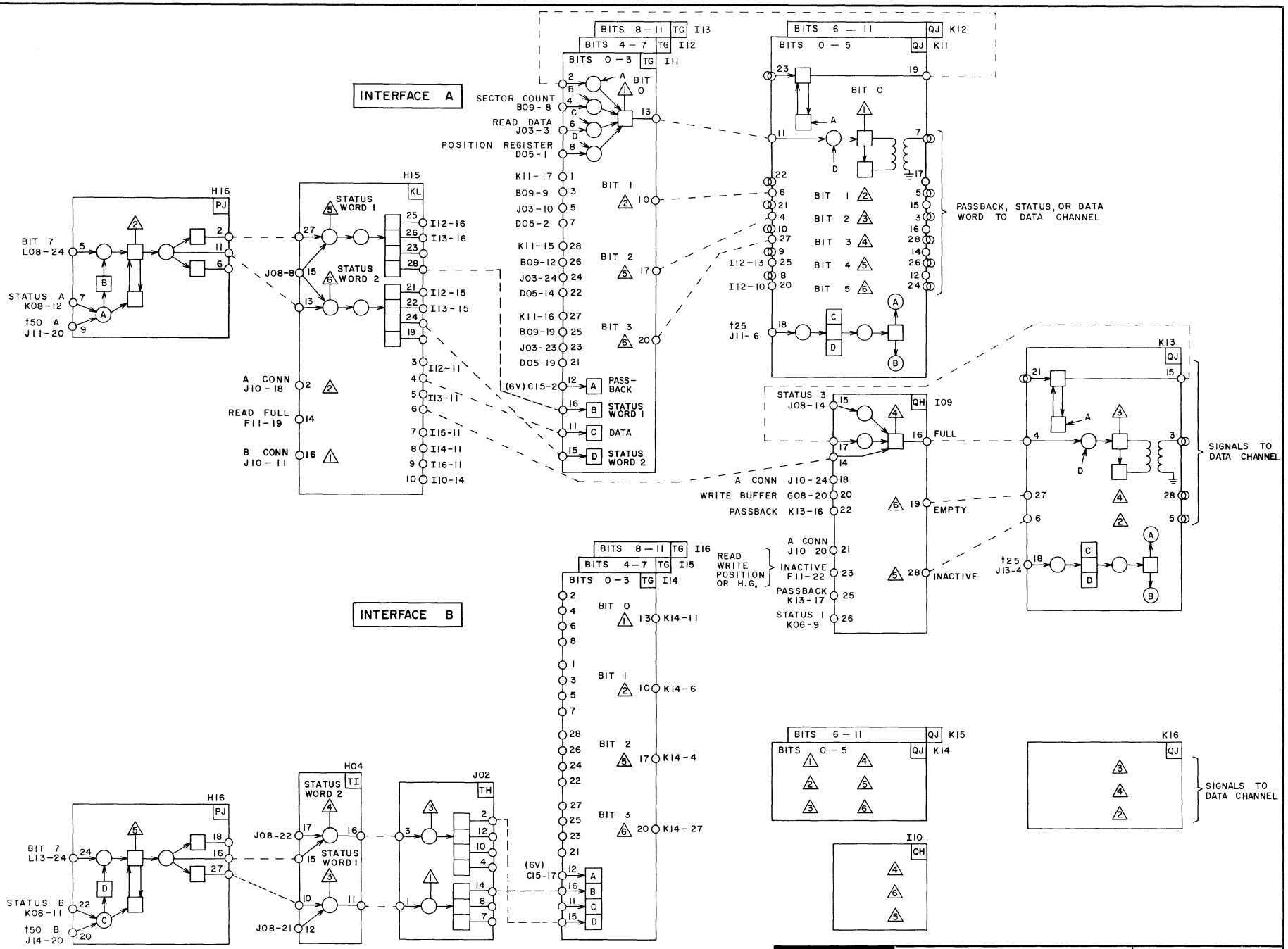
Receiving the Connect and Status function word and function signal causes the controller to set the Status 1 FF. This causes the controller to return an Inactive signal to the Data Channel, indicating acceptance of the function word. It also sets the Status 2 FF which, together with the Active signal from the Data Channel, sets the Status 3 FF. Setting the Status 3 FF enables the status word (and Full signal) to the Data Channel.

A function code of 1740 or 1540 will disconnect the controller from the Data Channel approximately 100 microseconds after a function instruction is received.


INTERFACE A
INTERFACE B
FUNCTION SIGNAL
MASTER CLEAR SIGNAL
ACTIVE INACTIVE FULL EMPTY
BIT 8 9 10 11
CONNECT A
STATUS 1
STATUS 2
STATUS 3
DISCONNECT K04-1
INACTIVE TO DATA CHANNEL I09-26
EMPTY FROM DATA CHANNEL L10-24
ACTIVE FROM DATA CHANNEL L10-5
PWR ON MC K08-17
UNIT I SELECT I10-4
ENABLES FUNCTION WORD
I09-14 UNIT 0 SELECT
H15-2 STATUS WORD
ENABLES FUNCTION SIGNALS
TO MC I05-27
TO STATUS I13-26
K06-4 A DISCONN
FULL TO DATA CHANNEL (STATUS WORD)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
CONTROLLER CONNECT AND STATUS
6639
C 60196300
REV. A
SHEET
PAGE 1-3

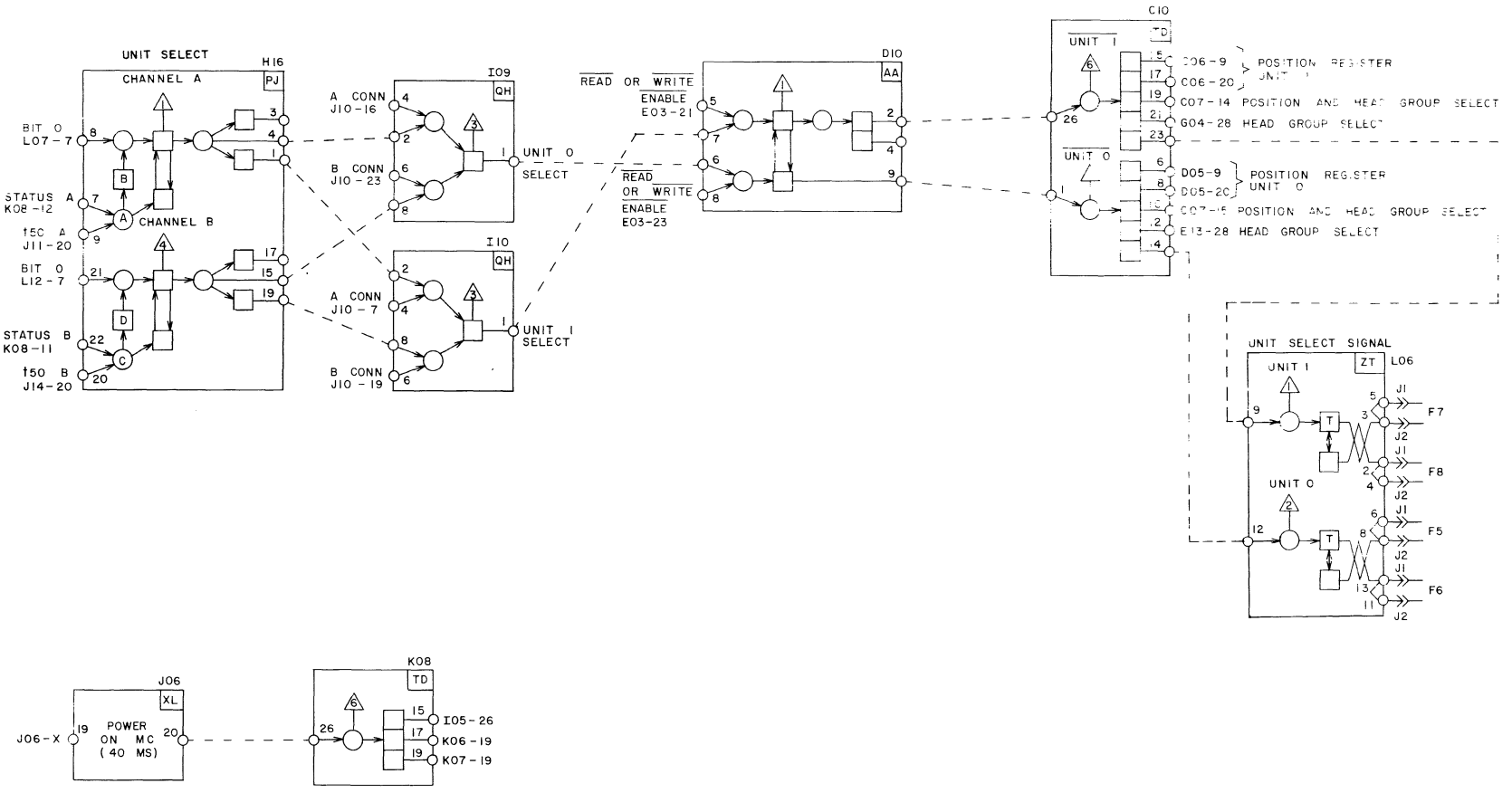
Bit 7 (17XX) of the Connect and Status function word is sampled to determine which of two status word formats the Data Channel is requesting. If bit 7 is a "1", the controller responds with the first format which provides indications of internal conditions within the disk file and the controller. If bit 7 (15XX) is a "0", the controller responds with the second format which provides the last position address issued to the disk file units.

Also, this logic indicates Fan-In circuits for data and for status words 1 and 2. It shows the transmitter cards for Passback, Status, and Data signals.



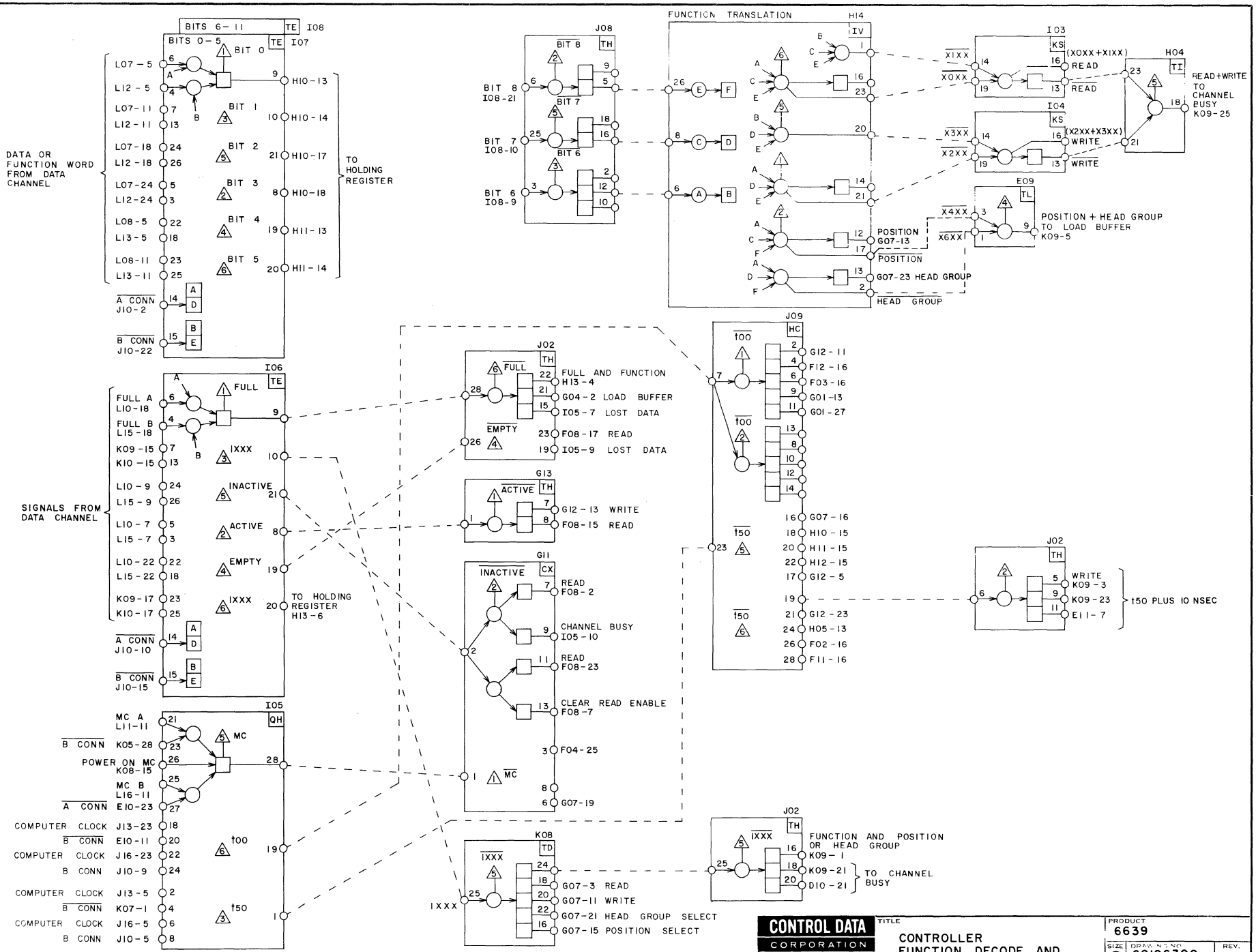
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER STATUS, GATES OUT TO CHANNEL	PRODUCT 6639 SIZE C · DRAWING NO. 60196300 · REV. A SHEET · PAGE 1-5	

Bit 0 of the Connect and Status function word is sampled to determine if disk file unit 0 or 1 is to be selected for operation. If bit 0 is a "0", unit 0 is selected. If bit 0 is a "1", unit 1 is selected. Selection of a disk file unit also provides enables for the Position Select and Head Group Select functions which will be performed on that unit. Unit selection is not permitted to be changed until Read or Write operations are completed.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER UNIT SELECT	PROJECT 6639	
		SIZE C	DRAWING NO. 60196300 REV. A
		SHEET	PAGE 1-7

Function words from the Data Channel are transmitted to the Holding Register and are also translated to initiate a Read, Write, Position Select, or Head Group Select. A Read or Write causes a Channel Busy condition prior to an I/O operation. A Position Select or Head Group Select function causes the position address or head group number to be gated to the Buffer register for transfer to the disk file. Inactive, Active, Full, and Empty signals sent by the Data Channel are distributed here to enable various controller operations. The function signal is fanned out to the position select, head group select, read, and write logic to enable the function being selected.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

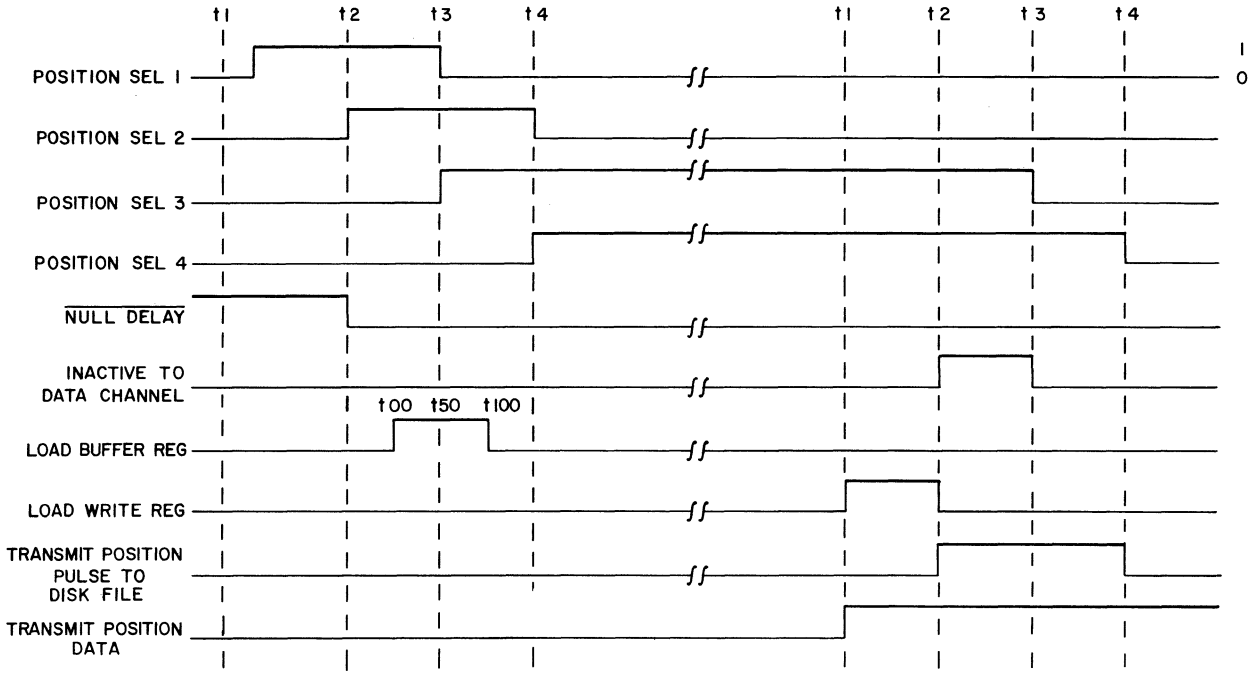
TITLE
CONTROLLER FUNCTION DECODE AND GATES IN FROM CHANNELS

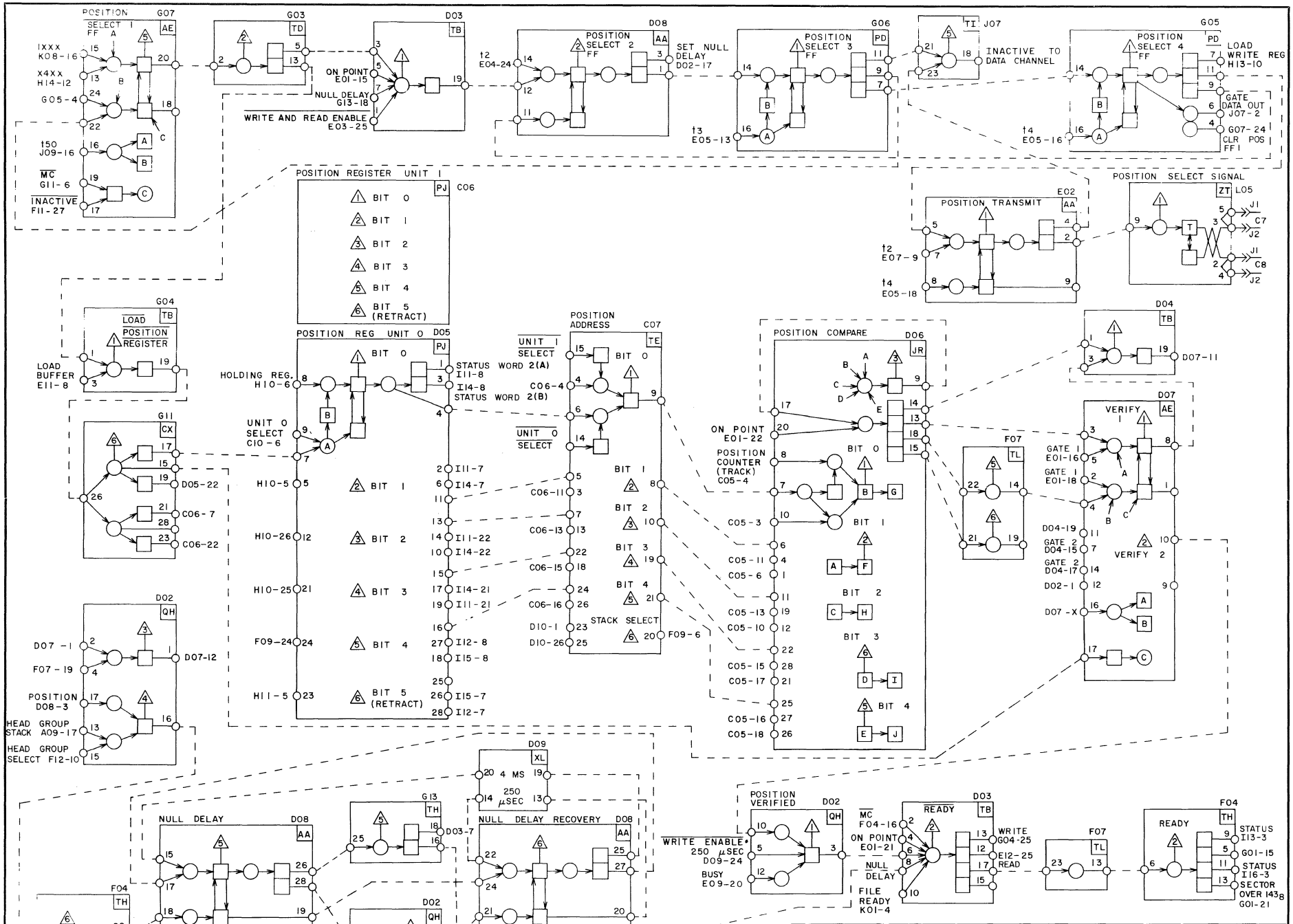
PRODUCT 6639
SIZE C | DRAW. NO. 60196300 | REV. A
SHEET | PAGE 1-9

The Position Select function word activates the position select logic and provides a position address for selecting one of 32 positions in the disk file. An Inactive signal is sent to the Data Channel which indicates acceptance of the Position Select function word by the controller. The address is fed through the Holding register (page 1-19), Buffer register, Write register and sent to the disk file. The address is also gated to the Position register unit 0 and 1 (as selected by the Connect and Status function code) for comparison against a Position code from the disk file. Two successive valid comparisons are necessary to set the Verify 1 and Verify 2 FFs, respectively, and to verify the new position.

Since it takes a comparatively long time (4 milliseconds) for the positioner mechanism to move from the old on point, a Null Delay circuit is provided to force a Not Ready condition for at least 4 milliseconds after the position is issued. This provides time for the positioner to become off point with respect to the original position. Otherwise, the controller could possibly output a Ready based on the previous on point, causing an I/O operation to begin before the positioning mechanism had begun to move.

POSITION SELECT TIMING



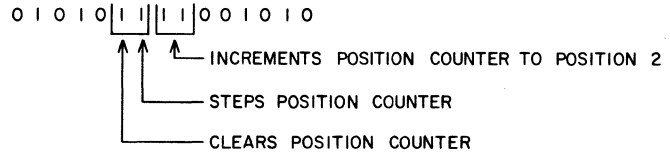


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER POSITION SELECT, POSITION VERIFY 1, NULL DELAY, AND READY	PRODUCT 6639 SIZE C DRAWING NO. 60196300 REV. A SHEET PAGE 1-11	

Position codes which have been prerecorded on separate tracks for each of the 32 positions in a disk file unit are translated to determine that the read/write heads are positioned properly on the disks. Each track contains one Position code which is repeated every 64 bits around the track. The Position codes are received in nonreturn to zero (NRZ) data. Examples of the first five Position codes are as follows:

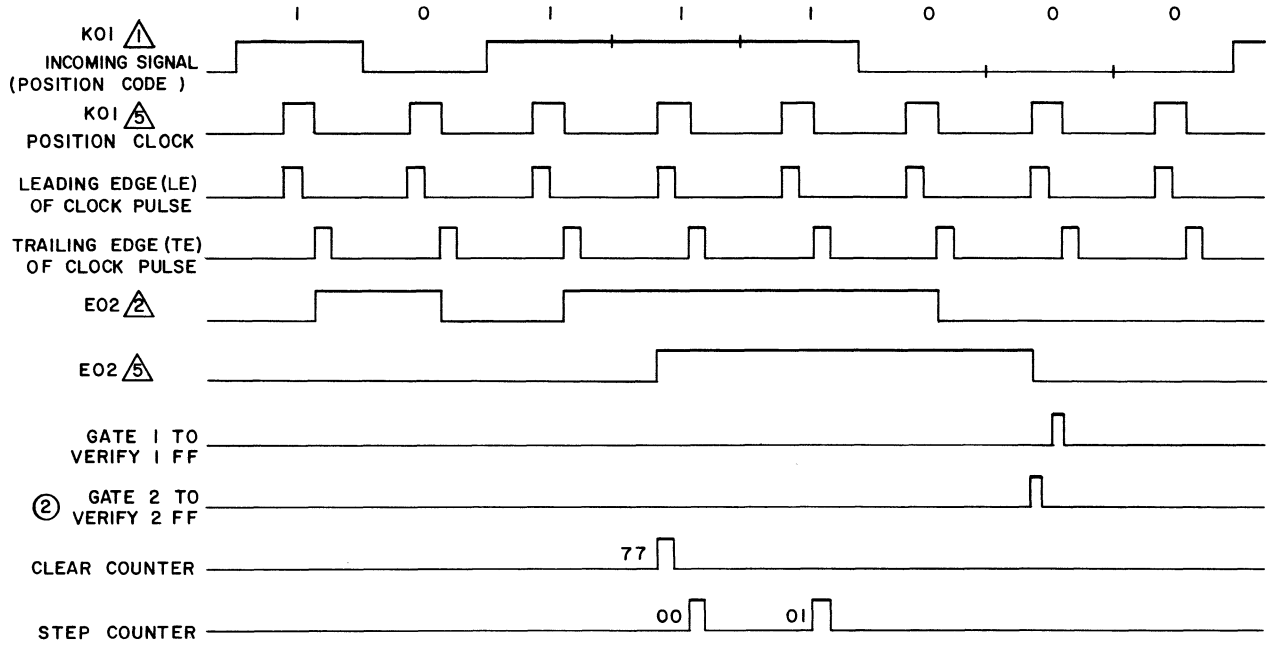
POSITION	DATA PATTERN
0	0 1 0 1 0 1 1 | 0 | 0 1 0 1 0 1 0
1	0 1 0 1 0 1 1 | 1 | 0 0 0 1 0 1 0
2	0 1 0 1 0 1 1 | 1 1 | 0 0 1 0 1 0
3	0 1 0 1 0 1 1 | 1 1 1 | 0 0 0 1 0
4	0 1 0 1 0 1 1 | 1 1 1 1 | 0 0 1 0

Position-Clock pulses derived from the Position code tracks are used to gate Position code data to the Position counter. The Position-Clock pulses provide Leading Edge (LE) and Trailing Edge (TE) pulses which gate the Position code data through the logic, causing the Position counter to be stopped if the proper bit combination of Position code data is present. An example of the bit combination for position 2 is as follows:



To increment the Position counter, two or more "1" bits in succession are required. In addition to the Position code data and the Position-Clock pulses, File Ready and On Point signals from the disk file are gated in for transfer to other logic circuits.

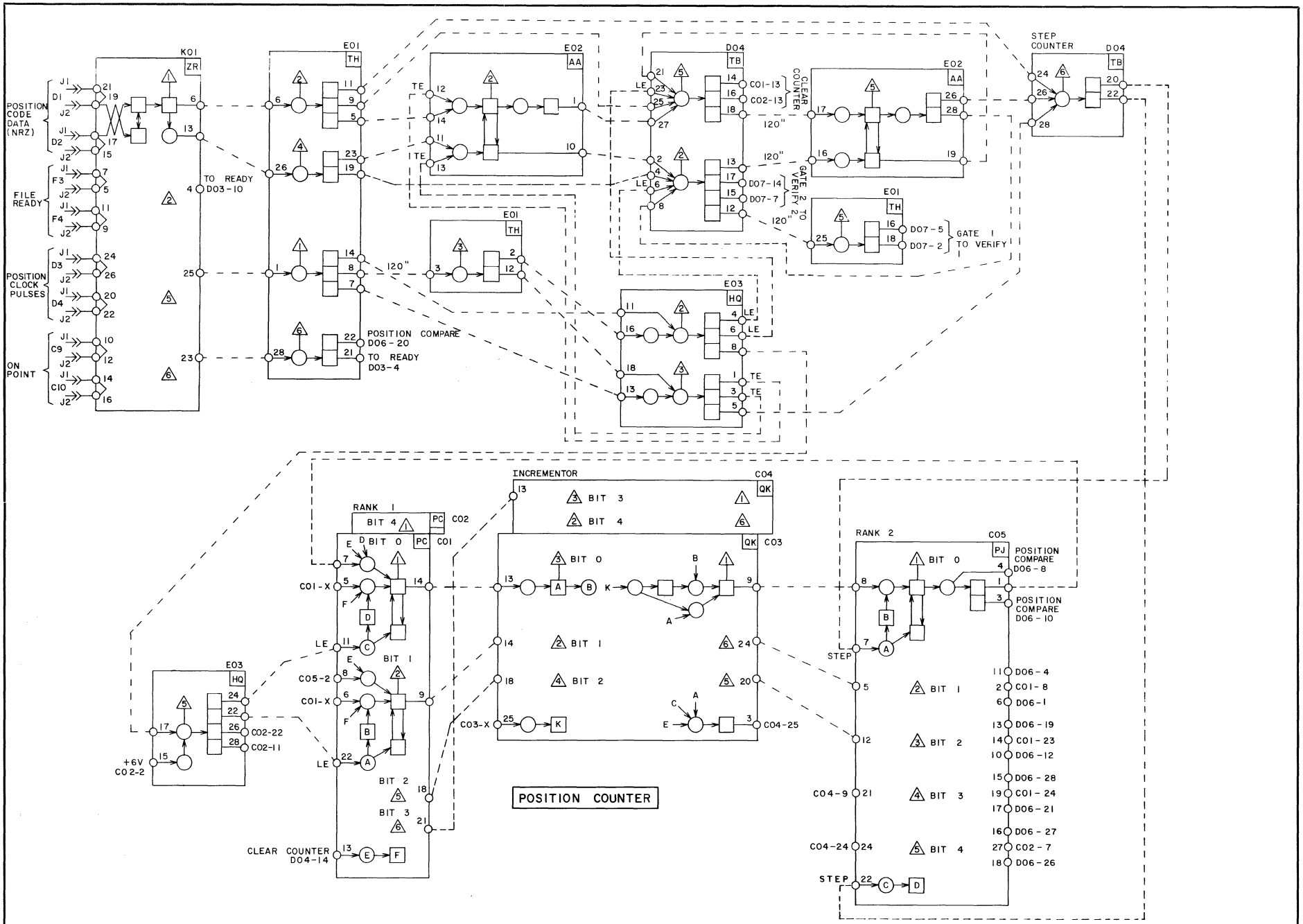
POSITION VERIFICATION ①



NOTES:

① POSITION VERIFICATION ON TRACK 1 IS SHOWN. THREE "1" BITS IN SUCCESSION SIGNIFY TRACK 1.

② AN ON-POINT AND TWO VERIFIES ARE NEEDED TO SET THE VERIFY 2 FF.



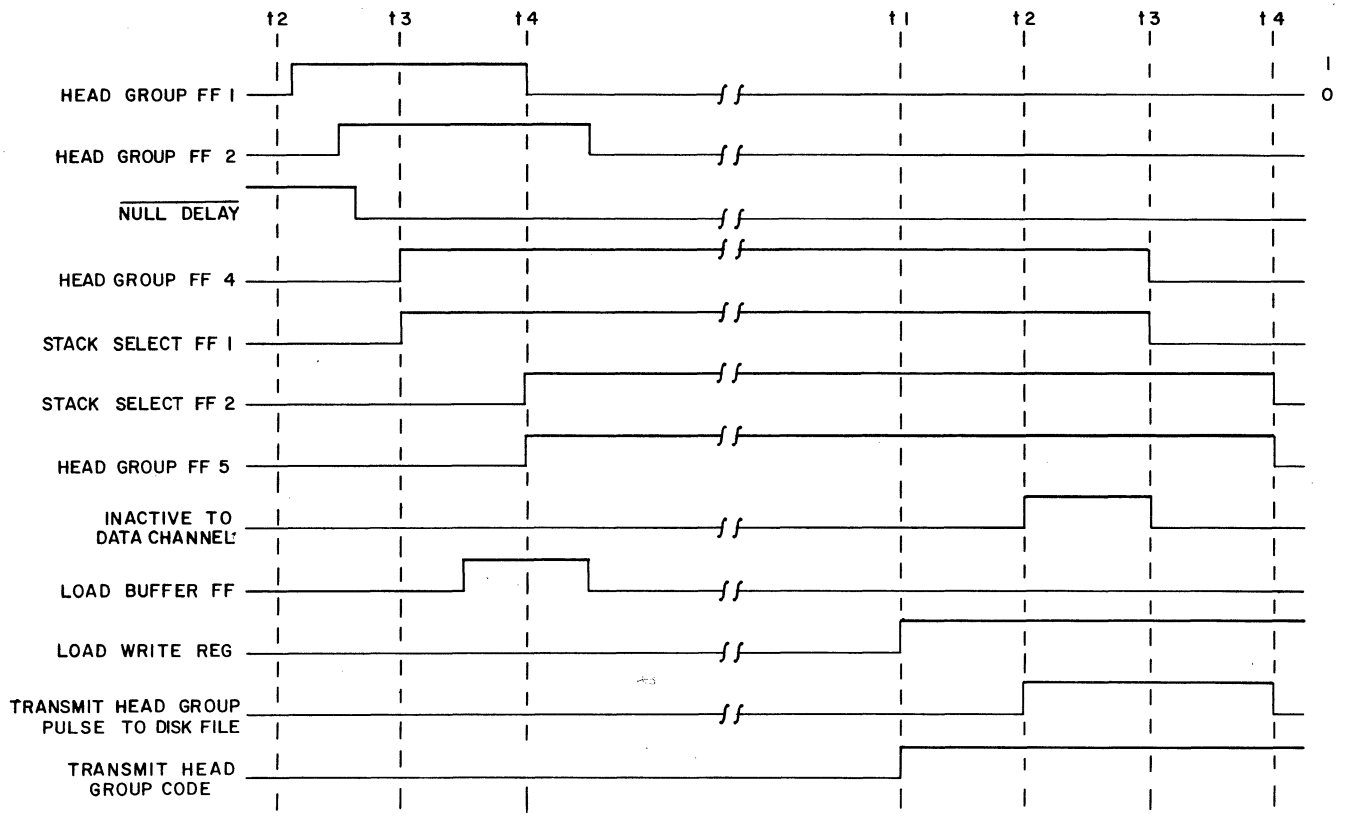
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER POSITION VERIFY 2	PRODUCT 6639	
		SIZE C	DRAWING NO. 60196300 REV. A
		SHEET	PAGE 1-13

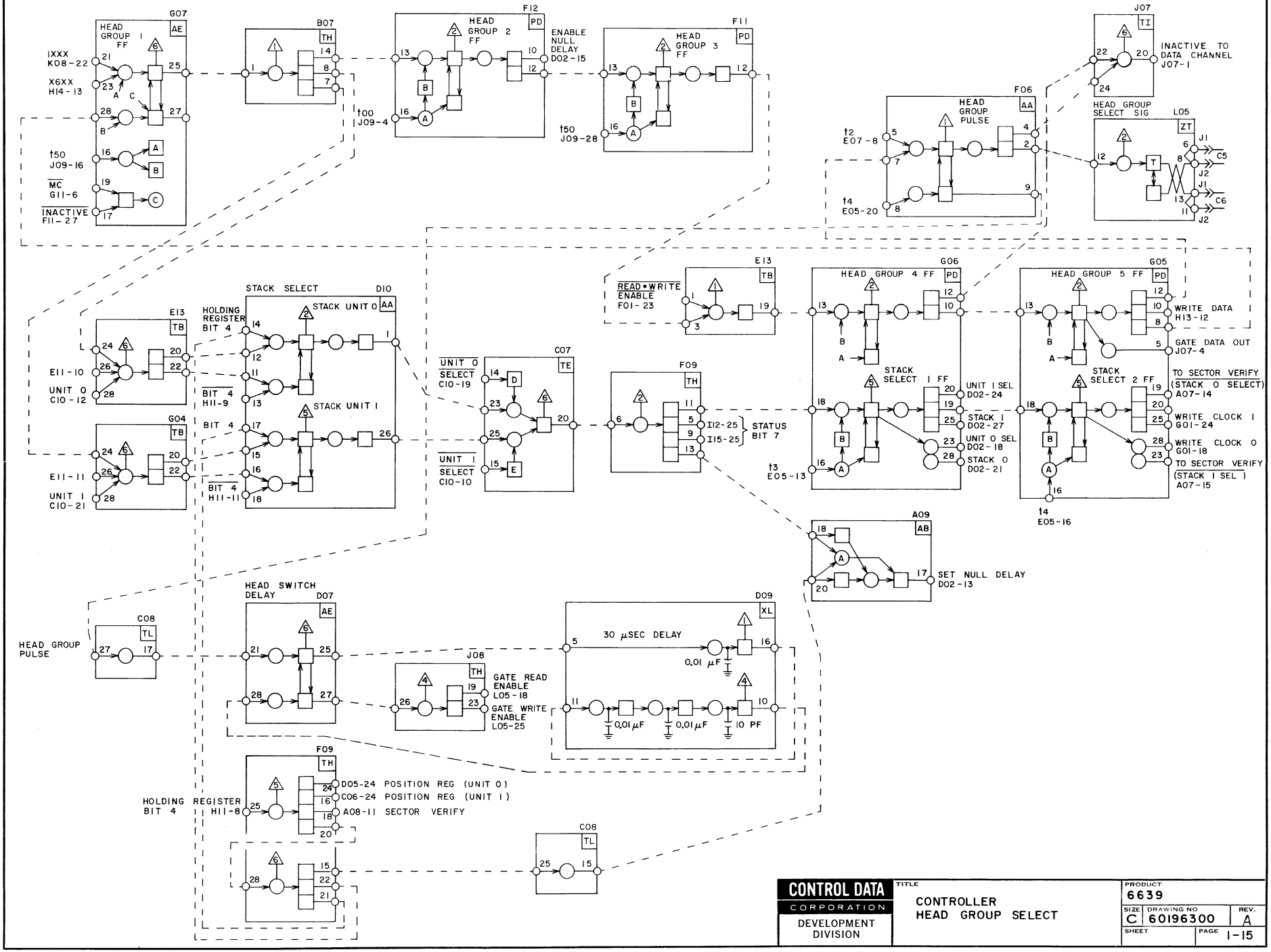
The Head Group Select function word activates the head group select logic and loads the 5-bit head group address in the Holding register. Activating the logic provides a Head Group pulse which 1) provides for transmitting a Head Group Inactive signal to the Data Channel indicating acceptance of the function word, 2) enables a Head Group Select signal to the disk file, and 3) activates the Head Switch Delay circuit to provide time for the read/write heads to complete their switching before a Read or Write operation. At completion of the delay, read or write enables are provided.

Bit 4 of the Holding register determines if a head group is to be selected in stack 0 or 1 (in unit 0 or 1 as previously selected by the Connect and Status function code). If bit 4 is a "0", the head group is selected in stack 0 (bits 0-15). If bit 4 is a "1", the head group is selected in stack 1 (bits 16-31). When the head group selection is made in the designated stack, this information is available for sampling as the next status word, and enables are provided for the write clock and sector verify logic.

If the head groups are to be selected (switched) during an I/O operation, a Head Group Select function can be issued to switch heads between sectors. However, if the switching involves changing to heads in the other stack, the Null Delay circuit (page 1-11) provides a 4-millisecond delay to allow the positioner to become off point and start to reposition on the other stack. This delay occurs each time that heads are switched between stacks.

HEAD GROUP SELECT TIMING

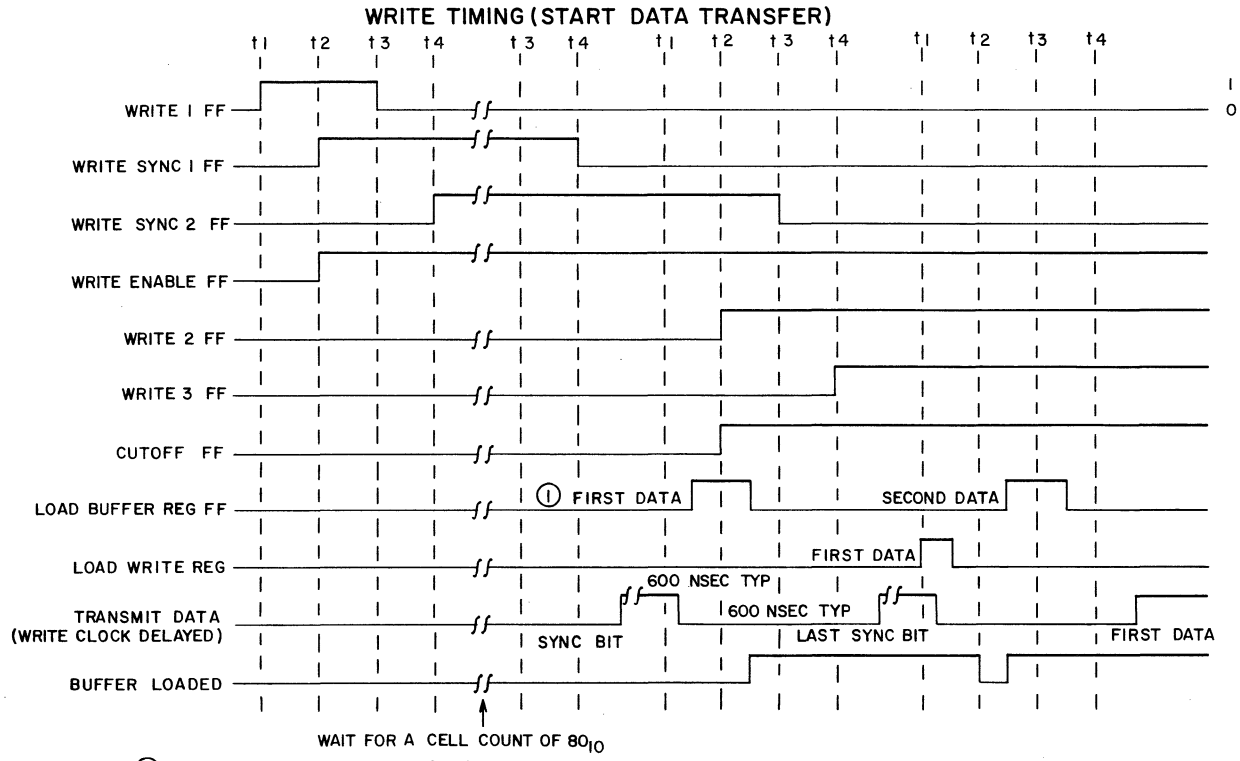


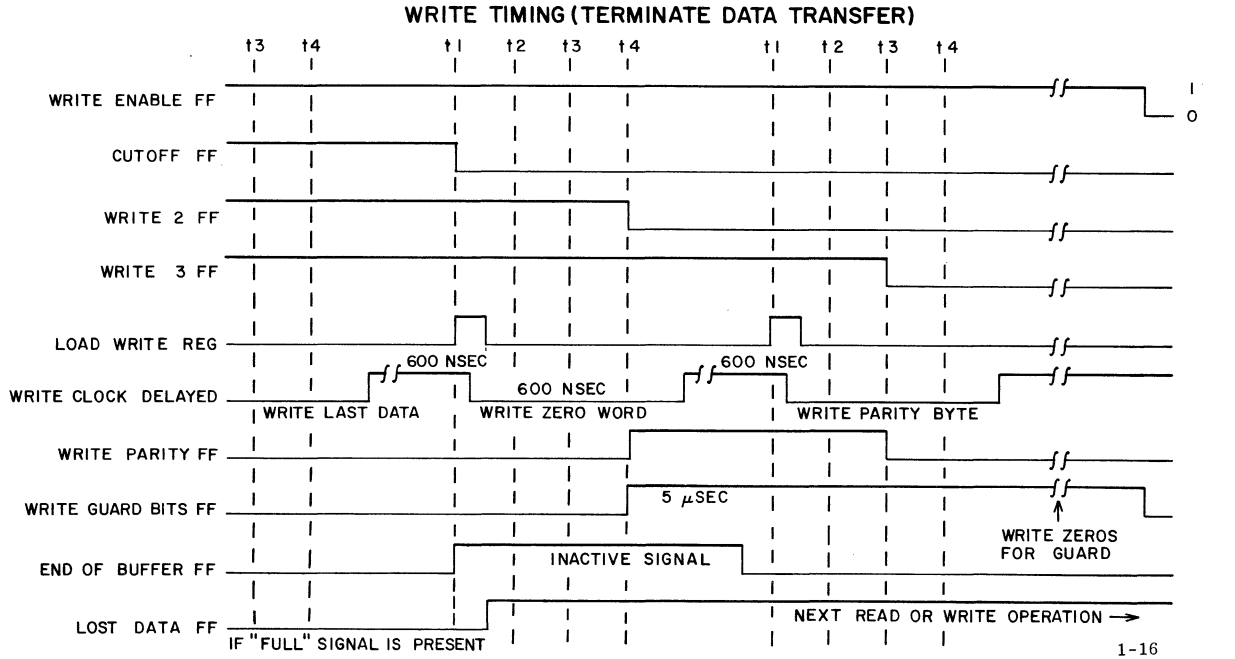


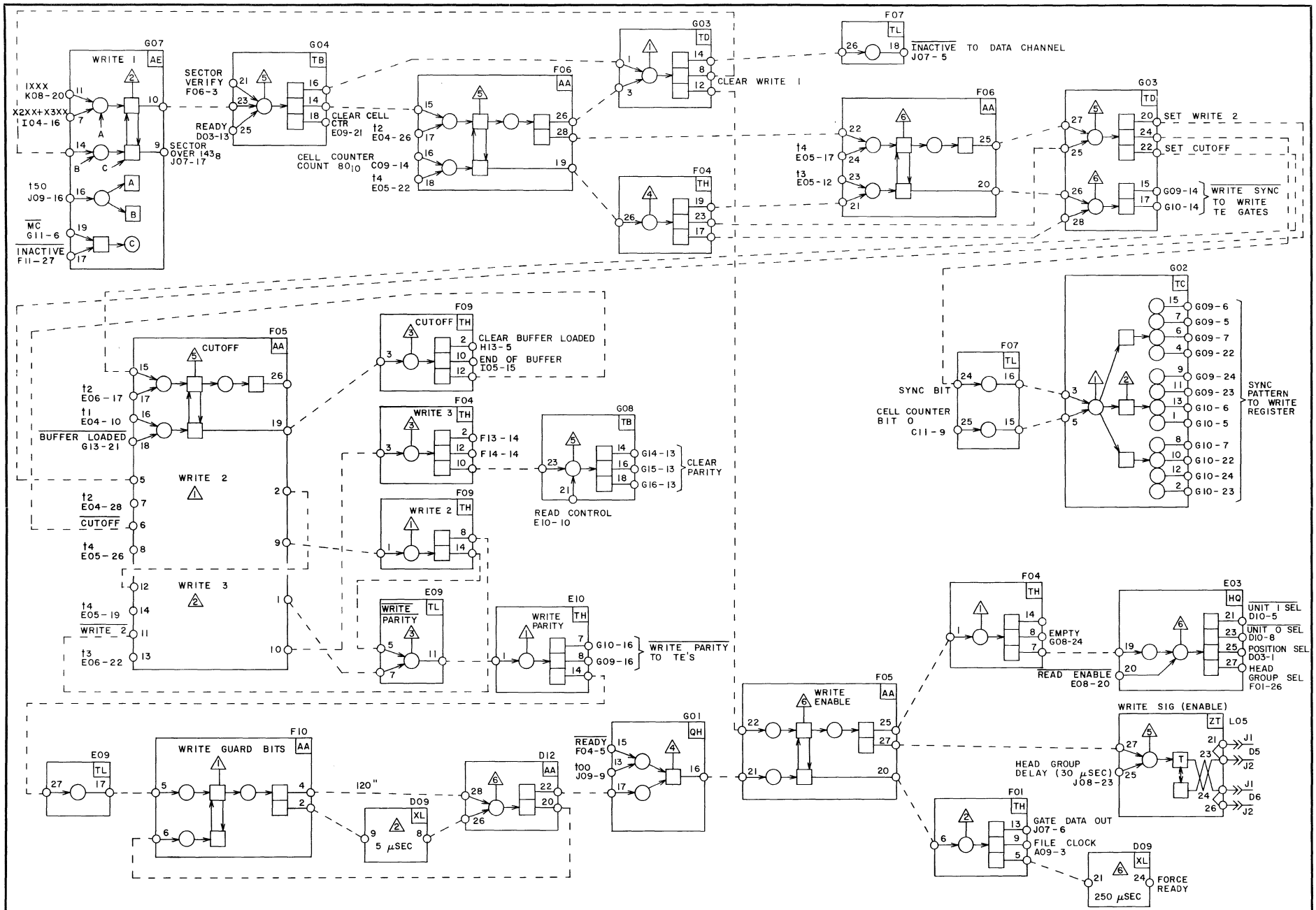
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER HEAD GROUP SELECT	PRODUCT 6639	
		SIZE C	DRAWING NO 60196300 REV. A
		SHEET	PAGE 1-15

The Write function word activates the write logic and loads the 7 bits of the function word containing the sector address to the Holding register. Further operations in the write control logic depend upon completion of Sector Verify and the presence of Ready. Sector Verify ensures that the Write operation will begin at the sector designated by the Write function word. A Ready indicates that the disk file positioner is on point, that the position at which the Write operation is to take place has been verified, and that the disk file is Ready for operation.

When the sector is verified and the system is Ready, the Write Enable gates the Write signal to the disk file. The Cell counter begins counting preamble bits, starting at the sector mark determined by sector verify; an Inactive signal is returned to the Data Channel to indicate acceptance of the Write function word. The 80 preamble bits are written in an alternating "1's" and "0's" pattern. Two "1" bits in succession signify the beginning of data. The second "1" bit is the sync bit. The data buffer (record) may cover from 1 to 10 sectors. At the end of data is the postamble, consisting of at least 28 bits, including the parity and guard bits. Only the parity and guard bits (5 bits) are written on the record. At the end of the record, the buffer register is not loaded, clearing the Cutoff FF. This causes the Write 2 FF to clear, resulting in the writing of the guard bit "0's". The Write 3 FF clears, enabling the parity byte generated from the last record to be written as well as the remainder of the postamble. If a new record is to be written, a new Write function code must be issued within 100 microseconds to retain the connect.





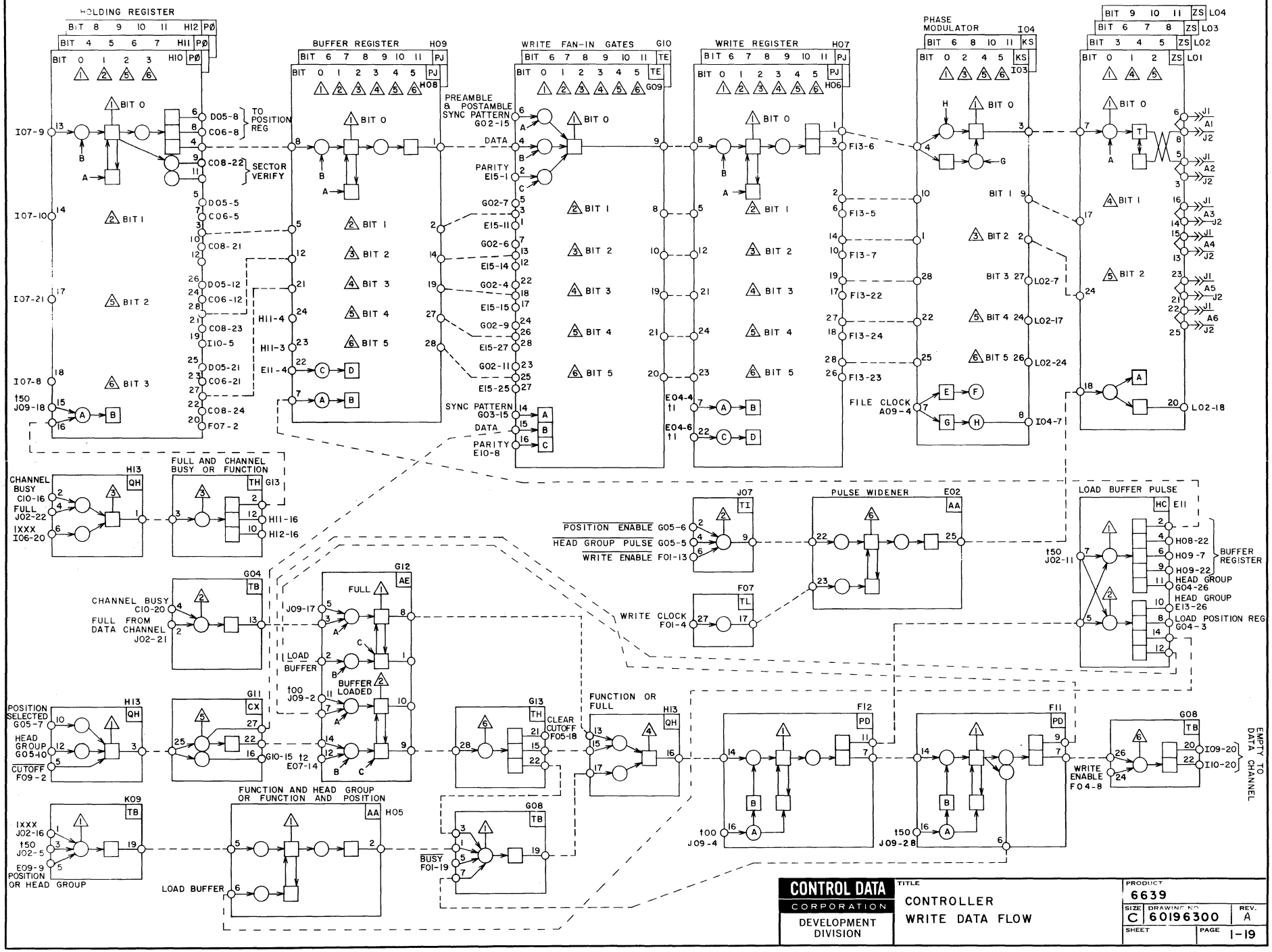


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER WRITE CONTROLS	PRODUCT 6639	
		SIZE C	DRAWING NO. 60196300 REV. A
		SHEET	PAGE 1-17

The Holding, Buffer, and Write registers, and write fan-in gates provide a path for the transmission of data out to the disk file. All function or data words are transmitted to the Holding register. During a Write, a Full signal is needed from the Data Channel to enable data to the Buffer register.

The write fan-in gates allow gating of the sync pattern (preamble) bits, data, or parity byte out to the disk file.

As data is shifted in parallel to the disk file, an Empty signal is generated and sent to the Data Channel. The Data Channel returns another data word with a Full pulse and the process is repeated. Operation continues in this manner until the end of the buffer (record).



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
CONTROLLER
WRITE DATA FLOW

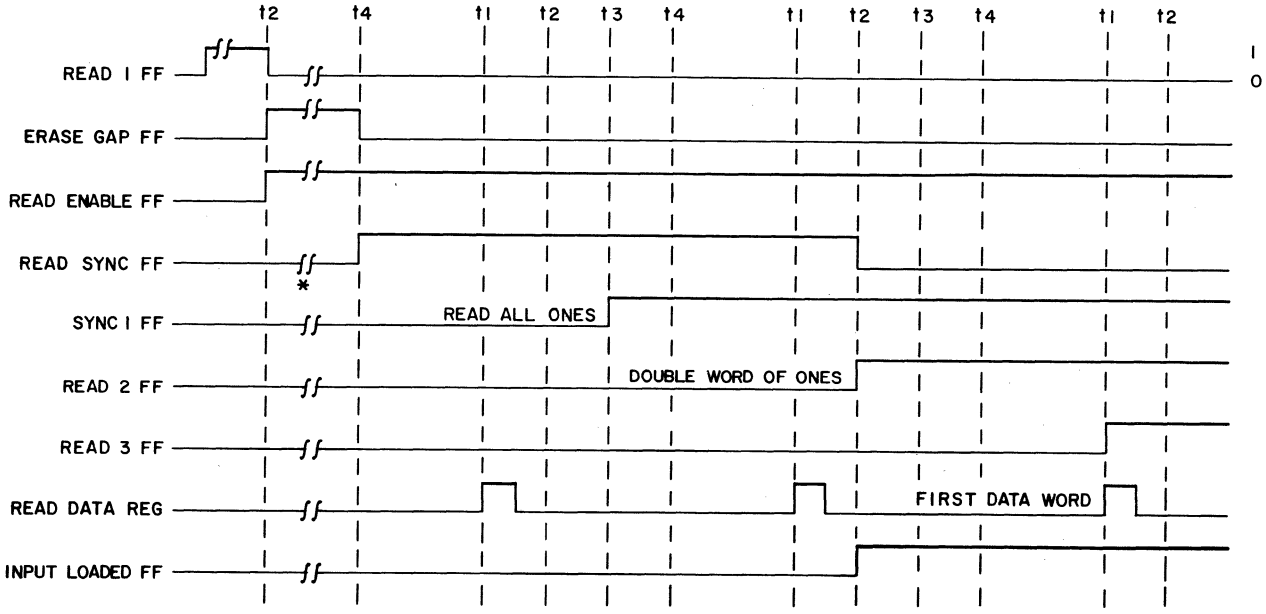
PRODUCT 6639
SIZE C | DRAWING NO. 60196300 | REV. A
SHEET | PAGE 1-19

The function code portion of the Read function word activates the read logic. The address portion of the Read function word contains the sector address.

Sector Verify and Ready signals must be present as for a Write function. The Sector Verify pulse indicates that the sector mark has been determined at which reading will begin. An Inactive signal is returned to the Data Channel to denote the acceptance of the function word. When the Cell counter reaches a count of 106_8 (70_{10}), the controller begins looking at the preamble. When 2 bytes of sevens are read in succession (page 1-23), the Read 2 FF sets. Setting the Read 2 and Read 3 FFs denotes the beginning of data transfer. It enables the data being read off the disk to be gated through the controller registers to the Data Channel.

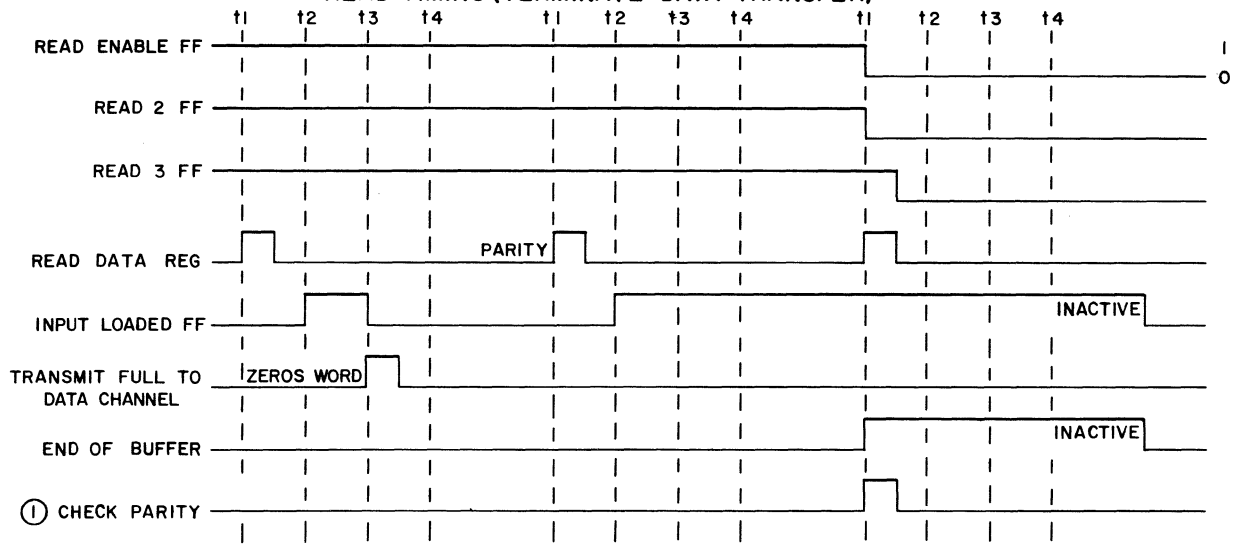
If 2 bytes of all sevens are not read in succession by the time the Cell counter reaches a count of 160_8 (112_{10}), the Read 2 FF is forced to set in order to prevent a hang-up, and the Parity Error FF is set automatically.

READ TIMING (START DATA TRANSFER)



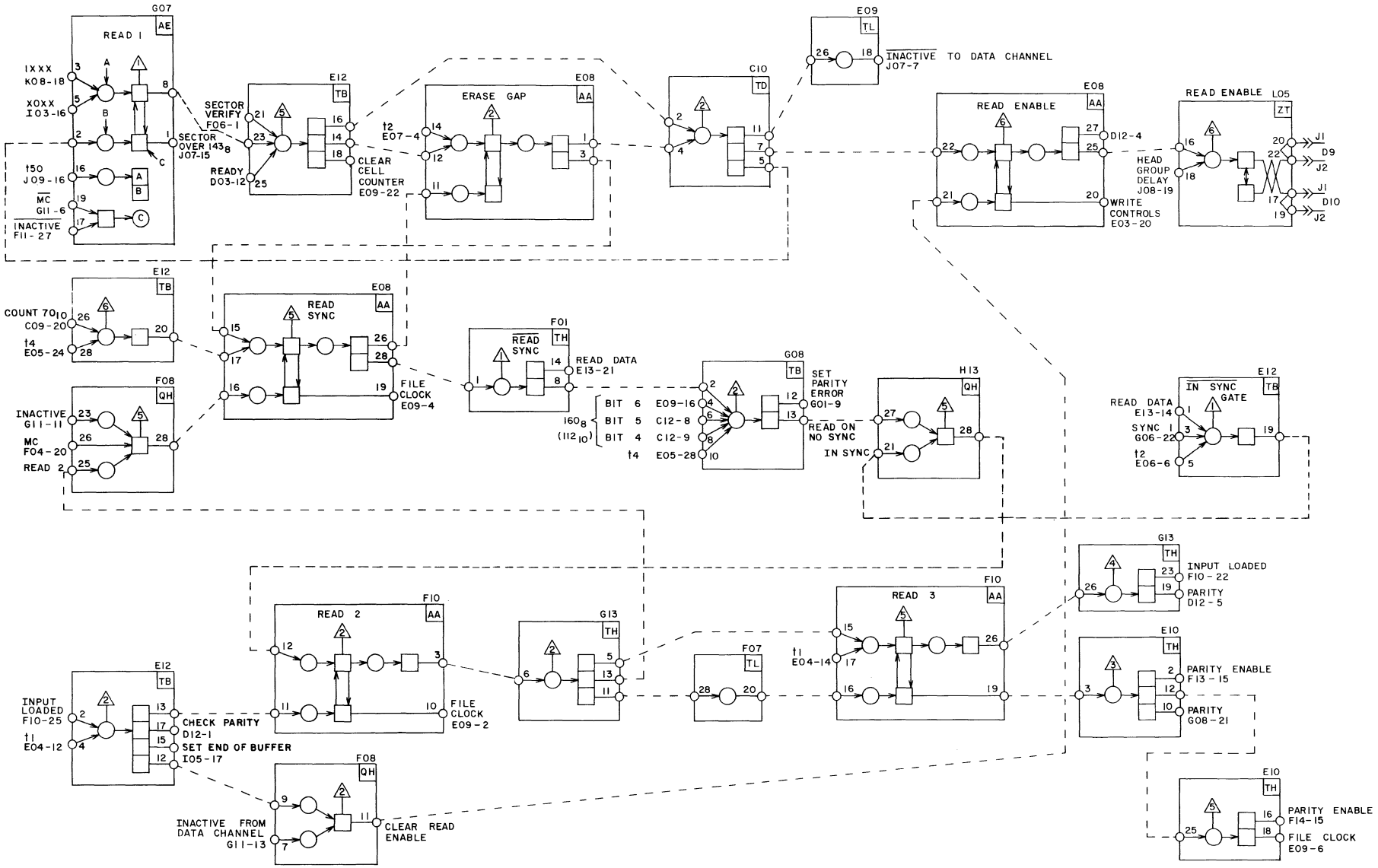
* WAIT FOR A CELL COUNT OF 70_{10}

READ TIMING (TERMINATE DATA TRANSFER)



NOTES:

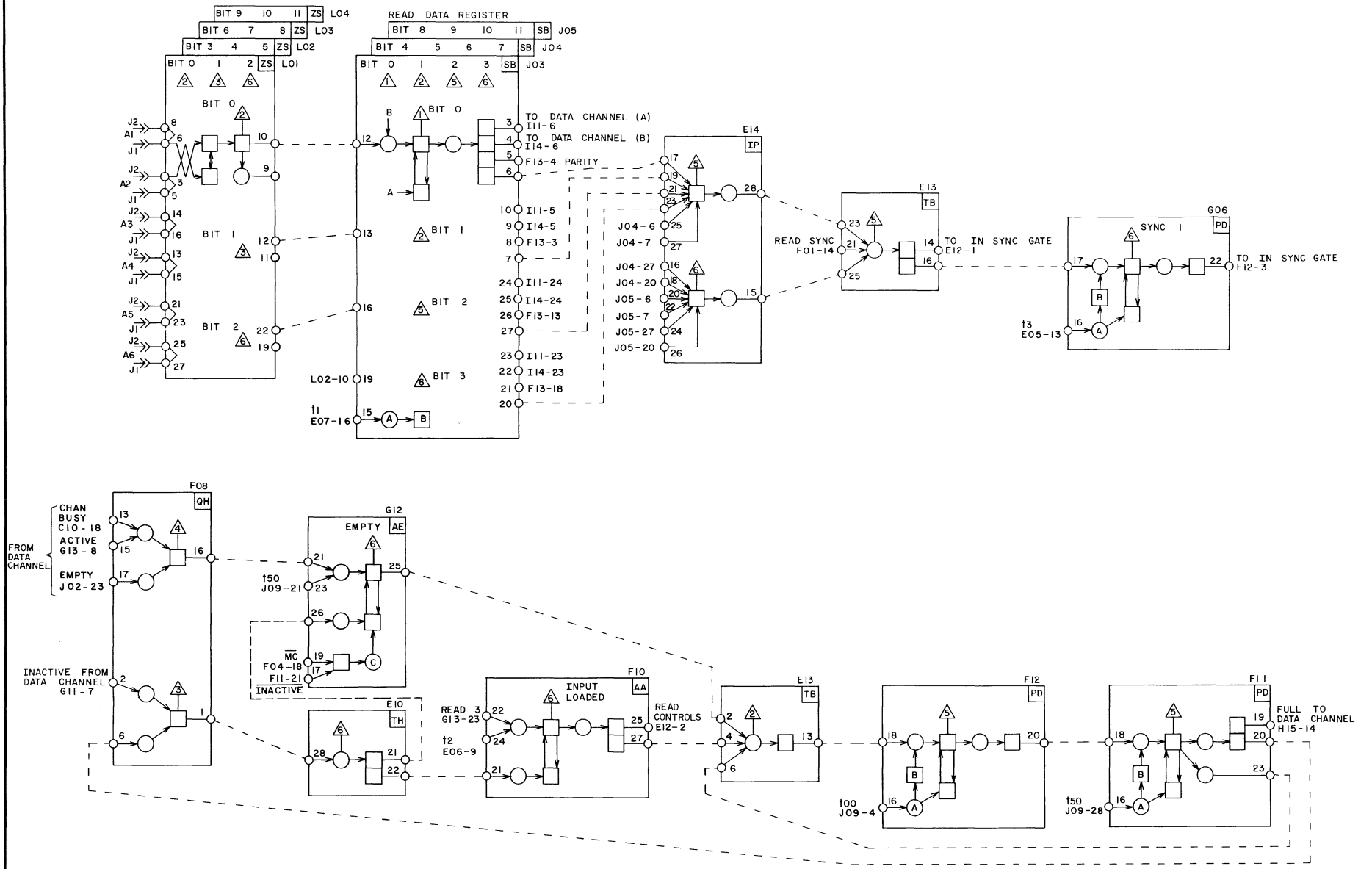
① SEE PAGE 1-29, GOI-TP2



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER READ CONTROLS	PRODUCT 6639	
		SIZE C	DRAWING NO 60196300
		REV. A	
		SHEET	PAGE 1-21

Data being read from the disk file is transmitted through the Read Data register to the Data Channel. During reading of the preamble, alternating bytes of "1's" (7777_8) and "0's" (0000) are read off the disk. Each time T1 comes up, a byte is gated into the Read Data register. A byte of "1's" sets the Sync I FF at T3. A byte of "0's" clears the Sync I FF. Since the preamble contains alternating "1's" and "0's" bytes, the Sync I FF is alternately set and cleared until the beginning of data. Two consecutive bytes of "1's" denotes the beginning of data. The Sync I FF is set, and the Read register is all sevens, allowing the in sync gate (page 1-21) to output a "1" at the next T2, thereby setting the Read 2 FF (page 1-21).

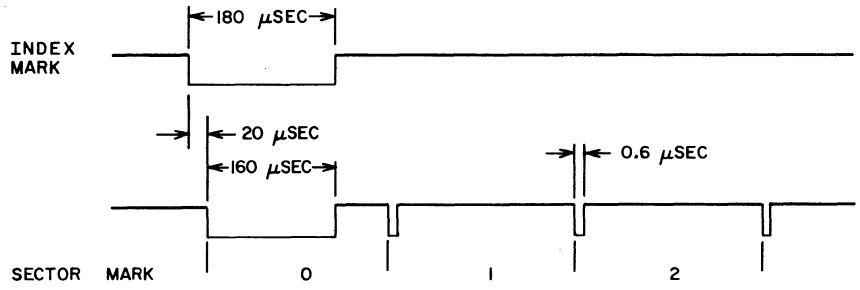
The Data Channel sends an Active signal requesting the controller to send the first data word. In this case, the Active serves as the first Empty. The controller responds with the data word accompanied by a Full signal. Thereafter, the Data Channel returns an Empty signal to request more data. The process is repeated to the end of the buffer (record).

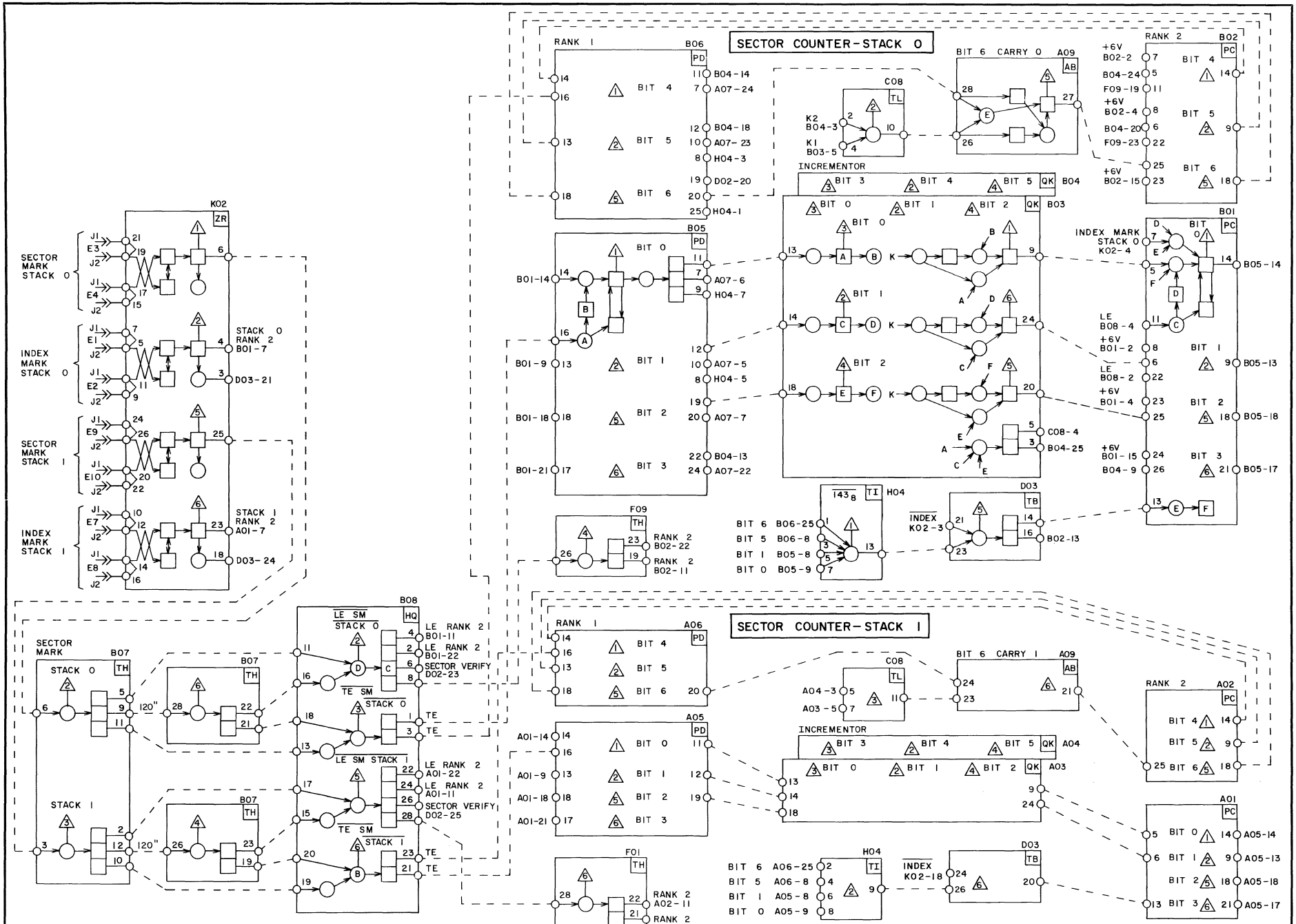


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER READ DATA FLOW	PRODUCT 6639	
		SIZE C	DRAWING NO 60196300
		REV. A	
		SHEET	PAGE 1-23

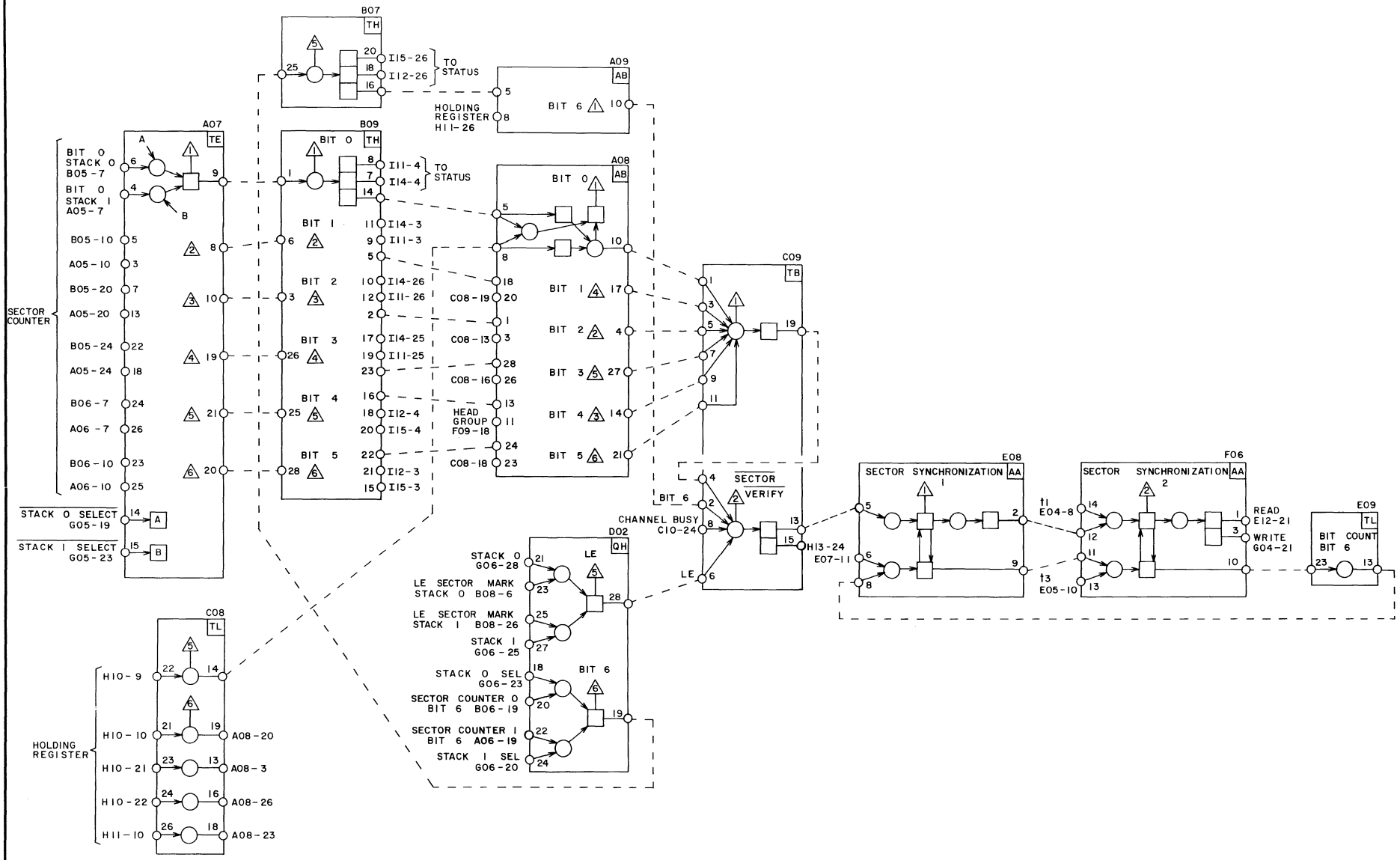
Sector Mark pulses received from the disk file are gated to the Sector counters for stacks 0 or 1. The leading edge of the Sector Mark pulse advances the incremented count in rank 2, and the trailing edge transfers the count in rank 1. The rank 1 count represents the actual position (plus 1) of the read/write heads.

Since only 100_{10} sectors are used, the counter must be cleared to 0000 when 143_8 (100_{10}) is reached. The Sector Mark 0 pulse lags the Index Mark pulse by 20 microseconds, and its duration is wider than the other pulses as shown:




SECTOR COUNTER-STACK 0
SECTOR COUNTER-STACK 1
RANK 1
RANK 2
INCREMENTOR
BIT 6 CARRY 0
BIT 6 CARRY 1
SECTOR MARK STACK 0
INDEX MARK STACK 0
SECTOR MARK STACK 1
INDEX MARK STACK 1
STACK 0 RANK 2 B01-7
STACK 1 RANK 2 A01-7
D03-21
D03-24
INDEX MARK STACK 0 K02-4
LE SM STACK 0
LE SM STACK 1
TE SM STACK 0
TE SM STACK 1
LE RANK 2 B01-11
LE RANK 2 B01-22
SECTOR VERIFY D02-23
LE RANK 2 A01-22
LE RANK 2 A01-11
SECTOR VERIFY D02-25
INDEX K02-3
INDEX K02-18
RANK 2 B02-22
RANK 2 B02-11
RANK 2 A02-11
RANK 2 A02-22
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
CONTROLLER SECTOR VERIFY 1
PRODUCT 6639
SIZE C
DRAWING NO. 60196300
REV. A
SHEET
PAGE 1-25

The contents of the Sector counter, which reflect the actual position of the read/write heads, are compared against the Holding register contents containing the designated sector address. Sector Verify occurs when 1) the Leading Edge pulse of a sector mark for the selected stack is present, and 2) the contents of the Sector counter and Holding register are equal.

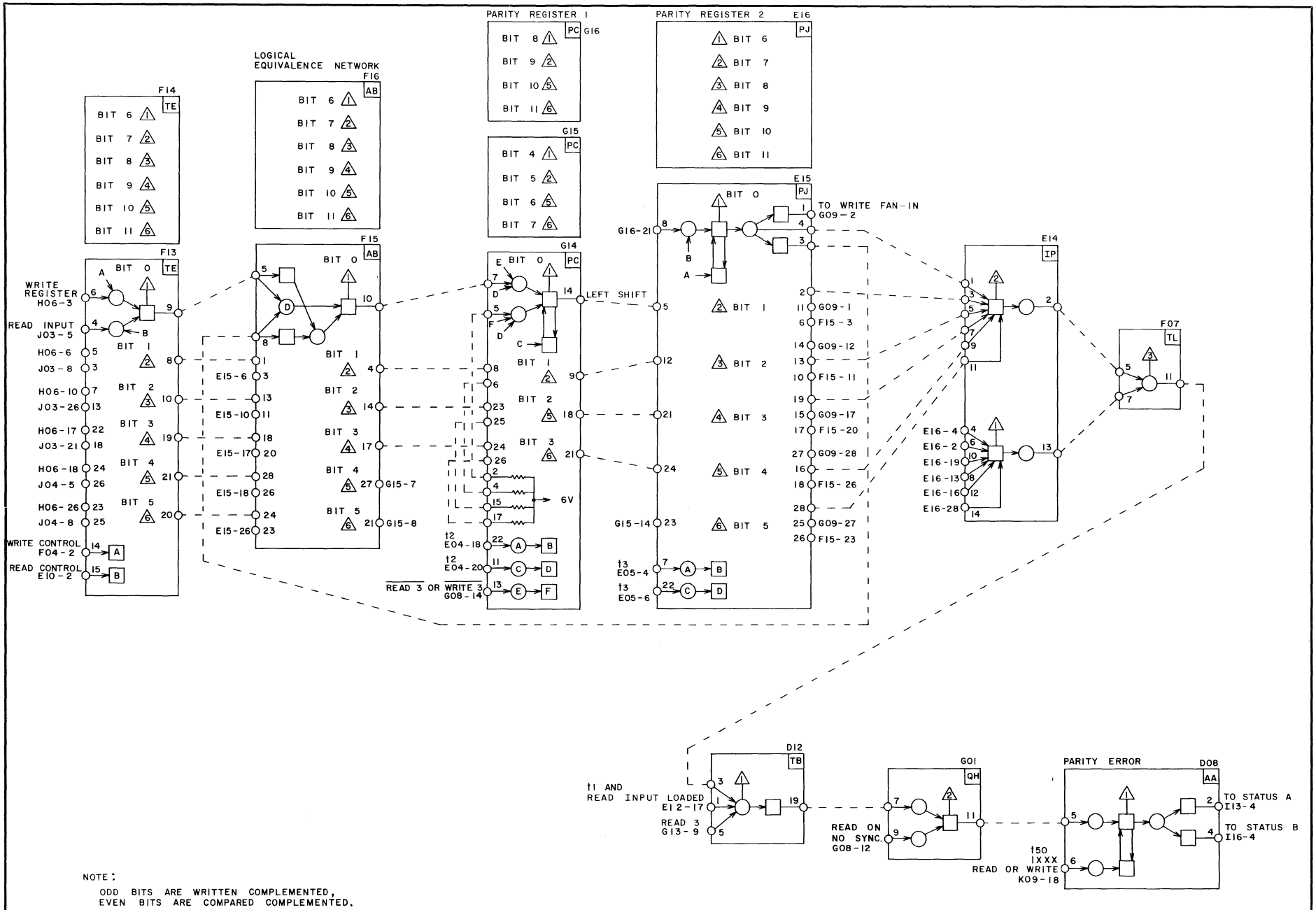


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER SECTOR VERIFY 2	PRODUCT 6639	
		SIZE C	DRAWING 60196300
		REV. A	
		SHEET	PAGE 1-27

A parity byte is generated for each record that is written on the disk. The parity byte is written on the disk at the end of the record. During a Read operation, this previously written parity byte is read back and it should be the same as the parity byte generated from the record being read. If not, a parity error is present.

On a Write, the contents of Parity register 2 (register 2) should be initially all "0's". The contents of register 2 are merged with the first byte of the write word in the logical equivalence network. This forms the logical equivalent which is gated to Parity register 1 (register 1). The contents of register 1 are then left-shifted one place (end-around) to register 2. The odd bits (1, 3, 5, etc) in register 2 are complemented and transferred to the write fan-in gates on each iteration. On the last iteration (at the end of the record), the complemented odd bits together with the uncomplemented even bits of register 2 are written on the disk as the parity byte.

As the record is transferred back during a Read, the process is the same as for the Write, except that the even bits in register 2 are complemented. Receiving a parity byte should cause a bit pattern of 2525_8 in register 1. The contents of register 1 are then left-shifted into register 2 for a resulting bit pattern of 5252_8. The even bits of the parity byte are then complemented and all bits compared. This should cause all "1's" to be gated out of register 2 which in turn results in no parity error.



NOTE:

ODD BITS ARE WRITTEN COMPLEMENTED,
EVEN BITS ARE COMPARED COMPLEMENTED.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER PARITY	PRODUCT 6639	
		SIZE C	DRAWING 60196300
		REV. A	
		SHEET	PAGE 1-29

CHANNEL BUSY

During initiation of a Read or Write operation, the Channel Busy FF sets to indicate an operation is in progress. It provides enables for gating Sector Verify, Full, and Empty signals to the Data Channel and terminating the operation when the right conditions are present. An Inactive signal generated by either the Data Channel or the controller clears the Channel Busy FF.

INACTIVE

The Inactive FF sets to return an Inactive signal to the Data Channel for normal replies to the functions (Read, Write, Position Select, or Head Group Select) or when the following abnormal conditions are present: 1) setting of Lost Data FF, or 2) channel Busy, Active, and Not Ready, or 3) sector of 144_8 or greater selected and Read 1 or Write 1 FF set.

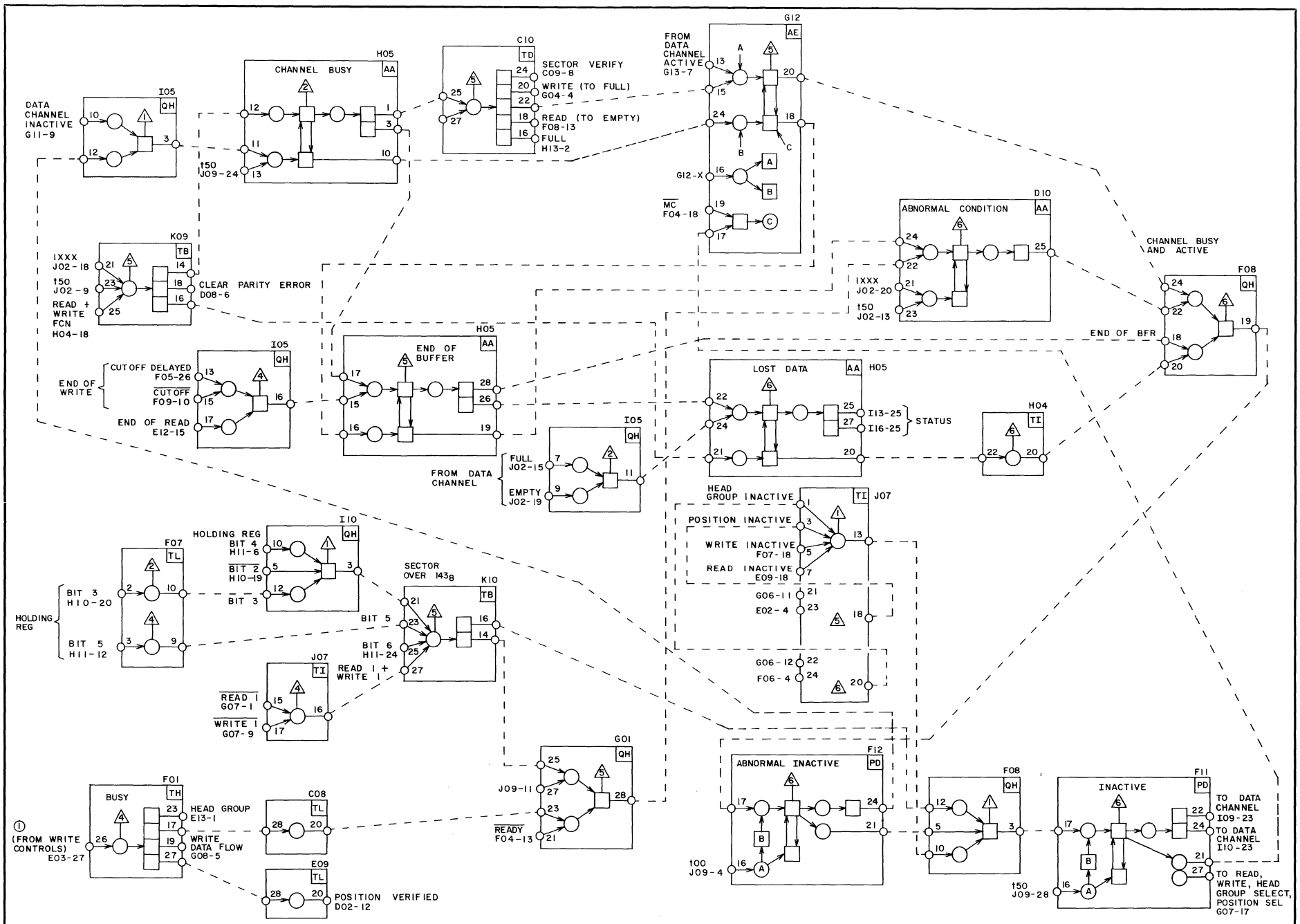
END OF BUFFER

The end of data on a Write or the end of a Read operation sets the End of Buffer FF. This enables the Lost Data FF to set if a new Full or Empty signal is seen before an Inactive.

LOST DATA

The Lost Data FF sets for the following conditions:

1) When an input or output buffer follows a Read or Write function, respectively, by more than 90 microseconds.
2) If program control issues a Read or Write function which is followed by two consecutive inputs or outputs.
3) If the instantaneous disk file rate exceeds the Data Channel rate.



NOTES:

① READ · WRITE ENABLE

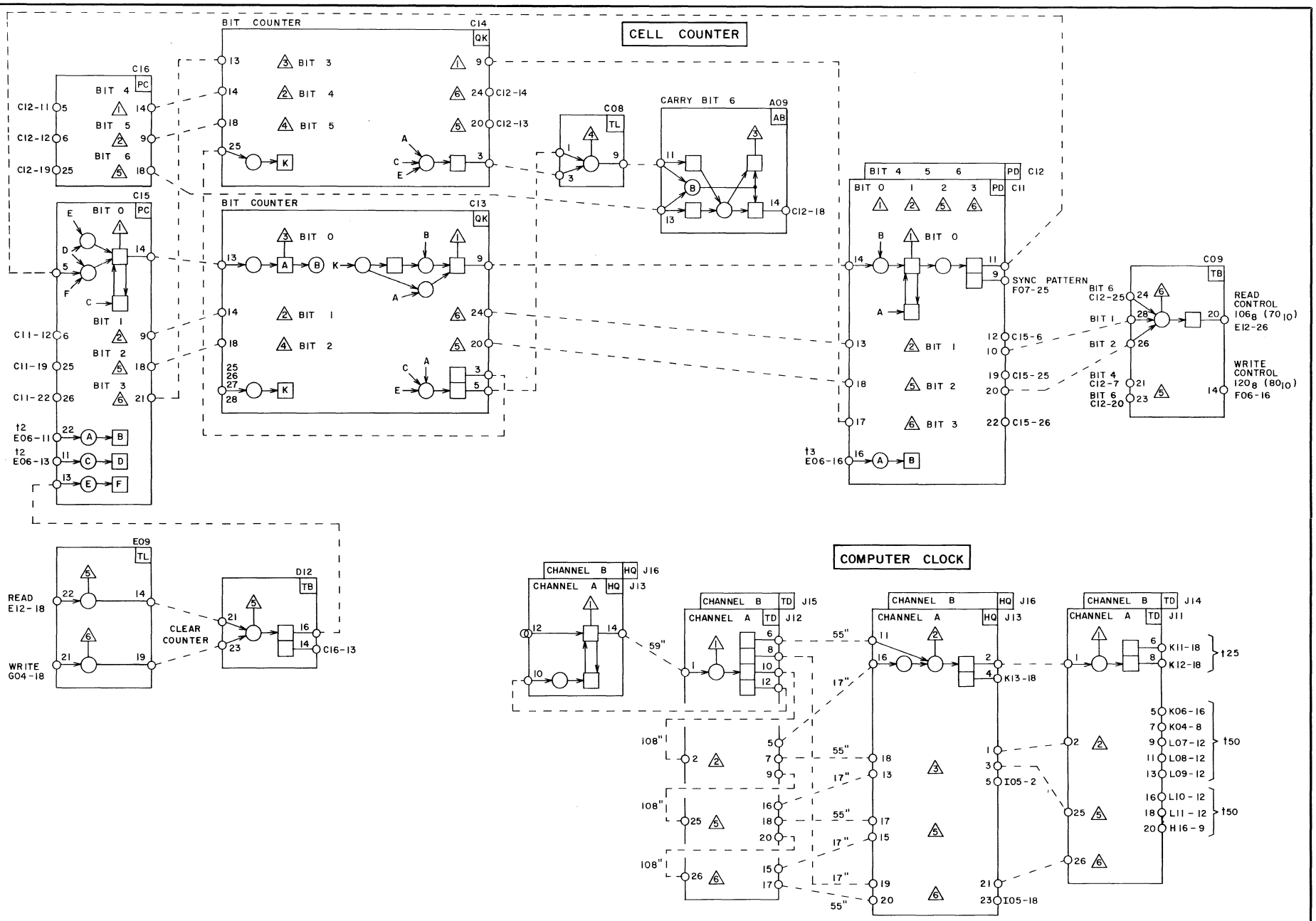
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER CHANNEL BUSY, INACTIVE, END OF BUFFER, AND LOST DATA CONTROLS	PRODUCT 6639	
		SIZE C	DRAWING NO. 60196300 REV. A
		SHEET	PAGE 1-31

CELL COUNTER

The Cell counter counts disk file Clock pulses. The Cell counter is used to count preamble bits for determining the beginning of data during a Read or Write operation. It provides three bit-count translations. These are 80_{10} (write preamble), 70_{10} (read preamble), and 112_{10} (forces setting of Read 2 FF, page 1-21, in the event it is not set at the end of the preamble).

COMPUTER CLOCK

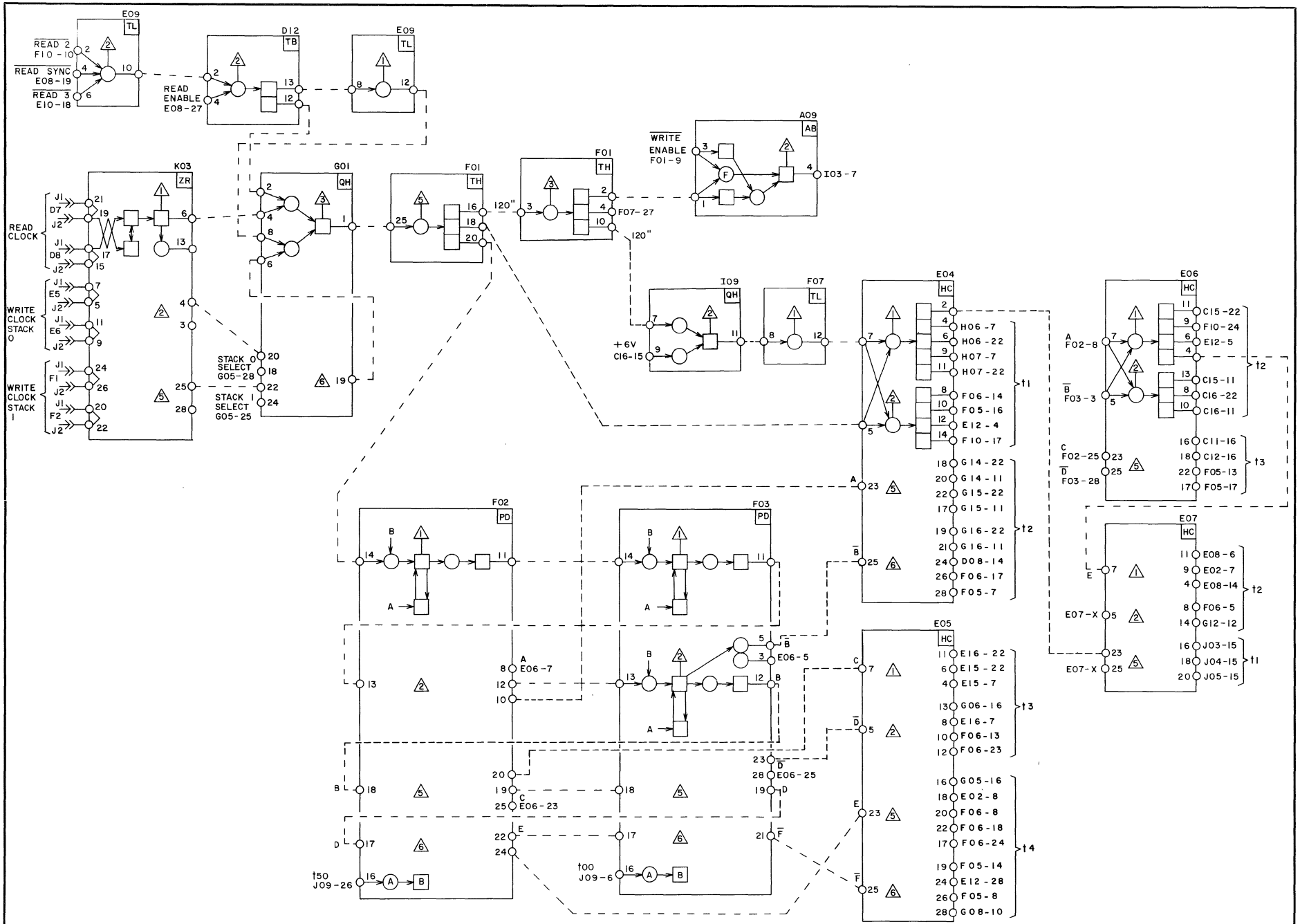
The 10-megacycle input from the Data Channel (computer clocks) is used to provide 25-nanosecond Timing pulses for sequencing operations between the computer and the controller.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER CELL COUNTER AND COMPUTER CLOCK	PRODUCT 6639	
		SIZE C	DRAWING NO 60196300
		REV. A	
		SHEET	PAGE 1-33

The file clock logic receives Clock pulses from a permanently recorded clock track in the disk file. These Clock pulses provide for synchronizing the writing of data in the disk file. Times T1, T2, T3, and T4 come up in 100-nanosecond intervals.

Time T1 is a Leading Edge pulse formed off the file clock. Times T2, T3, and T4 are synchronized with the computer clock. Provisions are made to use the read self-clock when reading.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONTROLLER FILE CLOCK	PRODUCT 6639	
		SIZE C	DRAWING NO. 60196300
		SHEET	PAGE 1-35

PART 2

MAINTENANCE

PART 2

MAINTENANCE

INTRODUCTION

The CONTROL DATA* 6639 Disk File Controller contains the circuitry necessary for controlling I/O operations between 6000 Series computers and the 808 Disk File. Maintenance procedures for the controller follow the same general routines used in other Control Data equipment.

In addition to this manual, the following supporting documents provide information to aid maintenance personnel in servicing the equipment:

CONTROL DATA 6000 Series Peripheral Equipment Reference Manual	Pub. No. 60156100
CONTROL DATA 6000 Series Input/Output Specifications Manual	Pub. No. 60045100
CONTROL DATA Peripheral Controller Cabinets Manual	Pub. No. 60097300
CONTROL DATA Cordwood Modules Manual, Volumes 1, 2, and 3	Pub. No. 60042700

PHYSICAL DESCRIPTION

Refer to Table 2-1 for physical, electrical, and environmental specifications for the controller.

TABLE 2-1. CONTROLLER SPECIFICATIONS

PHYSICAL		ELECTRICAL
Height	56-7/8 inches (1.44 m)	208 volts, 3-phase, 400 cycles, 2.3 amperes
Width	42 inches (1.07 m)	
Depth	20-1/2 inches (0.52 m)	120 volts, single-phase, 60 cycles, 2.8 amperes
Weight	659 pounds (300 kg)	
Operating Environment	60° to 78°F (15.5° to 25.5°C) temperature 25% to 75% relative humidity	
Heat Dissipation	4100 BTU/hr (1032 kg-cal/hr)	

*Registered trademark of Control Data Corporation

TRANSMISSION LINE ASSIGNMENTS

Refer to Tables 2-2 and 2-3 for cable wire assignments between the controller and the Data Channel and to Table 2-4 for controller-to-disk-file pin assignments.

TABLE 2-2. INPUT CABLE LINE ASSIGNMENTS - CONTROLLER TO DATA CHANNEL

Input to Data Chan A or B From Controller Data Bit or Sig	38W04 to Data Chan A From Controller Card, Pin	38W05 Pass-Back to Controller (Interface A) Card, Pin	38W06 to Data Chan B From Controller Card, Pin	38W07 Pass-Back to Controller (Interface B) Card, Pin	Color Code of Wires Between Controller and Data Chan
0	K11-23	K11-7	K14-23	K14-7	90
1	K11-22	K11-5	K14-22	K14-5	91
2	K11-21	K11-3	K14-21	K14-3	92
3	K11-10	K11-28	K14-10	K14-28	93
4	K11-9	K11-26	K14-9	K14-26	94
5	K11-8	K11-24	K14-8	K14-24	95
6	K12-23	K12-7	K15-23	K15-7	96
7	K12-22	K12-5	K15-22	K15-5	97
8	K12-21	K12-3	K15-21	K15-3	98
9	K12-10	K12-28	K15-10	K15-28	99
10	K12-9	K12-26	K15-9	K15-26	900
11	K12-8	K12-24	K15-8	K15-24	901
Active	K13-23	K13-7	K16-23	K16-7	902
Inactive	K13-22	K13-5	K16-22	K16-5	903
Full	K13-21	K13-3	K16-21	K16-3	904
Empty	K13-10	K13-28	K16-10	K16-28	905
Clock (10 mc)	J13-12	K13-26	J16-12	K16-26	906
Clock (1 mc)	K13-8	K13-24	K16-8	K16-24	907
Not Used					908

TABLE 2-3. OUTPUT CABLE LINE ASSIGNMENTS - DATA CHANNEL TO CONTROLLER

Output From Data Chan A or B to Controller Data Bit or Sig	38W00 From Data Chan A to Controller Card, Pin	38W01 Pass-On From Controller (Interface A) Card, Pin	38W02 From Data Chan B to Controller Card, Pin	38W03 Pass-On From Controller (Interface B) Card, Pin	Color Code of Wires Between Controller and Data Chan
0	L07-3	L07-1	L12-3	L12-1	90
1	L07-13	L07-15	L12-13	L12-15	91
2	L07-16	L07-14	L12-16	L12-14	92
3	L07-26	L07-28	L12-26	L12-28	93
4	L08-3	L08-1	L13-3	L13-1	94
5	L08-13	L08-15	L13-13	L13-15	95
6	L08-16	L08-14	L13-16	L13-14	96
7	L08-26	L08-28	L13-26	L13-28	97
8	L09-3	L09-1	L14-3	L14-1	98
9	L09-13	L09-15	L14-13	L14-15	99
10	L09-16	L09-14	L14-16	L14-14	900
11	L09-26	L09-28	L14-26	L14-28	901
Active	L10-3	L10-1	L15-3	L15-1	902
Inactive	L10-13	L10-15	L15-13	L15-15	903
Full	L10-16	L10-14	L15-16	L15-14	904
Empty	L10-26	L10-28	L15-26	L15-28	905
Function	L11-3	L11-1	L16-3	L16-1	906
Master Clear	L11-13	L11-15	L16-13	L16-15	907
Not Used					908

TABLE 2-4. CONTROLLER TO DISK FILE CABLE PIN ASSIGNMENTS

PIN	SIGNAL	DIRECTION
A1-2	Data Bit 0	Bi-Directional
A3-4	Data Bit 1	Bi-Directional
A5-6	Data Bit 2	Bi-Directional
A7-8	Data Bit 3	Bi-Directional
A9-10	Data Bit 4	Bi-Directional
B1-2	Data Bit 5	Bi-Directional
B3-4	Data Bit 6	Bi-Directional
B5-6	Data Bit 7	Bi-Directional
B7-8	Data Bit 8	Bi-Directional
B9-10	Data Bit 9	Bi-Directional
C1-2	Data Bit 10	Bi-Directional
C3-4	Data Bit 11	Bi-Directional
C5-6	Head Select	To Disk File
C7-8	Position Select	To Disk File
C9-10	On Point	From Disk File
D1-2	Position (Track) Verification Data	From Disk File
D3-4	Position (Track) Verification Clock	From Disk File
D5-6	Write Enable	To Disk File
D7-8	Read Clock	From Disk File
D9-10	Read Enable	To Disk File
E1-2	Index Mark Stack 0	From Disk File
E3-4	Sector Mark Stack 0	From Disk File
E5-6	Write Clock Stack 0	From Disk File
E7-8	Index Mark Stack 1	From Disk File
E9-10	Sector Mark Stack 1	From Disk File
F1-2	Write Clock Stack 1	From Disk File
F3-4	Ready	From Disk File
F5-6	Unit Select 0	To Disk File
F7-8	Unit Select 1	To Disk File
F9-10	Terminator Power	*

*Terminator Power is provided to the disk file and controller through a separate two-wire power cable.

PART 3

PARTS LIST

INTRODUCTION

The parts list provides the identification and ordering data necessary for the replacement of electrical and hardware parts for the CONTROL DATA 6639 Disk File Controller.

Electrical Contents: All Chassis and cabinet items are included except jumper wires and bulk wire.

The chassis assembly and associated subassemblies are broken down into individual parts, listed in alphabetical rather than disassembly order.

The following publications contain information on printed circuit card assemblies, peripheral cabinets, power supplies and vendor parts lists necessary to complete a total breakdown of the equipment:

Ault Power Supply Manual	Pub. No. 60107300
Control Data Power Supply Manual	Pub. No. 60120700
Peripheral Controller Cabinets Customer Engineering Instruction Manual (Includes cabinet parts list and Control Data modifications to vendor power supplies)	Pub. No. 60097300

ORDERING OF PARTS

When ordering Control Data Parts, include the following information: Control Data drawing number, description, quantity needed, equipment used on. When ordering vendor parts use the procedure indicated by that vendor.

6639 Disk File Controller

Dwg. No. 17963400 PARTS LIST

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
17801900	Bar, Mounting, Card	
18027900	Bar, Mounting, Receptacle	
18082800	Bar, Support	
17944100	Blank Card Cap	
17992900	Bracket, Mounting, Panel, LH	
17993000	Bracket, Mounting, Panel, RH	
18028000	Bus Bar, Horizontal	
17902300	Cabinet Assembly, Peripheral Type B	
18164200	Capacitor, Fixed, Electralytic, 300UF, 10 VDC	
18079700	Card Placement	
18039400	Chassis Assembly	
17928300	Clamp, Bus Bar	
17900200	Clamp, Bus Bar	
00863707	Clamp, Cable, 0.52 ID	
18240800	Connector Assembly, J01, 61 Socket	
24518103	Connector, Flexible, 3/4 Conduit	
24562500	Connector, Receptacle, 30 Socket	
24532300	Connector, Receptacle, 61 Pin	
30094402	Connector, Receptacle, Red, 10 Socket	
30094406	Connector, Receptacle, Blue, 10 Socket	
30094410	Connector, Receptacle, Black, 10 Socket	
30000901	Connector, Receptacle, 61 Socket	
46910000	Disk File	
00865004	Grommet, Strain Relief	
17912702	Insulator Strip, Bus Bar	
17913800	Member, Frame, Chassis, RH	
18038200	Member, Frame, Chassis, LH	
18076100	Panel, Mounting, Connector	
17941500	Panel, Filler	
17884500	Panel, Filler, Front	
17881400	Power Supply Assembly	
30001201	Resistor-Terminator Assembly	
17805300	Seal, Rubber, Connector	
30000902	Socket for Connector 30000901	

6639 Disk File Controller (Cont'd)

PARTS LIST

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
17932700	Strip, Marker, Horizontal, Light Blue, -6	
17932701	Strip, Marker, Horizontal, Light Red, +6	
18228800	Wire List, Logic	

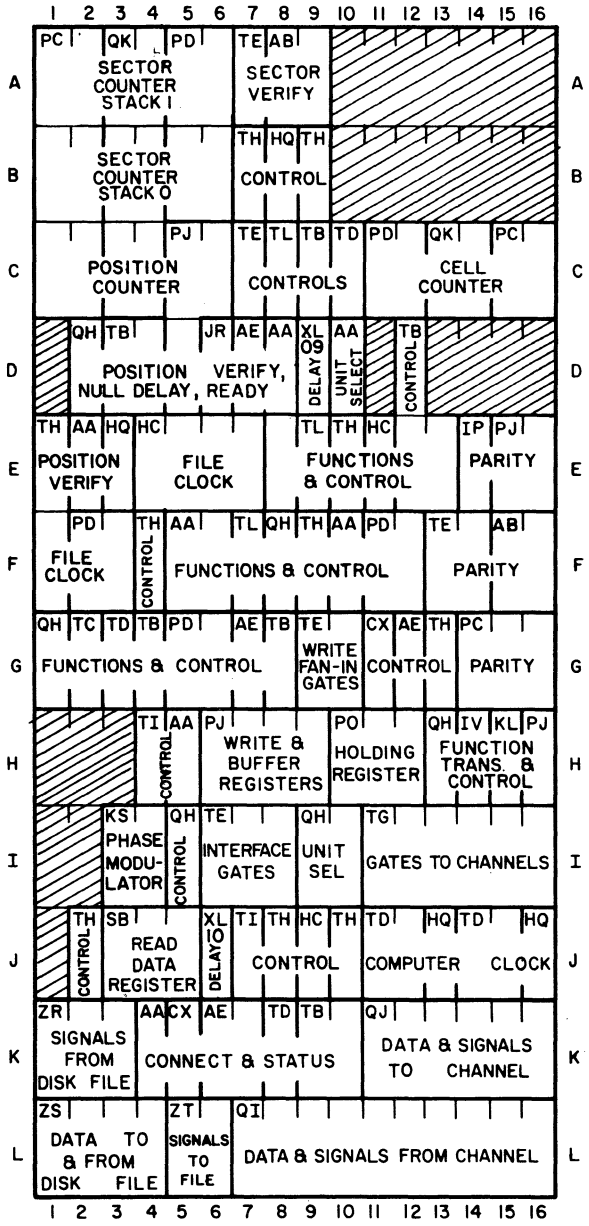
Printed Circuit Module Assembly

PARTS LIST

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
63040000	Printed Circuit Module Assembly, Type AA	
63040100	Printed Circuit Module Assembly, Type AB	
63040400	Printed Circuit Module Assembly, Type AE	
63042900	Printed Circuit Module Assembly, Type CX	
63044800	Printed Circuit Module Assembly, Type HC	
63046200	Printed Circuit Module Assembly, Type HQ	
63048700	Printed Circuit Module Assembly, Type IP	
63049300	Printed Circuit Module Assembly, Type IV	
63051500	Printed Circuit Module Assembly, Type JR	
63053200	Printed Circuit Module Assembly, Type KL	
63053800	Printed Circuit Module Assembly, Type KS	
63057800	Printed Circuit Module Assembly, Type PC	
63057900	Printed Circuit Module Assembly, Type PD	
63058400	Printed Circuit Module Assembly, Type PJ	
63058900	Printed Circuit Module Assembly, Type PO	
63060700	Printed Circuit Module Assembly, Type QH	
63060800	Printed Circuit Module Assembly, Type QI	
63060900	Printed Circuit Module Assembly, Type QJ	
63061000	Printed Circuit Module Assembly, Type QK	
63062700	Printed Circuit Module Assembly, Type SB	
63063400	Printed Circuit Module Assembly, Type TB	
63063500	Printed Circuit Module Assembly, Type TC	
63063600	Printed Circuit Module Assembly, Type TD	
63063700	Printed Circuit Module Assembly, Type TE	
63063900	Printed Circuit Module Assembly, Type TG	
63064000	Printed Circuit Module Assembly, Type TH	
63064100	Printed Circuit Module Assembly, Type TI	
63064400	Printed Circuit Module Assembly, Type TL	
63065500	Printed Circuit Module Assembly, Type XL	
17876300	Printed Circuit Module Assembly, Type ZR	
17876100	Printed Circuit Module Assembly, Type ZS	
17876500	Printed Circuit Module Assembly, Type ZT	

PART 4

CARD PLACEMENT


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
A
PC QK PD
SECTOR COUNTER STACK I
TE AB
SECTOR VERIFY
B
SECTOR COUNTER STACK O
TH HQ TH
CONTROL
C
PJ
POSITION COUNTER
TE TL TB TD
CONTROLS
PD QK PC
CELL COUNTER
D
QH TB
JR AE AA XL 09 DELAY
AA UNIT SELECT
TB CONTROL
POSITION NULL DELAY, VERIFY, READY
E
TH AA HQ HC
POSITION VERIFY
FILE CLOCK
TL TH HC
FUNCTIONS & CONTROL
IP PJ
PARITY
F
PD
FILE CLOCK
TH CONTROL
AA TL QH TH AA PD
FUNCTIONS & CONTROL
TE AB
PARITY
G
QH TC TD TB PD AE TB TE
FUNCTIONS & CONTROL
WRITE FAN-IN GATES
CX AE TH PC
CONTROL
PARITY
H
TI AA CONTROL
PJ
WRITE & BUFFER REGISTERS
PO
HOLDING REGISTER
QH IV KL PJ
FUNCTION TRANS. & CONTROL
I
KS
PHASE MODU-LATOR
QH CONTROL
TE
INTERFACE GATES
QH
UNIT SEL
TG
GATES TO CHANNELS
J
TH CONTROL
SB
READ DATA REGISTER
XL DELAY 10
TI TH HC TH
CONTROL
TD HQ TD HQ
COMPUTER CLOCK
K
ZR
SIGNALS FROM DISK FILE
AA CX AE
TD TB
CONNECT & STATUS
QJ
DATA & SIGNALS TO CHANNEL
L
ZS
DATA TO & FROM DISK FILE
ZT
SIGNALS TO FILE
QI
DATA & SIGNALS FROM CHANNEL
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

PART 5

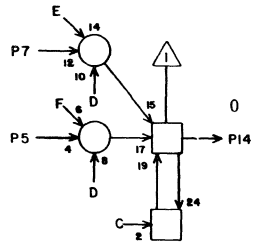
WIRE LISTS

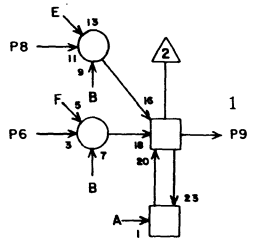
CHASSIS TABS

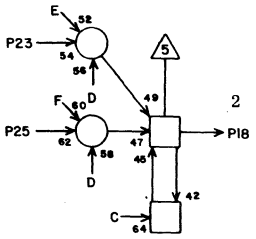
LS 63057800 C
ASSY REV

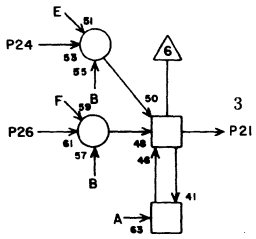
SECTOR COUNTER - STACK 1
RANK 2, BITS 0-3

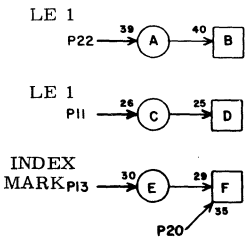
PC

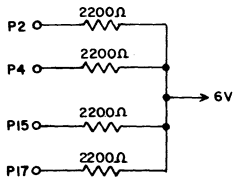












A01

1			
2	A01	8	3
3			
4	A01	23	5
5	A03	9	5
6	A03	24	5
7	K02	23	33
8	A01	2	3
9	A05	13	7
10			
11	B08	24	9
12			
13	D03	20	13
14	A05	14	7
15	A01	24	3
16			
17			
18	A05	18	7
19			
20	A01	X	2
21	A05	17	7
22	B08	22	9
23	A01	4	5
24	A01	15	3
25	A03	20	5
26	A04	9	5
27			
28			

JACK PIN LG

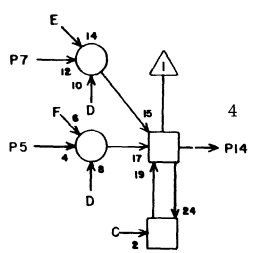
CIRCUIT SPECIFICATION 11827600

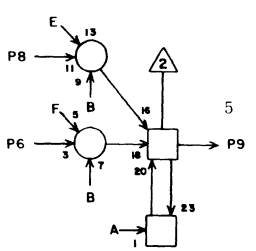
60196300
Rev A

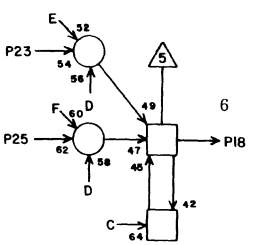
LS 63057800 C
ASSY REV

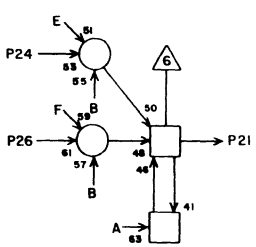
SECTOR COUNTER - STACK 1
RANK 2, BITS 4-6

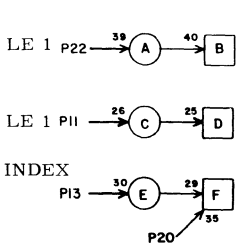
PC

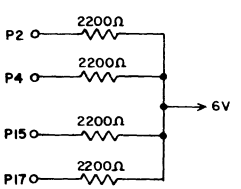












A02

1			
2	A02	7	3
3			
4	A02	8	3
5	A04	24	5
6	A04	20	5
7	A02	2	3
8	A02	4	3
9	A06	13	7
10			
11	F01	22	19
12			
13	D03	22	13
14	A06	14	7
15	A02	23	3
16			
17			
18	A06	18	7
19			
20			
21			
22	F01	21	17
23	A02	15	3
24			
25	A09	21	9
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

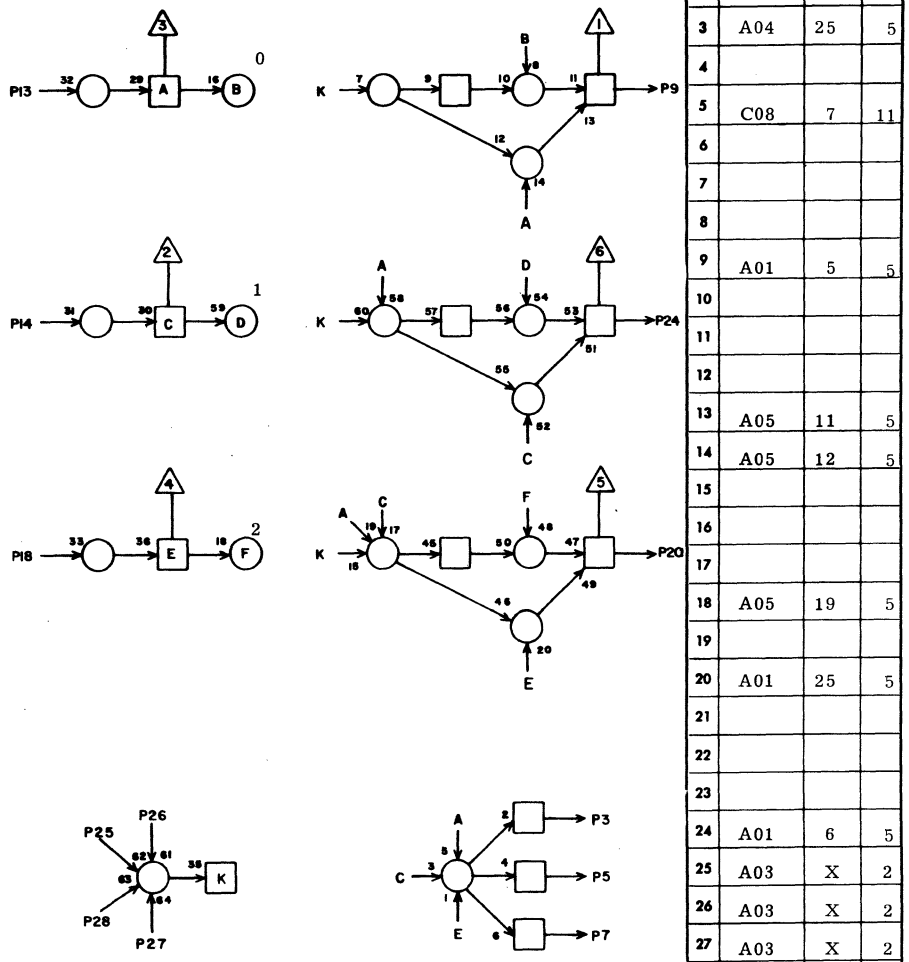
60196300
Rev A

LS 63061000 ASSY | B REV

SECTION COUNTER - STACK 1
INCREMENTOR, BITS 0-2

QK

A03



1			
2			
3	A04	25	5
4			
5	C08	7	11
6			
7			
8			
9	A01	5	5
10			
11			
12			
13	A05	11	5
14	A05	12	5
15			
16			
17			
18	A05	19	5
19			
20	A01	25	5
21			
22			
23			
24	A01	6	5
25	A03	X	2
26	A03	X	2
27	A03	X	2
28	A03	X	2

JACK PIN LG

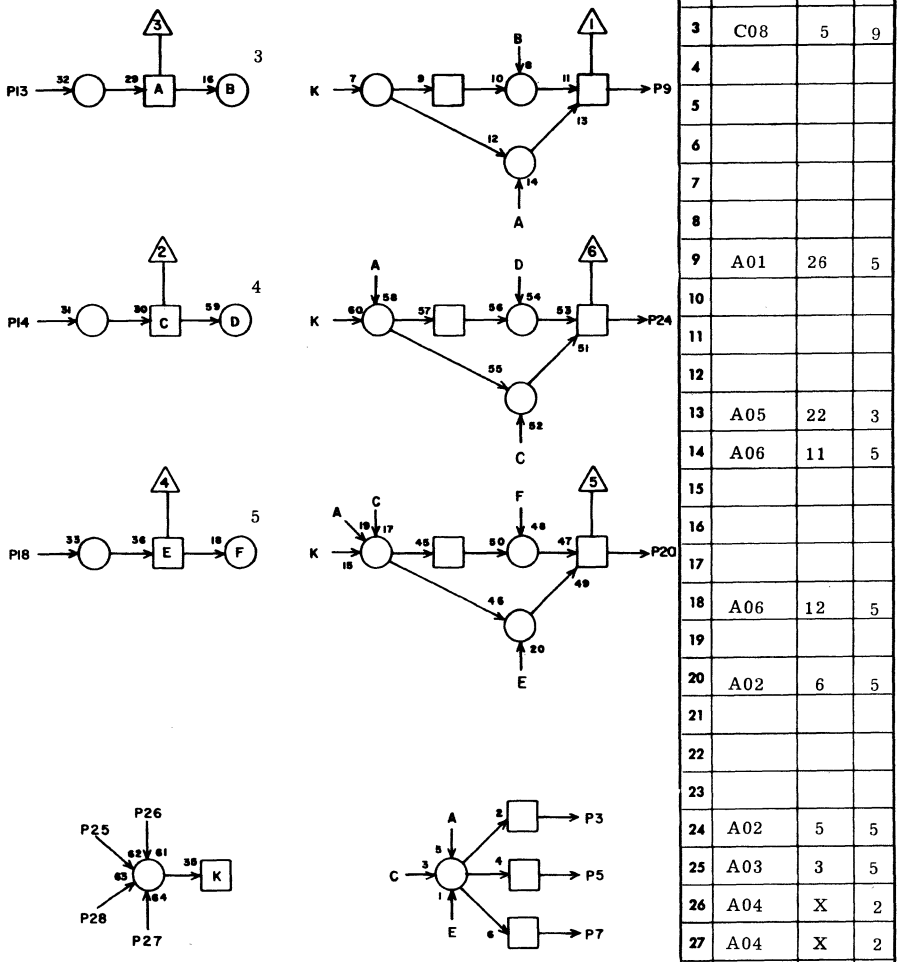
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63061000 ASSY | B REV

SECTION COUNTER - STACK 1
INCREMENTOR, BITS 3-5

QK

A04



1			
2			
3	C08	5	9
4			
5			
6			
7			
8			
9	A01	26	5
10			
11			
12			
13	A05	22	3
14	A06	11	5
15			
16			
17			
18	A06	12	5
19			
20	A02	6	5
21			
22			
23			
24	A02	5	5
25	A03	3	5
26	A04	X	2
27	A04	X	2
28	A04	X	2

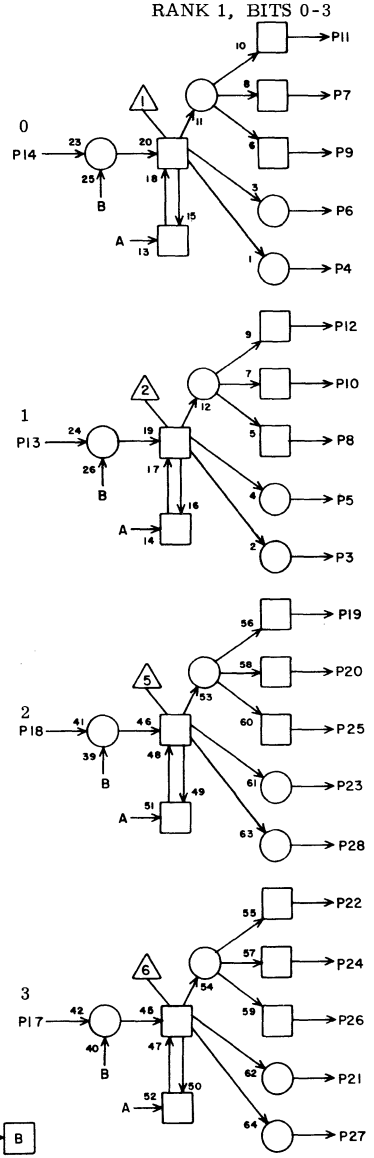
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63057900 ASSY | B REV

SECTOR COUNTER - STACK 1
RANK 1, BITS 0-3

PD



TE 1 P16 → 43 A 44 B

A05

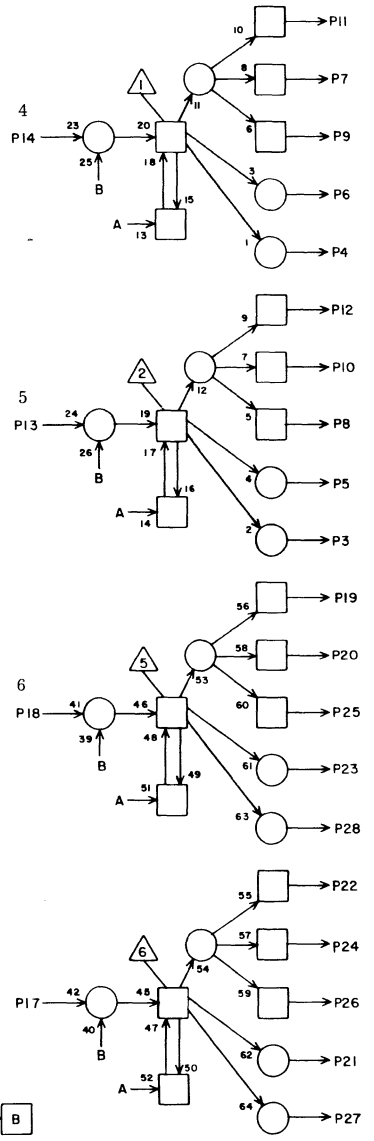
	JACK	PIN	LG
1			
2			
3			
4			
5			
6			
7	A07	4	3
8	H04	6	25
9	H04	8	25
10	A07	3	5
11	A03	13	5
12	A03	14	5
13	A01	9	7
14	A01	14	7
15			
16	B08	21	7
17	A01	21	7
18	A01	18	7
19	A03	18	5
20	A07	13	5
21			
22	A04	13	3
23			
24	A07	18	5
25			
26			
27			
28			

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63057900 ASSY | B REV

SECTOR COUNTER - STACK 1
RANK 1, BITS 4-6

PD



TE 1 P16 → 43 A 44 B

A06

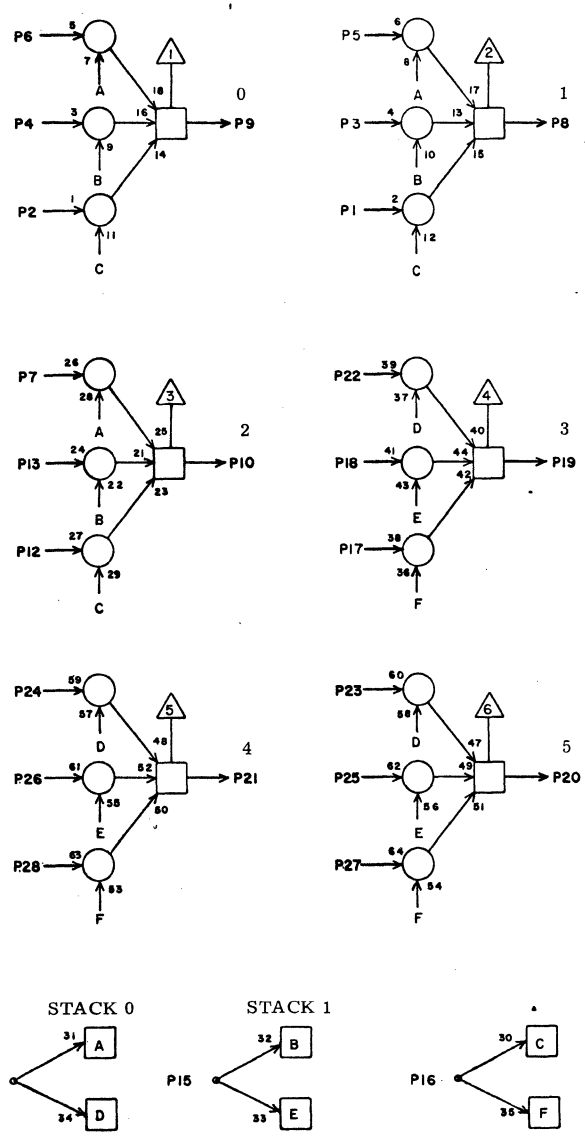
	JACK	PIN	LG
1			
2			
3			
4			
5			
6			
7	A07	26	3
8	H04	4	25
9			
10	A07	25	3
11	A04	14	5
12	A04	18	5
13	A02	9	7
14	A02	14	7
15			
16	B08	23	7
17			
18	A02	18	7
19	D02	22	13
20	A09	24	5
21			
22			
23			
24	H04	2	25
25			
26			
27			
28			

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63063700 ASSY C REV

TE

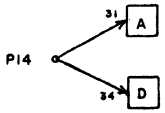
A07



1			
2			
3	A05	10	5
4	A05	7	3
5	B05	10	7
6	B05	7	7
7	B05	20	7
8	B09	6	7
9	B09	1	5
10	B09	3	5
11			
12			
13	A05	20	5
14	G05	19	21
15	G05	23	21
16	A07	X	2
17			
18	A05	24	5
19	B09	26	7
20	B09	28	7
21	B09	25	7
22	B05	24	7
23	B06	10	5
24	B06	7	5
25	A06	10	3
26	A06	7	3
27			
28			

JACK PIN LG

STACK 0



STACK 1

CIRCUIT SPECIFICATION 11827600

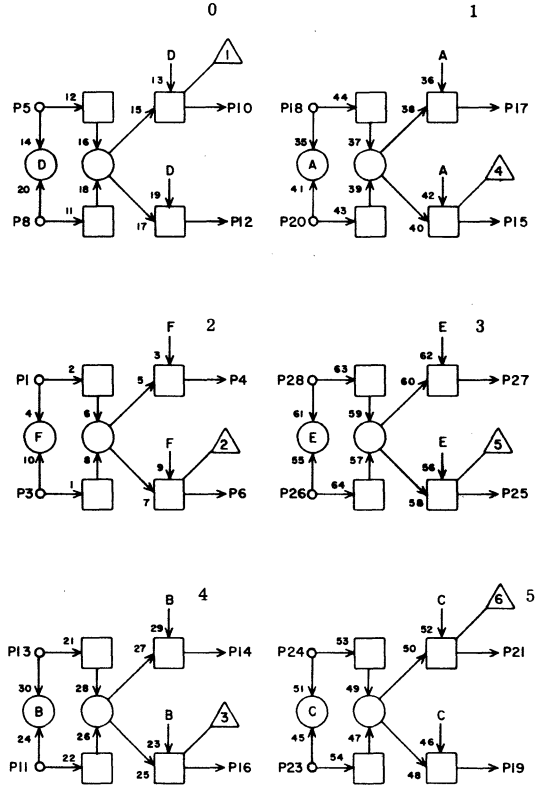
60196300

Rev A

LS 63040100 ASSY E REV

AB

A08



1	B09	2	5
2			
3	C08	13	9
4	C09	5	9
5	B09	14	5
6			
7			
8	C08	14	9
9			
10	C09	1	9
11	F09	18	19
12			
13	B09	16	5
14	C09	9	9
15			
16			
17	C09	3	7
18	B09	5	5
19			
20	C08	19	9
21	C09	11	7
22			
23	C08	18	9
24	B09	22	5
25			
26	C08	16	7
27	C09	7	7
28	B09	23	5

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

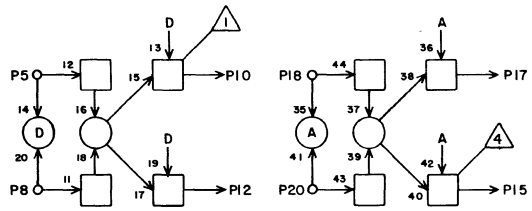
60196300

Rev A

LS 63040100 ASSY | E REV | AB | A09

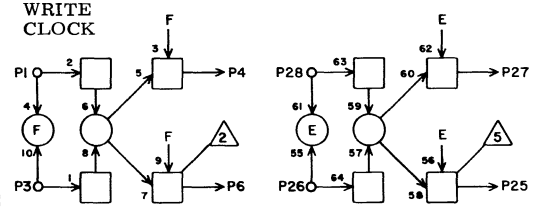
6

HEAD GROUP
NULL DELAY



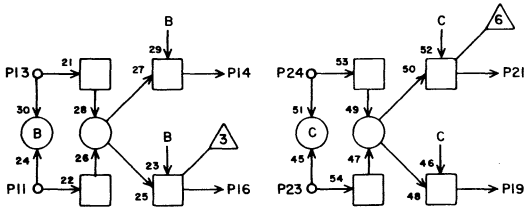
SECTOR COUNTER BIT 6
CARRY 0

WRITE
CLOCK



WRITE ENABLE

BIT COUNTER
CARRY BIT 6



SM BIT 6
CARRY 1

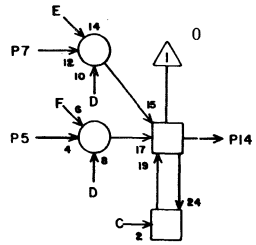
	JACK	PIN	LG
1	F01	2	21
2			
3	F01	9	21
4	I03	7	29
5	B07	16	7
6			
7			
8	H11	26	25
9			
10	C09	2	9
11	C08	9	9
12			
13	C16	18	11
14	C12	18	9
15			
16			
17	D02	13	13
18	F09	13	17
19			
20	C08	15	9
21	A02	25	9
22			
23	C08	11	7
24	A06	20	5
25			
26	C08	10	7
27	B02	25	13
28	B06	20	7

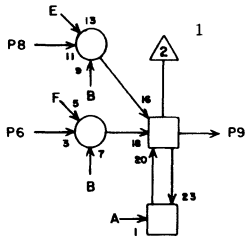
CIRCUIT SPECIFICATION 11827600

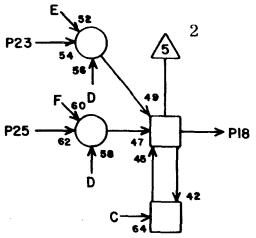
LS 63057800 C
ASSY REV

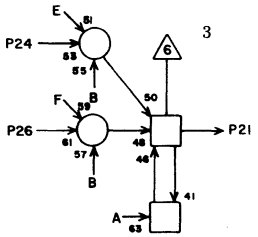
SECTOR COUNTER - STACK 0
RANK 2, BITS 0-3

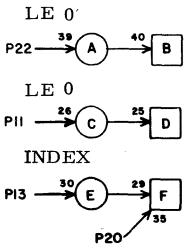
PC

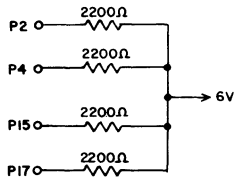












B01

1			
2	B01	8	3
3			
4	B01	23	5
5	B03	9	5
6	B03	24	5
7	K02	4	29
8	B01	2	3
9	B05	13	7
10			
11	B08	4	9
12			
13	D03	14	9
14	B05	14	7
15	B01	24	3
16			
17			
18	B05	18	7
19			
20			
21	B05	17	7
22	B08	2	9
23	B01	4	5
24	B01	15	3
25	B03	20	3
26	B04	9	5
27			
28			

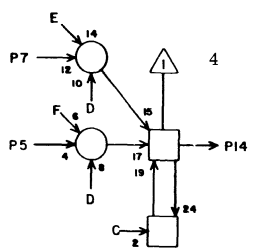
JACK PIN LG

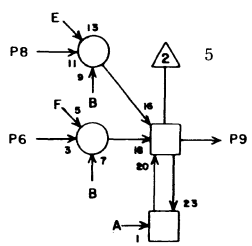
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

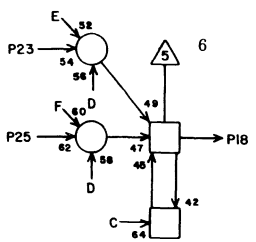
LS 63057800 C
ASSY REV

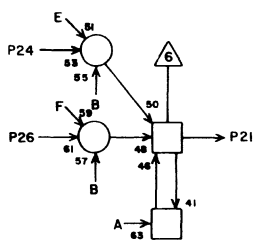
SECTOR COUNTER - STACK 0
RANK 2, BITS 4-6

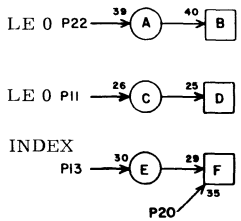
PC

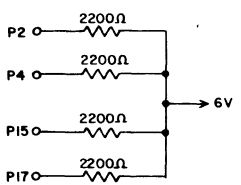












B02

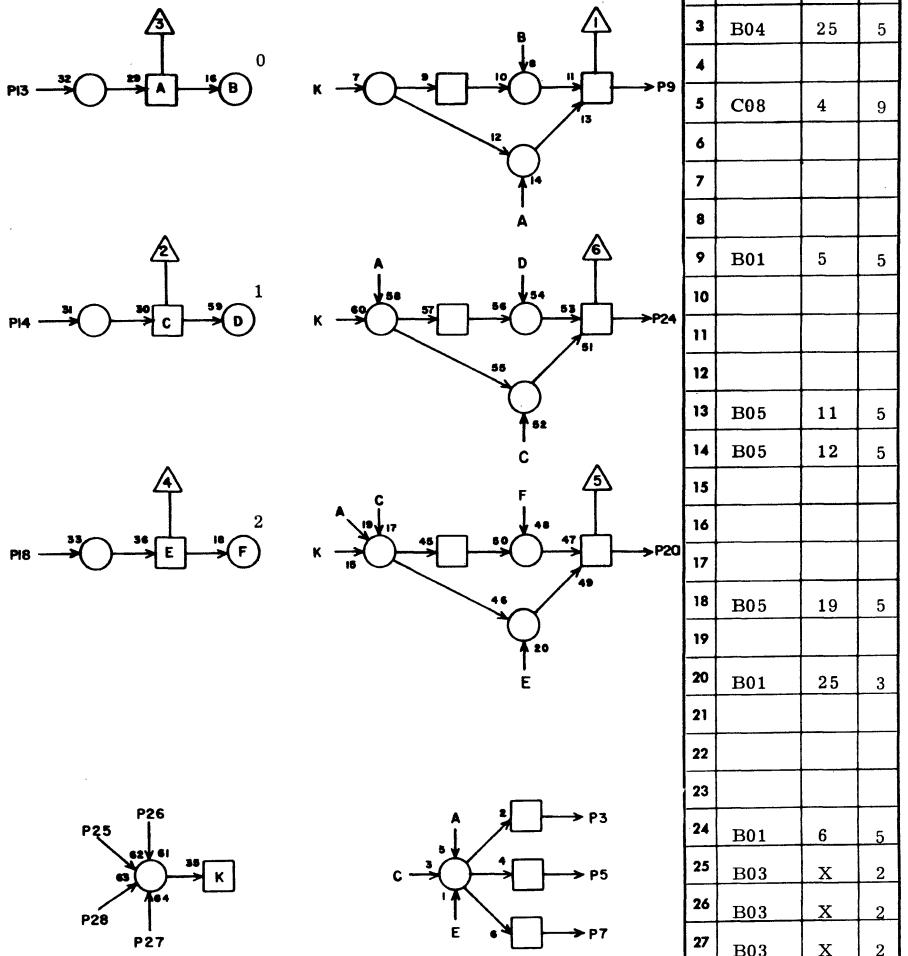
1			
2	B02	7	3
3			
4	B02	8	3
5	B04	24	5
6	B04	20	5
7	B02	2	3
8	B02	4	3
9	B06	13	7
10			
11	F09	19	11
12			
13	D03	16	9
14	B06	14	7
15	B02	23	3
16			
17			
18	B06	18	7
19			
20			
21			
22	F09	23	17
23	B02	15	3
24			
25	A09	27	13
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63061000 ASSY | B REV

SECTION COUNTER - STACK 0 QK
INCREMENTOR, BITS 0-2



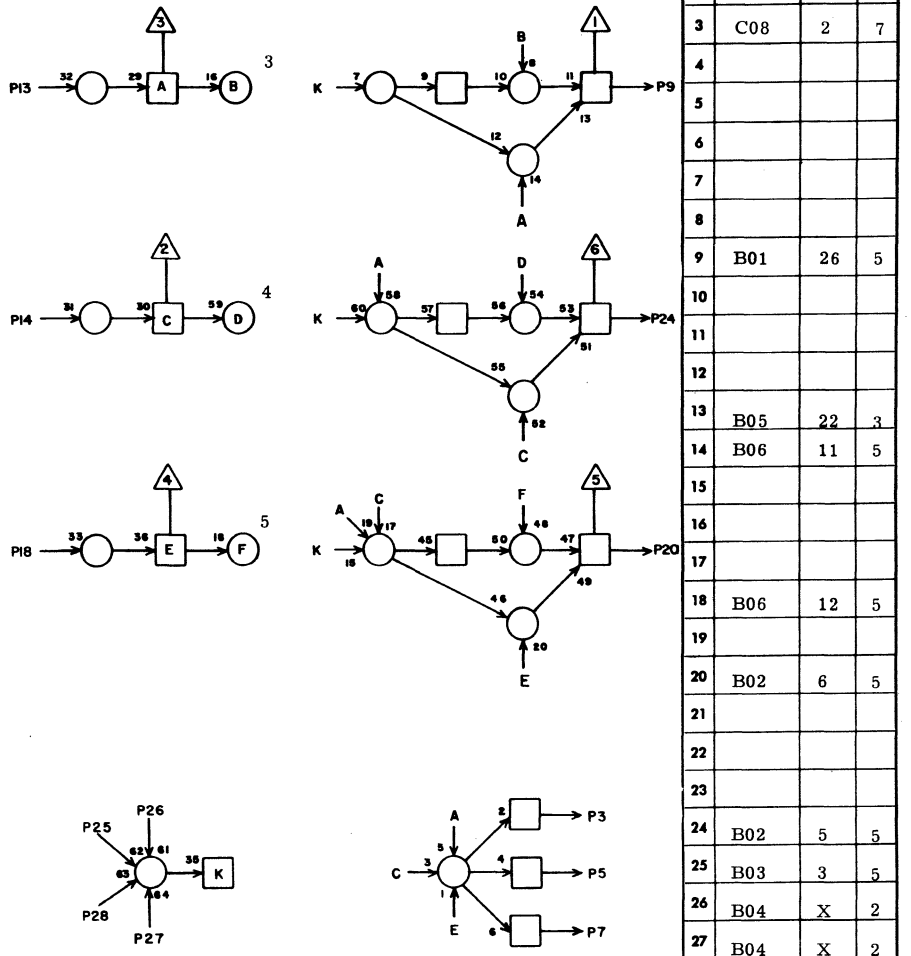
B03

1			
2			
3	B04	25	5
4			
5	C08	4	9
6			
7			
8			
9	B01	5	5
10			
11			
12			
13	B05	11	5
14	B05	12	5
15			
16			
17			
18	B05	19	5
19			
20	B01	25	3
21			
22			
23			
24	B01	6	5
25	B03	X	2
26	B03	X	2
27	B03	X	2
28	B03	X	2
	JACK	PIN	LG

CIRCUIT SPECIFICATION 1182600
60196300
Rev A

LS 63061000 ASSY | B REV

SECTOR COUNTER - STACK 0 QK
INCREMENTOR, BITS 3-5



B04

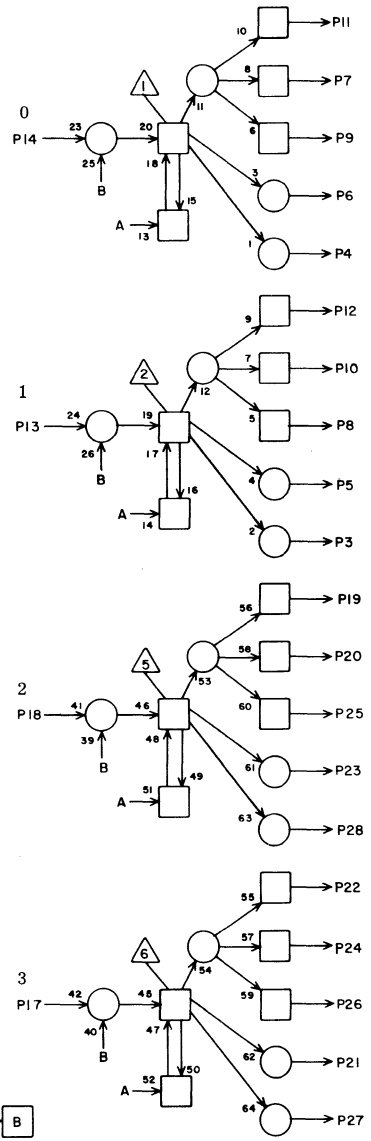
1			
2			
3	C08	2	7
4			
5			
6			
7			
8			
9	B01	26	5
10			
11			
12			
13	B05	22	3
14	B06	11	5
15			
16			
17			
18	B06	12	5
19			
20	B02	6	5
21			
22			
23			
24	B02	5	5
25	B03	3	5
26	B04	X	2
27	B04	X	2
28	B04	X	2
	JACK	PIN	LG

CIRCUIT SPECIFICATION 1182600
60196300
Rev A

LS 63057900 ASSY B REV

SECTOR COUNTER - STACK 0
RANK 1, BITS 0-3

PD



TE 0 P16 → 43 A 44 → B

B05

1			
2			
3			
4			
5			
6			
7	A07	6	7
8	H04	5	23
9	H04	7	23
10	A07	5	7
11	B03	13	5
12	B03	14	5
13	B01	9	7
14	B01	14	7
15			
16	B08	1	5
17	B01	21	7
18	B01	18	7
19	B03	18	5
20	A07	7	7
21			
22	B04	13	3
23			
24	A07	22	7
25			
26			
27			
28			

JACK PIN LG

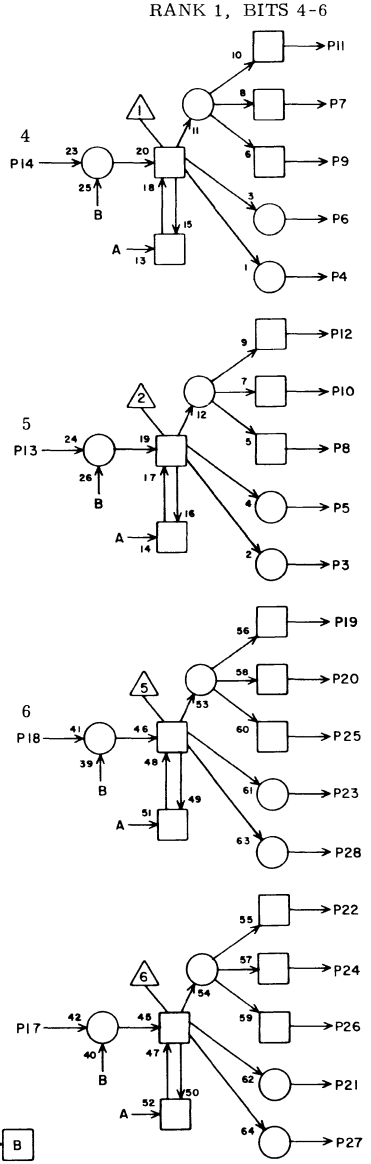
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63057900 ASSY B REV

SECTOR COUNTER - STACK 0
RANK 1, BITS 4-6

PD



TE 0 P16 → 43 A 44 → B

B06

1			
2			
3			
4			
5			
6			
7	A07	24	5
8	H04	3	23
9			
10	A07	23	5
11	B04	14	5
12	B04	18	5
13	B02	9	7
14	B02	14	7
15			
16	B08	3	5
17			
18	B02	18	7
19	D02	20	11
20	A09	28	7
21			
22			
23			
24			
25	H04	1	23
26			
27			
28			

JACK PIN LG

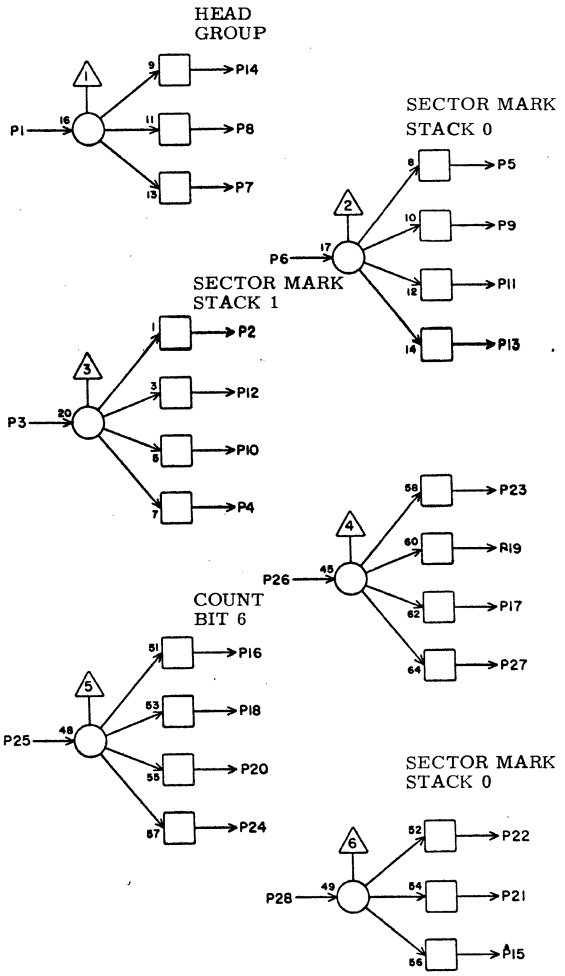
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064000 ASSY (C) REV

TH

B07



1	G07	25	19
2	B08	17	5
3	K02	25	31
4			
5	B08	11	3
6	K02	6	31
7	G04	24	21
8	E13	24	17
9	B07	28	121
10	B08	19	3
11	B08	13	3
12	B07	26	121
13			
14	F12	13	17
15			
16	A09	5	7
17			
18	I12	26	25
19	B08	20	3
20	I15	26	25
21	B08	18	3
22	B08	16	3
23	B08	15	3
24			
25	D02	19	11
26	B07	12	121
27			
28	B07	9	121

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

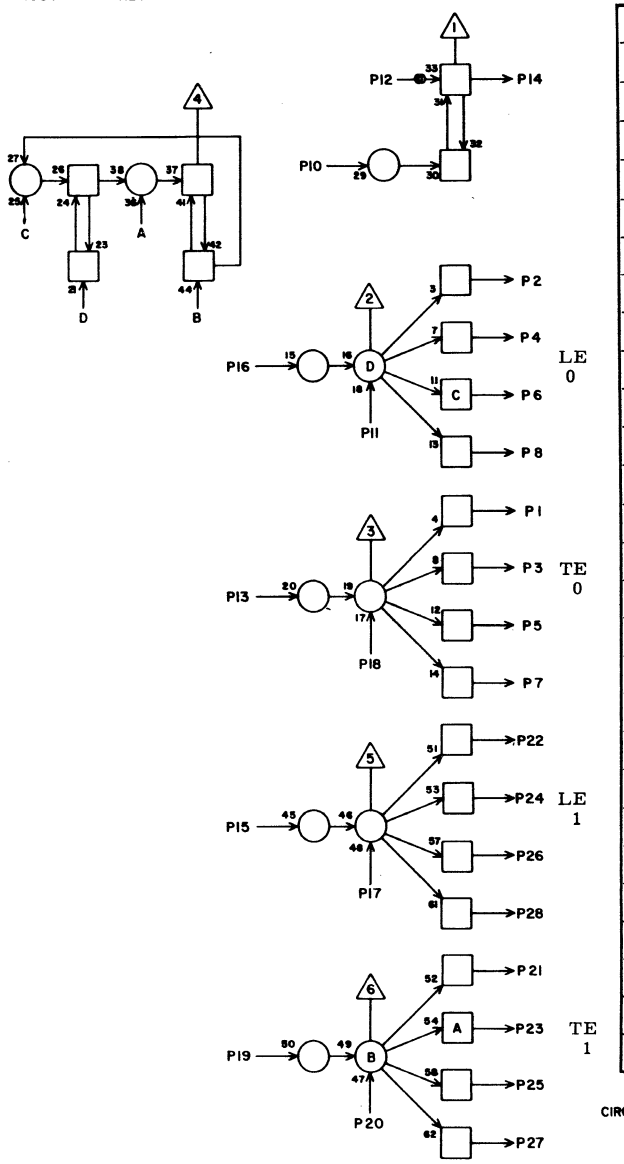
60196200

Rev A

LS 63046200 ASSY (D) REV

HQ

B08



1	B05	16	5
2	B01	22	9
3	B06	16	5
4	B01	11	9
5			
6	D02	23	13
7			
8	F09	26	17
9			
10			
11	B07	5	3
12			
13	B07	11	3
14			
15	B07	23	3
16	B07	22	3
17	B07	2	5
18	B07	21	3
19	B07	10	3
20	B07	19	3
21	A05	16	7
22	A01	22	9
23	A06	16	7
24	A01	11	9
25			
26	D02	25	11
27			
28	F01	28	11

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

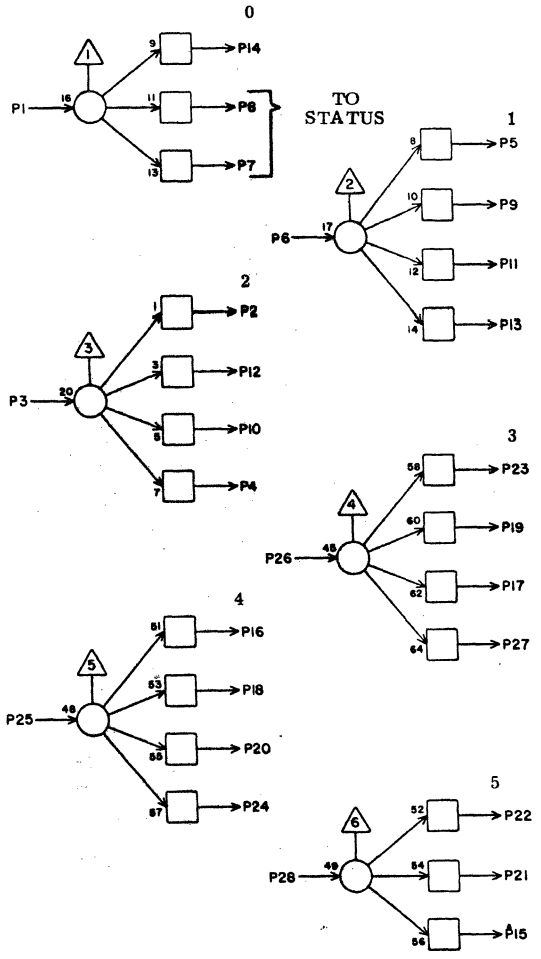
Rev A

LS 63064000 ASSY | REV

TH

B09

SECTOR COUNT



	JACK	PIN	LG
1	A07	9	5
2	A08	1	5
3	A07	10	5
4			
5	A08	18	5
6	A07	8	7
7	I14	4	23
8	I11	4	25
9	I11	3	25
10	I14	26	25
11	I14	3	23
12	I11	26	25
13			
14	A08	5	5
15	I15	3	23
16	A08	13	5
17	I14	25	25
18	I12	4	25
19	I11	25	25
20	I15	4	23
21	I12	3	23
22	A08	24	5
23	A08	28	5
24			
25	A07	21	7
26	A07	19	7
27			
28	A07	20	7

CIRCUIT SPECIFICATION 11827600

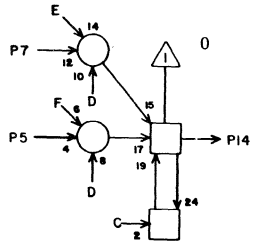
60196300
Rev A

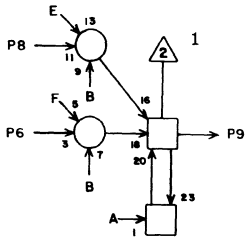
LS 63057800 C
ASSY REV

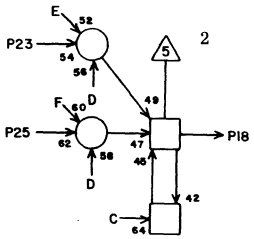
POSITION COUNTER
RANK 1, BITS 0-3

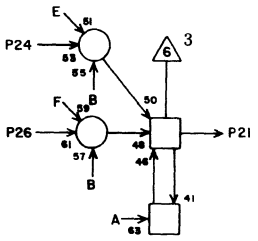
PC

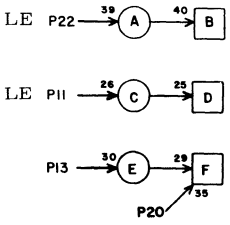
C01

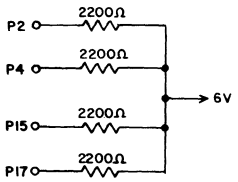












	JACK	PIN	LG
1			
2			
3			
4			
5	C01	X	2
6	C01	X	2
7	C05	1	7
8	C05	2	7
9	C03	14	5
10			
11	E03	24	9
12			
13	D04	14	7
14	C03	13	5
15			
16			
17			
18	C03	18	5
19			
20	C01	X	2
21	C04	13	5
22	E03	22	9
23	C05	14	7
24	C05	19	7
25	C01	X	2
26	C01	X	2
27			
28			

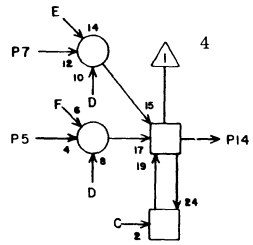
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

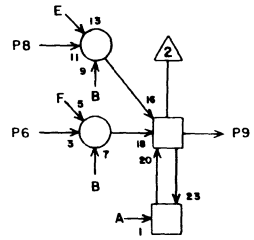
LS 63057800 C
ASSY REV

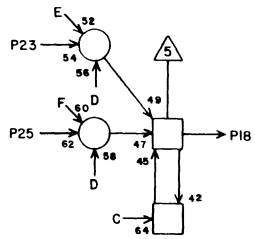
POSITION COUNTER
RANK 1, BIT 4

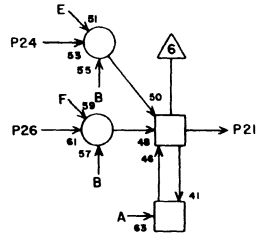
PC

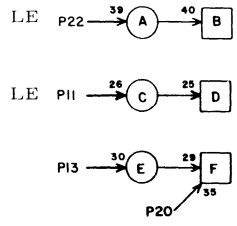
C02

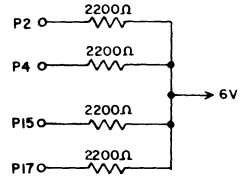












	JACK	PIN	LG
1			
2	E03	15	9
3			
4			
5	C02	X	2
6	C02	X	2
7	C05	27	7
8			
9			
10			
11	E03	28	9
12			
13	D04	16	7
14	C04	14	5
15			
16			
17	D02	6	5
18			
19			
20	C02	X	2
21			
22	E03	26	9
23			
24			
25	C02	X	2
26	C02	X	2
27			
28			

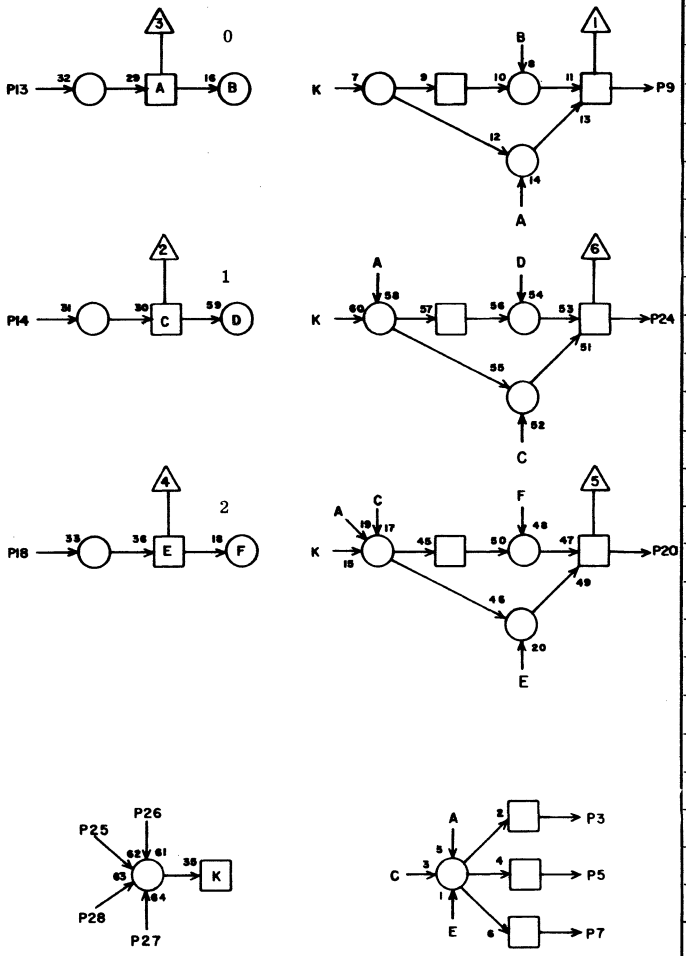
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63061000 ASSY | B REV

POSITION COUNTER INCREMENTOR, BITS 0-2

QK

C03



1			
2			
3	C04	25	5
4			
5			
6			
7			
8			
9	C05	8	5
10			
11			
12			
13	C01	14	5
14	C01	9	5
15			
16			
17			
18	C01	18	5
19			
20	C05	12	5
21			
22			
23			
24	C05	5	5
25	C03	X	2
26	C03	X	2
27	C03	X	2
28	C03	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

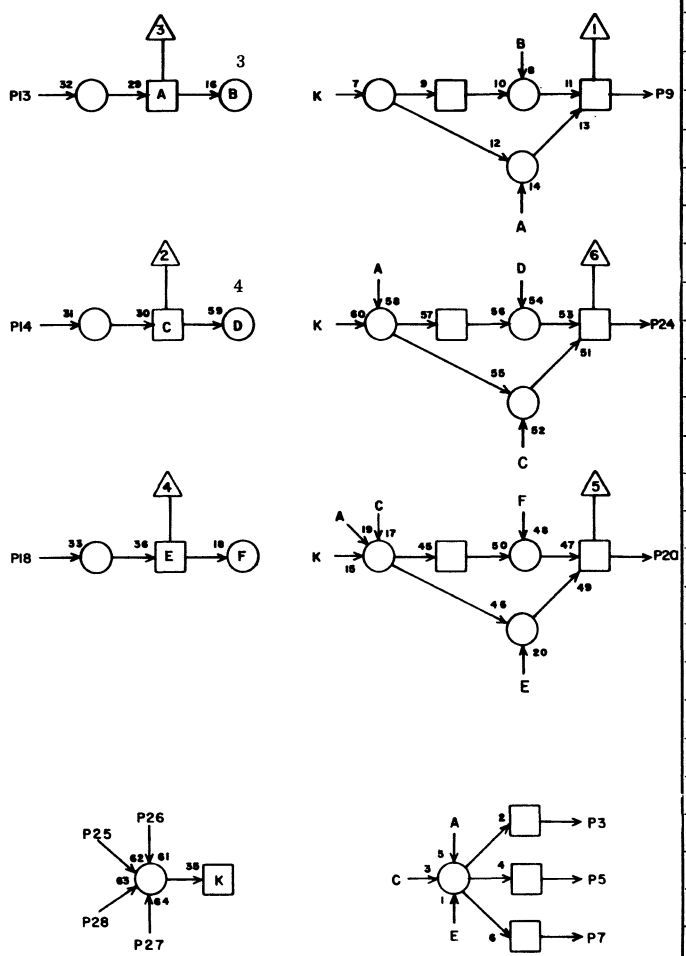
Rev A

LS 63061000 ASSY | B REV

POSITION COUNTER INCREMENTOR, BITS 3 & 4

QK

C04



1			
2			
3			
4			
5			
6			
7			
8			
9	C05	21	3
10			
11			
12			
13	C01	21	5
14	C02	14	5
15			
16			
17			
18			
19			
20			
21			
22			
23			
24	C05	24	3
25	C03	3	5
26	C04	X	2
27	C04	X	2
28	C04	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

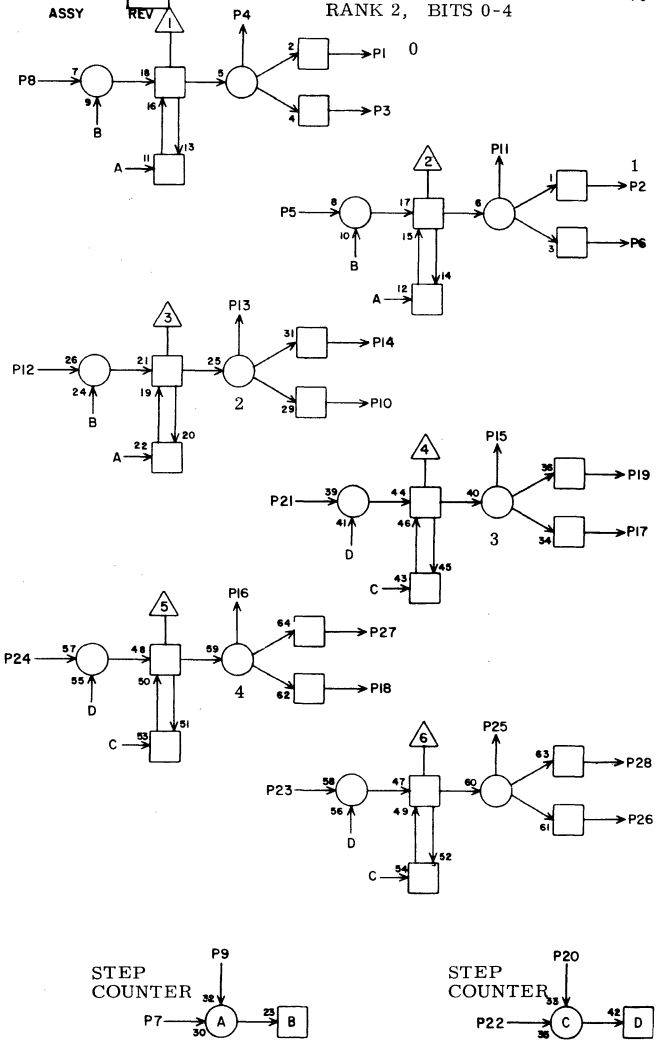
60196300

Rev A

LS 63058400 ASSY E REV 1

POSITION COUNTER RANK 2, BITS 0-4

PJ



C05

	JACK	PIN	LG
1	C01	7	7
2	C01	8	7
3	D06	10	5
4	D06	8	5
5	C03	24	5
6	D06	1	5
7	D04	20	7
8	C03	9	5
9	C05	X	2
10	D06	12	5
11	D06	4	5
12	C03	20	5
13	D06	19	7
14	C01	23	7
15	D06	28	7
16	D06	27	7
17	D06	21	7
18	D06	26	7
19	C01	24	7
20	C05	X	2
21	C04	9	3
22	D04	22	5
23			
24	C04	24	3
25			
26			
27	C02	7	7
28			

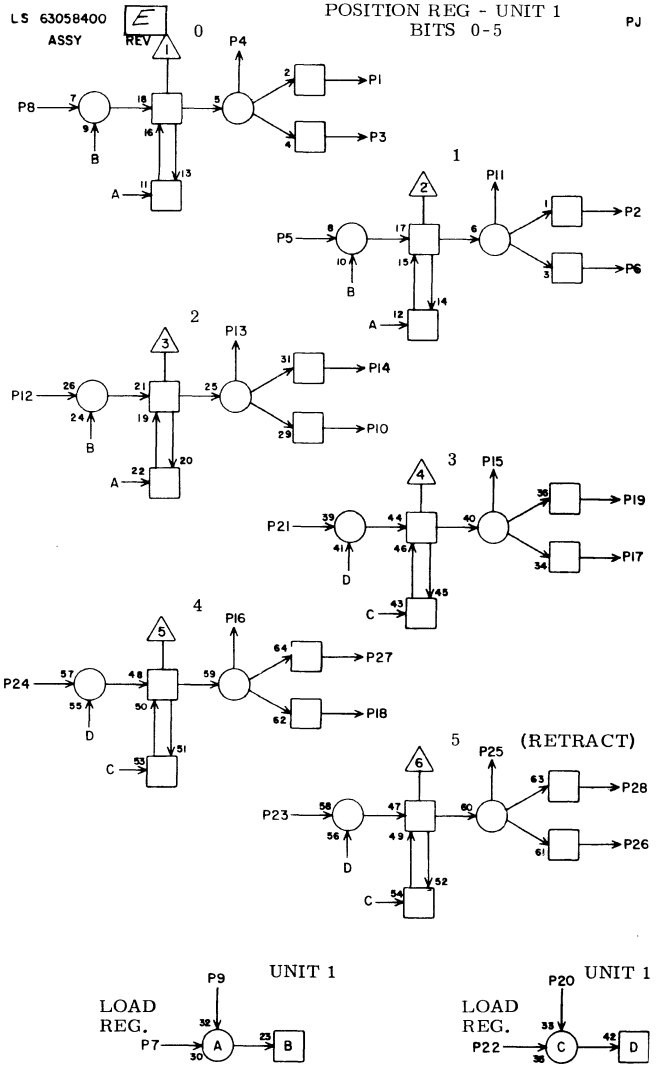
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63058400 ASSY E REV 1

POSITION REG - UNIT 1 BITS 0-5

PJ



C06

	JACK	PIN	LG
1	I12	22	23
2	I12	21	23
3	I15	22	25
4	C07	4	3
5	H10	7	19
6	I15	21	25
7	G11	21	17
8	H10	8	19
9	C10	15	7
10	I16	8	25
11	C07	3	3
12	H10	24	19
13	C07	13	3
14	I13	8	23
15	C07	18	3
16	C07	26	3
17	I16	7	25
18	I16	22	25
19	I13	7	21
20	C10	17	7
21	H10	23	19
22	G11	23	17
23	H11	7	17
24	F09	16	11
25			
26	I16	21	25
27	I13	22	21
28	I13	21	21

CIRCUIT SPECIFICATION 11827600

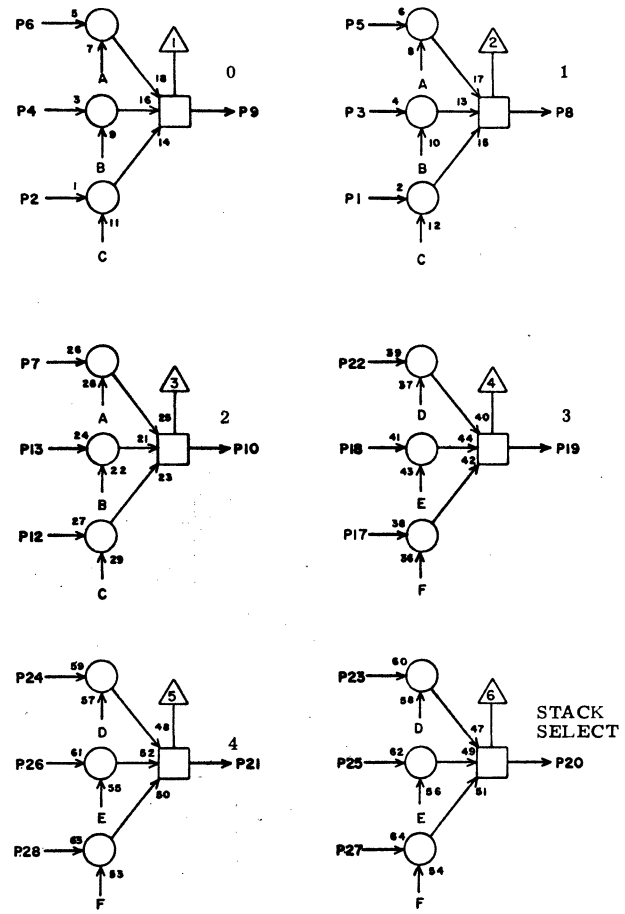
60196300
Rev A

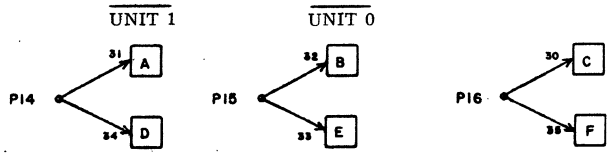
LS 63063700 ASSY — REV C

POSITION ADDRESS BITS 0-4

TE

C07





1			
2			
3	C06	11	3
4	C06	4	3
5	D05	11	7
6	D05	4	7
7	D05	13	7
8	D06	6	5
9	D06	7	5
10	D06	11	5
11			
12			
13	C06	13	3
14	C10	19	5
15	C10	10	5
16	C07	X	2
17			
18	C06	15	3
19	D06	22	5
20	F09	6	11
21	D06	25	7
22	D05	15	5
23	D10	1	5
24	D05	16	5
25	D10	26	7
26	C06	16	3
27			
28			

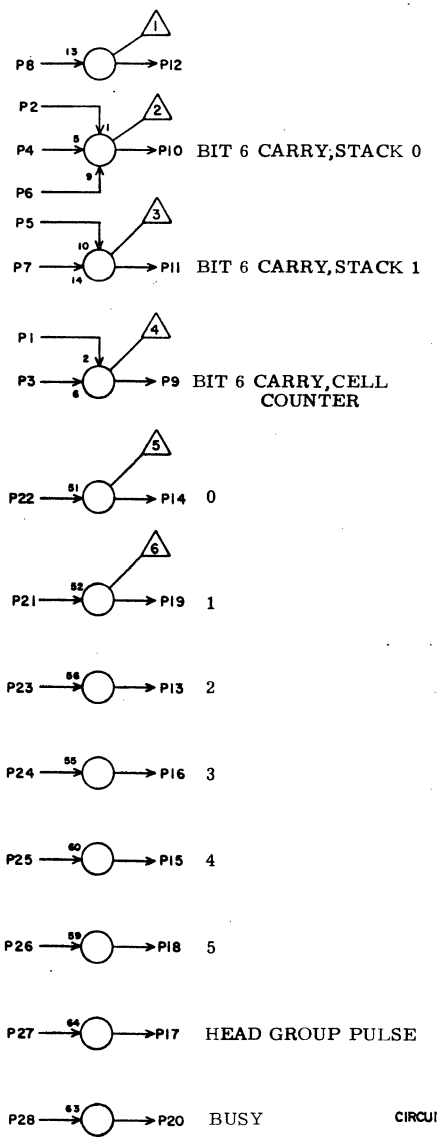
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63064400 ASSY — REV C

TL

C08



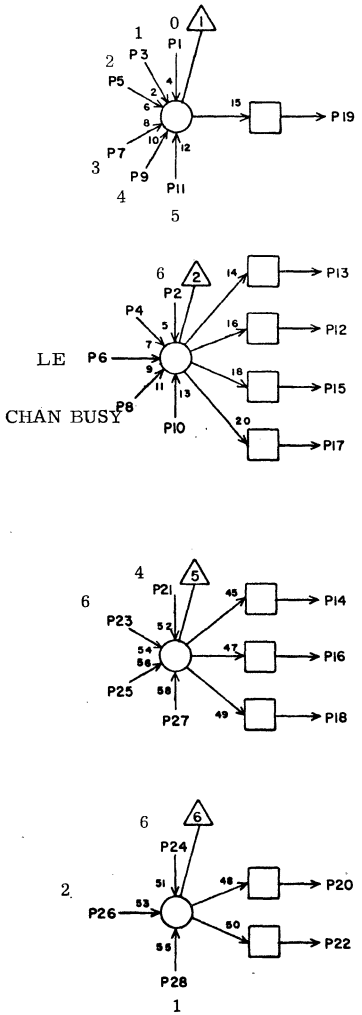
1	C13	5	7
2	B04	3	7
3	C14	3	9
4	B03	5	9
5	A04	3	9
6	C08	X	2
7	A03	5	11
8			
9	A09	11	9
10	A09	26	7
11	A09	23	7
12			
13	A08	3	9
14	A08	8	9
15	A09	20	9
16	A08	26	7
17	D07	21	5
18	A08	23	9
19	A08	20	9
20	G01	23	19
21	H10	10	17
22	H10	9	17
23	H10	21	17
24	H10	22	17
25	F09	15	11
26	H11	10	17
27	F06	9	11
28	F01	17	17

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63063400 ASSY | REV

TB | C09

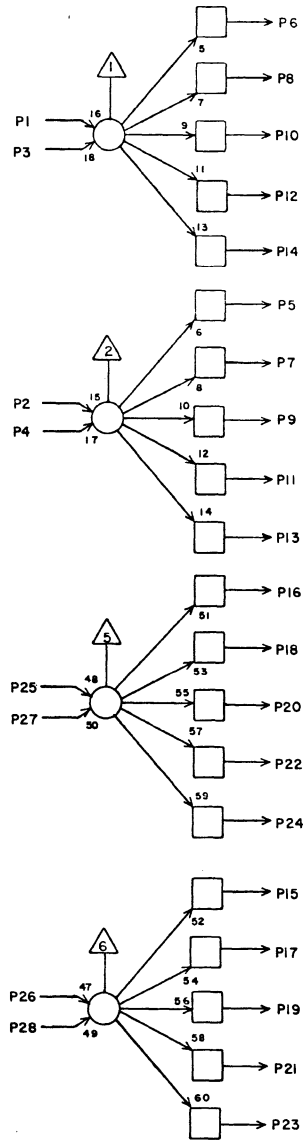


	JACK	PIN	LG
1	A08	10	9
2	A09	10	9
3	A08	17	7
4	C09	19	3
5	A08	4	9
6	D02	28	11
7	A08	27	7
8	C10	24	3
9	A08	14	9
10	C09	X	2
11	A08	21	7
12			
13	E08	5	9
14	F06	16	13
15	H13	24	19
16			
17			
18			
19	C09	4	3
20	E12	26	9
21	C12	7	5
22			
23	C12	20	5
24	C12	25	5
25	C09	X	2
26	C11	20	5
27	C09	X	2
28	C11	10	5

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63063600 ASSY | C REV

TD | C10



	JACK	PIN	LG
1	D10	9	7
2	E12	16	11
3	C10	X	2
4	E08	1	9
5	G07	2	19
6	D05	9	9
7	E08	22	9
8	D05	20	9
9			
10	C07	15	5
11	E09	26	9
12	E13	28	11
13			
14	L06	12	29
15	C06	9	7
16	H13	2	17
17	C06	20	7
18	F08	13	13
19	C07	14	5
20	G04	4	17
21	G04	28	17
22	G12	15	15
23	L06	9	29
24	C09	8	3
25	H05	1	17
26	D10	2	3
27	C10	X	2
28	C10	X	2

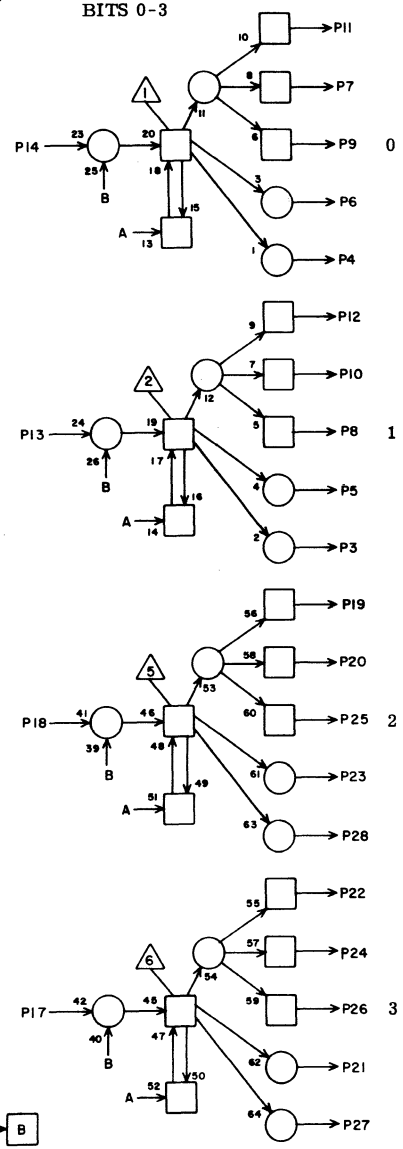
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63057900 ASSY | B REV

CELL COUNTER BITS 0-3

PD

C11



1			
2			
3			
4			
5			
6			
7			
8			
9	F07	25	15
10	C09	28	5
11	C15	5	7
12	C15	6	7
13	C13	24	3
14	C13	9	5
15			
16	E06	16	11
17	C14	9	5
18	C13	20	5
19	C15	25	7
20	C09	26	5
21			
22	C15	26	7
23			
24			
25			
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

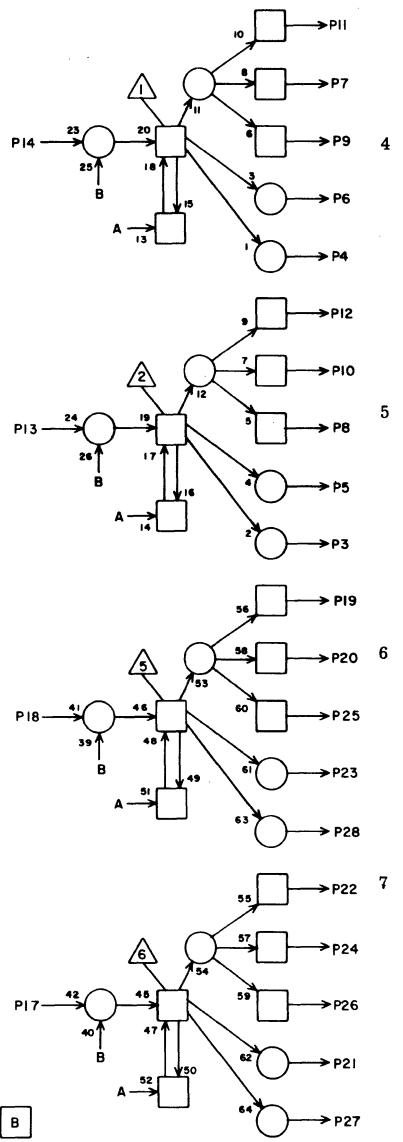
t3 P16 43 A 44 B

LS 63057900 ASSY | B REV

CELL COUNTER BITS 4-7

PD

C12



1			
2			
3			
4			
5			
6			
7	C09	21	5
8	G08	6	15
9	G08	8	17
10			
11	C16	5	7
12	C16	6	7
13	C14	20	3
14	C14	24	5
15			
16	E06	18	11
17			
18	A09	14	9
19	C16	25	7
20	C09	23	5
21			
22			
23	E09	24	11
24			
25	C09	24	5
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

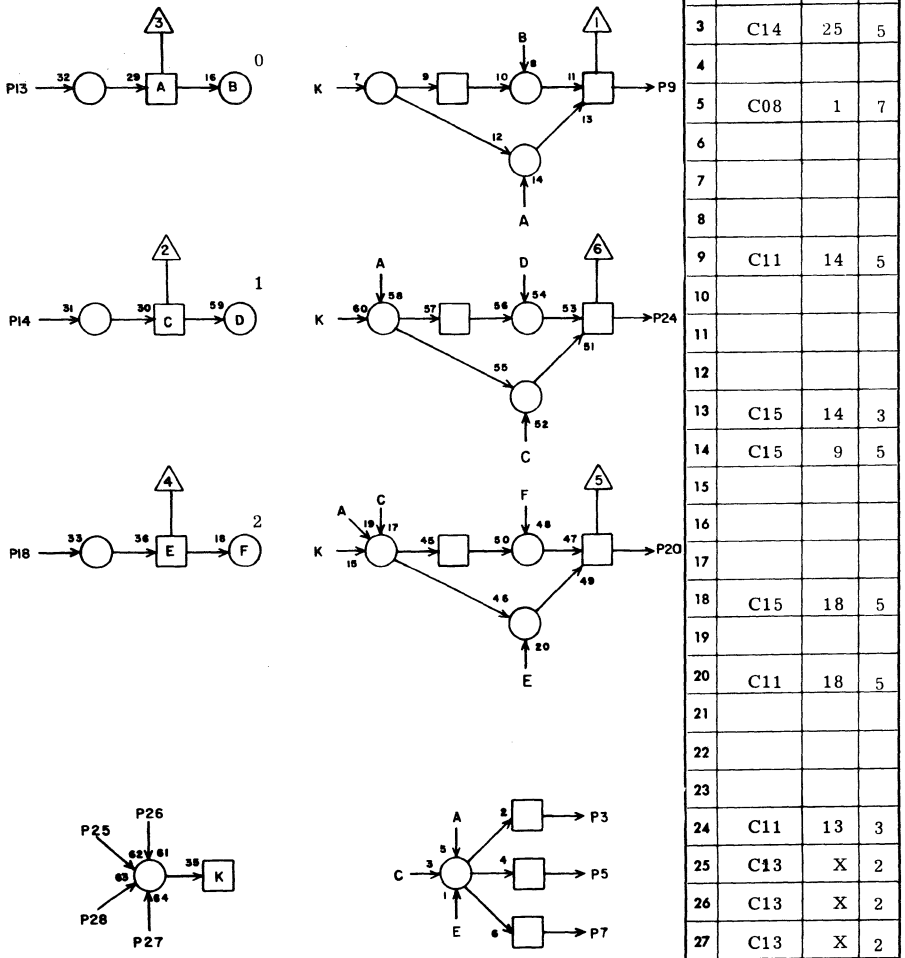
60196300
Rev A

t3 P16 43 A 44 B

LS 63061000 ASSY | B REV

CELL COUNTER
(BIT COUNTER)
BITS 0-2

QK



C13

1			
2			
3	C14	25	5
4			
5	C08	1	7
6			
7			
8			
9	C11	14	5
10			
11			
12			
13	C15	14	3
14	C15	9	5
15			
16			
17			
18	C15	18	5
19			
20	C11	18	5
21			
22			
23			
24	C11	13	3
25	C13	X	2
26	C13	X	2
27	C13	X	2
28	C13	X	2

JACK PIN LG

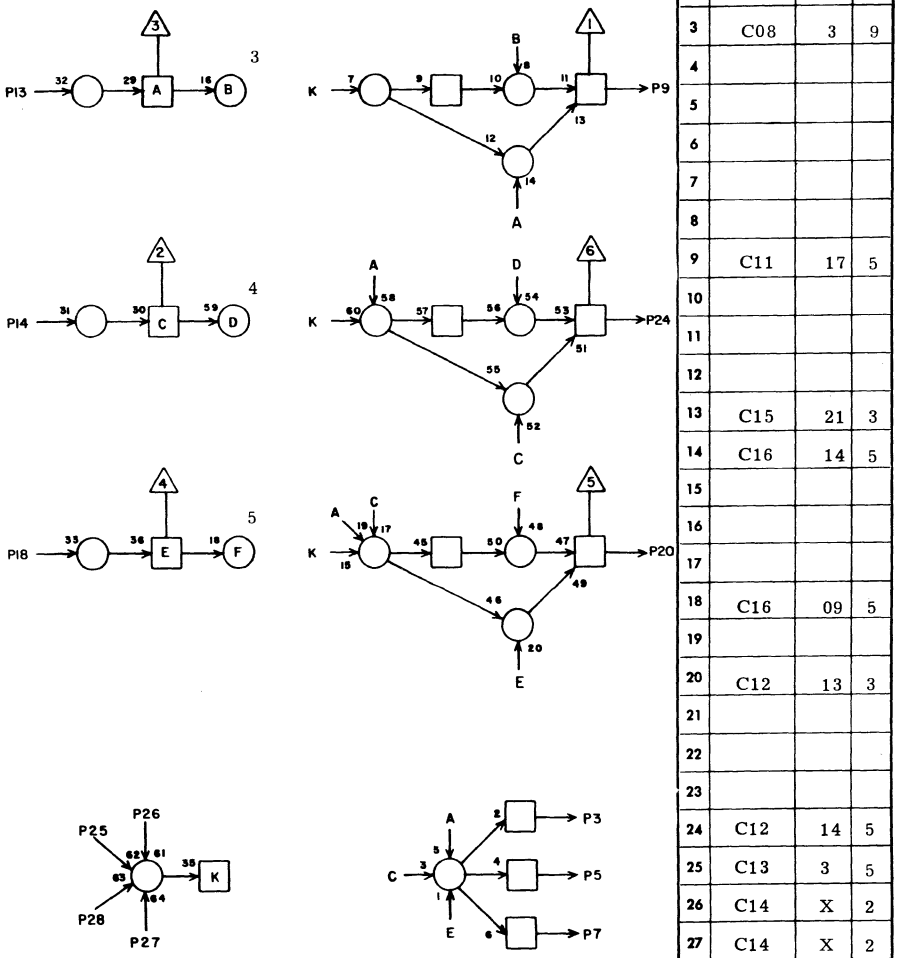
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63061000 ASSY | B REV

CELL COUNTER
(BIT COUNTER)
BITS 3-5

QK



C14

1			
2			
3	C08	3	9
4			
5			
6			
7			
8			
9	C11	17	5
10			
11			
12			
13	C15	21	3
14	C16	14	5
15			
16			
17			
18	C16	09	5
19			
20	C12	13	3
21			
22			
23			
24	C12	14	5
25	C13	3	5
26	C14	X	2
27	C14	X	2
28	C14	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

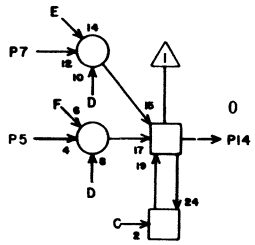
60196300
Rev A

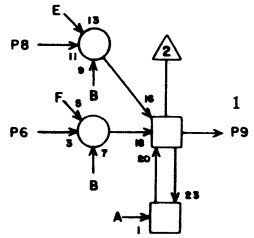
LS 63057800 C
ASSY REV

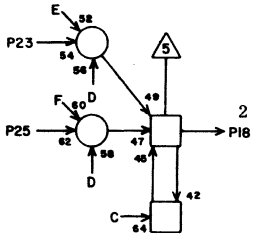
CELL COUNTER
BITS 0-3

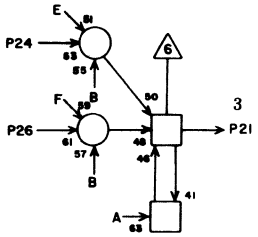
PC

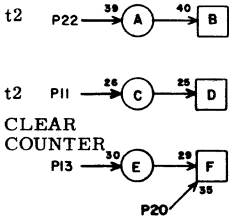
C15

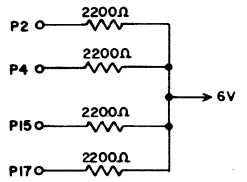












1			
2	I11	12	21
3			
4	I12	12	21
5	C11	11	7
6	C11	12	7
7	C15	X	2
8	C15	X	2
9	C13	14	5
10			
11	E06	13	13
12			
13	D12	16	7
14	C13	13	3
15	I13	12	21
16			
17	I14	12	21
18	C13	18	5
19			
20	C15	X	2
21	C14	13	3
22	E06	11	13
23	C15	X	2
24	C15	X	2
25	C11	19	7
26	C11	22	7
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

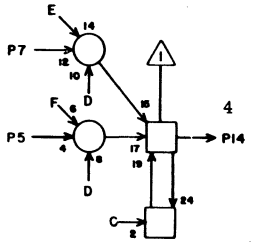
60196300
Rev A

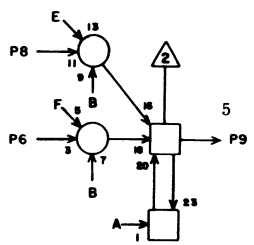
LS 63057800 C
ASSY REV

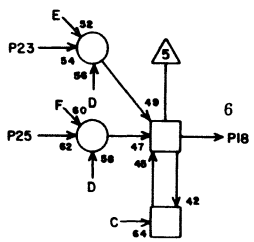
CELL COUNTER
BITS 4-7

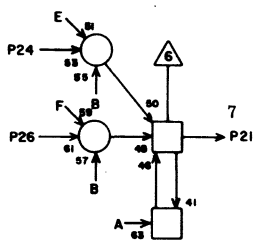
PC

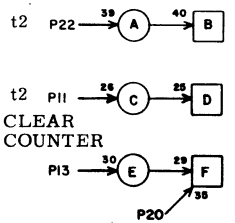
C16

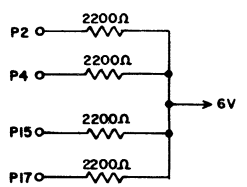












1			
2	I15	12	21
3			
4	I16	12	21
5	C12	11	7
6	C12	12	7
7	C16	X	2
8	C16	X	2
9	C14	18	5
10			
11	E06	10	15
12			
13	D12	14	7
14	C14	14	5
15	I09	9	23
16			
17			
18	A09	13	11
19			
20	C16	X	2
21			
22	E06	8	13
23	C16	X	2
24			
25	C12	19	7
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

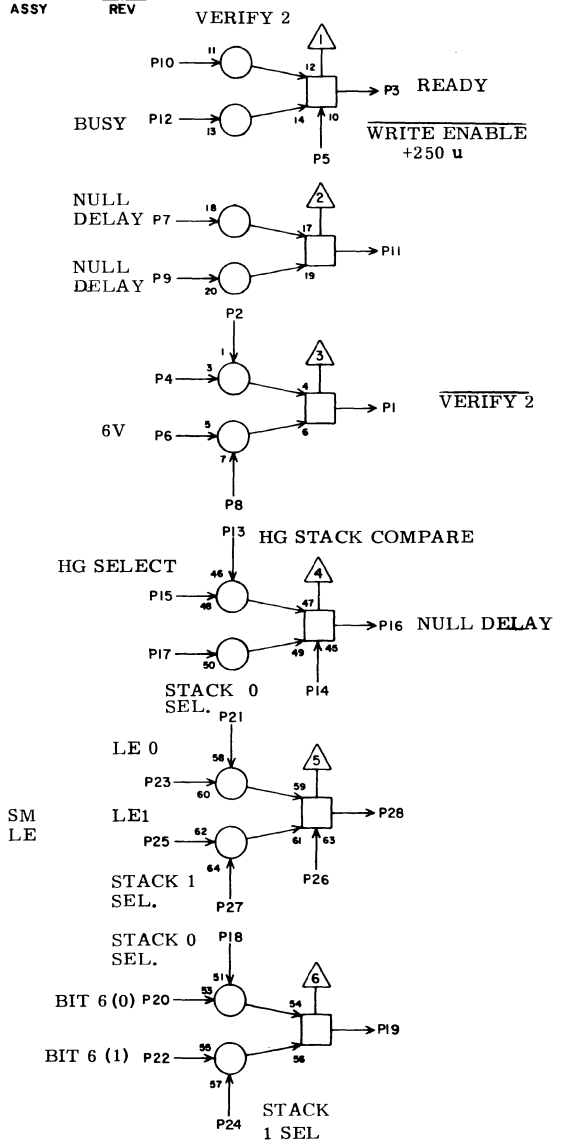
60196300
Rev A

LS 63060700 ASSY

REV C

QH

D02



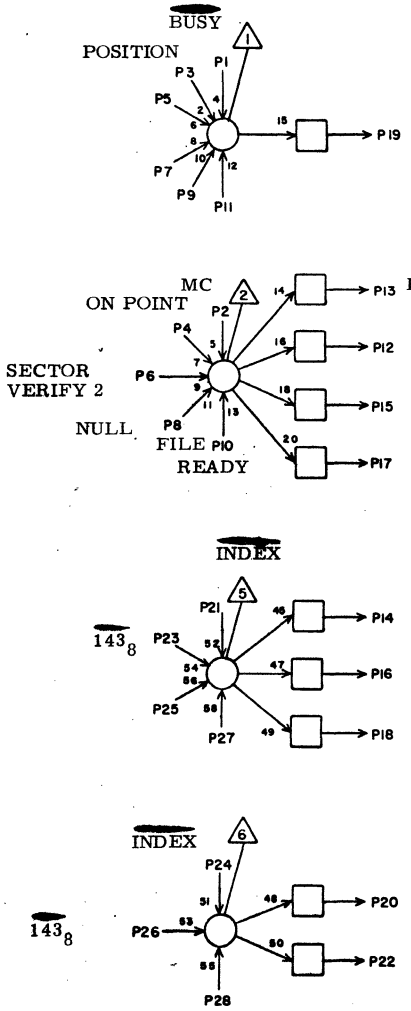
	JACK	PIN	LG
1	D07	12	7
2	D07	1	7
3	D03	6	3
4	F07	19	11
5	D09	24	9
6	C02	17	5
7	D08	28	9
8	D02	X	2
9	F04	21	9
10	D07	10	7
11	D08	21	9
12	E09	20	11
13	A09	17	13
14	D02	X	2
15	F12	10	13
16	F04	28	9
17	D08	3	9
18	G06	23	13
19	B07	25	11
20	B06	19	11
21	G06	28	13
22	A06	19	13
23	B08	06	13
24	G06	20	13
25	B08	26	11
26	D02	X	2
27	G06	25	13
28	C09	6	11

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63063400 ASSY ? REV

TB D03



1	E03	25	7
2	F04	16	9
3	G03	5	11
4	E01	21	7
5	E01	15	7
6	D02	3	3
7	G13	18	19
8	G13	16	19
9	D03	X	2
10	K01	4	23
11	D03	X	2
12	E12	25	13
13	G04	25	13
14	B01	13	9
15			
16	B02	13	9
17	F07	23	11
18			
19	D08	12	7
20	A01	13	13
21	K02	3	23
22	A02	13	13
23	H04	13	17
24	K02	18	23
25	D03	X	2
26	H04	9	17
27	D03	X	2
28	D03	X	2

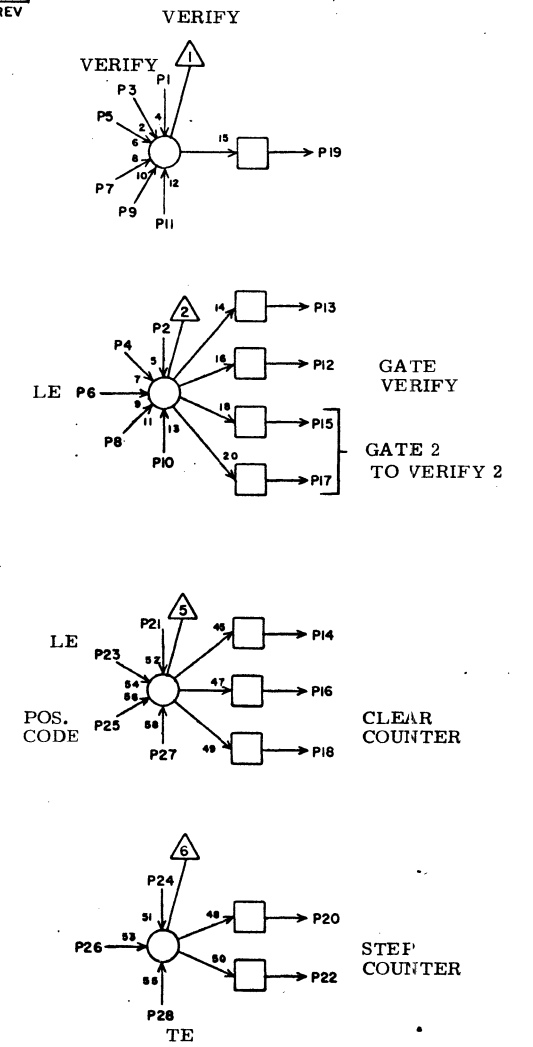
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63063400 ASSY ? REV

TB D04



1	D06	14	5
2	E02	10	7
3	D07	8	7
4	E01	19	7
5	D04	X	2
6	E03	4	5
7	D04	X	2
8	E02	28	7
9	D04	X	2
10	D04	X	2
11	D04	X	2
12	E01	25	121
13	E02	16	121
14	C01	13	7
15	D07	7	5
16	C02	13	7
17	D07	14	5
18	E02	17	121
19	D07	11	7
20	C05	7	7
21	E02	19	7
22	C05	22	5
23	E03	6	5
24	E01	11	7
25	E01	9	7
26	E02	26	7
27	E02	1	5
28	E03	5	5

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

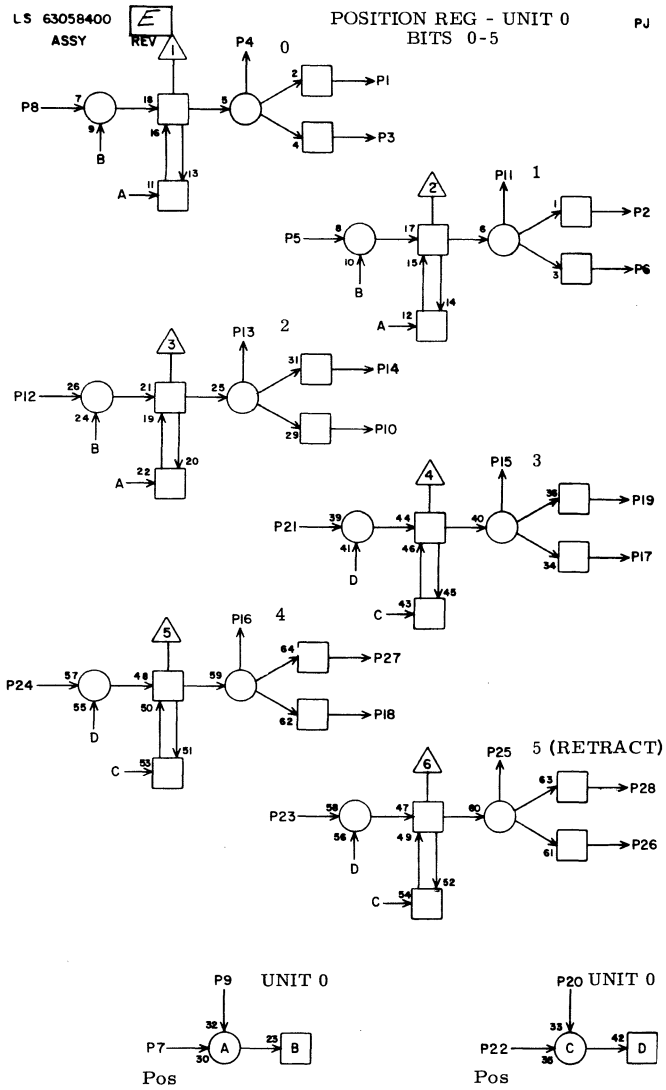
60196300
Rev A

LS 63058400 ASSY — REV E

POSITION REG - UNIT 0
BITS 0-5

PJ

D05



P9 UNIT 0

Pos

P20 UNIT 0

Pos

1	I11	8	19
2	I11	7	19
3	I14	8	21
4	C07	6	7
5	H10	5	15
6	I14	7	21
7	G11	17	15
8	H10	6	15
9	C10	6	9
10	I14	22	19
11	C07	5	7
12	H10	26	17
13	C07	7	7
14	I11	22	19
15	C07	22	5
16	C07	24	5
17	I14	21	21
18	I15	8	21
19	I11	21	19
20	C10	8	9
21	H10	25	15
22	G11	19	13
23	H11	5	17
24	F09	24	11
25			
26	I15	7	19
27	I12	8	19
28	I12	7	19

JACK PIN LG

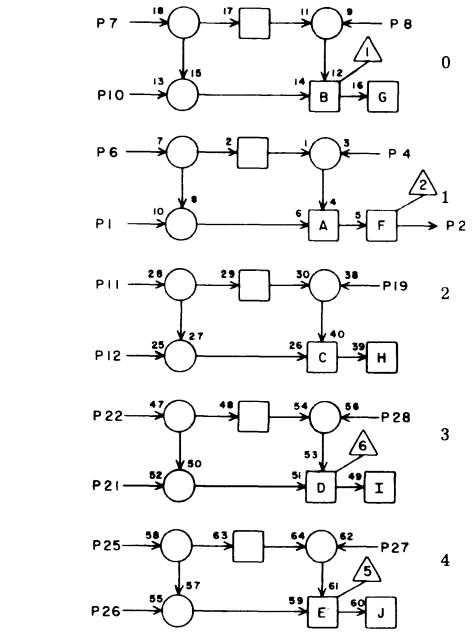
CIRCUIT SPECIFICATION 11827600

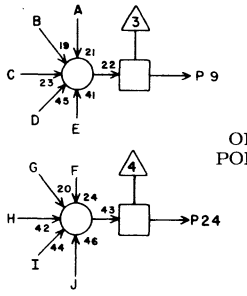
60196300
Rev A

LS 63051500 ASSY — REV B

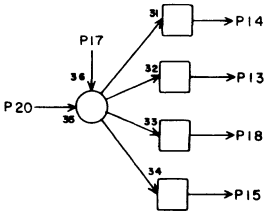
JR

D06





ON POINT



1	C05	6	5
2			
3			
4	C05	11	5
5			
6	C07	8	5
7	C07	9	5
8	C05	4	5
9	D06	17	3
10	C05	3	5
11	C07	10	5
12	C05	10	5
13	D07	3	3
14	D04	1	5
15	F07	21	9
16			
17	D06	9	3
18	F07	22	9
19	C05	13	7
20	E01	22	9
21	C05	17	7
22	C07	19	5
23			
24			
25	C07	21	7
26	C05	18	7
27	C05	16	7
28	C05	15	7

JACK PIN LG

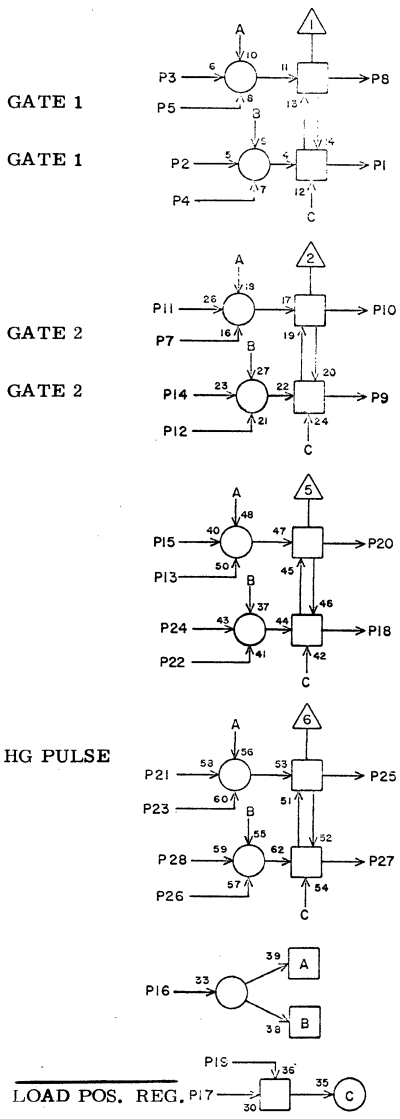
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63040400 ASSY C REV

AE

D07



1	D02	2	7
2	E01	18	121
3	D06	13	3
4	F07	14	9
5	E01	16	121
6			
7	D04	15	5
8	D04	3	7
9			
10	D02	10	7
11	D04	19	7
12	D02	1	7
13			
14	D04	17	5
15			
16	D07	X	2
17	G11	15	13
18			
19	D07	X	2
20			
21	C08	17	5
22			
23	D07	X	2
24			
25	D09	5	5
26	D07	X	2
27	J08	26	21
28	D09	10	5

VERIFY 1

VERIFY 2

HG & 30 MS

JACK P.N LG

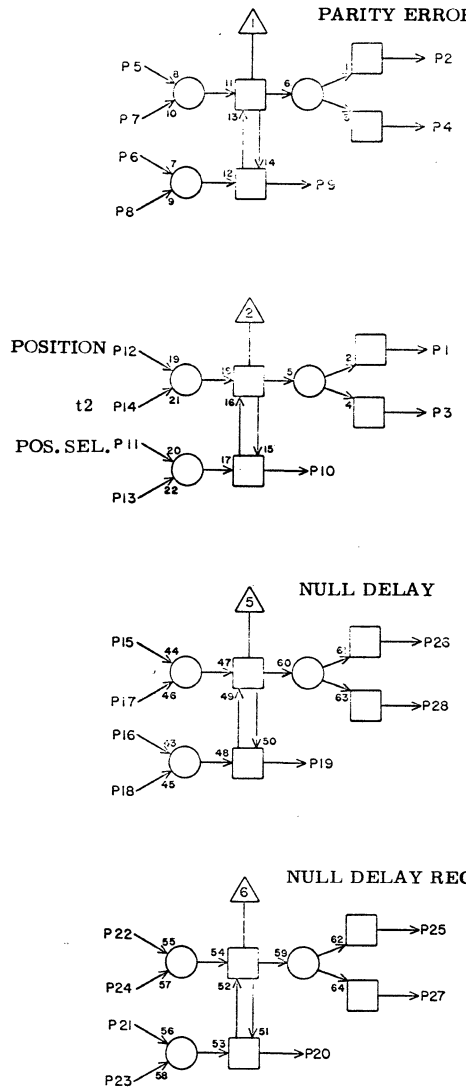
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63040000 ASSY D REV

AA

D08



1	G06	14	13
2	I13	4	19
3	D02	17	9
4	I16	4	21
5	G01	11	15
6	K09	18	25
7	D08	X	2
8	D08	X	2
9			
10			
11	G05	9	13
12	D03	19	7
13	D08	X	2
14	E04	24	9
15	D09	20	3
16	D08	X	2
17	D08	27	3
18	F04	22	11
19	D08	24	3
20	D09	13	5
21	D02	11	9
22	D09	14	5
23	D08	X	2
24	D08	19	3
25	D09	19	5
26	G13	25	15
27	D08	17	3
28	D02	7	9

JACK PIN LG

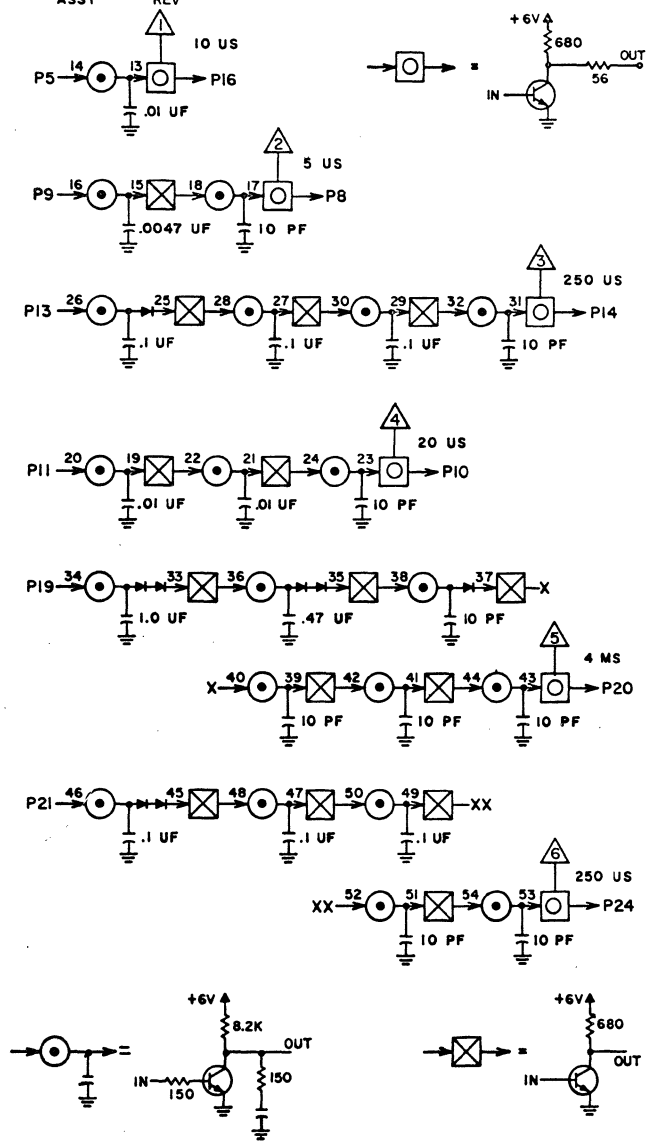
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63065529 ASSY

F REV

XL09



	D09		
1			
2			
3			
4			
5	D07	25	5
6			
7			
8	D12	26	5
9	F10	2	9
10	D07	28	5
11	D09	16	3
12			
13	D08	20	5
14	D08	22	5
15	D03	5	7
16	D09	11	3
17			
18			
19	D08	25	5
20	D08	15	3
21	F01	5	13
22			
23			
24	D02	5	9
25			
26			
27			
28			

JACK PIN LG

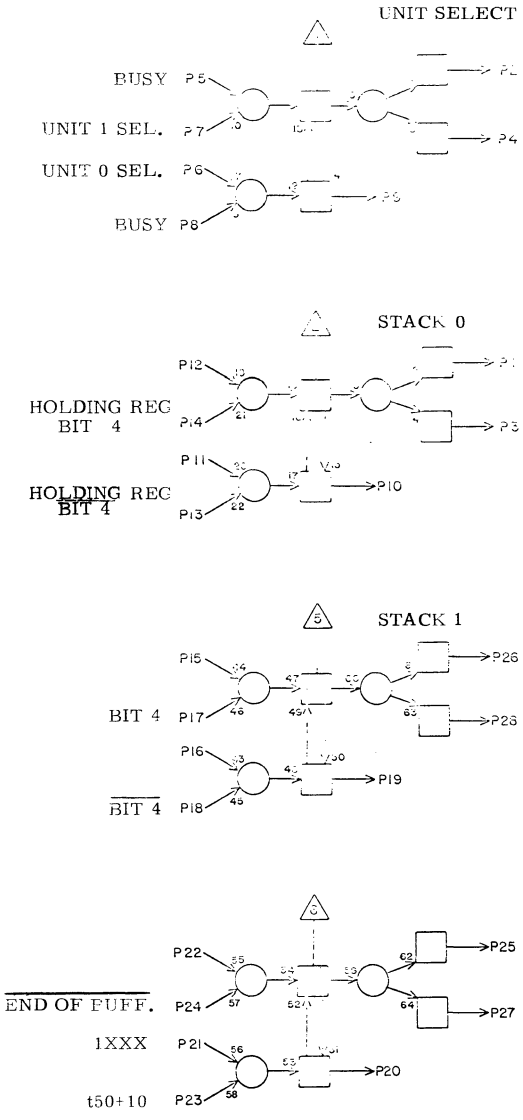
CIRCUIT SPECIFICATION 11827600

60196300

Rev A

LS 63065529 ASSY

D REV



	D10		
1			
2	C07	23	5
3	C10	26	3
4			
5			
6			
7	E03	21	11
8	I09	1	17
9	I10	1	17
10	E03	23	11
11	C10	1	7
12			
13	E13	22	7
14	E13	20	7
15	H11	9	15
16	F09	22	9
17	G04	20	15
18	G04	22	15
19	F09	21	9
20	H11	11	15
21			
22			
23	J02	20	25
24	G01	28	19
25	J02	13	25
26	H05	19	17
27	F08	22	9
28	C07	25	7

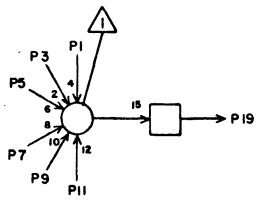
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

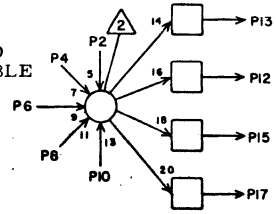
Rev A

LS 63063400 ASSY | 2 REV | TB | D12



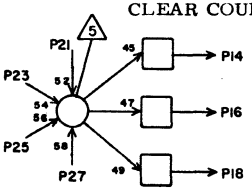
PARITY ERROR

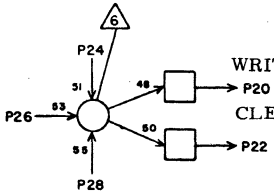
SELECT READ CLOCK



READ ENABLE

CLEAR COUNTER





WRITE GUARD BITS

CLEAR WRITE ENABLE

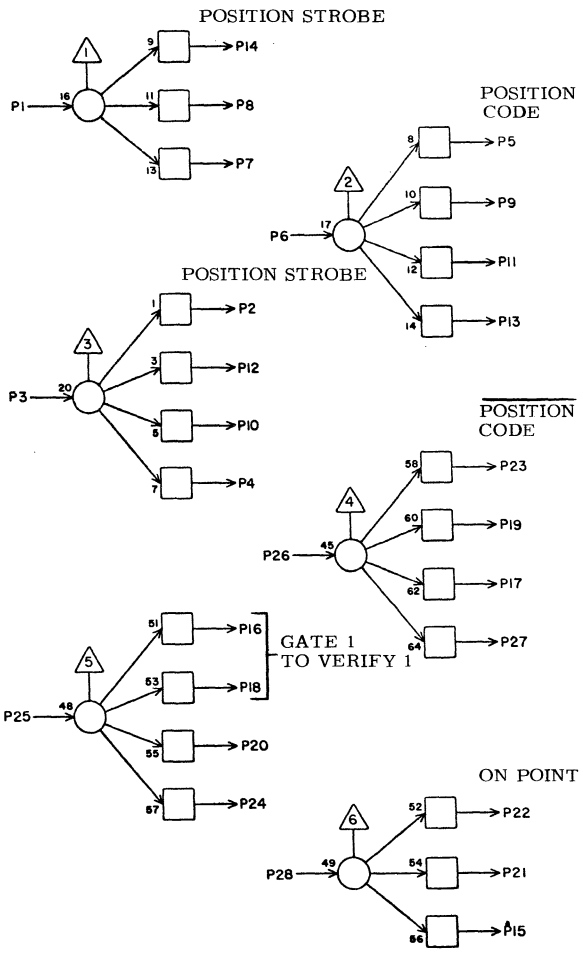
	JACK	PIN	LG
1	E12	17	7
2	E09	10	7
3	F07	11	11
4	E08	27	9
5	G13	19	13
6	D12	X	2
7	D12	X	2
8	D12	X	2
9	D12	X	2
10	D12	X	2
11	D12	X	2
12	G01	2	17
13	E09	8	7
14	C16	13	7
15			
16	C15	13	7
17			
18			
19	G01	7	17
20	F10	6	9
21	E09	14	7
22	G01	17	17
23	E09	19	7
24	D12	X	2
25	D12	X	2
26	D09	8	5
27	D12	X	2
28	F10	4	121

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064000 ASSY | REV

TH



	E01		
1	K01	25	23
2	E03	16	5
3	E01	8	121
4			
5	E02	14	3
6	K01	6	21
7	E03	13	5
8	E01	3	121
9	D04	25	7
10			
11	D04	24	7
12	E03	18	5
13			
14	E03	11	5
15	D03	5	7
16	D07	5	121
17			
18	D07	2	121
19	D04	4	7
20			
21	D03	4	7
22	D06	20	9
23	E02	11	3
24			
25	D04	12	121
26	K01	13	19
27			
28	K01	23	21
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600

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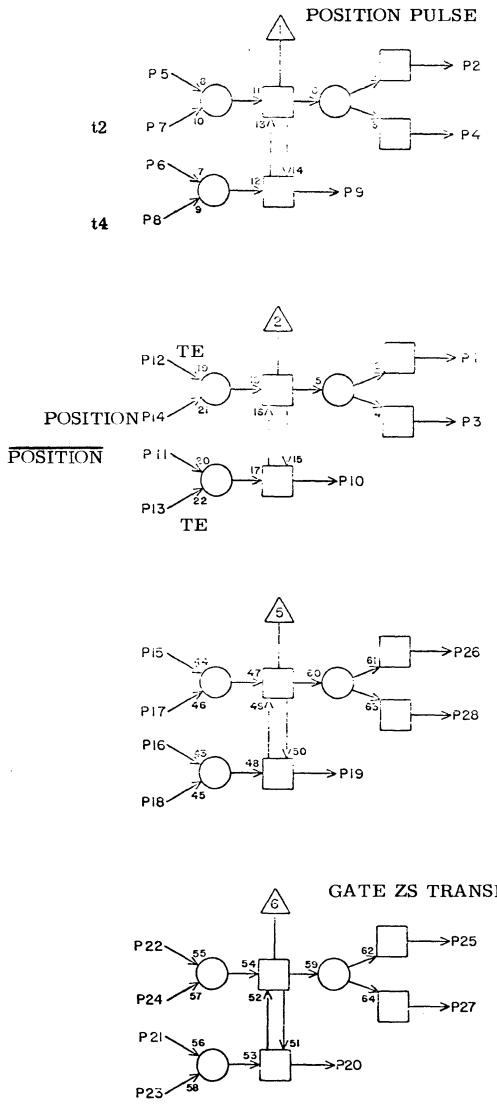
Rev A

LS 63064000 ASSY | D REV



	E02		
1	D04	27	5
2	L05	9	25
3			
4	J07	23	21
5	G05	11	9
6	E02	X	2
7	E07	9	7
8	E05	18	5
9			
10	D04	2	7
11	E01	23	3
12	E03	1	5
13	E03	3	5
14	E01	5	3
15	E02	X	2
16	D04	13	121
17	D04	18	121
18	E02	X	2
19	D04	21	7
20			
21	E02	X	2
22	J07	9	17
23	F07	17	9
24	E02	X	2
25	L01	18	25
26	D04	26	7
27			
28	D04	8	7
	JACK	PIN	LG

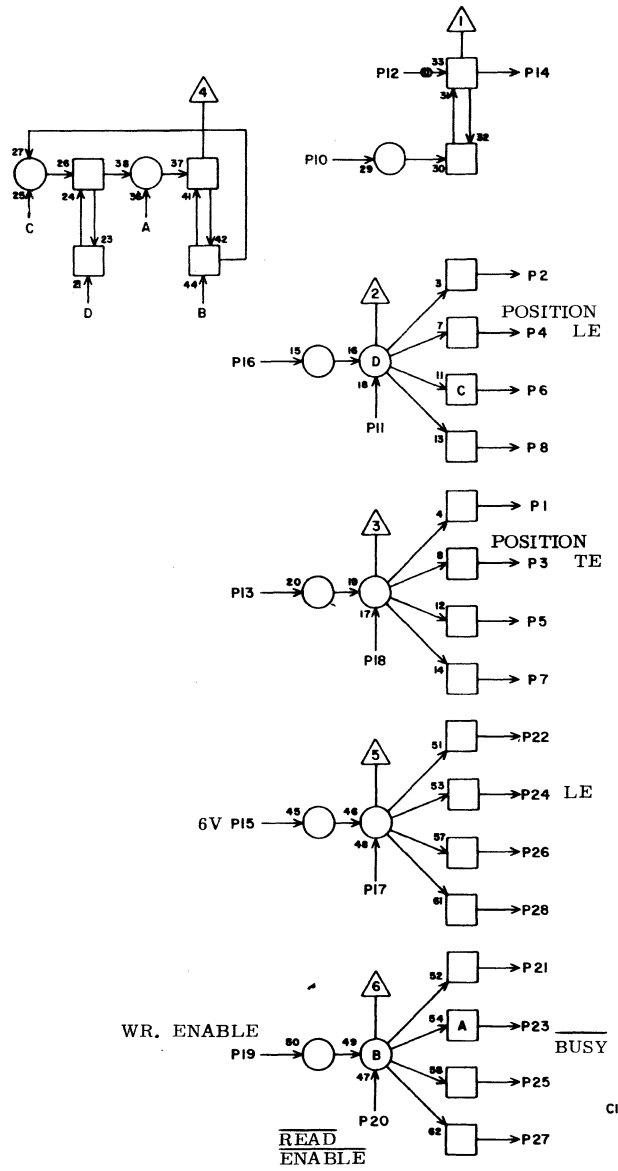
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63046200 ASSY D REV

HQ

E03



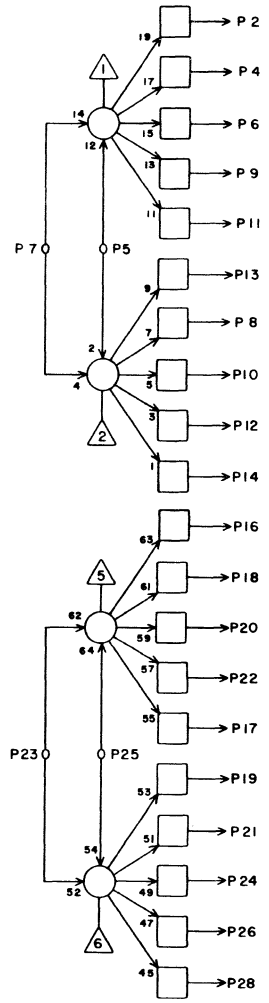
	JACK	PIN	LG
1	E02	12	5
2			
3	E02	13	5
4	D04	6	5
5	D04	28	5
6	D04	23	5
7			
8	E03	17	5
9			
10			
11	E01	14	5
12			
13	E01	7	5
14			
15	C02	2	9
16	E01	2	5
17	E03	8	5
18	E01	12	5
19	F04	7	5
20	E08	20	9
21	D10	5	11
22	C01	22	9
23	D10	8	11
24	C01	11	9
25	D03	1	7
26	C02	22	9
27	F01	26	7
28	C02	11	9

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63044800 ASSY B REV

HC

E04



	JACK	PIN	LG
1			
2	E07	23	7
3			
4	H06	7	13
5	F01	18	7
6	H06	22	13
7	F07	12	7
8	F06	14	7
9	H07	7	13
10	F05	16	7
11	H07	22	13
12	E12	4	11
13			
14	F10	17	9
15			
16			
17	G15	11	15
18	G14	22	15
19	G16	22	17
20	G14	11	15
21	G16	11	15
22	G15	22	15
23	F02	10	5
24	D08	14	9
25	F03	5	5
26	F06	17	7
27			
28	F05	7	5

CIRCUIT SPECIFICATION 11827600
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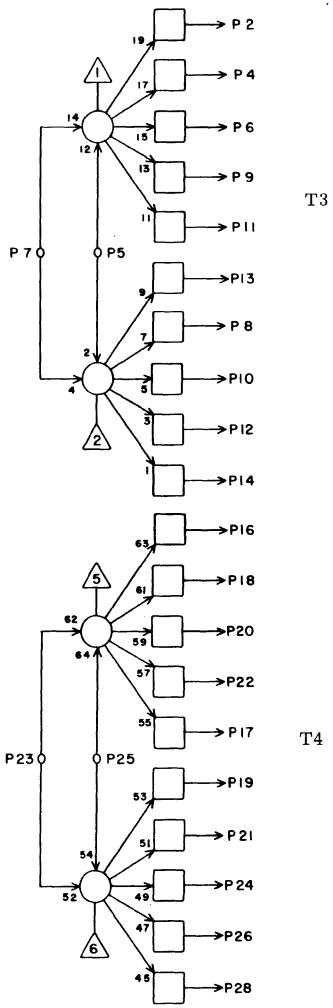
LS 63044800 ASSY B REV

HC E05



1			
2			
3			
4	E15	7	13
5	F03	23	7
6	E15	22	13
7	F02	20	7
8	E16	7	13
9			
10	F06	13	7
11	E16	22	13
12	F06	23	7
13	G06	16	9
14			
15			
16	G05	16	9
17	F06	24	7
18	E02	8	5
19	F05	14	7
20	F06	8	7
21			
22	F06	18	7
23	F02	24	7
24	E12	28	9
25	F03	21	7
26	F05	8	7
27			
28	G08	10	9

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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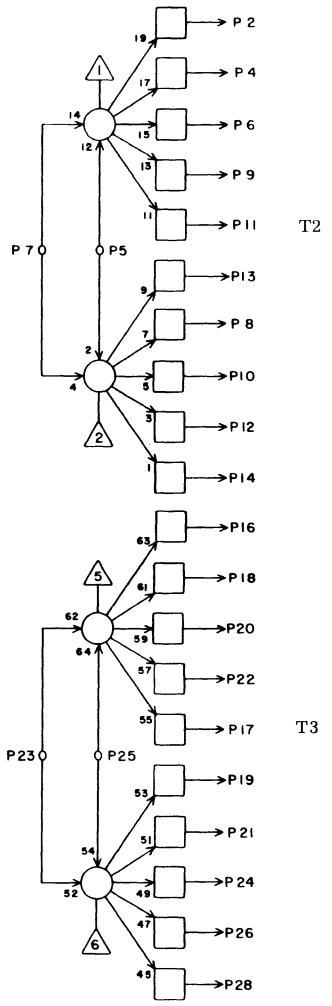
LS 63044800 ASSY B REV

HC E06



1			
2			
3			
4	E07	7	3
5	F03	3	7
6	E12	5	9
7	F02	8	9
8	C16	22	13
9	F10	24	9
10	C16	11	15
11	C15	22	13
12			
13	C15	11	13
14			
15			
16	C11	16	11
17	F05	17	7
18	C12	16	11
19			
20			
21			
22	F05	13	7
23	F02	25	9
24			
25	F03	28	9
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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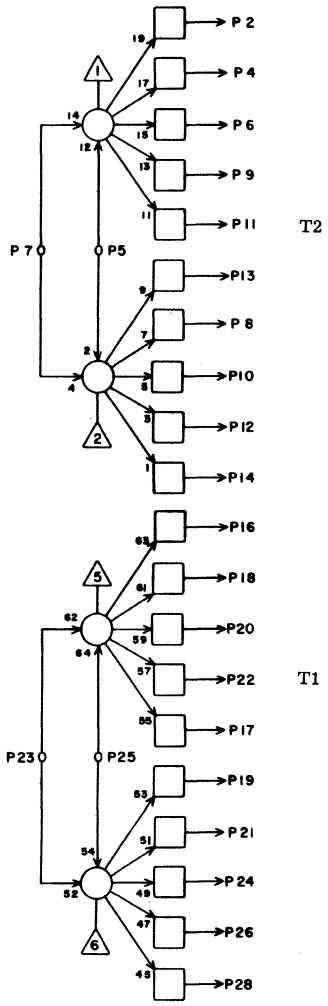
Rev A

LS 63044800 ASSY **B** REV



HC

	E07		
1			
2			
3			
4	E08	14	5
5	E07	X	2
6			
7	E06	4	3
8	F06	5	5
9	E02	7	7
10			
11	E08	6	3
12			
13			
14	G12	12	11
15			
16	J03	15	19
17			
18	J04	15	19
19			
20	J05	15	19
21			
22			
23	E04	2	7
24			
25	E07	X	2
26			
27			
28			

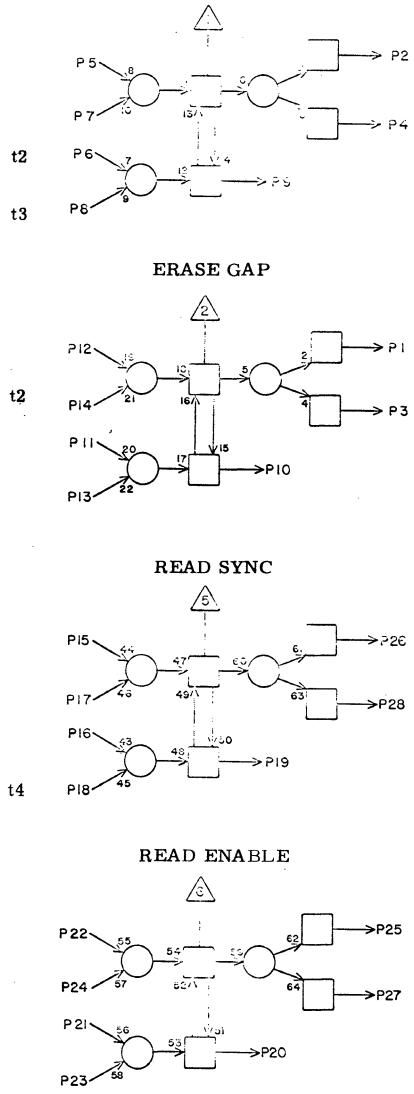
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63040000 ASSY **D** REV

SECTOR SYNC I



AA

	E08		
1	C10	4	9
2	F06	12	7
3	E08	15	3
4			
5	C09	13	9
6	E07	11	3
7	E08	X	2
8	E09	13	5
9	F06	11	7
10			
11	E08	26	3
12	E12	14	7
13	E08	X	2
14	E07	4	5
15	E08	3	3
16	F08	28	7
17	E12	20	7
18	E08	X	2
19	E09	4	3
20	E03	20	9
21	F08	11	5
22	C10	7	9
23	E08	X	2
24	E08	X	2
25	L05	16	23
26	E08	11	3
27	D12	4	9
28	F01	1	9

JACK PIN LG

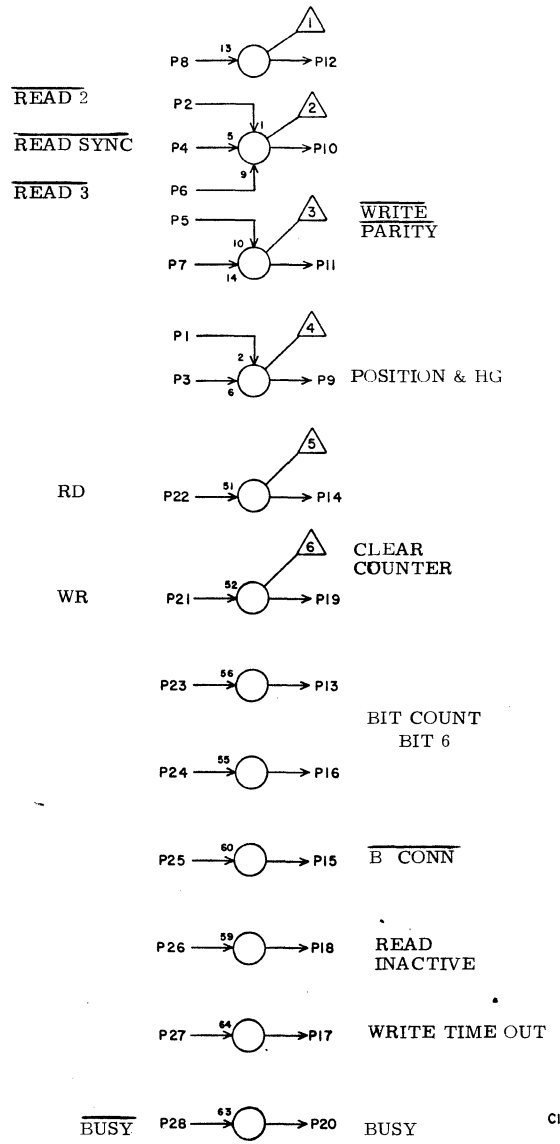
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064400 ASSY [2] REV

TL

E09



	JACK	PIN	LG
1	H14	2	13
2	F10	10	7
3	H14	17	13
4	E08	19	3
5	F09	14	7
6	E10	18	3
7	F05	1	7
8	D12	13	7
9	K09	5	21
10	D12	2	7
11	E10	1	3
12	G01	8	13
13	E08	8	5
14	D12	21	7
15	E10	6	5
16	G08	4	9
17	F10	5	5
18	J07	7	17
19	D12	23	7
20	D02	12	11
21	G04	18	11
22	E12	18	5
23	F06	10	7
24	C12	23	11
25	K05	23	23
26	C10	11	9
27	E10	14	5
28	F01	27	11

CIRCUIT SPECIFICATION 11827600

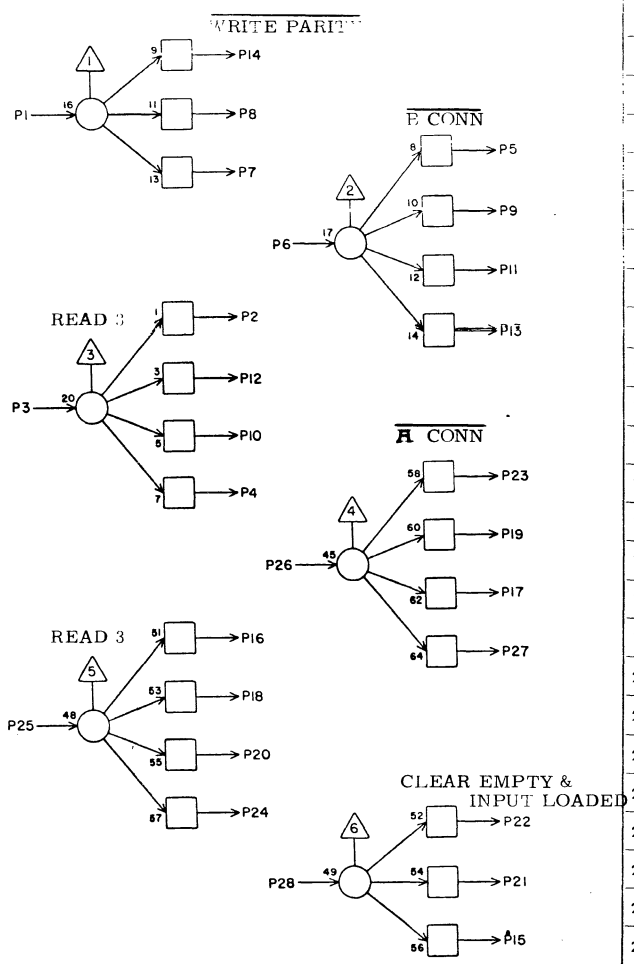
60196300

Rev A

LS 63064000 ASSY [ ] REV

TH

E10



	JACK	PIN	LG
1	E09	11	3
2	F13	15	7
3	F10	19	7
4			
5	I16	26	17
6	E09	15	5
7	G10	16	9
8	G09	16	9
9	K06	3	120
10	G08	21	9
11	I05	20	17
12	E10	25	3
13			
14	E09	27	5
15			
16	F14	15	7
17			
18	E09	6	3
19	I13	26	15
20			
21	G12	26	9
22	F10	21	5
23	I05	27	17
24			
25	E10	12	3
26	J10	4	17
27			
28	F08	1	5

CIRCUIT SPECIFICATION 11827600

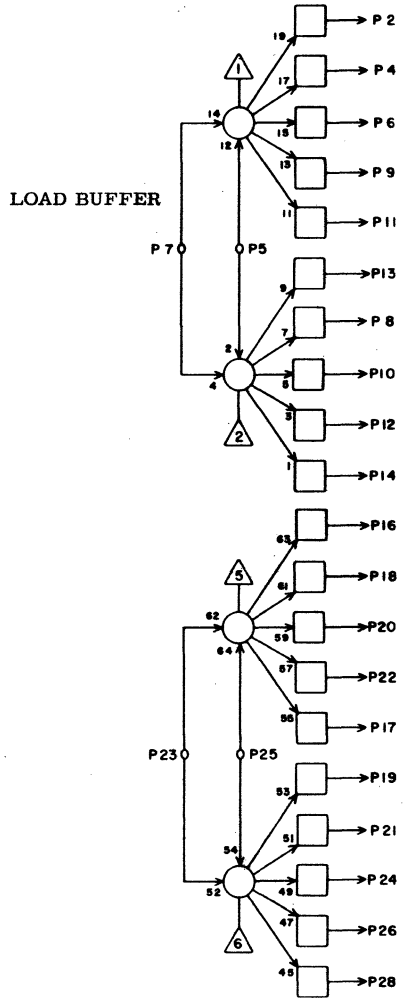
60196300

Rev A

LS 63044800 ASSY B REV

HC

E11



1			
2	H08	7	13
3			
4	H08	22	13
5	F12	11	7
6	H09	7	11
7	J02	11	25
8	G04	3	11
9	H09	22	13
10	E13	26	5
11	G04	26	13
12	G12	2	9
13			
14	H05	6	13
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			

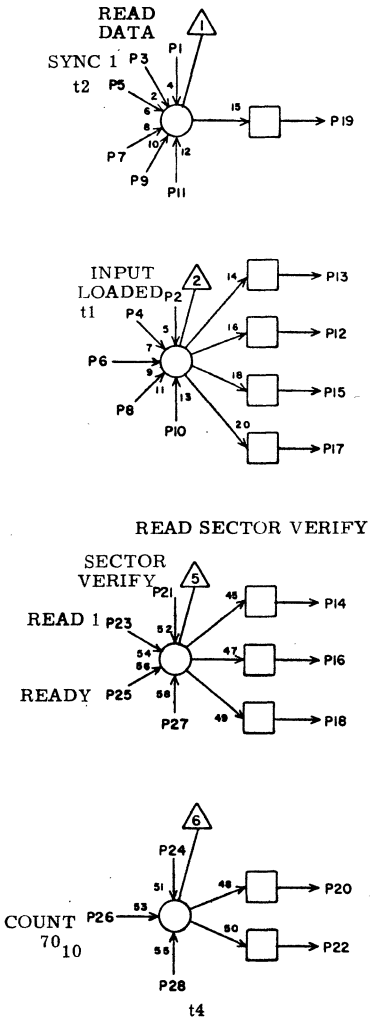
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63063400 ASSY 2 REV

IN SYNC



T8

E12

1	E13	14	3
2	F10	25	7
3	G06	22	13
4	E04	12	11
5	E06	6	9
6	E12	X	2
7	E12	X	2
8	E12	X	2
9	E12	X	2
10	E12	X	2
11	E12	X	2
12	F08	9	9
13	F10	11	7
14	E08	12	7
15	I05	17	17
16	C10	2	11
17	D12	1	7
18	E09	22	5
19	H13	21	13
20	E08	17	7
21	F06	1	9
22			
23	G07	8	11
24	E12	X	2
25	D03	12	13
26	C09	20	9
27	E12	X	2
28	E05	24	9

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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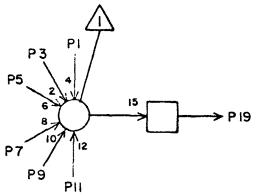
Rev A

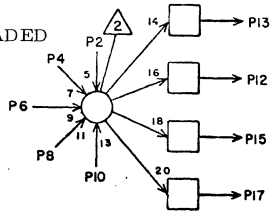
LS 63063400 ASSY [ ] REV

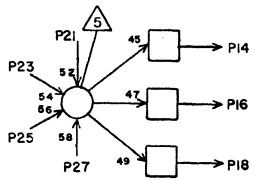
TB



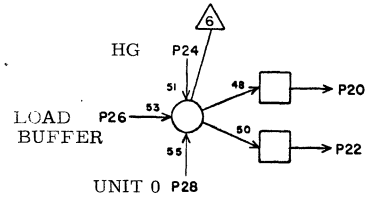
EMPTY

INPUT LOADED





TO IN SYNC GATE



E13

1	F01	23	15
2	G12	25	11
3	F11	12	7
4	F10	27	9
5	E13	X	2
6	F11	23	7
7	E13	X	2
8	E13	X	2
9	E13	X	2
10	E13	X	2
11	E13	X	2
12			
13	F12	18	7
14	E12	1	3
15			
16	G06	17	11
17			
18			
19	G06	13	11
20	D10	12	7
21	F01	14	15
22	D10	11	7
23	E14	28	3
24	B07	8	17
25	E14	15	3
26	E11	10	5
27	E13	X	2
28	C10	12	11

JACK PIN LG

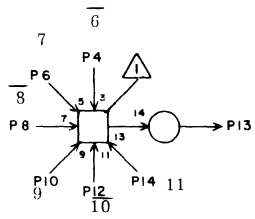
CIRCUIT SPECIFICATION 11827600

60196300

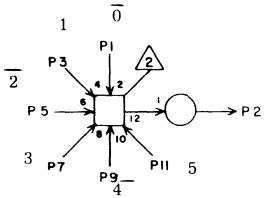
Rev A

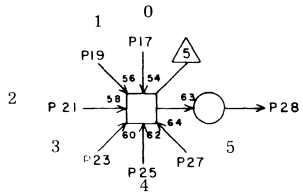
LS 63048700 ASSY [C] REV

IP

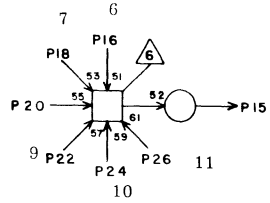


PARITY





TO IN SYNC GATE



E14

1	E15	4	3
2	F07	5	9
3	E15	2	3
4	E16	4	5
5	E15	13	3
6	E16	2	5
7	E15	19	3
8	E16	13	5
9	E15	16	3
10	E16	19	5
11	E15	28	3
12	E16	16	5
13	F07	7	9
14	E16	28	5
15	E13	25	3
16	J04	27	21
17	J03	6	21
18	J04	20	21
19	J03	7	21
20	J05	6	19
21	J03	27	21
22	J05	7	19
23	J03	20	21
24	J05	27	21
25	J04	6	19
26	J05	20	21
27	J04	7	19
28	E13	23	3

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

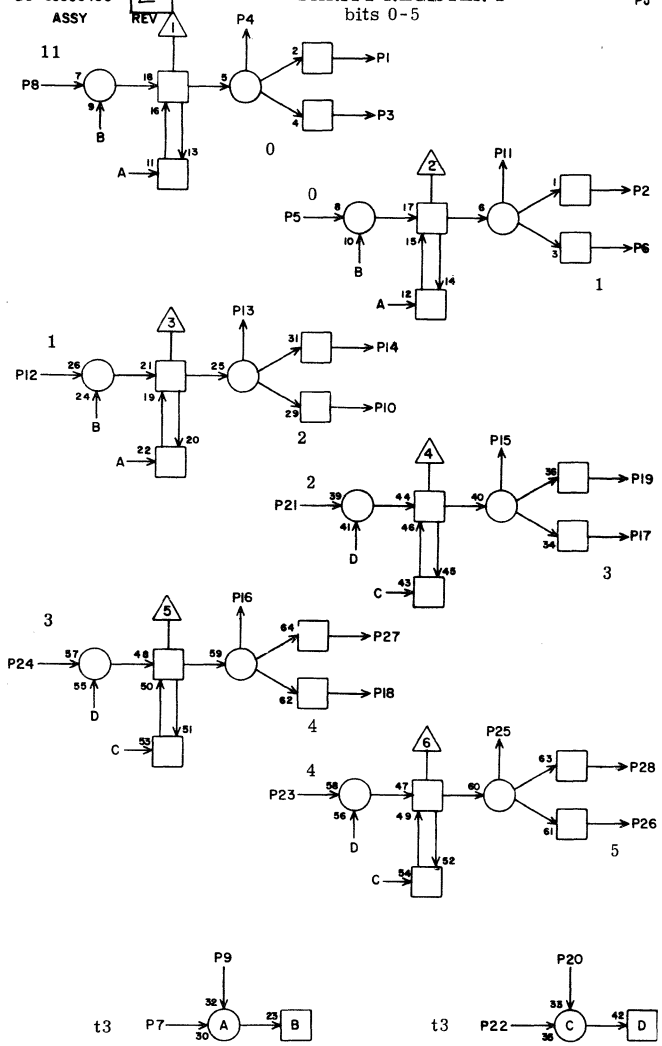
60196300

Rev A

LS 63058400 ASSY REV E 1

PARITY REGISTER 2
bits 0-5

PJ



E15

1	G09	2	11
2	E14	3	3
3	F15	8	7
4	E14	1	3
5	G14	14	9
6	F15	3	5
7	E05	4	13
8	G16	21	9
9	E15	X	2
10	F15	11	5
11	G09	1	11
12	G14	9	9
13	E14	5	3
14	G09	12	11
15	G09	17	11
16	E14	9	3
17	F15	20	5
18	F15	26	7
19	E14	7	3
20	E15	X	2
21	G14	18	9
22	E05	6	13
23	G15	14	7
24	G14	21	9
25	G09	27	11
26	F15	23	5
27	G09	28	11
28	E14	11	3

JACK PIN LG

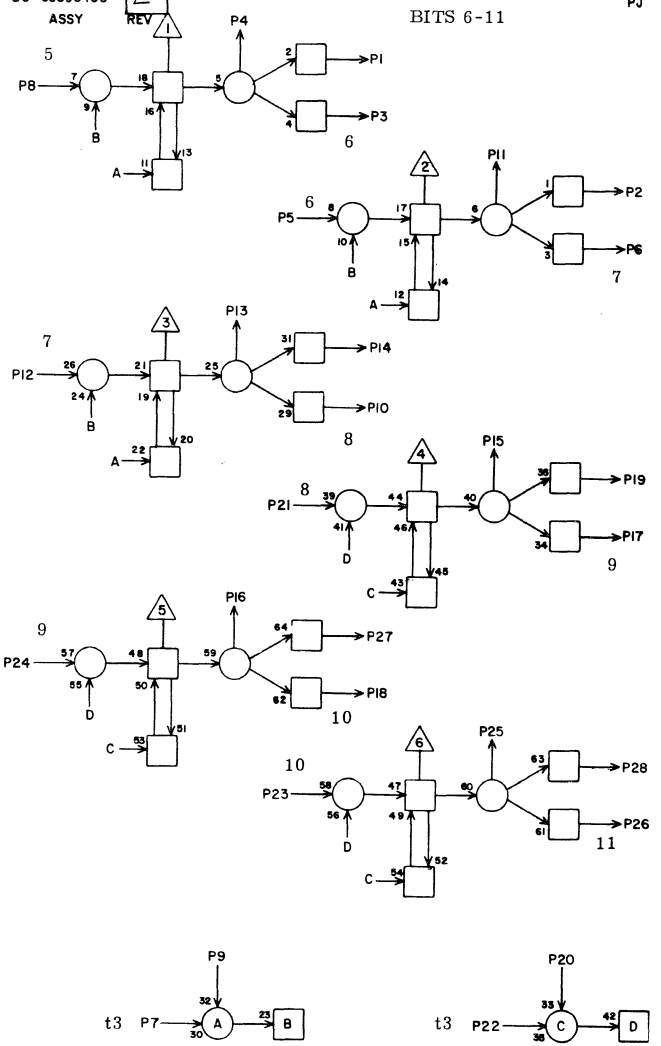
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63058400 ASSY REV E 1

PARITY REGISTER 2
BITS 6-11

PJ



E16

1	G10	2	11
2	E14	6	5
3	F16	8	5
4	E14	4	5
5	G15	18	9
6	F16	3	5
7	E05	8	13
8	G15	9	9
9	E16	X	2
10	F16	11	5
11	G10	1	11
12	G15	21	9
13	E14	8	5
14	G10	12	11
15	G10	17	11
16	E14	12	5
17	F16	20	5
18	F16	26	7
19	E14	10	5
20	E16	X	2
21	G16	14	7
22	E05	11	13
23	G16	18	7
24	G16	9	7
25	G10	27	11
26	F16	23	5
27	G10	28	11
28	E14	14	5

JACK PIN LG

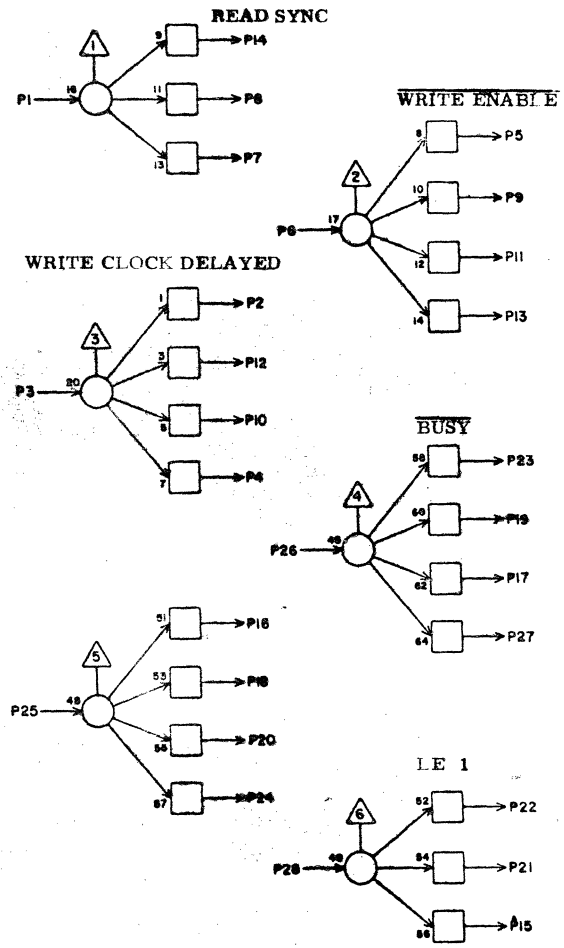
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064000 ASSY — REV

TH

F01



1	E08	28	9
2	A09	1	21
3	F01	16	121
4	F07	27	9
5	D09	21	13
6	F05	20	7
7			
8	G08	2	11
9	A09	3	21
10	I09	7	120
11			
12			
13	J07	6	17
14	E13	21	15
15			
16	F01	3	121
17	C08	28	17
18	E04	5	7
19	G08	5	9
20	F02	14	3
21	A02	22	17
22	A02	11	19
23	E13	1	15
24			
25	G01	1	5
26	E03	27	7
27	E09	28	11
28	B08	28	17

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

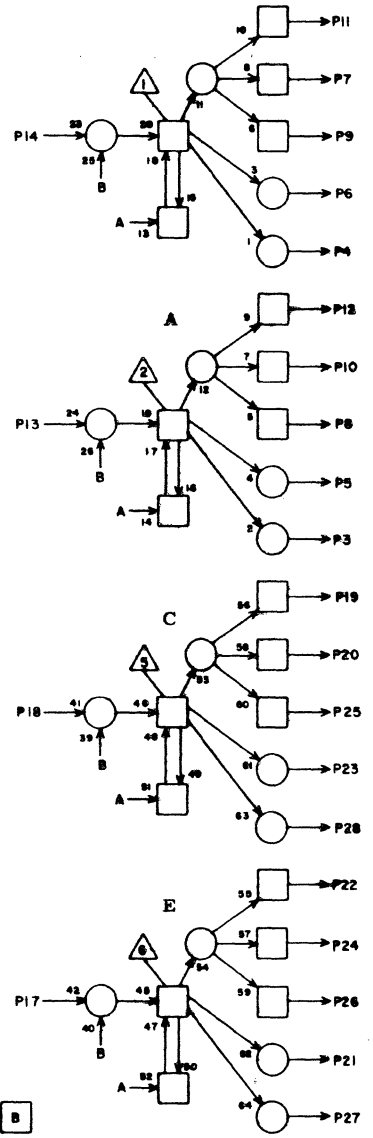
60196300
Rev A

LS 63057900 ASSY — B REV

FILE CLOCK
STROBE NETWORK

PD

F02



1			
2			
3			
4			
5			
6			
7			
8	E06	7	9
9			
10	E04	23	5
11	F03	14	3
12	F03	13	3
13	F03	11	3
14	F01	20	3
15			
16	J09	26	17
17	F03	19	3
18	F03	12	3
19	F03	18	3
20	E05	7	7
21			
22	F03	17	3
23			
24	E05	23	7
25	E06	23	9
26			
27			
28			

JACK PIN LG

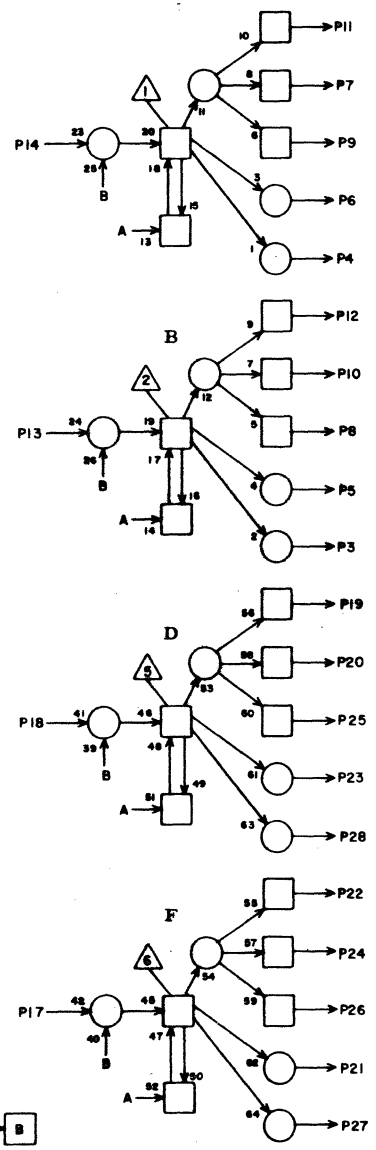
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

t50 P16 → 43 A 44 → B

LS 63057900 ASSY B REV

FILE CLOCK STROBE NETWORK



PD

F03

1			
2			
3	E06	5	7
4			
5	E04	25	5
6			
7			
8			
9			
10			
11	F02	13	3
12	F02	18	3
13	F02	12	3
14	F02	11	3
15			
16	J09	6	15
17	F02	22	3
18	F02	19	3
19	F02	17	3
20			
21	E05	25	7
22			
23	E05	5	7
24			
25			
26			
27			
28	E06	25	9

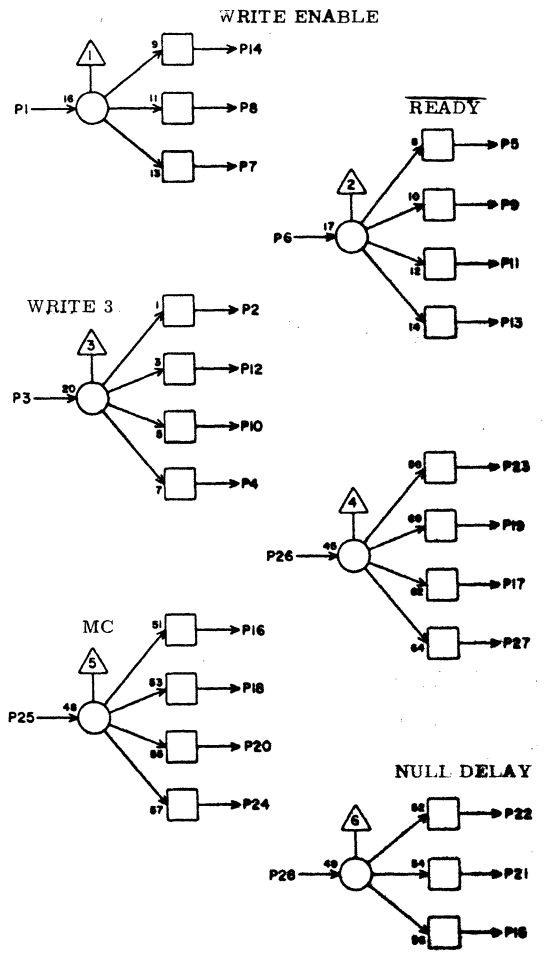
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064000 ASSY REV

TH



F04

1	F05	25	5
2	F13	14	13
3	F05	10	3
4			
5	G01	15	9
6	F07	13	7
7	E03	19	5
8	G08	24	9
9	I13	3	17
10	G08	23	9
11	I16	3	17
12	F14	14	13
13	G01	21	9
14			
15			
16	D03	2	9
17	G03	28	7
18	G12	19	11
19	F06	21	5
20	F08	26	7
21	D02	9	9
22	D08	18	11
23	G03	25	5
24	I05	5	11
25	G11	3	9
26	F06	19	5
27			
28	D02	16	9

JACK PIN LG

CIRCUIT SPECIFICATION 11827400

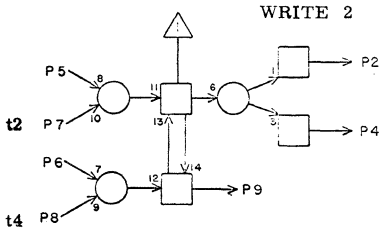
60196300
Rev A

LS 63040000 ASSY | D REV

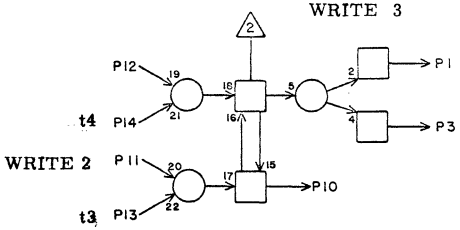
AA

F05

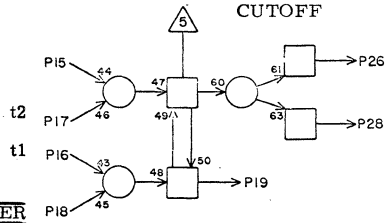
WRITE 2



WRITE 3

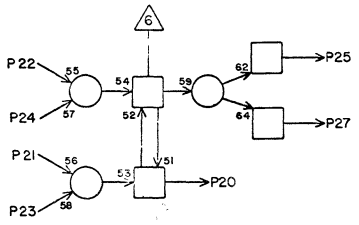


CUTOFF



BUFFER LOADED

WRITE ENABLE



	JACK	PIN	LG
1	E09	7	7
2	F05	12	3
3			
4			
5	G03	20	7
6	F09	12	7
7	E04	28	5
8	E05	26	7
9	F09	1	7
10	F04	3	3
11	F09	8	5
12	F05	2	3
13	E06	22	7
14	E05	19	7
15	G03	22	7
16	E04	10	7
17	E06	17	7
18	G13	21	11
19	F09	3	7
20	F01	6	7
21	G01	16	7
22	G03	12	5
23	F05	X	2
24	F05	X	2
25	F04	1	5
26	I05	13	121
27	L05	27	21
28			

CIRCUIT SPECIFICATION 11827600

60196300

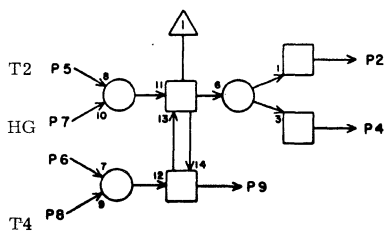
Rev A

LS 63040000 ASSY | D REV

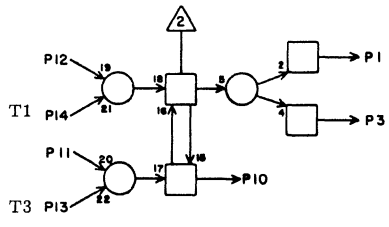
AA

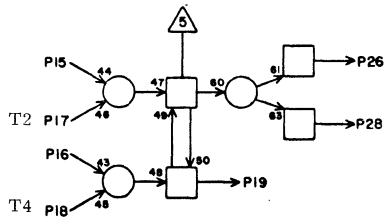
F06

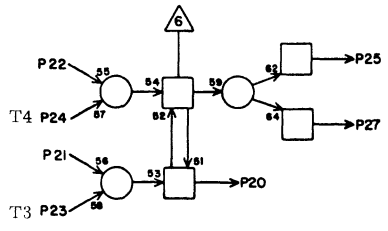
HEAD GROUP PULSE



SECTOR SYNCHRONIZATION 2







	JACK	PIN	LG
1	E12	21	9
2	L05	12	21
3	G04	21	7
4	J07	24	17
5	E07	8	5
6	F06	X	2
7	G05	12	7
8	E05	20	7
9	C08	27	11
10	E09	23	7
11	E08	9	7
12	E08	2	7
13	E05	10	7
14	E04	8	7
15	G04	14	7
16	C09	14	13
17	E04	26	7
18	E05	22	7
19	F04	26	5
20	G03	26	7
21	F04	19	5
22	F06	28	3
23	E05	12	7
24	E05	17	7
25	G03	27	7
26	G03	3	7
27			
28	F06	22	3

CIRCUIT SPECIFICATION 11827600

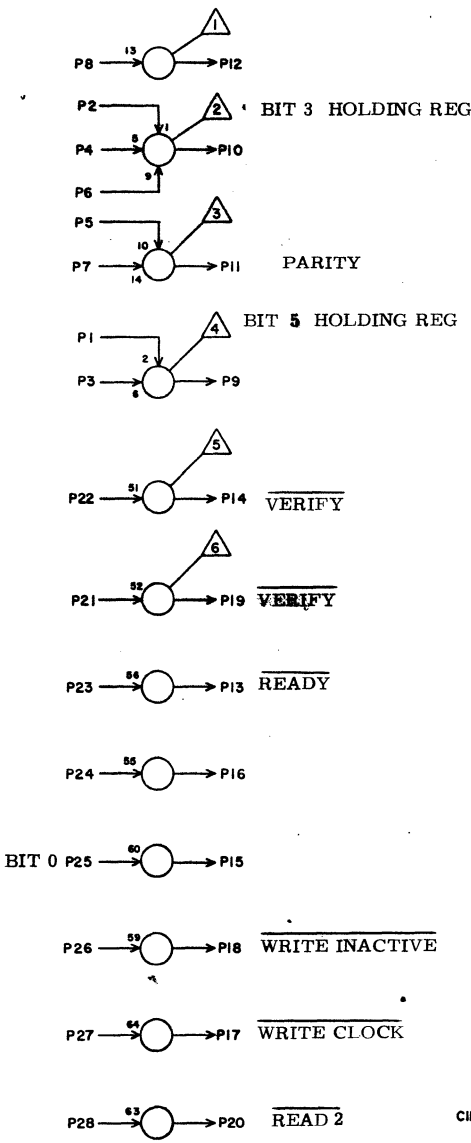
60196300

Rev A

LS 63064400 ASSY C REV

TL

F07



1	F07	X	2
2	H10	20	11
3	H11	12	13
4	F07	X	2
5	E14	2	9
6	F07	X	2
7	E14	13	9
8	I09	11	13
9	K10	23	23
10	I10	12	13
11	D12	3	11
12	E04	7	7
13	F04	6	7
14	D07	4	9
15	G02	5	9
16	G02	3	9
17	E02	23	9
18	J07	5	15
19	D02	4	11
20	F10	16	5
21	D06	15	9
22	D06	18	9
23	D03	17	11
24	G03	24	9
25	C11	9	15
26	G03	14	7
27	F01	4	9
28	G13	11	9

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

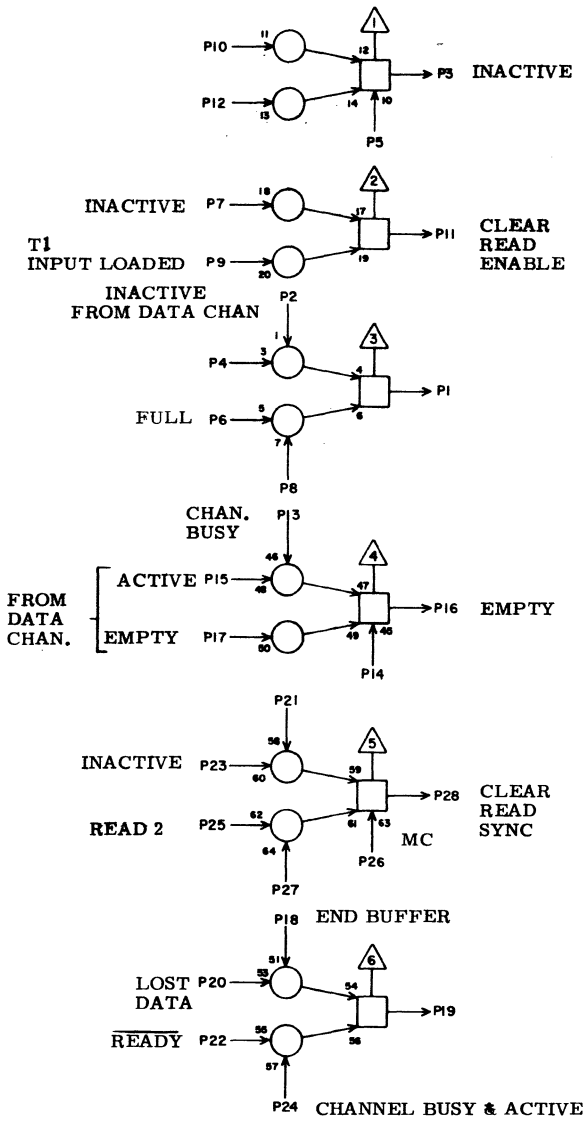
60196300

Rev A

LS 63060700 ASSY C REV

QN

F08



1	E10	28	5
2	G11	7	7
3	F11	17	5
4	F08	X	2
5	F12	21	7
6	F11	20	7
7	G11	13	11
8	F08	X	2
9	E12	12	9
10	J07	13	15
11	E08	21	5
12	K10	16	21
13	C10	18	13
14	F08	X	2
15	G13	8	9
16	G12	21	9
17	J02	23	19
18	H05	28	9
19	F12	17	7
20	H04	20	9
21	F08	X	2
22	D10	25	9
23	G11	11	11
24	G12	20	9
25	G13	13	9
26	F04	20	7
27	F08	X	2
28	E08	16	7

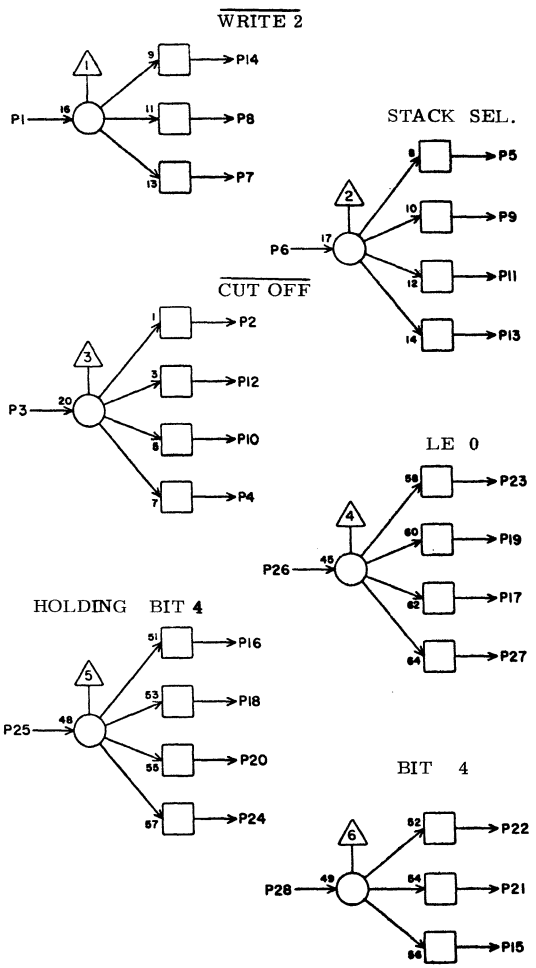
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

Rev A

LS 63064000 ASSY | REV | TH | F09



1	F05	9	7
2	H13	5	11
3	F05	19	7
4			
5	I12	25	13
6	C07	20	11
7			
8	F05	11	5
9	I15	25	15
10	I05	15	13
11	G06	18	7
12	F05	6	7
13	A09	18	17
14	E09	5	7
15	C08	25	11
16	C06	24	11
17			
18	A08	11	19
19	B02	11	11
20	F09	28	3
21	D10	17	9
22	D10	14	8
23	B02	22	17
24	D05	24	11
25	H11	8	7
26	B08	8	17
27			
28	F09	20	3

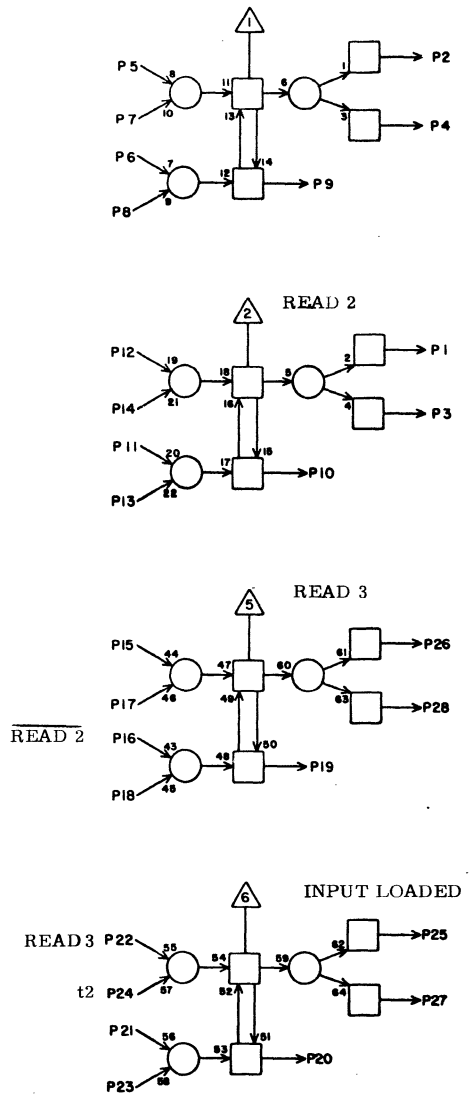
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

Rev A

LS 63040000 ASSY | REV | WRITE GUARD BITS TIME OUT | AA | E10



1			
2	D09	9	9
3	G13	6	7
4	D12	28	121
5	E09	17	5
6	D12	20	9
7	F10	X	2
8	F10	X	2
9			
10	E09	2	7
11	E12	13	7
12	H13	28	11
13	F10	X	2
14	F10	X	2
15	G13	5	7
16	F07	20	5
17	E04	14	9
18	F10	X	2
19	E10	3	7
20			
21	E10	22	5
22	G13	23	7
23	F10	X	2
24	E06	9	9
25	E12	2	7
26	G13	26	7
27	E13	4	9
28			

JACK PIN LG

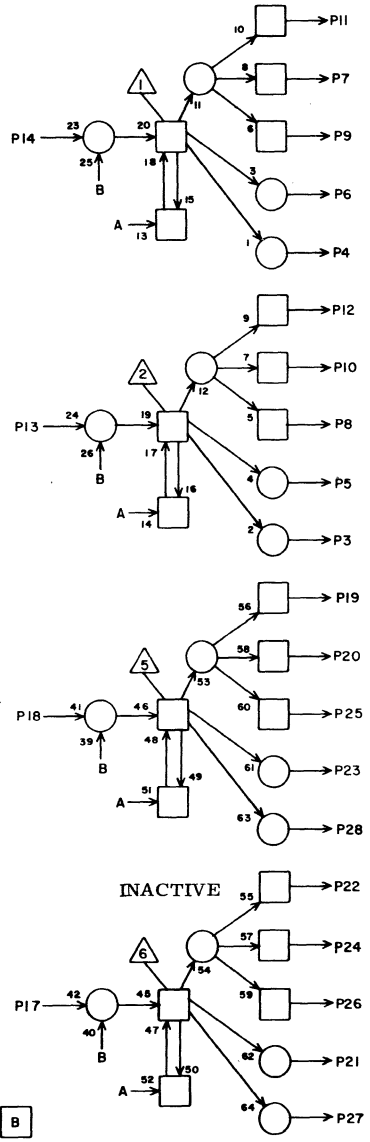
CIRCUIT SPECIFICATION 11827600

60196300

Rev A

LS 63057900 ASSY B REV

PD F11



t50 P16 43 A 44 B

1			
2			
3			
4			
5			
6	G08	7	9
7	G08	26	9
8			
9	G12	7	5
10			
11			
12	E13	3	7
13	F12	12	3
14	F12	7	5
15			
16	J09	28	17
17	F08	3	5
18	F12	20	3
19	H15	14	9
20	F08	6	7
21	G12	17	7
22	I09	23	13
23	E13	6	7
24	I10	23	13
25			
26			
27	G07	17	9
28			

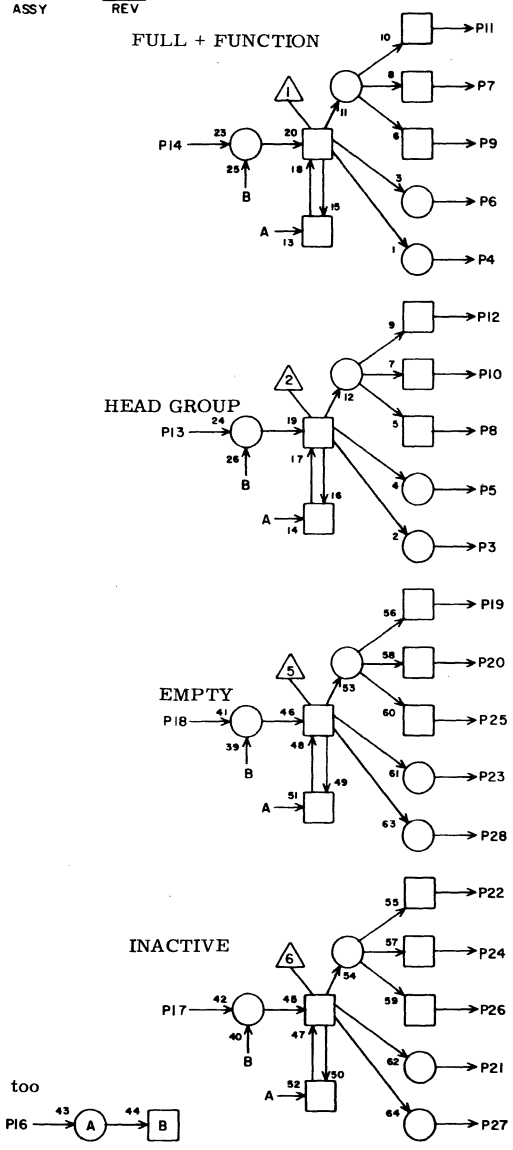
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63057900 ASSY B REV

PD F12



too P16 43 A 44 B

1			
2			
3			
4			
5			
6			
7	F11	14	5
8			
9			
10	D02	15	13
11	E11	5	7
12	F11	13	3
13	B07	14	17
14	H13	16	9
15			
16	J09	4	15
17	F08	19	7
18	E13	13	7
19			
20	F11	18	3
21	F08	5	7
22			
23			
24	I05	12	13
25			
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

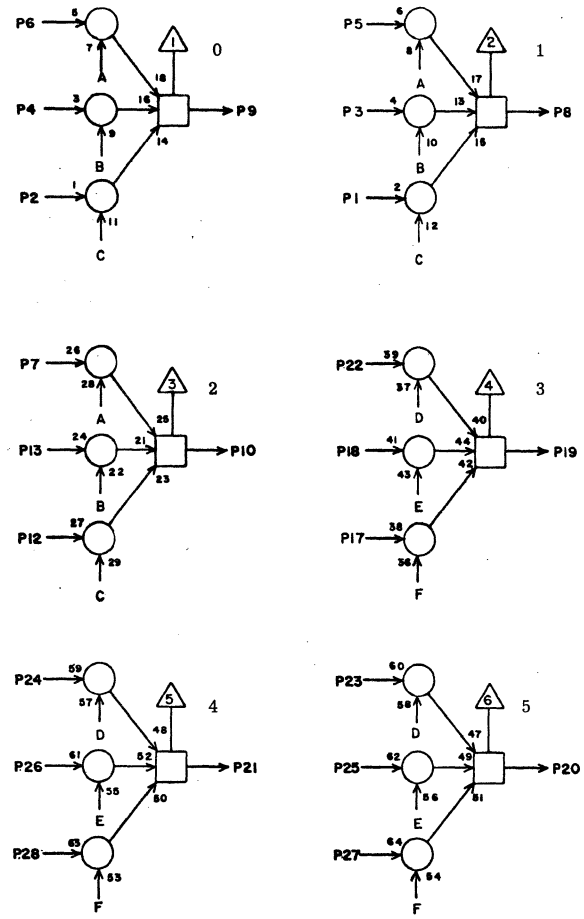
60196300
Rev A

LS 63063700 ASSY | REV

PARITY BITS 0-5

TE

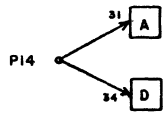
F13



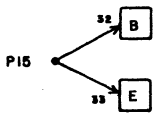
1			
2			
3	J03	8	19
4	J03	5	19
5	H06	6	13
6	H06	3	11
7	H06	10	13
8	F15	1	5
9	F15	5	5
10	F15	13	5
11			
12			
13	J03	26	19
14	F04	2	13
15	E10	2	7
16	F13	X	2
17			
18	J03	21	19
19	F15	18	5
20	F15	24	5
21	F15	28	5
22	H06	17	11
23	H06	26	13
24	H06	18	11
25	J04	8	17
26	J04	5	17
27			
28			

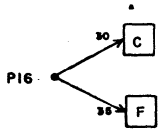
JACK PIN LG

WRITE 3



READ 3





CIRCUIT SPECIFICATION 11827600

60196300

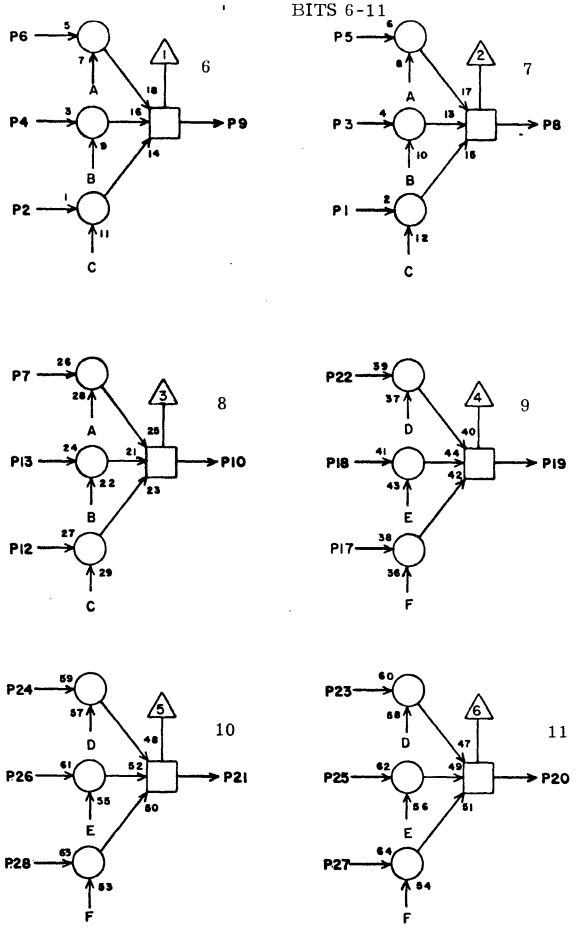
Rev A

LS 63063700 ASSY | REV

PARITY BITS 6-11

TE

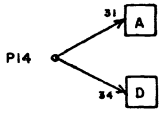
F14



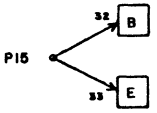
1			
2			
3	J04	21	19
4	J04	26	19
5	H07	6	13
6	H07	3	11
7	H07	10	13
8	F16	1	5
9	F16	5	5
10	F16	13	5
11			
12			
13	J05	5	17
14	F04	12	13
15	E10	16	7
16	F14	X	2
17			
18	J05	8	17
19	F16	18	5
20	F16	24	5
21	F16	28	5
22	H07	17	11
23	H07	26	13
24	H07	18	11
25	J05	21	17
26	J05	26	17
27			
28			

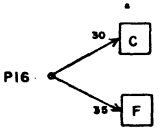
JACK PIN LG

WRITE 3



READ 3





CIRCUIT SPECIFICATION 11827600

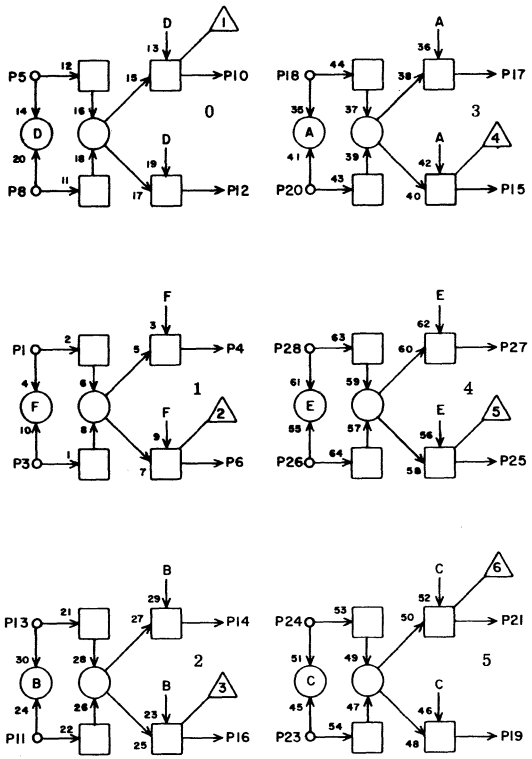
60196300

Rev A

LS 63040100 ASSY | E REV

LOGICAL EQUIVALENTS NETWORK - PARITY BITS 0-5

AB



F15

	JACK	PIN	LG
1	F13	8	5
2			
3	E15	6	5
4	G14	8	7
5	F13	9	5
6			
7			
8	E15	3	7
9			
10	G14	7	5
11	E15	10	5
12			
13	F13	10	5
14	G14	23	7
15			
16			
17	G14	24	7
18	F13	19	5
19			
20	E15	17	5
21	G15	8	5
22			
23	E15	26	5
24	F13	20	5
25			
26	E15	18	7
27	G15	7	5
28	F13	21	5

CIRCUIT SPECIFICATION 11827600

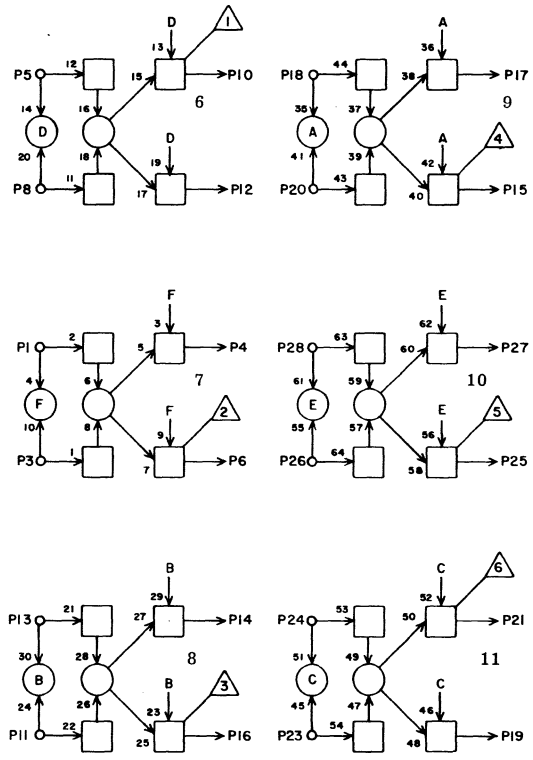
60196300

Rev A

LS 63040100 ASSY | E REV

LOGICAL EQUIPMENTS NETWORK - PARITY BITS 6-11

AB



E16

	JACK	PIN	LG
1	F14	8	5
2			
3	E16	6	5
4	G15	24	7
5	F14	9	5
6			
7			
8	E16	3	5
9			
10	G15	23	7
11	E16	10	5
12			
13	F14	10	5
14	G16	7	5
15			
16			
17	G16	8	5
18	F14	19	5
19			
20	E16	17	5
21	G16	24	5
22			
23	E16	26	5
24	F14	20	5
25			
26	E16	18	7
27	G16	23	5
28	F14	21	5

CIRCUIT SPECIFICATION 11827600

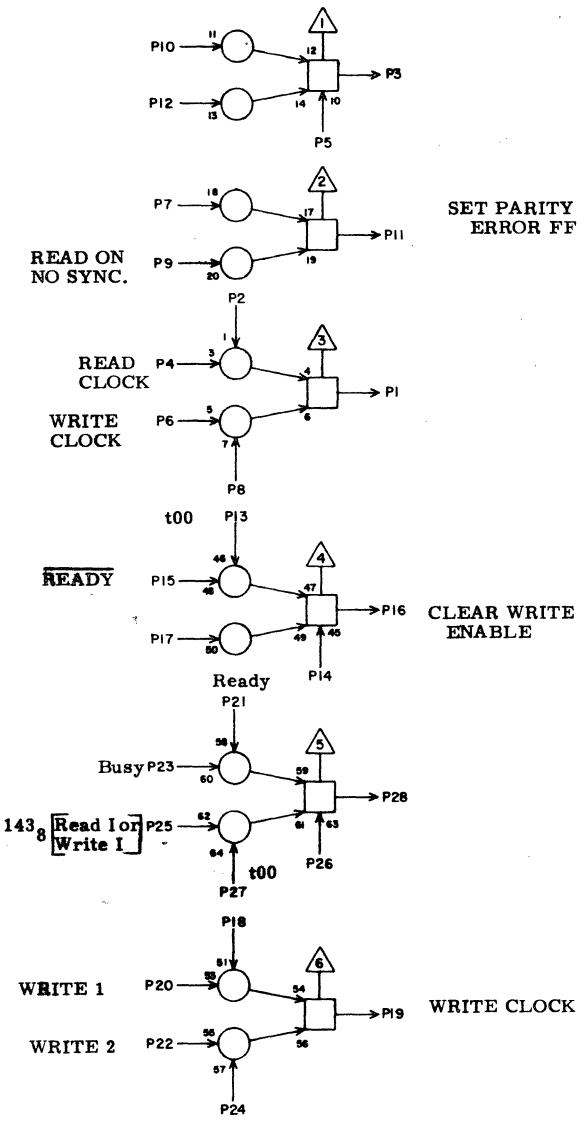
60196300

Rev A

LS 63060700 ASSY [C] REV

QN

G01



1	F01	25	5
2	D12	12	17
3			
4	K03	6	15
5			
6	G01	19	3
7	D12	19	17
8	E09	12	13
9	G08	12	9
10			
11	D08	5	15
12			
13	J09	9	15
14	G01	X	2
15	F04	5	9
16	F05	21	7
17	D12	22	17
18	G05	28	7
19	G01	6	3
20	K03	4	13
21	F04	13	9
22	K03	25	15
23	C08	20	19
24	G05	25	7
25	K10	14	17
26	G01	X	2
27	J09	11	120
28	D10	22	19

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

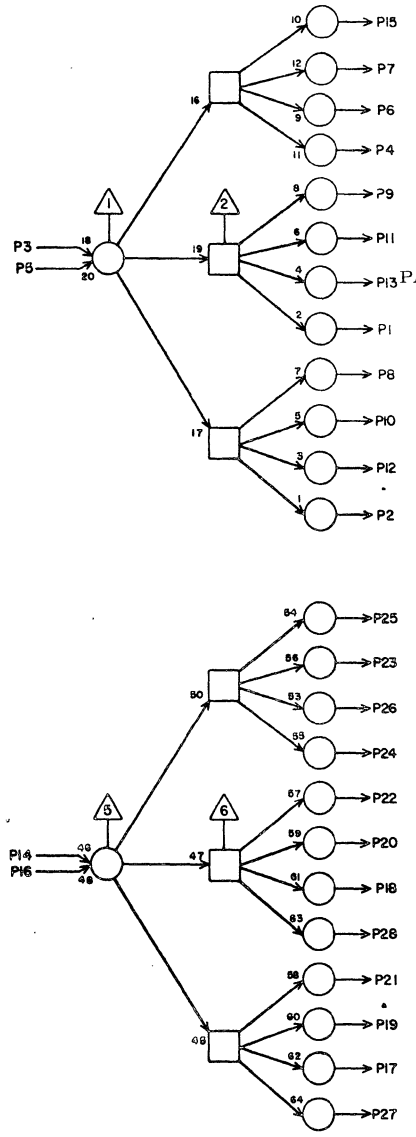
60196300

Rev A

LS 63063500 ASSY [D] REV

TC

G02



1	G10	5	11
2	G10	23	11
3	F07	16	9
4	G09	22	11
5	F07	15	9
6	G09	7	11
7	G09	5	11
8	G10	7	11
9	G09	24	9
10	G10	22	11
11	G09	23	9
12	G10	24	11
13	G10	6	11
14			
15	G09	6	9
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			

JACK PIN LG

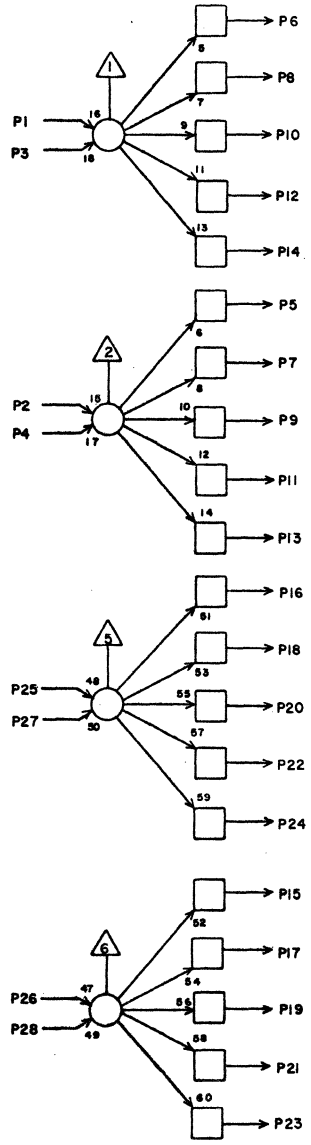
CIRCUIT SPECIFICATION 11827600

60196300

Rev A

LS 63063600 C
ASSY REV

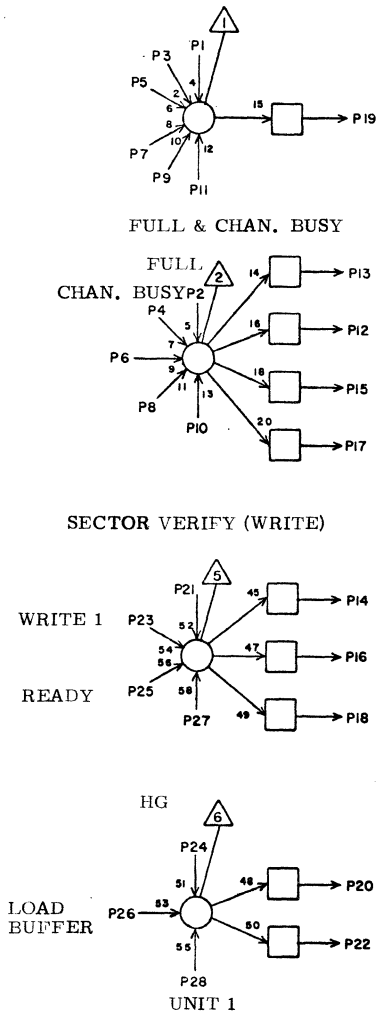
TD G03



1	G04	16	3
2	G07	20	7
3	F06	26	7
4	G03	X	2
5	D03	3	11
6			
7			
8	G07	14	7
9			
10			
11			
12	F05	22	5
13	G04	1	3
14	F07	26	7
15	G09	14	9
16			
17	G10	14	11
18			
19			
20	F05	5	7
21			
22	F05	15	7
23			
24	F07	24	9
25	F04	23	5
26	F06	20	7
27	F06	25	7
28	F04	17	7
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63063400
ASSY REV



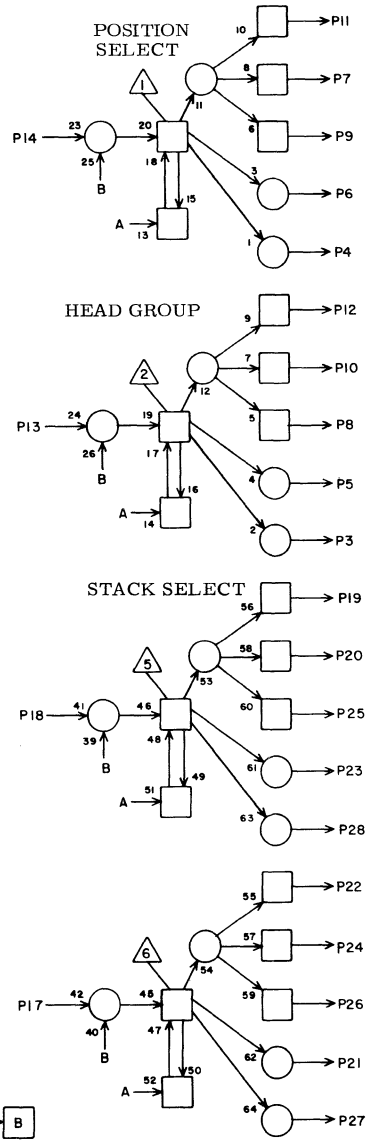
TB G04

1	G03	13	3
2	J02	21	13
3	E11	8	11
4	C10	20	17
5	G04	X	2
6	G04	X	2
7	G04	X	2
8	G04	X	2
9	G04	X	2
10	G04	X	2
11	G04	X	2
12			
13	G12	3	13
14	F06	15	7
15			
16	G03	1	3
17			
18	E09	21	11
19	G11	26	9
20	D10	15	15
21	F06	3	7
22	D10	16	15
23	G07	10	5
24	B07	7	21
25	D03	13	13
26	E11	11	13
27	G04	X	2
28	C10	21	17
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63057900 ASSY B REV

PD G05



T4 P16 43 A 44 B

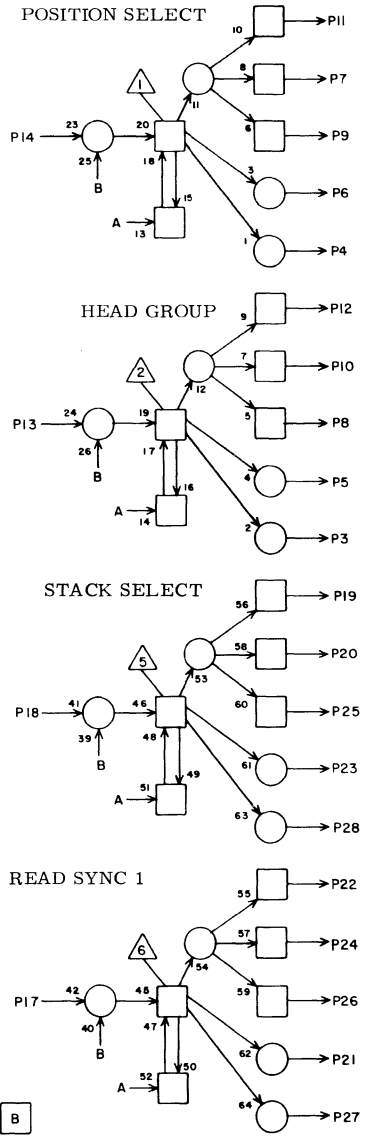
1			
2			
3			
4	G07	24	5
5	J07	4	13
6	J07	2	13
7	H13	10	11
8	G07	28	5
9	D08	11	13
10	H13	12	13
11	E02	5	9
12	F06	7	7
13	G06	10	3
14	G06	7	5
15			
16	E05	16	9
17			
18	G06	19	5
19	A07	14	21
20			
21			
22			
23	A07	15	21
24			
25	G01	24	7
26			
27			
28	G01	18	7

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63057900 ASSY B REV

PD G06



T3 P16 43 A 44 B

1			
2			
3			
4			
5			
6			
7	G05	14	5
8			
9	G07	22	5
10	G05	13	3
11	J07	21	13
12	J07	22	13
13	E13	19	11
14	D08	1	13
15			
16	E05	13	9
17	E13	16	11
18	F09	11	7
19	G05	18	5
20	D02	24	13
21			
22	E12	3	13
23	D02	18	13
24			
25	D02	27	13
26			
27			
28	D02	21	13

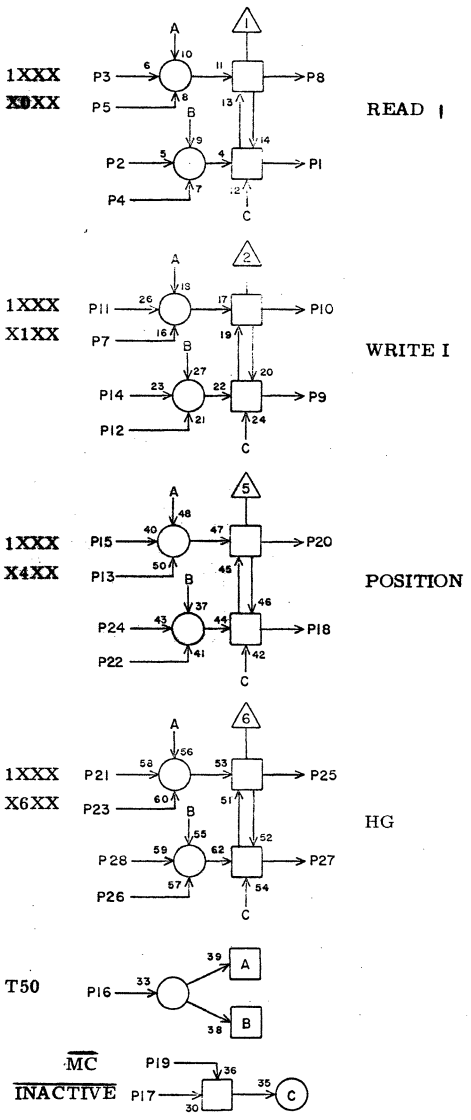
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63040400 C
ASSY REV

AE

G07



1	J07	15	13
2	C10	5	19
3	K08	18	15
4	G07	X	2
5	I03	16	11
6			
7	I04	16	11
8	E12	23	11
9	J07	17	13
10	G04	23	5
11	K08	20	15
12	G07	X	2
13	H14	12	11
14	G03	8	7
15	K08	16	15
16	J09	16	11
17	F11	27	9
18			
19	G11	6	7
20	G03	2	7
21	K08	22	15
22	G06	9	5
23	H14	13	11
24	G05	4	5
25	B07	1	19
26	G07	X	2
27			
28	G05	8	5

JACK PIN LG

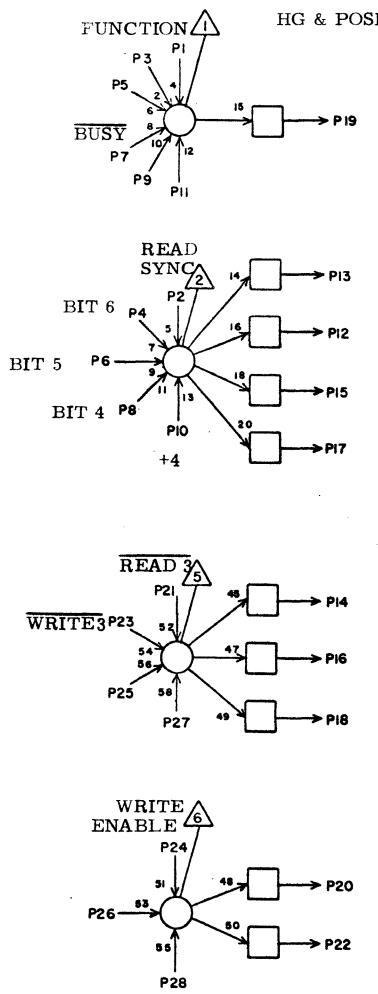
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63063400
ASSY REV

TB

G08



1	H05	2	7
2	F01	8	11
3	G13	22	11
4	E09	16	9
5	F01	19	9
6	C12	8	15
7	F11	6	9
8	C12	9	17
9	G08	X	2
10	E05	28	9
11	G08	X	2
12	G01	9	9
13	H13	27	11
14	G14	13	11
15			
16	G15	13	11
17			
18	G16	13	11
19	H13	17	9
20	I09	20	9
21	E10	10	9
22	I10	20	9
23	F04	10	9
24	F04	8	9
25	G08	X	2
26	F11	7	9
27	G08	X	2
28	G08	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

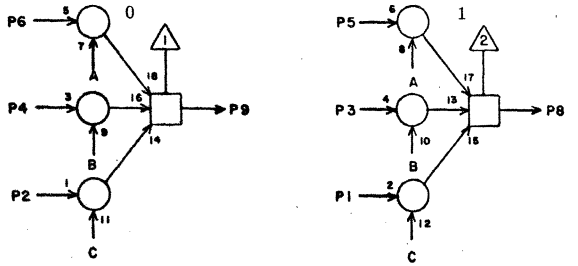
60196300
Rev A

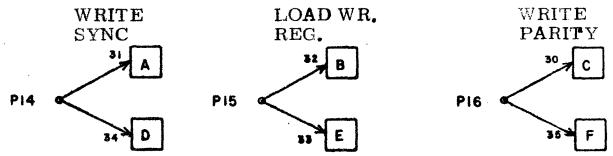
LS 63063700 ASSY [C] REV

WRITE FAN-IN GATES BITS 0 - 5

TE

G09





	JACK	PIN	LG
1	E15	11	11
2	E15	1	11
3	H08	2	5
4	H08	1	5
5	G02	7	11
6	G02	15	9
7	G02	6	11
8	H06	5	7
9	H06	8	7
10	H06	12	7
11			
12	E15	14	11
13	H08	14	5
14	G03	15	9
15	G11	27	5
16	E10	8	9
17	E15	15	11
18	H08	19	5
19	H06	21	7
20	H06	23	7
21	H06	24	7
22	G02	4	9
23	G02	11	9
24	G02	9	9
25	H08	28	5
26	H08	27	5
27	E15	25	11
28	E15	27	11

CIRCUIT SPECIFICATION 1182760D

801 [illegible]300

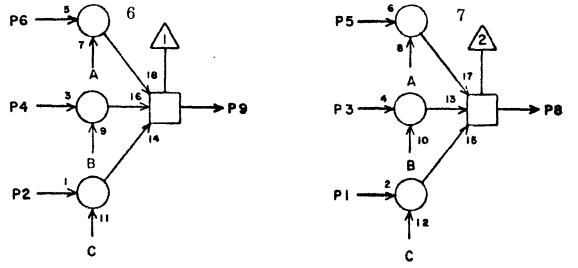
Rev A

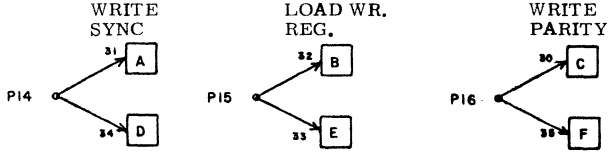
LS 63063700 ASSY [ ] REV

WRITE FAN-IN GATES BITS 6 - 11

TE

G10





	JACK	PIN	LG
1	E16	11	11
2	E16	1	11
3	H09	2	5
4	H09	1	5
5	G02	1	11
6	G02	13	11
7	G02	8	11
8	H07	5	7
9	H07	8	7
10	H07	12	7
11			
12	E16	14	11
13	H09	14	5
14	G03	17	11
15	G11	16	3
16	E10	7	9
17	E16	15	11
18	H09	19	7
19	H07	21	9
20	H07	23	9
21	H07	24	9
22	G02	10	11
23	G02	2	11
24	G02	12	11
25	H09	28	7
26	H09	27	7
27	E16	25	11
28	E16	27	11

CIRCUIT SPECIFICATION 1182760D

80196300

Rev A

LS 63042900 B
ASSY REV

CX

G11

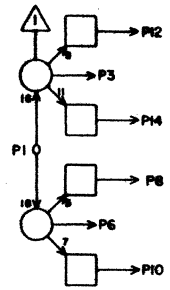
1	I05	28	13
2	I06	21	11
3	F04	25	9
4			
5			
6	G07	19	7
7	F08	2	7
8			
9	I05	10	11
10			
11	F08	23	11
12			
13	F08	7	11
14			
15	D07	17	13
16	G10	15	3
17	D05	7	15
18			
19	D05	22	13
20			
21	C06	7	17
22	G12	14	3
23	C06	22	17
24			
25	H13	3	5
26	G04	19	9
27	G09	15	5
28			

JACK PIN LG

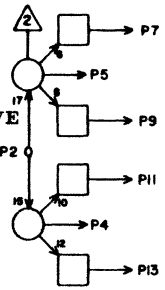
CIRCUIT SPECIFICATION 11327600

60196300
Rev A

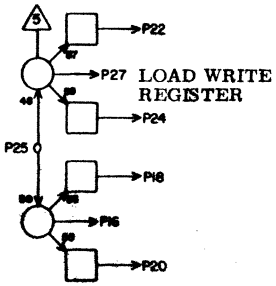
MC

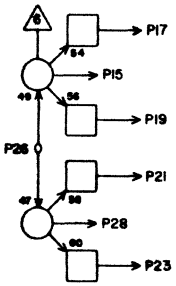


INACTIVE



LOAD POSITION REGISTER (UNIT 0 & 1)





LS 63040400 C
ASSY REV

AE

G12

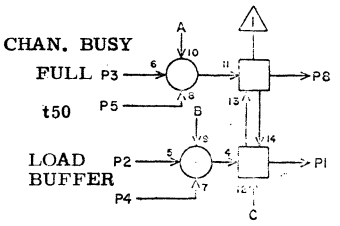
1			
2	E11	12	9
3	G04	13	13
4	G12	X	2
5	J09	17	13
6			
7	F11	9	5
8	H13	13	7
9	G13	28	3
10			
11	J09	2	13
12	E07	14	11
13	G13	7	3
14	G11	22	3
15	C10	22	15
16	G12	X	2
17	F11	21	7
18	H05	16	11
19	F04	18	11
20	F08	24	9
21	F08	16	9
22	G12	X	2
23	J09	21	13
24	H05	10	11
25	E13	2	11
26	E10	21	9
27			
28	G12	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11327600

60196300
Rev A

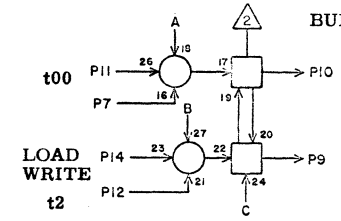
CHAN. BUSY
FULL P3
t50 P5
LOAD BUFFER P2
P4

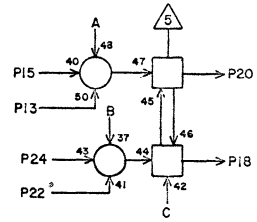


FULL

BUFFER LOADED

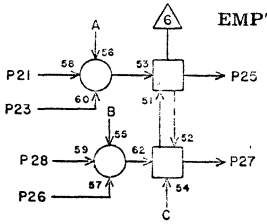
t00 P11
P7
LOAD WRITE t2 P14
P12

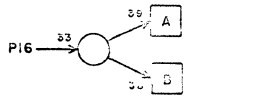




EMPTY

t50





MC
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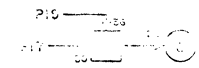
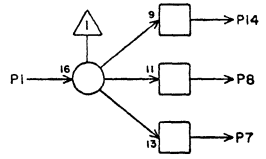


LS 63064000 ASSY | REV

TH

ACTIVE



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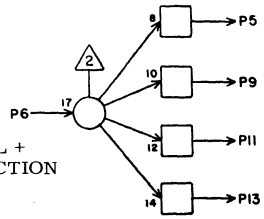
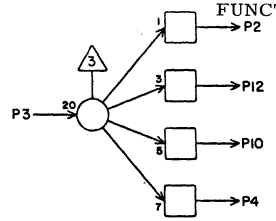
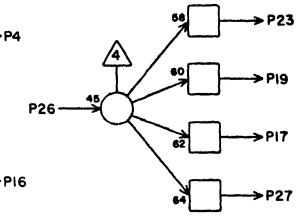
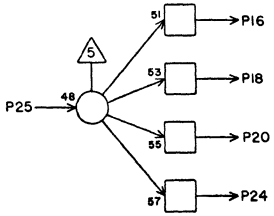


FULL + FUNCTION



READ 3





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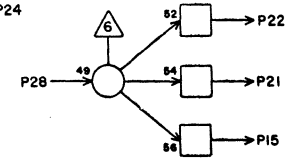

G13

1	I06	8	13
2	H10	16	7
3	H13	1	5
4			
5	F10	15	7
6	F10	3	7
7	G12	13	3
8	F08	15	9
9			
10	H12	16	5
11	F07	28	9
12	H11	16	7
13	F08	25	9
14			
15	H13	15	5
16	D03	8	19
17			
18	D03	7	19
19	D12	5	13
20			
21	F05	18	11
22	G08	3	11
23	F10	22	7
24			
25	D08	26	15
26	F10	26	7
27			
28	G12	9	3

JACK PIN LG

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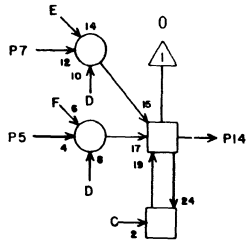
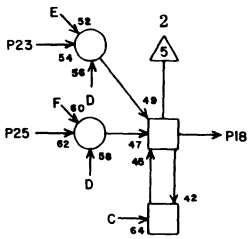
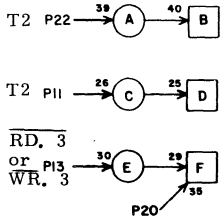
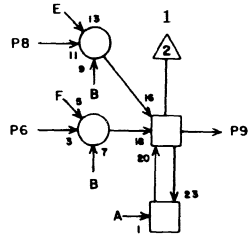


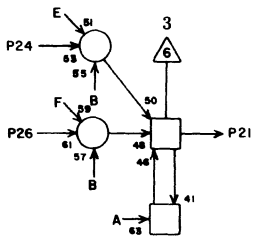


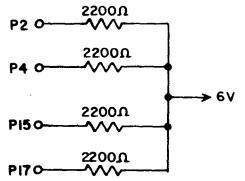


PARITY REGISTER 1
BITS 0 - 3

PC







G14

1			
2	G14	5	3
3			
4	G14	6	3
5	G14	2	3
6	G14	4	3
7	F15	10	5
8	F15	4	7
9	E15	12	9
10			
11	E04	20	15
12			
13	G08	14	11
14	E15	5	9
15	G14	25	3
16			
17	G14	26	3
18	E15	21	9
19			
20	G14	X	2
21	E15	24	9
22	E04	18	15
23	F15	14	7
24	F15	17	7
25	G14	15	3
26	G14	17	3
27			
28			

JACK PIN LG

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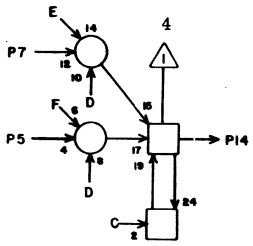
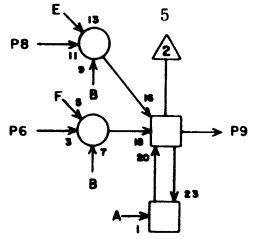
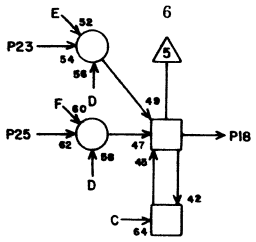
ASSY REV

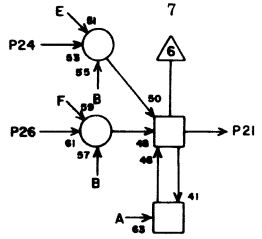
PARITY REGISTER 1
BITS 4-7

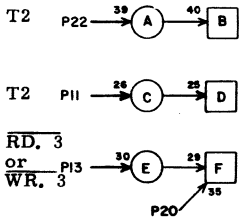
PC G15

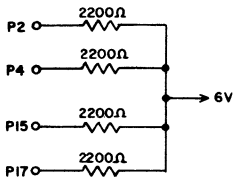












1			
2	G15	5	3
3			
4	G15	6	3
5	G15	2	3
6	G15	4	3
7	F15	27	5
8	F15	21	5
9	E16	8	9
10			
11	E04	17	15
12			
13	G08	16	11
14	E15	23	7
15	G15	25	3
16			
17	G15	26	3
18	E16	5	9
19			
20	G15	X	2
21	E16	12	9
22	E04	22	15
23	F16	10	7
24	F16	4	7
25	G15	15	3
26	G15	17	3
27			
28			

JACK PIN LG

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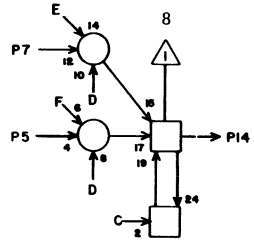
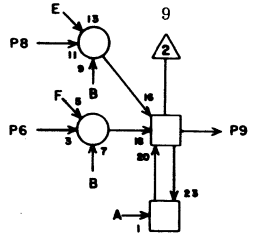
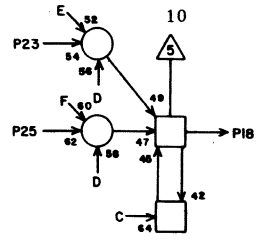
ASSY REV

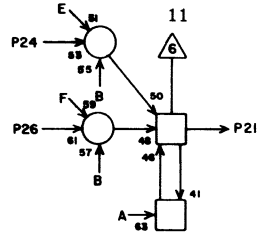
PARITY REGISTER 1
BITS 8 -11

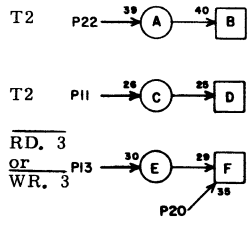
PC G16

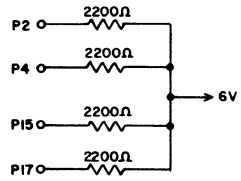












1			
2	G16	5	3
3			
4	G16	6	3
5	G16	2	3
6	G16	4	3
7	F16	14	5
8	F16	17	5
9	E16	24	7
10			
11	E04	21	15
12			
13	G08	18	11
14	E16	21	7
15	G16	25	3
16			
17	G16	26	3
18	E16	23	7
19			
20	G16	X	2
21	E15	8	9
22	E04	19	17
23	F16	27	5
24	F16	21	5
25	G16	15	3
26	G16	17	3
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064100 ASSY | C REV

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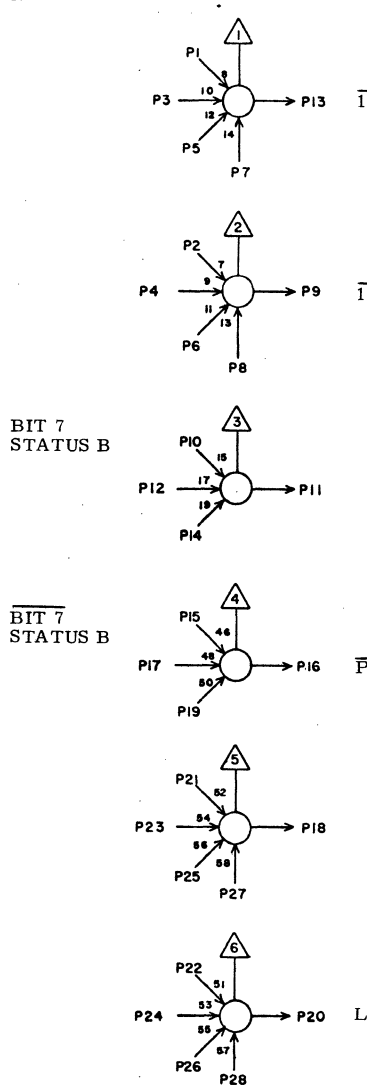
H04



SECTOR COUNTER 0 — $\overline{143}_8$

SECTOR COUNTER 1 — $\overline{143}_8$

BIT 7 STATUS B

$\overline{\text{STATUS FULL B}}$

$\overline{\text{BIT 7}}$ STATUS B

$\overline{\text{POSITION FULL B}}$

LOST DATA

	JACK	PIN	LG
1	B06	25	23
2	A06	25	25
3	B06	8	23
4	A06	8	25
5	B05	8	23
6	A05	8	25
7	B05	9	23
8	A05	9	25
9	D03	26	17
10	H16	27	15
11	J02	1	9
12	J08	21	11
13	D03	23	17
14	H04	X	2
15	H16	16	15
16	J02	3	9
17	J08	22	9
18	K09	25	15
19	H04	X	2
20	F08	20	9
21	I04	13	5
22	H05	20	3
23	I03	13	5
24	H04	X	2
25	H04	X	2
26	H04	X	2
27	H04	X	2
28	H04	X	2

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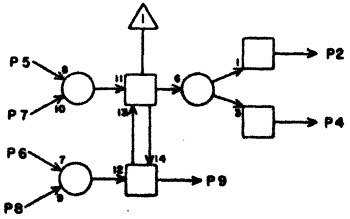
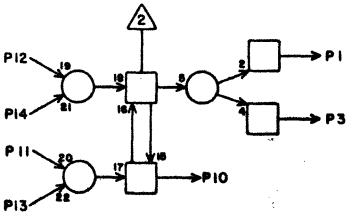
REV D

AA

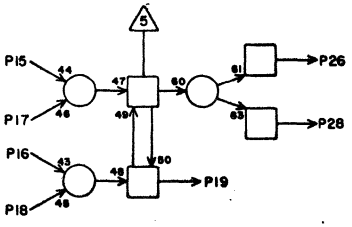
FUNCTION & HG + POSITION



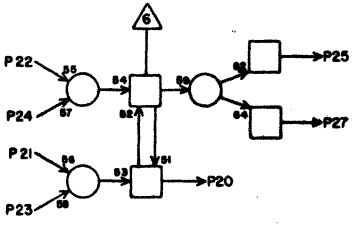
CHANNEL BUSY



END OF BUFFER



LOST DATA



H05

1	C10	25	17
2	G08	1	7
3	H05	17	3
4			
5	K09	19	13
6	E11	14	13
7	H05	X	2
8	H05	X	2
9			
10	G12	24	11
11	I05	3	7
12	K09	14	13
13	J09	24	13
14	H05	X	2
15	I05	16	5
16	G12	18	11
17	H05	3	3
18	H05	X	2
19	D10	24	17
20	H04	22	3
21	K09	16	13
22	H05	26	3
23	H05	X	2
24	I05	11	5
25	I13	25	11
26	H05	22	3
27	I16	25	13
28	F08	18	9

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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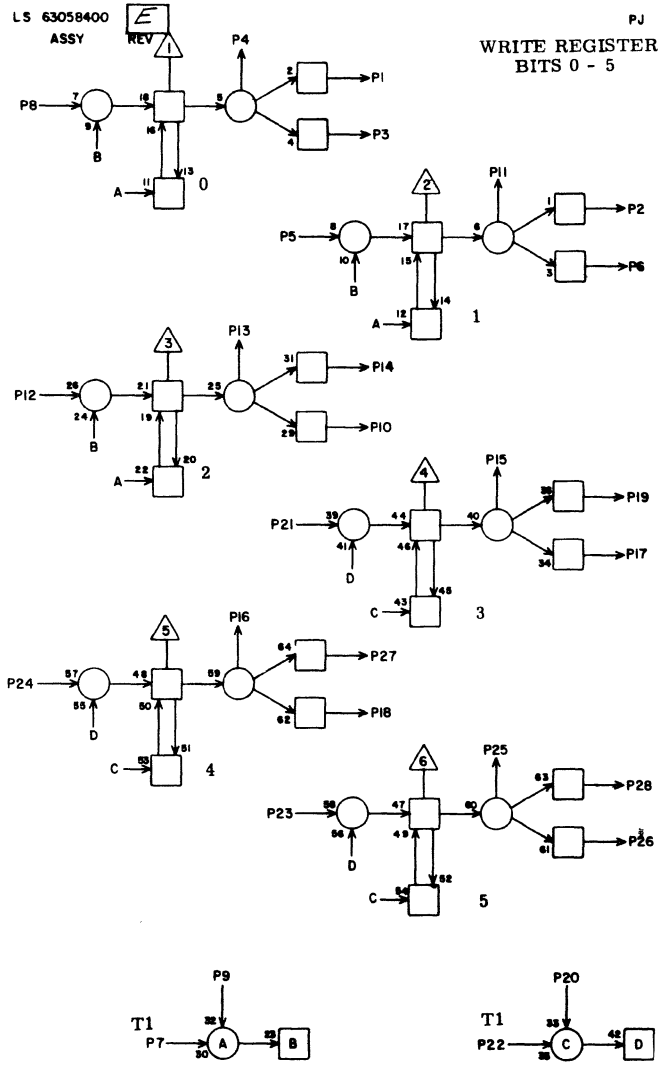
REV E

PJ

WRITE REGISTER BITS 0 - 5



H06

1	I03	4	7
2	I03	10	7
3	F13	6	11
4			
5	G09	8	7
6	F13	5	13
7	E04	4	13
8	G09	9	7
9	H06	X	2
10	F13	7	13
11			
12	G09	10	7
13			
14	I03	1	5
15			
16			
17	F13	22	11
18	F13	24	11
19	I03	28	7
20	H06	X	2
21	G09	19	7
22	E04	6	13
23	G09	20	7
24	G09	21	7
25			
26	F13	23	13
27	I03	22	7
28	I03	25	7

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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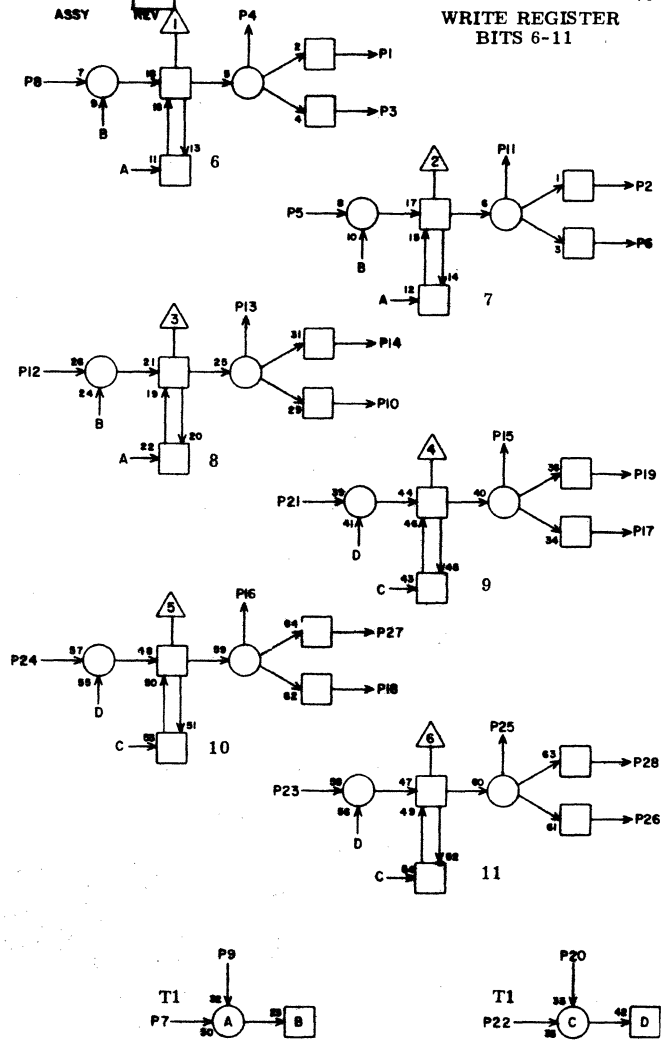
LS 63058400 E
ASSY REV 1

PJ

WRITE REGISTER BITS 6-11



H07

1	I04	4	7
2	I04	10	7
3	F14	6	11
4			
5	G10	8	7
6	F14	5	13
7	E04	9	13
8	G10	9	7
9	H07	X	2
10	F14	7	13
11			
12	G10	10	7
13			
14	I04	1	5
15			
16			
17	F14	22	11
18	F14	24	11
19	I04	28	7
20	H07	X	2
21	G10	19	9
22	E04	11	13
23	G10	20	9
24	G10	21	9
25			
26	F14	23	13
27	I04	22	7
28	I04	25	7

JACK PIN LG

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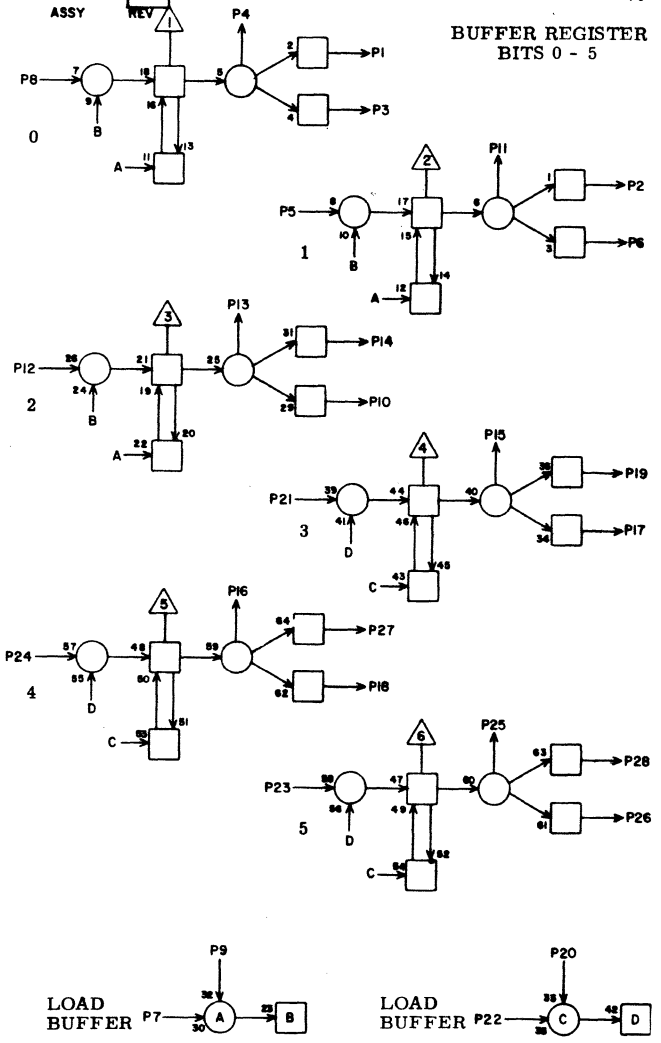
Rev A

LS 63058400 E
ASSY REV 1

PJ

BUFFER REGISTER BITS 0 - 5



H08

1	G09	4	5
2	G09	3	5
3			
4			
5	H10	3	5
6			
7	E11	2	13
8	H10	4	5
9	H08	X	2
10			
11			
12	H10	28	5
13			
14	G09	13	5
15			
16			
17			
18			
19	G09	18	5
20	H08	X	2
21	H10	27	5
22	E11	4	13
23	H11	3	7
24	H11	4	7
25			
26			
27	G09	26	5
28	G09	25	5

JACK PIN LG

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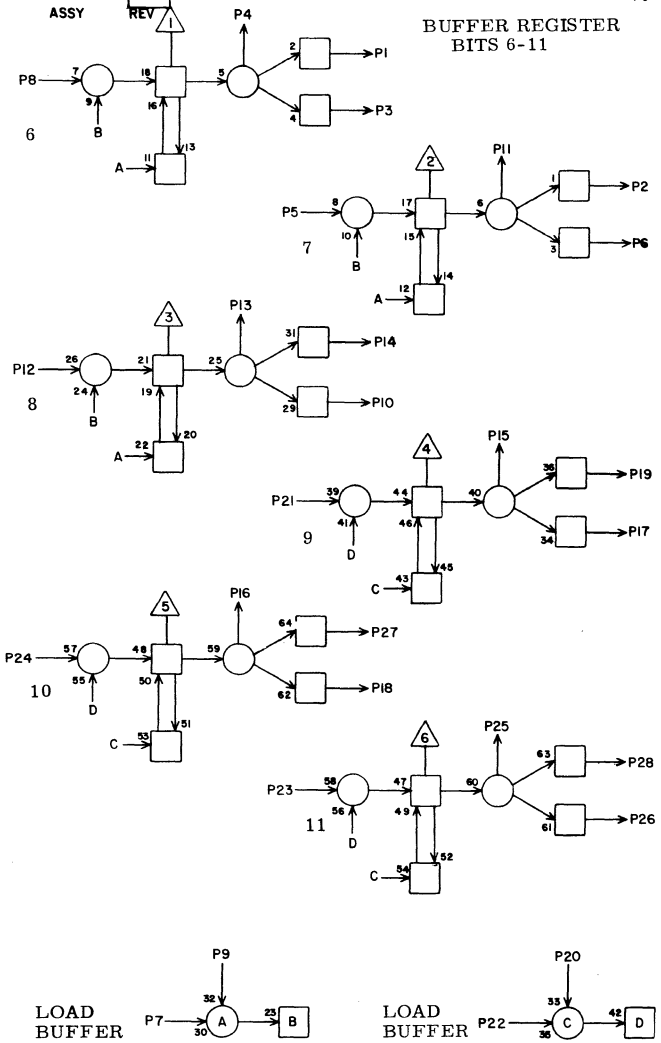
PJ

H09

BUFFER REGISTER
BITS 6-11



1	G10	4	5
2	G10	3	5
3			
4			
5	H11	27	5
6			
7	E11	6	11
8	H11	28	5
9	H09	X	2
10			
11			
12	H12	4	7
13			
14	G10	13	5
15			
16			
17			
18			
19	G10	18	7
20	H09	X	2
21	H12	3	7
22	E11	9	13
23	H12	27	5
24	H12	28	5
25			
26			
27	G10	26	7
28	G10	25	7

JACK PIN LG

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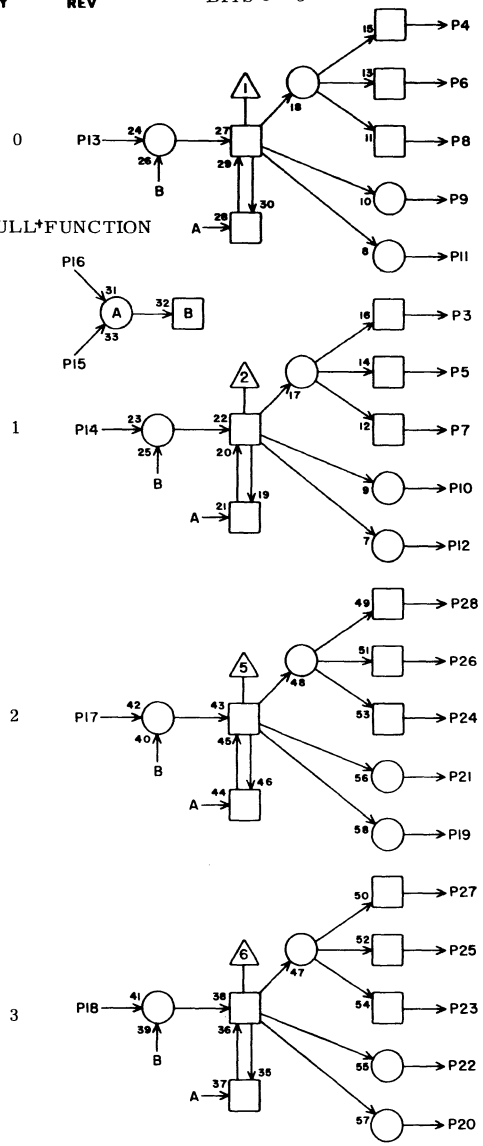
LS 63058900 ASSY B REV

PO

H10

HOLDING REGISTER
BITS 0 - 3



1			
2			
3	H08	5	5
4	H08	8	5
5	D05	5	15
6	D05	8	15
7	C06	5	19
8	C06	8	19
9	C08	22	17
10	C08	21	17
11			
12			
13	I07	9	7
14	I07	10	7
15	J09	18	9
16	G13	2	7
17	I07	21	7
18	I07	8	7
19	I10	5	5
20	F07	2	11
21	C08	23	17
22	C08	24	17
23	C06	21	19
24	C06	12	19
25	D05	21	15
26	D05	12	17
27	H08	21	5
28	H08	12	5

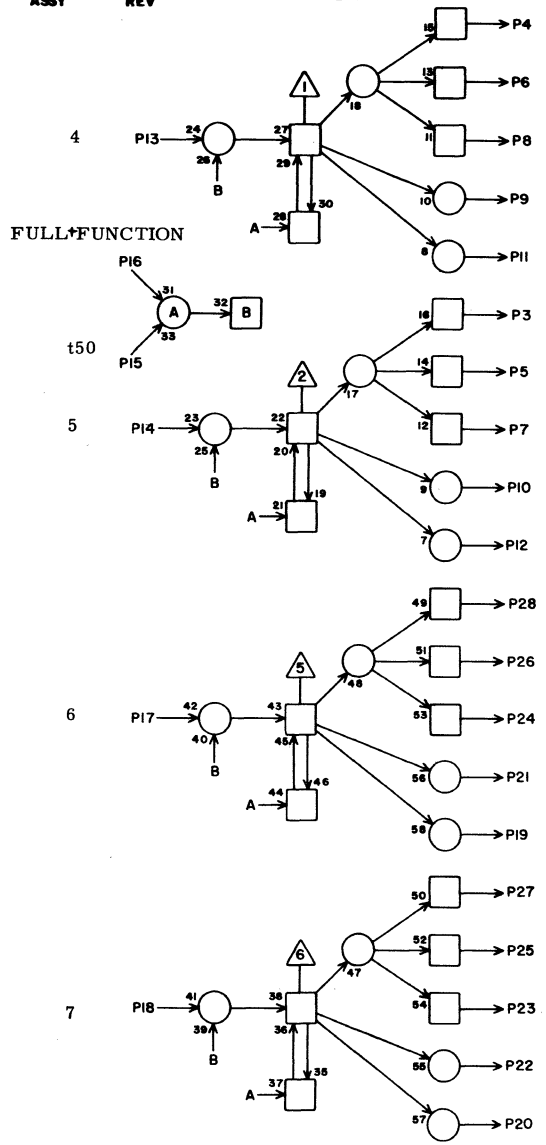
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63058900 ASSY B REV

HOLDING REGISTER BITS 4 - 7



P0 H11

1			
2			
3	H08	23	7
4	H08	24	7
5	D05	23	17
6	I10	10	7
7	C06	23	17
8	F09	25	7
9	D10	13	15
10	C08	26	17
11	D10	18	15
12	F07	3	13
13	I07	19	7
14	I07	20	7
15	J09	20	9
16	G13	12	7
17	J08	10	9
18	J08	18	9
19			
20			
21			
22			
23			
24	K10	25	13
25			
26	A09	8	25
27	H09	5	5
28	H09	8	5

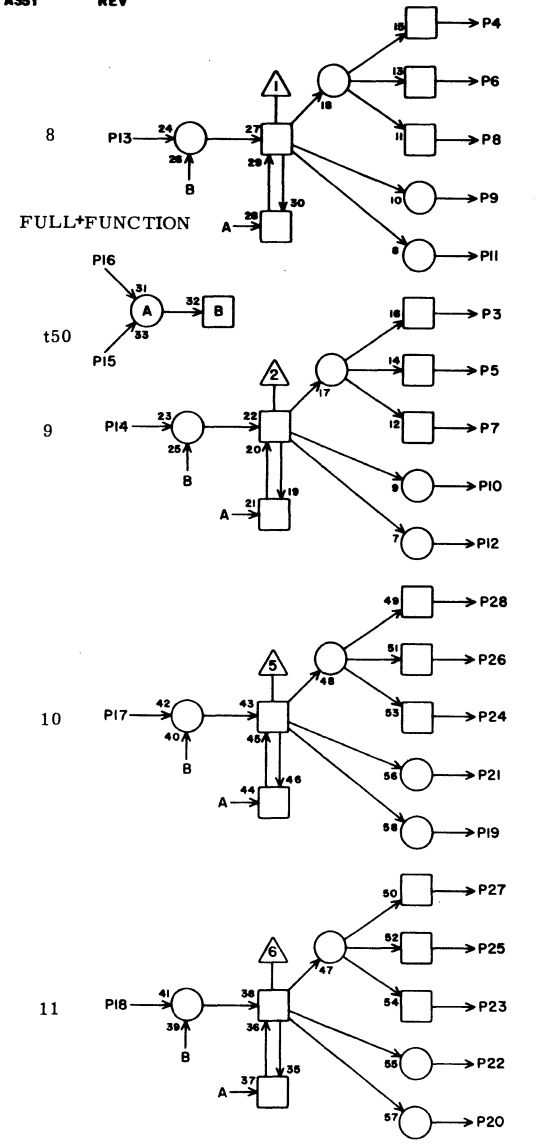
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63058900 ASSY B REV

HOLDING REGISTER BITS 8 - 11



P0 H12

1			
2			
3	H09	21	7
4	H09	12	7
5			
6			
7			
8			
9			
10			
11			
12			
13	J08	9	9
14	I08	8	7
15	J09	22	9
16	G13	10	5
17	I08	19	7
18	I08	20	7
19			
20			
21			
22			
23			
24			
25			
26			
27	H09	23	5
28	H09	24	5

JACK PIN LG

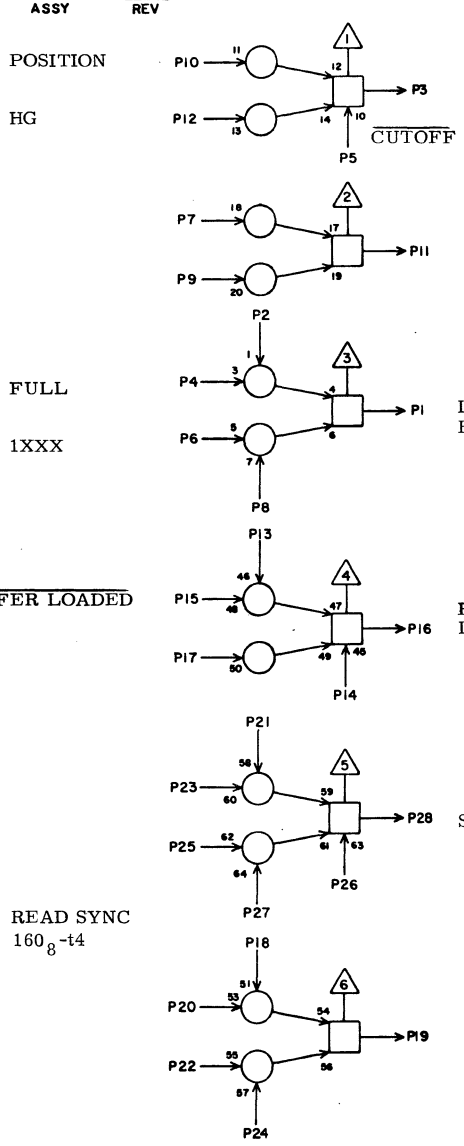
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63060700 ASSY C REV

QN

H13



		JACK	PIN	LG
1	G13	3	5
2	C10	16	17
3	G11	25	5
4	J02	22	17
5	F09	2	11
6	I06	20	11
7			
8	H13	X	2
9			
10	G05	7	11
11			
12	G05	10	11
13	G12	8	7
14	H13	X	2
15	G13	15	5
16	F12	14	9
17	G08	19	9
18			
19			
20			
21	E12	19	13
22			
23	H13	X	2
24	C09	15	19
25	H13	X	2
26	H13	X	2
27	G08	13	11
28	F10	12	11

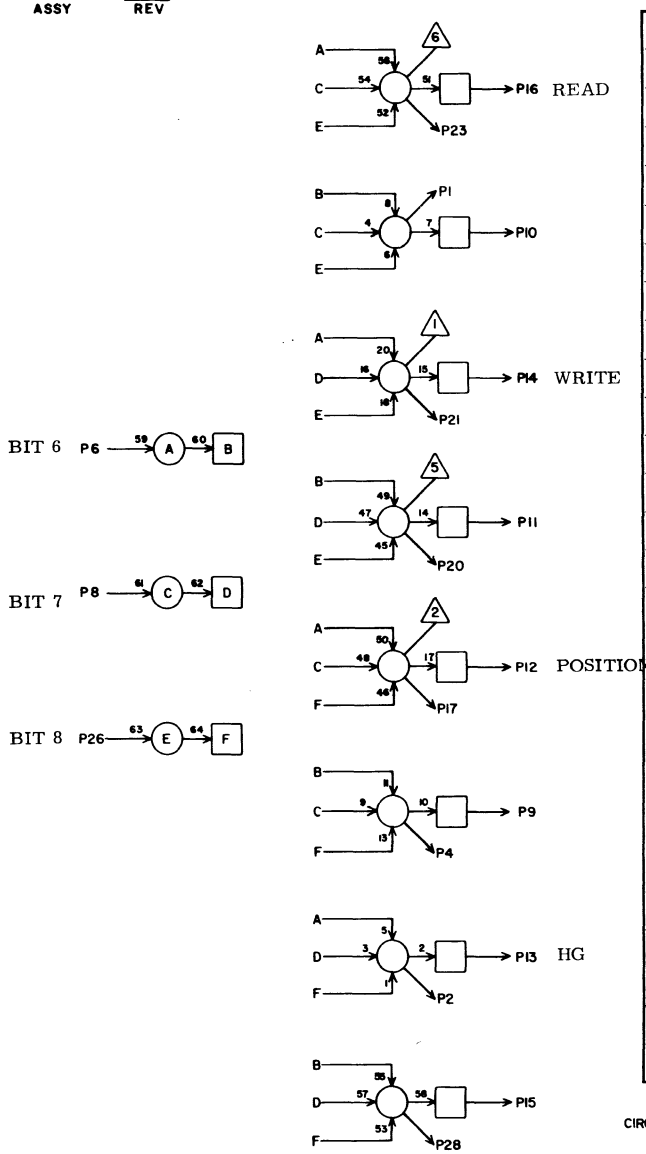
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63049300 ASSY D REV

IV

H14

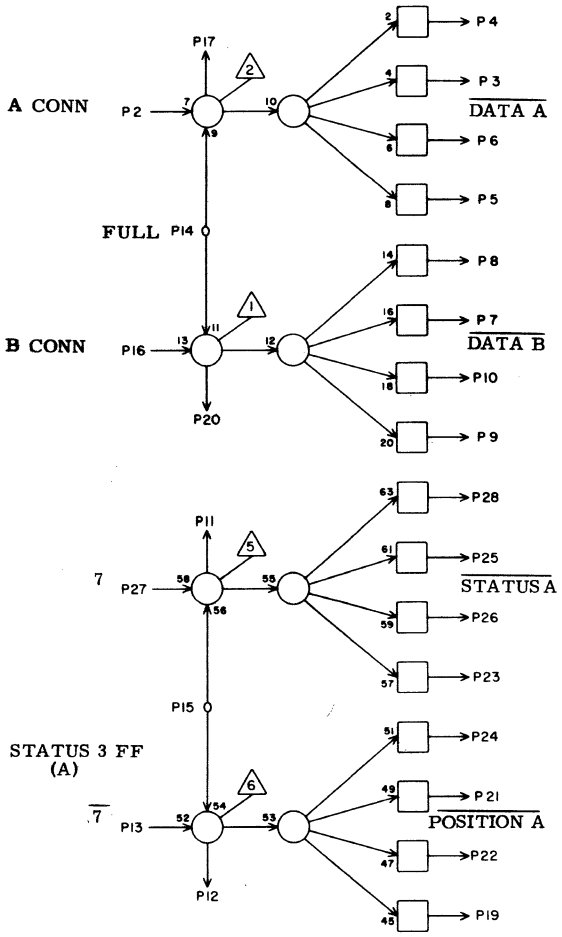


		JACK	PIN	LG
1	I03	14	15
2	E09	1	13
3			
4			
5			
6	J08	12	13
7			
8	J08	16	13
9			
10			
11			
12	G07	13	11
13	G07	23	11
14			
15			
16			
17	E09	3	13
18			
19			
20	I04	14	13
21	I04	19	13
22			
23	I03	19	15
24			
25			
26	J08	5	11
27			
28			

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 630532 ASSY | B REV | KL | H15

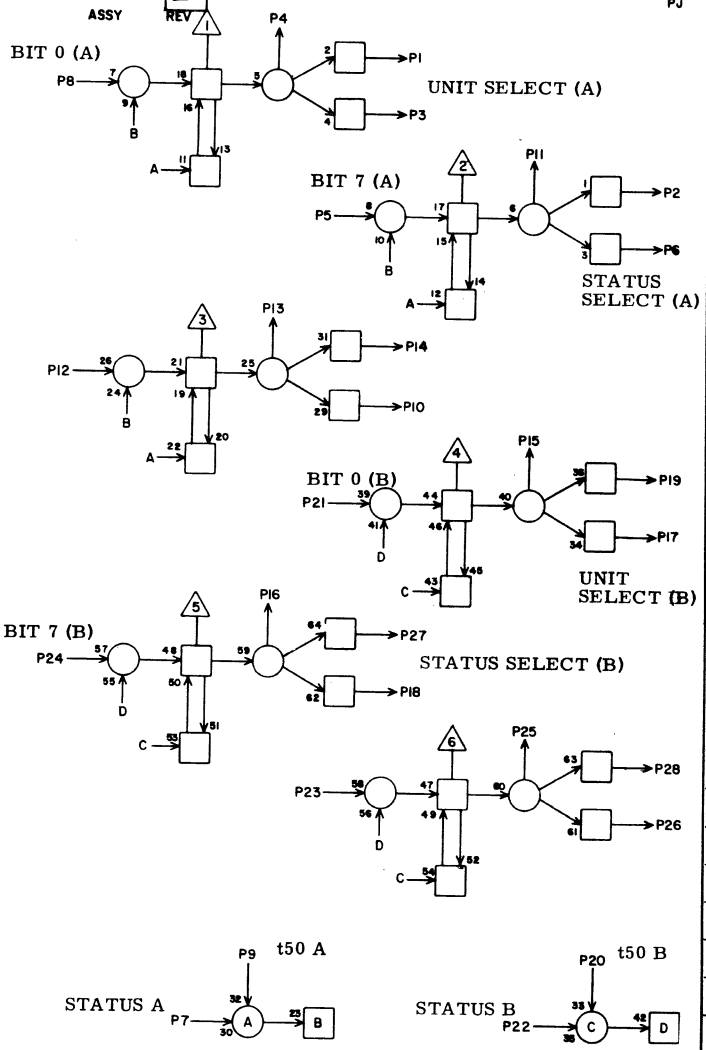


1			
2	J10	18	11
3	I12	11	7
4	I11	11	7
5	I13	11	7
6	I09	14	9
7	I15	11	5
8	I14	11	5
9	I16	11	5
10	I10	14	9
11			
12			
13	H16	11	3
14	F11	19	9
15	J08	8	13
16	J10	11	11
17			
18			
19			
20			
21	I12	15	7
22	I13	15	5
23			
24	I11	15	7
25	I12	16	7
26	I13	16	5
27	H16	2	5
28	I11	16	7

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63058400 ASSY | E REV | PJ | H16



1	I10	2	9
2	H15	27	5
3			
4	I09	2	11
5	L08	24	19
6			
7	K08	12	15
8	L07	7	17
9	J11	20	11
10			
11	H15	13	3
12	L08	9	17
13			
14	K04	5	19
15	I09	8	11
16	H04	15	15
17			
18			
19	I10	8	9
20	J14	20	9
21	L12	7	15
22	K08	11	15
23	L13	9	15
24	L13	24	15
25			
26			
27	H04	10	15
28	K04	15	19

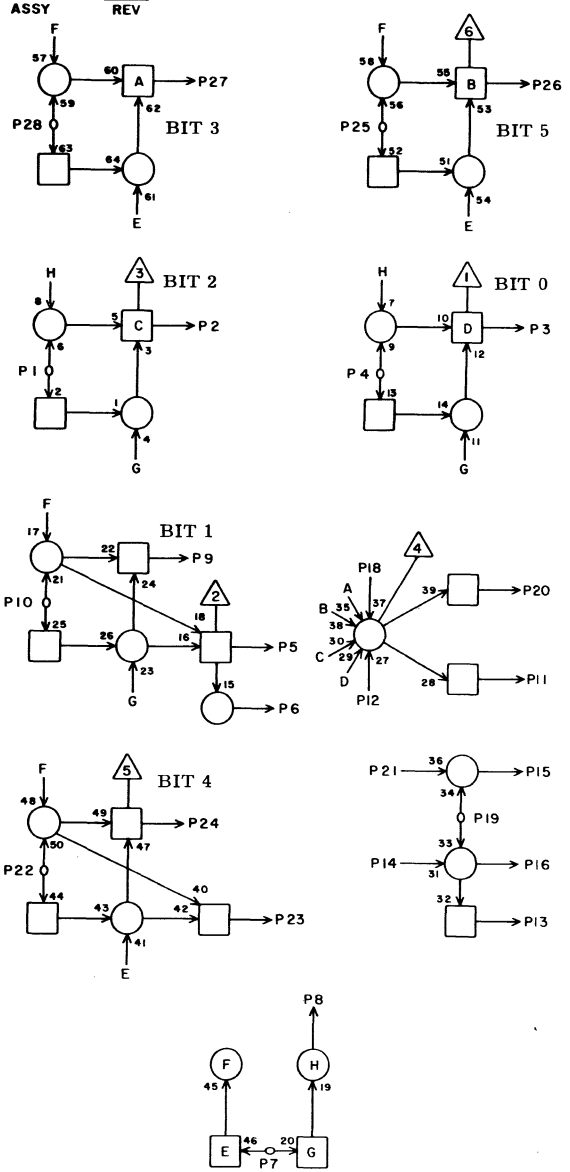
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63053800 ASSY B REV

KS

I03



1	H06	14	5
2	L01	24	13
3	L01	7	13
4	H06	1	7
5			
6			
7	A09	4	29
8	I04	7	3
9	L01	17	13
10	H06	2	7
11			
12			
13	H04	23	5
14	H14	1	15
15			
16	G07	5	11
17			
18			
19	H14	23	15
20			
21			
22	H06	27	7
23			
24	L02	17	11
25	H06	28	7
26	L02	24	11
27	L02	7	11
28	H06	19	7

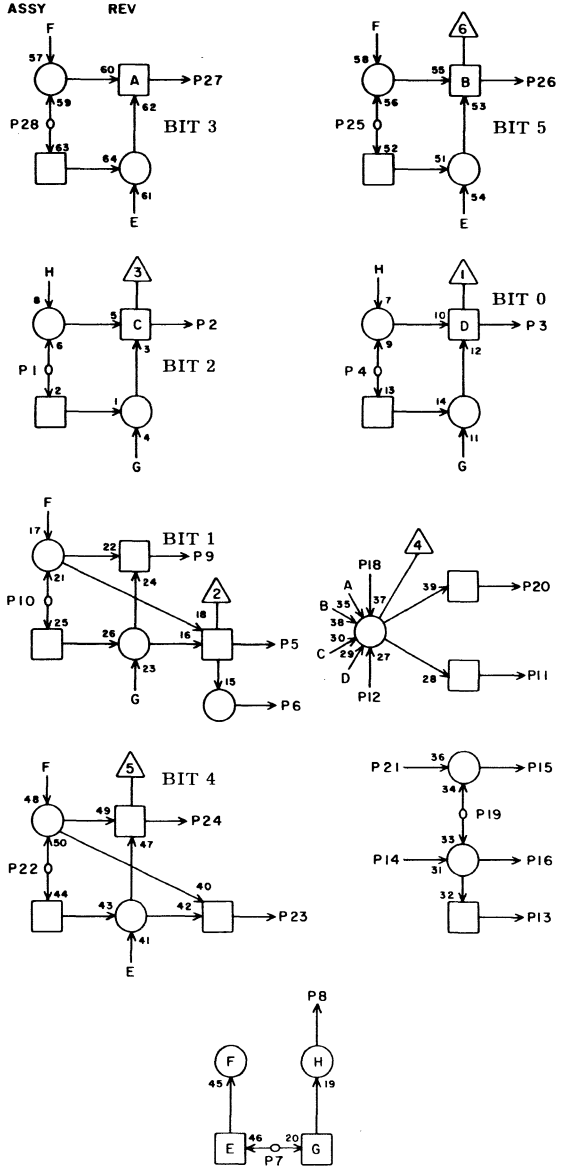
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63053800 ASSY B REV

KS

I04

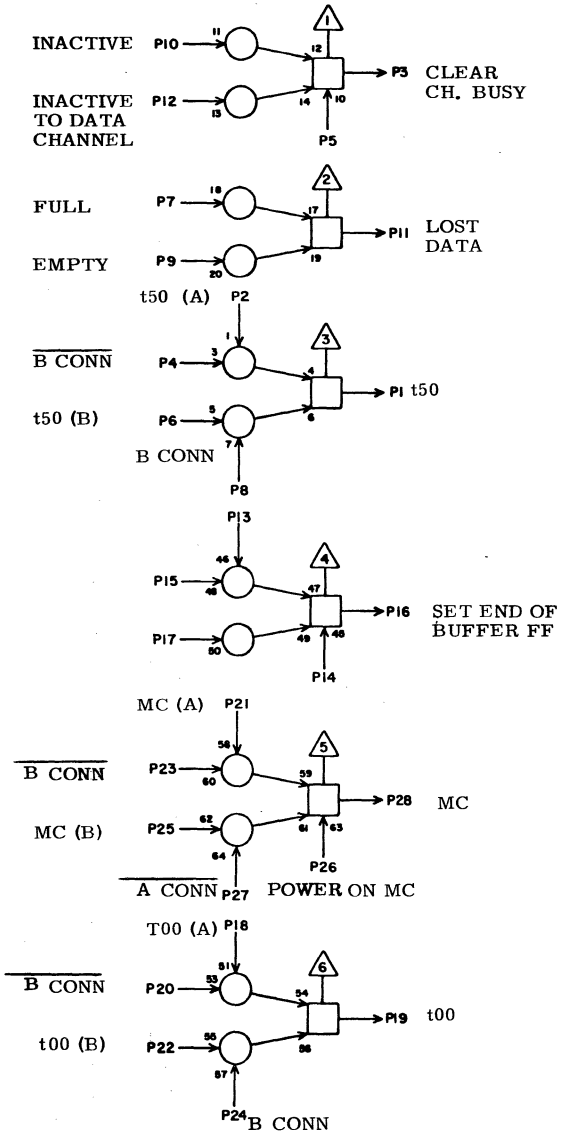


1	H07	14	5
2	L03	24	13
3	L03	7	13
4	H07	1	7
5			
6			
7	I03	8	3
8			
9	L03	17	13
10	H07	2	7
11			
12			
13	H04	21	5
14	H14	20	13
15			
16	G07	7	11
17			
18			
19	H14	21	13
20			
21			
22	H07	27	7
23			
24	L04	17	11
25	H07	28	7
26	L04	24	11
27	L04	7	11
28	H07	19	7

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63060700 ASSY C REV



QN

I05

1	J09	23	9
2	J13	5	11
3	H05	11	7
4	K07	1	11
5	F04	24	11
6	J16	5	15
7	J02	15	7
8	J10	5	9
9	J02	19	7
10	G11	9	11
11	H05	24	5
12	F12	24	13
13	F05	26	121
14	I05	X	2
15	F09	10	13
16	H05	15	5
17	E12	15	17
18	J13	23	13
19	J09	7	7
20	E10	11	17
21	L11	11	13
22	J16	23	15
23	K05	28	9
24	J10	9	9
25	L16	11	17
26	K08	15	11
27	E10	23	17
28	G11	1	13

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

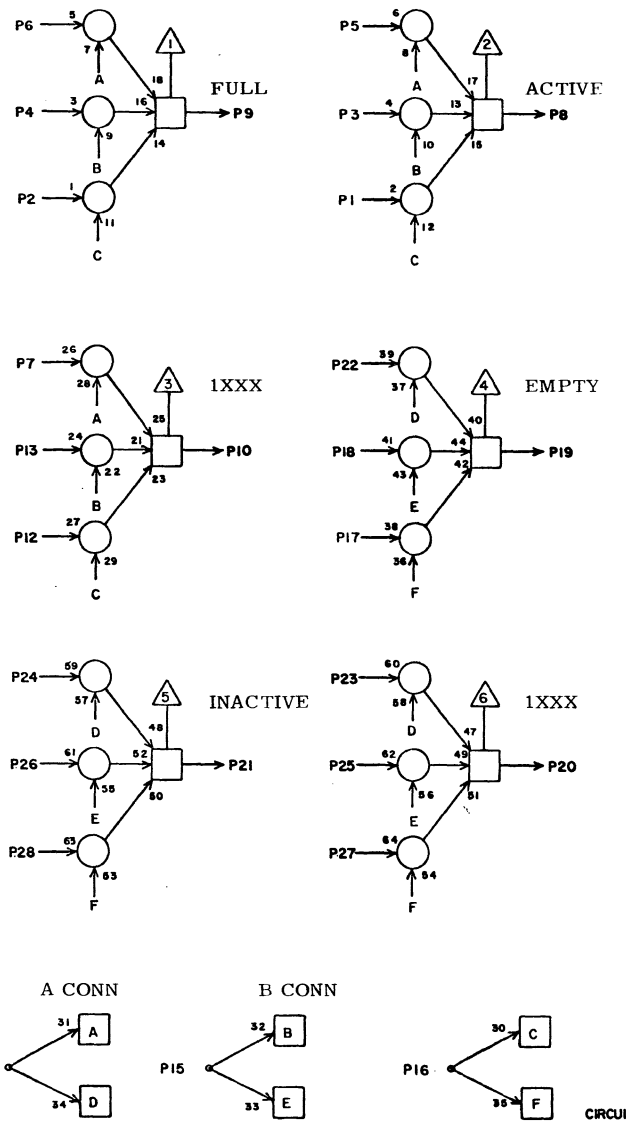
60136305

Rev A

LS 63063700 ASSY REV

TE

I06



1			
2			
3	L15	7	17
4	L15	18	17
5	L10	7	13
6	L10	18	13
7	K09	15	11
8	G13	1	13
9	J02	28	9
10	K08	25	11
11			
12			
13	K10	15	11
14	J10	10	7
15	J10	15	9
16	I06	X	2
17			
18	L15	22	15
19	J02	26	9
20	H13	6	11
21	G11	2	11
22	L10	22	13
23	K09	17	9
24	L10	9	11
25	K10	17	9
26	L15	9	15
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

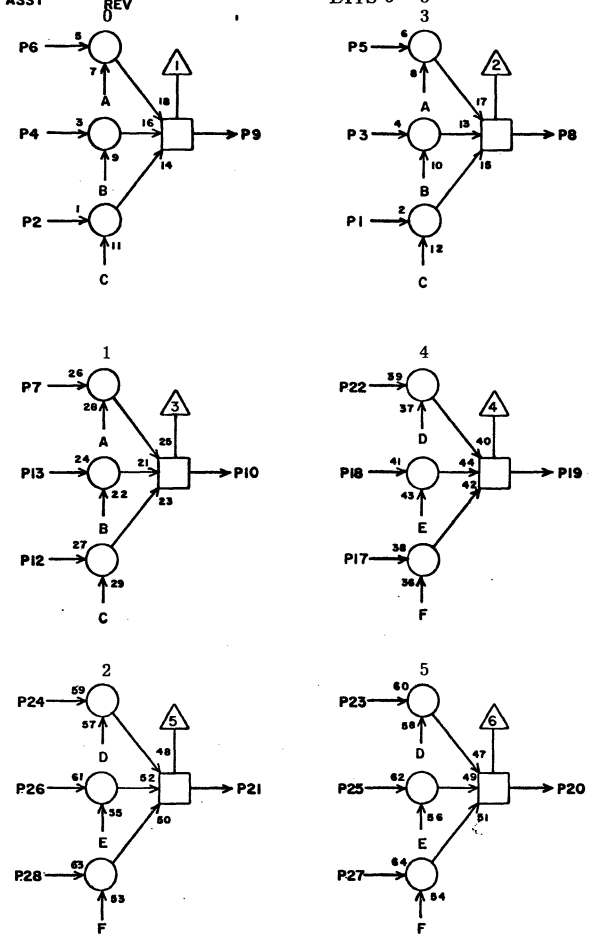
60136305

Rev A

LS 63063700 ASSY | REV

GATES IN FROM DATA CHANNEL TE
BITS 0 - 5

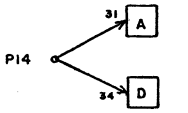
I07



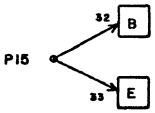
1			
2			
3	L12	24	15
4	L12	5	13
5	L07	24	13
6	L07	5	13
7	L07	11	13
8	H10	18	7
9	H10	13	7
10	H10	14	7
11			
12			
13	L12	11	13
14	J10	2	7
15	J10	22	9
16	I07	X	2
17			
18	L13	5	13
19	H11	13	7
20	H11	14	7
21	H10	17	7
22	L08	5	11
23	L08	11	11
24	L07	18	11
25	L13	11	13
26	L12	18	13
27			
28			

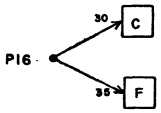
JACK PIN LG

A CONN



B CONN





CIRCUIT SPECIFICATION 11827600
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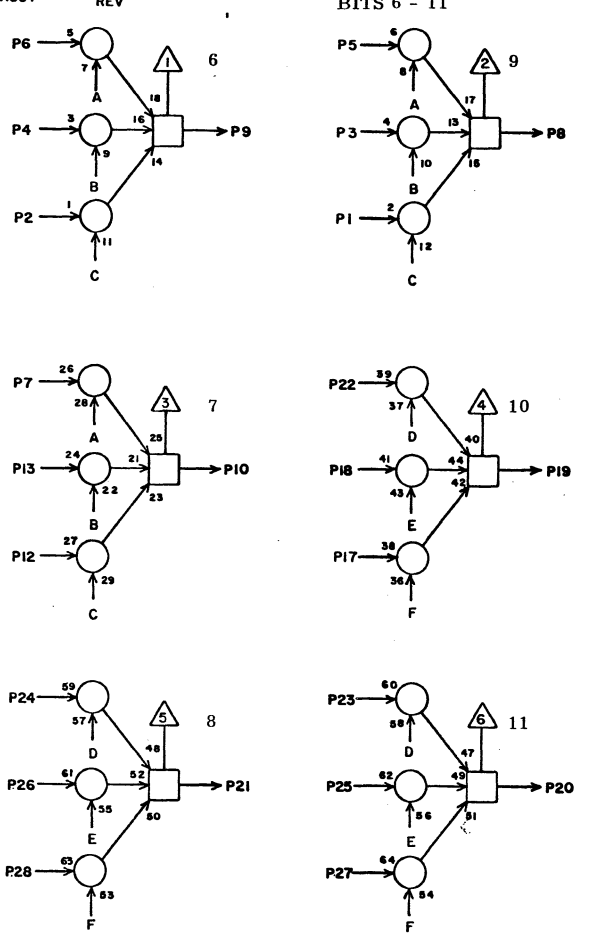
LS 63063700 ASSY | REV

GATES IN FROM DATA CHANNEL TE
BITS 6 - 11

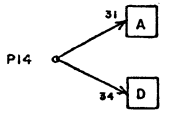
I08



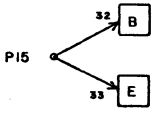
1			
2			
3	L14	9	13
4	L13	20	15
5	L09	9	13
6	L08	20	13
7	L08	22	13
8	H12	14	7
9	J08	3	5
10	J08	25	7
11			
12			
13	L13	22	13
14	J10	12	7
15	J10	21	7
16	I08	X	2
17			
18	L14	20	13
19	H12	17	7
20	H12	18	7
21	J08	6	5
22	L09	20	13
23	L09	22	13
24	L09	7	11
25	L14	22	13
26	L14	7	13
27			
28			

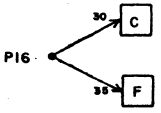
JACK PIN LG

A CONN



B CONN





CIRCUIT SPECIFICATION 11827600
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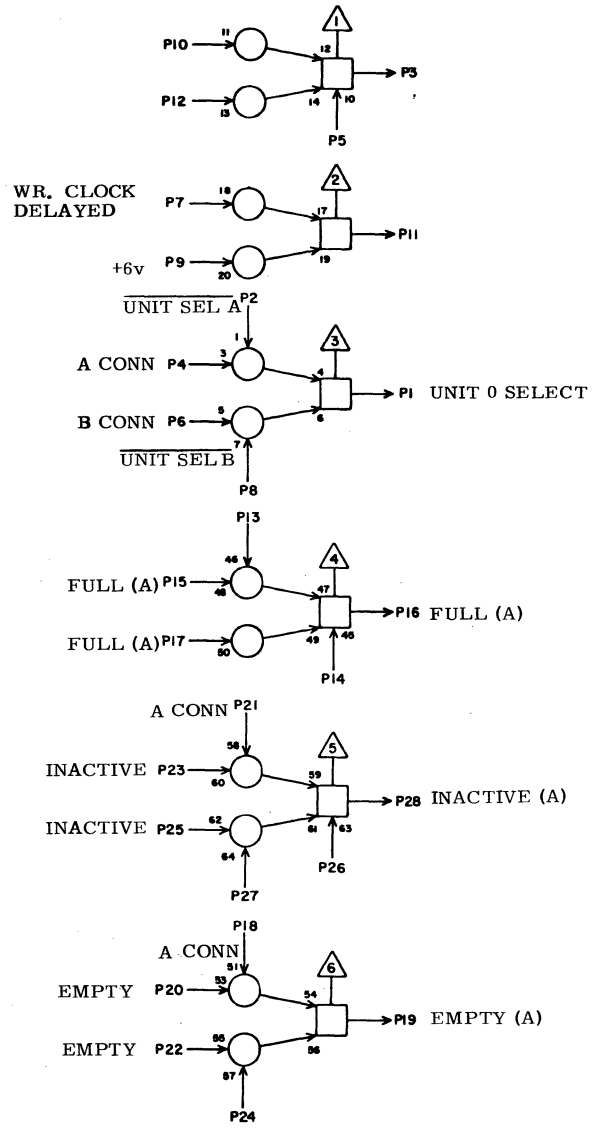
Rev A

LS 63060700 ASSY | C REV | QN | I09



	JACK	PIN	LG
1	D10	6	17
2	H16	4	11
3			
4	J10	16	7
5			
6	J10	23	7
7	F01	10	120
8	H16	15	11
9	C16	15	23
10			
11	F07	8	13
12			
13	I09	X	2
14	H15	6	9
15	J08	14	5
16	K13	4	9
17	K13	15	11
18	J10	24	7
19	K13	27	13
20	G08	20	9
21	J10	20	5
22	K13	16	11
23	F11	22	13
24	I09	X	2
25	K13	17	9
26	K06	9	9
27	I09	X	2
28	K13	6	9

CIRCUIT SPECIFICATION 11827600
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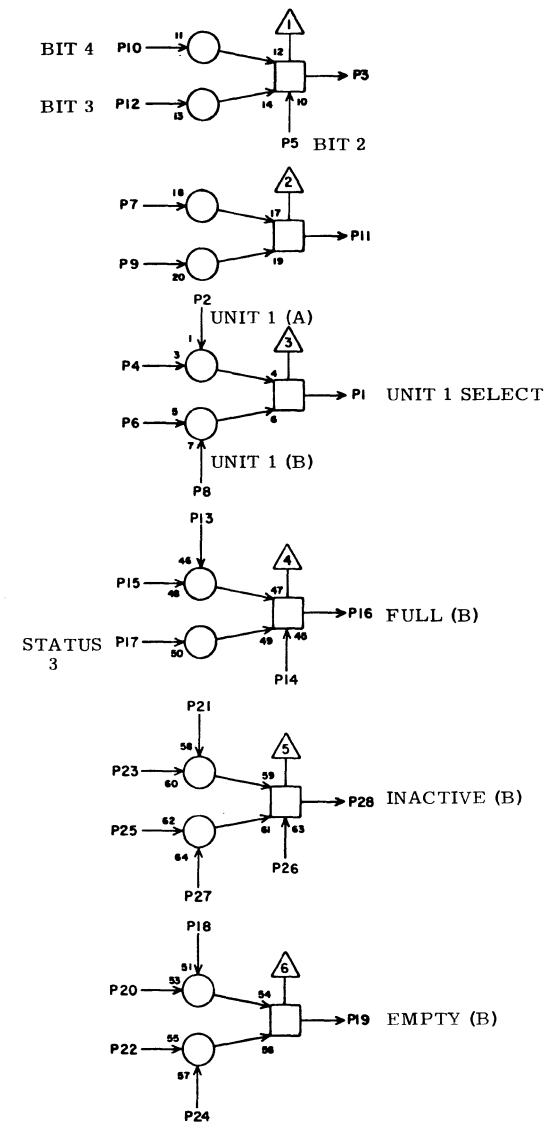
LS 63060700 ASSY | C REV | QN | I10



	JACK	PIN	LG
1	D10	7	17
2	H16	1	9
3	K10	21	11
4	J10	7	7
5	H10	19	5
6	J10	19	7
7			
8	H16	19	9
9			
10	H11	6	7
11			
12	F07	10	13
13	I10	X	2
14	H15	10	9
15	K16	15	11
16	K16	4	11
17	J08	15	7
18	J10	27	7
19	K16	27	11
20	G08	22	9
21	J10	17	5
22	K16	16	11
23	F11	24	13
24	I10	X	2
25	K16	17	11
26	K07	9	9
27	I10	X	2
28	K16	6	11

CIRCUIT SPECIFICATION 11827600
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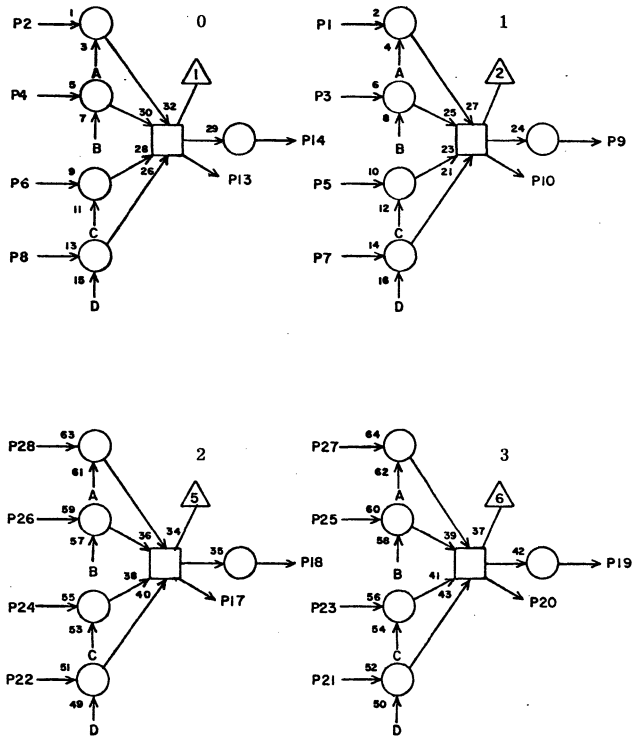
Rev A

LS 63063900 ASSY | E REV

INTERFACE A BITS 0-3

TG

I11



1	K11	17	9
2	K11	19	9
3	B09	9	25
4	B09	8	25
5	J03	10	11
6	J03	3	11
7	D05	2	19
8	D05	1	19
9			
10	K11	6	9
11	H15	4	7
12	C15	2	21
13	K11	11	9
14			
15	H15	24	7
16	H15	28	7
17	K11	4	7
18			
19			
20	K11	27	9
21	D05	19	19
22	D05	14	19
23	J03	23	11
24	J03	24	11
25	B09	19	25
26	B09	12	25
27	K11	16	9
28	K11	15	9

JACK PIN LG

+6V

PI2 → 31 A — PASSBACK

PI6 → 33 B — STATUS A

PI1 → 22 C — DATA A

PI5 → 44 D — POSITION A

CIRCUIT SPECIFICATION 11827600

60196300

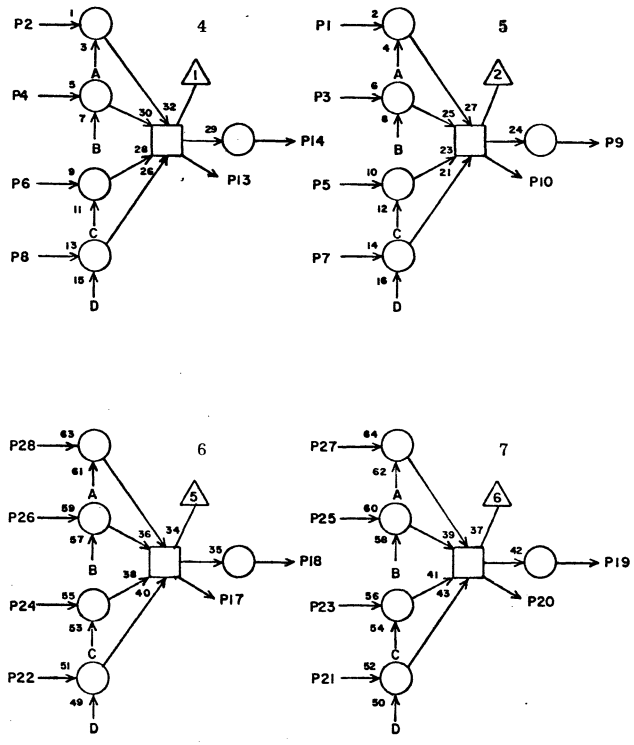
Rev A

LS 63063900 ASSY | F REV

INTERFACE BITS 4-7

TG

I12



1	K11	12	9
2	K11	14	9
3	B09	21	23
4	B09	18	25
5	J04	10	11
6	J04	3	11
7	D05	28	19
8	D05	27	19
9			
10	K11	20	9
11	H15	3	7
12	C15	4	21
13	K11	25	9
14			
15	H15	21	7
16	H15	25	7
17	K12	11	9
18			
19			
20	K12	6	9
21	C06	2	23
22	C06	1	23
23	J04	23	11
24	J04	24	11
25	F09	5	13
26	B07	18	25
27	K12	17	9
28	K12	19	9

JACK PIN LG

+6V

PI2 → 31 A — PASS BACK

PI6 → 33 B — STATUS A

PI1 → 22 C — DATA A

PI5 → 44 D — POSITION A

CIRCUIT SPECIFICATION 11827600

60196300

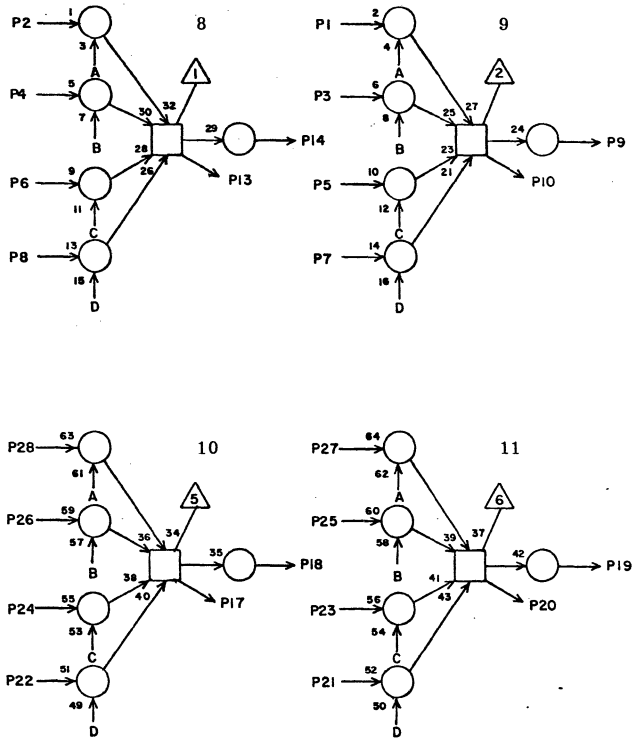
Rev A

LS 63063900 ASSY | E REV

INTERFACE A
BITS 8-11

TG

I13



+ 6V

P12 → 31 A PASS BACK

P16 → 33 B STATUS A

P11 → 22 C DATA A

P15 → 44 D POSITION A

	JACK	PIN	LG
1	K12	16	9
2	K12	15	9
3	F04	9	17
4	D08	2	19
5	J05	10	11
6	J05	3	11
7	C06	19	21
8	C06	14	23
9			
10	K12	27	9
11	H15	5	7
12	C15	15	21
13	K12	4	9
14			
15	H15	22	5
16	H15	26	5
17	K12	25	9
18			
19			
20	K12	20	9
21	C06	28	21
22	C06	27	21
23	J05	23	11
24	J05	24	11
25	H05	25	11
26	E10	19	15
27	K12	12	9
28	K12	14	9

CIRCUIT SPECIFICATION 11827600

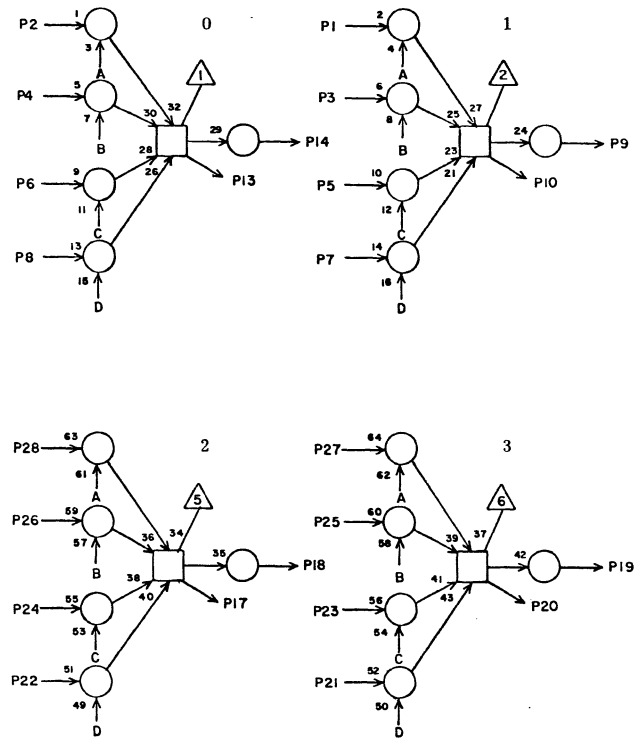
60196300
Rev A

LS 63063900 ASSY | E REV

INTERFACE B
BITS 0-3

TG

I14



+6v

P12 → 31 A PASS BACK

P16 → 33 B STATUS B

P11 → 22 C DATA B

P15 → 44 D POSITION B

	JACK	PIN	LG
1	K14	17	9
2	K14	19	9
3	B09	11	23
4	B09	7	23
5	J03	9	15
6	J03	4	15
7	D05	6	21
8	D05	3	21
9			
10	K14	6	9
11	H15	8	5
12	C15	17	21
13	K14	11	9
14			
15	J02	2	15
16	J02	14	15
17	K14	4	7
18			
19			
20	K14	27	9
21	D05	17	21
22	D05	10	19
23	J03	22	15
24	J03	25	15
25	B09	17	25
26	B09	10	25
27	K14	16	9
28	K14	15	9

CIRCUIT SPECIFICATION 11827600

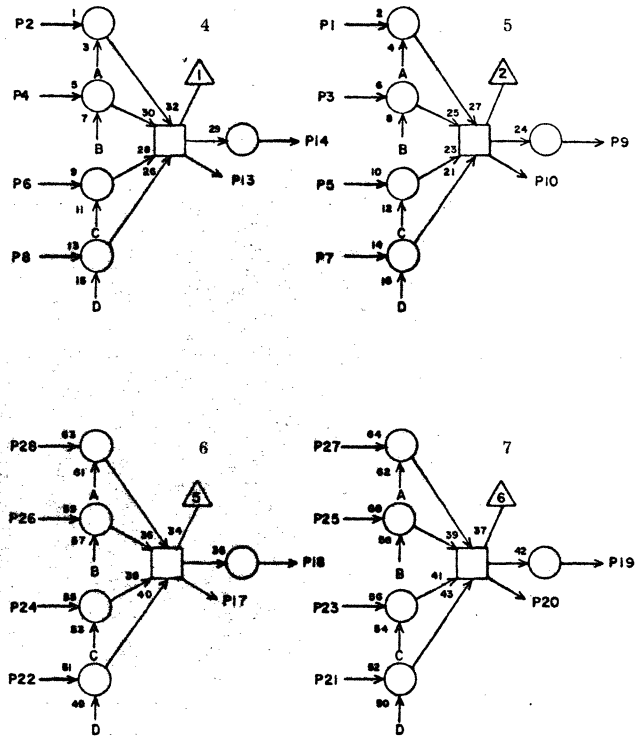
60196300
Rev A

LS 63063900 ASSY | E REV

INTERFACE B BITS 4-7

TG

I15



1	K14	12	9
2	K14	14	9
3	B09	15	23
4	B09	20	23
5	J04	9	15
6	J04	4	15
7	D05	26	19
8	D05	18	21
9			
10	K14	20	9
11	H15	7	5
12	C16	2	21
13	K14	25	9
14			
15	J02	12	17
16	J02	8	17
17	K15	11	9
18			
19			
20	K15	6	7
21	C06	6	25
22	C06	3	25
23	J04	22	15
24	J04	25	15
25	F09	9	15
26	B07	20	25
27	K15	17	9
28	K15	19	9

JACK PIN LG

+6v P12 → 31 A — PASS BACK

P16 → 33 B — STATUS B

P11 → 22 C — DATA B

P15 → 44 D — POSITION B

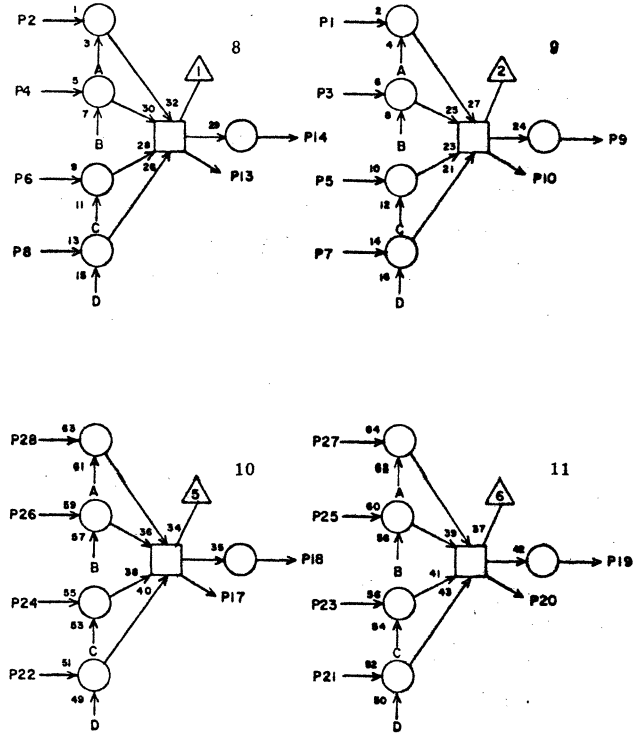
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63063900 ASSY | F REV

INTERFACE B BITS 8-11

TG

I16



1	K15	16	9
2	K15	15	9
3	F04	11	17
4	D08	4	21
5	J05	9	15
6	J05	4	15
7	C06	17	25
8	C06	10	25
9			
10	K15	27	9
11	H15	9	5
12	C16	4	21
13	K15	4	9
14			
15	J02	10	17
16	J02	7	17
17	K15	25	9
18			
19			
20	K15	20	9
21	C06	26	25
22	C06	18	25
23	J05	22	15
24	J05	25	15
25	H05	27	13
26	E10	5	17
27	K15	12	9
28	K15	14	9

JACK PIN LG

+6v P12 → 31 A — PASS BACK

P16 → 33 B — STATUS B

P11 → 22 C — DATA B

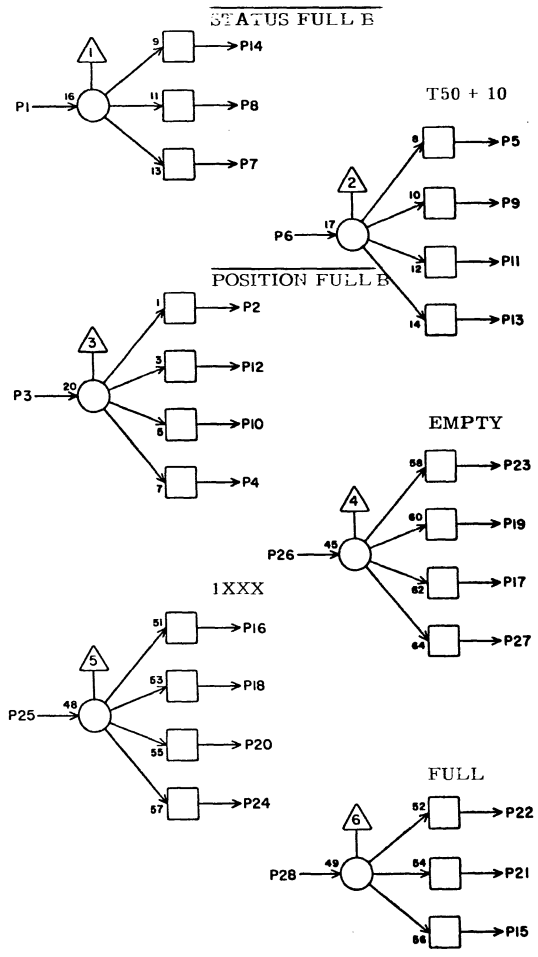
P15 → 44 D — POSITION B

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63064000 ASSY | REV

TH

J02



1	H04	11	9
2	I14	15	15
3	H04	16	9
4			
5	K09	3	13
6	J09	19	13
7	I16	16	17
8	I15	16	17
9	K09	23	13
10	I16	15	17
11	E11	7	25
12	I15	15	17
13	D10	23	25
14	I14	16	15
15	I05	7	7
16	K09	1	13
17			
18	K09	21	11
19	I05	9	7
20	D10	21	25
21	G04	2	13
22	H13	4	17
23	F08	17	19
24			
25	K08	24	13
26	I06	19	9
27			
28	I06	9	9
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600

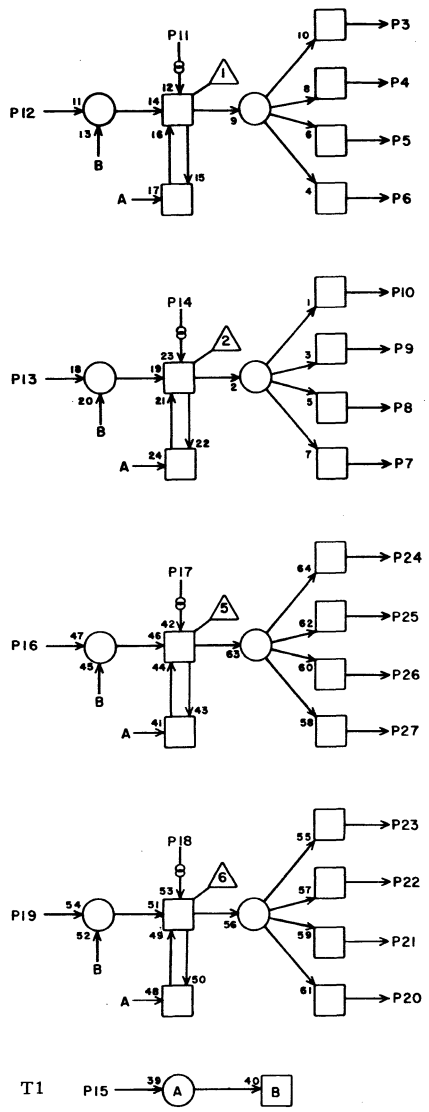
60196300
Rev A

LS 63062700 ASSY

D REV

READ DATA REGISTER BITS 0-3

SB



J03

1			
2			
3	I11	6	11
4	I14	6	15
5	F13	4	19
6	E14	17	21
7	E14	19	21
8	F13	3	19
9	I14	5	15
10	I11	5	11
11	J03	X	2
12	L01	10	9
13	L01	12	9
14	J03	X	2
15	E07	16	19
16	L01	22	9
17	J03	X	2
18	J03	X	2
19	L02	10	7
20	E14	23	21
21	F13	18	19
22	I14	23	15
23	I11	23	11
24	I11	24	11
25	I14	24	15
26	F13	13	19
27	E14	21	21
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

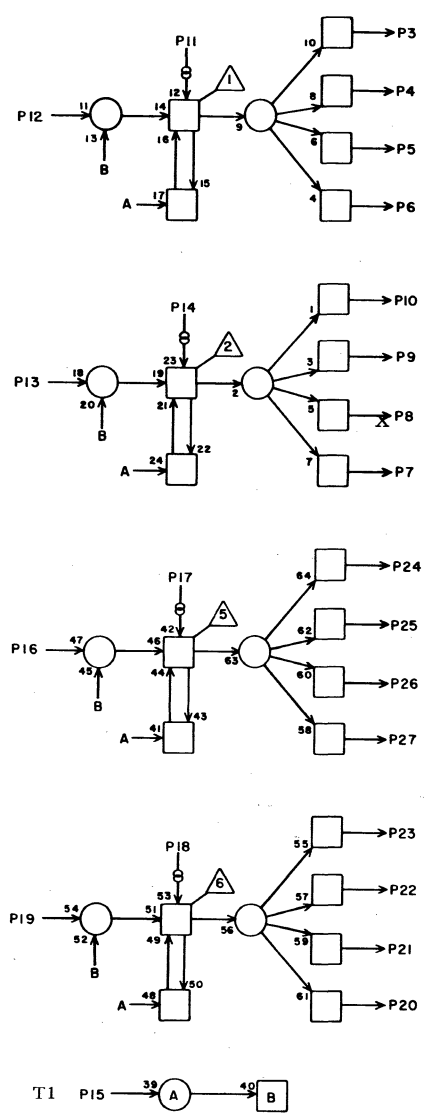
Rev A

LS 63062700 ASSY

D REV

READ DATA REGISTER BITS 4-7

SB



J04

1			
2			
3	I12	6	11
4	I15	6	15
5	F13	26	17
6	E14	25	19
7	E14	27	19
8	F13	25	17
9	I15	5	15
10	I12	5	11
11	J04	X	2
12	L02	12	9
13	L02	22	9
14	J04	X	2
15	E07	18	19
16	L03	10	9
17	J04	X	2
18	J04	X	2
19	L03	12	7
20	E14	18	21
21	F14	3	19
22	I15	23	15
23	I12	23	11
24	I12	24	11
25	I15	24	15
26	F14	4	19
27	E14	16	21
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300

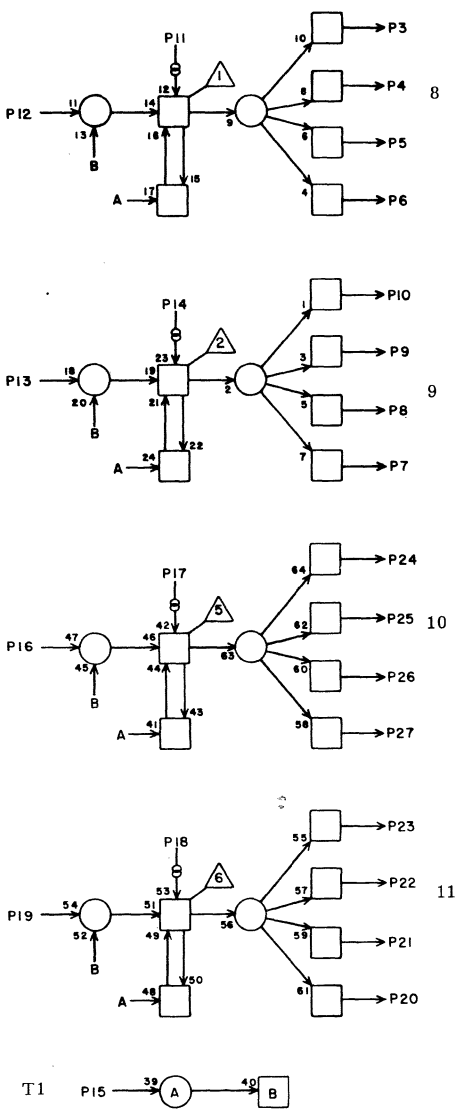
Rev A

LS 63062700
ASSY

D
REV

READ DATA REGISTER BITS 8-11

SB



J05

1			
2			
3	I13	6	11
4	I16	6	15
5	F14	13	17
6	E14	20	19
7	E14	22	19
8	F14	18	17
9	I16	5	15
10	I13	5	11
11	J05	X	2
12	L03	22	9
13	L04	10	9
14	J05	X	2
15	E07	20	19
16	L04	12	9
17	J05	X	2
18	J05	X	2
19	L04	22	9
20	E14	26	21
21	F14	25	17
22	I16	23	15
23	I13	23	11
24	I13	24	11
25	I16	24	15
26	F14	26	17
27	E14	24	21
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

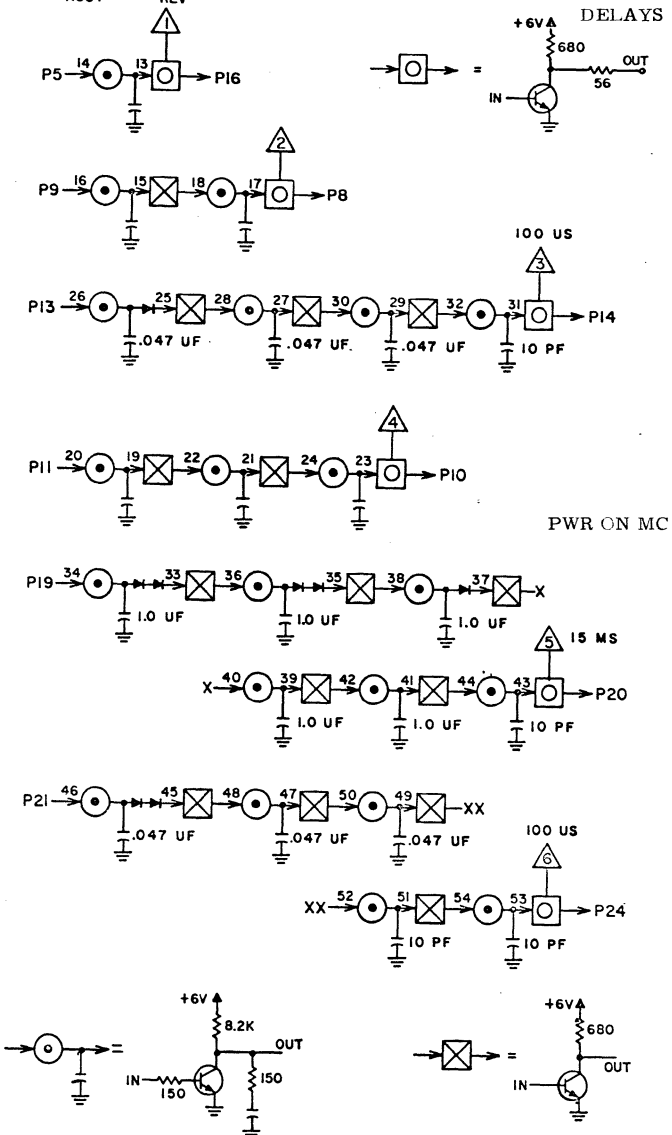
60196300
Rev A

LS 63065532
ASSY

F
REV

XL10

DELAYS



J06

1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13	K04	2	5
14	K04	14	7
15			
16			
17			
18			
19	J06	X	2
20	K08	26	7
21	K04	26	7
22			
23			
24	K04	24	7
25			
26			
27			
28			

JACK PIN LG

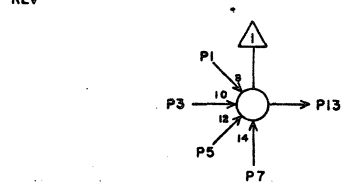
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

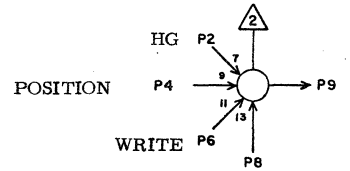
LS 63064100 ASSY (C) REV

TI

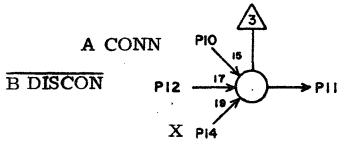
J07

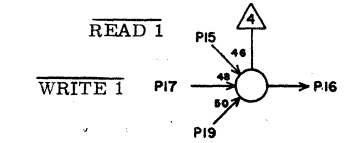


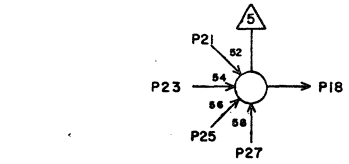
INACTIVE



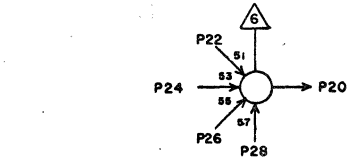
GATE ZS







INACTIVE POSITION SELECT



INACTIVE HEAD GROUP SELECT

1	J07	20	5
2	G05	6	13
3	J07	18	5
4	G05	5	13
5	F07	18	15
6	F01	13	17
7	E09	18	17
8	J07	X	2
9	E02	22	17
10	K05	16	7
11	K07	2	5
12	K04	20	7
13	F08	10	15
14	J07	X	2
15	G07	1	13
16	K10	27	9
17	G07	9	13
18	J07	3	5
19	J07	X	2
20	J07	1	5
21	G06	11	13
22	G06	12	13
23	E02	4	21
24	F06	4	17
25	J07	X	2
26	J07	X	2
27	J07	X	2
28	J07	X	2
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600

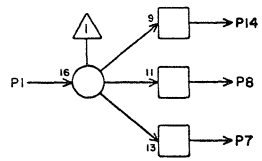
60196300
Rev A

LS 63064000 ASSY ( ) REV

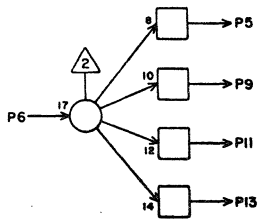
TH

J08

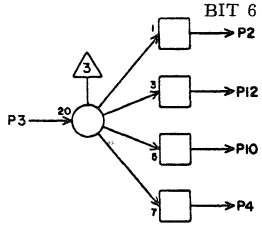
STATUS FULL (A)



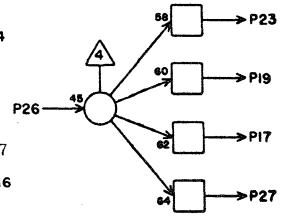
BIT 8



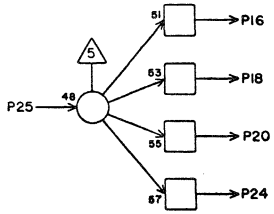
BIT 6



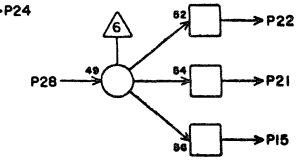
HG + 30 us



BIT 7



STATUS FULL (B)



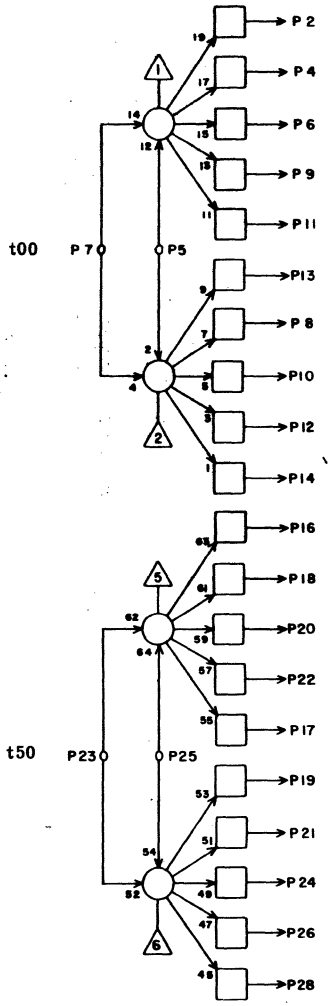
1	K06	25	9
2			
3	I08	9	5
4			
5	H14	26	11
6	I08	21	5
7			
8	H15	15	13
9	H12	13	9
10	H11	17	9
11			
12	H14	6	13
13			
14	I09	15	5
15	I10	17	7
16	H14	8	13
17			
18	H11	18	9
19	L05	18	11
20			
21	H04	12	11
22	H04	17	9
23	L05	25	11
24	(C)		
25	I08	10	7
26	D07	27	21
27			
28	K07	25	5
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63044800 ASSY [B] REV

HC



J09

1			
2	G12	11	13
3			
4	F12	16	15
5	J09	X	2
6	F03	16	15
7	I05	19	7
8			
9	G01	13	15
10			
11	G01	27	120
12			
13			
14			
15			
16	G07	16	11
17	G12	5	13
18	H10	15	9
19	J02	6	13
20	H11	15	9
21	G12	23	13
22	H12	15	9
23	I05	1	9
24	H05	13	13
25	J09	X	2
26	F02	16	17
27			
28	F11	16	17

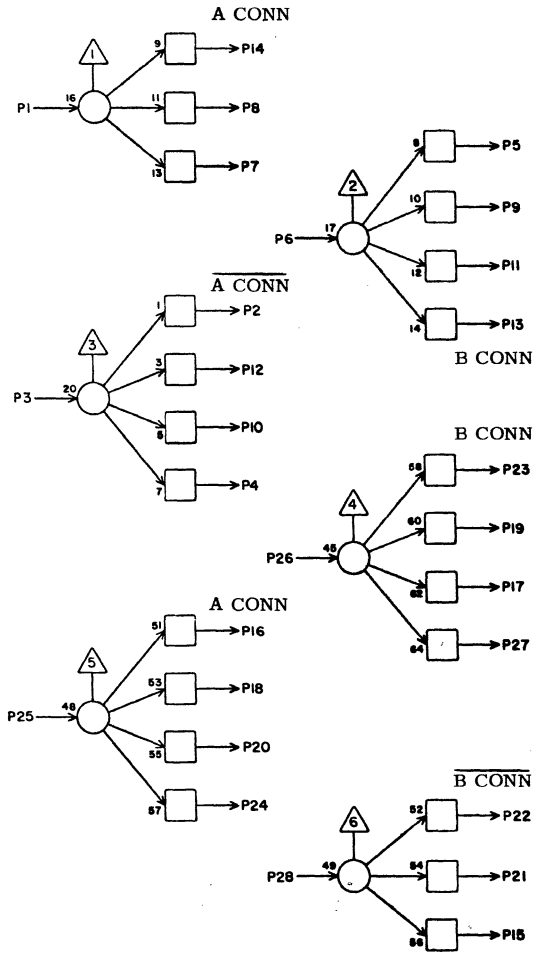
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63064000 ASSY [ ] REV

TH



J10

1	K05	22	11
2	I07	14	7
3	K05	27	11
4	E10	26	17
5	I05	8	9
6	K05	17	9
7	I10	4	7
8			
9	I05	24	9
10	I06	14	7
11	H15	16	11
12	I08	14	7
13			
14			
15	I06	15	9
16	I09	4	7
17	I10	21	5
18	H15	2	11
19	I10	6	7
20	I09	21	5
21	I08	15	7
22	I07	15	9
23	I09	6	7
24	I09	18	7
25	K05	24	9
26	K05	19	9
27	I10	18	7
28	K05	15	9

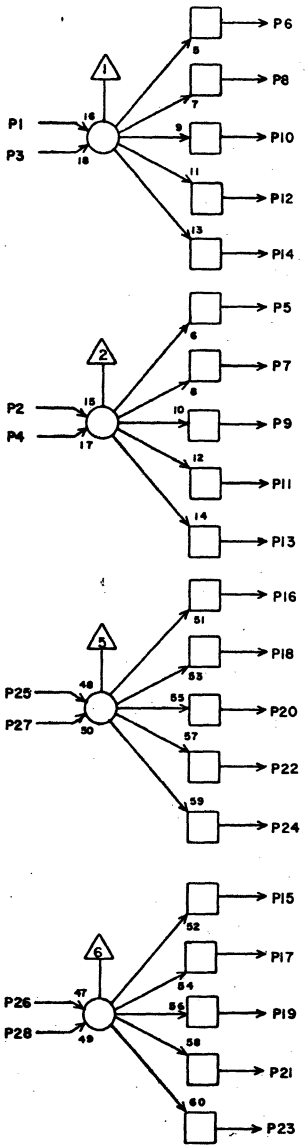
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63063600 ASSY C REV

TD J11



t25(A)

t50(A)

t50(A)

t00(A)

	JACK	PIN	LG
1	J13	2	5
2	J13	1	5
3	J11	X	2
4	J11	X	2
5	K06	16	9
6	K11	18	41
7	K04	8	11
8	K12	18	41
9	L07	12	11
10			
11	L08	12	9
12			
13	L09	12	9
14			
15	K04	7	11
16	L10	12	9
17			
18	L11	12	9
19			
20	H16	9	7
21			
22			
23			
24			
25	J13	3	5
26	J13	21	5
27	J11	X	2
28	J11	X	2

CIRCUIT SPECIFICATION 11827600

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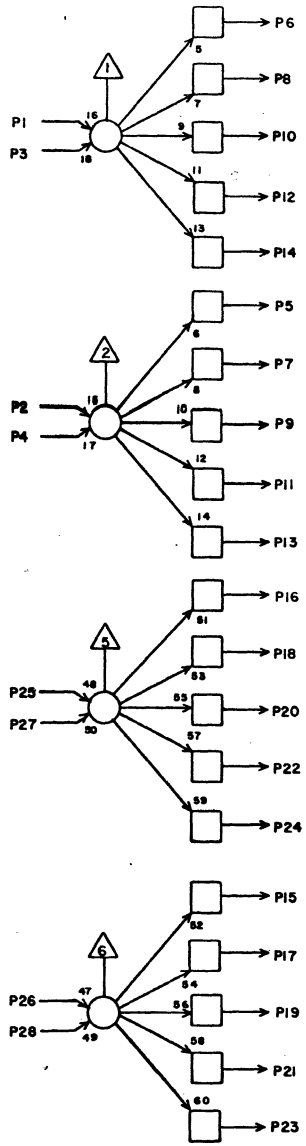
Rev A

LS 63063600 ASSY C REV

CHANNEL A CLOCK
STROBE NETWORK

TD J12



	JACK	PIN	LG
1	J13	14	59
2	J12	10	109
3	J12	X	2
4	J12	X	2
5	J13	16	17
6	J13	11	55
7	J13	18	55
8	J13	19	17
9	J12	25	109
10	J12	2	109
11			
12	J13	10	3
13			
14			
15	J13	15	17
16	J13	13	17
17	J13	20	55
18	J13	17	55
19			
20	J12	26	109
21			
22			
23			
24			
25	J12	9	109
26	J12	20	109
27	J12	X	2
28	J12	X	2

CIRCUIT SPECIFICATION 11827600

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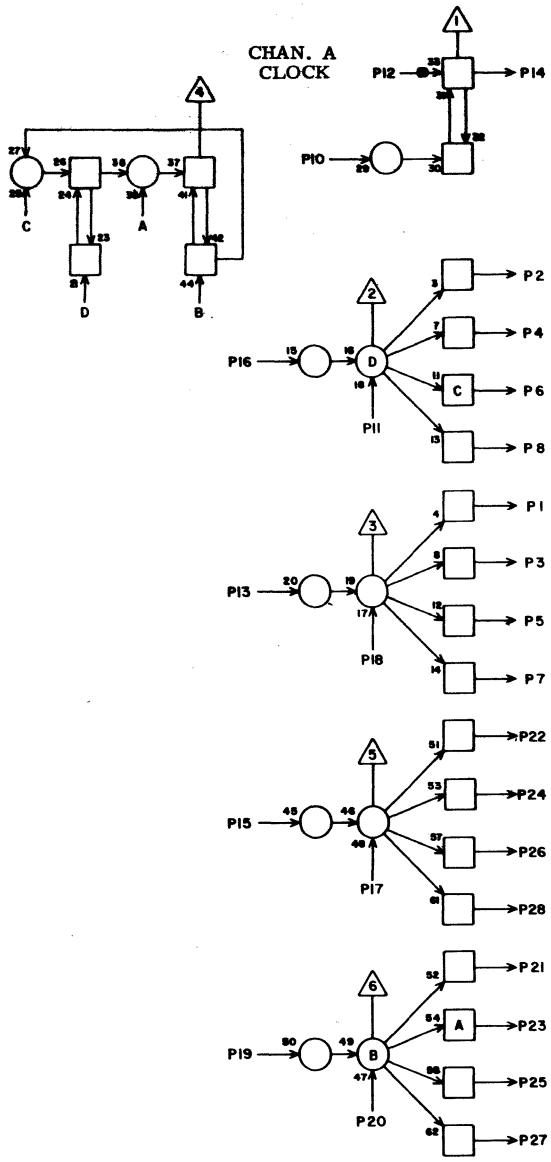
LS 63046200 ASSY D REV

HQ

J13



1	J11	2	5
2	J11	1	5
3	J11	25	5
4	K13	18	7
5	I05	2	11
6			
7			
8			
9			
10	J12	12	3
11	J12	6	55
12			
13	J12	16	17
14	J12	1	59
15	J12	15	17
16	J12	5	17
17	J12	18	55
18	J12	7	55
19	J12	8	17
20	J12	17	55
21	J11	26	5
22			
23	I05	18	13
24			
25			
26			
27			
28			

25 50 75 100

JACK PIN LG

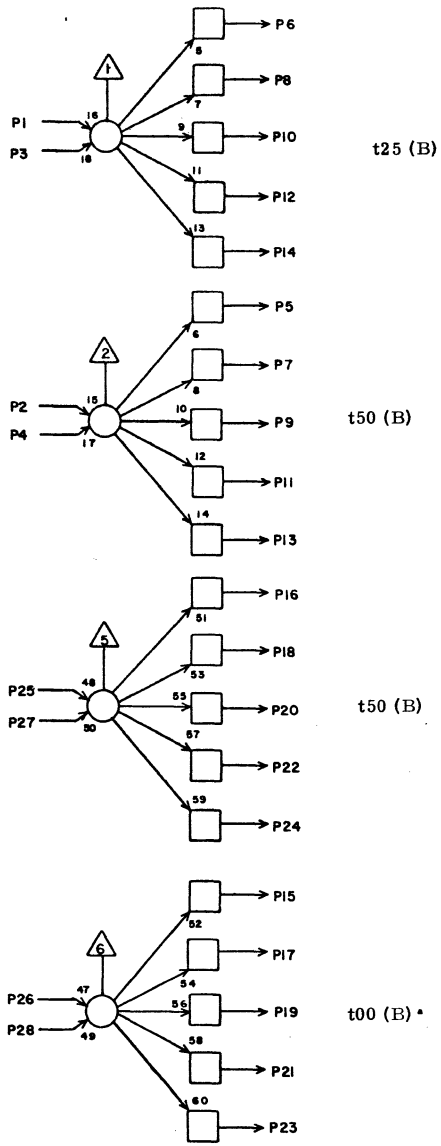
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63063600 ASSY C REV

TD

J14



1	J16	2	5
2	J16	1	5
3	J14	X	2
4	J14	X	2
5	K07	16	11
6	K14	18	41
7	K04	18	13
8	K15	18	41
9	L12	12	9
10			
11	L13	12	9
12			
13	L14	12	9
14			
15	K04	17	15
16	L15	12	9
17			
18	L16	12	9
19			
20	H16	20	9
21			
22			
23			
24			
25	J16	3	5
26	J16	21	5
27	J14	X	2
28	J14	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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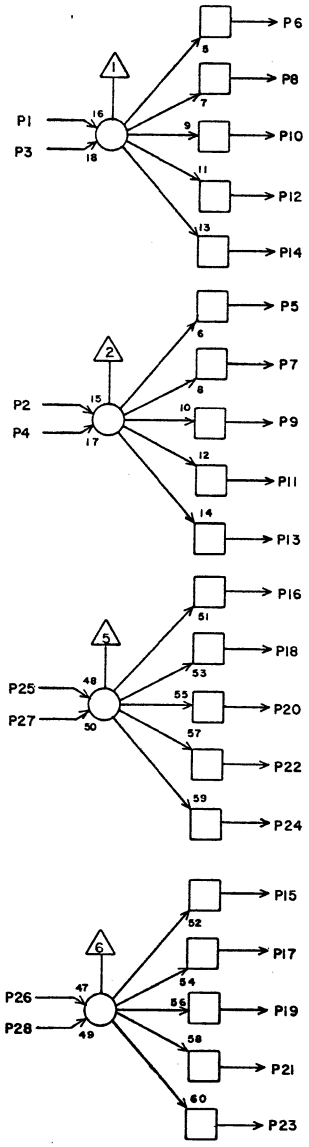
LS 63063600 ASSY [ ] REV

CHANNEL B CLOCK STROBE NETWORK



TD [J15]

1	J16	14	59
2	J15	10	109
3	J15	X	2
4	J16	X	2
5	J16	16	17
6	J16	11	55
7	J16	18	55
8	J16	19	17
9	J15	25	109
10	J15	2	109
11			
12	J16	10	3
13			
14			
15	J16	15	17
16	J16	13	17
17	J16	20	55
18	J16	17	55
19			
20	J15	26	109
21			
22			
23			
24			
25	J15	9	109
26	J15	20	109
27	J15	X	2
28	J15	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
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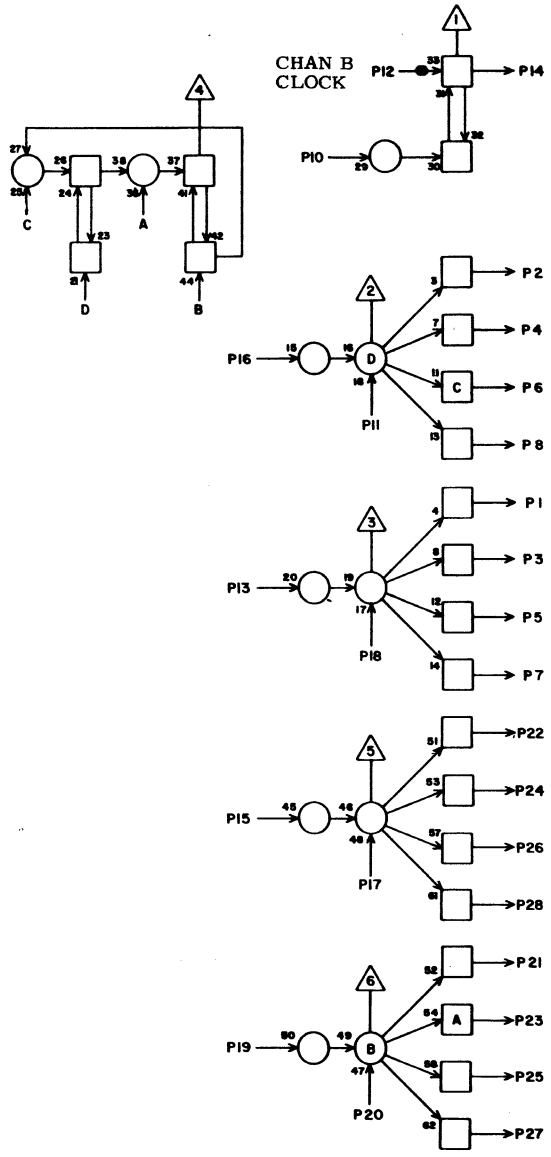
LS 63046200 ASSY [D] REV



HQ [J16]

1	J14	2	5
2	J14	1	5
3	J14	25	5
4	K16	18	7
5	I05	6	15
6			
7			
8			
9			
10	J15	12	3
11	J15	6	55
12			
13	J15	16	17
14	J15	1	59
15	J15	15	17
16	J15	5	17
17	J15	18	55
18	J15	7	55
19	J15	8	17
20	J15	17	55
21	J14	26	5
22			
23	I05	22	15
24			
25			
26			
27			
28			

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
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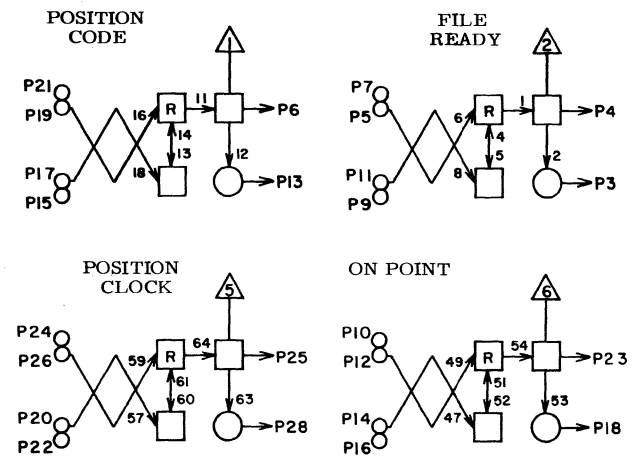
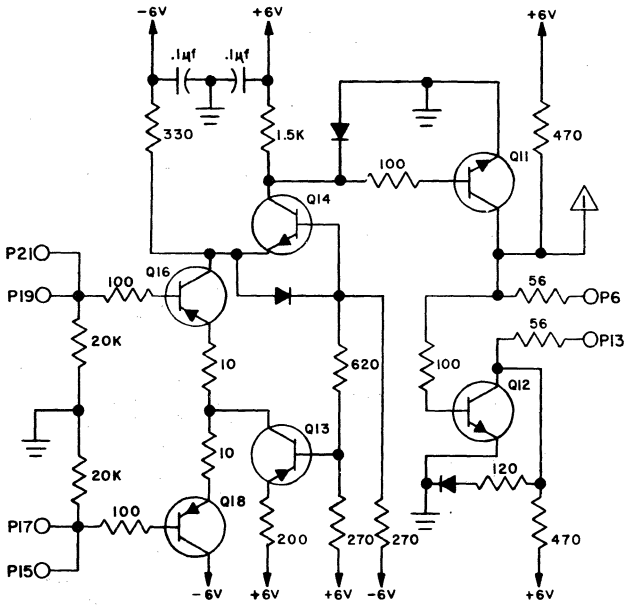
LSI7876300 ASSY | A REV | ZR





K01

1	-6V		2
2			
3			
4	D03	10	23
5	J-2	F3	9
6	E01	6	21
7	J-1	F3	9
8			
9	J-2	F4	9
10	J-1	C9	9
11	J-1	F4	9
12	J-2	C9	8
13	E01	26	19
14	J-1	C10	9
15	J-2	D2	8
16	J-2	C10	8
17	J-1	D2	12
18			
19	J-2	D1	8
20	J-1	D4	9
21	J-1	D1	9
22	J-2	D4	8
23	E01	28	21
24	J-1	D3	9
25	E01	1	23
26	J-2	D3	8
27			
28			

JACK PIN LG

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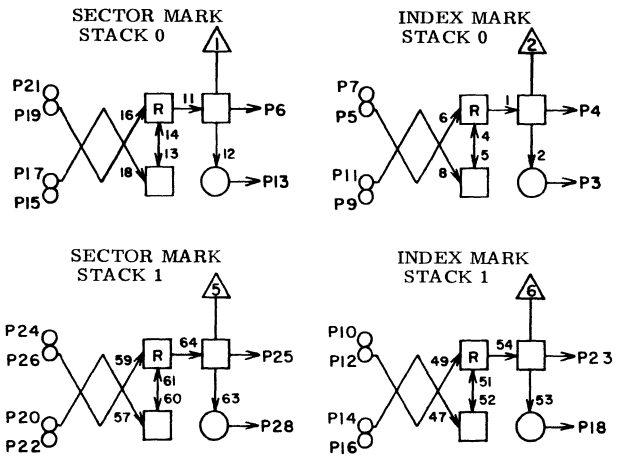
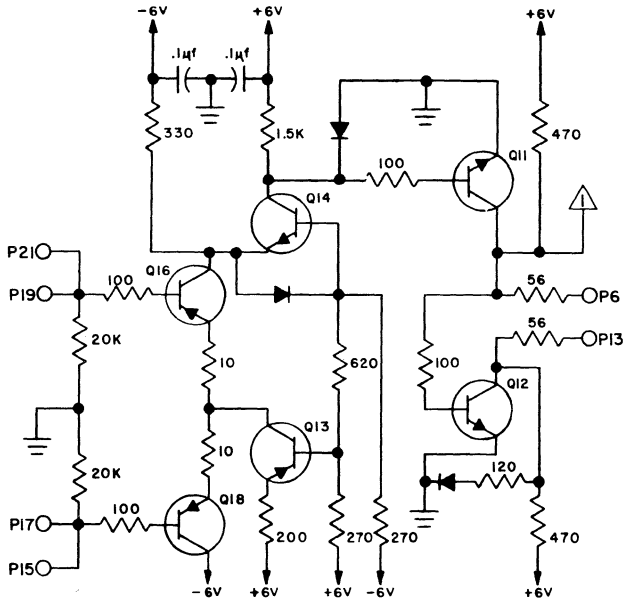
Rev A

LSI7876300 ASSY | A REV | ZR





K02

1	-6V		2
2			
3	D03	21	23
4	B01	7	29
5	J-2	E1	9
6	B07	6	31
7	J-1	E1	9
8			
9	J-2	E2	9
10	J-1	E7	9
11	J-1	E2	9
12	J-2	E7	8
13			
14	J-1	E8	9
15	J-2	E4	8
16	J-2	E8	8
17	J-1	E4	9
18	D03	24	23
19	J-2	E3	8
20	J-1	E10	9
21	J-1	E3	9
22	J-2	E10	8
23	A01	7	33
24	J-1	E9	9
25	B07	3	31
26	J-2	E9	8
27			
28			

JACK PIN LG

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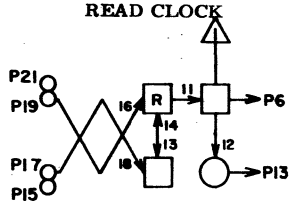
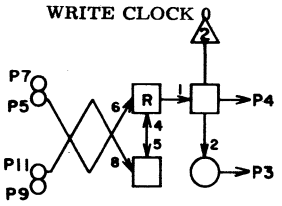
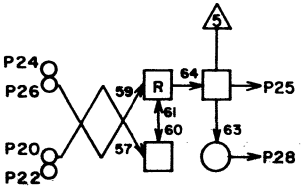
READ CLOCK

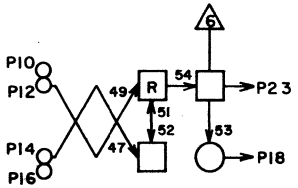


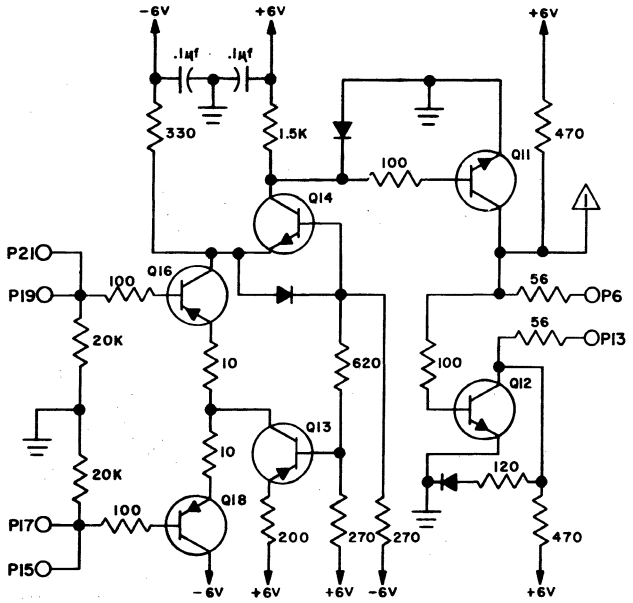
WRITE CLOCK



WRITE CLOCK I







	K03		
1	-6V		2
2			
3			
4	G01	20	13
5	J-2	E5	8
6	G01	4	15
7	J-1	E5	9
8			
9	J-2	E6	8
10			
11	J-1	E6	9
12			
13			
14			
15	J-2	D8	8
16			
17	J-1	D8	9
18			
19	J-2	D7	8
20	J-1	F2	8
21	J-1	D7	9
22	J-2	F2	7
23			
24	J-1	F1	8
25	G01	22	15
26	J-2	F1	7
27			
28			
	JACK	PIN	LG

60196300
Rev A

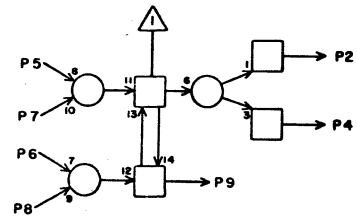
LS 63040000 ASSY | C REV | AA

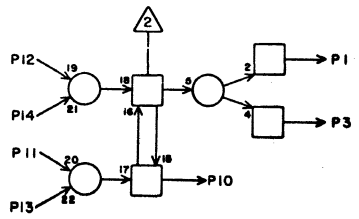
INACTIVE

A CONN

1XXX

+50





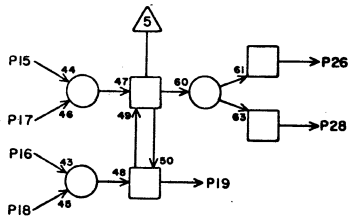
A DISCONNECT

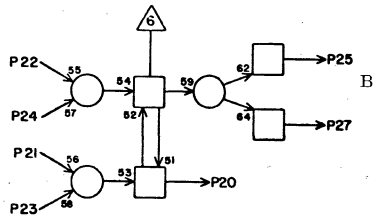
INACTIVE

B CONN

1XXX

+50





B DISCONNECT

	K04		
1	K06	4	5
2	J06	13	5
3			
4	K04	12	3
5	H16	14	19
6	K05	12	3
7	J11	15	11
8	J11	7	11
9	K04	11	3
10			
11	K04	9	3
12	K04	4	3
13	K04	X	2
14	J06	14	7
15	H16	28	19
16	K05	7	5
17	J14	15	15
18	J14	7	13
19	K04	21	3
20	J07	12	7
21	K04	19	3
22	K04	28	3
23	K04	X	2
24	J06	24	7
25			
26	J06	21	7
27			
28	K04	22	3
	JACK	PIN	LG

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LS 63042900 B
ASSY REV

CX

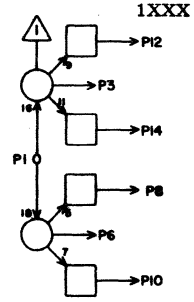
K05

1	K09	13	7
2	K10	13	9
3	K06	2	3
4	K07	14	5
5	K07	4	5
6	K06	14	3
7	K04	16	5
8			
9			
10			
11			
12	K04	6	3
13			
14			
15	J10	28	9
16	J07	10	7
17	J10	6	9
18	K04	7	3
19	J10	26	9
20			
21	K04	17	3
22	J10	1	11
23	E09	25	23
24	J10	25	9
25	K06	8	3
26	K07	8	5
27	J10	3	11
28	I05	23	9
	JACK	PIN	LG

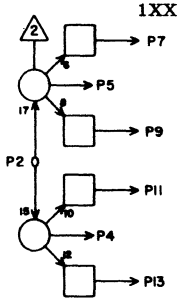
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

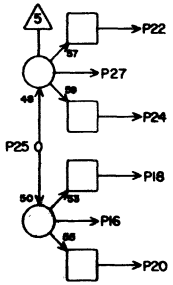
1XXX (A)



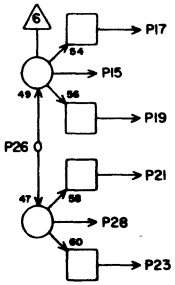
1XXX(B)



A CONN



B CONN

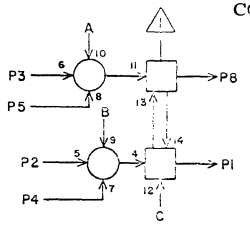


LS 63040400 C
ASSY REV

CONNECT A

B CONN
STATUS

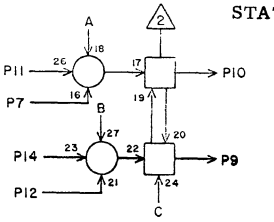
1XXX
DISCONNECT



STATUS 1

STATUS
X

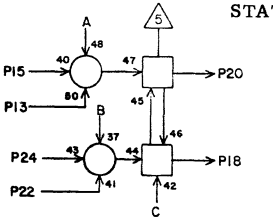
1XXX
X



STATUS 2

STATUS
X

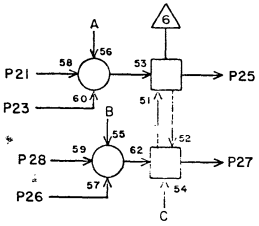
EMPTY
X



STATUS II
ACTIVE

ACTIVE
X

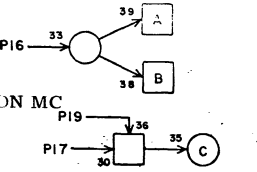
STATUS 3



t50 (A) P16

PWR ON MC

MC



K06

1	K07	3	3
2	K05	3	3
3	E10	9	120
4	K04	1	5
5	K08	6	5
6			
7	K06	X	2
8	K05	25	3
9	I09	26	9
10			
11	K08	8	5
12	K06	X	2
13	L08	8	7
14	K05	6	3
15	K08	10	5
16	J11	5	9
17	L11	8	7
18			
19	K08	17	5
20	K06	21	3
21	K06	20	3
22	K06	X	2
23	L10	5	7
24	L10	24	7
25	J08	1	9
26	K06	X	2
27			
28	L10	6	7
	JACK	PIN	LG

CIRCUIT SPECIFICATION 11827600

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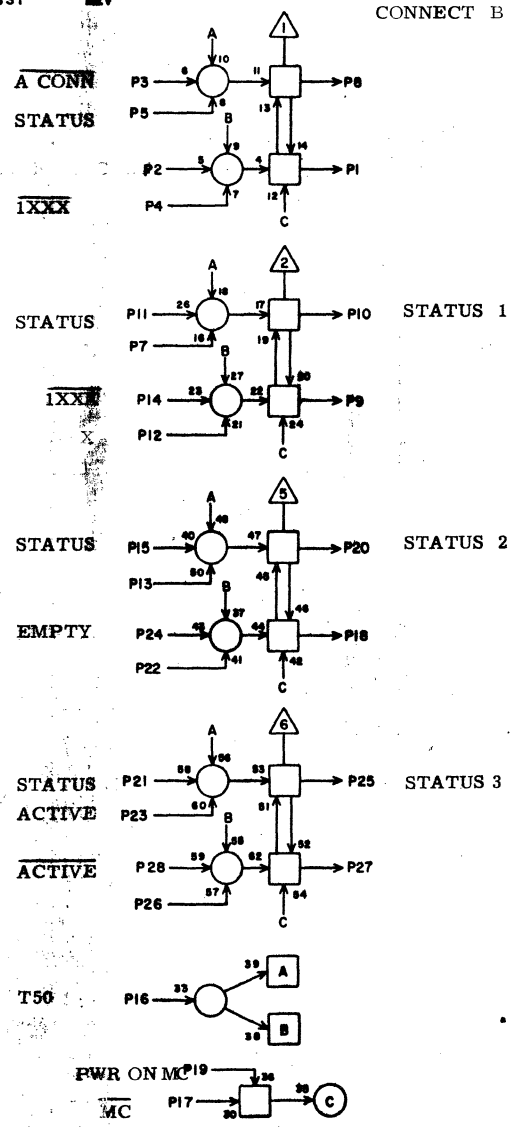
ASSY REV

AE

K07

CONNECT B



1	I05	4	11
2	J07	11	5
3	K06	1	3
4	K05	5	5
5	K08	5	3
6			
7	K07	X	2
8	K05	26	5
9	I10	26	9
10			
11	K08	7	3
12	K07	X	2
13	L13	8	9
14	K05	4	5
15	K08	9	3
16	J14	5	11
17	L16	8	11
18			
19	K08	19	3
20	K07	21	3
21	K07	20	3
22	K07	X	2
23	L15	5	11
24	L15	24	11
25	J08	28	5
26	K07	X	2
27			
28	L15	6	11

JACK PIN LG

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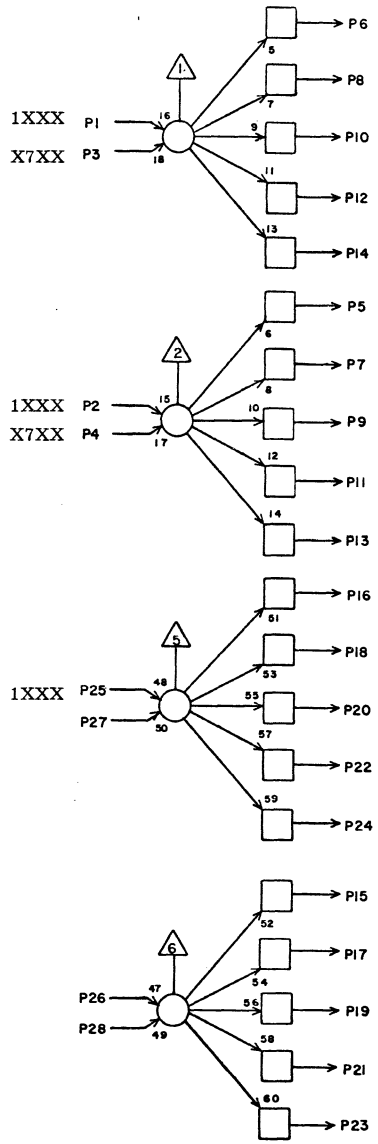
Rev A

LS 63063600
ASSY REV

TD

I08



STATUS A

STATUS B

1XXX

POWER ON MC

1	K09	12	3
2	K10	12	5
3	K09	20	3
4	K10	20	5
5	K07	5	3
6	K06	5	5
7	K07	11	3
8	K06	11	5
9	K07	15	3
10	K06	15	5
11	H16	22	15
12	H16	7	15
13			
14			
15	I05	26	11
16	G07	15	15
17	K06	19	5
18	G07	3	15
19	K07	19	3
20	G07	11	15
21			
22	G07	21	15
23			
24	J02	25	13
25	I06	10	11
26	J06	20	7
27	K08	X	2
28	K08	X	2

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

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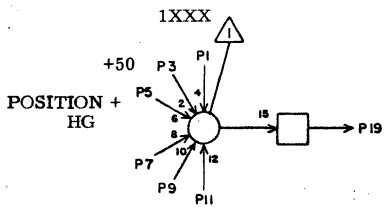
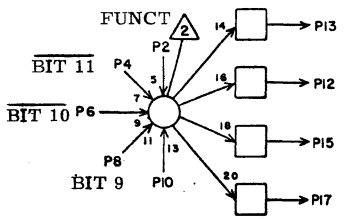
Rev A

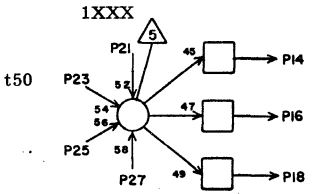
LS 63063400 ASSY REV

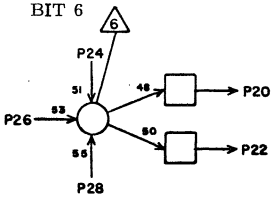
TB K09





1XXX (A)





X7XX (A)
+X5XX

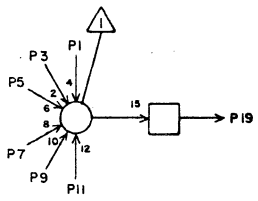
1	J02	16	13
2	L11	7	7
3	J02	5	13
4	L09	25	7
5	E09	9	21
6	L09	23	7
7	K09	X	2
8	L09	11	5
9	K09	X	2
10	K09	X	2
11	K09	X	2
12	K08	1	3
13	K05	1	7
14	H05	12	13
15	I06	7	11
16	H05	21	13
17	I06	23	9
18	D08	6	25
19	H05	5	13
20	K08	3	3
21	J02	18	11
22			
23	J02	9	13
24	L08	18	5
25	H04	18	15
26	K09	X	2
27	K09	X	2
28	L09	05	5

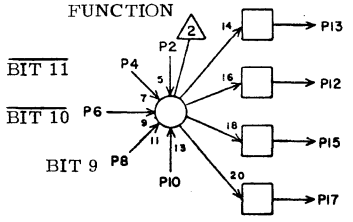
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63063400 ASSY REV

TB K10





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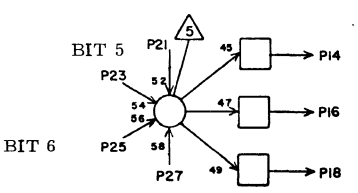
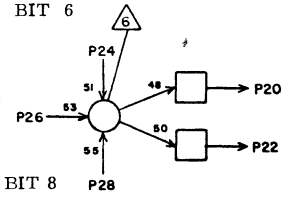


143_8 (Read 1 + Write 1)

Read 1 + Write 1



X7XX (B)

+ X5XX

1			
2	L16	7	9
3			
4	L14	25	9
5			
6	L14	23	9
7			
8	L14	11	7
9			
10	K10	X	2
11			
12	K08	2	5
13	K05	2	9
14	G01	25	17
15	I06	13	11
16	F08	12	21
17	I06	25	9
18			
19			
20	K08	4	5
21	I10	3	11
22			
23	F07	9	23
24	L13	18	7
25	H11	24	13
26	K10	X	2
27	J07	16	9
28	L14	5	7

JACK PIN LG

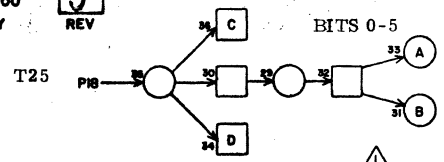
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

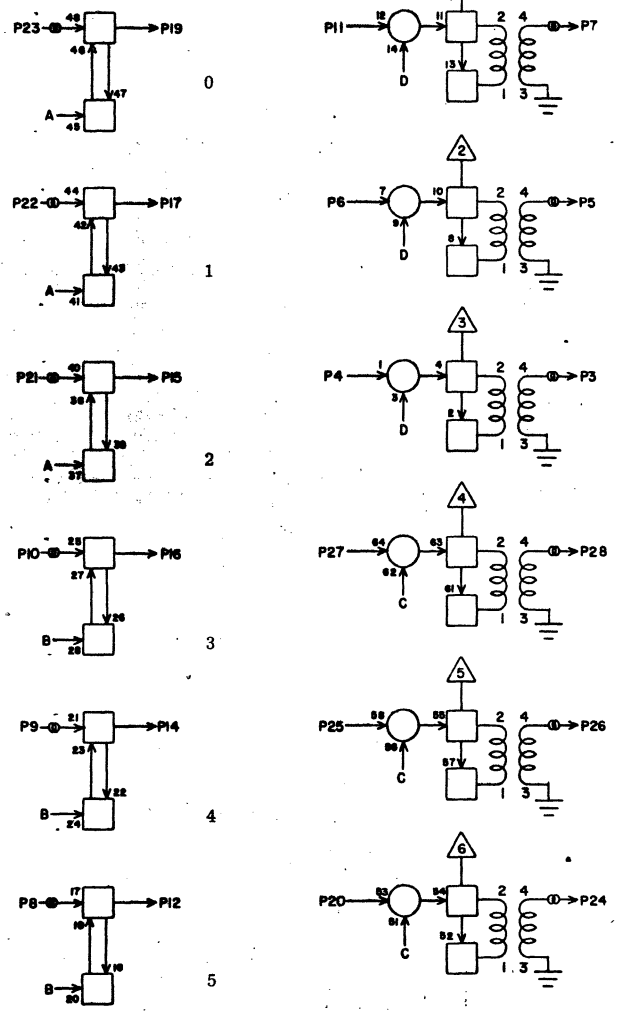
LS 63060900 ASSY | J REV

TO DATA CHANNEL A

BITS 0-5

QJ





K11

1			
2			
3			
4	I11	17	7
5			
6	I11	10	9
7			
8			
9			
10			
11	I11	13	9
12	I12	1	9
13			
14	I12	2	9
15	I11	28	9
16	I11	27	9
17	I11	1	9
18	J11	6	41
19	I11	2	9
20	I12	10	9
21			
22			
23			
24			
25	I12	13	9
26			
27	I11	20	9
28			
	JACK	PIN	LG

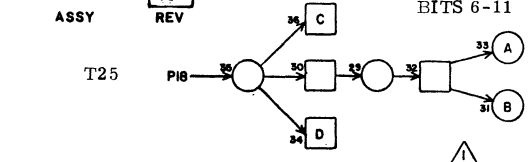
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

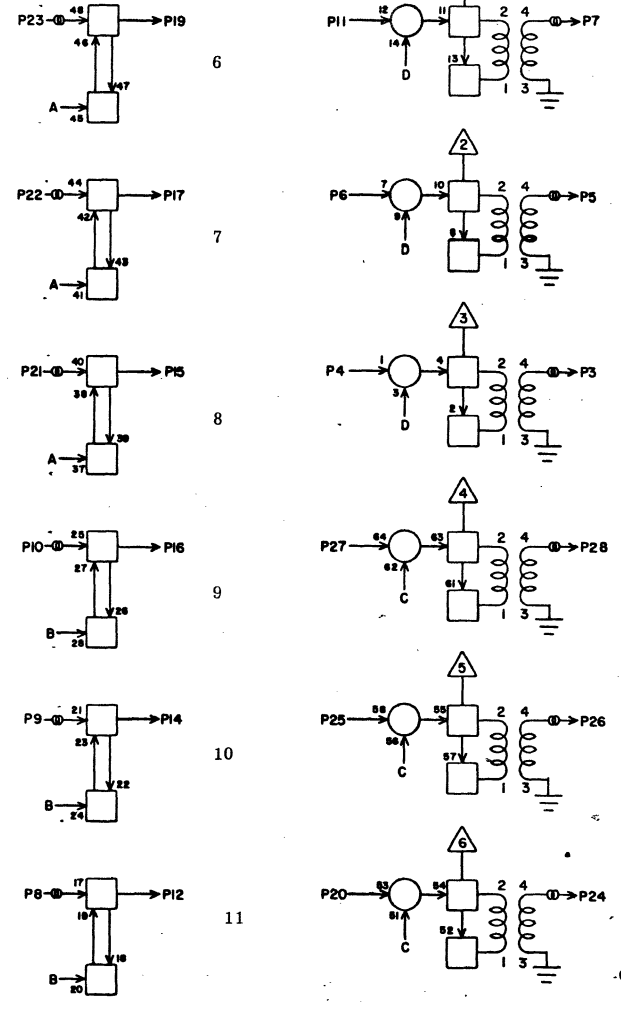
LS 63060900 ASSY | J REV

TO DATA CHANNEL A

BITS 6-11

QJ





K12

1			
2			
3			
4	I13	13	9
5			
6	I12	20	9
7			
8			
9			
10			
11	I12	17	9
12	I13	27	9
13			
14	I13	28	9
15	I13	2	9
16	I13	1	9
17	I12	27	9
18	J11	8	41
19	I12	28	9
20	I13	20	9
21			
22			
23			
24			
25	I13	17	9
26			
27	I13	10	9
28			
	JACK	PIN	LG

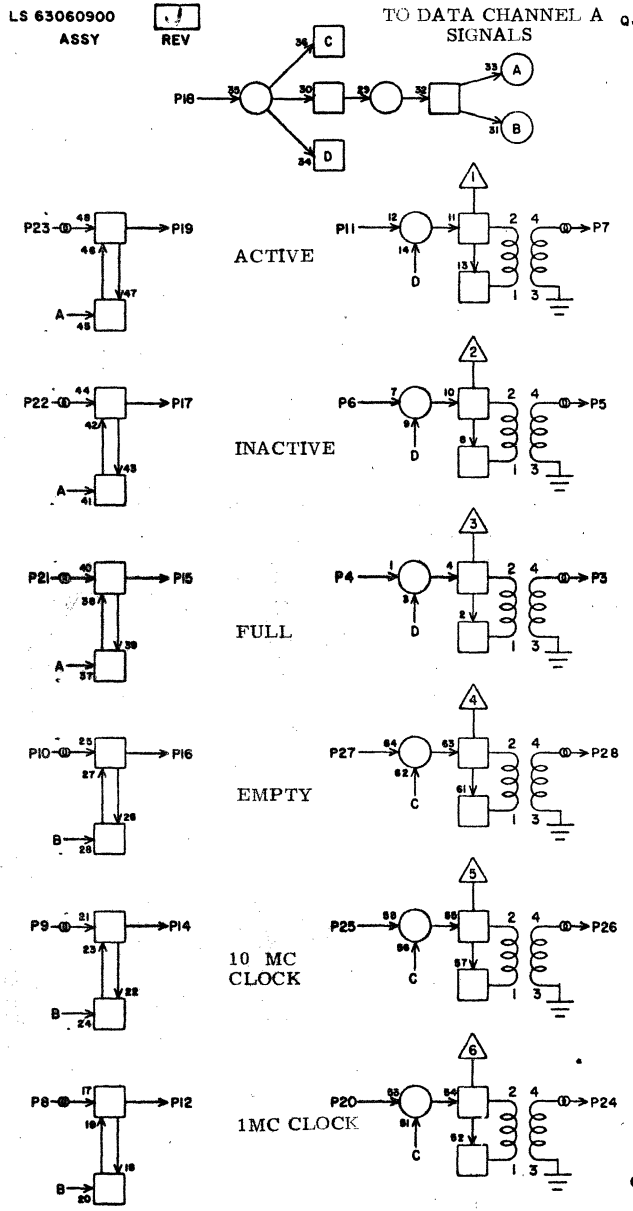
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63060900 ASSY

REV

TO DATA CHANNEL A SIGNALS

QJ



K13

	JACK	PIN	LG
1			
2			
3			
4	I09	16	9
5			
6	I09	28	9
7			
8			
9			
10			
11	K13	19	3
12	K13	20	3
13			
14			
15	I09	17	11
16	I09	22	11
17	I09	25	9
18	J13	4	7
19	K13	11	3
20	K13	12	3
21			
22			
23			
24			
25	K13	X	2
26			
27	I09	19	13
28			

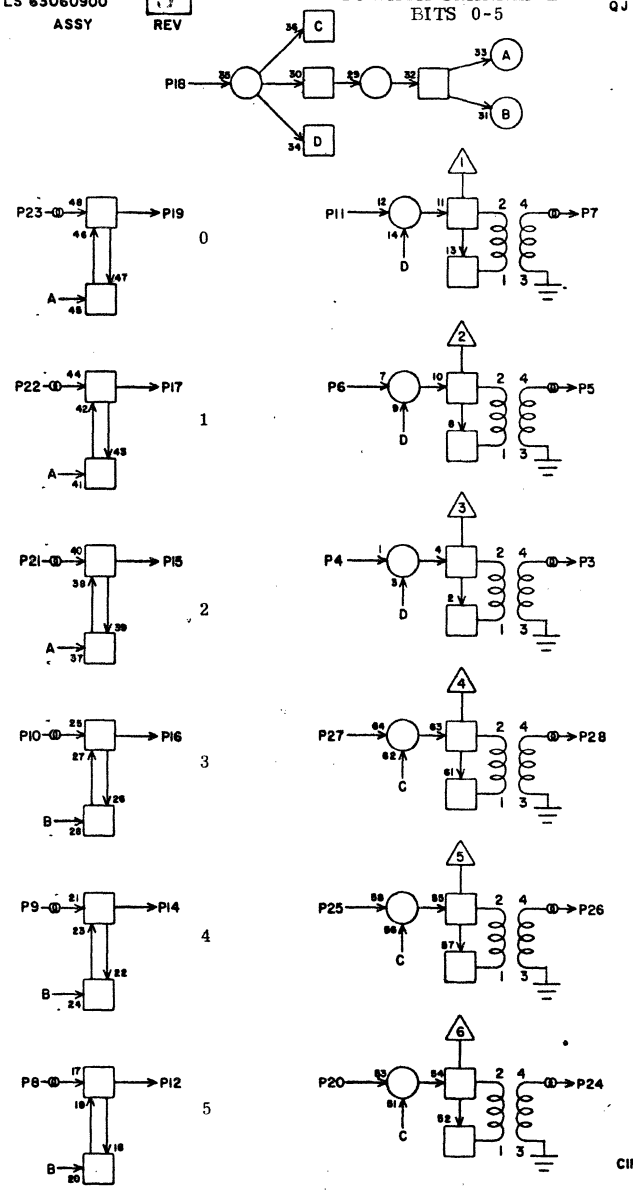
CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63060900 ASSY

REV

TO DATA CHANNEL B BITS 0-5

QJ



K14

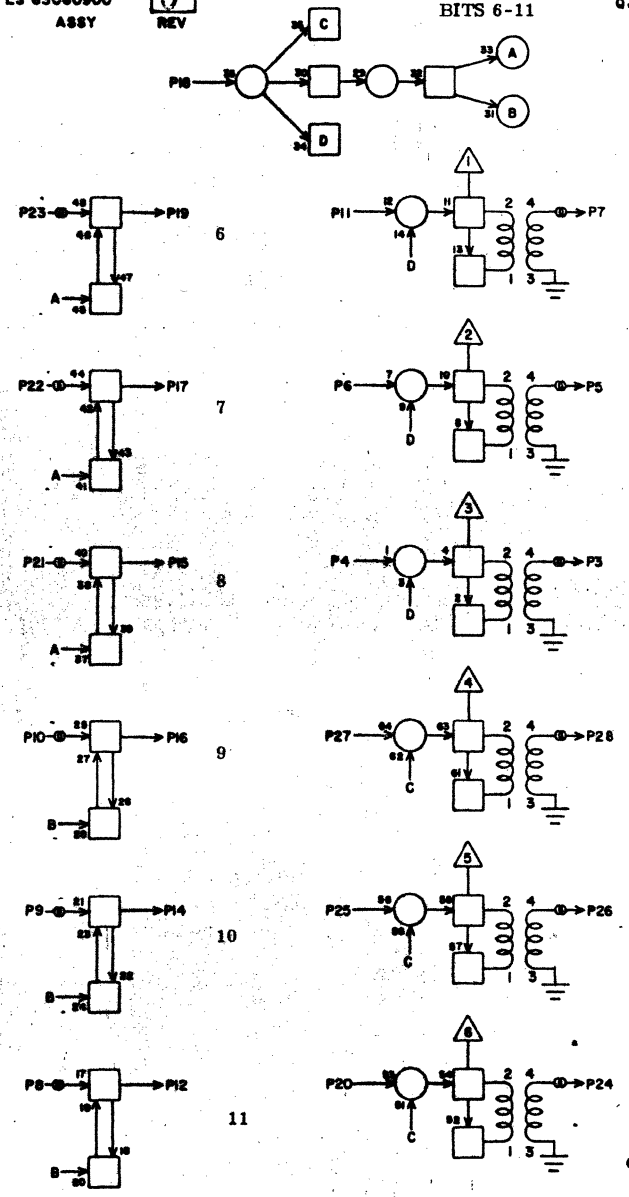
	JACK	PIN	LG
1			
2			
3			
4	I14	17	7
5			
6	I14	10	9
7			
8			
9			
10			
11	I14	13	9
12	I15	1	9
13			
14	I15	2	9
15	I14	28	9
16	I14	27	9
17	I14	1	9
18	J14	6	41
19	I14	2	9
20	I15	10	9
21			
22			
23			
24			
25	I15	13	9
26			
27	I14	20	9
28			

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63060900 ASSY REV

TO DATA CHANNEL B
BITS 6-11

QJ



K15

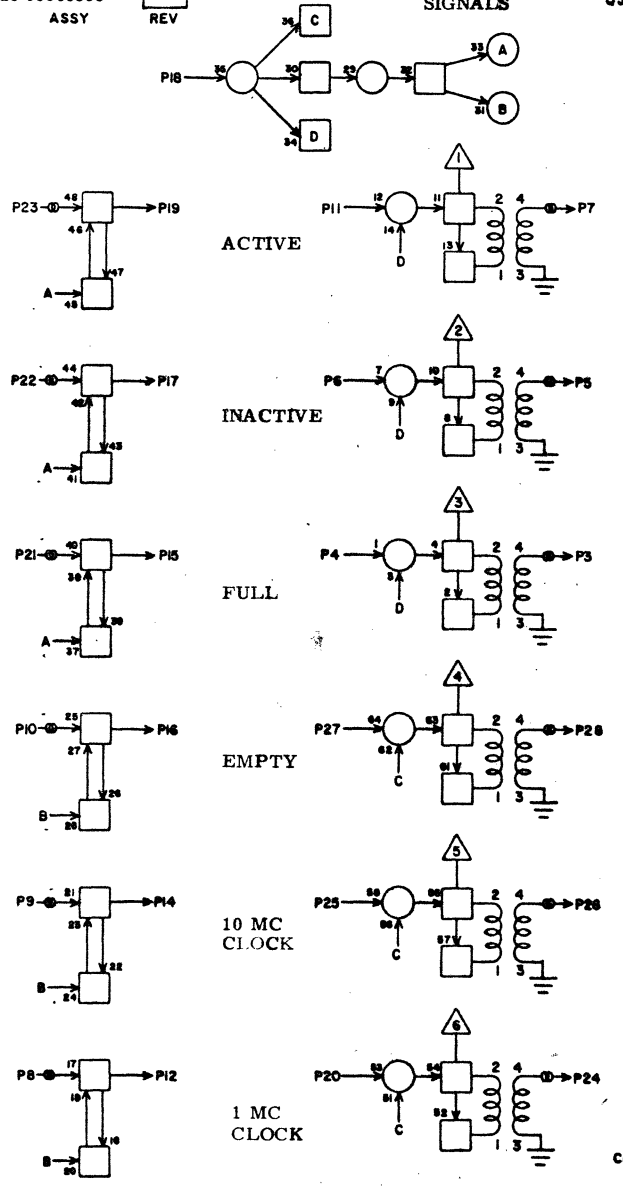
	JACK	PIN	LG
1			
2			
3			
4	I16	13	9
5			
6	I15	20	7
7			
8			
9			
10			
11	I15	17	9
12	I16	27	9
13			
14	I16	28	9
15	I16	2	9
16	I16	1	9
17	I15	27	9
18	J14	8	41
19	I15	28	9
20	I16	20	9
21			
22			
23			
24			
25	I16	17	9
26			
27	I16	10	9
28			

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LS 63060900 ASSY REV

TO DATA CHANNEL B
SIGNALS

QJ



K16

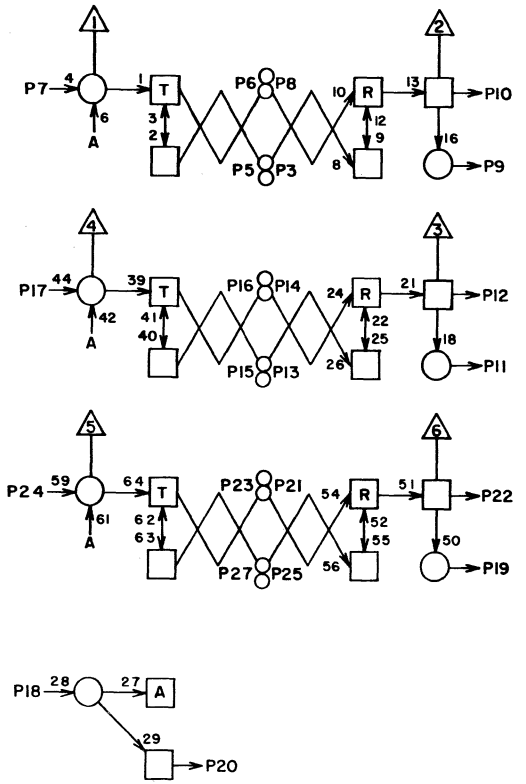
	JACK	PIN	LG
1			
2			
3			
4	I10	16	11
5			
6	I10	28	11
7			
8			
9			
10			
11	K16	19	3
12	K16	20	3
13			
14			
15	I10	15	11
16	I10	22	11
17	I10	25	11
18	J16	4	7
19	K16	11	3
20	K16	12	3
21			
22			
23			
24			
25	K16	X	2
26			
27	I10	19	11
28			

CIRCUIT SPECIFICATION 11827600
60196300
Rev A

LSI7876100 ASSY | A REV

DATA TO & FROM DISK FILE BITS 0-2

ZS



0

1

2

L01

1	-6V		2
2			
3	J-2	A2	6
4			
5	J-1	A2	8
6	J-1	A1	8
7	I03	3	13
8	J-2	A1	6
9			
10	J03	12	9
11			
12	J03	13	9
13	J-2	A4	6
14	J02	A3	6
15	J-1	A4	8
16	J-1	A3	8
17	I03	9	13
18	E02	25	25
19			
20	L02	18	3
21	J-2	A5	5
22	J03	16	9
23	J-1	A5	8
24	I03	2	13
25	J-2	A6	5
26			
27	J-1	A6	8
28			

JACK PIN LG

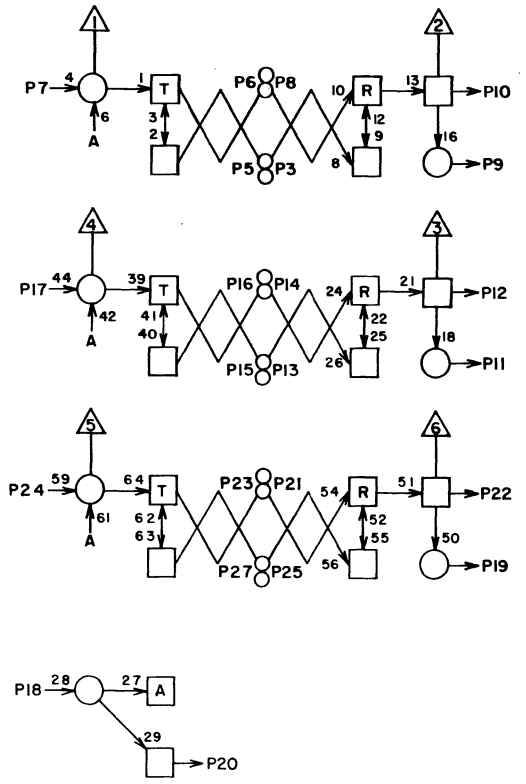
NOTES:

1. REFERENCE DRAWINGS:
   I7876500 LOGIC SCHEMATIC ZT
   I7876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

LSI7876100 ASSY | A REV

DATA TO & FROM DISK FILE BITS 3-5

ZS



3

4

5

L02

1	-6V		2
2			
3	J-2	A8	5
4			
5	J-1	A8	7
6	J-1	A7	7
7	I03	27	11
8	J-2	A7	5
9			
10	J03	19	7
11			
12	J04	12	9
13	J-2	A10	5
14	J-2	A9	5
15	J-1	A10	7
16	J-1	A9	7
17	I03	24	11
18	L01	20	3
19			
20	L03	18	3
21	J-2	B1	5
22	J04	13	9
23	J-1	B1	6
24	I03	26	11
25	J-2	B2	5
26			
27	J-1	B2	6
28			

JACK PIN LG

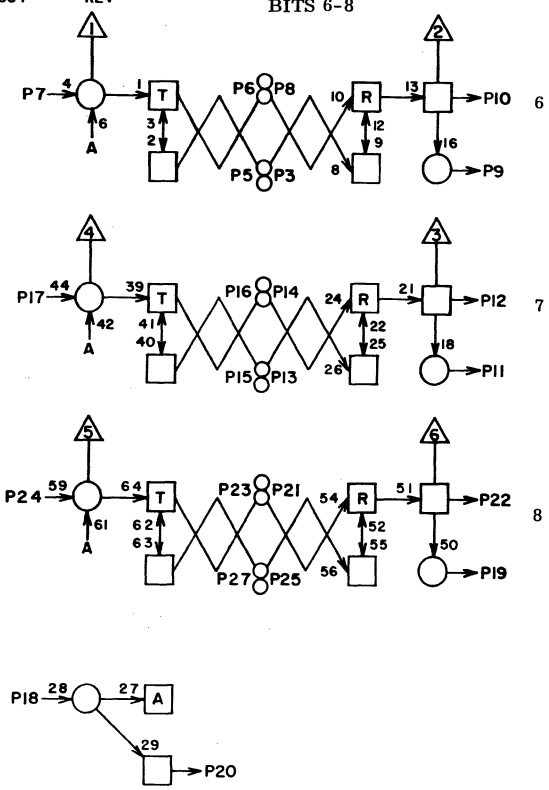
NOTES:

1. REFERENCE DRAWINGS:
   I7876500 LOGIC SCHEMATIC ZT
   I7876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

LSI7876100 ASSY | A REV

DATA TO & FROM DISK FILE
BITS 6-8

ZS



6 7 8

L03

1	-6V		
2			
3	J-2	B4	5
4			
5	J-1	B4	7
6	J-1	B3	7
7	I04	3	13
8	J-2	B3	5
9			
10	J04	16	9
11			
12	J04	19	7
13	J-2	B6	5
14	J-2	B5	5
15	J-1	B6	7
16	J-1	B5	7
17	I04	9	13
18	L02	20	3
19			
20	L04	18	3
21	J-2	B7	5
22	J05	12	9
23	J-1	B7	9
24	I04	2	13
25	J-2	B8	5
26			
27	J-1	B8	6
28			

JACK PIN LG

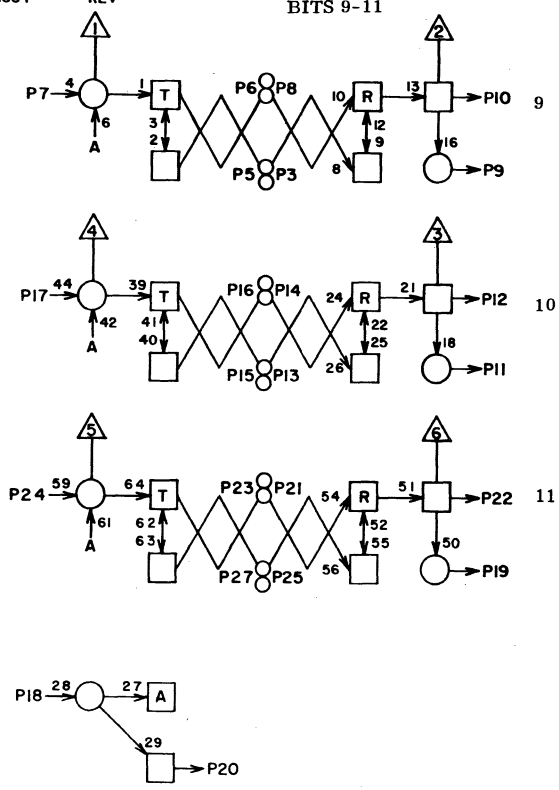
NOTES:

1. REFERENCE DRAWINGS:
   17876500 LOGIC SCHEMATIC ZT
   17876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

LSI7876100 ASSY | A REV

DATA TO & FROM DISK FILE
BITS 9-11

ZS



9 10 11

L04

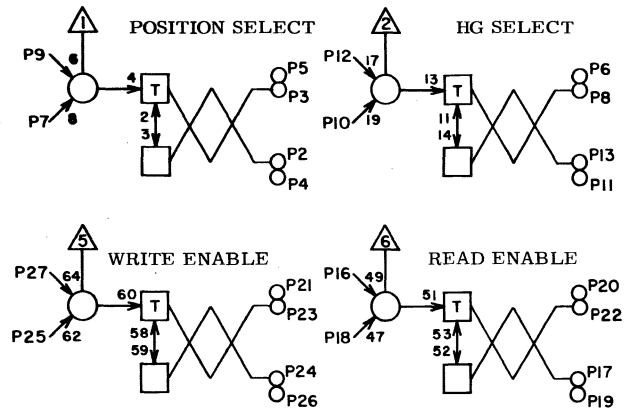
1	-6V		2
2			
3	J-2	B10	7
4			
5	J-1	B10	6
6	J-1	B9	6
7	I04	27	11
8	J-2	B9	7
9			
10	J05	13	9
11			
12	J05	16	9
13	J-2	C2	7
14	J-2	C1	7
15	J-1	C2	6
16	J-1	C1	6
17	I04	24	11
18	L03	20	3
19			
20			
21	J-2	C3	7
22	J05	19	9
23	J-1	C3	5
24	I04	26	11
25	J-2	C4	7
26			
27	J-1	C4	5
28			

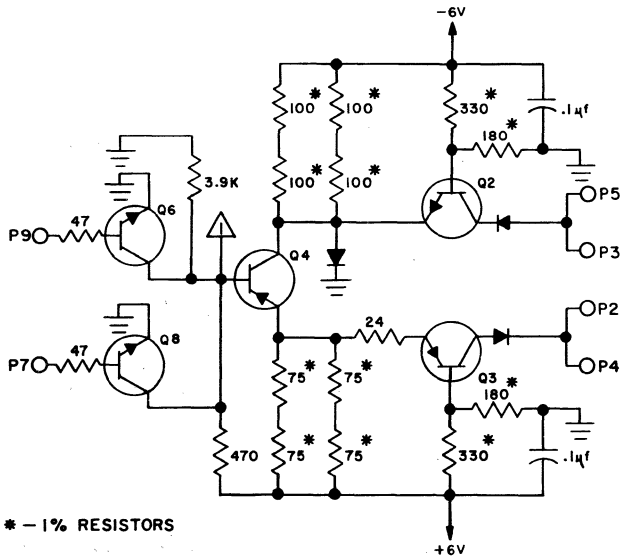
JACK PIN LG

NOTES:

1. REFERENCE DRAWINGS:
   17876500 LOGIC SCHEMATIC ZT
   17876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

LSI7876500 ASSY | A REV | ZT





* — 1% RESISTORS

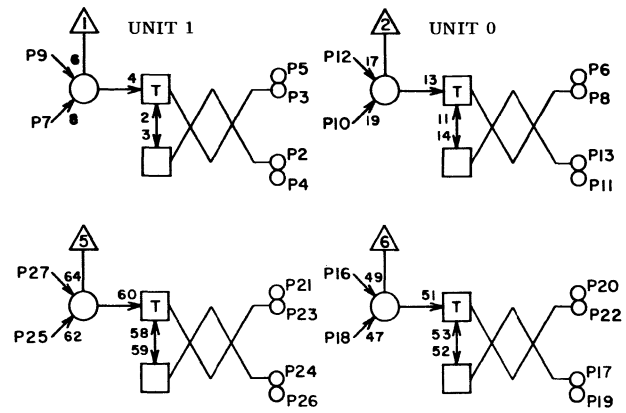
L05

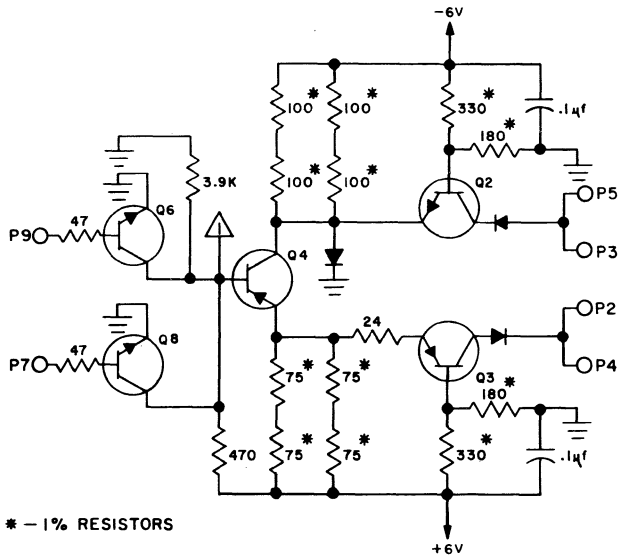
1	-6V		2
2	J-1	C8	6
3	J-2	C7	9
4	J-2	C8	9
5	J-1	C7	6
6	J-1	C5	6
7	L05	X	2
8	J-2	C5	9
9	E02	2	25
10	L05	X	2
11	J-2	C6	9
12	F06	2	21
13	J-1	C6	6
14			
15			
16	E08	25	23
17	J-1	D10	7
18	J08	19	11
19	J-2	D10	9
20	J-1	D9	7
21	J-1	D5	7
22	J-2	D9	9
23	J-2	D5	9
24	J-1	D6	7
25	J08	23	11
26	J-2	D6	9
27	F05	27	21
28			

JACK PIN LG

60196300
Rev A

LSI7876500 ASSY | A REV | ZT





* — 1% RESISTORS

L06

1	-6V		2
2	J-1	F8	8
3	J-2	F7	10
4	J-2	F8	10
5	J-1	F7	8
6	J-1	F5	8
7	L06	X	2
8	J-2	F5	10
9	C10	23	29
10	L06	X	2
11	J-2	F6	10
12	C10	14	29
13	J-1	F6	8
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			

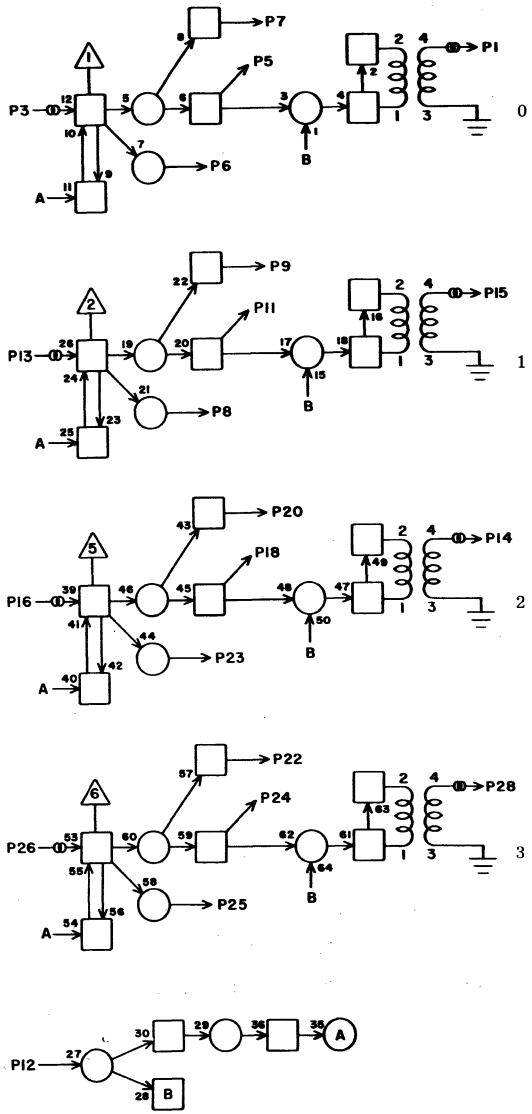
JACK PIN LG

60196300
Rev A

LS 63060800 ASSY F REV

DATA FROM CHANNEL A
BITS 0 - 3

Q1



L07

1			
2			
3			
4			
5	I07	6	13
6			
7	H16	8	17
8			
9			
10			
11	I07	7	13
12	J11	9	11
13			
14			
15			
16			
17			
18	I07	24	11
19			
20			
21			
22			
23			
24	I07	5	13
25			
26			
27			
28			

JACK PIN LG

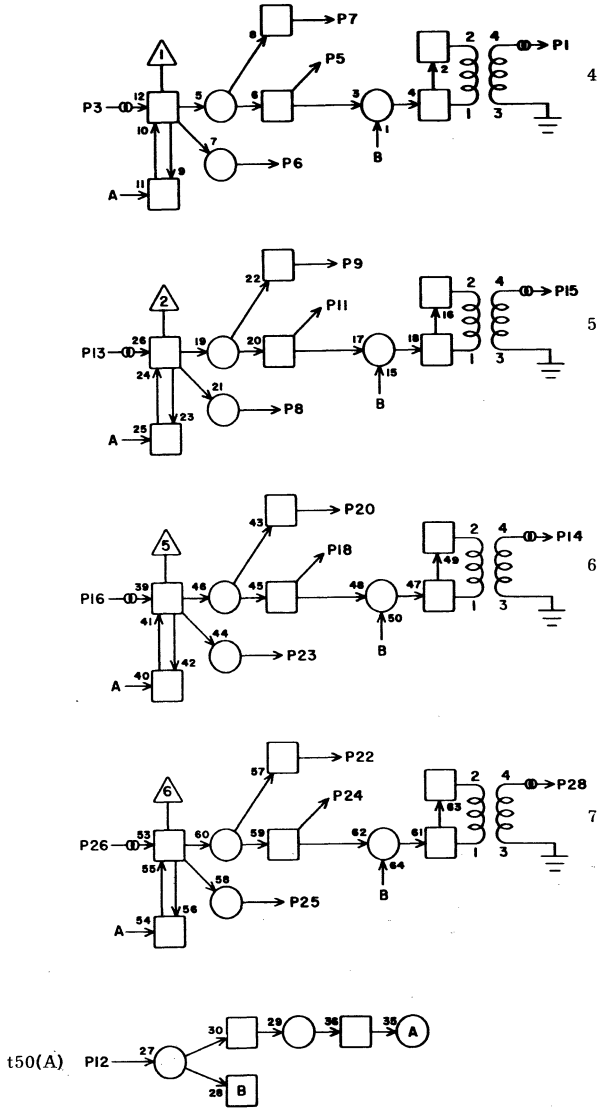
CIRCUIT SPECIFICATION 11827600

60196300
Rev A

LS 63060800 ASSY F REV

DATA FROM CHANNEL A

Q1



L08

1			
2			
3			
4			
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6			
7			
8	K06	13	7
9	H16	12	17
10			
11	I07	23	11
12	J11	11	9
13			
14			
15			
16			
17			
18	K09	24	5
19			
20	I08	6	13
21			
22	I08	7	13
23			
24	H16	5	19
25			
26			
27			
28			

JACK PIN LG

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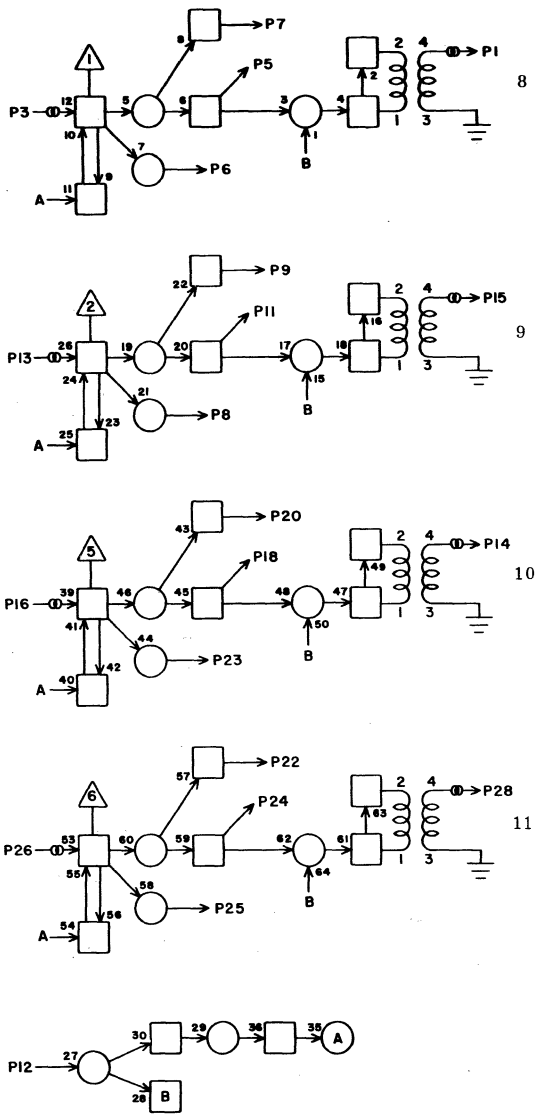
DATA FROM CHANNEL A

Q1



L09

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2			
3			
4			
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6			
7	I08	24	11
8			
9	I08	5	13
10			
11	K09	8	5
12	J11	13	9
13			
14			
15			
16			
17			
18			
19			
20	I08	22	13
21			
22	I08	23	13
23	K09	6	7
24			
25	K09	4	7
26			
27			
28			

JACK PIN LG

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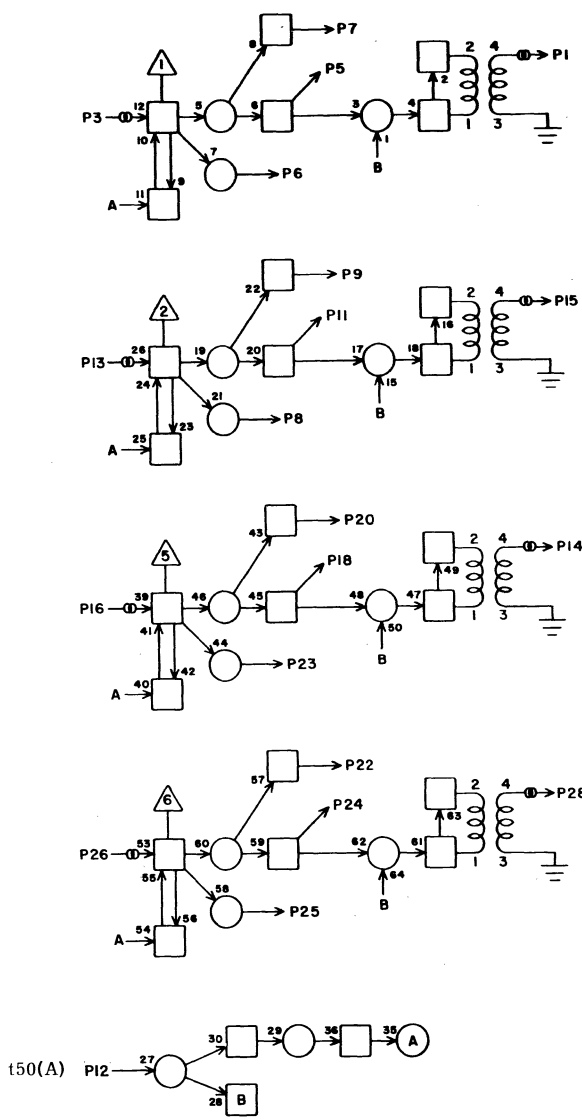
SIGNALS FROM CHANNEL A

Q1



L10

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2			
3			
4			
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7	I06	5	13
8			
9	I06	24	11
10			
11	K04	5	9
12	J11	16	9
13			
14			
15			
16			
17			
18	I06	6	13
19			
20			
21			
22	I06	22	13
23			
24	K06	24	7
25			
26			
27			
28			

JACK PIN LG

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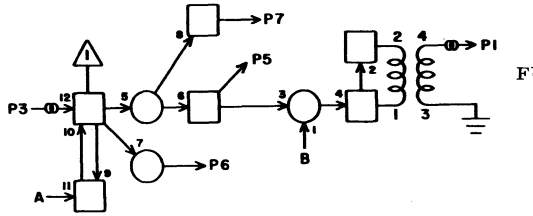
SIGNALS FROM CHANNEL A_{Q1}



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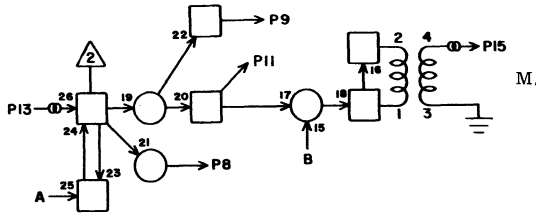

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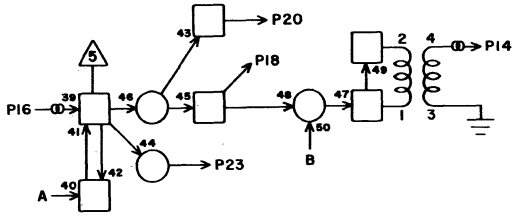

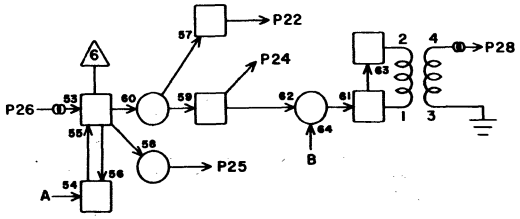

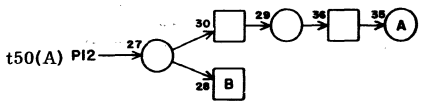

L11

1			
2			
3			
4			
5			
6			
7	K09	2	7
8	K06	17	7
9			
10			
11	I05	21	13
12	J11	18	9
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
	JACK	PIN	LG

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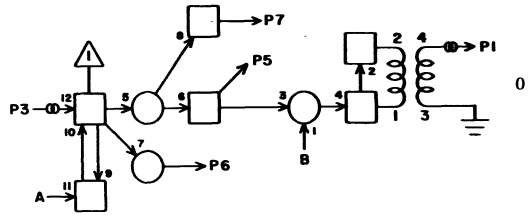
DATA FROM CHANNEL B
BITS 0 - 3

Q1



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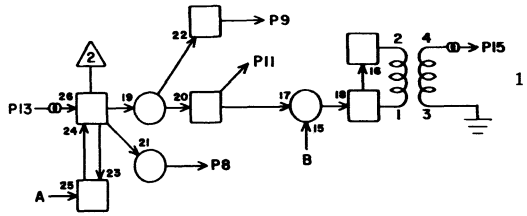
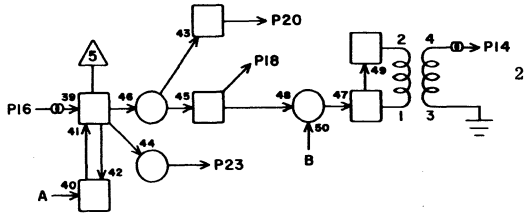


1



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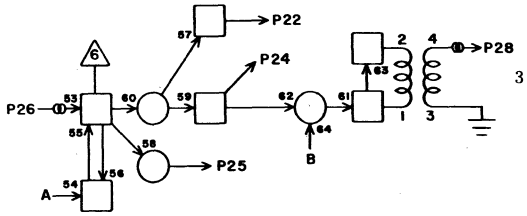

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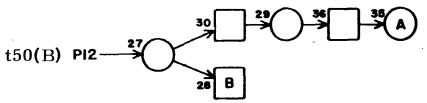

L12

1			
2			
3			
4			
5	I07	4	13
6			
7	H16	21	15
8			
9			
10			
11	I07	13	13
12	J14	9	9
13			
14			
15			
16			
17			
18	I07	26	13
19			
20			
21			
22			
23			
24	I07	3	15
25			
26			
27			
28			
	JACK	PIN	LG

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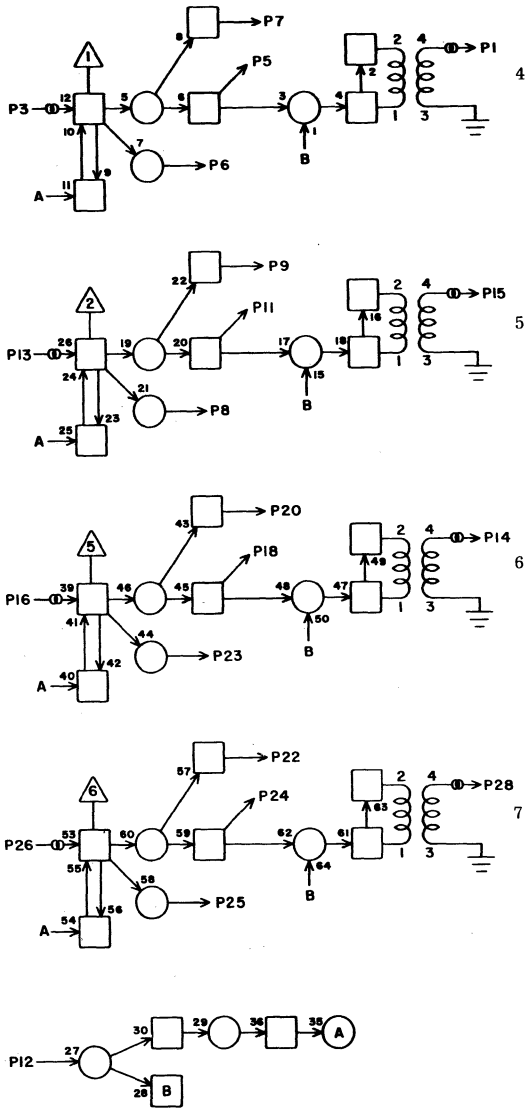
DATA FROM CHANNEL B
BITS 4-7

Q1



L13

1			
2			
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4			
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6			
7			
8	K07	13	9
9	H16	23	15
10			
11	I07	25	13
12	J14	11	9
13			
14			
15			
16			
17			
18	K10	24	7
19			
20	I08	4	15
21			
22	I08	13	13
23			
24	H16	24	15
25			
26			
27			
28			

JACK PIN LG

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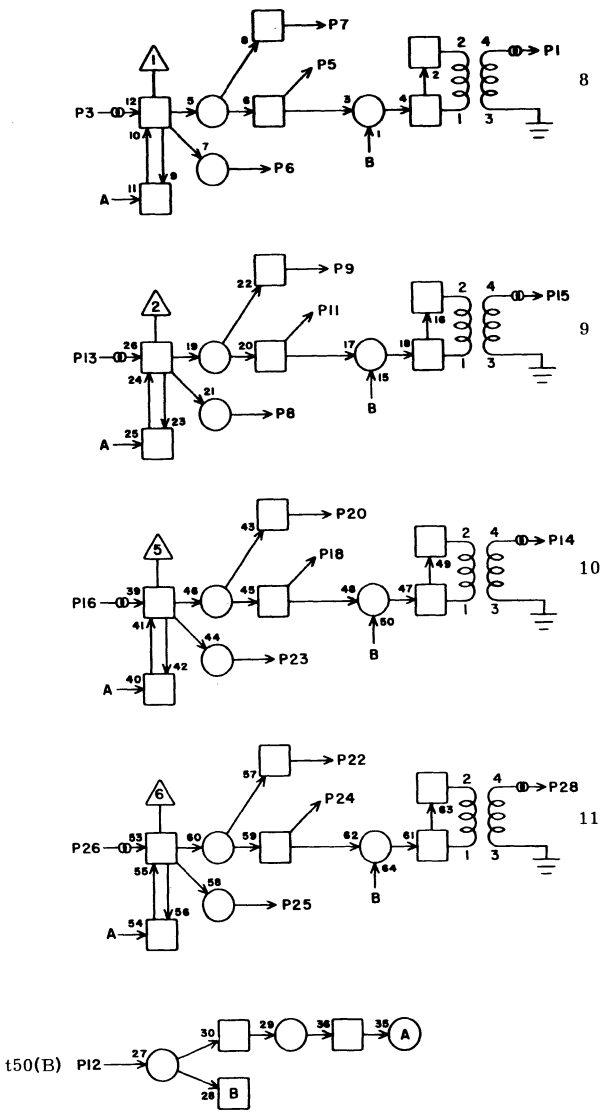
DATA FROM CHANNEL B
BITS 8-11

Q1



L14

1			
2			
3			
4			
5	K10	28	7
6			
7	I08	26	13
8			
9	I08	3	13
10			
11	K10	8	7
12	J14	13	9
13			
14			
15			
16			
17			
18			
19			
20	I08	18	13
21			
22	I08	25	13
23	K10	6	9
24			
25	K10	4	9
26			
27			
28			

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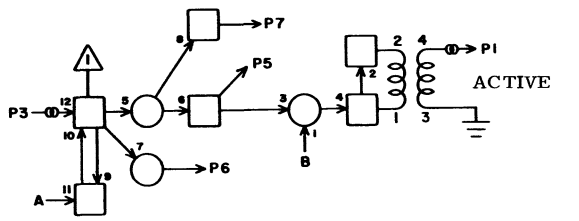
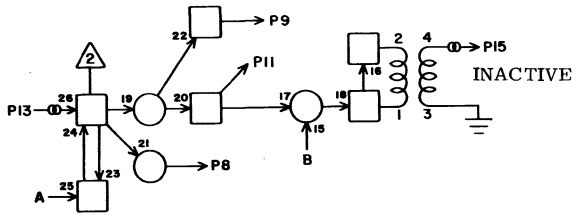
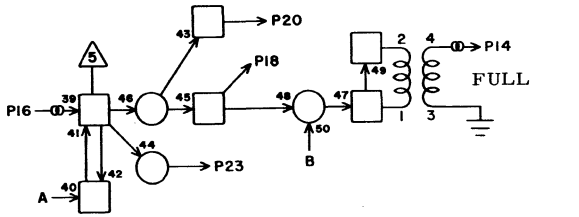
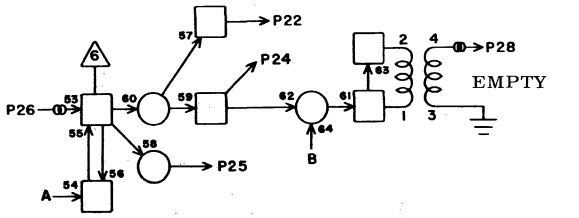
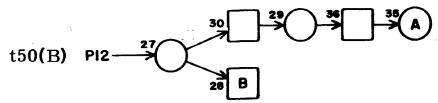
SIGNALS FROM CHANNEL B Q1











L15

1			
2			
3			
4			
5	K07	23	11
6	K07	28	11
7	I06	3	17
8			
9	I06	26	15
10			
11	K04	15	15
12	J14	16	9
13			
14			
15			
16			
17			
18	I06	4	17
19			
20			
21			
22	I06	18	15
23			
24	K07	24	11
25			
26			
27			
28			

JACK PIN LG

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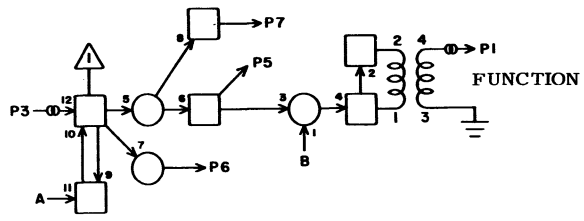
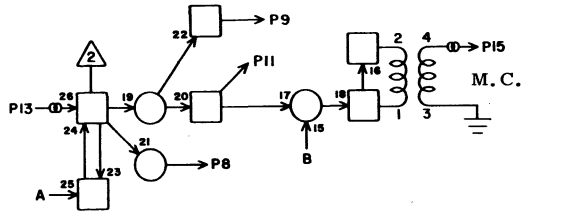
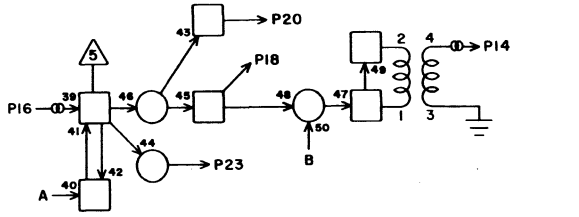
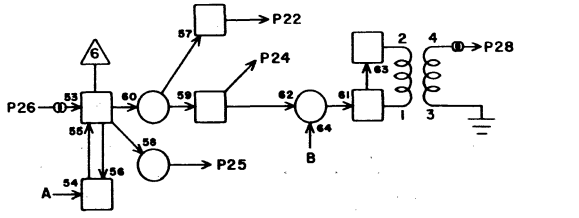
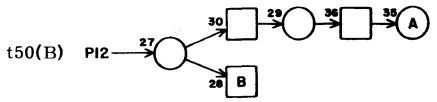
SIGNALS FROM CHANNEL B Q1











L16

1			
2			
3			
4			
5			
6			
7	K10	2	9
8	K07	17	11
9			
10			
11	I05	25	17
12	J14	18	9
13			
14			
15			
16			
17			
18			
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Customer Engineering Manual

Pub. No. 60196300

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