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**CONTROL DATA®  
6000 SERIES COMPUTER SYSTEM  
6642 DISTRIBUTIVE DATA PATH**

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**OPERATION AND PROGRAMMING  
REFERENCE MANUAL**



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## PREFACE

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This manual contains reference information for the CONTROL DATA® 6642 Distributive Data Path. For reference information pertaining to Extended Core Storage (ECS) and the 6640 ECS Controller, see the Extended Core Storage Reference Manual, Pub. No. 60225100. Refer to the Literature Distribution Services Catalog for the latest revision of this manual.



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INTRODUCTION

The Distributive Data Path unit (DDP) provides the capability for any 6000 Series PPU to communicate with Extended Core Storage. The DDP has one PPU port in the standard configuration, with two, three, and four PPU port configurations available (Figure 2-1). Each port accomodates one PPU channel.

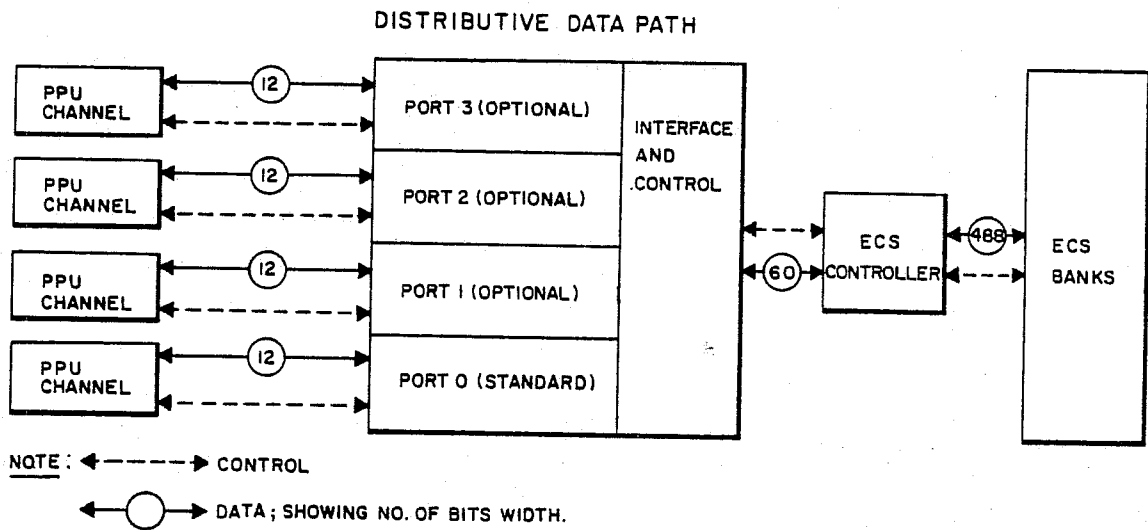


Figure 2-1. DDP Configuration

The DDP communicates with the ECS Controller through one of the four, 60-bit controller accesses, and communicates with PPU's through 12-bit normal data channels. The DDP allows a PPU to do block transfers, or to modify a 480-bit ECS record by writing a single 60-bit word into the ECS record.

A DDP port consists of nine 60-bit buffer registers, a 24-bit Address/Flag Word register, and PPU channel interface and control logic. A port may operate in maintenance mode to perform diagnostics, or to transmit an ECS record containing a parity error to a PPU.

## PROGRAMMING

### DATA ASSEMBLY

The DDP assembles (on a write operation) or disassembles (on a read operation) a full ECS record of 480 bits in eight of the buffer registers. The ninth buffer register accommodates 12-bit byte transfers between the PPU and the DDP port while the 480-bit ECS record is transferred between the DDP and the ECS Controller. The buffer registers hold 12-bit bytes as shown in Figure 2-2.



Figure 2-2. DDP Assembly of Bytes in a 60-bit Word

### FUNCTION CODES

A DDP port performs functions according to a 12-bit function code and the upper three bits of a 24-bit address/flag word. The most significant octal digit (5) is the equipment select code for the DDP. Table 2-1 shows codes and upper address bit values for legal functions.

TABLE 2-1. DDP FUNCTION CODES AND UPPER ADDRESS BITS

Function	Code	Address Bit 23	Address Bit 22	Address Bit 21
Block Read ECS	5001	0	0	0
Block Write ECS	5002	0	0	0
Select Status	5004	0	0	0
Master Clear Port	5010	0	0	0
Read ECS, One Reference	5001	0	1	0
Select Maintenance Mode	5001	0	0	1
Function Flag Register	5001	1	X	X

## 5001 — BLOCK READ ECS

This function causes the port to read data from ECS and direct the data to the PPU channel to be read by the PPU. The port responds to a Block Read ECS function by disconnecting the data channel. When the channel is activated by the PPU, the port accepts an output of two 12-bit bytes from the PPU and loads them into the 24-bit Address Register. The port then requests ECS and holds the data received for input to the PPU.

The first 12-bit byte received from the PPU is put into the upper portion of the Address Register; the second 12 bits are put into the lower portion of the Address Register. The Address Register now designates the address of the first 60-bit word to be made available to the PPU. This address is presented to the controller along with a Request signal. As data is received from the controller the Address Register is incremented once for each 60-bit word. When data is received from ECS, it is presented to the PPU. When the PPU has emptied the data buffer, a new ECS reference is made. Unless an error condition is encountered, the port continues to present data to the PPU in this manner until the PPU terminates the read operation by disconnecting the data channel.

Two error conditions cause the port to disconnect the data channel during a Block Read ECS operation. They are:

- ECS Abort
- ECS Parity Error

If the port receives either of these two conditions from the controller, the port will disconnect the data channel when it is Empty, rather than send a Full and the next byte of data. Thus, in order to prevent a data channel hang-up when disconnecting via the PPU, the PPU must look for a Full condition on the data channel before performing a disconnect.

### NOTE

The PPU must not disconnect the data channel if it senses the channel as being Empty, as the port may disconnect before the PPU disconnect instruction can be carried out causing the PPU to hang on that instruction.

When the data channel is disconnected by the port, the PPU must issue a Select Status (5004) function to determine the reason for the disconnect. In the case of Parity Error, the PPU may issue a Read function while in maintenance mode to input the data contained in the buffer registers. After a parity error, the PPU must issue a new Block Read ECS function or a Single Record Read function to read more data from ECS.

A typical instruction sequence to do a block ECS Read is:

Address	Instruction		Comments
	FNC	5001	Send 5001 function to channel
	ACN		Activate channel
	OAM	XXXX	(A)=2, output two bytes on channel for ECS address.
	IAM	XXXX	Input (A) bytes of data from channel
	NJN		Check reason for exit from previous instruction. If (A)=0 then transfer is complete; if (A)≠0 then DDP disconnected channel. In the latter case the NJN instruction would cause a jump to an error checking routine.
B	IJM	A	Jump to A if channel is inactive
	EJM	B	Jump to B if channel is empty
	DCN		Disconnect channel
A	Continue		

Note that the time required for the channel to change from the Active and Empty state may vary from 0 to 50 microseconds. The Block Read ECS condition is cleared by a disconnect or a Channel Master Clear.

#### 5002 — BLOCK WRITE ECS

This function causes the port to write data into ECS, from data sent to the port via the PPU. The port responds to an ECS Write function by disconnecting the data channel. When the PPU activates the channel, the port accepts a block output of data. The first two bytes of data received from the PPU are loaded into the 24-bit Address Register. Additional bytes received from the PPU are regarded as data to be sent to ECS.

The DDP places the first 12-bit byte into the upper portion of the Address Register, and the second byte into the lower portion of the Address Register. The Address Register now designates the address of the first 60-bit word to be written. The DDP presents this address to the ECS Controller along with a request signal after the buffer in the port is filled by the PPU or after a disconnect from the PPU. The Address Register is incremented as the buffer empties into ECS. Unless an error condition is encountered, data continues to be transferred. A disconnect from the PPU causes accumulated data to be written into ECS, but increments the Address Register only by the number of 60-bit words written into ECS. A disconnect also terminates the BlockWrite ECS condition. If the PPU disconnects with less than an integer multiple of 60-bit words assembled in the buffer registers, the port writes the partial 60-bit word into ECS with zeros in the missing byte(s).

A program sequence such as the following produces a partial ECS write with zero fill.

Instruction	Comments
FNC 5002	Send 5002 function to channel
ACN	Activate channel
LDC 20 <sub>10</sub>	Load A register with 20 <sub>10</sub> (18 bytes data 2 bytes address)
OAM	Output 20 <sub>10</sub> bytes on channel
DCN	Disconnect channel

When the channel is disconnected, the data in the buffers progresses to fill the buffer registers as shown in Figure 2-3.

Rank	0	1	2	3	4	5	6	7	8	
	0	0	0	0	0	X	X	X	X	Where X=one byte of PPU data
	0	0	0	0	0	X	X	X	X	
	0	0	0	0	0	X	X	X	X	
	0	0	0	0	0	0	X	X	X	
	0	0	0	0	0	0	0	X	X	
	0	0	0	0	0	0	0	X	X	

Figure 2-3. DDP Buffer Register Contents on a Partial Write

An ECS reference is then made. Only four 60-bit words are written into ECS: 216 bits of data followed by 24 bits of zero fill. The remaining 240 bits of the ECS record are not altered. Note that this allows writing a single 60-bit word anywhere in the ECS record by sending an address and five, 12-bit bytes to the port. The lower three bits of the address specify the 60-bit word to be written in the 480-bit record specified by the upper address bits.

Only the Abort error condition is possible on ECS Write. When the controller returns an Abort signal during a PPU-port transfer, the port disconnects the I/O channel. This disconnect is sent to the I/O channel in the place of an Empty response to a Full signal from the data channel. The Inactive status on the channel causes an exit from the OAM instruction to a jump instruction. Before issuing a new read or write function, the PPU must issue a Select Status (5004) function to determine whether the write status bit has dropped, or whether the ECS Controller returned an Abort to the port after the PPU disconnected the channel.

A typical instruction sequence to do a Block Write ECS is:

Instruction	Comments
FNC 5002	Send 5002 function to channel
*OAM XXXX	(A)=2; output two bytes on channel as ECS address
*OAM XXXX	Output data
NJN	Check reason for exit from previous instruction. If (A)=0 then transfer is complete; if (A)≠0 then DDP disconnected channel. In the latter case, the NJN instruction would cause a jump to an error checking routine.
DCN	Disconnect channel
FNC	Read status until either an Abort or an Accept is detected. This requires from zero to 50 μsec, depending on ECS activity.

The Block Write ECS condition is cleared out by a disconnect, a new function, or by a channel Master Clear.

\*A single OAM could be used.

## **5004 — SELECT STATUS**

This function makes the status of the port available for PPU input after the channel is activated by the PPU. The port responds to this function by disconnecting the channel. The PPU then activates the channel and performs an input.

Status bits are assigned to indicate the following: (Bits 4 through 11 are not used)

Bit 0	ECS Abort
Bit 1	ECS Accept
Bit 2	ECS Parity Error
Bit 3	ECS Write Selected

### **BIT 0 — ECS ABORT**

This status bit is cleared upon a new request to ECS, a Select Status or Master Clear Port function, or a channel Master Clear.

### **BIT 1 — ECS ACCEPT**

This status bit is cleared upon a new Request to a Select Status or Master Clear Port function, or a channel Master Clear.

### **BIT 2 — ECS PARITY ERROR**

This status bit indicates that a 60-bit word from ECS was found to have a parity error. This bit is cleared upon a Select Status or Master Clear Port function, or a channel Master Clear.

### **BIT 3 — ECS WRITE SELECTED**

The status bit indicates that the port is busy with an ECS Write. When the write terminates, the status bit clears.

## **5010 — MASTER CLEAR PORT**

This function performs a Master Clear on the port logic.

## **5001 — WITH ADDRESS BIT 22 SET, READ ECS, ONE REFERENCE**

This function is identical to Block Read ECS except that only one reference is made to ECS.

#### **5001 — WITH ADDRESS BIT 21 SET, SELECT MAINTENANCE MODE**

This function blocks the port associated with that channel from requesting ECS. This allows data to be put into the port buffer from the PPU, and then to be read back again for hardware maintenance purposes.

A PPU may input an ECS record containing a parity error by selecting maintenance mode and performing a Read function. The port returns only the record in its buffer registers. The PPU will hang if more data is requested than the buffer contains.

A Read or Write function with address bit 21 clear brings a port out of maintenance mode and allows it to function normally.

#### **5001 — WITH ADDRESS BIT 23 SET, FUNCTION FLAG REGISTER**

This function is used to do a Flag Register operation. The contents of the Flag Register in the ECS Controller cannot be read directly, but may be interrogated and/or changed. When address bit 23 is set, the controller treats the address as a Flag Function word, and no ECS reference is made.

The port responds to the 5001 function code by disconnecting the I/O channel. The PPU then activates the channel, and sends the Flag word out as two 12-bit bytes. The port places the first byte in the upper part of the Address Register, and the second byte in the lower part of the Address Register. When the port sends the contents of the Address Register to the controller, the controller monitors the upper three bits to determine which Flag Register Function to perform.

ECS Controller responses to Flag Function operations are described in the ECS Reference Manual, Publication Number 60225100.



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