UNISTAR
SYSTEM REFERENCE
MANUAL

304040A

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* First Printing: August 1982 *
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WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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CHAPTER 1 SYSTEM HARDWARE

This manual provides the user a complete description and specifications for the hardware elements which comprise the UNISTAR family of system products. Sufficient information is provided to allow system installation, checkout and configuration. However, this manual is not intended as a service manual.

Chapter 2 provides the specifications for the basic UNISTAR system enclosure. The power system with both A.C. voltage reconfiguration and D.C. load capabilities is provided in Chapter 3.

WARNING: THE LABEL ON THE REAR PANEL OF THE UNISTAR INDICATES THE AC OPERATING VOLTAGE REQUIRED. ONLY TRAINED AND QUALIFIED SERVICE PERSONNEL SHOULD RECONFIGURE A.C. OPERATING VOLTAGES. INCORRECT RECONFIGURATION CAN CAUSE DAMAGE TO THE UNIT AND VOID CALLAN WARRANTY.

First time UNISTAR operators should refer immediately to Chapter 4 for System Initialization,Checkout and Shutdown procedures in order to insure the integrity of the systems' installed software.

The Basic 5 1/4" disk drive configuration information and performance specifications are provided in Chapter 6. The UNISTAR incorporates a variety of I/O panel configuration options which are defined in Chapter 7.

The UNISTAR incorporates a family of Multibus boards installed in the system card cage. Chapter 8 defines the boards and their factory installed jumper configuration tables. Detailed hardware manuals are provided for each board in Volume II of the UNISTAR Hardware Reference Manual.

The Multibus/IEEE 796 Card Cage Motherboard and its configuration options are described in Chapter 9 as well as standard installation configuration for the UNISTAR board set.

Finally, Chapter 10 provides software system installation specific information and the system hard disk regeneration procedure from floppy disk.

The UNISTAR terminal controller which emulates VT100 style terminal, has certain configuration options which are covered in Chapter 5. Users requiring terminal programming information, should refer to the UNISTAR Intellegent Video Terminal Users' Manual included elsewhere in Volume I of the UNISTAR Hardware Reference Manual.

CHAPTER 2 UNISTAR SYSTEM SPECIFICATIONS

2.0 CHAPTER OVERVIEW

General system level specifications are presented here in tabulated format. The information is aimed at providing an indication of the appropriate operating environment within which to use the UNISTAR system. Additional information provides the OEM with the requirements to be placed upon additional subassemblies that may be potentially installed within the UNISTAR enclosure.

2.1 AC INPUT SPECIFICATIONS

Power is delivered to the UNISTAR enclosure via a standard male type power receptical on the rear I/O panel. The standard unit is delivered configured to operate at 115 VAC at 60 HZ nominal.

* 105 VAC - 125 VAC at 60 HZ, 4A(RMS) max. load
* 210 VAC - 250 VAC at 50 HZ, 2A(RMS) max. load
* Fans operate at 115 VAC nominal
* Maximum power-on inrush current 25 amps
* AC voltage internally reconfigurable

2.2 OPERATING ENVIRONMENT (EXCLUSIVE OF FLEXIBLE DISK MEDIA)

The following environmental specifications apply to normal operation of the UNISTAR and are specified to provide reliable system performance within the indicated ranges. The normal operating temperature range that applies to flexible disk media operation is 10 to 52 ^{o} C (50 to 125^{o} F).

* Temperature (rear access cover installed) 10.0 to 40.0^{o} C (50 to 104^{o} F)
* Temperature (rear cover removed for service) 10 to 26.7^{o} C(50 to 80^{o} F)
* Altitude 8000 ft (2.4 Km)

* Humidity, relative 10% to 90%

* Maximum wet bulb: 28° C (82° F)

* Minimum dew point: 2° C (36° F)

2.3 DIMENSIONS AND WEIGHT

* Width: 20 1/2" (52 cm)

* Depth: 19 1/4" (53 cm without keyboard)

* Depth: 25" (63.5 cm with keyboard)

* Height: 14 1/2" (37 cm)

* Weight: 75 lbs.

* Shipping weight: 87 lbs. not including documentation

2.4 POWER

* Input Power
  500 VA apparent
  300 watts maximum
  150 watts typical

* Current Limiting Fuse
  115 VAC 4A Type F, Callan P/N 663-0002
  230 VAC 2A Type F, Callan P/N 663-0003

* Power Cord
  115 VAC Callan P/N 694-0002
  230 VAC Callan P/N 694-0003

2.5 INTERNAL D.C. POWER SPECIFICATIONS

* Switching power supply outputs
  +5V at 25 amps
  +12V linear regulated at 4 amps
  +12V motors at 4 amps, (10 amps peak start current)
  -12V at 3 amps
  -5V at 0.5 amp

* Reserve card cage D.C. power with the UNISTAR CPU, 64K Multibus Memory, WDC and FDC Boards, minifloppy drive and Winchester Drive installed.

  Available power:
  +5V, 8.0 amps
  +12V, 1.3 amps
  -12V, 1.8 amps
  -5V, .5 amps

* No combination of loads to exceed a maximum of 225 watts on power supply outputs.

2.6 SYSTEM BOARD OPERATING REQUIREMENTS

The standard family of UNISTAR system Multibus circuit boards and other optional boards installed by an OEM meet the following specifications so that they operate reliably within the system environment.

* Voltages ± 5%
* Temperature, operating 0-55o C
* IEEE 796, Multibus compatible
* Available UNISTAR card slots; two

2.7 I/O PANEL CONNECTOR SLOTS

The rear panel of the UNISTAR contains an I/O connector area that has mounting provisions for the following connector options.

* One RS-423, pre-cabled to CPU
* Eight RS-232C
* One parallel, Centronics style printer interface, 36 pin, AMP 'champ style' cutout
* Ethernet 15 pin 'D type' cutout
* Two direct connect telephone line connector cut-outs

2.8 SAFETY

* Designed to U.L. and C.S.A. requirements, approvals pending

CHAPTER 3 POWER SYSTEM INFORMATION

3.0 CHAPTER OVERVIEW

This chapter provides system information on the AC power input and DC output of the UNISTAR switching power supply. Information is provided on changing AC input voltage.

DC output specifications are provided for spare card cage capacity.

3.1 POWER SYSTEM SCHEMATICS

The schematics of figures 3-1 and 3-2 show the distribution of AC and DC power within the UNISTAR package. Note that the P2 motherboard option shown on schematic 3-1 is not incorporated in UNISTAR systems. This schematic shows the overall connection of power in the Callan Data Systems, UNISTAR package. Power is distributed from the switching power supply by a power distribution board which provides all necessary power interconnection to the system.

The system incorporates two 115 VAC fans which are operated with an autotransformer in assembly #200085. This circuit allows the system to be operated at 230 VAC without replacement of the fans. Schematic of Figure 3-3 shows the interconnection of the fan power.

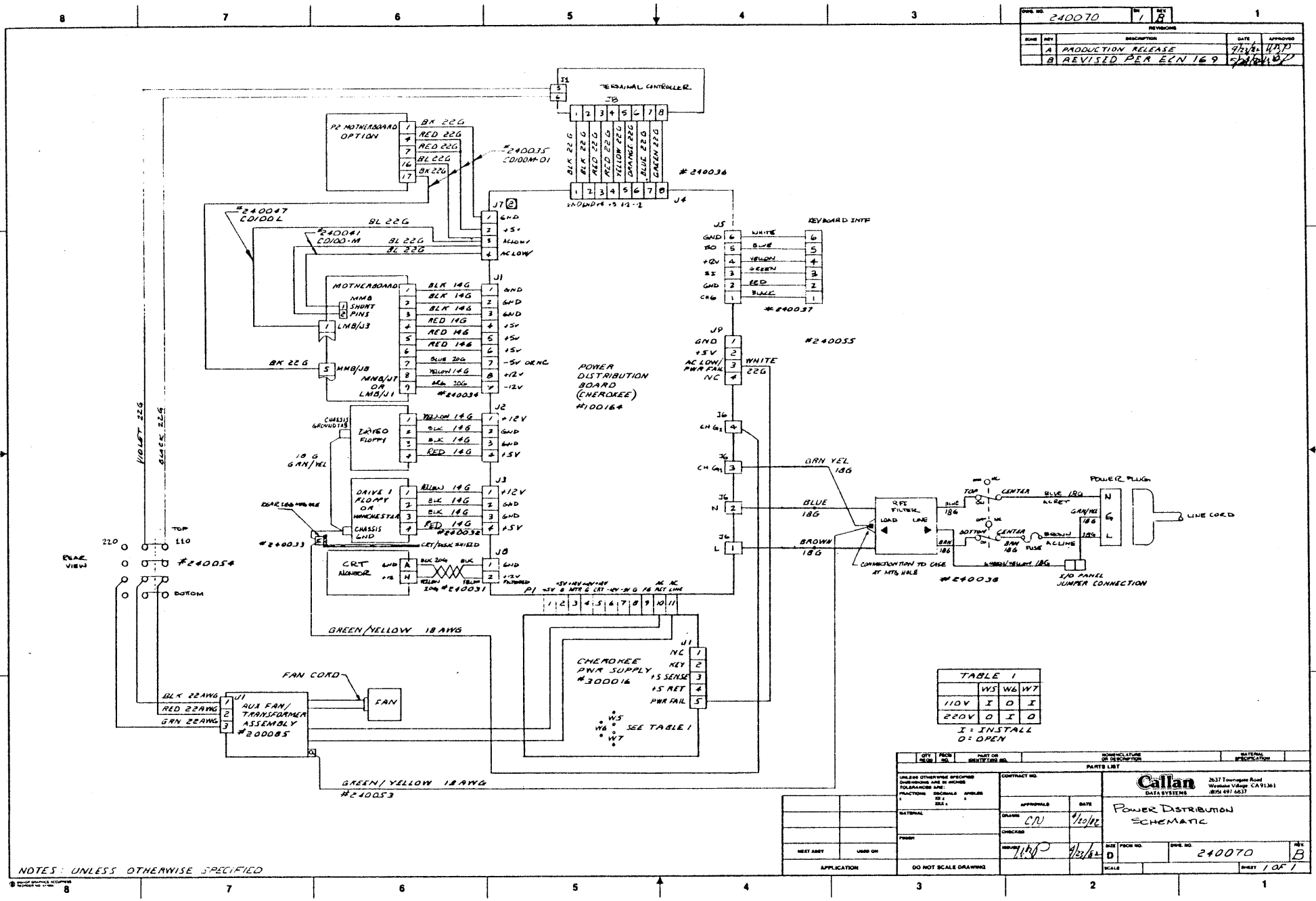

Figure 3-1
Power Distribution Schematic

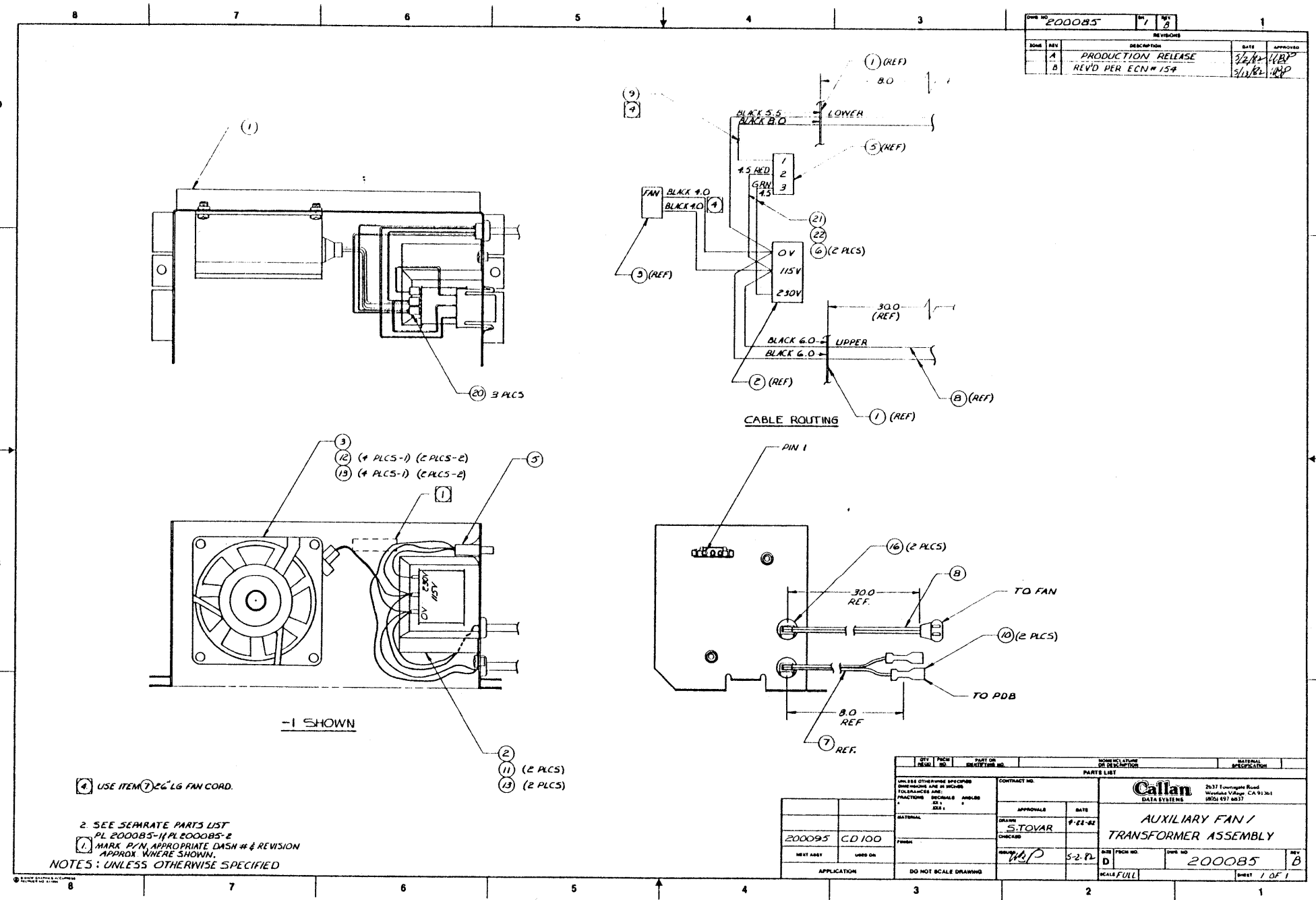

Figure 3-2

Auxiliary Fan/Transformer Assembly

	11	INDUCTION RELEASE	4/23/84	LBP
	A1	REVD, ECN 150	5/4/84	LBP

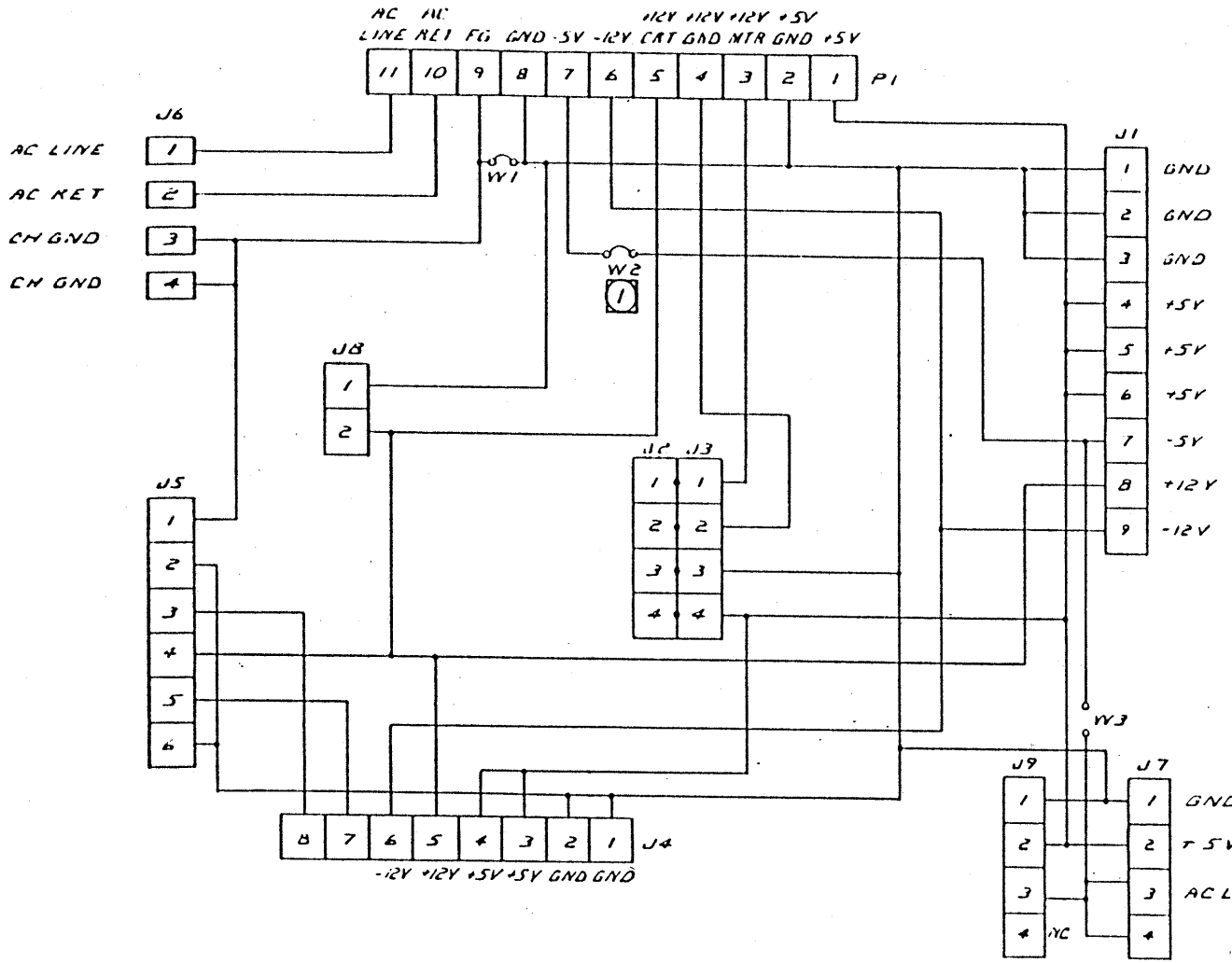

Figure 3-3
Power Distribution Board Schematic

1 W2 NOT INSTALLED IN CO100L SYSTEMS.

NOTES:

PARTS LIST

DO NOT SCALE DRAWING

APPLICATION

Callan

POWER DISTRIBUTION BOARD SCHEMATIC (CHEROKEE)

SIZE C | FSCM NO | DWG NO 100161 | A1

SCALE | SHEET 1 OF 1

3.2 AC VOLTAGE RECONFIGURATION

WARNING: THE LABEL ON THE REAR PANEL OF THE UNISTAR INDICATES THE AC VOLTAGE OPERATING REQUIREMENTS OF THE SYSTEM. ONLY TRAINED AND QUALIFIED SERVICE PERSONNEL SHOULD RECONFIGURE AC OPERATING VOLTAGES. IN THE EVENT THAT A UNIT IS RECONFIGURED, THE RATING LABEL MUST BE CHANGED. FAILURE TO DO THIS OR INCORRECT AC VOLTAGE RECONFIGURATION WILL VOID THE CALLAN WARRANTY. THE LATTER MAY CAUSE DAMAGE TO THE UNIT. TURN THE UNIT OFF AND REMOVE LINE CORD BEFORE RECONFIGURING AC VOLTAGES OR OPENING THE UNIT.

Located inside the rear access cover on the vertical bulkhead is a switch for selecting the operating voltages of the internal system AC fans. It also selects the CRT screen refresh frame rate. Place the switch in the left position for 115V/60Hz operation; place the switch in the right position for 230V/50Hz operation. To change the switch setting, remove the set screw, move the switch to the desired position then replace and secure the set screw. UNISTAR systems use a switching power supply which must be reconfigured with AC voltage selection jumpers. Open the unit to access the base area and reconfigure jumpers W5, W6, and W7 as follows: for 115V operation, install W5 and W7 and remove W6 for 230V operation, install W6 and remove W5 and W7. See Figure 3-4 for location of the jumpers on the power supply.

WARNING: Set this switch and configure power supply jumpers **PRIOR** to turning the unit on. Failure to do so damages the power supply and/or fans and voids the warranty.

JUMPER CONFIGURATION			
	W5	W6	W7
110V	I	O	I
220V	O	I	O

I = INSTALLED
O = OPEN

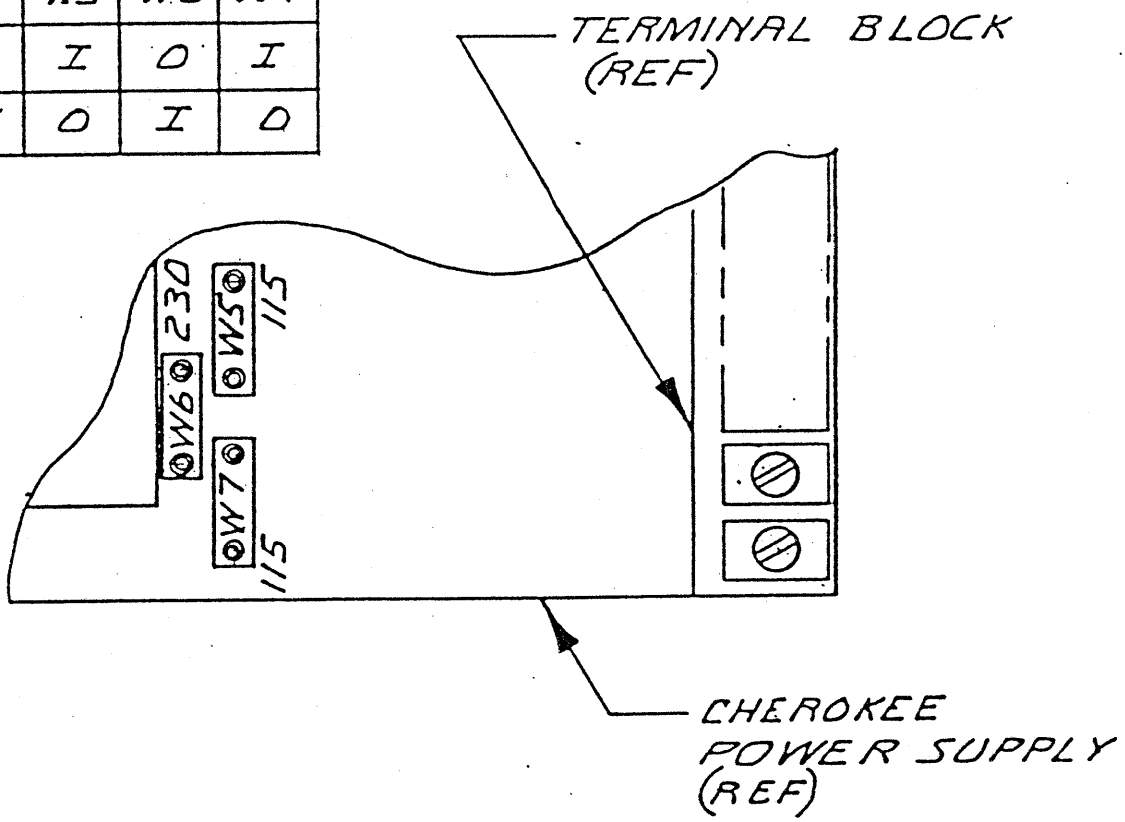

Figure 3-4
Power Supply 110V/220V Jumper Configuration

3.3 MOTHERBOARD POWER CAPACITY

The following current and power capacities are available to the Multibus/UNISTAR motherboard.

The column "UNISTAR SPARE SLOT CURRENT" defines the current available at the two spare UNISTAR slots. These currents can be used only such that the maximum additional power dissipated in the spare slots does not exceed 45 watts.

NOTICE: Failure to comply with the appropriate power or current limits voids the UNISTAR warranty.

VOLTAGE SPECIFICATIONS	MOTHERBOARD MAXIMUM CURRENT	UNISTAR SPARE SLOT CURRENT
+12 Volts ± 3.0%	2.0 Amps	1.3 Amps
+ 5 Volts ± 3.0%	21.5 Amps	8.0 Amps
-12 Volts ± 5%	2.5 Amps	1.8 Amps
- 5 Volts ± 5%	0.5 Amps	.5 Amps

CHAPTER 4 SYSTEM INITIALIZATION CHECKOUT AND SHUTDOWN

4.1 BRINGING UP THE UNISTAR SYSTEM

STEP 1: Turn the on/off switch to ON

STEP 2: Wait until the CRT screen warms up and begins to show the cursor. This takes about 30 seconds.

STEP 3: Depress the rocker switch marked "RESET". The "RESET" key is located just to the lower right of the CRT screen. Shortly after depressing the "RESET" key, the following message should appear on the CRT screen:

UniStar 68000 UNIX boot v2.2
(c) 1982 by Callan Data Systems Inc.

If the message does not appear, wait 5 seconds and depress the "RESET" again. If the message does not appear after several more depressions of the "RESET" key, then the UNISTAR is broken. The message normally appears approximately 3 seconds after release of the switch due to start up processing.

STEP 4: When the message shown in the above step is displayed, the UNISTAR UNIX system may be started up. To automatically start up the UNISTAR UNIX system, press the keyboard key marked,"RETURN". Immediately after the "RETURN" key is hit, the message shown below will appear:

w(0,0)/unix

This message shows that the Callan Data Systems UNIX Boot Monitor is loading UNIX into the UNISTAR. Loading UNIX into the UNISTAR will take about 20 seconds, during this loading process, several messages will appear, indicating such things as memory size of the UNISTAR and so on.

STEP 5: About 20 seconds after the "RETURN" was hit to load UNIX, a single line with a pound sign ('#') will appear. This indicates that UNIX is now running in the single-user mode. Since most UNIX systems will run in a multi-user mode, enter a

CONTROL-D to have UNIX begin execution of the multi-user mode. A CONTROL-D is entered by holding the "CTRL" key down while typing the "D" key.

If the single line with a pound sign does not appear, or if messages containing the word "error" appear during the UNIX loading process, then retry the entire procedure by turning off the machine and going back to STEP 1.

STEP 6: As UNIX begins execution of the multi-user mode, it will ask several questions of the user. These questions include the date and time, and whether the disk should be verified, and so on. Each question is explained. The entire time to boot UNIX for multi-user mode, including answering the questions, takes less than 2.5 minutes.

4.2 SHUTTING DOWN THE UNISTAR SYSTEM

STEP 1: Make sure that all users are either logged off the system or not actively entering UNIX commands.

STEP 2: Type in the command "shutdown". The shutdown command will shutdown UNIX from a multi-user system back to a single-user system. When the shutting down process is complete, "shutdown" will announce it as shown below(where <cr> denotes the RETURN key:

```
% shutdown <cr>
  working ....
  Shutdown complete
#
```

Once in the single-user mode, turn the power switch to OFF. NOTE: If the UNISTAR is going to be moved physically, you **MUST** perform the following steps before turning the power off.

STEP 3: This step is performed before turning the power off. It is needed **ONLY** if the UNISTAR machine is going to be physically moved. The purpose of this step is to position the arm of the Winchester disk to a "shipping zone" area so that hard shocks to the UNISTAR system do not damage the Winchester disk media. Depress the "RESET" button. Type in the following command:

```
w(0,0)ship
```

Now turn off the power immediately, do **NOT** depress"RESET" again.

CHAPTER 5 TERMINAL CONTROLLER CONFIGURATION

5.0 GENERAL INFORMATION

This section provides information necessary to configure the UNISTAR workstation's hardware options. Subsections cover configuring the terminal's RS-232C port, DIP switch settings for terminal mode control, and installation of alternate character sets. The graphics interface configuration and its use is also described.

5.1 TERMINAL RS-232C PHYSICAL INTERFACE

The UNISTAR terminal controller board provides a standard 25 pin "D" type female communication connector and circuitry per EIA Standard RS-232C. Configuration interface type "D" is used for Duplex operation with Request to Send used to indicate a non-transmit mode to the PM-68K. The one exception to the type "D" interface is that the terminal controller is not microprogrammed to respond to the Modem Ring Indicator signal (RS-232C Circuit CE).

Data transmission protocol is industry standard asynchronous start-stop protocol. One stop bit is used at baud rates above 150 baud and two bits are used at 110 baud and below.

The terminal controller is factory configured to disable use of various interchange circuits to accommodate a simpler three wire host interface with synchronization using XON/XOFF protocol. Table 5-1 summarizes thejumper option shunts for the terminal controller board. Refer to Figure 5-1 for the location of these jumper posts. The signal pinout summary for the terminal controller DB-25 RS-232C connector is given in Table 5-2. Other user options of the terminal controller are programmable by two DIP switches on the rear of the board. Table 5-3 summarizes all switch settings.

SHUNT		RS-232C INTERCHANGE CIRCUIT
SHUNT		
31-32	Enable Clear to Send from Host	(CKT CB)
31-30*	Disable Clear to Send from Host	
34-33	Enable Data Set Ready from Host	(CKT CC)
34-35*	Disable Data Set Ready from Host	
18-19	Enable Carrier Detect from Host	(CKT CF)
17-18*	Disable Carrier Detect from Host	
23-24*	Use Internal Terminal Receive Clock	
23-25	Use Receive Signal Element Timing from Host for Receive Data Clock	(CKT DD)
20-21	Use Transmitter Signal Element Timing from Host for Transmit Clock	(CKT DB)
21-22*	Use Internal Terminal Baud Clock normal.	

Note: The asteriks indicate the configuration of a standard factory delivered terminal controller.

Table 5-1
RS-232C Jumper Selection

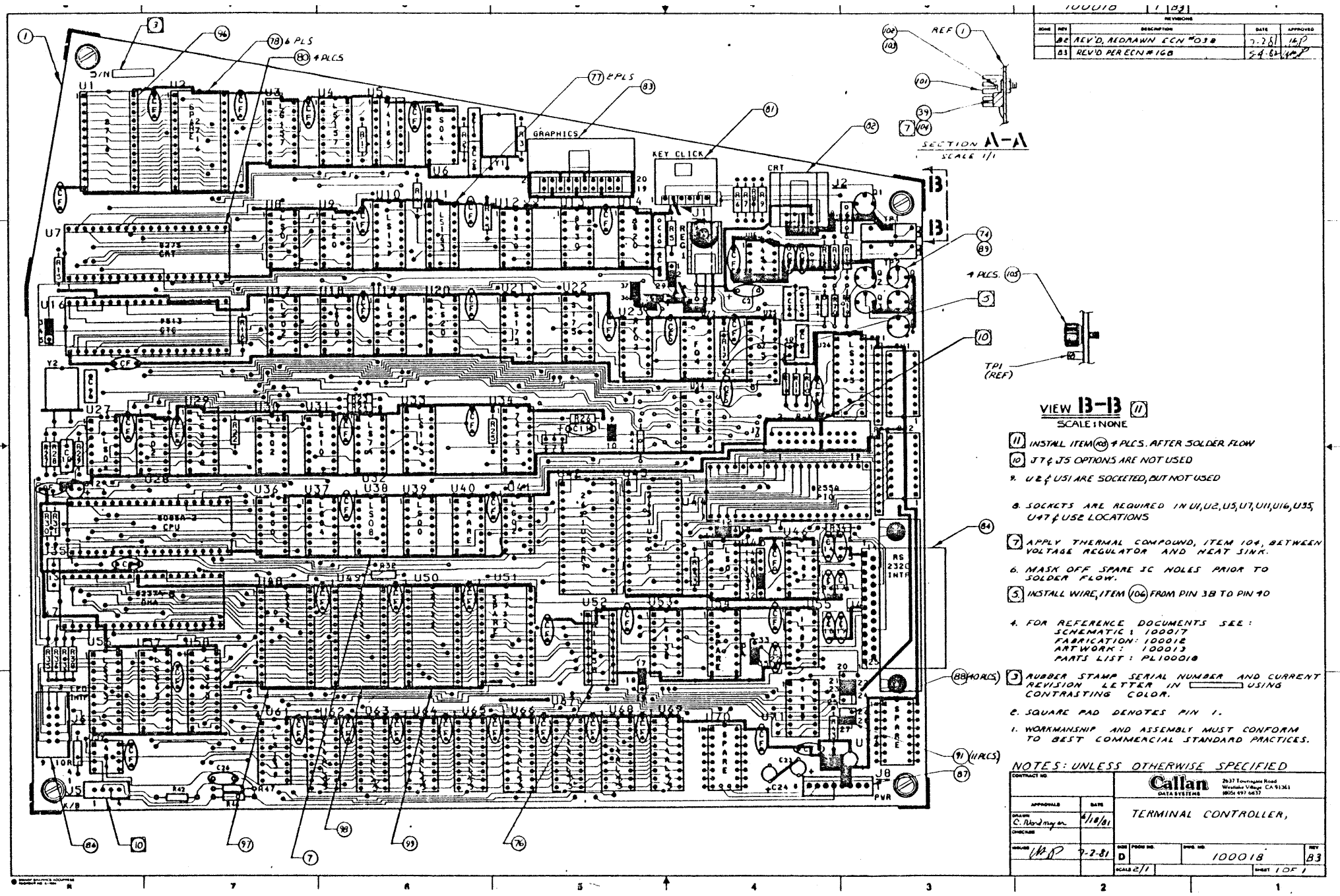

Figure 5-1
Terminal Controller Assembly

TABLE 5-2
RS-232C CONNECTOR PIN ASSIGNMENTS

SIGNAL NAMES	RS232 CIRCUIT	CONNECTOR PIN NUMBER	I/O*
Transmit Signal Element Timing.	DB	15	I
Receiver Signal Element Timing.	DD	17	I
Transmitter Clock	DA	24	O
Request to Send	CA	4	O
Data Terminal Ready	CD	20	O
Transmit Data	BA	2	O
Receive Data	BB	3	I
Clear to Send	CB	5	N/U
Data Set Ready	CC	6	N/U
Carrier Detect	CE	8	N/U
Signal Ground	AB	7	I/O
Protective Ground	AA	1	I/O

* I implys an input to the terminal controller
  O implys an output from the terminal controller

N/U = Not used

TABLE 5-3
TERMINAL CONTROLLER
REAR PANEL DIP SWITCH DEFAULT SETTINGS
FOR UNISTAR

SW1 - UPPER SWITCH BANK

SWITCH NUMBER	SWITCH NAME	OFF POSITION (LEFT)	ON POSITION (RIGHT)
1-8	Autowrap	Enabled	Disabled*
1-7	XON/XOFF	Disabled	Enabled*
1-6	New line mode	Enabled	Disabled*
1-5	Margin Bell	Enabled	Disabled*
1-4	ANSI/VT52 mode	VT52 mode	ANSI mode*
1-3	Cursor Blink	Steady Cursor	Blinking Cursor*
1-2	Cursor type	Dash Cursor	Block Cursor*
1-1	Screen mode	Reverse Video	Normal Video*

SW2 - LOWER SWITCH BANK

2-8	Local/Online	Local/Test mode	Online*
2-7	Data length	7 data bits	8 data bits*
2-6	Parity	Even Parity	Odd parity*
2-5	Parity	Process parity	Ignore parity*
2-4	Baud rate select code		
2-3	Baud rate select code		
2-2	Baud rate select code		
2-1	Baud rate select code		

BAUD RATE SELECT CODE (N=ON; F=OFF)

4 3 2 1 SW2		
N N N N	9600 BAUD*	(1 stop bit)
N N N F	7200	(1 stop bit)
N N F N	4800	(1 stop bit)
N N F F	3600	(1 stop bit)
N F N N	2400	(1 stop bit)
N F N F	2000	(1 stop bit)
N F F N	1800	(1 stop bit)
N F F F	1200	(1 stop bit)
F N N N	600	(1 stop bit)
F N N F	300	(1 stop bit)
F N F N	150	(1 stop bit)
F N F F	134.5	(1 stop bit)
F F N N	110	(2 stop bits)
F F N F	75	(2 stop bits)
F F F N	50	(2 stop bits)
F F F F	Not used	

* INDICATES THE STANDARD UNISTAR SETTING

5.2 ALTERNATE CHARACTER ROM GENERATION

An alternate character set can be incorporated in the UNISTAR terminal controller by installation of a 2716 EPROM or equivalent device in IC location U42 on the terminal controller board. Software driven commands are available for invoking the alternate character sets incorporated into this EPROM, the alternate character ROM standard character set and the alternate character ROM special Graphics character set. Up to 128 characters can be included in the alternate character ROM. Sixteen bytes are stored in sequence for each character to define its character font (see figure 5-1) A seven bit binary code is used to address each character as it is displayed in the same way that ASCII character codes are used to address characters in the standard set EPROM. Therefore, the seven bit character code is used on address lines A4-A10 of the 2716 where A4 is the least significant bit of the character code sent to the terminal. Address lines A0-A3 are used to select the rows of the character matrix as each character is displayed.

Each byte stored in the EPROM character generator represents a row of the character matrix. The most significant bit position of each byte (bit 7) in the EPROM is used as a control bit for the video logic to support line graphics characters. This bit when true expands bits 0 and 6 into their adjacent inter-character spaces thus allowing continuous lines between characters. The displayable character matrix is 7 x 13 bits (60 Hz refresh) or 7 x 15 (50 Hz refresh). Refer to Figure 5-2 for an example of the character matrix format.

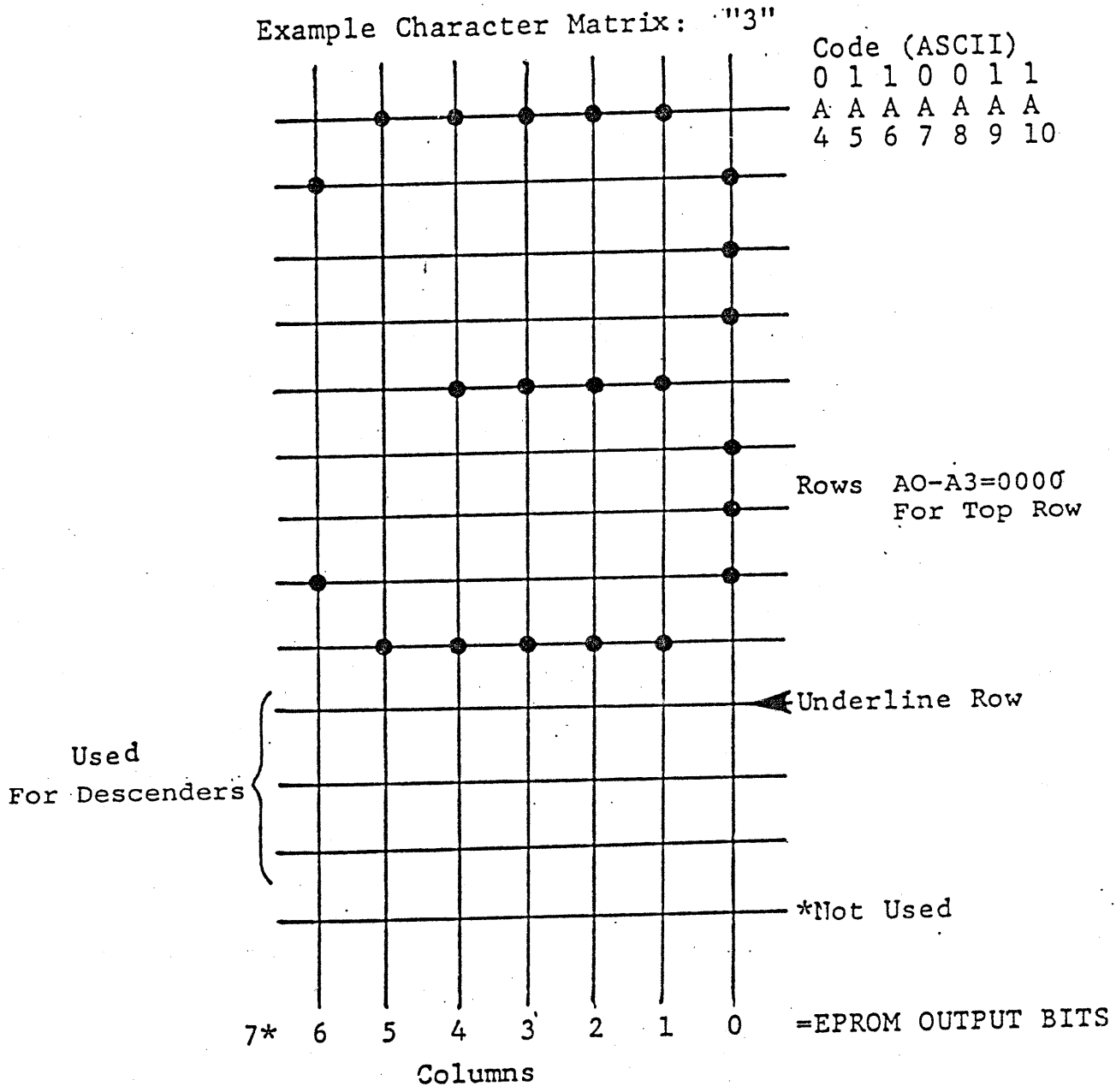

Figure 5-2
Character Matrix Format

* Bit 7 when true enables display of bit 0 and/or bit 6 in the intercharacter space if either is true.

5.3 TERMINAL CONTROLLER GRAPHICS INTERFACE

The UNISTAR terminal controller incorporates a graphics interface which permits field or factory installation of a graphics display controller. Located at the top of the terminal controller and labeled "graphics", the 20 pin interface provides basic binary signals to the graphics controller, which permit it to operate in synchronization with the alphanumeric terminal controller. The graphics controller also uses the cable to return video display data and intensity control information to the terminal controller which then uses it to drive the video output electronics and CRT.

The normal jumper configuration of the terminal controller without graphics interface is:

Jumper	Status:
2-29	IN
36-37	IN

To install the graphics controller, the jumpers above are removed and DS8830's (P/N 404-8830) are installed in U12 and U13 and a DS8820A (P/N 404-8820) is installed in U14. These IC's are provided with the graphics field installation kit as well as a 20 conductor ribbon cable which connects the graphics interface connector to the Multibus resident graphics controller.

CHAPTER 6 DISK UNIT SPECIFICATIONS AND CONFIGURATION

6.0 GENERAL INFORMATION

The Callan UNISTAR contains two integral disk units; a 5 1/4" minifloppy and a 5 1/4" Winchester. The characteristics and specifications of these two devices are provided in this chapter. Format information, where applicable, is provided in the System Software Configuration chapter. For disk unit service information, please refer to the Service Manual.

6.1 MINIFLOPPY SPECIFICATIONS

Media*: Certified for double sided double density reading. The approved source being Verbatim P/N: MD 557-01-18239
Note: Callan Data Systems does not warranty drive for use with non-approved media.
Tracks per inch: 96
Tracks per side: 77
Seek Time: 3 msec/track
Head Settling time: 15 msec
Error Rates: 1 per 10^9 (recoverable)
1 per 10^{12} (non-recoverable)
1 per 10^6 (seeks)
Head Life: 20,000 hours
Media Life: 3.6 X 10^6 passes per track
Disk Speed: 300 rpm $\pm$ 1.5% (long term)
Instantaneous speed variation: $\pm$ 3.0%
Start/Stop Time: 250/150 mSec (maximum)
Transfer Rate: 250 Kbytes/sec
Recording Mode: MFM
Power: +12 vdc $\pm$ 0.6v 900 ma AVG
+ 5 vdc $\pm$ 0.25v 600 ma AVG
Vendor: Tandon TM-100-4 or equivalent

*NOTE: Callan Data Systems does not warranty drive for use with non-approved media.

6.2 MINIFLOPPY DRIVE CONFIGURATION

The minifloppy disk drive units are capable of being configured to operate in a variety of modes depending upon a shunt block contained upon the drive electronics circuit board. The shunt options are described as follows. (Note that "*" denotes standard factory installed shunts for the UNISTAR system).

Shunt Pins (1E)	Function	
1 to 16	HS	Drive Motor from Select
* 2 to 15	NDS0	Drive 0 Enable
3 to 14	NDS1	Drive 1 Enable
4 to 13	NDS2	Drive 2 Enable
5 to 12	NDS3	Drive 3 Enable
6 to 11	MX	Daisy Chain Cable Disable
7 to 10	SPARE	Not Used
* 8 to 9	HM	Drive Motor from Cable

The TM-100 drive is provided with the capability of terminating input lines to the drive on the lines:

Motor On, Direction, Step, Write Data, Write Gate, and Side Select

If the TM-104 is used in a multiple drive setup then the termination network at location 2F on the circuit board must be removed from all units except the drive on the extreme end of the cable. For the standard UNISTAR in a single floppy installation the termination network is installed. The termination network is a 150 ohm pullup resistor for each line.

Figure 6-1 on the following page shows the configuration of the TM-104 drive electronics circuit board.

6.3 WINCHESTER SPECIFICATIONS

Capacity	
Unformatted	
Per Drive	12.76 Megabytes
Per Surface	3.19 Megabytes
Per Track	10416 Bytes
Formatted *	
Per Drive	10.0 Megabytes
Per Surface	2.5 Megabytes
Per Track	8192 Bytes
Per Sector	256 Bytes
Sectors per track	32

*With vendor standard formatting

	B	REV'D PER ECN 189	2/24/83

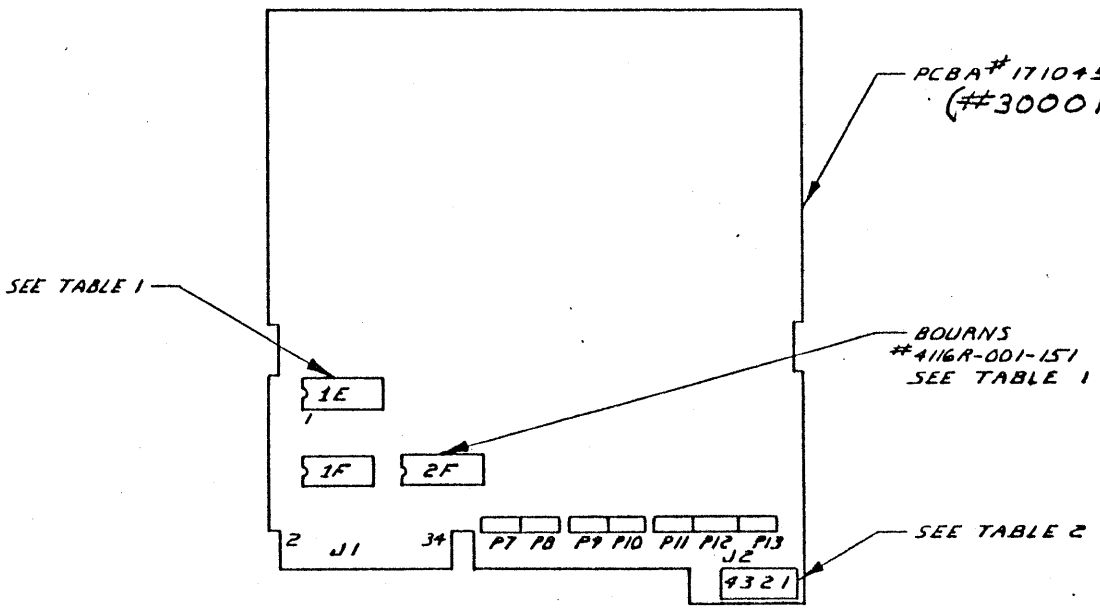

Figure 6-1
Floppy Disk Configuration Reference

TABLE 2	
J2 PIN	VOLTAGE
1	+12 VDC
2	GND
3	GND
4	+5 VDC

USED ON	APPLICATION	1E SHUNTS INSTALLED	2F RESISTOR PACK
-62	DUAL DRIVE - DRIVE 1	14 9 / 3 8	INSTALL
-62	DUAL DRIVE - DRIVE Ø	15 9 / 2 8	NOT USED
-71 OR -72	SINGLE DRIVE - DRIVE Ø	15 9 / 2 8	INSTALL

TABLE 1

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DRAWN C. Nordmeyer	1/19/82
CHECKED	
ISSUED R.B. Kruse	1/19/82

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION | DO NOT SCALE DRAWING

Callan DATA SYSTEMS
2637 Townsgate Road
Westlake Village CA 91361
(805) 497-6537

TANDON TM100 - 96TPI
CONFIGURATION

SIZE C | FSCM NO. | DWG. NO. 321006 | REV. B

SCALE FULL | SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO. A1-1663

4 3 2 1

WINCHESTER SPECIFICATIONS (Cont.)

Transfer Rate	5.0Mbits/sec
Average Latency	8.33 msec
Access Time	
Track to Track	3ms
Average	85ms**
Maximum	205ms**
Setting Time	15ms

**using burst mode (including settling)

Functional Specifications:

Rotational speed	3600 rpm ±.1%
Recording density	9074 bpi
Flux density	9074 fci
Track density	345 tpi
Cylinders	306
Tracks	1224
R/W Heads	4
Disks	2

Max Accoustic Output: 50 DBA

Shock
- Operating: 10G
- Non-operating: 20G

DC Power Requirements
- +12V ± 5%, 1.8A typical, 4.5A max (at power on)
- +5V ± 5%,.7A typical, 1.0A max
- -12V ± 5V Max Ripple = 50mV P-P

Error Rates:
- Soft read errors. . . . . 1 per 10^{10} bits read
- Hard read errors* . . . . 1 per 10^{12} bits read
- Seek errors . . . . . 1 per 10^{6} seek
- * Not recoverable within 16 retries

Vendor: Seagate ST412 or Equivalent.

6.4 WINCHESTER DRIVE CONFIGURATION

The Seagate ST-412 Winchester disk drive is capable of being configured in various ways depending upon a shunt block contained upon the drive electronics board. The shunt position functions are described as follows with an "*" indicating the standard installed shunt configuration for the UNISTAR system.

Shunt Pins	Function
1 to 16	Radial Enable
* 2 to 15	Defeat Auto Recal
* 3 to 14	Always Installed
* 4 to 13	Not Used
5 to 12	DS4 Drive Unit 3 Enable
6 to 11	DS3 Drive Unit 2 Enable
7 to 10	DS2 Drive Unit 1 Enable
* 8 to 9	DS1 Drive Unit 0 Enable

The ST-412 drive is provided with the capability of terminating input lines to the drive on these lines:

Reduced Write Current, Write Gate,
Head Address Lines, Step, and Direction

If the ST-412 is used in a multiple drive setup then the terminator network at location 6F on the circuit board must be removed from all units except the drive on the extreme end of the cable. For the standard UNISTAR in a single Winchester installation the terminator network is installed. The terminator network is a 220/330 ohm network for each line.

Figure 6-2 on the following page shows the configuration of the ST-412 drive electronics circuit board.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED
		A	PROD REL ERN 136	8-23-82	

Figure 6-2
Winchester Configuration Reference

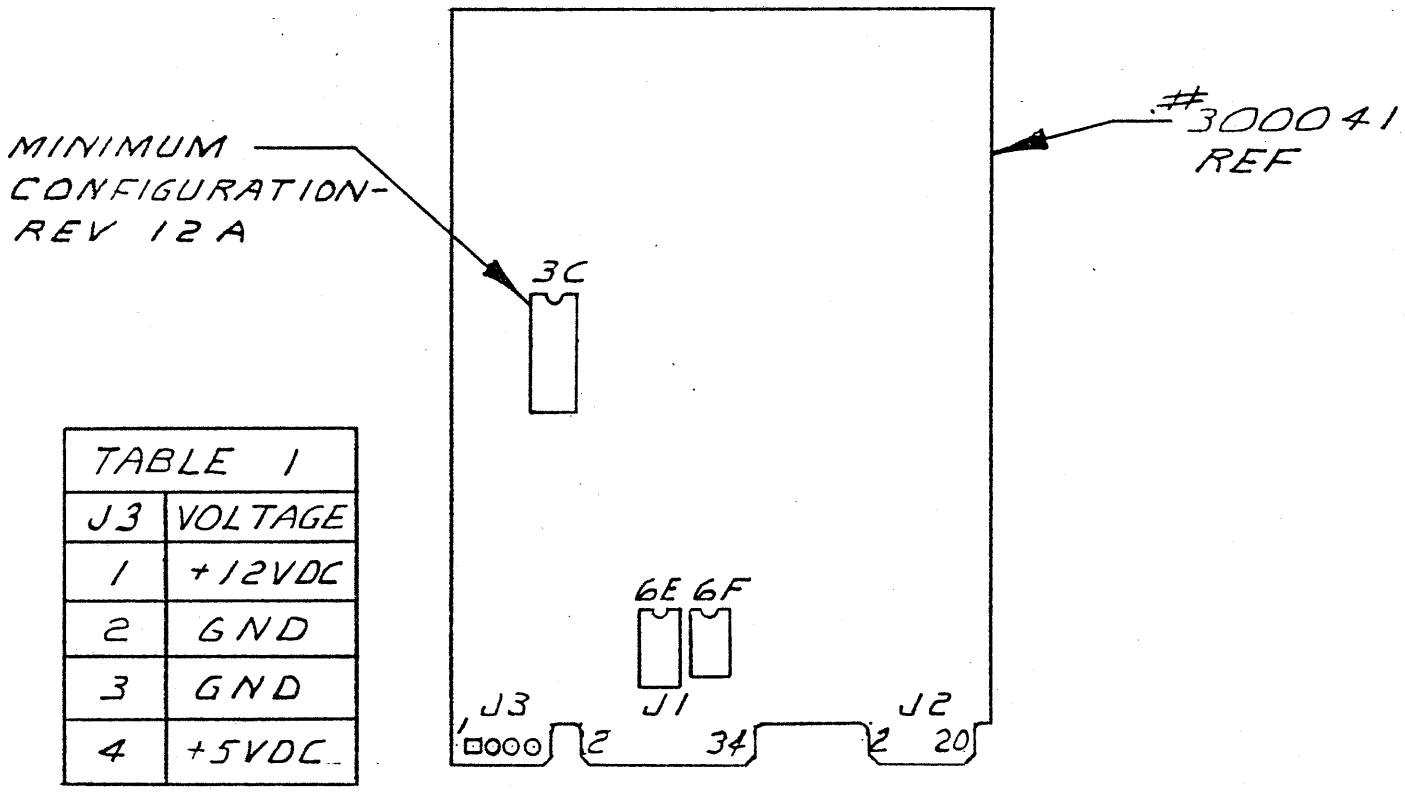

TABLE 1	
J3	VOLTAGE
1	+12VDC
2	GND
3	GND
4	+5VDC

USED ON	APPLICATION	6E SHUNT INSTALL	6F RES PACK
	DUAL DRV-DRV 1	15 14 13 10 / 2 3 4 7	INSTALL
	DUAL DRV-DRV 0	15 14 13 9 / 2 3 4 8	NOT USED
-423	SNGL DRV-DRV 0	15 14 13 9 / 2 3 4 8	INSTALL

TABLE 2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± ± .XXX ±	CONTRACT NO.	Callan DATA SYSTEMS	2637 Townsgate Road Westlake Village, CA 91361 (805) 497-6837
MATERIAL	APPROVALS / DRAWN C Nordmeyer	DATE 8/23/82	SEAGATE ST412 PCBA CONFIGURATION
FINISH	CHECKED M Kuo	8/27/82	SIZE A / FSCM NO. / DWG. NO. 321005 / REV. A
DO NOT SCALE DRAWING	ISSUED M Kuo	8/27/82	SCALE 1/2 / SHEET 1 OF 1

CHAPTER 7 I/O PANEL CONNECTOR INFORMATION

Figure 7-1 illustrates the UNISTAR I/O panel configuration. The panel supports the following I/O types.

. NINE RS-232C female D type communications connectors. One is cabled to the auxillary communication port on the PM-68KCPU board. The others are optionally cabled to an eight channel communication board on UNISTAR 200 systems (Multi-user).

. One Ethernet compatible 15 pin D connector Cinch type DA 51220-1 or equivalent cutout to be used for Ethernet options.

. One parallel printer, AMP 'champ' latch connector P/N 552834-7, cutout. This cutoutprovides for a future parallel printer.

. Two telephone cable, AMP modular jack P/N 520250-3, direct connect connector cutoutsto support a future integrated modem option.

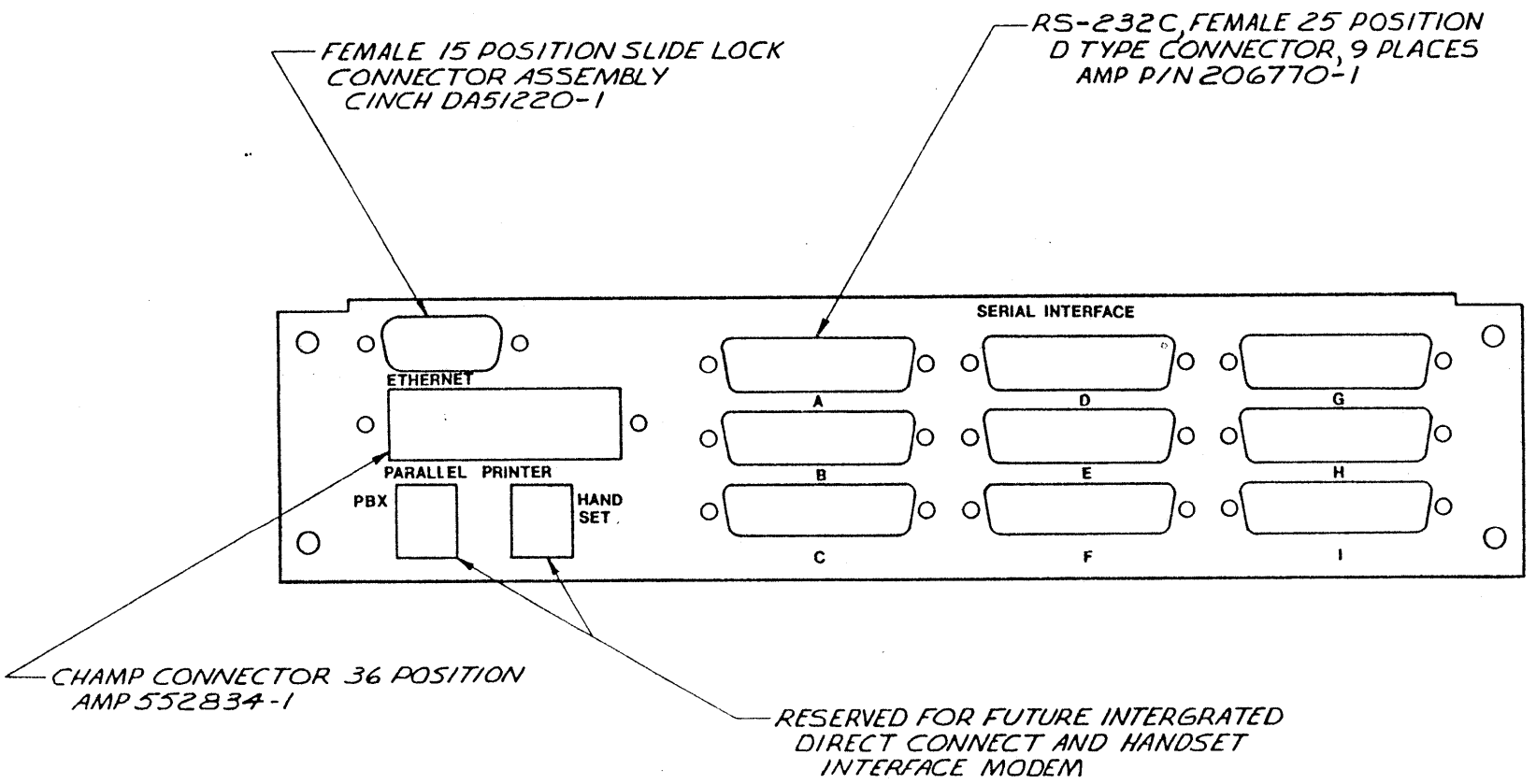

FIGURE 7-1

UNISTAR IO PANEL DETAIL

CHAPTER 8 SYSTEM BOARD CONFIGURATION

8.0 PRINTED CIRCUIT BOARD ASSEMBLIES, SWITCH AND SHUNT CONFIGURATIONS

This section provides a description of the factory installed configurations for all Multibus PCBAs in the UNISTAR Multibus motherboard (Ref: Section 9 for individual PCBA card locations).

8.1 CALLAN -83 FDC, FLEXIBLE DISK CONTROLLER

Configuration of the Callan -83 FDC Flexible Disk Controller PCBA for operation with 68000 UNIX I/O, with an I/O base address equal to 100 Hex (16 bit decode) and interrupt level 3 (Ref: Dwg.No. 100096, Floppy Disk Controller Board Configuration and Dwg.No. 304004, Callan Data System Floppy Disk Controller Reference Manual).

Address Decode Switchs (SW1 and SW2):

Switch	Designation	Position
SW1-1	(not used)	-
SW1-2	(not used)	-
SW1-3	(not used)	-
SW1-4	8B/16B	Closed
SW1-5	(not used)	-
SW1-6	A5	Closed
SW1-7	A6	Closed
SW1-8	A7	Closed
SW2-1	A8	Open
SW2-2	A9	Closed
SW2-3	AA	Closed
SW2-4	AB	Closed
SW2-5	AC	Closed
SW2-6	AD	Closed
SW2-7	AE	Closed
SW2-8	AF	Closed

Shunt Designation	Position	Function
1-2-3	1 to 2	Software Program Mode
4-5-6	4 to 5	Software Program Mode
LOW	Installed	Low Current Enable
TSD	Installed	Two Sided Enable
MHEAD	Installed	Mini Floppy Head Enable
RDY-D	Installed	Ready From Drive Enable
RDY-A	Installed	Floppy Always Ready Enable
FLT	Removed	Fault Input Disabled
FRST	Installed	Fault Reset Enabled
I0	Removed	Interrupt 0 Disabled
I1	Removed	Interrupt 1 Disabled
I2	Removed	Interrupt 2 Disabled
I3	Installed	Interrupt 3 Enabled
I4	Removed	Interrupt 4 Disabled
I5	Removed	Interrupt 5 Disabled
I6	Removed	Interrupt 6 Disabled
I7	Removed	Interrupt 7 Disabled
BPRO	Removed	Bus Priority Out Disabled

8.2 MSC-9205C, WINCHESTER DISK CONTROLLER

Configuration of the MSC-9205C Winchester Disk Controller PCBA for operation with 68000 UNIX I/O,with an I/O base address equal to 080 Hex (16 bits provided from CPU but only 8-bits decoded by controller) and interrupt level 5 (Ref: Dwg.No. MSC-9205C PCBA Configuration and Dwg.No. 304012, MSC-9205 Disk Controller Product Specification). As supplied, the MSC-9205C PCBA is configured for a disk drive with four heads, 512 byte sectors, 17 sectors per track, with parallel bus priority.

Shunt Designation	Position	Function
W1	Installed	Reset AM Enabled
W2	Installed	Increase Precomp Enabled
W3	Installed	Write AM Enabled
W4	Removed	BPRO Disabled
W5	Removed	I/O Base Address
W6	Installed	I/O Base Address
W7	Installed	I/O Base Address
W8	Removed	I/O Base Address
W9	Removed	I/O Base Address
W10	Removed	I/O Base Address
W11	Removed	(not used)
W12	Installed	512 Byte Sector Enabled
W13	Removed	(not used)
W14	Installed	Four Heads Enabled
W15	Removed	Four Heads Enabled
W16	Removed	(not used)
W17	Removed	512 Byte Sector Enabled
W18	Removed	(not used)
W19	Removed	Interrupt 0 (not used)
W20	Removed	Interrupt 1 (not used)
W21	Removed	Interrupt 2 (not used)
W22	Removed	Interrupt 3 (not used)
W23	Removed	Interrupt 4 (not used)
W24	Installed	Interrupt 5 (used)
W25	Removed	Interrupt 6 (not used)
W26	Removed	Interrupt 7 (not used)
W27	Installed	(not used)

8.3 MM-8086D/64 RANDOM ACCESS MEMORY

Configuration for the UNISTAR Multibus RAM is for 64 Kilobytes (32 Kilowords) with a Multibus base address of zero to FFFF Hex that is mapped by the PM-68K CPU to address 100000 Hex (Ref: Dwg.No. 321003, MM8086D Memory PCBA Configuration and Dwg.No. 304039, MM-8086D/64 RAM Manual). Addressing switches and shunt installations are as follows:

Address Decode Switchs (SW1 and SW2):

Switch	Designation	Position
SW1-1	Upper Limit 1	Closed
SW1-2	Upper Limit 2	Closed
SW1-3	Upper Limit 3	Closed
SW1-4	Upper Limit 4	Closed
SW1-5	Upper Limit 5	Open
SW1-6	Upper Limit 6	Open
SW1-7	Upper Limit 7	Open
SW1-8	Upper Limit 8	Open
SW2-1	Lower Limit 1	Open
SW2-2	Lower Limit 2	Open
SW2-3	Lower Limit 3	Open
SW2-4	Lower Limit 4	Open
SW2-5	Lower Limit 5	Open
SW2-6	Lower Limit 6	Open
SW2-7	Lower Limit 7	Open
SW2-8	Lower Limit 8	Open

Shunt Designation	Position	Function
E1-E2-E3	E2 to E3	Delay XACK/
E4-E5-E6	E4 to E5	+5 VDC for 64K DRAM
E7-E8-E9	E8 to E9	Delay Line Pin 11 RDCYC CLK
E10-E11-E12	E11 to E12	64K DRAM Type
E13-E14-E15	E14 to E15	64K DRAM Type
E16 thru E20	(all open)	Extended Address Selection
E21-E22-E23	E22 to E23	No Delay on MWTC (write)
Parity Error (Pad)	J1-37	Parity Error to INT4/

8.4 PM-68K, 68000 CPU

Configuration settings for the PM-68K 68000 CPU PCBA that are required to run 68000 UNIX I/O utilizing interrupt level 5 for the USART ('wire-or' with MSC-9205 interrupt 5) and interrupt level 6 for timer channel #2 (Ref: Dwg.No. 304041, PM-68K CPU Manual), is as follows:

Shunt Designation	Position	Function
J100 1 thru 8	1 to 3	Port B RS-423 RDATA DTE
J100 1 thru 8	2 to 4	Port B RS-423 TDATA DTE
J100 1 thru 8	7 to 8	A12 to 2732 EPROM pin 23
J800 1 thru 8	1 to 2	INT6/Timer #2 Interrupt
J800 1 thru 8	3 to 4	INT5/USART Interrupt
J9011 thru 10	1 to 2	Initialize Reset (receive)
J901 1 thru 10	5 to 6	Bus Clock (master)
J901 1 thru 10	9 to 10	Constant Clock (master)
J902 1 thru 16	5 to 6	Interrupt 5 (MSC-9205C)
J902 1 thru 16	7 to 8	Interrupt 4 (Memory Parity Er
J902 1 thru 16	9 to 10	Interrupt 3 (Callan -83 FDC)
J902 1 thru 16	11 to 12	Interrupt 2 (spare)
J902 1 thru 16	13 to 14	Interrupt 1 (spare)

CHAPTER 9 MULTIBUS MOTHERBOARD CONFIGURATION GUIDE

9.0 INTRODUCTION

This section provides a description of user configurable options available on the UNISTAR Multibus Motherboard. User options are configured by the installation of shunts or by wirewrap. Options affect bus arbitration and the use of the front panel reset and interrupt switches. For further information regarding operation and use of the Multibus refer to Intel document order number 98000683.

9.1 MULTIBUS MOTHERBOARD AND PCBA CONFIGURATION

The physical location of boards installed in the Multibus motherboard using the standard factory configured parallel bus arbitration scheme (see section 9.3), is as follows: (Note that J6 is located toward the rear connector panel of the UNISTAR Unit).

Connector	PCBA
J1	(spare)
J2	(spare)
J3	Callan -83 FDC, Disk Controller
J4	PM-68K, 68000 CPU
J5	MM-8086D/64, 64 Kilobyte RAM
J6	MSC-9205C, Disk Controller

9.2 SHUNT CONFIGURATION

Shuntconfiguration for the Multibus motherboard is factory installed for parallel priority bus arbitration, front panel interrupt disabled, an I/O address of 07FF Hex (status on DATA0), and with power supply 'low power sense' disabled, as follows:

Shunt Designation	Position	Function
1-2	1 to 2	(not used; Power Supply INIT/)
5	Removed	(not used; PINTR/ to INT6/)
6	Removed	(not used; PINTR/ to INT7/)
7	Removed	(not used; PINTR/ to INT4/)
8	Removed	(not used; PINTR/ to INT5/)
9	Removed	(not used; PINTR/ to INT2/)
10	Removed	(not used; PINTR/ to INT3/)
11	Removed	(not used; PINTR/ to INT0/)
12	Removed	(not used; PINTR/ to INT1/)
13-14	Installed	INT Switch Status DAT0/ Sense
15-16	Installed	Backplane I/O Address Enable
A-B-C	B to C	J1 BPRN/ Parallel
D-E-F	E to F	J2 BPRN/ Parallel
G-H-I	H to I	J3 BPRN/ Parallel
J-K-L	K to L	J4 BPRN/ Parallel
M-N-O	N to O	J5 BPRN/ Parallel
P-Q-R	Q to R	J6 BPRN/ Parallel
A0	Installed	I/O Address 0
A1	Installed	I/O Address 1
A2	Installed	I/O Address 2
A3	Installed	I/O Address 3
A4	Installed	I/O Address 4
A5	Installed	I/O Address 5
A6	Installed	I/O Address 6
A7	Installed	I/O Address 7
A8	Installed	I/O Address 8
A9	Installed	I/O Address 9
AA	Installed	I/O Address A
AB	Removed	I/O Address B
AC	Removed	I/O Address C
AD	Removed	I/O Address D
AE	Removed	I/O Address E
AF	Removed	I/O Address F

9.3 BUS ARBITRATION OPTIONS

For general information to the purchaser and user of the UNISTAR unit, the following section will describe the bus arbitration options available for the Multibus Motherboard. Each card slot has an assigned priority ranking for bus use arbitration by the various bus master boards plugged into the card cage. Two arbitration resolution schemes are supported by the UNISTAR. A serial scheme, permitting up to three (3) bus masters, is supported where the Motherboard provides the chaining of the BPRO/ to BPRN/ signals between adjacent card slots. The card slots are ordered in priority from J1 (highest) to J6 (lowest) in decreasing serial priority order toward the rear of the unit. The highest priority module must have its BPRN/ signal input on bus connector pin number 15 grounded to assert a continuously active level.

This level may be asserted by insertion of a shunt between two pins behind the connector. (For J1 the posts are located ahead of the connector to the right of the posts for J2. Also in the serial scheme, each card slot must propogate the signal daisy chain along the card cage, either through the bus acquire logic of a bus master card in the slot or hard wired through a slave type of board. A slot may be left empty by installing an insulated wire plug jumper across the empty slot between the middle posts on either side of the connector. The circuit board modulesinstalled in a serial bus scheme must have the BPRO/ signal enabled out to the P1 jumper post option on a Multibus compatible bus master PCBA. Some boards have an optional jumper post option to ground the BPRN/ priority input signal right on the board as opposed to on the motherboard. Jumpers of this type may be used in the serial scheme only if the module is the highest priority.

For system configurations where more than three bus masters may be required, the motherboard may be setup to do parallel bus arbitration. Here all six (6) card slots (maintaining the same J1 to J6 priority order as above) are arbitrated by routing the BREQ/ signals, pin #18, of each connector to an encoder/decoder logic network upon the motherboard. The decoder provides the "grant" signal to the highest priority requesting bus master via the BPRN/ line, pin #15. Each of the six (6) card slots has its own grant line from the logic network that is routed to the individual card slots through the third jumper post (away from the fan) between each of the connectors. To utilize the parallel bus arbitration scheme. two logic integrated circuits must be installed upon the motherboard. Socket position U11, nearest the small black signal cable, must contain a P/N 715-4138, and U10 closer to the card cage must contain a P/N 700-4148. On both cases the pin one end of the IC's is away from the card cage. If parallel arbitration is used, it is extremely important that BPRN/ ground shunts be removed from all master boards that use them.

The chart on the following page shows the nominal shunt locations for both serial arbitration, J2 as highest priority, and for parallel arbitration.

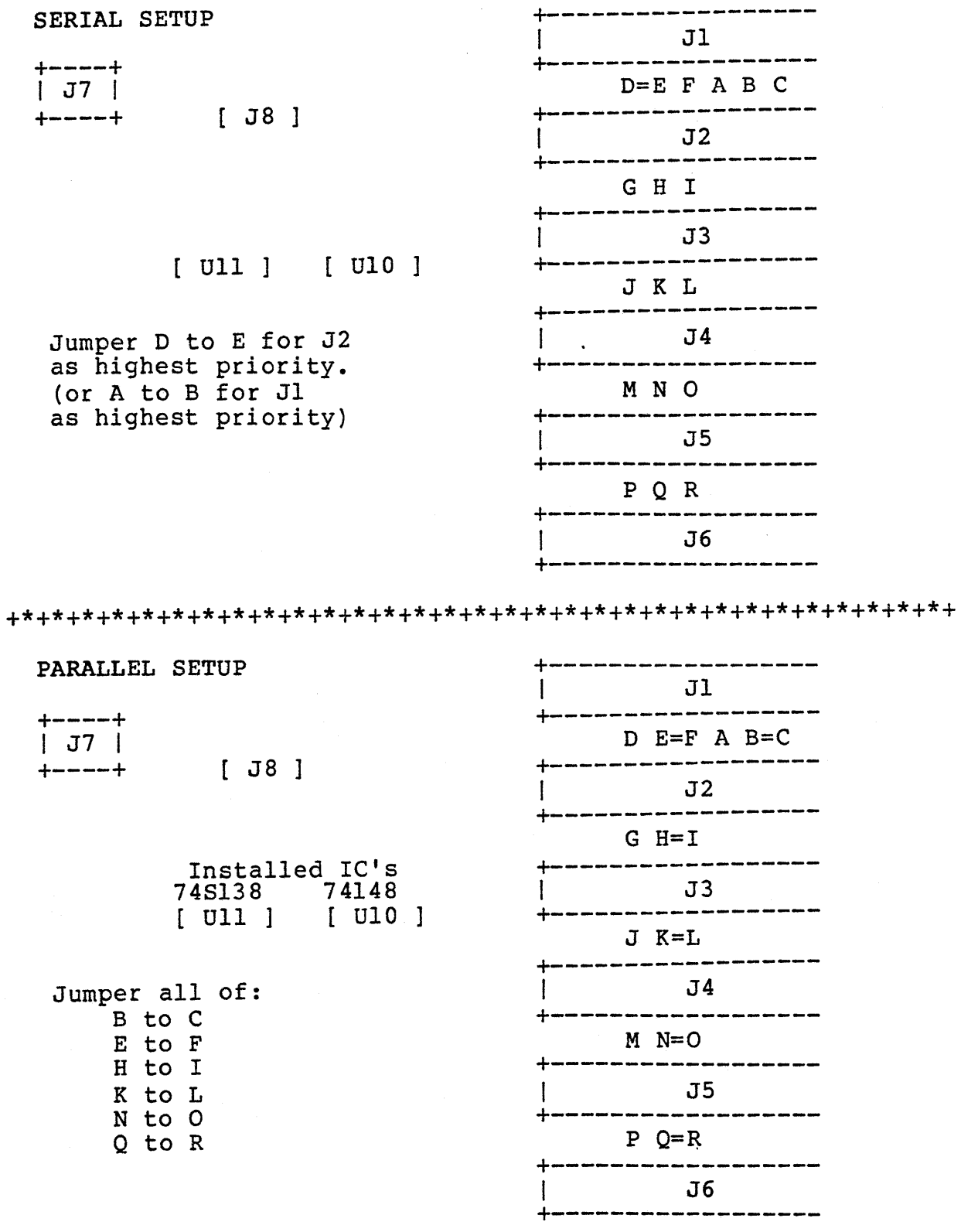

Figure 9-1
Motherboard Bus Arbitration Examples

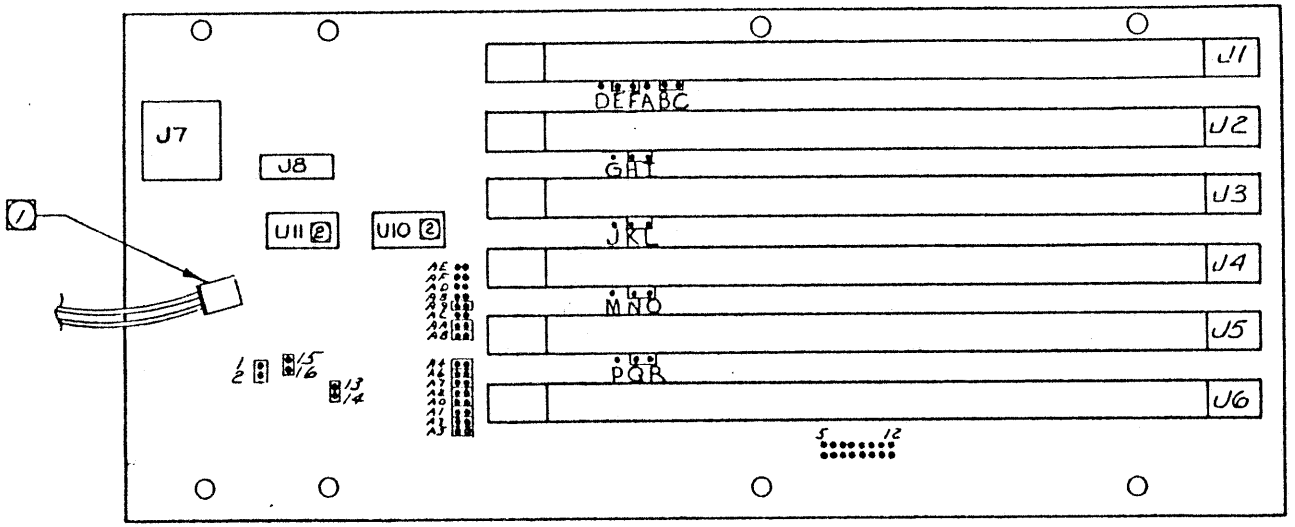

Figure 9-2
Multibus Motherboard Codfiguration

SHUNT CONFIGURATION TABLE

I = INSTALLED
O = OPEN

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I

1	2	5	6	7	8	9	10	11	12	13	14	15	16	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF
I	O	O	O	O	O	O	O	O	O	I		I		I	I	I	I	I	I	I	I	I	I	I	O	O	O	O	O

(1)

IO ADDRESS = 07FFH

(1) AUTO RESET CABLE ASSEMBLY (P/N 240041) TO FREE HANG. POSTS 1 AND 2 TO BE JUMPERED WITH SHUNT PLUG.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES °

CONTRACT NO

APPROVALS	DATE
DRAWN J. TOVAR	7-29-82
CHECKED [illegible]	
ISSUED [illegible]	8-17-82

MATERIAL

FINISH

NEXT ASSY | USED ON

UNISTAR

APPLICATION

DO NOT SCALE DRAWING

Callan DATA SYSTEMS

CDIOOM-423 MULTIBUS MOTHERBOARD CONFIGURATION

SIZE C | FSCM NO. | DWG. NO. 100066 | REV. A

SCALE NONE | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A11053

4 3 2 1

9.4 RESET SWITCH LOGIC

The UNISTAR System Workstation provides a front panel switch which may be used to reset boards installed in the backplane. Debounce logic and drivers are provided on the Motherboard. A factory installed shunt between posts labeled "1" and "2" connects the reset signal to the INIT/Spare signal on the backplane (initialization signal). The shunt can be removed to disable the reset switch.

The standard factory configured UNISTAR system has jumper 1 to 2 installed to permit system initialization from the front panel.

9.5 INTERRUPT SWITCH LOGIC CONFIGURATION

The front panel Interrupt switch can be configured to provide a NON-BUS VECTORED type of interrupt to the Multibus system using any of the eight Multibus interrupt request lines. It can be further configuredto respond to an 8 or 16 bit I/O address for clearing or reading of the Interrupt request flip flop.

Performing anI/O write cycle to the configured interruptI/O address port will clear the interrupt flip flop after it has been set by the leading edge of the interrupt switch signal. Reading the same address will allow the processor to read the status of the interrupt flip-flop in the least significant data bit. Note: The I/O address is set at the factory to 16-bit 07FF Hex.

Note: The Interrupt logic for the interrupt switch is not reset on power up. Therefore, in applications which use this switch, it is recommended that software clear the interrupt request as part to its intialization.

Option posts for the interrupt logic are defined as follows. Refer to Figure 9-2 for location on the Motherboard PCB. The factory configured Multibus motherboard is not delivered with any interrupt level selection jumper installed. The user may easily select an appropiate jumper shunt from the rear of the UNISTAR System.

POST(S) LABEL	FUNCTION
13-14	Connects the Interrupt flip-flop to data bus bit line DAT0/ to allow the CPU to read its value.

POST(S) LABEL	FUNCTION
15-16	Connects the upper 8 address bit comparator to allow response to 16 bit I/O addresses. When not installed only 8bit I/O addresses are used.
A0-Af	These positions configure the I/O address to which the Motherboard Interrupt Logic will respond. If an address bit is to be recognized as a logic one then the corresponding shunt must be installed in the position labeled with the address (i.e. ADR0=A0, etc.).
5	Connects Front Panel Interrupt to INT6/ line.
6	Connects Front Panel Interrupt to INT7/ line.
7	Connects Front Panel Interrupt to INT4/ line.
8	Connects Front Panel Interrupt to INT5/ line.
9	Connects Front Panel Interrupt to INT2/ line.
10	Connects Front Panel Interrupt to INT3/ line.
11	Connects Front Panel Interrupt to INT0/ line.
12	Connects Front Panel Interrupt to INT1/ line.

Table 9-1
Interrupt Switch Configuration Jumpers

9.6 Multibus/IEEE 796 Differences

The UNISTAR Multibus Motherboard was designed to the requirements of the Intel Multibus specifications as outlined in the Manual Order Number 98000683. However, the Intel P1 connector PIN 25 is used as the LOCK signal as required by the IEEE Standard. The UNISTAR motherboard also provides -5V which is not required by the IEEE specification but is by the Intel Multibus.

9.7 MOTHERBOARD POWER CAPACITY

The following table provides the maximum available power to the Multibus backplane (subtract P2 Motherboard requirements if installed). The UNISTAR system family of boards will consume a part of the available power and remaining power available to the spare card slots is specified in Chapter 2.

VOLTAGE SPECIFICATION	MAXIMUM AVAILABLE CURRENT
+12.0 V ± 5.0%	2.0 Amps
+ 5.0 V ± 3.0%	21.5 Amps
-12.0 V ± 5.0%	2.5 Amps
- 5.0 V ± 5.0%	0.5 Amps

The combination of the above supplies are not to exceed the power limit for the card cage of 145 Watts with the Winchester/Floppy disk combination of the UNISTAR system.

Table 9-2

Cardcage Power Specifications

CHAPTER 10 UNIX SYSTEM CONFIGURATION INFORMATION

10.1 UNIX SYSTEM CONFIGURATION INFORMATION

10.1.1 UNISTAR MEMORY

The UNISTAR comes with 320K bytes of RAM standard. The UNIX kernel takes up 148KB bytes, leaving 172K bytes for user applications. Note: The UNIX kernel actually occupies 84K bytes, out of 256K bytes of memory. For I/O performance reasons, a 64K byte board has been added to provide an enlarged buffer cache and Multibus I/O DMA memory area. Hence the 320K/148K figures.

The following sections describe each class of device provided on the UNISTAR. Each section is intended to be a summary, full information refer to section (4) of the UNIX Programmer's Manual, Volume I.

10.1.2 TERMINAL DEVICES

The UNISTAR provides from 2 to 10 asynchronous communications ports. One port (/dev/console) is always used for the UNISTAR console and keyboard, a second port (/dev/lp) generally attaches to a printer or similar device. The remaining 8 ports are optional equipment. Each port is configured as a DTE, i.e., transmits on pin 2, receives on pin 3. The following is the list of the special filenames for the ports:

MAJOR	MINOR	NAME	INITIAL SPEED	
0	0	/dev/console	9600	
0	1	/dev/lp	9600	
4	0	/dev/tty0	9600	(optional)
4	1	/dev/tty1	9600	(optional)
4	2	/dev/tty2	9600	(optional)
4	3	/dev/tty3	9600	(optional)
4	4	/dev/tty4	9600	(optional)
4	5	/dev/tty5	9600	(optional)
4	6	/dev/tty6	9600	(optional)
4	7	/dev/tty7	9600	(optional)

10.1.3 WINCHESTER DISK DEVICES

The UNISTAR provides an integral, 10MB 5.25 inch Winchester disk drive. The Winchester disk I/O device driver provides both block and character special files, as shown below:

TYPE	DRIVE	MAJOR/MINOR	NAME	START	END	HEADS	BLOCKS
B	0	0 / 9	/dev/w0z	000	305	4	19584
B	0	0 / 0	/dev/w0a	000	149	4	9600
B	0	0 / 12	/dev/w0b	150	305	4	9984
C	0	5 / 9	/dev/rw0z	000	305	4	19584
C	0	5 / 0	/dev/rw0a	000	149	4	9600
C	0	5 / 12	/dev/rw0b	150	305	4	9984

10.1.4 MINIFLOPPY DEVICES

The UNISTAR provides an 616K 5.25 inch floppy disk drive. The floppy disk I/O driver provides both block and character special files, as shown below:

TYPE	DRIVE	MAJOR/MINOR	NAME	START	END	BLOCKS
B	0	2 /35	/dev/f0	000	076	1232
C	0	7 /35	/dev/rf0	000	076	1232

10.1.5 UNISTAR UNIX

The following information specifies values selected for the current configuration of UNIX running of the UNISTAR. These values are subject to change at any time, without notice.

```
Number of blocks in the buffer cache . . . . . NBUF   = 20
Maximum number of unique inodes. . . . . NINODE = 60
Maximum no. of simultaneous open files . . . . NFILE  = 50
Maximum number of active processes . . . . . NPROC  = 40
Maximum number of mounted devices. . . . . NMOUNT = 12

Swap device......................./dev/w0a
Swap starting block number ...     100
Swap ending block number .....     149
Swap area in kilobytes........    1600
```

CHAPTER 11 REBUILDING THE UNIX SYSTEM FROM FLOPPY DISKS

11.0 GENERAL INFORMATION

If an occasion occurs when the UNIX system on the Winchester disk crashes and UNIX cannot be rebooted (see Chapter 4), then the UNIX system on the Winchester disk must be rebuilt.

*** WARNING ***

The following procedure to rebuild the UNIX system on the Winchester disk will overwrite any existing files on the Winchester disk. The UNIX system that will exist after the rebuild procedure will be a "fresh from the factory" system.

11.1 WINCHESTER REBUILD PROCEDURE

STEP 1: Initialize your system by turning the power off, and then follow steps 1 through 4 in section 4.2

STEP 2: Install the Callan Data Systems supplied floppy diskette labeled

Floppy disk 17, Bootable UNIX

into the floppy disk drive. (This is disk number 17).

Now boot in the UNIX system that exists on the floppy disk. This is done by typing the following command:

f(0,0)unix

The following message will appear:

Type Return to start at nXnnnn

At this time, press the RETURN key.

When the UNIX system comes up, it will display a single line with a pound sign ('#') on it. If this line is not displayed, or any line with the word 'ERROR' appear, repeat steps 1 and 2 above.

STEP 3: Execute the program f2w and follow its instructions. The f2w program will use the 16 diskettes (numbered 1-16) to restore the UNIX filesystems on the Winchester disk. A description of how to run f2w is contained in the next section.

11.2 FLOPPY DISK TO WINCHESTER RESTORE INCTRUCTOR (F2W)

NAME:

f2w - floppy disk to Winchester restore

SYNOPSIS:

f2w [raw_file]

DESCRIPTION:

F2W restores a UNISTAR Winchester disk from a set of floppy disks. The floppy disks must have been created by w2f, the Winchester to floppy backup program.

F2w normally reads from the floppy drive and restores to the Winchester disk drive that is 0. The optional argument raw_file can be specified to have f2w restore to another Winchester disk such as one on drive 1.

F2w works in a somewhat unusual way (for UNIX that is). UNIX is booted from a UNIX image on a floppy disk, and runs on that floppy disk. The f2w program is run off of the UNIX floppy. The UNIX floppy is then removed after the f2w program is executing so that the floppy drive may be used to read the backup diskettes.

This required of course that UNIX be booted and run off of the floppy in a single user mode so that no disk accesses by UNIS itself are made while f2w is running.

F2w is self-explanatory when running, the messages produced have been written for the UNIX novice.

EXAMPLE:

f2w

SEE ALSO:

WF2 - Winchester to floppy backup

FILES USED:

/dev/rf0 -- Input floppy
/dev/rw0z -- Output Winchester

11.3 WINCHESTER TO FLOPPY BACKUP INSTRUCTIONS (WF2)

NAME:

W2f - Winchester to floppy backup

SYNOPSIS:

w2f [-skip n]

DESCRIPTION:

W2f backsup a Winchester disk to a set of floppys. Fourteen floppys are required to back up the Winchester. The program f2w can later be used to restore the floppys to the Winchester.

The optional argument , skip -n, can be used to restart w2f if a floppy disk error causes w2f to abort. The number 'n' indicates the number of floppys o skip (i.e., are already backed up).

W2f should be run in the single user mode. A sync command should be issued prior tp running. All w2f messages are self-explanatory when running. The messages produced have been written for the UNIX novice.

EXAMPLE:

w2f w2f -skip 3 # redo from disk 4 onwards

SEE ALSO:

f2w - Floppy to Winchester restore

FILES USED:

/dev/rf0 -- Output floppy
/dev/rw0z -- Input Winchester