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CAL DATA

# SERIAL I/O CONTROLLER VARIABLE ADJUSTMENTS

SPEC. NO. C22410047

XO





california data processors

## INTRODUCTION

This Tech Tip describes the preparation of variable elements of the Cal Data SIO Serial I/O Controller, part number C81080330. These variable selections include:

a. Hardwired interrupt vectors
b. Bus-Request/Bus-Grant priority strap
c. Current loop adaption
d. EIA adaption
e. Baud-rate adjustment
f. MACROBUS address decode
g. Data transfer control

The information provided is with reference to schematic diagram C21080330.

## CONVENTIONS

Conventions used in the text include:

a. The proper names of signals are capitalized.
b. ZERO and ONE are used to express binary logic "0" and "1" states, respectively.
c. Octal numbers are preceded by a zero and hexadecimal numbers are preceded by a dollar sign for easy identification. Decimal and binary numbers are not prefixed.

Teleprinter input devices are identified as tape reader and keyboard. Output devices are tape punch and page printer.

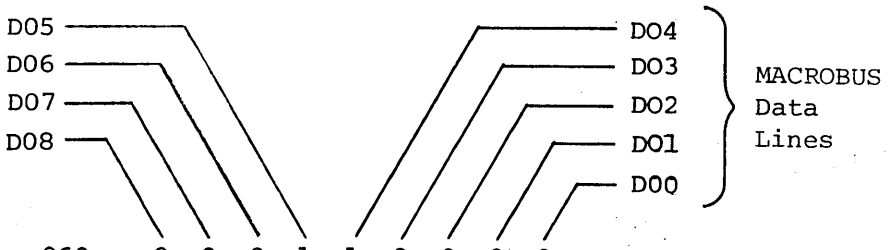
## HARDWIRED INTERRUPT VECTORS

The interrupt vector for the teleprinter paper tape reader and keyboard is currently at 060 and can be set for values from 0 to 0370 in increments of 010 by changing the "E" point connections on the SIO board. The vector for the printer is hardwired to be 04 greater than the vector for the tape reader (i.e., in the range of 04 to 0374).

The way this is determined is: each data bit has two "E" points associated with it. If a jumper connects the points, the associated bit is ZERO. If no jumper is used, the bit is ONE.

Examples:

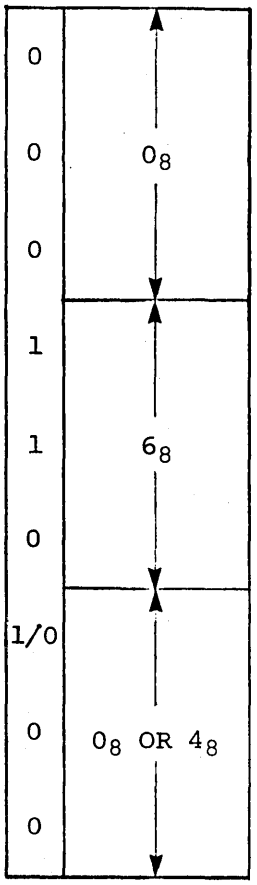
Refer to sheet 6 of the schematic.




VECTOR ADDRESS

READER/KEYBOARD = 060 = 0 0 0 1 1 0 0 0 0

PUNCH/PRINTER = 064 = 0 0 0 1 1 0 1 0 0




EITHER
READER/KEYBOARD:060
OR
PUNCH/PRINTER:064

*Data Lines D00-L, D01-2 and D08-L shown for illustrative purposes only, and do not appear on sheet 6 of S10 schematic or are they used for variable vector addressing.

## DATA TRANSFER CONTROL

The header at U35 makes available a number of options determing how data will be transferred. From the factory, all five control bits are in a logical ONE state. To set to a logical ZERO, a jumper is connected between corresponding pins, as follows:

| Corresponding Pins | Mnemonic | Logical State | Operation |
|---|---|---|---|
| 5, 12 | P1 | 1 | Parity bit inhibit. |
| | | 0 | Parity bit enable; appears after data bits and before stop bits. |
| 4, 13 | SBS | 1 | Selects two stop bits after byte. |
| | | 0 | Selects one stop bit. |
| 1, 16 | EPE | 1 | Selects even parity operation of parity bit. |
| | | 0 | Selects odd parity. |

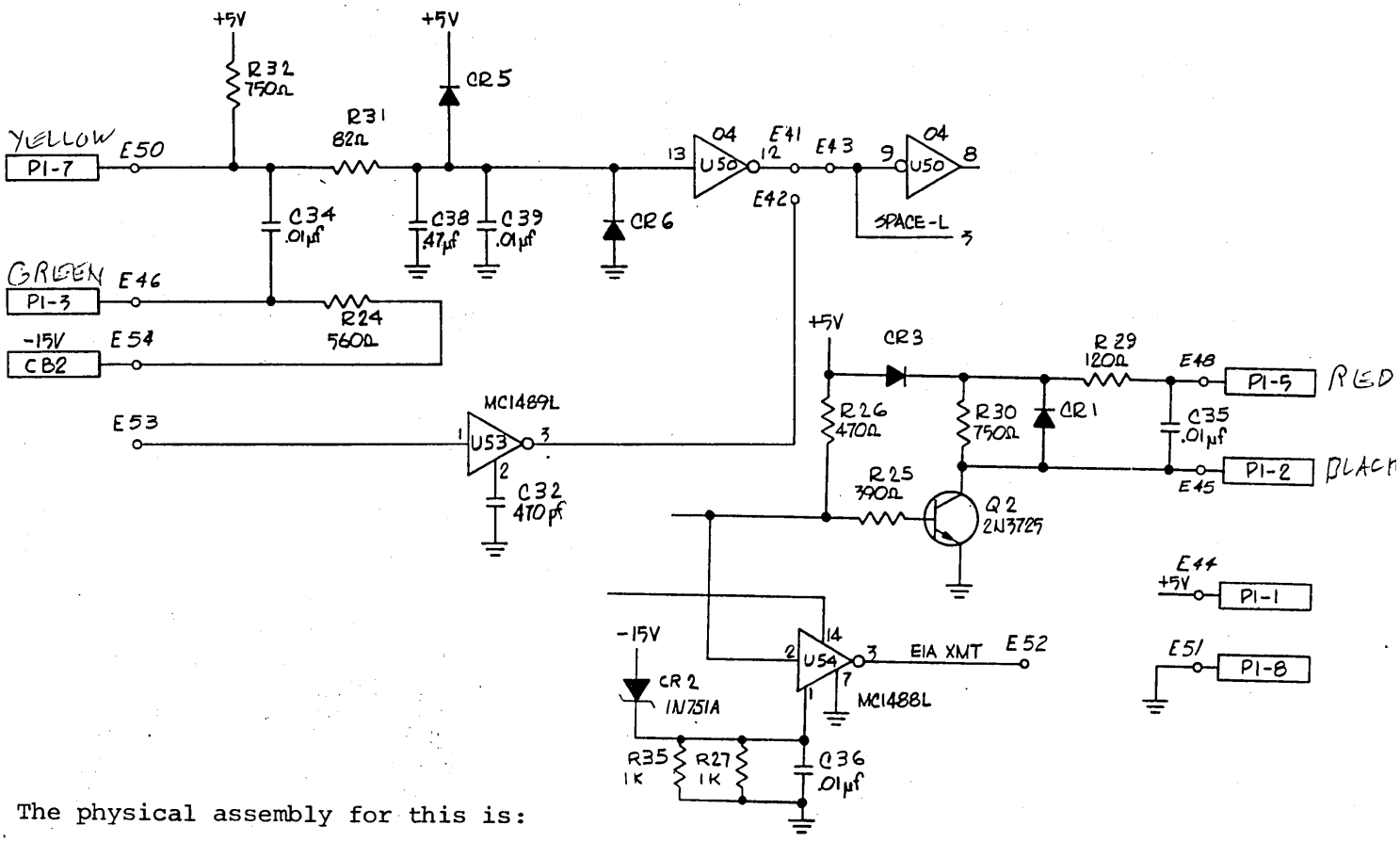
There are two bits to select the length of the byte to be transferred. WLS2 is the mnemonic for the bit corresponding to pins 2 and 15, and WLS1 corresponds to pins 3 and 14 of U35. The following indicate the type lengths as a function of these bits (as before, ZERO = jumper; ONE = no jumper):

| WLS2 | WLS1 | Byte Length |
|---|---|---|
| 0 | 0 | 5 bits |
| 0 | 1 | 6 bits |
| 1 | 0 | 7 bits |
| 1 | 1 | 8 bits |

Refer to sheet 3 of the schematic:

## CURRENT LOOP STRAPPING (TELEPRINTER)

Refer to sheet 4 of the schematic:




The physical assembly for this is:

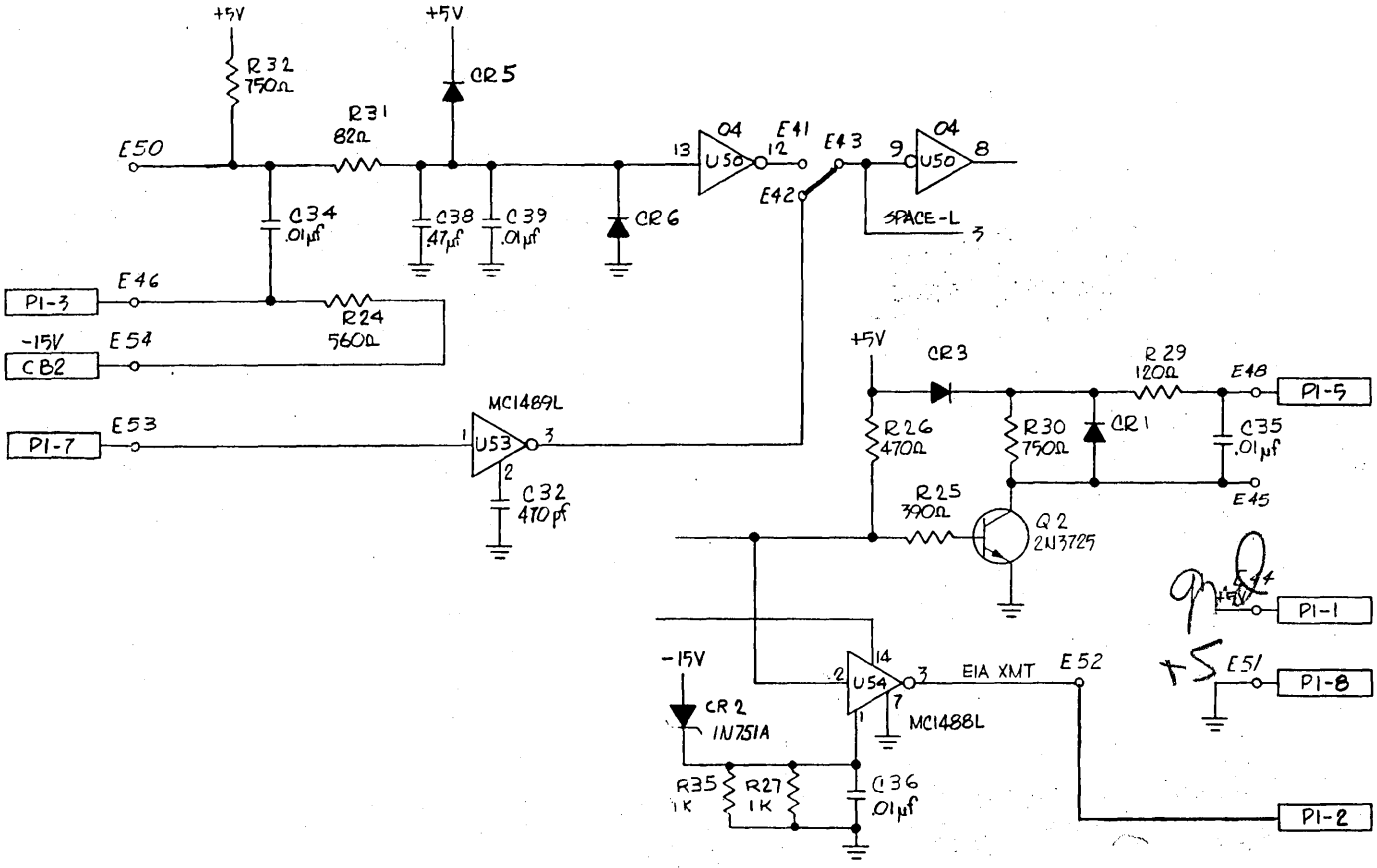
| Connections | |
|---|---|
| From | To |
| P1-1 | E-44 |
| P1-2 | E-45 |
| P1-3 | E-46 |
| P1-4 | E-47 |
| P1-5 | E-48 |
| P1-6 | E-49 |
| P1-7 | E-50 |
| P1-8 | E-51 |
| E-43 | E-41 |

## EIA ADAPTION

The SIO as it comes from the factory is assembled for use with a current-loop device (teleprinter). It has, however, the circuitry necessary to operate EIA devices, such as a CRT. There are only three modifications. Cut the etch between E41-E43 and replace this with a jumper between E42-E43. Secondly, remove the jumper between connector pin P1-7 and E50, and replace it with one from connector pin P1-7 to E53. Finally, remove the jumper between connector pin P1-2 and E45, and replace it with one from connector pin P1-2 to E52. The SIO now meets the accepted EIA specifications as a serial I/O controller.

## EIA Strapping (CRT, other SIO Devices)

Refer to sheet 4 of the schematic.



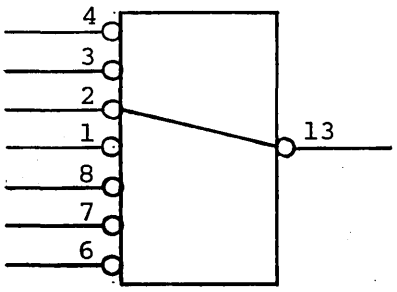
The physical assembly for this is:

| Connectors | |
|---|---|
| From | To |
| P1-1 | E-44 |
| P1-2 | E-52 |
| P1-3 | E-46 |
| P1-4 | E-47 |
| P1-5 | E-48 |
| P1-6 | E-49 |
| P1-7 | E-53 |
| P1-8 | E-51 |
| E-43 | E-42 |

NOTE: For clarity, only those connections for P1-2 and P1-7 are shown. All other connections remain the same as for current-loop operation.

## BAUD-RATE ADJUSTMENT

In order to set the baud rate to a particular frequency, two adjustments are necessary. The first is to insert the proper jumper into header U37, as shown on sheet 3 of the schematic. The header configuration is shown for a 600-baud configuration:




Each baud rate requires a strap from pin 13 to one of the first eight pins, depending on the rate.

The second necessary adjustment is the trimpot resistor R15, also on sheet 3. The trimpot should be adjusted so that the frequencies indicated below are observed at pin 40 of U51:

| Baud Rate | Baud Period (ms) | Strap from Pin 13 of U37 to Pin | Input Frequency (kHz) U51 Pin 40 | Input Period(µs) | Clock Frequency (kHz) U31 Pin 1 |
|---|---|---|---|---|---|
| 110 | 9.09 | 4 | 1.76 | 568 | 450.5 9.22 |
| 150 | 6.67 | 4 | 2.40 | 417 | 614.4 |
| 300 | 3.34 | 3 | 4.80 | 208 | 614.4 1.63 |
| 600 | 1.67 | 2 | 9.60 | 104 | 614.4 |
| 1200 | .833 | 1 | 19.20 | 52 | 614.4 |
| 2400 | .416 | 8 | 38.40 | 26 | 614.4 |
| 4800 | .208 | 7 | 76.80 | 13 | 614.4 |
| 9600 | .104 | 6 | 153.60 | 6.5 | 614.4 |

The baud rate is equal to the input frequency divided by 16. The baud period is equal to the input period times 16.

Example A: $\frac{9.6\ \text{kHz}}{16} = 600$ baud

Example B: 104 µs X 16 = 1.67

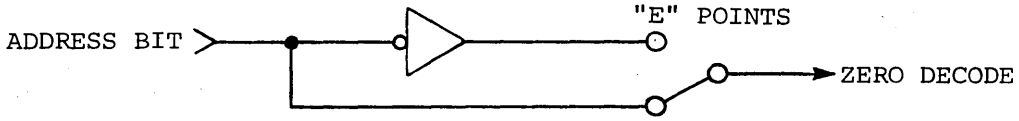
## ADDRESS DECODE

The MACROBUS addresses for the four SIO controller registers are hardwired at the factory as follows:

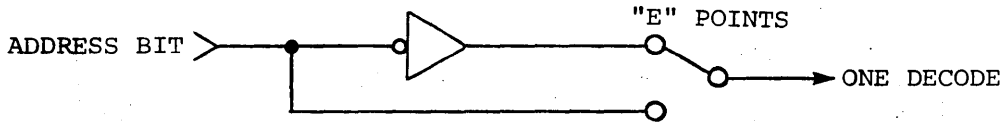
| Register | Address | Use |
|---|---|---|
| TKS | 0777560 | tape reader/keyboard status |
| TKB | 0777562 | tape reader/keyboard data buffer |
| TPS | 0777564 | printer/tape punch status |
| TPB | 0777566 | printer/tape punch data buffer |

These are as indicated on sheet 2 of the shcematic. By changing the "E" point connections, the TKS address is adjustable from 0770000 to 0777770. TKB, TPS and TPB have 02, 04 and 06 greater address values, respectively.

In order to set the registers to some address, it is necessary to set the address bits in the manner shown below. To set a bit to a logical ZERO decode, set the jumper between the "E" points (as indicated on sheet 2) corresponding to the lower position, so as to bypass the inverter:




For a logical ONE decode, set the jumper to the higher position:



Example:

Refer to sheet 2 of the schematic.