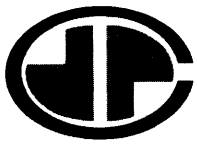
CDP-8KX16
MAGNETIC CORE MEMORY
(P/N C85500000)

TECHNICAL MANUAL
C21518001-X3



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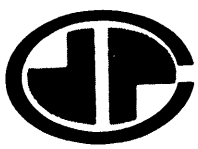

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REVISIONS

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X2	2-1-74		Release Edition
X3	9-12-74		Edited and Revised, New Repro

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ILLUSTRATIONS

SECTION 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides the information needed to understand, install and maintain the CDP-8KX16 Magnetic Core Memory when used with the drawing package provided. The information in this manual is for the use of a skilled technician familiar with standard test equipment, solid-state logic theory, common maintenance practices and standard troubleshooting techniques. A basic knowledge of design principles and circuits used in coincident-current core memories is assumed, hence no tutorial material of this kind is included. An understanding of the computers in which the CDP-8KX16 may be used is also assumed. Detailed information about these computers is available in published manuals.

As a stand-alone publication, this manual has a good functional and physical description of the CDP-8KX16, providing the information needed to understand the capabilities and optional features of the memory and to plan a system using it. The maintenance coverage of this manual is commensurate with the prerequisite skills and knowledge of the defined user, characteristics of the product and maintainability requirements established by Cal Data.

Users holding controlled copies will be provided with revisions and additions to this manual.

1.2 DOCUMENTATION

Cal Data products covered in this manual include:

85000	Standard CDP-8KX16
85001	Interleaved CDP-8KX16
85002	CDP-8KX16 with 7K-word option

The following paragraphs define publications and conventions that support this manual.

1.2.1 Publications

The Cal Data MACROBUS is described in publication C21518013, MACROBUS Channel Adapter Technical Manual.

For maintenance purposes, this manual is supported by a drawing package that contains theory of operation, schematic diagrams, assembly drawings and other required engineering drawings.

1.2.2 Abbreviations and Conventions

Table 1-1 lists the abbreviations found in this manual.

Conventions used in the text of this manual include:

a. Equipment panel nomenclature is reproduced in all upper case characters.
b. The proper names of instructions, microcommands and signals are capitalized.
c. ZERO and ONE are used to express binary logic "0" and "1" states, respectively.
d. Octal numbers are preceded by a dollar sign for easy identification. Decimal and binary numbers are not prefixed.

Table 1-1. Abbreviations

Abbreviation	Meaning
Cal Data or CDP	California Data Processors
A	ampere
cm	centimeter
dc	direct current
I/O	input/output
K	1,024 memory locations
lfm	linear feet per minute
lmm	linear meters per minute
mA	milliampere
ns	nanosecond
µA	microampere
V	volt
DMA	direct memory access
MMU	memory management unit

SECTION 2
DESCRIPTION

2.1 GENERAL

The CDP-8KX16, shown in Figure 2-1, is a plug-compatible storage element for the Cal Data and PDP-11 series of computers. The CDP-8KX16 offers several outstanding features and advantages. These include:

High speed. The 275-nanosecond access and 675-nanosecond cycle times offer a fast core memory system for the PDP-11 series.

Full compatibility. The CDP-8KX16 can be installed in all Cal Data and PDP-11 models, thus eliminating the need for different versions or expensive, space-consuming auxiliary mounting boxes, power supplies and interface cables.

Reduced bus loading. The Cal Data memory has a low MACROBUS (and UNIBUS) load specification, permitting expansion in large system configurations.

Low power consumption. The dc power consumption of the CDP-8KX16 is lower than comparable memory modules available.

7K-word option. This option permits Cal Data and PDP-11 systems to be expanded to 31K words (versus 28K words) without addition of a memory management unit. Only 1K rather than 4K word locations are reserved for I/O device addresses. (The system can be expanded to 127K words of addressable memory with the optional CDP-MMU Memory Management Unit.)

2.2 FUNCTIONAL DESCRIPTION

The CDP-8KX16 is a random-access, coincident-current ferrite core memory, arranged in a "three-wire, 3-D" configuration. The capacity is 8,192 words of 16 bits each. The CDP-8KX16 consists of:

a. A single full-size printed circuit board containing the memory electronic circuitry.
b. A plug-in magnetic core-plane board.

The CDP-8KX16 can be operated in one of four modes:

a. Read/restore (equivalent to PDP-11 DATI).
b. Half-cycle read (equivalent to PDP-11 DATIP).
c. Clear/write (equivalent to PDP-11 DATO).
d. Clear/write byte (equivalent to PDP-11 DATOB).

The full memory cycle (clear/write or read/restore) time is 675 nanoseconds for the worst case, measured at the memory interface connector. The worst case read-data access time is 275 nanoseconds.

Since the CDP-8KX16 is directly compatible with the PDP-11 computer series, the memory interface follows all rules of the standard UNIBUS.

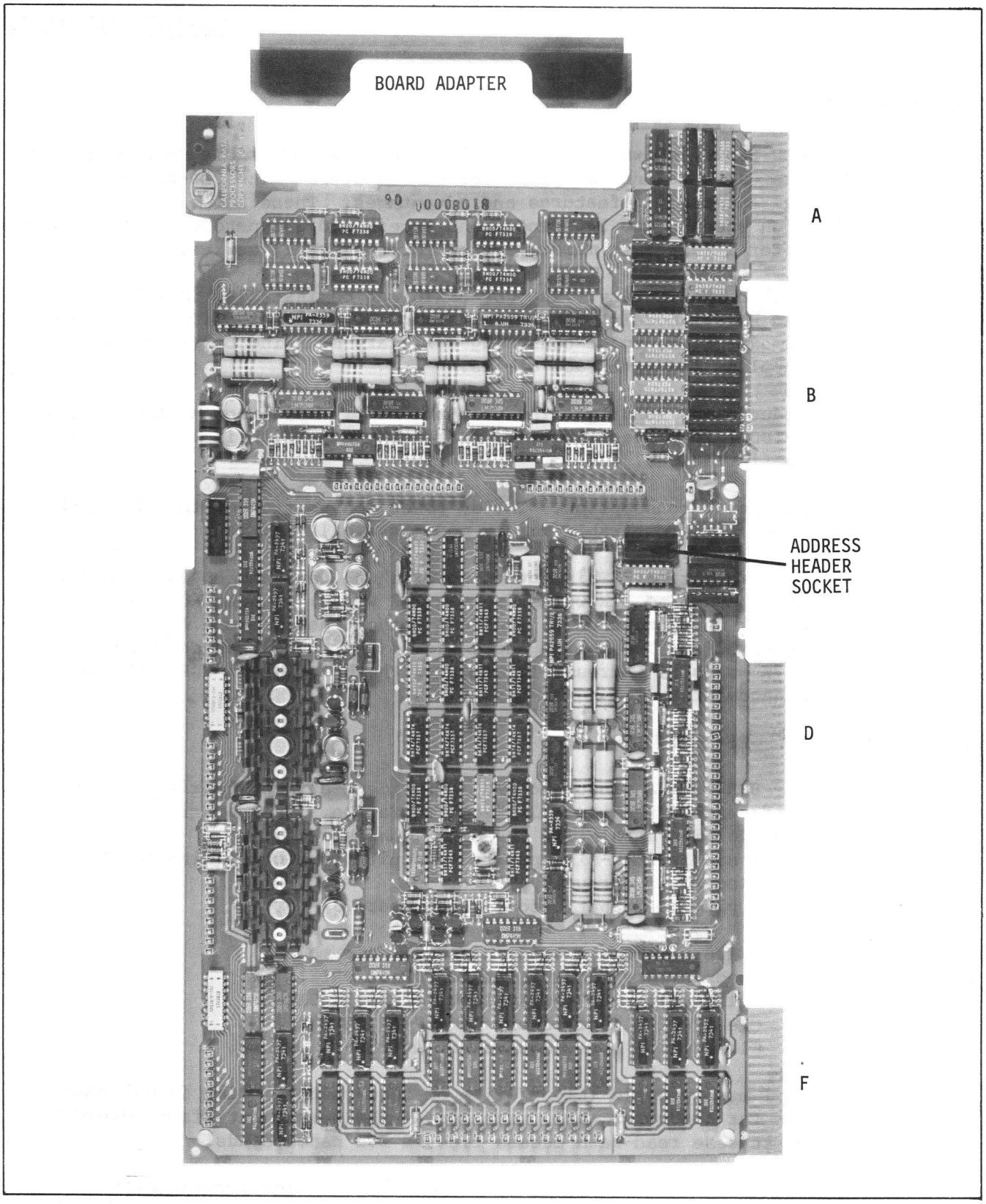


Figure 2-1. CDP-8KX16 Magnetic Core Memory, Component Side

The CDP-8KX16 is a functionally complete module and requires no additional supporting electronics (other than dc power) for operation in a MACROBUS (or UNIBUS) interface environment.

The CDP-8KX16 is addressed by a set of 18 address lines. In the standard configuration, each CDP-8KX16 module in a system uses the least-significant 14 bits of the address for byte or word selection. The least-significant bit (A00) selects either the more-significant (even) or less-significant (odd) data byte for modification during a clear/write-byte operation (DATOB). The most-significant four address bits select one of 16 possible module starting addresses, which can be between 0 and 120K in 8K increments. A plug-in address header assembly provided with each CDP-8KX16 patches the desired starting address.

In addition to the standard configuration described above, two optional configurations are available:

a. Interleaved modules
b. 7K-word option

2.2.1 Operating Modes

2.2.1.1 Read/Restore (DATI)

In a read/restore operation, the CDP-8KX16 reads information from a selected core location, transfers it to the MACROBUS and then writes the information back into the core location. Restoring is necessary, since the process of reading a core location erases the contents.

During the read cycle of the operation, the CDP-8KX16 loads the accessed information into a register while applying it to the MACROBUS.

During the restore cycle of the operation, the CDP-8KX16 writes the information held in the register back into the selected location.

2.2.1.2 Half-Cycle Read (DATIP)

In a half-cycle read operation, the CDP-8KX16 reads information from a selected core location, transfers it to the MACROBUS and then pauses.

During the read cycle, the CDP-8KX16 loads the accessed information into a register while applying it to the MACROBUS. Data are provided to a master device for modification prior to being restored in the same location. The half-cycle read operation should be followed by a write operation (DATO or DATOB), since any other subsequent operation leads to a memory error and can prevent proper operation of the MACROBUS.

2.2.1.3 Clear/Write (DATO) and Clear/Write Byte (DATOB)

In a clear/write operation, the CDP-8KX16 reads information from a selected core location, discards the information and then writes into the selected location the information provided on the MACROBUS. The read part of the cycle is necessary to clear the specified location prior to writing new data. If the clear/write operation is specified after a half-

cycle read operation (DATO following DATIP), the read cycle of the operation is not performed, reducing the operation time by about 50 percent. Regardless of whether the clear/write operation is commanded independently or after a half-cycle read operation, the data to be stored are loaded into a register immediately on receipt of the command. Any information previously stored in the register is lost. During the write cycle of the operation, the CDP-8KX16 writes the information held in the register into the selected location.

A clear/write byte operation is identical to a clear/write operation, except that only the byte to be stored is loaded into a register immediately on receipt of the command. Any information previously stored in that half of the register is lost. The other half of the register always contains the retained byte previously read from the selected location. The write cycle of the operation is identical for both clear/write operations.

2.2.2 Interleaved Modules

A pair of CDP-8KX16 modules can be set for interleaved operation in which words at even and odd word addresses are written into or read from alternate modules. A clear or read operation can begin in one module while a write or restore operation is being completed in the alternate module, giving a higher effective memory-transfer rate. This configuration is prepared by interchanging the least-significant word-address bit (A01) with the least-significant module-address bit (A14).

Interleaving is always associated with a pair of CDP-8KX16 modules, and the interleaved pair is effectively treated as a contiguous series of 16K word (32K byte) locations. Interleaved CDP-8KX16 modules must be ordered in this configuration.

2.2.3 7K-Word Option

The basic Cal Data and PDP-11 computer systems limit, by convention, the number of usable memory locations to 28K. The last 4K locations (out of a maximum of 32K) are reserved for I/O device addresses other than core memory. Expansion of addressable memory from 28K to 124K requires addition of a memory management unit.

In some systems, 1K is adequate for nonmemory I/O devices. The Cal Data 7K-word option permits addressable memory expansion to 31K (versus the usual maximum of 28K) without requiring the addition of a memory management unit. With a memory management unit installed, the 7K-word option permits addressable memory expansion to 127K.

2.2.4 Other Features

The CDP-8KX16 permits retention of previously stored contents during a power-up or a power-down sequence. A dc power status signal (DCLO) indicating availability of properly regulated dc power is supplied to the CDP-8KX16 on one of the interface pins. A low signal disables the select current drives to all memory locations and prevents erasure of data by spurious current pulses during a transient power condition. This dc power status signal is generated by the power supply when the CDP-8KX16 is used in a compatible computer environment.

Voltages required for memory operation are +5 Vdc and -15 Vdc. No special sequencing of these voltages is required by the CDP-8KX16.

2.3 PHYSICAL DESCRIPTION

The CDP-8KX16 (Figures 2-1 and 2-2) is contained on a drive electronics board having overall outline dimensions of 15.7 inches (39.9 cm) by 8.9 inches (22.7 cm). The drive board contains AMP Mod. 1 recepticles into which the core-plane assembly plugs from the back side of the board (Figure 2-3). The core-plane assembly is shown in Figure 2-4. The overall depth of the CDP-8KX16 assembly with core-plane installed is 0.9 inch (2.2 cm).

The drive board contains all electrical circuits of the memory except the steering diodes associated with the core-plane X and Y drive lines. The core-plane assembly is a planar array of magnetic cores mounted on a substrate, with a protective cover plate. The core-plane board also contains the X and Y drive-line steering diodes and current-probe test loops. The core-plane assembly is electrically connected by AMP pins to the drive board.

On the top right-hand edge of the board, a 0.2 by 5.3 inch (0.4 by 13.5 cm) indentation permits a flat I/O cable to exit the rear of the chassis over the top of the board.

CDP-8KX16 modules should normally be mounted nearest to the CPU inside the chassis, since I/O device cables are most easily routed outside from the rear of the chassis.

The right-hand edge of the board has a 1.0 by 5.5 inch (2.5 by 14.0 cm) cut out as clearance for the side-mounted cooling fans in the Cal Data, PDP-11/15 and PDP-11/20 computers, as well as the DEC BA11-EC and BA11-ES extension mounting boxes. When the CDP-8KX16 is installed in a PDP-11 model 05, 10, 35, 40 or 45, a board adapter can be inserted into the cut-out area to provide a continuous edge for mating with the card guides of these computers.

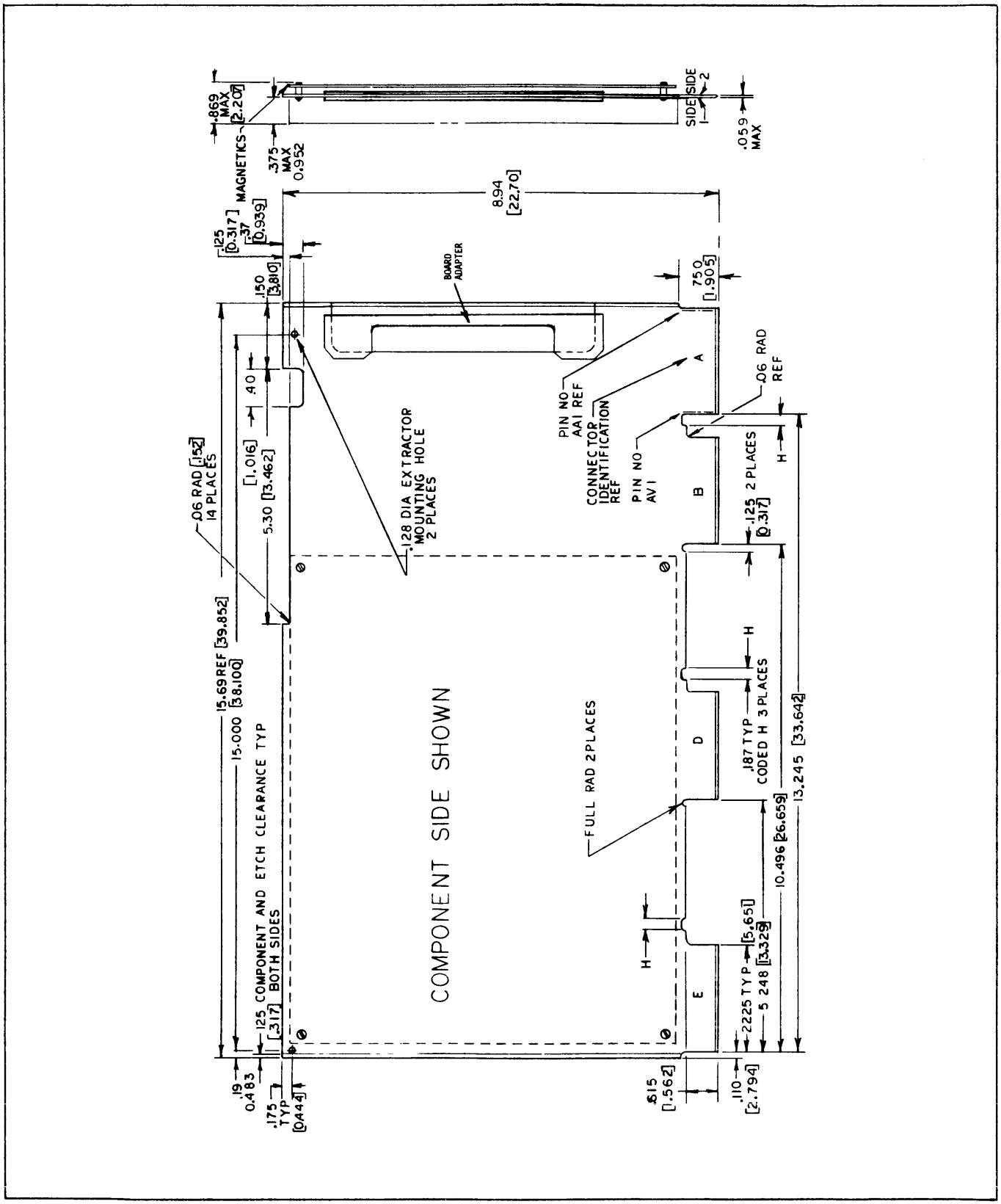


Figure 2-2. CDP-8KX16 Magnetic Core Memory, Mechanical Outline

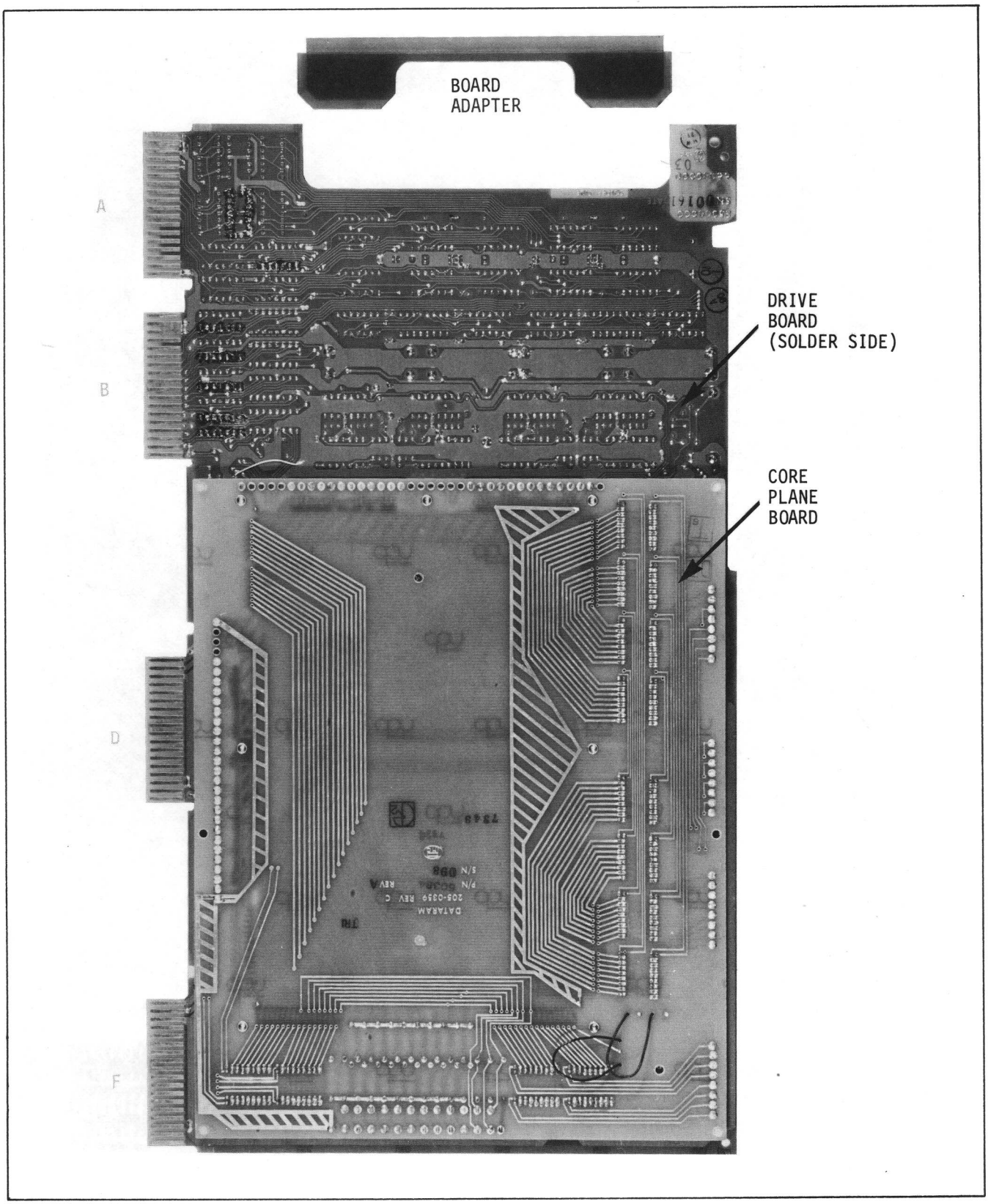


Figure 2-3. CDP-8KX16 Magnetic Core Memory, Core-Plane Side

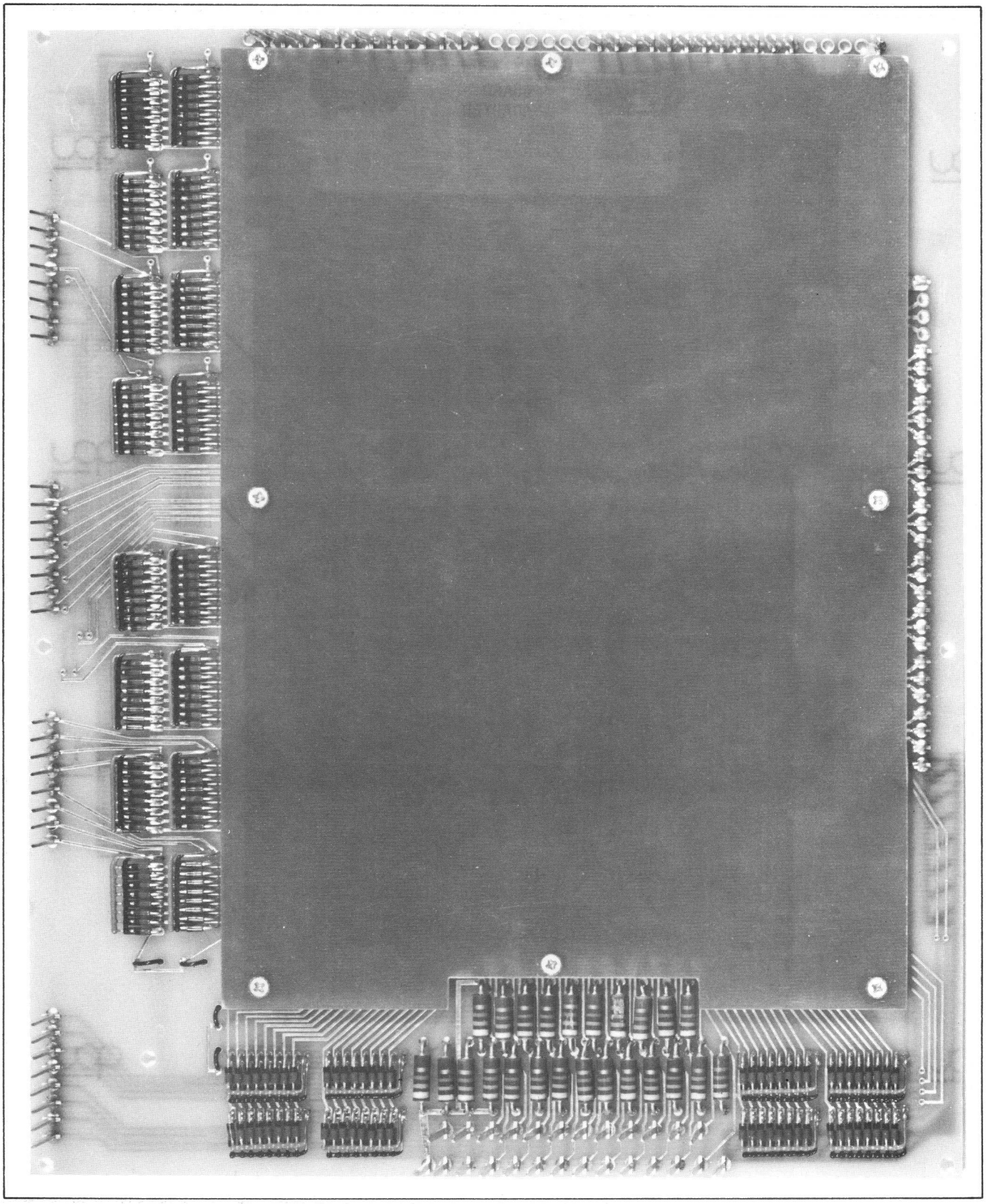


Figure 2-4. CDP-8KX16 Magnetic Core Memory, Core-Plane Assembly

2.4 SPECIFICATIONS

General specifications for the CDP-8KX16 are given in Table 2-1.

Table 2-1. CDP-8KX16 Memory General Specifications

Characteristic	Specification		
Type	Ferrite magnetic core, random access, coincident current.		
Organization	3-wire, 3-D planar core array.		
Word length	16 bits.		
Storage capacity	8,192 words (16,384 bytes).		
Operating times:		Cycle Time (1)	Access Time (1)
	Noninterleaved	Interleaved (2)	
Read/restore (DATI)	675 ns	425 ns	275 ns
Read (DATIP)	275 ns	275 ns	275 ns
Clear/write (DATO)	675 ns	340 ns	-
Half-cycle write	425 ns	450 ns	-
Interface signals:	Input	Bidirectional	Output
High (False)	+2.5 V min	+2.5 V min	
Low (True)	+1.4 V max	+1.4 V max	+0.5 V max at 50 mA
Input current	+120 µA max at 2.5 V	+120 µA max at 2.5 V	+120 µA max at 2.5 V
Power:	Operating (3) Amperes	Standby (3) Amperes	Voltage Tolerance
+5 Vdc	2.8	1.80	±5%
-15 Vdc	4.4	0.34	±5%
Ambient temperature	0 to 50°C with 200 lfm (56.6 lmm) airflow.		
Ambient humidity	0 to 90 percent without condensation.		
Dimensions	8.9 by 13.2 by 0.9 inches (22.7 by 33.6 by 2.2 cm).		
Mounting centers	1 inch (2.5 cm) recommended minimum.		

Notes:

1. Worst case, measured at the CDP-8KX16 module interface connector.
2. Effective cycle time for sequential access to contiguous interleaved memory locations.
3. Maximum current drain for continuous operation. For noninterleaved operation, only one memory module in the system is operating at a time. The others are on standby. If two CDP-8KX16 modules are interleaved, both should be considered as operating for power calculations.

SECTION 3
INTERFACE

3.1 GENERAL

This section describes the functional circuit design of the CDP-8KX16 and operation of the memory as an I/O device. The CDP-8KX16 conforms to all standard UNIBUS interfacing rules and interfaces equally well with the standard Cal Data MACROBUS or UNIBUS. This section assumes an understanding of these I/O structures. Detailed MACROBUS information is available in other technical publications.

3.2 INTERFACE DESCRIPTION

The CDP-8KX16 connects either to the MACROBUS or UNIBUS as a standard peripheral device. It always operates as a slave device (i.e., the memory never takes control of the bus as a master device). Thus, all transfers are controlled by a bus master, such as the CPU or a direct-memory-access controller.

The memory is designed to plug into a single standard hex-height connector row; however, the unit plugs into only connectors A, B, D and F. All functional interface signals used by the memory terminate on the A and B connectors, with standard pin assignments used. Bus Grant signals are not used by the memory module; however, these signals are jumpered through the D connector via etched lines on the board so that these priority interrupt lines are automatically propagated with the memory installed.

If a memory is removed from a location and no new board is installed, the Bus Grant lines must be jumpered on the connector if other I/O devices are operating on any of the priority interrupt lines. The D and F connectors are used for power and ground connection to the memory module.

The CDP-8KX16 decodes the 18-bit address transmitted on the MACROBUS when a Master Synchronization signal (MSYN) is asserted by the device in control of the bus (bus master). If the address corresponds to the CDP-8KX16 module address, the CDP-8KX16 responds by executing the operation specified by the mode Control lines (C0, C1) and asserting a Slave Synchronization signal (SSYN) on the MACROBUS to indicate acceptance or availability of data.

3.2.1 Interface Signals

Table 3-1 lists the mnemonic, name and description of each MACROBUS signal used by the CDP-8KX16. Signals not required for memory operation are ignored (open circuit); however, there are certain signals associated with chained priority operations on the MACROBUS that require physical line continuity through the interface connectors, whether or not the interface device uses the signals. The CDP-8KX16 ensures continuity of these signals, when installed, by propagating the necessary signal lines via etched conductors on the circuit board. If a memory module is removed from the

Table 3-1. MACROBUS Signal Definitions

Mnemonic	Name	Description	Memory Use
A17 to A00	Address	Selects slave device.	A17 to A14 select module; A13 to A01 select word; A00 selects byte.
D15 to D00	Data	Word or byte transferred.	Data in or out.
C0 and C1	Control	Selects mode.	Operation performed.
MSYN	Master Synchronization	Initiates operation.	Gates in A, D and C signals.
SSYN	Slave Synchronization	Response to MSYN.	Signals acceptance or availability of data.
PA			Reserved.
PB			Reserved.
NPR	Nonprocessor Request	Highest-priority bus request. Not used for interrupts.	Ignored.
BR7 to BR4	Bus Request	General bus request where CPU interrupts are involved.	Ignored.
NPG	Nonprocessor Grant	Grant response to NPR.	Ignored.
BG7 to BG4	Bus Grant	Grant response to BRn.	Propagated, ignored.
SACK	Selection Acknowledgement	Acknowledges bus grant.	Ignored.
BBSY	Bus Busy	Asserts bus mastership.	Ignored.
INTR	Interrupt	CPU interrupt notification sent with interrupt vector address.	Ignored.
INIT	Initialize	Clear and reset.	Initializes memory.
ACLO	AC Low	Impending power failure.	Ignored.
DCLO	DC Low	DC voltages out of tolerance.	Protects memory contents.

system, these signal lines must be closed by jumper wiring or other means if another board is not physically located in the vacated connector slot.

Appendix A lists interface pin assignments.

3.2.2 Control Modes

The CDP-8KX16 operates in one of four modes (Table 3-2) specified by bus Control lines C0 and C1. In modes requiring a byte operation (DATOB), address bit A00 specifies the byte affected.

Table 3-2. CDP-8KX16 Operating Modes

A00	C1	C0	Command	Operation
x	0	0	DATI	read/restore
x	0	1	DATIP	half-cycle read
x	1	0	DATO	clear/write
0	1	1	DATOB 0*	read/restore byte 1, clear/write byte 0
1	1	1	DATOB 1*	read/restore byte 0, clear/write byte 1

*Byte 0 = less-significant; byte 1 = more-significant.

CDP-8KX16 logic forces the operation immediately following DATIP to be a half-cycle write operation. The bus master initiates DATO or DATOB after DATIP, and these commands are interpreted by the memory logic as half-cycle write operations.

3.3 INTERFACE TIMING

Figure 3-1 shows interface timing for the basic CDP-8KX16 operations. The direction of data transfer is given with respect to the bus master rather than to the CDP-8KX16. Thus, data input implies a transfer to the master (output from the CDP-8KX16), and vice versa.

3.3.1 Read/Restore (DATI)

The CDP-8KX16 reads a 16-bit word from the location designated by the input address and places the word on the MACROBUS. The word is also restored automatically by the CDP-8KX16.

As shown in Figure 3-1, the Address and Control lines (A17 to A00, C0 and C1) must be settled at the CDP-8KX16 at least 50 nanoseconds prior to receipt of MSYN to permit decoding of these signals. Data (16-bit word) read from memory and SSYN are placed on the bus within a maximum of 275 nanoseconds from receipt of MSYN. The addressed word is restored during the next 400 nanoseconds. Address and Control signals received at 625

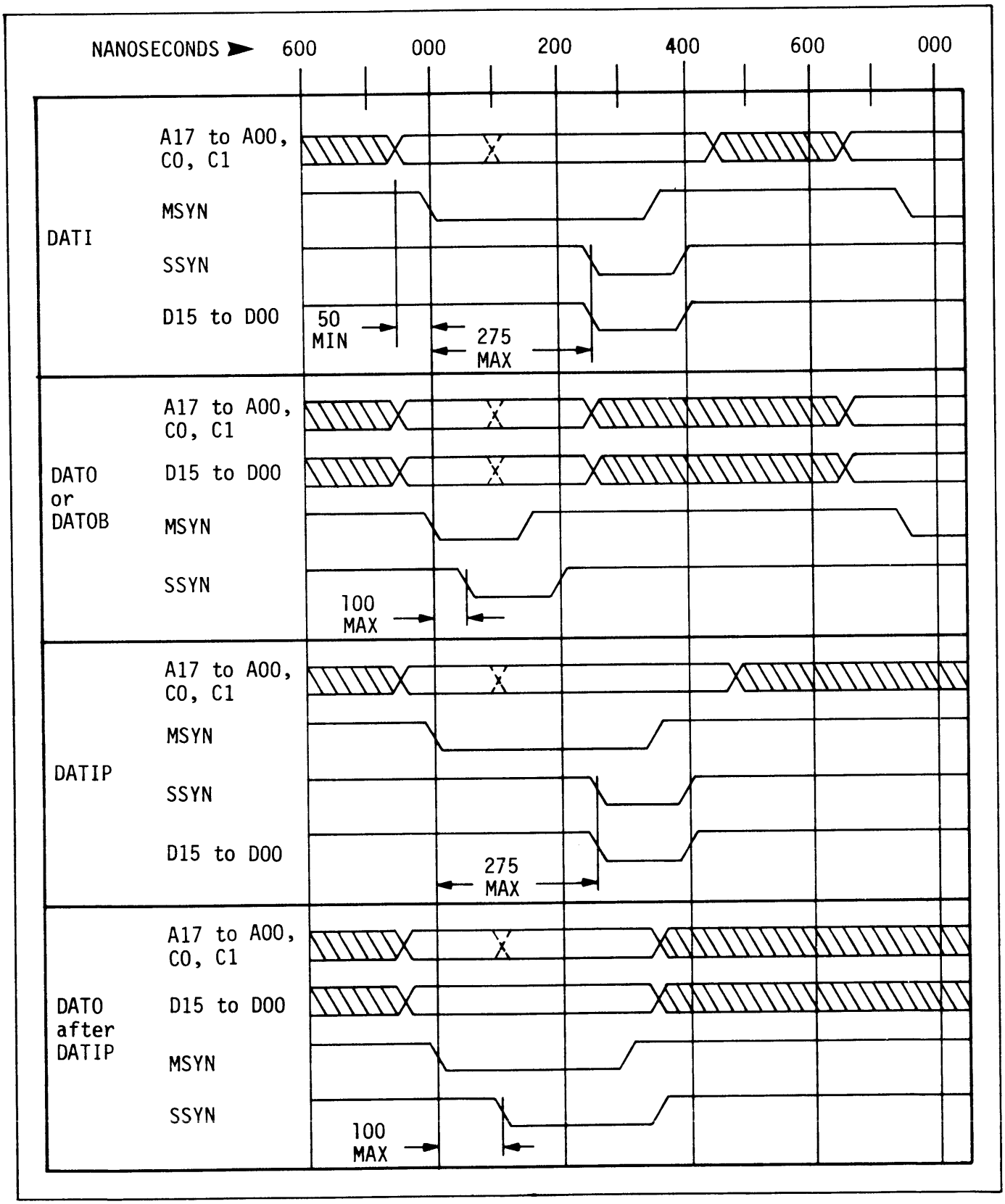


Figure 3-1. CDP-8KX16 Memory Interface Timing

nanoseconds, followed by a MSYN at 675 nanoseconds, result in a minimum repetitive read/restore cycle of 675 nanoseconds.

The CDP-8KX16 provides internal storage for the Address and Control signals, hence it is not necessary to retain information on these lines throughout the cycle. The earliest recommended time for removing the Address and Control signals is 100 nanoseconds after MSYN is received. Because of the asynchronous nature of the MACROBUS, the bus master has no indication that the memory operation has actually started until SSYN is received. Early removal of Address and Control signals is not useful in this case, but other applications could make use of this feature.

The operation timing shown represents the guaranteed worst-case and, in general, the CDP-8KX16 operates faster than specified. MSYN can be reasserted within 150 nanoseconds after it has been removed in response to SSYN, provided that the Address and Control signals have been established at least 50 nanoseconds earlier.

3.3.2 Clear/Write (DATO) and Clear/Write byte (DATOB)

For DATO, the CDP-8KX16 clears the location designated by the address lines and writes into that location the 16-bit word received from the MACROBUS.

As shown in Figure 3-1, the Address, Control and Data signals must be settled at the interface connector at least 50 nanoseconds prior to receipt of MSYN to permit decoding of the Address and Control signals, and storing of the data. SSYN is asserted on the MACROBUS within 100 nanoseconds after MSYN is recognized. The clear/write operation internal to the memory requires 675 nanoseconds, maximum.

MSYN can be reasserted within 150 nanoseconds after it is removed in response to SSYN, provided Address and Control signals are settled at least 50 nanoseconds earlier. The CDP-8KX16 generally operates at a speed higher than specified.

Timing for the clear/write-byte operation (DATOB) is identical to that for DATO. Functionally, the CDP-8KX16 clears and writes only the designated byte (odd or even). A read/restore operation is performed on the other byte.

3.3.3 Half-Cycle Read (DATIP)

The CDP-8KX16 reads a 16-bit word from the location designated by the input address and places the word on the MACROBUS along with SSYN. The word read out is not restored, but is held in the memory data register. Access timing at the interface is identical to that for DATI (Figure 3-1).

DATIP permits the word read out to be modified by the bus master and the modified word restored in the same location. The bus master must retain mastership until the modified word is restored. To ensure that proper design rules are followed, DATO and DATOB are the only commands permitted to follow DATIP. These operations can be initiated within 150 nano-

seconds (by reassertion of MSYN) after MSYN has been removed following the assertion of SSYN by the CDP-8KX16, provided that Address and Control signals are settled at least 50 nanoseconds earlier. Figure 3-1 shows the timing.

The CDP-8KX16 automatically performs a half-cycle write operation in response to the next MSYN after a DATIP, regardless of the states of C1 and C0.

3.4 INTERFACE CIRCUITS

Because memories are attached to the MACROBUS as peripheral devices, the bus loading introduced by CDP-8KX16 is an important system consideration for configurations containing a large amount of memory or numerous peripheral devices. The CDP-8KX16 minimizes the loading of receivers and the leakage current of drivers in the high state (these being the critical bus-loading parameters). This is accomplished in two ways:

a. The driver leakage load is limited to that of one gate instead of two (as is common in other designs).
b. A Cal Data proprietary bus receiver circuit improves speed and reduces drive requirements.

3.4.1 Line Driver

The line drive is a TTL buffer. The critical bus specifications for the device are:

Output-low voltage at 50 mA sink (V_{OL})	+0.5 V, max
Output-high leakage current at 2.5 V (I_{OH})	+60 µA, max

3.4.2 Line Receiver

The CDP-8KX16 uses a Cal Data line receiver. The critcal bus specifications for this device are:

Input-high threshold (V_{IH})	+2.5 V min
Input-low threshold (V_{IL})	+1.4 V max
Input current at +2.5 V (I_{IH})	+60 µA max
Input current at 0.0 V (I_{IL})	±25 µA max

3.4.3 Bus Loading

The limiting bus load occurs on the bidirectional data lines that have one receiver and one driver for each CDP-8KX16 memory module. Worst-case module bus load specifications are:

V_{IH}	+2.5 V min
V_{IL}	+1.4 V max
I_{IH}	+120 µA max at +2.5 V
I_{IL}	±25 µA max at 0.0 V

SECTION 4

INSTALLATION

4.1 GENERAL PROCEDURES

When used as part of a Cal Data system, the CDP-8KX16 will have been installed and tested by Cal Data prior to shipment. Thus, the following procedures describe the installation of modules received individually for addition to an existing installation.

The CDP-8KX16 core memory module is designed for direct installation in a Cal Data computer, in a CDP-EB Extension Box, a DEC BA11-EC or BA11-ES extension box or in any model computer of the PDP-11 series.

Before installing the CDP-8KX16 in a PDP-11 computer, the user should be familiar with physical details of the applicable system, particularly the backplane (system-unit signal wiring and power distribution). The CDP-8KX16 interfaces with the standard UNIBUS signals carried in the A and B connector columns of all PDP-11 series computers. The specific installation procedures vary with each model in the series, since the physical signal connector and power distribution schemes differ from model to model.

The signal, power and ground connections to the CDP-8KX16 are made via the A, B, D and F connectors as given in Appendix A. For any given installation, compare this signal list against that of the backplane of system unit for the intended installation.

The general installation procedure consists of inserting the CDP-8KX16 into the appropriate connectors so that A and B plugs interface with the MACROBUS (or UNIBUS) connectors. The component side of the CDP-8KX16 drive board faces the same direction as the component side of the standard circuit boards. In a DEC chassis, the CDP-8KX16 core-plane, which plugs into the rear of the drive board, blocks the next connector slot, since standard PDP-11 connector rows are on half-inch centers and the CDP-8KX16 requires 0.9 inch (2.2 cm). This restriction does not apply to Cal Data chassis, which have one-inch (2.5 cm) memory slot separation.

4.1.1 Unpacking and Inspection

Each CDP-8KX16 is shipped in an individual, padded shipping container for protection during transportation. This container can be saved for future use if the unit is returned for repair or reshipped separately from the associated computer system.

The following steps are recommended for unpacking and initially inspecting the memory:

1. Prior to opening, inspect the container for obvious damage.
2. Cut the packing tape, open the container and remove the module. Next remove the plastic wrapper and inspect the module for physical damage.

3. Inspect the board connector pins for any foreign matter and clean, if necessary, for reliable contact with the connectors.

It is important to note immediately any physical damage that might have resulted from shipment. The carrier should be notified of such damage and given the opportunity to inspect the unit and container. This helps establish the validity of any claims for shipping insurance.

4.1.2 Handling

The CDP-8KX16 can withstand all normal shock and vibration encountered in shipping and when installed in a computer system. While not a fragile device, the unit should be handled with reasonable care to avoid damage that might result in operational failure. The following are some general pointers on handling the unit during inspection, installation and maintenance operations:

a. The core stack plugs into the rear of the drive board and is held in place by safety nuts at several points on the stack assembly. These nuts should always be on and tight when the memory is installed in a system.
b. When inserting the CDP-8KX16, be sure that the component side faces the correct direction and that the board is aligned in the card guides.
   DO NOT EXERT PRESSURE ON THE CORE-PLANE BOARD.
c. Avoid bending components when handling the drive board. To prevent oxides from forming on the gold plating, do not touch the connector pins.
d. Always insert and remove modules with the system power OFF.
e. When inserting or removing the CDP-8KX16, be sure that the component side faces the correct direction and that the board is aligned in the card guides.
f. Insert and remove the memory slowly and carefully so that it does not make contact with adjacent boards.
g. Never use components as finger grips. Use the grip areas at the corners of the board.

4.1.3 Address Strapping

Each memory module in a system must have a different block starting address to prevent more than one unit responding to the same address from the CPU or DMA device (except for interleaved pairs, which have a common block starting address).

The CDP-8KX16 can be set to any starting address from 0 to 120K in 8K increments. Interleaved modules can have starting addresses from 0 to 112K in 16K increments.

Cal Data provides a memory address header assembly with each CDP-8KX16. This assembly can be delivered either prewired to a specified starting address, as defined in Table 4-1, or unwired, according to user specification. The assembly plugs into a socket on the board. This should be done prior to system installation.

Table 4-1. Jumpers for CDP-8KX16 Block Starting Addresses

Block Starting Addresses	Cal Data Part Number					
	Standard Module			Module with 7K-Word Option		
	Single	Interleaved		Single	Interleaved	
		Even	Odd		Even	Odd
0	56148015	56148015	56148016			
8K	56148016					
16K	56148017	56148017	56148018		56148032	56148030
24K	56148018			56148030		
32K	56148019	56148019	56148020			
40K	56148020					
48K	56148021	56148021	56148022			
56K	56148022					
64K	56148023	56148023	56148024			
72K	56148024					
80K	56148025	56148025	56148026			
88K	56148026					
96K	56148027	56148027	56148028			
104K	56148028					
112K	56148029	56148029	56148034		56148033	56148031
120K	56148034			56148031		

If the system contains a 4K-word memory unit, this unit must be set to the highest block starting address in the system (i.e., 8K-word modules occupy block starting addresses 0, 8K, 16K, etc.).

4.2 INSTALLATION IN THE PDP-11/05 OR PDP-11/10

CDP-8KX16 modules can be installed directly in the PDP-11/05 or PDP-11/10 chassis with or without an 8K MM11-L memory. The information presented in this subsection is also applicable to installations in the PDP-11/35 expansion chassis.

There are two standard DEC configurations of the models 05 and 10, each with a different backplane:

a. Configuration 1 is wired for 16K of memory with one small-peripheral controller slot (Figure 4-1).
b. Configuration 2 is wired for 8K of memory with four small-peripheral controller slots (Figure 4-2).

The following apply to those installations:

a. The CDP-8KX16 is installed with components toward the top of the cabinet and the core-plane toward the bottom of the cabinet. The keyed connectors prevent reversing the board.
b. Check the CDP-8KX16 for proper orientation (components up, core-plane down) before attempting to insert the board. Excessive force applied to a reversed board can result in damage to the backplane connectors.
c. Always install and remove boards with the system power OFF.
d. A UNIBUS terminator is placed at the end of the UNIBUS, either inside or outside the computer chassis.
e. The Cal Data board adapter assembly should be installed on the CDP-8KX16 to make contact with the card guides of the chassis.

CDP-8KX16 modules can be installed in various combinations with or without an MM11-L. No modification of the computer backplane is necessary and no electrostatic shield is required. The following subsections describe typical memory configurations.

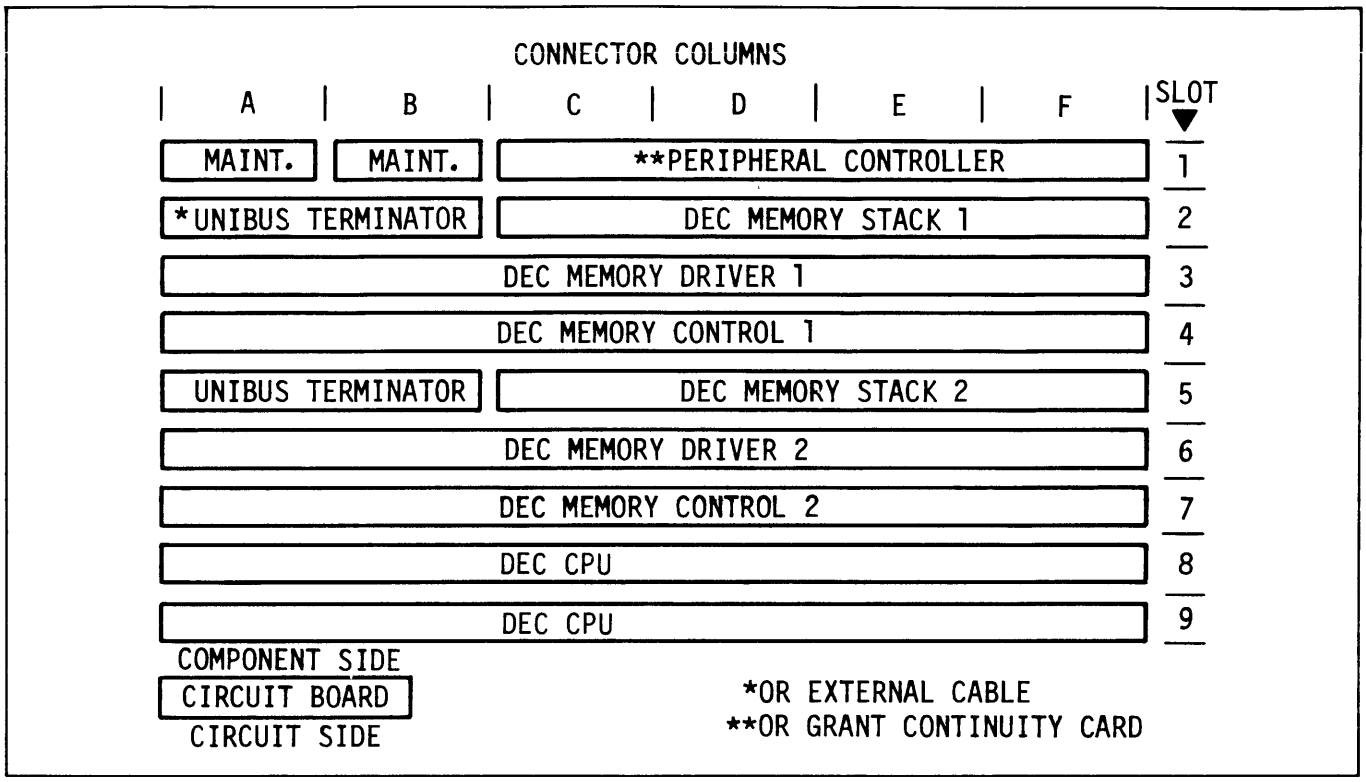


Figure 4-1. DEC PDP-11/05 and PDP-11/10 Standard Module Utilization - Configuration 1 (16K)

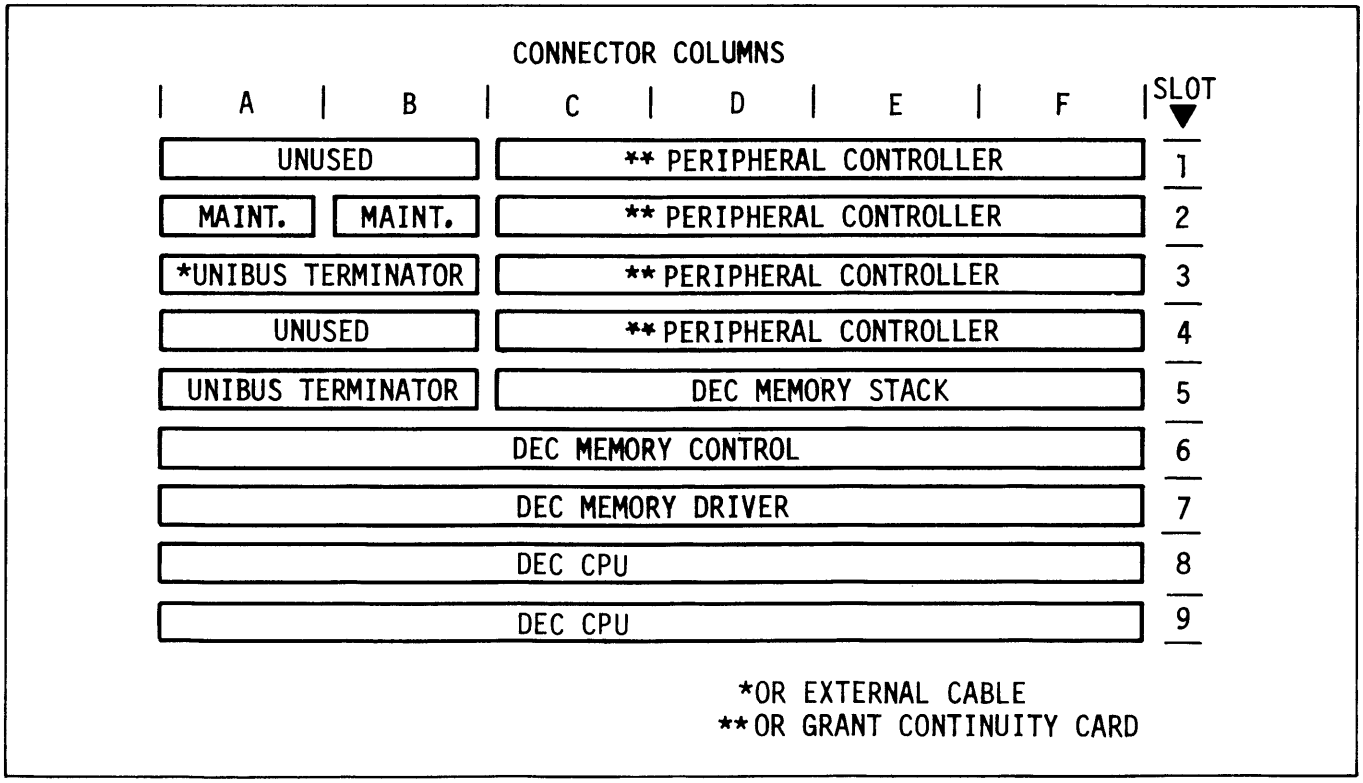


Figure 4-2. DEC PDP-11/05 and PDP-11/10 Standard Module Utilization - Configuration 2 (8K)

4.2.1 24K-Word Configuration 1A

The 24K-word configuration 1A (Figure 4-3) uses three CDP-8KX16 modules and no MM11-L.

The CDP-8KX16 modules are installed in slots 2, 4 and 6. Because of the core-plane board, the adjacent slots (3, 5 and 7, respectively) are blocked, even though no connections to the CDP-8KX16 modules are made in these locations.

For this installation, the UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installing any memories.

UNIBUS signals are available at connectors 3A/3B and 5A/5B. A UNIBUS terminator or external cable can be inserted in either of these locations, although 3A/3B are normally used.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
CPU	8.0	-	Approximate
One CDP-8KX16 operating	2.8	4.40	
Two CDP-8KX16 standby	3.6	0.68	
Terminator	1.2	-	
LOAD	15.6	5.08	
Available reserve	1.4	0.92	
SUPPLY LIMIT	17.0	6.00	

If the UNIBUS terminates in this chassis, an additional 1.2 A (+5 V) must be allowed for a second terminator.

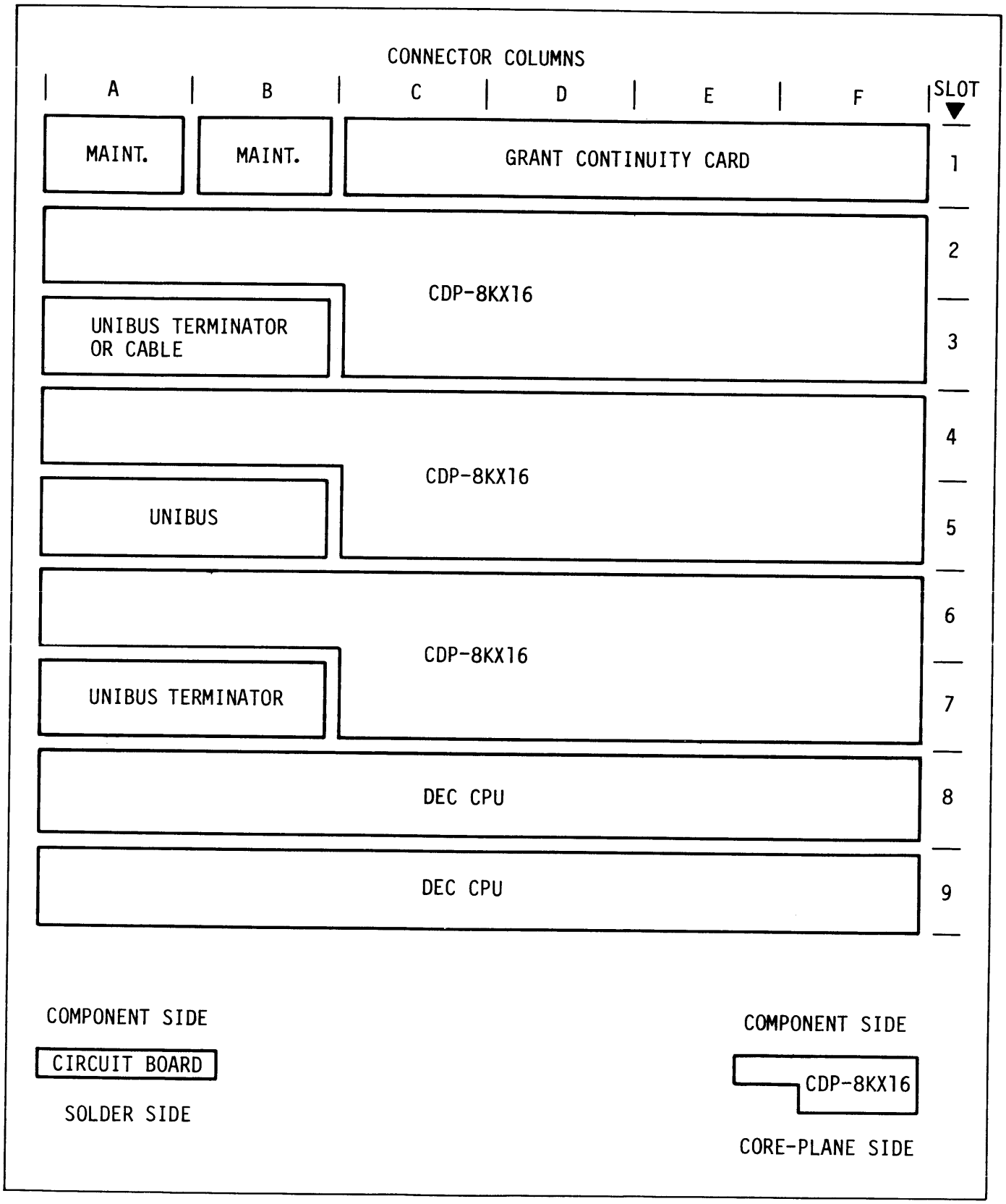


Figure 4-3. 24K-Word Configuration 1A

4.2.2 16K-Word Configuration 1B

The 16K-word configuration 1B (Figure 4-4) uses two CDP-8KX16 modules and no MM11-L.

The CDP-8KX16 modules are installed in slots 4 and 6. The core-plane board blocks the adjacent slots (5 and 7, respectively) even though no connections to the CDP-8KX16 modules are made in these locations.

For this installation, the UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installation of the memories.

UNIBUS signals are available at connects 5A/5B, 3A/3B and 2A/2B. A UNIBUS terminator or external cable can be inserted in any of these locations, although 2A/2B are normally used.

Note that empty slots 2 and 3 are wired to contain the MM11-L core stack and memory driver boards. This wiring does not conform to that used by a peripheral controller board, hence the slots cannot be used for standard DEC quad-height controller assemblies. These slots can, however, be used for expansion to a third CDP-8KX16 module (configuration 1A) and can also contain user-designed controllers on hex-height cards. Such cards obtain all UNIBUS communication from the A and B connectors, and power and ground inputs from the other connectors. Cal Data offers various hex-height controllers, including a general-purpose wire-wrap HEXBOARD, that plug into these slots.

Check that the overall power consumption does not produce an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
CPU	8.0	-	Approximate
One CDP-8KX16 running	2.8	4.40	
One CDP-8KX16 standby	1.8	0.34	
Terminator	1.2	-	Required
LOAD	13.8	4.74	
Available reserve	3.2	1.26	
SUPPLY LIMIT	17.0	6.00	

If the UNIBUS terminates in this chassis, an additional 1.2 A (+5 V) must be allowed for a second terminator.

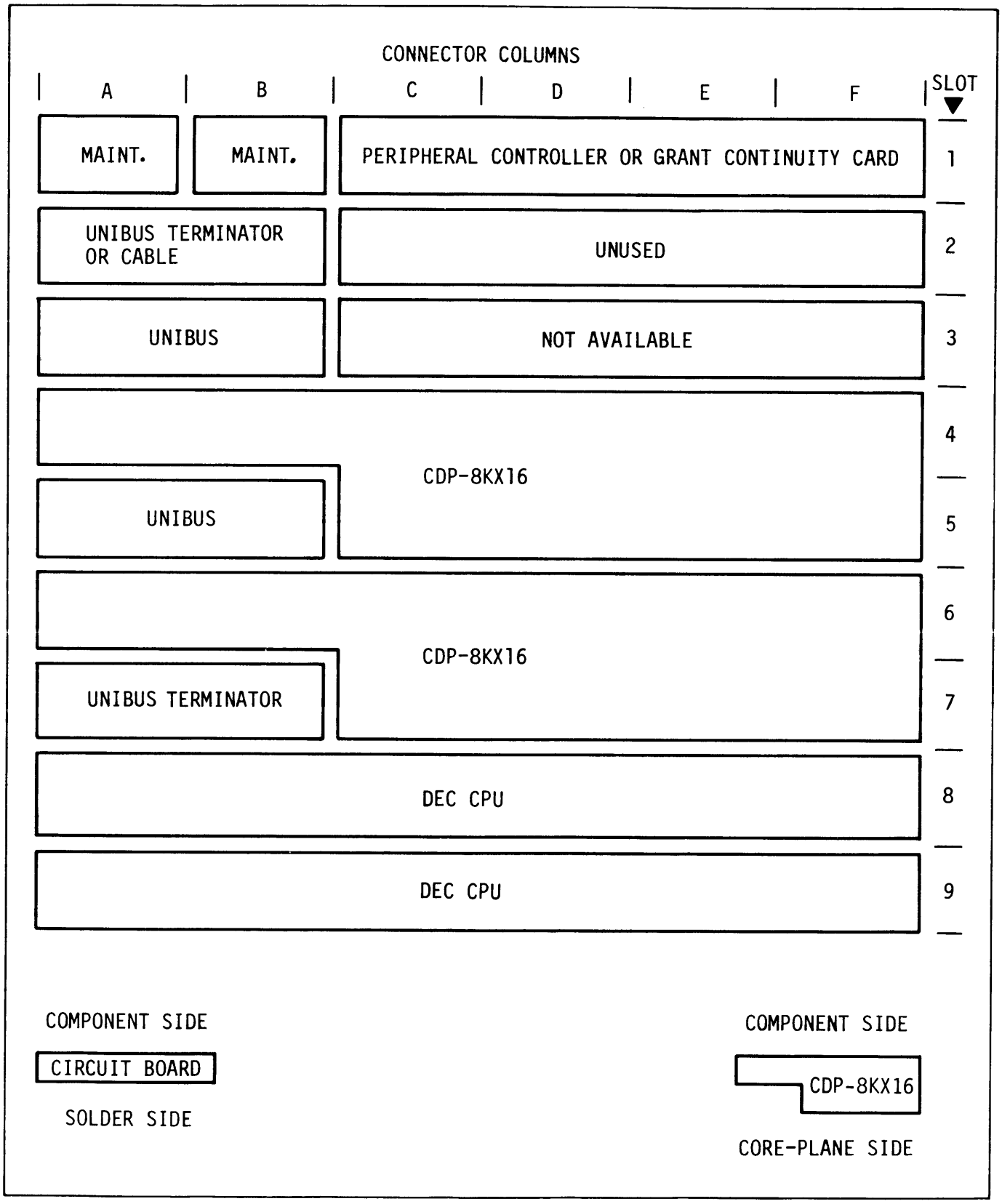


Figure 4-4. 16K-Word Configuration 1B

4.2.3 16K-Word Configuration 1C

The 16K-word configuration 1C (Figure 4-5) uses one CDP-8KX16 module and one MM11-L module.

The CDP-8KX16 module is installed in slot 3. The core-plane board blocks adjacent slot 4 even though no connection is made to the CDP-8KX16 in this location. The UNIBUS terminator remains in connectors 5A/5B.

UNIBUS signals are available at connectors 2A/2B and 4A/4B. A UNIBUS terminator or external cable can be inserted in either of these locations, although 2A/2B are normally used.

Note that empty slot 2 is wired to contain the MM11-L core stack. The wiring in this location does not conform to that used by a peripheral controller, hence the slot cannot be used for standard DEC quad-height controller assemblies. This slot can, however, be used for a user-designed controller on a HEXBOARD. Such a board obtains all UNIBUS communication from connectors 2A/2B, and power and ground inputs from the other connectors. Cal Data offers various hex-height controllers that interface in this slot.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
CPU	8.0	-	Approximate
One MM11-L operating	3.4	6.00	
One CDP-8KX16 standby	1.8	0.34	
Terminator	1.2	-	Required
LOAD	14.4	6.34	
Available reserve	2.6	-(0.34)	
SUPPLY LIMIT	17.0	6.00	

Note that the -15 V is over the supply limit in this configuration. The standby consumption on -15 V of a second MM11-L would be 0.5 A versus the 0.34 A of the CDP-8KX16, hence, the latter presents *less* of an overload than using two MM11-L memories (the CDP-8KX16 power rating given is for worst-case conditions). Should difficulties be experienced in running the -15 V supply above the rated load, consult the computer manufacturer concerning provisions for normal operation of two MM11-L units under the same conditions.

If the UNIBUS terminates in this chassis, an additional 1.2 A (+5 V) must be allowed for a second terminator.

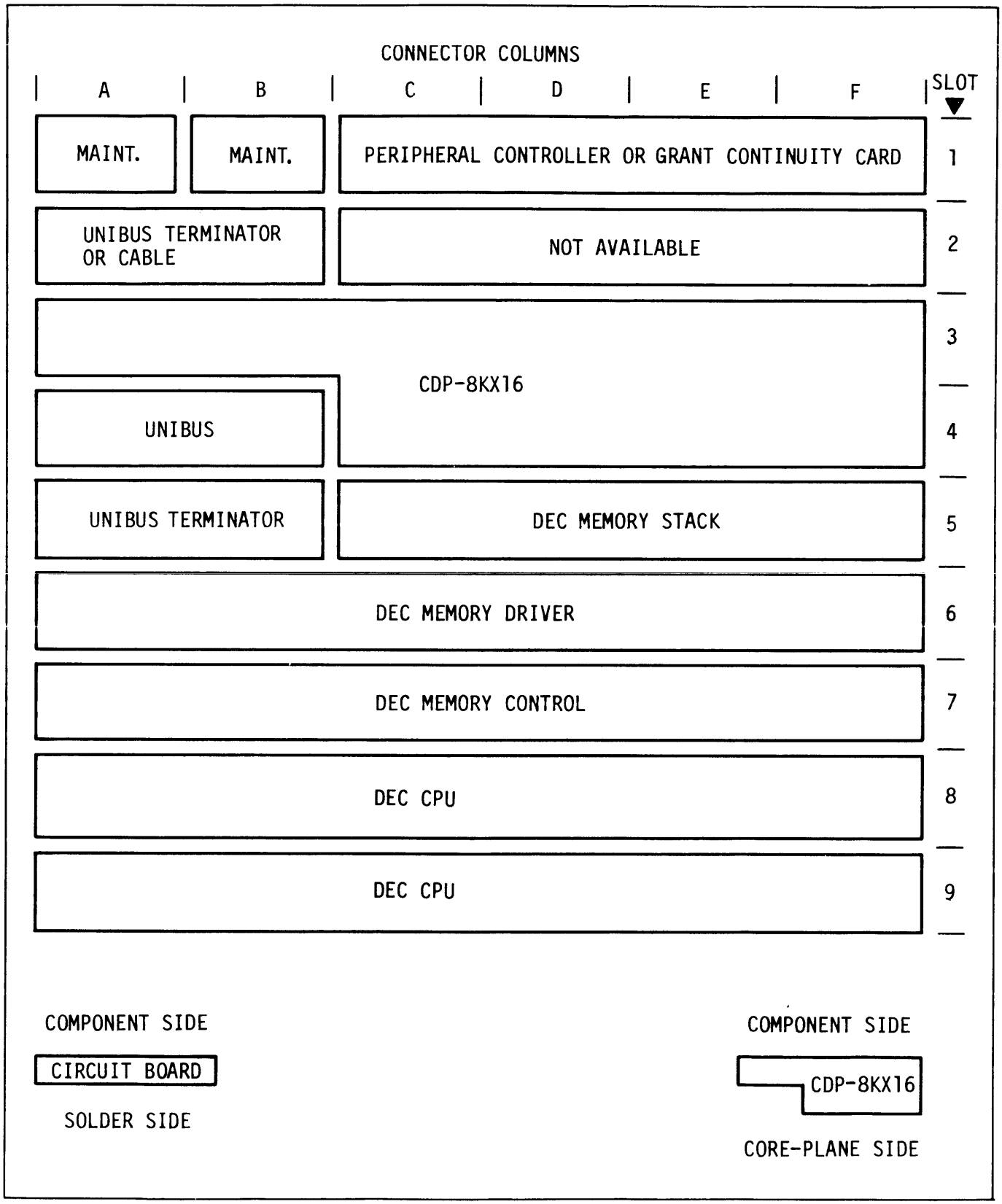


Figure 4-5. 16K-Word Configuration 1C

4.2.4 16K-Word Configuration 2A

The 16K-word configuration 2A (Figure 4-6) has two CDP-8KX16 modules and two peripheral controllers.

The CDP-8KX16 modules are installed in slots 4 and 6. Because of the core-plane board, the adjacent slots (5 and 7, respectively) are blocked even though no connections to the CDP-8KX16 modules are made in these locations.

For this installation, the UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installing any memories.

UNIBUS signals are available at connectors 3A/3B and 5A/5B. A UNIBUS terminator or external cable can be inserted in either of these locations, although 3A/3B are normally used.

Two small-peripheral controller slots are available for use, provided that the overall system power consumption does not cause an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
CPU	8.0	-	Approximate
One CDP-8KX16 operating	2.8	4.40	
One CDP-8KX16 standby	1.8	0.34	
Terminator	1.2	-	Required
LOAD	13.8	4.74	
Available reserve	3.2	1.26	
SUPPLY LIMIT	17.0	6.00	

If the UNIBUS terminates in this chassis, an additional 1.2 A (+5 V) must be allowed for a second terminator.

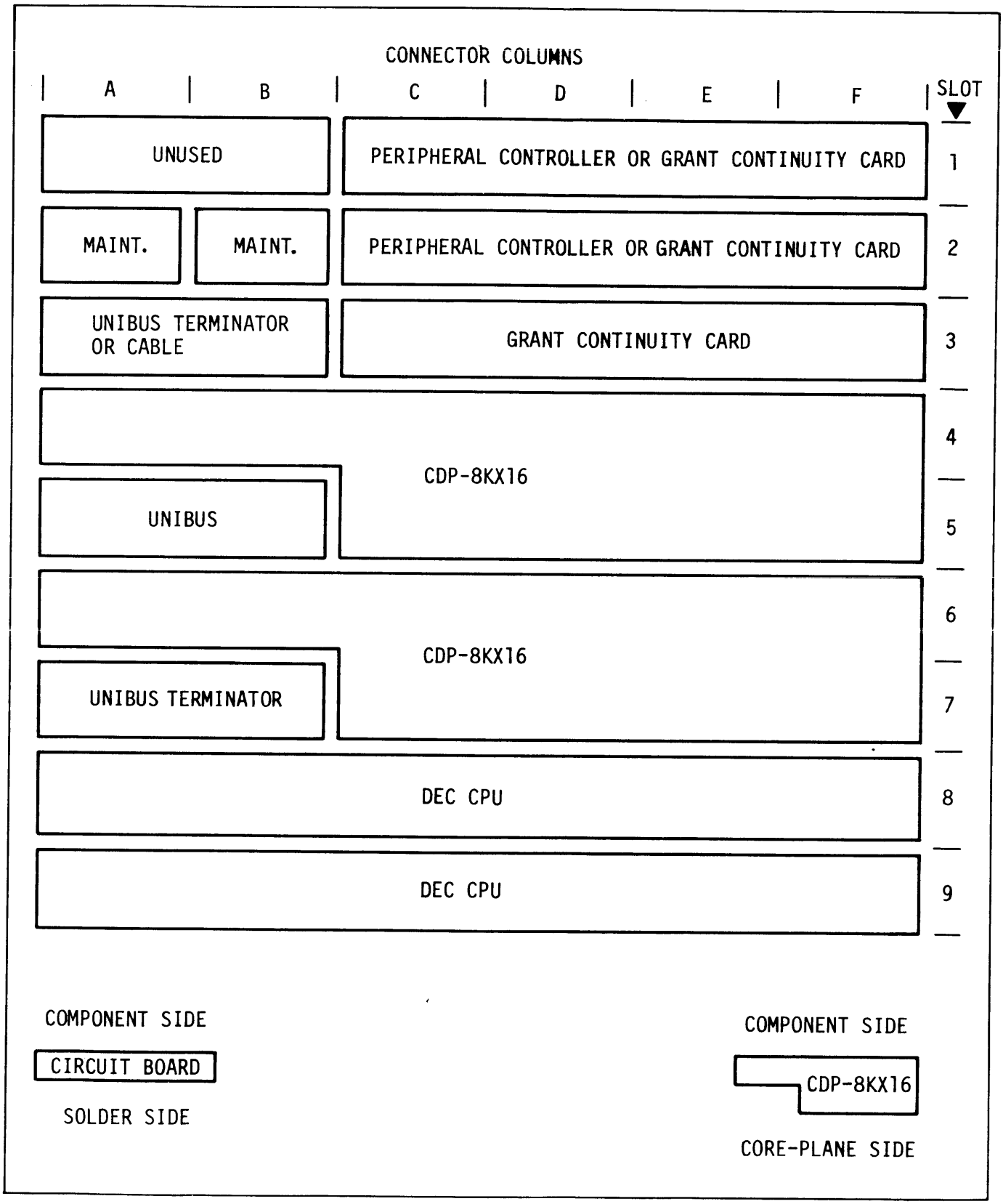


Figure 4-6. 16K-Word Configuration 2A.

4.2.5 16K-Word Configuration 2B

The 16K-word configuration 2B (Figure 4-7) has one CDP-8KX16 module, one MM11-L module and one peripheral controller.

The CDP-8KX16 module is installed in slot 3. Because of the core-plane board, the adjacent slot 4 is blocked even though no connections to the CDP-8KX16 are made in this location.

UNIBUS signals are available at connectors 2A/2B and 4A/4B. A UNIBUS terminator or external cable can be inserted in either of these locations, although 2A/2B are normally used.

One small-peripheral controller slot is available for use, provided that the overall system +5 V power consumption does not cause an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
CPU	8.0	-	Approximate
One MM11-L operating	3.4	6.00	
One CDP-8KX16 standby	1.8	0.34	
Terminator	1.2	-	Required
LOAD	14.4	6.34	
Available reserve	2.6	-(0.34)	
SUPPLY LIMIT	17.0	6.00	

Note that the -15 V is over the rated load in this configuration. The standby consumption on -15 V of a second MM11-L would be 0.5 A versus the 0.34 A of the CDP-8KX16, hence the latter presents *less* of an overload than using two MM11-L memories (the CDP-8KX16 power rating given is for worst-case conditions). Should difficulties be experienced in running with the -15 V supply above the rated load, consult the computer manufacturer concerning provisions for normal operation of two MM11-L units under the same conditions.

If the UNIBUS terminates in this chassis, an additional 1.2 A (+5 V) must be allowed for a second terminator.

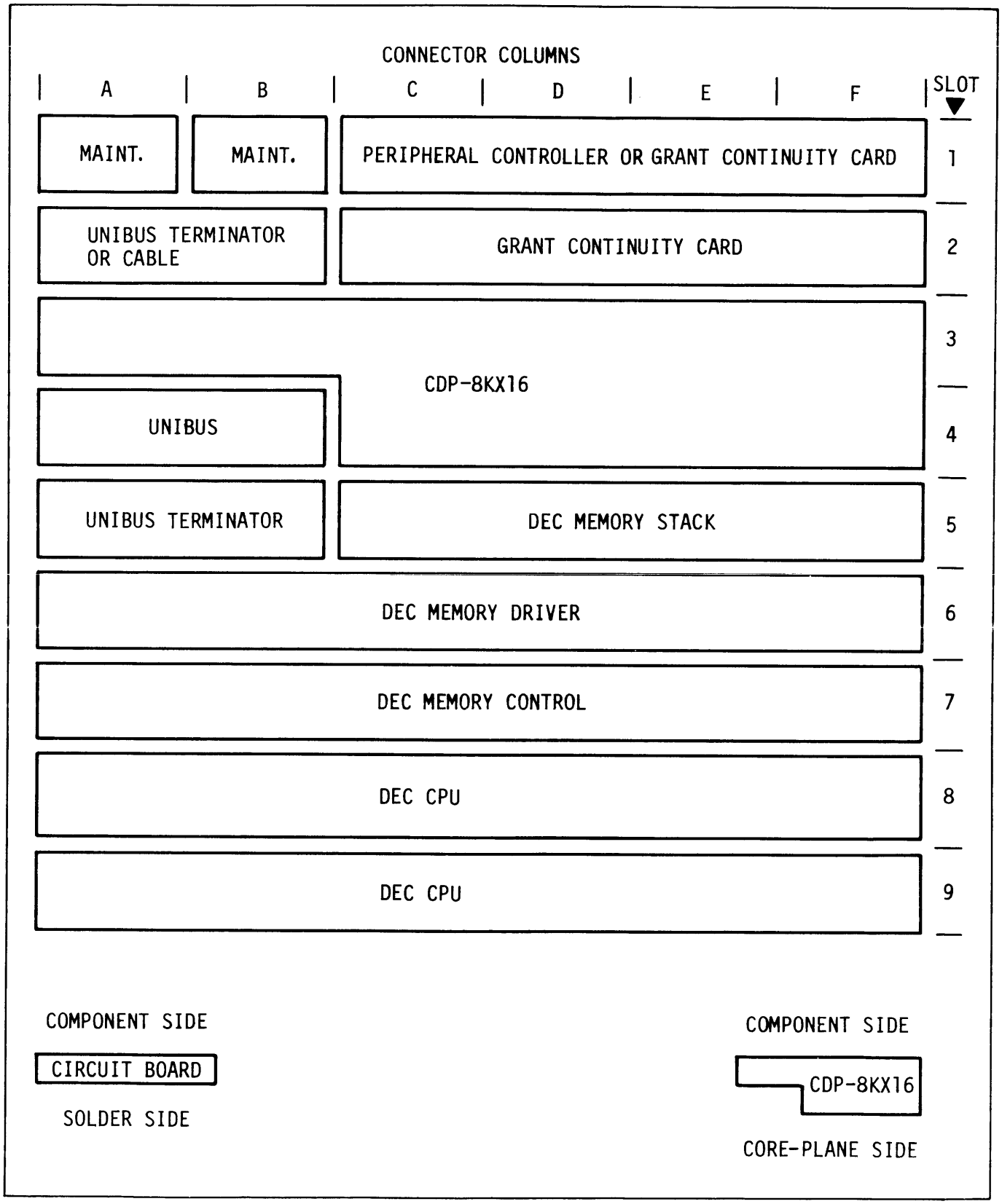


Figure 4-7. 16K-Word Configuration 2B

4.2.6 8K-Word Configuration 2C

The 8K-word configuration 2C (Figure 4-8) has one CDP-8KX16 module and four peripheral controllers.

The CDP-8KX16 is installed in slot 6. Because of the core-plane board, the adjacent slot 7 is blocked even though no connections to the CDP-8KX16 are made in this location.

For this installation, the UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installing the memory.

UNIBUS signals are available at connectors 3A/3B, 4A/4B and 5A/5B. A UNIBUS terminator or external cable can be installed in any of these locations, although 3A/3B are normally used.

Four small-peripheral controller slots are available for use, provided that the overall system power consumption does not cause an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
CPU	8.0	-	Approximate
One CDP-8KX16 operating	2.8	4.4	
Terminator	1.2	-	Required
LOAD	12.0	4.4	
Available reserve	5.0	1.6	
SUPPLY LIMIT	17.0	6.0	

If the UNIBUS terminates in this chassis, an additional 1.2 A (+5 V) must be allowed for a second terminator.

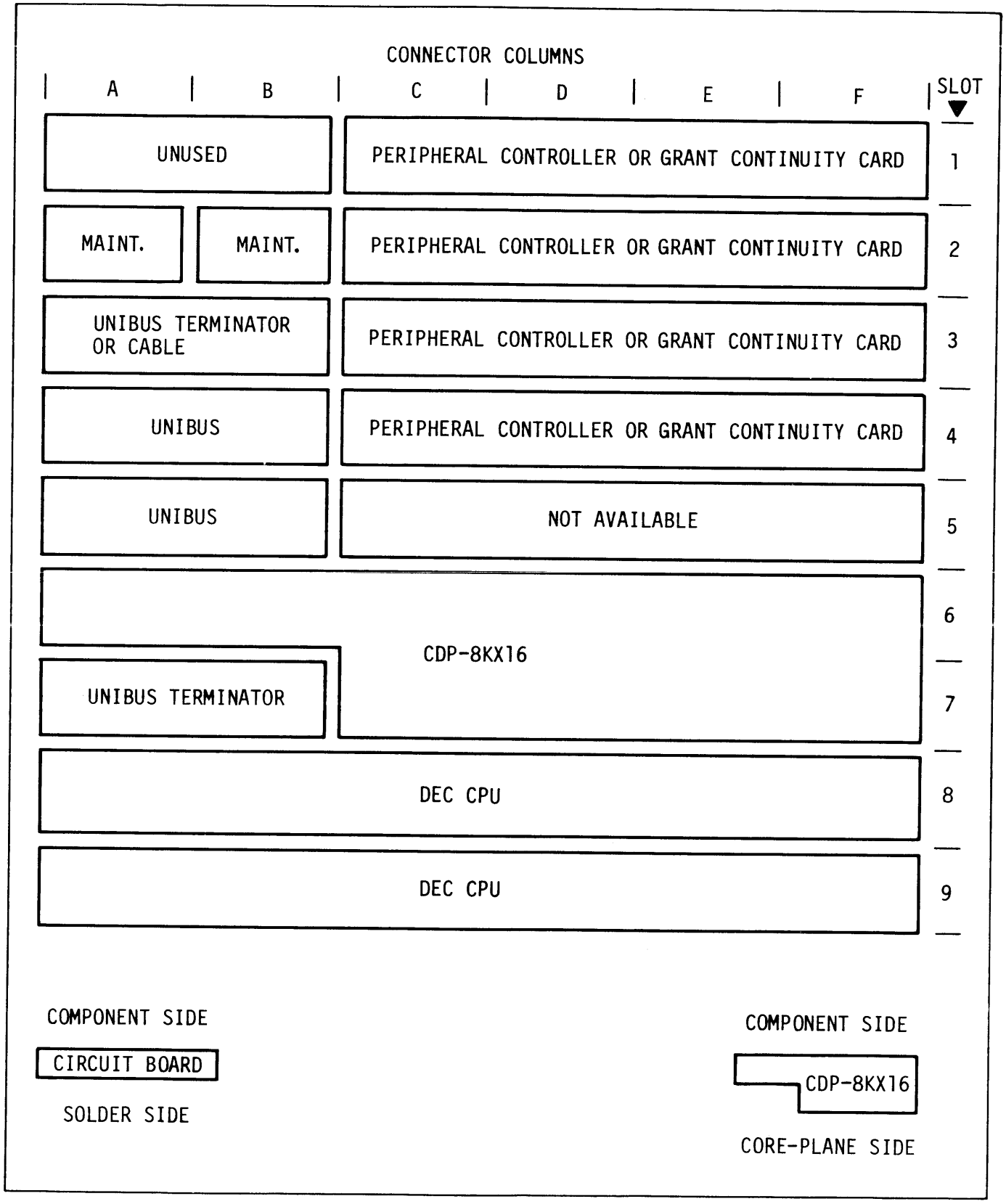


Figure 4-8. 8K-Word Configuration 2C

4.3 INSTALLATION IN THE PDP-11/35, PDP-11/40 OR PDP-11/45

CDP-8KX16 modules can be installed directly in the PDP-11/40 mounting box (BA11-FC). Figure 4-9 shows a view of the module side of the chassis, Figure 4-10 shows a multiple-module installation and Figure 4-11 shows the backplane connectors.

Although the material in this subsection is a specific description of CDP-8KX16 installations in the PDP-11/40, it is also applicable to the PDP-11/35 and the PDP-11/45, with minor modifications.

The basic system contains two double system units for board installation, each unit containing nine rows of connectors. The first nine-slot unit contains the CPU and associated option boards and is not used for memory installation.

The second double system unit is prewired for one to three MM11-L memory modules. Each MM11-L module is a three-board assembly consisting of a stack, memory driver and control board. Thus, this double system unit generally contains 8K to 24K of MM11-L memory.

The remainder of the BA11-FC box can be used for single or double system units for additional memory or peripheral interfaces. Each double system unit is equivalent to five single system units.

This section presents typical installation detail for mounting CDP-8KX16 modules in the assembly with or without MM11-L memories. Memory expansion beyond the basic double system unit for memory is identical when other MM11-L backplanes are installed. The user can use the information provided to determine the installation method required for other types of system mounting units.

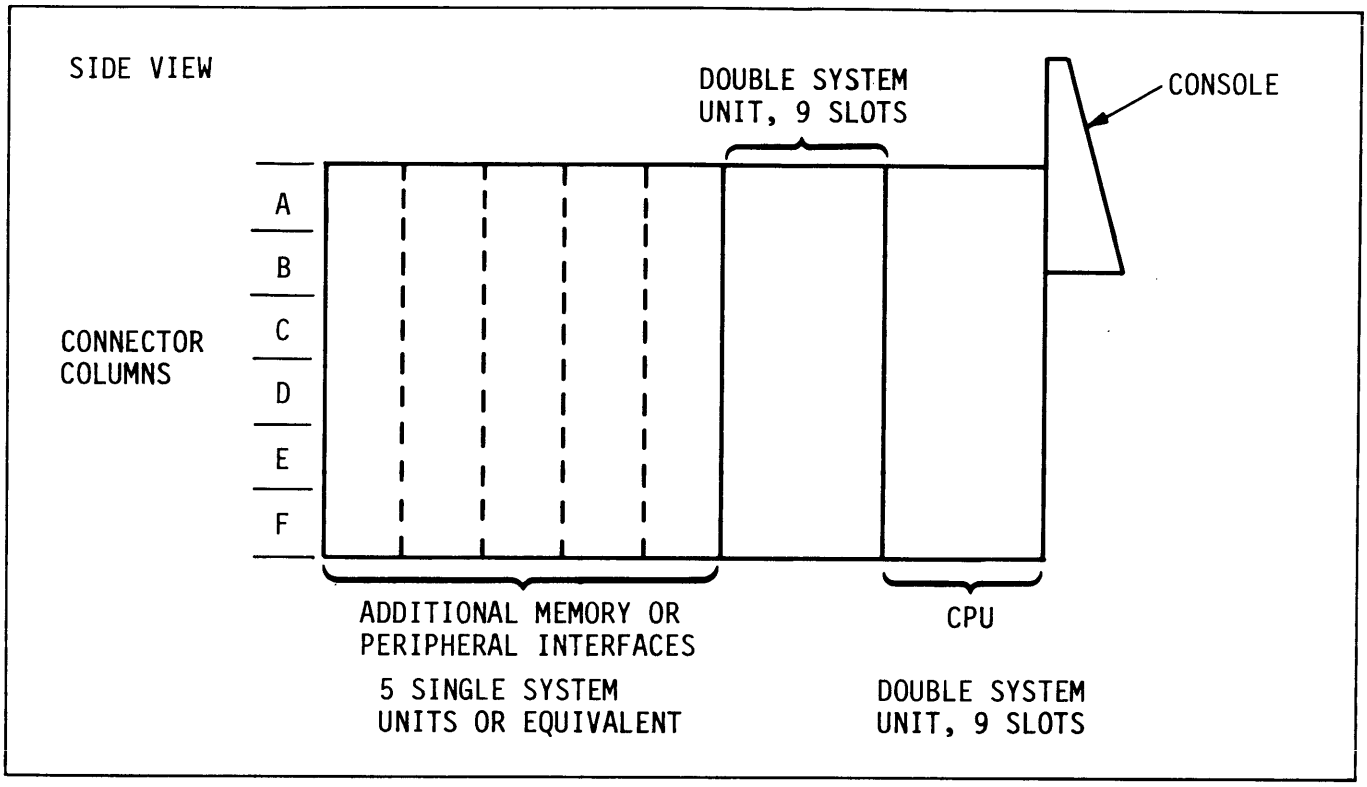


Figure 4-9. PDP-11/40 Mounting Box

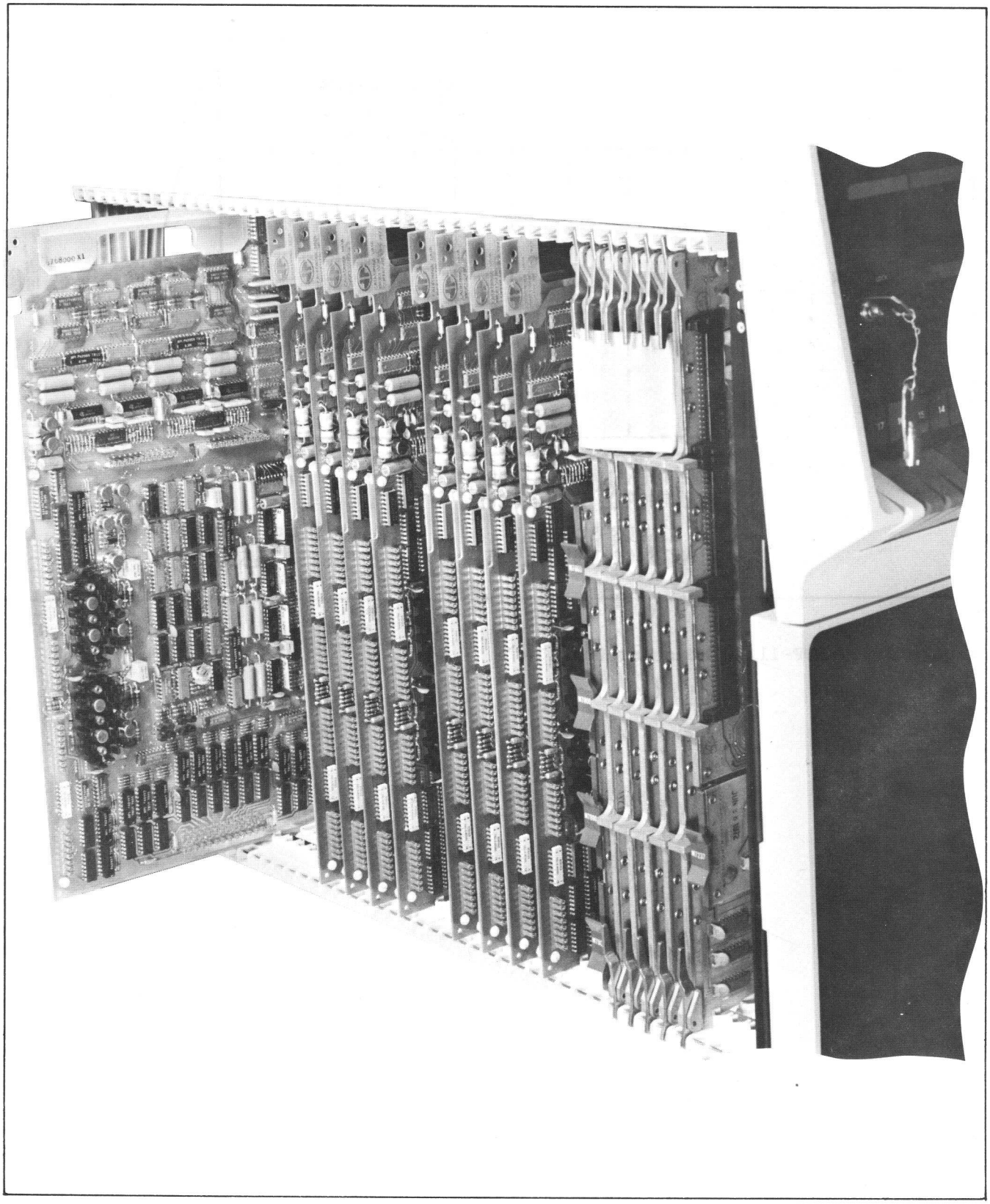


Figure 4-10. PDP-11/40 Multiple-Module Installation

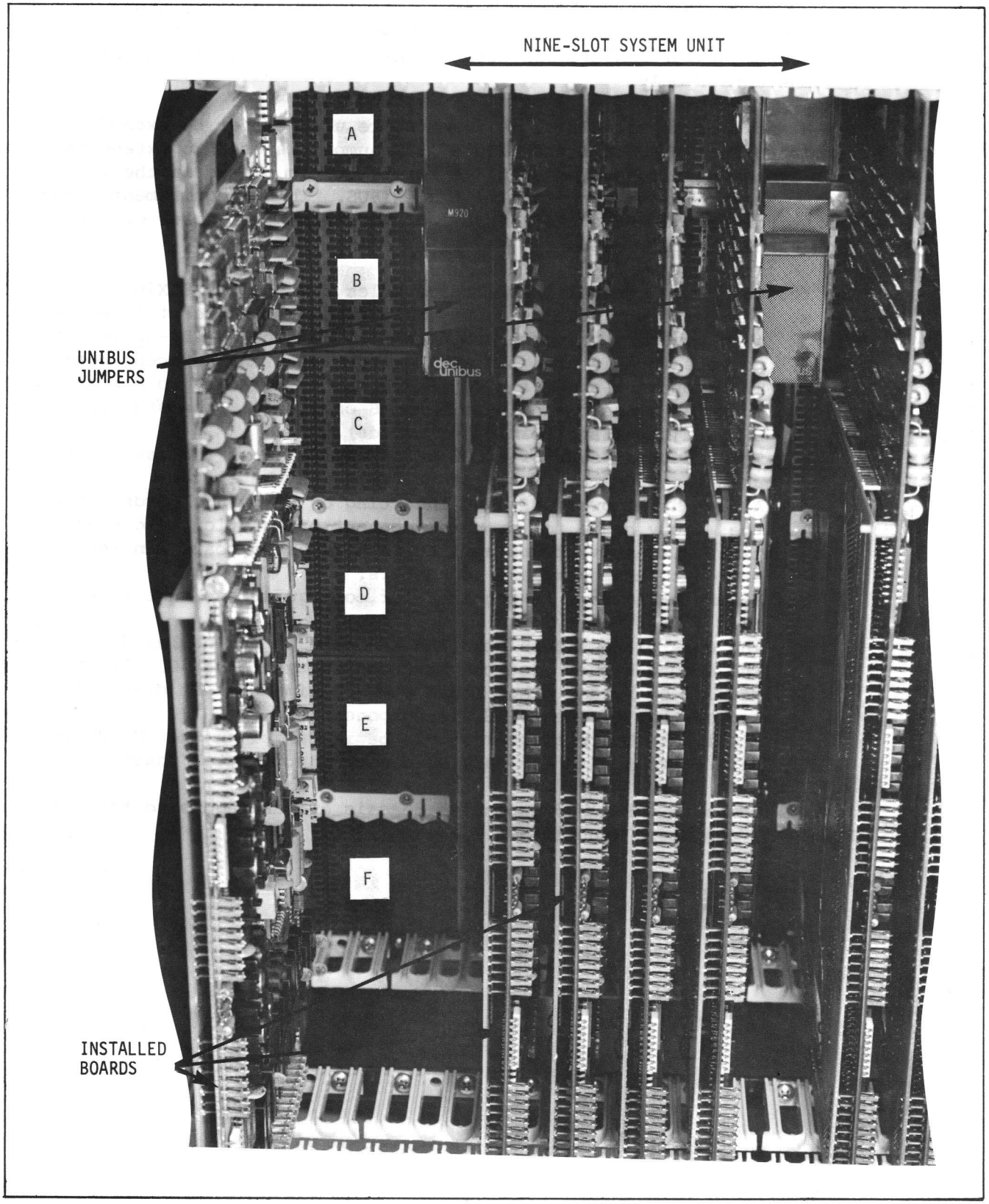


Figure 4-11. PDP-11/40 Backplane Connector Scheme

Figure 4-12 shows slot allocation for a fully-expanded 24K assembly. The MM11-L memory driver and control/data boards are hex-height and use all six connectors of a slot. The stack board is quad-height and occupies columns C to F only.

The A and B connectors in slots 1 and 9 are used either to extend or to terminate the UNIBUS. A standard UNIBUS jumper is used to extend the bus from system unit to system unit. A terminator is placed in the last system unit at or near the end of the UNIBUS. These requirements, and the number of MM11-L modules installed, determine the number of CDP-8KX16 modules that can be used.

The following are general installation rules for the CDP-8KX16:

a. The component side of a CDP-8KX16 cannot be adjacent to a board that occupies connector columns C to F, because CDP-8KX16 components in this area can make contact with the adjacent board.
b. The component side of a CDP-8KX16 can be adjacent to a board that occupies connector columns A and B only (e.g., the standard UNIBUS jumper and terminator boards).
c. The component side of a CDP-8KX16 always faces the same direction as the components of all other boards in the system.
d. Always have power OFF when inserting or removing boards. Check the memory board for proper component orientation before insertion. Excessive force applied to a reversed board can result in damage to the backplane connectors.
e. Memory management is required for configurations that total more than 32K of memory.
f. The core-plane side blocks the adjacent higher-numbered slot. The second-higher slot can be occupied by another CDP-8KX16 module, or by any other board whose maximum height does not exceed that of the CDP-8KX16 components.
g. A Cal Data board adapter should be installed on the CDP-8KX16 to make contact with the card guides of the computer chassis.

Installations in PDP-11/35 expansion chassis are analagous to those in PDP-11/05 computers (subsection 4.2).

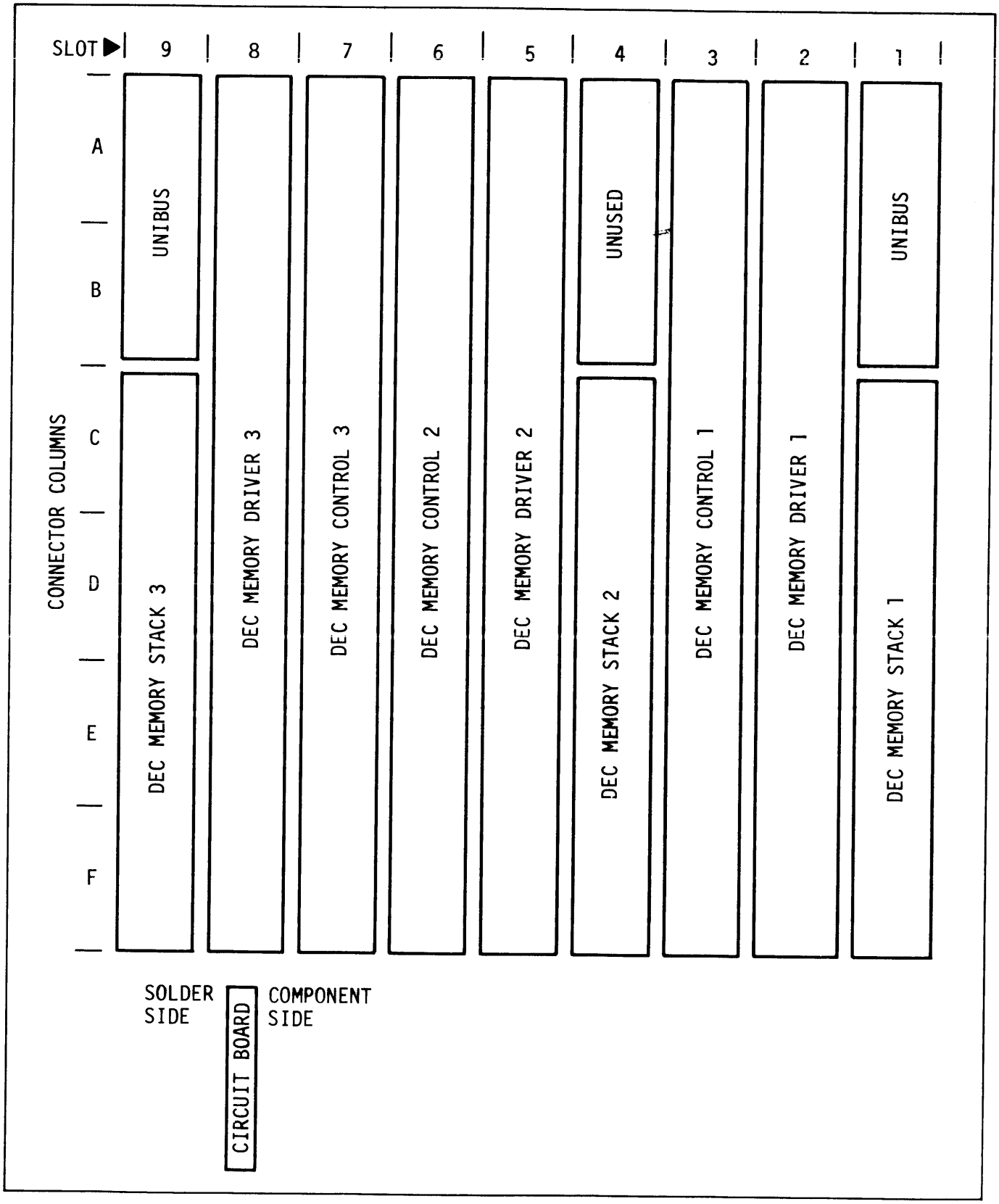


Figure 4-12. DEC Assembly Utilization (24K)

4.3.1 32K-Word Configuration 1

The 32K-word configuration 1 (Figure 4-13) has one MM11-L and three CDP-8KX16 modules in a nine-slot system unit.

The CPU can address only the first 28K core locations. Addressable memory capacity generally cannot be expanded beyond 28K without the addition of memory management; however, the Cal Data 7K-word option can be installed in a CDP-8KX16 module (or pair of interleaved modules) to obtain a 31K-word addressable capacity without memory management (with the last 1K-word addresses allocated to I/O devices).

CDP-8KX16 modules are installed in slots 5, 7 and 9. A UNIBUS terminator is installed in slot 8 if the bus is to be terminated at that point. If the bus is to be extended, a UNIBUS extension cable is used rather than the jumper, since connectors 9A/9B are not available. The CDP-8KX16 board is notched at the top to provide adequate clearance for the cable. Slot 4 is left empty to prevent CDP-8KX16 components from touching the board in slot 3.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One MM11-L operating	3.4	6.00	
Three CDP-8KX16 standby	5.4	1.02	
MINIMUM LOAD	8.8	7.02	
Terminator	1.2	-	If required
TOTAL LOAD	9.7	7.02	Noninterleaved
Interleaved	0.9	4.10	Optional
INTERLEAVE LOAD	10.6	11.12	

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

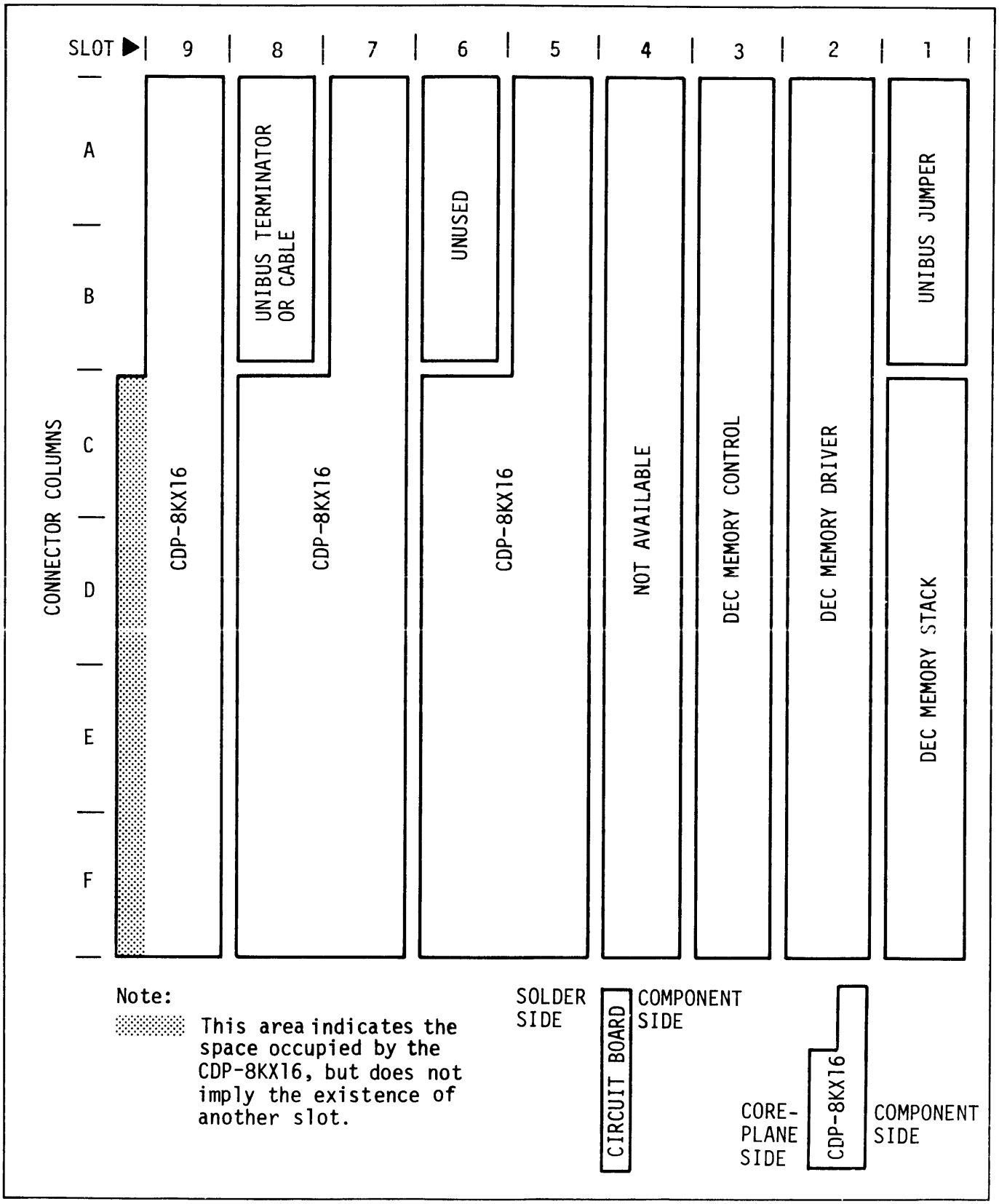


Figure 4-13. 32K-Word Configuration 1

4.3.2 32K-Word Configuration 2

The 32K-word configuration 2 (Figure 4-14) has four CDP-8KX16 modules in a nine-slot system unit with no MM11-L.

The CPU can address only the first 28K core locations. Addressable memory capacity generally cannot be expanded beyond 28K without the addition of memory management; however, the Cal Data 7K-word option can be installed in a CDP-8KX16 module (or pair of interleaved modules) to obtain a 31K-word addressable capacity without memory management (with the last 1K-word addresses allocated to I/O devices).

CDP-8KX16 modules are installed in slots 2, 4, 6 and 8. Slots 1 and 9 are empty, except that the UNIBUS is jumpered into slot 1 and is either extended or terminated in slot 9.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One CDP-8KX16 operating	2.6	4.40	
Three CDP-8KX16 standby	5.4	1.02	
MINIMUM LOAD	8.0	5.42	
Terminator	1.2	-	If required
TOTAL LOAD	9.2	5.42	Noninterleaved
Interleaved	0.9	4.10	Optional
INTERLEAVE LOAD	10.1	9.52	

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

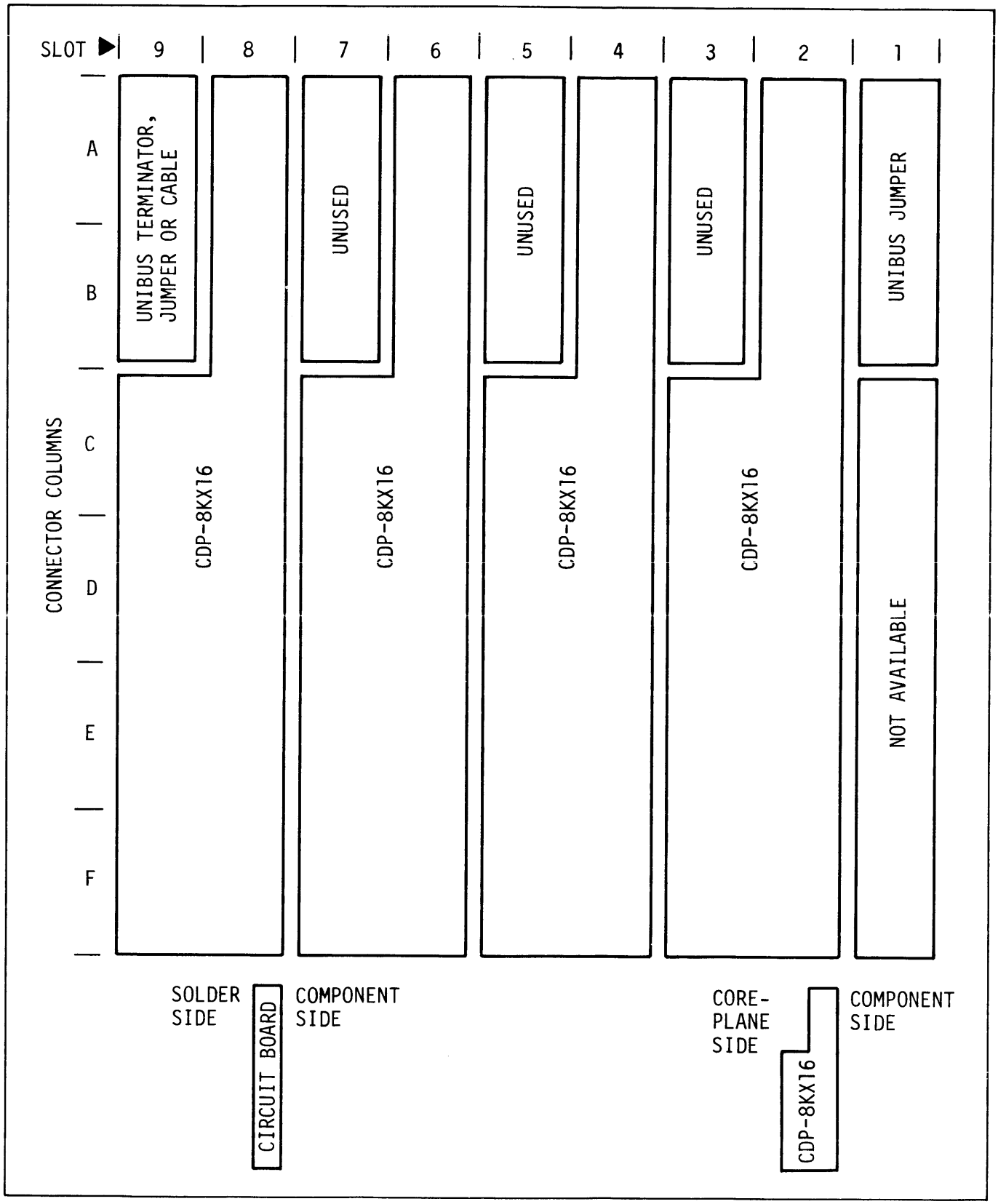


Figure 4-14. 32K-Word Configuration 2

4.3.3 24K-Word Configuration 1

The 24K-word configuration 1 (Figure 4-15) has two CDP-8KX16 modules with one MM11-L in a nine-slot system unit.

CDP-8KX16 modules are installed in slots 5 and 7. The UNIBUS is jumpered into slot 1 and is either extended or terminated in slot 9. Slot 4 is left empty to prevent CDP-8KX16 components from touching the board in slot 3.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One MM11-L operating	3.0	6.00	
Two CDP-8KX16 standby	3.6	0.68	
MINIMUM LOAD	6.6	6.68	
Terminator	1.2	-	
TOTAL LOAD	7.8	6.68	Noninterleaved
Interleaved	0.9	4.10	Optional
INTERLEAVE LOAD	8.7	10.78	

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

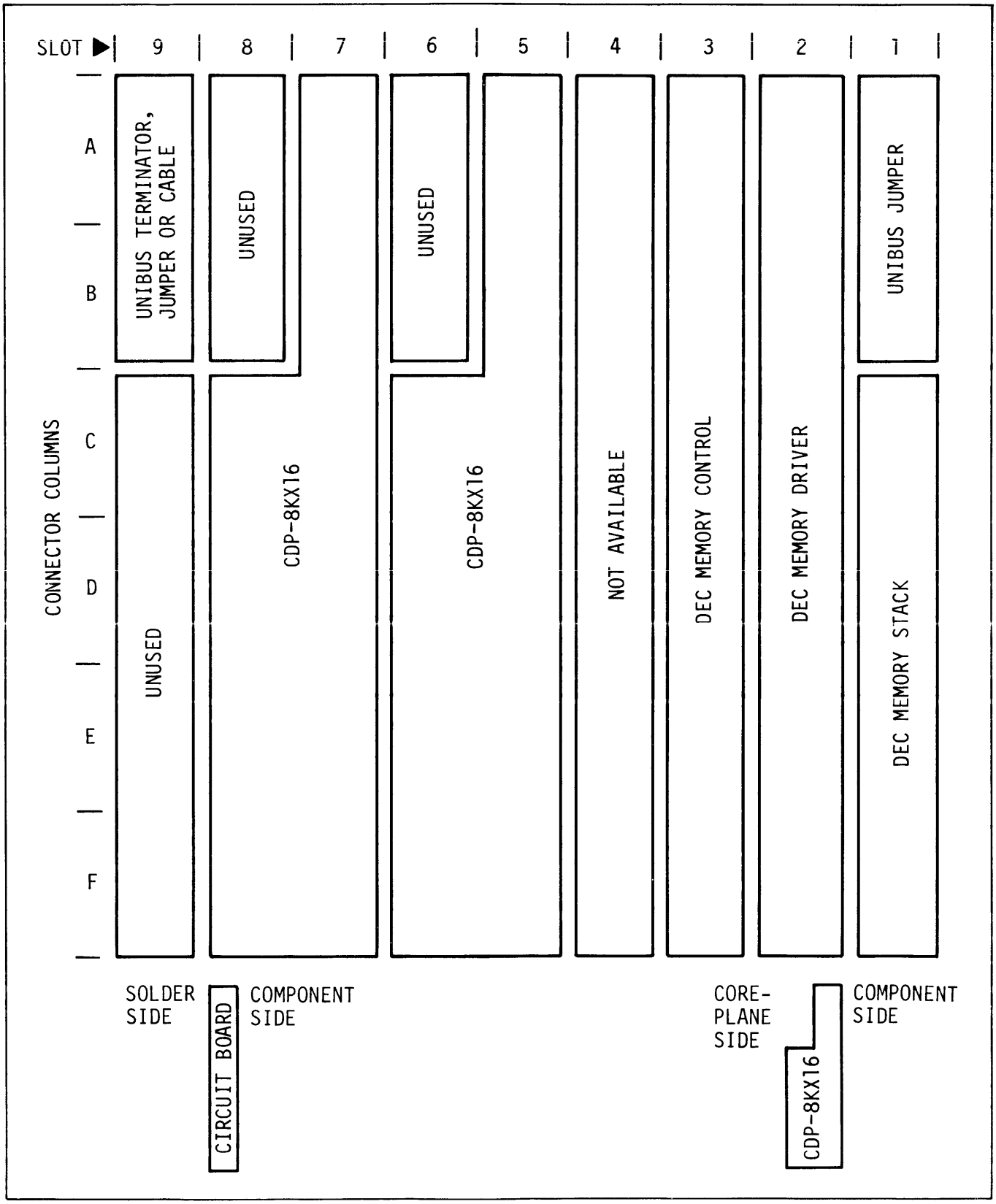


Figure 4-15. 24K-Word Configuration 1

4.3.4 24K-Word Configuration 2

The 24K-word configuration 2 (Figure 4-16) has one CDP-8KX16 and two MM11-L modules in a nine-slot system unit.

The MM11-L boards occupy slots 1 to 6. The CDP-8KX16 is installed in slot 8. The UNIBUS is jumpered into slot 1 and is either extended or terminated in slot 9. Slot 7 is left empty to prevent CDP-8KX16 components from touching the board in slot 6.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One MM11-L operating	3.4	6.00	
One MM11-L standby	1.7	0.50	
One CDP-8KX16 standby	1.8	0.34	
MINIMUM LOAD	6.9	6.84	
Terminator	1.2	-	If required
TOTAL LOAD	8.1	6.84	Noninterleaved

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

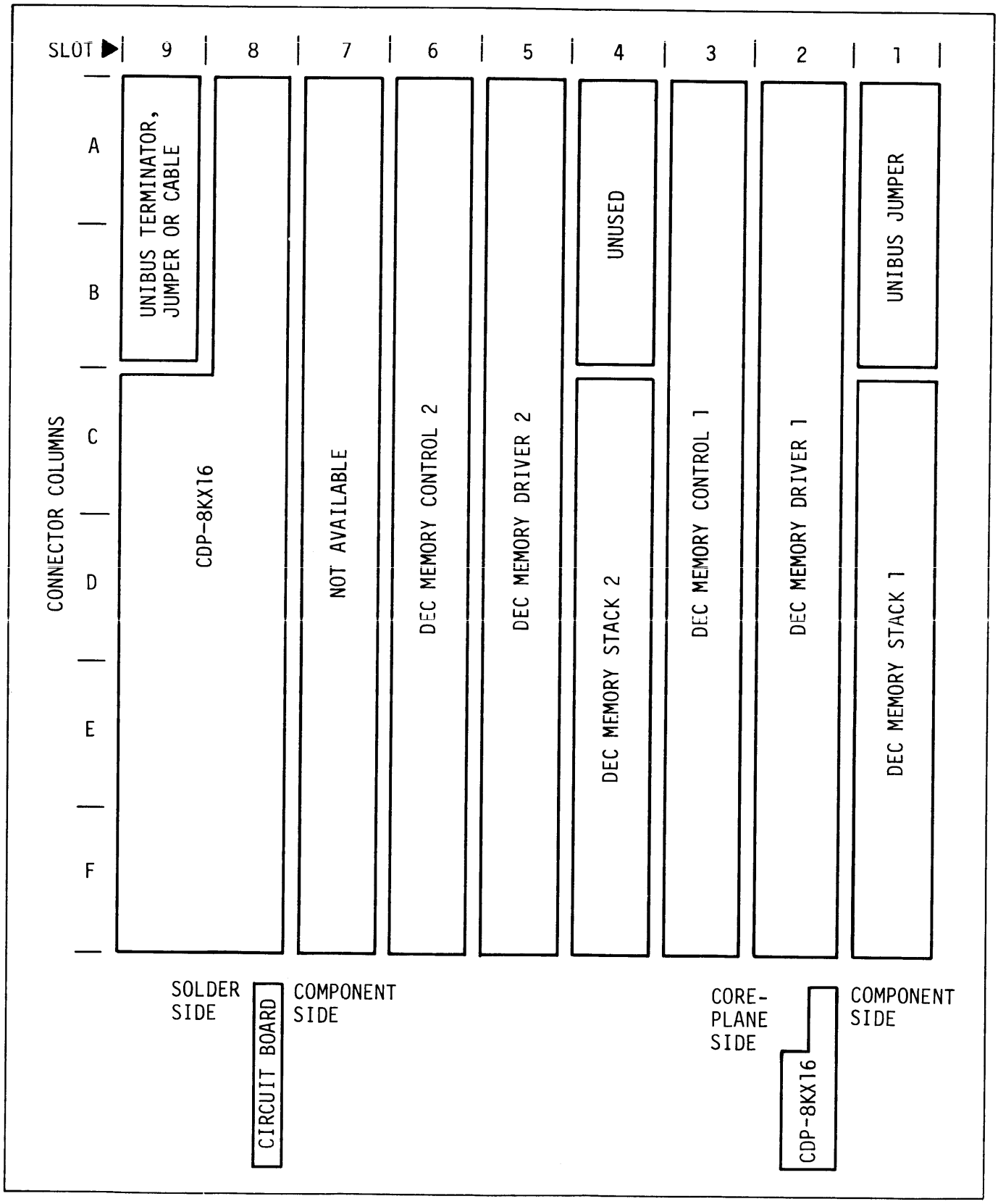


Figure 4-16. 24K-Word Configuration 2

4.4 INSTALLATION IN THE CAL DATA CHASSIS

Up to eight CDP-8KX16 modules can be installed in a typical Cal Data chassis, as shown in Figure 4-17.

Slots 1 to 5 are closely spaced for the CPU and related boards. Slots 6 and up are on wider centers so that each slot can accomodate either a CDP-8KX16 module (including core-plane board), a controller board or an option board (slots 6 and 7 only). If a memory management unit (MMU) is present, it must be installed in slot 6. The MMU is required for memory expansion beyond 32K words.

When a chassis contains both CDP-8KX16 modules and controllers, the memory modules are installed to occupy available slots close to the CPU, followed by the controllers toward the power supply.

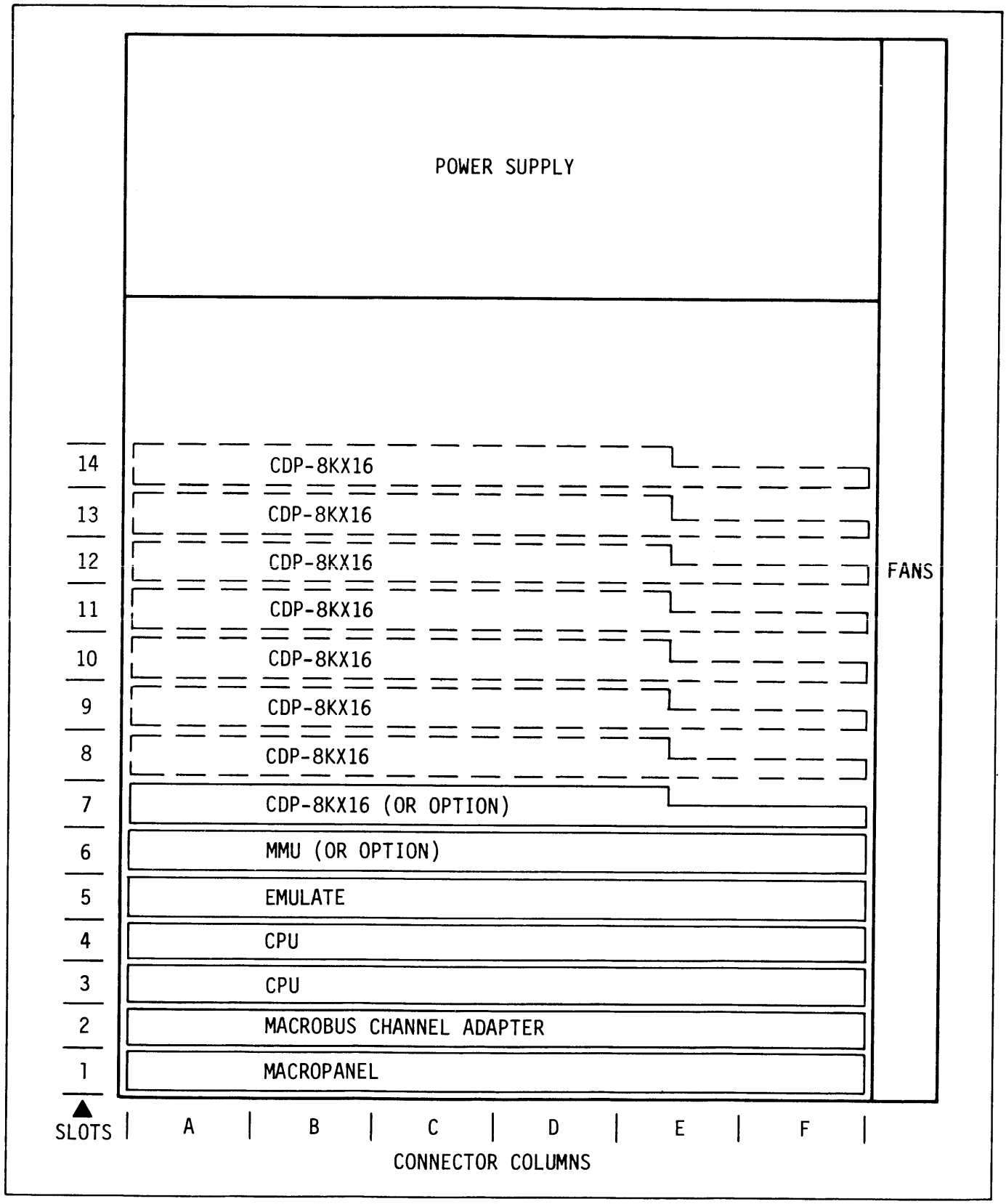


Figure 4-17. Typical Cal Data Chassis Layout

SECTION 5
MAINTENANCE

5.1 GENERAL

This section describes preventive and corrective maintenance procedures that apply to the CDP-8KX16. In general, corrective maintenance is limited to isolation of a fault to a specific CDP-8KX16 module, followed by replacement of the module. Troubleshooting may then be used to verify that the suspected module is malfunctioning and to help diagnose the specific problem. Repair should be conducted at the factory or by an authorized Cal Data representative.

5.2 PREVENTIVE MAINTENANCE

The CDP-8KX16 is a reliable solid-state device designed to perform continuously for many years without degredation. Preventive maintenance consists of performing the following tasks every six months:

a. Inspect the CDP-8KX16 for damaged wires, components or other obvious defects.
b. Using a low-pressure source of air (75 psi one foot from board, or 5 kg/cm^2 30 cm from board), blow off accumulated dust and foreign matter.
c. Check the +5 Vdc and -15 Vdc inputs to the memory. They should be within 15 percent.

5.3 CORRECTIVE MAINTENANCE

Repair or adjustment of the CDP-8KX16 in the field is not recommended. Separation of the core-plane board from the drive board or changing the adjustment of any potentiometer breaks factor seals on the module and voids the warranty.

If a malfunction is detected, replace the CDP-8KX16 with a spare module known to be operating properly and return the malfunctioning module for repair to California Data Prociessors or an authorized representative.

Malfunctions can be detected with the aid of test programs and by signal troubleshooting described in the following paragraphs.

5.3.1 Test Program

When the CDP-8KX16 is installed in any PDP-11 computer or Cal Data 1 equivalent, it can be tested by the DEC program MAINDEC-11-DZQMB 0-124K MEMORY EXERCISER. This program tests contiguous memory addresses from 0 to 0757776, verifying that each address is unique (address test) and that each location can be read from or written into reliably (worst-case noise test). If memory management is installed, all testing is performed with memory management enabled.

The 11 FAMILY INSTRUCTION EXERCISER DZQKA, and the KT11-C/KT11-D LOGIC TEST, if memory management is installed, are considered preliminary to the memory exerciser.

5.3.1.1 Program Description

The program verifies each location from 020000 to the end of memory by writing the value of each address into that location, printing the last address plus two on the teleprinter, and verifying each value written. The program then writes the complement of the address into each location from the end of memory back to 020000, and verifies each value written.

The next test comprises reading, writing and verifying memory using a Cal Data-supplied worst-case noise pattern (8 XOR 13). The test proceeds by exercising one block of memory at a time. If memory management is installed, the test is performed with memory management enabled.

One bit of a program indicator (location 01012) is set by the program for each 4K-word memory block between 4K and 28K that tested error free. After all locations from 020000 to the end of memory have been tested, the program relocates itself to the lowest 4K block that tested error free as noted in the program indicator. Locations 0 to 017776 are then tested as described above.

When testing is complete, the program relocates itself to its original position of 0 to 017776, increments the pass counter in location 010000 and restarts, beginning with the worst-case noise test. The teleprinter bell rings after 128 passes, after which the program restarts, beginning with the address test.

5.3.1.2 Loading, Starting and Running

To load and start the memory exerciser:

1. Load the program into memory using the ABS loader.
2. Load starting address 0200 into the program counter (0777707).
3. Set SWITCH REGISTER switches to the desired configuration (Table 5-1).
4. Press START.

The program loops and, on completion of 128 passes, rings the teleprinter bell. The pass number can be monitored by reading address location 01000

The program must be in the lowest 4K of memory when starting or restarting. It tests only contiguous areas of memory.

The program saves both loaders (BOOT and ABS) by relocating them. To restore them, restart at 0210 after ensuring that the program has not been relocated. The program has been relocated if location 0200 does not contain 0137 or if bit 15 of the macropanel data indicators is on.

In this case, the current 4K memory block number is indicated in program counter (PC) bits 15 to 13. Restart the program at 0X17400, where X is

Table 5-1. Test Program SWITCH REGISTER Switch Settings

Switch	When set (up)
15	The program halts on detection of an error. Correct data are not loaded into the faulty location. If the switch is raised after the error printout begins, the program halts when the message is completed, and the correct data are loaded into the faulty location.
14	Subtest loops.
13	Inhibits error printouts.
11	Inhibits subtest iterations.
10	Rings the teleprinter bell on detection of an error.
09	Displays the error count instead of the pass count in the display register (01000).

the octal value of PC bits 15 to 13. The program relocates itself to the lowest 4K of memory and halts at 0176. To resume testing, press CONT.

When the program is relocated, it verifies that the relocation has been made correctly. If the program cannot be relocated upward, the testing from the relocated area is bypassed. If there is an error while returning the program to the lowest 4K memory block, the program halts and types an error message. Continuing the program retries the downward relocation until successful or until the program is reloaded.

Stack-pointer file-register FR6 (location 0777706) starts at 0500 and resets to this value at the start of each subtest.

The program stores, in CPU file-register FR1 (location 0777701), the PC value of the last successful test. This can be used to aid in the isolation of a hardware failure.

The program makes 128 passes and then rings the teleprinter bell. The pass counter, location 01000, is displayed when switch 09 is down. but bit 15 is not part of the count. Bit 15 set indicates that the program has been relocated.

Each detected error increments the error counter, location 01002, which is displayed when switch 09 is up, but bit 15 is not part of the count. Bit 15 set indicates that the program has been relocated. The maximum error count is 017777, after which no further incrementation occurs.

If the program halts in trap/interrupt vector area 0 to 01000, examine stack-pointer FR6 to find the address of the instruction that caused the trap. File-register FR1 indicates the last successful test.

5.3.1.3 Error Printouts

The program prints the PC value where an error occurred, followed by the faulty location, the good data and the bad data, in the format:

PC xxxxxx ADDRESS aaaaaa GOOD DATA gggggg BAD DATA bbbbbb

The address is the actual 18-bit physical address, and is in FR2 (location 0777702). The good data are in FR0 (location 0777700) and the bad data are in FR3 (location 0777703).

When memory locations 0 to 017776 are tested, the PC printed is 020000 greater than that reflected in the program listing.

To recover from an error, press CONT or restart at location 0200, unless the program has been relocated. See paragraph 5.3.1.2.

APPENDIX A
INTERFACE PIN ASSIGNMENTS

Table A-1 gives interface pin assignments for A and B connectors that provide all active signal lines used by the CDP-8KX16. Table A-2 gives ground and power inputs and propagated Bus Grant line pins associated with the D and F connectors. Figure A-1 is a drawing of the connector layout.

Table A-1. CDP-8KX16 Interface Pin Assignments, Connectors A and B

Signal	Connector		Signal
INIT L	AA1	AA2	+5 V
* INTR L	AB1	AB2	GND
D00 L	AC1	AC2	GND
D02 L	AD1	AD2	D01 L
D04 L	AE1	AE2	D03 L
D06 L	AF1	AF2	D05 L
D08 L	AH1	AH2	D07 L
D10 L	AJ1	AJ2	D09 L
D12 L	AK1	AK2	D11 L
D14 L	AL1	AL2	D13 L
* PA 1	AM1	AM2	D15 L
GND	AN1	AN2	* PB 1
GND	AP1	AP2	* BBSY L
GND	AR1	AR2	* SACK L
GND	AS1	AS2	* NPR L
GND	AT1	AT2	* BR7 L
* NPG H	AU1	AU2	* BR6 L
* BG7 H	AV1	AV2	GND
* BG6 H	BA1	BA2	* +5 V
* BG5 H	BB1	BB2	GND
* BR5 L	BC1	BC2	GND
GND	BD1	BD2	* BR4 L
GND	BE1	BE2	* BG4 H
* ACLO L	BF1	BF2	DCLO 1
A01 L	BH1	BH2	A00 L
A03 L	BJ1	BJ2	A02 L
A05 L	BK1	BK2	A04 L
A07 L	BL1	BL2	A06 L
A09 L	BM1	BM2	A08 L
A11 L	BN1	BN2	A10 L
A13 L	BP1	BP2	A12 L
A15 L	BR1	BR2	A14 L
A17 L	BS1	BS2	A16 L
GND	BT1	BT2	C1 L
SSYN L	BU1	BU2	C0 L
MSYN L	BV1	BV2	GND

*Pins assigned in the MACROBUS, but not used by the CDP-8KX16.

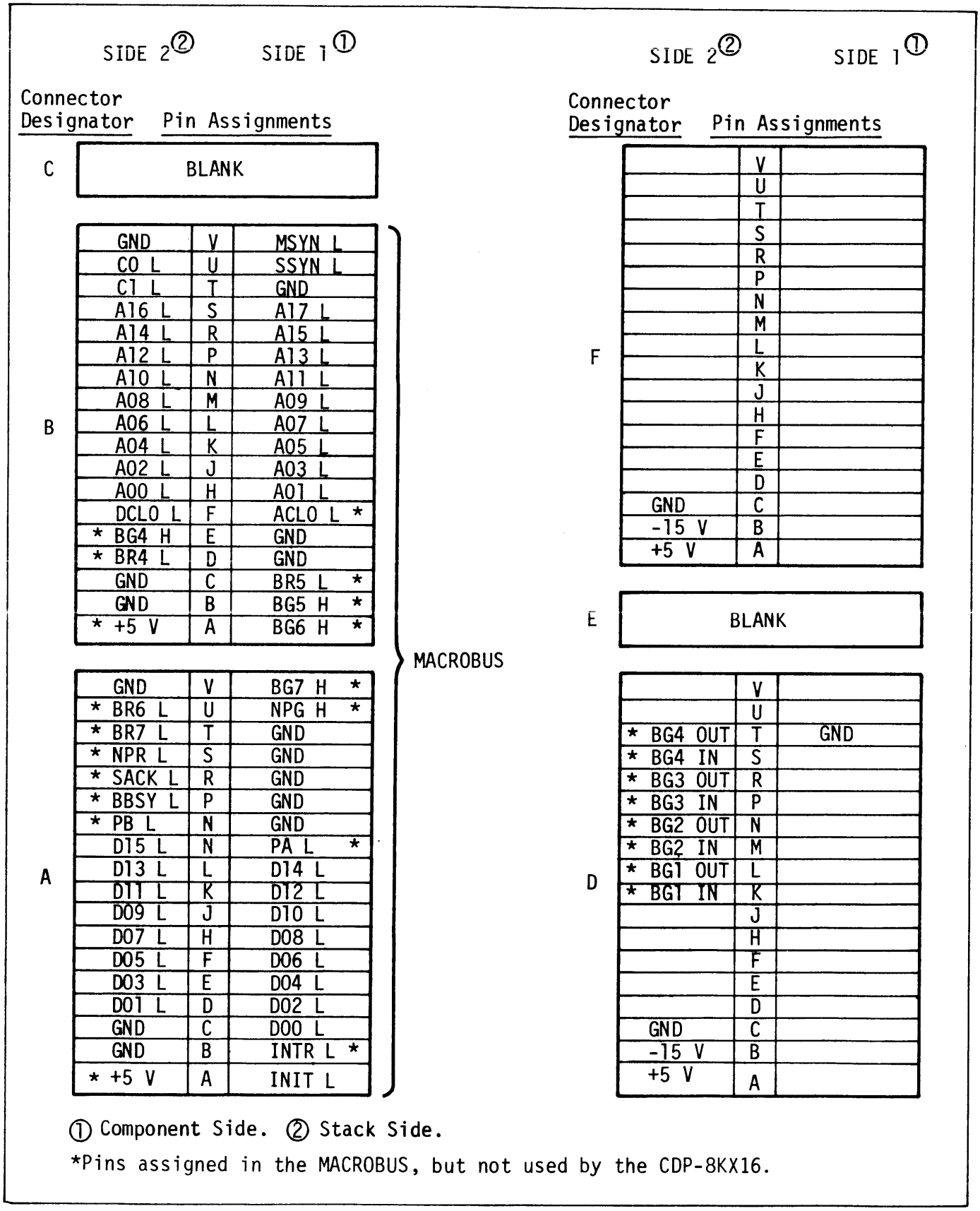
Table A-2. CDP-8KX16 Power and Bus-Grant Pin Assignments, Connectors D and F

Power	
Signal	Connector
+5 V	DA2
+5 V	FA2
-15 V	DB2
-15 V	FB2
GND	DC2
GND	FC2
GND	DT1
GND	FT1

Bus Grant	
Signal	Connector
* BG1 IN	DK2
* BG1 OUT	DL2
* BG2 IN	DM2
* BG2 OUT	DN2
* BG3 IN	DP2
* BG3 OUT	DR2
* BG4 IN	DS2
* BG4 OUT	DT2

*Pins assigned in the MACROBUS, but not used by the CDP-8KX16.

These signals are properly jumpered in the CDP-8KX16 to provide Bus Grant continuity.



① Component Side. ② Stack Side.

*Pins assigned in the MACROBUS, but not used by the CDP-8KX16.

Figure A-1. CDP-8KX16 Interface Connector Layout

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