

TABLE OF CONTENTS

SECTION 1	DESCRIPTION.....	1-1
1.1	General.....	1-1
1.2	Recording Media.....	1-2
1.3	Features.....	1-2
1.4	Performance Characteristics.....	1-3
1.4.1	Data Storage Capacity.....	1-3
1.4.2	Recording Parameters.....	1-3
1.4.3	Access Mechanism.....	1-3
1.4.4	Operating Environment.....	1-3
1.4.5	Shipping or Storage Environment.....	1-3
1.4.6	Reliability.....	1-4
1.5	Packaging Configuration.....	1-4
1.5.1	Disk Drive.....	1-4
1.5.2	Power Supply.....	1-4
1.6	Functional Description.....	1-5
1.6.1	Input/Output Board.....	1-5
1.6.2	Read/Write Amplifier Module (R/WA).....	1-5
1.6.3	Data Translator Board (DTB).....	1-5
1.6.4	Power Control Module (PCM).....	1-5
1.6.5	Control Sector Board (CSB).....	1-5
1.6.6	Servo Analog Board (SAB).....	1-5
1.6.7	Servo Logic Board (SLB).....	1-5
1.6.8	Drive Control Board (DCB).....	1-5
1.6.9	Temperature Compensation Board (TCB).....	1-5
1.6.10	Disk Cartridge.....	1-6
1.6.11	Read/Write Heads.....	1-6
1.6.12	Double-Frequency Encoding.....	1-6
1.6.13	Spindle Drive Assembly.....	1-6
1.6.14	Servo Positioner.....	1-6
1.6.15	Head/Arm Assembly.....	1-9
1.6.16	Head Loading.....	1-10
1.6.17	Air Filtration.....	1-10

TABLE OF CONTENTS (continued)

1.6.18	Baseplate Casting.....	1-10
1.6.19	Detent.....	1-10
1.6.20	Air Venting of Cartridge.....	1-11
1.6.21	Carriage Guide System.....	1-11
1.6.22	Velocity Transducer.....	1-11
1.7	Data Storage/Retrieval.....	1-11
1.7.1	General.....	1-11
1.7.2	Disk Select.....	1-11
1.7.3	Head Select.....	1-11
1.7.4	Write/Erase Amplifier (Figure 1-11).....	1-11
1.7.5	Read Amplifier.....	1-11
1.7.6	Discriminator (Optional).....	1-11
1.7.7	Index and Sector Detection.....	1-11
SECTION 2	INSTALLATION/INTERFACE.....	2-1
2.1	Unpacking the Drive for Installation.....	2-1
2.2	Special Grounding Instructions.....	2-1
2.3	Selection of Unit Identification.....	2-1
2.4	Input/Output Interface.....	2-5
2.5	Daisy-Chain Interconnection.....	2-6
2.6	Logic Levels.....	2-6
2.7	Input Lines.....	2-7
2.7.1	Cylinder Address.....	2-7
2.7.2	Disk Select.....	2-7
2.7.3	Head Select.....	2-7
2.7.4	Cylinder Seek.....	2-8
2.7.5	Controller Supplied +5 Volts (Optional)...	2-8
2.7.6	Address Clear.....	2-8
2.7.7	Write Enable.....	2-10
2.7.8	Read Enable.....	2-10
2.7.9	Write Data.....	2-10
2.7.10	Unit Select.....	2-10
2.8	Output Lines.....	2-10

TABLE OF CONTENTS (continued)

2.8.1	Drive Ready.....	2-10
2.8.2	Seek Complete.....	2-10
2.8.3	Ungated Attention.....	2-10
2.8.4	Read Data.....	2-10
2.8.5	Data Clock (Write Clock Optional).....	2-10
2.8.6	Index.....	2-10
2.8.7	Sector (Optional).....	2-10
2.8.8	Sector Address.....	2-10
2.8.9	Seek Incomplete.....	2-10
2.8.10	Write Inhibited.....	2-10
2.8.11	ILA/IDX FXD.....	2-11
2.8.12	ADD ACK/Sector FXD.....	2-11
2.9	Operator Controls and Indicators.....	2-11
2.9.1	Power Switch.....	2-11
2.9.2	Power Indicator.....	2-11
2.9.3	Start/Stop Switch.....	2-12
2.9.4	Ready Indicator.....	2-12
2.9.5	Stop Indicator.....	2-12
2.9.6	Write Inhibit Switches.....	2-12
2.10	Options.....	2-12
2.10.1	Fixed Sector Format.....	2-12
2.10.2	Data Encoding/Decoding.....	2-12
2.10.3	Data Decoding (Double Frequency).....	2-12
2.10.4	Sector Counter.....	2-12

SECTION 3

OPERATION.....	3-1
3.1 General.....	3-1
3.2 Acclimatization.....	3-1
3.3 Disk Cartridge Loading and Safety Interlocks.....	3-1
3.4 Cartridge Loading Sequence.....	3-4
3.5 Cartridge Removal Sequence.....	3-5
3.6 Disk Drive Operation.....	3-6
3.6.1 Starting the Drive.....	3-6

TABLE OF CONTENTS (continued)

3.6.2 Operation Online.....	3-6
3.6.3 Stopping the Drive.....	3-6
3.7 Operator Maintenance.....	3-6
3.8 Operator Troubleshooting Guide.....	3-6
SECTION 4 OPERATIONAL FLOW CHARTS.....	4-1
4.1 General.....	4-1
SECTION 5 CIRCUIT OPERATION.....	5-1
5.1 General.....	5-1
5.2 Logic Symbols.....	5-1
5.3 Circuitry.....	5-2
5.3.1 206 Interconnection Diagram.....	5-2
5.3.1.1 Transformer Interconnection.....	5-4
5.3.1.2 Spindle Motor.....	5-4
5.3.1.3 Power Control Module.....	5-4
5.3.1.4 Dynamic Brake.....	5-4
5.3.2 306 Interconnection Diagram.....	5-6
5.3.2.1 Transformer Interconnection.....	5-8
5.3.2.2 Spindle Motor.....	5-8
5.3.2.3 K1 and K2.....	5-8
5.3.2.4 Brush Motor.....	5-8
5.3.2.5 Power Control Module.....	5-8
5.3.2.6 Dynamic Brake.....	5-8
5.3.3 Mother Board.....	5-10
5.3.4 Functional Block Diagram.....	5-12
5.3.4.1 Carriage Position.....	5-12
5.3.4.2 New Address.....	5-12
5.3.4.3 Operational Status.....	5-12
5.3.4.4 Index/Sector Detection.....	5-12
5.3.4.5 Unit/Disk/Head Selection.....	5-12
5.3.4.6 Read or Write.....	5-12
5.3.4.7 Temperature Compensation.....	5-12

TABLE OF CONTENTS (continued)

5.4	Circuit Cards.....	5-14
5.4.1	Power Control Module (PCM).....	5-14
5.4.1.1	±15-Volt Regulator Circuit.....	5-14
5.4.1.2	+5-Volt Regulator Circuit.....	5-14
5.4.1.3	Servo Amplifier.....	5-14
5.4.1.4	Drive Status Circuitry.....	5-14
5.4.2	Input/Output Board (I/OB).....	5-18
5.4.2.1	Input/Output Board, Sheet 2 of 3.	5-18
5.4.2.2	Input/Output Board, Sheet 3 of 3.	5-20
5.4.2.3	Index and Sector Multiplexing....	5-20
5.4.3	Drive Control Board (DCB) Schematic.....	5-22
5.4.3.1	Index and Sector Circuitry.....	5-22
5.4.3.2	Up-Speed.....	5-24
5.4.3.3	Head Load Logic.....	5-24
5.4.3.4	Seek Complete/Incomplete Logic...	5-26
5.4.3.5	Forced Overcomp Check.....	5-26
5.4.4	Control Sector Board (CSB) Standard.....	5-28
5.4.4.1	Power On.....	5-28
5.4.4.2	Stop (+).....	5-28
5.4.4.3	Emergency Retract (-).....	5-28
5.4.4.4	Sector Address Counter.....	5-30
5.4.5	Control Sector Board (CSB) 48-Sector.....	5-32
5.4.5.1	Power On.....	5-32
5.4.5.2	Stop (+).....	5-32
5.4.5.3	Emergency Retract (-).....	5-32
5.4.5.4	Index and Sector Development.....	5-32
5.4.6	Servo Logic Board (SLB).....	5-34
5.4.6.1	Track Counting Circuit.....	5-34
5.4.6.2	Carriage Address Register.....	5-34
5.4.6.3	Adder IC's 20, 21 and 22.....	5-34
5.4.6.4	DAC 100.....	5-38
5.4.7	Servo Analog Board (SAB).....	5-40

TABLE OF CONTENTS (continued)

5.4.7.1	Coarse Servo Loop.....	5-40
5.4.7.2	Fine Servo Loop.....	5-40
5.4.8	Temperature Compensation Board (TCB).....	5-42
5.4.8.1	DC Thermal Compensation.....	5-44
5.4.8.2	Transient Thermal Compensation...	5-46
5.4.8.3	Settle Window and Zero Circuits..	5-48
5.4.8.4	100 TPI Differences.....	5-48
5.4.9	Read/Write Amplifier (R/WA).....	5-50
5.4.9.1	Head/Disk Select Circuit.....	5-50
5.4.9.2	Write Inhibit Circuit.....	5-50
5.4.9.3	Write Circuit.....	5-50
5.4.9.4	Read Circuit.....	5-52
5.4.10	Data Translator Board (DTB).....	5-54
5.4.10.1	Phase Locked Loop.....	5-54
5.4.10.2	Read Decode Circuitry.....	5-54
5.4.10.3	Write Encode Circuitry.....	5-56
5.4.11	Integrated Circuits.....	5-60
5.4.12	100 TPI Differences & Circuits.....	5-72
5.4.12.1	Read/Write Amplifier (R/WA) 2,400 rpm.....	5-73
5.4.12.2	Read/Write Amplifier (R/WA) 1,500 rpm.....	5-77
SECTION 6	TROUBLESHOOTING.....	6-1
SECTION 7	MAINTENANCE.....	7-1
7.1	General.....	7-1
7.2	Cautions.....	7-1
7.3	Tools and Materials.....	7-1
7.4	Preventive Maintenance.....	7-1
7.4.1	Periodic Checks (6-Month Intervals).....	7-1
7.4.2	Periodic Maintenance (12-Month Intervals).	7-2
7.4.3	Cleaning Kit.....	7-2
7.4.4	Fixed Disk Replacement Kit.....	7-2

TABLE OF CONTENTS (continued)

7.4.5	Drive Test Unit.....	7-2
7.5	Removal and Replacement Procedures.....	7-4
7.5.1	Top Cover.....	7-4
7.5.2	Rear Cover.....	7-4
7.5.3	Read/Write Amplifier Board (R/WA).....	7-4
7.5.4	Power Control Module (PCM).....	7-7
7.5.5	Input/Output Board.....	7-8
7.5.6	Drive Control Board (DCB).....	7-11
7.5.7	Control Sector Board (CSB).....	7-11
7.5.8	Data Translator Board (DTB).....	7-12
7.5.9	Servo Logic Board ("R" model only).....	7-12
7.5.10	Servo Analog Board ("R" model only).....	7-12
7.5.11	Servo Logic Board ("D" model using a DTU-2 only).....	7-14
7.5.12	Servo Analog Board ("D" model using a DTU-2 only).....	7-14
7.5.13	Servo Logic Board ("D" model using computer only).....	7-14
7.5.14	Servo Analog Board ("D" model using computer only).....	7-14
7.5.15	Temperature Compensation Board.....	7-15
7.5.16	Read/Write Heads (Refer to Fig. 7-16).....	7-17
7.5.17	Removable Disk Index/Sector Transducer....	7-20
7.5.18	Fixed Disk Index/Sector Transducer.....	7-21
7.5.19	Spindle Motor Belt (Refer to Fig. 7-25)...	7-22
7.5.20	Fixed Disk.....	7-23
7.5.21	Spindle Assembly.....	7-25
7.5.22	Velocity Transducer/Positioner Motor/Carriage.....	7-25
7.5.23	Air Filter.....	7-28
7.5.24	Spindle Motor Assembly.....	7-29
7.5.25	Mask Assembly.....	7-29
7.5.26	Detent Assembly.....	7-30

TABLE OF CONTENTS (continued)

7.5.27	Detent Alignment.....	7-31
7.5.28	Disk Cleaning Brushes - (306 models only).	7-33
7.6	Adjustments.....	7-34
7.6.1	Home Microswitch.....	7-34
7.6.2	Pack Interlock (306 models only) (See Fig. 7-38).....	7-35
7.6.3	Alignment of Receiver (206 models only)...	7-35
7.6.4	Head Load Cam Assembly.....	7-37
7.7	Bring-up Sequence of Adjustments.....	7-37
7.8	Packing Instructions.....	7-38
SECTION 8	DRAWINGS.....	8-1

LIST OF FIGURES

LIST OF FIGURES (continued)

<u>Figure</u>	<u>Title</u>	<u>Page</u>	<u>Figure</u>	<u>Title</u>	<u>Page</u>
1-1	Model 306, Front View.....	1-1	2-15	Seek Mode Timing Diagram, Sheet 1 of 5.....	2-14
1-2	Model 206, Front View.....	1-1	2-16	Seek Mode Timing Diagram, Sheet 2 of 5.....	2-15
1-3	Model 306, Front View, Covers Removed.....	1-2	2-17	Seek Mode Timing Diagram, Sheet 3 of 5.....	2-15
1-4	Model 206, Front View, Covers Removed.....	1-2	2-18	Seek Mode Timing Diagram, Sheet 4 of 5.....	2-16
1-5	Package Cross Section.....	1-4	2-19	Seek Mode Timing Diagram, Sheet 5 of 5.....	2-16
1-6	Model 306, Outline Dimensions.....	1-5	3-1	CMI Cartridge Loading Sequence.....	3-2
1-7	Model 206, Outline Dimensions.....	1-6	3-2	CMI Cartridge, Exploded View.....	3-2
1-8A	Data Track Configuration (200 TPI).....	1-7	3-3	Cartridge Loading Sequence.....	3-4
1-8B	Data Track Configuration (100 TPI).....	1-7	3-4	Cartridge Removal Sequence.....	3-5
1-9	Model 306 Series, Major Assemblies.....	1-8	4-1	Operational Flow Chart, Power Up/Install Cartridge.....	4-1
1-10	Model 206 Series, Major Assemblies.....	1-8	4-2	Operational Flow Chart, Run/First Seek.....	4-2
1-11	Model 206, Bottom View.....	1-9	4-3	Operational Flow Chart, Programmed Seek.....	4-3
1-12	Model 306, Top View.....	1-9	4-4	Operational Flow Chart, Write Mode.....	4-4
1-13	Model 306, Bottom View.....	1-10	4-5	Operational Flow Chart, Read Mode.....	4-5
1-14	Edge Erase Concept (200 TPI).....	1-12	4-6	Operational Flow Chart, Stop.....	4-6
1-15	Edge Erase Concept (100 TPI).....	1-13	5-1	Logic Symbols.....	5-1
1-16	Recording Waveforms.....	1-13	5-2	206 Interconnection Diagram, Sheet 1 of 2.....	5-3
2-1	Shipping Container.....	2-1	5-3	206 Interconnection Diagram, Sheet 2 of 2.....	5-5
2-2	Installation Dimensions (306).....	2-2	5-4	306 Interconnection Diagram, Sheet 1 of 2.....	5-7
2-3	Installation Dimensions (206).....	2-3	5-5	306 Interconnection Diagram, Sheet 2 of 2.....	5-9
2-4	Termination Board and I/O Cable.....	2-3	5-6	Mother Board Schematic.....	5-11
2-5	Carriage Holddown Screw.....	2-5	5-7	Block Diagram.....	5-13
2-6	Model 206, Rear View.....	2-5	5-8	Power Control Module Schematic.....	5-15
2-7	Line Drivers and Receivers.....	2-6	5-8	(Repeat) Power Control Module Schematic.....	5-17
2-8	Daisy-Chain Cabling Diagram.....	2-6	5-9	Input/Output Board Schematic, Sheet 2 of 3.....	5-19
2-9	Input/Output Interface.....	2-7	5-10	Input/Output Board Schematic, Sheet 3 of 3.....	5-21
2-10	Disk Select Timing.....	2-7	5-11	Drive Control Board Schematic.....	5-23
2-11	Head Select Timing.....	2-8	5-11	(Repeat) Drive Control Board Schematic.....	5-25
2-12	Cylinder Address Timing.....	2-8	5-11	(Repeat) Drive Control Board Schematic.....	5-27
2-13	Address Clear Timing.....	2-8	5-12	Index/Sector Timing.....	5-22
2-14	Read Data Timing at Interface.....	2-11			

LIST OF FIGURES (continued)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
5-13	Head Loading Sequence.....	5-24
5-14	Seek Complete Timing Diagram.....	5-26
5-15	Control Sector Board Schematic.....	5-29
5-15	Repeat) Control Sector Board Schematic.....	5-31
5-16	Sector Counter Outputs.....	5-30
5-17	Control Sector Board 48-Sector Schematic.....	5-33
5-18	Servo Logic Board Schematic.....	5-35
5-18	(Repeat) Servo Logic Board Schematic.....	5-37
5-18	(Repeat) Servo Logic Board Schematic.....	5-39
5-19	Servo Analog Schematic.....	5-41
5-20	Track Displacement Versus Track Number.....	5-42
5-21	Temperature Compensation Board Schematic.....	5-43
5-21	(Repeat) Temperature Compensation Board Schematic.....	5-45
5-21	(Repeat) Temperature Compensation Board Schematic.....	5-47
5-21	(Repeat) Temperature Compensation Board Schematic.....	5-49
5-22	Read/Write Amplifier Board Schematic.....	5-51
5-22	(Repeat) Read/Write Amplifier Board Schematic.....	5-53
5-23	DTB Timing.....	5-54
5-24	Data Translator Board Schematic.....	5-55
5-24	(Repeat) Data Translator Board Schematic.....	5-57
5-24	(Repeat) Data Translator Board Schematic.....	5-59
5-25	Write Data Timing Diagram.....	5-58
5-26	Series 74 Transistor-Transistor Logic.....	5-61
5-27	Up/Down 4-Bit Binary Counter, 74193.....	5-62
5-28	Dual D-Type Edge-Triggered Flip Flop, 7474.....	5-63
5-29	Dual JK Master-Slave Flip Flop, 74107.....	5-63
5-30	MSI 5-Bit Comparator, 9324.....	5-64
5-31	MSI Quad Two-Input Multiplexer, 9322.....	5-64
5-32	DC Dual Level Retriggerable Resettable Monostable Multivibrator, 9602.....	5-65
5-33	Bidirectional One Shot, 8T20.....	5-65

LIST OF FIGURES (continued)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
5-34	Voltage Comparator, LM311.....	5-66
5-35	Dual Voltage Tracking Regulator, 2501.....	5-66
5-36	Dual Operational Amplifier, 5558.....	5-66
5-37	Operational Amplifier, LM308.....	5-66
5-38	Voltage Regulator, MC 7815C.....	5-67
5-39	Voltage Regulator, MC 7915C.....	5-67
5-40	Hex Unified Bus Receiver, DM8837.....	5-67
5-41	Quad 2-Input Nor Gate, DM8836N.....	5-67
5-42	D/A Converter - 10 Bit Miniature, DAC100.....	5-68
5-43	4-Bit Binary Full Adders, SN7483.....	5-68
5-44	Dual J-K Positive-Edge-Triggered Flip Flop, SN74109.....	5-69
5-45	Hex Inverter, SN74H04.....	5-69
5-46	Dual D-Type Positive-Edge-Triggered Flip Flop with Preset and Clear, SN74H74.....	5-69
5-47	Hex/Quadruple D-Type Flip Flop with Clear, SN74174.....	5-70
5-48	Dual Peripheral Positive-Nand Driver, 75452.....	5-70
5-49	Timer, 555.....	5-71
5-50	Read/Write Amplifier (R/WA) 2,400 rpm.....	5-74
5-50	(Repeat) Read/Write Amplifier (R/WA) 2,400 rpm.....	5-76
5-51	Read/Write Amplifier (R/WA) 1,500 rpm.....	5-78
5-51	(Repeat) Read/Write Amplifier (R/WA) 1,500 rpm.....	5-80
5-51	(Repeat) Read/Write Amplifier (R/WA) 1,500 rpm.....	5-82
5-52	Operational Flow Chart, Write Mode.....	5-77
5-53	Timing Diagram, Typical Write Mode.....	5-79
5-54	Operational Flow Chart, Read Mode.....	5-81
5-55	Timing Diagram, Typical Read Mode.....	5-81
6-1	306 Troubleshooting Flow Chart, Sheet 1 of 8.....	6-2
6-2	306 Troubleshooting Flow Chart, Sheet 2 of 8.....	6-3
6-3	306 Troubleshooting Flow Chart, Sheet 3 of 8.....	6-4
6-4	306 Troubleshooting Flow Chart, Sheet 4 of 8.....	6-5
6-5	306 Troubleshooting Flow Chart, Sheet 5 of 8.....	6-6

LIST OF FIGURES (continued)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
6-6	306 Troubleshooting Flow Chart, Sheet 6 of 8.....	6-7
6-7	306 Troubleshooting Flow Chart, Sheet 7 of 8.....	6-8
6-8	306 Troubleshooting Flow Chart, Sheet 8 of 8.....	6-9
7-1	Model 306D/306R Series Major Assemblies.....	7-2
7-2	Model 206D/206R Series Major Assemblies.....	7-3
7-3	Drive Test Unit (DTU).....	7-4
7-4	Read/Write Shield.....	7-5
7-5	Write Current Waveform.....	7-5
7-6	Read/Write Board Test Points.....	7-6
7-7	Read/Write Board Test Points.....	7-6
7-8	Read/Write Board Test Points.....	7-6
7-9	Power Control Module Test Points and Adjustments.....	7-7
7-10	Sector Counter.....	7-10
7-11	Card Cage.....	7-10
7-12	TP4, Data Translator Board.....	7-12
7-13	Seek Time Adjustment.....	7-13
7-14	Temperature Compensation Board Assembly 302800.....	7-16
7-15	Temperature Versus Voltage Offset.....	7-17
7-16	Read/Write Heads.....	7-17
7-17	Dibit Information Waveform.....	7-19
7-18	Dibit Pattern and Fringes.....	7-19
7-19	Correctly Aligned Dibit Pattern.....	7-19
7-20	Dibit Pattern Fringes with Runout Centered on Scope.....	7-19
7-21	Index Alignment.....	7-20
7-22	Removable Disk Index/Sector Transducer.....	7-20
7-23	Fixed Disk Index/Sector Transducer.....	7-22
7-24	Index/Sector Transducer Output Waveform.....	7-22
7-25	Model 306, Bottom View.....	7-23
7-26	Fixed Disk Clamp Ring Screw Pattern.....	7-24
7-27	Velocity Transducer Removal.....	7-26

LIST OF FIGURES (continued)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
7-28	Carriage Guide Shaft Positioning.....	7-27
7-29	Race Assembly Installation.....	7-27
7-30	Voice Coil to Carriage Alignment.....	7-28
7-31	Optical Detent System (Viewed from Top).....	7-30
7-32	Detail of Detent Optics.....	7-31
7-33	Plug P6 Pin Assembly.....	7-31
7-34	Zero Adjustment.....	7-32
7-35	Zero Adjustment ("D" model using computer).....	7-33
7-36	Disk Brush Condition.....	7-34
7-37	Home Microswitch Adjustment.....	7-34
7-38	Pack Interlock Adjustment.....	7-35
7-39	Receiver in Lowest Position.....	7-36
7-40	Receiver	7-36
7-41	Head Load Cam Assembly Adjustment.....	7-37
8-1	206 Disk Drive Assembly, Sheet 1 of 5.....	8-2
8-2	206 Disk Drive Assembly, Sheet 2 of 5.....	8-3
8-3	206 Disk Drive Assembly, Sheet 3 of 5.....	8-4
8-4	206 Disk Drive Assembly, Sheet 4 of 5.....	8-5
8-5	206 Disk Drive Assembly, Sheet 5 of 5.....	8-6
8-6	306 Disk Drive Assembly, Sheet 1 of 5.....	8-7
8-7	306 Disk Drive Assembly, Sheet 2 of 5.....	8-8
8-8	306 Disk Drive Assembly, Sheet 3 of 5.....	8-9
8-9	306 Disk Drive Assembly, Sheet 4 of 5.....	8-10
8-10	306 Disk Drive Assembly, Sheet 5 of 5.....	8-11
8-11	206 Front Face Assembly.....	8-12
8-12	206 Shield Assembly.....	8-13
8-13	Switch Plate Assembly.....	8-14
8-14	Carriage Assembly.....	8-15
8-15	206 Spindle Assembly.....	8-16
8-16	306 Front Face Assembly.....	8-17

LIST OF FIGURES (continued)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
8-17	306 Shield Assembly.....	8-18
8-18	306 Shroud Assembly.....	8-19
8-19	306 Brush Motor Assembly.....	8-20
8-20	306 Spindle Assembly.....	8-21
8-21	Slide Kit.....	8-22
8-22	Mother Board Assembly.....	8-23
8-23	Power Control Module Assembly.....	8-24
8-24	Servo Logic Board Assembly.....	8-25
8-25	Servo Analog Board Assembly.....	8-26
8-26	Temperature Compensation Board.....	8-27
8-27	Paddle Board Assembly.....	8-28
8-28	Input/Output Board Assembly.....	8-29
8-29	200 TPI Read/Write Amplifier Assembly, Sheet 1 of 2.....	8-30
8-30	200 TPI Read/Write Amplifier Assembly, Sheet 2 of 2.....	8-31
8-31	Control Sector Board Assembly.....	8-32
8-32	Control Sector Board (48) Assembly.....	8-33
8-33	Data Translator Board.....	8-34
8-34	Drive Control Board Assembly.....	8-35
8-35	Termination Board Schematic.....	8-36
8-36	Termination Board Assembly.....	8-37
8-37	100 TPI, 1,500 rpm Read/Write Amplifier Assembly, Sheet 1 of 2.....	8-38
8-38	100 TPI, 1,500 rpm Read/Write Amplifier Assembly, Sheet 2 of 2.....	8-39
8-39	100 TPI, 2,400 rpm Read/Write Amplifier Assembly, Sheet 1 of 2.....	8-40
8-40	100 TPI, 2,400 rpm Read/Write Amplifier Assembly, Sheet 2 of 2.....	8-41

LIST OF TABLES

Table	Title	Page
2-1	Input/Output Board Options.....	2-9
2-2	Input Pin Assignments.....	2-12
2-3	Output Pin Assignments.....	2-12
2-4	Drive Control Board Options.....	2-13
2-5	Data Translator Board Options.....	2-13
2-6	Control Sector Board Options.....	2-13
2-7	Read/Write Board Options.....	2-13
2-8	Read/Write Board Options (100 TPI 1,500 rpm).....	2-13
2-9	Read/Write Board Options (100 TPI 2,400 rpm).....	2-13
5-1	Output Current Versus Input Codes (IC 13).....	5-36
5-2	Output Current Versus Input Codes (IC 12).....	5-36
5-3	Thermistor Values.....	5-44
5-4	Head/Disk Selection.....	5-50
5-5	D/A Converter, CS-1020.....	5-60
7-1	Standard Tools.....	7-1
7-2	Special Tools and Equipment, Electrical.....	7-1
7-3	Special Tools and Materials, Mechanical.....	7-2
7-4	Ungated Attention.....	7-9
7-5	Write Inhibit Options.....	7-9
7-6	Sector Counter Outputs.....	7-10
7-7	DCB One Shots.....	7-11

SECTION 1
DESCRIPTION

1.1 GENERAL

The Model 206 & 306 Series Disk Cartridge Drives have been designed to interface with and provide peripheral storage capabilities for small, general-purpose digital computers. The 306 series uses the EMM-Caelus CMIII or equivalent top-loading disk cartridge to provide mass random access storage. The 206 series uses the Caelus CMI or equivalent front loading disk cartridges.

The drives are available in eight different configurations.

DRIVE TYPE	100 TPI		200 TPI	
	3MB	6MB	6MB	12MB
Front Load	206D/1	206D/2	206R/1	206R/2
Top Load	306D/1	306D/2	306R/1	306R/2

The basic design philosophy uses the latest technological advances and innovations to achieve the primary objective of a highly reliable, low-cost memory expander for third generation minicomputers. Simplification of proven techniques, utilization of conservative design practices, and incorporation of advanced techniques have resulted in a reduction of over 60 percent of the component parts normally associated with a direct access device of this type while maintaining data integrity.



Figure 1-1. Model 306, Front View

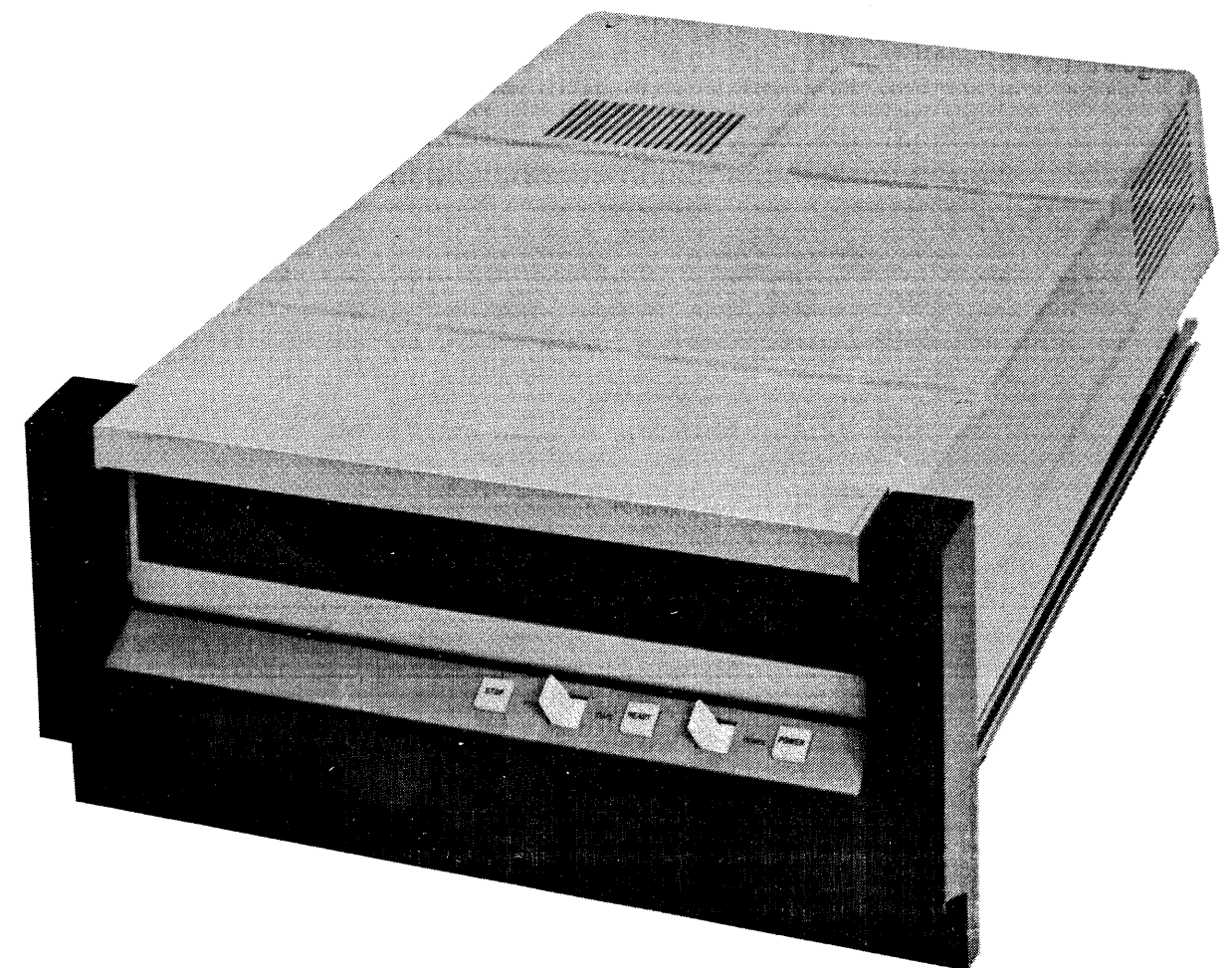


Figure 1-2. Model 206, Front View

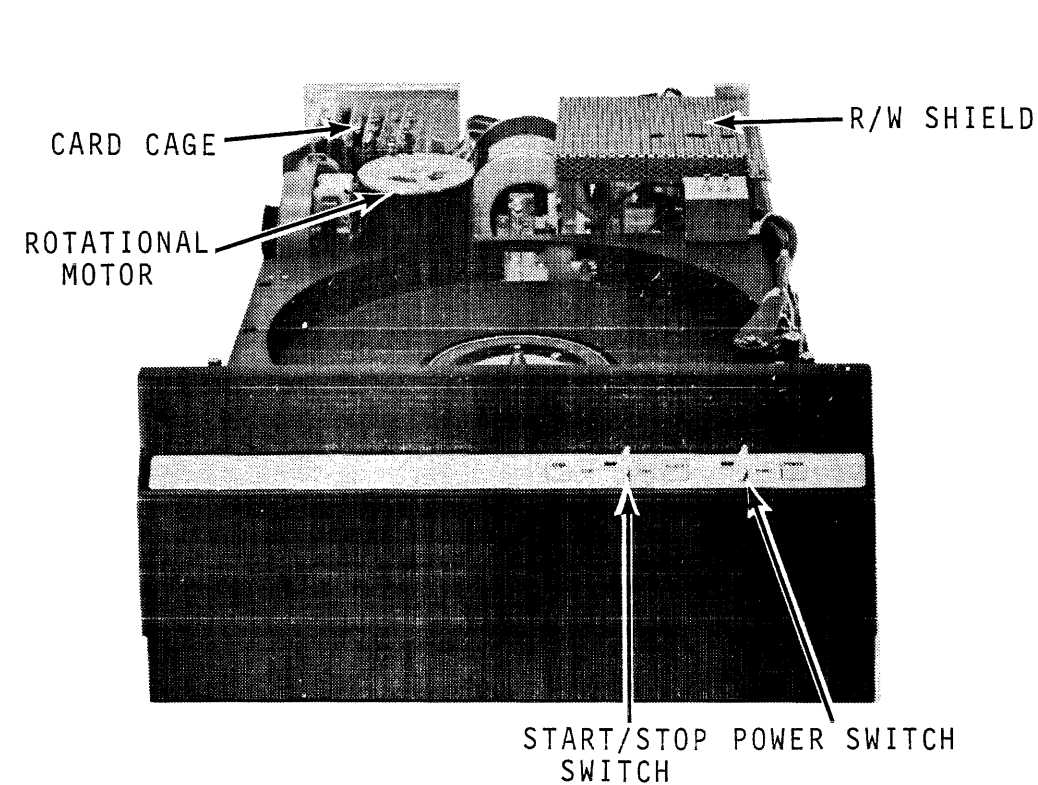


Figure 1-3. Model 306, Front View, Covers Removed

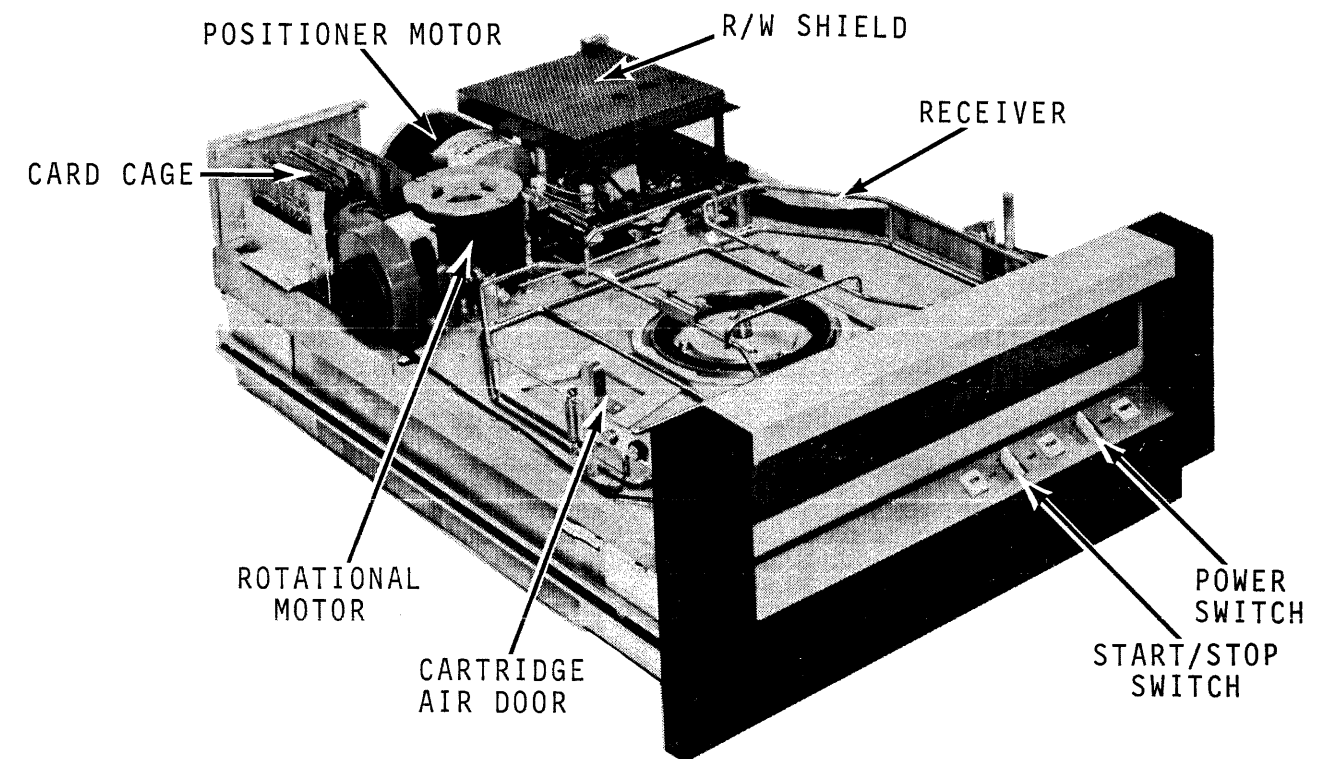


Figure 1-4. Model 206, Front View, Covers Removed

1.2 RECORDING MEDIA

The recording media are the removable EMM-Caelus CMIII-2X top-loading disk cartridge and the EMM-Caelus CMI-2X front loading disk cartridge.

The optional fixed disk is a double sided oxide coated disk housed permanently in the drive.

1.3 FEATURES

Rotational motion and relative position of the fixed and removable disk are monitored by means of a magnetic index/sector transducer.

Horizontal positioning of the read/write heads is accomplished by a servo driven voice coil actuator which receives positional information in digital format from an optical position transducer. Final positioning is accomplished by error comparison data from the same transducer, which is summed with the appropriate temperature compensation.

Data recording is accomplished through read/write heads which use the latest edge erase technique, eliminating cross-talk between tracks. Read data are passed through electronic circuits designed to discriminate data properly while compensating for bit shift. Temperature is constantly monitored to compensate dynamically for contractions and expansions of both the media and the mechanics. Disks written on 100-TPI drives can be read on 200-TPI drives by use of an optional jumper.

1.4 PERFORMANCE CHARACTERISTICS

The performance characteristics of the drive series offers users capacities and access times which extend the capabilities and applications of general purpose minicomputers.

1.4.1	<u>Data Storage Capacity</u>	<u>100 TPI</u>	<u>200 TPI</u>
	Removable Disk:	3MB	6MB
	Fixed Disk:	3MB	6MB
	Track:	7500 Bytes	7500 Bytes
	Number of Tracks Per Surface:	204	408
	Number of Sectors:	Index plus 00, 08, 12, 14, 16, 24, or 32	
1.4.2	<u>Recording Parameters</u>		
	Bit Density:	2,200 BPI inside track (maximum)	
	Track Density:	200 TPI (306R/206R) 100 TPI (306D/206D)	
	Medium:	Interchangeable cartridge, double-sided oxide coated disk in polycarbonate dustproof housing and fixed double-sided disk	
	Recording Band:	2.04 inches (5.18 cm)	
	Disk Diameter:	14 inches (35.56 cm)	
	Cartridge Diameter:	15 inches (38.1 cm)	
	Coding:	Double frequency	
	Transfer Rate:	1588.5 kHz at 1,500 rpm; 2.5 MHz at 2,400 rpm	
	Heads:	The magnetic transducer is an air-bearing head with the magnetic elements supported in a ceramic shoe	
	Bit Cell Time:	630 ns; 400 ns at 2,400 rpm	
	Sector Transducer Variation:	± 10 μs maximum, ± 7 μs at 2,400 rpm	
	Sector Rotational Speed Variation:	± 40 μs maximum, ± 25 μs at 2,400 rpm	
	Write to Read Switching Time:	30 μs maximum	
	Read to Write Switching Time:	7 μs maximum	

Erase After Write Delay:	20 μs maximum, 13 μs at 2,400 rpm
Write Clock Frequency Tolerance:	± 0.1%
Disk Rotational Speed:	1,500 rpm ± 1%, 2,400 rpm optional
Disk Rotation Time:	40 ms nominal, 25 ms at 2,400 rpm
Head Switching Time:	5 μs maximum
Data Discriminator Sync Time:	20 μs maximum, 15 μs at 2,400 rpm

1.4.3 Access Mechanism

Access Motion Time (including head settling)	
Track to Track:	12 milliseconds maximum
Average Random:	40 milliseconds
Maximum Access:	70 milliseconds maximum
Average Latency Time:	20 ms at 1,500 rpm, 12.5 ms at 2,400 rpm
	= $\frac{\text{Revolution Time}}{2}$

1.4.4 Operating Environment

Temperature:	+50° to +104°F, ambient; Maximum rate of change 20°F/hour
Humidity:	10% to 85% relative humidity, non-condensing
Cooling:	Forced room air, ambient at installed location
Vibration:	.25 g peak, 10 to 100 Hz, all axes
Air Filtration:	Absolute, 0.3 micron
Elevation:	Zero to 6,000 feet Optional 6,000 to 10,000 feet
Shock:	.3 to 75 g less than 5 seconds, all axes
AC Voltage Deviation:	± 10%
Line Frequency Deviation:	± 2%

1.4.5 Shipping or Storage Environment

Temperature:	-40° to +150°F
Humidity:	10% to 95% relative humidity, non-condensing

1.4.6 Reliability

Under normal operational conditions, preventive maintenance is recommended every six months. Mean time between failure, under normal operating conditions and with routine preventive maintenance, is specified at 4,500 hours. Mean time to repair is 30 minutes.

Soft Error Rate: 1 in 10^{10}
 Hard Error Rate: 1 in 10^{12}

1.5 PACKAGING CONFIGURATION

The Disk Cartridge Drives have been engineered to be clean and simple with a minimum of moving parts. A precision casting ensures rigidity of the drive and provides a base for all key mechanical components. A package cross-sectional view is shown in Figure 1-5.

Slide No. 3335 or equivalent. Physical dimensions (see Figure 1-6) are as follows: (See Figures 1-6 and 1-7.)

Overall Length: 30.06 inches (including front face, excluding termination board and I/O connector)
 Rack Depth: 28.0 inches minimum
 Rack Height: 8.75 inches minimum
 Rack Width: 17.75 inches (including slides)
 Overall Width: 19.00 inches (including front face)
 Weight: 84 pounds (less slides);
 91 pounds (with slides)

1.5.2 Power Supply

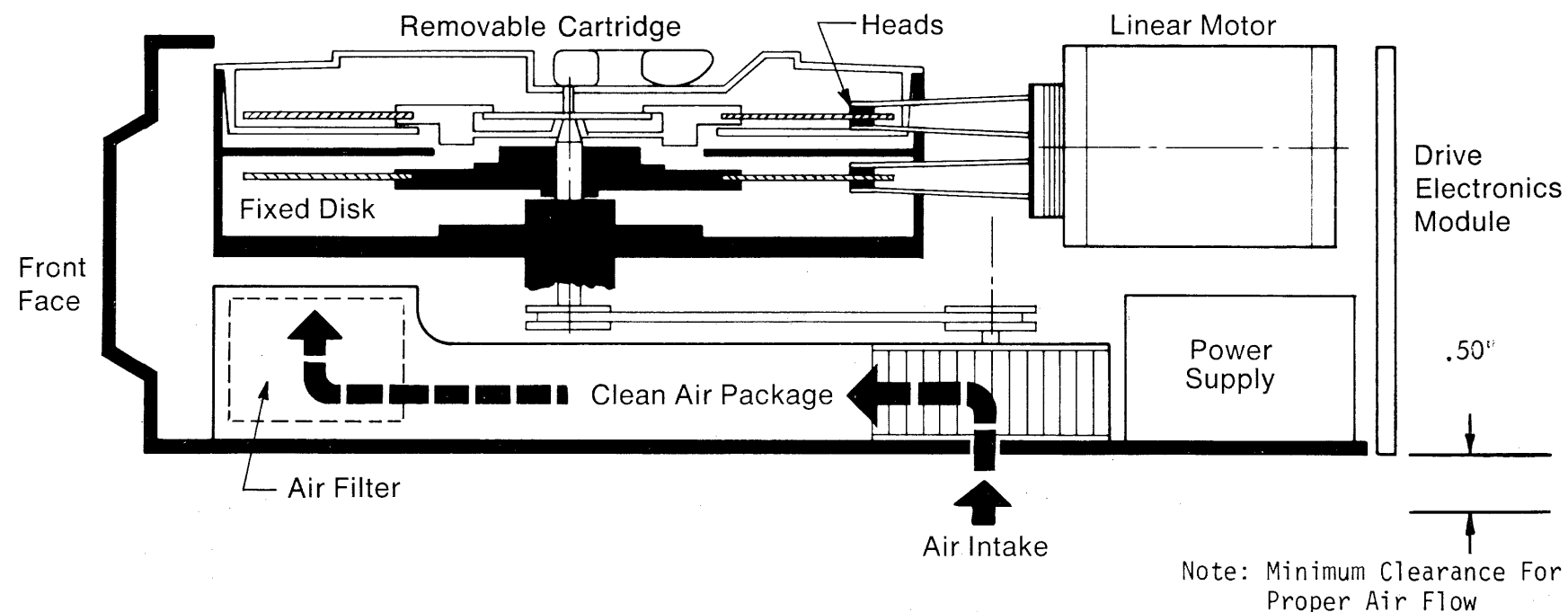
The built-in power supply provides power to the drive functions. Line voltage is either 50 or 60 Hz, 100 to 240 volts ± 10 percent. (A transformer is provided to accommodate international requirements through taps.)

Three classes of power output are provided:

- a. DC Regulated
 - +5 volts at 3 amps maximum
 - +15 volts at 1 amp maximum
 - 15 volts at 1 amp maximum
- b. DC Unregulated
 - ± 24 volts at 3 amps average, 12 amps peak for servo operation and operation of indicators and relays.
- c. AC Power for Spindle Motor
 - 60 Hz, 120 volt, 2 amps, single phase
 - 50 Hz, 120 volt, 3 amps, single phase

The regulated supplies are designed so that the total combined effects of ± 10 percent line voltage variations and load variations between the full and half loads cause the output voltages to vary no more than ± 2 percent of the nominal values.

Fuses are installed in the primary circuit and on the PCM for protection. All regulated voltages are current limited and short circuit proof.

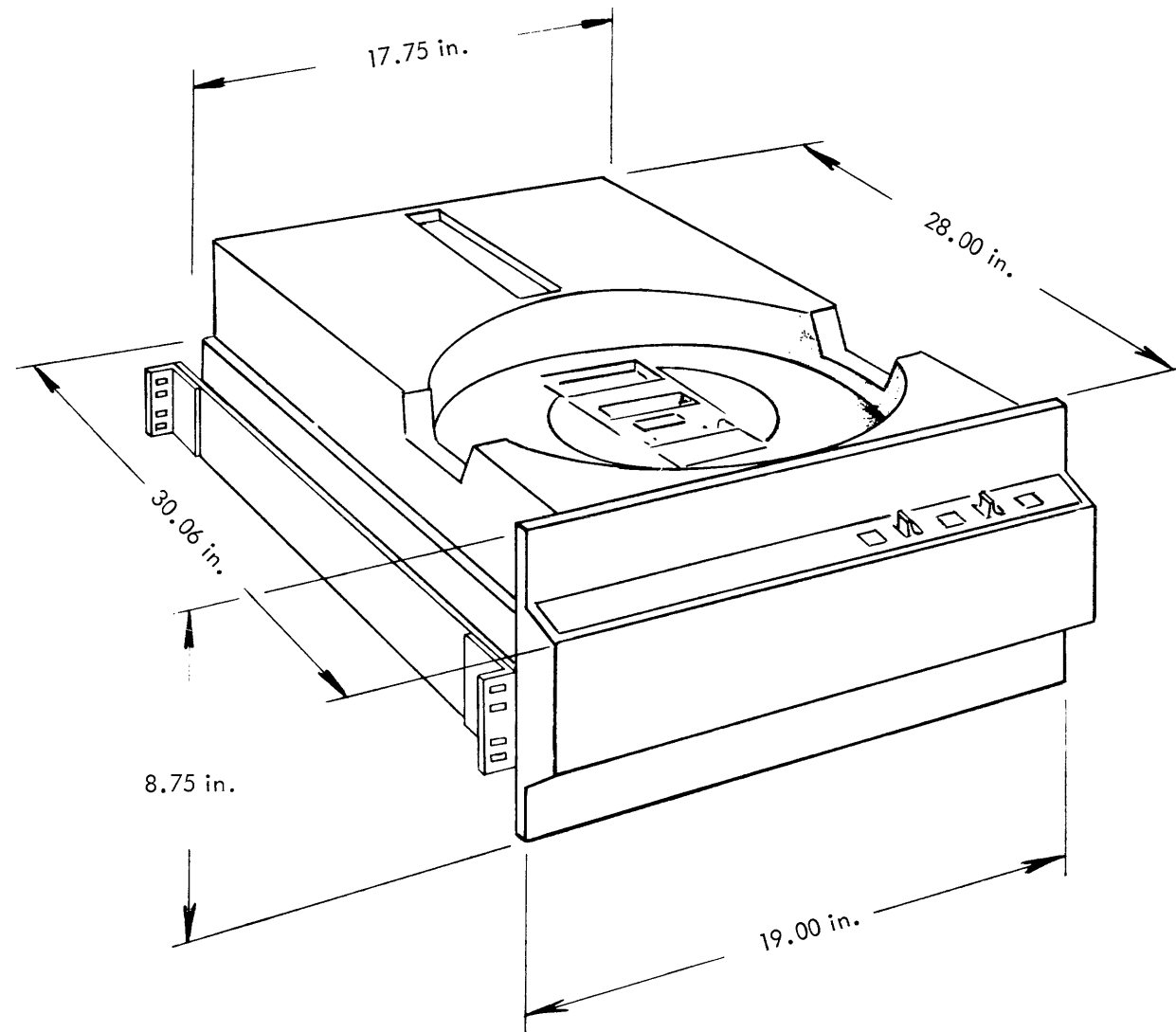


600-5

Figure 1-5. Package Cross Section

1.5.1 Disk Drive

The disk drive is rack mountable in a standard dimension RETMA relay rack. Front access is accomplished by use of Grant Chassis



600-6

Figure 1-6. Model 306, Outline Dimensions

1.6 FUNCTIONAL DESCRIPTION

1.6.1 Input/Output Board

The I/O board provides an interface to the user's controller and contains line drivers and receivers, index/sector pulse multiplexing, and unit select logic.

1.6.2 Read/Write Amplifier Module (R/WA)

The Read/Write Amplifier provides the circuitry necessary for the recording and recovery of data and consists of read, write, head and disk select, and write inhibit circuit functions.

1.6.3 Data Translator Board (DTB)

The DTB provides timing and data functions, including data discrimination and data encoding which are optional to the Model 306 series.

1.6.4 Power Control Module (PCM)

The Power Control Module contains voltage regulation circuits, servo power amplification, and the emergency head retract circuit.

1.6.5 Control Sector Board (CSB)

The Control Sector board provides sector counting and control logic.

1.6.6 Servo Analog Board (SAB)

The Servo Analog board contains the logic necessary to control speed and direction of the access mechanism for both servo loops, the optical detent, and the velocity counter loop.

1.6.7 Servo Logic Board (SLB)

The Servo Logic board provides the logic that maintains carriage track position, and provides the arithmetic necessary to provide a direction and velocity reference signal to the SAB.

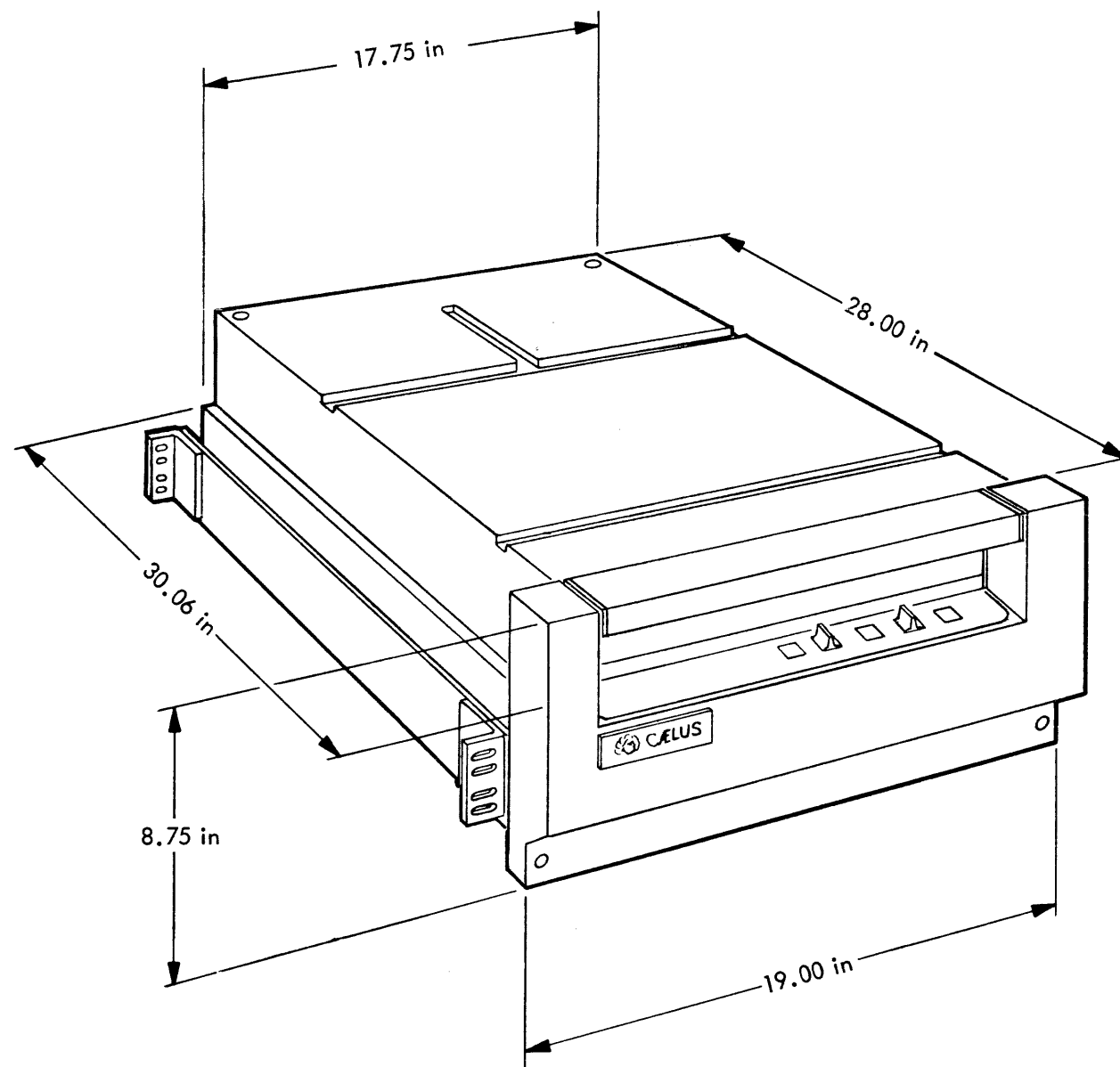
1.6.8 Drive Control Board (DCB)

The Drive Control board provides the logic necessary to perform the initialization sequence and to detect index and sector pulses.

1.6.9 Temperature Compensation Board (TCB) (Tampered out for 100 TPI)

The Temperature Compensation board contains the circuitry necessary to develop offsetting voltages proportional to temperature such that the position of the read/write heads can be offset to allow for contractions and expansions of both the media and the mechanics.

The Temperature Compensation board also provides a delay to the head load sequence. The time of the delay is dependent upon the temperature of the removable media in relation to the temperature of the mechanics. This delay is from none required to a maximum of 6 minutes and only occurs on 200 TPI versions.



200-6

Figure 1-7. Model 206 Series, Outline Dimensions

1.6.10 Disk Cartridge

The removable cartridge used by the disk Drives is composed of a single, 14-inch-diameter disk which is permanently enclosed in a polycarbonate housing. The disk is a rigid, aluminum substrate coated with an iron oxide formulation designed specifically for compatibility with the read/write heads.

Data are recorded serial-by-bit on concentric tracks of the oxide coated disk by two non-contact, flying heads which magnetize discrete areas of the disk. These heads float on a film of air, (approximately 60 microinches thick) generated by the spinning disk. The data recording surface of the disk is 2.030 inches wide, measured on the radius. (See Figure 1-8). The outer radius measures 6.500 inches, and the inner radius 4.470 inches.

Data are double-frequency encoded, permitting recording of self-clocked data at high densities.

1.6.11 Read/Write Heads

The read/write heads are mounted in a ceramic shoe and "fly" over the surface of the disk. Edge erase coils follow the read/write coils on the head surface and are energized when data are being written.

1.6.12 Double-Frequency Encoding

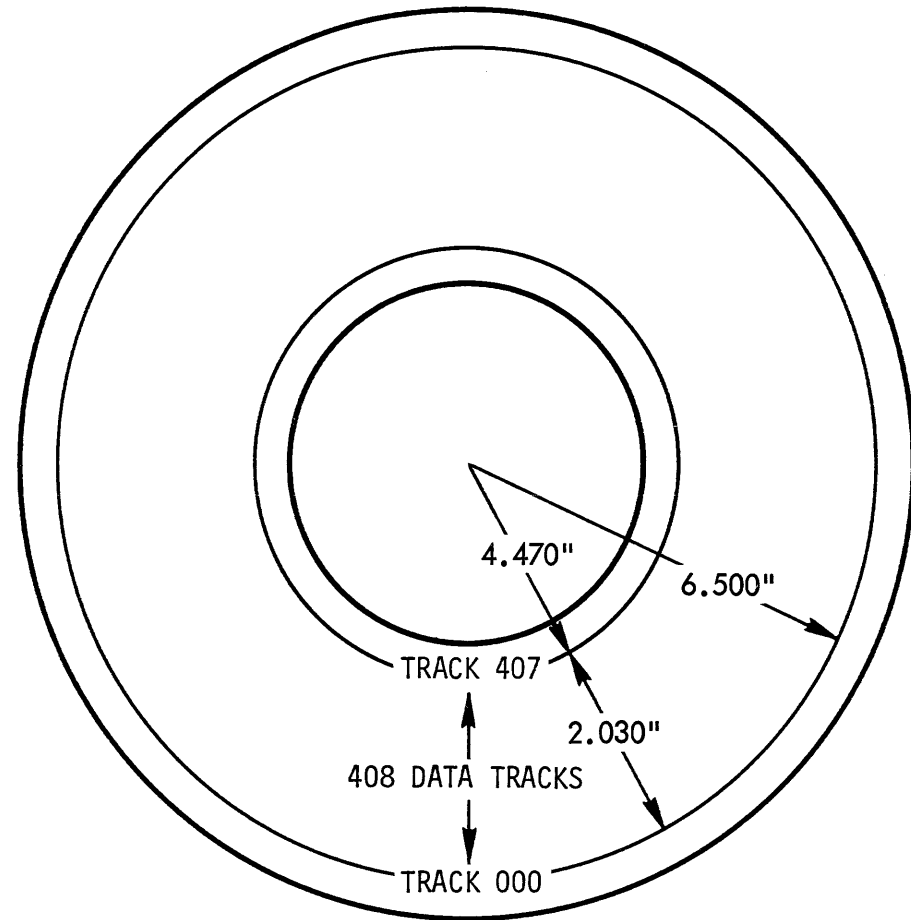
Write data are received in optional NRZ format from the Controller and are encoded internally to double-frequency format prior to writing. A flux change occurs at every bit cell boundary when a logical "0" is recorded. An extra flux change occurs at the center of the bit cell when a logical "1" is recorded.

1.6.13 Spindle Drive Assembly

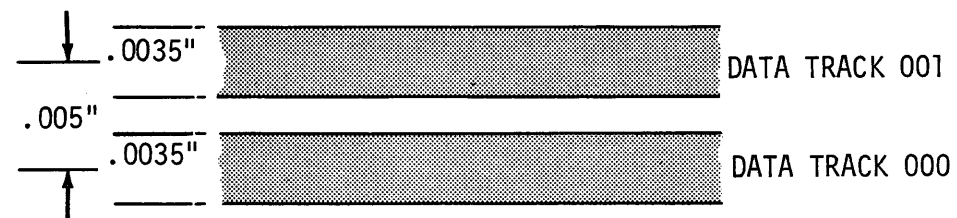
The spindle drive assembly accurately positions and holds the disk in place as the disk is rotated. The spindle is driven by a belt attached to the spindle drive motor pulley and the spindle pulley. The disk is held in position by the disk adapter and the spindle chuck. The spindle chuck consists of a magnetic ring and pole piece. When the disk cartridge is mounted on the spindle chuck, a magnetic path is completed to retain the disk securely on the spindle. The induction-type motor attains operating speed within a few seconds after turn-on.

1.6.14 Servo Positioner

The servo positioner motor has a stationary permanent magnet with a movable, wound-bobbin coil. The coil is driven in and out of the permanent magnet by the servo power amplifier. The carriage assembly is attached to the coil.

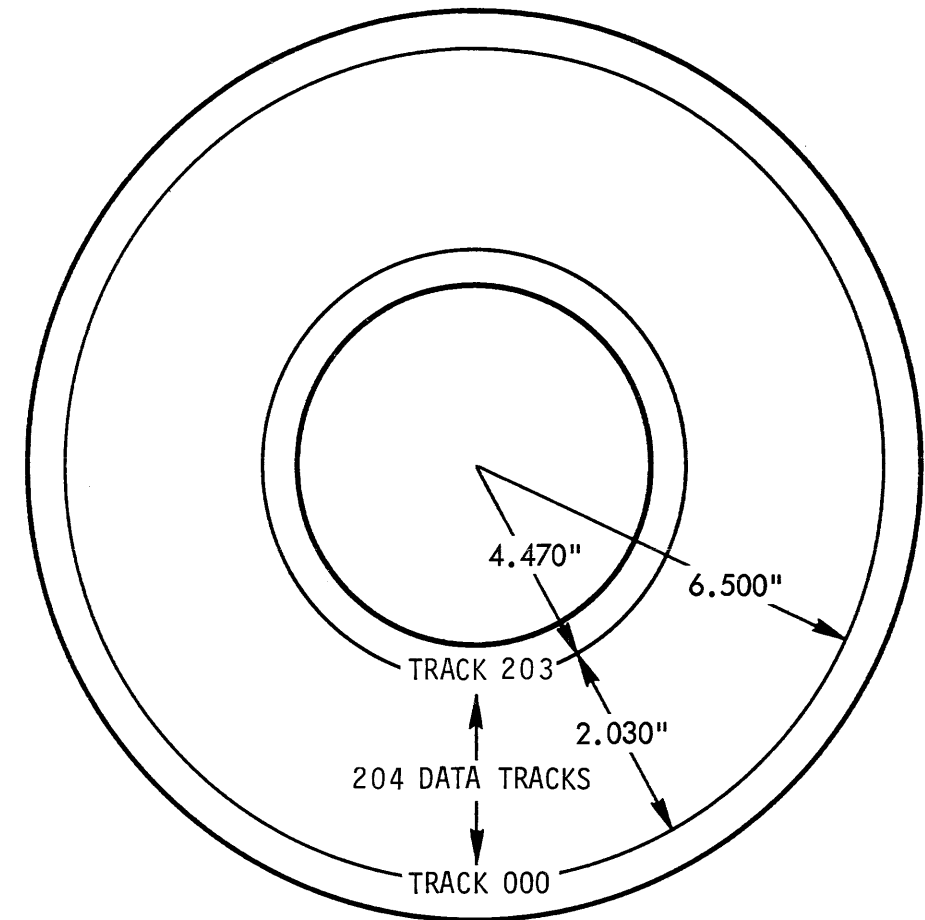


NOMINAL TRACK DIMENSIONS

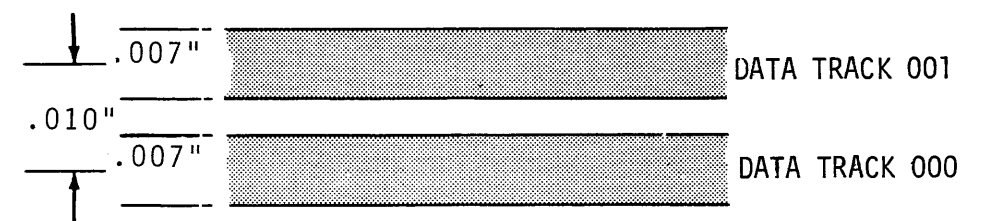


600-8

Figure 1-8A. Data Track Configuration (200 TPI)



NOMINAL TRACK DIMENSIONS



200-8

Figure 1-8B. Data Track Configuration (100 TPI)

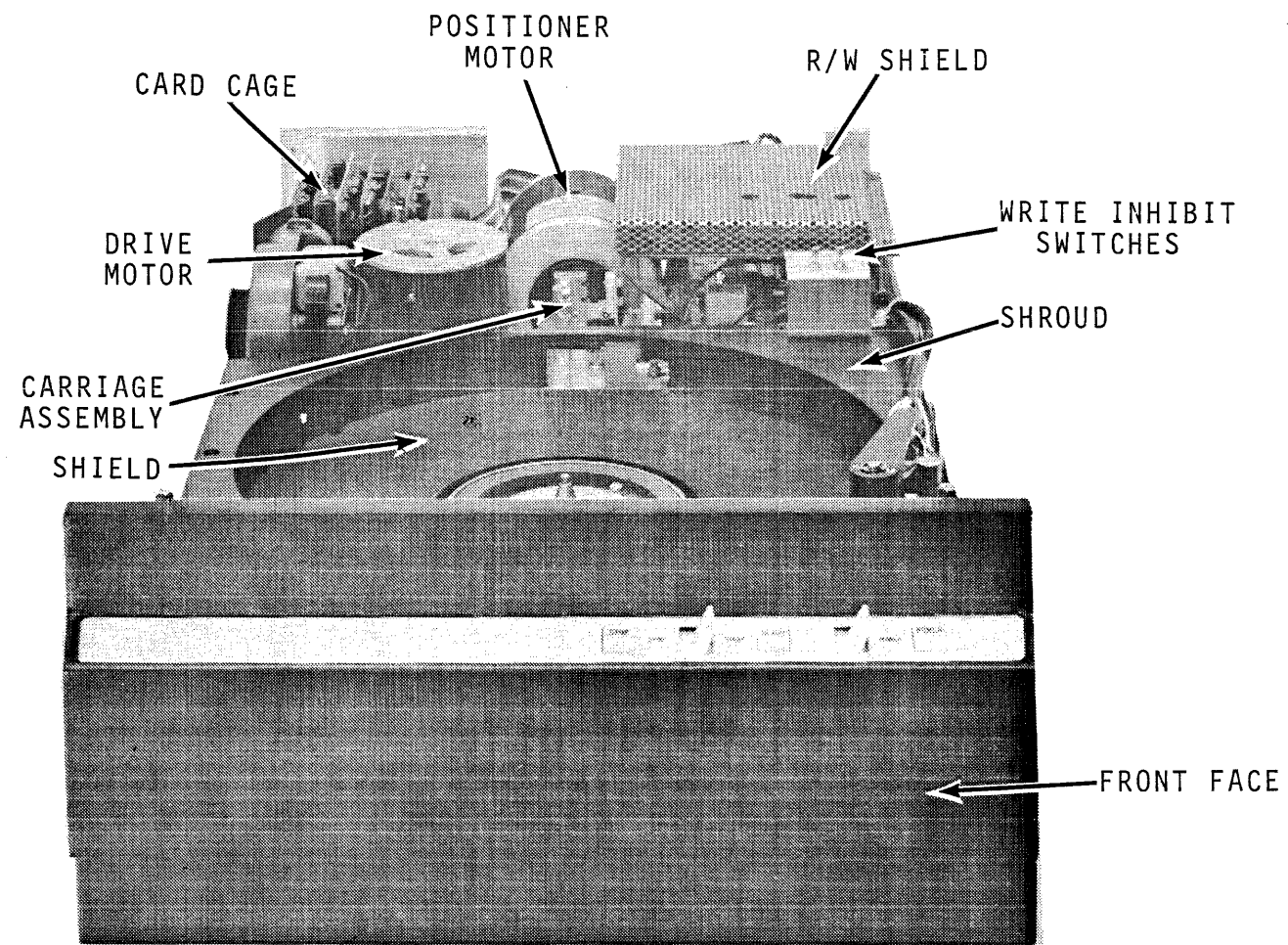


Figure 1-9. Model 306 Series, Major Assemblies

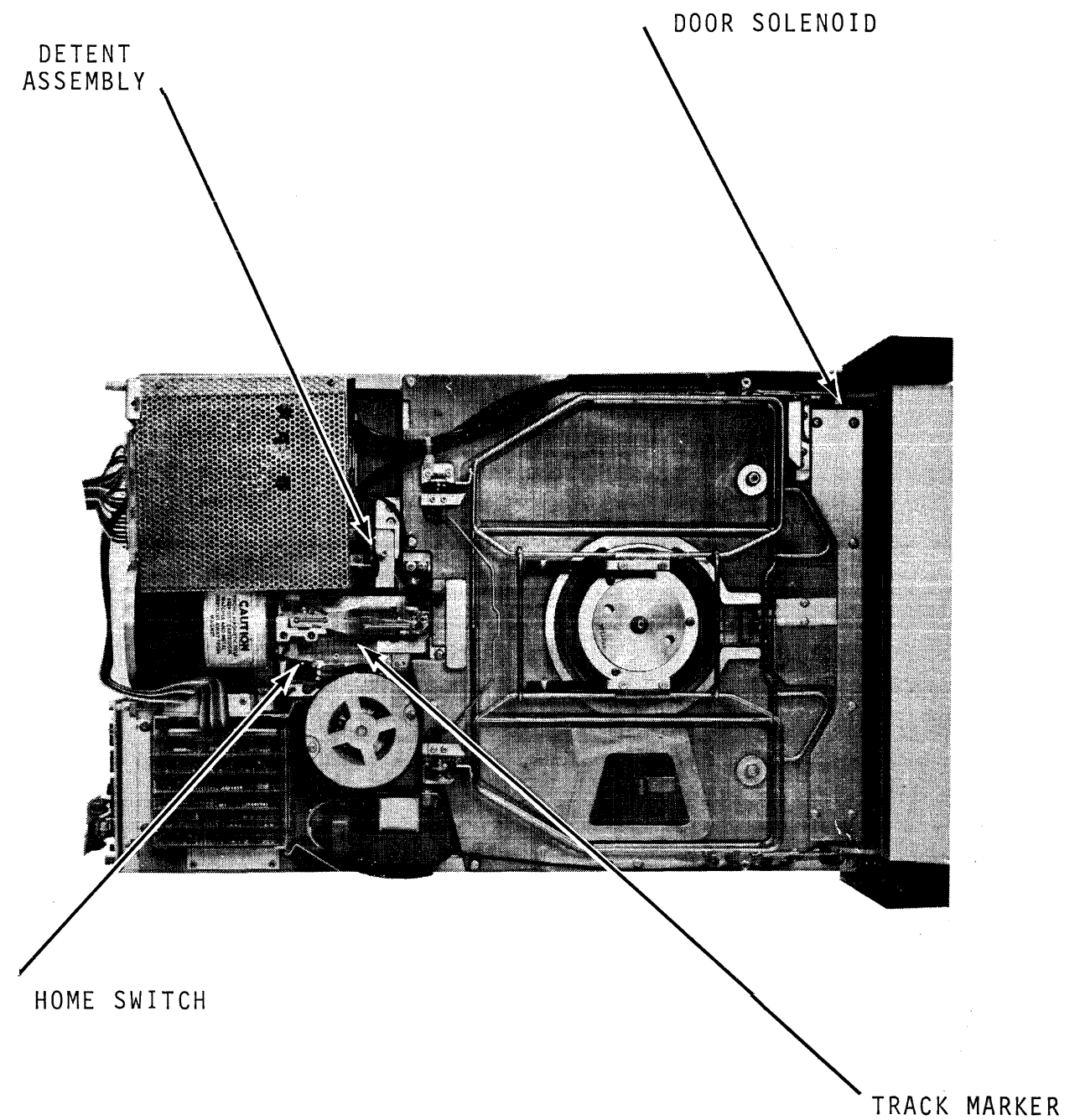


Figure 1-10. Model 206 Series, Major Assemblies.

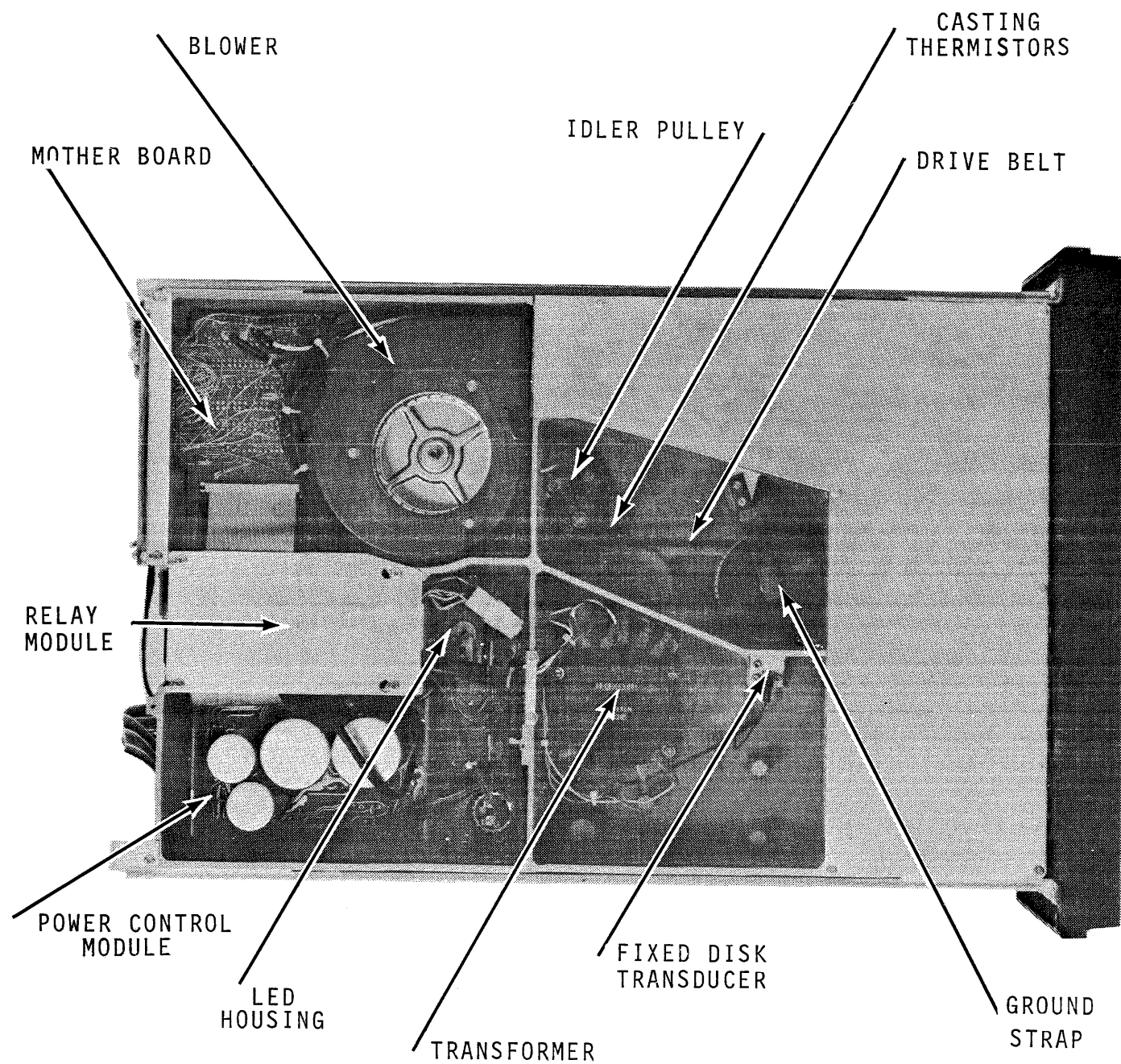
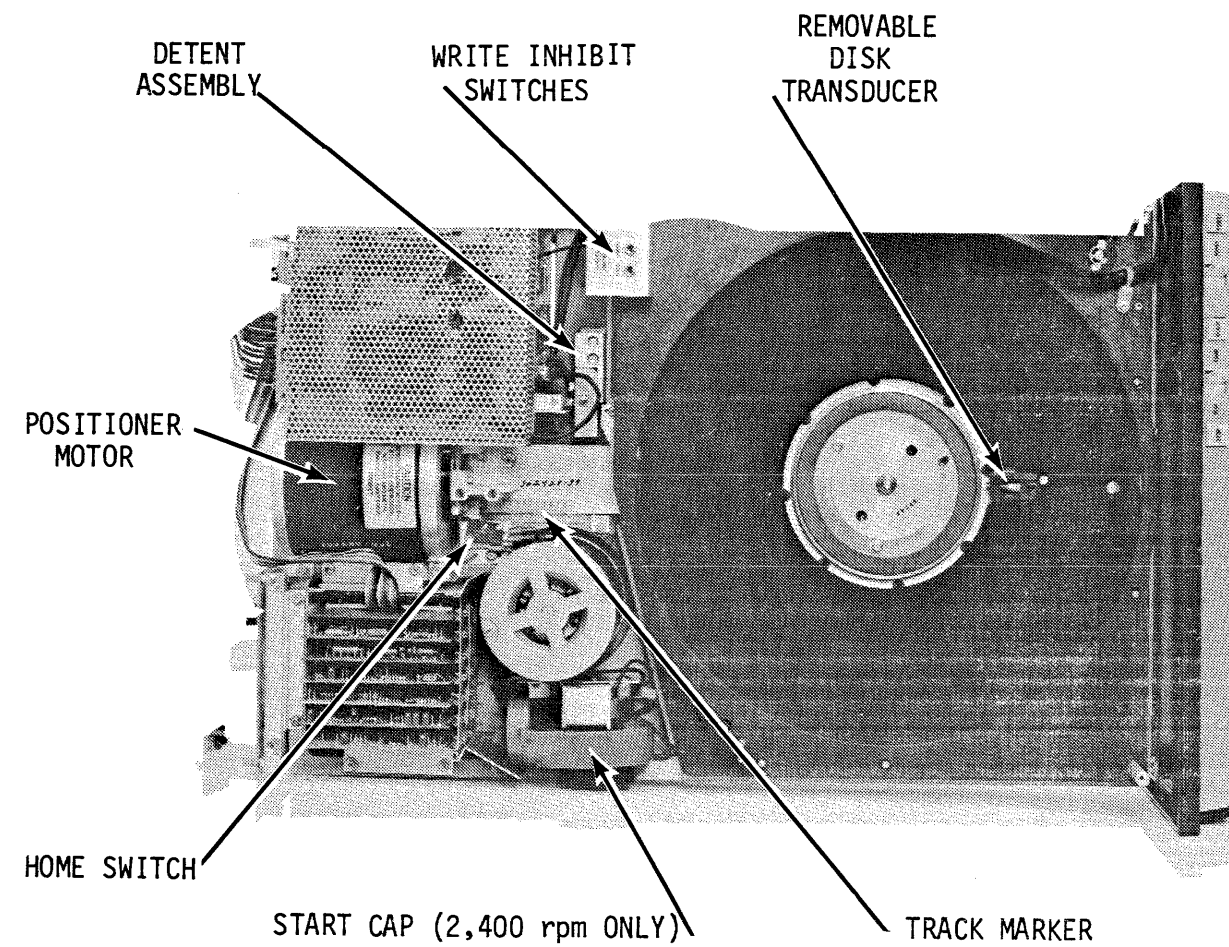


Figure 1-11. Model 206, Bottom View



600-9

Figure 1-12. Model 306, Top View

1.6.15 Head/Arm Assembly

The head/arm assembly is mounted onto the carriage. The flying head pad is attached to the access arm by a gimbal. Leaf springs are an integral part of the head assembly. These springs provide constant loading force on the flying heads so that the proper flying height is maintained.

Gimbal mounting of the head core assembly provides two degrees of movement (pitch and roll) in the horizontal axis. A *Delrin loading button transmits the loading force onto the shoe. As the disk

**Delrin is a DuPont trademark for acetal resin.*

rotates, the gimbal action allows the head shoe to attain the proper aerodynamic attitude when flying over the disk surface.

Two air bleed holes symmetrically spaced about the head core axis stabilize the head and permit it to fly at the proper height.

1.6.16 Head Loading

Head loading is achieved through the preformed, precision leaf springs. At the home position of the carriage, the leaf springs are maintained in the unloaded position by a self-lubricating Delrin ramp.

Forward motion of the carriage allows the leaf spring to be activated by sliding off the ramp. The ramp geometry controls the unloaded head-to-head spacing; ramp position controls the area on the disk at which the heads load and unload

1.6.17 Air Filtration

The disk drive is provided with an air filtration system which purges the disk cartridge and the fixed disk of all particles greater than 0.3 micron. The entire clean air system is contained within the drive.

1.6.18 Baseplate Casting

The baseplate is a rib-reinforced aluminum casting. The functional surfaces are machined to critical tolerances. The servo positioner motor, carriage rails, position transducer, spindle, spindle drive motor, cartridge receiver, electronics modules, interlocks, and air supply systems are mounted on the baseplate.

1.6.19 Detent

The absolute positioning accuracy of the read/write heads is determined by an electro/LED servo system consisting of a detent assembly and a carriage-mounted mask assembly.

The assembly contains the necessary solar cells and reticle, so that when properly positioned and adjusted over the carriage-mounted mask assembly, will produce two sine waves 90 degrees out of phase when the carriage is in movement. The LED source for the solar cells is mounted to the baseplate and is not connected to the detent assembly.

The positioning accuracy of the carriage-mounted read/write heads is governed by the critically spaced grid lines etched on the reticle and mask, therefore special alignment fixtures are not required. Only one of the two signals is used for positioning, the other is a direction-of-travel indicator.

An additional phototransistor circuit is provided to locate the read/write heads at cylinder 000 upon system start-up, address clear command, or in the event of an illegal address seek command.

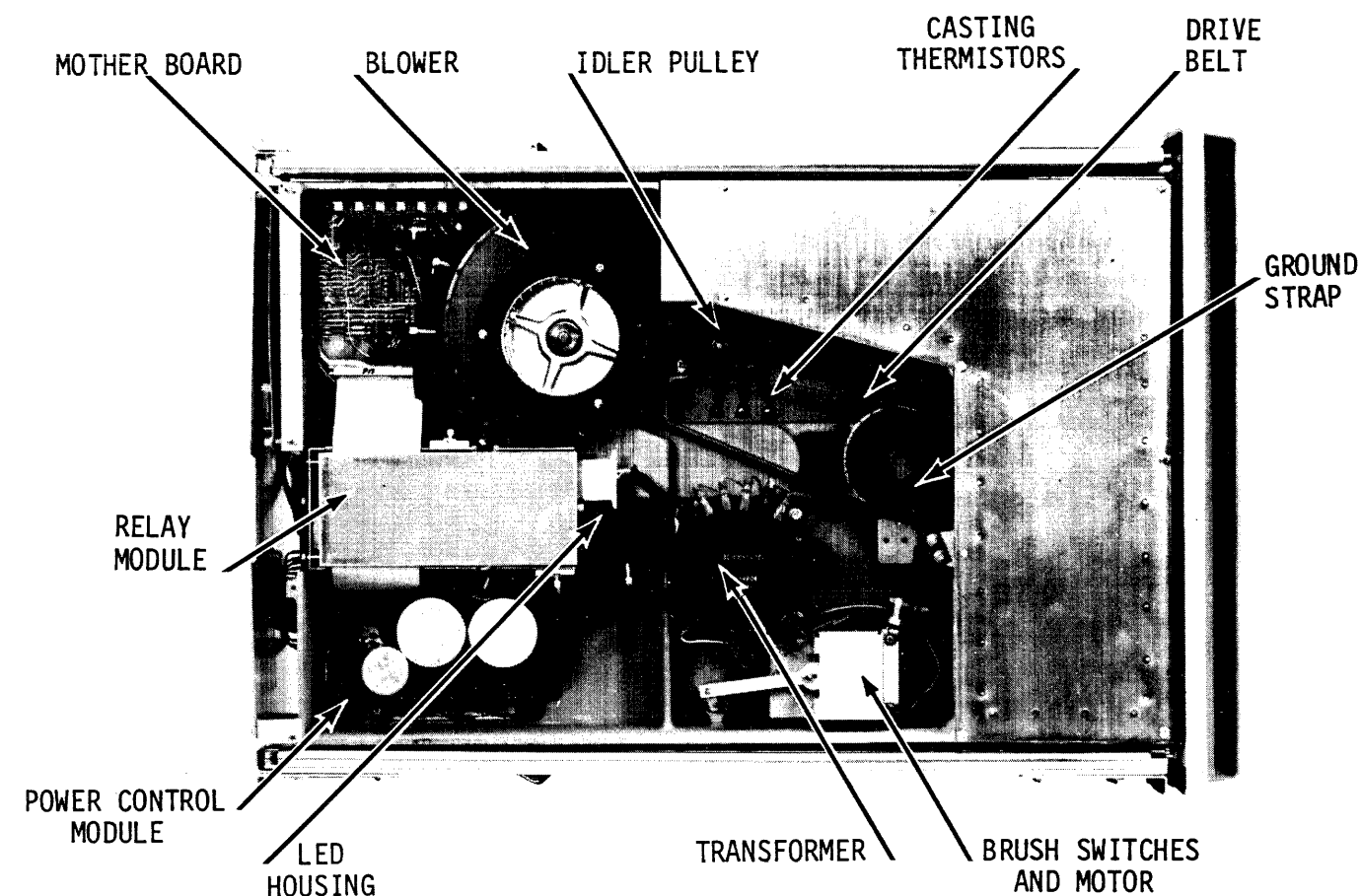


Figure 1-13. Model 306, Bottom View

600-10

1.6.20 Air Venting of Cartridge

Absolute filtered air is delivered to the disk area from a squirrel cage blower through an absolute air filter at a rate of 25 CFM. The air is filtered to 0.3 micron; the filter surface area is greater than 500 square inches. The air is exhausted out the head entry areas of the two disks with enough pressure to prohibit foreign matter from entering these openings. The purge time prior to flying the heads is approximately 40 seconds. During the 40-second period of time, brushes which sweep the disk surface clear of any contaminants are used.

NOTE

The 200 Series drive does not use brushes and purging is done in 10 seconds.

1.6.21 Carriage Guide System

The carriage is a lightweight aluminum extrusion which is guided on a precision, ball slide type race. The guide for the race is machined into the baseplate, thus eliminating additional mechanical parts and critical alignments.

The race is under the carriage and is continually being purged with clean air from the fixed disk area so that dust or other foreign matter cannot settle and possibly cause positioning inaccuracies.

1.6.22 Velocity Transducer

The Linear Velocity Transducer (LVT) is an electro-mechanical transducer mounted inside the servo positioner motor which produces a voltage output directly proportional to the velocity of a movable magnetic core which is connected to the carriage assembly. As the carriage moves, the lines of flux from the magnetic core cut the windings in the velocity transducer producing an output whose polarity is governed by the direction of movement. This output is fed to the servo system for velocity control purposes.

1.7 DATA STORAGE/RETRIEVAL

1.7.1 General

Upon transmittal of the Seek Complete and Ready signals, the drive is ready to receive read or write commands. All circuitry associated with Data Storage/Retrieval are described in this section.

1.7.2 Disk Select

The Disk Select circuitry switches either the removable or fixed disk electronics as controlled by the Disk Select Line.

1.7.3 Head Select

The Head Select circuitry switches either the upper or lower head to the read/write electronics as controlled by the state of the Head Select Line.

1.7.4 Write/Erase Amplifier (Figures 1-14 and 1-15).

The Write/Erase Amplifier is unconditionally turned on, provided that safety conditions are satisfied, the Write Inhibit switches are not on, and a Write Enable level is received from the Controller. The amplifier provides the write current for each write data pulse received. Write data are received in double-frequency format. Compensation for the spatial displacement between the erase-read gaps is provided in the erase circuitry.

1.7.5 Read Amplifier

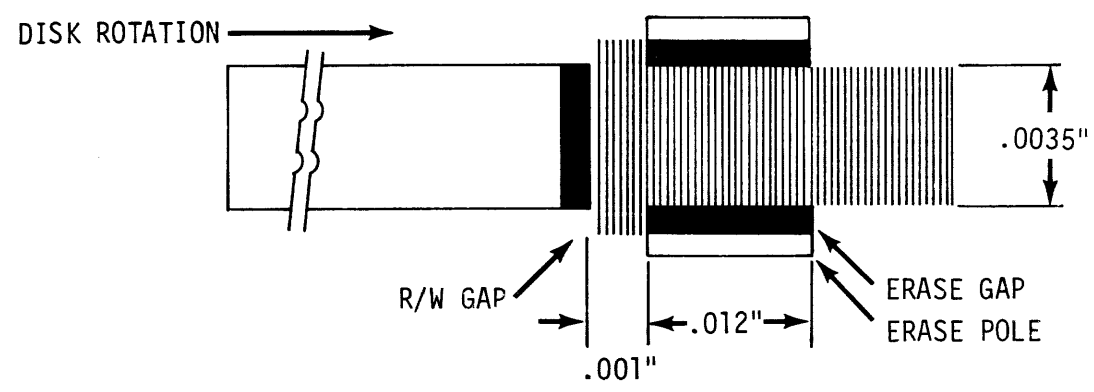
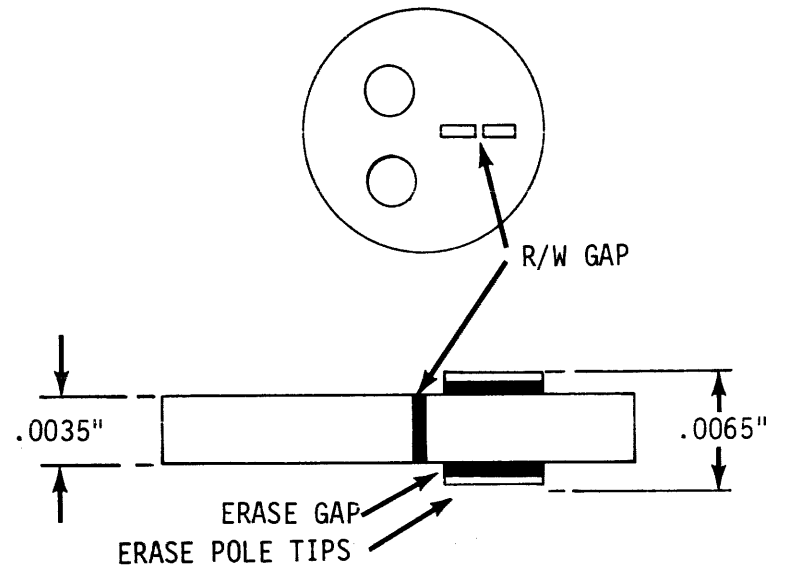
The read/write head detects the flux reversals that are recorded on the oxide-coated disk. This information is amplified and operated upon to re-create the flux reversal pattern.

1.7.6 Discriminator (Optional)

The user is supplied read data in a binary format along with a Clock. The advanced and unique discrimination scheme employed by EMM is capable of accommodating bit shifts that result from head resolution, drive spindle speed variations, etc. (See Figure 1-16.)

1.7.7 Index and Sector Detection

The disk cartridge may contain up to 32 sector notches plus an index notch as may the fixed disk sector ring. The index/sector transducers detect these notches. Detection circuitry provides two lines per disk to the user. One line provides a pulse for each sector and the other line, one pulse per revolution from the index. The Controller may use the Index/Sector pulses to synchronize its sector counter. The index and sector lines also constitute an input to the drive safety circuits, indicating that the spindle is up to speed.



600-11

Figure 1-14. Edge Erase Concept (200 TPI)

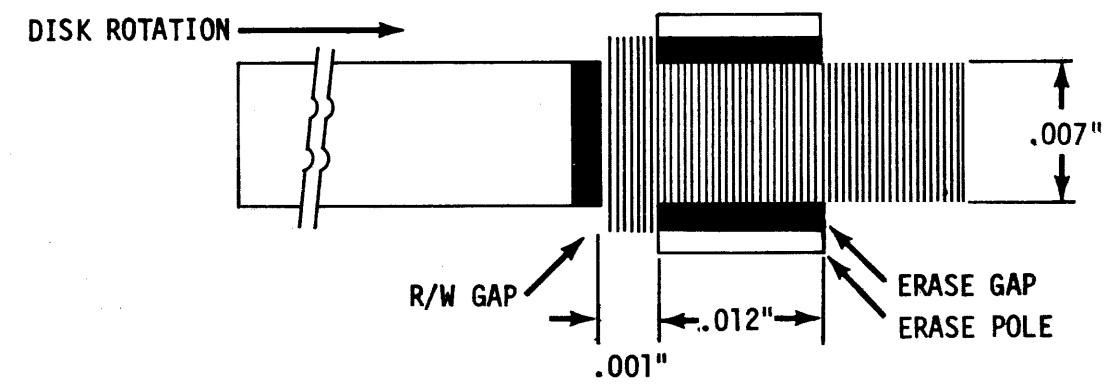
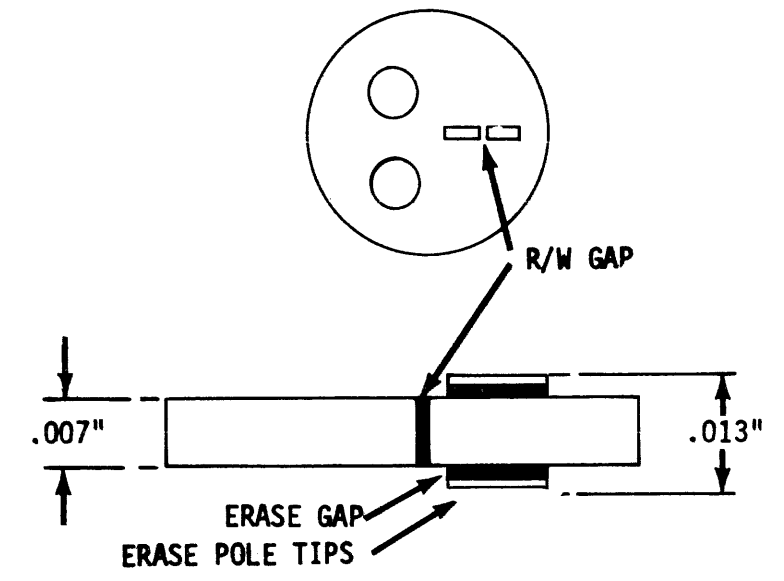
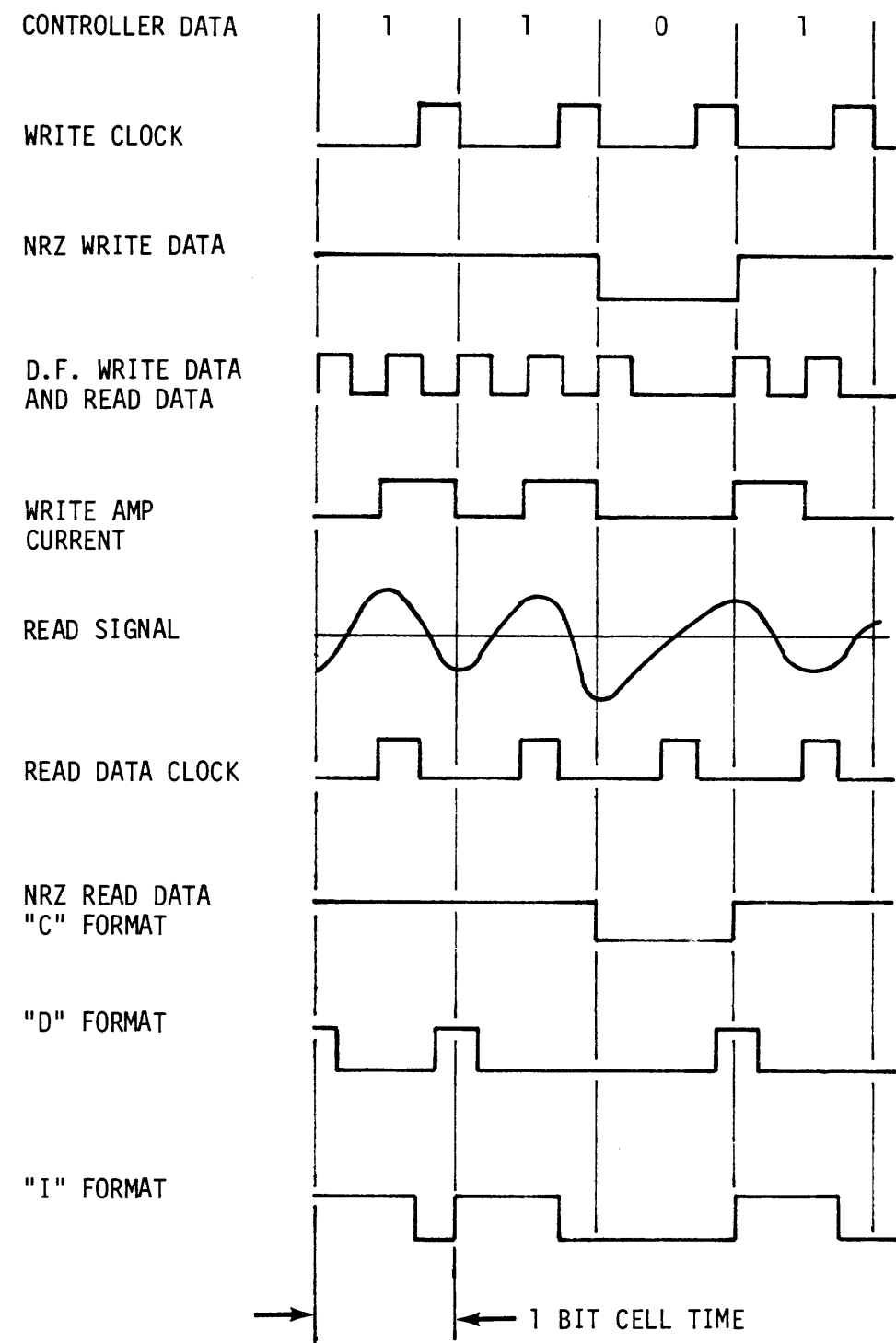


Figure 1-15. Edge Erase Concept (100 TPI)



600-12

Figure 1-16. Recording Waveforms

SECTION 2
INSTALLATION/INTERFACE

2.1 UNPACKING THE DRIVE FOR INSTALLATION

- a. Remove the drive from its shipping container and supports as illustrated in Figure 2-1. The glass tape around the drive provides a lifting handle. A schematic of the installation dimensions is shown in Figures 2-2 and 2-3.
- b. Remove the back cover from the drive.
- c. Remove the carriage holddown screw and flag (Figure 2-5).
- d. Select unit I.D. of file (subsection 2.3).
- e. Replace back cover.

2.2 SPECIAL GROUNDING INSTRUCTIONS

Grounding is provided by the center conductor of the power cord. The wall receptacles in the vicinity of the unit or system are all to be of a grounding type.

2.3 SELECTION OF UNIT IDENTIFICATION

At time of installation, the unit I.D. of each drive must be chosen by a switch on the Input/Output board as follows:

Drive I.D.	Switch Position	
0	1	7
1	2	8
2	3	9
3	4	0

If only one drive is to be connected to the Controller, select Unit I.D. "0," per the above tabulation.

For any drive to be operative, the Controller must select the appropriate Unit Select Line in the I/O cable.

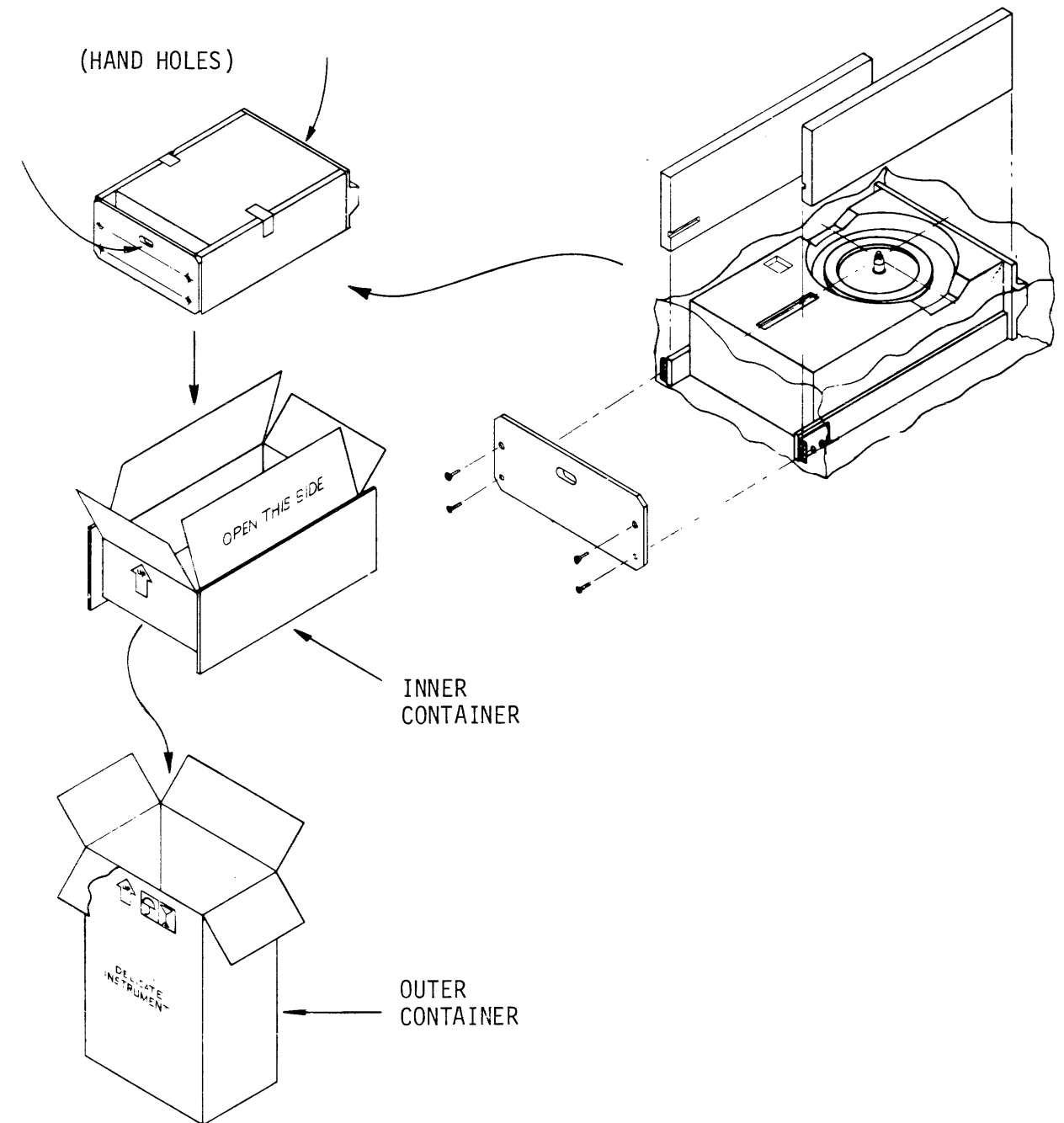
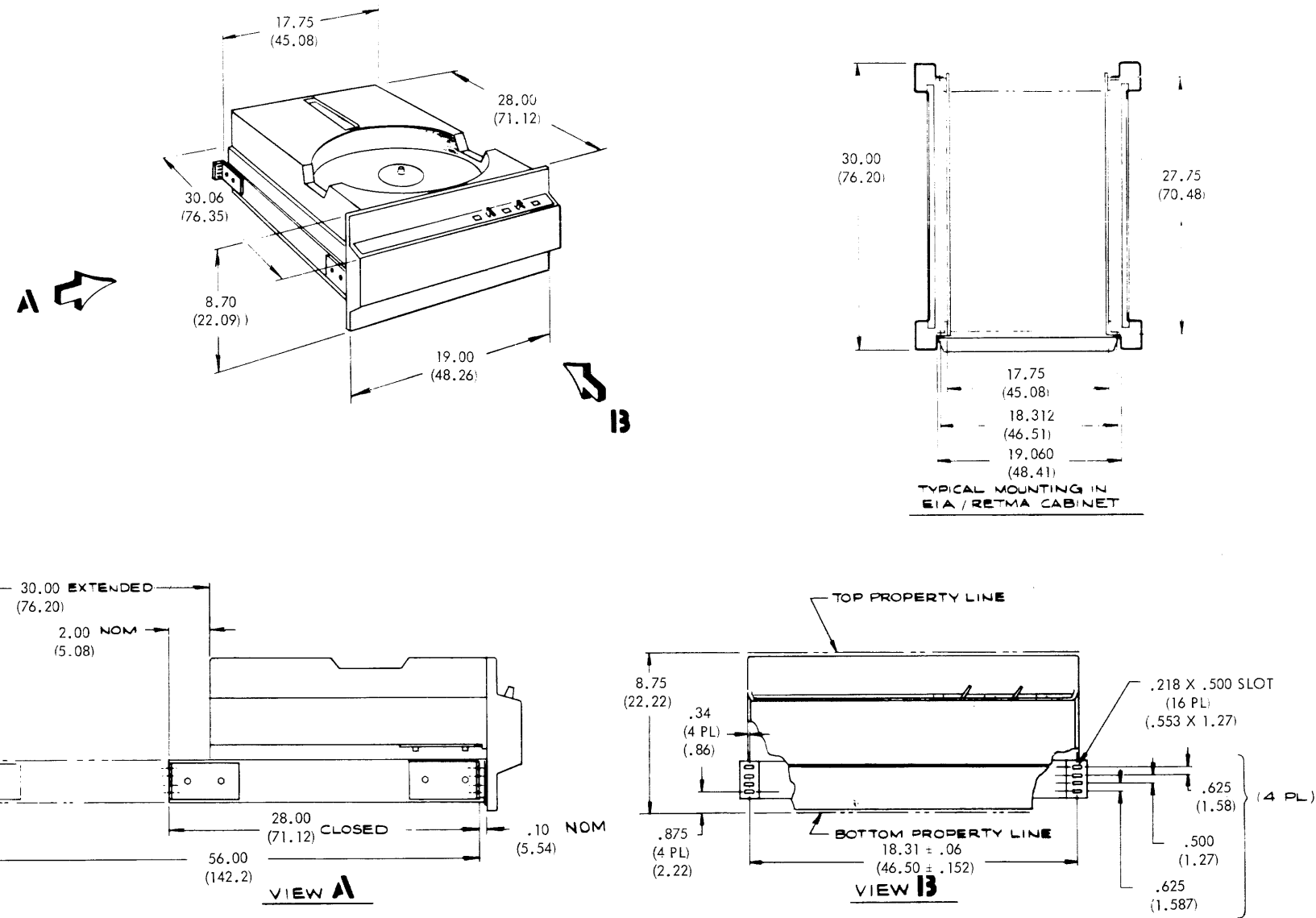


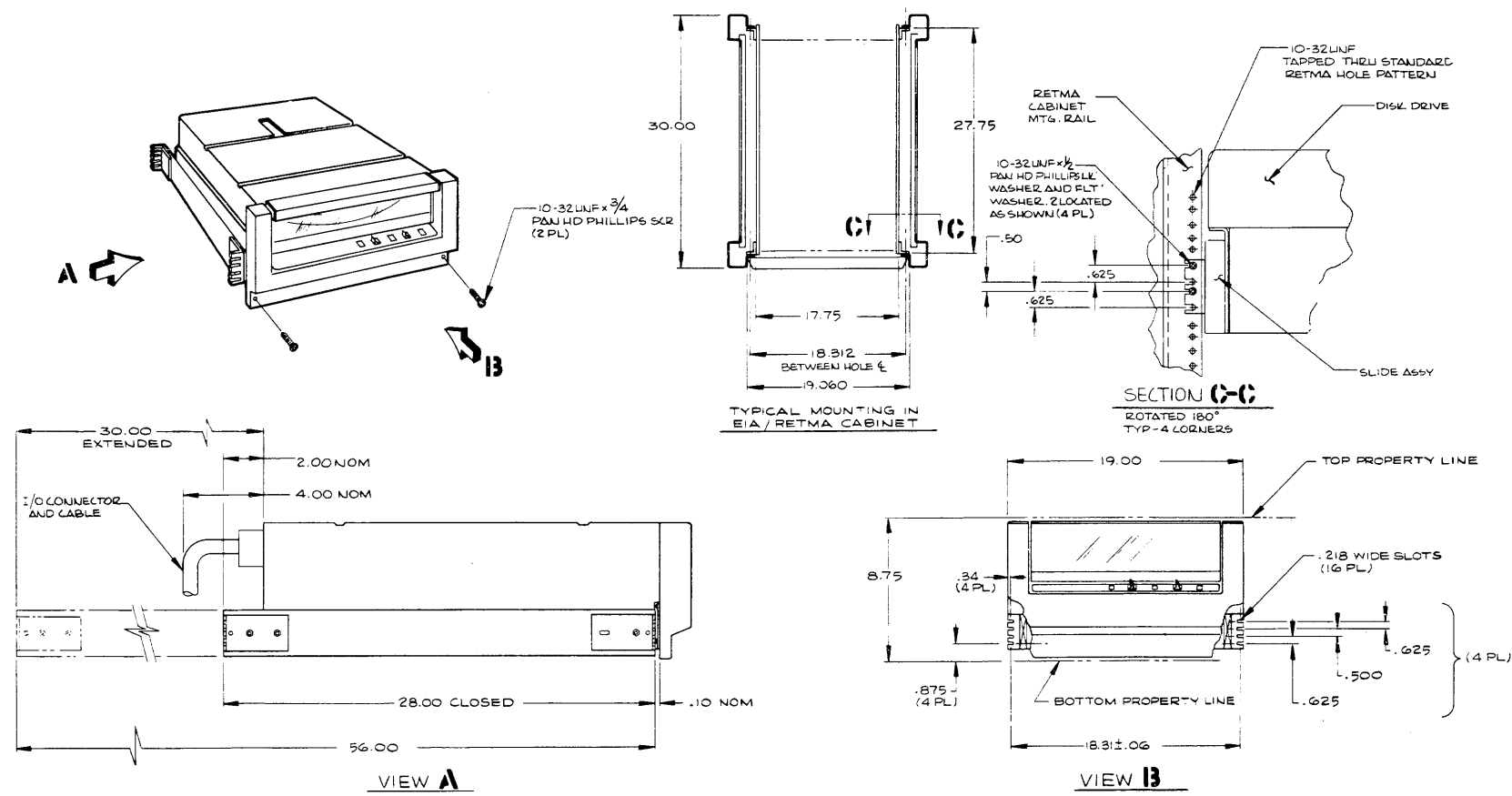
Figure 2-1. Shipping Container



NOTE: All dimensions in parentheses are in centimeters.

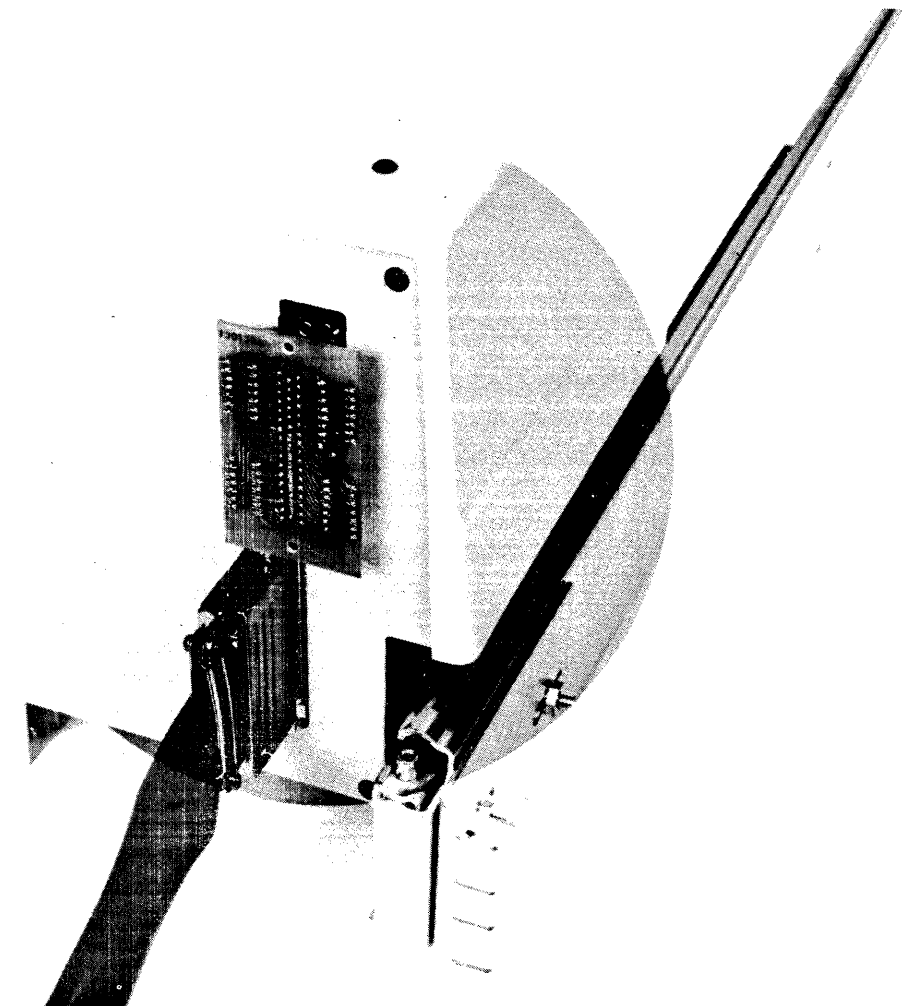
600-14

Figure 2-2. Installation Dimensions (306)



200-15

Figure 2-3. Installation Dimensions (206)



200-16

Figure 2-4. Termination Board and I/O Cable

This page intentionally left blank.

2.4 INPUT/OUTPUT INTERFACE

The I/O interface for data and control signals is an open-collector circuit with resistive termination at driving and receiving ends. The external I/O cable should be terminated with a Cannon DDC-50 connector. Each I/O line is a twisted pair with one side grounded. The terminations are single ended and permit operation at distances up to 50 feet. I/O cables are not normally supplied with the disk cartridge drive.

A termination board and I/O cable are shown in Figure 2-4. Line drivers and receivers are illustrated in Figure 2-7.

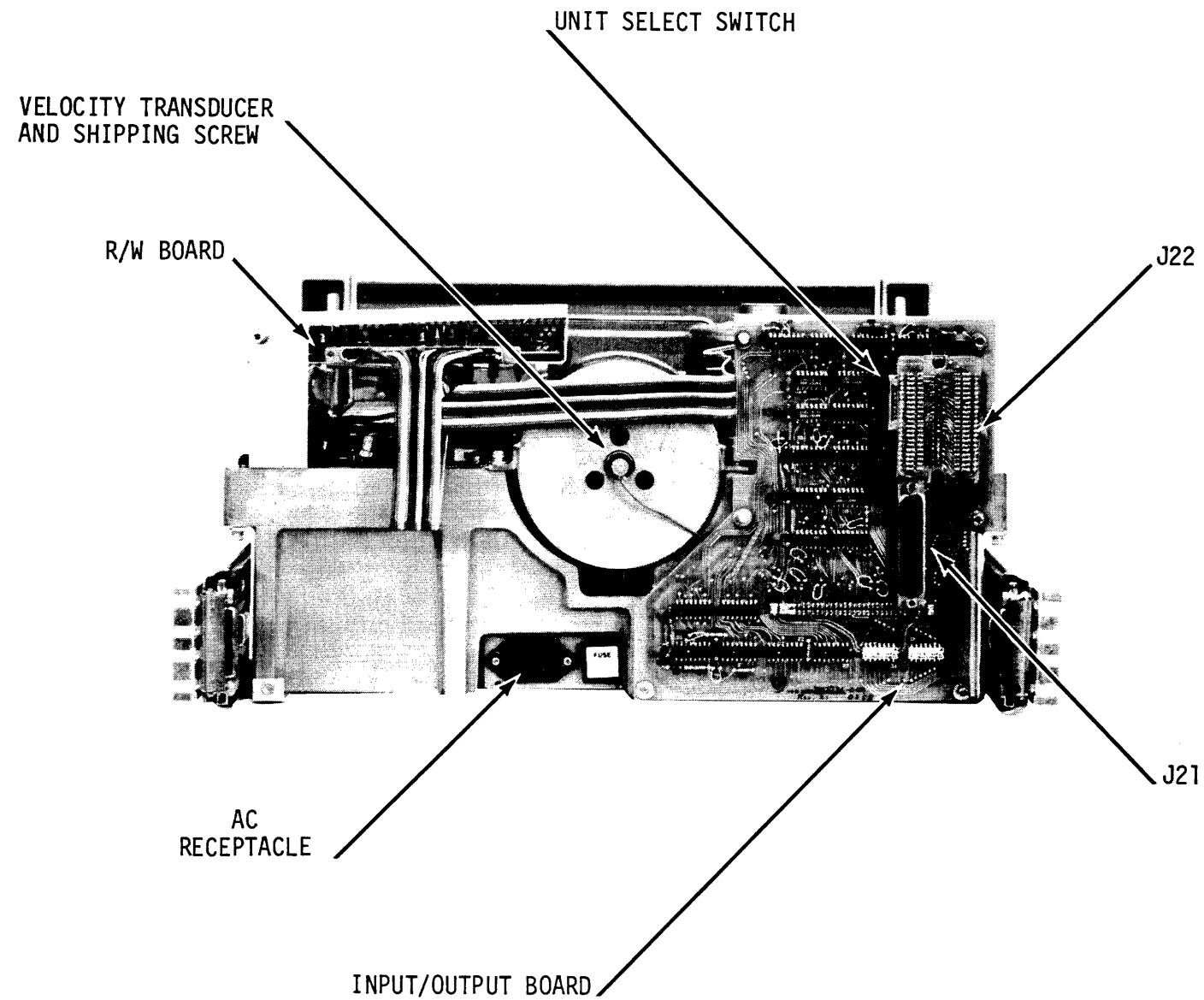


Figure 2-5. Carriage Holddown Screw

600-15

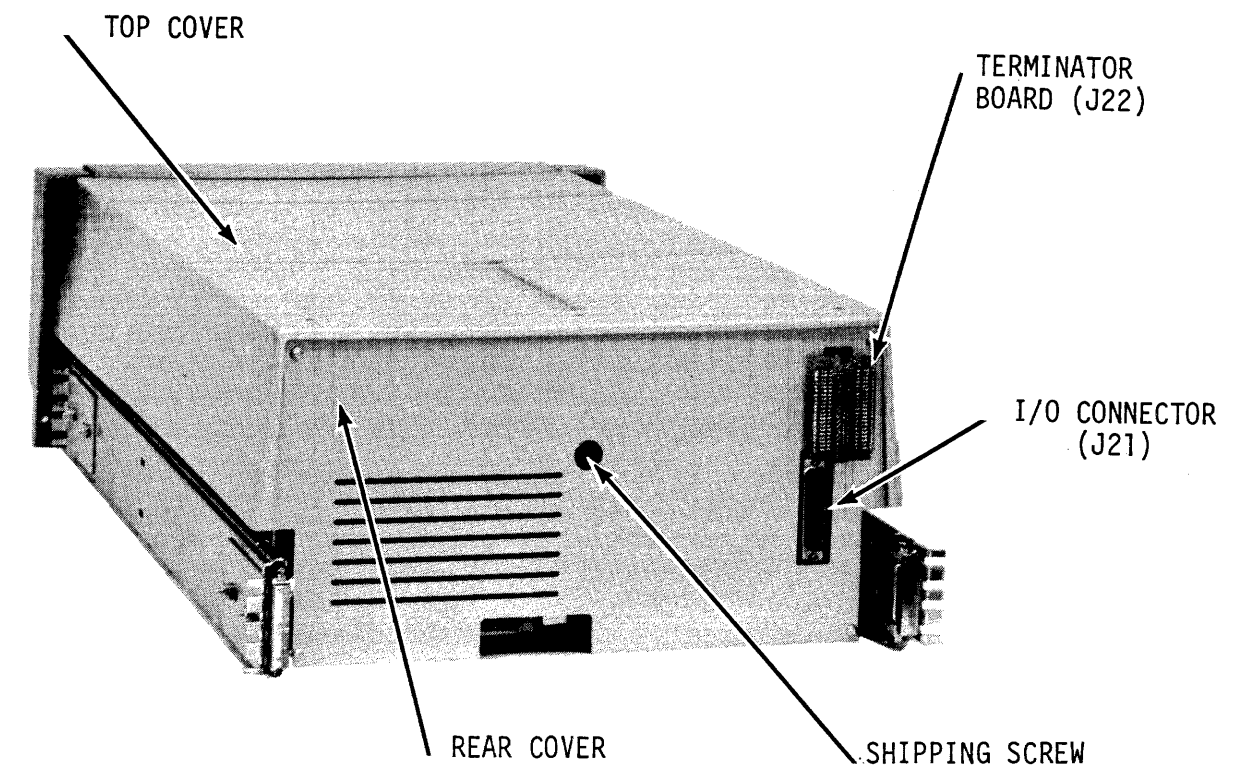


Figure 2-6. Model 206, Rear View

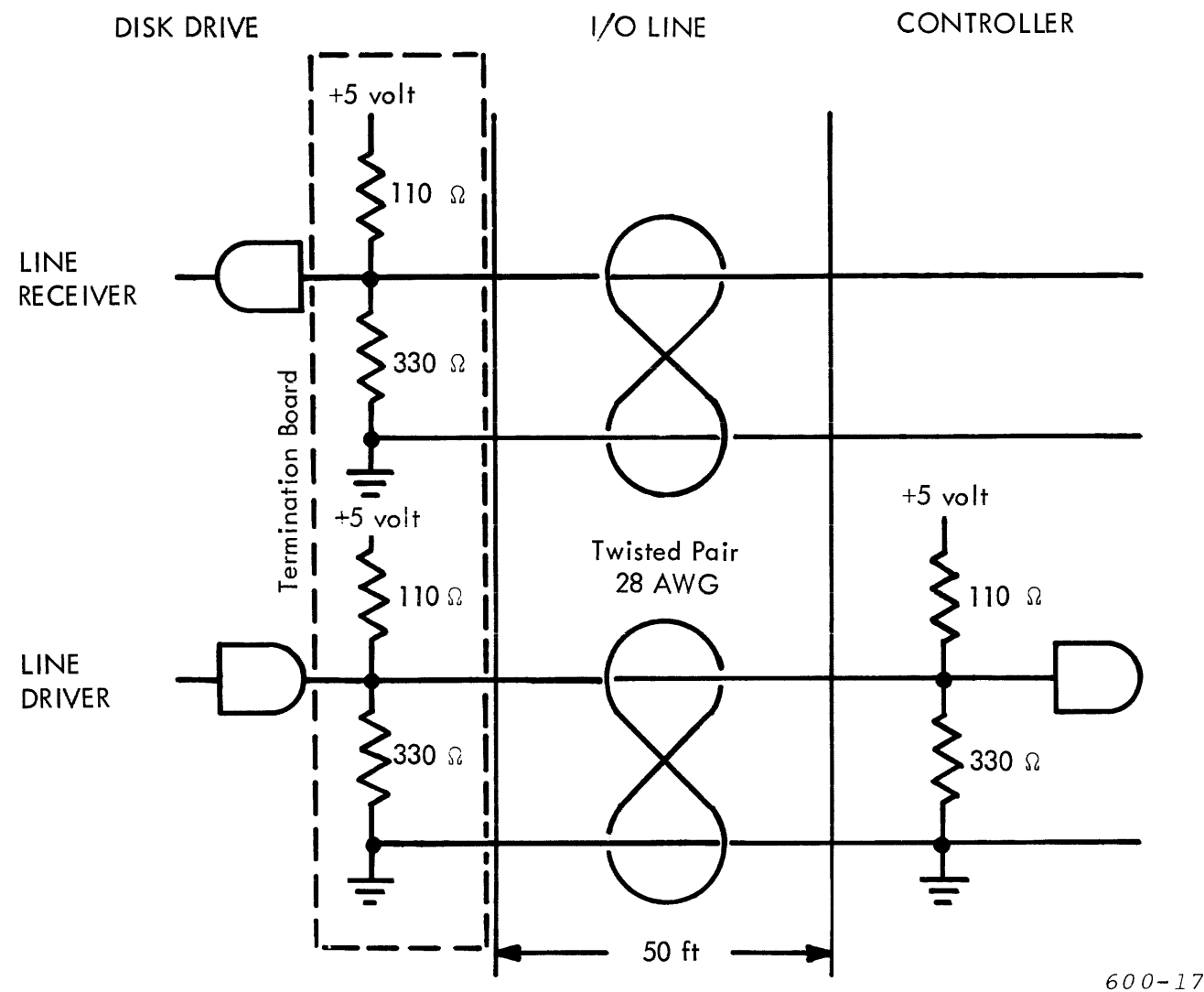


Figure 2-7. Line Drivers and Receivers

2.5 DAISY-CHAIN INTERCONNECTION

The daisy-chain option allows the external control to interface to a maximum of four drives. This option is mechanized by providing each drive with dual I/O connectors and eliminating all line terminations from the drive. An external termination board is required.

The maximum cable length between the Controller and the last drive in the daisy chain must be no more than 50 feet. If no daisy chain is used, the controller cable must be connected to J21 of the single drive and a terminator board is connected to J22.

- a. Termination board must be supplied +5 volts from either the IOB or the Controller, 1/2 amp nominal, 1 amp maximum.

- b. -09 on the terminator to provide +5 volts from the drive;
-19 on the terminator to provide +5 volts from the Controller.

If the daisy-chain feature is used, the controller cable is connected to J21 on the first drive and the daisy-chain cable is connected from J22 on the first drive to J21 on the next drive, etc. The terminator board is connected to J22 on the last drive in the daisy chain. A daisy-chain cabling diagram is illustrated in Figure 2-8.

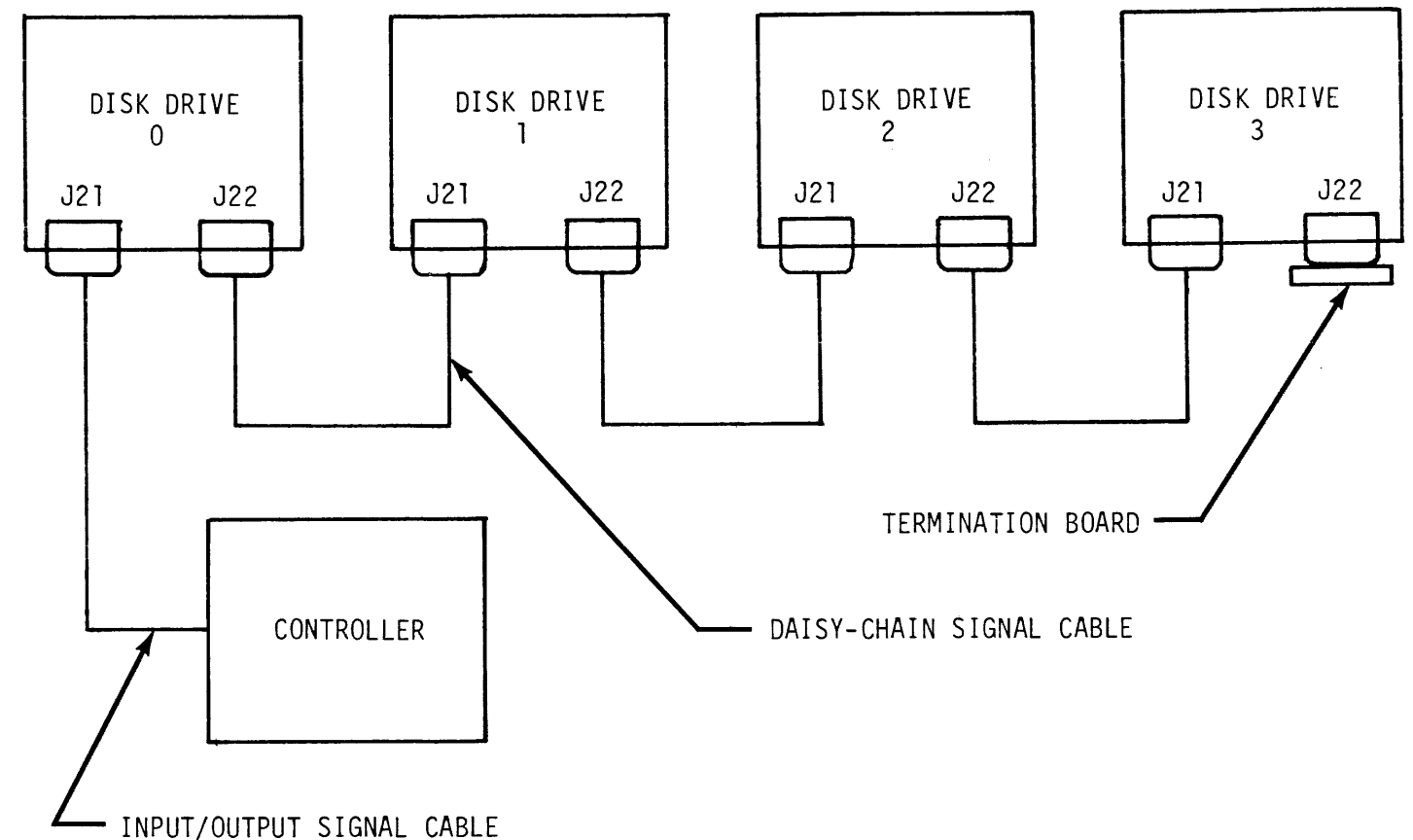


Figure 2-8. Daisy-Chain Cabling Diagram

2.6 LOGIC LEVELS

Logical "1" is signified by a voltage level between 0 and +0.5 volt; logical "0" by a voltage level between +2.5 and +5 volts. The functions of data lines and controls are described in the following paragraphs. (See Figure 2-9.)

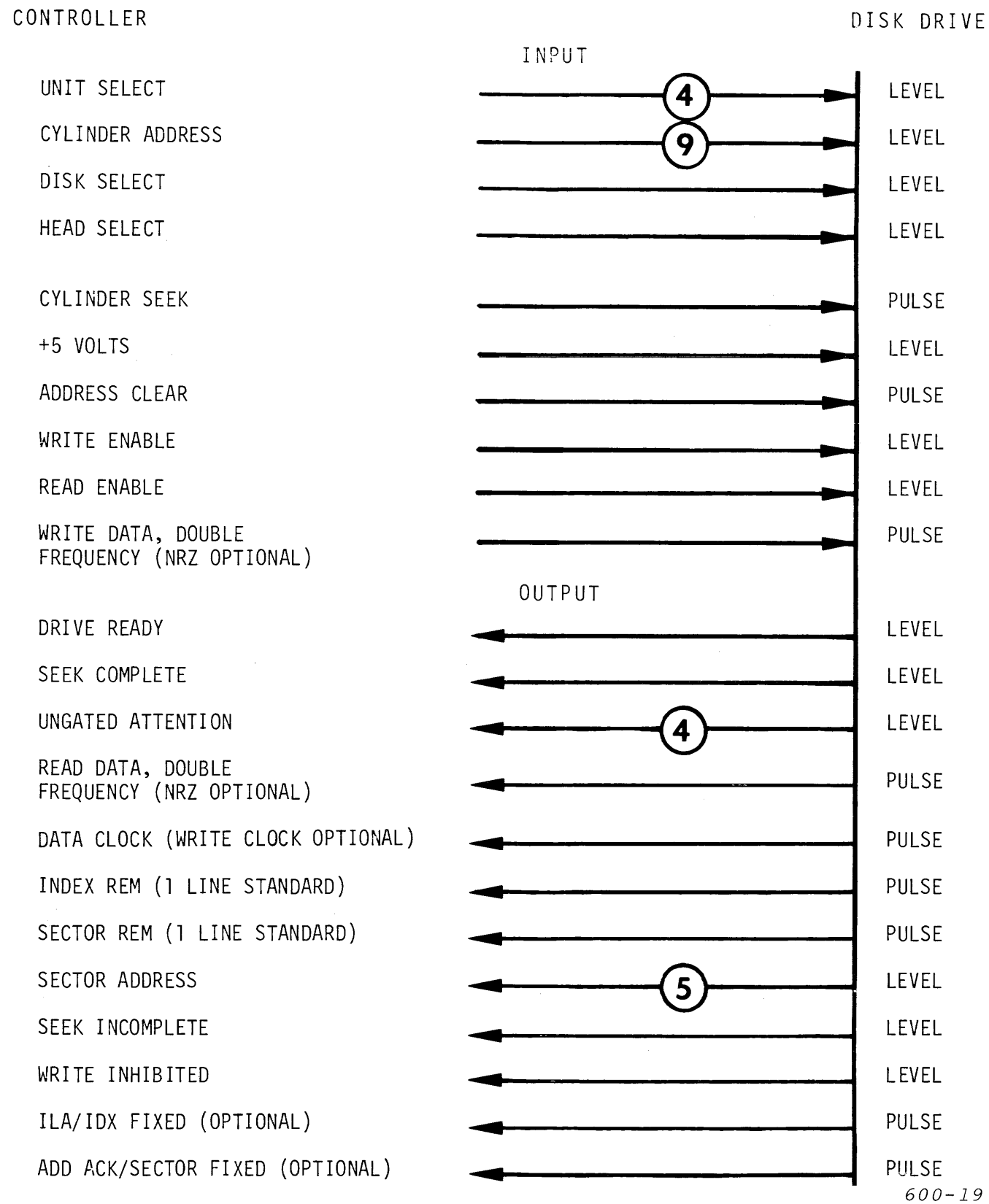


Figure 2-9. Input/Output Interface

2.7 INPUT LINES

All input/output lines are true in the low state.

2.7.1 Cylinder Address

Cylinder Address is transmitted on nine lines. These lines are strobed into a nine-bit address register by the Cylinder Seek pulse to be internally decoded. Each cylinder is addressed by the following binary notation:

	Decimal Cylinder	Binary Address
	000	000 000 000
	001	000 000 001
408 Cylinders	002	000 000 010
	405	110 010 101
	406	110 010 110
	407	110 010 111

2.7.2 Disk Select

Disk Select is a one-input line which selects the fixed disk or the removable disk. The logic necessary for selecting the appropriate disk is made optional by a jumper on the I/O board. (See Table 2-1 and Figure 2-10).

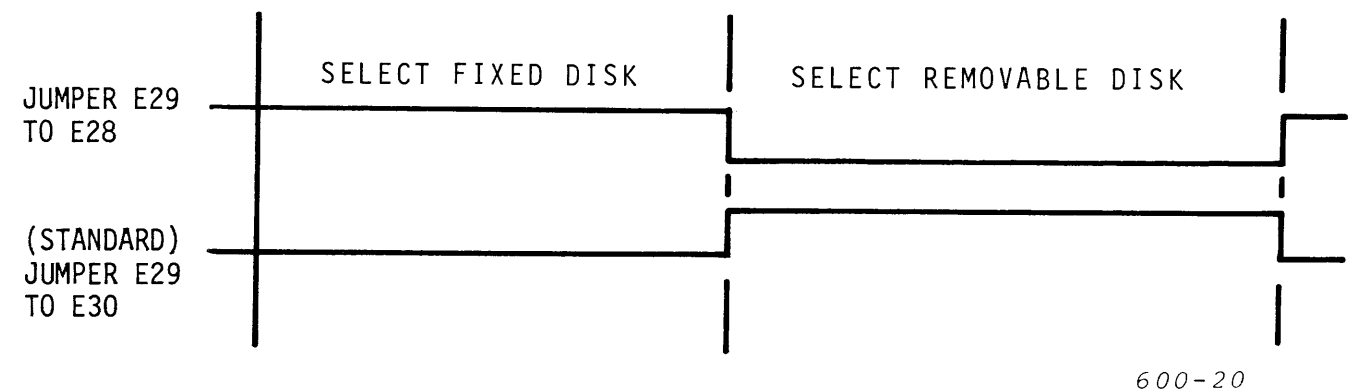


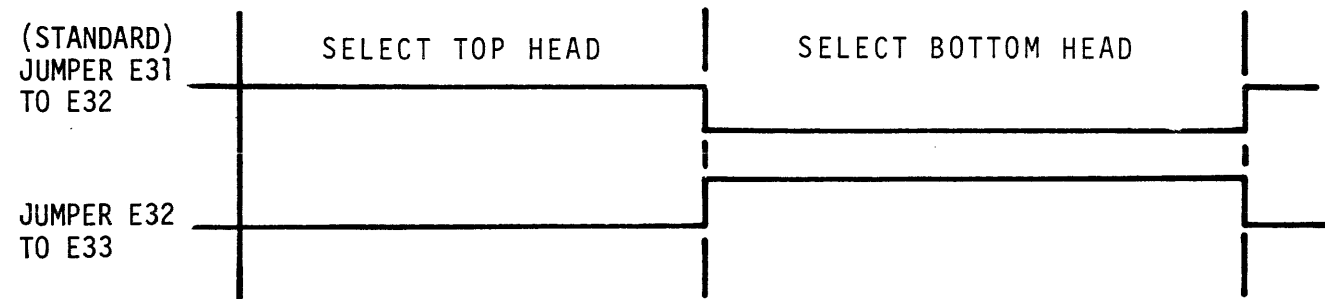
Figure 2-10. Disk Select Timing

2.7.3 Head Select

The logic that permits this line to select the top disk surface or the bottom disk surface is optional by selecting the appropriate jumper on the I/O board. (See Table 2-1 and Figure 2-11).

NOTE

Head Select is not gated with Unit Select.

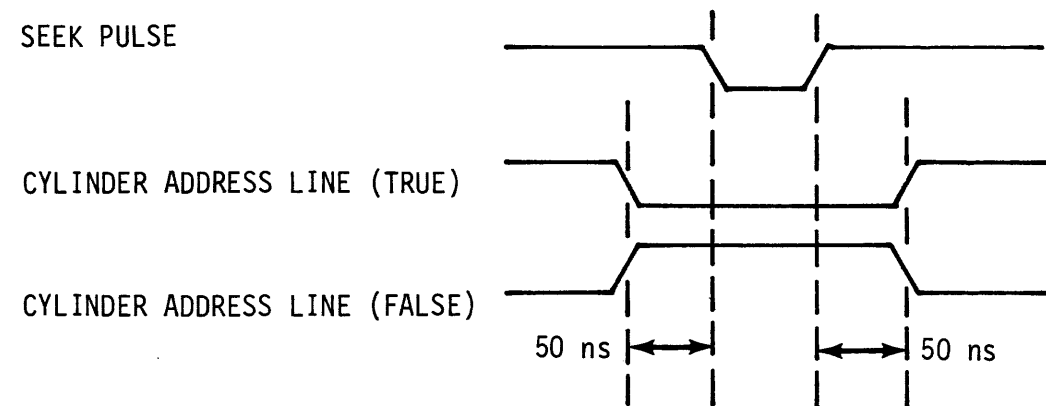


600-21

Figure 2-11. Head Select Timing

2.7.4 Cylinder Seek

This line provides a pulse with a minimum width of 600 ns that strobes the address information into the nine-bit address register in the drive unit. The pulse initiates the Cylinder Seek action. See Address Clear for reinitialization. (Refer to Figure 2-12.)



600-22

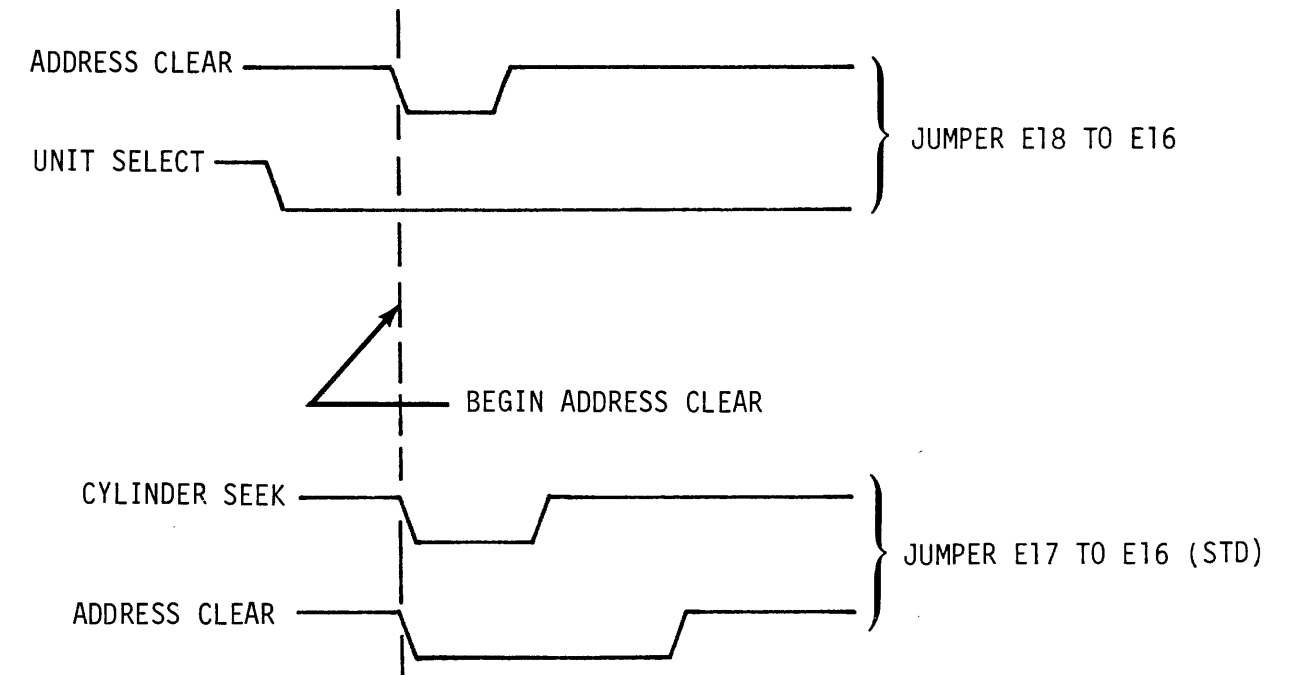
Figure 2-12. Cylinder Address Timing

2.7.5 Controller Supplied +5 Volts (Optional)

The +5 volts DC from the Controller is fed through the I/O cable and daisy-chain cables to the terminator board, where it is used to drive the resistor networks of the terminator. In the event of a power shutdown of any drive in the daisy chain, the terminator will still be able to drive the I/O cable using the power source. As an additional option, the heads can be made to retract and go to the home positions when this line goes to ground.

2.7.6 Address Clear

Address Clear is a pulse which (when used in conjunction with the Seek command or Unit Select) will automatically position the heads at track "0." This function is automatic when an illegal address is issued unless defeated by an optional jumper on the I/O board. (See Figure 2-13 and Table 2-1.)



600-23

Figure 2-13. Address Clear Timing

Table 2-1. Input/Output Board Options

ITEM	OPTION	JUMPERS	DESCRIPTION
1	a	E49 to E48	With Sector Multiplexing Standard
	b	None	Without Sector Multiplexing
2	a	E5 to E6 E41 to E40 E44 to E43 E47 to E46	Illegal Address, Address Acknowledge Pulses
	b	E41 to E40 E44 to E43 E47 to E46	Illegal Address, Address Acknowledge Level
	c	E41 to E39 E44 to E42 E47 to E45	Fixed Disk Sectors and Indexes
3	a	E10 to E9	Seek Incomplete with Illegal Address
	b	None	Seek Incomplete without Illegal Address
4	a	E20 to E21	Seek Complete Standard
	b	E20 to E19	Seek Complete Inverted
	c	E20 to E57	Gated Attention
5	a	E7 to E8	With Automatic Address Clear
	b	None	Without Automatic Address Clear
6	a	E50 to E52	Retract with Controller Power Loss
	b	E52 to E51	No Retract with Controller Power Loss

Table 2-1. Input/Output Board Options (continued)

ITEM	OPTION	JUMPERS	DESCRIPTION
7	a	E31 to E32	Head Select Standard
	b	E32 to E33	Head Select Inverted
8	a	E29 to E30	Disk Select Standard
	b	E29 to E28	Disk Select Inverted
9	a	E17 to E16	Address Clear Gated with Seek Pulse
	b	E18 to E16	Address Clear Gated with Unit Select
10	a	E37 to E38	Index Pulse Only
	b	None	Index and Sector Pulses
11	a	Standard, E11 to E12	Full Capacity
	b	No Option, E12 to E13	Half Capacity
12	a	E25 to E26	Double Frequency Data In
	b	E27 to E26	NRZ Data In
13	a	E23 to E24	NRZ Data Out
	b	E22 to E24	Double Frequency Data Out
14	a	E34 to E36	200 TPI Status (-) Negative
	b	None	200 TPI Status (+) Positive

2.7.7 Write Enable

This line turns on the write amplifiers and edge erase when in the true state. The line must go false after the write operation has been completed.

2.7.8 Read Enable

This line turns on the read data circuitry in the true state; the double-frequency data or the optional discriminator outputs will be placed on the Read Data and Clock lines.

2.7.9 Write Data

The Write Data line carries the double-frequency encoded write data from the Controller. NRZ encoding of write data is an option.

2.7.10 Unit Select

Unit Select consists of four lines and is selectable by a switch on the I/O board within each drive, allowing each drive to be selected by any one of the four lines.

2.8 OUTPUT LINES

Unless noted, all output lines are active when the unit is selected. The input/output pin assignments are listed in Tables 2-2 and 2-3.

2.8.1 Drive Ready

This line indicates to the user that the disk drive is ready for operation. When the drive has achieved operational speed, all interlocks and safety circuits are satisfied, and the drive is within temperature operating range. The heads are positioned over track "0" and the line goes to a true level.

2.8.2 Seek Complete

This line is gated with Unit Select and supplies a level to the user, indicating that the heads are positioned and stabilized. The drive is then ready to accept Read or Write commands. If an optional jumper is specified, Seek Complete will indicate busy seeking.

2.8.3 Ungated Attention

This function consists of four lines and is selectable by a switch on the I/O board. This signal indicates one of the following: that the heads are positioned and stabilized, an illegal address has been written, or the heads are not stabilized in 330 milliseconds. This signal is not gated with Unit Select.

2.8.4 Read Data

The Read Data line transmits double-frequency encoded read data to the Controller. When the NRZ option is specified, this line transmits decoded NRZ data. (See Tables 2-1, 2-5, and Figure 2-14.)

2.8.5 Data Clock (Write Clock Optional)

This line transmits the 1588.5 kHz at 1,500 rpm, 2,500 kHz at 2,400 rpm, write or read clock for the data. The clock output is used by the Controller to strobe the data.

2.8.6 Index

The Index line supplies a pulse for the index reference point on the disk. The index pulse is normally used to synchronize the Controller's sector counter. This line is multiplexed by the Disk Select line. Individual index lines for each disk are optional by jumper on the I/O board. (See Table 2-1.)

2.8.7 Sector (Optional)

This line supplies a pulse at the beginning of each sector and is normally used to advance the Controller's sector counter. This line is multiplexed by the Disk Select line. Individual sector lines for each disk are optional by jumper on the circuit board. (See Table 2-6.)

2.8.8 Sector Address

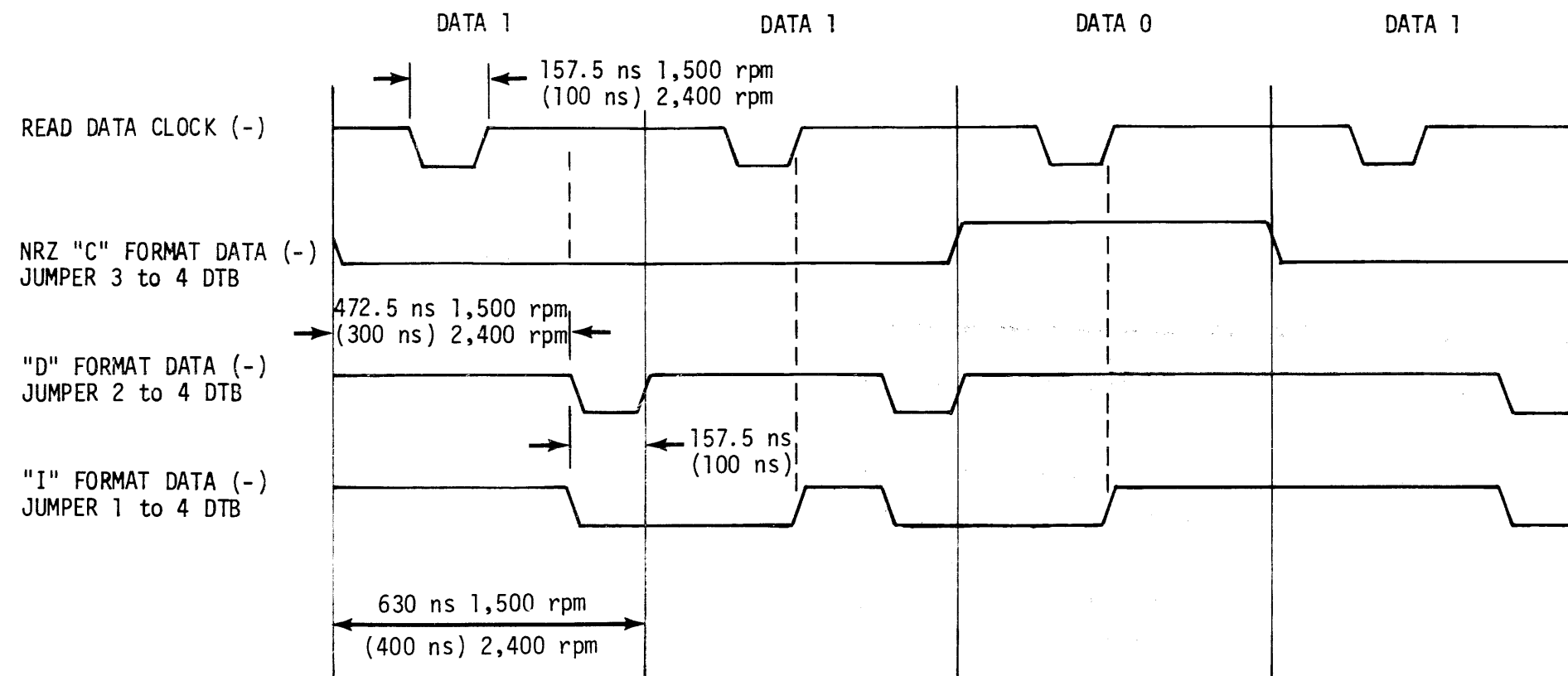
Sector Address consists of five lines which supply Sector Address information in binary format to the Controller. Sector Address is reset to "0" by the trailing edge of the first sector pulse after the index pulse; and the sector counter is advanced by the trailing or leading edge of each sector pulse as determined by jumpers on the control sector board.

2.8.9 Seek Incomplete

This line supplies a true level 330 milliseconds after the Cylinder Seek pulse, if the Seek Complete line indicates that an address has not been executed. This line may also indicate a Seek Incomplete if an illegal address has been given as long as the appropriate jumper on the I/O board is selected. This line will be reset by the next Seek pulse or optionally by an automatic Address Clear. (See Figures 2-15 through 2-19.)

2.8.10 Write Inhibited

This line is true for all times that the Write Operation is inhibited and is gated with Unit Select.



600-24

Figure 2-14. Read Data Timing at Interface

2.8.11 ILA/IDX FXD

This line may be either an Illegal Address signal or a Fixed Index signal by selecting the appropriate jumpers on the I/O board. If the ILA is selected, a pulse 2.3 microseconds wide approximately 23 microseconds from the Cylinder Seek line will appear when an illegal address is detected. If IDX FXD is selected, the fixed index pulse will appear at the appropriate time. (See Table 2-1.)

2.8.12 ADD ACK/Sector FXD

This line may be either an Address Acknowledge signal or a Fixed Sector signal by selecting the appropriate jumpers on the I/O board. If address acknowledge is selected, a 2.3-microsecond pulse approximately 23 microseconds after Cylinder Seek will appear if a legal address is selected. If Fixed Sector is selected, sector pulses from the Fixed Disk will appear at the appropriate time. (See Table 2-1 and Figures 2-15 through 2-19.)

2.9 OPERATOR CONTROLS AND INDICATORS

An operator control panel, which may be mounted remotely, is mounted on the front of the drive and contains the functions described below.

2.9.1 Power Switch

The Power switch is mounted on the front panel of the disk drive. When activated, AC power is applied to the drive.

2.9.2 Power Indicator

When lit, the Power Indicator indicates the AC power is applied to the drive.

Table 2-2. Input Pin Assignments

DESCRIPTIONS	PIN NUMBER		RETURN PIN NUMBER
	200 TPI	100 TPI	
INPUTS:			
Address 2 ⁰	26	9	27
Address 2 ¹	9	5	27
Address 2 ²	5	8	20
Address 2 ³	8	4	21
Address 2 ⁴	4	11	19
Address 2 ⁵	11	7	27
Address 2 ⁶	7	10	21
Address 2 ⁷	10	6	22
Address 2 ⁸	6	N/A	20
+5 Volts (Retract by Controller power loss)	28	28	27
Address Clear	48	48	27
Seek	33	33	27
Unit Select 0	46	46	27
Unit Select 1	29	29	27
Unit Select 2	45	45	27
Unit Select 3	44	44	27
Head Select	32	32	27
Disk Select	49	49	27
Clock (Write/Read)	38	38	22
Read Enable	30	30	27
Write Enable	31	31	27
Write Data	50	50	27

NOTE

The shift of address bits is utilized such that compatibility is accomplished between 100 TPI and 200 TPI units.

Table 2-3. Output Pin Assignments

DESCRIPTIONS	PIN NUMBER		RETURN PIN NUMBER
	200 TPI	100 TPI	
OUTPUTS:			
*+5V	17	17	27
Sector Address 2 ⁰	14	14	27
Sector Address 2 ¹	12	12	27
Sector Address 2 ²	13	13	27
Sector Address 2 ³	15	15	27
Sector Address 2 ⁴	16	16	27
Unit Address 0	43	43	21
Unit Address 1	42	42	21
Unit Address 2	41	41	22
Unit Address 3	40	40	22
Read Data	35	35	19
Seek Complete	39	39	20
Seek Incomplete	36	36	19
Ready	37	37	19
Index Removable	2	2	18
Sector Removable	3	3	18
Index Fixed/ILA	1	1	18
Sector Fixed/Add Ack	34	34	18
Write Inhibited	47	47	27

*Note: Termination voltage only and not supplied to output connector.

Table 2-4. Drive Control Board Options

OPTION	JUMPERS	DESCRIPTION
a	E1 to E2	306 Top Loader
b	E1 to E3	206 Front Loader

Table 2-5. Data Translator Board Options

ITEM	OPTION	JUMPERS	DESCRIPTION
1	a	E5 to E6	Double Frequency Data In
	b	None	NRZ Data In
2	a	E3 to E4	Caelus Formatted Data Out
	b	E2 to E4	Diablo Formatted Data Out
	c	E1 to E4	Iomec Formatted Data Out

Table 2-6. Control Sector Board Options

OPTION	JUMPER	DESCRIPTION
a	E2 to E1 E5 to E4 E8 to E7 E11 to E10	Sector Counting on Leading Edge of Notch
b	E3 to E1 E6 to E4 E9 to E7 E12 to E10	Sector Counting on Trailing Edge of Notch

Table 2-7. Read/Write Board Options (200 TPI R/W)

OPTION	JUMPER	DESCRIPTION
a	E3 to E5	Write Inhibit Switch On
b	E4 to E5	Write Inhibit Switch On Plus Write Inhibit
c	E4 to E5 E1 to E2	Write Inhibit Plus Write Inhibit Switch On and Write Inhibit Status Inactive Except During Write Enable

Table 2-8. Read/Write Board Options (100 TPI 1,500 rpm)

SEE 301171 SCHEMATIC

Table 2-9. Read/Write Board Options (100 TPI 2,400 rpm)

OPTION	JUMPER	DESCRIPTION
a	A to C	Write Inhibit Switch On
b	B to C	Write Inhibit Switch On Plus Write Inhibit
c	B to C E1 to E2	Write Inhibit Plus Write Inhibit Switch On and Write Inhibit Status Inactive Except During Write Enable

2.9.3 Start/Stop Switch

The Start/Stop switch is a maintained contact switch which applies power to the spindle motor and initiates the start-up cycle when it is turned to the start mode. When put in the stop mode, it removes power from the spindle and initiates the stop cycle.

2.9.4 Ready Indicator

At the successful completion of the start-up cycle, the Ready Indicator is lit.

2.9.5 Stop Indicator

At the conclusion of the stop cycle, when the motor comes to a complete stop and the disk cartridge is unlocked, the Stop Indicator is lit.

2.9.6 Write Inhibit Switches

Write Inhibit switches are mounted on the top of the disk drive shroud, one for each of the two disks. When activated, the respective disk cannot be written upon. (See Table 2-7.)

2.10 OPTIONS

2.10.1 Fixed Sector Format

When this option is specified, the drive supplies sector pulses to the external control. This option requires the use of a special cartridge such as EMM-Caelus CMIII-2X/24.

2.10.2 Data Encoding/Decoding

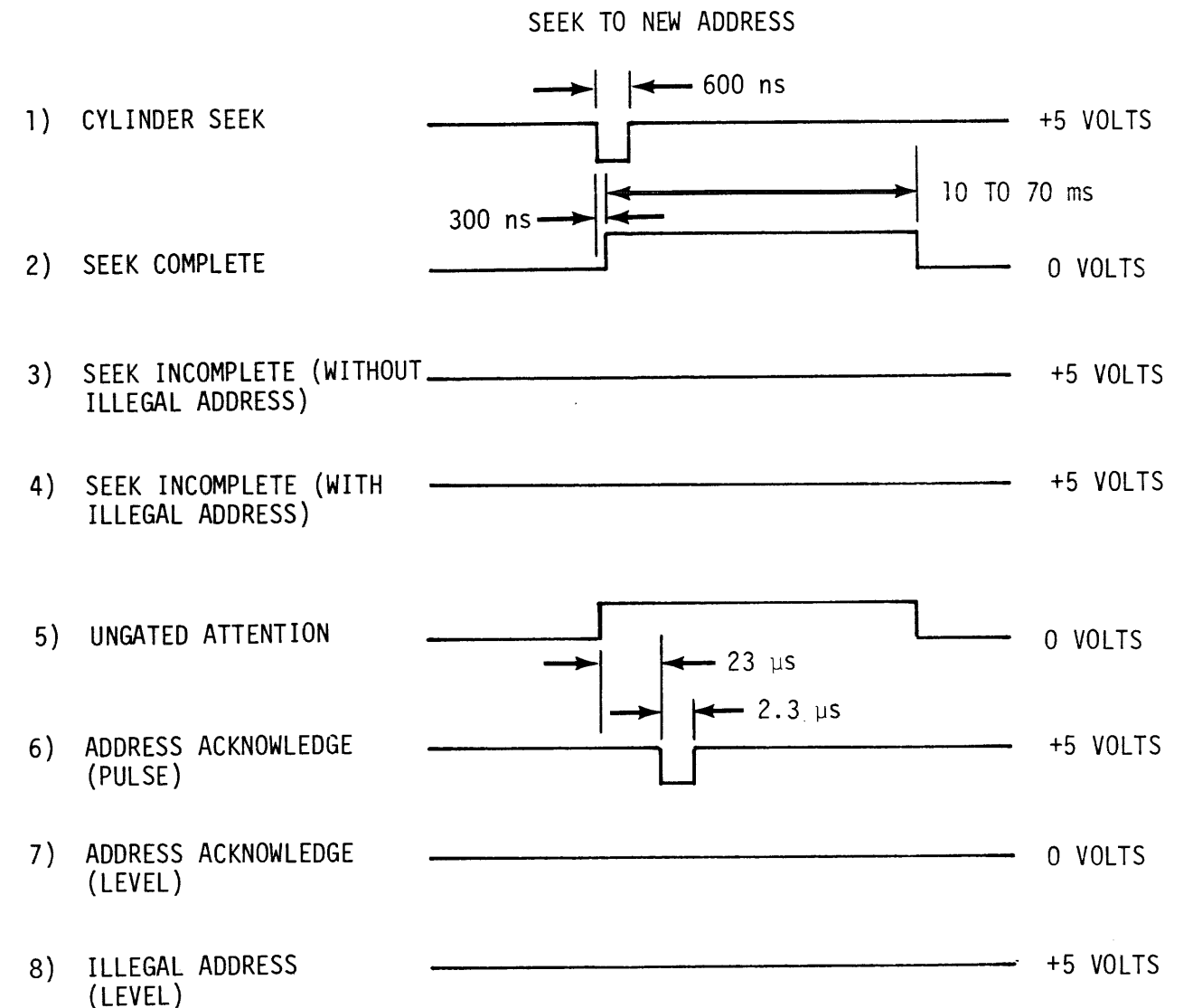
This option provides a crystal clock in the drive. It accepts data in NRZ form and encodes into double frequency for recording. In read mode, a data discriminator is provided to separate clock and data.

2.10.3 Data Decoding (Double Frequency)

For the user who supplies data in double-frequency format, a read discriminator is available to separate clock and data. (See Table 2-1.)

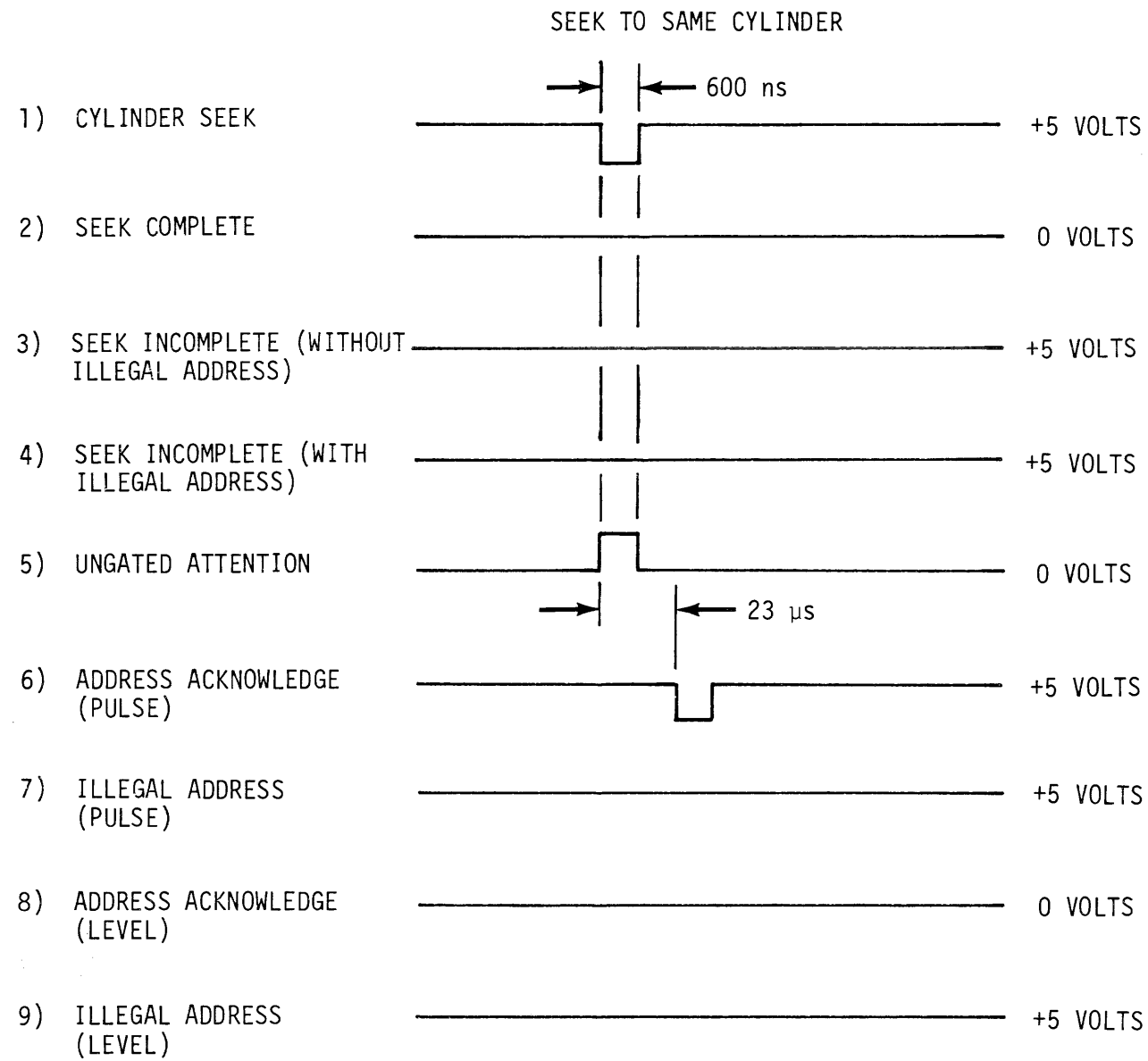
2.10.4 Sector Counter

A five-line, binary-format, sector address is provided. The sector counter outputs are multiplexed by the disk select line and are gated with Unit Select.



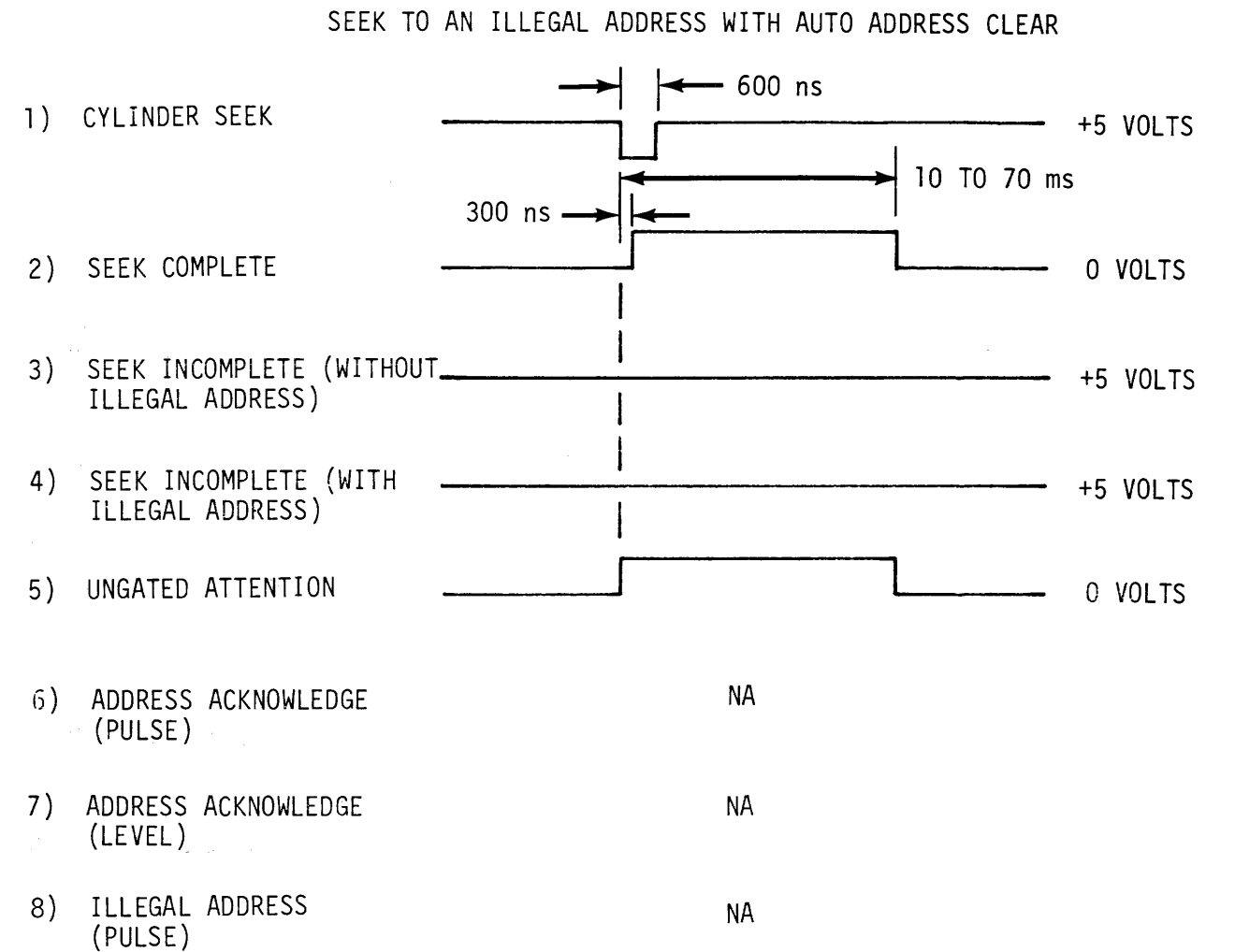
600-25

Figure 2-15. Seek Mode Timing Diagram, Sheet 1 of 5



600-26

Figure 2-16. Seek Mode Timing Diagram, Sheet 2 of 5



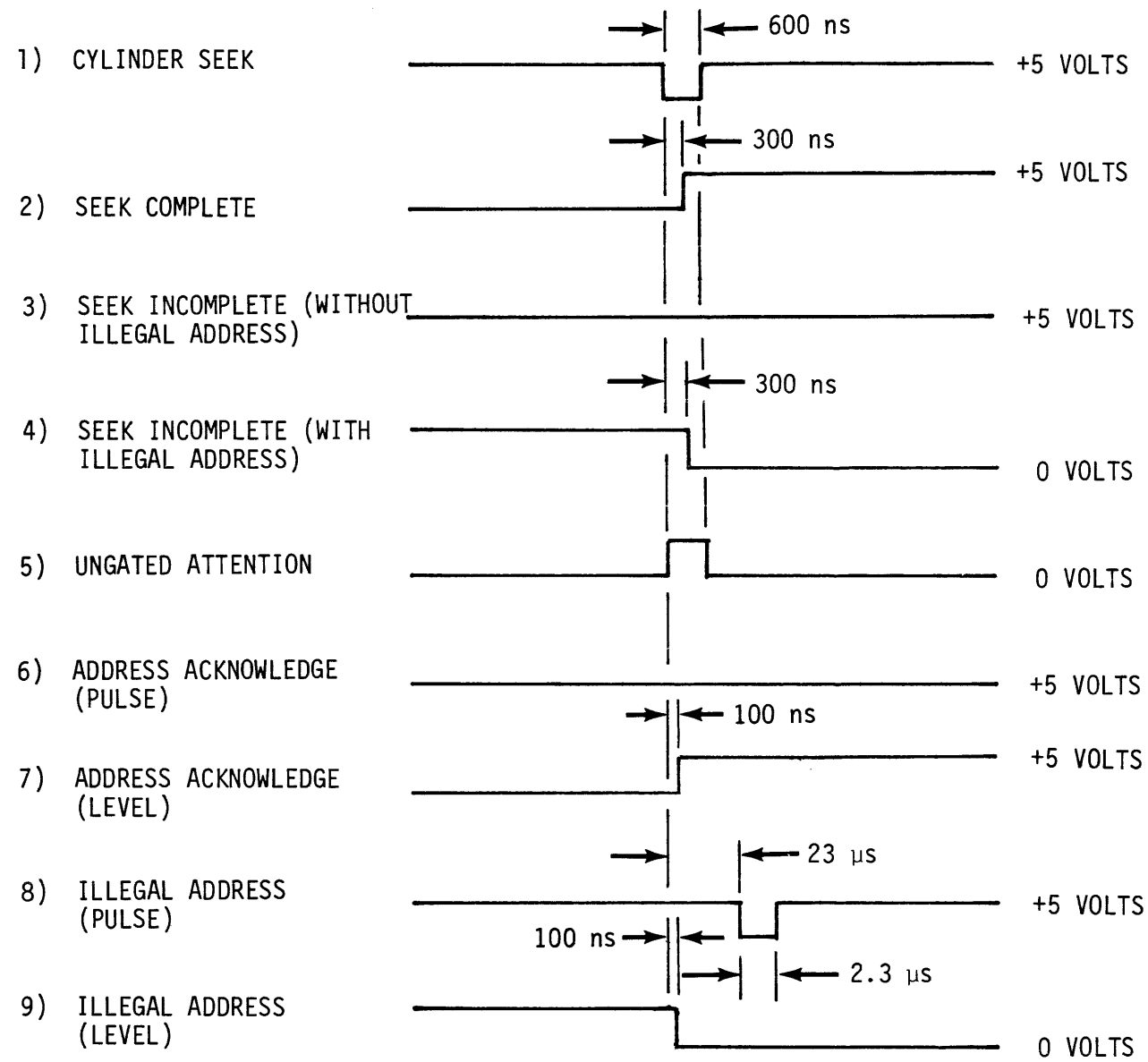
NOTE

In the auto address clear condition, Illegal Address and Address Acknowledge signals are not valid.

600-27

Figure 2-17. Seek Mode Timing Diagram, Sheet 3 of 5

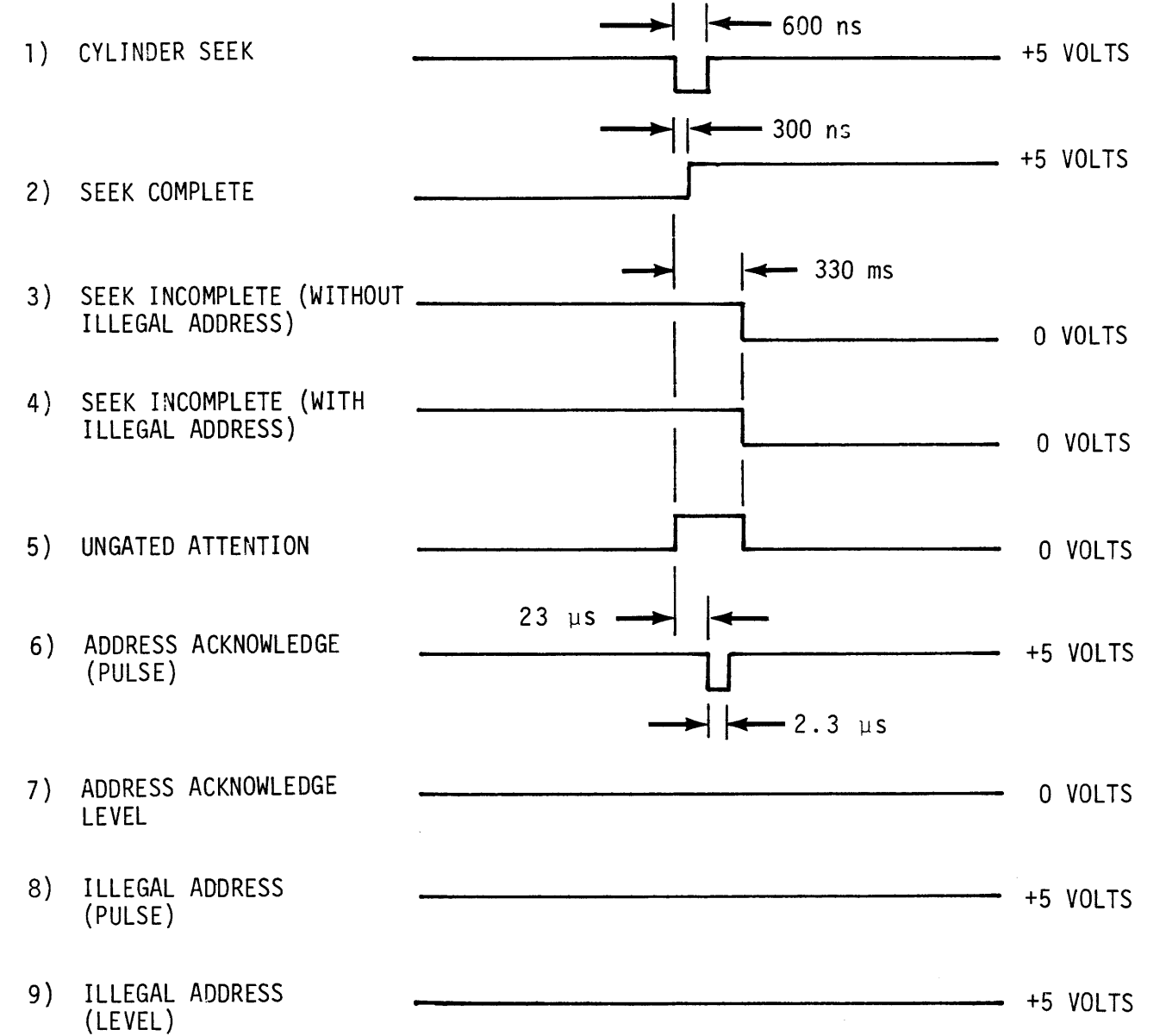
SEEK TO AN ILLEGAL ADDRESS WITHOUT AUTO ADDRESS CLEAR



600-28

Figure 2-18. Seek Mode Timing Diagram, Sheet 4 of 5

SEEK TO NEW ADDRESS OPTION NEVER FINISHES



600-29

Figure 2-19. Seek Mode Timing Diagram, Sheet 5 of 5

SECTION 3
OPERATION

3.1 GENERAL

The magnetic recording disk is a precision instrument, requiring more careful handling than other media such as tape. This is most clearly seen in its relationship with the disk drive. The read/write heads on the disk drive float above the disk surfaces at 60 to 100 millionths of an inch. There is no actual physical contact between the heads and the disk except during the loading operation. This means that any deviation from an ultra-flat, uniform disk (or any particle larger than about 60 millionths of an inch, such as a cigarette ash or any other kind of contaminant) could cause head-to-disk interference and possible damage to the heads and disk.

Care must be taken to avoid contaminants entering the disk cartridge and to prevent a bent disk from mishandling. To achieve maximum use of a magnetic disk, it is necessary to become familiar with the proper methods of handling and operation. The life of the cartridge and disk can be extended indefinitely by observing the following procedures:

- a. Replace cracked, chipped, or defective cartridges.
- b. Clean the cartridge periodically to remove dust and lint from the exterior of the housing, using a soft, lint-free cloth dampened with 91 percent isopropyl alcohol/9 percent water.

CAUTION

Do not use medicinal isopropyl alcohols from a drug store. They often contain additives harmful to the disk cartridge and disk drive.

- c. A disk suspected of being damaged should be removed from operation until it can be inspected.
- d. Keep all foods, beverages, and objects off the drive and away from the disk cartridge. Any of these items can cause permanent damage to either disk or the disk drive, or both.
- e. If a cartridge has been dropped or is visibly damaged, do not put it into operation.

- f. When a cartridge is not in use and the drive is inoperable, remove the cartridge and ensure that dust and contaminants do not enter it.
- g. Store cartridges in an environment of 50° to 100°F with a relative humidity of 10 to 80 percent.
- h. Do not store disk cartridges close to magnetic fields. A flux field greater than 50 gauss at the cartridge will destroy data previously recorded.
- i. Use a storage cabinet made of fire-resistant material with a metal door. The cabinet should be kept clean and free of dirt and other contaminants.

CAUTION

Improper handling of the disk cartridges will not only cause disk damage but can cause extensive damage to the disk drive.

3.2 ACCLIMATIZATION

The disks are made of precisely machined aluminum with a magnetic oxide coating. They will expand and contract with significant changes in temperature. If the ambient temperature at the point-of-use is less than 50°F or more than 104°F, the disk must be conditioned to the point-of-use temperature for a minimum of two hours before mounting it on the drive. This prevents loss of data from a shift in track location.

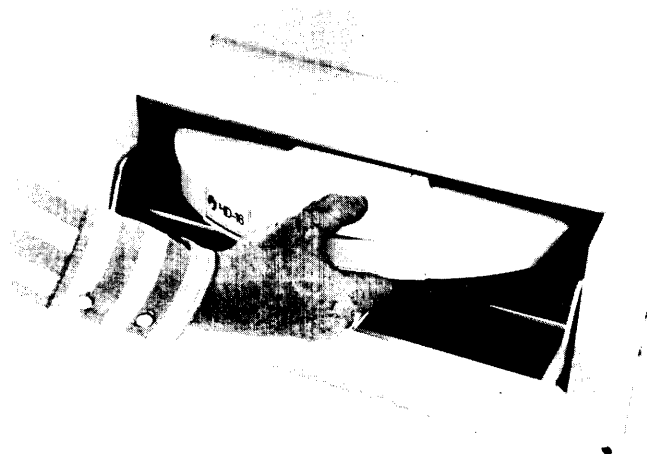
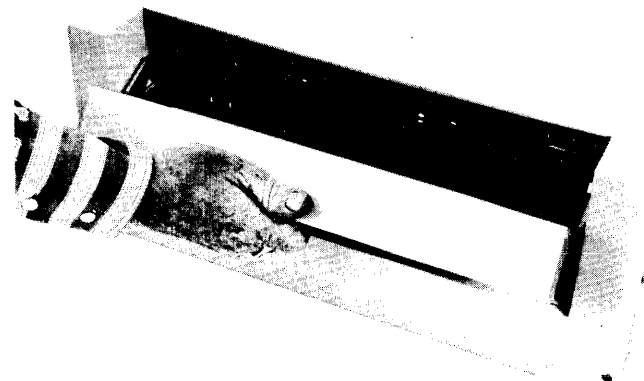
CAUTION

Disk cartridges must be acclimatized to room temperature for a minimum of two hours before being placed on the disk drive to prevent drive damage.

3.3 DISK CARTRIDGE LOADING AND SAFETY INTERLOCKS

- 3.3.1 The CMI cartridge utilized as the removable media in the Model 206 Series Disk Drives is loaded into the drive by pulling the cartridge receiver handle on the front of the drive down and inserting the cartridge into the mouth of the receiver. (See Figure 3-1.) Be certain that the cartridge is pushed all the way into the receiver, fully opening the head access door. Raise the receiver handle to the upright position, closing the door and seating the cartridge on the spindle. (An exploded view of the CMI cartridge is shown in Figure 3-2.)

PULL DOWN THE CARTRIDGE RECEIVER HANDLE, EXPOSING THE RECEIVER CAVITY IN THE LOADING POSITION.



INSERT THE CMI CARTRIDGE INTO THE RECEIVER, MAKING SURE THAT IT IS PUSHED IN ALL THE WAY, OPENING THE HEAD ACCESS DOOR.

RAISE THE RECEIVER HANDLE BACK TO THE CLOSED POSITION, SEATING THE CARTRIDGE ON THE SPINDLE.

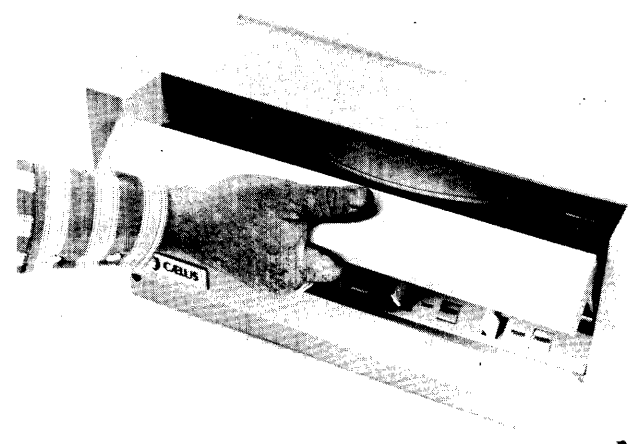


Figure 3-1. CMI Cartridge Loading Sequence

200-20

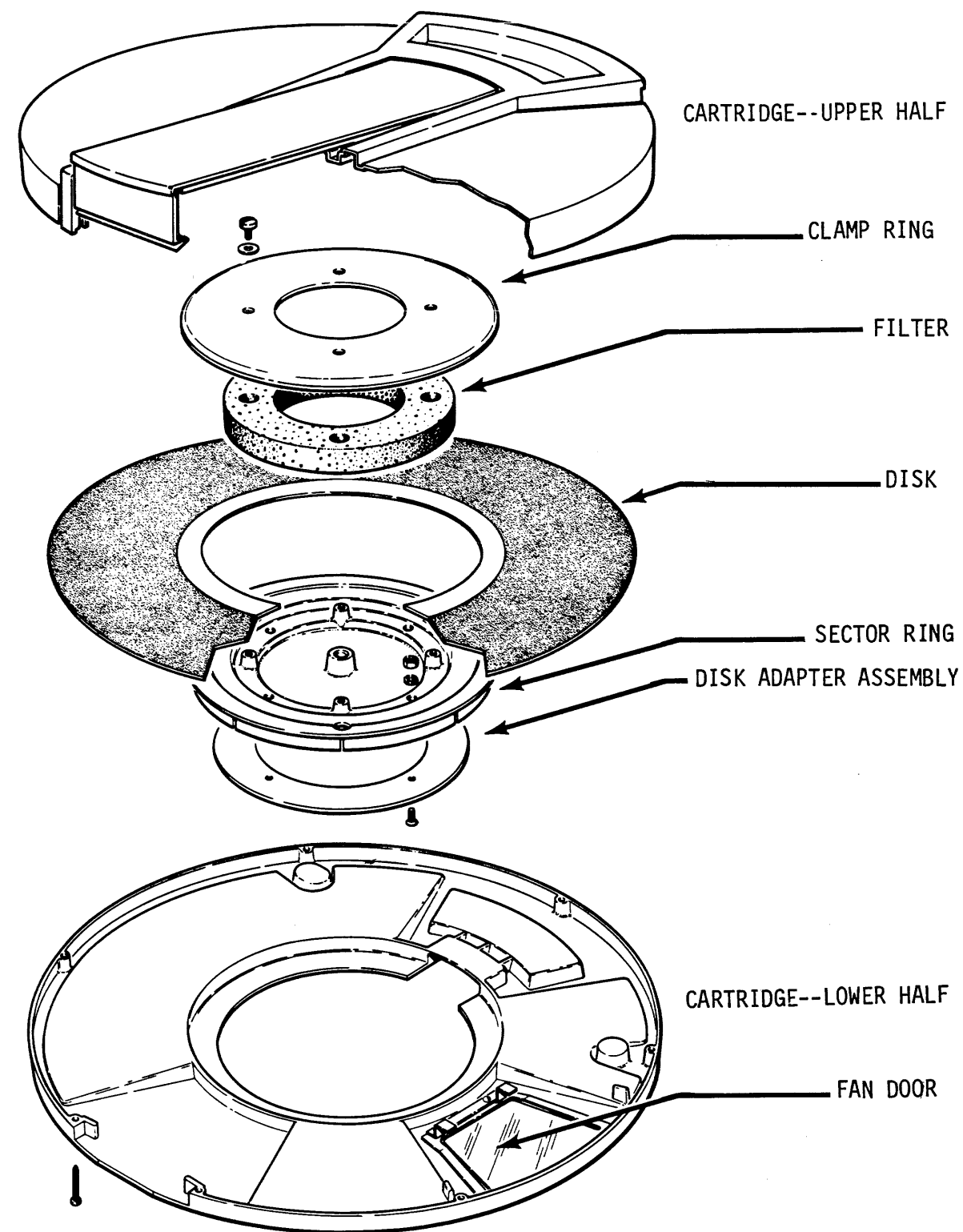


Figure 3-2. CMI Cartridge, Exploded View

200-21

- 3.3.2 The start/stop switch can now be placed in the start position. This turns off the stop light, locks the receiver handle, and starts disk rotation. Typically, from 15 seconds to six minutes later the heads will position to cylinder 000 and the ready light will come on.
- 3.3.3 Upon stopping the drive, there is a 10-second delay to allow the disk to stop. At the end of that time, the stop light will come on if the heads are fully retracted. When this condition is met, the receiver handle will unlock, permitting the operator to open the loading door and remove the cartridge. If the power is removed from the drive or the power switch is turned off while the receiver handle is closed, the door will remain locked, preventing cartridge removal.
- 3.3.4 The cartridge is removed by simply lowering the receiver handle and pulling the cartridge out. It is desirable to keep the receiver closed whenever a cartridge is not loaded, helping to eliminate contamination.

3.4 CARTRIDGE LOADING SEQUENCE

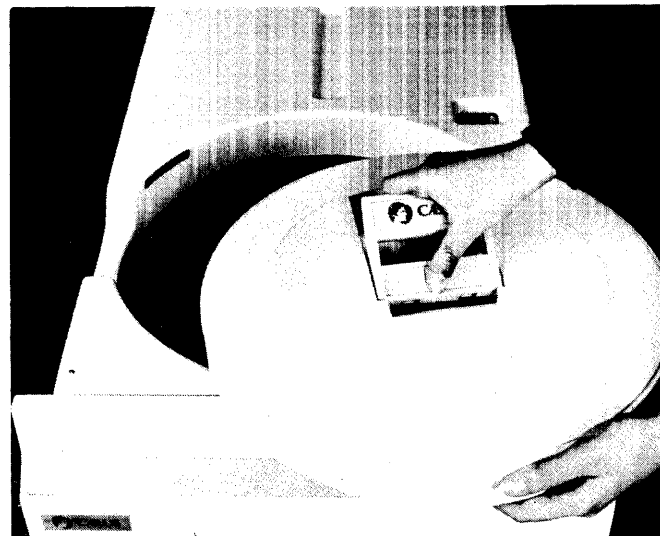
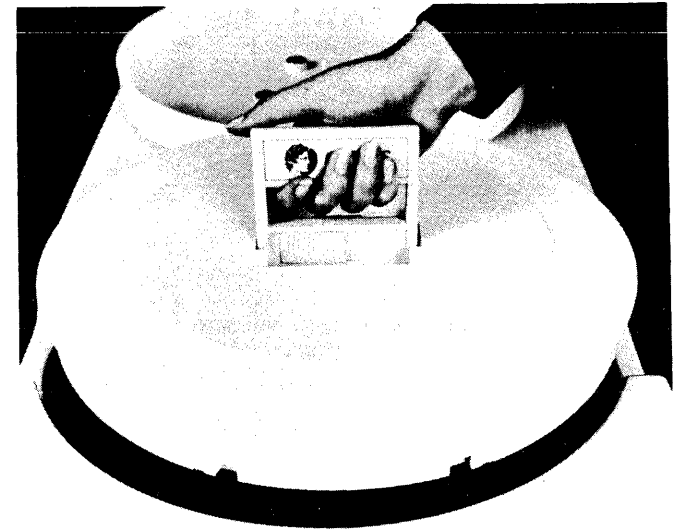
Be sure that drive power is On, the Start/Stop switch is in Stop position and the Stop indicator is lit. This will allow the cartridge latch arms to be unlocked and retracted. (Refer to Figure 3-2 for cartridge loading procedures.)

CAUTION

Do not set cartridge on the rear part of the drive cover as magnetism from the Positioner Motor may degrade data on the disk.

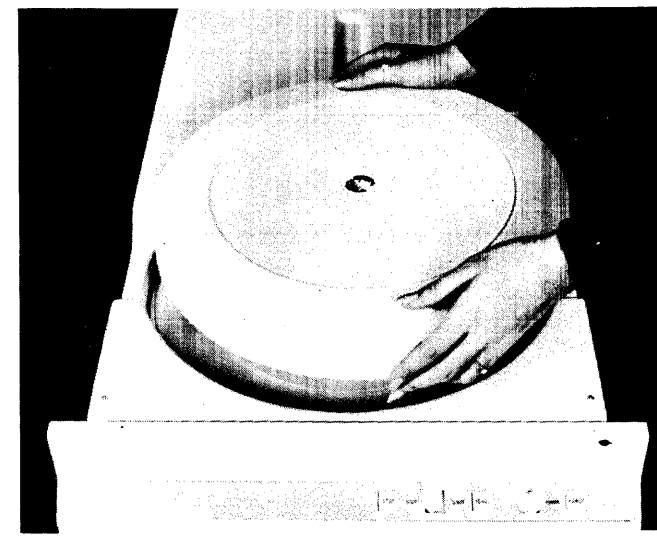
WITH THE CAELUS LOGO ON THE CARRYING HANDLE FACING TOWARD THE FRONT OF THE DRIVE, LOWER THE CARTRIDGE ONTO THE DRIVE SPINDLE.

ONCE THE CARTRIDGE IS SET FIRMLY IN PLACE, LOWER THE CARRYING HANDLE, ALLOWING THE CARTRIDGE HUB TO MAKE CONTACT WITH THE SPINDLE MAGNET.



SLIDE RELEASE BUTTON TO THE UNLOCKED POSITION TO RELEASE BOTTOM COVER.

LIFT CARRYING HANDLE TO THE UPRIGHT POSITION WHILE HOLDING THE RELEASE BUTTON IN THE UNLOCKED POSITION.

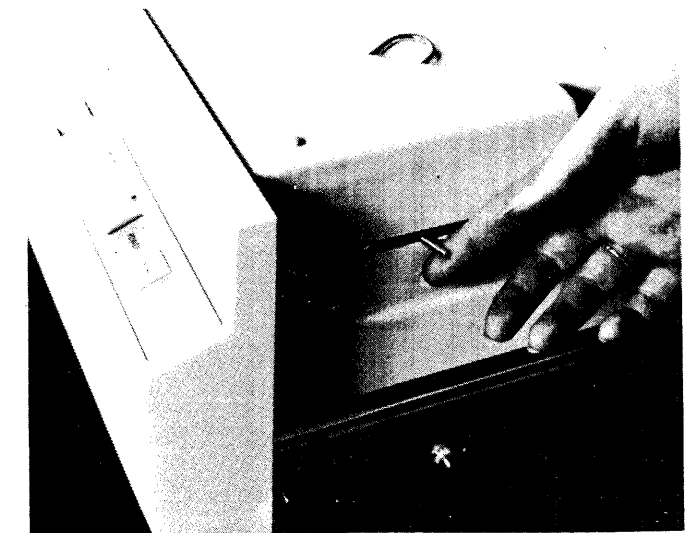


INVERT THE BOTTOM COVER AND PLACE IT EVENLY ON TOP OF THE INSTALLED CARTRIDGE.

LIFT CARTRIDGE CLEAR OF THE BOTTOM COVER WHILE HOLDING BOTTOM COVER SECURELY WITH THE LEFT HAND.



MOVE THE CARTRIDGE LATCH ARM INTO THE LOCKED POSITION, MOVING THE LOCKING ARMS OVER THE TOP OF THE CARTRIDGE, SECURING IT TO THE DRIVE.



600-31

Figure 3-3. Cartridge Loading Sequence.

3.5 CARTRIDGE REMOVAL SEQUENCE

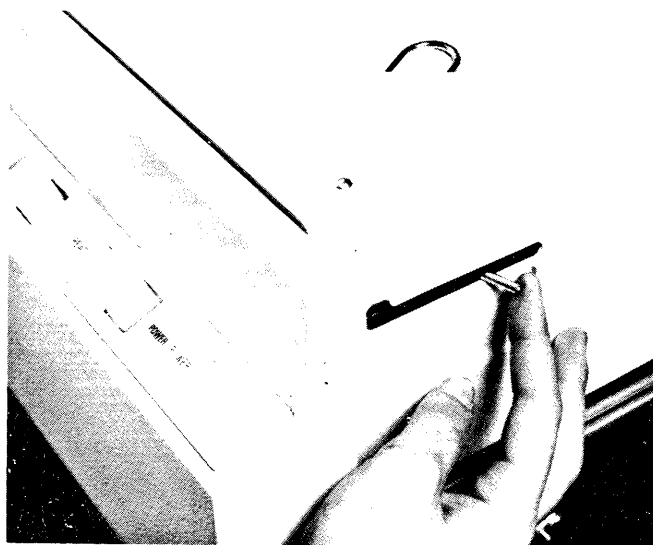
The drive Start/Stop switch must be turned to the Stop position. The disk takes nominally 10 seconds to stop spinning. During this time the cartridge latch solenoid is locked and the cartridge cannot be removed. (Refer to Figure 3-4 for cartridge removal procedures.)

CAUTION

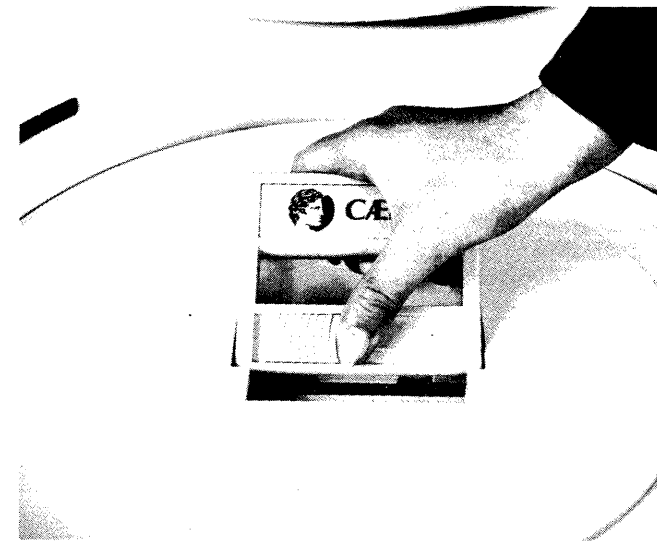
No attempt to remove the cartridge must be made until the Stop indicator comes on.

NOTE

A CMIII cartridge should be installed on the drive when it is not in use to protect the fixed disk from contamination.

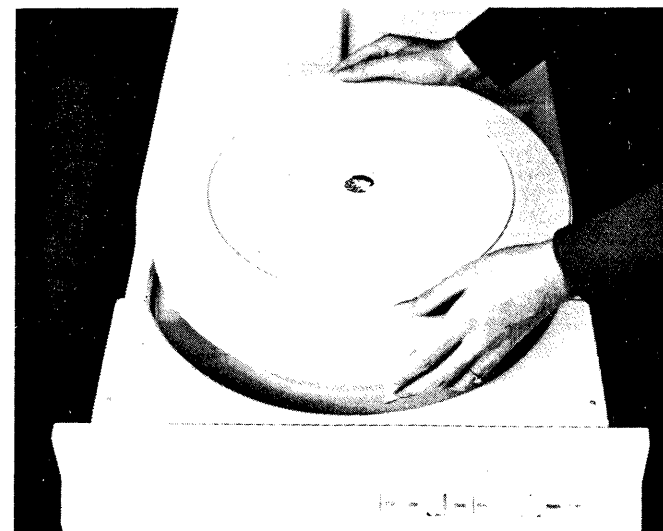


RETRACT THE LOCKING ARMS FROM OVER THE CARTRIDGE BY MOVING THE LATCH ARM TO THE FORWARD POSITION.



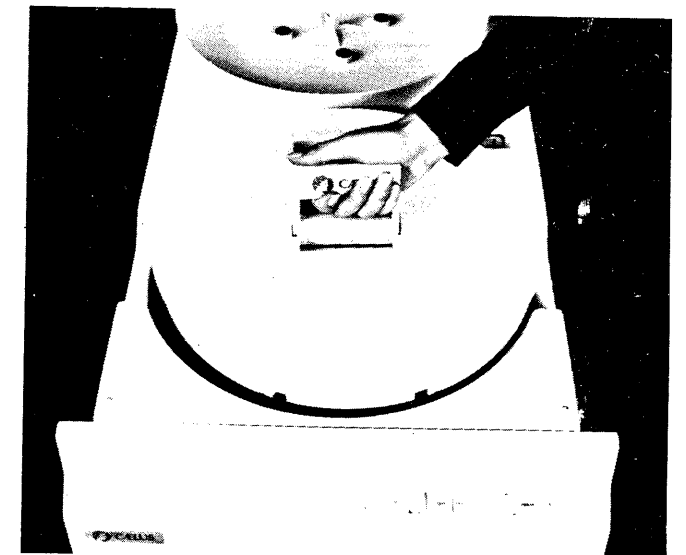
SLIDE THE RELEASE BUTTON TO THE UNLOCKED POSITION AND LIFT THE CARRYING HANDLE TO THE UPRIGHT POSITION WHILE HOLDING THE BUTTON. THIS RELEASES THE CARTRIDGE FROM THE SPINDLE MAGNET.

REMOVE THE INVERTED BOTTOM COVER, EXPOSING THE CARTRIDGE.



LIFT THE CARTRIDGE CLEAR OF THE SPINDLE HOUSING AND REPLACE THE BOTTOM COVER ONTO THE CARTRIDGE TO PROTECT IT FROM CONTAMINATION.

LOWER THE CARRYING HANDLE INTO THE CARTRIDGE RECESS, LOCKING THE BOTTOM COVER. THE HANDLE MAY THEN BE RAISED AGAIN TO THE CARRYING POSITION.



600-32

Figure 3-4. Cartridge Removal Sequence

3.6 DISK DRIVE OPERATION

CAUTION

3.6.1 Starting the Drive

Upon completion of disk cartridge loading, the disk drive may be started as follows:

- a. Set the drive Start/Stop switch to the Start position.
- b. Observe that the Stop indicator goes out immediately after setting the Start/Stop switch to start.
- c. Observe that the Ready indicator turns on within 6 minutes (maximum) after setting the Start/Stop switch to Start.
- d. Illumination of the Ready indicator indicates that the disk drive is ready to accept interface commands.

3.6.2 Operation Online

Once the Ready indicator is lit, the drive is ready for online operations, under user control. During this time, the following comments apply.

DO NOT TURN either the Power switch to Off or the Start/Stop switch to Stop while the drive is accessing, to prevent inadvertent data loss, should the drive be in a write mode at the time.

DO NOT SLIDE the drive in or out of its enclosure, to prevent possible jarring of the heads during operation.

Flickering of the Ready and Power indicators is normal and indicates that the drive is accessing to a different cylinder location.

In the event of AC power failure, the heads will retract to the home position. Upon regaining power, a normal start cycle will be initiated automatically, and the heads will position to cylinder 000.

Write Inhibit switches are used by the operator to prevent data from being written on the fixed and/or removable disks. The switch settings should be changed during online operation.

3.6.3 Stopping the Drive

Perform the following procedure to stop the disk drive:

- a. Set the Start/Stop switch to the Stop position.
- b. Observe that the Stop indicator turns on about 10 seconds after setting the Start/Stop switch to Stop. This indicates that the disk has stopped spinning and the cartridge may be removed.

3.7 OPERATOR MAINTENANCE

The only operator maintenance required is to ensure that the receiver cavity, in which the disk cartridge rests, is kept clean of all contaminants. The receiver cavity and disk cartridge should be wiped clean frequently to prevent contaminants entering the disk cartridge or fixed disk (under the receiver cavity).

3.8 OPERATOR TROUBLESHOOTING GUIDE

	<u>Symptom</u>	<u>Possible Cause</u>	<u>Remedy</u>
1.	Power Indicator does not light.	Burned out bulb or fuse. Power cord unplugged. Main system power off.	Call Field Service Personnel.
2.	Latch does not operate after 30 seconds/light inoperative.	Circuit problem.	Call Field Service Personnel. <u>DO NOT</u> force latch.
3.	Motor does not turn when Start/Stop switch turned on.	Cartridge improperly seated. Cover left off. Motor overheated.	Reseat cartridge. Install cartridge cover. Allow a few minutes to cool down. If problem reoccurs, call Field Service Personnel.

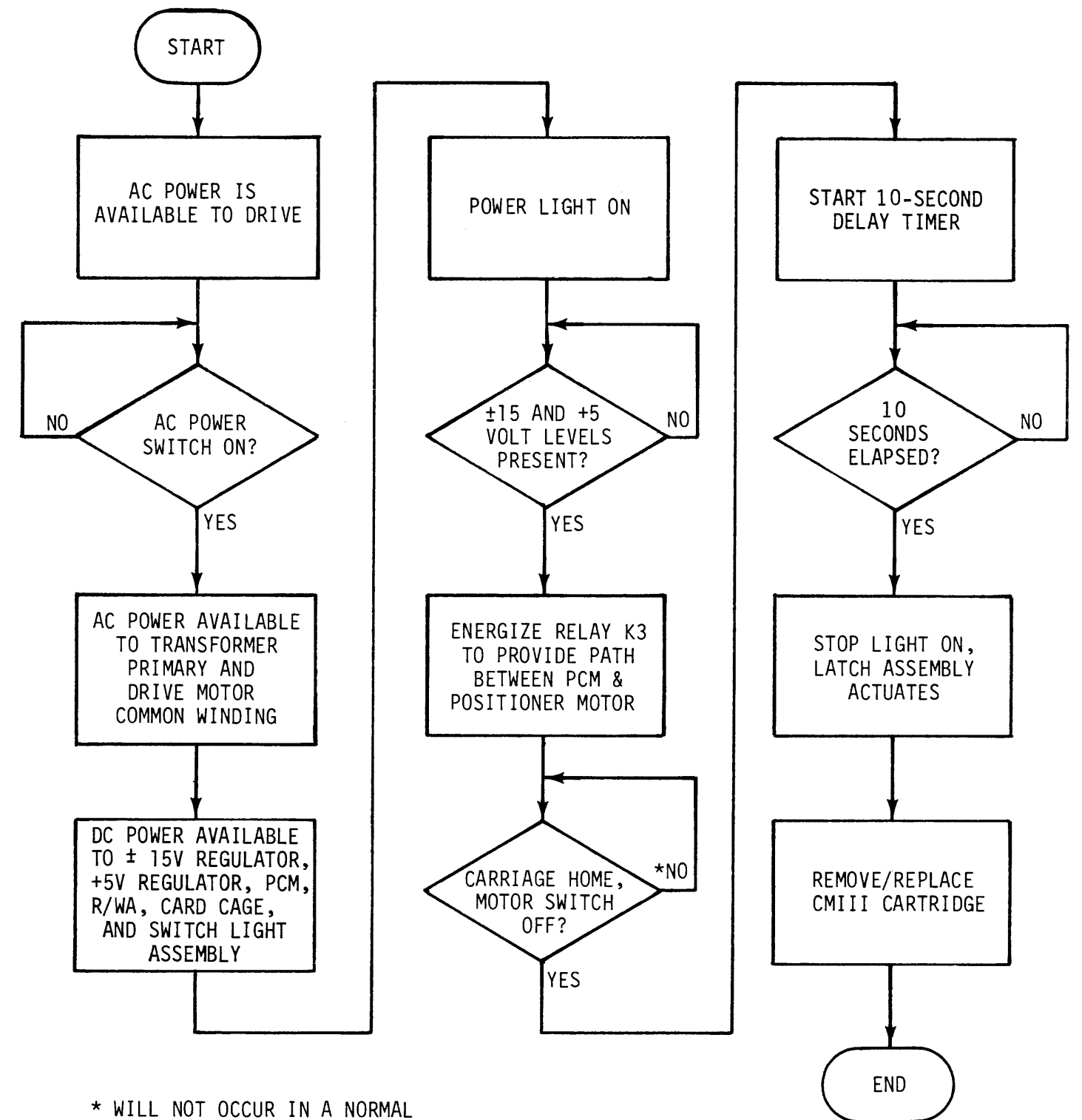
<u>Symptom</u>	<u>Possible Cause</u>	<u>Remedy</u>
4. Heads do not load, no ready light.	Shipping hardware installed. Termination board not installed (on drives that require one).	Call Field Service Personnel. Install Terminator board.
5. Heads retract during accessing operations.	Overcurrent sensing.	Turn Power switch off for one second; if symptom reoccurs, call Field Service Personnel.

SECTION 4
OPERATIONAL FLOW CHARTS

4.1 GENERAL

This subsection contains flow charts for Models 206 and 306 Disk Drive operations listed below. See Figures 4-1 through 4-6.

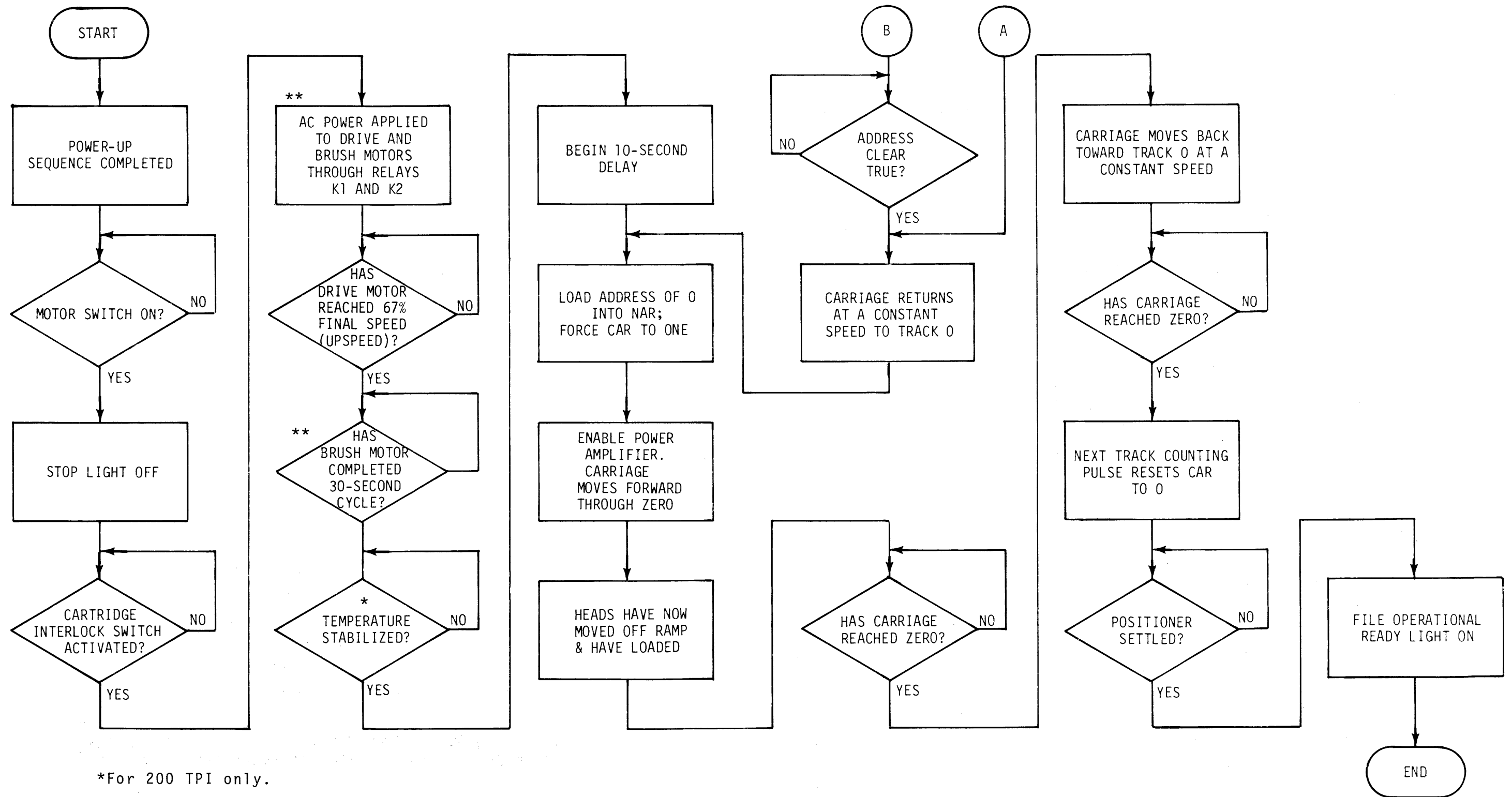
- a. Power Up/Install Cartridge
- b. Run/First Seek
- c. Programmed Seek
- d. Write Mode
- e. Read Mode
- f. Stop



* WILL NOT OCCUR IN A NORMAL POWER-UP SEQUENCE

600-33

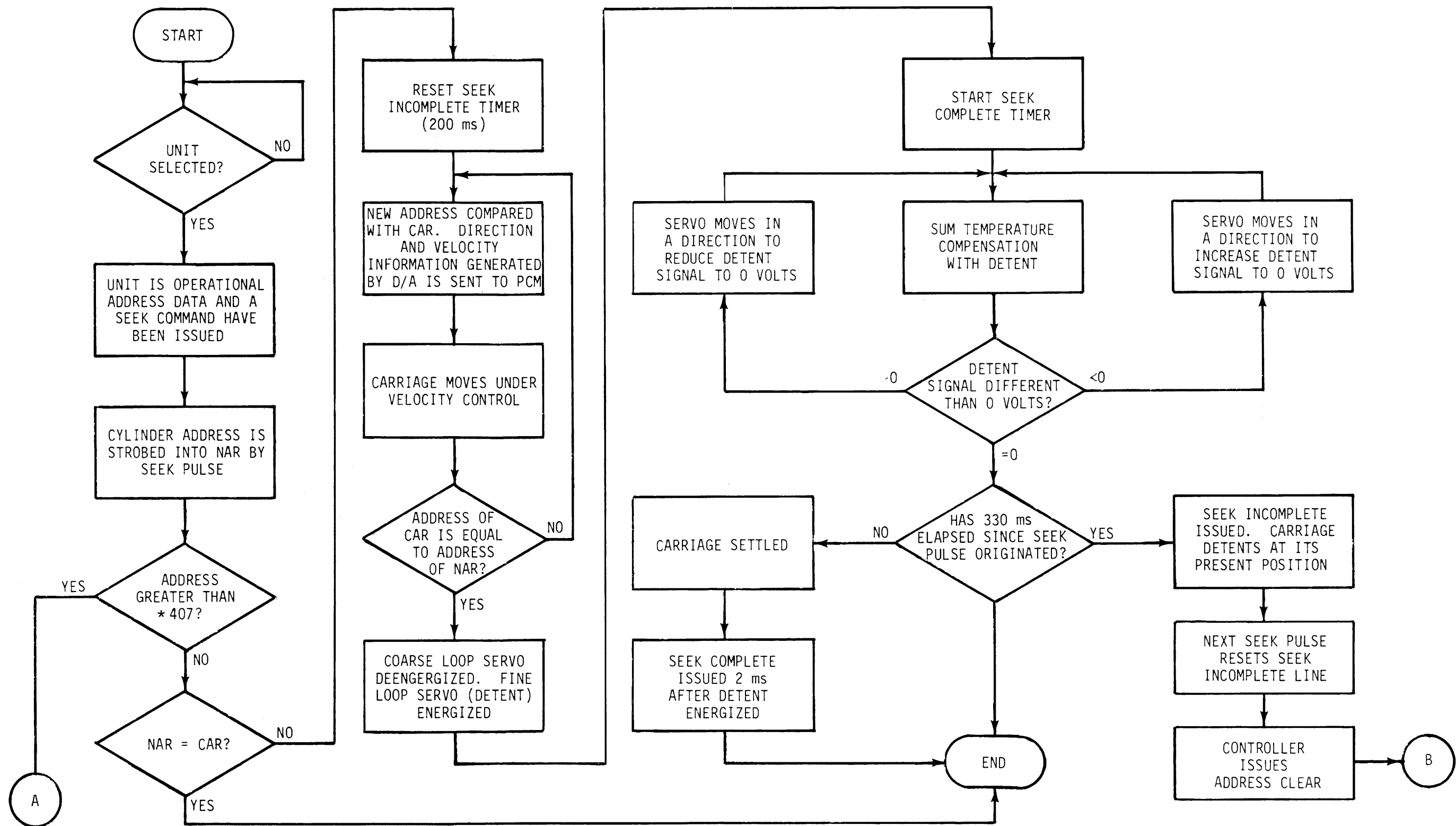
Figure 4-1. Operational Flow Chart, Power Up/Install Cartridge



*For 200 TPI only.

**Brush Motor is not available on front load models. See Interconnection Diagram.

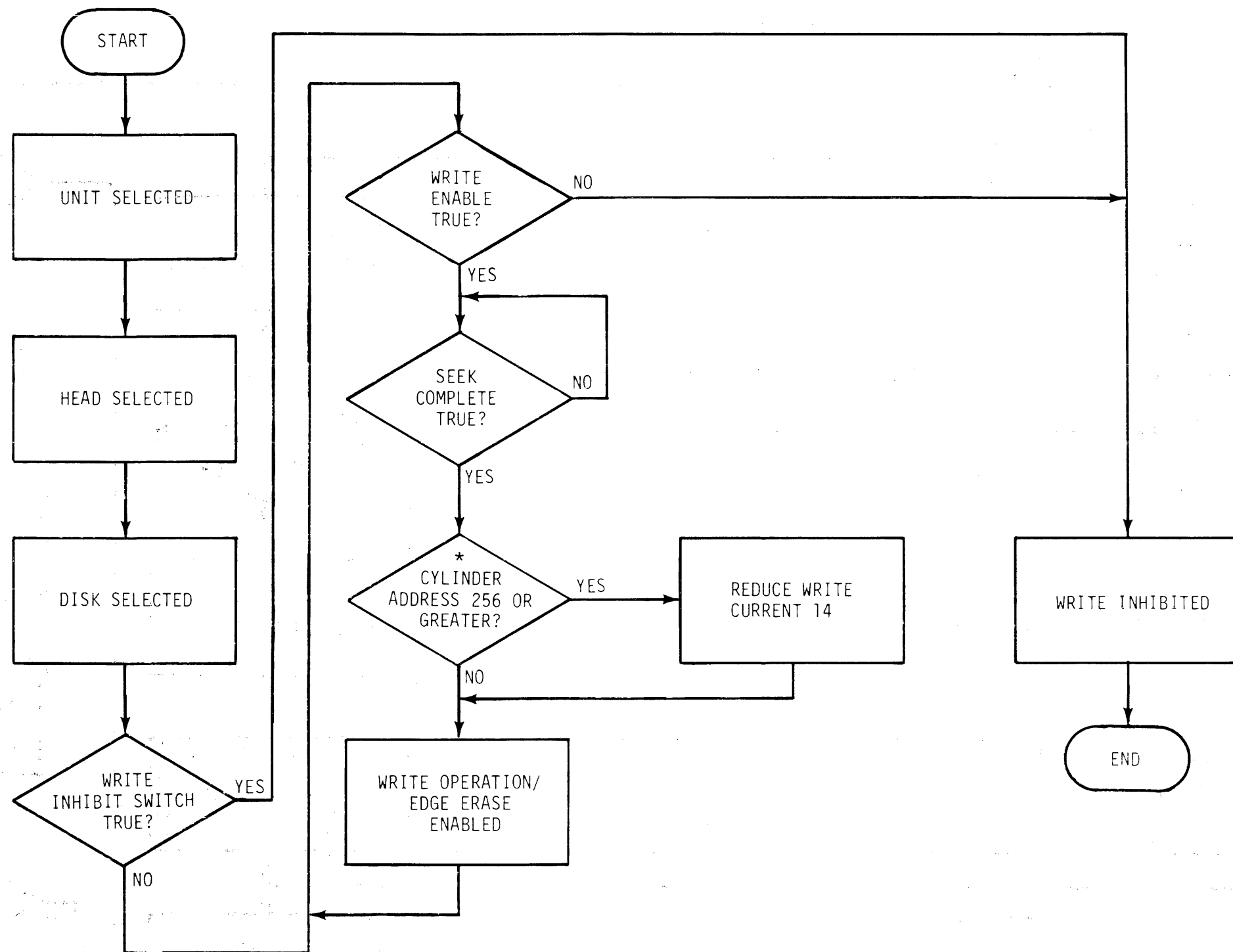
Figure 4-2. Operational Flow Chart, Run/First Seek



600-36

*203 for 100 TPI drives.

Figure 4-3. Operational Flow Chart, Programmed Seek



*128 for 100 TPI drawings

Figure 4-4. Operational Flow Chart, Write Mode

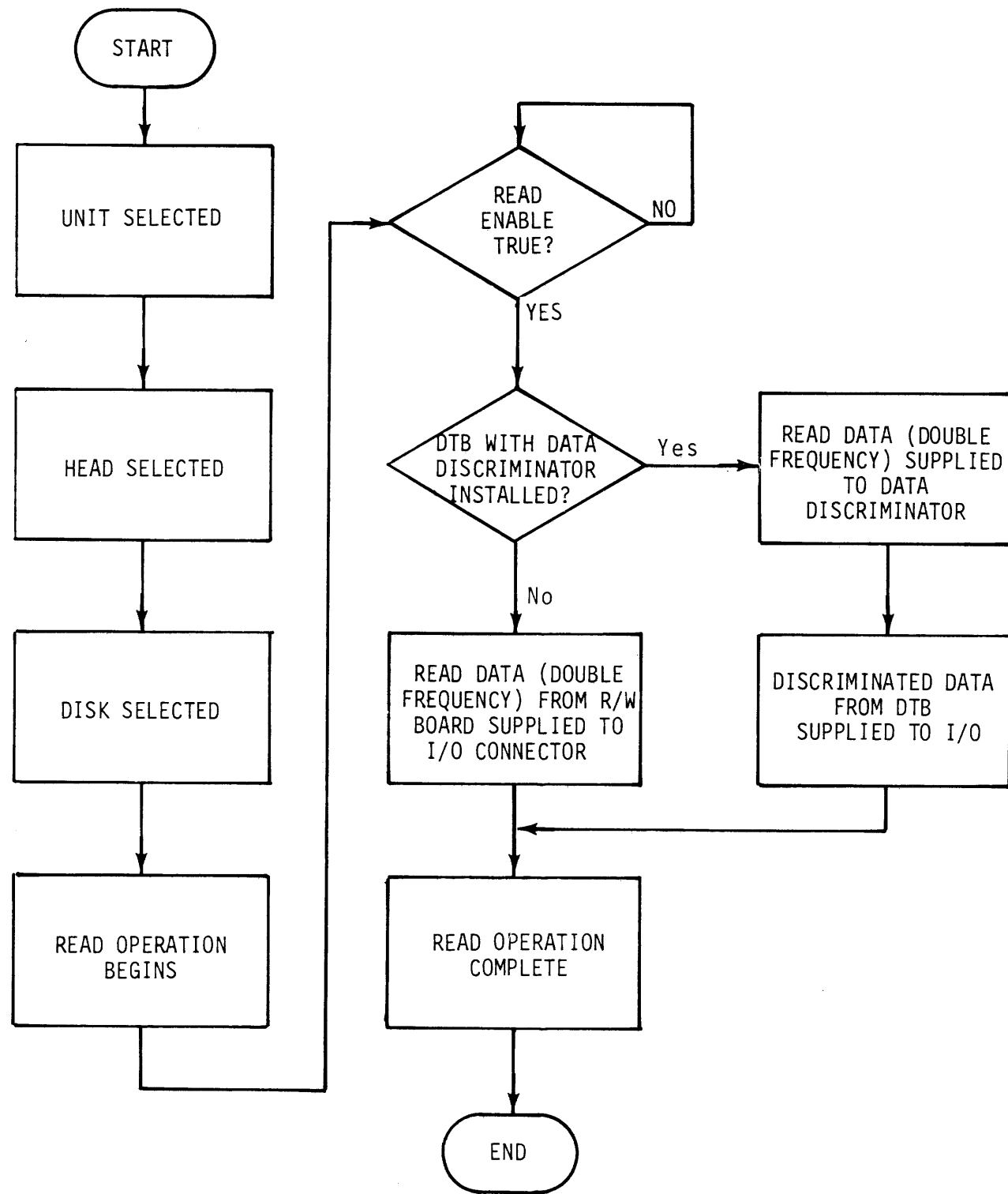


Figure 4-5. Operational Flow Chart, Read Mode

600-38

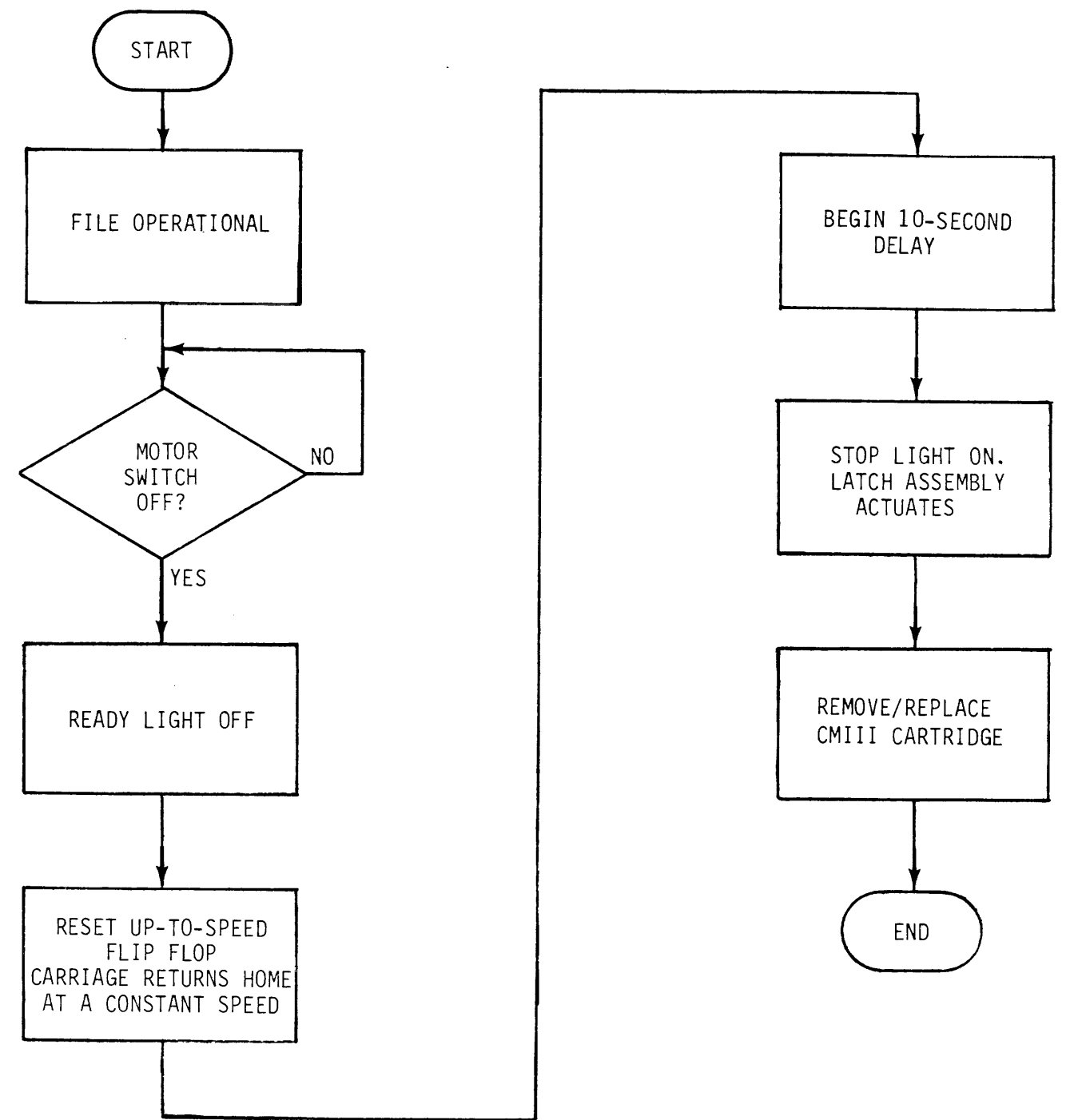


Figure 4-6. Operational Flow Chart, Stop

600-39

SECTION 5
CIRCUIT OPERATION

5.1 GENERAL

The electronic circuits of the Disk Cartridge Drives have been designed for high reliability and ease of maintenance. The circuit cards have test points located at strategic electrical locations within the circuits providing a rapid point-to-point signal tracing technique which isolates a malfunction to a particular circuit card.

5.2 LOGIC SYMBOLS

The logic symbols used in this subsection are illustrated in Figure 5-1.

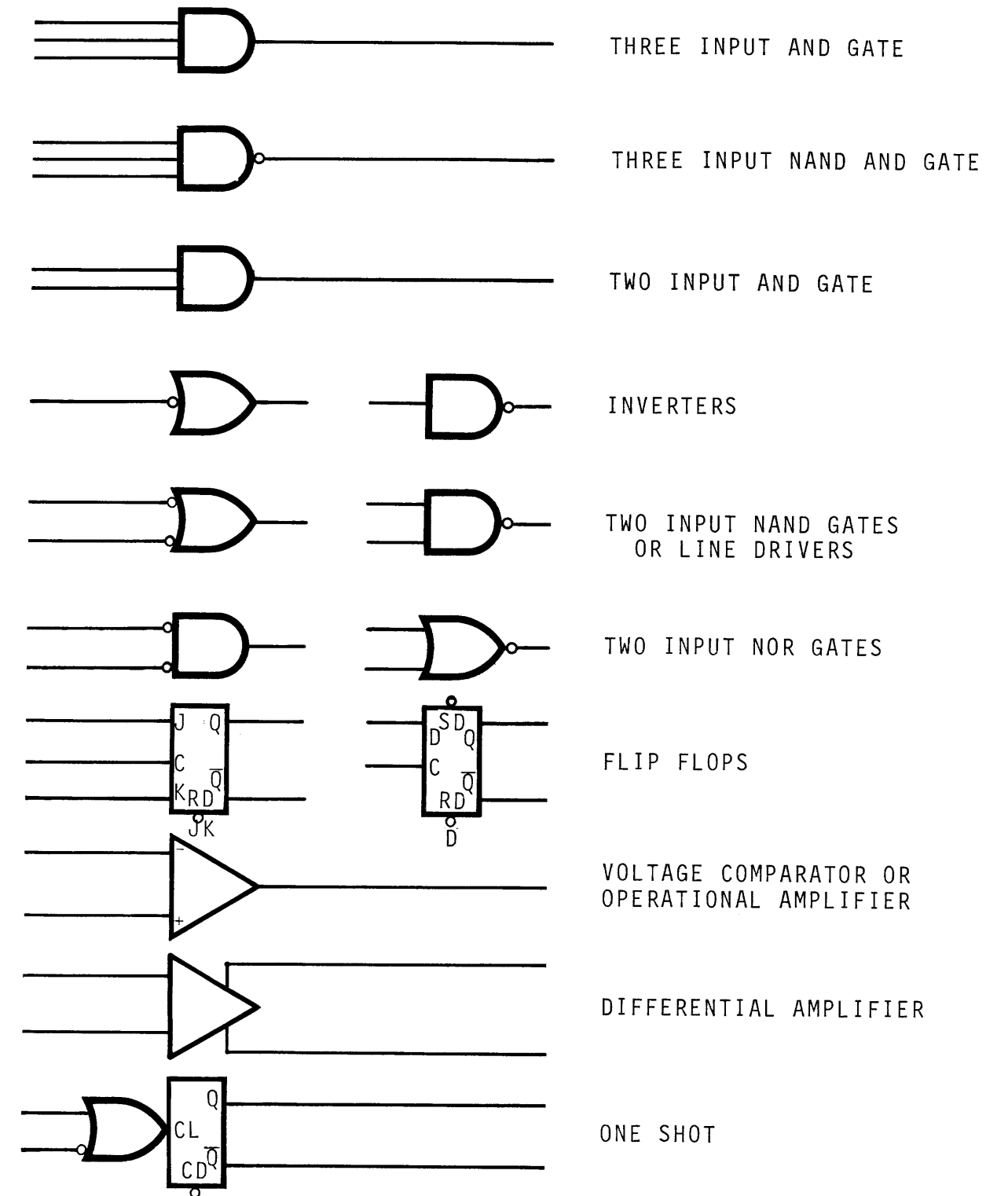


Figure 5-1. Logic Symbols

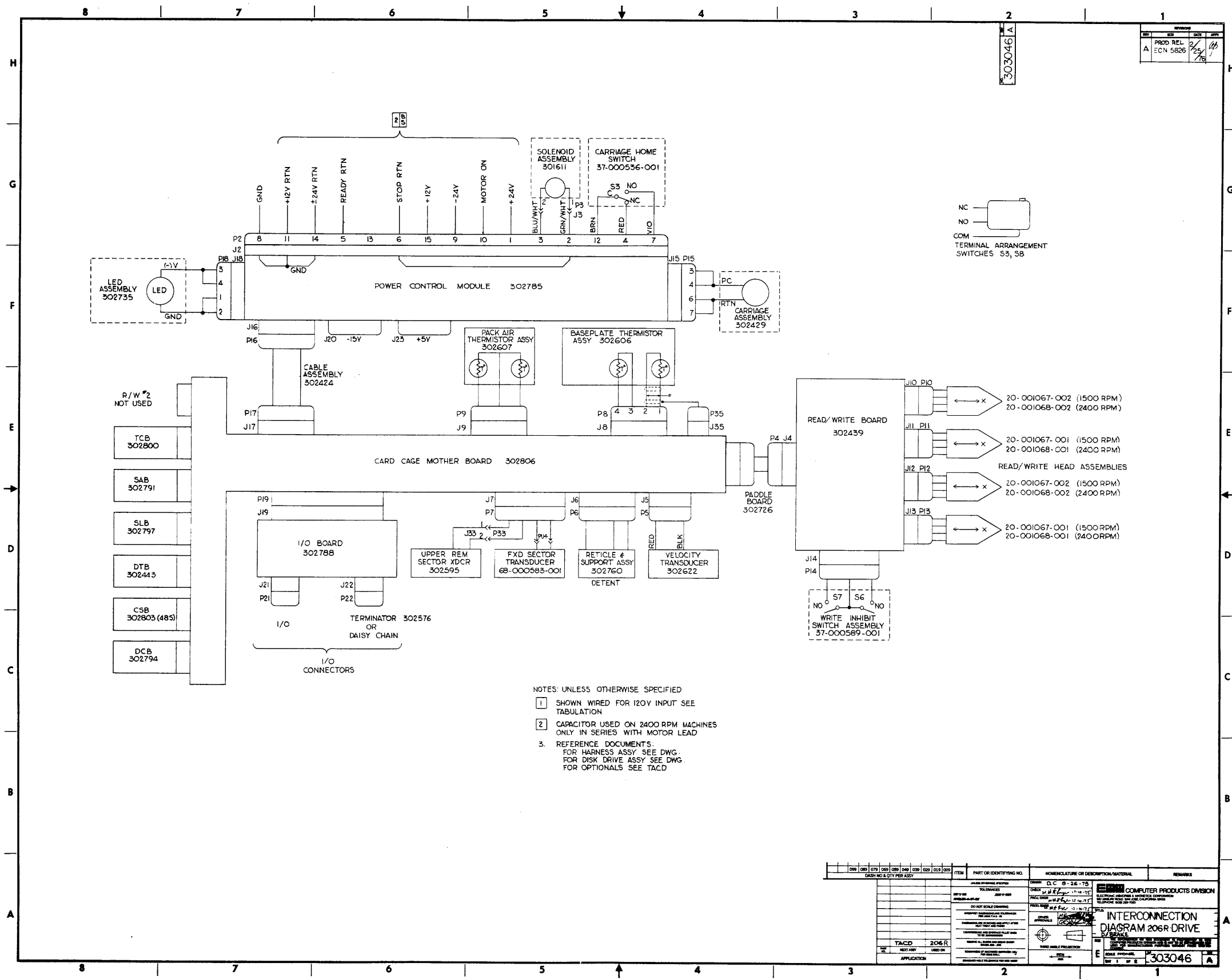
5.3 CIRCUITRY

This subsection contains a functional description of the drive interconnection diagram, block diagram, and each circuit board schematic. The logic on each board is described as it is used in a particular sequence, rather than a simple description of logic physically located on the board.

5.3.1 206 Interconnection Diagram

a. Sheet 1 of 2

The interconnection diagram shows all cable connectors used in the drive assembly to interconnect PC boards and components. This drawing should be referred to any time a signal is being traced from one PC board to another on the drive in conjunction with the Mother Board schematic. (See Figure 5-2).



REV	DATE	BY	CHKD	APP'D	DESCRIPTION
A	2/25/78				PROD REL. ECN 5826

ITEM	PART OR IDENTIFYING NO.	QUANTITY	DESCRIPTION
1	302785	1	POWER CONTROL MODULE
2	302806	1	CARD CAGE MOTHER BOARD
3	302788	1	I/O BOARD
4	302439	1	READ/WRITE BOARD
5	302735	1	LED ASSEMBLY
6	302429	1	CARRIAGE ASSEMBLY
7	302607	1	PACK AIR THERMISTOR ASSY
8	302606	1	BASEPLATE THERMISTOR ASSY
9	302595	1	UPPER REM SECTOR XDCR
10	68-000583-001	1	FIXD SECTOR TRANSDUCER
11	302760	1	RETICLE # SUPPORT ASSY
12	302622	1	VELOCITY TRANSDUCER
13	302576	1	TERMINATOR OR DAISY CHAIN
14	37-000589-001	1	WRITE INHIBIT SWITCH ASSEMBLY

Figure 5-2. 206 Interconnection Diagram, Sheet 1 of 2

b. Interconnection Diagram, Sheet 2 of 2

The incoming AC power RFI filtered in the relay module is shown on sheet 2 of the Interconnection Diagram. (See Figure 5-3). The components contained in the relay module are identified in the diagram by a heavy dark line. These components consist of the RFI filter, the main line fuse, motor start relay K2, and diode rectifiers CR1 and CR2. The filtered AC power is then applied through the connector J1-2 to the drive Power Switch, S1 (pin 2), and finally to the primary of transformer T1.

+24 volts to the PCM on P2-1 and -24 volts to P2-9. These voltages are used on the PCM to develop regulated +15, -15 and +5 volts.

5.3.1.1 Transformer Interconnection

A transformer connection chart shown in the bottom right-hand corner of the diagram indicates the various connections which may be applied to the transformer. The transformer is shown wired for 120-volt input. The voltages applied to T1 (100, 120, 200, 220, or 230/240 volts) determine how the transformer must be jumpered. Jumpering is identified on the drive by the center three digits of the serial number as shown in the tabulation below. The output of T1 at pin 3 will be 120 volts which is used by the drive spindle motor.

5.3.1.4 Dynamic Brake

The motor switch, when turned to the OFF position, activates the Dynamic Brake assembly at zone D4. The Dynamic Brake assembly is turned on for 12 seconds whenever the motor switch is turned off due to the action of the stop signal on P2 pin 6. This stop signal turns Q1 on which supplies a ground to one side of the motor (M1). The other side of the motor is supplied with +24 volts D.C. through S2 pin 3. When the stop timer runs out Q1 is disabled and current flow removed from the motor.

<u>Serial Number</u>	<u>Voltage</u>
-009	120
-019	100
-029	200
-039	220
-049	230/240

5.3.1.2 Spindle Motor

The 120 volts from T1, pin 6 is applied to the spindle motor start switch, S2. When S2 is energized, power is switched to the pack interlock switch, S8. When S8 is open, 120 volts are applied to the motor start relay K2. K2 supplies 120 volts to the start winding (red) of the drive motor (M1) for approximately 2 seconds, and 120 volts to the sustaining lead (blue). Return for the motor current is on pin 4 of the transformer T1.

5.3.1.3 Power Control Module

The diode bridges CR1 and CR2 receive their voltages from the secondary of transformer T1. CR1 provides a rectified +12 volts to the Power Control Module (PCM) at P2-15. CR2 provides

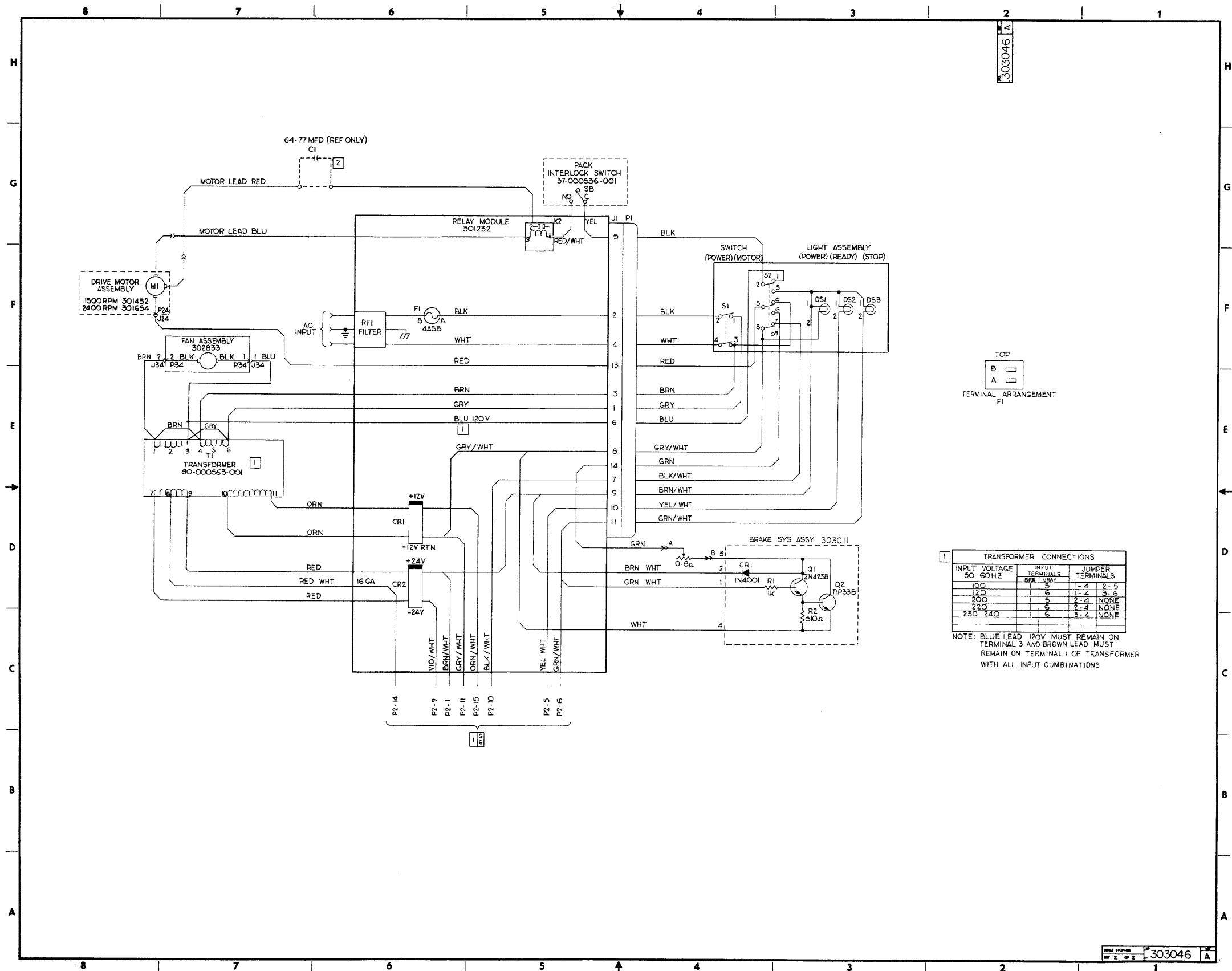


Figure 5-3. 206 Interconnection Diagram, Sheet 2 of 2

5.3.2 306 Interconnection Diagram

a. Sheet 1 of 2

The interconnection diagram shows all cable connectors used in the drive assembly to interconnect PC boards and components. This drawing should be referred to any time a signal is being traced from one PC board to another on the drive in conjunction with the Mother Board schematic. (See Figure 5-4).

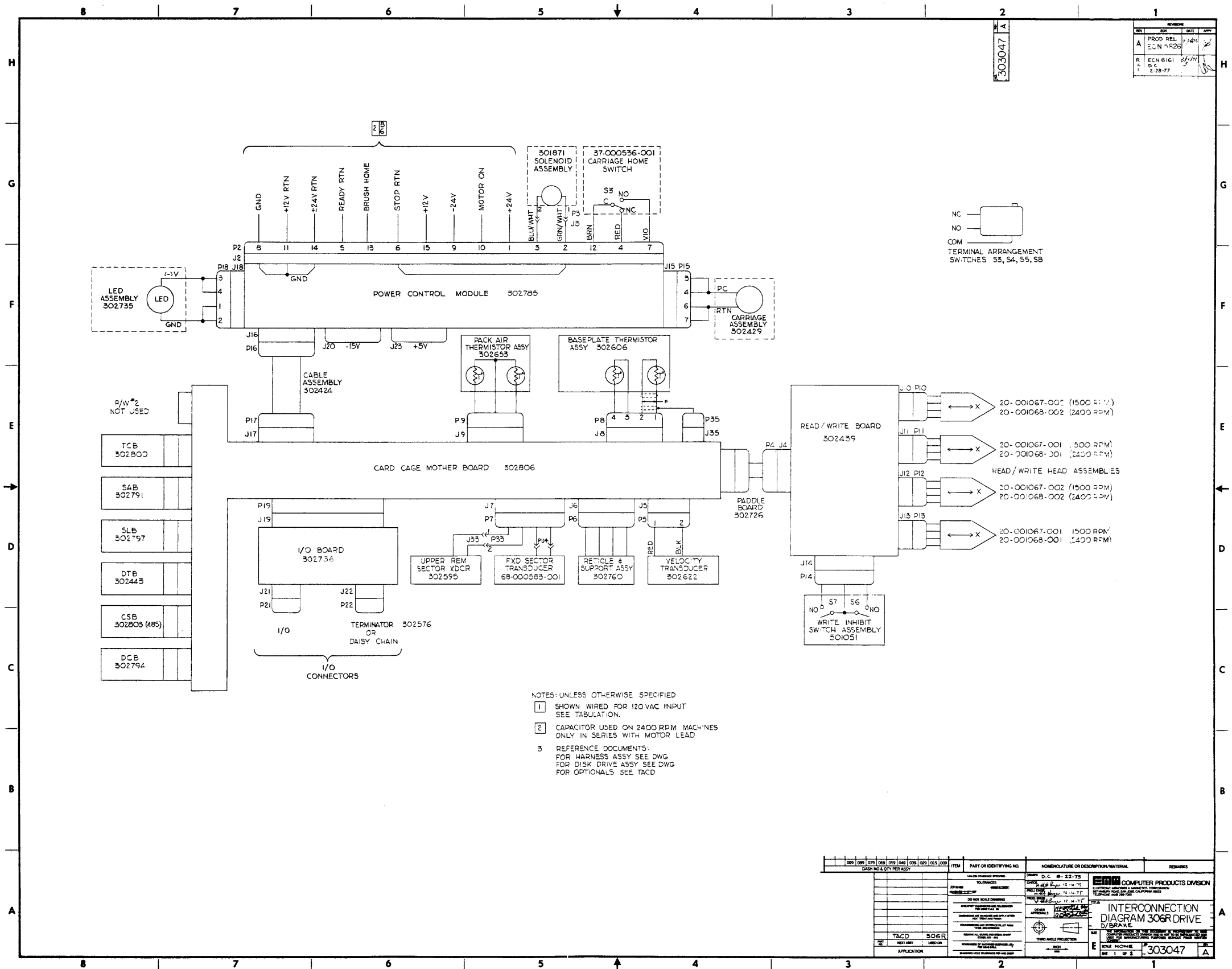


Figure 5-4. 306 Interconnection Diagram, Sheet 1 of 2

b. Interconnection Diagram, Sheet 2 of 2

The incoming AC power RFI filtered in the relay module is shown on sheet 2 of the Interconnection Diagram. (See Figure 5-5). The components contained in the relay module are identified in the diagram by a heavy dark line. These components consist of the RFI filter, the main line fuse, motor start relays K1 and K2, and diode rectifiers CR1 and CR2. The filtered AC power is then applied through the connector J1-2 to the drive Power switch, S1 (pin 2), and finally to the primary of transformer T1.

5.3.2.1 Transformer Interconnection

A transformer connection chart shown in the bottom right-hand corner of the diagram indicates the various connections which may be applied to the transformer. The transformer is shown wired for 120-volt input. The voltages applied to T1 (100, 120, 200, 220, or 230/240 volts) determine how the transformer must be jumpered. Jumpering is identified on the drive by the center three digits of the serial number as shown in the tabulation below. The output of T1 at pin 3 will be 120 volts which is used by the drive spindle motor.

<u>Serial Number</u>	<u>Voltage</u>
-009	120
-019	100
-029	200
-039	220
-049	230/240

5.3.2.2 Spindle Motor

The 120 volts from T1, pin 3 are applied to the spindle motor start switch, S2. When S2 is energized, power is switched to the pack interlock switches, S8 and S9. When S9 is open and S8 is closed, 120 volts are applied to the motor start relay K2. K2 supplies 120 volts to the start winding (red) of the drive motor (M1) for approximately 2 seconds, and 120 volts to the the brush motor relay K1.

5.3.2.3 K1 and K2

Motor start relays K1 and K2 have their (low impedance) coil between pins 3 and 4 and their contacts between pins 2 and 4. The contacts close as the coil current goes above 5 amps and open as the coil current drops below 4.25 amps. The heavy current surge in the motor run winding--which occurs at switch-on because the armature is not rotating--closes the relay contacts

of K2 and energizes the start winding. As the motor runs up to speed, the run winding current drops and the contacts open. This start-up cycle takes approximately 2 seconds from switch-on.

5.3.2.4 Brush Motor

The brush motor, M2, is controlled by start relay K1. The characteristics of K1 are identical to K2. When power is first applied to K1 pin 4, 120 volts are available on the output pin 2 for approximately 2 seconds. This voltage supplies the starting current to the brush motor, M2, whenever the Start/Stop switch has been turned on. Brush motor switch S5 is shown in Figure 5-5 in the normally closed position, which is the position of the switch while the brushes are sweeping the disk. S5 is normally open if the brushes are at home. Since the brushes are at home when the drive motor is first turned on, power is applied to the brush motor from the normally open contact of S5. The brush motor is now energized and the brushes start sweeping the disk. S5 switches to the normally closed contact and a new current path is enabled through the brush motor. This new path is from pin 3 of T1, through the brush motor to the normally closed contact of S5, and then returned to pin 4 of T1. When the brushes return home, S5 switches to normally open, and since there is no longer a voltage available from pin 2 of relay K1, the brush motor is deenergized and stops in this position.

5.3.2.5 Power Control Module

The diode bridges CR1 and CR2 receive their voltages from the secondary of transformer T1. CR1 provides a rectified +12 volts to the Power Control Module (PCM) at P2-15. CR2 provides +24 volts to the PCM on P2-1 and -24 volts to P2-9. These voltages are used on the PCM to develop regulated +15, -15, and +5 volts.

5.3.2.6 Dynamic Brake

The motor switch, when turned to the OFF position, activates the Dynamic Brake assembly at zone D4. The Dynamic Brake assembly is turned on for 12 seconds whenever the motor switch is turned off due to the action of the stop signal on P2 pin 6. This stop signal turns Q1 on which supplies a ground to one side of the motor (M1). The other side of the motor is supplied with +24 volts D.C. through S2 pin 3. When the stop timer runs out Q1 is disabled and current flow removed from the motor.

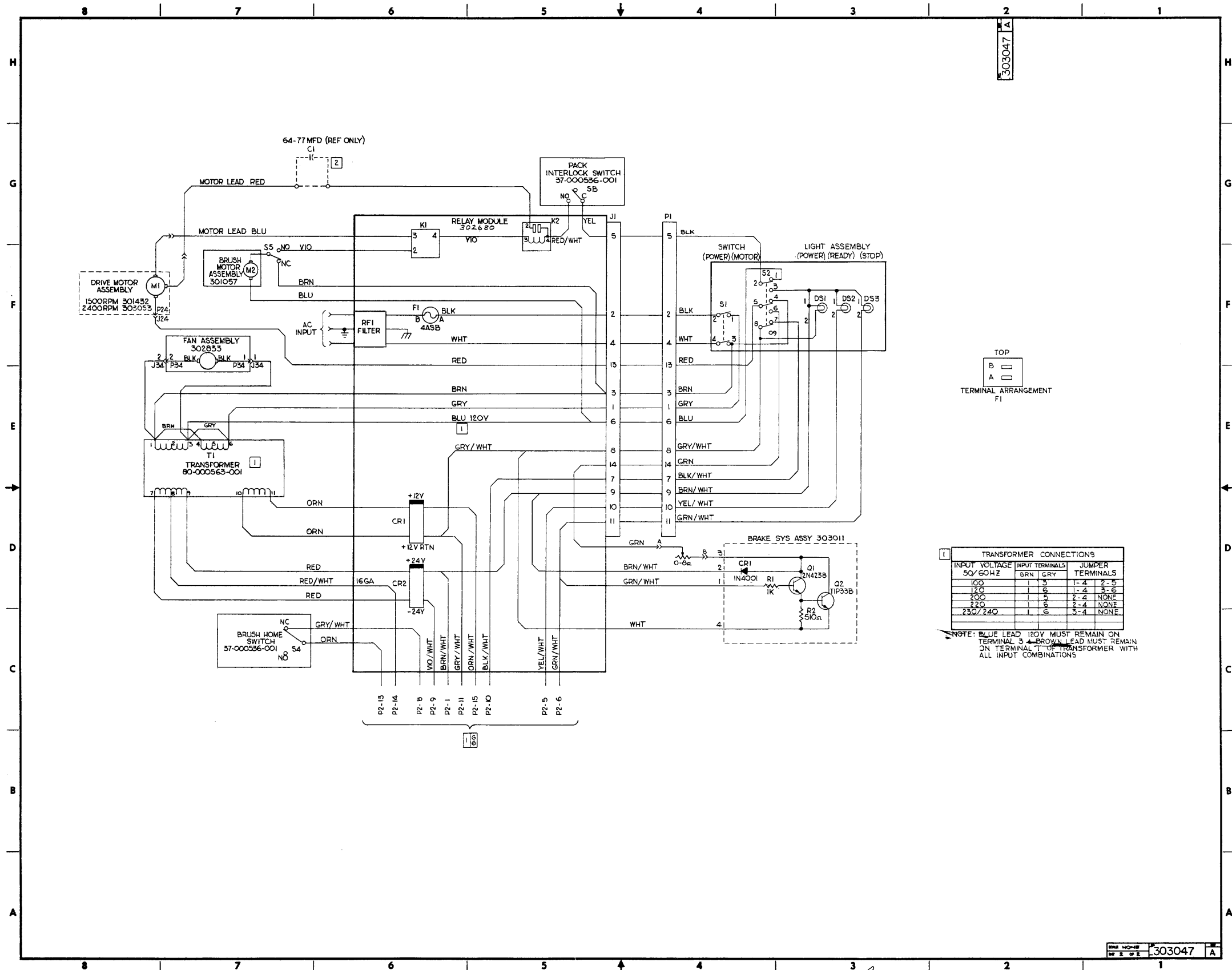


Figure 5-5. 306 Interconnection Diagram, Sheet 2 of 2

5.3.3 Mother Board

As shown in Figure 5-6, the Mother board is the principal means of interconnection for the drive. The Mother board contains connectors for the six logic cards contained in the card cage as well as connectors for the I/O board, PCM, Sector Transducers, Detent Assembly, Velocity Transducer, Thermistors, and Read/Write board. The Mother Board schematic is shown in Figure 5-6. This schematic should be referred to any time signal tracing is done from one logic board to another or from mechanical assembly to logic boards.

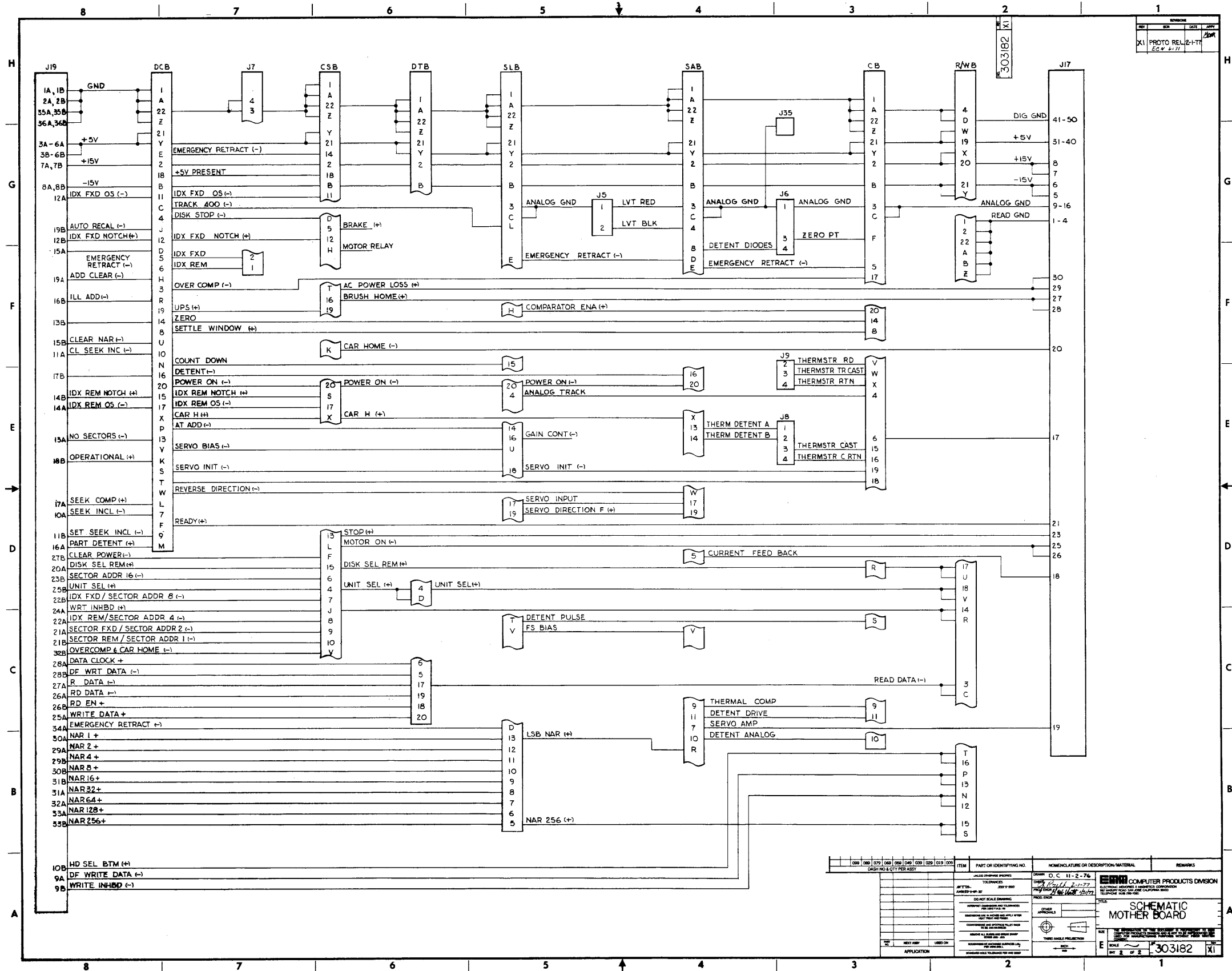


Figure 5-6. Mother Board Schematic

5.3.4 Functional Block Diagram

A block diagram of the drive is shown in Figure 5-7. Board name letters are shown on the blocks so that sections of the block diagram may be located on board schematic diagrams.

5.3.4.1 Carriage Position

The position of the carriage is maintained on the Servo Logic board. Carriage position is stored in complement form in the Cylinder Address Register (CAR). The Detent Assembly on J6 provides signals which are used to count the CAR up, or down, in relation to carriage movement. The CAR and the New Address Register (NAR) are summed on the SLB to develop a carriage drive voltage that is proportional to the distance the carriage is required to travel. The CAR counts down when the carriage moves to higher-numbered tracks. The Phase Detect circuits (on the SLB) determine whether the carriage is being driven toward higher-numbered tracks (count-down) or toward lower-numbered tracks (count-up).

5.3.4.2 New Address

The New Address Register (NAR), on the I/O board, is set by the Controller. The new address from the NAR is digitally added to the CAR, which is in one's complement form. The sum is used to address a pair of ROM's. The ROM outputs are operated in a D/A configuration. The error signal used to position the carriage is derived from these ROM outputs.

5.3.4.3 Operational Status

The movement of the carriage to a different track is begun by a Seek command from the Controller. At this time, the contents of the NAR are examined, and if the number just loaded exceeds 407 (203 for 206D, 306D), it is identified as an Illegal Address and no further action is taken. When the content of the NAR is a legal address, the error signal activates the Voice Coil control circuits on the SAB, which results in carriage motion. This operation is timed, and when the carriage reaches the new address within 300 milliseconds, the Controller is sent a Seek Complete status. The Operational status circuits also determine the Ready status. The Operational status is developed on the DCB and is indicated on the block diagram as control logic for Seek Complete.

5.3.4.4 Index/Sector Detection

Both the fixed disk and the removable disk have notches in their sector rings. These notches are detected magnetically. The index and sector pulses are separated by the pulse separation logic on the DCB and are then sent to the Controller via the multiplexing logic on the I/O board.

5.3.4.5 Unit/Disk/Head Selection

The Controller can select the particular drive, (from a daisy chain), the fixed or removable disk, and the top or bottom read/write head for that disk. The processed signals for disk and head selection are decoded by the Head Select circuits on the R/WA board to actuate a specific head for a read or write operation.

5.3.4.6 Read or Write

The Read/Write and Head Select circuits are shown in the Read/Write Amplifier schematic. The signals read from the disk are amplified by the Read Data Amplifier contained on the R/WA board. The R/W data are formatted by the Data Translator board whenever necessary. The recovered data and the data clock are output to the Controller.

5.3.4.7 Temperature Compensation

The drive uses four thermistors to develop temperature compensation. Three thermistors monitor baseplate temperature and one monitors disk air temperature. The thermistor information is used on the Temperature Compensation board to develop two off-setting voltages, DC thermal, and transient thermal. The off-setting voltages offset the heads in relation to temperature, thus maintaining them on track regardless of the expansion and contraction of the disk, head, and baseplate materials. Temperature compensation is not necessary when the unit is being utilized at 100 TPI and should be jumpered out in this configuration.

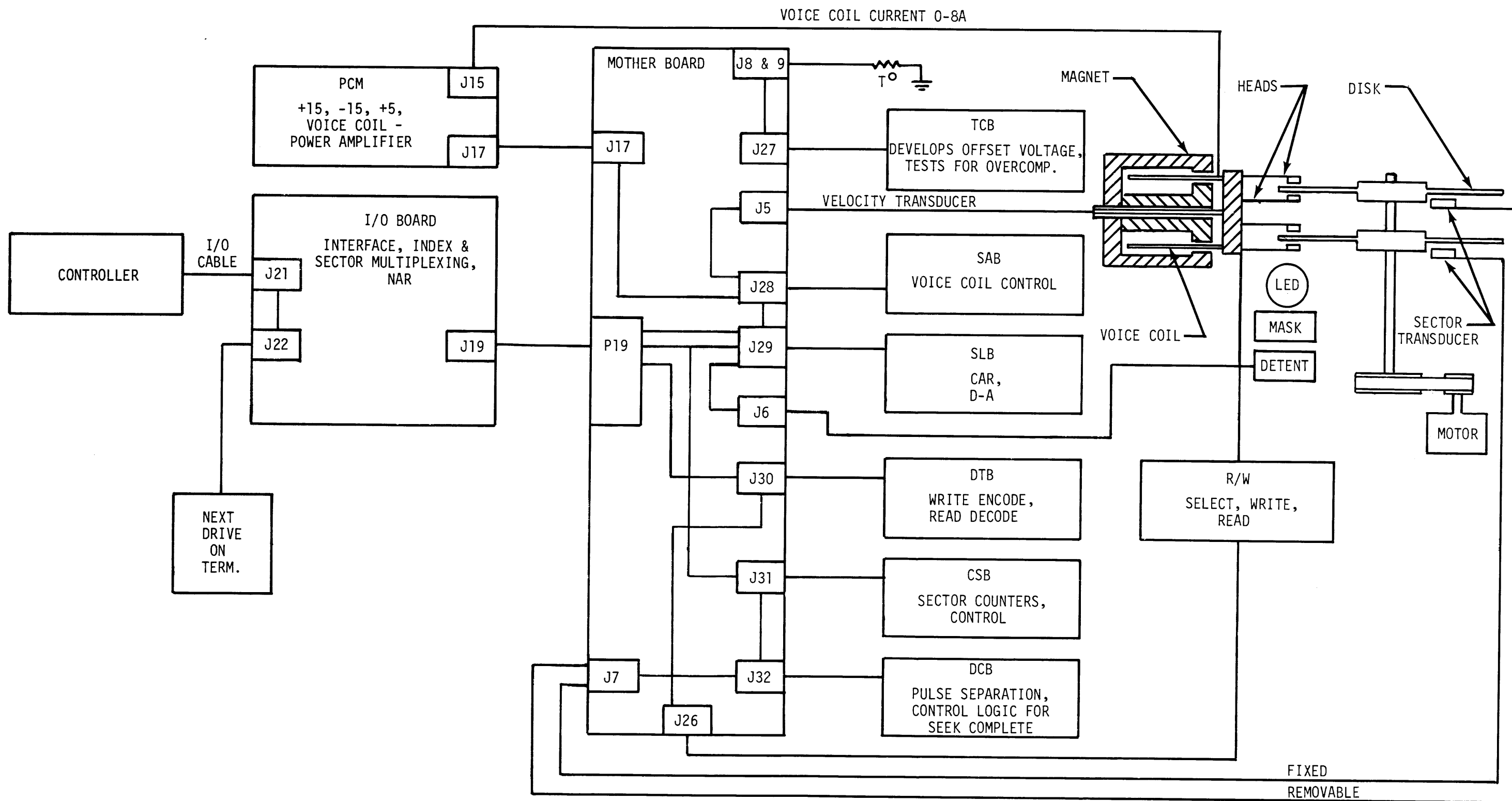


Figure 5-7. Block Diagram

5.4 CIRCUIT CARDS

The Disk Drives contain the following circuit cards.

- Power Control Module (PCM)
- Input/Output Board (I/OB)
- Drive Control Board (DCB)
- Control Sector Board (CSB)
- Servo Logic Board (SLB)
- Servo Analog Board (SAB)
- Temperature Compensation Board (TCB)
- Read/Write Module (R/W)
- Data Translator Board (DTB)

5.4.1 Power Control Module (PCM)

The PCM contains +15, -15, and +5-volt regulators, the servo amplifier, and drive interconnection circuitry. (Refer to Figure 5-8.)

5.4.1.1 ±15-Volt Regulator Circuit

The ±15-volt regulator (IC 3) is located at coordinates D6 in Figure 5-6. The +15 volts are developed from the +24 volts applied to IC 3-1. Regulated -15 volts are developed from the -24 volts applied to IC 1-3, which is the -15 volt regulator. The 15-volt regulators are adjustable and should be adjusted to 15 ± 0.1 volts.

5.4.1.2 +5-Volt Regulator Circuit

The +5-volt regulator (IC 2) is located at coordinates D3 in Figure 5-8. IC 2 is a 723 adjustable voltage regulator with emitter follower Q12 and current driver Q16. Output of the +5-volt regulator should be adjusted to $+5 \pm 0.1$ volts. The +5-volt supply is short-circuit protected by foldback limiting circuitry associated with the 723 regulator.

5.4.1.3 Servo Amplifier

The Servo Amplifier circuit is located at coordinates E through H in Figure 5-8. The servo amplifier is a DC amplifier driving the voice coil at connector J15 (referred to as positioner coil in the schematic) with an output signal between +24V and -24V. The +24 or -24 volts supplied to the amplifier is developed by diode rectifier, CR2 in the relay module. The driving current is applied to the voice coil on pins 3 and 4 of connector J15. Pins 6 and 7 of J15 are the return current path from the voice coil.

The voltage applied to J15-3 is controlled by the signal Servo Amp at coordinates F8 in Figure 5-8. When Servo Amp is at +6 volts, there is +24 volts output from J15-3. When Servo Input is at -6 volts, there is -24 volts output from J15-3. When Servo Amp is at ground, J15-3 is at ground. The unregulated +24 volts from diode rectifier CR2 is applied to the PCM at J2-1 and fused with F1 (4ASB). The +24 volts through F1 is applied to power transistors Q1, Q3, Q4, Q6, Q8, and Q18.

The -24 volts applied to the voice coil is the unregulated -24 volts from diode rectifier CR2. This voltage is applied to the PCM at J9 and is fused by F2 (4ASB). The -24 volts through F2 is applied to power transistors Q2, Q5, Q7, Q9, and Q19. Current feedback, derived from the 0.1-ohm series resistor R20 to IC 6A-2 in the Servo Analog board, ensures that the voice coil is current driven.

Before the output of the servo amplifier can be applied to the voice coil, the safety relay K1 must be energized, which closes the normally open contacts and ties pin 7 to pin 8. The coil of the safety relay is at coordinates D1 in Figure 5-8. K1 is energized whenever transistor Q15 is turned on. Q15 is turned on by the signal Emergency Retract which is from the CSB. This signal is positive when all DC voltages are active and all servo boards are installed on the card cage. When K1 is deenergized, a path is provided from contact pin 6 to pin 8 which forces an emergency retract to occur if the carriage is off the home switch; a -24 volts is available at J2-12, the home switch normally closed contact, whenever the carriage is extended. If the carriage was extended, this -24 volts is applied to the voice coil and will drive the carriage in a reverse direction until the home switch opens. This path can be traced through the interconnection diagram in Figure 5-2.

5.4.1.4 Drive Status Circuitry

Drive Status circuitry (Q13, Q14, and Q17) is located at coordinates B7 and C1 in Figure 5-8. Transistor Q14 is the driver for the interlock solenoid and the Stop indicator which are wired in parallel. Q14 is turned on by the signal Stop which is brought true approximately 60 seconds after the drive Start/Stop switch is set to the Stop position. Turning on Q14 energizes the solenoid and lights the Stop indicator. Transistor Q13 is the driver for the Ready indicator; Q13 is turned on when the signal Ready is at a positive level. Turning on Q13 lights the Ready indicator.

The three control signals CAR Home (-), Motor On (-), and Brush Home (+) are developed by switches. The CAR Home (-) signal at J16-31 is developed by the Carriage Home switch and is at ground level when the carriage is at home. The Motor On signal at J16-25 is developed by the Start/Stop switch and is at ground level

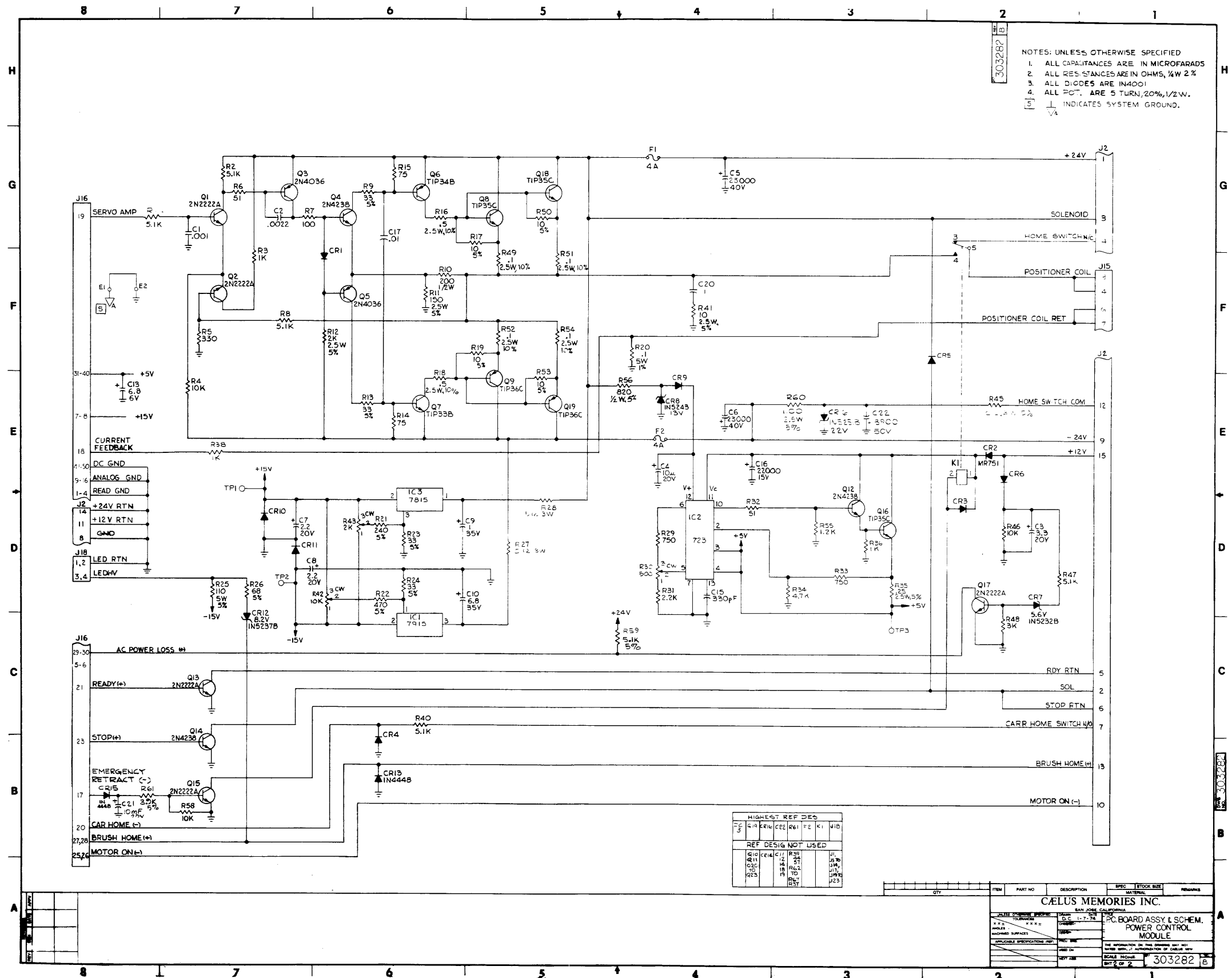


Figure 5-8. Power Control Module Schematic

when the Start/Stop switch is set to the Start position. The Brush Home signal at J16-23 is always at a positive level because there is no brush motor in a 206 drive.

The final signal developed on the PCM is AC Power Loss. This signal is generated by transistor Q17 located at coordinates C1 in Figure 5-8. Q17 is biased such that if the +12 volts applied drops below 8 volts, Q17 turns off, and AC Power Loss is generated. AC Power Loss high causes a low velocity head retract.

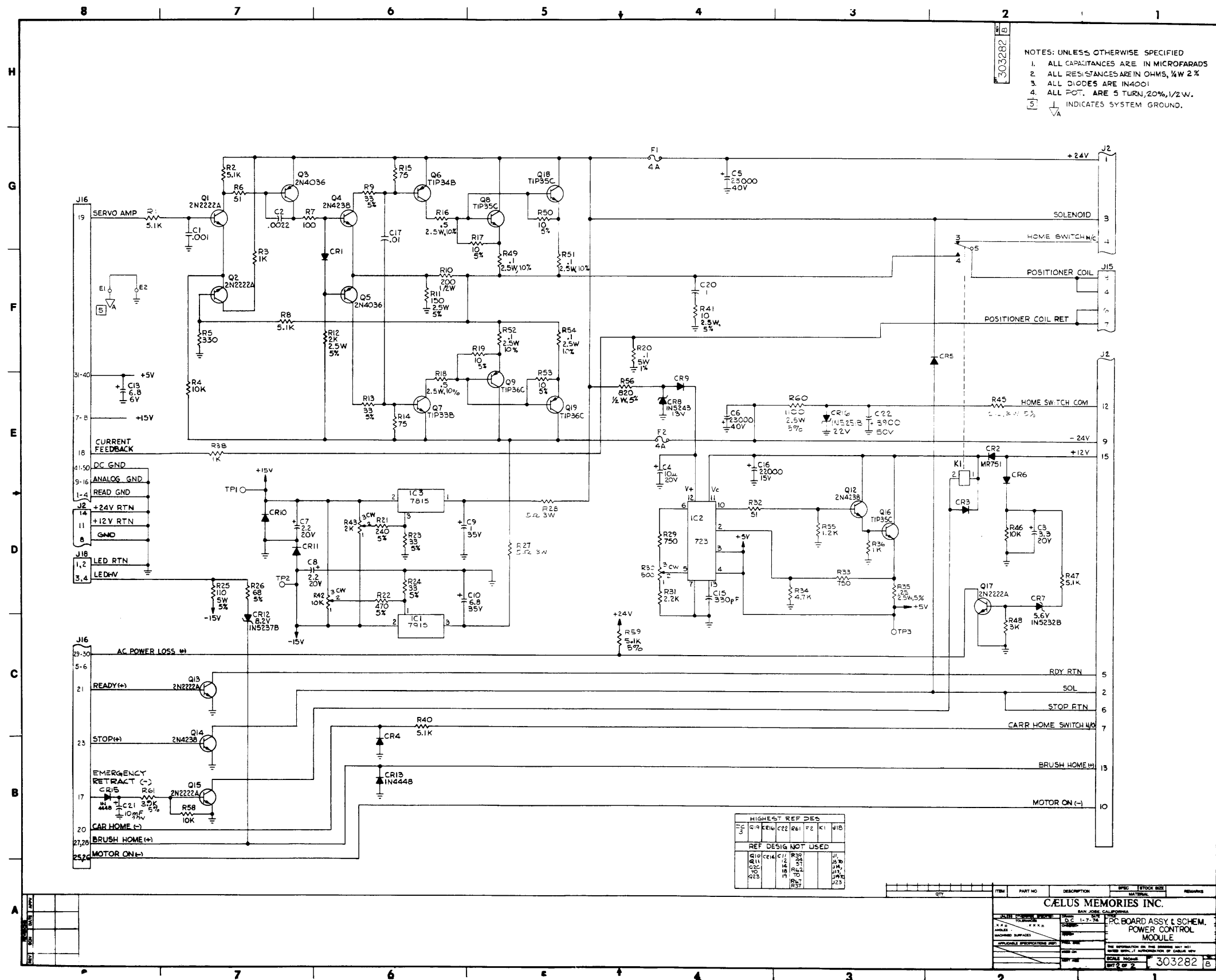


Figure 5-8. (Repeat) Power Control Module Schematic

5.4.2 Input/Output Board (I/OB)

The basic function of the I/O board is to interface between the drive and the Controller. Commands from the Controller are received on IC's 20, 21, 22, and 23. Line drivers IC's 8, 9, 10, 11, 12, and 13 send status and data to the Controller. To accommodate the various Controllers, optional jumpers have been designed into the I/O board; these jumpers are shown in Figure 5-10 and Table 2-1.

5.4.2.1 Input/Output Board, Sheet 2 of 3.

IC's 18 and 19 are the New Address Register (NAR). (See Figure 5-9). The NAR receives the address input lines from the Controller on IC's 22 and 23. This new address is strobed into the NAR with a Seek pulse from the Controller which is received by the drive on IC 22-5. The Seek pulse is Anded with PART DETENT (+) on IC 6-2 to ensure that a new Seek operation cannot be started until the previous Seek terminates. The NAR output is applied to J19, the Mother board connector, for interconnection with the Servo Logic board. The Servo Logic board contains the Cylinder Address Register and circuitry which will compare the sum (NAR plus CAR) to develop servo drive.

The NAR is also compared on IC's 1 and 2 with a hard-wired address of 407. Any address larger than 407 will cause IC 1-15 to be low: this output is Illegal Address. IC 3 is fired with each pulse for 23 microseconds to allow the address lines time to settle. IC 3-10 is then fired for 2.3 microseconds which establishes the pulse width of the Illegal Address, IC 6-8, and Address Acknowledge, IC 6-11, status lines. These lines will be a level if jumpers E5 to E6 are not connected.

The output of IC 9-3 (Ungated Attention) will be true due to either a Seek Incomplete (IC 7-1) or a Seek Complete (IC 7-2). Both Seek Complete and Seek Incomplete are developed on the Drive Control board. The jumper pins 22 through 27 control the data path; these jumpers are shown in Table 2-1.

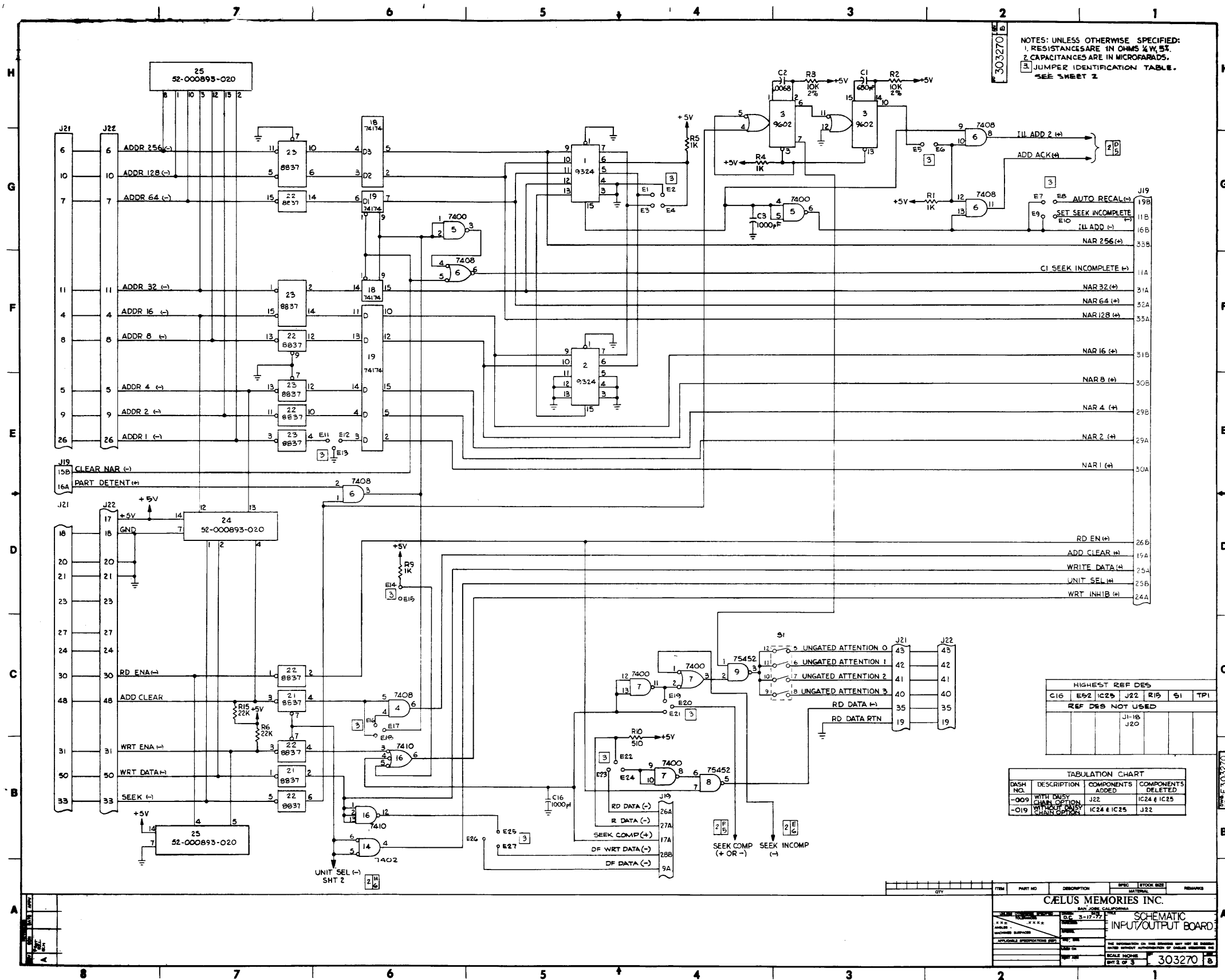


Figure 5-9. Input Output Board Schematic, Sheet 2 of 3

5.4.2.2 Input/Output Board, Sheet 3 of 3.

5.4.2.3 Index and Sector Multiplexing

Index and sector multiplexing is accomplished on the multiplexer chip IC 17. (See Figure 5-10). In the multiplex mode of operation, selected by connecting a jumper from E48 to E49, the outputs from IC 11-5 (Index Pulses) and IC 10-5 (Sector Pulses) are from the fixed disk when pin 1 of the multiplexer IC 17 is low, and from the removable disk when IC 17-1 is high.

When multiplex has been selected by jumper E48 to E49, IC 12-5 is connected to output Illegal Address (jumper E40 to E41), and IC 13-5 outputs Address Acknowledge (jumpers E43 to E44 and E46 to E47). The multiplexer IC 17 operates by connecting pins 2 to 4, 5 to 7, 14 to 12, and 11 to 9 when pin 1 is low, and pins 3 to 4, 6 to 7, 13 to 12, and 10 to 9 when pin 1 is high.

When multiplex is not used (no jumper E48 to E49), IC 12-5 outputs fixed disk index pulses (jumper E39 to E41), and IC 13-5 outputs fixed disk sector pulses (jumpers E42 to E44 and E45 to E47).

An Illegal Address is defined as being an address larger than 407. Any address presented to the drive by the Controller larger than 407 will drive IC 12-5 low. A Legal Address is defined as an address between 0 and 407 inclusive, and will cause Address Acknowledge to be true, i.e., IC 13-5 is low.

IC's 9 through 13 are all line drivers to the Controller. IC's 16 and 20 invert the head select and disk select lines such that any level may be used on the I/O line to select top or bottom. See Table 2-1 for head and disk select jumpers.

The Unit Select switch is shown in Figure 5-10 at coordinates H7. This is a four-position switch that is used to select the disk file address. The output of IC 20-10 is low when true, and IC 20-12 is high when true. Unit Select is used to gate the input and output lines within the drive.

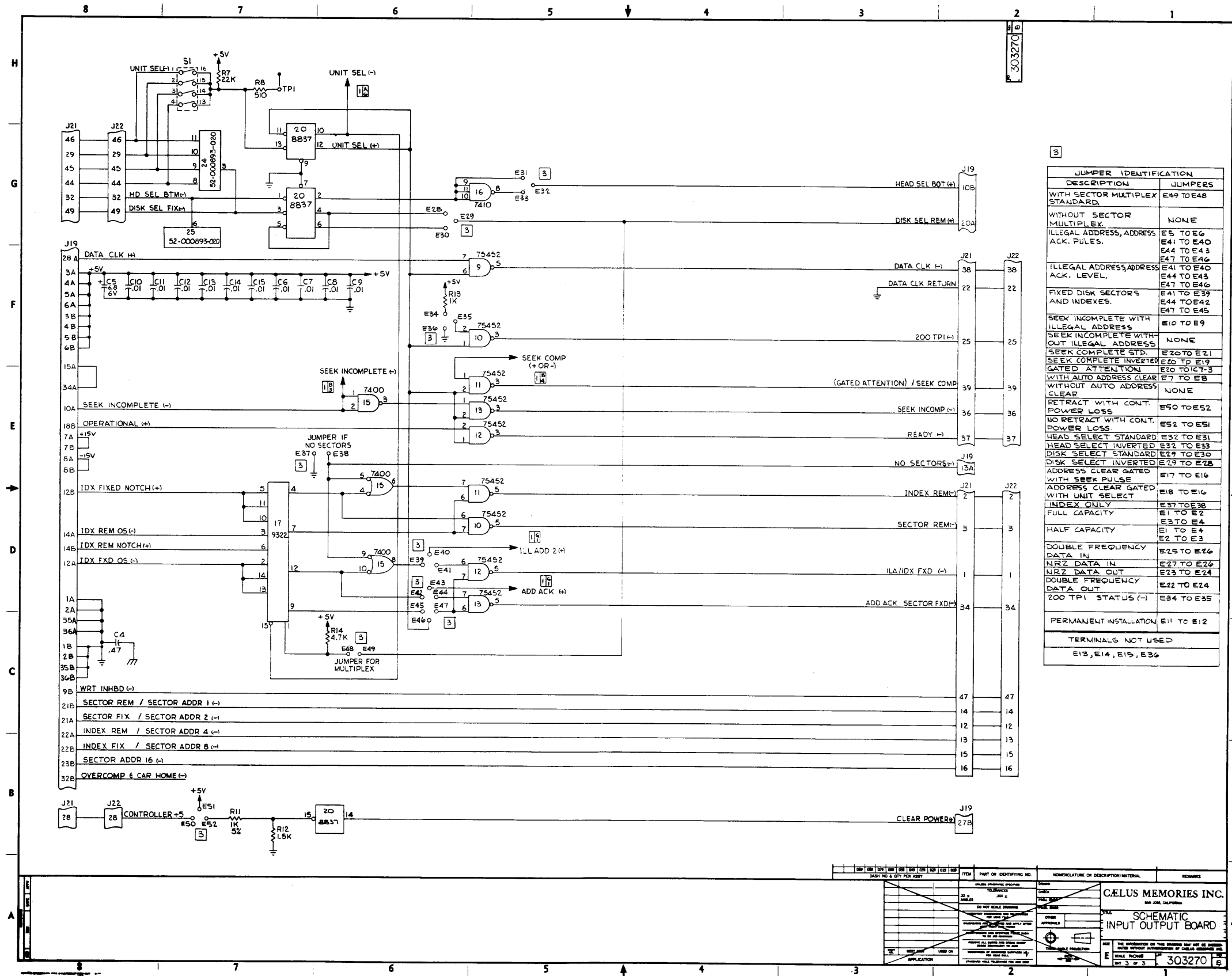


Figure 5-10. Input/Output Board Schematic, Sheet 3 of 3

5.4.3 Drive Control Board (DCB) Schematic

The Drive Control board has several functions. It receives index/sector information, generates the up-speed signal, and provides the sequential logic for loading the heads. It establishes that temperature compensation is within limits prior to initiating Ready and provides the servo Initialized signal. The Drive Control board is illustrated in Figure 5-11.

5.4.3.1 Index and Sector Circuitry

The Index and Sector circuitry consist of IC's 1 through 5 located at the top of Figure 5-11. The Index and Sector circuitry amplify and shape the pulses from the index/sector transducers, and monitor the rotational speed of the disks.

The raw index and sector waveform from the fixed disk transducer is applied to pin 5 of the Mother board connector, and can be monitored on test point 1. While monitoring TP1, the expected output from the transducer is from 200 to 600 millivolts measured base-to-peak.

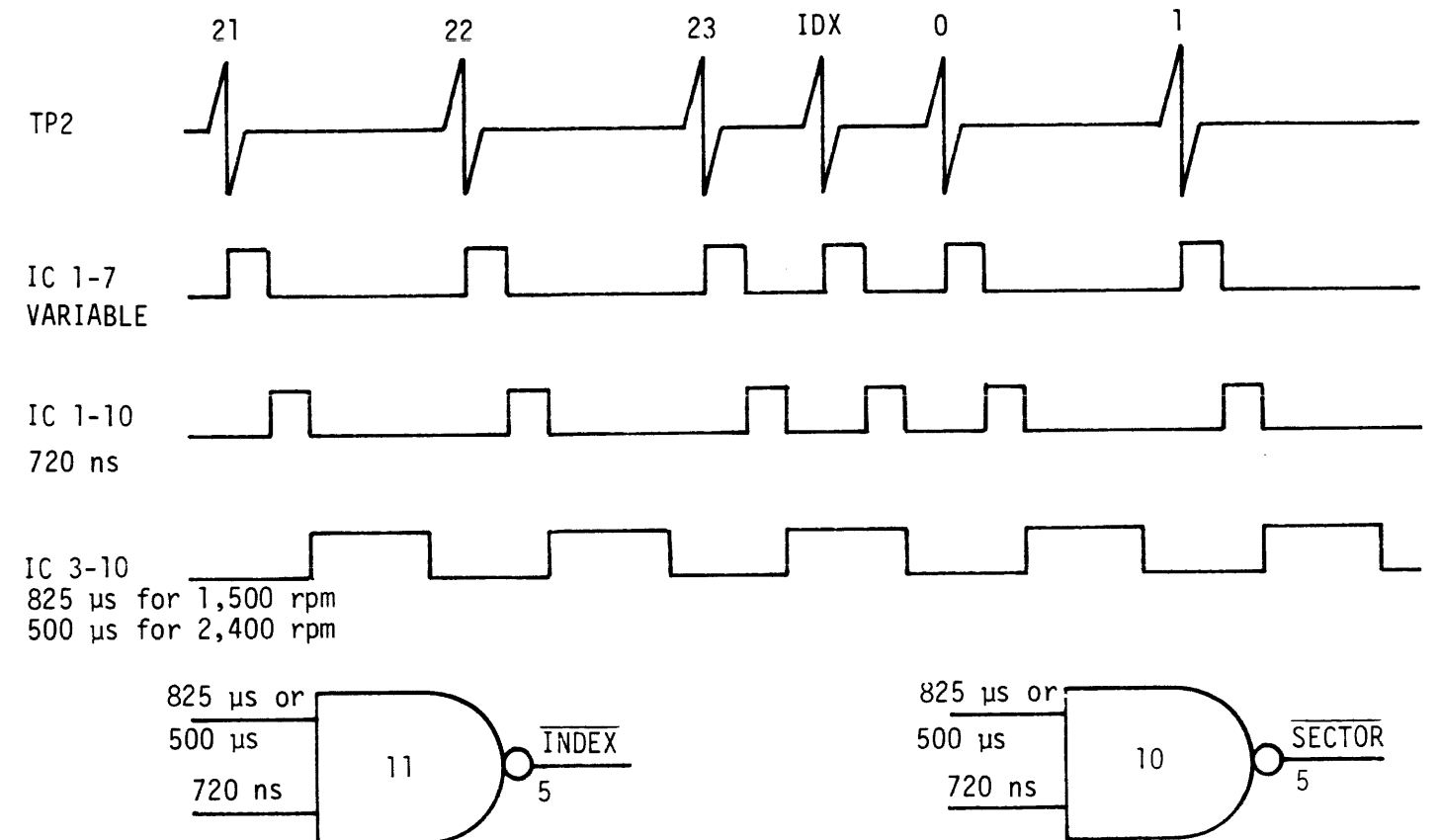
The raw index and sector waveform from the removable disk are first fed via pin 6 of the connector, and jumper pins E1 to E3, to the Processing Amplifiers IC's 8-7 and 8-1.

This is necessary because front-loading disk cartridges have slotted aluminum alloy hubs. The output waveform, caused by eddy-current effects in the magnetic transducer, is smaller in amplitude and has different characteristics from that obtained from a slotted magnetic-alloy hub.

The output waveform from the processing amplifier is similar in character to that obtained from the fixed disk transducer on the magnetic hub and is fed via jumper E4 to E2. It can be monitored at test point 2, and should be at least 0.5 volts base-to-peak.

The raw index and sector waveforms are applied to voltage comparators IC's 4 and 5. The outputs of IC's 4 and 5 are applied to a series of one shots which discriminate the index pulses from sector pulses. The index pulses and sector pulses are then output to the Controller on separate lines. IC's 1 and 3 and the one shots are used to discriminate index and sector pulses for the removable disk. IC 2 is the one shot used for the fixed disk. For a 206 drive, E1 is jumpered to E3, and E4 to E2.

There is an additional one shot, IC 1-7, which is used for the removable disk. This is an adjustable one shot and is used to delay the index and sector pulses prior to firing the first one shot in the chain. This is necessary to provide compatibility from drive to drive as there may be a difference in the mechanical po-

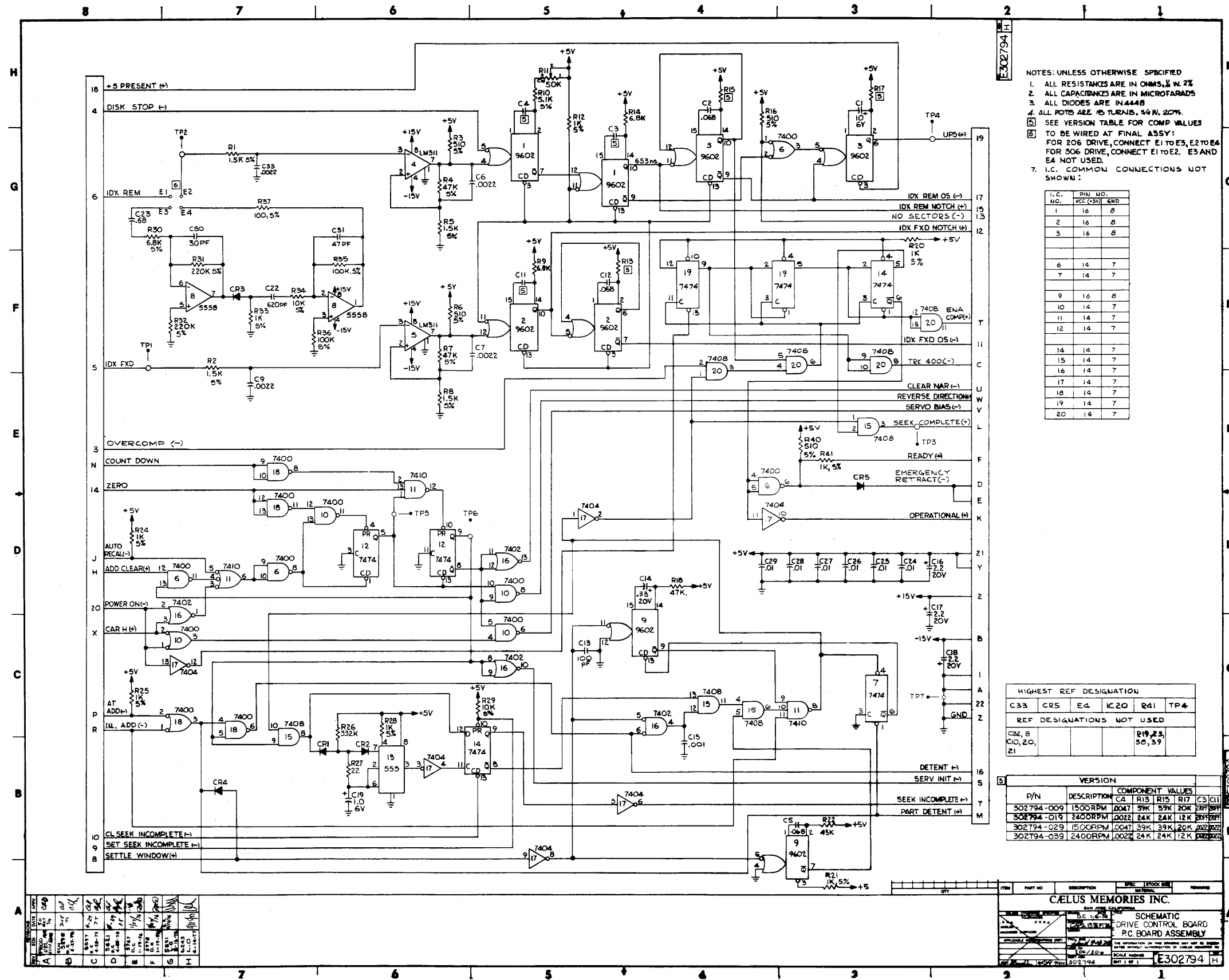


600-52

Figure 5-12. Index/Sector Timing

sitioning of the sector transducer. Every index or sector pulse detected fires IC 37-9 and when this one shot times out, it then fires the first one shot in IC 1 pins 9 and 10, the removable disk index/sector detection circuitry. This timing relationship can be seen by following the timing chart shown in Figure 5-12. The top line of the timing diagram represents the raw index and sector waveforms as seen on either TP1 or TP2. The pulses represented on the timing diagram are sector pulses 21, 22, 23, 0, and 1. The index pulse occurs between the sector 23 pulse and the sector 0 pulse. The second line on the timing chart shows the one shot IC 1-7. This one shot is only used in the removable disk circuit for drive compatibility. (The fixed disk circuit has no equivalent one shot.)

Every raw index or sector pulse will fire the one shot IC 1-7 whose output is adjustable and delays the raw index or sector pulse to the output line for the Controller. When the one shot



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTANCES ARE IN OHMS, $\frac{1}{2}$ W. 5%
 2. ALL CAPACITANCES ARE IN MICROFARADS
 3. ALL DIODES ARE IN4448B
 4. ALL POTS ARE 15 TURN, 1/4 W, 20%
 5. SEE VERSION TABLE FOR COMP VALUES
 6. TO BE WIRED AT FINAL ASSY:
 FOR 206 DRIVE, CONNECT E1 TO E2, E2 TO E4
 FOR 306 DRIVE, CONNECT E1 TO E2, E3 AND
 E4 NOT USED.
 7. I.C. COMMON CONNECTIONS NOT
 SHOWN:

I.C. NO.	PIN NO.	END
1	16	8
2	16	8
3	16	8
6	14	7
7	14	7
9	16	8
10	14	7
11	14	7
12	14	7
14	14	7
15	14	7
16	14	7
17	14	7
18	14	7
19	14	7
20	14	7

HIGHEST REF DESIGNATION				
C33	CR5	E4	K20	R41 TP4
REF DESIGNATIONS NOT USED				
C32, 8			R19, 23	
C10, 20,			30, 39	
Z1				

VERSION				
P/N	DESCRIPTION	COMPONENT VALUES		
		C4	R13	R15 R17 C3 C11
302794-009	1500RPM	.0047	39K	39K 20K 20K 20K
302794-019	2400RPM	.0022	24K	24K 12K 20K 20K
302794-029	1500RPM	.0047	39K	39K 20K .0022 .0022
302794-039	2400RPM	.0022	24K	24K 12K .0022 .0022

REV	DATE	BY	CHKD	DESCRIPTION
A	10/1/74
B	10/1/74
C	10/1/74
D	10/1/74
E	10/1/74
F	10/1/74
G	10/1/74
H	10/1/74
I	10/1/74

CELUS MEMORIES INC.

SCHEMATIC
 DRIVE CONTROL BOARD
 P.C. BOARD ASSEMBLY

302794

Figure 5-11. Drive Control Board Schematic

IC 1-7 times out, the 720-nanosecond one shot, IC 1-10, is fired. Then, 720 nanoseconds later when the one shot times out, the 825-microsecond one shot, IC 3-10, is fired. This is represented by line four of the timing chart.

The only time that the 825-microsecond one shot is true at the same time as the 720-nanosecond one shot is when the index pulse occurs. All other pulses, the sector pulses, fire the 720-nanosecond one shot during the period of time in which the 825-microsecond one shot was not true. IC's 10 and 11 on the I/O board, represented at the bottom of the timing chart, show the 720-nanosecond one shot Anded with the 825-microsecond one shot. The 720-nanosecond one shot firing at the same time as the 825-microsecond one shot fires develops an index pulse on the output of IC 11-5. The 720-nanosecond one shot is also Anded on IC 10 with the 825-microsecond not true. If the 720-nanosecond one shot was firing but the 825-microsecond one shot was not firing, then the output of 10-5 is true, developing a sector pulse. The one shot, IC 2, operates in exactly the same manner for the fixed disk.

5.4.3.2 Up-Speed

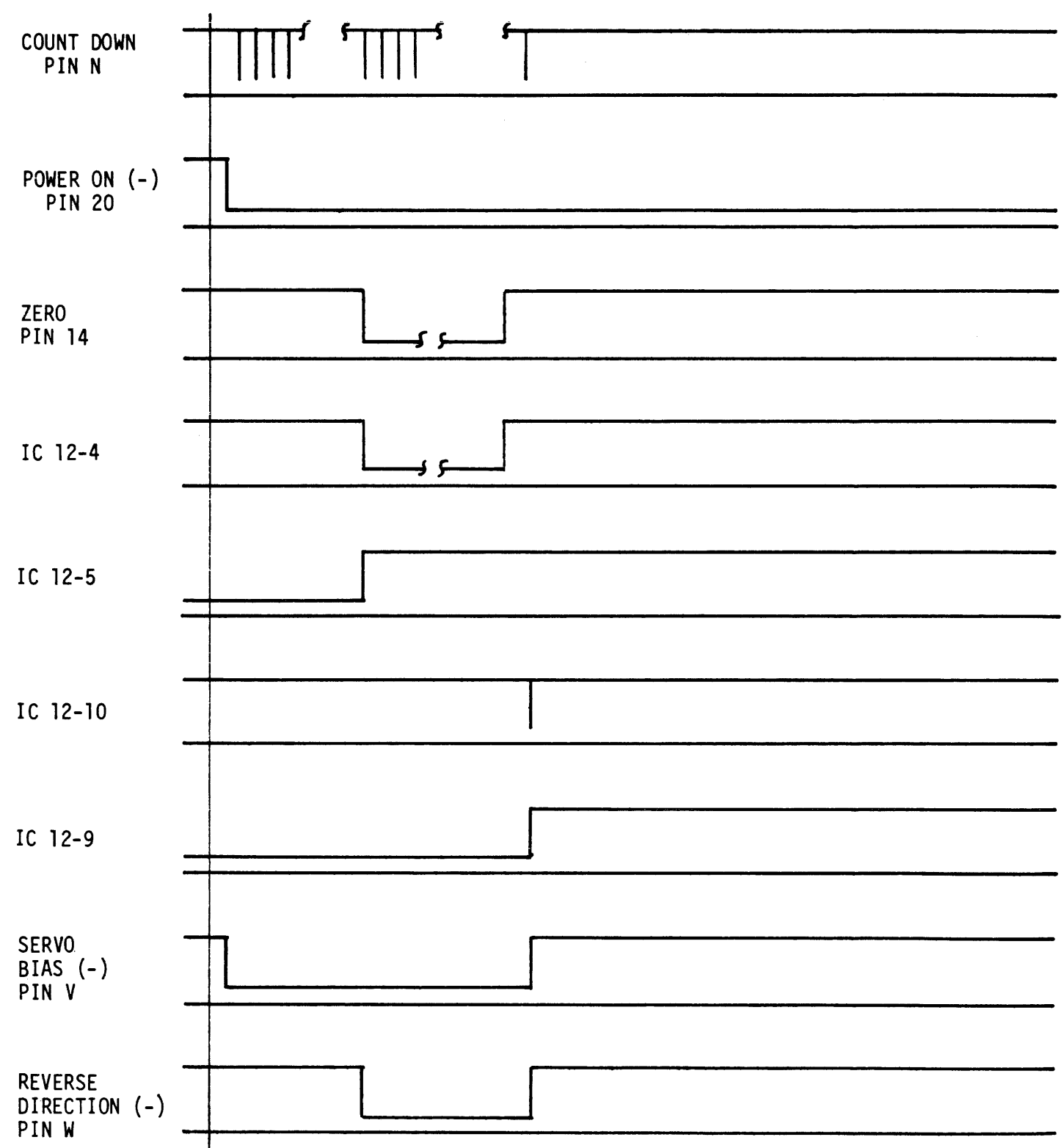
The firing time of IC 3-6 establishes the minimum time period between two consecutive index pulses. When the drive is rotating at 75 percent of speed, index pulses occur at a rate fast enough to retrigger the up-to-speed one shot with each index pulse and maintain the output pin 6 at a high level. If the speed of the drive drops below 75 percent, IC 3-6 will not remain at a high level. Each time the output of 3-6 goes low, the up-to-speed flip flop on the control sector will be reset. Before the up-to-speed flip flop can be set again, the up-to-speed one shot must be high for an additional 10 seconds.

The "no sectors" is selected on the I/O board by installing a jumper between pins E37 and E38. This allows the up-to-speed one shot to trigger once every rotation of the disk when there is only a single slot. Normally, the gating looks for an index pulse between two sector pulses.

5.4.3.3 Head Load Logic

When power is turned on and the disk is coming up to speed, Power On (-), pin 20 is false (+) which holds IC's 12-5 and 12-9 reset. This condition holds IC 10-8 high, which in turn gives a forward-direction signal to the servo (pin W). Servo Bias is held off by IC 10-3 being low. (See Figure 5-13.)

When Power On goes true, Servo Bias is turned on and the carriage moves forward. When the zero signal (pin 14) goes low, IC 12-5 is set via pin 4. This condition causes IC 10-8 to send reverse direction to the servo. The carriage reverses direction.



200-31

Figure 5-13. Head Loading Sequence

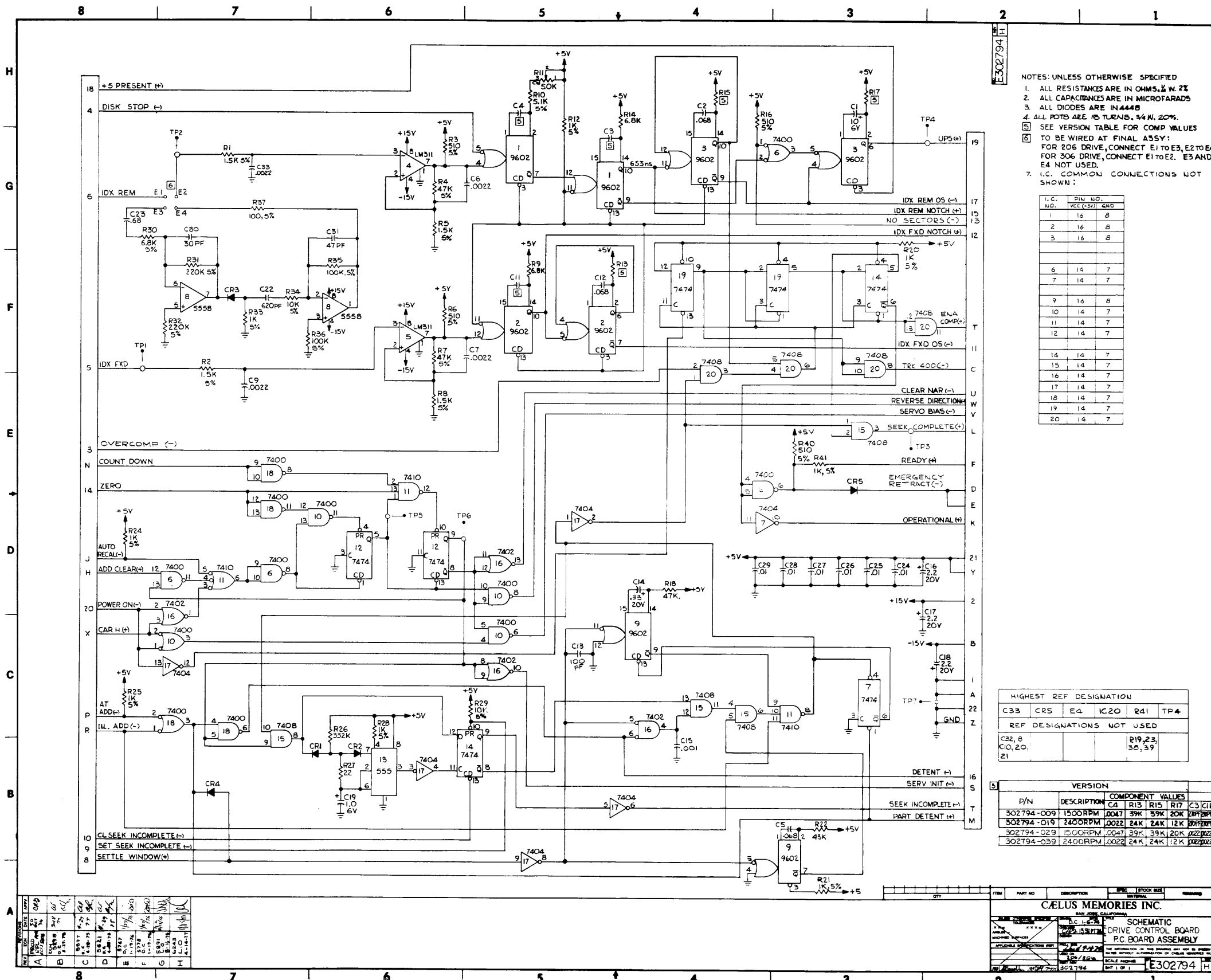
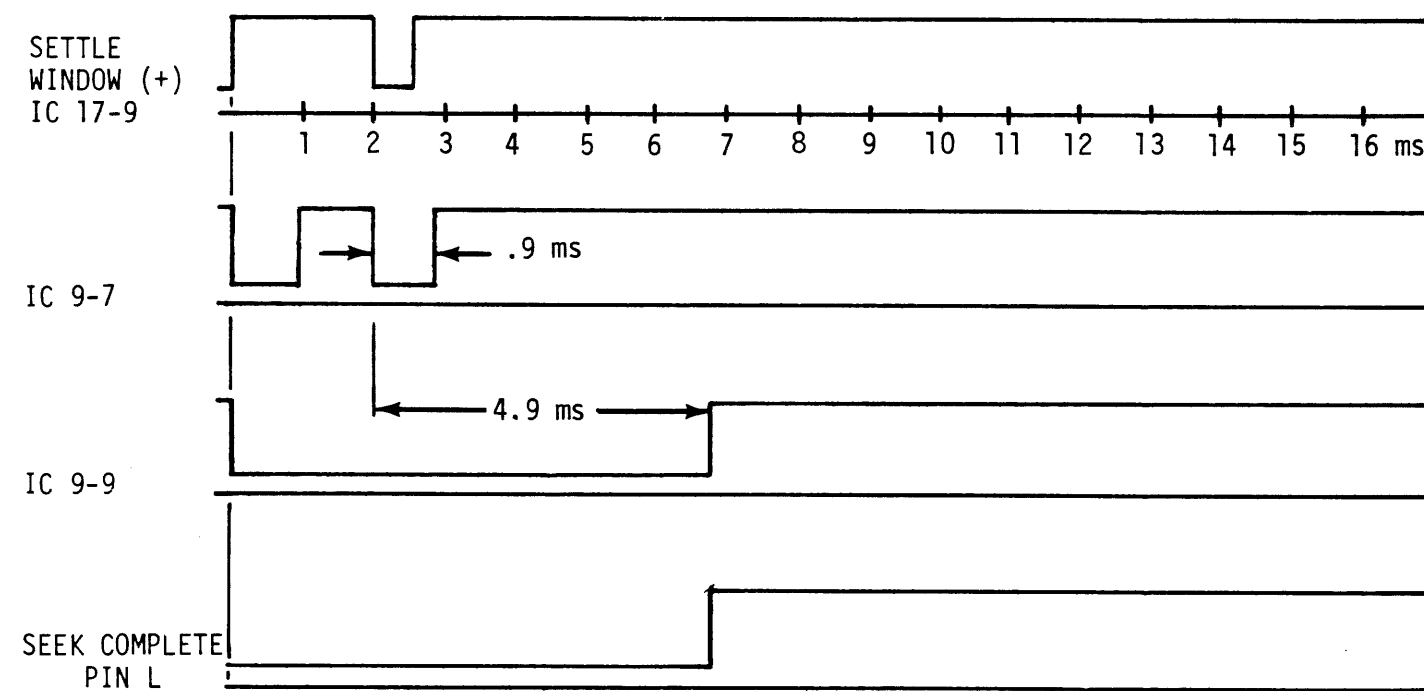


Figure 5-11. (Repeat) Drive Control Board Schematic

The zero signal changes state to high as it passes zero in this direction and enables IC 11-13. Thus, the next count-down pulse sets IC 12 through pin 10. The servo Initialized signal (pin S) goes true (low) via IC's 16-8, 9, and 10, putting the servo in a normal operating mode. Notice that the same sequence is initialized with an Auto Recall or Address Clear. A timing diagram for the head load sequence is included in Figure 5-13.

5.4.3.4 Seek Complete/Incomplete Logic

Refer to Figure 5-14 for a Seek Complete timing diagram. This diagram assumes no Illegal Address or temperature compensation.



(WORST CASE SHOWN FOR CLARITY)

200-32

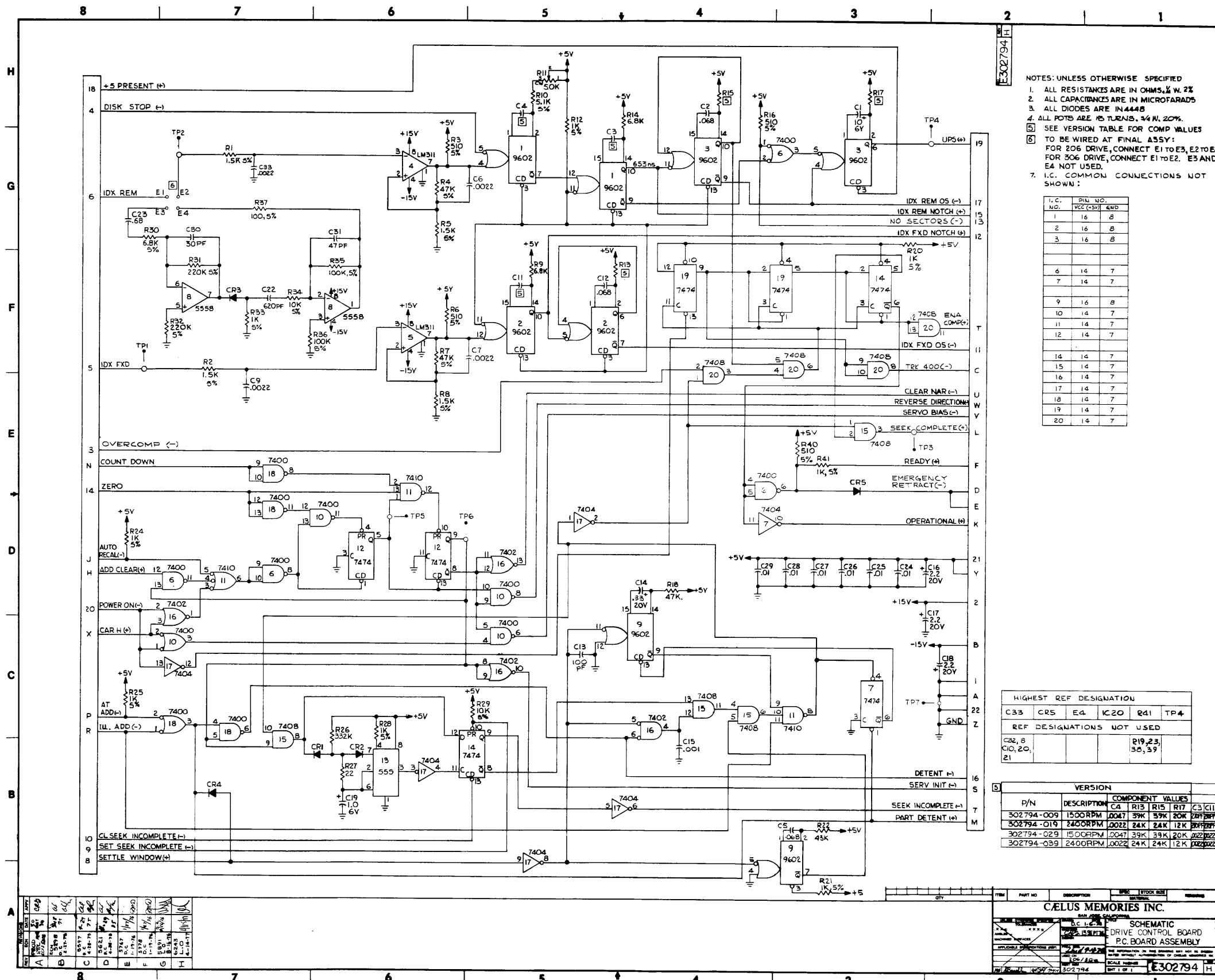
Figure 5-14. Seek Complete Timing Diagram

At the beginning of a Seek, the IC 13 timer at zone B6 is fired. If, at the 330-millisecond timeout, the carriage is not at the address, the timer fires, setting IC 14 (coordinates B6) causing a Seek Incomplete (pin 7).

In normal operation, the At Address and Settle Window signals will go true when the carriage arrives at the correct position. After a 6.8-millisecond timeout, pin L (Seek Complete) will go true.

5.4.3.5 Forced Overcomp Check

IC 19 at coordinates F4 forces a check of temperature compensation required at track 400 after the heads have loaded. If greater compensation is required than the circuit is capable of, Overcomp on pin 3 is developed, preventing a seek complete and thus ready from being developed. Once the temperature of the unit stabilizes, the final flip flop (IC 19) sets and ready is developed.



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTANCES ARE IN OHMS, % W. 2%
 2. ALL CAPACITANCES ARE IN MICROFARADS
 3. ALL DIODES ARE IN 444B
 4. ALL POTS ARE 10 TURNS, 1/4 W, 20%
 5. SEE VERSION TABLE FOR COMP VALUES
 6. TO BE WIRED AT FINAL ASSY:
 FOR 206 DRIVE, CONNECT E1 TO E3, E2 TO E4
 FOR 306 DRIVE, CONNECT E1 TO E2. E3 AND
 E4 NOT USED.
 7. I.C. COMMON CONNECTIONS NOT
 SHOWN:

I.C. NO.	PIN NO.	VCC (+5V)	GND
1	16	8	
2	16	8	
3	16	8	
6	14	7	
7	14	7	
9	16	8	
10	14	7	
11	14	7	
12	14	7	
14	14	7	
15	14	7	
16	14	7	
17	14	7	
18	14	7	
19	14	7	
20	14	7	

HIGHEST REF DESIGNATION			
C33	CR5	E4	IC20
R41	TP4		
REF DESIGNATIONS NOT USED			
C32, 8	C10, 20,		
21		R19, 23,	
		30, 39	

VERSION				
P/N	DESCRIPTION	CA	R13	R15
302794-009	1500RPM	0047	39K	39K
302794-019	2400RPM	0022	24K	24K
302794-029	1500RPM	0047	39K	39K
302794-039	2400RPM	0022	24K	24K

CELUS MEMORIES INC.

SCHMATIC
 DRIVE CONTROL BOARD
 P.C. BOARD ASSEMBLY

302794

Figure 5-11. (Repeat) Drive Control Board Schematic

5.4.4 Control Sector Board (CSB) Standard

The Control Sector board generates the following signals: Power On (-), Stop (+), Emergency Retract (-), and Sector Address lines 2⁰ through 2⁴. The Control Sector Board schematic is shown in Figure 5-15.

5.4.4.1 Power On

The Power On (-) signal, IC 10-4, is used to initiate the head load sequence and is generated when the motor is on, (Motor On (-), IC 9-3); the brushes are home (Brush Home (+), IC 9-11); the drive is up to speed (UPS (+), IC 9-10); and Clear Power (+) (IC 11-12) is not true.

NOTE

Brush Home (+) is always positive for a 206 drive.

When the above conditions are true, a 10-second timer, IC 5-3, is started and 10 seconds later a clock is provided to set the up-to-speed flip flop, IC 8-5. With the up-to-speed flip flop set, Power On (-) is developed which will initiate the head load.

5.4.4.2 Stop (+)

Stop (+), IC 6-6, is the signal that causes the stop light to light on the front panel and energizes the door-locking solenoid. Stop (+) is generated whenever the motor has been turned off (Motor On (-), IC 9-2); the carriage is at home (CAR Home (+), IC 9-1); and the Brush Home (+) signal is positive, IC 9-13. These conditions start the 555 timer, IC 4-3, and 12 seconds later when IC 4 times out, it will set the stop flip flop, IC 8-9.

5.4.4.3 Emergency Retract (-)

The Emergency Retract signal at zone B2 of Figure 5-15 is used for two purposes; one, to cause the heads to retract in case of a power supply failure and two, to prohibit the heads from loading in case of a servo board not being properly installed.

Power supply failure detection is implemented with the voltage divider network of Q1. A servo board improperly installed is detected by routing the Emergency Retract signal through the Temperature Compensation board, Drive Control board, Servo Logic board, Servo Analog board, and the I/O board.

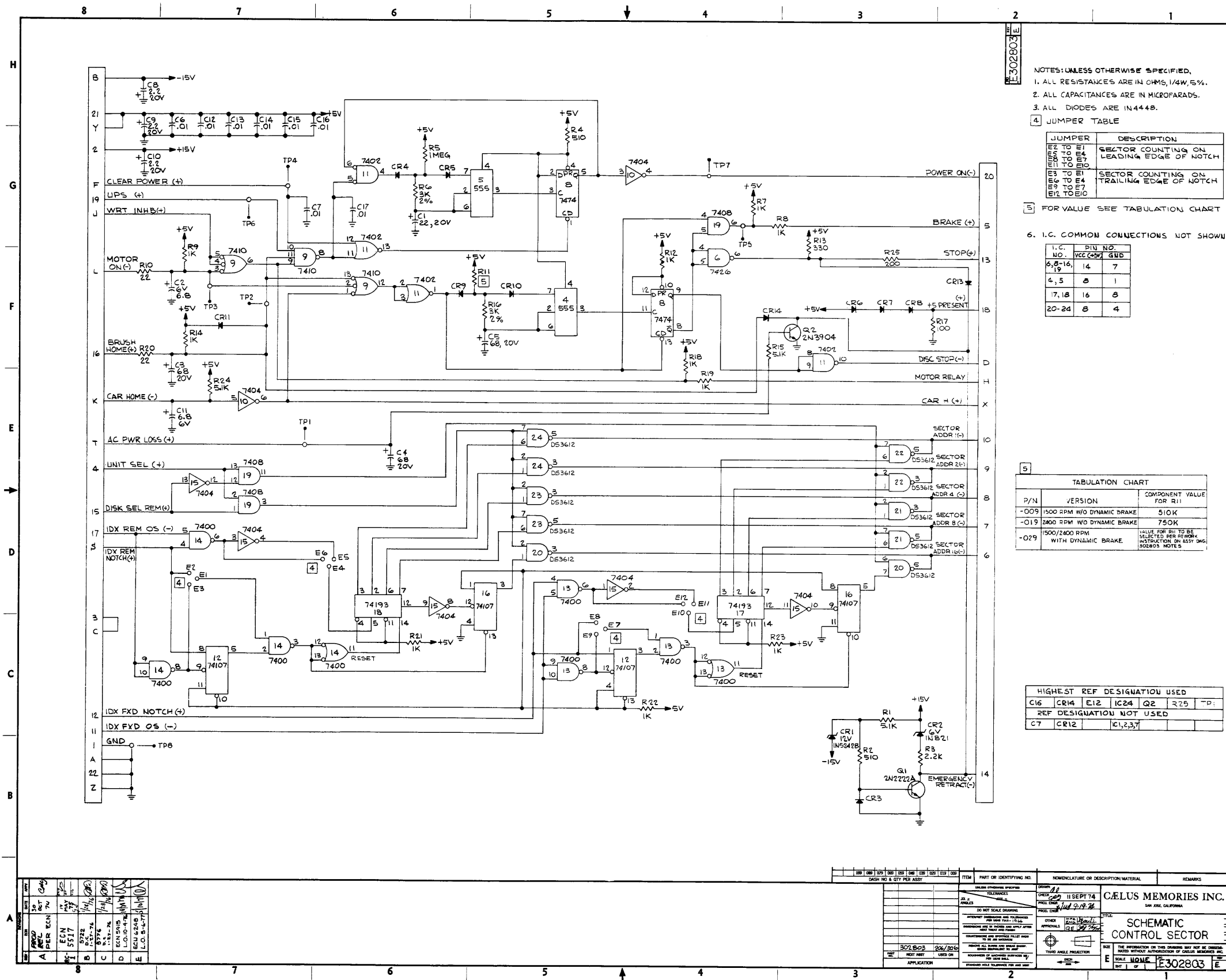


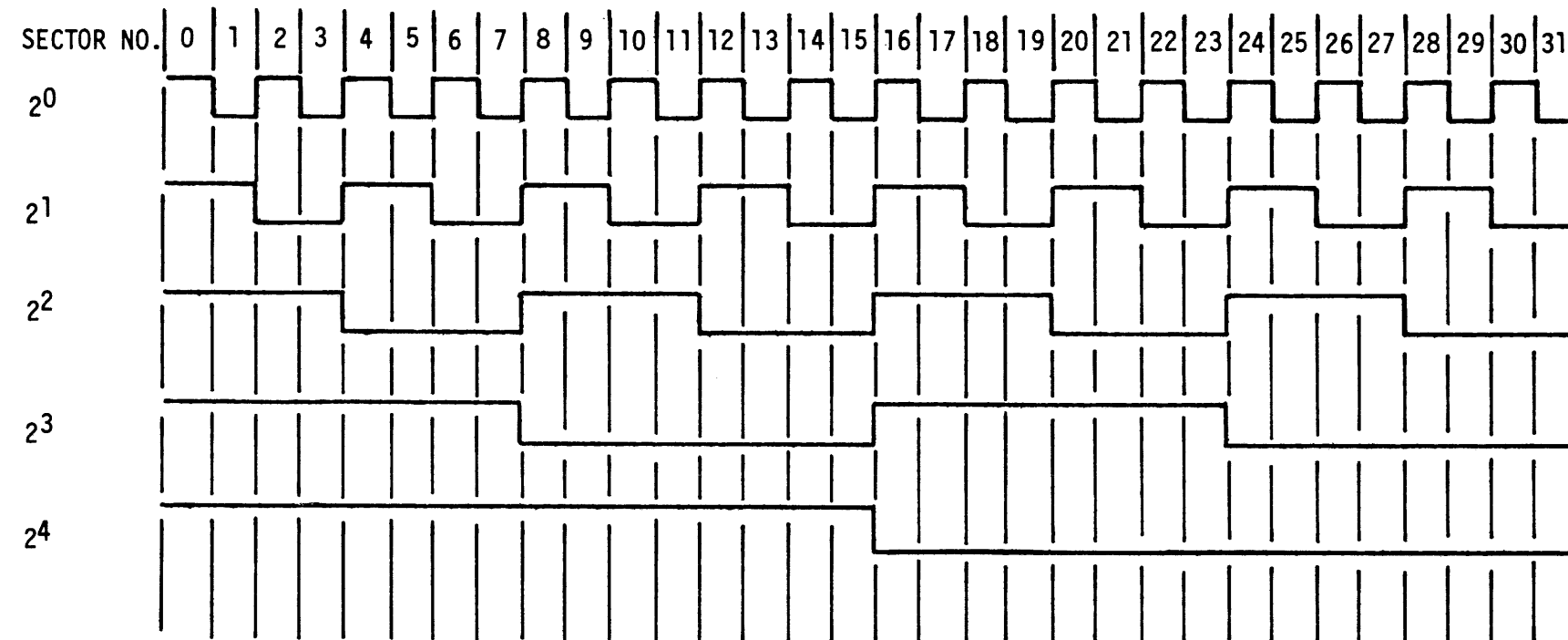
Figure 5-15. Control Sector Board Schematic

5.4.4.4 Sector Address Counter

There are two Sector Counters, one for the fixed disk (IC 17) and one for the removable disk (IC 18). The Sector Address Counters are reset on the first sector pulse following index and each sector pulse advances the counter on the leading or trailing edge of the sector count. This is selected by the option jumper as shown in Table 2-6.

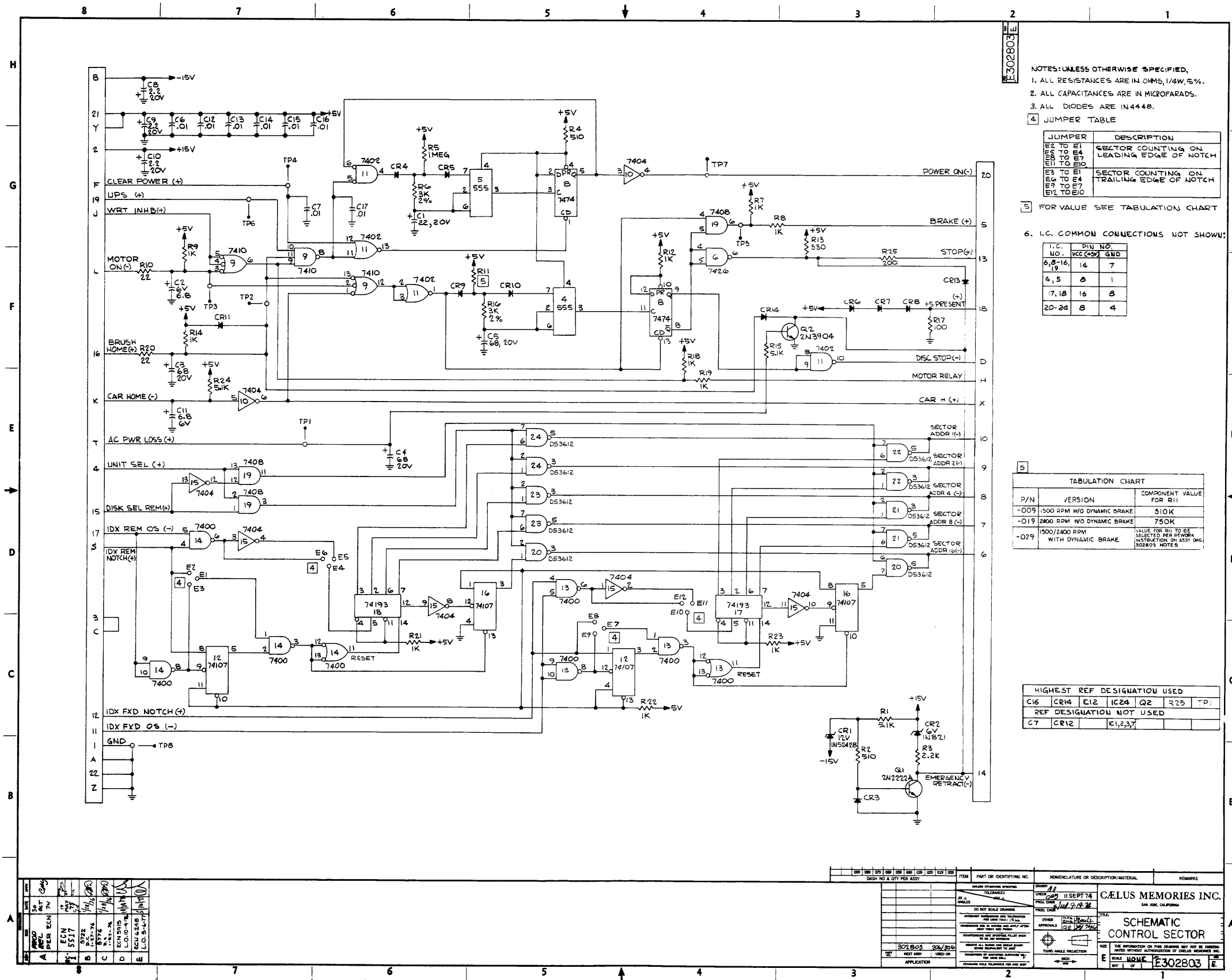
The output of the fixed disk sector counter is applied to IC's 20, 21, and 22. The output of the removable disk sector counter is applied to IC's 20, 23, and 24. The outputs of these gates are tied together as wired-Or-gates. The enabling signal that gates either the removable disk sector counter or the fixed disk sector counter to the output line is Disk Select Anded with Unit Select on IC 19. The operation of the fixed disk sector counter is identical to the removable disk sector counter, therefore, only the removable disk sector counter will be covered.

IC 18 is a 74193 up-down counter and is used as four stages of the sector counter. The fifth stage is the 74107, IC 16. The sector counter can count up to 32 sectors. The counter is reset with the first sector pulse following the index pulse which is defined as sector 0. The output of IC 14-11 is high with the first sector pulse following the index pulse and is tied to the master reset of the sector counter IC 18. IC 12 detects the index pulse and is referred to as the Index Detection flip flop. Detection of the index pulse is accomplished by Anding the removable notch one shot IDX REM NOTCH with the IDX REM OS. The time at which these two signals occur together is the index time. Once the Index Detection flip flop (IC 23) has been reset, each consecutive sector pulse counts the sector counter in an up direction by applying sector pulses to IC 18-5. The jumper pins E4, E5, and E6 determine whether sector counting is done on the leading or the trailing edge of the sector pulse. If jumper E4 to E5 is installed, counting will occur on the leading edge of the sector pulse. Figure 5-16 represents the sector counter outputs.



200-33

Figure 5-16. Sector Counter Outputs



NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%.
 2. ALL CAPACITANCES ARE IN MICROFARADS.
 3. ALL DIODES ARE IN 444B.

4. JUMPER TABLE

JUMPER NO.	DESCRIPTION
E2 TO E1	SECTOR COUNTING ON LEADING EDGE OF NOTCH
E3 TO E4	SECTOR COUNTING ON TRAILING EDGE OF NOTCH
E1 TO E0	
E3 TO E1	SECTOR COUNTING ON TRAILING EDGE OF NOTCH
E6 TO E4	
E9 TO E7	
E12 TO E10	

5. FOR VALUE SEE TABULATION CHART

6. I.C. COMMON CONNECTIONS NOT SHOWN:

I.C. NO.	VCC (+5V)	GND
6, 8-16, 19	14	7
4, 5	8	1
7, 18	16	8
20-24	8	4

5. TABULATION CHART

P/N	VERSION	COMPONENT VALUE FOR R11
-009	500 RPM W/O DYNAMIC BRAKE	510K
-019	2400 RPM W/O DYNAMIC BRAKE	750K
-029	1500/2400 RPM WITH DYNAMIC BRAKE	VALUE FOR R11 TO BE SELECTED PER PERFORM INSTRUCTION ON ASSY DNG. 302803 NOTES

HIGHEST REF DESIGNATION USED

REF DESIGNATION	VALUE
C16	CR4
E12	IC24
Q2	R25
TP1	
REF DESIGNATION NOT USED	
C7	CR12
	IC1,2,3,7

REV	DATE	BY	CHKD	APP	DESCRIPTION
1	11/16/74
2	11/16/74
3	11/16/74
4	11/16/74
5	11/16/74

302803	REV 5	DATE 11 SEPT 74	SCALE 1:1
PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION/MATERIAL	
CÆLUS MEMORIES INC.		SAN JOSE, CALIFORNIA	
SCHEMATIC CONTROL SECTOR		E 302803	

Figure 5-15. (Repeat) Control Sector Board Schematic

5.4.5 Control Sector Board (CSB) 48-Sector

The main purpose of the 48-sector Control Sector board is to generate the 48th sector pulse. (See Figure 5-17.) The cartridge used in conjunction with this board contains only 47 sector notches; the 48th needs to be generated electronically.

5.4.5.1 Power On

The Power On signal, IC 14-6, is used to initiate the head load sequence and is generated when the motor is on, Motor On (-), IC 12-3; the brushes are home, Brush Home (+), IC 12-11; the drive is up to speed, UPS (+), IC 12-10; and Clear Power (+), IC 13-12, is not true.

NOTE

Brush Home (+) is always positive for a 206 drive.

When the above conditions are true, a 10-second timer, IC 9-3, is started and 10 seconds later a clock is provided to set the up-to-speed flip flop, IC 11-5. With the up-to-speed flip flop set, Power On (-) is developed which will initiate the head load.

5.4.5.2 Stop (+)

Stop (+), IC 15-8, is the signal that causes the stop light to light on the front panel and energizes the door-locking solenoid. Stop (+) is generated when the motor is turned off, Motor On (-), IC 12-2; the carriage is at home, CAR Home (+), IC 14-1; and the Brush Home (+) signal is positive, IC 12-13. These conditions start the 555 timer IC 8-3 and 60 seconds later, when IC 8 times out, it will set the stop flip flop, IC 11-9.

5.4.5.3 Emergency Retract (-)

The Emergency Retract signal at zone B2 of Figure 5-17 is used for two purposes; one, to cause the heads to retract in case of a power supply failure and two, to prohibit the heads from loading in case of a servo board not being properly installed. Power supply failure is accomplished with the voltage divider network of Q1. A servo board improperly installed is detected by routing the Emergency Retract signal through the Temperature Compensation board, Drive Control board, Servo Logic board, Servo Analog board, and the I/O board.

5.4.5.4 Index and Sector Development

Index and sector detection for the removable disk is accomplished by IC's 3, 4, 6, and 7 for the removable disk and IC's 1, 2, 5,

and 7 for the fixed disk. The theory of both circuits is the same; theory for the removable will be covered. (See Figure 5-17.)

INDEX REM NOTCH, a 720-nanosecond pulse, which occurs for every sector or index notch detected, fires IC 4-10 for 4.6 microseconds. When IC 4-10 times out, IC 4-6 is fired for 720 microseconds, which establishes a window for the index slot. The 4.6-microsecond one shot, IC 4-10, firing during this period of time will be detected as an index pulse on IC 6-3. The window, IC 4-6, timing out prior to the next notch detected will be detected as a sector pulse on IC 6-6.

Every index pulse output from IC 6-3 fires IC 3-6 for 210 microseconds. IC 3-6 establishes the delay between the index pulse and the 48th sector pulse. When IC 3-6 times out, IC 3-9 is triggered for 4.6 microseconds which Ors the 48th sector pulse on IC 6-10 with the other 47.

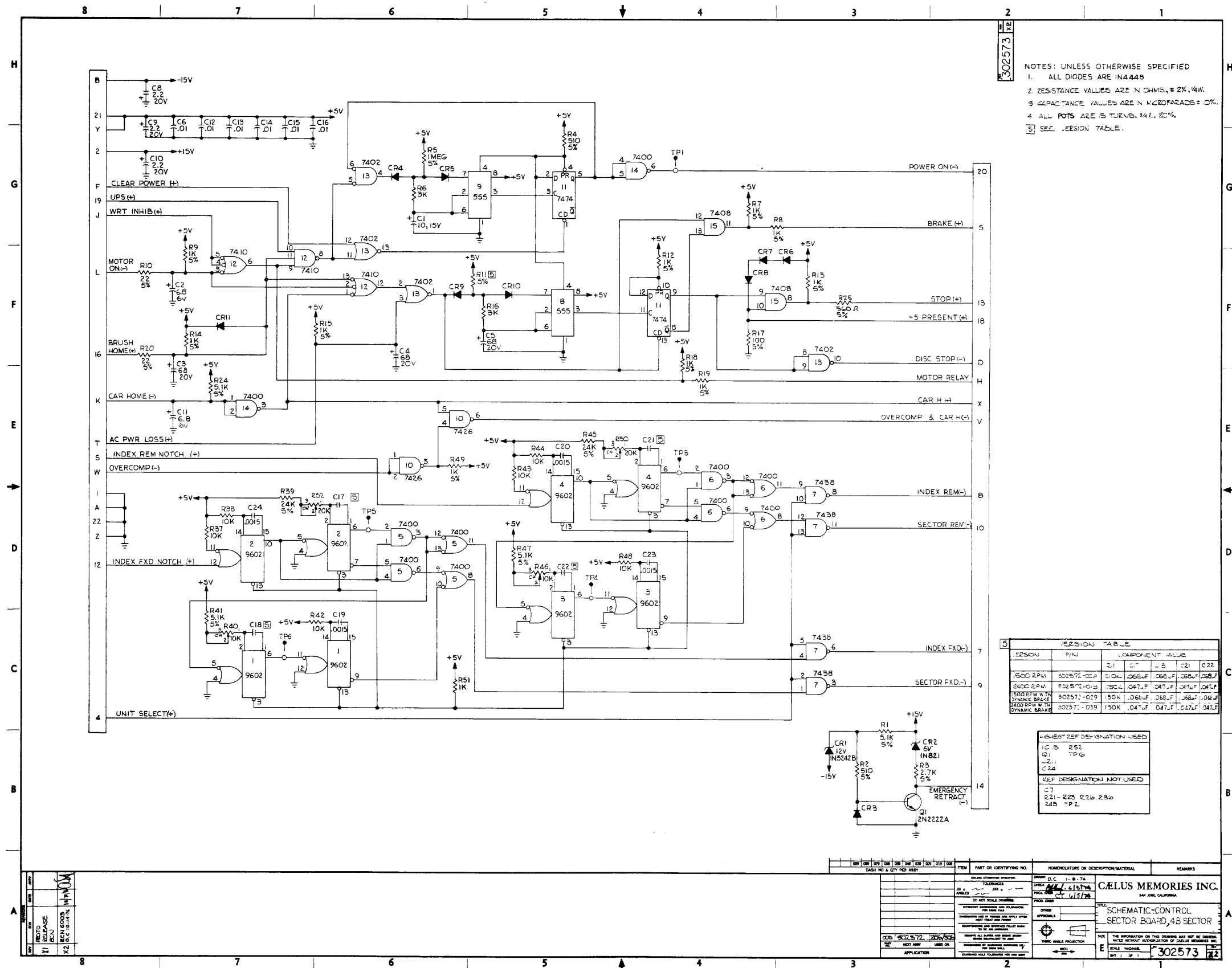


Figure 5-17. Control Sector Board 48-Sector Schematic

5.4.6 Servo Logic Board (SLB)

The major function of the Servo Logic board is to store the carriage track address and perform the arithmetic necessary to supply a servo drive signal to the Servo Analog board. (See Figure 5-18). The track address is stored in IC's 16, 17, and 18: the Carriage Address Register (CAR). The track address is stored in the CAR in one's complement form. With a track address of zero, all output pins from the CAR are true.

5.4.6.1 Track Counting Circuit

The track counting circuit consists of IC's 1, 2, 5 and 11 located at coordinates G7 in Figure 5-18. The function of the counting circuit is to develop count up or count down pulses for the carriage address register as each respective track is crossed.

Whenever the carriage is moving the detent pulse is developed which is high once for each track crossed. The track counting circuit develops either count-up pulses on the output of IC 11-8 or count-down pulses on the output of IC 11-11. When moving forward IC 22-6 is at a high level enabling count up pulses from IC 11-8 which counts the cylinder address register down by one for each pulse developed.

The Carriage Address Register on the 206 drive is maintained in one's complement form. Count-down pulses are developed when moving in a forward direction; count-up pulses are developed when the carriage is moving in a reverse direction.

5.4.6.2 Carriage Address Register

Count-up and count-down pulses generated by the track counting circuit are applied to the Carriage Address Register, IC's 16, 17, and 18 located at coordinates D4 in Figure 5-18. The function of the Carriage Address Register is to store the one's complement of the carriage address. The carriage moving forward (toward the disk center) generates pulses at IC 11-8. The carriage moving in the reverse direction (away from the disk center) generates pulses at IC 11-11.

IC 17 contains the least significant stage of the Carriage Address Register and IC 18 the most significant. Outputs of the Carriage Address Register are on pins 3, 2, 6, and 7. Count-up and count-down pulses count the Carriage Address Register in a direction to maintain current position address. The most significant stage of the CAR (IC 18) is counted down by the count-down pulses applied from pin 13 of the stage IC 16. Pin 12 of IC 16 is applied to the count-up pulse input (pin 5) of IC 18. Since the Carriage Address Register is maintained in one's complement form, a carriage address 0 would be represented in the CAR with all output

pins high. IC's 20, 21 and 22 add the Carriage Address Register to the New Address Register from the I/O board. Outputs from the CAR are on pins 3, 2, 6 and 7.

5.4.6.3 Adder IC's 20, 21 and 22

The outputs of the New Address Register are applied to the input of the adder chips IC's 20, 21 and 22. The adder chips add the New Address Register to the Carriage Address Register and supply a sum output on pins 9, 6, 2 and 15 of all stages of the adder. These output lines from the adder represent the sum of the Carriage Address Register and the New Address Register, i.e., one's complement of present carriage position plus new address. The resultant sum addresses the PROM's (IC's 12 and 13).

The PROM outputs are open collector. The outputs produce current through the D to A converter formed by R14 through R21. When a PROM output to its resistor-diode chain is low, the positive current from the resistor flows into the PROM output, the series diode is cut off because of insufficient forward voltage, and current flow from the resistor, via the diode to pin 17, is inhibited. After processing on the Servo Analog board, the output from pin 17 becomes the servo error signal. Tables of output currents against input codes for the two PROM's are contained in Tables 5-1 and 5-2. If the NAR and CAR codings for various carriage address and new address values are followed through the logic, it will be found that the output current from pin 17 is an approximately linear function of the difference between the current position of the carriage and the desired position of the carriage, i.e., a simple proportional error signal for any track delta of 128 or less (for separations of 128 or more tracks) the servo error signal remains constant. This is performed by disabling the PROM's (i.e., a high on IC 14-3) when there is no overflow from the most significant bit of the adder (i.e., a low on IC 22-15) or when there is no 512 bit from the adder (i.e., a low on IC 22-2). When the PROM's are disabled by IC (14-3) high, resistors R14 through R21 are enabled, giving the maximum error current at pin 17.

When the drive receives a Seek command, the new address appears on the NAR lines. The new address is added to the one's complement of the track address (CAR). As an example, assume a track address of 12 (decimal) and a seek to track 10 (decimal).

EXAMPLE: Address in Binary: NAR 000 001 010 (10)
Address in Binary: CAR 111 110 011 (one's complement of 12)
Sum Out of Adder

EXAMPLE: Addresses in Binary: NAR 000 001 010 (10)
Addresses in Binary: CAR 111 110 011 (one's complement of 12)
Sum Out of Adder: 111 111 101

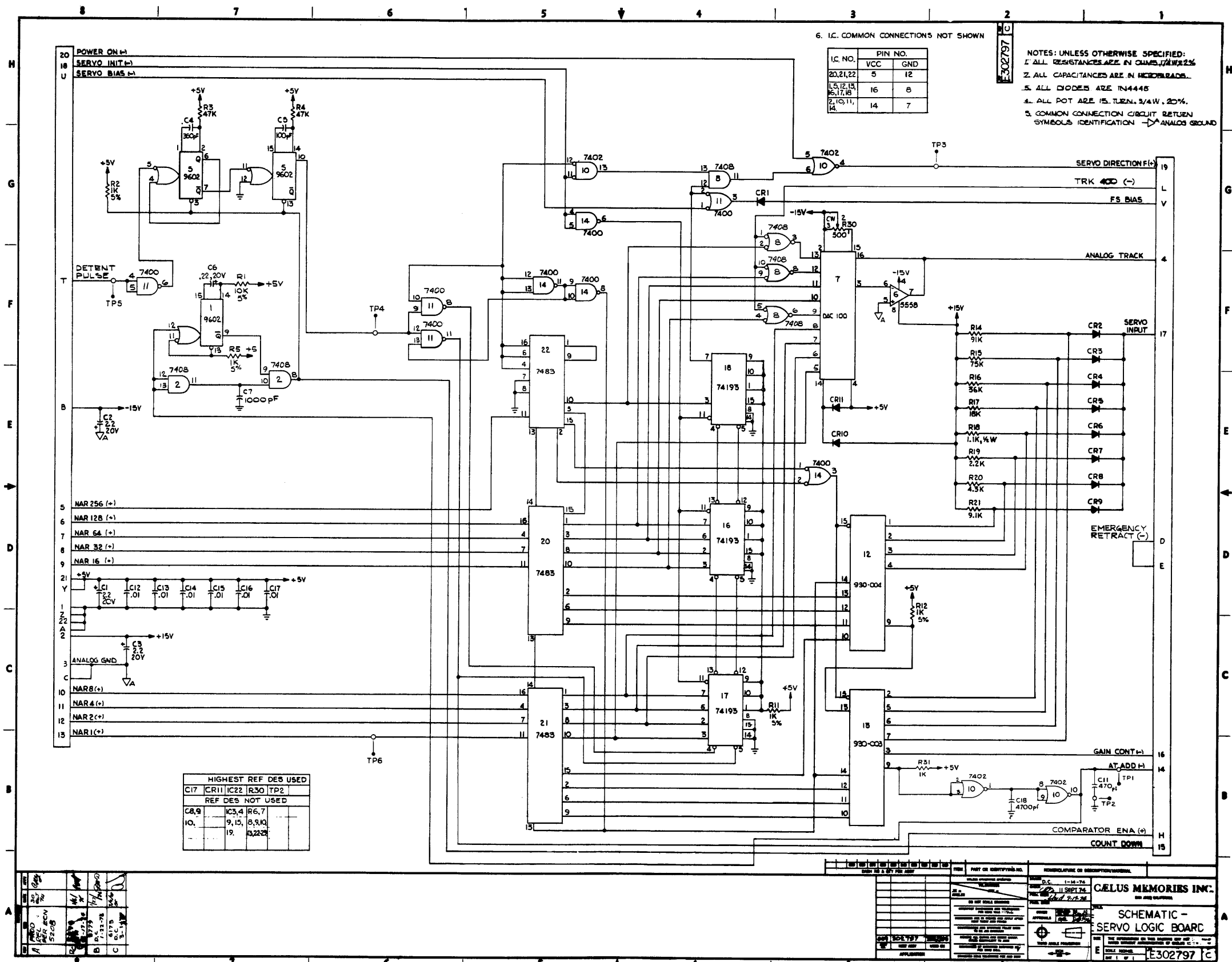


Figure 5-18. Servo Logic Board Schematic

Table 5-1. Output Current Versus Input Codes (IC 13)

IC 13 (930-003)							IC 13 (930-003)						
Decimal Input Value	Input Code					D to A Network Current, ma	Decimal Input Value	Input Code					D to A Network Current, ma
	14	13	12	11	10			14	13	12	11	10	
0	0	0	0	0	0	1.449	17	1	0	0	0	1	.165
1	0	0	0	0	1	1.249	18	1	0	0	1	0	.416
2	0	0	0	1	0	1.033	19	1	0	0	1	1	.616
3	0	0	0	1	1	.833	20	1	0	1	0	0	.833
4	0	0	1	0	0	.616	21	1	0	1	0	1	1.033
5	0	0	1	0	1	.416	22	1	0	1	1	0	1.249
6	0	0	1	1	0	.165	23	1	0	1	1	1	1.449
7	0	0	1	1	1	0							
8	0	1	0	0	0	1.449	24	1	1	0	0	0	0
9	0	1	0	0	1	1.249	25	1	1	0	0	1	.2
10	0	1	0	1	0	1.033	26	1	1	0	1	0	.416
11	0	1	0	1	1	.833	27	1	1	0	1	1	.616
12	0	1	1	0	0	.616	28	1	1	1	0	0	.833
13	0	1	1	0	1	.416	29	1	1	1	0	1	1.033
14	0	1	1	1	0	.2	30	1	1	1	1	0	1.249
15	0	1	1	1	1	0	31	1	1	1	1	1	1.449
16	1	0	0	0	0	0							

Note: Pin 13 is permanently high (see schematic), hence only the outlined portion of the table is valid. Pin 14 is high for forward motion and low for reverse motion.

To determine the total current from pin 17:

- Determine the Input address on each PROM as presented to pins 10 through 14.
- Determine the current generated by each PROM into the D to A network R14 through R21 (from the Tables).
- Total current from pin 17 is the sum of the current from both PROM's, IC's 12 and 13.

Table 5-2. Output Current Versus Input Codes (IC 12)

IC 12 (930-004)							IC 12 (930-004)						
Input Code					D to A Network Current, ma	Input Code					D to A Network Current, ma		
14	13	12	11	10		14	13	12	11	10			
0	0	0	0	0	25.534	1	0	0	0	0	0		
0	0	0	0	1	23.934	1	0	0	0	1	1.6		
0	0	0	1	0	22.054	1	0	0	1	0	3.48		
0	0	0	1	1	20.454	1	0	0	1	1	5.08		
0	0	1	0	0	18.716	1	0	1	0	0	6.818		
0	0	1	0	1	17.116	1	0	1	0	1	8.418		
0	0	1	1	0	15.236	1	0	1	1	0	10.298		
0	0	1	1	1	13.636	1	0	1	1	1	11.898		
0	1	0	0	0	11.898	1	1	0	0	0	13.636		
0	1	0	0	1	10.298	1	1	0	0	1	15.236		
0	1	0	1	0	8.418	1	1	0	1	0	17.116		
0	1	0	1	1	6.818	1	1	0	1	1	18.716		
0	1	1	0	0	5.08	1	1	1	0	0	20.454		
0	1	1	0	1	3.48	1	1	1	0	1	22.054		
0	1	1	1	0	1.6	1	1	1	1	0	23.934		
0	1	1	1	1	0	1	1	1	1	1	25.534		

Note: Pin 14 is high for forward motion and low for reverse motion.

To determine the total current from pin 17:

- Determine the Input address on each PROM as presented to pins 10 through 14.
- Determine the current generated by each PROM into the D to A network R14 through R21 (from the Tables).
- Total current from pin 17 is the sum of the current from both PROM's, IC's 12 and 13.

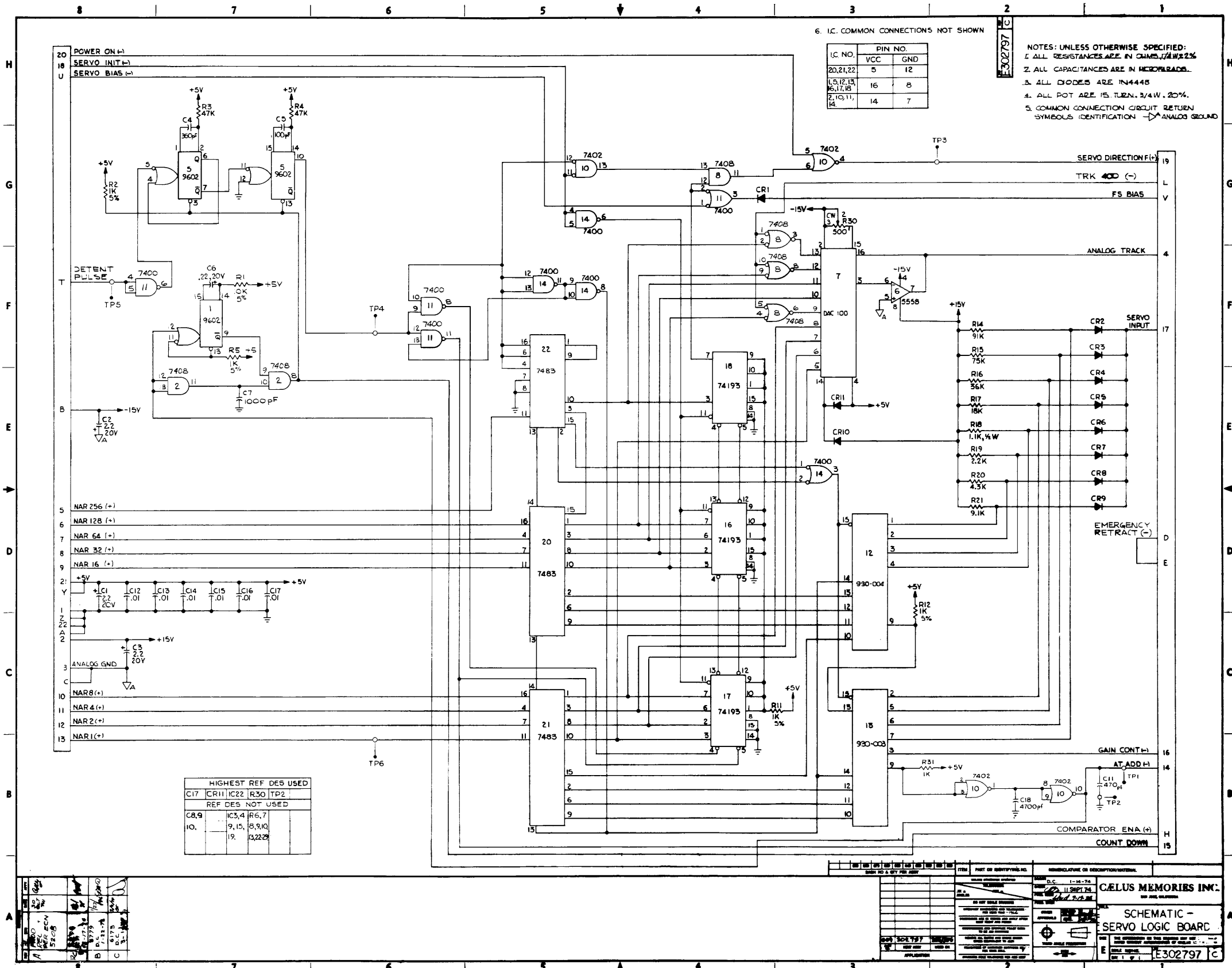


Figure 5-18. (Repeat) Servo Logic Board Schematic

In the example on page 5-34, there is no carry from the addition, and IC 22-6 is low, causing IC 10-4 to be low. IC 10-4 controls the polarity of drive to the positioner motor. A high causes forward drive and a low reverse drive.

A Seek to the outer diameter results in no carry; a Seek to the inner diameter results in a carry at IC 22-6.

5.4.6.4 DAC 100

The DAC 100 (IC 7) sends an analog representation of track position to be used on the Temperature Compensation board. At track 0 the pin 16 output of the DAC 100 should be 0 volts; at track rpp the output should be +7 volts. This is adjustable with R30.

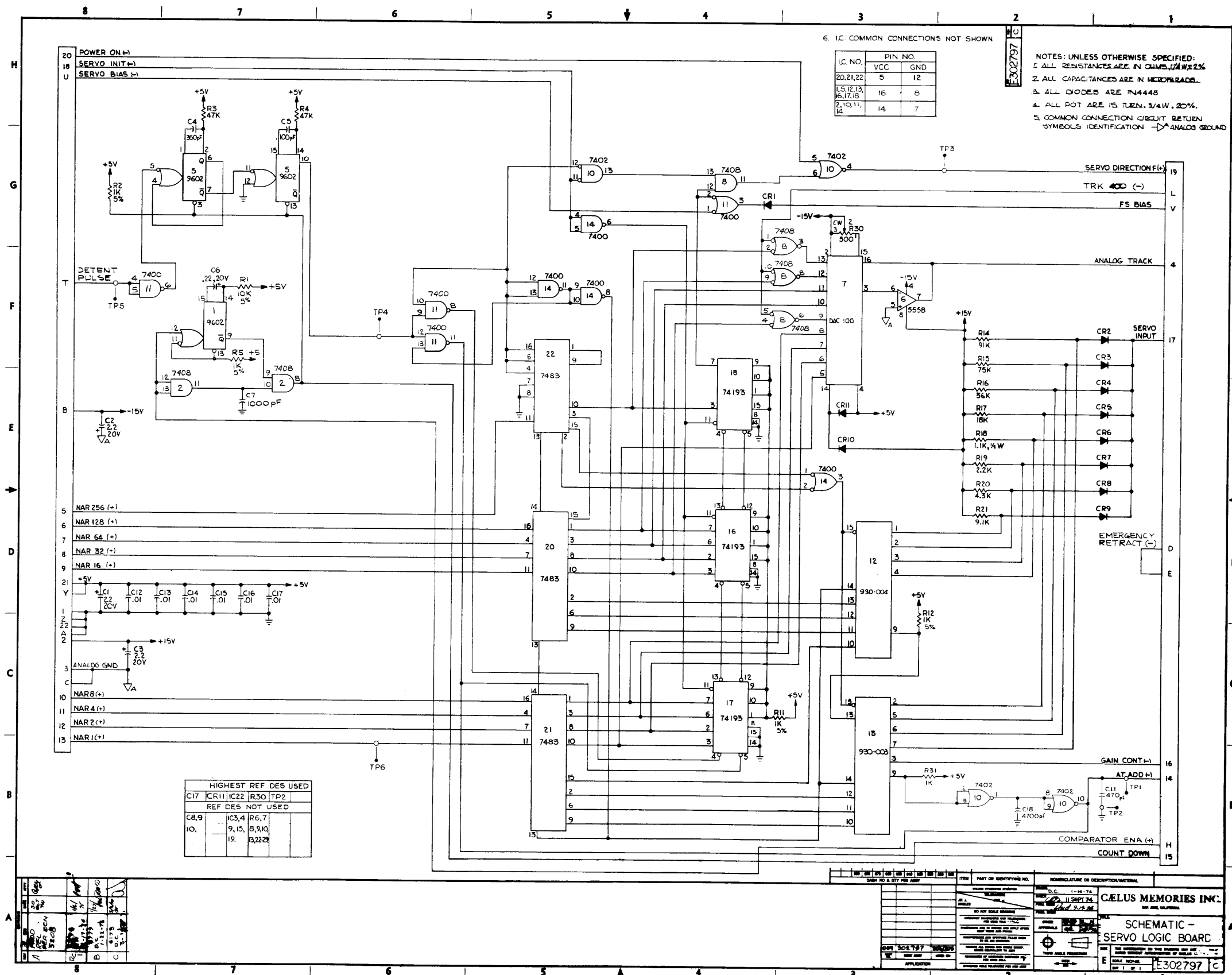


Figure 5-18. (Repeat) Servo Logic Board Schematic

5.4.7 Servo Analog Board (SAB)

The Servo Analog board contains the majority of the electronics for the servo loops. There are two loops; the optical detent or fine servo loop and the coarse servo loop. Injection of thermal compensation is accomplished in the fine servo loop. (See Figure 5-9.)

5.4.7.1 Coarse Servo Loop

The head load bias is injected at pin V, zone D8. The head load bias develops the servo amp signal at IC 6-1 during the head load sequence. During drive operation, IC 6-1 is a positive voltage to move the carriage in a forward direction and negative to move the carriage in a reverse direction.

The position error signal is injected at pin 17, zone D8. The purpose of IC 5-7 on the Servo Analog board and IC 9-1 and associated components is to generate a function which is the square root of the analog position. This gives an optimum velocity profile. The square root function is achieved by using nonlinear feedback from diodes CR12 through CR17. The output of IC 9-1 is always a positive voltage. The output of IC 9-1 applied to IC 5-2 is then either inverted or not inverted on IC 5-1 in relation to the servo direction signal on IC 8-10. IC 8-8 is positive whenever a reverse seek is being accomplished. This direction level turns on Q8 whenever the direction of movement is toward the outer diameter. Q8 turned on turns IC 5-1 into an inverting amplifier. The output of IC 5-1 is positive for a forward move and negative for a reverse move.

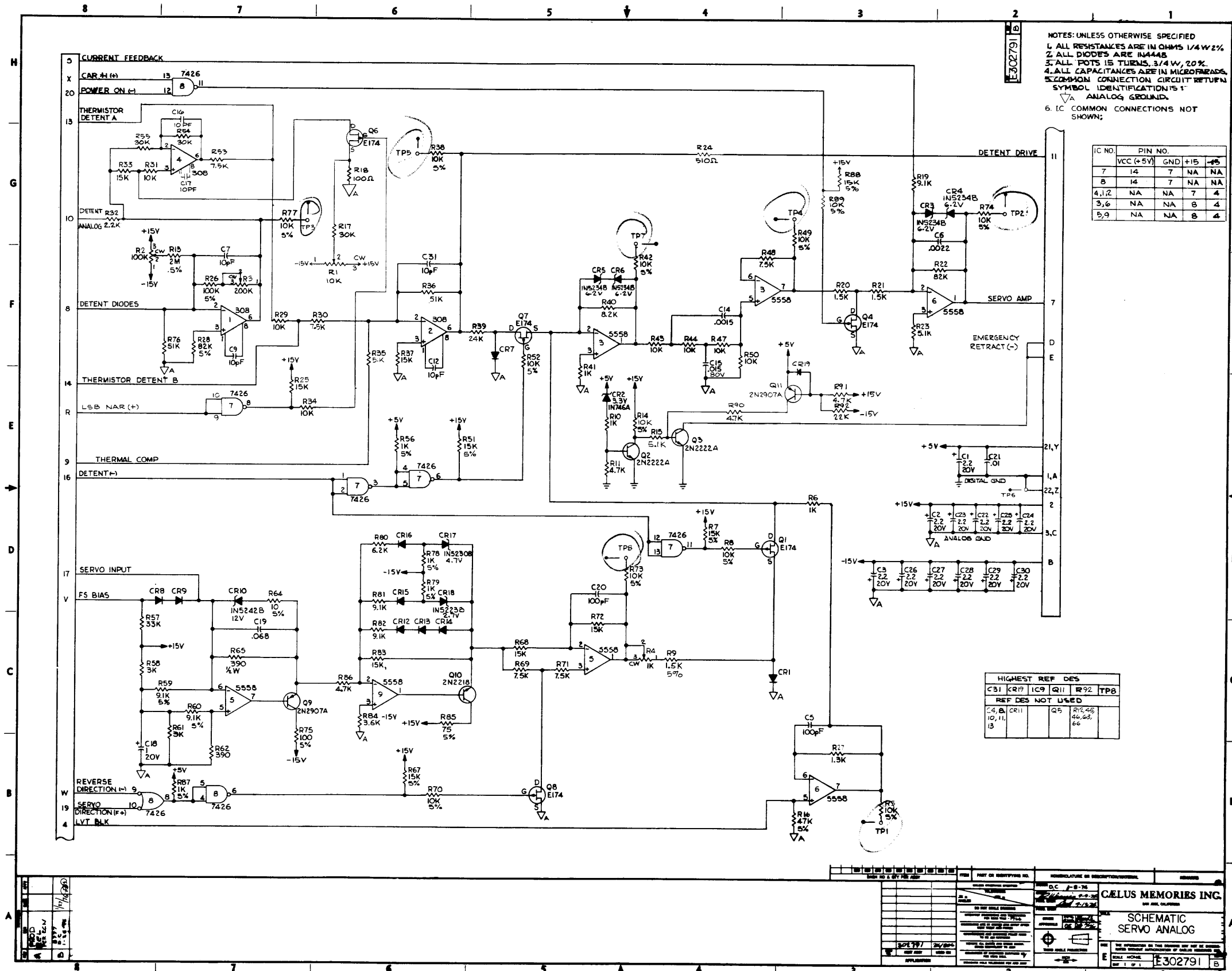
The output of IC 5-1 is applied to IC 3-2 whenever Q1 is turned on. Q1 is turned off when the signal Detent (+) is true, i.e., IC 7-11 is high. Detent (+) is true (high) whenever the sum of CAR plus NAR is 777 (octal) and false (low) whenever a difference does exist. The output of IC 3-1 is a positive voltage for reverse movement and a negative voltage for forward movement of the carriage. The next stage in the servo amplifier chain, IC 3-7, is a non-inverting notch filter with a gain of approximately 25. As long as the voltage sense network of Q2 and Q3 is not detecting loss of either +5 or +15 volts, the output of IC 3-7 is applied to IC 6-2. IC 6-1 goes directly to the first stage of the power amplifier on the PCM board.

The output of the velocity transducer, IC 6-7, at zone B3 is summed with the servo signal into the input of unity gain buffer amplifier IC 6-1. The servo signal can be either the coarse error signal from the PROM's in the SLB, out of IC 5-1, switched in by FET Q1, or the fine detent error signal from the photodiodes, out of IC 2-6, switched in by FET Q7. The velocity transducer develops an output voltage that is directly proportional to the speed of

the carriage. IC 6-7 is an impedance matching stage whose output is negative for a forward seek and positive for reverse. The velocity transducer provides velocity damping for the carriage.

5.4.7.2 Fine Servo Loop

The function of the Fine Servo Loop is to maintain the heads over a given track position. When the heads are positioned over the required track, Detent (-) on IC 7-1 is low, turning Q1 off. The coarse servo is disabled and Q7 is turned on, enabling the output of the fine servo IC's 2-6 to 3-2. The sensor for the optical loop is a pair of solar cells in an optical configuration which gives an output which varies sinusoidally with carriage position. ($\frac{1}{2}$ the period is from one track to the next track.) The positioning then occurs at every crossover point. The solar cell's output voltage is amplified by IC 1-6; R3 is a gain adjustment and R2 adjusts centering. The current output of IC 1-6 is amplified by IC 4-6 which is either an inverting or non-inverting amplifier in relation with the LSB input on IC 7-9. Whenever the LSB is true it indicates a seek to an ODD track. IC 4-6 is an inverting amplifier. This circuitry is necessary to enable detenting on the proper slope. The current output of IC 4-6 is summed with temperature compensation at IC 2-2. This composite positioning signal on the output of IC 2-6 maintains the heads on track regardless of the amount of track shift because of temperature variations on the removable media or mechanics.



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTANCES ARE IN OHMS 1/4W 2%
 2. ALL DIODES ARE 1N4448
 3. ALL POTS 15 TURNS, 3/4W, 20%
 4. ALL CAPACITANCES ARE IN MICROSECONDS
 5. COMMON CONNECTION CIRCUIT RETURN SYMBOL IDENTIFICATION: ∇ ANALOG GROUND
 6. IC COMMON CONNECTIONS NOT SHOWN

IC NO.	PIN NO.	VCC (+5V)	GND	+15	-15
7	14	7	NA	NA	NA
8	14	7	NA	NA	NA
4,1,2	NA	NA	7	4	4
3,6	NA	NA	8	4	4
5,9	NA	NA	8	4	4

HIGHEST REF DES					
C31	CR19	IC9	Q11	R92	TP8
REF DES NOT USED					
C4, B, 10, 11, 13	CR11	Q5	R16, 45, 46, 63, 66		

PART OR IDENTIFYING NO. MANUFACTURER'S PART NO. QUANTITY DATE BY	D.C. P-8-78 REV. 1-1-78 DATE BY CHECKED BY DATE	CALUS MEMORIES INC. 1000 N. GARDEN GAITHERSBURG, MD 20878 (301) 251-2500
SCHEMATIC SERVO ANALOG		E302791

Figure 5-19. Servo Analog Schematic

5.4.8 Temperature Compensation Board (TCB)

The primary purpose of the Temperature Compensation board is to generate a signal which is added to the detent loop. (See Figure 5-21.) This signal compensates for the relative head-to-disk movement which occurs from the thermal expansion of the materials used. A drive, stabilized at an ambient temperature, which gives a disk pack temperature of 22°C (or 72°F), can be considered as a reference; no thermal compensation at any track position is required for this condition. The casting is typically 12°F hotter than the removable disk, and so this means a casting temperature of 84°F. All packs can be considered (theoretically) as having been written with a uniform disk temperature of 22°C or 72°F.

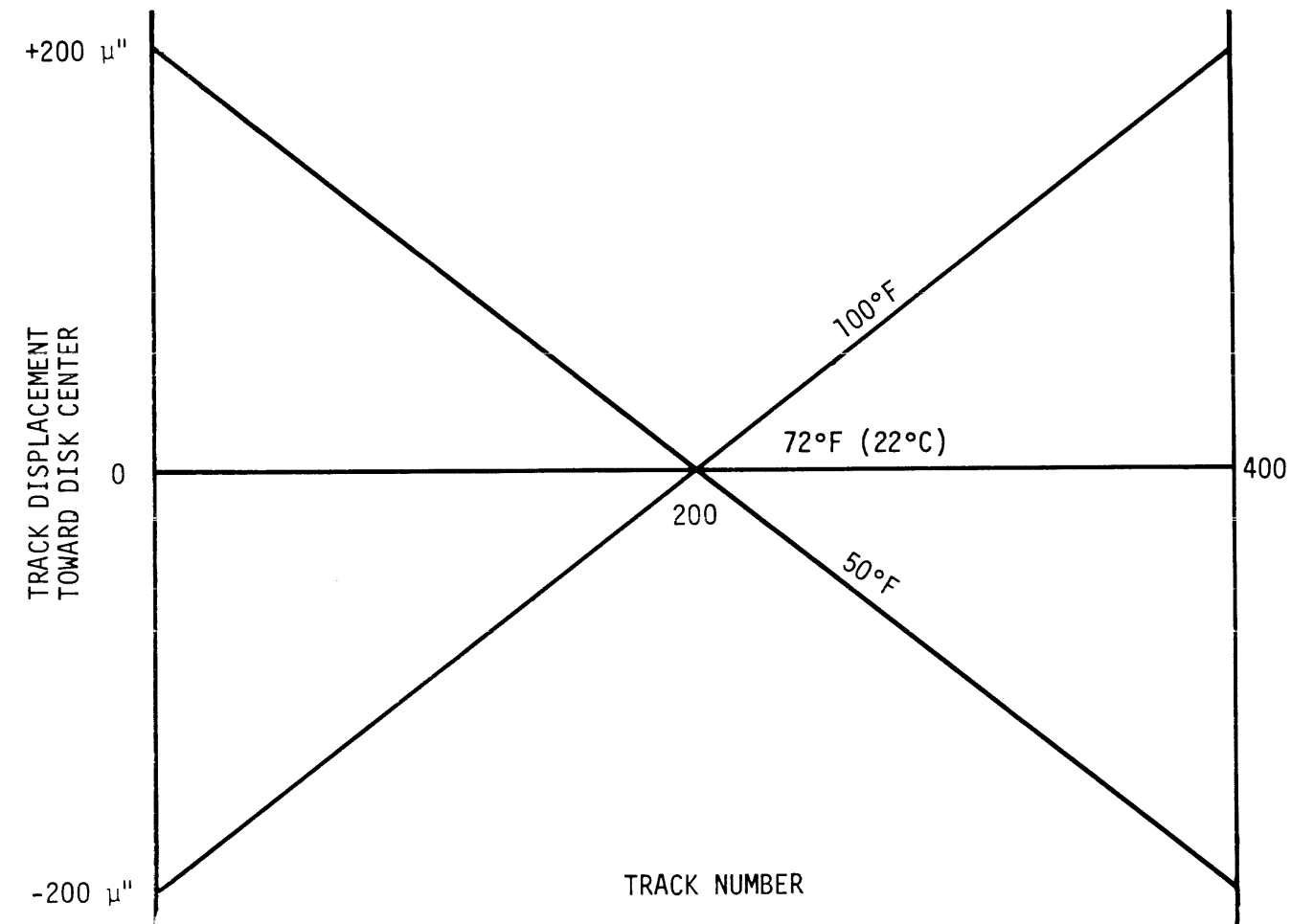
The central track, track 200, is also a reference point; no thermal compensation for track position is required at track 200 irrespective of casting temperature.

At track 400 (disk center) as the temperature of the casting rises, the track moves (effectively) toward the spindle away from the voice coil. At track 0 (disk outer edge) as the temperature of the casting rises, the track moves (effectively) away from the spindle toward the voice coil. As already stated, track 200 does not move as the temperature of the casting (and therefore the disk) changes. Hence, we have the maximum expansion rate at tracks 0 and 400, zero expansion at track 200, and expansion in proportion to the separation from track 200 at points in between.

This is illustrated in Figure 5-20, which is a graph of track displacement in microinches against track number for the two extremes of operating temperature (50°F to 100°F or 10°C to 38°C), with the zero displacement 72°F (22°C) plot shown for reference.

The displacements shown correspond to expansion rates of 8.6 microinches per degree Fahrenheit at tracks 0 and 400, and proportionally less toward track 200. This means that as the temperature rises from 72°F to 100°F, track 400 effectively moves 197.8 microinches toward the spindle.

Changes in temperature differential between the disk and the casting also cause track displacements. As the fixed disk operates in what is effectively a cavity in the casting, it remains at casting temperature and requires no compensation for a temperature differential. However, a removable pack can be inserted directly from storage at a different temperature, and therefore requires compensation for temperature differential change between it and the casting as it warms up. As the removable disk gets hotter (the casting staying at the same temperature), all tracks move effectively away from the disk center.



NOTE: TRACK DISPLACEMENT IN MICROINCHES VERSUS TRACK NUMBER FOR NORMAL (72°F), MAXIMUM (100°F), AND MINIMUM (50°F) DISK OPERATING TEMPERATURES.

200-34

Figure 5-20. Track Displacement Versus Track Number

Three thermistors are used: one measures casting temperature, and is connected between pins 15 and 16; the other two thermistors compare casting temperature to removable disk exhaust-air temperature in a bridge circuit. The casting thermistor of this pair is connected between pins X and W, and the pack-air thermistor is connected between pins X and V.

The casting thermistor between pins 15 and 16 eventually produces a signal called DC Thermal Compensation at pin IC 3-1; this compensates for overall machine temperature changes.

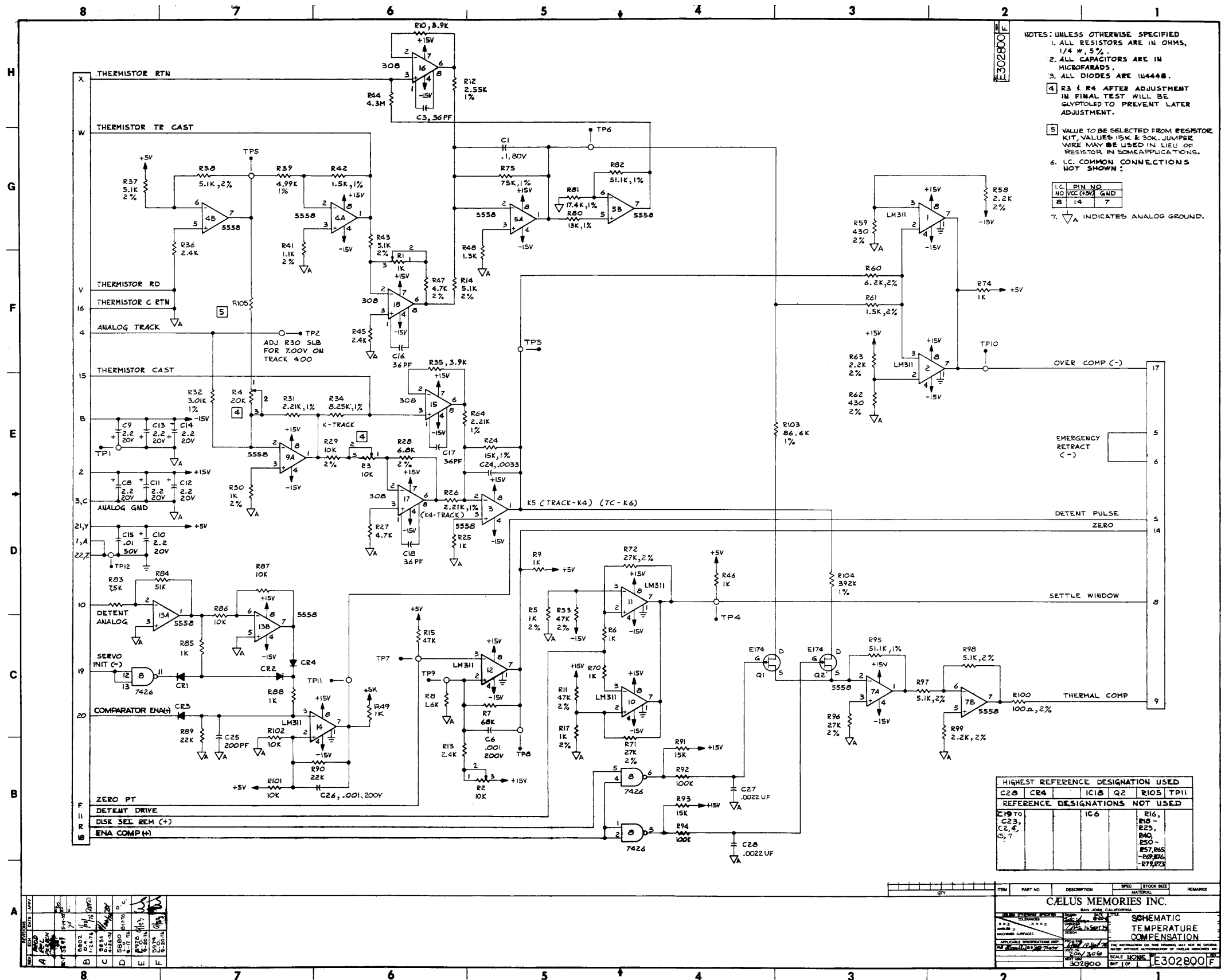


Figure 5-21. Temperature Compensation Board Schematic

The bridge-connected thermistors between pins V, X, and W eventually produce a signal called Transient Thermal Compensation on IC 5A-1, which compensates for temperature differences between the removable disk and the casting. This transient compensation is only switched in when the removable disk is selected.

5.4.8.1 DC Thermal Compensation

The DC Thermal Compensation voltage has to be both proportional to separation from track 200 and proportional to difference from 84°F, casting temperature; this means that:

- a. The output voltage must be zero at track 200 for all temperatures, and proportional to track separation from track 200. This is achieved by driving the thermistor with a current proportional to separation from track 200.
- b. The output voltage must be zero at 84°F casting temperature for all track numbers; i.e., the standing voltage across the thermistor at 84°F must be balanced out by subtraction from the compensation voltage, since we only want temperature change from 84°F to show as compensation.

This could not be achieved by a simple offset voltage because the current through the thermistor is varied from track to track.

The same thermistor type is used in all three positions; it has a resistance of 10k-ohms at 77°F; Table 5-3 is a list of resistance values against temperature for the thermistor used.

The input to pin 4, Analog Track, is a voltage proportional to track number, derived from D to A connector IC 7 in the Servo Logic board. The voltage is 0 volts at track 0 and +7V at track 400. The Analog Track voltage is fed via R32 to the input of an inverting amplifier, IC 9A-2.

A -5V reference is obtained by inverting the +5V supply voltage at IC 4B-7. Current from this negative source is summed (via potentiometer R4) with current from the Analog Track signal at amplifier input IC 9A-2. The output of the amplifier at IC 9A-1, which has a gain of 0.7, can therefore be offset by potentiometer R4 to be zero at track 200.

The casting thermistor, across pins 15 and 16, is driven (in series with resistor R34) by the output voltage from IC 9A-1, which is a voltage proportional to the separation of the track being used from track 200 (e.g., 0 volts at track 200, +2.5 volts at track 0, and -2.5 volts at track 400).

Table 5-3. Thermistor Values

Temperature °C	Resistance	Temperature °C	Resistance
0	32,650	26	9,573.0
1	31,030	27	9,167.0
2	29,500	28	8,777.0
3	28,050	29	8,407.0
4	26,690	30	8,057.0
5	25,390	31	7,723.0
6	24,170	32	7,403.0
7	23,010	33	7,097.0
8	21,920	34	6,807.0
9	20,830	35	6,530.0
10	19,900	36	6,267.0
11	18,970	37	6,017.0
12	18,090	38	5,777.0
13	17,250	39	5,547.0
14	16,460	40	5,327.0
15	15,710	41	5,117.0
16	15,000	42	4,917.0
17	14,320	43	4,727.0
18	13,680	44	4,543.0
19	13,070	45	4,370.0
20	12,490	46	4,200.0
21	11,940	47	4,040.0
22	11,420	48	3,890.0
23	10,920	49	3,743.0
24	10,450	50	3,603.0
25	10,000		

The voltage across the thermistor is therefore determined by:

- a. the track position, and
- b. the temperature of the casting.

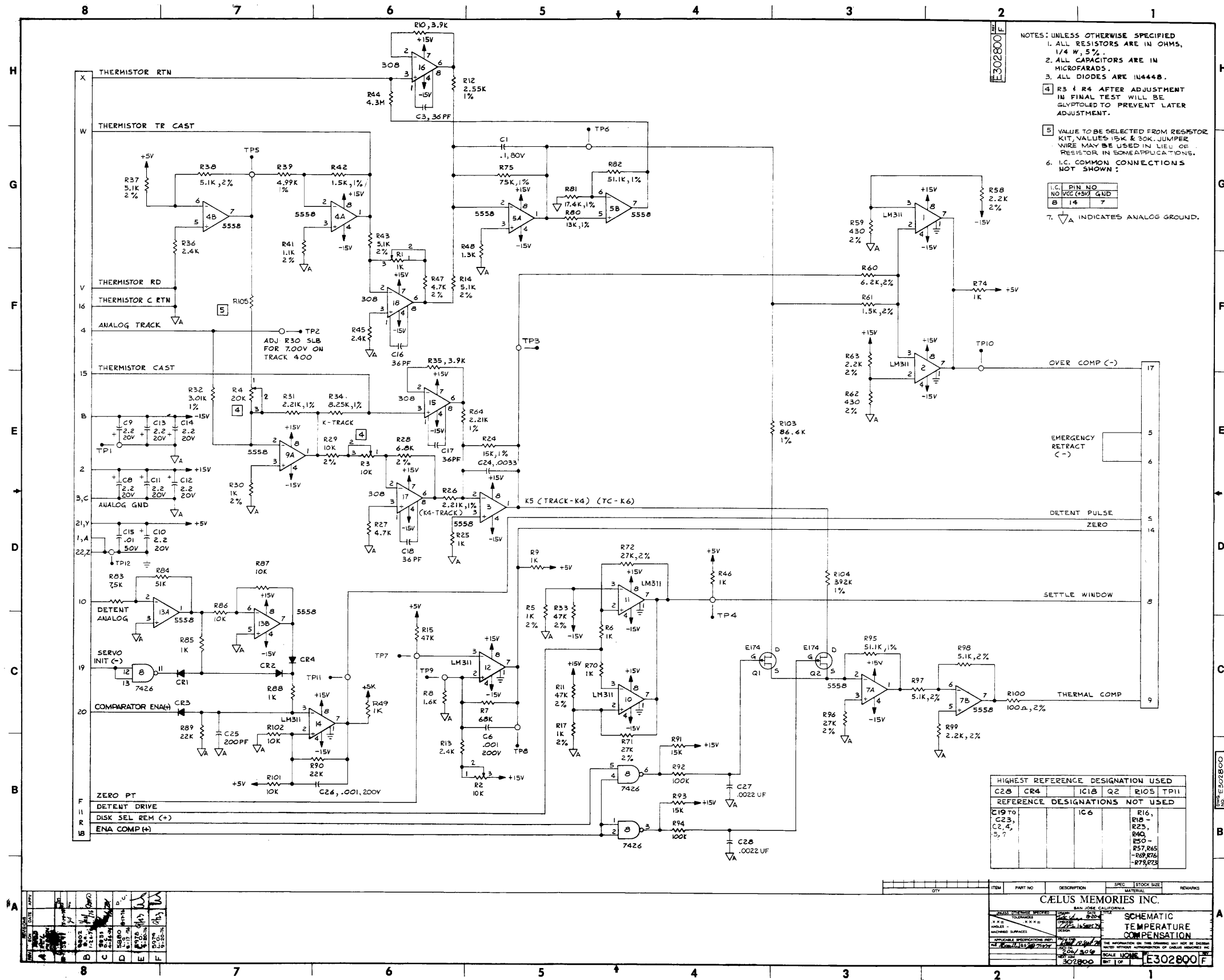


Figure 5-21. (Repeat) Temperature Compensation Board Schematic

Since the reference temperature is 84°F casting temperature, the DC compensation must be zero for all tracks at a casting temperature of 84°F. The inverted, track-proportional voltage is derived at IC 17-6 and scaled down by a factor of approximately 0.5 (since the volts across the thermistor are also scaled down by the potential divider formed by R34 thermistor). The buffered thermistor voltage and the correctly scaled, inverted, track-proportional voltage are summed at input IC 3-2. The output, IC 3-1, goes to R104 as DC Thermal Compensation.

Some typical examples of operating voltages for the DC Thermal Compensation at various track positions and temperatures are given below:

- a. At 84°F casting temperature
 1. At track 200, IC's 9-1, 15-3, 15-6, 17-6 and 3-1 should all be near zero volts.
 2. At track 400, IC 9-1 is approximately +2.5 volts, IC's 15-3 and 15-6 are approximately +1.4 volts, IC 17-6 is approximately -1.4 volts, and IC 3-1 is near zero volts.
- b. At 100°F (38°C)
 1. At track 200, IC's 9-1, 15-3, 15-6, 17-6, and 3-1 are all near zero volts.
 2. At track 400, IC 9-1 is approximately +2.5 volts, IC 17-6 is approximately -1.4 volts, IC 15-6 is approximately +1.0 volt, and IC 3-1 is approximately +2.5 volts.
 3. At track zero, IC 9-1 is approximately -2.5 volts, IC 17-6 is approximately +1.4 volts, IC 15-6 is approximately -1.0 volt, and IC 3-1 is approximately -2.5 volts.

This description of the DC Thermal Compensation has referred continually to track 200 as being the zero-expansion track, for clarity in explanation. In practice, the zero-expansion track, is not always track 200, but varies from machine to machine. This variation is accommodated by adjusting potentiometers R3 and R4. The adjustment is performed by changing the machine temperature and realigning the heads with R3 and R4 to di-bit written tracks on an alignment pack.

5.4.8.2 Transient Thermal Compensation

The Transient Thermal Compensation has to be proportional to the temperature difference between the casting and the exhaust air from the removable disk. This means that the output must be zero for all cases where the casting and exhaust air are of the same temperature.

The transient compensation is achieved by driving the casting and air thermistors in series from a reference voltage, the thermistors acting as a potential divider, and taking the voltage at the junction. This voltage will always be half the reference voltage for equal casting and air temperatures. A voltage equal to one half the driving reference voltage is then subtracted from the voltage at the junction (this gives a zero output for all equal temperatures regardless of what the temperature actually is), and suitably amplified and buffered, becomes the transient compensation output on pin 10.

The +1.5V reference voltage is generated at IC 4A-1 from the -5V at IC 4B-7, the inverting amplifier IC 4A-1 having a gain of 0.3. The reference voltage is applied to the casting thermistor at pin W. The casting thermistor connects to the air thermistor at pin X, and the air thermistor is grounded at pin V.

The junction potential from pin X is fed to the noninverting buffer amplifier input IC 16-3. The output of the unity gain buffer amplifier at IC 16-6 is fed via R12 to the inverting input, IC 5A-2, of amplifier IC 5A-1.

The +1.5V reference voltage is fed to inverting amplifier IC 18-6 which has a gain that can be set to unity. The output from IC 18-6 is taken via R14 to IC 5A-2, where it is summed with the buffered voltage from the potential divider formed by the two thermistors. This junction, therefore, effectively subtracts half the reference voltage from the potential divider voltage. (The ratio of one-half comes about effectively because of the 2 to 1 ratio of R14 to R12, feeding the summing junction IC 5A-2; R14 is 4k and R12 is 2k).

The output, IC 5A-1, of this summing amplifier is the Transient Thermal Compensation output. Feedback from the output, via noninverting buffer amplifier IC 5B-7 is used to linearize the volts versus temperature scale. IC 5A-1 will be at zero volts when no temperature difference exists between the casting and the removable disk air. A negative voltage on TP6 indicates the pack is colder than the casting and a positive voltage indicates the pack is hotter than the casting.

Transient Thermal Compensation is summed into the thermal loop whenever the removable disk is selected. Both Transient and DC Thermal Compensation voltages are fed to LM 311 comparators, IC's 1-2 and 2-3. The comparators have a threshold of ± 1 volt; if Transient or DC Compensation voltages are outside of this limit, pin 17 goes low, signaling overcompensation.

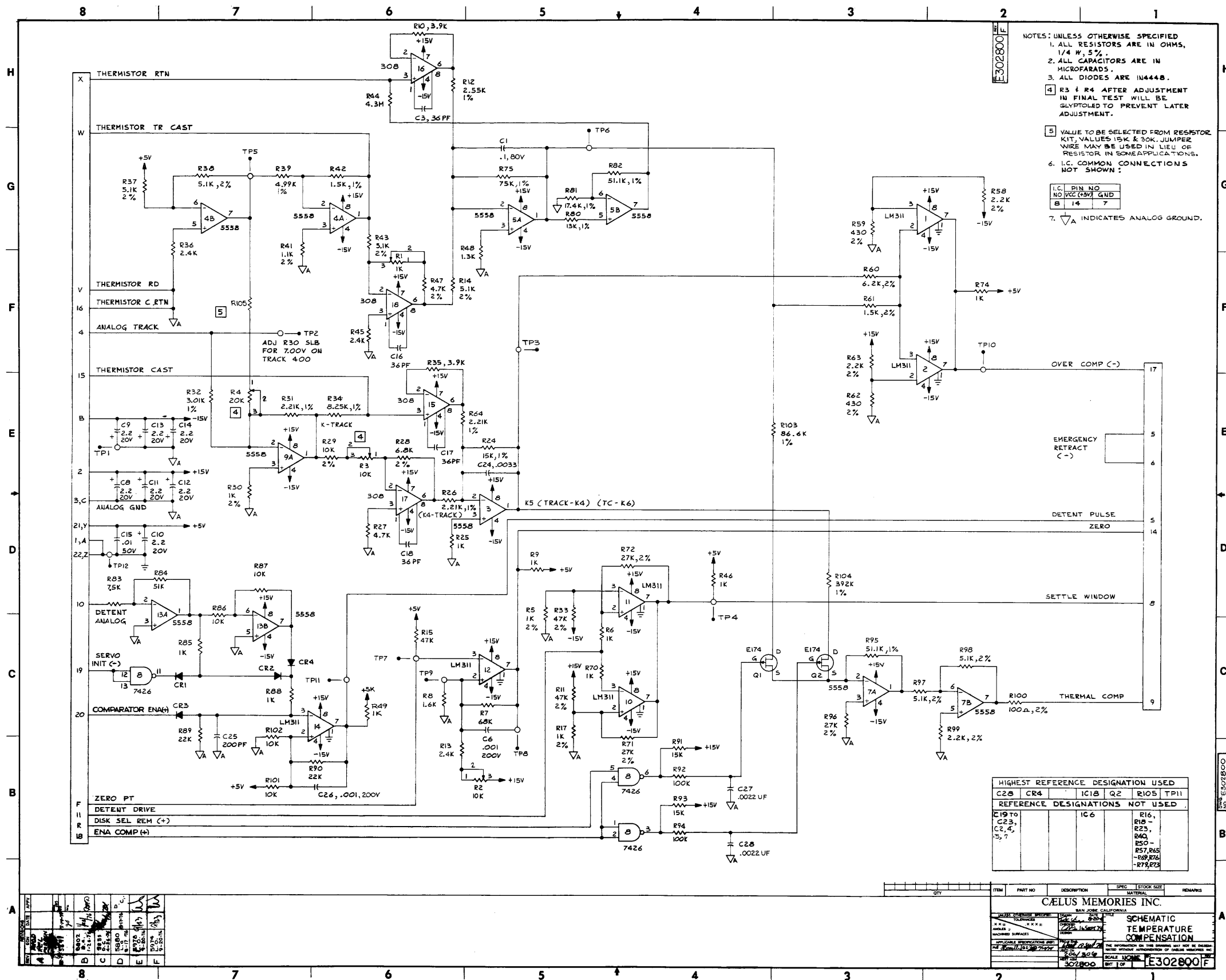


Figure 5-21. (Repeat) Temperature Compensation Board Schematic

The casting-to-removable-disk air temperature difference is monitored very closely by the overcompensation network; overcompensation goes true (low) at pin 17 whenever the difference exceeds 2°F. The casting temperature range can vary between 18° and 200°F before overcompensation goes true, and the main function of this part of the circuitry is to check for electrical failure of the thermistor, i.e., open or short circuits occurring.

5.4.8.3 Settle Window and Zero Circuits

Settle Window (+), which is output at pin 8, is generated by LM311 comparator IC's 10 and 11, connected in a wired-Or configuration. The output will go high when the Detent signal is within ± 600 millivolts of zero, which corresponds to a head position of approximately ± 300 microinches, or ± 1/16 track.

The trip level of the Zero PT is set by R2. IC 12 is the comparator used to generate a logic level switch at the track zero crossing. The zero signal switches between tracks 1 and 2.

5.4.8.4 100 TPI Differences

Whenever the 206 drive is utilized as a 100 TPI product, temperature compensation is not necessary and may be jumpered out. This is accomplished by jumpering test points 3 and 4 to ground.

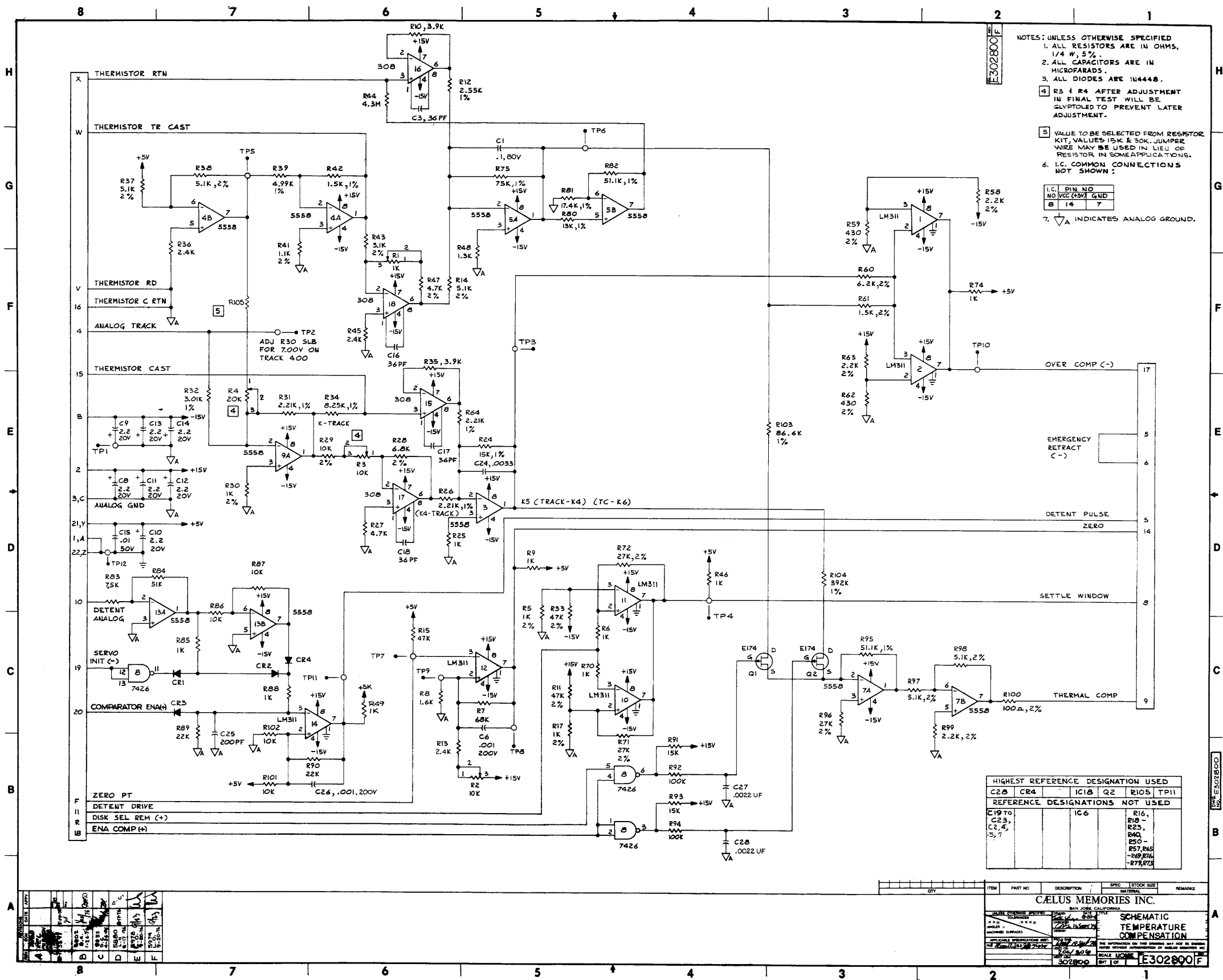


Figure 5-21. (Repeat) Temperature Compensation Board Schematic

5.4.9 Read/Write Amplifier (R/WA)

The Read/Write Amplifier provides the circuitry necessary for recording and recovery of data. Circuits contained on the R/WA include Head/Disk Select, Write Inhibit, Write, and Ready. (See Figure 5-22.)

5.4.9.1 Head/Disk Select Circuit

The read/write winding of each head is connected across pins 1 and 4 of its connector, and its center tap is connected to pin 3. Pins 1 and 4 from the read/write winding of each head are connected to two common Read/Write lines via diodes. The DC erase winding is connected across pins 2 and 3.

The head selection for the read or write function is performed by turning on the particular transistor (Q1 through Q4) connected to the center tap of the selected head.

NOTE

Only one transistor can be turned on at any given time.

In the write process, only the selected head can sink record current from Q12 or Q13 via its selector transistor.

During the read process, selector current flows from +15V, via the selector transistor into the center tap of the particular head. The selector current then flows out through pins 1 and 4 through the particular diodes into the two common read/write lines, then via CR41 into pin 1 of Transformer T1, via CR42 into pin 5 of T1, then out via the center tap pin 3 of T1, and finally via resistor R25 to ground.

The currents through the two halves of the read/write winding are in balanced opposition, so no net flux results in the head or transformer from the select current.

The particular diodes on pins 1 and 4 of the selected head are the only ones to be forward-biased by the select current, enabling the small Read signals from the head to be presented to the primary of T1.

The notations for the Head Select and Disk Select signals are indicated as being positive when true. In other words, if Head Select Bottom (+) was at ground level, the top head of the select disk would be enabled.

IC's 3A, 3B, and 5 comprise a decode matrix for the Head Select and Disk Select signals. The Head Select and Disk Select signals

are two lines which will provide four combinations for selecting fixed or removable disk, top or bottom head. (Refer to Table 5-4 for head and disk selection.)

Disk Select REM	Head Select Bottom	Disk	Storage Surface	Head	Transistor
High	Low	Removable	Upper	Top	Q1
High	High	Removable	Lower	Bottom	Q2
Low	Low	Fixed	Upper	Top	Q3
Low	High	Fixed	Lower	Bottom	Q4

5.4.9.2 Write Inhibit Circuit

The Write Inhibit circuit consists of Q22 and Q23 located at coordinates C6 in Figure 5-21. The output of Q22 switches Write Inhibited, WRT INHBD (-), status line to ground whenever a write operation is being attempted on a disk whose write inhibit switch is turned on.

There are several jumper configurations that can be applied to the Write Inhibit circuit. If jumper E3 to E5 is installed, Q22 is turned on when the write inhibit switch for the selected disk is on. (This is independent of a write operation.) Q22 is turned on because the output of IC 2-6 is high when the write inhibit switch for the selected disk is on. Turning on Q22 provides a ground level to the WRT INHBD (-) line.

If jumper E4 to E5 is installed, Q22 is controlled by Q5 and is turned off during a write operation. This is because the collector of Q5 is at ground when the write operation is in process. A write operation must be attempted to sample the WRT INHBD (-) when jumper E4 to E5 is installed.

If jumper E1 to E2 is installed, Q23 is allowed to turn off Q22, if the Controller is not performing a write operation. This prevents the write inhibited status from being true when not writing and is provided for those Controllers that inhibit the write operation if the status line is low prior to writing.

5.4.9.3 Write Circuit

The Write circuit consists of IC 7, Q10, Q11, Q12 and Q13. Any time a write operation takes place, an erase function is also performed. The erase function is a tunnel erase which limits the

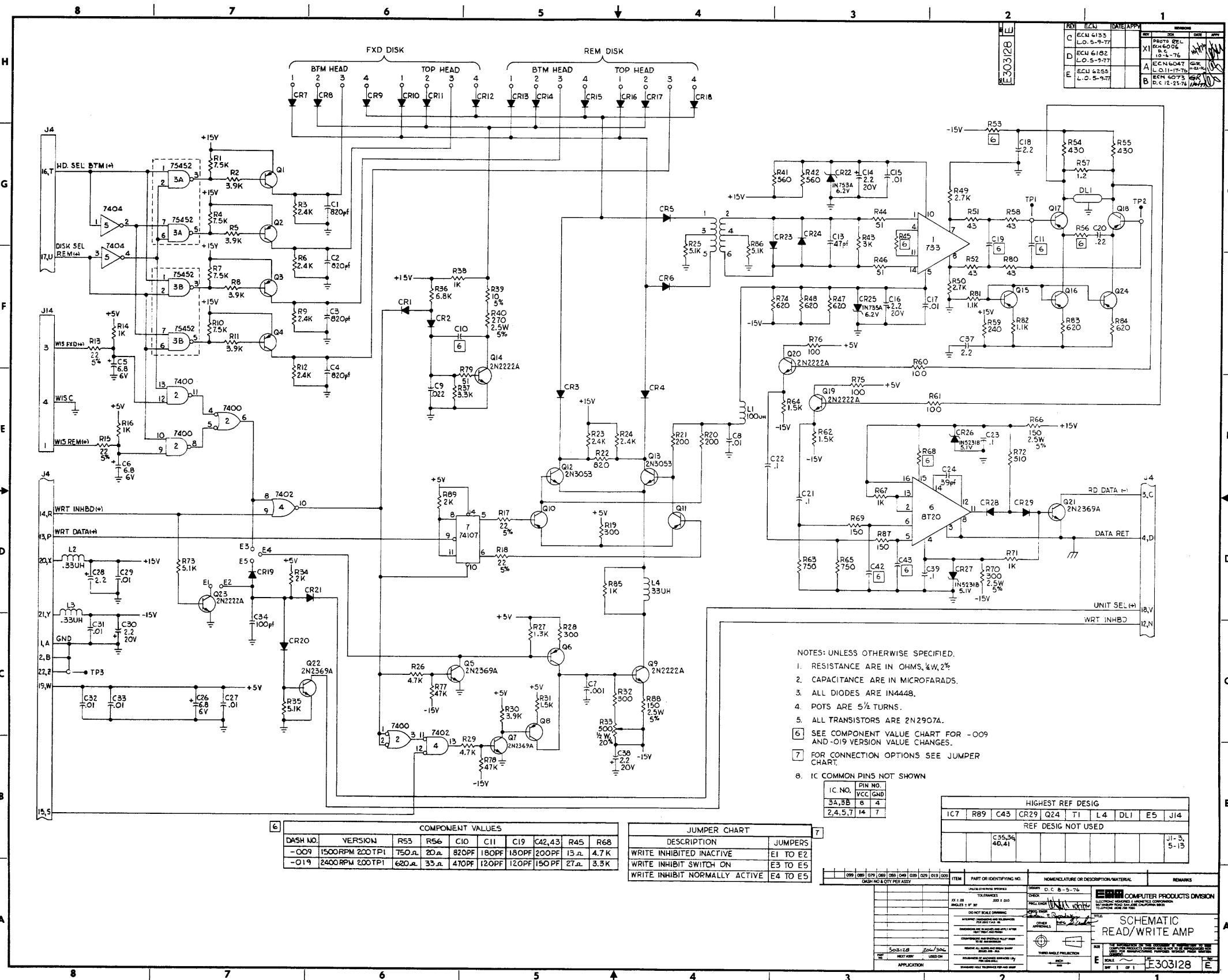


Figure 5-22. Read/Write Amplifier Board Schematic

width of the written track. The erase driver transistor Q14, located at coordinates E5, will be discussed with the Write circuit.

The Write Enable signal is located at coordinates D6 and is the output of IC 4-10. When this signal is positive, the write operation is enabled. The inputs on IC's 4-8 and 4-9 can inhibit the write operation. The input on IC 4-9 is a combination of Write Enable from the Controller and Seek Complete. The input on IC 4-8 is the output of IC 2-6 and can also inhibit the write operation from being performed. This signal is developed by Anding the write inhibit switch with the disk select line on IC 2. In other words, the write operation will only take place as long as the write inhibit switch for the selected disk is not turned on, the Controller is performing a write operation, and the drive is not performing a seek operation.

The output of IC 4-10 is simultaneously applied to three circuits. One circuit, Q14, is located at coordinates F5 in Figure 5-22. The positive output from IC 4-10 turns on Q14 after a 14-microsecond delay produced by C9, C10, and R37. Once Q14 is turned on, erase current is applied to pin 2 of the selected read/write head. This DC erases a 0.0015-inch zone on both sides of the written track. The 14-microsecond delay is necessary because of the physical displacement between the write and erase coils.

The positive output from IC 4-10 is also applied to the master reset of the write data flip flop, IC 7-10. This flip flop toggles as the write data, which are in double-frequency format, are applied to the clock input at IC 7-9. As IC 7 toggles, the write amplifiers Q10 and Q11, which are connected in push-pull, alternately turn on and off. Current drivers Q12 and Q13 allow the direction of current through the read/write coils to be toggled in relation to the data rate. This means that when zeros are being written, the direction of current through the read/write coils is reversed every 400 nanoseconds for 2,400 rpm and every 630 nanoseconds for 1,500 rpm. When ones are being written, this change occurs every 200 nanoseconds at 2,400 rpm and every 315 nanoseconds at 1,500 rpm.

The current source for Q12 and Q13 is transistor Q9. This transistor is also controlled by the output of IC 4-10. The output of IC 4-10 is also applied to pins 1 and 2 of IC 2 and is inverted through IC 2. The input on IC 4-11 will be low when a write operation is being performed. This Write signal is Anded with CYL 256 (+) on IC 4-12, allowing a high output from IC 4-13 when a write operation is being performed on cylinders 0 through 255. Q5 being turned on, turns Q6 on which in turn turns on Q9. Q9 then supplies write current to current ampli-

fiers Q12 and Q13. Whenever writing on cylinders less than 256, IC 4-13 being high turns on Q7 which turns on Q8, supplying 14 percent more write current while writing cylinders 0 through 255 than on cylinders 256 through 407. This is necessary because of the increased bit packing-density at the disk center.

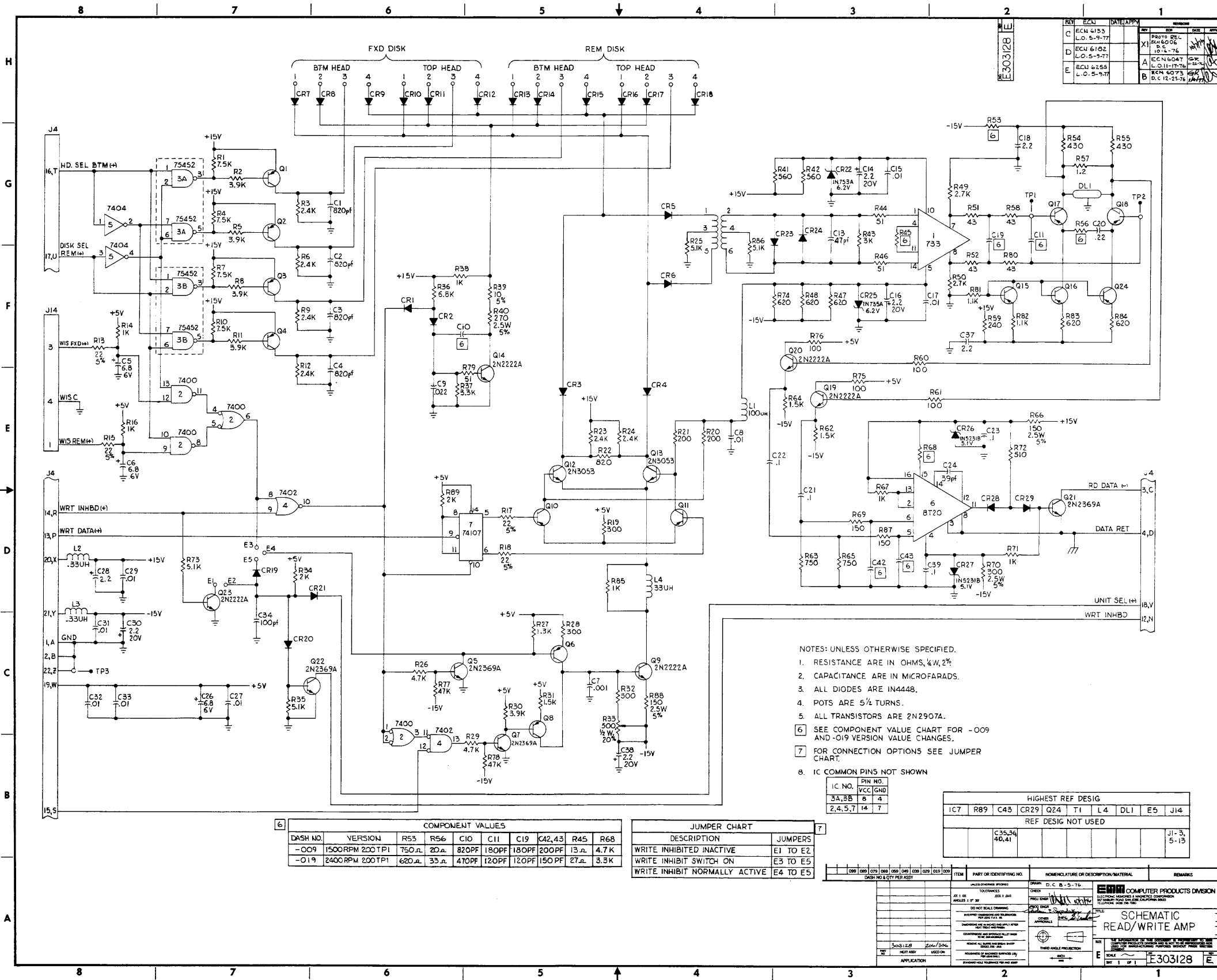
5.4.9.4 Read Circuit

The Read circuit consists of T1, IC 1, IC 6, and Q17 through Q21 located at coordinates G2 and G3 through E2 and E3 in Figure 5-22.

The rotational movement of the disk passing under the selected read/write head induces a voltage into the read/write coil which is fed to read transformer T1. The secondary of T1 drives pre-amplifier IC 1 where the signal is amplified and output on pins 7 and 8. The preamplifier output can be monitored on test points TP1 and TP2. TP1 is used while aligning the read/write heads and is a primary troubleshooting test point. During a write operation, TP1 or TP2 should measure from 6 to 8 volts peak-to-peak. During a read operation, the minimum amplitude from any read/write head as measured on TP1 or TP2 is 60 millivolts for 100 microseconds. (This amplitude measurement is taken at track 407.)

The outputs at pins 7 and 8 of preamplifier IC 1 are applied to differentiators Q17 and Q18 which drive emitter followers Q19 and Q20. The outputs of Q19 and Q20 are applied to the input pins 5 and 6 of IC 6, which is a bidirectional one shot, driven from an internal comparator. IC 6 gives a one shot output pulse for each axis-crossing of the amplified differentiated waveform from the head, thereby functioning as a peak detector. The output of IC 6 drives line driver Q21.

Q21 provides digital double-frequency read data to the card cage Mother board. If Controller design dictates, these double-frequency data must be applied to the Data Translator board prior to being sent to the Controller. The Data Translator board converts the double-frequency data to the proper format. The most common format is NRZ.



REV	ECN	DATE	APP'D	BY	CHK'D	DATE
C	ECN 6153	L.O. 5-9-77				
D	ECN 6162	L.O. 5-9-77				
E	ECN 6258	L.O. 5-9-77				

- NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTANCE ARE IN OHMS, $\frac{1}{2}$ W, 2%.
 2. CAPACITANCE ARE IN MICROFARADS.
 3. ALL DIODES ARE IN4448.
 4. POTS ARE $\frac{1}{4}$ TURNS.
 5. ALL TRANSISTORS ARE 2N2907A.
 6. SEE COMPONENT VALUE CHART FOR -009 AND -019 VERSION VALUE CHANGES.
 7. FOR CONNECTION OPTIONS SEE JUMPER CHART.
 8. IC COMMON PINS NOT SHOWN.

[6] COMPONENT VALUES									
DASH NO.	VERSION	R53	R56	C10	C11	C19	C42,43	R45	R68
-009	1500RPM 200TP1	750 Ω	20 Ω	820PF	180PF	180PF	200PF	13 Ω	4.7K
-019	2400RPM 200TP1	620 Ω	33 Ω	470PF	120PF	120PF	150PF	27 Ω	3.3K

[7] JUMPER CHART		
DESCRIPTION	JUMPERS	
WRITE INHIBITED INACTIVE	E1 TO E2	
WRITE INHIBIT SWITCH ON	E3 TO E5	
WRITE INHIBIT NORMALLY ACTIVE	E4 TO E5	

HIGHEST REF DESIG							
IC7	R89	C43	CR29	Q24	T1	L4	DL1
REF DESIG NOT USED							
		C35,36					J1-3
		40,41					5-13

ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	REMARKS
1	UNLESS OTHERWISE SPECIFIED	DRWTR D.C. 8-5-76	
2	AS SHOWN	TESTED	
3	AS SHOWN	TESTED	
4	AS SHOWN	TESTED	
5	AS SHOWN	TESTED	
6	AS SHOWN	TESTED	
7	AS SHOWN	TESTED	
8	AS SHOWN	TESTED	
9	AS SHOWN	TESTED	
10	AS SHOWN	TESTED	

COMPUTER PRODUCTS DIVISION
ELECTRONIC DRAWING & REVISIONS DEPARTMENT
1000 WEST 12TH AVENUE, DENVER, CO. 80202
TELEPHONE 862-2500

SCHEMATIC
READ/WRITE AMP

SCALE: 1" = 1"

E-303128

Figure 5-22. (Repeat) Read/Write Amplifier Board Schematic

5.4.10 Data Translator Board (DTB)

The Data Translator board consists of three portions. One portion of the DTB is a phase locked loop system which is used in conjunction with the data decoder. These two circuits receive raw double-frequency data from the Read/Write board and transmit decoded data in one of the three optional formats. A synchronous data clock is provided for optional data formats. The remainder of the board generates the double-frequency write data from the input write data if the input data is NRZ. An optional crystal controlled clock is used to maintain frequency stability. See Figure 5-24 for the Data Translator board schematic.

5.4.10.1 Phase Locked Loop

When a read cycle begins, the read enable goes true. This enables several circuits in the phase locked loop.

The raw data are then received from the Read/Write board. The first databit received will set the two input flip flops, IC 13. This, in turn, sets the blanking one shot, IC 11, at coordinates D6. The blanking one shot holds IC 6-13, at coordinates E4, reset. This inhibits transmission of erroneous data before the system has acquired phase lock. This time is 13 microseconds for 2,400 rpm, 21 microseconds for 1,500 rpm. During this period the preamble is being read, (all zeros).

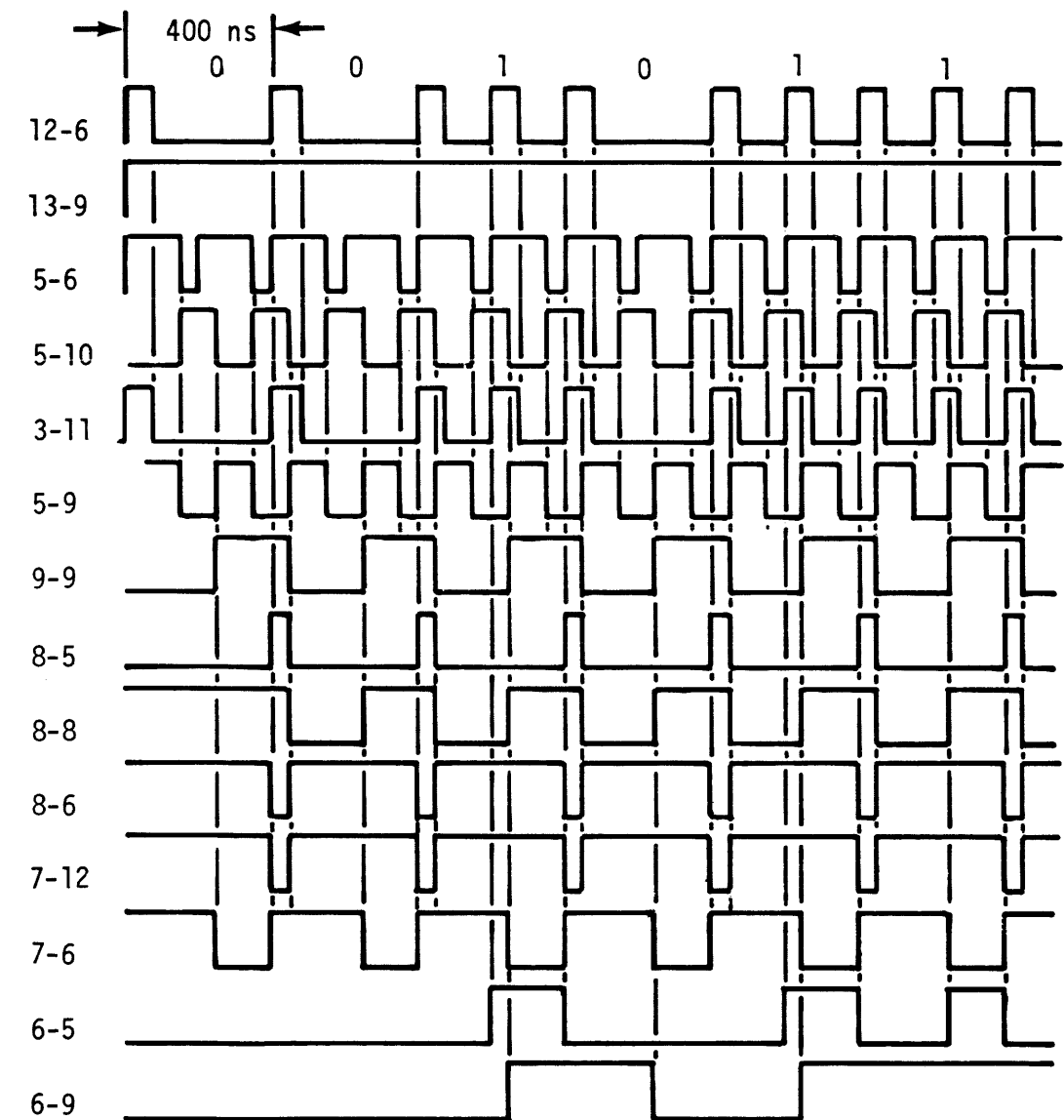
Phase locking is accomplished by varying the firing time of one shot IC 5-6. The charging current is provided by Q7 at coordinates F2 and is controlled by the voltage across C14.

C14 integrates the charge current of Q4 (G3) and discharge current of Q6 (F3). These current sources are enabled by a duty cycle which is modified in a direction such that the leading edge of the signal at IC 5-10 will tend to remain constant with respect to the leading edge of the read data.

A correction is handled in this manner: Assume the raw data frequency has increased. The signal at IC 3-11 will arrive earlier. In this case, IC 8-5 will fire sooner; thereby charging capacitor C14 for more time than discharging. The voltage at C14 will rise and more charging current will be supplied to the one shot, IC 5-6, from transistor Q7, increasing its speed.

5.4.10.2 Read Decode Circuitry

Conversion is illustrated with the timing chart in Figure 5-23. The first line on the timing chart represents raw data as seen by the DTB on IC 12-6. This line shows a clock bit occurring every 400 nanoseconds for approximately 75 nanoseconds.

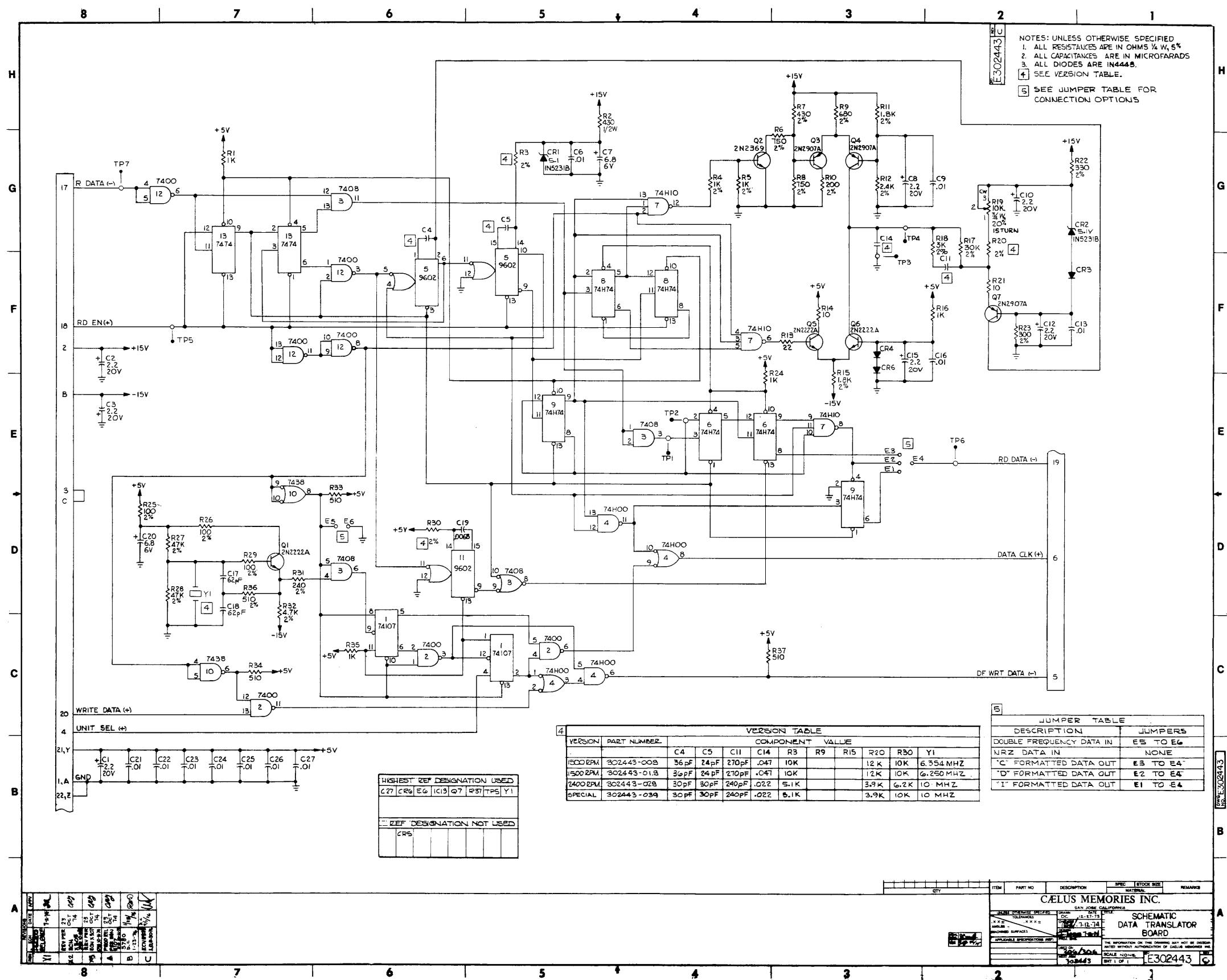


NOTE: SHOWN WITH SLIGHT PHASE LOCK ERROR FOR CLARIFICATION.

200-35

Figure 5-23. DTB Timing

The bit cell time at 2,400 rpm, 2,200 bits per inch is 400 nanoseconds. Lack of a bit between the clock bits represents a zero bit and a bit occurring between two consecutive clock bits represents a one bit. The data as drawn in this timing chart represents a 001011.



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTANCES ARE IN OHMS 1/4 W, 5%
 2. ALL CAPACITANCES ARE IN MICROFARADS
 3. ALL DIODES ARE 1N4448.
 4. SEE VERSION TABLE.
 5. SEE JUMPER TABLE FOR CONNECTION OPTIONS

VERSION	PART NUMBER	C4	C5	C11	C14	R3	R9	R15	R20	R30	Y1
1500ZPM	302443-008	36 pF	24 pF	270 pF	.047	10K			12 K	10K	6.354 MHZ
1500ZPM	302443-018	30 pF	24 pF	270 pF	.047	10K			12 K	10K	6.250 MHZ
2400ZPM	302443-028	30 pF	30 pF	240 pF	.022	5.1K			3.9 K	6.2 K	10 MHZ
SPECIAL	302443-039	30 pF	30 pF	240 pF	.022	5.1K			3.9 K	10 K	10 MHZ

DESCRIPTION	JUMPERS
DOUBLE FREQUENCY DATA IN	E5 TO E6
NRZ DATA IN	NONE
'C' FORMATTED DATA OUT	E3 TO E4
'D' FORMATTED DATA OUT	E2 TO E4
'I' FORMATTED DATA OUT	E1 TO E4

HIGHEST REF DESIGNATION USED
C27 CR4 EG IC13 Q7 R37 TP5 Y1
REF DESIGNATION NOT USED
CR5

REV	DATE	BY	CHKD	APP'D
1	11/18/74	WJ	WJ	WJ
2	12/10/74	WJ	WJ	WJ
3	1/10/75	WJ	WJ	WJ
4	2/10/75	WJ	WJ	WJ
5	3/10/75	WJ	WJ	WJ
6	4/10/75	WJ	WJ	WJ
7	5/10/75	WJ	WJ	WJ
8	6/10/75	WJ	WJ	WJ
9	7/10/75	WJ	WJ	WJ
10	8/10/75	WJ	WJ	WJ
11	9/10/75	WJ	WJ	WJ
12	10/10/75	WJ	WJ	WJ
13	11/10/75	WJ	WJ	WJ
14	12/10/75	WJ	WJ	WJ
15	1/10/76	WJ	WJ	WJ
16	2/10/76	WJ	WJ	WJ
17	3/10/76	WJ	WJ	WJ
18	4/10/76	WJ	WJ	WJ
19	5/10/76	WJ	WJ	WJ
20	6/10/76	WJ	WJ	WJ
21	7/10/76	WJ	WJ	WJ
22	8/10/76	WJ	WJ	WJ
23	9/10/76	WJ	WJ	WJ
24	10/10/76	WJ	WJ	WJ
25	11/10/76	WJ	WJ	WJ
26	12/10/76	WJ	WJ	WJ
27	1/10/77	WJ	WJ	WJ
28	2/10/77	WJ	WJ	WJ
29	3/10/77	WJ	WJ	WJ
30	4/10/77	WJ	WJ	WJ
31	5/10/77	WJ	WJ	WJ
32	6/10/77	WJ	WJ	WJ
33	7/10/77	WJ	WJ	WJ
34	8/10/77	WJ	WJ	WJ
35	9/10/77	WJ	WJ	WJ
36	10/10/77	WJ	WJ	WJ
37	11/10/77	WJ	WJ	WJ
38	12/10/77	WJ	WJ	WJ
39	1/10/78	WJ	WJ	WJ
40	2/10/78	WJ	WJ	WJ
41	3/10/78	WJ	WJ	WJ
42	4/10/78	WJ	WJ	WJ
43	5/10/78	WJ	WJ	WJ
44	6/10/78	WJ	WJ	WJ
45	7/10/78	WJ	WJ	WJ
46	8/10/78	WJ	WJ	WJ
47	9/10/78	WJ	WJ	WJ
48	10/10/78	WJ	WJ	WJ
49	11/10/78	WJ	WJ	WJ
50	12/10/78	WJ	WJ	WJ

ITEM	QTY	PART NO	DESCRIPTION	SPC	STOCK	REMARKS
CÆLUS MEMORIES INC.						
SAN JOSE CALIFORNIA						
SCHEMATIC						
DATA TRANSLATOR BOARD						
SCALE: 100% DATE: 11/18/74						
DRAWN BY: WJ CHECKED BY: WJ						
APPROVED BY: WJ						
THE INFORMATION ON THIS DRAWING MAY NOT BE USED WITHOUT AUTHORIZATION OF CÆLUS MEMORIES INC.						
SCALE: 100% DATE: 11/18/74						
PART 1 OF 1 E302443						

Figure 5-24. Data Translator Board Schematic

The next line on the timing diagram represents sync flip flop number 1, IC 13-9, which is set on the trailing edge of the first bit seen after Read Enable is true. This will, of course, be a clock bit since Read Enable must be true within the preamble: sync flip flop number 1 being in the set condition and sync flip flop number 2 being in the reset condition provide a timing pulse from IC 12-3 which starts the operation of the data discriminator. This timing pulse fires the variable frequency oscillator, IC 5-6, for approximately 150 nanoseconds. This timing pulse also fires the data masking one shot, IC 11-9, for approximately 13 microseconds. During the time that the data masking one shot is firing, a low is forced on the output of IC 3-8.

The low output from IC 3-8 holds the data formatter flip flop, IC 6-9, reset, forcing zeros on the output of the data formatter for the first 13 microseconds of the read operation, which allows time for the phase lock loop to sync to the data rate. When the variable frequency oscillator (IC 5-6) times out, the variable frequency oscillator fires the fixed frequency oscillator (IC 5-10) for approximately 100 nanoseconds and also sets sync flip flop number 2, IC 13-5.

The Q-not output of the fixed frequency oscillator, IC 5-9, is applied to the clock input of the frequency divider flip flop, IC 9-9. This flip flop is represented on line 7 of the timing chart and, as can be seen, has a 50 percent duty cycle which is true for 200 nanoseconds and false for 200 nanoseconds. This divider flip flop determines the timing for the data bits. The leading edge of IC 5-10 also retriggers IC 5-6 after two propagation delays, or about 50 nanoseconds. IC 5-6 is the controlled device in the phase locked loop.

IC's 7 and 8 are used to decode the rate of IC 5-6 timeout versus the incoming bit rate. The pulses from IC's 7-12 and 7-6 will vary in symmetry to maintain phase lock. These pulses are sent to current amplifiers Q4 and Q6. The current pulses are summed across integrating capacitor C14 to provide a voltage. This voltage is then added through a phase compensation network to the Q7 emitter. This controls the charging current to the timing network of IC 5-6, and modifies the timeout intervals to correspond to the incoming bit rate.

The data detection flip flop, IC 6-5, will be set any time a one bit is detected. This action occurs by applying raw data from the output of IC 3-3 as represented by line 4 of the timing chart, to the clock input of the flip flop. IC 9-8 is always high at bit time and low at clock time, therefore, every clock bit will reset the data detection flip flop, IC 6-5, and every one bit will set the flip flop. This flip flop is represented by line 8 of the timing diagram. Data from the first stage of the data detection flip flop are clocked to IC 6-9 whenever IC 9-9 resets.

The output of the data formatters IC 6-8 is NRZ data. When low, this line represents zero bits and when high it represents one bits. These data are clocked into the Controller receivers with the data clock output on IC 4-11. This data clock output is derived from the 10-MHz crystal during a write operation and from the read data decoder during a read operation. During a read operation, clock time is the time when one shot IC 5-10 is high and the frequency divider flip flop IC 9-9 is set.

The DTB has one adjustment which must be performed any time the board is replaced. This adjustment is accomplished by syncing positive on Read Enable while monitoring the AC voltage across the capacitor C5. The potentiometer R19 is then adjusted for a -1.2-volt differential across the capacitor.

5.4.10.3 Write Encode Circuitry

A crystal controlled write clock is generated using Q1, at coordinates D7. The crystal clock frequency is divided by four in two counter-stages. The logic is arranged so that when a write data zero is present, every other crystal/2 pulse is transmitted, thereby giving a double-frequency format. This is illustrated in Figure 5-25.

The Write Encode circuitry is located at coordinates C6 in Figure 5-24. This circuitry converts non-return-to-zero (NRZ) write data to the double-frequency format required by the Read/Write board.

The Write Encode circuitry operates by utilizing a 10-MHz crystal for 2,400 rpm and 6.354-MHz for 1,500 rpm. The frequency of the crystal is divided in half by flip flop IC 1. (A 10-MHz crystal will be assumed for this discussion.) The output frequency on pins 5 and 6 of IC 1 is 5 MHz or a 50 percent duty cycle pulse every 200 nanoseconds. The output at IC 1-6 is further divided in half by flip flop IC 1-2.

The output frequency at IC 1-2 is 2.5 MHz or a 50 percent duty cycle pulse every 400 nanoseconds. The write data line at coordinates C8 is write data in the NRZ format. These write data are Anded at IC 2-11 with Read Enable. As long as the drive is not performing a read operation, write data are gated to IC 4-2. A low signal level at IC 4-2 represents "1" bits and a high signal level represents "0" bits. This signal is inverted on IC 4-3 where it is Anded with the 5-MHz clock on IC 4-5. The output at IC 4-6 will be pulses every 200 nanoseconds whenever IC 4-2 is low or "1" bits are being written. If "0" bits were being written, as represented by IC 4-2 being high, then the output of IC 4-3 would follow the 2.5 MHz-clock from IC 1-2. This provides a pulse on the output of IC 4-6 every 400 nanoseconds.

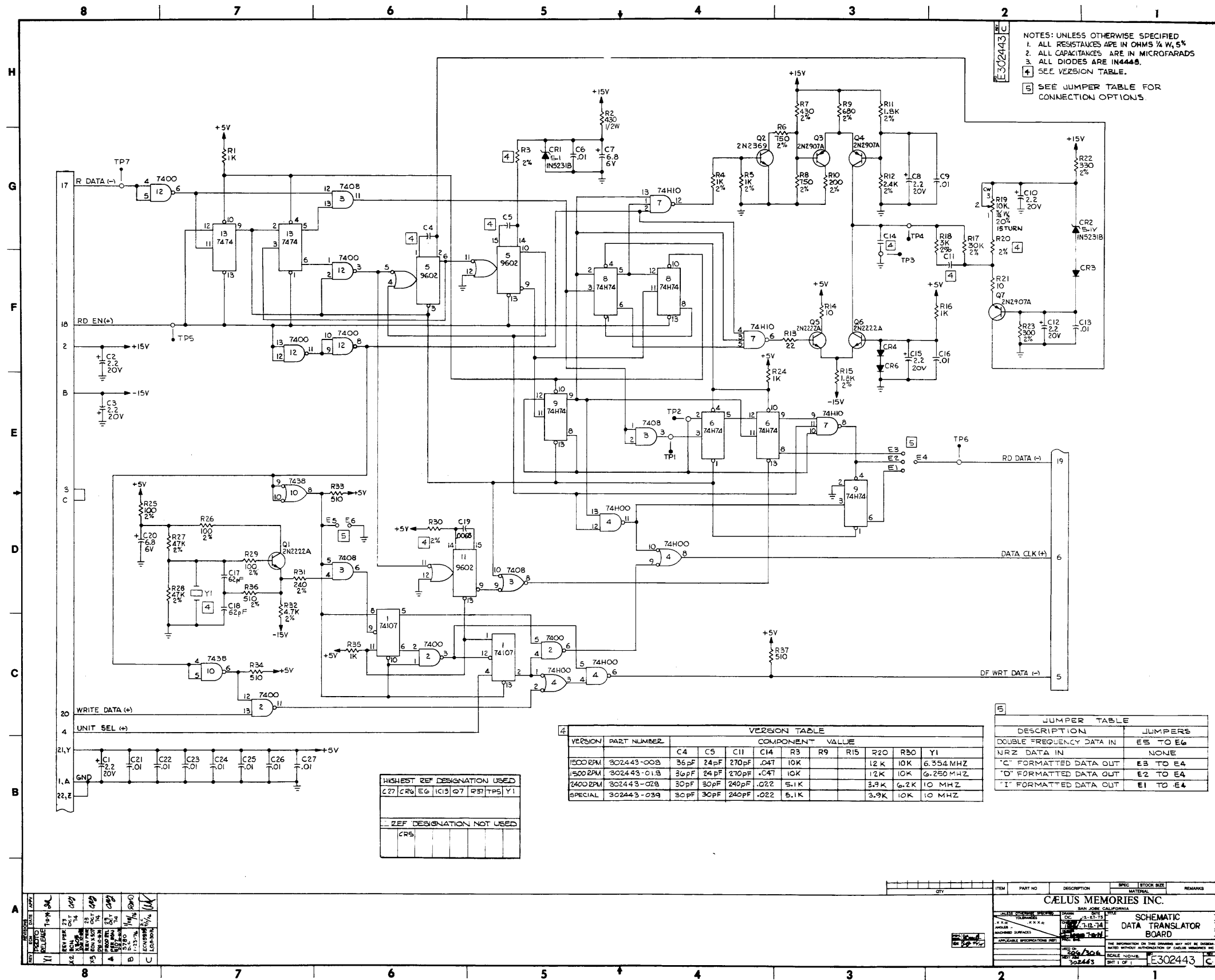
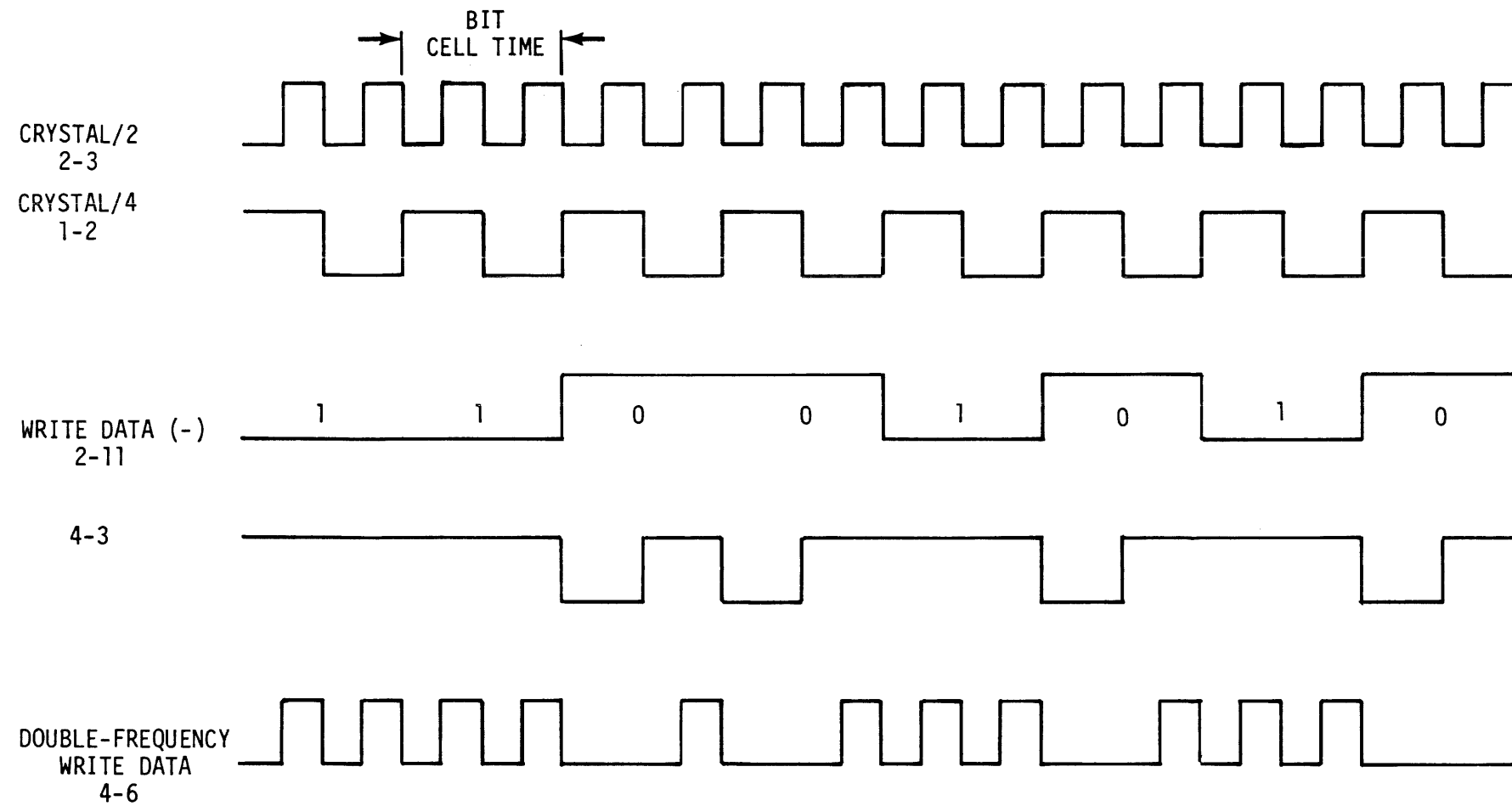


Figure 5-24. (Repeat) Data Translator Board Schematic



Jumpering pins E5 and E6 at coordinates D6 in Figure 5-22 shorts out the write clock and is used when the data provided by the Controller are in double-frequency format. With a jumper installed between pins E5 and E6, IC 1 is held reset and the outputs of IC's 1-6 and 1-2 are held high. This allows IC 4-6 to be controlled directly by the output of IC 2-11.

200-36

Figure 5-25. Write Data Timing Diagram

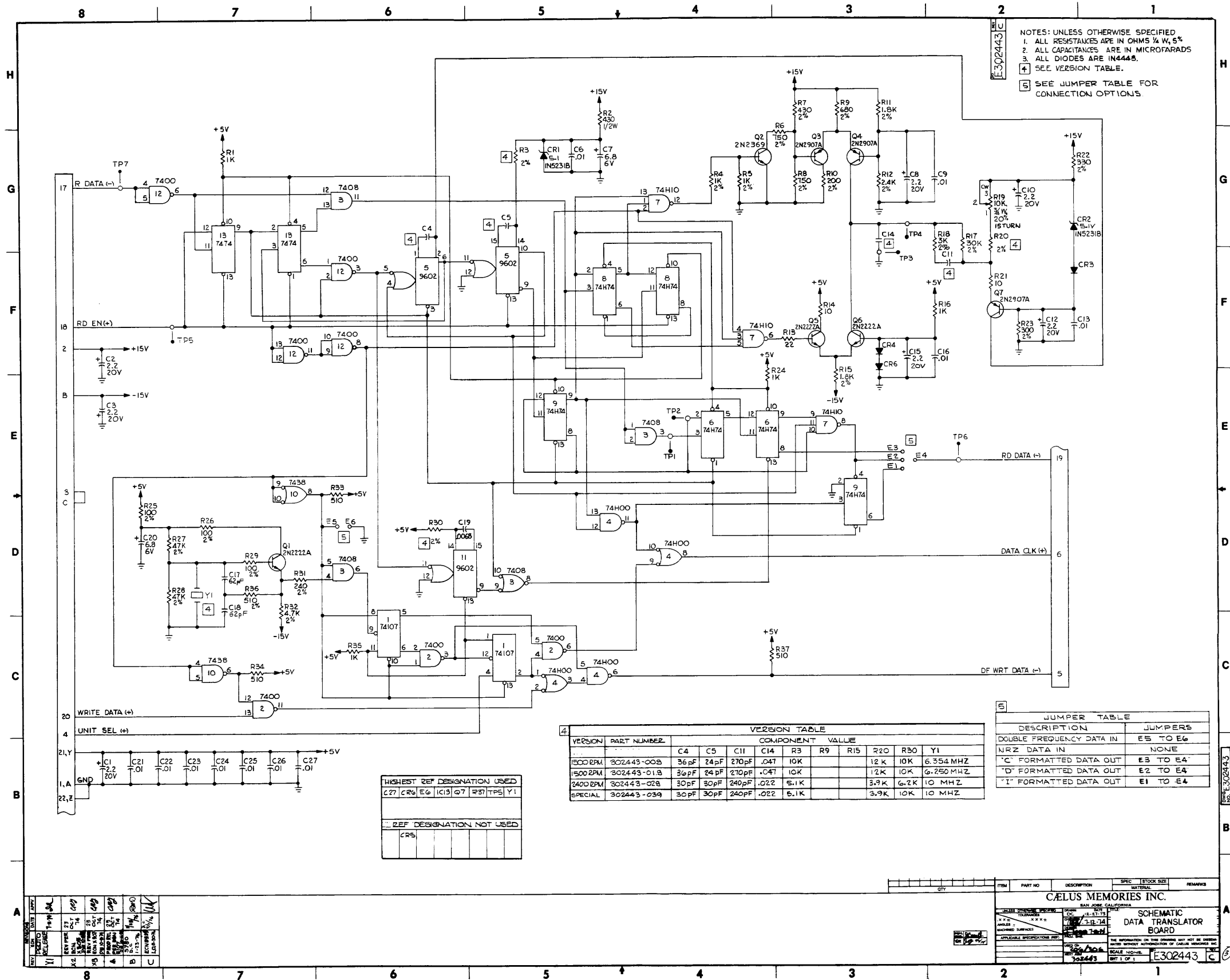


Figure 5-24. (Repeat) Data Translator Board Schematic

5.4.11 Integrated Circuits

This subsection contains Table 5-5 and Figures 5-26 through 5-49 which illustrate the various integrated circuits used on the drives.

Table 5-5. D/A Converter, CS-1020

CS-1020 SPECIFICATIONS	
Resolution	8 Bits
Linearity	$\pm .05\%$ (1/8 LSB)
Drift (Linearity)	5 ppm/ $^{\circ}\text{C}$
Full Scale	0 to E_{ref}
Open Circuit	$E_{\text{ref}} \pm 2\%$
25k Ω Termination	$\frac{E_{\text{ref}}}{2} \pm 2\%$
Drift (Referred to E_{ref})	± 20 ppm
Reference	-9V $\pm 5\%$
Zero	$\pm .025\%$
Drift (Zero)	$\pm .001\%/^{\circ}\text{C}$
Data Coding	Straight Binary, Positive True
Logic Levels	TTL Inputs 8 Parallel Bits 1 TTL Load Per Input V_{H} = Logical "1" 2.1 to 5.5V V_{L} = Logical "0" 0 volts to 7.5V
Temperature Range	
Rated Specs	-10 $^{\circ}\text{C}$ to +50 $^{\circ}\text{C}$
Storage	-55 $^{\circ}\text{C}$ to +100 $^{\circ}\text{C}$
Power Required	+20V at 20 ma -20V at 10 ma +5V at 45 ma All Supplies $\pm 5\%$

Description

Series 74 integrated circuits are designed and characterized for high-speed, general purpose digital applications where high DC noise margin and relatively low power dissipation are important system considerations. This logic series includes the basic gates, flip flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems.

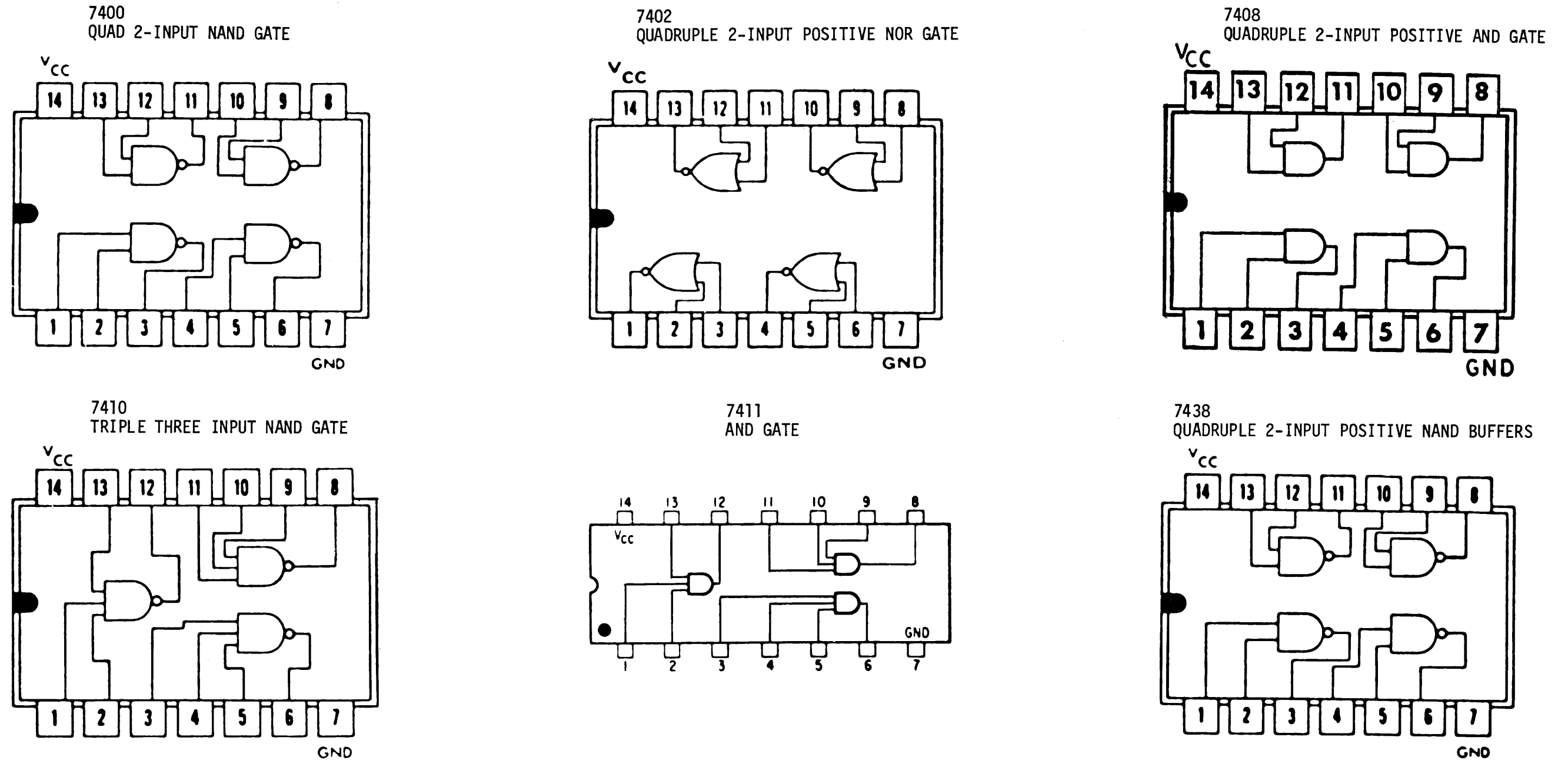
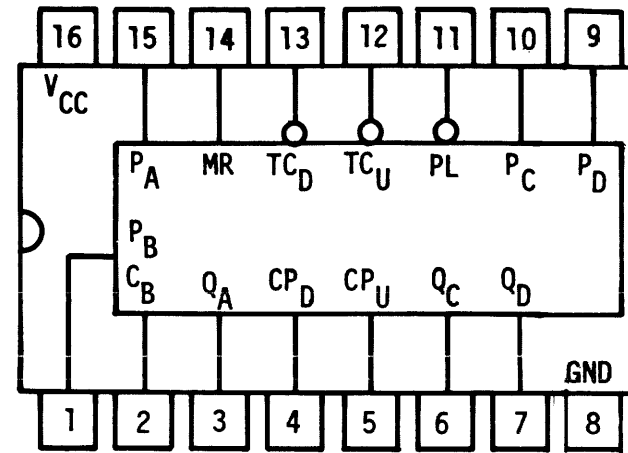


Figure 5-26. Series 74 Transistor-Transistor Logic

Description

The 74193 is a synchronous up/down 4-bit binary counter with separate up/down clocks, parallel load (asynchronous) facility, terminal count outputs for multidecade operation, and an asynchronous overriding master reset.



PIN NAMES

- \overline{PL} Parallel Load (Active Low) Input
- P_A, P_B, P_C, P_D Parallel Data Inputs
- CP_U Count Up Clock Pulse Input
- CP_D Count Down Clock Pulse Input
- MR Master Reset (Clear) Input (Asynchronous)
- Q_A, Q_B, Q_C, Q_D Counter Outputs
- TC_U Terminal Count-Up (Carry) Output
- TC_D Terminal Count-Down (Borrow) Output

CHARACTERISTICS

- TYPICAL SPEED 30 MHz Counting Frequency
- TYPICAL DELAY CP to Q 30 ns
- PACKAGE 16 Pin DIP (7B)
- TYPICAL POWER DISSIPATION 300 mw

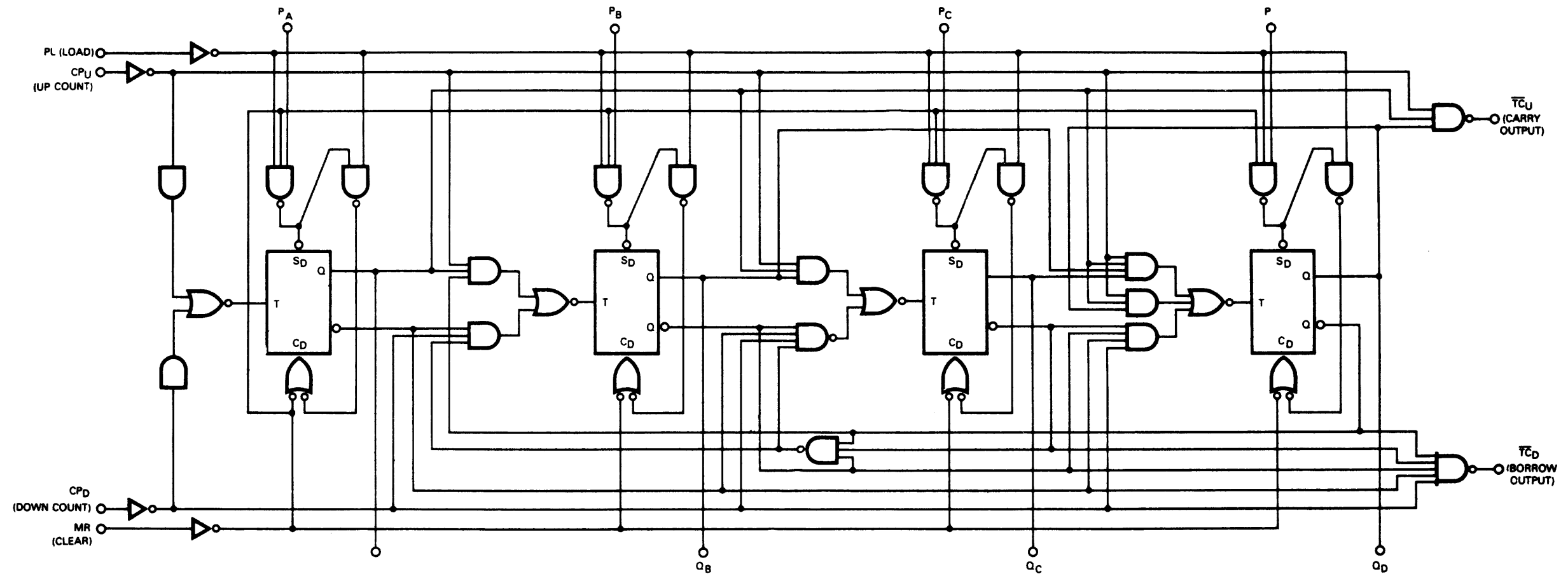
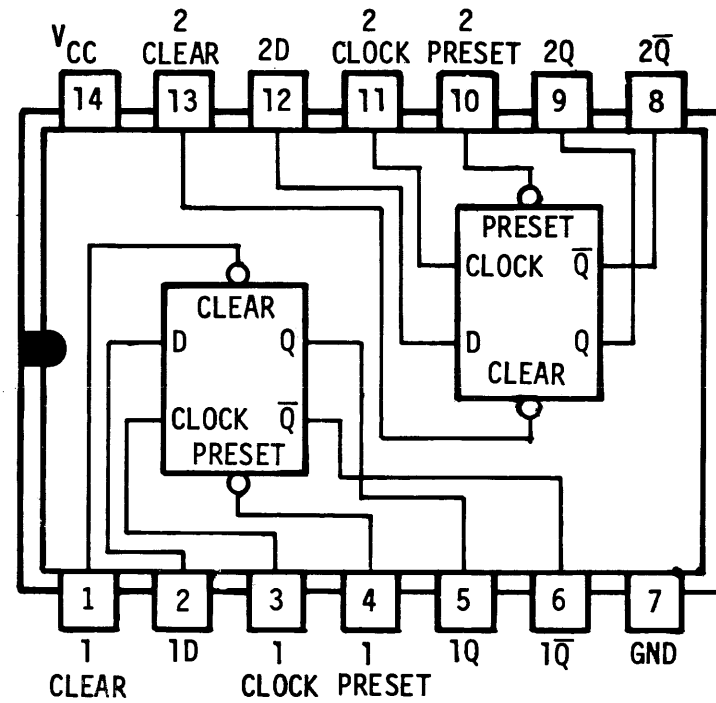
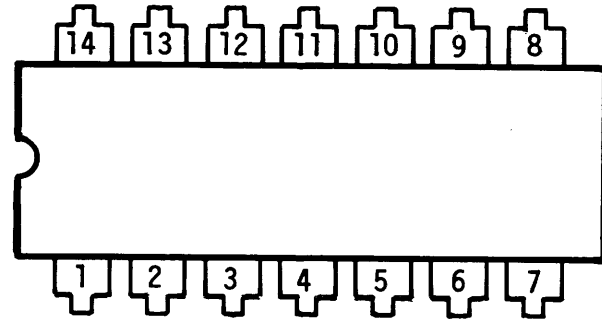


Figure 5-27. Up/Down 4-Bit Binary Counter, 74193

Description

D Flip-Flop: Edge-triggered with clear and preset inputs and complementary Q and \bar{Q} outputs. Input information is transferred to Q output on positive edge of clock pulse.

Clock triggering occurs as a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After clock input threshold voltage has been passed the data input "D" is locked out.



TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUT	OUTPUT
D	Q	\bar{Q}
0	0	1
1	1	1

- NOTES: 1. t_n = bit time before clock pulse.
 2. t_{n+1} = bit time after clock pulse.

Figure 5-28. Dual D-Type Edge-Triggered Flip Flop, 7474

Description

The 74107 is a JK Master/Slave flip flop. Asynchronous CLEAR inputs are provided on the 74107 flip flop.

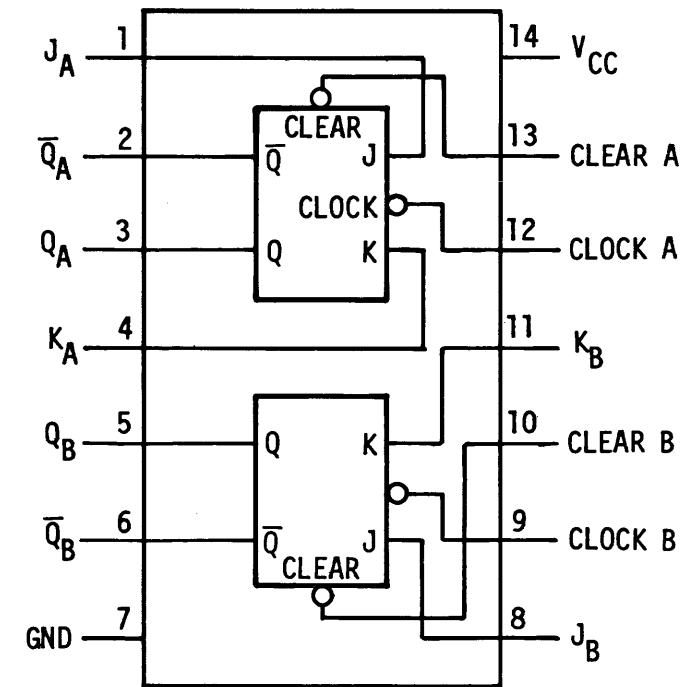
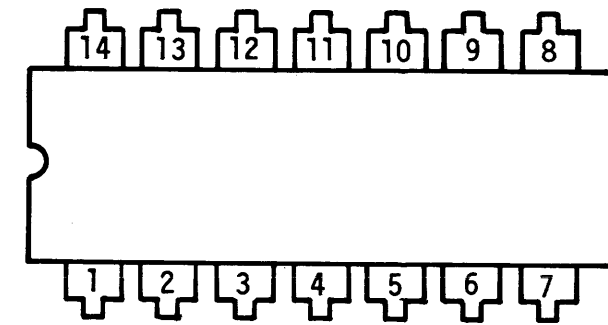


Figure 5-29. Dual JK Master-Slave Flip Flop, 74107

Description

The 9324 is a high speed expandable comparator which provides comparison between two 5-bit words and gives three outputs, "less than," "greater than," and "equal to." A high level on the active low enable input forces all three outputs low.

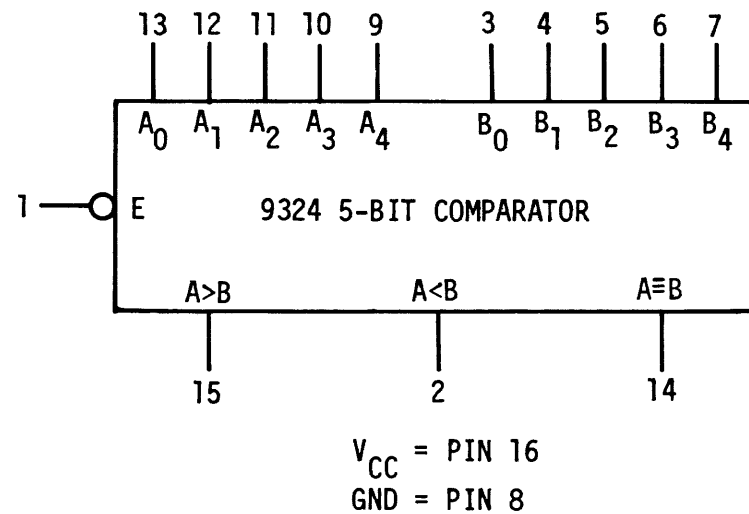
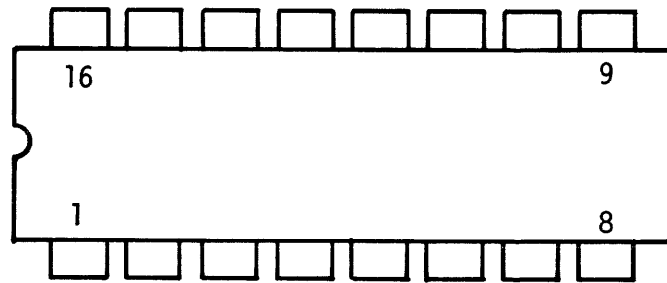
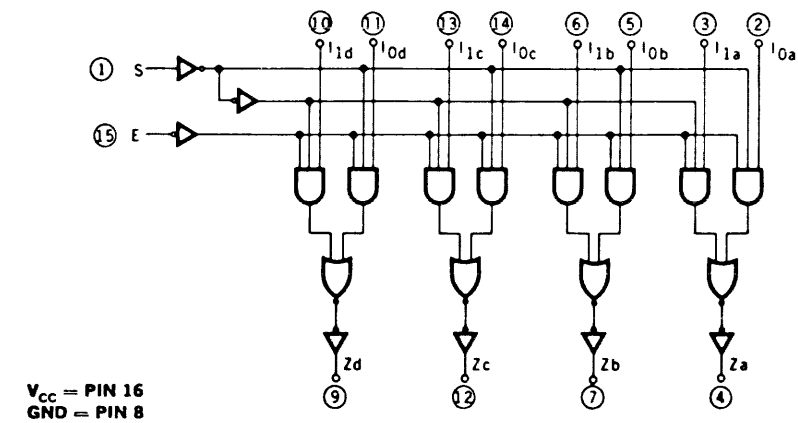


Figure 5-30. MSI 5-Bit Comparator, 9324

200-41

Description

The 9322 consists of four 2 input multiplexers with common input select logic, common active low enable and active high outputs. It allows four bits of data to be switched in parallel to the appropriate outputs from four 2 bit data sources. When the enable is not active, all the outputs are held low.



PIN NAMES		LOADING
S	Common Select Input	1 UL
\bar{E}	Enable (Active Low) Input	1 UL
Multiplexers A, B, C, D		
$1_0, 1_1$	Multiplexer Inputs	1 UL
Z	Multiplexer Outputs	10 UL

TRUTH TABLE

\bar{E}	S	$1_{0a}, 1_{0b}, 1_{0c}, 1_{0d}$	$1_{1a}, 1_{1b}, 1_{1c}, 1_{1d}$	Z_a, Z_b, Z_c, Z_d
H	X	X	X	L
L	L	H	X	H
L	L	L	X	L
L	H	X	H	H
L	H	X	L	L

H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care Condition

200-42

Figure 5-31. MSI Quad Two-Input Multiplexer, 9322

Description

The 9602 is a DC dual level sensitive retriggerable, resettable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components only. The 9602 has excellent immunity to noise on the V_{CC} and ground lines. The 9602 used TTL for high speed and high fanout capability.

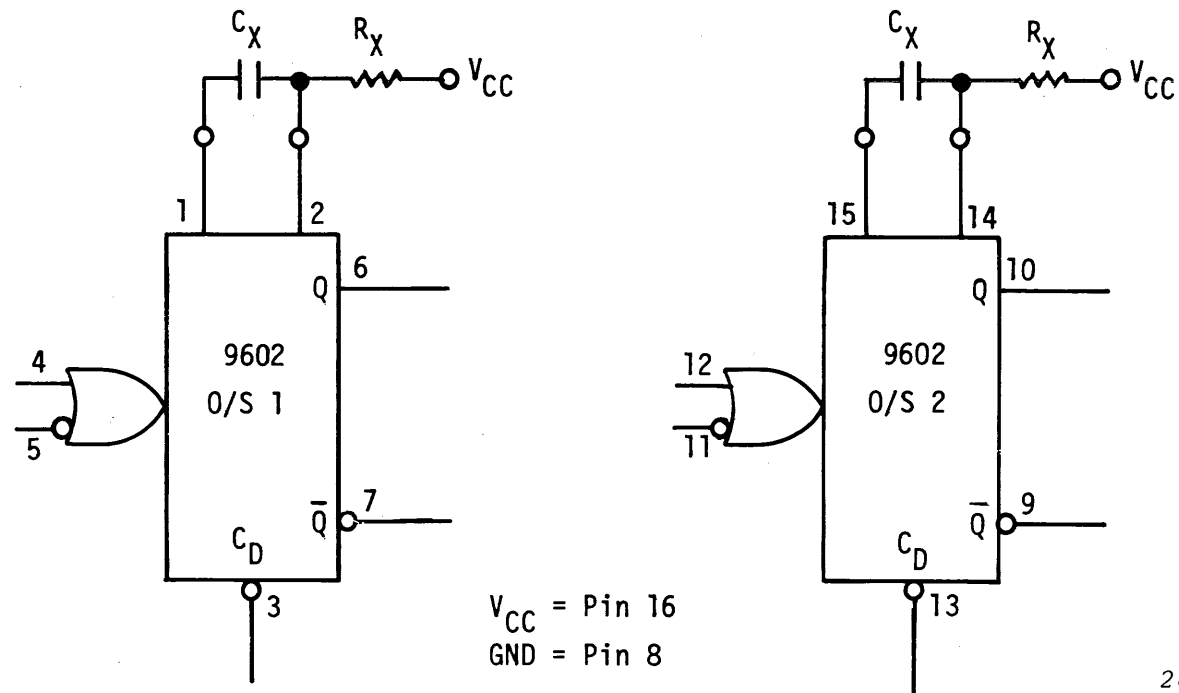
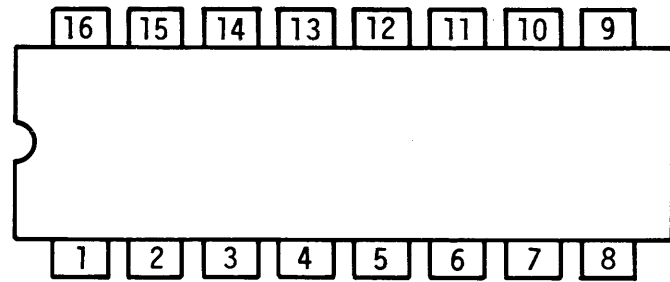
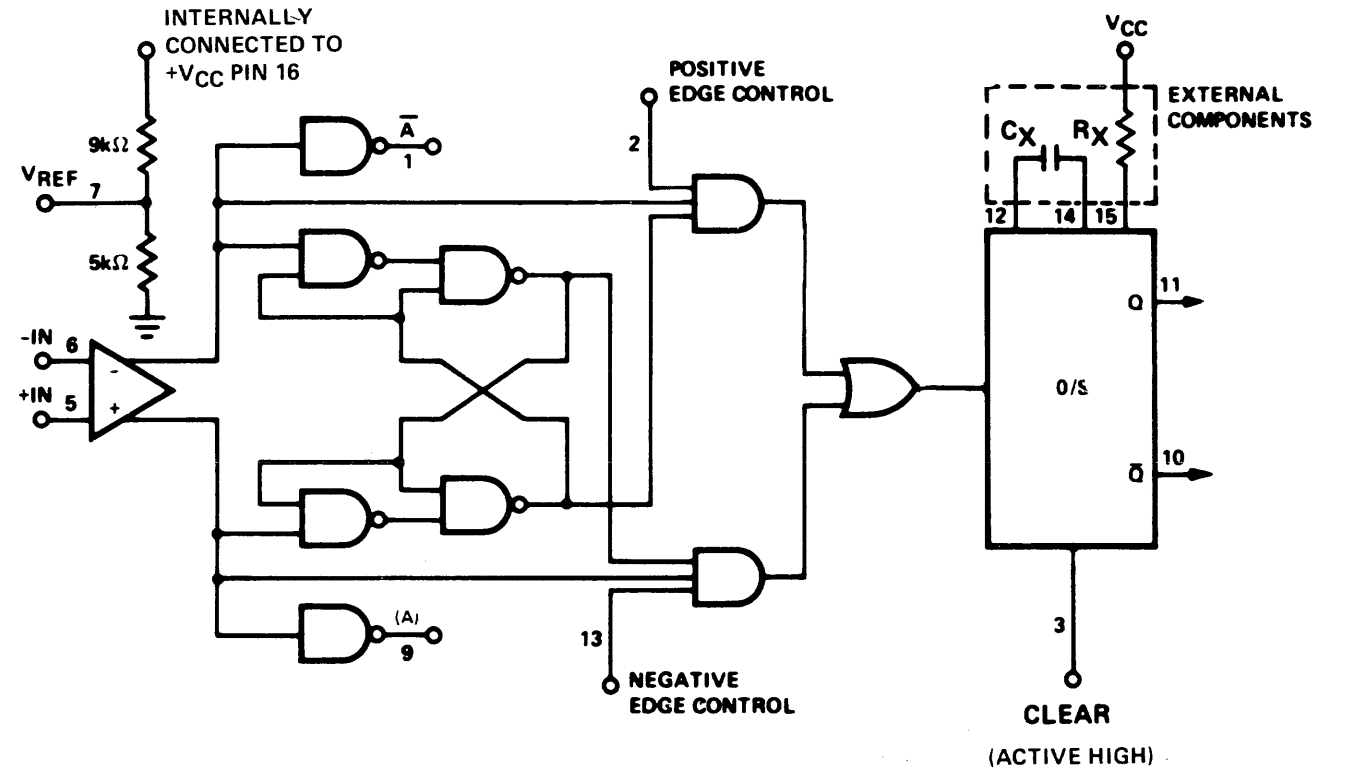


Figure 5-32. DC Dual Level Retriggerable Resettable Monostable Multivibrator, 9602

200-43



$V_{EE} = (4) (-5V \pm 5\%)$
 $V_{CC} = (16) (+5V \pm 5\%)$
 GND = (8)
 () = DENOTES PIN NUMBERS

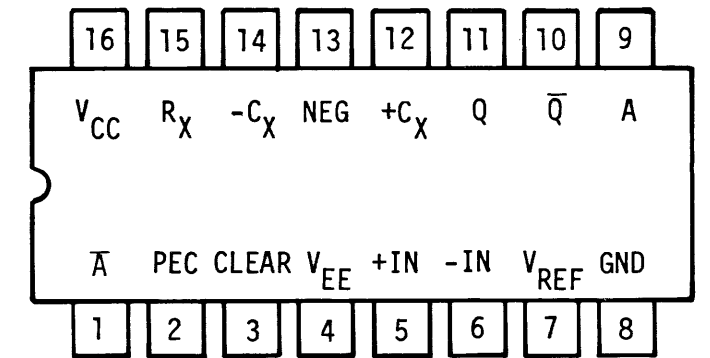


Figure 5-33. Bidirectional One Shot, 8T20

200-44

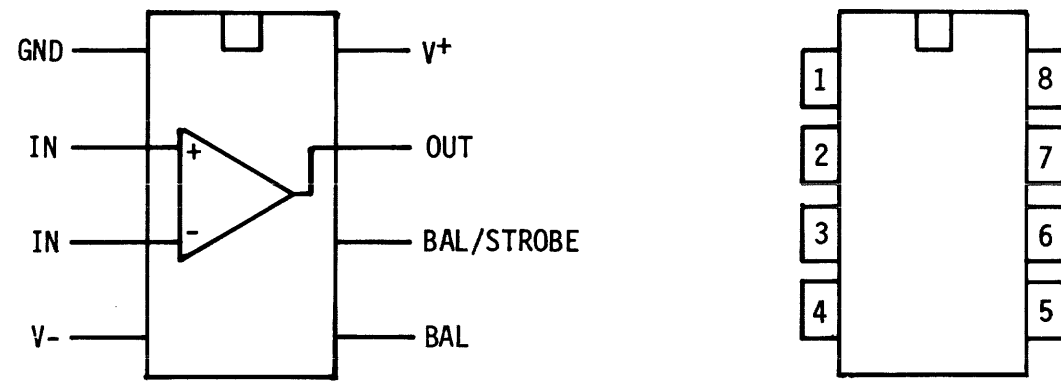
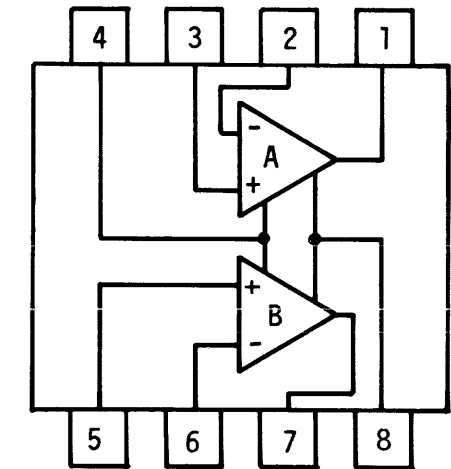


Figure 5-34. Voltage Comparator, LM311

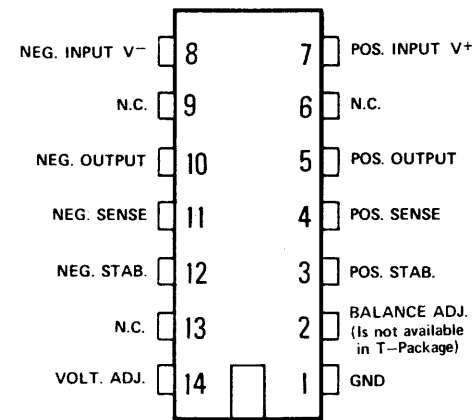
200-45

1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. V^+



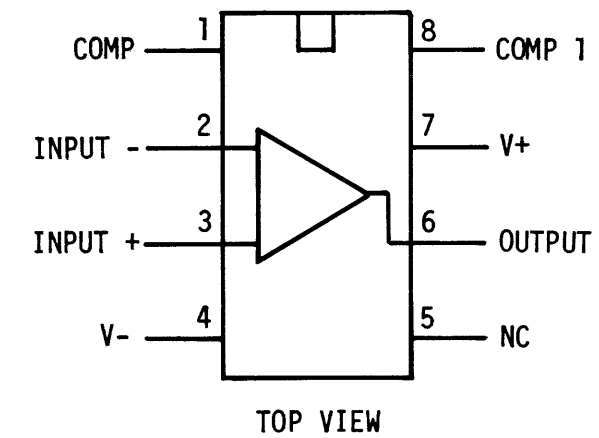
200-47

Figure 5-36. Dual Operational Amplifier, 5558



200-46

Figure 5-35. Dual Voltage Tracking Regulator, 2501



200-48

Figure 5-37. Operational Amplifier, LM308

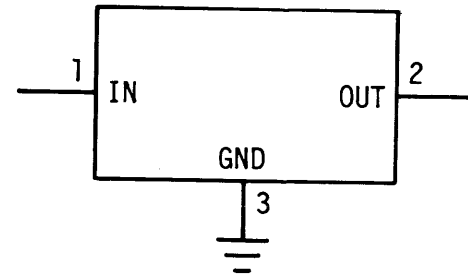


Figure 5-38. Voltage Regulator, MC 7815C

200-49

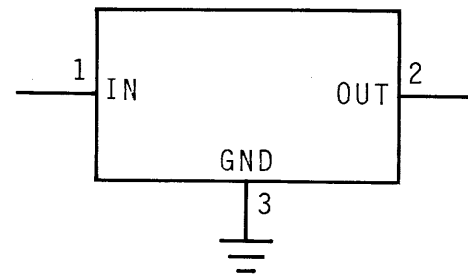


Figure 5-39. Voltage Regulator, MC 7915C

200-50

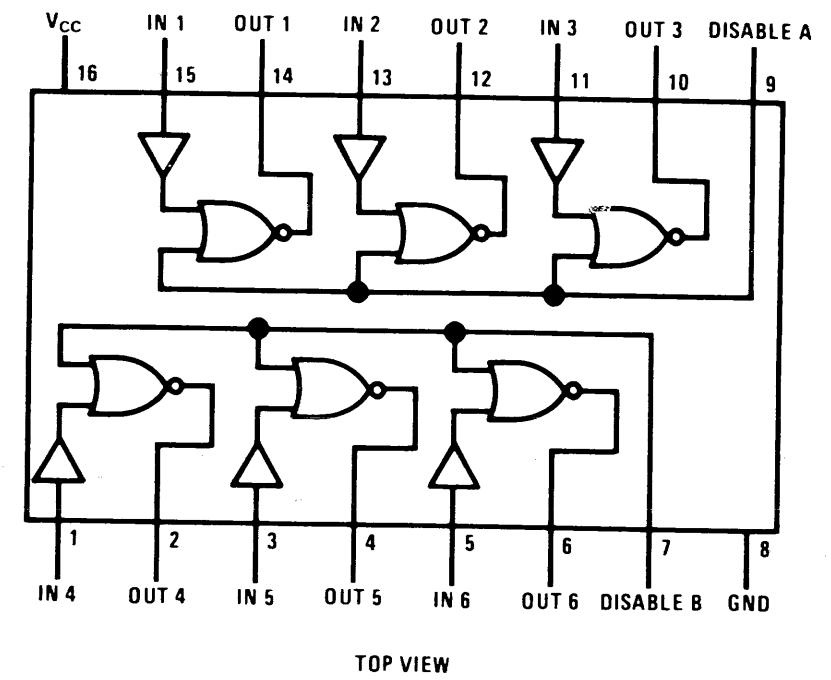


Figure 5-40. Hex Unified Bus Receiver, DM 8837

200-51

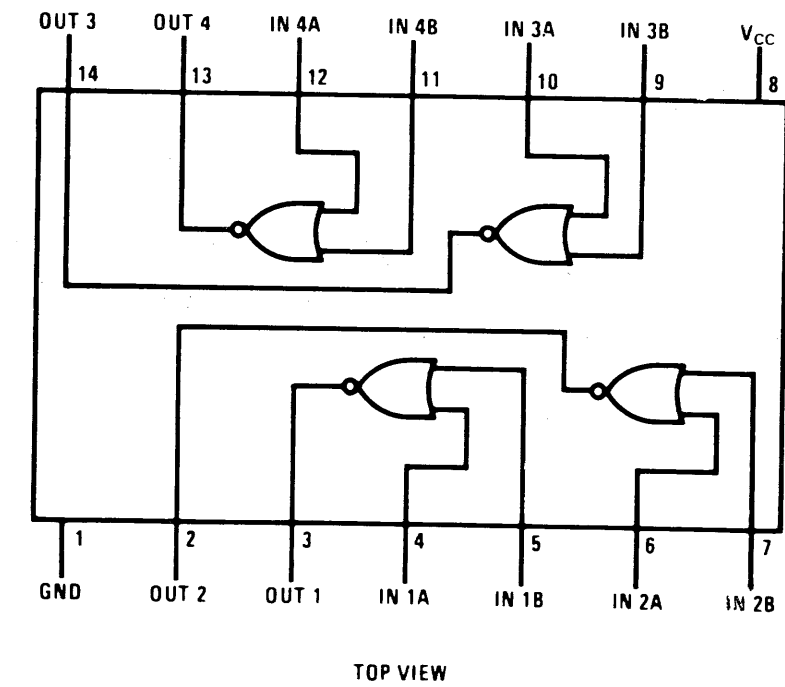


Figure 5-41. Quad 2-Input Nor Gate, DM8836N

200-52

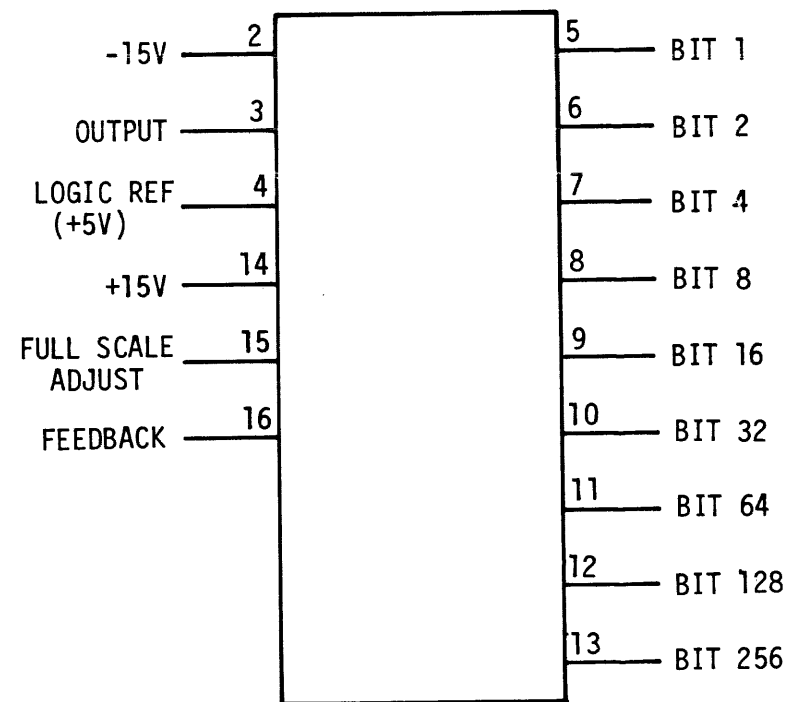


Figure 5-42. D/A Converter - 10 Bit Miniature, DAC100

200-53

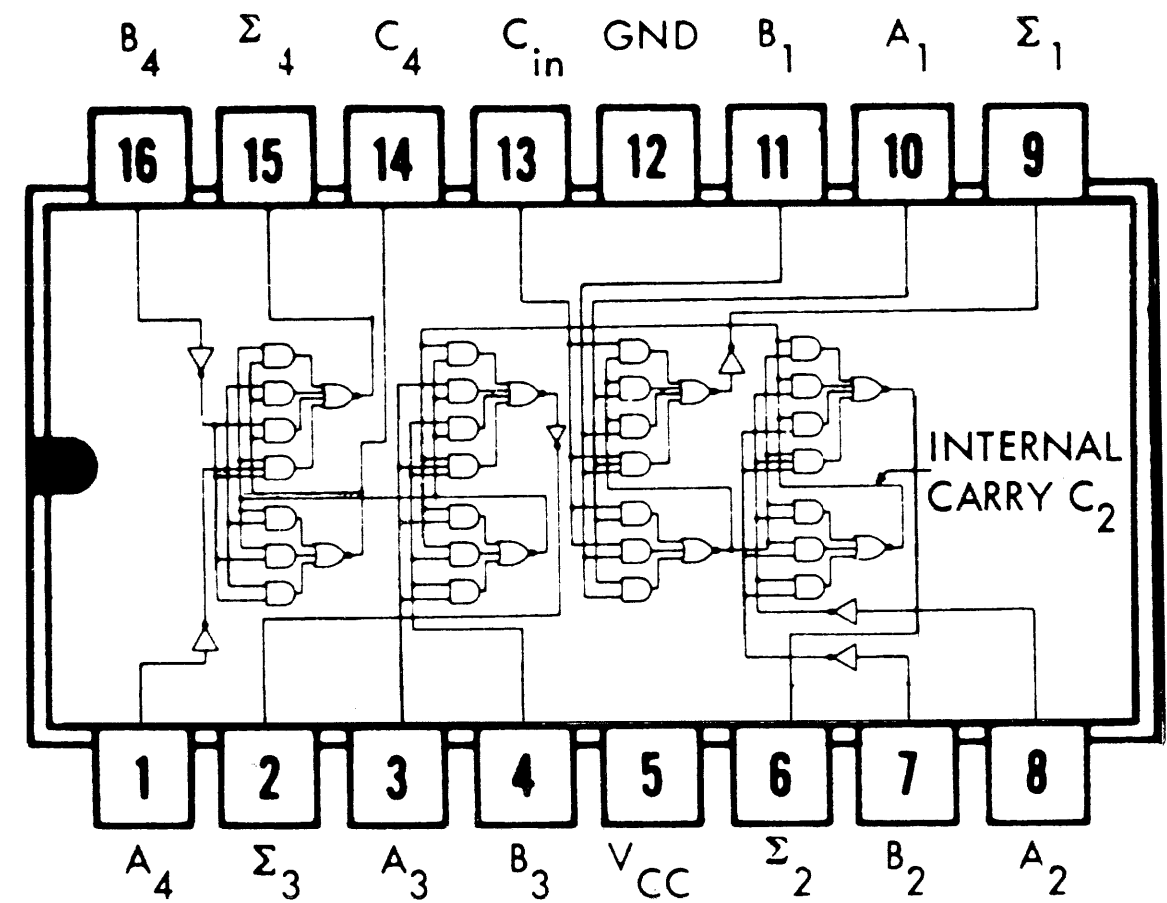
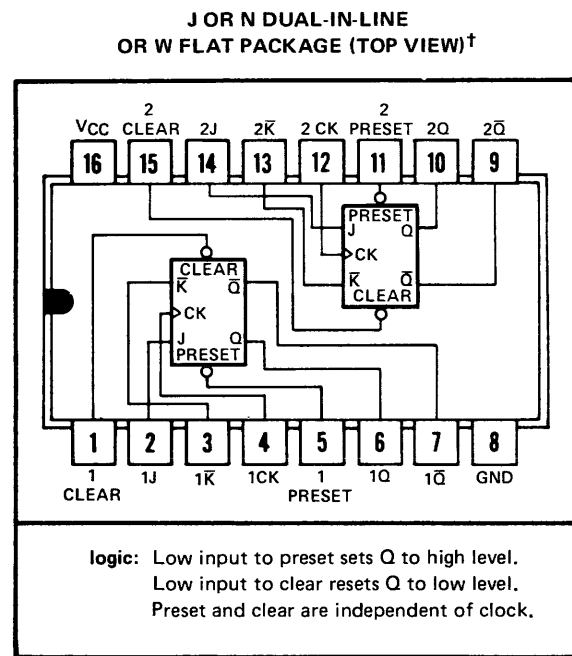
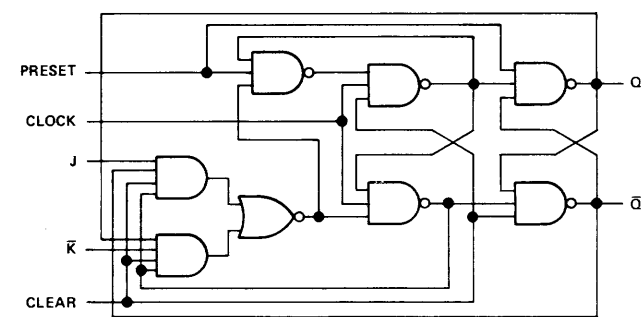


Figure 5-43. 4-Bit Binary Full Adders, SN7483

200-54

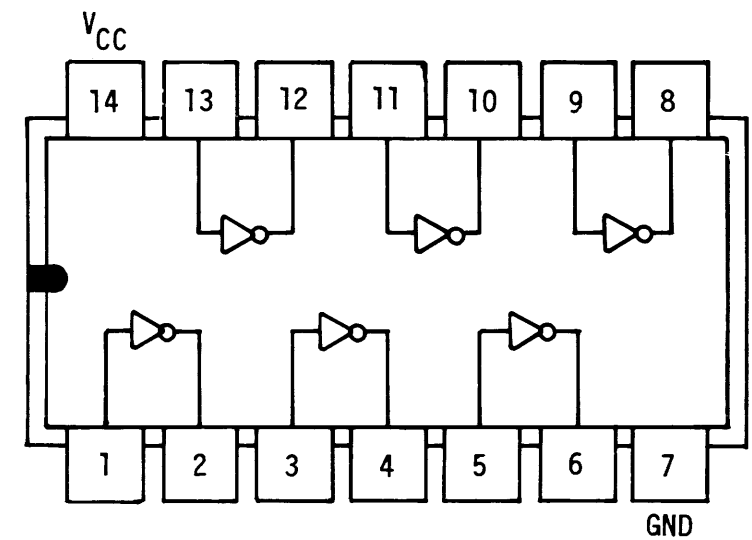


functional block diagram (each flip-flop)



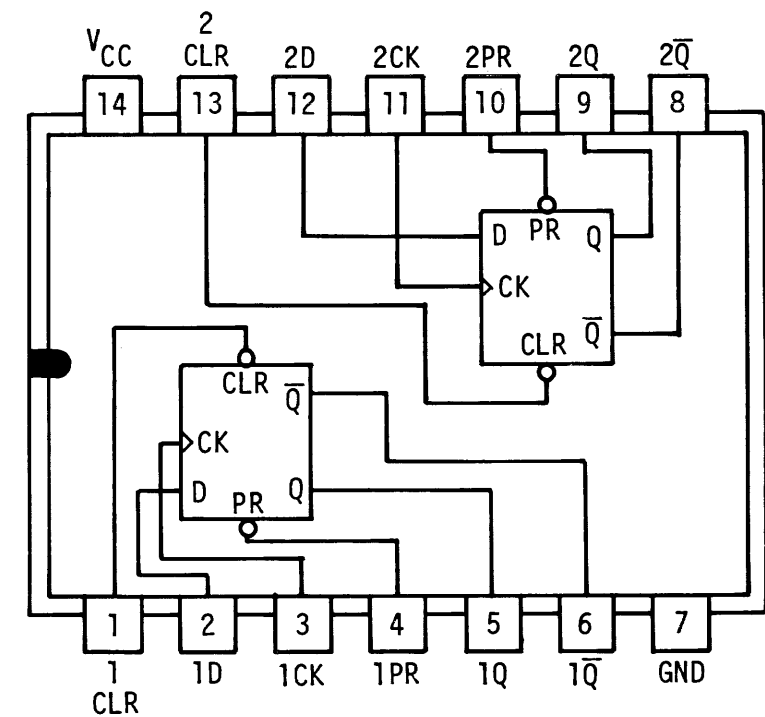
200-55

Figure 5-44. Dual J-K Positive-Edge-Triggered Flip Flop, SN74109



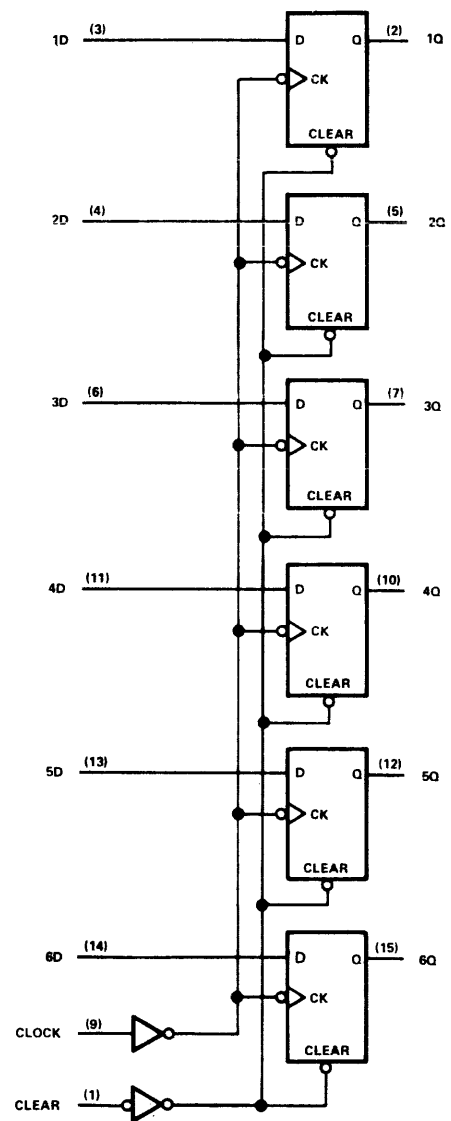
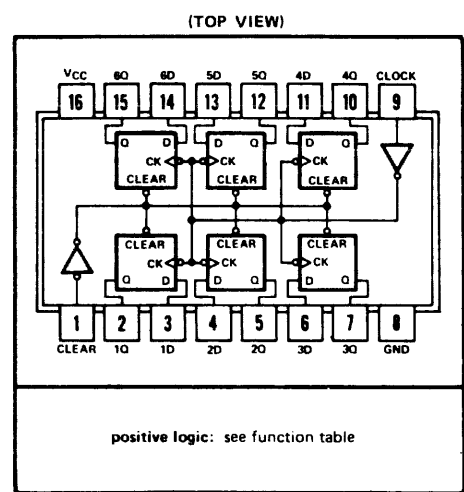
200-56

Figure 5-45. Hex Inverter, SN74H04



200-57

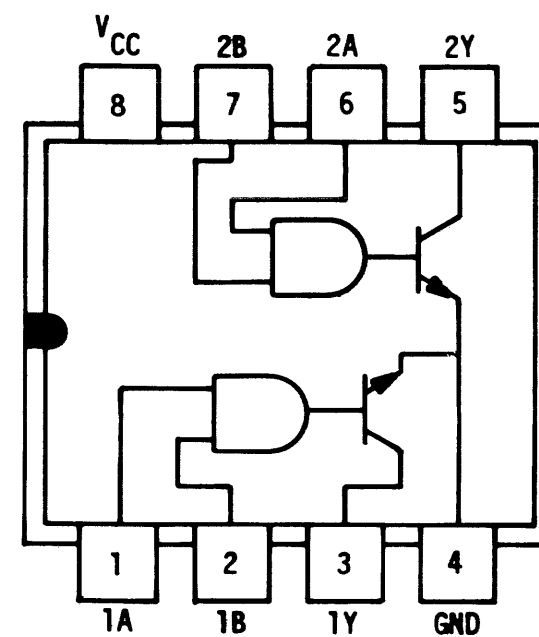
Figure 5-46. Dual D-Type Positive-Edge-Triggered Flip Flop with Preset and Clear, SN74H74



 . . . dynamic input activated by transition from a high level to a low level.

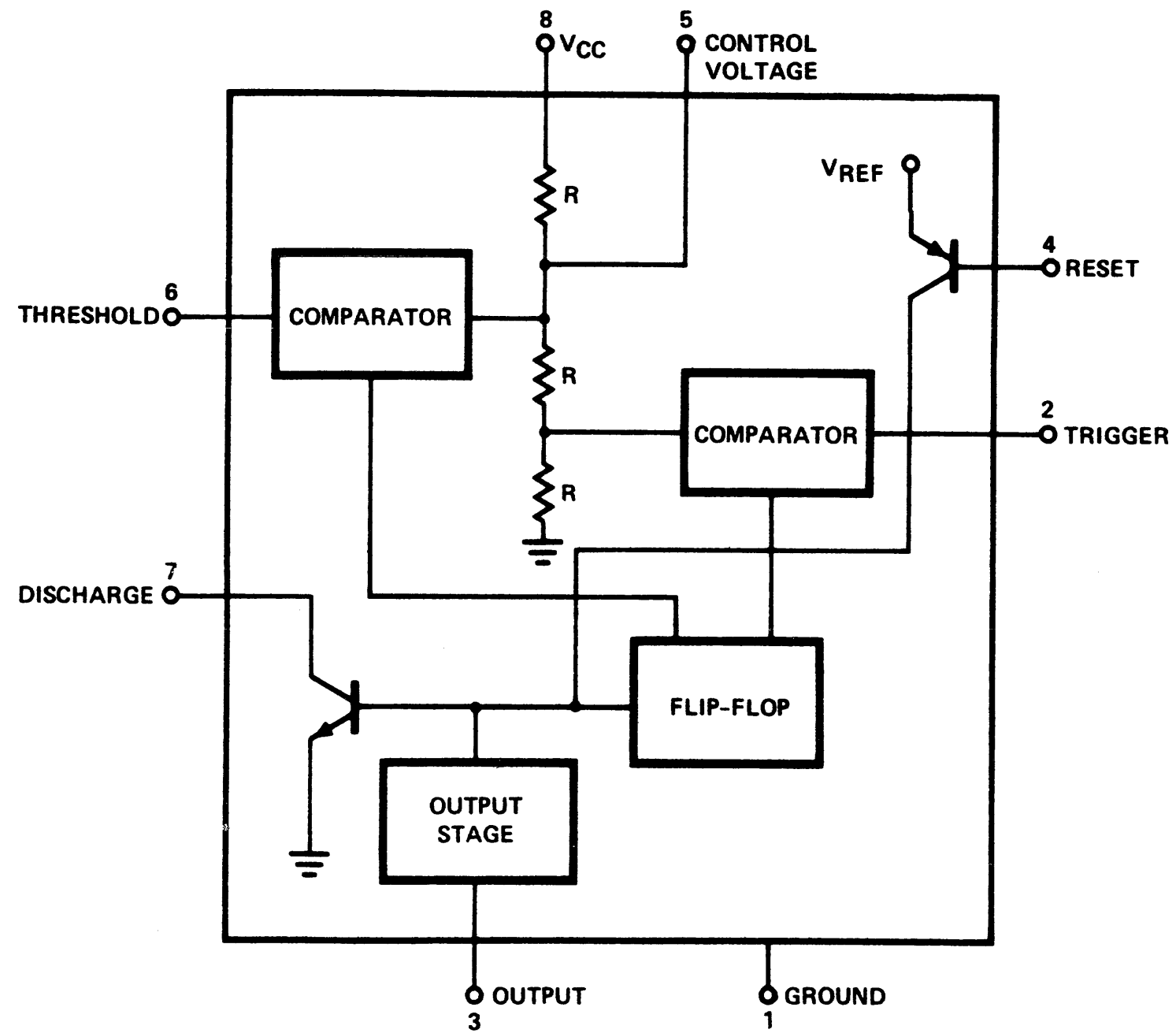
200-58

Figure 5-47. Hex/Quadruple D-Type Flip Flop with Clear, SN74174



200-59

Figure 5-48. Dual Peripheral Positive-Nand Driver



200-60

Figure 5-49. Timer, 555

5.4.12 100 TPI Differences & Circuits

The 206 drive has the built in capability of being utilized as a 100 TPI disk drive with a capacity of 6 megabytes if both fixed and removable disks are utilized. Without a fixed disk installed the capacity of this configuration is 3 megabytes. There are five differences in the 100 and 200 TPI versions of this disk drive. These differences are:

- a. Heads (100 TPI heads utilized, see your TACD for part numbers).
- b. Read/Write board (100 TPI R/W board installed).
- c. Temperature compensation (TP3 and TP6 on TCB jumpered to ground).
- d. I/O board jumpering (jumper E12 to E13, half capacity).
- e. I/O cable configuration (see 100 TPI column of Table 2-2).

The following sections are explanations of the 100 TPI, 1500 rpm and 2400 rpm R/W boards.

5.4.12.1 Read/Write Amplifier (R/WA) 2,400 rpm

The R/WA provides the circuitry necessary for the recording and recovery of data. Circuits contained on the R/WA include Head/Disk Select, Write Inhibited, the Write Amplifier, Read Preamp-lifier, and Signal Conditioning yielding double-frequency read data. (See Figure 5-50).

a. Head/Disk Select Circuit

The Read/Write winding of each head is connected across pins 1 and 4 of its connector, and its center-tap is connected to pin 3. Pins 1 and 4 from the read/write winding of each head are connected to two common Read/Write lines via diodes. The DC erase winding is connected across pins 2 and 3.

The head selection for the read or write function is performed by turning on the particular transistor (Q1 through Q4) connected to the center-tap of the selected head. One and only one head can be turned on at any given time.

The notations for the Head Select and Disk Select signals at zone D8 are indicated as being positive when true. In other words, if Head Select Bottom (+) was at ground level, the top head of the selected disk would be enabled.

b. Write Inhibit Circuit

The Write Inhibit circuit consists of Q22 and Q23 (optional) located at coordinates C6 in Figure 5-50. The output of Q22 switches the Write Inhibited, WRT INHBD (-), status line to ground whenever a write operation is being performed on a disk whose Write Inhibit switch is turned on.

There are several jumper configurations that can be applied to the Write Inhibited circuit. If jumper A to C is installed, Q22 is turned on when the Write Inhibit switch for the selected disk is on. (This is independent of a write operation). Q22 is turned on because the output of IC 2-6 is high when the Write Inhibit switch for the selected disk is on. Turning on Q22 provides a ground level to the WRT INHBD (-) line.

If jumper B to C is installed, Q22 is controlled by the state of the Write Inhibit switches at IC 4-8 at D6 on the schematic, or by WRT INHB (+) at IC 4-9. The latter signal is the inversion of Controller-generated Write Enable. The composite output, IC 4-10, controls Q5, located at C5 on the schematic. During a normal write mode, Q5 is on which turns Q22 off. Q5 is also a driver of constant write current source Q9. Hence,

when the drive is Write Inhibited, no current is flowing in the Write Amplifier. During this condition, the Write Data flip flop will be held reset. In summary, with B and C jumpered, the Controller knows that when Write Inhibited is true, the Write Amplifier is off because either the Write Inhibit switches are active, or Write Enable is false.

If jumper 1 to 2 is installed, Q23 is allowed to turn off Q22 if the Controller is not performing a write operation. This prevents the write inhibited status from being true when not writing and is provided for those Controllers that inhibit the write operation if the status line is low prior to writing.

c. Write Circuit

The Write circuit consists of IC 7, Q10, Q11, Q12 and Q13. Any time a write operation takes place, an erase function is also performed. The erase function performed is a tunnel erase which limits the width of the written track. The erase driver transistor, Q14, located at coordinates E5 will be discussed with the Write circuit.

The Write Enable signal is located at coordinates D6 and is the output of IC 4-10. When this signal is positive, the write operation is enabled. The inputs on IC's 4-8 or 4-9 inhibit the write operation when high. The input on IC 4-9 is developed on the DEM and is a combination of Write Enable from the Controller and Seek Complete. The input on IC 4-8 is the output of IC 2-6 and can also inhibit the write operation from being performed. This signal is developed by Anding the Write Inhibit switch with the Disk Select line on IC 2. In other words, the write operation will only take place as long as the Write Inhibit switch for the selected disk is not turned on, the Controller is commanding a write operation, and the drive is not performing a Seek operation.

The output of IC 4-10 is simultaneously applied to three circuits. One circuit (Q14) is located at coordinates F5 in Figure 5-50. The positive output from IC 4-10 turns on Q14 after a 14-microsecond delay produced by C9, C10, and R37. Once Q14 is turned on, erase current is applied to pin 2 of the selected read/write head. This DC erases a 0.003-inch zone on both sides of the written track. The 14-microsecond delay is necessary because of the physical displacement between the write and erase coils.

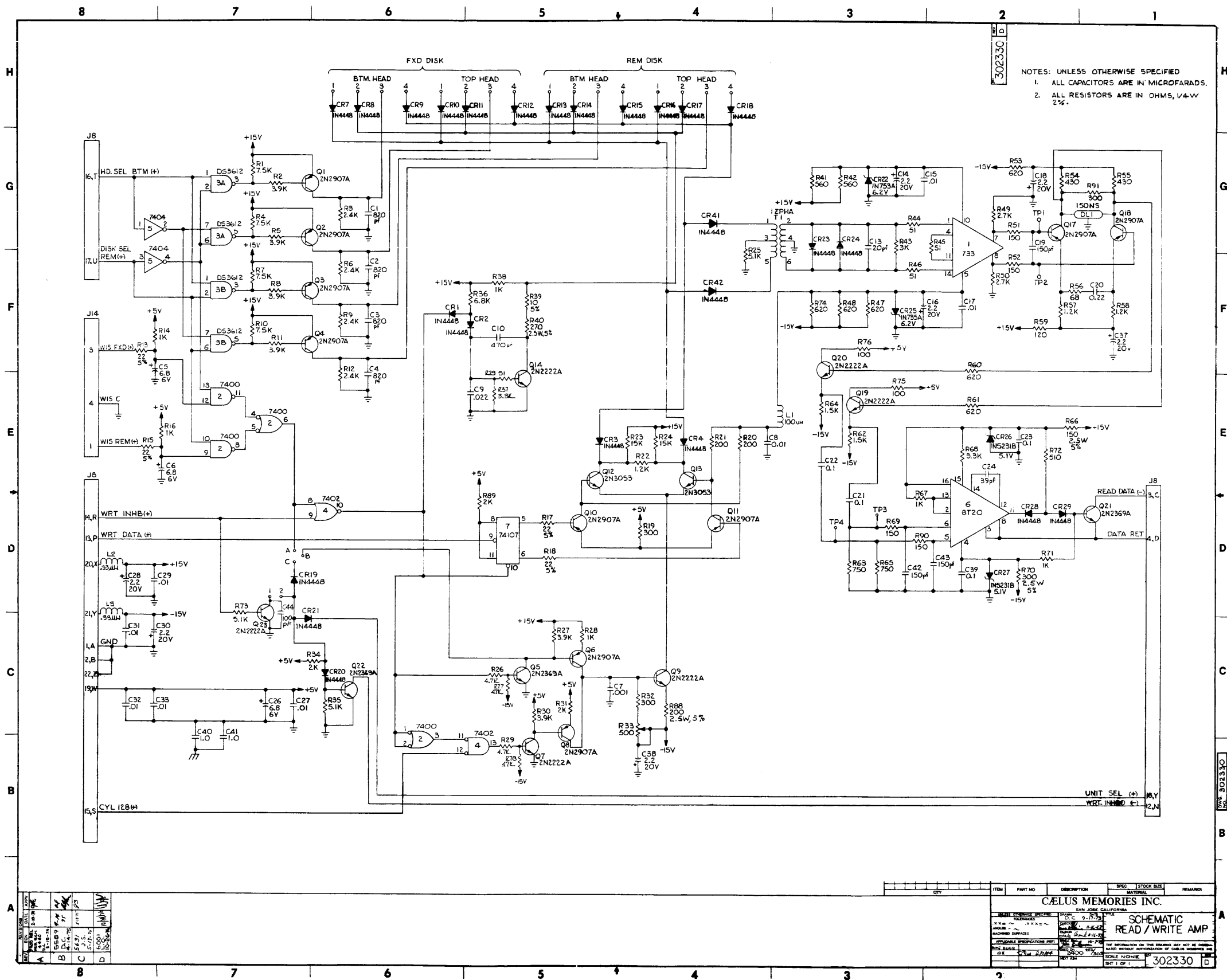


Figure 5-50. Read/Write Amplifier (R/WA) 2,400 rpm

The positive output of IC 4-10 is also applied to the master reset of the Write Data flip flop, IC 7-10. This flip flop toggles as the write data, which are in double-frequency format, are applied to the clock input at IC 7-9. As IC 7 toggles, switch transistors Q10 and Q11, which are connected in push-pull, alternately turn on and off. Current drivers Q12 and Q13 feed current through each half of the read/write coil alternately, in relation to the data. When zeros are being written, the direction of current through the read/write coils is reversed every 400 nanoseconds. When ones are being written, this change occurs every 200 nanoseconds.

The current source of Q12 and Q13 is transistor Q9. This transistor is also controlled by the output of IC 4-10. The output of IC 4-10 is applied to pins 1 and 2 of IC 2 and is inverted through IC 2. Therefore, the input of IC 4-11 will be low when a write operation is being performed. This Write signal is Anded with CYL 128 (+) on IC 4-12, allowing a high output from IC 4-13 when a write operation is being performed on cylinders 0 through 127. Q5 being turned on turns on Q6 which, in turn, turns on Q9. Q9 then supplies write current to current amplifiers Q12 and Q13.

When writing on cylinders less than 128, IC 4-13 being high turns on Q7 which turns on Q8, supplying 14 percent more write current while writing cylinders 0 through 127 than on cylinders 128 through 203. This is necessary because of the higher optimum record-current at the lower bit-packing density on the outer diameter.

d. Read Circuit

The Read circuit consists of T1, IC 1, IC 6, and Q17 through Q21 located at coordinates G2 and G3 through E2 and E3 in Figure 5-50.

The rotational movement of the disk passing under the selected read/write head induces a voltage into the read/write coil which is applied across read transformer T1 via its forward-biased selector diodes. The secondary of T1 drives preamplifier IC 1 where the signal is amplified. The preamplifier output can be monitored on test points 1 and 2. TP1 is used while aligning the read/write heads and is a primary troubleshooting test point.

During a write operation, TP1 should measure from 6 to 8 volts peak-to-peak. During a read operation, the minimum amplitude from any read/write head as measured on TP1 or TP2 is 80 millivolts for 100 microseconds. (This amplitude measurement is taken at track 203).

The outputs at pins 7 and 8 of preamplifier IC 1 are filtered and applied to differentiators Q17 and Q18 which drive emitter followers Q19 and Q20. The AC coupled outputs of Q19 and Q20 are filtered and applied to the input pins 5 and 6 of IC 6, which is used as a zero-crossing detector. IC 6 gives a one shot output pulse for each axis-crossing of the amplified differentiated waveform from the head, thereby functioning as a peak detector.

The output of IC 6 drives line driver Q21. Q21 provides digital double-frequency read data. If Controller design dictates, these double-frequency data must be applied to the Data Translator Board prior to being sent to the Controller. The Data Translator board converts the double-frequency data to the proper format. The most common format is NZR.

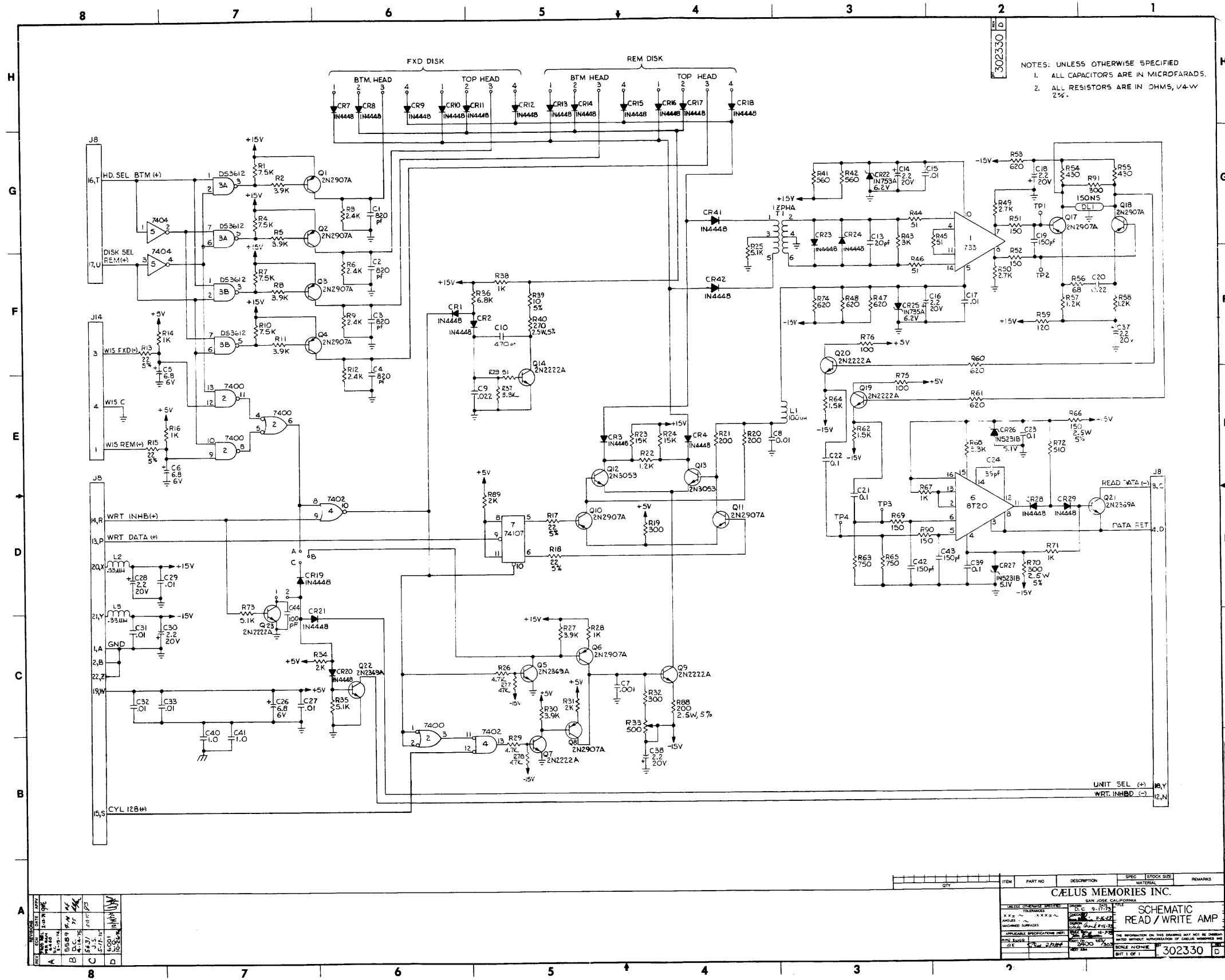


Figure 5-50. (Repeat) Read/Write Amplifier (R/WA) 2,400 rpm

5.4.12.2 Read/Write Amplifier (R/WA) 1,500 rpm

The Read/Write Amplifier provides the circuitry necessary for recording and recovery of data and consists of the following functions: Head/Disk Select, Write Inhibited, Write Amplifier, Read Preamplifier and Signal Conditioning, yielding double-frequency read data. (See Figure 5-51).

a. Head/Disk Select Circuit

The Head/Disk Select circuit consists of IC's 1 and 2, and Q1 through Q4, located at coordinates F6 in Figure 5-51. The Head Select and Disk Select signals are gated by IC's 1 and 2 such that only one of the four head select transistors, Q1 through Q4, is turned on at any one time, causing head current to flow through the appropriate head.

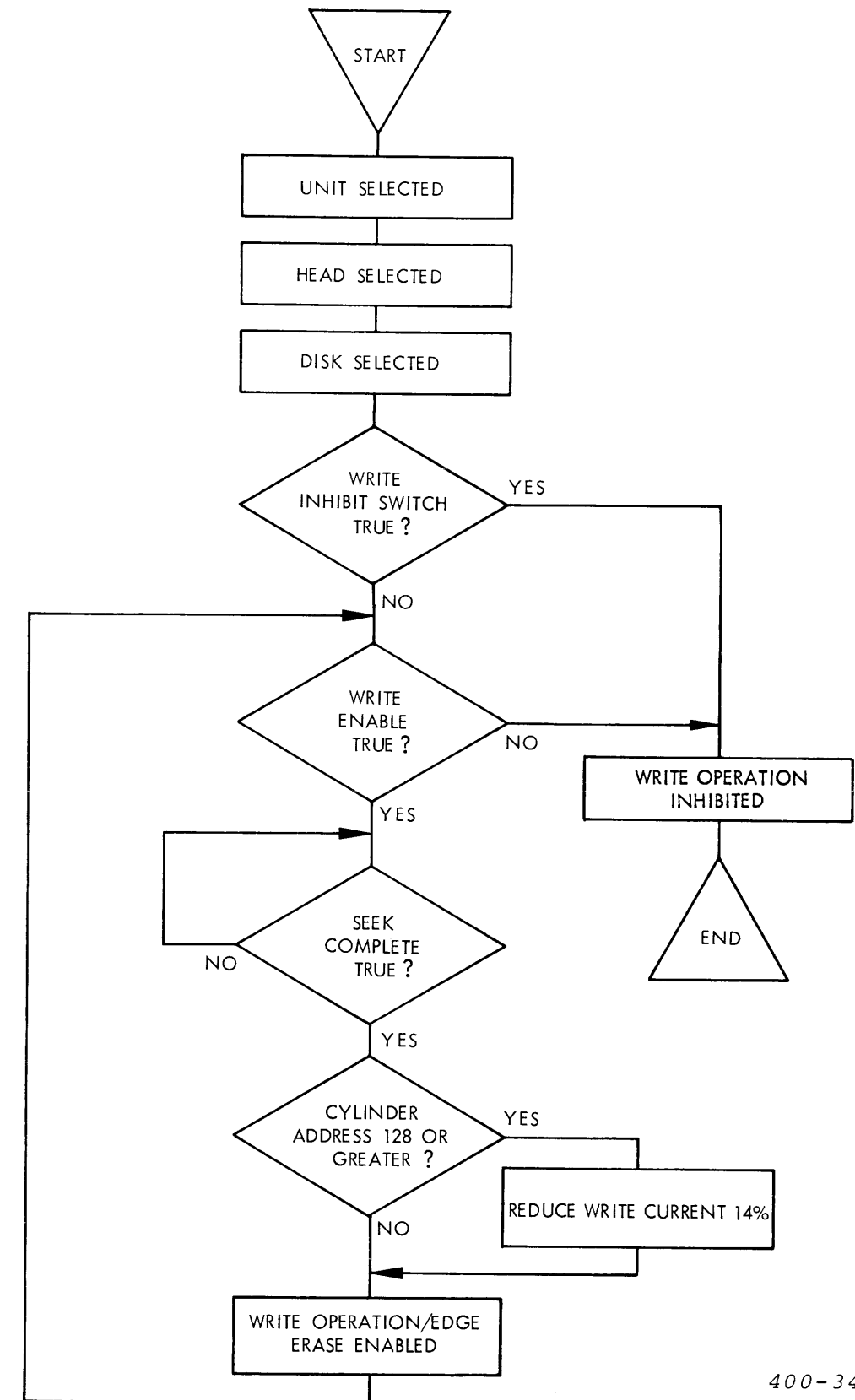
b. Write Inhibit Circuit

The Write Inhibit circuit consists of IC's 1 and 7 and Q17 located at coordinates C6 in Figure 5-51. An operational flow chart is shown in Figure 5-52. It becomes operational when the write function is inhibited for any of the following reasons:

1. The Write Inhibit switches are inadvertently disconnected.
2. A Write Inhibit switch is turned on and the corresponding disk is selected.
3. The negation of Write Enable signal from the Controller, WRT INHB (+), is true.
4. The carriage is not settled on a track.

When any of these conditions exists and Unit Select is true, transistor Q17 turns on, providing a Write Inhibited signal, WRT INHB (-), to the Controller, J8-12.

For the -019 configuration of the R/W Amplifier, transistor Q18 is added to gate the Write Inhibited signal with the controller Write Enable, such that a valid Write Inhibited signal exists only during Write Enable.



400-34

Figure 5-52. Operational Flow Chart, Write Mode

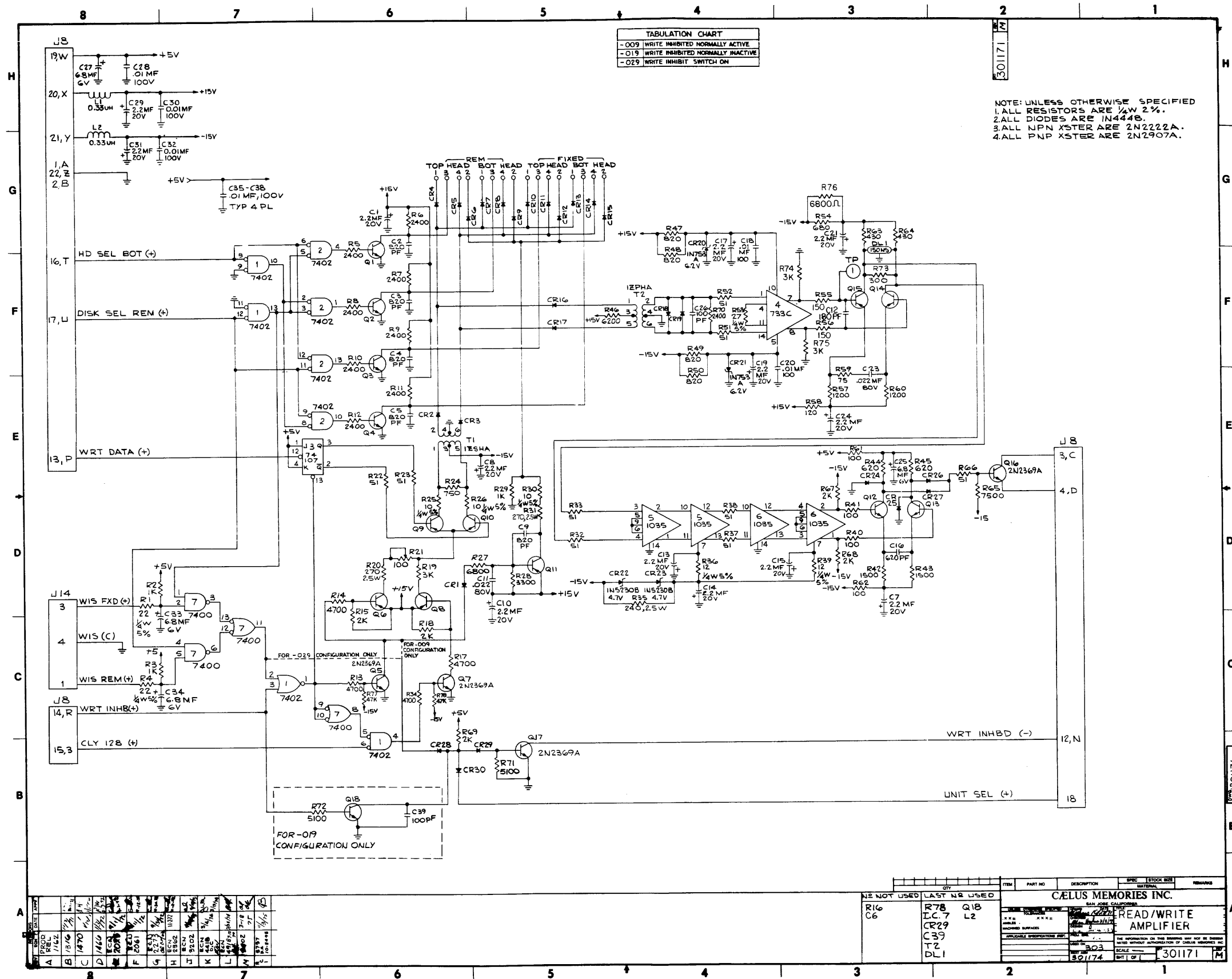
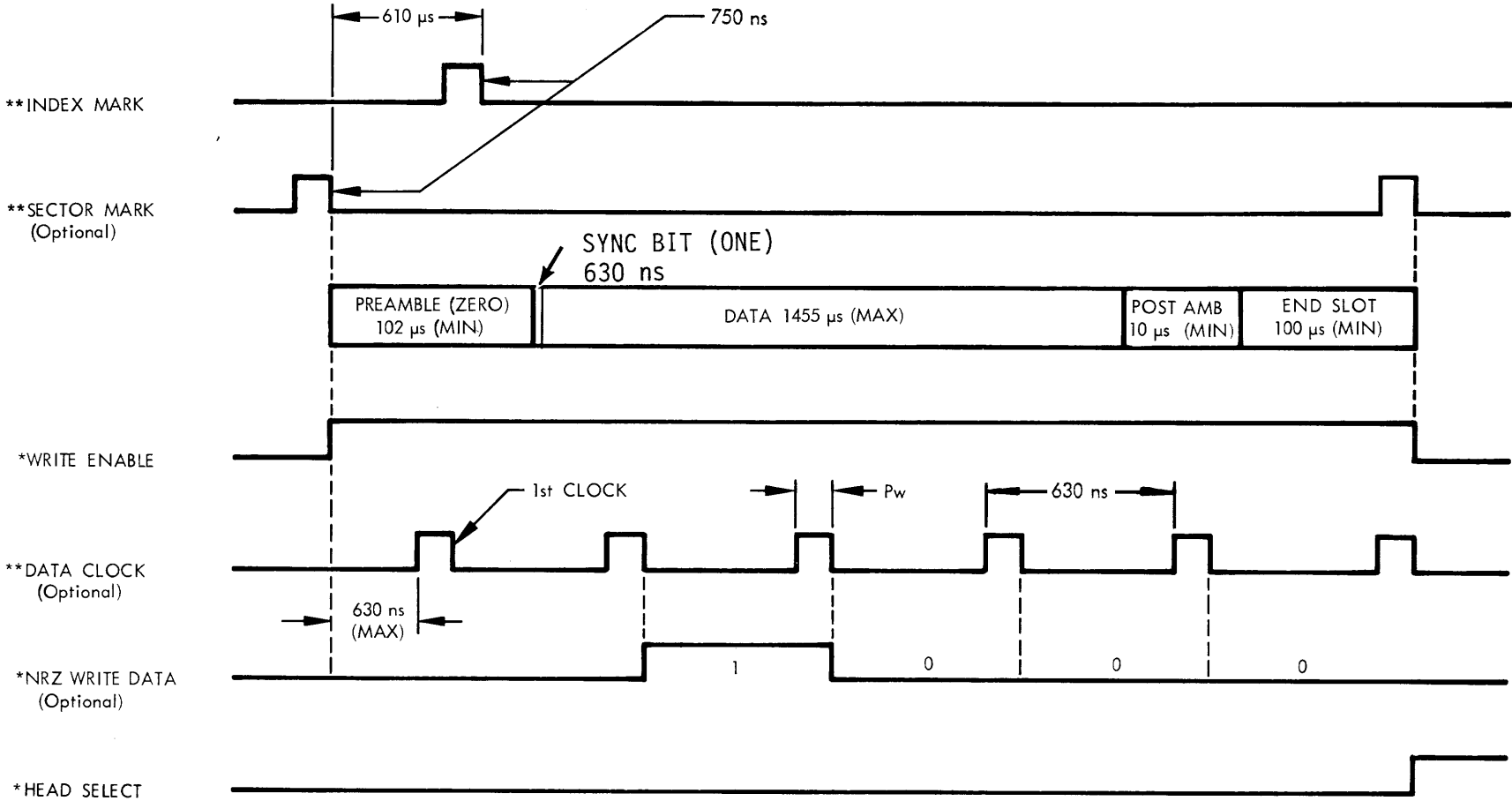


Figure 5-51. Read/Write Amplifier (R/WA) 1,500 rpm

c. Write Circuit

The Write circuit consists of the write flip flop (IC 3), the write and erase drivers (Q9, Q10, and Q11), and the Write Current Select circuit located at coordinates E6. Data to be recorded are supplied to the input of IC 3 in double-frequency format which drives the write amplifier, Q9 and Q10. The write amplifier is supplied current from Q6 and Q8 when writing tracks 0 to 127. When writing tracks 128 to 203, only Q6 supplies write current, reducing available current by 14 percent. Erase current is supplied by Q11. Turn-off of the erase current is delayed after the write operation ends by C11, R27, and R28. A timing diagram is shown in Figure 5-53.



NOTE:
 Data Transfer Rate: 1588.5 KHz
 2200 BPI
 1500 RPM
 24 Sector (Optional)
 1.667 ms per Sector

$$P_w = \frac{1}{4 \times \text{Data Transfer Rate}} \text{ (ns)}$$

*COMPUTER TO DRIVE
 **DRIVE TO COMPUTER

Figure 5-53. Timing Diagram, Typical Write Mode

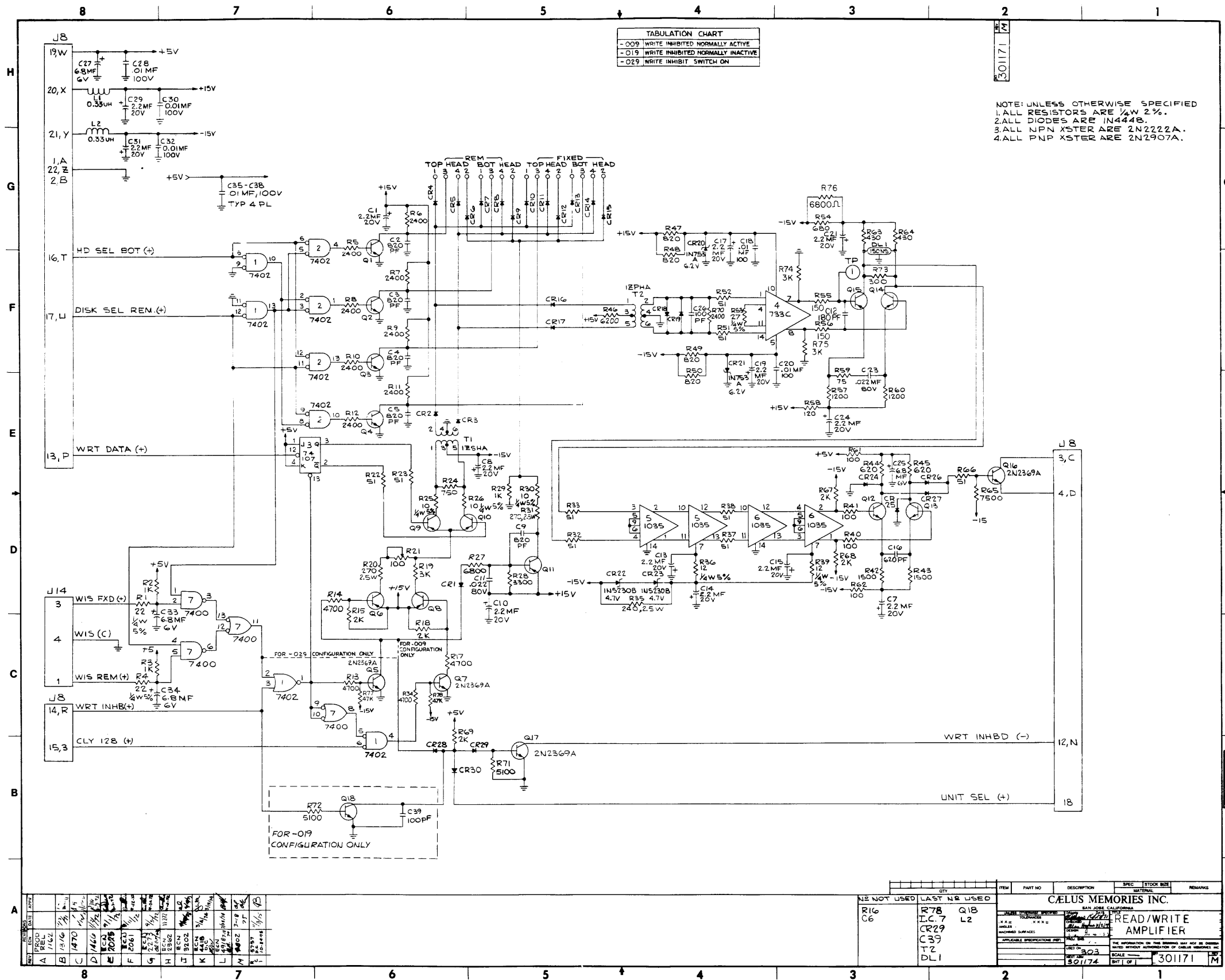
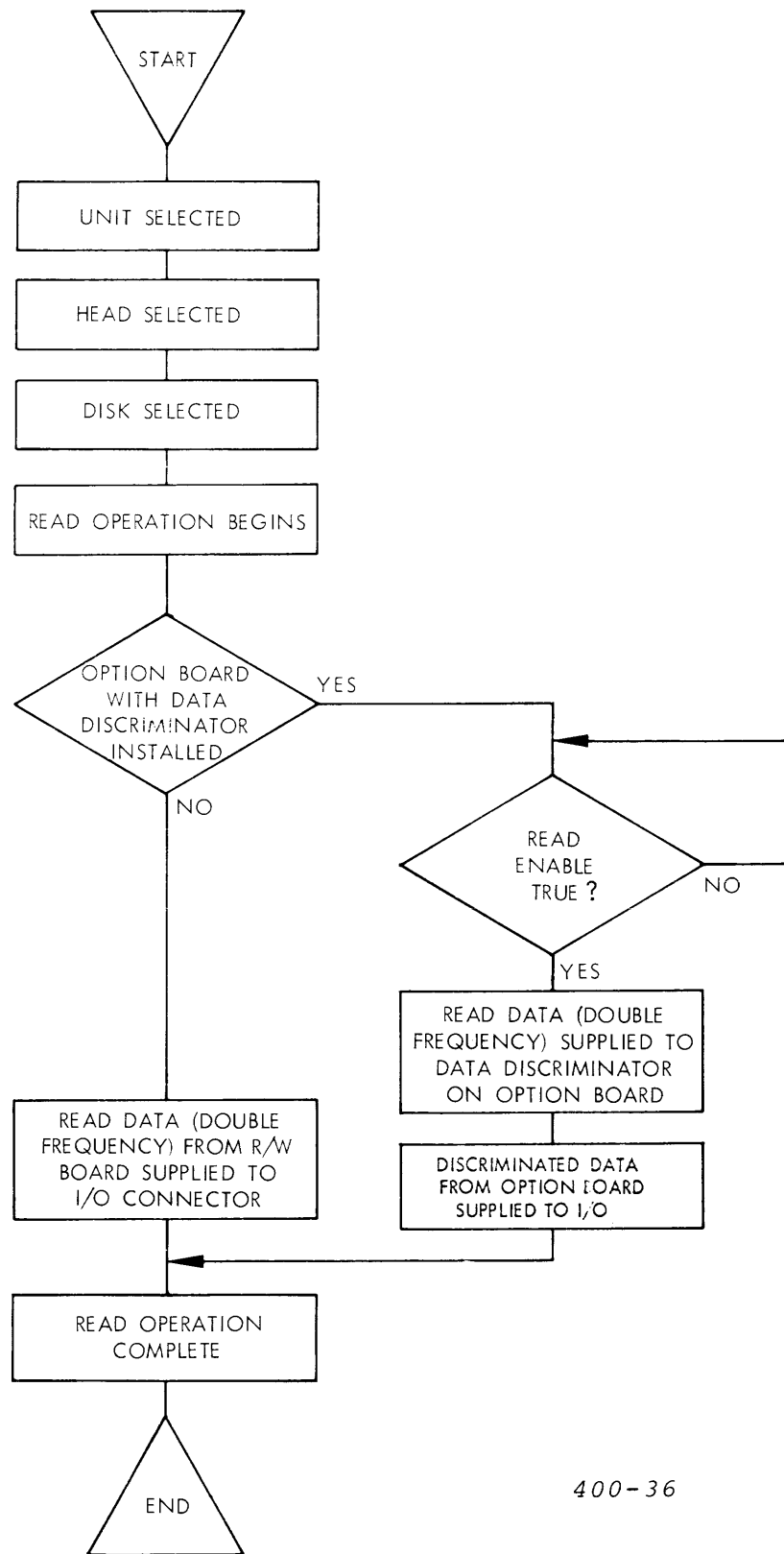


Figure 5-51. (Repeat) Read/Write Amplifier (R/WA) 1,500 rpm



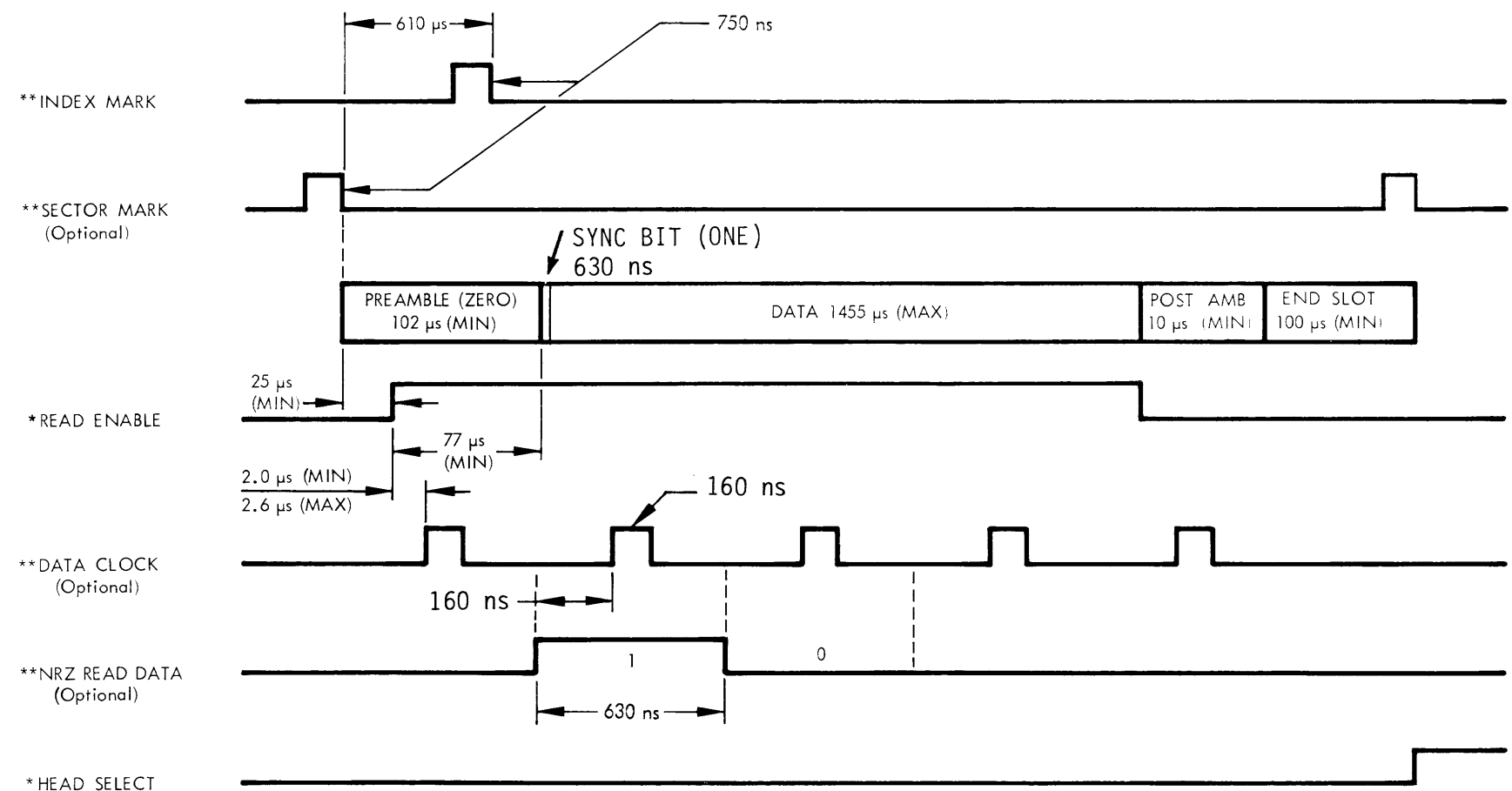
400-36

Figure 5-54. Operational Flow Chart, Read Mode

d. Read Circuit

The Read circuit consists of isolation transformer T2, diodes CR16 and CR17, preamplifier IC 4, differentiator Q14 and Q15, delay line DL1, and limiters IC 5 and IC 6 located at coordinates F3 and F4 through D3 and D4. Q12 and Q13 convert the limited signal to +5-volt logic, which is fed into line driver Q16. The output of the line driver (Q16) is double-frequency read data.

An operational flow chart for the read mode is shown in Figure 5-54; a timing diagram is shown in Figure 5-55.



NOTE:

- Data transfer rate 1588.5 KHz
- 2200 BPI
- 1500 RPM
- 24 Sector (optional)
- 1.667 ms per sector
- *COMPUTER TO DRIVE
- **DRIVE TO COMPUTER

400-37

Figure 5-55. Timing Diagram, Typical Read Mode

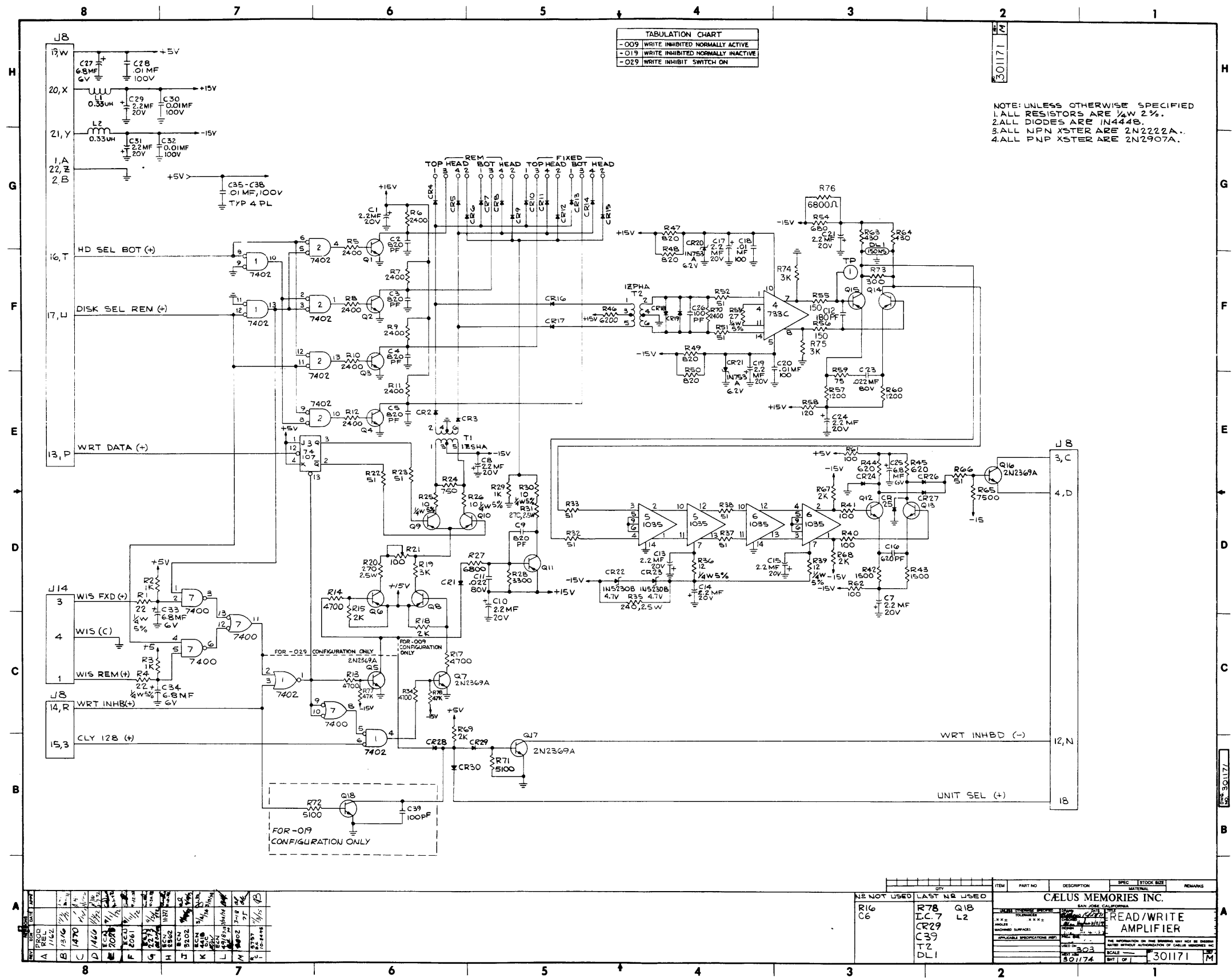
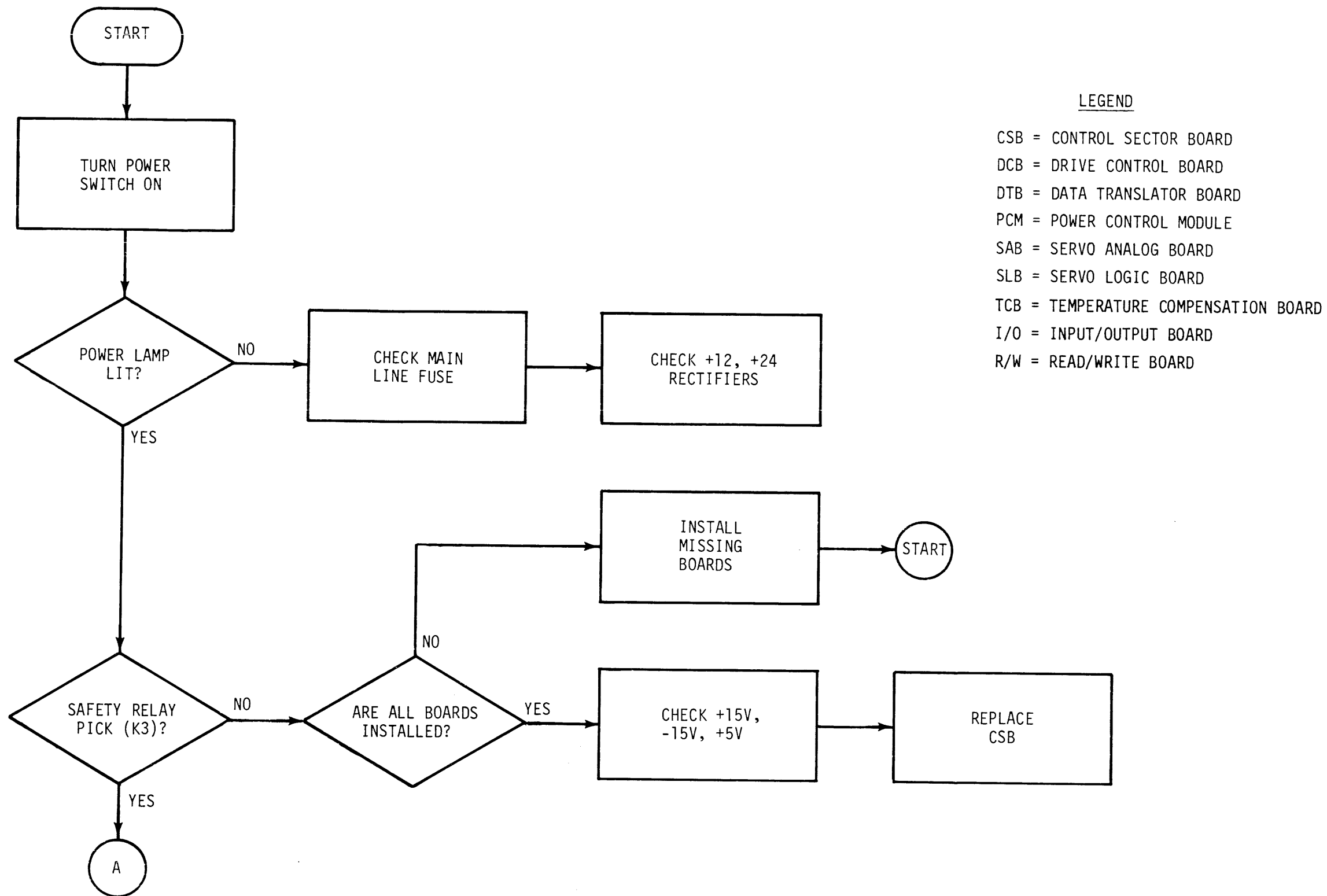


Figure 5-51. (Repeat) Read/Write Amplifier (R/WA) 1,500 rpm

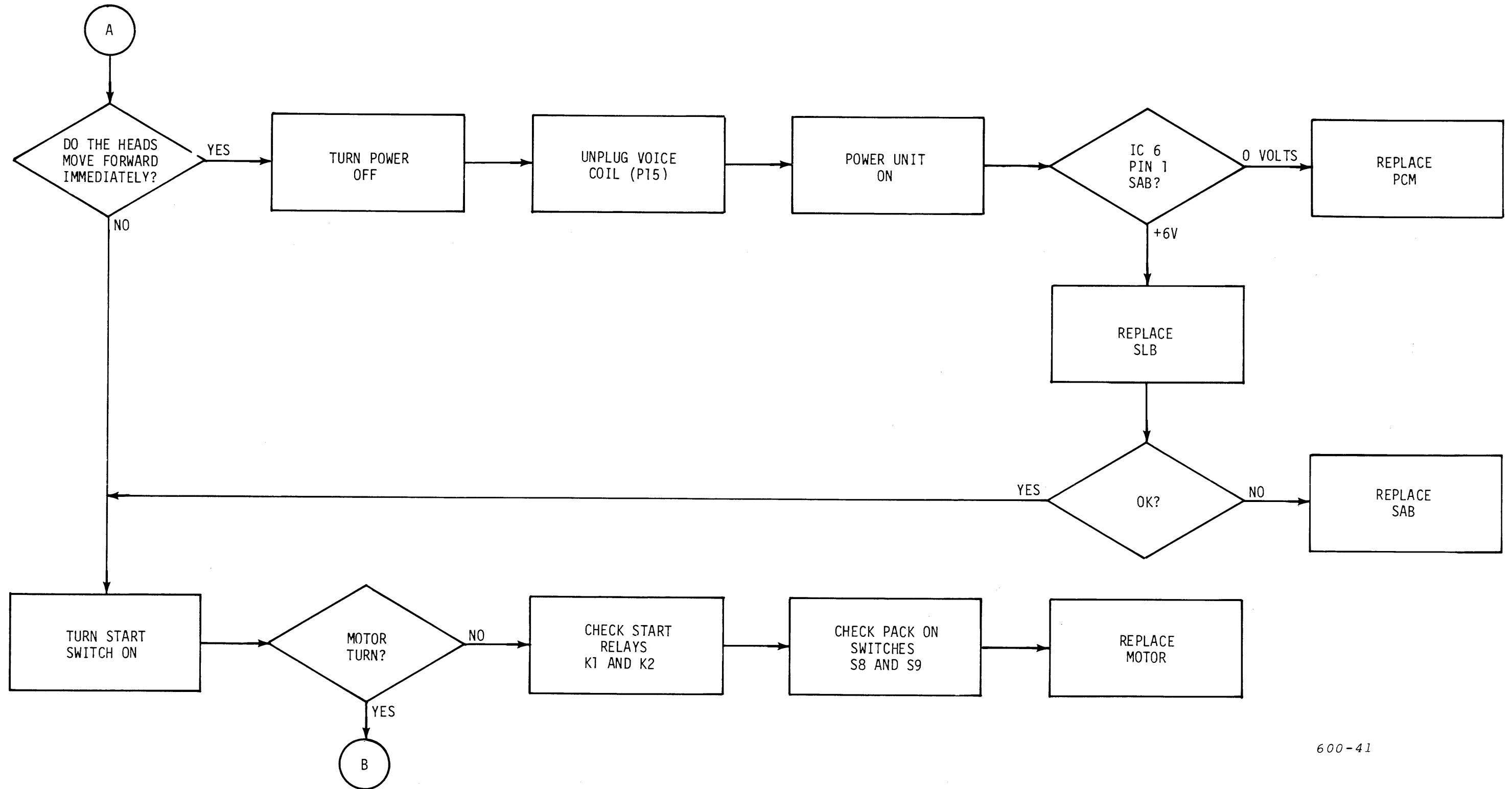
SECTION 6
TROUBLESHOOTING

This section consists of a troubleshooting flow chart to help the service engineer in isolating problems that may occur.



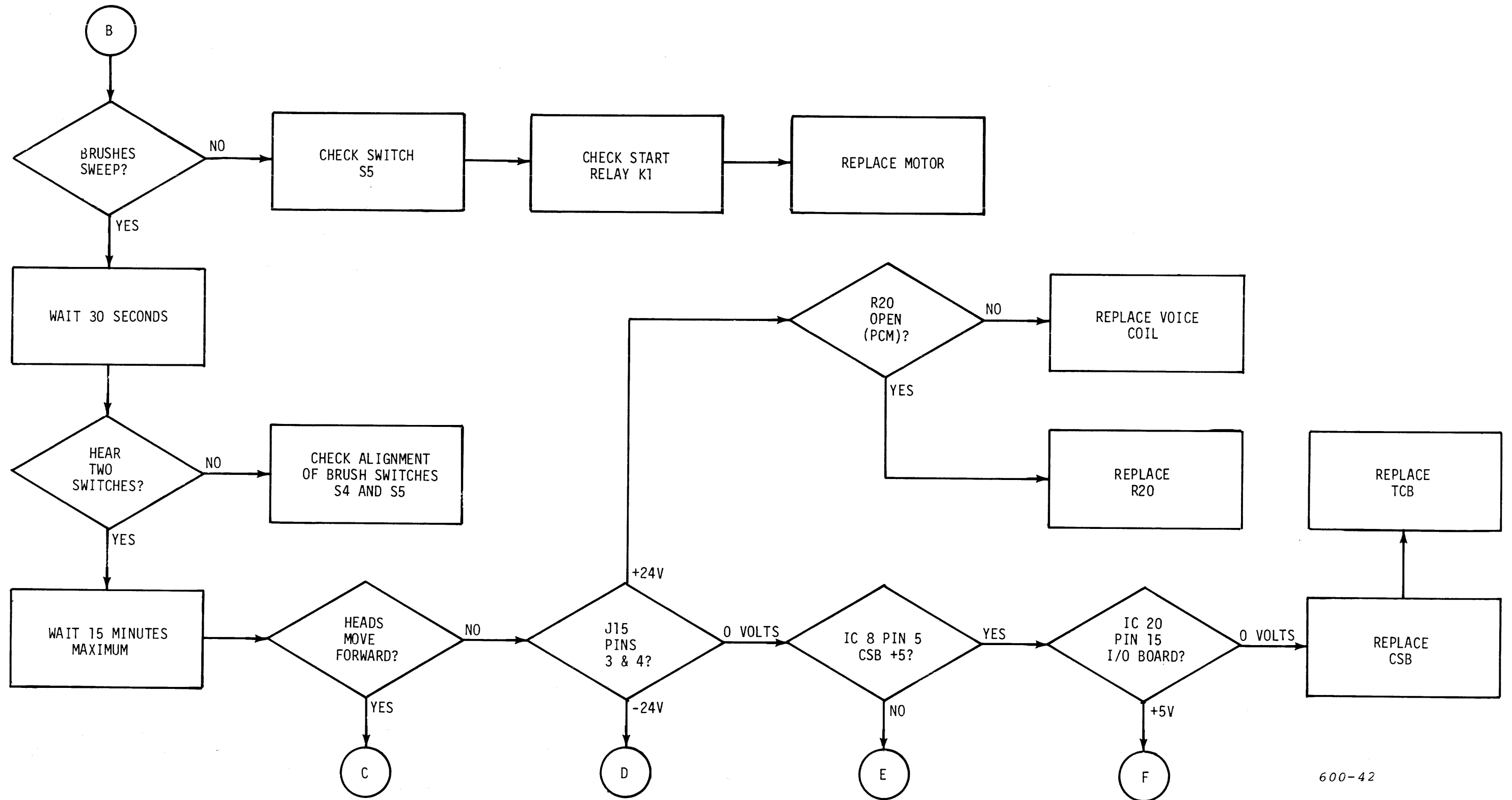
600-40

Figure 6-1. 306 Troubleshooting Flow Chart, Sheet 1 of 8



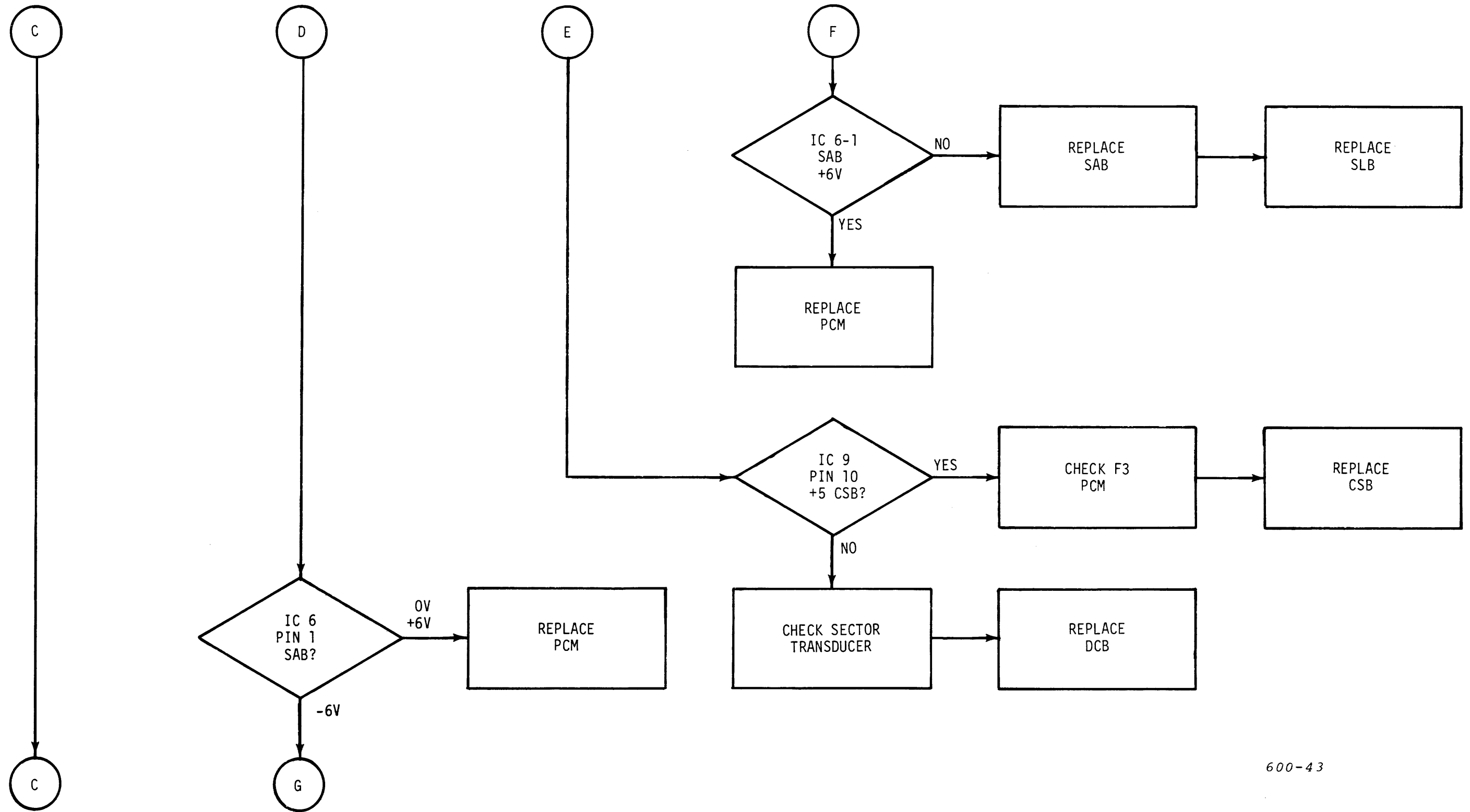
600-41

Figure 6-2. 306 Troubleshooting Flow Chart, Sheet 2 of 8



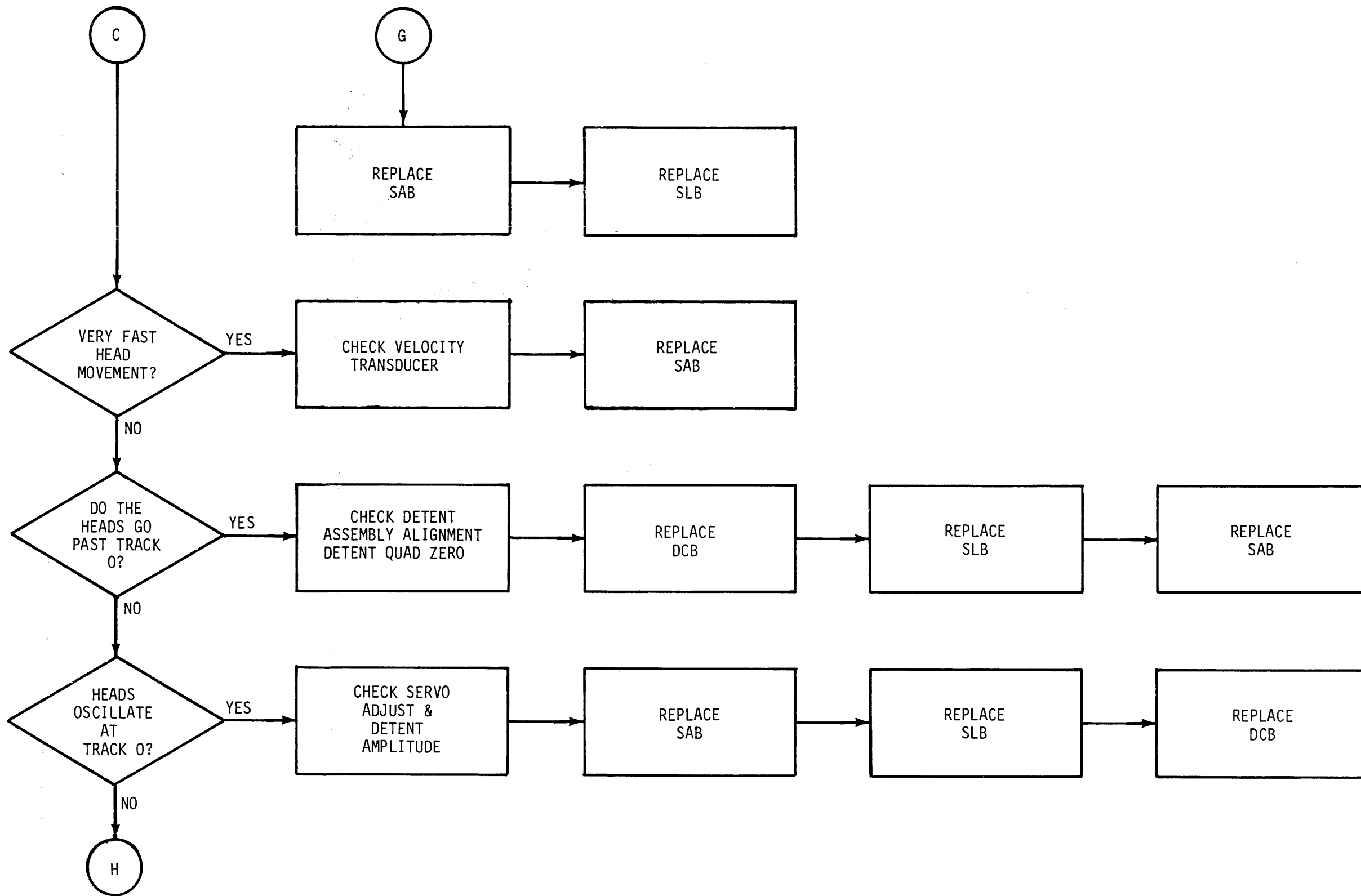
600-42

Figure 6-3. 306 Troubleshooting Flow Chart, Sheet 3 of 8



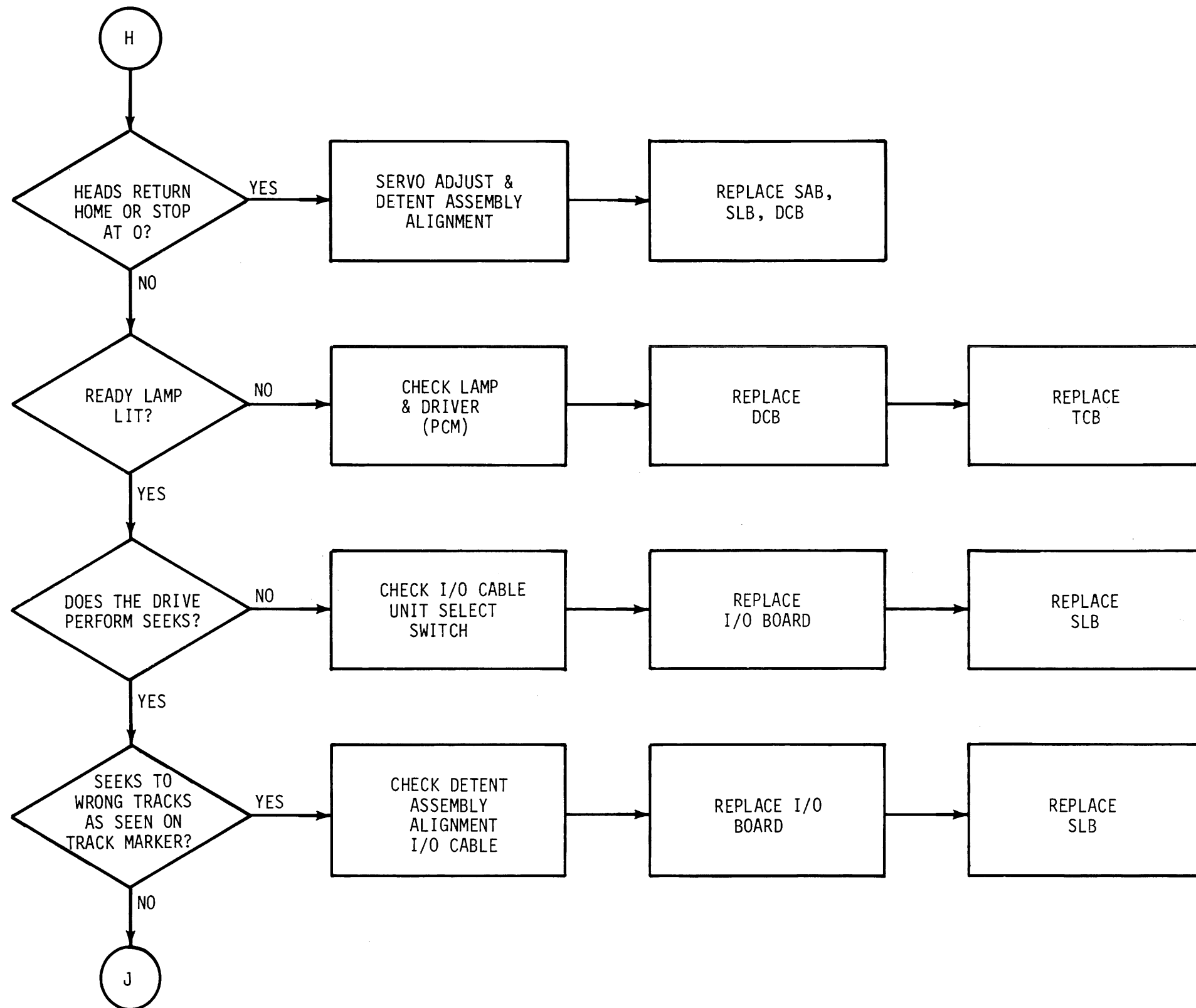
600-43

Figure 6-4. 306 Troubleshooting Flow Chart, Sheet 4 of 8



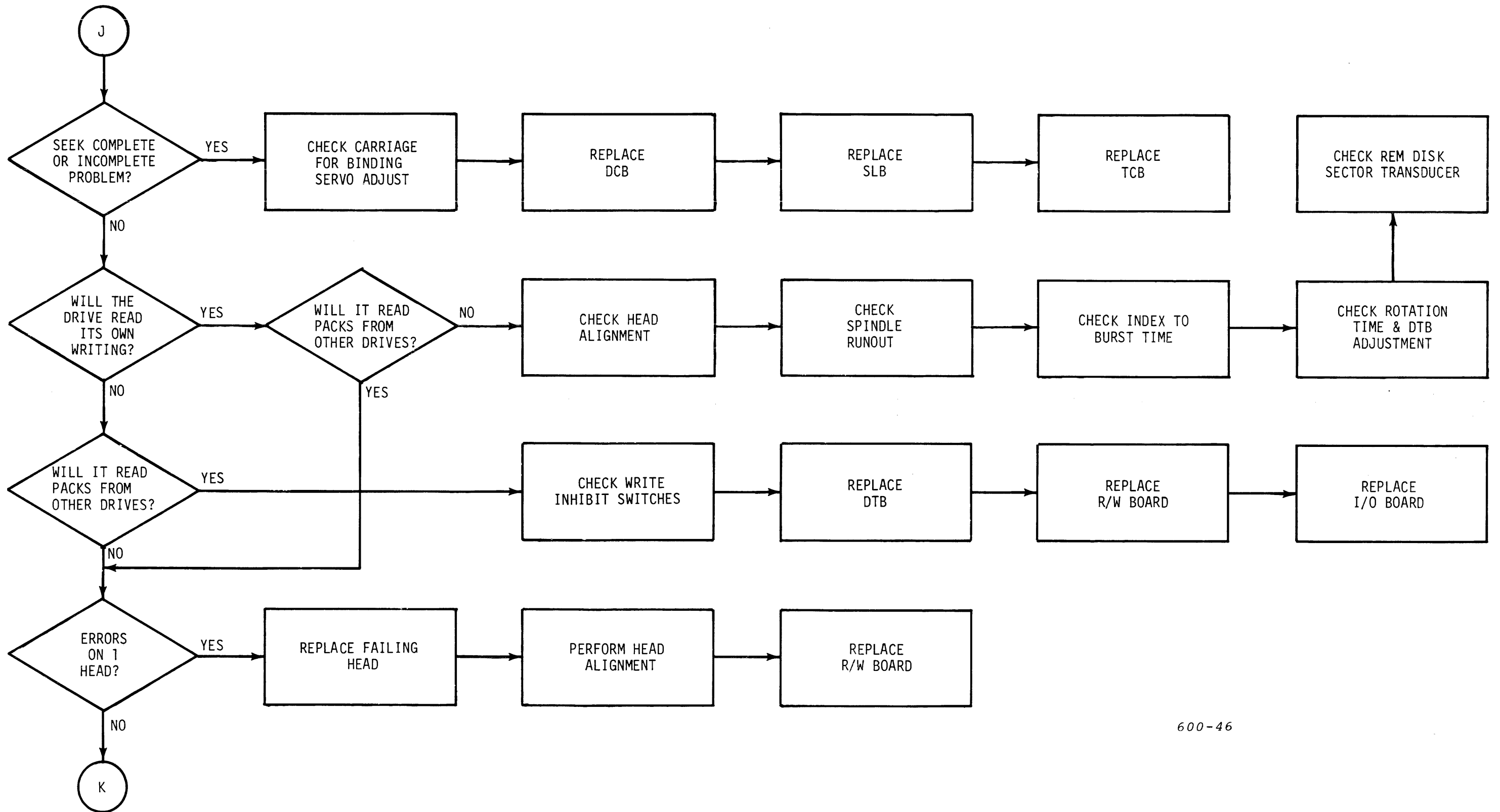
600-44

Figure 6-5. 306 Troubleshooting Flow Chart, Sheet 5 of 8



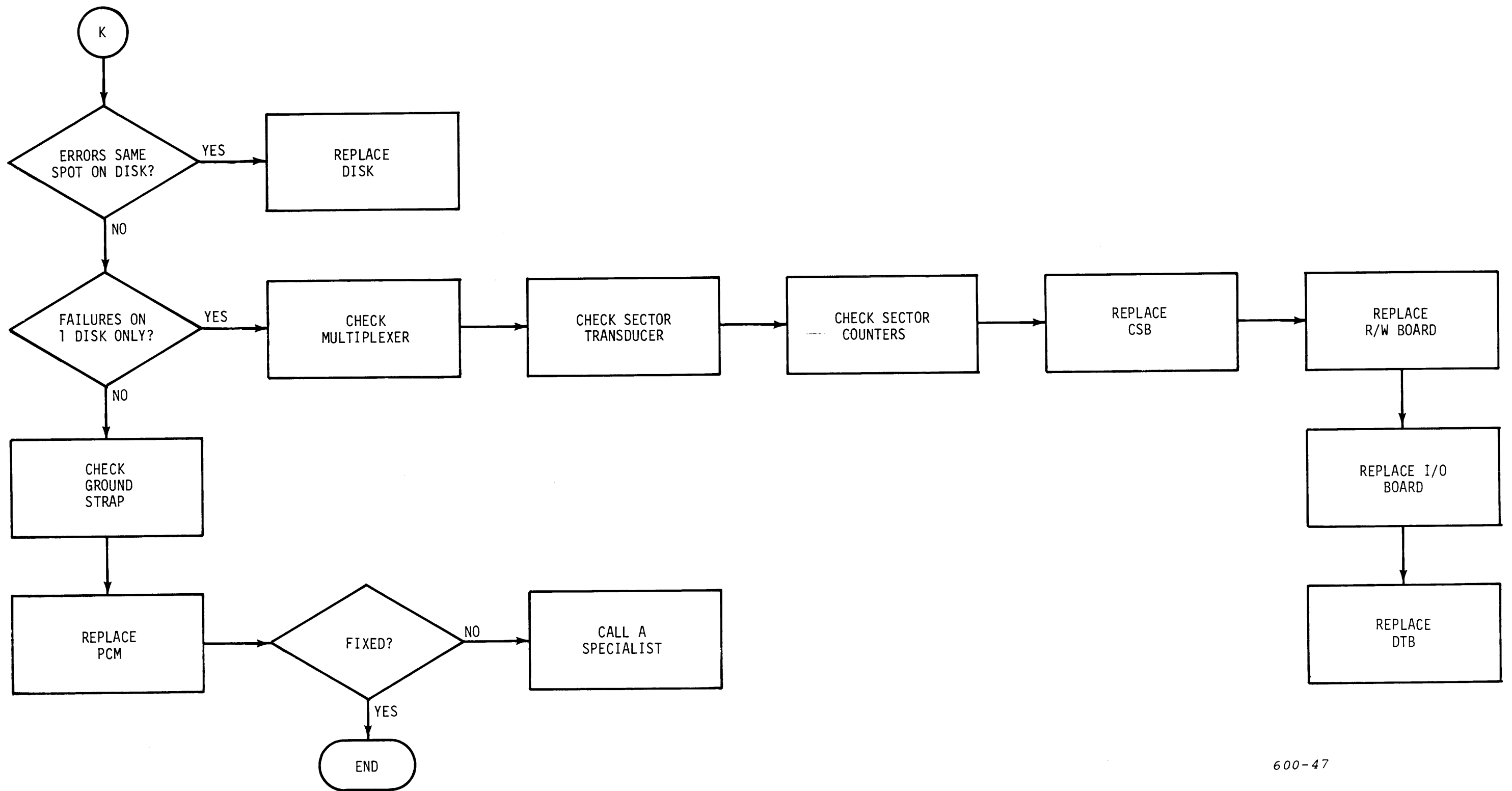
600-45

Figure 6-6. 306 Troubleshooting Flow Chart, Sheet 6 of 8



600-46

Figure 6-7. 306 Troubleshooting Flow Chart, Sheet 7 of 8



600-47

Figure 6-8. 306 Troubleshooting Flow Chart, Sheet 8 of 8

SECTION 7
MAINTENANCE

Table 7-1. Standard Tools

7.1 GENERAL

This section contains removal, replacement, and adjustment procedures for the Model 306 Series Disk Cartridge Drives. It is recommended that the entire procedure be read before performing any replacements or adjustments.

7.2 CAUTIONS

Many procedures in this section require that the drive be exposed either by removing necessary covers or by pulling the drive out of the cabinet if it is mounted on slides. When operating in this manner for prolonged periods of time, damage to the read/write heads, disks, carriage, and positioner motor can result if care is not exercised to keep foreign matter out of these areas. The read/write heads should be checked for contamination prior to restoring the drive in the cabinet.

7.3 TOOLS AND MATERIALS

Standard and special tools and materials required are listed in Tables 7-1 through 7-3.

7.4 PREVENTIVE MAINTENANCE

The following preventive maintenance operations and routine checks are recommended to ensure reliable operation of the disk drive. These recommendations are, however, only a guide and should be modified to meet the individual requirements of drives operating under extreme usage or environmental conditions. Refer to Figure 7-1 for the location of drive major assemblies.

7.4.1 Periodic Checks (6-Month Intervals)

Routine checks should be limited to the areas listed below as long as the drive is functioning properly. Refer to the specific sections of this manual for detailed procedures.

- Read/Write Head Inspection
- Detent Mask, checked and cleaned if necessary

Name	Manufacturer	Part Number
Allen Wrench 1/16"	Handi Hex Key	607
Ball Driver 5/64"	Bondhus	BS 5/64
Ball Driver 3/32"	Bondhus	BS 3/32
Ball Driver 7/64"	Bondhus	BS 7/64
Ball Driver 1/8"	Bondhus	BS 1/8
Ball Driver 9/64"	Bondhus	BS 9/64
Ball Driver 5/32"	Bondhus	BS 5/32
Adjustable Wrench 6"	Xcelite	46C
Screwdriver Set	Xcelite	PS 88
IC Extender, 14-pin	A.P., Inc.	Model TC-14
IC Extender, 16-pin	A.P., Inc.	Model TC-16
Torque Screwdriver	Utica	TS-30
Socket Tip	Utica	HW-4A
Phillips Tip	Utica	HW-17
Potentiometer Alignment Screwdriver	Walpco Electric	2525
Solder Iron	Weller	Model W60

Table 7-2. Special Tools and Equipment, Electrical

Name	Manufacturer	Part Number
Head Connector Current Loop Adapter	EMM-Caelus	430327
IC Extender, 14-pin	A.P., Inc.	Model TC-14
IC Extender, 16-pin	A.P., Inc.	Model TC-16
Oscilloscope	Tektronix	Model 465 or equiv.
Multimeter	-	-
Digital Voltmeter	Systron-Donner	7050 or equivalent
CE Alignment Cartridge	EMM-Caelus	CMIII 302209-009
AC Current Probe	Hewlett-Packard	Model 1110A or equiv.
Board Extender	EMM-Caelus	00430521-9

Table 7-3. Special Tools and Materials, Mechanical

Name	Manufacturer	Part Number
Voice Coil Alignment Kit	EMM-Caelus	430569
CMIII Test Hub 206 (24 sec)	EMM-Caelus	011037-49
CMIII Test Hub 306 (24 sec)	EMM-Caelus	301068-009
Mylar Shim, Detent	EMM-Caelus	430049
Fixed Disk Replacement Kit	EMM-Caelus	306
Cleaning Kit	Local Purchase	
Gram Guage	Scherr-Tumico	63-6383
Terminal Pins	Amphenol	85931
Grease	Aero Shell	7/GIA
Heat Sink Compound	Wakefield	120-2
Motor Oil (2,400-rpm Sleeve Only)	Shell	Turbo 33

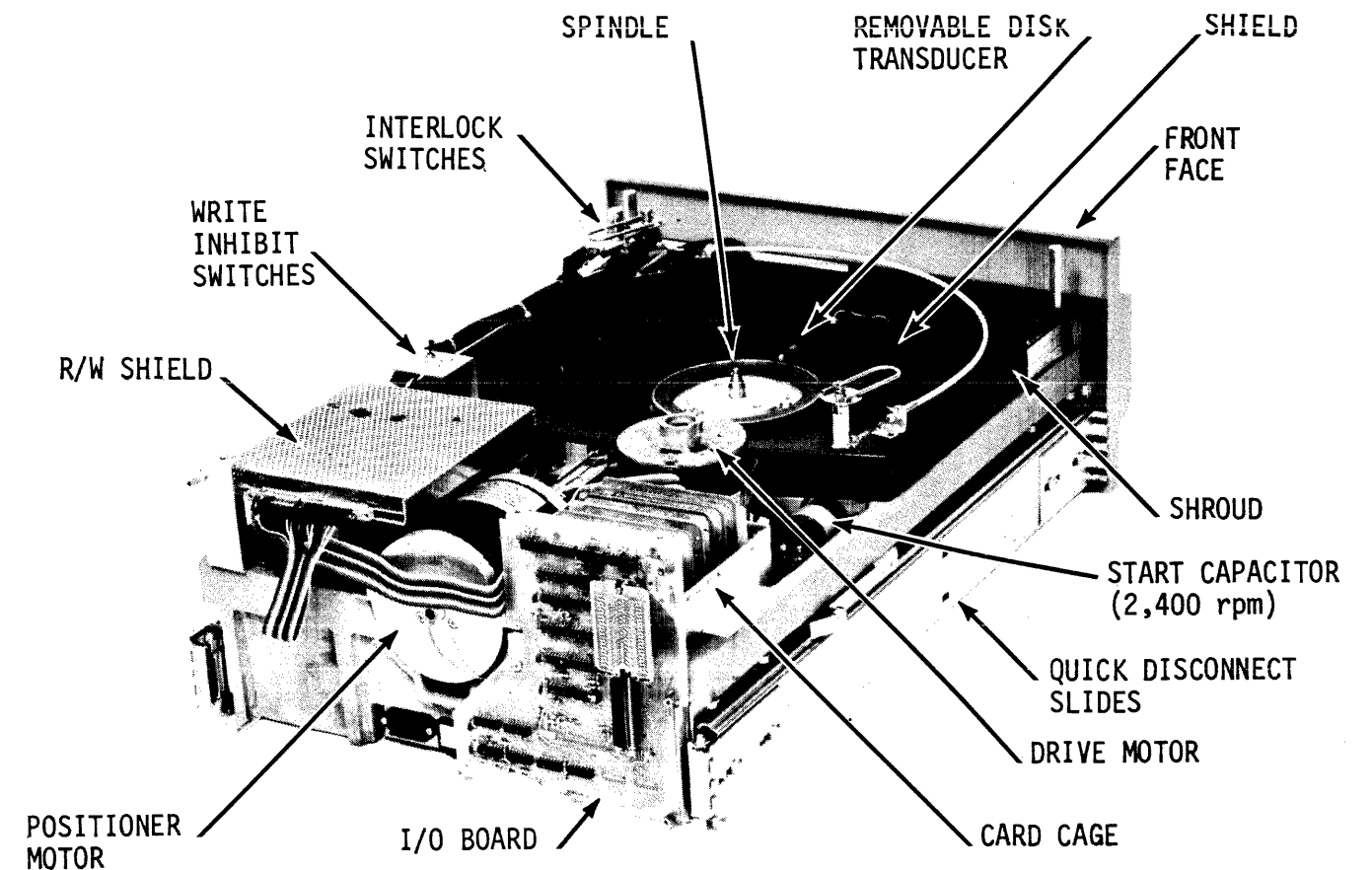


Figure 7-1. Model 306D/306R Series Major Assembly

dispenser, head and disk cleaning paddles, and lint-free tissues. Drug store isopropyl alcohol is not acceptable for this purpose.

7.4.2 Periodic Maintenance (12-Month Intervals)

a. Change Air Filter

Before installing a new air filter, inspect the air passage and blower blades for contamination. If cleaning is required, use a lint-free tissue moistened with the alcohol/water solution in the cleaning kit.

b. Clean Heads

Although the EMM-Caelus clean air system greatly increases the required time interval for read/write head cleaning, as a precautionary measure, the heads should be inspected any time the air filter is changed. When required, head shoes are to be cleaned using a cotton swab dampened in the alcohol/water solution. Wipe the face of the shoe until the swab shows no trace of discoloration. Exercise caution as the heads are delicate.

7.4.3 Cleaning Kit

The cleaning kit should include 91 percent reagent grade isopropyl alcohol and 9 percent distilled water cleaning fluid with

7.4.4 Fixed Disk Replacement Kit

This kit contains an EMM-Caelus C.P. recording disk and nylon glove.

7.4.5 Drive Test Unit

The Drive Test Unit (DTU-2) is a light-weight, portable electronic test device designed to check out the basic performance of the disk cartridge drive and provides the versatile control and test functions required to evaluate disk drive integrity; specifically, access mechanism performance and data reliability. (See Figure 7-3). The DTU-2 eliminates the necessity of using the computer for maintenance when a malfunction is suspected in a disk drive. The DTU-2, with internal power supply, is enclosed within a molded, vinyl carrying case.

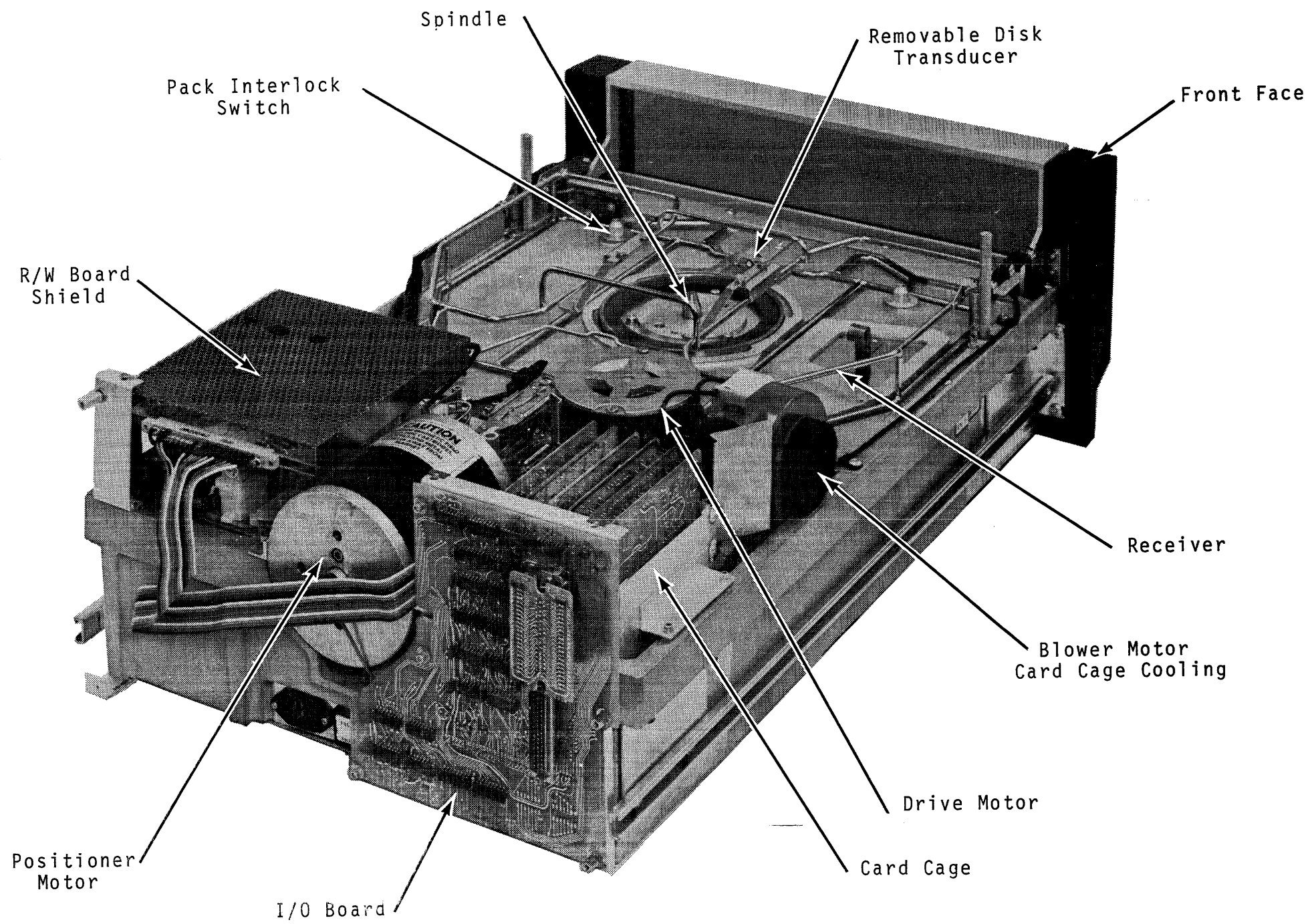


Figure 7-2. Model 206D/206R Series Major Assembly

7.5 REMOVAL AND REPLACEMENT PROCEDURES

7.5.1 Top Cover

a. Removal

1. Turn off drive Power switch.
2. Remove four Phillips head screws holding top cover to the drive.
3. Carefully lift the top cover straight up off the drive.

b. Replacement

1. Vacuum the inside of the drive.
2. Carefully lower the top cover into mounting position.
3. Install four Phillips head screws securing the top cover.
4. Turn on drive Power switch.

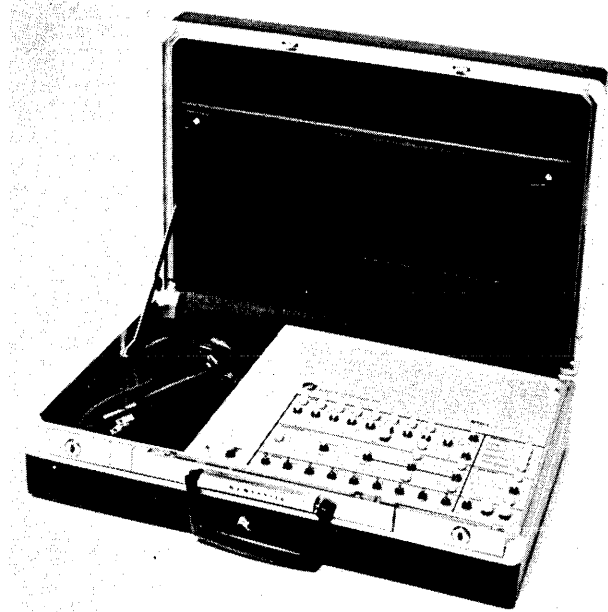
7.5.2 Rear Cover

a. Removal

1. Turn off drive Power switch.
2. Remove drive top cover. (Refer to subsection 7.5.1).
3. Remove the termination board from I/O board connector J22 if installed on drive.
4. Disconnect I/O cable.
5. Remove four Phillips head screws holding the rear cover to the drive.
6. Carefully remove the rear cover from the drive.

b. Replacement

1. Carefully hold the rear cover in mounting position and install four Phillips head screws.
2. Tighten mounting screws.



600-84

Figure 7-3. Drive Test Unit (DTU)

3. Replace terminator board if installed on drive.
4. Connect I/O cable.
5. Turn on drive Power switch.

7.5.3 Read/Write Amplifier Board (R/WA)

a. Removal

1. Remove covers. (Refer to subsections 7.5.1 and 7.5.2).
2. Remove the two No. 6-32 cap screws that retain the top of the read/write shield over the Read/Write board.
3. Remove the three No. 6-32 cap screws that retain the read/write shield to the PCM and positioner motor.
4. Disconnect the write inhibit switch connector, all head connectors, the ground strap, and the connector J14 from the Read/Write board. (See Figures 7-6, 7-7, and 7-8).
5. Remove the Read/Write board from the shield, being careful not to drop the spacers under the board into the drive.

b. Replacement

1. Mount the Read/Write board onto the shield using the Delrin spacers to prevent shorting the Read/Write board to the shield.
2. Connect J14, the write inhibit switch connector, the ground strap, and all head connectors to the Read/Write board. (Head connector locations are identified on the Read/Write board).
3. Install the shield and Read/Write board on the PCM and positioner motor.
4. Perform read/write amplifier adjustments.

c. Read/Write Amplifier (R/WA) Adjustments

1. Connect DTU or Controller to the drive (J21 on I/O board).
2. Ensure that a terminator board is connected to J22 on the I/O board.
3. Turn on drive Power switch.
4. Install disk cartridge.
5. Set drive Start/Stop switch to Start position.
6. Ensure that the removable disk write inhibit switch is off.
7. Connect the head loop adapter to the removable disk, top surface head connector (TR).

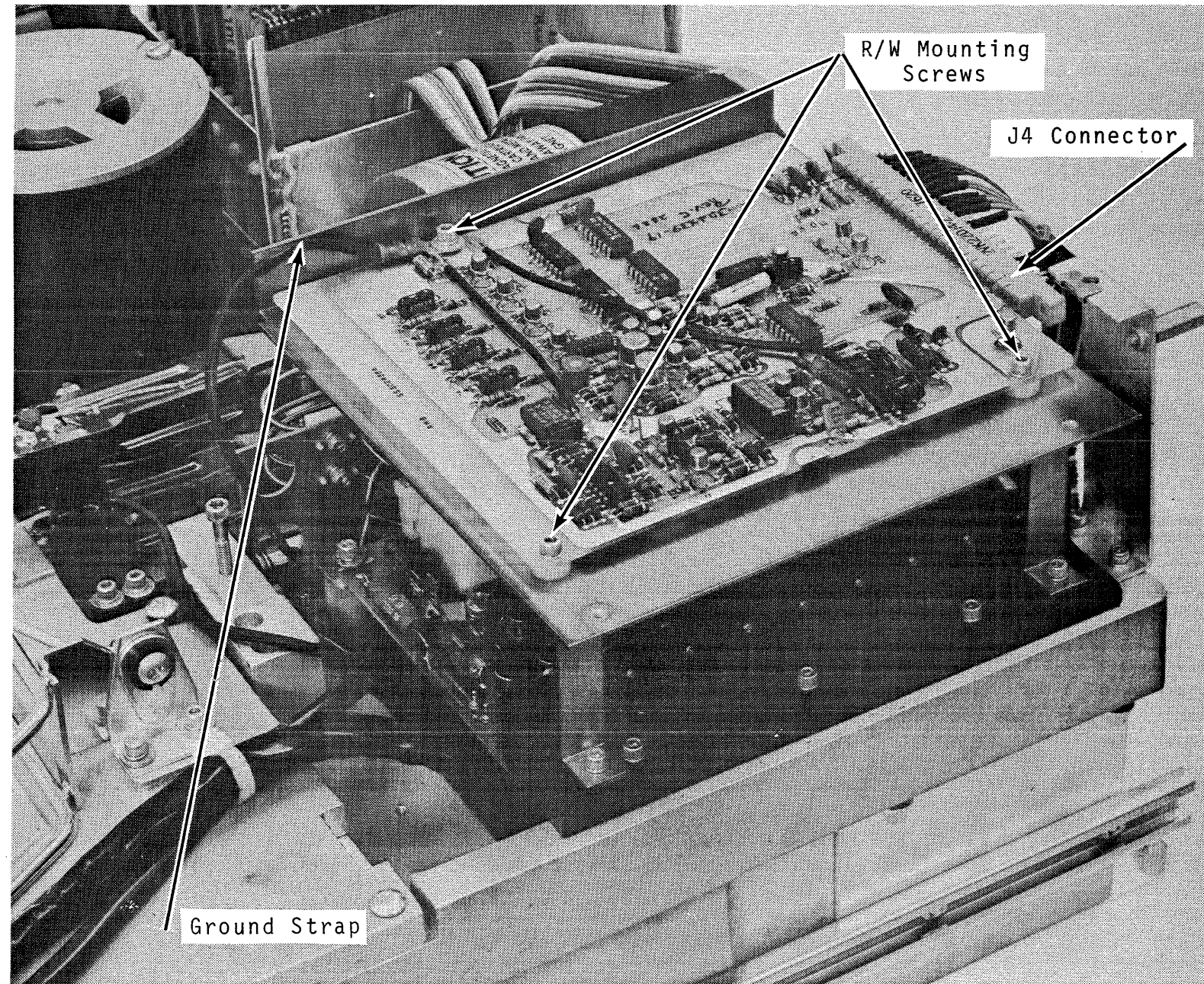
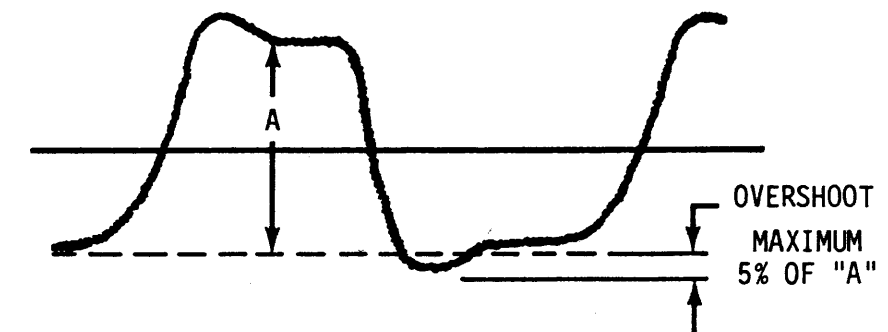


Figure 7-4. Read/Write Board

8. Set up to write all zeros on track 0 of the removable disk, top surface.
9. Set the oscilloscope as follows:

Sweep Speed	200 ns/cm
Vertical Gain	10 mv/cm
Trigger	Internal

10. Install a current probe on the oscilloscope and clamp it around the head adapter lead.
11. While writing all zeros on track 0, adjust R33 to obtain the write current waveform shown in Figure 7-5 with amplitude A equal to 85 ± 2 milliamps.
12. Set up to write all zeros on track 256 of the removable disk, top surface.
13. Verify that the write current waveform displayed on the oscilloscope is the same as shown in Figure 7-5 with amplitude A equal to 68 ± 2 milliamps.
14. Disconnect the current probe from the head adapter lead and remove from the oscilloscope.
15. Remove the head adapter from the removable disk, top surface head connector (TR).
16. Remount the shield over the Read/Write board.



600-87

Figure 7-5. Write Current Waveform

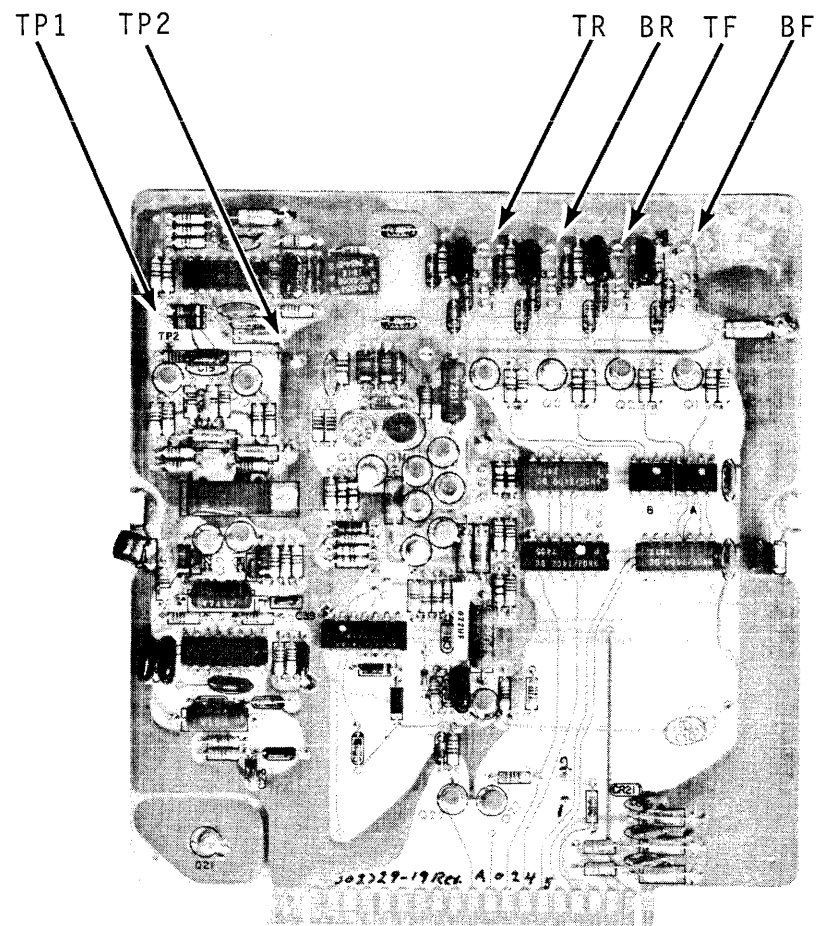
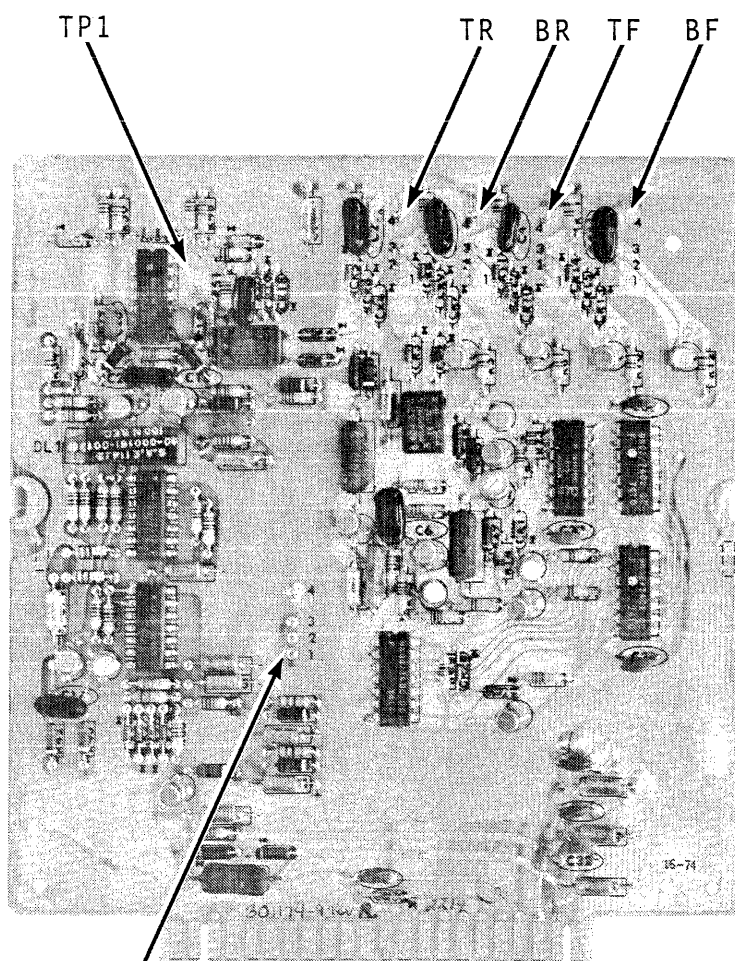
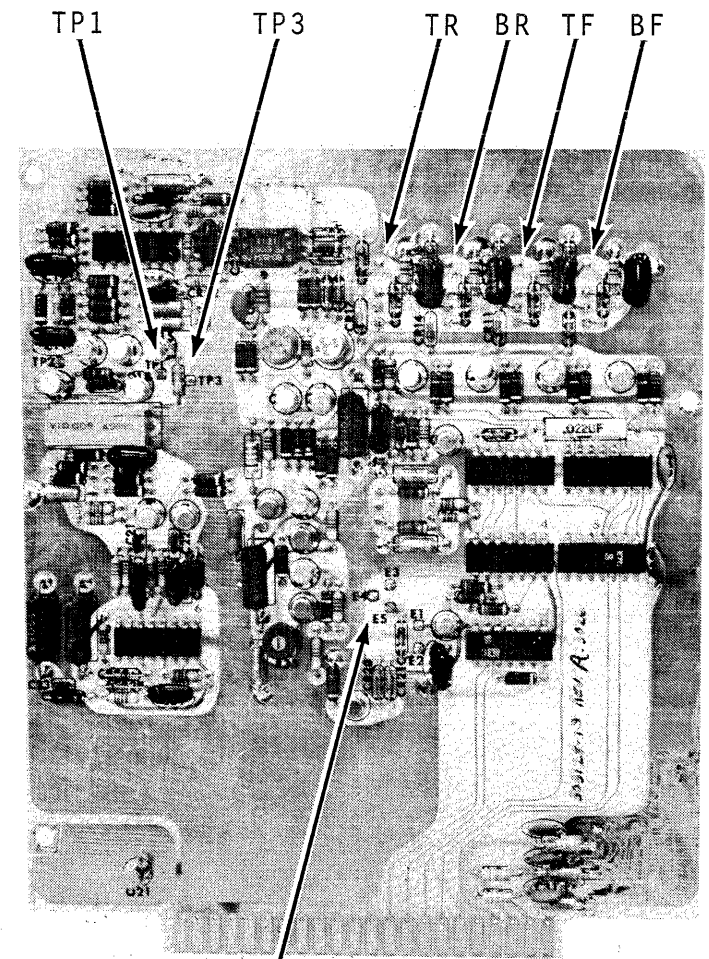


Figure 7-6. Read/Write Board Test Points (302329)



J14 - WRITE INHIBIT CONNECTOR

Figure 7-7. Read/Write Board Test Points (301174)



WRITE INHIBIT OPTION

Figure 7-8. Read/Write Board Test Points (303128)

7.5.4 Power Control Module (PCM)

a. PCM Removal

1. Turn off the Power switch and unplug the AC power cord.
2. To gain access to the PCM, the Read/Write board must be removed. To remove the Read/Write board, refer to subsection 7.5.3. The PCM is now accessible.
3. Remove the following connectors from the PCM:
 - J16 connector (34-pin flat cable) to the Mother board
 - J15 connector on the flex cable
 - J2 Molex connector (15-pin connector)
 - J18 for the detent LED
4. Remove the two No. 6-32 cap screws that mount the ground strap and PCM to the base casting.
5. Remove the No. 4-40 cap screws mounting the power transistor heatsink to the base casting.

b. PCM Replacement

1. Connect J18 for the detent LED on the PCM.
2. Install the No. 6-32 cap screws that mount the PCM to the casting.
3. Perform PCM checks and adjustments.

c. Power Control Module (PCM) Checks and Adjustments

NOTE

Unless indicated otherwise, all test points and adjustments are located on the PCM. (Refer to Figure 7-9).

1. Connect the positive and negative leads of the DVM as follows and ensure that required voltages are present.

NOTE

Do not ground the negative lead of the DVM to ground. The terminals on C5 and C6 are slotted screws.

<u>Positive Lead To</u>	<u>Negative Lead To</u>	<u>Voltage</u>
C5 (+) Terminal	C5 (-) Terminal	Minimum +21V Nominal +24V Maximum +30V
C6 (-) Terminal	C6 (+) Terminal	Minimum -21V Nominal -24V Maximum -30V
IC 2-11	C5 (-) Terminal	Minimum + 9V Nominal +12V Maximum +15V

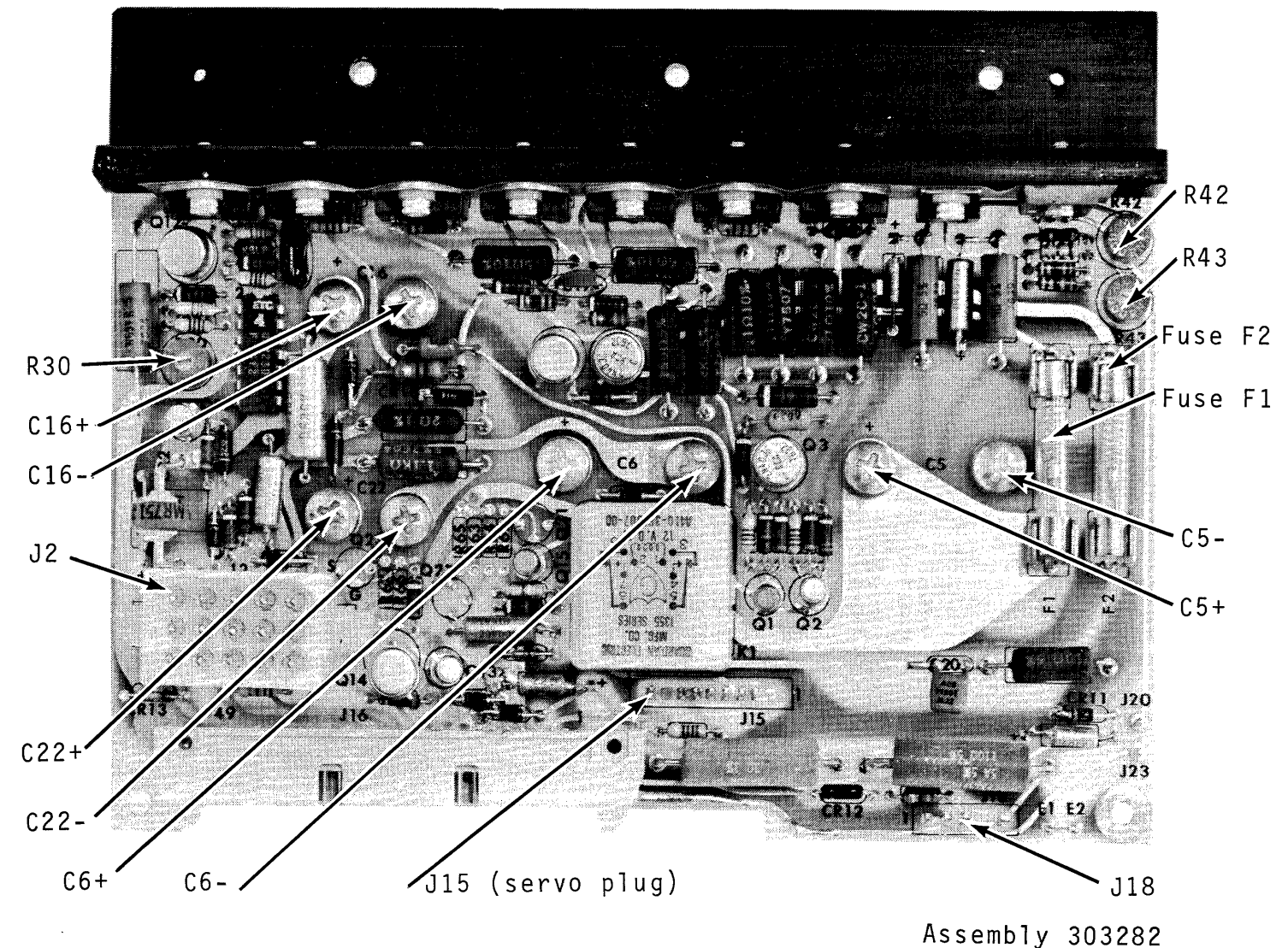


Figure 7-9. Power Control Module Test Points and Adjustments

2. Connect the positive lead of the DVM to IC 2-3 and the negative lead to IC 2-7. Adjust R30 of the PCM for 5.0 volts ± 0.1 volt.
3. Connect the DVM across CR10 and adjust R43 for +15 volts ± 0.1 volt.
4. Connect the DVM across CR11 and adjust R42 for -15 volts ± 0.1 volt.
5. Install Mother board connector J16.
6. Recheck PCM voltages.

7.5.5 Input/Output Board

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove covers. (Refer to subsections 7.5.1 and 7.5.2).
3. Remove the terminator board if installed.
4. Remove the three standoff screws and the three cap screws mounting the I/O board to the drive.
5. Pull the I/O board off the J19 Mother board connector.

b. Replacement

1. Position the I/O board on J19 and install the three cap screws and three standoffs.
2. Install terminator board and power up the drive.

c. I/O Board Checks

1. Place unit select switch to Position 1 (Unit 0). Ground J22, pin 46 to provide a unit select and enable the multiplexer (IC 17).
2. Check rotation time by monitoring IC 11, pin 5 (index removable). The period of the index pulses should be: 40 \pm 0.4 milliseconds for 1,500-rpm units and 25 \pm 0.25 milliseconds for 2,400-rpm units.
3. If the multiplex option is specified, a jumper shall be installed between pins E48 and E49 of the I/O board. If this is the case, check the operation of the multiplexer chip as follows:
 - (a) Connect channel A to IC 11, pin 5.
 - (b) Connect channel B to TP2 of the DCB. Use chop mode and trigger on channel A; set scope to 5 ms per division.

- (c) Connect a DTU or computer to the drive and select the removable disk--the index pulse on channel A should coincide with the index waveform pulse on channel B.
- (d) Select the fixed disk--the index pulses should no longer coincide.
- (e) Move channel B to TP1 of the DCB--the index pulses should once again coincide.

4. Check index and sector outputs for negative-going pulses at:

Index Removable	IC 11, Pin 5	
Sector Removable	IC 10, Pin 5	
Index Fixed	IC 12, Pin 5	} Only available if multiplex option is not specified.
Sector Fixed	IC 13, Pin 5	

NOTE

On a 306/1, fixed disk sector and index pulses are not available.

CAUTION

Whenever adjusting a 306/1, ensure the removable disk is being selected.

NOTE

If using a DTU and if the I/O board you are checking is an (-09), no pulses will be present because these lines are not terminated on the DTU.

NOTE

If illegal address/address acknowledge pulses are jumpered, pins E49-E41, E43-E44, and E46-E47, no Index fixed or Sector fixed pulses will appear.

5. Unit Select/Ungated Attention Circuits. Unit Select Circuit (Switch S1-A):
 - (a) Disconnect the DTU; turn the drive power on (do not start spindle) and connect a DVM to TP1 on the I/O board. The output should be 2.5 volts or higher.

- (b) Move the Unit Select switch to position No. 1 and connect one end of a jumper wire to ground. Connect the other end to J22-46. The DVM reading should go to zero. Next, ground J22-29, then J22-45, and then J22-44. The DVM should remain high (2.5 volts or higher).
 - (c) Move the Unit Select switch to position No. 2. DVM will go low if J22-29 is ground. DVM will stay high when J22-46, 45, and 44 are grounded.
 - (d) Move the Unit Select switch to position No. 3. DVM will go low if J22-45 is grounded. DVM will stay high when J22-46, 29, and 44 are grounded.
 - (e) Move the Unit Select switch to position No. 4. DVM will go low if J22-44 is grounded. DVM will stay high if J22-46, 29, and 45 are grounded.
6. Unit Address/Ungated Attention Circuit (S1-B):
- (a) Select switch position No. 7. With the heads in the home position, verify that J22-40, 41, 42, and 43 are all high (2.5 volts or higher).
 - (b) Allow the heads to load, then enter the sequential access mode. The outputs of J22 should be in accordance with row 1 of Table 7-4.
 - (c) Select switch position No. 8. The outputs should be in accordance with row 2 of Table 7-4.
 - (d) Sequentially select switch positions No. 9 and 0 and verify that the outputs are in accordance with Table 7-4.
 - (e) With the heads at track 0 and the DTU unplugged, verify that J22-37 is high (2.5 volts or higher).

Table 7-4. Ungated Attention

SWITCH POSITION	OUTPUTS ON J22 PINS			
	43	42	41	40
Selected				
7	Pulses	High	High	High
8	High	Pulses	High	High
9	High	High	Pulses	High
0	High	High	High	Pulses

7. Illegal Address Circuit: Position the Unit Attention switch to position No. 9, access track 128. Select the Illegal Address 408 for "R" models or 204 for "D" models.

If the auto recall jumper is not installed on the I/O board, the carriage will remain at track 128. With the auto recall jumper installed on the I/O board, the carriage will return to track 0 and alternate between tracks 0 and 1 every time a seek pulse is generated. Verify that the outputs at J22-40 are positive-going pulses (2.5 volts or higher).

- 8. Address Clear Circuit: Access track 128. Momentarily, short J22-48 to ground. The carriage will return to track 0, as long as E16 to E17 is not jumpered. If E16 is jumpered to E17, it will be necessary to short J22 pin 33 to ground also.
- 9. Write Inhibited (-) Circuit (R/W) Board: Leave the heads stationary while performing an alternate read/write operation. Look at the Read/Write board to see what the jumper configuration is for your drive. There will be one of three possible jumper configurations. Monitor J22-47. Referring to Table 7-5, ensure the correct output for your jumper configuration at J22 pin 47. Check both disk with write protect switches on and off.

Table 7-5. Write Inhibit Options

Description	Jumpers	Switch On	Switch Off
		J22-47	J22-47
Write Inhibited Active	E1 to E2	Pulses	Pulses
Write Inhibited Switch On	E3 to E5	Low	High
Write Inhibited Normally Active	E4 to E5	Low	Pulses

Note: On some R/W boards, E3 = A, E4 = B, E5 = C.

- 10. Sector Counters: Verify proper operation of the sector counters. If possible, use the same number of sectors on the removable as on the fixed disk. If such a cartridge is not available, use a 24-sector cartridge.

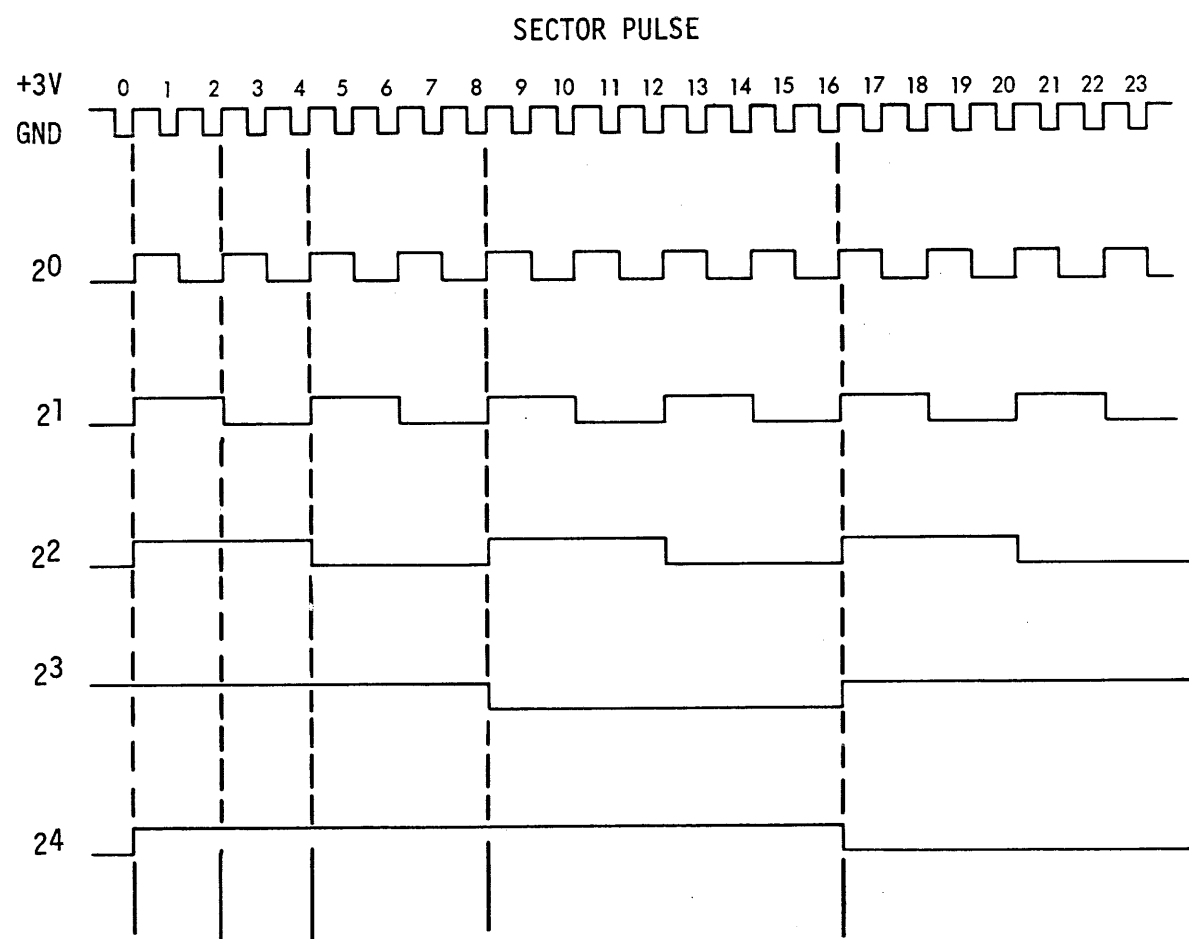
Scope set-up procedure:

- (a) Trigger the scope on index (I/O board IC 11 pin 5). Select the disk whose counter is to be observed. Use the 5 millisecond/div. time scale.
- (b) The diagram in Figure 7-10 gives the output condition of the counter after each sector pulse. When observing the counter with the above scope set-up, the maximum sector count will be displayed by the scope. The test point locations are given in Table 7-6.

(c) Next, observe the output of each counter bit for at least 40 milliseconds and verify that the signal amplitude is at least 2.5 volts whenever it is in the high state. Check to verify that output waveform agrees with Figure 7-10.

NOTE

If no multiplex option is specified, trigger scope on IC 12 pin 5 (index fixed) when checking the fixed disk sector counters.



600-89

Figure 7-10. Sector Counter

Table 7-6. Sector Counter Outputs

Counter Bit	Test Point
2^0	J22-14
2^1	J22-12
2^2	J22-13
2^3	J22-15
2^4	J22-16

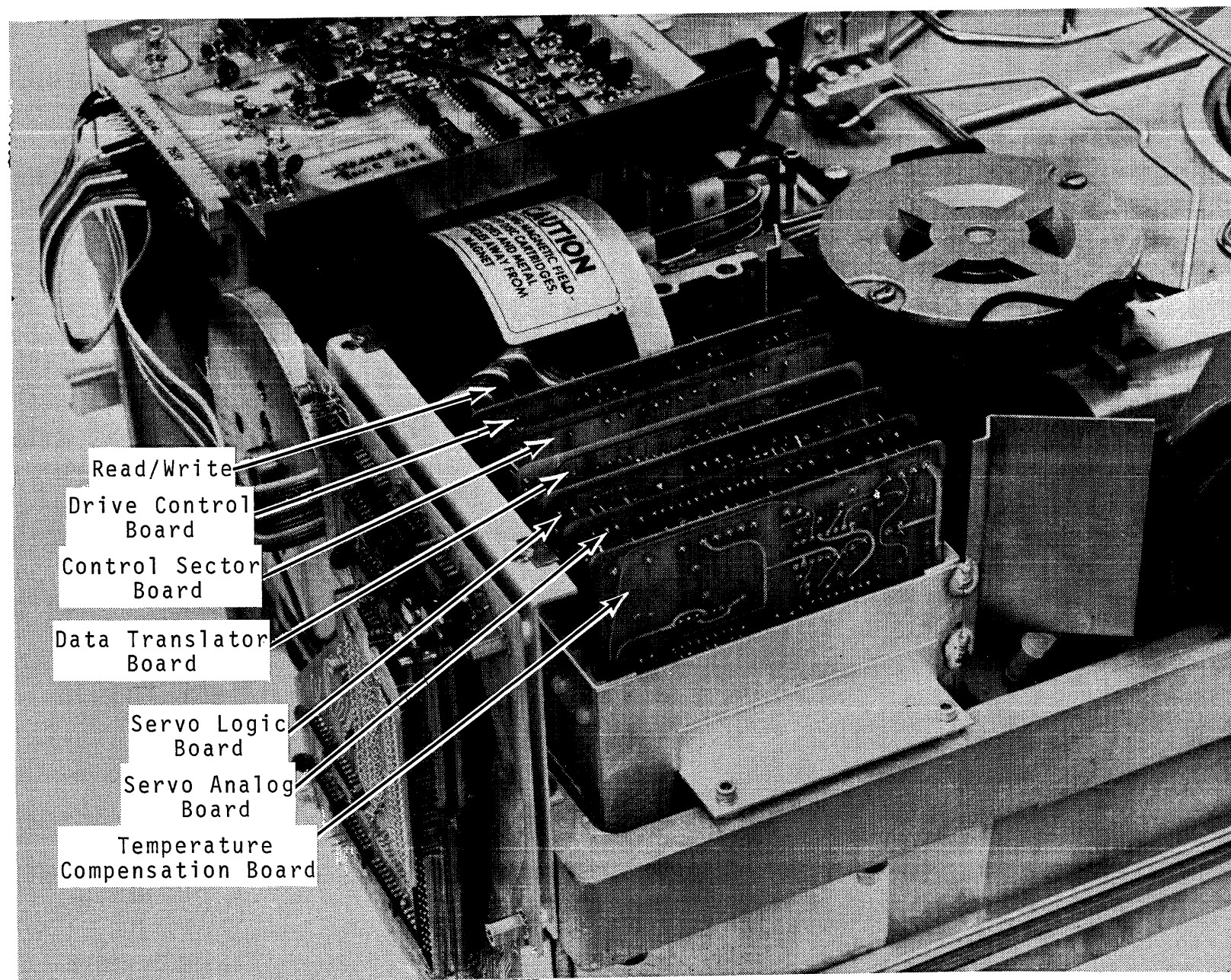


Figure 7-11. Card Cage

7.5.6 Drive Control Board (DCB)

a. Removal

1. Remove top and rear covers.
2. Pull the DCB out of the card cage. (See Figure 7-11).
3. Install new DCB on card extender and perform electrical checks.

b. DCB Electrical Checks

1. Turn power on.

Table 7-7. DCB One Shots

SIGNAL NAME	I/O BOARD	LOCATION	1,500 rpm	2,400 rpm
IDX FXD NOTCH	19A	IC 2, Pin 10	650 to 800 ns(+)	650 to 800 ns
IDX REM NOTCH	14A	IC 1, Pin 10	650 to 800 ns(+)	650 to 800 ns
IDX FXD OS	20A	IC 2, Pin 6	650 to 1000 μ s(-)	410 to 620 μ s
IDX REM OS	13A	IC 3, Pin 10	650 to 1000 μ s(-)	410 to 620 μ s

NOTE

If it is required that the drive be Diablo compatible the duration of Index Fixed Notch (+) and Index Removable Notch (+) will be 5 usec. The value of C3 and C11 on the DCB will be 0.0022 μ fd rather than the normal 270pf.

2. Check the one shots on the DCB to verify proper time delays. There are four one shots as indicated in Table 7-7.

NOTE

One shots can be checked on the I/O board at J19 without having to extend the DCB. Pin location is shown on Table 7-7.

3. Reinstall DCB in card cage.
4. Perform circumferential alignment. See subsection 7.5.16.d.6 (g, h, and i).
5. Replace top and rear covers.

7.5.7 Control Sector Board (CSB)

a. Removal

1. Remove top and rear covers from the drive.
2. Pull CSB from the card cage.
3. Install new CSB.
4. Perform electrical checks.

b. Electrical Checks for Standard CSB

1. Check sector counter outputs per subsection 7.5.5, step c.10.
2. Replace top and rear covers.

c. Electronic Check and Adjustment for 48-Sector CSB

NOTE

The following adjustments are made with a 48-sector pack on and rotating.

1. Trigger on the positive edge of the output at TP3 and adjust R50 for a pulse width of 720 ± 20 microseconds at TP3.
2. Trigger on the positive edge of the output at TP5 and adjust R32 for a pulse width of 720 ± 20 microseconds at TP5.
3. Trigger on the positive edge of the output on TP4 and adjust R46 for a pulse width of 210 ± 10 microseconds at TP4.
4. Trigger on the positive edge of the output on TP6 and adjust R40 for a pulse width of 210 ± 10 microseconds at TP6.
5. The procedure listed below will ensure the correctness of the index and sector one shot adjustments:
 - (a) Trigger negative on J22, pin 15 (index fixed) and observe same. Index should occur every 40 milliseconds. Observe J22, pin 12 (sector fixed), and ensure there are 48-sector pulses available from index to index.
 - (b) Trigger negative on J22, pin 13 (index removable) and observe same. Index should occur every 40 milliseconds. Observe J22, pin 14 (sector removable), and ensure 48-sector pulses available from index to index.

7.5.8 Data Translator Board (DTB)

a. Removal

1. Remove top and rear covers from the drive.
2. Pull DTB from the card cage.
3. Install new DTB and start up drive.
4. Perform data discriminator adjustments.

b. Data Discriminator Adjustment

1. Ensure that removable and fixed disk write inhibit switches are off.
2. Set up the Controller to write an alternate data pattern on track 0 of each disk surface.
3. Set the oscilloscope as follows:

Sweep Speed	10 ms/cm
Vertical Gain	500 mv/cm, AC
Trigger (+) internal	TP5 (Read Enable)
4. Connect the oscilloscope trigger to TP5 (Read Enable) of DTB. Set the oscilloscope to trigger on the positive edge of Read Enable, and display TP5 on channel A.
5. Connect oscilloscope channel B probe on TP4 of DTB.
6. Set up the Controller to read the previously written data while ignoring errors.
7. Observe the discriminator error voltage waveform displayed on the oscilloscope during the positive duration of Read Enable.
8. Adjust R19 for a negative 1.2 volts \pm 100 mv on TP4 during read time. (See Figure 7-12).
9. Replace top and rear covers on the drive.

7.5.9 Servo Logic Board ("R" model only).

a. Removal and Replacement

1. Remove top and rear covers.
2. Pull the Servo Logic board from the card cage.
3. Install new SLB.
4. Allow the heads to load and seek to track 400. While monitoring TP2 on the TCB, adjust R30 on the SLB for 7 volts \pm 20 millivolts. (Use DVM).

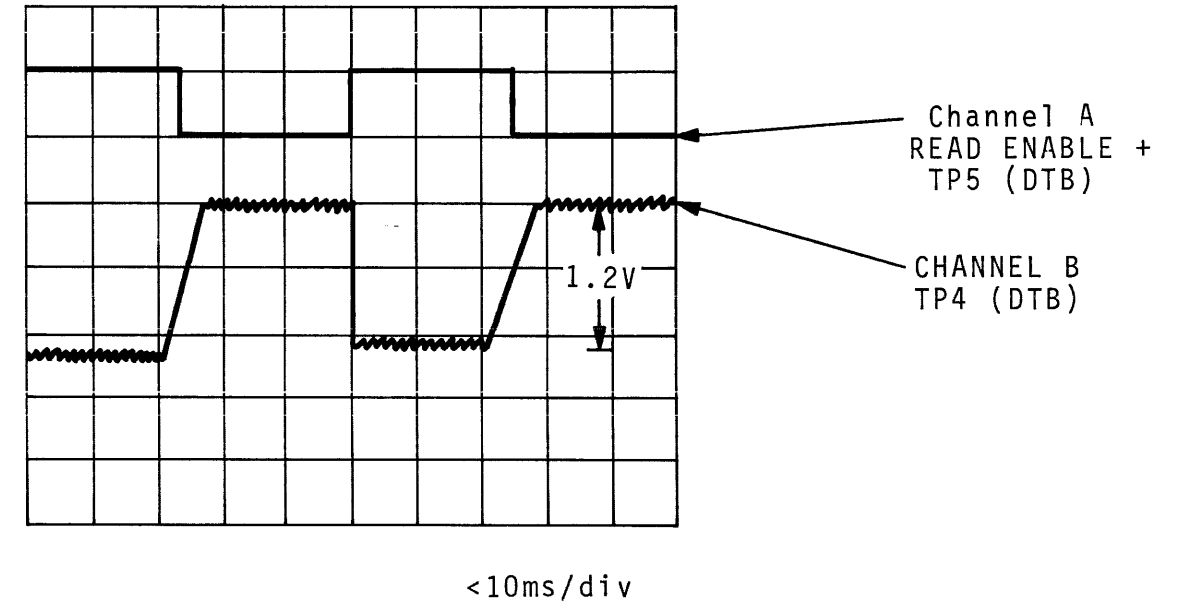


Figure 7-12. TP4, Data Translator Board

NOTE

In Figure 7-12 it is possible to adjust TP4 180° out of phase. To avoid this, be sure that when channel A (Read Enable +) is positive that channel B, TP4, is negative.

5. Seek to track zero. TP2 should now read zero volts \pm 20 millivolts. If not, readjust R30 on the SLB and repeat steps 4 and 5 until TP2 is within tolerance limits at both track zero and track 400.
6. Install top and rear covers on drive.

7.5.10 Servo Analog Board ("R" model only)

NOTE

For correct servo adjustment Read/Write heads should be installed.

a. Removal and Replacement

1. Remove top and rear covers from the drive.
2. Install new SAB board.

3. Remove servo motor plug from PCM.
4. Power up and start drive.
5. Perform SAB electrical alignment, steps 7.5.10(b.1.a and b.1.b).
6. Stop drive; power down.
7. Install servo motor plug to PCM.
8. Perform SAB electrical alignment, starting at step 7.5.10.b.2.
9. Stop drive; power down.
10. Replace top and rear covers.

b. Servo Analog Board Electrical Alignment

1. Detent Amplitude and Balance:

- (a) Ground out the transient thermal compensation and the DC thermal compensation (TP3 and TP6 on TCB). Monitor TP3 on the SAB and adjust the voltage at TP3 to swing evenly around ground while moving the carriage by hand.
- (b) Monitor TP6 on the SAB and adjust R27 for 5 volts ± 0.2 volt peak-to-peak on TP6 while moving the carriage by hand.

2. Op Amp Offset Adjustment (Initial)

- (a) With heads setting at track 0, monitor TP3 (SAB) with a digital voltmeter and record. Use millivolt scale.
- (b) Seek to track 1.
- (c) Adjust R1 (SAB) so that the amplitude at TP3 (SAB) is equal to that which you recorded in Step (a) but of opposite polarity.

3. Servo Alignment:

- (a) Turn power on and allow heads to load.
- (b) Connect the drive to either a DTU or computer.
- (c) Adjust R5 on the SAB clockwise to the Stop (or ten turns).
- (d) Condition the drive to access alternately between track 0 and 135.
- (e) Sync negative on seek complete (+), TP3 (DCB), with channel A of the scope.
- (f) Monitor TP5 on the SAB, on channel B.

- (g) Adjust R4 on the SAB such that the negative portion of seek complete is less than 40 milliseconds long, but not shorter than 35 milliseconds long.
- (h) NOTE: When making this adjustment, TP5 on the SAB should not look erratic. TP5 should be smooth and even. If this is not the case, the servo is breaking up. Refer to Figure 7-13.

4. Op Amp Offset Adjustment (Final)

- (a) Do not alternate seek between track 0 and 1.
- (b) Monitor TP3 (DCB) with channel A.
- (c) Monitor TP3 (SAB) with channel B.

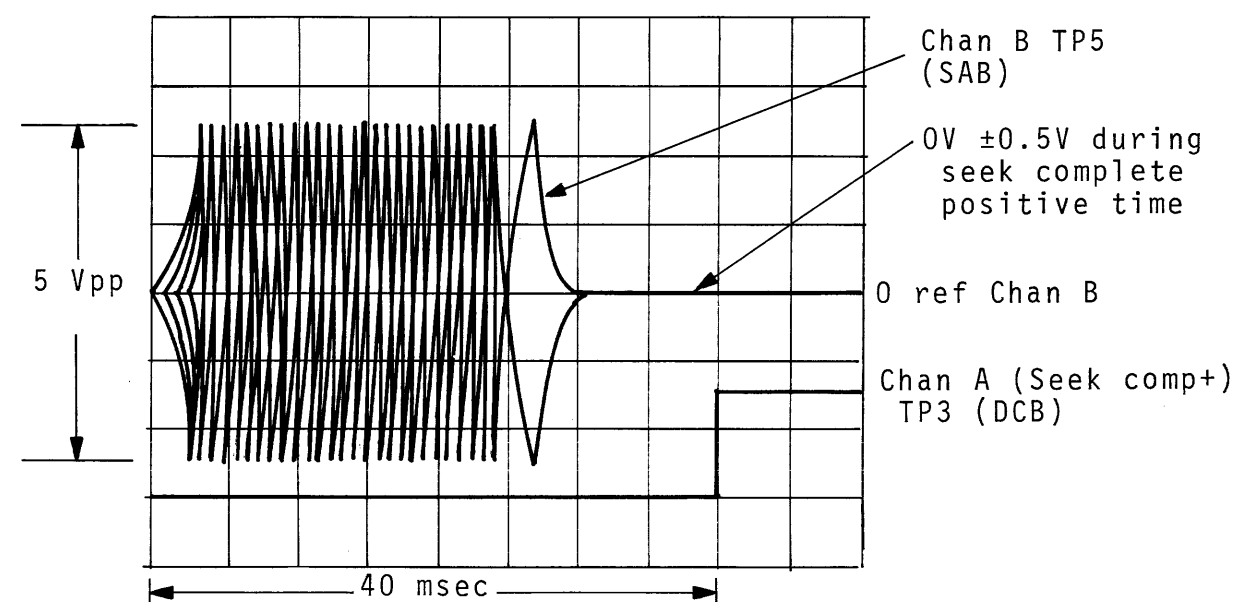


Figure 7-13. Seek Time Adjustment

Channel A: TP3 (DCB) seek complete (+) 2V/cm

Channel B: TP5 (SAB) 1V/cm

Sweep: 5 ms/cm

Syn: Internal neg channel A.

Operation: Alternate seek between track 0 and 135.

Adjust: Adjust R4 so that channel A goes positive with 40 ms or less.

NOTE

A small amount of jitter in the positive edge of seek complete (channel A) may be present.

- (d) Syn internal (+) on channel B.
- (e) Insure that at the time channel A is positive that channel B is less than ± 50 mv. If necessary, adjust R1 (SAB).

5. Remove ground jumper from TP3 and TP6 on the TCB.

7.5.11 Servo Logic Board ("D" model using a DTU-2 only)

a. Removal, Replacement, and Alignment.

1. Remove top and rear covers (See Section 7.5.1).
2. Pull the Servo Logic board from the card cage.
3. Install new SLB.
4. Look at the I/O board. Jumpers should be as follows for "D" model drives: E12-E13, E1-E4, and E2-E3.
5. Remove jumpers on I/O board called out in step 4.
6. Add the following jumpers on the I/O board: E11-E12, E1-E2, and E3-E4.
7. Go to section 7.5.9 entitled "Servo Logic Board ("R" model only). After completing section 7.5.9 return here.
8. Remove jumpers called out in step 6 and replace jumpers called out in step 4.

7.5.12 Servo Analog Board ("D" model using a DTU-2 only)

a. Removal, Replacement and Alignment.

1. Remove top and rear covers.
2. Replace Servo Analog Board.
3. Look at the I/O board. Jumpers should be as follows for "D" model drives: E12-E13, E1-E4, and E2-E3.
4. Remove jumpers on I/O board callout in step 3.
5. Add the following jumpers on the I/O board: E11-E12, E1-E2 and E3-E4.
6. Go to section 7.5.10 entitled "Servo Analog Board ("R" model only) and after completing return here.
7. Remove jumpers called out in step 5 and replace the jumpers called out in step 3.

7.5.13 Servo Logic Board ("D" model using computer only)

NOTE

When making servo adjustments on "D" model drives, adjustments are much easier to make using a DTU-2 rather than the computer to cause the necessary seek operations. If a DTU-2 is available, use section 7.5.11.

a. Removal, Replacement and Alignment.

1. Remove top and rear covers.
2. Pull the Servo Logic board from the card cage.
3. Install new SLB.
4. Power drive on and allow heads to load.
5. Monitor TP2 on the TCB with a DVM.
6. Using the computer, cause the drive to seek to track 200.
7. Adjust R30 on the SLB for 7 volts ± 20 millivolts at TP2 on the TCB.
8. Using the computer, cause the drive to seek to track 0. TP2 (TCB) should now read zero volts ± 20 millivolts. If not, readjust R30 on the SLB and repeat steps 6, 7 and 8 until TP2 is within tolerance limits at both track 0 and track 400.
9. Install top and rear covers on drive.

7.5.14 Servo Analog Board ("D" model using computer only)

NOTE

When making servo adjustments on "D" model drives, adjustments are much easier to make using a DTU-2 rather than the computer to cause the necessary seek operations. If a DTU-2 is available use section 7.5.12.

a. Removal and Replacement.

1. Remove top and rear covers from drive.
2. Install new SAB board.
3. Remove servo motor plug from PCM (P15).

4. Power up and start drive.
5. Perform SAB electrical alignment (section 7.5.14.b).
6. Replace top and rear covers.

b. Servo Analog Board Electrical Alignment.

1. Detent Amplitude and Balance
 - (a) Ground TP3 and TP6 on TCB. TP12 on TCB is ground.
 - (b) Unplug servo plug on PCM (P15).
 - (c) Power drive on and allow spindle to rotate.
 - (d) After disk is up to speed load heads by hand.
 - (e) Monitor TP3 on the SAB and adjust the voltage at TP3 to swing evenly around ground with R2 while moving the carriage by hand.
 - (f) Monitor TP5 on the SAB and adjust R3 for 5 volts \pm 0.1 volt peak-to-peak on TP5 while moving the carriage by hand.
 - (g) Move heads to home position by hand and then power off drive.
 - (h) Reconnect plug P15 on the PCM.
2. Op Amp Offset Adjustment (Initial)
 - (a) Remove wire wrap on I/O board E12-E13.
 - (b) Connect a temporary jumper to E12-E13 on the I/O board.
 - (c) Power drive on and allow heads to load.
 - (d) Using the computer have the drive seek to track 0.
 - (e) Monitor TP3 (SAB) with a DVM and record the voltage. Use millivolt scale.
 - (f) Carefully remove one end of the jumper on E12-E13 (I/O). Allow it to hang loose being careful that it does not short to anything.
 - (g) Using the computer seek to track 0 again.
 - (h) Adjust R1 (SAB) so that TP3 (SAB) is equal to the voltage recorded in step (e) but of opposite polarity.
 - (i) Go through steps (a) through (h) again to recheck adjustment.

NOTE

The Op Amp Offset adjustment is not critical on "D" model drives.

- (j) Remove temporary jumper on E12-E13 (I/O) and replace it with a permanent wire wrap jumper.

3. Servo Alignment

- (a) Turn power on and allow heads to load.
- (b) Using the computer condition the drive to seek alternately between track 0 and 67.
- (c) Set up scope as per Figure 7-13.
- (d) Adjust R4 on the SAB such that the negative portion of seek complete is less than 40 milliseconds long, but not shorter than 35 milliseconds.

NOTE

The length of seek operation on "D" model drives using a computer is track 0 to track 67. Not track 0 to track 135 as called out in Figure 7-9B.

7.5.15 Temperature Compensation Board

a. Removal and Replacement

1. Remove top and rear covers from the drive.
2. Pull the TCB from the card cage.
3. Install new TCB on Board Extender.
4. Perform electrical alignment.

b. Temperature Compensation Board Alignment.

1. Zero adjustment

R2 on the TCB needs to be adjusted for assurance that the correct track is detected as track zero. Refer to Section 7.5.27.d, e and f to perform this adjustment.

2. Temperature Compensation

- (a) Install a cartridge on the drive, turn drive on and allow one hour for the unit to reach temperature stabilization.
- (b) After the drive has been on for one hour, connect a DTU or system to the drive. As you go through this procedure it will be necessary to cause seeks to occur to tracks zero, 200 or 400.
- (c) Transient Thermal Comp Adjustment
 1. Using a DVM, monitor test point 6 on the TCB.

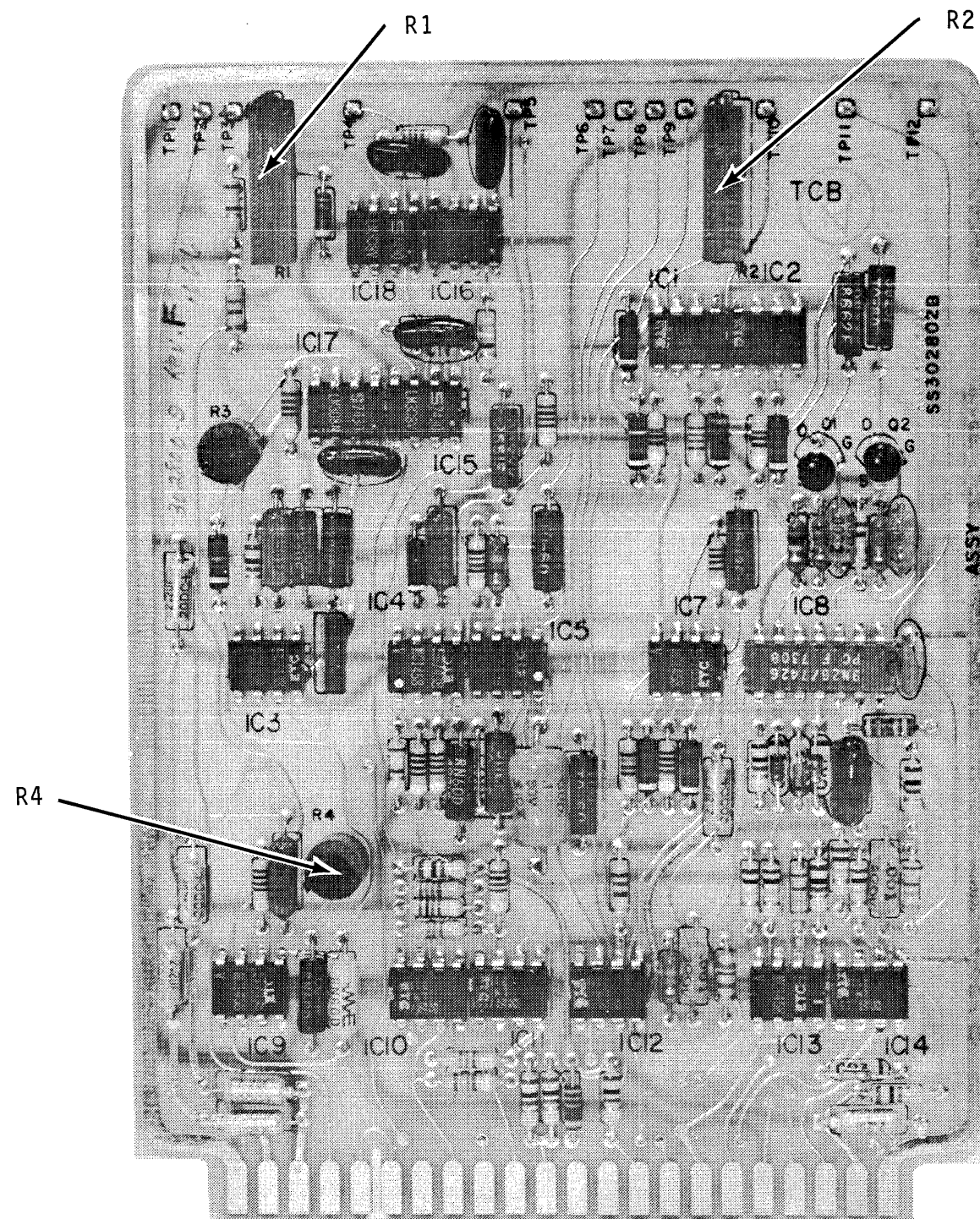


Figure 7-14. Temperature Compensation Board Assembly 302800

2. Adjust R1 such that TP6 reads 0.00 volts \pm 60 mv at any track.

(d) DC Thermal Comp Adjustment

1. Seek the drive to track 400.
2. Monitor TP2 on the TCB with a DVM.
3. Adjust R30 on the SLB such that TP2 reads +7 volts \pm 20 millivolts.
4. Seek the drive to track zero. (TP2 should now read zero volts \pm 20 mv). If not, readjust R30 on the SLB and repeat Steps 1 through 4 until TP2 is within tolerance limits at both tracks.
5. Monitor TP5 on the TCB with a DVM. It should read -5 volts \pm 100 mv. Any deviation from this probably means the +5 volts on the PCM needs to be readjusted.
6. Seek to the following tracks and adjust R4 on the TCB SUCH that the voltage on IC 9, pin 1 of TCB, as seen on a DVM, meets the following stated conditions: (Check each track twice).

TRACK	IC 9-1 (TCB)
0	2.5V \pm 100 mv
200	0V \pm 30 mv
400	-2.5V \pm 100 mv

7. Monitor the voltage at IC 15, pin 6 on the TCB with a DVM. (Refer to Figure 7-15). This voltage is representative of the drive casting temperature, and the voltage should be recorded for reference at this time.
8. Monitor TP3 on the TCB with a DVM. While referring to the corresponding voltage recorded in Step 7, adjust R3 on the TCB such that TP3 equals the correct value as shown in Figure 7-15. Note that the values given for TP3 in Figure 7-15 are for tracks zero and 400, and both track positions should be checked and adjusted for.

- EXAMPLE:
1. Seek to Track 0.
 2. IC 15-6 reads +1.32 volts
 3. You would then monitor TP3 and adjust R3 for -0.48V and if you seek to track 400, TP3 should read +0.48V.

IC-15 Pin-6

TP3

Temp. In Degrees F	Volts in Test Point		Volts in Test Point	
	TrackZero	Track 400	TrackZero	Track 400
50	+1.79	-1.79	-3.66	+3.66
52	+1.74	-1.74	-3.32	+3.32
54	+1.71	-1.71	-3.12	+3.12
56	+1.69	-1.69	-2.98	+2.98
58	+1.65	-1.65	-2.71	+2.71
60	+1.62	-1.62	-2.50	+2.50
62	+1.59	-1.59	-2.30	+2.30
64	+1.56	-1.56	-2.10	+2.10
66	+1.53	-1.53	-1.90	+1.90
68	+1.51	-1.51	-1.76	+1.76
70	+1.48	-1.48	-1.56	+1.56
72	+1.44	-1.44	-1.29	+1.29
74	+1.41	-1.41	-1.08	+1.08
76	+1.38	-1.38	-0.88	+0.88
78	+1.35	-1.35	-0.68	+0.68
80	+1.32	-1.32	-0.48	+0.48
82	+1.29	-1.29	-0.27	+0.27
84	+1.26	-1.26	-0.068	+0.068
86	+1.23	-1.23	0.0	0.0
88	+1.21	-1.21	+0.27	-0.27
90	+1.18	-1.18	+0.48	-0.48
92	+1.15	-1.15	+0.68	-0.68
94	+1.12	-1.12	+0.88	-0.88
96	+1.09	-1.09	+1.08	-1.08
98	+1.06	-1.06	+1.29	-1.29
100	+1.03	-1.03	+1.49	-1.49
102	+1.00	-1.00	+1.70	-1.70
104	+0.98	-0.98	+1.83	-1.83
106	+0.95	-0.95	+2.04	-2.04
108	+0.93	-0.93	+2.17	-2.17
110	+0.90	-0.90	+2.37	-2.37

Figure 7-15. Temperature Compensation Adjustment Voltages

9. Temperature compensation is now adjusted. If adjustments were made, head alignment will have to be redone to maintain compatibility.

7.5.16 Read/Write Heads (Refer to Figure 7-16)

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Disconnect head connectors from the R/WA board.
3. Loosen two cap screws securing the head lead clamps to the carriage assembly.

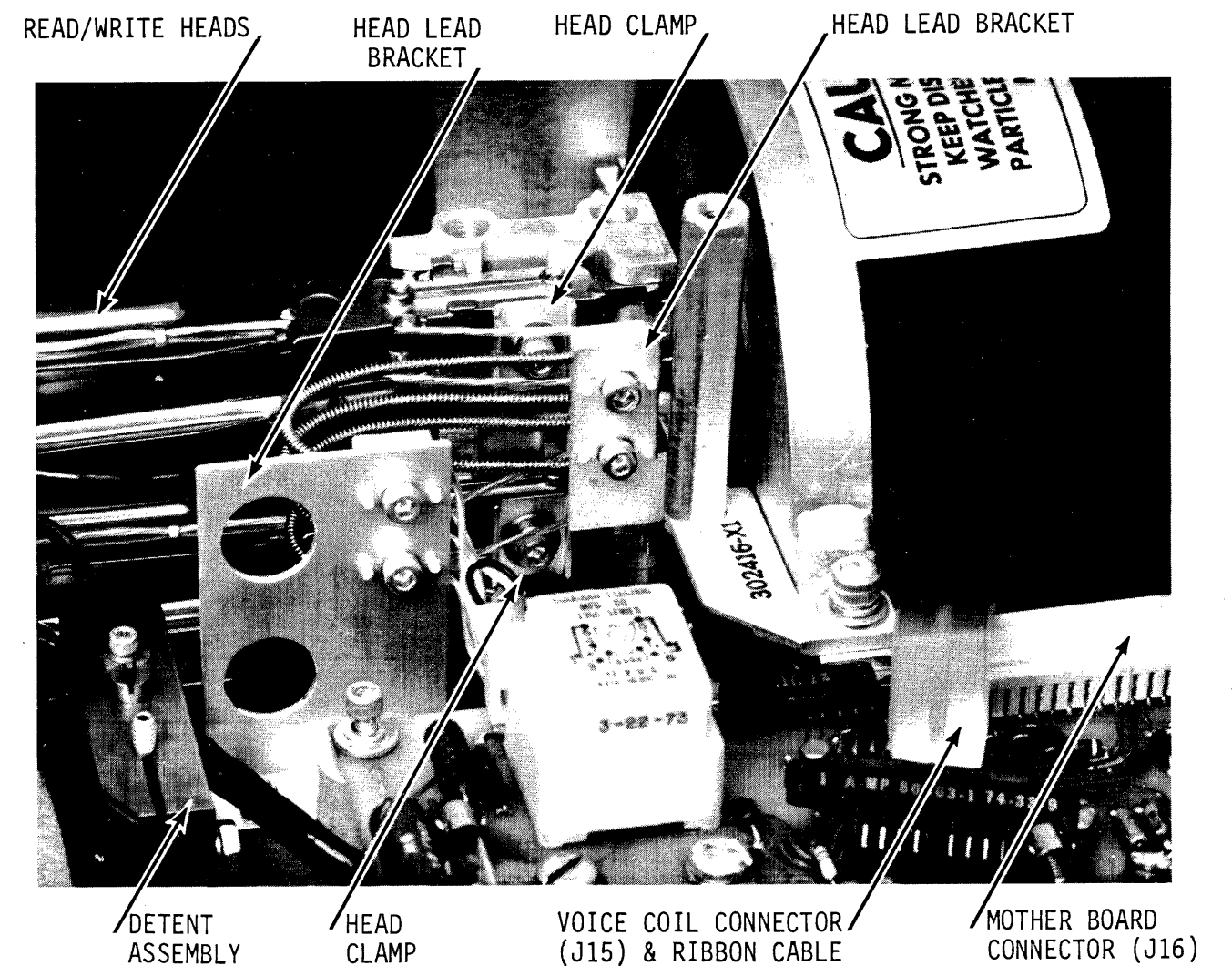


Figure 7-16. Read/Write Heads

4. Remove cap screw securing the head arm clamp for top and bottom heads.
5. Gently set the head assembly away from the ramp support, slightly lifting the top head assembly and depressing near head support. At the same time, pivot the other end of the head assembly away from the head support assembly and slide the head assembly out. (Do not touch the ceramic part or gimbal spring of the head assembly or allow it to contact surfaces, as contact will cause damage to the surface).

NOTE

It may be necessary to use a flat-blade screwdriver to remove the head assembly.

6. Repeat Step a.5 for all head assemblies to be replaced.

NOTE

To remove the bottom head assembly for the fixed disk, remove the top head assembly for the fixed disk first.

b. Replacement

1. Carefully insert the head assembly into the head support (leave 1/8 inch clearance between back of head and head support) and position the top of the head in the head loading area.
2. Install cap screw securing the head lead clamp (ensure that the head arm is on the load cam).
3. Repeat steps b.1 and b.2 for each head assembly being replaced.
4. Install head leads under the carriage head lead clamp.
5. Tighten two cap screws securing the carriage head lead clamp to carriage assembly.
6. Install head leads under the head lead clamps on the head lead bracket and tighten two screws securing the head lead clamps to the head lead bracket.
7. Connect head connectors to the R/WA board. (Head connector locations are identified on the R/WA board).
8. Connect AC power cord and turn on drive Power switch.
9. Perform signal read check, subsection 7.5.16, Step (c).

10. Perform read/write head alignment, Subsection 7.5.16, Step (d).

c. Read Signal Check

- 1. Ensure that the removable and fixed disk Write Inhibit switches are off.
- 2. Set up the Controller to write all ones on track 400 of all disk surfaces.
- 3. Set the oscilloscope as follows:

Sweep Speed	200 ns/cm
Vertical Gain	10 mv/cm
Trigger	TP5 of DTB (REN)
- 4. Connect the oscilloscope probe to TP1 of Read/Write board.
- 5. Set up the Controller to read the ones written on track 400 of each disk surface.
- 6. Record the minimum amplitude of each read signal displayed on the oscilloscope.
- 7. The minimum acceptable amplitude for each of the four heads is 50 millivolts peak-to-peak.
- 8. Set drive Start/Stop switch to Stop position.

d. Head Alignment

NOTE

This procedure assumes that temperature compensation is adjusted and operating correctly.

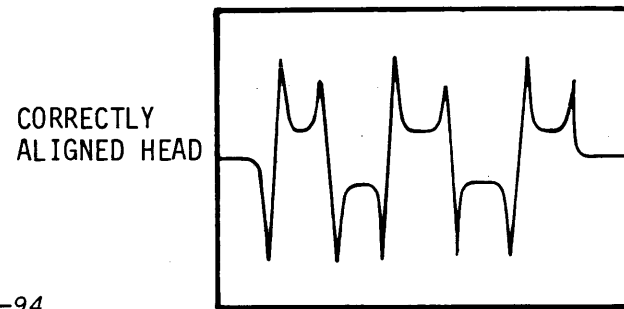
1. Connect Controller to the drive (J21 on I/OB).
2. Turn on removable disk Write Inhibit switch (or disconnect P14 (R/W)).
3. Install jumper between E37 and E38 on I/O board if cartridge is index only.
4. Mount C.E. cartridge on the drive and allow the heads to load.

NOTE

This procedure assumes an EMM/CAELUS Dabit Written Alignment cartridge. For cartridges manufactured by other manufacturers, refer to the manufacturers specifications.

5. Set the oscilloscope as follows:

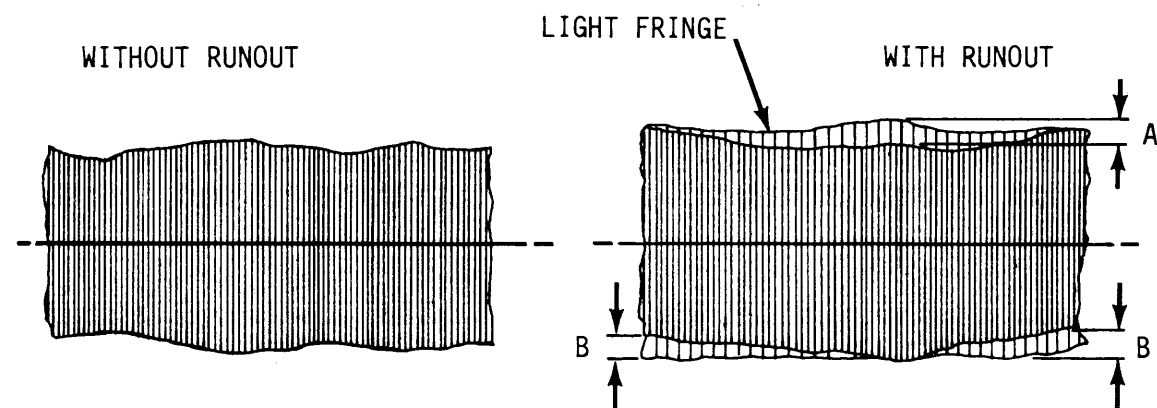
Sweep Speed	5 μ s/cm
Vertical Gain	20 mv/cm
Trigger	Internal
6. Connect oscilloscope probe to TPI on the R/WA.
 - (a) Set up the Controller to select the removable disk, bottom surface head, and seek to track 146.
 - (b) Adjust the removable disk, bottom surface head until dibit information shown in Figure 5-12 is obtained on the oscilloscope.



600-94

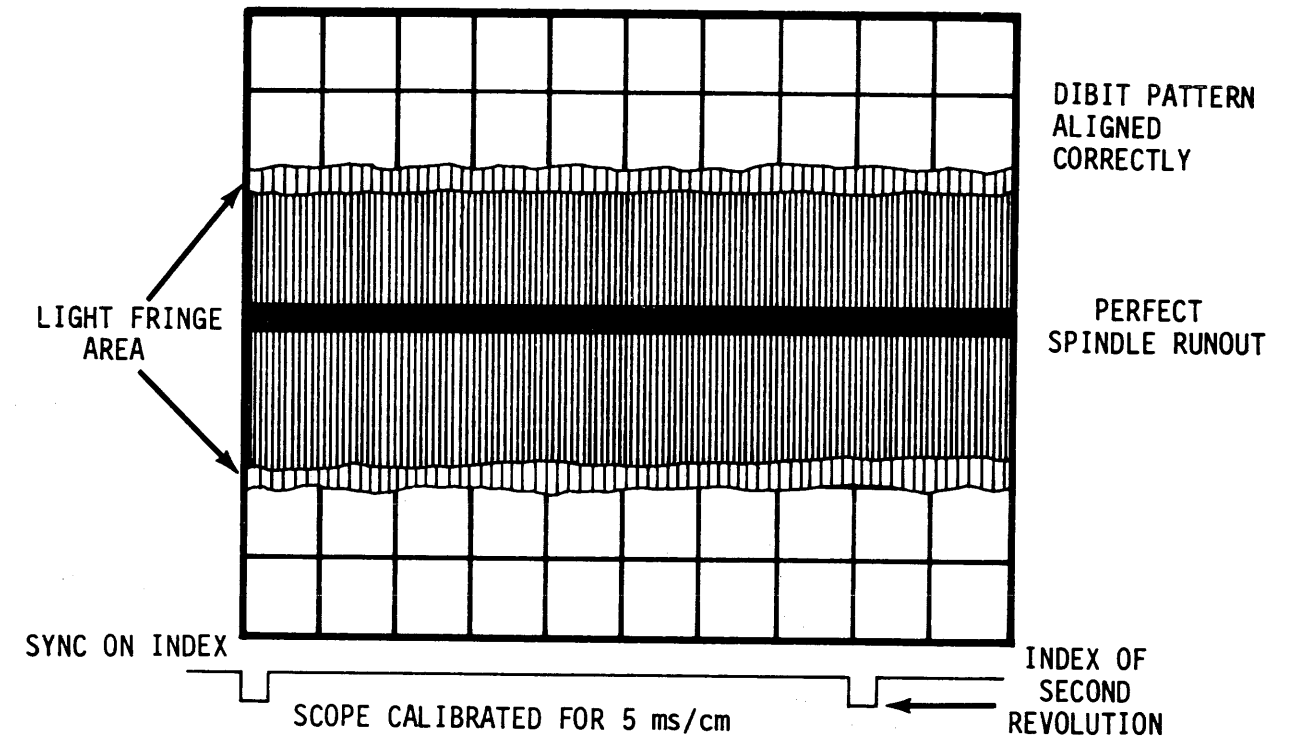
Figure 7-17. Dibit Information Waveform

- (c) Set the oscilloscope sweep speed to 5 ms/cm and trigger External (-) on J22-2.
- (d) Continue to adjust the removable disk, bottom surface head until the dibit pattern fringe areas A and B (refer to Figure 7-18) are equal or as close to equal as possible. (Refer to Figure 7-19).



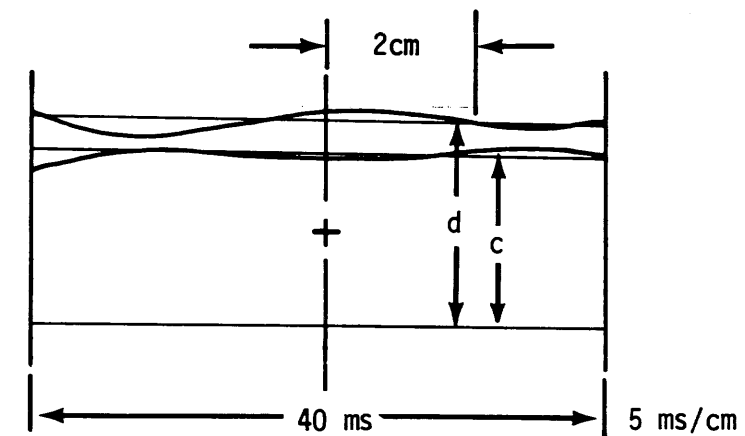
600-95

Figure 7-18. Dibit Pattern and Fringes



600-96

Figure 7-19. Correctly Aligned Dibit Pattern



600-97

Figure 7-20. Dibit Pattern Fringes with Runout Centered on Scope

NOTE

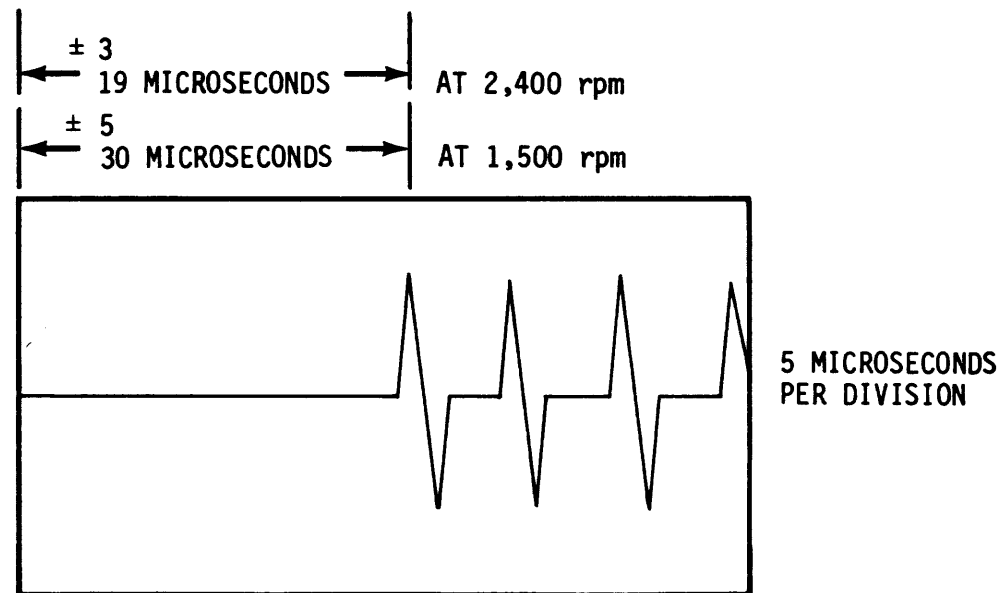
If fringe area equality is obtained in step d, proceed to step f. If fringe area equality is not obtained in step d, perform step e.

- (e) Position the data envelope horizontally so that the maximum point of runout is positioned at the center of the oscilloscope. (Refer to Figure 7-20.) Two centimeters to the left or right of this reference is the point at which average runout is observed and from which measurements c and d (see Figure 7-20) will be taken. The ratio of $c/d \times 100$ must be 85 percent or greater.
- (f) Repeat steps (a) through (e) for removable disk, top surface head.
- (g) To align the removable disk index transducer, set up the Controller to access track 10 of the removable disk, top surface.

Set the oscilloscope as follows:

Sweep Speed	5 μ s/cm
Vertical Gain	20 mv/cm
Trigger	External (-), J22-2

- (h) Adjust the removable disk index transducer or index pulse delay (R87 on DCB) as required until the peak of the first pulse (positive or negative) after the DC erase zone is located 30 ± 5 microseconds at 1,500 rpm or 19 ± 3 microseconds at 2,400 rpm from the leading edge of the index pulse. (Refer to Figure 7-21.)



600-98

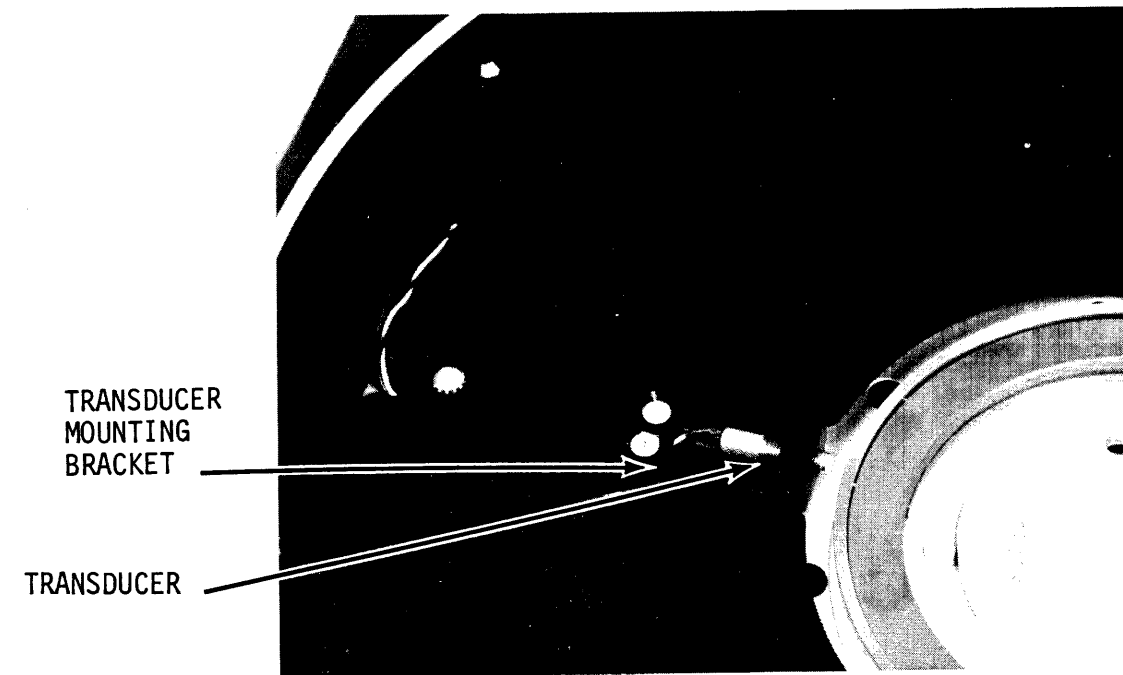
Figure 7-21. Index Alignment

- (i) Set up the Controller to access track 10 of the removable disk, bottom surface, and repeat step (h). Both heads are required to fall within the specifications given.
- (j) When head alignment is complete, disconnect oscilloscope leads and set drive Start/Stop switch to Stop position.
- (k) Turn off drive Power switch.
- (l) Replace top and rear covers.

7.5.17 Removable Disk Index/Sector Transducer

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove disk cartridge.
3. Remove top cover.
4. Loosen set screw that holds the transducer in the transducer mounting bracket. (Refer to Figure 7-22).



600-99

Figure 7-22. Removable Disk Index/Sector Transducer

5. Unsolder twisted-pair cables from transducer terminals.
6. Rotate the transducer counterclockwise as viewed from the front of drive to remove the transducer from the mounting bracket.

b. Replacement

1. Install the replacement transducer through the transducer mounting bracket.
2. Install the test hub on the drive.
3. Adjust the transducer until there is a 0.005-inch separation between the transducer and test hub.
4. Ensure that 0.005 inch clearance between the transducer and test hub exists through full hub rotation.
5. Remove the test hub and replace with the disk cartridge.
6. Connect AC power cord and turn on drive Power switch.
7. The transducer can now be checked for electrical alignment.

c. Removable Disk Transducer Alignment

1. Set drive Start/Stop switch to Start position.
2. Set the oscilloscope as follows:

Sweep Speed	5 ms/cm
Vertical Gain	50 mv/cm
Trigger	Internal
3. Connect the oscilloscope probe to TP2 on the DCB.
4. Adjust the removable disk index/sector transducer output for 200 mv to 600 mv measured base-to-peak if using .020-inch slotted hub, and from 800 mv to 1.5V if using a .080-inch slotted hub.

NOTE

Make sure the removable disk index/sector transducer waveform starts in a positive direction as shown in Figure 7-24. If not, the polarity is reversed at the transducer.

5. When removable disk index/sector transducer alignment is complete, perform circumferential alignment, subsection 7.5.16.d.6(g, h and i).

7.5.18 Fixed Disk Index/Sector Transducer

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Disconnect mating connector at the transducer located on the underside of the baseplate. (Refer to Figure 7-23.)
3. Loosen set screw that holds transducer in the transducer mounting bracket.
4. Rotate the transducer counterclockwise, viewing from the transducer toward the sector ring.

b. Replacement

1. Rotate replacement transducer clockwise through the transducer mounting bracket.
2. Use the 0.005-inch mylar shim to adjust the transducer until there is a 0.005-inch separation between the transducer and sector ring.
3. Ensure that the 0.005-inch minimum clearance exists through full hub rotation.
4. Connect transducer cable connector with shielded wire mating to the unmarked transducer terminal.
5. Connect AC power cord and turn on drive Power switch.
6. The transducer can now be checked for electrical alignment.

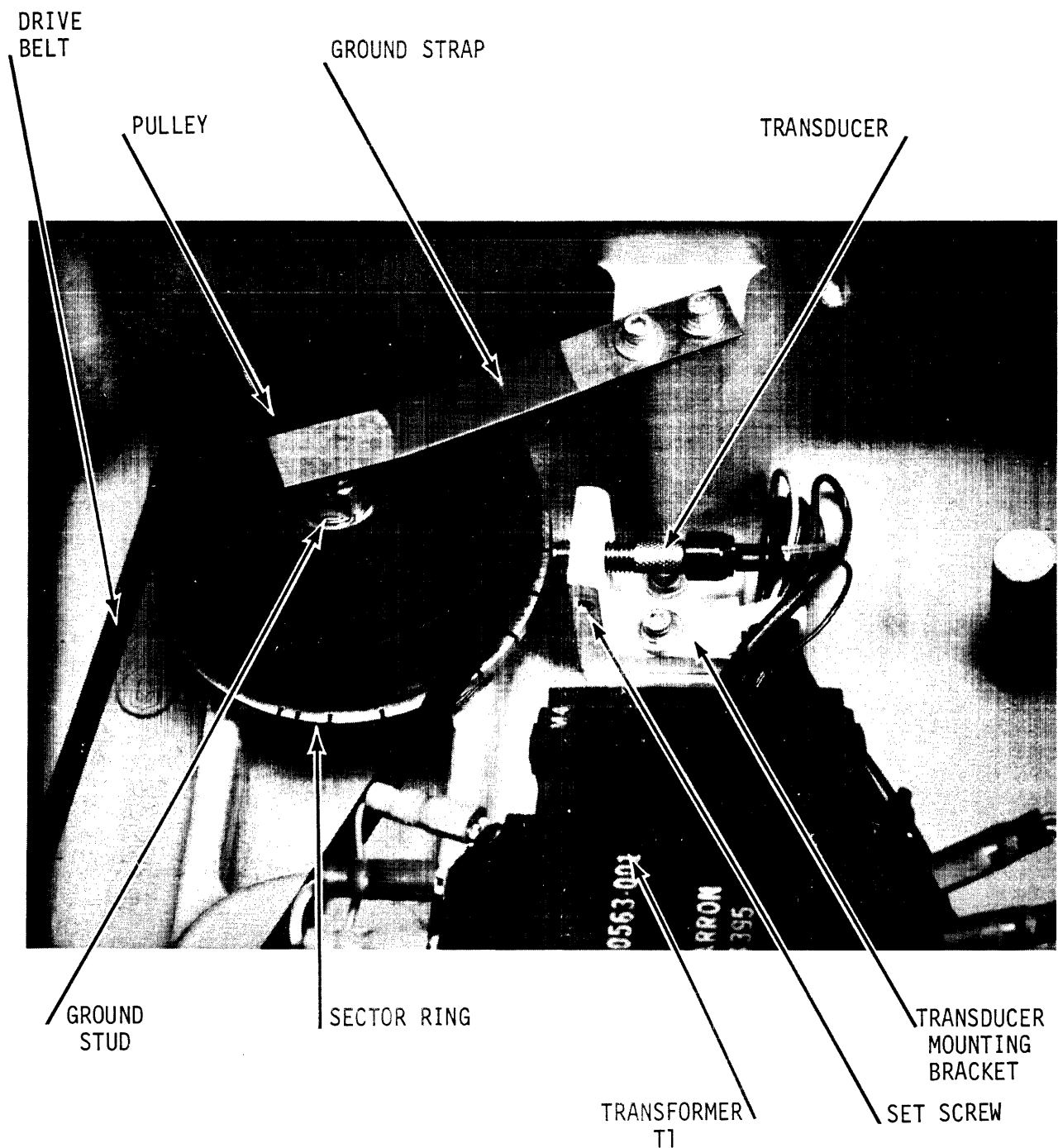
c. Fixed Disk Transducer Electrical Alignment

NOTE

If a disk cartridge is not installed, place a Q-tip between the pack on interlock switch and the interlock arm to close (activate) S8, and place the throw in its rearmost position to activate S9. This enables power to be supplied to the spindle motor.

1. Disconnect voice coil from PCM and turn on drive Power switch.
2. Set drive Start/Stop switch to Start position.
3. Set the oscilloscope as follows:

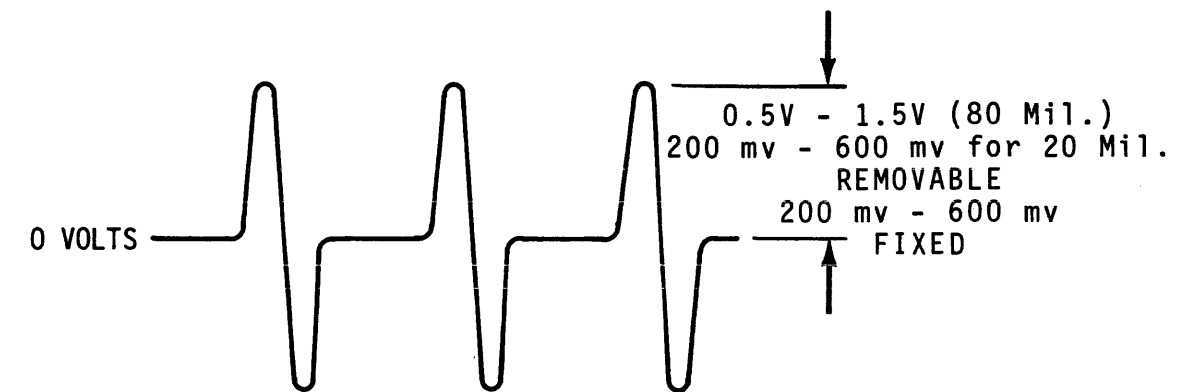
Sweep Speed	5 ms/cm
Vertical Gain	50 mv/cm
Trigger	Internal



600-100

Figure 7-23. Fixed Disk Index/Sector Transducer

4. Connect the oscilloscope probe to TP1 on the DCB.
5. Verify that the fixed disk index/sector transducer output agrees with the waveform shown in Figure 7-24.



600-101

Figure 7-24. Index/Sector Transducer Output Waveform

6. Adjust the fixed disk index/sector transducer for an output of not less than 200 millivolts and not more than 600 millivolts measured base-to-positive-peak.

NOTE

Make sure that the fixed disk index/sector transducer waveform starts in a positive direction as shown in Figure 7-24. If not, the polarity is reversed at the transducer.

7. When fixed disk index/sector transducer alignment is complete, disconnect oscilloscope leads and set drive Start/Stop switch to Stop position.
8. Turn off drive Power switch.
9. Connect J15 to the PCM.
10. Replace top and rear covers.

7.5.19 Spindle Motor Belt (Refer to Figure 7-25.)

NOTE

Under normal operating conditions and with proper tension, the spindle motor belt should last the lifetime of the machine. Proper belt tension must be maintained to avoid excessive wear.

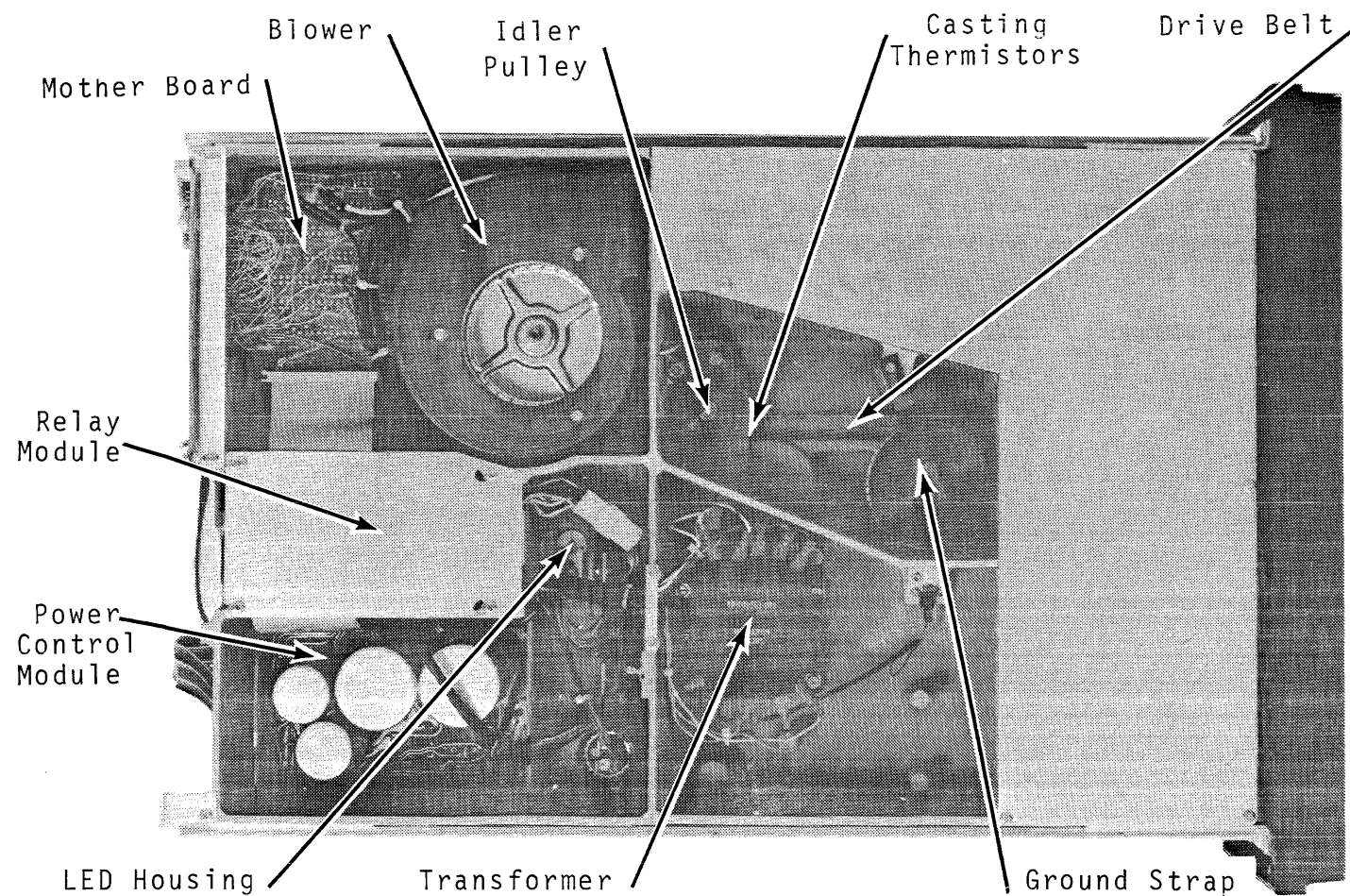


Figure 7-25. Model 206, Bottom View

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove three cap screws securing the blower inlet cover to the blower housing. Remove blower inlet cover.
3. Loosen blower impeller set screw and remove the blower impeller.
4. Remove three blower housing mounting screws and remove blower housing.

CAUTION

Exercise care not to damage rubber seal between the blower outlet and air plenum cover when removing blower housing.

5. Remove two ground strap mounting screws and remove ground strap.
6. Loosen the idler pulley holding screw to relieve spindle motor belt tension.
7. Remove the spindle motor belt.

b. Replacement

1. Slide replacement spindle motor belt over the motor pulley taking care not to disturb the sector transducer.
2. Ensure that the belt is centered on the motor pulley.
3. Use the gram gauge (Scherr-Tumico, Part Number 63-6383) to adjust spindle motor belt tension by applying pressure against the idler pulley.
4. When tension reads between 1,500 and 2,000 grams, tighten the idler pulley holding screw while maintaining pressure against the idler pulley.
5. Position ground strap on baseplate and install two mounting screws.
6. Position blower housing and install three mounting screws.
7. Install blower impeller and tighten blower impeller set screw.
8. Position blower inlet cover on the blower housing and install three mounting screws.

7.5.20 Fixed Disk

a. Removal

NOTE

Before removing the fixed disk, transfer data to another storage location.

1. Turn off drive Power switch and disconnect AC power cord.

2. Remove the disk cartridge.
3. Disconnect the write/inhibit switch plug (P14) and the latch solenoid plug.
4. Remove six shroud assembly mounting screws and remove shroud assembly.
5. Remove three shield assembly mounting screws.

CAUTION

Exercise care not to damage index/sector transducer or fixed disk when removing the shield assembly.

6. Remove shield assembly.
7. Remove eight screws securing clamp ring to the spindle assembly.
8. Remove clamp ring and store flat, protected by tissue.
9. Remove fixed disk.

b. Replacement

NOTE

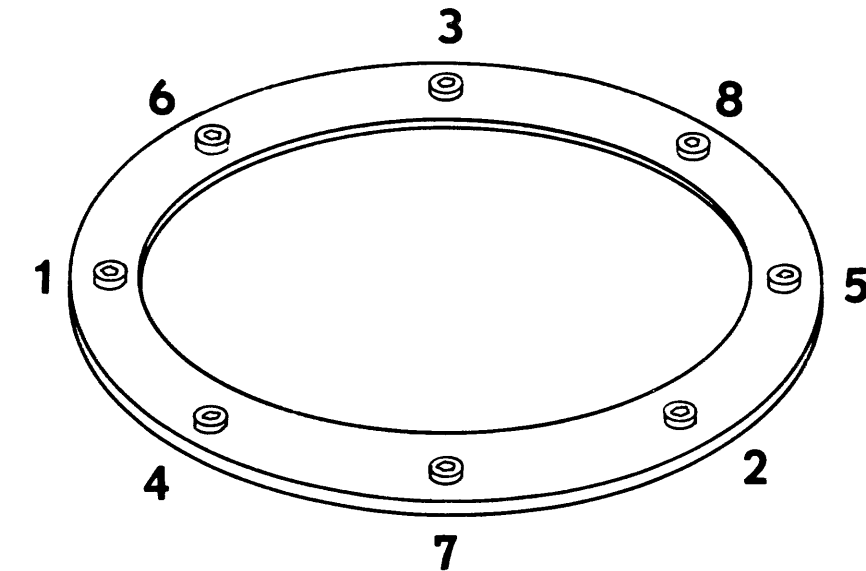
A new fixed disk is supplied in EMM-Caelus Fixed Disk Replacement Kit, Catalog No. 306, which also contains a nylon handling glove.

1. Thoroughly clean the cavity of the drive, using first a vacuum cleaner then isopropyl-alcohol-moistened tissues. Revacuum to remove any tissue lint.
2. Wipe the spindle assembly chuck and clamp ring.
3. Upon opening the disk shipping container, handle the disk only with the nylon glove.
4. Moisten a lint-free tissue with isopropyl alcohol and clean the lower surface of the disk.
5. Dry the lower surface of the disk with a dry tissue.
6. Still wearing the nylon glove, carefully place the replacement disk on the spindle assembly without allowing the coated surface to touch any part of the drive.

CAUTION

The spindle assembly chuck has a machined ridge which will align the disk to the spindle assembly but care must be exercised to ensure that the disk is properly seated.

7. Position the clamp ring and install the eight mounting screws.
8. Tighten the eight clamp ring mounting screws in sequence shown in Figure 7-26 to a torque of 18 ± 2 inch-pounds.



600-103

Figure 7-26. Fixed Disk Clamp Ring Screw Pattern

9. Inspect fixed disk top surface for foreign particles and repeat steps 4 and 5 to clean disk top surface.
10. Position shield assembly on baseplate and install mounting screws.
11. Position shroud assembly on baseplate and install six mounting screws.

12. Connect the write/inhibit switch plug (P14) and the latch solenoid plug.
13. Install the disk cartridge.
14. Connect AC power cord and turn on drive Power switch.
15. Perform circumferential alignment, subsection 7.5.12, step d.6(g).

NOTE

It is necessary to format fixed disk prior to returning the drive to system operation.

7.5.21 Spindle Assembly

a. Removal

1. Remove the fixed disk. (Refer to subsection 7.5.20.)
2. Remove the spindle motor belt. (Refer to subsection 7.5.19.)
3. Use a wrench (not pliers) to remove the ground stud from the spindle assembly to permit removal of the spindle pulley.
4. Remove spindle pulley.
5. Remove three spindle holddown screws through spindle chuck access holes. Care should be taken in removing the spindle as metal chips in the area of the spindle make it difficult to remove because of close tolerances.
6. The spindle assembly can now be removed from the top of the drive.

b. Replacement

1. Thoroughly clean the cavity of the drive using isopropyl-alcohol-moistened tissues.
2. Carefully install spindle assembly in baseplate.
3. Install spindle and secure with three holddown screws.
4. Position spindle pulley on spindle assembly.
5. Use a wrench (not pliers) to install ground stud, securing the spindle pulley to the spindle assembly.
6. Replace the spindle motor belt. (Refer to subsection 7.5.19.)
7. Replace the fixed disk. (Refer to subsection 7.5.20.)

7.5.22 Velocity Transducer/Positioner Motor/Carriage

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove the I/O board. (Refer to subsection 7.5.5.)
3. Remove the R/WA board. (Refer to subsection 7.5.3.)
4. Remove the read/write heads. (Refer to subsection 7.5.16.)
5. Remove the mask assembly. (Refer to subsection 7.5.25.)
6. Disconnect J15 from the PCM.
7. Move the carriage assembly as far toward the spindle as practical.
8. Loosen the velocity transducer set screw two turns. This set screw is threaded into the positioner motor core and is accessible through a hole in top of the positioner motor. (Refer to Figure 7-27.)
9. Pull the velocity transducer out from the rear of the positioner motor and unplug from Mother board.
10. Remove four socket head screws securing the positioner motor to the baseplate.
11. Remove positioner motor by carefully sliding positioner motor to the rear while holding its weight off the voice coil.

CAUTION

Cover all openings of positioner motor with masking tape prior to setting down. Set positioner motor, rear end down, on a clean surface. This will prevent debris from being ingested into the positioner motor.

12. Place the drive on its side if necessary for access to holes in bottom of baseplate.

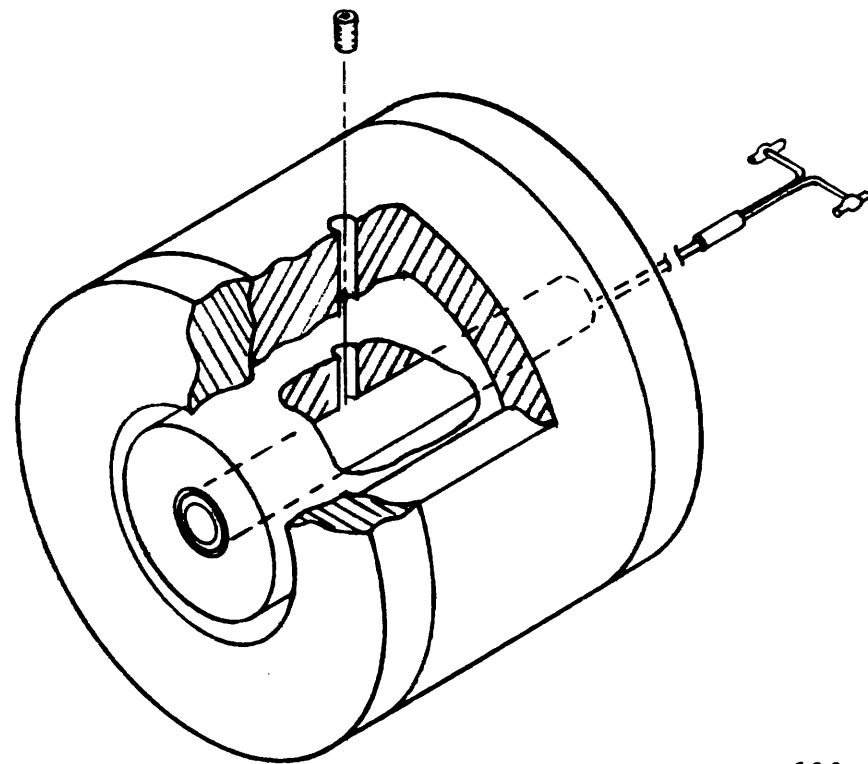
NOTE

The carriage race assembly is held in place with the carriage tension spring located on the bottom of the carriage assembly.

NOTE

Access to the carriage tension spring mounting screws is available through three holes located on the underside of the baseplate.

13. Through the three access holes, loosen but do not remove the three carriage tension spring holddown screws.
14. From the top of the drive, remove the flex circuit holddown clamp.



600-104

Figure 7-27. Velocity Transducer Removal

15. Remove two screws securing the guide retainer plate to the baseplate at rear of the carriage assembly.
16. While holding the race assemblies (located on either side of the carriage assembly), carefully slide the carriage assembly out of the baseplate.

NOTE

The carriage race assemblies ride on guide shafts inside the baseplate.

17. Remove all guide shafts from the baseplate.

CAUTION

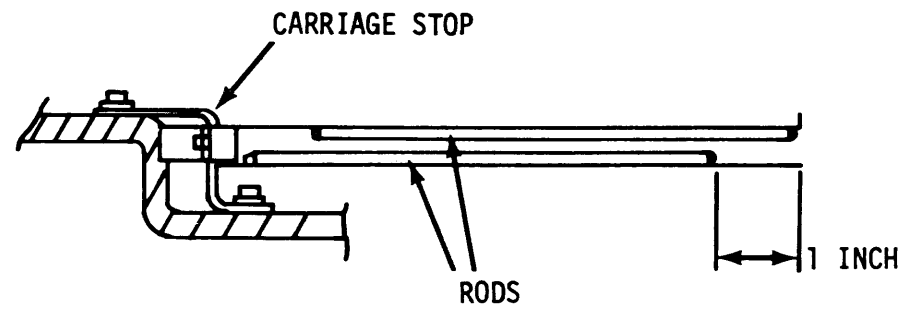
Do not remove the head support from the carriage assembly. The head support is located to the carriage assembly at the factory and cannot be aligned in the field.

b. Replacement

NOTE

Prior to replacing the carriage assembly, clean baseplate and all guide shafts with isopropyl alcohol/water mixture.

1. If the voice coil assembly was removed from the carriage assembly, loose assemble the replacement voice coil assembly to the head support bracket with the two voice coil mounting screws.
2. Loose assemble the flex and carriage tension spring to the bottom of the carriage assembly with three mounting screws.
3. Prepare guide shafts by wiping with a Kimwipe and very lightly greasing (Aero Shell Grease No. 7/GIA).
4. Position the four "long" guide shafts in baseplate channels with the bottom two pushed toward the spindle as far as possible (against the stop) and the two on top protruding approximately 1 inch farther out than the bottom guide shafts. (Refer to Figure 7-28.)
5. Position four "short" guide shafts in carriage assembly channels.
6. Install race assemblies in the carriage assembly as shown in Figure 7-29.



600-105

Figure 7-28. Carriage Guide Shaft Positioning

NOTE

The underneath side of the carriage casting springs accepts the race with the short end. The longer end race mounts to the other side. Mount the races such that the star wheels engage with the racks when the ends are flush with the ends of the carriage.

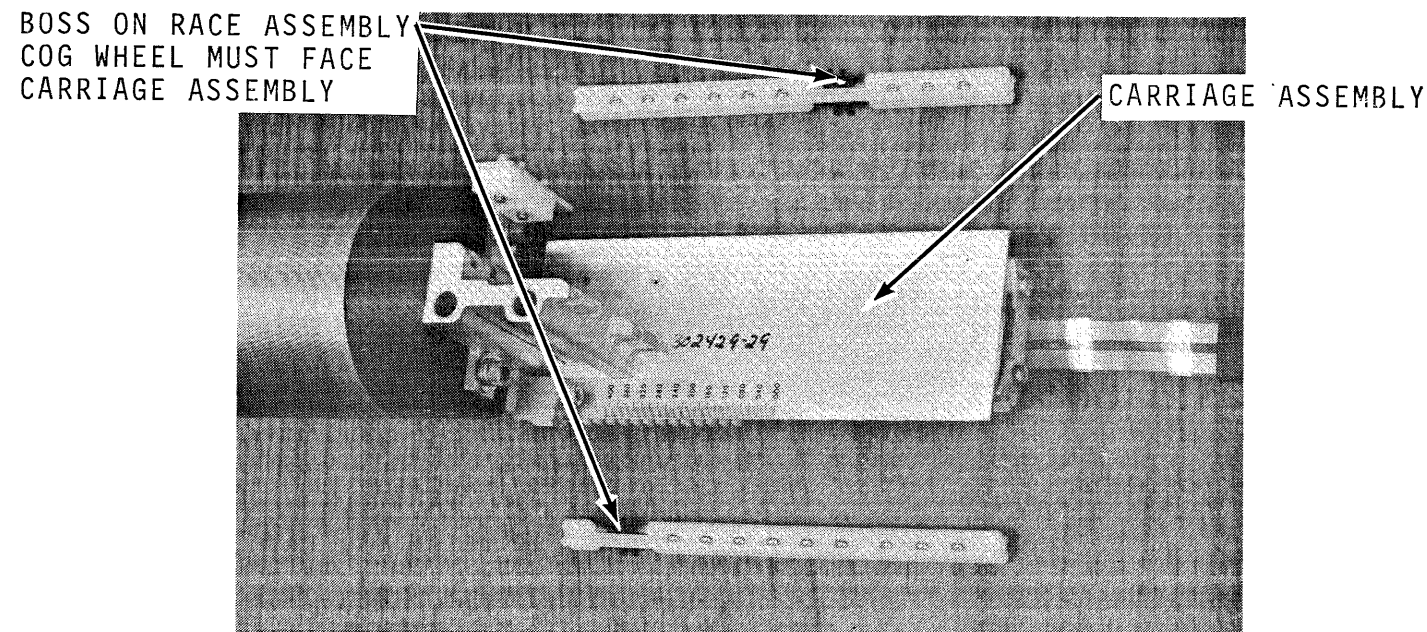


Figure 7-29. Race Assembly Installation

NOTE

To position the races, pull the carriage back until the races disengage; they can then be slipped into a new position.

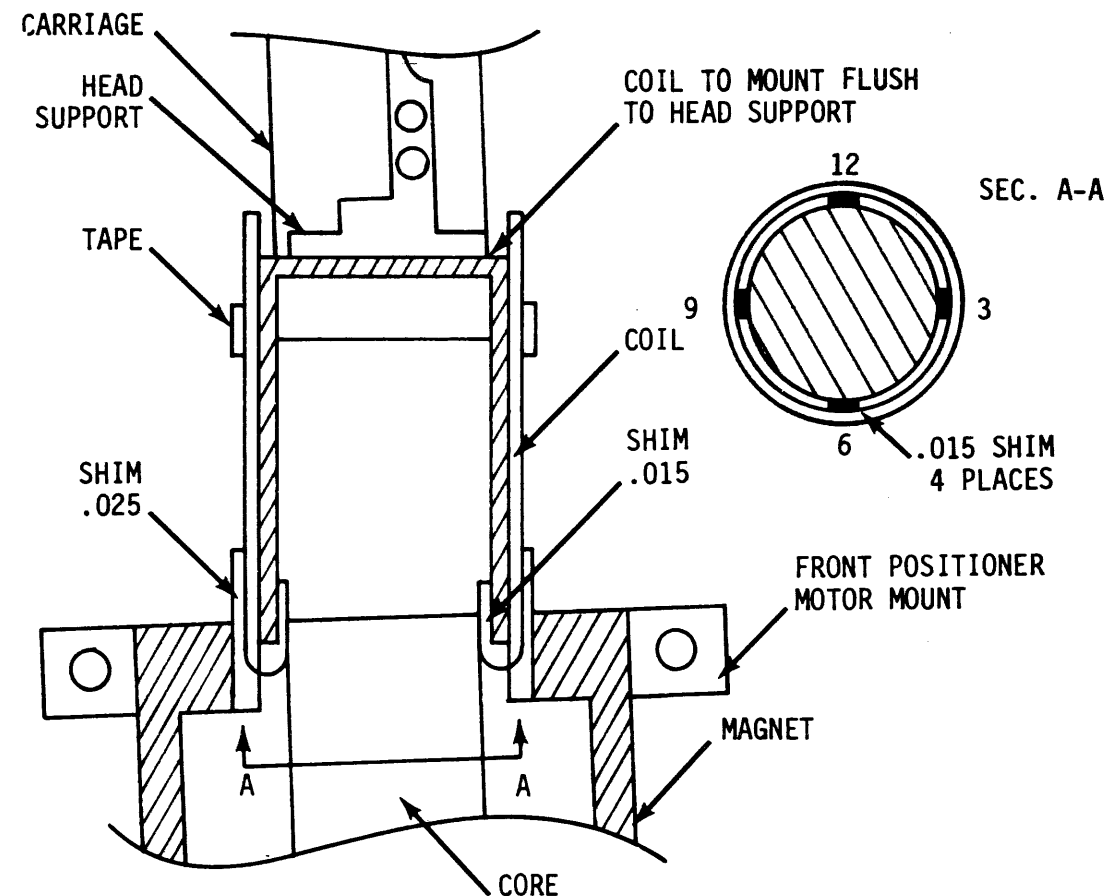
7. Install assembled carriage assembly in baseplate.
8. With the carriage assembly installed in the drive, move the carriage to the forward stop position (maximum travel).
9. Look from the back of the drive and locate the left-hand race assembly such that 2-28/32 inches \pm 1/16 inch are available from the end of the race to the end of the carriage channel.
10. Look from the back of the drive and locate the right-hand race assembly such that it measures the same as the left-hand assembly.
11. Position the guide retainer plate on the baseplate at the rear of the carriage assembly and install two mounting screws.
12. Tighten the three carriage tension spring mounting screws through the access holes in the bottom of the baseplate and replace flex circuit holddown clamp.
13. Locate four 0.015-inch shims on the voice coil assembly at 12, 3, 6, and 9 o'clock. (See Figure 7-30.) Secure shims to voice coil with Scotch tape.
14. Loosen two socket head screws securing the voice coil assembly to the head support.
15. Use a rubber band to secure the carriage assembly in a forward position toward the spindle.
16. Loose assemble the positioner motor on the baseplate.
17. Align the positioner motor for equal clearance around all four mounting holes and temporarily tighten two front mounting screws.
18. With the four 0.015-inch shims centering the voice coil assembly to the core of the positioner motor magnet, locate the mounting end of the voice coil on the head support so that it is seated at top, bottom, and both sides. Tighten the two voice coil assembly mounting screws. (See Figure 7-30.)
19. Remove the positioner motor from the drive and remove the two 0.015-inch shims located at 6 and 12 o'clock on the voice coil assembly.
20. Loose assemble the positioner motor on the baseplate.
21. Release the carriage assembly and move the voice coil into the positioner motor to the home position, aligning the positioner motor to the point where the voice coil does not bind and clearance around the positioner motor core is even.

22. Use the two inner mounting holes to secure the two metal stops (supplied with Voice Coil Alignment Kit) against the rear mounts of the positioner motor.

NOTE

One mounting hole is used for the I/O board support.

23. Move the carriage assembly to the stop position toward the spindle and measure the space between the positioner motor and voice coil assembly. There should be approximately 0.025 inch clearance on both sides of the voice coil assembly.
24. Carefully remove the positioner motor from the baseplate. (Do not disturb the position of the metal stops installed in step 22.)



600-107

Figure 7-30. Voice Coil to Carriage Alignment

25. Remove the remaining 0.015-inch shims from the voice coil assembly.
26. Reinstall the positioner motor on the baseplate.
27. Move the carriage assembly to the stop position and set the outside of the voice coil to positioner motor clearance using 0.025-inch shims.
28. Tighten the four socket head screws securing the positioner motor to the baseplate. Remove the two metal stops.
29. Install the velocity transducer in the positioner motor (transducer should protrude 1/4 inch from the rear of the positioner motor).
30. Tighten the velocity transducer set screw through the access hole in positioner motor.
31. Replace the mask assembly. (Refer to subsection 7.5.25.)
32. Replace the read/write heads. (Refer to subsection 7.5.16.)
33. Replace the I/O board support and install two mounting screws.
34. Replace the I/O board. (Refer to subsection 7.5.5.)
35. Replace the R/WA board. (Refer to subsection 7.5.3.)
36. Connect J15 to the PCM.
37. Connect AC power cord and turn on drive Power switch.
38. The read/write heads can now be checked for electrical alignment. (Refer to subsection 7.5.16.)

7.5.23 Air Filter

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove eight screws securing plenum cover to bottom of baseplate.
3. Carefully lower plenum cover and remove air filter.
4. If the filter is dirty or damaged, it should be discarded.

b. Replacement

NOTE

Prior to installing new air filter, the plenum area of the baseplate should be vacuumed and wiped clean with isopropyl alcohol/water solution.

1. Position air filter in baseplate opening with airflow direction arrow pointing toward the fixed disk.
2. Refit plenum cover to baseplate, ensuring that seal is intact.
3. Install eight screws securing plenum cover to baseplate.
4. Connect AC power cord and turn on drive Power switch.

7.5.24 Spindle Motor Assembly

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Disconnect plug P24 on the spindle drive motor (yellow wire).
3. Remove relay module cover mounting screw and remove relay module cover.
4. Disconnect blue and red spindle motor wires.

NOTE

The blue wire is connected to relay K1 in both 1,500- and 2,400-rpm drives. The red spindle motor lead is connected to relay K2 in a 1,500-rpm drive and to start capacitor C1 in a 2,400-rpm drive.

5. Carefully withdraw red and blue motor wires through opening in relay module and baseplate.
6. Remove spindle motor belt. (Refer to subsection 7.5.19.)
7. Place the drive in an upright position and remove four screws securing the spindle motor assembly to the baseplate.
8. Remove the spindle motor, pulley, and impeller shaft through the top of the baseplate.

CAUTION

The spindle motor assembly (motor, pulley, and impeller shaft) should be left assembled as they are preadjusted for height at the factory. If it should become necessary to disassemble the spindle motor assembly, use EMM-Caelus Drive Pulley Adjustment Tool No. 430366 to reassemble.

b. Replacement

NOTE

Replacement spindle motor assemblies are supplied complete with leads, plug P24, and lugs.

1. Position spindle motor assembly on baseplate.
2. Secure spindle motor assembly to baseplate with four mounting screws.
3. Route red and blue motor wires through hole in baseplate and into relay module.
4. Connect blue motor wire to terminal 3 of relay K1 in the relay module.
5. Connect red motor wire to terminal 2 of relay K2 in a 1,500-rpm drive and to start capacitor C1 in a 2,400-rpm drive.
6. Replace relay module cover and install cover mounting screw.
7. Connect the yellow motor wire to plug P24 on the main harness.
8. Replace the spindle motor belt. (Refer to subsection 7.5.19.)
9. Connect AC power cord and turn on drive Power switch.

7.5.25 Mask Assembly

CAUTION

Exercise extreme care not to damage read/write heads when removing and replacing mask assembly.

NOTE

Replacement of the mask assembly will cause the read/write heads to become misaligned. If possible, transfer data from fixed disk to temporary storage prior to replacing the mask assembly. If this is not possible, the fixed disk read/write heads must be aligned to the prerecorded data after replacement of the mask assembly.

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove the R/WA board. (Refer to subsection 7.5.3.)
3. Remove the head clamp support.

CAUTION

The mask-to-detent clearance is set at 0.005 inch. Therefore, extreme care must be exercised to prevent detent assembly damage when removing the mask assembly.

4. Remove screw holding the mask assembly in place and rotate the mask from under the detent assembly.

b. Replacement

CAUTION

Exercise extreme care to prevent detent damage when replacing the mask assembly.

1. Position mask assembly on the carriage with the shoulder on the underside of the mask assembly flush with the edge of the carriage. (See Figure 7-30.)
2. Install screw on the mask assembly.
3. Replace the head clamp support.
4. Replace the R/WA board.
5. Connect AC power cord and turn on drive Power switch.
6. Perform read/write head alignment. (Refer to subsection 7.5.16.)

7.5.26 Detent Assembly

CAUTION

Transfer data on the fixed disk to another disk. Unless a track has been prerecorded to align the heads, data stored on the fixed disk may not be recovered when the detent assembly is aligned.

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Disconnect J15 from PCM.
3. Disconnect J6 from underneath Mother board.
4. Loosen Allen screw on back of detent assembly. (See Figure 7-31.)
5. Slide the detent assembly up and off its mounting post on the baseplate.

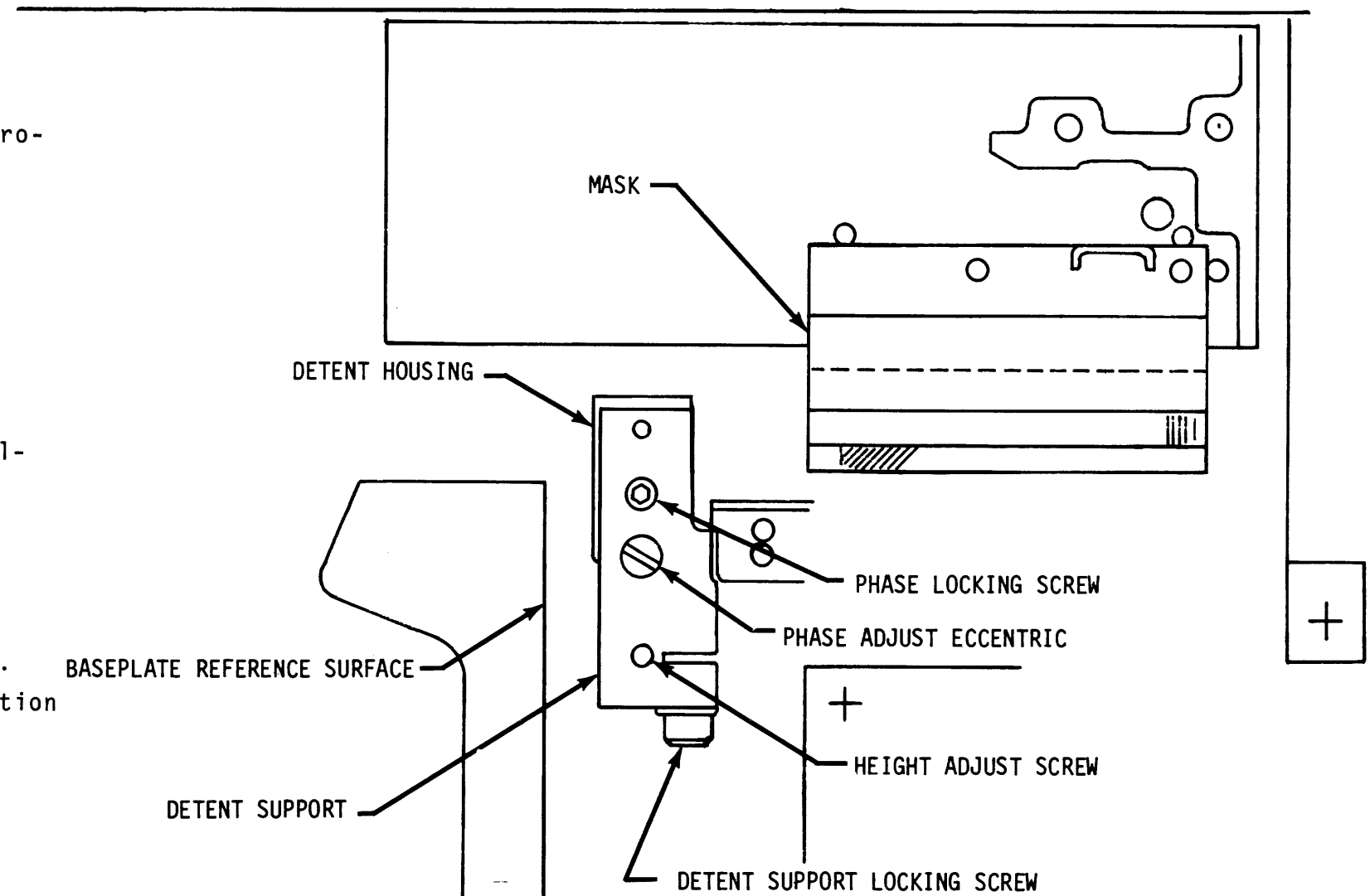


Figure 7-31. Optical Detent System (Viewed from Top)

b. Replacement

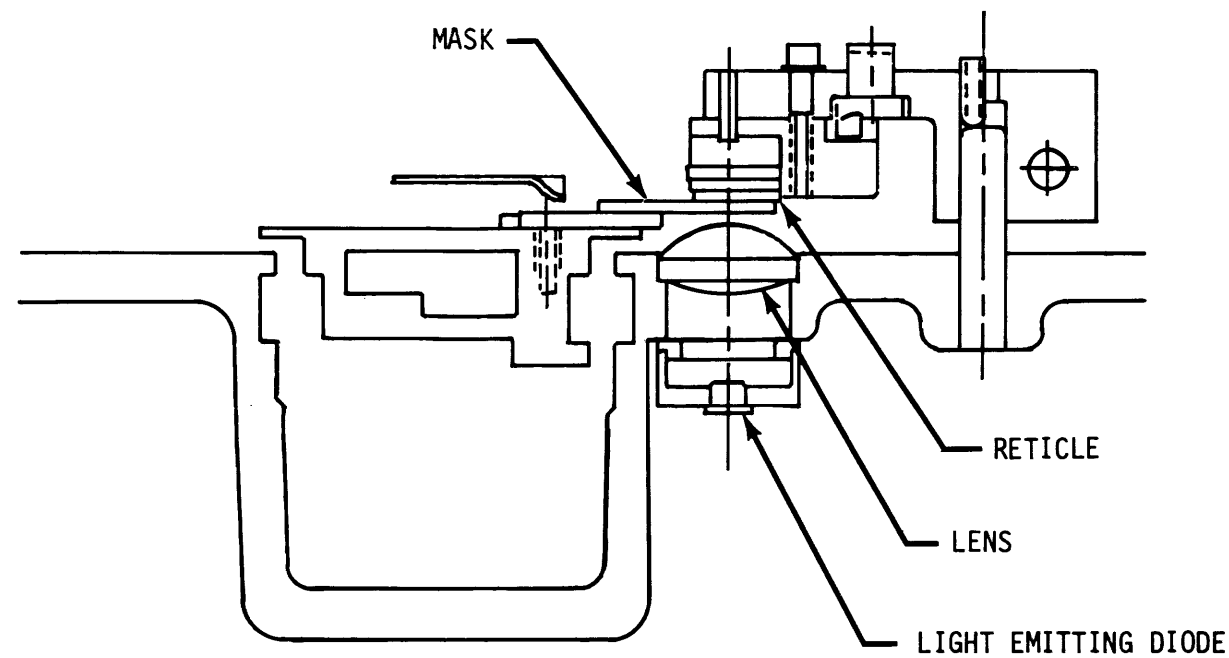
1. Install detent assembly on its mounting post. (See Figures 7-31 and 7-32.)
2. Place a 0.005-inch mylar shim between the detent assembly and the mask assembly.
3. Slide the detent assembly down until there is 0.005 inch clearance between the mask and detent assemblies.
4. Tighten the Allen screw on the back of the detent assembly. Recheck clearance with the 0.005-inch shim.
5. Connect AC power cord and turn on drive Power switch.
6. The detent assembly can now be checked for electrical alignment.

7.5.27 Detent Alignment

a. Detent Alignment--Mechanical (Refer to Figures 7-31 and 7-32.)

NOTE

This alignment must be performed with the positioner motor disconnected (P15 on PCM). Be sure the disk is up to speed to avoid head or disk damage.



600-109

Figure 7-32. Detail of Detent Optics

1. Align detent support by rotating it as necessary so that the detent housing is positioned directly over the center of the lens.
2. Set the height adjust screw for a light fit with a 0.005-inch shim between the mask and reticle.
3. Tighten detent support locking screw. Recheck a and b. Move the carriage through its complete range of travel.

b. Detent Assembly Signal Output Check

1. Remove plug P15 (servo) from the PCM.
2. Remove plug P6 from the Mother board.
3. Power drive on and allow spindle to rotate.
4. Loosen the hex head screw on the detent block assembly.

NOTE

See Figure 7-33 for P6 pin number assignments.

5. Using an oscilloscope, monitor P6, pin 4. Use P6, pin 1 for scope ground.

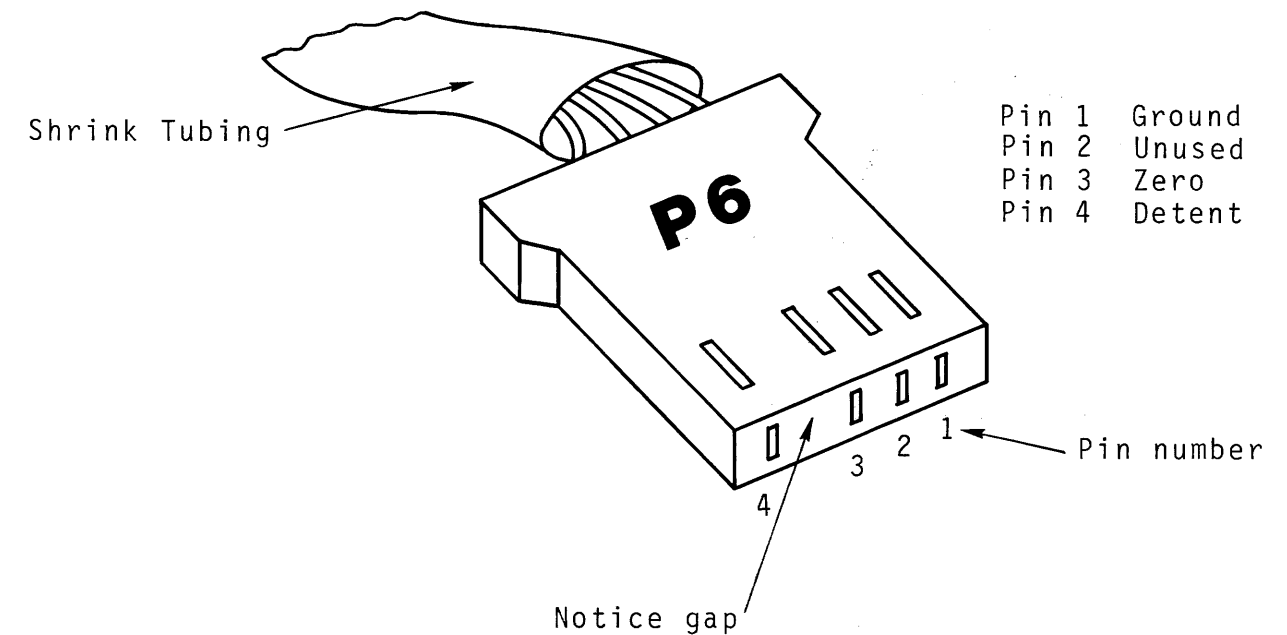


Figure 7-33. Plug P6 Pin Assignment

6. While moving the carriage by hand, adjust the eccentric screw on the detent block assembly for maximum peak-to-peak amplitude. Minimum acceptable amplitude is 300 mv peak-to-peak.
7. Tighten down the hex head screw that holds the detent block secure.
8. Recheck Step 6.
9. Monitor P6, pin 3 (zero). Ground scope on P6, pin 1.
10. While moving the carriage by hand between track 0 and 407, insure that an amplitude of at least 50 mv peak-to-peak is present.

c. Detent Alignment Electrical

NOTE

Anytime the detent block is aligned mechanically it will be necessary to do detent electrical alignment. Procedure follows this note.

1. Ground TP3 and TP6 (TCB).
2. Detent Balance Electrical
 - (a) Monitor TP3 (SAB).
 - (b) While moving the carriage by hand, adjust R2 (SAB) so that the signal at TP3 swings evenly above and below ground.
3. Detent Amplitude Electrical
 - (a) Monitor TP5 (SAB).
 - (b) While moving the carriage by hand, adjust R3 (SAB) so that the signal at TP5 is 5 volts \pm 0.1 volts peak-to-peak.
4. Check Zero Photo Cell
 - (a) Monitor TP8 (TCB).
 - (b) Insure that TP8 goes from ground to a logic high (+5V) when the carriage is moved by hand through track 0 coming from home position.
5. Move carriage by hand to home position and turn off disk.
6. Reconnect plug P15 (PCM).
7. Unground TP3 and TP6 (TCB).

d. Zero Adjustment ("R" model only)

1. Do alternate seeks between tracks 0 and 3 using a DTU-2 or computer.
2. Set up scope as per Figure 7-34.
3. Using R2 (TCB), adjust the positive transition of TP8 to fall within the area shown in Figure 7-34.

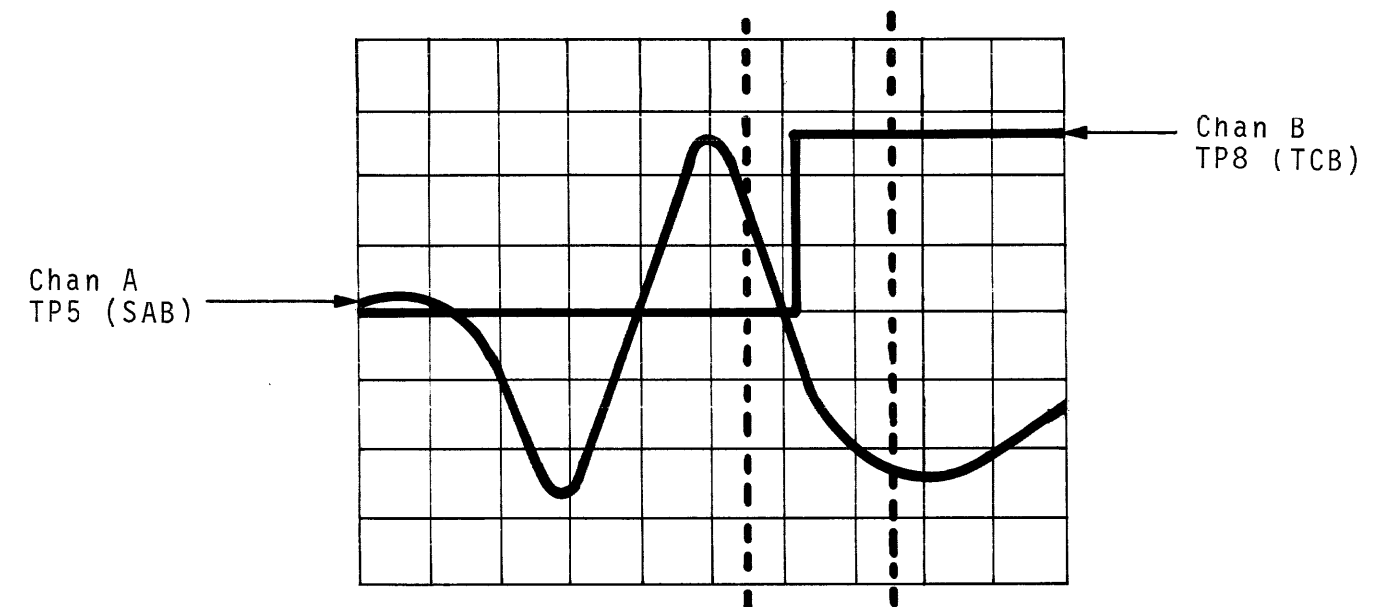


Figure 7-34. Zero Adjustment

Channel A:	TP5 (SAB)
	1V/cm
Channel B:	TP8 (TCB)
	2V/cm
Sweep:	0.5m/sec
Syn:	External positive E11 (I/O)
Operation:	Alternate seek between 0 and 3.
Adjust:	R2 (TCB) so that the positive transition of TP8 (TCB) is within the dotted lines.

e. Zero Adjustment ("D" model using a DTU-2)

1. Remove jumper wire E12-E13 (I/O) and add jumper wire E11-E12 (I/O).
2. Connect drive to a DTU-2 and go to step (d), entitled "Zero Adjustment" ("R" model only). After completion continue with Step 3.

3. Remove jumper E11-E12 (I/O) and add jumper E12-E13 (I/O).

f. Zero Adjustment ("D" model using computer).

1. Using a computer cause the drive to do alternate seeks between tracks 0 and 2.
2. Set up scope as per Figure 7-35.
3. Adjust R2 (TCB) so that the positive transistion of TP8 is within the dotted lines as shown in Figure 7-35.

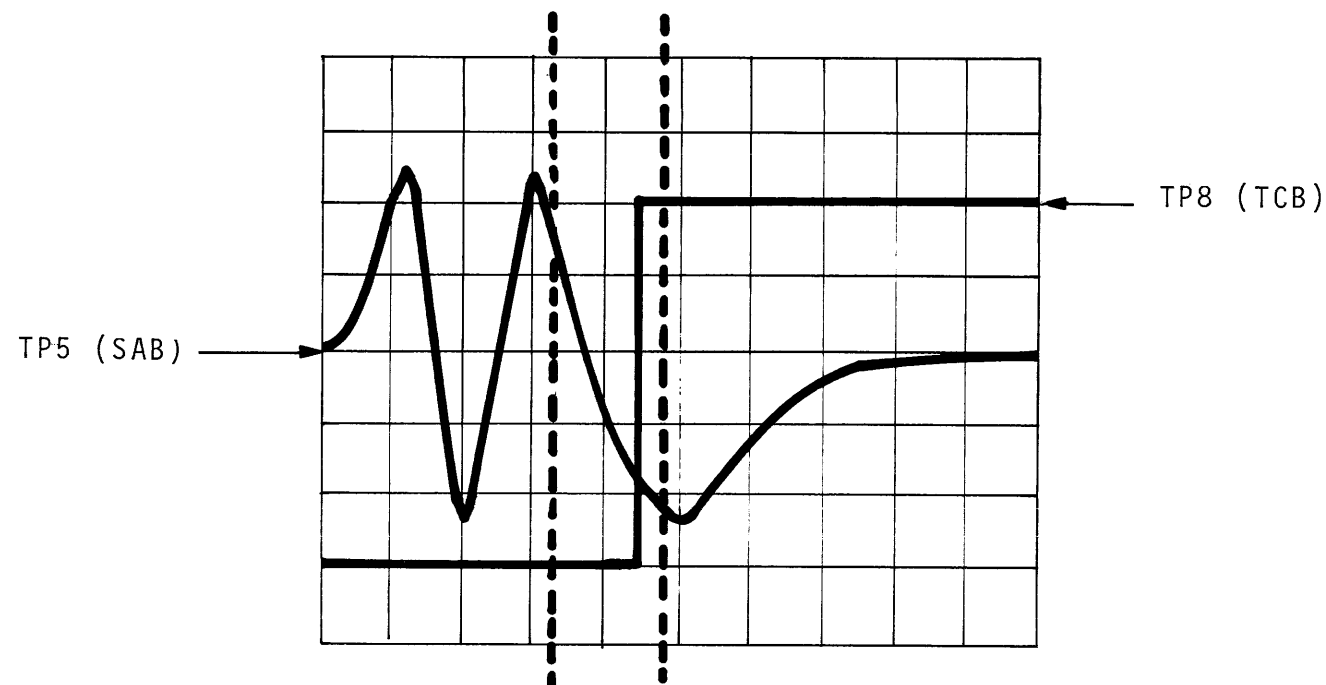


Figure 7-35. Zero Adjustment ("D" model using computer).

Channel A: TP5 (SAB)
1V/cm

Channel B: TP8 (TCB)
1V/cm

Syn: External positive IC 23 pin 13

Sweep Speed: 1 millisecond per centimeter

Operation: Alternate seek between track 0 and 2 using computer.

Adjust: R2 (TCB) so that the positive transistion of TP8 (TCB) is within the dotted lines.

NOTE

In Figure 7-35, the computer is telling the drive to seek between track 0 and 2. Actually the drive is seeking between 0 and 4.

7.5.28 Disk Cleaning Brushes - (306 models only)

NOTE

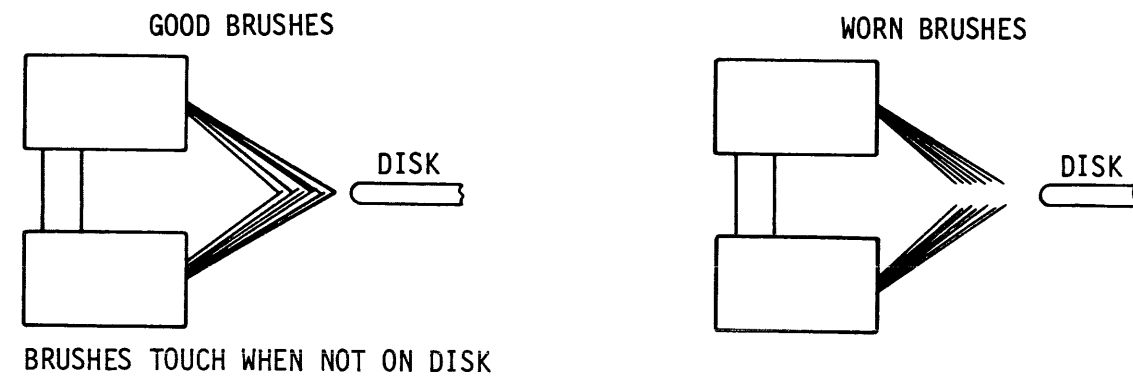
Check that brushes are not worn to the extent that they fail to be deflected as they pass over the disk. (Refer to Figure 7-36). If worn, brushes should be replaced.

a. Removal

1. Turn off drive Power switch and disconnect AC power cord.
2. Remove six shroud assembly mounting screws and remove shroud assembly.
3. Remove spring clip holding the brush arm to the brush shaft.
4. Slide the brush arm off the brush shaft.
5. Unclip worn brushes from the brush arm.

b. Replacement

1. Slide replacement brushes onto brush arm making sure that left- and right-hand brushes are in the proper position (bristles making contact per Figure 7-36).
2. Slide the brush arm onto the brush shaft.
3. Install spring clip holding the brush arm on the brush shaft.
4. Replace the shroud assembly and install six mounting screws.
5. Connect AC power cord and turn on drive Power switch.



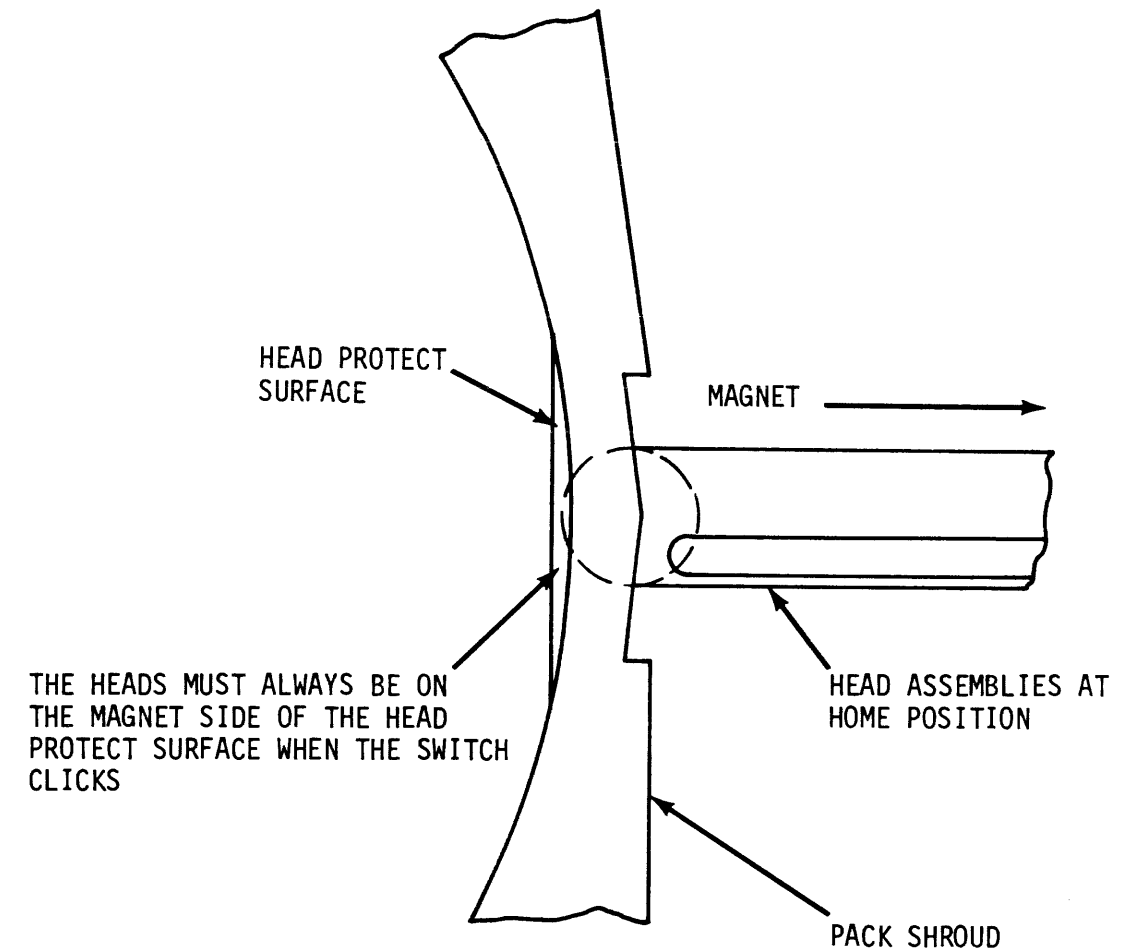
600-113

Figure 7-36. Disk Brush Condition

7.6 ADJUSTMENTS

7.6.1 Home Microswitch

- a. Remove covers. (Refer to subsections 7.5.1 and 7.5.2).
- b. Disconnect servo motor connector from the PCM.
- c. Turn on drive Power switch.
- d. Set the drive Start/Stop switch to Start position.
- e. When the spindle motor has reached up speed, manually move the carriage assembly to home position.
- f. Slowly move the carriage assembly toward the spindle until home microswitch clicks.
- g. Check read/write head locations to verify that they are on the magnet side of the head protect bracket. (See Figure 7-37).
- h. Loosen home microswitch mounting screws and adjust the switch position as necessary.
- i. Tighten home microswitch mounting screws.
- j. Set the drive Start/Stop switch to Stop position.
- k. Turn off drive Power switch.
- l. Connect servo motor connector to the PCM.
- m. Replace covers. (Refer to subsections 7.5.1 and 7.5.2).



600-114

Figure 7-37. Home Microswitch Adjustment

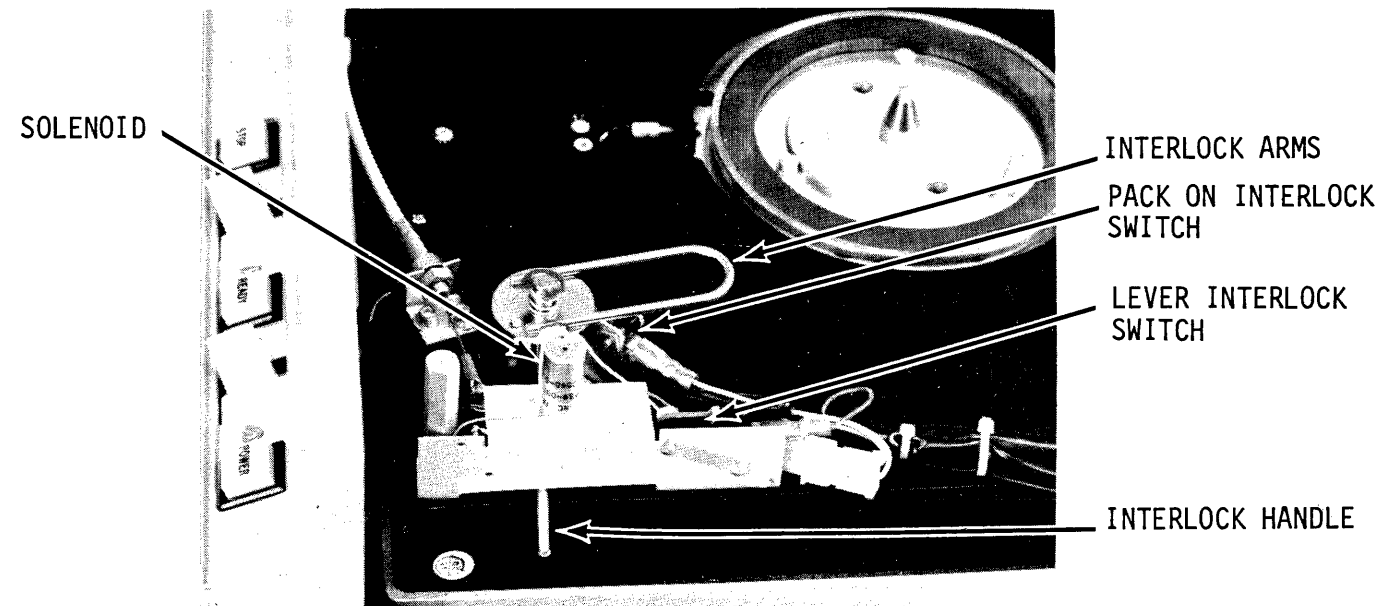


Figure 7-38. Pack Interlock Adjustment

600-15

7.6.2 Pack Interlock (306 models only)(See Figure 7-38).

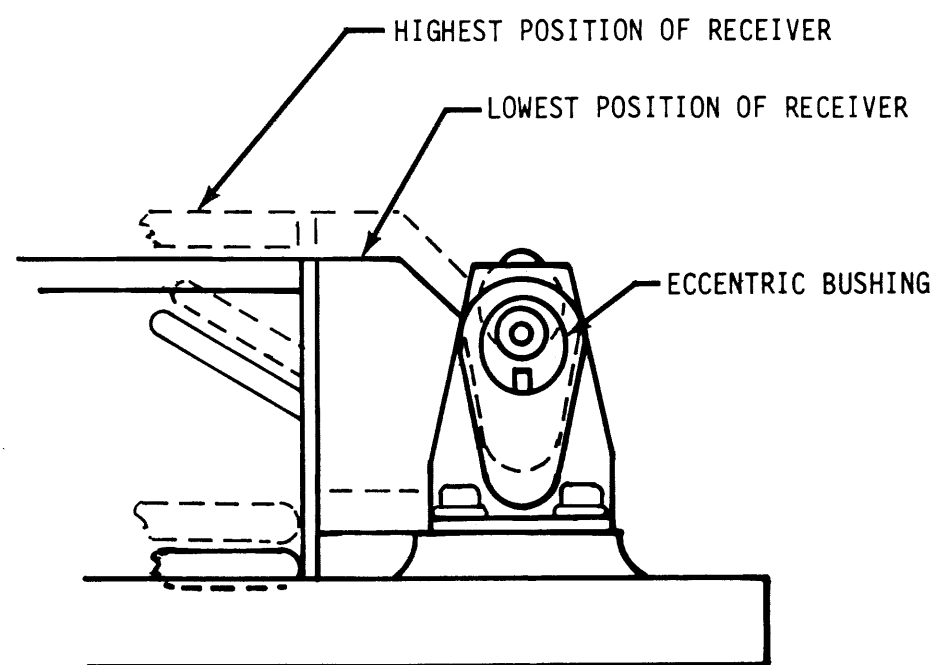
- a. Remove top cover. (Refer to subsection 7.5.1).
- b. Turn on drive Power switch and wait 45 seconds until solenoid energizes. This allows the interlock handle to be moved the full stroke.
- c. Install a disk cartridge.
- d. Move the interlock handle toward the rear of the drive until the pack on interlock switch closes (switch should close after the interlock arms are rotated over the disk cartridge).
- e. Adjust pack on interlock switch for condition required in step d and position the interlock handle toward the front of the drive.
- f. Move the interlock handle toward the rear of the drive until the lever interlock switch closes (switch should close after the interlock handle passes the solenoid).
- g. Now move the interlock handle toward the front of the drive until the lever interlock switch opens (switch should open after the interlock handle passes the solenoid).
- h. Adjust lever interlock switch for conditions required in steps f and g.
- i. Replace top cover. (Refer to subsection 7.5.1).

7.6.3 Alignment of Receiver (206 models only)

- a. Adjust eccentric bushings at rear of receiver with slot down. Refer to Figure 7-39 (Receiver in lowest position).
- b. Adjust receiver arms toward door as far as possible as shown in Figure 7-40. Tighten all adjustment points finger tight.
- c. Insert pack in receiver.
- d. Turn rear eccentric bushings to raise receiver until the receiver just clears the underside of the pack.
- e. Adjust eccentric bushings on receiver arms with slot up. Refer to Figure 7-40. (Receiver in lowest position). Continue adjustment of eccentric bushings until front door is flush with front face.
- f. Remove plug on end of ribbon cable attached to J4 on power board to deactivate carriage. Turn on power switch. Turn on start switch for an instant to start disk turning.
 1. If no rubbing of the disk on the pack occurs with momentary operation of the start switch, turn the start switch on to continuously spin the disk.
 2. Pull on the door as if to open until it comes against the stop. If the pack is not lifted by the receiver causing the disk to rub, no further adjustment is required. Secure button-head socket screws firmly in place.* Refer to Figure 7-40.
 3. If disk rubs in 1 or 2 above, make further adjustments as described below.
- g. Note location of rubbing (front or rear). Turn these eccentric bushings nearest to the end which is rubbing to lower receiver. Check for rubbing with start switch momentary operation. If no rubbing occurs, secure button-head socket screws firmly.*
- h. If rubbing continues, adjust the opposite set of eccentric bushings to those adjusted in Step g.
- i. Continue lowering receiver at front and rear eccentric bushings until rubbing disappears. Since the front bushings have the most effect on the door alignment, the principal attempts at relieving rubbing should be at the rear bushings.
- j. Turn power switch off and reconnect plug to J4.

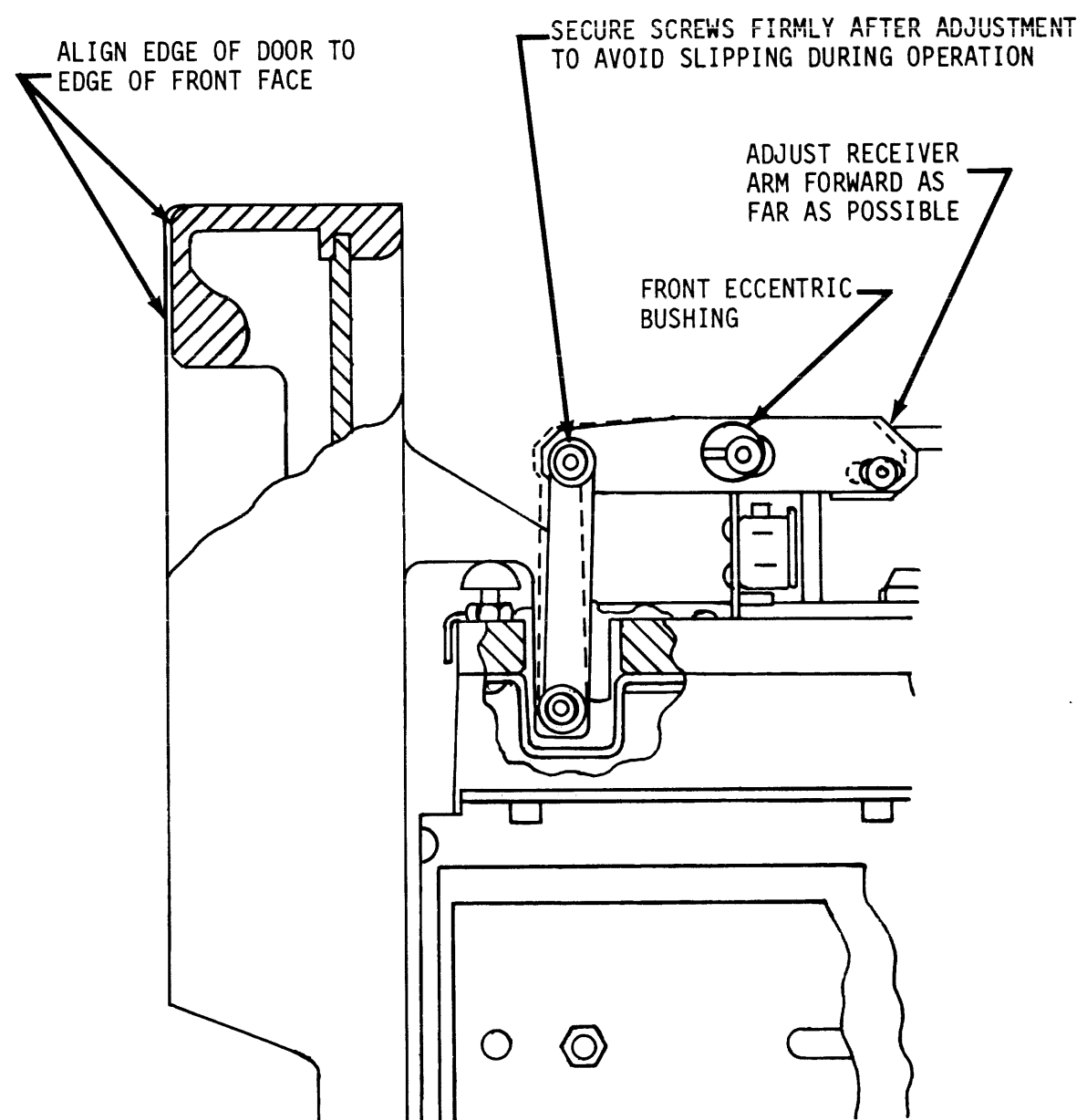
NOTE

It is very important that the screws securing the receiver arms both be tightened firmly to prevent slippage during operation.



400-80

Figure 7-39. Receiver in Lowest Position



400-81

Figure 7-40. Receiver

7.6.4 Head Load Cam Assembly

NOTE

The head load cam assembly can be adjusted with the read/write heads installed; however, the assembly can be replaced only if the read/write heads are removed.

- a. Loosen the two screws mounting the head load cam assembly to the baseplate. (See Figure 7-41).
- b. Push the head load cam assembly as far toward the positioner motor as possible and tighten the two mounting screws.

7.7 BRING-UP SEQUENCE OF ADJUSTMENTS

- a. In the event that a problem occurs in the drive that cannot be defined, you may wish to go through all the adjustments. The following would be the proper sequence.
 1. 7.5.4 Power Control Module (PCM)
 2. 7.5.17 Removable Disk Index/Sector Transducer
 3. 7.5.18 Fixed Disk Index/Sector Transducer
 4. 7.5.5.c I/O Board Checks (Index/Sector Pulses)
 5. 7.5.26 Detent Assembly
 6. 7.5.27 Detent Alignment
 7. 7.5.9/11/13 Servo Logic Board (SLB)
 8. 7.5.10/12/14 Servo Analog Board (SAB)
 9. 7.5.3 Read Write Amplifier Board (R/WA)
 10. 7.5.8 Data Translator Board (DTB)
 11. 7.5.16 Read/Write Heads
 12. 7.5.5 Input/Output Board (I/O)
 13. Run a comprehensive computer test.



600-116

Figure 7-41. Head Load Cam Assembly Adjustment

SECTION 8

DRAWINGS

This section contains drawings pertaining to the Model 206R/306R Disk Drive. A list of the specific drawings and page numbers is shown below.

<u>Drawing</u>	<u>Page</u>
206 Disk Drive Assembly, Sheet 1 of 5	8-2
206 Disk Drive Assembly, Sheet 2 of 5	8-3
206 Disk Drive Assembly, Sheet 3 of 5	8-4
206 Disk Drive Assembly, Sheet 4 of 5	8-5
206 Disk Drive Assembly, Sheet 5 of 5	8-6
306 Disk Drive Assembly, Sheet 1 of 5	8-7
306 Disk Drive Assembly, Sheet 2 of 5	8-8
306 Disk Drive Assembly, Sheet 3 of 5	8-9
306 Disk Drive Assembly, Sheet 4 of 5	8-10
306 Disk Drive Assembly, Sheet 5 of 5	8-11
206 Front Face Assembly	8-12
206 Shield Assembly	8-13
Switch Plate Assembly	8-14
Carriage Assembly	8-15
206 Spindle Assembly	8-16
306 Front Face Assembly	8-17
306 Shield Assembly	8-18
306 Shroud Assembly	8-19
306 Brush Motor Assembly	8-20
306 Spindle Assembly	8-21
Slide Kit	8-22
Mother Board Assembly	8-23
Power Control Module Assembly	8-24
Servo Logic Board Assembly	8-25
Servo Analog Board Assembly	8-26
Temperature Compensation Board	8-27
Paddle Board Assembly	8-28
Input/Output Board Assembly	8-29

<u>Drawing</u>	<u>Page</u>
200 TPI Read/Write Amplifier Assembly, Sheet 1 of 2	8-30
200 TPI Read/Write Amplifier Assembly, Sheet 2 of 2	8-31
Control Sector Board Assembly	8-32
Control Sector Board (48) Assembly	8-33
Data Translator Board	8-34
Drive Control Board Assembly	8-35
Termination Board Schematic	8-36
Termination Board Assembly	8-37
100 TPI, 1,500 rpm Read/Write Amplifier Assembly, Sheet 1 of 2	8-38
100 TPI, 1,500 rpm Read/Write Amplifier Assembly, Sheet 2 of 2	8-39
100 TPI, 2,400 rpm Read/Write Amplifier Assembly, Sheet 1 of 2	8-40
100 TPI, 2,400 rpm Read/Write Amplifier Assembly, Sheet 2 of 2	8-41

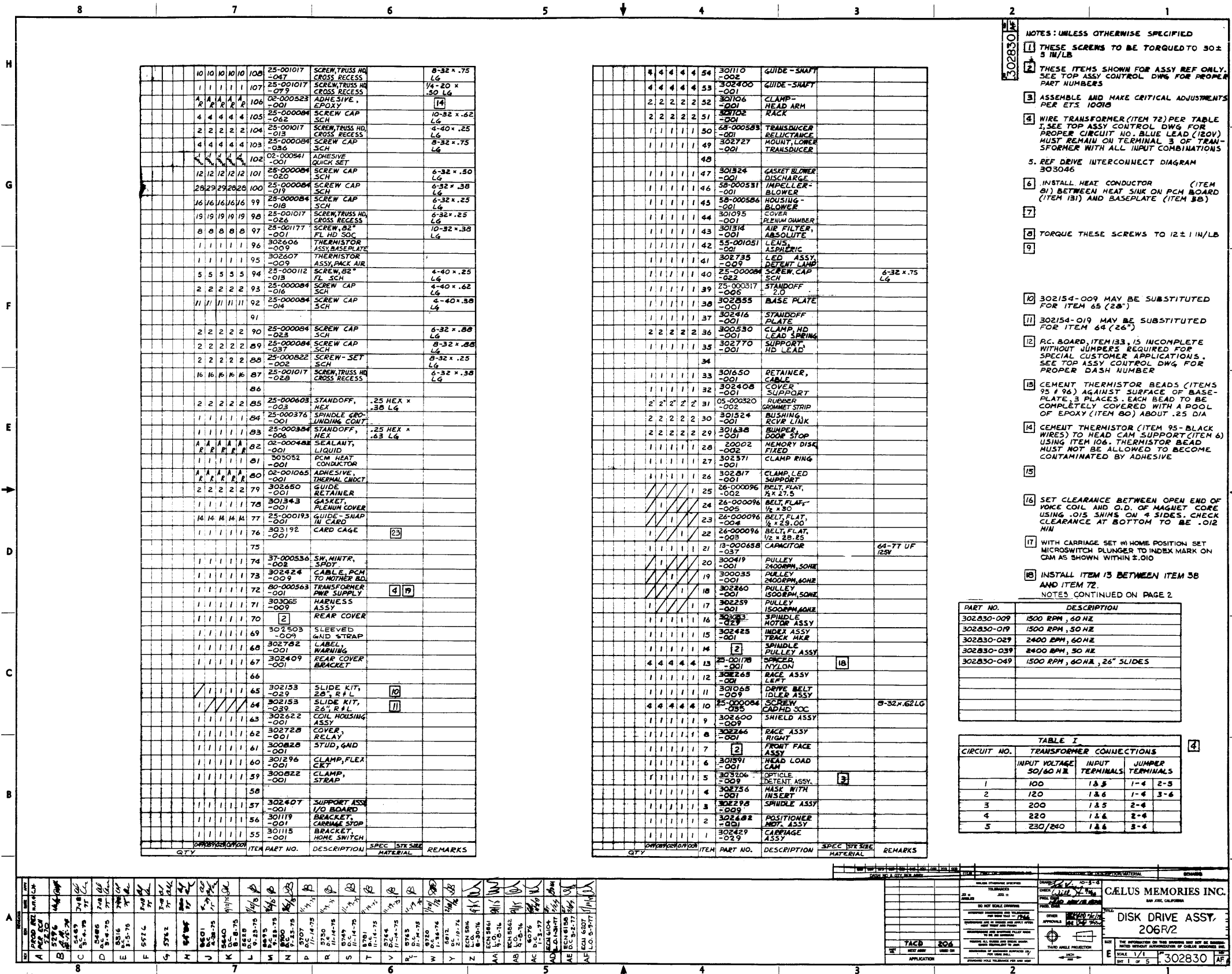
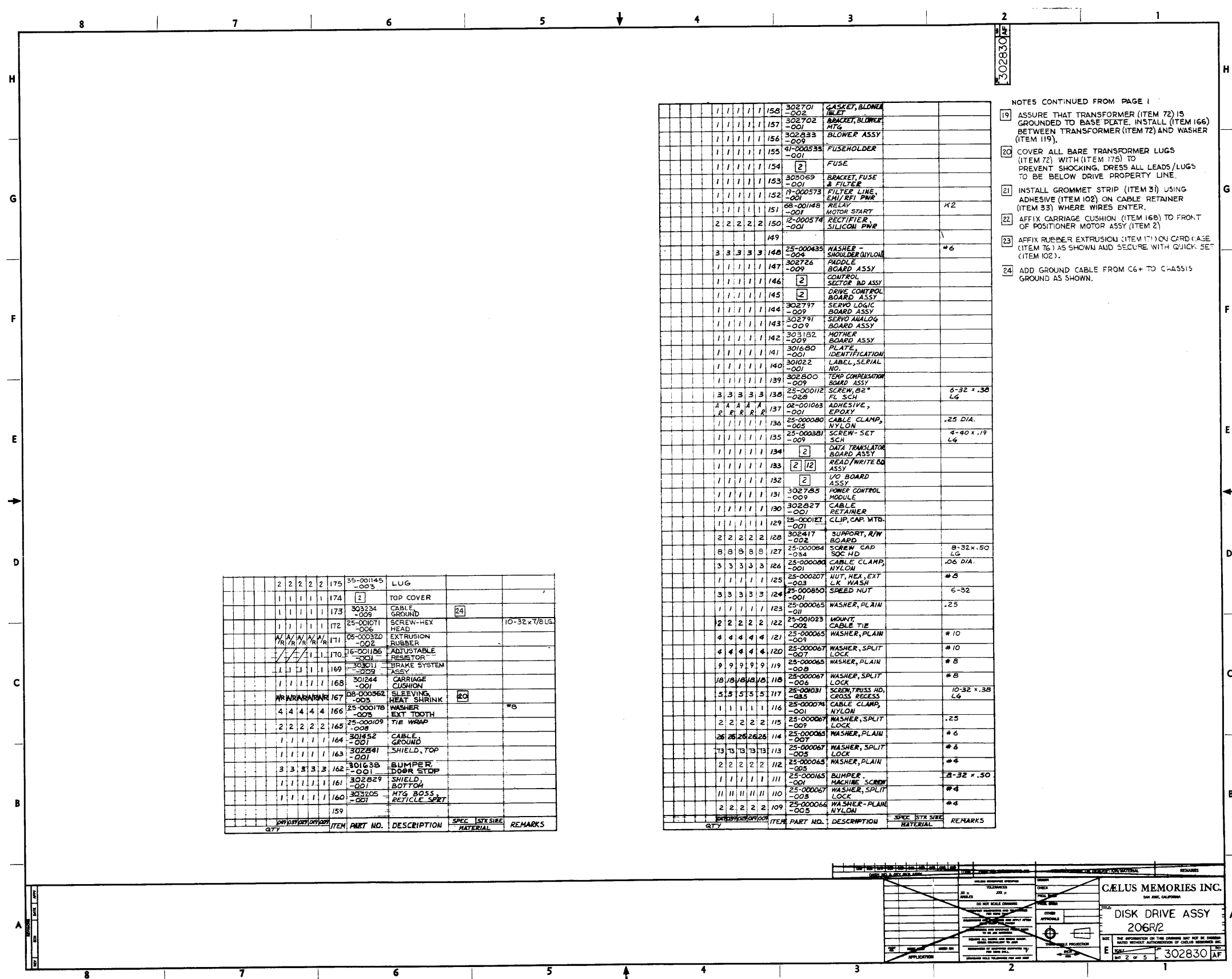


Figure 8-1. 206 Disk Drive Assembly, Sheet 1 of 5



QTY	ITEM	PART NO.	DESCRIPTION	SPEC	STR	SIZES	MATERIAL	REMARKS
2 2 2 2 2	175	35-001145-003	LUG					
1 1 1 1 1	174	[2]	TOP COVER					
1 1 1 1 1	173	303234-009	CABLE GROUND					[24]
1 1 1 1 1	172	25-001071-006	SCREW-HEX HEAD					10-32 x 7/8 LG.
A/A/A/A/A/A/A/A/A/A	171	05-000320-002	EXTRUSION RUBBER					
1 1 1 1 1	170	16-001185-001	ADJUSTABLE RESISTOR					
1 1 1 1 1	169	303011-009	BRAKE SYSTEM ASSY					
1 1 1 1 1	168	301244-001	CARRIAGE CUSHION					
W/W/W/W/W/W/W/W/W/W	167	08-000362-003	SLEEVING HEAT SHRINK					[20]
4 4 4 4 4	166	25-000178-005	WASHER EXT TOOTH					#8
2 2 2 2 2	165	25-000109-008	TIE WRAP					
1 1 1 1 1	164	301452-001	CABLE GROUND					
1 1 1 1 1	163	302241-001	SHIELD, TOP					
3 3 3 3 3	162	301638-001	BUMPER, DOOR STOP					
1 1 1 1 1	161	302229-001	SHIELD, BOTTOM					
1 1 1 1 1	160	303205-001	MTG BOSS, RETICLE SPRT					
	159							

QTY	ITEM	PART NO.	DESCRIPTION	SPEC	STR	SIZES	MATERIAL	REMARKS
1 1 1 1 1	158	302701-002	GASKET, BLOWER					
1 1 1 1 1	157	302702-001	BRACKET, BLOWER					
1 1 1 1 1	156	302233-009	BLOWER ASSY					
1 1 1 1 1	155	41-000533-001	FUSEHOLDER					
1 1 1 1 1	154	[2]	FUSE					
1 1 1 1 1	153	305069-001	BRACKET, FUSE & FILTER					
1 1 1 1 1	152	19-000573-001	FILTER LINE EMI/RFI PWR					
1 1 1 1 1	151	68-001148-001	RELAY MOTOR START					K2
2 2 2 2 2	150	12-000574-001	RECTIFIER SILICON PWR					
	149							
3 3 3 3 3	148	25-000435-004	WASHER - SHOULDER (NYLON)					#6
1 1 1 1 1	147	302726-009	PADDLE BOARD ASSY					
1 1 1 1 1	146	[2]	CONTROL SECTOR Bd ASSY					
1 1 1 1 1	145	[2]	DRIVE CONTROL BOARD ASSY					
1 1 1 1 1	144	302797-009	SERVO LOGIC BOARD ASSY					
1 1 1 1 1	143	302791-009	SERVO ANALOG BOARD ASSY					
1 1 1 1 1	142	303182-009	MOTHER BOARD ASSY					
1 1 1 1 1	141	301650-001	PLATE, IDENTIFICATION					
1 1 1 1 1	140	301022-001	LABEL, SERIAL NO.					
1 1 1 1 1	139	302800-009	TEMP COMPENSATION BOARD ASSY					
3 3 3 3 3	138	25-000112-028	SCREW, B2* FL SCH					6-32 x .38 LG
A A A A A	137	02-001063-001	ADHESIVE, EPOXY					
R R R R R	136	25-000080-065	CABLE CLAMP, NYLON					.25 DIA.
1 1 1 1 1	135	25-000381-009	SCREW-SET SCW					4-40 x .19 LG
1 1 1 1 1	134	[2]	DATA TRANSLATOR BOARD ASSY					
1 1 1 1 1	133	[2] [2]	READ/WRITE Bd ASSY					
1 1 1 1 1	132	[2]	I/O BOARD ASSY					
1 1 1 1 1	131	302785-001	POWER CONTROL MODULE					
1 1 1 1 1	130	302827-001	CABLE RETAINER					
1 1 1 1 1	129	25-000121-001	CLIP, CAP. MTS.					
2 2 2 2 2	128	302417-002	SUPPORT, R/W BOARD					
8 8 8 8 8	127	25-000084-014	SCREW CAP SOC HD					8-32 x .50 LG
3 3 3 3 3	126	25-000080-001	CABLE CLAMP, NYLON					.06 DIA.
1 1 1 1 1	125	25-000207-003	NUT, HD, EXT LK WASH					#8
3 3 3 3 3	124	25-000850-001	SPEED NUT					6-32
1 1 1 1 1	123	25-000065-001	WASHER, PLAIN					.25
2 2 2 2 2	122	25-001023-002	MOUNT CABLE TIE					
4 4 4 4 4	121	25-000065-009	WASHER, PLAIN					#10
4 4 4 4 4	120	25-000067-007	WASHER, SPLIT LOCK					#10
9 9 9 9 9	119	25-000065-008	WASHER, PLAIN					#8
18 18 18 18 18	118	25-000067-006	WASHER, SPLIT LOCK					#8
5 5 5 5 5	117	25-000031-035	SCREW TRUSS HD, CROSS RECESS					10-32 x .38 LG
1 1 1 1 1	116	25-000074-001	CABLE CLAMP, NYLON					
2 2 2 2 2	115	25-000067-009	WASHER, SPLIT LOCK					.25
26 26 26 26 26	114	25-000065-007	WASHER, PLAIN					#6
13 13 13 13 13	113	25-000067-005	WASHER, SPLIT LOCK					#6
2 2 2 2 2	112	25-000065-005	WASHER, PLAIN					#4
1 1 1 1 1	111	25-000165-001	BUMPER, MACHINE SCREEN					8-32 x .50
1 1 1 1 1	110	25-000067-008	WASHER, SPLIT LOCK					#4
2 2 2 2 2	109	25-000066-005	WASHER-PLAIN NYLON					#4

- NOTES CONTINUED FROM PAGE 1
- ASSURE THAT TRANSFORMER (ITEM 72) IS GROUNDED TO BASE PLATE. INSTALL (ITEM 166) BETWEEN TRANSFORMER (ITEM 72) AND WASHER (ITEM 119).
 - COVER ALL BARE TRANSFORMER LUGS (ITEM 72) WITH (ITEM 175) TO PREVENT SHOCKING. DRESS ALL LEADS/LUGS TO BE BELOW DRIVE PROPERTY LINE.
 - INSTALL GROMMET STRIP (ITEM 31) USING ADHESIVE (ITEM 102) ON CABLE RETAINER (ITEM 33) WHERE WIRES ENTER.
 - AFFIX CARRIAGE CUSHION (ITEM 168) TO FRONT OF POSITIONER MOTOR ASSY (ITEM 2).
 - AFFIX RUBBER EXTRUSION (ITEM 171) ON CARD CASE (ITEM 76) AS SHOWN AND SECURE WITH QUICK SET (ITEM 102).
 - ADD GROUND CABLE FROM C6+ TO CHASSIS GROUND AS SHOWN.

TITLE: DISK DRIVE ASSY 206R2		DATE: 10/1/72 DRAWN BY: JOK CHECKED BY: JOK APPROVED BY: JOK	C&LUS MEMORIES INC. SAN DIEGO, CALIFORNIA
PART NO.: 302830		SHEET 2 OF 5	

Figure 8-2. 206 Disk Drive Assembly, Sheet 2 of 5

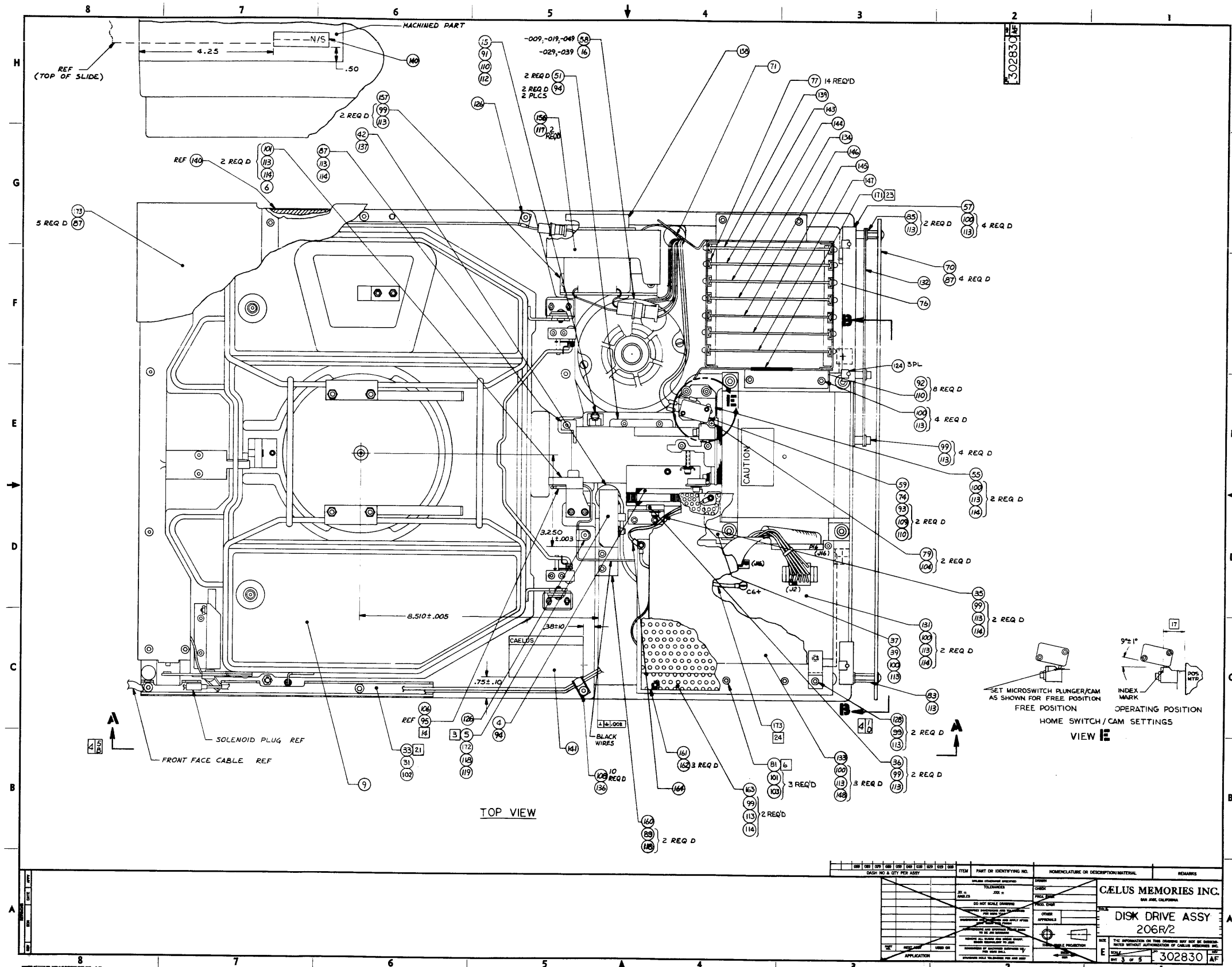


Figure 8-3. 206 Disk Drive Assembly, Sheet 3 of 5

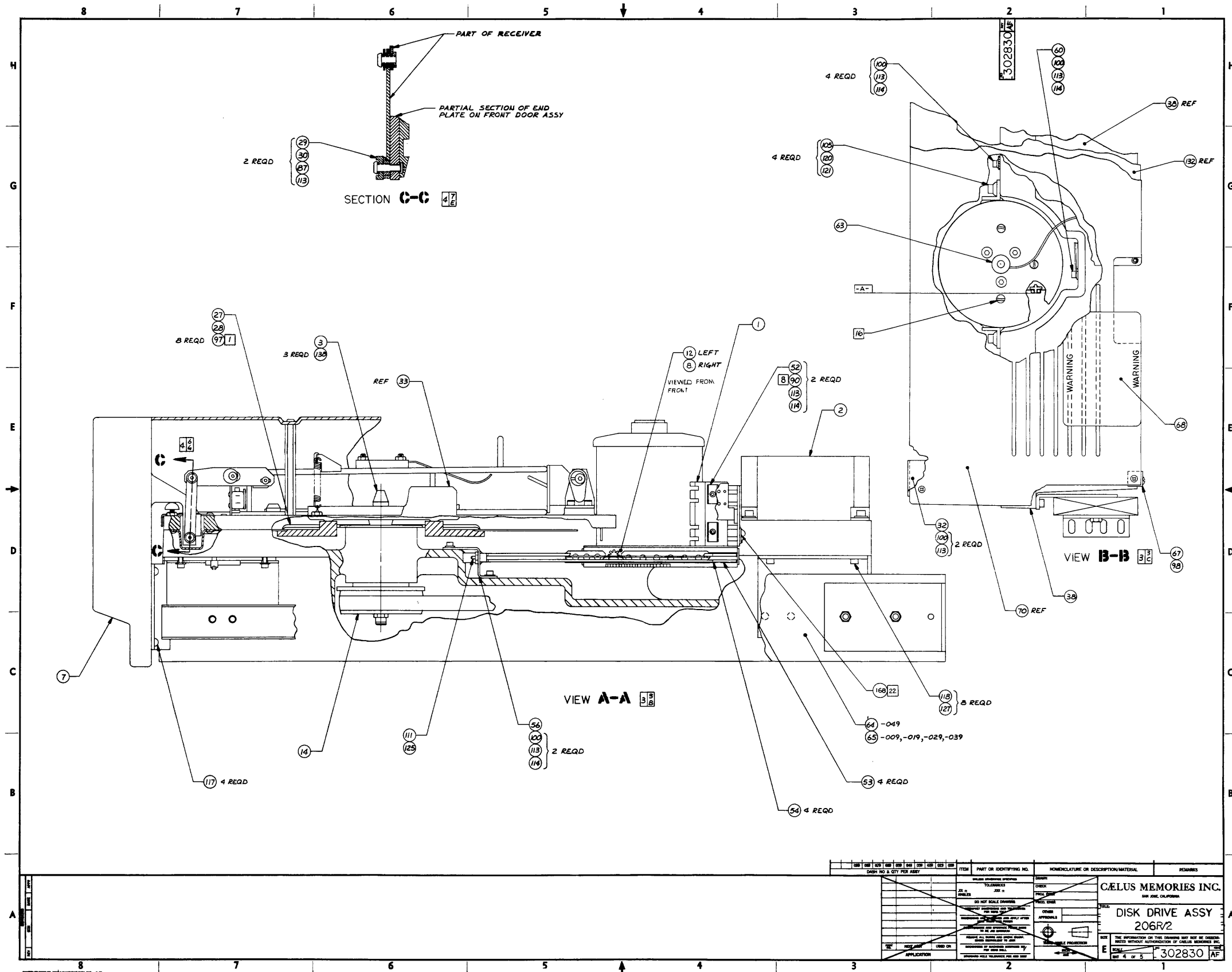


Figure 8-4. 206 Disk Drive Assembly, Sheet 4 of 5

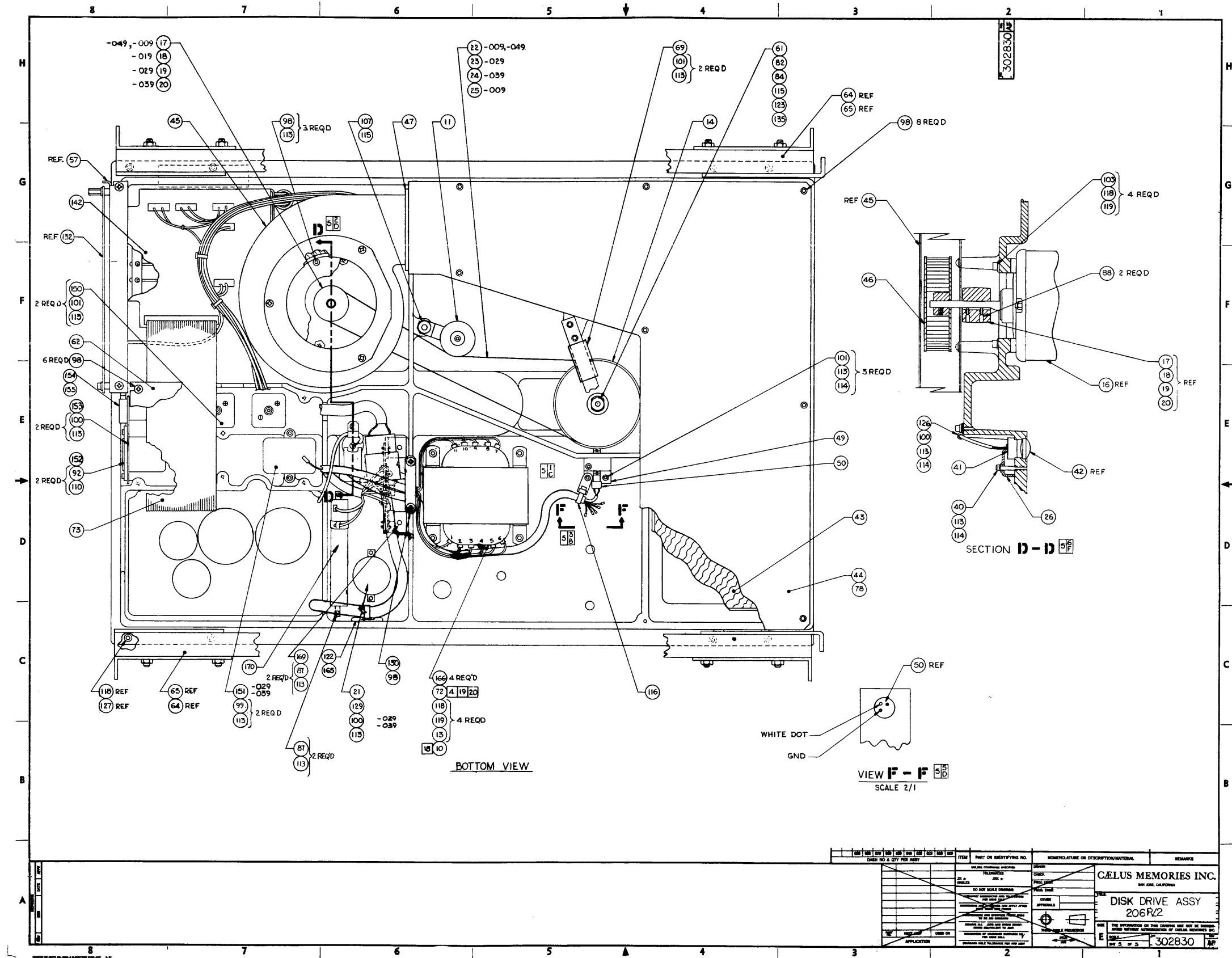


Figure 8-5. 206 Disk Drive Assembly, Sheet 5 of 5

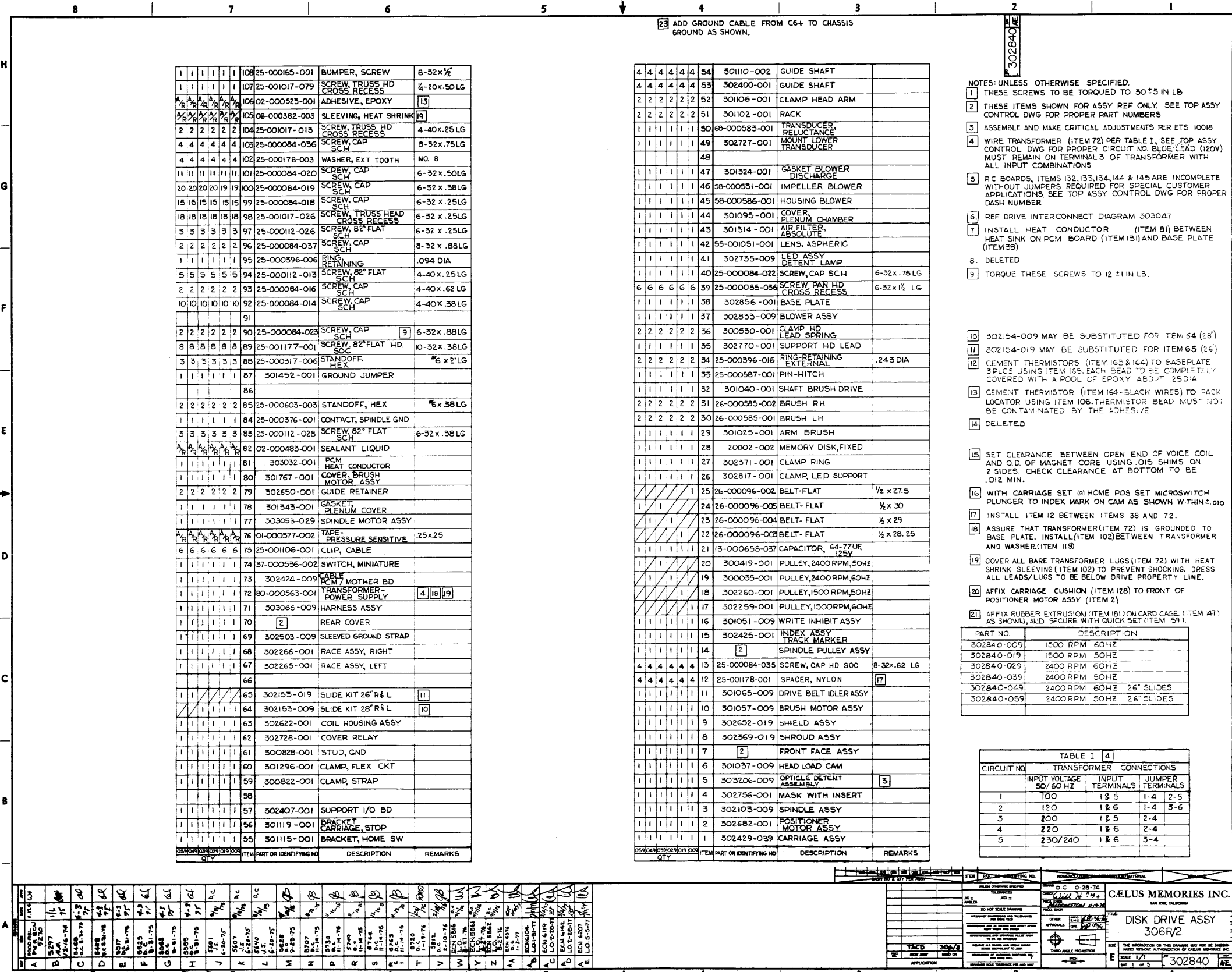
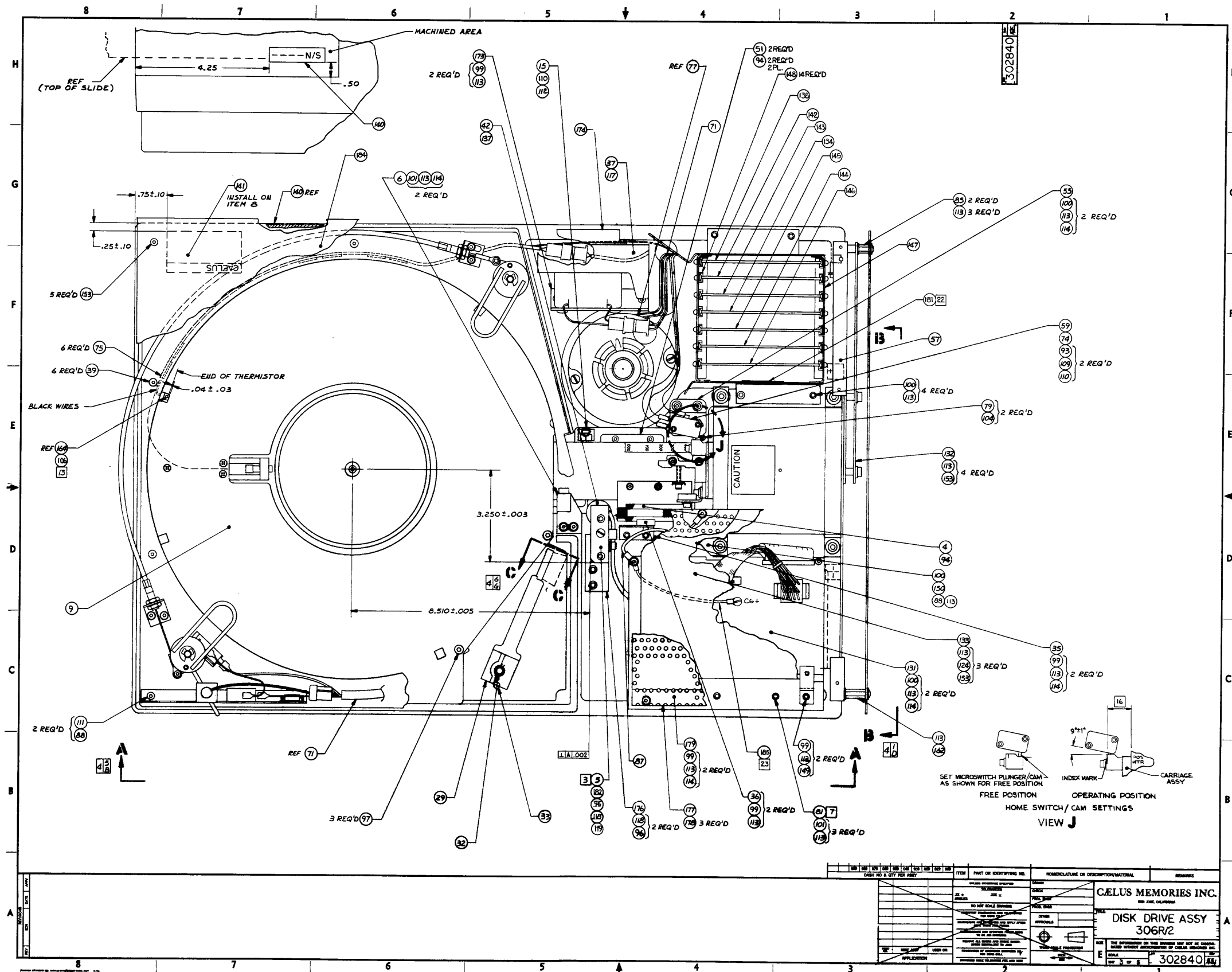


Figure 8-6. 306 Disk Drive Assembly, Sheet 1 of 5

QTY	ITEM	PART OR IDENTIFYING NO	DESCRIPTION	REMARKS
1	185	25-000127-001	CLAMP CAP	
1	184	2	TOP COVER	
1	183	303234-009	CABLE, GND	23
1	182	25-001071-006	SCREW-HEX HEAD	10-32x7/8 LG.
1	181	05-000320-002	EXTRUSION RUBBER	
3	180	25-000850-001	SPEED NUT	6-32
1	179	302841-001	SHIELD, TOP	
3	178	301638-001	BUMPER, DOOR STOP	
1	177	302829-001	SHIELD, BOTTOM	
1	176	303205-001	MOUNTING BOSS RETICLE SPRT	
1	175			
1	174	302701-002	GASKET- BLOWER	INLET
1	173	302702-001	BRACKET, BLOWER MTG	
1	172	503069-001	BRACKET, FILTER	
1	171	19-000573-001	FILTER LINE, EMV RFI PWR	
2	170	12-000574-001	RECTIFIER, SILICON PWR	
1	169	68-001148-001	RELAY MOTOR START	K2
2	168	25-000109-008	TIE WRAP	
1	167	75-000152-001	RELAY BRUSH MOTOR	K1
1	166	2	FUSE	
1	165	02-001065-001	ADHESIVE, THERMAL CNDCCT	
1	164	302653-009	THERMISTOR ASSY PACK AIR	
1	163	302606-009	THERMISTOR ASSY BASE PLATE	
1	162	25-000384-006	STAND-OFF, HEX	5/8 x .62 LG
1	161	302409-001	REAR COVER BRACKET	
1	160	302408-001	COVER, SUPPORT	
1	159	02-000541-001	ADHESIVE, QUICK SET	
QTY	ITEM	PART OR IDENTIFYING NO	DESCRIPTION	REMARKS
15	158	45-000208-001	GROMMET STRIP	
4	157	25-000084-061	SCREW CAP SCH	10-32 x .50 LG
1	156	16-001186-001	ADJUSTABLE RESISTOR	
1	155	41-000533-001	FUSE HOLDER	
2	154	25-000822-002	SCREW SET, SCH	5-32 x .25 LG
24	153	25-001017-028	SCREW TRUSS HD, CROSS RECESS	6-32 x .38 LG
1	152	302782-001	LABEL, WARNING	
1	151	303011-009	BRAKE SYSTEM ASSY	
1	150	302416-001	STANDOFF PLATE	
2	149	302417-002	R/W SUPPORT BOARD	
14	148	25-000193-001	GUIDE - SNAP IN CARD	
1	147	303192-001	CARD CAGE	21
1	146	302726-009	PADDLE BOARD ASSY	
1	145	2 5	CONTROL SECTOR BD ASSY	
1	144	2 5	DRIVE CONTROL BD ASSY	
1	143	302797-009	SERVO LOGIC BD ASSY	
1	142	302791-009	SERVO ANALOG BD ASSY	
1	141	301680-001	PLATE IDENTIFICATION	
1	140	301022-001	LABEL SERIAL NO.	
1	139	303182-009	MOTHER BD ASSY	
1	138	302800-009	TEMP COMPENSATION BOARD ASSY	
1	137	02-001063-001	ADHESIVE, EPOXY	
2	136	25-000074-001	CLAMP, CABLE NYLON	
1	135	25-000381-009	SCREW-SET SCH	4-40 x 3/8 LG
1	134	2 5	DATA TRANSLATOR BD	
1	133	2 5	READ WRITE BD ASSY	
1	132	2 5	INPUT OUTPUT BD ASSY	
1	131	302785-009	POWER CONTROL MOD	
1	130	302827-001	CABLE RETAINER	
1	129	25-000127-001	CLIP, CAP, MOUNTING	
1	128	301244-001	CARRIAGE CUSHION	
8	127	25-000084-034	SCREW CAP SOC HD	8-32 x .50
1	126	25-000080-001	CLAMP, CABLE NYLON	.06 DIA
1	125	25-000207-003	NUT, HEX EXT LK WASH	#8
3	124	25-000435-004	WASHER, SHOULDER	#6
1	123	25-000065-011	WASHER, PLAIN	1/4
2	122	25-001023-002	MOUNT, CABLE TIE	
4	121	25-000065-009	WASHER, PLAIN	#10
4	120	25-000067-007	WASHER, SPLIT LOCK	#10
5	119	25-000065-008	WASHER, PLAIN	#8
15	118	25-000067-006	WASHER, SPLIT LOCK	#8
4	117	25-001031-035	SCREW TRUSS HD, CROSS RECESS	10-32 x .38 LG
2	116	25-000066-007	WASHER, PLAIN NYLON	#6
2	115	25-000067-009	WASHER, SPLIT LOCK	1/4
22	114	25-000065-007	WASHER, PLAIN	#6
10	113	25-000067-005	WASHER, SPLIT LOCK	#6
1	112	25-000065-005	WASHER, PLAIN	#4
2	111	25-000982-001	STUD, DOUBLE END	6-32 x 2.25 LG
13	110	25-000067-003	WASHER, SPLIT LOCK	#4
2	109	25-000066-005	WASHER, PLAIN NYLON	#4

Figure 8-7. 306 Disk Drive Assembly, Sheet 2 of 5



REV	DATE	BY	CHKD	APP	DESCRIPTION
1					
2					
3					
4					
5					
6					
7					
8					

ITEM	PART OR IDENTIFYING NO.	QUANTITY	DESCRIPTION
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
51			
52			
53			
54			
55			
56			
57			
58			
59			
60			
61			
62			
63			
64			
65			
66			
67			
68			
69			
70			
71			
72			
73			
74			
75			
76			
77			
78			
79			
80			
81			
82			
83			
84			
85			
86			
87			
88			
89			
90			
91			
92			
93			
94			
95			
96			
97			
98			
99			
100			
101			
102			
103			
104			
105			
106			
107			
108			
109			
110			
111			
112			
113			
114			
115			
116			
117			
118			
119			
120			
121			
122			
123			
124			
125			
126			
127			
128			
129			
130			
131			
132			
133			
134			
135			
136			
137			
138			
139			
140			
141			
142			
143			
144			
145			
146			
147			
148			
149			
150			
151			
152			
153			
154			
155			
156			
157			
158			
159			
160			
161			
162			
163			
164			
165			
166			
167			
168			
169			
170			
171			
172			
173			
174			
175			
176			
177			
178			
179			
180			
181			
182			
183			
184			
185			
186			
187			
188			
189			
190			
191			
192			
193			
194			
195			
196			
197			
198			
199			
200			

Figure 8-8. 306 Disk Drive Assembly, Sheet 3 of 5

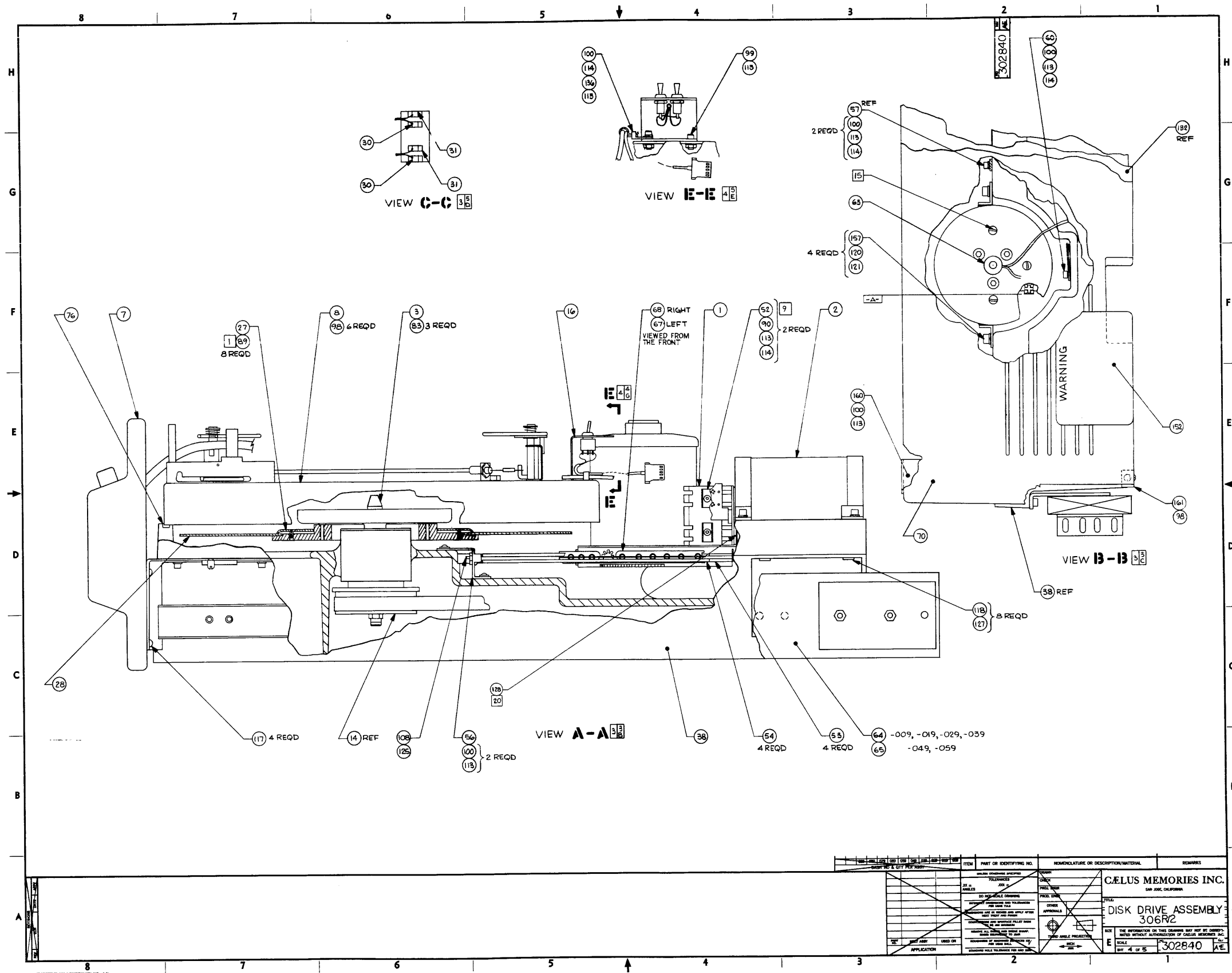


Figure 8-9. 306 Disk Drive Assembly, Sheet 4 of 5

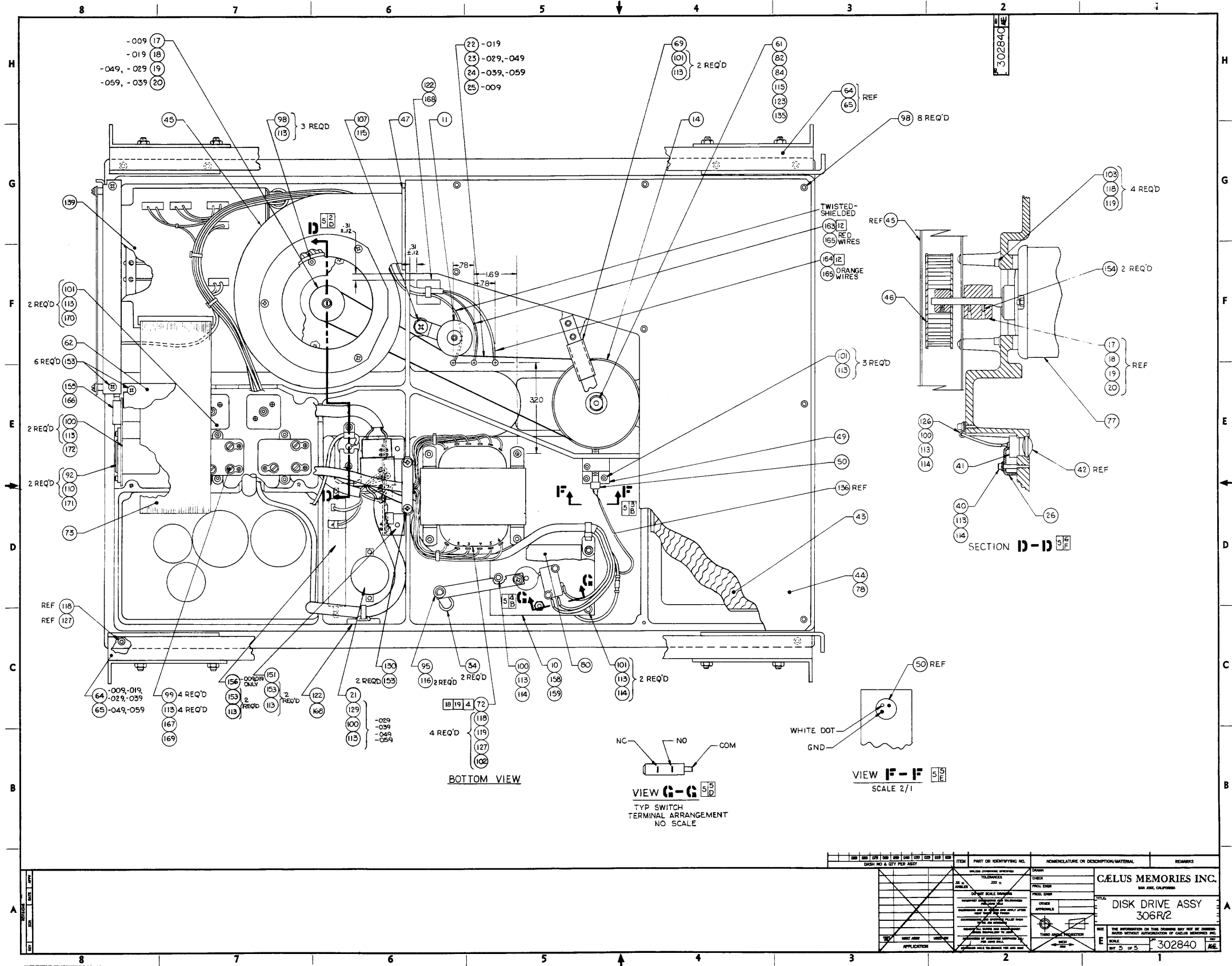


Figure 8-10. 306 Disk Drive Assembly, Sheet 5 of 5

ITEM	PART OR IDENTIFYING NO.	QUANTITY	REVISIONS	REMARKS

TOLERANCES UNLESS OTHERWISE SPECIFIED: FRACTIONS .0005" DECIMALS .0005" DIMENSIONS TO CENTER UNLESS OTHERWISE SPECIFIED DIMENSIONS TO SURFACE UNLESS OTHERWISE SPECIFIED DIMENSIONS TO EDGE UNLESS OTHERWISE SPECIFIED DIMENSIONS TO CENTER UNLESS OTHERWISE SPECIFIED DIMENSIONS TO SURFACE UNLESS OTHERWISE SPECIFIED DIMENSIONS TO EDGE UNLESS OTHERWISE SPECIFIED	CHECKED DRAWN DESIGNED APPROVED DATE	C.ELUS MEMORIES INC. SAN JOSE, CALIFORNIA DISK DRIVE ASSY 306R/2 SHEET 5 OF 5 302840
--	--	---

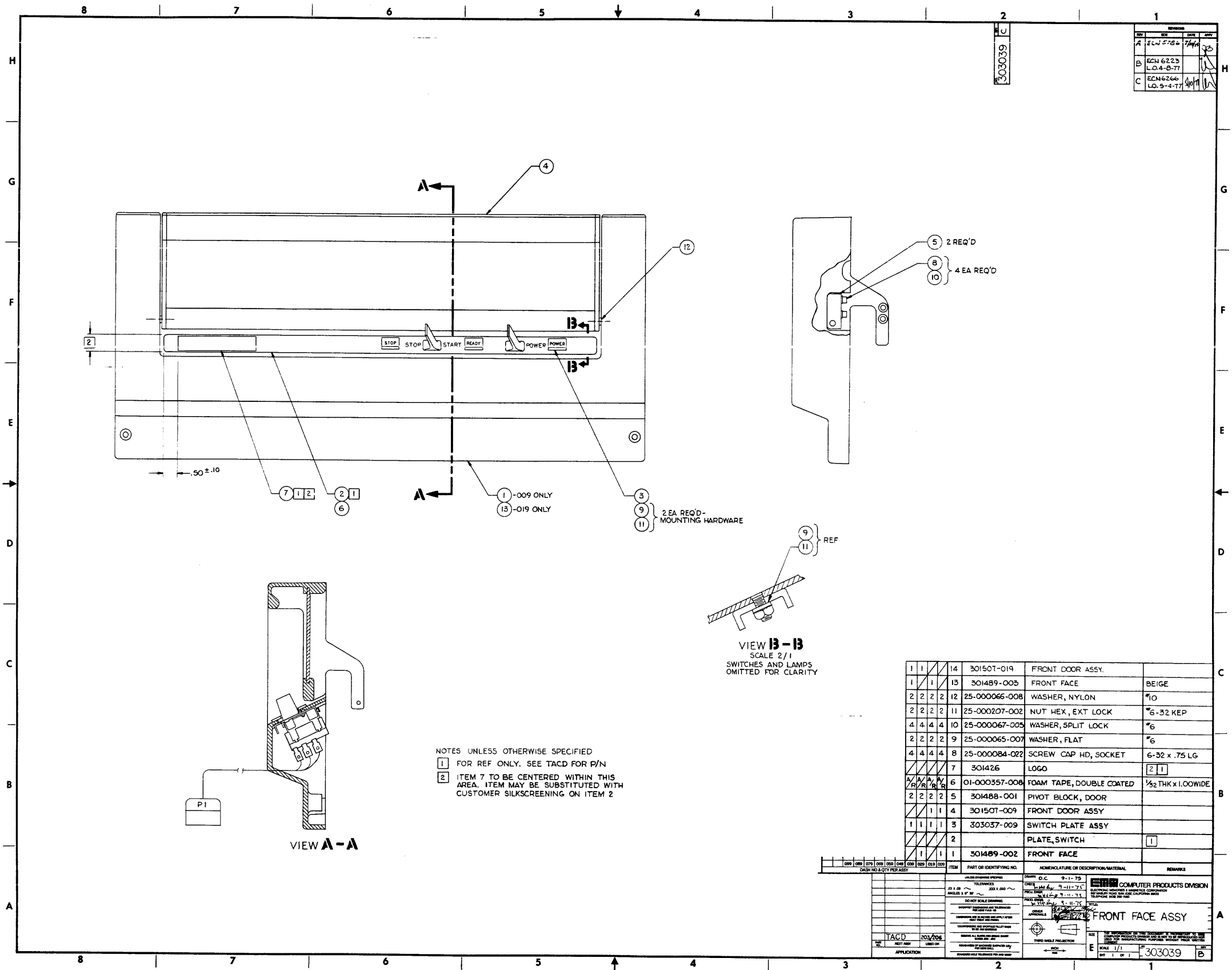


Figure 8-11. 206 Front Face Assembly

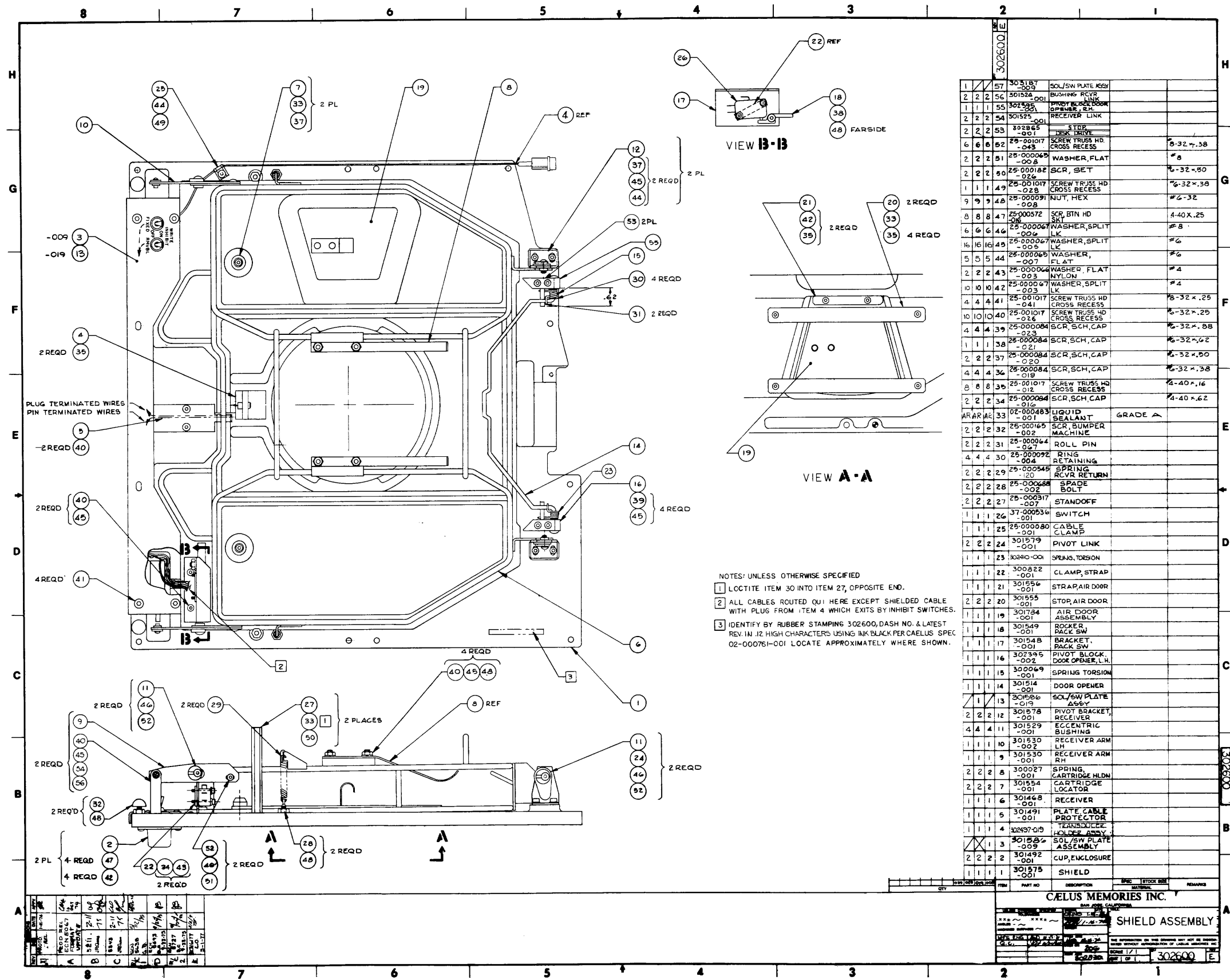


Figure 8-12. 206 Shield Assembly

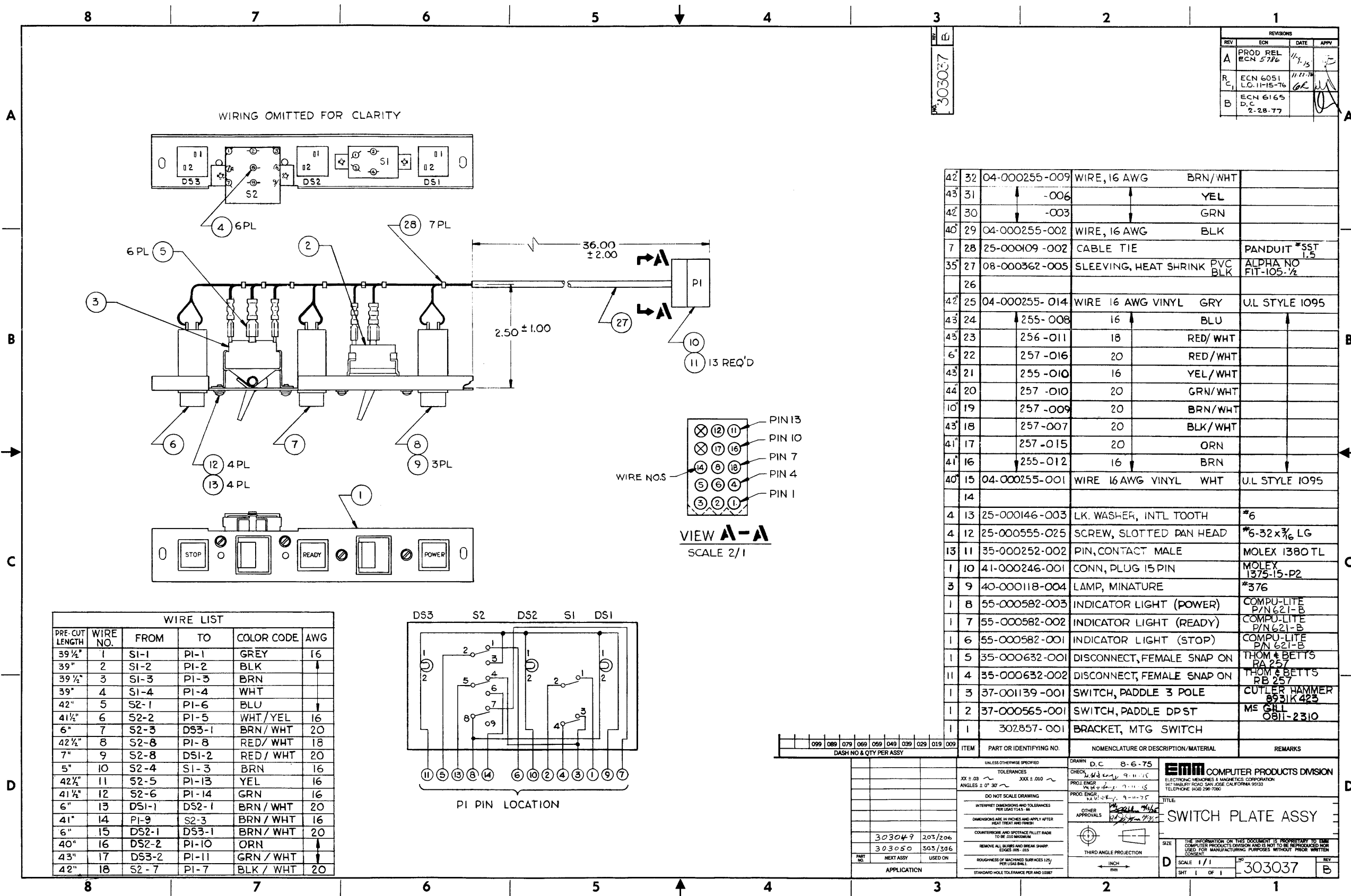


Figure 8-13. Switch Plate Assembly

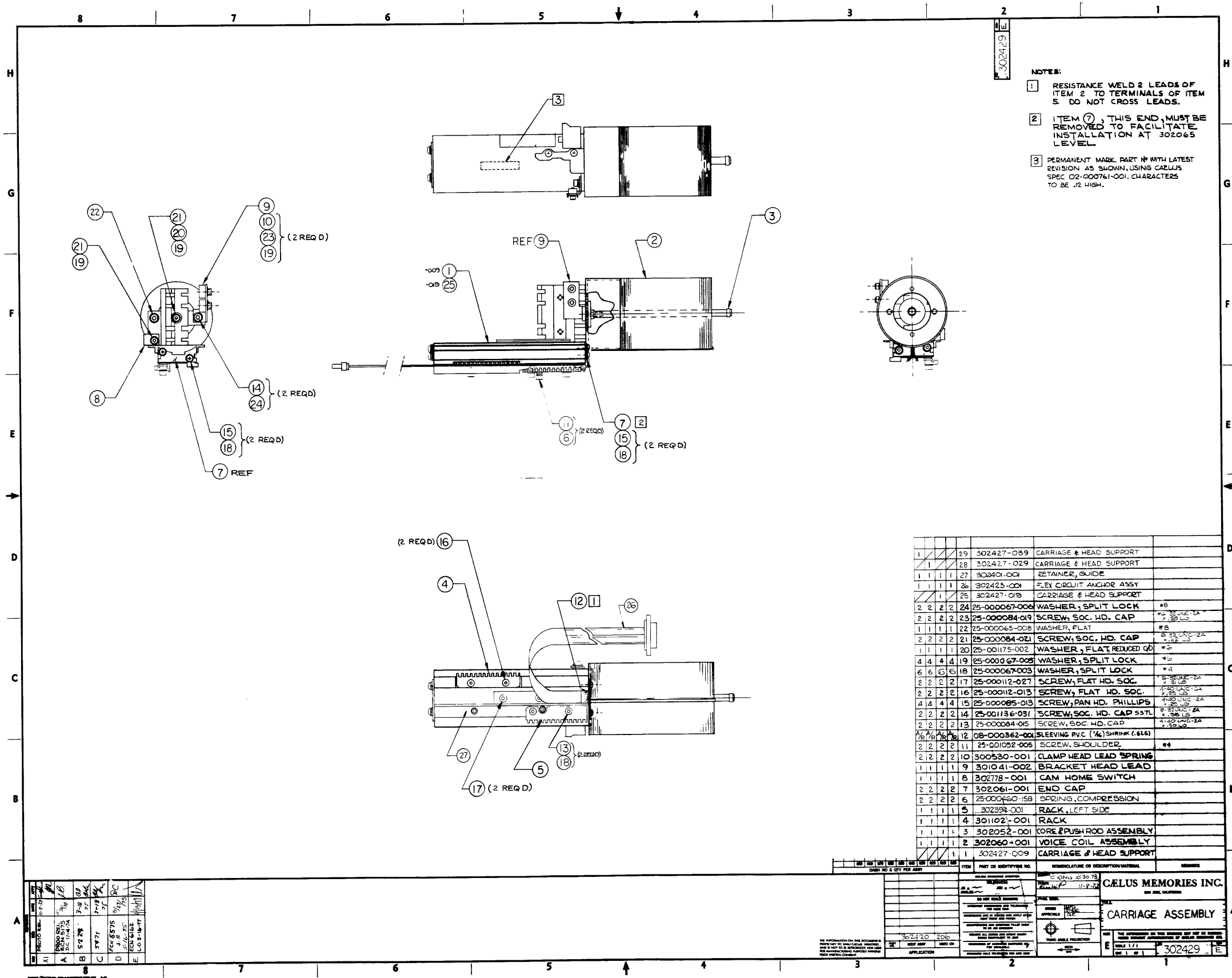
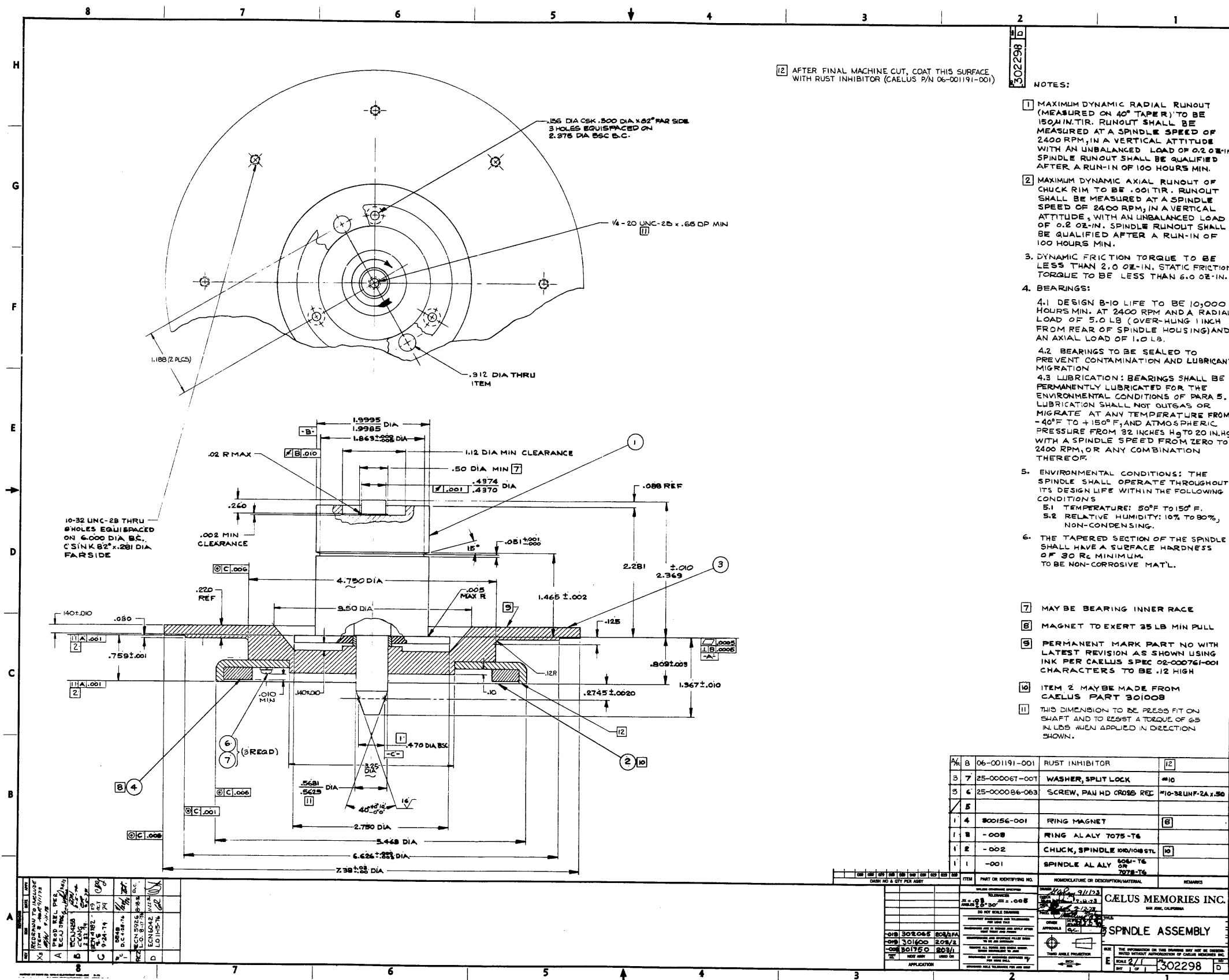


Figure 8-14. Carriage Assembly



(12) AFTER FINAL MACHINE CUT, COAT THIS SURFACE WITH RUST INHIBITOR (CAELUS P/N 06-001191-001)

- NOTES:
1. MAXIMUM DYNAMIC RADIAL RUNOUT (MEASURED ON 40° TAPER) TO BE 150 μIN. TIR. RUNOUT SHALL BE MEASURED AT A SPINDLE SPEED OF 2400 RPM, IN A VERTICAL ATTITUDE WITH AN UNBALANCED LOAD OF 0.2 OZ. IN. SPINDLE RUNOUT SHALL BE QUALIFIED AFTER A RUN-IN OF 100 HOURS MIN.
 2. MAXIMUM DYNAMIC AXIAL RUNOUT OF CHUCK RIM TO BE .001 TIR. RUNOUT SHALL BE MEASURED AT A SPINDLE SPEED OF 2400 RPM, IN A VERTICAL ATTITUDE, WITH AN UNBALANCED LOAD OF 0.2 OZ. IN. SPINDLE RUNOUT SHALL BE QUALIFIED AFTER A RUN-IN OF 100 HOURS MIN.
 3. DYNAMIC FRICTION TORQUE TO BE LESS THAN 2.0 OZ. IN. STATIC FRICTION TORQUE TO BE LESS THAN 6.0 OZ. IN.
 4. BEARINGS:
 - 4.1 DESIGN B-10 LIFE TO BE 10,000 HOURS MIN. AT 2400 RPM AND A RADIAL LOAD OF 5.0 LB (OVER-HUNG 1 INCH FROM REAR OF SPINDLE HOUSING) AND AN AXIAL LOAD OF 1.0 LB.
 - 4.2 BEARINGS TO BE SEALED TO PREVENT CONTAMINATION AND LUBRICANT MIGRATION.
 - 4.3 LUBRICATION: BEARINGS SHALL BE PERMANENTLY LUBRICATED FOR THE ENVIRONMENTAL CONDITIONS OF PARA 5. LUBRICATION SHALL NOT OUTGAS OR MIGRATE AT ANY TEMPERATURE FROM -40°F TO +150°F, AND ATMOSPHERIC PRESSURE FROM 32 INCHES Hg TO 20 IN. Hg WITH A SPINDLE SPEED FROM ZERO TO 2400 RPM, OR ANY COMBINATION THEREOF.
 5. ENVIRONMENTAL CONDITIONS: THE SPINDLE SHALL OPERATE THROUGHOUT ITS DESIGN LIFE WITHIN THE FOLLOWING CONDITIONS
 - 5.1 TEMPERATURE: 50°F TO 150°F.
 - 5.2 RELATIVE HUMIDITY: 10% TO 80%, NON-CONDENSING.
 6. THE TAPERED SECTION OF THE SPINDLE SHALL HAVE A SURFACE HARDNESS OF 30 Rc MINIMUM. TO BE NON-CORROSIVE MAT'L.
 7. MAY BE BEARING INNER RACE
 8. MAGNET TO EXERT 25 LB MIN PULL
 9. PERMANENT MARK PART NO WITH LATEST REVISION AS SHOWN USING INK PER CAELUS SPEC 02-000761-001 CHARACTERS TO BE .12 HIGH
 10. ITEM 2 MAY BE MADE FROM CAELUS PART 301008
 11. THIS DIMENSION TO BE PRESS FIT ON SHAFT AND TO RESIST A TORQUE OF 65 IN. LBS WHEN APPLIED IN DIRECTION SHOWN.

ITEM	PART OR IDENTIFYING NO.	QUANTITY	REMARKS
11	06-001191-001	1	RUST INHIBITOR (12)
3	75-000067-001	1	WASHER, SPLIT LOCK (810)
3	25-000086-063	1	SCREW, PAN HD CROSS REC #10-32 UNF-2A x .30
4	800156-001	1	RING MAGNET (8)
8	-008	1	RING AL ALY 7075-T6
8	-002	1	CHUCK, SPINDLE 100/108 STL (10)
1	-001	1	SPINDLE AL ALY 6061-T6 OR 7075-T6

REV	DATE	BY	CHKD	DESCRIPTION
A				PRELIMINARY DRAWING
B				REVISED PER 3/11/75
C				REVISED PER 3/11/75
D				REVISED PER 3/11/75

CAELUS MEMORIES INC.
SAN JOSE, CALIFORNIA

302298

SPINDLE ASSEMBLY

SCALE: 2/1

DATE: 3/11/75

APPROVED: [Signature]

DATE: 3/11/75

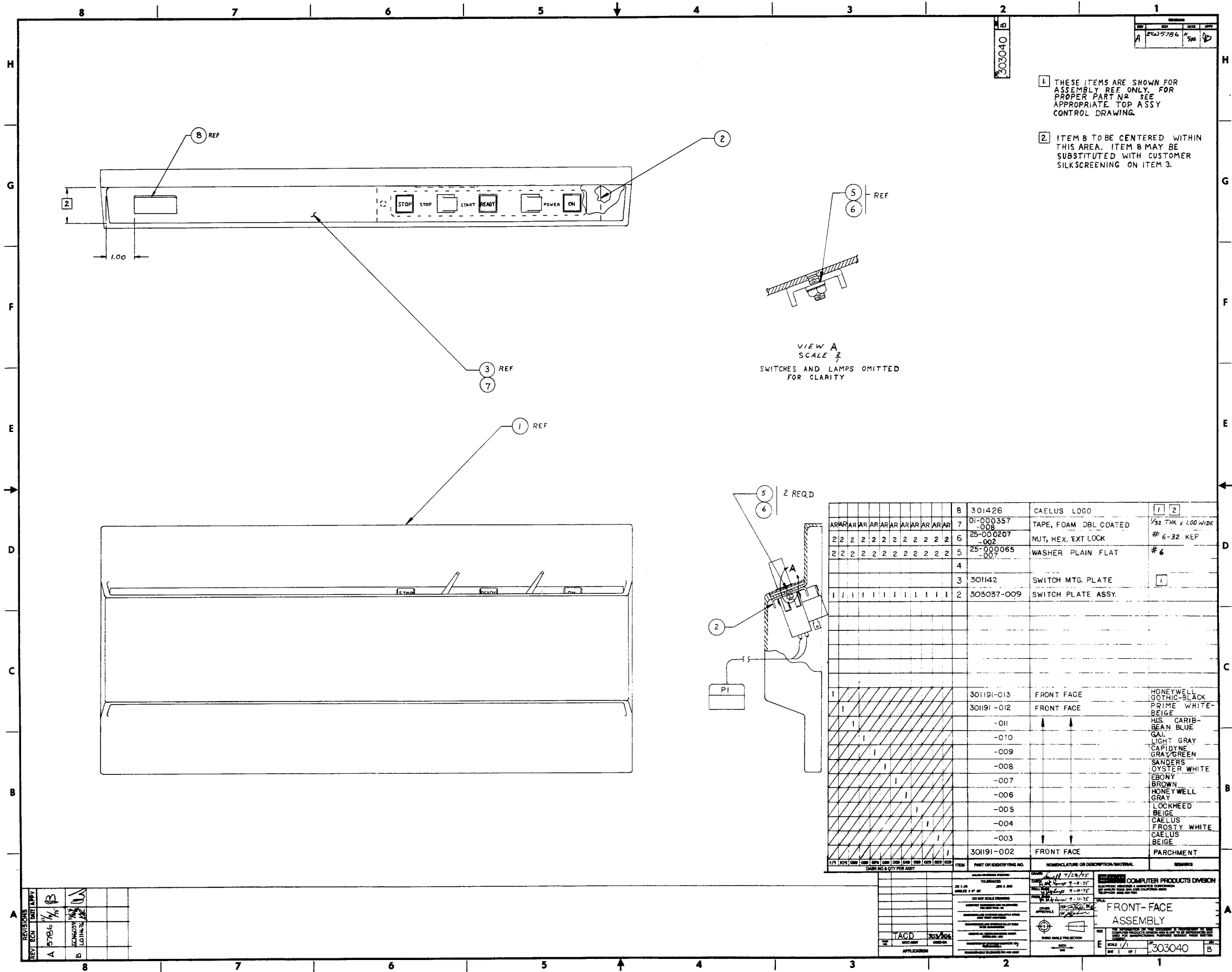
BY: [Signature]

DATE: 3/11/75

REVISIONS: [Table]

APPROVALS: [Table]

Figure 8-15. 206 Spindle Assembly



[1] THESE ITEMS ARE SHOWN FOR ASSEMBLY REF ONLY. FOR PROPER PART NR SEE APPROPRIATE TOP ASSY CONTROL DRAWING.
 [2] ITEM 8 TO BE CENTERED WITHIN THIS AREA. ITEM 8 MAY BE SUBSTITUTED WITH CUSTOMER SILKSCREENING ON ITEM 3.

VIEW A
 SCALE $\frac{2}{3}$
 SWITCHES AND LAMPS OMITTED FOR CLARITY

ITEM	QTY	PART OR IDENTIFYING NO.	DESCRIPTION	REMARKS
8	1	301426	CAELUS LOGO	[1] [2]
7	1	01-000357-008	TAPE, FOAM DBL COATED	1/32 THK x 1.00 WIDE
6	2	25-000207-002	NUT, HEX, EXT LOCK	# 6-32 KEP
5	2	25-000065-007	WASHER PLAIN FLAT	# 6
4	1	301142	SWITCH MTG. PLATE	[1]
2	1	303037-009	SWITCH PLATE ASSY.	
1	1	301191-013	FRONT FACE	HONEYWELL GOTHIC-BLACK
1	1	301191-012	FRONT FACE	PRIME WHITE-BEIGE
1	1	-011		HIS CARIB-BEAN BLUE
1	1	-010		GAL. LIGHT GRAY
1	1	-009		CAPLINE GRAY/GREEN
1	1	-008		SANDERS OYSTER WHITE
1	1	-007		EBONY BROWN
1	1	-006		HONEYWELL GRAY
1	1	-005		LOCKHEED BEIGE
1	1	-004		CAELUS FROSTY WHITE
1	1	-003		CAELUS BEIGE
1	1	301191-002	FRONT FACE	PARCHMENT

REV	BY	DATE	DESCRIPTION
A	5786		
B			

COMPUTER PRODUCTS DIVISION
 FRONT-FACE ASSEMBLY
 SCALE 1/1
 303040

Figure 8-16. 306 Front Face Assembly

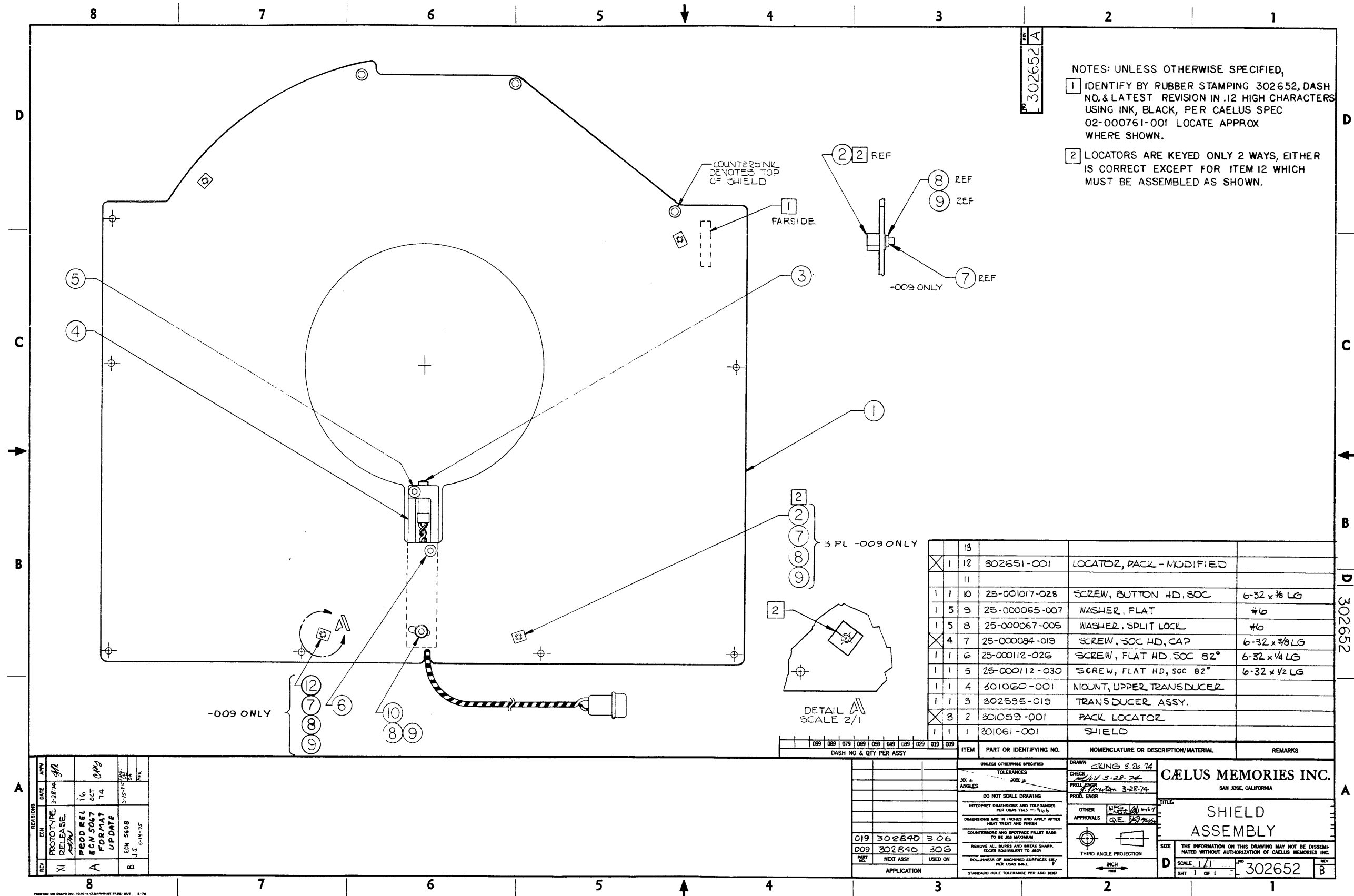


Figure 8-17. 306 Shield Assembly

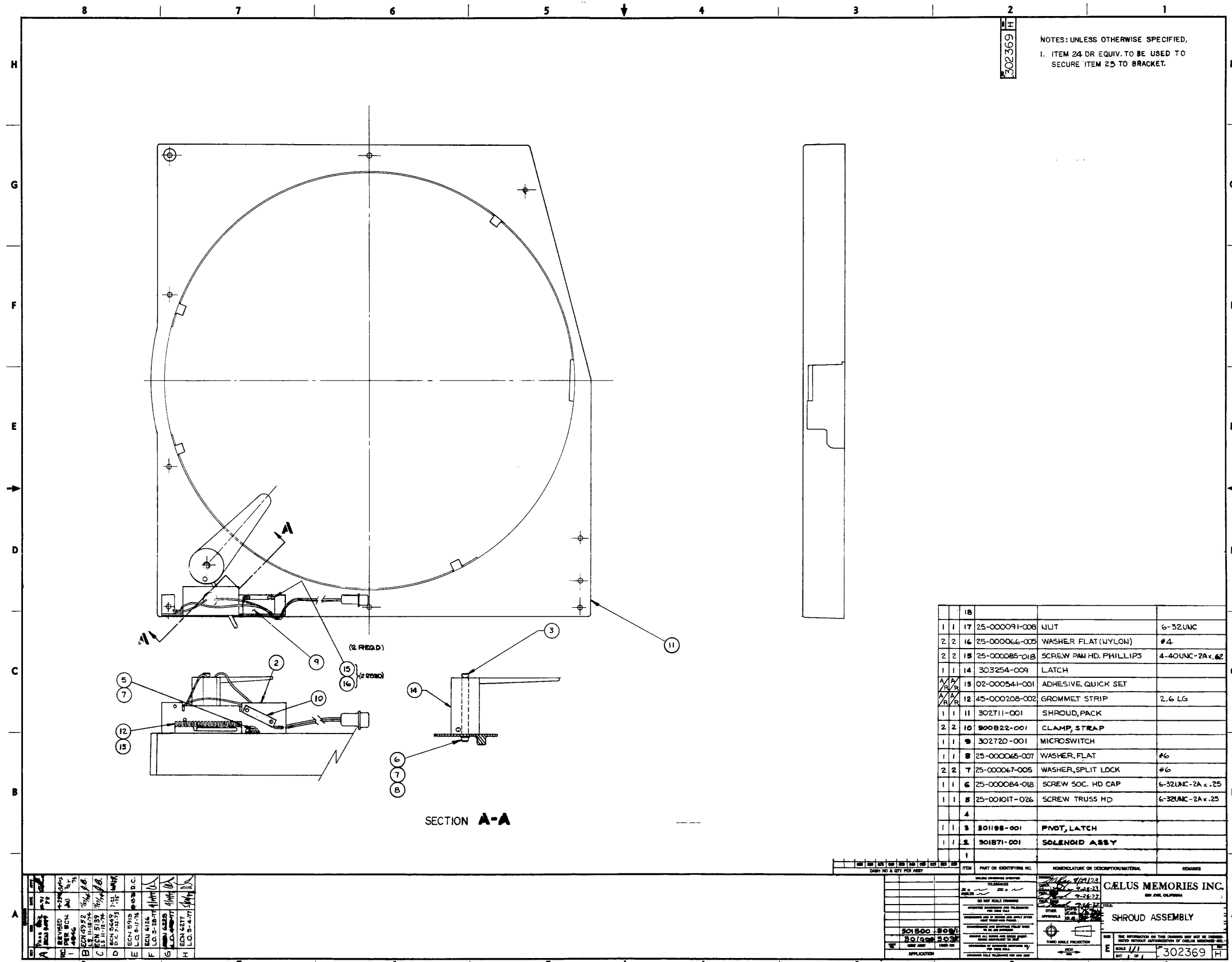


Figure 8-18. 306 Shroud Assembly

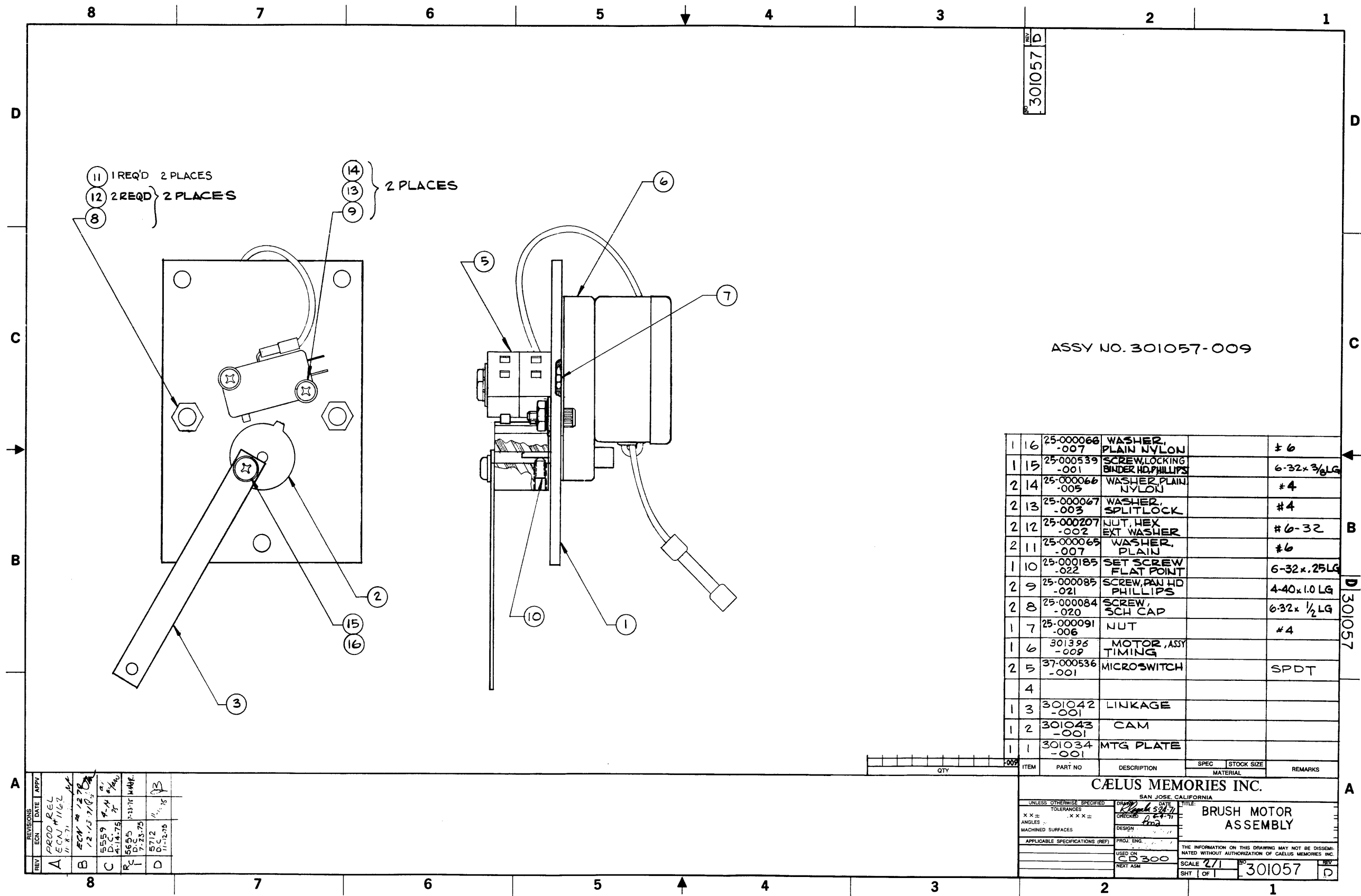


Figure 8-19. 306 Brush Motor Assembly

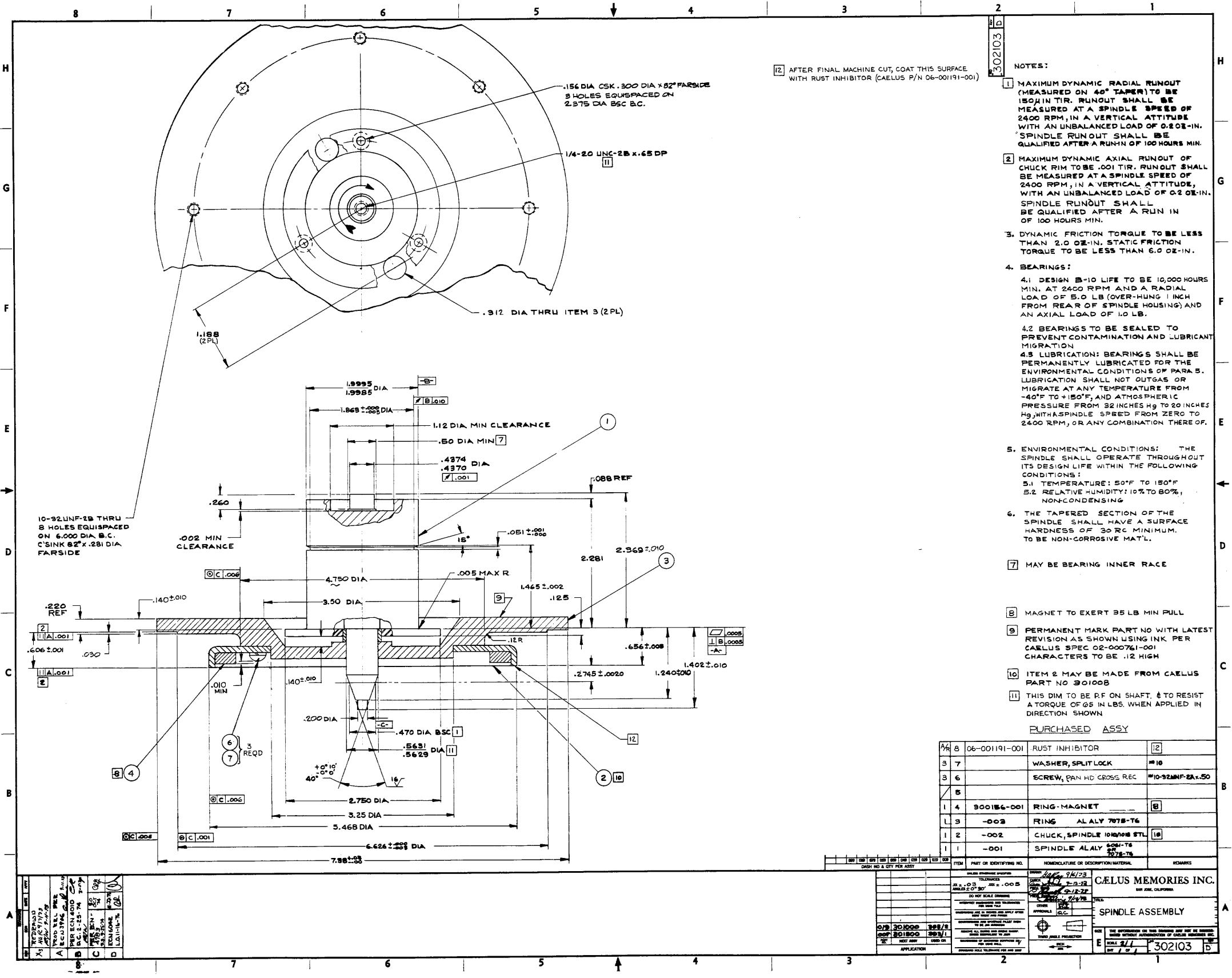
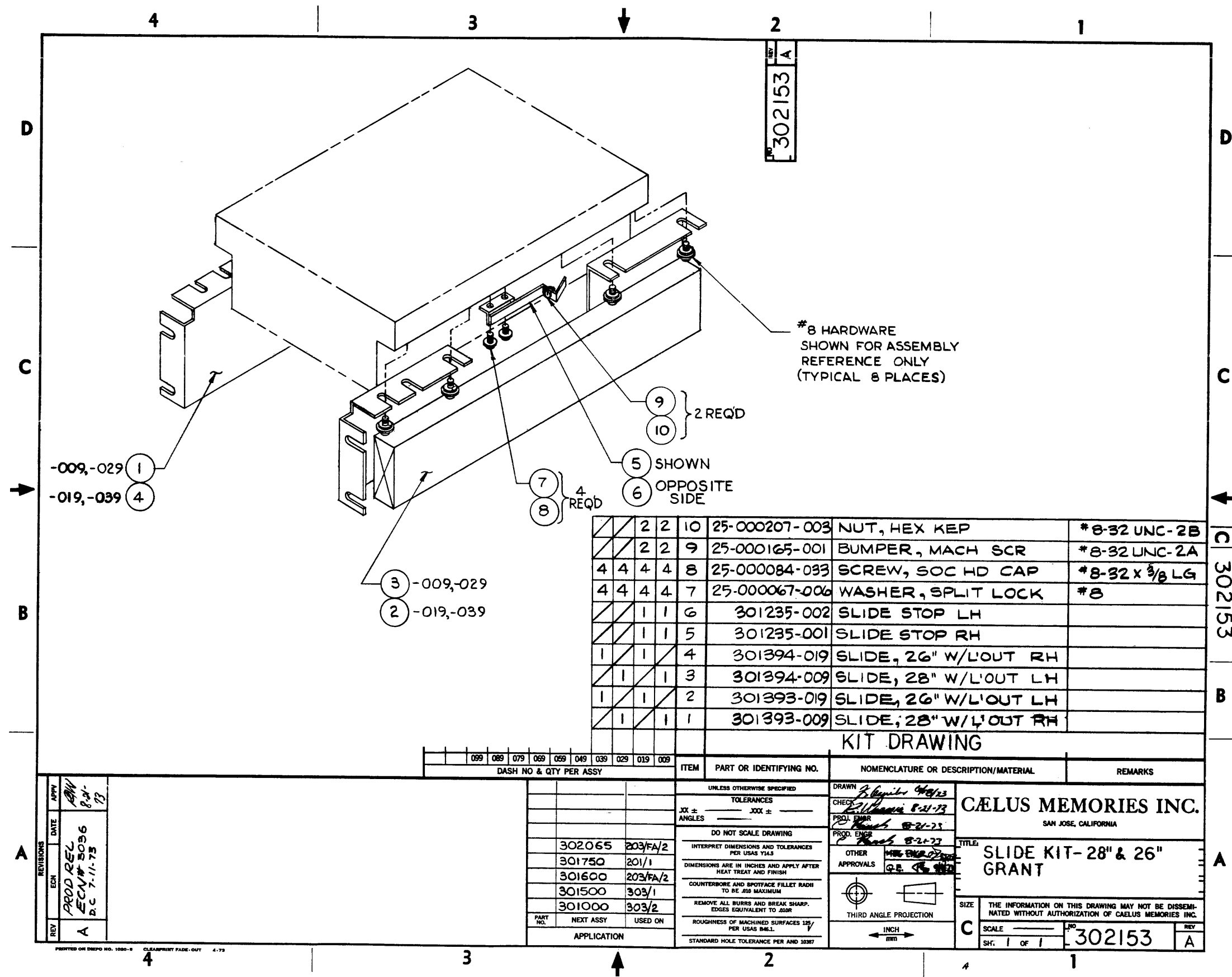


Figure 8-20. 306 Spindle Assembly



2	2	10	25-000207-003	NUT, HEX KEP	#8-32 UNC-2B
2	2	9	25-000165-001	BUMPER, MACH SCR	#8-32 UNC-2A
4	4	4	25-000084-033	SCREW, SOC HD CAP	#8-32 X 3/8 LG
4	4	4	25-000067-006	WASHER, SPLIT LOCK	#8
1	1	1	301235-002	SLIDE STOP LH	
1	1	1	301235-001	SLIDE STOP RH	
1	1	1	301394-019	SLIDE, 26" W/L'OUT RH	
1	1	1	301394-009	SLIDE, 28" W/L'OUT LH	
1	1	1	301393-019	SLIDE, 26" W/L'OUT LH	
1	1	1	301393-009	SLIDE, 28" W/L'OUT RH	

059	069	079	089	099	049	039	029	019	009
DASH NO & QTY PER ASSY									
ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	REMARKS						

REV	ECN	DATE	APPV
A		7-11-73	AW
ADD REL ECN# 5036 D.C. 7-11-73			

302065	203/FA/2	
301750	201/1	
301600	203/FA/2	
301500	303/1	
301000	303/2	
PART NO.	NEXT ASSY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED

TOLERANCES
XX ± JOX ±

ANGLES

DO NOT SCALE DRAWING

INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.3

DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH

COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM

REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R

ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1

STANDARD HOLE TOLERANCE PER AND 10387

DRAWN: *P. Grant 8-21-73*

CHECKED: *M. Grant 8-21-73*

PROL. ENGR: *P. Grant 8-21-73*

PROD. ENGR: *P. Grant 8-21-73*

OTHER APPROVALS: *G.E. 8-21-73*

THIRD ANGLE PROJECTION

INCH

MILL

CAELUS MEMORIES INC.
SAN JOSE, CALIFORNIA

TITLE: **SLIDE KIT-28" & 26" GRANT**

SIZE: THE INFORMATION ON THIS DRAWING MAY NOT BE DISSEMINATED WITHOUT AUTHORIZATION OF CAELUS MEMORIES INC.

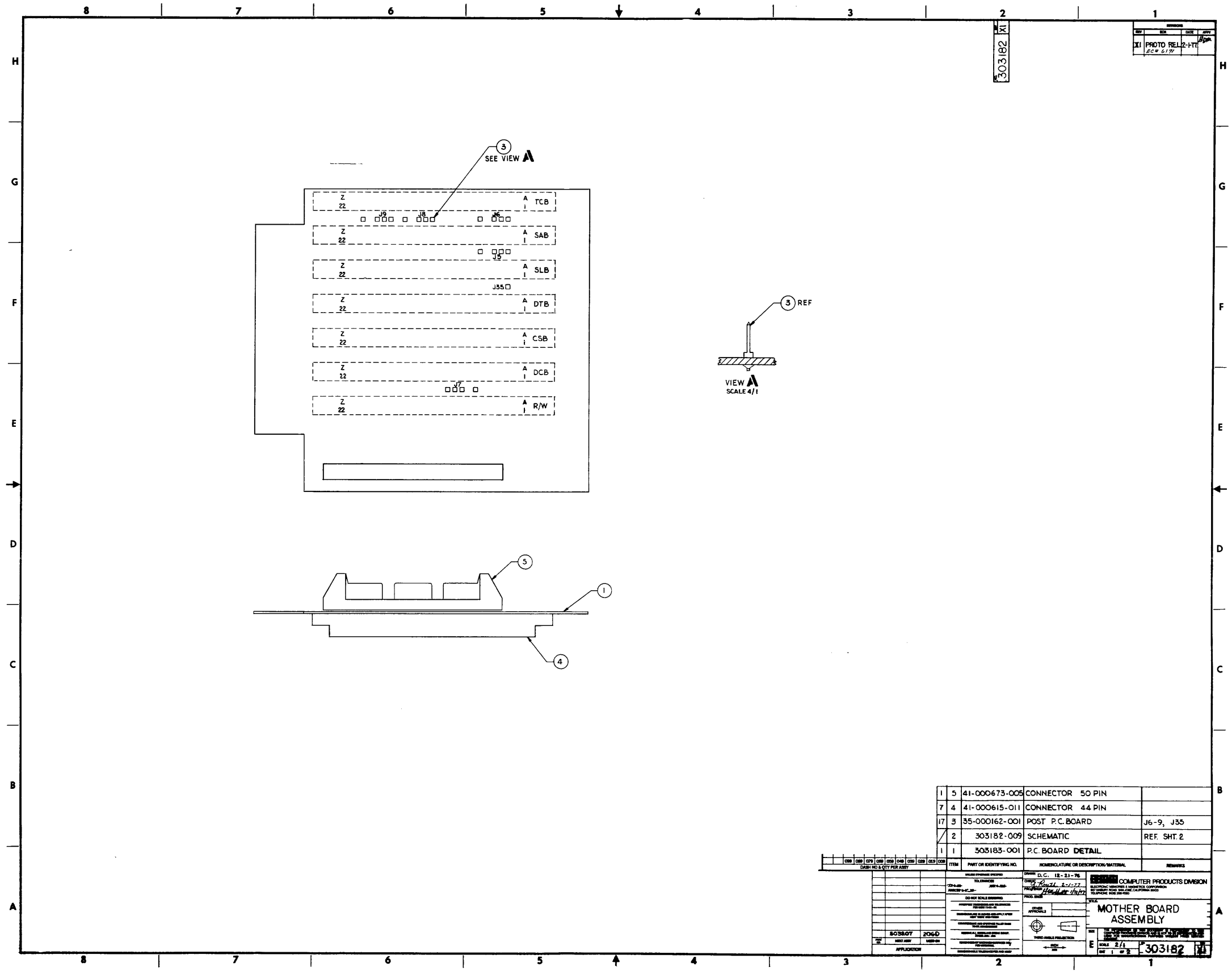
SCALE: _____

NO. **302153**

REV. **A**

SH. 1 OF 1

Figure 8-21. Slide Kit



ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	REMARKS
1	5	41-000673-005	CONNECTOR 50 PIN
7	4	41-000615-011	CONNECTOR 44 PIN
17	3	35-000162-001	POST P.C BOARD
2		303182-009	SCHEMATIC
1		303183-001	P.C BOARD DETAIL

BOSSBY 2060 APPROVED: _____ DATE: _____		COMPUTER PRODUCTS DIVISION ELECTRONIC LABORATORIES CORPORATION 10000 WOODBURY AVENUE WOODBURY, NEW YORK 11797 TEL: (516) 325-1000	
TITLE: _____ DRAWN BY: _____ CHECKED BY: _____ DATE: _____		PROJECT: _____ PART NO: _____ REV: _____ SHEET: 2/1 OF: 2	

Figure 8-22. Mother Board Assembly

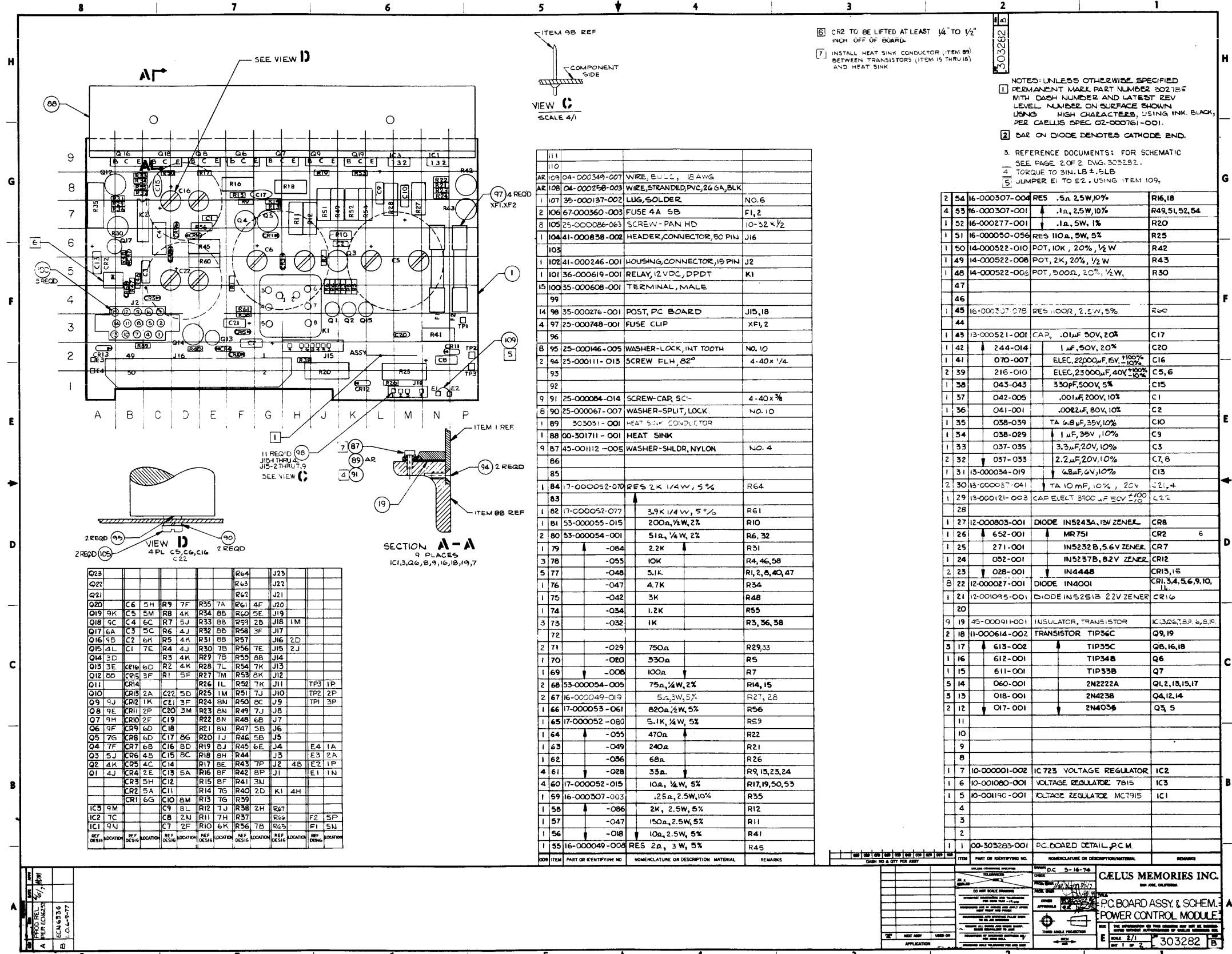


Figure 8-23. Power Control Module Assembly

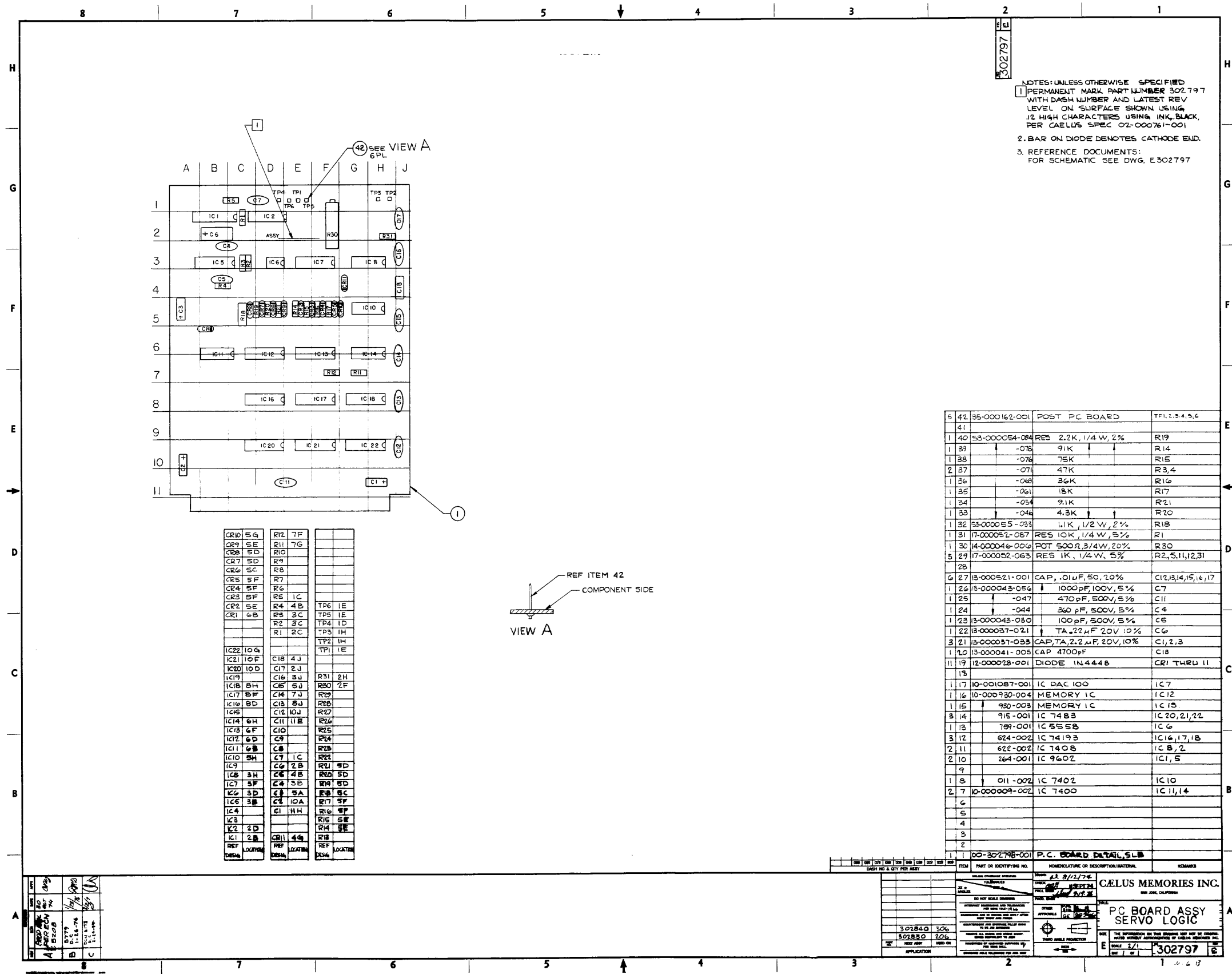


Figure 8-24. Servo Logic Board Assembly

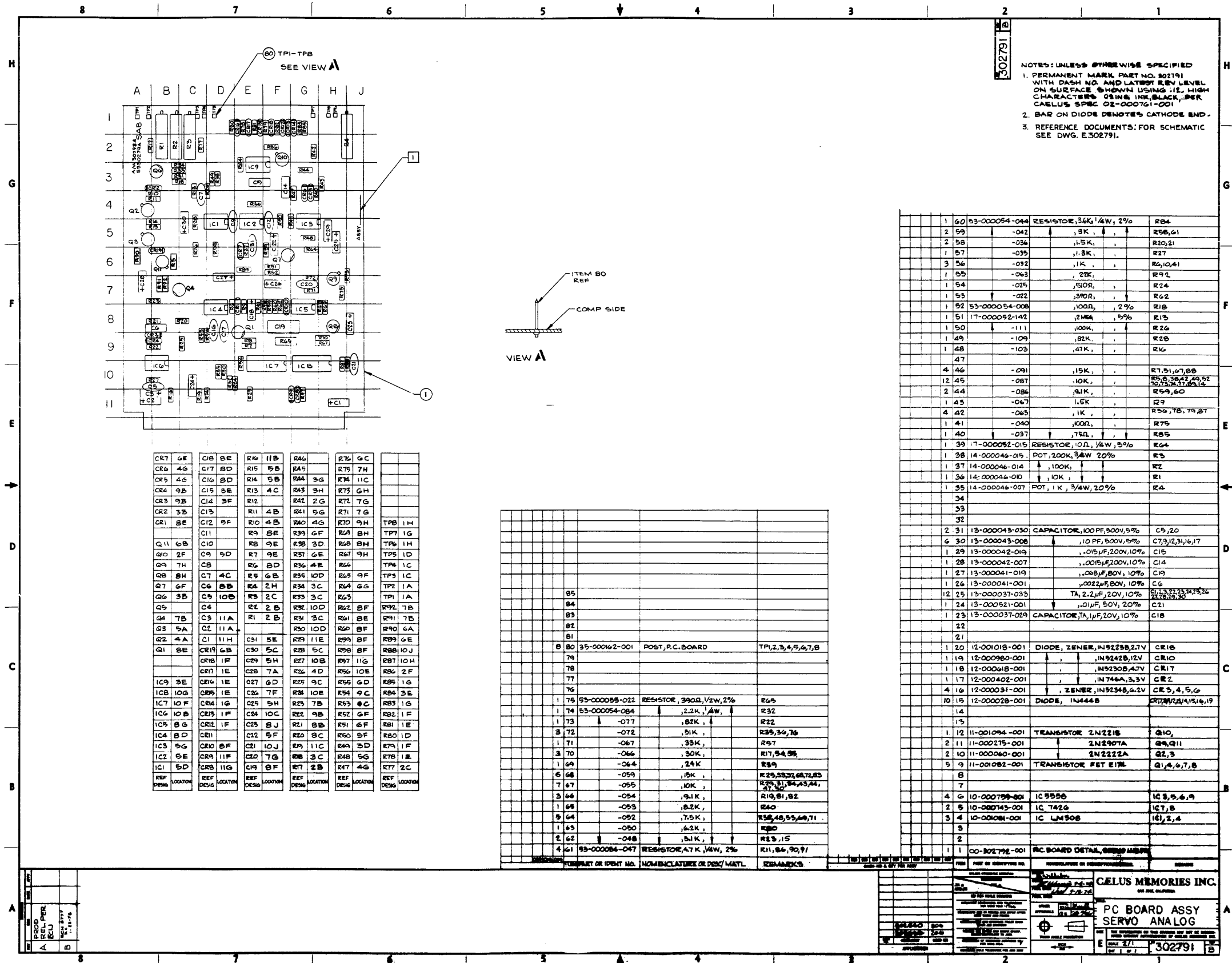


Figure 8-25. Servo Analog Board Assembly

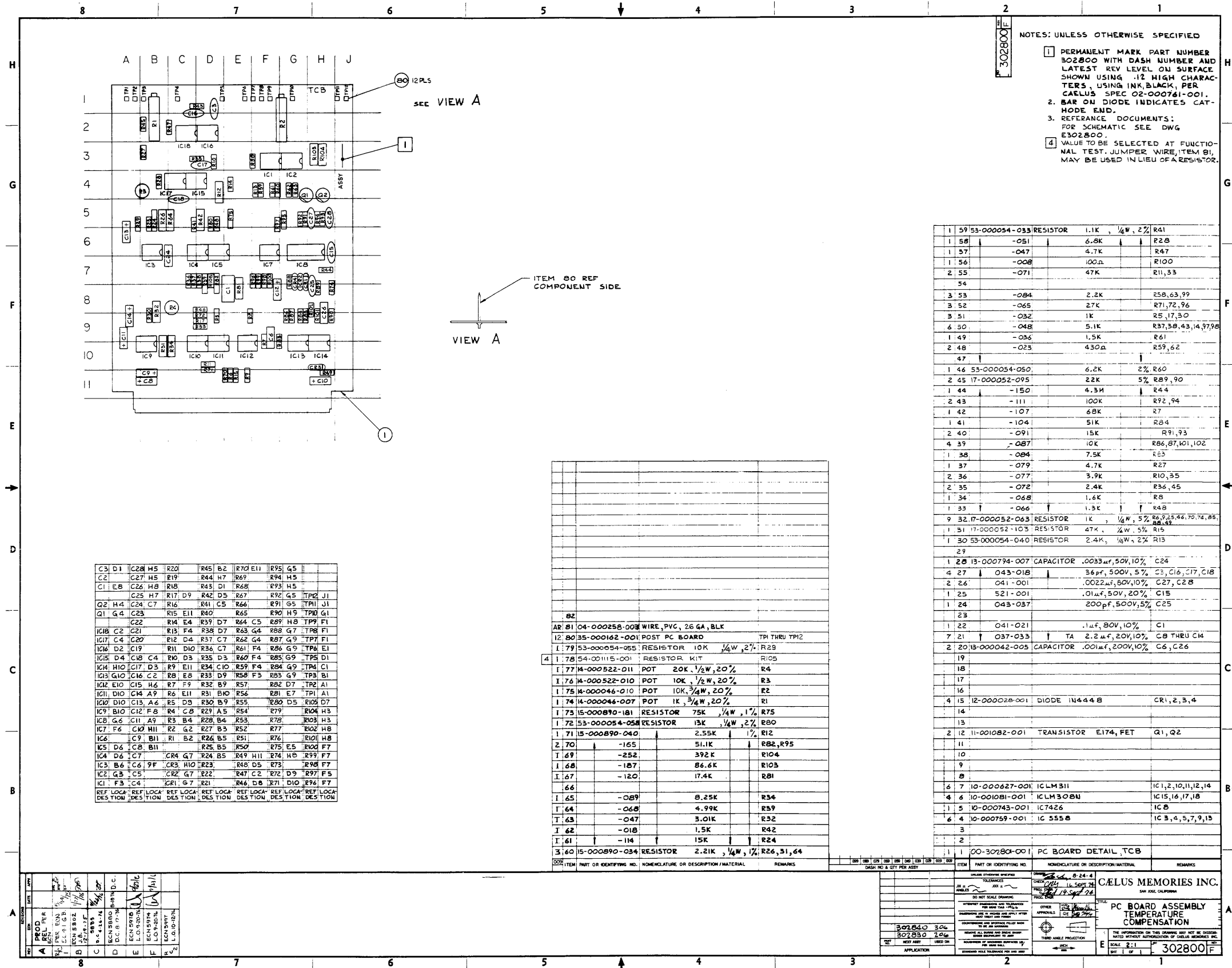


Figure 8-26. Temperature Compensation Board

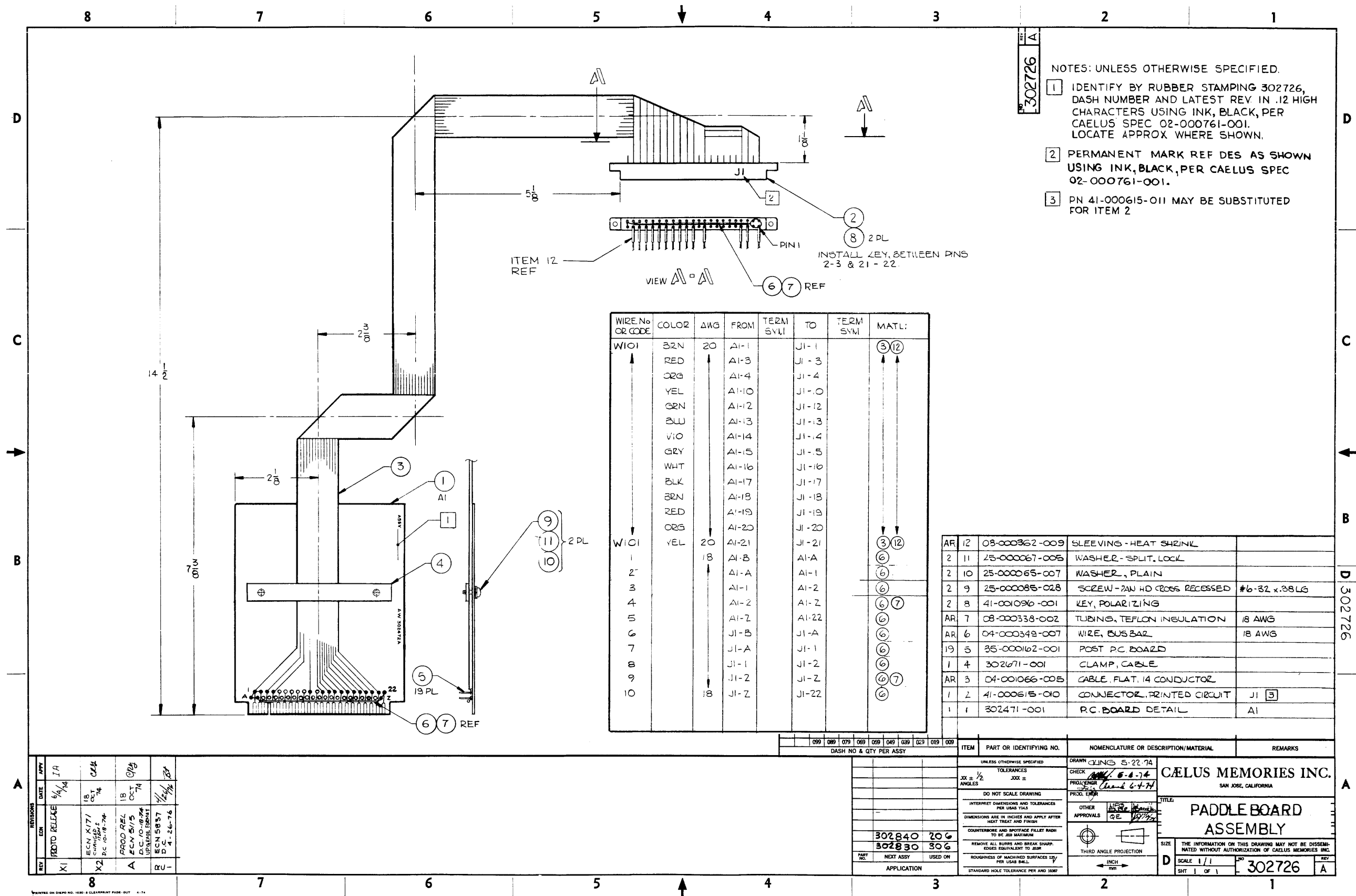


Figure 8-27. Paddle Board Assembly

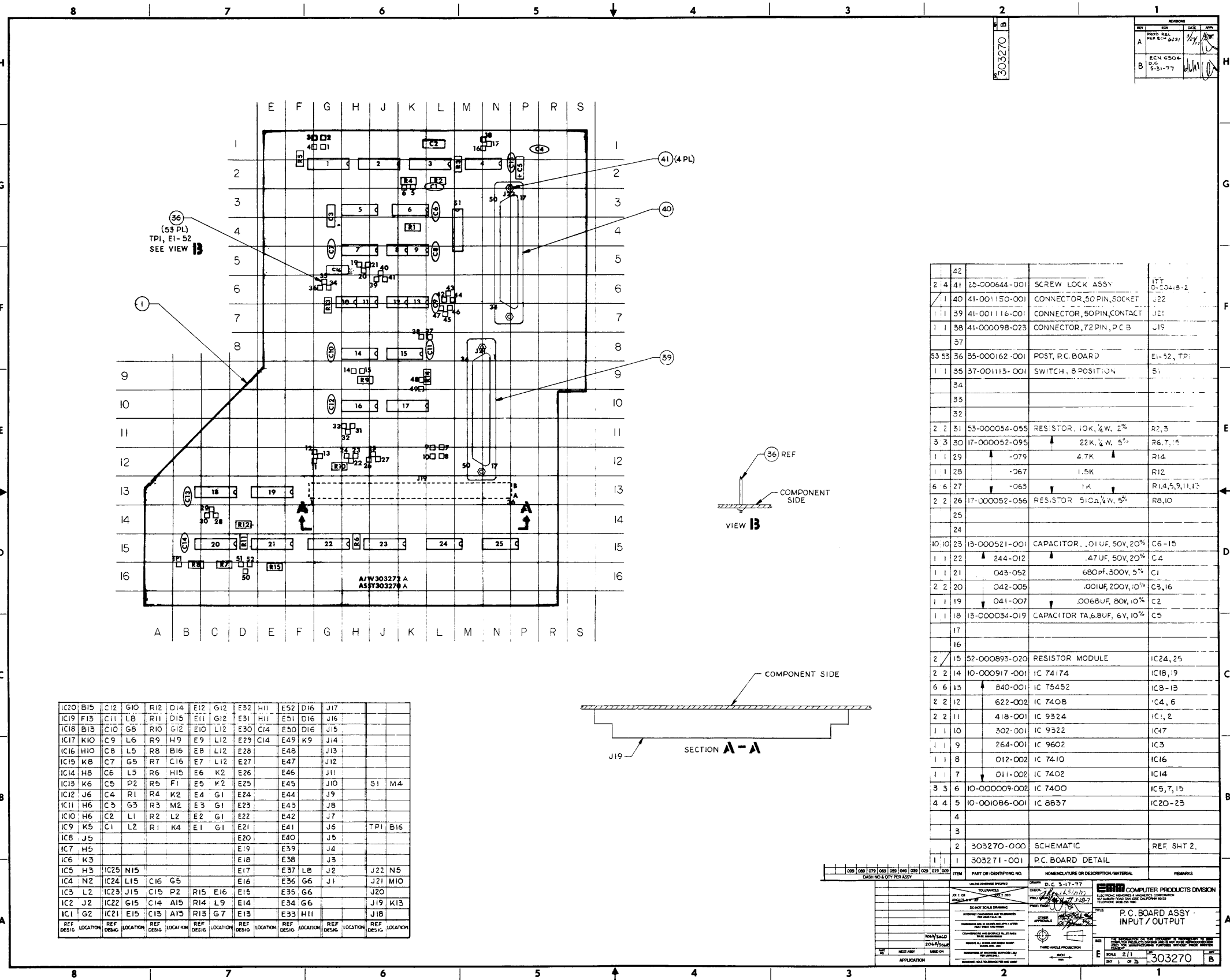


Figure 8-28. Input/Output Board Assembly

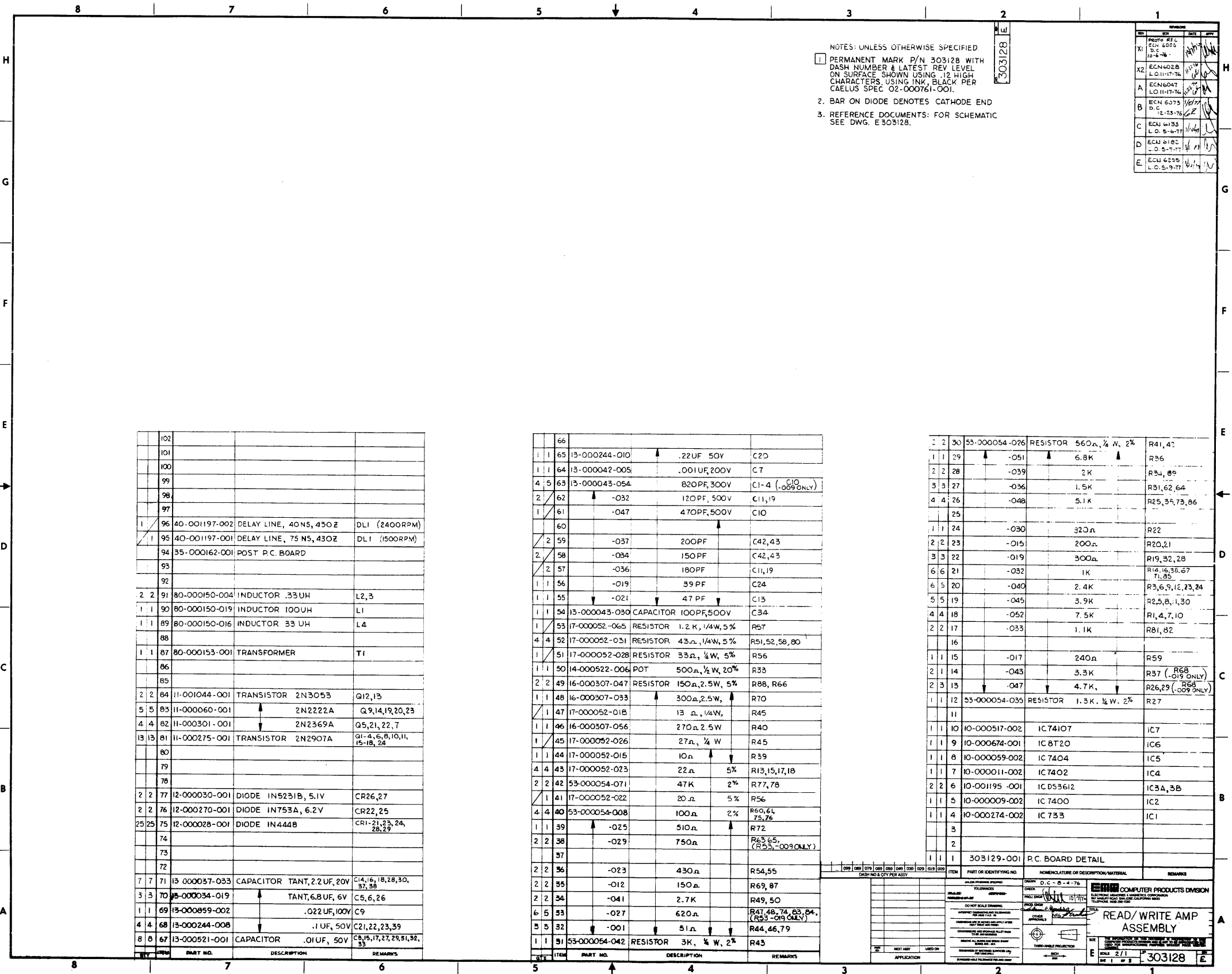
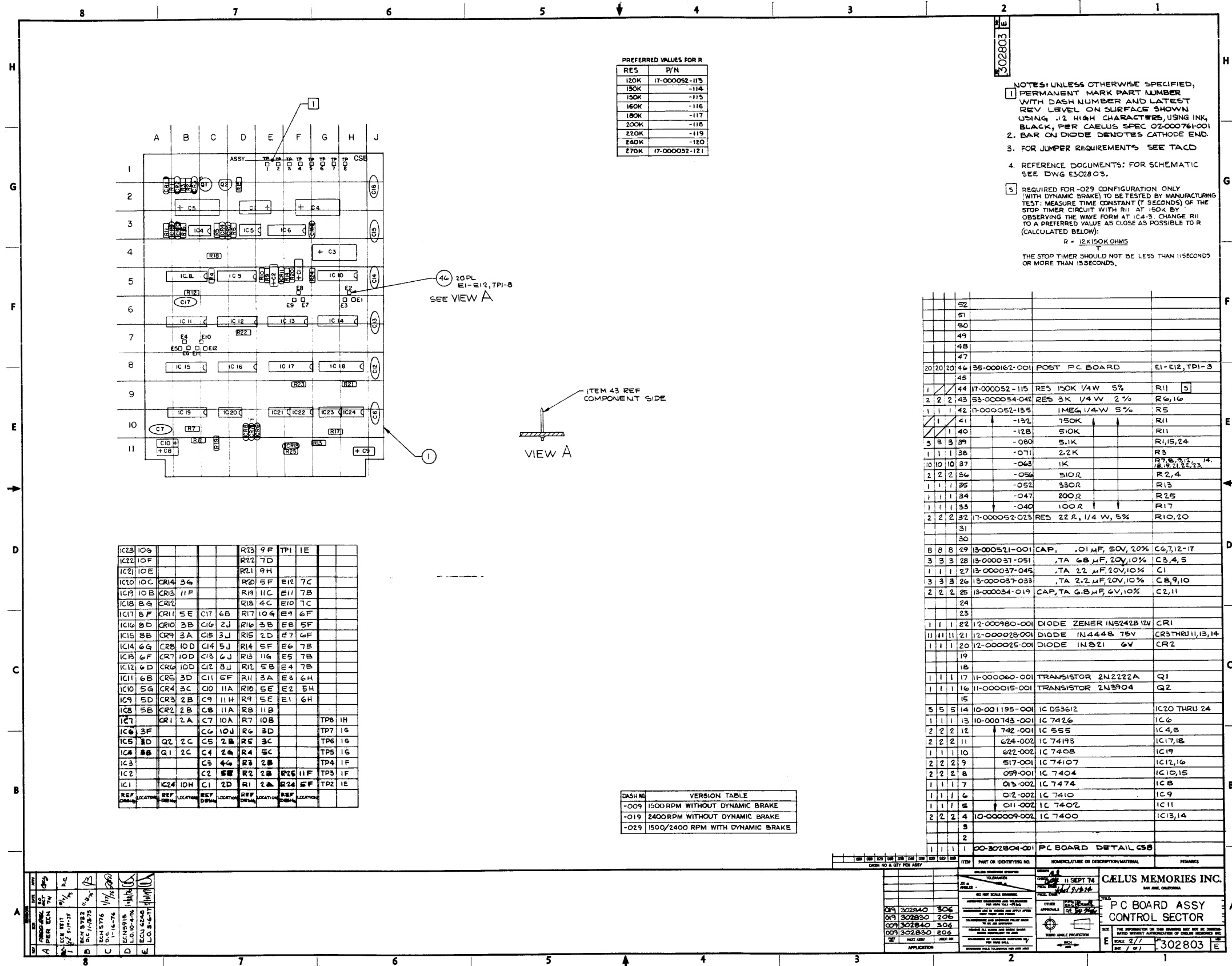


Figure 8-29. 200 TPI Read/Write Amplifier Assembly, Sheet 1 of 2



REFERRED VALUES FOR R

RES	P/N
120K	17-000052-113
150K	-114
180K	-115
200K	-116
220K	-117
240K	-118
270K	17-000052-121

- NOTES: UNLESS OTHERWISE SPECIFIED,
- PERMANENT MARK PART NUMBER WITH DASH NUMBER AND LATEST REV. LEVEL ON SURFACE SHOWN USING .12 HIGH CHARACTERS, USING INK, BLACK, PER CAELUS SPEC 02-000761-001
 - BAR ON DIODE DENOTES CATHODE END.
 - FOR JUMPER REQUIREMENTS SEE TACD
 - REFERENCE DOCUMENTS: FOR SCHEMATIC SEE DWG E302803.
3. REQUIRED FOR -029 CONFIGURATION ONLY (WITH DYNAMIC BRAKE) TO BE TESTED BY MANUFACTURING TEST MEASURE TIME CONSTANT (T SECONDS) OF THE STOP TIMER CIRCUIT WITH R11 AT 150K BY OBSERVING THE WAVE FORM AT IC4-3. CHANGE R11 TO A PREFERRED VALUE AS CLOSE AS POSSIBLE TO R (CALCULATED BELOW):
- $$R = 12 \times 150K \text{ OHMS}$$
- THE STOP TIMER SHOULD NOT BE LESS THAN 11 SECONDS OR MORE THAN 15 SECONDS.

IC23	IO6			R23	9 F	TP1	IE
IC22	IOF			R22	7 D		
IC21	IOE			R21	9 H		
IC20	IOC	CR4	3 G	R20	5 F	E12	7 C
IC19	IOB	CR3	11 F	R19	11 C	E11	7 B
IC18	8 G	CR2		R18	4 C	E10	7 C
IC17	8 F	CR1	5 E	C17	6 B	R17	10 G
IC16	8 D	CR10	3 B	C16	2 J	R16	3 B
IC15	8 B	CR9	3 A	C15	3 J	R15	2 D
IC14	6 G	CR8	10 D	C14	5 J	R14	5 F
IC13	6 F	CR7	10 D	C13	6 J	R13	11 G
IC12	6 D	CR6	10 D	C12	8 J	R12	5 B
IC11	6 B	CR5	3 D	C11	5 F	R11	3 A
IC10	5 G	CR4	3 C	C10	11 A	R10	5 E
IC9	5 D	CR3	2 B	C9	11 H	R9	5 E
IC8	5 B	CR2	2 B	C8	11 A	R8	11 B
IC7		CR1	2 A	C7	10 A	R7	10 B
IC6	3 F			C6	10 J	R6	3 D
IC5	3 D	Q2	2 C	C5	2 B	R5	3 C
IC4	3 B	Q1	2 C	C4	2 G	R4	5 C
IC3				C3	4 G	R3	2 B
IC2				C2	5 F	R2	2 B
IC1	IC24	IOH	C1	2 D	R1	2 A	5 F

DASH NO. VERSION TABLE

-009	1500RPM WITHOUT DYNAMIC BRAKE
-019	2400RPM WITHOUT DYNAMIC BRAKE
-029	1500/2400 RPM WITH DYNAMIC BRAKE

52			
51			
50			
49			
48			
47			
20	20	46	35-000162-001 POST PC BOARD E1-E12, TPI-3
45			
44	17-000052-115	RES 150K 1/4 W 5%	R11 5
43	53-000054-04E	RES 3K 1/4 W 2%	R6,16
42	17-000052-135	1MEG 1/4 W 5%	R5
41		750K	R11
40		510K	R11
39		51K	R11,5,24
38		2.2K	R3
37		1K	R7,8,9,12,14,18,19,21,22,23
36		510R	R2,4
35		330R	R13
34		200R	R25
33		100R	R17
32	17-000052-023	RES 22R, 1/4 W, 5%	R10,20
31			
30			
29	13-000521-001	CAP, .01MF, 50V, 20%	C6,7,12-17
28	13-000031-051	TA 6.8MF, 20V, 10%	C3,4,5
27	13-000037-045	TA 2.2MF, 20V, 10%	C1
26	13-000037-033	TA 2.2MF, 20V, 10%	C8,9,10
25	13-000034-019	CAP, TA 6.8MF, 6V, 10%	C2,11
24			
23			
22	12-000980-001	DIODE ZENER 1N5242B 12V	CR1
21	12-000028-001	DIODE 1N4448 75V	CR3 THRU 11,13,14
20	12-000025-001	DIODE 1N521 6V	CR2
19			
18			
17	11-000060-001	TRANSISTOR 2N2222A	Q1
16	11-000015-001	TRANSISTOR 2N3904	Q2
15			
14	10-001195-001	IC DS3612	IC20 THRU 24
13	10-000743-001	IC 7426	IC6
12		742-001	IC 555
11		624-002	IC 74193
10		622-002	IC 7408
9		517-001	IC 74107
8		099-001	IC 7404
7		013-002	IC 7474
6		012-002	IC 7410
5		011-002	IC 7402
4	10-000009-002	IC 7400	IC13,14
3			
2			
1	1	00-302804-001	PC BOARD DETAIL CSB

REV	DATE	BY	CHK	DESCRIPTION
A	11/17/74	WJ	WJ	REVISED FOR 1500 RPM
B	11/17/74	WJ	WJ	REVISED FOR 2400 RPM
C	11/17/74	WJ	WJ	REVISED FOR 1500/2400 RPM
D	11/17/74	WJ	WJ	REVISED FOR 1500/2400 RPM WITH DYNAMIC BRAKE
E	11/17/74	WJ	WJ	REVISED FOR 1500/2400 RPM WITH DYNAMIC BRAKE

REVISIONS

DATE: 11 SEPT 74

DESIGNER: WJ

CHECKED: WJ

APPROVED: WJ

DATE: 11 SEPT 74

SCALE: 2/1

302803

PC BOARD ASSY CONTROL SECTOR

Figure 8-31. Control Sector Board Assembly

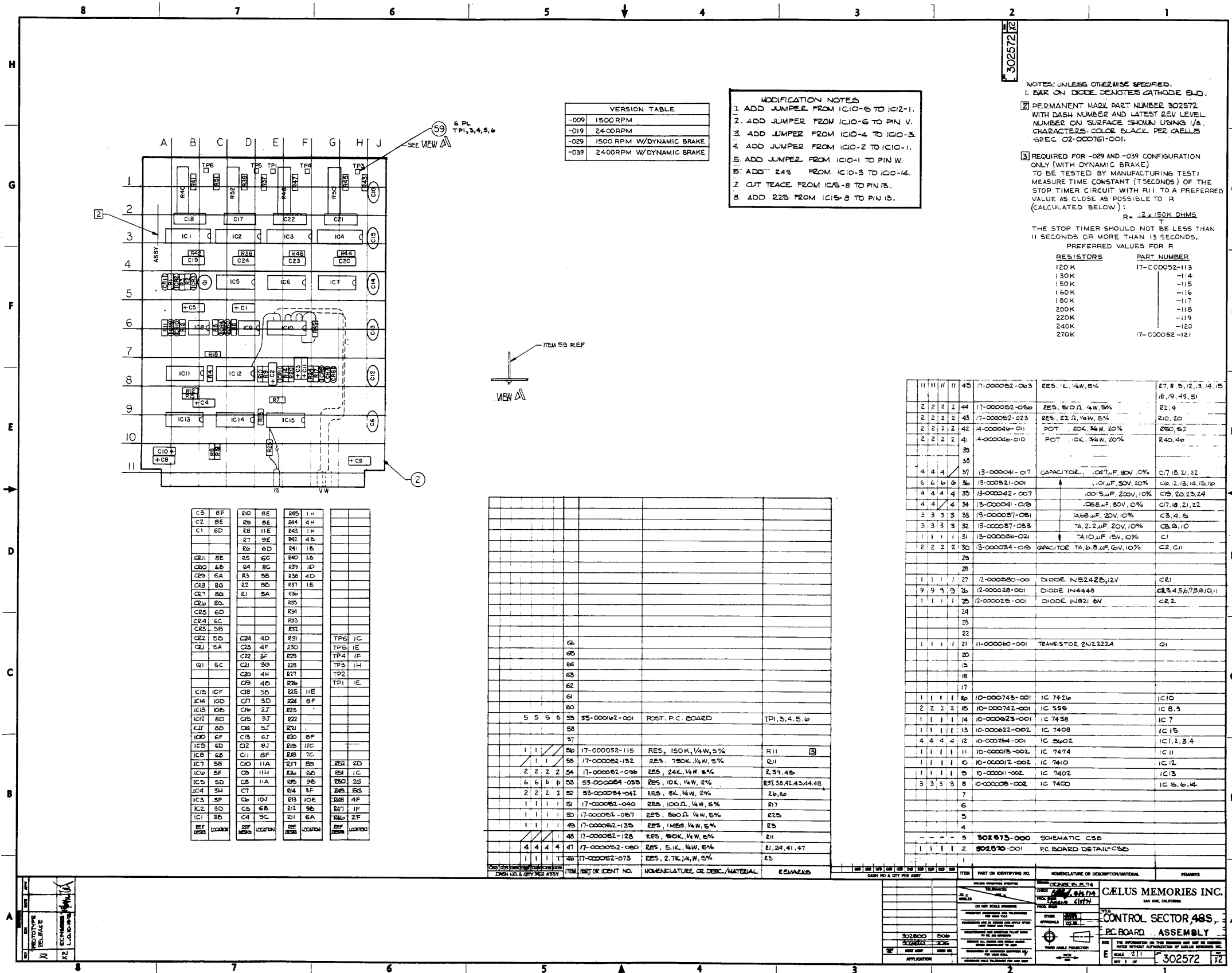


Figure 8-32. Control Sector Board (48) Assembly

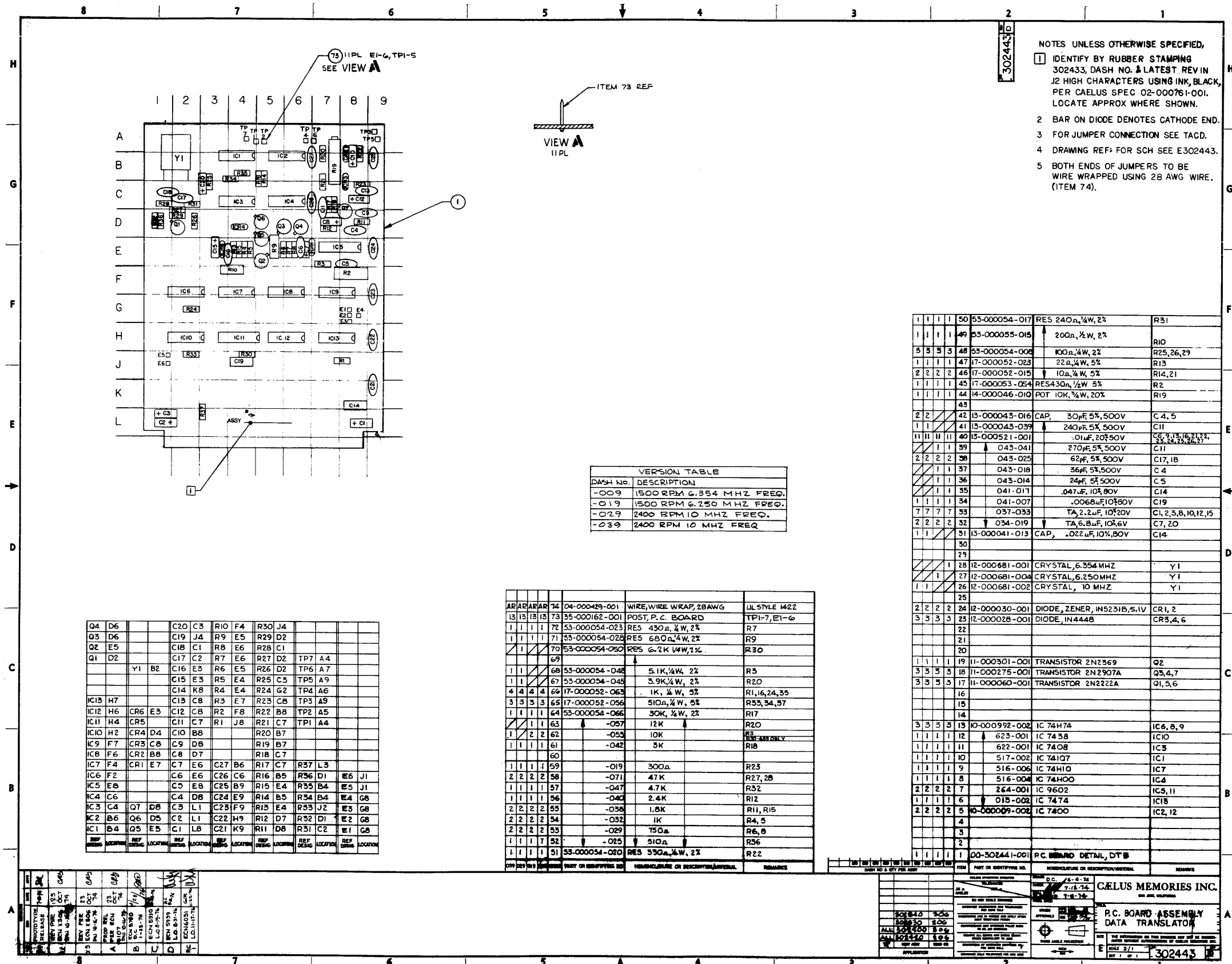


Figure 8-33. Data Translator Board

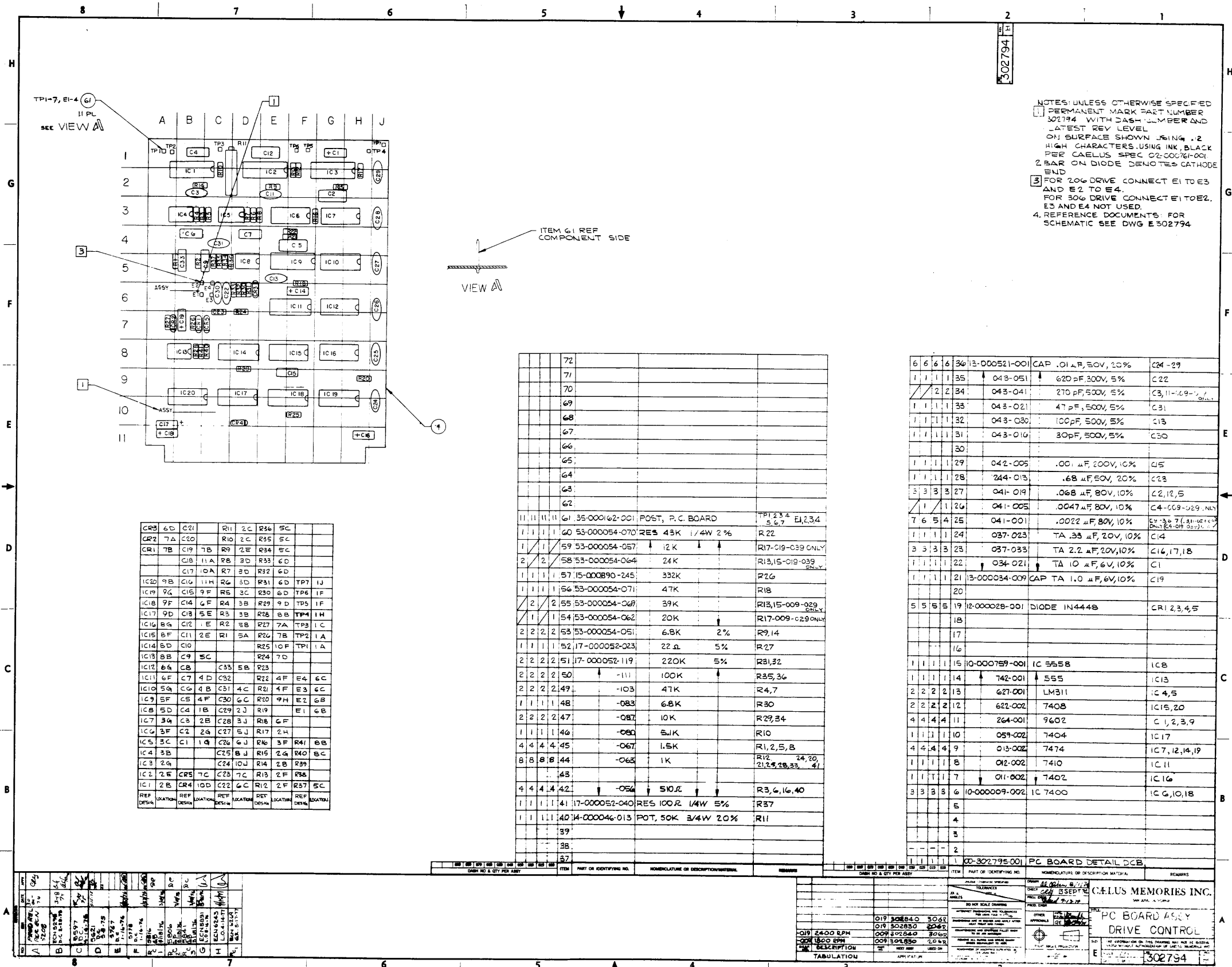
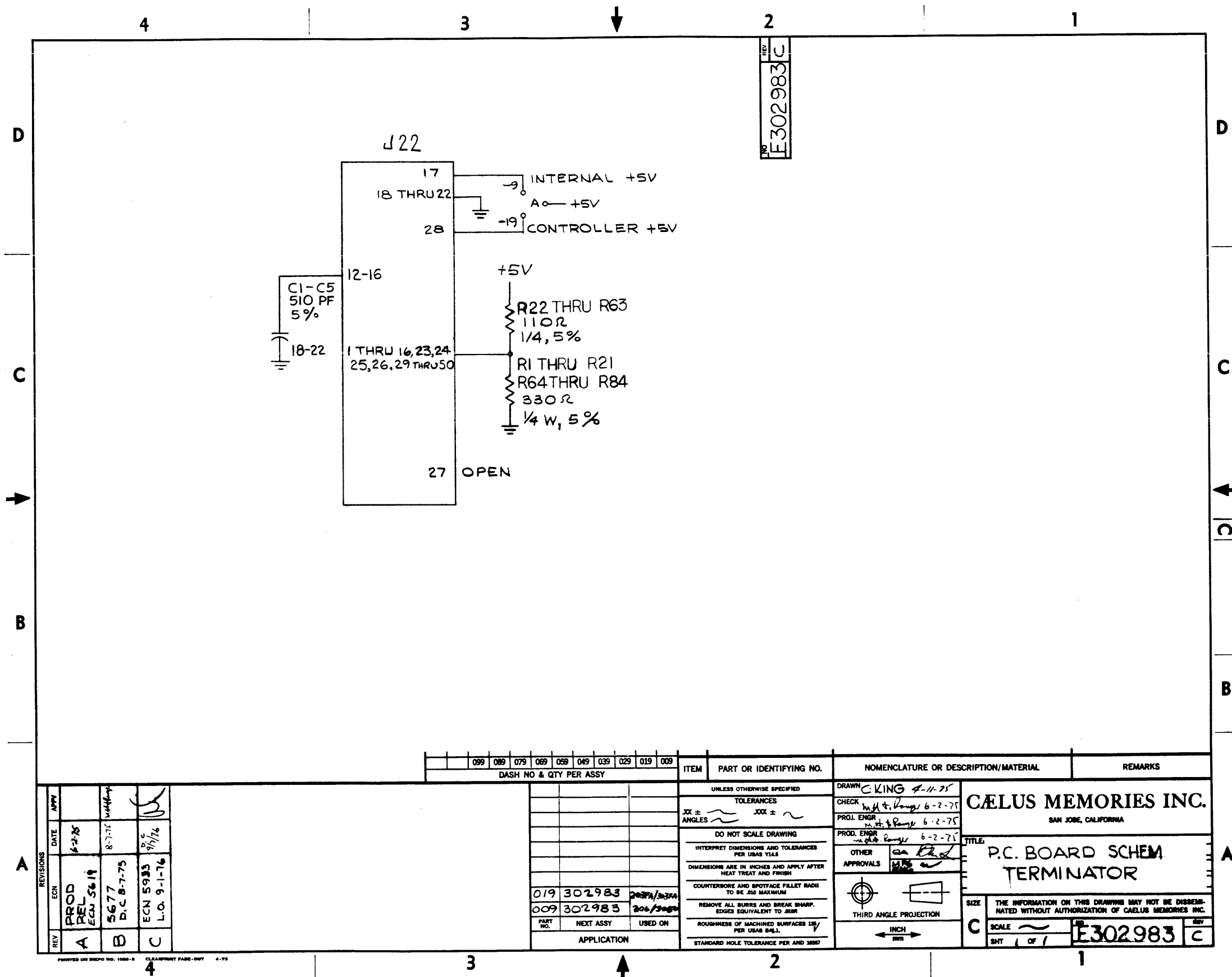
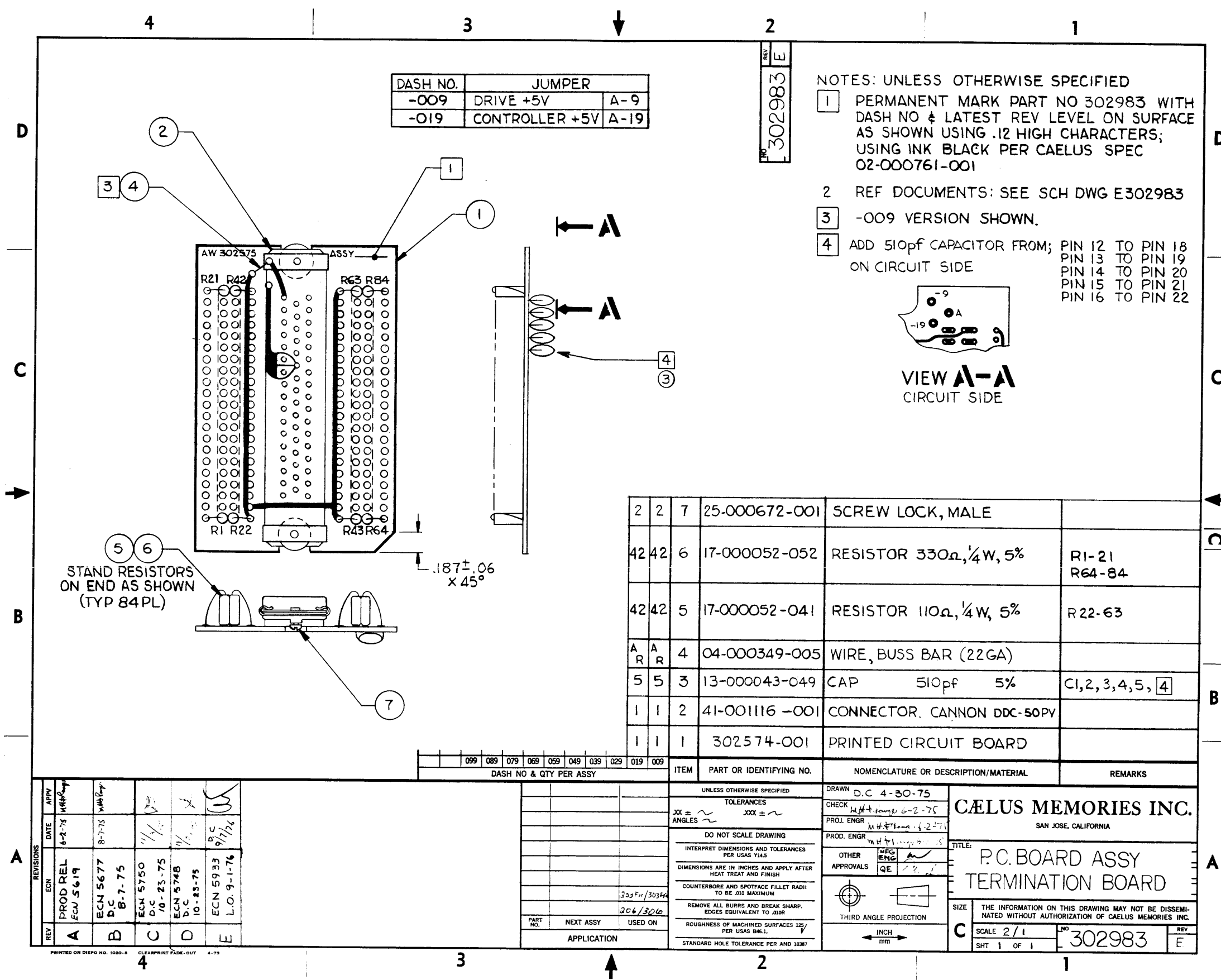


Figure 8-34. Drive Control Board Assembly



REVISIONS				DASH NO & QTY PER ASSY										ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	REMARKS				
REV	ECN	DATE	APPY	009	089	079	069	059	049	039	029	019	009								
A	PROD REL ECU S619	6-2-78												019	302983						
B	5677 D.C.B-7-75	8-7-75												009	302983						
C	ECN 5933 L.O. 9-1-76	9/1/76																			
														UNLESS OTHERWISE SPECIFIED TOLERANCES .XX ± .XX ± ANGLES DO NOT SCALE DRAWING INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5 DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH COUNTERBORE AND SPOTFACE FILLET RADI TO BE .50 MAXIMUM REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .50R ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1 STANDARD HOLE TOLERANCE PER AND 3897			DRAWN C. KING 4-11-75 CHECK [Signature] 6-2-75 PROD. ENGR [Signature] 6-2-75 OTHER APPROVALS [Signature] THIRD ANGLE PROJECTION INCH 25.4			CAELUS MEMORIES INC. SAN JOSE, CALIFORNIA TITLE: P.C. BOARD SCHEM TERMINATOR SIZE: THE INFORMATION ON THIS DRAWING MAY NOT BE DISSEMINATED WITHOUT AUTHORIZATION OF CAELUS MEMORIES INC. SCALE: 1 OF 1 SHT: 1 OF 1 E302983 C	

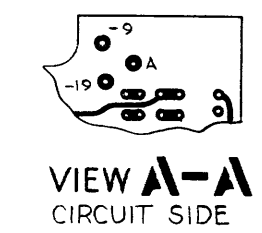
Figure 8-35. Termination Board Schematic



DASH NO.	JUMPER	
-009	DRIVE +5V	A-9
-019	CONTROLLER +5V	A-19

REV
E
302983

- NOTES: UNLESS OTHERWISE SPECIFIED
- 1 PERMANENT MARK PART NO 302983 WITH DASH NO & LATEST REV LEVEL ON SURFACE AS SHOWN USING .12 HIGH CHARACTERS; USING INK BLACK PER CAELUS SPEC 02-000761-001
 - 2 REF DOCUMENTS: SEE SCH DWG E302983
 - 3 -009 VERSION SHOWN.
 - 4 ADD 510pf CAPACITOR FROM; PIN 12 TO PIN 18
PIN 13 TO PIN 19
PIN 14 TO PIN 20
PIN 15 TO PIN 21
PIN 16 TO PIN 22



ITEM	QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	REMARKS
2	2	7	25-000672-001	SCREW LOCK, MALE
42	42	6	17-000052-052	RESISTOR 330Ω, 1/4W, 5% R1-21 R64-84
42	42	5	17-000052-041	RESISTOR 110Ω, 1/4W, 5% R22-63
A	A	4	04-000349-005	WIRE, BUSS BAR (22 GA)
5	5	3	13-000043-049	CAP 510pf 5% C1,2,3,4,5, 4
1	1	2	41-001116 -001	CONNECTOR, CANNON DDC-50PV
1	1	1	302574-001	PRINTED CIRCUIT BOARD

REV	ECN	DATE	APPR
A	ECN 5619	6-2-75	WAB/eng
B	ECN 5677	8-7-75	WAB/eng
C	ECN 5750	11/1/75	DC
D	ECN 5748	10-23-75	DC
E	ECN 5933	10-23-75	DC

PART NO.	NEXT ASSY	USED ON
302574	30344	206/306

UNLESS OTHERWISE SPECIFIED

TOLERANCES
XX ± ~
ANGLES ~

DO NOT SCALE DRAWING

INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5

DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH

COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM

REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R

ROUGHNESS OF MACHINED SURFACES 125/PER USAS B46.1

STANDARD HOLE TOLERANCE PER AND 10387

DRAWN D.C. 4-30-75

CHECK M.H. + Fong 6-2-75

PROJ. ENGR M.H. + Fong 6-2-75

PROD. ENGR M.H. + Fong 6-2-75

OTHER APPROVALS MFG ENGR M.H. + Fong 6-2-75

QA

THIRD ANGLE PROJECTION

INCH
mm

CÆLUS MEMORIES INC.
SAN JOSE, CALIFORNIA

TITLE: P.C. BOARD ASSY
TERMINATION BOARD

SIZE: THE INFORMATION ON THIS DRAWING MAY NOT BE DISSEMINATED WITHOUT AUTHORIZATION OF CAELUS MEMORIES INC.

SCALE 2/1

SHT 1 OF 1

NO 302983

REV E

Figure 8-36. Termination Board Assembly

REV		DATE	APPRV																	301174			
A		12/3	JH																	301174			
B		11/62	71																	301174			
C		1/30	PH																	301174			
D		1/22	PH																	301174			
UNLESS OTHERWISE SPECIFIED:				DRAWN DATE				TITLE				SCALE				REV							
TOLERANCES				301174				ASSEMBLY				2/1				301174							
ANGLES				301174				READ/WRITE AMP				SHT 1 OF 2				S							
MACHINED SURF.				301174																			
APPLICABLE SPECIFICATIONS REF:				301174																			
NEXT ASM				301100																			
SHT 1 OF 2																							

REV	DATE	APPRV	QTY	ITEM	PART NO.	DESCRIPTION	REF DESIGNATION	REMARKS
1	1	1	64					
1	1	1	63		13-000043-036	CAP 180PF 500V	CI2	
2	2	2	62		53-000054-012	RES 150 1/4W 2%	R55, R56	
27	27	27	61		35-000162-001	POST MOD II		
A	A	A	60		04-000429-001	WIRE, WIRE WRAP		UL STYLE 1422
1	1	1	59		80-000153-001	XFMR IZPHA	T2	
1	1	1	58		80-000153-002	XFMR IZSHA	T1	
2	2	2	57		80-000150-004	.33 μH. COIL	L1, L2	
1	1	1	56		40-000161-001	DL 150NS	DL1	

REV	DATE	APPRV	QTY	ITEM	PART NO.	DESCRIPTION	REF DESIGNATION	REMARKS
26	26	26	55		12-000028-001	DIO IN4448	CR THRU 19, 24 THRU 30	
2	2	2	54		12-000270-001	DIO IN753A 6.2V	CR 20, 21	
2	2	2	53		12-000618-001	DIO IN5230B 4.7V	CR 22, 23	
9	9	9	52		13-000521-001	CAP .01MF 100V	C18, 20, 28, 30, 32, 35 THRU 38	
13	13	13	51		13-000037-033	2.2MF 20V	C1, 7, 8, 10, 13, 14, 15, 17, 19, 21, 24, 29, 31	
2	2	2	50		13-000041-013	.022MF 80V	C11, 23	
4	4	4	49		13-000034-019	6.8MF 6V	C25, 27, 33, 34	
6	6	6	47		13-000043-054	820PF 500V	C2, 3, 4, 5, 9	
1	1	1	46		13-000043-051	620PF 500V	C16	
1	2	1	45		13-000043-030	CAP 100PF 500V	C26 C39 - C19 ONLY	
1	1	1	44		14-000045-004	POT 100Ω	R21	
2	2	2	43		53-000054-011	RES 41K 1/4W 2%	R77, 78	
2	2	2	42		16-000307-056	270.2.5W 5%	R 31, R20	
1	1	1	41		16-000307-145	240.2.5W 5%	R35	
1	1	1	40		17-000052-026	27Ω 1/4W 5%	R53	
2	2	2	39		17-000052-023	22Ω	R1, 4	
2	2	2	38		17-000052-017	12Ω	R36, 39	
3	3	3	37		17-000052-015	10Ω 1/4W 5%	R25, 26, 30	
1	1	1	36		53-000054-052	7500Ω 1/4W 2%	R65	
2	2	2	35		53-000054-051	6800Ω	R27, R76	
1	1	1	34		53-000054-050	6200Ω	R46	
3	3	3	33		53-000054-042	3K	R19, R74, R75	
1	1	1	32		53-000054-046	5100Ω	R 71	
4	4	4	31		53-000054-047	4700Ω	R14, 17, 13, 34	
1	1	1	30		53-000054-043	3300Ω	R28	
9	9	9	29		53-000054-040	2400Ω	R5 THRU 12, 70	
5	2	5	28		53-000054-039	2K	R15, 18, 67, 68, 69	
2	2	2	27		53-000054-036	1500Ω	R 42, 43	
2	2	2	26		53-000054-034	RES 1200Ω 1/4W 2%	R57, 60	

REV	DATE	APPRV	QTY	ITEM	PART NO.	DESCRIPTION	REF DESIGNATION	REMARKS
1	1	1	25		53-000054-019	RES 300Ω 1/4W 2%	R73	
3	3	3	24		53-000054-032	RES 1K 1/4W 2%	R2, 3, 29	
4	4	4	22		53-000054-030	820Ω	R47, 48, 49, 50	
1	1	1	21		53-000054-028	680Ω	R54	
2	2	2	20		53-000054-027	620Ω	R44, 45	
2	2	2	19		53-000054-023	430Ω	R63, 64	
9	9	9	18		53-000054-001	51Ω	R22, 23, 32, 33, 37, 38, 51, 52, 66	
1	1	1	17		53-000054-010	120Ω	R58	
4	4	4	16		53-000054-008	100Ω	R40, 41, 61, 62	
1	1	1	15		53-000054-005	75Ω	R59	
1	1	1	14		53-000054-048	RES 5100Ω 1/4W 2%	R72	
1	1	1	13		53-000054-029	RES 750Ω 1/4W 2%	R24	
4	4	4	12		11-000301-001	XSTR 2N2369A	Q16, 17, 5, 7	
7	7	7	11		11-000275-001	XSTR 2N2907A	Q6, 8, 9, 10, 11, 14, 15	
6	6	6	10		11-000060-001	XSTR 2N2222A	Q1, 2, 3, 4, 12, 13	
1	1	1	9		11-000060-001	XSTR 2N2222A	Q18	
1	1	1	7		10-000274-002	IC 733	IC 4	
1	1	1	6		10-000517-002	74107	IC 3	
2	2	2	5		10-000621-001	1035	IC 5, 6	
2	2	2	4		10-000011-001	7402	IC 1, 2	
1	1	1	3		10-000009-001	IC 7400	IC 7	
1	1	1	1		301172-001	R/W AMPLIFIER P.C. BOARD		

Figure 8-37. 100 TPI, 1,500 rpm Read/Write Amplifier Assembly, Sheet 1 of 2

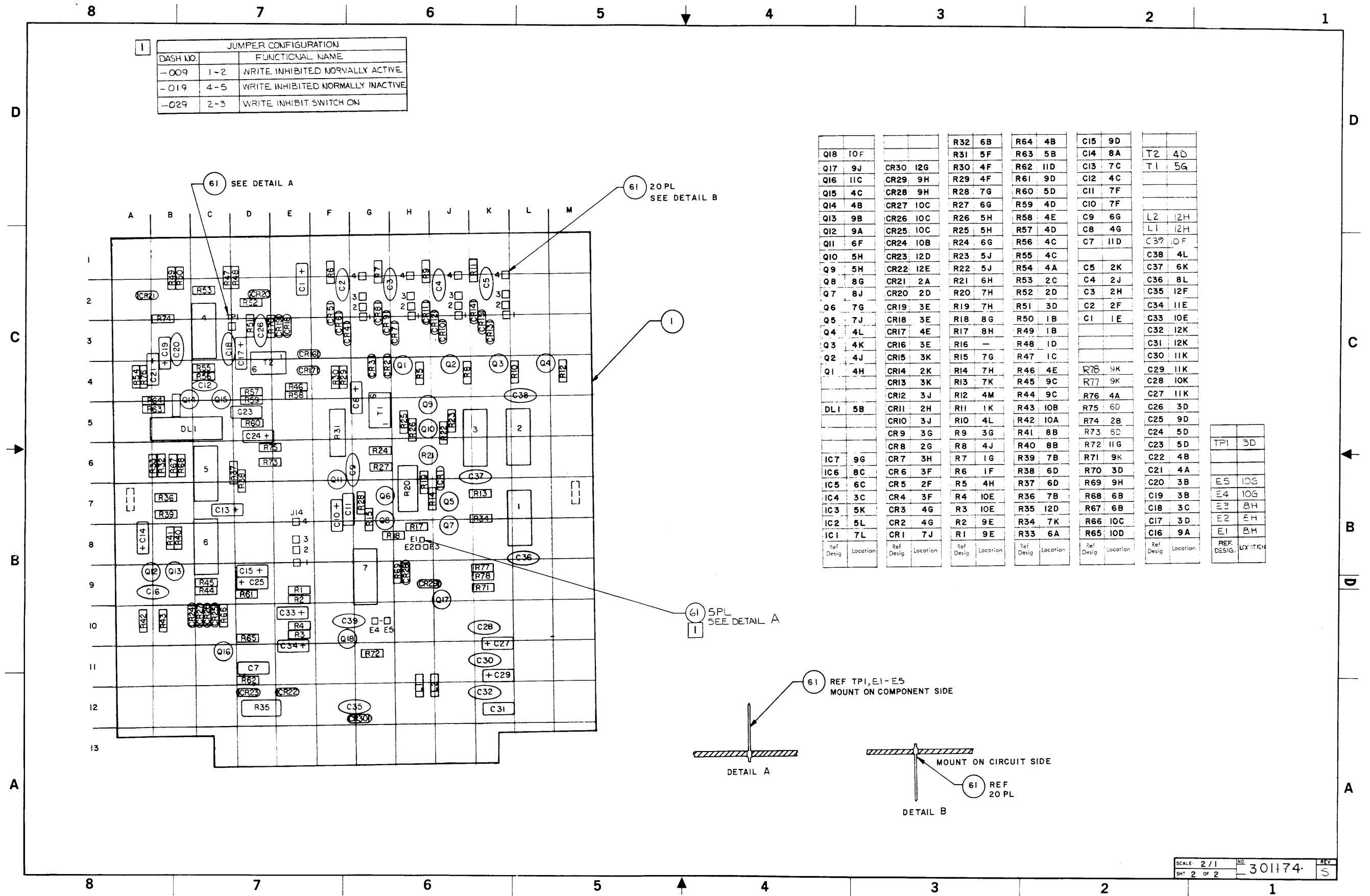


Figure 8-38. 100 TPI, 1,500 rpm Read/Write Amplifier Assembly, Sheet 2 of 2

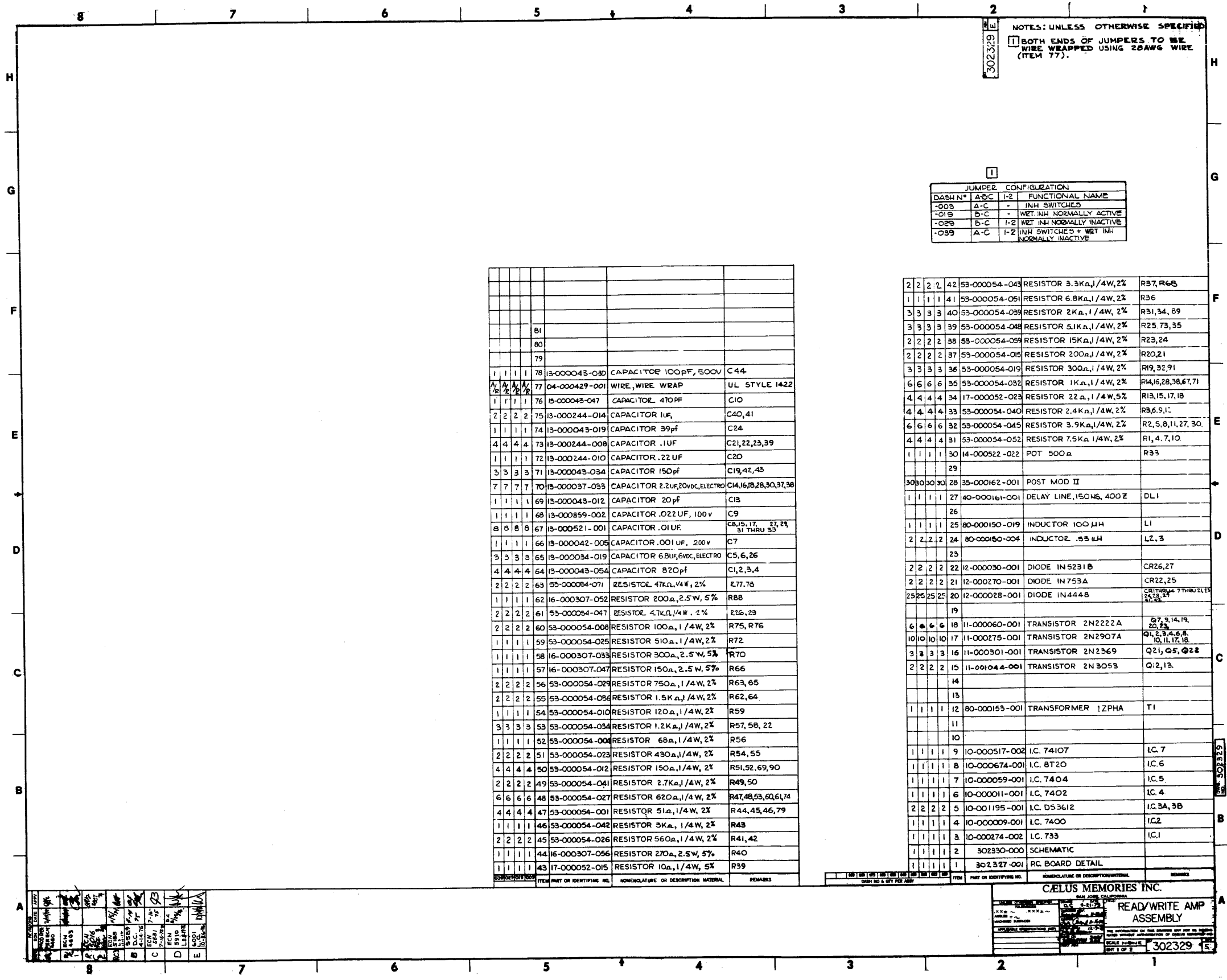
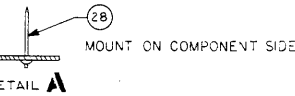
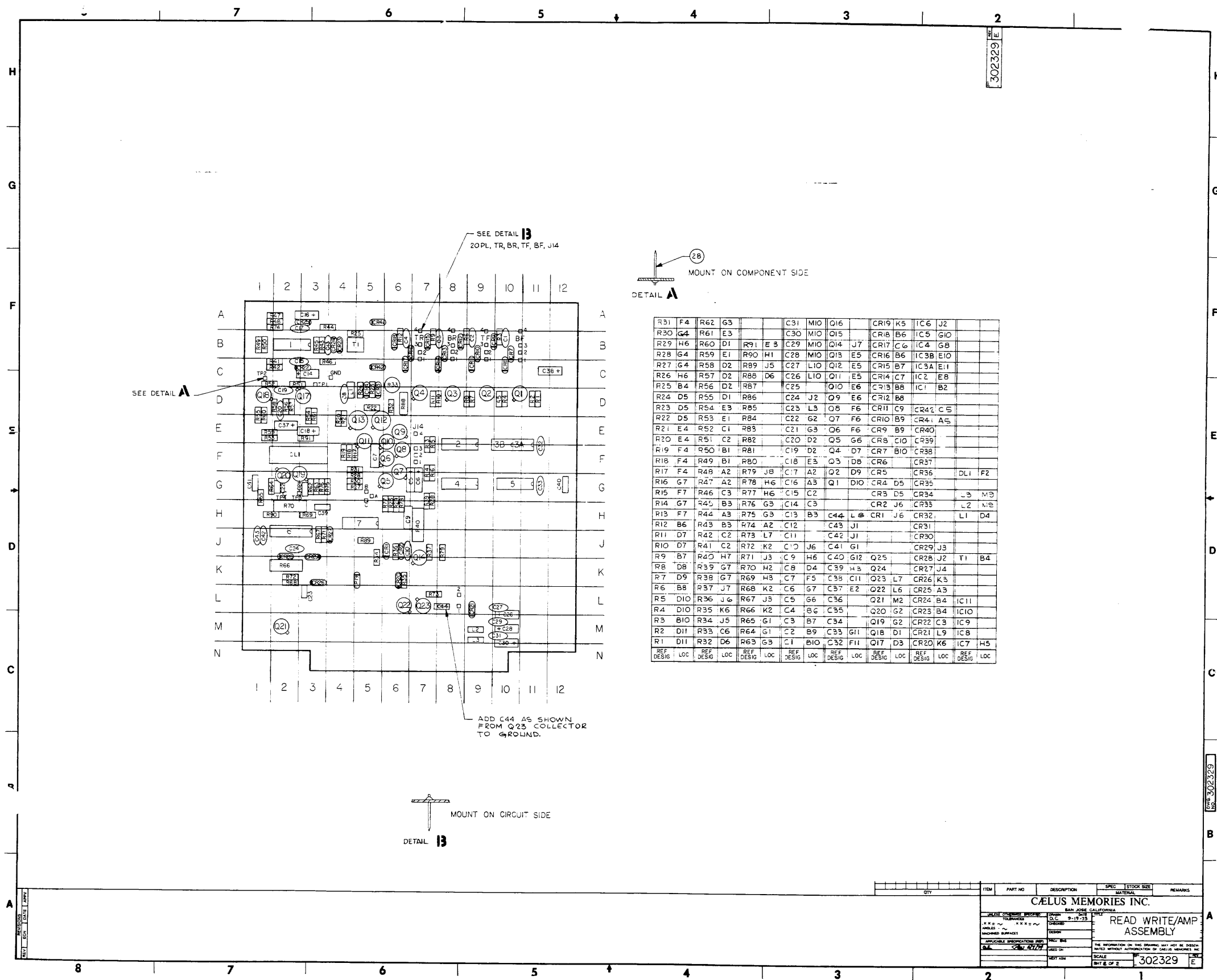
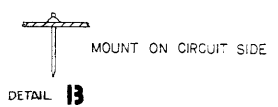


Figure 8-39. 100 TPI, 2,400 rpm Read/Write Amplifier Assembly, Sheet 1 of 2



R31	F4	R62	G3			C31	M10	Q16		CR19	K5	IC6	J2		
R30	G4	R61	E3			C30	M10	Q15		CR18	B6	IC5	G10		
R29	H6	R60	D1			R91	E3	C29	M10	Q14	J7	CR17	C6	IC4	G8
R28	G4	R59	E1			R90	H1	C28	M10	Q13	E5	CR16	B6	IC3B	E10
R27	G4	R58	D2			R89	J5	C27	L10	Q12	E5	CR15	B7	IC3A	E11
R26	H6	R57	D2			R88	D6	C26	L10	Q11	E5	CR14	C7	IC2	E8
R25	B4	R56	D2			R87		C25		Q10	E6	CR13	B8	IC1	B2
R24	D5	R55	D1			R86		C24	J2	Q9	E6	CR12	B8		
R23	D5	R54	E3			R85		C23	L3	Q8	F6	CR11	C9	CR42	C5
R22	D5	R53	E1			R84		C22	G2	Q7	F6	CR10	B9	CR41	A5
R21	E4	R52	C1			R83		C21	G3	Q6	F6	CR9	B9	CR40	
R20	E4	R51	C2			R82		C20	D2	Q5	G6	CR8	C10	CR39	
R19	F4	R50	B1			R81		C19	D2	Q4	D7	CR7	B10	CR38	
R18	F4	R49	B1			R80		C18	E3	Q3	D8	CR6		CR37	
R17	F4	R48	A2			R79	J8	C17	A2	Q2	D9	CR5		CR36	DL1 F2
R16	G7	R47	A2			R78	H6	C16	A3	Q1	D10	CR4	D5	CR35	
R15	F7	R46	C3			R77	H6	C15	C2			CR3	D5	CR34	L3 M3
R14	G7	R45	B3			R76	G3	C14	C3			CR2	J6	CR33	L2 M2
R13	F7	R44	A3			R75	G3	C13	B3	C44	L3	CR1	J6	CR32	L1 D4
R12	B6	R43	B3			R74	A2	C12		C43	J1			CR31	
R11	D7	R42	C2			R73	L7	C11		C42	J1			CR30	
R10	D7	R41	C2			R72	K2	C10	J6	C41	G1			CR29	J3
R9	B7	R40	H7			R71	J3	C9	H6	C40	G12	Q25		CR28	J2 T1 B4
R8	D8	R39	G7			R70	H2	C8	D4	C39	H3	Q24		CR27	J4
R7	D9	R38	G7			R69	H3	C7	F5	C38	C11	Q23	L7	CR26	K3
R6	B8	R37	J7			R68	K2	C6	G7	C37	E2	Q22	L6	CR25	A3
R5	D10	R36	J6			R67	J3	C5	G6	C36		Q21	M2	CR24	B4 IC11
R4	D10	R35	K6			R66	K2	C4	B6	C35		Q20	G2	CR23	B4 IC10
R3	B10	R34	J5			R65	G1	C3	B7	C34		Q19	G2	CR22	C3 IC9
R2	D11	R33	C6			R64	G1	C2	B9	C33	G11	Q18	D1	CR21	L9 IC8
R1	D11	R32	D6			R63	G3	C1	B10	C32	F11	Q17	D3	CR20	K6 IC7 H5
REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC

ADD C44 AS SHOWN FROM Q23 COLLECTOR TO GROUND.



302329

302329

ITEM	PART NO	DESCRIPTION	QTY	STOCK SIZE	REMARKS
CÆLUS MEMORIES INC.					
SAN JOSE CALIFORNIA					
DATE: 9-19-75					
READ WRITE/AMP ASSEMBLY					
SCALE: 302329					

Figure 8-40. 100 TPI, 2,400 rpm Read/Write Amplifier Assembly, Sheet 2 of 2