

Burroughs Corporation





BURROUGHS D 4 MODULAR INTEGRATED CIRCUIT MILITARY COMPUTER

CHARTS 1 THROUGH 11 — INTRODUCTION

CHARTS 12 THROUGH 27 — LOGIC/SYSTEM

CHARTS 28 THROUGH 37 — CIRCUITS

CHARTS 38 THROUGH 51 — PACKAGING

CHARTS 52 THROUGH 54 — SUMMARY

Burroughs Corporation-

1. FUNCTIONAL MODULARITY -MATRIX ORGANIZATION

D825 - 1962

D830 - 1964

B8500-1966

- 2. ADVANCED MICROCIRCUIT TECHNIQUES*, AND
- 3. ADVANCED MAULER COMPUTER DESIGN**
- * FEB. '64 COMPLETION OF 12-BIT ARITHMETIC UNIT (700 I.C.'s) LIFE-TEST CONTINUING.
- ** TO IMPROVE T.E.C. (REDUCE IN SIZE, INCREASE MTBF)

COMBINED TO PRODUCE D84*

FEATURING

PHYSICALLY INDEPENDENT FUNCTIONAL MODULES

ALL LOGIC IMPLEMENTED WITH MONOLITHIC

INTEGRATED CIRCUITS

FOR

FLEXIBILITY IN SYSTEMS CONFIGURATIONS

GROWTH POTENTIAL BUILT-IN

COMPACT

RELIABILITY

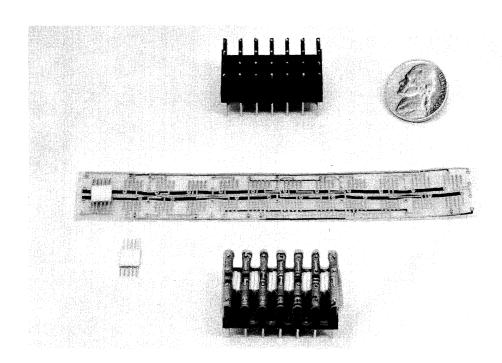
LIGHT-WEIGHT

LOW POWER CONSUMPTION

PROTOTYPE (OPERATIONAL JANUARY 65) DIFFERS FROM PRODUCTION D84

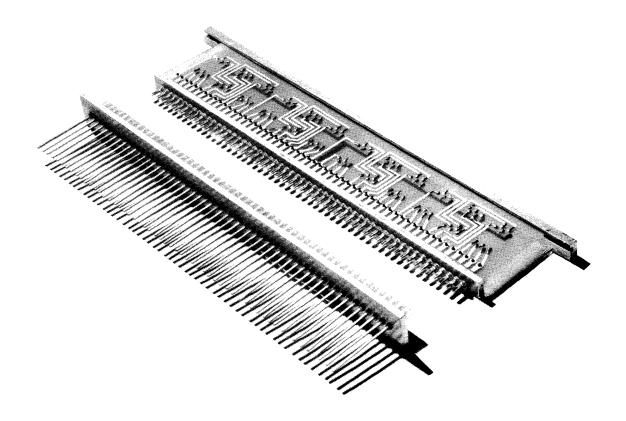
- (1) PACKAGING MORE COMPACT-100% FLATPACK UTILIZATION/LOGISTICAL DISADVANTAGE, AND
- (2) INSTRUCTION REPERTOIRE 35 BASIC COMMANDS VS. 47

T & D C. N. M. - "3-D"



OVER 100 TYPES -- ALL FLATPACKS USED:LINE MAINTENANCE AT FUNCTIONAL MODULE LEVEL

D84 C. N. M. -"2-D"



35 MAX. TYPES(ONLY 23 IN LOGIC*): AVERAGE FLATPACK UTILIZATION

IO TO 11 PER CNM: LINE, MAINTENANCE AT CNM (THROWAWAY) LEVEL—

MADE PRACTICAL VIA DIAGNOSTICS PROGRAM

MAJOR ADVANTAGES

- I. LOW COST
 - DEVELOPMENT COMPLETE
 - ONE TIME CHARGES RESTRICTED TO DESIGN OF SPECIAL INTERFACES IN THE I/O MODULE.
- 2. MODULAR EXPANSIBILITY THROUGH TO MULTIPROCESSING FOR MORE THROUGHPUT AND/OR GRACEFUL DEGRADATION.
- 3. MULTIPLE INDEXING
 - MULTI-LEVEL INDIRECT ADDRESSING
 - VERSATILE INSTRUCTION REPERTOIRE
 - LEADING TO REDUCED MEMORY REQUIREMENTS
 AND / OR REDUCED RUNNING TIME.

MAJOR ADVANTAGES CONTINUED

4. AGGRESSIVE INTERRUPT SYSTEM

- PROGRAMMABLE PRIORITIES
- INTERRUPTS MAY BE IGNORED OR STORED
 FOR DEFERRED ACTION 24 MAX, INTERRUPTS

5. FLEXIBILITY OF I/O

- CHANNEL TYPE AND NUMBER TAILORED TO APPLICATION
- PACKAGING FLEXIBILITY TO MAINTAIN LOWEST PRACTICAL
 SIZE FOR SPECIFIED I/O DESIGN-3 STANDARD PACKAGES

6. EXTENDED PRODUCT LIFE

- MODULAR GROWTH-IN MEMORY, I/O, & CENTRAL DATA PROCESSORS(MULTI-PROCESSING)
- HIGHER SPEED CIRCUITS FOR SYSTEM SPEED-UP WHEN USED WITH THIN-FILM MEMORIES (8:1 BY LAST QUARTER '67 DELIVERIES) PROGRAM COMPATIBLE WITH PRESENT SYSTEM.

MAJOR ADVANTAGES CONTINUED

7. MAINTENANCE

- NO PREVENTIVE MAINTENANCE
- EMERGENCY MAINTENANCE PHILOSOPHY SELECTED BY CUSTOMER
 - 1. ON-LINE, WHILE SYSTEM IS OPERATIVE (MULTI-PROCESSING) NO DOWNTIME
 - 2. AT FUNCTIONAL MODULE LEVEL- < 5 MIN. DOWNTIME
 - 3. AT CIRCUIT NETWORK MODULE LEVEL 30 MIN. DOWNTIME
 - 4. AT FLATPACK LEVEL

D84 - AVERAGE INSTRUCTION EXECUTE TIME

- I. "COMMAND AND CONTROL MIX" COMMUNICATIONS OF THE ACM MAY '64
 - A) WITH 4 μ s cycle time memory-10 μ s
 - B) WITH 3 μ S CYCLE TIME MEMORY 8 μ S
 - VS. $360/40 14\mu$ S $360/50 5\mu$ S
- 2. "GIBSON MIX" SCIENTIFIC CALCULATIONS
 - A) WITH 4 μ S CYCLE TIME MEMORY-19 μ S
 - B) WITH 3 μ S CYCLE TIME MEMORY-15 μ S
 - vs. $360/40 30 \mu s$ $360/50 - 7\frac{1}{2}\mu s$

SOFTWARE-INITIAL DELIVERIES (LATE 65 THRU 1st. HALF OF 66)

1 ASSEMBLER PROGRAM-FORTRAN IV FOR 7044 AND 7094

- SYMBOLIC MNEMONICS SPECIFY OPERATIONS
- SYMBOLIC TAGS SPECIFY MEMORY REFERENCES
- OBJECT PROGRAM PRODUCED (CARD DECK) FOR D84
- PROGRAM DECK PRODUCED FOR INPUT TO SIMULATOR

2. SIMULATOR PROGRAM - FORTRAN IV FOR 7044 AND 7094

- DEBUG OBJECT PROGRAM
- MEASURES PROGRAM RUNNING TIME

SOFTWARE-INITIAL DELIVERIES (LATE 65 THRU 1st. HALF OF 66) CONTINUED

3. SUBROUTINES (FOR CALL-UP BY THE ASSEMBLER)

- SQUARE ROOT
- TRIGONOMETRIC FUNCTIONS
- INVERSE TRIGONOMETRIC FUNCTIONS
- POLYNOMIAL OF DEGREE n
- ASCII TO BINARY CONVERSION
- DOUBLE PRECISION MULTIPLY, DIVIDE

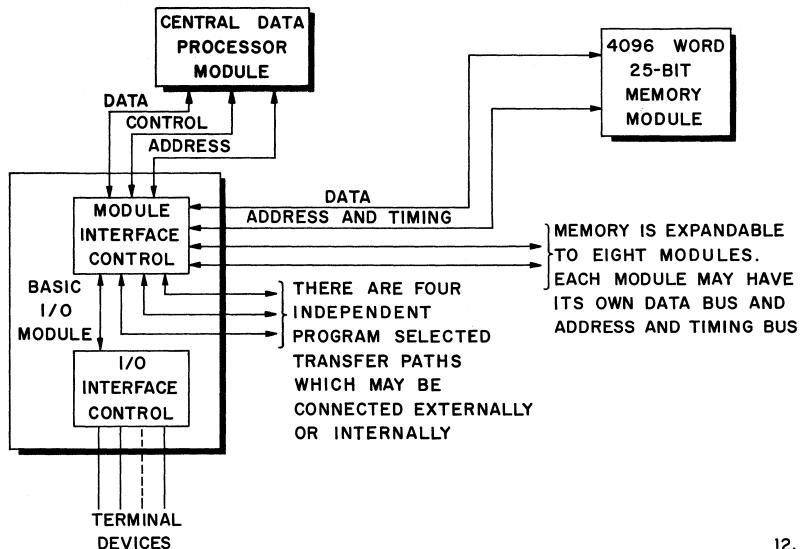
4. DIAGNOSTIC PROGRAM

- MINIMUM OPERATOR INTERVENTION
- LOCATES FAULT TO THROW-AWAY MODULES -9 MIN. MEAN TIME.

SUBROUTINES

MNEMONIC	DESCRIPTION	REQUIRED STORAGE	EXECUTION TIME (MS)
SIN	SINGLE-PRECISION SIN	93	0.75
cos	SINGLE-PRECISION COS	93	0.75
INTAN	SINGLE-PRECISION TAN -1	154	1.52
INSIN	SINGLE-PRECISION SIN -1	123	2.35
INCOS	SINGLE-PRECISION CON-1	123	2.35
SINCO	DOUBLE-PRECISION SIN OR COS	100	2.856
ARCTAN	DOUBLE-PRECISION TAN-1	167	5.850
ASICO	DOUBLE-PRECISION SIN OR COS-1	130	7.990
DPDIV	DOUBLE-PRECISION DIVIDE	37	0.416
DPMUL	DOUBLE-PRECISION MULTIPLY	33	0.248
SQRT	DOUBLE-PRECISION SQUARE-ROOT	52	1.762
POLNOM	DOUBLE-PRECISION POLYNOMIAL OF DEGREE n	47	(0.188+0.318n) where n = number of terms less one

BASIC D84M COMPUTER SYSTEM CONCEPT



MODULE FUNCTIONS

CENTRAL DATA PROCESSOR:

ARITHMETIC UNIT
INSTRUCTION EXECUTION

INDEXING

PROGRAM SEQUENCING

MEMORY ADDRESSING

MODULE INTERFACE CONTROL:

MEMORY ACCESS CONTROL

DATA ROUTING

PROGRAM INTERRUPTS

START/STOP CONTROLS

BOOTSTRAP CONTROLS

CONSOLE INTERFACE

I/O INTERFACE CONTROL:

TERMINAL DEVICE SELECTION

DATA TRANSFER TIMING

WORD BUFFER

SPECIAL FUNCTIONS

MEMORY:

PROGRAM STORE

DATA STORE

I/O BUFFER

FUNCTIONAL CHARACTERISTICS

OPERATION:

SYNCHRONOUS, PARALLEL

ARITHMETIC:

FRACTIONAL BINARY, FIXED POINT SIGN PLUS 23 BITS MAGNITUDE

OPERATING SPEEDS:

ONE MEGACYCLE CLOCK
EXECUTION OF UP TO 333,000 INSTRUCTIONS/SEC.

COMMAND REPERTOIRE:

47 BASIC COMMANDS
OVER 300 USEFUL VARIATIONS

ADDRESSING:

SINGLE ADDRESS, DIRECT MULTILEVEL INDIRECT

FUNCTIONAL CHARACTERISTICS (CONTINUED)

INDEXING:

INDEX REGISTERS IN MEMORY
NUMBER OF INDEX REGISTERS AND LOCATION PROGRAM DETERMINED

MEMORY:

MODULAR, 4096 WORD BASIC MODULE
EXPANDABLE TO 32768 WORDS (EIGHT MODULES)
ONE MICROSECOND ACCESS TIME
CYCLE TIME DETERMINED BY TYPE OF MEMORY

INPUT / OUTPUT:

MASKABLE INTERRUPTS

BUFFERED AND UNBUFFERED I/O CHANNELS

PROVISIONS FOR SPECIAL I/O FUNCTIONS

EXECUTION TIMES

	EXECUTION TIME FOR			
COMMAND	4μsec.R/R	3μsec.R/R MEMORY	2μsec.R/R	
ADD	8	6	4	
ADD LITERAL	4	4	3	
ADD DOUBLE PRECISION	12	9	6	
MULTIPLY	28	27	25	
DIVIDE	51	50	50	
STORE SINGLE WORD	8	6	4	
STORE DOUBLE WORD	12	9	6	
BRANCH	4	4	3	
TEST (EQUAL, GREATER, LESS)	8	6	4	
TEST (EQUAL, GREATER, LESS) LITERAL	4	4	3	
TEST (EQUAL, GREATER, LESS) BLOCK OF BLOCK SIZE m	16+8(m-1)	12+7(m-i)	10+5(m-1)	

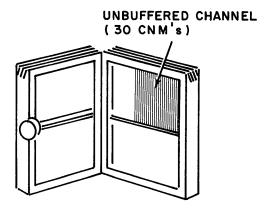
16.

TYPES OF STANDARD I/O

UNBUFFERED CHANNEL:

ADDRESSABLE TERMINAL DEVICES: 127 MAXIMUM DATA RATE:

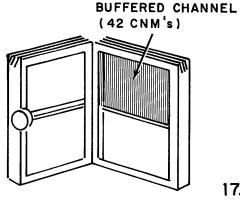
> 4μ SEC MEMORY: 35 700 WORDS/SEC. 2μ SEC MEMORY: 50 000 WORDS/SEC



BUFFERED CHANNEL:

ADDRESSABLE TERMINAL DEVICES: 64 BUFFERED CHANNELS PER CDP: 16 MAXIMUM DATA RATE:

> 4μ SEC MEMORY: 250 000 WORDS/SEC. 2μ SEC MEMORY: 500000 WORDS/SEC



17.

TYPES OF STANDARD I/O CONTINUED

CIRCULATING BUFFERED CHANNEL:

MODIFIED BUFFERED CHANNEL FOR USE WITH DISPLAY

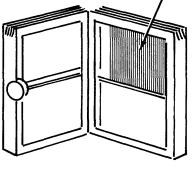
SINGLE WORD BUFFERED CHANNEL

ADDRESSABLE TERMINAL DEVICES 64 CHANNELS PER CDP 4 MAXIMUM DATA RATE:

 4μ SEC MEMORY: 27500 WORDS / SEC. 2μ SEC MEMORY: 41600 WORDS / SEC.

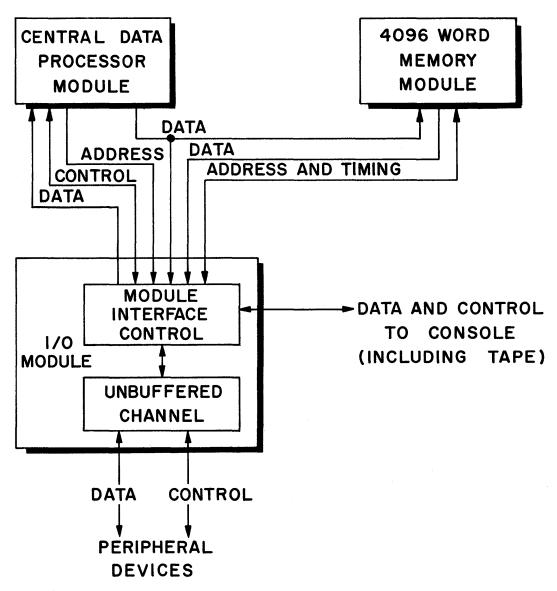


SINGLE WORD

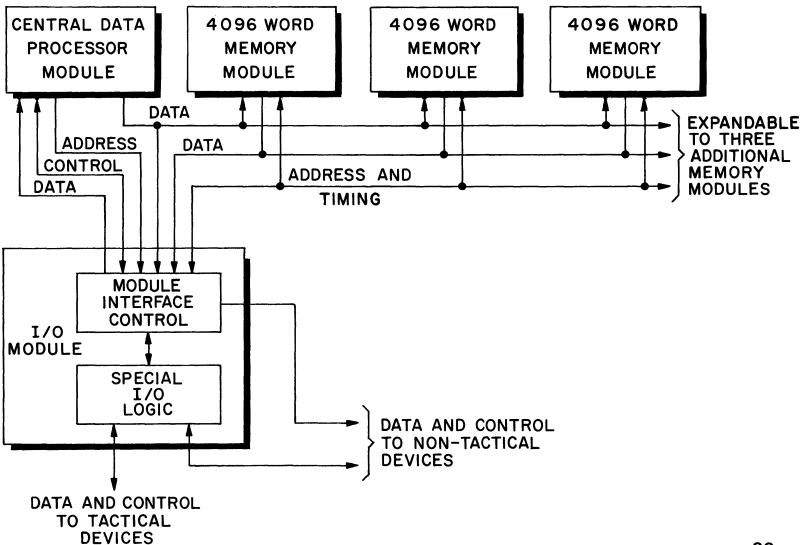


18.

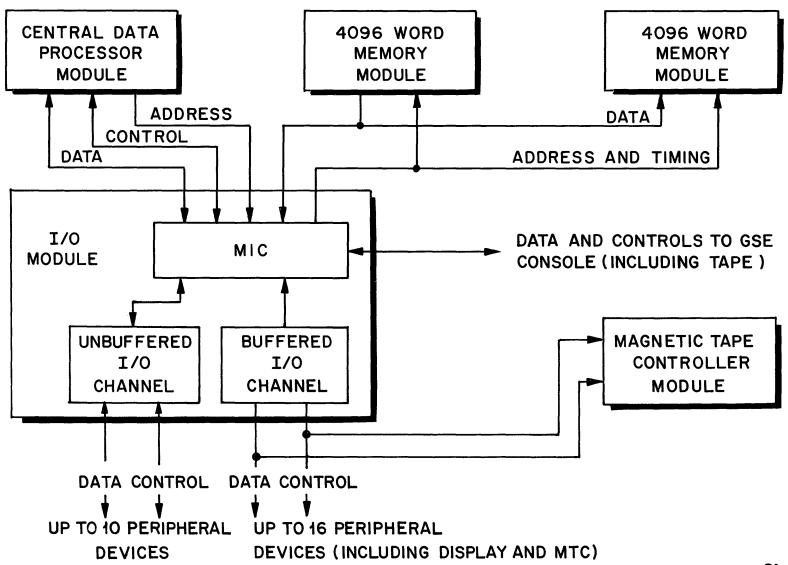
MINIMUM D84M COMPUTER SYSTEM



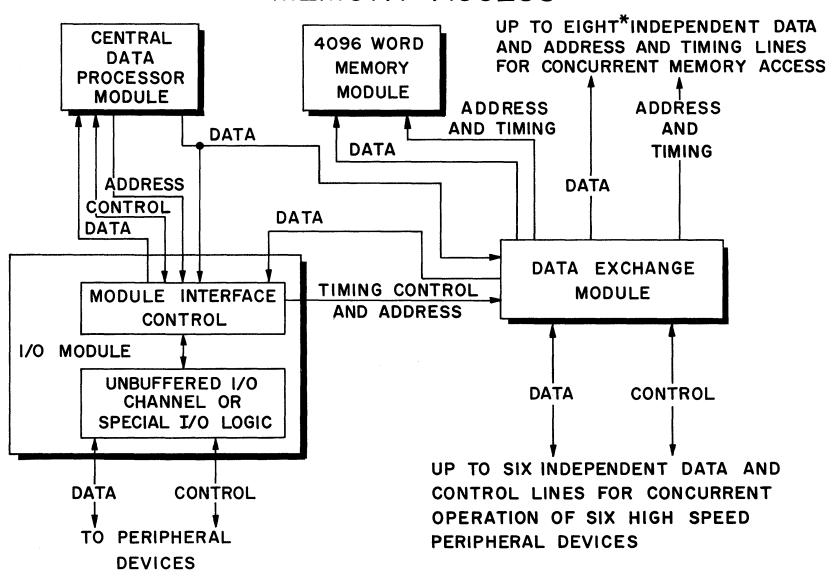
D84M COMPUTER FOR PERSHING IPTS



D84M COMPUTER FOR CLASSIFIED AIRBORNE APPLICATION



D84M COMPUTER WITH CONCURRENT MEMORY ACCESS



D84M ASSEMBLER PROGRAM

LANGUAGE: FORTRAN IX (COMPATIBLE WITH IBM 7044, 7094, 360, GE 625)

FEATURES:

47 BASIC INSTRUCTIONS
OVER 300 MNUMONICS
SOFTWARE LITERALS
LIBRARY SUBROUTINES
27 PSEUDO OPERATIONS

INPUT: CARD DECK

OUTPUTS:

HARD COPY

PAPER TAPE FOR LOADING PROGRAMS INTO D84

- A) MAGNETIC TAPE TO PREPARE PAPER TAPE
- B) CARD DECK TO PREPARE PAPER TAPE

SIMULATOR INPUT PROGRAM

- A) MAGNETIC TAPE
- B) CARD DECK

SUBROUTINE LIBRARY ON MAGNETIC TAPE

STORAGE REQUIREMENTS: 12,000 WORDS

RUNNING TIME: 6-7 MINUTES (AVERAGE)

D84M SIMULATOR PROGRAM

LANGUAGE: FORTRAN IV (COMPATIBLE WITH IBM

7044, 7094, 360, & GE 625)

FEATURES:

SIMULATION OF CDP AND I/O SPECIFIABLE MEMORY CONFIGURATION & CYCLE TIME

DEBUGGING AIDS:

FULL OR PARTIAL TRACE OF PROGRAM FULL OR PARTIAL LISTING OF MEMORY LOADING OF PORTIONS OF SIMULATED MEMORY **DURING SIMULATION**

MONITORING OF ERRORS DURING SIMULATION RUNNING MORE THAN ONE SIMULATION* SIMULATION OF REAL TIME SIMULATION OF INTERRUPTS UNDER OPERATOR CONTROL

D84M DIAGNOSTIC PROGRAM

MANUAL PROCEDURES

POWER - ON
MODULE SELECTION SWITCHES - OFF
DIAGNOSTIC SWITCH - ON
LAMP TEST - CK DRIVER AND LAMPS
LOAD DIAGNOSTIC TAPE
MANUAL CK OF TAPE READER

→ ISOLATION IN THIS PHASE 1.45-3.15 MIN.

STL TAPE CHECK

INPUT CHECK: - INPUT CIRCUITS FROM READER TO MEMORY

NIXIE CHECK: - LIGHT PATERNS AND DECODING CIRCUITS

PARITY CHECK: -PARITY DECODING CIRCUITS

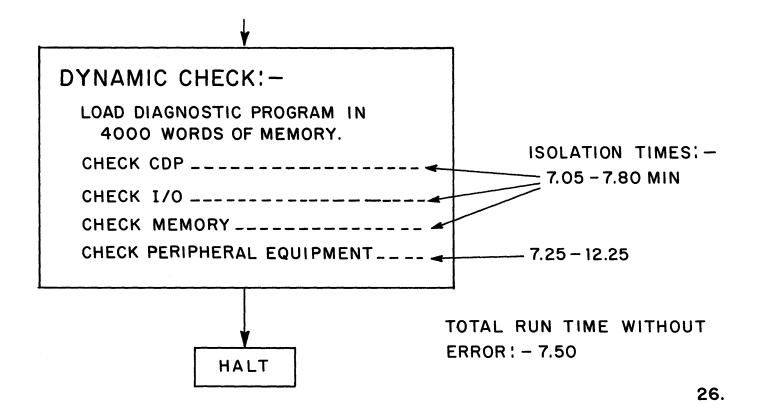
COMPARITOR CHECK: -

INITIAL MEMORY CHECK;

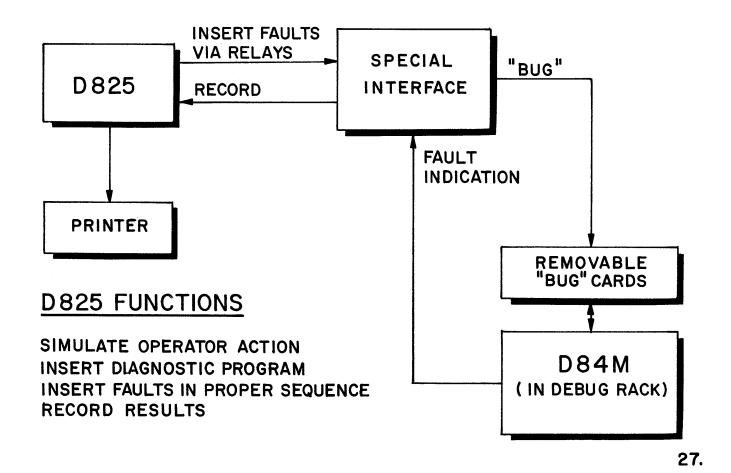
SINGLE INSTRUCTION CHECK: - TIMING CHAIN AND OP REG.

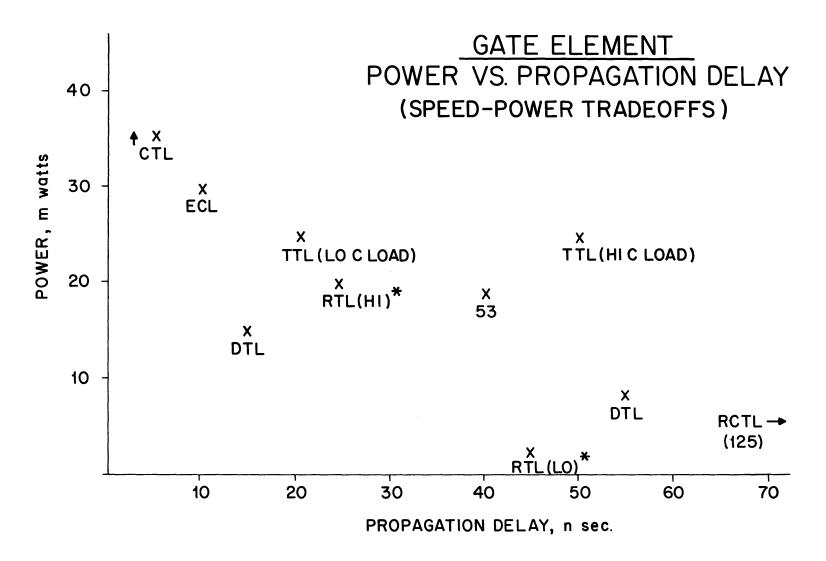
→ ISOLATION IN THIS
PHASE 4.25 - 6.70 MIN.

D84M DIAGNOSTIC PROGRAM-CONTINUED

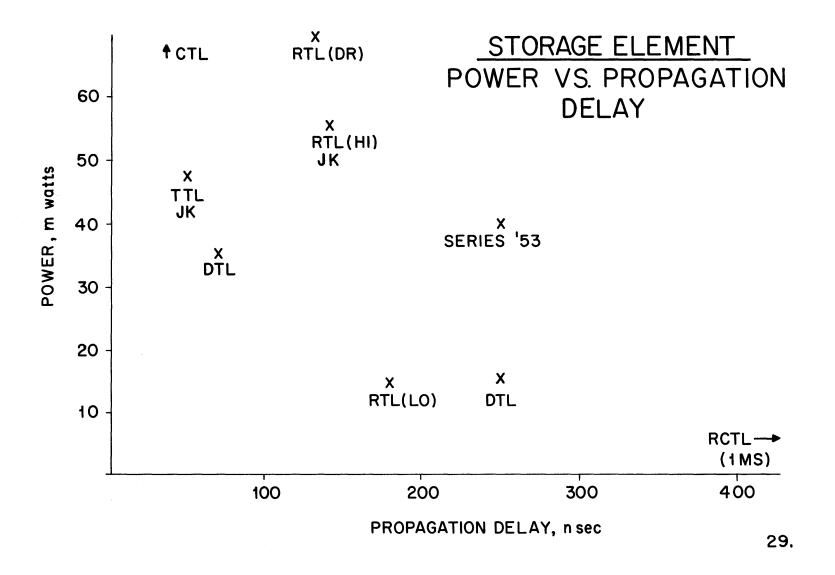


D84 DIAGNOSTIC PROGRAM VALIDATION

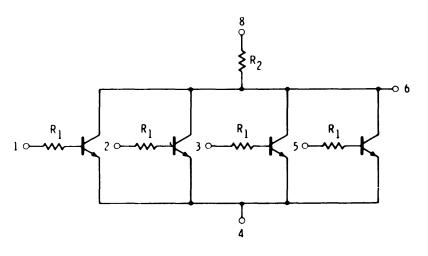




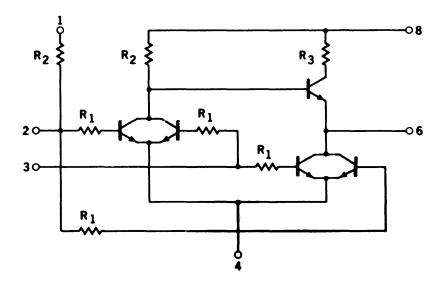
* D84 LOGIC USES >85% LOW-POWER, < 15% HIGH-POWER GATES.



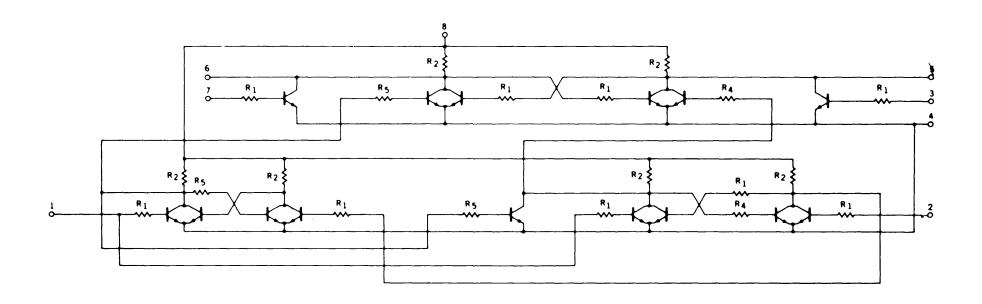
RTL GATE



RTL BUFFER

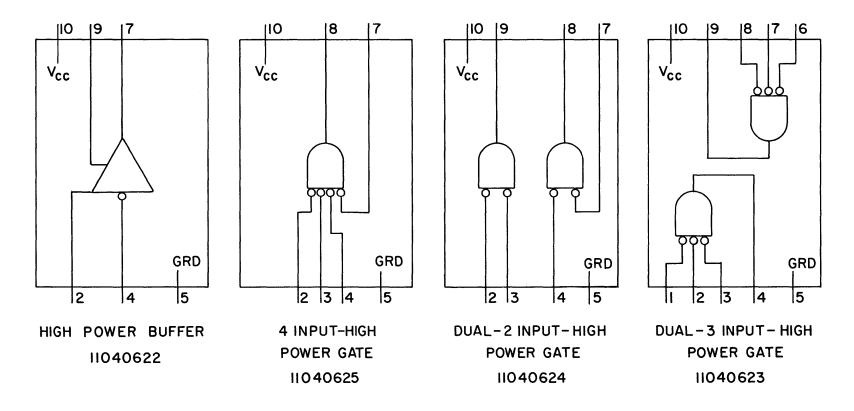


RTL FLIP-FLOP



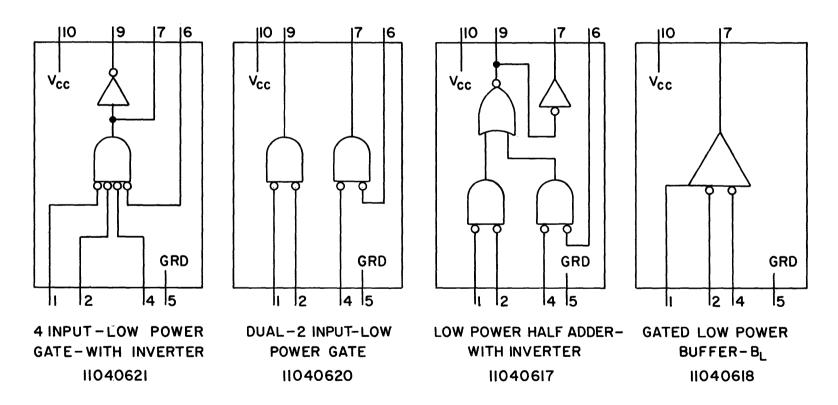
NEGATIVE LOGIC SYMBOLS USED IN D84 FOR FLAT PACKS

HIGH POWER LOGIC



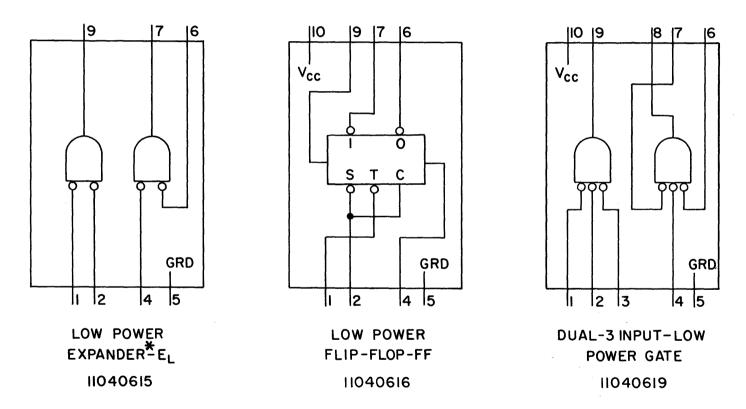
NEGATIVE LOGIC SYMBOLS USED IN D84 FOR FLAT PACKS

LOW POWER LOGIC

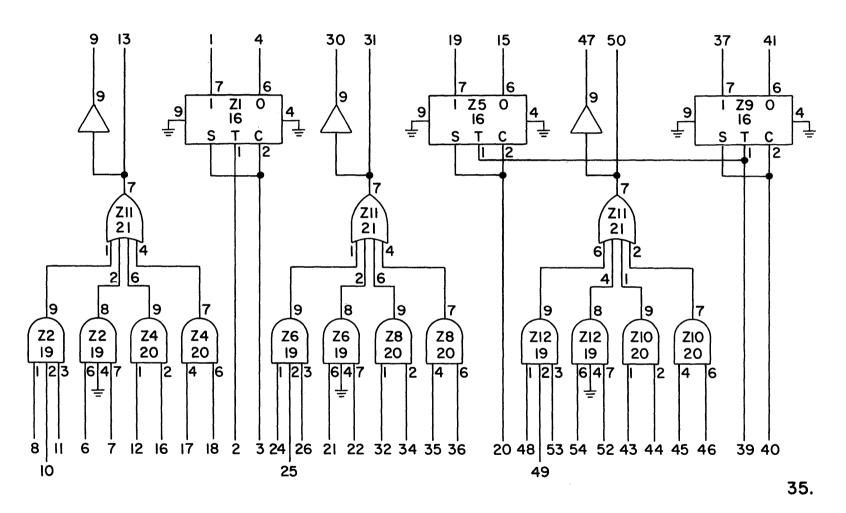


NEGATIVE LOGIC SYMBOLS USED IN D84 FOR FLAT PACKS

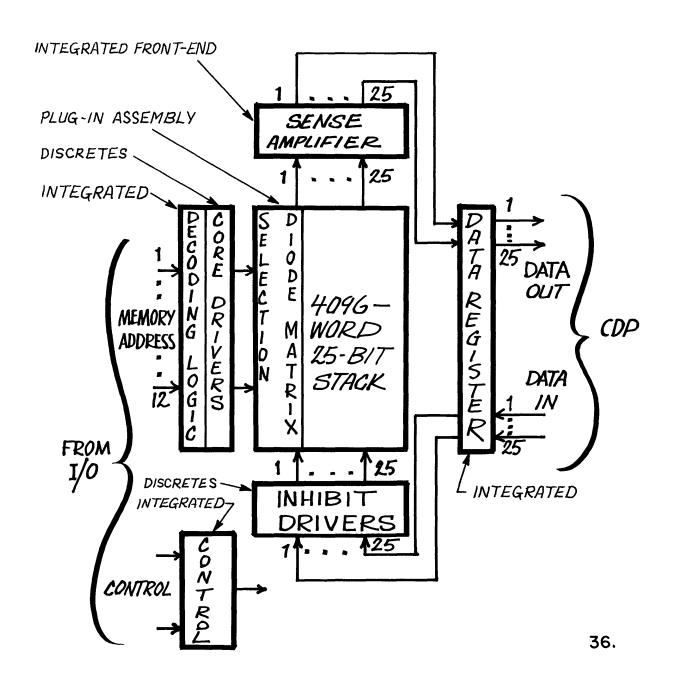
LOW POWER LOGIC (CONTINUED)



REGISTER CIRCUIT NETWORK MODULE



MEMORY SYSTEM BLOCK DIAGRAM



RELIABILITY - D84*

MODULE	FAILURE RATE	MTBF (Hours)
	(FAILURES/10 ⁶ HOURS)	(APPROXIMATE)
POWER SUPPLY	56.58	17,600
CDP	74.49	13,400
I/O	77.0(MIC &1 CHANN	EL) 13,000
MEMORY	269.27	3,700
SYSTEM	477	2,100 HRS.

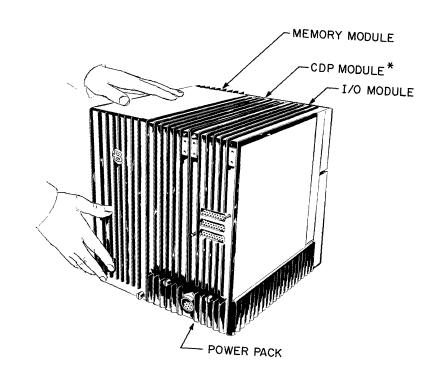
ESTIMATED IMPROVEMENT VIA MINUTEMAN SELECTION CRITERIA FOR DISCRETE COMPONENTS - 2 TO $2\frac{1}{2}$ TIMES.

* FOR BASIC SYSTEM DEFINED BY "GREEN SHEETS", WITH 4K MEMORY.

90% CONFIDENCE LEVEL.

.003% PER 1000 HRS. I.C. FAILURE RATE (0.03/10⁶ HOURS)

D84 PREPRODUCTION PROTOTYPE



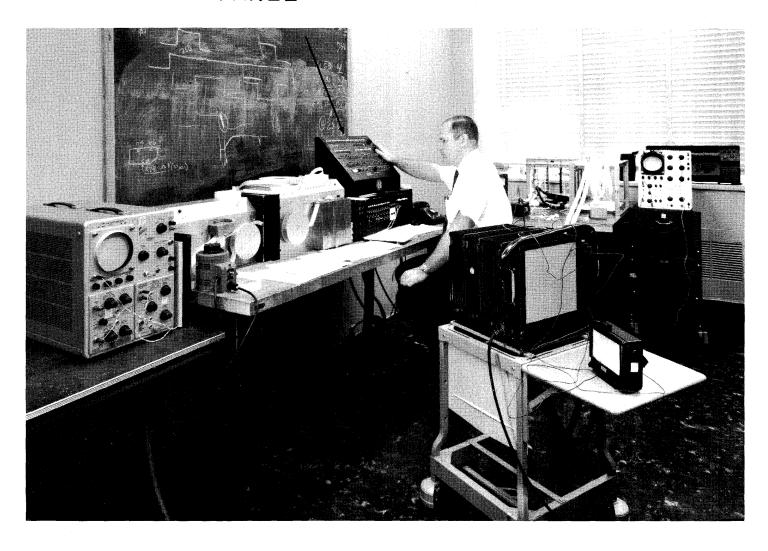
CONTAINS:

1 CDP MODULE
WIDTH: 13.7 IN.
1 I/O MODULE
DEPTH: 15.0 IN.
1 4096x25 BIT
CORE MEMORY
MODULE
POWER: 1.4 CU. FT.
WEIGHT: 100 LB.
POWER: 110 WATTS
COOLING: NONE

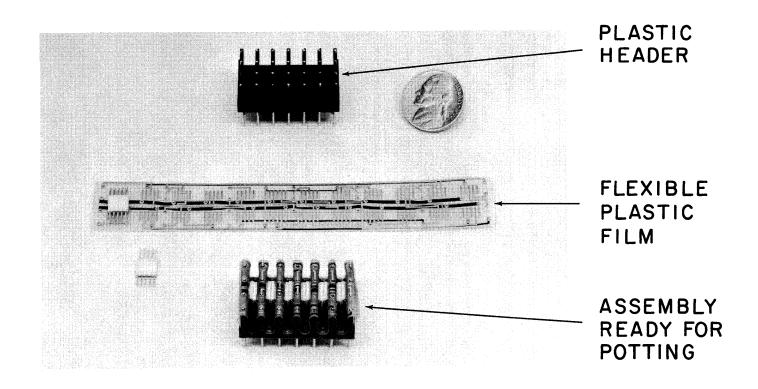
* CONTAINS 4 PLUGGABLE "CARDS", EACH A SANDWICH OF TWO PRINTED CIRCUIT (MOTHER) BOARDS CONTAINING UP TO 48 ("3-D") CIRCUIT NETWORK MODULES.

D84 PROTOTYPE TEST STATION

PROGRAMMER'S PANEL



CIRCUIT NETWORK MODULE FOR D84 PREPRODUCTION PROTOTYPE



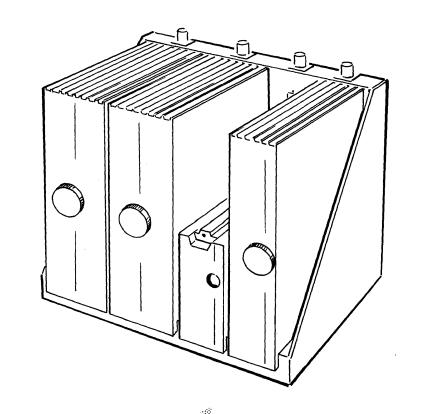
HEIGHT: 0.43 IN.

DEPTH : 0.8 IN. VOLUME: 0.45 CU. IN.

WIDTH: 1.3 IN. WEIGHT: 30 GRAMS

40.

D84M COMPUTER*



HEIGHT: 18.0 IN.

DEPTH : 16.5 IN.

WIDTH: 21.0 IN.

WEIGHT: 150 LB.

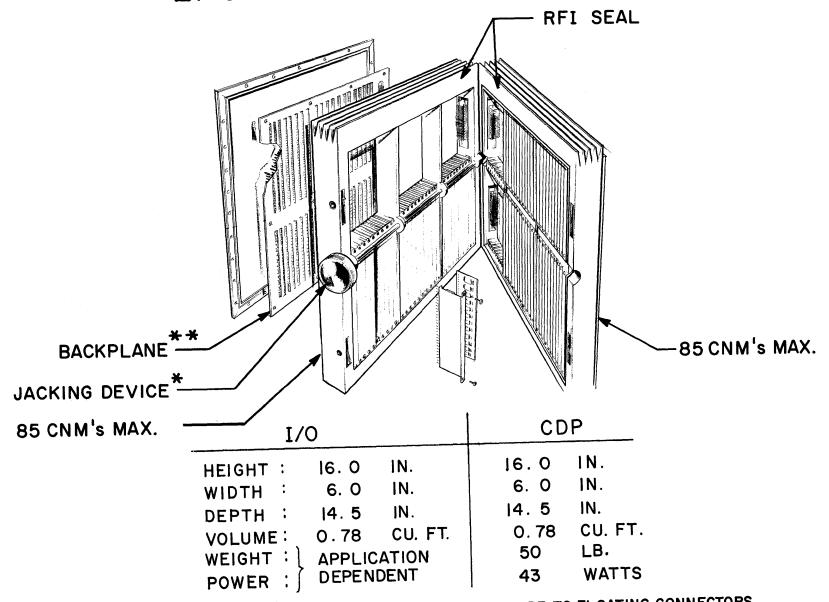
VOLUME: 3.9 CU. FT.

POWER : 160 WATTS

COOLING: NONE

* MINIMUM ("GREEN SHEET") SYSTEM

I/O AND CDP MODULES

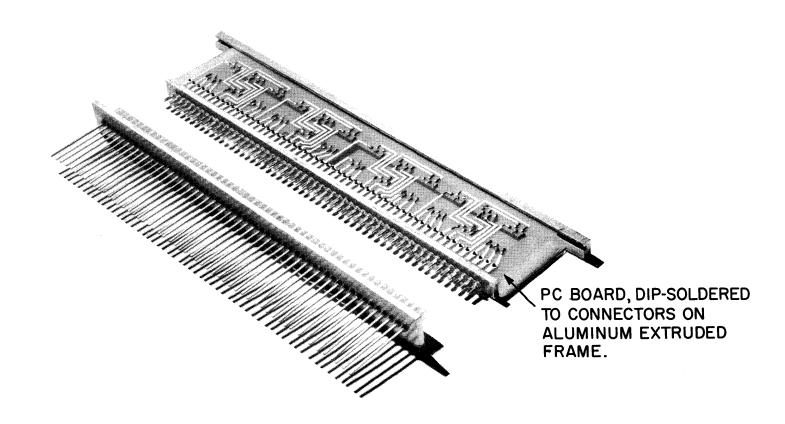


* MOVES MODULE TO MATE WITH SHEAR PINS, AND GUIDE TO FLOATING CONNECTORS.

** MAX. OF 3 WIRES / PIN - SOLDERED OR WIRE-WRAPPED AT CUSTOMER'S OPTION.

42.

D84M CIRCUIT NETWORK MODULE (CNM)

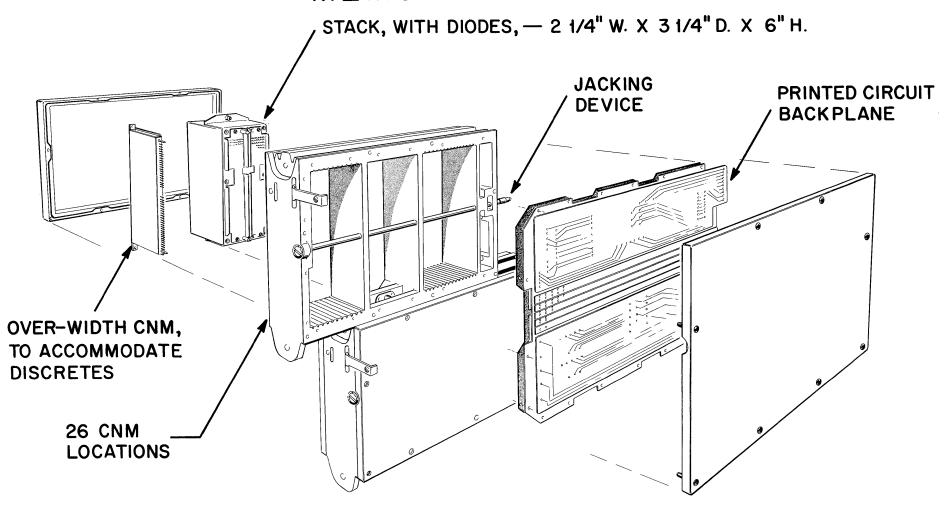


HEIGHT: 0.25 IN.

DEPTH: 6.5 IN. VOLUME: 2.5 CU. IN.

WIDTH: 1.5 IN. WEIGHT: 26 GRAMS

MEMORY MODULE



HEIGHT: 8.0 IN.

WEIGHT: 13 LB.

POWER:

DEPTH : 14.5 IN.

VOLUME: 0.26 CU. FT.

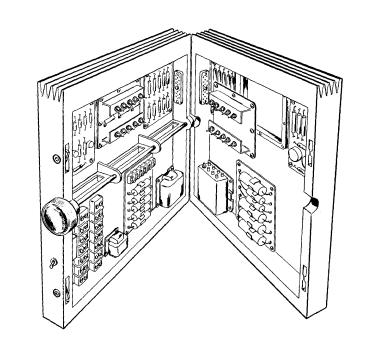
WIDTH : 3.9 IN.

75 WATTS ACTIVE *

12 WATTS STANDBY

^{*} WORST-CASE, WHEN WRITING ALL O's EACH MEMORY CYCLE.

POWER PACK



HEIGHT : 16.0 IN.

WEIGHT: 35 LB.

DEPTH : 14.5 IN.

VOLUME: 0.52 CU. FT.

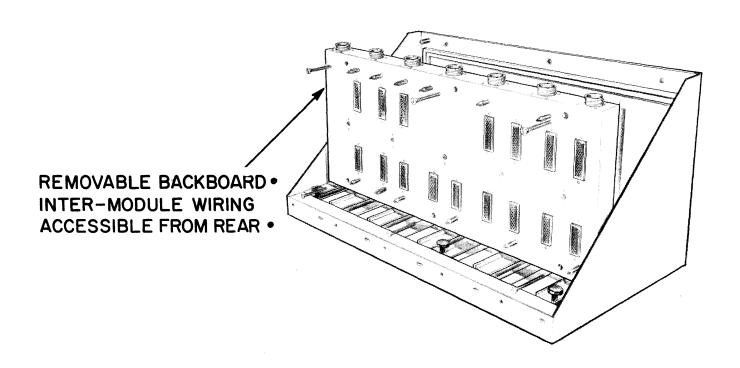
WIDTH: 4.5 IN.

POWER

CAPACITY: 300 WATTS

DISCRETE COMPONENTS, ALL ON REMOVABLE SUB-ASSEMBLIES

MOUNTING BASE ASSEMBLY



HEIGHT: 18.0 IN.

DEPTH: 16.5 IN.

WIDTH*: 30.0 IN.

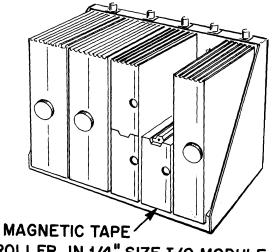
WEIGHT*: 41 LB.

* THIS ASSEMBLY PROVIDES FOR 24K MEMORY

TYPICAL D84M CONFIGURATIONS

CONTAINS:

- 1 CDP MODULE
- 1 I/O MODULE
- 2 4096 x 25 BIT **MEMORY MODULES**
- 1 MAGNETIC TAPE CONTROLLER
- 1 POWER PACK



CONTROLLER, IN 1/4" SIZE I/O MODULE

HEIGHT: 18.0 IN.

WIDTH: 25.0 IN.

DEPTH: 16.5 IN.

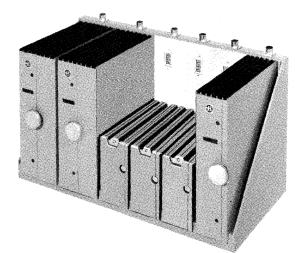
VOLUME: 4.5 CU.FT.

WEIGHT: 210 LB.

POWER: 230 WATTS *

CONTAINS

- 1 CDP MODULE
- 1 I/O MODULE
- 3 4096 x 25 BIT MEMORY MODULES
- 1 POWER PACK PROVISIONS FOR **EXPANSION TO** 24K MEMORY



HEIGHT: 18.0 IN.

WIDTH: 30.0 IN.

DEPTH: 16.5 IN.

VOLUME: 5.25 CU. FT.

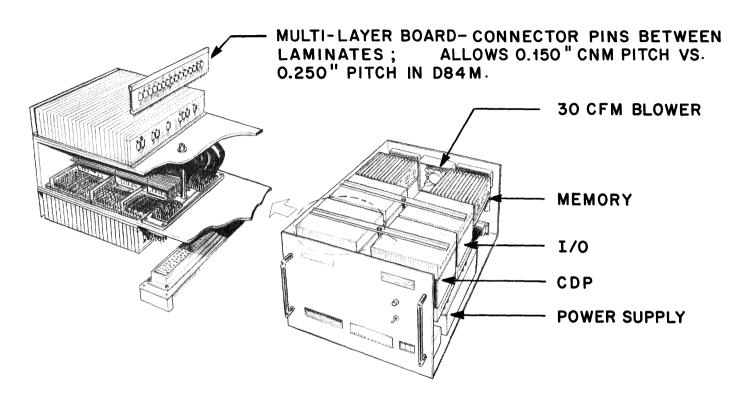
WEIGHT: 218 LB.

POWER: 230 WATTS*

* ONE 4096-WORD MEMORY ACTIVE, BALANCE ON STANDBY- WORST CASE

- (1) SYSTEM BLOCK DIAGRAM ON CHART 21.
- 2 SYSTEM BLOCK DIAGRAM ON CHART 20.

D84A AIRBORNE COMPUTER



CONTAINS:

1 CDP MODULE

1 I/O MODULE

1 4096 x 25 BIT CORE MEMORY MODULE

1 POWER PACK

HEIGHT: 75/8 IN.

WIDTH: 15³/8 IN. STANDARD
ATR CASE
MS 91403-CID

DEPTH : 19⁹/16 IN.

WEIGHT: 60 LB.

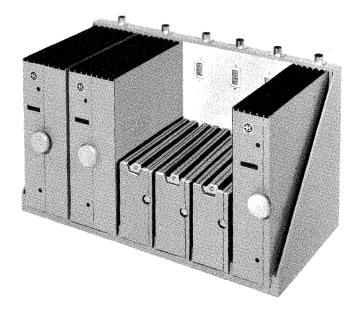
POWER: 170 WATTS

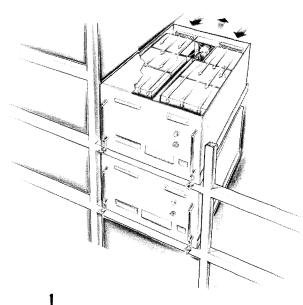
COOLING: 30 CFM (AT SEA LEVEL)

D84 M

VS.

D84A





CONTAINS:

1 CDP MODULE

1 I/O MODULE

1 POWER PACK

3 4096-WORD MEMORY MODULES

D84 M

HEIGHT: 18.0 IN.

WIDTH: 30.0 IN.

DEPTH: 16.5 IN.

WEIGHT: 218 LB.

VOLUME: 5.25 CU.FT.

POWER 230 WATTS

IN SAME VOLUME, 3
MORE 4096-WORD
MEMORIES ACCOMMODATED
(FOR 24 K TOTAL)

D84A

15/4 IN.

15 3/8 IN.

19⁹/16 IN.

88 LB.

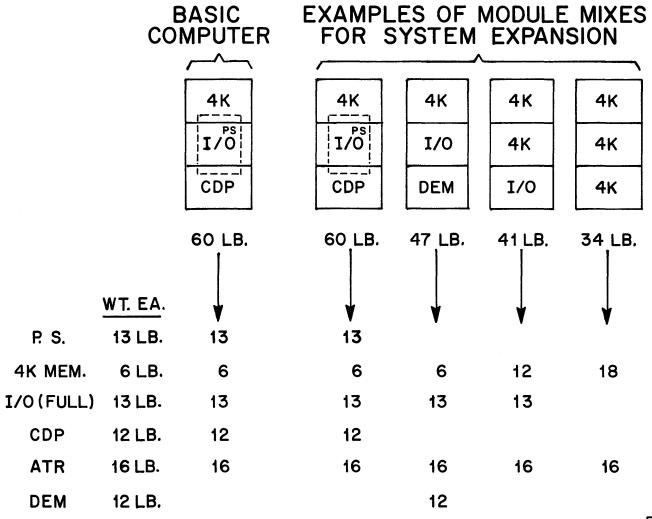
2.66 CU.FT.

194 WATTS

IN SAME VOLUME, 1
MORE 4096 - WORD
MEMORY ACCOMMODATED
(FOR 16 K TOTAL)

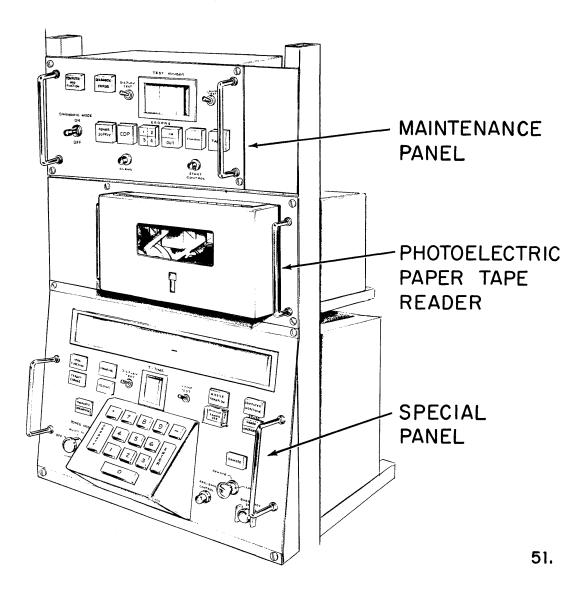
49.

D84A SYSTEM EXPANSION



50.

TYPICAL CONTROL AND MAINTENANCE EQUIPMENT



SOFTWARE-LATER DELIVERIES (2nd. HALF - 166)

- 1. ON-LINE ASSEMBLER
 - 2 PASS ON MINIMUM SYSTEM
 - RELOCATABLE SUBROUTINES
- 2. COMPILER
 - FORTRAN IX
- 3. EXECUTIVE PROGRAM
 - LOADER, ON MINIMUM SYSTEM
 - MULTIPROCESSING

NEW SPECIFICATION SHEETS TO BE RELEASED: DELIVERY

DELIVERY CAPABILITY

DATA EXCHANGE MODULES - 3 TYPES

2nd QUARTER '66

- 1- TO ADDRESS 65K HOMOGENEOUSLY
- 2— TO BUFFER WITH CONCURRENT ACCESS TO MEMORY
 BY I/O AND CDP (AND INCLUDE (1))
- 3- TO MULTI-PROCESS (AND INCLUDE 1AND 2)

BUFFERING OPTIONS	1st & 2nd QUARTER '66
D84A PACKAGING OPTION	3rd QUARTER '66
CONTROLLER LOGIC FOR COMMONLY USED PERIPHERALS	1st QUARTER '66
I/O EXCHANGE OPTION ON EACH CONTROLLER TYPE	2nd QUARTER '66
NDRO THIN FILM	1st QUARTER '67
CHARACTER MANIPULATION	2nd QUARTER '66
BINARY BCD CONVERSION HARDWARE	2nd QUARTER '66
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BUDGETARY PRICES

"GREEN SHEET MACHINE" - D84M OR D84A PACKAGING - WITH 4K MEMORY

I - \$96K (\$74K)

10 - \$70K (\$55K)

100 - \$57K (\$52K)

500 - \$48K (\$48K)

ADDITIONAL MEMORY MODULES

I - \$19K (\$17K)

10 - \$15K (\$14K)

100 - \$12K (\$12K)

500 - \$10K (\$10K)



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