A U T O N E T I C S
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INDUSTRIAL PRODUCTS
3584 Wilshire Blvd., Los Angeles 5, Calif.

August 31, 1960

RECOMP TECHNICAL BULLETIN NO. 14

TITLE: RECOMP II EXTERNAL OUTPUT DEVICE CONNECTION TO COMPUTER OUTPUT PLUG (J7)

PURPOSE: The following is a detailed description of the timing, voltage levels, impedances and waveforms available from the computer or required by the computer when outputting information to an external device. The output device can be a punch, a typewriter, a digital to analog converter, a plotter or any device capable of accepting a five level binary code.

EFFECTIVE DATE: August 31, 1960

CONTENTS: The output operation starts when flip-flop M_7 is turned on. During the first word time (U1) of the operation, the output register (F_5 - F_1) is loaded with the code to be sent to the output device. There is a fixed delay of 32 word times from the start of M_7 to the time that flip-flop X_9 is triggered, which indicates to the output device that the computer is ready to send the code to it. The timing of the output operation from that point on is determined primarily by the speed of the output equipment. The false to true transition of the TPP_p signal from the output unit may be sent to the computer at the same time as but not before the true to false transition of the TPP_p' signal from the output unit. The TPP_p signal must remain true for a minimum time of 12 microseconds; the maximum time of TPP_p is such that the true to false transition of TPP_p must happen at the same time as or before the false to true transition of TPP_p'.

TPP_p' true indicates to the computer that the output function has been completed. The TPP_p' true signal causes a two word delay in the computer, during which time the output register is reset to zero. At the end of the delay period the output instruction is terminated, and the computer continues with its program.

The accompanying chart and diagram (Figures 1 & 2) will aid in understanding the signals and voltages available on the output connector. The output rate, without considering the access time of instructions and data words or the speed of the output device, is a maximum of 100 characters per second. The minimum rate is determined by the output device.

INFORMATION TO: All concerned

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Output Plug Chart

J7 - Cannon DD50S Connector

Pin 1 X_9 - Indicates to output device that the computer is ready to output information. X_9 is the output of a driver and normally drives a 110 ohm load from the -28 volt source.

Pin 2 F_5 Signal Output - Flip-flop F_5 in output register triggers an output driver, which grounds one side of the load being driven when a true signal exists.

Pin 3 F_4 Signal Output - Flip-flop F_4 in output register triggers an output driver.

Pin 4 F_3 Signal Output - Flip-flop F_3 in output register triggers an output driver.

Pin 5 F_2 Signal Output - Flip-flop F_2 in output register triggers an output driver.

Pin 6 F_1 Signal Output - Flip-flop F_1 in output register triggers an output driver. Each of the signals, F_5 through F_1 normally drives a 220 ohm load.

Pin 7 -28V. - Supplies -28V unregulated dc at one (1) amp (including the F_5 - F_1 loads above). The waveform of this voltage is shown on Figure 2.

Pin 8 -12V. - Supplies -12 ± 0.5 volts at 60 ma with no appreciable ripple. This level should be loaded so that the simultaneous total from J7-8 and J21-39 is 60 maximum.

Pin 9 Chassis Ground - Provides the necessary ground connection between the computer and the output device.

Pin 10 TPP_p' - Tape punch pulse false, which indicates to the computer that the output device is not performing any function. The input impedance at the true level (-12V) is 400 ohms.

Pin 11 TPP_p - Tape punch pulse true, which indicates to the computer that the output device is performing its normal function, and is used by the computer as an interlock for its own operations. The input impedance at the true level (-12V) is 400 ohms.

Figure 1

TIMING DIAGRAM

OUTPUT CONNECTOR

PUNCH CHARACTER INSTRUCTION

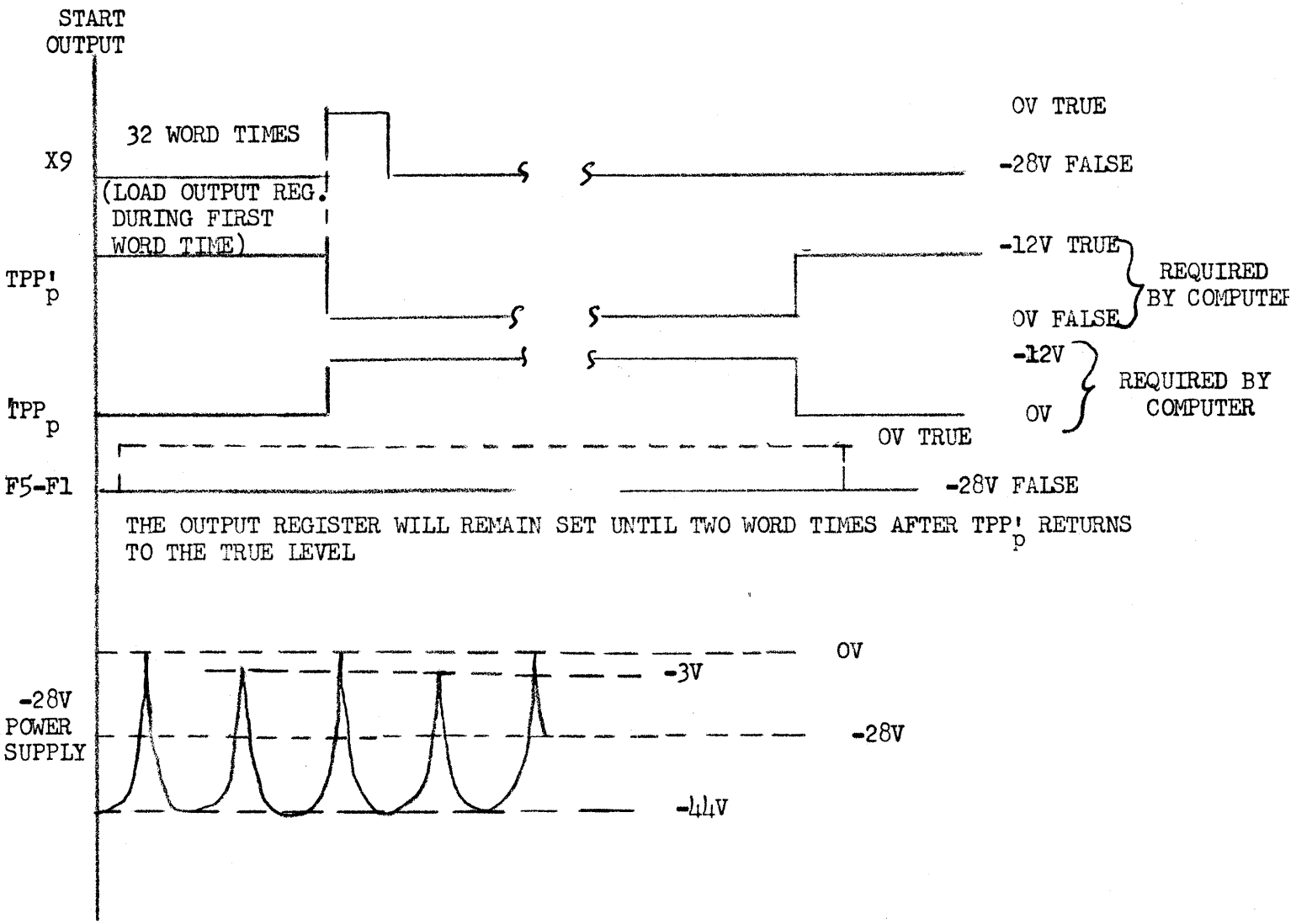

FIGURE 2