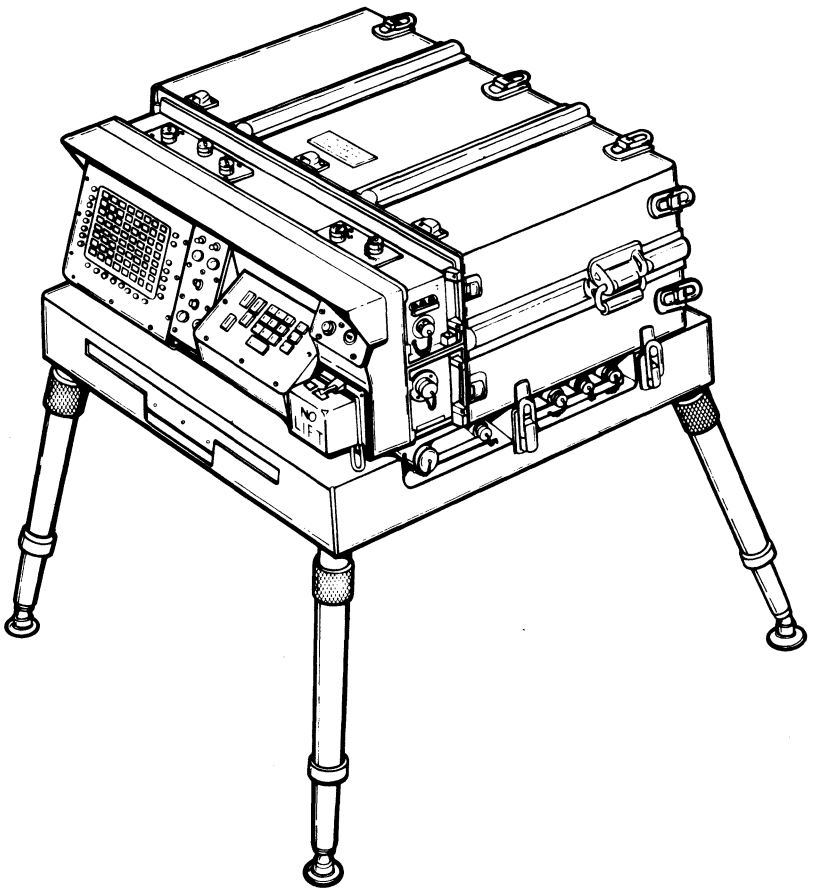
TM 9-1220-221-34/1

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

FOR



COMPUTER, GUN DIRECTION, M18

(FADAC)

(NSN 1220-00-448-0131)

HEADQUARTERS, DEPARTMENT OF THE ARMY
MAY 1981

Technical Manual)
)
No. 9-1220-221-34/1)

HEADQUARTERS,
DEPARTMENT OF THE ARMY
Washington, DC, 25 May 1981

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL

FOR

COMPUTER, GUN DIRECTION, M18
(FADAC)

(NSN 1220-00-448-0131)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Armament Materiel Readiness Command, ATTN: DRSAR-MAS, Rock Island, IL 61299. A reply will be furnished to you.

*This publication supersedes TM 9-1220-221-34/1, 5 December 1968, including

CHAPTER 4. TROUBLESHOOTING --Continued

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS--Continued

LIST OF TABLES

CHAPTER 1
INTRODUCTION

Section I. General

1-1. SCOPE

a. This manual contains instructions for the repair of the gun direction computer M18 (FADAC) by direct support and general support maintenance personnel.

NOTE

Instructions for overhaul/reconditioning of this material have been printed separately as Depot Maintenance Work Requirements (DMWR). Requests for DMWR's in support of approved overhaul/reconditioning programs, should be forwarded directly to the Commander, US Army Armament Materiel Readiness Command, ATTN: DRSAR-MAS, Rock Island, IL 61299.

b. These instructions are used in conjunction with and are supplementary to those in the operator's and organizational maintenance manual for the FADAC. Subsequent volumes of this manual contain logic, mechanization of logic equations, schematic diagrams (TM 9-1220-221-34/1/1), and specific detailed logic test program printouts for the computer; i.e., TM 9-1220-221-34/2 contains test tape B program printout, TM 9-1220-221-34/3 contains test tape C program printout, TM 9-1220-221-34/4 contains test tape D program printout, and TM 9-1220-221-34/5 contains test tape E program printout. It may be necessary to refer to the operator's or organizational maintenance technical manual in order to obtain complete procedures.

c. A description of the computer, use of special tools and equipment, inspection procedures, troubleshooting procedures, and repair operations peculiar to direct support and general support maintenance levels are presented in this manual.

d. The appendix contains a reference list including supply and technical manuals, forms, and other available publications applicable to direct support and general support maintenance of the computer.

e. In order to differentiate between a zero and the letter O, a zero will be shown thus (Ø) in only logic equations.

1-2. MAINTENANCE ALLOCATION AND PARTS

The maintenance allocation chart located in TM 9-1220-221-20&P and repair parts and tools listed in TM 9-1220-221-34P allocates maintenance responsibilities.

1-3. FORMS, RECORDS AND REPORTS

a. Reporting Equipment Improvement Recommendations (EIR). EIR's can and must be submitted by anyone aware of an unsatisfactory condition with the equipment design or use. It is not necessary to show a new design or list a better way to perform a procedure, just simply tell why the design is unfavorable or why a procedure is difficult. EIR's may be submitted on SF 368 (Quality Deficiency Report). Mail directly to Commander, US Army Armament Materiel Readiness Command, ATTN: DRSAR-MAO, Rock Island, IL 61299. A reply will be furnished to you.

b. Authorized Forms. The forms are listed in DA Pamphlet 310-2 and TM 38-750.

c. Report of Accidents. The necessary reports are prescribed in AR 385-40.

d. Materiel Failure Report. Reports will be in accordance with TM 38-750.

e. US Army Equipment Logbook.

(1) Refer to TM 38-750.

(2) The Army Equipment Logbook is composed of a looseleaf binder (750-00-889-3494) and the following DA Forms:

DA Form 2408-9
DA Form 2408-10
DA Form 2408-14

Section II. Description and Data

1-4. DESCRIPTION

FADAC is an acronym for Field Artillery Digital Automatic Computer (computer M18). Refer to TM 9-1220-221-10-1, TM 9-1220-221-10-2, and TM 9-1220-221-20&P for a description of the FADAC.

1-5. DATA (COMPUTER LOGIC)

Maintenance at the direct support and general support levels requires a detailed knowledge in the use of logic equations and test tape listings to isolate and correct malfunctions in the computer.

CHAPTER 2
TOOLS AND EQUIPMENT

2-1. COMMON TOOLS AND EQUIPMENT

Standard tools and equipment having general application to this material are authorized for issue by tables of allowances and tables of organization.

2-2. SPECIAL TOOLS AND EQUIPMENT

Table 2-1 lists the special equipment which is necessary to perform the operations described in this manual. Special tool sets of a general nature are authorized by table of allowance and table of organization. Special tools peculiar to this equipment are authorized in their respective -34P manuals referenced in table 2-1.

Table 2-1. Special Equipment

Nomenclature	National stock no.	Part no.	Reference	Use
Test Set, computer logic unit AN/GSM-70 (FALT)	4931-00-045-6540	8623273	TM 9-4931-204-12&P	To address and test logic circuitry in the computer.
			TM 9-4931-204-34P	For requisitioning purposes.
Reproducer, signal data AN/GSQ-64 (SDR)	1290-00-973-2180	10531830	TM 9-4931-204-12&P	Input program information into computer and to read test tapes when used in conjunction with FALT.
			TM 9-1290-326-34P	For requisitioning purposes.
Control Box, computer logic unit, test set C-4020/GSM-70	4931-00-020-8702	8623274	TM 9-4931-204-34/1	To manually test logic circuitry in computer.
			TM 9-4931-204-34P	For requisitioning purposes.

CHAPTER 3
INSPECTION

Section I. General

3-1. SCOPE

This chapter sets forth inspection of the FADAC for the using organization and in direct support or general support shops.

3-2. PURPOSE

Inspection is performed primarily to determine completeness; to determine the nature of unserviceability; to determine the work, repair parts, and supplies required to return the materiel to serviceability, to ensure that work in process is being performed properly; and to ensure that completed work complies fully with serviceability standards.

Section II. Inspection in the Hands of Troops

3-3. GENERAL

In general, the FADAC will be considered serviceable if it is complete and all deficiencies have been corrected, ensuring operation in accordance with serviceability standards.

3-4. FORMS AND RECORDS

Authorized forms and records for technical inspection by direct support and general support maintenance personnel are listed in the appendix. The equipment logbook will be examined to determine the maintenance background of the computer.

3-5. MODIFICATION WORK ORDERS (MWO)

All applicable modification work orders will be applied. DA Pamphlet 310-7 contains the MWO index and equipment records. DA Form 2408-5 or DA Form 2409 lists MWO's applied.

3-6. GENERAL INSPECTION

a. Note general appearance as an indication of the material and the type of treatment it has received.

b. Check exterior of material and accessible parts for dented surfaces, bent or broken parts, missing parts of hardware, moisture, corrosion, and other evidence of damage or misuse which might indicate need for repair.

c. Inspect all sealed and painted portions of the material to determine if sealing is complete. Inspect seal on mechanical reader cover assembly. Inspect for presence of gaskets under assemblies of the control panel

assembly. Inspect for presence of gasket between control panel and chassis assemblies. Inspect seals on front and rear covers of case assembly. Inspect for presence of covers on receptacles of FADAC and computer table.

d. Inspect all legends on main control panel assembly, reference designations on connectors to the right and left of control panel assembly, and lettering on nameplate for legibility. Inspect transparent material over readout panel for cleanliness, cracks, or abrasions which would impair visibility of tube indicators.

e. Inspect all bare spots or damaged finish which expose metal surfaces and lead to corrosion.

f. Inspect all controls for smooth operation.

g. The equipment must be clean and free from dirt.

h. Check for completeness of spare parts and equipment. Refer to TM 9-1220-221-20&P.

i. Check organizational spare parts and equipment for general condition and method of storage, and procedures for obtaining replacements.

j. Investigate mechanical and functional difficulties that troops may be experiencing and check for determinable causes such as inadequate design, poor workmanship or material, lack of knowledge, misinformation, neglect, or improper handling of equipment.

k. Instruct the using personnel in supply and preventive maintenance procedures if the need for such instruction is necessary.

3-7. INSPECTION OF ELECTRICAL ASSEMBLIES AND PARTS

NOTE

Inspect electrical assemblies in process, if possible, when equipment is normally disassembled (chassis assembly removed from case assembly).

Electrical material will be visually inspected for evidence of circuit faults or possible sources of trouble as indicated by the conditions in a thru f.

a. Burned or carbonized insulation.

b. Discolored resistors; cracked or swollen parts.

NOTE

In particular, inspect parts mounted on main frame of chassis assembly.

c. Corrosion on capacitors and other parts of power supply subassembly; bleeding transformers or chokes.

d. Improperly soldered connections; insecure wiring and harness. Loose connections at harness terminations.

e. Improper clamping of harness; abrasions; worn, or defrayed insulation on harness and wiring.

f. Excessive wear of associated cables and connectors, bent pins or sockets, dirt on connectors, and absence of protective caps on cables. Improper storage of cables.

3-8. PERFORMANCE TEST OF FADAC

a. Program Test. Perform program test 1, 2, and 3 with the MARGINAL TEST switch rotated to each of its six positions. The correct indications shall be obtained for all six positions (TM 9-1220-221-10-1 or TM 9-1220-221-10-2).

b. Test Problem. Perform a test problem which involves operating as many controls as possible with the MARGINAL TEST switch in each of its six positions. The correct solution shall be obtained for all positions. Refer to TM 9-1220-221-10 series of manuals for test problems and solutions.

Section III. Inspection and Receipt of Materiel

3-9. GENERAL

Technical inspection performed by the direct support or general support shop upon receipt of material turned in for repair determines the course of unserviceability, the amount of work required to return the material to serviceability, the work of tests accomplished thus far by organizational maintenance personnel, and the results of those tests. Furthermore, this inspection is to determine the amount of supplies, parts, or assemblies, necessary to accomplish repairs, insofar as is possible by a preliminary survey. When further diagnostic tests indicate the amount of supplies, parts, or assemblies necessary to accomplish repairs, the ordering of these should be expedited in order to reduce the time the equipment is unserviceable and in the shop for repair.

3-10. INSPECTION OF FADAC

a. Perform a general inspection in accordance with paragraph 3-6.

b. Inspect transfer documents, forms, and reports for indication of specific symptoms which caused the FADAC to be transferred to the direct support or general support organization for repair.

c. Inspect transfer documents, forms, reports, and logs for an indication of the specific tests performed by organizational maintenance personnel, and the results of those tests.

d. Determine the nature of the repairs required and consult the maintenance allocation chart (TM 9-1220-221-20&P) to determine if the anticipated repair is within the cognizance of direct support and general support maintenance and that the computer has been referred to the proper activity specified therein.

CHAPTER 4
TROUBLESHOOTING

Section I. General

4-1. PURPOSE

Troubleshooting is the systematic isolation and remedy of a malfunction by means of recognizing symptoms and testing for a malfunction. Close adherence to the procedures covered herein will reduce the time required to locate the trouble and restore the equipment to normal operation.

4-2. ORGANIZATIONAL MAINTENANCE PERSONNEL RESPONSIBILITY

Organizational maintenance personnel are responsible to correct all malfunctions within the scope of their authorization. For this purpose an inspection procedure and a troubleshooting table are provided. Organizational personnel are also responsible to tag all defective assemblies or the computer if the malfunction could not be corrected; indicating in either case the symptoms resulting from the malfunction. In the case of a known or suspected unit, such as the circuit breaker, blower, or elapsed time indicator, the tag on the computer must be marked as such.

4-3. DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE PERSONNEL RESPONSIBILITY

Direct support and general support maintenance personnel must return the computer to a serviceable condition unless a complete overhaul is required. This is accomplished either by replacement of assemblies or by correcting wiring malfunctions or faulty solder connections. This includes repair of cables and replacement of the computer table.

4-4. RECEPTION OF DEFECTIVE COMPUTER OR DEFECTIVE ASSEMBLIES

Defective units received at the direct support and general support level can be grouped into four general categories:

a. Tagged defective circuit boards, keyboard assemblies, mechanical readers, or matrix assemblies. Notify depot maintenance personnel.

b. Damaged computer table or defective cable. If the computer table is damaged, replace it and notify depot maintenance personnel. Repair all defective cables.

c. FADAC with known or suspected defective unit (circuit breaker, blower, elapsed time indicator, etc) noted on tag. Refer to paragraph 4-5.

d. Defective FADAC with unknown cause of trouble. Refer to paragraphs 4-5 and 4-6.

4-5. TROUBLESHOOTING TECHNIQUE

TM 9-1220-221-20&P, the troubleshooting chart, table 4-1, and other sections of this chapter are to be used by direct support and general support maintenance personnel to isolate and correct troubles that occur in the FADAC. The step-by-step inspection procedure and an organizational troubleshooting chart of TM 9-1220-221-20&P must be utilized first. Table 4-1 of this manual contains additional techniques that are to be used by direct and general support maintenance personnel to isolate and correct malfunctions other than those listed in TM 9-1220-221-20&P. Six other sections useful to troubleshooting are also included in this chapter. Section II covers troubleshooting power control circuitry. Section III covers troubleshooting power supply circuitry. Section IV covers malfunction isolation using the test tapes, FALT, and control box C-4020. Section V covers troubleshooting input-output circuitry. Section VI covers troubleshooting write and read circuitry. Section VII contains a description of each board. This particular section is of great use in all areas of troubleshooting.

CAUTION

DO NOT OPERATE MEMORY UNIT (MAGNETIC DISK) WHEN THE CHASSIS IS ON EDGE AND UNFOLDED.

4-6. METHOD OF APPROACH

The general maintenance troubleshooting approach for a malfunctioning computer is:

a. Determine if the problem is in power control or power supply circuitry. (See TM 9-1220-221-20&P and table 4-1.) If this is the case, refer to section II or III of this chapter. If problem is not one involving these circuits proceed to step b.

b. Run test tapes B thru E. Refer to section IV of this chapter. If the problem is not detected using the test tapes, proceed to step c.

c. Run the diagnostic test routines if available (procedures are contained in TM 9-1220-221-34/8). If the problem is not detected using these routines, proceed to step d.

d. Utilizing the symptoms of the failure, isolate problems to a general area within the computer and refer to appropriate section.

Table 4-1. Troubleshooting

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
1. FADAC DOES NOT REMAIN ON BECAUSE CIRCUIT BREAKER IS BEING TRIPPED.
Step 1. Check for mechanical binding of either of the two blower motors or binding of magnetic disk.
Replace defective unit. See chapter 6 for removal and installation procedures.
Step 2. Check for short to the three-phase input lines.
Refer to chapter 4, section II.
2. FADAC DOES NOT TURN ON, OR TURNS ON ONLY MOMENTARILY OR KICKS OUT DURING OPERATION (BLOWERS NOT OPERATING).
Check power control circuitry.
Refer to chapter 4, section II.
3. NONE OF THE FRONT PANEL INDICATORS ARE LIT (BLOWERS ARE OPERATING).
Check for excessive load on power supply causing the master kickout of regulated voltages.
Refer to chapter 4, section III.
4. FADAC POWER SUPPLY VOLTAGES ARE NOT CORRECT AS INDICATED BY VOLTAGE MONITOR OF FALT.
Check power supply circuitry.
Refer to chapter 4, section III.
5. TEST TAPE STOPS AND ERROR INDICATOR ON FALT FLASHES.
Check for faulty board(s) or assembly or faulty wiring.
Refer to chapter 4, section IV.
6. PROGRAM CANNOT BE LOADED AND VERIFIED THROUGH SDR. TEST TAPES FAIL TO LOCATE MALFUNCTION.
Step 1. Check input logic.
Refer to chapter 4, section V.

Table 4-1. Troubleshooting--Continued

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
6. PROGRAM CANNOT BE LOADED AND VERIFIED THROUGH SDR. TEST TAPES FAIL TO LOCATION MALFUNCTION.--Continued
Step 2. Check write or read circuitry.
a. Run a 45-second memory evaluation diagnostic test tape and loop test routine.
b. Refer to chapter 4, section VI.
7. PROGRAM TESTS FAIL, (PARITY, ERROR, OR NO SOLUTION) TO TEST PROBLEM WHEN PROGRAM TAPE IS LOADED INTO FADAC. TEST TAPES FAIL TO LOCATE MALFUNCTION.
Step 1. Check write or read circuitry.
Run 45-second memory evaluation diagnostic test tape and loop test routine.
Step 2. Check logic circuitry.
Refer to chapter 4, section VI.
8. DATA CANNOT BE LOADED THROUGH KEYBOARD. TEST TAPES FAIL TO LOCATE MALFUNCTION.
Check keyboard circuit.
Run control panel diagnostic test routine tape.
9. DATA CANNOT BE LOADED THROUGH MECHANICAL READER. TEST TAPES FAIL TO LOCATE MALFUNCTION.
Step 1. Check input logic.
Refer to chapter 4, section V.
Step 2. Check mechanical reader circuit.
Refer to chapter 4, section V.

Section II. Power Control

4-7. SCOPE

This section provides information useful in isolating malfunctions that occur in the power control circuitry of the FADAC. Replacement of the parts indicated in this section are authorized to the extent of available parts. Refer to TM 9-1220-221-20&P.

4-8. FUNCTION OF POWER CONTROL

The basic function of the power control system is to provide control over primary power application to the FADAC. This system must provide control over extremes of environment, field power source, and abnormal conditions; provide correct phase rotation; control synchronizing of the FADAC; and provide other control and safety functions.

4-9. POWER CONTROL POWER SUPPLY OPERATION

a. During initial turnon, closing of the POWER ON-OFF momentary switch energizes the power control relay (K1), the power control power supply, and phase detectors.

b. Various voltages from the power control supply are used in the operation of all the sensing circuits.

c. If all environmental and primary power conditions are within the specified limits, the main power relay drive is energized by input signals derived from the sensing elements which will allow the primary power to be supplied to the FADAC.

d. If any one condition or input is not correct during operation, the main power relay driver will be deenergized and power will be removed from the entire FADAC, including the power control system.

4-10. PRIMARY LINE VOLTAGE SUPPLY

a. The FADAC is designed to operate with a marginal primary voltage source.

b. A steady state voltage range of 100/173 vac to 140/243 vac or ±16.7 percent of the nominal voltage of 120/208 vac is required to operate the unit.

c. A voltage detector is designed in the FADAC which will allow the primary voltage surge down to approximately 80/138 vac for a period of approximately 5 seconds before the computer is turned off.

d. The main power relay driver is controlled by three voltage detectors:

(1) High voltage kickout (HVK').

(2) Low voltage kickout (LVK').

(3) Low voltage transient kickout (LVTK').

4-10. PRIMARY LINE VOLTAGE SUPPLY--Continued

e. The purpose of these input circuits is to sense an unregulated voltage from the power control power supply (-27 volts).

(1) If the line voltage moves above 140 or below 80 vac (line to neutral), power is immediately removed by either HVK' or LVK' lines.

(2) If the line voltage moves below 100 vac and remains between 80 and 100 vac for a period longer than 5 seconds, power is removed by the LVTK' line.

f. Voltage warning circuits also have been incorporated in the FADAC. The TRANSIENT indicator will flash if the line voltage is less than 107 volts ac or greater than 132 volts ac. The TRANSIENT indicator will also flash if a transient occurs on the line. This normally can be reset.

4-11. PRIMARY LINE SUPPLY FREQUENCY

a. The FADAC is designed to operate over a specified range of 380 to 420 Hz.

b. Since the FADAC is utilizing a free disk-type memory, a frequency detector is not necessary.

c. If the input frequency is too high or too low the transient indicator may flash and cannot be reset. The frequency must be correct at the power source.

4-12. TEMPERATURE SENSING

The FADAC is designed to operate over a specified temperature range of -40° to +125°F. A warmup period may be required for the memory if operation is started in the range of -40° to -25°F. When the internal air temperature of the computer is within the range of -40° to +125°F, two sensors (thermistors) will allow line TEK' (temperature kickout not) to enable the main power relay driver. These sensors are:

a. High Temperature Detector.

b. Low Temperature Detector.

4-13. LOCATION OF THERMISTORS

The high temperature thermistor is located in an area as to detect failure of the blowers. The temperature of this area will rise the fastest if the blowers stop. The thermistors near the air inlet check the incoming ambient air temperature and low temperature detectors are located on regulator no. 3, board no. 132.

4-14. LOW MEMORY TEMPERATURE SENSOR

a. For any temperature above -25°F the line LMT' (low memory temperature not), shown on foldout 1, will energize the memory motor relay which in turn supplies primary power to the memory motor.

b. The low memory temperature thermistor is mounted directly on the memory.

4-15. LOW TEMPERATURE OPERATION

a. In the temperature range between -25° and -40°F the operation of line TEK' allows power to be applied to the computer. However, line LMT' inhibits power to the memory.

b. Operation in this temperature range requires that the rear cover of the FADAC be left in place.

(1) A switch is operated by the rear cover which stops the rotation of the lower blower.

(2) The rear cover also closes the air path within the FADAC so that no external air is drawn in, thus the warmup period is aided by the entire power dissipation of the computer.

(3) The upper blower is operated to prevent any possibility of hot spots and to pass the heated air over the memory.

(4) When the temperature rises above -25°F, the memory motor relay operates, allowing power to flow to the memory motor.

NOTE

The rear cover can remain on if the ambient temperature remains in the region of -40° to -25°F. Maximum temperature will not be exceeded within the computer. Preliminary calculations indicate that the memory temperature will be approximately 35°F over the ambient temperature and the warmup time from -40° to -25°F will be approximately 20 minutes.

4-16. TD CIRCUIT

The purpose of the TD (time delay) circuit is to provide a 20-second delay to ensure the memory disk speed reaches the proper operating speed of 6000 RPM.

a. Input is LMT (low memory temperature). If the warmup cycle is required for memory, the TD circuit is not started until line LMT' comes true.

NOTE

FC^2 is an input from the FALT for testing.

b. Output of the TD circuit is to the TD/WI flip-flop located on the same circuit board.

4-17. TD/WI (TIME DELAY/WRITE INHIBIT) FLIP-FLOP

a. The TD/WI flip-flop is initially forced off (TD true and WI false) and remains off until triggered by the TD circuit.

b. During the delay period, line TD is at a true signal level to various gates required to synchronize the bit counter and set certain flip-flops to a required state. During the same period, the WI line provides a false signal level to the memory write switches to prevent any possibility of false writing into the memory unit.

4-17. TD/WI (TIME DELAY/WRITE INHIBIT) FLIP-FLOP--Continued

c. After the delay period, the TD/WI flip-flop is triggered on (TD false/-WI true).

d. The WI line enables the write switches and also controls the illumination of the POWER READY indicator on the control panel.

e. Power is turned off either by operating the POWER ON-OFF switch to the OFF position or if any one of the environmental or input power levels exceeds specified limits. As the main power relay starts to drop out, the TD/WI flip-flop immediately changes state thereby preventing any possibility of false writing into memory.

NOTE

Four control lines, FC^1, FC^2, and set-reset are test line inputs to the TD circuit and TD/WI flip-flop.

(1) Input from FC^1 and FC^2 of the FALT inhibit normal operation of the TD circuit when the FALT is used.

(2) Input from the set-reset lines (OSR-1SR) of the FALT control the state of the TD/WI flip-flop when tested by the FALT.

4-18. PRIMARY SUPPLY PHASING

Primary supply phasing is accomplished by two phase detectors, no. 1 and no. 2. The purpose of these circuits is to ensure that the proper phase voltages are applied to the blower motors and memory motor to ensure correct rotation.

4-19. EXPLANATION OF POWER CONTROL FUNCTIONAL SCHEMATIC DIAGRAM

The block diagram in foldout 1 illustrates the functional schematic diagram of the FADAC power control circuitry. It indicates the proper input and output voltages from each circuit, the input and output board and pin numbers, the function of each circuit, and the input and output terms. In the bottom right corner of some of the blocks is the letter A, B, or C. This indicates the type of board (Power Control A, B, or C).

4-20. OPERATION OF POWER CONTROL CIRCUITRY

Assuming that the main power circuit breaker is closed, momentary operation of the POWER ON-OFF switch to the ON position provides a ground return for K1. With K1 energized, three-phase voltage is applied to the primary of transformer T3, thus developing power for the power control circuits (FO-1). The POWER ON-OFF switch also provides -6 volts to the main power relay driver. If the prime input voltage is correct and the temperature of the computer is between -40° to 125°F, terms HVK', LVK', LVTK', and TEK' will all be true (-12-volt output). These voltages will enable the main power relay driver and provide a ground return path through the coil of relay K2. When the POWER ON-OFF switch is released, the P OFF term appears as an open. The ground return path for relay K1 is now through contacts 12 and 13 of K2. At the same time that the POWER ON-OFF switch is depressed, the phase detectors detect the phase of the prime power and either K3 or K4 is energized, providing the

proper phase input power, so that the memory and blower will rotate in the proper direction. Simultaneously, if the temperature and input voltages are normal, terms LMT', TEW', HVW', LVW' come true (-12-volt output). Term LVT' enables the TD circuit and also enables the memory motor relay driver, thus enabling relay K5 while allowing prime current to flow to the memory motor. Terms LMT' and TEW' cause output term TEMP to be at 0 volts. (The TEMP indicator will not flash if output TEMP is at 0 volts.) Terms HVW' and LVW' cause output term TRANS to be 0 volts. The TRANSIENT indicator will not flash if output TRANS is at 0 volts. Twenty seconds after the POWER ON-OFF switch is depressed, term WI (write inhibit) comes true (-12 volts). Term TD, which came true when power was applied to the power control power supply, now goes false (0 volts). When WI goes true, the POWER READY indicator will light. If the MKO (master kickout) which is generated by a main power supply failure comes true (+20 volts), term TD will go true (12 volts) and term WI will come false (0 volts). Button S3 (RESET) and its associated relay K6 are energized only in extremely cold weather. The contacts of K6 remove power from the lower blower. When button S3 (RESET) is depressed by the rear cover of the FADAC, the POWER READY indicator will flash.

NOTE

Refer to table 4-2 for physical location of circuits and table 4-3 for chart of environmental conditions or affected circuit vs computer reaction.

4-20. OPERATION OF POWER CONTROL CIRCUITRY--Continued

Table 4-2. Physical Location of Circuits

Circuit	Location
Low memory Temp Detector	Power Control A, board 204
Low Temp Warning Detector	Power Control A, board 204
High Temp Warning Detectors	Power Control A, board 204
Low Temp Kickout Detector	Power Control A, board 204
High Temp Kickout Detectors	Power Control A, board 204
Low Voltage Kickout Detector	Power Control B, board 203
Low Voltage Warning Detector	Power Control B, board 203
Low Voltage Transient Detector	Power Control B, board 203
High Voltage Kickout Detector	Power Control B, board 203
High Voltage Warning Detector	Power Control B, board 203
Voltage Warning Inverter	Power Control B, board 203
Main Power Relay Driver	Power Control B, board 203
Memory Motor Relay Driver	Power Control B, board 203
TD/WI Flip-Flop	Power Control C, board 101
TD Circuit	Power Control C, board 101
Temp Warning Inverter	Power Control C, board 101
Primary Power Rectifier	Power Control C, board 101
Phase Detector Rectifiers	Power Control C, board 101

Table 4-3. Chart of Environmental Condition or Affected Circuit Versus Computer Reaction

Environmental conditions	Affected circuit	Computer reaction: Disable Main Power Relay	Disable Memory Power	Phase Relay No. 1 Pickup	Phase Relay No. 2 Pickup	Voltage Warning Indicator	Temperature Warning Indicator
Input line to neutral voltage less than 80 vac	Low voltage kick-out circuit or main power relay driver circuit	X					
Input line to neutral voltage less than 100 vac for longer than 5 seconds	Lower voltage trans kickout circuit or main power relay driver circuit	X					
Input line to neutral voltage more than 140 vac	High voltage kick-out or main power relay driver circuit	X					
Internal air temperature less than -40°F.	Low temp detector circuit, temp kickout circuit or main power relay driver circuit	X					
Temperature too high in upper half of computer	High temp detector no. 1 circuit, temp kickout circuit or main power relay driver circuit	X					
Phase loss	Phase detectors no. 1 or no. 2 circuit	X					
Memory temperature less than -25°F.	Low memory temp detector circuit	X					X
Primary phase rotation ABC				X			

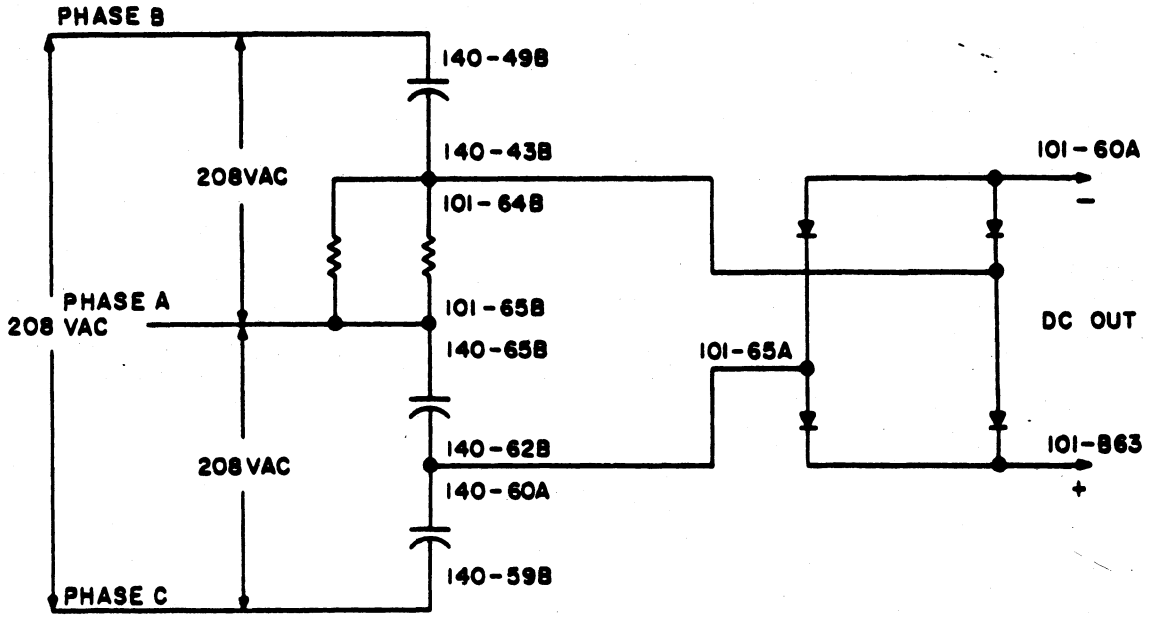
4-20. OPERATION OF POWER CONTROL CIRCUITRY--Continued

Table 4-3. Chart of Environmental Condition or Affected Circuit Versus Computer Reaction--Continued

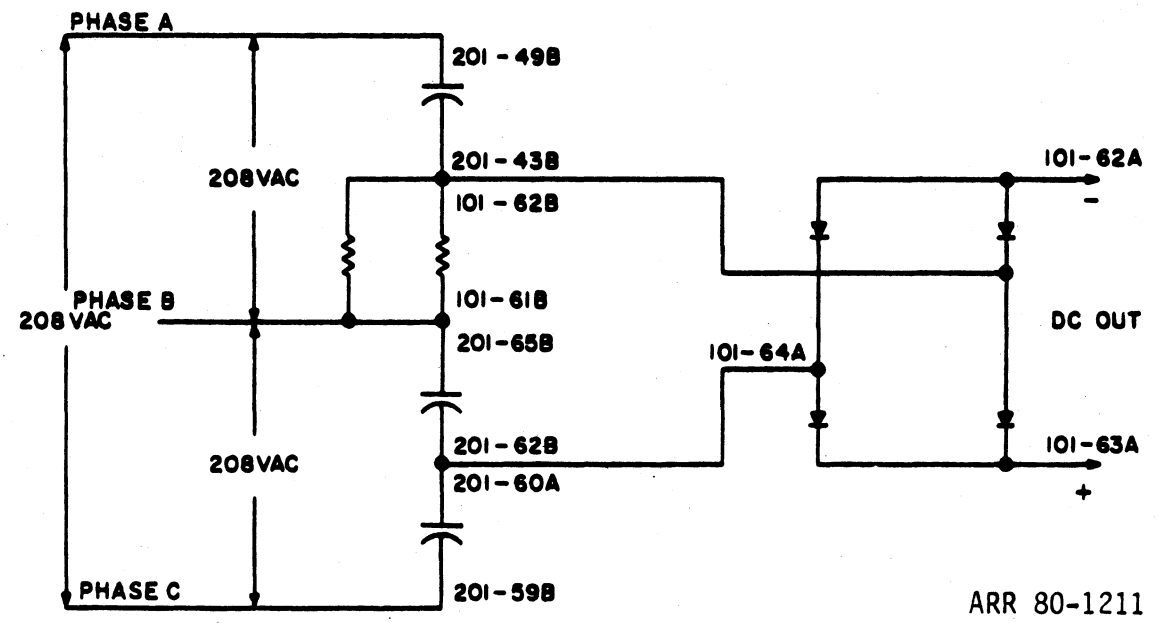
Environmental conditions	Affected circuit	Computer reaction: Disable Main Power Relay	Disable Memory Power	Phase Relay No. 1 Pickup	Phase Relay No. 2 Pickup	Voltage Warning Indicator	Temperature Warning Indicator
Primary phase rotation ACB					X		
Temperature in upper half of computer approaching high temp kickout point	High temp warning no. 1 circuit, temp warning inverter circuit						X
Internal air temperature approaching low temperature kickout point	Low temperature warning circuit temp, warning circuit, temp warning inverter circuit						X
Input line to neutral voltage less than 108 vac	Low voltage warning circuit, voltage warning inverter circuit					X	
Input line to neutral voltage more than 132 vac	High voltage warning circuit, voltage warning inverter circuit					X	

4-21. PHASE DETECTORS NO. 1 AND NO. 2

The input pins of the phase detectors are not shown on foldout 1. This is because the circuit is formed on two different boards. See figure 4-1 for mechanization of these circuits.



A. Phase detector 1.



B. Phase detector 2.

Figure 4-1. Phase Detectors 1 and 2.

4-22. INDICATORS ASSOCIATED WITH POWER CONTROL CIRCUITRY

a. TEMP Indicator (Fig. 4-2,A). The output from the Temp Warning Inverter, term TEMP, (FO-1) is in effect "anded" in network A board 402 with the 10-cycle oscillator output from network C board 323. If term TEMP is false (0 volts), the output of network A will be at a low voltage level and the TEMP indicator will light. If term TEMP is true, the output of network A will be at a low voltage level when the oscillator input is 0 and will be at a high voltage level when the oscillator input is true. Hence the indicator will flash.

b. TRANSIENT Indicator (Fig. 4-2,B). Theory of operation identical to that of TEMP indicator.

c. POWER READY Indicator (Fig. 4-2,C). The output term WI (FO-1) is in effect "nanded" in network A board 403 with term MOSCS. With the MARGINAL TEST switch in one of its ON positions and the output from network C, the 10-cycle oscillator term MOSCS is generated. With the MARGINAL TEST switch in the OFF position and with term WI true, the output of network A is at low potential and the POWER READY indicator will light (WI comes true approximately 20 seconds after turnon, para 4-17). With the MARGINAL TEST switch in one of its ON positions and with WI true, the POWER READY indicator will flash.

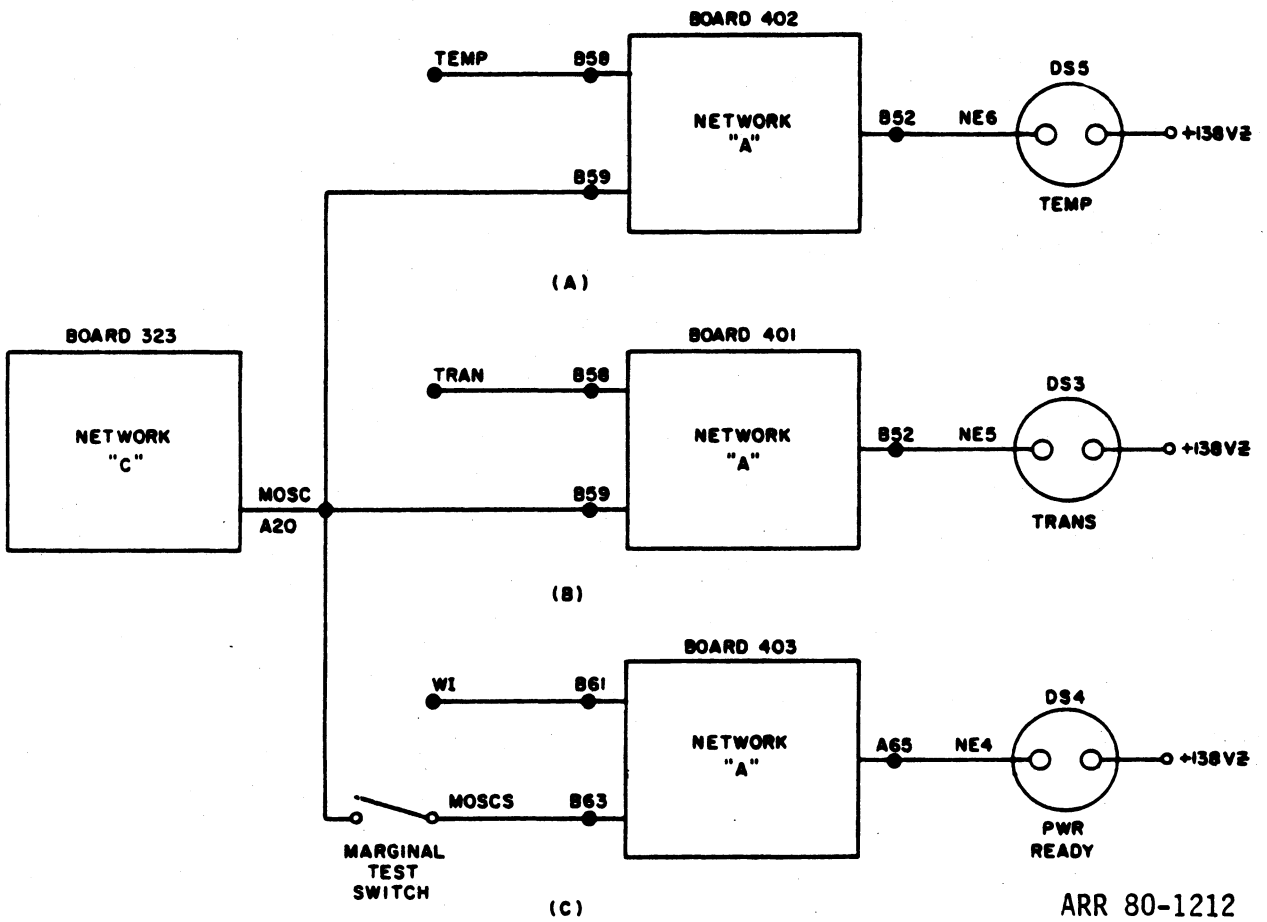


Figure 4-2. Mechanization of Indicator Circuitry.

Section III. Power Supply

4-23. SCOPE

This section provides information in determining and isolating malfunctions that occur in the power supply circuitry of the computer.

4-24. SETUP SWITCH IDENTIFICATION

In the schematic diagrams of this section, the setup switches are given a letter-number designation. This code is explained in figure 4-30.

4-25. INDICATOR LAMP IDENTIFICATION

In the schematic diagrams of this section, the indicator lamps are given a letter-number designation. This code is explained in figure 4-71.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION

To isolate a power supply malfunction or interconnecting wiring problem utilize block diagrams in figure 4-3 thru 4-16. Replace one or more associated circuit boards within the malfunctioning supply. Refer to problem example below.

CAUTION

The computer must be in the deenergized state during circuit board removal and installation.

a. Symptom. FADAC does not respond to the depression of any of the setup switches.

b. Procedure. The FALT is cabled to the computer to begin testing. The first step in testing the FADAC as prescribed in TM 9-1220-221-34/2 is monitoring of external voltages using the FALT. In monitoring the negative voltages the -10-volt supply is found to be reading high. Reference to figure 4-13 shows the circuit boards utilized in this supply. Any one, or combination of the circuit boards shown, could cause the malfunction. If the symptoms remain after board replacement, a transformer and bias voltage check may be made. Refer to table 4-4 for transformer voltage readings.

CAUTION

Due to the proximity of the circuit board connector pins, extreme caution must be exercised when voltage probing.

NOTE

The FADAC 66 volt Zener Diode output can be monitored using the voltage monitor on the FALT. This voltage may be measured at 139 E7 with a multimeter.

Wire list (TM 9-1220-221-34/6) and/or component list (TM 9-1220-221-34/7) should be used to trace wiring.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION--Continued

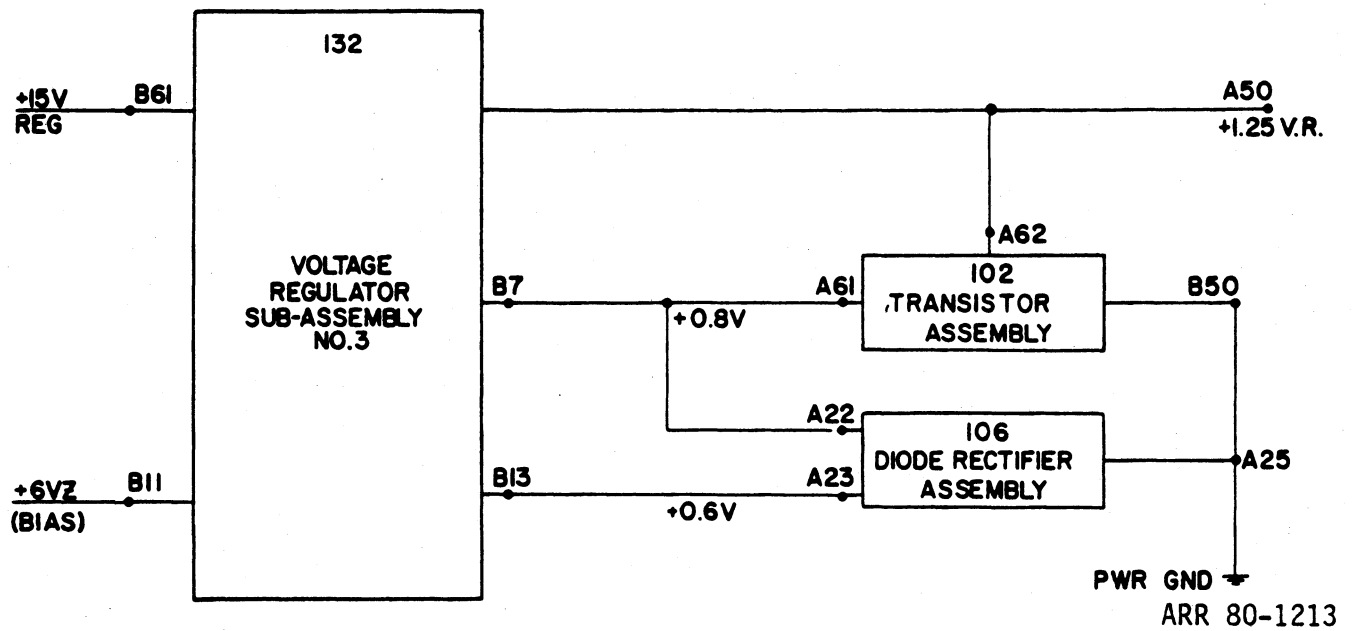


Figure 4-3. Block Diagram ±1.25V Regulated Power Supplies.

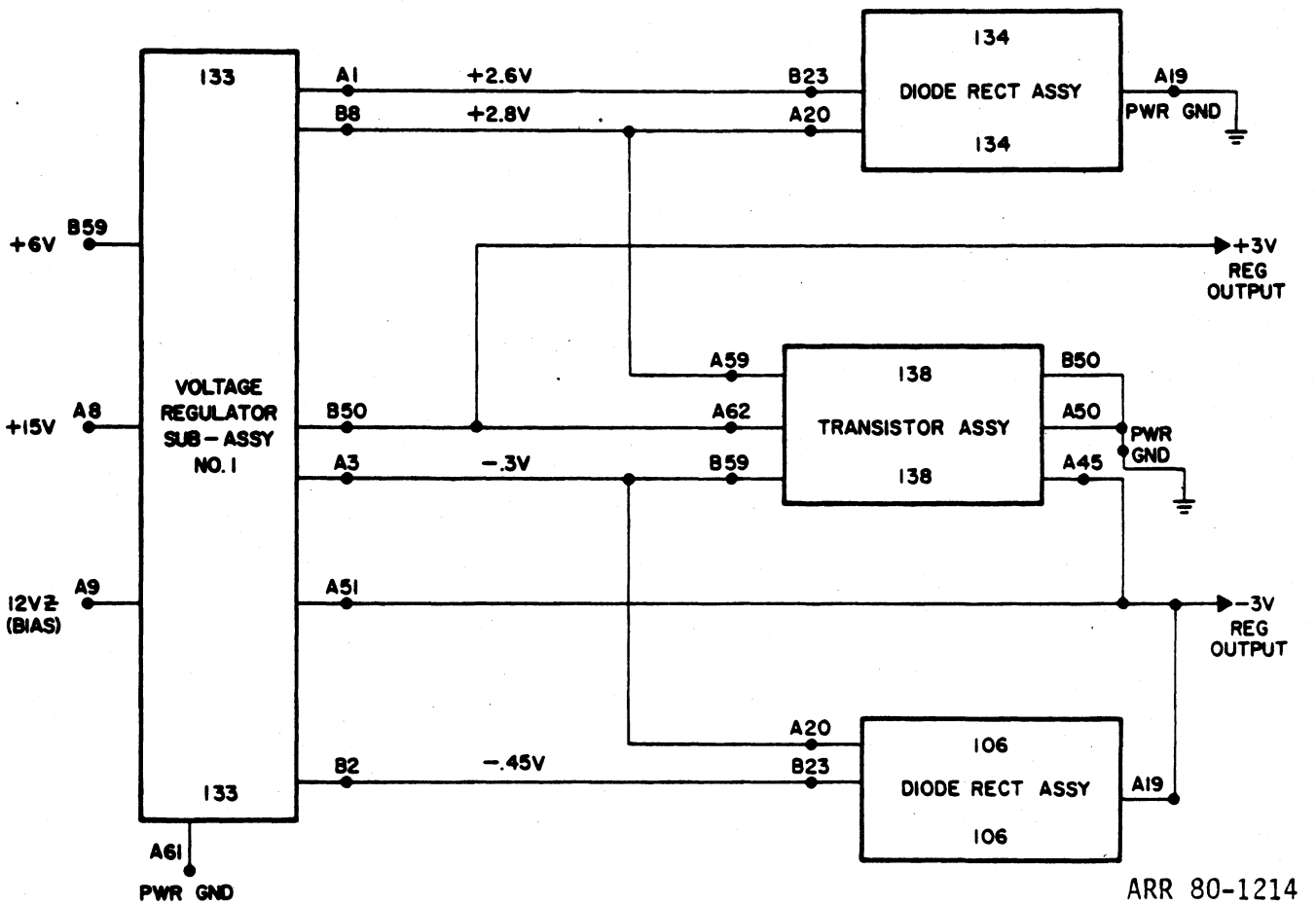
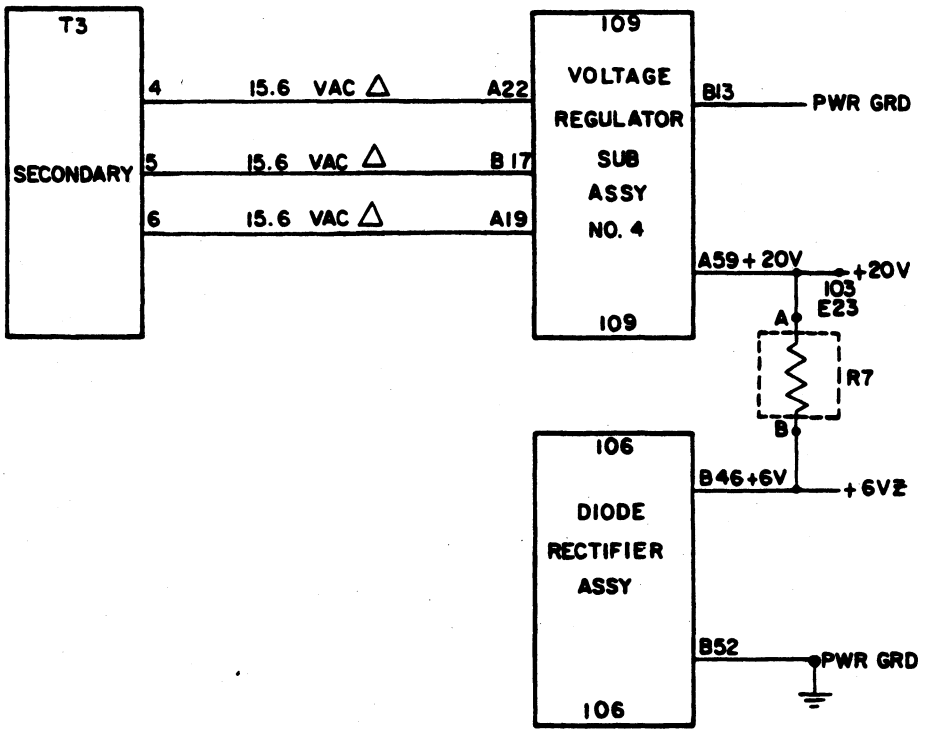


Figure 4-4. Block Diagram ±3V Regulated Power Supplies.



ARR 80-1215

Figure 4-5. Block Diagram +6VΣ, ±20V Power Supplies.

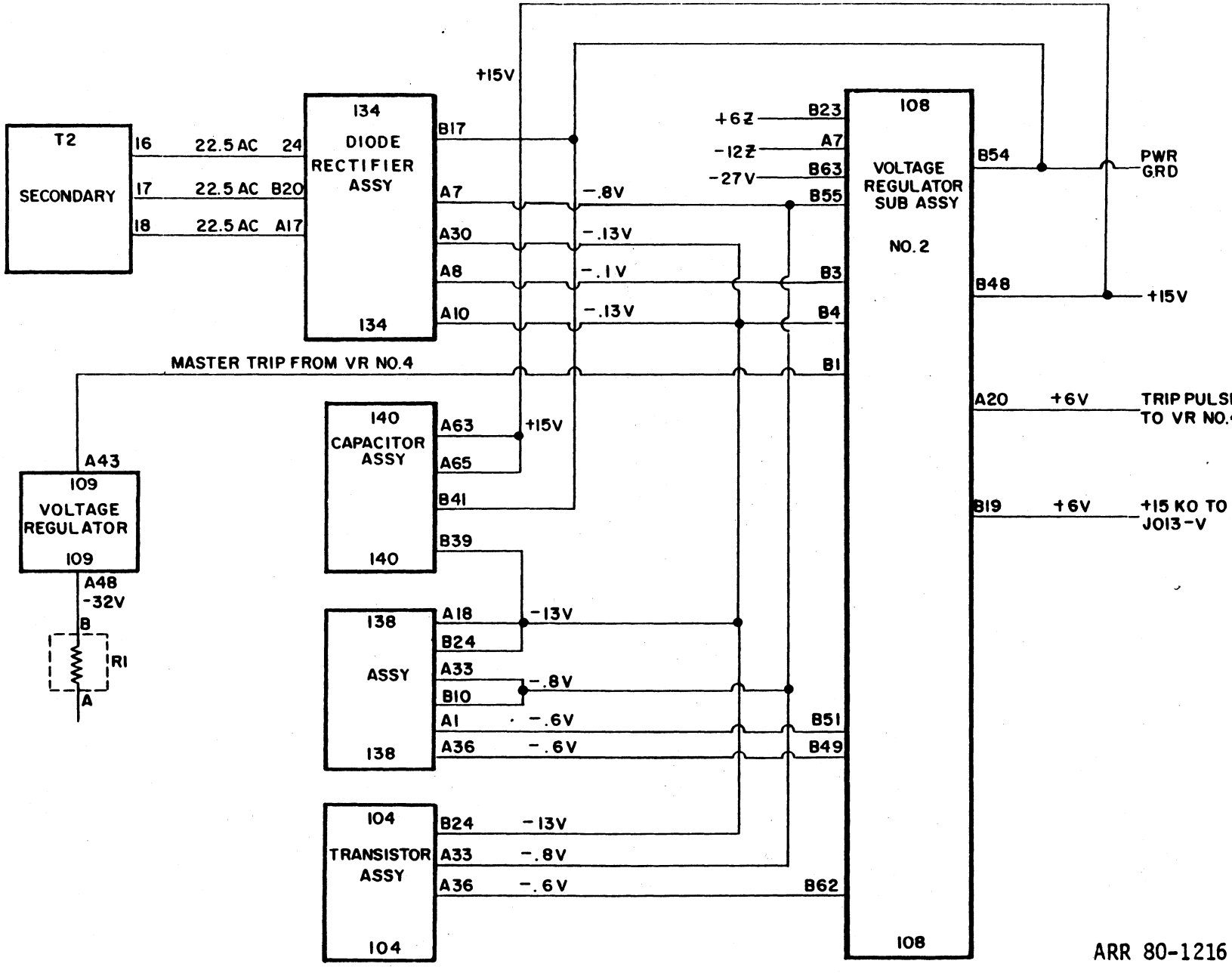


Figure 4-6. Block Diagram +15V Series Regulated Power Supply.

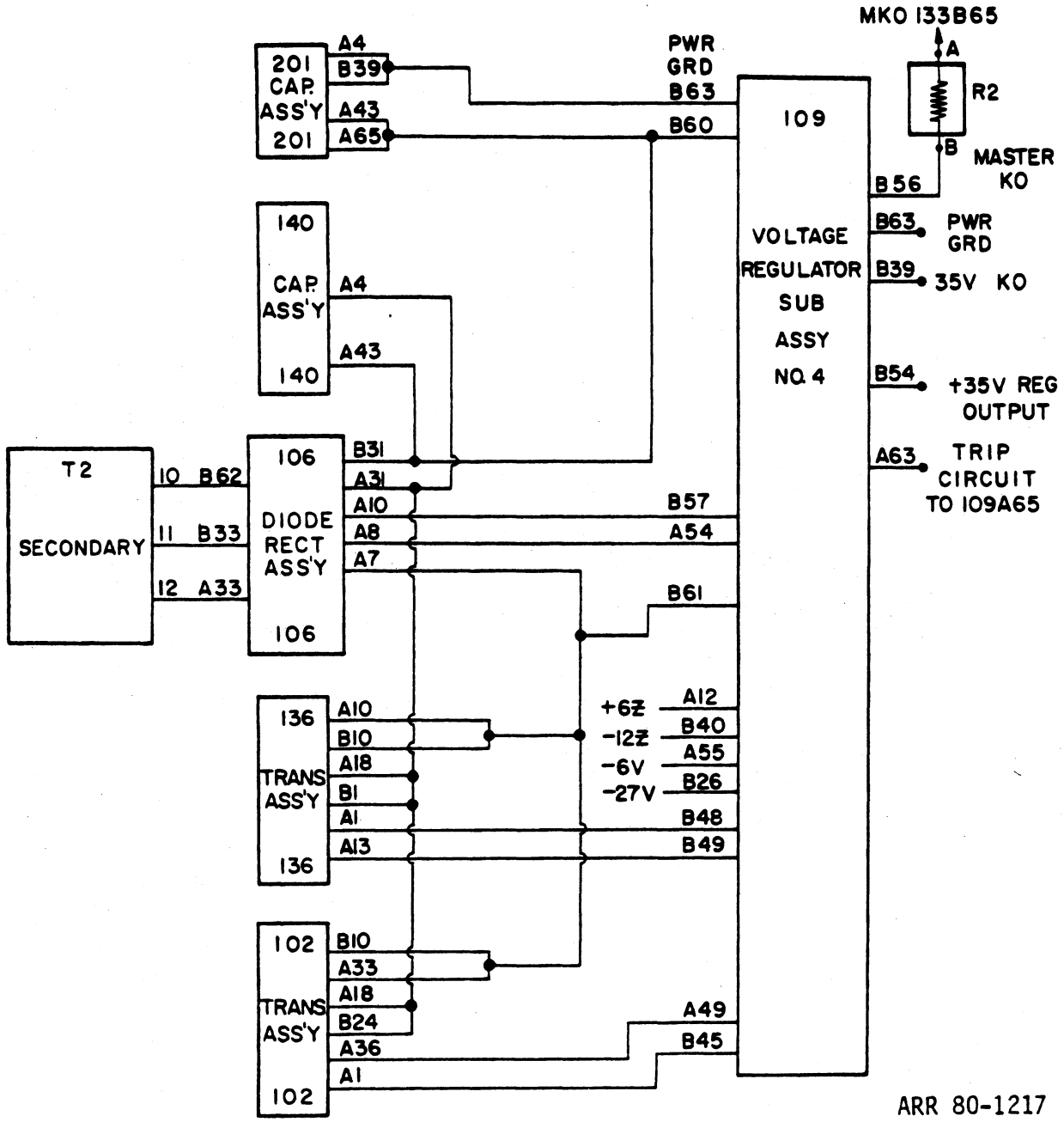


Figure 4-7. Block Diagram +35V Power Supply.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION--Continued

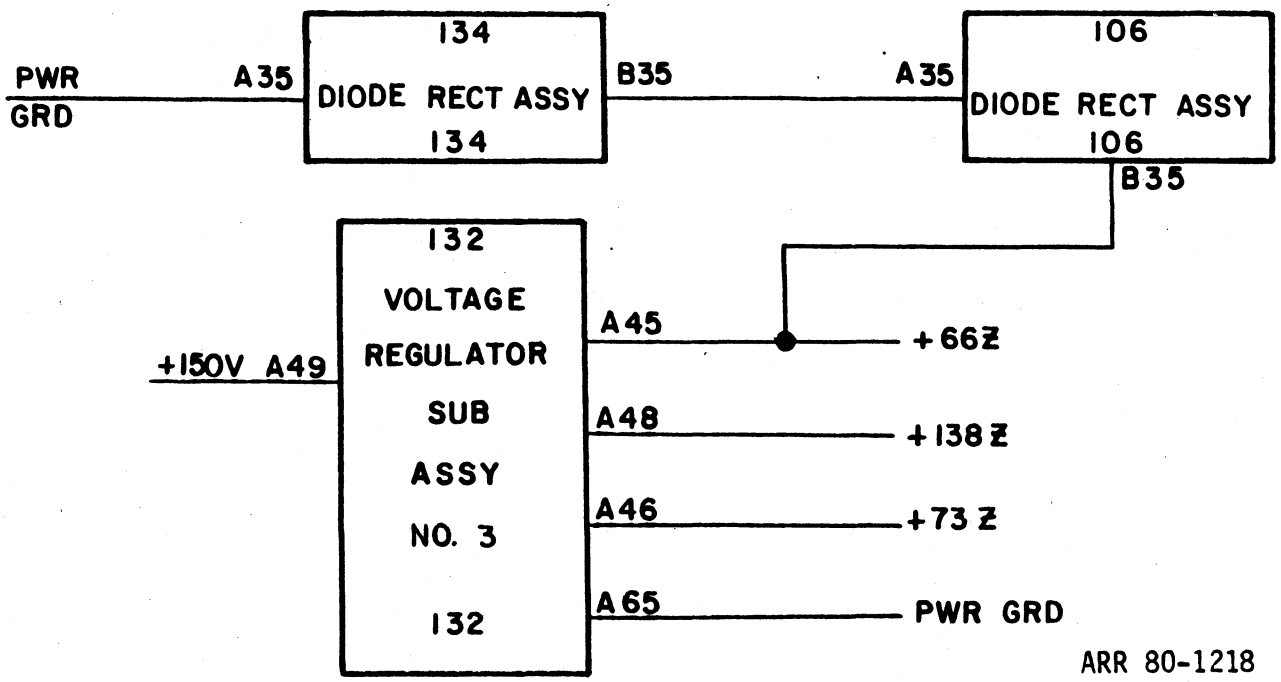


Figure 4-8. Block Diagram +66VZ, +138VZ, +73VZ Power Supplies.

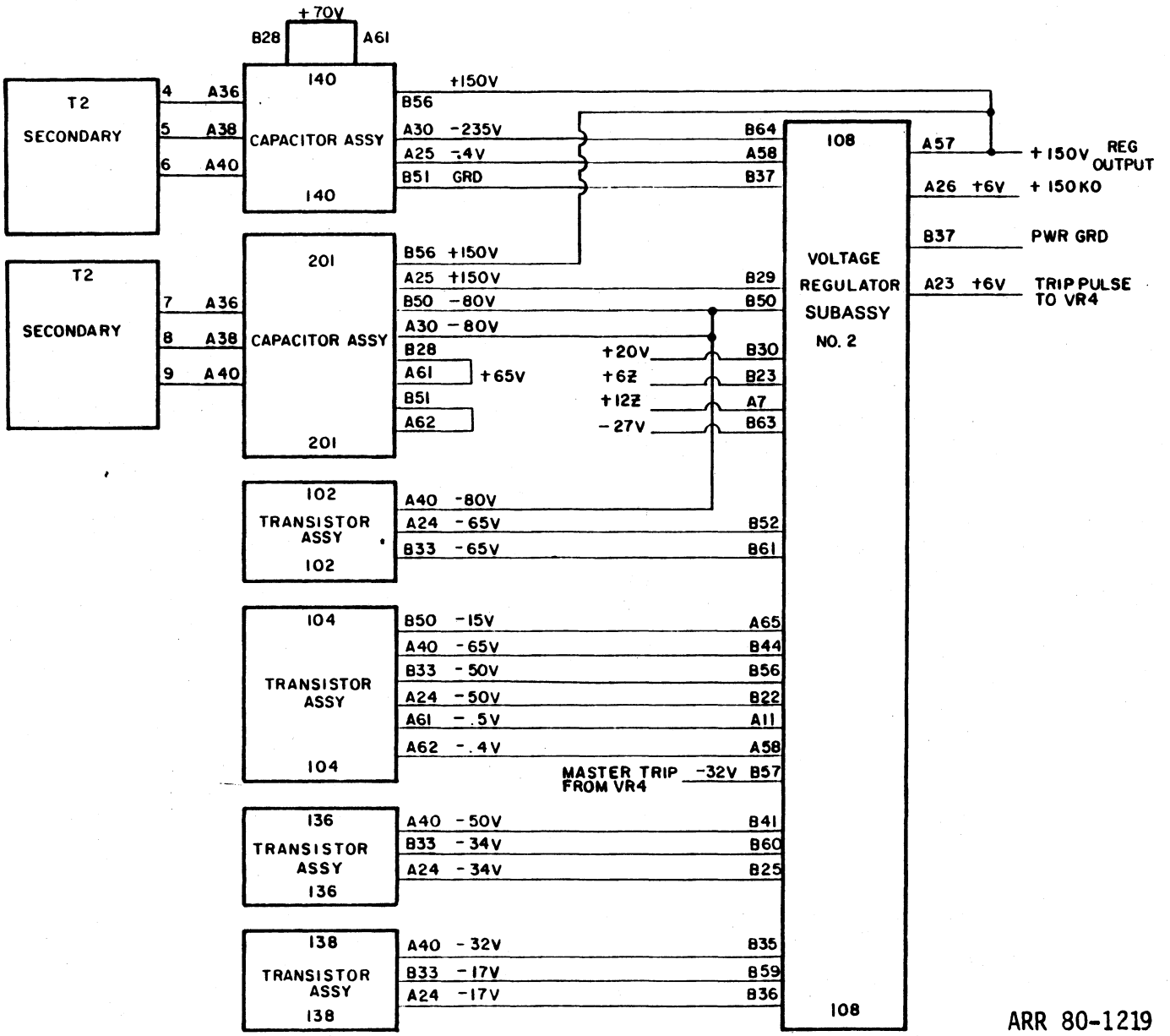


Figure 4-9. Block Diagram +150V Regulated Power Supply.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION--Continued

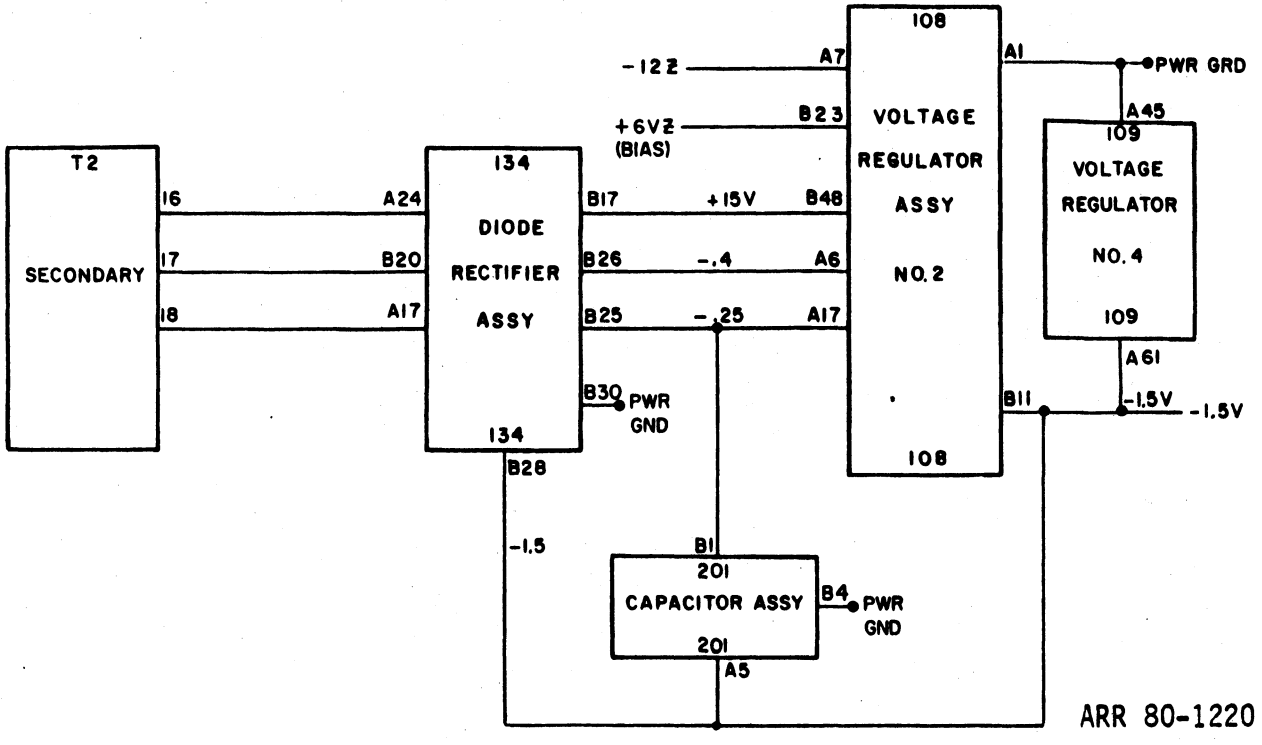


Figure 4-10. Block Diagram -1.5V Shunt Regulated Power Supply.

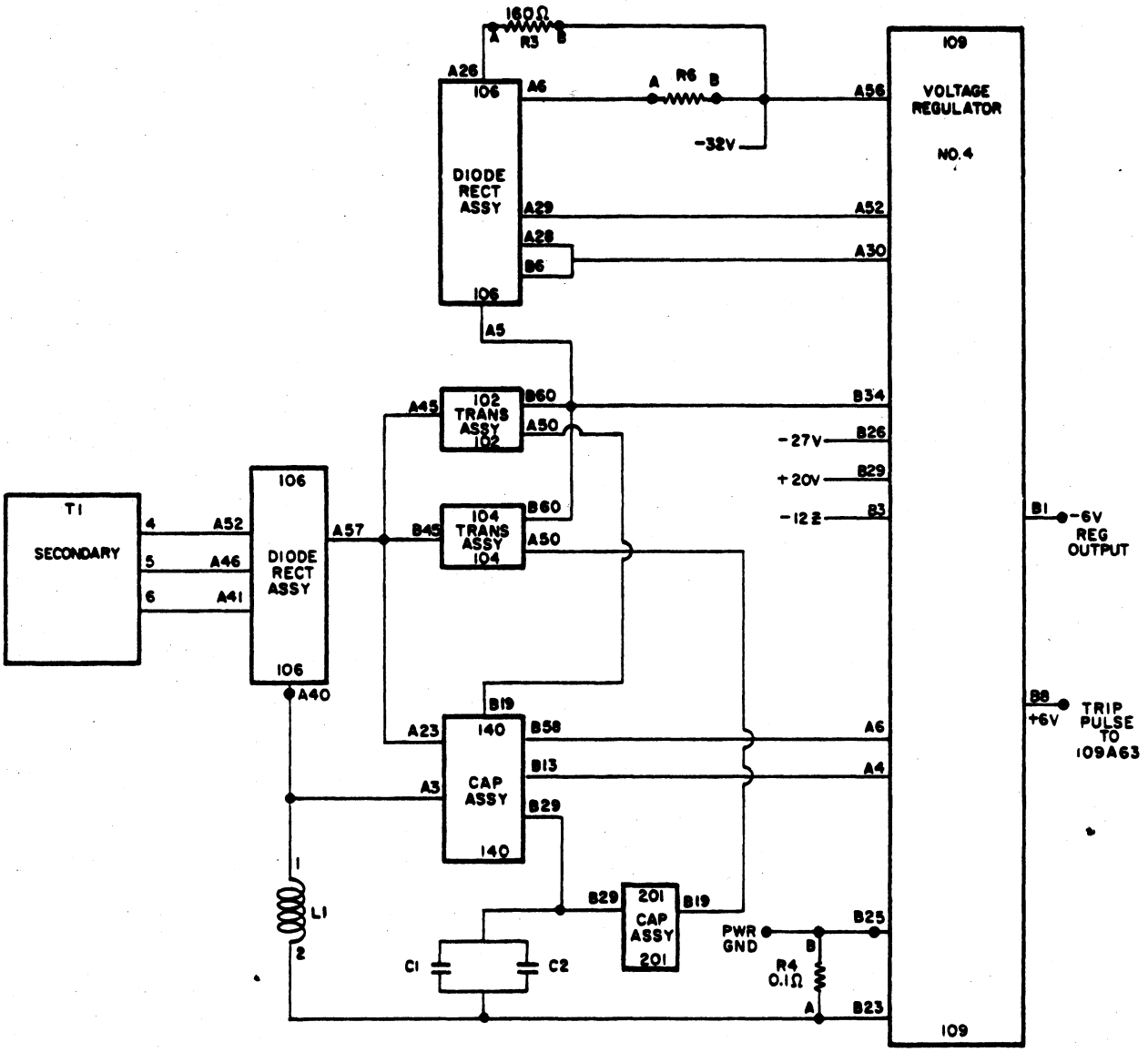
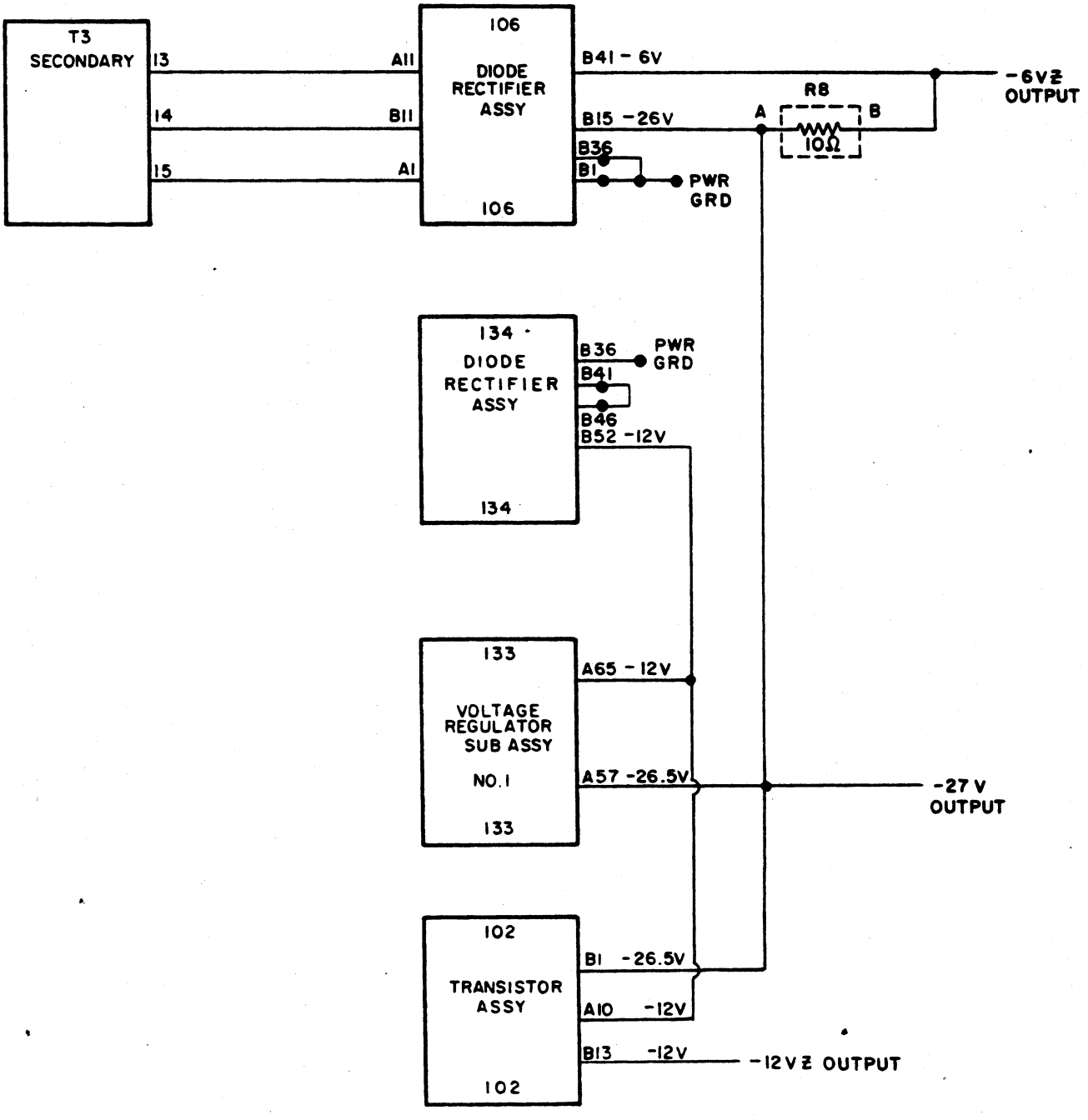


Figure 4-11. Block Diagram -6V Regulated Power Supply.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION--Continued



ARR 80-1222

Figure 4-12. Block Diagram -6VZ, -12VZ, -27V Power Supplies.

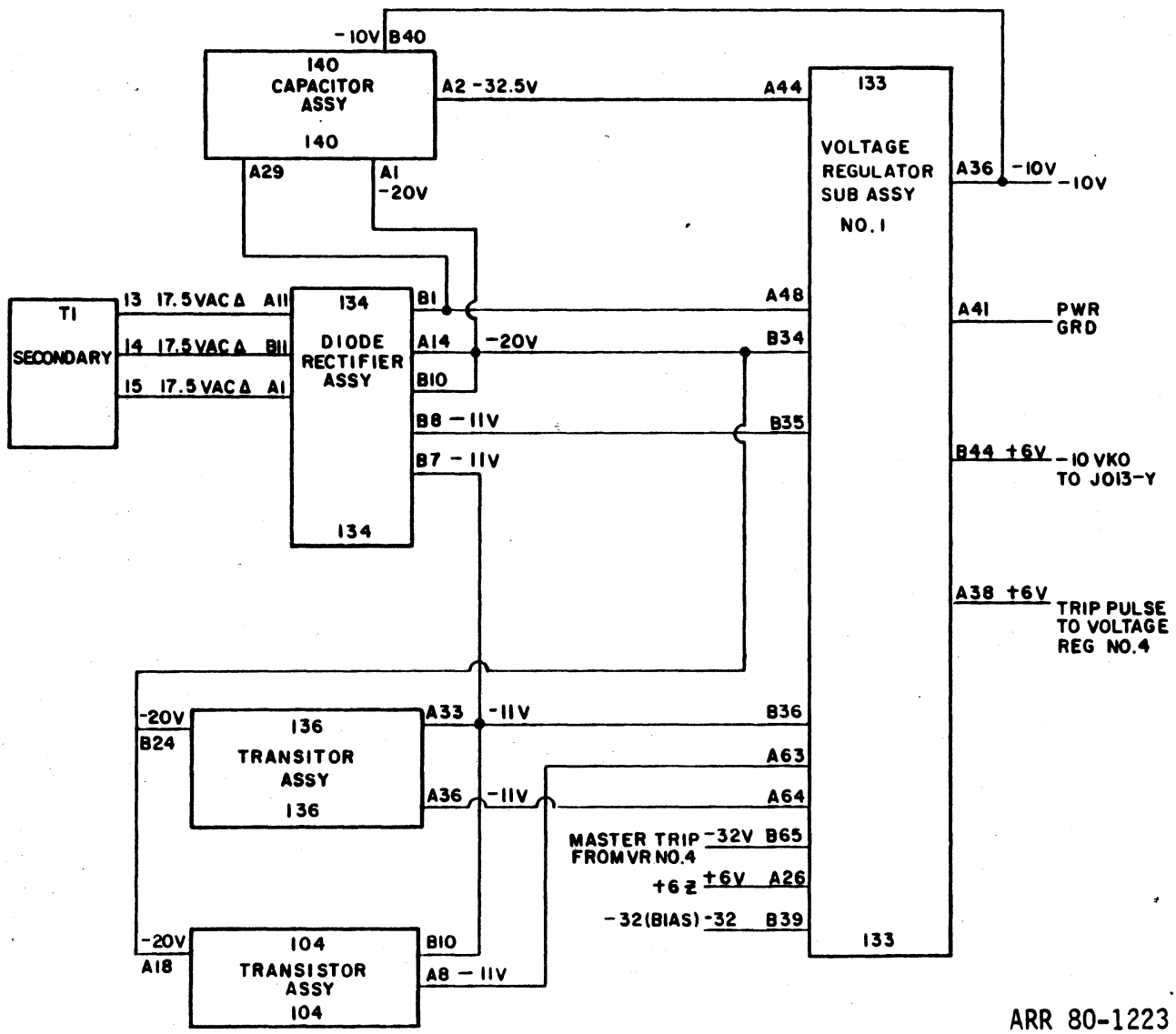


Figure 4-13. Block Diagram -10V Regulated Power Supply.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION--Continued

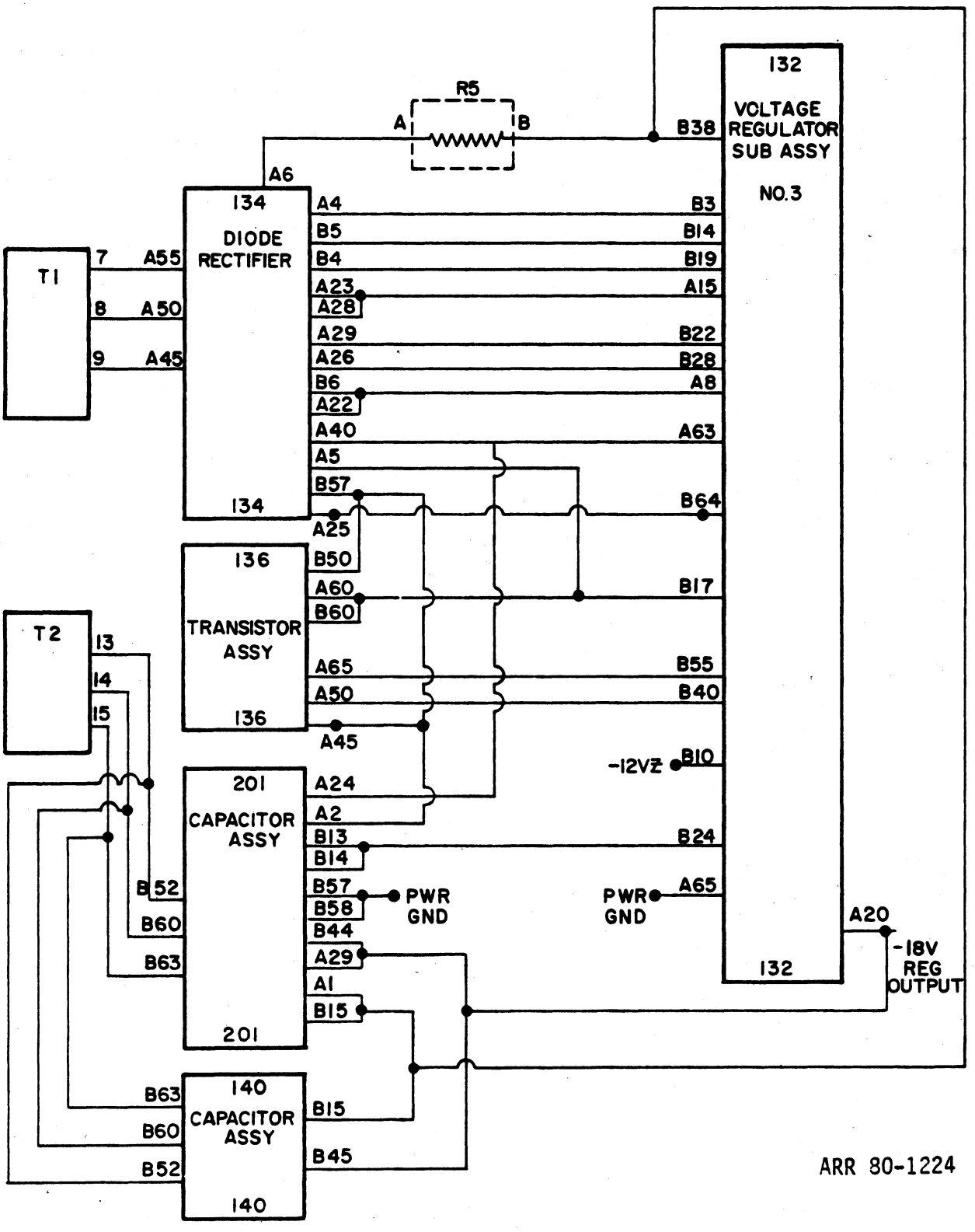


Figure 4-14. Block Diagram -18V Regulated Power Supply.

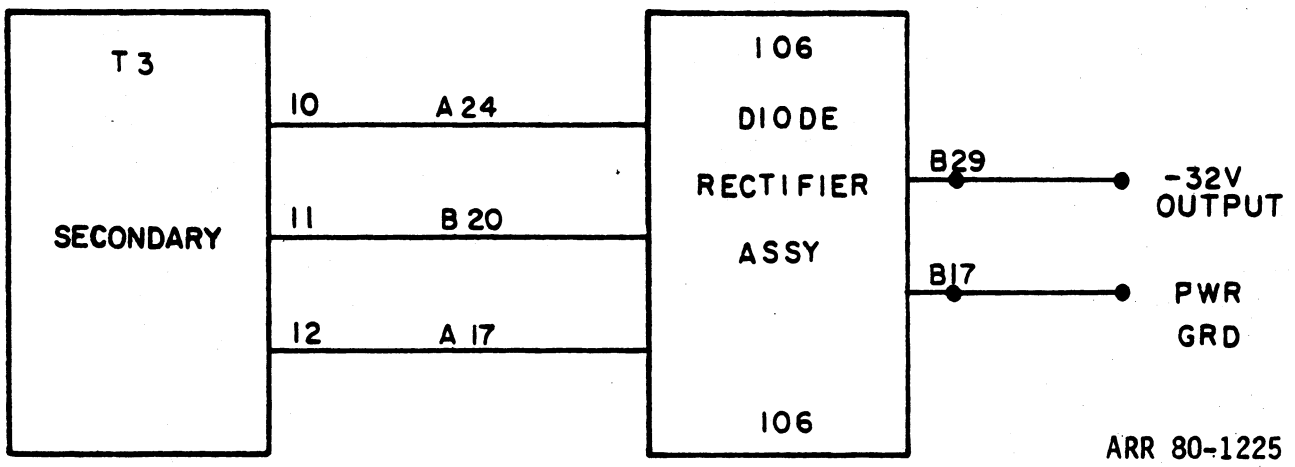


Figure 4-15. Block Diagram -32V Power Supply.

4-26. PROCEDURE NO. 1 FOR MALFUNCTION ISOLATION--Continued

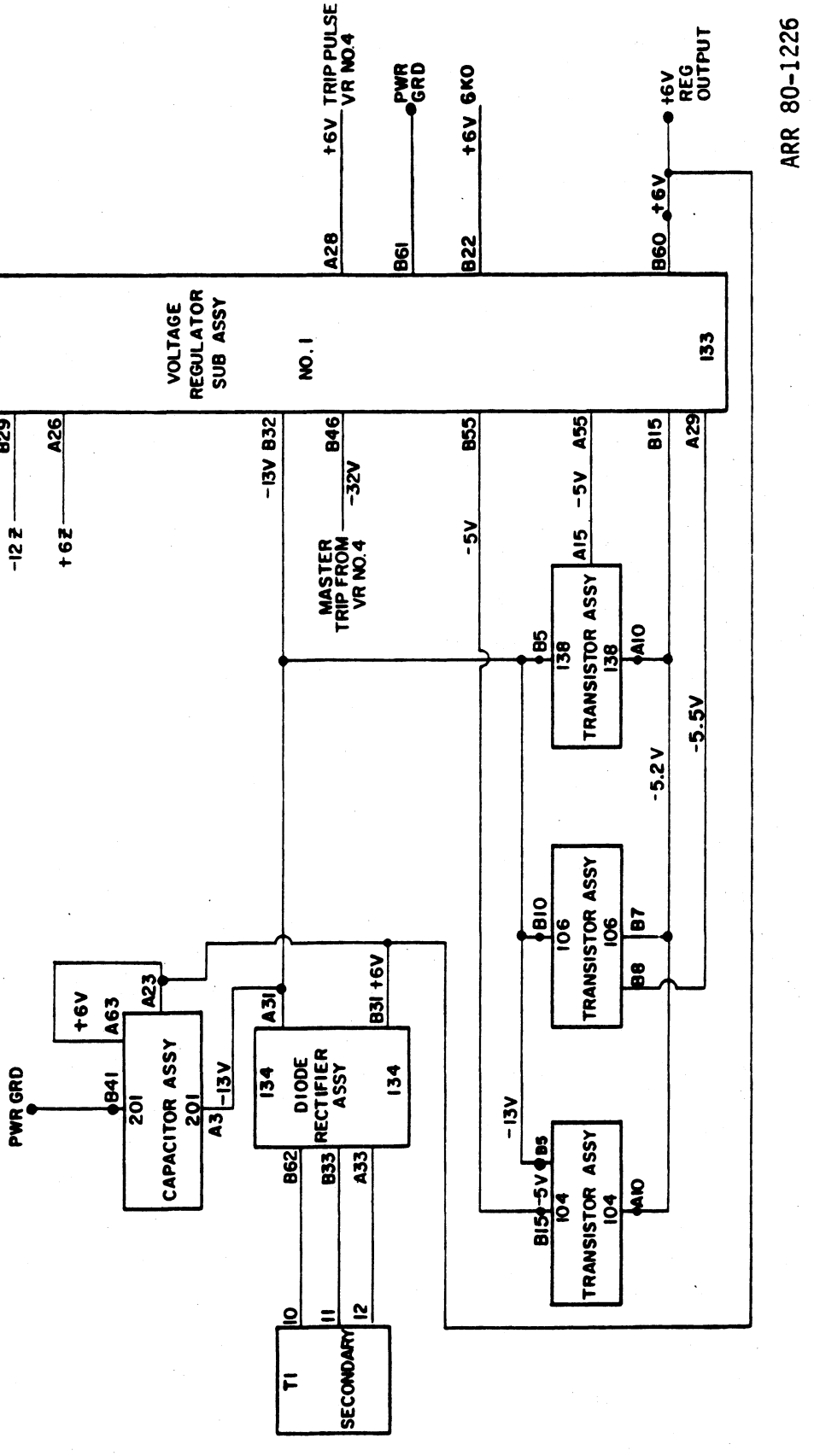


Figure 4-16. Block Diagram +6V KO Power Supply and Master Trip Circuit.

Table 4-4. Transformer Voltages

T1		T2		T3		T4	
Terminal	Voltage	Terminal	Voltage	Terminal	Voltage	Terminal	Voltage
1-3	208 Y	1-3	208 Y	1-3	208 Y	1	Chassis Ground
4-6	13.1	4-6	177	4-6	15.5	2	120 v
7-9	30.4	7-9	177	7-9	6.3	3, 4	7 v
10-12	15.6	10-12	44	10-12	24.3	5, 6	7 v
13-15	16.1	13-15	11.2	13-15	20.6	7, 8	7 v
16	Shd Gnd	16-18	21.7	16	Shd Gnd	9, 10	7 v
17	Core Gnd	19	Shd Gnd	17	Core Gnd	11, 12	7 v
		20	Core Gnd			13, 14	7 v
						15, 16	7 v
						17	Shd Gnd
						18	Core Gnd

4-27. MARGINAL TEST SWITCH

a. Marginal testing of the FADAC or FALT may be accomplished at the discretion of the operator and should be used in the daily performance check.

b. The marginal testing is performed by setting the MARGINAL TEST switch in each of the five positions for each operation. In each position the required dc power supply levels are statically offset by ±5 percent; the clock pulse is statically made wider or narrower by ±0.2 microseconds. Through the use of the MARGINAL TEST switch, intermittent conditions or marginal components may be detected.

c. Table 4-5 indicates circuit boards and voltage levels (regulated) applied to each board.

d. Table 4-6 shows those power supply levels affected by the MARGINAL TEST switch. Each position of the switch indicates voltage levels increased by 5 percent by a plus sign (+); decrease in levels by 5 percent with a minus sign (-).

Table 4-5. Power Supply Voltage Routing

	Negative									Positive									
	1.5	3	6	6Z	10	12Z	18	27	32	1.25	3	6	6Z	15	20	35	66Z	73Z	138Z	150
Capacitor Assy					X															
Diode Rectifier								•												
Logic Driver	X		X				X							X						
Logic Flip-Flop			X				X			X		X								
Network A	X	X	X				X				X	X		X			X			X
Network B	X	X	X				X					X		X			X	X	X	X
Network C	X	X	X		X		X			X	X	X		X		X	X		X	X
Power Control A						X							X							
Power Control B						X							X							
Power Control C		X				X	X						X	X		X				
Pulse Generator		X	X		X		X			X	X	X		X						
Read Amplifier	X	X	X		X		X		•	X		X		X						
Read Switch		X	X		X		X			X		X								
Transistors Assy																				
Voltage Regulator 1						X		X					X	X	.					
Voltage Regulator 2						X		X					X		X					
Voltage Regulator 3				X		X	X	X					X	X						X
Voltage Regulator 4				X		X		X	X				X		X					
Write Amplifier	X		X		X		X			X		X		X		X				
Write Switch		X	X		X		X							X		X				
Keyboard					X		X		X											
Matrix					X									X						
Mechanical Reader					X				X											
Memory														X						

Table 4-6. Power Supply Levels Affected By Marginal Test Switch

Switch position	+1.25	+6	+15	+35	-6	-10	-18	Clock
1	-	+	+	-	-	-	-	Wide
2	+	-	-	+	+	+	+	Narrow
3	+	-	+	-	+	-	-	Wide
4	-	-	-	+	-	-	-	Narrow
5	-	-	+	-	+	+	+	Wide

4-28. PROCEDURE NO. 2 FOR MALFUNCTION ISOLATION

This procedure is used to isolate an excessive load to the power supply caused by a malfunction of one of the circuit boards or other equipment utilizing that particular voltage or a wiring short.

a. Method. Systematically remove and replace all circuit boards utilizing this supply voltage. Table 4-5 shows the general distribution of the power supplies.

NOTE

Refer to the wire list (TM 9-1220-221-34/6) to determine the specific circuit board numbers that provide the load for each power supply. Short circuits due to wiring require the use of the wire list and/or component list (TM 9-1220-221-34/7) utilizing conventional troubleshooting methods.

b. Problem Example.

(1) Symptom. FADAC does not respond to the depression of any setup switches.

(2) Procedure. Following the isolation procedure outlined in paragraph 4-26b it is noted that the -10-volt supply is low. After replacing the associated power supply circuit boards the trouble still exists. At this time the computer is deenergized and the load is checked by removing not more than three circuit boards at a time. Refer to the wire list to determine circuit boards providing the load to the supply. With the boards removed, the FADAC is reenergized and checked for a change in performance. If the symptom persists, reinsert the three circuit boards and remove three more, continuing in this manner until the defective circuit board or other load component is isolated.

4-29. POWER SUPPLY PROTECTION CIRCUITS

a. A master kickout (MKO) circuit located on voltage regulator no. 4 circuit board is utilized to prevent overload damage to the power supply regulators. This circuit is connected to the +150-, +35-, +15-, +6-, -18-, -10-, and -6-volt regulators. Whenever an overcurrent is sensed by any one of the above regulators, the MKO circuit will energize and turn off all the regulators. The MKO circuit with the associated power supply regulator inputs is in figure 4-17.

b. Should one of the power supply regulators experience an overload condition it will cause the input to the MKO circuit, which is normally +6 volts, to change to 0 volts. This will result in a +20-volt output, rather than the normal -32-volt output, from the MKO circuit. All of the power supply regulators will turn off. In addition all of the indicators on the control panel will go off. The MKO circuit is reset by deenergizing the computer. If, upon reenergizing the FADAC, the trouble symptoms persist, either the MKO circuit located on regulator no. 4 board is defective, one or more of the power supply boards are defective, or there is an excessive load to the power supply caused by a malfunction of one of the circuit boards or other equipment utilizing one of the power supply voltages. Use malfunction isolation procedures no. 1 and/or no. 2 to find and correct the malfunction.

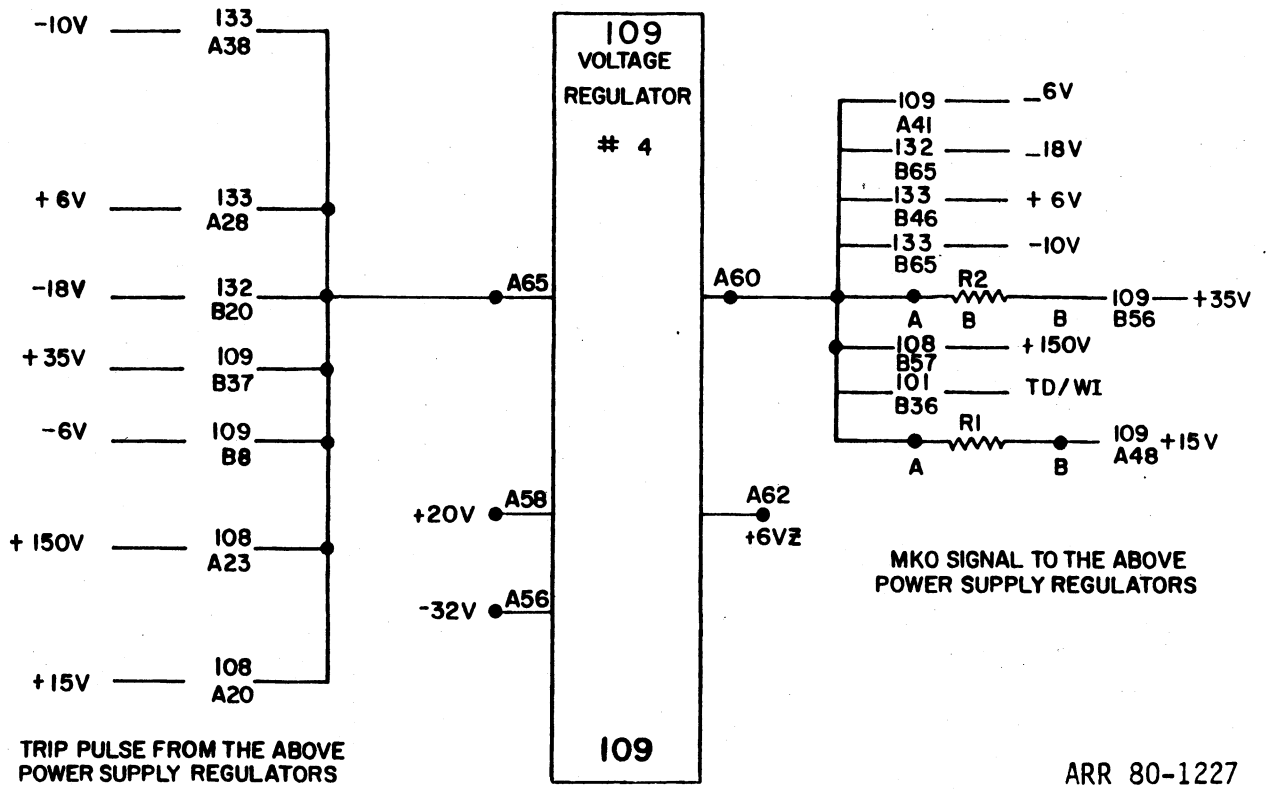


Figure 4-17. Master Kickout Circuit.

Section IV. Malfunction Isolation Using the FALT and Associated Test Tapes

4-30. GENERAL

This section covers malfunction isolation using the FALT and test tapes B thru E. Technical manuals containing test tape program printouts are TM 9-1220-221-34/2, B test tape; TM 9-1220-221-34/3, C test tape; TM 9-1220-221-34/4, D test tape; and TM 9-1220-221-34/5, E test tape. The maintenance technician must use these test tapes in the above order when testing the FADAC with the FALT. After an error has been corrected by replacement of a board, it is advisable to repeat all test tapes, thereby ensuring that no trouble exists on the new board.

4-31. LOGIC TROUBLESHOOTING

The length of this section demands that its contents be explained in order to save the maintenance technician much time and inconvenience locating the information sought. The section is broken down as follows:

a. Paragraphs 4-22 thru 4-35 describe each of the test tapes (B thru E), their function, which circuits are being tested, and how these tests are performed.

b. Paragraphs 4-36 thru 4-39 give information regarding terms pertinent to the FALT. This includes computer F1T and F0T response lines, flip-flop address and response lines, and FALT exciter flip-flops.

c. Paragraphs 4-40 thru 4-47 give troubleshooting procedures for errors detected by FALT front panel indications. This also includes logic malfunction isolation.

d. Paragraphs 4-48 thru 4-51 give general information for malfunction isolation. This includes location of pins on printed circuit board connector, F1T and F0T line troubleshooting, logic driver troubleshooting, primary "and" gate troubleshooting, and troubleshooting flip-flop logic that has failed.

4-32. DESCRIPTION OF B TEST TAPE

a. General. Before beginning a logic test of the computer it will be necessary to test the address and response lines for each flip-flop circuit in the computer. In order to logic test the computer, all logic equations must be checked. Refer to TM 9-1220-221-34/1/1 for lists of computer logic equations. Logic equations are composed of the outputs of one or more flip-flop circuits and since the FALT will be used to set these flip-flop circuits, the ability of the FALT to address and test these flip-flop circuits should be checked.

4-32. DESCRIPTION OF B TEST TAPE--Continued

b. Flip-Flops.

(1) Marker 001. As an example, flip-flops D7 and CN6 are tested during marker 001 on the B test tape. Refer to TM 9-1220-221-34/2 for printout of B test tape. Both of these flip-flops are located on circuit board 240. Printed circuit boards 101 and 432 are also called out in the test tape listing. Circuit board 101 contains the "or" diode circuit for F1T1 and FOT1 lines. Refer to paragraph 4-36 for a description of computer F1T and FOT lines. The pulse generator board no. 432 provides the clock timing. The B test tape then continues by testing the remaining flip-flops connected to F1T1 and FOT1 lines.

```
001     .....................................................OV
        Boards 101, 240, 432
        1SA    1TF    07    CN6    OSA    OTF    D7    CN6
        1V
```

(2) Marker 011. Beginning at marker 011 the flip-flops connected to F1T2 and FOT2 are tested. Since different "or" diodes are now involved, printed circuit board 101 is again called out in the test tape listing at marker 011. The B test tape continues by testing the remaining flip-flops in the FADAC according to their F1T and FOT lines. As the first flip-flops of new F1T and FOT lines are tested, the printed circuit board containing the "or" diode is called out in the test tape listing.

```
001     .....................................................OV
        Boards 101, 229
        1SA    1TF    C4    1D    OSA    OTF    C4    ID
        1V
```

(3) Marker 031. Marker 031 tests flip-flop MP and OFLO which are the first flip-flops of the F1T4 and FOT4 lines. The "or" diode for the F1T4 line is located on printed circuit board 433 which is called out in the test tape listing.

```
031     .....................................................OV
        Boards 433, 341
        1SA    1TF    MP    OFLO
        1V
```

(4) Marker 061. The response lines for the read and write flip-flops are tested in the B test tape starting at marker 061. Write flip-flops are located on write amplifier boards and read flip-flops are located on read switch boards.

```
061     .....................................................OV
        Board 439
        1SA    1TF     .     QP    OSA    OTF     .     QP
        1V
```

(5) Marker 066. Timing for the read flip-flops is provided by the strobe pulse which is generated on the network C board 323 which is called out in the B test tape listing at marker 066 where the first read flip-flop is tested. The main memory write flip-flops MW0 and MW1 are not tested at this time; main memory read flip-flops MMN and MMP are tested at marker 078 and 079. The time delay/write inhibit flip-flop, TDWI, is tested at marker 077.

NOTE

The time delay/write inhibit flip-flop is referred to as the PS flip-flop in all test tape listings.

```
066     .....................................................OV
        Board 303
        1SA     1TF     S     0SA     0TF     S
        1V
```

(6) Marker 080. At marker 080 the B test tape begins the testing of flip-flop addresses. Each flip-flop in the FADAC has a separate address and whenever any one flip-flop is addressed and set, no other flip-flop in the computer should be affected. For example, at marker 080 all flip-flops are one set by the 1SA command; flip-flop S is then addressed and zero set. Since flip-flop S is the only one that has been addressed, all other flip-flops should remain one set. The B test tape continues by one testing all the flip-flops whose address is similar, to ensure that they remained one set when the S flip-flop was addressed and zero set. The S flip-flop address is DUR02, DLR33; the RM flip-flop address is DUR03, DLR33; both S and RM have the same DLR address but different DUR addresses. However, if the DUR address diode CR65 located on circuit board 307 was open, the address gate would not be held false and the flip-flop RM would change states whenever the S flip-flop was addressed. The remaining flip-flops whose address is similar to the S flip-flop are also one tested to ensure they have not zero set when flip-flop S was addressed; L0 flip-flop is one tested at marker 081; flip-flop X0 is one tested at marker 082 and so on until all flip-flops with addresses similar to S have been tested. The B test tape continues by selecting one flip-flop, zero setting it, then one testing flip-flops with similar addresses. For a complete description of flip-flop addressing refer to paragraph 4-37.

```
080     .....................................................OV
        Board 307
        1SA     S     1TF     RM
        1V
```

4-32. DESCRIPTION OF B TEST TAPE--Continued

(7) Marker 265. An additional test of flip-flop addressing begins at marker 265; here the DU address diodes are being tested. The two flip-flop circuits located on any logic flip-flop circuit board have a common DL address. For example, flip-flops D7 and CN6, located on board 240, have the same DL address of 20 but different DU addresses. In marker 265 flip-flop D7 is zero set and flip-flop CN6 is one tested to verify it has not changed states. If, however, address diode CR60, located on board 240, was open, CN6 would have zero set. Also, an error indication would have appeared on the FALT. The DU address diode (CR59) for the D7 flip-flop is tested by addressing and zero setting CN6 and then one testing D7 to ensure it has not been zero set. All DU address diodes are tested by the B test tape in this manner.

265 .....OV

Board 240							
1SA	D7	1TF	CN6	1SA	CN6	1TF	D7
OSA	D7	OTF	CN6	OSA	CN6	OTF	D7
1V							

(8) Marker 347. After completing marker 347, the F1T and FOT response lines and "or" diodes have been tested; the DU/DL address lines have also been tested. Therefore, the flip-flop circuits can now be used to logic test the FADAC. The first logic circuits to be tested by the B test tape are the addressable logic drivers.

NOTE

Addressable logic drivers are those logic driver circuits whose outputs are directly connected to the FALT through the external test cables.

347										
	CN3	CR7	CR5	CR3	C7	C5	C3	DC	DSH	D8
	D6	DA8	DA6	DA4	DA2	D4	D2	D	FS	IC
	IP	LC	LX	MN	NC	CN2	OB6	OB4	OB2	OP3
	OP1	05	03	PE	PP	QX	RX	TP	XD	X2
	CLC	DP	L32	QP	XP	DO	LO	RO	QO	S
	MMN	.	.	.	.	.	.	.	.	.

c. Logic Drivers. There are a total of 85 logic drivers in the computer. Each of the four logic driver circuit boards contain 20 logic driver circuits; the remaining five logic drivers are located on the network A circuit board.

(1) Marker 348.

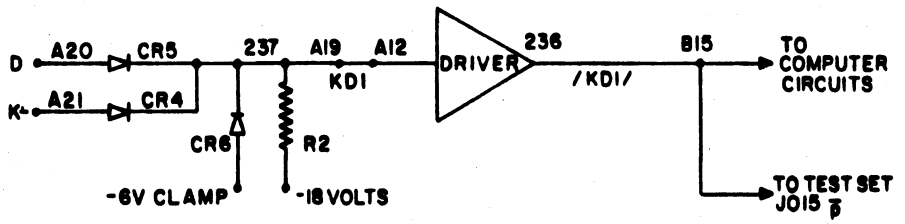
(a) The first logic driver to be tested is /KD1/ which is tested during marker 348. The logic for KD1 driver is reproduced below.

/KD1/ = + K' D 236 B15

NOTE

The circuit board and output connector pin is also included in the table of logic equations. The basic circuit for all flip-flop equations, including logic driver and primary gate circuits have been mechanized and are available in TM 9-1220-221-34/1/1.

(b) With reference to the schematic diagram (fig. 4-18) the "and" gate for the driver circuit is composed of diodes CR4 and CR5 located on circuit board 237. Flip-flop outputs D and K- are connected to pins A20 and A21 respectively. A clamp is provided to prevent damage to the driver circuit when using diode CR6. The output from the "and" gate is referred to as KD1. Marker 348 of the test listing is partially reproduced here for reference purposes.



ARR 80-1228

Figure 4-18. Mechanization of /KD1/.

(c) The first command in marker 348 is OSA (zero set all) and both D and K flip-flops will be zero set. After an OSA command the 1SF (one set following) command is generated by the FALT.

```
348   Logic for KD1 is on bords 236, 237.
      OSA   D    1TA   KD1     .   01    .    .    .    .    .
      1SA   K    1TA   KD1     .   01    .    .    .    .    .
      1SA   OTA  KD1     .   01 K-       .    .    .    .    .
      1SA   D    K     OTA     KD1       . 01 D    .    .    .
```

NOTE

Since the 1SF command is automatically generated by the FALT, the command does not appear on the test tape and is not shown on the test listing.

(d) Flip-flop D is then addressed and one set, completing the logic for KD1 driver. The 1TA (one test "and") command follows and then the logic driver is addressed and tested. If no error is detected by the FALT the B test tape continues with the next set of indexes. Both flip-flops are now one set by the command 1SA; flip-flop K is then addressed and zero set again, completing the necessary logic for KD1. Driver KD1 is again one tested to ensure it is on. The next test is a negation test of diode CR4 on circuit board 237. The flip-flops are both one set by the 1SA command. Since flip-flop K is now one set, the logic for KD1 is not true. However, if diode CR4 is open, it will not hold the gate false, therefore, the logic

4-32. DESCRIPTION OF B TEST TAPE--Continued

driver will be on and an error will be detected when the driver is zero tested by the OTA command. The last test in marker 348 is the negation test of diode CR5. Both flip-flops are again one set, addressed, and zero set. Since flip-flop D is now zero set, the logic gate should be false, however, if diode CR5 is open it will not hold the gate false, therefore, the logic driver KD1 has been tested to determine that it is turning on when the logic is true and remaining off when the logic is false.

(2) Marker 383. During marker 383 on the B test tape the last addressable logic driver is tested; the remaining driver circuits will be tested during other computer logic tests. For example, driver /NXD/ is tested during marker 384 when the primary "and" gate (BDX) is tested.

383 Logic for TSH is on boards 233, 236.

1SA		TO	TX		D	E	K	OB3	TP	OTA	TSH
.	01	DSP-	.		.	.	.	.	.	.	.
1SA		TO	TX		DSP	D	E	K	TP	TOA	TSH
.	01	OB3-	.		.	.	.	.	.	.	.
1SA		TO	TX		DSP	D	E	K	OB3	OB2	TP
OTA		TSH	.	01	OB2	.	.	.	.	.	.
1SA		TO	TX		DSP	D	E	K	OB3	OTA	TSH
.	01	TP-	.		.	.	.	.	.	.	.
1SA		TO	DSP		D	E	K	OB3	TP	OTA	TSH
.	01	TX-	.		.	.	.	.	.	.	.
1SA		TX	DSP		D	E	K	OB3	TP	OTA	TSH
.	01	TO-	.		.	.	.	.	.	.	.

d. Addressable Primary "And" Gates. Beginning with marker 384 in the B test tape the addressable primary "and" gates are tested. Addressable gates are those gates whose output is directly connected to the FALT through the external FALT cables.

(1) Marker 384, general. The first gate to be tested is (BDX); the logic for (BDX) is reproduced below.

(BDX) = X1 X2 /NXD/ 237 A24

(a) Gate (BDX) is made up of flip-flops X1 and X2 and logic driver circuit /NXD/. Logic driver circuit /NXD/ is not an addressable logic driver and therefore, has not been tested in the logic driver portion of the B test tape. During marker 384, however, "and" gate (BDX) and logic driver /NXD/ will be tested, since it is part of the logic for gate (BDX). In addition to the circuit boards containing gate (BDX), the circuit boards associated with driver /NXD/ are called out in the B test tape listing at the beginning of marker 384. The logic for /NXD/ is reproduced below.

/NXD/ = + DSP DSH- *WI XD- 404B1

(b) Term WI, in the logic for driver /NXD/, is the zero output side of TDWI flip-flop; this flip-flop is referred to in the tape listings as PS, therefore, whenever PS flip-flop is zero set, term WI is true. Primary "and" gate (BDX), including driver /NXD/, is mechanized below (fig. 4-19).

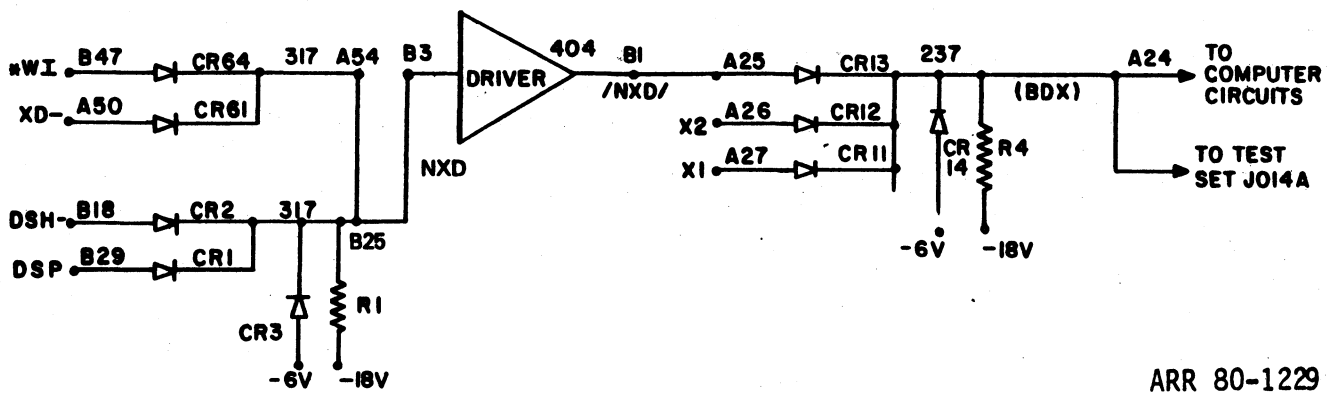


Figure 4-19. Mechanization of (BDX).

(c) The logic for driver /NXD/ is located on circuit board 317. Two separate "and" gates are used for /NXD/ logic driver input. These "and" gates are tied together to form one four-input "and" gate as shown on figure 4-19. As in all logic driver input gates, the circuit is clamped to -6 volts. The driver circuit itself is located on board 404. The input is on pin B3 and the output is pin B1 which is then tied to the input of gate (BDX) on pin A25 of board 237. The remaining inputs to the gate, X2 and X1, are on pins A26 and A27 respectively.

(d) Addressable primary "and" gates are tested by the FALT in basically the same manner as logic drivers were tested. Negation tests are also performed on the primary "and" gates. The (BDX) "and" gate test explanation may be followed by using the listing below.

(e) The test of (BDX) begins by addressing the necessary logic and then one testing the gate. The first command read on the tape is OSA which is followed by the address for DSP. This will then complete the logic for driver /NXD/. Flip-flops X2 and X1 are then addressed, completing the logic for (BDX), which is then one tested to ensure it is true.

```
384  Logic for BDX is on boards 237, 317, 404.
     OSA  DSP  X2   X1   ITA  BDX       .   01   .          .    .
     1SA  DSH  XD   PS   1TA  BDX       .   01   .          .    .
     1SA  DSH  XD   X1   PS   OTA       BDX      .    01    X1   .
     1SA  DSH  XD   X2   PS   OTA       BDX      .    01    X2   .
     1SA  DSH  DSP  XD   PS   OTA       BDX      .    01    NXD  DSP
     1SA  XD   PS   OTA  BDX  .   01    NXD      DSH-          .    .
     1SA  DSH  XD   OTA  BDX  .   01    NXD      *WI           .    .
     1SA  DSH  PS   OTA  BDX  .   01    NXD      XD-           .    .
```

4-32. DESCRIPTION OF B TEST TAPE--Continued

(2) Marker 384, index 011. The second test of (BDX) beginning with index 011 is also a one test of the gate. Here the first command is 1SA which is followed by the address for DSH, XD, and PS. Again, as in the first test, the logic is now set and (BDX) is one tested. The first negation test begins with index 021. In this test, driver /NXD/ and flip-flop X2 are both true.

(3) Marker 384, index 021. The X1 flip-flop has been zero set, therefore, gate (BDX) should be false and is zero tested to ensure this. The X1 flip-flop is tied to gate (BDX) through diode CR11 (fig. 4-19) on board 237. If the diode were open, it would not hold the gate false and an error is detected by the FALT, the next negation test begins with index 031. In this test, diode CR12 will be tested because the X2 flip-flop is now false and this diode should hold the gate false when it is zero tested.

(4) Marker 384, index 041. In the next test, beginning with index 041, a negation test of diode CR13 is made by turning off driver /NXD/ and zero testing gate (BDX). In order to turn off driver /NXD/, its input gate located on circuit board 317 must be false; therefore, one input to the driver input gate must be false. In the test beginning at index 041, flip-flop DSP is zero set, thereby making the driver input gate false, thus turning off the driver. With the driver false, gate (BDX) should be false and no errors should be detected by the FALT when (BDX) is zero tested. If the test passes with no error indication several things should be apparent. First, diode CR13 is conducting properly and holding gate (BDX) false; second, driver /NXD/ is turning off when its input gate is false; third, diode CR1 is conducting properly and holding the driver input gate false. The remaining diodes to the driver input gate must also be tested to ensure that they will hold the input gate false. Diode CR2 is tested in the next test when flip-flop DSH is one set; diode CR64 is tested next and finally diode CR61.

(5) Completion of marker 384. After completing marker 384 on the B test tape the primary "and" gates have both been tested even though logic driver /NXD/ is not an addressable logic driver. From marker 384 to 458 the addressable primary "and" gates are tested. However, not all primary "and" gates are addressable. The ones which are not will be tested in other computer logic tests. The addressable write switches associated with computer memory writing will be tested in the E test tape beginning at marker 252.

e. Flip-Flop Logic Tests.

(1) With the completion of the primary "and" gate tests, the B test tape begins the tests of flip-flop logic. There are four tests performed on the logic for each flip-flop. The tests performed include "or" tests for the one input, "and" tests for the one input, "or" tests for the zero input, "and" tests for the zero input. Flip-flop logic can be defined as all logic equations that are used to one or zero set a flip-flop. TM 9-1220-221-34/1/1 contains a complete list of the logic equations that exist in the computer.

(2) When a set all command (1SA or OSA) is read on tape the FALT reacts in two ways; first, all DU/DL drivers are turned on activating all DU/DL lines; second, a clock pulse is output to all flip-flop circuits. The FALT activates all DU/DL lines since all flip-flops are to be set. A 1 clock pulse results from a 1SA command and a 0 clock pulse results from a OSA command.

(3) To change the state of any flip-flop circuit, two things are required; a true logic input and a clock pulse. The DU/DL lines, when they are on, can substitute for a logic input. All that is required then, to change the state of a flip-flop with the DU/DL lines on, is the clock pulse. Therefore when the logic of a flip-flop is to be tested, it is used as the logic input.

(4) In the first test of flip-flop CL3 in marker 533 the output from the first equation is used to one set CL3. In addition to the input from the first equation, a 1 clock pulse is required to set CL3. The 1 clock pulse results when the 1SA command is generated in the FALT. However, with the clock pulse, DU/DL lines are also activated. Since the output of the first logic equation is being tested to ensure it will one set the flip-flop, the DU/DL lines cannot be used. However, these lines will be on when the 1SA command is generated. The reference or bias voltage used with the DU/DL diodes must be turned off to eliminate interference from the DU/DL lines. This reference or bias voltage in the computer is known as -18VFT. The -18VFT originates in the FALT and is on whenever the E18 flip-flop in the FALT is one set. By zero setting the E18 flip-flop, the -18VFT will be turned off. Since the -18VFT is the bias voltage for the DU/DL diodes they will not affect the flip-flop circuit when the bias voltage is off and the logic input can then be used to set the flip-flop. The OE18 command on tape will zero set the E18 flip-flop. This command will be followed by a set all command to generate the required clock pulse to set the flip-flop and effectively test the logic equation. After the set all command, the 1E18 command follows to one set the E18 flip-flop which turns on the -18VFT bias voltage required to test the flip-flop.

(5) Beginning at marker 533, the logic for flip-flop CL3 is tested. Due to the length of the test involved, it will not be reproduced here. However, the CL3 flip-flop logic test explanation may be followed by using the B test tape. Six equations make up the logic for the one-set side of CL3 flip-flop. The logic for 1CL3, as outlined in TM 9-1220-221-34/1/1, is reproduced below.

```
1CL3 = +CL4      (KB5)
       +(        +CL5- S LP-
        (        +CL5- S- LP
        (        +CL5 S LP
        (        +CL5 S- LP-
        )        /KTRS/
        +        /KA- /XC/TRC/(BL3)
```

4-32. DESCRIPTION OF B TEST TAPE--Continued

(6) The second thru fifth equations are first "ored" together, then "anded" with a common term driver, /KTRS/, using a tertiary gate. The output from tertiary gate is then "ored" with the first and sixth equations to form the logic for CL3.

(7) The logic for 1CL3 is mechanized in the schematic (fig. 4-20). The first equation for the one-set side of CL3 is tested during the first two tests in marker 533. The first equation is made up of terms CL4 and (KB5). The logic for "and" gate (KB5) is /KB/ and B5. Driver /KB/ is fed from the one output of flip-flop K which will complete the logic for the first equation. The next command OE18 turns off the -18VFT bias voltage. A 1SA command follows, generating the necessary 1 clock pulse. Flip-flop CL3 was zero set by the initial OSA command and since the logic for the first equation has been addressed, CL3 should one set with the 1 clock pulse from the 1SA command. With the next command the E18 flip-flop is one set to turn the -18VFT on for testing; this is followed by the 1TF (one test the following) command. Flip-flop CL3 is then addressed and tested. In this first test of the CL3 logic, only the first equation was tested since it was the only equation whose logic was true.

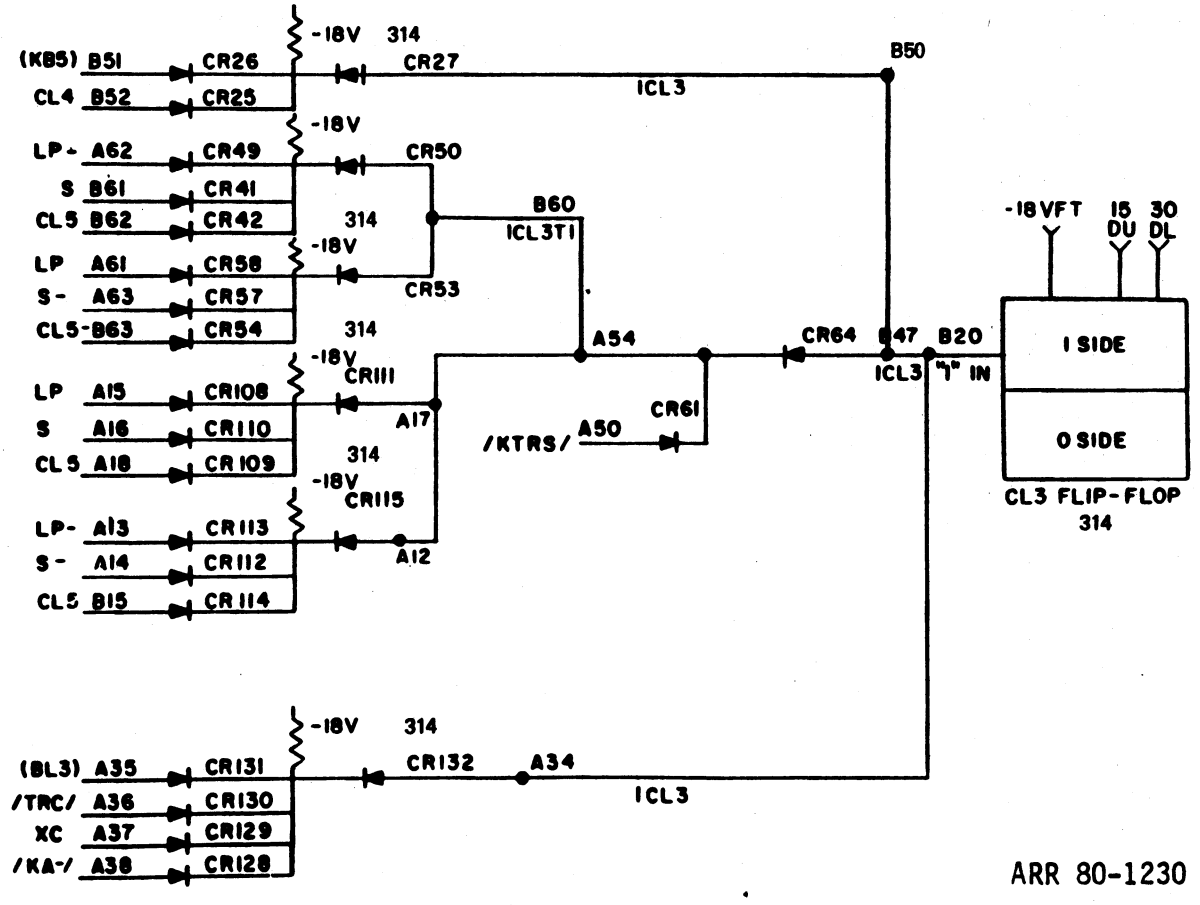


Figure 4-20. Mechanization for 1CL3.

(8) The second test marker 533 is also a test of the first equation. The first command in this test is 1SA which will complete the logic for the first equation. However, before clocking, CL3 must be zero set to test the logic. The -18VFT is then turned on, and the flip-flop is 1 clocked and then one tested.

(9) Index 021 begins the test of the second equation. Since the second equation is "anded" with tertiary term, driver /KTRS/ must also be true to set the flip-flop. The B test tape continues by testing each equation to ensure that when the logic for each equation is true the flip-flop will set.

(10) The "and" test of the logic for the one side of CL3 begins with marker 535. In an "and" or negation test the particular flip-flop is initially zero set and various logic inputs are set false so that no one-set logic equations are true. The flip-flop is then 1 clocked and zero tested to ensure it has not one set since no logic equation is true. In the first test of marker 535, the 1SA command is followed by the addresses for flip-flops no logic equation should be true. In the first equation CL4 has been zero set; in the sixth equation, driver /KA-/ is not on and equation two thru five are false. Flip-flop CL3 was also zero set and when 1 clocked should not one set.

(11) If CL3 one sets, two possible causes exist; either diode CR25 (associated with the CL4 flip-flop in the first equation) or diode CR128 (associated with driver /KA-/ in the sixth equation) is open, since both of these terms have been negated. In the test tape listing following the first test in marker 535 the terms associated with the diodes under test are called out. For example, 01 CL4 indicates that the diode associated with term CL4 of the first equation is under test. In the schematic (fig. 4-20), term CL4 is tied to the gate of the first equation on pin B52 through diode CR25. In the sixth equation the diode CR128 associated with term KA- is also under test (the schematic diagram, fig. 4-20). All of the diodes for each of the six equations will be tested in this manner. In addition, the diode of the tertiary gate will be tested. The B test tape continues by testing flip-flop logic. Flip-flop LX is the last flip-flop to be tested in the B test tape. At the end of marker 730 the composite listing for markers 340 thru 347 is printed.

4-33. DESCRIPTION OF TEST TAPE C

a. General. The C test tape begins by testing the logic for flip-flop CP3 and ends with logic tests of flip-flop 04. In all, the logic for 40 flip-flops will be tested during the C test tape. The tests performed on the logic for each flip-flop are the same tests as those performed in B test tape.

4-33. DESCRIPTION OF C TEST TAPE--Continued

b. Sample Tests.

(1) The BSC (both sides clock) command is used during the testing of flip-flop CP3. When the BSC command is read on the tape, the FALT generates both a 1 and 0 clock pulse which is applied to the flip-flop under test. In the case of flip-flop CP3, the BSC command is used in the "and" test for the one side and the zero side. The logic for the one and zero input of CP3 flip-flop is reproduced below:

1 CP3 = +CL4 (KFST)
+CP3- CP2/OCT/

0 CP3 = +CL4- (KFST)
+(CRS)
+CP3 CP2/OCT/

(2) In the second equation for the one input of CP3 the prime or zero set output is used; in the third equation for the zero input of CP3 the one set output is used. The logic for CP3 is mechanized in the schematic (fig. 4-21). The one-set output on pin B28 of the logic flip-flop board is tied to the zero input logic on pin A18 of board 318; the zero-set output on pin B27 is tied to the one-set input logic on pin B6.

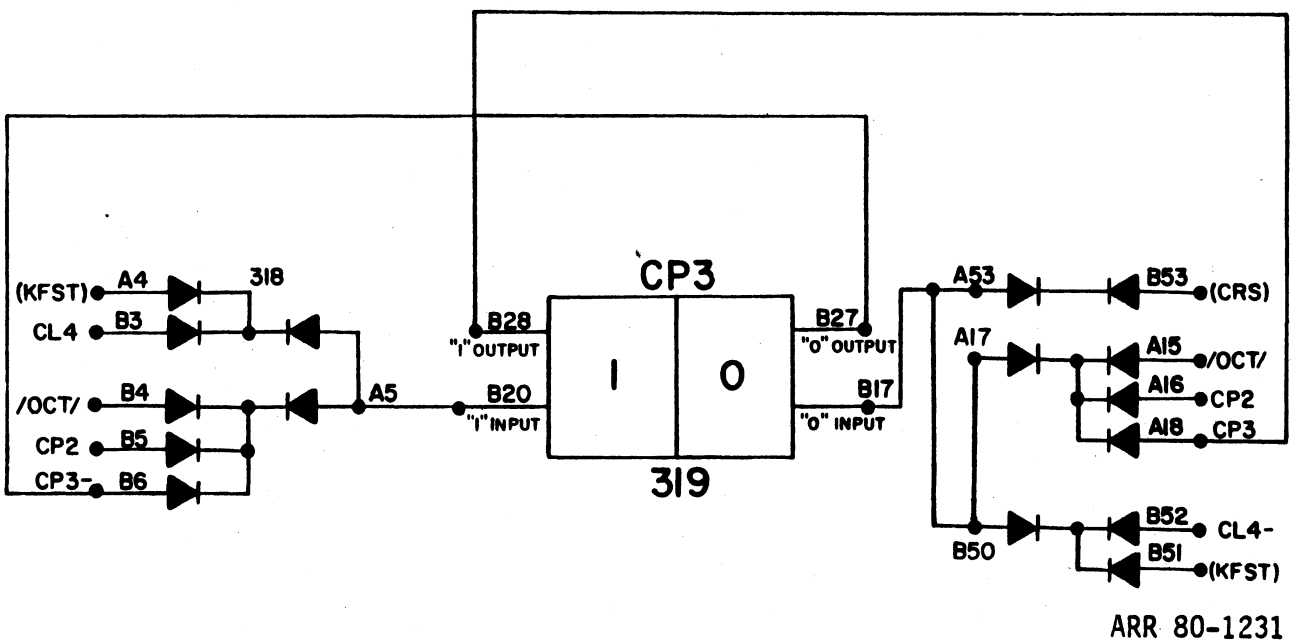


Figure 4-21. Mechanization of CP3 Logic.

(3) The "or" test for the one side of CP3 is similar to the "or" tests for the other flip-flop logic. Each equation is tested to ensure it will one set the flip-flop. The "and" test for the one side is also conducted in a similar manner except for the negation test of the diode associated with term CP3- in the second equation (CR106). To perform a negation test of diode CR106 it will be necessary to

one set flip-flop CP3 making term CP3- false. However, with CP3 flip-flop one set, it is now impossible to 1 clock the flip-flop and test it since it is already one set. To make the negation test of this diode the BSC command must be used. In the logic equation for CP3, terms CP2 and /OCT/ are common to the second equation for the one input side and the third equation for the zero input side. The difference in the two equations is CP3- and CP3. For a negation test of CP3- the other terms in the equation are true and CP3 is one set, making the third equation for the zero input true. With the BSC command, a clock pulse is applied to both sides of the flip-flop and because the third equation is true the flip-flop should zero set. However, if the diode associated with term CP3- in the second equation is open, it will not hold the gate false and, therefore, when the flip-flop is clocked it will remain one set.

(4) The test explanation for CP3 may be followed by using the test tape C program printout (TM 9-1220-221-34/3). The CP3 "and" test for the one side begins at marker 002. The negation test of diode CP3- begins with index 041. The 1SA command is followed by zero setting flip-flops B2, D, E, FS, K, and OB3. Once these flip-flops are zero set, the first equation for the one input side is false. Flip-flop K was zero set making gate KFST false. The second equation is also false since CP3 is one set. After the flip-flop addresses, the OE18 command follows turning off the -18VFT bias voltage. The next command on tape is BSC and both a 1 and 0 clock pulse are now applied to all flip-flop circuits. However no flip-flop in the computer will be affected by these clock pulses.

NOTE

Whenever a set all command (1SA or OSA) is read on tape, the FALT, in addition to generating a clock pulse, turns on all DU/DL drivers since both are required to set a flip-flop. But with a BSC command, the DU/DL drivers are not on. With the DU/DL drivers off, ground appears on the DU/DL lines to all flip-flop circuits and any logic input signal will then be grounded. When the logic input signal is grounded, the flip-flop will not change states when clocked. It is necessary, therefore, to address the flip-flop which is being tested. After the BSC command, the FALT will remain in the both sides clock mode and the flip-flop under test can then be addressed.

(5) After the BSC command, CP3 is addressed and a 1 and 0 clock pulse are applied to CP3. Flip-flop CP3 should now zero set since the third equation for the zero input logic is true. However, if a true signal is also present on the one input side, CP3 will remain one set. This condition will exist if the diode associated with term CP3- or term (KTRS) is open. After CP3 is addressed, the E18 flip-flop is one set and CP3 is then zero tested. If CP3 had zero set, no error will be detected and a negation test has been successfully performed on diode CR106 using the BSC command.

(6) There are many flip-flops in the computer whose logic is tested using the both sides clock command. In the negation test of the zero input logic of CP3 during marker 004 the BSC command will again be used. The C test tape continues with flip-flop logic tests ending at marker 344.

4-34. DESCRIPTION OF D TEST TAPE

a. General. The D test tape begins with the logic tests of flip-flop OB6 and ends with the logic tests of flip-flop X1. The computer shorting cable is used when running the D test tape. Tables 4-7 thru 4-9 indicate the computer shorting cable term and pin lists for connector J016, and J010. The mechanical reader, one of the input devices, is also tested with this tape.

Table 4-7. Computer Shorting Cable Term and Pin Listing Connector J016

From pin	Wire term	Connector	To pin	Term	Remarks
F	R7	J017	/J	F281	100-ohm resistor jumper/subassembly to J010-P
G	R7-	J017	/K	F291	100-ohm resistor jumper/subassembly to J010-R
H	R6	J017	/M	F301	100-ohm resistor jumper/subassembly to J010-S
J	R6-	J010	X	OPL10	Subassembly to J010/K
K	R5	J101	/T	F20	Subassembly to J010/E
L	R5-	J010	/U	F21	Subassembly to J017-HH/J010/A
M	R4	J016	Y	GPSS-	Jumper/subassembly to J010/V
N	R4-	J016	X	GPHH-	Jumper/subassembly to J010/W
P	R3	J010	/X	F24	Subassembly to J017-JJ
R	R3-	J017	/N	F25	Subassembly to J017-KK
S	R2	J017	/P	F26	Subassembly to J017-LL
T	R2-	J017	/Q	F27	Subassembly to J017-MM
U	RFS	J017	/R	F28	Subassembly to J017/R
V	RFS-	J017	/S	F29	Subassembly to J017/S
X	GPHH-	J016	N	R4-	Jumper/subassembly to J010/W
Y	GPSS-	J016	M	R4	Jumper/subassembly to J010/V

Table 4-8. Computer Shorting Cable Term and Pin Listing Connector J017

From pin	Wire term	Connector	To pin	Term	Remarks
D	I1G	J010	FF	ESU20	
E	I2G	J017	Z	PE00	Jumper
F	I3G	J017	Y	RDY0	Jumper
G	I4G	J010	K	D202	
H	I5G	J017	W	RG0	Jumper
J	I6G	J017	V	FB10	Jumper
K	I7G	J010	U	IMT0	
L	I8G	J010	T	AMT0	
M	TG	J010	V	FB00	
N	TG-	J017	X	RH0	Jumper
P	TG0-	J017	T	MTF	Jumper
R	TEIP	J017	S	TR-	Jumper
S	TR-	J017	R	TEIP	Jumper
T	MTF	J017	P	TG0-	Jumper
U	IFS	J010	/S	F19	
V	FB10	J017	J	I6G	Jumper
W	RG0	J017	H	I5G	Jumper
X	RH0	J017	N	TG-	Jumper
Y	RDY0	J017	F	I3G	Jumper
Z	PE00	J017	E	I2G	Jumper
/A	OPL40	J010	/P	F221	
/B	OPL50	J010	/Q	F231	
/C	OPL60	J010	/R	F241	
/G	F251	J010	L	D300	

4-34. DESCRIPTION OF D TEST TAPE--Continued

Table 4-8. Computer Shorting Cable Term and Pin Listing Connector J017--Continued

From pin	Wire term	Connector	To pin	Term	Remarks
/H	F26I	J010	M	D400	
/I	F27I	J010	N	D500	
/J	F28I	J016	F	R7	100-ohm resistor in series with pins (subassembly to J101-P)
/K	F29I	J016	G	R7-	100-ohm resistor in series with pins (subassembly to J010-R)
/M	F301	J016	H	R6	100-ohm resistor in series with pins (subassembly to J010-S)
/N	F25	J016	R	R3-	Subassembly to J017-KK
/P	F26	P017	LL	F17	Jumper/subassembly to J016-S
/Q	F27	J017	MM	F27	Jumper/subassembly to J016-T
/R	F28	J016	U	RFS	
/S	F29	J016	V	RFS-	
HH	F14	J010	/A	FTF-	Subassembly to J010-U
JJ	F15	J010	/X	F24	Subassembly to J016-P
KK	F16	J017	/N	F25	Jumper/subassembly to J016-R
LL	F17	J017	/P	F26	Jumper/subassembly to J016-S
MM	F18	J017	/Q	F27	Jumper/subassembly to J016-T
NN	CTT1	J010	EE	EER20	
PP	MRTT	J010	/G	TFA0-	

Table 4-9. Computer Cable Term and Pin Listing Connector J010

From pin	Wire term	Connector	To pin	Term	Remarks
J	D100	J010	/H	TFB0	Jumper
K	D200	J017	G	I4G	
L	D300	J017	/G	F25I	
M	D400	J017	/H	F26I	
N	D500	J017	/I	F27I	
P	D600	J016	F	R7	Subassembly to J017-/J
R	D700	J016	G	R7-	Subassembly to J017-/K
S	D800	J016	H	R6	Subassembly to J017-/M
T	AMT0	J017	L	I8G	
U	1MT0	J017	K	I7G	
V	FB00	J017	M	TG	
W	STB	J010	/I	TFB0-	Jumper
X	OPL1	J010	/K	F19I	100-ohm resistor in series with pins/subassembly to J016-J
Y	OPL2	J010	/M	F20I	Jumper
Z	OPL3	J010	/N	F21I	Jumper
/A	FTF-	J017	HH	F14	Subassembly to J010-/U
/E	OFS	J010	/T	F20	Jumper/subassembly to J016-K
/F	TFA1-	J010	/J	TEOP	Jumper
/G	TFA0-	J017	PP	MRTT	
/H	TFB0	J010	J	D100	Jumper
/I	TFB0-	J010	W	STB0	Jumper
/J	TEOP	J010	/F	TFA1-	Jumper

4-34. DESCRIPTION OF D TEST TAPE--Continued

Table 4-9. Computer Cable Term and Pin Listing Connector J010--Continued

From pin	Wire term	Connector	To pin	Term	Remarks
/K	F19I	J010	X	OPL10	100-ohm resistor in series with pins/subassembly to J016-J
/M	F20I	J010	Y	OPL20	Jumper
/N	F21I	J010	Z	OPL30	Jumper
/P	F22I	J017	/A	OPL40	
/Q	F23I	J017	/B	OPL50	
/R	F24I	J017	/C	OPL60	
/S	F19	J017	U	IFS	
/T	F20	J010	/E	OFS	Jumper/subassembly to J016-K
/U	F21	J017	HH	F14	Subassembly to J010-/A
/V	F22	J016	M	R4	Subassembly to J016-Y
/W	F23	J016	N	R4-	Subassembly to J016-X
/X	F24	J017	JJ	F15	Subassembly to J016-P
EE	EER20	J017	NN	CTT1	
FF	ESU20	J017	D	I1G	

b. Specific Tests Pertinent to D Test Tape.

(1) The input register in the computer is made up of flip-flop D1 thru D8. These same flip-flops are also used in the output and display functions. In the D test tape, the mechanical reader is tested using these input register flip-flops. During the E test tape these same flip-flops are used when the keyboard, another input device, is tested.

(2) D8 is the first input register flip-flop to be tested. The test begins at marker 133 in the test tape D program printout. The logic equations for D8 are contained in TM 9-1220-221-34/1/1. Input term *I8 appears in the first equation. I8 enters the computer from an external input device through connector J017. However, when testing

the computer, no input device is connected. The computer shorting cable which is tied to connector J017 during testing is used to simulate various input terms; in this case *I8. This input term enters the computer on pin L of J017 and is then routed to driver circuit on board 402. The output of the driver is then "anded" with gate (OSA) to form the first logic equation for flip-flop D8. The method used to simulate input terms *I8 is on figure 4-22. When the shorting cable is connected, pin L of J017 is tied to pin T of J010 (J10 is the computer output connector). Output term AMTO, the signal on pin T of J010 is used to identify the address period to some external output device. However, with the computer shorting cable connected, its function is to simulate the *I8 line. In the test of the first equation for D8, at marker location 133, the logic to turn on AMTO will be addressed. Once AMTO is true, the equation can be used to one set D8. In addition to testing the logic for D8, the *I8 input driver and the AMTO output driver have both been tested in marker 133.

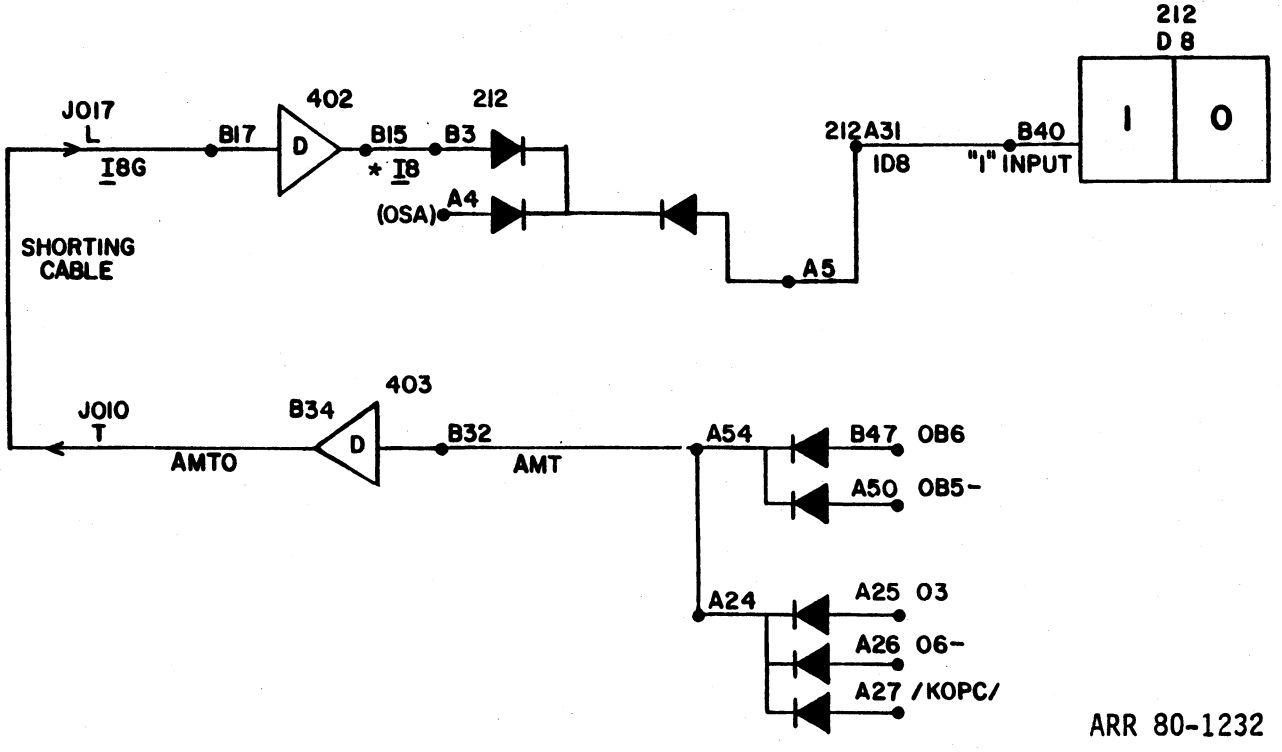


Figure 4-22. Stimulation of Input Terms *I8.

(3) Other computer output terms are also used to simulate inputs and are tested in this manner. When input term *I7 is tested during the D7 flip-flop tests, output term IMTO is used to simulate *I7.

(4) The eighth equation for the one input of D8 also contains an input term. This input term, *I8C, originates in the computer control panel and is an output of the mechanical reader or keyboard. There are a total of eight input lines from the computer control panel and each one is used with a different input register flip-flop. By using the D flip-flop the input device on the control panel can be tested. In the D test tape the mechanical reader input device will be tested.

4-34. DESCRIPTION OF D TEST TAPE--Continued

(5) The logic necessary to activate the mechanical reader solenoid is illustrated in the schematic in figure 4-23. The output from the tape sensing lever, called MRL, is used as an input in the mechanical reader logic. When the mechanical reader is to be used in the D test tape, a piece of tape must be placed under the tape sensing lever to complete the logic.

(6) The test of I-line 8 from the mechanical reader occurs in marker 134 beginning at index 081. Once the mechanical reader logic has been addressed, a time delay follows; this allows the solenoid to close and push the tape sensing pins up. Since no tape has been placed under the pins, they all indicate an output signal of -10 volts. I-line 8 is then "anded" in a gate circuit with 0B2- and then used to one set D8 flip-flop. Each of the I-line outputs from the mechanical reader are tested separately, when D7 is tested I-line 7 is tested. Term *TC (timing control) is also an output from the mechanical reader. This term which is used in the logic for 0B4 flip-flop was tested earlier in the D test tape when 0B4 was tested.

(7) The remaining input devices located on the control panel are tested when the E test tape is used; the D test tape continues with flip-flop logic tests similar to those described in paragraph 4-32d.

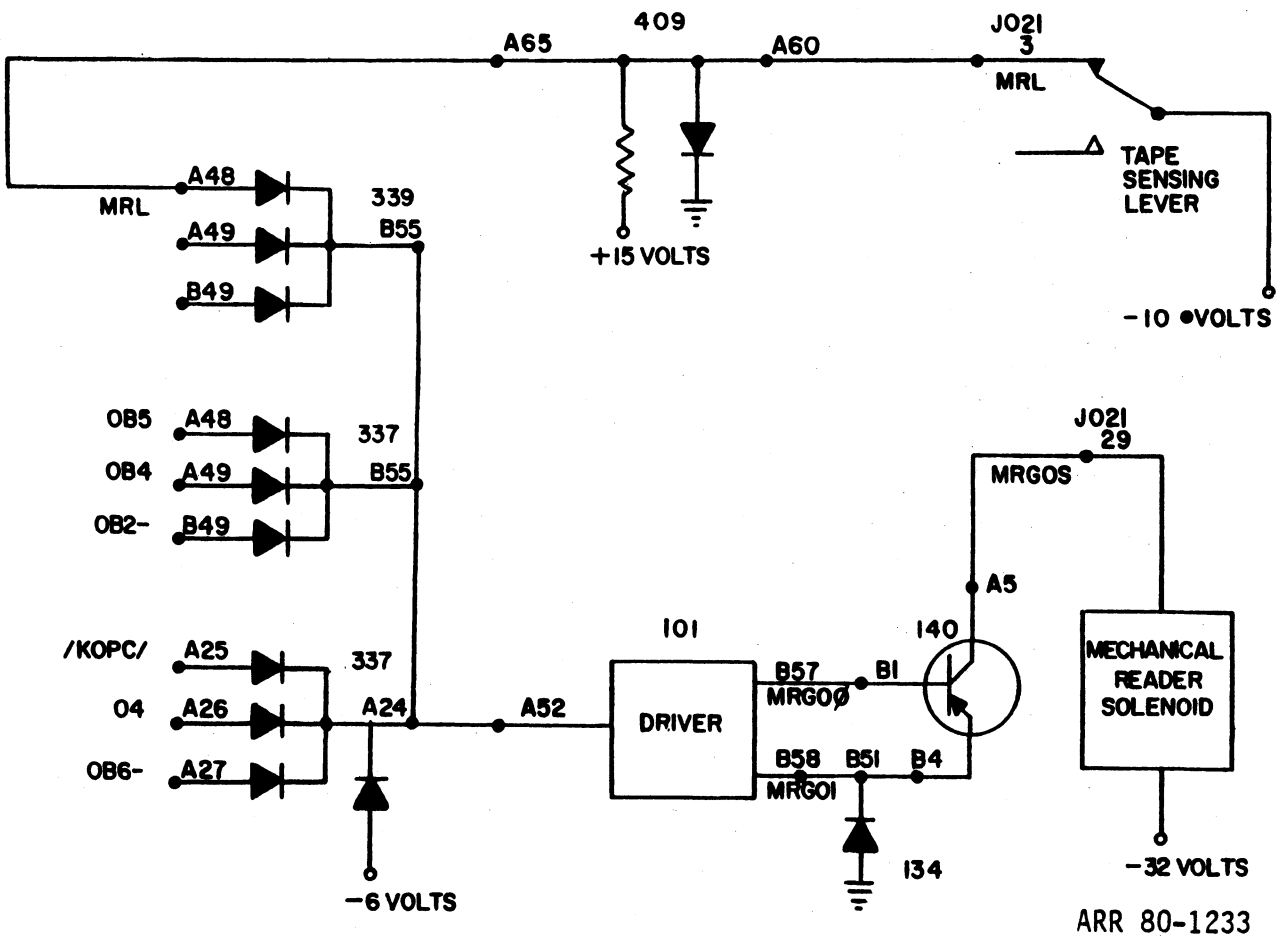


Figure 4-23. Logic Circuitry for Mechanical Reader.

4-35. DESCRIPTION OF E TEST TAPE

a. General.

(1) During the E test tape the remaining flip-flop logic will be tested; in addition, the E test tape also tests the nixie indicators, control panel setup buttons, neon lamps, matrix keyboard, the read and write circuitry, and the memory. The E test tape completes the testing of the computer using FALT.

(2) The E test tape begins with the logic tests of AP flip-flop. This is the A loop extension flip-flop and since the A loop is used in most computer functions there are many logic equations associated with AP. Following the logic tests of AP the mode control flip-flop D is tested. The logic tests of C7 and C3 follow the D flip-flop tests and complete the logic flip-flop tests.

b. C3 Logic Tests.

(1) Many of the logic equations used to one set flip-flop C3 contain input terms commonly referred to as F-lines. These F-lines originate from the FADAC control panel (front panel) or some external device. The matrix portion of the control panel is the source of F-lines 1 thru 13. The remaining F-lines enter the computer through connectors J010 and J017. Those F-lines which are not part of the logic for flip-flop C3 are contained in the logic for the C7 flip-flop.

(2) The output lines from the matrix switches S1 thru S8 and SA thru SH are "ored" together on the network A circuit boards to form F-lines 1 thru 7. These "or" diodes are illustrated in figure 4-24. F-lines 8 thru 13 are from the battery and weapon type buttons on the matrix and are illustrated in figure 4-25. These 13 F-lines together with the F-lines from other external devices are then used in the logic for flip-flops C3 and C7. The F-lines originating in the matrix may be tested by simply depressing the correct combination of matrix switches for any desired F-line. For example, F2 is true whenever the numbered switches S2, S4, S6, or S8 are depressed and F7 is true if any one of the lettered switches SE, SF, SG, or SH is depressed. F9 is true when battery button A is depressed. The remaining F-lines, those which originate from external devices, must be simulated to test the logic equation with which they are associated. The computer shorting cable connected between J010, J016, and J017 is used for this purpose. In the ninth equation for the one input of flip-flop C3, term F15 is simulated using computer circuitry and the shorting cable.

4-35. DESCRIPTION OF E TEST TAPE--Continued

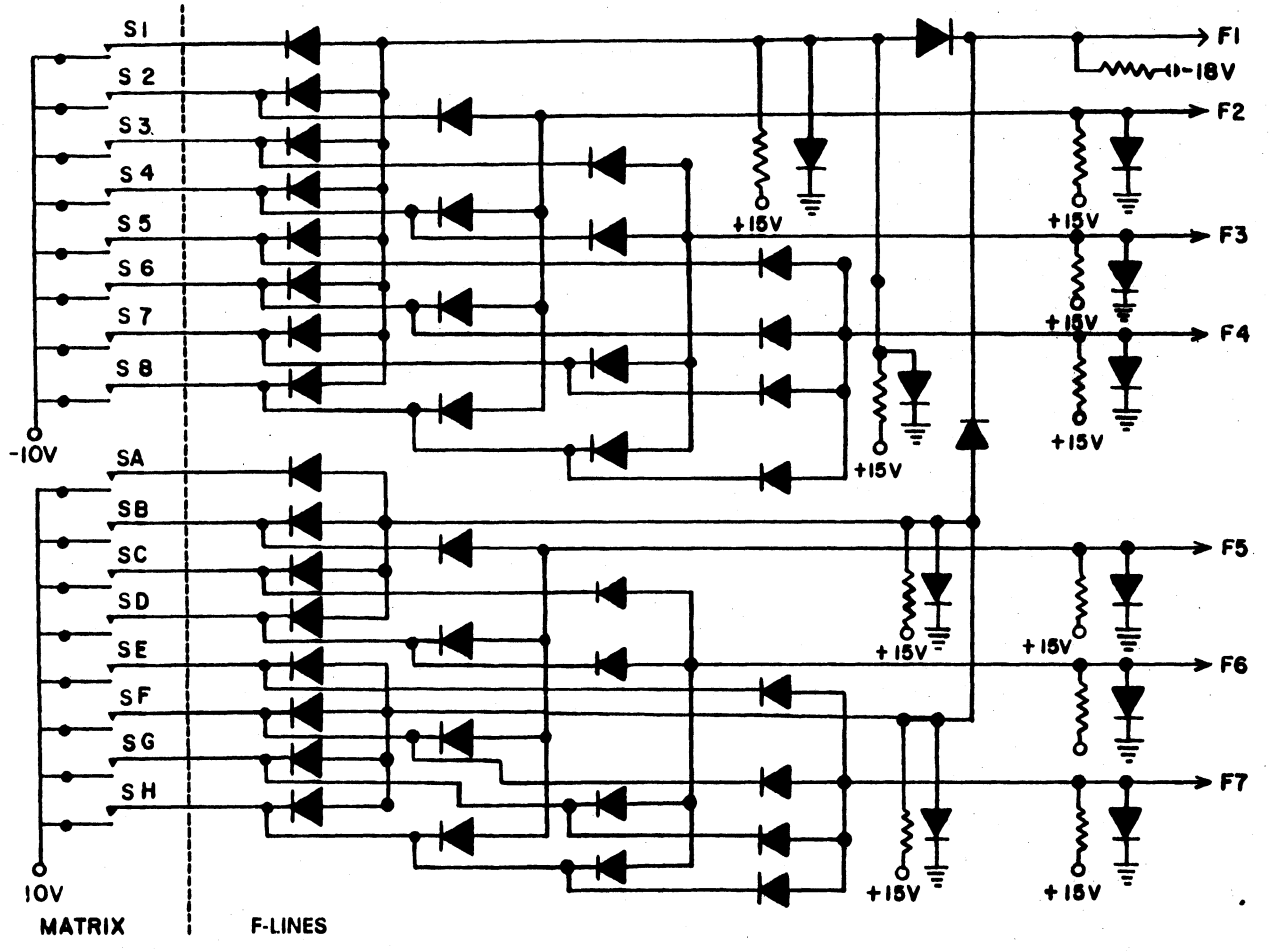


Figure 4-24. Mechanization of F-lines.

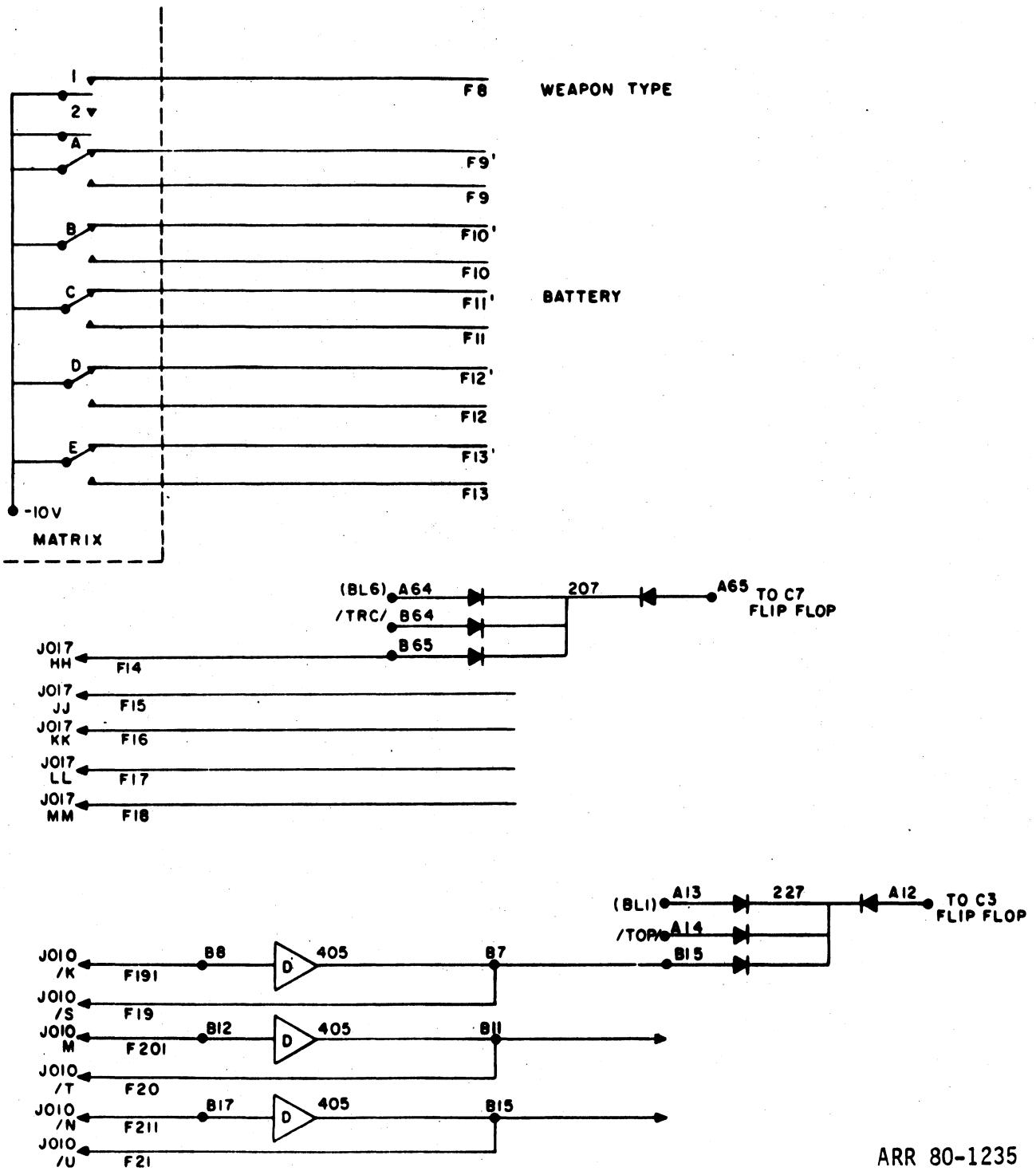


Figure 4-25. Mechanization of C7 Logic Input Utilizing F14.

4-35. DESCRIPTION OF E TEST TAPE--Continued

(3) The test of C3 logic begins in the E test tape at marker 104. The test of the second equation for the one input logic of C3 will be explained in detail; the explanation may be followed by referring to the test tape E program printout. The first test of the second equation begins at index 021 in marker 104. The second equation is shown below:

```
+ ( + *F1 /TOA/
  ) /OX/
```

According to the instructions preceding marker 104 in the E test tape, matrix buttons F and 8 must be depressed before starting the SDR. With the depression of any two matrix buttons, the F1 line will be true. The output from the matrix is "anded" with /TOA/; this output is then "anded" in a testing gate with /OX/. The first command in the test of the second equation is OSA. The logic for /TOA/ and /OX/ is then addressed completing the second equation. To negate the remaining logic equations for C3, flip-flops PS (TD/WI) and E1 are both one set. Exciter flip-flop E2 is also involved in the C3 logic tests and must be zero set. Table 4-25 contains the logic for all F-lines except F32 which will be discussed later. Following the address for PS, the -18VFT is turned off, a 1 clock pulse is generated, and C3 is then one tested. If C3 is one set, the second equation has been successfully tested, in addition, F1 from the matrix has also been tested. In the following test on the E test tape, the second equation is tested again. This test begins at index 041, the first command is 1SA, the logic is again addressed and the flip-flop is one tested. In this test flip-flops E2 and E4 were both zero set. E2 was zero set to negate logic and E4 was zero set to test for matrix button depression. The FALT exciter flip-flops and their uses are explained in detail in paragraph 4-38.

(4) The E test tape continues by testing the remaining C3 logic equations. To test other equations, other matrix buttons must be depressed. When the seventh equation is tested, battery button C must be depressed for F-line 11. Due to the extensive time which would be required to test all 64 possible matrix combinations all selections are not tested. However, all F-line outputs are tested in either the C3 or C7 logic tests. It should be noted, therefore, that the matrix is not entirely tested in the E test tape.

c. C7 Logic Tests.

(1) The logic tests of flip-flop C7 begin with marker 107 in the E test tape. The F-lines which are not part of the C3 logic are used with flip-flop C7. F-lines 2 thru 12 originate in the matrix and are tested in the same manner as described in C3 logic tests. The remaining F-1 lines except F32 originate from external devices and must be simulated using other computer circuitry. The test of the eighth equation which contains an external F-line will be discussed in detail. The eighth equation for the one input of C7 is shown below:

```
( + *V14/TRC/ (BL6)
) /OX/
```

Term F14 enters the computer on connector J017 pin HH. The output of the gate containing the above terms is "anded" with the term /OX/ (tertiary gate) for the eighth equation, as illustrated in figure 4-26. When the computer shorting cable is connected, the output from F21 is used as an input to F14. The input to F21 on J010 pin /N is the output driver of OPL30 which is tied to J010 pin Z. The logic for primary gate (OPL3) input to the driver, is composed of flip-flops OP1, OP2, and OP3-. The input circuit for F14, when the shorting cable is connected, is illustrated in figure 4-26. When F14 is to be tested, the logic to turn on driver OPL30 must be addressed. The output of driver OPL30 then turns on driver F21 which simulates input line F14. The test of the eighth equation for the one-input logic of C7 begins at index 041 in marker 112. After the OSA command the logic is addressed. In addition, flip-flops OP1 and OP2 are one set turning on OPL3. Line F14 should then be "on" completing the logic to one set C7. The remaining F-lines in C7 logic are simulated for testing in a manner similar to F14. The computer shorting cable term pin and listing (table 4-8) can be used to determine the input circuit for each F-line. The E test tape also contains negation tests on term F14 including the input circuitry. The diode associated with flip-flop OP1 in the input circuit of OPL3 driver is tested during marker 123 beginning at index 061. In the course of testing the eighth equation, drivers OPL30 and F21 have also been tested. Driver OPL30 is a discrete output driver that is not addressable and is not normally an input to any flip-flop logic circuit. Yet the FALT has effectively tested this driver along with its input circuitry.

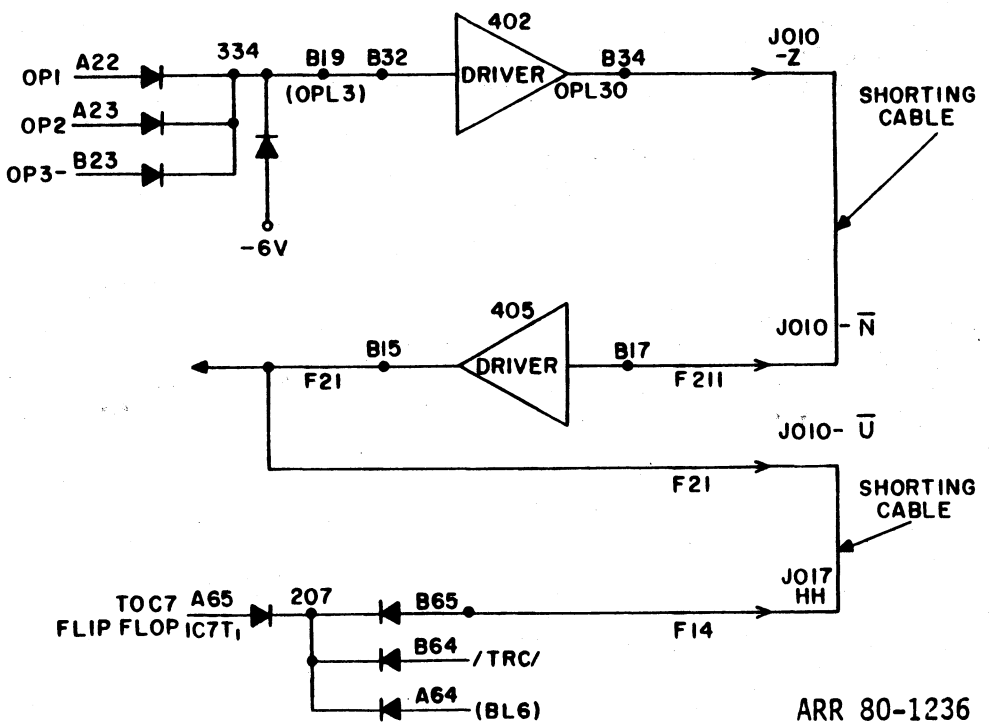


Figure 4-26. Input Circuit for F14.

4-35. DESCRIPTION OF E TEST TAPE--Continued

NOTE

The teletype comes from the factory set at 100 wpm. The TTY must be converted to 60 wpm for operation with FADAC. The TTY to FADAC cable connector is also wired wrong for FADAC operation. Rewire the connector as shown in figure 4-27.

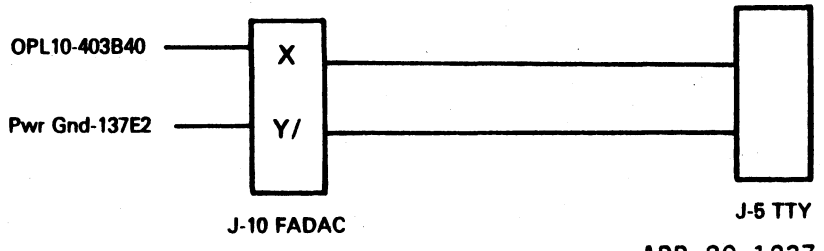


Figure 4-27. 537/G Teletype Connection to FADAC.

(2) The last equation for the one input of C7 contains an F-line which originates in the computer. The output of the teletype oscillator circuit on the network C board is called F32. The normal output of the teletype circuit is illustrated in figure 4-27. However, the teletype circuit will be under the control of the FALT when the last equation of C7 is being tested. Exciter flip-flops E6 and E7 are used to control the output of the oscillator for testing purposes. The output of E6 and E7 are used to control the output of the oscillator for testing purposes. The output of E6 and E7 enter the computer as ET6 and ET7 respectively on connector J015 pins /G and S. The last equation is tested beginning with index 081 during marker 114. Once the logic has been addressed, exciter flip-flop E7 is one set, the output from the teletype oscillator gives out a constant -6 volts as illustrated in figure 4-28. A time delay follows the one setting of E7, allowing the oscillator circuit to react to the exciter logic that was applied. After the time delay, the -18VFT is turned off and C7 is 1 clocked and one tested. In holding the oscillator circuit at a constant -6 volts, exciter flip-flop E6 was zero set and E7 was one set. When E6 is zero set and E7 is one set, term ET6 is false and ET7 is true. These signals are then applied to the oscillator circuit on pins B12 and A15 of the network C board to control the output. During the negation test of the F32 diode, the oscillator circuit is turned off by reversing the states of the two exciter flip-flops. The negation test of the F32 diode occurs during marker 130 in the E test tape. It should be noted that the FALT only controls the output of the teletypewriter, it has not been dynamically tested.

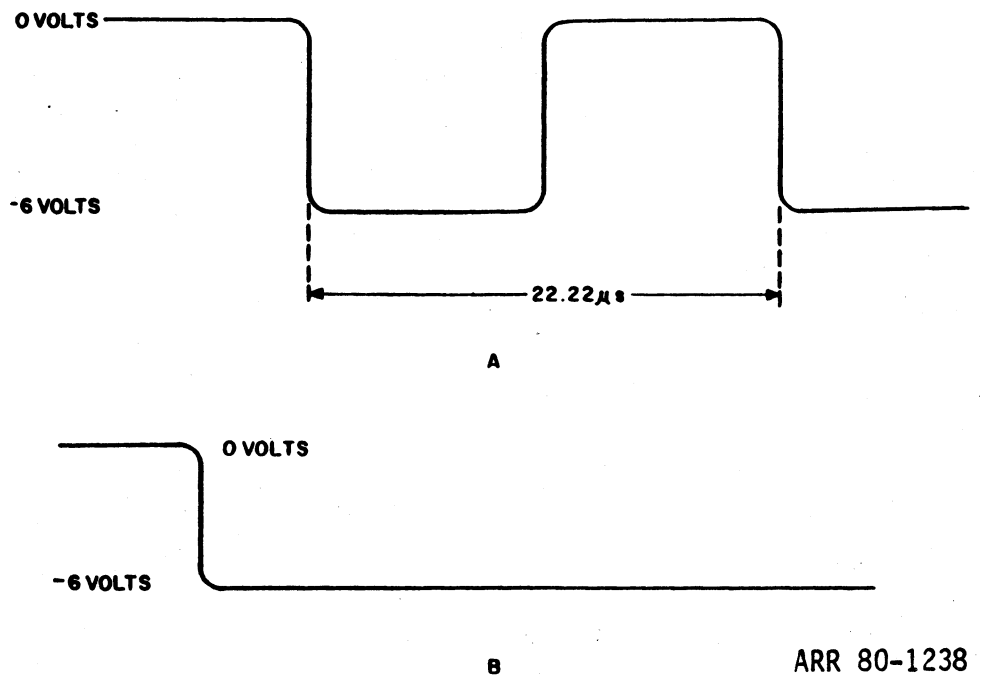


Figure 4-28. Teletype Oscillator Output (A) Normal, (B) Under Test Set Control.

d. Nixie Indicator Tests.

(1) Following the logic tests of flip-flops C3 and C7, the E test tape continues with the nixie indicator tests. In the nixie display the D and DA flip-flops are used to hold the numbers to be displayed. During the normal computer operation the display flip-flops are filled from the two-word D loop on the computer memory. However, while testing the nixie indicators, the FALT will control the D and DA flip-flops. In addition to the display register flip-flops, the FALT using the E test tape commands, must also control the anode driver logic flip-flops. The first test of the nixie indicators which begins at marker 148 is reproduced below:

```
148  DSH and test, zero side.
     1SA      B4       B3       B2    TS0   0E18   0SA    1E18   1TF   DSH
          01  X1-       .   02  T32   TS0     .      .      .      .     .
     1SA      B6       B3       B2    TS0   X1     0E18   0SA    1E18  1TF
     DSH       .   01  TOP       .     .     .      .      .      .     .
     1SA      B4       B1       TS0   X1    0E18   0SA    1E18   1TF   DSH
      .  01   BL1       .   02  T32   TS0     .      .      .      .     .
     1SA      B6       B1       TS0   0E18  0SA    1E18   1TF    DSH   .   02
     T32       .        .        .     .     .      .      .      .     .
```

4-35. DESCRIPTION OF E TEST TAPE--Continued

In the nixie indicator display it requires four flip-flops to hold the BCD (binary coded decimal) code for one decimal character and four decimal characters can be displayed at one time using the 16 display flip-flops. After addressing the display flip-flops in the first test the decimal characters that are held by the D and DA flip-flops are as follows:

BCD DECIMAL	D8- D7- D6 D5 / 3	BCD DECIMAL	D4- D3- D2 D1- / 2
BCD DECIMAL	DA8- DA7- DA6- DA5 / 1	BCD DECIMAL	DA4- DA3- DA2- DA1- / 0

To turn on any given nixie indicator both a cathode and anode driver are required. The display flip-flops will select the cathode driver depending on the BCD code and the quadrant counter composed of flip-flops X1 and X2 will control the anode driver. After addressing the flip-flops in the first test, anode driver one is true. The logic for AD1 is reproduced below:

$$AD1 = X1- \ X2- \ /NXD/$$

(2) The AD1 driver controls the voltage to the last three nixie indicators on the right side of the control panel and the first nixie indicator to the right of the sign nixie. The logic and circuitry to turn on these four indicators is illustrated in figure 4-29. Both the logic and the cathode driver circuit are on the same circuit board. Each network B circuit board contains one anode driver and 13 cathode driver circuits. Cathode drivers are also used in the battery and sign nixie indicators and the decimal neons. The F-lines from the battery buttons on the control panel matrix control the battery nixie indicators.

(3) In the second nixie indicator test, the display flip-flops hold the same counter; however, anode driver two on the second bank of nixie indicators will now light. The logic for AD1 and AD2 is similar except the X1 flip-flop is one set in AD2.

(4) All of the elements of each nixie indicator can be tested by controlling the display flip-flops and the anode driver logic.

e. Test of Control Panel Set Up Buttons.

(1) The eight set up buttons located on the computer control panel are tested during the E test tape. The outputs from the set up buttons enter the computer as SU-lines 0 thru 7. These eight SU-lines are then "ored" together on the network A circuit boards to form five output lines which are used in the computer logic. In figure 4-30 the set up buttons and the "or" gates are illustrated. The five output lines are: SU, SU-, SU1L, SU2L, and SU3L. Line SU- is true (-10 volts) as long as no set up button is depressed. Line SU is true whenever any one set up button is depressed. The remaining SU-

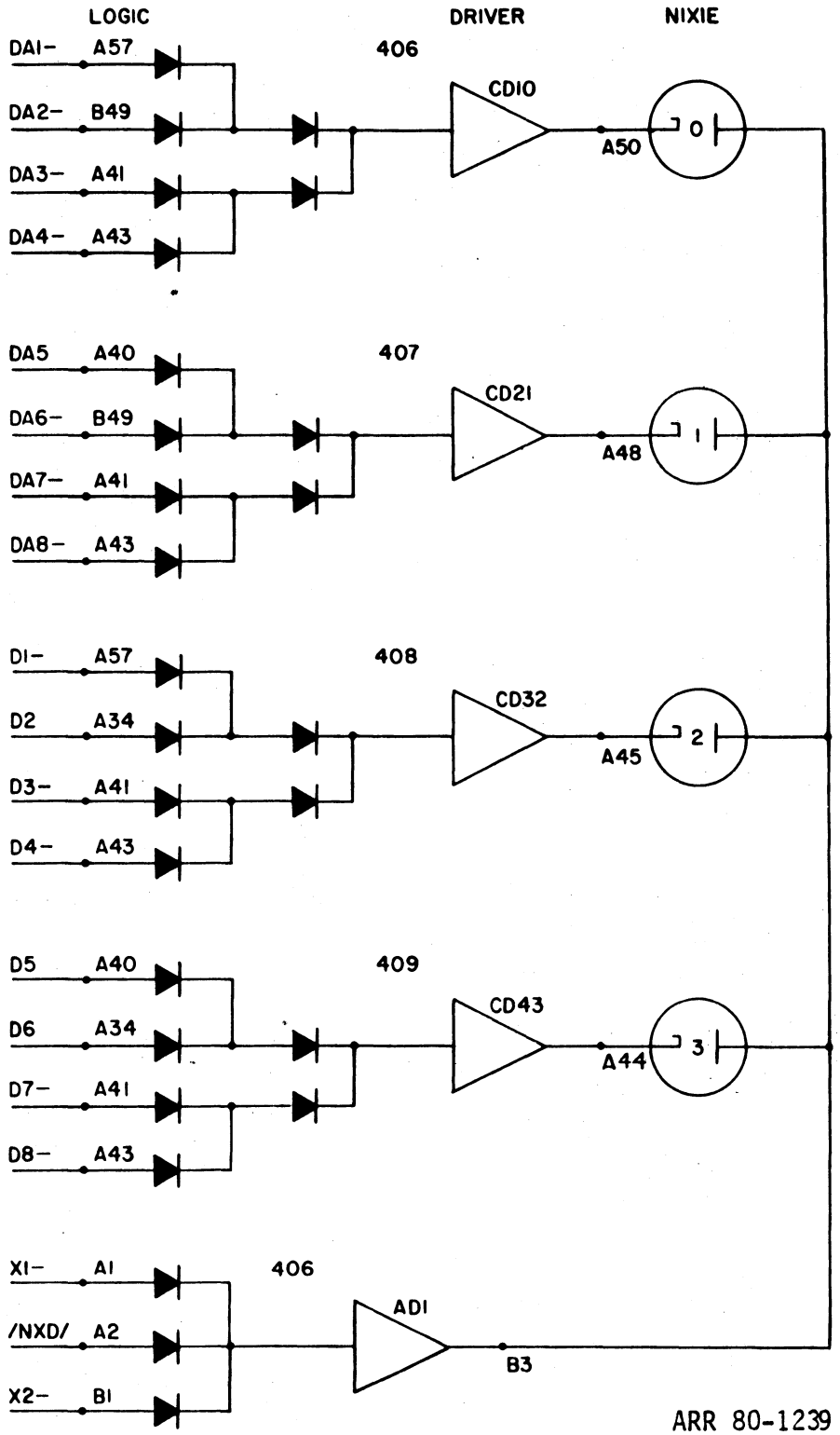


Figure 4-29. Nixie Indicator Logic Mechanization.

4-35. DESCRIPTION OF E TEST TAPE--Continued

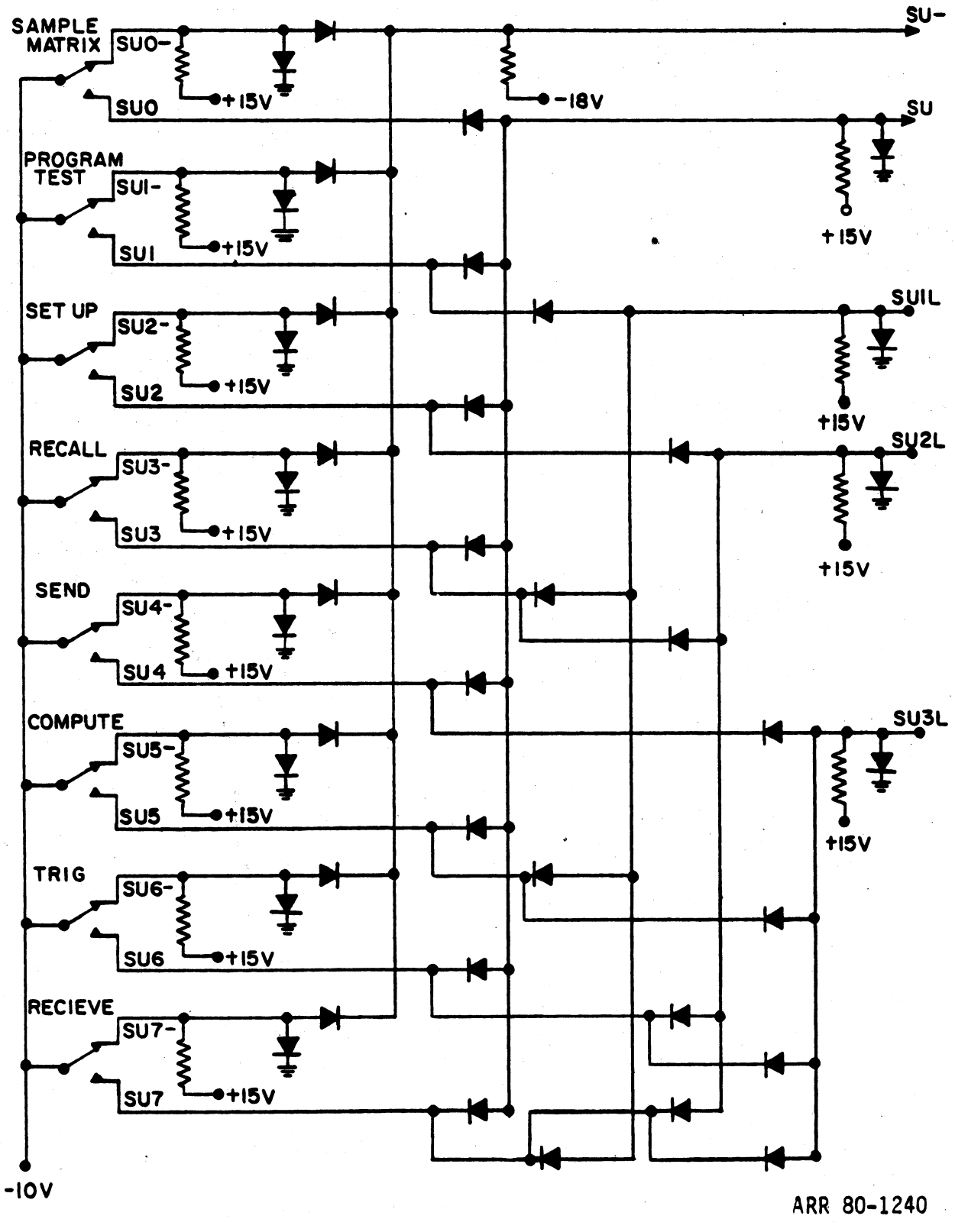


Figure 4-30. Set Up Buttons and Associated Lines.

lines are true depending on which set up button is depressed. With the depression of the COMPUTE button, line SU- becomes false (0 volts), and SU, SU1L, and SU3L, becomes true. When the RECEIVE button is depressed, all SU-lines are true except SU-. Since the SU-lines are used in the logic for several flip-flops these same flip-flops can be used to test the various set up buttons. The SU-lines and the logic equations in which they appear are listed below:

```
OD =  + /KD1/ (EAK0) *GPH- *SU- TSO
1IC =  (+ /KD1/ *SU
       ) /TOB/
1 OB6 = + /KD1/ *SU3L
1 OB5 = + /KD1/ *SU2L
0 OB2 = + /KD1/ *SU1L
```

(2) Each of the above equations has been previously tested while running other test tapes. In the D test tape the logic for OB6, OB5, and OB2 was tested including the above equations. In the test of these equations the FALT exciter flip-flop E1 was used to simulate the SU-lines. When E1 was zero set, the SU-lines were true. Therefore, in the test of the SU-lines, flip-flop E1 will be one set. In the set up button tests the E1 flip-flop is addressed and one set.

(3) The first set up button is tested during marker 216. The instructions in TM 9-1220-221-34/5 indicate that the PROG TEST button must be depressed before starting the SDR. With the PROG TEST button depressed, SU and SU1L, lines are true and the other SU-lines are false. Line SU1L is used in the logic for OB2 flip-flop and SU is used with the IC flip-flop. Therefore, when the PROG TEST button is depressed the other logic is true, OB2 should zero set and IC should one set. The remaining SU-lines are false and should not affect any of the computer flip-flops. In order to both one set IC and zero set OB2, the BSC command will be used to provide the necessary 1 and 0 clock pulses.

(4) The test of the first set up button can be followed by referring to TM 9-1220-221-34/5 at marker 216. The first command, OSA, is followed by the one setting of TO, D, E1, OB2, and TSO. Once these flip-flops are set, the logic to one set IC and zero set OB2 is true, providing the PROG TEST button is depressed. The next command turns off -18VFT. This is then followed by the BSC command and the flip-flop addresses. To one set IC a 1 clock pulse is required and to zero set OB2, a 0 clock pulse is needed. Therefore, the BSC command is used in this test. Since SU and SU1L, are the only lines true at this time, the OB6, OB5, and D flip-flops should not change state when they are addressed after the BSC command. Once the flip-flops are addressed after the BSC command, the -18VFT is turned on and the FALT one tests IC and D and zero tests OB2, OB5, and OB6. Flip-flop IC was zero set by the OSA and its logic was addressed so it should one set with the clock pulse. Flip-flop OB2 should zero set when clocked and flip-flops D, OB5, and OB6 should not change states when clocked since their logic is false. If no errors are detected by the FALT when the flip-flops are tested it can be assumed that the correct SU-lines are true when the PROG TEST button is depressed.

4-35. DESCRIPTION OF E TEST TAPE--Continued

(5) The E test tape continues by testing the SU-lines for each set up button. The last button tested in the E test tape is the RESET button which is not a true set up button since it does not affect any of the SU-lines. The output from the RESET button, however, does affect several flip-flops. The RESET button is used to reset an overflow or parity error. An overflow or parity error occurs whenever OFLO of PE flip-flops are one set. Therefore, the RESET button whose output is known as *ER is used in the zero input logic of these flip-flops. In addition, *ER is used in the zero input logic of the D flip-flop; it follows then that the OFLO, PE, and D can be used to test the RESET button. The RESET button is tested in the E test tape during marker 224.

f. Test of Control Panel Neon Lamps.

(1) The neon lamps located on the computer control panel are tested in the E test tape beginning with marker 226. Following marker 225 the POWER READY indicator on the control panel should be on because the PS flip-flop was zero set with the last OSA command in marker 225. The POWER READY indicator should flash when the MARGINAL TEST switch is placed in any one of its ON positions. By placing the switch on, the output from the 10-Hz oscillator called MOSC on network C board is tied to the POWER READY neon driver circuit through the MARGINAL TEST switch S1 on the control panel. In figure 4-31 the POWER READY incator circuitry is illustrated.

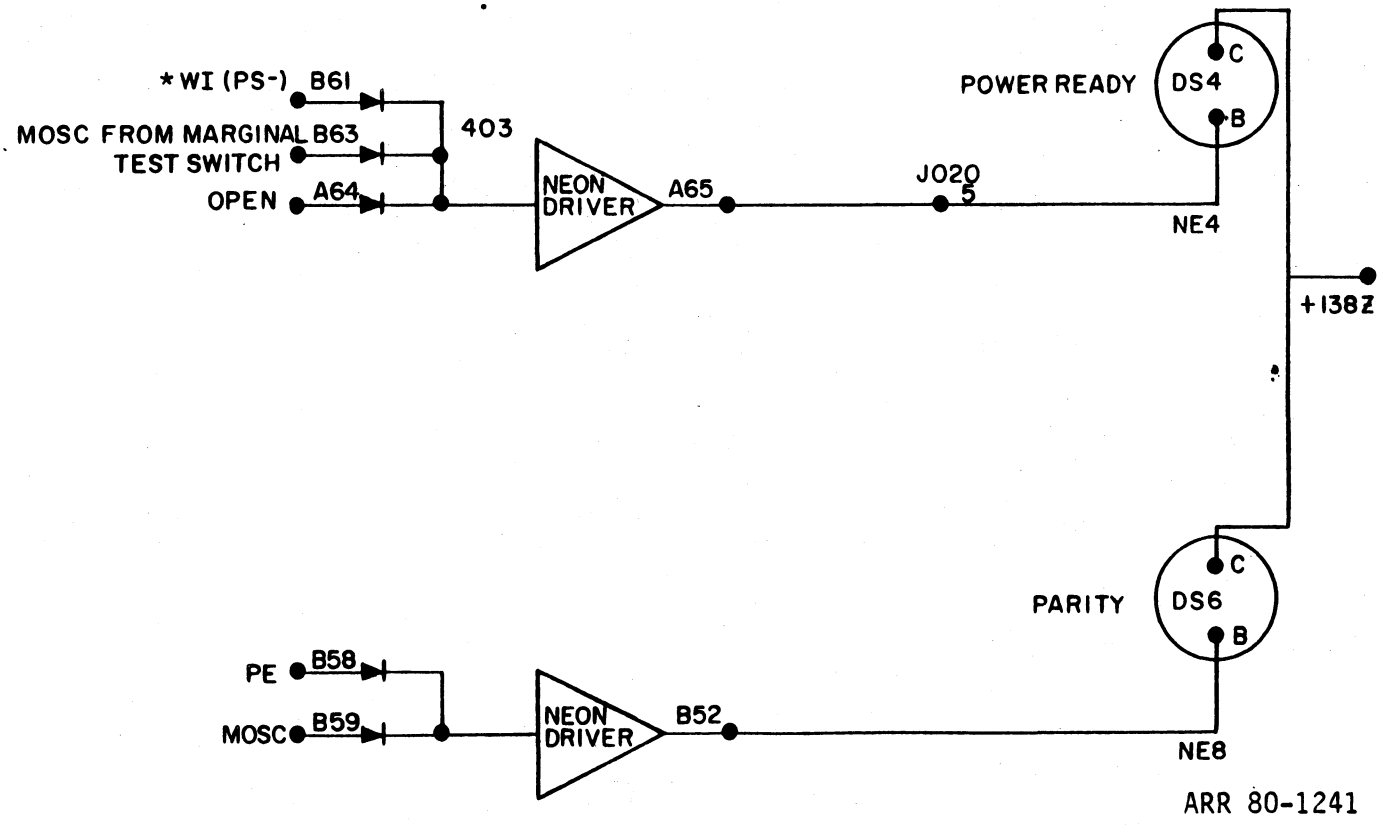


Figure 4-31. Power Ready Lamp and Parity Lamp Circuitry.

(2) During normal computer operation the PARITY indicator is on except when the PE flip-flop is one set by a parity error at which time the PARITY indicator will flash. To test the PARITY indicator to ensure it flashes, the PE flip-flop need only be one set. The output from PE is "anded" with MOSC (10-Hz oscillator) at the neon driver circuit gate. In figure 4-31 the PARITY indicator circuit is illustrated. In normal operation PE is zero set, making the driver input gate false; the PARITY indicator is on and not flashing at this time. When PE one sets, the PARITY indicator begins to blink since the neon driver circuit will now oscillate due to MOSC. The PARITY and ERROR indicators are tested during marker 229 when PE and OFLO are both one set. Several negation tests ("and" tests) are also performed during the same marker when flip-flops OB3, OP1, K, and CLC are addressed and one set. When K is one set, the IN-OUT indicator should be off; CLC should turn off the COMPUTE indicator and the NO SOLUTION indicator should not be flashing since OP2 is zero set. Several negation tests are also performed on the logic for the KEYBOARD indicator at the end of the neon lamp tests.

l. Keyboard Testing.

(1) The keyboard is the last input device to be tested in the E test tape. The outputs from the keyboard and the mechanical reader are tied together in the control panel to form a single input to the computer. The SM (sample matrix) and RECALL keys on the keyboard were tested during the set up button tests earlier in the E test tape. The output from the keyboard is in eight-level field data code which is fed to the input register composed of the D flip-flops. The flip-flops in the input register are used to test the keyboard.

(2) The test explanation may be followed by referring to the test tape E program printout beginning with marker 237. In the first test, the 0 key is tested and must be depressed once the tape reader has started. With the depression of the 0 key, the eight I-lines from the keyboard are in the following configuration 00110000. A zero indicates that no voltage is on the corresponding I-line while a one indicates -10 volts.

(3) With the first command on tape, the D flip-flops are all zero set; the flip-flops for the input/output mode and keyboard are then addressed. The zero-set E18 and 1SA command follow, allowing the output from the keyboard to set the D flip-flops. After several seconds the FALT begins to test the D flip-flops which should be set according to the keyboard output. In the first test, all I-lines were false except I-lines 5 and 6. Therefore, all of the D flip-flops should be false except D5 and D6. Each key is tested in the same manner. The plus (+), minus (-), decimal (.); ENTER and CLEAR keys also output a field data code.

4-35. DESCRIPTION OF E TEST TAPE--Continued

h. Write Switch Tests.

(1) There are 24 write switches located on the two write switch circuit boards in the computer. These write switches may be divided into three groups. The first group of eight write switches controls the center taps of all write heads in main memory. The second group of eight write switches controls the writing of ones in memory; the third group of eight controls the writing of zeros. The write heads and switches for main memory are illustrated in figure 4-32. In writing zeros in channel 000 it is necessary to turn on the write switch for the center tap, the write switch controlling the prime or zero side of channel 000 write head and to one set write flip-flop MW0. The 24 write switches used for channel selection are all addressable (see table 4-14) and are tested in the E test tape beginning with marker 252.

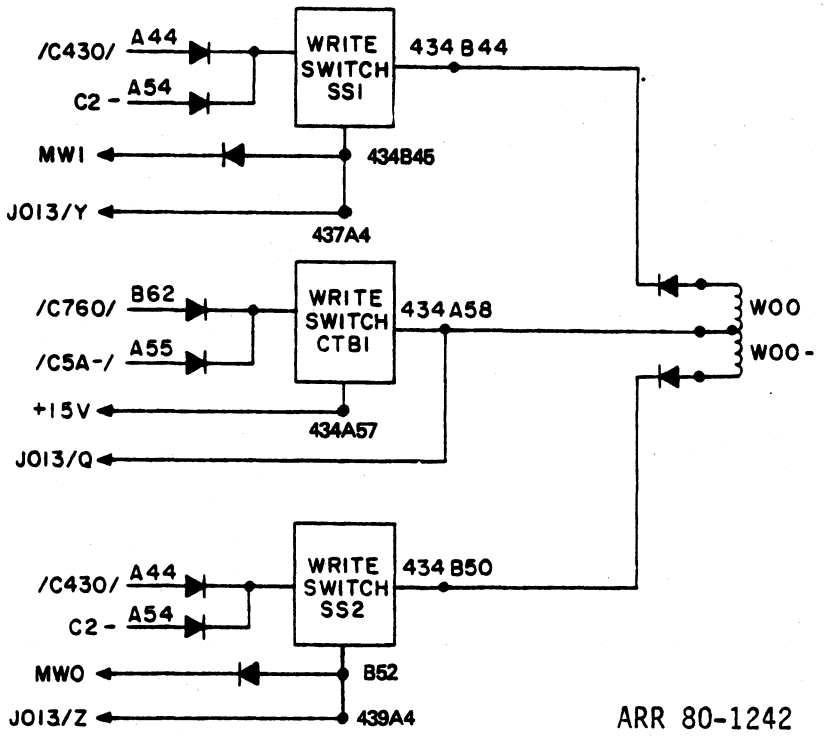


Figure 4-32. Write Switch Testing.

(2) In normal computer operation the storage selection switch located on the inside of the computer is used to determine the number of main memory channels that are active or hot. It is impossible to write into those channels which have not been activated by the storage switch. The storage switch controls the number of channels which are activated by controlling the +35 bias voltage used in the write switches. Thirty-five volts are used as the bias voltage for the base of the final transistor stage in each write switch. When the FALT is connected to the computer and the WR SW switch on the FALT front panel is placed in the ENABLE position all main memory channels are activated for testing purposes. When the computer memory is to be loaded from the SDR all channels again must be activated.

(3) Center tap write switch CTB1 is the first switch to be tested in the E test tape. Logic drivers /C760/ and /C5A/ make up the logic for CTB1 switch and both of these drivers were tested in the B test tape. The test explanation of CTB1 may be followed by referring to the test tape E program printout. After the OSA command in the first test of marker 252, the logic for CTB1 is true; the 1TA command then follows and CTB1 is addressed and tested. The 1TA command is used to test the write switches since they are addressable and are directly connected to the FALT. With the logic true the normal output of switch CTB1 is a positive voltage of about 15 volts. Before this positive output voltage can be used by the FALT error-sensing circuits, it must be converted to a negative voltage. This is accomlished by the write switch conversion amplifiers located on the network D and E boards in the FALT. To ensure voltage from the center tap write switches is positive, the main memory write flip-flops MS1 and MW0 are both zero set since their one-set outputs are connected to the center tap write switches through the write heads. If CTB1 is turned on in the first test, no error is detected by the FALT and the next test which is also a one test follows. The third test of the switch is a negation test. After addressing the logic, driver /C760/ is false and the switch which should also be false is zero tested using the OTA command. In the test tape E program printout following the third test of CTB1 the terms MSU0 and C760 appear. These terms indicate that the diode associated with driver /C760/ in gate MSU0 is under test. Although term MSU0 does not appear in the computer wire list (TM 9-1220-221-34/6) it is the logic term used to describe the "and" gate formed by the logic drivers /C760/ and C5A-/ on write switch circuit board. This "and" gate is the input gate for write switch CTB1 and is effectively tested when the write switch is tested. The diode associated with /C5A-/ is tested in the fourth and final test of CTB1 in marker 252. The remaining center tap write switches are tested in a similar manner.

(4) The test of write switch SS1 begins at marker 255. This write switch controls the writing of ones in eight different channels. Therefore, in testing SS1 there are eight separate tests performed. In the first test of SS1 the center tap write switch CTB1 is turned on by the OSA command and the +15-volt output from CTB1 is present on the center tap of channel 000 write head as illustrated in figure 4-32. The logic for SS1 is also true, and if SS1 turns on, the +15 volts will be present on the output line to the FALT from the SS1 write switch. This voltage is used to indicate that SS1 is turning on; it is tied to the FALT through J013 pin /Y. In each set of SS1 a different center tap write switch is turned on to test each write head that is associated with SS1. All main memory write heads and memory connecting plugs can be tested for continuity by using this method of testing write switches.

4-35. DESCRIPTION OF E TEST TAPE--Continued

i. Main Memory Write Flip-Flop Tests.

(1) The main memory write flip-flops MW1 and MW0 are located in circuit boards 437 and 439. The one-set output from the main memory write flip-flops feed eight "or" diodes. The "or" diodes on the one-set output of MW1 are then tied to the eight write switches SS1 thru SS15. When writing into the memory, the +15 volts from the center tap write switch is tied to the one-set output of MW1 through the write head, the SS write switch, and the "or" diode. When +15 volts is tied to the one-side output of MW1 and the flip-flop is one set, the FOT line is false and the flip-flop can be one tested. To one test either main memory write flip-flop it is necessary to activate a write head by turning on a center tap write switch and an SS write switch. When 15 volts is not present on the one side output of the main memory write flip-flop, the FOT line output is about -3 volts and there is an error indication on the FALT when the flip-flop is one tested. If one of the eight "or" diodes tied to the output of either main memory write flip-flop is open, an error indication will appear during the logic test of that flip-flop. Therefore, before beginning the logic tests of MW1 and MW0 the eight "or" diodes on the output of each flip-flop must be tested. These diodes are tested in the E test tape beginning at marker 280. The test explanation may be followed by referring to the test tape E program printout.

(2) After the OSA command in the first test, write switches CTB1 and SS1 are both on and +15 volts should be present on the output of MW1 providing the first "or" diode on pin A4 of board 437 is conducting. Write flip-flop MW1 can now be one set and one tested. The same diode is checked again in the second test. However, the center tap write switch CTB8 is now on together with SS1. After CTB8 is turned on, MW1 is one set and one tested completing the test of the first "or" diode. Each diode is tested in the same manner. In testing the second "or" diode, SS3 must be turned on. To test the third diode SS5 must be turned on. Once the eight "or" diodes for each main memory write flip-flop are tested the E test tape proceeds with their logic tests beginning at marker 284. The logic tests of the main memory write flip-flops are the same type of tests performed on logic flip-flops.

j. Read Switch Tests.

(1) There are 66 read switch circuits located on the eleven read switch boards in the computer. There are 64 channels in main memory. Therefore, only 64 read switches are used. The read switch circuit is tied directly to the memory read head which is constantly reading information as the memory rotates. However, no information flows from the read switch until it has been activated by computer logic. There are two types of information words in the computer memory, the number word and the program word. Since two different types of words exist, there are two different sets of logic to activate any one read switch. Illustrated in figure 4-33 is the read switch for channel 000. When a program word is to be read from channel 000 the "and" gates CPU0 and CPL0 are true; information will then flow from the read switch to the read amplifier circuit board.

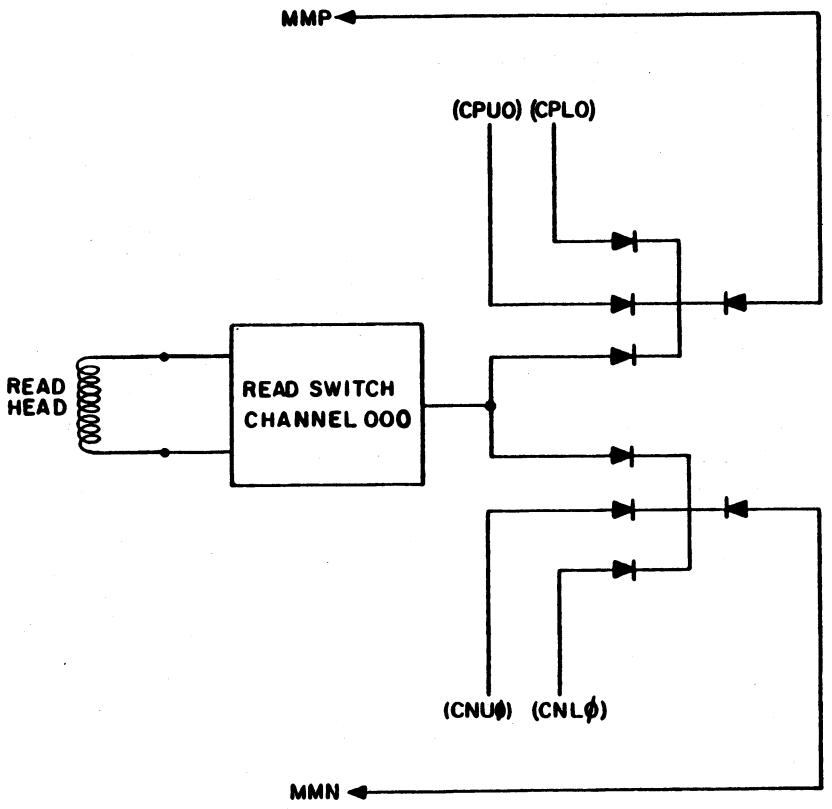


Figure 4-33. Channel "000" Read Switch Circuitry.

(2) The read switch test beginning at marker 296 is divided into two sections. In the first section each read switch is addressed and tested using logic associated with the reading of a number word. In the second section the read switches are again addressed and tested, this time using logic associated with a program word. The ON flip-flops are used to select the read switch when a number word is to be read while the CP flip-flops select the switch when a program word is to be read. During read switch testing, the FALT exciter flip-flops are also involved in selection. The read switch for channel 000 is turned on to read a number word by "and" gates (CNUO) and (CNLO) as shown in figure 4-33. The "and" gates (CPUO) and (CPLO) will also turn on this read switch if a program word is to be read. The logic for these "and" gates is illustrated in figure 4-34. Logic gate (CNLO) is true when flip-flop CN2, CN3, and CN4 are zero set and when term EM5 from the FALT is true. Term EM5 is an "and" gate whose inputs are exciter flip-flops E1, E2-, and E3. The "and" gate (CNUO) is composed of the CN flip-flops and exciter flip-flop E7. To turn on the read switch for channel 000, the CN flip-flops must all be zero set and the exciter flip-flops must also be properly set. The FALT, by using the exciter flip-flops, can accurately control the read switches even when the computer logic is defective.

(3) The first read switch test in marker 296 is reproduced below:

OSA E7 E3 E1 E4 1TA MNF

4-35. DESCRIPTION OF E TEST TAPE--Continued

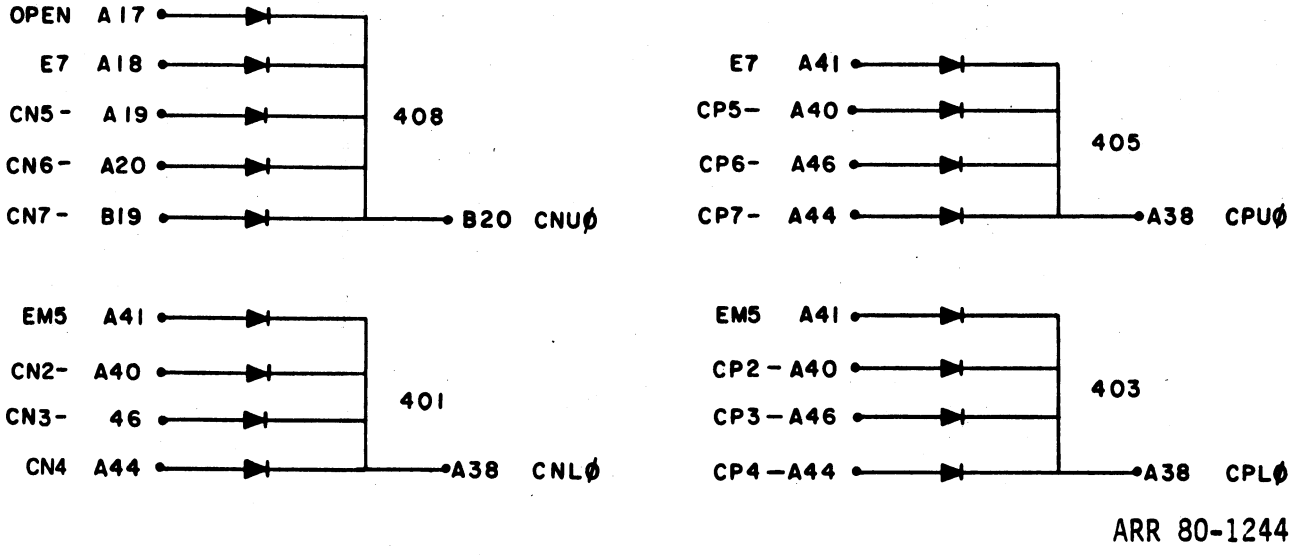


Figure 4-34. Read Head Logic.

(4) The CN flip-flops are all zero set by the initial OSA command. The E7 term in the FALT is then one set, making gate (CNUO) true. After the E3 and E1 flip-flops are one set, term EM5 is true and gate (CNLO) will be true. Once the "and" gates are true the read switch for channel 000 should be on. The output from the channel 000 read switch is then fed to the emitter-follower circuit on the read amplifier board as shown in figure 4-33. The output from the emitter-follower feeds the threshold circuit and transistor amplifier circuit which is used to test the read switch. The collector of the transistor is tied to the FALT through connector J013. When the read switch is on, term MNF is true and no error is detected in the FALT. In the first read switch, test exciter flip-flop E4 was also one set to ensure that only the read switch for channel 000 was addressed. In the second section of the read switch tests when channel 000 is tested for a program word the CP's are set and term MPF from the other read amplifier board is addressed thus testing the read switch for program operation. Negation tests of the read switch diodes are also performed in the E test tape; for the number word operation these tests begin at marker 313. Each read switch is tested by addressing the computer logic and the necessary FALT exciter flip-flops, then testing terms MNF or MPF.

k. Memory Tests.

(1) The last portion of the E test tape is devoted to testing the computer memory. Each channel in main memory is tested. In addition, the channel containing the eight recirculating loops is also tested. The explanation of the test of channel 000 may be followed by referring to the test tape E program printout at marker 346. The first command in the tape is OSA. With this command, write switches CTB1, SS1, and SS2 are on, thus selecting the write head for channel 000.

Once the exciter flip-flops E7, E4, E3, and E1 are one set, the read switch for channel 000 is on. The FALT strobe control flip-flop E5 is then one set, allowing the FALT to control the main memory read flip-flops. MW0 is then one set and zeros are written into memory during the time delay. The OSF command then follows, and the read flip-flops are zero set; MW0 is also zero set along with E5. With E5 zero set, the strobe output from the network C board is a constant negative voltage of about 10 volts; this will allow signals from the read switch to set the read flip-flops. Flip-flop MW1 is then one set and a time delay follows while ones are written into channel 000 of the memory. As the memory rotates, the ones are read by the read switch and the main memory read flip-flops should both one set. The FALT then one tests the read flip-flops. If channel 000 is defective, the read flip-flops will not be one set and an error will be detected. MW1 is then zero set and MW0 is one set. A time delay follows while zeros are written into memory. The read switch should then begin to read the zeros and zero set the main memory read flip-flops which are zero tested by the FALT.

(2) In the test of a memory channel, the channel is first cleared or zeroed; ones are then written and the read flip-flops are tested. The next step is to write zeros and again test the read flip-flops. Each channel, therefore, is tested for writing both ones and zeros.

(3) The E test tape continues by testing the remaining channels in memory. Since the logic for each channel is different, the flip-flops which are addressed for each test will differ. In testing channel 002 flip-flops CN2, CP2, and C2 must be one set to select the read and write circuitry for channel 002. The recirculating loops or registers are tested during marker 378 in the E tape. The loops are tested for both ones and zeros. When the two 16-word loops are tested the intermediate read flip-flops are tested in addition to the read flip-flops located at the end of the loops.

4-36. COMPUTER F1T and F0T RESPONSE LINES

Computer flip-flop circuit outputs are sensed in the FALT through the F1T (flip-flop 1 test) and F0T (flip-flop 0 test) lines. Every flip-flop circuit is connected to both an F1T and F0T line through "or" diodes located on the flip-flop circuit board. For example, the one-set output of flip-flop DA5 is connected to the F1T1 line through "or" diode CR43 and the zero-set output is connected through "or" diode CR80 to F0T1 line. The flip-flop circuits located on board 230 thru 240 are tied together to form F1T1 and F0T1 lines as shown in figure 4-36. Lines F1T1 thru F1T7 feed the seven "or" diodes on circuit boards 101 and 433. The outputs from these two "or" gates are tied together to form a single one test response line known at F1T which is connected to the FALT through the red FALT cable. Before any flip-flop circuit can be one or zero tested it must be addressed by the FALT and since only one flip-flop circuit can be addressed at any given time only one response line is required for one testing and one line for zero testing.

4-37. FLIP-FLOP ADDRESS AND RESPONSE LINES

a. General. All computer flip-flop circuits including read and write flip-flops may be set and tested using the address and response lines.

b. Specific Testing.

(1) Two conditions are required to one set or zero set any flip-flop. First a true signal (-6 volts) on the one or zero set input line and second a 1 or 0 clock pulse. Assume the flip-flop in figure 4-36 to be zero set and a true signal (-6 volts) to be present on pin B40 the one-set input line. When a 1 clock pulse is applied to diode CR46 the flip-flop will one set. It is also possible to one set this flip-flop using the DU/DL address lines. By applying -6 volts to the DU/DL address line, pins B37 and B34 the address gate composed of diodes CR60 and CR63 will be true and -6 volts will be present on the one set input line via diode CR35. Bias voltage for CR35 is supplied from the -18 volt test voltage (-18VFT) on pin B24 through resistor R13. The flip-flop will one set with a 1 clock pulse.

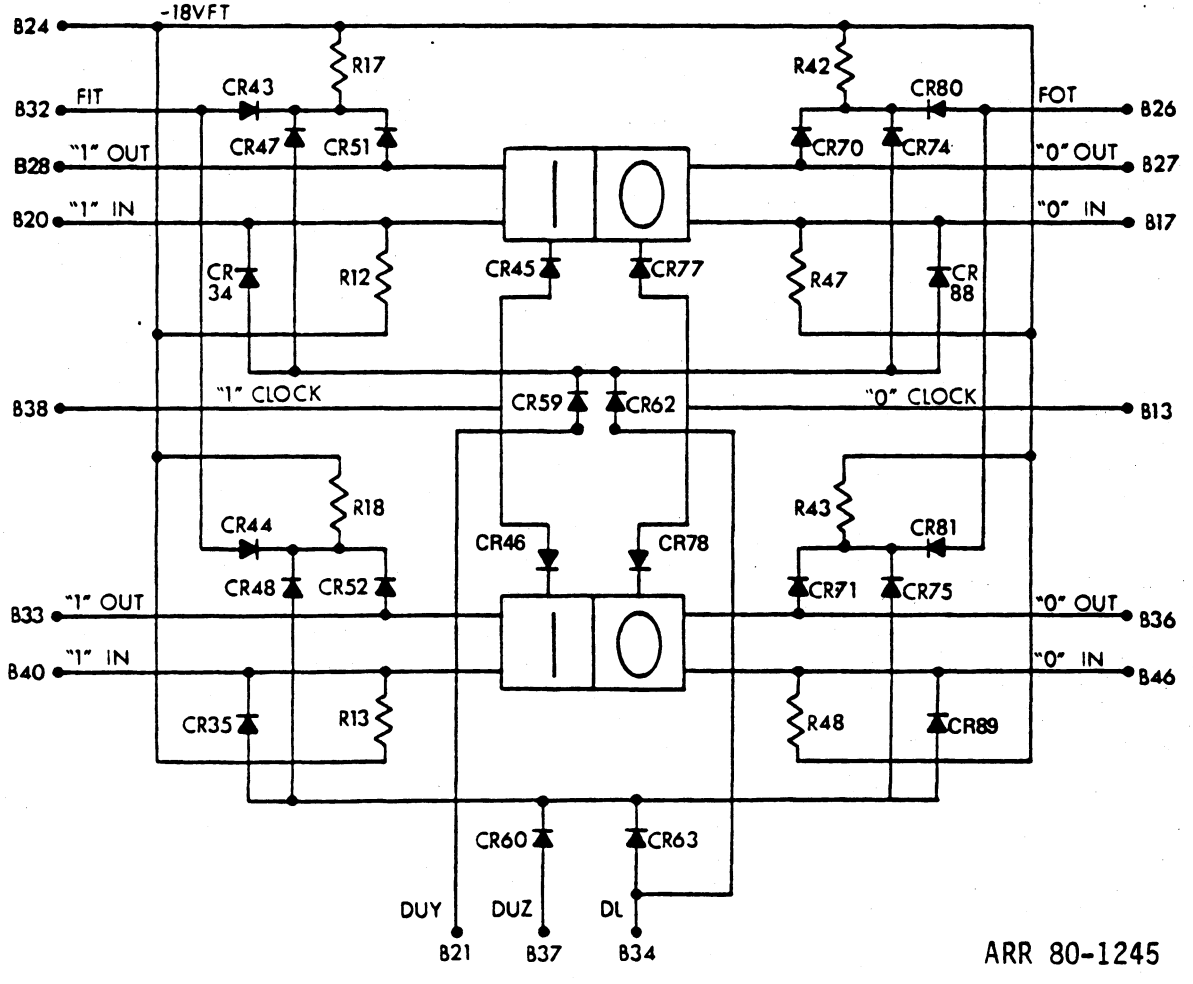


Figure 4-35. Flip-flop Address and Response Lines.

(2) Once the DU/DL address gate is true, it is also possible to zero set the flip-flop because -6 volts or a true input signal is also present on the zero-set input line of the flip-flop through diode CR89. However, when zero setting a flip-flop a 0 clock pulse is applied through CR78. By utilizing the DU/DL lines the FALT can control the state of every flip-flop circuit in the computer.

(3) Any flip-flop circuit in the computer can also be one or zero tested by the FALT. Assume the flip-flop in figure 4-35 to be in the one-set state. When the flip-flop is one set, -6 volts will be present on the one-set output line of the flip-flop. Diode CR52 is fed by the flip-flop; diode CR48 is fed by the DU/DL address gate. These two diodes form the response line gate whose output is true when the flip-flop is one set and the DU/DL address gate is true. Bias voltage for the response line gate is provided through resistor R18. The FALT senses or tests the output of the flip-flop circuit through the F1T-line diode CR44. For a complete description of the computer F1T and F0T lines, refer to paragraph 4-36. The flip-flop is zero tested in the same manner except the FALT senses through the F0T line.

(4) The DU/DL lines and the -18 volt test voltage originate in the FALT; the 1 and 0 clock pulses, however, are controlled by the FALT.

4-38. FALT EXCITER FLIP-FLOPS

a. General. There are eight exciter flip-flops located in the FALT. These flip-flops are connected to the computer through the FALT cables and are used to simulate or control various logic terms for testing purposes.

b. Specific Use of Exciter Flip-Flops.

(1) The use of each exciter flip-flop while logic testing is outlined in table 4-10. In the first column, at the left, the exciter flip-flop is listed; the connector and pin is listed in the second column and the computer term that the exciter flip-flip is simulating or controlling is outlined in the third column. The last column is a description of the use of the exciter flip-flop. Table 4-10 contains only the use of the exciter flip-flops while logic testing the computer. When the read circuitry and memory are tested, the exciter flip-flops are used in a different manner. In testing the read circuitry each "and" gate used in the read head selection contains one exciter term. The "and" gate (CNL0) contains exciter term EM5. If the exciter term is false, the read head selection gate will also be false. Term EM5 is an "and" gate located in the FALT composed of flip-flops E3, E2-, and E1. Contained in table 4-11 are the exciter terms that are used while testing the read circuitry and memory.

(2) When testing the computer using the control box it is sometimes necessary to address and set the exciter flip-flops. When an exciter flip-flop is one set, the corresponding indicator on the FALT front panel will light. The exciter flip-flop DU/DL address is listed in TM 9-4931-204-34/1.

4-38. FALT EXCITER FLIP-FLOPS--Continued

Table 4-10. FALT Exciter Flip-flops

Exciter term	Cable and pin	Computer term	Remarks
E1	J12/Z	GPRC-	The one output of E1 is used to simulate computer term GPR- when logic testing mode control flip-flops E and K.
E1-	J12GG	ESU	The zero output of E1 simulate SU-lines when testing flip-flop logic; with E1 zero set, all SU-lines except SU- are true for testing purposes. E1- is also used as the I-line input when D1 is tested in the D test tape.
E2	J12AA	OPE	E2 simulates term OPE when output driver D100 thru D800 are tested. These output drivers are tested when they are used to simulate other terms; D200 is used as I4G when D4 is tested.
E2-	J12HH	FH	The zero output of E2 is used as term FH when zero input logic of K is tested.
E3	J12BB	FB	E3 simulates input terms FB, FBPR and FBCP in the CP6 logic tests. These input terms are used by an external input device to indicate to the computer that information is about to be read.
E3-	J12JJ	FBH	The zero output of E3 is used as term FBH when the zero input logic of K flip-flop is tested.
E4	J12CC	EER	E4 simulates terms ER when PE and OFLO flip-flops are tested and CTT when CP7 is tested.
E4-	J12KK	F1	Matrix F-line test; if two matrix buttons are not depressed E4 will indicate an error when zero set.
E5-	J12DD	TC-	Timing control prime; E5 is used to simulate this signal when testing flip-flop logic.
E5-	J12/Q	FSC-	FALT strobe control; E5- is used to control the strobe pulse while testing memory.
E6	J15/G	ET6	E6 controls the output of the teletype oscillator when F32 is tested.
E7	J15S	ET7	E7 controls the output of the teletype oscillator when F32 is tested during the C7 logic tests.

Table 4-11. Exciter Terms Used in Read Selection

Exciter term	Logic			Cable and pin	Gates	
EM2	E3-	E2	E1	J12/S	(CNL1) (CPL1)	(CNL6) (CPL6)
EM3	E3-	E2	E1	J12/T	(CNL2) (CPL2)	(CNL5) (CPL5)
EM4	E3	E2-	E1-	J12/U	(CNL3) (CPL3)	(CNL4) (CPL4)
E6	E3	E2	E1-	J12EE	(CNL0) (CPL0)	(CNL7) (CPL7)
EM6	E3	E2	E1-	J12/W	(CNX)	(CPX)
E4-				J12/X	(CNU2) (CNU2)	(CNU5) (CNU5)
EM5				J12/V	(CNU1) (CNU1)	(CNS4) (CPS4)
E7				J12FF	(CNU0) (CPU0)	(CNS3) (CPS3)
EM7	E8			J12/W	(CNU4) (CPU4)	(CNS5) (CNS5)

4-39. PROBABLE ERROR FROM FALT FRONT PANEL INDICATION

a. Basically the FALT addresses and tests logical terms in the computer. A DU (upper address) and a DL (lower address) selects the term to be set or tested. The F1T (flip-flop one test) line and F0T (flip-flop zero test) line are then monitored. If the voltage output on the F1T and F0T lines are correct, the test passes and another term is addressed and tested. This process is continued until all terms have been tested. The test indicators 1TF and 0TF indicate the test being performed. The 1SF and 0SF indicators indicate that a particular flip-flop is to be set up either the one-set or the zero-set state. The F1 and F0 indicators indicate the output from the F1T and F0T lines from the computer. When a test tape has stopped because of a malfunction in the computer, the TEST ERROR indicator in the FALT will flash. This is a result of the F1T and F0T lines inputting incorrect voltages to the FALT threshold amplifiers. When a logical term is being one set or one tested the F1T-line should be -6 volt level and the F0T-line should be at the 0-volt level. When a logical term is being zero set or zero tested the F0T-line should be at a -6-volt level and the F1T-line should be at a 0-volt level.

4-39. PROBABLE ERROR FROM FALT FRONT PANEL INDICATION--Continued

NOTE

If the lines have the correct voltages on them, the TEST ERROR indicator will not flash and the F1 and F0 indicators will not light.

b. When a test tape has stopped and the TEST ERROR indicator is flashing, the F0 and F1 indicators will indicate the type of malfunction that caused the error.

c. If the logical term was to be one set or one tested and the ERROR indicator flashes, the F0 and F1 indicators will be in one of the four following configurations.

(1) Neither the F0 nor the F1 indicator is lit. This indicates a shorted output from the particular term or a shorted output to the F1T line or open F1T diode. See paragraph 4-40 for procedure to locate and correct malfunction.

(2) Both F0 and F1 indicators are lit. This indicates that the F0T line which is supposed to be at 0 volts is -6 volts or an open DU/DL diode. See paragraph 4-41 for procedure to locate and correct malfunction.

(3) The F1 indicator is lit; the F0 indicator is not lit. The F0T-line which is supposed to be at 0 volts is at some potential between 0 and -6 volts. See paragraph 4-42 for procedure to locate and correct malfunction.

(4) The F0 indicator is lit, the F1 indicator is not lit. This indicates a logical error to the input of the circuit board or a faulty circuit board. See paragraph 4-43 for procedure to locate and correct malfunction.

d. If the logical term was to be zero set or zero tested, the configuration would be as follows:

(1) Neither the F0 nor the F1 indicator is lit. This indicates a shorted output to that particular term, a shorted output to the F0T line or open F0T diode. See paragraph 4-40 procedures to locate and correct malfunction.

(2) Both the F0 and the F1 indicator are lit . This indicates the F1T-line which is supposed to be at 0 volts is at -6 volts, or DU/DL diode is open. See paragraph 4-41 for procedure to locate and correct malfunction.

(3) The F0 indicator is lit; the F1 indicator is not lit. The F1T-line is supposed to be at 0 and -6 volts. See paragraph 4-42 for procedure to locate and correct malfunction.

(4) The F1 indicator is lit; the F0 indicator is not lit. This indicates a logical error. See paragraph 4-43.

4-40. PROCEDURES IN TROUBLESHOOTING WHEN FO AND F1 INDICATORS ARE NOT LIT AND ERROR INDICATOR IS FLASHING

a. Determine the test being conducted by cross-referencing the marker index number in the test tape program printouts. The term being one or zero tested is now known. Use tables 4-13 thru 4-15 to find the particular board location of the term being tested and its output pin; use the one side if being one tested, zero side if being zero tested. Replace that board and rerun test tape. If error is still present, use TM 9-1220-221-34/6 and look up that particular term. There will be a list of all circuit board connector pins connected to that output. Pull out each of the boards listed, one at a time, except the board that the term is located on until the test error lamp stops flashing. If this does not correct the problem, carefully examine each one of the board and pins listed for that term. If this does not locate the problem, use an ohmmeter to determine which lead(s) is shorted to ground.

NOTE

For clarity it will be assumed that a one test is being conducted.

b. If the -6 volts is present at the one output pin, F1T-line circuitry is defective. Referring to the appropriate schematic, find the F1T output pin. Using a voltmeter, check that -6 volts is present at that pin. If not, again referring to the schematic check the input to the DU and DL input terms. If DU or DL term is not present as represented by -6 volts at each pin, there is a short at that pin. Locate it using component list (TM 9-1220-221-34/7) and ohmmeter. If DU and DL input terms are correct then one of the F1T-lines is defective. Using the component list (TM 9-1220-221-34/7) look up the board and pin number of that particular F1T-line. Assume that when that board and pin are referenced F1T1-Line is indicated. Using the wire list (TM 9-1220-221-34/6) look up F1T1. Replace each of the boards except that board being tested until the short is removed (-6 volts is present). If this does not correct the problem carefully examine each one of the pins listed for that term. If this does not locate the problem use an ohmmeter to determine which lead(s) is shorted to ground.

c. If both F1T1 and output are true, replace boards 101, 433, and 434. These boards contain the "or" gates whose outputs are F1T and FOT. (Refer to fig. 4-36). In this example F1T1 is an input term to board 101 pin A2 as found by referencing term F1T1 in the wire list. The output of this "or" gate referencing the schematic of the power control C board is on pin B1 (F1T). By using a voltmeter and/or an ohmmeter and the wire list, the pin can be detected and corrected.

4-41. PROCEDURE FOR TROUBLESHOOTING WHEN FO AND F1 INDICATORS ARE BOTH LIT AND ERROR INDICATOR IS FLASHING

a. Continue running test tape until only one light is lit.

b. Replace board indicated in the tape listing.

4-41. PROCEDURE FOR TROUBLESHOOTING WHEN FO AND F1 INDICATORS ARE BOTH LIT AND ERROR INDICATOR IS FLASHING--Continued

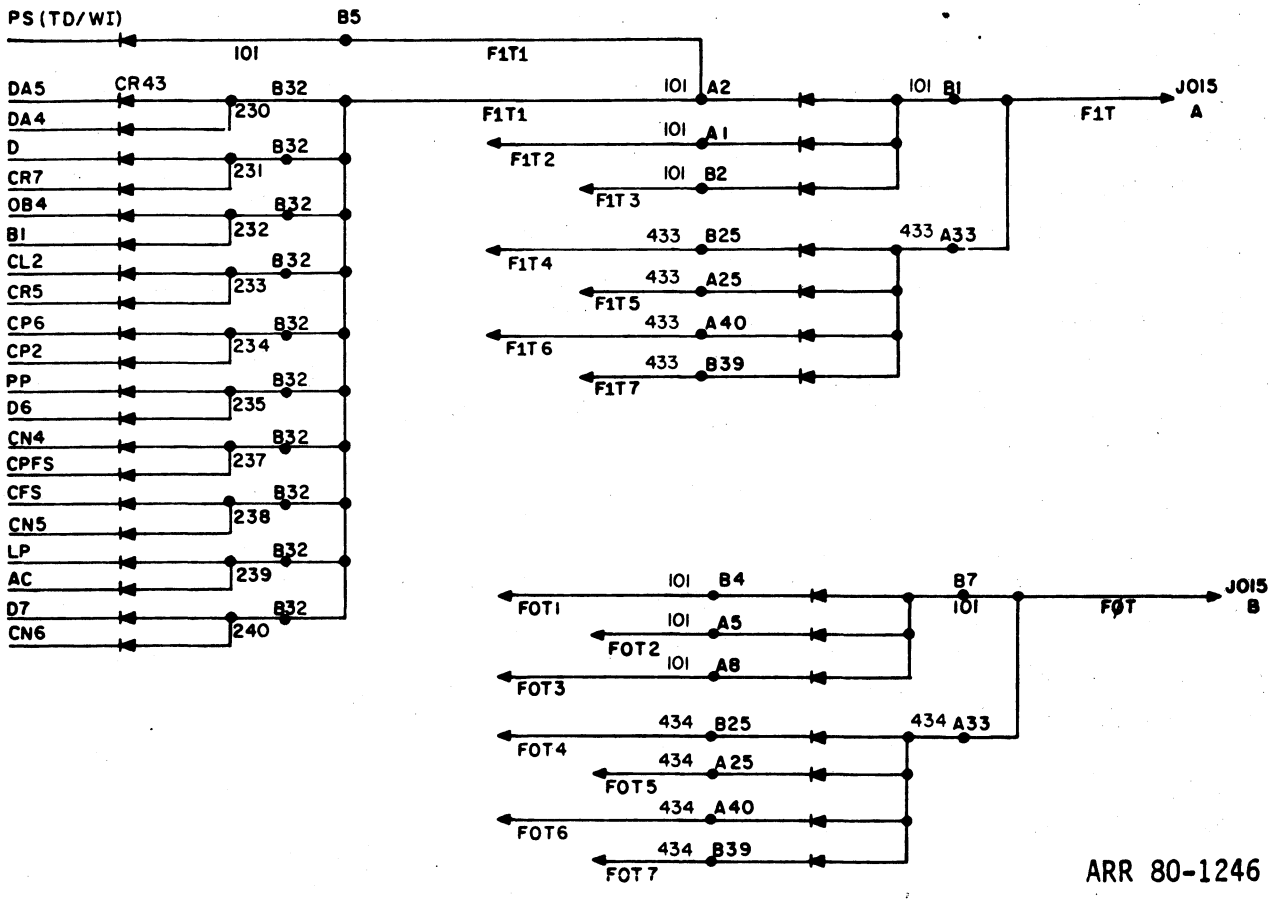


Figure 4-36. Computer F1T and FØT Response Lines.

4-42. PROCEDURE FOR TROUBLESHOOTING WHEN ONE SET OR ONE TEST COMMAND HAS BEEN EXECUTED AND F1 IS ON AND ERROR INDICATOR IS FLASHING

Follow the same procedure as above. Replace board indicated in tape listing.

4-43. PROCEDURE FOR LOCATION AND CORRECTION OF LOGIC MALFUNCTIONS IN THE COMPUTER

a. No absolute step-by-step procedures will be given. The method of approach will be given in the form of an example. The example given is based upon a typical test tape listing from TM 9-1220-221-34/2. It is possible that in the future, minor changes in logic may appear but the listing will be similar in format.

b. To analyze and correct malfunctions the list of logic equations must be used (TM 9-1220-221-34/1/1). In addition, the following TM's must be available.

(1) TM 9-1220-221-34/2, test tape B program printout.

(2) TM 9-1220-221-34/3, test tape C program printout.

(3) TM 9-1220-221-34/4, test tape D program printout.

(4) TM 9-1220-221-34/5, test tape E program printout.

(5) TM 9-1220-221-34/6, wire list.

(6) TM 9-1220-221-34/7, component list.

c. If the control box C-4020 is available, it offers the following advantages in malfunction isolations.

(1) It verifies that the test tape has not been misread and that the error is legitimate.

(2) It saves the time necessary to back up and rerun the test tape.

(3) It permits the maintenance man to directly address a particular flip-flop, logic driver, etc at the generating board. However, this measurement by the FALT is taken at that particular board and does not detect broken wires, poor solder connections, and defective diodes in other logic circuits where the addressable term is used.

NOTE

Refer to TM 9-4931-204-34/1 for operation and use of the control box.

4-44. MALFUNCTION ISOLATION

a. A B test tape has been placed in the SDR and run. The tape has stopped, indicating a malfunction in the computer. The MARKER INDEX READOUT on the FALT is 692 007.

b. The operator must now consult the technical manual corresponding to the tape used in the SDR. An example of the listing from one of the technical manuals is given below.

692 XP and test, zero side.

```
1SA     E       0E18    OSA     1E18    1TF     XP      .    01 MP.     .
1SA     CL4     E       K       MP      0E18    OSA     1E18    1TF     XP
.   01 KB    .    02 CL4     .    04 XC-     .       .       .       .
1SA     K       MP      0E18    OSA     1E18    1TF     XP      .    02 E-
.   01 KB    K       .    03 IX-     .       .       .       .       .
1SA     E       K       MP      XC      0E18    OSA     1E18    1TF     XP
.   02 XC    .    01 KB    K       .    04 CL4-    .       .       .
1SA     CL4     E       K       MP      IX      0E18    OSA     1E18    1TF
XP      .    03 E       .    01 KB    K       .    02 CL4     .    04 XC-
1SA     K       MP      XC      IX      0E18    OSA     1E18    1TF     XP
.   03 XC    .    01 KB    K       .    04 CL4-    .       .       .
1SA     CL4     XC      0E18    OSA     1E18    1TF     XP      .    04 KB-
.   01 MP-     .       .       .       .       .       .       .       .
```

4-44. MALFUNCTION ISOLATION--Continued

c. Observe that the marker number is 692. The operator selects the marker number corresponding to the readout. Counting commands after the marker number, 1SA, E, 0E18, 0SA, 1E18, 1TF, and XP counts to 007 corresponding to the index number 007 displayed in the readout. The operator then knows the following:

(1) The tape stopped when flip-flop XP was being tested for one state.

(2) It is apparent that XP did not remain in the one state as it should have since it was previously one set during the one set all (1SA) command, hence an error occurred and the tape stopped.

d. Reading across, the action which has taken place up to the point of failure (index 007) is as follows: one set all (1SA) was given to place all flip-flops in the machine in the one state. This command is automatically followed by zero set the following (0SF) generated internally within the FALT. The flip-flop symbols which follow the internally generated 0SF command are all zero set through the set-reset lines of each listed flip-flop. In this case only flip-flop E is listed. Therefore, E should be zero set. The next three commands (0E18, 0SA, and 1E18) act as a clock pulse to zero set all flip-flops. This will result in those flip-flops which have a true condition at their zero set logic inputs being zero set. The next command listed is one test the following (1TF), and the next listed flip-flop, XP will be one tested. This is accomplished by means of threshold amplifiers in the FALT which are capable of discerning, with tolerance, the voltage on a line; in this case, the output of flip-flop XP.

e. It is at this point that the test failed (index 007). Flip-flop XP was found zero set as indicated by the F0 indicator on the FALT being lit (instead of F1) and a flashing error indicator. Flip-flop XP should have remained one set when it was set previously by the 1SA command.

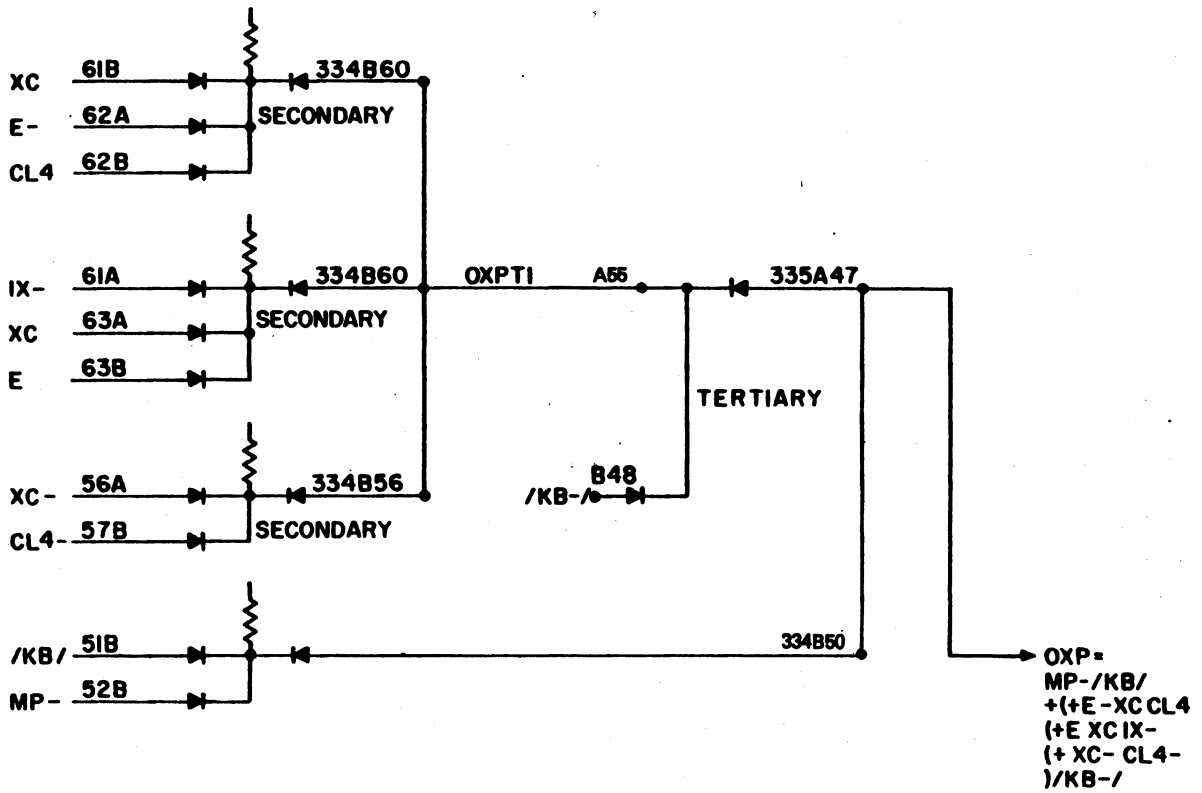
f. Replace each of the boards suggested in the tape listing one at a time, each time backing up the tape or by using the control box C-4020 to enter the given test rerunning the test until the suggested boards and/or assemblies are tested and/or replaced. In this case boards 334, 335, and 436 are listed.

g. If this does not correct the problem, the operator should refer to the logic listing (TM 9-1220-221-34/1/1). The portion of the logic under test in this example is reproduced on the following page for convenience.

h. Inspection of the test listing and the logic equations reveal that this particular portion of the test, the "and" diodes to the zero-set side of the flip-flop XP are being tested by negation tests. A negation test is one in which each input to an "and" gate is made false in turn, while all other are held true. If an "and" gate output is found to be true, the diode held false is thereby shown incapable of holding the output of the entire gate false, hence that particular diode is probably open. The "or" gate (01, 02, etc) and the "and" gate term (MP-, /KB/,

etc) tested is listed, after the numbers 01, 02, etc, offset from the regular column positions. For example, at marker 692, index 007, 01 MP- indicated that the first "or" gate term MP- in the "and" gate of the logic has just been tested.

i. Refer to figure 4-37 for a view of the mechanization of XP logic. For an overall illustration of the equations mechanized, refer to TM 9-1220-221-34/1/1.



ARR 80-1247

Figure 4-37. Mechanization of OXP.

j. Referring to the tape listing, (marker 692 index 007) and starting from the first 1SA or 0SA command preceding the term that failed, and not preceded by an 0E18 command; determines the state (one set of zero set) of each one of the terms involved in the specific logic equation (TM 9-1220-221-34/1/1).

k. In this case all terms are one set except the E term which is zero set. Gate 01 (MP- /KB/) is false because MP is one set not zero set. Gate 02 (E XC CL4) is true because all of its terms are true. Gate 03 (E XC 1X-) is false because term IX is one set and term E is zero set. Gate 04 (XC- CL4-) is false because terms XC and CL4 are both one set.

4-44. MALFUNCTION ISOLATION--Continued

1. Referring to the mechanized equation in figure 4-37, monitor the output voltage of each one of the output gates.

   (1) In this case the voltages should be:

   334B50, gate 01--approx 0 volts (F)
   334B60, gate 02--approx -6 volts (T)
   334B60, gate 03--approx 0 volts (F)
   334B56, gate 04--approx 0 volts (F)

   (2) Gate 01 should be false; the tertiary term /KB-/, which should also be false is "anded" with gates 02 thru 04. XP is one set. Therefore, XP should remain one set because the logic to zero set XO should not be true. However, XP is being zero set. Therefore, the most likely gates to be at fault are gate 01 and the tertiary gate.

m. Normal electronic signal tracing techniques may now be utilized to troubleshoot and correct the logical error.

4-45. EXPLANATION OF DU/DL ADDRESS TABLES

The operator using the tape printouts can acknowledge the commands of flip-flops and desires the DU/DL address (address code is needed either for testing using a voltmeter or for addressing using the control box C-4020 or for both). Table 4-12 contains the flip-flop primary functions; table 4-13 contains the flip-flop address and location; table 4-14 contains the write flip-flop address and location; table 4-15 contains the read flip-flop address and location; table 4-16 contains the flip-flop address and response lines; table 4-17 contains the read flip-flop address and response lines; table 4-18 contains the address for the addressable primary "and" gates, logic drivers, and write switches.

Table 4-12. Flip-Flop Primary Function

Logic name	Purpose	Logic name	Purpose
AC	A loop control.	CFS	Channel field switch.
AK	Carry for addition; mode control.	CFSW	Channel field switch for writing.
AP	A loop extension, Tp phasing.	CLC	Computer light control.
AX	A loop extension, TX phasing.	CL2 CL3	Channel no. buffer (next instruction address).
B1	Bit counter.	CL4	
B2		CL5	
B3		CL6	
B4		CL7	
B5			
B6			

Table 4-12. Flip-Flop Primary Function--Continued

Logic name	Purpose
CN2 CN3 CN4 CN5 CN6 CN7	Number channel selection register for reading.
CP2	Program channel selection register.
CP3 CP4 CP5 CP6 CP7	
CPFS	Channel program field switch.
CP76	Special program channel control.
CR2 CR3 CR4 CR5 CR6 CR7	Channel no. buffer (operand address).
C2 C3 C4 C5 C6 C7	Number channel selection register for writing.
DC	D loop control.
DSH	Display shift timing.
DSP	Display control.
DX	D loop extension. TX phasing.
D1 D2 D3 D4 D5 D6 D7 D8	Display register; input-output register.
DA1 DA2 DA3 DA4 DA5 DA6 DA7 DA8	Display register.
D	Mode control (down mode).
E	Mode control (execute).
FS	Field switch.
G	Psuedo mode control.
IC	I loop control.
ID	Instruction disagreement.
IP	I loop extension, Tp phasing.
K	Mode control (compute).
LC	L loop control.
LP	L loop extension, Tp phasing.
LX	L loop extension, TX phasing.
MC	Main memory read control.
MMN	Number read.
MMP	Program read.

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-12. Flip-Flop Primary Function--Continued

Logic name	Purpose
MN	Main memory number collector.
MP	Main memory instruction collector.
MWI MWØ	Main memory write.
NC	N loop control.
ND	Number disagreement.
NX	N loop extension, TX phasing.
OB2 OB3 OB4 OB5 OB6	Operation code buffer.
OFLO	Overflow indicator.
OP1 OP2 OP3	Discrete output register.
02 03 04 05 06	Operation code register.
PE	Parity error indicator.
PN	Parity generation and detection for numbers.
PP	Parity generation and detection for instructions.
QC	Q loop control.
QX	Q loop extension, TX phasing.
RC	R loop control.
RX	R loop extension, TX phasing.
S	Selector track read.
TO	Timing
TP	Timing
TSO	Timing
TX	Timing
XC	X loop control.
XD	Display delay.
XR	X loop recirculation control.
X1 X2	Display anode counter.
A32 DP I32 L32 NP QP RP XP	Loop write flip-flops.
AO DO IX LO NO RO RM QO QM XO	Loop read flip-flops.

Table 4-13. Flip-Flop Address and Location

Flip-flop	Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU		DL	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
AC	239	40B	46B	33B	36B	05	D	20	N
AK	224	20B	17B	28B	27B	06	E	22	R
AP	320	20B	17B	28B	27B	15	L	27	W
AX	315	40B	46B	33B	36B	14	K	30	X
B1	232	40B	46B	33B	36B	05	D	21	V
B2	340	20B	17B	28B	27B	04	C	25	U
B3	208	20B	17B	28B	27B	11	G	24	T
B4	440	20B	17B	28B	27B	04	C	31	Y
B5	441	20B	17B	28B	27B	02	A	31	Y
B6	226	40B	46B	33B	36B	05	D	22	R
CL2	233	20B	17B	28B	27B	02	A	21	P
CL3	314	20B	17B	28B	27B	15	L	30	X
CL4	339	40B	46B	33B	36B	07	F	25	U
CL5	330	20B	17B	28B	27B	15	L	26	V
CL6	317	40B	46B	33B	36B	07	F	30	X
CL7	218	40B	46B	33B	36B	16	M	22	R
CN2	333	20B	17B	28B	27B	06	E	26	Y
CN3	332	40B	46B	33B	36B	12	H	26	P
CN4	237	20B	17B	28B	27B	11	G	20	N
CN5	238	40B	46B	33B	36B	07	F	20	N

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-13. Flip-Flop Address and Location--Continued

Flip-flop	Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU		DL	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
CN6	240	40B	46B	33B	36B	03	B	20	N
CN7	335	20B	17B	28B	27B	02	A	26	V
CP2	234	40B	46B	33B	36B	16	M	20	N
CP3	319	20B	17B	28B	27B	02	A	30	X
CP4	321	20B	17B	28B	27B	13	J	27	W
CP5	213	20B	17B	28B	27B	13	J	23	S
CP6	234	20B	17B	28B	27B	15	L	20	N
CP7	337	20B	17B	28B	27B	13	J	25	U
CP76	319	40B	46B	33B	36B	03	B	30	X
CR2	328	40B	46B	33B	36B	05	D	27	W
CR3	206	40B	46B	33B	36B	16	M	24	T
CR4	217	40B	46B	33B	36B	03	B	23	S
CR5	233	40B	46B	33B	36B	03	B	21	P
CR6	227	40B	46B	33B	36B	03	B	22	R
CR7	231	40B	46B	33B	36B	07	F	21	V
C2	336	40B	46B	33B	36B	16	M	25	U
C3	227	20B	17B	28B	27B	02	A	22	R
C4	229	20B	17B	28B	27B	13	J	21	P
C5	228	40B	46B	33B	36B	16	M	21	P
C6	330	40B	46B	33B	36B	16	M	26	V

Table 4-13. Flip-Flop Address and Location--Continued

Flip-flop	Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU		DL	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
C7	207	40B	46B	33B	36B	14	K	24	T
CFS	238	20B	17B	28B	27B	06	E	20	U
CFSW	338	20B	17B	28B	27B	11	G	25	U
CLC	338	40B	46B	33B	36B	12	H	25	U
CPFS	237	40B	46B	33B	36B	12	H	20	U
DC	212	20B	17B	28B	27B	15	L	23	S
DX	216	40B	46B	33B	36B	05	D	23	S
DSH	215	40B	46B	33B	36B	07	F	23	S
DSP	213	40B	46B	33B	36B	14	K	23	S
DA1	440	40B	46B	33B	36B	05	D	31	Y
DA2	340	40B	46B	33B	36B	05	D	25	U
DA3	211	40B	46B	33B	36B	03	B	24	T
DA4	230	40B	46B	33B	36B	12	H	21	P
DA5	230	20B	17B	28B	27B	11	G	21	P
DA6	321	40B	46B	33B	36B	14	K	27	R
DA7	326	40B	46B	33B	36B	12	H	27	R
DA8	336	20B	17B	28B	27B	15	L	25	U
D1	316	20B	17B	28B	27B	11	G	30	X
D2	314	40B	46B	33B	36B	16	M	30	X

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-13. Flip-Flop Address and Location--Continued

Flip-flop	Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU		DL	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
D3	320	40B	46B	33B	36B	16	M	27	W
D4	223	20B	17B	28B	27B	11	G	22	R
D5	224	40B	46B	33B	36B	07	F	22	R
D6	235	40B	46B	33B	36B	14	K	20	N
D7	240	20B	17B	28B	27B	02	A	20	N
D8	212	40B	46B	33B	36B	16	M	23	S
D	231	20B	17B	28B	27B	06	E	21	P
E	315	20B	17B	28B	27B	13	J	30	X
FS	441	40B	46B	33B	36B	03	B	31	Y
G	211	20B	17B	28B	27B	02	A	24	T
IC	208	40B	46B	33B	36B	12	H	24	T
ID	229	40B	46B	33B	36B	14	K	21	P
IP	317	20B	17B	28B	27B	06	E	30	X
K	215	20B	17B	28B	27B	06	E	23	S
LC	218	20B	17B	28B	27B	15	L	22	R
LP	239	20B	17B	28B	27B	04	C	20	N
LX	217	20B	17B	28B	27B	02	A	23	S
MC	216	20B	17B	28B	27B	04	C	23	S
MN	210	20B	17B	28B	27B	04	C	24	T

Table 4-13. Flip-Flop Address and Location--Continued

Flip-flop	Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU		DL	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
MP	341	20B	17B	28B	27B	02	A	25	U
NC	327	40B	46B	33B	36B	07	F	27	W
ND	328	20B	17B	28B	27B	04	C	27	W
NX	327	20B	17B	28B	27B	06	E	27	W
OB2	209	40B	46B	33B	36B	07	F	24	T
OB3	214	20B	17B	28B	27B	11	G	23	S
OB4	232	20B	17B	28B	27B	04	C	21	P
OB5	226	20B	17B	28B	27B	04	C	22	W
OB6	228	20B	17B	28B	27B	15	L	21	W
OFLO	341	40B	46B	33B	36B	03	B	25	U
OP1	318	40B	46B	33B	36B	05	D	30	X
OP2	223	40B	46B	33B	36B	12	H	22	R
OP3	334	40B	46B	33B	36B	05	D	26	V
02	222	40B	46B	33B	36B	14	K	22	R
03	318	20B	17B	28B	27B	04	C	30	X
04	335	40B	46B	33B	36B	03	B	26	V
05	331	20B	17B	28B	27B	13	J	26	V
06	222	20B	17B	28B	27B	13	J	22	R
PE	209	20B	17B	28B	27B	06	E	24	T

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-13. Flip-Flop Address and Location--Continued

Flip-flop	Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU		DL	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
PN	329	20B	17B	28B	27B	02	A	27	W
PP	235	20B	17B	28B	27B	13	J	20	N
QC	331	40B	46B	33B	36B	14	K	26	V
QX	334	20B	17B	28B	27B	04	C	26	V
RC	326	20B	17B	28B	27B	11	G	27	W
RX	329	40B	46B	33B	36B	03	B	27	W
TO	339	20B	17B	28B	27B	06	E	25	U
TP	210	40B	46B	33B	36B	05	D	24	T
TSO	332	20B	47B	28B	27B	11	G	26	V
TX	207	20B	17B	28B	27B	13	J	24	T
X1	214	40B	46B	33B	36B	12	H	23	S
X2	337	40B	46B	33B	36B	14	K	25	U
XC	316	40B	46B	33B	36B	12	H	30	X
XD	333	40B	46B	33B	36B	07	F	26	V
XR	206	20B	17B	28B	27B	15	L	24	T

Table 4-14. Flip-Flop Address and Location (Write Flip-Flops)

Logic (symbol) write	Board location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DU line no.	DL line no.
L32	435	46B	56B	37B	64B	03	32
DP	435	10B	19B	8A	23A	02	32
NP	436	46B	56B	37B	64B	16	31
XP	436	10B	19B	8A	23A	15	31
RP	437	46B	56B	37B	64B	13	31
I32	438	46B	56B	37B	64B	12	31
A32	438	10B	19B	8A	23A	11	31
QP	439	46B	56B	37B	64B	07	31
MWØ	439	10B	19B	3B	23A	06	31
MW1	437	10B	19B	3B	23A	14	31

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-15. Flip-Flop Address and Location (Read Flip-Flops)

Logic symbol read	Board Location	One set input (pin)	Zero set input (pin)	Output true if one set (pin)	Output true if zero set (pin)	DUR		DLR	
						Line no.	M18 J12 pin	Line no.	M18 J12 pin
S	303	3A	19B	6B	5A	02	/A	33	/E
XO	304	3A	19B	6B	5A	02	/A	34	/F
DO	305	3A	19B	6B	5A	02	/A	35	/G
RO	306	3A	19B	6B	5A	02	/A	36	/H
RM	307	3A	19B	6B	5A	03	/B	33	/E
QO	308	3A	19B	6B	5A	03	/B	34	/F
QM	309	3A	19B	6B	5A	03	/B	35	/G
NO	310	3A	19B	6B	5A	03	/B	36	/H
LO	311	3A	19B	6B	5A	04	/C	33	/E
IX	312	3A	19B	6B	5A	04	/C	34	/F
AO	313	3A	19B	6B	5A	04	/C	35	/G
MMN	302	2A	11B	12B	7A	04	/C	36	/H
MMP	301	2A	11B	12B	7A	05	/D	33	/E
TD/WI	101	12A	14A	17B	31B	05	/D	34	/F
(PS/ PS-)				(TD) (PS)	(WI) (PS-)				

Table 4-16. Flip-Flop Address and Response Lines.

	DU02	DU03	DU04	DU05	DU06	DU07	DU11	DU12	DU13	DU14	DU15	DU16	
FIT 1 &	D7	CN6	LP	AC	CFS	CN5	CN4	CPFS	PP	D6	CP6	CP2	
	240	240	239	238	238	237	237	237	235	235	234	234	DL20
FOT 1	CL2	CR5	OB4	B1	D	CR7	DA5	DA4	C4	ID	OB6	C5	
	233	233	232	231	231	231	230	230	229	229	228	228	DL21
FIT 2 &	C3	CR6	OB5	B6	AK	D5	D4	OP2	O6	O2	LC	CL7	
	227	227	226	226	224	224	223	223	222	222	218	218	DL22
FOT 2	LX	CR4	MC	DX	K	DSH	OB3	X1	CP5	DSP	DC	D8	
	217	217	216	216	215	215	214	214	213	213	212	212	DL23
FIT 3 &													
FOT 3	G	DA3	MN	TP	PE	OB2	B3	IC	TX	C7	XR	CR3	
	211	211	210	210	209	209	208	208	207	207	206	206	DL24
FIT 4 &	MP	OFLO	B2	DA2	TO	CL4	CFSW	CLC	CP7	X2	DA8	C2	
	341	341	340	340	339	339	338	338	337	337	336	336	DL25
FOT 4	CN7	O4	QX	OP3	CN2	XD	TSO	CN3	O5	QC	CL5	C6	
	335	335	334	334	333	333	332	332	331	331	330	330	DL26
FIT 5 &	PN	RX	ND	CR2	NX	NC	RC	DA7	CP4	DA6	SP	D3	
	329	329	328	328	327	327	326	326	321	321	320	320	DL27
FOT 5	CP3	CP76	O3	OP1	IP	CL6	D1	XC	E	AX	CL3	D2	
	319	319	318	318	317	317	316	316	315	315	314	314	DL30
FIT 6 &													
FOT 6	B5	FS	B4	DA1	MWØ	QP	A32	I32	RP	MW1	XP	NP	
	441	441	440	440	439	439	438	438	437	437	436	436	DL31
FIT 7 &													
FOT 7	DP	L32											
	435	435											DL32

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-17. Read Flip-Flop Address and Response Lines

	DUR02	DUR03	DUR04	DUR05	
F1T 7 & FOT 7	S 303	RM 307	LO 311	MMP 301	DLR33
	XO 304	QO 308	IX 312	TDWI PS 101	DLR34
	DO 305	QM 309	AO 313		DLR35
F1T 6 & FOT 6	RO 306	NO 310	MMN 302		DLR36
			F1T 7 & FOT 7	F1T 1 & FOT 1	

Table 4-18. Addressable Primary Gates, Logic Drivers and Write Switches

DU 02	03	04	05	06	07	DL
(CTB1)	(CTB2)	(CTB3)	(CTD4)	(CTB5)	(CTB6)	20
(SS5B)	(SS6B)	(SS7B)	(SS8B)	(SS9B)	(SS10B)	21
(BDX)	(BL1)	(BL2)	(BL3)	(BL5)	(BL6)	22
(CR65)	(CL34)	(D21-)	(D43)	(D43-)	(D51)	23
(KAK1)	(KB5)	(KD3M)	(KED3)	(DEO)	(DHRS)	24
(KFST)	(KW)	(MAXO)	(MAX1)	(MAX2)	(MAX3)	25
(ODO)	(OEL)	(OF)	(OGC)	(OJ)	(OLP)	26
(OMNF)	(OOP)	(OSA)	(OSHB)	(OTR)	(ORT4)	27
(O4X)	(OTL)	(QT1)	(TXP-)		(TO1C)	30
/C432/	/C433/	/C5A/	/C760/	/C761/	/CFSU/	31
/KED2/	/KD1/	/KIOA/	/KOPC/	/KTP/	/MNA/	32
/OX/	/SA/	/TOA/	/TOA-/	/TOB/	/TOX-/	33
/TLS/	/T32/	/02A/	/C4A-/	/TXC/	/TRC/	34

Table 4-18. Addressable Primary Gates, Logic Drivers and Write Switches--Continued

DU 11	12	13	14	15	16	DL
(CTB7)	(CTB8)	(SS1B)	(SS2B)	(SS3B)	(SS4B)	20
(SS11B)	(SS12B)	(SS13B)	(SS14B)	(SS15B)	(SS16B)	21
(BL7)	(B5L4)	(CNU6)	(CPS4)	(CPS5)	(CR75)	22
(DOP)	(DSPH)	(EAKO)	(ERR-)	(FST)	(ICP)	23
(KIOC)	(KIOP)	(KIOX)	(KLC-)	(KSUO)	(KSUI)	24
(MMPT)	(NDX-)	(OA)	(OBN)	(OBW)	(OCL)	25
(OLPT)	(OLO)	(OL4)	(OMDL)	(OMDM)	(OMF)	26
(OW)	(OWT)	(OYAC)	(OYB)	(OYC5)	(OYR)	27
(T15)	(T19)	(VER)	(XCT)	/C430/	/C431/	30
	/DA-/	/IPA/	/IPA-/	/IXA/	/KA-/	31
/MNA-/	/OCT/	/OM/	/OMD/			32
/TPA/	/TSH/	/TXA-/				33
/TRS/	MNF	MPF				34

4-45. EXPLANATION OF DU/DL ADDRESS TABLES--Continued

Table 4-19. Wire Color Versus Function Chart

Wire Color	Function
Black	Power Ground, Shield Ground, Chassis Ground, Read Ground
Red	+15 volts
Orange	+1.25 volts
Yellow	1 and Ø clock pulses
Green	+150 volts, one and zero input logic, tertiary outputs
Blue	+6 volts
Violet	+35 volts
Grey	+73-volt Zener
White-Black	+20 volts
White-Brown	-10 volts
White-Red	-12-volt Zener
White-Orange	-3 volts
White-Yellow	Strobe pulse
White-Green	-1.5 volts
White-Blue	-6 volts
White-Violet	-27 volts
White-Grey	-18-volt test, -18 volts
White	+138-volt Zener, +66- volt Zener, logic

4-46. GENERAL INFORMATION FOR MALFUNCTION ISOLATION

a. Printed Circuit Board Connector.

(1) Each printed circuit board in the computer connects circuitry through a printed circuit board connector. Voltage levels and various input/output signals which are used with a particular printed circuit board, are tied to the board connector on the wiring side. When the computer is open, the wiring side of all board connectors is exposed. The board connector is divided into the A side and the B side. There are 65 pins on each of these sides for a total of 130 pins. In troubleshooting the computer, it is sometimes necessary to test or measure various signals tied to the pins on the board connector. The pins are identified by using a combination of letters and numbers. For example, A15 would be the 15th pin on the A side of the connector. Pins can be located by the color code insulating sleeving used on every five pins of the connector. Illustrated in figure 4-38 is a circuit board connector showing the various colors used to identify the pins. Those pins where color is not called out have white insulating sleeving. To locate pin A28 it is easiest to first locate the orange pin A30 and then count two pins to the right or left depending on the position of the computer. The A and B side of the connector is easily identified by noting the position of the printed circuit boards. The components on the printed circuit board are mounted on the A side and the etched wiring is on the B side. Pins 1 and 2 of the A side are both brown while only pin 1 of the B side is brown.

(2) Due to the keying arrangements for each type of printed circuit board, several pins on each connector have been removed. When locating on a connector, allowance must be made for the missing pins.

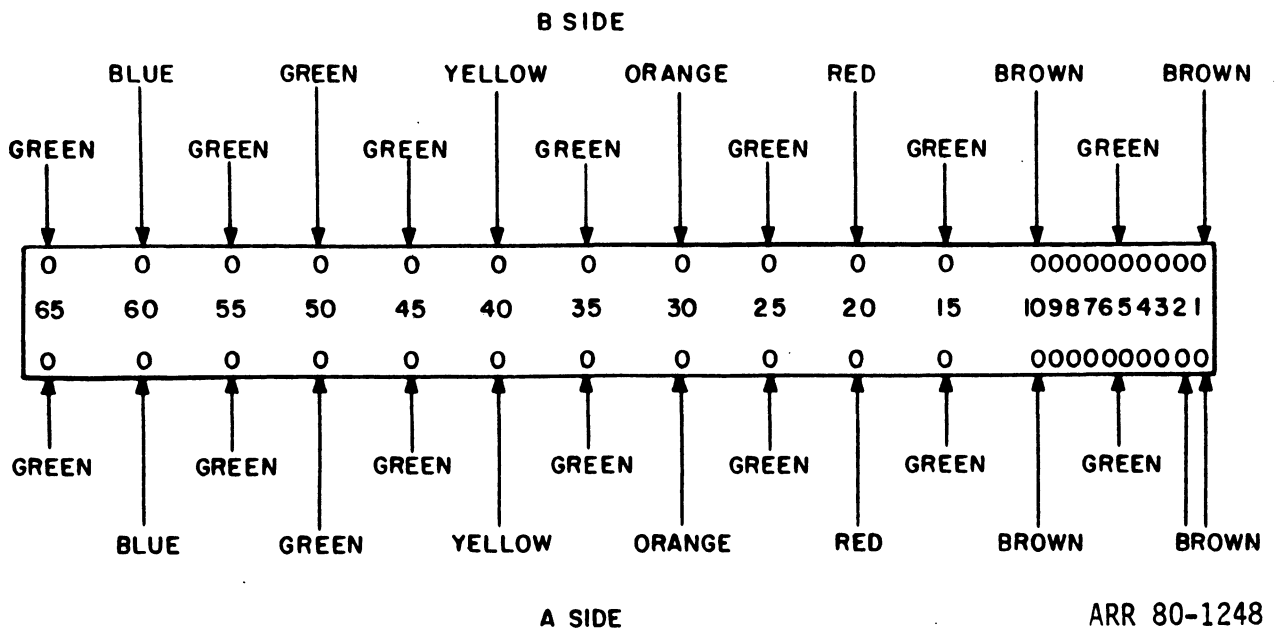


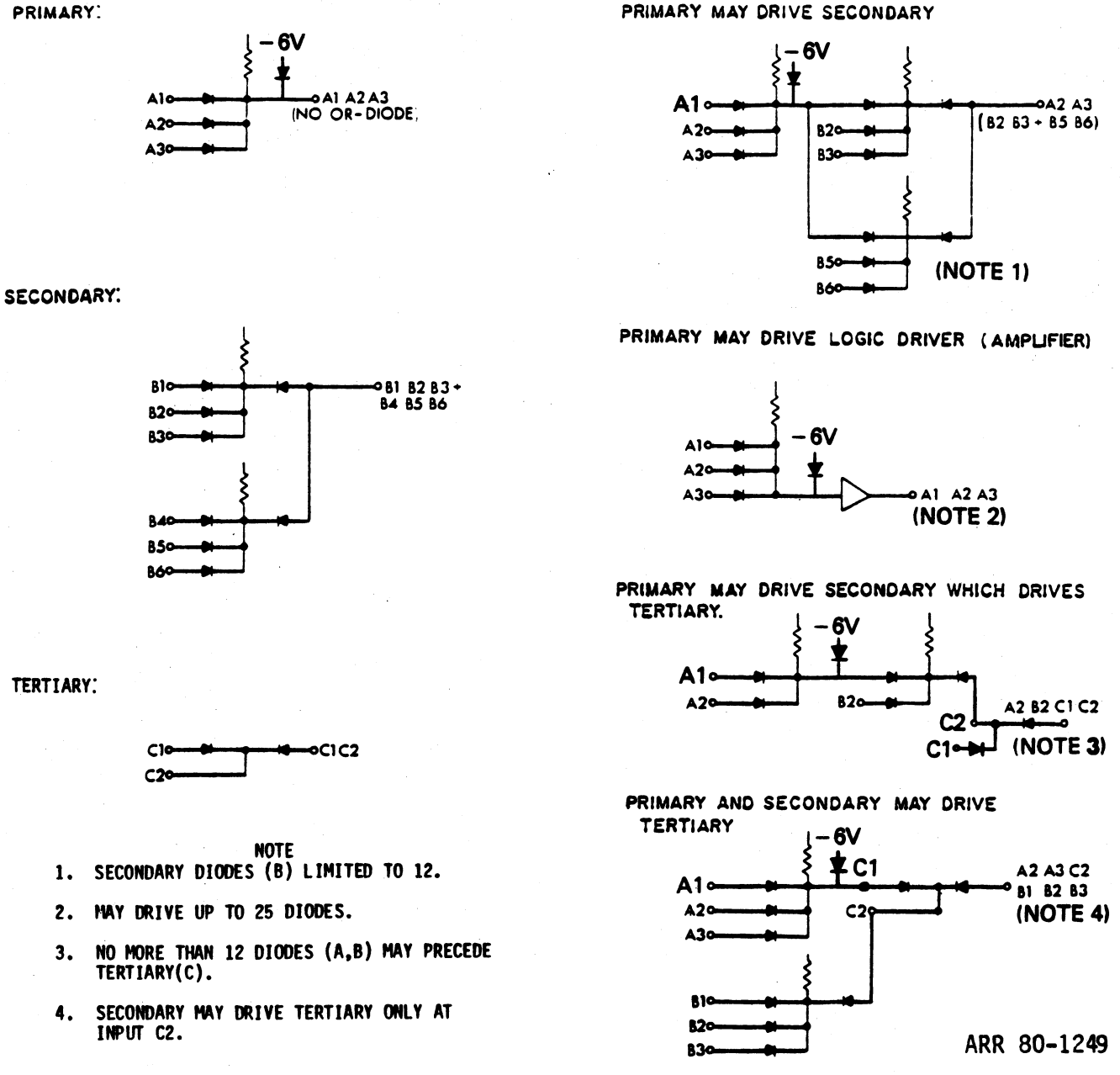
Figure 4-38. Printed Circuit Board Connector.

4-46. GENERAL INFORMATION FOR MALFUNCTION ISOLATION--Continued

b. Wiring Color Codes. Some wires used to carry various voltage levels and signals throughout the computer are also color-coded according to their functions. Many wires are coded using two colors such as white-black. When two colors are used, the first color indicated the tracer. The computer wire color-coding scheme is outlined in table 4-19.

4-47. DIODE GATES

There are three types of diode gates contained in the FADAC. They are the primary, secondary, and tertiary gates. An example of the three types of gates and brief explanation and illustration follows.



NOTE

1. SECONDARY DIODES (B) LIMITED TO 12.
2. MAY DRIVE UP TO 25 DIODES.
3. NO MORE THAN 12 DIODES (A,B) MAY PRECEDE TERTIARY(C).
4. SECONDARY MAY DRIVE TERTIARY ONLY AT INPUT C2.

Figure 4-39. Three Types of Diode Gates.

Table 4-20. Flip-Flop Logic Pin To Gate Chart

A SIDE	PIN NRS	B SIDE
15	1	15
15	2	15
15	3	18
16	4	18
18	5	18
16	6	18
16	7	16
16	8	16
17	9	16
17	10	17
17	11	17
9	12	+6V
9	13	DC
9	14	2
8	15	9
8	16	2
8	17	IN F1-
8	18	25
24	19	27
24	20	IN F1
24	21	DUY
27	22	-6V
27	23	27

A SIDE	PIN NRS	B SIDE
26	24	-18V
26	25	25
26	26	FOT
26	27	OUT F1-
10	28	OUT F1
10	29	25
10	30	10
7	31	GND
7	32	FIT
7	33	OUT F2
13	34	DL
13	35	7
13	36	OUT F2-
13	37	DUZ
13	38	I-C
-18V	39	+1.25
14	40	in F2
	41	
14	42	12

A SIDE	PIN NRS	B SIDE
12	43	12
12	44	12
14	45	14
14	46	IN F2-
21	47	20
23	48	21
23	49	23
20	50	4
22	51	4
22	52	4
1	53	1
20	54	22
21	55	23
3	56	3
5	57	3
5	58	5
6	59	6
6	60	19
19	61	19
19	62	19
19	63	19
11	64	11
11	65	11

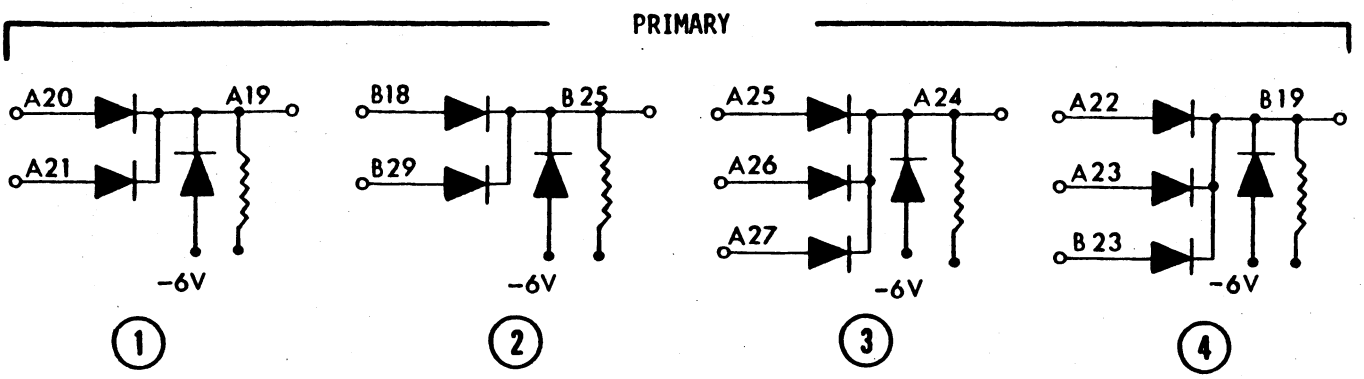


Figure 4-40. Primary Diode Gates.

4-47. DIODE GATES--Continued

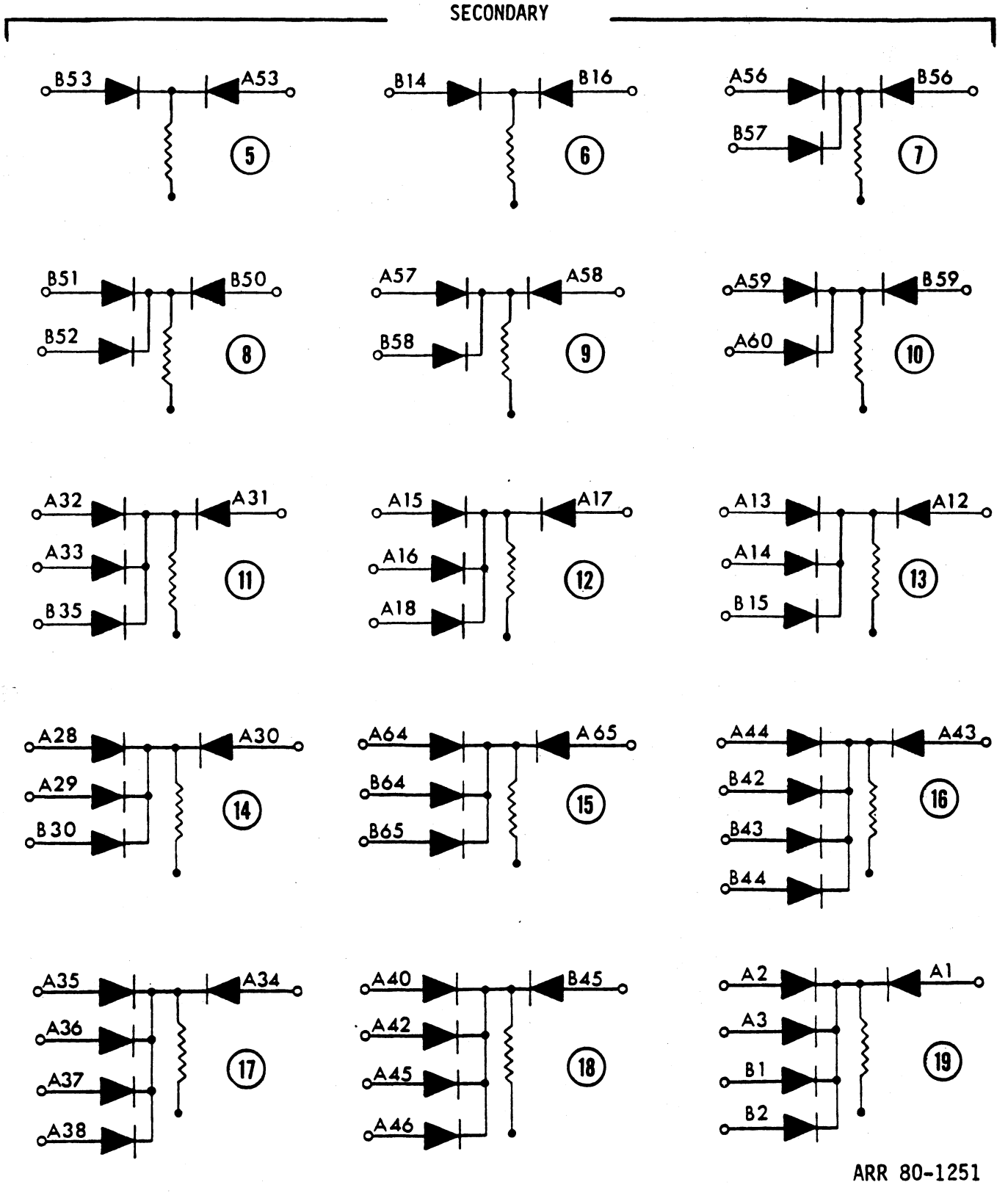


Figure 4-41. Secondary Diode Gates (sheet 1 of 2).

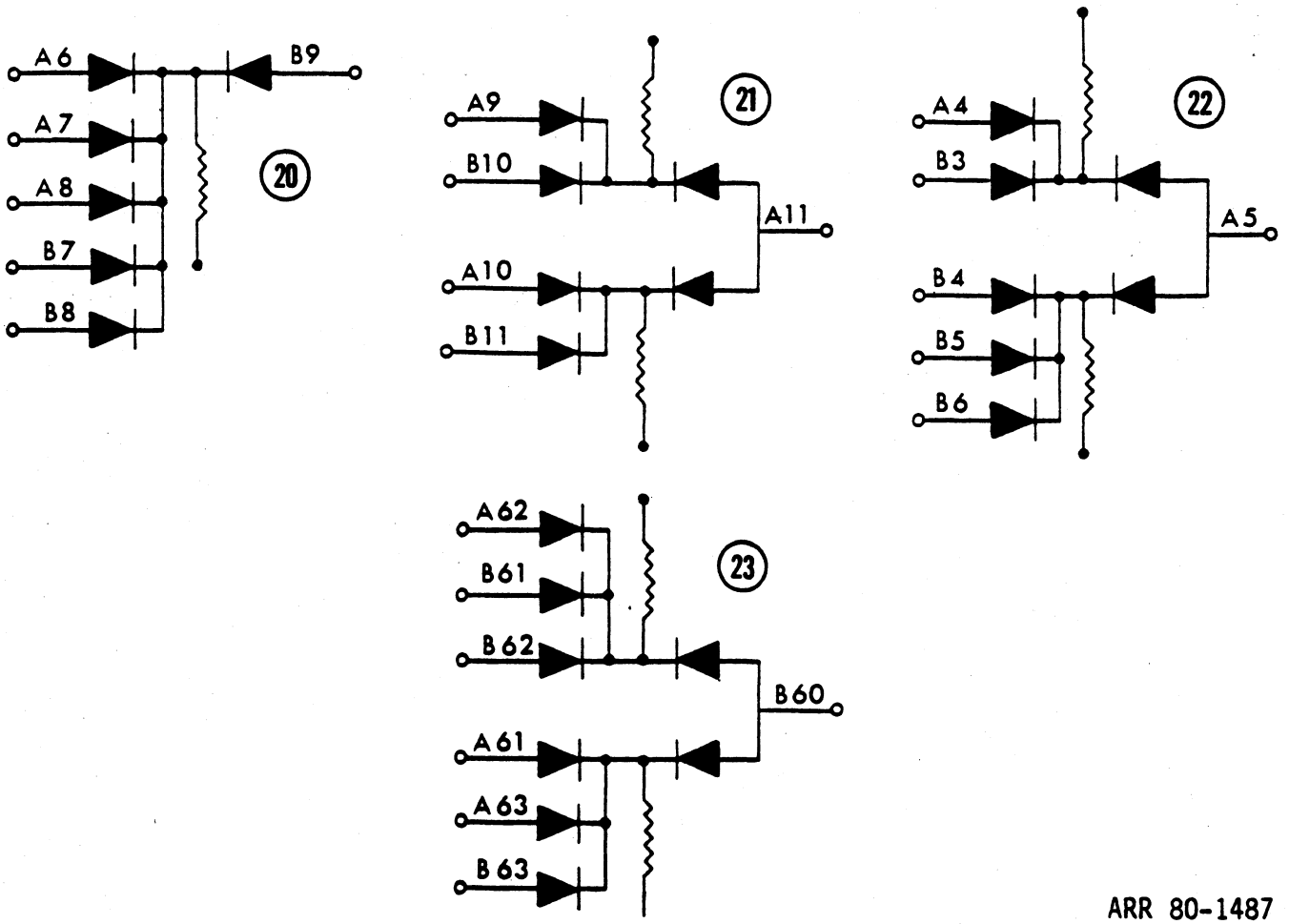


Figure 4-41. Secondary Diode Gates (sheet 2 of 2).

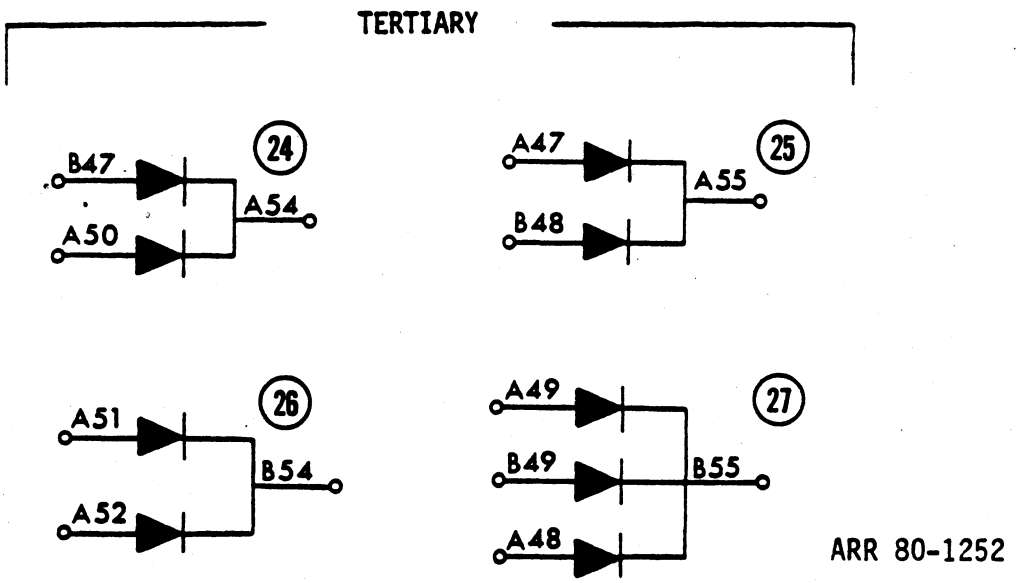


Figure 4-42. Tertiary Diode Gates.

4-48. F1T and F0T LINE TROUBLESHOOTING

a. General. The FALT one and zero tests the computer flip-flop circuits through the F1T AND F0T lines. The "or" diodes are used to the one F1T and F0T lines. If this "or" diode is open, an error will result when the flip-flop circuits on that particular F1T or F0T line.

b. Line Troubleshooting.

(1) The flip-flop circuits located on boards 230 thru 240 are tied together to form F1T1 and F0T1. Assume that diode CR43 on logic flip-flop board 230 is shorted. This diode ties the one-set output of DA5 flip-flop to the F1T1 line. When the B test tape is run, the first error will occur at marker 001, index 003, "or" D7 one test. Replacing the boards called put for marker 001 will not solve the problem. A voltmeter can be used to measure the one-set output of D7 on pin B28 of board 240. Voltage measurement will show that D7 is one set. However, due to the shorted diode on board 230, 0 volts appears on the F1T-line resulting in an error on the FALT. The remaining flip-flop circuits on F1T1, except DA5, would all indicate an error when they are one tested, even though they are one set. The zero testing of these same flip-flops will not be affected by the shorted diode in the F1T1 circuit. The solution to the error would be to replace and circuit board involved in F1T1-line, one at a time, until the board with the shorted diode has been found. Each time a new board has been replaced, D7 should be one tested until the test passes. The computer wire list (TM 9-1220-221-34/6) contains lists of all boards involved in F1T1. The wire list calls out boards 101 and 230 thru 240 except 236 as being involved with F1T1.

(2) Board replacement should solve the majority of F1T and F0T line problems. However, other problem areas will also arise. Computer wiring, cold solder connections, and defective test cables could also be the source of F1T and F0T line problems. When board replacement fails then these other areas must be investigated.

4-49. LOGIC DRIVER TROUBLESHOOTING

a. General. The computer logic driver circuit may be divided into three parts: the input gate, the driver circuit, and the output load. When the logic drivers are tested in the B test tape, the circuit boards containing the input gate and driver circuit are called out in the program printout. To determine the circuit boards which comprise the output load, the maintenance technician should refer to the computer wire list (TM 9-1220-221-34/6). The majority of logic driver failures can be corrected by replacement of the circuit boards called out in the program printout. When replacement of these circuit boards does not solve the problem, the defective area can be easily isolated using a voltmeter.

b. Input Gate Tests. The input circuit for all logic drivers except /TOS/ is an "and" gate. Logic drivers which are fed by a single term also have an "and" gate as their input circuit. When a logic driver is one tested, all terms in the input gate are true. The logic driver circuit

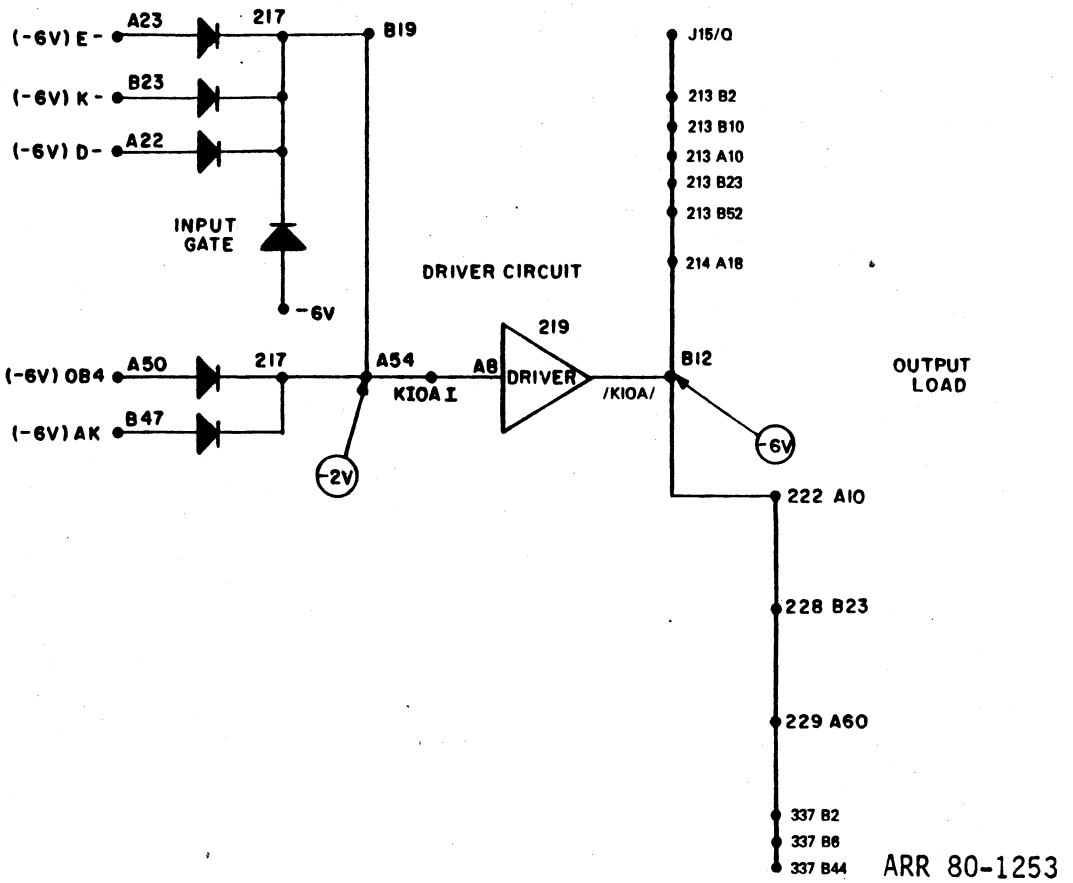


Figure 4-43. Mechanization of /KIOA/.

can be mechanized and these input terms can be measured using a voltmeter. Illustrated in figure 4-43 is logic driver /KIOA/. Since five terms make up the input for /KIOA/, two circuits are used to form the input "and" gate. Three input terms and the -6-volt clamp are tied to the remaining two input terms forming a five-input "and" gate. When the input terms are measured using the voltmeter, the common lead of the meter should be connected to a suitable ground point. A negative voltage of about 6 volts should appear on each pin of the input gate when the logic driver is one tested. If all inputs are normal, the output from the gate can then be measured. When all inputs are true the normal output level of the driver input gate is -2 volts. This low output voltage is due to the loading effect of the logic driver circuit on the input gate. Negation tests are also performed on the logic driver input circuit. One term of the input gate will be false and the driver will be zero tested. A failure in this area usually indicates an open diode and board replacement will correct the majority of failures. When board replacement fails to correct the error, the driver circuit, which is illustrated in TM 9-1220-221-34/1/1, can be retested using the voltmeter. The first step in the solution of a negation error is to determine the diode under test. At the end of each negation test in the program printout, the term which has been negated is called out. In the first negation test of driver /KIOA/, which is mechanized in figure 4-43, term K- is false and the driver should also be false. When the input pin is measured, pin B23 of board 217 should be at 0 volts. If B23 is 0 volts and the output of the gate circuit is

4-49. LOGIC DRIVER TROUBLESHOOTING--Continued

true (-2 volts in this case) then an open circuit exists in one negated term. Board replacement eliminated the possibility of an open diode. Therefore, wiring continuity from the gate input back to the source of the negated term must be tested. A high resistance cold solder connection on B23 of board 217 would be a possibility. A poor or dirty contact between the circuit board and the board connector on pin B23 is still another possibility which must be checked. When the negated term is false and the gate output is also false then the input circuit is functional and a problem would exist elsewhere in the circuitry.

c. Driver Tests. With a true signal on the input of the logic driver, the output should also be true. If the input to the driver is false, then the output should also be false. The signal level measured at the gate output should be the same as that measured at the driver input. When these signals differ, wiring continuity from the driver input back to the gate output must be checked. The output of the driver circuit should be at -6 volts when measured with the voltmeter. When the driver output is false (0 volts) while the input is true then the driver circuit is defective and the circuit board should be replaced with a functional one. A low resistance short in the output load is a possible problem area when the driver circuit output is low. If board replacement does not solve the problem of a defective output, then the output load must be checked.

d. Output Load Tests. The output level of a driver circuit can be determined by referring to the computer wire list. The output load of driver /KIOA/ is illustrated in figure 4-43. The output load will vary with each driver ciruit. Some drivers are tied to as many as 25 logic circuits. Determining the defective circuit board in the output load is simply a matter of removal or replacement. Whenever a circuit board is to be removed or replaced the computer must be turned off. When many boards are involved in the output several may be removed at one time; each time a group of boards is removed the driver can be tested again using the control box C-4020. Circuit boards that are involved in both the output load and the input circuit must not be removed. However, these boards can be replaced with boards from stock. Other possible problem areas in the output load are the computer wiring and the FALT cables. Resistance measurements can be made to test these other areas.

4-50. PRIMARY "AND" GATE TROUBLESHOOTING

a. General. Many of the failures incurred while testing the primary "and" gates in the B test tape will be corrected by replacing the circuit boards contained in the program printout. When board replacement fails to solve the error, the defective area can be isolated by voltage measurement.

b. "And" Gate Troubleshooting.

(1) If the error occurs during a one test, the gate illustrated in TM 9-1220-221-34/1/1 can be viewed and the voltmeter used to measure the inputs. In the one test, all inputs should be true with a signal level of about -6 volts. A false signal on any of the input pins will localize the problem to that input term. When all input terms are true and the output is false, then the problem could exist in the output load.

(2) The majority of primary "and" gate input terms are outputs of flip-flop and logic driver circuits. When a circuit is part of the "and" gate logic, it is usually the first test of this driver circuit. If a primary "and" gate error has been isolated to a logic driver, the logic driver input circuit and the remaining output load must be considered as the possible source of the failure. A malfunction in another portion of the logic driver output load will be reflected in the primary "and" gate. A defective logic driver circuit will also affect the "and" gate when it is tested.

4-51. TROUBLESHOOTING FLIP-FLOP LOGIC

a. "Or" Test Failures. During "or" testing of flip-flop logic, each logic equation "or" gate is usually tested separately. When an error occurs, note the marker and index numbers which are displayed on the FALT and locate the test in the program printouts. A number indicating the equation being tested is printed following the address of the flip-flop under test. When circuit board replacement fails to correct the error, the voltmeter is used to isolate the defective term. The normal input to each diode of the gate under test will be a negative voltage of about -6 volts. A voltmeter reading of 0 volts on any input will localize the problem to that input term.

NOTE

Logical mechanization of terms is detailed in TM 9-1220-221-34/1/1.

b. "And" Test Failures. For "and" tests of flip-flop logic, one or more terms may be negated during a test. The test tape program printout will indicate the terms of an equation that have been negated for any given test. Using the mechanized logic diagram the negated terms can be checked with a voltmeter. A negated term should read about 0 volts on the voltmeter. When a negated term is true, the problem is with this input term. If board replacement does not solve the problem, the wiring should be checked for an open circuit and the board connector pins should be checked for proper contact.

Section V. Input-Output

4-52. GENERAL

a. This section covers troubleshooting pertinent to input and output circuitry.

b. Inputs to the computer can be any one of the following: the SDR, keyboard unit, mechanical reader unit, matrix unit, or external devices, e.g. another computer, auxiliary memory storage devices.

c. The primary output is to the nixie readout panel. When properly programmed, the computer will output to external devices such as the teletypewriter, another computer, or other equipment.

d. The schematics in figures 4-44 and 4-45 depict the scheme and sequence of coverage to be disclosed in this section.

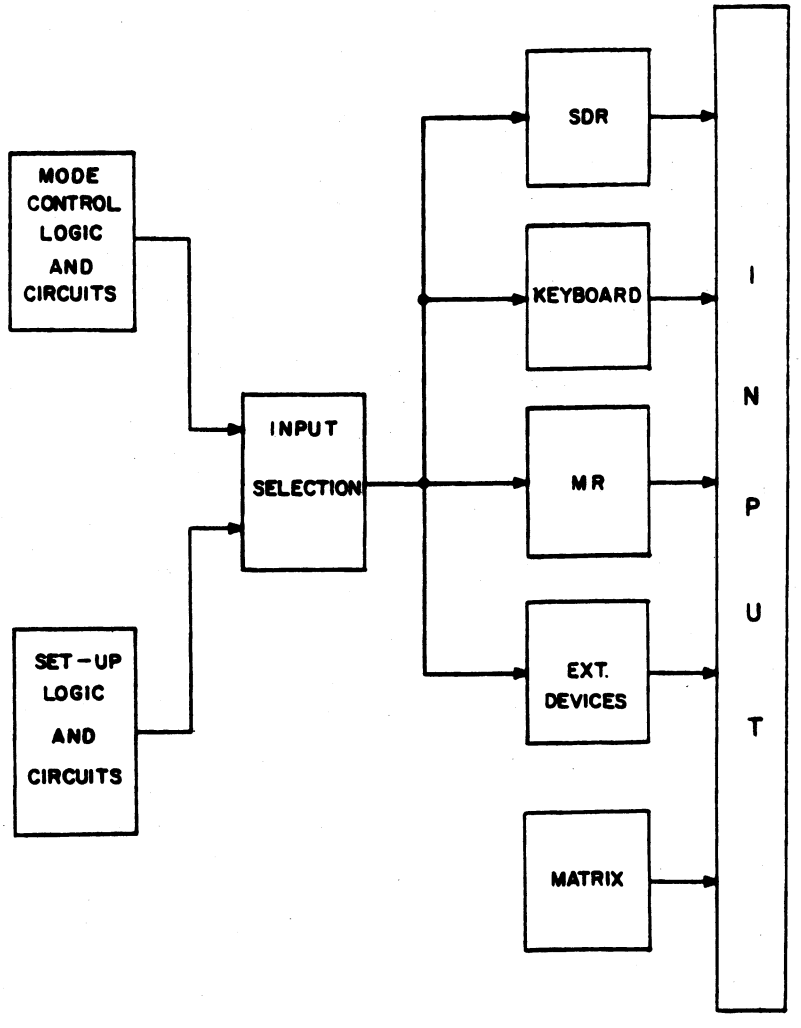


Figure 4-44. Input Scheme.

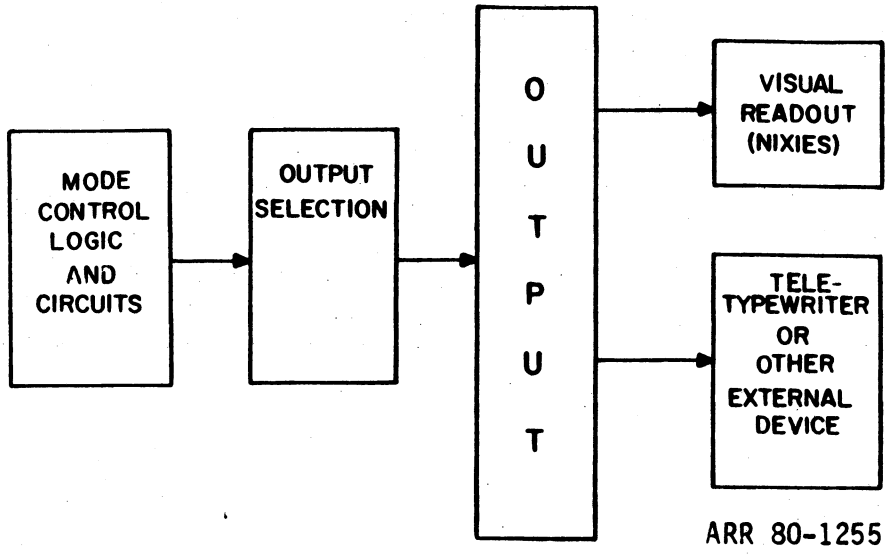


Figure 4-45. Output Scheme.

4-53. MODE CONTROL FOR IN/OUT SET UP OPERATION

a. Main Operation No. 1.

(1) The computer mode of operation is controlled by the AK, D, E, and K flip-flops (flip-flop G is used during some modes). Computer turnon generates the TD signal, forcing the mode control flip-flops into the following states:

1 AK = * Td
1 D = * Td
0 E = * Td
0 K = * Td

NOTE

During logic discussions, reference may be made to logic equations in TM 9-1220-221-34/1/1.

(2) The mode control veitch diagram for input-output operation in figure 4-46 will be referred to throughout this text and should be referenced each time a particular mode configuration is noted.

(3) The computer will remain in the sync bit counter mode until the bit counter flip-flops (B1 thru B6) synchronize with the sector track on the memory disk. This action occurs during the presence of Td. Refer to paragraph 4-55 bit counter sector track and synchronization. With the bit counter synchronized, flip-flop TX one sets, allowing flip-flop E to one set.

1 E = /KD1/ E- /AKA/ /TXA/

4-53. MODE CONTROL FOR IN/OUT SET UP OPERATION--Continued

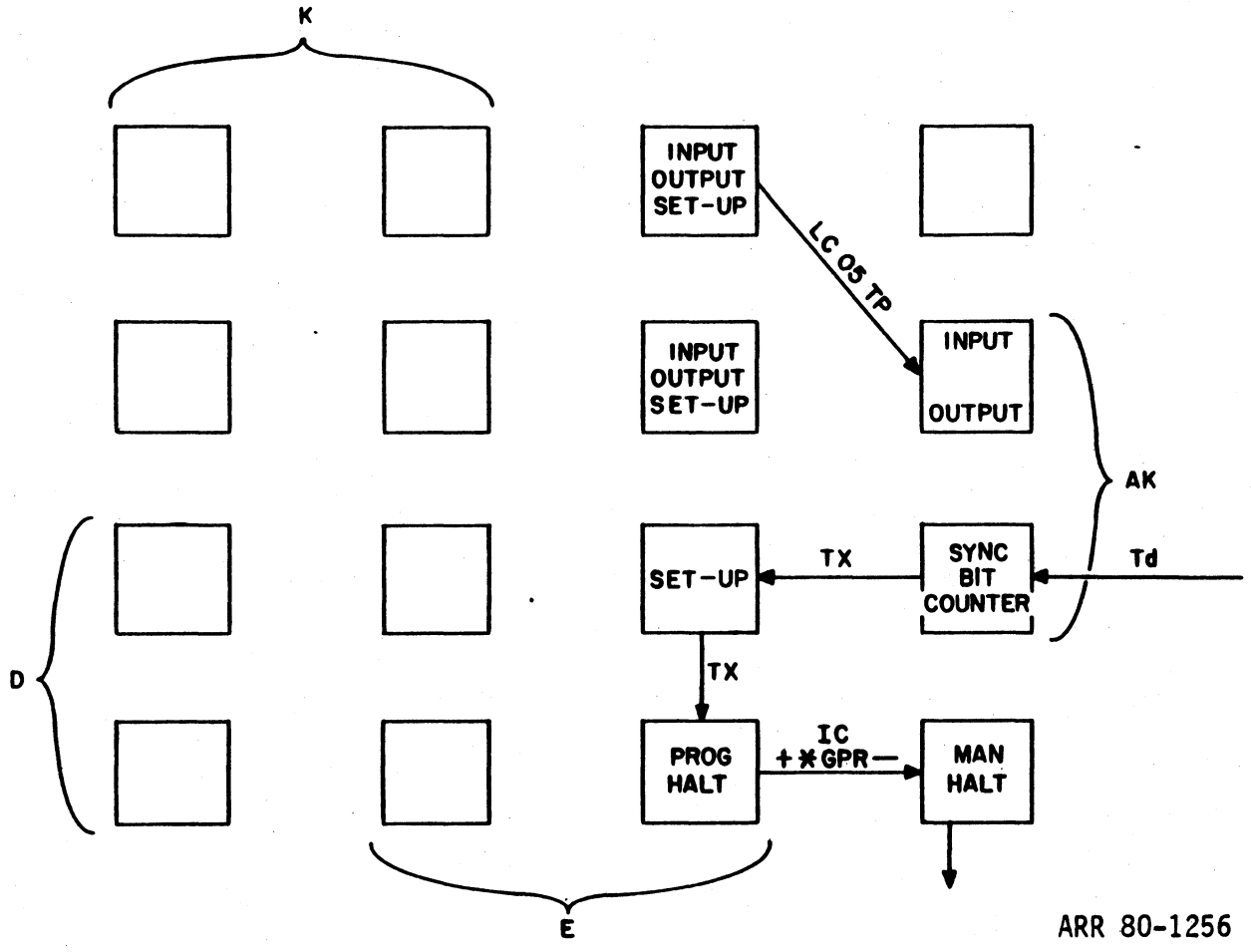


Figure 4-46. Mode Control Veitch Diagram for I/O.

(4) With TX flip-flop now one set, every word time the computer will enter the program halt mode.

0 AK = /ED3/ /TXB/

(5) While in the program halt mode, the following are some of the actions that will take place in anticipation of going to the input-output mode.

Ø 03 = (KED3) 1 04 = (KED3) Ø 0B6 = (KED3)
Ø 02 = (KED3) 1 0B3 = (KED3) Ø 0B5 = (KED3)
Ø CP6 = /KA-/ E 1 0B4 = (KED3)
Ø 05 = (KED3) 1 0B2 = /KA-/E

(6) The computer will remain in the program halt mode until actuated by the operator or an external device such as the SDR. Reference to figure 4-49 will show that the term GPR- is true when the SDR is cabled to J017 and the COMPUTE switch on the SDR is in the HALT position. This condition places flip-flop E in the off state:

Ø E = *GPR- (KED3) AK-

The computer is now in the manual halt mode.

b. Main Operation No. 2.

(1) Depression of the START FADAC button on the SDR results in the following:

(a) The computer will go to the input-output mode.

NOTE

Refer to paragraph 4-56 for discussion of input device selection.

(b) Input device determination is made.

(c) The FADAC and SDR generate logic signals causing information to be transferred from the SDR to the computer.

(2) Reference to the illustration in figure 4-52 shows that depression of the START FADAC button generates the term FBPR from the SDR. The term FB in the computer causes the one setting of CP6.

$$1\ CP6 = /KD1/\ (EAKO)\ *FB\ /TPA/$$

(3) The one setting of CP6 provides logic necessary to one set flip-flop E and zero set the D flip-flop.

$$1\ E = /KD1/\ (EAKO)\ CP6$$
$$\emptyset\ D = /KD1/\ (EAKO)\ CP6$$

(4) The computer is now in the input-output setup mode and will remain so for 17 word times. At this time the IN-OUT indicator on the front panel is illuminated (fig. 4-47).

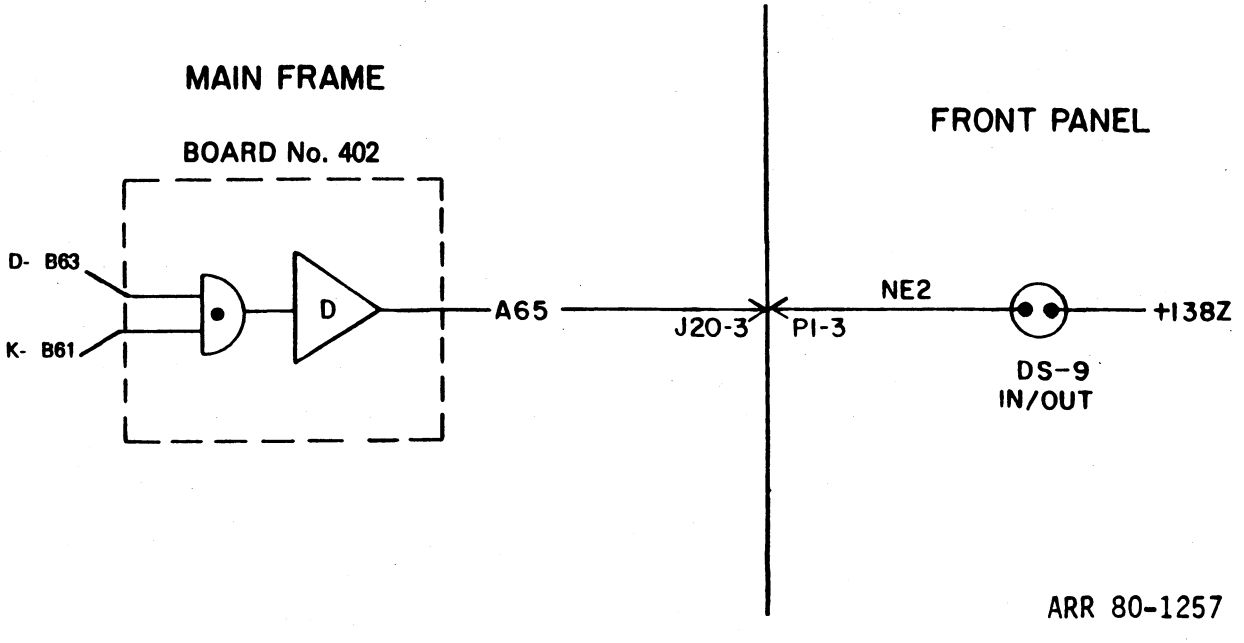


Figure 4-47. Input-Output Lamp Circuit.

4-53. MODE CONTROL FOR IN/OUT SET UP OPERATION--Continued

c. Main Operation No. 3.

(1) The computer will remain in the input-output setup mode for 17 word times to allow zeroing of the Q loop at TP time of each Q word, to prevent information flow into memory until desired. During information flow, a one at TP time in the Q loop indicates data in the Q loop is to go to memory. To prevent flow of nonpertinent data into memory, this bit (TP) is zeroed until the proper time. This 17-word period is controlled by the L register maintaining a count of 16. At the beginning of this 17-word period the left channel of the L register is zeroed:

```
1 LC  = /KED2/ (TLC) (BL1) (ERR-)
Ø LP  = 05- B6 K- LC
Ø L32 = LP- /TOA/ /KB-/
```

(2) The illustration in figure 4-48 shows that the above logic will zero the left channel portion (T28-T32) of the L register. At TP time of the first word of the 17, LC is zero set and 05 is one set:

```
Ø LC /TPA/
1 05 = 05- /04A/ (KSUØ) /TPA/
```

(3) With 05 in the one state, Q loop control flip-flop QC one sets and will remain on for the duration of each of the ensuing 16 words, except at TP time:

```
1 QC = (KSUØ) (054) OB3 /032-/ (ERR-) /TXC/
Ø QC = TP
Ø QP = /TOB/
      +(KSUØ) QC 04 TP
```

At T28 of the second word, LC will one set:

```
1 LC = /KED2/ (TLC) (BL1) (ERR-)
```

During this word time at T30, LP will one set through:

```
1 LP = 05 B6 LX- (KLC-)
```

And LC will zero set and remain off until T28 of the next word:

```
Ø LC LX- (KLC-) 05 B6
```

(4) Flip-flop LP now will be controlled by recirculate logic and will remain off due to the writing of zeros during the first word time of this mode. Refer to figure 4-49. At the end of second word time, the left channel portion of the L register contains a count of one.

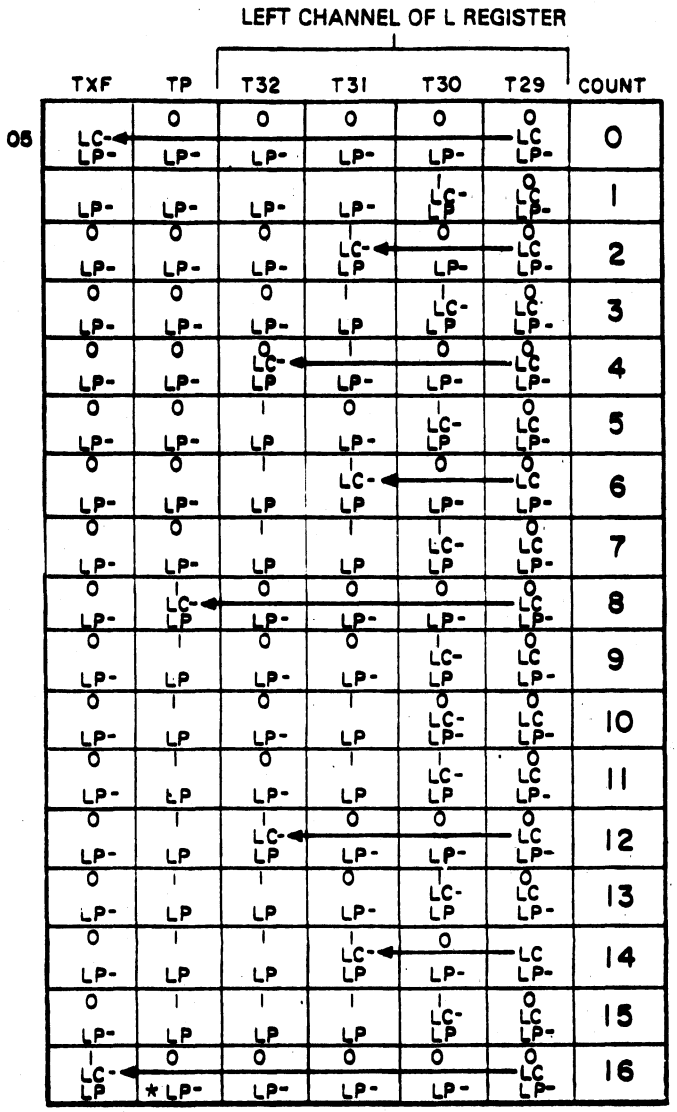


Figure 4-48. L Register Counter.

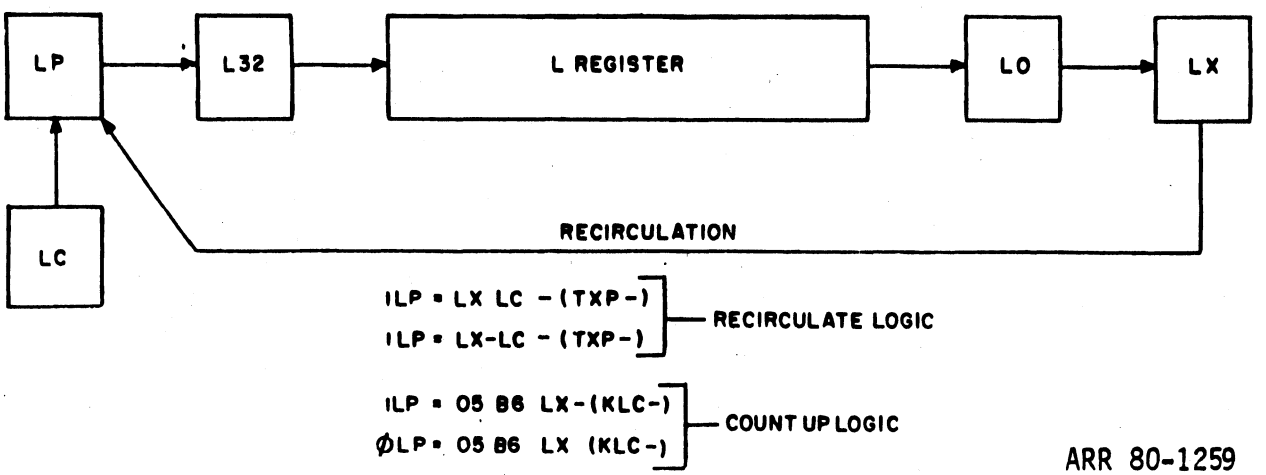


Figure 4-49. L Register Block Diagram.

4-53. MODE CONTROL FOR IN/OUT SET UP OPERATION--Continued

(5) At T28 of the third word, LC will once again one set:

1 LC = (KED2) (TLC) (BL1) (ERR-)

LP will remain zero set due to LX being on as a result of recirculate logic. The L register contains a count of one from the last word time. At T31 LC will zero set due to recirculation logic:

Ø LC = 05 B6 (KLC-)

And LP one sets as a result of the same logic:

1 LP = 05 B6 LX- (KLC-)

Recirculate logic will zero set LP at T32:

Ø LP = LX- LC- (TXP-)

(6) The conclusion of the third word time will show the L register contains a count of two. Refer to figure 4-48, the L register counter. The L register will continue counting in the manner shown above for the next 14 word times.

(7) Logical counting by the L register counter will show that LC, TP, and 05 flip-flops are one set at Tp time of the 17th word, or the L register containing a count of 16, and will allow the computer to go to the input-output mode, AK D- E- K-.

1 AK = /KED2/ (OLTP) (ERR-)
Ø E = (054) OB3 LC /KED2/ /TPB/ (ERR-)

NOTE
Refer to mode control veitch figure 4-46.

(8) At this same time 05 will zero set:

Ø 05 = LC 05 (KSUØ) TP

The term RGO, comprising /KOPC/, 04, and OB5- is now true, and energizes the SDR tape feed mechanism, refer to figure 4-52.

4-54. INPUT-OUTPUT MODE OPERATION

a. General. All explanations of input-output mode operations will be detailed by means of the input-output mode operations veitch diagram. The box numbers used below refer to the box numbers in figure 4-50.

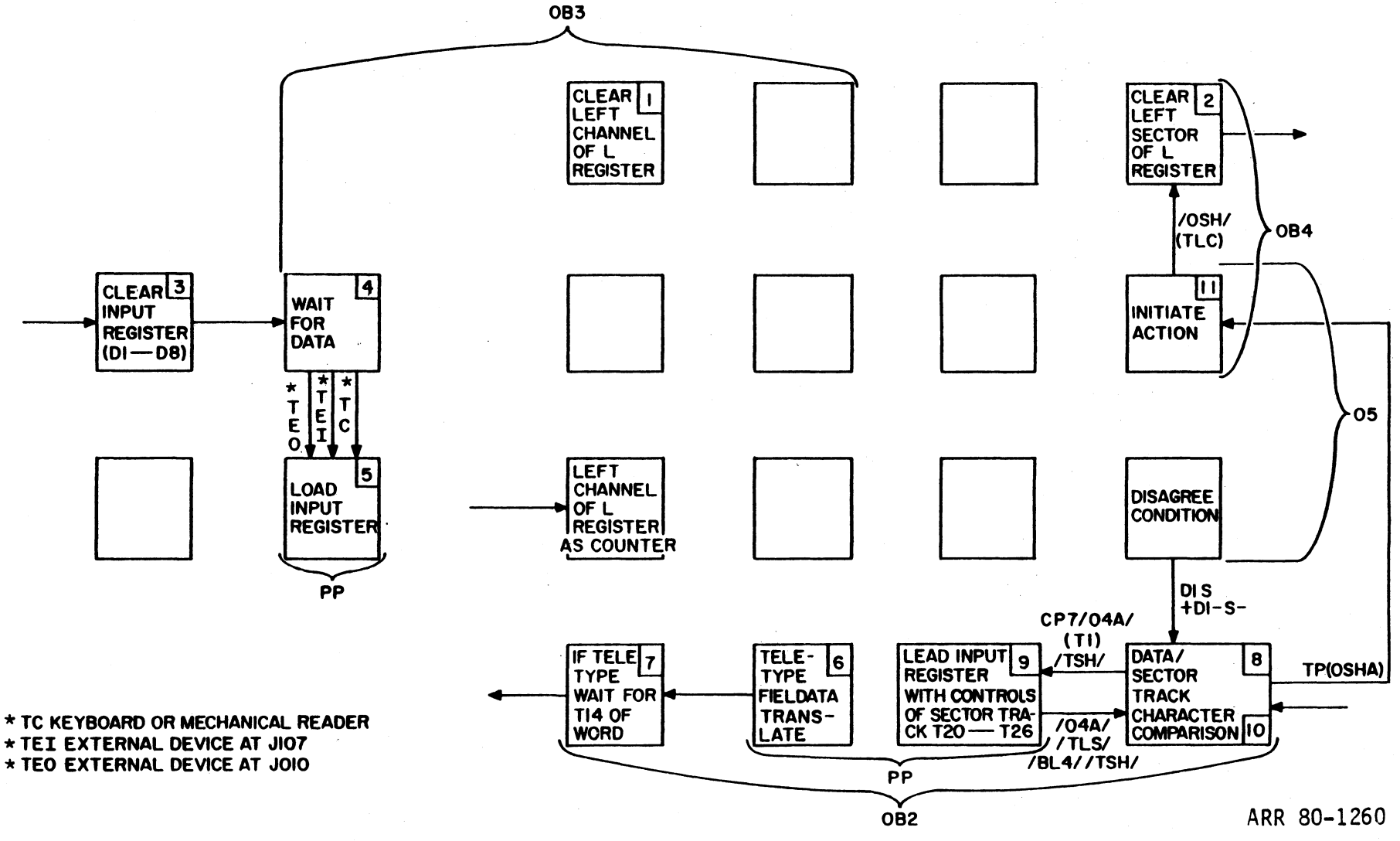


Figure 4-50. Input-Output Mode Operations Veitch Diagram.

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

b. Box 1.

(1) The left channel portion of the L register is zeroed during the first word time in the input-output mode:

1 LC = /KIO/ (TLC) (BL1)
Ø LP = 05- B6 (KLC-)
Ø L32 = /KB-/ LP- /TOA-/

The display control flip-flop DSP also zero sets:

Ø DSP = /KIOA/ OB5-

(2) The next word time brings the zero setting of OB3, and the one setting of CP7 if the SDR is in teletype input; refer to figure 4-53 for term *CTT generation.

Ø OB3 = /KIOA/ OB3 OB2 TO
1 CP7 = *CTT /04A/ OB5- /KIOA/

c. Box 2. During the next word the left sector portion of the L register is zeroed and flip-flop OB2 is zero set:

Ø OB2 = /04A/ (OSHB) 05- /TXA/

d. Box 3. Flip-flops D1 thru D8 which are used as the input-output register are zero set by (OCL):

Ø D1 D8 = (OCL)

Additionally, OB3 and PP flip-flops are one set:

1 OB3 = /KIO/ OB3- OB2-
1 PP = /KOPC/ OB2-

e. Box 4.

(1) The term TEI is generated whenever the SDR reads an information line from the program tape and will cause OB4 flip-flop to zero set which allows loading of the input-output register (D1 thru D8). See figure 4-52 for generation of TEI.

0 OB4 = *TEI OB6- OB5- (OWT)

(2) Term TEI is derived from the SDR term, TR, and is used in conjunction with TEI-, a term derived from the SDR term, TR-. These terms, TEI and TEI- control OB2 and OB3 flip-flops which in turn control OB4, thereby controlling the input-output register. OB4 flip-flop must be zero set before D1 thru D8 can accept an input. The OB4 flip-flop prevents signal bounce from affecting the D1 thru D8 flip-flops. See figure 4-51 for analysis of input signals and effect on OB3 and OB4 flip-flops.

TC MECHANICAL READER OR KEYBOARD SEQUENCING TERMS. TC IS TRUE SHORTLY AFTER AN I-LINE IS TRUE. TC- IS TRUE PRIOR TO I-LINE GOING FALSE.

TC-

TEI WITH SDR AT JOI7 TEI IS TRUE WITH ANY I-LINE TRUE. WITH EXTERNAL INPUT EQUIPMENT THIS TERM CAN BE SET TRUE WITH A SWITCHING DEVICE.

TEI- WITH SDR AT JOI7 TEI- IS TRUE DURING READING OF A SPROCKET, OR CLOCK ON EACH I-LINE. WITH EXTERNAL INPUT EQUIPMENT THIS TERM CAN ALSO BE SET TRUE WITH A SWITCHING DEVICE

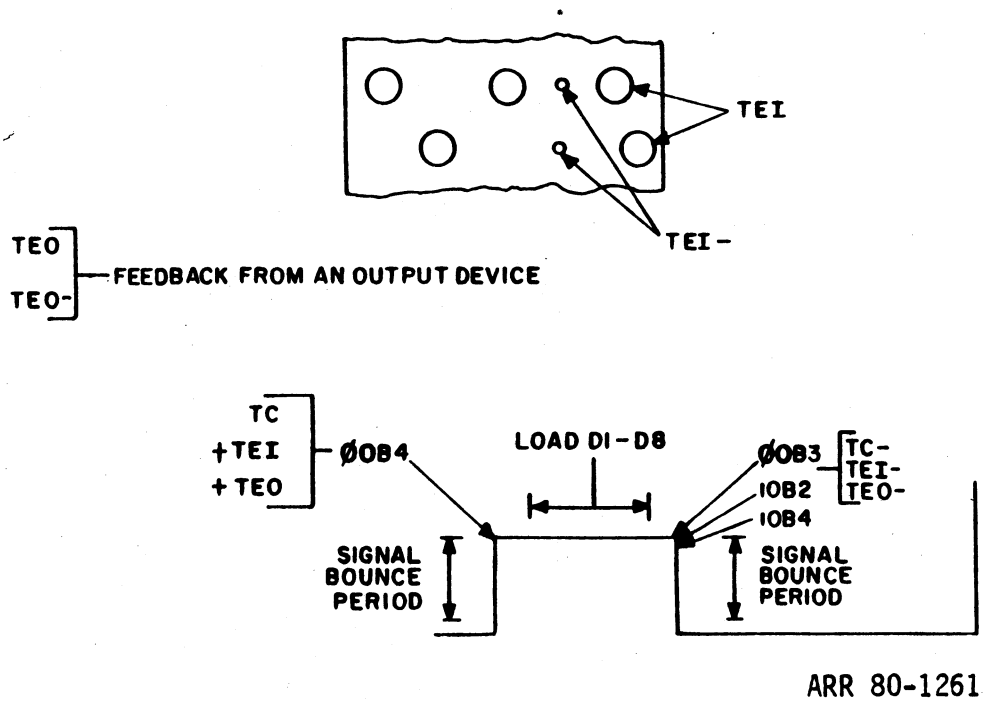


Figure 4-51. Input Information Line Breakdown.

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

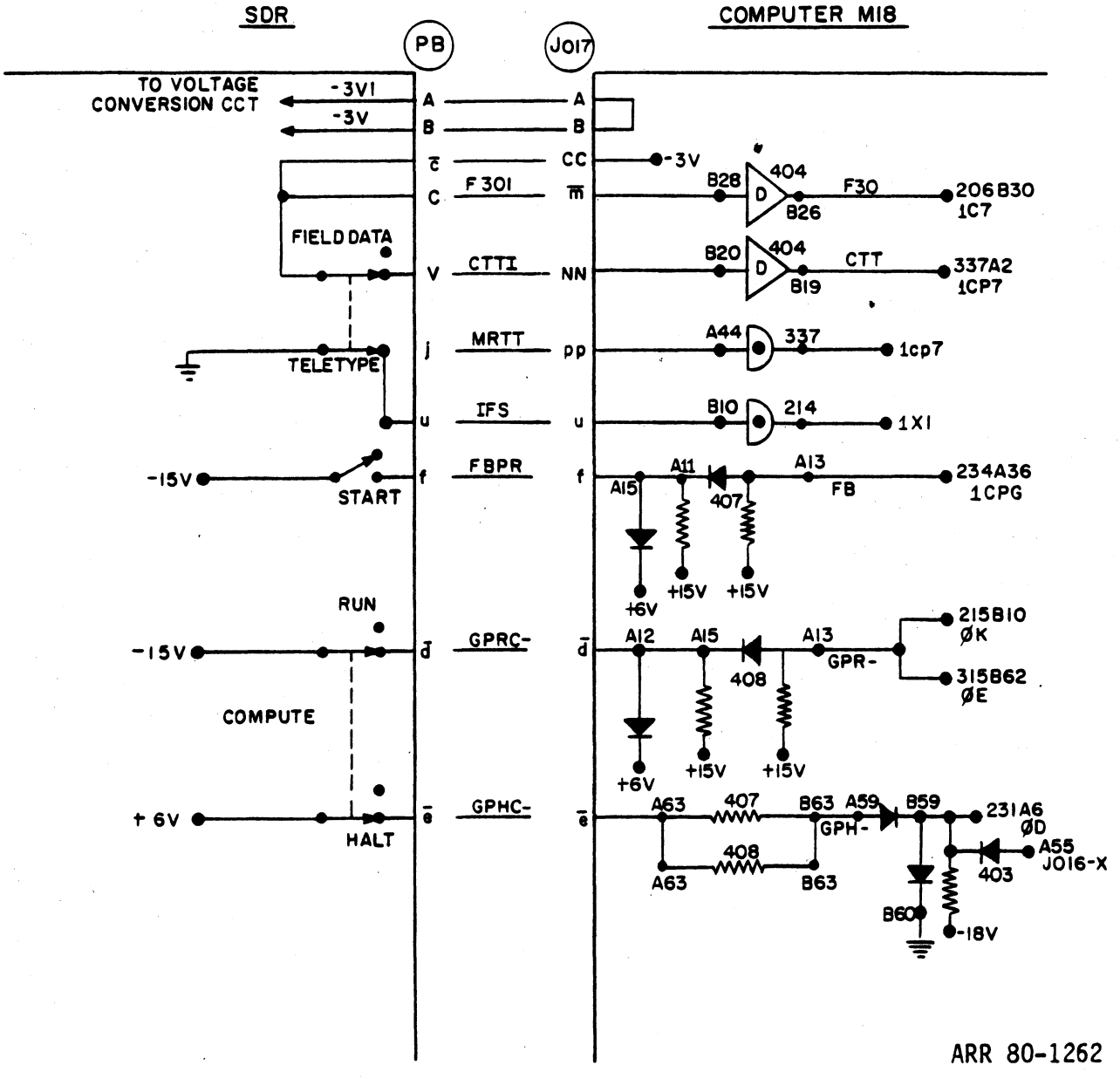


Figure 4-52. SDR To M18 Computer Input Cable (sheet 1 of 3).

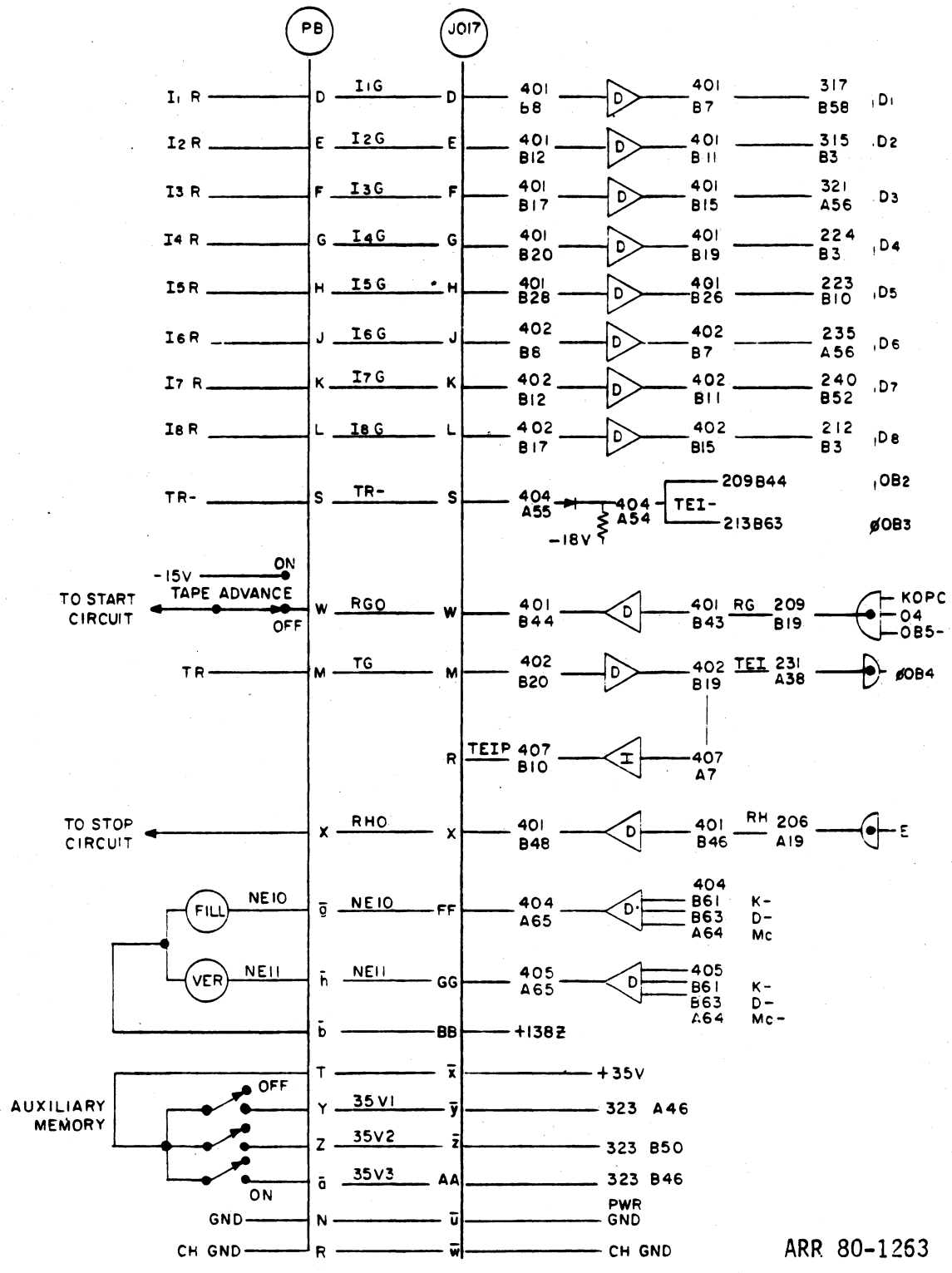


Figure 4-52. SDR To M18 Computer Input Cable (sheet 2 of 3).

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

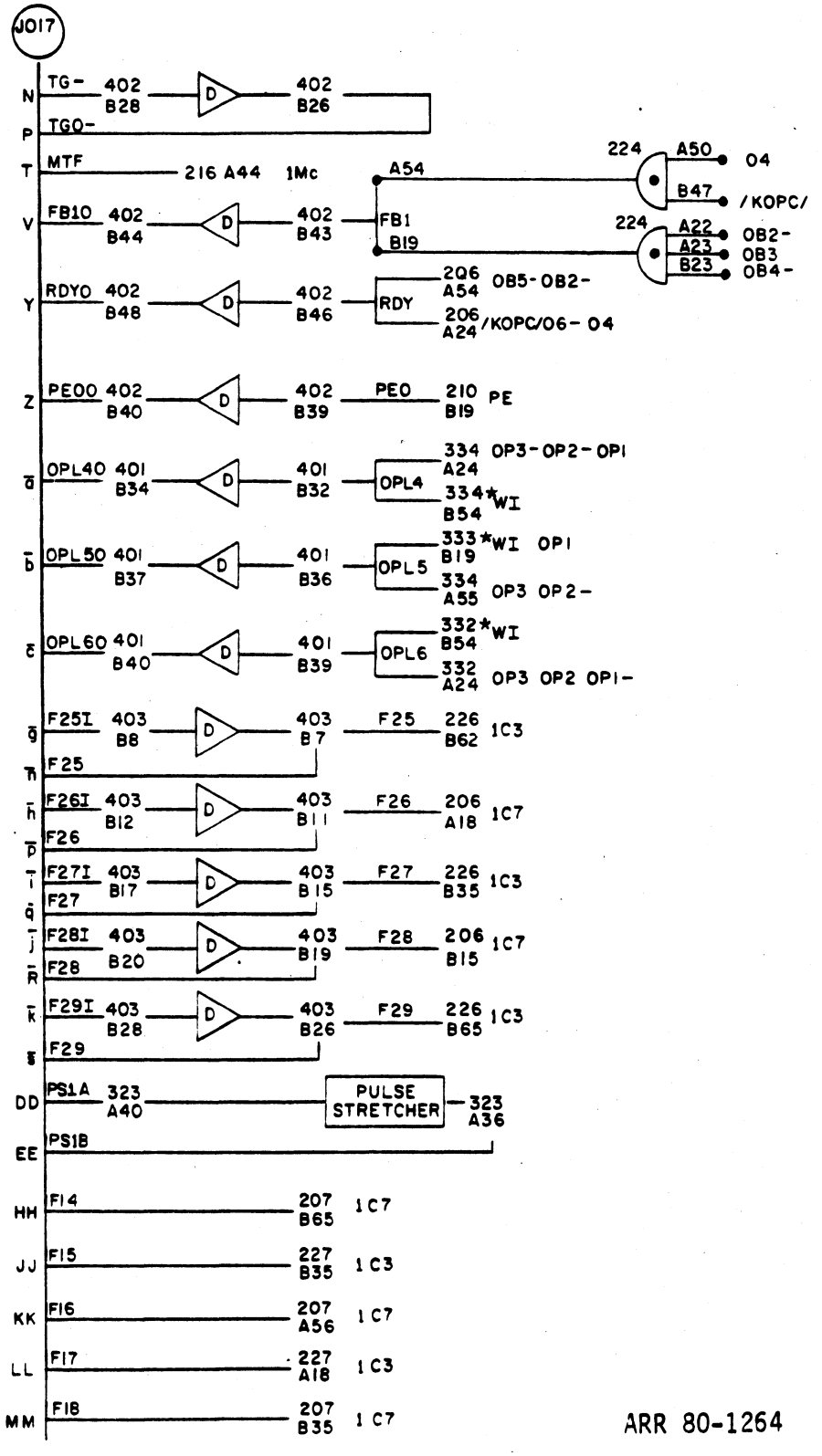


Figure 4-52. SDR To M18 Computer Input Cable (sheet 3 of 3).

f. Box 5.

(1) The input-output register can be loaded:

1 D1 = *I1 (OSA)
1 D8 = *I8 (OSA)

NOTE
Refer to figure 4-52 for I-line generation from SDR.

(2) With TEI- present, OB2 will one set:

1 OB2 = OB6- OB5- /KIOS/

g. Box 6.

(1) Flip-flop PP is zero set for teletype-sector track or field data-sector track character comparison.

Ø PP = (OTR) /04A/

(2) At this time if the input characters were field data, OB3 would zero set:

Ø OB3 = CP7- /04A/ 02- /TRS/ (OGO) /BL4/

(3) Field data-sector track character comparison will not be discussed here because it is similar to teletype-sector track character comparison, which is discussed in paragraph 1.

h. Box 7. Because T15 thru T19 of the sector track contains the teletype comparison information, OB3 must be zero set to indicate this time:

Ø OB3 = CP7 /04A/ 02- /TRC/ (BL4) (OGO)

Term /TSH/ is now true.

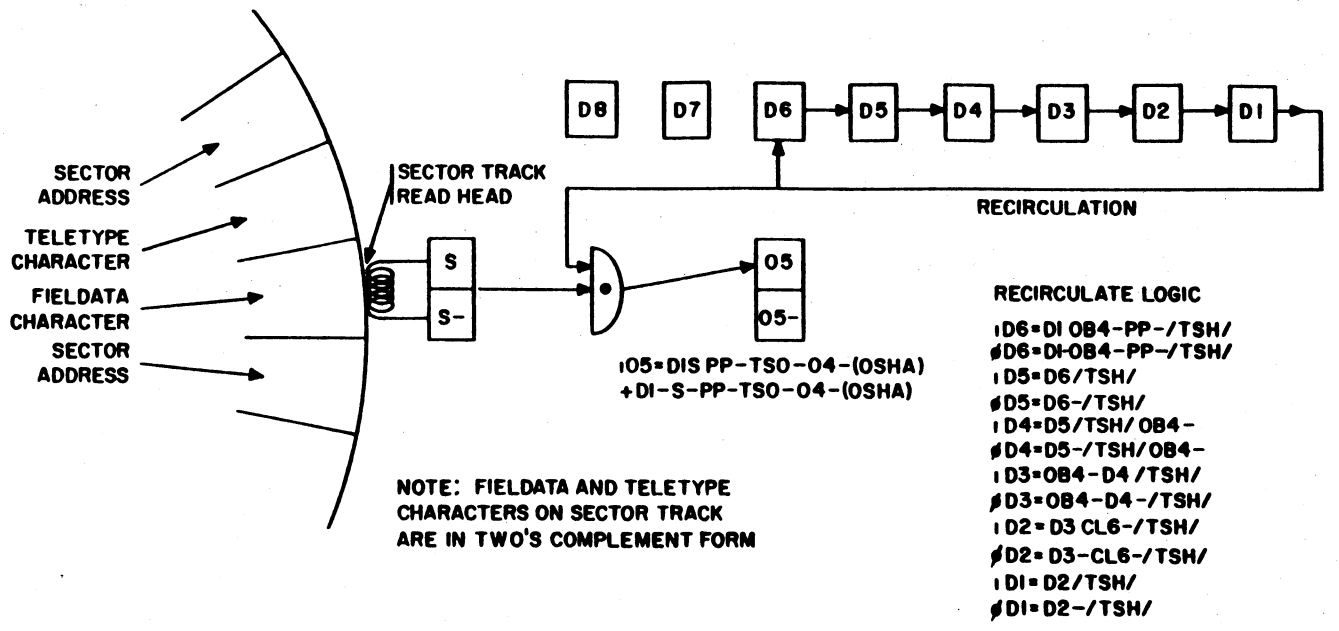
/TSH/ = K- E- D- AK DSP- OB3- OB2 TP- TD- TX-

i. Box 8.

(1) Teletype character in the input register, which is being recirculated, is compared with the sector track teletype codes for legitimacy. See figure 4-53.

(2) The computer will accept 16 field data characters and any character other than one of the 16 will be ignored. See table 4-21 for input/output characters acceptable to the computer. In that the sector track teletype and field data information is written in two's complement, inverse comparison must be made between S, the sector track read flip-flop, and flip-flop D1 of the input register. The following shows the agreement and disagreement conditions.

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued



ARR 80-1265

Figure 4-53. Sector Track Input Character Comparison.

(a) Agreement. With inverse agreement between T15 and T19, flip-flops 05 and PP have been zero set at box 6 and 05 zero set with entrance to the input-output mode. At T19, PP will one set:

1 PP = CP7 /04A/ (T19) /TSH/ 05-

With field data input:

1 PP = CP7- /04A/ /TRC/ /BL4/ /TSH/ 05-

If flip-flops S and D1 are inverse from T15 thru T19, flip-flop D8 will copy the sector track information from T20 thus copying the BCD conversion of the teletype code.

1 D8 = S- /TSH/ (OOP)
Ø DB = S /TSH/ (OOP) 04

(b) Disagreement. If flip-flops S and D1 are the same at any time from T15 thru T19, 05 will one set and prevent the one set of PP which prevents reading of the teletype to BCD conversion into the input register.

1 05 = D1 S PP- TSO- 04 (OSHA)
+ D1- S- PP- TSO- 04 (OSHA)

PP will now remain in the off state. With 05 one set, go to the disagree box until T7 when OB3 is one set:

1 OB3 = (OSHA) 05 /TRS/ (BL6)

Table 4-21. Computer Input/Output Characters

Teletype Meaning		Computer Meaning			Field Data Meaning	
Character	Tape code	Octal mode	BCD mode	Binary conversion	Tape code	Character
0, P	01101	0	0	0000	00110000	0
1, Q	11101	1	1	0001	10110001	1
2, W	11001	2	2	0010	10110010	2
3, E	10000	3	3	0011	00110011	3
4, R	01010	4	4	0100	10110100	4
5, T	00001	5	5	0101	00110101	5
6, Y	10101	6	6	0110	00110110	6
7, U	11100	7	7	0111	10110111	7
8, I	01100	HALT	8	1000	10111000	8
9, O	00011	COMPUTE	9	1001	00111001	9
(+)", Z	10001	FILL	+	1010	00100010	+
-, A	11000	VERIFY	-	1011	00100001	-
., M	00111	LOCATION	.	1100	10111101	.
/, X	10111	CLEAR	CLEAR	1101	11011101	X
Car. Ret.	00010	ENTER	ENTER	1110	01000100	Car. Ret.
Blank	00000	BLANK	BLANK	1111	00000000	BLANK

05 also allows the L register to once again begin a counting sequence up to 16.

```
1 LC  = /KIO/ (TLS) (BL1)
1 LP  = 05 B6 LX- K- LC
1 032 = /KB-/ LP
```

Refer to figure 4-50 and 4-51 which illustrate the L register as a counter. At the end of the word time, flip-flop 05 will zero set:

```
Ø 05 = (KEO) OB3 PP- /TPA/
```

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

At T15 of the next word, teletype-sector track character comparison will resume. This word time will bring the character in the next sector being compared with D1 flip-flop. If disagreement continues, 05 will once again one set and cause the L register counter to up its count by one. The comparison by the S and D1 flip-flops is continued until inverse agreement is reached, or the L register counts to 16. If the L register counts to 16, this is indicative of an illegitimate character. At the count of 16 in the L register left channel, flip-flop LC is one set, TP is one set at the end of that word time, and 05 is one set due to disagreement logic (D1 and 5 or D1- and 5-). Under this condition return is made to box 1 to begin processing of the next input character.

j. Box 9.

(1) If inverse comparison was successful, the BCD code on the sector track is copied into the input register.

```
1 D8 = S- /TSH/ (OOP)
Ø D8 = S /TSH/ (OOP) 04
1 D6 = D8- (OOP) /04A/ /TSH/
Ø D6 = D8 (OOP) /04A/ /TSH/
1 D5 = D6 /TSH/
Ø D5 = D6- /TSH/
1 D4 = D5 /TSH/ OB4-
Ø D4 = D5- /TSH/ OB4-
1 D3 = D4 /TSH/ OB4-
Ø D3 = D4- /TSH/ OB4-
1 D2 = D3 /TSH/ CL6-
Ø D2 = D3- /TSH/ CL6-
1 D1 = D2 /TSH/
Ø D1 = D2- /TSH/
```

NOTE

Flip-flop D7 is not utilized in that only seven bits are copied from the sector track.

(2) At T26 flip-flop PP will zero set:

```
Ø PP = /04A/ /TLS/ /BL4/ /TSH/
```

k. Box 10. Go to box 10 and remain until TP time of the word when:

```
1 OB4 = (OSHA) /TPA/
1 05  = (OSHA) CP7 /TPA/
```

l. Box 11. Reference to table 4-21 will show that the computer uses the octal format, digits 0 thru 7, for information purposes. The remainder of the 16 characters are used for control purposes. While in box 11, the octal character will be loaded into the A register, and shifted left in the A register with the processing of each new character. Reference to figure 4-54 shows the flow of an input character from a device such as the SDR.

Table 4-22. Sample Piece of Program Tape

Tape code	Teletype meaning	BCD meaning	Octal meaning	Tape code	Teletype meaning	BCD meaning	Octal meaning
11101	1	1	1	11001	2	2	2
11101	1	1	1	01010	4	4	4
10000	3	3	3	11001	2	2	2
11001	2	2	2	00001	5	5	5
10000	3	3	3	01101	0	0	0
00111	.	.	Location	10000	3	3	3
11101	1	1	1	11001	2	2	2
11101	1	1	1	10000	3	3	3
10000	3	3	3	00010	Carriage return	Enter	Enter

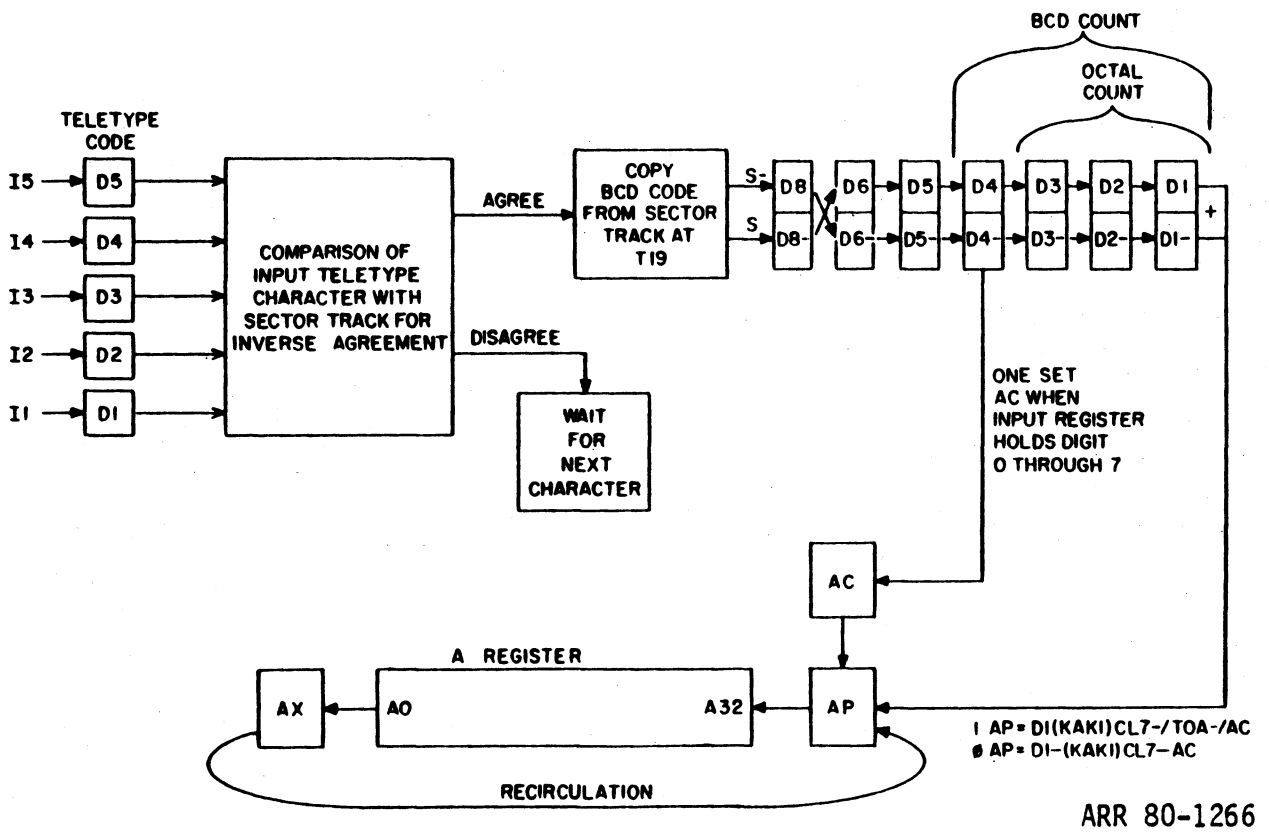


Figure 4-54. Input Character Flow Diagram.

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

m. Sample input flow.

(1) As an example of flow, the following information is shown on a piece of program tape (table 4-22). When this instruction is interpreted it directs the computer as follows:

(a) Go to location channel 112, sector 123.

(b) At this location enter next instruction-channel 112, sector 124; command 24 (clear and add); and operand address-channel 112, sector 123.

NOTE

Refer to paragraph 4-62 for explanation of meaning and formation of computer word.

(2) The location is the first piece of information processed into the A register. Look at the first digit of location 11323. The input register would be the following with the digit 1.

0 0 0 0 0
D5- D4- D3- D2- D1-

(3) With D4 flip-flop zero set, AC will one set and allow AP to copy flip-flop D1.

1 AC = D4- /OCT/
Ø AC = AC /TXF/ /DA-/
1 AP = D1 (KAK1) CL7- /TOA-/ AC
Ø AP = D1- (KAK1) CL7- AC
1 D3 = AX /TSH/ OB4 /032-/
Ø D3 = AX- /TSH/ OB4 /032-/
1 D2 = D3 /TSH/ CL6-
Ø D2 = D3- /TSH/ CL6-
1 D1 = D2 /TSH/
Ø D1 = D2- /TSH/

(4) The AC flip-flop will remain one set until TXF time allowing D1 and AP to copy the first digit of the address into the A register. At T27 of this word, the 05 flip-flop will be zero set allowing flip-flop OB3 to one set:

Ø 05 = /OSH/ (TLC)
1 OB3 = (OSHB) 05- (04X)

(5) Return is now made to box 1 to begin processing of the next character, the second digit of the address 11323. This process is continued until five octal characters, indicative of the channel and sector location address are in the A register.

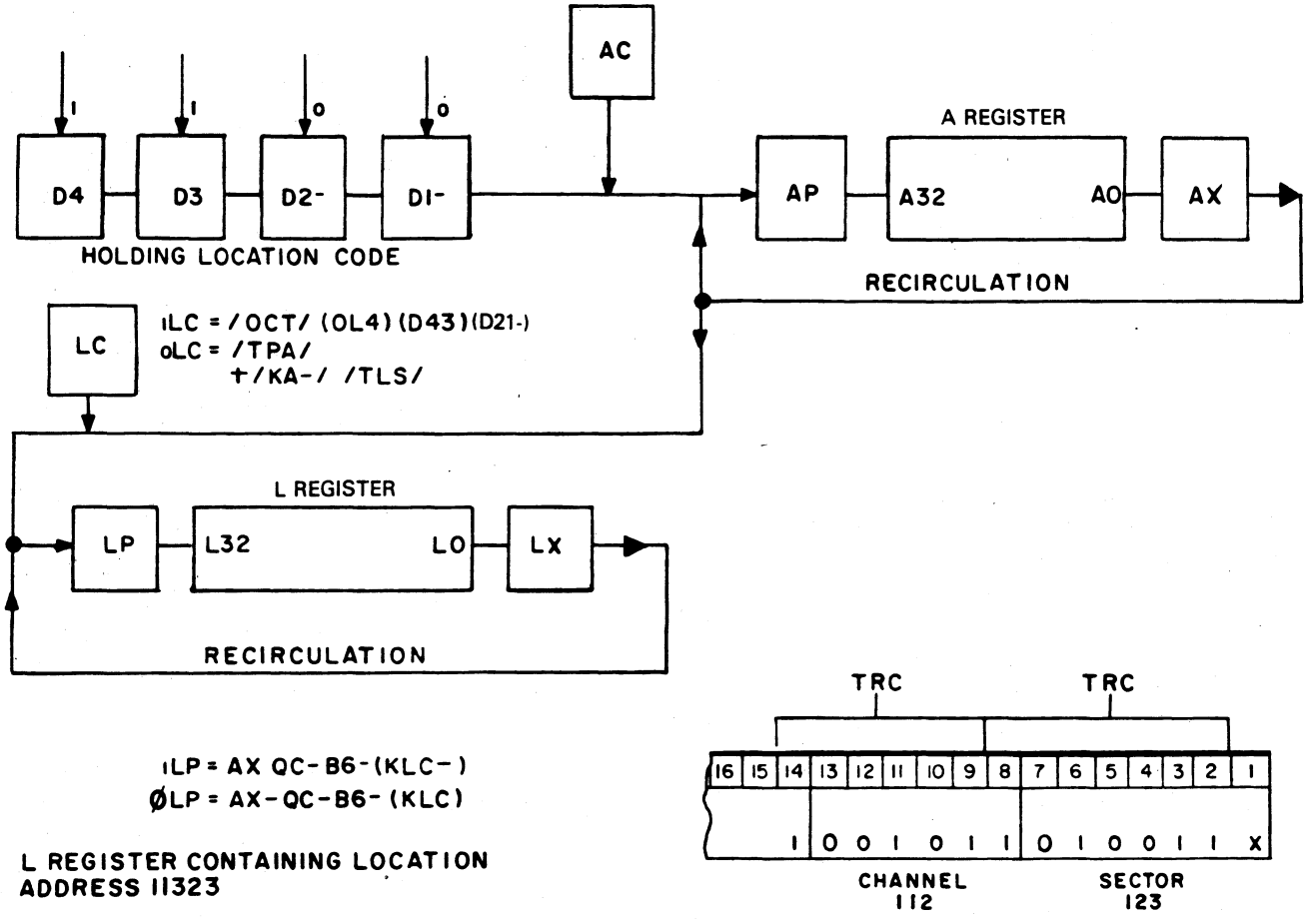


Figure 4-55. Loading L Register with Location Address.

(6) Upon receiving a location code, the input register, after inverse agreement, would be the following:

1 1 0 0
D4 D3 D2- D1-

This will allow the L register to copy the contents of the A register (fig. 4-55). The following logic will then be effected.

1 LC = /OCT/ (OL4) (D43) (D21-)
Ø LC = /TPA/
+ /KA-/ /TLS/
1 LP = AX QC- B6- (KLC-)
Ø LP = AX- QC-B6- (KLC-)

Between T2 and T14 the L register will copy and hold from the A register, location address 11323.

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

(7) The next piece of information to be processed will be the 11 octal characters that constitute an operand word or an instruction word. Each character of the 11-character word will be processed into the A register in the same manner as the location address. Upon receiving an enter code (1110), the contents of the register A will be loaded into the N register. The enter code allows CL7 flip-flop to one set:

1 CL7 = (OL4) /OCT/ (D43) D2 D1-

(8) At the beginning of the next word, CL2 flip-flop will one set:

1 CL2 = (KIOC) /TOA/ (OL4)

CL2 will be used in the processing of the information word into memory through control of the R loop. The N register will now copy the contents of the A register:

1 NC = (KIQC) 04 /TOB/
Ø NC = /KA-/ /T32/

With NC one set:

1 NP = AX /KB-/ 04 NC /TPO-/
Ø NP = AX- /KB-/ 04 NC /TPO-/

Refer to figure 4-56 for loading of N register.

(9) It should be noted that the first word of both 16-word loops, R and Q, is under the read head when the location address is for sector 1. For sector 2 location address, the second word of the 16-word loops would be under the read head if 16-word agreement. On input by character, the R, Q, and D loops are not used. One word time after the N register contents are copied into the R loop, the contents of the L register, containing the location address, is copied into the Q loop (figure 4-57).

(10) The QC flip-flop will one set due to the RC flip-flop being in the one state.

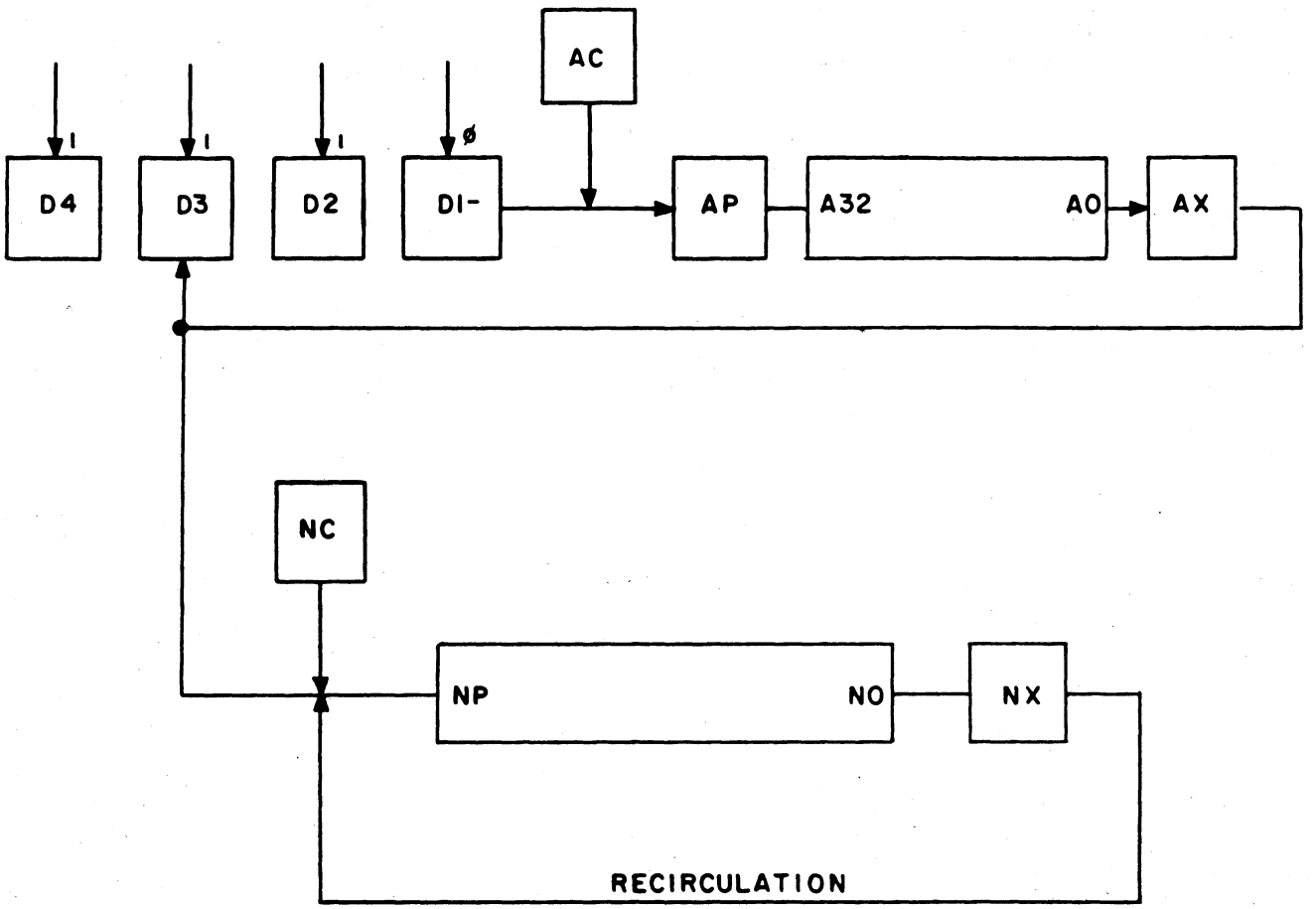
1 QC = /KIO/ RC 04 (ERR-) /TXC/

And will zero set at the end of each word:

Ø QC = TP

With QC in the one state, QP will copy the contents of the L register:

1 QP = /KB-/ QC LX TP-
Ø QP = /KB-/ QC LX- TP-



1CL7 = (OL4) /OCT/ (D43) D2 DI-
1CL2 = (KIOC) /TOA/ (OL4)

1NC = (KIOC) 04 /TOB/
øNC = /KA-/ /T32/

1NP = AX /KB-/ 04 NC / TPO-/
øNP = AX- /KB-/ 04 NC / TPO-/

ARR 80-1268

Figure 4-56. N Register Loading.

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued

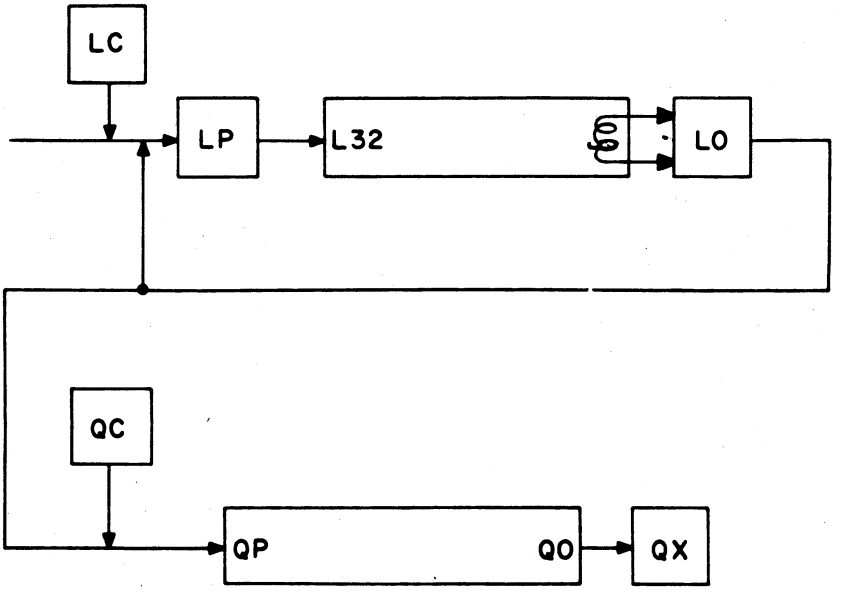


Figure 4-57. Copying of Location Address Into Q Loop.

When the Q loop copies the contents of the L register, a 1 is always written in the Tp bit position of the Q loop word to indicate storage of the word in main memory:

1 QP = (KAK1) QC TP

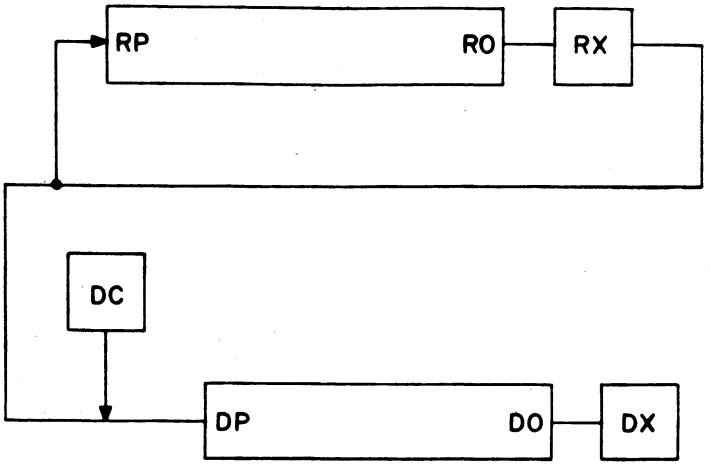
(11) The contents of the R loop are copied into the D loop continuously (fig. 4-58).

(12) While the R loop has been recirculating the word, or loading the word into the D loop, the Q loop, which contains the location address of the word in the R and D loops, is copied into the I register. This is done to allow 128-word writing agreement between IP + 2 and S. Flip-flop IC one sets every word time through:

1 IC = /KIO/ /TOB/

And zero sets at T18 or TP of the word:

ø IC = /TOP/ (KAK1)
+ TP



1DC = /KIO/ (OL4) /TOB/
ØDC = /TPA/
1DP = /KB-/DC RX
ØDP = /KB-/DC RX-/TOB/

ARR 80-1270

Figure 4-58. D Loop Copying the R Loop.

(13) With IC one set, the IP flip-flop will copy the location address contained in the Q loop:

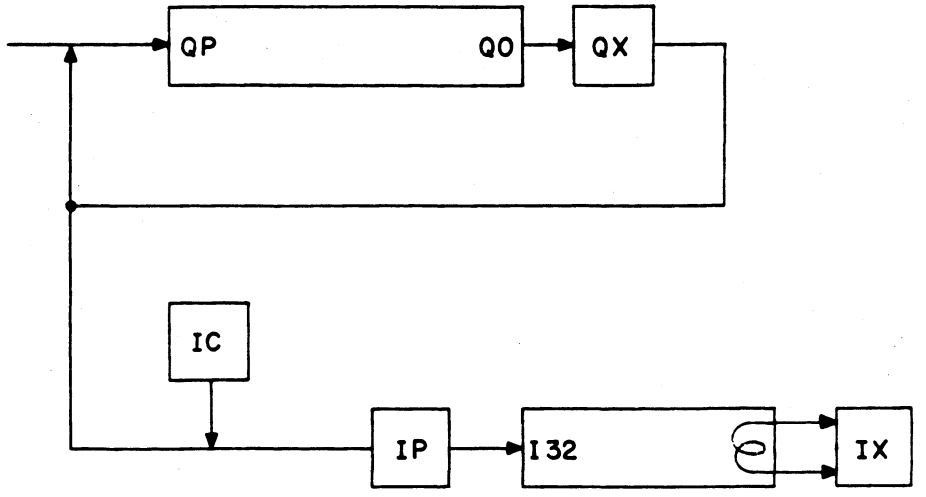
1 IP = QX (KAK1) IC
Ø IP = QX- (KAK1) IC

See figure 4-59 for loading of the I register. Flip-flop ID in the zero state will indicate 128-word writing agreement and will allow the word contained in the D loop to be loaded into main memory (fig. 4-60).

(14) Flip-flop MN will copy DO continuously:

1 MN = /KA-/ DO MC
Ø MN = /KA-/ DO- MC

4-54. INPUT-OUTPUT MODE OF OPERATION--Continued



$_{1}$IC = /KIO/ /TOB/

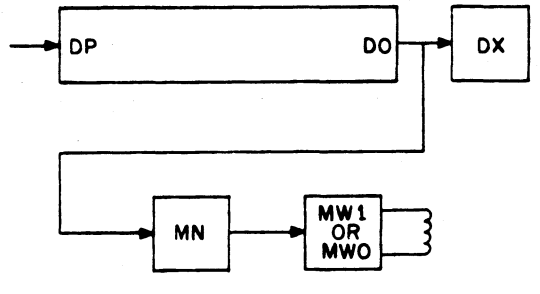
øIC = /TOP/ (BL6)(KAK1) + TP

$_{1}$IP = QX(KAK1)IC

øIP = QX - (KAK1)IC

ARR 80-1271

Figure 4-59. Loading I Register.



$_{1}$MN = /KA-/ DO MC

øMN = /KA-/ DO-MC

$_{1}$MW1 = /MNA/(KW)/TPO-/

$_{1}$MWO = /MNA-/(KW)/TXP-/

ARR 80-1272

Figure 4-60. Main Memory Loading From the D Loop.

4-55. BIT COUNTER SYNCHRONIZATION

a. Sequential Timing.

(1) Initial turnon of the computer causes generation of the TD signal which places the computer in the sync bit counter mode (fig. 4-46).

1 AK = *TD
1 D = *TD
Ø E = *TD
Ø K = *TD

Refer to figure 4-61 for the makeup and the prescribed count of the bit counter.

(2) Flip-flops B1 thru B6 comprise the bit counter and are controlled by the timing flip-flops TO, TX, TP, and TSO. To show the sequencing of the bit counter assume energization of the computer causes the timing flip-flops to be at random and B1 thru B6 to be in the configuration shown in table 4-23.

b. Synchronization of Bit Counter.

(1) Once the bit counter comes into the proper counting sequence, it must now synchronize with the sector track on the memory disk. There are 128 sectors or word locations on each of the 64 main memory channels and are numbered octally 000 thru 177. The sector track tells the computer what sector on the disk is passing under the read or write heads at any given time. Each sector on the sector track contains the address of the next sector at T2 thru T8, and T20 thru T26. In addition, the two's complement format of the 16 acceptable teletype and field data characters are contained on the sector track for comparison with input characters. The requirement of two's complement for character designation on the sector track will be discussed during sector track-bit counter synchronization.

(2) As shown, the first four bits of each sector are the same except sectors 036, 076, 136, and 176. In that the highest location address is 177, seven bits are satisfactory for addressing. The field data and teletype information, during input-output mode, is compared with the two's complement of that information on the sector track. Table 4-21 shows the character seven being 110111 in field data and 11100 in teletype. In two's complement it takes the form shown in sector 026. It might be noted that bits 8 and 7 of the field data code are utilized for parity and timing and are not considered on the sector track. Sector track information is read from memory by read flip-flop S.

(3) During the synchronizing phase, the TO flip-flop will be controlled by the S read flip-flop. Flip-flop TO will one set each time the S flip-flop zero sets.

1 TO = /KD1/ E- /AKA/ S- TO-

4-55. BIT COUNTER SYNCHRONIZATION--Continued

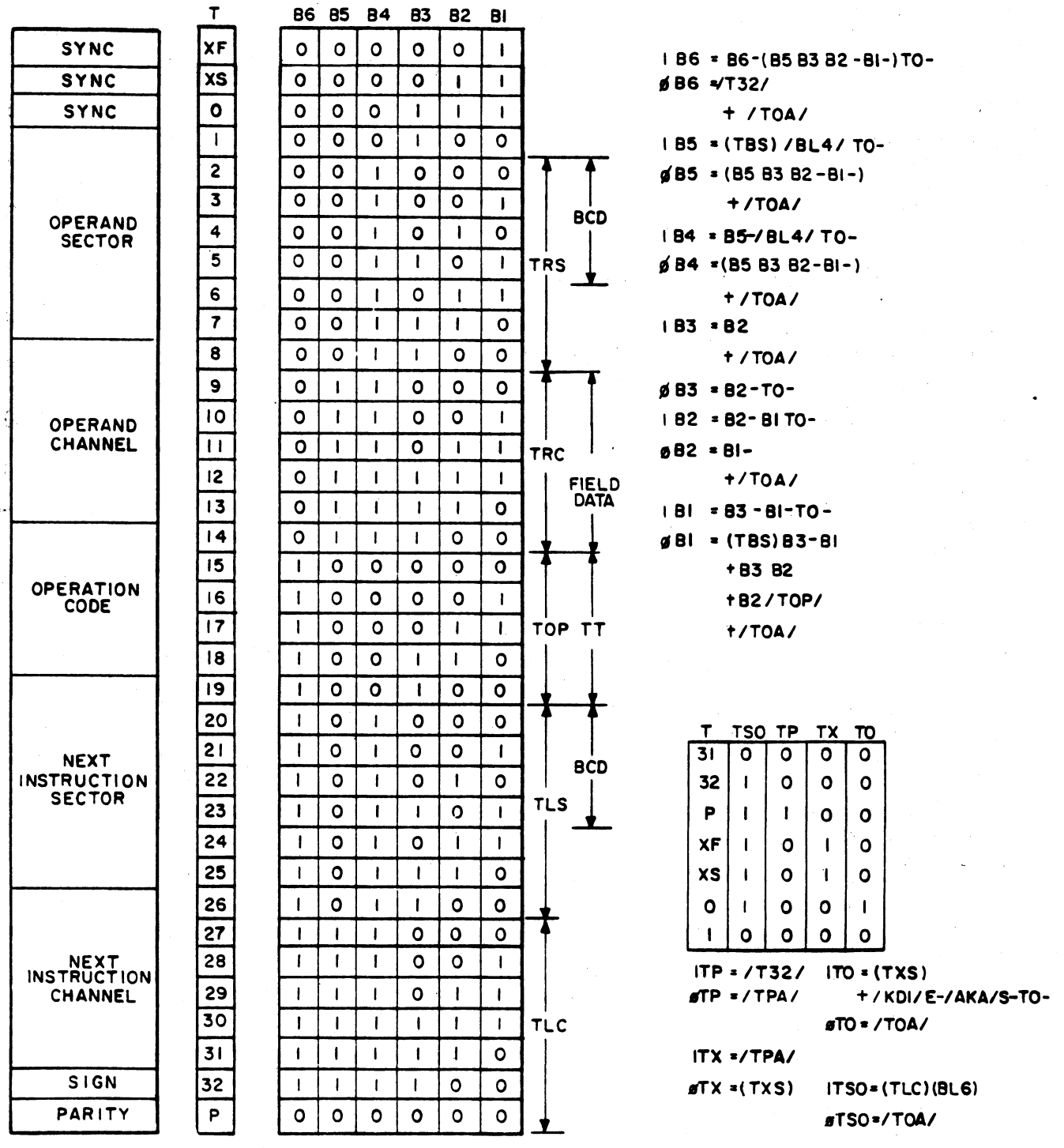


Figure 4-61. Bit Counter Configuration.

Table 4-23. Sample of Bit Sequencing.

	Bit counter						Logic	Timing Flip-Flops			
	B6	B5	B4	B3	B2	B1	TURNON	TSO	TP	TX	TO
*	0	1	0	1	0	1	1 B2 = B2- B1 TO-	0	0	0	0
	0	1	0	0	1	1	Ø B3 = B2- TO-	0	0	0	0
	0	1	0	1	1	1	1 B3 = B2	0	0	0	0
	0	1	0	1	1	0	Ø B1 = B3 B2	0	0	0	0
	0	1	0	1	0	0	Ø B2 = B1-	0	0	0	0
**	0	0	0	0	0	0	Ø B3 = B2- TO-	0	0	0	0
	0	0	0	0	0	1	1 B1 = B3- B1- TO-	0	0	0	0
	0	0	0	0	1	1	1B2 = B2- B1 TO-	0	0	0	0

*Bit counter in an improper counting sequence.

**Bit counter in proper counting sequence (Tp time).

(4) When TO is one set, the bit counter will go to T1 through:

Ø B6 = /TOA/
Ø B5 = /TOA/
Ø B4 = /TOA/
1 B3 = /TOA/
Ø B2 = /TOA/
Ø B1 = /TOA/

(5) This action will take place for each zero read from the sector track. There is only one sector on the sector track that will allow synchronization of the sector track with the bit counter. Table 4-22 shows that sector 176 contains ones with the exception of TXF and TXS. TO will be one set at TO time due to the zero at TXS time. At T1, the TO flip-flop will zero set.

Ø TO = /TOA/

(6) At T1 time, the bit counter will begin counting and continue through the remainder of the word due to TO not one setting again until the next word. The sector track is now in synchronization with the bit counter.

4-56. INPUT DEVICE SELECTION

a. Control of Input.

(1) Input device selection is controlled by the OB6, OB5, and 04 flip-flops. At computer turnon:

Ø OB6 = (KED3)
Ø OB5 = (KED3)
1 04 = (KED3)

Figure 4-62 shows that the input plug is selected at turnon of the computer.

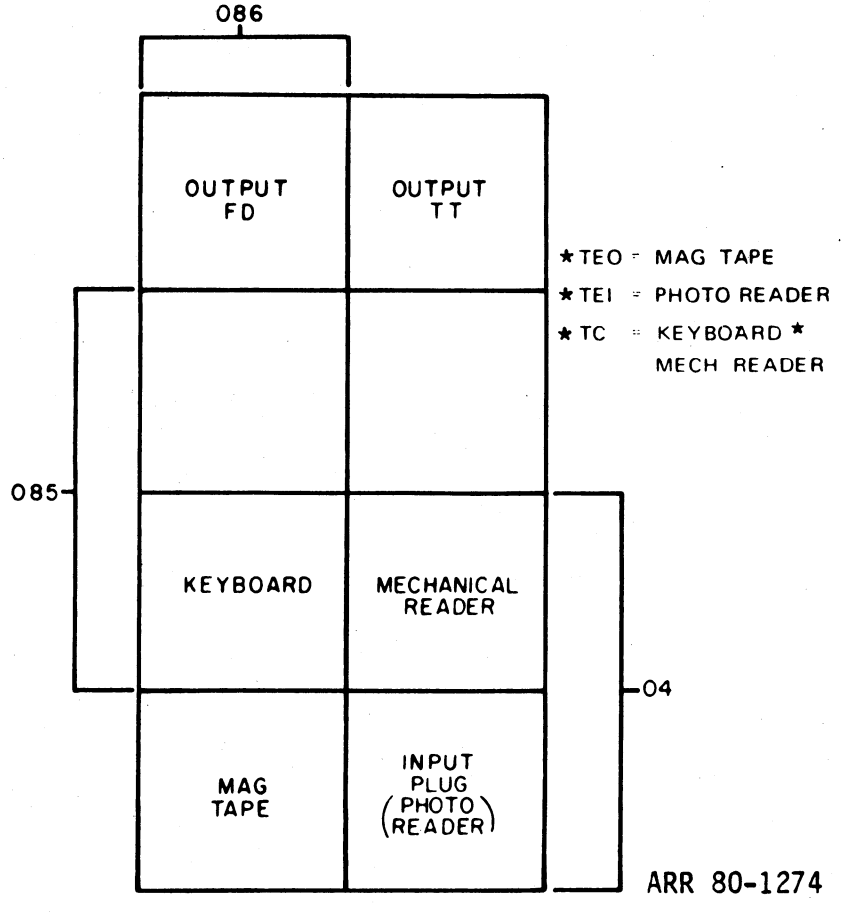


Figure 4-62. Input Device Selection Veitch Diagram.

(2) At times it may be desired to use the keyboard or mechanical reader units to input short routines or other information. These units may be energized under program control, or through external means. When energized externally, the SDR must be connected to the computer or provisions made to simulate the GPRC-, GPHC-, and FBPR signals; see figure 4-52.

b. Energizing of Input Unit.

(1) To energize the mechanical reader or keyboard unit, the SDR is cabled to J017, and the COMPUTE switch on the SDR is placed in the HALT position. Depression of command switches RECALL or SET UP on the FADAC front panel will energize set up lines SU1 and SU2 (fig. 4-30). This action will one set OB5:

1 OB5 = /KD1/ *SU2

(2) Flip-flops OB6 and 04 will not change; figure 4-62 shows the mechanical reader as the selected device. Depression of the START FADAC button on the SDR will complete the logic requirements necessary to energize the mechanical reader, and the IN-OUT indicator. See subparagraph c that follows for detailed discussion of the mechanical reader. Depression of the TRIG or RECEIVE switches on the FADAC front panel will energize the SU2 and SU3 set up lines (fig. 4-30). These terms true will:

1 OB5 = (KD1) *SU2
1 OB6 = (KD1) *SU3

(3) Flip-flop 04 will remain one set; figure 4-62 shows the keyboard as the selected device. Depression of the START FADAC button on the SDR will provide logic necessary to allow keying of data through the keyboard. See paragraph d below for detailed discussion of the keyboard.

c. Mechanical Reader as an Input Device.

(1) The mechanical reader is a plug-in type tape reader using a rotary solenoid as a driving force for tape feed. In the Soroban-manufactured tape reader, reading contacts close during the solenoid energizing stroke and remain closed until the solenoid is deenergized. Tape advance occurs during the solenoid deenergizing stroke. The following logic requirements must be met:

*MRL	OB4	OB2-	/KOPC/
OB5	OB6-	04	

(2) The control and stepping of the solenoid is provided by flip-flops OB4, OB3, and OB2. To energize the solenoid the computer must be in the input-output mode, and is accomplished by the following:

(a) After turnon, the computer will go from the program halt mode to the manual halt mode when the SDR is connected to J017:

Ø E = GRP- (KED3) AK-

(b) Depression of the RECALL switch on the FADAC front panel will one set OB5 and zero set OB2:

1 OB5 = /KD1/ SU2
Ø OB2 = /KD1/ SU1

See figure 4-30 for generation of SU terms.

4-56. INPUT DEVICE SELECTION--Continued

(c) Depression of the START FADAC button on the SDR will one set CP6:

$$1\ CP6 = /KD1/\ (EAKO)\ *FB\ /TPA/$$

(d) Flip-flops E and D will:

$$1\ E = /KD1/\ (EAKO)\ CP6$$
$$\emptyset\ D = /KD1/\ (EAKO)\ CP6$$

(3) The computer is now in the input-output setup mode and will go to the input-output mode after the L register counter completes a 17-word count. Refer to paragraph 4-53 for an explanation of the L register as counter. Once in the input-output mode the logic driver /KOPC/ will be true (-6 volts).

$$/KOPC/ = K- E- D- AK PS-$$

Figure 4-63 shows the logic and circuitry necessary to energize the mechanical reader drive solenoid.

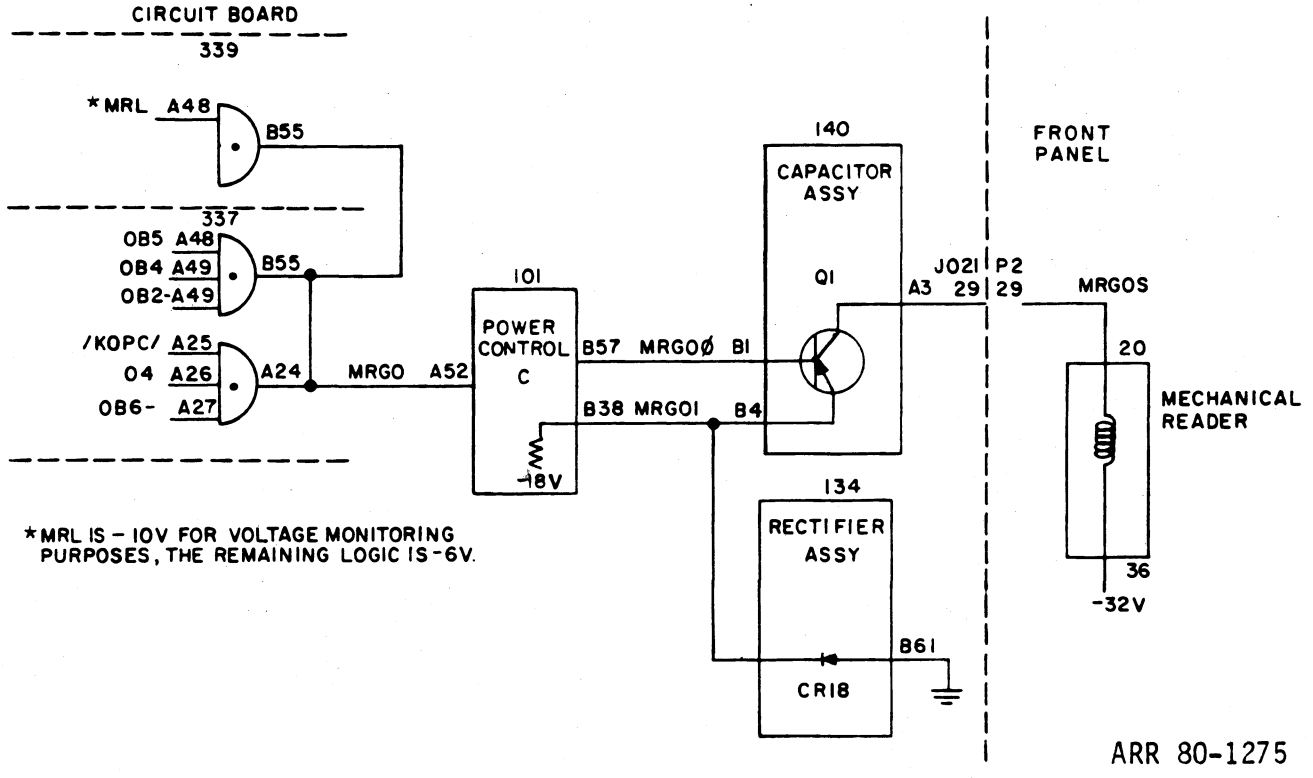


Figure 4-63. Mechanical Reader Logic.

(4) The term MRL is true when the tape is properly positioned in the mechanical reader. Flip-flops 04, 0B6, and 0B4 were set in the required states at computer turnon. Flip-flops 0B5 and 0B2 were set in the required states by the RECALL switch. With MRGO in a true state (-6 volts), the switch amplifier circuit on the power control C board will turn on Q1 on the capacitor assembly board and energize the solenoid in the mechanical reader (refer to section VII and reference appropriate schematic). Figure 4-64 shows the makeup and the logical terms generated by the mechanical reader.

(5) The following describes the terms corresponding to the mechanical reader connector pins.

(a) MRL. With a piece of tape under the tape contact arm and wheel, switch S12 will close and provide a true output of -10 volts.

(b) TC. This term is true (-10 volts) when switch S9 is energized through solenoid advancement.

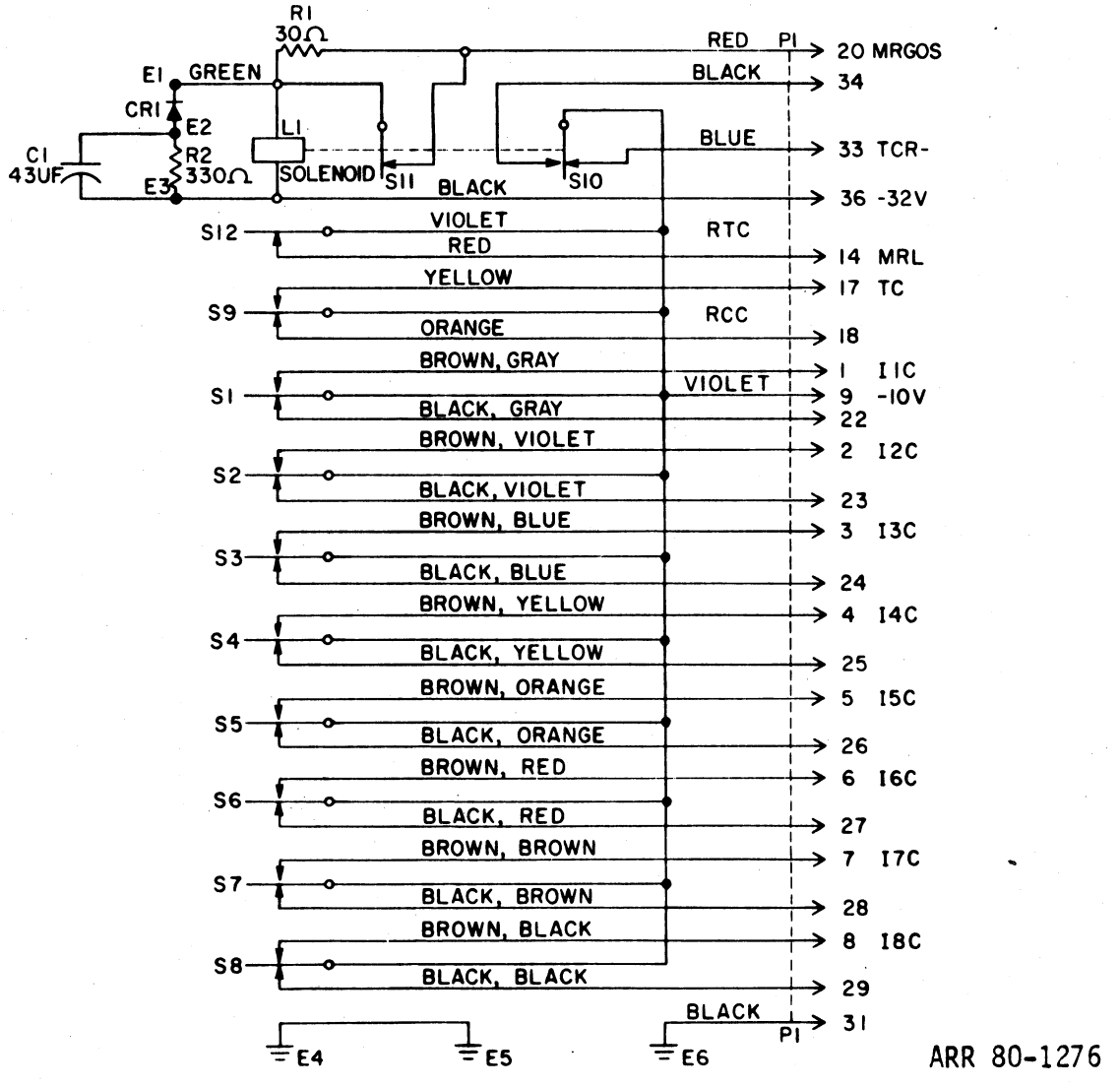


Figure 4-64. Mechanical Reader Diagram.

4-56. INPUT DEVICE SELECTION--Continued

(c) MRGOS. An output from a switching circuit resulting from logic necessary to energize the mechanical reader.

(d) TCR-. This term is controlled by S10 and will be false (0 volts) during the reading of a hole in the tape. When the mechanical reader solenoid deenergizes, this term is true (-10 volts).

(e) -32V. Solenoid energizing voltage.

(f) -10V. Logic voltage.

(6) When the START FADAC button on the SDR is depressed, the mechanical reader will energize and read the I-lines on the tape. The I-lines are true (-10 volts) during the solenoid advance. At the same time the term TC will be true (-10 volts) and cause flip-flop OB4 to zero set:

Ø OB4 = *TC (OWT)

(7) Figure 4-63 shows that OB4 must be one set to allow energizing of the solenoid. With OB4 zero set, O1 on the capacitor assembly board will cut off, causing the solenoid to deenergize. The TCR- term will now be true at -10 volts and cause OB2 to one set and OB3 to zero set:

1 OB2 = *TC- OB5 O4 /KIOS/
Ø OB3 = *TC- OB5 O4 (OWT)

(8) To reenergize the mechanical reader solenoid, flip-flops OB4 and OB3 must one set and OB2 must zero set. The OB3 flip-flop will one set after 16-word agreement or disagreement:

1 OB3 = (OSHB) O5- (O4X) (agreement)
+ (OSHA) O5 /TRS/ (BL6)(disagreement)

(9) After 16-word agreement or disagreement has been determined, flip-flops O5 and OB2 will zero set:

Ø O5 = (KEO) OB3 PP- /TPA/
Ø OB2 = /O4A/ /TXA/ (OSHB) O5-

(10) The logic necessary to energize the mechanical reader solenoid is again present and will allow the solenoid to advance the tape to the next character where the above action will resume.

d. Keyboard as an Input Device.

(1) The FADAC keyboard provides a manual means for entering information into the computer. The keyboard consists of 17 keys, 15 of which provide a field data code output. The remaining two are set up switches. When the computer is in the keyboard entry mode, depression of the key sets up the field data code on the I-lines controlled by the particular key that has been depressed. Inputting through the keyboard unit follows much the same scheme as with the

mechanical reader. The keyboard unit can be program controlled or externally controlled. With the SDR connected to J017, the computer will go to the manual halt mode. To energize the keyboard, the RECEIVE switch on the FADAC control panel is depressed. See figure 4-30 for generation of SU terms. This will cause flip-flops OB5 and OB6 to one set and OB2 to zero set.

1 OB6 = /KD1/ SU3
1 OB5 = /KD1/ SU2
Ø OB2 = /KD1/ SU1

(2) Depression of the START FADAC button on the SDR will one set the CP6 flip-flop causing flip-flop E to one set and D to zero set.

1 CP6 = /KD1/ (EAKØ) *FB /TPA/
1 E = /KD1/ (EAKØ) CP6
Ø D = /KD1/ (EAKØ) CP6

(3) The computer is now in the input-output setup mode and will go to input-output after the L register counter completes a 17-word count. Refer to paragraph 4-53 for an explanation of the L register as a counter. Once in input-output mode, logic driver /KOPC/ is true (-6 volts). Depression of the START FADAC button also energizes the keyboard and IN/OUT indicator on the front panel. See figure 4-47 for the IN-OUT indicator schematic, and figure 4-65 for the keyboard lamp circuit.

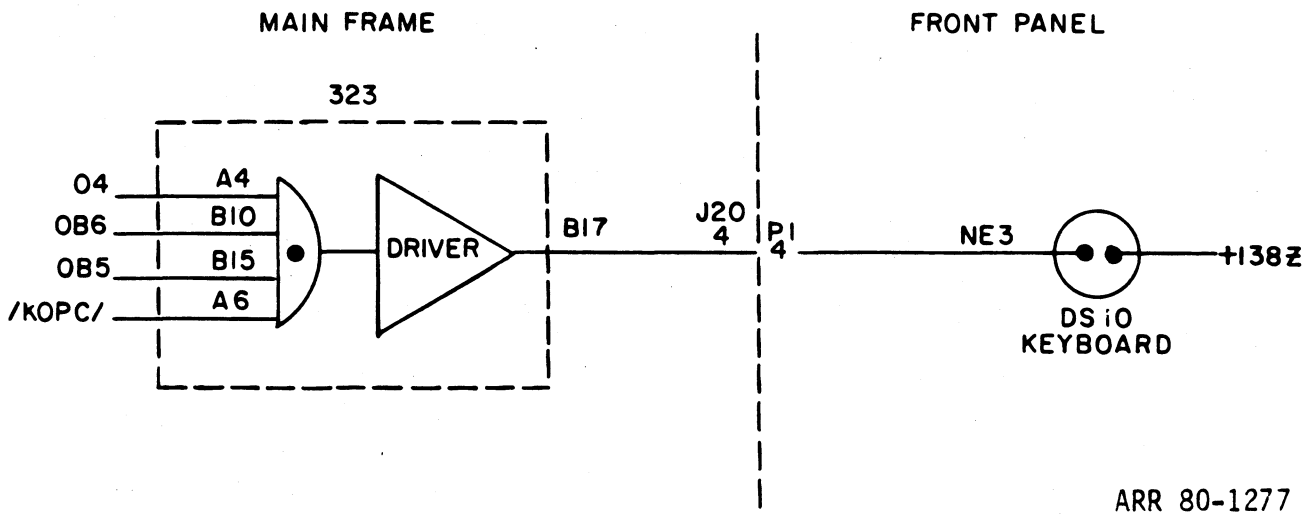


Figure 4-65. Keyboard Lamp Circuit.

4-56. INPUT DEVICE SELECTION--Continued

(4) The keyboard is enabled through the term KGOS. Figure 4-66 shows the logical and electrical makeup of this term. The term KGOS is "anded" with keyboard I-line terms to generate I-line information to the input register (D1 thru D8). (See table 4-24 for keyboard coding.) The input register flip-flops (D1 thru D8) are set by the following logic when the mechanical reader or keyboard is used:

1 D1 = I1C OB2-
1 D8 = I8C OB2-

NOTE

X indicates a true condition. The SM and RECALL keys generate SU line terms.

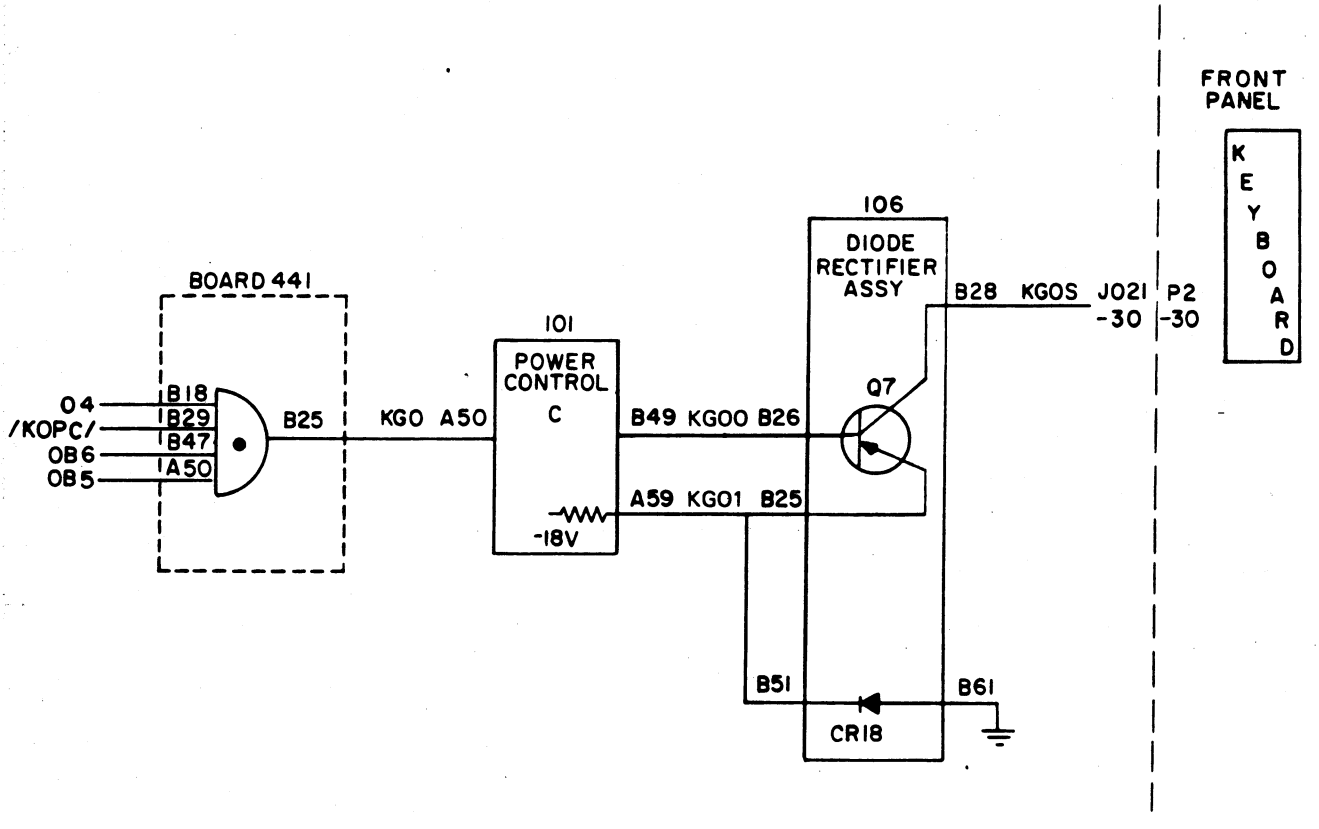


Figure 4-66. Keyboard Logic Diagram.

Table 4-24. Keyboard Coding

Key function	I8	I7	I6	I5	I4	I3	I2	I1
0			X	X				
1	X		X	X				X
2	X		X	X			X	
3			X	X			X	X
4	X		X	X		X		
5			X	X		X		X
6			X	X		X	X	
7	X		X	X		X	X	X
8	X		X	X	X			
9			X	X	X			X
Left Down Drop			X					X
Right Up Add			X				X	
Decimal Point (.)	X		X	X	X	X		X
CLEAR	X	X		X	X	X		X
ENTER		X				X		

(5) On input by character, which is the case when using the keyboard, the flow of information is from the input register into the A register; then from A register to the N register. The Q loop and R loop are not used during character input. Figure 4-67 shows the terms and voltages used with the keyboard unit.

(6) The following is a description of the terms corresponding to the keyboard connector pins:

4-56. INPUT DEVICE SELECTION--Continued

(a) TC. This term will be true just after a key is depressed on the keyboard. It will remain true for approximately 25 milliseconds after the key is depressed, then turn false.

(b) TCK-. This term will be false approximately 5 milliseconds before TC is true, for the duration of TC and 5 milliseconds after TC turns false. At any other time TCK- is true.

(c) I1C thru I8C. Information line outputs from keyboard circuits.

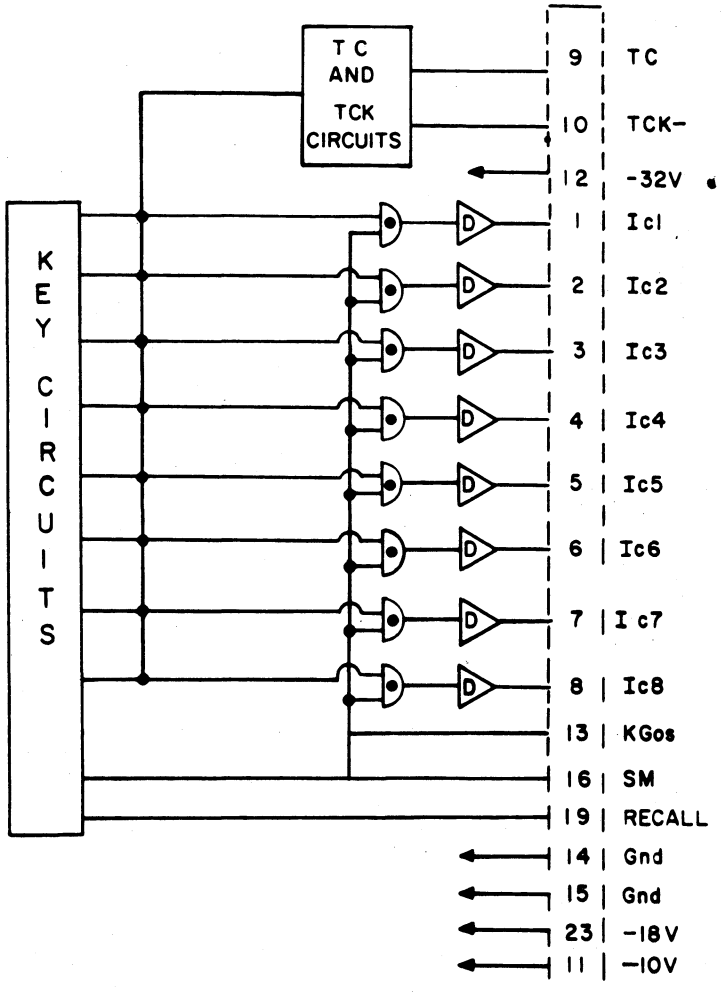


Figure 4-67. Keyboard Unit Diagram.

NOTE

The wave shapes in figure 4-68 represent the timing sequence of the above signals.

(d) KGOS. The keyboard enable term. This term is controlled by logic generated by a programmed instruction or an external device.

(e) SM. A set up switch not associated with keyboard logic.

(f) RECALL. Same as SM key.

(g) -32V. Keying circuits voltage.

(h) -18V. Reference and driver voltage.

(i) -10V. Logic voltage.

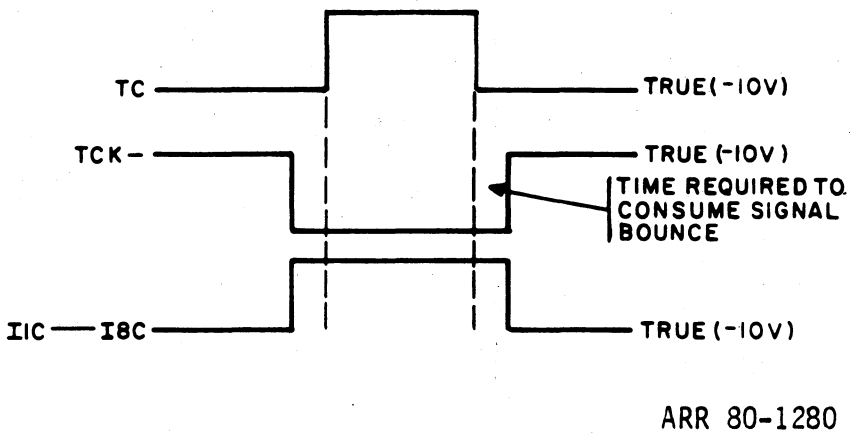


Figure 4-68. TC, TCK-, and I1C to I8C Wave Shapes.

e. Matrix Unit as Input Device.

(1) The matrix unit consists of 64 indicating windows, each illuminated by a lamp module containing a single removable lamp in series with a single removable diode. The lamp module lights when two associated matrix selection switches are depressed. Additionally, a logic term is generated corresponding to a program parameter. Figure 4-69 shows the makeup of the matrix unit.

(2) Terms with an F-line designation are generated through the depression of the switches and are so shown in table 4-25.

4-56. INPUT DEVICE SELECTION--Continued

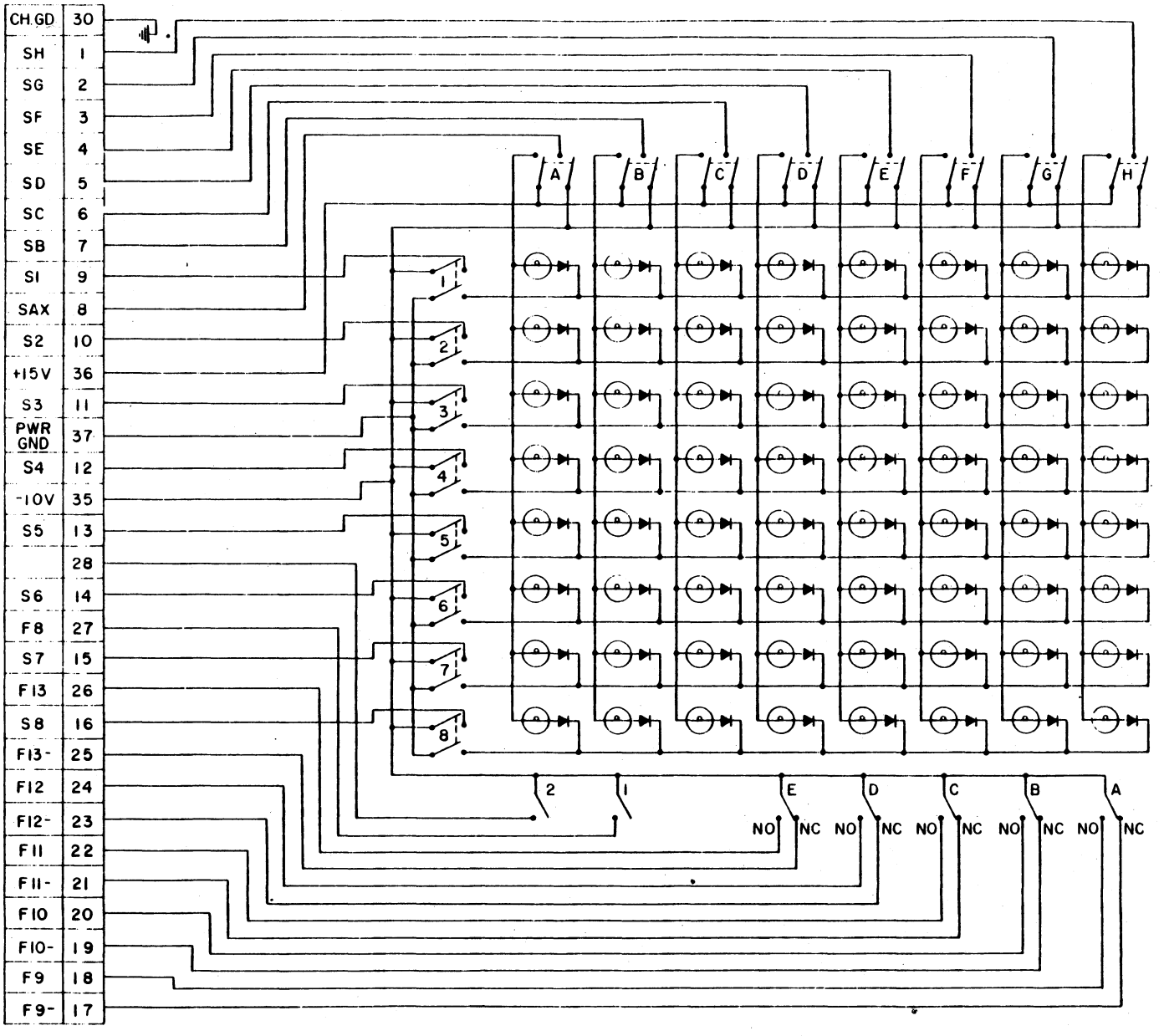


Figure 4-69. Matrix Unit Diagram.

Table 4-25. F-Line Versus Switch Selector

Switch	Terms	Switch	Terms
A	F1	1	F1
B	F1 F5	2	F1
C	F1 F6	3	F1 F3
D	F1 F5 F6	4	F1 F2 F3
E	F1 F7	5	F1 F4
F	F1 F5 F7	6	F1 F2 F4
G	F1 F6 F7	7	F1 F3 F4
H	F1 F5 F6 F7	8	F1 F2 F3 F4
Weapon 1 or 2	F8		
Battery A	F9		
Battery B	F10		
Battery C	F11		
Battery D	F12		
Battery E	F13		

f. Input Cable. The cable connected to J17 is the input cable to the computer from the SDR. This cable and associated logic pertinent to input are shown in figure 4-52.

4-57. TROUBLESHOOTING DURING INPUT

a. Table 4-26 shows some tests that may be conducted to check input operation.

b. During input through the keyboard, the A, L, and N register contents may be monitored using an oscilloscope. Utilization of an improvised template made according to figure 4-70 and placed over the face of the oscilloscope will allow observation of the bits of input data being processed through the A, L, and N registers. Using a dual trace oscilloscope trigger with the output of the TP flip-flop and use TX as the reference for a word length. The TP flip-flop can be obtained at J016 pin C. TX (/TXC/) can be obtained at J015 pin KK. See figure 4-70 for TP pattern.

4-57. TROUBLESHOOTING DURING INPUT--Continued

Table 4-26. Input Operation Testing Chart

Condition	Circuit	Test
The computer is in program halt mode (POWER READY indicator is lit).	Flip-flops AK, K, 02, 03, 05, OB5, and CP6.	Zero set
	Flip-flops D, E*, 04, OB2, OB3, and OB4.	One set
Input through the mechanical reader.	Control logic and circuits.	Refer to figures 4-63 and 4-64 for voltage monitoring points.
	Mechanical reader switch contacts.	Figure 4-64 shows the connector pins of the mechanical reader. Manual advancement of the solenoid will allow ohmmeter monitoring of logic and I-lines switch contacts.
Input through the keyboard.	Control logic and circuits.	Refer to figures 4-66 and 4-67 for voltage monitoring.
	Output logic and circuits.	Rapid successive depressions of the keyboard keys will allow voltage monitoring of the I-lines and control logic at the input of D1 thru D8, OB2, OB3, and OB4 flip-flops.

*Flip-flop E will be zero set if the computer is in manual halt mode.

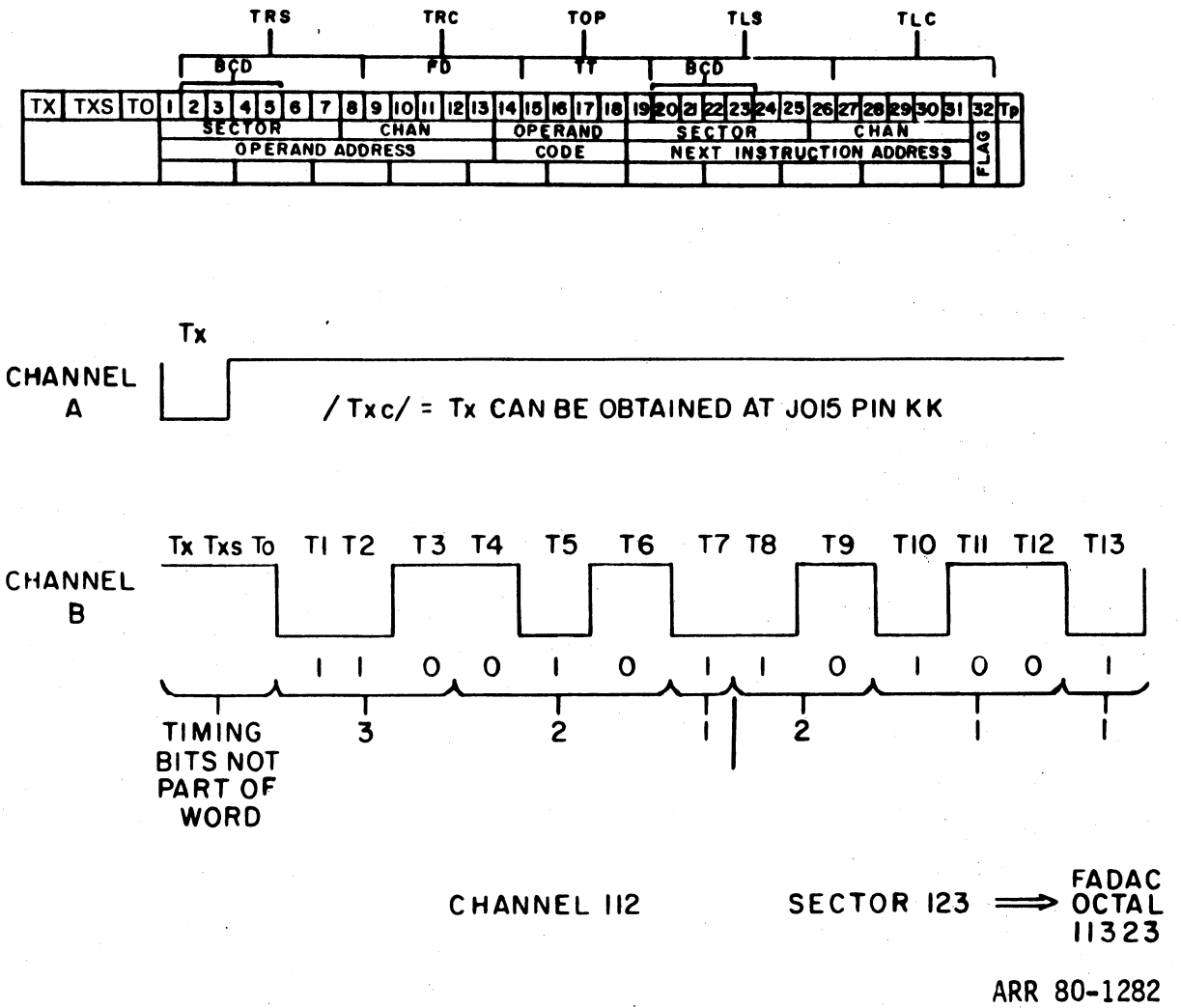


Figure 4-70. Oscilloscope Template and Patterns.

NOTE
Computer word format is detailed in paragraph 4-62.

c. Figure 4-70 also shows the oscilloscope presentation when monitoring AP flip-flop at board 320 pin B28. Channel A of the oscilloscope displays the TX bit and can be obtained at J015 pin KK. Keying in of the address 11323 is shown in binary form, as monitored using channel B of the oscilloscope in figure 4-70. Depression of the decimal point (.) key on the keyboard will transfer this address from the A register to the L register and can be monitored at LP on circuit board 239 pin B28.

d. Troubleshooting of the matrix unit can be done using figure 4-69. Table 4-27 provides pin number and corresponding logic term found on the front panel to main frame interconnecting cables.

e. For troubleshooting of the logic, involving the front panel lamps, use figure 4-71.

4-57. TROUBLESHOOTING DURING INPUT--Continued

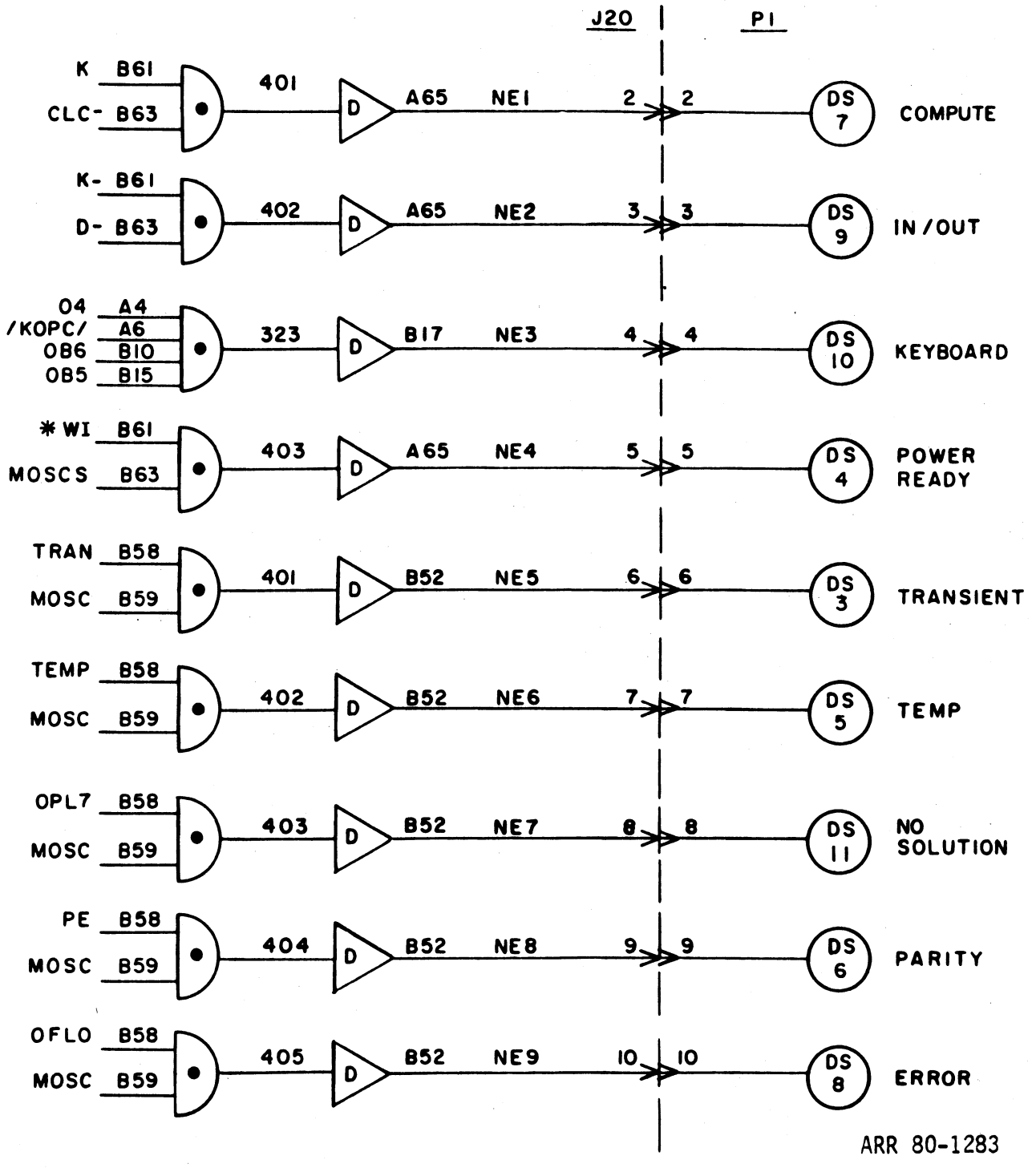


Figure 4-71. Front Panel Logic Diagram.

Table 4-27. Front Panel to Main Frame Wiring

Pin	J018 to P5	J019 to P6	J020 to P1	J021 to P2
1	Pwr Gnd	CD1	138Z	Spare wires
2	AD1	CD2	NE1	Mechanical reader
3	AD2	CD3	NE2	
4	AD3	CD4	NE3	-18V
5	AD4	CD10	NE4	Spare wires
6	BAD	CD11	NE5	Keyboard
7	CDA	CD12	NE6	
8	CDB	CD13	NE7	
9	CDC	CD14	NE8	
10	CDD	CD15	NE9	-10VC
11	CDE	CD16	NLC	-10VD
12	CDM	CD17	-6Z	-32VA
13	CDP	CD18	6VAC1	-32VB
14	F8	CD19	6VAC2	SU3
15	F9	CD20	6VAC3	SU3-
16	F9-	CD21	SPARE	Shd Gnd
17	F10	CD22	SPARE	Ch Gnd
18	F10-	CD23	-10VB	I1C
19	F11	CD24	SER	12C
20	F11-	CD25	SU1	I3C
21	F12	CD26	SU1-	I4C

4-57. TROUBLESHOOTING DURING INPUT--Continued

Table 4-27. Front Panel to Main Frame Wiring--Continued

Pin	J018 to P5	J019 to P6	J020 to P1	J021 to P2
22	F12-	CD27	SU2	I5C
23	F13	CD28	SU2-	16C
24	F13-	CD29	SU4	I7C
25	SAX	CD30	SU4-	18C
26	SB	CD31	SU5	TC
27	SC	CD32	SU5-	TCR-
28	SD	CD33	SU6	TCK-
29	SE	CD34	SU6-	MRGOS
30	SF	CD35	SU7	KGOS
31	SG	CD36	SU7-	SUO
32	SH	CD37	Pwr Gnd	SUO-
33	S1	CD38	P Off	Pwr Gnd
34	S2	CD39	N2	
35	S3	CD40	Ph 4A*	
36	S4	CD41	Ch Gnd*	
37	S5	CD42	Shd Gnd	
38	S6	CD43		
39	S7	CD44		
40	S8	CD45		
41	-10VA	CD46		
42	+15V	CD47		
43		CD48		
44		CD49		

Table 4-27. Front Panel to Main Frame Wiring--Continued

Pin	J018 to P5	J019 to P6	J020 to P1	J021 to P2
45				
46				
47				
48	Matrix			
49	Spare Wires	Spare Wires		
50				

*Shielded wires.

4-58. OUTPUT

a. General.

(1) Primary output is to the visual display (nixies) on the front panel. It is also possible to program the output to other external devices. Output information can be either five-level teletype, two-wire teletype, or field data.

(2) Output, like input, is by character or by word. In character output, the A, L, and N registers are used; in word output the A, L, N, R, and Q loops are utilized. Unlike input, output is program-controlled only. The following shows the purpose of the flip-flops utilized during output:

(a) DSP. Controlled by the program instruction for display.

(b) DSH. DSH along with DSP will control the shift of information from the D loop into the display register.

(c) D1 thru D8 and DA1 thru DA8. Display register.

(d) OB6. Output device selection.

(e) OP1 and OP3. Three-bit counter to determine output line to be used. Counts currently used are shown in table 4-28.

(f) X1 and X2. Comprise quadrant counter; sector track controlled.

(g) XD. Display delay.

4-58. OUTPUT--Continued

Table 4-28. Input/Output Count Codes

Count	Location	Purpose	Count	Location	Purpose
1	J010	Two-wire teletype	5	J017	Input device
2	J010	Output device	6	J017	Input device
3	J010	Output device	7	Front panel NO SOLUTION indicator	
4	J017	Input device			

b. Output via Nixie Display.

(1) As mentioned earlier, the primary output is to the nixie display. The nixie display is a programmed visual display in which output information converted to BCD characters, is stored in the two-word D loop and displayed. This display consists of 17 tubes and 16 neon lamps used as decimal points. The sign nixie assembly does not contain a neon lamp. The battery nixie is not part of the D loop, but is wired into display which battery button, A, B, C, D, or E, is depressed on the matrix unit. See figure 4-72 for relationship between D loop and nixie display.

(2) Nixies 2 thru 9 will display the contents of D1 of the D loop, while nixies 10 thru 17 will display the contents of D0 of the D loop. Only the BCD characters shown in table 4-29 may be displayed at positions 2 thru 17.

(3) The flow of information from the D loop to the display register (D1 thru D8, DA1 thru DA8) is shown in figure 4-73. Up to 16 BCD characters can be programmed into the two-word D loop and displayed. The display register can hold only four BCD characters, see figure 4-73.

(4) For this reason the memory disk has been divided into four quadrants. Table 4-31 will show these quadrants appearing at sectors 036, 076, 136, and 176. Four characters are displayed during one quadrant of disk revolution, followed by four more during the next quadrant, and so on until all 16 characters are displayed during one disk revolution. The cycle is repeated under program control. Since the operating frequency of the disk is 100 rps, the display appears to be continuous.

(5) Flip-flops X1 and X2 serve as a counter to determine the quadrant on the memory disk. The loading of the display register will be controlled by DSH and DSP flip-flops. Once the computer has read the display instruction (IDM), flip-flop DSP will one set:

1 DSP = (0X0) C5 (CNL2) C6

With DSP one set, (XCT) will be true when the sector read head senses a zero at TXF time; this occurring at sectors 036, 076, 136, and 176. Table 4-30 (XCT) energizing the quadrant counter (X1 and X2) each time a zero is read from the sector track at TXF time.

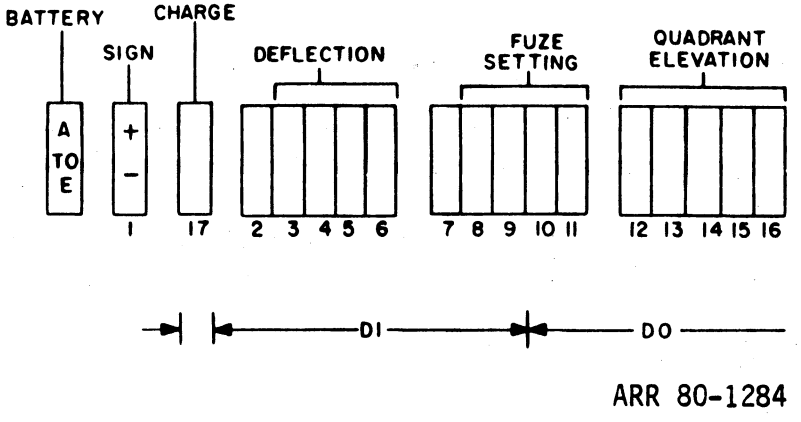


Figure 4-72. Relationship Between D Loop and Nixie Display.

Table 4-29. Binary Coded Decimal Code Versus Digit Displayed

Digit displayed	BCD code	Digit displayed	BCD code
0	0000	B	1000
1	0001	9	1001
2	0010	+	1010*
3	0011	-	1011*
4	0100	Decimal point	1100
5	0101	Blank	1101
6	0110	Blank	1110
7	0111	Blank	1111

*Usable in nixie position 17. However, it shows up as blank in all other nixie positions.

4-58. OUTPUT--Continued

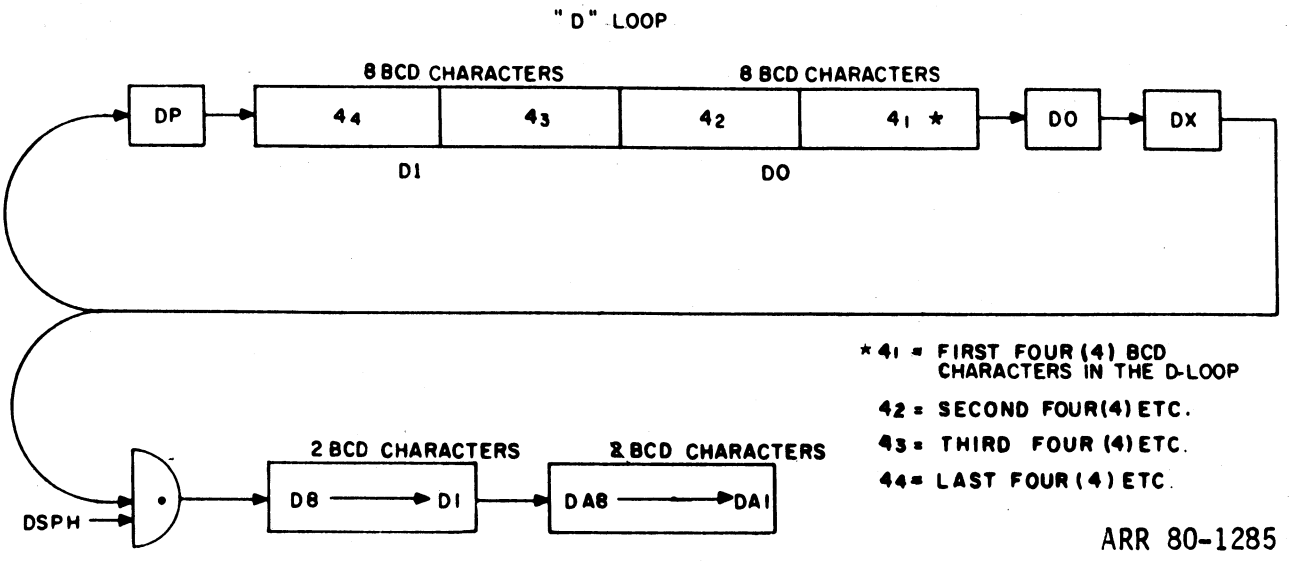


Figure 4-73. D Loop to Display Register Configuration.

(6) In addition to controlling the quadrant counter, (XCT) will one set flip-flop DSH:

$$1\ DSH = (XCT) + X2\ S\text{-}\ TO$$

When DSH is one set, information in the D loop will be loaded into the display register, Table 4-31 shows that four BCD characters are shifted into the display register each quadrant of disk revolution. The D loop, for explanation purposes, is shown as 4_1 and 4_2 (eight BCD characters), and is held in DO. The second word of the D loop, 4_3 and 4_4 (eight BDC characters), is held in D1, (fig. 4-73).

Table 4-30. Quadrant Counter

X2	X1	Count	Logic
0	0	0	1 X1 = X1- (XCT)
0	1	1	1 X2 = X2- X1 (XCT)
1	0	2	Ø X1 = X1 (XCT)
1	1	3	1 X1 - X1- (XCT) Ø X2 = X2 X1 (XCT)
0	0	0	Ø X1 = X1 (XCT)

Table 4-31. Loading Operation of Display Register D Loop

Display register contents	Quadrant counter*	Sector track location	Remarks
-01 1 DSH = (XCT)	X2- X1-	036	First 16 bits (D0) of the D loop are loaded into the display register and displayed.
-00**		037	No action.
-02 1 DSH = (XCT)	X2- X1-	076	The second 16 bits of the D loop are shifted in the display register and displayed.
-02**		077	No action.
-01 1 DSH = (XCT) Ø DSH = X1- /TOP/ (BL1)	X2 X1-	136	The first 16 bits (D1) of the D loop are shifted into the display register, but not displayed. This is due to the display register reloading one word time later (137), preventing display.
-03** 1 DSH = X2 S- TO Ø DSH = X1- /TOP/ (BL1)		137	The third 16 bits, which are held in D1, are shifted into the display register and displayed.
-02 1 DSH = (XCT) Ø DSH = /T32/	X2 X1	176	All of D1 is loaded into the display register, but not displayed. This is due to the display register reloading during sector 177.
-04** 1 DSH = X2 S- TO Ø DSH = /T32/		177	The last 16 bits of D1 will be held in the display register and displayed.

*See table 4-30 for logic.

**Indicates the portion of the D loop that is held in the display register during this quadrant.

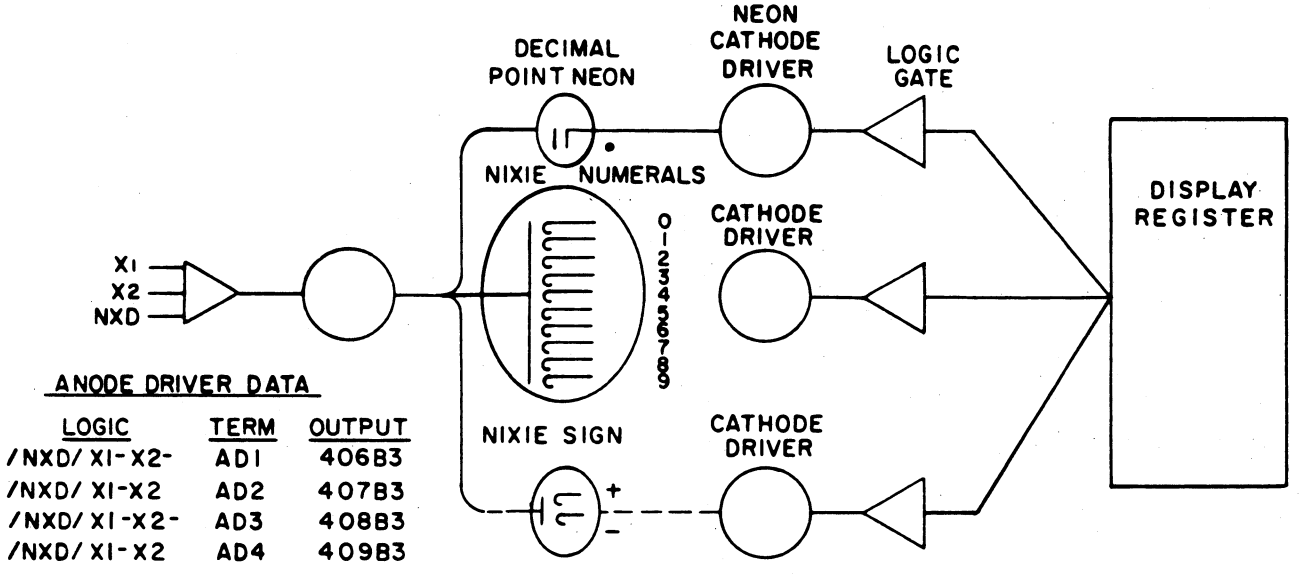
4-58. OUTPUT--Continued

(7) The display register will copy the DX flip-flop during the time that DSP and DSH are one set. The display register will copy the D loop serially:

1 D8 = DX (DSPH)
Ø D8 = DX- (DSPH)
1 D7 = D8 (DSPH)
Ø D7 = D8- (DSPH)
1 DA1 = DA2 (DSPX)
Ø DA1 = DA2 (DSPX)

(8) Figure 4-74 shows that the output of the display register together with anode driver output AD1, AD2, AD3, or AD4 will allow energizing of a nixie numeral, nixie sign, or a neon decimal point.

(9) During memory disk rotation, anode driver 1 (AD1) will be true from sectors 036 thru 076, and will allow energizing of the SIGN or CHARGE nixie and nixies in plugs 17, 18, and 15. AD2 will be true between sectors 077 and 136 and allow nixies in plugs 12, 13, 14, and 16 to energize; AD3 will be true between sectors 137 and 176 and allow nixies in plugs 9, 10, 7, and 11 to energize; AD4 will be true between sectors 177 and 036 and allow nixies in plugs 4, 5, 6, and 8 to energize (fig. 4-75).



ANODE DRIVER DATA

LOGIC	TERM	OUTPUT
/NXD/ X1-X2-	AD1	406B3
/NXD/ X1-X2	AD2	407B3
/NXD/ X1-X2-	AD3	408B3
/NXD/ X1-X2	AD4	409B3

DECIMAL POINT DATA

LOGIC	TERM	OUTPUT
SEE TABLE 4-29 FOR BCD CODE	CD1D	406B23
	CD2D	407B23
	CD3D	408B23
	CD4D	409B23

SIGN DATA

SIGN	LOGIC	TERM	OUTPUT
+		CDP	406A54
		CDM	407A54

ARR 80-1286

Figure 4-74. Nixie Driver Interconnection.

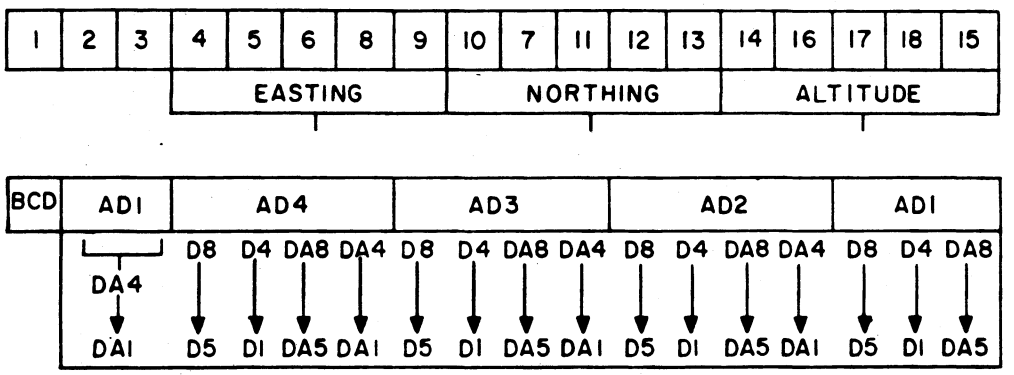
(10) The following is an example of the numeral 8 being illuminated in nixie plug 10:

NOTE
Refer to figure 4-75 during text discussion.

(a) Nixie plug 10 anode is energized when AD3 is true. The cathode of the tube is controlled by a cathode driver which in this case will be CD48. The CD output is a result of inputs from the display register. Figure 4-75 shows D8 to D5 flip-flops containing the numeral for nixie plug 12. The numeral 8 is represented through:

D8 D7- D6- D5

(b) Reference to the matrix decoder in TM 9-1220-221-34/1/1 shows CD48 at 409A24 and AD3 output at 408B3. With the anode energized through AD3 and the cathode through CD48, the numeral 8 in the nixie tube will be illuminated.



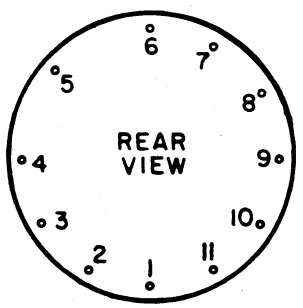
CD10 SERIES = DA4 DA3 DA2 DA1 BOARD 406

CD20 SERIES = DA8 DA7 DA6 DA5 BOARD 407

CD30 SERIES = D4 D3 D2 D1 BOARD 408

CD40 SERIES = D8 D7 D6 D5 BOARD 409

NUMERAL TUBE		SIGN TUBE	
PIN	ELEMENT	PIN	ELEMENT
1	1	1	NO CONNECTION
2	2	2	C
3	3	3	B
4	4	4	"–"
5	5	5	E
6	6	6	+
7	7	7	NO CONNECTION
8	8	8	A
9	9	9	NO CONNECTION
10	0	10	D
11	ANODE	11	ANODE



NIXIE TUBE PINS

ARR 80-1287

Figure 4-75. Anode and Cathode Selection.

4-58. OUTPUT--Continued

(11) The battery nixie is controlled by the battery switches on the matrix unit and term BDX. The terms associated with battery selection are shown in table 4-32.

Table 4-32. Battery Selection Terms

Battery switch	Term	Logic	Output
A	CDA	*F9 (BDX)	406A52
B	CDB	F10 (BDX)	407A52
C	CDC	F11 (BDX)	408A52
D	CDD	F12 (BDX)	409A52
E	CD3	F13 (BDX)	408A54

*F terms are from the battery switches.

c. Output to Teletypewriter.

(1) Output to a teletypewriter is performed through the use of the output device stepping -1 command. This command has a code of 36 102; changing of the code energizes the output driver term OPL10 found on J010 pin X. Figure 4-76 shows the logic configuration when using a teletypewriter as an output device.

(2) The output of the teletype oscillator on network C is a 22-millisecond square wave, alternating true and false every 11 milliseconds. During the true period and TLC (timing left channel), flip-flop C7 will one set:

1 C7 = *F32 (TLC) (BL6) /OX/

(3) When C7 is one set, primary "and" gate (OXO) will be true each TO time. This term, with C5- and C2 true, will allow OP1 to one set:

1 OP1 = C2 (OXO) C5-

(4) OP1, OP2, and OP3 flip-flops were zero set at turnon:

Ø OP1 = *TD
Ø OP2 = *TD
Ø OP3 = *TD

(5) If OP2 and OP3 are one set as the result of another operation the following would zero set both flip-flops:

$$\emptyset \text{ OP2} = \text{C3-} (\text{OXO}) \text{ C5-}$$
$$\emptyset \text{ OP3} = \text{C4-} (\text{OXO}) \text{ C5-}$$

(6) The primary "and" gate (OPL1) is fed to a driver circuit on network A and output at J010X as OPL10. By turning (OPL1) on and off through program control, a train of pulses representing the various characters is fed to the teletypewriter for printout.

NOTE

For a dynamic test of the teletype output capability of the computer, use the teletype output test tape routine. Refer to TM 9-1220-221-34/8 for operation and maintenance procedure.

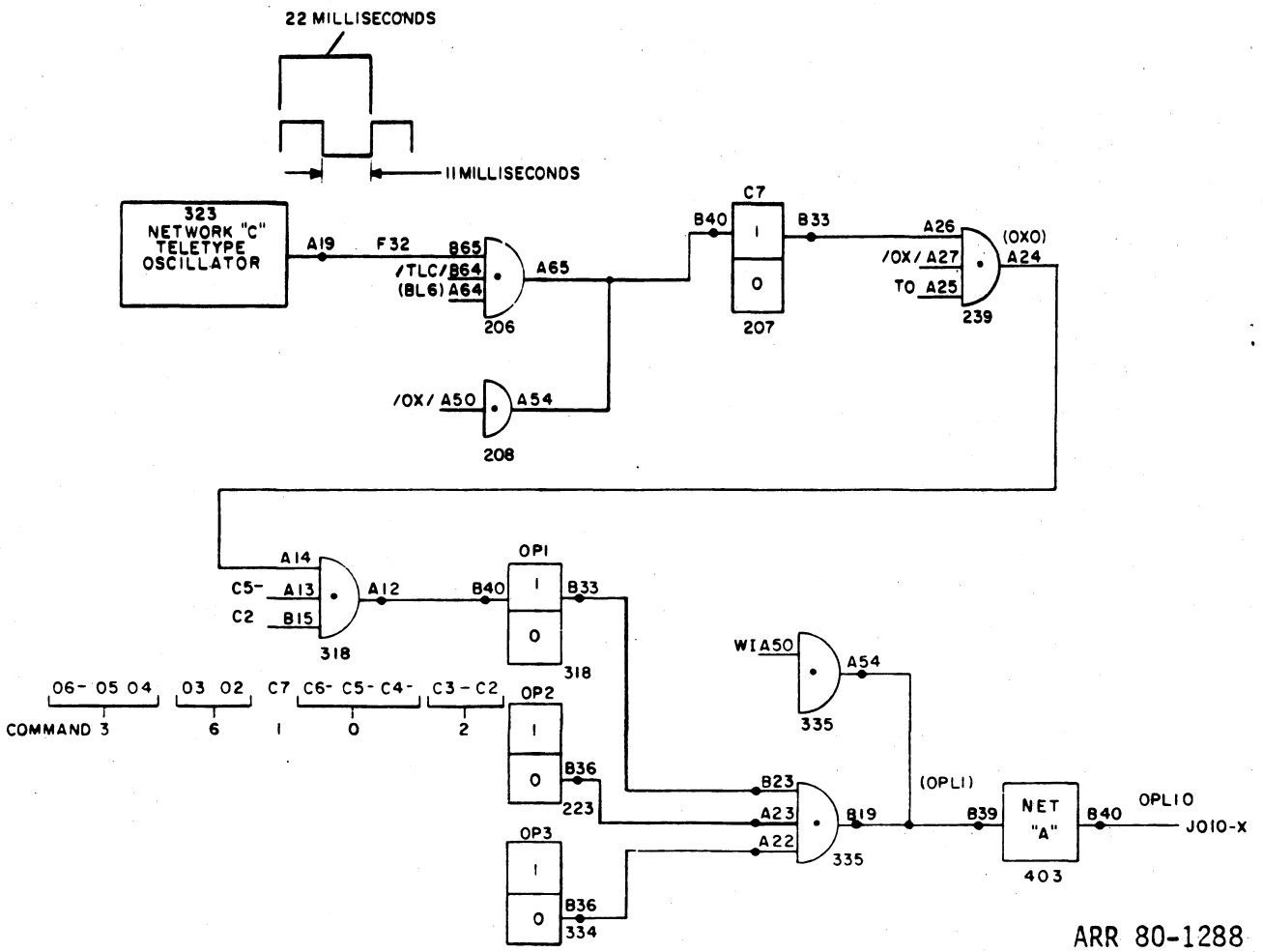


Figure 4-76. Output to the Teletypewriter.

4-59. FUTURE OUTPUT DEVICES

Figure 4-77 illustrates the output connector J010 and figure 4-78 illustrates output connector J016. These two illustrations indicate other inputs and outputs that may be used in future input-output devices used in conjunction with the computer.

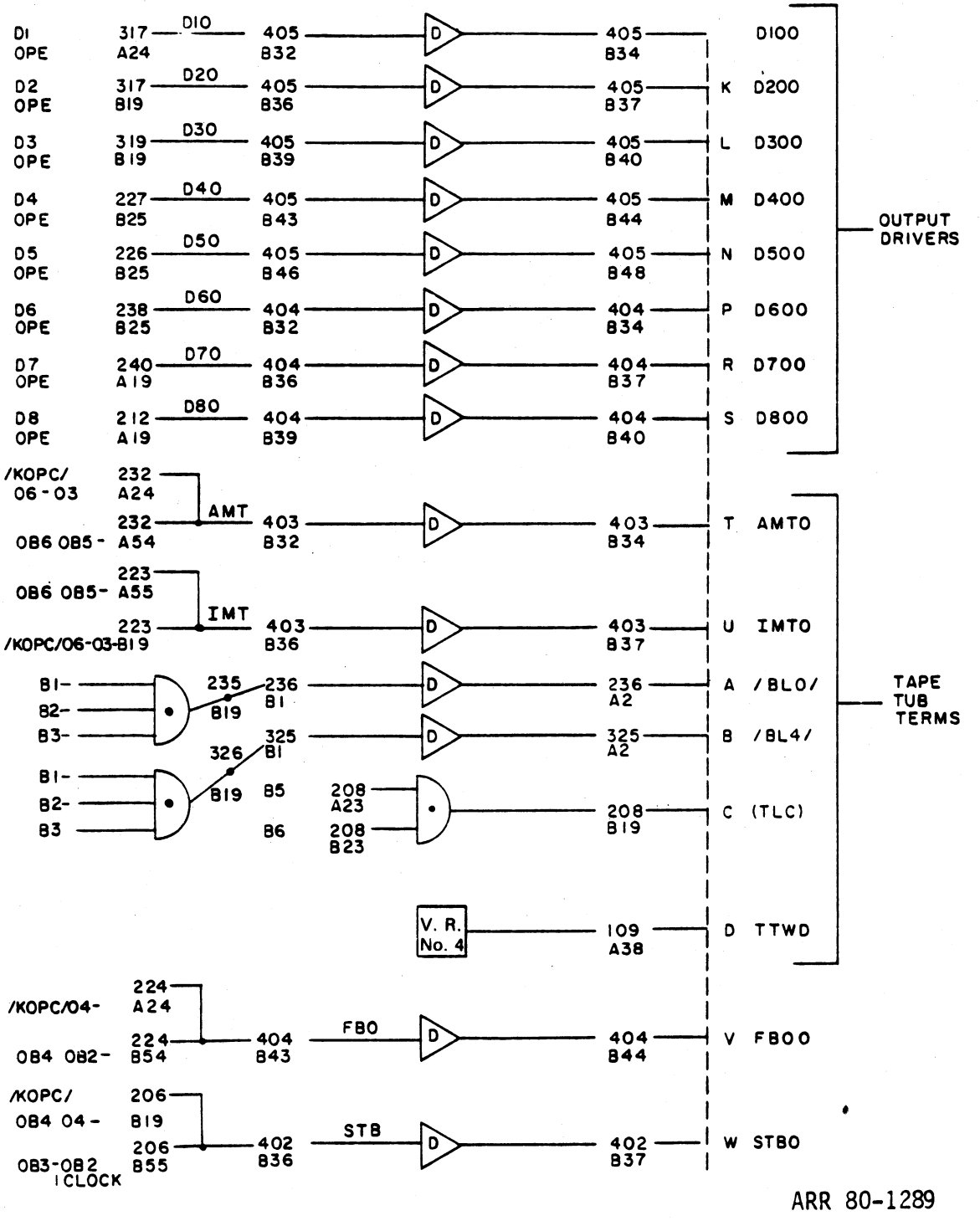


Figure 4-77. Output Connector J010 (sheet 1 of 3).

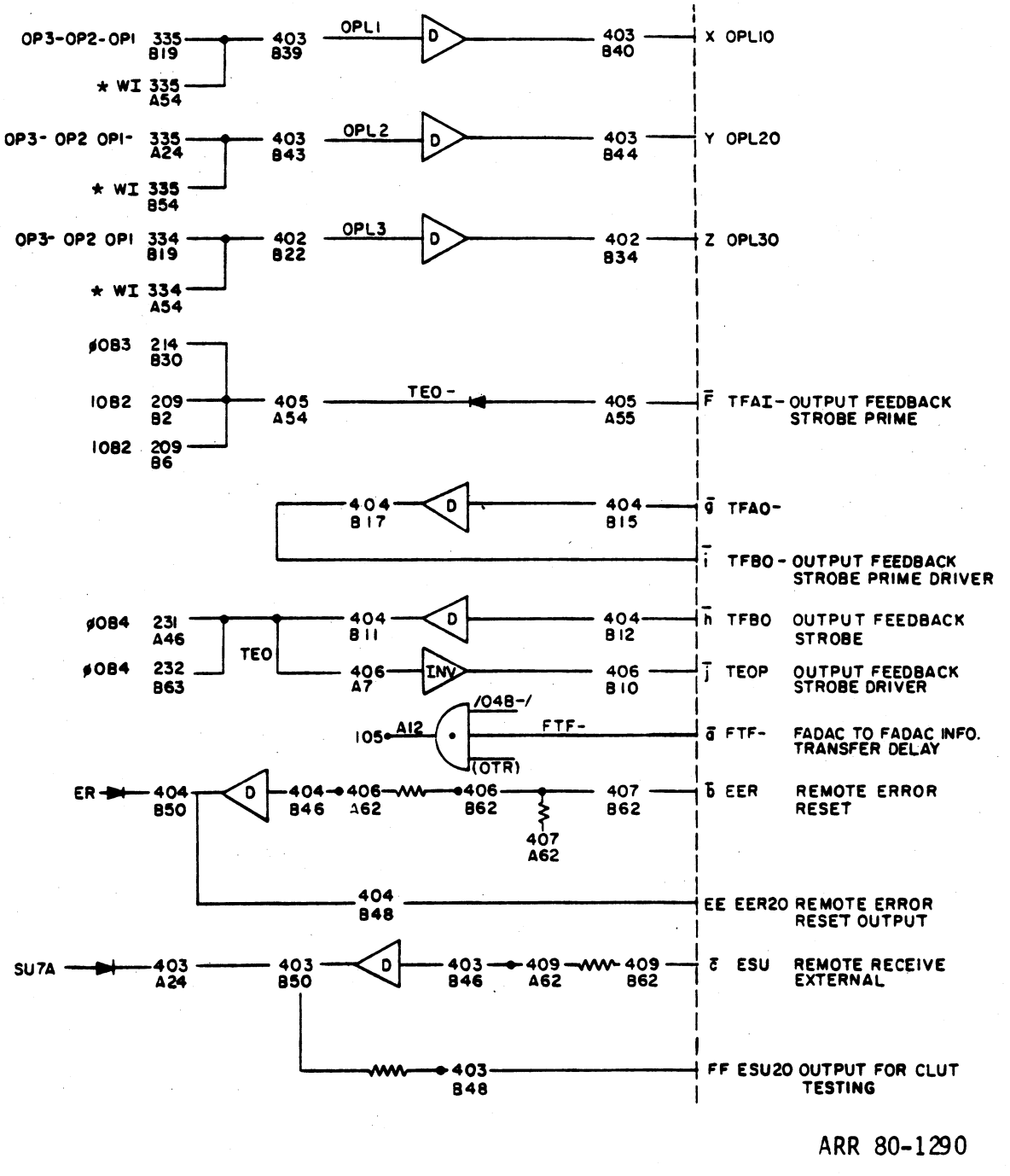


Figure 4-77. Output Connector J010 (sheet 2 of 3).

4-59. FUTURE OUTPUT DEVICES--Continued

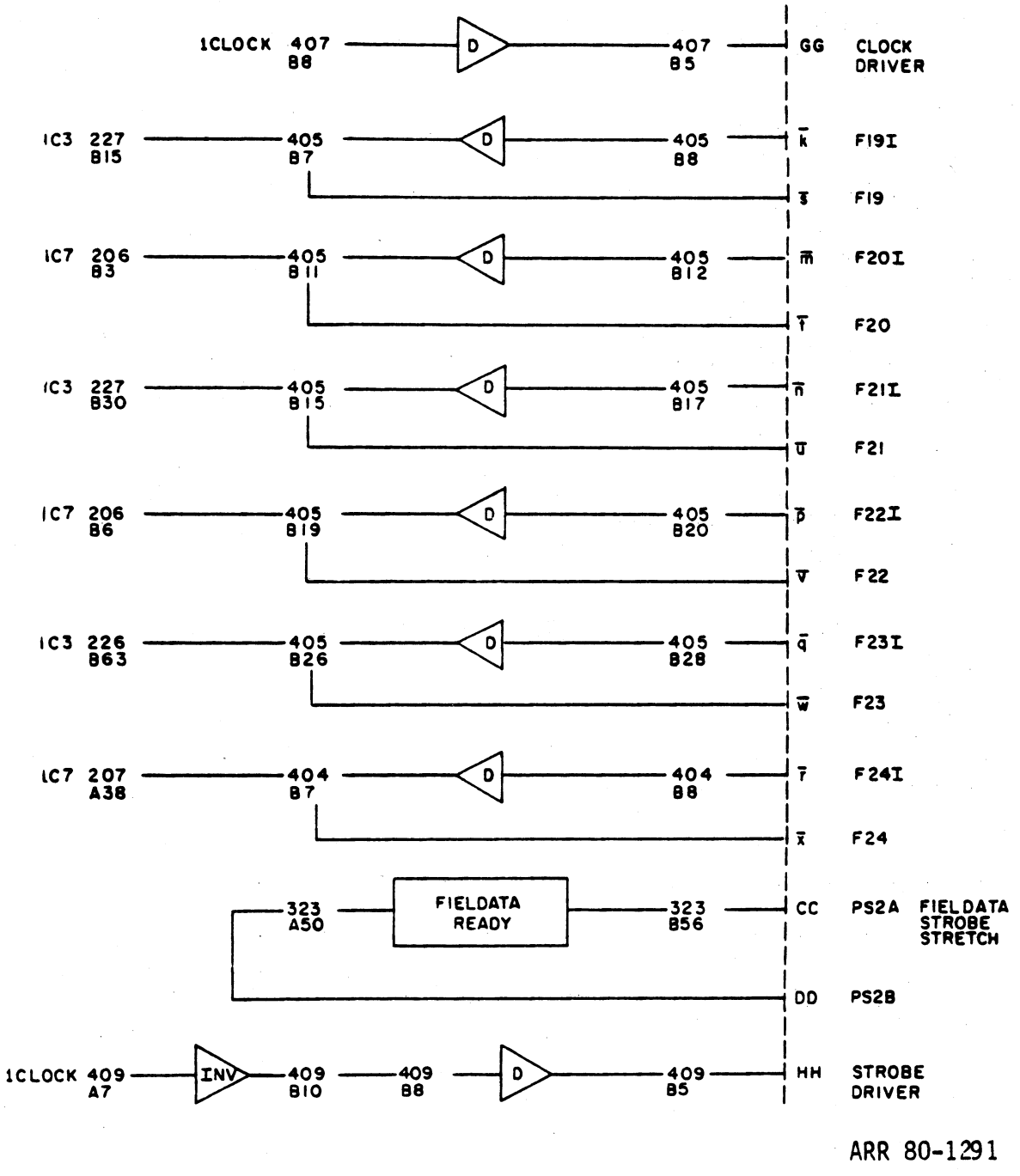


Figure 4-77. Output Connector J010 (sheet 3 of 3).

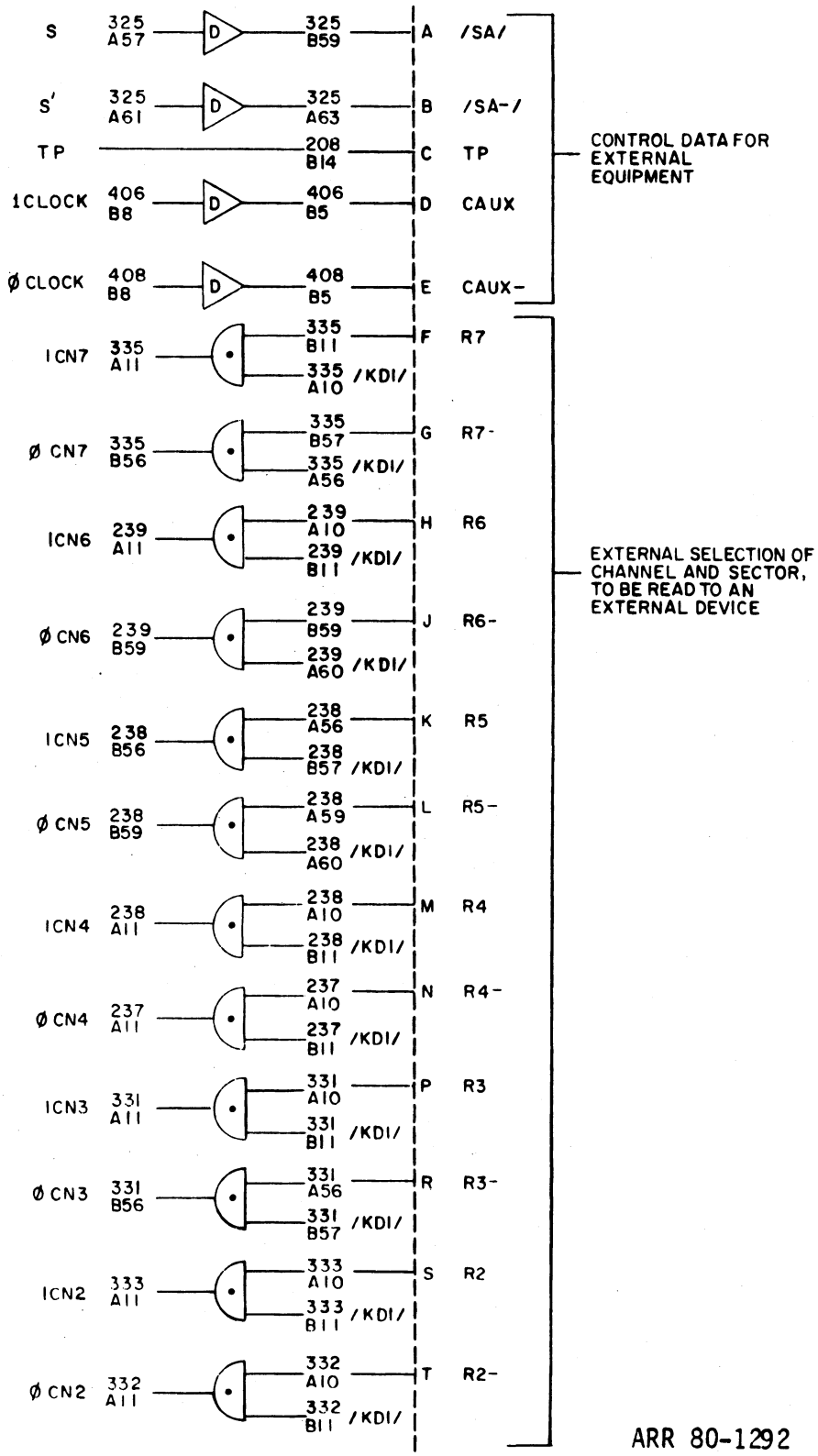


Figure 4-78. Output Connector J016 (sheet 1 of 2).

4-59. FUTURE OUTPUT DEVICES--Continued

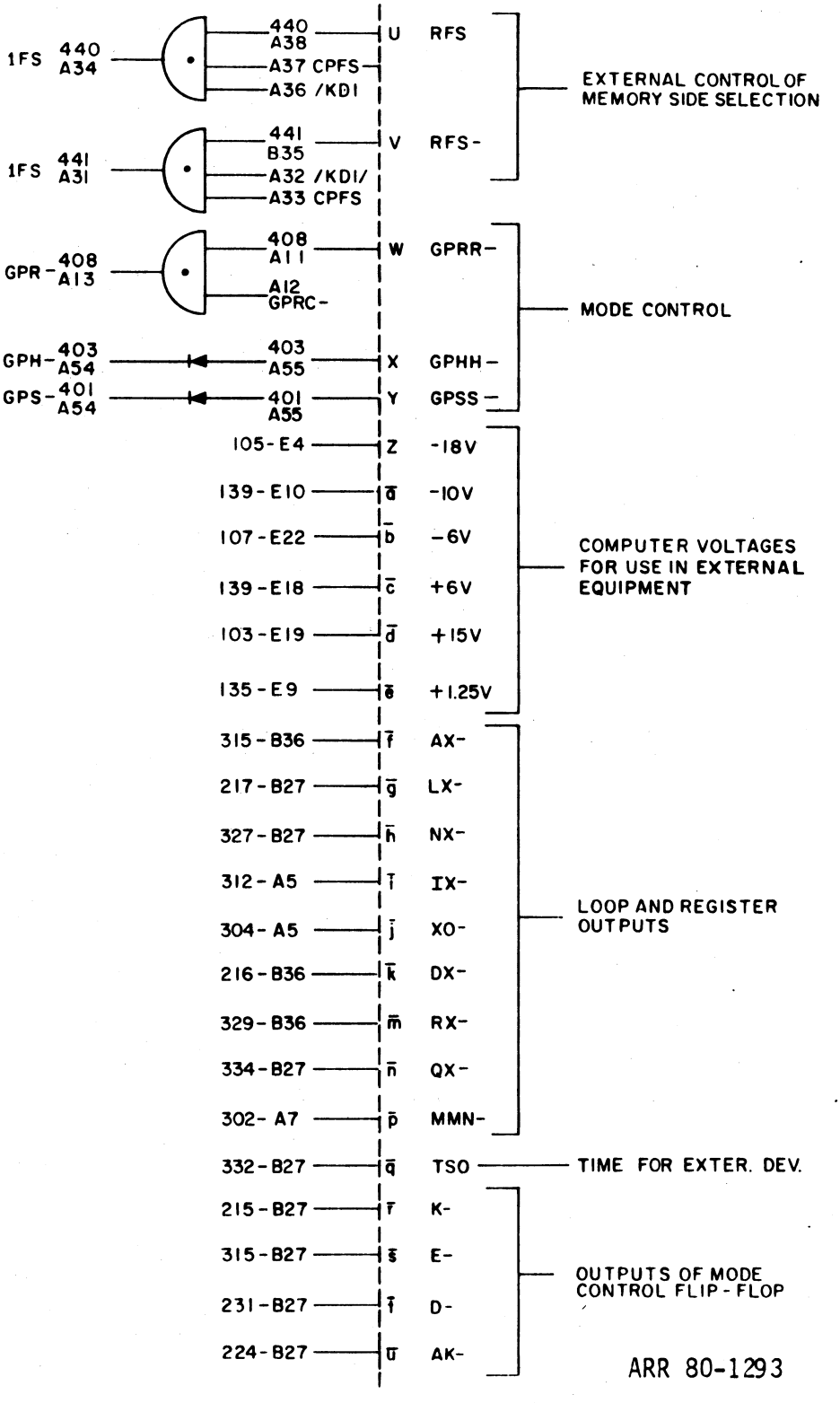


Figure 4-78. Output Connector J016 (sheet 2 of 2).

Section VI. Read and Write Circuitry

4-60. SCOPE

This section covers troubleshooting pertinent to read and write circuitry in the computer. Contained in this section is the theory of operation of the write switch, write amplifier, the logic involved in loading the memory, the read switch, read amplifiers used in reading out of memory, as well as a description of the memory itself.

4-61. COMPUTER MEMORY

a. General. The computer memory is a rotating magnetic disk driven by a three-phase, 120/208 ±20 volt line-to-neutral, 400 ±20 Hz motor at a nominal speed of 6000 rpm. The disk is coated on both sides with ferrous oxide similar to the coating on conventional magnetic tape. The disk rotates between an upper and lower head plate which contains stationary magnetic read heads and write heads. Binary numbers may be written by the write heads as the disk rotates or read by the read heads. To write information on the disk, a current is caused to flow in a write head producing a magnetic field (fig. 4-79). This field produces magnetization on the disk which remains until replaced by new information. The polarity of the magnetization on the disk is a function of the current direction in the write head. The read heads are similar to the write heads but operate in reverse. A change in magnetization on the disk produces an electrical current in the head (fig. 4-80). This signal is sent to the read amplifier circuitry.

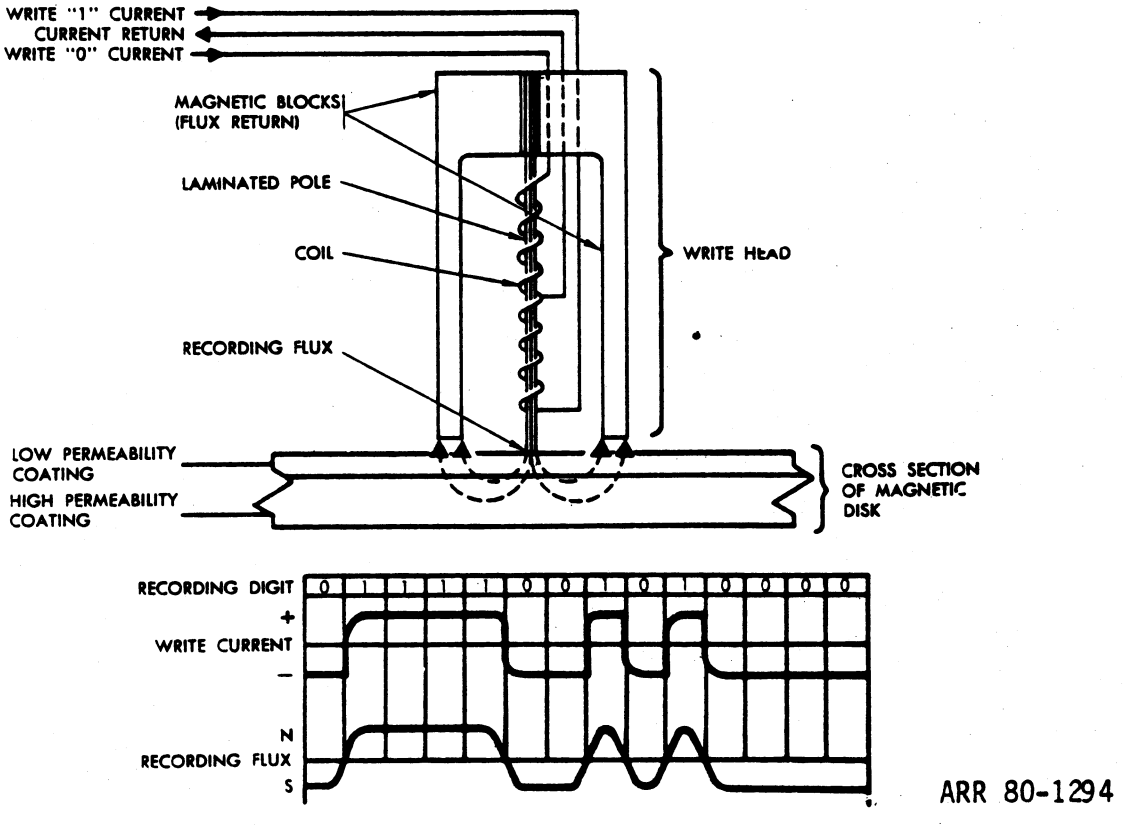


Figure 4-79. Memory Channel Writing Process and Write Head Cross Section.

4-61. COMPUTER MEMORY--Continued

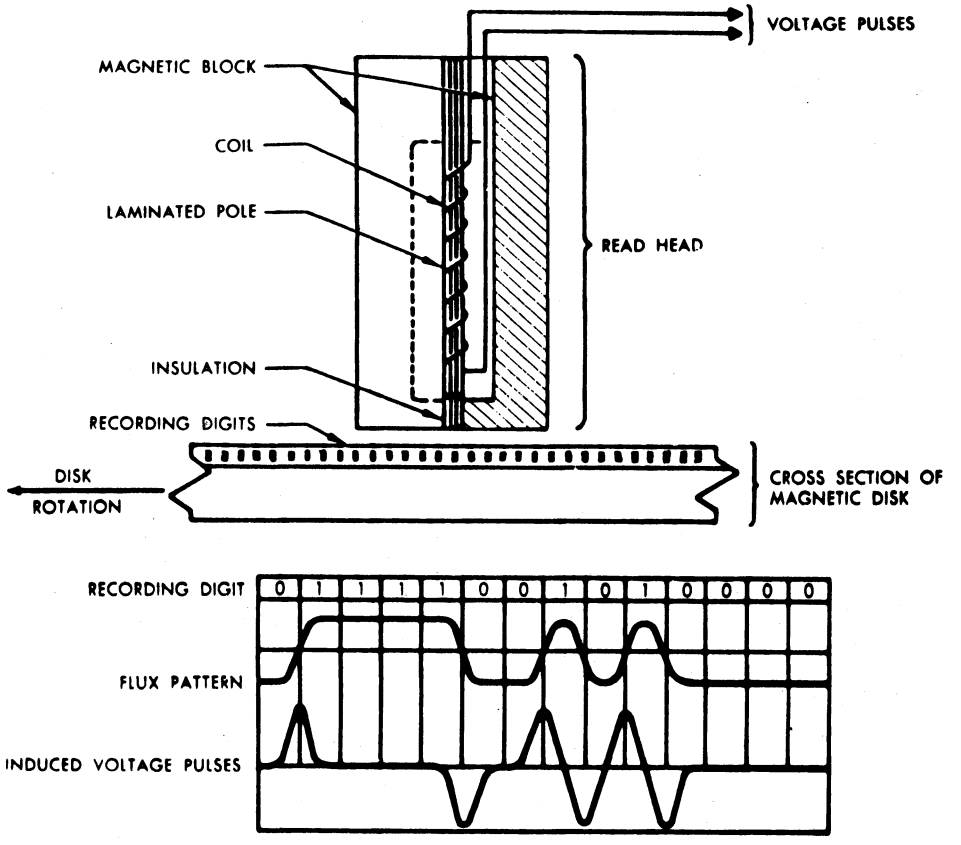


Figure 4-80. Memory Reading Process and Read Head Cross Section.

b. Memory Contents and Layout.

(1) The memory disk has 64 permanent channels (tracks) for information storage. There are 32 tracks on the side (channel 000 thru channel 076) of the disk and 32 on the other (channel 330 thru channel 336). Refer to figure 4-81.

(2) Each track has a storage capacity for 128 words (64 x 128 = 9192-word total) of 36 bits each word. Each word includes three sync bits and a parity bit. The remaining 32 bits are used for a 32-bit instruction "or" number, including one bit for sign. The three sync bits of each word provide the necessary switching time between the channels that is required by the write and read switch circuitry.

(3) Four, 12, or 16 channels may be used for working storage (fig. 4-81). The remaining channels are used for storage of the permanent program. The permanent program is loaded into the computer using the SDR and a selected program tape. (See section V for inputting information). Once the memory is loaded and the SDR is disconnected the permanent program is unchangeable. The working storage channels

are used for temporary storage of information under control of the permanent program and information fed in by the operator. The permanent and working storage channels constitute main memory channels.

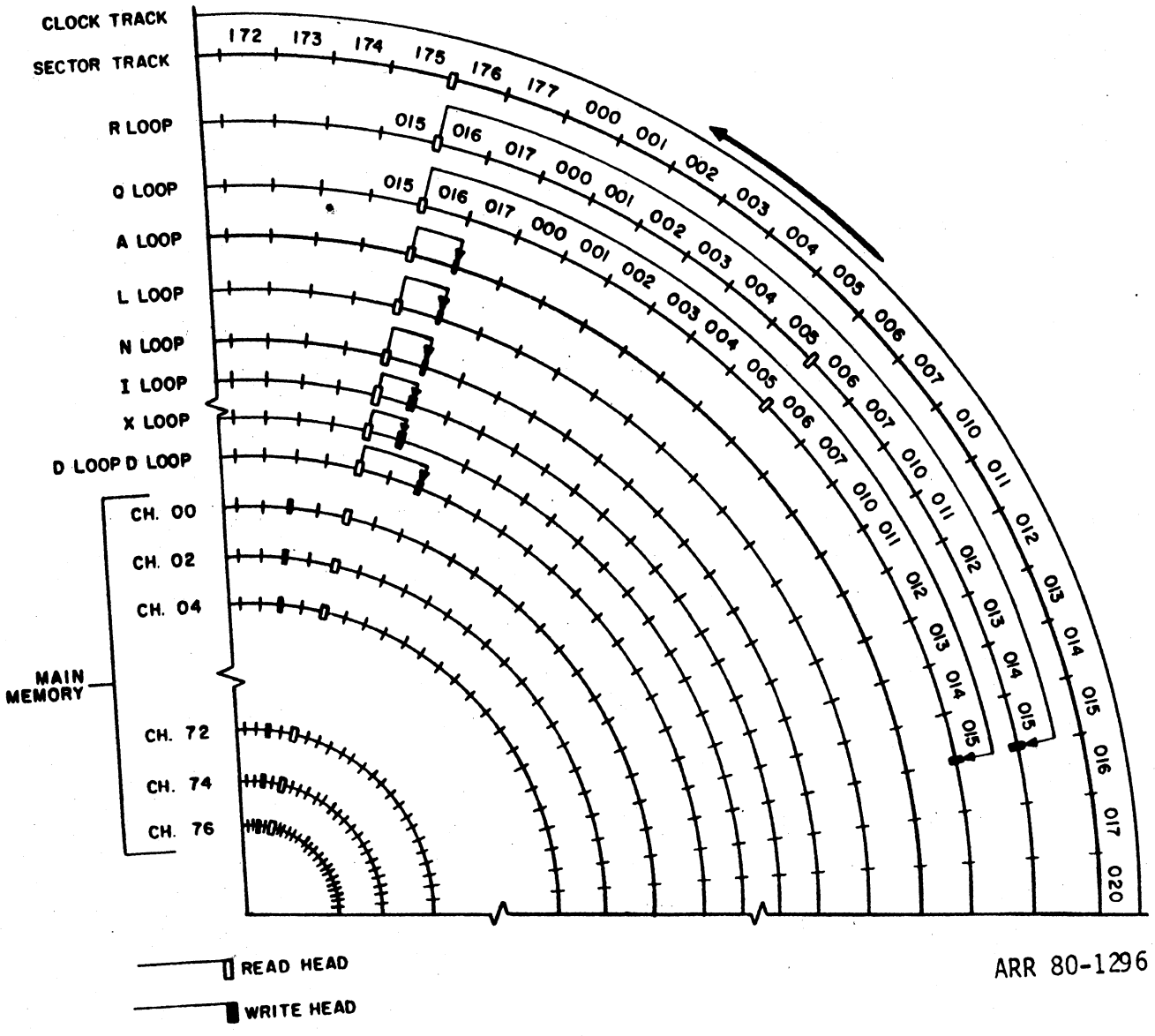


Figure 4-81. Conceptual Layout of Memory.

4-61. COMPUTER MEMORY--Continued

(4) In addition to the main memory channels, one channel contains eight recirculating loops (registers). They are as follows:

(a) R register. This is a 16-word recirculating rapid access loop, with an eight-word intermediate register output.

(b) Q register. This is a 16-word recirculating rapid access loop, with an eight-word intermediate register output.

(c) A register. This is a one-word recirculating accumulator loop. It is used to accumulate words during arithmetic operations and input operation (see section V).

(d) L register. This is a one-word recirculating lower accumulation register (see section V for use).

(e) N register. This is a one-word recirculating lower accumulation register (see section V for use).

(f) D register. This is a two-word recirculating output loop. It is used for processing of output information to display indicators (nixies) (see section V for use).

(g) I register. This is a one-word recirculating instruction register. It is used to store instructions.

(h) X register. This is a one-word recirculating instruction register. It is used to store instructions.

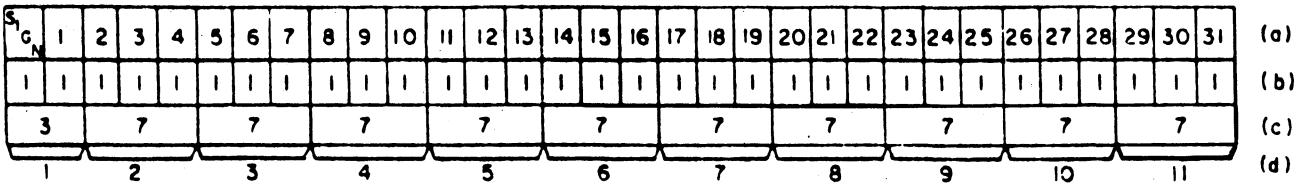
(5) Two permanently recorded channels contain data for timing purposes. These channels are the clock track and the sector track. The information read from the clock track is a continuous sine wave of frequency approximately 460 KHz. This sine wave is amplified and shaped by the clock board and provides synchronization within the computer. The sector track provides sector address. (See section V for information on the use of sector in inputting.)

4-62. WORD FORMATS

a. General. As numbers appear in memory, there is no distinction between operands and instructions. Both are stored as 32 bit numbers of words with, in addition, one parity bit and three sync bits. When a number is read from memory it is interpreted by the control unit according to the computer phase. In the operand read phase, the number is read as an operand word; in the instruction read phase, it is read as an instruction word. Such a 32 bit word may be a number, an instruction, or any pattern of 32 bits desired for any reason. The 32 bits are labeled from the sign or flag position to the least significant position, 31, as shown on figure 4-82(a).

b. Computer Octal Format (fig. 4-82(d)). Each 32 bit computer word is represented by 11 octal digits. The first digit is formed from the two most significant bits of the binary word, and has a maximum value of 3.

Each of the remaining digits is formed from three bits of the computer word, and has a maximum value of 7. Because of the short (two bits) first octal digit in the computer format, it can be seen that a pure octal number and its octal representation are not the same.



ARR 80-1297

Figure 4-82. Computer Word.

c. Instruction Word Format (fig. 4-83(A)).

(1) Commands are stored in the memory in the form of one instruction per computer word represented by 11 computer octal digits. Each command consists of four separate fields, a flag, a next instruction address, an operation code, and an operand address.

(2) The FLAG, which is in the sign position, provides for the modification of the computer instruction, and is represented by an octal 2.

(3) The NEXT INSTRUCTION ADDRESS, which tells the computer where to go next in the program sequence, consists of a channel and a sector portion.

(a) The channel portion consists of 6 binary bits. These are represented by 3 octal digits which are evenly numbered from 000 to 176.

(b) The sector portion consists of 7 binary bits. These are represented by 3 octal digits which are numbered sequentially from 000 to 177.

(4) The operation code consists of 5 binary bits. These are represented by 2 octal digits and are even numbered from 00 to 76. Refer to tables 4-33 and 4-34 for computer operations codes.

(5) The operand address is the address of the number to be operated upon. It consists of a channel and sector portion and is in the same form as the next instructions address.

(6) Referring to figure 4-84 it can be seen that a total of 15 octal digits are required to represent an instruction word: 1 for the flag, 2 for the operation code, and 6 each for the addresses. Since a word is only 11 octal digits, it is necessary to "absorb" the four extra digits in the following manner (fig. 4-84).

(a) Let X represent the octal digits in each of the four fields and Y represent the octal digits.

4-62. WORD FORMATS--Continued

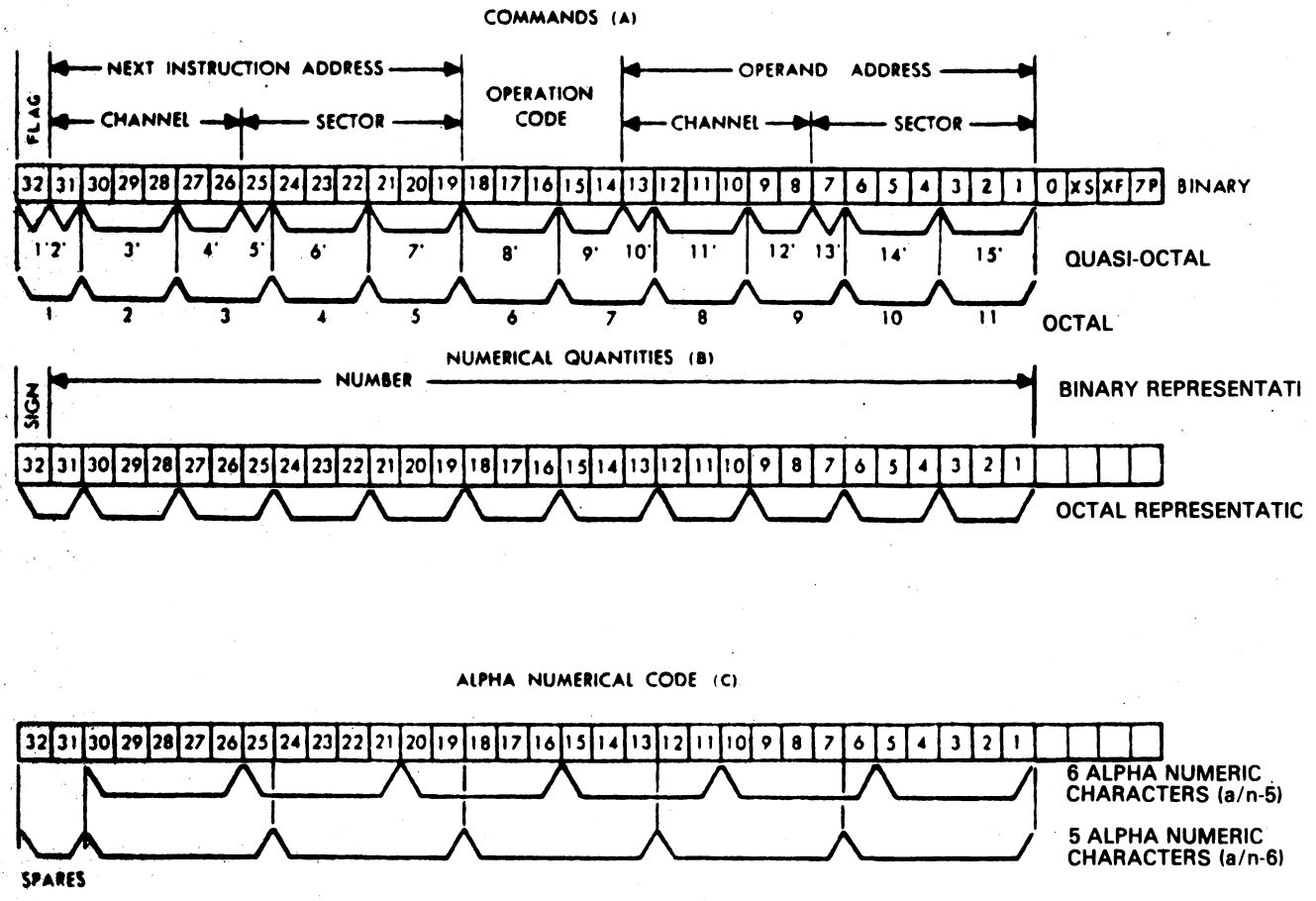


Figure 4-83. Actual Word Format.

FLAG	NEXT INSTRUCTION		OP. CODE	OPERAND ADDRESS		
	CHANNEL	SECTOR		CHANNEL	SECTOR	
X1	X2 X3 X4	X5 X6 X7	X8 X9	X10 X11 X12	X13 X14 X15	OCTAL
Y1	Y2 Y3	Y4 Y5	Y6 Y7	Y8 Y9	Y10 Y11	COMPUTER OCTAL

ARR 80-1299

Figure 4-84. Computer Instruction Word Formation.

Table 4-33. Operation Codes

Computer Instruction	Mnemonic	Flag	Op Code	Right Channel	Right Sector
Clear and add[1]	CLA	0/2	24		
Clear and subtract	CLS	0/2	26		
Add	ADD	0/2	00		
Subtract	SUB	0/2	02		
Multiply	MPY	0	20		
Divide	DIV	0/2	30		
Store A-register[2]	STA	0/2	50		
Store N-register	STN	0	40		
Store D-register	STD	0/2	42		
Store L-register	STL	0/2	52		
Store Operand Address[3]	STO	0/2	70		
Store Program Address	STP	0	60		
Load R-loop[4]	LDR*	2	72		
Load Q-loop	LDQ	0	72		
Store R-loop	STR	0	62		
Transfer on Zero	TZE	0/2	12		
Transfer on Plug	TPL	0/2	10		
Transfer	TRA	0/2	14		
Transfer on Overflow	TOV	0/2	16		
"A" Right Cycle[5]	ARC	0	76	000	S
"A" Right Shift[5]	ARS	0	76	002	S
"A" Left Cycle	ALC	0/2	76	004	S
"A" Left Shift	ALS	0/2	76	006	S
Long Right Cycle[5]	LRC	0	76	020	S

4-62. WORD FORMATS--Continued

Table 4-33. Operation Codes--Continued

Computer Instruction	Mnemonic	Flag	Op Code	Right Channel	Right Sector
Long Right Shift	LRS	0	76	022	S
Long Left Cycle	LLC	0/2	76	024	S
Long Left Shift	LLS	0/2	76	026	S
Extract	EXT	0	34		
Take Absolute Value	ABS	0/2	36	170	
Replace A on Minus from L	RML	0/2	36	172	
Replace A on Minus from N	RMN	0/2	36	174	
Zero L	ZEL	0	36	162	
Equal Search	EQS	0/2	64		
Greater than or Equal Search	GES	0/2	66		
Halt Program	HLT	0	36	120	
Halt Display Mode	HDM	0	36	166	
Initiate Display Mode	IDM	0	36	164	
Discrete Input to A	DIA	0	36	040	
Discrete Outputs Off	DOF	0	36	100	
Output Device Stepping-1	OD1	0	36	102	
Output Device Stepping-2	OD2	0	36	104	
Output Device Stepping-3	OD3	0	36	106	
Input Device Stepping-1	ID1	0	36	110	

Table 4-33. Operation Codes--Continued

Computer Instruction	Mnemonic	Flag	Op Code	Right Channel	Right Sector
Input Device Stepping-[2]	ID2	0	36	112	
Input Device Stepping-[3]	ID3	0	36	114	
No Solution Light	NSL	0	36	116	

[1]The flat bit is indicated by a (2) and not a (1).

[2]The mnemonic for this command was formerly STO.

[3]The mnemonic for this command was formerly STA.

[4]LDR - the Op Code for this command is a flagged LDQ command.

[5]One can code a (2) here as a flag bit; however, it is not recommended.

Table 4-34. Input-Output Command Summary

Mnemonic	Flag	Op Code	Right Channel	Right Sector	Interpretation
REO	0	54	000		Read Ext. device in Octal Mode.
RTO	0	54	020		Read tape device in Octal Mode.
PKO	0/2	54	060		Read Keyboard in Octal Mode.
RED	0/2	54	10X	No. of blocks	Read Ext. device in Decimal Mode.
RTD	0/2	54	12X	No. of blocks	Read Tape device in Decimal Mode.
RKD	0/2	54	16X	No. of blocks	Read Keyboard device in Decimal Mode.
RE6	0/2	56	00X	No. of blocks	Read Ext. device in Alpha-6 Mode.
RT6	0/2	56	02X	No. of blocks	Read Tape Device in Alpha-6 Mode.

4-62. WORD FORMATS--Continued

Table 4-34. Input-output Command Summary--Continued

Mnemonic	Flag	Op Code	Right Channel	Right Sector	Interpretation
RM6	0/2	56	04X	No. of blocks	Read Mag. Tape in Alpha-6 Mode.
RK6	0/2	56	06X	No. of blocks	Read Kayboard in Alpha-6 Mode.
RE5	0/2	56	10X	No. of blocks	Read Ext. device in Alpha-5 Mode.
RT5	0/2	56	12X	No. of blocks	Read Tape device in Alpha-5 Mode.
RM5	0/2	56	14X	No. of blocks	Read Mag. Tape in Alpha-5 Mode.
RK5	0/2	56	16X	No. of blocks	Read Keyboard in Alpha-5 Mode.
WEOT	0/2	44	00X	No. of blocks	Write FADAC to Ext. Octal Info. in teletype code.
WFOT	0/2	44	02X	No. of blocks	Write FADAC to FACAC Octal Info. in teletype code.
WEOF	0/2	44	04X	No. of blocks	Write FADAC to Ext. Octal Info. in Fieldata code.
WFOF	0/2	44	06X	No. of blocks	Write FADAC to FADAC Octal Info. in Fieldata.
WEDT	0/2	44	10X	No. of blocks	Write FADAC to Ext. decimal Info. in teletype code.
WFDT	0/2	44	12X	No. of blocks	Write FADAC to FADAC decimal Info. in teletype code.
WEDF	0/2	44	14X	No. of blocks	Write FADAC to Ext. decimal Info. in Fieldata code.
WFDF	0/2	44	16X	No. of blocks	Write FADAC to FADAC decimal Info. in Fieldata code.
WE6	0/2	46	00X	No. of blocks	Write FADAC to Ext. Alpha-6 Info.

Table 4-34. Input-output Command Summary--Continued

Mnemonic	Flag	Op Code	Right Channel	Right Sector	Interpretation
WF6	0/2	46	02X	No. of blocks	Write FADAC to FADAC Alpha-6 Info.
WE5*	2	46	10X	No. of blocks	Write FADAC to Ext. Alpha-5 Info.
WF5*	2	46	12X	No. of blocks	Write FADAC to FADAC Alpha-5 Info.
WE4	0	46	10X	No. of blocks	Write FADAC to Ext. Alpha-5 Info.
WF4	0	46	12X	No. of blocks	Write FADAC to FADAC Alpha-6 Info.

(b) Then Yn will have the following values:

$Y_1 = X_1 + X_2$

$y_2 = X_3$

$Y_3 = X_4 + X_5$

$Y_4 = X_6$

$Y_5 = X_7$

$Y_6 = X_8$

$Y_7 = X_9 + X_{10}$

$Y_8 = X_{11}$

$Y_9 = X_{12} + X_{13}$

$Y_{10} = X_{14}$

$Y_{11} = X_{15}$

NOTE

All channels and operation codes are evenly numbered. Therefore, whenever an odd number appears in a channel address, a sector greater than or equal to 100 is addressed (i.e., $Y_3 = X_4 + X_5$ or $Y_2 = X_{12} + X_{13}$). Whenever an odd number appears in the Op code, the channel of the operand address is greater than or equal to 100 (i.e., $Y_7 = X_9 + X_{10}$).

4-62. WORD FORMATS--Continued

(c) The flag digit is derived as follows:

$Y_1 = X_1 + X_2$

$Y_1 = 0$ When no flag is called and Next Instruction (NI) channel is less than 100.

$Y_1 = 1$ When no flag is called and NI channel is greater than or equal to 100.

$Y_1 = 2$ When flag is called and NI channel is less than 100.

$Y_1 = 3$ When flag is called and NI channel is greater than or equal to 100.

(7) To illustrate an instruction word;

(a) Given the instruction "Clear and Add (CLA = 24 from table 4-34), the contents of channel 102, sector 123, and go to channel 112, sector 124" the word format as shown in figure 4-85.

(b) Thus the computer octal code referring to figure 4-85 is as shown in figure 4-82.

FLAG	NEXT INSTRUCTION		OP CODE	OPERAND ADDRESS		
	CHANNEL	SECTOR		CHANNEL	SECTOR	
0	112	124	24	102	123	OCTAL
1	13	24	25	03	123	COMPUTER OCTAL

ARR 80-1300

Figure 4-85. Sample Instruction Word.

d. Operand Word Format (fig. 4-83). Operand words, include a sign bit and 31 information bits. If a number is positive, the first bit position or sign position always contains a Ø. The subsequent 31 bits are the binary representation of a fixed part fraction. Negative numbers are represented in two's complement form and, therefore, always have a 1 in the sign position. Since the first octal digit is the sum of the sign position and the most significant bit position (fig. 4-82) in the computer this digit will equal a Ø or 1 when a number is positive and 2 or 3 when a number is negative.

e. Special Code Formats. Special alpha-numeric codes also form words. These special codes are used mainly to control external devices connected to the computer (fig. 4-83(C)).

4-63. WRITING DATA INTO MEMORY

a. General. There are five write amplifier boards and two write switch boards. On each amplifier board there are two write amplifier circuits, making a total of 10 write amplifier circuits. Five write amplifiers are used for the five one-word loops (A, L, N, X, I), two write amplifiers are used for the 16-word loops (Q and R), one write amplifier is used for the one two-word loop (D), and two write amplifiers are used for main memory writing. On each write switch board there are 12 write switch circuits.

NOTE

Refer to TM 9-1220-221-34/1/1 for the write amplifier schematic and for the write switch schematic.

b. Writing Operation.

(1) As explained in a. above, the two main circuits in the writing operation are the write switches and the write amplifiers. Two write switch circuits, a number of isolation diodes, and a write amplifier circuit are used in writing into memory. TM 9-1220-221-34/1/1 illustrates the entire main memory write head configuration with the write switch logic indicated by block diagram. Utilizing this chart the technician is afforded complete mechanization of main memory write heads.

(2) As an example of mechanization the writing of a 1 into memory location 60 will be performed. The procedure to accomplish this is as follows:

(a) Locate the one side of memory write head 60--location W60.

(b) The center tap of this write head is the output of CTB4--a write switch circuit.

(c) The one side output is connected through an isolation diode to SS1A output--the tap write switch.

(d) W60 logic is mechanized.

(3) The writing of information (1 or Ø) in memory will be given by example. Referring to figure 4-86, the signal flow for writing a 1 into memory location 60 will be as follows:

(a) Determine the configuration of the channel flip-flops. The channel flip-flops (C7 thru C2) will be in the state shown in figure 4-86.

(b) Since the logic C7 C6- is true, C761 will be true.

(c) Since C5 is true and C761 is true; transistor Qc will turn on, allowing +15 volts to be present at the center tap of the write head 60.

(d) Since the logic C4- C3- is true, C430 will be true.

4-63. WRITING DATA INTO MEMORY--Continued

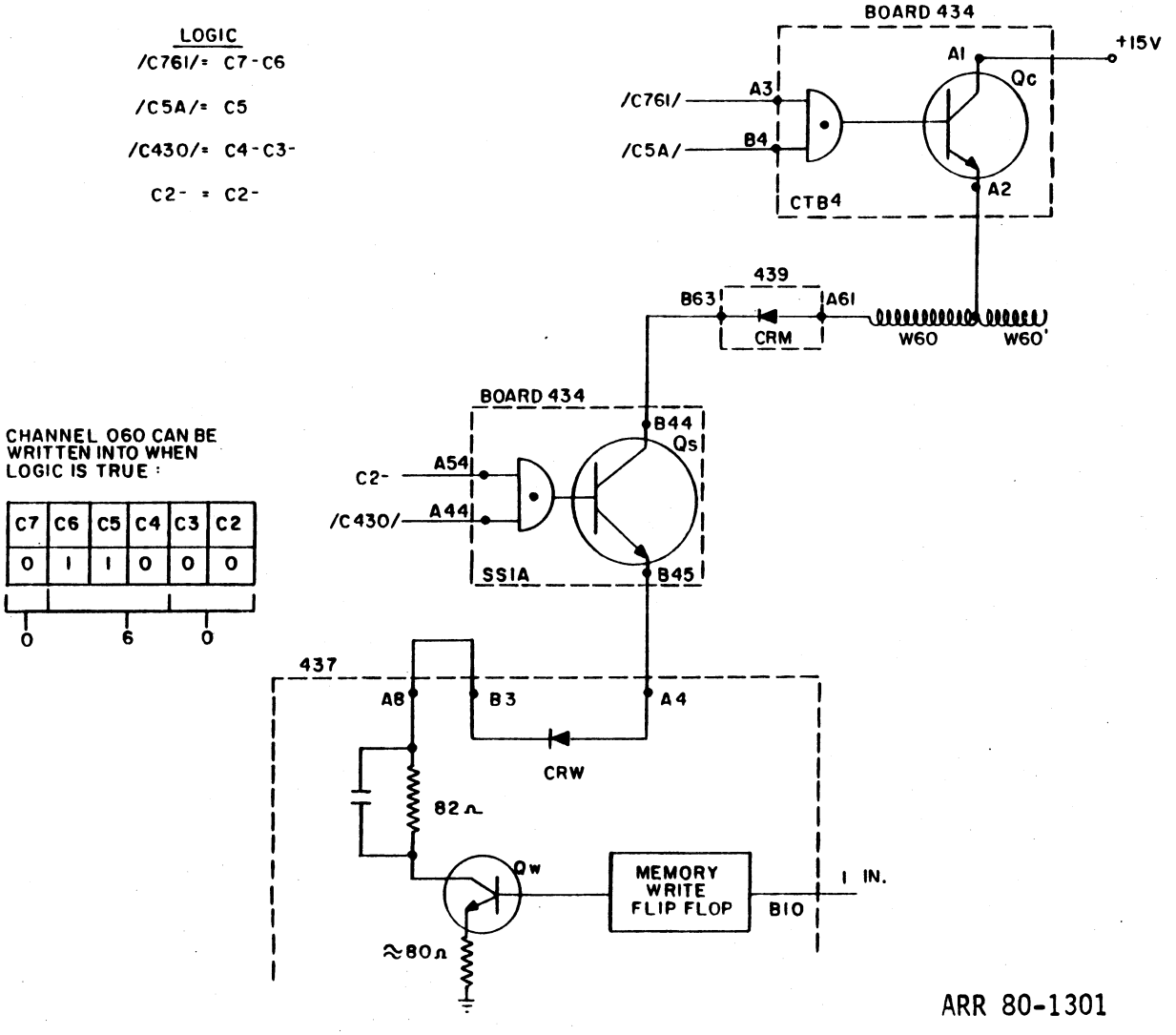


Figure 4-86. Circuitry for W60.

(e) Because C2- is true and C430 is true, transistor Qs will also turn on.

(f) When the logic to write a 1 comes true, transistor Qw turns on.

(g) Current will now flow through the write head. The path is from ground, through the 80-ohm resistor, through transistor Qw, through the 82-ohm resistor, through diode CRW, through transistor Qs, through diode CRM, through the write head W60, through transistor Qe to the +15-volt source. A 1 has been written into memory location 60.

NOTE
Refer to TM 9-1220-221-34/1/1 for the MW1 and MWØ circuitry. Also refer to paragraph 4-61a for write head current necessary to magnetize the disk.

4-64. READING DATA FROM MEMORY

a. General. Read heads passing over recorded flux areas on the memory generate voltage pulses. Induced pulses are interpreted by the computer as binary digits (fig. 4-80).

(1) The read head senses only changes in magnetic polarities. A positive pulse occurs when one of two adjacent digits change from binary Ø to binary 1. A negative pulse occurs when one of two adjacent digits change from binary 1 to binary Ø. A succession of identical binary digits does not affect the read head. After a positive pulse, all succeeding digits are interpreted as binary 1's until a negative pulse occurs. Similarly successive zero digits are interpreted as Ø's until a positive pulse occurs.

(2) Each of the 64 main memory channels require one read head. A channel is selected (see para b below) when the correct sector of word is addressed. The sector address digits stored within a command are compared with the sector digits stored in the sector channel of memory. When agreement occurs, meaning that the read head is passing over the correct sector in the memory channel, the output from the head is sent through the appropriate read switch to the read amplifier whose output--(read flip-flop) is sent to the logic circuitry.

(3) Clock and sector channels also have one read head each and require no addressing.

(4) There are also read heads for loops A, N, L, I, X, D, R, and Q. Loops R and Q having intermediate loop read heads (fig. 4-81), require two read amplifiers per loop.

b. Selection of Read Head.

(1) TM 9-1220-221-34/1/1 shows the entire main memory read head configuration. All the read switches involved in selecting a given memory location are depicted here. The output from the read head is controlled by two separate sets of read switches. The reason for this is the parallel search capability of the configuration. Both operand data and next instruction data are searched simultaneously. The inputs to the read switches whose outputs are connected to the input of the MMN (main memory number) read amplifier are related to the CN flip-flops. These allow searching for an operand. The inputs to the read switches whose outputs are connected to the input of the MMP (main memory program) read amplifier are related to the C flip-flops. These CP flip-flops allow searching for instructions.

(2) The operation of read head selection will be given by example. Read selection of channel 066 for next instruction data will be described.

4-64. READING DATA FROM MEMORY--Continued

NOTE

The specific reading of a given word by sector location and comparison is explained logically in section V of the chapter.

(3) Referring to the read switch shematic in TM 9-1220-221-34/1/1 to find the CP logic input, any given read switch can be mechanized. Figure 4-87 shows the specific circuitry for M66. The logic for (CPU3) and (CPL3) is as follows:

(CPU3) = CP7- CP6 CP5
(CPL3) = CP4- CP3 CP2

This logic allows instruction information to be felt at pin A65, the input to the MMP read amplifier.

(4) This circuit functions as a class A emitter-follower. The voltage is induced into the read head by the magnetic flux on the disk. Q3 is normally on so that the emitter is a few tenths of a volt negative. If the signal is positive, indicating a 1, the transistor will conduct more and the voltage at the emitter will increase toward ground. If the signal is negative, indicating a Ø, the transistor will conduct less and the voltage at the emitter will become more negative. Gate (CPU3), (CPL3), and the output from Q3 form an "and" gate. Pin A65 will read what is contained in memory channel 066 when gates (CPU3) and (CPL3) are true.

c. Amplification of Selected Read Switch Output Signal.

(1) As explained previously, the output from the read head is at a low level (in the millivolt range) and has the form:

(a) A positive pulse if a series of 1's are being read.

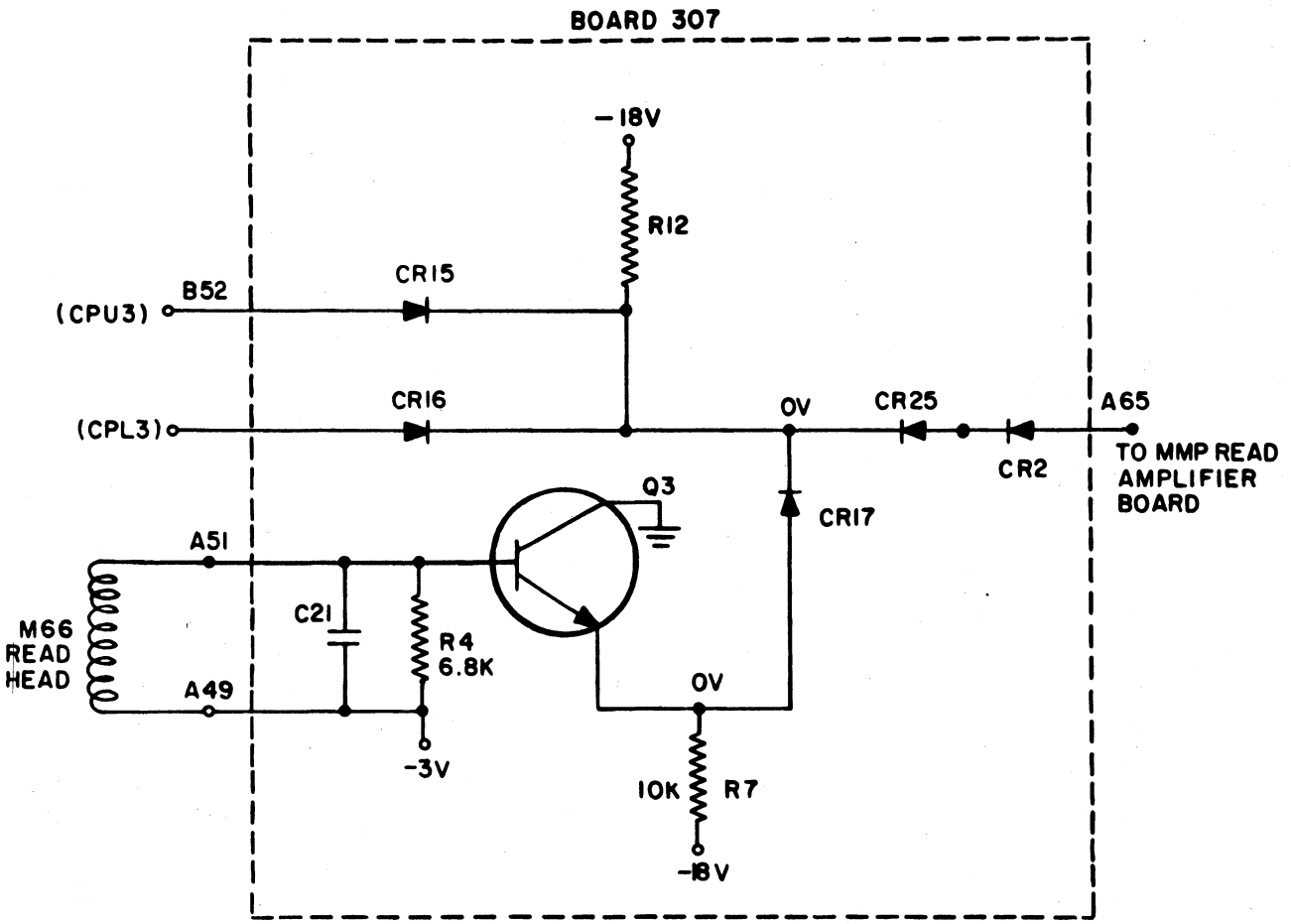
(b) A negative pulse if a series of 0's are being read.

(2) The function of the read amplifier is to amplify these pulses and convert them to logical read outputs (a 1 represented by a -6-volt output, a Ø represented by a 0-volt output).

(3) The block diagram in figure 4-88 is from the read amplifier board. The discussion will begin at TP time. At this time the TP input after being shaped and amplified, will zero set the read flip-flop.

(4) The output from the read switch comes into the read amplifier at pin 65A and is amplified in the low level amplifier.

(5) If the pulse is positive indicating a 1 or a series of 1's, the output is fed into the degenerative amp whose function is to clip the wave to maintain a constant output. After this stage the pulse is fed to the read one amplfier where it is again amplified and shaped.



FLIP FLOP CONFIGURATION

CP7	CP6	CP5	CP4	CP3	CP2
0	1	1	0	1	1
0		6		6	

ARR 80-1302

Figure 4-87. Memory Read Head and Read Switch Mechanization.

4-64. READING DATA FROM MEMORY--Continued

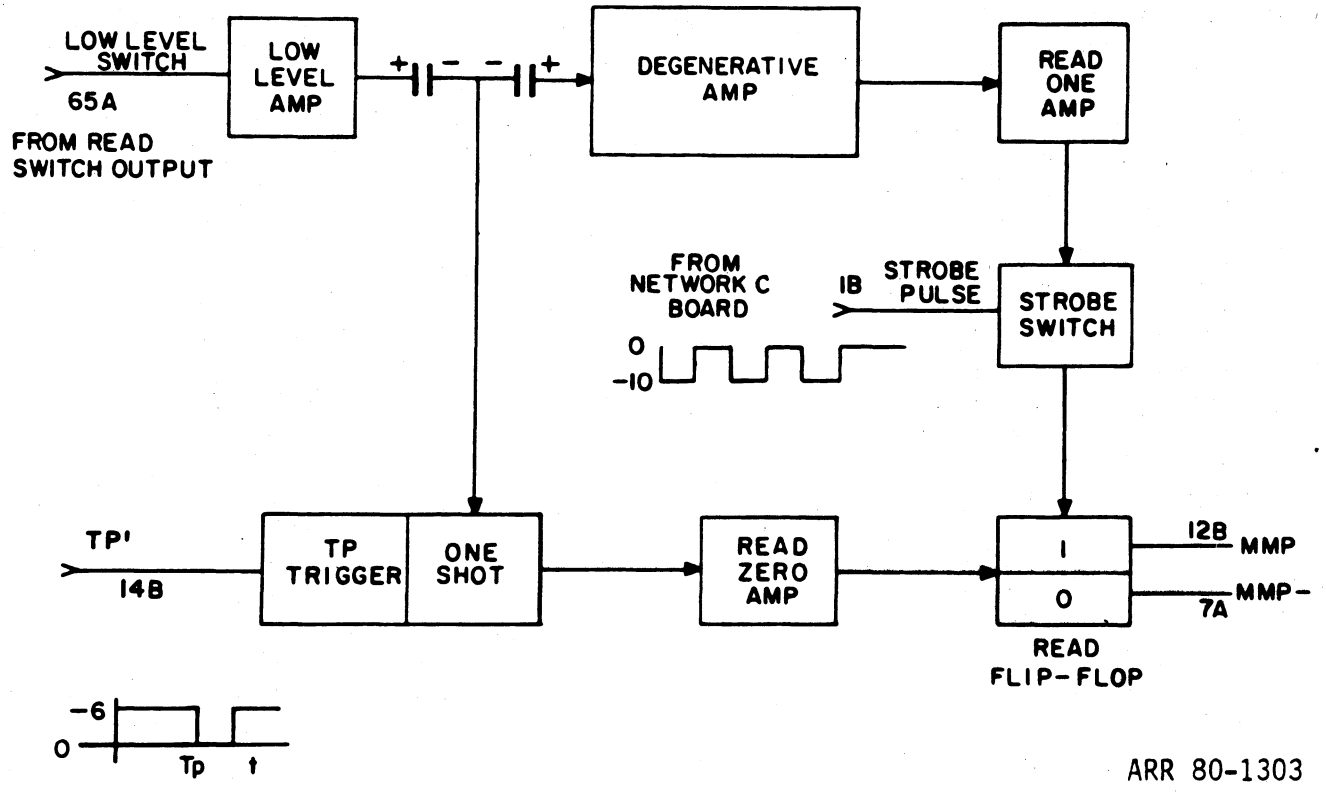


Figure 4-88. Read Amplifier Block Diagram.

(6) When the strobe switch is turned on, that is when the strobe signal is -10 volts, the read flip-flop will one set if a 1 was read from memory.

NOTE

Although not shown in the block diagram, the output of the read flip-flop is the input of an output driver. Therefore, when we speak of the output of the flip-flop we are truly speaking of output of driver fed by the flip-flop.

(7) The flip-flop will remain one set until either Tp time (the end of the sector) or a negative spike (representing of Ø) is read from the memory.

(8) As before, the negative spike is amplified in the low level amplifier.

(9) The negative spike now, however, triggers the one-shot multivibrator.

(10) The pulse from the one shot is amplified in the read zero amplifier and when the strobe pulse is true, will zero set the read flip-flop.

(11) It will remain zero set until another positive pulse is detected by the read head.

NOTE

Refer to TM 9-1220-221-34/1/1 for the schematic of the read amplifier board.

d. Parity Generation and Detection. Parity errors are detected when reading data out of memory. Since operands (numbers) and instructions can be read simultaneously, two flip-flops are used to detect parity errors. Take the case of operand readout first. Flip-flops MN and PN, which were used in generating the parity bit during writing of information into memory, are now used in detecting parity errors in reading operands (numbers) out of memory. If there are an even number of ones in a word while reading, then PN will be zero set at parity bit checking time, TP. This tells the computer that an even number of zeros (which also makes an even number of ones in a 32-bit word) were recorded while reading. The computer then compares the next bit out of MN which was generated by the computer when this word was originally written into memory. If, in this case, a zero was originally written into the TP bit position of this word, a parity error would exist and computations verifying would halt and the PARITY indicator would flash. PE would be one set by one of the following gates depending on whether in compute or verify modes.

```
1 PE = + C7- /MNA-/ KE (MMPT) PN-
       + C6- /MNA-/ KE (MMPT) PN-
       + C7- /MNA-/ ND- (KIOP) (MMPT) PN-
       + C6- /MNA-/ ND- (KIOP) (MMPT) PN-
```

Note that PN- and MN- both must be true (zero set) in the above gates in order to one set PE and thus designate a parity error. Other gates take care of the other parity error conditions when PN is one set and MN reads a 1 bit at Tp time; i.e.,

```
1 PE = + PN /MNA/ KE (MMPT)
       + PN /MNA/ KD- (KIOP) (MMPT)
```

In the case of reading instructions, flip-flops PP and MP are used as a control to one set PE by

```
1PP = PP- MP- CP76- /KD3/ XC
```

This in turn causes PE to one set by

```
1 PE = PP /TXF/ K
```

An even number (2, 4, etc) of altered bits in a word being read from memory cannot be detected by this method. Parity checks (on characters, not words) are also made when inputting into memory with the field data (8 level) code.

4-65. REGISTER READING AND WRITING

a. General. Figure 4-89 is a diagram of a typical register (A register). The register shown has the storage capacity of 36 bits with 34 of the bits on the disk (which would include one each being sensed by the A0 and A32 flip-flops). The information on the disk is constantly being read, passed through the flip-flops, and written back onto the disk. As the read head picks up a binary digit from the memory channel, it is immediately stored in read flip-flop A0. The bit that was in A0 is sent to flip-flop AX (A loop extension flip-flop), the bit that was in AX is sent to the AP flip-flop, what was in AP is then copied by the write amplifier A32, which is immediately sensed by the write head, and the bit is written back on memory.

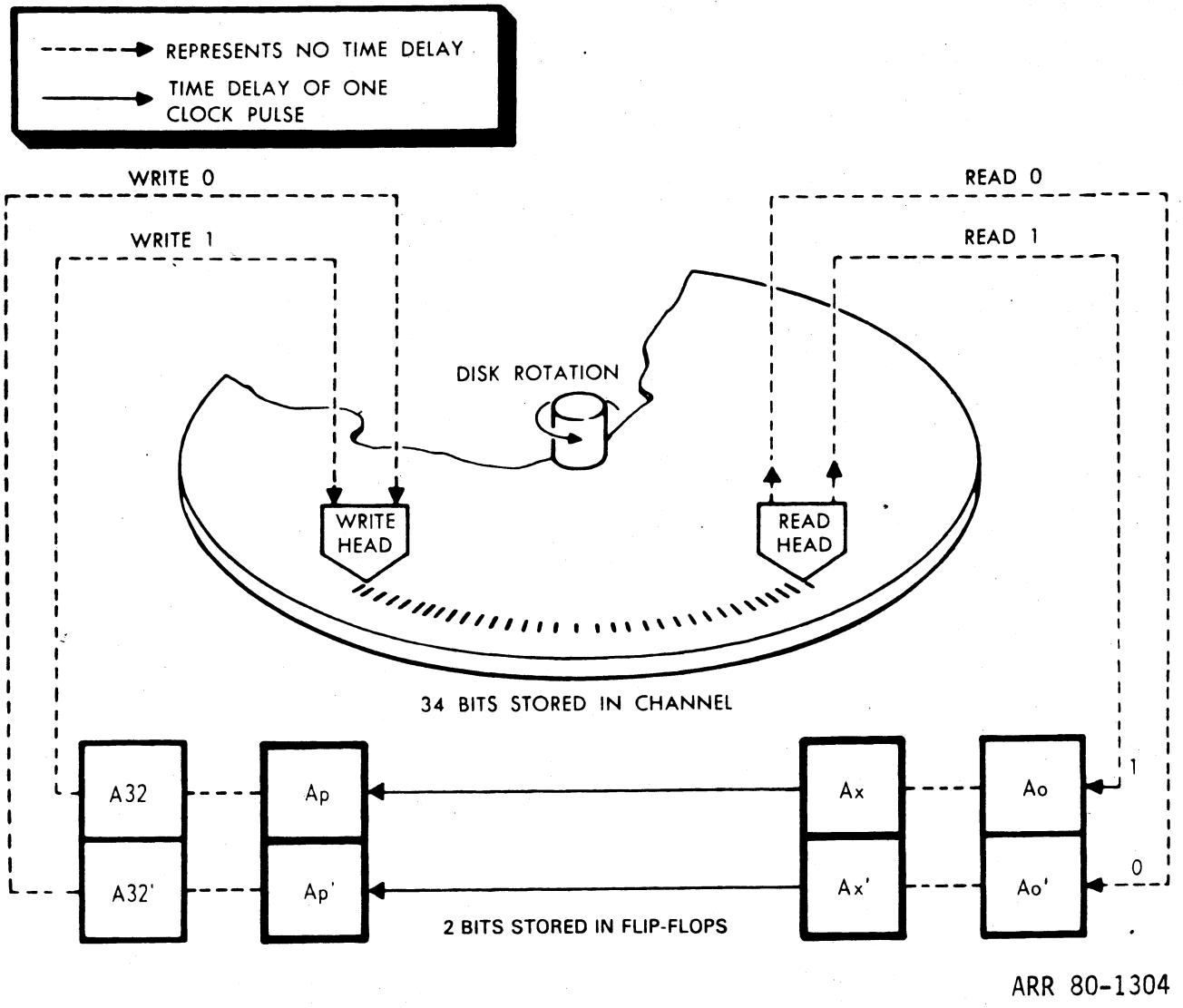


Figure 4-89. Functional Diagram of A Register.

b. Addressing and Loop Length.

(1) The number of words between the read and write heads determine the length of the particular loop. The A, L, and N registers are one-word registers since their contents are available every word or sector time. They are addressed as channels 170, 172, and 174 respectively.

NOTE
The sector numbers are ignored for these registers.

(2) The R and Q rapid access loops are of 16-word lengths but have intermediate read heads which makes the contents of a particular sector available every eight word times. The intermediate read heads have no effect on the recirculation process. The channel address of R is 142 and the channel address of Q is 152. The sector address may be any sector number from 000 to 177 but only the last four binary bits are interpreted by the computer. Thus, the sector addresses are actually 000 to 017. The intermediate read heads for the R and Q loops have as their channel addresses 140 and 150.

(3) The display register or D loop is a two-word loop and has a channel address of 160. The right half of the two-word loop is addressed by odd sector numbers (i.e., 003) while the left half is addressed by even sector numbers (i.e., 004).

(4) The instruction register 1 and the X register are one-word loops and have no channel address. They are used to perform interim tasks.

c. Reading and Writing into Registers.

(1) Table 4-35 shows the various registers, channel designations, and the associated flip-flop functions.

(2) The write flip-flop writes information directly into the memory. The writing operation is basically the same as writing into main memory with one exception, write switches are not necessary to select the given channel. The write amplifiers of the registers are connected directly to the write heads, with +15 volts applied to the center taps. Therefore, when the write flip-flop is one set, a ground return path is provided for the +15 volts through the write to ground through the write amplifier output. The same is true for writing a 0.

NOTE
Refer to paragraph 4-63 for main memory writing operation and table 4-35 for the write flip-flop used for each register.

(3) Information read from a given register is fed directly to a read amplifier circuit (the circuit is located on one of the read switch boards). As in the case of writing no switches are necessary to select a given memory location. The read amplifier circuit functions exactly the same as the main memory read amplifiers (refer to para 4-64). The read flip-flop for each of the registers is shown in table 4-35.

4-65. REGISTER READING AND WRITING--Continued

Table 4-35. Register Flip-Flop Functions

Register	Channel designation	Write flip-flop[1]	Read flip-flop[2]	Loop control flip-flop[3]	Loop extension flip-flop (Tp phasing)[3]	Loop extension flip-flop (Tx phasing)[3]
A	170	A32	AO	AC	AP	AX
L	172	L32	LO	LC	LP	LX
N	174	NP	NO	NC	None	NX
R	142 140	RP	RO RM[4]	RC	None	RX
Q	152 150	QP	QO QM[4]	QC	None	QX
D	160	DP	DO	DC	None	DX
I	None	132	IX	IC	IP	None
X	None	XP	XO	XC	None	None

[1]Refer to table 4-14 for location.

[2]Refer to table 4-15 for location.

[3]Refer to table 4-13 for location.

[4]RM and QM are rapid access loop read flip-flops. They allow access to a given word in 8 word lengths instead of 16. They are not involved in the recirculation process (table 4-15).

d. Recirculation.

(1) The specific recirculation process is given in paragraphs (2) thru (9) below. In all cases of recirculation the loop control flip-flop must be zero set. Refer to table 4-35 for each of the flip-flops referred to in text.

NOTE

Specific logic can be followed by referring to the appropriate logic list in TM 9-1220-221-34/1/1.

(2) The A register recirculation process is as follows:

(a) A32 writes information into memory.

(b) AO copies information from memory.

(c) AX copies AO.

(d) Since AC is zero set, AP copies AX.

(e) A32 copies AP and hence the loop is completed.

(3) The L register recirculate process is as follows:

(a) L32 writes information into memory.

(b) LO copies information from memory.

(c) LX copies LO.

(d) Since LC is zero set, LP copies LX.

(e) L32 copies LP and hence the logic is completed.

(4) The N register recirculate process is as follows:

(a) NP writes information into memory.

(b) NO copies information from memory.

(c) NX copies NO.

(d) If NC flip-flop is zero set, NP copies NX. This completes the loop.

(5) The R register recirculates information as follows:

(a) RP writes information into memory.

(b) RO reads information from memory.

NOTE

RM also reads information for rapid access but is not involved in recirculation.

(c) RX copies RO.

(d) If RC is zero set, then RP copies RX. This completes the loop.

(6) The Q register is identical in operation to the R loop. Merely substitute Q for R in each of the steps.

(7) The D register is identical in operation to the R loop. Merely substitute D for R in each of the steps.

4-65. REGISTER READING AND WRITING--Continued

(8) The I register recirculates information as follows:

(a) 132 writes information into memory.

(b) IX copies this information from memory.

(c) If IC is zero set, IP will copy IX.

(d) Since IC is zero set, I32 will then copy IP. This completes the loop recirculation.

(9) The X register does not recirculate information. Its reading and writing operation, however, is as follows:

(a) XP writes information into memory.

(b) XO copies this information from memory.

4-66. TROUBLESHOOTING

Troubleshooting can be approached by two general procedures. One method is the replacement of modules on the basis of probable failure. The second is isolation of malfunctioning part by dc voltage measurements, wave shaped tracing the resistance readings. The basis for approach here will be the former. However, a procedure will be given here for writing into and reading from any main memory channel and sector. Using this procedure and the theory of operation in paragraphs preceding this one, wave shape tracing can be accomplished.

FILL AND VERIFY PROCEDURE

1 Connect the SDR to the FADAC as shown in TM 9-1220-221-20&P.

2 Set the SDR controls as follows:

a. TAPE ADVANCE switch to OFF position.

b. COMPUTE switch to HALT position.

c. FIELD DATA-TELETYPE switch to TELETYPE position.

d. AUXILIARY MEMORY switch to OFF position.

e. FILL-VERIFY switch to FILL position.

f. POWER switch to ON position.

g. SIGNAL switch to ON position.

3 Turn computer on.

4 After POWER READY indicator lights, depress RESET button on FADAC.

5 Depress RECEIVE button on FADAC.

6 Depress START FADAC button on SDR (KEYBOARD and IN/OUT indicator will light on FADAC, and FILL indicator lights on SDR).

7 Address desired channel and sector using five octal digits. The most significant digit of the sector number is combined/added to the least significant digit of the channel number. Thus channel 002 sector 100 is entered as 00300.

NOTE

The channel flip-flops, C7 thru C2, and the logic associated with the write switches (para 4-63b) should be properly set and can be measured if so desired.

8 Depress decimal point (.) key (this is the locate code).

9 Key in on keyboard the word to be written into the location selected. One word length is 11 octal characters. A good test pattern is a two-five pattern (25252525252). This will write alternate 1's and Ø's into memory when the ENTER key is depressed.

NOTE

When the ENTER key is depressed, the information, 1's and Ø's alternately in this case, can be viewed at the write amplifier board. (See TM 9-1220-221-34/1/1 for schematic and para 4-63b for theory of operation.)

10 Depress ENTER key (word is now in memory). To enter into the next sector of the same channel with the same word, depress ENTER key again. Each time the ENTER key is depressed the next sector will be filled.

11 To verify the contents once it is entered depress minus (-) key on keyboard. VERIFY indicator on SDR will light.

12 Address the same channel and sector again and depress point (.) key (as in example previously 00300 and then decimal point (.)).

13 Key in same word (i.e., 25252525252 as before) and depress ENTER key. As before, each time the ENTER key is depressed the next sector within that channel is verified.

NOTE

The read switch output and the logic input can be checked now (see para 4-46 and in TM 9-1220-34/1/1). The output from the read amplifier can also be monitored (alternate 6 volts and 0 volts). See paragraph 4-64b for theory of operation of the read amplifier and TM 9-1220-221-34/1/1 for read amplifier schematic.

14 If the ERROR indicator on the computer is flashing the word did not verify. Either information was tested incorrectly or a malfunction exists in write circuitry, the read circuitry, in the memory or in the associated wiring.

4-66. TROUBLESHOOTING--Continued

NOTE

To enter keyboard mode again to test another memory location (providing word verified ok) depress the plus (+) key on the computer keyboard.

15 In the event that testing was not correct enter and verify information again.

16 If problem persists follow either of the two troubleshooting procedures discussed above. The procedure for malfunction on the basis of probable failure is contained below.

MALFUNCTION REPAIR BY MEANS OF REPLACEMENT AND RESISTANCE CHECKING

1 Once the defective channel is determined by either keyboard entry testing, by using the memory evaluation tape, or by any other means, the technician should begin by replacing the appropriate read switch board.

2 To locate the board, refer to table 4-36. The read switch boards and the input pins from the read head associated with the channel location (left column) are listed here. The memory plug and the pins connected to the read head in memory are also listed.

3 The technician should replace this board and retest. If the channel passes successfully, replace the original board to verify that it is defective and rerun test. A loose read switch board may result in a parity error. If a new read board does not correct the parity, replace the original board and proceed to step (4).

NOTE

Since FALT testing has, it is assumed, been performed, the CP and CN flip-flops and the CPU, CPL CNU, and CNL gates should have been tested. However, if unsuccessful in remaining steps of this procedure these terms (see TM 9-1220-221-34/1/1 for term associated with memory locator) should be referenced using TM 9-1220-221-34/6 to their associated boards, replaced and retested.

4 Replace read amplifier boards 301 and 302 and retest. If the channel passes successfully, replace read amplifiers one at a time to determine which one is defective or overly sensitive to noise. If the read amplifier boards do not correct the parity, replace the original boards and proceed to paragraph (5) below.

5 Replace network C board 323 and retest. If the channel passes successfully, replace original board to verify that it is defective and rerun memory evaluation test tape. Network C board contains the strobe circuit. (See para 4-64 for use of strobe in setting read flip-flop on read amplifier board.) If a new network C board does not correct parity, replace original board and proceed to paragraph (6) below.

Table 4-36. Memory Read Switches and Plugs

Memory channel	Read switch board pins			Memory Plug	Pins		Memory channel	Read switch board pins			Memory Plug	Pins	
M00	303	B48	B46	P1	25	26	M56	306	A56	A58	P2	28	29
M02	303	A48	A46	P1	27	28	M60	307	B46	B48	P2	30	31
M04	303	B51	B49	P1	29	30	M62	307	A46	A48	P2	32	33
M06	303	A49	A51	P1	31	32	M64	307	B49	B51	P2	34	35
M10	303	B56	B58	P1	34	35	M66	307	A49	A51	P2	36	37
M12	303	A56	A58	P1	36	37	M70	307	B56	B58	P2	38	39
M14	304	B46	B48	P1	38	39	M72	307	A56	A58	P2	40	41
M16	304	A46	A48	P1	40	41	M74	308	B46	B48	P2	42	43
M20	304	B49	B51	P1	43	44	M76	308	A46	A48	P2	44	45
M22	304	A49	A51	P1	45	46	M100	308	B49	B51	P5	1	2
M24	304	B56	B58	P2	1	2	M102	308	A49	A51	P5	3	4
M26	304	A56	A58	P2	3	4	M104	308	B56	B58	P5	5	6
M30	305	B49	B51	P2	5	6	M106	308	A56	A58	P5	7	8
M32	305	A49	A51	P2	7	8	M110	309	B49	B51	P5	9	10
M34	305	B56	B58	P2	9	10	M112	309	A49	A51	P5	11	12
M36	305	A56	A58	P2	11	12	M114	309	B56	B58	P5	13	14
M40	305	B46	B48	P2	13	14	M116	309	A56	A58	P5	15	16
M42	305	A46	A48	P2	15	16	M120	309	B46	B48	P5	18	19
M44	306	B46	B48	P2	18	19	M122	309	A46	A48	P5	20	21
M46	306	A46	A48	P2	20	21	M124	310	B46	B48	P5	22	23
M50	306	B49	B51	P2	22	23	M126	310	A46	A48	P5	24	25
M52	306	A49	A51	P2	24	25	M130	310	B49	B51	P5	26	27
M54	306	B56	B58	P2	26	27	M132	310	A49	A51	P5	28	29

4-66. TROUBLESHOOTING--Continued

Table 4-36. Memory Read Switches and Plugs--Continued

Memory channel	Read switch board pins			Memory Plug		Pins	Memory channel	Read switch board pins			Memory Plug		Pins
M134	310	B56	B58	P5	30	31	M316	312	A46	A48	P6	15	16
M136	310	A56	A58	P5	32	33	M320	312	B49	B51	P6	18	19
M300	311	B46	B48	P6	1	2	M322	312	A49	A51	P6	20	21
M302	311	A46	A48	P6	3	4	M324	312	B56	B58	P6	22	23
M304	311	B49	B51	P6	5	6	M326	312	A56	A58	P6	24	25
M306	311	A49	A51	P6	7	8	M330	313	B49	B51	P6	26	27
M310	311	B56	B58	P6	9	10	M332	313	A49	A51	P6	28	29
M312	311	A56	A58	P6	11	12	M334	313	A56	A58	P6	30	31
M314	312	B46	B48	P6	13	14	M336	313	A56	A58	P6	32	33

6 Replace the write switch boards 433 and 434 and rerun memory test. If the channel passes without a parity replace original boards one at a time to determine which one is defective. If new write switch boards do not correct the parity, replace original board and proceed to paragraph (7) below.

7 Replace write amplifier boards 437 and 439 and rerun memory test. If channel passes successfully, replace write amplifier boards one at a time to determine which one is defective. If the new write amplifiers do not correct parity, replace original boards and proceed to paragraph (8) below.

8 Determine from table 4-37 the circuit board associated with the write head wiring. For example, channel 004 is associated with write amplifier board 436. If the defective channel is associated with a circuit board which has not as yet been replaced, replace this board and rerun memory test. If the defective channel wiring is associated with a board that has already been replaced, proceed directly to paragraph (9) below.

9 Refer to TM 9-1220-221-34/1/1 and reference all boards, write switch and write amplifiers associated with the defective channel. For example, W64 has associated with it boards 436, 433, 437, 434, and 439. Replace these boards if not previously replaced and retest. If the channel passes successfully replace these boards one at a time to determine which one is defective. If replacement of these boards does not correct the error, replace the original boards and proceed to paragraph (10) below.

Table 4-37. Memory Write Amplifiers and Plugs

Channel	Write head wiring		Memory Plug	Pin	Channel	Write head wiring		Memory Plug	Pin
W00	439	A63	P4	1	W20	439	A57	P4	34
W00/	437	A63	P4	2	W20/	437	A57	P4	35
W00CT	434	A58	P4	17	W20CT	434	B64	P4	18
W02	438	A63	P4	3	W22	438	A57	P4	36
W02/	438	A4	P4	4	W22/	438	A12	P4	37
W02CT	434	A58	P4	17	W22CT	434	B64	P4	18
W04	436	A63	P4	5	W24	436	A57	P4	38
W04/	436	A4	P4	6	W24/	436	A12	P4	39
W04CT	434	A58	P4	17	W24CT	434	B64	P4	18
W06	435	A63	P4	7	W26	435	A57	P4	40
W06/	435	A4	P4	8	W26/	435	A12	P4	41
W06CT	434	A58	P4	17	W26CT	434	B64	P4	18
W10	434	B31	P4	9	W30	434	A31	P4	42
W10/	434	B38	P4	10	W30/	434	A38	P4	43
W10CT	434	A58	P4	17	W30CT	434	B64	P4	18
W12	434	A45	P4	11	W32	434	A46	P4	44
W12/	434	B40	P4	12	W32/	434	A41	P4	45
W12CT	434	A58	P4	17	W32CT	434	B64	P4	18
W14	433	B31	P4	13	W34	433	A31	P4	46
W14/	433	B38	P4	14	W34/	433	A38	P4	47
W14CT	434	A58	P4	17	W34CT	434	B64	P4	18
W16	433	A45	P4	15	W36	433	A46	P4	48
W16/	433	B40	P4	16	W36/	433	A41	P4	49
W16CT	434	A58	P4	17	W36CT	434	B64	P4	18

4-66. TROUBLESHOOTING--Continued

Table 4-37. Memory Write Amplifiers and Plugs--Continued

Channel	Write head wiring		Memory Plug	Pin	Channel	Write head wiring		Memory Plug	Pin
W40	439	B65	P3	1	W56CT	434	A6	P3	17
W40/	437	B65	P3	2	W60	439	A61	P3	34
W40CT	434	A6	P3	17	W60/	437	A61	P3	35
W42	438	B65	P3	3	W60CT	434	A2	P3	18
W42/	438	A3	P3	4	W62/	438	A6	P3	37
W42CT	434	A6	P3	17	W62CT	434	A2	P3	18
W44	436	B65	P3	5	W64	436	A61	P3	38
W44/	436	A3	P3	6	W64/	436	A6	P3	39
W44CT	434	A6	P3	17	W64CT	434	A2	P3	18
W46	435	B65	P3	7	W66	435	A61	P3	40
W46/	435	A3	P3	8	W66/	435	A6	P3	41
W46CT	434	A6	P3	17	W66CT	434	A2	P3	18
W50	434	B30	P3	9	W70	434	A30	P3	42
W50/	434	B37	P3	10	W70/	434	A37	P3	43
W50CT	434	A6	P3	17	W70CT	434	A2	P3	18
W52	434	A48	P3	11	W72	434	A39	P3	44
W52/	434	B43	P3	12	W72/	434	A43	P3	45
W52CT	434	A6	P3	17	W73CT	434	A2	P3	18
W54	433	B30	P3	13	W74	433	A30	P3	46
W54/	433	B37	P3	14	W74/	433	A37	P3	47
W54CT	434	A6	P3	17	W74CT	434	A2	P3	18
W56	433	A48	P3	15	W76	433	A39	P3	48
W56/	433	B43	P3	16	W76/	433	A43	P3	49

Table 4-37. Memory Write Amplifiers and Plugs--Continued

Channel	Write head wiring		Memory Plug	Pin	Channel	Write head wiring		Memory Plug	Pin
W76CT	434	A2	P3	18	W116CT	433	A2	P8	18
W100	439	A64	P8	1	W120	439	A60	P8	34
W100/	437	A2	P8	2	W120/	437	A60	P8	35
W100CT	433	A2	P8	18	W120CT	433	A6	P8	30
W102	438	A64	P8	3	W122	438	A60	P8	36
W102/	438	A2	P8	4	W122/	438	A7	P8	37
W102CT	433	A2	P8	18	W122CT	433	A6	P8	30
W104	436	A64	P8	5	W124	436	A60	P8	38
W104/	436	A2	P8	6	W124/	436	A7	P8	30
W104CT	433	A2	P8	18	W124CT	433	A6	P8	30
W106	435	A64	P8	7	W126	435	A60	P8	40
W106/	435	A2	P8	8	W126/	435	A7	P8	41
W106CT	433	A2	P8	18	W126CT	433	A6	P8	30
W110	434	B34	P8	9	W130	434	B35	P8	42
W110/	434	A28	P8	10	W130/	434	B28	P8	43
W110CT	433	A2	P8	18	W130CT	433	A6	P8	30
W112	434	A20	P8	11	W132	434	A19	P8	44
W112/	434	B24	P8	12	W132/	434	A24	P8	45
W112CT	433	A2	P8	18	W132CT	433	A6	P8	30
W114	433	B34	P8	13	W134	433	B35	P8	46
W114/	433	A28	P8	14	W134/	433	B28	P8	47
W114CT	433	A2	P8	18	W134CT	433	A6	P8	30
W116	433	A20	P8	15	W136	433	A19	P8	48
W116/	433	B24	P8	16	W136/	433	A24	P8	49

4-66. TROUBLESHOOTING--Continued

Table 4-37. Memory Write Amplifiers and Plugs--Continued

Channel	Write head wiring		Memory Plug	Pin	Channel	Write head wiring		Memory Plug	Pin
W136CT	433	A6	P8	30	W316CT	433	A58	P7	18
W300	439	A65	P7	1	W320	439	A59	P7	34
W300/	437	A65	P7	2	W320/	437	A59	P7	35
W300CT	433	A58	P7	18	W320CT	433	B64	P7	30
W302	438	A65	P7	3	W322/	438	B7	P7	37
W302/	438	A1	P7	4	W322CT	433	B64	P7	30
W302CT	433	A58	P7	18	W324	436	A59	P7	38
W304	436	A65	P7	5	W324/	436	B7	P7	39
W304/	436	A1	P7	6	W324CT	433	B64	P7	30
W304CT	433	A58	P7	18	W326	435	A59	P7	40
W306	435	A65	P7	7	W326/	435	B7	P7	41
W306/	435	A1	P7	8	W326CT	433	B64	P7	30
W306CT	433	A58	P7	18	W330	434	B36	P7	42
W310	434	A36	P7	9	W330/	434	B29	P7	43
W310/	434	A29	P7	10	W330CT	433	B64	P7	30
W310CT	433	A58	P7	18	W332	434	B26	P7	44
W312	434	A26	P7	11	W322/	434	A23	P7	45
W312/	434	B23	P7	12	W322CT	433	B64	P7	30
W312CT	433	A58	P7	18	W334	433	B36	P7	46
W314	433	A36	P7	13	W334/	433	B29	P7	47
W314/	433	A29	P7	14	W334CT	433	B64	P7	30
W314CT	433	A58	P7	18	W336	433	B26	P7	48
W316	433	A26	P7	15	W336/	433	A23	P7	49
W316/	433	B23	P7	16	W336CT	433	B64	P7	30

10 Refer to table 4-36 and determine memory plug associated with defective channel. For example, channel 024 is plug P2 pins 1 and 2. Remove the plug from the memory, clean the male pins on the memory jack and the female pins on the plug using trichloroethylene (NSN 6810-00-664-0338). Reconnect plug and tighten securely. Repeat cleaning procedure for memory plug used in writing; refer to table 4-37 for plug and pins associated with write circuitry. Rerun memory test; if parity persists, proceed to paragraph (11) below.

CAUTION

When using the ohmmeter to measure resistance do not place ohmmeter probes on pins B39 and B41 of read switch board 303 or pins B59 and B60 of pulse generator board 432. Do not place ohmmeter probes on pins 22, 23, 47, and 48 of memory jack J001. These are the sector track and clock read heads and this information may be damaged by the ohmmeter current.

NOTE

For any given memory unit the resistance measured should be the same for all heads. For example: if resistance measured was 17 ohms then all heads should be near 17 ohms. Use extra caution in establishing a good electrical contact when using the ohmmeter for this measurement.

11 Remove the read switch board associated with the defective channel according to table 4-36. Make a resistance measurement between the two pins on the read switch board connector. For example, channel 042 is board connector 305 pins A46 and A48. The ohmmeter should be on the R x 1 range; zero the meter to obtain the most accurate measurement. The resistance should be between 14 and 19 ohms. The resistance of the read head should be constant, that is, it should not vary in any way. When the resistance is changing or slowly floating it usually indicates a cold solder joint or an insecure connection in the wiring, plug, or memory. To eliminate the wiring and plug remove the plug and check the resistance directly at the memory jack; check continuity of wiring between memory plug and board pin. Examine plug to eliminate possibility of a loose solder connection within the memory plug itself which could cause intermittent parity errors. Refer to table 4-36 for the correct pins. When the resistance measurement of the read head is less than 14 ohms or more than 19 ohms the read head may be defective; however, before changing the memory measure the read circuitry ground loop resistance according to step (13) of this procedure. An open or cold solder joint in the group loop may result in a parity. If the read head resistance measurement is between 14 and 19 ohms proceed to step (12) of this procedure.

12 Refer to table 4-37 and determine the write head wiring connections for the defective channel. Measure the resistance between the one and prime sides of the write head first. The resistance measurement should be 2 ohms. Now measure the resistance between each side and the center tap. The resistance measurement should be 1 ohm. When the resistance is not within tolerance, check the wiring and plug before changing the memory. If the resistance is within tolerance, proceed to step (13).

4-66. TROUBLESHOOTING--Continued

CAUTION

When using the ohmmeter to measure resistance do not place the ohmmeter probes on pins 21, 22, and 23 of memory jack J003 or pins 21, 22, and 23 of memory jack J004. These pins are the write head connections for the clock and sector track and the information will be damaged by the ohmmeter current.

13 Locate board connector 301 pin B60. Remove (unsolder) the black wire from 313 A57 on 301 B60. Do not remove the remaining black wire on this pin. Insert an ohmmeter in series with pin B60 and the wire that was removed. The resistance would be 0.5 ohms or less. When the resistance is greater than 0.5 ohms there is a cold solder joint in the ground loop, refer to figure 4-90 for read shield ground wiring. After making the resistance measurement replace the wire on pin B60, board 301. When it appears that the parity error exists only during the first few minutes of operation or that the parity error is intermittent it may be helpful to run the memory test in one of the five marginal test positions. An intermittent parity may become more consistent in a marginal position which will aid in trouble-shooting. If it appears that the parity error disappears after running the computer in a few minutes it may also be helpful to measure the resistance of the read and write heads before turning the computer on and then again after the computer has operated for a period of time and compare the measurements.

14 When the resistance measurement of the read or write head indicates either one is defective or after all other possibilities have been exhausted, the memory should be replaced. (Refer to para 5-8.) If possible, the defective memory should be installed in another computer to verify that it is the cause of the parity. With a new memory in the computer the defective channel must pass the memory test.

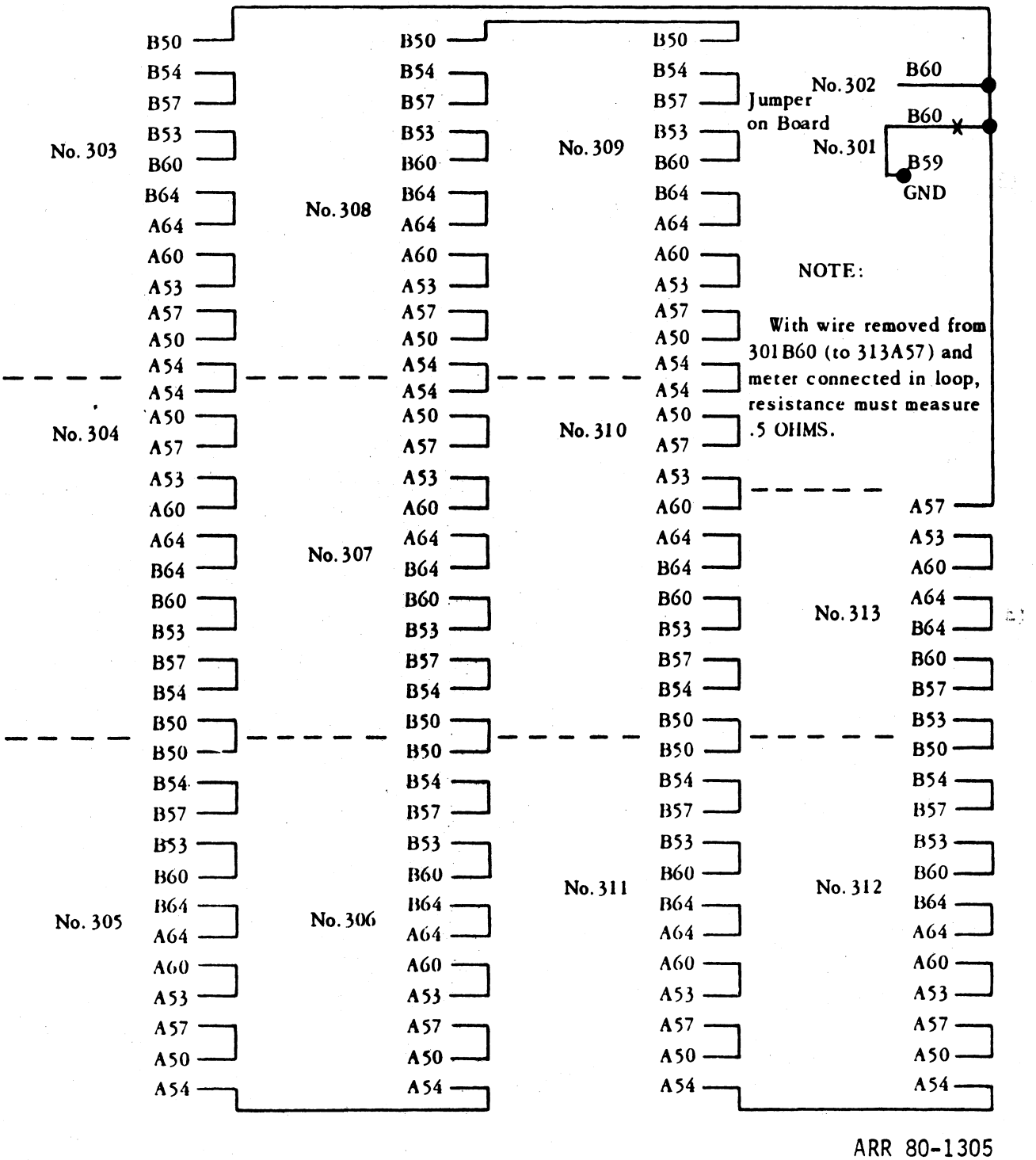


Figure 4-90. Shield Ground Loop for Read Head Circuitry.

Section VII. Computer Board Circuitry

4-67. SCOPE

This section provides the technician with a detailed explanation and an electrical schematic of each FADAC circuit board. It contains a brief theory of operation on the circuitry located on each board and a reference to other sections of this chapter that utilize these various circuits.

NOTE

All component designations can be referenced to actual component value by referring to TM 9-1220-221-34P under the board in question.

4-68. POWER CONTROL A BOARD

The power control A board is intended to monitor extreme ambient temperature conditions and to detect cooling fan failures. The board consists of the low memory temperature detector, the low and high temperature warning detector, and the low and high temperature kickout detector circuits. TM 9-1220-221-34/1/1 contains the schematic of the power control A board. See section II for its integrated function in power control of the FADAC.

4-69. POWER CONTROL B BOARD

a. High Voltage Kickout Detector. Gives a false output (0 volts) when prime input voltage exceeds 140 vac. This prime input voltage level is detected by an unregulated -27-volt power control power supply. When the input prime voltage is at 140 vac the output from the unregulated -27-volt source is -31.5 volts. This unregulated source is the input to the high voltage kickout detector.

b. Low Voltage Kickout Detector. Gives a false output (0 volts) when prime input voltage is less than 80 vac. The input to the low voltage kickout detector is the same -27-volt unregulated supply to the detector will be -16.5 volts if the prime voltage is 80 vac.

c. Low Voltage Warning Detector. Gives a false output voltage (0 volts) when prime input voltage is 108 vac or less. The -27-volt input source will be at -20 volts or greater (e.g., -19 volts). The TRANS indicator will flash.

d. High Voltage Warning Detector. Gives a false output voltage (0 volts) when prime input voltage is 132 vac or more. The -27 volt input source will be at -29.5 volts or less (e.g., -30 volts).

e. Low Voltage Transient Kickout. Gives a false output voltage (0 volts) when prime input voltage is below 100 vac for 7 or more seconds. The -27-volt input voltage will be -18.6 volts for 7 or more seconds.

f. Voltage Warning Inverter. Gives a true output signal when one or both of the inverter inputs are false. See foldout-1 for inputs to voltage warning inverter.

g. Main Power Relay Driver. Activates the main relay which applies power to the computer.

h. Memory Motor Relay Driver. Activates a relay to apply the power to the memory motor when the memory motor temperature is above a specific limit.

NOTE

See section II for the power control B board function of the computer.

4-70. POWER CONTROL C BOARD

Power control C board consists of and is intended to do the following:

a. TD/WI Flip-flop. Inhibits the normal operation during the turnon and turnoff state of the computer.

b. TD Circuit. Allows the memory motor to attain operating speed during the turnon state.

c. Temperature Warning Inverter. Gives a true output signal when one or both of the inverter inputs is false. See foldout-1 for input terms.

d. Keyboard and Mechanical Reader Solenoid Switch Driver. Operates power transistors. See section V for further explanation.

e. Primary Power Rectifiers. Applies a dc voltage to a relay (K1) (FO-1).

f. Phase Detector Rectifiers. Operates relays to apply the proper phase voltage to the memory and blower motors. See section II of this chapter.

NOTE

See section II for the power control C board function of the computer and section V for circuits associated with input-output circuitry.

4-71. POWER SUPPLY SUBASSEMBLY (CAPACITOR ASSEMBLY)

NOTE

Refer to section III for the power supply function in the power supply circuitry.

This assembly consists of two fullwave diode rectifier bridges, various capacitors, a power transistor, and a power resistor used in the power supply circuits of the computer. Each rectifier bridge circuit uses six diodes to supply fullwave rectified voltages to the +150-volt regulator and the -18-volt pwm (pulse width modulated) regulator. The power transistor is used as a shunt regulating element in the -1.5-volt regulator. The capacitors are used throughout the power supply circuits as filter capacitors, blocking capacitors, and by-pass capacitors.

4-72. TRANSISTOR ASSEMBLY BOARD

NOTE
Refer to section III for its function in power supply circuitry.

This assembly consists of six PNP transistors which are used as series or shunt regulating elements in the power supplies used in the computer. These transistors operate either class A (between cutoff and saturation) or as a switch (cutoff or saturation). The impedance presented by each transistor may be controlled by the base. Regulation of the external circuit is thereby obtained.

4-73. RECTIFIER TRANSISTOR ASSEMBLY BOARD

NOTE
Refer to section III for its function in power supply circuitry.

This assembly houses the power rectifiers used to convert three-phase voltage into dc voltages. It also contains the medium power transistors used as drivers for several of the regulated power supplies. Zener diodes, mounted on the board, are used to establish bias levels for the power supplies.

4-74. VOLTAGE REGULATOR SUBASSEMBLY (REGULATOR NO. 1) BOARD

NOTE
Refer to section III for its function in power supply circuitry.

This voltage regulator subassembly contains the control elements of a +6-volt-type series-voltage regulator, a +3-volt shunt-type voltage regulator, and a -3-volt shunt-type voltage regulator. Provisions are made for fail safe remote sensing at the load for increasing or decreasing the output voltage by five percent for marginal testing procedures. Temperature compensated over-current protection is provided for the +6-volt and the -10-volt regulators. When overcurrent conditions are detected, a signal is sent to an external master trip circuit that shuts down selected regulators. Efficiency is increased by directing the +6-volt load current through the -3-volt shunt regulator and its load.

4-75. VOLTAGE REGULATOR SUBASSEMBLY (REGULATOR NO. 2) BOARD

NOTE
Refer to section III for its function in power supply circuitry.

This voltage regulator contains the control elements of a ±150-volt series-type voltage regulator, a -1.5-volt shunt-type regulator, and a +15-volt series-type regulator. Provisions are made for fail safe remote sensing at the load for increasing or decreasing the +15-volt output voltage by five percent for marginal testing procedures. Temperature compensated overcurrent protection is provided for the 150-volt and +15-volt regulators. When over-current conditions are detected, a signal is sent to an external master trip circuit that shuts down selected regulators.

4-76. VOLTAGE REGULATOR SUBASSEMBLY (REGULATOR NO. 3) BOARD

NOTE
Refer to section III for its function in power supply circuitry.

This voltage regulator subassembly contains the sensing and amplifier portions of a +1.25-volt shunt regulator, the sensing and amplifier portions of a -18-volt pulse width modulated regulator and nixie neon supply circuits.

a. +1.25-Volt Shunt Regulator. With the output power transistors connected to the voltage regulator and the -18-volt pulse width modulated regulator operating to supply the current, the +1.25-volt shunt regulator is designed to maintain its +1.25-volt level for a load of 1.27 to 1.88 amps.

b. -18-Volt Pulse Width Modulated Regulator. With the output power transistors and the filtering portions connected to the voltage regulator the -18-volt pulse width motor modulator is designed to maintain -18 volts for variation in a load from 3.2 to 5.6 amps.

c. Nixie Neon Supply. The nixie neon supply by the use of zener diodes and a +150-volt supply will output +138-volt, +73-volt bias voltage for the nixie driver circuits.

4-77. VOLTAGE REGULATOR SUBASSEMBLY (REGULATOR NO. 4) BOARD

NOTE
Refer to section III in power supply circuitry.

This voltage regulator subassembly contains the sensing and amplifier portions of a +35-volt series regulator, the sensing and amplifier portions of a 6-volt pulse width modulated regulator, and a master trip circuit.

a. +35-Volt Series Regulator. With the output power transistors connected to the voltage regulator the +35-volt series regulator is designed to maintain +35 volts for a variation in load from 0.39 to 1.02 amps.

b. -6-Volts Pulse Width Modulated Regulator. With the output power transistors and the filtering portions connected to the voltage regulator the -6-volt pulse width modulated regulator is designed to maintain -6 volts for a load variation from 3.8 to 6.7 amps.

c. Master Trip Circuit. With the master trip circuit connected to the +150-, +35-, ±15-, +6-, -6-, -10-, and -18-volt regulators, the master trip circuit will turn off all of the above regulators whenever an overcurrent is sensed by any one of the above regulators. The master trip circuit remains tripped until it is reset by removing the power from the master trip circuit by turning off the computer.

4-78. PULSE GENERATOR (CLOCK)

The pulse generator is intended to form, amplify, and generate three output signals to be used for synchronizing the computer circuits. The input is derived from a synchronous 448 KHz sine wave signal, permanently recorded on the timing or clock channel of the memory disk. The theory of operation is as follows (fig. 4-91):

a. Clock Pulse Circuits. The clock sine wave from the memory disk is amplified in the preamplifier and applied to the first limiter stage as a 3 ±2-volt peak-to-peak signal. This sine wave is shaped into a

4-78. PULSE GENERATOR (CLOCK)--Continued

square wave in two successive limiter (clipping) stages. The output of the second limiter stage is the input into a differentiator and drive. Differentiation of the input square wave results in an output of positive and negative pulses. The negative going pulse drives an emitter-follower into conduction which in turn triggers the next stage, a monostable multivibrator. The monostable multivibrator (one shot) generates the required pulse width of the clock pulse. Circuit constants of the one shot are such that the clock pulse is true for 1.7 microseconds and false for 0.5 microseconds. True level is -6 volts ±1 volt, false level is 0 to -0.5 volts. The clock pulses are then applied to the two final amplifiers to develop the clock output and the strobe output. The strobe output is the exact inversion of the clock output. The strobe output is used in read amplifier circuits.

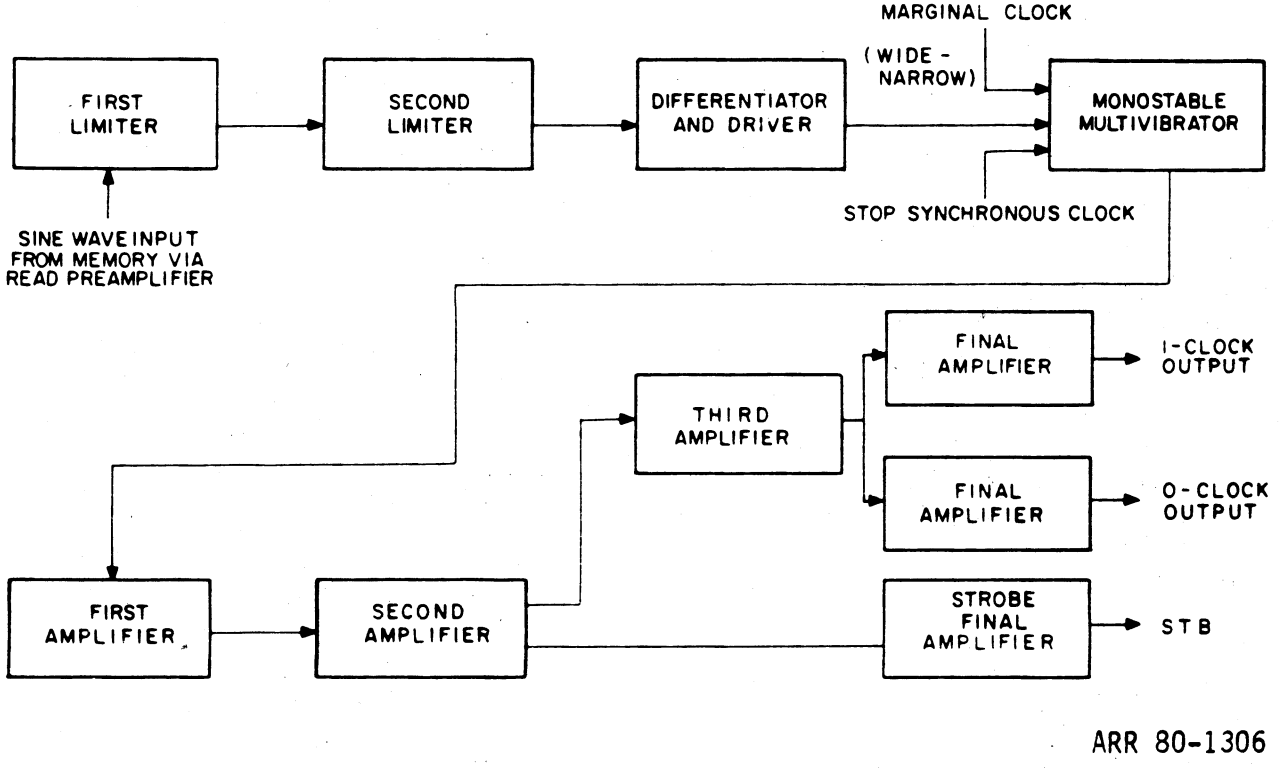


Figure 4-91. Block Diagram of Clock Pulse Circuits.

b. Split Synchronous Clock. The clock pulse drivers are so arranged that one set of clock pulse drivers drive the one side (1 clock output) of all flip-flops while a second set drive the zero side (Ø clock output) of all flip-flops.

4-79. LOGIC FLIP-FLOP BOARD

NOTE
Refer to section IV to see how the FALT tests these flip-flops and logic gates.

The logic flip-flop circuit board consists of two bistable multivibrator circuits used for performing logical computer processes such as counting and storing information. Each bistable multivibrator is capable of driving 28 standard logical gates. Each flip-flop has a zero side input and output and a one side input and output. When the logic to the one input is true and the clock pulse goes false the one output of that flip-flop will be true (-6 volts) and zero output will be false (0 volts). It will remain in this state until the logic for the zero side comes true and the clock pulse goes false. At this time the one output will be false (0 volts) and zero output will be true (-6 volts). The circuit board also contains logic gates ("and" and "or" gates) which are connected to various points in the computer to mechanize the logical processes which the computer performs.

4-80. LOGIC DRIVER BOARD

The logic driver circuit board consists of 20 identical driver circuits. Each circuit is used to provide power amplification of primary "and" gate outputs to drive 20 secondary "and" gates.

4-81. NETWORK A BOARD

There are five of these boards in the computer. On each board there are five input drivers, five output drivers, a logic driver, and two neon drivers. The theory of operation of each circuit is explained below.

NOTE
Refer to table 4-38 for A_0 input and output terms for all network A boards.

a. Output Driver. These drivers consist of two transistor circuits using Q1 and Q8, Q2 and Q9, Q3 and Q10, Q4 and Q11, and Q5 and Q12. These drivers convert logic signals into output signals. An example of a typical output driver is shown in figure 4-92. When A_0 input is false (0 volts) Q1 is in effect open. The voltage at the base of Q8 is -6 volts. The bias voltage at the emitter to base junction of Q8 is 0. Therefore, Q8 is in effect open, resulting in a false output at the collector. When A_0 input is true (-6 volts) Q1 is forward biased and hence turns on. The collector of Q1 is now a potential of -1.5 volts. The base of Q8 is now more positive than the emitter and hence this transistor turns on producing a true output or -6 volts.

b. Input Driver. These drivers consist of two transistor circuits using Q13 and Q18, Q14 and Q19, Q15 and Q20, Q16 and Q21, and Q17 and Q22. These circuits convert computer input signals into logic signals. An example of a typical input driver circuit is shown in figure 4-93. When A_1 input is false (0 volts) Q13 is forward biased. The base of Q13 will be approximately -1.5 volts. Q13 is now forward biased and will conduct. A_1 output will be at a false potential (0 volts) due to the forward bias of CR19. When A_1 input is true (-6 volts) Q13 is

4-81. NETWORK A BOARD--Continued

reverse biased and its collector voltage arises to +6 volts. This voltage reverse biases Q18 cutting it off. The A_1 output is now at a true level (approximately -6 volts).

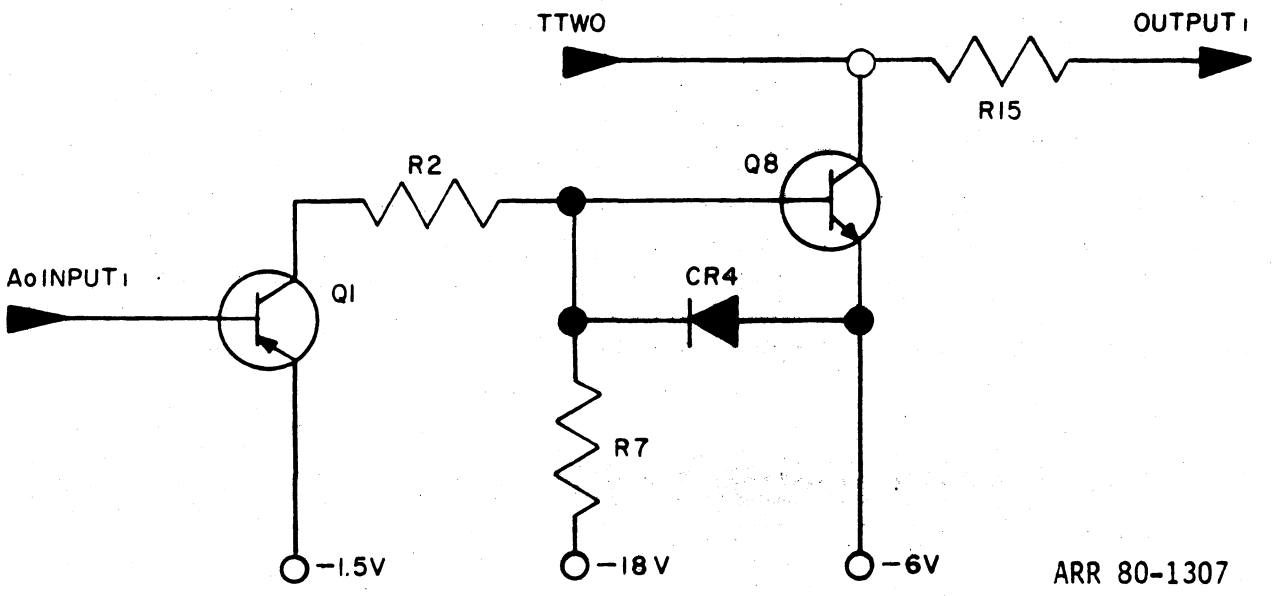


Figure 4-92. A_0 Driver Circuit.

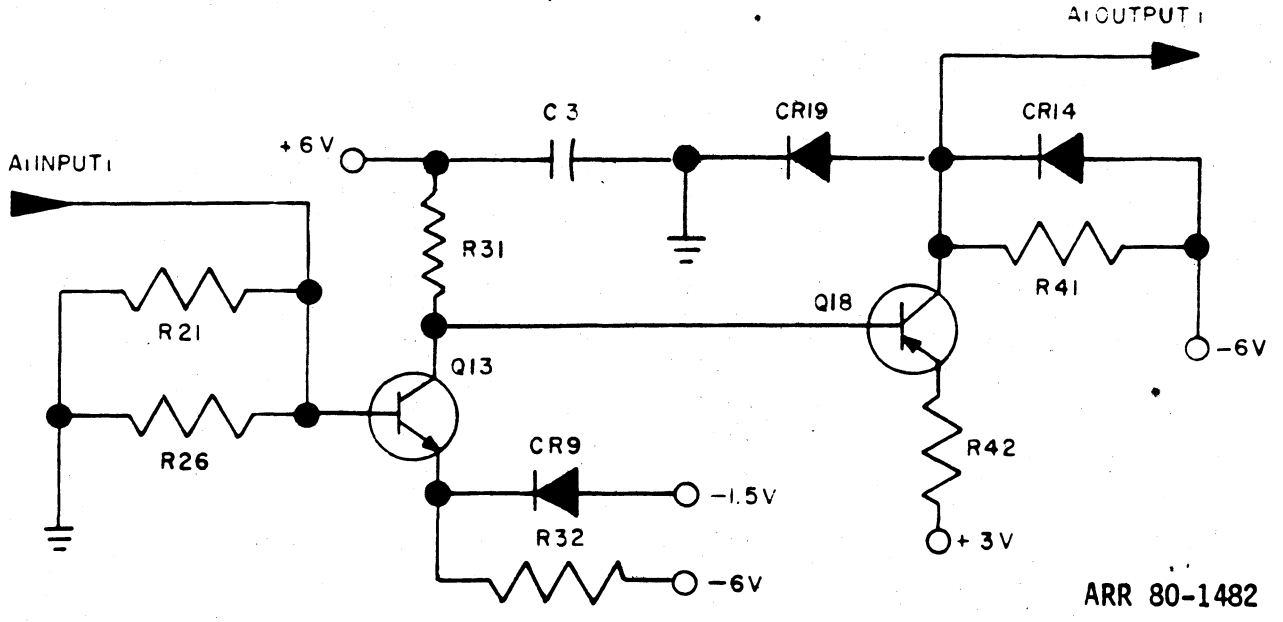


Figure 4-93. A_1 Driver Circuit.

c. Logic Driver. This circuit is the same as those on the logic driver board. The transistors used are Q23 and Q25.

NOTE

Refer to table 4-38 for A_1 input and output terms for all network A boards.

d. Neon Driver. These drivers consist of two transistor circuits, Q6 and Q7 in one and Q24 and Q26 in the other. These circuits utilize logic signals to drive the neon indicators on the front panel. The two neon driver circuits are shown in figure 4-94 for N1 drivers and figure 4-95 for N2 drivers.

NOTE

Refer to table 4-38 for N1 and N2 input and output terms for all network A boards.

(1) N1 neon drivers. When any one of the N1 outputs are false the emitter of Q6 will be at a 0-volt potential. Q6 is now biased off. Since Q7 is open circuited, the collector of Q7 will see the voltage developed by the voltage driver made up of R13 and R14 or approximately +111 volts. N1 output is connected to one side of a neon lamp. The other side of the neon lamp is connected to +138 volts. Approximately 90 volts difference of potential is needed to ionize the lamp. Therefore, with +111 volts at the collector of Q7 and +138 volts on the other side of the neon lamp, the lamp will not light. When all the N1 inputs are true the emitter of Q6 will be at a -6 volt potential and that transistor will be forward biased. Q7 now has a return path and therefore, will conduct. The collector of Q7 will be at approximately -6-volt potential. The voltage across the neon lamp is now sufficient to cause ionization.

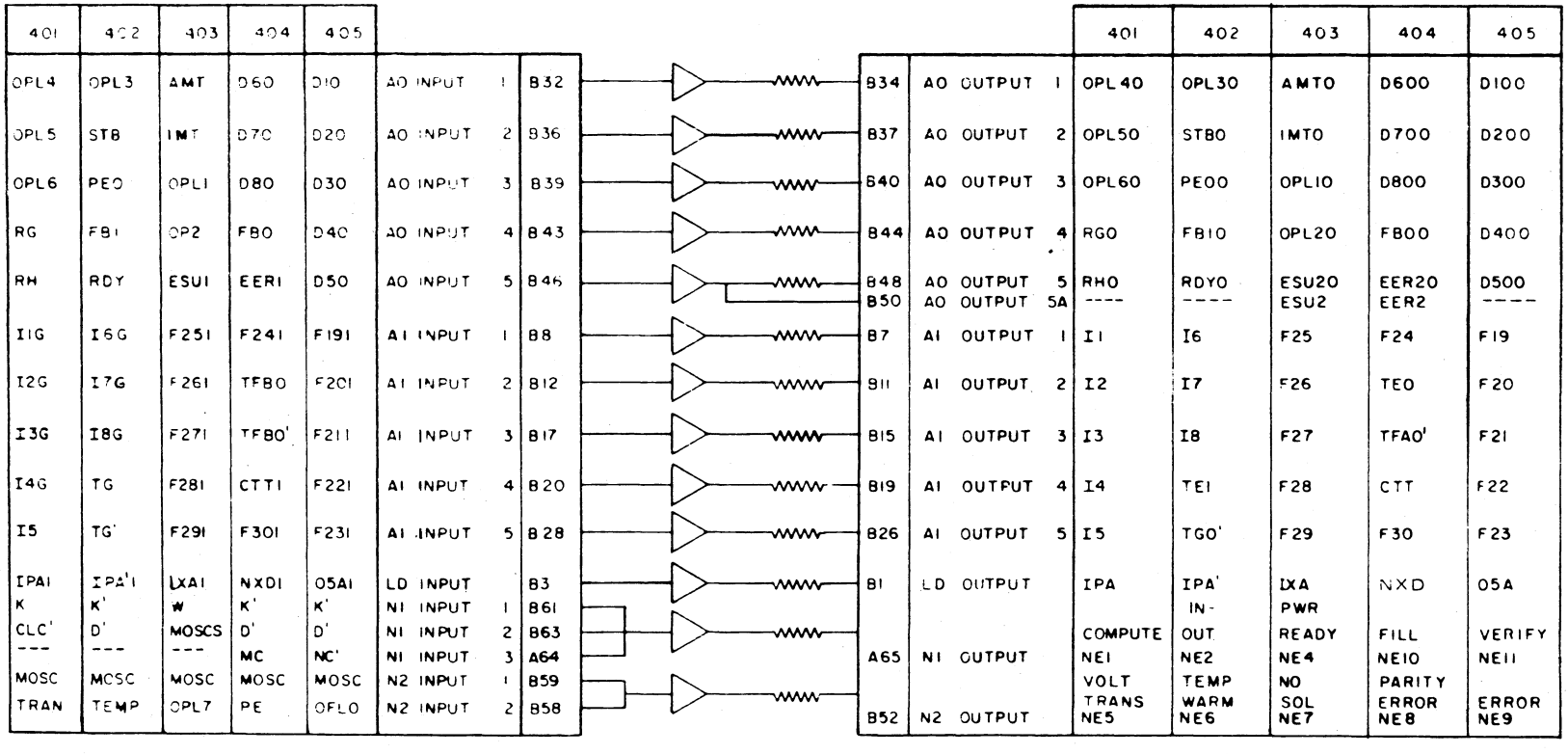
(2) N2 neon drivers. When any one of the N2 outputs is false, a 0-volt potential will be present at the base of Q24. The emitter of Q24 will be present at the base of Q24. The emitter of Q24 will be at a -3-volt potential. Therefore, Q24 will conduct being forward biased. Q26 will also be forward biased and will conduct heavily; -3 volts will be present at the collector of Q26. The N2 output is connected to one side of a neon lamp. The other side of the lamp is connected to +138 volts. With N2 output approximately at -3 volts, the lamp will light. When all the inputs are true the base of Q24 will be at a -6-volt potential. This will in turn cut off Q24 and open circuit Q26. The collector of Q24 will not be at a +150-volt potential and the neon lamp will extinguish.

e. Matrix Decoder. The decoder matrix consists of the diodes shown in TM 9-1220-221-34/1-1 on all five network A boards. This circuit is used to convert the signals from the matrix buttons, the set up buttons, etc, into the proper codes for use in logic.

NOTE

Refer to section V to see its use in input-output circuitry.

Table 4-38. Network A Input and Output (sheet 1 of 3).



401	402	403	404	405						401	402	403	404	405
OPL4	OPL3	AMT	D60	D10	AO INPUT 1	B32	B34	AO OUTPUT 1		OPL40	OPL30	AMTO	D600	D100
OPL5	STB	IMT	D70	D20	AO INPUT 2	B36	B37	AO OUTPUT 2		OPL50	STBO	IMTO	D700	D200
OPL6	PEO	OPL1	D80	D30	AO INPUT 3	B39	B40	AO OUTPUT 3		OPL60	PEOO	OPL1O	D800	D300
RG	FB1	OP2	FBO	D40	AO INPUT 4	B43	B44	AO OUTPUT 4		RGO	FB1O	OPL2O	FB00	D400
RH	RDY	ESU1	EER1	D50	AO INPUT 5	B46	B48	AO OUTPUT 5		RHO	RDYO	ESU2O	EER2O	D500
							B50	AO OUTPUT 5A		----	----	ESU2	EER2	----
I1G	I6G	F251	F241	F191	AI INPUT 1	B8	B7	AI OUTPUT 1		I1	I6	F25	F24	F19
I2G	I7G	F261	TFBO	F201	AI INPUT 2	B12	B11	AI OUTPUT 2		I2	I7	F26	TEO	F20
I3G	I8G	F271	TFBO'	F211	AI INPUT 3	B17	B15	AI OUTPUT 3		I3	I8	F27	TFAO'	F21
I4G	TG	F281	CTT1	F221	AI INPUT 4	B20	B19	AI OUTPUT 4		I4	TEI	F28	CTT	F22
I5	TG'	F291	F301	F231	AI INPUT 5	B28	B26	AI OUTPUT 5		I5	TGO'	F29	F30	F23
IPA1	IPA'1	LXA1	NXD1	05A1	LD INPUT	B3	B1	LD OUTPUT		IPA	IPA'	IXA	NXD	05A
K	K'	W	K'	K'	N1 INPUT 1	B61					IN-	PWR		
CLC'	D'	MOSCS	D'	D'	N1 INPUT 2	B63				COMPUTE	OUT	READY	FILL	VERIFY
---	---	---	MC	NC'	N1 INPUT 3	A64	A65	N1 OUTPUT		NE1	NE2	NE4	NE10	NE11
MOSC	MOSC	MOSC	MOSC	MOSC	N2 INPUT 1	B59				VOLT	TEMP	NO	PARITY	
TRAN	TEMP	OPL7	PE	OFLO	N2 INPUT 2	B58	B52	N2 OUTPUT		TRANS NE5	WARM NE6	SOL NE7	ERROR NE8	ERROR NE9

Table 4-38. Network A Input and Output (sheet 2 of 3).

401	402	403	404	405		
SU0	SU2	SE	SB	S5	D1 INPUT 1	A3
SU1	SU3	SF	SD	S6	D1 INPUT 2	A5
SU2	SU6	SG	SF	S7	D1 INPUT 3	A6
SU3	SU7A	SH	SH	S8	D1 INPUT 4	A8
SU4	SU1	SE	S1	S5	D2 INPUT 1	A12
SU5	SU3	SF	S2	S6	D2 INPUT 2	A14
SU6	SU5	SG	S3	S7	D2 INPUT 3	A15
SU7A	SU7A	SH	S4	S8	D2 INPUT 4	A18
SU4	SAX	SC	S2	S3	D3 INPUT 1	A22
SU5	SB	SD	S4	S4	D3 INPUT 2	A23
SU6	SC	SG	S6	S7	D3 INPUT 3	A25
SU7A	SD	SH	S8	S8	D3 INPUT 4	A26
SUC'	SU3'	SU6'	TCK'	F11'	CL1INPUT	A4
SU1'	SU4'	SU7'	F9'	F12	CL2INPUT	A11
SU2'	SU5'	TCR'	F10	F13'	CL3 INPUT	A19
F9	F10	F11	F12	F13	CLAMP	A32
GPSS'	SL	SPHH'	TR'	TFAI'	CL5INPUT	A55
----	SU7A	SU7A	SR		DIODE 1A	A31
-----	-----	-----	----		DIODE 2A	A28

		401	402	403	404	405
A7	D1 OUTPUT	SU	SU2L	SL	F5	F4
A13	D2 OUTPUT	SU	SU1L	F7	SR	SR
A20	D3 OUTPUT	SU3L	SL	F6	F2	F3
A10	CL1 OUTPUT	SU'	SU'	SU'	TC'	SUB'
A17	CL3 OUTPUT	SU'	SU'	SU'	SUB'	SUB'
A24	CL3 OUTPUT	SU'	SU'	TC'	SUB'	SUB'
B25	+15V	←		+15V		→
B23 B24	GRD. PWR	←	GRD	PWR		→
A54	CL5 OUTPUT	GPS'	F1	GPH'	TEL'	TEO'
B5	-18V	←		-18V		→
A34	DIODE 1B	---	SU7	ESU2	F1	
A2	DIODE 2B	---	---	---	---	

4-81. NETWORK A BOARD--Continued

Table 4-38. Network A Input and Output (sheet 3 of 3).

401	402	403	404	405		
CN4'	CN4	CP4'	CP4	CP7'	P12 INPUT 1	A44
CN3'	CN3'	CP3'	CP3'	CP6'	P12 INPUT 2	A46
CN2'	CN2'	CP2'	CP2'	CP5'	P1 INPUT 3	A40
E6	EM4	E6	EM4	E7	P1 INPUT 4	A41
CN2	CN2	CP2	CP2	CP5	P2 INPUT 3	A50
EM2	EM3	EM2	EM3	EM5	P2 INPUT 4	A51
CN4'	CN4	CP4'	CP4	CP7'	P34 INPUT 1	A59
CN3	CN3	CP3	CP3	CP6	P34 INPUT 2	A58
CN2'	CN2'	CP2'	CP2'	CP5'	P3 INPUT 3	A57
EM3	EM2	EM3	EM2	EM7	P3 INPUT 4	A61
CN2	CN2	CP2	CP2	CP5	P4 INPUT 3	A62
EM4	E6	EM4	E6	E7	P4 INPUT 4	A63

401	402	403	404	405		
A38	P1 OUTPUT	CNL0	CNL4	CPL0	CPL4	CPU0
A48	P2 OUTPUT	CNL1	CNL5	CPL1	CPL5	CPU1
A56	P3 OUTPUT	CNL2	CNL6	CPL2	CPL6	CPU2
A60	P4 OUTPUT	CNL3	CNL7	CPL3	CPL7	CPU3
B5	-18V				-18V	
A52	-6V				-6V	

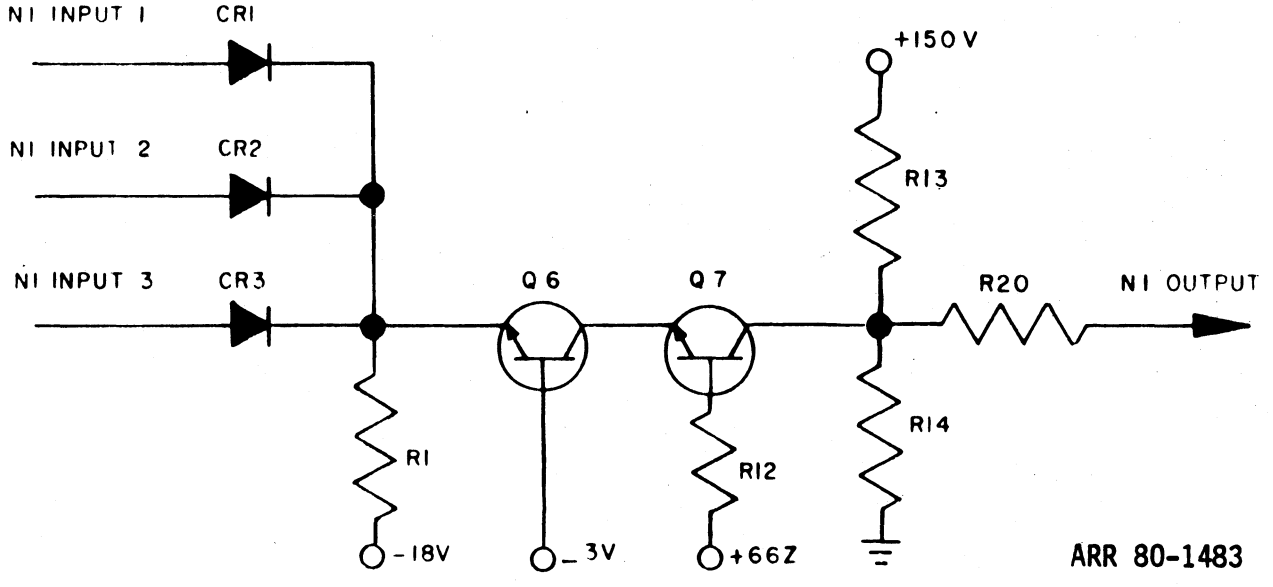


Figure 4-94. Neon N_1 Driver Circuit.

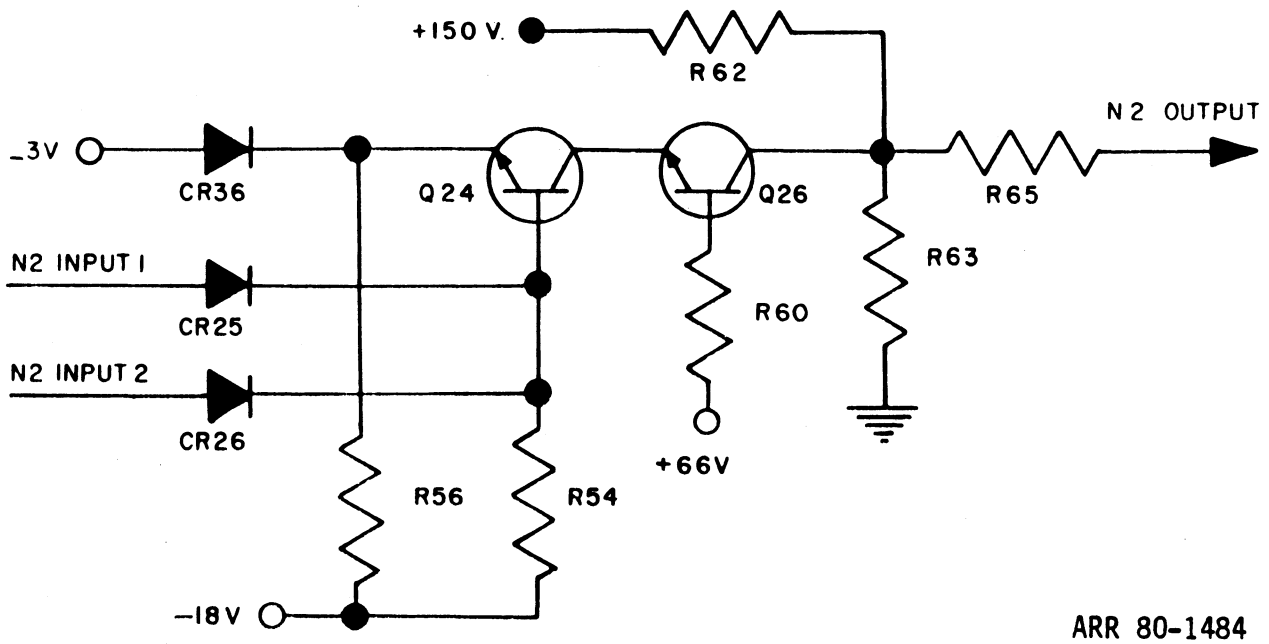


Figure 4-95. Neon N_2 Driver Circuit.

4-82. NETWORK B BOARD

The board has 1 anode driver, 12 cathode drivers, 1 inverter, 1 clock driver, and 5 clamping circuits on it. There are four network boards.

NOTE

Refer to TM 9-1220-221-34/1/1 for input and output terms of all network B boards.

a. Anode Driver. This circuit uses Q2, Q11, and Q12. The anode driver controls the voltage on the anodes of the nixies on the readout panel. Refer to section V for its function in outputting information through the nixies.

b. Cathode Driver. These are one-transistor circuits using Q3 thru A8 and Q13 thru Q19. The cathode drivers control the voltage on the cathode of the nixies on the readout panel. Refer to section V for its function in outputting information through the nixies.

c. Inverter. Q9 is the only transistor in the inverter. This circuit inverts a clock signal to provide a strobe signal to field data equipment.

4-82. NETWORK B BOARD--Continued

d. Clock Driver. Q1 and Q10 are in this circuit. The clock driver supplies a clock signal to field data equipment.

e. Clamping Circuits. These clamps use CR17, CR18, CR19, CR21, and CR22. They are used to clamp the input lines from keyboard, the mechanical reader, and the SDR. The clamp using CR22 has an "or" gate connected to it so that the FALT signal may replace the input signal.

NOTE
Refer to section V for use of some of these circuits.

4-83. NETWORK C BOARD

This board contains a 10 Hz multivibrator, a neon driver, pulse stretcher circuits (PS1 and PS2 one shot), the clock strobe circuit, the teletype (TT) flip-flop and a battery anode supply circuit (BAD supply).

a. Neon Driver. Transistors Q5 and Q6 make up the neon driver circuit which controls the illumination of the KEYBOARD indicator (NE-3) on the control panel. Circuit operation is identical to that of neon driver no. 1 on network A board (para 4-81d).

b. PS1 One-Shot. Q15, Q18, Q19, Q22, Q24, and Q28 are in this circuit. The PS1 one-shot is used with field data equipment while inspecting signals to the computer. It is used to delay input signals by a period of 6.2 microseconds or greater. Refer to section V for its purpose in inputting signals.

c. PS2 One-Shot. Q15, Q17, Q20, Q23, Q25, and Q29 are used in this circuit. It is used with field data equipment while outputting signals from the computer. Refer to section V for its use in outputting signals.

d. Clock Strobe. This circuit uses Q1, Q2, Q8, and Q9. The input is from the pulse generator (clock). The output is the strobe signal. The strobe circuit provides a signal for driving the strobe switches of the reading system. Refer to section VI for reading and writing into memory.

e. Ten Cycle Oscillator. This circuit uses Q21, Q26, and Q27. Q21 and Q27 constitute the free running 10 Hz multivibrator. Q27 is the driver. This circuit provides the term MOSC which causes the blinking action of the neon lamps on the control panel to indicate malfunctions of the computer. Refer to section II to see how the oscillator is used to indicate malfunctions.

f. TT Oscillator. Q2, Q7, Q11, and Q14 are used in this circuit. It is used to control the two-wire teletype output. Refer to section V for further explanation.

g. BAD Supply. This circuit is composed of a 6.2-volt zener diode (CR7) and a 22,000-ohm resistor (R11). The input is +138 volts zener. The output on pin B14 will be +131.8 volts. This circuit is used to reduce the anode supply voltage for battery display nixie indicators.

4-84. WRITE SWITCH BOARD

NOTE

Refer to section VI for an explanation of the write switches and other circuitry involved in writing into memory.

The write switch board contains 12 separate write switches, write head isolation diodes, test diodes, and a temperature sensing thermistor. The write switches (Q1, Q5, Q2 in TM 9-1220-221-34/1/1 make up a typical write switch) are used to complete continuity from the center tape of main memory write heads to selected wire amplifiers. The head isolation diodes isolate the selected write heads in the write switch matrix. The test diodes are used for logic testing circuitry elsewhere in the computer. The thermistor is connected to power control circuitry elsewhere in the computer.

4-85. WRITE AMPLIFIER BOARD

NOTE

Refer to section VI for a detailed explanation of its function in writing into memory.

The write amplifier contains two bistable flip-flop circuits with emitter-follower output drivers. The circuit's function is to supply a ground return path for the selected write head in the main memory. The two groups of diodes on the module are used to isolate a selected write head from other write heads within the computer's write switch matrix.

4-86. READ SWITCH BOARD

NOTE

Refer to section VI for a detailed explanation of the read switch board circuits in reading and converting signals.

The read switch board has two distinct functions. The six read switches are used to select the channel to be read from main memory. These signals are then amplified in the read amplifier board and converted to local signals. The amplifier consisting of transistor circuits Q7, Q11, Q15, Q17, Q18, Q19, Q20, and Q21, the strobe switch consisting of transistor circuits Q10 and Q14 and the flip-flop and driver circuits consisting of transistor circuits Q12, Q13, Q9, and Q16 on the read switch board are used to amplify and convert the signals from the circulating registers (loops) of memory into logical signals.

4-87. READ AMPLIFIER BOARD

NOTE

Refer to section VI for detailed explanation of the role of the read amplifier in amplifying and logic converting of read head signals.

The read amplifier receives main memory signals from the read switches. These read signals are amplified and converted into logical signals.

CHAPTER 5
REPAIR OF FADAC

Section I. Common Procedures

5-1. GENERAL

This section contains repair procedures that are commonly used throughout the computer. Refer to TM 9-254 for general maintenance procedures on electronic equipment.

WARNING

Shut down power and disconnect power source before attempting any removal or installation procedure.

CAUTION

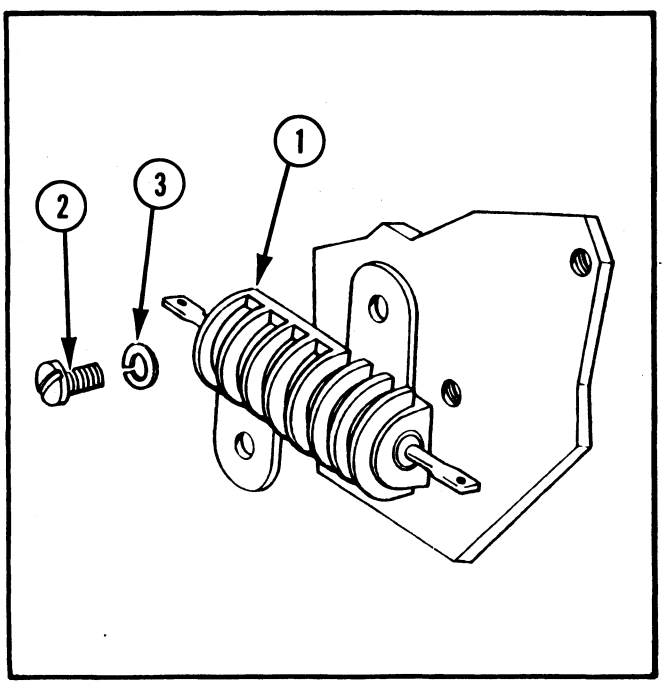
Do not operate memory unit when the chassis is on edge and unfolded.

5-2. REMOVAL AND INSTALLATION OF POWER RESISTORS

NOTE

This procedure is used by general support maintenance only. Refer to table 5-1 and 5-2 if required.

REMOVAL



1 Make note of wires soldered to terminals on resistor (1).

2 Indicate which end (arbitrarily designated A and B) of resistor (1) receives which set of wires.

3 Unsolder wires.

4 Remove screw (2), washer (3), and resistor (1).

INSTALLATION

1 Clean excess solder from wires and resistor terminals.

2 Strip insulation on wires, if necessary, to obtain clean tinned end with no broken strands.

3 Install resistor (1), using two screws (2) and two washers (3).

4 Attach wire to terminal, using at least one full turn through eyelet.

5 Solder wires, as noted, to terminals on resistor (1).

5-2. REMOVAL AND INSTALLATION OF POWER RESISTORS--Continued

Table 5-1. Power Resistor Location

Reference designation	Ohms	Rating tolerance	Watts	Attaching hardware	National stock no. (Part no.)	Location
R1	125	3%	10	Screw: no. 2-56 x 1/4 Washer, Helical: no. 2	5905-00-809-9651 (10525778-18)	Front of chassis assembly on upper control (main control panel removed).
R2	125	3%	10	Screw: no. 2-56 x 1/4 Washer, Helical: no. 2	5905-00-809-9651 (10525778-18)	
R3	160	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-809-9667 (10525778-7)	
R4	0.1	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-809-9655 (10525778-2)	
R5	14	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-809-9666 (10525778-6)	
R6	40	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-809-9665 (10525778-5)	
R7	32	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-080-6497 (10525778-3)	
R8	70	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-081-1074 (10525778-4)	
R9	200	3%	10	Screw: no. 2-56 x 1/4 Washer, Helical: no. 2	5905-00-087-2718 (10525778-17)	Power supply chassis wiring side (main control panel removed and chassis unfolded).
R10	1	3%	10	Screw: no. 2-56 x 1/4 Washer, Helical: no. 2	5905-00-087-2718 (10525778-16)	
R11	0.1	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-809-9655 (10525778-2)	

Table 5-1. Power Resistor Location--Continued

Reference designation	Ohms	Rating tolerance	Watts	Attaching hardware	National stock no. (Part no.)	Location
R12	32	3%	25	Screw: no. 4-40 x 3/8 Washer, Helical: no. 4	5905-00-080-6499 (10525778-3)	

*This information is given for guidance in replacing authorized parts. Do not use for requisitioning. Refer to TM 9-1220-221-34P for requisitioning.

Table 5-2. Power Resistor Wiring

Gage	Color	From	To
22	WHITE	R1A	108B-57
22	WHITE	R1A	101B-36
22	WHITE	R1B	109A-48
22	WHITE	R2A	133B-65
22	WHITE	R2B	109B-56
22	WHITE	R3A	106A-26
22	WHITE	R3B	R6-B
22	BLACK	R4A	107T-8
22	BLACK	R4B	137T-11
22	BLACK	R4B	137T-10
22	WHITE	R5A	134A-6
22	WHITE	R5A	132B-38
22	WHITE	R6A	106A-6
22	WHITE	R6B	R3-B
22	WHITE	R6B	105T-6
22	WHITE/BLACK	R7A	109A-59
22	BLUE	R7B	133A-26
22	WHITE/VIOLET	R8A	133A-57
22	WHITE/BLUE	R8B	132B-6
20	BLACK	R9A	CR2-A
22	BLACK	R9A	137T-2
20	WHITE	R9B	C4-A
20	WHITE	R9B	CR1-A
22	WHITE/BLACK	R10A	103T-23
22	WHITE	R10B	201A-64
20	WHITE	R10B	CR2-B
20	WHITE	R11A	L2-2
20	WHITE	R11A	L2-2

5-3. REMOVAL AND INSTALLATION OF REACTORS, CHOKES, AND TRANSFORMERS

NOTE

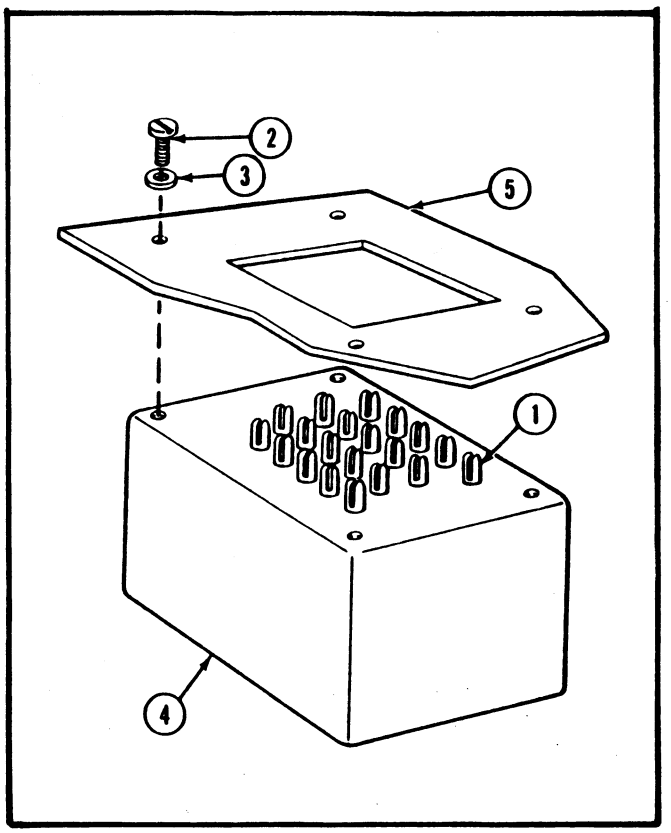
This procedure is used by general support maintenance only. Refer to tables 5-3 thru 5-8.

REMOVAL

1 Make note of wires soldered to lugs (1) on part to facilitate installation of replacement part. Do not remove more than one part at a time.

2 Unsolder or detach wires from lugs (1).

3 Remove four screws (2) and washers (3) attaching reactor, choke, or transformer (4). Support heavy items from beneath chassis (5).



INSTALLATION

1 Install reactor, choke, or transformer (4) in place and attach to chassis (5), using four screws (2) and washers (3).

2 Clean wires and terminals. Solder wires to lugs (1). Dress wires and provide as much wire service loop as possible.

5-4. EXPLANATION OF SYMBOLS

For tables 5-4 thru 5-7, the following symbols are used:

a. An asterisk (*) after the number in the Gage column denotes 600-volt wiring.

b. A letter A in the To column denotes the component side of the etched circuit board.

c. A letter B in the To column denotes the wiring side of the etched circuit board.

d. A letter T denotes a terminal strip.

Table 5-3. Reactors, Chokes, and Transformers*

Reference destination	National stock no. (Part no.)	Attaching hardware
L1	1220-00-861-3841 (10525930)	
L2	1220-00-870-3748 (10525920)	Screw: no. 8-32 x 3/8 (MS35233-43), 5305-00-543-2580
L3	1220-00-862-4769	
T1	5950-00-862-0001 (10525905)	Lockwasher: split, no. 8, (MS35337-80), 5310-00-042-9067
T2	5950-00-861-7103 (10525900)	
T3	5950-00-862-0002 (10525910)	
T4	5950-00-862-0003 (10525915)	Lockwasher, split, no. 2 (MS35337-77), 5310-00-058-2950 Screw: no. 2-56 x 5/16, (MS35233-4), 5305-00-543-2759

*Do not use this information for requisitioning. Refer to TM 9-1220-221-34P.

5-4. EXPLANATION OF SYMBOLS--Continued

Table 5-4. Power Supply Wiring of Transformer T1

Gage	Color	From	To
22*	WHITE	T1-1	K6-1
22*	WHITE	T1-1	T2-1
22*	WHITE	T1-2	K6-7
22*	WHITE	T1-2	T2-2
22*	WHITE	T1-3	T2-3
22SH	WHITE	T1-3	M2-3
22	WHITE	T1-4	106A-56
22	WHITE	T1-4	106A-52
22	WHITE	T1-4	106B-54
22	WHITE	T1-4	106B-56
22	WHITE	T1-5	106B-48
22	WHITE	T1-5	106A-46
22	WHITE	T1-5	106A-50
22	WHITE	T1-5	106B-50
22	WHITE	T1-6	106A-45
22	WHITE	T1-6	106A-41
22	WHITE	T1-6	106B-43
22	WHITE	T1-6	106B-45
22	WHITE	T1-7	134B-54
22	WHITE	T1-7	134B-52
22	WHITE	T1-7	134B-56
22	WHITE	T1-7	134A-56
22	WHITE	T1-8	134A-50
22	WHITE	T1-8	134A-46
22	WHITE	T1-8	134B-48
22	WHITE	T1-8	134B-50
22	WHITE	T1-9	134A-45
22	WHITE	T1-9	134A-41
22	WHITE	T1-9	134B-43
22	WHITE	T1-9	134B-45
22	WHITE	T1-10	134B-63
22	WHITE	T1-11	134B-34
22	WHITE	T1-12	134A-34
22	WHITE	T1-13	134A-11
22	WHITE	T1-14	134B-11
22	WHITE	T1-15	134A-1
22	BLACK	T1-16	T2-19
22	BLACK	T1-17	T2-20
22	BLACK	T1-17	137E-15

Table 5-5. Power Supply Wiring of Transformer T2

Gage	Color	From	To
22	WHITE	T2-9	201A-41
22	WHITE	T2-10	106B-62
22	WHITE	T2-11	106B-33
22	WHITE	T2-12	106A-33
22	WHITE	T2-13	201B-54
22	WHITE	T2-13	140-52
22	WHITE	T2-14	201B-61
22	WHITE	T2-14	140B-60
22	WHITE	T2-15	201B-64
22	WHITE	T2-15	140B-63
22	WHITE	T2-16	134B-24
22	WHITE	T2-17	134B-20
22	WHITE	T2-18	134A-17
22	BLACK	T2-19	T1-16
22	BLACK	T2-19	T3-16
22	BLACK	T2-20	T1-17
22	BLACK	T2-20	T3-17
22SH	WHITE	T2-1	J20-35
22*	WHITE	T2-1	T1-1
22SH	WHITE	T2-1	M2-1
22*	WHITE	T2-2	T1-2
22SH	WHITE	T2-2	M2-2
22*	WHITE	T2-3	K3-6
22*	WHITE	T2-3	T1-3
22	WHITE	T2-4	140A-37
22	WHITE	T2-5	140A-39
22	WHITE	T2-6	140A-41
22	WHITE	T2-7	201A-37
22	WHITE	T2-8	201A-39

5-4. EXPLANATION OF SYMBOLS--Continued

Table 5-6. Power Supply Wiring of Transformer T3

Gage	Color	From	To
22*	WHITE	T3-1	K1-9
22SH	WHITE	T3-1	104B-65
22*	WHITE	T3-2	K1-6
22*	WHITE	T3-2	T4-2
22*	WHITE	T3-3	K1-2
22SH	WHITE	T3-3	140B-59
22	WHITE	T3-4	109A-22
22	WHITE	T3-5	109B-17
22	WHITE	T3-6	109A-19
22	WHITE	T3-7	109A-51
22	WHITE	T3-8	J020-14
22	WHITE	T3-9	J020-15
22	WHITE	T3-10	106B-24
22	WHITE	T3-11	106B-20
22	WHITE	T3-12	106A-17
22	WHITE	T3-13	106A-11
22	WHITE	T3-14	106B-11
22	WHITE	T3-15	106A-1
22	BLACK	T3-16	T2-19
22	BLACK	T3-16	T4-17
22	BLACK	T3-17	T2-20
22	BLACK	T3-17	T4-18

Table 5-7. Power Supply Wiring of Transformer T4

Gage	Color	From	To
22SH	WHITE	T4-1	141E-2
22*	WHITE	T4-2	T3-2
22SH	WHITE	T4-2	140B-49
22	WHITE	T4-3	204B-29
22	WHITE	T4-4	204B-34
22	WHITE	T4-5	109A-57
22	WHITE	T4-6	204B-50
22	WHITE	T4-7	204B-46
22	WHITE	T4-8	204A-48
22	WHITE	T4-9	132A-61
22	WHITE	T4-10	204B-18
22	WHITE	T4-11	204B-23
22	WHITE	T4-12	204B-24
22	WHITE	T4-13	204A-2
22	WHITE	T4-14	132A-1
22	WHITE	T4-15	204B-64
22	WHITE	T4-16	109B-4
22	BLACK	T4-17	T3-16
22	BLACK	T4-17	137E-15
22	BLACK	T4-18	T3-17

Table 5-8. Power Supply Wiring of Reactors and Chokes L1, L2, L3

Gage	Color	From	To
20	BLACK	L1-1	107E-11
20	BLACK	L1-2	C2-A
20	BLACK	L1-2	107E-9
20	BLACK	L1-2	107E-8
20	WHITE	L2-1	135E-20
20	WHITE	L2-2	R11-A
22	WHITE/GREY	L3-1	135E-5
20	WHITE/GREY	L3-1	CR3-B
20	WHITE	L3-2	CR3-A
22	WHITE	L3-2	107E-1

5-5. REMOVAL AND INSTALLATION OF CAPACITOR AND BRACKET

NOTE
Refer to table 5-9 if required.

REMOVAL

1 Make note of wires soldered to capacitor terminals (1). Note the orientation of the positive and negative terminals of capacitor. Mark if necessary.

2 Unsolder and detach wires from capacitor terminals (1), remove nuts (2) and washers (3), and remove bracket (4) and capacitor (5).

3 Remove insulator (6) from capacitor (5).

INSTALLATION

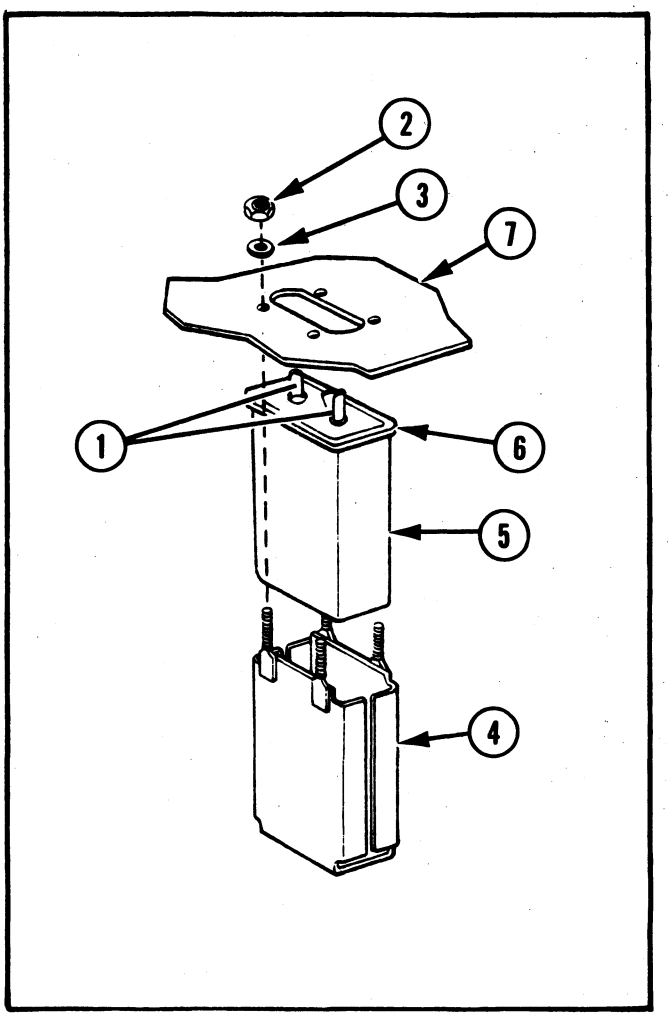
1 Install insulator (6) on capacitor (5).

2 Assemble capacitor (5) to bracket (4).

3 Install assembled capacitor (5) and bracket (4) to chassis (7), using nuts (2) and washer (3). Make note of terminal orientation.

4 Solder wiring to capacitor terminals (1) of capacitor (5) in accordance with previously noted arrangement.

5 Press wires against chassis (7). Leave service loop.



5-5. REMOVAL AND INSTALLATION OF CAPACITOR AND BRACKET--Continued

Table 5-9. Power Supply Wiring of Capacitors

Gage	Color	From	To
20	BLACK	C1A	C2A
22	WHITE/BLUE	C1B	107E16
20	BLACK	C2A	C1A
20	BLACK	C2A	L12
22	WHITE/BLUE	C2B	107E17
20	WHITE	C3A	C4A
20	WHITE	C3A	R9B
22	WHITE/GREY	C3B	135E2
20	WHITE	C4A	R9B
20	WHITE	C4A	C3A
22	WHITE/GREY	C4B	135E3
20 (600v)	WHITE	C5-A	CB-2
20	WHITE	C5-B	C6-2
20	WHITE	C5-B	135E-4

Section II. Removal and Installation of Specific Items

5-6. GENERAL

a. Scope. This section contains procedures that are applicable and unique to particular parts and assemblies and that are used only once in servicing the computer.

b. Reference. For procedures on removal of front and rear covers from case assembly, removal of chassis assembly from case assembly, removal of cover panels from top or bottom of chassis assembly, and removal of circuit boards, refer to TM 9-1220-221-20&P.

WARNING

Shut down power and disconnect power source before attempting any removal or installation procedure.

CAUTION

Do not unfold chassis to obtain access to wiring unless every means possible has been exhausted to determine if the malfunction is due to a broken circuit or a short.

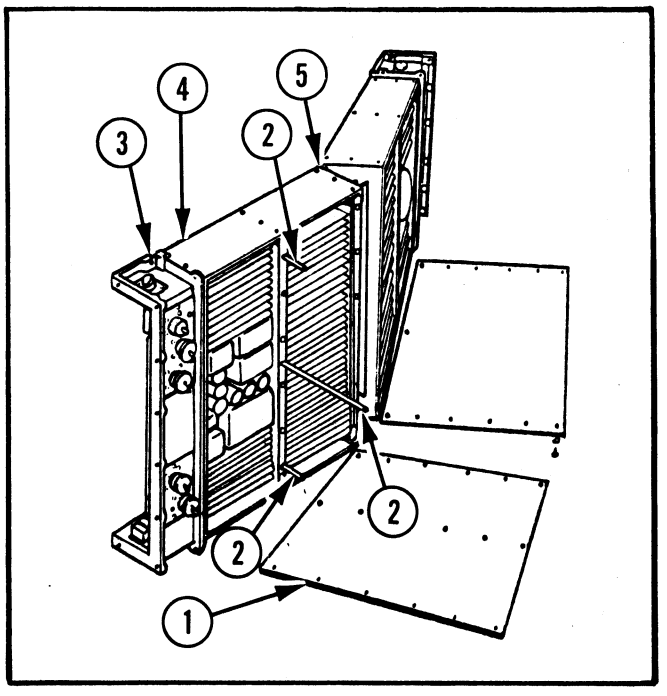
5-7. GAINING ACCESS TO CHASSIS WIRING

1 Remove chassis assembly from case assembly.

2 Remove upper cover (1) and loosen three tie bolts (2).

3 Loosen two captive screws (3) on upper chassis assembly (4).

4 Unfold chassis along axis of hinge (5).



ASSEMBLY OF CHASSIS ASSEMBLIES

1 Fold chassis along hinge (5).

2 Secure with two captive screws (3) and three tie bolts (2).

3 Install upper cover (1).

5-8. REMOVAL AND INSTALLATION OF MEMORY

CAUTION

Do not place magnetized screwdrivers or other maintenance tools within 1 foot of the memory.

Do not place memory in an area subject to high magnetic fields. Do not place energized soldering irons producing magnetic field within 1 foot of the memory. Store clear of high current conductors or machinery.

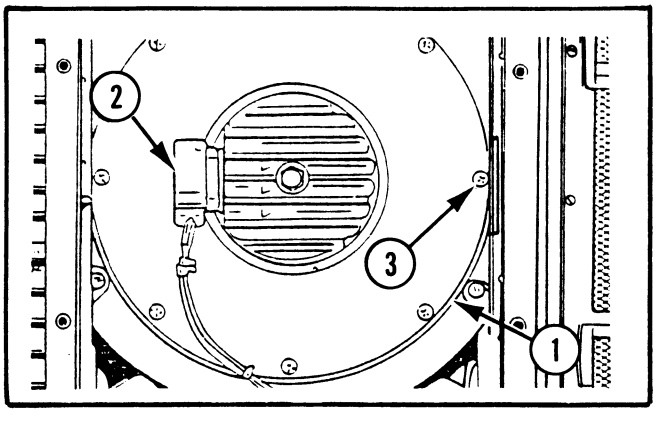
Protect connectors with caps or suitable devices.

REMOVAL

1 Gain access to memory (1220-00-861-3842) (1) by removing chassis assembly from case assembly. Unfold and remove lower cover from lower chassis assembly.

2 Remove connector (2) from outer face of memory (1).

3 Remove three retaining screws (3) from outer face of memory (1).



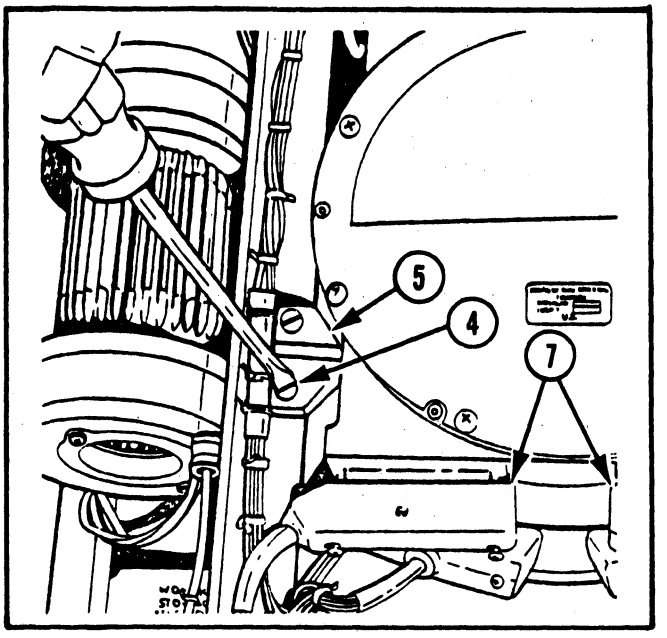
5-8. REMOVAL AND INSTALLATION OF MEMORY--Continued

4 Remove two attaching screws (4) from two mounting brackets (5) on inner side of chassis assembly. Remove mounting brackets.

5 Tilt top of memory (1) to inner side of chassis assembly to gain access to top connectors (6). Remove top connectors.

6 Tilt bottom of memory (1) to inner side of chassis assembly to gain access to bottom connectors (7). Support memory and remove bottom connectors and temperature sensor (8).

7 Remove memory.



INSTALLATION

1 Position memory (1) in place in lower half of computer.

2 Support memory (1). Tilt bottom of memory to inner side of chassis assembly and install bottom connectors (7) and temperature sensor (8).

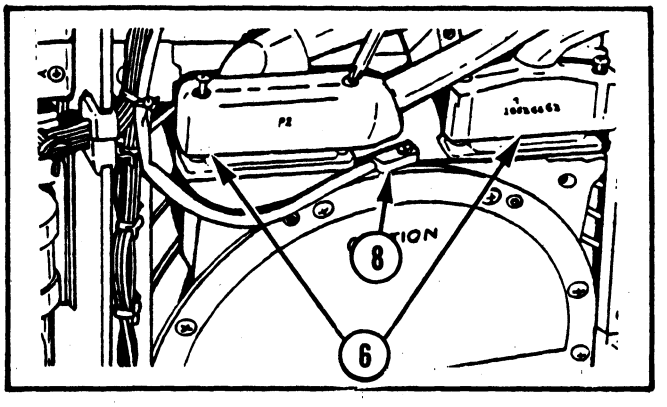
3 Tilt top of memory (1) to inner side of chassis assembly and install top connectors (6).

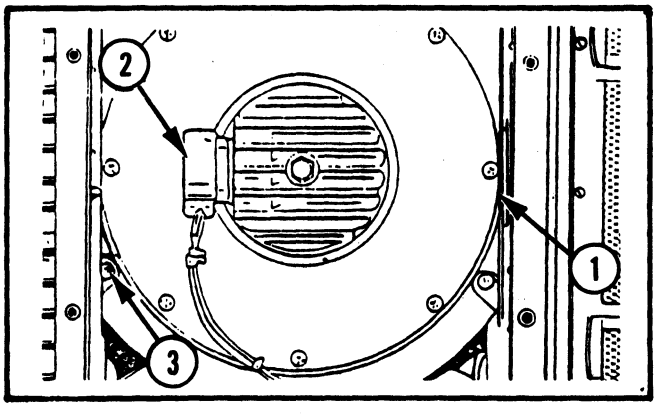
4 Position two mounting brackets (5) on inner side of chassis assembly and attaching screws (4).

5 Install and tighten three retaining screws (3) in the outer face of the memory (1).

6 Install small connector (2) on outer face of memory (1).

7 Fold computer together and install chassis in case.





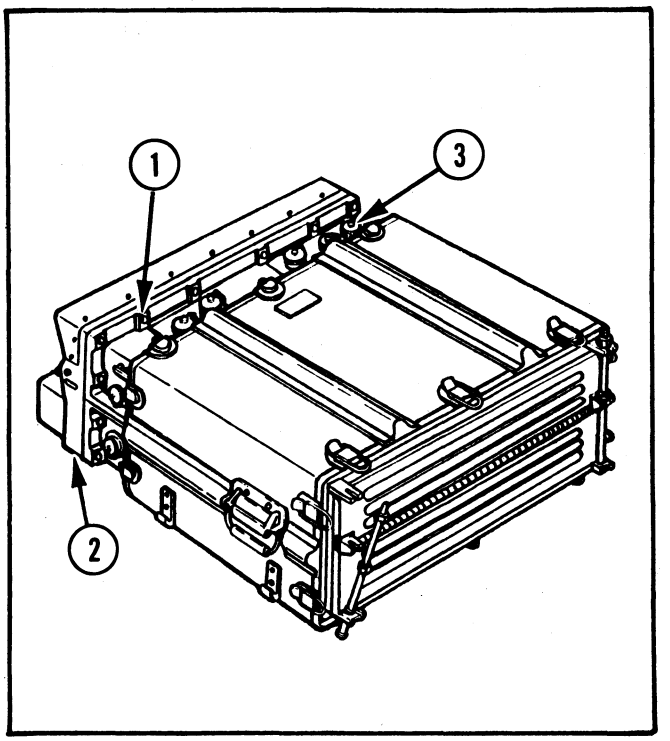
5-9. REMOVAL AND INSTALLATION OF MAIN CONTROL PANEL ASSEMBLY

REMOVAL

1 Remove 16 bolts and washers (1).

2 Pull away main control panel assembly (2) until free from chassis assembly (3) while supporting the main control panel assembly.

3 Remove four connectors P2, P1, P6, and P5 from receptacles J18, J19, J20, and J21 on chassis assembly.



INSTALLATION

1 Plug the four connectors P2, P1, P6, and P5 respectively into receptacles J18, J19, J20, and J21 on chassis assembly and secure tightly.

2 Attach main control panel assembly (2) to chassis assembly (3), using 16 bolts and washers (1).

5-10. REMOVAL AND INSTALLATION OF BLOWER

REMOVAL

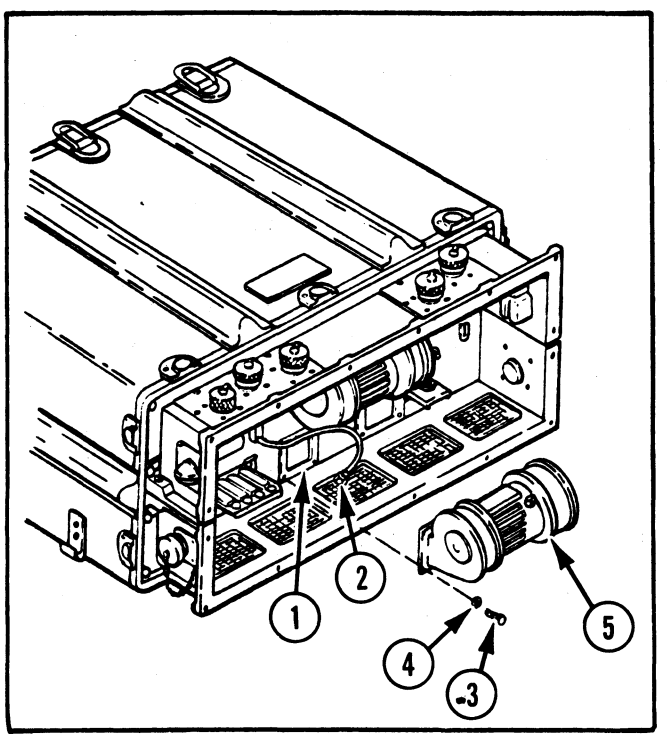
1 Remove main control panel assembly.

CAUTION
Avoid damage to gasket (1).

2 Disconnect blower connector (2) and remove eight screws (3) and washers (4).

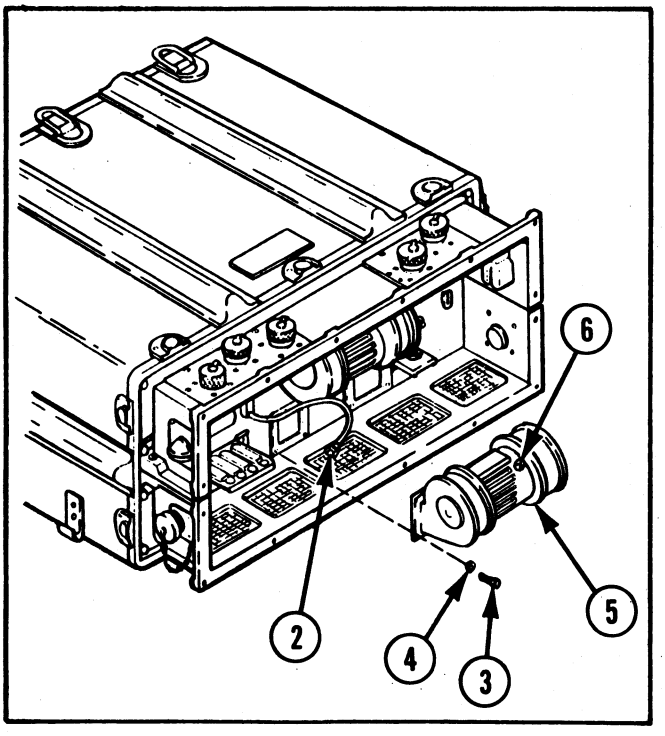
NOTE
The illustration shows removal of lower blower. Blower on upper part of chassis is removed in a similar manner.

3 Remove blower (5).



5-10. REMOVAL AND INSTALLATION OF BLOWER--Continued

INSTALLATION



1 Dress connector lead away from blower (5).

2 Install blower (5) in place.

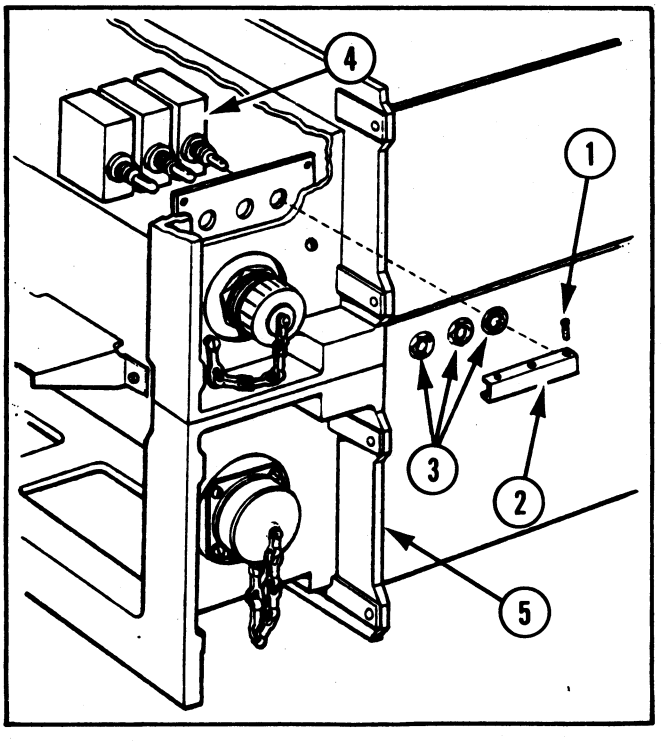
3 Fasten with eight washers (4) and screws (3).

4 Install connector (2) in mating receptacle (6) on blower (5).

5-11. REMOVAL AND INSTALLATION OF MAIN POWER CIRCUIT BREAKER

NOTE
Refer to table 5-10 for circuit breaker wiring.

REMOVAL



1 Remove covers on computer.

2 Remove control panel assembly.

3 Remove three screws (1) and bracket (2) from circuit breaker assembly.

4 Remove three nuts (3) and circuit breaker (4).

5 Make note of wires attached to circuit breaker.

6 Dress wires away from chassis assembly (5), and remove wires from circuit breaker (4).

5-11. REMOVAL AND INSTALLATION OF MAIN POWER CIRCUIT BREAKER--Continued

INSTALLATION

1 Clean excess solder from removed wires.

2 Solder wires to circuit breaker (4).

3 Install circuit breaker (4), using three nuts (3).

4 Install bracket (2) and three screws (1).

5 Perform physical inspection. Clean chaff from the area. Retouch paint on external surface of chassis assembly (5) if required.

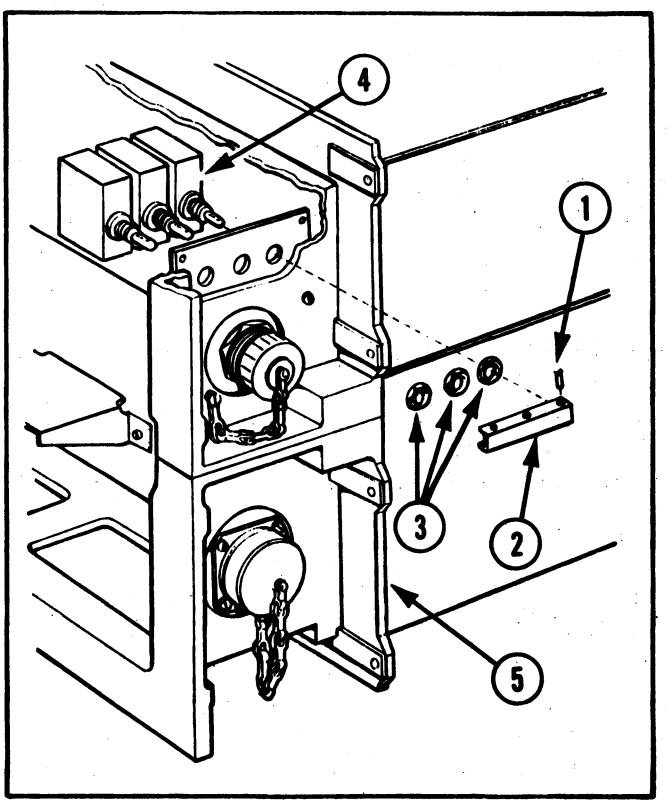


Table 5-10. Circuit Breaker Wiring

Gage	Color	From	To
20 (600v)	WHITE	CB-1	J11-A
22 (SHLD)	WHITE	CB-2	K1-10
20 (600v)	WHITE	CB-2	C5-A
20 (600v)	WHITE	CB-3	J11-B
22 (SHLD)	WHITE	CB-4	K1-5
20 (600v)	WHITE	CB-4	C6-A
20 (SHLD)	WHITE	CB-5	J11-C
22 (SHLD)	WHITE	CB-6	K1-3
20 (600v)	WHITE	CB-6	C7-A

CHAPTER 6
FINAL INSPECTION

6-1. GENERAL

Final inspection is performed after repair has been completed to ensure that materiel is serviceable according to established serviceability standards. Any item containing defects disclosed by the final inspection will be further repaired to place it in a serviceable condition.

6-2. PHYSICAL INSPECTION

a. Soldering.

(1) Inspect for burned insulation around areas where removal and installation of a soldered item was accomplished.

(2) Check for broken strands where wiring was removed.

(3) Inspect for presence of sleeving on terminals where wiring has been removed.

(4) Check for broken strands next to soldered joints.

(5) Check for loose solder, hardware, or other chaff which may have resulted from the work accomplished.

b. Screws and Washers.

(1) Check for presence and tightness of all screws attaching connectors.

(2) Check for proper dress of harness, proper support with clamps, and attaching screws on detail parts.

(3) Check for presence of washers where required.

6-3. INSPECTION CHECKOUT PROCEDURE

Perform inspection checkout procedure as detailed in TM 9-1220-221-20&P.

6-4. LOGIC TEST

Run all tapes in a complete logic test in accordance with TM 9-1220-221-20&P, TM 9-1220-221-34/2, TM 9-1220-221-34/3, TM 9-1220-221-34/4, and TM 9-1220-221-34/5 with the MARGINAL TEST switch in each of its positions.

6-5. DYNAMIC EVALUATION

Perform dynamic evaluation of the computer utilizing self-test and problem solution as detailed in TM 9-1220-221-20&P.

6-6. ASSOCIATED EQUIPMENT

Perform physical inspection of associated equipment and computer table. Inspect condition of basic issue items for physical condition and completeness in accordance with TM 9-1220-221-10-1 or TM 9-1220-221-10-2.

APPENDIX
REFERENCES

A-1. Scope
This appendix lists all forms, field manuals, and technical manuals referenced in this manual.

A-2. Forms
Accident Reporting and Records ..... AR 385-40
Equipment Control Record - Transfer Report ..... DA Form 2408-9
Equipment Daily Log ..... DA Form 2408-10
Equipment Improvement Recommendation ..... SF 368
Equipment Maintenance Log (Consolidated) ..... DA Form 2409
Equipment Modification Record ..... DA Form 2408-5
Recommended Changes to Publications ..... DA Form 2028
Uncorrected Fault Record - Aircraft ..... DA Form 2408-14

A-3. Pamphlets
Index of Blank Forms ..... DA PAM 310-2
US Army Equipment Index of Modification Work Orders ..... DA PAM 310-7

A-4. Technical Manuals
Direct Support and General Support Maintenance Manual:
Computer Gun Direction M18 (1220-448-0131) (Logic Equations and Schematic Diagrams) ..... TM 9-1220-221-34/1/1
Direct Support and General Support Maintenance Manual:
Computer, Gun Direction: M18 (Test tape B program printout) (Reprinted w/Basic Incl C1) Changes 1 .....TM 9-1220-221-34/2
Direct Support and General Support Maintenance Manual:
Computer, Gun Direction: M18 (Test Tape B Program Printout) (Reprinted w/Basic Incl C1) Changes 1 ..... TM 9-1220-221-34/3
Direct Support and General Support Maintenance Manual:
Computer, Gun Direction: M18 (Test Tape D Program Printout) (Reprinted w/Basic Incl C1-2) Changes 1,2 .. TM 9-1220-221-34/4
Direct Support and General Support Maintenance Manual:
Computer, Gun Direction: M18 (FSN 1220-448-0131) (Test Tape E Program Printout) (Reprinted w/Basic Incl C1-3) Changes 1-3 ..... TM 9-1220-221-34/5
Direct Support and General Support Maintenance Manual:
Computer, Gun Direction, M18 (Wire List) (Reprinted w/ Basic Incl C1) Changes 1 ..... TM 9-1220-221-34/6
Direct Support and General Support Maintenance Manual: Computer Gun Direction: M18 W/E (FSN 1220-448-0131) (Component List) (Reprinted w/Basic Incl C1) Changes 1 ..... TM 9-1220-221-34/7
Direct Support and General Support Maintenance Manual:
Computer: Gun Direction M18 (1220-448-0131) ..... TM 9-1220-221-34/8
Direct Support and General Support Maintenance Repair Parts and Special Tools List for Computer, Gun Direction M18 W/E (1220-448-0131) ..... TM 9-1220-221-34P
Direct Support and General Support Maintenance Repair Parts and Special Tools List for Reproducer, Signal Data AN/GSQ-64 W/E (1290-973-2180) ..... TM 9-1290-326-34P

Appendix A--Continued

A-4. Technical manuals--continued

Direct Support and General Support Repair Parts and Special Tools List for Test Set, Computer Logic Unit AN/GSM-70 (4931-045-6540) ..... TM 9-4931-204-34P

Direct Support and General Support Maintenance Manual: Test Set, Computer Logic Unit AN/GSA-70; Control Box, Computer Logic Unit Test Set C-4020/GSM-70 (4931-045-6540) ..... TM 9-4931-204-34/1

General Maintenance Procedures for Fire Control Materiel ..... TM 9-254

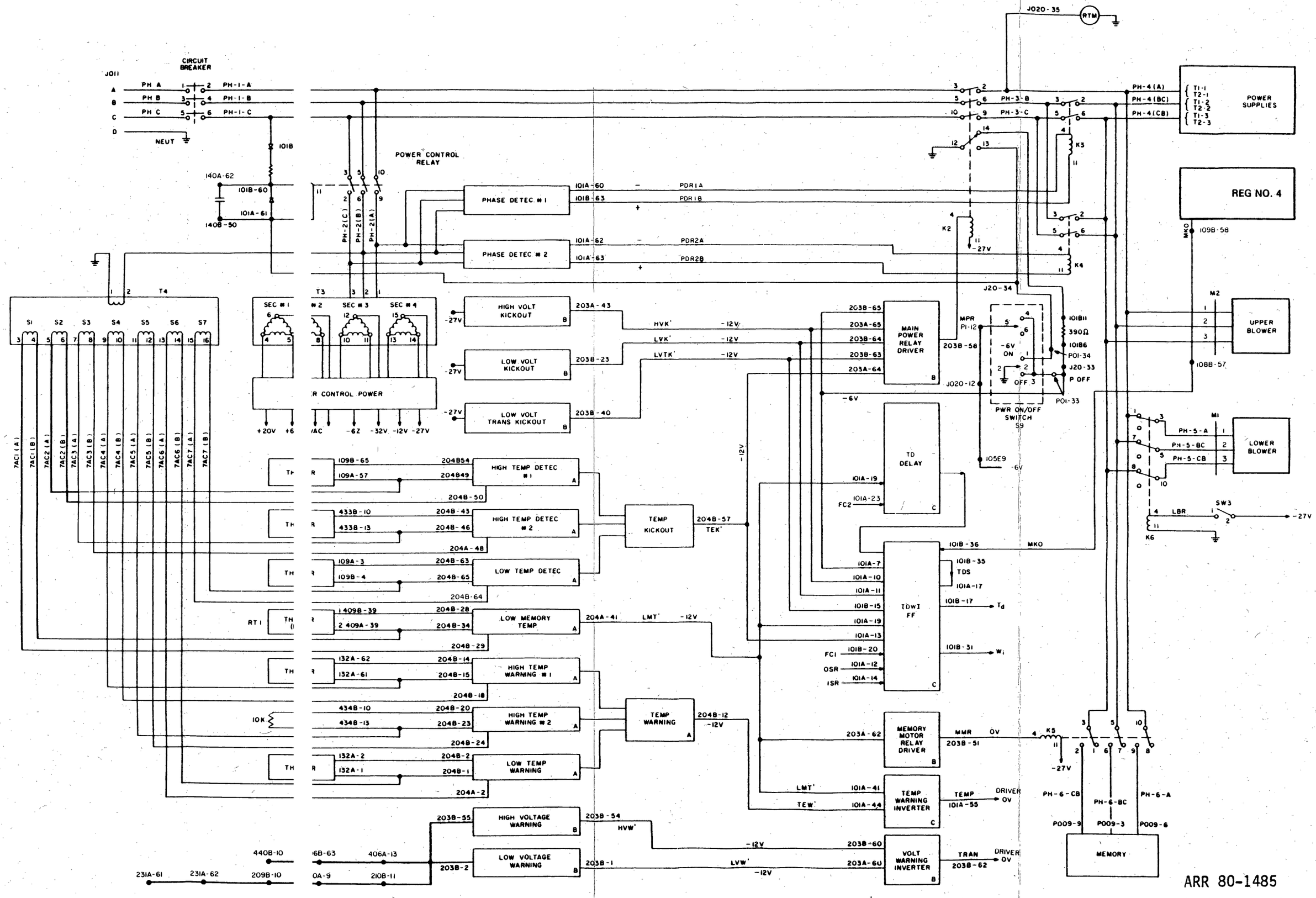
Operation and Maintenance Manual for Computer, Gun Direction, M18 (FADAC) 1220-00-448-0131 ..... TM 9-1220-221-10-1

Operation and Maintenance Manual for Computer, Gun Direction, M18 (FADAC) 1220-00-448-0131 ..... TM 9-1220-221-10-2

Operator and Organizational Maintenance Manual Including Repair Parts and Special Tools List for Reproducer, Signal Data, AN/GSQ-64 (SDR) 1290-00-973-2180 and Test Set, Computer Logic Unit, AN/GSM-70 (FALT) 4931-00-045-6540 ..... TM 9-4931-204-12&P

Organizational Maintenance Repair Parts and Special Tools List for Computer, Gun Direction M18 W/E (1220-448-0131) Changes 1 ..... TM 9-1220-221-20&P

The Army Maintenance Management System (TAMMS) (Reprinted w/Basic Incl C1) Changes 1 ..... TM 38-750



ARR 80-1485

FO-1. FADAC Power Control Circuitry.

ALPHABETICAL INDEX

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

ALPHABETICAL INDEX--Continued

By Order of the Secretary of the Army:

E. C. MEYER
General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
Major General, United States Army
The Adjutant General

Distribution:

To be distributed in accordance with DA Form 12-41, Direct and General Support maintenance requirements for Computer, Gun Direction.

U.S. GOVERNMENT PRINTING OFFICE: 1981—703-029/1177

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

Your mailing address

DATE SENT

Date you filled out this form

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 9-1220-221-34/1	25 May 81	M18 Gun Direction Computer (FADAC)

BE EXACT. PIN-POINT WHERE IT IS

PAGE NO.	PARAGRAPH	FIGURE NO	TABLE NO
4-186	4-65d		

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Add this note after subparagraph (1).

NOTE

Specific logic can be followed by referring to the appropriate logic list in TM 9-1220-221-34/1/1.

SAMPLE

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

JOHN DOE SP/4 XXX-XXXX

SIGN HERE: John Doe

DA FORM 1 JUL 79 2028-2 PREVIOUS EDITIONS ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

U.S. MAIL

Commander
US Army Armament Materiel Readiness Command
ATTN: DRSAR-MAS
Rock Island, IL 61299

TEAR ALONG PERFORATED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 9-1220-221-34/1	25 May 81	M18 Gun Direction Computer (FADAC)

BE EXACT. PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

SIGN HERE:

DA FORM 1 JUL 79 2028-2 PREVIOUS EDITIONS ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

U.S. MAIL

Commander
US Army Armament Materiel Readiness Command
ATTN: DRSAR-MAS
Rock Island, IL 61299

TEAR ALONG PERFORATED LINE