AUERBACH STANDARD EDP REPORTS

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for the Electronic Data Processing Field

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Philadelphia, Penna.

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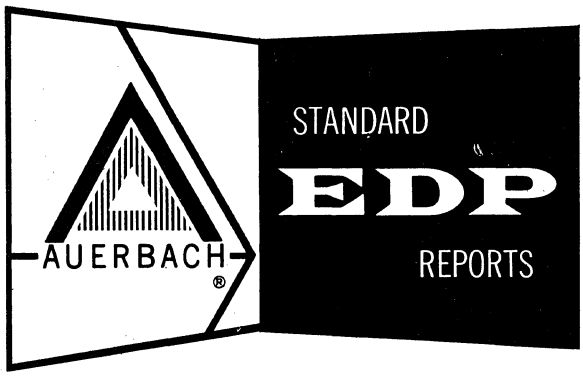

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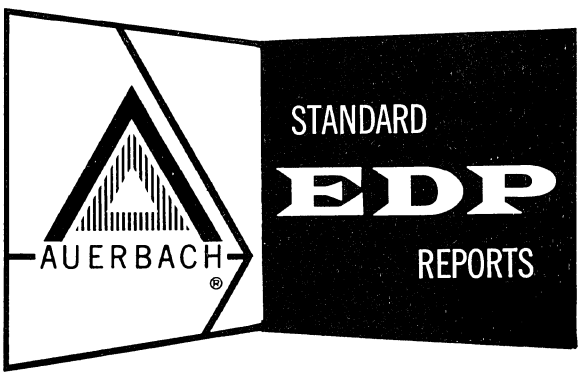
7/64

UNIVAC 1004

Univac

(A Division of Sperry Rand Corporation)



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UNIVAC 1004

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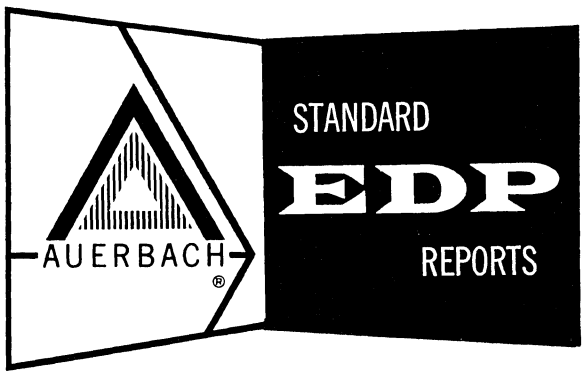

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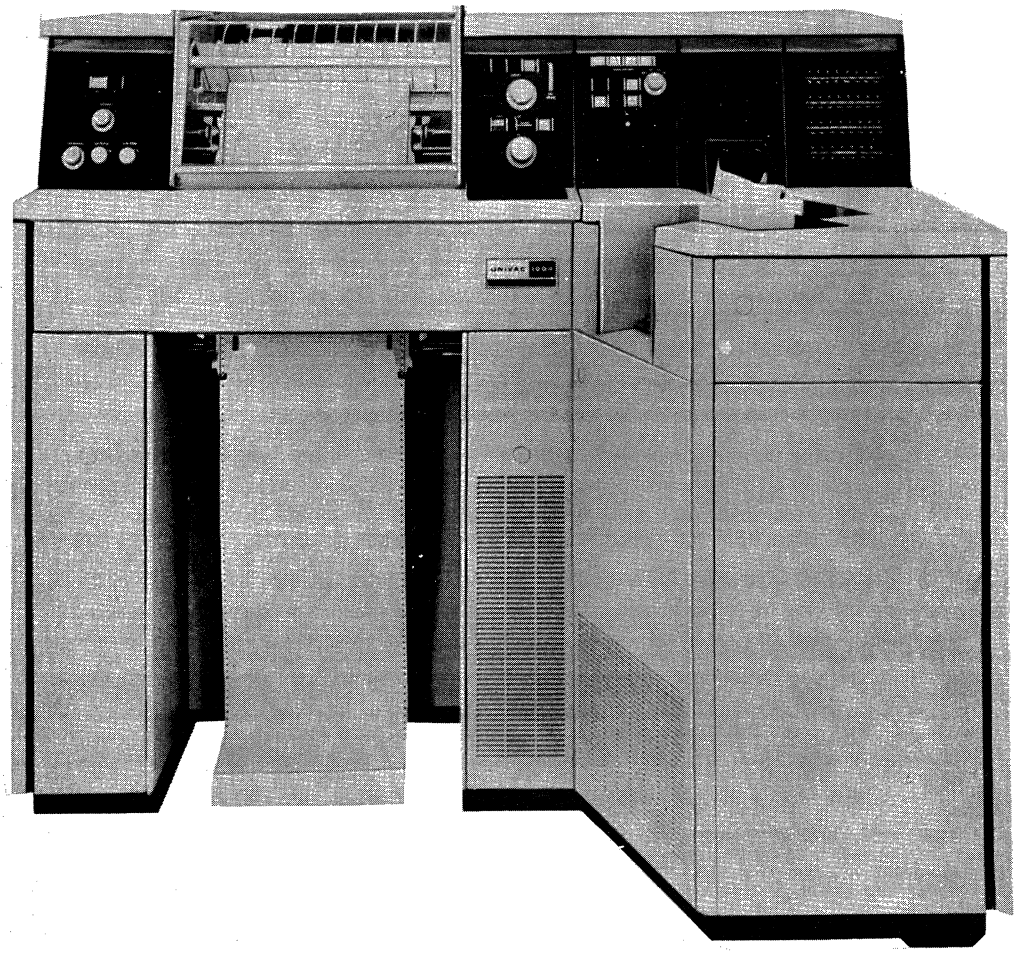
§ 001.



UNIVAC 1004 CARD PROCESSOR

Photograph courtesy of UNIVAC Division of Sperry Rand Corp.

INTRODUCTION

§ 011.

The UNIVAC 1004 is a compact, plugboard-programmed computer. Its two basic models, the 1004 I and 1004 II, can process punched card input at speeds of about 340 and 600 cards per minute, respectively, including the necessary allowances for a typical amount of computation and for I/O interlocks. (Card reading and printing can proceed simultaneously, but cannot be overlapped with computation.)

Rentals for the basic 1004 system (consisting of processor, card reader, and printer in a single cabinet) range from $1,150 to $1,625 per month. Additional peripheral equipment that can be connected includes a card punch, a second card reader, a card read/punch unit, paper tape equipment, and data communication terminals. A special processor model, the 1004 III, can control one or two magnetic tape units in addition to the above equipment.

First deliveries of the UNIVAC 1004 I were made in January 1963, and over 1,300 systems have been installed to date. The faster 1004 II and 1004 III were announced in March 1964.

The 1004 is most commonly used as an independent data processing system for small business applications. As such, it is attractive to many organizations considering a step upward from conventional tabulating installations because the 1004 requires less retraining of their staffs than a stored-program computer system would require. Furthermore, the 1004 offers economic advantages over stored-program systems for many applications whose processing and internal storage requirements are relatively small.

The 1004 can serve as a satellite system for a larger computer, such as a UNIVAC 490 or 1107. It is also suitable for use as a small computer in a branch office, communicating with a larger, home-office computer either by means of direct communication lines or simply through physical interchange of card decks or tape reels.

Where the 1004 is used as a complete data processing installation, there is no larger program-compatible computer system into which the installation can grow as its workload increases. UNIVAC, however, has announced provisions for connecting a 1004 system to its larger 1050 series of computers (described in Computer System Report 777:). The 1050 can then be used in conjunction with, and perhaps eventually replace, the 1004.

The UNIVAC 1004 can be used with more than one coding system. It normally operates with either the standard UNIVAC XS-3 code or with the Remington Rand 90-column card code. Which code is to be used is program-selectable, so it is possible to use both codes within a single program. This allows, for instance, reading a mixture of 80-column and 90-column cards, or reading 80-column cards and punching 90-column cards.

Codes other than the XS-3 and 90-column codes can be automatically translated to either of these codes by a special Translate Feature, provided that there are no more than 6 data bits per character in the original code. In particular, the IBM BCD codes used on the 1401 and other IBM systems can be translated, thus allowing the 1004 to be used as a satellite to many non-UNIVAC computer systems.

The UNIVAC 1004 has 961 alphameric character positions of core storage. Each core position contains six data bits. Core storage cycle time is 8.0 microseconds in the UNIVAC 1004 I and 6.5 microseconds in the UNIVAC 1004 II and III.

The plugboard of the basic machine has a capacity for 31 program steps (expandable to 62). Each step can specify two operand addresses, and multiple operations can be performed in a single program step. Arithmetic operations include add and subtract (both algebraic and absolute) and compare. Multiply and divide operations require the use of wired subroutines. Seven types of transfer processes are provided, including several with editing facilities. Input-output areas are assigned fixed locations in core storage. Input-output commands can be combined in the same step with other operations.

Operands can be of any length up to the capacity of core storage. Operand length is specified by the operand addresses wired in each program step. Instructions are executed at the rate of about 6,500 instructions per second in the 1004 I processor and about 8,000 instructions per second in the 1004 II and III.

§ 011. INTRODUCTION (Contd.)

The 1004 can read cards and print simultaneously, but neither of these operations can be overlapped with computation. Card punching can overlap either computing or other peripheral operations. The optional peripheral devices may:

(1) be able to overlap both computing and card reading and/or printing (e.g., the paper tape punch or the card read/punch operations);

(2) be able to overlap computing but not card reading or printing (e.g., the auxiliary card reader or the paper tape reader); or

(3) be unable to overlap any other operation (e.g., the Data Line Terminals).

The 1004 is available in 80-column, 90-column, or 80/90-column models. The basic system consists of a card reader, central processor with plugboard control, and printer. All are housed in a single compact cabinet. The card reader in the 1004 I Processor has a rated speed of 300 cards per minute, and the printer has a rated speed of 300 lines per minute. These rated speeds include an allowance for 35 milliseconds of computation per card or line, which has been found to be quite conservative. In typical applications, computation time is about 5 milliseconds per card, and reading and/or printing speeds of about 340 cards/lines per minute are obtained.

In the 1004 II and III, the card reader operates at a speed of 615 cards per minute, and the printer operates at 600 lines per minute; both these speeds are based on 5 milliseconds of computation per record.

A card punch can be connected to the UNIVAC 1004. It punches at a speed of 200 cards per minute. The card punch is available in a read/punch model which reads and/or punches cards at a speed of 200 cards per minute. The read/punch enables a 1004 system to read data from and punch results into the same card. A 400-card-per-minute Auxiliary Card Reader can also be used with the 1004 Processor.

Two different Data Line Terminals are available. The Data Line Terminal, Type 1, can be used to communicate with a UNIVAC 1050, 490, 1107, or another 1004. The Data Line Terminal, Type 2, permits communication with magnetic tape terminals such as the Digitronics Dial-O-Verter.

A 400-character-per-second paper tape reader and a 110-character-per-second paper tape punch can be used with the 1004.

One or two Uniservo magnetic tape units can be connected to the UNIVAC 1004 III processor only. Three density levels — 200, 556, and 800 pulses per inch — provide speeds of 8,000, 23,000, and 34,000 characters per second, respectively. These magnetic tapes can be written in a mode compatible with either UNIVAC or IBM standards, although programmed translation may be required.

The software available with the 1004 is naturally limited. It consists primarily of short subroutines for handling multiplication, division, and a number of common commercial problems. These include suggested methods for handling reconciliations, deleting subtotals where there has only been a single card to be totaled, handling missing numbers in a matching operation, checking the sequence of alphanumeric identification numbers, and verifying check digits.

In addition, a number of complete programs are available. These include standard listing and transcription programs, and at least one General Purpose Program, which is a report writer that can facilitate setting up the equipment for new reports. A start has been made on supplying some scientific routines, such as sine-cosine and square root routines, and a Critical Path Method routine has been announced.

Software routines are circulated by the UNIVAC Division to 1004 users.

ADDITIONS AND CHANGES

§ 015.

.1 AUXILIARY CORE STORAGE UNIT

An Auxiliary Core Storage (ACS) Unit that doubles the internal storage capacity of a UNIVAC 1004 I, II, or III processor was announced by UNIVAC on September 29, 1964. The new optional unit provides 961 additional character positions of program-addressable core storage, expanding the total core storage capacity of any 1004 processor to 1,922 characters. Programs written for a 1004 with the standard 961-character storage capacity can be run without alteration on a 1004 equipped with the new ACS unit.

The additional storage provided by the ACS will considerably increase the amount of processing that can be performed by a 1004 during a single pass. The ACS will also increase the efficiency of 1004 Data Line Terminal communications by permitting the transmission of longer messages. In 1004 III systems, the ACS will permit the use of longer magnetic tape blocks, enabling the 1004 III to meet the block length requirements for efficient use in many satellite system applications.

Delivery of Auxiliary Core Storage Units for 1004 processors will begin in late December, 1964. Rental for the ACS is $100 per month, and purchase price is $2,950.

.2 UNIVAC BANK PROCESSOR IV

A new check processing system, the UNIVAC Bank Processor IV, was introduced by UNIVAC on September 28, 1964. The system consists of a UNIVAC 1004 processor (with built-in card reader and printer), an MICR document sorter-reader, and a card punch. UNIVAC states that this combination will handle all accounting operations in most banks with deposits of less than 50 million dollars.

Numerous optional features and peripheral devices can be added to the basic Bank Processor IV. It can be connected by common-carrier communications facilities to a remote large-scale computer, enabling a bank to tie in all of its branches with a central computer. Compatibility with competitive computers can be achieved via magnetic tape. Input can be in the form of MICR documents, punched cards, paper tape, or messages from remote points.

The MICR sorter-reader has a peak sorting rate of 1,200 documents per minute. It will be available in models with 6, 12, and 18 pockets, and can be used as a free-standing document sorter while the 1004 processes other work. The sorter-reader will accept intermixed paper and card documents of varying size and thickness, will use radial stackers to control document alignment, and will handle endorsing and automatic batch numbering with no reduction in the document handling rate. Pocket capacity is 2,000 documents, and the feed bin will hold 3,000 documents.

Rental prices for the UNIVAC Bank Processor IV system begin at $3,480 per month, and purchase prices begin at $139,200.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Character:	6 bits	basic addressable data storage unit; holds 1 letter, numeral, or special symbol.
Punched card:	80 or 90 columns	primary 1004 input-output medium; generally holds 1 character per column.

.2 INFORMATION FORMATS

Type of Information	Representation
Numeral:	1 character.
Letter or special symbol:	1 character.
Field:	1 to 961 characters, delimited by plugboard wiring.
Instruction:	plugboard wiring; instructions are not stored internally.

SYSTEM CONFIGURATION

§ 031.

A UNIVAC 1004 system includes the following units:

- One 1004 Model I, II, or III Processor with built-in console and 961-character core memory.
- One Card Reader — peak speed is 400 cpm in 1004 I; 615 cpm in 1004 II and III.
- One Printer — peak speed is 400 lpm in 1004 I; 600 lpm in 1004 II and III.

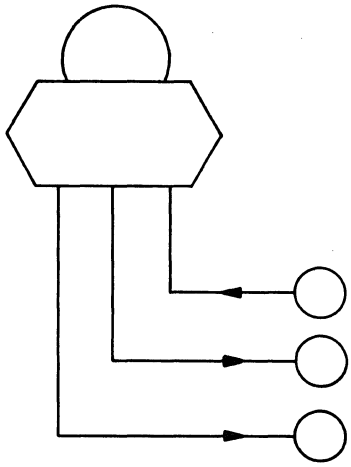
Other peripheral equipment that can be connected to a 1004 includes:

- One Card Punch or Card Read/Punch (200 cpm).
- One additional Card Reader (400 cpm).
- One Paper Tape Reader.
- One Paper Tape Punch.
- One Data Line Terminal, Type 1 or Type 2.
- One or two Uniservo Magnetic Tape Units (on 1004 III only).

§ 031.

.1 TYPICAL CARD SYSTEM; CONFIGURATION I (1004 I)

Deviations from Standard Configuration I: . . . . . core storage is 75% smaller.
62 "steps" instead of 1,000 instructions.
no index registers.
printer is 60% slower.
reader is 60% slower.

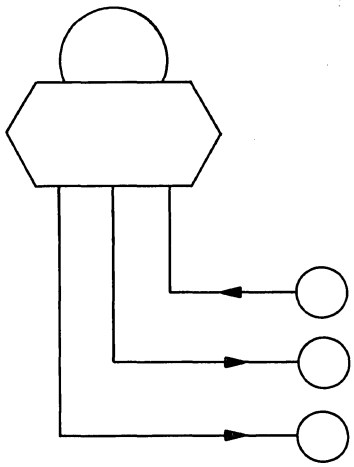


Equipment	Rental
Core Storage: 961 positions	
1004 I Card Processor, Model C: 8 μsec cycle, 80-column	$1,500
Card Reader: 400 cpm max.	
Printer: 400 lpm max.	
2009 Card Punch: 200 cpm	300
TOTAL:	$1,800

§ 031.

.2 TYPICAL CARD SYSTEM; CONFIGURATION I-A (1004 II)

Deviations from Standard Configuration I: . . . . . core storage is 75% smaller.
62 "steps" instead of 1,000 instructions.
no index registers.
printer is 37% slower.
reader is 40% slower.

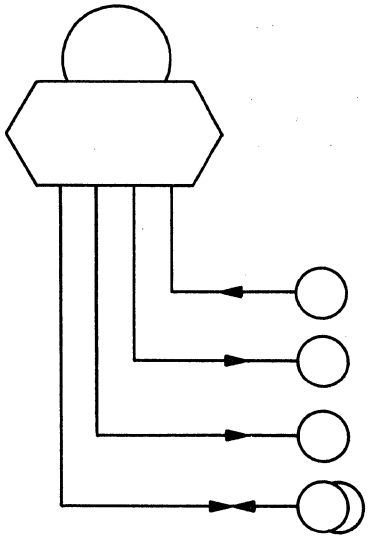


Equipment	Rental
Core Storage: 961 positions	
1004 I Card Processor, Model C: 6.5 μsec cycle, 80-column	$1,625
Card Reader: 615 cpm max.	
Printer: 600 lpm max.	
2009 Card Punch: 200 cpm	300
TOTAL:	$1,925

§ 031.

.3 4-TAPE BUSINESS SYSTEM; CONFIGURATION II (1004 III)

Deviations from Standard Configuration II: . . . . . core storage is 75% smaller.
62 "steps" instead of 1,000 instructions.
2 tapes instead of 4.
reader is 23% faster.
printer is 20% faster.
punch is 100% faster.
tape is 120% faster.



Equipment	Rental
Core Storage: 961 positions	
1004 III Magnetic Tape Processor, Model C: 6.5 μsec cycle, 80-column	$1,625
Card Reader: 615 cpm max.	
Printer: 600 lpm max.	
2009 Card Punch: 200 cpm	300
0857 Uniservos (2 tape drives and 1 control): 8/23/34KC	800
TOTAL:	$2,725

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . . Core Storage; contained in -
1004 I Card Processor.
1004 II Card Processor.
1004 III Magnetic Tape Processor.

.12 Basic Use: . . . . . working storage for data.

.13 Description

Each UNIVAC 1004 processor contains a core memory consisting of 961 six-bit character locations, each one of which is individually addressable. Core storage cycle time is 8.0 microseconds in the 1004 I processor and 6.5 microseconds in the newer 1004 II and III processors.

Each of the six cores comprising a character location is in a separate core plane, and each of the six planes consists of a 31-by-31 matrix (31 "rows" by 31 "columns"). A storage location is designated by an address made up of its row number (the R Address) and its column number (the C Address). For example, address R15/C3 refers to the third character location in the 15th row.

Input-output areas for card reading, card punching, and printing are fixed for any specific 1004 system; these areas are part of the 961-character core memory and can be used as working storage when not required for input-output purposes. Instructions are wired into a plugboard — not held in working storage as in all stored-program digital computers.

No parity checking, or any other form of redundancy checking, is performed upon data transferred into or out of core storage.

.14 Availability

1004 I: . . . . . 3 months.
1004 II: . . . . . 6 months.
1004 III: . . . . . 6 months.

.15 First Delivery

1004 I: . . . . . January, 1963.
1004 II: . . . . . June, 1964.
1004 III: . . . . . July, 1964.

.16 Reserved Storage

Purpose	Number of Locations	Locks
Index registers:	none.	
Arithmetic registers:	none.	
Logic registers:	none.	
I/O control —		
Card read area:	80, 90, or 160 char*	none.
Card punch area:	80, 90, or 160 char*	none.
Printer area:	132 char*	none.

*Areas or portions of areas not used for I/O can be made available for working storage.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.22 Physical Dimensions

.221 Magnetic core storage
Array size: . . . . . 31 by 31 by 6 bits.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by program: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . no interleaving.

.28 Access Technique: . . . coincident current.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates -
1004 I: . . . . . 125,000 cps.
1004 II and III: . . . . 154,000 cps.
Unit of data: . . . . . character
Conversion factor: . . 6 bits/character.
Data rate -
1004 I: . . . . . 125,000 char/sec.
1004 II and III: . . . . 154,000 char/sec.

§ 041.

.3 DATA CAPACITY: . . . 961 characters (one core storage module) per UNIVAC 1004 system.

.4 CONTROLLER: . . . . . no separate controller required.

.5 ACCESS TIMING

.51 Arrangement of Heads: . . . . . 1 access device per system.

.52 Simultaneous Operations: . . . . . none.

.53 Access Time Parameters and Variations

.531 For uniform access
Cycle time -
1004 I: . . . . . 8.0 μsec.
1004 II and III: . . . . 6.5 μsec.
For data unit of: . . . . 1 character.

.6 CHANGEABLE STORAGE: . . . . . no.

.7 PERFORMANCE

.72 Transfer Load Size: . . 1 to N characters, limited only by capacity of core storage.

.73 Effective Transfer Rate (With Self)

1004 I: . . . . . 62,400 char/sec.
1004 II and III: . . . . . 76,700 char/sec.

.8 ERRORS, CHECKS, AND ACTION: . . . . . no error checking is provided on core storage operations.

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 Processing Section:
1004 I.
1004 II.
1004 III.

.12 Description

The UNIVAC 1004 processor is an externally-programmed computer that works with variable-length fields. All processing is performed on a character-by-character basis. The 1004 has decimal addition, subtraction, and comparison facilities, and powerful editing features that include character insertion, zero suppression, and check protection. Functions such as multiplication, division, code translation, and table look-up can be accomplished through the use of simple wired subroutines.

The UNIVAC 1004 I Card Processor was first delivered in January 1963. It has 961 character positions of core storage with a cycle time of 8 microseconds per character, and can accommodate punched card, printer, and paper tape input-output equipment and data communication terminals, but not magnetic tape.

The 1004 II and III processors, announced in March 1964, have 961 character positions of core storage with a cycle time of 6.5 microseconds per character — 23% faster than the 1004 I. The 1004 II has the same input-output capabilities as the 1004 I, while the 1004 III can control one or two magnetic tape units in addition to the other facilities.

Typical processing times for 5-digit operands on the three 1004 models are as follows:

	1004 I	1004 II and III
Addition:	112 μsec	91 μsec
Multiplication (subroutine):	3,800 μsec	3,100 μsec
Division (subroutine):	7,100 μsec	6,000 μsec

The 1004 processor is able to handle two numeric machine codes — either the 80-column XS-3 code or the 90-column card code. The arithmetic circuits can use either code, as specified by plugboard wiring. The 90-column card code is already a 6-bit code, so no translation is required for 90-column systems. The 80-column code is a 12-bit code, and automatic translation is performed when 80-column cards are read or punched. Letters are regarded as bit patterns only, so a number of different codes can be used provided that the printer can be made to recognize the correct characters. An optional feature — Code Conversion — performs translations between the XS-3 code and the 90-column code automatically.

.12 Description (Contd.)

The "processing steps" that constitute a UNIVAC 1004 program are wired into a plugboard, not held in core storage. A maximum of 62 steps can be directly wired into the standard plugboard. Model A processors are able to use only 31 of these steps, Model B processors can use 47 steps, and Model C processors can use all 62 steps.

There are 21 different versions of the 1004 processor, with varying plugboard capacities, core storage speeds, and input-output capabilities. All 21 versions are listed in the Price Data section, Page 775:221.100. The following designations are used to distinguish between the various versions.

- Models I, II, and III

  These indicate the memory cycle time, and the ability to use one or two magnetic tape drives.

  Model I processors have a cycle time of 8.0 microseconds, and cannot use magnetic tapes.

  Model II processors have a cycle time of 6.5 microseconds, and cannot use magnetic tapes.

  Model III processors have a cycle time of 6.5 microseconds, and can use magnetic tapes.

- A, B, and C versions

  This designation indicates how much of the plugboard has been activated. All models use the same size plugboard, but in some models some parts of it are not functional.

  A versions have one-half of the plugboard activated (31 steps).

  B versions have approximately three-quarters of the plugboard activated (47 steps).

  C versions have the entire plugboard activated (62 steps).

- 80-column, 90-column, and 07 or 80/90 versions.

  Where a system uses one type of card exclusively, it is called an 80-column system or a 90-column system. Where both types of cards are used, it is called an 80/90 system and designated by an 07 after the actual model number (e.g., the 1004 I-07). In these 80/90 systems, the full 62-step plugboard is always activated.

The following section briefly explains the main concepts of external programming as practiced on the UNIVAC 1004. This is followed by a description of

§ 051.

.12 Description (Contd.)

the major facilities of the processor plugboard, which can be read independently. A diagram of the complete plugboard is shown in the Instruction List section, on page 770:121.102.

.121 Programming the 1004

The UNIVAC 1004 uses two-address instructions called "processing steps." The programmer specifies these by using wires to physically interconnect hubs on the processor plugboard. He may, for example, connect the hub for the function code of Step Number 3 to the hub representing Addition, the hub for Operand 1 of the same step to core storage address 213*, and the hub for Operand 2 to address 545, as illustrated in Figure 1. These actions would be equivalent to writing the machine-code instruction "Add 213, 545" for an internally-programmed computer. When a plugboard is used, the processor does not need to interpret the meaning of each instruction by means of a network of logical AND and OR gates. Instead, an electrical pulse is sent to the hubs which represent the program step and is picked up again from the hubs representing the correct function and operands, having passed along the wires which were inserted by the programmer when he "wired" the plugboard.

* The UNIVAC 1004 actually uses a more complex form of addressing, which is described in paragraph (f) of the next section. This form is used to simplify the illustrations in this section.

.121 Programming the 1004 (Contd.)

The basic instruction format is two-address, but some function codes do not use any operands. These include the input-output commands Read, Print, Punch, etc., which use fixed input-output areas so that the simple commands themselves are sufficient. An operation that requires no operand addresses can be specified at the same time as one of the two-address instructions. The programmer simply wires the plugboard so that when the particular step is "pulsed," the pulse is conducted to a hub for the appropriate operation. This pulse is picked up internally, and the operation is performed in parallel with the two-address instruction. Figure 2 shows how a Card Read operation can be wired on the same step as an Add operation.

The function codes that use the two-address format are Add, Subtract, Transfer, and Compare; all are variable-length operations. Editing is performed during Transfer operations. The result of a Compare operation is to set a physical relay (called a "comparator") to one of three conditions, usually corresponding to positive, negative, or zero. Other interpretations of these three positions are possible, depending upon the specific type of comparison which was performed (e.g., greater, less than, or equal results for a direct comparison, or identical or not identical results for an alphanumeric operation). Figure 3 shows the plugboard wiring for a typical Compare operation.

The setting of a comparator can be used to change the order of computation or the choice of operands, depending upon the program requirements. Operand

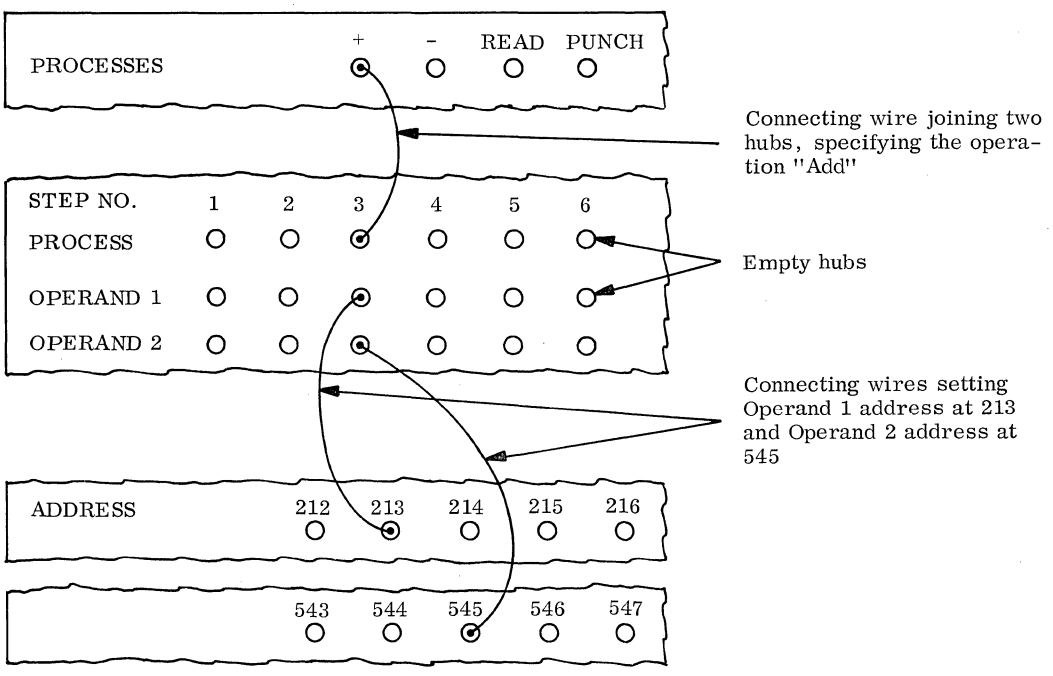


Figure 1: Partial view of a simplified plugboard showing electrical hubs for various program steps, addresses, and processes. Step 3 is shown wired for "Add the contents of 213 to the contents of 545."

§ 051.

.121 Programming the 1004 (Contd.)

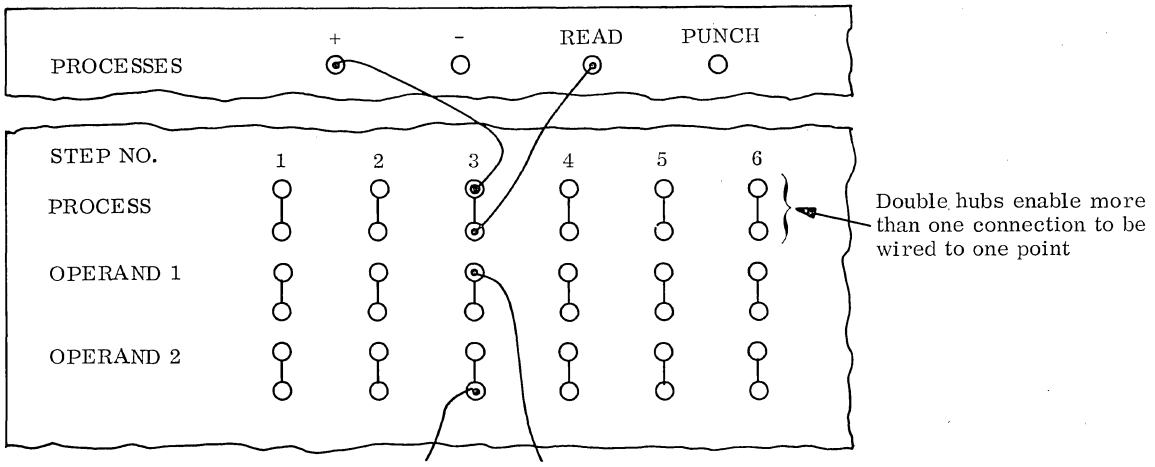


Figure 2: Partial view of a simplified plugboard showing double electrical hubs being used to specify an input operation without the use of an additional program step. Step 3 is shown wired to both an Add operation and a Card Read operation.

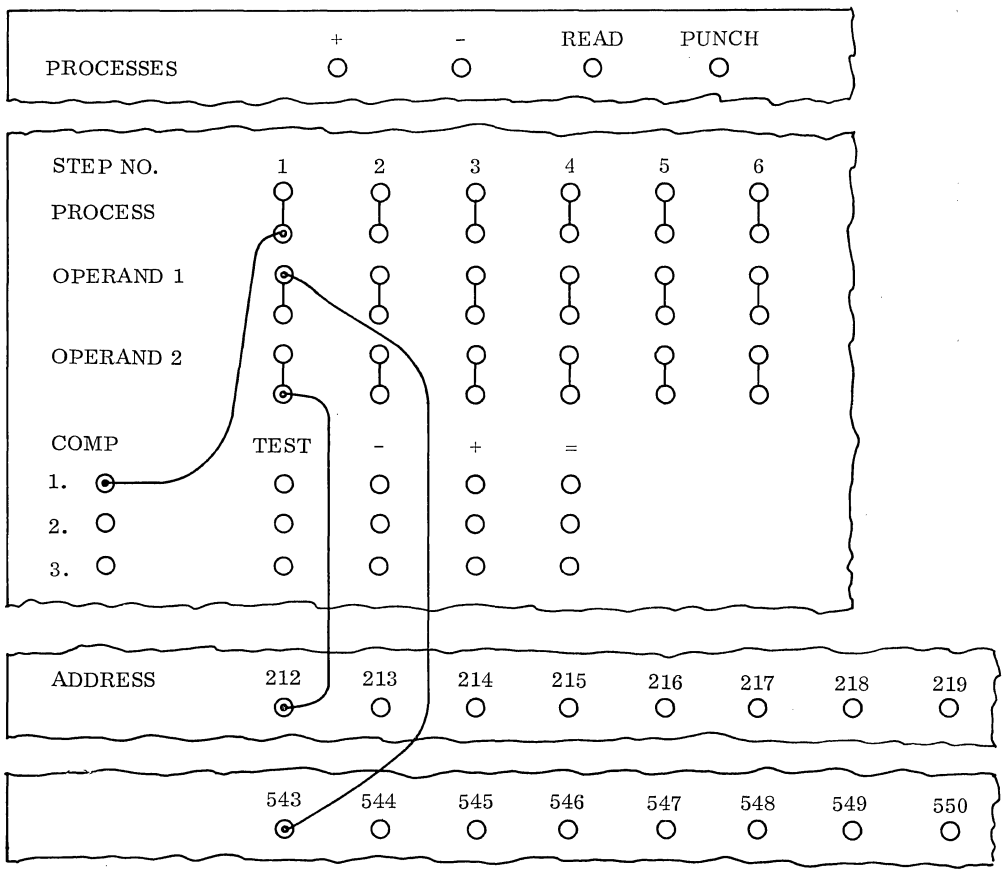


FIGURE 3: Partial view of a simplified plugboard showing the setting of a switch based upon the result of a comparison. Step 1 performs a comparison of the operands stored in locations 212 and 543 and sets Comparator 1 accordingly.

§ 051.

.121 Programming the 1004 (Contd.)

selection is performed by connecting the plugboard hub representing each of the possible conditions to the operand which is wanted under that condition. At the same time, an input hub to the comparator is used as the operand address of the instruction step. Then, when the electrical pulse is sent to the hubs for that particular instruction step, it will be picked up internally only at the operand position which corresponds to the current setting of the comparator. Figure 4 shows how a comparator setting can be used to select an operand in this manner.

Processing in the UNIVAC 1004 is performed in a serial, character-by-character manner. Operands can, therefore, be of any desired length. This capability is frequently utilized during the setting up of a plugboard program to make one operation perform a number of functional actions upon contiguous data fields. The most common case is where there are a number of sums to be generated. If these are

.121 Programming the 1004 (Contd.)

stored next to each other, all can be generated by a single instruction. For instance, if 1 is to be added to 5034, $5.67 to $10,389.00, and 28 to 30, the whole job can be done by a single instruction adding 000 001 000 000 567 000 028 to 005 034 001 038 900 000 030. By using the appropriate field length — in this case 21 digits — all the additions are performed in the same step; the processor simply works its way through the field in character-by-character fashion.

A further use of the plugboard for control purposes can occur while the character-by-character operation is taking place. After each character is processed and immediately before it is stored, an electrical pulse is sent ("emitted") to the plugboard hubs which represent its storage position. If its address position is not wired, then the character is stored in the normal way. However, if wires are connected to the appropriate hubs on the plugboard, electrical circuits are completed which can modify the store command so that some desired action can be taken at the same time.

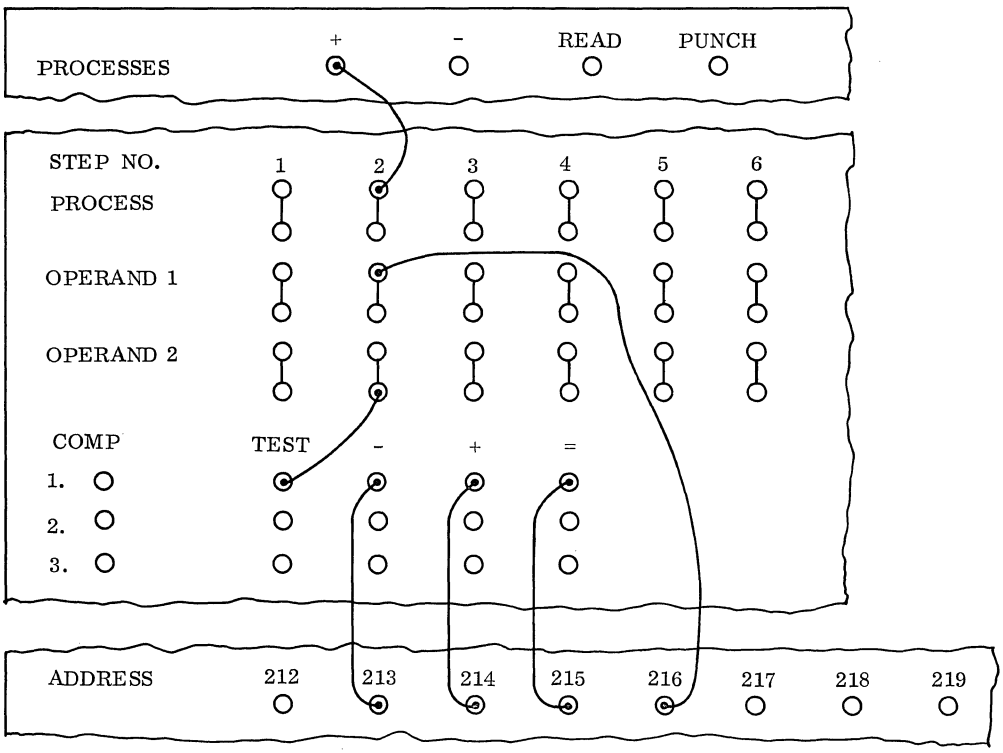


FIGURE 4: Partial view of a simplified plugboard showing the use of a switch to select an operand. Step 2 adds the contents of location 216 to one of three different locations, depending upon the present setting of Comparator 1.

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.121 Programming the 1004 (Contd.)

There are two main ways in which these store commands can be modified. In some cases, the operation itself may be changed. This provides the ability to insert characters, zero-suppress fields to be used for output purposes, delete characters, etc. In zero-suppression, for example, the plugboard addresses of the first and last characters of a field to be zero-suppressed are wired to the hubs "Start Zero-suppression" and "End Zero-suppression." Then, when the starting address is reached during a transfer, the store operation is modified to replace any leading zeros with space codes. Storing, with zero-suppression in operation, will continue until an address is reached which, when pulsed, allows the pulse to flow into the hub marked "End Zero-suppression."

Other cases where the store operation itself is modified mainly involve editing. Asterisks can be inserted instead of blanks for check protection purposes. Other characters, such as spaces, dollar signs, decimal points, commas, or zeros, can be inserted into a field; the character which would normally have been stored in that particular location is held back and stored in the next location.

The other way in which a store command can be modified brings the bit pattern of the character being stored directly to some hubs on the plugboard. This can be done by emitting a pulse for each "one" bit in the pattern from a set of hubs representing the six bit positions of the character being stored.* These pulses can be used to change the paths of some of the electrical connections, allowing changes to be made in the program sequence or in the choice of operands simply because some particular character has been stored in a specific location, and without any action of the program steps.

The programmer wires the board so that when electrical pulses representing the character being stored are emitted from the hubs, a pulse will pass through if, and only if, the desired character is being stored. Then the presence or absence of the pulse can be used to govern a two-way switch that is similar in other ways to the three-way comparators mentioned above. These two-way switches, called "selectors," can later be used by the programmer to route the program according to his needs.

For instance, suppose that the first column of a card is a control column, with different punchings to represent an issue note, a receipt, or some other type of transaction. Then by properly wiring core storage position 1 (which is the first column position of the standard card input area), the storage of the control character into this location will automatically cause the changes which the programmer desires in the various wired networks. No change in the program itself is needed — the source of control here is the actual data being stored.

* The UNIVAC 1004, in fact, has two hubs for each of the six bit positions. One is pulsed if the corresponding bit is a "one," and the other if it is a "zero."

.121 Programming the 1004 (Contd.)

A plugboard program, therefore, has two independent, complementary portions: a sequential portion much like ordinary internally-stored programs, and another portion which is sensitive to the data and environment factors. The power of plugboard-programmed systems like the UNIVAC 1004 is often restricted mainly by the physical configuration of the plugboard and the ability of the programmer to get the wires into position, rather than by the logical limitations of the instruction facilities.

.122 The 1004 Plugboard

The UNIVAC 1004 plugboard is a large one, having a maximum size of 80 by 64 hubs. Not all of these hubs are activated in all options. The plugboard's main components are:

(a) Program Steps

There are 31 steps in the basic system (Model A); 47 or 62 steps are available in Model B or C, respectively. Each program step has six hubs that can be connected to operands, processes, and other facilities.

(b) Operations

- Addition and subtraction: Available in both algebraic and absolute form. No multiplication or division facilities are directly available; the standard multiply and divide subroutines require four and seven steps, respectively.

- Transfers: Transfers of any length can be programmed. Editing can be done during transfers. Facilities include the insertion and deletion of characters, zero suppression and replacement with either spaces or asterisks, optional deletion of zero balances, bit superimposition, and specialized treatments of signs and zone bits.

- Input/Output Operations: Card Read, Card Punch, Print, Printer Space (under control of a two-level paper tape loop), Magnetic Tape Read, Write, Write and Check, Backspace, and Rewind operations are available, as well as special operations for other peripheral devices.

  Some of these operations can overlap other input/output operations; details are given in the Simultaneous Operations section (770:111).

(c) Other Facilities

A number of other hubs are used to control various modes of operation. These include the types of editing available, overflow and sentinel tests, printer control signals, and specific character generators for C, D, G, R, T, $, *, -, +, period, and comma. Bit generators can be used to create other desired characters.

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.122 The 1004 Plugboard (Contd.)

(d) Switches

These are two or three-way switches which are set by the program, by data, or by the operator. The switches are used as the variable connectors in the networks which control the program. The full plugboard has ten 3-way comparators, sixty 2-way general purpose selectors, each with four sets of switches; twenty 2-way program selects; and four 2-way holds reflecting the setting of console switches.

(e) Auxiliary Hardware

To set up the switching networks needed for the program, a large number of auxiliary connectors are needed. Sometimes it is necessary to bring a number of paths together. For this purpose a connector is used. The UNIVAC 1004 plugboard has 102 such connectors, mostly consisting of 8 hubs connected to 2 hubs. Sometimes, on the other hand, a single pulse must be sent along a number of paths. For this purpose, "distributors" are used, and the full plugboard has 160 of these.

(f) Store Address Hubs

There are two complete sets of "store address" hubs on the plugboard. One set is used for Operand 1 references and the other set for Operand 2 references. The core memory is considered as a 31-row by 31-column matrix holding 961 alphanumeric characters in all. To wire the address of a particular location, both the row number and the column number of the location must be connected to the Operand hubs of the program step concerned. To indicate a field, the addresses of both its first and last character positions must be wired.

Further control is provided by 80 "address combines." These usually emit a pulse if the following conditions are simultaneously satisfied: (1) the presence of a specific pulse coming from the storage address being used and the data to be stored during an operation, and (2) the absence of an inhibiting pulse from anywhere else on the board. The address combines are often used to restrict some special function (such as editing) so that it will occur only when the data is moved by one particular program step.

.123 Optional Features

Code Image: Permits two characters in the 6-bit XS-3 code to be read from or punched into each column of a standard 80-column card by suspending the automatic translation between the usual Hollerith card code and the XS-3 internal code. This doubles the effective data capacity of an 80-column card to 160 characters. The Code Image feature is available in two forms: for card reading only or for both reading and punching.

Code Conversion: Allows automatic translation between the XS-3 (80-column card) code and the 90-column card code. It is available only with processors which have a 62-step plugboard, and prevents the installation of a Data Line Terminal in the processor. When Code Conversion is installed, the printer can print from either of the two internal codes, as selected by program, and the card readers can read either type of card. Any card punches connected to the system are restricted to being either 80-column or 90-column punches, but either type of punch can be connected and serviced by a computer with the Code Conversion feature. In an installation which has both types of punch available, changing over from one punch to the other is a manual operation which takes two or three minutes.

Translate Feature: Allows automatic conversion between any two six-bit codes. (A five-bit code, or any code with less than six bits, can be regarded as a six-bit code.) The translation process uses a table stored in memory containing the 64 characters of the code to be used. These character codes are stored in addresses based on the binary patterns of the 64 characters of the code they are to replace. Where translation is to take place in both directions, or where more than one code is to be translated, additional 64-character tables are required.

Card Processor Expansion Kits: The UNIVAC 1004 is capable of field conversion either by increasing the capacity of the plugboard beyond its basic size of 31 steps or by converting a 1004 I into a 1004 II or III. The Card Processor Expansion Kits are designed to increase the plugboard from either 31 steps (an A model) to 47 steps (a B model) or from the 47-step B model to a full 62-step C model. A, B, and C model processors are available for either 80-column or 90-column cards, and for 1004 I, II, or III processors.

.13 Availability

1004 I: . . . . . 3 months.
1004 II:. . . . . 6 months.
1004 III: . . . . . 6 months.

.14 First Delivery

1004 I: . . . . . January, 1963.
1004 II:. . . . . June, 1964.
1004 III: . . . . . July, 1964.

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.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add-subtract:	automatic	decimal	1 to N char.
	Multiply:	subroutine	decimal	1 to N char.
	Divide:	subroutine	decimal	1 to N char.
.212	Floating point:	none.		
.213	Boolean —			
	AND:	none.		
	Inclusive OR:	automatic	binary	1 to N char.
.214	Comparison —			
	Numbers:	automatic		1 to N char.
	Absolute:	automatic		1 to N char.
	Letters:	automatic		1 to N char.
	Mixed:	automatic		1 to N char.

Collating sequence:

Only numeric data is regarded as having a collating sequence, which is 0 through 9. Letters and special characters are regarded as "patterns" which, when compared, can only be found "identical" or "not identical."
Where there is a direct relationship between the binary magnitudes of the codes assigned to the various alphabetic characters (as in 80-column card systems), then a routine can be written which effectively provides alphanumeric comparisons. Where such a direct relationship does not exist (as in the 90-column systems), then such a routine will not work.

		Provision	Between	And	Size
.215	Code translation:	automatic	internal XS-3 code	80-column card code	1 to 80 columns.
		automatic*	XS-3 code	90-column card code	1 to N characters.
		automatic*	any 6-bit code	any 6-bit code	1 to N characters.

* With optional equipment.

.216 Radix conversion:. . . . none.

		Provision	Size
.217	Edit format —		
	Alter size:	automatic	1 to N characters.
	Suppress zero:	automatic	
	Round off:	none.	
	Insert point:	automatic	
	Insert spaces:	automatic	
	Insert CDGRT., $*-+ :	automatic	
	Float $:	none.	
	Protection:	automatic	

.218 Table look-up:. . . . . subroutine.

.22 Special Cases of Operands

.221 Negative numbers —
80-column systems: . zone bit in least significant digit.
90-column systems: . zero bit in least significant digit.
.222 Zero:. . . . . 2 forms: +0 and -0.
.223 Operand size determination: . . . . . location of least and most significant digits is specified in each operand address.

.23 Instruction Formats (See Description, Paragraph .12, for complete description)

.231 Basic instruction structure:. . . . . plugboard wiring defines process to be performed and 2 operands. The operands are chosen at execution time, and the choice may be conditional upon the setting of various switches.
.232 Instruction layout: . . . wired in "steps" on plugboard; each step contains the following hubs:

- o Process
- Operand 1
- Operand 2
- o Step Sequence Change

.233 Instruction parts

Name	Purpose
Process:.	operation to be performed.
Operands 1 and 2:. . .	most significant location and least significant location of each data field to be operated upon.
Step Sequence Change:	used to initiate changes in program sequence.

§ 051.

.234 Basic address structure: . . . . . 2-address steps; operands are addressed by row and column numbers of their most significant and least significant locations (e.g., R1C2-R1C9 indicates field begins at row 1, column 2 and ends at row 1, column 9).

.235 Literals: . . . . . one character, for comparisons and tests only.

.236 Directly addressed operands: . . . . . 1 to 961 characters, in core storage.

.237 Address indexing:. . . . none.

.238 Indirect addressing: . . none.

.239 Stepping:. . . . . none.

.24 Special Processor Storage: . . . . . none.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: sequencing is either:
(1) indicated by plugboard wiring; or
(2) implied (i.e., next higher numbered step) if not wired.

.32 Look-Ahead: . . . . . none.

.33 Interruption: . . . . . none.

.34 Multi-running: . . . . . none.

.35 Multi-sequencing:. . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

D = operand length in decimal digits.
C = operand length in characters.

	1004 I	1004 II and III
.411 Fixed point —		
Add-subtract:	32 + 16D	26 + 13D
Multiply:	Subroutine	Subroutine.
Divide:	Subroutine	Subroutine.
.413 Additional allowance for unlike signs:	16D	13D
.414 Control —		
Compare:	40 + 16C	32.5 + 13C
Branch:	no additional time	no additional time.
.415 Counter control:	none	none.
.416 Edit:	32 + 16E + 16S where E = number of characters in edited field; S = number of fields with specialized treatment (zero-suppress, superimpose, etc.)	26 + 13E + 13S

.42 Processor Performance in Microseconds

	1004 I	1004 II
.421 For random addresses		
c = a + b:	64 + 32D	52 + 26D
b = a + b:	32 + 16D	26 + 13D
Sum N items:	(32 + 16D)N	(26 + 13D)N
c = ab:	2,000 to 8,000*	1,800 to 6,500*
c = a/b:	3,000 to 16,000*	2,700 to 14,000*
.422 For arrays of data:	**	**
.423 Branch based on comparison:	**	**

* These multiplication and division times are based on 4- to 8-digit operands and will vary depending upon data values, choice of subroutines, etc.

** No performance times are listed for items .422 and .423 because the standard methods for computing these times are not suitable for the plugboard-programmed 1004.

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.424	Switching —		
	Unchecked:	no additional time	no additional time.
	Checked:	no additional time	no additional time.
	List search (N items):	120N	97.5N
.425	Format control, per character —		
	Unpack:	17.6	14.3
	Compose:	20.3	16.4
.426	Table look up, per comparison —		
	For a match:	120	97.5
	For least or greatest:	176	136.5
	For interpolation point:	120	97.5
.428	Moving:	32 + 16C	26 + 13C

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	set program-testable switch.
Underflow:	none.	
Zero divisor:	software check	as programmed.
Invalid data:	none.	
Missing operation:	check	processor stalls.
Arithmetic error:	none.	
Invalid address:	check	processor stalls.
Receipt of data:	none.	
Dispatch of data:	none.	

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . Display Panel.
Control Panel.
Test Switch Panel.

.12 Description

The UNIVAC 1004 does not have a separate console. A Control Panel and a Display Panel are mounted in open view on the main frame, while a Test Switch Panel is covered during normal running. There is no provision for an operator's seat or for working space; the system is normally controlled by a standing operator. See page 770:001.002 for an illustration of the UNIVAC 1004 Card Processor showing its console control facilities.

The Control Panel handles initialization and similar actions; the Test Switch Panel sets up the conditions under which the system will operate (continuous running or step-by-step, etc.); and the Display Panel monitors the existing conditions during operation. Further details of these three panels are presented below.

Operator communication with the 1004 system is more restricted than in most internally-programmed computer systems; however, it is adequate for the types of operation handled by the system. Use of the Display Panel to isolate the particular points of immediate interest to whoever is operating the system — be it operator, programmer, or engineer — allows operations to be conducted in a simple and efficient manner.

.12 Description (Contd.)

Display Panel

The Display Panel is located on the upper front of the Processor at the extreme right. This panel contains some 280 indicator lights to portray different phases of the Processor's operation. The design of the Display Panel is unusual and provides a programmer with most of the necessary program checkout facilities.

The internal panel housing the indicators contains 36 rows of eight indicators per row. The Display Panel cover contains four horizontal slots in which four rows of eight indications are visible at any one time. The remaining 32 rows of indicators are masked by this cover and are not visible. The set of indicators displayed at any one time is termed a "Display Mask." The inner panel housing the indicators is positioned vertically by means of a knurled wheel at the left of the panel. Each display mask is lettered appropriately for simple reading. The functions of the nine Display Masks are listed in Table I.

TABLE I: FUNCTIONS OF THE DISPLAY MASKS

Mask No.	Display Items	Display Usage
1	displays bit or character generation.	program analysis.
2	decoding chart for storage locations of operands.	program analysis.
3	displays contents of the Data Register and control conditions during Arithmetic or Transfer steps.	program analysis.
4	indicates reason for Processor stoppage during continuous operation, and displays I/O operations.	normal operation monitoring.
5 and 6	indicate step just completed when the STOP indicator is lit during continuous operation.	program analysis.
7	indicates processes, transfers, and test results.	program analysis.
8	indicates the six Processor cycles and Program Select Power.	program analysis.
9	indicates present comparator results.	program analysis.

§ 061.

.12 Description (Contd.)

Control Panel

The Control Panel consists of three sections. Control Panels 1 and 2 are located on the left portion of the Processor on either side of the printing section. They contain controls to turn the power on and off and to adjust the printer. The third section of the Control Panel is the Central Control Panel. This is located to the right of Control Panel 2 and provides switches for altering, clearing, starting, and stopping a program and for manual card feeding.

.12 Description (Contd.)

Test Switch Panel

The Test Switch Panel is a covered section of the console, located below the Central Control Panel. By means of the switches on this panel:

- Program Select Control can be set.
- The Step Counter can be adjusted to start at, stop at, or repeat a particular step.
- The contents of a location in core storage can be read.
- A character or bit pattern can be written into a core storage location.
- One or more cards can be fed arbitrarily.

INPUT–OUTPUT: CARD READERS

§ 071.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 I Card Reader.
UNIVAC 1004 II/III Card Reader.
Model 0704 Auxiliary Card Reader.

.12 Description

A card reader which can read either 80-column or 90-column cards is included as an integral part of each 1004 processor. The reader operates at a peak speed of 400 cards per minute in 1004 I systems and 615 cards per minute in 1004 II and III systems. There is only one stacker on the reader, so it is not possible to sort cards as part of the input process.

In systems using 80-column cards, it is possible to mix standard card punching with binary punching, thus allowing a larger amount of data to be held on a single card. Plugboard control can be used to switch the type of translation as required, on a column-by-column basis.

In a Model 07 processor, both 80-column and 90-column translation logic is available, and 80-column and 90-column cards can be read by the same reader and intermixed if desired.

A second, optional reader is available, which is functionally identical to the standard reader in the 1004 I processor except that it has three output stackers so that limited sorting operations can be performed on a card file during processing. The optional reader also has a wait station after the reading station to allow time for program selection of the stackers.

All the readers are photoelectric and read a column at a time. Error checking of the actual read operation is not provided; instead, UNIVAC relies on checking that each of the photoelectric cells is operational before each card is read. The use of a wait station before the actual read station is said to minimize problems related to card positioning, card size variation, and card friction.

Card reading can also be handled by the Card Read/Punch units which are described in the next section of this report (770:072.100).

A major advantage of having two card readers on-line with a 1004 system is that this enables two separate card files to be processed together without any need for collation or decollation of the cards. Typically, a master inventory file and a daily transaction file could be processed together to produce the necessary documentation from the printer.

.12 Description

Card reading can be overlapped with printing and card punching, but not with processing. When full cards are being read, the maximum speed of the 1004 I and 1004 II/III readers is 365 and 615 cards per minute, respectively. This reading speed can be maintained only if the amount of processing per card is comparatively small — under five milliseconds. The card reading speed is proportionately reduced as the amount of processing per card increases. However, the time available for processing at a specific speed can be increased when only the first portion of the card image is needed. Card reading is done on a column-by-column basis and can be stopped at any particular position; but, once it has been stopped, reading cannot be restarted on the same card. The speed achieved is related to the number of columns read. Details of this mode, and other factors which differ among the eight different readers available for the 1004 system, are presented in Table I.

Fixed input areas in the core store are used for card read operations. The actual position of these areas depends on the reader models involved. In the case of 80-column readers, the size of the area differs depending upon whether the cards are being used normally (one character per column, which is automatically translated into the internal 6-bit code during the read operation) or whether column binary cards are being read. Column binary cards use the 12 punch positions in each card column to hold two 6-bit characters. These are read into the core memory untranslated, so a single card fills up to 160 character positions.

The operator uses Display Mask 4 during normal running. This provides him with a display indication when the card reader requires attention — loading, unloading, clearing card jams, etc. The frequency of such attention depends on the operational speed, as well as on the size and number of the hoppers. All the input hoppers can hold 1,000 cards, and the Auxiliary Card Reader has 3 output hoppers which will handle 1,500 cards each. Selection of the output hoppers is accomplished by programming. Under full reading speed conditions, some attention by the operator will be needed at least 3 times every 5 minutes.

Optional Features

Short Card Feeding: Allows the reader to feed and read stub cards (51-column or 66-column cards in the 80-column mode, 29-column cards in the 90-column mode). The device consists of two inserts for the input magazine and a filler for the card stacker.

80/90-Column Read: Permits both 80-column and 90-column cards to be read by the same reader. A 62-step (Model C) processor is a prerequisite.

§ 071.

TABLE I: DETAILS OF THE CARD READERS FOR UNIVAC 1004 SYSTEMS

1004 Model	Reader Model	Maximum Speed, cards/min.	Processing Time Available at Max. Speed, msec	Speed Decrease per msec of Added Processing	Add'l. Processing Time per Column Not Read, msec	
					80-column	90-column*
I	Std.	400 (365 when full cards are read)	none	2 cards/min.	1.4	2.5
II or III	Std.	615	5.5	3 cards/min.	0.8	1.4
I, II, or III	0704 Aux. Reader	400 (365 when full cards are read)	none	2 cards/min.	1.4	2.5

* A "column" here consists of the upper and lower character positions in one column of a 90-column card; e.g., character positions 1 and 46 are in the first card column, positions 2 and 47 are in the second column, etc. It should be noted that a "90-column" card actually contains only 45 vertical columns, each of which normally holds two characters.

INPUT–OUTPUT: CARD PUNCHES

§ 072.

.1 GENERAL

.11 Identity: . . . . . Card Punch, Models 2009 and 2011.
Read/Punch Units, Models 2009, 2011.

.12 Description

No card punch is included as an integral part of the 1004 processor, although the standard card reader and printer are physically incorporated into the processor cabinet. An optional punch unit operates at a maximum speed of 200 cards per minute. It is available either as a simple punch or as a read/punch unit produced by incorporating a read station in front of the punch station.

There are two output stackers on the card punch units — a normal stacker and an error stacker for cards where some punch malfunction has been detected. In the basic unit the program cannot deflect a card into the second (error) stacker, but an optional modification is available which provides this facility.

In any specific system, either an 80-column or a 90-column card punch model must be used. It is not possible to use the same unit to punch both 80-column and 90-column cards.

The major advantage of having a punch within the system is that updated card files can be maintained automatically. A read/punch unit has the additional advantages of being able to punch processor-generated results directly into each transaction card or serve as a second card reader. This allows two separate files to be processed together without any need for collation or decollation of cards.

Card punching and/or reading, once initiated, can be overlapped with any other input-output operation or with processing. Punching is a row-by-row operation, and there is no limit on the number of holes which can be punched into a single card.

Fixed output areas are used for punching. The actual position of these areas in core storage

.12 Description (Contd.)

depends upon the punch models involved and, in the case of 80-column cards, on whether column binary punching is being done. Column binary cards use the 12 punch positions in each column to hold two 6-bit characters, thus doubling the potential data capacity of the card.

The operator uses Display Mask 4 during normal running. This provides him with a display indication when the equipment requires attention — card loading or unloading, forced stalls, or other contingencies. The frequency with which such attention will be needed depends on the operational speeds as well as the 1,000-card capacity of the input hopper and the 1,000-card capacity of the main output stacker. Under full speed operation, some attention will have to be given at least 2 times every 5 minutes.

A weighted hole count check is performed after each punch operation. This provides protection against any single punching error, or against compensating errors provided that they do not occur in the same row. If an error is found, the card is diverted into an error stacker which can hold up to 1,000 cards. At the same time, the processor can optionally be stalled.

Optional Features.

- Card Punch Selective Stacker: Allows the program to divert a card into the second (error) stacker.
- Scored Card Feature: Allows scored cards to be punched on the card punches.
- Card Read/Punch Feature: Adds a read station in front of the punch station. Cards can be read only, punched only, or both read and punched. This feature is available for both 80-column and 90-column punches.
- Code Image: Allows cards to be punched, either wholly or in part, in the internal machine code rather than the conventional card code. This feature applies only to 80-column card punches, and provides a theoretical maximum data capacity of 160 characters per card.

INPUT–OUTPUT: PAPER TAPE EQUIPMENT

§ 074.

.1 GENERAL

.11 Identity: . . . . . Paper Tape Reader, Model 0902.
Paper Tape Punch, Model F 0606.

.12 Description

The Model 0902 Paper Tape Reader operates at 400 characters per second, and the Model F 0606 Paper Tape Punch punches at 110 characters per second. One reader and/or one punch can be connected to any UNIVAC 1004 in addition to any other peripheral equipment. Field connection of the paper tape units is possible.

Paper tape with 5, 6, 7, or 8 tracks can be read and punched; the different tape widths involved are handled by a manual adjustment. Because the basic character code of the UNIVAC 1004 has six bits, special arrangements are needed for 7- or 8-track tape. This is handled in one of two ways, depending on whether or not there are more than six data bits in the paper tape character:

- If there are more than six data bits, each character is split into two portions, one consisting of six bits, and the other consisting of the remaining one or two bits. These are stored in contiguous character positions in the core storage, two UNIVAC 1004 character positions being allocated for each paper tape character.

- If there are only six data bits, the additional bits are stripped off during input or generated during output, and the six data bits are stored in a single core position.

The second situation occurs when, as in most current paper tape codes, the additional tracks are used for such purposes as parity checks and control functions (e.g., for an "end-of-line" indication). Odd parity can be checked by the hardware during input and generated during output. Even parity checking and generation is available by special request. The presence of a control character can be used to generate a pulse from the appropriate plugboard hub during input, and can be similarly created by such a pulse during output.

.12 Description (Contd.)

The position of the various tracks on the paper tape (data tracks 1 through 6, the parity track, the control track, etc.) is important, because, while they can be rearranged to suit the installation, this rearrangement is fixed before the installation takes place, and cannot be varied to suit a particular program or a particular tape source. These track positions are rearranged before the data enters or leaves the computer. This facility provides flexibility in dealing with certain paper tape codes which might otherwise require more complex internal processing.

Special translation routines exist for the Flexowriter paper tape code and a version of the ASCII code.

Data blocks of up to 960 internal characters (480 tape characters if two internal characters are being used to store one tape character) can be handled in a single paper tape input or output instruction. Reading can overlap printing, but not card reading (some of the circuits are shared) or processing. Paper tape punching can overlap printing or processing, but not card punching. A photoelectric system is used for the reading operation, while punching is handled by a conventional die punch system. Chadless tape (where the holes are not fully punched) is not acceptable to this equipment. In both the reader and the punch, the operation is character-by-character, and the equipment is able to stop between characters.

The F 0606 Paper Tape Punch is the familiar Teletype BRPE unit. Physically, the paper tape equipment is of small size and is mounted on the main frame of the 1004. The reader is mounted on the side of the punched card reader, and the punch on the side of the printer or card punch.

INPUT–OUTPUT: PRINTERS

§ 081.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 I Printer.
UNIVAC 1004 II/III Printer.

.12 Description

A printer is included as an integral part of each 1004 processor. Its rated speed is 300 lines per minute in the 1004 I and 600 lines per minute in the later 1004 II and III systems. Field conversion of the original printers so that they work at the faster rate is possible, and is part of the general conversion of 1004 I systems to 1004 II or III systems.

The print line consists of 132 positions at 1/10th-inch horizontal spacing and either 1/6th- or 1/8th-inch vertical spacing, at the operator's option. Sixty-three printable characters are available on the standard print drum, and the operational speeds quoted above assume that all these are in use. If fewer than 63 different characters are used, the asynchronous operation of the printer permits increased speeds, as shown in the accompanying graphs.

Skipping speeds for all printers is 20 inches per second, and the paper forms may be from 4 inches to 22 inches wide. Format control is provided by a three-column paper tape loop.

.12 Description (Contd.)

The same printer model is used in both 80-column and 90-column 1004 systems. The different codes used in these systems for the various printable characters are interpreted appropriately under control of the plugboard hub which indicates which code is being used in the processor.

Printing can be overlapped with card reading or card punching, but not with processing. Paper movement, which takes place after the printing has been completed, is handled as an off-line operation and can be overlapped with computation.

The characters are stored on the print drum in the order A through Z, followed by 0 through 9, and then the characters - * . / , $ + (') = ; > : < [! ?] △ \ ≠ @ % # and □.

A fixed output area in core storage is used to hold the data to be printed.

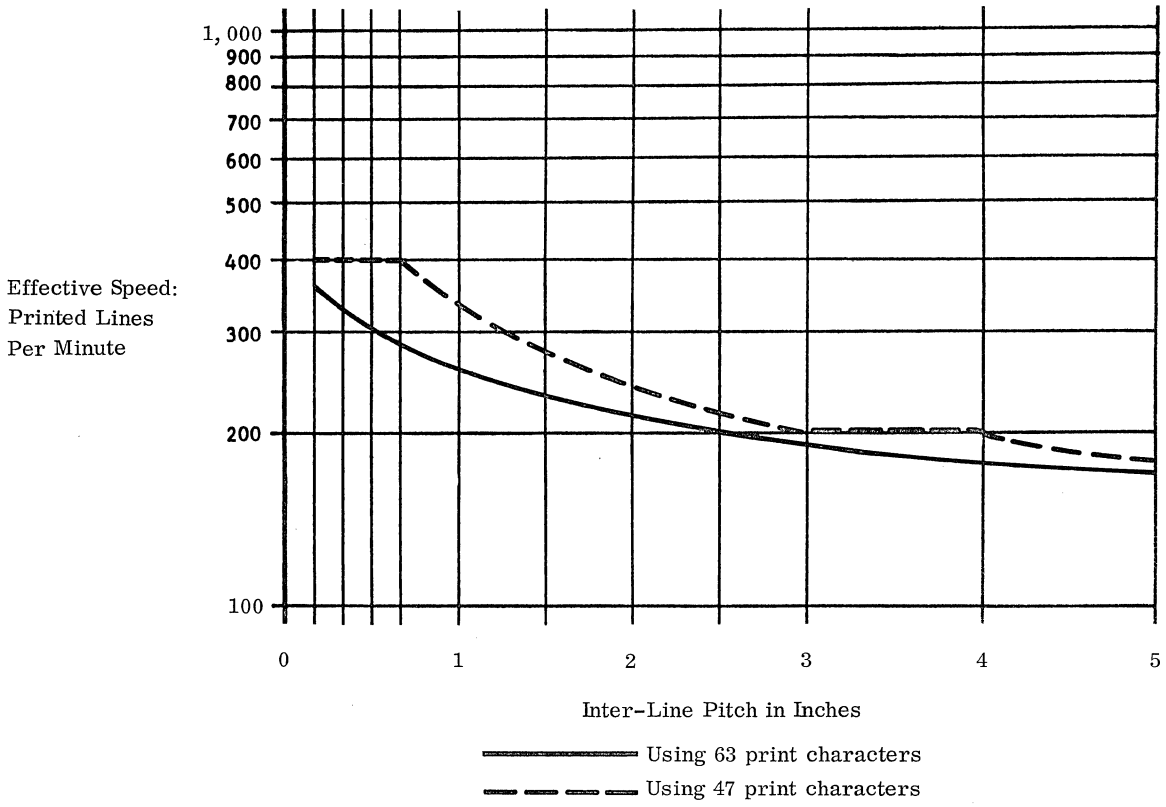
No error checks are made on the accuracy of the actual printing.

Only one printer can be connected to a single UNIVAC 1004 system.

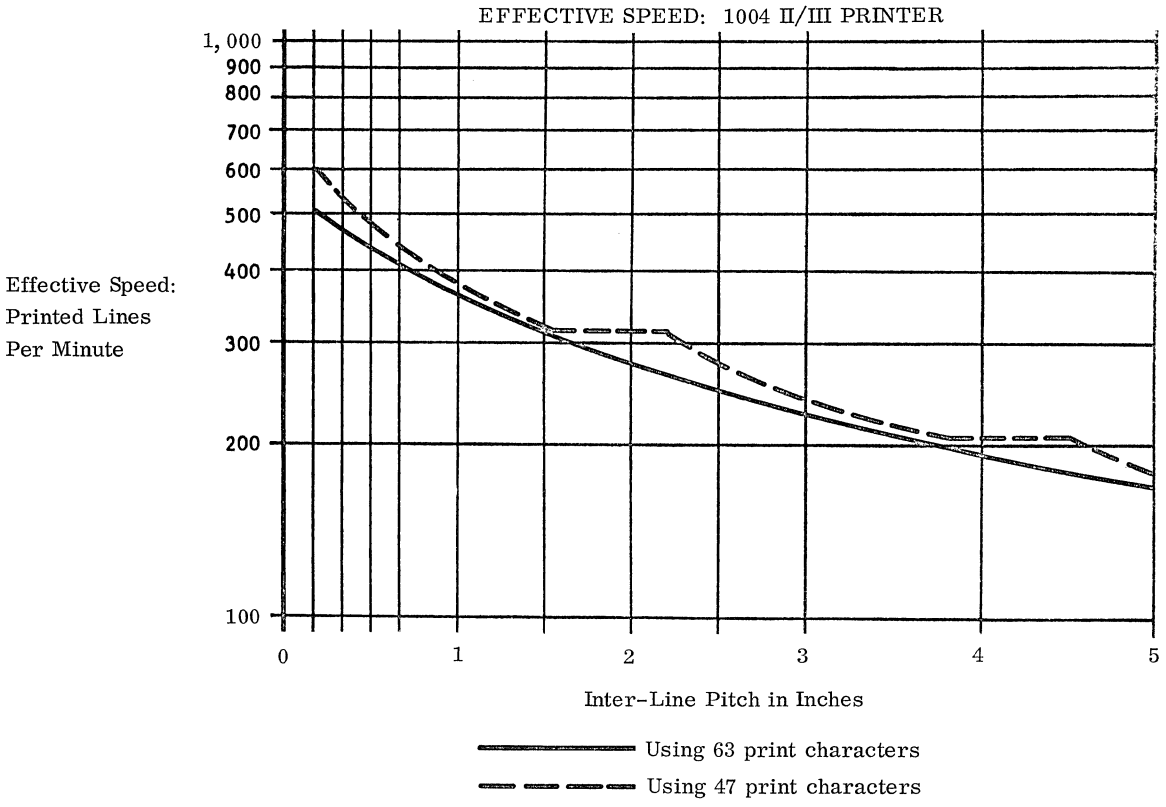
The printer delivery and availability is the same as that of the 1004 system itself; i.e., first deliveries of the original 1004 I in January 1963, the 1004 II in June 1964, and the 1004 III in July 1964. Availability is between 60 and 180 days, depending on the processor model.

§ 081.

EFFECTIVE SPEED: 1004 I PRINTER



EFFECTIVE SPEED: 1004 II/III PRINTER



INPUT–OUTPUT: MAGNETIC TAPE

§ 091.

.1 GENERAL

.11 Identity: . . . . . Uniservo and Control, Model 0857-00. Uniservo (without Control), Model 0857-02.

.12 Description

A UNIVAC 1004 III Magnetic Tape System can have one or two Model 0857 Uniservo magnetic tape units with a maximum transfer rate of 33,664 characters per second. Any 1004 system can be field-converted into a 1004 III, and can subsequently accept either magnetic tapes written by UNIVAC systems using XS-3 coding or, with program translation, tapes using other 6-bit coding systems such as the IBM BCD code. Recording densities of 200, 556, or 800 characters per inch can be used and odd or even parity is program-selectable. These Uniservo magnetic tape units also have the same read-after-write error checking as IBM 729 and 7330 magnetic tape units, so properly recorded magnetic tapes can be interchanged between the 1004 and computer systems of the IBM 1400 and 7000 series.

Magnetic tape reading or writing can be overlapped with printing or card reading, but not with internal processing. The relatively high speed of the tape units, compared to the mechanical speeds of the reader and punch unit, makes it possible to run card-to-tape and tape-to-printer data transcription operations in parallel.

Because a maximum of two tape servos can be connected when file updating operations are in process, it is normally not possible to avoid losing the rewind time through tape swapping or similar means. The rewind speed of 190 inches per second controls the time lost through rewinds, and rewinding a 2,400-foot reel takes under 3 minutes.

Data can be recorded in variable-length blocks separated by a three-quarter inch interblock gap. The input-output area in core storage can be any length up to 961 characters. The programmed operations for magnetic tape are Read Forward, Write Forward, Backspace One Block, Transport Select, and Data Ignore. The Data Ignore instruction allows tape blocks which are larger than the core memory size to be read into the UNIVAC 1004. This is done by reading part of the block, coasting over the rest of the block, backspacing, coasting over the first portion of the block and reading the second portion, etc.

.13 Availability: . . . . . 6 months.

.14 First Delivery: . . . . . July, 1964.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . . pinch roller friction; capstan drive.

.212 Reservoirs –
- Number: . . . . . 2.
- Form: . . . . . vacuum.
- Capacity: . . . . . 1 foot of tape.

.213 Feed drive: . . . . . electric motor.

.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by a magnetic write head.

.222 Sensing system: . . . . . magnetic read head.

.223 Common system: . . . . no.

.23 Multiple Copies: . . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . mylar tape.

.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . 1 to 961 rows, at 200, 556, or 800 rows/inch.

.322 Parallel by: . . . . . 7 tracks.

.324 Track use –
- Data: . . . . . 6.
- Redundancy check: . . 1.
- Timing: . . . . . 0.
- Control signals: . . . . 0.
- Unused: . . . . . 0.
- Total: . . . . . 7.

.325 Row use –
- Data: . . . . . all.
- Redundancy check: . . 1 per block.
- Timing: . . . . . 0.
- Control signals: . . . . 0.
- Unused: . . . . . 0.
- Interblock gap: . . . . . 0.75 inch.

§ 091.

.33 Coding:. . . . . any 6-bit data code; UNIVAC XS-3 or IBM BCD codes are most commonly used.

.34 Format Compatibility

Other device or system	Code translation
Other UNIVAC systems using Uniservo III C, IV C, or VI C tape units:.	no translation required.
IBM or "IBM-compatible" systems:. . .	program translated, with optional special translate feature.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.5 inch.
.352 Length:. . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . controller is part of first Uniservo (Model 857-00) attached to 1004 III Processor.

.42 Connection to System

.421 On-line: . . . . . 1 controller per 1004 III.
.422 Off-line:. . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1 or 2.
.432 Restrictions:. . . . . one tape drive is included with controller; one additional drive may be attached.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 961 characters.
.442 Input-output areas:. . . core storage.
.443 Input-output area access:. . . . . each character.
.444 Input-output area lockout: . . . . . none; but processor is interlocked during tape reading or writing.
.445 Table control: . . . . . none.
.446 Synchronization:. . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block:. . . . . 1 to 961 characters.
.512 Block demarcation —
Input:. . . . . interblock gap.
Output:. . . . . least-significant and most-significant addresses are wired on plugboard.

.52 Input-Output Operations

.521 Input:. . . . . read forward 1 block (with select or data ignore).
.522 Output:. . . . . write forward 1 block.
.523 Stepping:. . . . . backspace one block.
.524 Skipping:. . . . . none.
.525 Marking:. . . . . none.
.526 Searching:. . . . . none.

.53 Code Translation:. . . . matched codes or programmed translation.

.54 Format Control:. . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . at end of tape only.
Select format: . . . . . no.
Select code:. . . . . no.
Rewind: . . . . . yes.
Unload:. . . . . no.

.56 Testable Conditions

Disabled: . . . . . no.
Busy device: . . . . . no.
Output lock:. . . . . no.
Nearly exhausted:. . . . no.
Busy controller:. . . . . no.
End of medium marks: . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . performance varies with recording density, as indicated below.

.62 Speeds

.621 Nominal or peak speed —
200 char/inch:. . . . . 8,416 char/sec.
556 char/inch:. . . . . 23,396 char/sec.
800 char/inch:. . . . . 33,664 char/sec.
.622 Important parameters —
Tape speed:. . . . . 42.08 inches/sec.
Rewind speed: . . . . . 190 inches/sec.
Density: . . . . . 200, 556, or 800 char/inch.
Read start: . . . . . 9.5 msec.
Read stop:. . . . . 10.5 msec.
Write start:. . . . . 8.2 msec.
Write stop: . . . . . 9.0 msec.
Read start after backspace: . . . . . 12.0 msec.
Backspace start after read: . . . . . 12.0 msec.
Backspace start after write:. . . . . 7.2 msec.
Backspace stop:. . . . 10.5 msec.
Write check: . . . . . 7.0 msec.
Transport select:. . . 6.0 msec.

§ 091.

.62 Speeds (Contd.)

.623 Overhead —
Read: . . . . . 20.0 msec/block
Write: . . . . . 17.2 msec/block

.624 Effective speeds, in char/sec.

At 200 char/inch —
Reading: . . . . . 8,416N/(N + 168)
Writing: . . . . . 8,416N/(N + 145)

At 556 char/inch —
Reading: . . . . . 23,396N/(N + 468)
Writing: . . . . . 23,396N/(N + 402)

At 800 char/inch —
Reading: . . . . . 33,664N/(N + 673)
Writing: . . . . . 33,664N/(N + 579)

N = number of characters per block.
See also Graph 770:091.900.

.63 Demands on System: . . processor is interlocked except during stop or transport select times and during rewind operations.

.7 EXTERNAL FACILITIES

.73 Loading and Unloading

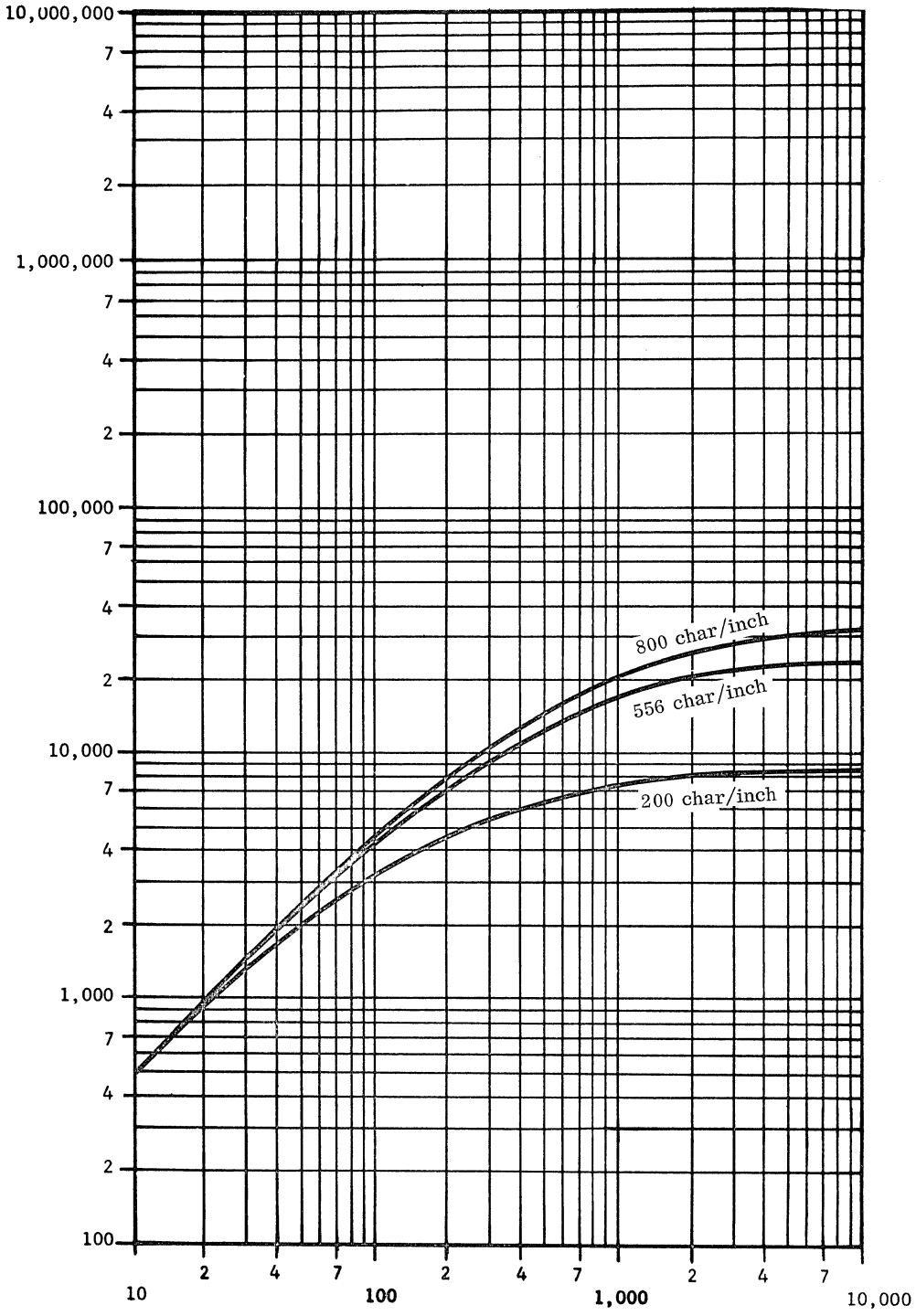
.731 Volumes handled: . . . . 2,400 feet per reel.
.732 Replenishment time: . . 0.5 to 1.0 minute; tape unit needs to be stopped.
.734 Optimum reloading period: . . . . . 11.4 minutes.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Recording:	read-after-write parity check	pulse to plugboard.
Reading:	row and track parity	pulse to plugboard.
Input area overflow:	check	pulse to plugboard.
Output block size:	not possible.	
Invalid code:	all codes are valid.	
Exhausted medium:	check	pulse to plugboard.
Imperfect medium:	read-after-write parity check	data not recorded on bad spot

§ 091.

EFFECTIVE SPEED: MODEL 857 UNISERVO



INPUT–OUTPUT: DATA LINE TERMINALS

§ 101.

.1 GENERAL

.11 Identity: . . . . . Data Line Terminals, Type 1 and Type 2.

.12 Description

Two types of Data Line Terminals are available for the UNIVAC 1004. Type 1 is suitable for transmission at instantaneous rates of 300 to 350 characters per second to another UNIVAC 1004, 490, or 1107.

The Type 2 Data Line Terminal is suitable for transmission at slightly lower instantaneous rates (250 to 300 characters per second) to or from another UNIVAC 1004 or a Digitronics Dial-O-Verter Magnetic Tape Terminal. The Dial-O-Verter translates and records the transmitted information on magnetic tape in UNIVAC or some other 6-bit code. The magnetic tape it creates is suitable for operation on almost any magnetic tape computer system, including IBM 1400 and 7000 series computers. This type of communication link can provide fast data transmission and conversion capabilities between UNIVAC 1004 systems and larger tape-oriented computer systems — typically, the computers at a headquarters operational center.

Using either type of Data Line Terminal, the practical rate is considerably less than the instantaneous transmission rate. Before each message is transmitted, it is necessary to confirm that the previous message was correctly received. To do this, two "turn-arounds" must be made between transmission and receiving. Except in the case of full-duplex private wire lines, each turn-around takes 150 milliseconds, so that a minimum of 300 milliseconds is required between successive messages. This reduces the effective transmission rate to about 125 cards per minute for a 1004 card processor. A tape processor may be able to obtain operational speeds approaching the instantaneous transmission speed, provided that messages of some 500 characters per tape block are pre-recorded on tape.

Bell System model 201A or 201B Data Sets, or their equivalents, are required at each transmitting and receiving location. Public telephone lines or private voice-grade communication facilities can be used. In an attended operation, connection is first established by the sending operator telephoning the receiving operator and ascertaining that the distant equipment is ready for operation. Both operators then switch their phones to data communication and lay the handsets aside. The receiving operator starts his 1004, which initiates the actual transmission of data.

The transmission follows a strict message format. The six data bits in each character are transmitted serially and are protected by an individual parity bit. A longitudinal parity check also protects the entire message. If any character is found to have wrong parity upon reception, transmission is interrupted.

.12 Description (Contd.)

At the end of the message, the receiving computer becomes the transmitting computer and advises whether or not the message was received correctly. If not, the message will be retransmitted automatically. A count of the number of retransmissions needed is kept, and if for any particular message this number exceeds a program-provided parameter, the system halts transmission and stalls. Display lights keep the operator informed about repeated transmissions.

If the message is apparently received correctly, but is not of the expected length, an indication of this condition is sent to the plugboard. The action to be taken is then under program control.

In the case of transmission to a UNIVAC 490 system, intervention by the 490 operator is not necessary if the 490 system is operating in the "unattended state." In this state, the presence or absence of a "burst tone," which the 1004 operator can hear on the phone connection, will indicate whether the transmission can be accepted by the 490 system. In all other ways, the operation is identical with the operator-controlled 1004-to-1004 transmission.

Operation with the Digitronics Dial-O-Verter follows the same general pattern, except that during transmission an eighth bit is transmitted with each character. This is a synchronizing bit, used to identify the character position on magnetic tape.

Table I summarizes the timing details for the various types of Data Line Terminal operation.

Programming techniques used for data transmission operations in UNIVAC 1004 systems are mainly related to two major possibilities for improved performance. One of these is to use the extensive editing capabilities of the computer to reduce the amount of data that needs to be transmitted. These editing facilities are described in the Central Processor section (770:051).

The second technique is to program the transmission to obtain the maximum amount of overlapping operation between messages. During this period, an interlock is necessary while checks are made to verify that the previous transmission was in order. This time can be used for reading cards, processing, or initiating punching operations, depending upon the program requirements.

Data transmission cannot be overlapped with processing, magnetic tape operations, card reading, or printing. It can be overlapped with card punching or paper tape punching.

§ 101.

.12 Description (Contd.)

TABLE I: CHARACTERISTICS OF DATA COMMUNICATION SYSTEMS INVOLVING THE UNIVAC 1004

Data Line Terminal Type	Data Set Model	Normal Direct Connections	Normal Indirect Connections	Transmission Rate (char/sec)	Inter-Message Time (msec)	Message Protection
1	Bell 201A, over dialed exchange lines	UNIVAC 1004 UNIVAC 490 UNIVAC 1107	None	286	332	Character and Message Parity
1	Bell 201B, over private half-duplex lines	UNIVAC 1004 UNIVAC 490 UNIVAC 1107	None	295	330	Character and Message Parity
2	Bell 201A	UNIVAC 1004 Dial-O-Verter	to most computer systems via magnetic tape	250	340	Character and Message Parity
2	Bell 201B, over private 2-wire lines	UNIVAC 1004 Dial-O-Verter	to most computer systems via magnetic tape	300	330	Character and Message Parity
2	Bell 201B, over private 4-wire lines	UNIVAC 1004	to most computer systems via magnetic tape	300	40	Character and Message Parity

SIMULTANEOUS OPERATIONS

§ 111.

Processing in the UNIVAC 1004 can be fully overlapped by card punch, paper tape punch, or card read/punch operations. The processor is interlocked during all other input-output operations, with the exception of printer spacing and magnetic tape stop and rewind times. Punching can occur simultaneously with any other input-output functions. Reading of cards or paper tape can be overlapped with printing. The following rules and the chart on the next page describe the UNIVAC 1004's capabilities for simultaneous operations.

RULES

- When processing, magnetic tape input-output, or data transmission is in process, only the card read/punch or the paper tape punch can proceed.
- When processing, magnetic tape input or output, or data transmission is not in process, a card or paper tape reader, the printer, and a card or paper tape punch can proceed.
- Processing, magnetic tape input-output, and data transmission are all mutually exclusive.
- Paper spacing on the printer and rewinding of the magnetic tape units can proceed, once initiated, without regard to other activities of the system.

§ 111.

SIMULTANEOUS OPERATIONS WITH THE 1004 PROCESSOR

Operation	Cycle Time, msec	Start Time		Data Transmission		Stop Time	
		Time, msec	Processor Interlocked	Time, msec	Processor Interlocked	Time, msec	Processor Interlocked
Card Reader, 365/400 cpm	165	0	-	165	yes	0	-
Card Reader, 615 cpm	93	0	-	93	yes	0	-
Auxiliary Card Reader, 400 cpm	165	0	-	165	yes	0	-
Card Punch 200 cpm	300	40	no	240	no	20	no
Card Read/Punch, 200 cpm	300	40	no	240	no	20	no
Paper Tape Reader, 400 cps	2.5	10	yes	variable	yes	?	no
Paper Tape Punch, 110 cps	9.1	40	no	variable	no	?	no
Printer, 400 lpm	170 + 8LS	0	-	150	yes	20 + 8LS	no
Printer, 600 lpm	100 + 8LS	0	-	80	yes	20 + 8LS	no
Magnetic Tape — read	-	9.5	yes	variable	yes	10.5	no
Magnetic Tape — write (8, 23, or 34 KC)	-	8.2	yes	variable	yes	9.0	no
Data Line Terminal	3.3	0	-	variable	yes	0	-

LS = number of lines skipped between successive printed lines.

INSTRUCTION LIST

§ 121.

There are three basic groups of machine operations for the UNIVAC 1004. Certain allowable combinations of these operations can be executed in a single program step. The chart below (Figure 1) shows the possible combinations. To use the chart, find the principal operation to be performed in the step in the Principal Operations column. Reading across the page, any auxiliary operation marked with an X may be combined with the principal operation in any one program step.

Each of the UNIVAC 1004 operations mentioned in Figure 1 is explained in detail on the next page. Subsequent paragraphs describe some of the possible modifications, testable conditions, etc. Figure 2 is a diagram of the complete plugboard, or "connection panel."

FIGURE 1: ALLOWABLE COMBINATIONS OF UNIVAC 1004 MACHINE OPERATIONS

PRINCIPAL OPERATIONS	AUXILIARY OPERATION																			
	GROUP I ARITHMETIC						GROUP II LOGICAL								GROUP III INPUT-OUTPUT†					
	ADD ALG	ADD ABS	SUBT ALG	SUBT ABS	SIGN COMP	COMP	TRF	ZD	ZDS (Ascending only)	DØB (Descending only)	Ø-Δ	Ø-*	IN	SI	SP (1-2)	SK (1-4)	PR	RD	EX	PU (H-C)
ADD. ALG.					X										X	X	X	X	X	X
ADD. ABS.					X										X	X	X	X	X	X
SUBT. ALG.					X										X	X	X	X	X	X
SUBT. ABS.					X										X	X	X	X	X	X
SIGN COMP.	X1	X1	X1	X1											X	X	X	X	X	X
COMP.															X	X	X	X	X	X
TRF.								X2	X2	X	X3	X3	X4	X4	X	X	X	X	X	X
ZD							X			X	X3	X3	X4	X4	X	X	X	X	X	X
ZDS							X				X3	X3	X4	X4	X	X	X	X	X	X
DØB							X	X			X3	X3	X4	X4	X	X	X	X	X	X
Ø-Δ							X	X2	X2	X			X4	X4	X	X	X	X	X	X
Ø-*							X	X2	X2	X			X4	X4	X	X	X	X	X	X
IN							X	X2	X2	X	X3	X3			X	X	X	X	X	X
SI							X	X2	X2	X	X3	X3			X	X	X	X	X	X
SP (1-2)	X1	X1	X1	X1	X5	X5	X	X2	X2	X	X3	X3	X4	X4		X	X	X	X	X
SK (1-4)	X1	X1	X1	X1	X5	X5	X	X2	X2	X	X3	X3	X4	X4	X		X	X	X	X
PR	X1	X1	X1	X1	X5	X5	X	X2	X2	X	X3	X3	X4	X4	X	X		X	X	X
RD	X1	X1	X1	X1	X5	X5	X	X2	X2	X	X3	X3	X4	X4	X	X	X		X	X
EX	X1	X1	X1	X1	X5	X5	X	X2	X2	X	X3	X3	X4	X4	X	X	X	X		X
PU (H-C)	X1	X1	X1	X1	X5	X5	X	X2	X2	X	X3	X3	X4	X4	X	X	X	X	X	
NO PRO.															X	X	X	X	X	X

NOTES: A. Only one operation with a like sub-number (1 through 5) can be performed on any one step.
B. Group I and Group II operations can not be combined on the same step. Groups I and III, or Groups II and III are allowable combinations.

Reproduced from UNIVAC 1004 Card Processor, Publication UT 2543 REV. 1A, page 67.

† Other instructions are available for the various optional I/O devices.

§ 121.

UNIVAC 1004 OPERATIONS

Group I: Arithmetic

- Add Algebraic (ADD ALG) — adds the algebraic values of two signed operands.
- Add Absolute (ADD ABS) — adds the absolute values of two operands.
- Subtract Algebraic (SUBT ALG) — subtracts the algebraic values of two signed operands.
- Subtract Absolute (SUBT ABS) — subtracts the absolute values of two operands.
- Compare (COMP) — compares two operands in one of three manners:
  (1) Numeric — signs and magnitudes are considered, but zone bits are ignored; result is condition greater, less, or equal.
  (2) Sign Compare — performed on same step as Add or Subtract; sign is +, -, or zero.
  (3) Alphanumeric — bit-for-bit comparison; result is match or nonmatch.

Group II: Logical

- Transfer (TRF) — moves data from one core storage location to another.
- Zone-Delete (ZD) — transfers data, stripping off all zone bits and minus signs.
- Zone-Delete with Sign (ZDS) — same as ZD except sign is not removed (ascending transfers only).
- Delete Zero Balance (DØB) — transfers data except when zero-balance indicator is set. In that case, spaces are transferred to receiving field (descending transfers only).
- Zero-Suppress with Space Fill (Ø- Δ) — transfers data, replacing nonsignificant zeros with spaces.
- Zero-Suppress with Asterisk Fill (Ø-*) — transfers data, replacing nonsignificant zeros with asterisks.
- Insert (IN) — transfers data, inserting specified characters at specified locations.
- Superimpose (SI) — transfers data, superimposing bits or characters onto the contents of specified locations.

Group III: Input-Output

- Space 1-2 (SP) — advances paper form in printer one or two lines.
- Skip 1-4 (SK) — advances paper form in printer to one of seven codes in the carriage-control loop.

Group III: Input-Output (Contd.)

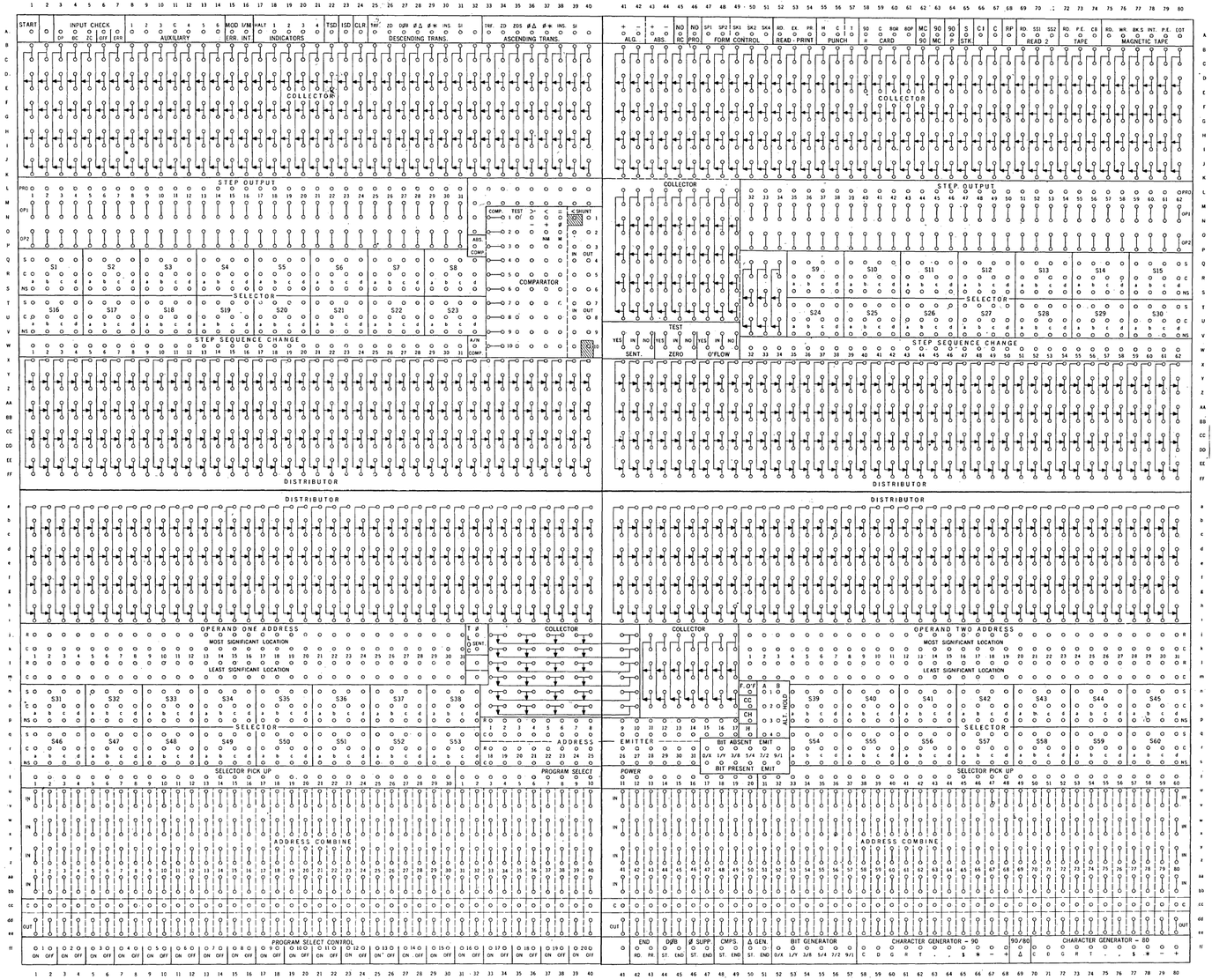
- Print (PR) — alerts printer to perform a Print operation when an Execute order is given.
- Read (RD) — alerts reader to perform a Read operation when an Execute order is given.
- Execute (EX) — causes reading and/or printing operations previously alerted to be performed.
- Punch Hold — punches without altering contents of the punch storage area.
- Punch Clear — punches and clears punch storage area to spaces.
- Punch Test — tests whether a punching operations is in process, and, if it is, delays step advance until punching is completed.
- No Process (NO PRO) — must be wired if an Arithmetic or Logical process is not included as part of a step.

MODIFICATIONS, TESTABLE CONDITIONS, ETC.

The following plugboard hubs can be used to provide the indicated additional processing capabilities.

- F. O'F. (form overflow) — emits during the time a line is being printed if, when the order to execute that line of print was given, the carriage-control loop was positioned so that the over-capacity punching was sensed.
- TEST Ø — indicates whether a zero is present in a location tested.
- TEST SENT — indicates whether a sentinel is present in a location tested.
- TEST O'FLOW — indicates whether an arithmetic overflow has occurred.
- CHARACTER GENERATORS — indicate characters to be inserted or superimposed.
- BIT GENERATORS — internally generate any specified character or special code.
- HALT — stops the processor.
- INDICATORS — four indicators which are associated with display lights on the console and indicate the reason for halting.
- T. LOC — tests a location for presence or absence of a zero or sentinel.
- NO RC — suspends automatic recomplementation of a complementary result obtained during an arithmetic step.
- ADDRESS EMITTERS — instruct the machine to insert characters, start or stop certain operations, determine control punching, etc.
- BIT PRESENT EMITTERS and BIT ABSENT EMITTERS — search a storage location to determine whether certain bits are absent or present (used in control punching in cards).

§ 121.



DATA CODE TABLE NO. 1

§ 141.

.1 Use of Codes: . . . . . internal code (XS-3 code), 80-column punched card code, and printer characters.

.2 Character Codes:

80-Col. Card Code	Printable Characters	XS-3 Code	80-Col. Card Code	Printable Characters	XS-3 Code
12-1	A	01 0100	7	7	00 1010
12-2	B	01 0101	8	8	00 1011
12-3	C	01 0110	9	9	00 1100
12-4	D	01 0111	12	&	01 0000
12-5	E	01 1000	11	- (minus)	00 0010
12-6	F	01 1001	12-0	?	01 0011
12-7	G	01 1010	11-0	! (exclam.)	10 0011
12-8	H	01 1011	0-1	/	11 0100
12-9	I	01 1100	2-8	+	11 0011
11-1	J	10 0100	3-8	#	01 1101
11-2	K	10 0101	4-8	@	10 1110
11-3	L	10 0110	5-8	: (colon)	01 0001
11-4	M	10 0111	6-8	>	11 1110
11-5	N	10 1000	7-8	' (apos.)	10 0000
11-6	O	10 1001	12-3-8	. (period)	01 0010
11-7	P	10 1010	12-4-8	⌑	11 1101
11-8	Q	10 1011	12-5-8	[	00 1111
11-9	R	10 1100	12-6-8	<	01 1110
0-2	S	11 0101	12-7-8	=	01 1111
0-3	T	11 0110	11-3-8	$	10 0010
0-4	U	11 0111	11-4-8	*	10 0001
0-5	V	11 1000	11-5-8	]	00 0001
0-6	W	11 1001	11-6-8	; (semi-col)	00 1110
0-7	X	11 1010	11-7-8	Δ	10 1111
0-8	Y	11 1011	0-2-8	≠	11 0000
0-9	Z	11 1100	0-3-8	, (comma)	11 0010
0	0	00 0011	0-4-8	%	11 0001
1	1	00 0100	0-5-8	(	10 1101
2	2	00 0101	0-6-8	\	00 1101
3	3	00 0110	0-7-8	)	11 1111
4	4	00 0111			
5	5	00 1000	Blank	Space N.P.	00 0000
6	6	00 1001			

Reproduced from UNIVAC 1004 Card Processor — 80 Column, Publication UT 2543 REV. 1A, page 4.

DATA CODE TABLE NO. 2

§ 142.

.1 Use of Codes: . . . . . internal and 90-column punched card code, and printer characters.

.2 Character Codes:

PRINTED CHARACTERS	90-COLUMN CARD CODE	PRINTED CHARACTERS	90-COLUMN CARD CODE
A	1-5-9	7	7
B	1-5	8	7-9
C	0-7	9	9
D	0-3-5	&	0-1-3-5-7
E	0-3	(- minus)	0-3-5-7
F	1-7-9	?	0-1-3
G	5-7	! (exclam.)	0-3-7-9
H	3-7	/	3-5-7-9
I	3-5	+	1-5-7-9
J	1-3-5	#	0-1-5-7
K	3-5-9	@	0-1-3-7
L	0-9	: (colon)	1-3-7-9
M	0-5	>	0-3-5-7-9
N	0-5-9	' (apos.)	0-1-5-7-9
O	1-3	. (period)	1-3-5-9
P	1-3-7	¤	0-1-3-9
Q	3-5-7	[	0-5-7-9
R	1-7	<	0-1-5-9
S	1-5-7	=	0-1-3-5-7-9
T	3-7-9	$	0-1-3-5-9
U	0-5-7	*	0-1
V	0-3-9	]	1-3-5-7
W	0-3-7	; (semi-colon)	1-3-5-7-9
X	0-7-9	Δ	0-1-7
Y	1-3-9	≠	0-1-7-9
Z	5-7-9	, (comma)	0-3-5-9
0	0	%	0-1-5
1	1	(	0-1-9
2	1-9	\	0-1-3-7-9
3	3	)	0-1-3-5
4	3-9		
5	5	SPACE N.P.	BLANK
6	5-9		

Reproduced from UNIVAC 1004 Card Processor — 90 Column, Publication UT 2541 REV. 1B, page 4.

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

UNIVAC has, in the past, made no commitments to provide software support for the 1004 beyond the basic multiply and divide subroutines. Many of the advanced software facilities that are now offered for most stored-program computers (assemblers, compilers, sorts, operating systems, etc.) are simply not applicable to plugboard-programmed computers like the 1004. Nevertheless, a number of specialized programs and subroutines developed by 1004 users and by UNIVAC branch offices are now available for distribution. These include a variety of listing methods, and some sophisticated programs such as the report generator described below. A report generator is a program which uses a description of a required report — showing the fields to be accumulated, the position of various subtotal and total lines, etc. — to automatically create the desired program. Such generators can be valuable time-savers where special reports are needed in a hurry.

.14 Report Writing

General Purpose Program

Reference: . . . . . Preliminary Specifications: UNIVAC 1004 General Purpose Program.
Date Available: . . . . . December, 1963.

Description:

The General Purpose Program is available for both 80-column and 90-column 1004 systems, Models C (62 steps) and A (31 steps). The program requires about 1,800 wires, and consists of two phases. The first phase loads core storage with headers and other control information and defines what is to be done with the various quantities in the input deck. The second phase consists of printing the desired report from the data cards. The 80-column version permits the punching of cards for totals. Three types of fields can be indicated on the data cards: accumulating fields (numbers to be totaled), list fields (data to be printed directly), and control fields (which indicate when totals are to be computed and printed). Restrictions are imposed upon the position, length, and number of these fields.

.14 Report Writing (Contd.)

Description (Contd.)

The report produced by the program contains a heading, body, and totals. Provisions are made for a one-line report title and for page headings. In the body of the report, the list fields must be to the left of the accumulating fields. Four editing options are allowed for accumulating fields: no insertions, no decimal point (insertion of commas and sign), one decimal place (insertion of commas, sign, and decimal point), and two decimal places.

The accumulating fields may be added to each other or "crossfooted", with the result being placed in another field, usually to the right. There may be several levels of totals, controlled by the Alternate Hold Switches. The total lines are marked with asterisks — the lowest level with one asterisk and an additional one for each higher level. These totals may be either spaced an extra space below the body of the report or printed at the bottom of the page. In either case, the paper can be advanced to the next page if desired.

By use of other Alternate Hold Switches, it is possible either to suppress all accumulating fields or to print only total lines. In the 80-column version of the program, certain fields can be deleted under card control.

.15 Data Transcription: . . no specific routines.

.16 File Maintenance: . . . no specific routines.

.17 Other

A number of standard commercial routines are available, including methods for floating dollar sign, check-digit verification, elimination of report lines when only a single total is involved, sequence checking of alphanumeric keys on 80-column card machines, packing of numerical data so that three digits can be stored in two character positions, etc.

Since-cosine and square root routines have been released, and a Critical Path Method routine has been announced.

SYSTEM PERFORMANCE

§ 201.

GENERALIZED FILE PROCESSING (770:201.100)

These problems involve updating a master file from information in a detail file and producing a printed record of each transaction. This application is one of the most common commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide. Standard File Problems A, B, and C differ in that three different record sizes are used in the master file. In Standard File Problem D, the amount of computation performed upon each transaction is increased by a factor of three. Performance upon each problem is estimated for activity factors (ratios of number of detail records to number of master records) ranging from zero to unity. In all cases a uniform distribution of activity is assumed.

Because the UNIVAC 1004 is programmed by means of plugboard wiring, the sequence and grouping of instructions in the Users' Guide were modified to conform with wired program "steps." One notable change is that the control column test is made as the card is being read into core storage, and is used to set a switch which is executed later in the program.

Because of the lack of a floating-dollar editing capability and the limitations of plugboard wiring, the floating dollar sign requirement for the report file was waived, and check-protect editing was used instead. It was also assumed that items in the detail file were zero-filled if used in computations. The five-millisecond delay for selectors was found not to be important.

In Configurations I and I-A, the master and detail input files are on the card reader. The output files are on the card punch (updated master file) and printer (report file). For Problems A and C in Configuration I, the 200-cpm card punch is the controlling factor on overall processing time. For Problems B and D, the Central Processor time (which includes the time the processor is interlocked during card reader operations) is controlling. For Configuration I-A, the punch is the controlling factor for all Problems A, B, C, and D. (Note: It is assumed that an off-line collator will be used to remove all inactive records from the master card file before processing, so only the processing times at an activity factor of 1.0 are shown for Configurations I and I-A.)

In Configuration II, the master files are on magnetic tape, blocked three records per block because of the limited capacity of the 1004's core storage. The detail file is assigned to the card reader and the report file to the printer. In Problems A, B, and C, the master file tapes and the printer (which overlaps the card reader) are the controlling factor at all activities from zero to unity. For Problem D, the Central Processor is controlling at activities from 0.1 to 1.0, while the tapes and printer are controlling at activities below 0.1.

The UNIVAC 1004 was deemed unsuitable for execution of our other standard measures of system performance: Sorting, Matrix Inversion, and Mathematical Processing.

§ 201. SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 1 (STANDARD FILE PROBLEM A)

	ITEM		CONFIGURATION I	CONFIGURATION I-A	CONFIGURATION III	REFERENCE
1 Input-Output Times	Char/block	(File 1)	80	80	324	4:200.112
	Records/block	K (File 1)	0.5	0.5	3	
	msec/block	File 1 / File 2	165/300	93/300	29.7/26.9	
		File 3	165	93	93	
		File 4	210	140	140	
	msec/switch	File 1 / File 2	0	0	0	
		File 3	0	0	0	
		File 4	0	0	0	
	msec penalty	File 1 / File 2	165/0.6	93/0.5	19.2/17.9	
		File 3	165	93	93	
		File 4	150	80	80	
2 Central Processor Times	msec/block	a_1	5.1	4.1	4.1	4:200.1132
	msec/record	a_2	1.0	0.8	0.8	
	msec/detail	b_6	1.4	1.1	1.1	
	msec/work	$b_5 + b_9$	30.8	25.0	25.0	
	msec/report	$b_7 + b_8$	2.4	2.0	2.0	
3 Standard File Problem A F = 1.0	nsec/block for C.P. and dominant column.		C.P. / Punch	C.P. / Punch	C.P. / I/O	4:200.114
		a_1	5.1 /	4.1 /	4.1 /	
		a_2 K	0.5 /	0.4 /	2.4 /	
		a_3 K	17.3 /	14.1 /	84.3 /	
		File 1 Master In	165.0 /	93.0 /	19.2 / 29.7	
		File 2 Master Out	0.0 / 300.0	0.0 / 300.0	17.9 / 26.9	
		File 3 Details	82.5 /	46.5 /	279.0 / **	
		File 4 Reports	** /	** /	** / 420.0	
		Total	270.4 / 300.0	158.1 / 300.0	406.9 / 476.6	
4 Standard File Problem A Space	Unit of measure	(characters)				4:200.1151
		Std. routines	*	*	*	
		Fixed	-	-	-	
		3 (Blocks 1 to 23)	*	*	*	
		6 (Blocks 24 to 48)	*	*	*	
		Files	520	520	848	
		Working	100	100	100	
		Total	620	620	948	

* Instructions are wired into a plugboard, so no core storage space is required.
** The cycles for the card reader and printer are overlapped; thus only the longer time is used.

SYSTEM PERFORMANCE

§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

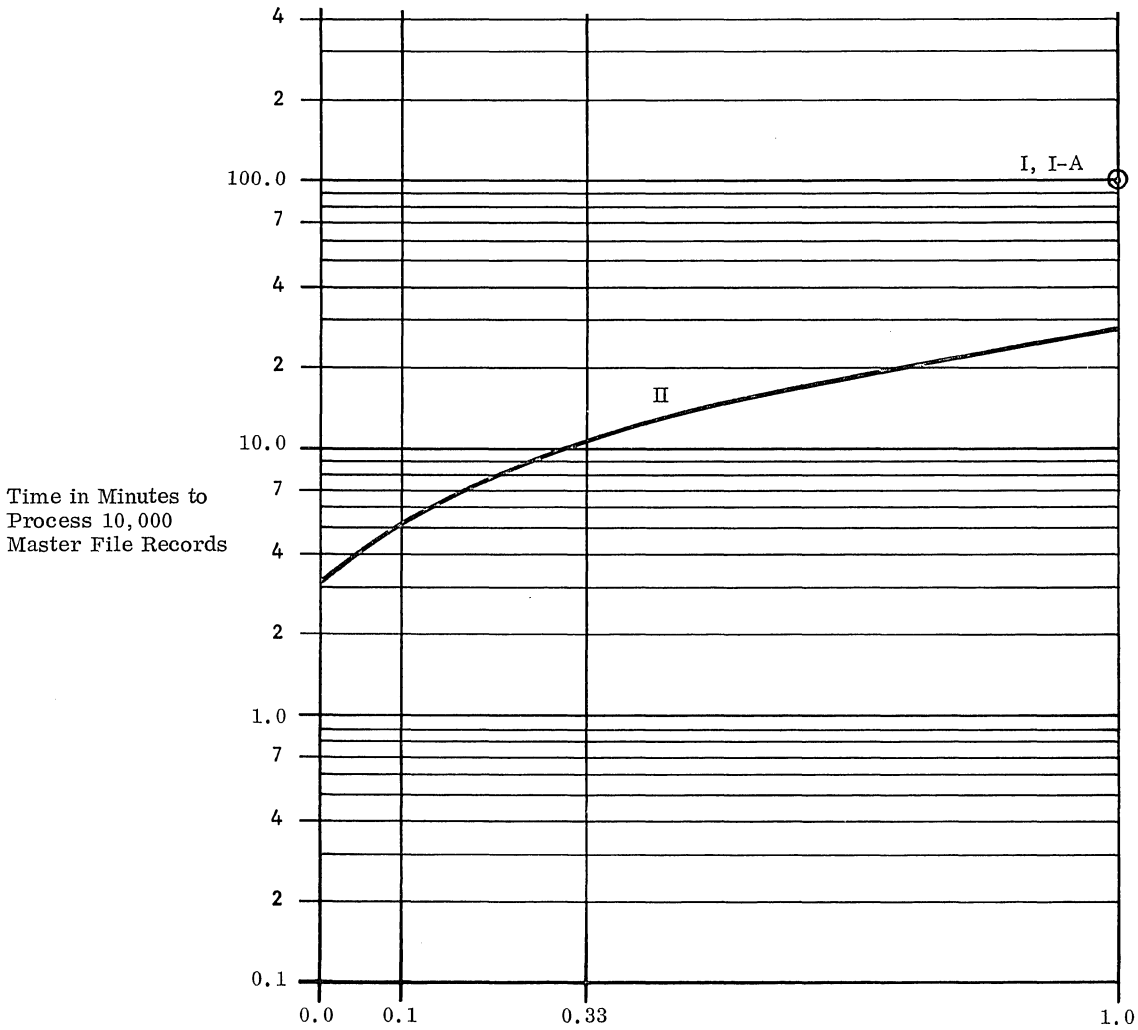
.112 Computation: . . . . . standard, with modifications as described on Page 770:201.001.

.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . . see graph below.

.115 Storage space required
Configuration I: . . . . 620 characters.*
Configuration I-A: . . 620 characters.*
Configuration II: . . . . 948 characters.*

*Program steps are wired into a plugboard, so no core storage space is required.



(Roman numerals denote standard System Configurations.)

§ 201.

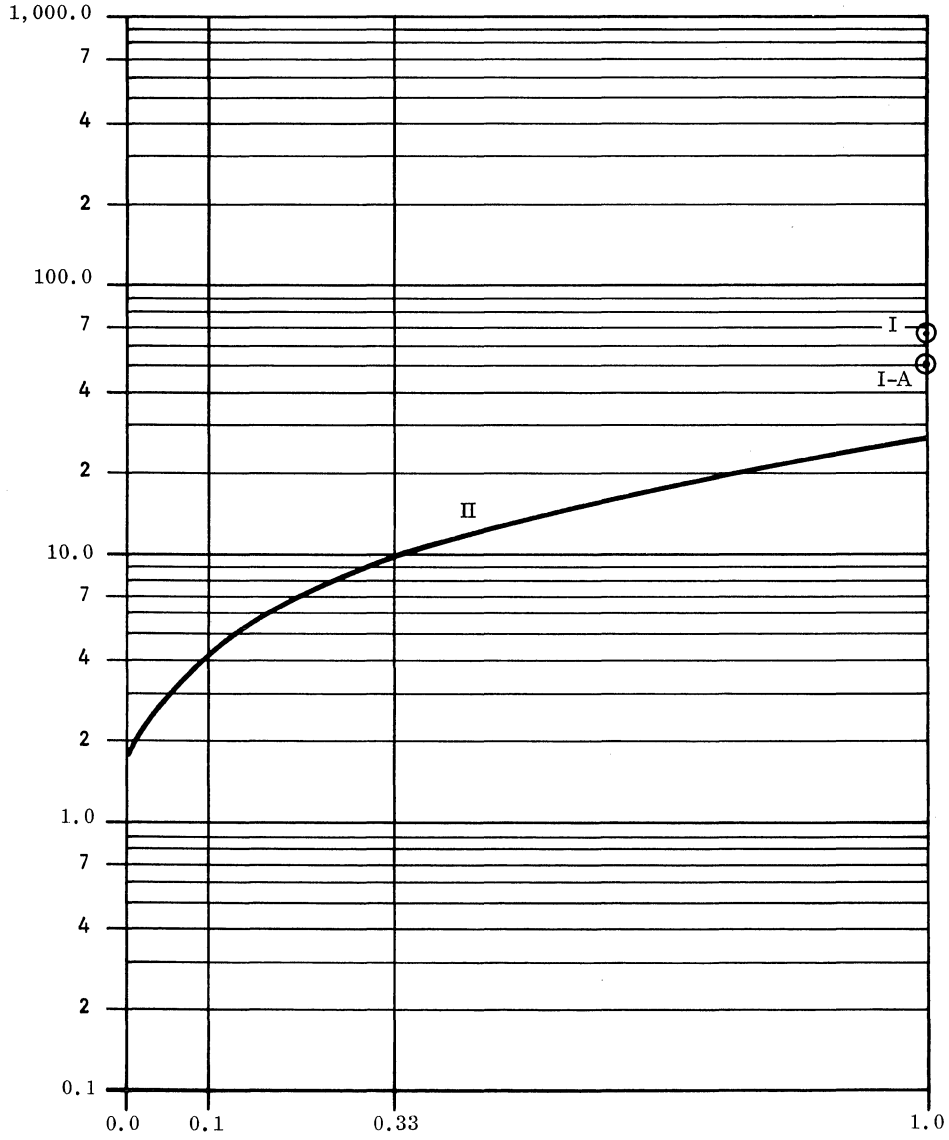
.12 Standard File Problem B

.121 Record sizes
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard, with modifications as described on Page 770:201.001.

.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.

.124 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

§ 201.

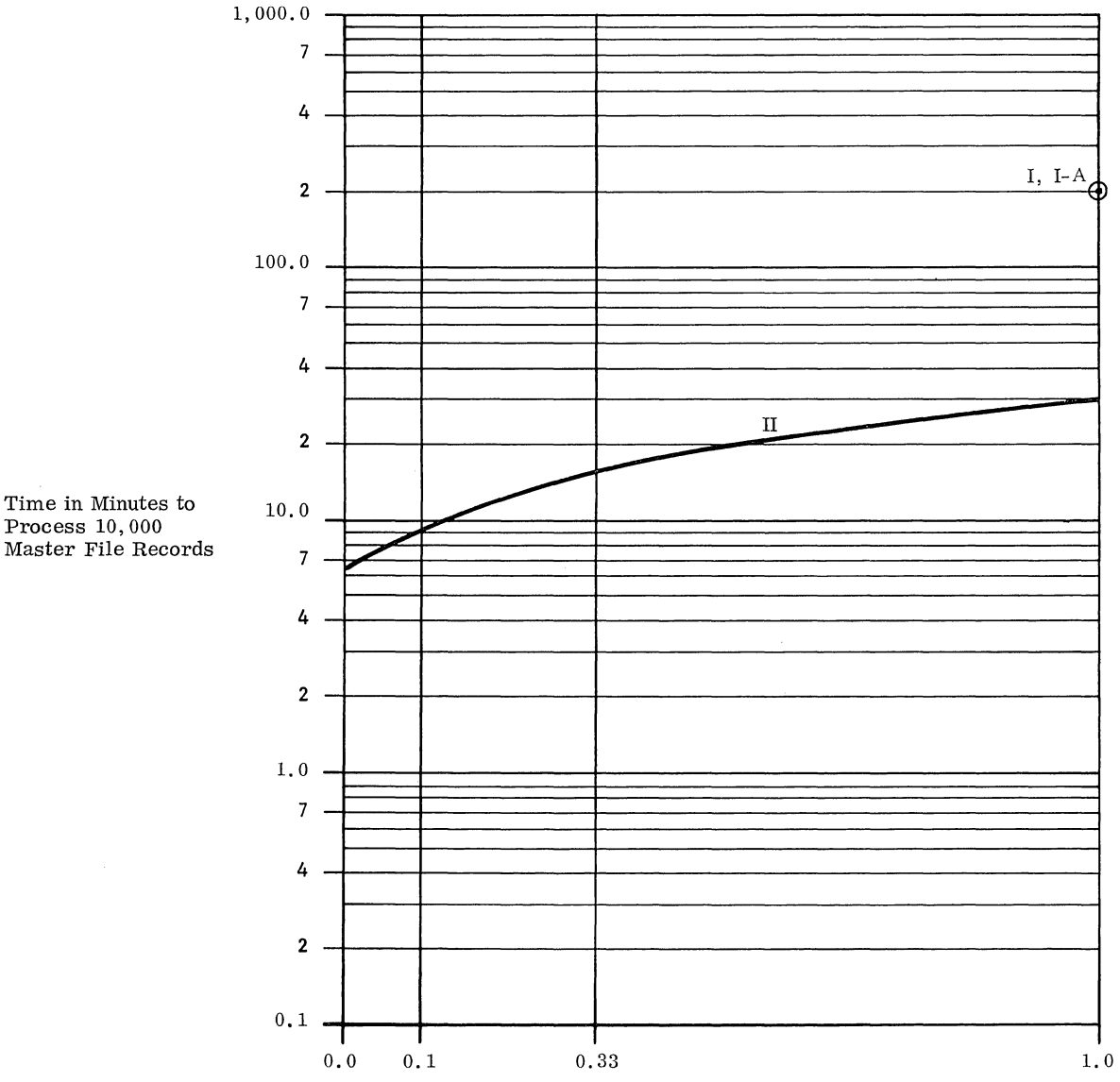
.13 Standard File Problem C

.131 Record sizes
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard, with modifications as described on Page 770:201.001.

.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.

.134 Graph: . . . . . see graph below.



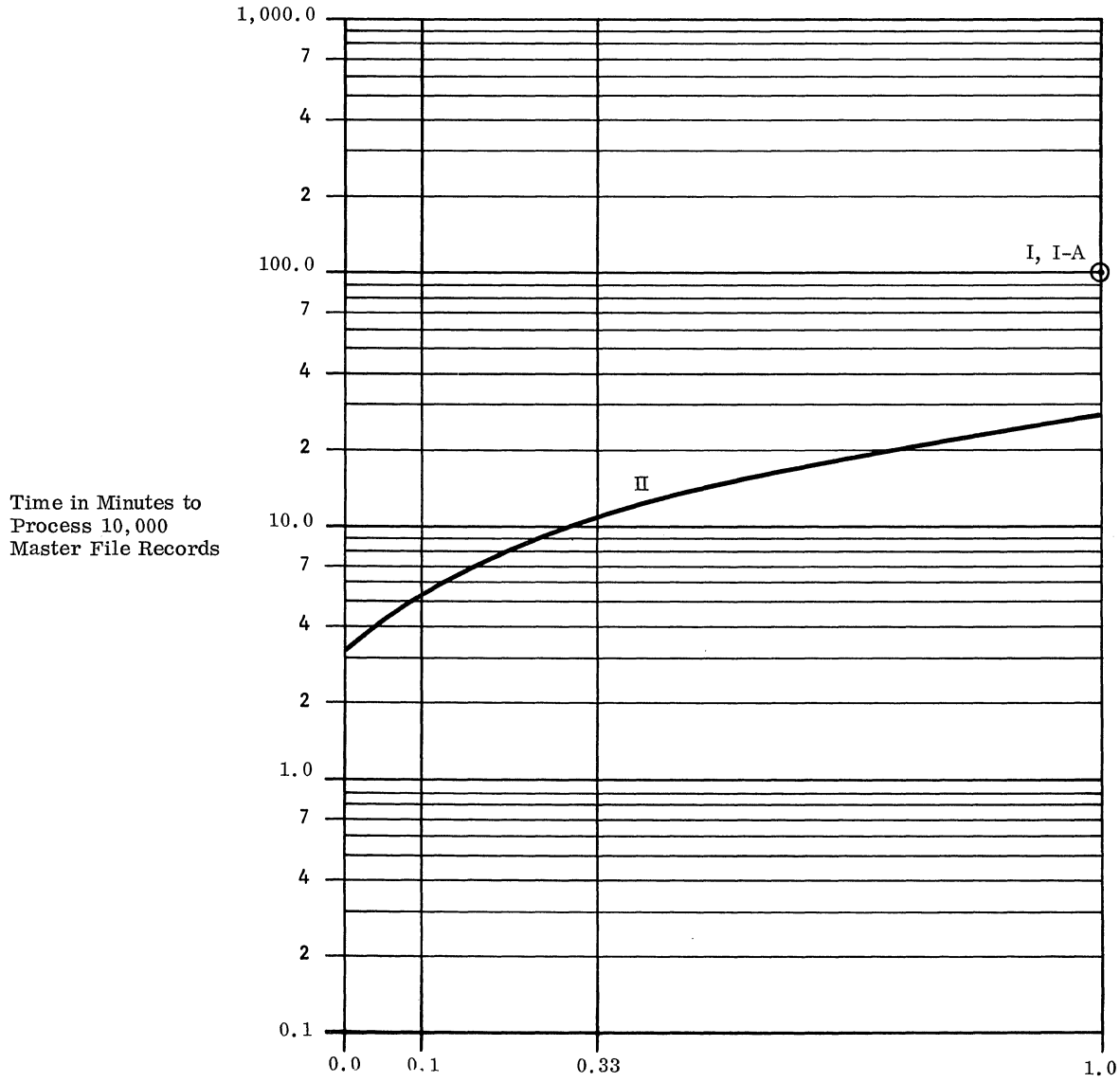
(Roman numerals denote standard System Configurations.)

§ 201.

.14 Standard File Problem D

.141 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

PHYSICAL CHARACTERISTICS

§ 211.

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power KVA	BTU per hr.
1004 I Processor*	71	63	55	2,021	3.0	8,500
1004 II Processor*	71	63	55	2,021	3.0	8,500
1004 III Processor*	71	63	55	2,021	3.0	8,500
Auxiliary Card Reader	31	24	42	415	0.3	683
Card Punch	42	25	49	870	1.5	3,500
Card Read/Punch	42	25	49	870	1.5	3,500
Paper Tape Reader†	-	-	-	-	-	-
Paper Tape Punch†	-	-	-	-	-	-
Uniservo, Model 857-00	27	32	72.5	470	1.0	4,700
Uniservo, Model 857-02	52	32	72.5	920	1.4	5,220
Data Line Terminal, Type 1†	-	-	-	-	-	-
Data Line Terminal, Type 2†	-	-	-	-	-	-

General Requirements

Operating temperature: . . . . . 50 to 90 °F.
Relative humidity: . . . . . 20 to 85%.
Power: . . . . . 208-230 volt, 60-cycle, 1-phase, 3-wire AC.

* Standard card reader and printer are housed in Processor cabinet and included in these figures.

† These units are mounted inside or outside the Processor, and are included in the measurements of the Processor.

PRICE DATA

§ 221. PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR		Card Processor (includes 300 cpm Reader and 300 lpm Printer)– 8 μsec cycle time			
	1004 I-01	Model A - 90-column	1,150	205.00	46,000
	1004 I-02	Model A - 80-column	1,150	205.00	46,000
	1004 I-03	Model B - 90-column	1,400	225.00	56,000
	1004 I-04	Model B - 80-column	1,400	225.00	56,000
	1004 I-05	Model C - 90-column	1,500	235.00	60,000
	1004 I-06	Model C - 80-column	1,500	235.00	60,000
	1004 I-07	80/90 column	1,650	250.00	66,000
		Card Processor (includes 615 cpm Reader and 600 lpm Printer)– 6.5 μsec cycle time			
	1004 II-01	Model A - 90-column	1,275	270.83	51,000
	1004 II-02	Model A - 80-column	1,275	270.83	51,000
	1004 II-03	Model B - 90-column	1,525	290.83	61,000
	1004 II-04	Model B - 80-column	1,525	290.83	61,000
	1004 II-05	Model C - 90-column	1,625	300.83	65,000
	1004 II-06	Model C - 80-column	1,625	300.83	65,000
	1004 II-07	80/90 column	1,775	315.83	71,000
		Magnetic Tape Processor (includes 615 cpm Reader and 600 lpm Printer) - 6.5 μsec cycle time			
	1004 III-01	Model A - 90-column	1,275	270.83	51,000
	1004 III-02	Model A - 80-column	1,275	270.83	51,000
	1004 III-03	Model B - 90-column	1,525	290.83	61,000
	1004 III-04	Model B - 80-column	1,525	290.83	61,000
	1004 III-05	Model C - 90-column	1,625	300.83	65,000
	1004 III-06	Model C - 80-column	1,625	300.83	65,000
	1004 III-07	80/90 column	1,775	315.83	71,000
		Optional Features			
	F0586-00	Short Card Feeding — 51-column cards in 80-column code; 29-column cards in 90-column code	40	10.00	1,000
	F0621-00	Short Card Feeding — 66-column cards in 80-column code	40	10.00	1,000
	F0587-00	Code Image Read - 80-column processor only	25	5.00	1,000
	F0588-00	Code Image Punch - 80-column processor only	25	3.00	1,000

§ 221. **PRICE DATA (Contd.)**

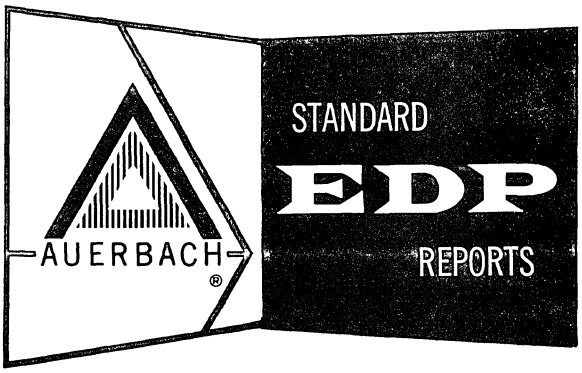
CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR (Contd.)		Optional Features			
	F0590-00	Code Conversion	1,000	10.00	4,000
	F0594-00	Card Processor Expansion Kit (Model A to Model B)	250	20.00	10,000
	F0595-00	Card Processor Expansion Kit (Model B to Model C)	100	10.00	4,000
	F0601-00	80/90 Read - 80-column processor	150	15.00	6,000
	F0602-00	80/90 Read - 90-column processor	150	15.00	6,000
	F0599-00	Processor Form Stacker	—	—	90
	?	Special Print Code Wheel	—	—	395
INPUT-OUTPUT		Punched Card Equipment			
	2009-00	Card Punch - 80-column - 200 cpm	300	90.00	12,000
	2011-00	Card Punch - 90-column - 200 cpm	300	90.00	12,000
	2009-01	Card Read/Punch - 90-column - 200 cpm	450	140.00	18,000
	2011-01	Card Read/Punch - 90-column - 200 cpm	450	140.00	18,000
	0704-00	Auxiliary Card Reader - 400 cpm	180	37.08	7,200
		Optional Features			
	F0619-00	Scored Card - 80-column Punch	15	6.17	600
	F0619-01	Scored Card - 90-column Punch	15	6.17	600
	F0591-00	Double Punch - Blank Column Detection Device	15	—	600
	F0592-00	Selective Stacker	5	—	200
	F0620-00	Card Punch Read - 80-column	150	50.00	6,000
	F0620-01	Card Punch Read - 90-column	150	50.00	6,000
	F0619-02	Scored Card - 80-column Read/ Punch	15	6.17	600
	F0619-03	Scored Card - 90-column Read/ Punch	15	6.17	600
		Paper Tape Equipment			
	0902-00	Paper Tape Reader - 400 cps	150	15.00	6,000
	F0606-00	Paper Tape Punch - 110 cps	250	33.33	10,000
		Magnetic Tape (on 1004 III only)			
	0857-00	First Uniservo and Control	500	124.58	20,000
	0857-02	Second Uniservo	300	75.42	12,000
		Communications Equipment			
	F0585-00	Data Line Terminal, Type 1	200	20.00	8,000
	F0611-00	Data Line Terminal, Type 2	200	20.00	8,000

UNIVAC SS 80/90

MODEL I

Univac

(A Division of Sperry Rand Corporation)



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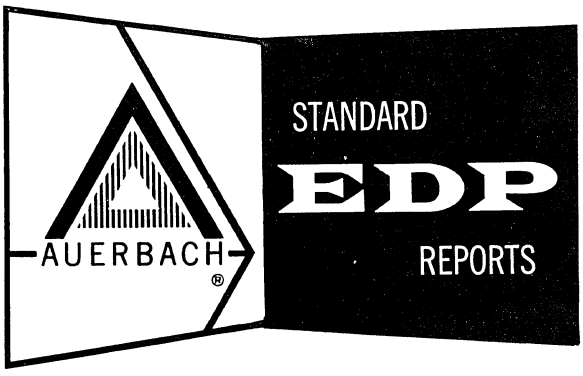
UNIVAC SS 80/90

MODEL I

Univac

(A Division of Sperry Rand Corporation)



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INTRODUCTION

§ 011.

The UNIVAC Solid-State Model I was originally introduced in 1958 as a punched card processing computer. The two main features of the Model I were its solid-state design, which reduced installation and maintenance costs, and its fully buffered card reader, punch, and line printer. The storage drum and the actual computation times were not in themselves major attractions, but in combination with each other, they were well able to keep up with the input-output.

In the 5 years since the original introduction of the Model I, a number of changes have been made. The three major changes are the introduction of:

- Magnetic tapes.
- Variable storage capacity drums.
- The Solid-State Model II with core and drum storage.

The Model II, which has very different performance characteristics, is presented in a separate report (See Computer System Report 772:). Introduction of the two other features, namely the tape units and the variable storage capacities of the drums, increased the applications range of the Solid-State 80/90 systems. The tapes allow large files to be used; however, their slow speed (effectively 16,400 characters per second) and the fact that only one tape can operate at any time place a limit on the over-all throughput of the system.

The introduction of the variable storage capacity drum also increased the number of situations in which the Solid-State 80/90 could be used, mainly by allowing a considerable reduction in price. This reduction came after the introduction of the IBM 1401, which showed how much work could be done with a small internal storage capacity.

The Model I has been one of the more popular computer systems marketed so far. While the number of systems sold does not compare with the number of IBM 1401 systems sold (more than 5,000), there are more than 500 Solid-State Model I systems presently in use. Some of these systems are now available as used systems at purchase prices which can be negotiated. Such systems could be good buys, as the problem of maintenance for obsolescent solid-state computers is much simpler than for the obsolescent vacuum-tube computers.

The Model I processor handles data in words of 10 digits plus a sign bit. Each digit has an odd parity bit associated with it. Parity is checked during all data movements to or from storage. The central computer uses only numeric data, whereas the peripheral units use alphameric card data. This difference is resolved by splitting each alphameric word (10 characters) into 2 words, 1 zone and 1 numeric. The computer has three 1-word arithmetic registers A, X, and L. Register A is the accumulator and forms one half of a double length register, (combined AX), which is used for shifts and multiplication instructions.

Programming for the SS 80/90 Model is similar to programming for the IBM 650. As in most drum storage computers, latency problems emphasize the importance of program complexity. The instruction form is 1 + 1, (known as one and one half address). This instruction form uses the second address to state the location from which the next instruction is to be taken. There are 62 instructions including arithmetic (fixed point only), logical masking instruction, comparison instructions, a right-shift and a left-shift instruction, a zero-suppress instruction, and automatic translation instructions. These all operate on full words. Character manipulation is performed by a combination of shifts and logical AND and OR instructions.

INTRODUCTION (Contd.)

§ 011.

The Model I has three index registers, which can be used to modify the first address in an instruction. Normally this address is the operand, but it can be a transfer-of-control address. The second (or Next-instruction) address cannot be modified by index registers.

Data is held on the drum in 200-word "bands". There are two types of bands, with either one or four read/write heads. The access time to a particular operand is either from 0 to 3.4 milliseconds or 0 to 0.875 milliseconds respectively for either one or four heads. These are much longer times than the actual instruction times themselves. (Addition only takes 0.085 millisecond.)

The primary differences between the Solid-State 80 and the Solid-State 90 processors are the code translation instructions and the buffer storage pattern arrangements. Each is peculiar to the kind of card handled, 80- or 90-column. The buffer patterns on the drum optimize input-output transfers to peripheral units. This optimizing involves the "interlaced" positioning of input-output data in order to achieve greater efficiency.

UNIVAC Solid-State systems are buffered so that virtually all of the peripheral units can operate simultaneously with computing. The exception is the input-output channels which are used with the synchronizers. These synchronizers can control up to 10 magnetic tape units and 10 RANDEX drum units. Only one unit connected to a synchronizer can be read or written upon at a time. The Model I can have only one synchronizer, while the Model II can have a second synchronizer which permits an additional 10 magnetic tape units to be connected to the system. In Model I systems, only simultaneous read/compute or write/compute are possible. In Model II systems, read, write, and compute operations can be handled simultaneously through the use of a second synchronizer.

Input/output buffer areas are held on the drum, and when the data are transferred from the buffer bands to the actual drum, "interlaces" are used in the main storage. In the main storage, an 80-column card image is split into 16 words, 8 of which represent the zone punches, and 8 of which represent the balance of the card. These 16 words are entered on the drum in scattered locations on the same band which are called the "card interlace". Similar interlaces exist for all input/output units in different positions.

The input-output units connected to any one system in addition to the synchronizers can include the following:

- 600 card per minute Card Reader.
- 150 card per minute Card Read-Punch.
- 600 line per minute Printer.
- 500 character per second Punched Tape Reader and/or 100 characters per second Punch.

The card reader operates at 600 cards per minute and each card is read at two separate read stations. These readings are not compared in the reader itself, but both images are read into storage and are compared there for accuracy. Optionally the reader can be equipped with three stackers instead of one; and with an automatic program interrupt system; otherwise, the program has to make constant checks during card reads as to the current status of the reader.

The Read-Punch unit operates at 150 cards per minute and can use only a single file of cards for reading and punching. The unit has two read stations, one which reads before and one which reads after punching. No accuracy checking of punching occurs in the unit itself; all checking is handled by the stored program. The punch is able to handle all standard Hollerith or 90-column code punching but cannot handle all possible binary punching operations. Optionally, this unit can include two read stations and two output stackers. Without this option, no check is made on the accuracy of the output cards.

INTRODUCTION (Contd.)

§011.

The High Speed Printer is a 600 line per minute printer with basically the same printing mechanism as has been used in UNIVAC printers since 1952. A constantly revolving drum holds 51 print characters, and the firing of the print hammers occurs at a fixed time. The printed line can be 100, 110, 120, or 130 characters long. No paper loop controls the format; all controls are effected internally. Echo checks are performed to text the accuracy of the printing, and the printer is "disabled" if the checks fail.

The Central Processor, the drum, the card reader, the read punch and the printer make up the basic system. Additional units which can be included are the magnetic tape system, the RANDEX System, the Paper Tape System, and the Card-Punching Printer. The magnetic tape system can either read or write while computing, but cannot do both. The fixed block length (normally 1,100 characters) provides an effective speed of 16,400 characters per second. Up to 10 tape decks can be connected, via a synchronizer.

The Tape Synchronizer can also control up to 10 RANDEX Units. Each unit consists of two large drums mounted one above the other, with a single read/write head assembly which moves on a boom between the drums. The drums revolve once each 70 milliseconds and carry some 24 million characters. Records made up of forty-eight 10-digit words can be accessed within 600 milliseconds, irrespective of their position on the drums.

A Paper Tape system can also be included with UNIVAC Solid-State systems. The card-punching printer is used primarily in utility billing, in which a card must have the accounting details punched into it and the address printed on both sides, all at the same time.

Development of software for the Model I has had a number of false starts. The Model I was originally advertised as being designed for programming in FLOW-MATIC Source language (the precursor of COBOL); however, the plans for this never materialized. A COBOL-60 compiler was also announced for the system, but now has been withdrawn. No FORTRAN-type of compiler has been announced, but one is rumored to be currently under field test.

The software situation has a positive side, however, which is encouraging. Two assembly systems are being used in the United States, and a number of specialized programs have been developed by UNIVAC branches and by users. These programs include versions of the BELL Interpretive system and a numerical control system for machine tool control.

The software provided for the systems includes service routines, mathematical functions and routines, linear programs, and two assembly programs (X-6 and the more recent S-4). X-6 is an elementary drum-type assembly program for Model I processors and S-4 is a more advanced system for both processors. Problems coded in X-6 can, with minor revisions, be assembled using S-4. At present, no process oriented languages have been implemented for these systems.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or use
Digit:	4 bits	Decimal digit, algebraic sign.
Word:	41 bits	Instruction or 10 digits and sign.
2 Words:	20 digits	10 characters.
Band:	200 words	Magnetic drum.
Block:	48 words	RANDEX Store.
Track:	12 blocks	RANDEX Store.
Sector:	20 tracks	RANDEX Store.
Drum Half:	100 sectors	RANDEX Store.
Units:	4 drum halves	RANDEX Store.

.2 DATA FORMATS

Type of Information	Representation
Numeral:	1 digit.
Alphabetic:	2 digits.
Instruction:	1 word.
Number:	10 digits + sign.
Interlace:	Refers to input-output area of each peripheral unit. It consists of a number of words on a single 200-word band of the drum, the arrangement and number being fixed by the peripheral unit and the type of data transmission.

SYSTEM CONFIGURATION

§ 031.

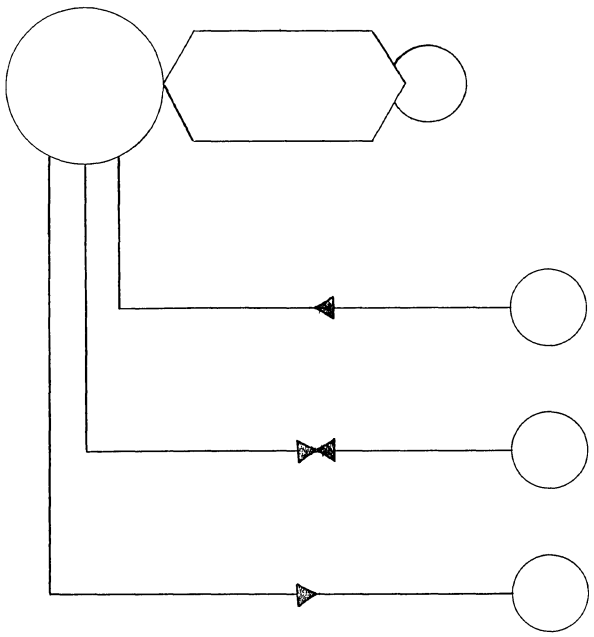
I. TYPICAL CARD SYSTEM

Deviations from standard configuration: . . . . . 80% more storage.
full simultaneity included.

Card Reader 40% slower.

Printing 40% slower.

Rental. $4,325



Equipment	Rental
Processor and Console: 2,600 Word Drum.	$1,735
High Speed Card Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 lines/min.	935

Optional Features Included: . . . . .

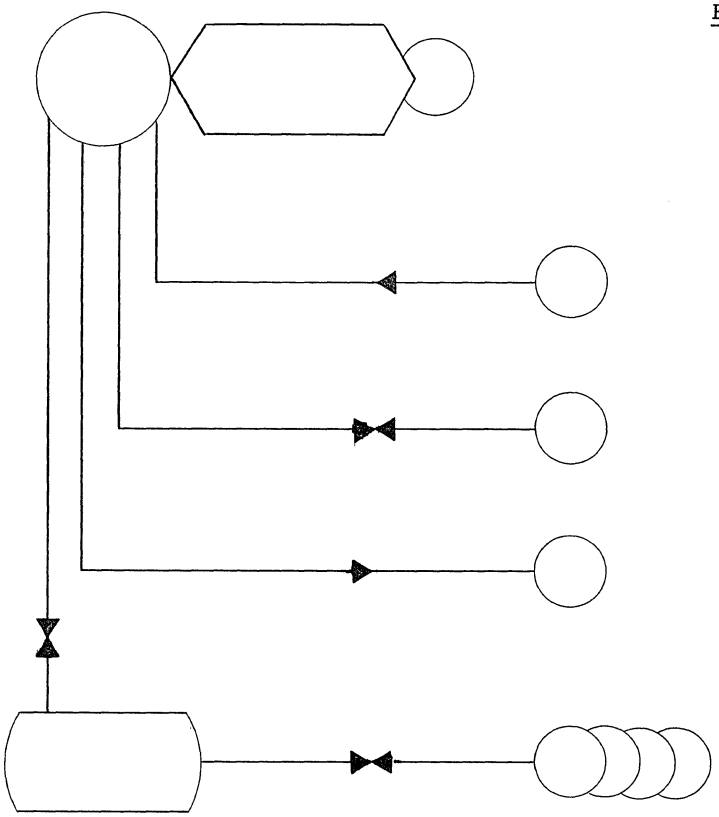
Multiply-divide.	400
20 print positions.	30
Stacker-Select on Reader.	35
Post Read Station on Read Punch.	100
Stacker-Select on Punch.	50
Program Interrupt	60
TOTAL	$4,325

§ 031.

II. 4-TAPE BUSINESS SYSTEM

Deviations from standard configuration: . . . . . 80% more storage.
full simultaneity included.
indexing included.

Rental: . . . . . $7,125.



Equipment	Rental
Processor and Console: 2,600 Word Drum	$1,735
High Speed Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 lines/min.	935
Control: Synchronizer	1,000
4 Uniservo IIs	1,800
16,400 char/min.	

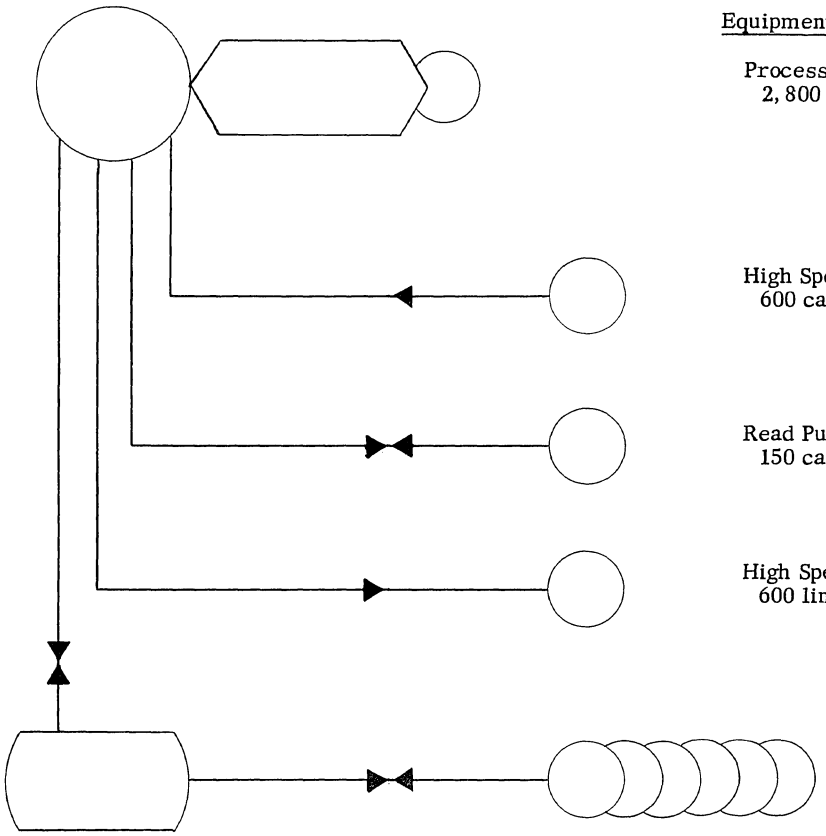
Optional Features Included: . . . . . Multiply-divide. 400
20 print positions. 30
Stacker Select on Reader and Punch. 85
Post-Read Station on Punch. 100
Program Interrupt. 60

TOTAL $7,125

III. 6-TAPE BUSINESS SYSTEM

Deviations from standard configurations: . . . . . full simultaneity included.
no console typewriter.
magnetic tape units 50% slower.

Rental: $7,400



Equipment	Rental
Processor and Console: 2,800 Word Drum	$2,010
High Speed Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 lines/min.	935
Control: Synchronizer	1,000
6 Unisevo IIs	1,800
16,400 char/sec	

Optional Features Included: . . . . . Multiply-divide. 400
20 print positions. 30
Stacker-Select on Reader and Punch. 85
Post-Reader Station on Punch. 100
Program Interrupt 60

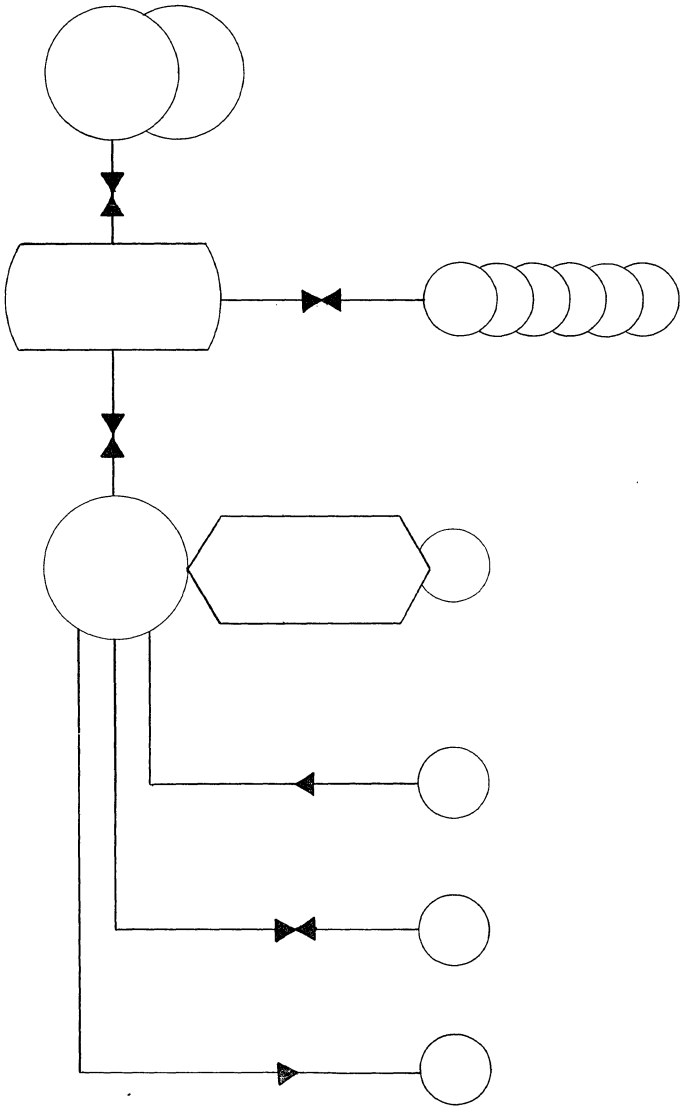
TOTAL $7,400

§ 031.

V. 6-TAPE AUXILIARY STORAGE

Deviation from standard configuration: . . . . . no console typewriter.
full simultaneity included.
magnetic tape units 50% slower.

Rental: $9,900



Equipment	Rental
Store: 21.5 million characters in 2 RANDEX File Drum Units.	$2,500
Control: Synchronizer	1,000
6 Uniservo IIs 16,400 char/sec.	1,800
Processor and Console: 2,800 Word Drum	2,010
High Speed Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 lines/min.	935

Optional Features Include: . . . . . Multiply-divide. 400
20 print positions. 30
Stacker-Select on Reader and Punch. 85
Post-Read Station on Punch. 100
Program Interrupt. 60

TOTAL $9,900

INTERNAL STORAGE: MAGNETIC DRUM

§ 041.

.1 GENERAL

.11 Identity: . . . . . SS 80/90 Magnetic Drum, Model I and Model II.

.12 Basic Use: . . . . . working storage.

.13 Description

The Magnetic Drum is the major store for all UNIVAC Solid-State systems. The drum rotates once every 3.4 milliseconds, and any reference to an operand or an instruction must wait until the drum is correctly positioned under the read/write heads. This action can take up to the 3.4 milliseconds necessary for a full revolution; however, for 1, 2, 3, 4, 5 or 8 bands of the drum, the maximum is reduced to 0.85 millisecond by the use of 4 read/write heads spaced 90 degrees apart around the circumference of the drum. (The nomenclature of these portions is confusing and has varied over the years. The official terminology is "Fast Access" for the slower access area of the drum, and "High Speed Access" for the faster access areas. Alternatively, the terms "Normal" and "Fast" have also been used to describe the same respective areas.)

Information is arranged on the drum in bands of 200 words, each of eleven 4-bit characters, and is operated upon in the Model I as words of 10 numeric characters with sign bit. However, the Model II uses the full four-bit sign character. Two models of the drum are available, a 25-band (5,000-word) drum, and a 46-band (9,200-word) drum. These numbers for bands do not include the buffer bands, which are also actually located on the drum. The smaller drum can be supplied with only 13 or more of the 25 bands being usable as in the STEP (Simple Transaction to Economical Processing). The other bands, however, are still physically present. Each band has either one or four read/write heads, so that the respective maximum access time is either one complete revolution or one-fourth of a revolution (3.4 milliseconds).

The decreased price which results from reduction in the drum storage capacity accounts for the greatest part of the price difference between the basic UNIVAC Solid-State system, and the reduced systems.

.14 Availability: . . . . . 10 months.

.15 First Delivery: . . . . 1958.

.16 Reserved Storage

Purpose: . . . . . I/O control.
Number of locations: . 2 to 4 bands, 200 words each.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic drum.

.22 Physical Dimensions

.222 Drum or Disc
Diameter: . . . . . approx. 5.
Thickness or length: . approx. 8.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by program: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume Per Band of 5 Tracks

Words with sign: . . . . 200.
Characters: . . . . . 1,000.
Digits: . . . . . 2,000.
Instructions: . . . . . 200.

.26 Bands Per Physical Unit: 15 to 49 per drum.

.27 Interleaving Levels: . . 1.

.28 Access Techniques

.281 Recording method: . . . fixed heads.
.283 Type of access

Description of Stage	Possible Starting Stage
Wait for drum rotation:	yes.
Read or write word:	no.

.29 Potential Transfer Rates

.291 Peak bit rates
Cycling rates: . . . . 17,670 rpm.
Track/head speed: . . 4,628 inches/sec.
Bits/inch/track: . . . 153.
Bit rate per track: . . 707,000 bits/sec/track.
.292 Peak data rates
Unit of data: . . . . . word (5 alpha or 10 numeric char).
Conversion factor: . . 60 bits/word.
Gain factor: . . . . . 5 tracks/band.
Loss factor (degree of interleaving): . . . . none.
Data rate: . . . . . 58,825 words/sec.

§ 041.

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see table.

.32 Rules for Combining Modules: . . . . . any combination of increments is possible.

.4 CONTROLLER: . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Stacks per system: . . 18 to 79.
Stacks per module: . . 18 to 79.
Stacks per yoke: . . . . 1, 2, or 4.
Yokes per module: . . . 18 to 49.
.512 Stack movement: . . . . none.
.513 Stacks that can access any particular location: . . . . . 1 per band, fast access.
4 per band, high speed access.
.514 Accessible locations By single stack: . . . 200 words.
.515 Relationship between stacks and locations: . Band (Address/200).
Band position Address (mod 200).

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . . 0 to 3,400 μsec.
Cycle time: . . . . . 17μsec.
For data unit of: . . . 1 word.

.532 Variation in access time

Stage	Time	Example
Wait for word to reach head		
Fast:	0 to 3,400 μsec.	1,700.
High Speed: . . .	0 to 850 μsec.	425.
Transmit word: .	17 μsec.	

.6 CHANGEABLE STORAGE: . . . . . none.

.7 AUXILIARY STORAGE PERFORMANCE

.71 Data Transfer: . . . . . data can be transferred from the drum to any part of the computer store.

.72 Transfer Load Size

With self: . . . . . 1 word, or 200 via tape buffer.
With core: . . . . . 1 to 200 words.

.73 Effective Transfer Rate

High speed store with self: . . . . . 1,850 words/sec.
High speed store with fast store: . . . . . 460 words/sec.
Fast store with self: . . 460 words/sec.

.8 ERRORS, CHECKS AND ACTION

Errors	Check or Interlock	Action
Invalid address:	none	accesses a predictable address.
Receipt of data:	parity	sets indicator.
Dispatch of data:	parity	processor stop.
Conflicting commands:	yes	processor stop.
Recovery of data:	parity	processor stop.

MODULE AND SYSTEM SIZES

Identity	Minimum Storage	"Fast" Increment	High Speed Increment	Maximum Storage
Drums:	1	-	-	1
Words:	2,600	200	400	8,800
Characters:	13,000	1,000	2,000	44,000
Instructions:	2,600	200	400	8,800
Bands:	13	1	2	44
Digits:	26,000	2,000	4,000	88,000
Modules:	1	-	-	1

INTERNAL STORAGE: RANDEX DRUM

§ 043.

.1 GENERAL

.11 Identity: . . . . . RANDEX Drum Storage Types No. 7965, 7957, and 7966.
RANDEX.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description:

The RANDEX Drum storage provides the auxiliary storage for the Solid-State system. Each module has either the capacity for one or two drums. Each drum has a capacity of 1,152,000 words of 44 data bits each, plus parity bits. A maximum system contains 10 such pairs of drums, for a capacity of 23,040,000 words.

Each drum is mounted with its axis horizontal and pairs are mounted one above the other. A common yoke mounted between them carries two heads, one to access a track on the upper drum and one to access a track on the lower drum.

Each drum is divided into 2,000 bands of 1 track each. Each track of 576 words is divided into 12 sectors of 48 words each. Only one sector in the RANDEX system can be accessed at a time.

Each sector can be considered also as four subsectors, each containing 1 key word and 11 data words. Special "search-read" and "search-write" instructions can be used with reference to subsector keys.

These instructions read and check a 10-character word against the labels on a 6-block area. Up to four labels per block can be used, thus providing a maximum search area of 24-records or six 48-word blocks, whichever is smaller. Fifteen areas per record can be searched.

Access time varies from 5 to 540 milliseconds and a typical time to locate, read, and update data in a subsector is approximately 450 milliseconds. However, except for 7 milliseconds of this time, all other simultaneity is preserved, provided that magnetic tapes on the RANDEX Synchronizer are not used.

This store is accessed as a peripheral device using a Buffer band and a Synchronizer which needs a special adaptation for the first RANDEX module only. Only one Synchronizer can be used.

The Synchronizer is capable of handling up to 10 RANDEX Drum units and up to 10 magnetic tape units.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . January, 1962.

.16 Reserved Storage: . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic drums.

.22 Physical Dimensions

.222 Drum or Disc
Diameter: . . . . . 24.3 inches.
Thickness or length: . . 44 inches.
Number on shaft: . . . 1.

.23 Storage phenomenon: . . magnetization.

.24 Recording Permanence

.241 Data erasable by program: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . . no.
.245 Storage changeable: . . . no.

.25 Data volume per band of 1 track

Words:	576
Characters:	2,880.
Digits:	5,760.
Instructions:	576.
Model 1 packed characters:	3,840.
Model 2 packed characters:	3,600.

.26 Bands per physical unit: 2,000.

.27 Interleaving Levels: . . . 1.

.28 Access Techniques

.281 Recording method: . . . moving heads.
.282 Reading method: . . . . same.
.283 Type of access

Description of stage

Wait for synchronizer not busy:	Access to a record can occur at any one of these stages, providing the drum is in the correct position.
Move head to selected track:	
(If writing) Fill buffer: . . .	
Wait for selected sector:	
(If reading) Empty buffer:	

§ 043.

.29 Potential Transfer Rates

.291 Peak bit rates
Cycling rates: . . . . . 870 rpm.
Track/head speed:. . . 1,108 inches/sec.
Bits/inch/track: 650
Bit rate per track: . . . 720,000 bits/sec/track.

.292 Peak data rates
Unit of data (character or word): . . . . . word.
Conversion factor (bits for unit): . . . . 44 bits/word.
Gain factor (tracks per band):. . . . . 1.
Loss factor (degree of interleaving): . . . 12.
Data rate: . . . . . 696 words/sec/device.

.3 DATA CAPACITY

.31 Module and System Sizes

[See table below]

.32 Rules for Combining Modules: . . . . . none, or 1 7965; or 1 7957; or up to 9 7966's with a 7965 or a 7957.

.4 CONTROLLER

.41 Identity: . . . . . Synchronizer. Type No. 7914.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . 1 to 10.
.432 Restrictions: . . . . . see Paragraph .13.

.44 Data Transfer Control

.441 Size of Load: . . . . . 48 words (1 block).
.442 Input-Output area:. . . . buffer band in Magnetic Drum.
.443 Input-Output area access:. . . . . entire block.
.444 Input-Output area lockout: . . . . . none, test busy required in program to protect area.
.445 Synchronization:. . . . automatic.
.446 Synchronizing aids: . . . test busy.
.447 Table control:. . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Stacks per system: . . . 20 maximum.
Stacks per module: . . . 2.
Stacks per yoke:. . . . . 2.
Yokes per module: . . . 1.
.512 Stack movement: . . . . across length of drum.
.513 Stacks that can access any particular location: . . . . . entire drum accessible.
.514 Accessible locations
By single stack
With no movement:. . 12 blocks.
With all movement:. . 12,000 blocks.
By all stacks
With no movement:. . 24 blocks per module. 240 blocks per system.

.53 Access Time Parameters and Variations

.532 Variation in access time

Stage	Variation, msec.	Example, msec.
Wait for Synchronizer not busy:	0 to 15	0.0.
Move head to selected track:	0, or 125 to 540	300.0
Fill buffer (writing):	3.4	3.4
Wait for selected block:	0 to 69	20.0
Write or read:	34.5	34.5
Empty buffer (reading):	3.4	0.0.
Total:		357.9.

.6 CHANGEABLE STORAGE: . . . . . none.

MODULE AND SYSTEM SIZES

	Minimum Storage				Maximum Storage
Identity:		No. 7965	No. 7957	No. 7966	
Drums:	0	1	2	2	20.
Words:	0	1,152,000	2,304,000	2,304,000	23,004,000.
Characters:	0	5,760,000	11,520,000	11,520,000	115,200,000.
Instructions:	0	1,152,000	2,304,000	2,304,000	23,040,000.
Blocks:	0	24,000	48,000	48,000	480,000.
Digits:	0	11,520,000	23,040,000	23,040,000	230,400,000.
Model 2 packed character:	0	7,680,000	15,360,000	15,360,000	153,600,000.
Model 1 packed character:	0	7,200,000	14,400,000	14,400,000	144,000,000.
Modules:	0	1	1	1	10.

§ 043.

.7 AUXILIARY STORAGE PERFORMANCE

.71 Data Transfer

Pair of storage units possibilities
With self: . . . . . no.
With Magnetic Drum: . yes.

.72 Transfer Load Size

With Magnetic Drum,
Model 2: . . . . . units of 320 packed characters.
With Magnetic Drum,
Model 1: . . . . . units of 300 packed characters or 240 characters.

.73 Effective Transfer Rate

With Magnetic Drum,
Model 2: . . . . . 4,640 packed char/sec.
With Magnetic Drum,
Model 1: . . . . . 4,350 packed char/sec or 3,480 char/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	sets indicator.
Receipt of data:	check	sets indicator.
Dispatch of data:	check	sets indicator.
Off Normal*:	check	sets indicator.
Physical record missing:	check	sets indicator.
Parity	check	sets indicator.

* Off Normal includes: . . . . . Buffer overflow
Buffer underflow
Block size
Bad spot
Bad track
Faulty operation
Interlock

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . . Central Processor. Model I.

.12 Description

The Central Processor is a solid state device with a basic operating cycle of 17 microseconds which operates on fixed length, fixed point decimal words of 10-digits size. Numbers are held in sign and absolute value; a zero may have either sign. Alphameric characters are regarded as two numeric characters, and alphameric comparison requires a short programming subroutine.

Preparing a line of print in accordance with a given format requires complex programming. No code conversions are normally required and zero suppression is available; however, all other editing functions (check protect, comma insertions, etc.) must be internally programmed. Transfer of data to the print buffer track, which consists of 26 words, must also be so programmed.

Programming of the Model I is basically governed by two factors:

(1) The input-output volume determines the minimum amount of central processor time to be used. If the time allotted to input-output provides sufficient time for the related internal processing, no reduction in overall timing can be effected. On the other hand, if internal processing should exceed input-output time, the total time for the problem will be the central processor time plus 10 per cent of the input-output time.

(2) The allocation of instructions and data on the drum so as to reduce instruction latency.* In general, the machine instructions are kept on either portion of the drum (i.e., either the fast or the normal), but an attempt is made always to keep the data on the fast portions.

The overall speed capacity of the Model I system is approximately 14,000 additions per second, if no input-output operation is in process. With all input-output units operating, the speed is reduced to approximately 12,000 additions per second, or approximately 1,200 possible instructions for each card read in. There are three arithmetic registers, three index registers, and one instruction register. The Magnetic Drum is also contained in the same cabinet.

* The "latency" of an operand or an instruction is the time spent waiting for it to come under the read/write heads. Programming the UNIVAC Solid State is often concerned with minimizing latency, and many techniques are used for this purpose.

.12 Description (Contd.)

The control of simultaneous operations is extremely simple because, in general, each peripheral device has a separate buffer band and controller circuits. The transfers between Buffer bands and working storage are different on the 80-column and 90-column versions and are again different for each type of peripheral device.

The Model I processor handles data in words of 10 digits plus a sign bit. Four bits are used for each digit, and a biquinary code is for the numbers 0 to 9. The other six characters of the code are called "undigits" and are written as A, B, C, F, G, and H. Each digit has an odd parity bit associated with it. Parity is checked during all data movements to or from storage. The central computer uses only numeric data, whereas the peripheral units use alphameric card data. This difference is resolved by splitting each alphameric word (10 characters) into 2 words, 1 zone and 1 numberic. The computer has three 1-word arithmetic registers A, X, and L. Register A is the accumulator and forms one half of a double length register, (combined AX), which is used for shifts and multiplication instructions.

Programming for the SS 80/90 Model is similar to programming for the IBM 650. As in most drum storage computers, latency problems emphasize the importance of program complexity. The instruction form is 1 + 1, (known as one and one half address). This instruction form uses the second address to state the location from which the next instruction is to be taken. There are 62 instructions including arithmetic (fixed point only), logical masking instruction, comparison instructions, a right-shift and a left-shift instruction, a zero-suppress instruction, and automatic translation instructions. These all operate on full words. Character manipulation is performed by a combination of shifts and logical AND and OR instructions.

The Model I has 3 index registers, which can be used to modify the first address in an instruction. Normally this address is the operand, but it can be a transfer-of-control address. The second (or next-instruction) address cannot be modified by index registers.

Data is held on the drum in 200-word "bands". There are two types of bands, with either one or four read/write heads. The access time to a particular operand is either from 0 to 3.4 milliseconds or 0 to 0.875 millisecond respectively for either one or four heads. These are much longer times than the actual instruction times themselves. (Addition only takes 0.085 millisecond.)

The data processing speed of the processor depends not only on the type of storage in which the instructions are held, but also on the degree of optimization

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.12 Description (Contd.)

estimates of data processing speeds are based on the assumption that standard practice has been followed. These are outlined in the performance section. attained. Both of the assembly programs do a considerable amount of automatic optimization. The

.13 Availability: . . . . . 10 months.

.14 First Delivery: . . . . June, 1959.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point			
Add-Subtract	yes	decimal	10 digits + sign.
Multiply			
Short:	sentinel	decimal	2 to 8 + sign.
Long:	yes	decimal	10 digits + sign.
Divide			
No remainder:	no.		
Remainder:	yes	decimal	2 to 10 digits + sign.
.212 Floating point			
Add-Subtract:	subroutine	decimal.	
Multiply:	subroutine	decimal.	
Divide:	subroutine	decimal.	
.213 Boolean			
AND:	yes } Binary		40 bits.
Inclusive OR:	yes }		40 bits.
.214 Comparison			
Numbers:	yes		10 digits.
Absolute:	subroutine		10 char.
Letters:*	subroutine		10 char.
Mixed:*	subroutine		10 char.

* requires 9 instructions (6 executed).

.215 Code translation: . . . all UNIVAC Solid-State systems except 90-column card systems have automatic code translation during card operations. All systems can translate word-by-word, between the internal coding and the appropriate card codes, and for the purposes of compatibility with UNIVAC I, II, etc., to Excess-3 code.

.217 Edit format

	Provision	Comment	Size
Alter size:	no.		
Suppress zero:	yes	also commas	10 chars.
Round off:	no.		
Insert point:	no.		
Insert spaces:	no.		
Insert:	yes	see Boolean	10 half chars.
Float:	no.		
Protection:	no.		

.218 Table look-up: . . . . . subroutine.

.219 Others: . . . . . in tape systems, the tape buffer may be utilized to transfer a band of 200 words from one part of the store to another. During the transfer all words move cyclically back one word in relative position, thus word number 6 becomes word number 5. Word number 1 becomes word number 0 and number 0 becomes number 199.

.22 Special Cases of Operands

.221 Negative numbers: . . . least significant 4 bits of each word always contain sign digit, 0 for positive, and 5 for negative.

.222 Zero: . . . . . both plus and minus zero can occur and are not equal in comparisons.

.223 Operand size determination: . . . . fixed.

.23 Instruction Formats

.231 Instruction structure: . 1 word.

.232 Instruction layout:

Part	Op	m	c	S
Size (digits)	2	4	4	1

.233 Instruction parts

Name	Purpose
OP:	operation code.
m:	memory address (indexable) second instruction address, or operation variation.
c:	next instruction address.
S:	Index Register.

.234 Basic address structure: 1 + 1.

.235 Literals

Arithmetic: . . . . . only set register to zero.

Comparisons and tests: . . . . . none.

.236 Incrementing modifiers: . . . . . yes.

.236 Directly addressed operands

.2361 Internal storage type

	Min. size	Volume accessible
Magnetic Drum:		9,200 words.
Magnetic Core:		1,280 words.
RANDEX:		23,040,000 words.

.2362 Increase address capacity: . . . . . not needed.

.237 Address indexing

.2371 Number of methods: . 2.

.2372 Names: . . . . . Indexing.
Band Modification.

.2373 Indexing rule: . . . . . increment added to instruction address. Under certain circumstances the address is made to cycle within a band (200 words) of drum store. Otherwise, it cycles either modulo 5,000 or modulo 10,000 depending on the store size.

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.2374 Indexing specification: by the programmer: numbers 1 to 3 on the coding sheet.
in the machine instruction: use of the sign bit, and 1 bit of the operation code.
.2375 Number of potential indexers: . . . . . 3.
.2376 Addresses which can be indexed: . . . . . all.
.2377 Cumulative indexing: . none.
.2378 Combined index and step: . . . . . no.
.238 Indirect addressing: . . none.
.239 Stepping
.2391 Specification of increment: . . . . . in stepping instruction.
.2392 Increment sign: . . . . positive; complements used for decrements.
.2393 Size of increment: . . 4 digits (16 bits used hexadecimally in Model 2 when addressing core).
.2394 End value: . . . . . in test instruction.
.2395 Combined step and test: . . . . . no.

.24 Special Processor Storage

.241 Category of storage

	Number of locations	Size in words	Program usage
Register:	4	1	arithmetic, temporary storage, and control.
Index:	3 or 9	0.4	indexing.
Buffers:	3 to 5	200	input-output.

.242 Category of storage

	Total No. of locations	Physical Form	Access time μsec	Cycle time μsec
Register:	4	hardware	17	17.
Index:	3 or 9	3 in hardware, 6 in core	17	17.
Buffers:	3 to 5	drum bands	3,400 to 5,100	3,400

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: 1 + 1 addressing.

.32 Look-Ahead: . . . . . yes, the next instruction.

.33 Interruption

.331 Possible causes
In-out units: . . . . . High Speed Reader Buffer Loaded (optional).
.332 Program control
Individual control: . . High Speed Reader.
Method: . . . . . executing a Card Read instruction will activate interruption when Read buffer is loaded.
Restriction: . . . . . none.
.333 Operator control: . . . none.
.334 Interruption conditions: buffer loaded.
.335 Interruption process
Disabling interruption: none.
Registers saved: . . . next instruction stored in fixed location.
Destination: . . . . . a fixed location.
.336 Control methods
Determine cause: . . implicit.
Enable interruption: . always enabled.

.34 Multi-running: . . . . . none.

.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μsec:

.411 Fixed point
Add-subtract: . . . . 85.
Multiply: . . . . . 85 + 170D.
Divide: . . . . . 85 + 187D.
.412 Floating point: . . . . . none.
.413 Additional allowance for
Indexing: . . . . . 17.
Indirect addressing: . none.
Re-complementing: . none.
.414 Control
Compare: . . . . . none.
Branch: . . . . . 34.
Compare & branch: . 51.
.415 Counter control
Step: . . . . . 68.
Step and test: . . . . . none.
Test: . . . . . 51.
.416 Edit: . . . . . 68 (10 char zero suppress).
.417 Convert: . . . . . 51 (10 char).
.418 Shift: . . . . . 51 + 17D.

.42 Processor Performance in μsec

.421 For random addresses
For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data are held in random positions on the High speed portion.
c = a + b: . . . . . 833.
b = a + b: . . . . . 1,411.
Sum N items: . . . . 289N.
c = ab: . . . . . 867 + 187D.
c = a/b: . . . . . 867 + 187D.
.422 For arrays of data
For the following times, it is assumed that the instructions are stored on Normal access portions of the drum, but executed in the Fast portion. This effectively reduces the time lost at the end of each iteration of the loop because of poor latency. It does involve some additional word in actually transferring the data, and this is shown separately under Set-Up Time.

	Set-Up	Execution
$c_i = a_i + b_j$:	3,400	1,700.
$b_j = a_i + b_j$:	3,400	1,700.
Sum N items:	1,700	850N.
$c = c + a_i b_j$:	3,400	2,550N.

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.423 Branch based on comparison

For the following times, it is assumed that the instructions are stored on Normal access portions of the drum, but executed in the Fast portion. This effectively reduces the time lost at the end of each iteration of the loop because of poor latency. It does involve some additional word in actually transferring the data, and this is shown separately under Set-Up Time.

	Set-Up	Execution
Numeric data: . . .	3,400	1,700.
Alphabetic data: . .	5,100	1,870.

.424 Switching

For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data are held in random positions on the High speed portion.

Unchecked:	510N.
Checked:	799N.
List search:	850N.

.425 Format control per character

For the following times, it has been assumed that the instructions are held on the Normal access portions of the drum in known positions, and that the data are held in random positions on the High speed portion.

Unpack:	51N.
Compose:	485N.

.426 Table look up per comparison

For the following times, it is assumed that the instructions are stored on Normal access portions of the drum, but executed in the Fast portion. This effectively reduces the time lost at the end of each iteration of the loop because of poor latency. It does involve some additional word in actually transferring the data, and this is shown separately under Set-Up Time.

.426 Table look up per comparison (Contd.)

	Set-Up	Execution
For a match:	340	1,700N.
For least or greatest:	510	1,700N.
For interpolation point:	510	1,700N.

.427 Bit indicators

For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data are held in random positions on the High speed portion.

Set bit in separate location:.	340.
Set bit in pattern:. .	1,122.
Test bit in separate location:.	374.
Test bit in pattern: .	442.
Test AND for B bits:	442.
Test OR for B bits: .	442.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	program jump.
Underflow (float-pt):	none.	
Zero divisor:	check	program jump.
Invalid data:	not possible.	
Invalid operation:	some checks	stops or partial execution.
Arithmetic error:	some checks	sometimes stops.
Invalid address:	checks	modulo store size.
Receipt of data:	error word	program jump.
Dispatch of data:	error word	program jump.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . Central Processor Control Panel.

.12 Associated Units: . . . . Processor Keyboard standing on the desk.

.121 Description:

The keyboard has 13 keys which include:

1. The digits 0 through 9
2. Plus and minus enter keys
3. An Alert key that clears a preselected input register
   Any combination of four bits can be entered. A lamp lights on the keyboard after pushing the Alert key indicating that the processor is ready to accept input from the keyboard.

.2 CONTROLS

.21 Power

Name	Form	Function
AC:	button-light	turns off AC and DC power.
DC:	button-light	turns off DC power.
DC Ready:	button-light	turns on AC and DC power.
Drum:	button-light	turns off AC and DC power.
Uniservo:	button-light	turns power to Uniservos on and off.

.22 Connections: . . . . . no positive indication.

.23 Stops and Restarts

.231 Stops

Name	Form	Function
Tape:	button	Causes Tape Off-Normal condition.
HSP:	button	Causes High Speed Printer Off-Normal condition.
FR:	button	Causes High Speed Reader Off-Normal condition.
RPU:	button	Causes Read Punch Off-Normal condition.
Comparison Stop:	button	Causes Stop on compare instructions.
Stop:	button	Stop Processor.

.232 Starts

Name	Form	Function
Tape Check:	button	Completes partially-executed tape commands.
Start:	button	Starts processor.
m:	button	Selects next address of two.
c:	button	Addresses to which control will be transferred when the Start button is depressed.

.24 Stepping

Name	Form	Function
W/O Index Regs:	button	execute one instruction without index registers when start button pushed.
W Index Regs:	button	execute one instruction with index registers when start button pushed.
Continuous:	button	executes instructions under program control when start button pushed.

.25 Resets

Name	Form	Function
General Clear:	button	resets indicators and logic.

.26 Loading: . . . . . none.

.27 Special

Name	Form	Function
No Print:	button-light	print orders executed but no printing occurs.
96 Check:	button-light	causes stop if card buffer is not emptied fast enough.
No Punch	button-light	punch orders executed but no punching occurs.

.3 DISPLAY

.31 Alarms: . . . . . none.

.32 Conditions

Name	Form	Function
Printer:	light	Off-Normal
Fast Reader:	light	Indicates that a malfunction
Read Punch:	light	has occurred in the particu-
Processor:	light	lar unit.
Test:	light	
Tape Sync.:	light	

§061.

.33 Control Registers

Name	Form	Function
Static Register:	two 5, 4, 2, 1 bit neon decades	indicates statically and dynamically what instruction is being executed.
Sign:	two neons	indicates the sign of quantity in display register.
Display Register:	ten decades	in one of the following registers: rA, rC, rL, or rX, depending upon which display button is pushed.

.34 Storage: . . . . . displayed in the Display register via rA, rC, rL, or rX.

.4 ENTRY OF DATA

.41 Into Control Registers: . same as Control Registers but via a control register plus executing store instruction, also keyed in.

.5 CONVENIENCE

.51 Communication: . . . . . none.

.52 Clock: . . . . . none.

.53 Desk Space: . . . . . length 22", depth 6", height 48".

.54 View: . . . . . operator must be standing to operate console; view is unobstructed by peripheral units Punch, Printer, and Reader.

INPUT-OUTPUT: HIGH SPEED READER

§ 071.

.1 GENERAL

.11 Identity: . . . . . High Speed Reader.
I: 80-Column Reader.
Unit No. 7935.

II: 90-Column Reader.
Unit No. 7945.

.12 Description

The high speed reader reads up to 600 cards per minute using two read stations, translating card images into machine codes and transferring them into the computer store. During 95 per cent of the time involved in the transfer, the central processor can continue operations. A standard subroutine function which uses up 7 per cent more of the card cycle time compares the card images, giving a total effective performance of 3,600 cards per minute read, translated, and verified with 88 per cent central processor overlap.

Both types of the 600 cards per minute reader are equipped with a hopper, 2 read stations, and optionally, 3 stackers. The only difference between the two types is the number of columns sensed by the read stations. A vacuum system to assist card feeding is standard equipment. A Stacker Select and an Automatic Program Interrupt feature are available as options.

The buffer between the reader and processor receives card images from both read stations whenever a card passes either. Should either of the stations be empty, the empty station will transmit the image of a card with every hole punched. Another feature of the reader is that a card is passed by both read stations and is moved into a stacker without stopping. A control routine is required to prevent the image from the first read station being overwritten by another image transmitted when the card passes the second read station unless the Automatic Program Interrupt option is used. When this option is available, the processor performs the following operations when the buffer is loaded. First the current instruction is completed and the next instruction is stored in a fixed location. Control is then transferred to a subroutine. The last instruction of the subroutine causes control to be returned to the fixed location from which normal program sequencing is resumed.

Correctness of card reading is verified by routines in the processor and not in the reader. This internal redundancy check is more secure than hole counts and similar reader checks because it also covers the transfers between the reader and internal storage. However, this check requires both processor time and storage space to hold the separate images which are not required by automatic input checking systems. When checking is desired, an area must be reserved in storage for both images so that the comparison may be performed.

.13 Availability: . . . . . 3 months.

.14 First Delivery: . . . . . November, 1958 - 90-Col.
December, 1959 - 80-Col.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . . pinch roller.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording systems: . . . none.
.222 Sensing system: . . . . . brush.
.223 Common system: . . . . none.

.23 Multiple Copies: . . . . . none.

.24 Arrangement of Heads

	80-Column	90-Column
Use of station:	Read	Read.
Stacks:	1	1.
Heads/stack:	80	45.
Method of use:	1 row at a time	1 row at a time.
Use of station:	Verify read	Verify read.
Distance:	15 rows	15 rows.
Stacks:	1	1.
Heads/stack:	80	45.
Method of use:	1 row at a time	1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . Standard punched card.
.312 Phenomenon: . . . . . punched holes; rectangular on 80-column; round on 90-column.

.32 Positional Arrangement

.321 Serial by: . . . . . 12 rows.
.322 Parallel by: . . . . . 80- or 45-columns.

.33 Coding: . . . . . 80-column (Hollerith, binary, column binary).
90-column (standard 90 column code).

.34 Format Compatibility: . . 80-column card, any 80-column equipment.
90-column card, any 90-column equipment.

.35 Physical Dimensions: . . standard punched card.

.4 CONTROLLER

.41 Identity: . . . . . built into Central Processor and the unit. Contains a special buffer band on the processor's drum to transmit and receive card images.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

§ 071.

.43 Connection to Device

.431 Devices per controller: . 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 2 cards.
.442 Input-Output areas: . . . 2 interlaces on buffer band of 200 words.
.443 Input-Output area access: . . . . . 1 band.
.444 Input-Output area lockout: . . . . . area insecure without program tests unless Automatic Interrupt feature is used.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . . automatic.
.447 Synchronizing aids: . . . interrupt.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 card.
.512 Block demarcation Input: . . . . . fixed size (80- or 90-column).

.52 Input-Output Operations

.521 Input: . . . . . one image from each of two stations if a card was read at either.
.522 Output: . . . . . none.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . . instruction provided.

.54 Format Control: . . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . no.
Offset card: . . . . . no.
Select stacker: . . . . . yes.
Select format: . . . . . no.
Select code: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . no.
Busy device: . . . . . yes.
Output lock: . . . . . no.
Nearly exhausted: . . . . no.
Busy controller: . . . . . yes.
End of medium marks: . no.
Input buffer full: . . . . . yes.
Off-Normal*: . . . . . yes.

* Off-Normal is a general term for any abnormal condition including:
empty stations.
full stacker.
empty hopper.
card jam.
equipment malfunction.

.6 PERFORMANCE

.61 Conditions: . . . . . no variation.

.62 Speeds

.621 Nominal or peak speed: . 600 c.p.m.
.622 Important parameters:

Name	Value
Cycle time:	100 m sec.
Select stacker time span:	100 m sec.
Feed card instruction time span:	100 msec.
Unload buffer time span:	15 msec.

.623 Overhead: . . . . . 1 clutch point.
Note: up to four read orders can be stacked by this unit.
.624 Effective speeds: . . . . (600-C) c.p.m.
C = number of clutch points missed per minute.

.63 Demands on System

Component	Condition	msec per card		Percentage
Central Processor:	unload images	3.5	or	3.0.
Central Processor:	verify overhead	7.0	or	6.0

Note 1: If the second read station is used to verify the reading at the first read station, the central processor must unload the second image and perform the comparison.

Note 2: The data read into the buffer band are stored in interleaved locations around the drum. To maximize processing efficiency, these data should be processed from the interleaved locations, since outputting computed results requires another kind of interleaved pattern which is best loaded from the input interleaved array.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Clear:	button-light	turn off "Off-Normal".
Computation:	2 buttons	stops and starts processor.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	1,000 cards.
Stackers (3):	1,200 cards each.

.732 Replenishment time: . . 0.2 to 1.0 min. does not need to be stopped.
.733 Adjustment time: . . . . 1 to 5 minutes.
.734 Optimum reloading period: . . . . . 1.66 minutes.

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.8 ERRORS, CHECKS AND ACTION

Errors	Check or Interlock	Action
Reading:	none.	
Input area overflow:	fixed.	
Invalid code:	all legal.	
Exhausted medium:	see "Off-Normal".	
Imperfect medium:	none.	
Timing conflicts:	program stall.	wait.
Off-Normal*:	check.	set indicator.

* Off-Normal includes: . . . . . exhausted medium.
equipment malfunction.

INPUT-OUTPUT: READ PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . . Read Punch.
80-column Punch Unit.
No. 7936.

90-column Punch Unit.
No. 7946.

.12 Description:

These two card punching units are able to process cards at a peak speed of 150 cards per minute, using a single point clutch.

Type 7936 contains 5 card stations: read, wait, punch, wait and read. The punch station is fitted for 80-column cards.

Type 7946 contains 3 card stations: read, punch and read. The punch station is fitted for 90-column cards.

The read stations are optional and can be fitted to read either 80- or 90- column cards in either type, although it is unlikely that mixtures are required. Each type has one hopper and two stackers, but the stacker select feature is optional.

There are automatic input code translations and four special instructions are available to perform some translation (see Internal Storage, Magnetic Drum, paragraphs 1.3) either for 80-column patterns or 90-column patterns.

The optional read stations are intended for use in conjunction with the punch. The last station permits sending an image of the card to enable verification in a routine. The first station permits reading part-punched cards before completing the punching. Note that two input and one output images are transmitted on any stimulated cycle of the device.

.13 Availability: . . . . . 7 months.

.14 First Delivery: . . . . . No. 7936 - December, 1959.
No. 7946 - June, 1958.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . . pinch rollers.
.212 Reservoirs: . . . . . Type 7936 only.
Number: . . . . . 2.
Form: . . . . . wait stations.
Capacity: . . . . . 1 card each.
.213 Feed drive: . . . . . pinch rollers.
.214 Take-up drive: . . . . . pinch rollers.

.22 Sensing and Recording Systems

.221 Recording system: . . . . punch and die.
90 char, round holes.
80 char, rectangular holes.
.222 Sensing system: . . . . . brush.
.223 Common system: . . . . no.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

	80-Column	90-Column
• Use of station:	read	read.
Stacks:	1	1.
Heads/stack:	80 or 45	45 or 80.
Method of use:	1 row at a time	1 row at a time.
Use of station:	wait	none.
Distance:	5 card rows.	
Stacks:	none.	
Heads/stack:	none.	
Method of use:	N. A.	
Use of station:	punch	punch.
Distance:	5 card rows	1 card.
Stacks:	1	1.
Heads/stack:	80	45.
Method of use:	1 row at a time	1 row at a time.
Use of station:	wait	none.
Distance:	5 card rows.	
Stacks:	none.	
Heads/stack:	none.	
Method of use:	N. A.	
• Use of station:	read	read.
Distance:	5 card rows	1 card.
Stacks:	1	1.
Heads/stack:	80 or 45	45 or 80.
Method of use:	1 row at a time	1 row at a time.

• These stations are optional.

.33 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard punch card.
.312 Phenomenon: . . . . . punched holes.
80 char rectangular.
90 char round.

.32 Positional Arrangement

.321 Serial by: . . . . . row (1 out of 12).
.322 Parallel by: . . . . . 80 col on 80 char card.
45-col on 90 char card.

.33 Coding: . . . . . Hollerith, column binary, binary, on 80-col card. Standard 90-col card code.

§ 072.

.34 Format Compatibility

80-column: . . . . . any 80-column equipment.
90-column: . . . . . any 90-column equipment.

.35 Physical Dimensions: . . standard punched card.

.4 CONTROLLER

.41 Identity: . . . . . built into Central Processor and the unit. Contains a special buffer band on the processor's drum to transmit and receive card images.

.42 Connection to System

.421 On-line: . . . . . 1 max.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . 1 max.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 3 cards (2 input and 1 output).
.442 Input-output areas: . . . 3 interlaces on 1 buffer band.
.443 Input-output area access: . . . . . band.
.444 Input-output area lockout: . . . . . punch area of buffer is locked out until punches are set up from previous instruction.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 card.
.512 Block demarcation
Input: . . . . . fixed.
Output: . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . 2 cards.
.522 Output: . . . . . 1 card.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . . automatic.

.54 Format Control: . . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . . no.
Offset card: . . . . . no.
Select stacker: . . . . . yes.
Select format: . . . . . no.
Select code: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . no.
Busy device: . . . . . yes.
Output lock: . . . . . no.
Nearly exhausted: . . . . no.
Busy controller: . . . . . yes.
End of medium marks: . no.
Off Normal*: . . . . . yes.
Input buffer full: . . . . yes.

* Off Normal includes: . empty stations.
full stackers.
empty hopper.
card jam.
equipment malfunction.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed . 150 c.p.m.
.622 Important parameters

Name	Value
Cycle:	400 m.sec.
Stacker select time span:	116 m.sec.
Start time span: . . .	133 m.sec.
Buffer unload time span:	136 m.sec.

.623 Overhead: 1 clutch point.
.624 Effective speeds: . . . . (150-C) c.p.m.
C = number of clutch points missed per minute.

.63 Demands on System

Component	Condition	m.sec. per card		Percentage
Central Processor	load buffer 1	3.5	or	0.9.
Central Processor:	unload buffers 2 & 3	3.5	or	0.9.
Central Processor:	note 1 below	10.4	or	2.7.

Note 1: If the second read station is used to verify the reading at the first station plus the punching done at the punch station, the program must merge the punch and first read images and compare punch and second read images.

Note 2: The data read into the buffer hand are stored in interleaved locations around the drum. To maximize processing efficiency, these data should be processed from the interleaved locations as the output computed results require another kind of interleaved pattern which is best loaded from the interleaved array upon input.

§ 072.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Computation	2 Buttons	starts & stops processor.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	600 cards.
Stackers (2):	1,200 cards each.

.732 Replenishment time: . . 0.25 to 1 mins.
does not need to be stopped.

.733 Adjustment time: . . . . 1 to 2 mins.

.734 Optimum reloading period: . . . . . 4 mins.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording	none.	
Reading:	none.	
Input area overflow:	not possible.	
Output block size:	fixed.	
Invalid code:	none.	
Exhausted medium:	see "off normal".	
Imperfect medium:	none.	
Timing conflicts:	interlock	wait.
Off Normal*:	check	set indicator.

* Off Normal includes: . . . . . punch bin full.
hopper empty.
stacker full.
card jam.
malfunction.

INPUT-OUTPUT: PAPER TAPE READER

§ 073.

.1 GENERAL

The paper tape reader and punch are two separate units housed in the same cabinet with their joint controller. The photoelectric reader operates at 500 characters per second. Five-, six-, seven-, or eight-channel tape can be read, checked for parity, translated into six-bit biquinary code, and stored in a 20-character buffer found in the synchronizer that is part of the entire paper tape unit.

The program is able to test the buffer to transfer 10 characters at a time into the arithmetic registers of the computer. The time involved is 187 microseconds per transfer, or less than 1 per cent of the overall computer capacity.

.2 PHYSICAL FORM

A friction drive mechanism is used, with two 1-foot capacity reservoirs. A spooler can be added as an optional extra to take up the paper tape after it has been read.

.3 EXTERNAL STORAGE

Normal punched tape, with fully punched holes, is used. Five-, six-, or seven-channel tapes can be used normally. An eight-channel tape can be used, but the eighth channel is restricted to some special function, as all other channels must be unpunched when the eighth is punched.

Various codes can be accommodated, including Teletype, Flexowriter and DaSPan. Each installation decides its own "End of Message" and "End of Tape" signals, which can be two or three characters long. In addition, an installation-chosen signal is used as the "ignore" signal. Neither the "ignore" nor "blank" characters are read into the buffer.

.4 CONTROLLER

The central processor in a UNIVAC Solid-State system is the controller. Only one paper-tape system can be connected to a system. Access is directly into the arithmetic registers, and occurs only upon request. The amount transferred each time is 10 characters. The paper tape synchronizer contains a 20-character buffer. After the buffer has been filled, the reader pauses until it becomes unloaded.

.5 PROGRAM FACILITIES AVAILABLE

Reading, once started, continues until either a stop character is read or a stop instruction is executed. Failure to unload the 20-character buffer causes an indefinite pause in reading. Translation is

.5 PROGRAM FACILITIES AVAILABLE (Contd.)

controlled by plugboard and parity checking is controlled by a rotary switch. The reader shares both these controls with the punch unit.

"Ignore" characters and blanks are suppressed before the buffer is loaded. The program can test for whether the buffer is loaded or whether the unit is disabled, but cannot distinguish between the various possible disabling causes, such as torn tape, plugboard not in place, overheating, or no paper.

.6 PERFORMANCE

The peak speed of the reader is 500 characters per second. The effective speed is the same, provided that the buffer is unloaded once each 20 milliseconds. If not, the cost is the ? -millisecond stop-start time, which would otherwise be overlapped.

During the reading of the tape, the buffer is first filled; then its contents are transferred to the automatic registers. Transfer of the buffer contents to the registers takes place each 20 milliseconds, or within from 6 to 7 drum revolutions. This operation takes only 0.20 millisecond, including subsequent transfer of data to storage as well. The transfer to storage can take an additional 3.4 milliseconds or 0.85 millisecond, depending upon whether the store data is in Normal or Fast areas of the drum.

.7 EXTERNAL FACILITIES

The plugboard which controls the code translation can be changed in approximately 20 seconds if a new one is available, or it can be rewired in less than 20 minutes.

The parity control switch sets the unit to check a specific channel for odd or even parity, or to ignore that channel altogether.

The optional spooler holds a 500-foot reel, which can be read in 2 minutes. Changing reels takes about 1 minute. Take-up facilities are standard.

.8 ERRORS, CHECKS AND ACTION

Parity is checked during reading, and buffer overflow is avoided by an automatic pause, or interlock.

These errors effectively cause the unit to be "disabled":

Torn Tape.
Power Off.
Overheating.
Improper Airflow.
Plugboard Not in Place.

INPUT-OUTPUT: PAPER TAPE PUNCH

§ 074.

.1 GENERAL

The paper tape reader and punch are two separate units housed in the same cabinet with their controller. The punch operates at 100 characters per second. Tape with five, six, seven, or eight channels can be punched, with or without parity being generated for each character. A plugboard is used to translate from six-bit biquinary code to output code. A 10-character buffer in the synchronizer is used to store the data being punched.

The program is able to test the buffer and to transfer 10 characters at a time into the computer's arithmetic registers. The time involved is 85 microseconds per transfer, or less than 0.1 percent of the overall central processor capacity.

.2 PHYSICAL FORM

A sprocket drive mechanism is used.

.3 EXTERNAL STORAGE

Normal punched tape, with fully punched holes, can be used. Tapes with five, six, or seven channels can be used normally. An eight-channel tape can be used, but the eighth channel is restricted to some special function, as all other channels must be unpunched when the eighth is punched.

Various codes can be accommodated, including Teletype, Flexowriter, DaSPan, etc.

.4 CONTROLLER

The central processor functions as the controller, and only one paper-tape system can be connected to a UNIVAC Solid-State system. The rather unusual procedure for providing data to the punch is directly from the arithmetic registers, and 10 characters are transferred each time. The paper

.4 CONTROLLER (Contd.)

tape synchronizer has a 10-character buffer, which is tested to determine whether the previous operation has been completed.

.5 PROGRAM FACILITIES AVAILABLE

Punching occurs serially in sets of 10 characters. For instance, six characters can be punched accompanied only by four blanks. The punch buffer is not automatically protected, and a program check must be made prior to loading. Translation is controlled by plug-board, and parity checking by a rotary switch. Both these controls are shared with the reader.

.6 PERFORMANCE

Both the peak and effective speeds are 100 characters per second.

.7 EXTERNAL FACILITIES

The plugboard which controls the code translation can be changed in approximately 1 minute if a new one is available, or can be rewired in less than 20 minutes. The parity control switch sets the unit to check a specific channel for odd or even parity, or to ignore that channel altogether. An additional option is the ability to punch Teletype code. The supply spooler has a 500-foot reel which can be punched in 10 minutes. Changing reels takes approximately 1 minute. Take-up facilities are standard.

.8 ERRORS, CHECKS AND ACTION

Parity is checked during reading, and buffer overflow is avoided by an automatic pause, or interlock. Physical conditions which cause the unit to become disabled include torn paper, overheating, insufficient airflow, or no power.

INPUT-OUTPUT: HIGH SPEED PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . . High Speed Printer.
Printer.
Unit No. 7912.

.12 Description

The High Speed Printer has been used with UNIVAC systems since 1952. Its peak speed is 600 lines per minute, dropping to 300 lines per minute for 2½-inch spacing of lines.

The print line can contain 100, 110, 120 or 130 positions at a pitch of 10 per inch; lines may be spaced at either 6 or 8 per inch as set by the operator.

The printer has a set of 51 characters engraved on print wheels and up to 5 carbon copies can be produced.

Inter-line spacing can be controlled only by specifying the number of line spaces between printed lines in the program. There is no form control loop and a program must count its way over pre-printed forms.

The stationery must be sprocket-punched, card or paper stock.

.13 Availability: . . . . . 10 months.

.14 First Delivery: . . . . June, 1958.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket push-pull.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . on-the-fly hammer stroke against print wheels.
.222 Sensing system: . . . . none.
.223 Common system: . . . none.

.23 Multiple Copies

.231 Maximum number
Interleaved carbon at least: . . . . . 5.
Carbon creep: . . . . none.
.233 Types of master
Multilith: . . . . . special ribbon and form.
Xerox: . . . . . yes.
Spirit: . . . . . special form.

.24 Arrangement of Heads

Use of station: . . . . . print.
Stacks: . . . . . 1.
Heads/stack: . . . . . 100 - 130 (increments of 10).
Method of use: . . . . . line at a time.

.25 Range of Symbols

Numerals:	10	0 - 9.
Letters:	26	A - Z.
Special:	15	: , $ - # * % ; / + . & ' ( )
Alternatives:		none.
FORTRAN set:		no.
Basic COBOL set: . . .		see note.
Total:	51.	

Note: With a substitution of the apostrophe (') for the required COBOL quotation mark ("), this would be an acceptable required COBOL set.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . paper stock.
.312 Phenomenon: . . . . . printing.

.32 Positional Arrangement

.321 Serial by: . . . . . line.
.322 Parallel by: . . . . . 100 to 130 positions.

.33 Coding: . . . . . 6-bit printer code.

.35 Physical Dimensions

.351 Overall width: . . . . . 4 to 21 inches.
.352 Length: . . . . . any length is acceptable.
.353 Maximum margins
Left: . . . . . 3.5 inches.
Right: . . . . . 3.5 inches.

.4 CONTROLLER

.41 Identity: . . . . . built into Central Processor and the unit contains a special 200 word buffer band on the processor's drum which transmits the print data to the unit.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

§ 081.

.44 Data Transfer Control

.441	Size of load:	1 line.
.442	Input-output areas: . .	buffer band.
.443	Input-output area access:	1 band.
.444	Input-output area lockout:	locked out while Printer is printing or spacing.
.445	Table control:	none.
.446	Synchronization:	automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511	Size of block:	1 line.
.512	Block demarcation	
	Input:	none.
	Output:	fixed.

.52 Input-Output Operations

.521	Input:	none.
.522	Output:	1 line.
.523	Stepping:	feed 0 to 79 lines alone or as a preliminary to printing.
.524	Skipping:	none.
.525	Marking:	none.
.526	Searching:	none.

.53 Code Translation: . . . none.

.54 Format Control: . . . . none.

.55 Control Operations

Disable:	no.
Request interrupt: . . .	no.
Select format:	no.
Select code:	no.
Unload:	no.

.56 Testable Conditions

Disabled:	see Off Normal.
Busy device:	yes.
Output lock:	no.
Nearly exhausted: . . .	no.
Busy controller:	yes.
End of medium marks:	no.
Off Normal*:	yes.
*Off Normal includes:	no paper. no ribbon. equipment malfunction.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 600 lpm.

.622 Important parameters

Name	Value
Vertical speed:	20 inches/sec, max.

.623	Overhead:	number of lines spaced before printing.
.624	Effective speeds: . . .	60,000/(100 + 8 (L-1)) lines a minute. L = average number of lines skipped per line printed.

.63 Demands on System

Component	Condition	msec per line	Percentage
Central Processor:	load buffer	10.1	10.1
Central Processor:	(note)	4.0	4.0

Note: As data must be arranged in the print interleaved pattern, 26 words must be moved.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Form tractors:	set screws	
Vertical alignment:	clutched drive	normally disengaged.

.72 Other Controls

Function	Form	Comment
Computation:	button	starts/stops Central Processor.
Paper Feed:	button light	advances paper 1 line.
Change Ribbon:	button	rewinds ribbon.
General Clear:	button light	resets error interlocks.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Bin:	1,000 sets.

.732	Replenishment time: . .	2 to 5 minutes. printer needs to be stopped.
.733	Adjustment time: . . .	2 to 5 minutes.
.734	Optimum reloading period:	100 minutes.

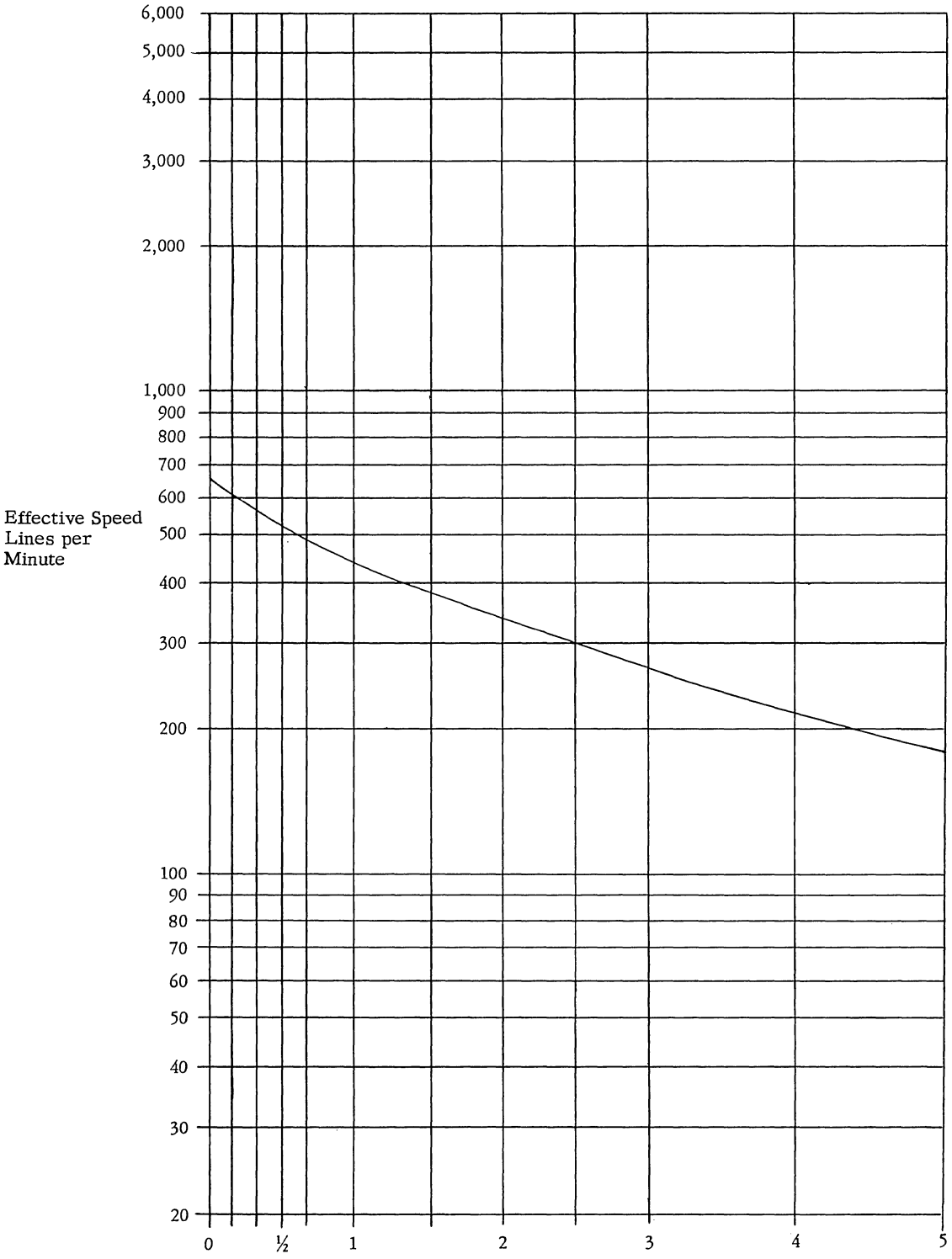
.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Reading:	none.	
Input area overflow:	not possible.	
Output block size:	fixed.	
Invalid code:	check	set indicator.
Exhausted medium:	see "Off Normal".	
Imperfect medium:	none.	
Timing conflicts:	interlock	wait.
Off Normal*:	check	set indicator.

*Off Normal: includes: . . . . . paper feed check.
equipment malfunction.

§ 081.

EFFECTIVE SPEED
(Unit No. 7912)



INPUT-OUTPUT: CARD PUNCH PRINTER

§ 082.

.1 GENERAL

.11 Identity: . . . . . Card Punching Printer. Unit No. 7911.

.12 Description

This is an 80-column card unit designed not only to punch cards but also to print data on them, independently of their punching. The unit consists of a single card track from the hopper to the stacker which is divided into two parts. The first part starts at the hopper and passes a punch station and a read station; then there is a gate between the two parts. The second part passes two printing stations, one for each face of a card, and ends at the stacker. The movements of cards along both parts are independently controlled by instructions. If one card attempts to overtake another, an interlock stops the unit.

The unit has a single point clutch in the first part and moves one card at a time. In the second part, it moves in multiples of one-line spacings. The speed of operation with no printing is 150 cards per minute, but it drops as many lines are printed. Peak printing speed is 900 lines per station per minute.

Up to 13 lines of print can be placed on each face of each card. The lines interleave with the punch rows. Each line has 70 printing positions. A full alphameric set of 40 engraved characters is available.

The unit can also handle restricted column post cards.

Separate instructions are used to:

a) punch one card and read the previous card.
b) print one line on the face of one card and another on the back of another card if they are present at the printing stations.

This unit uses the buffer bands that are also used by the High Speed Printer and Read Punch, and cannot be operated simultaneously with them if it is using their buffer bands.

.13 Availability: . . . . . no longer available.

.14 First Delivery: . . . . August, 1959.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . die punch and on the fly hammer stroke against engraved drum.
.222 Sensing system: . . . . brush.
.223 Common system: . . . none.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station:	wait.
Stacks:	0.
Heads/stack:	0.
Method of use:	none.

Use of station:	punch.
Distance:	1 card.
Stacks:	1.
Heads/stack:	80.
Method of use:	row at a time.

Use of station:	wait.
Distance:	1 card.
Stacks:	0.
Heads/stack:	0.
Method of use:	none.

Use of station:	read-verify.
Distance:	1 card.
Stacks:	1.
Heads/stack:	80.
Method of use:	row at a time.

Use of station:	wait.
Distance:	1 card.
Stacks:	0.
Heads/stack:	0.
Method of use:	none.

Use of station:	print one side.
Distance:	6 card rows.
Stacks:	1.
Heads/stack:	70.
Method of use:	row at a time.

Use of station:	print other side.
Distance:	23 card rows.
Stacks:	1.
Heads/stack:	70.
Method of use:	row at a time.

.25 Range of Symbols

Numerals:	10	0 - 9.
Letters:	26	A - Z.
Special:	4	. * & /
Alternatives:		none.
FORTRAN set:		no.
Basic COBOL set: . . .		no.
Total:	40.	

§ 082.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . card.
.312 Phenomenon: . . . . . punched holes and printing.

.32 Positional Arrangement: Punch section Print section

.321 Serial by: . . . . . row (1 of 12) row (1 of 13).
.322 Parallel by: . . . . . column (80) column (70).

.33 Coding: . . . . . Punch: Hollerith, binary, and column binary.
Print: 40 characters in standard six bit code.

.34 Format Compatibility

Other device or system	Code translation
Any 80-column equipment:	none if Hollerith code used.

.35 Physical Dimensions: . standard post or punch card.

.4 CONTROLLER

.41 Identity: . . . . . uses buffer bands in the Central Processor normally used by the Read Punch and High Speed printers.

.42 Connection to System

.421 On-line: . . . . . 1 max.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 max.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

	Printer	Punch
.441 Size of load:	2 line image	2 card images.
.442 Input-output areas: . .	1 buffer band	1 buffer band.
.443 Input-output area access:	buffer	buffer.
.444 Input-output area lockout:	when printing	when buffer is being loaded.
.445 Table control:	none	none.
.446 Synchronization:	automatic	automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 80-column punching.
2 lines of printing.

.512 Block demarcation
Input: . . . . . fixed.
Output: . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . 1 card.
.522 Output: . . . . . 1 card punched or 2 lines printed.
.523 Stepping: . . . . . 0 - 48 card rows in printing station.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . automatic.

.54 Format Control: . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . no.
Offset card: . . . . . no.
Select stacker: . . . . . yes.
Select format: . . . . . no.
Select code: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . no.
Busy device: . . . . . no.
Output lock: . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: no.
Off Normal*: . . . . . yes.
*Off Normal includes: . equipment malfunction.
stacker full.
hopper empty.
punch chip box full.
print error.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 150 cards/minute.
.622 Important parameters

Name	Value
Punch cycle:	400 m. sec (for other parameters, see Punch).
Feed printed card: . .	20 m. sec.
Advance and print 2 lines:	67 m. sec.
Advance additional lines:	9 m. sec each.

.623 Overhead: . . . . . 1 clutch point in punch section.

.624 Effective speeds: . . . The minimum of 150 or 60,000/(250 + 58P) cpm.
P = average number of lines printed on the side of the card with the most printing on it (13 max).

§ 082.

.63 Demands on System

Component	Condition	m.sec per card		Percentage
Central Processor:	load buffer to punch	3.5	or	0.9
	unload buffer from punch	3.5	or	0.9
	load buffer to print	10.1 to 262.6	or	2.5 to 14.2.
	verify punch images	3.5	or	0.9
	arrange print to punch	8.0 to 208.0	or	2.0 to 11.2.

Note: The following operations are performed by routines previous to the actual punching and printing operations when needed: compare, verify, and punch images, and arrange into print interleaved patterns.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Computation:	2 buttons	starts and stops processor.
Clear:	1 button	resets interlocks.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	1,000 cards.
Stackers (3):	1,000 cards each.

.732 Replenishment time: . . 0.5 to 2.0 mins. no need to be stopped.

.733 Adjustment time: . . . 1 to 2 mins.

.734 Optimum reloading period: . . . . . 6.7 mins.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	see "Off Normal".	
Reading:	none.	
Input area overflow:	not possible.	
Output block size:	not possible.	
Invalid code:	Check	set indicator.
Exhausted medium:	see "Off Normal".	
Imperfect medium:	none.	
Timing conflicts:	interlocks	wait.
Off Normal*:	check	set indicator.

* Off Normal includes: . . . . . equipment malfunction.
exhausted medium.
stacker full.
hopper empty.
punch chip box full.
print error.

INPUT-OUTPUT: UNISERVO MAGNETIC TAPE UNIT

§ 091.

.1 GENERAL

.11 Identity: . . . . . Uniservo Magnetic Tape Unit.
Type No. 7915.

.12 Description

The UNIVAC Solid-State system normally reads 1,100-alphameric-character blocks at an effective rate of 16,400 characters per second. (This block length is related to a band on the UNIVAC Solid-State drum, but other block lengths are possible to provide compatability with other UNIVAC systems.)

Internally, the system uses four-bit characters, but the magnetic tape characters are 6-bits. The difference is resolved by:

(1) Upon Reading: Using two 4-bit storage characters per 6-bit tape character read.

(2) Upon Writing: Recording on magentic tape only six bits out of each two 4-bit characters.

Some format problems result but the effective transmission rate is not reduced.

The tape is buffered into and out of the unit with an overlap of 95 percent of the elapsed time between the central processor and tape transmission. The tape buffer can also be used to move 200-word bands from one part of storage to another if no tape transmission is in progress.

The Uniservo II tape unit can be used in a variety of ways in which the tape material, packing density, block size and amplifier gain can be varied. They are used in conjunction with Synchronizers. There can be up to two Synchronizers, each of which may have up to 10 tape units connected to it. One Synchronizer may also serve any RANDEX system attached. The address of each unit can be chosen by a patch panel on its Synchronizer.

The recording can be made on metal or Mylar tapes and is compatible with UNIVAC I, II & III, File Computer, 490 and 1107. There is a special translate instruction for data in XS-3 code.

A second station is used to read-back tape and check the row parity, setting an indicator when a check fails. Three levels of amplification can be used when reading: low, normal, and high. Conventional practice is for the operator to read low to minimize noise; then, if difficulties arise, switch to normal or high on the Synchronizer.

.12 Description (Contd.)

The program can also switch the level, but the operator can override its choice upward.

Extra protection is provided to the tape and head both electrostatically and mechanically by a plastic guard interposed between the tape and the heads.

A write lock-out is obtained by inserting a ring in a reel.

Only tapes that have been edited to mark the flaws should be used. Tapes are edited by first recording a pattern of "all ones" along the tape and then reading and checking. When errors occur while using metallic tape, a special hand punch is used to perforate the tape in that area. When Mylar tape is used and errors occur, its oxide is manually scraped off, leaving a clear spot on the tape. The clear spots indicate the start and end of the flaw. This operation requires at least two passes through the tape plus manual punching time.

.13 Availability: . . . . . 7 months.

.14 First Delivery: . . . . . May, 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . . pinch roller.
.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum.
Capacity: . . . . . 6 feet of tape.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by a magnetic write head.
.222 Sensing system: . . . . . magnetic read head.
.223 Common system: common magnetic read/write head.

.23 Multiple Copies: . . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: 8
Method of use: . . . . . all tracks

Use of station: . . . . . read/write
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . . all tracks read or write.

§ 091.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . metal or plastic tape.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . 1,100 or 720 or 120 frames at 125 or 250 per inch.
.322 Parallel by: . . . . . 8 tracks.
.323 Bands: . . . . . 1.
.324 Track use
Data: . . . . . 6 bits per character.
Redundancy check: . . . 1 parity.
Timing: . . . . . 1 clock
Control signals: . . . . 0.
Unused: . . . . . 0.
Total: . . . . . 8.
.325 Row use
Data: . . . . . 1,100 or 720 or 120.
Redundancy check: . . . 0.
Timing: . . . . . 0.
Control signals: . . . . 0.
Gap: . . . . . see .622.

.33 Coding: . . . . . SS 80/90 six-bit or UNIVAC XS-3.

.34 Format Compatibility

Other device or system	Code translation
Univac I II III:	XS-3 translate instruction in 80/90.
Univac High Speed Printer:	special write instruction.
Univac 490, 1107: . . .	program translation to be handled by 490/1107.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.5 inch.
.352 Length
Plastic: . . . . . 2,400 ft.
Metal: . . . . . 1,500 ft.

.4 CONTROLLER

.41 Identity: . . . . . Synchronizer. Type No. 7914.

.42 Connection to System

.421 On-line: . . . . . 1 max.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 10.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1,100 or 720 or 120 characters.
.442 Input-output areas: . . . buffer band of 200 words.
.443 Input-output area access: . . . . . band.
.444 Input-output area lockout: . . . . . yes, and testable.
.445 Table control: . . . . . no.
.446 Synchronization: . . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1,100 or 720 or 120 characters.
.512 Block demarcation
Input: . . . . . fixed.
Output: . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . minimum 720 characters (Could be six 120-character blocks with gap as delimiter).
.522 Output: . . . . . 1,100 or 720 or 120. character block, forward only.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . automatic over pre-edited marked flaws.
.525 Marking: . . . . . holes punched in tape indicate beginning and flaws.
.526 Searching: . . . . . none.

.53 Code Translation: . . . . program

.54 Format Control:
Control: . . . . . program
Format alternatives: . . none.
Rearrangement: . . . . . none.
Suppress zeros: . . . . . none.
Insert Point: . . . . . none.
Insert spaces: . . . . . none.
Recording density: . . . yes.
Section sizes: . . . . . yes.

.55 Control Operations
Disable: . . . . . yes.
Request interrupt: . . . no.
Select format: . . . . . no.
Select code: . . . . . XS3 or SS 80/90.
Rewind: . . . . . yes.
Unload: . . . . . no.
Amplifier gain: . . . . . yes (3 levels).

.56 Testable Conditions
Disabled: . . . . . yes.
Busy device: . . . . . yes.
Output lock: . . . . . yes.
Nearly exhausted: . . . . no.
Busy controller: . . . . . yes.
End of medium marks: . no.
Error Type: . . . . . yes.

.6 PERFORMANCE

.61 Conditions

Case	Char/block	Char/inch
I:	1,100	250
II:	720	250
III:	1,100	125
IV:	720	125
V:	120	125

.62 Speeds

.621 Nominal or peak speed:

I:	25,000 char/sec.
II:	25,000 char/sec.
III:	12,500 char/sec.
IV:	12,500 char/sec.
V:	12,500 char/sec.

§ 091.

.622 Important parameters

Name	Value
Read start/stop 125 cpi:	18.3/16.3 msec.
Read start/stop 250 cpi:	12.1/9.2 msec.
Write start/stop 125 cpi:	18.8/17.8 msec.
Write start/stop 250 cpi:	12.0/11.1 msec.
Gap 125 cpi/250 cpi:	2.4/1.05 inches

.623 Overhead: . . . . . start/stop time

.624 Effective speeds: . . . .

I:	16,400 char/sec.
II.	13,600 char/sec.
III.	8,800 char/sec.
IV.	7,800 char/sec.
V.	2,600 char/sec.

.63 Demands on System

Component	Condition	msec per block		Percentage
Central Processor:	select unit	0.3	or	0.2 - 0.7
	load or unload buffer	3.5	or	2.6 - 7.6
	rewind	600.		

Note: When computation is to be performed on UNIVAC XS-3 coded information read from tape, the data must be converted to SS 80/90 code. Similarly, when preparing XS-3 coded information to write on tape, the inverse conversion must be programmed. The cost in either case is a subroutine which has an inside loop length of 3 instructions requiring no less than 0.2 millisecond per word using a translate instruction.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method
Metallic to Plastic:	switch

.72 Other Controls

Function	Form	Comment
Rewind:	button	rewinds tape.
Forward Backward:	2 button lights	forces direction.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel of Plastic tape:	2,400 ft. or 5,500,000 char or more at 250 pulses per inch.
Reel of Metal tape:	1,500 ft. or 2,000,000 char at 125 pulses per inch.

.732 Replenishment time: . . . 1 to 6 minutes. yes needs to be stopped.

.733 Adjustment time: . . . . . 0.5 to 1.0 minutes.

.734 Optimum reloading period: . . . . . 6.0 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	row parity	set indicator.
Reading:	row parity	set indicator.
Input area overflow:	not possible.	
Output block size:	not possible.	
Invalid code:	check	set indicator
Exhausted medium:	mechanical	turns off unit.
Imperfect medium:	interlock	wait (tape passes) set indicator.
Timing conflicts:	interlock	wait.
Noise in gap:	check	set indicator.
No sprocket pulse:	check	set indicator.

SIMULTANEOUS OPERATIONS

§ 111.

The basic Model I system consists of a central processor with almost totally buffered input and output facilities, except for the limitation of only one magnetic tape operating at any given time. The buffering would be complete except that it takes time to actually transfer the data block from the drum buffer bands to the main drum storage area.

This transfer of a data block takes one drum revolution (3.4 milliseconds) per transfer, except for transfers to the print buffer band, which take three revolutions per transfer. The extent to which the peripheral units are used determines the load on the central processor. When all units of a card system are working, the central processor penalty is less than 15 percent; for a tape system the delay is still less than 20 percent.

This simultaneity between all peripheral units and the computer applies only to a basic system which has no RANDEX Drum. This uses the buffers otherwise allocated to the tape units. Thus, there can be no simultaneity between reading or writing the RANDEX Units and the Magnetic Tapes.

Tables

The following operations can progress simultaneously:

Processing.
Reading a card by means of High Speed Card Reader.
Reading paper tape.
Punching paper tape.
Printing a line.
Reading and/or punching a card by means of the Read-Punch Unit.
Reading or writing of a block of tape or a block from RANDEX.
Reposition any RANDEX heads not otherwise in use.
Rewinding any tape units, not otherwise in use.

§ 121.

INSTRUCTION LIST

INSTRUCTION				OPERATION
OPERATION				
ABSOLUTE	X-6 or S-4	M	C	
				ARITHMETIC
70	ADD	M	C	(M) + (rA) ⟶ (rA)
75	SUB	M	C	(rA) - (M) ⟶ (rA)
85	MUL	M	C	(rL) x (M) ⟶ (rA)
55	DIV	M	C	(M) ÷ (rL) ⟶ (rA)
				LOGIC
20	BUF	M	C	(rA) "OR" (M) ⟶ (rA)
35	ERS	M	C	(rA) "AND" (M) ⟶ (rA)
32	SHR	onoo	C	Shift (rA) and (rX) right, circular
37	SHL	onoo	C	Shift (rA) left Zero ⟶ rA LSD
62	ZUP	-	C	Zero and comma suppress (rA)
00	JMP	M	C	Jump
67	HLT	M	C	Halt, go to M or C depending on start button pushed
82	TEQ	M	C	Compare (rA) to (rL); if =, go to M; if ≠ , go to C
87	TGR	M	C	Compare (rA) to (rL); if =, go to M; if ≠, go to C
82*	TEA	M	C	Compare (rA + bits 1 & 2 of rX); to (rL + bits 4 & 5 of rX); if =, go to M; if ≠ , go to C.
87*	TGA	M	C	Compare (rA + bits 1 & 2 or rX) to (rL + bits 4 & 5 of rX); if = , go to M; if ≠ , go to C
				* Bit is sign digit set (Model II only)
				MISCELLANEOUS INTERNAL
02	LIR	M	C	M ⟶ Index Register
07	IIR	M	C	M + (Index Register) ⟶ (Index Register), and m of (rA) Zeros ⟶ balance of rA
12	CTM	-	C	Translate card to computer code
17	MTC	-	C	Translate computer to card code
C3	MTX	M	C	Translate XS-3 to computer code
C1	XTM	M	C	Translate computer to XS-3 code
				DATA TRANSFER
25	LDA	M	C	(M) ⟶ (rA)
60	STA	M	C	(rA) ⟶ (M)
05	LDX	M	C	(M) ⟶ (rX)
65	STX	M	C	(rX) ⟶ (M)
30	LDL	M	C	(M) ⟶ (rL)
50	STL	M	CQ	(rL) ⟶ (A)
77	ATL	-	C	(rA) ⟶ (rL)
26	CLA	M	C**	0 ⟶ (rA)
31	CLL	M	C**	0 ⟶ (rL)
06	CLX	M	C**	0 ⟶ (rX)
36	CAA	M	C**	0 ⟶ (rA), save sign
86	CAX	M	-	0 ⟶ (rA), and (rX)

§ 121.

INSTRUCTION LIST–Contd.

INSTRUCTION				OPERATION
OPERATION				
ABSOLUTE	X-6 or S-4	M	C	
23	CTA	M	-	(rC) ⟶ (rA)
90*	SML	M	C	M.S.D. of (M) ⟶ Sign of (rL)
F0*	SMA	M	C	Sign of (M) ⟶ M.S.D. of (rA)
B8*	TCD	M	C	1 to 200 words of Core ⟶ Drum
B0*	TDC	M	C	1 to 200 words of Drum ⟶ Core
05*	LSX	M	C	(Bits 1 & 2 of M) ⟶ (Bits of 4 & 5 of rX)
06*	ZSR	M	C**	0 ⟶ Subregisters 3 and 4 of rX; sign +.
				* Model II only
				CARD READ-PUNCH
81	RCC	aa00	C	Load punch buffer with binary image from band aa
81	RCC	aa01	C	Load punch buffer translating the band aa machine code to card image
46	RBU	aa00	C	Unload punch buffer transferring the binary image to band aa
46	RBU	aa01	C	Unload punch buffer translating to machine code into band aa
22	RBT	M	C	Test buffer; if loaded, go to M, (rC) ⟶ (rA); if not, go to C
57	RSS	-	C	Select Stacker
				HIGH SPEED READER
72	HCC	M	C	Feed Card; if interlocked, go to M & (rC) ⟶ (rA); if not, go to C
96	HBU	aa00	C	Unload buffer with binary image into band aa
96	HBU	aa01	C	Unload buffer translating to machine code into band aa
42	HBT	M	C	Test buffer; if loaded, go to M & (rC) ⟶ (rA); if not, go to C
47	HSS	0a00	C	Select stacker a
				HIGH SPEED PRINTER
11	PRN	aann	C	Feed nn lines loading the print buffer from band aa
16	PFD	00nn	C	Feed nn lines
27	PBT	M	C	Test printer; if free, go to M, (rC) ⟶ (rA); if not, go to C
				MAGNETIC TAPE
C2	TST	M	C	Synchronizer test; if free, go to M & (rC) ⟶ (rA); if not, go to C
C6	TBL	aa00	C	Load tape buffer from band aa (Drum)
C7	TBT	M	C	Buffer Test; if free, go to M & (rC) ⟶ (rA); if not, go to C
F2	TRW	0a00	C	Rewind tape a
F2	TRW	0a20	C	Rewind and disable tape a
F6	TBU	aa00	C	Transfer contents of tape buffer to band aa
G2	TRD	0abc	C	Read block from tape a, mode and density b, direction and gain C
H2	TWR	0ab0	C	Write block on tape a, mode and density b
C6	TBL	BXXX	C	Load tape buffer from core, where BXXX is beginning word address
FX	TLB	BXXX	C	Transfer contents of tape buffer to core address BXXX. BXXX is beginning word address (core)

** If next instruction is to be found in core, then "M" and "C" must be same address.

§ 121.

INSTRUCTION LIST–Contd.

INSTRUCTION				OPERATION
OPERATION				
ABSOLUTE	X-6 or S-4	M	C	
				RANDEX
40	LSR	M	C	Load Synchronizer Instruction Register
18	PDH	M	C	Position Head
92	DBT	M	C	Test HPFF, if set go to M; if not, go to C
43	DPT	M	C	Test head position; if positioned, set HPFF
28	DWT	M	C	Write a record
38	DRD	M	C	Read a record
48	DWC	M	C	Write and check a record
58	DSW	M	C	Find record and write
68	DSR	M	C	Find record and read
F6	TBU	aa00	C	Transfer contents of tape buffer to band aa
C6	TBL	aa00	C	Transfer contents of band aa to tape buffer
C7	TBT	M	C	Test Tape buffer: if free, rC ⟶ rA and go to M; if not, go to C
C2	TST	M	C	Test Synchronizer: if free, rC ⟶ rA and go to M; if not, go to C
				N. B. 1. There are 4 special registers: rA: Accumulator rC: Command (complete instruction) rL: Lower accumulator rX: Used for comparisons and code conversions 2. Next instruction specified by C unless otherwise stated.

CODING SPECIMEN: X - 6

§ 131.

.1 CODING SPECIMEN

SAMPLE LISTING

The following is a sample of the listing produced by X-6 which affords the programmer a detailed correlation of machine and X-6 code.

```
X6B90  OP   CD  LOCA OP MMMM CCCC K   A TAG  C   OP  M TAG C TAG   TP   CD     COMMENTS              071659   PAGE   2
       AAR   1                                                       7          ADDRESS ANALYSIS ROUTINE
       AAR   2 0200 50 4002  204     AAR1N      STL AAR5F AAR2N     8  0001    SET EXIT
       AAR   3 0204 31  207          AAR2N      CLL                 8  0002    REENTRY POINT CIRCLE 1
       AAR   4 0207 25 4009  211                LDA W   0 AAR3N     8  0003    PPPPPUUUUU
       AAR   5 0211 82  414  214     AAR3N      TEQ   19N    1N     8  0004    SWITCH 1 A SETTING  LDX AAR6N
       AAR   6 0414 50 4116  218       19N      STL W  13           8  0005    ZERO TO FN INDICATOR
       AAR   7 0218 30 4002  254                LDL AAR5F MAR1N     8  0006    GO TO MEMORY AVAILABILITY ROUTINE
       AAR   8 0214 05 4009  261        1N      LDX W   0           8  0007    PPPPPUUUUU
       AAR   9 0261 26  264                     CLA                 8  0008
       AAR  10 0264 32 0500  272                SHR  0500           8  0009
       AAR  11 0272 20    T  276                BUF    RX           8  0010    UUUUUPPPPP
       AAR  12 0276 35 4028  280                ERS K  29           8  0011    0000T0000T
       AAR  13 0280 30    K  284                LDL    RA           8  0012    0000U0000P
       AAR  14 0284 06  287                     CLX                 8  0013
       AAR  15 0287 32 0500  295                SHR  0500           8  0014
       AAR  16 0295 37 0500  303                SHL  0500           8  0015
       AAR  17 0303 12       306                CTM                 8  0016    0000D00000
       AAR  18 0306 17       309                MTC         47N     8  0017    RA IS 1111U1111 RX IS 0000P00000
       AAR  19 0509 32 0500  317       48N      SHR  0500           8  0018
       AAR  20 0317 37 0500  325                SHL  0500           8  0019
       AAR  21 0325 20    T  329                BUF    RX'          8  0020    0000U0000P
       AAR  22 0329 82  532  332                TEQ          6N     8  0021    IF NOT EQUAL DIGIT 5 IS ALPHA
       AAR  23 0532 25 4009  361                LDA W   0           8  0022    PPPPPUUUUU
       AAR  24 0361 35 4013  365                ERS K   8           8  0023    TTTTTT0000
       AAR  25 0365 37 0500  373                SHL  0500           8  0024    UNPRIMED PART OF DIGIT 1 D00000000000
```

CODING SPECIMEN: S-4

§ 132.

.1 TRANSLATOR LISTINGS

CD NO.	LOCA.	OP	MMMM	CCCC	S	SYM A	OP	IR	SYM M	SYM C	remarks
1			0000	4999			BLR		0000	4999	
2			0400	0700			BLA		0400	0700	
3	0400	25	0402	0404		RANGE	LDA		X		
4	0404	30	0406	0408			LDL		CCO7		
5	0408	87	0411	0611			TGR		OUT		
6	0611	82	0414	0614			TEQ		EQU		
7	0614	30	0416	0418			LDL		CCO5		
8	0418	87	0421	0621			LGR		IN		
9	0621	82	0414	0411			TEQ		EQU	OUT	
10	0416		00000	00005		CCO5				5	
11	0406		00000	00007		CCO7				7	
12	0414	67	0005	0414		EQU	HLT		0005	EQU	
13	0411	67	0006	0411		OUT	HLT		0006	OUT	
14	0421	67	0004	0421		IN	HLT		0004	IN	

Without Forward Search

1			0000	4999			BLR		0000	4999	
2			0400	0700			BLA		0400	0700	
3	0400	25	0402	0404		RANGE	LDA		X		
4							HED		B		
5	0404	30	0406	0408			LDL		CCO7		
6	0408	87	0424	0411			TGR		OUT		
7	0411	82	0624	0414			TEQ		EQU		
8	0414	30	0416	0418			LDL		CCO5		
9	0418	87	0421	0621			TGR		IN		
10	0621	82	0624	0424			TEQ		EQU	OUT	
11	0416		00000	00005		CCO5				5	
12	0406		00000	00007		CCO7				7	
13	0624	67	0005	0624		EQU	HLT		0005	EQU	
14	0424	67	0006	0424		OUT	HLT		0006	OUT	
15	0421	67	0004	0421		IN	HLT		0004	IN	

With Forward Search

The listings on the right show the symbolic coding; those on the left show the final machine coded program. The path of the program goes from RANGE to the three possible end-points IN, OUT, or EQUAL. Two of these, EQU and OUT, can be reached from two separate points in the program sequence.

When Forward search is not used, these are allocated as soon as the first point is reached, wasting a drum revolution each time the second path is taken. With Forward search, the allocation starts with the later path, and the delay is reduced to 13-word times (as against 187 in the former case).

DATA CODE TABLE NO. 1

§ 141.

.1 USE OF CODE: . . . . . internal and printer.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 6 bit (split between two words: Most significant = zone or unprimed. Least significant = numeric or primed).

.22 Character Structure

.221 More significant pattern: . . . . . 2 bits values for pattern 16, 32, 0, 0.

.222 Less significant pattern: . . . . . 4 bits values for pattern 1, 2, 4, 8.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MOST SIGNIFICANT PATTERN			
	0	16	32	48
0	0	NO PRINT		+
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	-	.	$	,
6	Space	:	*	%
7	)	&		
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H	Q	Y
12	9	I	R	Z
13	(			
14	;			
15	'	#		

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE: . . . . . XS3 use to communicate with other UNIVAC Machines.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 6 bit:
Most significant = zone or unprimed.
Least significant = numeric or unprime.

.22 Character Structure

.221 More significant pattern: . . . . . 2 bits: 16, 32.

.222 Less significant pattern: . . . . . 4 bits: 1, 2, 4, 8.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0				
1	Space	,	"	
2	-	.		:
3	0	;	)	+
4	1	A	J	/
5	Z	B	K	S
6	3	C	L	T
7	4	D	M	U
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H	Q	Y
12	9	I	R	Z
13	'	#		
14	&			
15	(			

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . . In reading or punching cards with non-standard punching.

.2 STRUCTURE OF CODES

80-Column

The 80-column punched card is represented in the computer as 24 words. Each group of 10 columns forms a data word of 3 images called the unprimed, primed and duo-primed images. Each image is a computer word and is an exact representation of the holes appearing on a particular section of the card - a punch equals a "1" bit. The signs of all images are positive.

Rows Y / X	Word 0 (10 4-bit chars)	Word 1 (10 4-bit chars)	Word 2 (10 4-bit chars)	Word 3 (10 4-bit chars)	Word 4 (10 4-bit chars)	Word 5 (10 4-bit chars)	Word 6 (10 4-bit chars)	Word 7 (10 4-bit chars)
0 1								
2 3 4 5	Word 0' (10 4-bit chars)	Word 1' (10 4-bit chars)	Word 2' (10 4-bit chars)	Word 3' (10 4-bit chars)	Word 4' (10 4-bit chars)	Word 5' (10 4-bit chars)	Word 6' (10 4-bit chars)	Word 7' (10 4-bit chars)
6 7 8 9	Word 0" (10 4-bit chars)	Word 1" (10 4-bit chars)	Word 2" (10 4-bit chars)	Word 3" (10 4-bit chars)	Word 4" (10 4-bit chars)	Word 5" (10 4-bit chars)	Word 6" (10 4-bit chars)	Word 7" (10 4-bit chars)
Columns	1-10	11-20	21-30	31-40	41-50	51-60	61-70	71-80

90-Column

The 90-column punched card is represented in the Central Processor as 20 words. Each group of 10 columns forms a data word of 2 images called the umprimed and the primed images or a word-pair. (Columns 41-45 and 86-90 are each treated as 10-column groups and are placed into the 5 least significant digit positions in the computer words.) Each image is a computer word and is an exact representation of the holes appearing on a particular section of the card - a punch equals a "1" bit. The signs of all images are positive.

Row					
0 1 3 5	0	1	2	3	4
7 9	0'	1'	2'	3'	4'
Columns	1-10	11-20	21-30	31-40	41-45
0 1 3 5	5	6	7	8	9
7 9	5'	6'	7'	8'	9'
Columns	46-55	56-65	66-75	76-85	86-90

§ 143.

.3 EXAMPLES (80-Column card)

Card Column		11	12	13	14	15	16	17	18	19	20
Alphabetic Character		K	L	M	N	O	P	Q	R	S	T
	Card Row										
10-digit Unprimed Word	Y	0	0	0	0	0	0	0	0	0	0
	X	1	1	1	1	1	1	1	1	0	0
	0	0	0	0	0	0	0	0	0	1	1
	1	0	0	0	0	0	0	0	0	0	0
10-digit Primed Word	2	1	0	0	0	0	0	0	0	1	0
	3	0	1	0	0	0	0	0	0	0	1
	4	0	0	1	0	0	0	0	0	0	0
	5	0	0	0	1	0	0	0	0	0	0
10-digit Duo-primed Word	6	0	0	0	0	1	0	0	0	0	0
	7	0	0	0	0	0	1	0	0	0	0
	8	0	0	0	0	0	0	1	0	0	0
	9	0	0	0	0	0	0	0	1	0	0

Note:

Holes would appear in the punched card wherever a "1" occurs in the above table.

In bi-quinary, the three words would be:

Unprimed word:

4 4 4 4 4 4 4 4 2 2

Primed word:

5 4 2 1 0 0 0 0 5 4

Duo-primed word:

0 0 0 0 5 4 2 1 0 0

DATA CODE TABLE NO. 4

§ 144.

.1 USE OF CODE: . . . . comparisons.

.2 NUMERIC CODE

(in ascending sequence)

0
1
2
3
4
Undigit A
Undigit B
Undigit C
5
6
7
8
9
Undigit F
Undigit G
Undigit H

.3 ALPHAMERIC CODE

(in ascending sequence)

0	A	J	/
1	B	K	S
2	C	L	T
3	D	M	U
4	.	$	,
-	:	*	%
Space	&	N	V
)	E	O	W
5	F	P	X
6	G	Q	Y
7	H	R	Z
8	I	+	
9	#		
(			
;			

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . none.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

SR 012
Reference: . . . . . SR012.
Record size: . . . . 1 to 100 words.
Block size: . . . . . 100 words.
Key size: . . . . . 1 to 12 words.
File size: . . . . . 4,800 block reel.
Number of tapes: . . 4 to 10.
Date available: . . . currently.
Description:

SR 012 accepts as input a file of 12-word items in the standard interlace from a tape written in USS mode. It produces as output the same items in sequence, in the standard interlace, on a tape written in USS mode. One full reel may be sorted at a time; however, the input data may appear on more than one tape. Both input and output tapes adhere to standard tape conventions (labels, sentinels, block counts, etc.).

Similar routines are available for 5, 10, 25, and 50 word items.

.14 Report Writing: . . . none.

.15 Data Transcription: . . a body of input-output routines are available which can be easily connected for data transcription purposes.

.16 File Maintenance: . . . none.

.17 Other

Program testing procedures, and a tape input-output system (Mascot II) are available. A series of mathematical function routines are available.

.2 PROBLEM ORIENTED LANGUAGES

A linear programming package is available.

PROCESS ORIENTED LANGUAGE

§ 161.

.1 GENERAL

.11 Identity: . . . . . Process Oriented Languages.
FLOW MATIC
COBOL
UNITRAN.

.12 Description

These systems have been announced at various times for one or more parts of the UNIVAC SS 80/90 series. They have now been withdrawn.

MACHINE ORIENTED LANGUAGE: X-6

§ 171.

.1 GENERAL

.11 Identity: . . . . . X-6.

.12 Origin: . . . . . UNIVAC Remington Rand.

.13 Reference: . . . . . UNIVAC Remington Rand.

.14 Description:

X-6 is a basic drum-storage oriented assembly system, which uses three-character mnemonic operation codes and permits the use of symbolic notation to identify the locations of data and instructions. The ratio of source statements is one to one.

This system uses 10 card types to define a source program. The majority of these types deal with storage reservation. Pseudo-operations included in the language are used for optimizing instruction and data placement where the assembler is not designed to handle automatically; e.g., short-length multiplication.

Library routines which have no parameters are inserted by reserving the locations that they require, then adding the preassembled routines to the object programs. Table and Input-Output area reservation is provided.

Library routines with parameters can be inserted by means of a mechanism for incorporating symbolic subroutines with substitution of actual symbols for variables used in the general routine.

.15 Publication Date: . . 1959.

.2 LANGUAGE FORMAT

.21 Diagram (see below)

.22 Legend

Card Type: . . . . . 1 of 10 which define the the kind of processing that the card will receive.
Operation No.: . . . . . designates a part of a program containing less than 1,000 statements.
Card No.: . . . . . indicates sequence of cards in a subsection.
normally not used. This space can be used to indicate the sequence of cards inserted between cards with adjacent card numbers. This, however, requires changing X-6 coding. If columns 9-10 are used without changing the coding, an error results.
a: . . . . . may be used to specify a label for the line or left blank.
Control: . . . . . specifies the configuration of the sign digit or whether the c and m field should be interpreted as zone or numeric data. Used to specify types of constants to be generated or number of the index register applicable to the line, if it is an instruction.
Instruction Code: . . specifies a 3-character mnemonic operation code or is left blank if contants are being written.
Blank: . . . . . no function.
m: . . . . . operand address.
c: . . . . . next instruction address.
m and c: . . . . . program constant.
Comments: may contain any information as this field does not affect the assembly.

.23 Corrections: . . . . no automatic procedures.

1 2	3 5	6 8	9 10	11 15	16	17 19	20	21 25	26 30	31 80
Card Type	Operation No.	Card No.	Blank	a	Control	Instruction Code	Blank	m	c	Comment

§171

.24 Special Conventions

.241 Compound addresses: . . none possible.
.242 Multi-addresses: . . . . none possible.
.243 Literals: . . . . . requires 1 line of coding generally.
.244 Special coded addresses: . . . . . none.

.3 LABELS

.31 General

.311 Maximum number of labels
Procedures: . . . . . 300 Universal & 50 Local per part (operation).
Constants: . . . . . 300 pooled (K label).
Files: . . . . . none.
Record: . . . . . reserved labels are available for 70 input-output areas.
Items: . . . . . none.
Work Area: . . . . . 300 (W label).
Tables: . . . . . 30, each with its own base and increment.
Input-Output Area: . . 70, interlaces can be used.
.312 Common label formation rule: no.
.313 Reserved labels
For A register: rAΔΔΔ
For R register: rRΔΔΔ
For X register: rXΔΔΔ
For next instruction or location . . . . blanks.
For interlaces . . . special rules.
.315 Designators
Constant: . . . . . initial K.
Working storage: . . . initial W.
.316 Synonyms permitted: . . yes.

.32 Universal Labels

.321 Labels for procedures
Existence: . . . . . mandatory if referred to elsewhere in program.
Formation rule
First character: . . . any.
Last character: . . . N, F, O or P.
Others: . . . . . any.
Number of characters: . . . . . 5.
.322 Labels for library routines: . . . . . same as procedures.
.323 Labels for constants
Existence: . . . . . not mandatory unless pooled.
Formation rule
First character: . . . K.
Last 3 characters: . . ΔΔ0 to 299.
Others: . . . . . Δ or 0.
Number of characters: 5
Others: . . . . . none.
.324 Labels for files: . . . . . none.
.325 Labels for records: . . . none.
.326 Labels for variables: . . may appear in any form listed here.
.327 Labels for Work Areas
Existence: . . . . . yes.
Formation rule
First character: . . . W.
Last 3 characters: . ΔΔ0 -299.
Others: . . . . . any, no effect.
Number of characters: . . . . . 5.
.328 Labels for Tables
Existence: . . . . . yes.
Formation rule
First character: . . S, U, V.
Others: . . . . . 0000 through 9999.
Number of characters: . . . . . 5.
.329 Labels for Input-Output Areas
Existence: . . . . . yes.
Formation rule
First character: . . . H, R, O, P, T, Z.
Second character: . . 0 - 9.
Third character: . . U, P, D, N, Z.
Fourth and fifth characters: . . . 00 - 99.

.33 Local Labels

.331 Region: . . . . . local to 1 part (operation) of a program.
.332 Labels for procedures
Existence: . . . . . mandatory if referred to in this operation.
Region: . . . . . local to operation.
Formation rule
First 2 characters: . blank.
Last character: . . . N, F, O or P.
Others: . . . . . any.
Number of characters: . . . . . 5.
.333 Labels for library routines
Existence: . . . . . same as procedures.
.334 Labels for constants
Existence: . . . . . same as procedures.
.335 Labels for files: . . . . . none.
.336 Labels for records: . . . none.
.337 Labels for variables: . . none.
.338 Labels for library parameters
Existence: . . . . . optional.
Formation rule
First character: . . . X.
Last 2 characters: . . Δ0 to 19.
Others: . . . . . blank
Number of characters: . . . . . 5.

.4 DATA

.41 Constants

.411 Maximum size constants
Integer
Decimal: . . . . . 10 digits.
Octal: . . . . . none.
Hexadecimal: . . . . . 10 digits.
Fixed numeric: . . . . none.
Floating numeric: . . . none.
Alphabetic: 10 digits for Zone and 10 digits for Underpunch.
Alphameric: same as alphabetic.

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.412 Maximum size literals
Integer
Decimal: . . . . . 10 digits.
Octal: . . . . . none.
Hexadecimal: . . . . . 10 digits.
Instructions: . . . . . 10 digits.
Fixed numeric: . . . . none.
Floating numeric: . . . none.
Alphabetic: . . . . . 10 digits for Zone and 10 digits for Underpunch.
Alphameric: . . . . . same as alphabetic.

.42 Working Areas

.421 Data layout
Implied by use: . . . . W label.
Specified in program: . yes.
.422 Data type: . . . . . implied.
.423 Redefinition: . . . . . no.

.43 Input-Output Areas

.431 Data layout: . . . . . layout within each band is peculiar to each peripheral device.
.432 Data type: . . . . . implied in format of symbolic address.
.433 Copy layout: . . . . . not necessary.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . . mandatory.
Number: . . . . . 50.
Example: . . . . . ADD.
Comment: . . . . . 3 Alpha Characters.
.512 Absolute: . . . . . none.

.52 Macro-Codes: . . . . . none.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control
Allocation counter: . . 6 pseudo operations.
Label adjustment: . . . card type 3.
Annotation: . . . . . card types 1, 7, 8, 9, 10.
.542 Allocation counter
Set to absolute: . . . . pseudo operation.
Set to label: . . . . . pseudo operation.
Step forward: . . . . . pseudo operation.
Step backward: . . . . pseudo operation.
Reserve area: . . . . card types 3, 4, 5.
.543 Label adjustment:
Set labels equal: . . . . none.
Set absolute value: card type 2.

.544 Annotation
Comment phrase: . . . card field.
Title phrase: . . . . . card type 1.

.6 SPECIAL ROUTINES
AVAILABLE: . . . . . none.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . none.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . . yes.
.723 Private: . . . . . generally.

.73 Storage Form: . . . . . cards.

.74 Varieties of Contents: . . depends on installation.

.75 Mechanism

.751 Insertion of new item: . . manual file in card library.
.752 Language of new item: . . X-6.
.753 Method of call: . . . . . cards inserted by programmer.

.76 Insertion in Program

.761 Open routines exist: . . . yes.
.762 Closed routines exist: . . yes.
.763 Open-closed is optional: no.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros: none.

.82 Pseudos

Code	Description
ADA:	Modify succeeding a and m addresses.
ADM:	Modify succeeding m and c addresses.
ADC:	Modify succeeding c address.
SEA:	Set succeeding a address.
SEM:	Set succeeding m address.
SEC:	Set succeeding c address relative to a symbolic address.

MACHINE ORIENTED LANGUAGE: S-4

§ 172.

.1 GENERAL

.11 Identity: . . . . . S-4.

.12 Origin: . . . . . UNIVAC Division.

.13 Reference: . . . . . S-4 Assembly, General Manual. UP - 1774-6, Revision 1. S-4 Assembly For 90 Card Configuration. UP-1774-7

.14 Description

The S-4 assembler is the standard assembler for UNIVAC Solid-State systems, Models I and II. S-4 is machine oriented, its decimal operands being arranged in 10-digit fixed point words exactly as in the normal machine instruction.

S-4 is an assembly language which produces one machine instruction for each symbolic instruction. However, S-4 contains a set of 20 controls which are independent of the machine language and provide various facilities at assembly time. An S-4 programmer can use these controls to relieve himself of the machine language coding problems. These facilities are of two types:

- Allocation Controls, which, while comprehensive, do not provide the same result as hand coding.
- Compatibility Controls.

Allocation Control

Model I systems use magnetic drums as basic storage and have a minimum of two levels of storage. Model II systems also have core stores, while a tape system uses the tape buffer. The efficiency of any program depends more on the allocation of operands to storage than on the actual instructions. A well-allocated add instruction (one optimized as to the number of word cycles that must elapse before the operand is available) takes 85 microseconds. At random drum positioning, this instruction takes 20 times as long, and in the worst case, it would take 80 times as long.

S-4 provides three levels of allocation control to the programmer: provisional, general, and by exception. At the first level, each label contains a character position which defines the label as being provisionally allocated to either normal or fast drum storage, or to core storage. In any part of a program, these provisional labels can be overridden (the second level of control). Thus, allocations coded for the normal drum access are forced into fast access, but the reverse is not true. The third control level is provided for situations in which the provisionally selected allocation cannot be made optimal. When this condition exists, the programmer has a choice of using a higher level store to attempt to obtain optimal allocation before accepting a non-optimal allocation.

.14 Description (Contd.)

Compatibility Controls

S-4 provides for compatibility with both actual programs and symbolic programs.

The compatibility with actual programs comes from the design of the Availability Table. This table is a storage map which indicates to the assembler which positions are available for allocation. At any time in the program, this allocation can be changed by reading in a new availability table. The change can be a complete or partial replacement of the availability table or the addition of reservations. Similarly, the whole table can be punched out as needed to allow for similar subsequent uses, permitting:

(1) Existing programs to have their own availability tables to be read in, and therefore reserved, prior to an assembly.

(2) Overlays to be created at any position in the assembly.

Symbolically, programs can be merged into assembly programs either by physically adding cards or by calling the programs to be added from a tape unit. The S-4 language itself is a simple representation of the standard machine instructions. Thus, ADD is the mnemonic used for 70, the addition machine code. Similar to the machine instruction, the S-4 representation must have a location, an operation code, an operand address, and a next instruction address. However, the programmer's job in keeping track of the addresses is eased by:

(1) Using blanks if the address is obvious and will not be referred to again.

(2) Using "Local Reference Points" (up to 20 can be operational at a given time) to denote points which are only of local importance; that is, normally within 20 to 50 lines of coding.

(3) Using Temporary Tags for all those labels which are only used within a segment of the program.

(4) Using specialized labels for each word of the input-output areas defined in the program, and for the registers.

(5) Using specialized tags for tables (up to 30 of these can be defined at any one point).

§ 172.

.15 Publication Date: . . . . 1962.

.2 LANGUAGE FORMAT

LINE	LINE NO.	SYMBOLIC "A"	OPERATION CL	OPERATION Symbolic	IR	SYMBOLIC "M"	SYMBOLIC "C"
	13 14 15 16	46 47 48 49 50	51	52 53 54	55	56 57 58 59 60	61 62 63 64 65

.22 Legend

LINE: . . . . . line of coding on the coding sheet.
LINE NO: . . . . . line number optionally allocated by programmer, always reallocated by the translator.
SYMBOLIC a: . . . . . location of the instruction in the store. May be in absolute or symbolic form.
OPERATION: . . . . . defines the type of constant which follows; or is the instruction in symbolic form.
IR: . . . . . Index Register Modification, if it is to be used.
SYMBOLIC m: . . . . . the address of an operand, in symbolic or absolute form.
SYMBOLIC c: . . . . . the address of the next instruction, in symbolic or absolute form.
SYMBOLIC m & c combined: . . . . . 10 digits, to be treated as an absolute constant.
WORD TIME: . . . . . 3 digit number which directs the compiler as to time to be allowed to the instruction.

.23 Corrections

Insertions, deletions, and corrections can be made by altering the original coding. Special pseudo operations are available in the language which make it unnecessary to do more than nominate what parts of a previous assembly should be omitted and require the programmer to provide only full details of any additions (including changes).

.24 Special Conventions

A number of conventions are used to simplify programming or assembly, which add considerably to the writing speed, ease of insertions, etc., in addition to readability.

BLANKS are used in the location, the operand and/or the next instruction addresses within each instruction when normal sequencing is desired.

Constants can be given in some simple form, with an additional instruction (a designator) as to what part of the given constant is wanted. These instructions include:

For I/O codes: Unprinted, printed, or double printed; numeric or zone portions.

.24 Special Conventions (Contd.)

For general use: Either the negative or the reciprocal of the given instruction.

.3 LABELS

.31 General

Labels are used in S-4 to define parts of a program and units of the computer. In general, five alphameric characters are used to provide a label, and the fact that specific positions either are or are not numeric, distinguishes one type of label from another. Position of characters in label fields is critical.

.32 Universal Labels

.321 Labels for instructions
Existence: . . . . . optional.
Formation rule
First character: . . must not be numeric.
Last character: . . . designating type of storage, i.e., fast or normal drum or core) for provisional allocation or overflow control.
Others: . . . . . alphameric.
Number of characters: . . . . 5.

.323 Labels for constants or variables: . . . . . same as instructions.

.324 Labels for files or records: . . . . . no; but there are labels reserved for I/O areas.

.327 Labels for regions and tables
Existence: . . . . . yes; i.e., A Δ Δ Δ Δ
Formation rule
First character: . . alphabetic character.
Others: . . . . . 0000 to 9200.
Number of characters: . . . . 1 label, 4 element.

.33 Local Labels

Temporary labels are used extensively in S-4. The three methods of writing them are:

(1) Local Reference Points, which are constantly redefined. These are numbered 1 through 9 and 0, and a reference applies to the nearest reference point in the indicated direction.

(2) Temporary Tags. These differ in formation from permanent tags (They have numerics in the center of the tag; e.g., B123N) and are all cleared at once from the symbol table by a control card.

(3) Permanent Tags. However, any permanent tag can be made local by clearing it from the symbol table, and then redefining it as the new value.

.333 Labels for library routines
Formation rule
First character: . . must not be numeric.
Last 2 characters: . designating type of storage for provisional allocation.
Others: . . . . . numeric.
Number of characters: . . . . 5.

§ 172.

.4 DATA

.41 Constants

.411 Maximum size constants or literals: . . . . . 10 hexadecimal or decimal digits or one part. 10 alphabetic characters (i.e., numeric or zone portion).

.42 Working Areas: . . . . compiled by use, or by definition as reserved or table areas.

.43 Input-Output Areas

.431 Data layout: . . . . . controlled by parameters preset for units connected to system.

.5 PROCEDURES

.51 Direct Operation Codes

All machine codes are given mnemonic codes, such as ADD, LDA (Load Register A). These, or their absolute equivalents, can be used interchangeably.

.52 Macro-Codes: . . . . . none.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control: . . . a large number of pseudo operation codes give direct control over the translator. In addition, the translator includes a load feature, which allows its own tables to be overwritten by new data in the middle of an assembly.

.542 Allocation counter
- Set to absolute: . . . . yes.
- Set to label: . . . . . yes.
- Step forward: . . . . . yes.
- Step backward: . . . . yes.
- Reserve area: . . . . yes.

.543 Label adjustment
- Set labels equal: . . . yes.
- Set absolute value: . . yes.
- Clear label table: . . yes, local, relative, and specific permanent labels can be cleared separately.

.544 Annotation
- Comment phrase: . . yes.
- Title phrase: . . . . . yes.

.545 Other

Allocation is handled by three methods.

(1) Explicitly. Each label is coded to indicate whether it should be placed in core storage, or onto the fast access or normal access portion of the drum.

(2) By policy statements which overrule the explicit statements. Special pseudo codes are available which cause the translator to allocate core store, or fast store to all subsequent labels despite the allocation instruction implicit in the actual label. (This is very helpful when utilizing subroutines.)

(3) By directing the translator to leave a specific amount (entered in the word time column on the coding sheet) of time between particular instructions. This provision overrules the amount of time which would be generally used for the specific instruction.

.6 SPECIAL ROUTINES AVAILABLE: . . . . . none in S-4 language.

.7 LIBRARY FACILITIES

Libraries can be created and held on magnetic tape. These libraries consist of regular S-4 programs, and are called in by naming the first and last statement number which is to be incorporated into the assembly and the tape unit where it is to be found. No program is named by these instructions, and it is the responsibility of the programmer to position the tapes correctly.

A special Constants Library facility is available during assembly. All library constants are read and their labels checked against the list of labels. If the label has been used previously in the program, the value of the constant is entered. If no such use has been made, no entries are created in the object program.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . . none.

.82 Pseudos

ASSEMBLY CONTROL PSEUDO OPERATION

- RST: . . . . . Initialize for Assembly.
- END: . . . . . End Card Output.

STORAGE ALLOCATION PSEUDO OPERATIONS

- BLR: . . . . . Block Reservation.
- BLA: . . . . . Block Availability.
- REG: . . . . . Regional Specifications, providing labels and revising space.
- INT: . . . . . Interlace Pattern Reserve, revising an I/O and providing labels.
- SYN: . . . . . Synonym.

ALLOCATION-CONTROL PSEUDO OPERATIONS

- HED B: . . . . . Initiate Forward Search.
- HED A: . . . . . End Forward Search.
- HED D: . . . . . Extend in High-Speed Memory.
- HED H: . . . . . Extend in Core Memory.
- HED E: . . . . . Terminate HED D and HED H Functions.
- HED F: . . . . . Assign High-Speed Storage.
- HED G: . . . . . Assign Core Storage.
- HED J: . . . . . High-Speed Tags to Core Storage.

§ 172.

.82 Pseudos (Contd.)

ALLOCATION-CONTROL PSEUDO OPERATIONS (Contd.)

HED N: . . . . . Cancel effect of HED F, G, and I.
HED Z: . . . . . Allocate in Normal Speed Storage. Execute in High Speed Storage.
HED Y: . . . . . Terminate HED Z Control.
WDT: . . . . . Word-Time Control.

TAG TABLE CONTROL PSEUDO OPERATIONS

EQU: . . . . . Equivalence.
HED C: . . . . . Clear Temporary Tag Table.

TAPE ASSEMBLY PSEUDO OPERATIONS

HED T: . . . . . Accept Tape Input, from indicated tape.

.82 Pseudos (Contd.)

TAPE ASSEMBLY PSEUDO OPERATIONS (Contd.)

HED I: . . . . . Rewind Input Servo, from indicated tape.
HED O: . . . . . Rewind Output Servo.

CONSTANT LIBRARY PSEUDO OPERATIONS

HED L: . . . . . Process Constant Library, inserting any constants which have been called.
HED K: . . . . . End Constant Library Processing.

PROGRAM TESTING PSEUDO OPERATIONS

HED X: . . . . . Printer Output.
HED M: . . . . . Tape Output.
HED P: . . . . . Resume Punch Output.
PPA: . . . . . Print and Punch the Availability Table.
PAT: . . . . . Print Availability Table.
SYP: . . . . . Print Symbol Table.

PROGRAM TRANSLATOR (X-6)

§ 181.

1 GENERAL

.11 Identity: . . . . . X-6.

.12 Description

The X-6 translator is a card-based assembler which first creates a storage map as determined by the input instructions and then allocates symbolic program cards. Each symbolic program card represents a single machine code instruction. Allocation is therefore far from optimal under normal circumstances. Also, although six pseudo codes are available to help optimization, a more usual method of optimizing is to look over the coding after assembly and rewrite any areas inefficiently allocated.

Translators are available which can run on any UNIVAC Solid-State system. Model I systems with 9,200-word drums and all Model II systems must use the S-4 assembly language if they wish to use storage areas beyond location 5000. Macro instructions cannot be used in the X-6 system.

.13 Originator: . . . . . Remington Rand UNIVAC.

.14 Maintainer: . . . . . Remington Rand UNIVAC.

.15 Availability: . . . . . currently available.

.2 INPUT

.21 Language

.211 Name: . . . . . X-6.
.212 Exemptions: . . . . . none.

.22 Form

.221 Input media: . . . . . punched card.
.222 Obligatory ordering: . . by 8 digit code.
.223 Obligatory grouping: . . Card Types 1 through 5 must come first and in order, the types 6 through 9 in as many batches as desired, and finally 1 type 10 card.

.23 Size Limitations

.231 Maximum number of source statements: . . 4,800.
.232 Maximum size source statements: . . . . . 1 card.
.233 Maximum number of data items: . . . . . 4,800.
.234 Others all: . . . . . 4,800.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . machine code.
.312 Language style: . . . . decimal words.
.313 Output media: . . . . . punch cards.

.32 Conventions

.321 Standard inclusions: . . none.

.33 Documentation

Subject	Provision
Source program: . . .	listing A.
Object program: . . .	listing A.
Storage map:	listing B optional.
Restart point list: . .	none.
Language errors: . .	listing A.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes: . . one pass assembler.

.42 Optional Modes

.421 Translate: . . . . . yes.
.422 Translate and run: . . . no.
.423 Check only: . . . . . no.
.424 Patching: . . . . . no.
.425 Up-dating: . . . . . no.

.43 Special Features

.431 Alter to check only: . . no.
.432 Fast unoptimized translate: . . . . . no.
.433 Short translate on restricted program: . . no.

.44 Bulk Translating: . . . no reloading.

.45 Program Diagnostics: . none.

.46 Translator Library

.461 Identity: . . . . . Univac Systems Routines Series.
.462 User restriction: . . . none.
.463 Form
Storage medium: . . . punched cards.
Organization: . . . . . machine code.
.464 Contents
Routines: . . . . . closed.
Functions: . . . . . yes.
Data Descriptions: . . none.
.465 Librarianship
Insertion: . . . . . manual.
Amendment: . . . . . manual.
Call Procedure: . . . manual.

§ 181.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511	Fixed overhead:	none.
.512	Space required for each input-output file: . . .	variable with peripheral unit 32 to 200 words.
.513	Approximate expansion of procedures:	1 to 1.

.52 Translation Time

.521	Normal translating: . .	approx. 70 to 80 statements per minute until allocation is difficult at which time assembly slows down to approx. 10 cards per minute.
.522	Checking only:	none.
.523	Unoptimized translating:	none.
.53	Optimizing Data: . . .	Pseudo-operations. (See X-6 language)
.54	Object Program Performance:.	input/output limited programs are not affected. Otherwise object programs take between 2 and 5 times longer to run their equivalent hand code programs.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611	Minimum configuration:	2,600-word drum SS 80/90. High Speed Reader. Read Punch. High Speed Printer.
.612	Larger configuration advantages:	more tables and labels can be used.

.62 Target Computer

.621	Minimum configuration:	Any Solid-State 80/90 with 2,600-word drum.
.622	Usable extra facilities:	magnetic tape.

.7 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Missing entries:	check	stop.
Unsequenced entries:	check	stop.
Duplicate names:	none.	
Improper format:	check	error listing.
Incomplete entries:	check	error listing.
Target computer overflow:	check	error listing.
Inconsistent program:	none.	
Symbol table exceeded:	check	error listing.
Assembly table overflow:	check	error listing.

.8 ALTERNATIVE TRANSLATORS: . . . . . none for X-6.

PROGRAM TRANSLATOR: S-4

§ 182.

.1 GENERAL

.11 Identity: . . . . . S-4 80 Card Assembly System.
S-4 80 Card-Tape-Core Assembly System.
S-4 90 Tape-Core Assembly System.

.12 Description

The most interesting factor about the S-4 Translator relates to the source card design. The input is keypunched into the second half of the card and is reproduced in the same relative position on output. During input, the first half of the card is ignored; however, the output object program is punched into it. As a result:

(1) The output deck contains a complete, up-dated record of machine code and symbolic code, in addition to comments. The output deck is therefore independent of the input deck, which can be discarded or dispersed to its original sources. Up-to-date documentation, particularly of new routines, is therefore much easier to obtain simply by listing the object program deck.

(2) As the actual input area of the card does not coincide with the input area of the other UNIVAC Solid State Assembly System, X-6, one card can hold a code in both languages. Thus, routines can be issued which are suitable for compilation by either the S-4 or the X-6 assembly.

The assembly time for the S-4 is computer-limited. Tape or card input-output can be used, and translation speeds of approximately 60 instructions per minute can be obtained under favorable circumstances. These speeds are drastically reduced when the drum is filling up. A single large assembly can require an hour.

The object program is "optimized" by using the first available location whenever a new allocation has to be made. Normally, this is done in a forward direction, which means that no other point is referenced. However, the method has three disadvantages:

(1) In a program relying heavily on subroutines, parts of the drum can become unnecessarily crowded, causing delays in other parts of the program because of latency.
(2) If a location is jumped to from a number of positions, it is "optimized" as relative to the first jump encountered, even if this results in nearly the worst possible latency time for all other entries (which often happens.)

.12 Description (Contd.)

(3) When two or more variables which are to be considered for allocation to a particular position are considered, space allocation is provided on a first come, first served basis. This allocation gives fair, but far from the best results.

The S-4 Translator includes "Forward Search," a facility which, if carefully used, can reduce the impact of the first two disadvantages just enumerated. This facility allocates space backwards from the next fixed point. This allocation tends to be random, relieves the overcrowding, and optimizes on the last of a series of exits. A group of a maximum of 10 instructions can be handled at any one time.

S-4 Translators differ according to the machines on which they are run, or basically according to the following characteristics:

- Whether 80-column or 90-column cards are used.
- Whether the system is the Model I or Model II.
- Whether the minimum drum size is 2,600, 5,000, or 8,800 words.
- Whether the system is a card or tape system.

It can be seen that there are 24 possible basic configurations, and it is not surprising that some of them have been omitted. What is surprising is that the Model II users, who have no other assembly system available, have a very restricted choice. Only two versions are available:

(1) If a user's drum capacity is less than 5,000 words; a specialized, restricted version of the language must be used.

(2) If a user's drum capacity is 5,000 words or more, the Model I 5,000-word drum version can be used, which means that during the compilation, programs can utilize only the 5,000-word drum, and can make no use of the core.

.13 Originator: . . . . . UNIVAC Division.

.14 Maintainer: . . . . . UNIVAC Division.

.15 Availability: . . . . . April, 1962.

.2 INPUT

.21 Language

.211 Name: . . . . . S-4.
.212 Exemptions: . . . . . variable for different versions.

§ 182.

.22 Form

.221 Input media: . . . . . punched cards. magnetic tape.
.222 Obligatory ordering: . program sequence.
.223 Obligatory grouping: . no.

.23 Size Limitations

.231 Maximum number of source and data statements: . . . . 1 per word available in store.
.232 Maximum size source statements: . . . . 1 card.

.3 OUTPUT

.31 Object Program (Contd.)

The output can be punched into cards (one card per instruction) or recorded on magnetic tape (one tape block per instruction).

.32 Conventions

It is assumed that specific loaders will be used to load the output deck.

.33 Documentation

The source and object programs are listed side-by-side, including indications of the errors.

Details of the symbol table and a storage map are provided by inserting the appropriate control cards.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes: . . one pass only through the source program is required.

.42 Optional Mode

.421 Translate: . . . . . yes.
.422 Translate and run: . . . no.
.423 Check only: . . . . . yes, by omitting punching the object program.
.424 Patching: . . . . . yes, Re-Set card inserted between decks automatically causes re-initialization.
.425 Updating: yes, as for patching.

.43 Special Features

.431 Alter to check only: . . yes, by halting output of object program.
.432 Fast translate, by omitting the Forward Search feature: . . . . yes.
.433 Short translate on restricted program: . no.

.44 Bulk Translating: . . . yes, Re-Set card inserted between decks automatically causes re-initialization.

.45 Program Diagnostics: . none can be inserted directly, but the object program can be made compatible with the standard diagnostic programs.

.46 Translator Library: . . none.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . normally 200 words for loader.
.513 Approximate expansion of procedures: . . . . 1-for-1 correspondence between input and output.

.52 Translation Time

	Instruction Per Minute	
	Card System	Tape System
.521 Normal translating, including FORWARD SEARCH:	20 down to 5	25 down to 10.
.522 Checking only:	100 down to 10	120 down to 10.
.523 Translating without FORWARD SEARCH:	70 down to 10	90 down to 10.

The number instruction per minute decreases as the store fills, therefore requiring that the tables be searched more before allocation can take place.

.53 Optimizing Data

The assembler allocates the nearest-to-optional location available whenever it comes to a previously unallocated symbol. This allocation is made under control of the programmer's general instructions as to which level of store should be used.

In estimating where such a location could be, the assembler uses either the maximum instruction times for the specific instruction or the time given with the instruction.

When FORWARD SEARCH is in progress, this allocation is finally made backwards, which tends to prevent uneven distribution of data around the drum, and prevents the loss of a cycle in some simple branch and rejoin operations. The effect of FORWARD SEARCH overall has not been determined and it is unlikely to lead to an improvement in running time of more than 20 percent.

.54 Object Program Performance

With full utilization of the 12 different control operations, FORWARD SEARCH, and of the Word Time column on the coding sheet, timing efficiency should approximate 90 per cent at the start of an assembly and drop to about 70 per cent when the store is nearly full.

With only simple coding, the efficiency factors are probably 75 per cent and 50 per cent under the same circumstances.

§ 182.

.54 Object Program Performance (Contd.)

The loss of efficiency, even in the best care, occurs because the assembler is unable to judge the comparative costs of and value of the allocation it makes, and therefore cannot juggle them around to obtain optional overall performance.

The object program requires no more space than machine code programmer's does.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: UNIVAC Solid-State Model I with 5,000 word drum (either SS 80 or SS 90 systems can be used).

.612 Larger configuration advantages:. . . . . magnetic tapes give faster compilation and better re-assembly and library facilities.

.62 Target Computer

.621 Minimum configuration: any UNIVAC Solid-State system.

.622 Usable extra facilities: card reader, card punch, and printer.
core storage for UNIVAC Solid-State II system.
RANDEX units.
Paper Tape units.

.7 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	none.	
Duplicate names:	none.	
Improper format:	various checks, to ensure apparently valid entry.	error rotation on output.
Incomplete entries:		
Target computer overflow:	check	fictitious entry placed in all positions.
Inconsistent program:	none	assembly continues.

OPERATING ENVIRONMENT

§ 191.

.1 GENERAL

.11 Identity: . . . . . no integrated system available.

.12 Description

No comprehensive supervisor system has been published or announced for the UNIVAC Solid-State Systems. The facilities described in this section must be covered by incorporating specific routines in each program.

Normally, one 200-word band on the drum is reserved for loaders, dumps, traces, etc., and is not used for the actual program.

.13 Availability: . . . . . presently available.

.14 Originator: . . . . . various.

.15 Maintainer: . . . . . UNIVAC Division of Sperry Rand.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Libraries: . . . . . can be held on cards and physically chosen, or held on tape and be loaded under control of the tape control system.

.212 Independent programs: loaded from card and tape.

.213 Data: . . . . . normally via card reader, possible via Read/Punch unit, or via tape.

.214 Master routines: . . . . as for independent programs.

.22 Library subroutines: can be inserted at translation time using the S-4 or X-6 library facilities, if they are written in the appropriate symbolic language; otherwise must be treated as independent programs.

.23 Loading Sequence: . . . manual sequencing of card decks or program tapes.

.3 HARDWARE ALLOCATION: . . . . as incorporated in user's program.

.4 RUNNING SUPERVISION: . . . . as incorporated in user's program.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . Instruction-by-instruction trace available, provided 1 complete 200-word band on the drum is reserved.

.512 Snapshots: . . . . . not available.

.52 Post Mortem: . . . . . available provided 1 complete 200-word band on the drum is reserved. (This band may be the same one used for loaders and for tracing).

.6 OPERATOR CONTROL: as incorporated in user's program.

.7 LOGGING: . . . . . as incorporated in user's program.

.8 PERFORMANCE

.81 System Requirements

.813 Reserved equipment: normally the first 200 words of the drum.

.82 System Overhead

.821 Loading time: . . . . . condensed card decks at 3,200 instructions or constants per minute.
Program tapes at 90,000 instructions per minute after the tape has been positioned.

UNIVAC SS 80/90 MODEL I
SYSTEM PERFORMANCE

UNIVAC SS 80/90 MODEL I SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 1									
Worksheet	Item		Configuration						Reference
			1		OTHERS				
1 INPUT-OUTPUT TIMES	Char/block	(File 1)	80		1,000				
	Records/block	K (File 1)	0.5		8				
	msec/block	File 1 = File 2	100/400		67				
		File 3	100		100				
		File 4	133		133				
	msec/switch	File 1 = File 2	---		---				4:200.112
		File 3	---		---				
		File 4	---		---				
	msec penalty	File 1 = File 2	3.4		3.4				
		File 3	3.4		3.4				
		File 4	10.2		10.2				
2 CENTRAL PROCESSOR TIMES	msec/block	a1	19.9		13.1				
	msec/record	a2	15.4		15.4				
	msec/detail	b6	7.0		7.0				4:200.1132
	msec/work	b5 + b9	31.4		31.4				
	msec/report	b7 + b8	43.0		43.0				
3 STANDARD PROBLEM A F = 1.0	msec for C. P. and dominant column.	a1	C. P. 19.9		13.1	Printer			
		a2 K	7.7		123.0				
		a3 K	40.7		651.0				
		File 1 Master In	3.4		3.4				4:200.114
		File 2 Master Out	3.4	400	3.4				
		File 3 Details	1.7		27.2				
		File 4 Reports	5.2		83.0	1,133.0			
		Total	82.0	400	904.1	1,133.0			
4 STANDARD PROBLEM A SPACE	Unit of measure	(10-digit words)							
		Std. routines	600		600				
		Fixed	200		200				
		3 (Blocks 1 to 23)	300		300				4:200.1151
		6 (Blocks 24 to 48)	240		240				
		Files	500		500				
		Working	100		100				
		Total	1,900		1,900				

SYSTEM PERFORMANCE

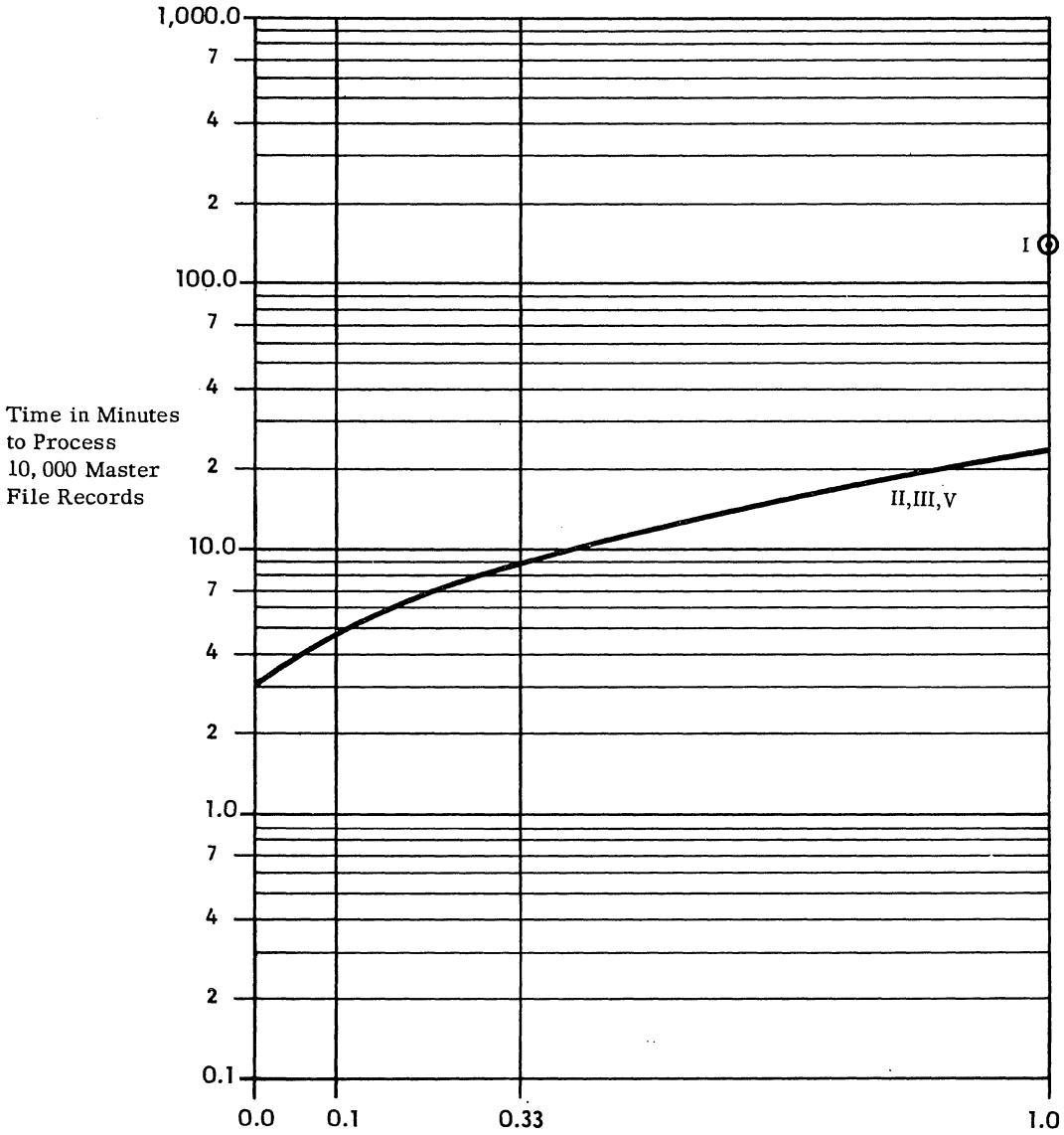
§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record Sizes
Master File: . . . . . 108 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.112 Computation: . . . . . standard.
.113 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.
.114 Graph: . . . . . see graph below.
.115 Storage Space Required . 1,900 words.

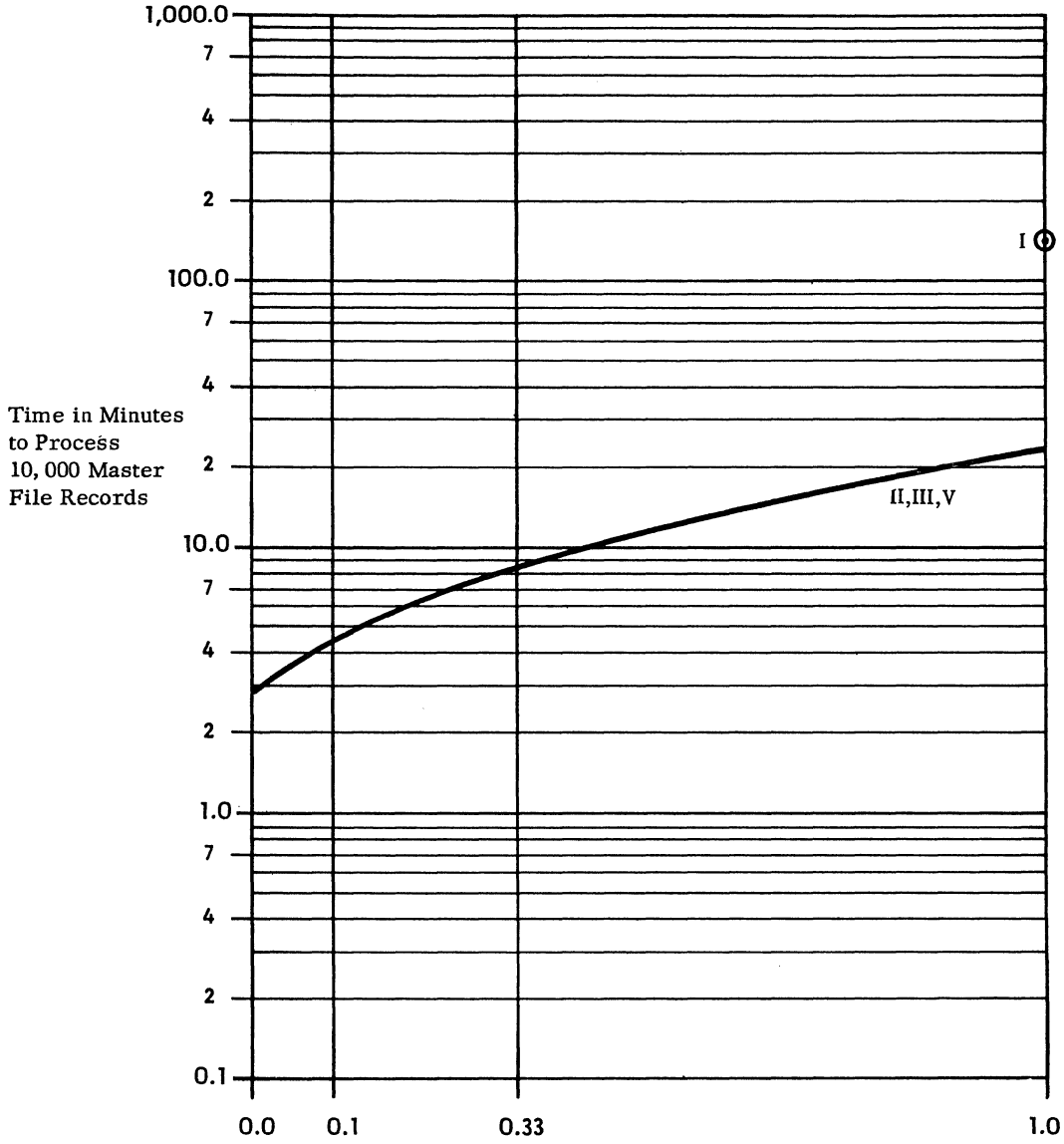


§ 201.

.12 Standard File Problem B

.121 Record Sizes
Master File: . . . . . 54 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.

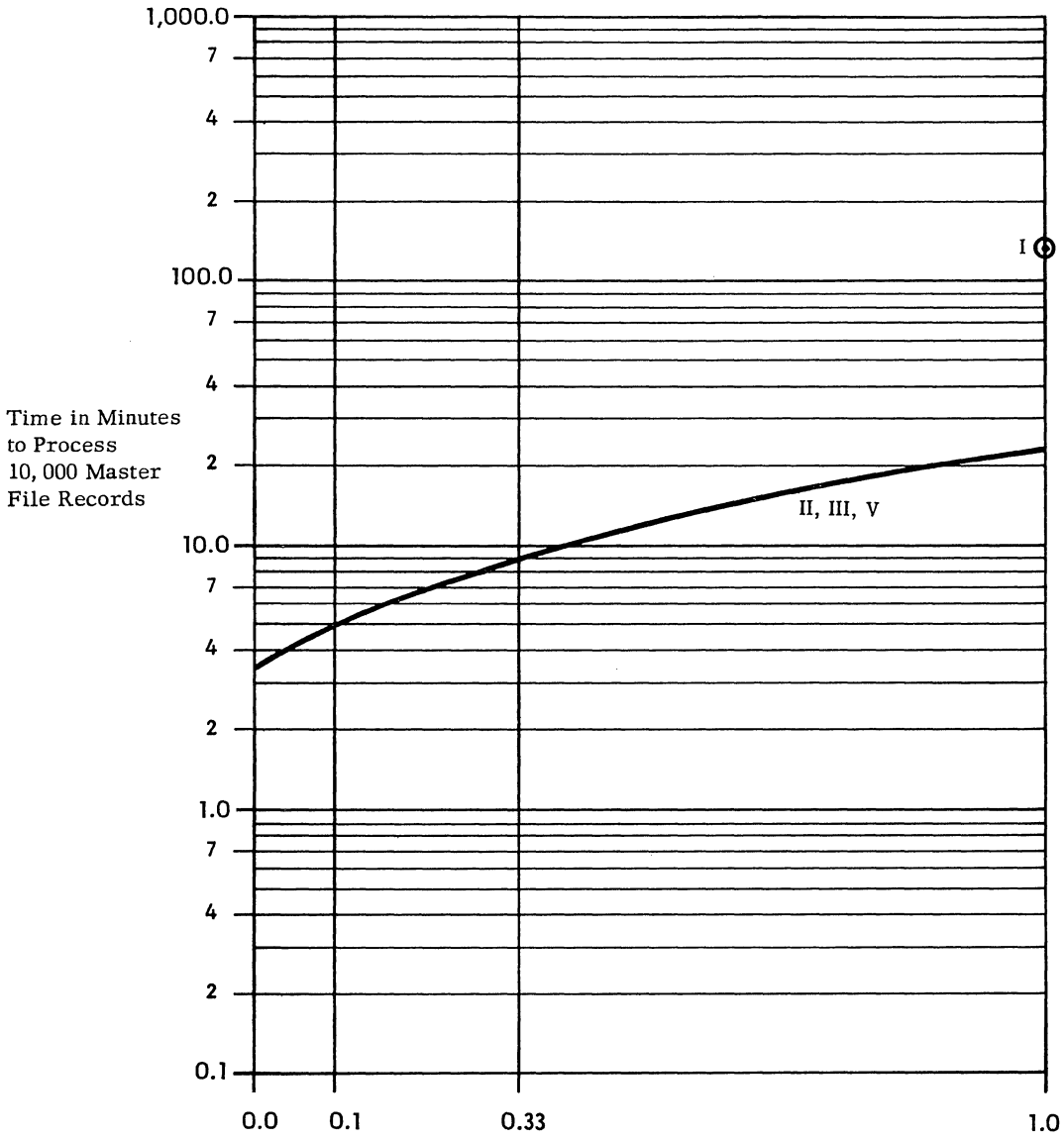


§ 201.

.13 Standard File Problem C

.131 Record Sizes
Master File: . . . . . 216 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13
.134 Graph: . . . . . see graph below.

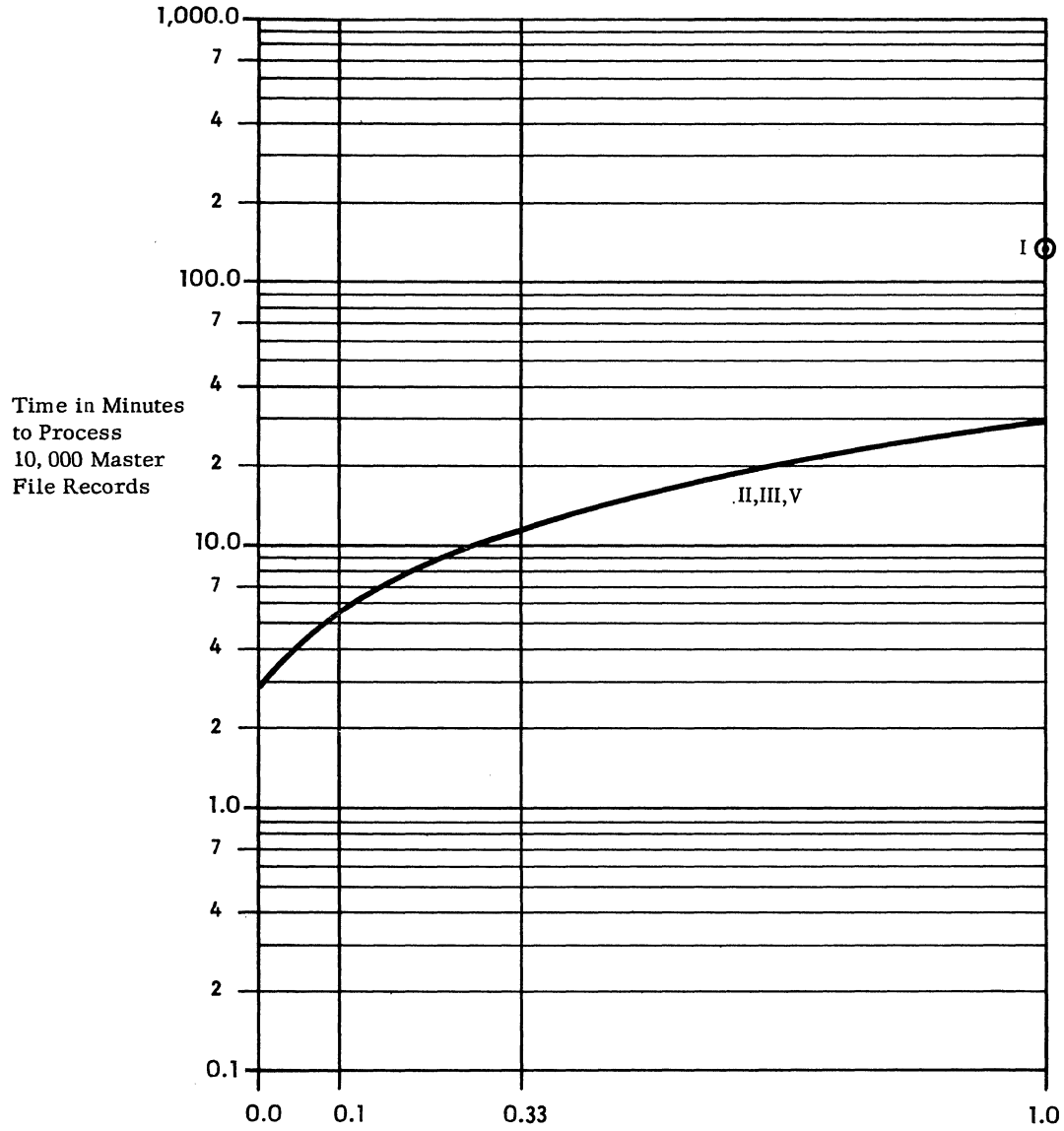


§ 201.

.14 Standard File Problem D

.141 Record Sizes
Master File: . . . . . 108 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



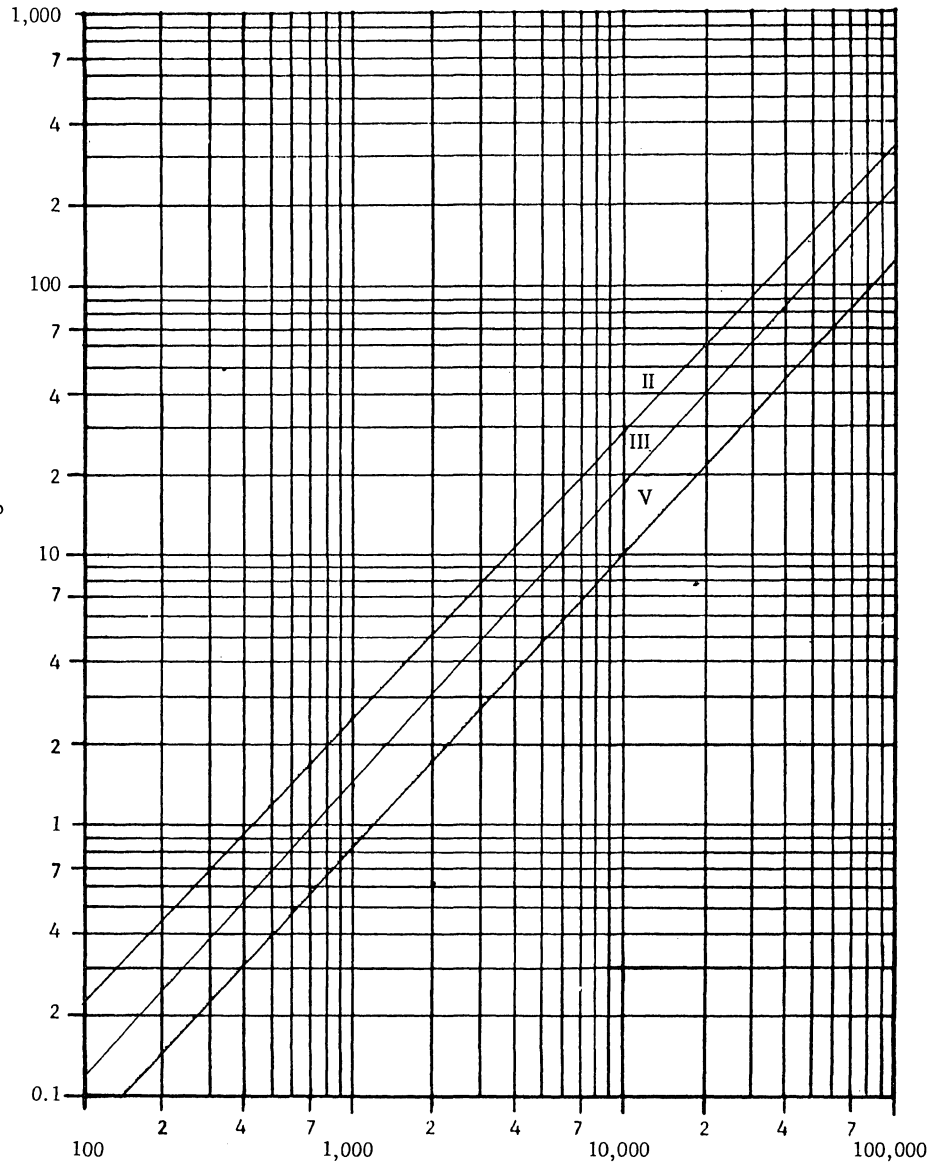
§ 201.

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.

.212 Key size: . . . . . 8 characters.
.213 Timing Basis: . . . . . as in 4:200.22.
.214 Graph: . . . . . see graph below.



Graph E. Number of Records

UNIVAC SS 80/90 MODEL I
PHYSICAL CHARACTERISTICS

UNIVAC SS 80/90 MODEL I PHYSICAL CHARACTERISTICS

IDENTITY	Unit Name		Central Processor	High Speed Printer	High Speed 80-Col. Reader	Card Read 80-Col. Punch Unit
	Model Number		SEE PRICES	7912	7935	7936
PHYSICAL	Height × width × depth, inches		69 × 108¼ × 32	53 × 72¼ × 32	48 × 50 × 24	54 × 49 × 27
	Weight, pounds		3,532	1,538	758	950
	Maximum cable lengths	Power Data	From CP	27' 3" 27' 1" To CP	25' 1" 24' 7" To CP	26' 11" 26' 3" 3 27' 0" Cables To CP
ATMOSPHERE	Storage Ranges	Temperature, °F.	← NOT AVAILABLE →			
		Humidity, %				
	Working Ranges	Temperature, °F.	60° – 85°	60° – 85°	60° – 85°	60° – 85°
		Humidity, %	30 – 70	30 – 70	30 – 70	30 – 70
	Heat dissipated, BTU/hr.		27,660	11,910	3,396	3,780
	Air flow, cfm.		2,100	550	200	200
ELECTRICAL	Voltage	Nominal	208 – 240	Contained in Central Processor		
		Tolerance	±10% into regulator	Contained in Central Processor		
	Cycles	Nominal	60	Contained in Central Processor		
		Tolerance	±0.5	Contained in Central Processor		
	Phases and lines		Single phase 3 wire	Contained in Central Processor		
	Load KVA		16.9	Contained in Central Processor		
NOTES	1. Maximum floor loading. 150 lbs./sq. ft.		2. For all equipment 90% Filtration per US Bureau of Standards. Dust Spot Discoloration Test.		3. Internal dust filters are provided.	

UNIVAC SS 80/90 MODEL I PHYSICAL CHARACTERISTICS (Contd.)

Uniservo II Magnetic Tape Unit	First Randex 24 Million Digits Unit	First Randex 12 Million Digits Unit	Additional Randex 24 Million Digits Unit	Synchronizer	Randex Power Control Unit
7915	7957	7965	7966	7914	
69 × 31 × 31	69 × 76 × 33	69 × 76 × 33	69 × 76 × 33	69 × 76 × 32	69 × 48 × 31
758	2,335	2,335	2,335	2,566	1,284
18' 10" 21' 5" To SYNC	Drum to Synchronizer 67 ft. maximum. Information not currently available To SYNC	To SYNC	To SYNC	22' 4" From CP	58 ft. to Synchronizer
←	NOT AVAILABLE				→
60° – 85°	60° – 85°	60° – 85°	60° – 85°	60° – 85°	60° – 85°
30 – 70	30 – 70	30 – 70	30 – 70	30 – 70	30 – 70
8,160	7,140	7,140	7,140	11,520 to 15,180	4,080
300	550	550	550	2,100	360
See Note 4				208 – 240	
See Note 4	FROM RANDEX POWER			±10% to regulator	±10%
	Information not currently			60	60
		available		±0.5	±0.5
	1ϕ 3 wire			1 or 3	1 or 3
2.7 each		2.4 KVA each		4.3 KVA	2.4 KVA per Drum
4. Contained in Synchronizer					

§ 221.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchases $
MODEL I STEP CENTRAL PROCESSOR	7944 7934 7947 7937	90-Column Card Only 80-Column Card Only 90-Column Card and Tape 80-Column Card and Tape			
		Standard Equipment: 2,400 Words 1.7 msec. average access store 200 Words 0.4 msec. average access store 3 Index Registers	1,735	350	110,000
		Options:			
		Program Interrupt	60	—	3,000
		Multiply and Divide	400	70	12,000
		200 Words of 0.4 msec. average access store (800 word max.).	275	20	10,250
		400 Words of 1.7 msec. average access store (1,600 word max.).	400	25	12,500
MODEL I STANDARD CENTRAL PROCESSOR	7907 7909 7933 7913	90-Column Card Only 80-Column Card Only 90-Column Card and Tape 80-Column Card and Tape			
		Standard Equipment: 4,000 Words 1.7 msec. average access store. 1,000 Words 0.4 msec. average access store. Multiply and Divide 3 Index Registers	4,835	600	213,000
		Options:			
		Program Interrupt	60	—	3,000
MODEL 1 EXPANDED CENTRAL PROCESSOR	7940 7930	90-Column Card and Tape 80-Column Card and Tape			
		Standard Equipment: 7,600 Words 1.7 msec. average access store 1,600 Words 0.4 msec. average access store Multiply and Divide 3 Index Registers	5,635	620	248,200
		Options:			
		Program Interrupt	60	—	3,000

§ 221. PRICE DATA (Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT	7945	600 cpm 90-Column Card Reader	255	55	11,200
		(or)			
	7935	600 cpm 80-Column Card Reader (1 max)	255	55	11,200
		Options:			
		Stacker Select	50	10	2,300
		80-Column Read Feature	35	18	1,350
		90-Column Read Feature	35	18	1,350
	7946	150 cpm 90-Column Read Punch	725	200	32,000
		(or)			
	7936	150 cpm 80-Column Read Punch (1 max)	725	200	32,000
		Options:			
		Preread (80- or 90-Column)	100	20	4,200
		Post read (80- or 90-Column)	100	20	4,200
		Stacker Select	50	10	2,300
	7914	Synchronizer (Tape and Randex) (2 max)	1,000	250	50,000
	7915	Uniservo II (max 10 per synchronizer)	450	112	20,000
		Paper Tape Reader	700	170	35,000
		Paper Tape Punch	100		5,000
		Options:			
		Spooling Feature	100	—	5,000
STORAGE	7965	RANDEX Unit (First) (max 1) 12 million digits	1,900	565	125,000
	7957	RANDEX Unit (First) (max 1) 24 millio digits	2,500	650	140,000
	7966	RANDEX Unit 24 million digits (Additional) (max 9)	1,900	195	85,000

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PRICE DATA (Contd.)

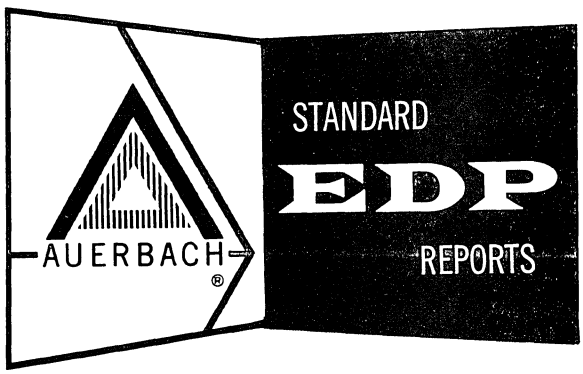
CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchases $
INPUT-OUTPUT	7914	Synchronizer (Tape and Randex) (1 max)	1,000	250	50,000
	7915	Uniservo II (max 10 per synchronizer)	450	112	20,000
		Paper Tape Reader	700	170	35,000
		Paper Tape Punch	100		5,000
		Options:			
		Spooling Feature	100	—	5,000
STORAGE	7965	RANDEX Unit (First) (max 1) 12 million digits	1,900	565	125,000
	7957	RANDEX Unit (First) (max 1) 24 million digits	2,500	650	140,000
	7966	RANDEX Unit 24 million digits (Additional) (max 9)	1,900	195	85,000

UNIVAC SS 80/90

MODEL II

Univac

(A Division of Sperry Rand Corporation)



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UNIVAC SS 80/90

MODEL II

Univac

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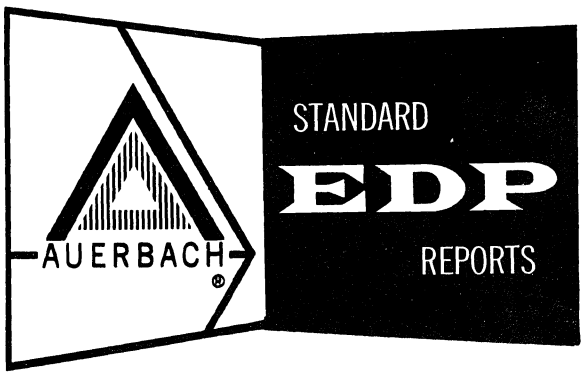

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INTRODUCTION

§ 011.

The UNIVAC Solid-State Model II computer system consists of a central processor with a drum store, a core store of 1,240 words (a word consists of 10-digits plus a sign), and buffered peripheral units. Standard peripherals include a 600 card per minute card reader, 150 card per minute read punch unit, 600 line per minute printer, and up to 20 tape units. RANDEX mass storage drums, paper tape equipment, etc., can all be added; however, inclusion of these units in a configuration is comparatively rare as yet.

The principle advantage of the Model II over the Model I is that a greater amount of internal processing can be performed in a given time than was the case with the Model I. Concurrently, the complexities of programming involved in getting an efficient input-output limited program working for the Model I have been greatly reduced in the Model II through the use of the core store, new instructions, and faster instruction execution for certain conditions. (See Central Processor, Section :051)

The Model II has a fixed word length of 10 digits plus a sign digit. Data not conforming to the word size exactly must be extracted by means of the logical and shift instructions, and isolated before being used. Similarly, data for output by printer or punch may have to be prepared by the reverse process. Alphameric data are considered as two numeric digits and held in separate words; therefore, all manipulations to isolate or pack such data must be repeated.

The UNIVAC Solid-State system originally was conceived as an integrated card system, with cards being read and punched, output being printed all at the same time, and the central processor powerful enough to keep up with this loading. The system has now been expanded by the addition of the tapes, but in many ways it is still card-oriented, using the tapes for large volume files. The tape format, when placed on the drum storage is awkward, owing to the different character representation (six-bit character rather than four-bit character).

The performance of the Model II is basically limited by the input-output speeds of its peripherals, all of which can operate in parallel with processing. Computation, however, can proceed at any speed up to 10 times faster than the Model I, and is frequently faster than on the IBM 1401. Applications which require several thousand words of storage (drum) and/or use a considerable amount of computation can be conveniently handled.

Model II processors can have from 2,600 to 8,800 words of drum storage. The Model II processor contains 9 index registers and 1,280 words of magnetic core storage as standard equipment. The Model II processor also has an expanded instruction complement which permits block transfer of words between core and drum, data packing, and easier programming of alphameric operations.

Both processors handle data in words which contain 10 digits plus a sign bit. Each digit has an odd parity bit associated with it. Parity is checked during all data movements to or from storage. Both alphameric and numeric data can be handled and comparisons made. Additional program steps are required for alphameric comparisons. Standard subroutines facilitate this operation.

The primary differences between the Solid-State 80 and the Solid-State 90 processors are the code translation instructions and the buffer pattern arrangements. Each is peculiar to the kind of card handled, 80- or 90-column. The storage of data words on the drum optimizes input-output transfers to peripheral units. This involves the "interlaced" positioning of input-output data in order to achieve greater efficiency in the use of drum storage.

UNIVAC Solid-State systems are fully buffered so that virtually all the peripheral units can operate simultaneously with computing. The exception is the input-output channels

INTRODUCTION (Contd.)

§ 011.

which are used with synchronizers. These synchronizers can control up to 10 magnetic tape units and 10 RANDEX drum units. Only one unit connected to a synchronizer can be read or written upon at a time. The Model I can have only one synchronizer, while the Model II can have a second synchronizer which permits an additional 10 magnetic tape units to be connected to the system. In Model I systems, only read/compute and write/compute are possible. In Model II systems, read, write, and compute operations can be handled simultaneously through the use of a second synchronizer.

The input-output units connected to any one system in addition to the synchronizer can include the following:

600 card per minute Card Reader.
150 card per minute Card Read-Punch.
600 line per minute Printer.
500 character per second Paper Tape Reader and/or 100 character per second Punch.

The software provided for the system includes service routines, mathematical functions and routines, linear programs, and two assembly programs (X-6 and the more recent S-4). X-6 is an elementary drum-type assembly program for Model I processors and S-4 is a more advanced system incorporating provision to call in symbolic library routines for either Model I or Model II Processors. Problems coded in X-6 with minor revisions can be assembled using S-4.

From the point of view of software, very few programs which are written specifically for the Model II presently exist in the library. Most appear to be adaptations of their Model I equivalents, and do not fully utilize the faster facilities. (Software support for the Model I appears to be phasing out presently, and while users can look forward to new programming during the current year, it appears doubtful that anything other than maintenance can be expected thereafter.)

Other systems carried over from the Model I include a BELL interpretive system (user developed) and a numerical control system. No COBOL or FORTRAN systems are presently available.

The Model II is essentially a modified Model I. For details, refer to the Introduction for that system (Report 771:).

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or use
Digit:	4 bits	Decimal digit, algebralic sign
Word:	44 bits	Instruction or 10 digits and sign.
2 Words:	20 digits	10 characters.
Band:	200 words	Magnetic drum.
Block:	48 words	RANDEX store.
Track:	12 blocks	RANDEX store.
Sector:	20 tracks	RANDEX store.
Drum Half:	100 sectors	RANDEX store.
Units:	4 drum halves	RANDEX store.

.2 DATA FORMATS

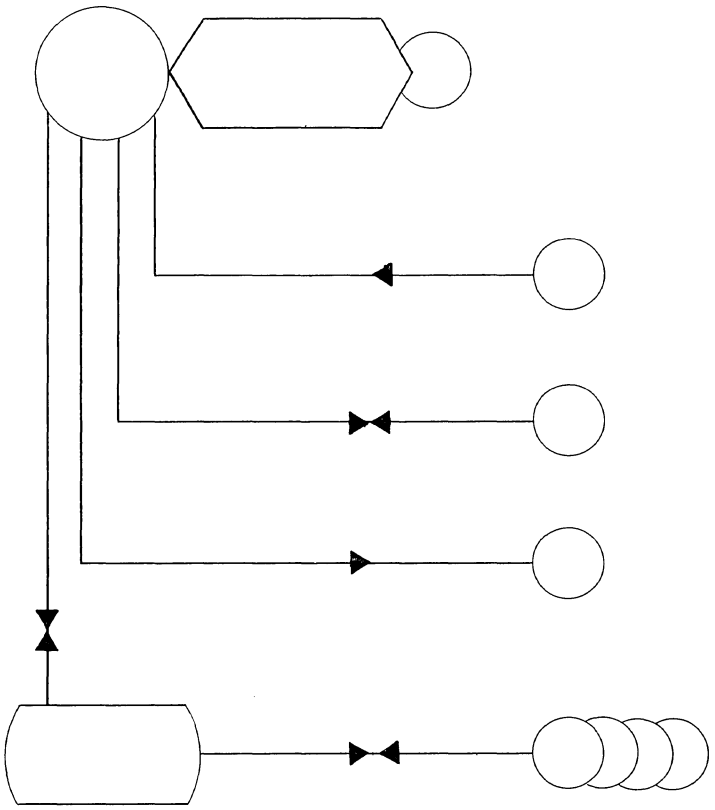
Type of Information	Representation
Numeral:	1 digit.
Alphabetic:	$1\frac{1}{2}$ or 2 digits.
Instruction:	1 word.
Number:	10 digits + sign.
Interlace:	refers to input-output area of each peripheral unit. It consists of a number of words on a single 200-word band of the drum, the arrangement and number being fixed by the peripheral unit and the type of data transmission.

SYSTEM CONFIGURATION

§ 031.

.1 4-TAPE BUSINESS SYSTEM

Deviations from standard configuration:. . . . . 160% more storage.
full simultaneity included.
indexing included.



Equipment	Rental
Processor and Console:	
2, 600 Word Drum.	
1, 280 Word Core Store.	$3, 235
High Speed Reader:	
600 cards/min.	255
Read Punch:	
150 cards/min.	725
High Speed Printer:	
600 lines/min.	935
Control:	
4 Uniservo IIs	1, 000
16, 400 char/sec.	1, 800

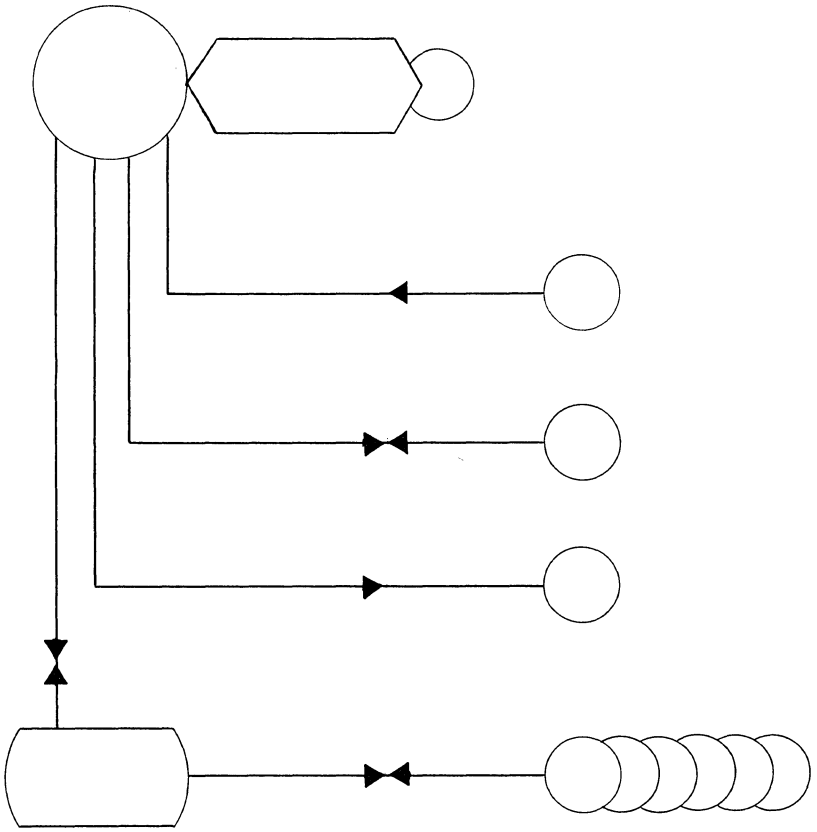
Optional Features Included:. . . . . Program Interrupt. 60
Multiply-divide. 400
20 print positions. 30
Stacker-Select on Reader and Punch. 100
Post-Read Station on Punch. 100

TOTAL $8, 640

§ 031.

.2 6-TAPE BUSINESS SYSTEM

Deviations from standard configuration: . . . . . full simultaneity included.
no console typewriter.
magnetic tapes 50% slower.
6 extra Index Registers.

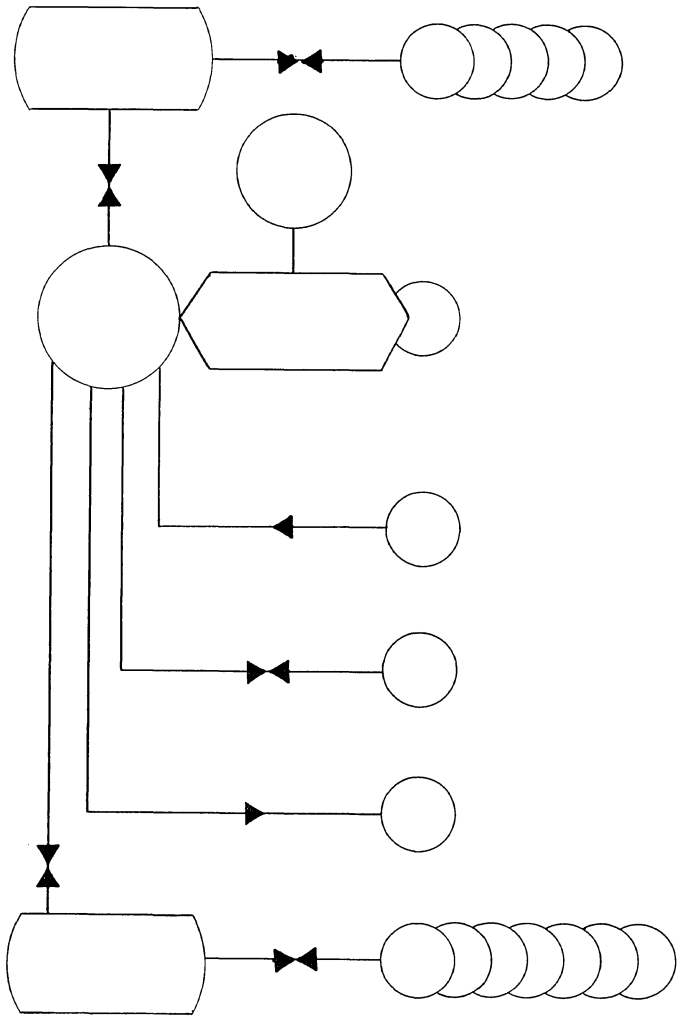


Equipment	Rental
Processor and Console: 2,600 Word Drum. 1,280 Word Core.	$3,235
High Speed Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 lines/min.	935
Control: 6 Uniservo IIs	1,000
16,400 char/sec.	2,700
Optional Features Included:	
Program Interrupt.	60
Multiply-divide.	400
20 print positions.	30
Stacker Select on Reader and Punch.	100
Post-Read Station on Punch.	100
TOTAL	$9,540

§ 031.

.3 12-TAPE BUSINESS SYSTEM

Deviations from standard configuration: . . . . . 900 words less storage.
no console typewriter.
Printer and Card Reader 40% slower.
Magnetic Tapes 75% slower.



Equipment	Rental
Control:	
5 Magnetic Tape Units	$1,000
16,400 char/sec.	2,250
Core Storage:	
1,280 words.	
Processor and Console:	5,935
5,000 word Drum.	
High Speed Reader:	
600 cards/min.	255
Read Punch:	
150 cards/min.	725
High Speed Printer:	
600 lines/min.	935
Control:	
7 Uniservo IIs	1,000
16,400 char/min.	3,150

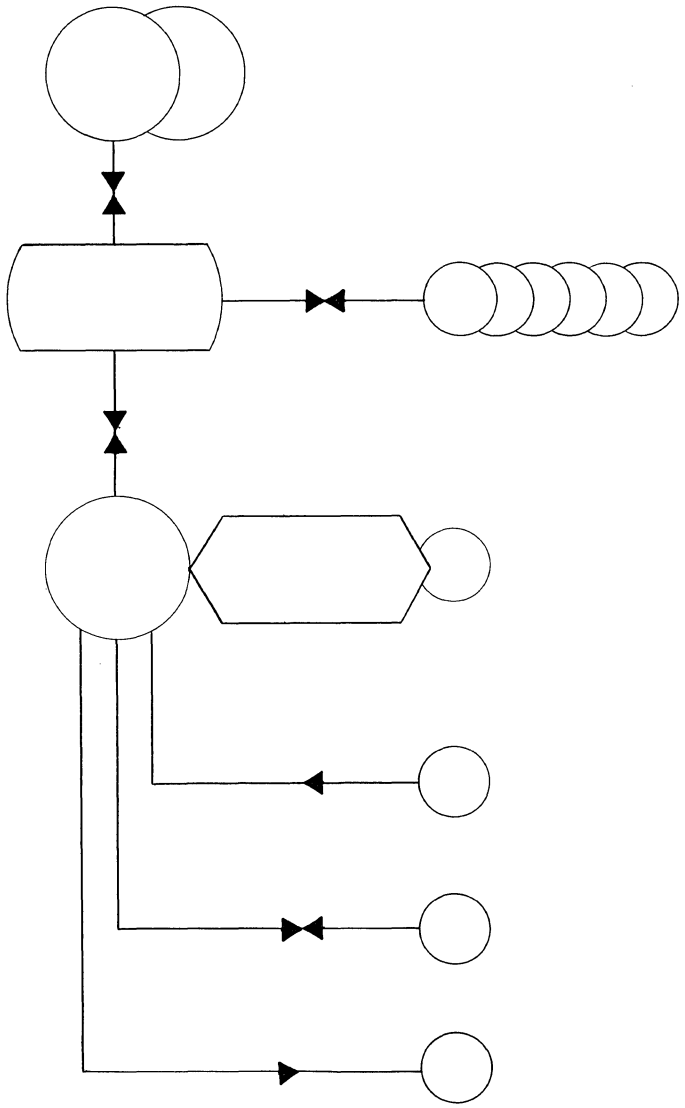
Optional Features Include: . . . . . Program Interrupt. 60
Multiply-divide. 400
20 print positions. 30
Stacker-Select on Reader and Punch. 100
Post-Read Station on Punch. 100

TOTAL $15,940

§ 031.

.4 6-TAPE AUXILIARY STORAGE

Deviation from standard configuration: . . . . . no console typewriter.
full simultaneity included.
magnetic tape units 50% slower.

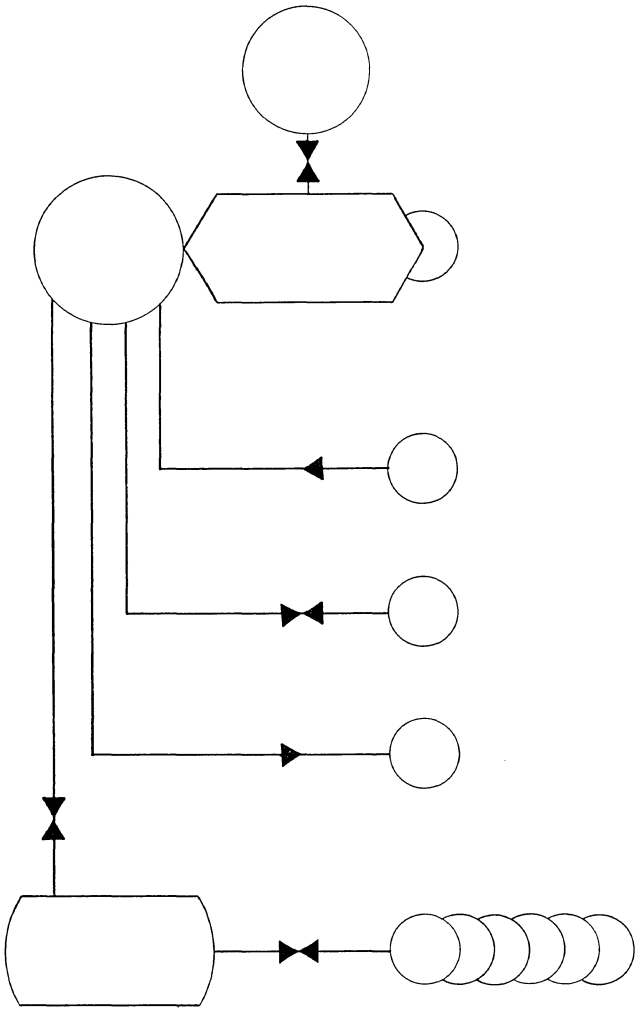


Equipment	Rental
Store: 21.5 million characters in 2 RANDEX File Drum Units.	$2,500
Control: 6 Uniservo IIs 16,400 char/sec.	1,000 1,800
Processor and Console: 2,600 word Drum. 1,200 core store.	3,235
High Speed Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 lines/min.	935
Optional Features Include:	
Program Interrupt.	60
Multiply-divide.	400
20 print positions.	30
Stacker-Select on Reader and Punch.	100
Post-Read Station on Punch.	100
TOTAL	$11,140

§ 031.

.5 6-TAPE BUSINESS/SCIENTIFIC

Deviations from standard configuration: . . . . . no floating point.
no console typewriter.
full simultaneity included.
magnetic tape units 50% slower.



Equipment	Rental
Core Storage: 1,280 words.	
Processor and Console: 8,800 Word Drum.	$7,135
High Speed Reader: 600 cards/min.	255
Read Punch: 150 cards/min.	725
High Speed Printer: 600 cards/min.	935
Control:	
6 Uniservo IIs	1,000
16,400 char/sec.	2,700

Optional Features Include: . . . . . Program Interrupt. 60
20 Print Positions. 30
Stacker Select on Reader and Punch. 100
Post-Read Station on Punch. 100

TOTAL $13,040

INTERNAL STORAGE: MAGNETIC DRUM

§ 041.

.1 GENERAL

.11 Identity: . . . . . SS 80/90 Magnetic Drum, Model I and Model II.

.12 Basic Use: . . . . . working storage.

.13 Description

The Magnetic Drum is the major store for all UNIVAC Solid-State systems. The drum rotates once every 3.4 milliseconds, and any reference to an operand or an instruction must wait until the drum is correctly positioned under the read/write heads. This action can take up to the 3.4 milliseconds necessary for a full revolution; however, for 1, 2, 3, 4, 5 or 8 bands of the drum, the maximum is reduced to 0.85 millisecond by the use of 4 read/write heads spaced 90 degrees apart around the circumference of the drum. (The nomenclature of these portions is confusing and has varied over the years. The official terminology is "Fast Access" for the slower access area of the drum, and "High Speed Access" for the faster access areas. Alternatively, the terms "Normal" and "Fast" have also been used to describe the same respective areas.)

Information is arranged on the drum in bands of 200 words, each of eleven 4-bit characters, and is operated upon in the Model I as words of 10 numeric characters with sign bit. However, the Model II uses the full four-bit sign character. Two models of the drum are available, a 25-band (5,000-word) drum, and a 46-band (9,200-word) drum. These numbers for bands do not include the buffer bands, which are also actually located on the drum. The smaller drum can be supplied with only 13 or more of the 25 bands being usable as in the STEP (Simple Transaction to Economical Processing). The other bands, however, are still physically present. Each band has either one or four read/write heads, so that the respective maximum access time is either one complete revolution or one-fourth of a revolution (3.4 milliseconds).

The decreased price which results from reduction in the drum storage capacity accounts for the greatest part of the price difference between the basic UNIVAC Solid-State system, and the reduced systems.

.14 Availability: . . . . . 10 months.

.15 First Delivery: . . . . 1958.

.16 Reserved Storage

Purpose:	I/O control.
Number of locations: .	2 to 4 bands, 200 words each.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic drum.

.22 Physical Dimensions

.222 Drum or Disc

Diameter:	approx. 5 inches.
Thickness or length: .	approx. 8 inches.
Number on shaft: . . .	1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by program:	yes.
.242 Data regenerated constantly:	no.
.243 Data volatile:	no.
.244 Data permanent:	no.
.245 Storage changeable: . .	no.

.25 Data Volume Per Band of 5 Tracks

Words with sign:	200.
Characters:	1,000.
Digits:	2,000.
Instructions:	200.

.26 Bands Per Physical Unit: 15 to 49 per drum.

.27 Interleaving Levels: . . 1.

.28 Access Techniques

.281 Recording method: . . .	fixed heads.

.283 Type of access

Description of Stage	Possible Starting Stage
Wait for drum rotation:	yes.
Read or write word: .	no.

.29 Potential Transfer Rates

.291 Peak bit rates

Cycling rates:	17,670 rpm.
Track/head speed: . .	4,628 inches/sec.
Bits/inch/track: . . .	153.
Bit rate per track: . .	707,000 bits/sec/track.

.292 Peak data rates

Unit of data:	word (5 alpha or 10 numeric char).
Conversion factor: . .	60 bits/word.
Gain factor:	5 tracks/band.
Loss factor (degree of interleaving):	none.
Data rate:	58,825 words/sec.

§ 041.

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see table.

.32 Rules for Combining Modules: . . . . . any combination of increments is possible.

.4 CONTROLLER: . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Stacks per system: . . 18 to 79.
Stacks per module: . . 18 to 79.
Stacks per yoke: . . . . 1, 2, or 4.
.512 Stack movement: . . . . none.
.513 Stacks that can access any particular location: . . . . . 1 per band, fast access.
4 per band, high speed access.
.514 Accessible locations By single stack: . . . 200 words.
.515 Relationship between stacks and locations: . . . . . Band (Address/200).
Band position Address (mod 200).

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . . 0 to 3,400 μsec.
Cycle time: . . . . . 17 μsec.
For data unit of: . . . 1 word.

.532 For variable access

Stage	Time	Example
Wait for word to reach head		
Fast:	0 to 3,400 μsec	1,700.
High Speed: . . .	0 to 850 μsec	425.
Transmit word: .	17 μsec	17.
Total:		2,142.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 AUXILIARY STORAGE PERFORMANCE

.71 Data Transfer: . . . . data can be transferred from the drum to any part of the computer store.

.72 Transfer Load Size

With self: . . . . . 1 word, or 200 via tape buffer.
With core: . . . . . 1 to 200 words.

.73 Effective Transfer Rate

High speed store with self: . . . . . 1,850 words/sec.
High speed store with fast store: . . . 460 words/sec.
Fast store with self: . 460 words/sec.
High speed or fast store magnetic core: . .10,000 words/sec.

.8 ERRORS, CHECKS AND ACTION

Errors	Check or Interlock	Action
Invalid address:	none	accesses a predictable address.
Receipt of data:	parity	sets indicator.
Dispatch of data:	parity	processor stop.
Conflicting commands:	yes	processor stop.
Recovery of data:	parity	processor stop.

MODULE AND SYSTEM SIZES

	Minimum Storage	"Fast" Increment	High Speed Increment	Maximum Storage
Identity:				
Drums:	1	-	-	1
Words:	2,600	200	400	8,800
Characters:	17,333	1,333	2,666	59,000
Instructions:	2,600	200	400	8,800
Bands:	13	1	2	44
Digits:	26,000	2,000	4,000	88,000
Modules:	1	-	-	1

INTERNAL STORAGE: MAGNETIC CORE

§ 042.

.1 GENERAL

.11 Identity: . . . . . Magnetic Core.
Core.

.12 Basic Use: . . . . . working storage.

.13 Description:

The magnetic core store is the major difference between a Model II UNIVAC Solid-State system and a Model I. The effect of this difference has been to increase considerably the amount of processing that can be performed in a given time period. This increase means that many applications which were formerly computer-limited become input-output limited. Naturally, applications which are initially input-output limited will not be affected.

Transfer of a Model I program to Model II may not automatically relieve computerbound applications. The reason is to be found in the means of addressing the core. Addressing the core uses non-numeric characters, which are not always as easy to handle as the numeric addresses of the drum store. As a result, currently running applications may require reprogramming to capitalize fully on the potential advantages of the faster core store.

The core store is actually faster than the basic machine word time (13.5 microseconds rather than 17). Thus, any word in the core store can be accessed only each 17 microseconds. The tape units can use the core store as their input-output areas, but data from input-output units must first be entered onto the actual drum store, and then transferred to core separately.

The magnetic core contains 1,280 words of 44 bits, and is divided into two logically separate areas:

(a) the first 1,000 locations
(b) the last 280 locations.

Both areas can operate as working storage for both data and instructions, but area (b) is intended for use as index registers and other special uses, and it has two restrictions: first, any instruction that uses index registers or causes overflow, error jumps, or block transfers is not executed correctly from this area; second, any address to core storage formed by indexing is effected in a non-standard manner.

Transfers to core are possible directly to and from the input-output area buffer bands but must be made from sections commencing at an address which is a multiple of 200.

.14 Availability: . . . . . 10 months.

.15 First Delivery: . . . . July, 1962.

.16 Reserved Storage

Purpose	Number of Locations	Locks
Index registers:	6	none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic core.

.22 Physical Dimensions:

.221 Magnetic core type storage
Array size: . . . . . 64 by 64 bits.
No. of arrays . . . . 16.

.23 Storage phenomenon: . . magnetization.

.24 Recording Permanence

.241 Data erasable by program: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . yes.
.244 Data permanent: . . . no.
.245 Storage changeable: . . . . . no.

.28 Access Techniques

.281 Recording method: . . coincident current.
.282 Reading method: . . . sense wire.
.283 Type of access: . . . uniform.

.3 DATA CAPACITY

.31 Module and System Sizes

	Only Size
Words:	1,280
Characters:	64,000 or 85,333 depending on packing.
Instructions:	1,280
Digits:	12,800
Digits and Signs: . . .	14,080
Modules:	1

.4 CONTROLLER: . . . None.

.5 ACCESS TIMING . . . 17 msec/word.

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . 13.5 μ sec.
Cycle time: . . . . 17 μ sec.
For data unit of: . . 44 bits.
For actual unit of: . . 48 bits (i.e., with 4 parity bits).

§ 042.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 AUXILIARY STORAGE PERFORMANCE

.71 Data Transfer . . . . data can be transferred between the core and the drum.

.72 Transfer Load Size

With self: . . . . . 1 word.
With drum: . . . . . 1 to 200 words.

.73 Effective Transfer Rate

With self (using program loop): . . . . 7,356 words per second.

.8 ERRORS, CHECKS AND ACTION

Errors	Check or Interlock	Action
Invalid address	none	any specific invalid address will refer to a predictable but incorrect address.
Receipt of data:	parity	stop.
Dispatch of data:	parity	stop.
Conflicting commands:	not possible.	
Physical record missing:	not possible.	
Recovery of data:	parity	stop.

INTERNAL STORAGE: RANDEX DRUM

§ 043.

.1 GENERAL

.11 Identity: . . . . . RANDEX Drum Storage Types No. 7965, 7957, and 7966.
RANDEX.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description:

The RANDEX Drum storage provides the auxiliary storage for the solid-state system. Each module has the capacity for either one or two drums. Each drum has a capacity of 1,152,000 words of 44 data bits each, plus parity bits. A maximum system contains 10 such pairs of drums for a capacity of 23,040,000 words.

Each drum is mounted with its axis horizontal and pairs are mounted one above the other. A common yoke mounted between them carries two heads, one to access a track on the upper drum and one to access a track on the lower drum.

Each drum is divided into 2,000 bands of 1 track each. Each band of 576 words is divided into 12 sectors of 48 words each. Only one sector in the RANDEX system can be accessed at a time.

Each sector can be considered also as 4 subsectors, each containing 1 key word and 11 data words. Special "search-read" and "search-write" instructions can be used with reference to subsector keys.

These instructions read and check a 10-character word against the labels on a 6-block area. Up to four labels per block can be used, thus providing a maximum search area of 24 records or six 48-word blocks, whichever is smaller. Fifteen areas per record can be searched.

Access time varies from 5 to 540 milliseconds and a typical time to locate, read, and update data in a random subsector is approximately 450 milliseconds. However, except for 7 milliseconds of this time, all other simultaneity is preserved, provided that magnetic tapes on the RANDEX Synchronizer are not used. As these figures indicate, designing the data layout on the drum can very greatly affect the overall timings.

This store is accessed as a peripheral device using a Buffer band and a Synchronizer which needs a special adaptation for the first RANDEX module only. Only one Synchronizer can be used.

The Synchronizer is capable of handling up to 10 RANDEX Drum units and up to 10 magnetic tape units.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . January, 1962.

.16 Reserved Storage: . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic drums.

.22 Physical Dimensions

.222 Drum or Disc
Diameter: . . . . . 24.3 inches.
Thickness or length: . . . . . 44 inches.
Number on shaft: . . 1.

.23 Storage phenomenon: . . . . . magnetization.

.24 Recording Permanence

.241 Data erasable by program: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . . . . . no.

.25 Data volume per band of 1 track

Words:	576
Characters:	2,880.
Digits:	5,760.
Instructions:	576.
Model 1 packed characters:	3,840.
Model 2 packed characters:	3,600.

.26 Bands per physical unit: . . . . . 2,000.

.27 Interleaving Levels: . 1.

.28 Access Techniques

.281 Recording method: . . . moving heads.
.282 Reading method: . . . same.
.283 Type of access

Description of stage	
Wait for synchronizer not busy:	Access to a record can occur at any one of these stages, providing the drum is in the correct position.
Move head to selected track:	
(If writing) Fill buffer:	
Wait for selected sector:	
(If reading) Empty buffer:	

§ 043.

.29 Potential Transfer Rates

.291 Peak bit rates
Cycling rates: . . . . 870 rpm.
Track/head speed: . . 1,108 inches/sec.
Bits/inch/track: . . . 650
Bit rate per track: . . 720,000 bits/sec/track.
.292 Peak data rates
Unit of data (character or word): . . . word.
Conversion factor (bits for unit): . . . 44 bits/word.
Gain factor (tracks per band): . . . . . 1.
Loss factor (degree of interleaving): . . 12.
Data rate: . . . . . 696 words/sec/device.

.3 DATA CAPACITY

.31 Module and System Sizes

[See table below]

.32 Rules for Combining Modules: . . . . . none, or 1 7965; or 1 7957; or up to 9 7966's with either a 7965 or a 7957.

.4 CONTROLLER

.41 Identity: . . . . . Synchronizer. Type No. 7914.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1 to 10.
.432 Restrictions: see Paragraph .13.

.44 Data Transfer Control

.441 Size of Load: . . . . . 48 words (1 block).
.442 Input-Output area: . . . . . buffer band in Magnetic Drum.
.443 Input-Output area access: . . . . . entire block.
.444 Input-Output area lockout: . . . . . none, test busy required in program to protect area.
.445 Synchronization: . . . automatic.
.446 Synchronizing aids: . . . . . test busy.
.447 Table control: . . . . none.

MODULE AND SYSTEM SIZES

	Minimum Storage				Maximum Storage
Identity:		No. 7965	No. 7957	No. 7966	
Drums:	0	1	2	2	20.
Words:	0	1,152,000	2,304,000	2,304,000	23,004,000.
Characters:	0	5,760,000	11,520,000	11,520,000	115,200,000.
Instructions:	0	1,152,000	2,304,000	2,304,000	23,040,000.
Blocks:	0	24,000	48,000	48,000	480,000.
Digits:	0	11,520,000	23,040,000	23,040,000	230,400,000.
Model 2 packed character:	0	7,680,000	15,360,000	15,360,000	153,600,000.
Model 1 packed character:	0	7,200,000	14,400,000	14,400,000	144,000,000.
Modules:	0	1	1	1	10.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Stacks per system: . . . . . 20 maximum.
Stacks per module: . . 2.
Stacks per yoke: . . . 2.
Yokes per module: . . 1.
.512 Stack movement: . . . across length of drum.
.513 Stacks that can access any particular location: . . . . . entire drum accessible.
.514 Accessible locations
By single stack
With no movement: . . . . . 12 blocks.
With all movement: . . . . . 12,000 blocks.
By all stacks
With no movement: . . . . . 24 blocks per module. 240 blocks per system.

§ 043.

.53 Access Time Parameters and Variations

.532 Variation in access time

Stage	Variation, msec.	Example, msec
Wait for Synchronizer not busy:	0 to 15	0.0.
Move head to selected track:	0, or 125 to 540	300.0.
Fill buffer (writing):	3.4	3.4.
Wait for selected block:	0 to 69	20.0.
Write or read:	34.5	34.5.
Empty buffer (reading):	3.4	0.0.
Total:		357.9.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 AUXILIARY STORAGE PERFORMANCE

.71 Data Transfer

Pair of storage units possibilities
With self: . . . . . no.
With Magnetic Drum: . . . . . yes.

.72 Transfer Load Size

With Magnetic Drum, Model 2: . . . . . units of 320 packed characters.
With Magnetic Drum, Model 1: . . . . . units of 300 packed characters or 240 characters.

.73 Effective Transfer Rate

With Magnetic Drum, Model 2: . . . . . 4,640 packed char/sec.
With Magnetic Drum, Model 1: . . . . . 4,350 packed char/sec or 3,480 char/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	sets indicator.
Receipt of data:	check	sets indicator.
Dispatch of data:	check	sets indicator.
Off Normal*:	check	sets indicator.
Physical record missing:	check	sets indicator.
Parity	check	sets indicator.

* Off Normal includes . . . . Buffer overflow
Buffer underflow
Block size
Bad spot
Bad track
Faulty operation
Interlock

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . . Central Processor. Model II.

.12 Description

The UNIVAC Solid-State Model II Central Processor is designed to process alphameric data from card and magnetic tape input-output media. The use of the core store as the primary program execution area makes optimization much easier and results in more operations per second. All operations occur in decimal, fixed point mode. The division order provides a remainder, and alphameric comparison instructions are included in the repertoire.

A zero suppress instruction is included in the instruction repertoire, and translation to or from card code is automatic. Commercial format, particularly for output purposes, is not simple because the other editing functions (punctuation, check protection, etc.) must be programmed. Also, the drum storage interlace introduced in the Model I to speed input-output operations is still used in the Model II, although it is no longer so advantageous.

The programming technique used on the Model II is an extension of the Model I technique. Data is preferentially held in core storage, and with it, those instruction loops which would operate inefficiently if held on the drum. Such inefficiencies could be due to the fact that they were not optimally programmed, they did not fit exactly within the duration of the drum revolution, or they used multiplication and division instructions. These two instructions are variable-time instructions which preclude optimal programming of ensuing instructions.

The over-all speed capability of the Model II system is approximately 20,000 additions per second. With all input-output fully operating, this speed is reduced from 16,000 to 17,000 additions per second because complete overlap is possible more than 80 per cent of the time.

This capability, which is an improvement of 40 per cent over the UNIVAC Solid-State Model I, has been achieved by overlapping within instructions rather than by changing instruction logic.

Operands and instructions which are stored in the core are accessed in parallel with other parts of the instruction cycle. An add to accumulator instruction, which formerly took five word times, is now completed in three word times.

.13 Availability: . . . . . 10 months.

.14 First Delivery: . . . . June, 1962.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point			
Add-Subtract:	yes	decimal	10 digits + sign.
Multiply			
Short:	sentinel	decimal	2 to 8 + sign.
Long:	yes	decimal	10 digits + sign.
Divide			
No remainder:	no.		
Remainder:	yes	decimal	2 to 10 digits + sign.
.212 Floating point			
Add-Subtract:	subroutine	decimal.	
Multiply:	subroutine	decimal.	
Divide:	subroutine	decimal.	
.213 Boolean			
AND:	yes } Binary		40 bits.
Inclusive OR:	yes }		40 bits.
.214 Comparison			
Numbers:	yes		10.
Absolute:	subroutine		10 char.
Letters:*	subroutine		10 char.
Mixed:*	subroutine		10 char.

* requires 5 instructions (5 executed).

.215 Code translation: . . . all UNIVAC Solid-State systems except 90-column card systems have automatic code translation during card operations. All systems can translate word-by-word between the internal coding and the appropriate card codes, and for the purposes of compatibility with UNIVAC I, II, etc., to Excess 3 code.

.217 Edit format

	Provision	Comment	Size
Alter size:	no.		
Suppress zero:	yes	also commas	10 chars.
Round off:	no.		
Insert point:	no.		
Insert spaces:	no.		
Insert:	no.		
Float:	no.		
Protection:	no.		

.218 Table look-up: . . . . . subroutine.

.219 Others: . . . . . in tape systems, the tape buffer may be utilized to transfer a band of 200 words from one part of the store to another. During the transfer all words move cyclically back one word in relative position, thus word number 6 becomes word number 5. Word number 1 becomes word number 0 and number 0 becomes number 199.

§ 051.

.22 Special Cases of Operands

.221 Negative numbers:. . . least significant 4 bits of each word always contain sign digit, 0 for positive, and 5 for negative.
.222 Zero:. . . . . both plus and minus zero can occur and are not equal in comparisons.
.223 Operand size determination: . . . . fixed.

.23 Instruction Formats

.231 Instruction structure: . 1 word.
.232 Instruction layout:

Part	Op	m	c	S
Size (digits)	2	4	4	1

.233 Instruction parts

Name	Purpose
OP:	operation code.
m:.	memory address (indexable) second instruction address, or operation variation.
c:	next instruction address.
S:	Index Register.

.234 Basic address structure: 1 + 1.
.235 Literals
Arithmetic:. . . . . only set register to zero.
Comparisons and tests: . . . . . none.
Incrementing modifiers: . . . . . yes.
.236 Directly addressed operands
.2361 Internal storage type

	Min. size	Volume accessible
Magnetic Drum:	2,600 words	8,800 words.
Magnetic Core:	1,280 words	1,280 words.
RANDEX:	optional	23,040,000 words.

.2362 Increase address capacity: . . . . . not needed.
.237 Address indexing
.2371 Number of methods: . 2.
.2372 Names: . . . . . Indexing.
Band Modification.
.2373 Indexing rule: . . . . increment added to instruction address. Under certain circumstances the address is made to cycle within a band (200 words) of drum store. Otherwise, it cycles either modulo 5,000 or modulo 10,000 depending on the store size.
.2374 Indexing specification: by the programmer; number 1 to 9 on the coding sheet. in the machine instruction: use of the sign char, and 1 bit of the operation code.
.2375 Number of potential indexers: . . . . . 9.
.2376 Addresses which can be indexed: . . . . . all.
.2377 Cumulative indexing: . none.
.2378 Combined index and step:. . . . . no.
.238 Indirect addressing: . . none.
.239 Stepping
.2391 Specification of increment: . . . . . in stepping instruction.
.2392 Increment sign:. . . . positive; complements used for decrements.
.2393 Size of increment: . . 4 digits.
.2394 End value: . . . . . in test instruction.
.2395 Combined step and test: . . . . . no.

.24 Special Processor Storage

.241 Category of storage

	Number of locations	Size in words	Program usage
Register:	4	1	arithmetic, temporary storage, and control.
Index:	9	0.4	indexing.
Buffers:	3 to 5	200	input-output.

.242 Category of storage

	Total no. of locations	Physical form	Access time μsec	Cycle time μsec
Register:	4	hardware	17	17.
Index:	9	3 in hardware, 6 in core	17	17.
Buffers:	3 to 5	drum bands	3,400 to 5,100	3,400.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: 1 + 1 addressing.

.32 Look-Ahead: . . . . . yes, for the next instruction.

.331 Possible causes
In-out units: . . . . . High Speed Reader Buffer Loaded (optional).
.332 Program control
Individual control: . . High Speed Reader.
Method:. . . . . transfer to special location when card reader buffers are loaded.
Restriction: . . . . . none.
.333 Operator control: . . . none.
.334 Interruption conditions: buffer loaded.
.335 Interruption process
Disabling interruption: none.
Registers saved: . . . next instruction stored in fixed location.
Destination: . . . . . a fixed location.
.336 Control methods
Determine cause: . . implicit.
Enable interruption: . always enabled.

.34 Multi-running: . . . . . none.

.35 Multi-sequencing: . . . none.

§ 051.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μsec: . . . . . the times given assume that both instructions and operands are contained in the core.

.411 Fixed point
- Add-subtract: . . . . 51.
- Multiply: . . . . . 68 + 170D.
- Divide: . . . . . 51 + 170D.

.412 Floating point: . . . . . none.

.413 Additional allowance for
- Indexing: . . . . . 17.
- Instructions on the drum: . . . . . 17 plus latency of 0 to 3,400.
- Operands on the drum: 17 plus latency of 0 to 3,400.

.414 Control
- Branch: . . . . . 34.
- Compare and branch: 51.

.415 Counter control
- Step: . . . . . 68.
- Step and test: . . . . . none.
- Test: . . . . . 51.

.416 Edit
- 10-character zero suppression: . . . . 68.

.417 Convert: . . . . . 51.

.418 Shift: . . . . . 51 + 17D.

.42 Processor Performance in μsec: . . . . . it is assumed that in addition to the specific conditions which follow, the program has been written for the Model II, and not simply transferred from the Model I.

.421 For random addresses

For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data is held in Random positions on the core.
- c = a + b: . . . . . 136.
- b = a + b: . . . . . 136.
- Sum N items: . . . . 51N.
- c = ab: . . . . . 119 + 170D.
- c = a/b: . . . . . 119 + 170D.

.422 For arrays of data

For the following times, it is assumed that the instructions are stored on Normal access portions of the drum, but executed in the core storage. This effectively reduces the time lost at the end of each iteration of the loop because of poor latency. It does involve some additional work in actually transferring the data, and this is shown separately under Set-Up Time.

	Set-Up	Execution
$c_i = a_i + b_j$:	238	374.
$b_j = a_i + b_j$:	238	340.
Sum N items:	204	153N.
$c = c + a_i b_j$:	238	2,057N.

.423 Branch based on comparison

For the following times, it is assumed that the instructions are stored on Normal access portions of the drum, but executed in the core storage. This effectively reduces the time lost at the end of each iteration of the loop because of poor latency. It does involve some additional work in actually transferring the data, and this is shown separately under Set-Up Time.

	Set-Up	Execution
Numeric data: . . .	306	459.
Alphabetic data: . .	340	505.

.424 Switching

For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data is held in Random positions on the core.
- Unchecked: . . . . . 238N.
- Checked: . . . . . 459N.
- List search: . . . . 255N.

.425 Format control per character

For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data is held in Random positions on the core.
- Unpack: . . . . . 27N.
- Compose: . . . . . 190N.

.426 Table look up per comparison

For the following times, it is assumed that the instructions are stored on Normal access portions of the drum, but executed in the core storage. This effectively reduces the time lost at the end of each iteration of the loop because of poor latency. It does involve some additional work in actually transferring the data, and this is shown separately under Set-Up Time.

	Set-Up	Execution
For a match:	221	442N:
For least or greatest:	255	459N.
For interpolation point:	255	459N.

.427 Bit indicators

For the following times, it has been assumed that the instructions are held on the Normal access portion of the drum in known positions, and that the data is held in Random positions on the core.
- Set bit in separate location: . . . . . 68.
- Set bit in pattern: . . 102.
- Test bit in separate location: . . . . . 136.
- Test bit in pattern: . 170.
- Test AND for B bits: 170.
- Test OR for B bits: . 170.

.428 Moving: . . . . . See Internal Storage .73.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	program jump.
Underflow (float-pt):	none.	
Zero divisor:	check	program jump.
Invalid data:	not possible.	
Invalid operation:	some checks	stops or partial execution.
Arithmetic error:	some checks	sometimes stops.
Invalid address:	checks	modulo store size.
Receipt of data:	error word	program jump.
Dispatch of data:	error word	program jump.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . Central Processor Control Panel.

.12 Associated Units: . . . . Processor Keyboard standing on the desk.

.121 Description:

The keyboard has 13 keys which include:

1. The digits 0 through 9
2. Plus and minus enter keys
3. An Alert key that clears a preselected input register
   Any combination of four bits can be entered. A lamp lights on the keyboard after pushing the Alert key indicating that the processor is ready to accept input from the keyboard.

.2 CONTROLS

.21 Power

Name	Form	Function
AC:	button-light	turns off AC and DC power.
DC:	button-light	turns off DC power.
DC Ready:	button-light	turns on AC and DC power.
Drum:	button-light	turns off AC and DC power.
Uniservo:	button-light	turns power to Uniservos on and off.

.22 Connections: . . . . . no positive indication.

.23 Stops and Restarts

.231 Stops

Name	Form	Function
Tape:	button	Causes Tape Off-Normal condition.
HSP:	button	Causes High Speed Printer Off-Normal condition.
FR:	button	Causes High Speed Reader Off-Normal condition.
RPU:	button	Causes Read Punch Off-Normal condition.
Comparison Stop:	button	Causes Stop on compare instructions.
Stop:	button	Stop Processor.

.232 Starts

Name	Form	Function
Tape Check:	button	Completes partially-executed tape commands.
Start:	button	Starts processor.
m:	button	Selects next address of two.
c:	button	Addresses to which control will be transferred when the Start button is depressed.

.24 Stepping

Name	Form	Function
W/O Index Regs:	button	execute one instruction without index registers when start button pushed.
W Index Regs:	button	execute one instruction with index registers when start button pushed.
Continuous:	button	executes instructions under program control when start button pushed.

.25 Resets

Name	Form	Function
General Clear:	button	resets indicators and logic.

.26 Loading: . . . . . none.

.27 Special

Name	Form	Function
No Print:	button-light	print orders executed but no printing occurs.
96 Check:	button-light	causes stop if card buffer is not emptied fast enough.
No Punch	button-light	punch orders executed but no punching occurs.

.3 DISPLAY

.31 Alarms: . . . . . none.

.32 Conditions

Name	Form	Function
Printer:	light	Off-Normal
Fast Reader:	light	Indicates that a malfunction
Read Punch:	light	has occurred in the particu-
Processor:	light	lar unit.
Test:	light	
Tape Sync.:	light	

§061.

.33 Control Registers

Name	Form	Function
Static Register:	two 5, 4, 2, 1 bit neon decades	indicates statically and dynamically what instruction is being executed.
Sign:	two neons	indicates the sign of quantity in display register.
Display Register:	ten decades	in one of the following registers: rA, rC, rL, or rX, depending upon which display button is pushed.

.34 Storage: . . . . . displayed in the Display register via rA, rC, rL, or rX.

.4 ENTRY OF DATA

.41 Into Control Registers: . same as Control Registers but via a control register plus executing store instruction, also keyed in.

.5 CONVENIENCE

.51 Communication: . . . . . none.

.52 Clock: . . . . . none.

.53 Desk Space: . . . . . length 22", depth 6", height 48".

.54 View: . . . . . operator must be standing to operate console; view is unobstructed by peripheral units Punch, Printer, and Reader.

INPUT-OUTPUT: HIGH SPEED READER

§ 071.

.1 GENERAL

.11 Identity: . . . . . High Speed Reader.
I: 80-Column Reader.
Unit No. 7935.

II: 90-Column Reader.
Unit No. 7945.

.12 Description

The high speed reader reads up to 600 cards per minute using two read stations, translating card images into machine codes and transferring them into the computer store. During 95 per cent of the time involved in the transfer, the central processor can continue operations. A standard subroutine function which uses up 7 per cent more of the card cycle time compares the card images, giving a total effective performance of 3,600 cards per minute read, translated, and verified with 88 per cent central processor overlap.

Both types of the 600 cards per minute reader are equipped with a hopper, 2 read stations, and 3 stackers. The only difference between the two types is the column size of the read stations. Although the unit will function without it, a vacuum system to assist card feeding is standard equipment. A Stacker Select and an Automatic Program Interrupt feature are available as options. The buffer between the reader and processor receives card images from both read stations whenever a card passes either. Should either of the stations be empty, the empty station will transmit the image of a card with every hole punched. Another feature of the reader is that a card is passed by both read stations and is moved into a stacker without stopping. A control routine is required to prevent the image from the first read station being overwritten by another image transmitted when the card passes the second read station unless the Automatic Program Interrupt option is used. When this option is available, the processor performs the following operations when the buffer is loaded. First, the current instruction is completed and the next instruction is stored in a fixed location. Control is then transferred to a subroutine. The last instruction of the subroutine causes control to be returned to the fixed location from which normal program sequencing is resumed.

Card images are represented internally in either translated or untranslated form. In the translated form, the internal code equivalents of the characters are punched into each column. In the untranslated form, an image of the physical card, each hole position is represented by a bit. Details of this presentation are given in the Data Code Tables.

.12 Description (Contd.)

Correctness of card reading is verified by routines in the processor and not in the reader. This internal redundancy check is more secure than hole counts and similar reader checks because it also covers the transfers between the reader and internal storage. However, this check requires both processor time and storage space to hold the separate images which are not required by automatic input checking systems. When checking is desired, an area must be reserved in storage for both images so that the comparison may be performed.

.13 Availability: . . . . . 7 months.

.14 First Delivery: . . . . November, 1958 - 90-Col.
December, 1959 - 80-Col.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording systems: . . none.
.222 Sensing system: . . . . brush.
.223 Common system: . . . none.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

	80-Column	90-Column
Use of station: . .	Read	Read.
Stacks:	1	1.
Heads/stack: . . .	80	45.
Method of use: . .	1 row at a time	1 row at a time.
Use of station: . .	Verify read	Verify read.
Distance:	15 rows	15 rows.
Stacks:	1	1.
Heads/stack: . . .	80	45.
Method of use: . .	1 row at a time	1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard punched card.
.312 Phenomenon: . . . . . punched holes;
rectangular on 80-column;
round on 90-column.

.32 Positional Arrangement

.321 Serial by: . . . . . 12 rows.
.322 Parallel by: . . . . . 80- or 45-columns.

§ 071.

.33 Coding: . . . . . 80-column (Hollerith, binary, column binary). 90-column (standard 90-column code).

.34 Format Compatibility: . 80-column card, any 80-column equipment. 90-column card, any 90-column equipment.

.35 Physical Dimensions: . standard punched card.

.4 CONTROLLER

.41 Identity: . . . . . built into Central Processor and the unit. Contains a special buffer band on the processor's drum to transmit and receive card images.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 2 cards.
.442 Input-Output areas: . . 2 interlaces on buffer band of 200 words.
.443 Input-Output area access: . . . . . 1 band.
.444 Input-Output area lockout: . . . . . area insecure without program tests unless Automatic Interrupt feature is used.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.
.447 Synchronizing aids: . . interrupt.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 card.
.512 Block demarcation Input: . . . . . fixed size (80- or 90-column).

.52 Input-Output Operations

.521 Input: . . . . . one image from each of two stations if a card was read at either.
.522 Output: . . . . . none.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . instruction provided.

.54 Format Control: . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . no.
Offset card: . . . . . no.
Select stacker: . . . . . yes.
Select format: . . . . . no.
Select code: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . no.
Busy device: . . . . . yes.
Output lock: . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: no.
Input buffer full: . . . . yes.
Off-Normal*: . . . . . yes.

* Off-Normal is a general term for any abnormal condition including:
empty stations.
full stacker.
empty hopper.
card jam.
equipment malfunction.

.6 PERFORMANCE

.61 Conditions: . . . . . no variation.

.62 Speeds

.621 Nominal or peak speed: 600 c.p.m.
.622 Important parameters

Name	Value
Cycle time:	100 msec.
Select stacker time span:	100 msec.
Feed card instruction time span: . .	100 msec.
Unload buffer time span:	15 msec.

.623 Overhead: . . . . . 1 clutch point. Note: Up to four read orders can be stacked by this unit.
.624 Effective speeds: . . . (600-C) c.p.m. C = number of clutch points missed per minute.

.63 Demands on System

Component	Condition	msec per card		Percentage
Central Processor:	unload images	3.5	or	3.0.
Central Processor:	verify overhead	7.0	or	6.0.

Note 1: If the second read station is used to verify the reading at the first read station, the central processor must unload the second image and perform the comparison.

§ 071.

.63 Demands on System (Contd.)

Note 2: The data read into the buffer band are stored in interleaved locations around the drum. To maximize processing efficiency, these data should be processed from the interleaved locations, since outputting computed results requires another kind of interleaved pattern which is best loaded from the input interleaved array.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Clear:	button-light	turn off "Off-Normal".
Computation:	2 buttons	stops and starts processor.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	1,000 cards.
Stackers (3):	1,200 cards each.

.732 Replenishment time: . . 0.2 to 1.0 min. does not need to be stopped.

.733 Adjustment time: . . . 1 to 5 minutes.

.734 Optimum reloading period: . . . . . 1.66 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	none.	
Input area overflow:	fixed.	
Invalid code:	all legal.	
Exhausted medium:	see "Off-Normal".	
Imperfect medium:	none.	
Timing conflicts:	program stall	wait.
Off-Normal*:	check	set indicator.

* Off-Normal includes: exhausted medium
equipment malfunction.

INPUT-OUTPUT: READ PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . . Read Punch.
80-column Punch Unit.
No. 7936.

90-column Punch Unit.
No. 7946.

.12 Description:

These two card punching units are able to process cards at a peak speed of 150 cards per minute, using a single point clutch.

Type 7936 contains 5 card stations: read, wait, punch, wait and read. The punch station is fitted for 80-column cards.

Type 7946 contains 3 card stations: read, punch and read. The punch station is fitted for 90-column cards.

The read stations are optional and can be fitted to read either 80- or 90- column cards in either type, although it is unlikely that mixtures are required. Each type has one hopper and two stackers, but the stacker select feature is optional.

There are automatic input code translations and four special instructions are available to perform some translation (see Internal Storage, Magnetic Drum, paragraphs 1.3) either for 80-column patterns or 90-column patterns.

The optional read stations are intended for use in conjunction with the punch. The last station permits sending an image of the card to enable verification in a routine. The first station permits reading part-punched cards before completing the punching. Note that two input and one output images are transmitted on any stimulated cycle of the device.

.13 Availability: . . . . . 7 months.

.14 First Delivery: . . . . . No. 7936 - December, 1959.
No. 7946 - June, 1958.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . . pinch rollers.
.212 Reservoirs: . . . . . Type 7936 only.
Number: . . . . . 2.
Form: . . . . . wait stations.
Capacity: . . . . . 1 card each.
.213 Feed drive: . . . . . pinch rollers.
.214 Take-up drive: . . . . . pinch rollers.

.22 Sensing and Recording Systems

.221 Recording system: . . . . punch and die.
90 char, round holes.
80 char, rectangular holes.
.222 Sensing system: . . . . . brush.
.223 Common system: . . . . no.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

	80-Column	90-Column
* Use of station:	read	read.
Stacks:	1	1.
Heads/stack:	80 or 45	45 or 80.
Method of use:	1 row at a time	1 row at a time.
Use of station:	wait	none.
Distance:	5 card rows.	
Stacks:	none.	
Heads/stack:	none.	
Method of use:	N. A.	
Use of station:	punch	punch.
Distance:	5 card rows	1 card.
Stacks:	1	1.
Heads/stack:	80	45.
Method of use:	1 row at a time	1 row at a time.
Use of station:	wait	none.
Distance:	5 card rows.	
Stacks:	none.	
Heads/stack:	none.	
Method of use:	N. A.	
* Use of station:	read	read.
Distance:	5 card rows	1 card.
Stacks:	1	1.
Heads/stack:	80 or 45	45 or 80.
Method of use:	1 row at a time	1 row at a time.

* These stations are optional.

.33 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard punch card.
.312 Phenomenon: . . . . . punched holes.
80 char rectangular.
90 char round.

.32 Positional Arrangement

.321 Serial by: . . . . . row (1 out of 12).
.322 Parallel by: . . . . . 80 col on 80 char card.
45-col on 90 char card.

.33 Coding: . . . . . Hollerith, column binary, binary, on 80-col card. Standard 90-col card code.

§ 072.

.34 Format Compatibility

80-column: . . . . . any 80-column equipment.
90-column: . . . . . any 90-column equipment.

.35 Physical Dimensions: . . standard punched card.

.4 CONTROLLER

.41 Identity: . . . . . built into Central Processor and the unit. Contains a special buffer band on the processor's drum to transmit and receive card images.

.42 Connection to System

.421 On-line: . . . . . 1 max.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . 1 max.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 3 cards (2 input and 1 output).
.442 Input-output areas: . . . 3 interlaces on 1 buffer band.
.443 Input-output area access: . . . . . band.
.444 Input-output area lockout: . . . . . punch area of buffer is locked out until punches are set up from previous instruction.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 card.
.512 Block demarcation
Input: . . . . . fixed.
Output: . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . 2 cards.
.522 Output: . . . . . 1 card.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . . automatic.

.54 Format Control: . . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . . no.
Offset card: . . . . . no.
Select stacker: . . . . . yes.
Select format: . . . . . no.
Select code: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . no.
Busy device: . . . . . yes.
Output lock: . . . . . no.
Nearly exhausted: . . . . no.
Busy controller: . . . . . yes.
End of medium marks: . no.
Off Normal*: . . . . . yes.
Input buffer full: . . . . yes.

* Off Normal includes: . empty stations.
full stackers.
empty hopper.
card jam.
equipment malfunction.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed . 150 c.p.m.
.622 Important parameters

Name	Value
Cycle:	400 m.sec.
Stacker select time span:	116 m.sec.
Start time span: . . .	133 m.sec.
Buffer unload time span:	136 m.sec.

.623 Overhead: 1 clutch point.
.624 Effective speeds: . . . . (150-C) c.p.m.
C = number of clutch points missed per minute.

.63 Demands on System

Component	Condition	m.sec. per card		Percentage
Central Processor	load buffer 1	3.5	or	0.9.
Central Processor:	unload buffers 2 & 3	3.5	or	0.9.
Central Processor:	note 1 below	10.4	or	2.7.

Note 1: If the second read station is used to verify the reading at the first station plus the punching done at the punch station, the program must merge the punch and first read images and compare punch and second read images.

Note 2: The data read into the buffer hand are stored in interleaved locations around the drum. To maximize processing efficiency, these data should be processed from the interleaved locations as the output computed results require another kind of interleaved pattern which is best loaded from the interleaved array upon input.

§ 072.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Computation	2 Buttons	starts & stops processor.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	600 cards.
Stackers (2):	1,200 cards each.

.732 Replenishment time: . . 0.25 to 1 mins.
does not need to be stopped.

.733 Adjustment time: . . . . 1 to 2 mins.

.734 Optimum reloading period: . . . . . 4 mins.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording	none.	
Reading:	none.	
Input area overflow:	not possible.	
Output block size:	fixed.	
Invalid code:	none.	
Exhausted medium:	see "off normal".	
Imperfect medium:	none.	
Timing conflicts:	interlock	wait.
Off Normal*:	check	set indicator.

* Off Normal includes: . . . . . punch bin full.
hopper empty.
stacker full.
card jam.
malfunction.

INPUT-OUTPUT: PAPER TAPE READER

§ 073.

.1 GENERAL

The paper tape reader and punch are two separate units housed in the same cabinet with their joint controller. The photoelectric reader operates at 500 characters per second. Five-, 6-, 7-, or 8-channel tape can be read, checked for parity, translated into 6-bit biquinary code, and stored in a 20-character buffer found in the synchronizer that is part of the entire paper tape unit.

The program is able to test the buffer and then transfer 10 characters at a time into the arithmetic registers of the computer. The average time involved is 187 microseconds per transfer, or less than 1 percent of the overall computer capacity.

.2 PHYSICAL FORM

A friction drive mechanism is used, with two 1-foot capacity reservoirs. A spooler can be added as an optional extra to take up the paper tape after it has been read.

.3 EXTERNAL STORAGE

Normal punched tape, with fully punched holes, can be used. Five-, six-, or seven-channel tapes can be used normally. An eight-channel tape can be used, but the eighth channel is restricted to some special function, as all other channels must be unpunched when the eighth is punched.

Various codes can be accommodated, including Teletype, Flexowriter, and DaSPan. Each installation decides its own "End of Message" and "End of Tape" signals, which can be two or three characters long. In addition, an installation-chosen signal is used as the "ignore" signal. Neither the "ignore" nor "blank" characters are read into the buffer.

.4 CONTROLLER

The central processor in a UNIVAC Solid-State system is the controller. Only one paper-tape system can be connected to a system. Access is directly into the arithmetic registers, and occurs only upon request. The amount transferred each time is 10 characters. The paper tape synchronizer contains a 20-character buffer. After the buffer has been filled, the reader pauses until it becomes unloaded.

.5 PROGRAM FACILITIES AVAILABLE

Reading, once started, continues until either a stop character is read or a stop instruction is executed. Failure to unload the 20-character buffer causes an

.5 PROGRAM FACILITIES AVAILABLE (Contd.)

indefinite pause in reading. Translation is controlled by plugboard and parity checking is controlled by a rotary switch. The reader shares both these controls with the punch unit.

"Ignore" characters and blanks are suppressed before the buffer is loaded. The program can test for whether the buffer is loaded or whether the unit is disabled, but cannot distinguish between the various possible disabling causes, such as torn tape, plug board not in place, overheating, no power.

.6 PERFORMANCE

The peak speed of the reader is 500 characters per second. The effective speed is the same, provided that the buffer is unloaded once each 20 milliseconds.

During the reading of the tape, the buffer is first filled; then its contents are transferred to the automatic registers. Transfer of the buffer contents to the registers takes place each 20 milliseconds, or within from 6 to 7 drum revolutions. This operation takes only 0.20 millisecond, including subsequent transfer of data to storage as well. The transfer to storage can take an additional 3.4 milliseconds or 0.85 millisecond, depending upon whether the store data is in Normal or Fast areas of the drum.

.7 EXTERNAL FACILITIES

The plugboard which controls the code translation can be changed in approximately 20 seconds if a new one is available, or it can be rewired in less than 20 minutes.

The parity control switch sets the unit to check a specific channel for odd or even parity, or to ignore that channel altogether.

The optional spooler holds a 500-foot reel, which can be read in 2 minutes. Changing reels takes about 1 minute. Take-up facilities are standard.

.8 ERRORS, CHECKS AND ACTIONS

Parity is checked during reading, and buffer overflow is avoided by an automatic pause, or interlock.

The following conditions effectively cause the unit to be "disabled":

- Torn tape
- Power off
- Overheating
- Improper airflow
- Plugboard not in place

INPUT-OUTPUT: PAPER TAPE PUNCH

§ 074.

.1 GENERAL

The paper tape reader and punch are two separate units housed in the same cabinet with their controller. The punch operates at 100 characters per second. Tape with five, six, seven, or eight channels can be punched, with or without parity being generated for each character, a plugboard is used to translate from six-bit biquinary code to output code. A 10-character buffer in the synchronizer is used to store the data being punched.

The program is able to test the buffer and to transfer 10 characters at a time into the computer's arithmetic registers. The time involved is 85 microseconds per transfer, or less than 0.1 percent of the overall central processor capacity.

.2 PHYSICAL FORM: . . . A sprocket drive mechanism is used.

.3 EXTERNAL STORAGE

Normal punched tape, with fully punched holes, can be used. Tapes with five, six, or seven channels can be used normally. An eight-channel tape can be used, but the eighth channel is restricted to some special function, as all other channels must be unpunched when the eighth is punched.

Various codes can be accommodated, including Teletype, Flexowriter, DaSPan, etc.

.4 CONTROLLER

The central processor functions as the controller, and only one paper-tape system can be connected to a UNIVAC SS 80/90 system. The rather unusual procedure for providing data to the punch is directly from the arithmetic registers, and 10 characters are transferred each time. The paper tape synchronizer has a 10-character buffer, which is tested to determine whether the previous operation has been completed.

.5 PROGRAM FACILITIES AVAILABLE

Punching occurs serially in sets of 10 characters. Six characters can be punched accompanied only by four blanks. The punch buffer is not automatically protected, and a program check must be made prior to loading. Translation is controlled by plug-board, and parity checking by a rotary switch. Both these controls are shared with the reader.

.6 PERFORMANCE

Both the peak and effective speeds are 100 characters per second.

.7 EXTERNAL FACILITIES

The plugboard which controls the code translation can be changed in approximately 1 minute if a new one is available, or can be rewired in less than 20 minutes.

The parity control switch sets the unit to check a specific channel for odd or even parity, or to ignore that channel altogether. An additional option is the ability to punch Teletype code.

The supply spooler has a 500-foot reel which can be punched in 10 minutes. Changing reels takes approximately 1 minute. Take-up facilities are standard.

.8 ERRORS, CHECKS AND ACTIONS

Parity is checked during reading, and buffer overflow is avoided by an automatic pause, or interlock.

Physical conditions which cause the unit to become disabled include torn paper, overheating, insufficient airflow, and no power.

INPUT-OUTPUT: HIGH SPEED PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . . High Speed Printer. Printer. Unit No. 7912.

.12 Description

The High Speed Printer has been used with UNIVAC systems since 1952. Its peak speed is 600 lines per minute, dropping to 300 lines per minute for $2\frac{1}{2}$-inch spacing of lines.

The print line can contain 100, 110, 120 or 130 positions at a pitch of 10 per inch; lines may be spaced at either 6 or 8 per inch as set by the operator.

The printer has a set of 51 characters engraved on print wheels and up to 5 carbon copies can be produced.

Inter-line spacing can be controlled only by specifying the number of line spaces between printed lines in the program. There is no form control loop and a program must count its way over pre-printed forms.

The stationery must be sprocket-punched, card or paper stock.

.13 Availability: . . . . . 10 months.

.14 First Delivery: . . . . June, 1958.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket push-pull.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . on-the-fly hammer stroke against print wheels.
.222 Sensing system: . . . . none.
.223 Common system: . . . none.

.23 Multiple Copies

.231 Maximum number Interleaved carbon at least: . . . . . 5.
Carbon creep: . . . . none.
.233 Types of master
Multilith: . . . . . special ribbon and form.
Spirit: . . . . . special form.

.24 Arrangement of Heads

Use of station: . . . . . print.
Stacks: . . . . . 1.
Heads/stack: . . . . . 100 - 130 (increments of 10).
Method of use: . . . . . line at a time.

.25 Range of Symbols

Numerals:	10	0 - 9.
Letters:	26	A - Z.
Special:	15	: , $ - # * % ; / + . & ' ( )
Alternatives:		none.
FORTRAN set:		no.
Basic COBOL set: . . .		see note.
Total:	51.	

Note: With a substitution of the apostrophe (') for the required COBOL quotation mark ("), this would be an acceptable required COBOL set.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . paper stock.
.312 Phenomenon: . . . . . printing.

.32 Positional Arrangement

.321 Serial by: . . . . . line.
.322 Parallel by: . . . . . 100 to 130 positions.

.33 Coding: . . . . . 6-bit printer code.

.35 Physical Dimensions

.351 Overall width: . . . . . 4 to 21 inches.
.352 Length: . . . . . any length is acceptable.
.353 Maximum margins
Left: . . . . . 3.5 inches.
Right: . . . . . 3.5 inches.

.4 CONTROLLER

.41 Identity: . . . . . built into Central Processor and the unit contains a special 200-word buffer band on the processor's drum which transmits the print data to the unit.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

§ 081.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 line.
.442 Input-output areas: . . buffer band.
.443 Input-output area access: . . . . . 1 band.
.444 Input-output area lockout: . . . . . locked out while Printer is printing or spacing.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 line.
.512 Block demarcation
Input: . . . . . none.
Output: . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . none.
.522 Output: . . . . . 1 line.
.523 Stepping: . . . . . feed 0-79 lines alone or as a preliminary to printing.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . none.

.54 Format Control: . . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . no.
Select format: . . . . . no.
Select code: . . . . . no.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . see Off Normal.
Busy device: . . . . . yes.
Output lock: . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: no.
Off Normal*: . . . . . yes.

* Off Normal includes: no paper.
no ribbon.
equipment malfunction.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 600 lpm.

.622 Important parameters

Name	Value
Vertical speed: . . .	20 inches/sec, max.

.623 Overhead: . . . . . number of lines spaced before printing.
.624 Effective speeds: . . . 60,000/(100 + 8 (L-1)) lines a minute.
L = average number of lines skipped per line printed.

.63 Demands on System

Component	Condition	msec per line	Percentage
Central Processor:	load buffer	10.1	10.1
Central Processor:	(note)	4.0	4.0

Note: As data must be arranged in the print interleaved pattern, 26 words must be moved.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Form tractors:	set screws	
Vertical alignment:	clutched drive	normally disengaged.

.72 Other Controls

Function	Form	Comment
Computation:	button	starts/stops Central Processor.
Paper Feed:	button light	advances paper 1 line.
Change Ribbon:	button	rewinds ribbon.
General Clear:	button light	resets error interlocks.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Bin:	1,000 sets.

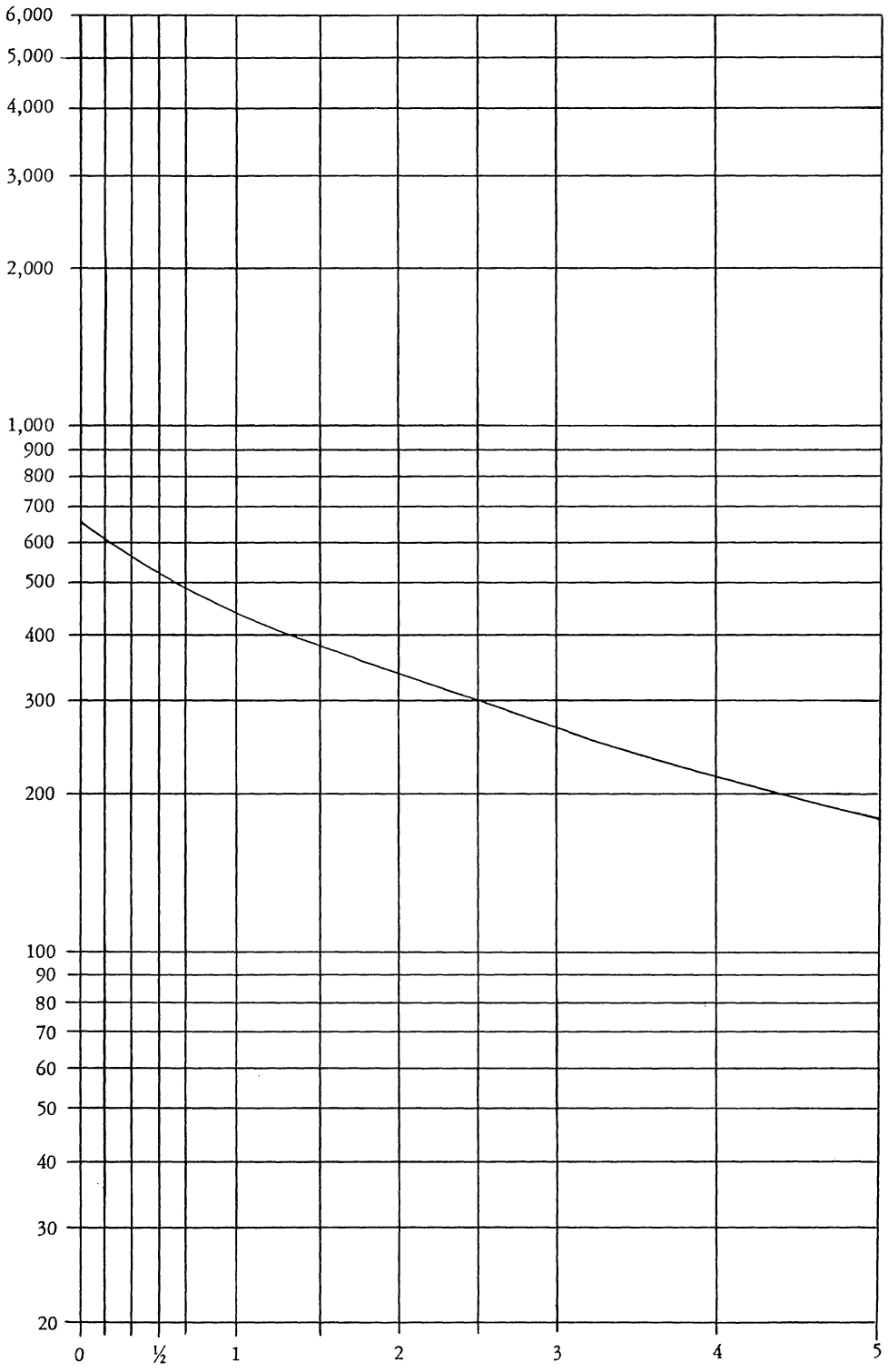
.732 Replenishment time: . . 2 to 5 minutes. printer needs to be stopped.
.733 Adjustment time: . . . 2 to 5 minutes.
.734 Optimum reloading period: . . . . . 100 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Reading:	none.	
Input area overflow:	not possible.	
Output block size:	fixed.	
Invalid code:	check	set indicator.
Exhausted medium:	see "Off Normal".	
Imperfect medium:	none.	
Timing conflicts:	interlock	wait.
Off-Normal*:	check	set indicator.

* Off Normal: includes: . . . paper feed check.
equipment malfunction.

EFFECTIVE SPEED
(Unit No. 7912)



INPUT-OUTPUT: UNISERVO MAGNETIC TAPE UNIT

§ 091.

.1 GENERAL

.11 Identity: . . . . . Uniservo Magnetic Tape Unit.
Type No. 7915.

.12 Description

The UNIVAC Solid-State system normally reads 1,100-alphameric-character blocks at an effective rate of 15,000 characters per second. (This block length is related to a band on the UNIVAC Solid-State drum, but other block lengths are possible to provide compatibility with other UNIVAC systems.)

Internally, the system uses four-bit characters, but the magnetic tape characters are 6-bits. The difference is resolved by:

(1) Upon Reading: Using two 4-bit storage characters per 6-bit tape character read.

(2) Upon Writing: Recording on magnetic tape only six bits out of each two 4-bit characters.

Some format problems result but the effective transmission rate is not reduced.

The tape is buffered into and out of the unit with an overlap of 95 percent of the elapsed time between the central processor and tape transmission. The tape buffer can also be used to move 200-word bands from one part of storage to another if no tape transmission is in progress.

The Uniservo II tape unit can be used in a variety of ways in which the tape material, packing density, block size and amplifier gain can be varied. They are used in conjunction with Synchronizers. There can be up to two Synchronizers, each of which may have up to 10 tape units connected to it. One Synchronizer may also serve any RANDEX system attached. The address of each unit can be chosen by a patch panel on its Synchronizer.

The recording can be made on metal or Mylar tapes and is compatible with UNIVAC I, II & III, File Computer, 490 and 1107. There is a special translate instruction for data in XS-3 code.

A second station is used to read-back tape and check the row parity, setting an indicator when a check fails. Three levels of amplification can be used when reading: low, normal, and high. Conventional practice is for the operator to read low to minimize noise; then, if difficulties arise, switch to normal or high on the Synchronizer. The program can also switch the level, but the operator can override its choice upward.

.12 Description (Contd.)

Extra protection is provided to the tape and head both electrostatically and mechanically by a plastic guard interposed between the tape and the heads.

A write lock-out is obtained by inserting a ring in a reel.

Only tapes that have been edited to mark the flaws should be used. Tapes are edited by first recording a pattern of "all ones" along the tape and then reading and checking. When errors occur while using metallic tape, a special hand punch is used to perforate the tape in that area. When Mylar tape is used and errors occur, its oxide is manually scraped off, leaving a clear spot on the tape. The clear spots indicate the start and end of the flaw. This operation requires at least two passes through the tape plus manual punching time.

.13 Availability: . . . . . 7 months.

.14 First Delivery: . . . . May, 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller.
.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum.
Capacity: . . . . . 6 feet of tape.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by a magnetic write head.
.222 Sensing system: . . . . magnetic read head.
.223 Common system: . . . common magnetic read/write head.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . . all tracks

Use of station: . . . . . read/write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . . all tracks read or write.

§ 091.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . metal or plastic tape.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . 1,100 or 720 or 120 frames at 125 or 250 per inch.
.322 Parallel by: . . . . . 8 tracks.
.323 Bands: . . . . . 1.
.324 Track use
Data: . . . . . 6 bits per character.
Redundancy check: . . 1 parity.
Timing: . . . . . 1 clock.
Control signals: . . . 0.
Unused: . . . . . 0.
Total: . . . . . 8.
.325 Row use
Data: . . . . . 1,100 or 720 or 120.
Redundancy check: . . 0.
Timing: . . . . . 0.
Control signals: . . . 0.
Gap: . . . . . see .622.

.33 Coding: . . . . . SS 80/90 six-bit or UNIVAC XS-3.

.34 Format Compatibility

Other device or system	Code translation
UNIVAC I, II, III: . .	XS-3 translate instruction in 80/90.
UNIVAC High Speed Printer:	special write instruction.
UNIVAC 490, 1107: .	program translation to be handled by 490/1107.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.5 inch.
.352 Length
Plastic: . . . . . 2,400 ft.
Metal: . . . . . 1,500 ft.

.4 CONTROLLER

.41 Identity: . . . . . Synchronizer. Type No. 7914.

.42 Connection to System

.421 On-line: . . . . . 1 max (Model I). 2 max (Model II).
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 10.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1,100 or 720 or 120 characters.
.442 Input-output areas: . . buffer band of 200 words.
.443 Input-output area access: . . . . . band.
.444 Input-output area lockout: . . . . . yes, and testable.
.445 Table control: . . . . . no.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1,100 or 720 or 120 characters.
.512 Block demarcation
Input: . . . . . fixed.
Output: . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . minimum 720 characters (could be six 120-character blocks with gap as delimiter).
.522 Output: . . . . . 1,100 or 720 or 120-character block, forward only.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . automatic over pre-edited marked flaws.
.525 Marking: . . . . . holes punched in tape indicate beginning and flaws.
.526 Searching: . . . . . none.

.53 Code Translation: . . . program.

.54 Format Control

Control: . . . . . program.
Format alternatives: . none.
Rearrangement: . . . . none.
Suppress zeros: . . . . none.
Insert point: . . . . . none.
Insert spaces: . . . . . none.
Recording density: . . . yes.
Section sizes: . . . . . yes.

.55 Control Operations

Disable: . . . . . yes.
Request interrupt: . . . no.
Select format: . . . . . no.
Select code: . . . . . XS-3 or SS 80/90.
Rewind: . . . . . yes.
Unload: . . . . . no.
Amplifier gain: . . . . yes (3 levels).

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Output lock: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: no.
Error type: . . . . . yes.

§ 091.

.6 PERFORMANCE

.61 Conditions

Case	Char/block	Char/inch
I:	1,100	250.
II:	720	250.
III:	1,100	125.
IV:	720	125.
V:	120	125.

.62 Speeds

.621 Nominal or peak speed

I:	25,000 char/sec.
II:	25,000 char/sec.
III:	12,500 char/sec.
IV:	12,500 char/sec.
V:	12,500 char/sec.

.622 Important parameters

Name	Value
Read start/stop 125 cpi:	18.3/16.3 msec.
Read start/stop 250 cpi:	12.1/9.2 msec.
Write start/stop 125 cpi:	12.0/11.1 msec.
Gap 125 cpi/250 cpi:	2.4/1.05 inches.

.623 Overhead: . . . . . start/stop time.

.624 Effective speeds:

I:	16,400 char/sec.
II:	13,600 char/sec.
III:	8,800 char/sec.
IV:	7,800 char/sec.
V:	2,600 char/sec.

.63 Demands on System

Component	Condition	Msec per block		Percentage
Central:				
Processor:	select unit	0.3	or	0.2 - 0.7
	load or unload buffer	3.5	or	2.6 - 7.6
	rewind	600.		

Note: When computation is to be performed on UNIVAC XS-3 coded information read from tape, the data must be converted to SS 80/90 code. Similarly, when preparing XS-3 coded information to write on tape, the inverse conversion must be programmed. The cost in either case is a subroutine which has an inside loop length of 3 instructions requiring no less than 0.2 millisecond per word using a translate instruction.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method
Metallic to Plastic:	switch

.72 Other Controls

Function	Form	Comment
Rewind:	button	rewinds tape.
Forward Backward:	2 button lights	forces direction.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel of Plastic tape:	2,400 ft. or 5,500,000 char or more at 250 pulses per inch.
Reel of Metal tape:	1,500 ft. or 2,000,000 char at 125 pulses per inch.

.732 Replenishment time: . . 1 to 6 minutes.
yes, needs to be stopped.

.733 Adjustment time: . . . 0.5 to 1.0 minute.

.734 Optimum reloading period: . . . . . 6.0 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	row parity	set indicator.
Reading:	row parity	set indicator.
Input area overflow:	not possible.	
Output block size:	not possible.	
Invalid code:	check	set indicator.
Exhausted medium:	mechanical	turns off unit.
Imperfect medium:	interlock	wait (tape passes) set indicator.
Timing conflicts:	interlock	wait.
Noise in gap:	check	set indicator.
No sprocket pulse:	check	set indicator.

SIMULTANEOUS OPERATIONS

§ 111.

The basic Model II system consists of a central processor with almost totally buffered input and output facilities, except for the limitation of only one magnetic tape per synchronizer operating at any given time. The buffering would be complete except that it takes time to actually transfer the data block from the drum buffer bands to the main drum storage area.

This transfer of a data block takes one drum revolution (3.4 milliseconds) per transfer, except for transfers to the print buffer band, which take three revolutions per transfer. The extent to which the peripheral units are used determines the load on the central processor. When all units of a card system are working, the central processor penalty is less than 5 percent.

This simultaneity between all peripheral units and the computer applies only to a basic system which has no RANDEX Drum. This uses the buffers otherwise allocated to one of the synchronizer tape units. Thus, there can be no simultaneity between reading or writing the RANDEX Units and the Magnetic Tapes on that synchronizer.

Tables

The following operations can progress simultaneously:

Processing.
Reading a card by means of High Speed Card Reader.
Reading paper tape.
Punching paper tape.
Printing a line.
Reading and/or punching a card by means of the Read-Punch Unit.
Reading or writing of a block of tape or a block from RANDEX via the RANDEX Tape Synchronizer.
Reading or writing a block of tape via the Tape Synchronizer.
Reposition any RANDEX heads not otherwise in use.
Rewinding any tape units, not otherwise in use.

INSTRUCTION LIST

§ 121.

INSTRUCTION				OPERATION
OPERATION				
ABSOLUTE	X-6 or S-4	M	C	
				ARITHMETIC
70	ADD	M	C	(M) + (rA) ⟶ (rA)
75	SUB	M	C	(rA) - (M) ⟶ (rA)
85	MUL	M	C	(rL) x (M) ⟶ (rA)
55	DIV	M	C	(M) ÷ (rL) ⟶ (rA)
				LOGIC
20	BUF	M	C	(rA) "OR" (M) ⟶ (rA)
35	ERS	M	C	(rA) "AND" (M) ⟶ (rA)
32	SHR	onoo	C	Shift (rA) and (rX) right, circular
37	SHL	onoo	C	Shift (rA) left Zero ⟶ rA LSD
62	ZUP	-	C	Zero and comma suppress (rA)
00	JMP	M	C	Jump
67	HLT	M	C	Halt, go to M or C depending on start button pushed
82	TEQ	M	C	Compare (rA) to (rL); if =, go to M; if ≠ , go to C
87	TGR	M	C	Compare (rA) to (rL); if =, go to M; if ≠, go to C
82	TEA	M	C	Compare (rA + bits 1 & 2 of rX); to (rL + bits 4 & 5 of rX); if =, go to M; if ≠ , go to C.
87	TGA	M	C	Compare (rA + bits 1 & 2 or rX) to (rL + bits 4 & 5 of rX); if = , go to M; if ≠ , go to C
				MISCELLANEOUS INTERNAL
02	LIR	M	C	M ⟶ Index Register
07	IIR	M	C	M + (Index Register) ⟶ (Index Register), and m of (rA) Zeros ⟶ balance of rA
12	CTM	-	C	Translate card to computer code
17	MTC	-	C	Translate computer to card code
C3	MTX	M	C	Translate XS-3 to computer code
C1	XTM	M	C	Translate computer to XS-3 code
				DATA TRANSFER
25	LDA	M	C	(M) ⟶ (rA)
60	STA	M	C	(rA) ⟶ (M)
05	LDX	M	C	(M) ⟶ (rX)
65	STX	M	C	(rX) ⟶ (M)
30	LDL	M	C	(M) ⟶ (rL)
50	STL	M	CQ	(rL) ⟶ (A)
77	ATL	-	C	(rA) ⟶ (rL)
26	CLA	M	C**	0 ⟶ (rA)
31	CLL	M	C**	0 ⟶ (rL)
06	CLX	M	C**	0 ⟶ (rX)
36	CAA	M	C**	0 ⟶ (rA), save sign
86	CAX	M	-	0 ⟶ (rA), and (rX)

§ 121.

INSTRUCTION LIST (Contd.)

INSTRUCTION				OPERATION
OPERATION				
ABSOLUTE	X-6 or S-4	M	C	
23	CTA	M	-	(rC) ⟶ (rA)
90	SML	M	C	M.S.D. of (M) ⟶ Sign of (rL)
F0	SMA	M	C	Sign of (M) ⟶ M.S.D. of (rA)
B8	TCD	M	C	1 to 200 words of Core ⟶ Drum
B0	TDC	M	C	1 to 200 words of Drum ⟶ Core
05	LSX	M	C	(Bits 1 & 2 of M) ⟶ (Bits of 4 & 5 of rX)
06	ZSR	M	C**	0 ⟶ Subregisters 3 and 4 of rX; sign +.
				CARD READ-PUNCH
81	RCC	aa00	C	Load punch buffer with binary image from band aa
81	RCC	aa01	C	Load punch buffer translating the band aa machine code to card image
46	RBU	aa00	C	Unload punch buffer transferring the binary image to band aa
46	RBU	aa01	C	Unload punch buffer translating to machine code into band aa
22	RBT	M	C	Test buffer; if loaded, go to M, (rC) ⟶ (rA); if not, go to C
57	RSS	-	C	Select Stacker
				HIGH SPEED READER
72	HCC	M	C	Feed Card; if interlocked, go to M & (rC) ⟶ (rA); if not, go to C
96	HBU	aa00	C	Unload buffer with binary image into band aa
96	HBU	aa01	C	Unload buffer translating to machine code into band aa
42	HBT	M	C	Test buffer; if loaded, go to M & (rC) ⟶ (rA); if not, go to C
47	HSS	0a00	C	Select stacker a
				HIGH SPEED PRINTER
11	PRN	aann	C	Feed nn lines loading the print buffer from band aa
16	PFD	00nn	C	Feed nn lines
27	PBT	M	C	Test printer; if free, go to M, (rC) ⟶ (rA); if not, go to C
				MAGNETIC TAPE
C2	TST	M	C	Synchronizer test; if free, go to M & (rC) ⟶ (rA); if not, go to C
C6	TBL	aa00	C	Load tape buffer from band aa (Drum)
C7	TBT	M	C	Buffer Test; if free, go to M & (rC) ⟶ (rA); if not, go to C
F2	TRW	0a00	C	Rewind tape a
F2	TRW	0a20	C	Rewind and disable tape a
F6	TBU	aa00	C	Transfer contents of tape buffer to band aa
G2	TRD	0abc	C	Read block from tape a, mode and density b, direction and gain C
H2	TWR	0ab0	C	Write block on tape a, mode and density b
C6	TBL	BXXX	C	Load tape buffer from core, where BXXX is beginning word address
FX	TLB	BXXX	C	Transfer contents of tape buffer to core address BXXX. BXXX is beginning word address (core)

** If next instruction is to be found in core, then "M" and "C" must be same address.

§ 121. INSTRUCTION LIST (Contd.)

INSTRUCTION				OPERATION
OPERATION				
ABSOLUTE	X-6 or S-4	M	C	
				RANDEX
40	LSR	M	C	Load Synchronizer Instruction Register
18	PDH	M	C	Position Head
92	DBT	M	C	Test HPFF, if set go to M; if not, go to C
43	DPT	M	C	Test head position; if positioned, set HPFF
28	DWT	M	C	Write a record
38	DRD	M	C	Read a record
48	DWC	M	C	Write and check a record
58	DSW	M	C	Find record and write
68	DSR	M	C	Find record and read
F6	TBU	aa00	C	Transfer contents of tape buffer to band aa
C6	TBL	aa00	C	Transfer contents of band aa to tape buffer
C7	TBT	M	C	Test Tape buffer: if free, rC ⟶ rA and go to M; if not, go to C
C2	TST	M	C	Test Synchronizer: if free, rC ⟶ rA and go to M; if not, go to C
				N. B. 1. There are 4 special registers: rA: Accumulator rC: Command (complete instruction) rL: Lower accumulator rX: Used for comparisons and code conversions 2. Next instruction specified by C unless otherwise stated.

CODING SPECIMEN: S-4

§ 131.

.1 TRANSLATOR LISTING

CD NO.	LOCA.	OP	MMMM	CCCC	S	SYM A	OP	IR	SYM M	SYM C	remarks
1			0000	4999			BLR		0000	4999	
2			0400	0700			BLA		0400	0700	
3	0400	25	0402	0404		RANGE	LDA		X		
4	0404	30	0406	0408			LDL		CCO7		
5	0408	87	0400	0611			TGR		OUT		
6	0611	82	0414	0614			TEQ		EQU		
7	0614	30	0416	0418			LDL		CCO5		
8	0418	87	0421	0621			LGR		IN		
9	0621	82	0414	0411			TEQ		EQU	OUT	
10	0416		00000	00005		CCO5				5	
11	0406		00000	00007		CCO7				7	
12	0414	67	0005	0414		EQU	HLT		0005	EQU	
13	0411	67	0006	0411		OUT	HLT		0006	OUT	
14	0421	67	0004	0421		IN	HLT		0004	IN	

Without Forward Search

1			0000	4999			BLR		0000	4999	
2			0400	0700			BLA		0400	0700	
3	0400	25	0402	0404		RANGE	LDA		X		
4							HED		B		
5	0404	30	0406	0408			LDL		CCO7		
6	0408	87	0424	0411			TGR		OUT		
7	0411	82	0624	0414			TEQ		EQU		
8	0414	30	0416	0418			LDL		CCO5		
9	0418	87	0421	0621			TGR		IN		
10	0621	82	0624	0424			TEQ		EQU	OUT	
11	0416		00000	00005		CCO5				5	
12	0406		00000	00007		CCO7				7	
13	0624	67	0005	0624		EQU	HLT		0005	EQU	
14	0424	67	0006	0424		OUT	HLT		0006	OUT	
15	0421	67	0004	0421		IN	HLT		0004	IN	

With Forward Search

The listings on the right show the symbolic coding; those on the left show the final machine coded program. The path of the program goes from RANGE to the three possible end-points IN, OUT, or EQUAL. Two of these, EQU and OUT, can be reached from two separate points in the program sequence.

When Forward search is not used, these are allocated as soon as the first point is reached, wasting a drum revolution each time the second path is taken. With Forward search, the allocation starts with the later path, and the delay is reduced to 13-word times (as against 187 in the former case).

DATA CODE TABLE NO. 1

§ 141.

.1 USE OF CODE: . . . . . internal and printer.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 6 bit (split between two words: Most significant = zone or unprimed. Least significant = numeric or primed).

.22 Character Structure

.221 More significant pattern: . . . . . 2 bits values for pattern 16, 32, 0, 0.

.222 Less significant pattern: . . . . . 4 bits values for pattern 1, 2, 4, 8.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MOST SIGNIFICANT PATTERN			
	0	16	32	48
0	0	NO PRINT		+
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	-	.	$	,
6	Space	:	*	%
7	)	&		
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H.	Q	Y
12	9	I	R	Z
13	(			
14	;			
15	'	#		

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE: . . . . . XS3 use to communicate with other Univac Machines.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 6 bit:
Most significant = zone or unprimed.
Least significant = numeric or unprime.

.22 Character Structure

.221 More significant pattern: . . . . . 2 bits: 16, 32.

.222 Less significant pattern: . . . . . 4 bits: 1, 2, 4, 8.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0				
1	Space	,	"	
2	-	.		:
3	0	;	)	+
4	1	A	J	/
5	Z	B	K	S
6	3	C	L	T
7	4	D	M	U
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H	Q	Y
12	9	I	R	Z
13	'	#		
14	&			
15	(			

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . . In reading or punching cards with non-standard punching.

.2 STRUCTURE OF CODES

80-Column

The 80-column punched card is represented in the computer as 24 words. Each group of 10 columns forms a data word of 3 images called the unprimed, primed and duo-primed images. Each image is a computer word and is an exact representation of the holes appearing on a particular section of the card - a punch equals a "1" bit. The signs of all images are positive.

Rows								
Y	Word	Word	Word	Word	Word	Word	Word	Word
X	0	1	2	3	4	5	6	7
0	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit
1	chars)	chars)	chars)	chars)	chars)	chars)	chars)	chars)
2	Word	Word	Word	Word	Word	Word	Word	Word
3	0'	1'	2'	3'	4'	5'	6'	7'
4	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit
5	chars)	chars)	chars)	chars)	chars)	chars)	chars)	chars)
6	Word	Word	Word	Word	Word	Word	Word	Word
7	0"	1"	2"	3"	4"	5"	6"	7"
8	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit	(10 4-bit
9	chars)	chars)	chars)	chars)	chars)	chars)	chars)	chars)
Columns	1-10	11-20	21-30	31-40	41-50	51-60	61-70	71-80

90-Column

The 90-column punched card is represented in the Central Processor as 20 words. Each group of 10 columns forms a data word of 2 images called the umprimed and the primed images or a word-pair. (Columns 41-45 and 86-90 are each treated as 10-column groups and are placed into the 5 least significant digit positions in the computer words.) Each image is a computer word and is an exact representation of the holes appearing on a particular section of the card - a punch equals a "1" bit. The signs of all images are positive.

Row					
0 1 3 5	0	1	2	3	4
7 9	0'	1'	2'	3'	4'
Columns	1-10	11-20	21-30	31-40	41-45
0 1 3 5	5	6	7	8	9
7 9	5'	6'	7'	8'	9'
Columns	46-55	56-65	66-75	76-85	86-90

§ 143.

.3 EXAMPLES (80-Column card)

Card Column		11	12	13	14	15	16	17	18	19	20
Alphabetic Character		K	L	M	N	O	P	Q	R	S	T
	Card Row										
10-digit Unprimed Word	Y	0	0	0	0	0	0	0	0	0	0
	X	1	1	1	1	1	1	1	1	0	0
	0	0	0	0	0	0	0	0	0	1	1
	1	0	0	0	0	0	0	0	0	0	0
10-digit Primed Word	2	1	0	0	0	0	0	0	0	1	0
	3	0	1	0	0	0	0	0	0	0	1
	4	0	0	1	0	0	0	0	0	0	0
	5	0	0	0	1	0	0	0	0	0	0
10-digit Duo-primed Word	6	0	0	0	0	1	0	0	0	0	0
	7	0	0	0	0	0	1	0	0	0	0
	8	0	0	0	0	0	0	1	0	0	0
	9	0	0	0	0	0	0	0	1	0	0

Note:

Holes would appear in the punched card wherever a "1" occurs in the above table.

In bi-quinary, the three words would be:

Unprimed word: 4 4 4 4 4 4 4 4 2 2

Primed word: 5 4 2 1 0 0 0 0 5 4

Duo-primed word: 0 0 0 0 5 4 2 1 0 0

DATA CODE TABLE NO. 4

§ 144.

.1 USE OF CODE: . . . . comparisons.

.2 NUMERIC CODE

(in ascending sequence)

0
1
2
3
4
Undigit A
Undigit B
Undigit C
5
6
7
8
9
Undigit F
Undigit G
Undigit H

.3 ALPHAMERIC CODE

(in ascending sequence)

0	A	J	/
1	B	K	S
2	C	L	T
3	D	M	U
4	.	$	,
-	:	*	%
Space	&	N	V
)	E	O	W
5	F	P	X
6	G	Q	Y
7	H	R	Z
8	I	+	
9	#		
(			
;			

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . none.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

SR 012
Reference: . . . . . SR012.
Record size: . . . . . 1 to 100 words.
Block size: . . . . . 100 words.
Key size: . . . . . 1 to 12 words.
File size: . . . . . 4,800 block reel.
Number of tapes: . . 4 to 10.
Date available: . . . currently.
Description:

SR012 accepts as input a file of 12-word items in the standard interlace from a tape written in USS mode. It produces as output the same items in sequence, in the standard interlace, on a tape written in USS mode. One full reel may be sorted at a time; however, the input data may appear on more than one tape. Both input and output tapes adhere to standard tape conventions (labels, sentinels, block counts, etc.).

Similar routines are available for 5, 10, 25, and 50 word items.

.14 Report Writing: . . . . none.

.15 Data Transcription: . . a body of input-output routines are available which can be easily connected for data transcription purposes.

.16 File Maintenance: . . . none.

.17 Other

Program testing procedures, and a tape input-output system (Mascot II) are available. A series of mathematical function routines are available.

.2 PROBLEM ORIENTED LANGUAGES

A linear programming package is available.

MACHINE-ORIENTED LANGUAGE: S-4

§ 171.

.1 GENERAL

.11 Identity: . . . . . S - 4

.12 Origin: . . . . . UNIVAC Division.

.13 Reference: . . . . . S-4 Assembly, General Manual.
UP - 1774-6, Revision I.
S-4 Assembly For 90 Card Configuration.
UP-1774.7

.14 Description

The S-4 assembler is the standard assembler for UNIVAC Solid-State systems, Models I and II. S-4 is machine oriented, its decimal operands being arranged in 10-digit fixed point words exactly as in the normal machine instruction.

S-4 is an assembly language which produces one machine instruction for each symbolic instruction. However, S-4 contains a set of 20 controls which are independent of the machine language and provide various facilities at assembly time. An S-4 programmer can use these controls to relieve himself of the machine language coding problems.

These facilities are of two types:

- Allocation Controls, which, while comprehensive, do not provide the same result as hand coding.
- Compatibility Controls.

Allocation Control

Model I systems use magnetic drums as basic storage and have a minimum of two levels of storage. Model II systems also have core stores, while a tape system uses the tape buffer. The efficiency of any program depends more on the allocation of operands to storage than on the actual instructions. A well-allocated add instruction (one optimized as to the number of word cycles that must elapse before the operand is available) takes 85 microseconds. Normally, this instruction takes 20 times as long, and, in the worst case, it would take 80 times as long.

S-4 provides three levels of allocation control to the programmer: provisional, general, and by exception. At the first level, each label contains a character position which defines the label as being provisionally allocated to either normal or fast drum storage, or to core storage. In any part of a program, these provisional labels can be overridden (the second level of control). Thus, allocations coded for the normal drum access are forced into fast access, but the reverse is not true. The third control level is provided for situations in which the provisionally

.14 Description (Contd.)

Allocation Control (Contd.)

selected allocation cannot be made optimal. When this condition exists, the programmer has a choice of using a higher level store to attempt to obtain optimal allocation before accepting a non-optimal allocation.

Compatibility Controls

S-4 provides for compatibility with both actual programs and symbolic programs.

The compatibility with actual programs comes from the design of the Availability Table. This table is a storage map which indicates to the assembler which positions are available for allocation. At any time in the program, this allocation can be changed by reading in a new availability table. The change can be a complete or partial replacement of the availability table or the addition of reservations. Similarly, the whole table can be punched out as needed to allow for similar subsequent uses, permitting:

(1) Existing programs to have their own availability tables to be read in, and therefore reserved, prior to an assembly.
(2) Overlays to be created at any position in the assembly.

Symbolically, programs can be merged into assembly programs either by physically adding cards or by calling the programs to be added from a tape unit.

The S-4 language itself is a simple representation of the standard machine instructions. Thus, ADD is the mnemonic used for 70, the addition machine code. Similar to the machine instruction, the S-4 representation must have a location, an operation code, an operand address, and a next instruction address. However, the programmer's job in keeping track of the addresses is eased by:

(1) Using blanks if the address is obvious and will not be referred to again.
(2) Using "Local Reference Points" (up to 20 can be operational at a given time) to denote points which are only of local importance; that is, normally within 20 to 50 lines of coding.
(3) Using Temporary Tags for all those labels which are only used within a segment of the program.
(4) Using specialized labels for each word of the input-output areas defined in the program, and for the registers.
(5) Using specialized tags for tables (up to 30 of these can be defined at any one point).

.15 Publication Date: . . . 1962.

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.2 LANGUAGE FORMAT

LINE	LINE NO.	SYMBOLIC "A"	OPERATION CL	OPERATION Symbolic	IR	SYMBOLIC "M"	SYMBOLIC "C"
	13 14 15 16	46 47 48 49 50	51	52 53 54	55	56 57 58 59 60	61 62 63 64 65

.22 Legend

LINE: . . . . . line of coding on the coding sheet.

LINE NO: . . . . . line number optionally allocated by programmer, always reallocated by the translator.

SYMBOLIC a: . . . . location of the instruction in the store. May be in absolute or symbolic form.

OPERATION: . . . . defines the type of constant which follows; or is the instruction in symbolic form.

IR: . . . . . Index Register Modification, if it is to be used.

SYMBOLIC m: . . . . the address of an operand, in symbolic or absolute form.

SYMBOLIC c: . . . . the address of the next instruction, in symbolic or absolute form.

SYMBOLIC m & c combined: . . . . . 10 digits, to be treated as an absolute constant.

WORD TIME: . . . . 3 digit number which directs the compiler as to time to be allowed to the instruction.

.23 Corrections

Insertions, deletions, and corrections can be made by altering the original coding. Special pseudo operations are available in the language which make it unnecessary to do more than nominate what parts of a previous assembly should be omitted and require the programmer to provide only full details of any additions (including changes).

.24 Special Conventions

A number of conventions are used to simplify programming or assembly, which add considerably to the writing speed, ease of insertions, etc. in addition to readability.

BLANKS are used in the location, the operand and/or the next instruction addresses within each instruction when normal sequencing is desired.

Constants can be given in some simple form, with an additional instruction (a designator) as to what part of the given constant is wanted. These instructions include:

for I/O codes: Unprimed, primed, or double primed; numeric or zone portions.

for general use: either the negative or the reciprocal of the given instruction.

.3 LABELS

.31 General

Labels are used in S-4 to define parts of a program and units of the computer. In general, five alphameric characters are used to provide a label, and the fact that specific positions either are or are not numeric distinguishes one type of label from another. Position of characters in label fields is critical.

.32 Universal Labels

.321 Labels for instructions

Existence: . . . . . optional.

Formation rule

First character: . . must not be numeric.

Last character: . . designating type of storage (i.e., fast or normal drum or core) for provisional allocation or overflow control.

Others: . . . . . alphameric.

Number of characters: . . . . . 5.

.323 Labels for constants or variables: . . . . same as instructions.

.324 Labels for files or records: . . . . . no; but there are labels reserved for I/O areas.

.327 Labels for regions and tables

Existence: . . . . . yes; i.e., A Δ Δ Δ Δ

Formation rule

First character: . . alphabetic character.

Others: . . . . . 0000 to 9200.

Number of characters: . . . . . 1 label, 4 element.

.33 Local Labels

Temporary labels are used extensively in S-4. The three methods of writing them are:

1) Local Reference Points, which are constantly redefined. These are numbered 1 through 9 and 0, and a reference applies to the nearest reference point in the indicated direction.

2) Temporary Tags. These differ in formation from permanent tags (They have numerics in the center of the tag; e.g., B123N) and are all cleared at once from the symbol table by a control card.

3) Permanent Tags. However, any permanent tag can be made local by clearing it from the symbol table, and then redefining it as the new value.

§ 171.

.333 Labels for library routines
Formation rule
First character: . . must not be numeric.
Last 2 characters: . . . . . designating type of storage for provisional allocation.
Others: . . . . . numeric.
Number of characters: . . . . . 5.

.4 DATA

.41 Constants

.411 Maximum size constants or literals: . . 10 hexadecimal or decimal digits or one part.
10 alphabetic characters (i.e., numeric or zone portion).

.42 Working Areas: . . . . . complied by use, or by definition as reserved or table areas.

.43 Input-Output Areas

.431 Data layout: . . . . . controlled by parameters preset for units connected to system.

.5 PROCEDURES

.51 Direct Operation Codes

All machine codes are given mnemonic codes, such as ADD, LDA (Load Register A). These, or their absolute equivalents, can be used interchangeably.

.52 Macro-Codes: . . . . none.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control: . . a large number of pseudo operation codes give direct control over the translator. In addition, the translator includes a load feature, which allows its own tables to be overwritten by new data in the middle of an assembly.

.542 Allocation counter
Set to absolute: . . . yes.
Set to label: . . . . yes.
Step forward: . . . yes.
Step backward: . . . yes.
Reserve area: . . . yes.

.543 Label adjustment
Set labels equal: . . yes.
Set absolute value: . . yes.
Clear label table: . . yes, local, relative and specific permanent labels can be cleared separately.

.544 Annotation
Comment phrase: . . yes.
Title phrase: . . . . yes.

.545 Other
Allocation is handled by three methods.

(1) Explicity. Each label is coded to indicate whether it should be placed in core storage, or onto the fast access or normal access portion of the drum.

(2) By policy statements which overrule the explicit statements. Special pseudo codes are available which cause the translator to allocate core store, or fast store to all subsequent labels despite the allocation instruction implicit in the actual label. (This is very helpful when utilizing subroutines.)

(3) By directing the translator to leave a specific amount (entered in the word time column on the coding sheet) of time between particular instructions. This provision overrules the amount of time which would be generally used for the specific instruction.

.6 SPECIAL ROUTINES AVAILABLE: . . . . none in S-4 language.

.7 LIBRARY FACILITIES

Libraries can be created and held on magnetic tape. These libraries consist of regular S-4 programs, and are called in by naming the first and last statement number which is to be incorporated into the assembly and the tape unit where it is to be found. No program is named by these instructions, and it is the responsibility of the programmer to position the tapes correctly.

A special Constants Library facility is available during assembly. All library constants are read and their labels checked against the list of labels. If the label has been used previously in the program, the value of the constant is entered. If no such use has been made, no entries are created in the object program.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . . none.

.82 Pseudos

ASSEMBLY CONTROL PSEUDO OPERATION

RST: . . . . . Initialize for Assembly.
END: . . . . . End Card Output.

STORAGE ALLOCATION PSEUDO OPERATIONS

BLR: . . . . . Block Reservation.
BLA: . . . . . Block Availability.
REG: . . . . . Regional Specifications, providing labels and reading space.
INT: . . . . . Interlace Pattern Reserve, revising an I/O and providing labels.
SYN: . . . . . Synonym.

§ 171.

.82 Pseudos (Contd.)

ALLOCATION-CONTROL PSEUDO OPERATIONS

HED B:	Initiate Forward Search.
HED A:	End Forward Search.
HED D:	Extend in High-Speed Memory.
HED H:	Extend in Core Memory.
HED E:	Terminate HED D and HED H Functions.
HED F:	Assign High-Speed Storage.
HED G:	Assign Core Storage.
HED J:	High-Speed Tags to Core Storage.
HED N:	Cancel effect of HED F, G, and I.
HED Z:	Allocate in Normal Speed Storage. Execute in High Speed Storage.
HED Y:	Terminate HED Z Control.
WDT:	Word-Time Control.

TAG TABLE CONTROL PSEUDO OPERATIONS

EQU:	Equivalence.
HED C:	Clear Temporary Tag Table.

.82 Pseudos (Contd.)

TAPE ASSEMBLY PSEUDO OPERATIONS

HED T:	Accept Tape Input, from indicated tape.
HED I:	Rewind Input Servo. from indicated tape.
HED O:	Rewind Output Servo.

CONSTANT LIBRARY PSEUDO OPERATIONS

HED L:	Process Constant Library, inserting any constants which have been called.
HED K:	End Constant Library Processing.

PROGRAM TESTING PSEUDO OPERATIONS

HED X:	Printer Output.
HED M:	Tape Output.
HED P:	Resume Punch Output.
PPA:	Print and Punch the Availability Table.
PAT:	Print Availability Table.
SYP:	Print Symbol Table.

PROGRAM TRANSLATOR: S-4

§ 181.

.1 GENERAL

.11 Identity: . . . . . S-4 80 Card Assembly System.
S-4 80 Card-Tape-Core Assembly System.
S-4 90 Tape-Core Assembly System.

.12 Description

The most interesting factor about the S-4 Translator relates to the source card design. The input is keypunched into the second half of the card and is reproduced in the same relative position on output. During input the first half of the card is ignored; however, the output object program is punched into it. As a result:

(1) The output deck contains a complete, up-dated record of machine code and symbolic code, in addition to comments. The output deck is therefore independent of the input deck, which can be discarded or dispersed to its original sources. Up-to-date documentation, particularly of new routines, is therefore much easier to obtain simply by listing the object program deck.

(2) As the actual input area of the card does not coincide with the input area of the other UNIVAC Solid State Assembly System, X-6, one card can hold a code in both languages. Thus, routines can be issued which are suitable for compilation by either the S-4 or the X-6 assembly.

The assembly time for the S-4 is computer-limited. Tape or card input-output can be used, and translation speeds of approximately 60 instructions per minute can be obtained under favorable circumstances. These speeds are drastically reduced when the drum is filling up. A single large assembly can require an hour.

The object program is "optimized" by using the first available location whenever a new allocation has to be made. Normally, this is done in a forward direction, which means that no other point is referenced. However, the method has three disadvantages:

(1) In a program relying heavily on subroutines, parts of the drum can become unnecessarily crowded, causing delays in other parts of the program because of latency.

(2) If a location is jumped to from a number of positions, it is "optimized" as relative to the first jump encountered, even if this results in nearly the worst possible latency time for all other entries, (which often happens.)

12 Description (Contd.)

(3) When two or more variables which are to be considered for allocation to a particular position are considered, space allocation is provided on a first come, first served basis. This allocation gives fair, but far from the best results.

The S-4 Translator includes "Forward Search," a facility which, if carefully used, can reduce the impact of the first two disadvantages just enumerated. This facility allocates space backwards from the next fixed point. This allocation tends to be random, relieves the overcrowding, and optimizes on the last of a series of exits. A group of a maximum of 10 instructions can be handled at any one time.

S-4 Translators differ according to the machines on which they are run, or basically according to the following characteristics:

- Whether 80-column or 90-column cards are used.
- Whether the system is the Model I or Model II.
- Whether the minimum drum size is 2,600, 5,000, or 8,800 words.
- Whether the system is a card or tape system.

It can be seen that there are 24 possible basic configurations, and it is not surprising that some of them have been omitted. What is surprising is that the Model II users, who have no other assembly system available, have a very restricted choice. Only two versions are available:

(1) If a user's drum capacity is less than 5,000 words, a specialized, restricted version of the language must be used.

(2) If a user's drum capacity is 5,000 words or more, the Model I 5,000-word drum version can be used, which means that during the compilation, programs can utilize only the 5,000-word drum, and can make no use of the core.

.13 Originator: . . . . . UNIVAC Division.

.14 Maintainer: . . . . . UNIVAC Division.

.15 Availability: . . . . . April, 1962.

.2 INPUT

.21 Language

.211 Name: . . . . . S-4.
.212 Exemptions: . . . . . variable for different versions.

§ 181.

.22 Form

.221 Input media: . . . . . punched cards. magnetic tape.
.222 Obligatory ordering: . . program sequence.
.223 Obligatory grouping: . . no.

.23 Size Limitations

.231 Maximum number of source and data statements: . 1 per word available in store.
.232 Maximum size source statements: . . . . . 1 card.

.3 OUTPUT

.31 Object Program

The object program is put out both in machine language code and in symbolic S-4 coding. The latter is suitable for re-entry during an updating run.

The output can be punched into cards (one card per instruction) or recorded on magnetic tape (one tape block per instruction).

.32 Conventions

It is assumed that specific loaders will be used to load the output deck.

.33 Documentation

The source and object programs are listed side-by-side, including indications of the errors.

Details of the symbol table and a storage map are provided by inserting the appropriate control cards.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes: . . one pass only through the source program is required.

.42 Optional Mode

.421 Translate: . . . . . yes.
.422 Translate and run: . . . no.
.423 Check only: . . . . . yes, by omitting punching the object program.
.424 Patching: . . . . . yes, provided the object program is on tape.
.425 Updating: . . . . . yes, as for patching.

.43 Special Features

.431 Alter to check only: . . yes, by halting output of object program.
.432 Fast translate, by omitting the Forward Search feature: . . . . yes.
.433 Short translate on restricted program: . no.

.44 Bulk Translating: . . . yes, Re-Set card inserted between decks automatically causes re-initialization.

.45 Program Diagnostics: . none can be inserted directly, but the object program can be made compatible with the standard diagnostic programs.

.46 Translator Library: . . none.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . normally 200 words for loader.
.513 Approximate expansion of procedures: . . . . 1-for-1 correspondence between input and output.

.52 Translation Time

	Instruction Per Minute	
	Card System	Tape System
.521 Normal translating, including FORWARD SEARCH:	20 down to 5	25 down to 10.
.522 Checking only:	100 down to 10	120 down to 10.
.523 Translating without FORWARD SEARCH:	70 down to 10	90 down to 10.

The number instruction per minute decreases as the store fills, therefore requiring that the tables be searched more before allocation can take place.

.53 Optimizing Data

The assembler allocates the nearest-to-optional location available whenever it comes to a previously unallocated symbol. This allocation is made under control of the programmer's general instructions as to which level of store should be used.

In estimating where such a location could be, the assembler uses either the maximum instruction times for the specific instruction or the time given with the instruction.

When FORWARD SEARCH is in progress, this allocation is finally made backwards, which tends to prevent uneven distribution of data around the drum, and prevents the loss of a cycle in some simple branch and rejoin operations. The effect of FORWARD SEARCH overall has not been determined and it is unlikely to lead to an improvement in running time of more than 20 per cent.

.54 Object Program Performance

With full utilization of the 12 different control operations, FORWARD SEARCH, and of the Word Time column on the coding sheet, timing efficiency should approximate 90 per cent at the start of an assembly and drop to about 70 per cent when the store is nearly full.

With only simple coding, the efficiency factors are probably 75 per cent and 50 per cent under the same circumstances.

§ 181.

.54 Object Program Performance (Contd.)

The loss of efficiency, even in the best care, occurs because the assembler is unable to judge the comparative costs of and value of the allocation it makes, and therefore cannot juggle them around to obtain optional overall performance.

The object program requires no more space than machine code programmer's does.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: UNIVAC Solid-State Model I with 5,000 word drum (either SS 80 or SS 90 systems can be used).

.612 Larger configuration advantages:. . . . . magnetic tapes give faster compilation and better reassembly and library facilities.

.62 Target Computer

.621 Minimum configuration: any UNIVAC Solid-State system.

.622 Usable extra facilities: card reader, card punch, and printer.
core storage for UNIVAC Solid-State II system.
RANDEX units.
Paper Tape units.

.7 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	none.	
Duplicate names:	none.	
Improper format: / Incomplete entries:	various checks, to ensure apparently valid entry.	error rotation on output.
Target computer overflow:	check	fictitious entry placed in all positions.
Inconsistent program:	none	assembly continues.

OPERATING ENVIRONMENT

§ 191.

.1 GENERAL

.11 Identity: . . . . . no integrated system available.

.12 Description

No comprehensive supervisor system has been published or announced for the UNIVAC Solid-State Systems. The facilities described in this section must be covered by incorporating specific routines in each program.

Normally, one 200-word band on the drum is reserved for loaders, dumps, traces, etc., and is not used for the actual program.

.13 Availability: . . . . . presently available.

.14 Originator: . . . . . various.

.15 Maintainer: . . . . . UNIVAC Division of Sperry Rand.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Libraries: . . . . . can be held on cards and physically chosen, or held on tape and be loaded under control of the tape control system.

.212 Independent programs: . loaded from card and tape.

.213 Data: . . . . . normally via card reader, possible via Read/Punch unit, or via tape.

.214 Master routines: . . . as for independent programs.

.22 Library subroutines: . . . can be inserted at translation time using the S-4 or X-6 library facilities, if they are written in the appropriate symbolic language; otherwise must be treated as independent programs.

.23 Loading Sequence: manual sequencing of card decks or program tapes.

.3 HARDWARE ALLOCATION: . . . as incorporated in user's program.

.4 RUNNING SUPERVISION: . . . as incorporated in user's program.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . instruction-by-instruction trace available, provided 1 complete 200-word band on the drum is reserved.

.512 Snapshots: . . . . . not available.

.52 Post Mortem: . . . . available provided 1 complete 200-word band on the drum is reserved. (This band may be the same one used for loaders and for tracing).

.6 OPERATOR CONTROL: . . . . as incorporated in user's program.

.7 LOGGING: . . . . . as incorporated in user's program.

.8 PERFORMANCE

.81 System Requirements

.813 Reserved equipment: . . . . . normally the first 200 words of the drum.

.82 System Overhead

.821 Loading time: . . . . condensed card decks at 3,200 instructions or constants per minute. Program tapes at 90,000 instructions per minute after the tape has been positioned.

UNIVAC SS 80/90 MODEL II
SYSTEM PERFORMANCE

UNIVAC SS 80/90 MODEL II SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 1						
Worksheet	Item		Configuration			Reference
			All			
1 INPUT-OUTPUT TIMES	Char/block	(File 1)	1,000			4:200.112
	Records/block	K (File 1)	8			
	msec/block	File 1 = File 2	67			
		File 3	100			
		File 4	133			
	msec/switch	File 1 = File 2	---			
		File 3	---			
		File 4	---			
	msec penalty	File 1 = File 2	3.4			
		File 3	3.4			
		File 4	10.2			
2 CENTRAL PROCESSOR TIMES	msec/block	a1	9.2			4:200.1132
	msec/record	a2	7.2			
	msec/detail	b6	8.0			
	msec/work	b5 + b9	16.5			
	msec/report	b7 + b8	36.0			
3 STANDARD PROBLEM A F = 1.0	msec for C. P. and dominant column.	a1	C. P. 9.2	Printer		4:200.114
		a2 K	57.6			
		a3 K	480.0			
		File 1 Master In	3.4			
		File 2 Master Out	3.4			
		File 3 Details	27.2			
		File 4 Reports	83.0	1,133		
		Total	663.0	1,133		
4 STANDARD PROBLEM A SPACE	Unit of measure	(Word)				4:200.1151
		Std. routines	550			
		Fixed	200			
		3 (Blocks 1 to 23)	300			
		6 (Blocks 24 to 48)	240			
		Files	440			
		Working	100			
		Total	1,830			

SYSTEM PERFORMANCE

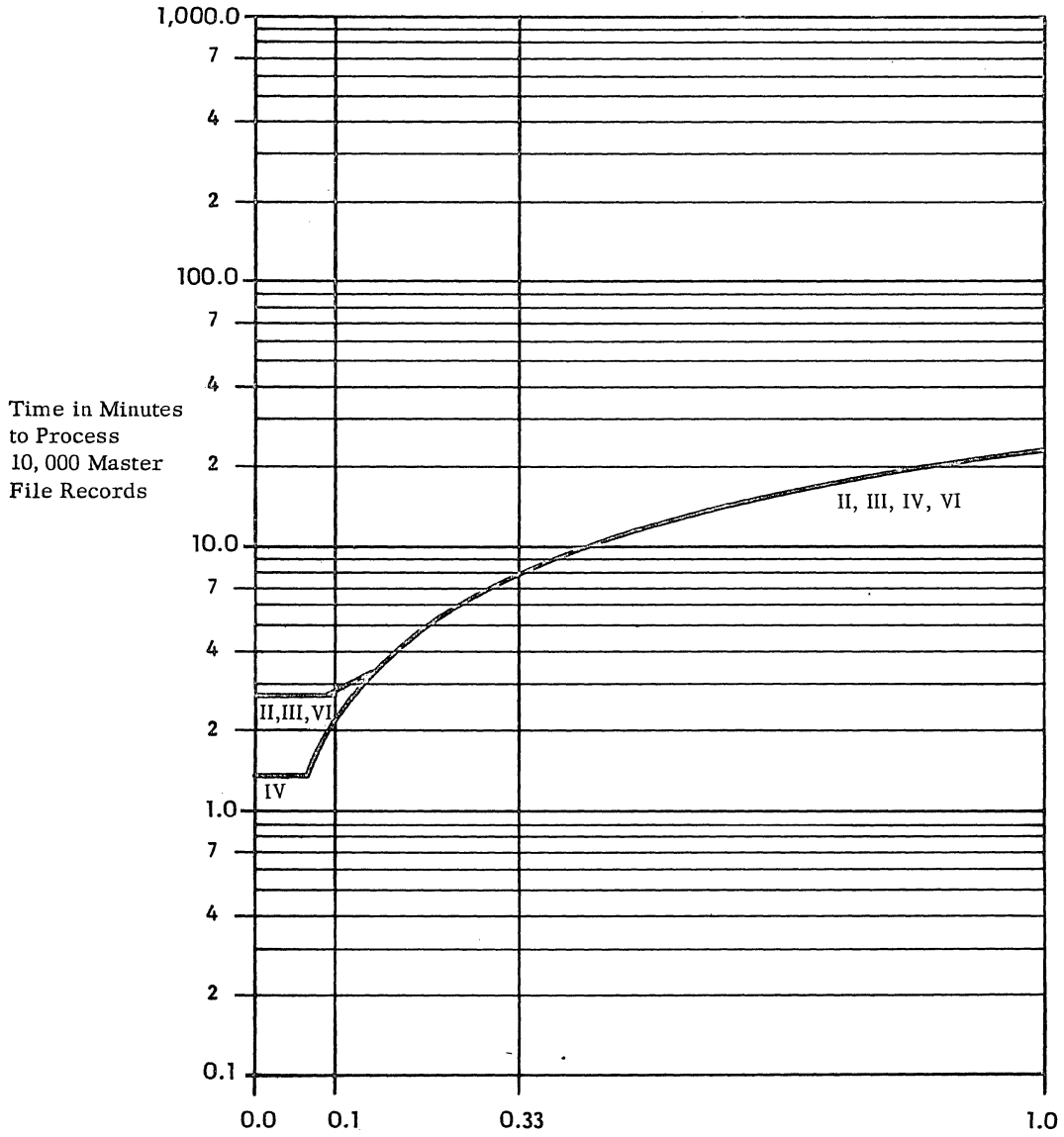
§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record Sizes
Master File: . . . . . 108 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.112 Computation: . . . . . standard.
.113 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.
.114 Graph: . . . . . see graph below.
.115 Storage Space Required: 1,830 words.



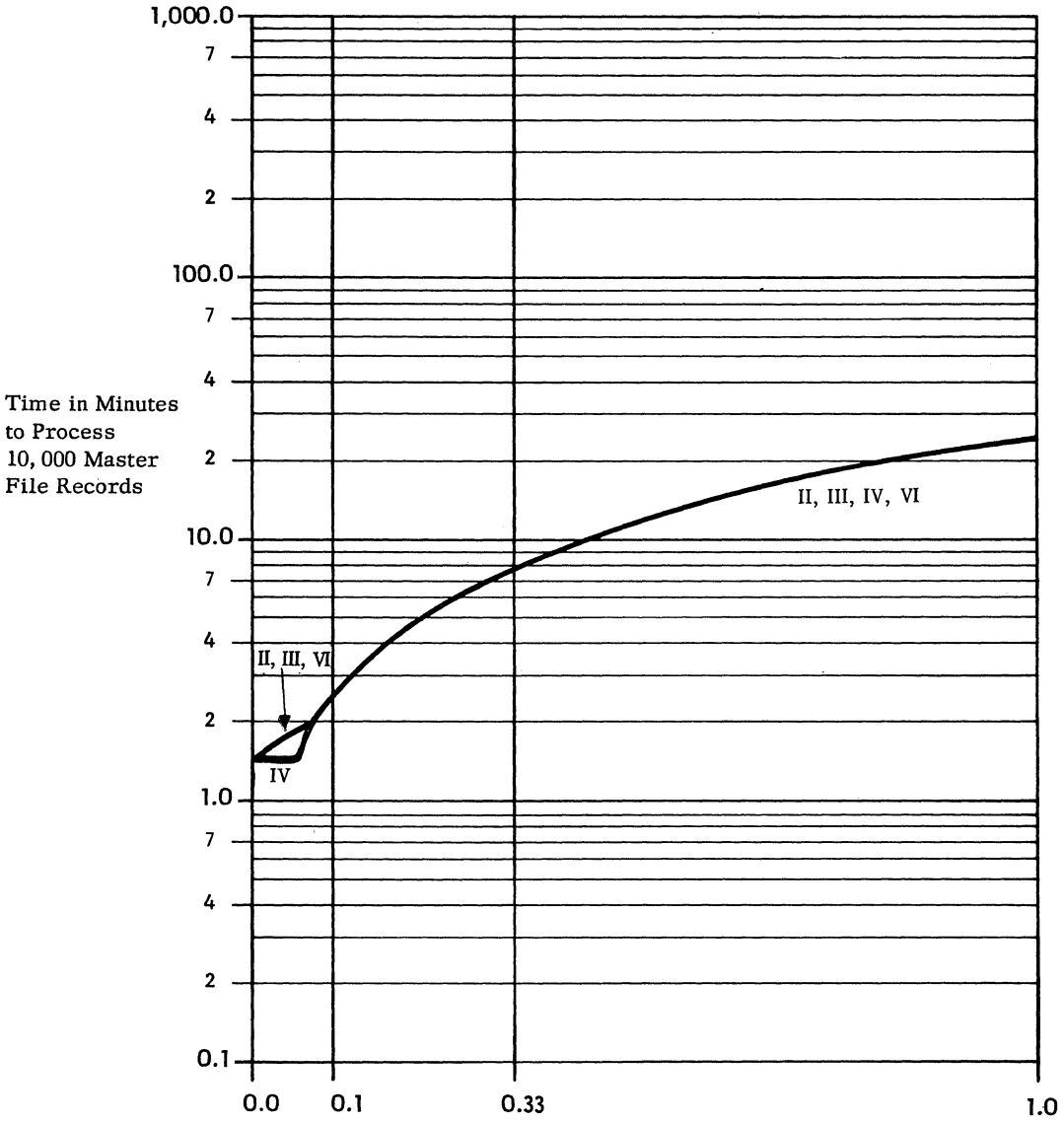
(Roman numerals denote standard System Configuration)

§ 201.

.12 Standard File Problem B

.121 Record Sizes
Master File: . . . . . 54 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



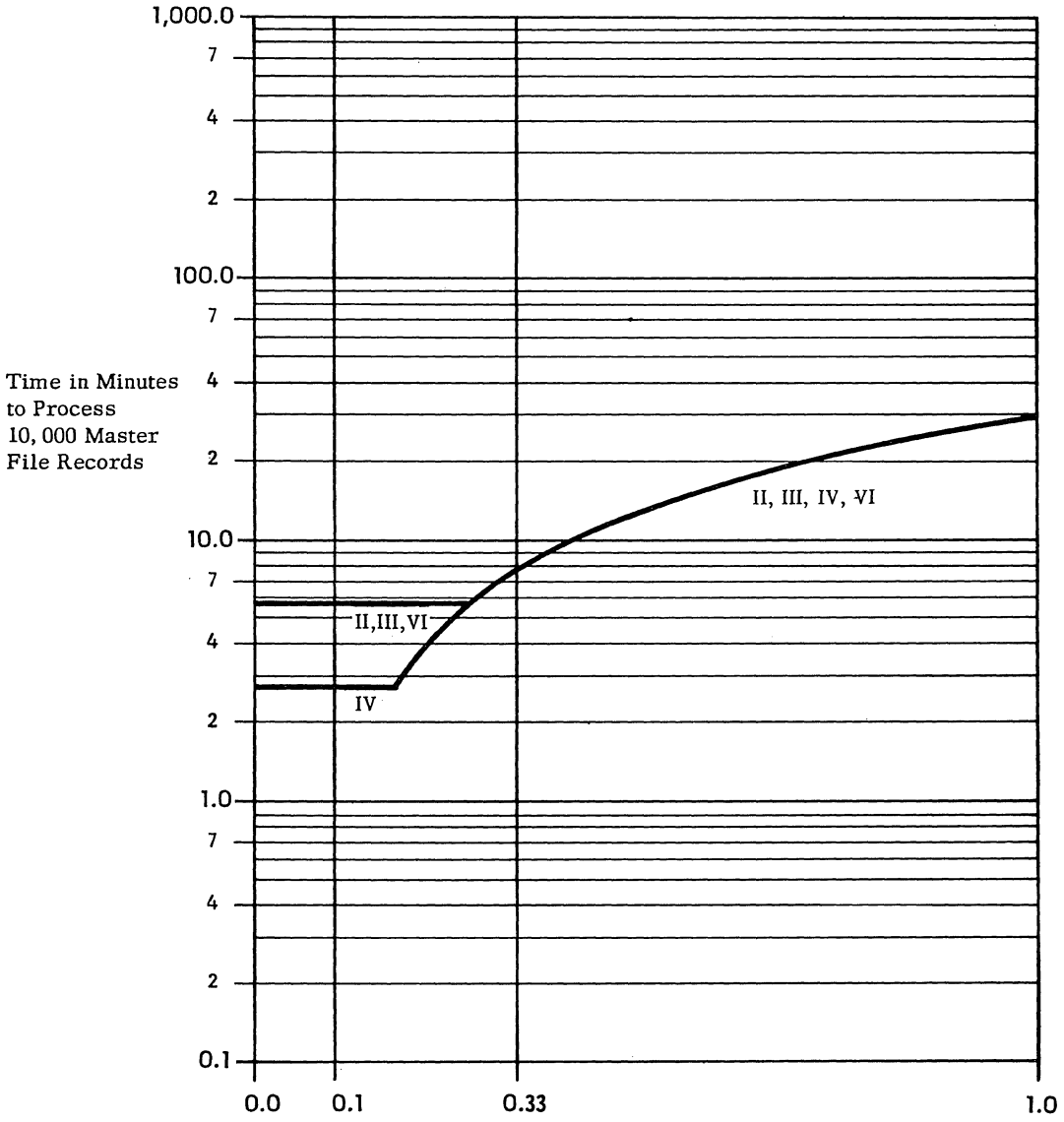
(Roman numerals denote standard System Configuration)

§ 201.

.13 Standard File Problem C

.131 Record Sizes
Master File: . . . . . 216 characters.
Detail Rile: . . . . . 1 card.
Report File: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

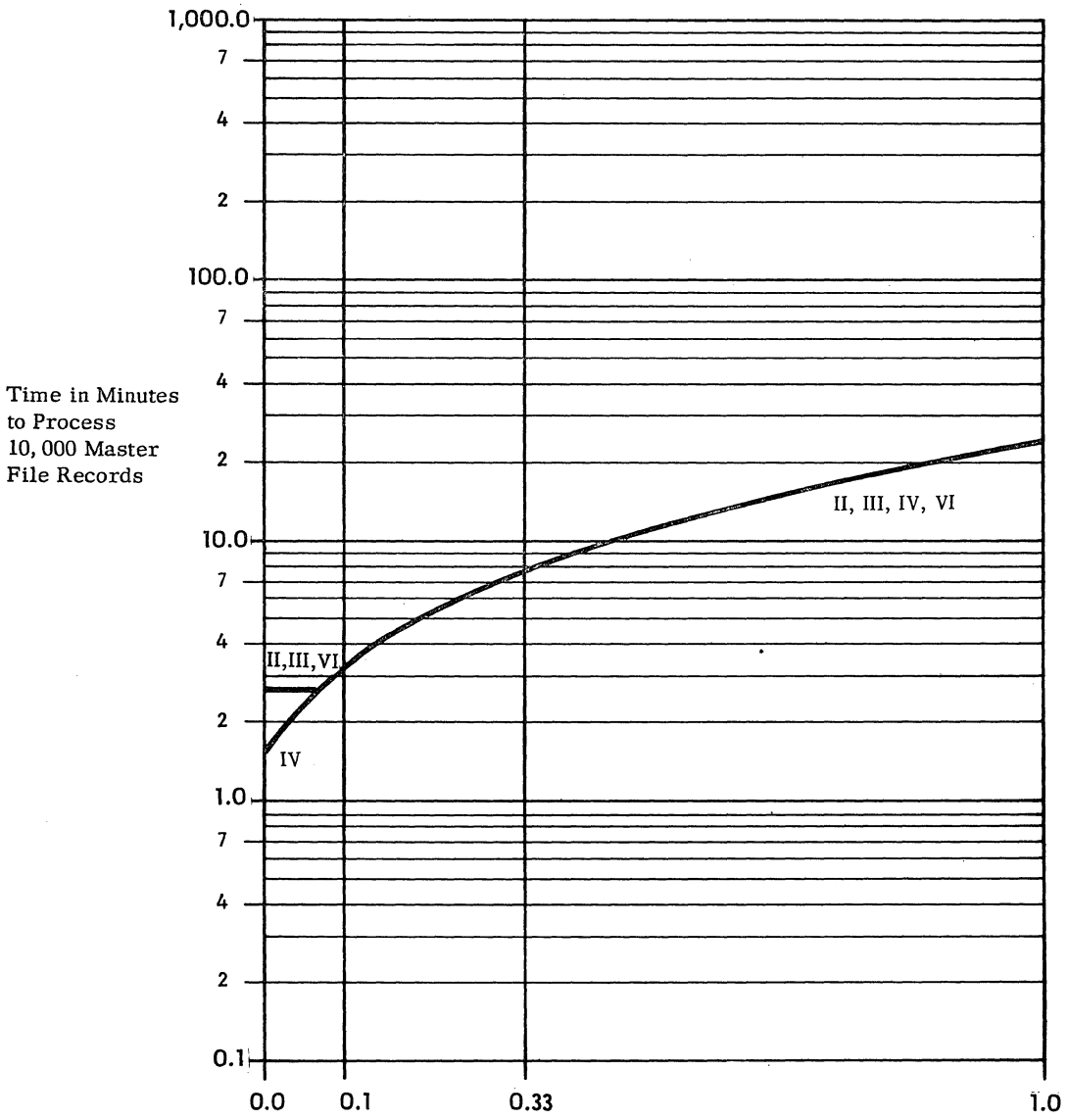
(Roman numerals denote standard System Configuration)

§ 201.

.14 Standard File Problem D

.141 Record Sizes
Master File: . . . . . 108 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configuration)

§ 201.

.2 SORTING

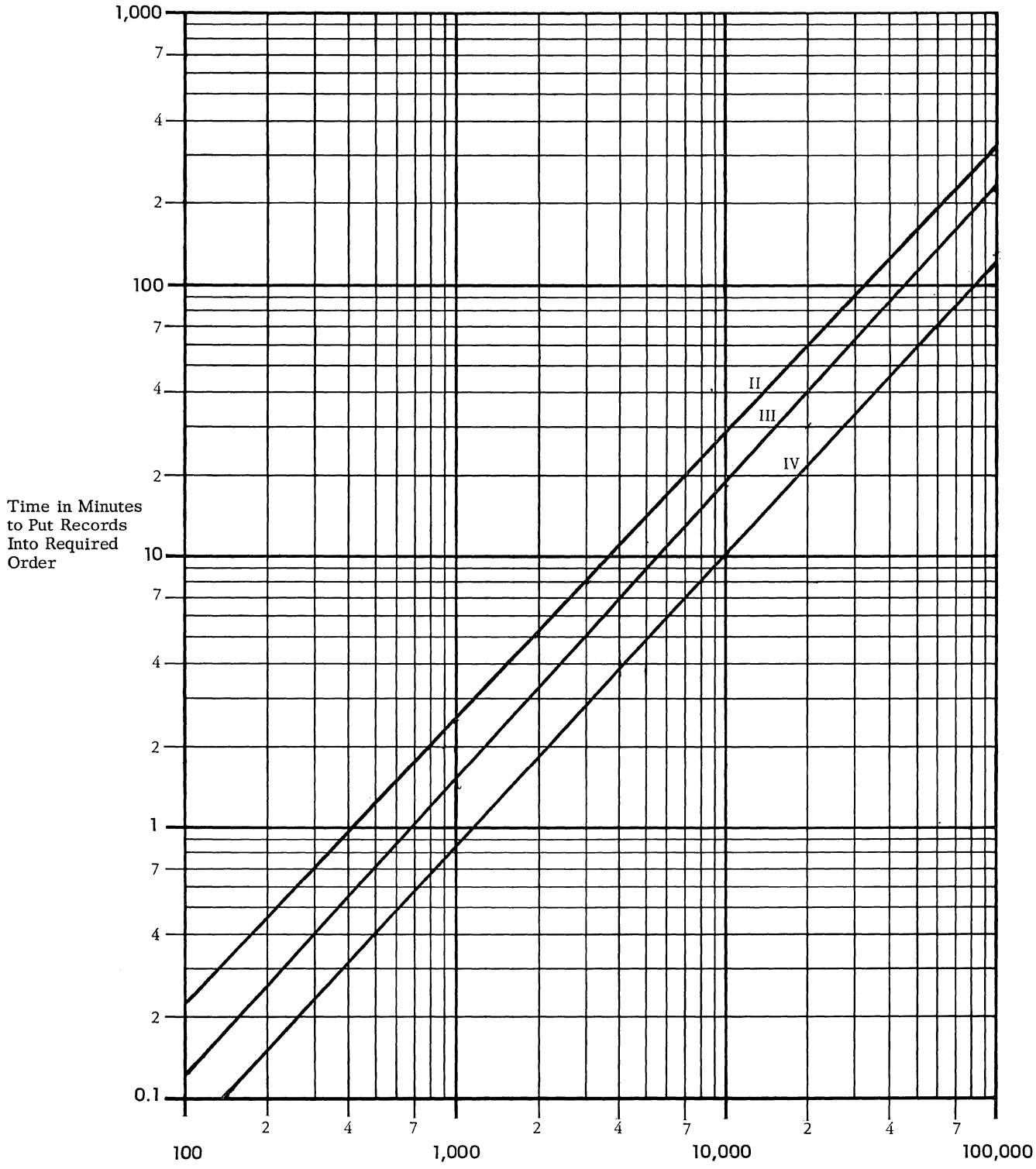
.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.

.212 Key size: . . . . . 8 characters.

.213 Timing basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph:. . . . . see graph below.



UNIVAC SS 80/90 MODEL II
PHYSICAL CHARACTERISTICS

UNIVAC SS 80/90 MODEL II PHYSICAL CHARACTERISTICS

IDENTITY	Unit Name		Central Processor	High Speed Printer	High Speed 80-Col. Reader	Card Read 80-Col. Punch Unit
	Model Number		SEE PRICES	7912	7935	7936
PHYSICAL	Height × width × depth, inches		69 × 108¼ × 32	53 × 72¼ × 32	48 × 50 × 24	54 × 49 × 27
	Weight, pounds		3,532	1,538	758	950
	Maximum cable lengths	Power Data	From CP	27' 3" 27' 1" To CP	25' 1" 24' 7" To CP	26' 11" 26' 3" 3 27' 0" Cables To CP
ATMOSPHERE	Storage Ranges	Temperature, °F.	← NOT AVAILABLE →			
		Humidity, %				
	Working Ranges	Temperature, °F.	60° – 85°	60° – 85°	60° – 85°	60° – 85°
		Humidity, %	30 – 70	30 – 70	30 – 70	30 – 70
	Heat dissipated, BTU/hr.		27,660	11,910	3,396	3,780
	Air flow, cfm.		2,100	550	200	200
ELECTRICAL	Voltage	Nominal	208 – 240	Contained in Central Processor		
		Tolerance	±10% into regulator	Contained in Central Processor		
	Cycles	Nominal	60	Contained in Central Processor		
		Tolerance	±0.5	Contained in Central Processor		
	Phases and lines		Single phase 3 wire	Contained in Central Processor		
	Load KVA		16.9	Contained in Central Processor		
NOTES	1. Maximum floor loading. 150 lbs./sq. ft.		2. For all equipment 90% Filtration per US Bureau of Standards. Dust Spot Discoloration Test.		3. Internal dust filters are provided.	

UNIVAC SS 80/90 MODEL II PHYSICAL CHARACTERISTICS (Contd.)

Uniservo II Magnetic Tape Unit	First Randex 24 Million Digits Unit	First Randex 12 Million Digits Unit	Additional Randex 24 Million Digits Unit	Synchronizer	Randex Power Control Unit
7915	7957	7965	7966	7914	
69 × 31 × 31	69 × 76 × 33	69 × 76 × 33	69 × 76 × 33	69 × 76 × 32	69 × 48 × 31
758	2,335	2,335	2,335	2,566	1,284
18' 10" 21' 5" To SYNC	Drum to Synchronizer 67 ft. maximum. Information not currently available To SYNC	To SYNC	To SYNC	22' 4" From CP	58 ft. to Synchronizer
← NOT AVAILABLE →					
60° – 85°	60° – 85°	60° – 85°	60° – 85°	60° – 85°	60° – 85°
30 – 70	30 – 70	30 – 70	30 – 70	30 – 70	30 – 70
8,160	7,140	7,140	7,140	11,520 to 15,180	4,080
300	550	550	550	2,100	360
See Note 4				208 – 240	
See Note 4	FROM RANDEX POWER			±10% to regulator	±10%
	Information not currently			60	60
		available		±0.5	±0.5
	1ϕ 3 wire			1 or 3	1 or 3
2.7 each		2.4 KVA each		4.3 KVA	2.4 KVA per Drum
4. Contained in Synchronizer					

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
MODEL II BASIC	7961	90-Column Card and Tape			
	7962	80-Column Card and Tape			
CENTRAL PROCESSOR		Standard Equipment:			
		2,400 Words 1.7 msec. average access store	3,235	560	177,500
		200 Words 0.4 msec. average access store			
		1,280 Words 0.017 msec. access store			
		9 Index Registers			
		Options:			
		Program Interrupt	60		3,000
		200 Words 1.7 msec. average access store (800 word max)	275	70	10,250
		400 Words 0.4 msec. average access store (1,600 word max)	400	20	12,500
		Multiply and Divide	400	25	12,000
MODEL II EXPANDED	7963	90-Column Card and Tape			
	7964	80-Column Card and Tape			
CENTRAL PROCESSOR		Standard Equipment:			
		7,600 Words 1.7 msec. access	7,135	830	315,700
		1,200 Words 0.4 msec. access			
		1,280 Words 0.017 msec. access			
		Multiply and Divide			
		9 Index Registers			
		Options:			
		Program Interrupt	60	—	3,000
INPUT-OUTPUT	7912	600 lpm 100-Column Printer (1 max)	935	335	41,100
		Options:			
		10-Column additional	20	5	800
		20-Column additional (maximum 130 columns)	30	10	1,320
		Variable 6 or 8 inch line spacing	NONE	15	275

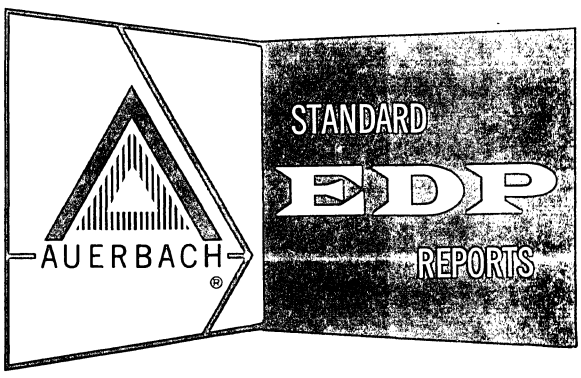
§ 221. PRICE DATA (Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchases $
INPUT-OUTPUT	7912	600 lpm 100-Column Printer (1 max)	935	335	41,100
		Options:			
		10-Column additional	20	5	800
		20-Column additional (maximum 130 columns)	30	10	1,320
		Variable 6 or 8 inch line spacing	None	15	275
	7945	600 cpm 90-Column Card Reader	255	55	11,200
		(or)			
	7935	600 cpm 80-Column Card Reader (1 max)	255	55	11,200
		Options:			
		Stacker Select	50	10	2,300
		80-Column Read Feature	35	18	1,350
		90-Column Read Feature	35	18	1,350
INPUT-OUTPUT	7946	150 cpm 90-Column Read Punch	725	200	32,000
		(or)			
	7936	150 cpm 80-Column Read Punch (1 max)	725	200	32,000
		Options:			
		Preread (80- or 90-Column)	100	20	4,200
		Post read (80- or 90-Column)	100	20	4,200
		Stacker Select	50	10	2,300

UNIVAC III

Univac

(A Division of Sperry Rand Corporation)



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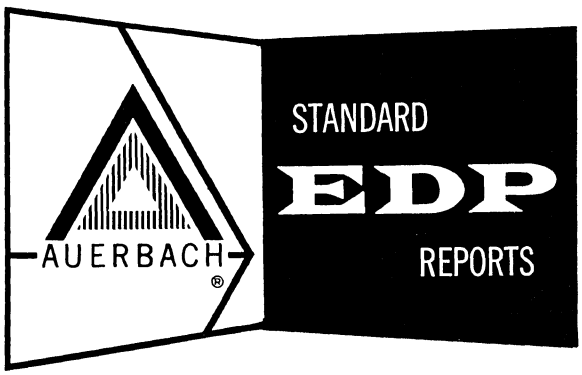
UNIVAC III

Univac

(A Division of Sperry Rand Corporation)



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CONTENTS

CONTENTS (Contd.)

INA = Information Not Available.

INTRODUCTION

§ 011.

The UNIVAC III is a large scale data processing system suitable for both business and scientific applications. System rentals range from approximately $19,000 to $40,000 per month, and most installations will probably fall within the $25,000 to $35,000 range. By means of the software operating system, it is possible to utilize hardware facilities for simultaneous processing of a number of independent programs. Hardware facilities that have been incorporated to help achieve this objective are:

- A series of interrupt levels which permit varied peripheral equipments to make their demands on the central processor.
- Provision of scatter-read and gather-write facilities through the use of function specification words to specify address assignments.
- Availability of 9 or 15 index registers plus indirect addressing.
- Four one-word arithmetic registers, which may be used individually or in combination in ascending order only.
- Control of all input-output operations by independent input-output channels. Up to 13 channels can be connected, and all channels can operate simultaneously with each other and with the central processor.

The central processor can perform additions or subtractions on binary or decimal operands. These operands can be distributed over one to four words of 27 bits each. Each UNIVAC III word uses two bits for modulo 3 checking. The remaining 25 bits can contain an instruction word, four 6-bit alphameric characters plus a sign bit, six 4-bit numeric characters plus a sign bit, or 24 binary data bits plus a sign.

Multiplication and division can be performed on decimal data only. The UNIVAC III can perform logical AND and inclusive OR functions and binary comparison operations. Branching, alphameric-to-decimal and decimal-to-alphameric conversion, and zero suppression capabilities ease data manipulation and program control; however, most editing functions, floating point arithmetic, and conversion of data to floating point format must be handled by subroutines. Scatter-read and gather-write facilities provide fast means of assembling data into and disseminating data from core storage.

Core storage capacity ranges from 8,192 to 32,768 word locations in increments of 8,192. Cycle time is 4 microseconds per word, but the majority of instructions take 8 microseconds.

A wide range of input-output equipment is offered for the UNIVAC III. A system can include a maximum of 32 Uniservo IIIA Magnetic Tape Units, 6 Uniservo IIA Magnetic Tape Units, and a total of 8 units of the following equipments in any combination: High Speed Card Readers, High Speed Printers, Card Punch Units, Punched Paper Tape Units, and Uniservo IIIC Magnetic Tape Synchronizers controlling from 2 to 8 tape units each.

Two models of both card readers and card punches are available. Cards can be read at a peak rate of 800 cards per minute and punched at a peak rate of 300 cards per minute. Punched paper tape can be read at 250, 500, or 1,500 characters per second, and punched at 110 characters per second. The line printer has 128 print positions and a set of 51 characters, and can print 700 alphameric or 922 numeric single-spaced lines per minute.

INTRODUCTION (Contd.)

§ 011.

Three types of Uniservo Magnetic Tape Units are available for the UNIVAC III system, the Uniservo IIIA, IIA, and IIIC.

The Uniservo IIIA Magnetic Tape Unit operates at peak data transfer rates of 133,000 alphameric characters or 200,000 numeric digits per second with a density of 1,000 frames (1,330 characters or 2,000 digits) per inch. Tape can be read forward or backward, but data can be recorded in the forward direction only. Tape can be read or written in either the Start-Stop mode or the Non-Stop mode. A read-after-write check is made upon recording.

The Uniservo IIA Magnetic Tape Unit operates at peak data transfer rates of 25,000 or 12,500 characters per second at densities of 250 or 125 characters per inch respectively. When recording at 250 characters per inch, the format is compatible with the UNIVAC II; the 125 character per inch recording makes the format compatible with the UNIVAC I.

The Uniservo IIIC Magnetic Tape Unit operates at peak data transfer rates of 22,500 or 62,500 characters per second at densities of 200 and 556 characters per inch. The block lengths are variable and the format is IBM-compatible. Tape can be read or written either with or without translation. When translation is specified, the six-bit IBM tape code is converted to six-bit excess three code or vice versa. A read-after-write check is made upon recording.

Major emphasis has been placed on development of software packages to achieve the maximum throughput capabilities of the system and to simplify programming. These packages provide complete input-output control, the means of associating and running independently prepared programs simultaneously, the ability to call many routines and subroutines, and the ability to incorporate new routines or subroutines in the library. Program testing aids such as SNAPshot, DUMP, and TRACE have also been incorporated in the software packages. Data sorting and merging are provided by a sort generator which generates the instructions for the sort or merge from a set of parameters outlined by the user. The original input and final output routines are the responsibility of the user. Input-output routines provided for the intermediate collating pass use any available tape in the system (even the unused portion of data tapes).

Two complete machine oriented software packages are available for the UNIVAC III; however, no compatibility exists between them. One package consists of SALT, a machine oriented language; DUTY, a library of routines and subroutines; and CHIEF, an executive routine. The other consists of UTMOST, a machine-oriented language; SUPPORT III, a library of routines and subroutines; and BOSS III, an executive routine. New developments and innovations will be incorporated in the already more sophisticated UTMOST, SUPPORT III, and BOSS III package; however, both packages will be maintained.

Both SALT and UTMOST provide an easily understandable mnemonic representation of instructions, pseudo operations for directing the assembler, and the ability to perform operations to develop the operand address. UTMOST is more extensive than SALT in the functions that it provides.

DUTY and SUPPORT III each provide the ability to update and maintain a library of routines and subroutines, and an independent library of object programs for the system.

Both CHIEF and BOSS III are comprehensive operating systems that control the scheduling, loading, and multi-running of programs; handle most errors; and permit two-way communication between the operator and the system. All functions of these executive routines are initiated by and closely integrated with the hardware interrupt facilities.

Both COBOL-61 and FORTRAN IV have been implemented for the UNIVAC III. Object programs produced by both the COBOL and FORTRAN compilers can be run under the control of BOSS III.

INTRODUCTION (Contd.)

§ 011.

UNIVAC III COBOL is essentially Required COBOL-1961. Several useful electives have been implemented, including segmentation of the object program and arithmetic operands up to 18 digits in size. Extensions to COBOL-61 include a SORT facility, a MONITOR verb that facilitates program testing, and the ability to add independently compiled COBOL subprograms to a main program at run time.

The UNIVAC III FORTRAN language is largely compatible with the IBM 7090/7094 implementation of FORTRAN IV. Most FORTRAN II statements will also be accepted and correctly interpreted by the translator. Double precision and complex variables, however, are not permitted.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	27 bits	data or instruction; basic storage location.
Record (Segment):	1 to 511 words	magnetic tape.
Block:	1 to N segments (N segments are limited to available core storage)	magnetic tape.
File:	1 to N records	magnetic tape.
Unit Record:	80- or 90-column	punched card paper tape.

.2 DATA FORMATS

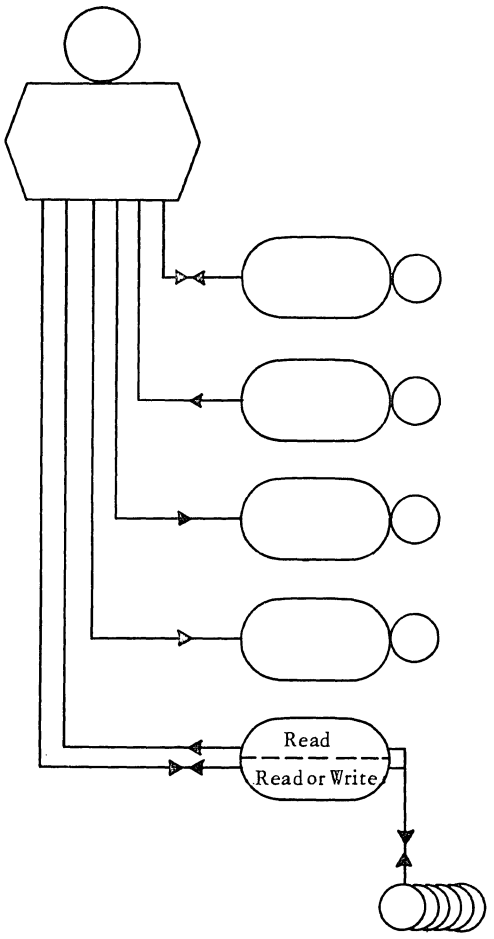
Type of Information	Representation
Decimal Digit	4 bits (expressed in excess-three code).
Alphameric Character	6 bits.
Instruction	1 word.
Decimal Word	6 decimal digits plus 1 sign plus 2 check bits.
Alphameric Word	4 alphameric characters plus 1 sign plus 2 check bits.
Binary Word	24 bits plus 1 sign plus 2 check bits.

SYSTEM CONFIGURATION

§ 031.

1. 6-TAPE BUSINESS SYSTEM; CONFIGURATION III

Deviations from Standard Configuration: . . . . . Core storage larger by 4,192 words.
One more simultaneous transfer while computing possible (tape operation).
Nominal tape speed exceeded by 103,000 characters per second.
Printer faster by a minimum of 205 lines per minute.
Card reader faster by 200 cards per minute.
Card punch faster by 200 cards per minute.
Two more simultaneous transfers possible (other than tape).
Eight more index registers.
Console typewriter input.
Five general-purpose, two Uniservo III-A, and one Uniservo II Input-Output channels not used.

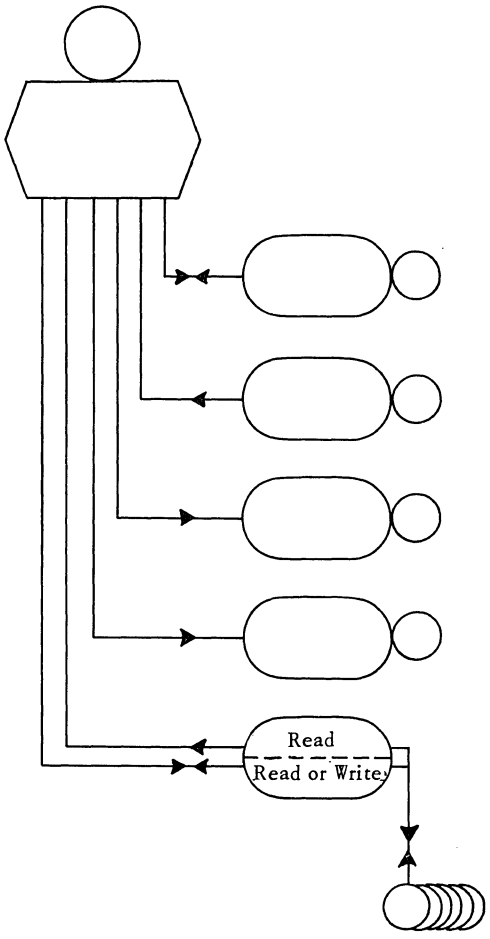


Equipment	Rental
Core Storage: 8,192 words	
Model 4121 Central Processor	$8,000
Console and Typewriter Buffer	
Model 4133 or Model 4182 Card Reader and Synchronizer: 700 cards/min.	750
Model 4127 or Model 4183 Card Punch and Synchronizer: 300 cards/min.	850
Model 4152 Printer and Synchronizer: 700 to 922 lines/min.	1,650
Uniservo III A Synchronizer: two channels	2,900
Model 4123 Power Supply	350
Model 4209 Magnetic Tape Units (6): 133,000 characters/sec.	4,500
Total Rental:	$19,000

§ 031.

2. 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration: . . . . . One more simultaneous transfer possible (tape operation).
Nominal tape speed exceeded by 103,000 characters per second.
Printer faster by a minimum of 205 lines per minute.
Card reader faster by 200 cards per minute.
Card punch faster by 200 cards per minute.
Two more simultaneous transfers possible (other than tape).
Six more index registers.
Console typewriter input.
Five general-purpose, two Uniservo IIIA, and one Uniservo II Input-Output channels not used.
No floating point.

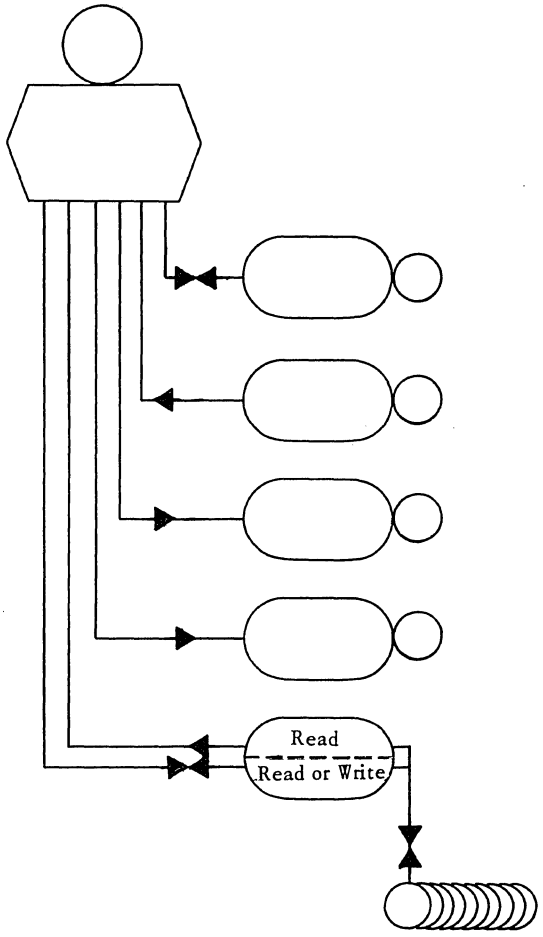


Equipment	Rental
Model 4197 Core Storage: 16,384 words Model 4121 Central Processor Console and Typewriter Buffer	$9,400
Model 4133 or Model 4182 Card Reader and Synchronizer; 700 cards/min.	750
Model 4127 or Model 4183 Card Punch and Synchronizer: 300 cards/min.	850
Model 4152 Printer and Synchronizer: 700 to 922 lines/min.	1,650
Uniservo IIIA Synchronizer: two channels	2,900
Model 4123 Power Supply	350
Model 4209 Magnetic Tape Units (6): 133,000 characters/sec.	4,500
Total Rental:	$20,400

§ 031.

3. 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . . Core storage larger by 576 words.
Nominal tape speed exceeded by 73,000 characters per second.
Printer faster by a minimum of 205 lines per minute.
Card reader faster by 200 cards per minute.
Card punch faster by 200 cards per minute.
One more simultaneous transfer while computing possible (other than tape).
Three more index registers.
Five general-purpose, two Uniservo IIIA and one Uniservo II Input-Output channels not used.
No floating point.



Equipment	Rental
Model 4122 Core Storage: 24,576 words Model 4121 Central Processor Console and Typewriter Buffer	$11,000
Model 4133 or Model 4182 Card Reader and Synchronizer: 700 cards/min.	750
Model 4127 or Model 4183 Card Punch and Synchronizer: 300 cards/min.	850
Model 4152 Printer and Synchronizer: 700 to 922 lines/min.	1,650
Uniservo IIIA Synchronizer: two channels.	2,900
Model 4123 Uniservo Power Supply	350
Model 4209 Magnetic Tape Units (10): 133,000 characters/sec.	7,500
Total Rental:	$25,000

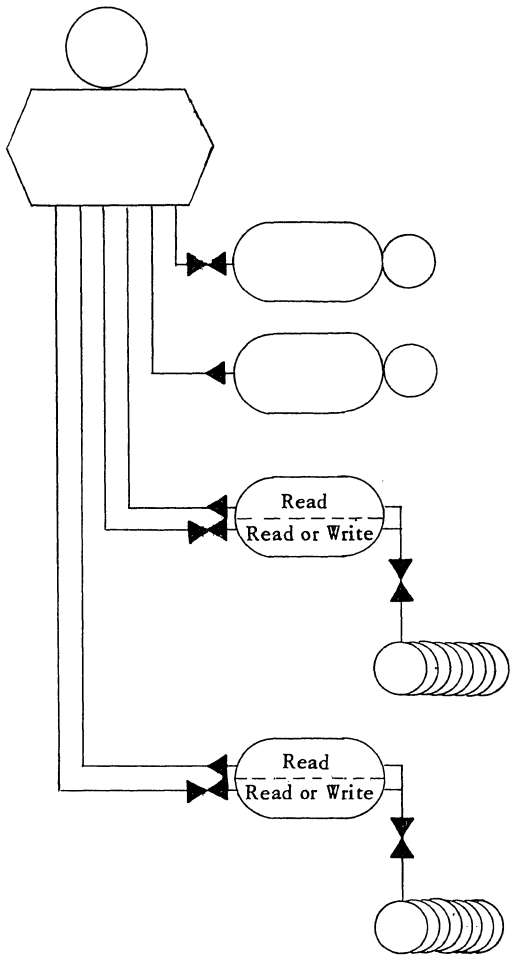
§ 031.

4. 20-TAPE GENERAL SYSTEM (PAIRED); CONFIGURATION VIIIB

Deviations from Stardard Configuration:

On-line equipment: . . . . . Core storage larger by 768 words.
Nominal tape speed exceeded by 13,000 characters per second.
Card reader faster by 600 cards per min.
One more simultaneous transfer while computing possible (other than tape).
Five more index registers.

Off-line equipment: . . . . . Core storage larger by 3,192 positions.
Two fewer tape units.
Nominal tape speed exceeded by 83,000 characters per second.
Printer is slower by a minimum of 78 lines per minute.
Card punch faster by 100 cards per minute;
Four more index registers available.

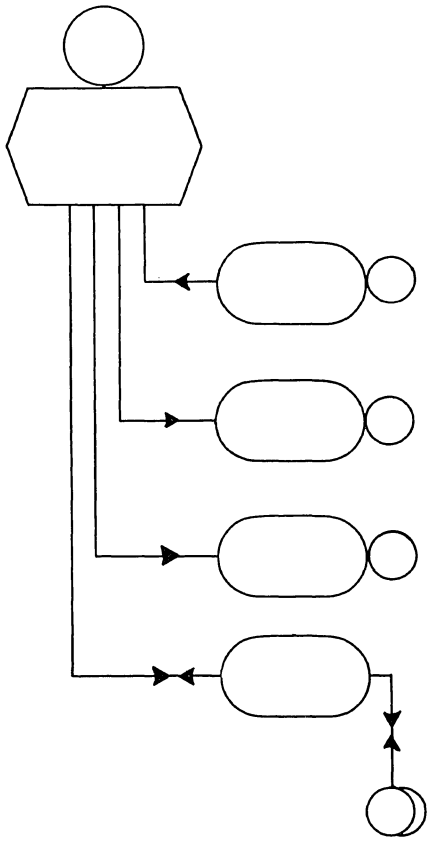


On Line Equipment	Rental
Model 4197 and Model 4122 Core Storage: 32,768 words	
Model 4121 Central Processor	$12,030
Console and Typewriter Buffer	
Model 4133 and Model 4182 Card Reader and Synchronizer: 700 cards/min.	750
Uniservo IIIA Synchronizer: two channels.	2,900
Model 4123 Power Supply	350
Model 4209 Magnetic Tape Units (8): 133,000 char/sec.	6,000
Uniservo IIIA Synchronizer: two channels.	2,900
Model 4123 Power Supply	350
Model 4209 Magnetic Tape Units (8): 133,000 char/sec.	6,000
Optional Features Included: . . . . . 6 additional index registers	300
Total Rental:	$31,580
Total including off-line equipment:	$38,730

§ 031.

4. 20-TAPE GENERAL SYSTEM (PAIRED); CONFIGURATION VIIIB - (Contd.)

Off-Line Equipment (Univac 1050):



	Rental
Core Storage: 8,192 positions Central Processor	$1,850
Card Reader and Synchronizer: 1000 cards/min.	400
Card Punch and Synchronizer: 300 cards/min.	700
Printer and Synchronizer: 922 lines/min.	800
Print Buffer	350
Uniservo IIIA Synchronizer	1,200
Power Supply	350
Uniservo IIIA Magnetic Tape Units (2); 133,000 char/sec.	1,500
Total Rental:	$7,150

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . . Core Storage. Model 4122.

additional core storage 8, 192, 16, 384, or 24, 576 words.

.12 Basic Use: . . . . . working storage.

.13 Description

Core stores are used to provide either 8, 192, 16, 384, 24, 576 or 32, 768 words of working storage. Each word consists of 27 bits, of which 25 bits (including sign) are used for data or instruction words and the remaining 2 bits are reserved for checking purposes. The check bits are used to produce a modulo 3 sum of zero of the 27 bits. A word can contain either an instruction, a control word, or data. Data can be in either alphameric, decimal or binary format, or any combination thereof. The cycle time of the store is four microseconds.

Nineteen locations of the store are reserved for specific functions. Locations 0003 through 0015 are input-output standby locations, and locations 0016 through 0021 are automatic program interrupt locations.

Scatter-read and gather-write capabilities in the input-output make it possible to distribute a tape record into a number of areas in core storage or to assemble several areas of core storage into a tape record. Individual digits or fields within a word can be addressed in the central processor through a Field Select Control Word.

.14 Availability: . . . . April, 1961.

.15 First Delivery: . . August, 1962.

.16 Reserved Storage: . none.

.2 PHYSICAL FORM

.21 Storage Medium: magnetic core.

.22 Physical Dimensions

.221 Magnetic core type storage
Core diameter: . . 0.05 inch.
Core bore: . . . . 0.03 inch.
Array size:. . . . 64 bits by 64 bits.

.23 Storage Phenomenon: direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . yes.
.242 Data regenerated constantly:. . . . no.
.243 Data volatile: . . . yes.
.244 Data permanent: . . no.
.245 Storage changeable: no.

.28 Access Techniques

.281 Recording method:. . .coincident current.
.282 Reading method:. . . .sense wires.
.283 Type of access: . . .uniform.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates: . . 250, 000 cps.
Unit of data: . . . word.
Conversion factor: 27 bits/word.
Data rate: . . . . 250, 000 words/sec.
Compound data rate: 250, 000 words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage			Maximum Storage
Words:	8, 192	16, 384	24, 576	32, 768
Characters:				
numeric:	49, 152	98, 304	147, 456	196, 608
alphabetic:	32, 768	65, 536	98, 304	131, 072
Instructions:	8, 192	16, 384	24, 576	32, 768
Modules:	1	2	3	4

.32 Rules for Combining Modules: . . . . all combinations are shown in paragraph .31.

.4 CONTROLLER: . . Central Processor.

.5 ACCESS TIMING

.52 Simultaneous Operations: none.

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . 1.5 μsec.
Cycle time: . . . . . 4 μsec.
For data unit of: . . . 1 word.

.6 CHANGEABLE STORAGE:. . . . no.

§ 041.

.7 STORAGE PERFORMANCE

.71 Data Transfer

Pair of storage units possible with self: . . . . yes.

.72 Transfer Load Size

With arithmetic register: . . . . 1 bit to 4 words.

.73 Effective Transfer Rate

With self: (straight coding) . . 100,000 words/sec.
With self: (program loop) . . 62,500 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	memory address check	interrupt.
Invalid code:	invalid op code	interrupt.
Receipt of data:	modulo 3 check	interrupt.
Recording of data:	2 check bits carried with data	none.
Recovery of data:	2 check bits recovered with data	interrupt.
Dispatch of data:	modulo 3 check	interrupt.
Timing conflicts:	none.	
Physical record missing:	none.	
Reference to locked area:	none.	

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . . Arithmetic and Control Module. Type 4121.

.12 Description

The UNIVAC III is a single-address, fixed word length, digital processor. The main arithmetic and control circuitry, core storage, and I/O channels are all housed in the processor cabinet. The four models differ only in the amount of core storage they contain. Word length of core storage location and arithmetic registers is 27 bits. Two bits of each location are used for Modulo 3 Check bits. The remaining 25 bits may contain an instruction word, a binary data word consisting of a sign bit and 24 data bits, an alphameric data word consisting of a sign bit and four six-bit BCD characters, or a decimal data word consisting of a sign bit and six 4-bit excess-three binary-coded decimal digits.

Arithmetic operations are performed in any individual or combination of the four available Arithmetic Registers, with the results placed in the Arithmetic register(s). Two modes of operation can be specified: binary for addition and subtraction; or decimal for addition, subtraction, multiplication, and division. Numeric fields are processed serial-by-digit in arithmetic instructions.

The instruction repertoire operates on the theory of addressing fixed-length words; however, through field selection options, any bits making up a word can be addressed. From one bit to four words can be operated on at one time for internal data movement. The word size is six digits, but addition and subtraction can be performed on one to four words at a time, giving a total capability of 24 digits. Multiplication is performed on one-word multiplicands and one-word multipliers, giving a two-word product. The six most significant digits are in Arithmetic Register 2 and the six least significant digits are in Arithmetic Register 3. Division is restricted to 6-digit divisors and 12-digit dividends, giving a quotient of six digits in Arithmetic Register 2 and a remainder of six digits in Arithmetic Register 1.

Ten-bit operand addresses are automatically indexed by the register specified in positions 21 and 24 of the instruction. If no index register is specified, binary zeros are added to the operand address to make it 15 bits long. Indirect addressing is possible on the majority of instructions. All input-output instructions refer to a function specification word for a starting address. Internal facilities for editing and format control are severely limited, but subroutines are available to perform these functions. Many load, store, add, subtract, and compare operations can be carried out in any of the four arithmetic registers.

.12 Description (Contd.)

The most common operand length is one 25-bit word, but the field definition feature permits arithmetic, load, store, and compare instructions to be carried out on specified portions of a word. The control portion of a field-select word specifies the high- and low-order bit positions of the field to be used. Several fields of like sign can be stored in a single core storage location. Field overflow (from an arithmetic operation) and zero division checks are performed, and cause an indicator to be set, and result in a Program Interrupt, which in turn automatically transfers control to a correction routine. Modulo 3 checks are made on all transfers to and from core storage and on all arithmetic operations performed. If an error occurs in this check, a program testable indicator is set.

Scatter-read and gather-write capabilities are used in input-output operations. A block of data on tape can be scattered into a number of smaller segments in core storage or a number of smaller segments in core storage can be gathered to form one large block on tape. The addresses of the several segments from or to which data is to be gathered or scattered are specified in a list of record definition words, one word for each segment to be transferred. The end of a block transfer operation is indicated by a record definition word with a "1-bit" in position 25.

Automatic interruption of a program in progress occurs whenever an input-output operation has been completed, or when either an error or operation request has been assigned, with the following class priority: (1) Processor Error, (2) Contingency (overflow, invalid operation code, and operator requests), and (3) Input-output (error and completion). Interrupt routines are interrupted by higher priority interrupts. When an interrupt occurs, the contents of the Control Counter (address of the next sequential instruction) are stored and control is transferred to the pre-assigned location that will service that class of interrupt. When the interrupt has been serviced, control is returned to the interrupted program.

Multi-running of independently prepared programs is accomplished using the input-output interrupt. No hardware provision has been made for preventing one program from using storage space also assigned to another program.

Optional Features

Optional features include a programmable clock and six additional Index Registers.

.13 Availability: . . . . . September, 1962.

.14 First Delivery: . . . . August, 1962.

§ 051.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point			
	Add-Subtract:	automatic	decimal	1 bit to 4 words.
	Multiply			
	Short:	none.		
	Long:	automatic	decimal	1 word.
	Divide			
	No remainder:	none.		
	Remainder:	automatic	decimal	2-word dividend and 1-word divisor.
.212	Floating point			
	Add-Subtract:	subroutine.		
	Multiply:	subroutine.		
	Divide:	subroutine.		
.213	Boolean			
	AND:	automatic	binary	25-bit word.
	Inclusive OR:	automatic	binary	25-bit word.
.214	Comparison			
	Numbers:	automatic		1 bit to 4 words.
	Absolute:	automatic		1 bit to 4 words.
	Letters:	automatic		1 bit to 4 words.
	Mixed:	automatic		1 bit to 4 words.

		Provision	From	To	Size
.215	Code translation:	automatic	alphameric	decimal	3 words.
		automatic	decimal	alphameric	2 words.
.216	Radix conversion:	subroutine	decimal	binary	1 to 4 words.
		subroutine	binary	decimal	1 or 2 words.

		Provision	Comment	Size
.217	Edit format			
	Alter size:	automatic	in code translation	3 words.
	Suppress zero:	automatic	alphameric zero & comma	1 to 4 words.
	Round Off:	subroutine.		
	Insert point:	subroutine.		
	Insert spaces:	automatic	zero suppress only	1 to 4 words.
	Float:	subroutine.		
	Protection:	subroutine.		

.218 Table look-up: . . . . . subroutine.

		Provision	Comment	Size
.219	Others			
	decimal shift:	automatic	left or right	1 to 2 words.
	alphameric shift:	automatic	left or right	1 to 2 words.
	binary shift:	automatic	circular right	1 word.
	record gather:	automatic		1 to 511 words per segment.
	record scatter:	automatic		1 to 511 words per segment.

.22 Special Cases of Operands

.221 Negative numbers: . . . sign and absolute.
.222 Zero: . . . . . 2 forms; not equal in comparisons.
.223 Operand size determination: . . . . counter and sign.

.23 Instruction Formats

.231 Instruction structure: . 1 word of 25 bits.

.232 Instruction layout:

Part	IA/FS	X	OP	AR/XO/CH/OI	M/SC/IND/CI
Size (bits)	1	4	6	4	10

.233 Instruction parts

Name	Purpose
IA:	indirect addressing.
FS:	field selection.
X:	incrementing index register.
OP:	operation code.
AR:	object arithmetic register.
XO:	object index register.
CH:	channel for I/O operation.
OI:	object indicator address.
M:	address of operand.
SC:	shift count.
IND:	indirect address.
CI:	contingency indicators.

.234 Basic address structure: 1 address.
.235 Literals
Arithmetic: . . . . . none.
Comparisons and tests: . . . . . none.
Incrementing modifiers: . . . . . none.

	Internal storage type	Minimum size	Maximum size	Volume accessible
.2361	Core:	1 bit	4 words 100 (bits)	first 1,024 words.

.2362 Increased address capacity

Method	Volume accessible
Indexing:	total capacity.
Indirect addressing:	total capacity.

.237 Address indexing
.2371 Number of methods: . 1.
.2372 Names: . . . . . indexing.
.2373 Indexing rule: . . . . . binary addition (any carry beyond bit 15 is ignored).
.2374 Index specification: . . automatic (specific register specified in bits 21 to 24 of the instruction).
.2375 Number of potential indexers: . . . . . 15.
.2376 Addresses which can be indexed: . . . M/SC/IND (see Paragraph .233).
.2377 Cumulative indexing: . none.
.2378 Combined index and step: . . . . . none.
.238 Indirect addressing
.2381 Recursive: . . . . . yes.
.2382 Designation: . . . . . a "1" in the IA position of the instruction.
.2383 Control: . . . . . the last address in the recursive sequence specifies a direct address with a "0" in the IA position of the instruction.
.2384 Indexing with indirect addressing: all of the addresses in an indirect address chain may be indexed. The index register specification is an independent function at every level.

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.239 Stepping

.2391	Specification of increment:	control word.
.2392	Increment sign:	control word.
.2393	Size of increment: . .	9 bits (in control word).
.2394	End value:	control word.
.2395	Combined step and test:	yes.

.24 Special Processor Storage

.241 Category of storage	Number of locations	Size in bits	Program usage
Processing unit:	9 or 15	15	indexing.
Processing unit:	4	25	arithmetic registers.
Core storage:	21	25	input-output control.
Core storage:	4	25	tape input-output control.
Clock:	1	20	timing.

.242 Category of storage	Total number locations	Physical form	Access time μsec	Cycle time μsec
Processing unit:	13 or 19	?	?	?
Clock:	1	?	?	?
Core Storage:	25	?	?	?

.3 SEQUENCE CONTROL FEATURE

.31 Instruction Sequencing

.311	Number of sequence control facilities: . .	1.
.314	Special sub-sequence counters:	none.
.315	Sequence control step size:	1 word (2 words in certain test instructions).
.316	Accessibility to routines:	yes.
.317	Permanent or optional modifier: . .	no.

.32 Look-Ahead: . . . . . none.

.33 Interruption

.331	Possible causes	
	In-out controllers: . .	initiation or completion of an input-output operation. occurrence of an error or some condition requiring manual intervention when the synchronizer attempts to perform an operation.
	Storage access: . . .	none.
	Processor errors: . .	Memory Address Checks. Modulo 3 Check on instruction. Modulo 3 Check on operand. Adder Error Check. Overflow. Invalid Op. Code.
.331	Possible causes (Contd.)	
	Other:	Keyboard Request. Keyboard Release. Depression of Stop Button. Typewriter Interrupt.
.332	Control by routine	
	Individual control: . .	by groups of causes.
	Method:	by instruction.
	Restriction:	none.
.333	Operator control: . . .	yes, unit can be placed off-line
.334	Interruption conditions:	completion of an instruction cycle in which an indicator was set and interruption was not inhibited.
.335	Interruption process	
	Disabling interruption:	yes.
	Registers saved: . . .	contents of Control Counter stored in variable location depending on class of cause of interruption.
	Destination:	depends on class of cause.
.336	Control methods	
	Determine cause: . .	automatic into three groups, then by own coding for specific cause.
	Enable interruption: .	program control.

.34 Multi-running

.341	Method of control: . . .	CHIEF and BOSS Executive Systems, using interruption facilities.
.342	Maximum number of programs:	not specified.
.343	Precedence rules: . . .	strict sequence.
.344	Program protection: . .	none.

.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μ sec

.411	Fixed point	
	Add-subtract:	8 for 1 word. 12 for 2 words. 16 for 3 words. 20 for 4 words.
	Multiply:	76 to 124, depending on multiplier digits.
	Divide:	68 to 144, depending on quotient digits.
.412	Floating point:	none.
.413	Additional allowance for	
	Indexing:	no additional time.
	Indirect addressing: .	4.
	Re-complementing: .	4 to 16 for 1 to 4 words.
.414	Control	
	Compare:	8 to 20 for 1 to 4 words.
	Branch:	4.
	Compare and branch: .	none.
.415	Counter control	
	Step:	12.
	Step and test:	16.
	Test:	none.
.416	Edit:	8 (4 char zero suppress).
.417	Convert:	32 (12 char alphmeric to decimal). 32 (12 character decimal to alphameric).

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.418 Shift: . . . . . 12 or 16 (6 decimal or 4 alphameric characters).

.42 Processor Performance in μsec

.421 For random addresses Fixed point Floating point 6 decimal digits.
- c = a + b: . . . . . 24.
- b = a + b: . . . . . 24.
- Sum N items: . . . . . 8.
- c = ab: . . . . . 92 to 140.
- c = a/b: . . . . . 88 to 164.

.422 For arrays of data
- $c_i = a_i + b_j$: . . . . . 56.
- $b_j + a_i + b_j$: . . . . . 56.
- Sum N items: . . . . . 28.
- $c = c + a_i b_j$: . . . . . 140 to 188.

.423 Branch based on comparison
- Numeric data: . . . . 50.
- Alphabetic data: . . . 50.

.424 Switching
- Unchecked: . . . . . 16.
- Checked: . . . . . 48.
- List search: . . . . . -4 + 36N.

.425 Format control per character
- Unpack: . . . . . 4.8.
- Compose: . . . . . ?

.426 Table look up per comparison
- For a match: . . . . . 36C.
- For least or greatest: 36C.
- For interpolation point: . . . . . 36C.

.427 Bit indicators
- Set bit in separate location: . . . . . 16.
- Set bit in pattern: . . 16.
- Test bit in separate location: . . . . . 8.
- Test bit in pattern: . . 8.
- Test AND for B bits: . 20.
- Test OR for B bits: . . 20.

.428 Moving: . . . . . 10 per word.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	contingency interrupt.
Underflow (float-pt):	none.	
Zero divisor:	overflow check set	contingency interrupt.
Invalid data:	none.	
Invalid operation:	check	contingency interrupt.
Arithmetic error:	check	processor error interrupt.
Invalid address:	check	processor error interrupt.
Receipt of data:	check	input-output interrupt.
Dispatch of data:	check	input-output interrupt.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . Console. Type 4124.

.12 Associated Units: . . . Console Typewriter set on Console desk.

.13 Description

The Console, which is a necessary part of every UNIVAC III system, consists of a desk with a Console Typewriter, a Control Unit, and a Monitor panel. The Control Unit contains the main operating controls for the system, the power status lights, and the typewriter keyboard. The Monitor panel, which is located to the right and behind the Control Unit, contains the status indicators and the fault lights for the eight general-purpose channels, the Uniservo power supply, and the Central Processor. Control register displays are provided only by programmed printouts on the Console Typewriter.

.2 CONTROLS

.21 Power

Name	Form	Function
AC on-off:	button-light	depressing button while in the off state turns power on.
		depressing button while in the on state turns power off.

.22 Connections: . . . . . none.

.23 Stops and Restarts

Name	Form	Function
Program run	button-light	causes the Central Processor to begin execution of instructions.
Program stop	button-light	causes a contingency stop in the program. may also be lit by the execution of a Wait instruction.

.24 Stepping: . . . . . none.

.25 Resets

Name	Form	Function
Clear:	button	depressing button causes the following indicators to be reset: Processor Error Interrupt Indicator. Contingency Interrupt Indicator. Input-Output Interrupt Indicator. Interrupt Mode Indicator. Inhibit Input-Output Interrupt Indicator. Sense Indicators. the following registers are also cleared to binary 0's: Control Counter. Index Registers. Memory Address Counters.
Rewind:	button-light	depressing button causes logical Uniservo III 0000 to rewind without interlock; button only effective when the program stop light is lit.

.26 Loading

Name	Form	Function
Load	button-light	depressing button causes logical Uniservo III 0000 to read forward one block without control word; button only effective when the program stop light is lit.

.27 Sense Switches: . . . . none.

.28 Special

Name	Form	Function
Keyboard request:	button	depressing button sets Keyboard Request Indicator and causes a Contingency Interrupt to occur.
Keyboard release:	button	depressing button sets the Keyboard Release Indicator and causes a Contingency Interrupt.
Typewriter on-line: Typewriter off-line:	button-light	depressing button switches the typewriter from off-line to on-line or on-line to off-line.

.3 DISPLAY

.31 Alarms

Name	Form	Function
General Purpose Channels (8): Servo Power supply: Central Processor:	lights and buzzer	when line status light is lit, unit is off-line. When fault light is lit and buzzer sounds, unit has an abnormal condition such as no airflow, overheat, or power failure.

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.32 Conditions

Name	Form	Function
Processor Error Stop:	light	lit when a second Processor Error has occurred while in Processor Error Interrupt Mode, causing a stop condition.
Prevent I/O Interrupt:	light	when Inhibit I/O Interrupt Indicator is set.
Keyboard active:	light	lit by the action of an Activate Keyboard (ACT) Instruction.
Ready:	light	lit when power is supplied.

.33 Control Registers: . . . none.

.34 Storage: . . . . . none.

.4 ENTRY OF DATA

.41 Into Control Registers

(1) Put typewriter on line.
(2) Depress the Keyboard Request button.
(3) Type in data.
(4) Depress Keyboard Release button when all data has been entered.

.42 Into Storage: . . . . . same as Control Register.

.5 CONVENIENCES

.51 Communications: . . . none.

.52 Clock: . . . . . contents of the computer clock may be typed by program control.

.53 Desk Space: . . . . . adequate free work space on either side of the control panel.

.54 View: . . . . . designed for operation by person seated at console desk; unobstructed view in all directions.

.6 INPUT-OUTPUT UNIT

.61 Identity: . . . . . Console Typewriter.

.62 Description: . . . . . the console typewriter has a 51-character set (0 through 9, A through Z, and 15 special characters). The format is program-controlled. Printing is on sprocket fed continuous forms 5-1/2 or 11 inches long by 8-1/2 inches wide including sprocket holes. An original with up to five copies may be produced simultaneously.

.63 Performance: . . . . . the output speed can be ten characters per second. The input speed is governed by the ability of the operator.

INPUT-OUTPUT: CARD READER

§ 071.

.1 GENERAL

.11 Identity: . . . . . 80 column Card Reader. Model No. 4133.

90 column Card Reader. Model No. 4182.

.12 Description

The UNIVAC III card reader has a maximum operating speed of 700 cards per minute and is available in both 80-column and 90-column models. Both models may be included in one system. The 80-column model automatically translates standard Hollerith card code into UNIVAC III character code; it can also process any other 80-column card code. The 90-column model automatically translates 90-column Remington Rand card code into UNIVAC III character code; it can also process any other 90-column card code. Card reading is checked by a hole count check, a modulo 3 check, and the number of memory accesses made. A program-testable indicator is set if an error is detected in any of these checks. The unit has one 2,000-card capacity hopper and three 1,000-card capacity, program-selectable stackers. A variety of read instructions permit reading one card: with or without feeding another card; with or without translation; with or without stacker selection. When a read-with-feed instruction is given, care must be exercised to give another read instruction before the card being fed has reached the reading station; otherwise, the card image is transferred to the last designated read-in area and loss of data results. The entire read operation is performed under control of the reader synchronizer, thereby freeing the processor to continue other operations.

Optional Features:

Eighty-column read feature for 90-column reader permits 80-column cards to be read untranslated on a 90-column card reader.

Ninety-column read feature for 80-column reader permits 90-column cards to be read untranslated on an 80-column card reader.

Stub card feature for the 80-column reader permits reading of one stub card size of 22, 23, 51, or 66 columns in addition to the standard 80-column cards.

Stub card feature for the 90-column reader permits reading of one stub card size of 16/32, 27/54, or 29/58 columns in addition to the standard 90-column card.

.13 Availability: . . . . . February, 1962.

.14 First Delivery: . . . . August, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . . . . pinch roller friction (unclutched).
.212 Reservoirs: . . . . . none.
.213 Feed drive: . . . . . picker knife.
.214 Take-up drive: . . . . pinch roller friction.

.22 Sensing and Recording Systems

.221 Recording system: . . none.
.222 Sensing system: . . . brush.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of read station 1: . reading (hole-count control).
Stacks: . . . . . 1.
Heads/stack: . . . . . 80 or 90.
Method of use: . . . . 1 row at a time.

Use of read station 2: . reading.
Distance: . . . . . 1 card.
Stacks: . . . . . 1.
Heads/stack: . . . . . 80 or 90.
Method of use: . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard 80 or 90 column cards †.
.312 Phenomenon: . . . . . rectangular holes for 80 column cards.
round holes for 90 column cards.

† Eighty-column reader also permits feeding of one stub card size of 22, 23, 51, or 66 columns. Ninety-column reader also permits feeding of one stub card size of 16/32, 27/54, or 29/58 columns.

.32 Positional Arrangement

.321 Serial by: . . . . . 12 rows.
.322 Parallel by: . . . . . 80 or 90 columns at standard spacing.
.324 Track use: . . . . . all for data.
.325 Row use: . . . . . all for data.

.33 Coding: . . . . . column code as in Data Code Table No. 3 and 4.

§ 071.

.34 Format Compatibility

Other device or system: . . . . . all devices using standard 80 or 90-column cards.
Code translation: . . not required.

.35 Physical Dimensions: . standard 80 or 90-column cards.

.4 CONTROLLER

.41 Identity: . . . . . general purpose channel.

.42 Connection to System

.421 On-line: . . . . . 8.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1.
.432 Restrictions: . . . . none.

.44 Data Transfer Control

.441 Size of load

	80 column cards	90 column cards
With translation:	20 words	24 words.
Without translation:	40 words	24 words.

.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . each character.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic within a card, by program for sucessive cards.
.447 Synchronizing aids: . interruption.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 card.
.512 Block demarcation
Input . . . . . fixed.

.52 Input-Output Operations

.521 Input: . . . . . feed 1 card forward and read previous card. Cards are read continuously in this manner until a card read with no feed instruction is given.
.522 Output: . . . . . none.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . variable by program instruction.

	80-column card	90-column card
Translate to UNIVAC III code:	Standard Hollerith	Remington Rand card code.
Use code as is:	any	any.

.54 Format Control: . . . none.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . yes.
Offset card: . . . . . no.
Select stacker: . . . . yes.
Select format: . . . . no.
Select code: . . . . . yes, in "read" command.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: no.
Hopper empty: . . . . yes.
Stacker full: yes.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: . . . . . 700 cards per minute.
.622 Important parameters
Clutch cycle: . . . . 85.8 msec.
.623 Overhead: . . . . . 1 clutch point per cycle.
.624 Effective speeds: . . . 700 cards/minute when reading continuously.
350 cards/minute maximum when reading on demand.

.63 Demands on System

Component	Condition	msec. per card	or Percentage
Core storage:	80-column card with translation	1.92	2.24.
	80-column card with no translation	1.92	2.24.
	90-column card	1.92	2.24.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Feed one card:	button-light	feeds one card and transfers card image without translation to memory.
Operations off-line:	button-light	Places unit either on or off-line.
Abnormal clear	button-light	indicates an abnormal condition in card reader.

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.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	2,000 cards.
Stacker:	1,000 cards.

.732 Replenishment time: . . . . . 0.25 to 0.50 minute reader does not need to be stopped.

.734 Optimum reloading period: . . . . . 2.86 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	hole count check	set indicator and interlock unit.
Input area overflow:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	check	set indicator and interlock unit.
Imperfect medium:	none.	
Timing conflicts:	check	set indicator and interlock unit.
Input area underflow:	check if insufficient data	set indicator and interlock unit.
Transmit data to storage:	modulo 3 check	set indicator and interlock unit.
Feed jam:	check	set indicator and stop drive motor.
Stacker jam:	check	set indicator and stop drive motor.

INPUT-OUTPUT: CARD PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . . 80-Column Card Punch. Model No. 4127.

90-column Card Punch. Model No. 4183.

.12 Description

This punch has a maximum speed of 300 cards per minute and is available in either an 80-column or 90-column model. Both models may be included in the system. The 80-column model automatically translates the UNIVAC III character code into the standard Hollerith card code before punching; it can also punch any other card code. The 90-column model automatically translates the UNIVAC III character code into Remington Rand 90-column card code before punching; it also can punch any other code. Punching is checked by a hole-count check, a modulo 3 check, and the number of memory accesses made. A program-testable indicator is set if an error is detected in any of these checks.

The unit has one hopper with a 1,000-card capacity and two program-selectible stackers, each with a 1,000 card capacity. A variety of punching instructions permit punching one card with or without translation; and with or without stacker selection. The entire punching operation is performed under the control of the punch unit synchronizer, thereby permitting the processor to continue other operations.

.13 Availability: . . . . . February, 1962.

.14 First Delivery: . . . . August, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller friction (clutched).
.212 Reservoirs: . . . . . none.
.213 Feed drive: . . . . . picker knife.
.213 Take-up drive: . . . . pinch roller friction (clutched).

.22 Sensing and Recording Systems

.221 Recording system: . . die punch.
.222 Sensing system: . . . brush.
.223 Common system: . . . no.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . punching.
Stacks: . . . . . 1.
Heads/stack: . . . . . 80 or 90.
Method of use: . . . . 1 row at a time.
Use of station: . . . . check reading.
Distance: . . . . . 1 card.
Stacks: . . . . . 1.
Heads/stack: . . . . . 80 or 90.
Method of use: . . . . 1 row at a time; checking for total holes punched.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard 80 or 90 column punched cards.
.312 Phenomenon: . . . . . punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . 12 rows at standard spacing.
.322 Parallel by: . . . . . 80 or 90 columns at standard spacing.
.324 Track use: . . . . . all for data.
.325 Row use: . . . . . all for data.

.33 Coding: . . . . . Column code as in Data Code Tables No. 3 and 4.

.34 Format Compatibility

Other device or system
All devices using standard 80 or 90-column cards: . . . . . Code translation not required.

.35 Physical Dimensions: . standard 80 or 90-column cards.

.4 CONTROLLER

.41 Identity: . . . . . general purpose channel.

.42 Connection to System

.421 On-line: . . . . . 8.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . none.

.44 Data Transfer Control

.441

Size of load	80-column card	90-column card
With translation:	20 words	24 words
Without translation:	40 words	24 words

§ 072.

.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.
.447 Synchronizing aids: . . check indicators.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . 1 card.
.512 Block demarcation Output: . . . . . size fixed by instruction.

.52 Input-Output Operations

.521 Input: . . . . . none.
.522 Output: . . . . . 1 card forward.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . optional depending on punch unit used.

Translate from UNIVAC III code:	80-column punch to Standard Hollerith	90-column punch to Remington Rand code.
Use code as is:	any	any

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . yes.
Offset card: . . . . . no.
Select stacker: . . . . yes.
Select format: . . . . no.
Select code: . . . . . no.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . yes.
End of medium marks: no.
Hopper empty: . . . . yes.
Stacker full: . . . . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 300 cards/minute.
.622 Important parameters
Clutch cycle: . . . . 200 msec.
Clutch points: . . . . 1.
.623 Overhead: . . . . . 200 msec. per card unless punch instruction is given prior to completion of previous punch command.
.624 Effective speeds: . . . 300 cards/minute.

.63 Demands on System

Component	Condition	msec. per card	Percentage
Core storage	80-column cards	0.96	0.48
	90-column cards	0.96	0.48

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Feed One Card:	button	advances cards one position when unit is off-line.
Operation Off-Line:	button	places unit off-line if on or on-line if off.
Abnormal Clear:	button-light	indicates abnormal conditions in card punch unit.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	1,000 cards.
Stacker:	1,000 cards.

.732 Replenishment time: 0.25 to 0.50 minute. punch does not need to be stopped.
.733 Adjustment time: . . . none.
.734 Optimum reloading period: . . . . . 3.3 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording		
Core storage to synchronizer:	modulo 3 check	set indicator and interlock unit.
Synchronizer to card:	reread for hole count	set indicator and interlock unit.
Output block size:	check	set indicator and interlock unit.
Invalid code:	all codes valid	
Exhausted medium:	check	set indicator and interlock unit.
Imperfect medium:	none.	
Timing conflicts:	check	set indicator and interlock unit.
Feed jam:	check	set indicator and turn drive motor off
Stacker jam:	check	set indicator and turn drive motor off
Full stacker:	check	set indicator and interlock unit.
Empty hopper:	check	set indicator and interlock unit.

INPUT-OUTPUT: PUNCHED PAPER TAPE UNIT

§ 073.

.1 GENERAL

.11 Identity: . . . . . Punched Paper Tape Unit.

.12 Description

The paper tape reader and punch are two separate units housed in the same cabinet with their synchronizer. The synchronizer is connected to one General Purpose Channel, thus permitting only one input or output operation to be executed at a time. However, input and output operations can be intermixed and malfunction of either unit does not affect the operation of the other.

Standard 5-, 6-, 7-, or 8-track tape of 11/16-, 7/8- or 1-inch widths is used. Either strips of tape or 8- or 10½-inch NAB (National Association of Broadcasters) spools with capacities of 500 feet and 1,000 feet respectively can be used on either unit.

The photoelectric reader generally operates at a rate of 500 characters per second; but can also operate at a rate of 250 characters per second. A special non-stop mode can be selected to read from 1,500 to 2,500 characters per second. This mode of operation permits reading a whole reel of tape without stopping. If a reader fault indicator is set while in the non-stop mode, the tape is brought to a slow stop and data between the point of error and the stopping point are skipped. Strips of tape cannot be read in the non-stop mode, nor can 10½-inch spools be read at the rate of 500 characters per second.

The punch operates at a rate of 110 characters per second. For both reading and punching, the external code is the same as the internal code; 1-bits are represented by holes punched in the tape and 0-bits by unpunched positions. Each row on tape appears in the least significant 5-, 6-, 7-, or 8-bits of a UNIVAC III word. Either a variable number from 1 to 126 or a fixed number of 256 characters can be read or punched by one input-output instruction.

Input/Output data are processed (detachable plugboard) which performs the following functions:

For the Reader:

(1) Defines the number of channels to be read.
(2) Permits rearrangement of bits from their tape-channel positions to relatively different bit positions in the UNIVAC III word.
(3) Defines the wired stop code for the reader.
(4) For five-channel tape, specifies the interpretation of space, carriage return, and line feed codes as they individually affect the reader shift status.

.12 Description (Contd.)

(5) Selects whether odd parity, even parity, or no parity checking will be employed.
(6) Can prevent parity bits from entering storage.
(7) Can enter the shift status into storage as a bit.

For the Punch:

(1) Permits rearrangement of bits from their positions in the UNIVAC III word to relatively different positions in the tape channels.
(2) Defines the wired stop code for the punch.
(3) Can cause odd or even parity bits to be generated for punching (however, they are not checked at the punch).
(4) Permits double frame punching for five-channel tape.

.13 Availability: . . . . . September, 1961.

.14 First Delivery: . . . . January, 1961.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller friction.
.212 Reservoirs
Number: . . . . . 2 on reader; none on punch.
Form: . . . . . swinging arm.
Capacity: . . . . . 1.0 to 1.5 ft.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . die punch.
.222 Sensing system: . . . . photoelectric.
.223 Common system: . . . no; separate read and punch units.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . reading.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . reads 1 row at a time.

Use of station: . . . . punching.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . punches 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . paper tape.
.312 Phenomenon: . . . . . punched holes.

§ 073.

.32 Positional Arrangement

.321 Serial by:. . . . . either 1 to 126 (variable), or 256 (fixed) rows, at 10 per inch.

.322 Parallel by:. . . . . 5, 6, 7, or 8 tracks with standard spacing.

.323 Bands: . . . . . none.

.324 Track use

	8-track	7-track	6-track	5-track
Data:	8	7	6	5
Redundancy check:	0	0	0	0
Timing (sprocket track):	1	1	1	1
Control signals:	0	0	0	0
Unused:	0	0	0	0
Total (plus sprocket track):	8	7	6	5

.325 Row use

Data: . . . . . all.
Redundancy check: . . 0.
Timing: . . . . . 0.
Control signals: . . . 0.
Unused: . . . . . 0.
Gap: . . . . . 0.

.33 Coding:. . . . . any 5-, 6-, 7-, or 8-track tape code; code translation is programmed.

.34 Format Compatibility

Other device or system: all devices using standard punched tape.
Code translation: . . . by program.

.35 Physical Dimensions

.351 Overall width:. . . . . 0.686, 0.875, or 1.0 inch.
.352 Length:. . . . . 500 or 1,000 ft. reels.

.4 CONTROLLER

.41 Identity: . . . . . no separate identity; part of punched paper tape unit.

.42 Connection to System

.421 On-line: . . . . . 1 to 8; governed by the physical availability of 1 general purpose channel per unit.

.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 2 (1 reader, 1 punch).
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . either 1 to 126 (variable) or 256 (fixed) words, 1 character per word.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . either 1 to 126 (variable) or 256 (fixed) rows.
.512 Block demarcation
Input: . . . . . "stop" character or count in instruction.
Output: . . . . . "stop" character or count in instruction.

.52 Input-Output Operations

.521 Input: . . . . . either 1 to 126 or 256 words; cut-off by I/O instruction or "stop" character.
.522 Output: . . . . . either 1 to 126, or 256 words; cut-off by I/O instructions or "stop" character.
.523 Stepping: . . . . . backspace 1 frame a reader only.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . end of record by "stop" character code.
.526 Searching: . . . . . none.

.53 Code Translation: . . by program only, at approximately 85 microseconds per character.

.54 Format Control

Control: . . . . . plugboard.
Format alternatives: . indefinite number.
Rearrangement: . . . yes.
Suppress zeros: . . . no.
Insert point: . . . . . no.
Insert spaces: . . . . no.
Define stop code:. . . yes.

.55 Control Operations

Disable:. . . . . no.
Request interrupt: . . yes.
Select format: . . . . yes.
Select code: . . . . . no.
Rewind: . . . . . no.
Unload: . . . . . no.

.56 Testable Conditions

Disabled:. . . . . yes.
Busy device: . . . . . yes.
Nearly exhausted: . . . yes; punch: approximately 80 inches of tape remaining; reader: variable per program.
Busy controller:. . . . yes.
End of medium marks: no.
Parity check: . . . . . yes.

§ 073.

.6 PERFORMANCE

.61 Conditions

I: . . . . . 1,500 char/sec reading.
II: . . . . . 500 char/sec reading.
III: . . . . . 250 char/sec reading.
IV: . . . . . 110 char/sec punching.

.62 Speeds

.621 Normal or peak speed

Condition	Characters/sec
I:	1,500.
II:	500.
III:	250.
IV:	110.

.622 Important parameters
Reader start time: . . 3 msec.
Reader stop time: . . 2 msec.

.623 Overhead
Reader: . . . . . 5 msec.
Punch: . . . . . none (?).

.624 Effective speeds

Condition	Speed
I:	1,500 char/sec. †
II:	500N/ (N + 2.5) char/sec. (?).
III:	250N/ (N + 1.25) char/sec.
IV:	110 char/sec.

N = number of char/block.
† Usable only for reading a whole reel of tape without stopping.

.63 Demands on System

Component	Condition	msec per block	or	Percentage of transfer time
Core storage:	I	0 + 0.004N		0.6%
Core storage:	II	0 + 0.004N		0.2%
Core storage:	III	0 + 0.004N		0.1%
Core storage:	IV	0 + 0.004N		0.004%

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . tape width.
Method: . . . . . movable guide.
Comment: . . . . . 3-position mechanical indented slide.

.72 Other Controls

Reader

Function	Form	Comment
Put reader on-line:	switch.	
Put reader off-line:	switch.	
Set speed to 500 char/sec or 250 char/sec:	switch.	
Put reader in non-stop mode:	switch.	
Clear synchronizer fault:	switch.	
Clear reader fault:	switch.	
Rewind:	switch.	

Punch

Put punch on-line:	switch.	
Put take-up spool on:	switch.	
Clear punch fault:	switch.	
Clear synchronizer fault:	switch.	

.73 Loading and Unloading

.731 Volumes handled
Storage: . . . . . reel.
Capacity: . . . . . 1,000 feet.

.732 Replenishment time: . 0.5 to 1.0 minute. unit needs to be stopped.

.733 Adjustment time: . . . 0.5 to 1.0 minute to adjust tape width guides.

.734 Optimum reloading period in minutes

Condition	500-foot reel	1,000-foot reel
I:	0.66	1.33.
II:	2	not usable.
III:	4	8.
IV:	9	18.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	modulo 3	set indicator.
Reading:	parity and modulo 3	set indicator.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	none.	
Exhausted medium:	check	set indicator.
Imperfect medium:	none.	
Timing conflicts:	none.	

INPUT-OUTPUT: HIGH SPEED PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . . High Speed Printer. Model No. 4152.

.12 Description

The High Speed Printer uses a continuously rotating drum and 128 print hammers which correspond to the 128 printing positions. Documents are printed at a rated peak speed of 922 lines per minute for all-numeric data single-spaced. The minimum speed for continuous single-spaced alphameric data is 700 lines per minute. The print cycle is considered complete when all of the characters have been printed; therefore, effective printed-lines-per-minute depends on the required paper advance and on the group of characters to be printed. Skipping speed is either 20 inches per second for 6 lines per inch or 19½ inches per second for 8 lines per inch. The print instruction may include a skip from 1 to 64 lines. The lack of a true skipping facility is inconvenient and requires the counting of all lines on continuous sheets.

Each printer output operation requires one initiate instruction word and one function specification word. The initiate instruction word causes the function specification word to be placed in the printer standby location. Execution of the function is under control of the printer Synchronizer. The central processor is free for other operation after the Synchronizer has loaded itself with the 32 consecutive core storage words that are to be printed. One printer and its Synchronizer may be connected to any of the eight general purpose channels.

Program-testable indicators are set for: successful completion of a printing function, modulo 3 data error check, fault error check for a physical printer defect, and an out-of-paper warning.

One original with up to five carbon copies can be produced.

.13 Availability: . . . . . February, 1962.

.14 First Delivery: . . . . August, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . 1 set of sprocket drives on each side.

.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . on-the-fly hammer stroke against etched drum.

.222 Sensing system: . . . . none.

.23 Multiple Copies

.231 Maximum number Interleaved carbon: . 1 + 5.

.233 Types of master
Multilith: . . . . . yes.
Spirit: . . . . . yes.

.24 Arrangement of Heads

Use of station: . . . . . printing.
Stacks: . . . . . 1.
Heads/stack: . . . . . 128.
Method of use: . . . . . 1 line at a time.

.25 Range of Symbols

Numerals:	10	0 to 9.
Letters:	26	A to Z.
Special:	18	see below.

Alternatives: . . . . . none.
FORTRAN set: . . . . . yes.
Basic COBOL set: . . . yes.
Total: . . . . . 54.

Special Characters

blank	.
;	=
-	*
:	$
<	(
>	;
+	'
)	/
#	%

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . continuous fan-fold sprocket-punched stationery.

.312 Phenomenon: . . . . . printing.

.32 Positional Arrangement

.321 Serial by: . . . . . 1 line at 6 or 8 per inch.

.322 Parallel by: . . . . . 128 columns at 10 char per inch.

.324 Track use: . . . . . all for data.

.325 Row use: . . . . . all for data.

.33 Coding: . . . . . etched character font.

.34 Format Compatibility: . none.

§ 081.

.35 Physical Dimensions

.351 Overall width: . . . . . 4 to 22 inches by vernier.
.352 Length: . . . . . 1 to 22 by 1/6 inches at 6 lines/inch.
1 to 22 by 1/8 inches at 8 lines/inch.
.353 Maximum margins
Left: . . . . . 18 inches.
Right: . . . . . 18 inches.

.4 CONTROLLER

.41 Identity: . . . . . general purpose channels (functions carried out by programmed instructions).

.42 Connection to System

.421 On-line: . . . . . max. of 8 allowable in a system.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 line of 128 characters.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . no.
.445 Table control: . . . . . no.
.446 Synchronization: . . . . automatic by line; by program for successive line steps.
.447 Synchronizing aids: . . interruption.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 line of 128 characters.
.512 Block demarcation Output: . . . . . 32 sequential storage locations.

.52 Input-Output Operations

.521 Input: . . . . . none.
.522 Output: . . . . . 1 line forward with programmed format control.
.523 Stepping: . . . . . step 1 to 63 lines (via combined step and print instructions).
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . automatic, by controller.

.54 Format Control

Control: . . . . . program.
Format alternatives: . unlimited.
Rearrangement: . . . . by program.
Suppress zeros: . . . . by program.
Insert point: . . . . . by program.
Insert spaces: . . . . . by program.

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . yes.
Select format: . . . . . no.
Select code: . . . . . no.
Suppress print in cycle: no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Nearly exhausted: . . . yes (2.5 inches of paper remain below the printing position).

.6 PERFORMANCE

.61 Conditions

I: . . . . . alphameric data.
II: . . . . . numeric data.

.62 Speeds

.621 Nominal or peak speed: 700 lines per minute (condition I with single spacing).
922 lines per minute (condition II with single spacing).
.622 Important parameters
Skipping speed: . . . . first line 14 inches/sec.
succeeding lines 20 inches/sec.
Paper stabilization: . 10 msec.
.623 Overhead: . . . . . skipping time in msec:
$t = 20 + K(L - 1)$.
L = number of lines skipped.
K = 8.3 for 6 lines/inch spacing or 6.25 for 8 line/inch spacing.
.624 Effective speeds:
Condition I: . . . . . alphameric data at 6 lines per inch spacing:
$\frac{60}{0.085+0.0083(N-1)}$ lines/min.
Condition I: . . . . . alphameric data at 8 lines per inch spacing:
$\frac{60}{0.085+0.00625(N-1)}$ lines/inch
Condition II: . . . . . numeric data at 6 lines per min. spacing:
922 lines/min, where $N < 6$.
461 lines/min, where $5 < N < 12$.
Condition II: . . . . . numeric data at 8 lines per inch spacing:
922 lines/min, where $N < 8$.
461 lines/min, where $7 < N < 16$.
Note: N = lines of spacing.

§ 081.

.63 Demands on System

Component: . . . . . processor.
Condition: . . . . . instructions and transfer time.
Msec per cycle: . . . . 0.140.
or
Percentage: . . . . . 0.22 max.
0.165 min.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Thickness	dial	adjusts printer mechanism for form thickness.
Line position:	dial	vertical alignment.
Form tension:	dial	vertical tension applied to forms.
Form advance:	dial	advances paper.
Left tractor:	dial	adjusts for horizontal position of paper.
Right tractor:	dial	adjusts for horizontal position of paper.

.72 Other Controls

Function	Form	Comment
Carriage in:	button	causes carriage to move into or out of printing position.
Carriage out:	button	causes carriage to move into or out of printing position.
8 lines/inch:	button	select vertical spacing desired.
6 lines/inch:	button	select vertical spacing desired.

.73 Loading and Unloading

.731 Volumes handled

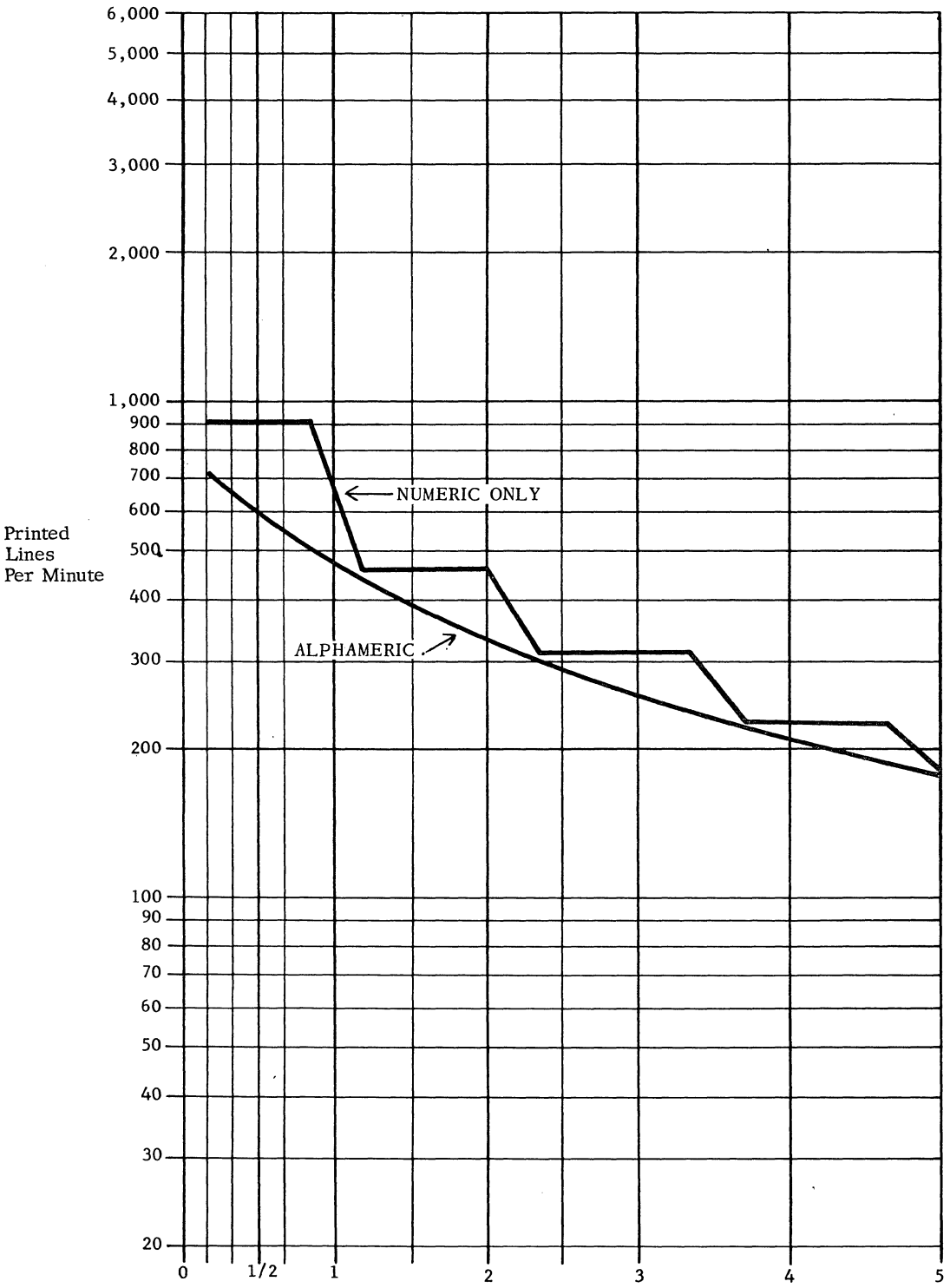
Storage	Capacity
Hopper:	1,000 2-copy forms.
Stacker:	1,000 2-copy forms.

.732 Replenishment time: . . 1 to 2 min. printer needs to be stopped.
.733 Adjustment time: . . . 3 to 5 min.
.734 Optimum reloading period
Period: . . . . . 34 min.
Basis: . . . . . 2-part sets 17 inches long, at 1-inch line spacing.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Output block size:	automatic cut-off.	
Invalid code:	all valid.	
Exhausted medium:	advanced sensing	set indicator.
Imperfect medium:	none.	
Timing conflicts:	none.	
Printer inoperable:	check	set indicator.
Receipt of data:	modulo 3 check	set indicator.

EFFECTIVE SPEED
HIGH SPEED PRINTER MODEL 4152



INPUT-OUTPUT: UNISERVO IIIA

§ 091.

.1 GENERAL

.11 Identity: . . . . . Uniservo IIIA.
Magnetic Tape Unit.
Model No. 4209.

.12 Description

The Uniservo IIIA tape units are the high speed input-output devices for the UNIVAC III Computer system. The tape units are used in conjunction with a Uniservo IIIA Synchronizer. Either one or two Uniservo IIIA Synchronizers, each with up to 16 Uniservo IIIA tape units, can be connected to the UNIVAC III.

Each Synchronizer has two communication channels, one for reading and the other for either writing or reading. These channels function independently; therefore, a variety of simultaneous tape unit operations are possible.

Data is recorded using pulsed-phase modulation at a density of approximately 1,000 frames per inch. A frame contains nine bits, one for each recording track along the tape. Three frames on tape hold one 27-bit UNIVAC III word.

The peak six-bit alphameric character transfer rate is 133,300 characters per second. The peak four-bit decimal digit transfer rate is 200,000 digits per second.

Using 1,000 six-bit alphameric characters per block, the effective transfer rate is 73,900 characters per second. Using 1,000 four-bit decimal digits per block, the effective transfer rate is 91,000 digits per second. The effective transfer rate based on 2,000 character blocks is 99,000 six-bit characters per second or 149,400 four-bit characters per second. A block can contain several different sections, called segments. Each segment is the result of writing from 1 to 511 words from consecutive core storage locations in the gather-write operation. Gather-write and scatter-read operations are important features which, if used properly, reduce the internal processor time usage and increase the effective tape transfer rates by increasing the block size.

The maximum capacity of a 3,500-foot reel of tape is 56,000,000 six-bit alphameric characters. The effective storage on a reel of tape using 1,000 characters per block is 33,600,000 characters. Using 2,000 characters per block, the effective reel storage capacity is as follows: Normal (0.6-inch block gap) 42,000,000 characters; Continuous-write mode (0.4-inch block gap)44,200,000 characters. In the latter mode, the program continuously supplies the synchronizer with Write Function specifications, thereby eliminating the need to stop the tape.

.12 Description (Contd.)

Reading backward may be specified for either the scatter-read or regular block-read instructions. A read-after-write check is provided to ensure the accuracy of recorded data. .An inaccuracy in the recording causes a bad-spot pattern to be recorded on the tape, and a program-testable indicator is set to allow for programmed actions. Subsequent reading of the bad-spot pattern causes a program-testable indicator to be set to allow for programmed action. A write lock-out is obtained by removing a ring in the reel. Numeric designation of tape units is controlled by a plugboard mounted in a cabinet between the power supply and the first tape unit.

Optional Feature

A compatible-mode option is available, making it possible to interchange data tapes with the UNIVAC 490 Real-Time System and the UNIVAC 1107 Thin-Film Memory Computer.

.13 Availability: . . . . . September, 1962.

.14 First Delivery: . . . . February, 1963.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan.
.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum.
Capacity: . . . . . approx. 5 ft.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by a magnetic write head.
.222 Sensing system: . . . . magnetic read head.
.223 Common system: . . . read/write head.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 9.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read/write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 9.
Method of use: . . . . . 1 row at a time.

§ 091.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311	Medium:	mylar tape.
.312	Phenomenon:	magnetization.

.32 Positional Arrangement

.321	Serial by:	3 to 3N rows at 1,000 rows per inch, where N = Number of words per block-segment. maximum N = 511 words.
.322	Parallel by:	9 tracks.
.324	Track use	
	Data:	7.
	Modulo 3 check or data:	2.
	Timing:	0.
	Control signals:	0.
	Unused:	0.
	Total:	9.
.325	Row use	
	Data:	3 to 3N, where N is the number of words.
	Redundancy check:	0.
	Timing:	0.
	Control signals:	0.
	Unused:	0.
	Inter-block gap:	see .622.

.33 Coding

	External:	binary image. 3 rows for 1 word (containing 25 data bits and 2 modulo 3 check bits).

.34 Format Compatibility

Other device or system	Code translation
UNIVAC 490:	compatible mode.
UNIVAC 1107:	compatible mode.

.35 Physical Dimensions

.351	Overall width:	0.5 inch.
.352	Length:	3,500, 1,700, or 625-foot reels available.

.4 CONTROLLER

.41	Identity:	Uniservo IIIA. Synchronizer.

.42 Connection to System

.421	On-line:	2; no restrictions.
.422	Off-line:	none.

.43 Connection to Device

.431	Devices per controller:	1 to 16.
.432	Restrictions:	none.

.44 Data Transfer Control

.441	Size of load:	1 to N words from (or into) different areas of core storage as specified by record definition word.
.442	Input-output areas:	core storage.
.443	Input-output area access:	each word.
.444	Input-output area lockout:	none.
.445	Table control:	yes; scatter-read and gather-write controlled by record definition words.
.446	Synchronization:	automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511	Size of block-segment:	1 to 511 words.
.512	Block demarcation	
	Input:	gap on tape or record definition count.
	Output:	record definition count.

.52 Input-Output Operations

.521	Input:	read one block forward or backward into core storage locations specified by record definition word(s); segments of blocks may be specified by record definition word.
.522	Output:	write one block forward from core storage location specified by record definition word(s).
.523	Stepping:	one block backward or forward.
.524	Skipping:	none.
.525	Marking:	interblock gap, segment marks.
.526	Searching:	none.

.53 Code Translation

	Binary image:	matched.

.54 Format Control

	Control:	program.
	Format alternatives:	1.
	Rearrangement:	yes, scatter-read and gather-write.
	Suppress zeros:	yes, up to 6 numeric characters per word.
	Insert point:	no.
	Insert spaces:	no.
	Recording density:	no.
	Section sizes:	yes.

§ 091.

.55 Control Operations

Disable:	yes, after rewind with interlock.
Request interrupt:	yes, input-output interrupt.
Select format:	no.
Select code:	no.
Rewind:	yes.
Unload:	no.

.56 Testable Conditions

Disabled:	yes.
Busy device:	yes.
Output lock:	yes.
Nearly exhausted:	no.
Busy controller:	no.
End of medium marks:	yes.
Modulo 3 error:	yes.

.6 PERFORMANCE

.61 Conditions: none.

.62 Speeds

.621 Nominal or peak speed:	200,000 decimal characters/sec. or 133,000 alphameric characters/sec.
.622 Important parameters	
Density:	1,000 frames per inch.
Tape speed:	100 inches per second.
Rewind:	125 seconds for 3,500 ft. reel of tape.
Interblock gap:	approximately 0.4 or 0.6 inch.
Start-stop time:	4.25 to 13.2 msec total.
.623 Overhead:	4.25 to 13.2 msec/block.
.624 Effective speeds:	133,000N/(N+800) char/sec. where N = number of 6-bit characters per block. 200,000D/(D+1200) digits/sec. where D = number of 4-bit digits per block.

.63 Demands on System

Component:	core storage.
Condition:	load or unload buffer.
Msec per block-segment: or	0.03 msec. times number of words per block plus number of segments.
Percentage of transfer time:	13.3.

Note: each rewind instruction interlocks storage for 182 to 357 msec.

.7 EXTERNAL FACILITIES

.71 Adjustments: none.

.72 Other Controls

Function	Form	Comment
Forward:	button	set tape for forward operation.
Backward:	button	set tape for backward operation.
Rewind:	button	tape rewinds with interlock.
Change tape:	button	advances tape to load point.
Compatible mode:	button (optional)	for tape units used for compatible mode operations.

.73 Loading and Unloading

.731 Volumes handled

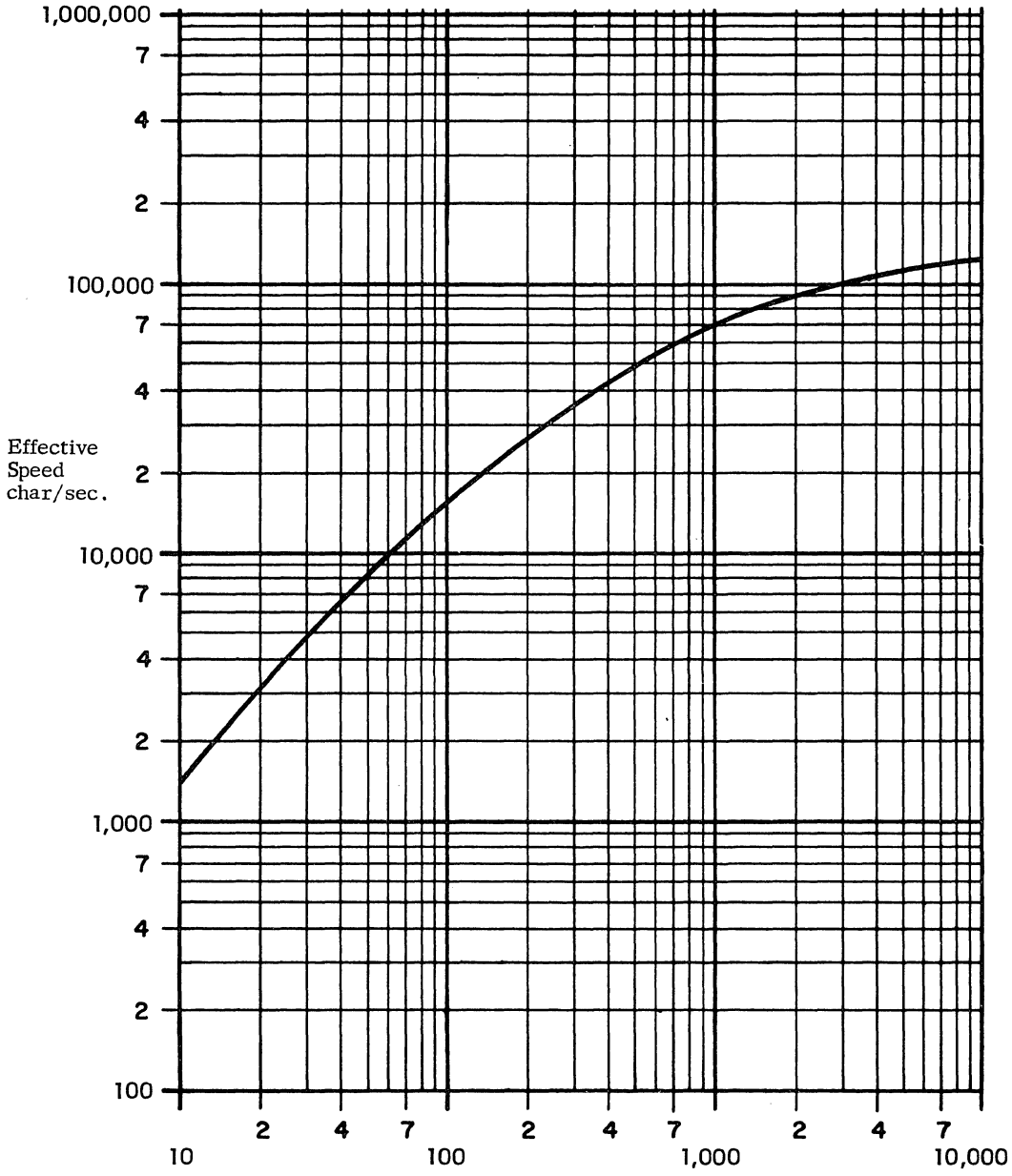
Storage	Capacity
Reel:	3,500 feet or 42,000,000 six-bit alphameric characters blocked 2,000 char per block.

.732 Replenishment time:	0.5 to 2.0 min., tape unit needs to be stopped.
.734 Optimum reloading period:	7.0 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read-after write modulo 3 check	indicator.
Reading:	modulo 3 check	indicator.
Input area overflow:	not possible.	
Output block size:	not possible.	
Invalid code:	all codes valid.	
Exhausted medium:	check	indicator.
Imperfect medium:	check	indicator.
Timing conflicts:	not possible.	

EFFECTIVE SPEED



INPUT-OUTPUT: UNISERVO IIA

§ 092.

.1 GENERAL

.11 Identity: . . . . . Uniservo IIA Tape Unit. Model?

.12 Description

The Uniservo IIA tape units are used in conjunction with a Uniservo IIA synchronizer. Only one Uniservo IIA synchronizer, with up to six Uniservo IIA tape units, can be connected to the UNIVAC III computer system. The address of each tape unit is selected via a patch panel on the synchronizer. Data can be recorded on either Mylar or metallic tapes. Compatibility with the Uniservo I and II is achieved by using packing densities of 250 or 125 8-bit characters per inch, as specified by instruction. With a packing density of 250 characters per inch, a block of 720 characters is read or written at a peak speed of 25,000 characters per second. The effective speed is 18,300 characters per second for the continuous mode of operation and 16,300 characters per second for stop/start mode. With a packing density of 125 characters per inch, six blockettes of 120 characters each, separated by 1.05 inch gaps, are read or written at a peak speed of 12,500 characters per second. The effective speed is 6,800 or 6,500 characters per second, depending upon the mode of operation.

When reading from tape, four 6-bit (plus 1 parity bit) characters are combined to form the first 24 bits of a UNIVAC III word. When writing on tape, the first 24 bits of a UNIVAC III word are used to make four 6-data-bit (plus 1 parity bit) characters on tape.

No automatic check of tape writing occurs. Three levels of amplification can be used when reading: low, normal, and high. Information transferred between the tape and synchronizer is checked for odd parity. Information transferred between the synchronizer and core storage is checked for modulo 3 errors.

A write lockout can be obtained by inserting a ring in the tape reel.

Only tapes that have been edited to mark the flaws should be used. Tapes are edited by first recording a pattern of "all 1's" along the tape and then reading and checking. When bad spots are detected on metallic tape, a special hand punch is used to perforate the tape in that area. When bad spots are detected on Mylar tape, its oxide is manually scraped off, leaving a clear spot on the tape. The limits of the clear spot indicate the start and end of the flaw.

.13 Availability: . . . . . April, 1962.

.14 First Delivery: . . . . July, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . single capstan center drive.
.212 Reservoirs
- Number: . . . . . 2.
- Form: . . . . . vacuum.
- Capacity: . . . . . 6 feet of tape.

.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by a magnetic write head.
.222 Sensing system: . . . . magnetic head.
.223 Common system: . . . . yes, common magnetic read/write head.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read/write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . metal or plastic tape.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . 720 rows at 125 or 250 per inch.
.322 Parallel by: . . . . . 8 tracks.
.323 Bands: . . . . . 1.
.324 Track use
- Data: . . . . . 6 (1 character).
- Redundancy check: . . 1 (odd parity).
- Timing: . . . . . 1 (clock).
- Control signals: . . . 0.
- Unused: . . . . . 0.
- Total: . . . . . 8.

§ 092.

.325 Row use
- Data: . . . . . 720.
- Redundancy check: . . 0.
- Timing: . . . . . 0.
- Control signals: . . . 0.
- Gap: . . . . . 1.05 inches between 720 character blocks (at 250 rows/inch); or 1.05 inches between 120 character blockettes and 2.4 inches between each block of 6 blockettes (at 125 rows/inch).

.33 Coding: . . . . . Univac III 6-bit internal code, as in Data Code Table 1.

.34 Format Compatibility

Other device or system	Code translation
Unityper II:	by program.
Univac Input Verifier:	by program.

.35 Physical Dimensions

.351 Overall width: . . . . 0.5 inch.
.352 Length
- Plastic: . . . . . 2,400 ft.
- Metal: . . . . . 1,500 ft.

.4 CONTROLLER

.41 Identity: . . . . . Uniservo II A Synchronizer Type ?

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 6.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 180 words (720 characters).
.442 Input-output areas: . . . core storage.
.443 Input-output area access: . . . . . addressable bit by bit.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 720 characters (divided into 6 blockettes of 120 characters each at low density).

.512 Block demarcation
- Input: . . . . . fixed by instruction.
- Output: . . . . . fixed by instruction.

.52 Input-Output Operations

.521 Input: . . . . . read 1 block, forward or backward.
.522 Output: . . . . . write 1 block, forward only.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . automatically by pre-edited marked flaws.

.525 Marking
- Metallic type: . . . . holes punched in tape indicate beginning and end of flaws.
- Plastic type: . . . . scraping oxide coating in the flaw area.

.526 Searching: . . . . . none.

.53 Code Translation: . . matched codes.

.54 Format Control

Control: . . . . . program.
Format alternatives: . . none.
Rearrangement: . . . . none.
Suppress zeros: . . . . none.
Insert point: . . . . . none.
Insert spaces: . . . . . none.
Recording density: . . . yes; 125 or 250 rows/inch.
Section sizes: . . . . . fixed.

.55 Control Operations

Disable: . . . . . yes.
Request interrupt: . . . yes.
Select format: . . . . . no.
Select code: . . . . . no.
Rewind: . . . . . yes.
Unload: . . . . . no.
Amplifies gain: . . . . yes (3 levels).

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Output lock: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: . . . . . yes.
Error type: . . . . . yes.

.6 PERFORMANCE

.61 Conditions

I: . . . . . 250 rows/inch in stop/start mode.
II: . . . . . 250 rows/inch in continuous mode.
III: . . . . . 125 rows/inch in stop/start mode.
IV: . . . . . 125 rows/inch in continuous mode.

§ 092.

.62 Speeds

.621 Nominal or peak speed
I: . . . . . 25,000 char/sec.
II: . . . . . 25,000 char/sec.
III: . . . . . 12,500 char/sec.
IV: . . . . . 12,500 char/sec.

.622 Important parameters
250 rows/inch
Cost of gap/block: . . . . . 10.5 msec.
Cost of stop/block: . . . . . 5.0 msec.
125 rows/inch
Cost of gaps/block: . . . . . 76.5 msec.
Cost of stop/block: . . . . . 5.0 msec.

.623 Overhead
I: . . . . . 15.5 msec/block start/stop time.
II: . . . . . 10.5 msec/block gap time.
III: . . . . . 81.5 msec/block start/stop time.
IV: . . . . . 76.5 msec/block gap time.

.624 Effective speeds
I: . . . . . 16,300 char/sec.
II: . . . . . 18,300 char/sec.
III: . . . . . 6,500 char/sec.
IV: . . . . . 6,800 char/sec.

.63 Demands on System

Component	Condition	Msec per block	or Percentage
Central Processor:	select unit	0.012	0.011 to 0.031%.
	load or unload buffer	0.720	0.65 to 1.88%.
	rewind	0.6 (approx.)	

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . metallic to plastic tape.
Method: . . . . . switch.

.72 Other Controls

Function	Form	Comment
Manual run:	switch	manually start or stop unit.
Rewind:	button	manual rewind.
Change tape:	button	returns unit to system control.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel of plastic tape:	2,400 feet, or 5,588,000 characters at 250 rows/inch.
Reel of metal tape:	1,500 feet, or 3,480,000 characters at 250 rows/inch.

.732 Replenishment time: . . 0.5 to 1.0 minute; tape unit power needs to be turned off.
.733 Adjustment time: . . . 0.5 to 1.0 minute.
.734 Optimum reloading period: . . . . . 4.8 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Reading:	row parity check	set indicator.
Input area overflow:	check (720 character count)	set indicator.
Output block size:	check (720 character count)	set indicator.
Invalid code:	not possible.	
Exhausted medium:	check	set indicator.
Imperfect medium:	bad spot check	wait (tape passes), then continue operation.
Timing conflicts:	not possible.	

INPUT-OUTPUT: UNISERVO IIIC

§ 093.

.1 GENERAL

.11 Identity: . . . . . Uniservo IIIC Tape Unit.

.12 Description

The Uniservo IIIC Tape Unit provides peak transfer rates of 22,500 or 62,500 characters per second at recording densities of 200 or 556 characters per inch, respectively. Tape speed is 112.5 inches per second when reading or writing. Six data tracks and one parity track are recorded on half-inch tape. The format is compatible with all IBM tape units except the Model 7340 Hypertape Drive. Up to eight Uniservo IIIC Tape Units can be included in a UNIVAC III system. These units are connected to a Uniservo IIIC Adapter Unit, which is then connected to a Uniservo IIIC Synchronizer. The synchronizer is in turn connected to a General Purpose input-output channel, which controls the communication with core storage. This synchronizer allows only one Uniservo IIIC read or write operation to be performed at one time.

Reading and writing can be performed in either the translate or untranslated mode. In the translate mode each tape row represents one six-bit BCD character and is translated to the corresponding six-bit UNIVAC III character. Four characters make up one UNIVAC III word. In the untranslated mode, each tape row represents six-bits of the UNIVAC III word. Four tape rows make up one UNIVAC III word. Input block length can vary from one character to the capacity of core storage. The read operation is terminated either by a word count in the instruction specification control word or by an inter-block gap on tape. Output block length can vary from 4 characters (1 word) to 8,188 characters (2,047 words). The unit operation is terminated by the word count in the Function Specification control word. Reading or writing operations can be performed in the forward direction only.

Seven-channel two-gap heads provide a read-after-write check on recording. A longitudinal parity check character is written after the last data row in each block. Both longitudinal and row parity are checked during each read operation. Checks are made for end-of-file when reading and for end-of-tape when writing. Abnormal conditions (such as longitudinal and row parity errors, modulo 3 errors, tape skew errors, tape erasure errors) cause a specific indicator to be set which causes an interrupt.

Loading and unloading are facilitated by a detachable tape leader that remains on the take-up reel and in the vacuum columns when the rewound supply reel is removed. The new reel is simply mounted on the hub and the end of its tape is attached to the leader. The entire reloading operation can take as little as 30 seconds.

.13 Availability: . . . . .

.14 First Delivery: . . . .

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan.
.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum.
Capacity: . . . . . approximately 6 feet of tape.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . magnetic write head.
.222 Sensing system: . . . magnetic read head.
.223 Common system: . . . 2-gap head provides read-after-write checking.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . 1 row at a time.

Use of station: . . . . write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . 1 row at a time.

Use of station: . . . . read.
Distance: . . . . . 0.25 inch after write head.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . 1 to 8,188 rows at 200 or 556 rows per inch.
.322 Parallel by: . . . . . 7 tracks.
.323 Bands: . . . . . 1.
.324 Track use
Data: . . . . . 6 (1 character).
Redundancy check: 1 (parity).
Timing: . . . . . 0.
Control signals: . . . 0.
Unused: . . . . . 0.
Total: . . . . . 7.

§ 093.

.325 Row use
- Data: . . . . . 1 to N.
- Redundancy check: 1.
- Timing: . . . . . 0.
- Control signals: . . . 0.
- Unused: . . . . . 0.
- Gap: . . . . . 0.75 inch.

.33 Coding: . . . . . 1 character per row, in IBM 6-bit BCD code or any other 6-bit code.

.34 Format Compatibility

- Other device or system: all IBM 700, 1400, and 7000 series systems via IBM 727, 729, and 7330 Magnetic Tape Units.
- Code translation: . . . none required.

.35 Physical Dimensions

.351 Overall width: . . . . 0.50 inch.
.352 Length: . . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . Uniservo IIIC Synchronizer.

.42 Connection to System

.421 On-line: . . . . . 1.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 2 to 8.
.432 Restrictions: . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 8,188 alphameric characters.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . each character.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block
- Input: . . . . . 1 to N characters; N limited by core storage.
- Output: . . . . . 1 to 8,188 characters.

.512 Block demarcation
- Input: . . . . . interblock gap on tape, or word count in the instruction descriptor.
- Output: . . . . . word count in instruction descriptor.

.52 Input-Output Operations

.521 Input: . . . . . read one block forward only into core storage; stop when gap on tape or specified word count is reached.
.522 Output: . . . . . write one block forward from core storage, followed by 0.75 inch gap.

.523 Stepping: . . . . . 1 block backward (backspace).
3.6 inches to 13 inches forward (to skip and erase defective tape areas.)
.524 Skipping: . . . . . none.
.525 Marking: . . . . . end-of-file mark (≠) after last record in file.
.526 Searching: . . . . . none.

.53 Code Translation: . . . variable; can be automatically translated or used as matched code as specified by instruction.

.54 Format Control

- Control: . . . . . program.
- Format alternatives: 2.
- Rearrangement: . . . none.
- Suppress zeros: . . . none.
- Insert point: . . . . . none.
- Insert spaces: . . . . none.
- Recording density: . . yes.
- Section sizes: . . . . yes.

.55 Control Operations

- Disable: . . . . . yes.
- Request interrupt: . . yes.
- Select format: . . . . yes.
- Select code: . . . . . yes.
- Rewind: . . . . . yes.
- Unload: . . . . . yes.

.56 Testable Conditions

- Disabled: . . . . . yes.
- Busy device: . . . . . yes.
- Output lock: . . . . . yes.
- Nearly exhausted: . . no.
- Busy controller: . . . yes.
- End of medium marks: yes; 14 feet from physical end.

.6 PERFORMANCE

.61 Conditions

- I: . . . . . 200 rows per inch density.
- II: . . . . . 556 rows per inch density.

.62 Speeds

.621 Nominal or peak speed
- I: . . . . . reading at 22,500 char/sec.
- II: . . . . . reading at 62,500 char/sec.
- III: . . . . . writing at 22,500 char/sec.
- IV: . . . . . writing at 62,500 char/sec.

§ 093.

.622 Important parameters

Tape speed: . . . . 112.5 inches/sec.
Start time
read: . . . . . 3.5 msec.
write: . . . . . 4.3 msec.
Stop time
read: . . . . . 8.0 msec.
write: . . . . . 10.2 msec.
Full rewind time: . . 87 seconds.

.623 Overhead

Start-Stop Time
Reading: . . . . . 11.5 msec.
Writing: . . . . . 14.5 msec.

.623 Effective speeds

Condition	Formulae	
I:	$\frac{22,500N}{N+259}$	char/sec.
II:	$\frac{62,500N}{N+719}$	char/sec.
III:	$\frac{22,500N}{N+326}$	char/sec.
IV:	$\frac{62,500N}{N+906}$	char/sec.

(See Graph)

.63 Demands on System

Component	Condition	msec per block or	Percentage of data
Core Storage	I	0 + 0.001N	2.25.
	II	0 + 0.001N	6.25.
	III	0 + 0.001N	2.25.
	IV	0 + 0.001N	6.25.

where N = char/block

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . none.

.72 Other Controls

Function	Form	Comment
Rewind and Unload:	switch indicator	rewinds and positions tape for reading or writing.
Forward tape movement:	switch indicator	sets tape to handle forward movement.
Backward tape movement:	switch indicator	sets tape to handle backward movement.

.73 Loading and Unloading

.731 Volumes handled
Storage: . . . . . reel.
Capacity: . . . . . 2,400 feet; for 1,000-char blocks, 5,000,000 char at 200 char/inch, 11,300,000 chars at 556 char/inch.

.732 Replenishment time: 0.5 to 1.0 minutes. tape unit needs to be stopped.

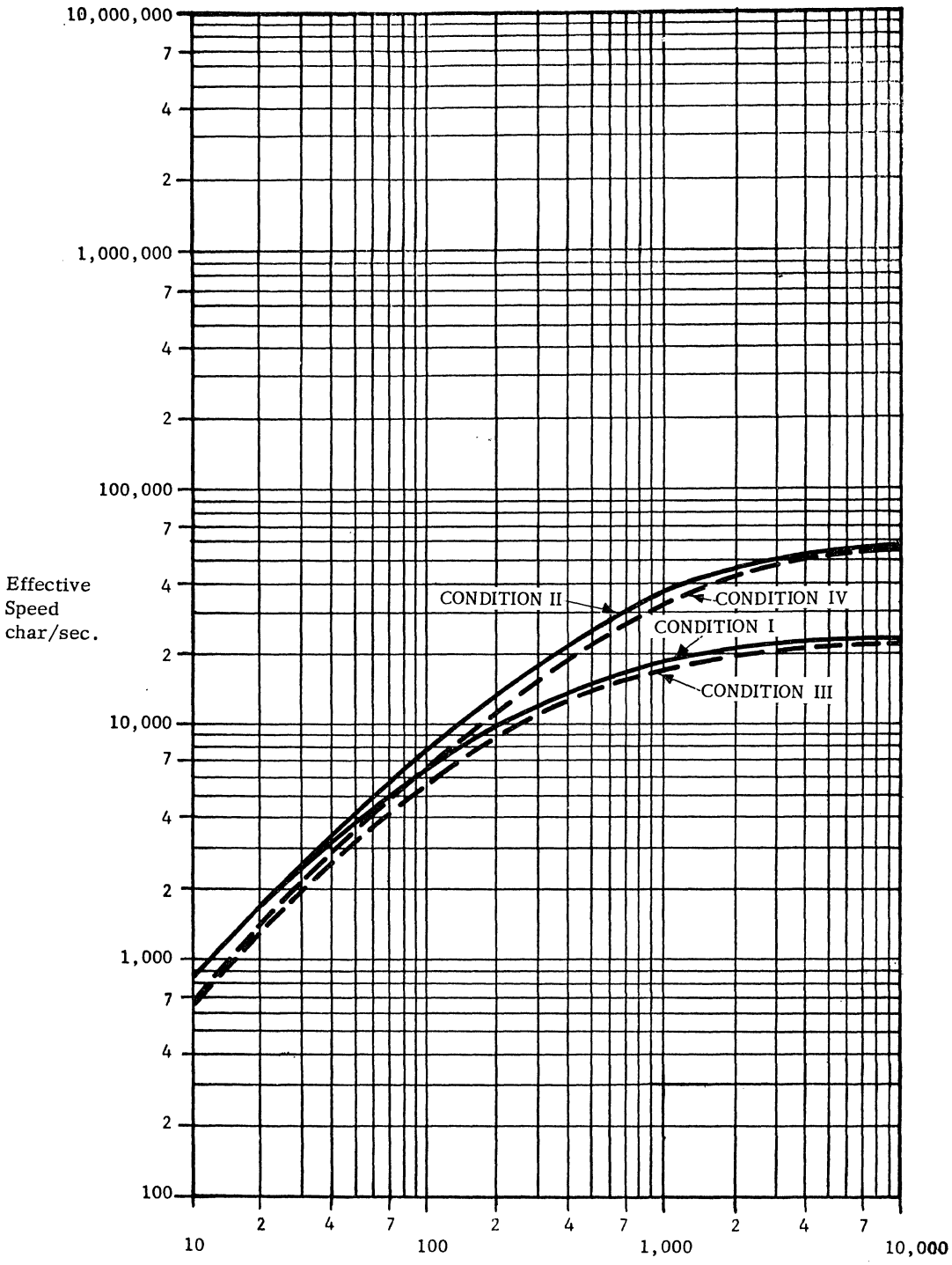
.733 Adjustment time: . . 0.5 to 1.0 minute.

.734 Optimum reloading period: . . . . . 4 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read-after-write with parity check	set indicator.
Reading:	lateral and longitudinal parity.	set indicator.
Input area overflow:	none.	
Input area underflow:	check	set indicator.
Output block size:	check	set indicator.
Invalid code:	none.	
Exhausted medium:	check	set indicator.
Imperfect medium:	none.	
Timing conflicts:	none.	

EFFECTIVE SPEED



SIMULTANEOUS OPERATIONS

§ 111.

.1 SPECIAL UNITS: . . . none.

.12 Description

A major feature of the UNIVAC III is the flexibility and simultaneity of its input-output operations. The UNIVAC III has 13 input-output channels for the transfer of data and control information between the input-output units and the Central Processor. Four channels (two read and two write) are reserved for the Uniservo IIIA tape system; eight channels are general-purpose input-output channels reserved for card-reader units, card-punch units, printers, and other peripheral devices; and one channel is reserved for the Uniservo IIA tape system as a read-write channel.

Each channel has an input-output synchronizer for control functions of the unit(s) on the channel. This feature makes it possible for input-output operations to proceed in parallel with one another and with operations of the Central Processor.

Requests for access to core storage are serviced by the automatic Program Interrupt and the priority circuits of the control unit in the following sequence:

1. Uniservo IIIA synchronizers
2. Uniservo IIA synchronizers
3. General-purpose input-output channels
4. Central Processor operand access
5. Central Processor instruction access

The criteria for establishing this priority order are the repetition rate of storage access demands and the consequence of not gaining access in time; the processor can wait indefinitely without danger of error or loss of information. Priority order for other units is in accordance with the relative data transfer rates of the input-output devices. This method of handling simultaneous operations is straight-forward and efficient.

Several programs can be run simultaneously on the UNIVAC III. Such operation is facilitated by software packages designed to allocate available processing time to the various programs running concurrently. Central processor time is allocated by using the automatic program interrupt as a clock.

.12 Description (Contd.)

For example, program "A" controls the central processor until an automatic program interrupt occurs or a request for input-output operation is initiated. At this time, program "B" is given control until a like condition occurs. Program "C" then gets control, and similarly, "D", "E", etc., until all of the programs have had a turn at which time program "A" once again gets control. This method of control permits optimum utilization of central processor time and peripherals.

Console Typewriter operations are buffered separately and can occur similtaneously with other operations in the same manner as described above.

Optional Feature:

A "Read-Read" feature is available, which permits two reading operations to be performed simultaneously through one Uniservo IIIA Synchronizer.

.2 CONFIGURATION CONDITIONS: . . . . none.

.3 CLASSES OF OPERATIONS

Class	Member
A :	read card.
B :	punch card.
C :	print line.
D :	advance forms on printer.
E :	read magnetic tape.
F :	write magnetic tape.
G :	rewind magnetic tape.
H :	read or write on console typewriter.
I :	processing in Central Processor.

.4 RULES

a + b + c + d	= at most, 8.
f	= at most, S plus T.
e + f	= at most, 2S plus T.
e + f + g	= at most, 16S plus 6T.
h	= at most, 1.
i	= at most, 1.
a + b + c + d + e + f + h + i	= at most, 10 plus 2S plus T.
a + b + c + d + e + f + g + h + i	= at most, 10 plus 16S plus 6T.

where S = number of Uniservo IIIA synchronizers (2 max).
T = number of Uniservo IIA synchronizers (1 max).

§ 121. INSTRUCTION LIST

INSTRUCTION						OPERATION
SALT CODE	IA/FS	X	OP	AR/XO/CH/OI	M/SC/IND/CI	
						Arithmetic
A	IA/FS	X	20	AR	M/IND	$(AR_i) + (M') \rightarrow AR_i$.
AH	IA/FS	X	22	AR	M/IND	$(AR_i) + (M') \rightarrow AR_{i'}$; where i' > i.
BA	IA/FS	X	24	AR	M/IND	Binary $(AR_i) + (M') \rightarrow AR_i$.
BAH	IA/FS	X	26	AR	M/IND	Binary $(AR_i) + (M') \rightarrow AR_{i'}$, where i' > i.
BS	IA/FS	x	25	AR	M/IND	Binary $(AR_i) - (M') \rightarrow AR_i$.
BSH	IA/FS	X	27	AR	M/IND	Binary $(AR_i) - (M') \rightarrow AR_{i'}$, where i' > i.
S	IA/FS	X	21	AR	M/IND	$(AR_i) - (M') \rightarrow AR_i$.
SH	IA/FS	X	23	AR	M/IND	$(AR_i) - (M') \rightarrow AR_{i'}$, where i' > i.
D	IA	X	31	AR1, AR2	M/IND	(AR1, AR2) ÷ (M') ⟶ AR1 remainder, AR2 quotient.
M	IA	X	30	AR1, AR2, AR3	M/IND	(M') X (AR1) ⟶ AR2 6MSD, AR3 6LSD.
IX	IA	X	52	XO	M/IND	(XO) ± (M') 9LSB ⟶ XO.
						Logic
TEQ	IA	X	60	OI	M/IND	Jump to M if Equal indicator is set.
THI	IA	X	60	OI	M/IND	Jump to M if High indicator is set.
TLO	IA	X	60	OI	M/IND	Jump to M if Low indicator is set.
TPOS	IA	X	60	OI	M/IND	Jump to M if Sign of Arithmetic Register is positive.
TUN	IA	X	06	-	M/IND	Jump to M unconditionally.
TR	IA	X	07	CH	M/IND	Transfer 1 plus contents of Control Counter on designated memory address counter into M' and replace the contents of the counter with M' + 1.
TSI	IA	X	60	OI	M/IND	Jump to M if Sense indicator specified is set.
TCI	IA	X	64	OI	CI	Jump 1 instruction if Contingency indicator specified is reset.
TPE	IA	X	64	OI	CI	Jump 1 instruction if Processor-Error indicator specified is reset.
TIO	IA	X	64	OI	CI	Jump 1 instruction if Input-Output indicator specified is reset.
TIOP	IA	X	60	OI	M	Jump to M if Inhibit Input-Output Interrupt indicator is set.
ICX	IA	X	53	XO	M/IND	$(XO_i) + 9LSB\ (M') \rightarrow XO_i$; $\lvert (XO_i) \rvert : \lvert (m') \rvert$ bits 10 through 24. Appropriate comparison indicator set after comparison.
SUP	IA/FS	X	15	AR	M/IND	(AR_i) OR $(M') \rightarrow AR_i$.
ERS	IA/FS	X	16	AR	M/IND	(AR_i) AND $(M') \rightarrow AR_i$.
C	IA/FS	X	54	AR	M/IND	$(AR_i) : (M')$; algebraic comparison; appropriate comparison indicators set.
CA	IA/FS	X	55	AR	M/IND	$\lvert (AR_i) \rvert : \lvert (M') \rvert$; absolute value comparison; appropriate comparison indicators set.
CONE	IA/FS	X	57	AR	M/IND	$(AR_i) : (M')$ for 1-bits; if M' contains 1-bit in every position AR_i has 1-bit, equal indicator set; otherwise high indicator set.
CZRO	IA/FS	X	56	AR	M/IND	$(AR_i) : (M')$ for 0-bits; if M' contains 0-bit in every position where AR_i contains 1-bit equal indicator set; otherwise high indicator set.
						Data Transfer
L	IA/FS	X	12	AR	M/IND	$(M') \rightarrow AR_i$.
LCS	IA/FS	X	13	AR	M/IND	$-(M') \rightarrow AR_i$.

§ 121. INSTRUCTION LIST (Contd.)

INSTRUCTION						OPERATION
SALT CODE	IA/FS	X	OP	AR/XO/CH/OI	M/SC/IND/CI	
						Data Transfer (Contd.)
EXT	IA/FS	X	14	AR	M/IND	(M') → AR_i (M' is defined by field select word).
ST	IA	X	10	AR	M/IND	(AR_i) → M'.
STCS	IA	X	11	AR	M/IND	- (AR_i) → M'.
SR	IA	X	40	AR	SC	Shift (AR_i) right SC decimal digits.
SL	IA	X	41	AR	SC	Shift (AR_i) left SC decimal digits.
SAR	IA	X	42	AR	SC	Shift (AR_i) right SC alphameric characters.
SAL	IA	X	43	AR	SC	Shift (AR_i) left SC alphameric characters.
SBC	IA	X	44	AR	SC	Shift (AR_i) binary circular right SC bit positions with sign.
LX	IA	X	51	XO	M/IND	(M') 15LSB → XO.
STX	IA	X	50	XO	M/IND	(XO) → M' 15LSB.
ATD	IA	X	72	AR	M/IND	Convert alphameric to decimal (M' - 2, M' - 1, M') → AR_i - 1, AR_i.
DTA	IA	X	71	AR	M/IND	Convert decimal to alphameric (AR_i - 1, AR_i) → M' - 2, M' - 1, M'.
ZUP	IA	X	73	AR	M/IND	Zero suppress (M') → AR_i; replaces the following leading alphameric characters with space codes: semicolon, minus, zero, comma.
						Input-Output
IOF	IA	X	70	CH	M/IND	Initiate I/O function; (M') → channel stand-by location; set stand-by location Interlock indicator.
ACT	0	0	66	O	Binary 0's	Activate typewriter keyboard.
WT	IA	X	02	OI	M/IND	Type one character.
RT	0	0	01	AR	Binary 0's	Add alphameric character in typewriter buffer register to AR designated.
RIO	IA	X	65	CH	CI	Reset I/O indicator(s) specified.
AIO	0	-	61	OI	-	Allow I/O interrupt.
PIO	0	-	62	OI	-	Prevent I/O interrupt.
						Miscellaneous
SSI	0	-	62	OI	-	Sense indicator specified set.
RSI	0	-	61	OI	-	Sense indicator specified reset.
RCI	IA	X	65	OI	CI	Contingency indicator(s) specified reset.
RPE	IA	X	65	OI	CI	Processor Error indicator(s) specified reset.
NOP	-	-	00	-	-	No operation.
STMC	IA	X	04	OI	M/IND	Memory Address counter (MAC) → M' 15LSB stored.
STCR	IA	X	05	OI	M/IND	Tape Control Word register (TCWR) → M' stored.
WAIT	IA	X	77	-	M	Stop; then Jump to M'.
LT	0	0	76	AR	Binary 0's	Clock → AR_i; if time valid Jump 1 instruction; if time invalid, go to next instruction.
DIS	IA	X	03	0000	M/IND	Display memory (M') → Memory Information display on the engineer's maintenance panel.

§ 121. INSTRUCTION LIST (Contd.)

INSTRUCTION						OPERATION
SALT CODE	IA/FS	SERVO NUMBER (SN)	FUNCTION CODE (FC)	AUTO INTERRUPT	L ADDRESS (NOT INDEXABLE)	
						Uniservo III Tape Units
BCSR	FS	SN	FC	AI	L-ADD	Backward contingency scatter read.
BBR	FS	SN	FC	AI	L-ADD	Backward 1 block read.
BSR	FS	SN	FC	AI	L-ADD	Backward scatter read.
BCBR	FS	SN	FC	AI	L-ADD	Backward contingency block read.
FCSR	FS	SN	FC	AI	L-ADD	Forward contingency scatter read.
FBR	FS	SN	FC	AI	L-ADD	Forward 1 block read.
FSR	FS	SN	FC	AI	L-ADD	Forward scatter read.
FCBR	FS	SN	FC	AI	L-ADD	Forward contingency block read.
GWT	FS	SN	FC	AI	L-ADD	Gather write.
OWT	FS	SN	FC	AI	L-ADD	Write bad spot pattern, then gather write.
RW	FS	SN	FC	AI	-	Rewind to load point.
RWI	FS	SN	FC	AI	-	Rewind with interlock.
						Uniservo II Tape Units
CBRH	FS	SN	FC	AI	L-ADD	Compatible backward read high.
CBRL	FS	SN	FC	AI	L-ADD	Compatible backward read low.
CBRN	FS	SN	FC	AI	L-ADD	Compatible backward read normal.
CFRH	FS	SN	FC	AI	L-ADD	Compatible forward read high.
CFRL	FS	SN	FC	AI	L-ADD	Compatible forward read low.
CFRN	FS	SN	FC	AI	L-ADD	Compatible forward read normal.
CRW	FS	SN	FC	AI	L-ADD	Compatible rewind.
CRWI	FS	SN	FC	AI	L-ADD	Compatible rewind with interlock.
CWRT	FS	SN	FC	AI	L-ADD	Compatible write.
CWSD	FS	SN	FC	AI	L-ADD	Compatible write subdivide.
						High Speed Reader
CAD	FS	-	FC	AI	L-ADD	No feed, read card, place previous card in stacker 0.
CS1	FS	_	FC	AI	L-ADD	No feed, read card, place previous card in stacker 1.
CS2	FS	-	FC	AI	L-ADD	No feed, read card, place previous card in stacker 2.
CT	FS	-	FC	AI	L-ADD	No feed, read card, place previous card in stacker 0.
CTS1	FS	-	FC	AI	L-ADD	No feed, read card, place previous card in stacker 1.
CTS2	FS	-	FC	AI	L-ADD	No feed, read card, place previous card in stacker 2.
FC	FS	-	FC	AI	L-ADD	Feed card, read card, place previous card in stacker 0.
FCS1	FS	-	FC	AI	L-ADD	Feed card, read card, place previous card in stacker 1.
FCS2	FS	-	FC	AI	L-ADD	Feed card, read card, place previous card in stacker 2.
FCT	FS	-	FC	AI	L-ADD	Feed card, translate card, place previous card in stacker 0.
FCTS1	FS	-	FC	AI	L-ADD	Feed card, translate card, place previous card in stacker 1.
FCTS2	FS	-	FC	AI	L-ADD	Feed card, translate card, place previous card in stacker 2.
						Card Punch
CCS	FS	-	FC	AI	L-ADD	Select stacker 1.
PC	FS	-	FC	AI	L-ADD	Feed card, punch card, place previous card in stacker 0.
PCS	FS	-	FC	AI	L-ADD	Feed card, punch card, place previous card in stacker 1.
PCT	FS	-	FC	AI	L-ADD	Feed card, translate card, place previous card in stacker 0.
PCTS	FS	-	FC	AI	L-ADD	Feed card, translate card, place previous card in stacker 1.

§ 121. INSTRUCTION LIST (Contd.)

INSTRUCTION						OPERATION
SALT CODE	IA/FS	SERVO NUMBER (SN)	FUNCTION CODE (FC)	AUTO INTERRUPT	L ADDRESS (NOT INDEXABLE)	
						High Speed Printer
PAD	FS	Note 1	Note 1	AI	L-ADD	Paper advance.
PRT	FS	Note 1	Note 1	AI	L-ADD	Paper advance, print 1 line.
						Paper Tape
PTP	FS	Note 2	Note 2	AI	L-ADD	Punch (specified number of words).
PTR	FS	Note 2	Note 2	AI	L-ADD	Read (specified number of words).
PTB	FS	Note 2	Note 2	AI	L-ADD	Back space (1 frame).

Note 1: Field specifies number of lines of vertical spacing and function code.
Note 2: Field specifies number of words and function code.

INSTRUCTION LIST NOMENCLATURE

Symbol	Definition
AI:	Allow interrupt indicator (1 = allow interrupt, 0 = inhibit interrupt).
AR:	Any arithmetic register.
AR_i:	Arithmetic register designated.
AR_i':	Arithmetic register designated (higher than i).
AR1:	Arithmetic register 1.
AR2:	Arithmetic register 2.
AR3:	Arithmetic register 3.
AR4:	Arithmetic register 4.
CH:	Channel for I/O operation.
CI:	Contingency indicator.
FC:	Function code.
FS:	Field Selection indicator.
IA:	Indirect Address indicator.
IND:	Indirect address.
L-ADD:	Unindexed address of operand.
LSB:	Least significant bit.
LSD:	Least significant digit.
M:	Address of operand.
M':	Contents of operand.
MAC:	Memory Address counter.
MSD:	Most significant digit.
OI:	Object indicator address.
OP:	Octal Operation Code.
SC:	Shift count.
SN:	Tape unit number.
TCWR:	Tape Control Word register.
X:	Incrementing Index Register.
XO:	Object Index Register.

```
  SEGMENT  001                SALT  PARALLEL  CODEDIT  OF  ROUTINE  SIMLSA          11-21-62                    PAGE     0012
ITEM NO.   TAG    C FORM ...............CONTENT.....•.......... MF   OCTAL    S.....OBJECT  CODE.....•    BLK WD OCTAL WD EW
                          ST•2• DEL SET•                          0  00470    0  04   100200    01301    008 31 20411301
                          TUN•P3•                                 1  00471    0  01   06  00    00462    008 32 04300462
           P4             C•1• A/(   A) •                         0  00472    0  07   541000    00316    008 33 36620316
                         TLO•START3+8•                            1  00473    0  01   60  05    00147    008 34 07012147
                                                                                                  0101    008 35
                          C•1• A/(   F) •                         0  00474    0  07   541000    00320    008 36 36620320
                         THI•START3+9•                            1  00475    0  01   60  07    00150    008 37 07016150
                          BS•1• DB/9 •    •AEQ11•                 0  00476    0  07   251000    00220    008 38 35260220
                          TU•P3•                                  1  00477    0  01   06  00    00462    008 39 04300462
                                                                                                  0101    008 40
           P5             4•L•2••                                 0  00500    0  04   120200    00000    008 41 20510000
                          ERS•2• DB/7777 •                        0  00501    0  07   140200    00300    008 42 34710300
                         C•2•A/(  09)•                            0  00502    0  07   540200    00324    008 43 36610324
                          THI•P0•                                 1  00503    0  01   60  07    00517    008 44 07016517
                                                                                                  0001    008 45
                          C•2• A/(   0) •                         0  00504    0  07   540200    00312    008 46 36610312
                         TLO•START3+10•                           1  00505    0  01   60  05    00151    008 47 07012151
                          BS• 2• DB/3 •                           0  00506    0  07   250200    00217    008 48 35250217
           X3             ST•2•T+8•                               0  00507    0  05   100200    00372    008 49 24410372
                                                                                                  0100    008 50
                          L••1••SERVOERD•                         0  00510    0  07   121000    00203    008 51 34520203
                          BA•1•T+9•                               0  00511    0  05   241000    00373    008 52 25220373
                          ST•1•T+9•                               0  00512    0  05   101000    00373    008 53 24420373
                          IA••ST•2•T+9•  •SV TBL HAS CORR EN      0  00513    1  05   100200    00373    008 54 24410373
                                                                                                  0000    008 55
                          ICX•4•XMOD98•                           1  00514    0  07   53  04    00157    008 56 36550157
           XMOD98  * xMOD  ZER-1 +48•+1•                                                          11167
                          TEQ•P0•                                 1  00515    0  01   60  06    00523    008 57 07014523
                          TU•X2•                                  1  00516    0  01   06  00    00446    008 58 04300446
           P6             C•2•A/(  10)•                           0  00517    0  07   540200    00326    008 59 36610326
                                                                                                  1110    008 60
                         THI•START3+11•                           1  00520    0  01   60  07    00152    009 01 07016152
                          BS•2•DB/371•  •MAKES  11  EQ 12         0  00521    0  07   250200    00270    009 02 35250270
                          TU•X3•                                  1  00522    0  01   06  00    00507    009 03 04300507
           XPAK2   * xPAK  •ERR••                                                                 11013
                   -      63•START 7•
                   -      •
           XLIST2  * xLST   1••XPAK2 + 2 •                                                        11040
```

CODING SPECIMEN: UTMOST ASSEMBLER PRINTOUT

§ 132.

.1 CODING SPECIMEN

A	B	C	D	E	F	G		
0311		03	0435	10435	03 24 04 1033		BA	A2,BASELOCA
0312		03	0436	10436	03 10 04 1104		SA	A2,TS
0313		03	0437	10437	03 51 02 1104		LX	2,TS
0314		03	0440	10440	03 12 10 1117		LA	A1,B0
0315		03	0441	10441	03 54 02 1110		C	A3,D0
0316		03	0442	10442	03 60 06 0452		JF	ST0
0317		03	0443	10443	03 21 02 1151		DS	A3,D50
0318		03	0444	10444	03 54 02 1110		C	A3,D0
0319		03	0445	10445	03 60 06 0450		JF	ST2
0320		03	0446	10446	03 60 05 0451		JL	ST1
0321		03	0447	10447	03 24 10 1114	ST3	BA	A1,B1
0322		03	0450	10450	03 24 10 1114	ST2	BA	A1,B1
0323		03	0451	10451	03 24 10 1114	ST1	BA	A1,B1
0324		03	0452	10452	03 10 10 1113	ST0	SA	A1,SL
0325		03	0453	10453	-03 06 00 0367		J	*FINDHEAD
0326		03	0454	10454	00 00 00 0000	LOOP	NOP	
0327		03	0455	10455	03 51 04 1172		LX	4,SEGAD
0328		03	0456	10456	02 12 14 0001		LA	A12,1,2
0329		03	0457	10457	-03 43 14 1113		ASL	A12,*SL
0330		03	0460	10460	04 10 10 1035		SA	A1,SP-SW1C,4
0331		03	0461	10461	03 53 04 1224		IXC	4,(SW1C+16,1)
0332		03	0462	10462	-03 60 06 0454		JF	*LOOP
0333		03	0463	10463	03 53 02 1165		IXC	2,LIMT

Legend

A: 4-digits, line number assigned by UTMOST.
B: n digits of ERROR codes, alpha or special character.
C: 2 digits, index register covering the object code.
D: 4 digits, the segment relative location counter from 0000_8 to 2000_8.
E: 5 digits, the program relative location counter from 00000_8 to the limit of program memory.
F: 10 digits, octal representation of assembled object code.
G: n digits, original source code input to UTMOST.

DATA CODE TABLE NO. 1

§ 141.

.1 USE OF CODE: . . . . internal alphameric data.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 6 bits.

.22 Character Structure

.221 More significant pattern: 2 bits; 32, 16.
.222 Less significant pattern: . . . . . 4 bits; 8, 4, 2, 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	Blank	+		
1	&	)	*	(
2	-	.	$	,
3	0			'
4	1	A	J	/
5	2	B	K	S
6	3	C	L	T
7	4	D	M	U
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H	Q	Y
12	9	I	R	Z
13	:	=		
14	<			
15	>			

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE: . . . . High Speed Printer.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: 2 bits; 32, 16.
.222 Less significant pattern: . . . . . 4 bits; 8, 4, 2, 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	Space	+		
1	;	)	*	(
2	-	.	$	,
3	0			'
4	1	A	J	/
5	2	B	K	S
6	3	C	L	T
7	4	D	M	U
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H	Q	Y
12	9	I	R	Z
13	:	=		
14	<			
15	>			

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . . punched cards (80-column).

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 1 column.

.23 Character Codes

UNDERPUNCH	OVERPUNCH			
	None	12	11	0
None	Blank	+		
------	-----	-----	-----	-----
------	-----	-----	-----	-----
0	0			
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
--------	-----	-----	-----	-----
8-3	=	.	$	,
8-4	'	)	*	(
1-4-8	;			
4-6-8	:			
4-5-8	<			
3-5-8	>			

DATA CODE TABLE NO. 4

§ 144.

.1 USE OF CODE: . . . . punched cards (90-column).

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 punch positions per character; 2 characters per card column.

.23 Character Codes

Upper entry represents the card punching positions.
Lower entry represents the character.
The table parameter represents the character structure in Core Storage.

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	Blank Space	01357 +		
1	1357 ;	1379)	01 *	015 (
2	0357 -	1359 .	01359 $	0359 ,
3	0 0			1579 '
4	1 1	159 A	135 J	3579 /
5	19 2	15 B	359 K	157 S
6	3 3	07 C	09 L	379 T
7	39 4	035 D	05 M	057 U
8	5 5	03 E	059 N	039 V
9	59 6	179 F	13 O	037 W
10	7 7	57 G	137 P	079 X
11	79 8	37 H	357 Q	139 Y
12	9 9	35 I	17 R	579 Z
13	01379 :	0157 =		
14	13579 <			
15	0579 >			

DATA CODE TABLE NO. 5

§ 145.

.1 USE OF CODE: . . . . Console Typewriter.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . . 2 bits; 32, 16.
.222 Less significant pattern: 4 bits; 8, 4, 2, 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	Space	+	5	$
1	:	)	*	(
2	-	.	$	,
3	0	CR & LF	RB	'
4	1	A	J	/
5	2	B	K	S
6	3	C	L	T
7	4	D	M	U
8	5	E	N	V
9	6	F	O	W
10	7	G	P	X
11	8	H	Q	Y
12	9	I	R	Z
13	:	=	2	:
14	<	-	HT	FF
15	>	0	4	U

CR & LF - Carriage return and line feed.
RB - Ring bell.
HT - Horizontal tab.
FF - Form feed.

DATA CODE TABLE NO. 6

§ 146.

.1 USE OF CODE: . . . . internal collating sequence.

.2 STRUCTURE OF CODE

In ascending sequence:

blank	H
&	I
-	=
0	*
1	$
2	J
3	K
4	L
5	M
6	N
7	O
8	P
9	Q
:	R
<	(
>	,
+	'
)	/
.	S
A	T
B	U
C	V
D	W
E	X
F	Y
G	Z

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers

UNIVAC I/II
Reference: . . . . . UNIVAC Publication UT 2505.
Date available: . . . . currently available.
Description:
The UNIVAC I/II Simulator enables a UNIVAC III system to simulate UNIVAC I and II systems, including off-line peripherals. The Simulator package consists of the following seven routines:

UNIVAC I/II Dynamic Interpretative Simulator
This routine interprets the original machine instructions and performs their functions on UNIVAC III by duplicating the memory registers, adder, and control circuitry of UNIVAC I or II.

The Simulator is a tape-to-tape processing program which requires 16,000 UNIVAC III core storage locations and as many Uniservo IIIA Tape Units as the UNIVAC I/II system being simulated. The input data (converted from UNIVAC I/II tape by a routine to be described later) must be written on Uniservo III tapes. The original format and character structure of UNIVAC I/II tapes is maintained.

It is not possible to carry alphabetics in the simulated control counter. No error indication is provided for the foregoing restrictions; therefore, it is important to know that this condition will never occur, regardless of the input data used, before simulation is attempted. The Simulator does not have the ability to simulate the addition of a space code (bit structure 000001) to an ignore code (bit structure 000000).

Run time of the simulator approximates that of the UNIVAC II. A trace routine, which can be optionally activated or ignored by the user, is included within the Simulator.

Instruction Tape Copier, UNIVAC I/II to UNIVAC III
This routine operates within tape speed and requires approximately 600 UNIVAC III core storage locations, one Uniservo II tape unit, and one Uniservo III tape unit.

Data Tape Copier, UNIVAC III to UNIVAC I/II
This routine operates within tape speed and requires approximately 1,000 UNIVAC III core storage locations; two Uniservo II tape units, and two Uniservo III tape units.

Data Tape Copier, UNIVAC I/II to UNIVAC III
This routine operates within tape speed and requires approximately 1,000 UNIVAC III core storage locations, two Uniservo II tape units, and two Uniservo III tape units.

.11 Simulators of Other Computers (Contd.)

Off-Line Card-to-tape Converter Simulator
This routine operates within maximum card reader speed and requires approximately 1,000 UNIVAC III core storage locations, one card reader, and one Uniservo III tape unit.

Off-Line Tape-to-Card Converter Simulator
This routine operates within maximum card punch speed and requires approximately 600 UNIVAC III core storage locations, one Uniservo III tape unit, and one card punch unit.

Off-Line High Speed Printer Simulator
This routine operates within maximum printing speed and requires approximately 2,000 UNIVAC III core storage locations, one Uniservo III tape unit, and one high speed printer.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

SODA SORT
Reference: . . . . . UNIVAC Publication UT 2504.
Record size: . . . . . variable by full words; 511 words maximum without own coding.
Block size: . . . . . variable by full words; determined by available storage, or key may contain as many words as the item.
Key size: . . . . . up to 3 words; no limit to number of keys.
File size: . . . . . 1 reel of magnetic tape.
Number of tapes: . . . 3 to 6 units.
Date available: . . . . currently available.
Description:
The SODA Sort is a sort generator that produces a sort routine which will become an integral part of a run. The initial input and the final output must be handled by "own coding". The intermediate input-output passes are handled by the generated routine. Provision has been made to facilitate handling "own coding" routines in each merge pass of the sort.

The first pass of the sort operates on a replacement selection method, thereby taking advantage of biased input to form longer strings - the cascade method of merging is used in all collating passes. The user can control the amount of core storage and the number of tape units made available to the sort routine. The sort will operate under control of CHIEF, the UNIVAC III Executive routine, making it capable of concurrent operation with other programs.

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.13 Data Sorting and Merging (Contd.)

SORT III
The SORT III will be available for sorting, however, specifications are not currently available.

SODA MERGE
Reference: . . . . . UNIVAC Publication UT 2504.
Record size: . . . . . variable by full word; 511 words maximum without own coding.
Block size: . . . . . variable by full word; determined by accessible storage.
Key size: . . . . . key may contain as many words as the item.
File size: . . . . . one reel.
Number of tapes: . . . 3 to 6 units.
Data available: . . . . not currently available.
Description
The SODA merge is a merge generator that produces a merge routine which becomes an integral part of a run. The cascade method of merging is used, and the user can control the amount of core storage and the number of tape units made available to the routine. The merge operates under control of CHIEF, the UNIVAC III Executive routine, making it capable of concurrent operation with other programs.

20 WORD SORT ROUTINE
Reference: . . . . . UNIVAC Publication UT 2506.
Record size: . . . . . 20 words.
Block size: . . . . . 20 words.
Key size: . . . . . 1 to 10 words.
File size: . . . . . 1 reel of tape.
Number of tapes: . . . 4 tape units required.
Date available: . . . . currently available.
Description
The 20-Word Sort Routine will accept 20-word items and sort them into ascending sequence on a key occupying the first 10 words of each item. The key size can be manipulated from 1 to 10 words by physically altering a part of the routine. The initial input and final output must be handled by own coding.

This routine will operate under control of CHIEF, the UNIVAC III Executive Routine, making it capable of concurrent operation with other programs.

.14 Report Writing: . . . . none.

.15 Data Transcription: . . none.

.16 File Maintenance: . . . none.

.17 Other

SUPPORT III
Reference: . . . . . UNIVAC Publication U 3519.
Date available: . . . . currently available.
Description
SUPPORT III is a library consisting of the following routines and sub-routines for UNIVAC III:
On-Line Binary Card Loader routine for loading binary cards from the on-line reader into the locations, specified on each card.

Composite Card Loader routine for loading absolute instruction or data in octal, decimal, and alphameric formats, using the on-line 80-column reader.

Card Reader Routine 1.0003 is a routine used for maintaining a flow of 700 cards per minute through the card reader in either translated or untranslated format.

Boot is a routine for loading specified routines from the system tape or from binary punched cards.

WST (Write System Tape) is a routine that reads binary cards and control cards through the card reader and writes corresponding records on the system tape.

On-Line Memory Dump is a routine for providing a memory dump on the printer. This routine can be activated either through a programmed calling sequence or through typewriter input.

Editing Routines provide for editing input or output information on a character-by-character basis. These routines have the ability to delete or insert blanks and to accept octal, decimal, or alphameric information.

Move Procedure provides a routine for moving N words from one area of core storage to another.

Floating Dollar Sign and Edit Routine generates a routine for editing an 11-character field, floating a dollar sign, and inserting a decimal point and commas where required.

.2 PROBLEM ORIENTED LANGUAGES: . . . . none.

PROCESS ORIENTED LANGUAGE: COBOL-61

§ 161.

.1 GENERAL

.11 Identity: . . . . . UNIVAC III COBOL.

.12 Origin: . . . . . Computer Sciences Corporation.

.13 Reference: . . . . . UNIVAC III COBOL Programmer's Guide, Publication U-3389.

.14 Description

UNIVAC III COBOL is a version of COBOL-61, the most widely implemented pseudo-English common language for business applications. It represents a nearly complete implementation of Required COBOL-61 (though there are a few omissions), along with 15 COBOL electives and several useful extensions. The deficiencies of UNIVAC III COBOL with respect to Required COBOL-61, the extensions, and the facilities of Elective COBOL-61 that have and have not been implemented are tabulated at the end of this description. No part of UNIVAC III COBOL has been implemented in a manner contrary to the COBOL definition.

Useful extensions to the COBOL-61 language include a SORT facility, a MONITOR verb that facilitates program testing, the ability to sequence files in either ascending or descending order, and a facility that permits interchange of data between independently prepared subprograms. See Paragraph .143 for more details on these extensions.

The most significant omission from the list of electives implemented for the UNIVAC III is the COMPUTE verb. COMPUTE permits arithmetic operations to be expressed in a concise formula notation similar to that of FORTRAN; e.g.:

```
COMPUTE X = (A - B)/C
```

Without the COMPUTE verb, only one type of arithmetic operation can be performed in each COBOL statement, so the above formula must be expressed as:

```
SUBTRACT B FROM A GIVING T
DIVIDE C INTO T GIVING X
```

The decision not to implement this useful verb is hard to understand in the case of a system with the speed and power of the UNIVAC III.

Tape reading and writing is partly under the programmer's control in that he can specify the PRESELECTION method of reading if he wishes, and can determine which files shall have their input-output

.14 Description (Contd.)

areas pooled together. PRESELECTION only saves storage space. (This feature has not been implemented as yet.) The various files have their keys in the same relative positions in the records.

Input-output control also provides for a rerun feature based on the number of records in a specified file; i.e., RERUN ON ERROR-LISTING EVERY 10,000 RECORDS OF EDIT-SHIPMENTS.

File and Record Descriptions and Procedure Division entries can be copied into the user's programs from the UNIVAC III COBOL Library, but Environment Division entries cannot. Furthermore, the non-standard COPY verb allows only single-paragraph procedures to be inserted without alteration, whereas the more flexible INCLUDE verb of Elective COBOL-61 (not implemented for the UNIVAC III) allows library procedures consisting of sections, independent paragraphs, or paragraphs within sections to be inserted, with replacement of any number of names in the procedure by other names specified by the programmer. The elective verb ENTER, as implemented for the UNIVAC III, makes it possible to enter either an independently compiled COBOL-coded subprogram or a closed subroutine in relocatable machine language form. Parameters can be listed by the main program for use by the subsidiary program, thus partly covering the same ground that the INCLUDE verb is designed to cover. A non-standard verb, RETURN, is used to denote the end of such subprogram linkages.

Segmentation is handled as in Elective COBOL-61, except that the SEGMENT LIMIT feature has not been implemented. A particular segment must either be part of the main program or an overlay. It cannot be specified to be stored "if there is space available."

The following priorities are available:

- Sections with assigned priorities of 1 through 49 will be present in Core Memory at all times.
- Sections with assigned priorities of 50 through 89 will be grouped into segments by priority number. One segment at a time will be loaded (in the order referenced) into a single Core Memory area whose size is equal to that of the largest segment.
- Sections with assigned priorities of 90 through 99 are treated similarly, but a diagnostic print-out is produced if they are called more than once.

Data items upon which arithmetic is to be performed can be represented internally in decimal form with either 6 or 4 bits per digit by specifying USAGE IS DISPLAY or COMPUTATIONAL, respectively. Operands can be up to 18 decimal digits. Arithmetic

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.14 Description (Contd.)

can be performed upon mixed DISPLAY and COMPUTATIONAL items; radix conversion and point alignment will be automatically performed when necessary.

The UNIVAC III COBOL Compiler will operate under control of the BOSS III operating system. Minimum configuration requirements are 7 Uniservo IIIA Magnetic Tape Units, a 16,384-word core store, and 9 index registers.

Compilation is divided into six logical phases. Documentation will consist of a source program listing, diagnostic messages, and an object program listing containing symbolic instructions, locations, and machine words, with interspersed references to the source program listing. Four different types of error diagnostics are included within the translator; they are interpreted as follows:

- Precautionary diagnostic - print warning messages and continue compilation.
- Correctible error - make a reasonable attempt at correction, print explanatory message, and continue compilation.
- Uncorrectible error - when a reasonable guess of the programmer's intent cannot be made, print message, reject the statement or clause, and continue.
- Destructive errors - when errors have multiplied to the point where it is probable that no more useful diagnostic information can be produced, terminate the compilation at the end of the current phase.

There are no specific limitations on the number of data names, procedure names, or other source program entities. When the COBOL segmentation facility is used, there are no practical limits on object program size. No information on compilation speed is yet available.

.141 Availability

Language: . . . . . October, 1962.
Translator: . . . . . no release date has been designated.

.142 Deficiencies with respect to Required COBOL-61

Environment Division

- SOURCE-COMPUTER, OBJECT-COMPUTER, and SPECIAL-NAMES paragraphs cannot be copied from the Library.

.142 Deficiencies with respect to Required COBOL-61 (Contd.)

Data Division

- The integer-4 TO option of the RECORD CONTAINS clause is not permitted; there is no provision for efficient handling of variable length records; i.e., the compiler will consider all records to be the size of the largest record within a given file.
- The VALUE clause of the File Description entry can apply only to "IDENTIFICATION" or "ID," a specific item that appears in the standard label record.

Procedure Division

- The option of the PERFORM verb that permits loop control based upon a varying subscript-name has not been implemented.

.143 Extensions to COBOL-61

- A SORT facility is provided. It consists of subroutines that arrange related records in either ascending or descending sequence. Input and output procedures must be supplied by the COBOL programmer. While functions of the UNIVAC III SORT facilities are similar to those of the SORT verb as defined in COBOL-61 Extended, the format of the required source coding is entirely different.
- The operational symbol H can be used in a PICTURE clause to specify that the field is to be represented in four-bit decimal form; the effect is the same as that of the clause USAGE IS COMPUTATIONAL.
- Files can be sequenced in either ASCENDING or DESCENDING order.
- Procedures can be copied from the COBOL library into a program.
- Provision is made for intercommunication between separately prepared parts of a program by use of either a COMMON storage section and/or a parameter list provided with the ENTER verb.
- An augmented error recovery system is included. This includes procedures which are programmer-stipulated for errors other than tape read/write errors. These procedures are entered after the standard executive routine error control function has been completed. They are executed by a parameter-controlled section of the standard executive routine.

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.144 COBOL-61 Electives Implemented (see 4:161.3)

Key No.	Elective	Comment
	Characters and Words	
3	Semicolon	; , always ignored.
4	Long literals	up to 128 characters.
	File Description	
11	SEQUENCED ON	allows a list of keys to be specified for ASCENDING or DESCENDING sequencing.
	Verbs	
24	ENTER	permits entry to independently compiled COBOL subprograms.
26	USE	allows additional handling of error conditions.
	Verb Options	
27	LOCK	locks rewound tapes.
30	ADVANCING	permits paper advance of the specified number of lines.
33	Operand size	up to 18 digits.
	Environment Division	
41	OBJECT-COMPUTER	includes all clauses except SEGMENT-LIMIT and ASSIGN OBJECT-PROGRAM.
46	I-O-CONTROL	only the APPLY and RERUN clauses may be written.
	Identification Division	
47	DATE-COMPILED	current date will be inserted automatically.
	Special Features	
48	Library	procedures in source language can be called from the Library (but implementation is non-standard).
49	Segmentation	object programs can be segmented.

§ 161.

.145 COBOL-61 Electives NOT Implemented (see 4:161.3)

Key No.	Elective	Comment
	Characters and Words	
5	Figurative constants	HIGH-BOUND(S); LOW-BOUND(S).
6	Figurative constants	HIGH-VALUE(S); LOW-VALUE(S).
7	Computer-name	no alternative computer-names.
	File Description	
8	BLOCK CONTAINS	no range can be specified.
9	FILE CONTAINS	approximate file size cannot be shown.
10	Label formats	labels must be standard or omitted.
12	HASHED	hash totals cannot be created.
	Record Description	
13	Table-length	items cannot be specified in binary.
16	RANGE IS	value range of items cannot be shown.
17	RENAMES	alternative groupings of elementary items cannot be specified.
18	SIGN IS	no separate signs allewed.
19	SIZE clause option	variable item lengths cannot be specified.
20	Conditional range	a conditional value cannot be specified as a range.
21	Label handling	only standard labels (or none) may be used without specialized programming.
	Verbs	
22	COMPUTE	algebraic formulas may not be used.
23	DEFINE	new verbs cannot be defined.
25	INCLUDE	library subroutines cannot be called in the standard COBOL manner.
	Verb Options	
28	MOVE CORRESPONDING	each item in a record must be individually moved.
29	OPEN REVERSED	tapes cannot be read backward.
32	Formulas	algebraic formulas may not be used.
34	Relationship	IS UNEQUAL TO, EQUALS, and EXCEEDS are not provided; similar forms are available.
35	Tests	IF { } IS NOT ZERO form is not provided.
36	Conditionals	no implied objects with implied subjects.
37	Compound conditionals	ANDs and ORs cannot be intermixed.
38	Complex conditionals	not permitted.
39	Conditional statements	only ON SIZE ERROR or AT END conditions may follow an imperative statement.
	Environment Division	
40	SOURCE-COMPUTER	only computer-name can be specified.
42	SPECIAL-NAMES	ACCEPT, WRITE, and DISPLAY verbs use standard hardware.
43	FILE-CONTROL	cannot be taken from library.
44	PRIORITY IS	no file priorities can be assigned for multiprogramming.
45	I/O CONTROL	cannot be taken from library.

PROCESS ORIENTED LANGUAGE: FORTRAN IV

§ 162.

.1 GENERAL

.11 Identity: . . . . . UNIVAC III FORTRAN.

.12 Origin: . . . . . UNIVAC.

.13 Reference: . . . . . UNIVAC Publications U-3517, U-3549.

.14 Description

No formal standard for FORTRAN IV exists. This report uses as a basis for its comparison the advance specifications for IBM 7090/7094 FORTRAN IV as contained in IBM Publication J28-6197-0.

The UNIVAC III FORTRAN language is largely compatible with the FORTRAN IV language as implemented for the IBM 7090/7094. A reasonable degree of compatibility with the IBM 709/7090 FORTRAN II language is also maintained by accepting and correctly interpreting the following FORTRAN II statements:

IF ACCUMULATOR OVERFLOW n_1, n_2
IF QUOTIENT OVERFLOW n_1, n_2
IF DIVIDE CHECK n_1, n_2
IF (SENSE LIGHT i) n_1, n_2
IF (SENSE SWITCH i) n_1, n_2
PRINT Format, List
PUNCH Format, List
READ i, List
READ INPUT TAPE i, Format, List
READ TAPE i, List
SENSE LIGHT i
WRITE OUTPUT TAPE i, Format, List
WRITE TAPE i, List
CALL EXIT

The FREQUENCY statement of FORTRAN II will be ignored if it appears in a program. Symbolic, double precision, and complex statements will not be accepted. It is not clear how the incompatibilities between FORTRAN II and FORTRAN IV in the handling of Boolean (LOGICAL) operations and in COMMON-EQUIVALENCE interactions will be reconciled.

Restrictions and extensions of the UNIVAC III FORTRAN language relative to IBM 7090/7094 FORTRAN IV are summarized below.

Restrictions:

(1) DOUBLE precision and COMPLEX variables are not permitted.

(2) A variable name may not appear in an EXTERNAL type statement.

(3) Octal digits may not be defined in a DATA statement.

.14 Description (Contd.)

Restrictions (Contd.)

(4) The magnitude of an integer data value may not exceed 10^6, versus 2^{35} (or slightly over 10^{10}) in 7090/7094 FORTRAN IV.

Extensions:

(1) Seven additional library functions are provided (see Paragraph .411).

(2) The magnitude of a floating point data value can range from 10^{-51} to 10^{+49}, versus 10^{-38} to 10^{+38} in 7090/7094 FORTRAN IV.

.15 Publication Date: . . . . June, 1962.

.2 PROGRAM STRUCTURE

.21 Divisions: . . . . . one division, composed of the following types of statements.

Procedure statements: algebraic formulae.
comparisons and jumps.
input and output.

Data statements: . . . . FORMAT: describes the layout, size, scaling, and code of input-output data.
EQUIVALENCE: causes two variables to have a common location or specifies synonyms.
COMMON: causes data storage areas to be shared by more than one subprogram.
DIMENSION: specifies the maximum number of elements in each dimension of an array or set of arrays.
TYPE: specifies mode of a list of variables; INTEGER, REAL, LOGICAL.
DATA: assigns constant values to variables at load time.
EXTERNAL: declares the following identifiers to be function names.

.22 Procedure Entities

Program: . . . . . composed of statements, subroutines, and functions.
Subroutine: . . . . . composed of statements.
Function: . . . . . composed of statements.
Statement: . . . . . composed of characters; blanks are ignored except when part of alphameric literals.

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.23 Data Entities

Array:	a group of variables of any one of the following classes, referenced by subscript notation.
Item:	integer variable or constant. floating point (REAL) variable or constant. Boolean (LOGICAL) variable or constant. Hollerith item. alphameric item.
Hollerith item:	alphameric item that can only be used for output; it is not named.
Alphameric:	alphameric item that can be used for output or as a format statement; it is named.

.24 Names

.241	Simple name formation	
	Alphabet:	A to Z, 0 to 9.
	Size:	1 to 6 char.
	Avoid key words:	yes.
	Formation rule:	first char must be a letter.
.242	Designators	
	Procedures	
	Statement label:	unsigned integer.
	Function label:	governed by the rules of the resulting variables.
	Subroutine label:	no designator.
	Data (if not specified in a TYPE statement)	
	Integer variable:	initial I, J, K, L, M, N.
	Floating point variable:	any other initial letter.
	Equipment	
	Card:	implied by verbs READ, PUNCH; or by reference to a logical input-output table.
	Magnetic tape:	use key word TAPE; or READ, WRITE; or by reference to a logical input-output table.
	Printer:	implied by verb PRINT; or by reference to a logical input-output table.
	Comments:	C in col. 1 of statement.
	Translator control:	key words EQUIVALENCE, COMMON, TYPE.

.25 Structure of Data Names

.251	Qualified names:	none.
.252	Subscripts	
	Number per item:	0 to 3.
	Applicable to:	all variables.
	Class may be	
	Special index variable:	no.
	Any variable:	only integer variables.
	Literal:	yes; except Hollerith.
	Expression:	at most C * N ± C', where C and C' are literals and N is an integer variable.
.252	Subscripts (Contd.)	
	Form may be	
	Integer only:	yes.
	Signed:	no.
	Truncated fraction:	yes.
	Rounded fraction:	no.
.253	Synonyms	
	Preset:	EQUIVALENCE statement causes sharing of storage locations.
	Dynamically set:	no.
.26	Number of Names:	information not currently available.

.27 Region of Meaning of Names

In the straightforward use of FORTRAN, each name is established in a subprogram and is local to that particular subprogram. A name can be made to reference the same storage location in 2 or more subprograms by specifying the name in the corresponding position of a COMMON statement in each subprogram.

.3 DATA DESCRIPTION FACILITIES

.31 Methods of Direct Data Description

.311	Concise item picture:	FORMAT statement only.
.312	List by kind:	yes; TYPE declarations.
.313	Qualify by adjective:	no.
.314	Qualify by phrase:	no.
.315	Qualify by code:	first letter of name if not listed by TYPE.
.316	Hierarchy by list:	no.
.317	Level by indenting:	no.
.318	Level by coding:	no.
.319	Others	
	Array size:	DIMENSION ARRAY (4,7).
	Four-digit integer:	FORMAT (I4).
	Five four-digit integers:	FORMAT (5I4).
	Two floating point items:	FORMAT (F8.3, E10.4) for +999.999 and +.9999E+99.

.32	Files and Reels:	own coding.
.33	Records and Blocks	
.331	Variable record size:	dynamic.
.332	Variable block size:	?
.333	Record size range:	1 to N blocks.
.334	Block size	
	READ TAPE, WRITE TAPE:	? words.
	READ INPUT TAPE, WRITE OUTPUT TAPE:	? characters (BCD format).
	READ, PUNCH:	80 or 90 columns.
	PRINT:	128 characters.
.335	Choice of record size:	READ, WRITE statement.
.336	Choice of block size:	?
.337	Sequence control:	own coding.
.338	In-out error control:	automatic.
.339	Blocking control:	?

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.34 Data Items

.341	Designation of class:	by name or TYPE declaration.
.342	Possible classes	
	Integer:	yes.
	Fixed point:	no.
	Floating point:	yes.
	Logical:	yes.
	Double precision:	no.
	Complex:	no.
	Alphameric:	yes.
.343	Choice of external radix:	FORMAT statement.
.344	Possible external radices	
	Decimal:	yes.
	Octal:	yes.
.345	Internal justification:	alpha automatic left justified. integers automatic right justified.
.346	Choice of external code:	FORMAT statement and READ, WRITE statement.
.347	Possible external codes	
	Decimal:	yes.
	Octal:	yes.
	Hollerith:	yes.
	Alphameric:	yes.
.348	Internal item size	
	Variable size:	fixed.
	Designation:	none.
	Range	
	Fixed point numeric:	fixed, 1 word.
	Floating point numeric:	fixed, 2 words.
	Logical:	fixed, 1 word.
	Alphameric:	fixed, 1 word of up to 4 characters.
.349	Sign provision:	optional.

.35 Data Values

.351	Constants	
	Possible sizes	
	Integer:	$\pm 2^{20}$.
	Fixed point:	none.
	Floating point:	10^{-51} to 10^{49}.
	Alphameric:	? characters.
	Logical:	.TRUE. or .FALSE. only.
	Subscriptible:	yes.
	Sign provision:	optional.
.352	Literals:	same as constants.
.353	Figuratives:	own coding; e.g., TEN = 10.0.
.354	Conditional variables:	computed GO TO.

.36 Special Description Facilities

.361	Duplicate format:	by multiple references to a single FORMAT statement.
.362	Re-definition:	COMMON statement. EQUIVALENCE statement.
.363	Table description	
	Subscription:	mandatory in DIMENSION statement.
	Multi-subscripts:	1 to 3.
	Level of item:	variables.
.364	Other subscriptible entities:	input-output units.

.4 OPERATION REPERTOIRE

.41 Formulae

.411 Operator List

Arithmetic

+	addition, also unary.
-	subtraction, also unary.
*	multiplication.
/	division.
**	exponentiation.
=	is set equal to.

Functions

ABS ( )	absolute value; floating argument and function.
IABS ( )	absolute value; fixed argument and function.
AINT ( )	truncate; reduce to integer value; floating argument and function.
INT ( )	truncate; reduce to integer value; floating argument and fixed function.
AMOD (A,B)	remainder A ÷ B; floating argument and function.
MOD (A,B)	remainder A ÷ B; fixed argument and function.
AMAX0 (A,...)	maximum value; fixed argument and floating function.
AMAX1 (A,...)	maximum value; floating argument and function.
AMX0 (A,...)	maximum value; fixed argument and function.
MAX1 (A,...)	maximum value; floating argument and fixed function.
AMIN0 (A,...)	minimum value; fixed argument and floating function.
AMIN1 (A,...)	minimum value; floating argument and function.
MIN0 (A,...)	minimum value; fixed argument and function.
MIN1 (A,...)	minimum value; floating argument and fixed function.
FLOAT ( )	float an integer; fixed argument and floating function.
IFIX ( )	fix a floating point variable; floating argument and fixed function.
SIGN (A,B)	transfer sign of A to B; floating argument and function.
ISIGN (A,B)	transfer sign of A to B; fixed argument and function.
DIM (A,B)	diminish A by A or B, whichever is smaller; floating argument and function.
IDIM (A,B)	diminish A by A or B, whichever is smaller; fixed argument and function.
SIN ( )	sine.
COS ( )	cosine.
TAN ( ) ‡	tangent.
ASIN ( ) ‡	arcsine.
ACOS ( ) ‡	arccosine.
ATAN ( )	arctangent.
SINH ( ) ‡	hyperbolic sine.
COSH ( ) ‡	hyperbolic cosine.
TANH ( )	hyperbolic tangent.

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.411 Operator List (Contd.)

Functions (Contd.)

SQRT ( ).	square root.
EXPN ( ).	exponential (e^x).
EXP10 ( ) ‡	exponential (10^x).
ALOG ( )	natural log.
ALOG10 ( ) ‡ . . .	common log.

‡ denotes functions which are extensions of the language relative to IBM 7090/7094 FORTRAN IV.

Logical

AND:	.AND..
Inclusive OR:	.OR..
Exclusive OR: . . .	none.
NOT:	.NOT..

Relational

Equal:.	.EQ..
Not Equal:	.NE..
Greater than:	.GT..
Less than:	.LT..
Greater than or equal:	.GE..
Less than or equal:	.LE..

.412 Operands allowed

Classes:	INTEGER, REAL, LOGICAL.
Mixed scaling:	yes, floating point.
Mixed classes:	only in exponentiation and functions.
Mixed radices:	no.
Literals:	yes.

.413 Statement structure

Parentheses

a - b - c means: . .	(a-b) - c.
a + b x c means: . .	a + (b x c).
a ÷ b ÷ c means: . .	(a ÷ b) ÷ c.
a^{b^c} means:	illegal; parentheses must be used.
Multi-results:	no.

.414 Rounding of results: . . truncation of integers at each step in expression.

.415 Special cases

	Fixed	Floating
x = -x:	K = -K	X = -X.
x = x + 1:	K = K + 1	X = X + 1.
x = 4.7y:	K = 47*L/10	X = 4.7 * Y.
$x = 5x10^7 + y^2$:	50000000+L**2	X = 5.E7+Y**2.
x = |y|:	K = IABS (L)	X = ABS (Y).
x = integer part of (y):	K = AINT (L)	X = INT (Y)

.416 Typical examples: . . . X = (-B+SQRT(B*B-4.0*A*C))/(2.0*A).

.42 Operations on Arrays:. . . . . by own FORTRAN coding only.

.43 Other Computation: . . subprograms in symbolic or COBOL language may reference or be referenced by FORTRAN subprograms.

.44 Data Movement and Format

.441 Data copy example: . . Y = X.
.442 Levels possible: . . . . items.
.443 Multiple results:. . . . none.
.444 Missing operands: . . . not possible.

.445 Size of operands

Exact match:	implied, except for alpha or input-output.
Alignment rule	
Numbers:	right justified or normalized.
Alpha:.	left justified.
Filler rule	
Numbers:	zeros.
Alpha:.	blanks.
Truncating rule	
Numbers:	truncate at left.
Alpha:.	truncate at right.
Variable size destination:	no.

.446 Editing possible

Change class:	yes.
Change radix:	yes.
Insert editing symbols	
Actual point:	automatic.
Suppress zeroes: . .	automatic.
Insert:	automatic point.
Float:	minus sign only.

.447 Special moves:. . . . . none.
.449 Character manipulation: none.

.45 File Manipulation

Open:.	own coding.
Close:	own coding.
Advance to next record:	READ, WRITE, PUNCH, PRINT.
Step back a record: . .	BACKSPACE.
Set restart point: . . .	none.
Restart:	none.
Start new reel:.	own coding.
Start new block:	implied in each input-output statement.
Search on key:	none.
Rewind:	REWIND.
Unload:.	none.

.46 Operating Communication

.461 Log of progress:. . . .	PRINT uses on-line printer.
.462 Messages to operator:.	same as log (error messages are automatically typed on console typewriter).
.463 Offer options:	PAUSE and type decimal integer. PRINT message and PAUSE.
.464 Accept option:	none.

.47 Object Program Errors

Error	Discovery	Special Actions
Overflow:	IF clauses	own coding.
In-out:	automatic	by executive routine.
Invalid data:	format checks	typed messages.

.5 PROCEDURE SEQUENCE CONTROL

.51 Jumps

.511 Destinations allowed: . statement.
.512 Unconditional jump: . . GO TO N.

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.513 Switch: . . . . . GO TO M, OR GO TO M, (35, 47, 18).

.514 Setting a switch: . . . . ASSIGN 35 TO M.
.515 Switch on data: . . . . . GO TO (35, 47, 18), I.

.52 Conditional Procedures

.521 Designators
Condition: . . . . . IF.
Procedure: . . . . . implied.
.522 Simple conditions: . . . expression or variable versus zero.
.523 Conditional relations
Equal: . . . . . .EQ.
Not equal: . . . . . .NE..
Greater than: . . . . . .GT..
Less than: . . . . . .LT..
Greater than or equal: .GE..
Less than or equal: . .LE..
.524 Variable conditions: . . true or false for logical expressions.
less than, equal to, or greater than zero for arithmetic expressions.
.525 Compound Conditionals
IF x AND y: . . . . . yes.
IF x OR y: . . . . . yes.
IF x DO a AND y DO b: no.
IF x DO a OR y DO b: no.
.526 Alternative designator: none.
.527 Condition on alternative: no.
.528 Typical examples: . . . IF (X**2.0-3.0) 29, 37, 18: go to 29, 37 or 18 if X^2-3 is respectively less than, equal to, or greater than zero.
IF (((A*B).GT.C).AND.(D.EQ.E)) GO TO 7: go to 7 if the expression is true and to the next statement if false.

.53 Subroutines

.531 Designation
Single statement: . . . not possible.
Set of statements
First: . . . . . SUBROUTINE.
Last: . . . . . END.
.532 Possible subroutines: . any number of statements.
.533 Use in-line in program: no.
.534 Mechanism
Cue with parameters: CALL XXX (X, Y, Z).
Number of parameters: . . . . ?
Cue without parameters: . . . . CALL XXX.
Formal return: . . . . RETURN at least once.
Alternative return: . . more RETURN statements.
.535 Names
Parameter call by value: . . . . . yes.
Parameter call by name: . . . . . no.
Non-local names: . . use COMMON.
Local names: . . . . . all.
Preserved own variables: . . . . . all.
.536 Nesting limit: . . . . . ?
.537 Automatic recursion allowed: . . . . . no.

.54 Function Definition by Procedure

.541 Designation
Single statement: . . . same as set.
Set of statements
First: . . . . . FUNCTION.
Last: . . . . . END.
.542 Level of procedure: . . any number of statements.
.543 Mechanism
Cue: . . . . . by name in expression.
Formal return: . . . . RETURN.
.544 Names
Parameter call by value: . . . . . yes.
Parameter call by name: . . . . . no.
Non-local names: . . use COMMON.
Local names: . . . . . all.
Preserved own variables: . . . . . all.

.55 Operand Definition by Procedure: . . . . . none.

.56 Loop Control

.561 Designation of loop
Single procedure: . . . none.
First and last procedures: . . . . . current place to numbered end; e.g., DO 173 I = 1, N, 2.
.562 Control by count: . . . indirect.
.563 Control by step
Parameter
Special index: . . . . no.
Any variable: . . . . integer only.
Step: . . . . . positive integer.
Criteria: . . . . . greater than.
Multiple parameters: require nested loops.
.564 Control by condition: . no.
.565 Control by list: . . . . no.
.566 Nesting limit: . . . . . ?
.567 Jump out allowed: . . . yes.
.568 Control variable exit status: . . . . . available.

.6 EXTENSION OF THE LANGUAGE: . . . . . new functions can be added to the library.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . ?

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.

.73 Storage Form: . . . . . magnetic tape; variable length blocks in relocatable binary format.

.74 Varieties of Contents: . subroutines.
functions.
service routines.

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.75 Mechanism

.751 Insertion of new item: . separate run.
.752 Language of new item:. FORTRAN.
.753 Method of call:. . . . . named in procedures.

.76 Types of Routines

.761 Open routines exist: . . ?
.762 Closed routines exist: . yes.
.763 Open-closed is variable: no.

.8 TRANSLATOR CONTROL

.81 Transfer to Another Language: . . . . . via subprograms in symbolic or COBOL language.

.82 Optimizing Information Statements

.821 Process usage statements: . . . . none.
.822 Data usage statements: . . . . COMMON, EQUIVALENCE.

.83 Translator Environment: . . . no.

.84 Target Computer Environment: . . . no.

.85 Program Documentation Control: . . . . . no.

.9 TARGET COMPUTER ALLOCATION CONTROL

.91 Choice of Storage Level: none.

.92 Address Allocation: . . none.

.93 Arrangement of Items in Words in Unpacked Form: . . . . . standard; no control is provided.

.94 Assignment of Input-Output Devices: . . . specified in input-output table statements.

.95 Input-Output Areas: . . none.

MACHINE ORIENTED LANGUAGE: UTMOST

§ 171.

.1 GENERAL

.11 Identity: . . . . . UTMOST (UNIVAC III Machine Oriented Symbolic Translator)

.12 Origin

UTMOST: . . . . . UNIVAC.

.13 Reference

UTMOST: . . . . . UNIVAC Publication U-3520.

.14 Description

UTMOST, the basic machine oriented language for the UNIVAC III, is a straightforward symbolic assembly system that permits access to library routines and connection with executive routines for full utilization of the system's capabilities. Coding sheets are designed so that no strict adherence to column definition for label, operation, operand, and comments is necessary; however, very rigid specifications for format of these fields must be followed. Use and contents of literals may be specified in a variety of ways.

UTMOST has 16 "assembly directives". Fifteen are used as pseudo operation codes for generation of data, reserving areas, forming subroutines, etc. One of the directives, DO, is used as a macro instruction. The PROC and DO assembly directives are especially useful, since they effectively allow the coder to set up a library of subroutines using the PROC directive and then call the subroutines into any part of the program using the DO directive. These are 13 operand "operators" which may be used to perform arithmetic or logical operations while generating the address or data desired.

Communication with other independently written routines is facilitated by referencing a label that does not appear in the program or defining a label that is to be considered externally available to other programs or segments. The actual linkage between external references and definitions are consummated when the programs or segments are loaded at object time.

The final output of UTMOST is in the form of relocatable binary program either on card or tape media and a listing of the original symbolic coding together with an octal representation of the word generated.

.15 Publication Date: . . . . ?

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . see Section 774:132.

.22 Legend

Label: . . . . . identifies either a symbolic line of coding or a word of data.

Operation: . . . . . can contain a mnemonic machine operation code, an expression representing a machine function or assembler directive, a label associated with a directive, or a data gathering code.

Operand: . . . . . expression defining the information required by the operation field of the line.

.23 Corrections: . . . . . the control directive COR permits insertions, deletions, and alterations to be made before reassembling a program.

The COR option is written in the operation field followed by n, a decimal sequence line number, in the operand field. Line n will be replaced and followed by all lines following the COR line until another COR line is encountered. COR 9999 ends the operation. The INS option is written in the operation field followed by n, a decimal sequence line number, in the operand field. The lines following the INS line will be inserted following n. INS and COR are part of the Updating Control (UPCO).

.24 Special Conventions

.241 Compound addresses: . 13 forms available (see Paragraph .83).

.242 Multi-addresses: . . . none.

.243 Literals

Alphabetics: . . . . . enclose alphameric characters within apostrophes (').

Octal: . . . . . precede the desired value (in base 8) with a zero.

Decimal: . . . . . non-zero digit followed by decimal (0-9) digits.

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.243 Literals (Contd.)
BCD (binary-coded decimal, excess-three): . . . . . precede the value with a colon (:).
Floating point numbers: . . . . . a number expressed decimally and preceded by a colon (:) will produce excess 50 floating point format with 10 digit mantissa and a 2-digit characteristic.

.244 Special coded addresses: . . . . . $ refers to this address.
* refers to indirect address or external definition of address.
() refers to literal address.

.3 LABELS

.31 General: . . . . . A label must begin in column 1 of the coding sheet by definition. Exception: a label of the operand of a DO line must immediately follow the separating comma of the DO line by definition. The asterisk may be appended as a suffix to a label to designate that it is available to the region in which it is a subset. The labels of Procedures, NAME lines and DO lines have special denotations.

.311 Maximum number of labels: . . . . . no practical limit.

.312 Common label formation rule:. . . . 1 to 8 alphabetic or numeric characters; First character must be alphabetic; there must be no blanks nor special characters.

.313 Reserved labels: . . . none, since any label may be regional.

.314 Other restrictions: . . procedure or name labels should not conflict with mnemonics or directives.

.315 Designators: . . . . . permitted via EQU directive* is an indirect address or field select indicator. ( ) is a literal indicator where grouping is not intended.

.316 Synonyms permitted: via EQU directive and via Procedure directive.

.32 Universal Labels

.321 Labels for procedures
Existence: . . . . . mandatory if referenced.
Formation rule
First character: . . letter.
Others: . . . . . letters or numerals; no blanks or special characters except *
Number of characters: . . . . 1 to 8.

.322 Labels for library routines: . . . . . same as procedures.

.323 Labels for constants: . same as procedures.

.324 Labels for files: . . . . same as procedures.

.325 Labels for records: . . same as procedures.

.326 Labels for variables: . same as procedures.

.33 Local Labels

.331 Region:. . . . . local to PROC routine in which they appear.

.332 Labels for procedures
Existence: . . . . . mandatory if referenced.
Region: . . . . . local, provided they are within another procedure.
Formation rule
First character: . . alphabetic.
Others: . . . . . alphabetic or numeric, no blank or special char.
Number of characters: . . . . . 1 to 8.

.333 Labels for library routines: . . . . . none.

.334 Labels for constants: . same as procedures.

.335 Labels for files: . . . . same as procedures.

.336 Labels for records: . . same as procedures.

.337 Labels for variables: . same as procedures.

.4 DATA

.41 Constants

.411 Maximum size constants
Integer
Decimal: . . . . . 12 decimal digits.
Octal: . . . . . 16.
Binary: . . . . . 25.
Fixed numeric:. . . . none.
Floating numeric
Decimal: . . . . . 10-decimal-digit mantissa and 2-decimal-digit characteristic.
Octal: . . . . . none.
Hexadecimal: . . . . none.
Alphabetic: . . . . . alphameric characters.
Alphameric: . . . . . alphameric characters.

.412 Maximum size literals
Integer
Decimal: . . . . . 12 characters.
Octal: . . . . . 16.
Binary: . . . . . 25.
Fixed numeric:. . . . none.
Floating numeric
Decimal: . . . . . 10-digit mantissa and 2-digit characteristic.
Octal: . . . . . none.
Hexadecimal: . . . . none.
Alphabetic: . . . . . 8 characters.
Alphameric: . . . . same as alphabetic.

.42 Working Areas

.421 Data layout
Implied by use:. . . . no.
Specified in program: by reserving area.

.422 Data type: . . . . . implied by use.

.423 Redefinition: . . . . . yes; EQU, RES, SEG pseudo.

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.43 Input-Output Areas

.431 Data layout: . . . . . explicit layout.
.432 Data type: . . . . . not required.
.433 Copy layout: . . . . . PROC directive will define common statement. DO directive will cause the common statement to be copied the specified number of times.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . . practical.
Number: . . . . . 74.
Example: . . . . . DA = decimal add.
.512 Absolute
Existence: . . . . . may be set up as constants or literals and interpreted with form directive.

.52 Macro-Codes: . . . . . none.

.53 Interludes: . . . . . none.

.54 Translator Control

Allocation counter: . . pseudo operation.
Label adjustment: . . . pseudo operation.
Annotation: . . . . . see Paragraph .544.

.542 Allocation counter
Set to absolute: . . . . RES pseudo.
Set to label: . . . . . RES pseudo.
Step forward: . . . . . RES pseudo.
Step backward: . . . . RES pseudo.
Reserve area: . . . . RES pseudo.
.543 Label adjustment
Set labels equal: . . . EQU pseudo.
Set absolute value: . . EQU pseudo.
Clear label table: . . none.
Limit label table: . . to area of Procedure, or within DO loop.
.544 Annotation
Comment phrase: . . any card, separated from operand by a period (.) and a blank.
Title phrase: . . . . . preceded by a period (.) and a blank.
.545 Other
Allocation mode: . . . relocatable.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: . . to be provided in SUPPORT III; see Paragraph 772:151.113.

.62 Special Functions: . . . library access, maintenance, designation control.

.63 Overlay Control: . . . . yes, DECO (Segment, Chain).

.64 Data Editing: . . . . . yes, in SUPPORT III.

.642 Format control: . . . . yes, in SUPPORT III.

.65 Input-Output Control

.651 File labels: . . . . . by use.
.652 Reel labels: . . . . . by use.
.653 Blocking: . . . . . by use.
.654 Error control: . . . . . under control BOSS III Executive System.
.655 Method of call: . . . . . EQU pseudo op.

.66 Sorting

.661 Facilities: . . . . . SODA Sort; see Paragraph 772:151.113.
20-word Sort; see Paragraph 772:151.113.
.662 Method of call: . . . . . Library Reference.

.67 Diagnostics

.671 Dumps: . . . . . SUPPORT III dump on printer.
.672 Tracers: . . . . . none.
.673 Snapshots: . . . . . in form of memory dump at intervals specified by in-line coding.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . SUPPORT III.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.
.723 Private: . . . . . private facilities may be added.

.73 Storage Form: . . . . . card . or tape.

.74 Varieties of Contents: . routines and subroutines.

.75 Mechanism

.751 Insertion of new item: . physically before reference in program.
.752 Language of new items: UTMOST., or binary.
.753 Method of call: . . . . . EQU pseudo op.

.76 Insertion in program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: yes.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Code: . . . . . DO directive.
Description: . . . . . generates designated line(s) of coding.

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.82 Pseudos

Code	Description
EQU:	equate operand value to label field.
RES:	reserve memory locations.
USE:	assign index registers for area addressing.
FORM:	designate arbitrary word format.
FLD:	specify field selection pattern.
END:	designate end of program or procedure.
PROC:	specifies the following in a subroutine.
NAME:	qualify procedural coding.
SET:	set index register to assumed value.
GO:	means to transfer within a PROC.
NACL:	rename mnemonic code.
ICW:	generate a word in suitable format for incrementing and comparing an index register.
TWC:	generate a 2-word constant.
',+,-,*,( ):	generate a word of data these may be compounded.

.83 Operators: used in operand portion of instruction to form compound addresses or data words, also used for decision-making.

Code	Description
+ :	arithmetic sum.
- :	arithmetic difference.
* :	arithmetic product.
/ :	arithmetic quotient.
++:	logical sum (OR).
-- :	logical difference (exclusive OR).
** :	logical product (AND)
// :	covered quotient $(a/\ /b = \frac{a+b-1}{b})$.
= :	equals.
> :	greater than.
*+:	$a*+b = a*10^{b}$.
*-:	$a*-b = a*10^{-b}$.
:	less than.

Note: = , > , < are used to develop truth statements which generate a binary value depending on truth or falseness of statement.

MACHINE ORIENTED LANGUAGE: SALT

§ 172.

.1 GENERAL

.11 Identity: . . . . . SALT.

.12 Origin: . . . . . UNIVAC.

.13 Reference: . . . . . UNIVAC Publication U2558.

.14 Description

SALT is an assembly language for the UNIVAC III System, which, in conjunction with the UNIVAC III SALT executive routine and SALT service library, forms a complete assembly system. Generally a one-to-one correspondence exists between source statements not including macros or subroutines and machine language instructions. Through the use of macro and subroutine statements, the programmer can call and cue open or closed library routines at will, thereby reducing coding time and effort. User-defined macros and subroutines can be inserted into the library.

The SALT executive routine provides complete control and all necessary macro operations to handle all multi-running control functions, input-output functions, checkpoints, and error checking. Information pertaining to hardware and core storage requirements for a program must be included in the source routine in the form of a series of descriptive entries. Hardware facilities can be assigned either by a specific assignment in a descriptive entry in the source routine or by letting the executive routine assign the facilities at object time.

Program documentation is implemented with a side by side listing of source and object program, including error codes.

No compatibility exists between the SALT and UTMOST (see Paragraph 774:171) language. Even the mnemonic codes differ.

.15 Publication Date: . . . . July, 1961.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . refer to Appendix A.

.22 Legend

Item Number: . . . . . sequence number of lines, through which any desired relationship among lines may be imposed.

Tag Field: . . . . . names the location of an instruction or data item. local reference point if one digit numeric tag is used.

.22 Legend (Contd.)

C-class Field: . . . . . used for defining the disposition of the level it is associated with.

Form Field: . . . . . used for defining the content field.

Content Field: . . . . . used for representing either instructions, control words, data words, or comments.

.23 Corrections: . . . . . 1. spare lines of coding sheet and gaps in line number sequence if corrections are to be made to program source card deck.
2. correcting routine on existing library (tape) by use of systems routines, Source Code Service One, if any routine in the library is to be assembled, Source Code Service Two, if no routine is to be assembled.
3. by object code corrections to Master reference File and/or Master instruction tape during Object Code Service routine. It is suggested that minor corrections be made at 3 above, major corrections be made through 2. above and no corrections be made through 1. above.

.24 Special Conventions

.241 Compound addresses: . BASE ± ADJUSTMENT ± ADJUSTMENT where BASE is any label or a reflexive address ($ HERE), which causes SALT to assign an address equal to the address of the line containing the reflexive address, and ADJUSTMENT is: a permanent tag; a decimal number, or the symbol $ SEG i which represents an amount equal to all the lines in the ith segment.

.242 Multi-addresses: . . . in defining parameters of subroutines and macro-instructions only.

.243 Literals: . . . . . any valid representation of data, instructions, and control words appearing as the address portion of an instruction in the format: (f:r) where f is a valid form field entry and r is a representation of the type indicated by f.

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.243 Literals (Contd.)

DCML:	decimal number: maximum of 6 digits plus sign.
DDML:	decimal number: maximum of 12 digits plus sign.
BINY:	binary number: 1 to 24 bits plus sign.
DTOB:	decimal number plus sign in the range of 0 to 16,777,215, which is to be converted to binary.
OTOB:	octal number with sign in the range of 0 to 77,777,777, which is to be translated to binary.
ALPH:	up to four alphameric characters.
INST:	instruction.
INAD:	indirect address control word.
FSEL:	field select control word.
XMOD:	Index Register Modification control word.
SCAT:	Scatter Read or Gather Write control word.
STOP:	stop control word.
DATE:	defines an alphameric symbol which will occupy one computer word. The value specified by this form may be replaced in the program by another value after assembly.
SGAD:	defines program relative address of first line in segment which contains label line referred to by this form.
LOCA:	defines program relative address of label referred to in this form.
AREA:	defines space to accommodate data.
XLOC:	defines termination of program, overlay request or memory dump request.
XFAD:	defines control word used in requesting memory dumps.
XLST:	defines input-output control word.
TCON:	define the length, direction, and location of typewriter message.
LDID:	defines a five-word program load identifier for the executive routine.
IOFS:	defines input-output function specification control word.
XFRE:	releases or assigns hardware facilities to a file.

244 Special coded addresses: Reflexive Address - $HERE causes SALT to assign an address equal to the address of the line containing the reflexive address. Temporary Storage Tag address - $Tn where n is a decimal number in the range of 1 to 1024. SALT allocates storage for temporary use by reserving as many locations as the maximum "n" occurring in any $Tn address. Standard Location address - $LOCn which allows object program to communicate with the executive routine.

.245 Other

Actual core storage addresses: decimal number ranging from 0 to 1,023 for relative addressing of any line in a segment.

.3 LABELS

.31 General

.311 Maximum number of labels	
Procedures:	no limit.
Constants:	same as procedures.
Files:	same as procedures.
Record:	same as procedures.
Items:	same as procedures.
.312 Common label formation rule:	yes, except for local labels; see Paragraph .332.
.313 Reserved labels:	none.
.314 Other restrictions:	Duplicate labels will cause error notation on codedit.
.315 Designators:	none.
.316 Synonyms permitted:	yes; 2 or more labels may refer to the same storage area address form entry.

.32 Universal Labels

.321 Labels for procedures	
Existence:	mandatory if referenced by other procedures.
Formation rule	
First character:	alphabetic.
Others:	alphameric: A through Z and 0 through 9.
Number of characters:	1 to 8.
.322 Labels for library routines:	same as procedures.
.323 Labels for constants:	same as procedures.
.324 Labels for files:	same as procedures.
.325 Labels for records:	same as procedures.
.326 Labels for variables:	same as procedures.

.33 Local Labels

.331 Region:	local to area until same number is used again.
.332 Labels for procedures	
Existence:	mandatory if referenced by another procedure.
Region:	local to area until same number is used again.
Formation rule	
First character:	0 through 9.
Number of characters:	1.

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.333 Labels for library routines: . . . . . same as procedures.
.334 Labels for constants: . same as procedures.
.335 Labels for files: . . . . same as procedures.
.336 Labels for records: . . same as procedures.
.337 Labels for variables: . same as procedures.

.4 DATA

.41 Constants

.411 Maximum size constants

Machine form	External form
Integer	
Decimal:	12 decimal digits.
Octal:	none.
Hexadecimal: . . .	none.
Binary:	24 bit binary number plus sign.
Binary:	decimal number with sign in the range of 0 to 16,777,215.
Binary:	octal number with sign in the range of 0 to 77,777,777.
Fixed numeric	
Decimal:	none.
Octal:	none.
Hexadecimal: . . .	none.
Floating numeric	
Decimal:	none.
Octal:	none.
Hexadecimal: . . .	none.
Alphameric:	4 alphameric characters.

.412 Maximum size literals

Machine code	External code
Integer	
Decimal:	12 decimal digits.
Octal:	none.
Hexadecimal: . . .	none.
Binary:	24-bit binary number plus sign.
Binary:	decimal number with sign in the range of 0 to 16,777,215.
Binary:	octal number with sign in the range of 0 to 77,777,777.
Fixed numeric	
Decimal:	none.
Octal:	none.
Hexadecimal: . . .	none.
Floating numeric	
Decimal:	none.
Octal:	none.
Hexadecimal: . . .	none.
Alphameric:	4 alphameric characters.

.42 Working Areas

.421 Data layout: . . . . . implied by use.
.422 Data type: . . . . . not required.
.423 Redefinition: . . . . . yes; by defining a temporary storage area assigned to a pool

.43 Input-Output Areas

.431 Data layout: . . . . . implied by writing procedures.
.432 Data type: . . . . . not required.
.433 Copy layout: . . . . . implied by writing.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . . optional.
Number: . . . . . 61.
Example: . . . . . Arm - add contents of storage location to arithmetic register r.

.512 Absolute
Existence: . . . . . optional.
Number: . . . . . 50.
Example: . . . . . 20 r m = add contents of storage location m to arithmetic register r.

.52 Macro-Codes

.521 Number available
Input-output: . . . . . 51.
Arithmetic: . . . . . 2.
Math Functions: . . . 24.
Error Control: . . . . none, included in executive routine "CHIEF".

.522 Examples
Simple: . . . . . MCRO DPM01,
Elaborate: . . . . . SUBR - MOVE ZZ, P,
INDX X_1, X_2, X_3, X_4
SLCT STRATOPN,: STRAIGHT LINE coding, open Subroutine
or; SLCT STRATCLS,: STRAIGHT LINE coding, closed Subroutine
or; SLCT ITRATOPN,: Iterative coding, open subroutine
or; LSCT ITRATCLS,: Iterative coding, closed subroutine
where p = n = number of words to be moved. (straight line) or number of words to be moved per iteration (iterative)
X_1 = Index register for coding
X_2 = Starting address of area containing the words to be moved.
X_3 = Starting address of area in which to move words.
X_4 = Number of times to iterate.

.523 New macros: . . . . . can be inserted into program or put on the library tape in a separate run.

.53 Interludes

Statements	Description
SGMT:	defines the interrelationship of segments within a program and the first item in the segment.
LOAD:	defines an unbroken sequence of segments that are to be in core storage at the same time.

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.53 Interludes (Contd.)

Statements	Description
MAPS:	equates a segment line with a particular index register designation.
OVER:	designates unexpected overflow condition routine.
INOP:.	designates invalid operation routine.
STRT:	designates the starting address of a program.
EQUL:	assigns a label to an actual or symbolic address.
EQDX:	assigns a label relative to a data storage area.

.54 Translator Control

.541 Method of control	
Allocation Counter: .	pseudo operations.
Label adjustment: . .	pseudo operation.
Annotation:	see .544.
.542 Allocation counter	
Set to absolute:. . . .	none.
Set to label:	EQUL pseudo.
Step forward:.	SGMT pseudo.
Step backward:	SGMT pseudo.
Reserve area:	AREA pseudo.
.543 Label adjustment	
Set labels equal: . . .	EQUL pseudo.
Set absolute value: . .	none.
Clear label table: . .	none.
.544 Annotation	
Comment phrase: . .	colon (:) followed by comment in the contents field.
Title phrase:	colon (:) followed by title in the contents field or title appearing in contents field of a LABEL card.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic

.611 Facilities:	see macros - 521.
.612 Method of call:.	see macros - 521.

.62 Special Functions

.621 Facilities:	see macros - 521.
.622 Method of call:.	see macros - 521.

.63 Overlay Control

.631 Facilities:	load and execute segment of object language.
.623 Method of call:.	use XLOC Control word.

.64 Data Editing

.641 RADIX conversion	
MCRO C1DTB: . . .	converts a one-word decimal number into a one-word binary number.
MCRO C2DTB: . . .	converts a two-word decimal number into two binary words.
.641 RADIX conversion (Contd.)	
MCRO C3DTB: . . .	converts a three-word decimal number into three binary words.
MCRO C4DTB: . . .	converts a four-word decimal number into four binary words.
MCRO C1BTD: . . .	converts one binary word into one or two decimal words.
MCRO C2BTD: . . .	converts two binary words into three decimal words.
.642 Code Translation: . . .	this is accomplished as a hardware feature or as a translation parameter in the software package. There are no special routines available to translate images which entered memory using the untranslated parameters in the software package.
.643 Format control	
Zero suppression: . .	function of hardware.
Size control:	supplied by user.
Sign control:	function of hardware.
Special characters: .	supplied by user.
.644 Method of call:.	for radix conversions; macro statements, for others; mnemonic or absolute operation codes.
.65 Input-Output Control: .	normally handled by the executive routine with provision for incorporating "own coding" if desired.

.66 Sorting

.661 Facilities:	none - a sort of the type defined in the users guide is not available.
.662 Method of call:.	none.

.67 Diagnostics

.671 Dumps:.	memory print available.
.672 Tracers:	analyzes each instruction of a program to determine that it stops in memory allocated to that program, then puts printable record of the instruction on tape. selective by specifying parameters or by conditional basis.

.7 LIBRARY FACILITIES

.71 Identity:	1. Standard Super Library (SALT source code of all subroutines and macros maintained by UNIVAC). 2. option of user.

.72 Kinds of Libraries

.721 Fixed masters:	yes.
.722 Expandable master: . .	yes.
.723 Private:	yes.
.73 Storage Form:	magnetic tape.

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.74 Varieties of Contents: . Programs, subroutines, and macro's in SALT source code.

.75 Mechanism

.751 Insertion of new item: . restricted to special library runs.
.752 Language of new item:. SALT source.
.753 Method of call:. . . . . pseudo operation.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: yes.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macro

Input-Output

Subroutine using
-SER 3ZZ: . . . . . I/O control systems for tape files using UNISERVO *III tape units.
P1: . . . . . permanent tag naming line to which control is to be transferred when an end-of-file sentinel is encountered.
P2: . . . . . a number, 1 through 15, designating the communication index register for this macro-instruction.
M: . . . . . marker for call statement.
f: . . . . . external alphabetic file designation.

Input Macro set - Type One - Index Register Communication

Code	Description
MCRO M * START f, P1, P2,:	reads and checks the label on the first reel of file "f".
MCRO M * ADV f, P1, P2,:.	advances next input item into current status.
MCRO M * END f, P2,:.	early termination of file.

Output Macro set - Type One - Index Register Communication .

Code	Description
MCRO M * START f, P2,:	writes label on first reel of file "f."
MCRO M * ADV f, P2,:	advances next delivered output area into current status.

.81 Macro (Contd.)

Code	Description
MCRO M * ENDR f, P2,:	terminate current reel of file "f" and write label on next reel of file "f."
MCRO M * END f, P2,:	terminates file "f" including control information and physical disposition of tape.

Area Source Macro set - Type One - Index Register Communication

Code	Description
MCRO M * ADV, P2,:	advances next input item into current status.

Output Macro set - Copy - Arithmetic Register Communication

Code	Description
MCRO M * START f,:	writes label on first reel of file "f".
MCRO M * COPY f,:	copies current item onto output file "f."
MCRO M * COPYV f,:	copies variable size items onto file "f."
MCRO M * ENDR f,:	terminates current reel of file "f" and writes label on the next reel of file "f."
MCRO M * END f,: .	terminates file "f."
MCRO M * HOLD,: .	prevents item in current area from being overlaid by another item.
MCRO M * FREE,: .	releases area previously retained through execution of M * HOLD.

Input macro instruction set - Type Two - Arithmetic Register Communications

Code	Description
MCRO M * START f, P1,:	reads and checks the label on the first reel of file "f."
MCRO · M * ADV f, P1,:.	advances the next item into current status.
MCRO M * END f,: .	early termination of file.

Output macro instruction set - Type Two - Arithmetic Register Communications

Code	Description
MCRO M * START f,:	writes label on first reel of "f."
MCRO M * ADV f,: .	advances neat area to current status.

§ 172.

.81 Macro (Contd.)

Code		Description
MCRO	M * ENDR f,:	terminates current reel of file "f" and writes label on next reel of file "f."
MCRO	M * END f,: . .	terminates file "f."

Area source macro set - Type Two - Arithmetic Register Communication

Code		Description
MCRO	M * ADV f,: .	advances next area into current status.

Subroutine Using

Servo 2ZZ: . . .	I/O control system for tape files using UNISERVO *II tape units.

Input Code		Description
MCRO	M * INIT,: . .	Initialize, read first record.
	M * READ,: .	Read a record.
	M * RWI,: . .	Rewinds with interlock.
	M * RWO,: . .	Rewinds without interlock.

Output Code		Description
MCRO	M * INIT,: . .	Initialize output.
	M * BWRITE,:	Write 720 character block.
	M * SWRITE,:	Write six 120 character blockettes.
	M * RWI,: . .	Rewind with interlock.
	M * RWO,: . .	Rewind without interlock.

Subroutine Using

CRD 80 RZZ,:	reads 80-column cards.

Code		Description
MCRO	M * INIT,: . .	sets all initial conditions for card reader.
MCRO	M * ADV,: . .	causes reading of cards in card reader.

Subroutine Using

CRD 90 RZZ:.	reads 90-column cards.

Code		Description
MCRO	M * INIT,: . .	sets all initial conditions of card reader.
MCRO	M * ADV,: . .	causes reading of cards in card reader.

Subroutine Using

PUN 80 PZZ: .	card punch 80-column cards.

Code		Description
MCRO	M * INIT:. . .	sets up initial conditions of 80-column card punch.

.81 Macro (Contd.)

Code		Description
MCRO	M * ADV:. . .	causes reserve storage area to be made available for editing data to be punched.
MCRO	M * PUNCH: .	causes punching of data from reserve storage area into a card.

Subroutine Using

PUN 90 PZZ,:	punches 90-column cards.

Code		Description
MCRO	M * INIT, . .	sets up initial conditions for 90-column card punch.
MCRO	M * ADV,: . .	causes reserve storage area to be made available for editing data to be punched.
MCRO	M * PUNCH,:.	causes punching of data from reserve storage area into a card.

Subroutine Using

RDPTTZZ,: .	read paper tape.

Code		Description
MCRO	M * INIT,: . .	sets initial conditions.
MCRO	M * RDPT,: .	causes reading of paper tape.

Subroutine Using

PUNPTTZZ,: .	punch paper tape.

Coding		Description
MCRO	M * INIT:. . .	sets all initial conditions.
MCRO	M * PUNPT: .	initiates paper tape punch instructions to punch data from the reserve area onto paper tape.

Subroutine Using

PRNT01ZZ:. .	printer subroutine.

Code		Description
MCRO	M * INIT:. . .	sets initial conditions of printer routine.
MCRO	M * SELECT, P2,:.	selects next 32-word printer storage area and makes it the current storage area.
MCRO	M * PRINT,: .	prints contents of area selected.
MCRO	M * PADN,n,:	causes paper to be advanced n lines. n = number of lines paper is to be advanced.
MCRO	M * PADTOL, 1,:	advances paper to line L. L = line number to which paper will be advanced.

§ 172.

.81 Macro (Contd.)

Arithmetic

Code	Description
MCRO DPM01,: . . .	Double precision multiplication produces a four-word decimal product by multiplying a two-word decimal multiplicand by a two-word decimal multiplier.
MCRO DPD01,: . . .	double precision divide produces a two-word decimal quotient and a two-word decimal remainder from a two-word dividend and two-word divisor.

Math functions

Subroutine Using

MATH PAC: .	used to call in following math functions if applicable.

Coding	Description
MATH * FAD:	compute sum of two floating point numbers.
MATH * FMP:	compute product of two floating point numbers.
MATH * FDV:	compute quotient of two floating point numbers.
MATH * DMP:	compute product of two double precision floating point numbers.
MATH * DDV:	compute quotient of two double precision floating point numbers.
MATH * NRM:	normalize floating point number into twelve digit integer.
MATH * FIT:	convert twelve digit integer into floating point number.
MATH * DTF:	convert on unnormalized double precision with a two digit scale factor into a floating point number.
MATH * SIN:.	compute value of SINE (X), where X is a floating point number.
MATH * COS:	compute value of cosine (X), where X is a floating point number.
MATH * TAN:	compute the value of TANGENT (X) where X is a floating point number.
MATH * A SIN:	compute the value of Arcsine (X), where X is a floating point number.
MATH * A COS:	compute the value of Arccosine (X) where X is a floating point number.
MATH * A TAN:. . . .	compute the value of Arctangent (X), where X is a floating point number.

.81 Macro (Contd.)

Code	Description
MATH * SIN H:	compute the value of Hyperbolic sine (X), where X is a floating point number.
MATH * COS H:	compute the value of Hyperbolic cosine (X) where X is a floating point number.
MATH * TAN H:. . . .	compute the value of Hyperbolic tangent (X), where X is a floating point number.
MATH * SQRT:	compute the value of the square root of X, where X is a floating point number.
MATH * CBRT:	the value of the Cube Root of X, where X is a floating point number.
MATH * LOGT:	compute the value of log (X) (base 10) where X is a floating point number.
MATH * LOGN:	compute the value of log (X) (base e), where X is a floating point number.
MATH * EXP:	compute the value of e^X, where X is a floating point number.
MATH * TENX:	compute the value of 10^X, where X is a floating point number.
MATH * XTOP:	compute the value of XP where both X and P are floating point numbers.

Other Macros

MOVEZZ:	provides coding to transfer a designated number of words from one memory location to another.

.82 Pseudos

Code	Description
DCML:	defines a decimal number not greater than 6 digits.
DDML:	defines a decimal number not greater than 12 digits.
BINY:.	defines a 1 to 24-bit binary number.
DTOB:	defines a decimal number which is to be translated to binary.
OTOB:	defines an octal number which is to be translated to binary.
ALPH:	defines up to 4 alphameric characters.
INAD:	defines an Indirect Address Control word.
FSEL:	defines a Field Select Control word.
XMOD:	defines an Index Register Modification Control word.
STOP:	defines a Stop Control word.
(.) period:	in SALT coding sheet form section means form is the same as previous form.

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.82 Pseudos (Contd.)

Code	Description
SGMT:	defines a segment line.
SGRT:	defines relationship of one segment to another.
MAPS:	equates a segment line with a particular index register designation.
LOCA:	defines program relative address of label referred to in contents.
SGAD:	defines program relative address of first line in segment which contains label line referred to by this form.
ZERO:	when used in SGMT statement defines the predecessor segment to be ZERO or no segment.
AREA:	defines space to accommodate data.
EQUL:	assigns a label to an actual or symbolic address.
EQDX:	assigns a label to a line relative to a data storage area.
STRT:	designates the starting address of a program.
OVER:	designates unexpected overflow condition routine.
INOP:	designates invalid operation routine.
LOAD:	defines an unbroken sequence of segments that are to be in core storage at the same time.
SER3:	defines UNISERVO III facility for a file.
SER2:	defines UNISERVO III facility for a file.
RDER:	defines Card Reader 80 facility for a file.
PNCH:	defines Card Punch 80 facility for a file.
PRINT:	defines High-Speed Printer facility for a file.
XLST:	defines input-output control word.
TCON:	defines length, direction, and location of typewriter message.
XLOC:	defines termination program, or overlay request, or memory dump request.
XFRE:	releases or assigns hardware facilities to a file.

.82 Pseudos (Contd.)

Code	Description
LDID:	fabricates a five-word program identifier for the Executive Routine.
SUBR:	calls a subroutine.
INDX:	assigns index registers to subroutines.
SLCT:	selects specific parts of subroutines.
MCRO:	calls a macro.
CONF:	defines subroutine configurations.
MCDF:	defines first line of a macro.
MCND:	defines last line of a macro.
PCH9:	defines Card Punch 90 facility for a file.
RDR9:	defines Card Reader 90 facility for a file.
PAPT:	defines paper tape unit facility for a file.
TAPE:	fabricates a five-word tape packet for Executive Routine.
IOFS:	defines an input-output function specification control word by which user may request I/O.
XPAK:	input-output control word defined in XLST which defines I/O function used, address of required indicator coding and address of next XPAK in three lines connected by hyphens.
TPAK:	typewriter control word defines in XLST which defines typewriter section.
XFAD:	defines control word used in requesting memory dumps.
MAXM:	defines memory boundaries in order to allow more memory than program needs.
PART:	assigns a part number to a section of a subroutine.
SCAT:	defines a Scatter read/gather write control word.
DATE:	specifies an alphameric symbol which will occupy one computer word. The value specified by this form may be replaced in the program by another value after assembly.

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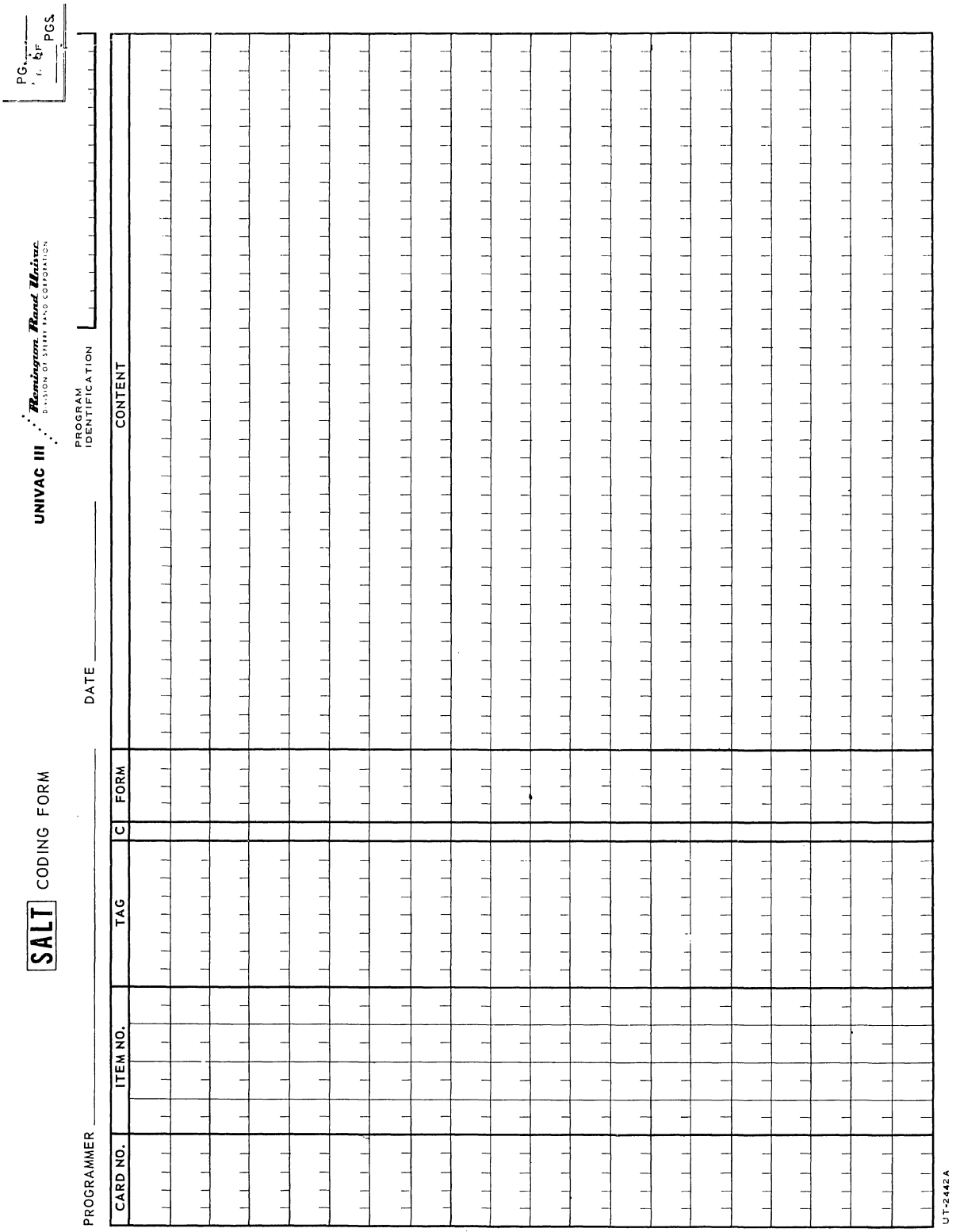
APPENDIX "A"



OPERATING ENVIRONMENT: SALT EXECUTIVE ROUTINE

§ 191.

.1 GENERAL

.11 Identity: . . . . . SALT Executive System.
SALT Library Routines.
(formerly called CHIEF Executive System and Duty Service Library Routine, respectively.)

.12 Description

The SALT Executive System and the SALT Library Routines provide a comprehensive operating system for the UNIVAC III that is the key to effective use of the multi-running capabilities of the UNIVAC III hardware (i.e., the ability to process several independent programs concurrently). The object programs produced by the SALT Translator, and the translator itself, are designed for operation under control of the SALT Executive Routine. However, no compatibility is maintained between SALT and the UTMOST machine oriented language. The SALT Library Routines provide the facilities to make additions, deletions, or corrections to the Master Program Library and prepare the Master Instruction Tape in the format required for input. The Master Instruction Tape is a linked series of object programs with a specified order of execution. SALT Library Routines are run under control of the SALT Executive Routines.

SALT Executive Routines are a related set of subroutines designed to provide automatic control over UNIVAC III system operation in the following areas:

Loading and executing programs.
Allocation of core storage and external units.
Input-output operations.
Multi- and concurrent processing.
Automatic handling of most errors.
Communication between operator and system.
Logging of system operations.

The Master Instruction Tape is prepared by the SALT Object Code Service routines from the following input:

A Master Program Library, which contains the object programs for the system.
Additional object programs for the system.
A control file containing: system parameter specifications, schedule of runs to be performed, and corrections for object programs.

The Object Code Service routines create an updated Master Program Library, a Master Program Library listing, and the Master Instruction Tape. The Master Instruction Tape contains the schedule of computer runs, the system parameter definitions, and the object programs, including the executive routine as the first program on the tape.

After the executive program has been loaded from the Master Instruction Tape, operational control of the computer is completely automatic. The predetermined schedule establishes the sequence of loading object programs, but the operator can change this sequence via the input typewriter. Core storage and external units are assigned by continually updating a table of available facilities as outlined by the system parameter specifications. If insufficient facilities are available for the program, a message is typed out and the operator can then type in the desired corrective action. Assignment of facilities is optimized by allocation of the smallest segment of available core storage large enough to hold the program being loaded. This mode of memory allocation can be altered by the programmer to assign either the highest or the lowest order memory area which is available at run time. External facilities can be assigned on a demand or optional basis as specified in the object program, thus providing a wide margin for flexibility and optimization of available equipment.

Requests for input-output operations are controlled and scheduled by the executive routine. Requests are serviced on a first-come, first-served basis for the input-output channel involved. The automatic program interrupt feature dictates when requests are serviced. If more than one interrupt occurs simultaneously, those from Uniservo III Synchronizers are first, followed by those from the General Purpose Channels in an order determined by the speed of their connected units.

Multi- and concurrent processing are scheduled and controlled by the executive routine. As each program is loaded into storage, a control address is added to the end of a priority list. When control is released to the executive routine either by an automatic program interrupt or by a voluntary release of control by the program, the control address of the interrupted program is placed at the end of the priority list and the control addresses which follow it are advanced on the list. After servicing the release of control or interrupt, control is returned to the program which is currently at the head of the priority list. Control is rotated to each of the concurrent programs in this manner, permitting independently prepared programs to share both the available input-output facilities and the available computer time.

All automatic program interrupt conditions are serviced by the executive routine. If unique corrective procedures are required, control is transferred to the program involved for the specific corrective action.

§ 191.

.12 Description (Contd.)

If the condition cannot be corrected, the executive routine determines whether to terminate only the program involved or all currently running programs. In either event, the operator can initiate restart procedures and/or diagnostic memory dumps by typing in the appropriate option.

.13 Availability

SALT Executive System: currently available.
SALT Library:. . . . . currently available.

.14 Originator:. . . . . UNIVAC Division.

.15 Maintainer: . . . . . UNIVAC Division.

.16 First Use: . . . . . June, 1962.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries:. . . . . Master Instruction Tape contains pre-assembled relocatable programs which can be called either from a predetermined schedule or from operator intervention.

.212 Independent programs: preassembled relocatable programs called by operator intervention.

.213 Data:. . . . . 50 words of data used as a parameter.

.214 Master routines:. . . . incorporated in the Master Instruction Tape.

.22 Library Subroutines: . incorporated in the Master Instruction Tape in relocatable form and called automatically.

.23 Loading Sequence: . . . pre-determined schedule incorporated on the Master Instruction Tape can be varied by operator intervention at any time.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . . routines can be segmented by the insertion before assembly of segment and overlay statements.

.312 Occupation of working storage: . . . relocation codes are inserted in object program at time of assembly. routines can be loaded anywhere in core storage.

.32 Input-Output Units

.321 Initial assignment:. . . either specified when program is written or can allow assignment at object time.

.322 Alternation: . . . . . specified in parameters defining allocation of hardware for each program.

.323 Reassignment: . . . . . operator can at all times choose which physical tape units shall be used by typing in selection.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: initiated by program and supervised by SALT Executive System.

.42 Multi-programming:. . supervised by SALT Executive System in rotation. Sequence activated by return of control to SALT Executive System. Number of programs limited by physical capacity of equipment available.

.43 Multi-sequencing: . . . none.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Allocation impossible:	check	typed message to operator.
In-out error - single:	check	reposition and re-read tape.
In-out error - persistent:	check	operator option to try again or to jettison the run.
Loading input error:	check	same as 1 in-out error.
Storage overflow:	none.	
Invalid instructions:	check	typed message to operator.
Arithmetic overflow:	check	programmed routine.
Invalid operation:	check	programmed routine.
Improper format:	check	typed message to operator.
Invalid address:	checked only when tracing	error indicator in trace routine output.
Reference to forbidden area:	checked only when tracing	error indicator in trace routine output.

.45 Restarts

.451 Establishing restart points: . . . . . when memory dump requests occur in program.

.452 Restarting process: . . type in request to SALT Executive System specifying the number of the memory dump required for restart. The location of SALT Executive System will then automatically restart the process.

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.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . available from the library by calling program. Printed output showing contents of all registers and operation conditions.

.512 Snapshots: . . . . . available from the library by calling program. Output in memory print format.

.52 Post Mortem: . . . . . available from the library by operator exercising option. dumps can be used for restart or for diagnostic purposes.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . . accept, reject, or change facility allocations and for persistent input-output errors; has option to try again or jettison the run.

.612 Action required by operator: . . . . . tape and card handling, and initiation of new programs as facilities become available.

.613 Reporting progress of run: . . . . . console typewriter types log.

.62 Operator's Decisions: . typed in from console typewriter.

.63 Operator's Signals

.631 Inquiry: . . . . . typewriter inquiry.

.632 Change of normal progress: . . . . . typed in from console typewriter.

.7 LOGGING

.71 Operator Signals: . . . console typewriter or log tape.

.72 Operator Decisions: . . console typewriter or log tape.

.73 Run Progress: . . . . . console typewriter or log tape.

.74 Errors: . . . . . console typewriter or log tape.

.75 Running Times: . . . . console typewriter.

.76 Multi-running Status: . console typewriter and listing.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: 6 Uniservo III tape units.
1 Uniservo III Synchronizer.
8,192 words of core storage.
1 High Speed Reader.
1 High Speed Printer.

.812 Usable extra facilities: all.

.813 Reserved equipment: . 1 magnetic tape for the Master Instruction Tape.
approximately 2,970 words of core storage.

.82 System Overhead

.821 Loading time: . . . . . less than 10 seconds after Master Instruction Tape has been mounted.

.822 Reloading frequency: . once a day or until such time as it is desired to run the system under control of another routine.

.83 Program Space Available: . . . . . C-2,900 words.
where C = words of core storage available.

.84 Program Loading Time: done in parallel while other programs are running.

.85 Program Performance: the major overhead is the processing of input-output requests and interrupts. This amounts to approximately 2 milliseconds of central processor time per request. Other input-output requests continue concurrently during this processing time.

NOTES ON SYSTEM PERFORMANCE

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The UNIVAC III system has the ability to process several independently prepared programs concurrently. The manufacturer recommends that the system be programmed so as to obtain the maximum throughput capabilities of the system.

The practical approach to this end is to generate several small programs rather than one large one (e.g., a card-to-tape, a tape-to-tape, and a tape-to-print program, as opposed to one large program to achieve the desired results directly from card input to print output). This approach releases the central processor and high speed peripherals for other jobs rather than monopolize the entire system for the total time required by the slowest peripheral unit.

The system performance problems are based on the assumption that the problem is the only one the system has to process. This approach therefore uses the one-large-program method, and effectively monopolizes the entire system for the total time it takes the slowest peripheral unit, which in the selected problem is in most cases, the printer.

The solid-line curve on the graphs indicates that total time to process the problem. The CP curve indicates the time the central processor is monopolized. The amount of central processor time available for multi-running can be read by taking the difference between the two curves.

UNIVAC III
SYSTEM PERFORMANCE

UNIVAC III SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 1

Worksheet	Item		Configuration								Reference
			III		VI		VII A		VIII B		
									C. P.	Blocked Details	Unblocked Details	
1 Input-Output Times	Char/block	(File 1)	1,092		1,092		1,092			1,092	1,092	4:200.112
	Records/block	K (File 1)	13		13		13			13	13	
	m.sec/block	File 1 = File 2	14.2		14.2		14.2			14.2	14.2	
		File 3	85.7		85.7		85.7			15.8	8.6	
		File 4	126.5		126.5		126.5			20.4	8.9	
	m.sec/switch	File 1 = File 2	0		0		0			0	0	
		File 3	0		0		0			0	0	
		File 4	0		0		0			0	0	
	m.sec penalty	File 1 = File 2	1.1		1.1		1.1			1.1	1.1	
		File 3	1.92		1.92		1.92			1.04	0.08	
		File 4	0.13		0.13		0.13			1.69	0.13	
2 Central Processor Times	m.sec/block	a1	0.192		0.192		0.192		0.192			4:200.1132
	m.sec/record	a2	0.364		0.364		0.364		0.364			
	m.sec/detail	b6	0.064		0.064		0.064		0.064			
	m.sec/work	b5 + b9	1.474		1.474		1.474		1.474			
	m.sec/report	b7 + b8	2.153		2.153		2.153		2.153			
3 Standard Problem A F = 1.0	m.sec for C. P. and dominant column.	a1	0.192		0.192		0.192		0.192			4:200.114
		a2 K	4.732		4.732		4.732		4.732			
		a3 K	47.944		47.944		47.944		47.944			
		File 1 Master In	1.100		1.100		1.100		1.100			
		File 2 Master Out	1.100		1.100		1.100		1.100			
		File 3 Details	24.960		24.960		24.960		1.040			
		File 4 Reports	1.690	1,644.5	1.690	1,644.5	1.690	1,644.5	1.690	20.4	114.7	
		Total	81.718	1,644.5	81.718	1,644.5	81.718	1,644.5	57.798	20.4	114.7	
4 Standard Problem A Space	Unit of measure	(word)										4:200.1151
		Std. routines	4,990†		4,990†		4,990†			4,183†	4,990†	
		Fixed	0		0		0			0	0	
		3 (Blocks 1 to 23)	162		162		162			162	162	
		6 (Blocks 24 to 48)	420		420		420			420	420	
		Files	1,344		1,344		1,344			2,400	1,344	
		Working	100		100		100			100	100	
		Total	7,016		7,016		7,016			7,265	7,016	

† Includes 3,000 words for the Executive routines.

UNIVAC III SYSTEM PERFORMANCE (Contd.)

WORKSHEET DATA TABLE 2						
Worksheet	Item		Configuration			Reference
			III, VI, VII A			
5	Fixed/Floating point		Fixed	Floating		
	Unit name	input	Uniservo III	Uniservo III		
		output	Printer	Printer		
	Size of record	input	80 characters	80 characters		
		output	128 characters	128 characters		
	m.sec/block	input T1	8.6	8.6		
		output T2	126.5	126.5		
	m.sec penalty	input T3	0.08	0.08		
		output T4	0.13	0.13		
	m.sec/record	T5	0.068	0.068		
	m.sec/5 loops	T6	16.524	24.001		
	m.sec/report	T7	3.084	3.084		
Standard Mathematical Problem A						4:200.413

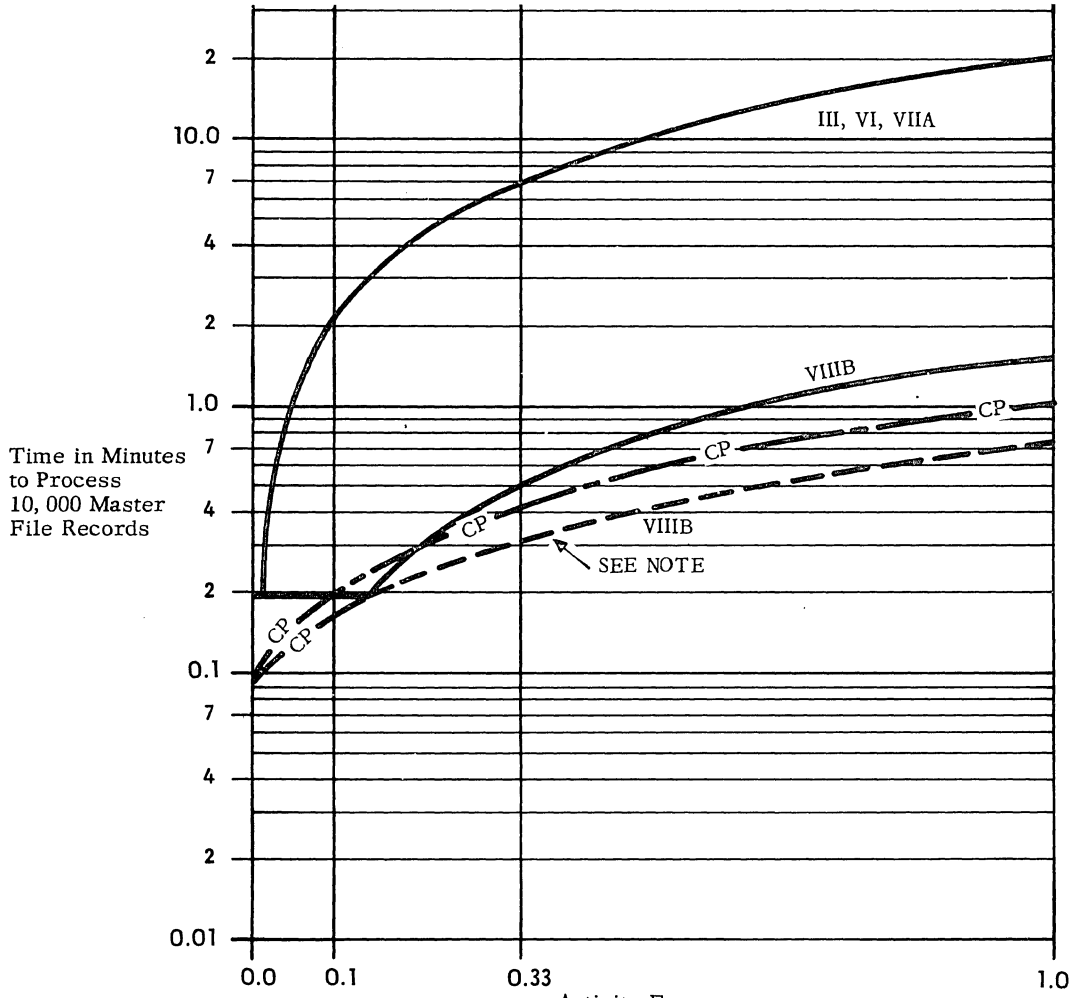
SYSTEM PERFORMANCE

§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.
.112 Computation: . . . . . standard.
.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.
.114 Graph: . . . . . see graph below.
.115 Storage space required
Configuration III: . . . 7,016 words.
Configuration VI: . . . 7,016 words.
Configuration VIIA: . . 7,016 words.
Configuration VIIIB (unblocked details):. . 7,016 words.
Configuration VIIIB (blocked details):. . . 7,016 words.



LEGEND

——————— Elapsed Time; Unblocked Files 3 & 4
— — — — — — — — Elapsed Time; Blocked Files 3 & 4
——— CP ——— — — Central Processor Time

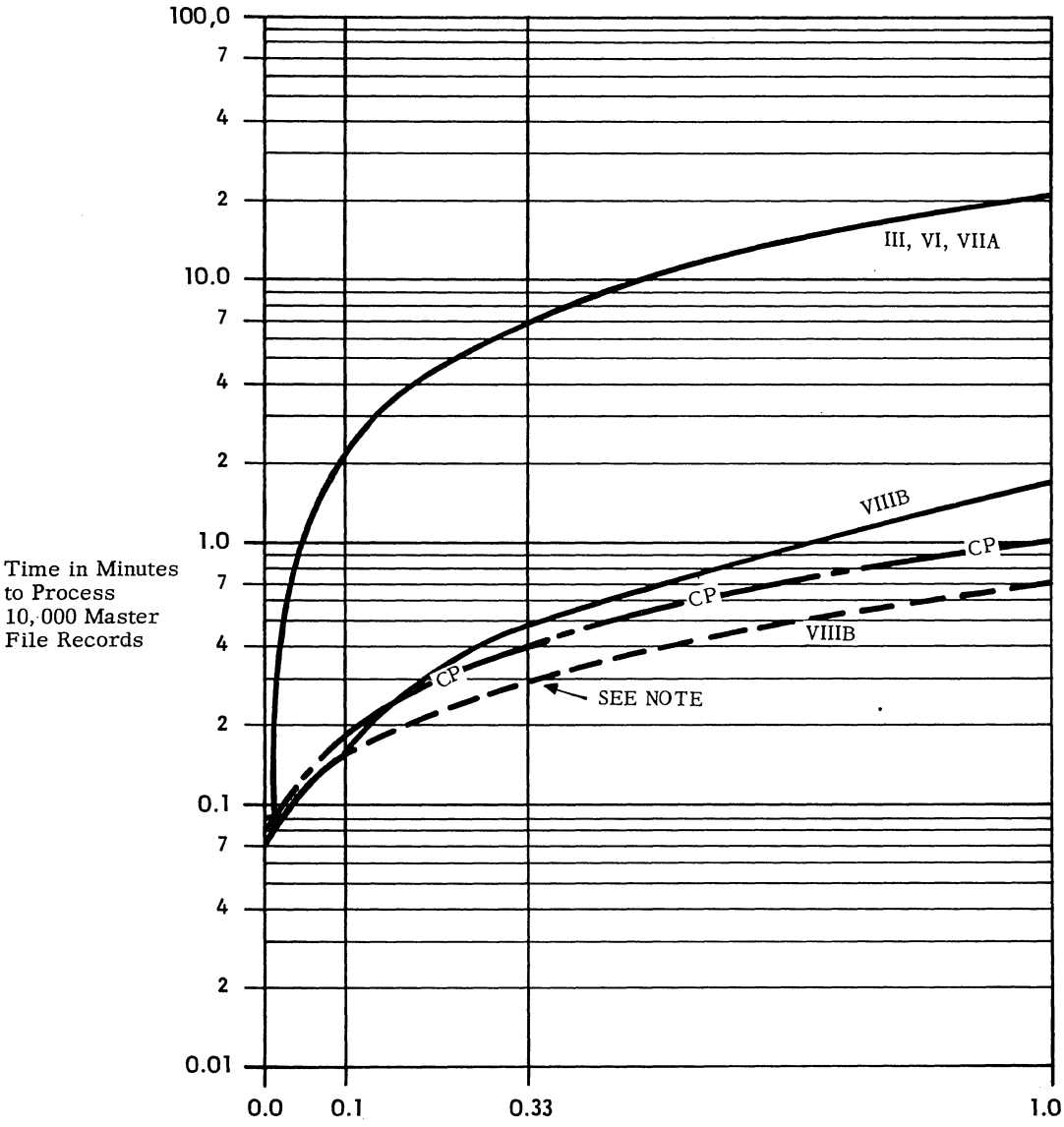
Note: This line also represents Central Processor Time for Configuration VIIIB.

§ 201.

.12 Standard File Problem B

.121 Record sizes
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



LEGEND

Elapsed Time; Unblocked Files 3 & 4
Elapsed Time; Blocked Files 3 & 4
CP Central Processor Time

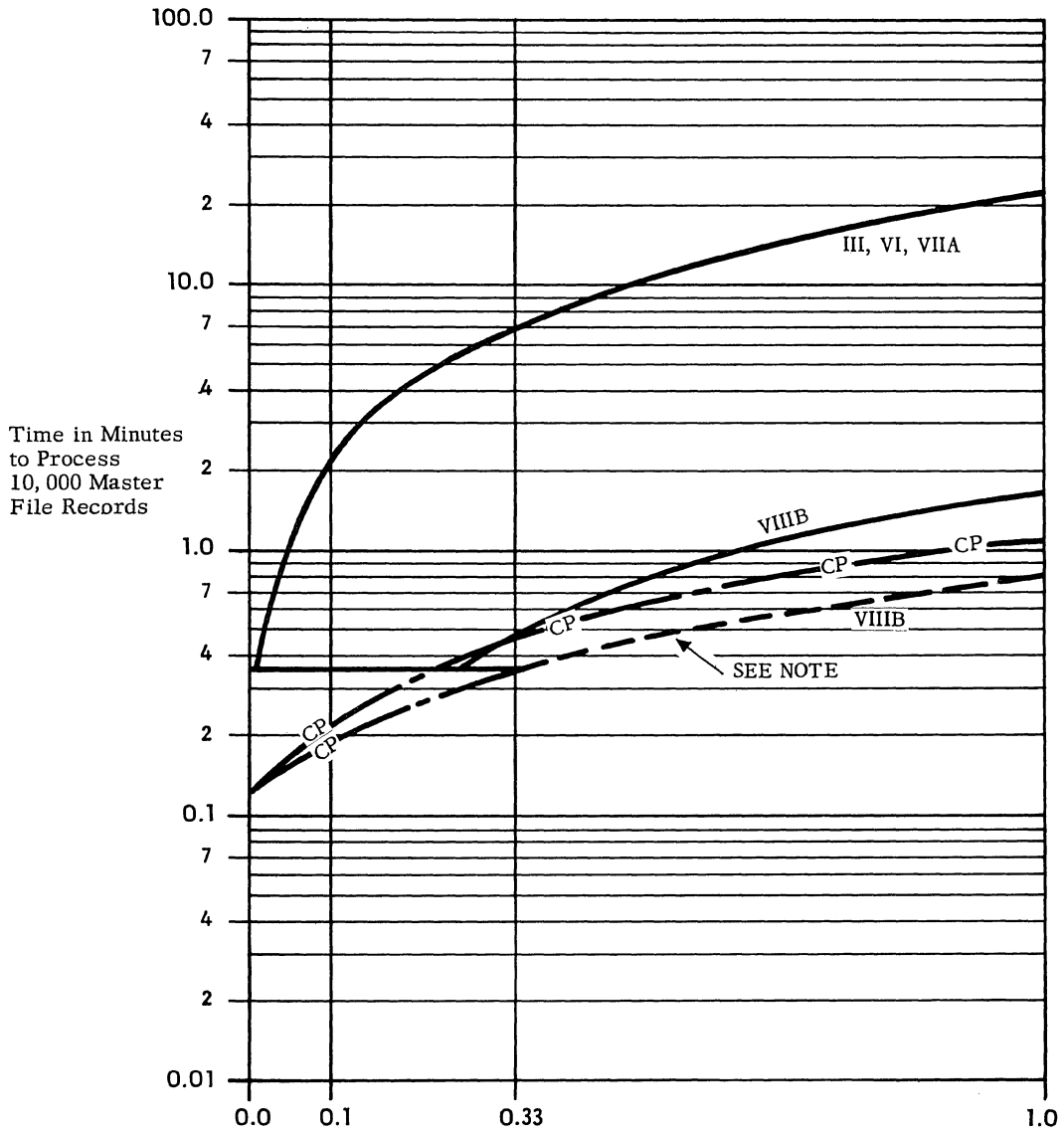
Note: This line also represents Central Processor Time for Configuration VIIIB.

§ 201.

.13 Standard File Problem C

.131 Record sizes
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.



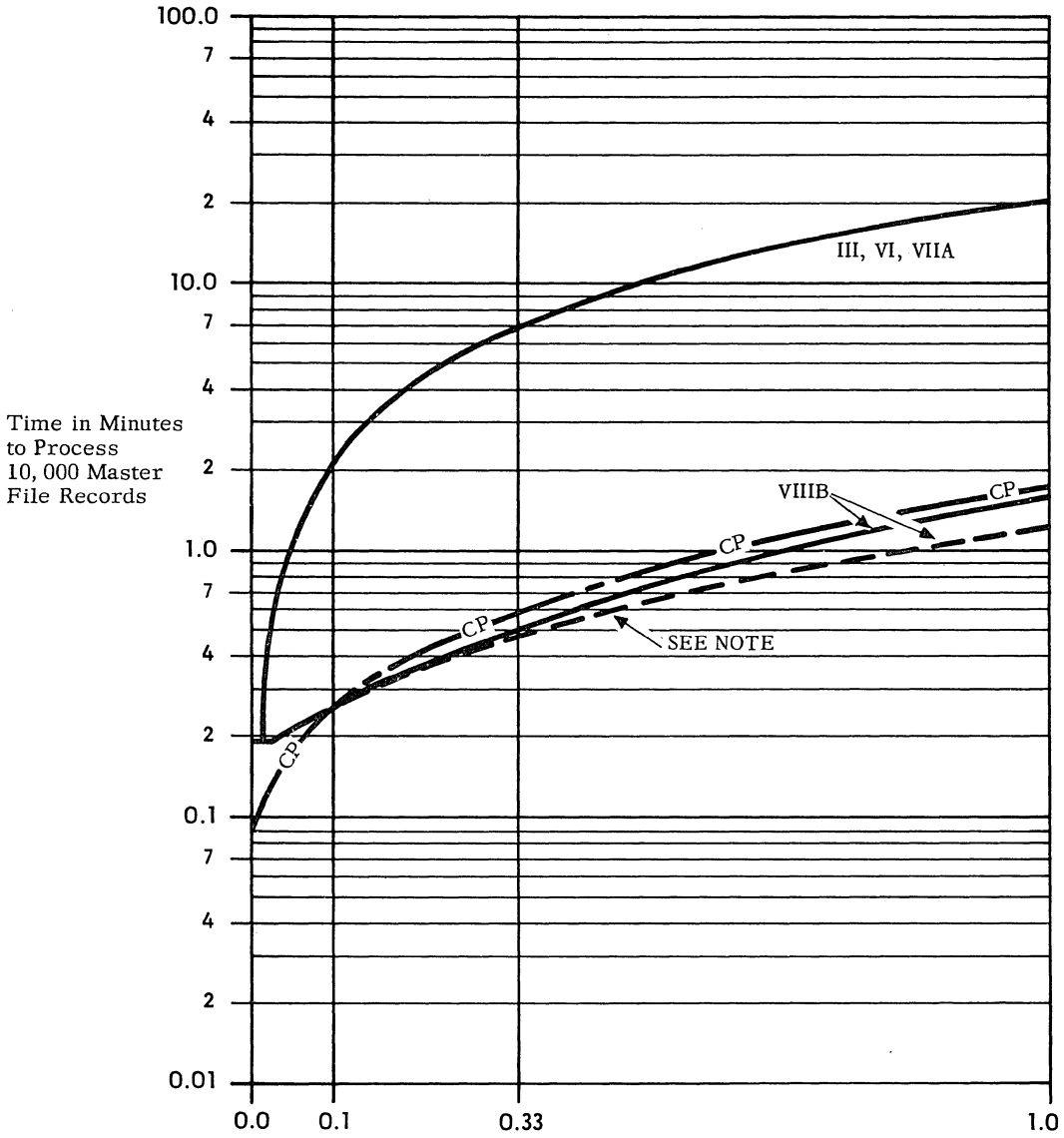
Note: This line also represents Central Processor Time for Configuration VIIIB.

§ 201.

.14 Standard File Problem D

.141 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.144 Graph: . . . . . see graph below.



Note: This line also represents Central Processor Time for Configuration VIIIB.

§ 201.

.2 SORTING

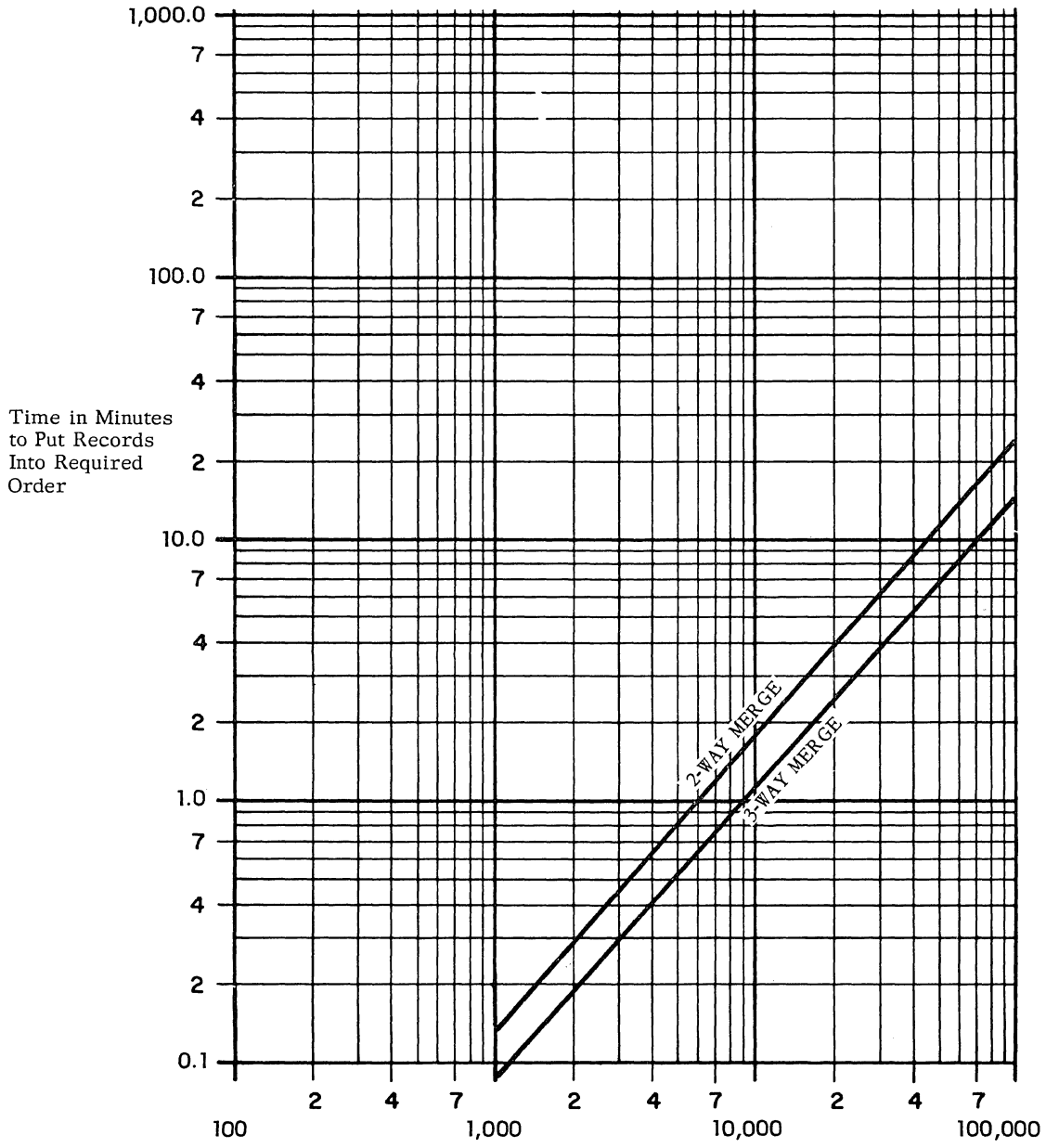
.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.

.212 Key size: . . . . . 8 characters.

.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . . see graph below.



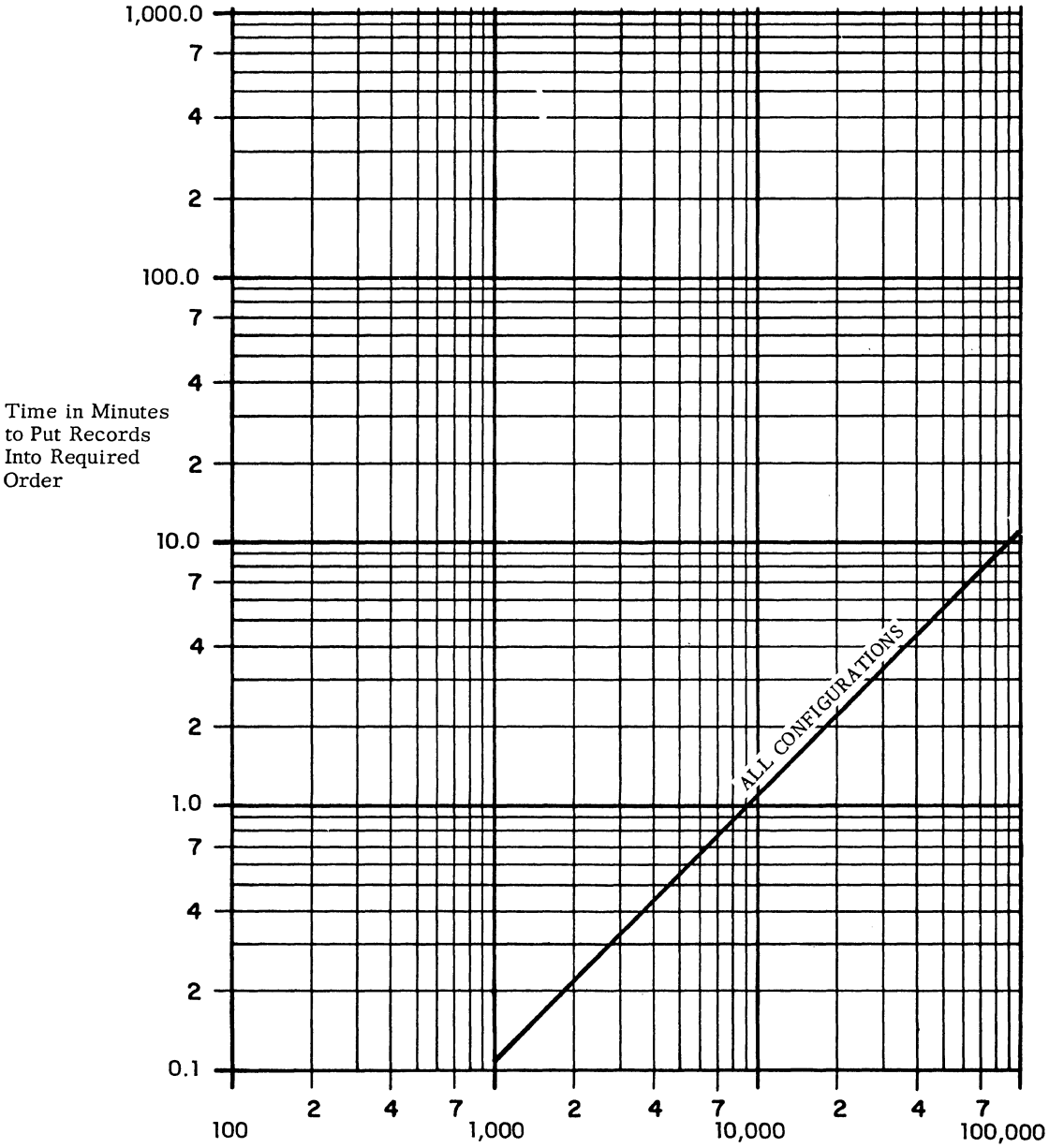
§ 201.

.22 SODA SORT

.221 Record size: . . . . . 80 characters.
.222 Key size: . . . . . 8 characters.

.223 Timing basis: . . . . UNIVAC Publication UT 2504, using 5,600 words of core storage for internal sorting and 6 tape units.

.224 Graph . . . . . see graph below.



§ 201.

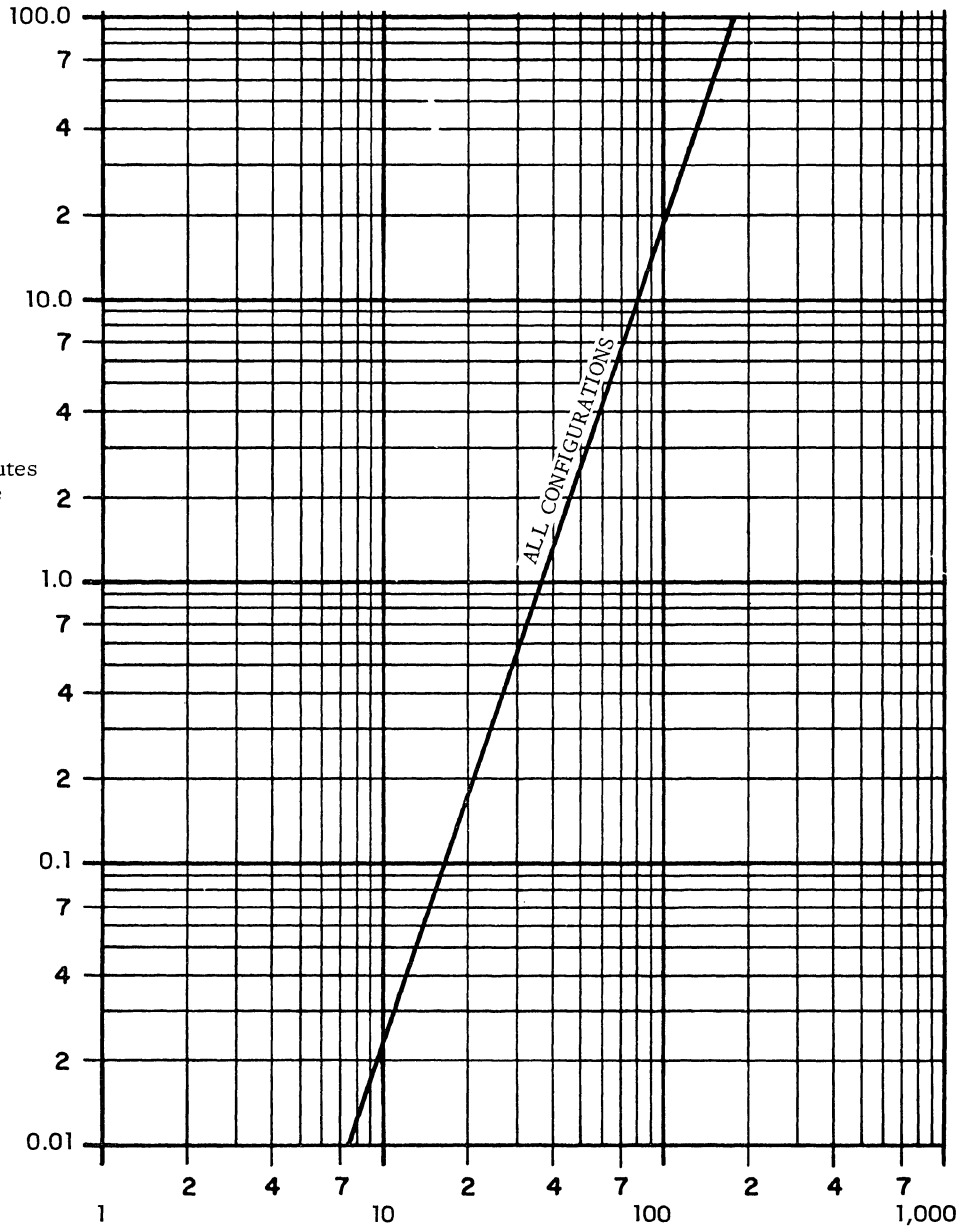
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic Parameters: . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312 with floating point subroutine times from Support III.

.313 Graph: . . . . . see graph below.



§ 201.

.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

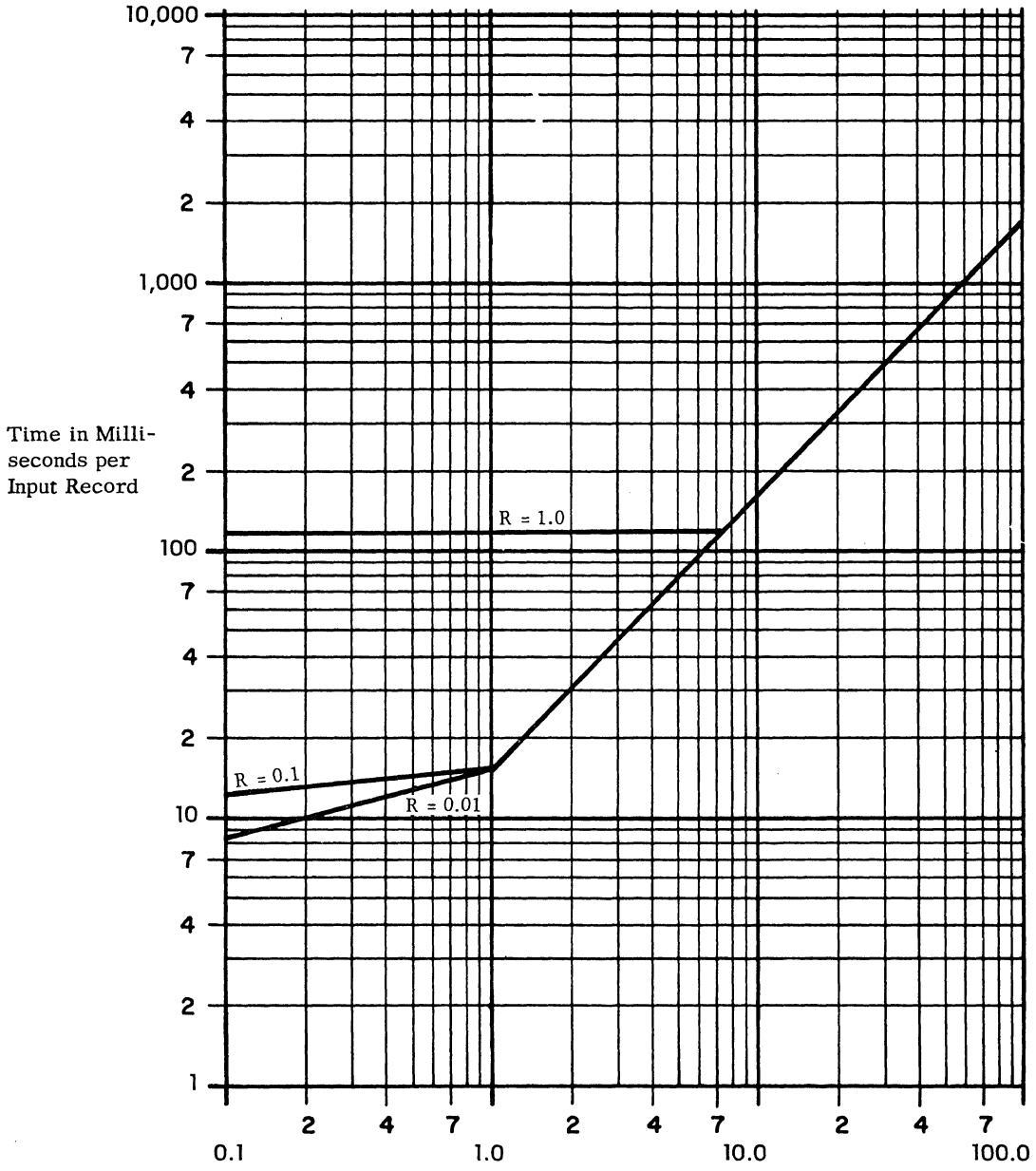
.411 Record sizes: . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

.412 Computation: . . . . . 5 fifth-order polynomials.
5 divisions.
1 square root.

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . . see graph below.

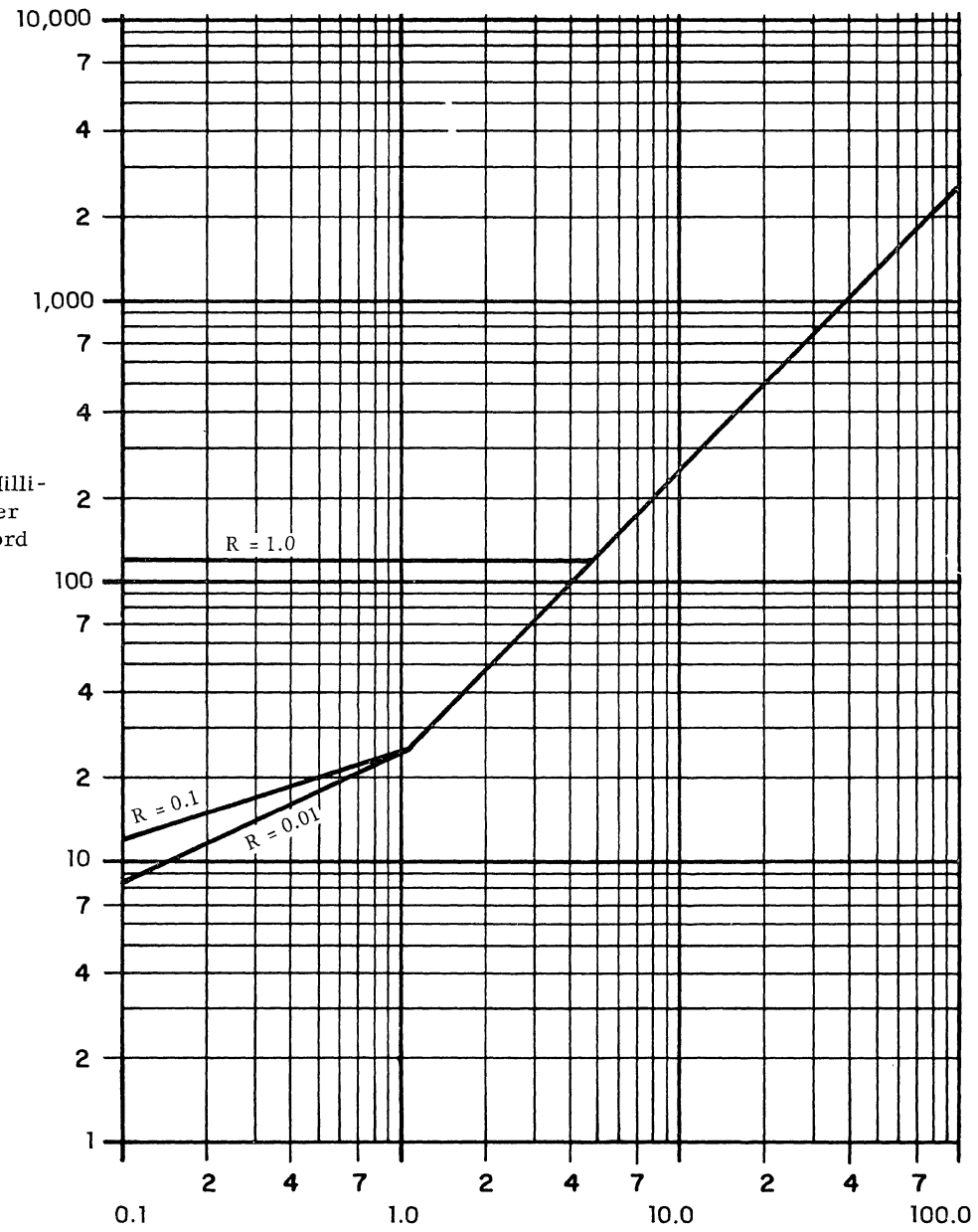
CONFIGURATION III, VI, VIIA; DOUBLE LENGTH (12 DIGIT PRECISION); FIXED POINT.
R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



§ 201.

.415 Graph: . . . . . see graph below.

CONFIGURATION III, VI, VIIA DOUBLE LENGTH (12 DIGIT PRECISION); FLOATING POINT
R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



Time in Milli-seconds per Input Record

C, Number of Computations per Input Record

UNIVAC III
PHYSICAL CHARACTERISTICS

UNIVAC III PHYSICAL CHARACTERISTICS

			Arithmetic and Control	Console	Power Control	Power Supply	16,384-Word Core Storage*	8,192-Word Core Storage	Uniservo III Synchronizer	Uniservo III and II Synchronizer	Uniservo IIIC Synchronizer
IDENTITY	Unit Name										
	Model Number		4121	4121	4121	4121	4122	4122	4135	4144	
PHYSICAL	Height × Width × Depth, in.		70×44×33	30×69×33	70×44×33	71×45×33	70×22×33	70×22×33	70×44×33	70×44×33	
	Weight, lbs.		1,400	500	2,000	2,800	870	650	1,400	1,400	
	Maximum Cable Lengths to Designated Units, Feet		†	61 (4121 Power Control)	†	†	†	†	61 (To last 4126 or 4072 in-line via the Related Transition Cabinet)	61 (To last 4126 or 4072 in-line via the Related Transition Cabinet)	
ATMOSPHERE	Storage Ranges	Temperature, °F.	← Normal Atmospheric Conditions →								
		Humidity, %	← Normal Atmospheric Conditions →								
	Working Ranges	Temperature, °F.	← 60-80 →								
		Humidity, %	← 40-70 →								
	Heat Dissipated, BTU/hr.		4,400	---	6,200	14,000	12,300	12,300	3,760	4,100	INA
	Air Flow, cfm.		1,000	---	500	2,300	1,400	1,400	1,000	1,000	
	Internal Filters		← Yes →								
ELECTRICAL	Voltage	Nominal	‡	‡	208	‡	‡	‡	‡	‡	
		Tolerance	‡	‡		‡	‡	‡	‡	‡	
	Cycles	Nominal	‡	‡	60	‡	‡	‡	‡	‡	
		Tolerance	‡	‡	±½	‡	‡	‡	‡	‡	
	Phases and Lines		‡	‡	3-phase, 4-wire separate ground	‡	‡	‡	‡	‡	
	Load KVA		1.6	---	2.3	5.2	4.5	4.5	1.4	1.5	
NOTES	† Central processor modules assembled side by side; no cable required. ‡ Power supplied by Power Control, Model 4121.						* For 32,768 word core storage, double BTU/hr, Air Flow, KVA				INA — Information not available.

UNIVAC III PHYSICAL CHARACTERISTICS (Contd.)

	Unit Name		Uniservo II Tape Unit	Uniservo IIIA Tape Unit	Uniservo IIIC Tape Unit	Uniservo Power Supply	Uniservo IIIC Tape Adapter Cabinet	Paper Tape Unit	80-column Card Reader	90-column Card Reader	80-column Card Punch	90-column Card Punch	Printer	Transition Unit I	Transition Unit II	Transition Unit III	Corner Cabinet
IDENTITY	Model Number		4072	4126	↑	4123	↑	4181	4133	4182	4127	4183	4152				
PHYSICAL	Height × Width × Depth, in.		69 × 31 × 30	64 × 31 × 30		70 × 45 × 33		66 × 40 × 35	53 × 56 × 29	53 × 56 × 29	48 × 56 × 32	48 × 56 × 32	55 × 77 × 35	71 × 12 × 35	71 × 12 × 35	70 × 12 × 33	64 × 30 × 30
	Weight, lbs.		745	745		2,800		500	800	800	775	775	2,100	100	150	150	200
	Maximum Cable Lengths to Designated Units, Feet		61 (From last unit in line to Synchronizer via Related Transition Cabinet)	61 (From last unit in line to Synchronizer via Related Transition Cabinet)		---		← 61 (4121 Arithmetic and Control Unit) →						---	---	---	---
ATMOSPHERE	Storage Ranges	Temperature, °F.	Normal Atmospheric Conditions			Normal Atmospheric Conditions		← Normal Atmospheric Conditions →									
		Humidity, %	Normal Atmospheric Conditions			Normal Atmospheric Conditions		← Normal Atmospheric Conditions →									
	Working Ranges	Temperature, °F.	← 60-80 →			60-80		← 60-80 →									
		Humidity, %	← 40-70 →			40-70		← 40-70 →									
	Heat Dissipated, BTU/hr.		7,140	7,480	INA	10,340	INA	6,850	3,760	3,760	4,780	4,780	11,950	---	680	680	---
	Air Flow, cfm.		300	350		2,300		550	250	250	250	250	900	---	150	150	---
	Internal Filters		Yes	Yes		No		Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	
ELECTRICAL	Voltage	Nominal	◊	◊		208		‡	‡	‡	‡	‡	‡	◊	◊	◊	
		Tolerance	◊	◊				‡	‡	‡	‡	‡	‡	◊	◊	◊	
	Cycles	Nominal	◊	◊		60		‡	‡	‡	‡	‡	‡	◊	◊	◊	
		Tolerance	◊	◊		±½		‡	‡	‡	‡	‡	‡	◊	◊	◊	
	Phases and Lines		◊	◊		3 phase, 4 wire separate ground		‡	‡	‡	‡	‡	‡	◊	◊	◊	
	Load KVA		2.63	2.75		3.8		2.5	1.4	1.4	1.8	1.8	4.4	---	0.25	0.25	---
NOTES	‡ Power supplied by Power Control, Model 4121. ◊ Power supplied by Uniservo Power Supply, Model 4123.				INA — Information not available.		INA — Information not available.										

§ 221. PRICE DATA

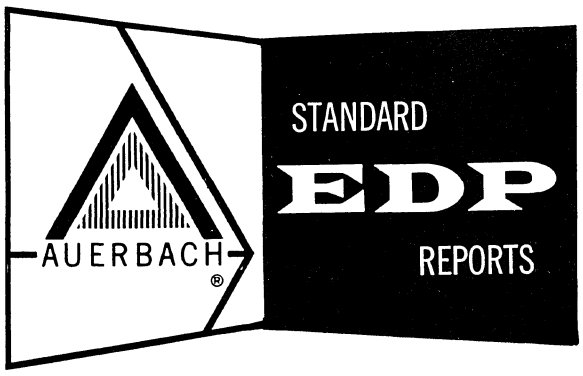
CLASS	IDENTITY OF UNIT		PRICES as of 12-19-62		
	No.	Name	Monthly Rental $	Single-Shift Monthly Maintenance $	Purchase $
Central Processor	4121	UNIVAC IIIA Central Processor Includes: Arithmetic and Control Module 8,192-word Core Storage Power Supply Module Power Control Module Control Console 9 Index Registers	8,000	500	390,000
		Optional Features			
	4197	Additional 8,192-word Core Storage	1,400	90	67,500
	4122	Additional 16,384-word Core Storage	3,000	150	144,000
		Additional 24,576-word Core Storage	4,030	200	193,500
		Programmable Clock	200	40	10,000
		6 Additional Index Registers	300	12	15,000
Input-Output	4209	Uniservo IIIA Magnetic Tape Unit	750	155	36,500
	4072	Uniservo IIA Magnetic Tape Unit	450	90	20,000
	NA	Uniservo IIIC Magnetic Tape Unit	800	62	38,400
	4133	Card Reader (80-column)	750	150	35,000
		Optional Features			
	NA	90-Column Reader Feature for 80-column Reader	35	NA	1,350
	NA	Stub Card Feature for 80-column Reader	60	NA	3,000
	4182	Card Reader (90-column)	750	150	35,000
		Optional Features			
	NA	80-Column Reader Feature for 90-column Reader	35	NA	1,350
	NA	Stub Card Feature for 90-column Reader	60	NA	3,000
	4127	Card Punch (80-column)	850	285	40,000
	4183	Card Punch (90-column)	850	285	40,000
	4152	Printer	1,650	360	79,000
		Optional Features			
	NA	When specified at time printer is ordered Currently Available Special Characters Set (Special Character Print Drum manufactured to identical specifications of a previously manufactured Print Drum)	---	---	250
	NA	New Special Character Set Art Work, Glass Master, and Etching Negative	---	---	2,500
		Each Special Character	---	---	75
		Additional Drum for previously manufactured Printer			
	NA	Currently Available Special Character Set (Same specifications as above)			1,700†
	NA	New Special Character Set (Same specifications as above) Replacement Print Drum			3,950†
		Each Special Character			75
	4181	Paper Tape Read and Punch Unit	1,600	143	80,000
Controllers	NA	Uniservo IIIA Synchronizer (Includes Read-Read Feature)	2,900	200	145,000
	4144	Uniservo IIA Synchronizer	1,925	150	92,500
	NA	Uniservo IIIC Synchronizer	2,050	109	102,500
	NA	Uniservo IIIC Tape Adapter Cabinet	1,000	50	48,000
Power	4123	Uniservo Power Supply	350	30	17,500

NA - Not Available.
† - Plus $12 per hour installation charge.

UNIVAC 1050

Univac

(A Division of Sperry Rand Corporation)



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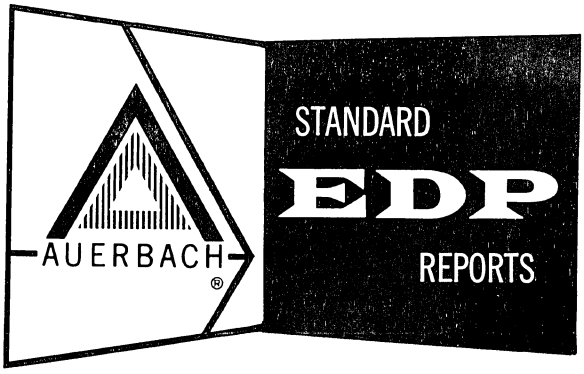
UNIVAC 1050

Univac

(A Division of Sperry Rand Corporation)



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CONTENTS

§ 001.

INTRODUCTION

§ 011.

The UNIVAC 1050 is a small to medium scale, solid-state computer that is oriented toward business data processing applications. Two central processors and associated core memories are available for use in 1050 systems: the Model III and the Model IV. Both models have the same set of instructions and are completely program-compatible, given the same peripheral equipment and input-output channel assignments. Most instructions are executed about 3.5 times as fast by the Model IV processor as by the Model III. Typical internal processing speeds are about 8,500 instructions per second for the 1050 Model III and about 30,000 instructions per second for the 1050 Model IV.

A wide range of peripheral devices is offered for the UNIVAC 1050, permitting effective use of the system as an off-line input-output processor for larger, tape-oriented computers and as a control center for a data communications network. A novel feature (the 1050-1004 Adapter) permits the UNIVAC 1050 to be used as an "expansion package" to increase the processing capacity of UNIVAC 1004 installations. UNIVAC 1050 system rentals range from approximately $1,400 to over $20,000 per month, but most installations will probably fall within the $5,000 to $12,000 rental range.

The UNIVAC 1050 was conceived several years ago as a contender for the IBM 1401-class market. For marketing reasons, it was first announced in May 1962 as an off-line input-output processor, with a maximum of two magnetic tape units, for larger UNIVAC systems. An expanded version, the UNIVAC 1050-II, was developed which included communications and Fastrand mass storage equipment. This system was eminently successful — 152 systems were ordered by the U. S. Air Force in November 1963. Finally, in March 1964, the UNIVAC 1050 Model III and Model IV were announced as general-purpose, commercial EDP systems, with a complete line of peripheral equipment and software.

The first delivery of the Model III Processor was made in 1963, and first deliveries of the Model IV Processor are scheduled for 1965. Still another processor, with increased performance and capabilities, may be announced shortly. While the UNIVAC 1050 offers many useful features and is a relatively easy machine to program, its earlier origin is apparent in some performance comparisons of the Model III against other recently-announced computer systems in the same price class. The 1050 Model IV rents for $1,200 to $1,500 more than the Model III in typical configurations and will be considerably more competitive.

Hardware

UNIVAC 1050 systems using the Model III Processor can have from 4,096 (included with the processor) to 32,768 character positions of core storage in 4,096-character modules. Systems using the Model IV Processor can have from 8,192 (included with the processor) to 65,536 character positions of core storage in 8,192-character modules. Each core storage location contains six data bits and one parity bit. Cycle time is 4.5 microseconds per character in the Model III and 2.0 microseconds per two-character access in the Model IV.

The two Processors (Model III and Model IV) are functionally identical, differing only in instruction execution time and certain input-output channel features (discussed later). The processors have typical single-address logic, with the addition of add-to-storage capabilities. Two 16-character accumulators and 7 index registers are provided. Facilities for indirect addressing are not provided. Arithmetic is basically decimal, but binary add and subtract instructions are provided to facilitate address modification and binary arithmetic. (The core storage addressing mode is pure binary.) All operations are performed serially by character.

The basic instruction format is a 30-bit "binary word" (5 consecutive characters) which usually contains a 5-bit operation code, a 3-bit index register specification, a 16-bit address, and a 6-bit modifier. The External Function (input-output) instruction uses the 30 bits in a slightly different manner. Operand length is variable and can range from 1 to 16 characters for most instructions, as specified in the instruction. All instructions except the multiply and divide instructions and the input-output instructions can be indexed.

§ 011.

Extensive editing facilities, including character insertion, floating dollar, and check protection, are provided. A block transfer instruction can cause the transfer of up to 1,024 characters from one location in core storage to another. A translate instruction can automatically translate up to 64 different characters from one 6-bit code to any other 6-bit code defined by a table supplied by the programmer. The only optional hardware facility is the decimal multiply-divide feature. Floating-point arithmetic hardware is not available for the 1050 Processors.

An extensive system of interrupts and testable indicators provides program control. Interrupts are divided into three priority levels and may occur upon detection of such conditions as internal parity errors, operator request, decimal overflow, successful completion of an input-output operation, or malfunction of an input-output device. All interrupts except the one for internal parity errors can be program-inhibited. Recognition of an interrupt signal causes a transfer of control to a specific location, depending on the type of interrupt, which can contain a branch to a routine to handle the condition.

Testable indicators which enhance the interrupt system include indicators for decimal overflow and for the status of the device on a particular input-output channel. The results of comparisons and arithmetic functions are also indicated by testable indicators. Conditions that can be tested include equal, not-equal, greater-than, and less-than after comparisons, and result-zero, result-negative, and decimal or binary overflow after arithmetic operations.

There are eight input-output channels available for the Model III Central Processor, each of which is assigned to a single peripheral subsystem (i.e., there are no facilities for programmed switching of the channel assignments). Three (any three) channels are included in the basic price of the processor. The synchronizers (control units) for the card reader, card punch, and printer are internal to the main frame of the Model III Processor, each using one input-output channel. Two other channels are reserved for a magnetic tape subsystem, leaving three general-purpose input-output channels.

The Model IV Processor can also be equipped with up to eight input-output channels. Each of these channels is also connected full-time to a single peripheral subsystem, but the Model IV channels are all general-purpose (i.e., any peripheral subsystem can be plugged into any one of the channel positions).

The peripheral subsystems available for use in UNIVAC 1050 systems are summarized below. Each peripheral subsystem requires the full use of one input-output channel, except that a magnetic tape subsystem requires the use of two. Additional synchronizers will be required (on special order) to add a second card reader, card punch, or printer to a system using the Model III Central Processor.

- Card Reader: column reader; 800/900 or 600 cards per minute; 80 or 90 columns.
- Card Punch: row punch; 300 or 200 cards per minute; 80 or 90 columns.
- Printer: 700/922 or 600/750 lines per minute; 128 (132 optional) print positions; 63 printable characters.
- Uniservo III A Magnetic Tape Subsystem: 1 to 6 tape handlers; up to 133,000 characters per second; read-compute or write-compute overlap; read-after-write modulo-3 check; read-backward capability.
- Uniservo IV C Magnetic Tape Subsystem: 1 to 6 tape handlers; up to 90,000 characters per second, read-compute or write-compute overlap; read-after-write parity check; IBM 729- compatible.
- Uniservo VI C Magnetic Tape Subsystem: 1 to 16 tape handlers; up to 34,100 characters per second; read-write-compute overlap; read-after-write parity check; IBM 729-compatible; relatively low-cost.
- Fastrand I Mass Storage Subsystem: 1 to 8 storage units; over 66 million characters per storage unit; 93 milliseconds average access time; up to 185,000 characters per second data transfer rate; search feature; read-compute, write-compute, or position-compute overlap.

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- Fastrand II Mass Storage Subsystem: over 132 million characters per storage unit; otherwise same as Fastrand I.
- UNIVAC 1004 Subsystem: connects a UNIVAC 1004 Model I, II, or III (Computer System Report 770:) on-line with the UNIVAC 1050.
- Punched Paper Tape Subsystem: 1,000 or 300 characters-per-second reader; 110 characters-per-second punch; 5-, 6-, 7-, or 8-level tape.
- Standard Communications Subsystem: Communications Multiplexer controls 1 to 64 Communication Line Terminals; console typewriter can monitor messages; messages on all lines can be handled simultaneously; will accept various telephone and teletypewriter communications services with data transfer rates of up to 800 characters per second.

In typical business data processing systems using the Uniservo VI C tape handlers, simultaneity of input-output operations can be quite good; but in systems using the faster Uniservo III A or IV C tape handlers or Fastrand I or II, simultaneity can be severely restricted. The complete picture of the UNIVAC 1050's capabilities for simultaneous operations is complex, particularly for the Model III Processor, and is presented in detail in Sections 777:111 and 777:112 of this report.

Software

UNIVAC is developing a generously large array of software for the 1050 system. All of the programming systems and routines summarized below are scheduled for delivery before or during the first quarter of 1965.

- PAL JR: Basic symbolic assembly system, usable on minimum UNIVAC 1050 configurations with card input-output units and 4,096 character positions of core storage.
- PAL CARD: Basic symbolic assembly system, usable on expanded UNIVAC 1050 card-oriented systems with at least 8,192 positions of core storage. PAL CARD features more versatile input-output control routines than PAL JR.
- PAL 1004: A basic assembly system utilizing the UNIVAC 1004 for input and output.
- PAL TAPE: A more advanced assembly system requiring two magnetic tape units, card punch (optional if tape-only output is desired), card reader, printer, and at least 8,192 positions of core storage on the translating computer. Macro, file control, and library facilities are provided.
- PAL DRUM: A Fastrand-oriented version of PAL TAPE; a Fastrand magnetic drum replaces the magnetic tape units.
- PATCH Assembler: Provides the capability for patching object programs without the need for full reassembly. Facilities are provided for addition, deletion, or alteration of sections of coding. Input and output are on cards only.
- COBOL: Detailed language specifications for UNIVAC 1050 COBOL are not available to date; however, UNIVAC states that it will be implemented in accordance with the specifications for COBOL-61 Extended as announced November 20, 1962. UNIVAC plans to include all of Required COBOL-61, as defined in X3.4 COBOL Information Bulletin #3, and all the extensions accepted by the CODASYL Committee on November 1, 1963. The minimum configuration for COBOL compilation will probably include a printer, card reader, four tape units (all of the same type) and a minimum of 16,384 positions of core storage.

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- FORTRAN IV: Detailed language specifications for UNIVAC 1050 FORTRAN are not available to date, but UNIVAC states that it will be basically FORTRAN IV. UNIVAC expects the minimum configuration for compilation to include a printer, a card reader, four tape units (all of the same type) and a minimum of 16,384 positions of core storage.

- REGENT CARD: Provides facilities for generating report programs for card-oriented systems. Sections of the user's own coding in PAL symbolic language can be included.

- REGENT TAPE: Generates report programs for tape-oriented systems. Sections of the user's own coding in PAL symbolic language can be included.

- UNIVAC 1050 SORT Routine: Performs tape sorting operations, using decimal, binary, or alphanumeric keys, on a system with 3 to 6 magnetic tape units. The Sort routine can be used with as little as 8,192 core storage positions, but additional storage will increase its efficiency. Sections of the user's own coding can be incorporated.

- COORDINATOR: An executive routine for the UNIVAC 1050, which provides the linkages between the "worker program" and routines from the PAL Library. COORDINATOR can be modified to control data communications devices. One version of COORDINATOR provides for the loading and execution of two programs in parallel, on a time-shared basis.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Character:	6 data bits + parity bit	basic addressable storage unit; holds 1 letter, numeral, special character, or 6 binary bits.
Row (Uniservo IIIA):	9 bits (See section 777:091)	holds 1 character per row or 4 characters per 3 rows (+1 sign and 2 parity bits).
Row (Uniservo IV C and VI C):	7 bits (6 data, 1 parity)	holds 1 character in IBM-compatible format.
Row (punched tape):	5 to 8 bits	holds 1 character.
Column:	12 positions	punched cards; holds 1 character in standard format or 2 characters in column binary format.
Line:	64 or 128 characters	high-speed printer line of print.
Sector:	168 characters	Fastrand addressable storage unit.
Block:	1 to 4,096 characters (Model III) 1 to 8,192 characters (Model IV)	magnetic or punched tape.

.2 INFORMATION FORMATS

Type of Information	Representation
Numeral:	1 character.
Letter or special symbol:	1 character.
Instruction:	5 characters (30 bits).
Character field:	usually 1 to 16 characters.
Binary field:	usually 6 to 96 bits.

SYSTEM CONFIGURATION

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Every UNIVAC 1050 EDP system includes the following units:

- Central Processor — Model III or Model IV.
- Console — Integrated or Free-Standing.
- Core Memory — Model III has 4,096 characters in the basic system, expandable to 32,768 characters in modules of 4,096 characters: Model IV has 8,192 characters in the basic system, expandable to 65,536 characters in modules of 8,192 characters.

The peripheral subsystems available for the UNIVAC 1050 include the following:

- Card Reader — Type 0706-00 or 0706-04 (800/900 cpm, 80 or 90 column) or Type 0706-01 or 0706-05 (600 cpm, 80 or 90 column).
- Card Punch — Type 0600-00 or 0600-01 (300 cpm, 80 or 90 column) or Type 0600-12 or 0600-13 (200 cpm, 80 or 90 column).
- Printer — Type 0755-01 (700/922 lpm) or Type 0755-02 (600/750 lpm).
- Uniservo III A Magnetic Tape Subsystem — consists of a synchronizer, a power supply, and 1 to 6 tape handlers.
- Uniservo IV C Magnetic Tape Subsystem — consists of a synchronizer, a power supply, and 1 to 6 tape handlers.
- Uniservo VI C Magnetic Tape Subsystem — consists of a synchronizer, 1 to 4 control units, and 1 to 16 tape handlers (maximum of 4 tape handlers per control).
- Fastrand I or II Mass Storage Subsystem — consists of a synchronizer and 1 to 8 Fastrand I or II drum units.
- UNIVAC 1004 Subsystem — consists of a 1004 Adapter and a UNIVAC 1004 Model I, II, or III.
- Punched Paper Tape Subsystem — Type 0903-00 (1000 char/sec read and 110 char/sec punch) or Type 0903-01 (300 char/sec read and 110 char/sec punch).
- Standard Communication Subsystem — consists of a Communications Multiplexer (4, 8, 16, 32, or 64 positions) and 1 to 64 Communication Line Terminals.

Each peripheral subsystem requires the exclusive use of one input-output channel, except the Magnetic Tape Subsystems, which require two channels each. Only one type of Magnetic Tape Subsystem is normally allowed in any one UNIVAC 1050 system.

The 1050 Processor supplies power for the card reader, card punch, printer, and one other peripheral subsystem. If additional subsystems are added, a "B" Power Supply must also be added.

The Model IV Central Processor has eight input-output channels available, all optional. The peripheral subsystems can be connected in any combination, subject to the restrictions mentioned above.

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Of the eight input-output channels available (3 standard, 5 optional) on the Model III Central Processor, three channels are reserved for a card reader, a card punch, and a printer, and two channels are reserved for one Magnetic Tape Subsystem. Any peripheral subsystems may be connected to the three remaining channels, but if a second card reader, card punch, or printer is added, a separate synchronizer is required. A second printer and its sychronizer are a standard option.

For marketing purposes, UNIVAC has labeled various combinations of UNIVAC 1050 peripherals as follows:

UNIVAC 1050-C: Card processing system

UNIVAC 1050-T: Tape system

UNIVAC 1050-M: Mass storage system

UNIVAC 1050-R: Real-time system

UNIVAC 1050-S: Satellite system

UNIVAC 1050-4: System using UNIVAC 1004 on-line

Table I shows the configurations of the above systems and the standard software provided for each type of system.

TABLE I: STANDARD UNIVAC 1050 SYSTEM CONFIGURATIONS AND SOFTWARE

	ITEM	UNIVAC 1050-C					UNIVAC 1050-T						UNIVAC 1050-M[2] ALL OF C & T SOFTWARE PLUS	UNIVAC 1050-R[2] ALL OF C, T, M SOFTWARE PLUS	UNIVAC 1050-S							UNIVAC 1050-4	
		4K[3]	4K[3]	8K	8K	8K	8K	8K	8K	8K	8K	16K	12K REQUIRED	12K REQUIRED	8K	8K	8K	8K	8K	8K	8K	4K[3]	8K
EQUIPMENT	UNIVAC 1050 PROCESSOR																						
	600 OR 800/900 CPM READER	1	1	1	1	1	1	1	1	1	1	1	REQUIRED	REQUIRED	1	1	1	1	1	1	1		1
	200 OR 300 CPM PUNCH	1	1	1	1	1	1	1	1	0	1	1			0	1	0	1	0	1	1		1
	600/750 OR 700/922 LPM PRINTER	1	1	1	1	1	1	1	1	1	1	1	REQUIRED	REQUIRED	1	1	1	1	2	2	1		1
	PRINT BUFFER (NOTE 4)		1		1	1	1	1	1	1	1	1	REQUIRED	REQUIRED	1	1	1	1	2	2	1		1
	PAPER TAPE READ/PUNCH UNIT					1					1										1		1
	1004 ON LINE																					1	1
	TAPE UNITS						1	2	3+	3+	3+	4+			1	1	2	2	2	2	2		3+
	MASS MEMORY												1 TO 8										
	COMMUNICATIONS													REQUIRED									
	SOFTWARE PROVIDED																						
ASSEMBLERS	PAL JR*	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
	PAL CARD*			✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
	PAL TAPE							✓	✓	✓	✓	✓						✓		✓	✓		✓
	PAL DRUM												✓										
	PAL 1004*																					✓	✓
	PATCH ASSEMBLER			✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
CONTROL ROUTINES	READER	✓	✓	✓*	✓*	✓*	✓	✓**	✓**	✓**	✓**	✓**				✓		✓**		✓**	✓**		✓**
	PUNCH	✓	✓	✓*	✓*	✓*	✓	✓**	✓**		✓**	✓**				✓		✓**		✓**	✓**		✓**
	PRINTER	✓	✓	✓*	✓*	✓*	✓	✓**	✓**	✓**	✓**	✓**				✓		✓**		✓**	✓**		✓**
	PAPER TAPE					✓					✓**										✓**		✓**
	1004 PERIPHERALS																					✓	✓**
	MAGNETIC TAPE FILES							✓**	✓**	✓**	✓**	✓**						✓**		✓**	✓**		✓**
	DRUM—MASS MEMORY												✓										
	MEMORY DUMP	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
OPERATING SYSTEM	COORDINATOR						✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓		✓
	LOADER	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
	TAPE CONTROL						✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓		✓
	DRUM CONTROL												✓										
	COMMUNICATIONS CONTROL													✓									
	LIBRARIAN							✓	✓	✓	✓	✓					✓	✓	✓		✓		✓
REPORT GENERATORS	REGENT—CARD			✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
	REGENT—TAPE							✓	✓	✓	✓	✓						✓		✓	✓		✓
	REGENT—DRUM												✓										
SORTS	DRUM—SORT												✓										
	TAPE—SORT								✓	✓[1]	✓	✓											✓
	TAPE—MERGE								✓	✓	✓	✓											✓
SATELLITE UTILITIES	CARD → TAPE														✓	✓	✓	✓	✓	✓	✓		
	TAPE → CARD															✓		✓		✓	✓		
	TAPE → PRINT														✓	✓	✓	✓	✓	✓	✓		
COMPILERS	COBOL											✓											
	FORTRAN											✓											

*SPECIALIZER I/O CONTROL **OFF LIBRARY TAPE [1]3—6 TAPES REQUIRED [2]DEPENDING ON CONFIGURATION OF C, T OR M SYSTEMS [3]8K REQUIRED WITH MODEL IV

[4]OPTIONAL FOR 600/750 LPM PRINTER ONLY WITH 600 CPM READER ON 1050-C SYSTEMS

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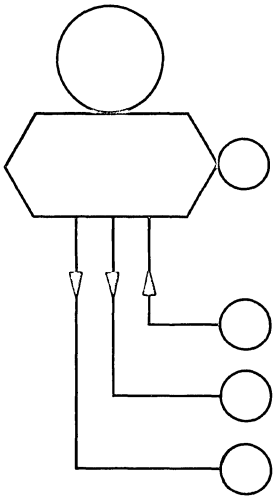
SYSTEM CONFIGURATION

§ 031.

.1 TYPICAL CARD SYSTEM; CONFIGURATION I (UNIVAC 1050-C)

Deviations from Standard Configuration I: . . . . . card reader is 10% to 20% slower.
printer is up to 30% slower.
all peripherals can run simultaneously.
7 index registers instead of 1.

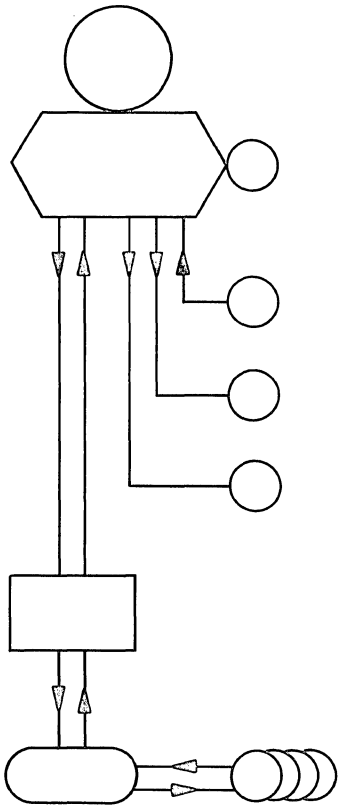


Equipment	Rental
Core Storage: additional 4,096 character positions	$ 325
Model III Central Processor and Integrated Console (with 4,096 characters of Core Storage and 3 input-output channels)	1,230
Card Reader: 800/900 cards/min	380
Card punch: 200 cards/min	400
Printer: 700/922 lines/min (includes Print Buffer)	985
Optional Features Included: . . . . . Multiply-Divide	150
TOTAL RENTAL:	$3,470

§ 031.

.2 4-TAPE BUSINESS SYSTEM; CONFIGURATION II (UNIVAC 1050-T)

Deviations from Standard Configuration II: . . . . . card reader is 20% faster.
card punch is 100% faster.
printer is at least 20% faster.
magnetic tape is up to 130% faster.
7 index registers.
ability to read and write magnetic tape simultaneously is standard.

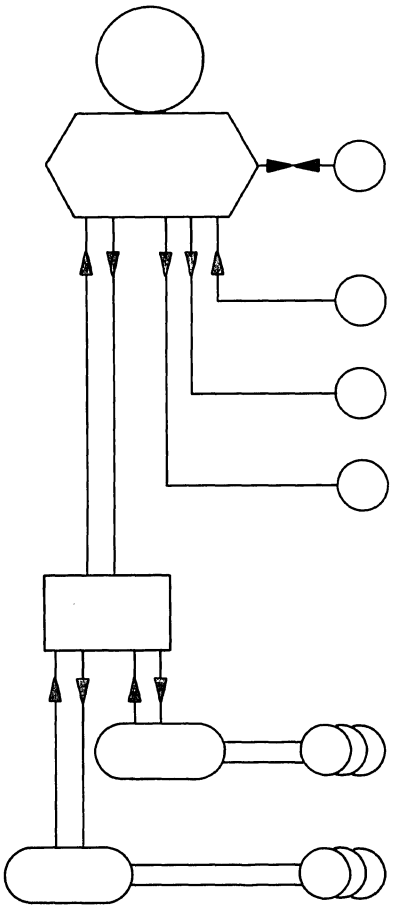


Equipment	Rental
Core Storage: additional 4,096 character positions	$ 325
Model III Central Processor and Integrated Console (with 4,096 characters of Core Storage and 3 input-output channels)	1,230
Card Reader: 600 cards/min	225
Card Punch: 200 cards/min	400
Printer: 600/750 lines/min (includes Print Buffer)	760
Uniservo VI C Synchronizer	600
Uniservo VI C Control and 4 tape drives: up to 34,100 char/sec	1,400
Optional Features Included: . . . . . Input-Output Channels (2)	90
TOTAL RENTAL:	$5,030

§ 031.

.3 6-TAPE BUSINESS SYSTEM: CONFIGURATION III (MODEL III CENTRAL PROCESSOR: UNIVAC 1050-T)

Deviations from Standard Configuration III: . . . . . card reader is 20% faster.
card punch is 100% faster.
printer is at least 20% faster.
7 index registers instead of 3.
console typewriter is not included.
ability to read and write magnetic tape simultaneously is standard.



Equipment	Rental
Core Storage: additional 12,288 character positions	$ 975
Model III Central Processor and Free-Standing Console (with 4,096 characters of Core Storage and 3 input-output channels)	1,260
Card Reader: 600 cards/min	225
Card Punch: 200 cards/min	400
Printer: 600/750 lines/min (includes Print Buffer)	760
Uniservo VI C Synchronizer	600
2 Uniservo VI C Controls and 6 tape drives: up to 34,100 char/sec	2,200

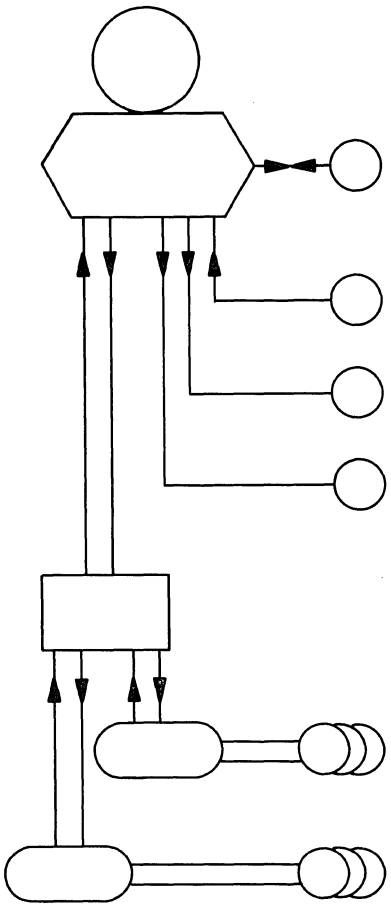
Optional Features Included: . . . . . Input-Output Channels (2) 90
Multiply-Divide 150

TOTAL RENTAL: $6,660

§ 031.

.4 6-TAPE BUSINESS SYSTEM; CONFIGURATION III-A (MODEL IV CENTRAL PROCESSOR; UNIVAC 1050-T)

Deviations from Standard Configuration III: . . . . . card reader is 20% faster.
card punch is 100% faster.
printer is at least 20% faster.
7 index registers instead of 3.
console typewriter is not included.
ability to read and write magnetic tape simultaneously is standard.



Equipment	Rental
Core Storage: additional 8,192 character positions	$ 685
Model IV Central Processor and Free-Standing Console (with 8,192 characters of Core Storage)	2,460
Card Reader: 600 cards/min	225
Card Punch: 200 cards/min	400
Printer: 600/750 lines/min (includes Print Buffer)	760
Uniservo VI C Synchronizer	600
2 Uniservo VI C Controls and 6 tape drives: up to 34,100 char/sec	2,200

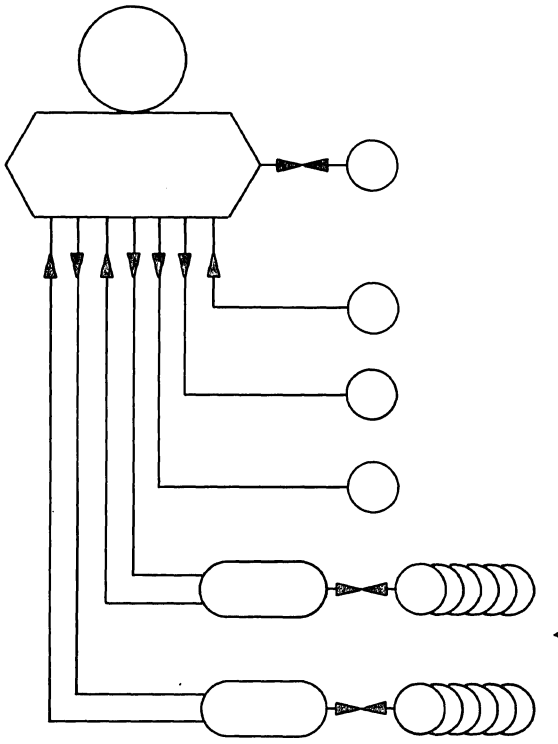
Optional Features Included: . . . . . Input-Output Channels (5) 425
Multiply-Divide 275

TOTAL RENTAL: $8,030

§ 031.

.5 12-TAPE BUSINESS SYSTEM; CONFIGURATION IV (UNIVAC 1050-T)

Deviations from Standard Configuration IV: . . . . . card reader is 20% slower.
printer is up to 30% slower.
magnetic tape is up to 120% faster.
3 fewer index registers.
console typewriter is not included.
only 1 magnetic tape data transfer at a time is possible.

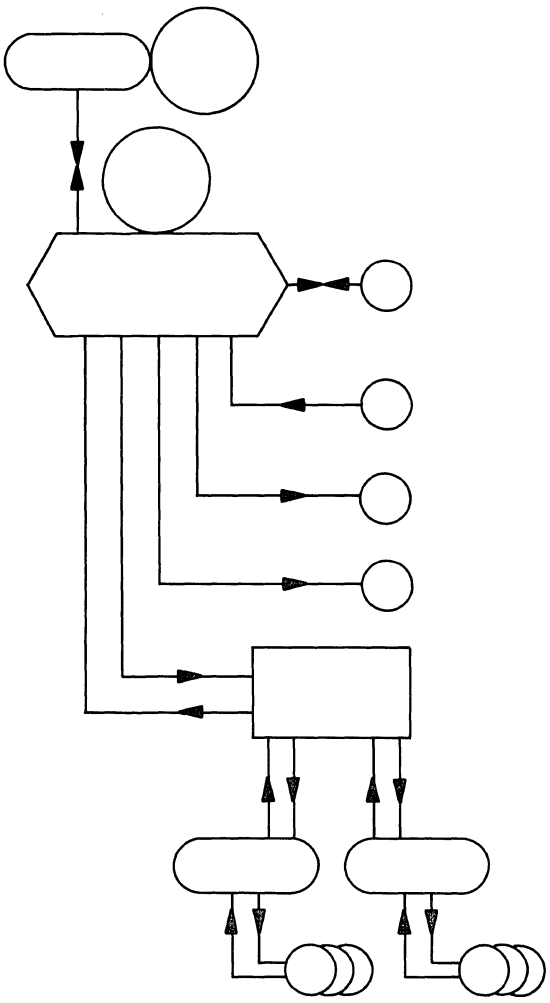


Equipment	Rental
Core Storage: additional 24,576 character positions	$ 2,055
Model IV Central Processor, Free-Standing Console, and "B" Power Supply (with 8,192 characters of Core Storage)	2,610
Card Reader: 800/900 cards/min	380
Card Punch: 200 cards/min	400
Printer: 700/922 lines/min (includes Print Buffer)	985
Uniservo III A Synchronizer (2)	1,990
Uniservo III A Power Supply (2)	430
Uniservo III A Tape Drives (12): 100,000 rows/sec	9,000
Optional Features Included: . . . . . Input-Output Channels (7)	595
Multiply-Divide	275
TOTAL RENTAL:	$18,720

§ 031.

.6 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V (UNIVAC 1050-M)

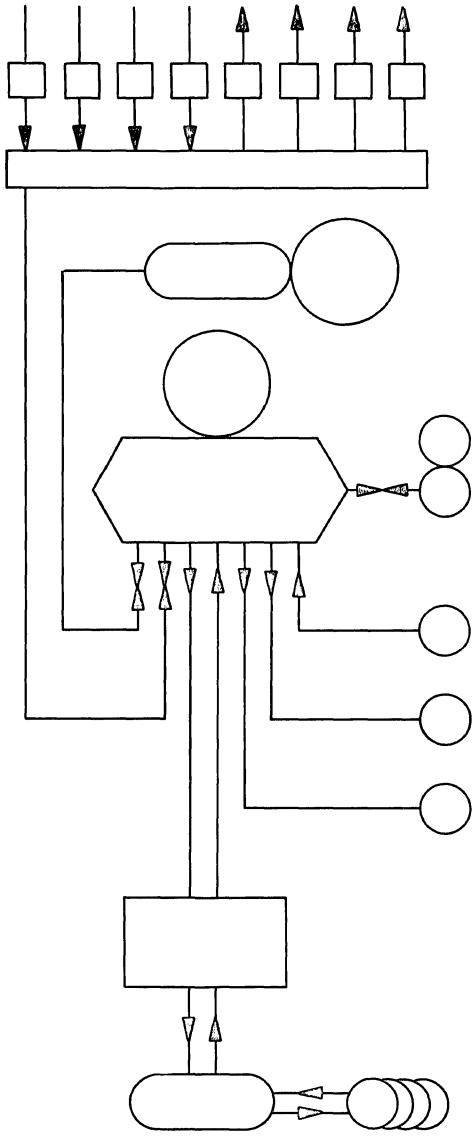
Deviations from Standard Configuration V: . . . . . auxiliary storage is 230% larger.
card reader is 20% faster.
card punch is 100% faster.
printer is at least 20% faster.
console typewriter is not included.
7 index registers instead of 3.
ability to read and write magnetic tape simultaneously is standard.



Equipment	Rental
Fastrand I Storage Unit and Synchronizer: 66,050,288 characters	$ 4,295
Core Storage: additional 8,192 character positions	685
Model IV Central Processor, Free-Standing Console, and "B" Power Supply (includes 8,192 characters of Core Storage)	2,610
Card Reader: 600 cards/min	225
Card Punch: 200 cards/min	400
Printer: 600/750 lines/min (includes Print Buffer)	760
Uniservo VI C Synchronizer	600
2 Uniservo VI C Controls and 6 tape drives: up to 34,100 char/sec	2,200
Optional Features Included: . . . . . Input-Output Channels (6)	510
Multiply-Divide	275
TOTAL RENTAL:	$12,500

§ 031.

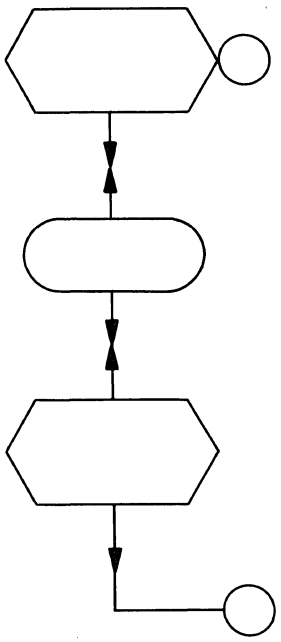
.7 TYPICAL REAL-TIME SYSTEM (UNIVAC 1050-R)



Equipment	Rental
CLT51L (2): up to 300 bits/sec input; 5 level	$ 40
CLT50L (2): up to 300 bits/sec output; 5 level	50
CLT81M (2): up to 1600 bits/sec input; 5, 6, 7, or 8 level	50
CLT80M (2): up to 1600 bits/sec output; 5, 6, 7, or 8 level	70
C/M-8 Communications Multiplexer: 8 positions	725
Fastrand I Storage Unit and Synchronizer: 66,050,288 characters	4,295
Core Storage: additional 12,288 character positions	975
Console Typewriter: 10 char/sec	165
Model III Central Processor, Free-Standing Console and "B" Power Supply (includes 4,096 characters of Core Storage and 3 input-output channels)	1,410
Card Reader: 600 cards/min	225
Card Punch: 200 cards/min	400
Printer: 700 lines/min (includes Print Buffer)	985
Uniservo VI C Synchronizer	600
Uniservo VI C Control and 4 tape drives: up to 34,100 char/sec	1,400
Optional Features Included: . . . . . Input-Output Channels (4)	180
Multiply-Divide	150
TOTAL RENTAL:	$11,720

§ 031.

.8 TYPICAL ON-LINE CARD PROCESSING SYSTEM (UNIVAC 1050-4)



Equipment	Rental
UNIVAC 1050 Model III and Integrated Console (with 4,096 character positions of Core Storage and 3 input-output channels)	$1,230
UNIVAC 1004 Adapter	200
UNIVAC 1004 Model I, including 961 positions of Core Storage, 400 cards/min Reader, and 400 lines/min Printer	1,150
Card Punch: 200 cards/min	300
TOTAL RENTAL:	$2,880

INTERNAL STORAGE: CORE STORAGE – MODEL III

§ 041.

.1 GENERAL

.11 Identity: . . . . . Core Storage.
Main Memory of the 1050 Model III Central Processor.
Additional Memory Module of 4,096 characters.

.12 Basic Use: . . . . . working storage.

.13 Description

The basic 1050 Model III Central Processor contains 4,096 character positions of core storage. Additional storage is obtained by adding from one to seven modules of 4,096 positions each, providing a maximum capacity of 32,768 character positions. Cycle time is 4.5 microseconds for each access of one alphanumeric character. Each character position consists of 7 bits: 6 data bits and 1 parity bit.

Core storage is used for all input-output areas, index registers, arithmetic registers, input-output control storage, and interrupt control storage. Any locations in core storage can be used as input-output areas, with the restriction that the address of every card read or card punch area must be a multiple of 64.

A total of from 161 to 289 character positions of the basic 4K block of storage are reserved for special purposes, depending upon the optional features installed. Although all reserved areas may be used as working storage, a programmer would be well-advised to refrain from using the first 340 positions of core storage for any purpose other than those described above (except tetrads 22 through 31, which have no special assignments).

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . 1963.

.16 Reserved Storage

Purpose	Number of locations	Locks
Index registers:	7 registers of 3 characters each	none.
Arithmetic registers:	2 registers of 16 characters each	none.
I-O control registers:	16 characters per channel	none.
Interrupt control registers:	16 characters, plus 8 characters per I/O channel	none.
Multiplier-Quotient (if multiply-divide feature is incorporated):	8 characters	none.
Control counter storage:	4 characters	none.
Special instructions:	16 characters	none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic cores.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . no.

.28 Access Techniques

.281 Recording method: . . coincident current.
.283 Type of access: . . . uniform.

.29 Potential Transfer Rates

.292 Peak data rates —
Cycling rates: . . . 222,222 cps.
Unit of data: . . . . character.
Conversion factor: . 6 data bits/character.
Data rate: . . . . . 222,222 char/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	2nd to 8th Increment	Maximum Storage
Identity:	in basic processor	additional 4K module	-
Words:	variable	variable	variable.
Characters:	4,096	4,096	32,768.
Instructions:	819	819	6,553.
Decimal digits:	4,096	4,096	32,768.
Modules:	1	1	8.

§ 041.

.32 Rules for Combining Modules: . . . . . from 1 to 8 modules per system may be used.

.4 CONTROLLER . . . . control unit is part of Model III Central Processor.

.5 ACCESS TIMING

.52 Simultaneous Operations: . . . . . none.

.53 Access Time Parameters and Variations

.531 For uniform access —
Access time: . . . . 2.25 μsec.
Cycle time: . . . . . 4.50 μsec.
For data unit of: . . . 1 character.

.7 PERFORMANCE

.72 Transfer Load Size

With self: . . . . . 1 to 1,024 characters.

.73 Effective Transfer Rate

With self: . . . . . 90 + 9C μsec, where C is the number of characters transferred, using block transfer instruction.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	generates interrupt signal and sets testable indicator.
Invalid code:	none.	
Receipt of data:	parity check	generates interrupt signal and sets testable indicator.
Recording of data:	record parity bit.	
Recovery of data:	parity check	generates interrupt signal and sets testable indicator.
Dispatch of data:	send parity bit.	
Timing conflicts:	check	generates interrupt signal.

INTERNAL STORAGE: CORE STORAGE – MODEL IV

§ 042.

.1 GENERAL

.11 Identity: . . . . . Core Storage.
Main Memory of the 1050 Model IV Central Processor.
Additional Memory Module of 8,192 characters.

.12 Basic Use: . . . . . Working storage.

.13 Description

The basic 1050 Model IV Central Processor contains 8,192 character positions of core storage. Additional storage is obtained by adding from one to seven modules of 8,192 positions each, providing a maximum capacity of 65,536 character positions. Each position consists of 7 bits: 6 data bits and 1 parity bit.

Memory is accessed two characters at a time, with a cycle time of 2 microseconds per access. Internal circuitry handles the selection of the relevant characters when accessing an operand with an odd number of characters or an instruction. Effective cycle time is 1.2 microseconds per character or less when accessing operands 5 or more characters in length.

Core storage is used for all input-output areas, index registers, arithmetic registers, input-output control storage, and interrupt control storage. Any locations in core storage can be used as input-output areas, with the restriction that the address of every card read or card punch area must be a multiple of 64.

A total of from 161 to 289 character positions of the basic 8K block of storage are reserved for special purposes, depending upon the optional features installed. Although all reserved areas may be used as working storage, a programmer would be well-advised to refrain from using the first 340 positions of core storage for any purpose other than those described above (except tetrads 22 through 31, which have no special assignments).

.15 First Delivery: . . . . . December 1965.

.16 Reserved Storage

Purpose	Number of locations	Locks
Index registers:	7 registers of 3 characters each	none.
Arithmetic registers:	2 registers of 16 characters each	none.
I-O control registers:	16 characters per channel	none.
Interrupt control registers:	16 characters, plus 8 characters per I-O channel	none.
Multiplier-Quotient (if multiply-divide feature is incorporated):	8 characters	none.
Control counter storage:	4 characters	none.
For special instructions:	16 characters	none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic cores.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent:. . . . . no.
.245 Storage changeable: . . no.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.283 Type of access: . . . . . uniform.

.29 Potential Transfer Rates

.292 Peak data rates —
Cycling rates: . . . . . 500,000 cps.
Unit of data: . . . . . 2 characters.
Conversion factor: . . 6 data bits/character.
Data rate: . . . . . 1,000,000 char/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	2nd to 8th Increment	Maximum Storage
Identity:	in basic processor	additional 8K module	—
Words:	variable	variable	variable.
Characters:	8,192	8,192	65,536.
Instructions	1,638	1,638	13,107.
Decimal digits:	8,192	8,192	65,536.
Modules:	1	1	8.

§ 042.

.32 Rules for Combining Modules:. . . . . from 1 to 8 modules per system may be used.

.4 CONTROLLER . . . . . control unit is part of Model IV Central Processor.

.5 ACCESS TIMING

.52 Simultaneous Operations:. . . . . none.

.53 Access Time Parameters and Variations

.531 For uniform access —
Access time:. . . . . 1 μsec.
Cycle time:. . . . . 2 μsec.
For data unit of:. . . . . 2 characters per cycle.

.7 PERFORMANCE

.72 Transfer Load Size

With self: . . . . . 1 to 1,024 characters.

.73 Effective Transfer Rate

With self: . . . . . 34 + 2C μsec, where C is the number of characters transferred, using block transfer instruction.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	generates interrupt signal and sets testable indicator.
Invalid code:	none.	
Receipt of data:	parity check	generates interrupt signal and sets testable indicator.
Recording of data:	record parity bit.	
Recovery of data:	parity check	generates interrupt signal and sets testable indicator.
Dispatch of data:	send parity bit.	
Timing conflicts:	check	generates interrupt signal.

INTERNAL STORAGE: FASTRAND I AND II

§ 043.

.1 GENERAL

.11 Identity: . . . . . Fastrand I and II Mass Storage Subsystems.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The UNIVAC 1050 Fastrand Mass Storage Subsystem is basically the same as Fastrand for the UNIVAC 490, with certain changes to permit operation with the 1050's character-type data structure and testable indicator-type control system. The subsystem provides fairly rapid random access to large quantities of data stored on magnetic drums.

Two versions of the Fastrand Storage Unit are available. Fastrand II has twice the number of tracks per drum as Fastrand I. There is no difference in physical size or other characteristics. Each Fastrand I Storage Unit has a capacity of over 66 million characters; each Fastrand II Storage Unit, over 132 million characters. From one to eight storage units can be connected to a Fastrand Control and Synchronizer Unit to comprise a Fastrand Subsystem. One subsystem can be connected to each unassigned input-output channel (up to 3 for the 1050 Model III and 8 for the Model IV). Maximum storage capacity, therefore, ranges from 1.585 billion characters for systems incorporating the Model III Central Processor and Fastrand I, to 8.454 billion characters for those using the Model IV Central Processor and Fastrand II.

Average random access time to any record is 93 milliseconds. Peak transfer rate, when the data to be transferred is contained in several sectors of the same track, is 154,000 characters per second. Peak transfer rate within a sector is 185,000 characters per second.

An option called Fastbands can be added to either type of Fastrand Storage Unit. It adds 24 tracks (258,048 characters) with 1 fixed head per track. The access time to records contained on these tracks depends only on rotational delay and averages 35 milliseconds per random access of a record.

Each Fastrand Storage Unit contains two magnetic drums, which are treated as a single logical unit by the controller. There are 64 aerodynamically-supported read/write heads per storage unit (32 per drum). All 64 heads are connected to a common positioning mechanism and move in unison to one of 96 discrete positions in Fastrand I or to one of 192 positions in Fastrand II.

.13 Description (Contd.)

The tracks available at each position are numbered sequentially, enabling up to 688,128 characters of data to be read or recorded without repositioning the heads. (This is analogous to the "cylinder" concept in IBM 1301 and 1311 Disk Storage.) From one character to the limit of core storage can be transferred with a single instruction.

Head positioning time varies from 30 to 86 milliseconds and averages 58 milliseconds. Drum speed is 870 revolutions per minute, so the rotational delay varies from 0 to 69 milliseconds and averages 35 milliseconds. Activation of addressing circuits requires 5 milliseconds, but this is usually overlapped with the other access time factors.

Each of the two drums in a Fastrand I Storage Unit has 3,072 data tracks, while each Fastrand II drum has 6,144 data tracks. Each track is divided into 64 sectors, and each sector holds 168 characters.

The Search feature allows an operand to be compared with the first 8, 16, or 32 characters (key) of each sector within the 64 tracks at a particular position of the heads. The key is compared bit by bit with the whole operand, or only with the particular bit positions indicated by a mask. The operand to be compared is stored in core storage, and no demand on the central processor is made except during the actual comparisons. When a "find" is made, an interrupt signal is generated (optional) and a testable indicator is set. Searching may be for an equality condition or for an equal to or greater than condition.

Parity check bits and phase-monitoring circuits are used for error detection and correction, providing for the recovery of up to 11 bits of missed data. (The technique used for error recovery is considered proprietary information.) Other checks are made for invalid addresses, illegal function codes, timing conflicts, and sector length errors. Detection of any error causes the controller to generate an interrupt signal and set a particular testable indicator, depending upon the type of error.

Average times available for processing during a Fastrand operation are shown in the table on the following page.

In UNIVAC 1050 systems using the Model III Central Processor, the Fastrand unit can operate simultaneously with the Communications Subsystem, Punched Paper Tape Subsystem, Buffered Printer, and the UNIVAC 1004 Subsystem on-line. In systems using the Model IV Central Processor, the Fastrand unit can operate simultaneously with all peripheral subsystems except the Uniservo III A, the Uniservo IV C, or another Fastrand Subsystem.

§ 043.

.13 Description (contd.)

TABLE I: AVERAGE PROCESSING TIME AVAILABLE DURING A ONE-SECTOR FASTRAND READ OR WRITE OPERATION

	Model III Processor	Model IV Processor
Average time to access and read or write a sector	93 msec	93 msec
Memory interlock	0.97%	0.54%
Software execution*	2.69%	0.65%
Available for processing	96.32%	98.81%

*Includes execution of instruction and all necessary control functions, such as handling the interrupt generated upon successful completion of an operation.

.14 Availability: . . . . . immediate.

.15 First Delivery: . . . . . 2nd quarter, 1964.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drums.

.22 Physical Dimensions

.222 Drum —
Diameter: . . . . . 23.8 inches.
Length: . . . . . 61.2 inches, effective.
Number on shaft: . . . 1.
Number per Storage Unit: . . . . 2.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 1 Track

Characters: . . . . . 10,752.
Digits: . . . . . 10,752.
Instructions: . . . . . 2,150.
Sectors: . . . . . 64 (168 characters each).
Address tags: . . . . . 1 (48 bits).

.26 Bands per Physical Unit

Fastrand I: . . . . . 3,072 per drum.
6,144 per Storage Unit.
Fastrand II: . . . . . 6,144 per drum.
12,288 per Storage Unit.

.27 Interleaving Levels: . . no interleaving.

.28 Access Techniques

.281 Recording method: . . . 64 moving heads per Storage Unit, connected to a common positioning mechanism.

.283 Type of access —

Description of stage	Possible starting stage
Move heads to specified position:	when a different position is selected.
Wait for specified sector:	when previously selected position is used.
Read or write:	when rotational delay is used.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 870 rpm.
Track/head speed: . . 1,086 inches/sec.
Bits/inch/track: . . . 1,000.
Bit rate per track: . . 1,086,000 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . character.
Conversion factor: . . 6 data bits plus parity bit per character.
Gain factor: . . . . . 1 track per band.
Data rate —
Within a sector: . . . 185,000 char/sec.
Within a track: . . . . 153,846 char/sec.

§ 043.

.3 DATA CAPACITY

.31 Module and System Sizes

FASTRAND I	Minimum Storage	Maximum per Subsystem	Maximum Storage (Model III)	Maximum Storage (Model IV)
Subsystems:	1	1	3	8
Storage Units:	1	8	24	64
Drums:	2	16	48	128
Characters:	66,050,288	528×10^6	$1,585 \times 10^6$	$4,227 \times 10^6$
Instructions:	13,210,057	105×10^6	317×10^6	845×10^6
Sectors:	393,216	3,145,728	9,437,184	25,165,784

FASTRAND II	Minimum Storage	Maximum per Subsystem	Maximum Storage (Model III)	Maximum Storage (Model IV)
Subsystems:	1	1	3	8
Storage Units:	1	8	24	64
Drums:	2	16	48	128
Characters:	132,100,576	$1,056 \times 10^6$	$3,170 \times 10^6$	$8,454 \times 10^6$
Instructions:	26,420,114	210×10^6	634×10^6	$1,690 \times 10^6$
Sectors:	786,432	6,291,456	18,874,368	50,331,568

.32 Rules for Combining Modules: . . . . . 1 to 8 Storage Units per Fastrand Subsystem; 1 to 3 subsystems per UNIVAC 1050 Model III system; 1 to 8 subsystems per UNIVAC 1050 Model IV system.

.4 CONTROLLER

.41 Identity: . . . . . Fastrand Control and Synchronizer, Type 5002-02.

.42 Connection to System

.421 On-line: . . . . . 1 to 3 controllers per Model III system; 1 to 8 controllers per Model IV system; 1 per Fastrand Subsystem.

.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1 to 8 Fastrand Storage Units.

.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N characters, beginning with the first character of a drum sector, where N is limited only by core storage capacity.

.442 Input-output area: . . . core storage.

.443 Input-output area access: . . . . . each character.

.444 Input-output area lockout: . . . . . none.

.445 Synchronization: . . . . automatic.

.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —
Stacks per Fastrand Subsystem: . . . . . 64 to 512.
Stacks per storage unit: . . . . . 64.
Stacks per drum: . . . 32.
Stacks per yoke: . . . 64.
Yokes per storage unit: . . . . . 1.

.512 Stack movement: . . . . all 64 stacks in a Storage Unit move in unison, to 1 of 96 or 192 discrete positions, depending on the type.

.513 Stacks that can access any particular location: . . . . . 1.

.514 Accessible locations
By single stack —
With no movement: . 64 sectors.
With all movement: . 6,144 or 12,288 sectors.
By all stacks —
With no movement: . 4,096 sectors per storage unit.
up to 32,768 sectors per subsystem.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer or search operation per Fastrand Subsystem, and 1 head-positioning operation per Fastrand Storage Unit.

§ 043.

.53 Access Time Parameters and Variations

.532 Variation in access time

Stage	Variation, μsec	Average, μsec
Activate addressing circuits:	5,000*	*
Position heads:	0 or 30,000 to 86,000	58,000.
Wait for specified sector:	0 to 69,000	35,000.
Read or write:	see Para. .292	-
Total:	5,000 to 155,000	93,000.

*Usually overlapped with other timing factors.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to N characters, beginning with the first character of a drum sector, where N is limited only by core storage capacity.

.73 Effective Transfer Rate

With core storage —
Within a sector: . . . . 185,00 char/sec.
Within a track: . . . . 153,846 char/sec.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity bit and phase monitoring	interrupt.
Timing conflicts:	check	interrupt.
Physical record missing:	check	interrupt.
Reference to locked area:	check	interrupt.
Sector length error:	check	interrupt.
End of position reached:	check	interrupt.

Note: The type of error is indicated by the settings of particular testable indicators.

CENTRAL PROCESSOR – MODEL III

§ 051.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1050 Model III Processor.

.12 Description:

The Model III Central Processor is primarily character oriented, with some capabilities for processing pure binary operands. Core storage (from 4,096 to 32,767 character positions, in modules of 4,096 positions) is completely character addressable, with addressing in pure binary form rather than decimal. It features fixed-point decimal arithmetic (multiply-divide feature optional), automatic translation of 6-bit codes, good editing facilities, and three levels of interrupts.

The first 256 positions of core storage are divided into 64 fields of 4 characters each, called "tetrads", all of which are addressable either by tetrad or by character. Contained in this area are the two addressable arithmetic registers (16 characters each) and the seven addressable index registers (the 15 low-order bits of tetrads 9-15). Address indexing is specified in a three-bit field within the instruction. There is no provision for indirect addressing.

A 30-bit (5-character), single-address instruction format is used. The operation code and detail field of the instruction specify the location of the second field if any is required by the instruction. In the binary mode, operand lengths are specified in the instruction. In the decimal mode, the length of one operand is specified in the instruction, and the other by a sentinel in the arithmetic register. This sentinel (the character "&") is automatically inserted immediately to the left of the operand when an arithmetic register is loaded in the decimal mode. This sentinel is the only "word-mark" device used in the 1050, and it is not transmitted when storing the contents of one of the arithmetic registers. If a full 16-character operand is used in the arithmetic register, the sentinel is implied; conversely, if the sentinel does not appear, a full 16-character operand is implied in decimal operations.

Facilities for the use of literals (operands contained in the instruction rather than in storage) include the binary addition of one character to any location, storage of one character, comparison of one character, testing of selected bits of a character (logical compare), storing of a 15-bit field in the low-order positions of a tetrad (which can be an index register), and the very useful ability to increment or decrement an index register or any other tetrad by a 15-bit literal field. In addition, one-character Boolean operations (inclusive OR and logical AND) are provided, in which one operand must be a literal.

.12 Description (Contd.)

The incorporation of two additional instructions to the operations permits limited handling of data on the bit level. These are the two "bit shift" instructions:

(1) Bit Shift - shift left 1 to 7 bit positions and fill with zeros on the right; and

(2) Bit Circulate - shift left 1 to 7 bit positions, bringing the high-order bits shifted out around to the low-order positions.

The Bit Circulate instruction effectively provides the ability to shift right. Both instructions deal with an integral number of characters (1 to 4).

Two modes of comparison are provided: decimal and binary. The decimal mode compares two fields algebraically, ignoring zone bits except for the sign bit in the least significant character. A bit-by-bit comparison of two equal-length operands is made in the binary mode. The results of both are stored in four program-testable indicators (high, low, equal, unequal).

A sophisticated system of testable indicators is provided, permitting, for one thing, the use of comparison results (high, low, equal, unequal) and arithmetic results (zero result, negative decimal result, decimal overflow, binary overflow) for program control. Utilization of the interrupt system for program control and input-output control is also facilitated by the system of indicators.

Program interrupts are signals to the Central Processor generated upon the recognition of a condition that requires immediate attention. They result from two general types of occurrences:

- Error, fault, or emergency condition in either the Central Processor or in an I/O device;
- Successful completion of an I/O function or, in some cases, readiness of an I/O device to accept an I/O command.

The interrupt signals are divided into a hierarchy of three classes, listed in descending priority:

- Class I — internal parity error;
- Class II - decimal overflow operator request, or memory overload anticipated;
- Class III - I/O condition.

When servicing an interrupt, additional interrupt signals of the same or a lower class are not accepted, but are stored in testable indicators for future action. In addition to this automatic inhibit,

§ 051.

.12 Description (Contd.)

Class II and Class III interrupts may be inhibited or enabled at will by the program, and the Class II interrupt may be manually inhibited by means of a console switch.

Associated with Class I interrupts, Class II interrupts, and each I/O channel is a group of 8 consecutive character positions (an Interrupt Control Register) through which communication with the interrupt routines is maintained. When an interrupt occurs and is not inhibited, the contents of the control counter are stored in one part of the appropriate Interrupt Control Register, and the starting address, located in another part of the Interrupt Control Register, is read into the control counter. At the end of the service routine, control can be returned to the interrupted program by utilizing the previously stored control counter information.

Addition and subtraction are provided in both the decimal and binary modes. In the decimal mode, there are the following considerations:

- One operand is in the arithmetic register; one is in core storage; the result may be programmed to appear in either location.
- The length of the operand in core storage is specified in the instruction.
- The length of the operand in the arithmetic register is specified by the sentinel.
- Except for the sign bit in the least significant character, the zone bits are ignored and do not appear in the result.
- A decimal overflow condition (carry beyond the most significant digit of the result field) terminates the instruction, sets a testable indicator, and initiates a Class II interrupt.
- The four characters (blank, +, @ , ≠) having the internal form XX0000 will be converted to decimal zeros (000011) before the operation.

Binary arithmetic operations facilitate address modification. Use of these facilities for general processing of binary operands is limited by the following considerations:

- No algebraic signs are associated with either operand.
- Binary overflow terminates the instruction and sets a testable indicator but does not initiate any interrupt.

.12 Description (Contd.)

The optional Multiply-Divide Feature provides fixed-point decimal multiply and divide hardware. Subroutines will be provided for installations not electing this option. No floating-point hardware is available for the UNIVAC 1050, but routines will be provided to accomplish floating-point operations with the FORTRAN compiler.

A wide range of editing facilities is provided as standard equipment. For character insertion, the field to be edited is loaded into Arithmetic Register 1, and the characters are inserted according to the contents of a mask which has been previously loaded into Arithmetic Register 2. Any characters may be inserted, subject to one restriction: the final edited field must contain no more than 16 characters. Zero suppression, asterisk fill, or floating dollar sign operations may be carried out on a field anywhere in core storage under the same restriction that the field operated on must contain 16 or fewer characters.

The Translate instruction enables the Processor to translate any 6-bit code to any other 6-bit code. This is necessary on 90-column card systems since 90-column cards are read and punched without automatic translation between the Processor XS-3 code and the card code. Automatic translation is available, at the option of the programmer, for 80-column cards. Fields of up to 64 characters can be translated with a single instruction, at a cost of 13.5 microseconds per character plus an overhead of 36 microseconds per instruction. Up to 63 programmer-constructed translating codes of 64 characters each can be stored at one time.

There are eight input-output data channels available; three are standard and five are optional. Five of the channels have fixed assignments:

Channel 0 — Printer

Channel 1 — Card Reader

Channel 2 — Card Punch

Channel 4 — Tape Read

Channel 5 — Tape Write.

Any other peripheral unit can be connected to any of the remaining three channels, with the provision that two data channels are required for one tape synchronizer. Detailed consideration is given to the handling of data channels and input-output operations in the section on Simultaneous Operations (777:111).

A limited capability for multirunning is provided, using the interrupt system discussed previously. The Coordinator executive routine (discussed in Operating Environment, Section 777:191) handles all the details involved when running two programs concurrently.

.14 First Delivery: . . . . . 1963.

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.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point —			
Add-subtract:	automatic	decimal or binary	16 characters.
Multiply —			
Short:	none.		
Long:	subroutine	decimal	16 character product.
	automatic (with Multiply-Divide feature)	decimal	16 character product.
Divide —			
No remainder:	none.		
Remainder:	subroutine	decimal	?
	automatic (with Multiply-Divide feature)	decimal	8 character quotient.
.212 Floating point:	Subroutine only	decimal	?
.213 Boolean —			
AND:	automatic	binary	1 character.
Inclusive OR:	automatic	binary	1 character.
Exclusive OR:	none.		
.214 Comparison:	sets testable indicators for high, low, equal, unequal.		
Numbers:	automatic	1 to 16 characters.	
Absolute:	none.		
Letters:	automatic	1 to 16 characters.	
Mixed:	automatic	1 to 16 characters.	
Collating sequence:	0-9, A-Z, with special characters interspersed; see Data Code Table, Section 777:141.		

	Provision	From	To	Size
.215 Code translation:	automatic (using code table constructed by programmer)	any code	any code	1 to 64 characters.

.216 Radix conversion: none.

	Provision	Comment	Size
.217 Edit format			
Alter size:	automatic	expand but not contract	the edited field may not exceed 16 characters after insertions.
Suppress zero:	automatic		
Round off:	none		
Insert point:	automatic		
Insert spaces:	automatic		
Insert any character:	automatic		
Float $:	automatic		
Protection:	automatic		

.218 Table look-up:. . . . . none; however, the Fastrand unit provides search capabilities; see Section 777:042.

.219 Others —		
Branch on Manual Sense Switches:	automatic	8 possible settings.
Branch on Internal Sense Switches:	automatic	program set; 8 possible settings.
Bit Shift:	automatic	1 to 4 characters are shifted 1 to 7 bit positions, to left only.

§ 051.

.22 Special Cases of Operands

.221 Negative numbers: . . . absolute value, with a B zone bit in the least significant character.

.222 Zero: . . . . . positive and negative decimal zeros and blanks give the same results in decimal arithmetic operations, but are unequal in comparisons.

.223 Operand size determination: . . . . . for most instructions there is a counter in the instruction. Some instructions imply one character; others, four characters.

.23 Instruction Formats

.231 Instruction structure: . five characters (30 bits).

.232 Instruction layout (see tables below)

.233 Instruction parts —

Name	Purpose
OP:	operation code.
IR:	specifies which index register is to be used; if no indexing is desired, this field should be binary zeros.
M:	specifies address of operand or field.
Detail:	may specify operand length, tetrad number, a comparison indicator, or number of bits, depending upon the particular instruction.
I/O:	always octal 40.
Channel:	channel assignment for I/O device referenced in the Function part of the instruction.
Unit:	specifies which of several of the same type I/O devices is to be used.
Function:	specifies which I/O operation is to be performed, whether or not the central processor is to be locked out during the operation, whether or not to inhibit normal interrupts; or can cause certain indicators to be tested or reset.

.233 Instruction parts (Contd.)

Name	Purpose
D:	specifies which indicator or set of indicators is to be tested or reset when the corresponding Function is given; or controls certain actions such as automatic translate on 80-column system card devices, stacker selection (card punch), half-line print (printer), advance base address, etc.

.234 Basic address structure: . . . . . 1 + 0.

.235 Literals —

Arithmetic:	1 character (binary addition only).
Comparison:	1 character.
Store:	1 character.
Store binary:	15 bits (low-order bits in one of the tetrads).
Boolean operations: .	1 character.
Incrementing or decrementing index registers:	15 bits.

.236 Directly addressed operands —

.2361 Internal storage type:	core.
Minimum size:	1 character.
Maximum size:	16 characters.
Volume accessible: .	total capacity.

.237 Address indexing —

.2371 Number of methods: .	1.
.2372 Name:	indexing.
.2373 Indexing rule:	addition; formation of an address beyond the size of store causes a Class I interrupt to be generated.
.2374 Index specification: . .	bits 25 to 23 in the instruction.
.2375 Number of potential indexers:	7.
.2376 Addresses which can be indexed:	all.
.2377 Cumulative indexing: .	none.
.2378 Combined index and step:	none.

.238 Indirect addressing: . . none.

.239 Stepping —

.2391 Specification of increment:	in stepping instruction.
.2392 Increment sign:	always negative.
.2393 Size of increment: . .	always 1.
.2394 End value:	zero.
.2395 Combined step and test:	yes.

.232 Instruction layout —
General instruction:

Part:	OP	IR	M	Detail
Size (bits):	5	3	16	6

External Function (input-output) instruction:

Part:	I/O	Channel	Unit	Function	D
Size (bits):	5	3	4	6	12

§ 051.

.24 Special Processor Storage

.241 Category of storage:. . control counter.
Number of locations:. . 1.
Size in bits: . . . . . 16.
Program usage:. . . . . holds address of next instruction.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities:. . . 1.
.312 Arrangement: . . . . . in processor.
.314 Special sub-sequence counters: . . . . . the jump loop instruction will cause a loop to be repeated 1 to 62 times based on the value of a literal in the instruction. The literal is automatically decremented by 1 for each repeat, stopping when the value becomes zero.
.315 Sequence control step size: . . . . . 1 instruction (5 characters).

.32 Look-Ahead: . . . . . none.

.33 Interruption

.331 Possible causes —

Class (in decreasing priority)	Possible causes
I:	internal parity errors, except those occurring while I/O devices are accessing main store.
II:	decimal overflow, operator request (manual), or memory overload anticipated.
III:	interrupts generated by the synchronizers associated with the I/O devices upon the occurrence of successful completion, detection of an error or fault condition, issuance of an I/O instruction to a "busy" device, or by a "demand" device (one which generates an interrupt at fixed time intervals whether or not an instruction has been issued to it).

.332 Control by routine —
Individual control: . . each I/O device "successful completion" interrupt individually, all Class III interrupts as a group, decimal overflow interrupts, and operator request interrupts can be inhibited or enabled at will by the program. Class I, Class II, or Class III automatic inhibits can be program enabled.
Method: . . . . . set an indicator bit.
Restriction: . . . . . none.

.333 Operator control:. . . . manual interrupt request is possible.
.334 Interruption conditions:. . . . . (1) current instruction completed (except Class I).
(2) not in the process of transferring control to a routine because of a prior interrupt request.
(3) no higher-priority interrupt requests outstanding. (If a Class I interrupt occurs while processing a prior Class I interrupt, the central processor stalls).

.335 Interruption process —
Disabling interruption: . . . . . automatically inhibits same-priority and lower-priority interrupt requests.
Registers saved: . . . control counter is stored automatically.
Destination: . . . . . automatic branch to address contained in the location appropriate to the interrupt cause.
.336 Control methods —
Determine cause:. . . COORDINATOR or own coding, utilizing testable indicators.
Enable interruption:. . own coding; reset interrupt indicator.
.34 Multirunning: . . . . . limited capability, using automatic priority interrupt feature described above.
.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

D = operand length in decimal digits.
C = operand length in characters.

.41 Instruction Times in Microseconds

.411 Fixed point
Add-subtract —
Decimal add to or subtract from accumulator:. . . . $49.5 + 27D$
Decimal add to or subtract from memory: . . . . . $49.5 + 13.5D$
Binary add to or subtract from accumulator:. . . . $27 + 13.5C$
Multiply (subroutine):. . . . approximately 3500 (3-digit by 4-digit).
Multiply (optional hardware): . . . . . $33.75D^2 + 63,5D + 99$
Multiply cumulatively (optional hardware): . . . . . $33.75D^2 + 63.5D + 27$
Divide (optional hardware): . . . . . $74.25D^2 + 141.75 + 49.5$
.412 Floating point:. . . . . subroutine timings not available to date.
.413 Additional allowance for —
Indexing: 13.5
Re-complementing: . 18D (included in above times).

§ 051.

.414 Control
Compare —
Decimal: . . . . . 36 + 13.5D (36 if signs are opposite).
Binary: . . . . . 27 + 13.5C
Branch: 31.5
.415 Counter control —
Step and test: 40.5
.416 Edit: . . . . . 36+13.5C+ 9E, where E = number of characters inserted.
.417 Translate: . . . . . 36 + 13.5C
.418 Shift left: . . . . . 40.5 + B(9 + 18C), where B = number of bit positions shifted.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Binary	Decimal
c = a + b:	108 + 40.5C	112.5 + 45D
b = a + b:	54 + 22.5C	85.5 + 36D
Sum N items:	(54 + 22.5C)N	(49.5 + 27D)N
c = ab (optional hardware):	—	$33.75D^2 + 99.5D + 225$
c = a/b (optional hardware):	—	$74.25D^2 + 168.75D + 212.5$

.422 For arrays of data —

	Binary	Decimal
$c_i = a_i + b_j$:	324 + 40.5C	315 + 45D
$b_j = a_i + b_j$:	243 + 22.5C	274.5 + 36D
Sum N items:	(175.5 + 22.5C)N	(157.5 + 27D)N
$c = c + a_i b_j$ (optional hardware):	—	$33.75D^2 + 90.5D + 315$

.423 Branch based on comparison —
Numeric data: . . . . 319.5 + 13.5D
Alphabetic data:. . . . 310.5 + 13.5C
.424 Switching —
Unchecked:. 373.5
Checked: 535.5
List search: . . . . . 135 + 189N
.425 Format control, per character
Unpack —
90-column (translation):. . . . . 14.
80-column:. . . . . 0.
Compose:. . . . . 27.
.426 Table look-up, per comparison —
For a match:. . . . . 166.5 + 13.5C
For least or greatest: 247.5 + 40.5C
For interpolation point: . . . . . 166.5 + 13.5C

.427 Bit indicators —
Set bit in separate location: 40.5
Set bit in pattern:. . . 40.5
Test bit in separate location: 72.0
Test bit in pattern:. . 72.0

.428 Moving —
Large block, using block transfer instruction:. . . . . 216 + 9C (up to 1024 characters).

Small block, using arithmetic register as intermediate store: 54 + 18C (up to 16 characters).

§ 051.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:*	check	set program-testable indicator.
Decimal overflow:*	check	set program-testable indicator and generate a Class II interrupt unless inhibited.
Zero divisor:	causes decimal overflow.	
Invalid data:	none.	
Invalid operation:	none.	
Arithmetic error:	none.	
Invalid address:	check	cause a Class I interrupt to be generated.
Receipt of data from I/O device:	parity check	set program-testable indicator and cause a Class III interrupt if not inhibited.
Dispatch of data to I/O device:	parity check	set program-testable indicator and cause a Class III interrupt if not inhibited.
Accessing or transferring data within core storage:	parity check	cause a Class I interrupt.
Attempt to exceed basic transfer rate of memory:	check	cause a Class II interrupt.

* Overflow can occur due to the binary add or subtract or the optional multiply instruction. Decimal overflow can occur due to the decimal add or subtract or the optional cumulative multiply or divide instruction.

CENTRAL PROCESSOR – MODEL IV

§ 052.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1050 Model IV Processor.

.12 Description

All the information in Section 777:051 on the Model III Processor applies to the Model IV Processor as well, except that:

- The Model IV is appreciably faster (see PROCESSOR SPEEDS, below).
- All eight data channels are optional, with no fixed assignments, although the standard software may fix some assignments.
- The basic size of core storage is 8,192 characters, expandable to 65,536 characters in modules of 8,192 characters.

All programs coded for the Model III can be run on the Model IV. If the storage limits and fixed assignment of data channels of a system using the Model III Central Processor are taken into consideration when programming, programs written for the Model IV can also be run on the Model III without problems.

.14 First Delivery: . . . . . December 1965.

.2 PROCESSING FACILITIES

Same as for the 1050 Model III Processor (see Paragraph 777:051.2 in the preceding section).

.3 SEQUENCE CONTROL FEATURES

Same as for the 1050 Model III Processor (see Paragraph 777:051.3 in the preceding section).

.4 PROCESSOR SPEEDS

D = operand length in decimal digits.
C = operand length in characters.

.41 Instruction Times in Microseconds

.411 Fixed point
Add-subtract —
Decimal add to or subtract from accumulator:. . . . 20 + 6D
Decimal add to or subtract from memory: . . . . . 20 + 3D
Binary add to or subtract from accumulator:. . . . 10 + 3C
Multiply (optional hardware): . . . . . $15D^2 + 18D + 26$
Multiply cumulatively (optional hardware) $15D^2 + 54D + 16$

.412 Floating point:. . . . . subroutine times are not available to date.

.413 Additional allowance for indexing: . . . . . 4.

.414 Control
Compare —
Decimal: . . . . . 14 + 3D
Binary: . . . . . 10 + 3D
Branch: 12

.415 Counter control —
Step and test: 16

.416 Edit: . . . . . 14 + 6(C + E), where E = number of characters inserted.

.417 Translate: . . . . . 12 + 6C.

.418 Shift left: . . . . . 16 + B(6 + 4C), where B = number of bit positions shifted.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Binary	Decimal
c = a + b:	40 + 9C	44 + 10D
b = a + b:	20 + 5C	34 + 8D
Sum N items:	(20 + 5C)N	(20 + 6D)N
c = ab (optional hardware):	—	$15D^2 + 26D + 58$
c = a/b (optional hardware):	—	$15D^2 + 60D + 78$

.422 For arrays of data —

	Binary	Decimal
$c_i = a_i + b_j$:	113 + 9C	113 + 10D
$b_j = a_i + b_j$:	85 + 5C	99 + 8D
Sum N items: $= c + a_i b_j$ (optional hardware):	(63 + 5C)N	(59 + 6D)N $15D^2 + 24D + 113$

.423 Branch based on comparison —
Numeric data:. . . . . 108 + 3D
Alphabetic data:. . . . 104 + 3C

.424 Switching —
Unchecked:. 130
Checked: 188
List search: . . . . . 45 + 65N

.425 Format control, per character
Unpack —
90-column (translation):. 6
80-column:. 0
Compose:. 7

.426 Table look-up, per comparison —
For a match:. . . . . 61 + 3C
For least or greatest:. . . . . 87 + 5C
For interpolation point:. . . . . 61 + 3C

.427 Bit indicators —
Set bit in separate location:. 16
Set bit in pattern:. . . 16
Test bit in separate location:. 28
Test bit in pattern:. . 28

§ 052.

.428 Moving —
Large blocks (up to 1024 characters):. . 74 + 2C
Small blocks (up to 16 characters, using arithmetic register as intermediate store): . . . 20 + 4C

.5 ERRORS, CHECKS, AND ACTION

Same as the 1050 Model III Processor (see Paragraph 777:051.5 in the preceding section).

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . Consoles: Integrated and Free-Standing.

.12 Associated Units: . . . a Console Typewriter is currently available only on UNIVAC 1050 Real-Time Systems (1050-R).

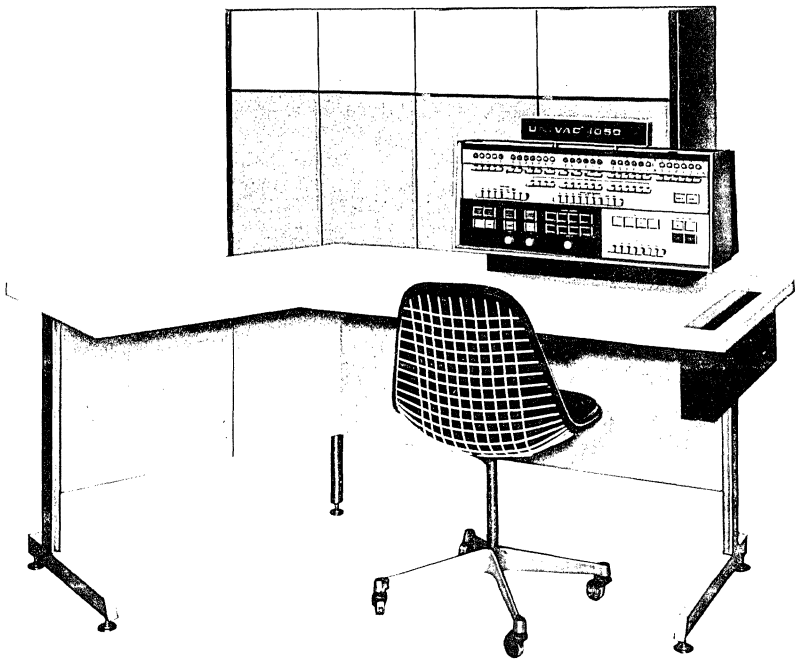
.13 Description

The UNIVAC 1050 control panel may be mounted either directly on the front of the Central Processor cabinet — the Integrated Console — or on a separate L-shaped table — the Free-Standing Console. Both units have the same switches and lights. A drop shelf, 18 inches by 26 inches, is provided with the Integrated Console, conveniently located about 35 inches above the floor. The Free-Standing Console table has sufficient room for the Console Typewriter (currently used in Real-Time systems only), as shown in the photograph below.

.13 Description (Contd.)

Included in the Console are switches and lights that enable an operator to:

- Turn the power supply on or off.
- Clear all indicators.
- Load an initial block of information into core storage from the card reader or a magnetic tape unit.
- Start the execution of a stored program at any particular location.
- Stop the execution of a program.
- Display or alter the instruction counter setting.
- Display or alter the contents of the instruction register.
- Interrogate and load core storage locations.
- Execute single instructions.
- Initiate an Operator Request interrupt.
- Trace the address of a particular operation code or instruction.
- Halt the central processor when the data in a particular storage location is altered (of great value when debugging a program).



UNIVAC 1050 FREE-STANDING CONSOLE

INPUT–OUTPUT: CARD READERS

§ 071.

.1 GENERAL

.11 Identity: . . . . . Card Readers.
Type 0706-01 — 600 cpm, 80-column.
Type 0706-05 — 600 cpm, 90-column.
Type 0706-00 — 800/900 cpm, 80-column.
Type 0706-04 — 800/900 cpm, 90-column.

.12 Description

Each of the two basic card readers for the UNIVAC 1050 is available in either an 80-column or 90-column version. Reading is performed column by column, so no full-card buffer is required. Types 0706-01 and 0706-05 will read at a maximum rate of 600 cards per minute. Types 0706-00 and 0706-04 will read complete cards at a maximum rate of 800 cards per minute or the first 72 columns of each card at a maximum rate of 900 cards per minute.

Some of the significant characteristics of these readers are:

- A 2,500-card input hopper;
- A 2,500-card output stacker;
- Optional stub-card feed;
- Photodiode sensing with automatic checking of the sensing elements before each card is read;
- Infinite clutch;
- Binary image reading;
- Automatic translation from Hollerith to internal code at the option of the programmer (80-column models only);
- Generation of an interrupt signal upon successful completion of an operation (can be program inhibited), an error condition, or an off-normal condition;
- Setting of testable indicators upon detection of registration check error, parity error, sensing element error, unit busy, and unit not ready (off-normal) conditions.

.12 Description (Contd.)

The column binary format for the 80-column card reader is two characters per column, with the more significant character at the top of the card. This format is compatible with the column binary card punch instructions. The 90-column binary format is the standard Remington Rand card format. Input areas of 80, 90, or 160 consecutive characters, depending upon the format, may be located anywhere in core storage, but the address of the storage location for the character from the first card column must be a multiple of 64. The base address of the input area must be stored in the appropriate I/O Channel Register prior to the initiation of a read instruction and is automatically incremented for each character transmitted. The base address can be automatically reset or advanced to the next input area by the read instruction. (Channel 1 is permanently assigned to the card reader in the Model III Central Processor, but there is no fixed channel assignment in the Model IV Central Processor.) The effective rate of reading will be governed by such considerations as:

- The number of input areas set up;
- The amount of computation necessary before a card is to be read;
- The operation of other peripheral subsystems (see Sections 777:111 and 777:112, Simultaneous Operations: Model III and Model IV).

The ability to initiate a card read cycle at any time (due to the infinite clutch) and the relatively small demands made on the central processor by the reader should permit reading speeds approaching the maximum rate to be obtained most of the time.

The Model III Central Processor can be connected to a maximum of four card readers, while the Model IV can handle up to eight. Separate synchronizers (RPQ for the Model III) are required for each unit after the first, and all units must have the exclusive use of an input-output channel.

The amount of processing time available for each card cycle is shown in Table I. Simultaneity is discussed in Sections 777:111 and 777:112, Simultaneous Operations.

§ 071.

TABLE I: CARD READER TIMING DATA

Reader speed	900 cpm*		600 cpm	
Processor model	Model III	Model IV	Model III	Model IV
Card cycle time	66 msec	66 msec	100 msec	100 msec
Memory interlock I/O	9%	0.24%	6%	0.16%
Software execution**	3%	0.79%	2%	0.52%
Time available for processing	88%	98.97%	92%	99.32%

* Based on reading 72 columns per card; speed is 800 cpm when reading full cards.
** Includes execution of read instruction and all necessary control functions, such as handling the interrupt generated upon successful completion of an operation.

INPUT–OUTPUT: CARD PUNCHES

§ 072.

.1 GENERAL

.11 Identity: . . . . . Card Punches.
Type 0600-00 — 300 cpm, 80-column.
Type 0600-01 — 300 cpm, 90-column.
Type 0600-12 — 200 cpm, 80-column.
Type 0600-13 — 200 cpm, 90-column.

.12 Description

There are two basic card punches for the UNIVAC 1050. Each of these is available in either an 80-column or 90-column version. Types 0600-00 and 0600-01 operate at a maximum rate of 300 cards per minute, and Types 0600-12 and 0600-13 at a maximum rate of 200 cards per minute.

Some of the significant characteristics of these punches are:

- A 1,000-card input hopper;
- Two 850-card output stackers;
- Four card stations (2 wait stations followed by the punch station and the Post Punch Check station);
- One clutch point;
- Binary image punching;
- Automatic translation from internal to Hollerith code (80-column models only);
- Hole-count check;
- Generation of an interrupt signal upon successful completion of an operation, (can be program inhibited), an error condition, or an off-normal condition;
- Setting of testable indicators upon detection of parity error, hole-count error, unit busy, and unit not ready (off-normal) conditions.

Column binary format for the 80-column punch is two characters per column, with the more significant character at the top of the card. This format is compatible with the column binary card read instructions. The 90-column binary format is the standard Remington Rand card format.

.12 Description (Contd.)

Different synchronizers are used for the card punch depending upon whether it is connected to the Model III or Model IV Central Processor. The Card Punch Synchronizer used with Model III is built directly into the Processor and accesses information in a manner typical of a row-by-row device: a separate core storage access is made to each character of the output field for each row to be punched. The synchronizer used with the Model IV is not internal to the processor and contains a full-card buffer, reducing the number of core storage accesses to one per card column.

Punch output areas of 80, 90, or 160 consecutive characters, depending upon the format, may be located anywhere in core storage, but the address of the character to be punched in the first column of the card must be a multiple of 64. The base address of the output area must be stored in the appropriate I/O Channel Register prior to the execution of a punch instruction and is automatically incremented for each character transmitted. The base address can be automatically reset or advanced to the next output area by the punch instruction. (Channel 2 is permanently assigned to a card punch unit in the Model III Central Processor, but there is no fixed channel assignment in the Model IV Central Processor.) The effective rate of punching will be governed by such considerations as:

- The number of punch output areas set up;
- The amount of computation necessary before a card is to be punched;
- The operation of other peripheral subsystems (see Sections 777:111 and 777:112, Simultaneous Operations: Model III and Model IV).

Accuracy controls include a parity check on each character transmitted to the synchronizer and a hole-count check after punching each card. Any failure of these checks causes the card to be automatically directed into Stacker 1 and causes an immediate interrupt. Programming can also cause cards to be deposited in Stacker 1 instead of the normally-selected Stacker 2.

The Model III Central Processor can be connected to a maximum of four card punch units, while the Model IV can handle up to eight. Separate synchronizers (RPQ for the Model III) are required for each unit after the first, and all units must have the exclusive use of an input-output channel.

The amount of processing time available during each 80-column punch cycle is shown in Table I, below. Simultaneity is discussed in Sections 777:111 and 777:112, Simultaneous Operations.

§ 072.

TABLE I: CARD PUNCH TIMING DATA

Punch speed	300 cpm		200 cpm	
Processor model	Model III	Model IV	Model III	Model IV
Card cycle time	200 msec	200 msec	300 msec	300 msec
Memory interlock	2.6 %	0.08%	1.70%	0.05%
Software Execution*	1.0%	0.26%	0.67%	0.17%
Time available for processing	96.4%	99.66%	97.63%	99.78%

* Includes execution of punch instruction and all necessary control functions, such as handling the interrupt generated upon successful completion of an operation.

INPUT–OUTPUT: PUNCHED TAPE SUBSYSTEM

§ 073.

.1 GENERAL

.11 Identity: . . . . . Punched Paper Tape Subsystem (1000 or 300 char/sec reader and 110 char/sec punch).

.12 Description

A UNIVAC 1050 Punched Paper Tape Subsystem consists of a separate reader and punch unit housed in the same cabinet as their synchronizer. The two available models use the same punch unit, which is a modification of the Teletype BRPE-11 punch and has a peak speed of 110 characters per second. One model employs a modified Digitronics Model B 3000 paper tape reader, while the other uses the slower Digitronics Model 2500 reader.

Both readers can operate in the normal mode, and the faster model can also operate in a non-stop mode. In the normal mode, a character count in the appropriate I/O Channel Register determines the number of characters to be read; while in the non-stop mode, the unit reads continuously until the supply of tape is exhausted or until a stop character is recognized. Error conditions occurring while reading in the non-stop mode result in a loss of data between the point of error and the stopping point.

The faster reader has peak speeds of "1,000 characters per second or greater" in the non-stop mode and either 500 or 250 characters per second in the normal mode; spooling facilities are optional. The slower reader has a peak speed of 300 characters per second and reads tape in strip form only; no spooling facilities are offered.

From one to three Punched Paper Tape Subsystems can be connected to the Model III Central Processor, and up to eight Subsystems can be connected to the Model IV. The synchronizer is connected to one unassigned channel, permitting one input or output operation to be executed at a time. Input and output operations can be intermixed, and malfunctioning of either the reader or punch unit does not affect the operation of the other.

The readers in both subsystems are quite similar except for speeds. Some of their important characteristics are:

- Photo-electric reading;
- Tape is advanced by pinch rollers;
- Strip reading is standard;
- Spooling option is available on the higher-speed model only, permitting use of 8-inch or 10 1/2-inch NAB (National Association of Broadcasters) spools;

.12 Description (Contd.)

- Tension arm reservoirs for both feed and take-up spools;
- Reads standard 5-, 6-, 7-, or 8- track tape of 11/16-, 7/8-, or 1-inch width;
- Reads chad-type (fully punched) tape;
- Reads either plastic (Mylar) or paper tapes with less than 40% transmissivity;
- Single-frame backspace;
- Code translation must be programmed.

Some of the important characteristics of the punch unit are:

- 110 char/sec peak punching speed;
- Tape is advanced by sprocket drive;
- Feed spool is standard, permitting use of 8-inch or 10 1/2-inch NAB spools;
- Take-up spool is optional;
- Punches 5-, 6-, 7-, or 8-level codes in tapes of 11/16-, 7/8-, or 1-inch widths;
- No read-after-write check on punching accuracy.
- Produces chad-type (fully punched) tapes;
- All code translations must be programmed.

Block length is variable from 1 to 256 characters, controlled by a character count in the appropriate I/O Channel Register.

Extensive switching capabilities (in the form of a detachable plugboard) can provide the following functions —

For the reader:

- Define the number of tracks to be read.
- Permit the rearrangement of bits from their tape-track positions to relatively different positions in the UNIVAC 1050 character codes.
- Define the wired stop code for the reader.
- For five-track tape, specify the interpretation of space codes as they individually affect the reader shift status.

§ 073.

.12 Description (Contd.)

- Select whether odd parity, even parity, or no parity checking will be employed.
- Cause parity bits to be generated.
- Enter the shift status into storage as a character if desired.

For the punch:

- Permit rearrangement of bits from their positions in the UNIVAC 1050 character to relatively different positions in tape tracks.
- Define the wired stop codes for the punch.
- Cause odd or even parity bits to be generated for punching (but not checked at the punch).
- Permit double-frame punching for five-track tape (in which one UNIVAC 1050 character occupies two contiguous row positions on the tape), or two-character mode for tape codes of more than six bits (in which one tape code occupies two contiguous character positions in 1050 core storage).

.12 Description (Contd.)

Malfunctions and parity errors, either in data sent to the synchronizer for punching or from the tape when reading (if the plugboard is appropriately wired), cause an interrupt and transfer of control to the location specified in the corresponding I/O Channel Register. An interrupt signal can also be generated, at the option of the programmer, upon successful completion of an operation. Testable indicators are set for the various conditions, enabling a recovery routine to determine the cause of interruption and proceed accordingly.

Some typical times available for processing during a punched tape read or write operation are shown in Table 1.

Either Punched Paper Tape Subsystem can operate simultaneously with any other peripheral subsystem.

TABLE 1: PUNCHED TAPE TIMING DATA

Speed	Read: 1000 char/sec		Read: 500 char/sec		Punch: 110 char/sec	
Processor model	Model III	Model IV	Model III	Model IV	Model III	Model IV
Block time*	100 msec	100 msec	200 msec	200 msec	910 msec	910 msec
Memory interlock	0.45%	0.2%	0.22%	0.1%	0.05%	0.02%
Software execution**	2.0%	0.52%	1.0%	0.26%	0.2%	0.06%
Time available for processing	97.55%	99.28%	98.78%	99.64%	99.75%	99.92%

* For 100-character blocks.
** Includes execution of paper tape instruction and all necessary control functions, such as handling of the interrupt generated upon sucessful completion of an operation.

INPUT–OUTPUT: HIGH SPEED PRINTERS

§ 081.

.1 GENERAL

.11 Identity: . . . . . High Speed Printers.
Type 0755-02: 600/750 lines per minute.
Type 0755-01: 700/922 lines per minute.

.12 Description

The Type 0755-01 and Type 0755-02 printers are identical except for speed. The maximum rates of printing for the Type 0755-01 printer are 750 single-spaced lines per minute when printing with a restricted 42-character set (A through Z, 0 through 9, and 6 special characters) and 600 single-spaced lines per minute when using the full 63-character set. Under the same conditions the maximum rates of printing for the Type 0755-02 printer are 922 and 700 lines per minute, respectively. The maximum rates attainable at larger inter-line spacings are shown on the accompanying graphs.

Some of the pertinent features of both printers are:

- Printing by an on-the-fly hammer stroke which presses the ribbon and paper against an engraved drum;
- 63 printable characters (see Table II below for a listing);
- 128 print positions per line (132 print positions optional);
- Full-line or half-line printing (64 characters) at the option of the programmer (half-line printing reduces the memory interlock time);
- Vertical spacing of either 6 or 8 lines per inch at the option of the operator;
- Horizontal spacing of 10 characters per inch;
- Ability to handle paper stock from 4 to 22 inches wide, up to card stock thickness;
- Ability to produce at least five carbon copies with 10- to 12-pount paper;
- Parity checking of the data received for printing;

.12 Description (Contd.)

- Generation of an interrupt signal upon successful completion of an operation (can be program inhibited), an error condition, or an off-normal condition.

Skipping is under program control, with the number of lines to be skipped set by the program in the appropriate I/O Channel Register. From 0 to 63 lines can be skipped with one instruction. Form control must be accomplished by programming since there is no vertical spacing control tape. Skipping speed after the first line is 20 inches per second (equivalent to 120 lines per second at 6 lines per inch).

The Print Buffer is required with the Type 0755-01 700/922 lpm Printer and is optional with Type 0755-02 Printer. The buffer is also required in all 1050 systems except a system using the Model III Central Processor and having only the low-speed card reader, low-speed printer, and either card punch as peripherals.

Printer output areas can be located anywhere in core storage. The base address must be stored in the appropriate I/O Channel Register and can be automatically incremented by the print instruction. (Channel 0 is permanently assigned to a printer unit in the Model III Central Processor, but there is no fixed channel assignment in the Model IV Central Processor.) The effective rate of printing will be governed by such considerations as:

- The amount of computation necessary before a line is printed;
- Whether or not the print buffer is incorporated;
- The inter-line spacing;
- Use of the full or a restricted character set.

The Model III Central Processor can be connected to a maximum of four printers, while the Model IV can handle up to eight. Separate synchronizers are required for each printer after the first, and all printers must have the exclusive use of an I/O channel.

The amount of processing time available during each print cycle is shown in Table I, below. Simultaneity is discussed in Section 777:111, Simultaneous Operations.

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TABLE I; PRINTER TIMING DATA

Printer Speed	600/750 lpm			700/922 lpm	
Processor Model	Model III, No buffer	Model III With buffer	Model IV With buffer	Model III With buffer	Model IV With buffer
Print cycle*	80 msec.	80 msec.	80 msec.	65 msec.	65 msec.
Memory interlock	33.5%	0.75%	0.33%	0.92%	0.4%
Software execution**	2.5%	2.5%	0.65%	3.08%	0.8%
Time available for processing	64.0%	96.75%	99.02%	96.0%	98.8%

* Includes printing and spacing one 128-character line, using the restricted 42-character set.
** Includes execution of the print instruction and all necessary control functions, such as handling the interrupt generated upon successful completion of an operation.

TABLE II: STANDARD CHARACTER SET

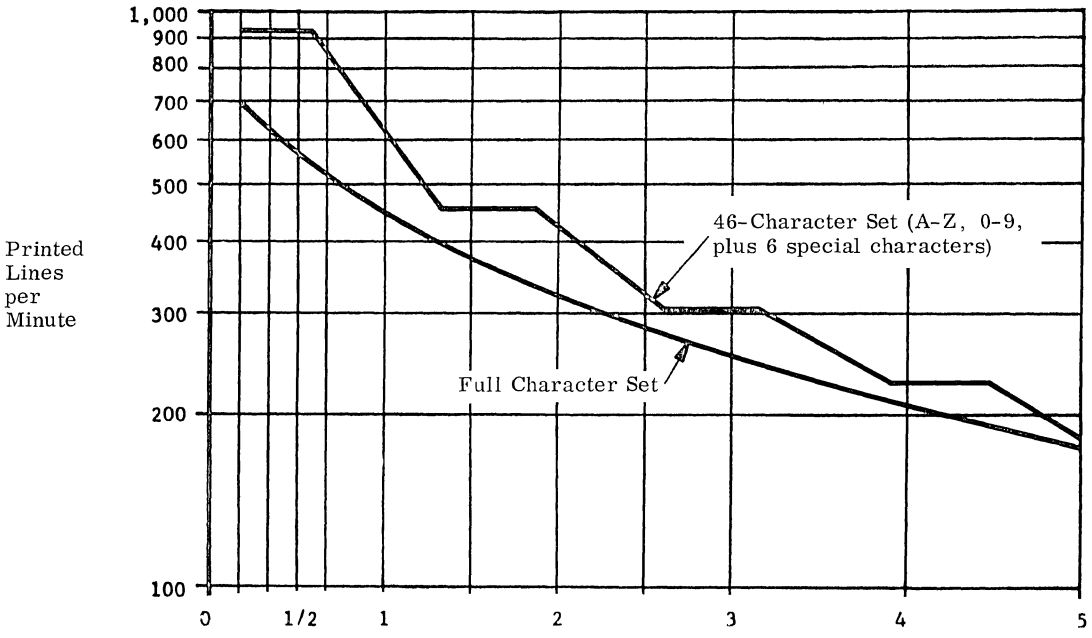
Type 0755-01 and 0755-02 High Speed Printers

Character	Printed Symbol	Character	Printed Symbol
Close Bracket	]	At the Rate of	@
Minus or Hyphen	-	Asterisk	*
Zero	0	Dollar Sign	$
One	1	Exclamation Mark	!
Two	2	J	J
Three	3	K	K
Four	4	L	L
Five	5	M	M
Six	6	N	N
Seven	7	O	O
Eight	8	P	P
Nine	9	Q	Q
Left Oblique	\	R	R
Semicolon	;	Percent	%
Open Bracket	[	Apostrophe	'
Plus	+	Delta	Δ
Colon	:	Not Equal	≠
Period	.	Open Parenthesis	(
Question Mark	?	Comma	,
A	A	Ampersand	&
B	B	Slash	/
C	C	S	S
D	D	T	T
E	E	U	U
F	F	V	V
G	G	W	W
H	H	X	X
I	I	Y	Y
Equal	=	Z	Z
Less	<	Close Parenthesis	)
Number	#	Greater	>
		Lozenge	⌑

§ 081.

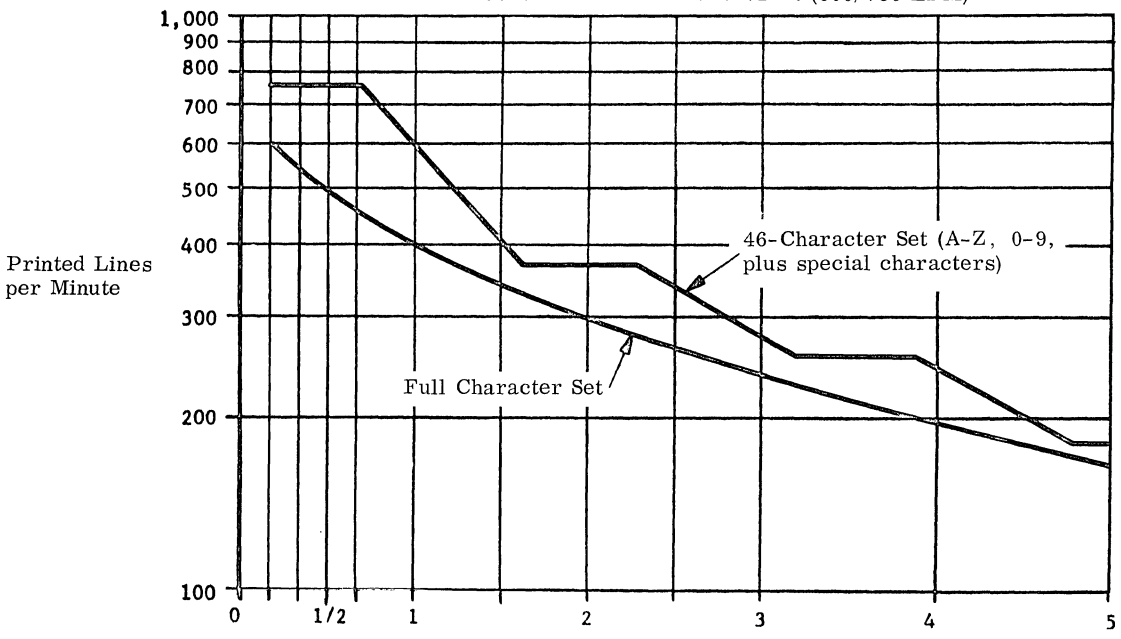
EFFECTIVE SPEED:

TYPE 0755-01 HIGH SPEED PRINTER (700/922 LPM)



EFFECTIVE SPEED:

TYPE 0755-02 HIGH SPEED PRINTER (600/750 LPM)



INPUT–OUTPUT: UNISERVO III A

§ 091.

.1 GENERAL

.11 Identity: . . . . . Uniservo III A Magnetic Tape Handler. Type 0850-00.

.12 Description

The Uniservo III A provides high speed magnetic tape input-output for the UNIVAC 1050 and compatibility between the 1050 and UNIVAC III, 490, or 1107 computer systems using Universo III A Tape Handlers. It is the same tape handler offered for the UNIVAC III, but with a slightly different control unit. From one to six Uniservo III A Tape Handlers can be connected to a Uniservo III A Control and Synchronizer Unit and a Uniservo Power Supply, forming a Magnetic Tape Subsystem. Each subsystem fully occupies two input-output channels, and only one tape handler per subsystem can read or write at a time. One or two synchronizers can be connected to the Model III Central Processor, while up to four synchronizers can be connected to the Model IV. The logical address of each tape handler is assigned by plugboard wiring.

Data is recorded by the "pulse phase" method, which is fully described in the UNIVAC 490 report (see Paragraph 775:092.12). Tape speed is 100 inches per second. Recording density is 1,000 rows per inch, with 9 tracks recorded across the tape. The number of rows per block must be a multiple of three.

Three formats are available for writing or reading a record and can be selected under program control. We shall call them Formats 1, 2, and 3. Format 1 is the basic mode of reading tape records in UNIVAC 1050 systems using Uniservo III A tape handlers. One character (6 data bits plus 1 parity bit) is contained in each tape row. The two unused tracks are ignored when reading and set to zero when writing in this mode. Format 1 also enables the UNIVAC 1050 to read tapes produced by or write tapes for UNIVAC 490 or UNIVAC 1107 systems, provided these systems' Univervo III A Tape Handlers are operating in the format of 5 rows per word (30 bits) or 6 rows per word (36 bits), respectively.

Formats 2 and 3 provide compatibility with UNIVAC III systems. Three rows (27 bit positions) are used to record one 24-bit UNIVAC III word plus 1 bit for the sign and 2 bits for a modulo-3 check. Format 2 is used when the sign bit is of no importance. The 24 bits of four consecutive characters of UNIVAC 1050 core storage represent one UNIVAC III word. The sign bit is set to zero (positive) when writing and is not transmitted when reading on the UNIVAC 1050. A fifth character (least significant) is added in Format 3. The sign

.12 Description (Contd)

bit is interpreted as the most significant bit of this character. The other five bits of the character are set to zero when reading in this mode and are not transferred when writing.

In Format 3, the UNIVAC 1050 Control and Synchronizer Unit performs a modulo-3 check on incoming data, using the 2 check bits on the tape. During write operations in this mode, the control unit generates modulo-3 check bits and transcribes them onto the tape. When reading into UNIVAC 1050 core storage, parity bits are generated to prevent parity errors when the data is subsequently used.

Under program control, a UNIVAC 1050 can unpack data recorded by a UNIVAC III in the form of six 4-bit digits per word in Format 2 or 3. A peak data transfer rate of 200,000 decimal digits per second is attained in this mode.

As each block of data is recorded, the control unit automatically "surrounds" it by writing a 27-row pattern (containing "1"s in all tracks) and a 3-row sentinel both before and after the data itself. The pattern and sentinel alert the reading circuits to the beginning and end of data, whether the block is read forward or backward. In addition, each normally-written block is followed by a 223-row pattern consisting of "0"s in the odd tracks only. Each block containing an error detected at recording time (e.g., incorrect parity) contains 725 additional rows of special patterns which indicate that the contents of the block shall be ignored when read. This is identical to the operation of the Uniservo III A in UNIVAC III, 490, and 1107 systems.

Peak data transfer rates are as follows:

Condition	Peak Transfer Rate
Format 1:	100,000 char/sec.
Formats 2 and 3 (alphanumeric):	133,000 char/sec.
Formats 2 and 3 (decimal):	200,000 digits/sec.

Effective speeds are shown in the graph on page 777:091.801.

A read-after-write row parity or modulo-3 check (depending upon the format) permits detection of most recording errors at the time of occurrence. A "frame count" error is detected whenever the number of data rows in a block is not an integer multiple of three. Four special 9-bit registers in the control unit permit automatic compensation for skew of up to four rows (0.004 inch) in the tape being read. Excessive skew causes an error indication. Every tape recording and reading error, as well as a successful completion of an

§ 091.

.12 Description (Contd.)

operation (optional), initiates an interrupt and causes a particular testable indicator to be set, depending upon the condition. In addition, recording errors cause the previously mentioned special patterns to be added to each incorrectly-written block.

The UNIVAC 1050's capabilities for simultaneous operations are discussed in Section 777:111.

.13 Availability: . . . . . immediate.

.14 First Delivery: . . . . . 1963.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan.
.212 Reservoirs —
Number: 2
Form: . . . . . vacuum column.
Capacity: . . . . . approximately 5 feet.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by magnetic write head.
.222 Sensing system: . . . . . magnetic read head.
.223 Common system: . . . . yes; common read/write head.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 9.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read/write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 9.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape with magnetizable coating.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . row, at 1,000 rows per inch.
.322 Parallel by: . . . . . 9 tracks.
.324 Bit use —

	Format 1 (per row)	Format 2 (per 3 rows)	Format 3 (per 3 rows)
Data:	6	24	24.
Redundancy check:	1	2	2.
Timing:	0	0	0.
Control signals:	0	0	0.
Sign:	0	0	1.
Unused:	2	1	0.
Total:	9	27	27.

.325 Row use, per block —
Data: . . . . . 3 to 3N.
Redundancy check: . . 0.
Timing: . . . . . 0.
Control signals: . . . . 283.
Interblock gap: . . . . 0.750 inch (includes control signals).

.33 Coding: . . . . . binary image of data in core storage.

.34 Format Compatibility: only with Uniservo III A units in UNIVAC III, 490, 1107, or other 1050 systems.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.50 inch.
.352 Length: . . . . . 3,500 feet, 1,800 feet, or 600 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . Uniservo III A Control and Synchronizer.
Type 0551-01.

.42 Connection to System

.421 On-line: . . . . . Model III Central Processor: 1 or 2 Control and Synchronizer units.
Model IV Central Processor: 1 to 4 Control and Synchronizer units.
Each unit fully occupies 2 input-output channels.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 6 tape handlers.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load —
Model III: . . . . . 1 to 4,096 characters.
Model IV: . . . . . 1 to 8,192 characters.
.442 Input-output areas: . . . core storage.
.443 Input-output area access: . . . . . each character.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block —
Model III: . . . . . 1 to 4,096 UNIVAC 1050 characters.
Model IV: . . . . . 1 to 8,192 UNIVAC 1050 characters.
.512 Block demarcation —
Input: . . . . . inter-block gap or character count in I/O Channel Register.
Output: . . . . . character count in I/O Channel Register.

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.52 Input-Output Operations

.521 Input: . . . . . read one block forward or backward into core storage locations specified by appropriate I/O Channel Register.
.522 Output:. . . . . write one block forward from core storage locations specified by appropriate I/O Channel Register.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . interblock gap.
.526 Searching: . . . . . none.

.53 Code Translation: . . . none; binary images of data in core storage are recorded on tape (see Paragraph .324).

.54 Format Control: . . . . there are three formats available by program control, permitting compatibility with UNIVAC 490, III, and 1107 systems. See Paragraph .12 for further information.

.55 Control Operations

Disable:. . . . . yes, following rewind with interlock.
Request interrupt: . . . yes.
Select format:. . . . . yes.
Select code: . . . . . no.
Rewind: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device:. . . . . no.
Output lock: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End-of-medium marks: yes.
Modulo 3 error (Formats 2 and 3):. . yes.
Parity check error (Format 1):. . . . . yes.

.6 PERFORMANCE

.61 Conditions

I: . . . . . Format 1; one 6-bit character per row.
II:. . . . . Format 2; four 6-bit characters per three rows (no sign bit).
III: . . . . . Format 3; four 6-bit characters per three rows (plus sign bit).
IV: . . . . . Format 2; six 4-bit decimal digits per three rows.

.62 Speeds

.621 Nominal or peak speed: . . . . . 100,000 rows/sec for all conditions.
Condition I:. . . . . 100,000 char/sec.
Conditions II and III:. 133,000 char/sec.
Conditions IV:. . . . . 200,000 digits/sec.
.622 Important parameters —
Recording density:. . 1,000 rows/inch.
Tape speed: . . . . . 100 inches/sec.
Rewind time:. . . . . 125 seconds per 3,500-ft. reel.
Interblock gap: . . . . 0.75 inch (includes necessary control characters).
Start-stop time:. . . . 13.2 msec.
.623 Overhead:. . . . . 13.2 msec/block.
.624 Effective speeds

Condition	Effective speed
I:	100,000C/(C + 1320) char/sec.
II and III:	133,000C/(C + 1760) char/sec.
IV:	200,000D/(D + 2640) digits/sec.

where C = number of 6-bit characters per block, and D = number of 4-bit decimal digits per block; see also graph 777:091.801.

.63 Demands on System

Component	Condition	Msec per character	Percentage
Model III Central Processor Core Storage:	I	0.0045	45.
	II	0.0045	60.
	III	0.0056	75.
	IV	0.0030*	60.
Model IV Central Processor Core Storage:	I	0.0020	20.
	II	0.0020	27.
	III	0.0025	33.
	IV	0.0013*	27.

* msec per digit.

Note: each rewind instruction interlocks core storage for 182 to 357 msec.

.7 EXTERNAL FACILITIES

.71 Adjustments:. . . . . none.

.72 Other Controls

Function	Form	Comment
Forward:	button	sets tape for forward operation.
Backward:	button	sets tape for backward operation.
Rewind:	button	rewinds tape.
Change Tape:	button	moves tape to load point.

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.73 Loading and Unloading

.731 Volumes handled —
Storage: . . . . . reel.
Capacity: . . . . . 3,500 feet of tape. For blocks of 1,000 characters this represents the following capacities:
Format 1: . 23.7 million 6-bit characters.
Formats 2 and 3:. . . . 28.0 million 6-bit characters.
Formats 2 and 3: . . . 34.2 million 4-bit decimal digits.

.732 Replenishment time:. . 0.5 to 1.0 minute; tape unit needs to be stopped.

.734 Optimum reloading period: . . . . . 7 minutes.

.8 ERRORS, CHECKS, AND ACTION

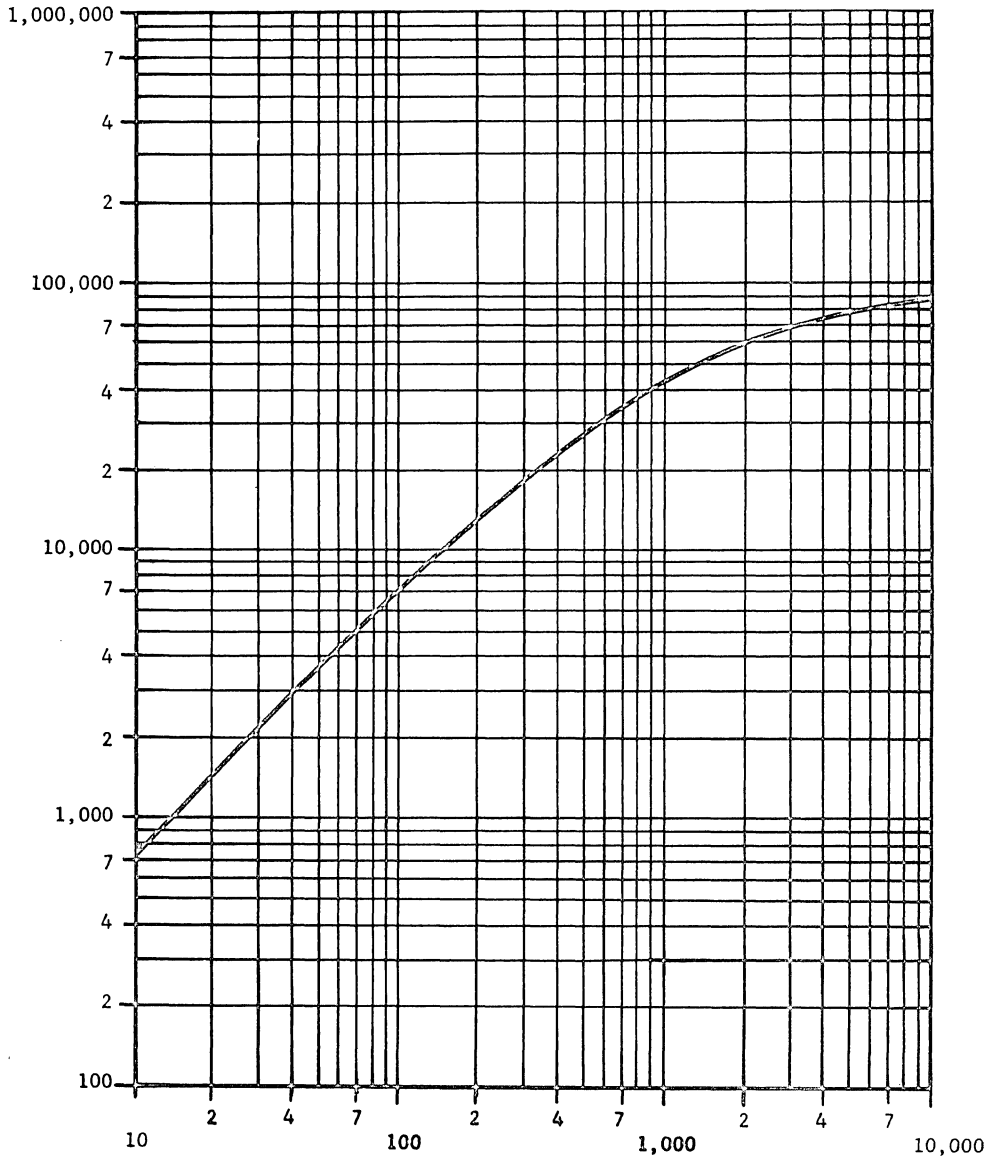
Error

Recording:	read-after-write modulo-3 check or row parity check, depending on Format.	set indicator and interrupt.
Reading:	modulo-3 check or row parity check, depending on Format	set indicator and interrupt.
Invalid code:	all codes are valid	
Exhausted medium:	check	set indicator and interrupt.
Imperfect medium:	"bad spot" check	set indicator and interrupt.
Timing conflicts:	check	set indicator and interrupt.
Excessive skew:	check	set indicator and interrupt.

Note: The type of error is determined by testing the individual indicators.

§ 091.

EFFECTIVE SPEED:
UNISERVO III A MAGNETIC TAPE HANDLER



Note: A "data row" may contain more than one character; see Description, Paragraph 777:091.12.

INPUT–OUTPUT: UNISERVO IV C

§ 092.

.1 GENERAL

.11 Identity: . . . . . Uniservo IV C Magnetic Tape Handler.
Type 0851-04.

.12 Description

The Uniservo IV C Tape Handler is a modification of the Uniservo III C Tape Handlers previously offered by UNIVAC. The IV C can read or write at a density of 800 rows per inch (optional) in addition to the densities of 200 rows per inch and 556 rows per inch offered in the III C. The Uniservo IV C processes tapes in a format compatible with all tape units currently produced by IBM except the Model 7340 Hypertape Drive and the new 2400 Series units.

A Uniservo IV C Control and Synchronizer Unit, a Power Supply, and from one to six Uniservo IV C tape handlers comprise a Compatible Tape Subsystem. Each Subsystem fully occupies two input-output channels. Systems with the 1050 Model III Central Processor can have one or two subsystems connected, while the Model IV can have up to four. Only one Uniservo IV C tape handler can be reading or writing at any one time. The logical address assigned to each tape handler can only be changed by means of a plugboard on the Tape Adapter Cabinet

Tape speed is 112.5 inches per second. Recording density may be 200, 556, or 800 (optional) rows per inch, providing peak data transfer rates of 22,500, 62,500, or 90,000 characters per second, respectively. Each tape row consists of six data bits and one parity bit. Reading and writing can be performed in the binary mode (with odd parity) or the BCD mode (with even parity). Binary images are transferred in the binary mode. Internal circuitry automatically performs code conversions between the UNIVAC 1050 internal code and the IBM 6-bit BCD code in the BCD mode.

Block length is variable from one character to the capacity of one core storage module (4,096 characters for the Model III Central Processor and 8,192 characters for the Model IV). The base address of the input-output area, as well as a block character count, is contained in the appropriate I/O Channel Register. The External Function instruction specifies a read or write operation, the unit involved, the recording mode (binary or BCD), the density, and whether or not an external interrupt shall occur upon successful completion of the operation. This instruction is also used to test or reset indicators that show which condition caused an interrupt.

.12 Description (Contd.)

The Uniservo IV C tape handler can read only in the forward direction and, unlike the Uniservo III C as used with the UNIVAC 490 system, cannot perform any search or skip operations.

As in IBM tape units, two-gap magnetic heads are used, permitting a read-after-write parity check on recording. A longitudinal parity check character is written after the last data row in each block. Both longitudinal and lateral (row) parity are checked during each read or write operation. Abnormal conditions (such as parity errors, control busy, or end-of-tape marks) and successful completion of an operation (optional) cause interrupts and set testable indicators. By testing the status of the indicators, the program can determine the cause of interruption and jump to a subroutine to handle the condition.

Simultaneity is discussed in Sections 777:111 777:112, Simultaneous Operations.

.14 First Delivery: . . . . . January 1964.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . vacuum capstan and tape tension.

.212 Reservoirs —
Number:. . . . . 2.
Form: . . . . . vacuum columns.
Capacity: . . . . . approx. 6 feet of tape.

.213 Feed drive:. . . . . electric motor.

.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.

.222 Sensing system:. . . . . magnetic head.

.223 Common system: . . . . 2-gap head provides read-after-write parity checking.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station:. . . . . erase.
Stacks:. . . . . 1.
Heads/stack: . . . . . 7.
Method of use:. . . . . 1 row at a time.

Use of station:. . . . . write.
Stacks:. . . . . 1.
Heads/stack:. . . . . 7.
Method of use:. . . . . 1 row at a time.

Use of station:. . . . . read.
Distance: . . . . . 0.25 inch after write head.
Stacks:. . . . . 1.
Heads/stack:. . . . . 7.
Method of use:. . . . . 1 row at a time.

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.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape with magnetizable surface.
.312 Phenomenon:. . . . . magnetization.

.32 Positional Arrangement

.321 Serial by:. . . . . row, at 200, 556, or 800 (optional) rows per inch.
.322 Parallel by: . . . . . 7 tracks.
.324 Track use —
Data:. . . . . 6.
Redundancy check:. . 1 (parity).
Timing: . . . . . 0.
Unused: . . . . . 0.
Total: . . . . . 7.
.325 Row use, per N-character block —
Data:. . . . . 1 to N.
Redundancy check:. . 1 (parity).
Timing: . . . . . 0.
Control signals:. . . . 0.
Unused: . . . . . 0.
Interblock gap: . . . . 0.75 inch.

.33 Coding: . . . . . in the binary mode, row images are transferred. In the BCD mode, the image is automatically translated from IBM 6-bit BCD code to UNIVAC 1050 internal code (or the reverse).

.34 Format Compatibility: with all IBM 700, 1400, and 7000 series systems via IBM 727, 729, and 7330 Magnetic Tape Units; with UNIVAC III, 490, 1107, or other 1050 systems using Uniservo III C, IV C, or VI C Tape Handlers; and with other "IBM compatible" tape units.

.35 Physical Dimensions

.351 Overall width:. . . . . 0.50 inch.
.352 Length: . . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity:. . . . . Uniservo IV C Control and Synchronizer, Type 0556-00.
Uniservo IV C Power Supply, Type 1353-01.

.42 Connection to System

.421 On-line:. . . . . 1 or 2 Magnetic Tape Subsystems can be connected to the Model III Central Processor; up to 4 can be connected to the Model IV; each requires 1 Control and Synchronizer unit and 1 Power Supply, and each fully occupies 2 input-output channels.
.422 Off-line:. . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 6.
.432 Restrictions:. . . . . none.

.44 Data Transfer Control

.441 Size of load —
Model III:. . . . . 1 to 4,096 characters.
Model IV:. . . . . 1 to 8,192 characters.
.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . . each character.
.444 Input-output area lockout: . . . . . none.
.445 Table control:. . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block —
Model III:. . . . . 1 to 4,096 characters.
Model IV:. . . . . 1 to 8,192 characters.
.512 Block demarcation —
Input:. . . . . interblock gap on tape, or character count in I/O Channel Register.
Output:. . . . . character count in I/O Channel Register.

.52 Input-Output Operations

.521 Input:. . . . . read 1 block of data forward only at 200, 556, or 800 rows per inch and in either binary mode (odd parity) or BCD mode (even parity); external interrupt upon completion is optional.
.522 Output:. . . . . write 1 block of data forward at 200, 556, or 800 rows per inch and in either binary mode (odd parity) or BCD mode (even parity); external interrupt upon completion is optional.
.523 Stepping: . . . . . 1 block backward (backspace); approximately 5 inches forward (to skip and erase defective tape areas).
.524 Skipping: . . . . . none.
.525 Marking: . . . . . end-of-file mark; interblock gap.
.526 Searching: . . . . . none.

.53 Code Translation: . . . automatic in the BCD mode; none in the binary mode, since binary images of data are transferred.

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.54 Format Control: . . . . by program.

.55 Control Operations

Disable: . . . . . yes, following rewind with interlock.
Request interrupt: . . . yes.
Select format: . . . . . yes, binary or BCD.
Rewind: . . . . . yes.
Unload: . . . . . no.
Terminate current operation: . . . . . yes.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . no.
Output lock: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: yes, 14 feet from physical end.
End of file: . . . . . yes.
Rewinding: . . . . . yes.

.6 PERFORMANCE

.61 Conditions

I: . . . . . reading at 200 rows/inch.
II: . . . . . reading at 556 rows/inch.
III: . . . . . reading at 800 rows/inch.
IV: . . . . . writing at 200 rows/inch.
V: . . . . . writing at 556 rows/inch.
VI: . . . . . writing at 800 rows/inch.

.62 Speeds

.621 Nominal or peak speed —
I and IV: . . . . . 22,500 char/sec.
II and V: . . . . . 62,500 char/sec.
III and VI: . . . . . 90,000 char/sec.

.622 Important parameters —
Recording density: . . 200 or 556 rows/inch.
Tape speed: . . . . . 112.5 inches/sec.
Full rewind time: . . . 87 seconds.
Interblock gap: . . . . 0.75 inch.
End-of-file gap: . . . . 3.7 inches.
Start time —
Read: . . . . . 6.3 msec.
Write: . . . . . 4.1 msec.
Stop time —
Read: . . . . . 9.0 msec.
Write: . . . . . 9.0 msec.

.623 Overhead (start plus stop time)
Reading: . . . . . 15.3 msec.
Writing: . . . . . 13.1 msec.

.624 Effective speeds (char/sec.)
I: . . . . . 22,500N/(N + 347).
II: . . . . . 62,500N/(N + 965).
III: . . . . . 90,000N/(N + 1389).
IV: . . . . . 22,500N/(N + 295).
V: . . . . . 62,500N/(N + 820).
VI: . . . . . 90,000N/(N + 1179).
where N = number of characters per block (see graph).

.63 Demands on System

Component	Condition	Msec per char. or	Percentage of data transfer time
Model III Core Storage:	I and IV	0.0045	10.1
	II and V	0.0045	28.1
	III and VI	0.0045	40.5
Model IV Core Storage:	I and IV	0.0020	4.5
	II and V	0.0020	12.5
	III and VI	0.0020	18.0

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Rewind:	switch/light	rewinds and positions tape.
Forward:	switch/light	moves tape forward.
Backward:	switch/light	moves tape backward.
Change tape:	switch/light	moves tape to load point.

.73 Loading and Unloading

.731 Volumes handled: . . . 2,400 feet per reel; for 1,000-character blocks, 5,000,000 characters at 200 char/inch, 11,300,000 characters at 556 char/inch, or 14,400,000 characters at 800 char/inch.

.732 Replenishment time: . . 0.5 to 1.0 minute; tape handler needs to be stopped.

.734 Optimum reloading period: . . . . . 4 minutes.

.8 ERRORS, CHECKS, AND ACTION

Error	Check of Interlock	Action
Recording:	read-after-write parity check	set indicator and interrupt.
Reading:	lateral and longitudinal parity check	set indicator and interrupt.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	all codes are valid.	
Exhausted medium:	check	set indicator and interrupt.
Imperfect medium:	see Recording.	
Timing conflicts:	check	set indicator and interrupt.

Note: The type of error is determined by testing individual indicators.

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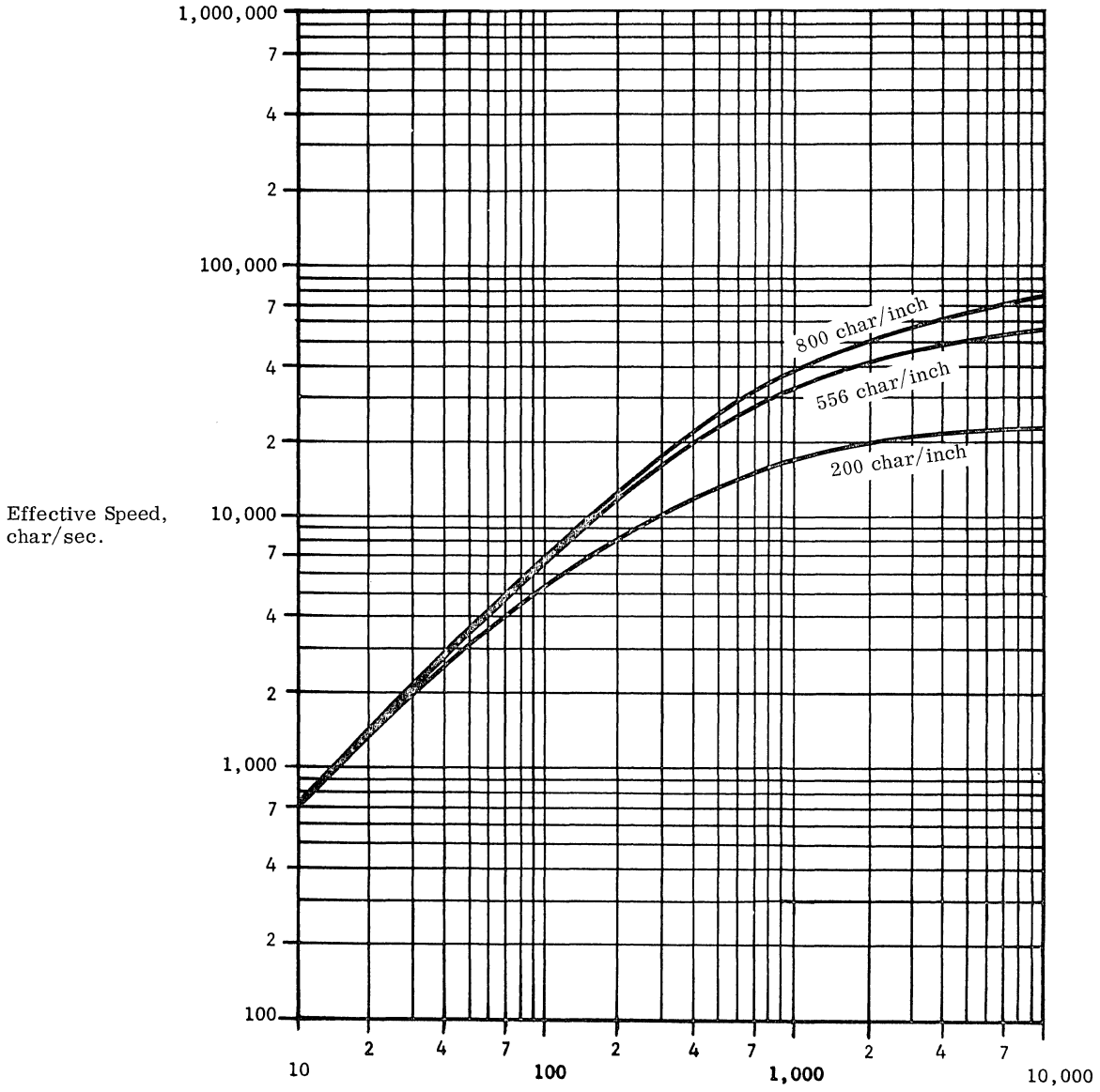
EFFECTIVE SPEED:

UNISERVO IV C MAGNETIC TAPE HANDLER



Note: Effective speeds are based on the average of reading and writing speeds.

INPUT–OUTPUT: UNISERVO VI C

§ 093.

.1 GENERAL

.11 Identity: . . . . . Uniservo VI C Magnetic Tape Handler.
Type 0858-00 (Tape Handler plus Control).
Type 0858-01 (additional Tape Handler).

.12 Description

The Uniservo VI C Tape Handler is a completely new unit, functionally similar to the Uniservo III C and IV C, but having a substantially reduced tape speed of 42.7 inches per second and a significantly lower cost. The format of the Uniservo VI C is compatible with all currently-produced IBM magnetic tape drives except the Model 7340 Hypertape Drive and the new 2400 Series units. Code conversion between UNIVAC 1050 internal code and IBM 6-bit BCD code is not automatic, as in the Uniservo IV C, but must be done by subroutines if needed. The conversion is facilitated by the automatic translate instruction.

A Uniservo VI C Magnetic Tape Subsystem consists of a Synchronizer Unit, from 1 to 4 Control Units, and from 1 to 16 Uniservo VI C Magnetic Tape Handlers (1 to 4 tape handlers can be connected to each Control Unit). Each subsystem fully occupies two input-output channels. The controllers are two-way units, making possible simultaneous read and write operations involving any two tape handlers in the subsystem. The Uniservo VI C tape handler can read only in the forward direction and cannot perform any skip or search operations.

Recording density can be either 200, 556, or 800 rows per inch, providing peak data transfer rates of 8,500, 23,700, or 34,100 characters per second, respectively. Each tape row consists of six data bits and one parity bit. Block length is variable from one character to the capacity of one core storage module (4,096 characters for the Model III Central Processor and 8,192 characters for the Model IV). The base address of the input-output area, as well as a block character count, is contained in the appropriate I/O Channel Register. The External Function instruction specifies a read or write operation, the unit involved, the recording density, and whether or not an external interrupt shall occur upon successful completion of the operation. This instruction is also used to test or reset indicators that show which condition caused an interrupt.

Two-gap magnetic heads are used, permitting a read-after-write parity check on recording. A longitudinal parity check character is written after the last data row in each block. Both longitudinal and lateral (row) parity are checked during each

.12 Description (Contd.)

read or write operation. Abnormal conditions (such as parity errors, control busy, or end of tape marks) and successful completion of an operation (optional) cause interrupts and set testable indicators. By testing the status of the indicators, the program can determine the cause of interruption and jump to a subroutine to handle the condition.

Simultaneity is discussed in Sections 777:111 and 777:112, Simultaneous Operations.

.14 First Delivery: . . . . January 1965.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . vacuum capstan.
.212 Reservoirs -
Number: . . . . . 2.
Form: . . . . . vacuum columns.
Capacity: . . . . . approximately 2 feet of tape.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . magnetic head.
.222 Sensing system: . . . . magnetic head.
.223 Common system: . . . 2-gap head provides read-after-write parity checking.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read.
Distance: . . . . . 0.25 inch after write head.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

§ 093.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape with magnetizable surface.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . row, at 200, 556, or 800 (optional) rows per inch.
.322 Parallel by: . . . . . 7 tracks.
.324 Track use -
Data: . . . . . 6.
Redundancy check: . 1 (parity).
Timing: . . . . . 0.
Unused: . . . . . 0.
Total: . . . . . 7.
.325 Row use, per N-character block -
Data: . . . . . 1 to N.
Redundancy check: . 1.
Timing: . . . . . 0.
Control signals: . . . 0.
Unused: . . . . . 0.
Interblock gap: . . . 0.75 inch.

.33 Coding: . . . . . binary image, using 1 tape row per UNIVAC 1050 character.

.34 Format Compatibility: with all IBM 700, 1400, and 7000 series systems via IBM 727, 729, and 7330 Magnetic Tape Units; with UNIVAC III, 490, 1107, or other 1050 systems using Uniservo III C, IV C, or VI C Tape Handlers; and with other "IBM compatible" tape units.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.5 inch.
.352 Length: . . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . Uniservo VI C Control Unit, Type 0858-01.
Uniservo VI C Synchronizer Unit, Type 5307-00.

.42 Connection to System

.421 On-line: . . . . . a Uniservo VI C Subsystem consists of a Synchronizer Unit and from 1 to 4 Control Units. Each subsystem fully occupies 2 input-output channels. Two subsystems may be connected to Model III systems; four to Model IV systems.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1 to 4 tape handlers per Control Unit; 1 to 16 per Synchronizer Unit.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 character to the capacity of one core storage module (4,096 characters for the Model III Central Processor, 8,192 characters for the Model IV).
.442 Input-output areas: core storage.
.443 Input-output area access: . . . . . each character.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 character to the capacity of one core storage module (4,096 characters for the Model III Central Processor; 8,192 characters for the Model IV).
.512 Block demarcation -
Input: . . . . . interblock gap on tape or character count in I/O Channel Register.
Output: . . . . . character count in I/O Channel Register.

.52 Input-Output Operations

.521 Input: . . . . . read 1 block of data forward only at 200, 556, or 800 rows per inch.
.522 Output: . . . . . write 1 block of data forward only at 200, 556, or 800 rows per inch; external interrupt upon completion is optional.
.523 Stepping: . . . . . 1 block backward (backspace); approximately 5 inches forward (to skip and erase defective tape areas).
.524 Skipping: . . . . . none.
.525 Marking: . . . . . end-of-file mark; interblock gap.
.526 Searching: . . . . . none.

.53 Code Translation: . . none; binary images are transferred.

.54 Format Control: . . . by program.

.55 Control Operations

Disable: . . . . . yes, following rewind with interlock.
Request interrupt: . . yes.
Rewind: . . . . . yes.
Unload: . . . . . no.

§ 093.

.56 Testable Conditions

Disabled:	yes.
Busy device:	yes.
Output lock:	yes.
Nearly exhausted:	no.
Busy controller:	yes.
End of medium marks:	yes.
End of file:	yes.
Rewinding:	yes.

.6 PERFORMANCE

.61 Conditions

I:	reading or writing at 200 rows per inch.
II:	reading or writing at 556 rows per inch.
III:	reading or writing at 800 rows per inch.

.62 Speeds

.621 Nominal or peak speed -

I:	8,500 char/sec.
II:	23,700 char/sec.
III:	34,100 char/sec.

.622 Important parameters -

Recording density:	200, 556, or 800 (optional) rows/inch.
Tape speed:	42.7 inches/sec.
Full rewind time:	180 seconds.
Inter-block gap:	0.75 inch.
Start plus stop time:	24 msec.

.623 Overhead: 17.6 msec per block (continuous tape motion).

.624 Effective speeds

I:	8,500N/(N + 150) char/sec.
II:	23,700N/(N + 417) char/sec.
III:	34,100N/(N + 600) char/sec.

where N is the number of characters (i.e., tape rows) per block (see graph).

.63 Demands on System

Component	Condition	Msec per character	or Percentage of Data Transfer Time
Model III Core Storage:	I	0.0045	4.0
	II	0.0045	11.1
	III	0.0045	16.0
Model IV Core Storage:	I	0.0020	1.6
	II	0.0020	5.8
	III	0.0020	6.7

.7 EXTERNAL FACILITIES

.71 Adjustments: none.

.72 Other Controls

Function	Form	Comment
Rewind:	switch/light	rewinds and positions tape.
Forward:	switch/light	moves tape forward.
Backward:	switch/light	moves tape backward.
Change tape:	switch/light	moves tape to load point.

.73 Loading and Unloading

.731 Volumes handled: 2,400 feet per reel; for 1,000-character blocks, 5,000,000 characters at 200 char/inch, 11,300,000 characters at 556 char/inch, or 14,400,000 characters at 800 char/inch.

.732 Replenishment time: 0.5 to 1.0 minute; tape unit needs to be stopped.

.734 Optimum reloading period: 11 minutes.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Recording:	read-after-write parity check	set indicator and interrupt.
Reading:	lateral and longitudinal parity check	set indicator and interrupt.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	all codes are valid.	
Exhausted medium:	check	set indicator and interrupt.
Imperfect medium:	see Recording.	
Timing conflicts:	check	set indicator and interrupt.

Note: The type of error is determined by testing individual indicators.

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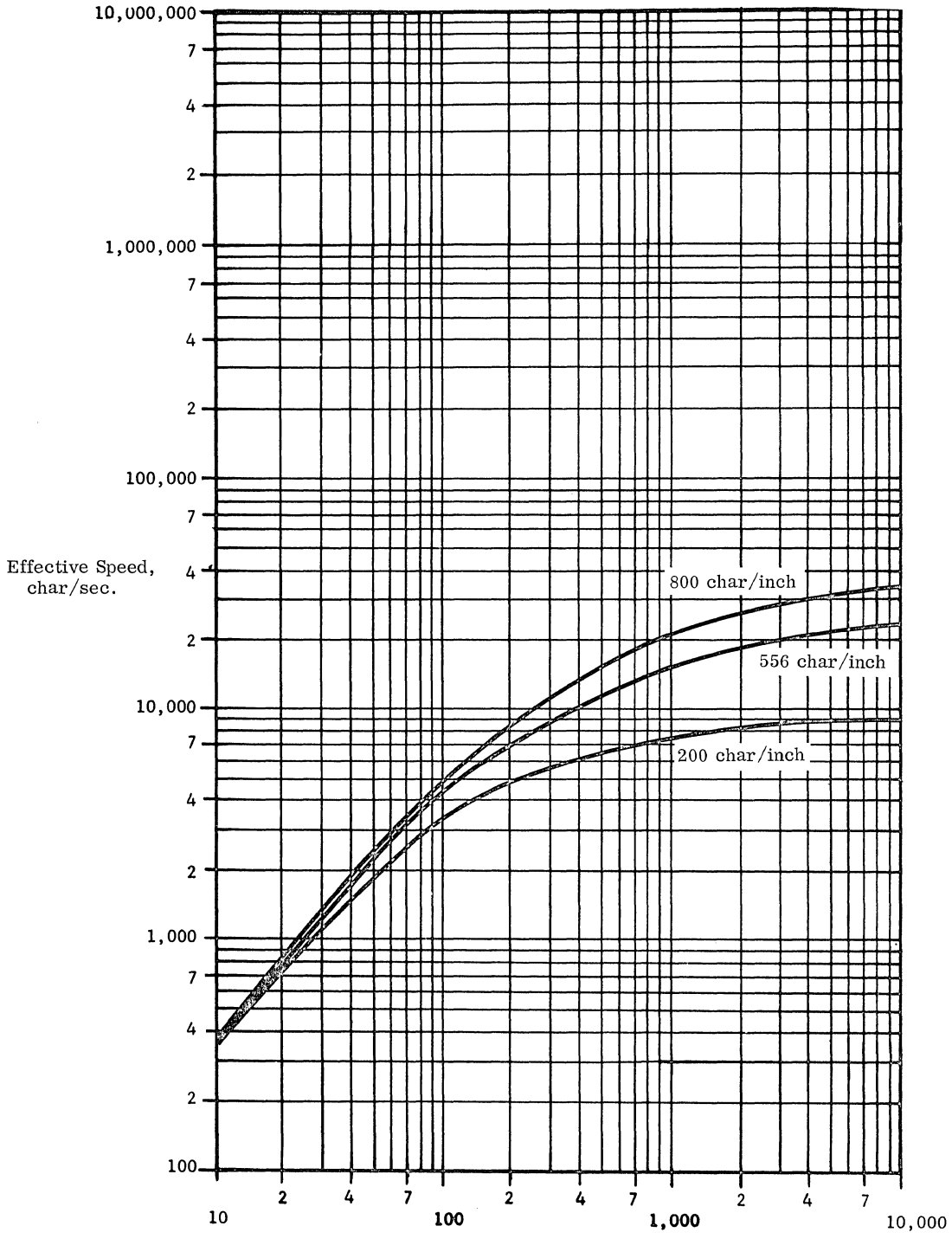
EFFECTIVE SPEED:

UNISERVO VI C MAGNETIC TAPE HANDLER



Note: Effective speeds are based upon continuous operation, with no stops between blocks.

INPUT–OUTPUT: STANDARD COMMUNICATIONS SUBSYSTEM

§ 101.

.1 GENERAL

.11 Identity: . . . . . Standard Communications Subsystem, consisting of 1 to 64 Communication Line Terminals connected to a Communication Multiplexer.

.12 Description

The Standard Communications Subsystem enables the UNIVAC 1050 to receive and transmit data via any common carrier, in any standard code of up to 8 levels, at any standard rate of transmission up to 4,800 bits per second. It can receive or transmit data via high-speed, medium-speed, or low-speed lines in any combination.

The two principal components of the Standard Communications Subsystem are the Communication Line Terminals (CLT's), which are connected directly to the communication facilities, and the Communication Multiplexer, which links up to 64 CLT's to the Central Processor. One or two Communication Multiplexers can be connected to the Model III Central Processor, and up to 8 to the Model IV.

Communication Line Terminals

A CLT is required for each input line and each output line to be connected to a UNIVAC 1050 system. There are three basic types of input and output CLT's: low-speed (up to 300 bits per second), medium-speed (up to 1,600 bits per second), and high-speed (2,000 to 4,800 bits per second). The characteristics of the available CLT models are summarized in Table I.

A special type of output CLT is the CLT-Dialing, which enables the Central Processor to establish communication with a particular remote point via the common carrier's switching network. Each CLT-Dialing requires one output position on the Communication Multiplexer and is always used in conjunction with another output CLT, an input CLT, or (for two-way communication) both.

Communication Multiplexer

The Communication Multiplexer is available in five different models, capable of connecting the following maximum numbers of Communication Line Terminals to a single UNIVAC 1050 input-output channel:

C/M-4: 2 input and 2 output CLT's

C/M-8: 4 input and 4 output CLT's

C/M-16: 8 input and 8 output CLT's

.12 Description (Contd.)

C/M-32: 16 input and 16 output CLT's

C/M-64: 32 input and 32 output CLT's

When several CLT's simultaneously request access to Core Memory, the Communication Multiplexer assigns priorities and lets the Central Processor know which CLT has been granted access.

Clocks

All CLT's require a timing source to establish the proper sequencing of data bits or characters as they are transferred to and from the communication facilities. Medium-speed parallel input CLT's, dialing CLT's, and high-speed synchronous input and output CLT's use the modem or dialing unit to which they are connected as their timing source, while all other CLT's use electronic clocks which are components of the Standard Communications Subsystem as their timing source.

Each asynchronous input CLT has its own clock; however, all asynchronous or parallel output CLT's which operate at the same speed share a common clock. Up to six output clocks are provided with the Standard Communications Subsystem.

Registers

Communication facilities usually operate in a bit-serial, character-serial mode in contrast to UNIVAC 1050 systems, which handle data characters in a bit-parallel, character-serial mode. To accomplish compatibility, input CLT's are equipped with an assembly register in which the bits comprising each character, as they are received, are assembled into a complete data character for parallel transfer to the 1050. Output CLT's are similarly equipped with a disassembly register.

When low-speed CLT's are used, data must be transferred between the CLT and the Central Processor during the time interval between the arrival of the last data bit of one character and the start bit of the next character. Medium-speed and high-speed CLT's, however, contain a single-character buffer or queuing register, which permits a time interval corresponding to the length of a complete data character to elapse between data transfers to or from the Central Processor.

Buffer

Buffer areas are program set in core storage and may be either 64 or 128 characters in length. When data is being sent or received, an interrupt signal is automatically generated every 32 or 64 characters, depending upon the length of the buffer. This enables the 1050 Central Processor to load

§ 101.

.12 Description (Contd.)

or unload one half of a buffer while the other half is being filled or emptied by a communications device. An interrupt is also generated at the end of a message to enable unloading of a partially full buffer.

Special Features

- Automatic parity checking and generation, under program control, for each line.
- Automatic insertion of a sixth bit — 0 for figures and 1 for letters — when receiving a message in the 5-level Baudot code. This permits programmed translation using the Translate instruction.
- Automatic generation of an interrupt upon recognition of any program-set special 6-, 7-, or 8-bit character.

Simultaneity

All Communication Line Terminals may be active simultaneously. In addition, messages may be transmitted or received while any other peripheral subsystem is operating or while the Central Processor is computing.

.12 Description (Contd.)

Types of Communication Service

Through the use of the appropriate Communication Line Terminals and associated common carrier equipment, any or all of the following types of communication service can be tied into a UNIVAC 1050 system:

- Private Line Teletypewriter: up to 100 words per minute; simplex, half duplex, or full duplex.
- Teletypewriter Exchange Service (TWX): 100 words per minute; half duplex.
- Direct Distance Dialing (DDD) or Wide Area Telephone Service (WATS): 110 to 2,000 bits per second; half duplex.
- Private Line Telephone: 1,200 bits per second and up; full or half duplex.

TABLE I: COMMUNICATION LINE TERMINAL CHARACTERISTICS

Type No. (Input only)	Type No. (Output only)	Code Level (Bits/char)	Mode	Timing	Speed
CLT-51L	CLT-50L	5	Bit serial	Asynchronous	Up to 300 bits/sec
CLT-81L	CLT-80L	6, 7, or 8	Bit serial	Asynchronous	Up to 300 bits/sec
CLT-81M	CLT-80M	5, 6, 7, or 8	Bit serial	Asynchronous	Up to 1,600 bits/sec
CLT-81P	CLT-80P	up to 8	Bit parallel	Timing Signal	Up to 75 char/sec
CLT-81H	CLT-80H	5, 6, 7, or 8	Bit serial	Synchronous	2,000 to 4,800 bits/sec.
	CLT-Dialing	4	Bit parallel	Timing Signals	Determined by common carrier

Note: "Asynchronous" means that start and stop bits are used with each character to establish timing; "Synchronous" means that timing characters are used at predetermined intervals between data characters.

INPUT–OUTPUT: UNIVAC 1004

§ 102.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 Card Processor; Models I, II, and III.
UNIVAC 1004 Adapter.

.12 Description

The UNIVAC 1004 is a small plugboard-programmed computer with 961 positions of core storage. It can be connected to the UNIVAC 1050 by means of the 1004 Adapter, enabling transmission of data, in one direction at a time, between 1050 core storage and 1004 core storage. While the 1004 Subsystem does provide a means of attaching several low-speed peripherals to a single 1050 input-output channel, as well as data editing, code translation, and similar data manipulation facilities outside the 1050 program, the primary aim of this configuration seems to be as an "expansion package" for UNIVAC 1004 installations. All operations must be initiated by the 1050 program, or by the plugboard wiring under control of the 1050 program; i.e., the UNIVAC 1004 cannot act as an inquiry station for the 1050. When it is not in use as an on-line peripheral, the UNIVAC 1004 can be used as an off-line data processor, under sole control of its plugboard wiring.

Some of the important characteristics of the 1004 are:

- Plugboard programming.
- 961 positions of core storage.
- 31, 47, or 62 program steps (instructions).
- 8 μsec cycle time for the 1004 Model I; 6.5 μsec cycle time for Models II and III.
- Editing and decimal arithmetic facilities.
- Maximum card reading rate of 400 or 615 cards/minute, depending upon the model.
- Maximum printing rate of 400 or 600 lines/minute, depending upon the model.
- 132 alphanumeric printing positions.

.12 Description (Contd.)

- 63 character printing set.
- Optional card punch — 200 cards/minute.
- Punched paper tape units available — 400 char/sec reading and 110 char/sec punching.
- Magnetic tape units available.

For more detailed information on the capabilities and performance of the UNIVAC 1004, see Computer System Report 770.

A UNIVAC 1004 operation is initiated in the same way as other peripherals: by the External Function instruction. Six basic functions are provided, such as read a card, print a line, punch a card, etc. In addition, upon initiation of a UNIVAC 1004 operation by the 1050 (using the operation code 00), the 1004 Adapter accesses the first character of the input or output field in the 1050 (whose location must be set in the appropriate I/O Channel Register), interprets this character according to plugboard wiring, and causes certain hubs of the 1004 plugboard panel to emit pulses which control the operation of the 1004. Data is transmitted character-by-character to and from the 1050, interlocking core storage for only one cycle per transmitted character. Except for data transmission, the 1004 operates independently of the 1050.

The 1004 Subsystem requires the exclusive use of one UNIVAC 1050 input-output channel and can run simultaneously with all other peripherals. Two 1004 Subsystems can be connected to the UNIVAC 1050 Model III Central Processor, and up to eight 1004 Subsystems to the Model IV Processor.

There are no parity or other checking devices in the 1004, although characters read by the card reader can be checked for validity by programming. Parity bits are generated by the 1004 Adapter prior to transmission to the 1050. The parity bit for each character sent from the 1050 is also transmitted and is checked in the adapter. Parity errors, malfunctions, or other errors cause an interrupt signal to be sent to the 1050 Central Processor, as in other peripheral devices, and can cause a branch to a recovery routine.

SIMULTANEOUS OPERATIONS: MODEL III PROCESSOR

§ 111.

Each peripheral subsystem in a UNIVAC 1050 Model III system is permanently connected to a separate input-output channel (two channels are required for each tape subsystem), and there are a maximum of eight channels available. Unlike many currently-available computer systems, the UNIVAC 1050's control circuitry does not conduct a priority scan of all the input-output channels during each core storage cycle to determine whether that particular cycle shall be allocated to one of the channels or to the central processor. Consequently, simultaneity of operations is not as extensive nor as clearly defined as one might expect in a system having this number of data channels. However, in certain cases up to six operations can be overlapped (see Figure 1).

The synchronizers for the card reader, card punch, and printer are built directly into the Model III Processor and are connected to channels 1, 2, and 0, respectively. Internal circuitry permits the simultaneous operation of these three peripherals (even when the printer is unbuffered). Simultaneity with other subsystems is described later in this section.

Channels 4 and 5 are reserved for a magnetic tape subsystem, and channel 6 is usually assigned to a Fastrand subsystem. The design of the Uniservo III A, Uniservo IV C, and Fastrand synchronizers preclude the simultaneous operation of these units with like subsystems or with the card reader or punch. The Uniservo VI C can operate simultaneously with the card reader but not with the card punch.

All simultaneous operations are, of course, limited by the maximum gross data transfer rate of the central processor, which is 222,000 characters per second.

The usual peripheral assignment of input-output channels is indicated below. Deviations from these assignments could require RPQ's and modifications of the standard software, and could also limit program compatibility with other 1050 systems.

Input-Output Channel	Usual Peripheral Subsystem Assignment
0	Printer (Synchronizer internal to processor).
1	Card Reader (Synchronizer internal to processor).
2	Card Punch (Synchronizer internal to processor).
3	Communications.
4 and 5	Magnetic Tape (III A, IV C, or VI C).
6	Fastrand.
7	Punched Paper Tape, UNIVAC 1004 On-Line Card Processor, or second printer.

Each input-output operation is initiated by an External Function (XF) instruction which specifies the input-output channel, unit, operation to be performed (read a card, print a line, etc.), and such details as whether the processor shall be interlocked for the duration of the operation and whether the automatic interrupt upon successful completion of an operation shall be inhibited. Indicators are set for various errors or malfunctions and may be tested or reset by means of the XF instruction. The base address of each input-output area is set by the program in the appropriate I/O Channel Register, and control of the peripheral subsystems is accomplished through the system of interrupts and testable indicators discussed in Paragraph 777:051.12. In general, the Processor is free to resume internal processing after execution of an External Function instruction, except for the core storage accesses required for transmission of data between the Processor and the peripherals, and the control functions necessary for proper handling of the input-output devices.

Some important considerations regarding simultaneous operations for the UNIVAC 1050 system using the Model III Central Processor are:

- Any subsystem can operate simultaneously with internal processing.
- The card punch, card reader, and printer can operate simultaneously.
- Subsystems connected to channels 3 and 7 (see normal channel assignments above) can operate simultaneously with any other subsystems.

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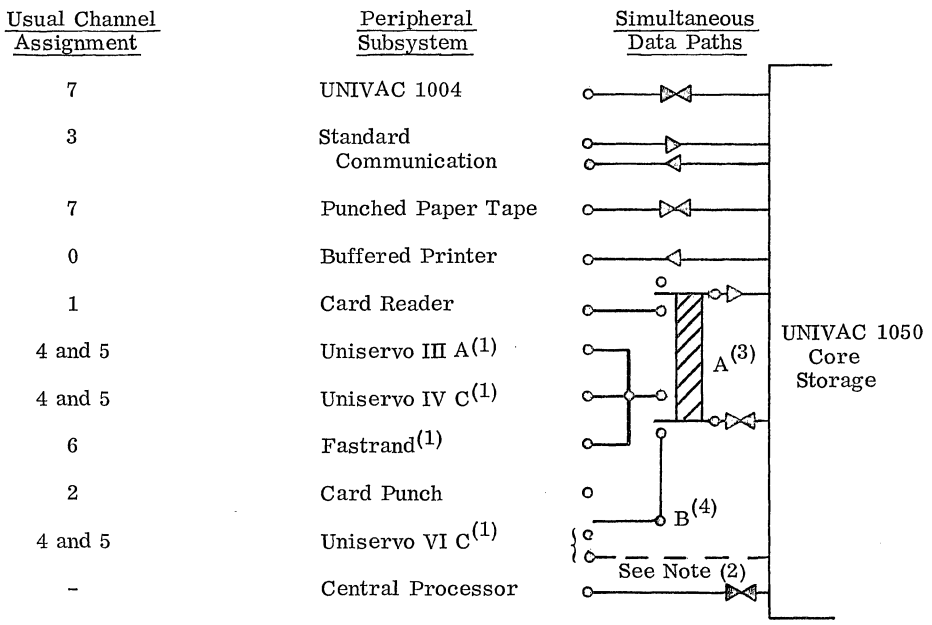
- The buffered printer can operate simultaneously with any other peripheral, including additional printers.
- In general, only one-way data transfers are possible; e.g., the Fastrand unit can either read or write, but cannot do both simultaneously. The two exceptions to this generality are the Standard Communications Subsystem, which can receive and transmit messages simultaneously, and the Uniservo VI C Magnetic Tape Subsystem, which can perform one read and one write operation simultaneously.
- Magnetic Tape Subsystems using Uniservo III A's or IV C's or the Fastrand Mass Storage Subsystem can operate simultaneously only with peripherals attached to channels 3 and 7 (see above) and the buffered printer. The card reader and card punch must be brought to a halt before issuing input-output instructions to these magnetic tape or drum peripherals.
- The card punch cannot operate simultaneously with any Magnetic Tape Subsystem or with a Fastrand Subsystem.

Violation of the above considerations will not result in a non-recoverable loss of data. If non-allowable simultaneous data transfers are requested, or if the maximum data rate of the processor is in danger of being exceeded, a "memory-overload-anticipated" interrupt is generated that inhibits the issuance of the second command until the first is completed.

A schematic summary of the 1050 Model III's capabilities for simultaneous operations is presented in Figure 1. There is no significance to the order of listing since no priority scan is made.

FIGURE 1: SIMULTANEOUS OPERATIONS — UNIVAC 1050 MODEL III



Notes:
(1) A Fastrand unit can execute a positioning operation (no data transfer) simultaneously with the operation of any magnetic tape unit.

(2) Any two Uniservo VI C's can read and write simultaneously.

(3) "Switch" A indicates that the card reader, card punch, and Uniservo VI C cannot operate simultaneously with the Uniservo III A, Uniservo IV C, or Fastrand.

(4) "Switch" B indicates that the card punch cannot operate simultaneously with a Uniservo VI C.

SIMULTANEOUS OPERATIONS: MODEL IV PROCESSOR

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The 1050 Model IV Processor, like the Model III Processor, can have up to eight input-output channels, each permanently connected to a peripheral subsystem (magnetic tape subsystems require two channels); but the simultaneity of operations possible with Model IV is more extensive than with Model III.

This increased simultaneity is primarily due to different synchronizers for the card reader and card punch. These synchronizers, as well as the printer synchronizer, are not built directly into the Model IV Processor as they are in the Model III. The new synchronizers permit the card punch and card reader to operate simultaneously with any other peripheral device.

Each input-output operation is initiated by an External Function (XF) instruction which specifies the input-output channel, unit, operation to be performed (e.g., read a card, print a line, etc.), and such details as whether the processor shall be interlocked for the duration of the operation and whether the automatic interrupt upon successful completion of an operation shall be inhibited. Indicators are set for various errors or malfunctions and may be tested or reset by using the XF instruction. The base address of each input-output area is set by the program in the appropriate I/O Channel Register, and control of the peripheral subsystems is accomplished through the system of interrupts and testable indicators discussed in Paragraph 777:051.12. In general, the Processor is free to resume internal processing after execution of an External Function instruction, except for the core storage accesses required for transmission of data between the Processor and the peripherals, and the control functions necessary for proper handling of the input-output devices.

Each character transmitted to and from an I/O synchronizer requires one core storage cycle, limiting the maximum gross data transfer rate of the Model IV Processor to 500,000 characters per second between core storage and peripheral subsystems.

Some important considerations regarding simultaneous operations for the UNIVAC 1050 system using the Model IV Central Processor are:

- Total data transfer rate cannot exceed 500,000 char/sec.
- Any subsystem can operate simultaneously with internal processing.
- In general, only one-way data transfers are possible; e.g., the Uniservo III A Magnetic Tape Subsystem can either read or write, but cannot do both simultaneously. The two exceptions to this generality are the Standard Communications Subsystem, which can receive and transmit messages simultaneously, and the Uniservo VI C Magnetic Tape Subsystem, which can perform one read and one write operation simultaneously.
- Data transfers involving the Uniservo III A Magnetic Tape Subsystem, the Uniservo IV C Magnetic Tape Subsystem, and the Fastrand Mass Storage Subsystem are mutually exclusive; i.e., only one of the three can operate at a time. However, any one of these three subsystems can operate simultaneously with any group of subsystems not including one of these three.

Some typical time demands on the central processor by the various peripherals are shown in Table I. Additional timing information is presented in the sections on particular peripheral devices (Sections 777:043 through 777:102).

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TABLE 1: MODEL IV CENTRAL PROCESSOR USAGE BY PERIPHERAL SUBSYSTEMS

Peripheral Subsystem	Cycle Time, msec	Central Processor Usage†	Conditions
Card Reader, 800 cards/min	75	0.91%	reading full 80-column cards.
Card Punch, 300 cards/min	200	0.34%	punching 80-column cards.
Printer, 700 lines/min	86	1.20%	printing full lines with a full character set and spacing one line.
Uniservo III A, 133,000 char/sec	16.8	25.6%	1200-character blocks.
Uniservo IV C, 90,000 char/sec	29.4	14.6%	1200-character blocks.
Uniservo VI C, 34,100 char/sec	58.8	7.3%	reading or writing 1200-character blocks.
	58.8	14.6%	reading and writing 1200-character blocks simultaneously.
Fastrand	93*	1.18%*	*
Punched Paper Tape, 1000 char/sec	100	0.72%	100-character blocks.
UNIVAC 1004 Model I	150	0.63%	reading cards at 400 cards/min.
	150	0.69%	printing at 400 lines/min.
	300	0.31%	punching cards at 200 cards/min.

† Includes execution of standard I/O routines.

* The figures shown are for an average random access time of 92 msec and a block length of one sector. Central Processor usage could vary from 0.71% for maximum access time to almost 100% for large blocks and minimum access time.

INSTRUCTION LIST

§ 121.

1st CHARACTER	2nd CHARACTER		3rd CHARACTER	4th CHARACTER	5th CHARACTER
OPERATION CODE 30–26	INDEX REGISTER 25–23	RES. 22	MAIN STORE 21–13	ADDRESS 12–7	DETAIL 6–1

INSTRUCTION WORD FORMAT

		WRITTEN FORM						DEC. IND.	INTERNAL FORM (OCTAL)			
		30-26							25 23	22	21 7	6 1
TYPE	MNEM CODE	OP CODE	INSTRUCTION	DESCRIPTION	LSD MSD	OPERANDS	NO.	X		M	DETAIL
TRANSFERS	BDa	56	BRING DECIMAL	$(M)_L \rightarrow$ AR, DECIMAL + &	L	M, L, X		0 7	0	0—77777	1/6 0/1* 5 4 0 L 17** 1
	BAa	56	BRING ALPHANUMERIC	$(M)_L \rightarrow$ AR, BINARY	L	M, L, X					0/6 0/1* 5 4 0 L 17** 1
	BT	46	BRING TETRAD	(M) → T	L	M, T, X					0 T 77
	SAa	52	STORE ARITHMETIC REG.	$(AR)_L \rightarrow M_L$	L	M, L, X					0/1* 5 4 0 L 17** 1
	SAR	52	STORE BOTH ARITHMETIC REGISTERS	(AR1, AR2)→M→M−31	L	M , , X					61(110001)
	ST	42	STORE TETRAD	(T) → M	L	M, T, X					0 T 77
	SC	44	STORE CHARACTER	$C_1 \rightarrow$ M	L	M, C, X					0 C 77
	FT	20	FIX TETRAD	$M_1 \rightarrow$ T	L	M, T, X					0 T 77
	TFI	24	TRANSFER BLOCK FROM STORE, INCREMENT	(M, M + 1, M + ---) DST (TET 16)	M	M , , X					20(010000)
	TFR	24	TRANSFER BLOCK FROM STORE, RESET	(M, M + 1, M + ---) DST (TET 16)	M	M , , X					0
	TTI	24	TRANSFER BLOCK TO STORE, INCREMENT	(ORIGIN)→M, M + 1, M + ---	M	M , , X					60(110000)
	TTR	24	TRANSFER BLOCK TO STORE, RESET	(ORIGIN)→M, M + 1, M + ---	M	M , , X					40(100000)
ARITHMETIC	ADa	66	ADD DECIMAL	$(AR) + (M)_L \rightarrow$ AR	L	M, L, X	37, 38				0/6 0/1* 5 4 0 L 17** 1
	ABa	72	ADD BINARY	$(AR)_L + (M)_L \rightarrow M_L$	L	M, L, X	37, 39				0/6 0/1* 5 4 0 L 17** 1
	AMa	62	ADD TO MEMORY	$(AR)_L + (M)_L \rightarrow M_L$, DECIMAL	L	M, L, X	37, 38				0/6 0/1* 5 4 0 L 17** 1
	AT	76	ADD TO TETRAD	(M) + (T)→T	L	M, T, X	39				0 T 77
	AC	60	ADD CHARACTER	C_1 + (M)→M, CARRIES	L	M, C, X	39				0 C 77
	SDa	66	SUBTRACT DECIMAL	$(AR) - (M)_L \rightarrow$ AR	L	M, L, X	37, 38				1/6 0/1* 5 4 0 L 17** 1
	SBa	72	SUBTRACT BINARY	$(M)_L - (AR)_L \rightarrow M_L$	L	M, L, X	37, 39				1/6 0/1* 5 4 0 L 17** 1
	SMa	62	SUBTRACT FROM MEMORY	$(M)_L - (AR)_L \rightarrow M_L$, DECIMAL	L	M, L, X	37, 38				1/6 0/1* 5 4 0 L 17** 1
	MPN	50	MULTIPLY NON-CUMULAT.	(AR2) x (T20, 21)→AR1		, L	37, 38, 40	0		0	0/6 0 5 0 4 3 0 L 7§ 1
	MPC	50	MULTIPLY CUMULATIVE	(AR2) x (T20, 21)→AR1 CUM.		, L					0/6 1 5 0 4 3 0 L 7§ 1
	DV	50	DIVIDE	(AR1) ÷ (AR2)→QTN (TET 20, 21) ; REMAIN.→AR1		, L					1/6 0 5 0 4 3 0 L 7§ 1
COMPARISON	CDa	26	COMPARE DECIMAL	$(AR) : (M)_L$	L	M, L, X	33-36	0 — 7		0—77777	1/6 0/1* 5 4 0 L 17** 1
	CBa	70	COMPARE BINARY	$(AR)_L : (M)_L$	L	M, L, X					1/6 0/1* 5 4 0 L 17** 1
	CC	34	COMPARE CHARACTER	C_1 : M	L	M, C, X					0 C 77
	CT	74	COMPARE TETRAD	(T) : (M)	L	M, T, X					0 T 77
	LC	14	LOGICAL COMPARE	IF M_X HAS A 1 BIT FOR EVERY 1 BIT IN C THEN =	L	M, C, X					0 C 77
SEQUENCE CONTROL	JE	30	JUMP EQUAL	IF I 34 IS SET, M→CC		M, X	34				42(100010)
	JG	30	JUMP GREATER	IF I 33 IS SET, M→CC		M, X	33				41(100001)
	JS	30	JUMP SMALLER	IF I 36 IS SET, M→CC		M, X	36				44(100100)
	JU	30	JUMP UNEQUAL	IF I 35 IS SET, M→CC		M, X	35				43(100011)
	J	30	JUMP	M→CC		M, X					0
	JC	30	JUMP CONDITIONAL	IF I_n = 1, M→CC (SEE INDICATOR LIST)		M, I, X	ALL				I 0 — 77
	JL	32	JUMP LOOP	IF (N) − 1≠ 0, M→CC		M, N, X					N 0 — 77
	JR	10	JUMP RETURN	IF I_n = 1, CC→M; M + 5→CC		M, I, X	ALL				I 0 — 77
	JD	30	JUMP DISPLAY	STOP, DISPLAY M_1, NEXT INSTR. ON RESTART		M, X					60(110000)
	JHJ	30	HALT, THEN JUMP	STOP, M→CC ON RESTART		M, X					20(010000)
SHIFT	BCn	16	BIT CIRCULATE	CIRCULATE n CHAR., 5 BIT POS. LEFT MAX. 7 BIT POS.	L	M, S, X					1/6 5 0 n 3† 4 3 0 S 7 1
	BSn	16	BIT SHIFT	SHIFT n CHAR., 5 BIT POS. LEFT MAX. 4 CHAR. AND 7 POS.	L	M, S, X					0/6 5 0 n 3† 4 3 0 S 7 1
EDIT	LS	64	LOGICAL SUM	$(M_X) \vee C \rightarrow M_X$	L	M, C, X					0 C 77
	LP	54	LOGICAL PRODUCT	$(M_X) \wedge C \rightarrow M_X$	L	M, C, X					0 C 77
	PD	26	PAD BLANKS	BINARY ZEROS→M_L	L	M, L, X					0/6 0 5 0 L 17**
	PD0	26	PAD ZEROS	XS-3 ZEROS→M_L	L	M, L, X					0/6 1 5
	ZS	22	ZERO SUPPRESS	FROM MSD CHANGE PRECEDING 0'S, ,'S AND BLANKS TO BLANKS	M	M, L, X					1/6 0 5
	ZS$	22	ZERO SUPPRESS AND FLOATING $ SIGN	TO $'S	M	M, L, X					0/6 0 5
	ZS*	22	ZERO SUPPRESS WITH ASTERISK FILL	TO *'S	M	M, L, X					1/6 1 5
	ED	52	EDIT	(AR1)→M_L CONTROLLED BY (AR2)	L	M, L, X					1/6 0 5 4 1
	TR	12	TRANSLATE	$(M)_{JL} \rightarrow M_{JL}$ (T18 = ROW ADD.)	L	M, L, X					L 0 — 77

∧ = LOGICAL AND & = SENTINEL
∨ = LOGICAL OR

† 00 IS INTERPRETED BY THE CIRCUITRY AS 04.
§ 000 IS INTERPRETED BY THE CIRCUITRY AS 010.
** 0000 IS INTERPRETED BY THE CIRCUITRY AS 020.

* IF a = 1, BIT 5 = 0; IF a = 2, BIT 5 = 1.

N. B. SUBSCRIPT I INDICATES IMMEDIATE DATA

UNIVAC 1050 INSTRUCTION REPERTOIRE

§ 121.

I/O INST FORMAT

OPERATION	CHANNEL	UNIT	FUNCTION	DETAIL
. XF (040)	X 0 – 7	U 0 – 17	F 0 – 77	D 0 – 7777
30 – 26	25 – 23	22 – 19	18 – 13	12 – 1

INPUT/OUTPUT INSTRUCTIONS AND INDICATORS

UNIT	FUNCTION 18	17	16	15	14	13	EXPANSION OF FUNCTION (DETAIL) 12	11	10	9	8	7	6	5	4	3	2	1
CARD READER	LOCK-OUT PRO-CESSOR	INHIBIT INTERRUPT				FEED AND READ				*b SCAN 72 COLS.	ADVANCE BASE ADDRESS	TRANS-LATE						
CARD PUNCH				FEED PUNCH					SELECT STACKER									
PRINTER				ADVANCE	PRINT		INHIBIT LOADING OF BUFFER	MANUAL PRINT	PRINT 132 CHAR. LINE	PRINT HALF LINE								
UNISERVO III C TAPE UNIT			REWIND (WITH INTER-LOCK)	REWIND	WRITE	READ	WRITE TAPE MARK	LOW DENSITY	BACK-SPACE	SKIP ERASE		TRANS-LATE 0 = BCD 1 = BINARY						
UNISERVO IV C TAPE UNIT								DENSITY										
UNISERVO VI C TAPE UNIT								200 PPI	BACK-SPACE			PARITY MODE						
UNISERVO III A TAPE UNIT								800 PPI										
FASTRAND MASS STORAGE UNIT			STORE DRUM AD-DRESS	POSITION HEAD BAR	WRITE	READ		TRANS. 5 CHAR./ 3 FRAMES	BACK-WARD (WITH READ)	CONTIG. READ OR WRITE		TRANS. ONE CHAR./ FRAME						
								DRUM PREP	COUNT 0 = SECT. 1 = CHAR.	8 CHAR. MASK.	16 CHAR. MASK	SEARCH FOR = OR >	RELEASE DRUM LOCK	TRANS-FER SIGNAL				
							OVERFLOW DRUM PREP			32 CHAR. MASK								
COMMUNICATIONS					EX-TERNAL FUNCTION													

UNIT	FUNCTION 18	13	TESTABLE INDICATORS 12	1
CARD READER	RESET INDI-CATORS		MEMORY OVER-LOAD ANTICI-PATED	UNIT BUSY	NON-READY		CONTROL PARITY	MEMORY PARITY ERROR	*a PHOTO-CELL CHECK ERROR	*d READ STATION ERROR	*e OUTPUT-JAM	*c REGIS. ERROR		
CARD PUNCH									HOLE COUNT ERROR					
PRINTER			DOES NOT APPLY TO BUFFER				DOES NOT APPLY TO BUFFER		CODE WHEEL PARITY ERROR	LINE FEED PARITY ERROR		PAPER LOW OVERRIDE	PAPER LOW	
UNISERVO III C TAPE UNIT									TAPE PARITY ERROR	MEMORY OVER-LOAD OC-CURRED	OFF-LINE	WRITE ERROR	END OF TAPE	TAPE MARK DET.
UNISERVO IV C TAPE UNIT														
UNISERVO VI C TAPE UNIT						*PARITY ERROR ZERO						WRITE ERROR		
UNISERVO III A TAPE UNIT														
FASTRAND						SYNC. BUSY	TRANS-FER SIGNAL		MISSING SECTOR	HEAD COUNT OVER-FLOW	LONG. PARITY ERROR	RECORDED MEMORY ADDRESS ERROR	PHASE SHIFT ERROR	PHASE SHIFT ERROR
COMMUNICATIONS			NON-READY	1 SEC. INTER-RUPT										

* a = COLUMN SERIAL READER-HOPPER EMPTY STACKER FULL * b = COLUMN SERIAL READER ONLY * c = COLUMN SERIAL READER – MISFEED
* d = S1 ON ROW READER * e = S2 ON ROW READER

INDICATOR LIST

Unconditional Jump to M Address

DEC	OCT	
00	00	Unconditional Jump
14	16	Release Operator Interrupt Inhibit and jump to M_x
15	17	Set Operator Interrupt Inhibit and jump to M_x
16	20	Stop, Jump when Console Restart Button is depressed
17	21	Set Tracing Stall and Jump
18	22	Set Sense Indicator 1 to 1 and jump
19	23	Set Sense Indicator 2 to 1 and jump
20	24	Set Sense Indicator 3 to 1 and jump
21	25	Set Sense Indicator 1 to 0 and jump
22	26	Set Sense Indicator 2 to 0 and jump
23	27	Set Sense Indicator 3 to 0 and jump
24	30	Unconditional Jump
*25	31	Release Class 3 Interrupt Inhibit and jump to M_x
26	32	Set I/O Interrupt Inhibit and jump to M_x (Class 3)
27	33	Release I/O Interrupt Inhibit and jump (Class 3) Resets Programmed Inhibit Only)
28	34	Set Decimal Overflow Interrupt Inhibit and jump (Class 2)
*29	35	Release Class 2 Interrupt Inhibit and jump to M_x
*30	36	Release Processor Parity or Abnormal Interrupt inhibit and jump (Class 1)
31	37	Release Decimal Overflow Interrupt Inhibit and jump (Class 2), (Resets Programmed Inhibit Only)

Conditional Jump

Exceptions to conditional jump are 32, 41, 42, 48, and 56. The status of the indicators is unaltered by the JC and JR instructions except d's shown.

DEC	OCT	
32	40	NOOP
33	41	High
34	42	Equal } These four indicators are affected by the comparison instructions: CC, LC, CD, CB, CT.
35	43	Unequal
36	44	Low
37	45	Result of last arithmetic operation was zero
38	46	Result of last decimal arithmetic operation was negative.
39	47	No overflow in last binary add operation or overflow did occur in the last binary subtract operation.
40	50	Decimal Overflow occurred since last test. If the indicator is set to 1, reset it to 0 and jump.
41	51	Store Indicators 33-40 in M_X memory position and proceed to next instruction
42	52	Set Indicators 33-40 from M_X memory position and proceed to next instruction
43	53	Input-Output status test found indicator(s) set to 1
44	54	Test and reset operator interrupt request
45	55	Input-Output Interrupt is inhibited (Class 3)
47	57	Decimal Overflow Interrupt is inhibited (Class 2)
48	60	Stop/Go to control counter when console start is depressed, ignore M used for display.
49	61	Processor Parity and Abnormal Interrupt is inhibited (Class 1) (Manual Switch Only)
50	62	Sense Switch 1 on console is ON
51	63	Sense Switch 2 on console is ON
52	64	Sense Switch 3 on console is ON
53	65	Sense Indicator 1 is set (to 1)
54	66	Sense Indicator 2 is set (to 1)
55	67	Sense Indicator 3 is set (to 1)
56	70	Skip (no operation)
57	71	If Trace Indicator is set to 1, reset Trace Indicator and Trace Stall to 0 and jump
58	72	Jump to M_x if Operator Interrupt is inhibited

*RESETS the inhibit automatically generated when the interrupt occurred.

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DATA CODE TABLE

§ 141.

CARD CODES		COMPAT. TAPE CODE	MACHINE CODE	STANDARD PRINTER CHAR.	OCT.	NO.
80 COLUMN	90 COLUMN					
NO PUNCH	NO PUNCH	NOT USED①	000000	SPACE (NON-PRINT)	00	0
11-5-8	1-3-5-7	10 1101	000001	⌐	01	1
11	0-3-5-7	10 0000	000010	- (MINUS OR HYPHEN)	02	2
0	0	00 1010	000011	0	03	3
1	1	00 0001	000100	1	04	4
2	1-9	00 0010	000101	2	05	5
3	3	00 0011	000110	3	06	6
4	3-9	00 0100	000111	4	07	7
5	5	00 0101	001000	5	10	8
6	5-9	00 0110	001001	6	11	9
7	7	00 0111	001010	7	12	10
8	7-9	00 1000	001011	8	13	11
9	9	00 1001	001100	9	14	12
0-6-8	0-1-3-7-9	01 1110	001101	\	15	13
11-6-8	1-3-5-7-9	10 1110	001110	;	16	14
12-5-8	0-5-7-9	11 1101	001111	⊏	17	15
12	0-1-3-5-7	01 0000①	010000	+ &	20	16
5-8	1-3-7-9	00 1101	010001	: (COLON)	21	17
12-3-8	1-3-5-9	11 1011	010010	. (PERIOD)	22	18
12-0	0-1-3	11 1010	010011	?	23	19
12-1	1-5-9	11 0001	010100	A	24	20
12-2	1-5	11 0010	010101	B	25	21
12-3	0-7	11 0011	010110	C	26	22
12-4	0-3-5	11 0100	010111	D	27	23
12-5	0-3	11 0101	011000	E	30	24
12-6	1-7-9	11 0110	011001	F	31	25
12-7	5-7	11 0111	011010	G	32	26
12-8	3-7	11 1000	011011	H	33	27
12-9	3-5	11 1001	011100	I	34	28
3-8	0-1-5-7	11 1111	011101	= #	35	29
12-6-8	0-1-5-9	11 1110	011110	<	36	30
12-7-8	0-1-3-5-7-9	00 1011	011111	# =	37	31
7-8	0-1-5-7-9	00 1100	100000	@ ' (APOS.)	40	32
11-4-8	0-1	10 1100	100001	*	41	33
11-3-8	0-1-3-5-9	10 1011	100010	$	42	34
11-0	0-3-7-9	10 1010	100011	!	43	35
11-1	1-3-5	10 0001	100100	J	44	36
11-2	3-5-9	10 0010	100101	K	45	37
11-3	0-9	10 0011	100110	L	46	38
11-4	0-5	10 0100	100111	M	47	39
11-5	0-5-9	10 0101	101000	N	50	40
11-6	1-3	10 0110	101001	O	51	41
11-7	1-3-7	10 0111	101010	P	52	42
11-8	3-5-7	10 1000	101011	Q	53	43
11-9	1-7	10 1001	101100	R	54	44
0-5-8	0-1-9	01 1100	101101	% (	55	45
4-8	0-1-3-7	00 1111②	101110	' (APOS.) @	56	46
11-7-8	0-1-7	10 1111	101111	Δ ⑤	57	47
0-2-8	0-1-7-9	01 1010	110000	≠	60	48
0-4-8	0-1-5	01 1101	110001	(%	61	49
0-3-8	0-3-5-9	01 1011	110010	, (COMMA)	62	50
2-8	1-5-7-9	11 0000	110011	& +	63	51
0-1	3-5-7-9	01 0001	110100	/	64	52
0-2	1-5-7	01 0010	110101	S	65	53
0-3	3-7-9	01 0011	110110	T	66	54
0-4	0-5-7	01 0100	110111	U	67	55
0-5	0-3-9	01 0101	111000	V	70	56
0-6	0-3-7	01 0110	111001	W	71	57
0-7	0-7-9	01 0111	111010	X	72	58
0-8	1-3-9	01 1000	111011	Y	73	59
0-9	5-7-9	01 1001	111100	Z	74	60
12-4-8	0-1-3-9	01 1111	111101	) ⌗	75	61
6-8	0-3-5-7-9	00 1110	111110	>	76	62
0-7-8	0-1-3-5	11 1100	111111	⌗)	77	63

THE SECOND STANDARD CHARACTER SHOWN IS OPTIONAL
NOTE: ① 2-8 CARD PUNCH COMBINATION GENERATES 01 0000 OR SPACE WHEN USED WITH COMPATIBLE TAPE. ② 00 1111 = TAPE MARK.

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PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . none, but see entry 777:151.15.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

UNIVAC 1050 Tape Sort (Magnetic Tape)

Reference: . . . . . not published to date.
Record size: . . . . . 1 to 1,024 characters; preset.
Block size: . . . . . 56 to ? characters; preset.
Key size: . . . . . 1 to 10 keys of from 1 to 16 characters each.
File size: . . . . . 1 reel of tape maximum.
Number of tapes: . . . . 3 to 6.
Date available: . . . . . currently in use.
Description:

The UNIVAC 1050 Tape Sort routine is of the generated-program type, using a forward-read-only, polyphase merge technique. The routine is generalized to sort data in various formats (ascending or descending, binary or decimal). The format and priority for each key are specified in parameter lists.

Own coding options permit modification, addition, or deletion of items during both pre-sort and post-sort time. More than one input source is allowed. Rerun points can be established, if desired, which permit restarts when a run needs to be interrupted or when errors occur in the transfer of data.

The 1050 Tape Sort routine is designed to operate most effectively on systems having at least 12K positions of core storage, but it can be run on 8K systems. From three to six tape units (all of the same type) can be utilized, with the operator having the privilege of reducing the number of tape units to be used (but not to less than three) at object time. This permits a sort to be executed, although more slowly, if one of the tape handlers becomes inoperative.

The 1050 Tape Sort must run under control of COORDINATOR (see Section 777:191) and can run concurrently with a second program if sufficient peripheral units and core storage are available.

UNIVAC 1050 Drum Sort

Details of this routine have not been released to date. The parameters (key size, block size, etc.) are expected to be the same as for the Tape Sort.

.14 Report Writing

REGENT - CARD

Reference: . . . . . UNIVAC Publication UP 3932.
Date available: . . . . . currently in use.
Description:

REGENT - CARD is a program generator designed to reduce the amount of programming time necessary to produce report writing programs for UNIVAC 1050 systems. Report specifications are written on standard PAL coding sheets and transcribed to cards. These cards are translated by the REGENT - CARD report generator into an intermediate deck in PAL machine-oriented language. Control routines for input and output devices are added to the intermediate deck, and the combined deck is assembled in two passes by the PAL CARD assembler, producing a ready-to-run object deck.

The generator has provisions for specifying file formats, decimal arithmetic functions, constants, editing functions, comparisons, and up to nine levels of control breaks. Subroutines and own coding may also be included.

Input files can only be on cards; the object program output can be in the form of printed documents, summary cards, or both.

A card reader, card punch, printer, and a minimum of 8,192 positions of core storage are required to generate a report program using REGENT - CARD.

REGENT - TAPE

Reference: . . . . . UNIVAC Publication UP 3932.
Date available: . . . . currently in use.
Description:

REGENT - TAPE includes everything that REGENT - CARD does (see above) and, in addition, can incorporate all input-output control routines on the PAL Library Tape.

The report specification cards are translated directly into an object deck by the PAL Tape Assembler in one of two forms — one for running under control of COORDINATOR; the second for running separately. If assembled for running with COORDINATOR, a report writing program can run with a second program on a time-shared basis provided that sufficient core storage and peripheral units are available.

§ 151.

.14 Report Writing (Contd.)

A card reader, a printer, two magnetic tape units (of the same type), and a minimum of 8,192 positions of core storage are required to generate a report program using REGENT - TAPE. Summary cards can be punched if a card punch is included in the system.

REGENT - DRUM

Details of this report generator have not been released to date; however, it is expected to be functionally the same as REGENT - TAPE.

.15 Data Transcription

The data transcription facilities furnished for the UNIVAC 1050 are oriented primarily toward providing the necessary format conversions when using the 1050 as an off-line satellite system for the UNIVAC III, 1107, or 490. Facilities announced to date are tape-to-card, card-to-tape, and tape-to-print.

.16 File Maintenance

The library maintenance routine MARION originally announced for the UNIVAC 1050 system is being discontinued in favor of two routines called AJAX and OPUS.

AJAX is designed to maintain tape or card libraries of source coding; OPUS is designed to maintain tape or card libraries in object coding. A single library may contain both object and source coding, with the different sections being maintained by the appropriate routine.

.17 Other

Tape System Diagnostics

Reference: . . . . . not published to date.
Date available: . . . . . October, 1964.
Description:

DUMP is a routine contained on the PAL Library Tape which can be called into any program assembled by PAL TAPE at assembly time, enabling selected portions of the contents of core storage to be printed. The routine is entered by the SNAP macro instruction, which can cause:

- From one character to the entire contents of core storage to be printed in either alphanumeric or octal format.
- The contents of the entire tetrad area (first 256 positions of core storage) or just the arithmetic and index registers to be printed in addition to the selected area; printing may be in either alphanumeric or octal format.

The PCALL routine is contained on the PAL Library Tape and permits the conditional or unconditional printing of the value of a designated field. The routine is entered by the PRIN macro instruction, which causes the value of the field specified (by label) to be printed, depending upon the results of a binary or decimal comparison with a specified constant. Comparisons can be for equal, unequal, greater-than, or less-than conditions. Unconditional printing of the field can also be specified.

The DUMP and PCALL routines and linkages to them can be eliminated from the program only by deletion and re-assembly.

PROCESS ORIENTED LANGUAGE: COBOL–61

§ 161.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1050 COBOL.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corporation.

.13 Reference: . . . . . none published to date.

.14 Description

Detailed language specifications for UNIVAC 1050 COBOL are not available to date; however, UNIVAC states that it will be implemented in accordance with the specifications for COBOL-61 Extended as published November 20, 1962. UNIVAC plans to include all of Required COBOL-61 as defined in X3.4 COBOL Information Bulletin #3, published February 5, 1964, and all the extensions accepted by the CODASYL Committee on November 1, 1963.

UNIVAC expects the minimum configuration for COBOL compilation to include a printer, card reader, four tape units (all of the same type), and a minimum of 16,384 positions of core storage.

.141 Availability: . . . . . first quarter of 1965.

PROCESS ORIENTED LANGUAGE: FORTRAN IV

§ 162.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1050 FORTRAN.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corporation.

.13 Reference: . . . . . none published to date.

.14 Description

Detailed language specifications for UNIVAC 1050 FORTRAN are not available to date, but UNIVAC states that it will be basically FORTRAN IV. UNIVAC expects the minimum configuration for compilation to include a printer, a card reader, four tape units (all of the same type), and a minimum of 16,384 positions of core storage.

.141 Availability: . . . . . first quarter of 1965.

MACHINE ORIENTED LANGUAGE: PAL

§ 171.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1050 PAL Assembly Language.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corporation.

.13 Reference: . . . . . UNIVAC Publication UP 2590.

.14 Description

PAL will probably be the most widely used coding system for the UNIVAC 1050. It is a symbolic machine-oriented language, and when used in conjunction with the PAL Library Tape, it has powerful macro-generating abilities. There are no differences in the coding between systems using the Model III and Model IV Central Processors.

Using the PROC, NAME, and DO directives, routines can be written which will generate the appropriate coding when a user-defined macro code is given. The routines can be included in the program itself or placed on the Library Tape for future reference.

Standard routines for the control of all input-output devices, as well as for file control of magnetic tape files, are included on the PAL Library Tape. Communication between the program and input-output control routines is by subroutine linkages except for magnetic tape functions. Macro and pseudo instructions exist for reading, writing, and file control on the magnetic tape units.

Five translators are available: PAL JR, PAL CARD, PAL TAPE, PAL DRUM, and PAL 1004.

PAL JR and PAL CARD use restricted versions of the basic PAL language and are intended for card-oriented systems. The limitations and special considerations affecting the use of these two translators are pointed out in the appropriate Program Translator sections (see Sections 777:182 and 777:183).

PAL TAPE is intended for tape-oriented systems having at least two magnetic tape units and utilizes the full PAL language as described in this section. The PAL TAPE translator is described in Section 777:181.

Complete details have not been released as yet on PAL DRUM and PAL 1004, but they are intended for systems having a Fastrand Mass Storage subsystem or an on-line UNIVAC 1004 subsystem, respectively.

All material in this report section applies to the PAL language as implemented for a tape-oriented system (PAL TAPE). The major language

.14 Descriptions (Contd.)

restrictions and differences to be considered when using the other PAL translators are discussed in the appropriate Program Translator sections.

.15 Publication Date: . . . . November 1963.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . see coding form, Page 777:171.900.

.22 Legend

Sequence: . . . . . first 3 digits for page number; next 2 for line number; last one for insertions.

Label: . . . . . may be blank or may contain a symbolic tag. (If a period appears in column 7 followed by a blank in column 8, the rest of the line is treated as a comment.)

Operation: . . . . . contains a mnemonic instruction code, a data-defining code, a library call, or an assembly control instruction code.

Operands: . . . . . contains symbolic or absolute descriptions (separated by commas) of the Index Register, Main Store Address, and Detail portions of an instruction, in free form.

Comments: . . . . . comments can follow the terminating space of the Operands field.

Program-ID: . . . . . must contain the program name. Columns 81-90 are ignored by the assembler in 90-column systems.

.23 Corrections

.231 Insertions: . . . . . at bottom of page; resulting lines must then be sorted into sequence prior to assembly.

.232 Deletions: . . . . . cross out offending line.

.233 Alterations: . . . . . erase and correct.

.24 Special Conventions

.241 Compound addresses: . Adjustment ± Base ± Adjustment, where Base and Adjustment are labels, decimal or octal integers, in any combination.

.242 Multi-addresses: . . . . in macros only.

.244 Special coded addresses: . . . . . $ refers to the address of the most significant character of the line in which it is used.

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.245 Absolute addresses: . . any decimal or octal number from zero to the largest number that can be contained in the address field (65,536).

.246 Indexed addresses: . . . decimal or octal number of the index register in the appropriate position of the Operands field (may be a symbolic label if previously defined by EQU).

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . . no practical limit.

.312 Common label formation rule: . . . . yes.

.313 Reserved labels: . . . . no programmer-defined label may begin with X. All I/O control routines have labels beginning with X.

.314 Other restrictions: . . . the three special characters ", +, and - are not allowed in programmer-defined symbols.

.315 Designators: . . . . . none.

.316 Synonyms permitted: . . yes; EQU pseudo.

.32 Universal Labels

.321 Labels for procedures
Existence: . . . . . mandatory if referenced by other instructions, unless address arithmetic is used.
Formation rule —
First character: . . . . any alphabetic except X.
Last character: . . . . numeric or alphabetic.
Others: . . . . . numeric or alphabetic.
Number of characters: . . . . . 1 to 5.

.322 Labels for library routines: . . . . . same as procedures.

.323 Labels for constants: . same as procedures.

.324 Labels for files: . . . . same as procedures.

.325 Labels for records: . . same as procedures.

.326 Labels for variables: . same as procedures.

.33 Local Labels: . . . . . none.

.4 DATA

.41 Constants

.411 Maximum size constants
Integer —
Decimal: . . . . . 5 decimal digits.
Octal: . . . . . 16 octal digits (8 character positions).
Alphabetic: . . . . . 16 characters preceded and followed by
Alphameric: . . . . . same as alphabetic.

.412 Maximum size literals: the only literals allowed, other than address literals, are the incrementing and comparison literals in certain machine instructions and certain expressions of some pseudo operations.

.42 Working Areas

.421 Data layout —
Implied by use: . . . . alternative.
Specified in program: alternative (through use of AREA control instruction).

.422 Data type: . . . . . not required.

.423 Redefinition: . . . . . yes.

.43 Input-Output Areas

.431 Data layout: . . . . . implicit or specified with AREA control instruction.

.432 Data type: . . . . . not required.

.433 Copy layout: . . . . . no.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . . mandatory.
Number: . . . . . 48 (many variations through Detail portion of instruction).
Example: . . . . . ADa = decimal add to arithmetic register a.

.512 Absolute: . . . . . not permitted.

.52 Macro-Codes

.521 Number available —
Input-output: . . . . . 4.
Arithmetic: . . . . . 2.
Math functions: . . . . 2 (multiply and divide).
Error control: . . . . . 0.
Restarts: . . . . . 1.
Diagnostic: . . . . . 2.

.523 New macros: . . . . . inserted into library by special routine.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter: . . pseudo-operation.
Label adjustment: . . . pseudo-operation.
Annotation: . . . . . special card.

.542 Allocation counter —
Set to absolute: . . . . ORIG with absolute decimal or octal address as operand.
Set to label: . . . . . ORIG with label operand (label may have a constant modifier).
Step forward: . . . . . ORIG with $ + D operand, where D is any decimal integer.
Step backward: . . . . . ORIG with $ - D operand, where D is any decimal integer.
Reserve area: . . . . . AREA.

.543 Label adjustment —
Set labels equal: . . . . EQU.
Set absolute value: . . EQU.
Clear label table: . . . none.

.544 Annotation —
Comment phrase: . . . COMMENT card (period in Column 7).
Title phrase: . . . . . no provision.

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.545 Other —
Define data area: . . . AREA.
Define macros: . . . . PROC.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic

.611 Facilities:. . . . . multiply, divide.
.612 Method of call:. . . . . macro.

.62 Special Functions: . . . none to date.

.63 Overlay Control: . . . . by SEG JUMP pseudo.

.64 Data Editing

.641 Radix conversion:. . . . none.
.642 Code translation: . . . . by hardware translation capability.
.643 Format control:. . . . . by hardware editing capabilities.

.65 Input-Output Control

.651 File labels:. . . . . yes.
.652 Reel labels:. . . . . yes.
.653 Blocking: . . . . . yes.
.654 Error control:. . . . . yes.
.655 Method of call:. . . . . jump to standard routine for card and paper tape instructions; macros for magnetic tape instructions.

.66 Sorting: . . . . . UNIVAC 1050 TAPE SORT can be incorporated as a subroutine (see Paragraph 777:151.13).

.67 Diagnostics

.671 Dumps:. . . . . core memory dumps may be called in by operator or connected by program linkage.
.672 Tracers: . . . . . none (extensive trace facilities using console).
.673 Snapshots:

The SNAP macro causes the printing of the contents of a selected area of core storage. The entire tetrad area, or just the Arithmetic and Index Registers, can be printed in addition to the selected area if desired. The size of the selected area to be dumped can be from one character to the total core storage capacity. Printing may be in either octal or alphanumeric format. This routine can be removed from a program only by deletion and reassembly.

The PRIN macro causes the printing of the value of any designated field up to 16 characters in length. The field may be printed unconditionally or conditionally based on the results of a binary or decimal comparison between the designated field and a specified constant. The comparison may be for an equal, unequal, greater than, or less than condition. This routine is removed by deletion and reassembly.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . UNIVAC 1050 PAL Library.
.72 Kinds of Libraries:. . . expandable master.
.73 Storage Form:. . . . . magnetic tape.
.74 Varieties of Contents:. subroutines and macro routines.
.75 Mechanism

.751 Insertion of new item:. AJAX or OPUS routine (see Section 777:151).
.752 Language of new item:. PAL.
.753 Method of call:. . . . . macro.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist:. yes.
.763 Open-closed is optional:. . . . . yes.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Code	Description
SNAP:	causes a selected area of core storage to be printed (see Paragraph .673).
PRIN:.	causes the value of a selected field to be printed (see Paragraph .673).
OPEN*:	initializes a magnetic tape file and checks its label.
CLOSE*:	terminates and deactivates a magnetic tape file.
GET*:	locates a record from a magnetic tape file for processing.
PUT*:	inserts a record in a magnetic tape output file.
RERUN*:	establishes rerun points to provide for restarts in case a program is interrupted or a data transfer error occurs.
DO*:	causes the specified number of subsequent lines of coding to be repeated the specified number of times, either conditionally or unconditionally. The conditions can be for equality, non-equality, greater-than, or less-than between two specified expressions which can be the label of any DO line, the key of a PROC line, a literal constant, or any two of the preceding. An entry in the label field will be used as a counter; it will be incremented by one each time the DO is executed.

Note: Macros marked * are not available in PAL JR, PAL CARD, or PAL 1004.

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.82 Pseudos

Code	Description
BEGIN:	first card of the program; initiates the assembly of a program and can specify whether the program is to be assembled relative to zero (relocatable) or absolute (non-relocatable).
END:	last card of the program; terminates the assembly process and generates a branch to a specified label. (END can also signify the end of a subroutine assembled by the PROC pseudo.)
ORIG:	specifies that the following coding is to be assigned to memory locations starting at the location written in the operand field, or to the next location larger than the expression in the operand field that is an integer multiple of 64 (facilitates handling of card input and output areas).
EQU:	assigns the value written in the operand field to the tag in the label field. The operand can be an absolute or symbolic address or a decimal or octal constant. If $ is used, it refers to the next location available for allocation.
AREA:	defines an area of memory which contains fields or subfields.

.82 Pseudos (Contd.)

Code	Description
PROC*:	identifies the subsequent coding (until an END is reached) as a procedure (subroutine). A single expression is allowed in the Operands field, which can be used as a key for sequence control within the procedure.
NAME*:	allows alternate labels and keys to be assigned to a procedure defined by PROC.
TAPE*:	specifies the parameters necessary to generate the magnetic tape input-output subroutines.
FILE*:	specifies the parameters describing a magnetic tape file which are used to generate the necessary constants and working storage areas.
FORM:	specifies the format for the storage (and conversion if necessary) of the equivalent addresses of labels. The format can be absolute, tetrad number, or index register number.
SEG JUMP:	specifies the end of a segment for overlay control; causes loading to stop at execution time and causes the necessary linkage to be set up for the loader section of COORDINATOR.

Note: Pseudos marked * are not available in PAL JR, PAL CARD, or PAL 1004.

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UNIVAC
DIVISION OF SPERRY RAND CORPORATION

UNIVAC 1050 PAL ASSEMBLER CODING FORM

PROGRAM-ID 75 80

PROGRAM _____ PROGRAMMER _____ DATE _____ PAGE ____ OF ____ PAGES

For BEGIN only.

SEQUENCE			LABEL	OPERATION	OPERANDS	COMMENTS →	PROGRAM-ID →
PAGE 1 3	LINE 4 5	INS 6	7 11	13 18	19 30 40 45	46 50 60 70 72	75 80 90

UP-2591 Rev. 1

(80-90 COLUMN FORM)

PROGRAM TRANSLATOR: PAL TAPE

§ 181.

.1 GENERAL

.11 Identity: . . . . . PAL TAPE Assembly System.

.12 Description

This translator permits utilization of all the facilities of the PAL language as described in section 777:171.

Its operation requires at least two magnetic tape units, a card reader, a card punch (optional if card output is not desired), and at least 8,192 positions of core storage. With two tape units, input is on cards and output can be either on cards or tape. If a third tape unit is available, input may be on tape. The translator and a library of input-output routines and user-defined procedures are provided on the PAL Library Tape, which also contains REGENT (the 1050 report generator) and the Tape Sort Routine, described in Section 777:151.

Additions, deletions, or alterations to the Library Tape can be made by using a library maintenance program in a separate run (see Paragraph 777:151.16). Corrections to the object program can be made by reassembly or with the PATCH Assembler (see Paragraph .4 below).

.13 Originator: . . . . . UNIVAC Division, Sperry Rand Corporation.

.14 Maintainer: . . . . . as above.

.15 Availability: . . . . . currently in use.

.2 INPUT

The PAL TAPE Assembler accepts source programs written in PAL Assembly Language on punched cards or, if three tape units are available, on magnetic tape. Source statements must be sequenced according to coding sheet page, line, and insertion numbers. There is no practical limit to the number of source statements or tags that can be assembled. Other limitations are as follows: maximum number of NAME lines within a procedure definition is 10; maximum number of nested DO's is 10.

.3 OUTPUT

The output object program is in UNIVAC 1050 machine language on punched cards or on magnetic tape. Documentation consists of a printed listing showing source code, object code and location, and coding errors. Some of the errors that will be detected are out-of-sequence condition, duplicated or undefined labels, invalid operation codes, directive errors, and missing procedures. In addition, a symbol table can be punched if desired.

.3 OUTPUT (Contd.)

This table is required if the PATCH Assembler is to be used.

.4 TRANSLATING PROCEDURE

PAL TAPE is a four-pass assembler. The action in each of the passes is as follows:

Pass 1 - collects all PROC's (subroutines from input and library tape).

Pass 2 - performs a tag edit to a scratch tape.

Pass 3 - builds the tag table.

Pass 4 - assembles instructions and produces the object code, code-edit listings, and punched symbol table (optional).

The program diagnostics that can be included are the DUMP and PCALL routines, described in Paragraph 777:171.67.

The PAL TAPE Library contains the translator and input-output routines for all peripherals. User-defined routines can be added, using OPUS.

PATCH Assembler

Additions, deletions, or alterations of the object program can be made in a separate run, using the PATCH Assembler without a full reassembly. Input to PATCH are the symbol table (optional output from the PAL Assembler) and the Insertion, Change, and Deletion cards written in PAL Language. Output consists of an updated symbol table, patch cards, and a listing of the changes in object and source code.

The PATCH Assembler has facilities for the addition or deletion of coding and the replacement of sections of coding. The replacement section of coding can be the same size as, larger than, or smaller than the original section. The same precautions must be observed when using PATCH as when patching by hand; e.g., jumps into areas modified by PATCH can cause errors. There will probably be few advantages to using PATCH on small programs, but it could be quite useful on large programs where the assembly time is appreciable.

.5 TRANSLATOR PERFORMANCE

The assembler generates one machine instruction for each line of coding except for macro calls and directives. Except for the input-output and file control routines, the space requirements and running time of an assembled object program should be the same as for good hand-coding. The generalized input-output and file control routines provide

§ 181.

.5 TRANSLATOR PERFORMANCE (Contd.)

the required coding for a specific program but are, in general, less efficient than a hand-coded routine for a specific application. However, use of the standard routines should significantly decrease the amount of programming time required. Typical storage requirements and execution times of the input-output routines are shown in Table I.

Assembly speed is approximately 300 source language statements per minute; it varies with the number of macros called and the different input and output media.

COORDINATOR (Section 777:191) is required during the execution of the PAL TAPE object program to furnish the connection between the I/O control routines and the object program.

.6 COMPUTER CONFIGURATIONS

Minimum configuration required for PAL TAPE assemblies is two magnetic tape units, card reader, card punch, printer, and at least 8,192 positions of core storage. If three tape units are available, input and/or output can be on magnetic tape. Programs can be assembled to run on any UNIVAC 1050 system.

.7 ERRORS, CHECKS, AND ACTION

The following types of errors are detected and indicated by symbols on the printed listing:

Duplicate or undefined label.
Expression too long.
Operation code error.
Card sequence error.
TAPE block count error.
More than 10 nested DO's.
Incorrect expression in a DO statement.
Incorrect statement form.
Missing procedure.
More than 30 parameters in a PROC statement.

TABLE I: STORAGE REQUIREMENTS AND EXECUTION TIMES FOR I/O ROUTINES

Name	Storage Required, characters	Execution Time, msec	Comment
COORDINATOR	3200	—	single-program version
COORDINATOR	4200	—	two-program version
CARD READER	637	2*	includes three input areas
CARD PUNCH	928	2*	includes three output areas
PRINTER	908	2*	includes two output areas
MAGNETIC TAPE FILE CONTROL	900	0.6	to place the absolute address of the next input or output item in the arithmetic register.
		1.3*	to obtain the next item from an input file and transfer it to a working area or output file.
		1.2*	to obtain the next item from an input file or working area and transfer it to an output file.

* Does not include data transfer time between peripheral device and core storage.

PROGRAM TRANSLATOR: PAL JR

§ 182.

.1 GENERAL

.11 Identity: . . . . . PAL JR Assembly System.

.12 Description

The PAL JR translator permits the use of a highly restricted version of the PAL Language described in Section 777:171 on minimum-configuration systems consisting of a card punch, card reader, printer, and 4,096 positions of core storage. The main restrictions upon PAL JR, with respect to PAL TAPE (as described in Section 777:181), are as follows:

- No I/O control routines other than those for printer, card reader, and card punch are provided.
- I/O areas have fixed labels and cannot exceed two per peripheral device.
- Maximum label size is three characters, and the maximum number of labels is 100.

.12 Description (Contd.)

- There is no library.
- PROC declarations (user-defined macros) cannot be processed.
- There is no PATCH assembler.

The I/O routines are in the form of card decks which are added to the user's own coding prior to assembly. PAL JR is a two-pass assembler. The first pass develops the tag table, and the second assembles the instructions and produces an object deck and code listing. The listing is identical to that for PAL TAPE.

.13 Originator: . . . . . UNIVAC Division, Sperry Rand Corporation.

.14 Maintainer: . . . . . as above.

.15 Availability: . . . . . November, 1964 (date available to users).

PROGRAM TRANSLATOR: PAL CARD

§ 183.

.1 GENERAL

.11 Identity: . . . . . PAL CARD Assembly System.

.12 Description

PAL CARD permits the full use of the PAL language as described in Section 777:171, with the exception of magnetic tape input-output and file control macros and the processing of PROC's (user-defined macros). PAL CARD is intended for card-oriented systems with a card reader, card punch, printer, punched paper tape subsystem (optional), one magnetic tape unit (optional), and at least 8,192 positions of core storage. Standard input-output routines are of the generator type and are processed with the source coding in a preassembly pass. The output of this pass is a set of input-output routines in source code that have been tailored to the specific object program. These and the source code deck form the input to the assembler.

.12 Description (Contd.)

PAL CARD is a two-pass assembler that assembles one instruction for each line of coding, except for certain directives. The first pass develops the tag table; the second assembles the instructions and produces the object code deck, the code-edit listing (identical to that for PAL TAPE), and a symbol table deck (optional). A maximum of 280 labels can be processed on systems having 8,192 positions of core storage; an additional 400 labels are permitted for each additional 4,096 core positions.

The PATCH assembler can be used to modify the object program without the need for full reassembly (as described in Paragraph 777:171.4).

.13 Originator: . . . . . UNIVAC Division, Sperry Rand Corporation.

.14 Maintainer: . . . . . as above.

.15 Availability: . . . . . currently in use.

OPERATING ENVIRONMENT: COORDINATOR

§ 191.

.1 GENERAL

.11 Identity: . . . . . COORDINATOR.

.12 Description

While complete details on COORDINATOR, the executive routine for the UNIVAC 1050, are not available to date, the following general specifications are known:

- Assembled programs incorporating routines from the PAL Library Tape must run under control of COORDINATOR. COORDINATOR provides the linkage between a "worker program" and the routines (including I/O control routines) incorporated from the Library Tape.
- The coordination of all I/O requests, including requests from communications equipment, can be handled by COORDINATOR.
- One version of COORDINATOR provides for the loading and execution of one program by itself or of two programs in parallel, on a time-shared basis.
- Programs can be called from a master tape either by control cards or by use of the console. Provision is made for aborting a program presently being executed in order to call a program of higher priority. (The establishment of rerun points has not been defined as yet.)

.12 Description (Contd.)

- Transfer of control from one program to the other, when two programs are running together, is made when the central processor would be delayed in fulfilling an I/O request by the program having control; i.e., when the program becomes I/O-limited.
- No log of operations is produced as yet.
- Errors presently detected by COORDINATOR include: program exceeds available memory, program is not on master tape, attempted simultaneous loading of two programs, an absolute-code program would overlay COORDINATOR. These errors cause the processor to halt with a specific error display.
- Storage requirements are 3200 characters for the single-program version and 4200 positions for the dual-program version.

.13 Availability: . . . . . initial version is currently in use.

.14 Originator: . . . . . UNIVAC Division, Sperry Rand Corporation.

.15 Maintainer: . . . . . as above.

.16 Reference: . . . . . none published to date.

SYSTEM PERFORMANCE

§ 201.

GENERALIZED FILE PROCESSING (777:201.100)

These problems involve updating a master file from transaction data in a detail file and producing a printed record of the results of each transaction. This type of run is one of the most common commercial data processing jobs (e.g., in payroll, billing and inventory control applications). The Standard File Problems are fully described in Section 4:200.1 of the Users' Guide.

As noted in Section 777:111, Simultaneous Operations, the overall capability of the UNIVAC 1050 for simultaneous input-output operations is less than one would expect when the high speed tape units (Uniservo III A and IV C) or the Fastrand units are used. These units have no read-write overlap and, with the Model III Processor, the card equipment is interlocked during their operation. However, in typical equipment configurations such as Configurations I, II, and III, the overlap of I/O functions is very high.

In Configuration I (the Typical Card System), the master and detail input files are on the card reader. For problems A, B, C, and D, the 200-cpm card punch is always the controlling factor on overall processing time. A faster (300-cpm) card punch is available, which would increase the Configuration I throughput by 50% for an increase of only about 8% in the system cost. The faster punch was not used in Configuration I because the guidelines for Standard Configuration I only called for a 200-cpm capability. *

The master files are on magnetic tape in Configurations II, III, and IV.* The detail file is assigned to the card reader and the report file to the printer. To permit the Generalized File Processing Problem to be performed within the 8,192-character core storage of Configuration II, the block length of master file records is held to 648 characters (6 records) for this configuration only. Master files for Configurations III and IV contain 1,080 characters (10 records) per block.

Because of the relatively high speeds of both the Model III and Model IV Central Processors, the I/O units are the controlling factors with only one exception, mentioned later in this section. In general the printer is the controlling factor at moderate and high activity ratios and the magnetic tapes at low ratios. Consequently, the upper (printer-limited) portions of the curves for a particular configuration are identical for all problems. The differences in the upper portions of the curves for the various configurations are a result of the different printing rates of the printers in the respective configurations (see pages 777:031.200 through 777:031.500).

The only situation in which the central processor is limiting is Configurations II and III, Problem B, for activity ratios of less than 0.04. Note that Configuration IIIA (which uses the faster Model IV Central Processor but is the same as Configuration III otherwise) does not become central processor limited in this situation.

The point at which the magnetic tape units, rather than the printer, become the controlling factor depends on the master-file blocking factor (number of records per block). In general, the higher the blocking factor, the lower the activity ratio at which the magnetic tapes become limiting. This effect can be seen by comparing the curves for Configuration II with the curves for Configuration III. Both configurations have the same type printer, magnetic tape units, and central processor; but Configuration III has a larger core store, allowing a higher blocking factor.

Configurations III and IIIA have identical performance (except for the case mentioned previously) although Configuration IIIA uses the significantly faster Model IV Central Processor. Again, this is because the I/O devices, not the central processor, are the controlling factor.

---

* See Users' Guide Section 4:030 for definition of Standard Configurations and Section 777:031, this report, for a description of the Standard Configurations as applied to the UNIVAC 1050.

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Since two programs can be run concurrently under control of the executive routine, COORDINATOR, the timings for the central processors are shown for each file problem for Configurations III, IIIA, and IV. (The special input-output routines required to fit the Standard File Problems into the 8K available storage capacity in Configuration II probably would not work with COORDINATOR). As can be seen from the curves, a large share of the central processor's time is unused during file processing. This time could be used to process another program simultaneously, under control of COORDINATOR, provided sufficient peripheral devices were provided to handle the second program's files and sufficient core storage were available to hold the second program and its data areas.

SORTING (777:201.200)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A by the method explained in Paragraph 4:200.213 of the Users' Guide. A two-way merge was used in System Configuration II (which has only four magnetic tape units), and a three-way merge was used in Configurations III and IV. The results are shown in Graph 777:201.200. Configurations II, III, and IIIA use Uniservo VI C Tape Units which provide read-write-compute simultaneity, giving excellent performance from tape units which can transfer data at only 34,000 characters per second. On the other hand, Configuration IV employs the Uniservo III A tape units, which have a peak transfer rate of 133,000 characters per second but a very limited read-write overlap. The performance of the UNIVAC 1050 Configuration IV is not significantly better than the other configurations, due to this limited capability for read-write overlap.

Times for the standard UNIVAC 1050 sort routines (magnetic tape and magnetic drum) are not available to date.

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WORKSHEET DATA TABLE 1 (STANDARD FILE PROBLEM A)

	ITEM		CONFIGURATION I		CONFIGURATION II		CONFIGURATION III		CONFIGURATION IIIA		CONFIGURATION IV		REFERENCE
1	Char/block	(File 1)	80		648		1,080		1,080		1,080		
	Records/block	K (File 1)	0.5		6		10		10		10		
	msec/block	File 1/File 2	75/300		36.5		49.2		49.2		15.9		
		File 3	75		100		100		100		75		
Input-Output Times		File 4	128		142		142		142		128		
	msec/switch	File 1/File 2	0		0		0		0		0		4:200.112
		File 3	0		0		0		0		0		
		File 4	0		0		0		0		0		
	msec penalty/block	File 1/File 2	6.8/5.1		2.9		4.9		2.2		2.2		
		File 3	6.8		6.0		6.0		0.2		0.2		
		File 4	0.6		0.6		0.6		0.3		0.3		
2	msec/block	a_1	1.0		1.1		1.1		0.4		0.4		
Central	msec/record	a_2	3.3		3.3		3.3		0.9		0.9		4:200.1132
Processor	msec/detail	b6	0.5		0.5		0.5		0.2		0.2		
Times	msec/work	b5 + b9	10.1		31.0		10.1		3.1		3.1		
	msec/report	b7 + b8	3.5		3.5		3.5		1.1		1.1		
3	msec/block	a_1	1.0		1.1		1.1		0.4		0.4		
System	for C. P.	a_2 K	1.6		19.6		32.7		8.7		8.7		
Performance	and	a_3 K	7.1		210.0		141.0		44.4		44.4		
at	dominant	File 1 Master In	6.8		2.9		4.9		2.2		2.2		
F = 1.0	column.	File 2 Master Out	5.1	300	2.9		4.9		2.2		2.2		4:200.114
		File 3 Details	3.4		36.0		60.0		1.6		1.6		
		File 4 Reports	0.3		3.6	852	6.0	1,420	2.6	1,420	2.6	1,280	
		Total	25.3	300	276.1	852	250.6	1,420	62.1	1,420	62.1	1,280	
4	Unit of measure	characters											
		Std. routines	1,600		1,400*		5,000**		5,000**		5,000**		
		Fixed	169		217		217		217		265		
Space		3 (Blocks 1 to 23)	600		615		615		615		615		
		6 (Blocks 24 to 48)	3,000		2,600		3,000		3,000		3,000		4:200.1151
		Files	1,024		3,104		4,832		4,832		3,752		
		Working	50		50		50		50		200		
		Total	6,443		7,986		13,714		13,714		12,832		

* simplified I/O control (own coding).

** includes COORDINATOR.

SYSTEM PERFORMANCE

§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

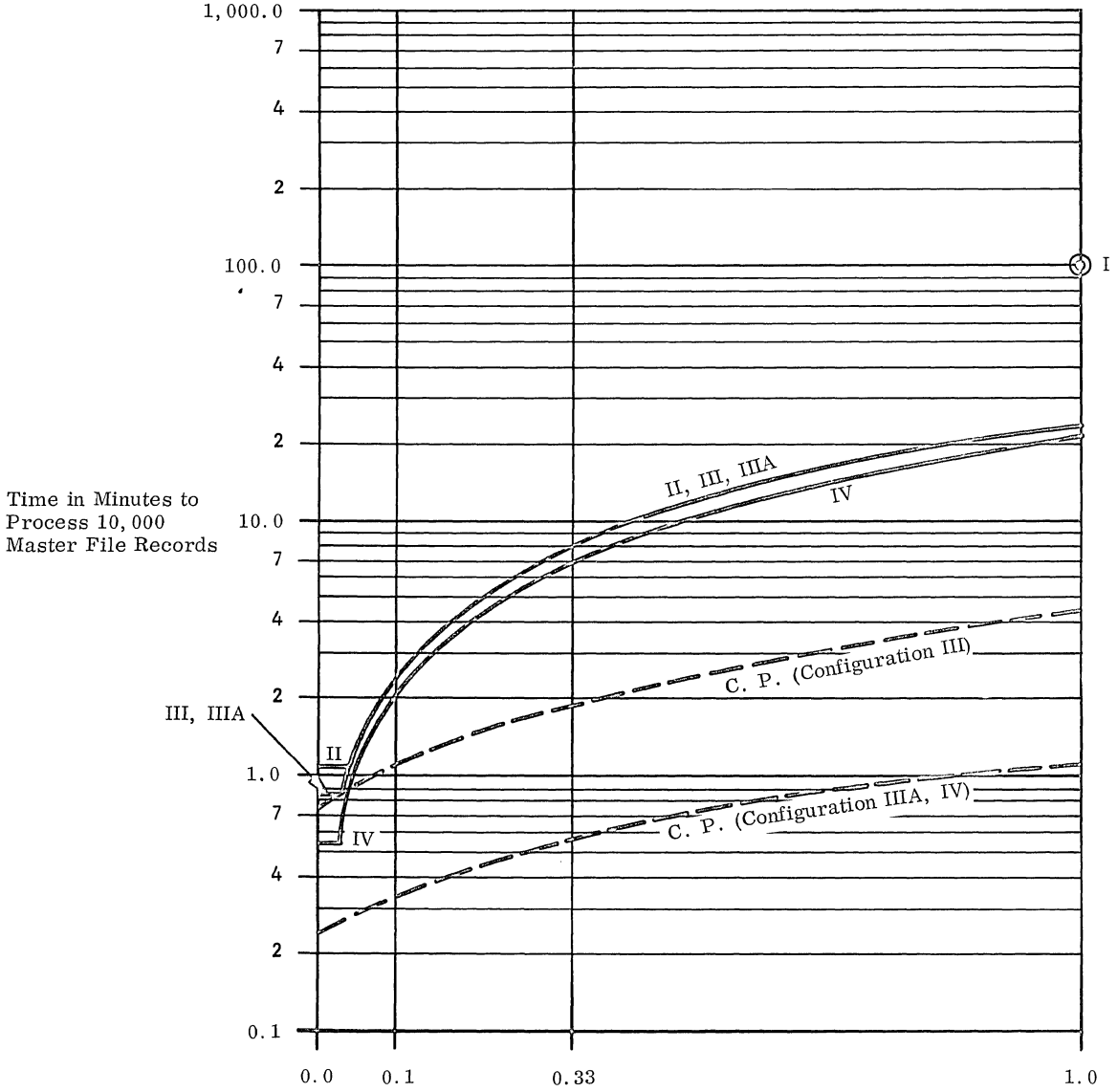
.111 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

.112 Computation:. . . . . standard.

.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . . see graph below.

.115 Storage space required
Configuration I: . . . . 6,400 characters.
Configuration II: . . . 8,000 characters.
Configuration III: . . . 13,700 characters.
Configuration IIIA: . . 13,700 characters.
Configuration IV: . . . 12,800 characters.



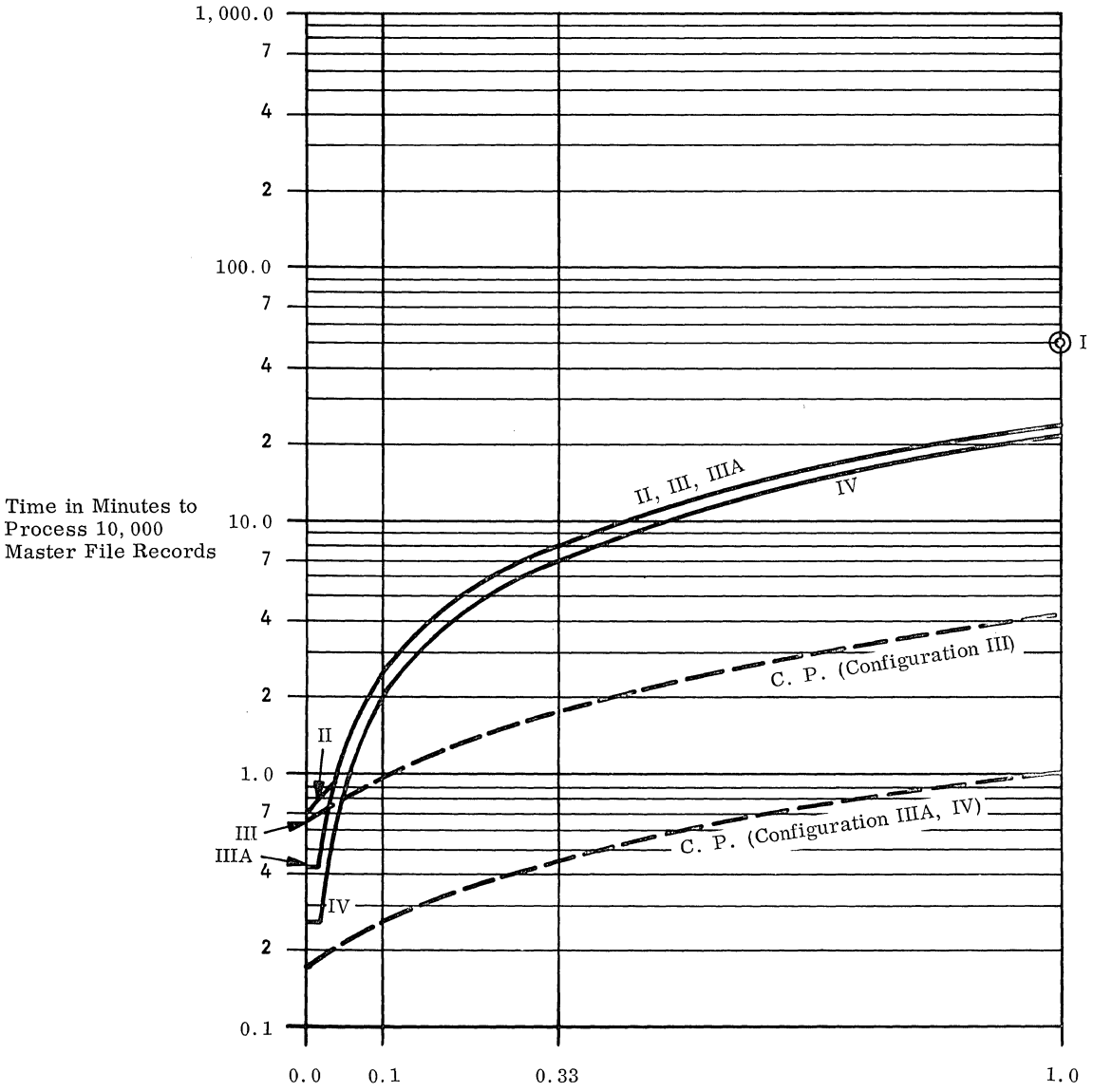
(Roman numerals denote standard System Configurations)

§ 201.

.12 Standard File Problem B

.121 Record sizes
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

.122 Computation:. . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



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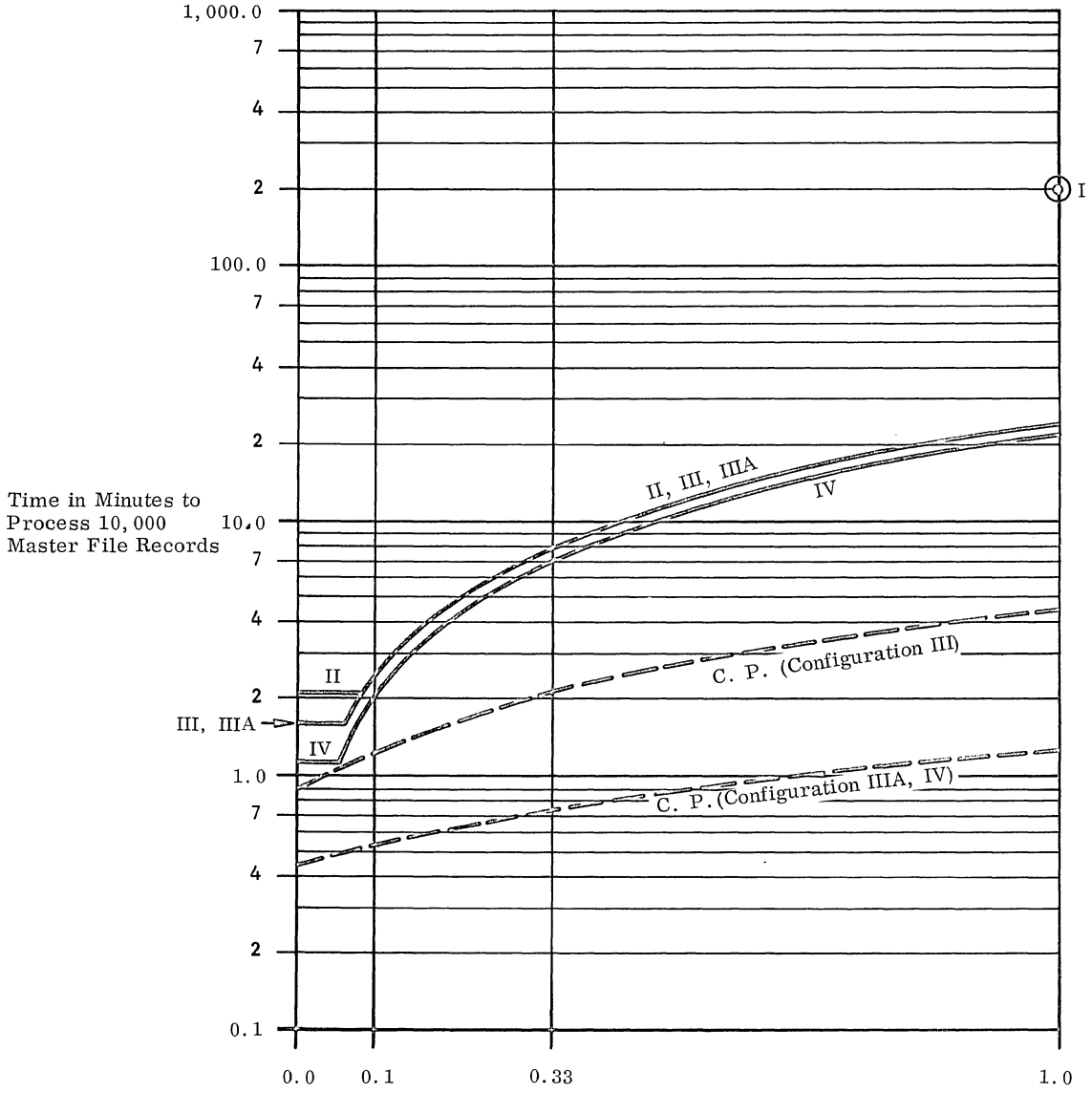
.13 Standard File Problem C

.131 Record sizes
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

.132 Computation:. . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.



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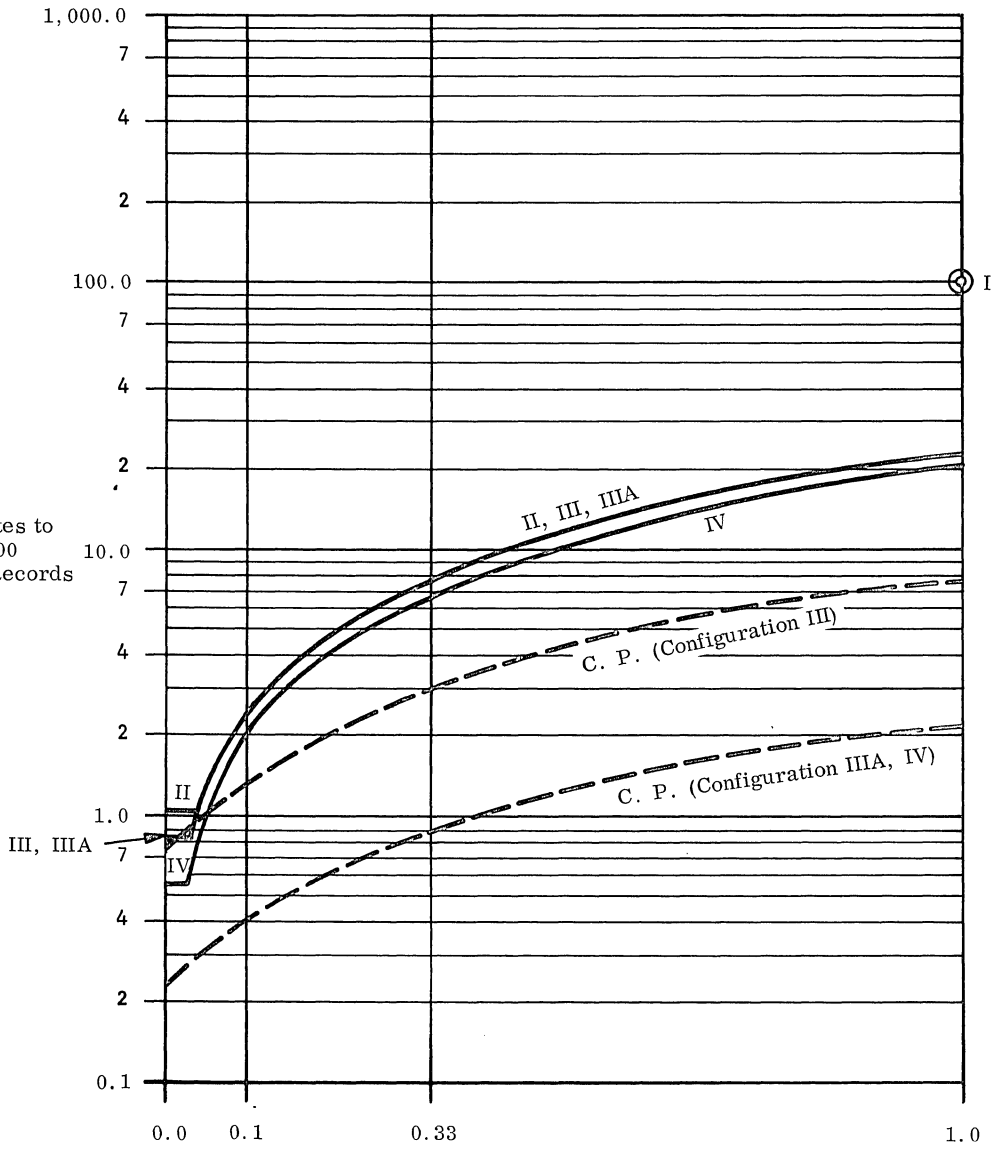
.14 Standard File Problem D

.141 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

.142 Computation:. . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

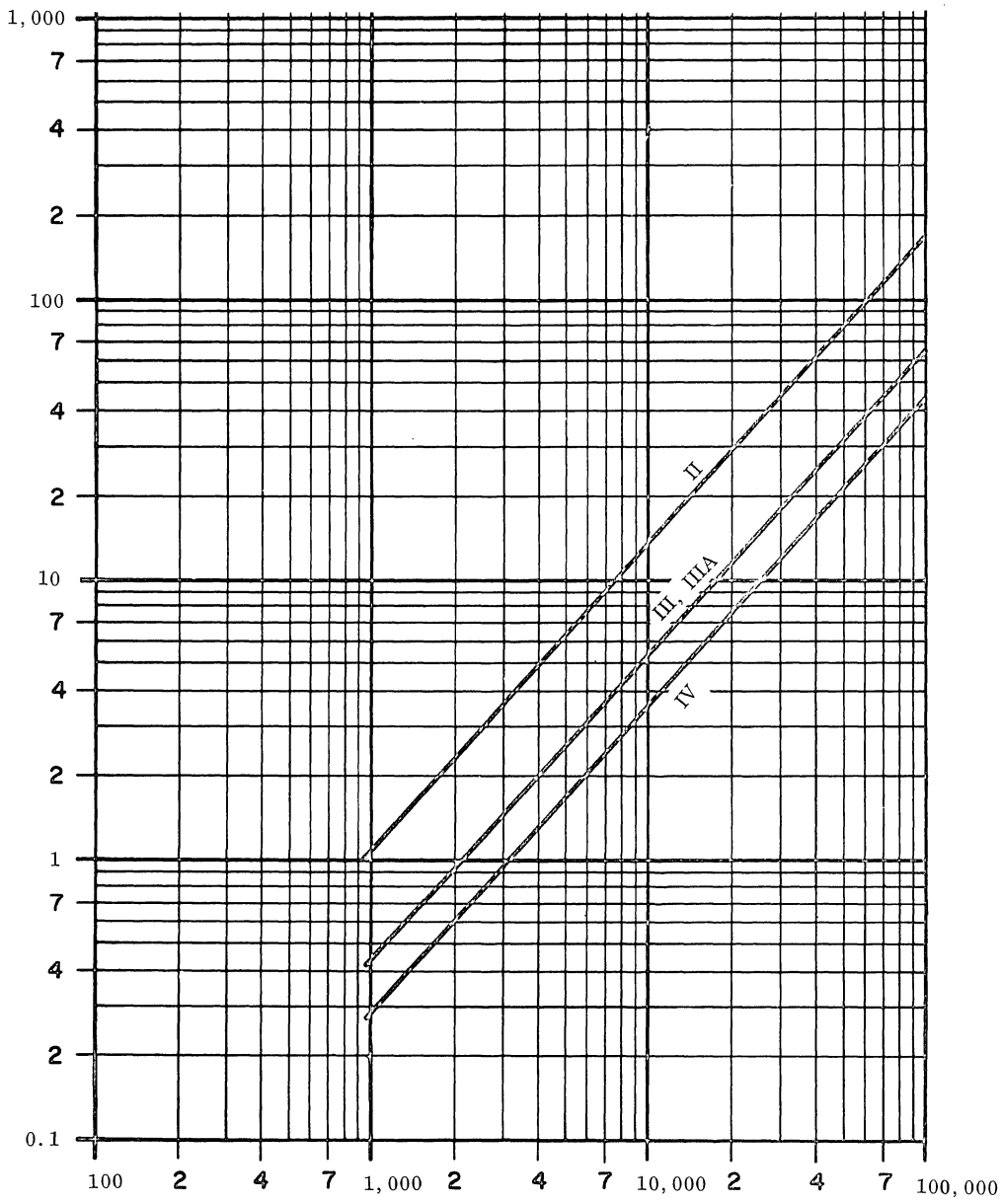
§ 201.

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.
.212 Key size: . . . . . 8 characters.

.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.
.214 Graph: . . . . . see graph below.



Time in Minutes to Put Records Into Required Order

Number of Records

(Roman numerals denote standard System Configurations)

PHYSICAL CHARACTERISTICS

§ 211.

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
Model III Central Processor (includes 4,096 characters)	26	75	55	2,500	5.0	13,640
Model IV Central Processor (includes 8,192 characters)	?	?	?	?	?	?
Central Processor Power Supply	26	24	55	*	*	*
Additional Memory Module — Model III (4,096 characters)	*	*	*	*	*	*
Additional Memory Module — Model IV (8,192 characters)	*	*	*	*	*	*
"B" Power Supply	26	24	55	1,415	2.5	6,825
Uniservo Synchronizer (all models)	36	26	55	650	1.1	3,500
Uniservo Power Supply (all models)	22	26	55	815	3.0	8,200
Uniservo IIIA or IVC Tape Handler	31	30	63	810	3.0	8,850
Uniservo VIC Tape Handler (Control is included in first tape unit)	24	26	64	500	1.2	3,500
Transition Cabinet (Required for first IIIA or IVC tape handler)	18	30	63	150	-	-
High Speed Printer (all models)	43	33	55	1,250	1.7	4,930
Card Reader (all models)	40	22	45	600	1.0	2,500
Card Punch (all models)	38	26	47	800	1.5	4,600
Console — Integrated (mounts atop the processor)	8	28	11	60	-	-
Console — Freestanding	60	31	41	200	-	-
Inquiry Typewriter	25	26	39	151	-	-
Punched Paper Tape Subsystem (includes reader, punch, and synchronizer in one cabinet)	40	35	66	500	2.5	6,850
Fastrand Mass Storage Unit (all models)	122	32	63	5,150	12.5	19,500
Fastrand Control Unit (all models)	36	26	55	650	1.0	2,800
Communications Subsystem Cabinet (Each Communication Multiplexer and associated equipment requires 2 cabinets.)	48	26	96 (80 optional)	2,000	5.9	6,000

* included in Central Processor specifications.

General Requirements

Temperature: . . . . . between 60° F and 80° F.
Relative Humidity: . . . . . between 40% and 70%.
Power: . . . . . 230-volt, 1-phase, 60-cycle, 3-wire; or 208-volt, 3-phase, 60-cycle, 4-wire.

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR		Model III Central Processor (includes 4,096 characters of core storage and 3 I/O channels)	1,185	115	47,500
		Model IV Central Processor (includes 8,192 characters of core storage)	2,385	230	95,500
		Optional Features			
		Multiply-Divide —			
		Model III	150	5	6,000
		Model IV	275	10	11,500
		Input/Output Channels (per channel) —			
		Model III	45	3	1,800
		Model IV	85	7	4,600
		Inquiry Typewriter	165	15	6,600
		Console - Freestanding	75	5	3,000
		Console - Integrated	45	3	1,800
	0670-00	"B" Power Supply (Required when any peripherals except card reader, card punch, printer, and one additional subsystem are used)	150	15	6,000
INTERNAL STORAGE		Core Storage			
		Model III Memory Module - 4,096 characters (7 max)	325	15	13,000
		Model IV Memory Module - 8,192 characters (7 max)	685	25	27,400
		Random Access Drum Storage			
	0900-00	Fastrand I Storage Unit - 66 million characters (8 per controller max)	3,300	*	160,000
		Fastrand II Storage Unit - 132 million characters (8 per controller max)	3,800	**	184,000
	5002-02	Fastrand I Control Unit	995	100	39,800

* $250 for first unit, $120 for each additional unit.
** $265 for first unit, $125 for each additional unit.

§ 221. **PRICE DATA (Contd.)**

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INTERNAL STORAGE (Contd)		Fastrand II Control Unit	995	85	39,800
		Fastbands option (24 bands)	200	22	9,000
INPUT-OUTPUT	0706-00	Card Reader - 800/900 cpm; 80 columns	380	100	15,200
	0706-05	Card Reader - 800/900 cpm; 90 columns	380	100	15,200
	0706-01	Card Reader - 600 cpm; 80 columns	225	55	9,000
	0706-04	Card Reader - 600 cpm; 90 columns	225	55	9,000
	0600-00	Card Punch - 300 cpm; 80 columns	665	200	26,600
	0600-01	Card Punch - 300 cpm; 90 columns	665	200	26,600
	0600-12	Card Punch - 200 cpm; 80 columns	400	115	18,200
	0600-13	Card Punch - 200 cpm; 90 columns	400	115	18,200
	0755-01	Printer - 700/922 lpm	800	240	38,400
	0755-02	Printer - 600/750 lpm	575	195	24,300
	9150-18	Printer Buffer	185	15	7,400
	5003-00	Second Printer Synchronizer and Buffer	550	25	22,000
	0903-00	Paper Tape Reader - 1,000 cps	385	135	15,400
	0903-01	Paper Tape Reader - 300 cps	?	?	?
	0636-00	Paper Tape Reader Spooled Option	85	30	3,400
	0606-01	Paper Tape Punch -110 cps	165	58	6,600
	0637-00	Paper Tape Punch Take-up Reel Option	5	-	200
	5005-00	Paper Tape Control Unit	235	83	9,400
	0635-00	1050/1004 Adapter Unit	200	20	8,000
		Magnetic Tape Units			
	0850-00	Uniservo IIIA - 133,000 char/sec	750	155	36,500
	0551-01	Uniservo IIIA Synchronizer	995	50	39,800
	1353-00	Uniservo IIIA Power Supply	215	35	8,600
		Uniservo IVC - 62,500 char/sec	750	62	36,500
	0851-04	Uniservo IVC - 90,000 char/sec	800	95	38,400
	0556-01	Uniservo IVC Synchronizer	995	85	39,800
	1353-01	Uniservo IVC Power Supply	215	35	8,600
	0858-00	Uniservo VIC - Control and one tape unit	500	125	20,000
	0858-01	Uniservo VIC tape unit - 34,000 char/sec	300	75	12,000
	5307-00	Uniservo VIC Synchronizer	600	30	24,000

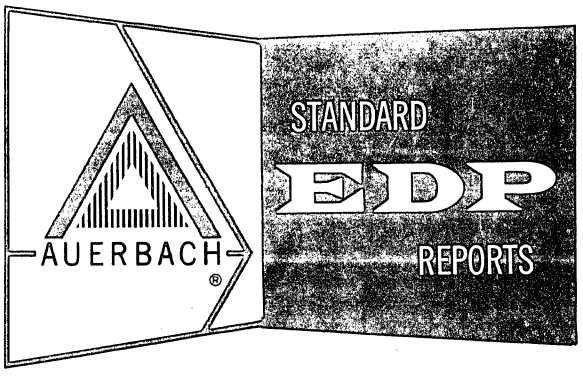
§ 221. PRICE DATA (Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd)		Communications Multiplexer			
	0900-04	4 Simplex positions	675	186	30,375
	0900-03	8 Simplex positions	725	200	32,625
	0900-02	16 Simplex positions	800	220	36,000
	0900-01	32 Simplex positions	1,000	275	45,000
	0900-00	64 Simplex positions	1,300	358	58,500
		Communications Line Terminals			
	CLT-50L	Low Speed Output - 5 Level Asynchronous	25	5	1,125
	CLT-51L	Low Speed Input - 5 Level Asynchronous	20	6	900
	CLT-80L	Low Speed Output - 6, 7, and 8 Level Asynchronous	30	8	1,350
	CLT-81L	Low Speed Input - 6, 7, and 8 Level Asynchronous	25	7	1,125
	CLT-80M	Medium Speed Output - 5, 6, 7, and 8 Level Asynchronous	35	10	1,575
	CLT-81M	Medium Speed Input - 5, 6, 7, and 8 Level Asynchronous	25	7	1,125
	CLT-80H	High Speed Output - 5, 6, 7, and 8 Level Synchronous	45	12	2,025
	CLT-81H	High Speed Input - 5, 6, 7, and 8 Level Synchronous	45	12	2,025
	CLT-12IH	High Speed Input - 5 thru 12 Level Synchronous	50	14	2,250
	CLT-Parallel	Parallel Output	35	10	1,575
	CLT-Parallel	Parallel Input	35	10	1,575
	CLT-Dialing	Automatic Dialing	20	6	900

UNIVAC 1107

Univac

(A Division of Sperry Rand Corporation)



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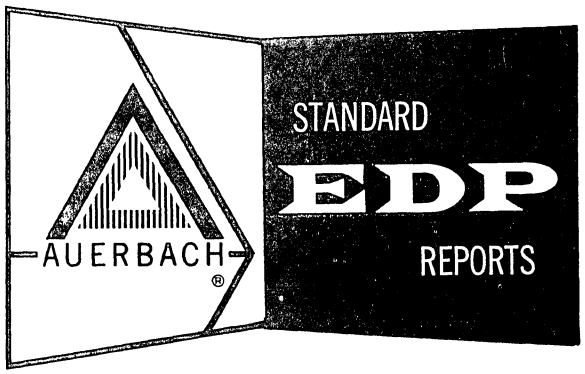
UNIVAC 1107

Univac

(A Division of Sperry Rand Corporation)



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CONTENTS

INA = Information not available

RIP = Report in process

§ 001. CONTENTS (Contd.)

RIP = Report in process

INTRODUCTION

§ 011.

The UNIVAC 1107 Thin-Film Memory Computer is a large scale data processing system suitable for both scientific and commercial applications. The 1107 is the solid-state successor to the vacuum-tube UNIVAC 1105 and 1103 scientific systems and provides greatly increased speed and flexibility of both internal processing and input-output operations. There is, however, no program compatibility between the 1107 and its predecessors. Monthly rentals for most 1107 systems will fall within the $40,000 to $70,000 range. The first customer delivery of a UNIVAC 1107 was made in September, 1962.

Although the UNIVAC 1050 (described in Computer System Report 777:) appears to be well suited for use as an off-line input-output processor for tape-oriented 1107 systems, the two 1107 operating systems are designed to provide efficient on-line input-output via the card reader, punch, and printer through multi-program running techniques. The System Configuration section includes examples of a fully integrated system (page 784:031.200) and of a tape-oriented system with an off-line UNIVAC 1050 (page 784:031.300).

Hardware

The main feature that distinguishes the UNIVAC 1107 from other currently available large scale computer systems is its 128 word locations of Thin-Film Memory. These locations consist of permalloy spots deposited on a thin plate by a vacuum process. Each spot represents one bit-position of storage, and its direction of magnetization determines whether it is storing a binary zero or one. The Film Memory has a read access time of 0.333 microsecond and a cycle time of 0.667 microsecond, so it can theoretically be referenced up to 1,500,000 times per second. Specific functions are assigned to 63 of the 128 Film Memory locations. Fifteen locations serve as index registers and 16 as arithmetic registers or "accumulators." This abundance of arithmetic and index registers contributes heavily to the power and flexibility of UNIVAC 1107 programming. The remaining 65 Film Memory locations are available as general-purpose working storage, but there are certain programming restrictions on their use. Furthermore, instruction execution times are no faster when the operands are in Film Memory than when they are properly located in Core Memory.

Core Memory can consist of 16,384, 32,768, 49,152, or 65,536 word locations. Each 36-bit word location can hold 1 instruction, 1 floating point data item, from 1 to 6 fixed point data fields, or 6 alphameric characters. There is no parity bit, and no parity checking is performed on internal operations. The 16,384-word store can consist of either 1 or 2 banks; the larger models are all divided into 2 independently accessed, asynchronous banks. Read access time is 1.8 microseconds and cycle time is 4.0 microseconds for each 36-bit word. By storing instructions in one bank and data in the other, it is possible to overlap the operation of the two banks to reduce the effective cycle time by a factor of two. This "alternate bank" storage allocation technique decreases the execution time for most instructions by 4.0 microseconds; e.g., each add, subtract, load, or store instruction takes 8.0 microseconds when the instruction and its operand are in the same bank and only 4.0 microseconds when they are in alternate banks.

The UNIVAC 1107 Central Computer can perform fixed and floating point arithmetic on one-word binary operands. The 16 arithmetic registers, 15 index registers, a versatile repertoire of 7-part instructions, recursive indirect addressing, and a partial-word transfer facility permit efficient processing of most scientific problems. Commercial processing will be somewhat less efficient because the 1107 lacks automatic facilities for editing, decimal arithmetic, and radix conversions.

Although the 1107 uses a 1-address instruction format, a limited 2-address capability is provided by the fact that most instructions can specify the use of any one of the 16 arithmetic registers. The partial-word load and store instructions can transfer any half,

INTRODUCTION (Contd.)

§ 011.

third, or sixth of a word to or from the least significant bit positions of any arithmetic register. A wide variety of logical, shift, search, and block transfer operations can be performed. All instructions can be indexed, and each index register can be automatically incremented or decremented each time it is referenced. Indirect addresses can be "chained," and indexing can be performed upon each address in the chain. Straightforward programming of the UNIVAC 1107 is not unusually complex, but only skilled, highly-trained programmers will be able to take full advantage of the powerful optional elements offered in most instructions.

A program interrupt facility causes a transfer of control to one of 74 fixed core locations upon completion of an input-output operation, upon detection of a processor or input-output error, or upon count-down to zero of the real-time clock (whose contents are decremented by 1 every millisecond). The interrupt facility permits full utilization of the Central Computer and all peripheral devices, usually under the control of an integrated operating system that handles multi-program running.

The 1107 has 16 input-output channels, and each channel is capable of transmitting data in one direction at a time. One channel is normally occupied by the Control Console, which provides keyboard input and typed output at 10 characters per second. Each of the remaining 15 channels can accommodate 1 peripheral subsystem, and each subsystem can consist of any of the following groups of devices and their associated control units.

- 1 to 8 Flying Head 880 Magnetic Drums. Each drum stores 786,432 words, with an average access time of 17 milliseconds. Peak data transfer rate is 60,000 words per second. This rapid-access auxiliary storage plays an important role in the operation of several of the software systems.

- 1 to 8 Fastrand Mass Storage Units. Each unit has 2 drums served by 64 movable heads, and stores 12,976,128 words with an average access time of 92 milliseconds. Peak data transfer rate is 25,000 words per second.

- 2 to 16 Uniservo IIIA Magnetic Tape Handlers. Read forward or backward at a peak transfer rate of 100,000 rows per second. Nine tracks are recorded on $\frac{1}{2}$-inch-wide tape at a density of 1,000 rows per inch, with read-after-write row parity checking.

- 2 to 12 Uniservo IIA Magnetic Tape Handlers. Read forward or backward at a peak transfer rate of 12,500 or 25,000 rows per second. Eight tracks are recorded on $\frac{1}{2}$-inch-wide tape at a density of 125 or 250 rows per inch; there is no read-after-write checking.

- 2 to 12 Uniservo IIIC Magnetic Tape Handlers. Read forward only at a peak transfer rate of 22,500 or 62,500 rows per second. Seven tracks are recorded on $\frac{1}{2}$-inch-wide tape at a density of 200 or 556 rows per inch, with read-after-write checking of longitudinal and row parity. The tape format is fully compatible with the IBM 727, 729, and 7330 Magnetic Tape Units.

- 1 Card Reader and 1 Card Punch. These units read standard 80-column cards at 600 cards per minute and punch them at 150 or 300 cards per minute. Reading and punching can be performed in alphameric, row binary, or column binary mode.

- 1 High-Speed Printer. Two models are available: one uses a 51-character set and prints up to 600 alphameric lines per minute; the other uses a 63-character set and prints up to 700 alphameric lines per minute (or up to 922 lines per minute when a restricted set of 40 characters is used).

- 1 Paper Tape Reader and 1 Paper Tape Punch. These units (housed in a single cabinet) can read standard 5-, 6-, 7-, or 8-track punched tape at up to 400 characters per second and punch it at 110 characters per second.

INTRODUCTION (Contd.)

§ 011.

As the above summary indicates, three different types of magnetic tape handlers are available for the 1107, and there is no format compatibility between any two of them. This situation resulted from the manufacturer's decisions to provide a tape handler compatible with earlier UNIVAC systems (the Uniservo IIA), a tape handler compatible with IBM systems (the Uniservo IIIC), and a high-performance tape handler for use where compatibility is not a primary concern (the Uniservo IIIA).

Software

Two different basic software packages are being developed for the UNIVAC 1107, and there is little or no compatibility between them. The manufacturer states that the two basic packages will be maintained in parallel. The "SLEUTH I Package," also called the "A Package," was developed by UNIVAC's Scientific Computer Department in St. Paul, and includes the following routines:

- SLEUTH I - a symbolic assembly system with macro instruction facilities that translates symbolic source programs into either relocatable or absolute machine language object programs.

- EXEC I - an operating system designed to facilitate effective use of 1107 systems by providing the means for automatically processing a scheduled set of jobs with a minimum of operator intervention. Jobs can be processed serially or concurrently (i.e., multi-running is optional).

- CLAMP - a Relative Load Routine that loads either absolute or relocatable object programs independently or under control of EXEC I.

- Librarian - a library maintenance routine that creates a library tape and adds, deletes, corrects, resequences, lists, and catalogs programs on existing library tapes.

- LION (Library of Input-Output Numerical Subroutines) - a set of subroutines, called by SLEUTH macro instructions, that perform the following functions in connection with EXEC I:

  Opening and closing of files and reels;

  Input and output on tape, drum, cards, or printer;

  Conversions between decimal and binary radix;

  Data transcriptions (cards to tape or drum, tape or drum to cards, and tape or drum to printer).

- MIDAS (Macro Instructions for Dumping Areas of Store) - a set of subroutines designed to aid debugging by providing printed listings of the contents of specified areas of storage. A valuable option permits listing only those locations whose contents have been altered during execution of the program being tested.

- Sort/Merge - a generalized, relocatable subroutine for sorting or merging files into ascending or descending order. Control parameters are supplied on cards. From 4 to 12 magnetic tape units can be used, and FH-880 Magnetic Drums provide increased sorting speed when available.

The "Sleuth II Package," also called the "B Package," was developed by Computer Sciences Corporation and includes the following routines:

- SLEUTH II - a symbolic assembly system with macro instruction facilities that translates symbolic source programs into relocatable machine language object.

INTRODUCTION (Contd.)

§ 011.

programs. A magnetic drum is required, but magnetic tape is not. (There is no compatibility between SLEUTH I and SLEUTH II; even the mnemonic codes for machine instructions are totally different.)

- EXEC II - an operating system designed to monitor the compilation and execution of programs, maximize utilization of the available hardware, and minimize operator intervention. The system utilizes an FH-880 Magnetic Drum as a high capacity buffer store to keep the card readers, punches, and printers fully occupied and as a fast access auxiliary store for program segments. An integrated set of diagnostic aids and library maintenance facilities is included.

- COBOL - a compiler for COBOL-61 source programs that operates under control of EXEC II. Language facilities include nearly all of Required COBOL-61 (there are a few minor deficiencies); several COBOL-61 electives (but not the extremely useful COMPUTE verb); a MONITOR verb (which provides dynamic printouts of the values of specified items); and a SORT facility (but not the one defined as part of Extended COBOL-61). A magnetic drum is required for COBOL compilations, but magnetic tape is not.

- FORTRAN - a compiler for FORTRAN IV source programs that operates under control of EXEC II. Language facilities are largely compatible with those of FORTRAN IV as defined for the IBM 7090/7094. FORTRAN II source programs can be converted to FORTRAN IV by means of the SIFT Translator, which has been compiled and successfully run on the 1107. The FORTRAN compiler achieves rapid compilation speeds through use of an FH-880 Magnetic Drum.

- SORT II - a generalized sort/merge routine that will operate under control of EXEC II.

The SLEUTH II Package will probably be the more widely used of the two software packages because it includes the COBOL and FORTRAN compilers. UNIVAC 1107 users may join USE, the UNIVAC Scientific Exchange, which distributes user-developed programs. Furthermore, the FORTRAN compiler and the SIFT Translator will enable 1107 users to utilize the extensive libraries of FORTRAN-coded routines that are now available.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	36 bits	basic addressable storage unit in core, film, and drum storage.
Field:	6, 12, or 18 bits	an integral portion of a word, addressable by field definition in certain 1107 instructions.
Row (Uniservo IIA):	8 bits (6 data, 1 parity, 1 clock)	magnetic tape; holds 1 character or 1/6 of an 1107 word.
Row (Uniservo IIIA):	9 bits (8 data, 1 parity)	magnetic tape; holds 1/5 or 1/6 of an 1107 word.
Row (Uniservo IIIC):	7 bits (6 data, 1 parity)	magnetic tape; holds 1 character in IBM-compatibile format.
Column:	12 positions	punched cards; usually holds 1 character.
Line:	128 characters	High-Speed Printer reports.
Block:	1 to N words	magnetic or punched tape.

.2 DATA FORMATS

Type of Information	Representation
Instruction:	1 word.
Fixed point number: . .	1 word; 35 data bits and sign bit.
Floating point number:	1 word; 27 data bits and sign for fractional part, 8 bits for exponent.
Alphameric character:	6 bits (internal), 1 row (tape), or 1 column (cards).
Card image (row binary):	3 words (2 with 36 bits and 1 with 8 bits) per card row; 36 consecutive words per card.
Card image (column binary):	3 card columns per word; 27 consecutive words per card.
Record:	1 to N words of logically related information.
File:	1 to N records.

SYSTEM CONFIGURATION

§ 031.

Every UNIVAC 1107 system includes a Central Computer Group consisting of the following units:

- Central Computer
- Power Control
- 25 KVA Motor-Alternator
- Control Console
- Core Memory - any one of the following:
  - 16,384 words - one bank
  - 16,384 words - two banks
  - 32,768 words - two banks
  - 49,152 words - two banks
  - 65,536 words - two banks

Up to 15 peripheral subsystems can be connected, in any combination of the following subsystems:

- FH-880 Magnetic Drum Subsystem
  - 1 to 8 FH-880 Drums
  - 1 FH-880 Drum Control and Synchronizer Unit
- Fastrand Mass Storage Subsystem
  - 1 to 8 Fastrand Storage Units
  - 1 Fastrand Synchronizer
- Uniservo IIIA Magnetic Tape Subsystem
  - 2 to 16 Uniservo IIIA Tape Units
  - 1 Uniservo IIIA Control and Synchronizer Unit (single or dual channel †)
  - 1 Uniservo Power Supply ‡
- Uniservo IIA Magnetic Tape Subsystem
  - 2 to 12 Uniservo IIA Tape Units
  - 1 Uniservo IIA Control and Synchronizer Unit
  - 1 Uniservo Power Supply ‡
- Uniservo IIIC Magnetic Tape Subsystem
  - 2 to 12 Uniservo IIIC Tape Units
  - 1 Uniservo IIIC Control and Synchronizer Unit
  - 1 Tape Adapter Cabinet
  - 1 Uniservo Power Supply ‡

† Each dual channel Synchronizer occupies 2 of the 15 input-output channels.

‡ Uniservo Power Supply capacity is 14 IIA, 16 IIIA, or 16 IIIC tape units; one Power Supply can serve two or more subsystems, within certain limits.

SYSTEM CONFIGURATION (CONTD.)

§ 031.

- Punched Card Subsystem (80-column)

  1 Card Reader - 600 CPM
  1 Card Punch - 150 or 300 CPM
  1 Card Control and Synchronizer Unit

- High-Speed Printer Subsystem

  1 Printer - 600 or 700 LPM
  1 Printer Control and Synchronizer Unit

- Paper Tape Subsystem

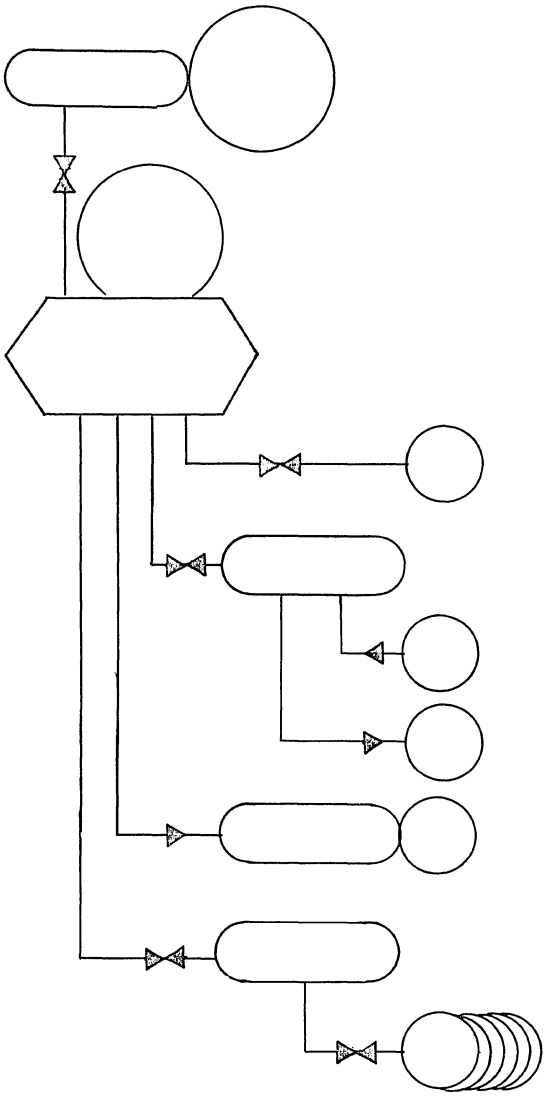
  (Reader, Punch, and Control in single cabinet)

SYSTEM CONFIGURATION

§ 031.

.1 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration: . . . . . FH-880 Drum is required for use of most software systems.
Console typewriter provides input as well as output.
Twelve more index registers.
More simultaneity.
Core Memory is larger by 3,050 words.
Magnetic tape is slower by 5,000 char/sec.

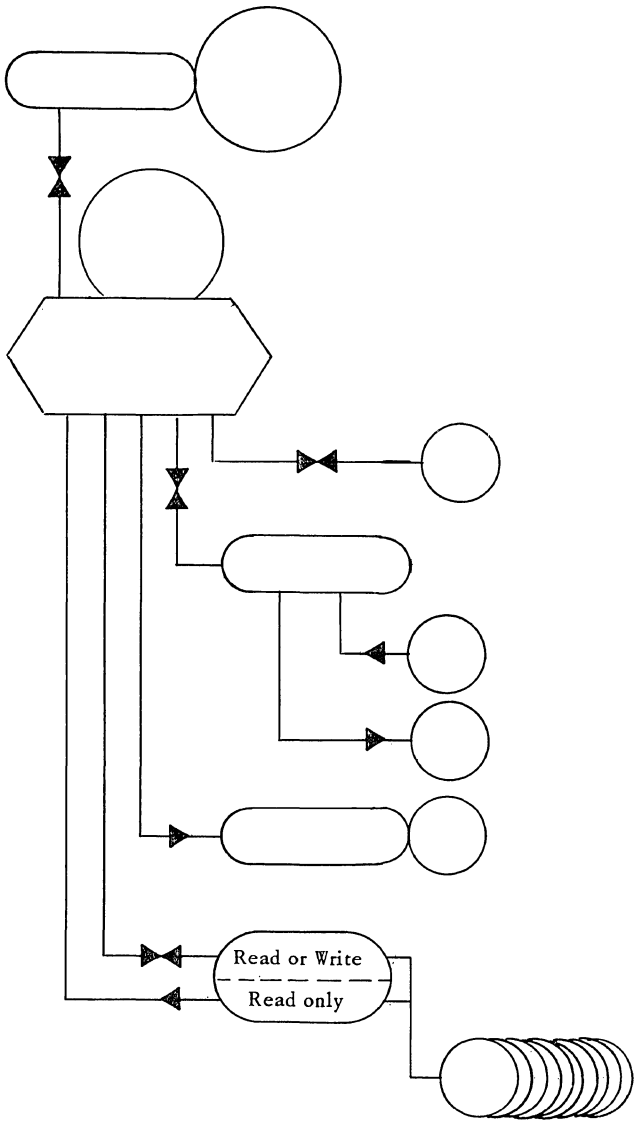


Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$3,440
Core Memory: 16,384 words (2 banks)	7,000
Central Computer	19,750
Console	
Card Control & Synchronizer	1,850
Card Reader: 600 cards/min.	350
Card Punch: 150 cards/min.	500
Printer & Synchronizer: 600 lines/min.	2,050
Uniservo IIA Synchronizer	1,550
Uniservo IIA Tape Units (6): 25,000 char/sec.	2,700
Uniservo Power Supply (not shown)	550
TOTAL RENTAL:	$39,740

§ 031.

.2 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VII A

Deviations from Standard Configuration: . . . . . FH-880 Drum is required for use of most software systems.
Core Memory is smaller by 3,616 words.
Magnetic tape is faster by 60,000 characters per second.
Nine more index registers.



Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$3,440
Core Memory: 16,384 words (2 banks)	7,000
Central Computer	19,750
Console	
Card Control & Synchronizer	1,850
Card Reader: 600 cards/min.	350
Card Punch: 150 cards/min.	500
Printer & Synchronizer: 600 lines/min.	2,050
Uniservo IIIA Synchronizer: dual channel model	5,000
Uniservo IIIA Tape Units (10): 120,000 char/sec.	7,500
Uniservo Power Supply (not shown)	550
TOTAL RENTAL:	$47,990

§ 031.

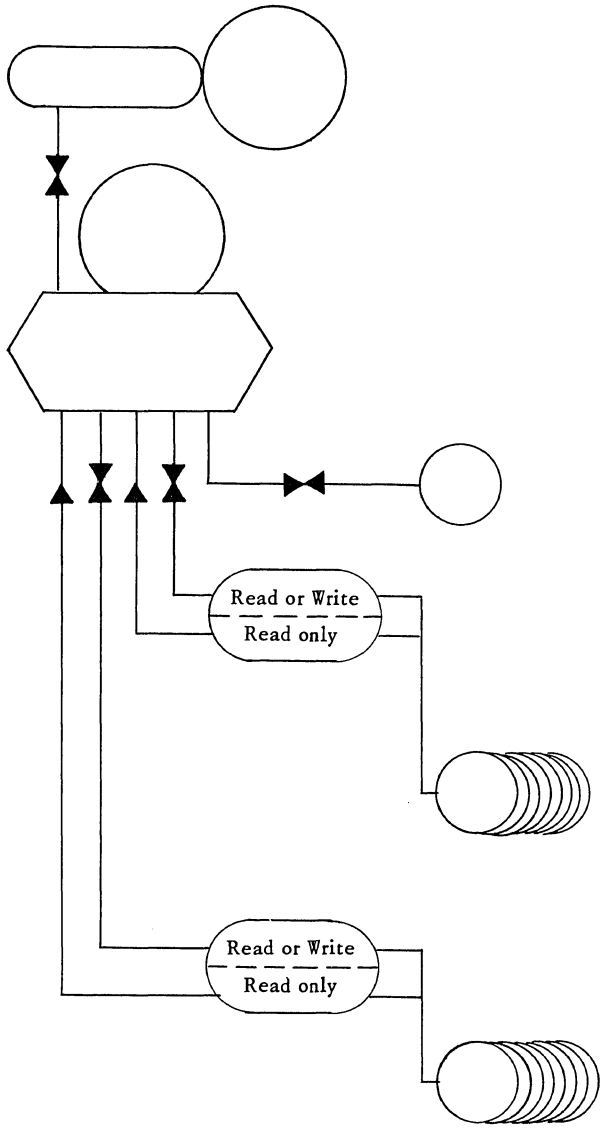
.3 20-TAPE GENERAL SYSTEM (PAIRED); CONFIGURATION VIIIB

Deviations from Standard Configuration

On-line equipment: . . . . . FH-880 Drum is required for use of most software systems.
Core Memory is larger by 6,100 words.
Five more index registers.
No on-line card reader is used.

Off-line equipment: . . . . . Core storage is larger by 3,192 positions.
Magnetic tape is faster by 60,000 char/sec.
Card punch is faster by 100 cards/minute.
Four more index registers.

On-Line Equipment

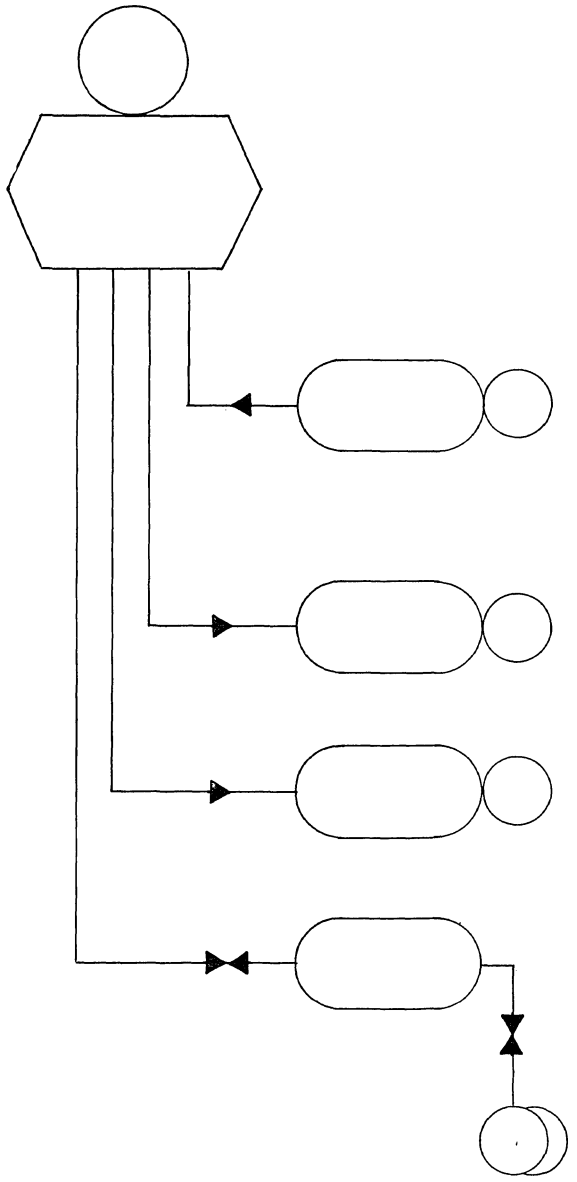


Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$3,440
Core Memory: 32,768 words (2 banks)	9,000
Central Computer Console	19,750
Uniservo IIIA Synchronizer: dual channel model	5,000
Uniservo Power Supply	550
Uniservo IIIA Tape Units(8): 120,000 char/sec.	6,000
Uniservo Power Supply (not shown)	550
Uniservo IIIA Synchronizer: dual channel model	5,000
Uniservo IIIA Tape Units (8): 120,000 char/sec.	6,000
TOTAL RENTAL:	$54,740
Total including off-line equipment:	$61,890

§ 031.

.3 20-TAPE GENERAL SYSTEM (PAIRED); CONFIGURATION VIIIB - (Contd.)

Off-Line Equipment (Univac 1050):



Equipment	Rental
Core Storage: 8,192 positions Central Processor	$1,850
Card Reader and Synchronizer: 1000 cards/min.	400
Card Punch and Synchronizer: 300 cards/min.	700
Printer and Synchronizer: 922 lines/min.	800
Print Buffer	350
Uniservo IIIA Synchronizer	1,200
Power Supply	350
Uniservo IIIA Magnetic Tape Units (2): 120,000 char/sec.	1,500
TOTAL RENTAL:	$7,150

INTERNAL STORAGE: CORE MEMORY

§ 041.

.1 GENERAL

.11 Identity: . . . . . Core Memory. Types 7230, 7231, 7232, 7233, 7234.

.12 Basic Use: . . . . . working storage.

.13 Description

Core Memory forms the principal working storage medium for the UNIVAC 1107 and can consist of from 16,384 to 65,536 word locations in one or two banks. The following configurations are offered:

Type Number	Banks	Word Locations
7230	1	16,384
7231	2	16,384
7232	2	32,768
7233	2	49,152
7234	2	65,536

Read access time is 1.8 microseconds and cycle time is 4.0 microseconds for each 36-bit word. In the two-bank models, each bank has independent access facilities and can operate asynchronously. By storing instructions in one bank and data in the other, the effective storage cycle time can be reduced to a minimum of 2.0 microseconds. This "alternate bank" storage allocation decreases the overall execution time for most instructions by 4.0 microseconds.

Each 36-bit word location can hold one instruction, one floating point data item, from one to six fixed point data items, or six alphameric characters. Block transfer operations from one area of Core Memory to another can transfer full words or either half (18 bits), any third (12 bits), or any sixth (6 bits) of successive word locations at a peak rate of 125,000 words per second. The source addresses can be N words apart and the destination addresses M words apart, with N not necessarily equal to M. No parity checking is provided.

To prevent accidental writing into Core Memory areas where no alteration of the stored data is permissible, a Memory Lockout Register is provided. This register, set by an instruction, defines the upper and lower address limits of the area in each bank in which writing is permitted. The address limit codes are modulo 2,048; thus storage can be locked out only in 2,048-word increments. A write instruction referencing an address outside the limits specified in the Memory Lockout Register causes an error interrupt and an automatic jump to a fixed storage location.

.13 Description (Contd.)

The 128 lowest-order locations of Core Memory are called "hidden" memory. Their addresses (000_8 through 177_8) are the same as those of Film Memory, and they can be accessed only by indirect addressing, by jump instructions, or by input-output operations. All other instructions refer to the correspondingly numbered locations in Film Memory. The "hidden" core locations are therefore protected from internal write operations but not from input-output operations; the converse applies to all of Film Memory. To minimize confusion between the contents of Film and "hidden" memory, the safest policy is to avoid program references to the core locations below address 177_8.

The 75 core locations with addresses 200_8 through 312_8 are assigned for the specific purposes shown below:

Octal addresses	Assignment
200-217	External request interrupts.
220-237	Input data termination interrupts.
240-257	Output data termination interrupts.
260-277	Function termination interrupts.
300-307	Error interrupts.
310	Real-time clock interrupt.
311	External status word.
312	External synchronization interrupt.
Greater than 312	Unassigned.

.14 Availability: . . . . . 9 to 12 months.

.15 First Delivery: . . . . September, 1962.

.16 Reserved Storage

Purpose	Number of Locations	Locks
Index registers:	0 †	
Arithmetic registers:	0 †	
Logic registers:	0	
Interrupt control:	75	only via programming.
"Hidden memory":	128	protected from internal write operations.

† In Film Memory; see Section 784:042.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

§ 041.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . all models except Type 7230 are divided into two banks with independent access facilities.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.282 Reading method: . . . . coincident current.
.283 Type of access: . . . . read-out followed by rewrite.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates: . . . . up to 250,000 cps per bank.
Unit of data: . . . . . one 36-bit word.
Gain factor: . . . . . 2 banks (optional).
Data rate: . . . . . 250,000 words/sec per bank.
Compound data rate: . 500,000 words/sec in all models except Type 7230.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage				Maximum Storage
Type Number:	7230	7231	7232	7233	7234
Banks:	1	2	2	2	2
Words:	16,384	16,384	32,768	49,152	65,536
Characters:	98,304	98,304	196,608	294,912	393,216
Instructions:	16,384	16,384	32,768	49,152	65,536

.4 CONTROLLER: . . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: 1 access facility per bank.

.52 Simultaneous Operations: . . . . . access to each bank is asynchronous and independent of the other bank.

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . . 1.8 μsec.
Cycle time: . . . . . 4.0 μsec.
For data unit of: . . . . 1 word.

Note: When instructions are stored in one bank and operands in the other, effective cycle time approaches a minimum of 2.0 μsec. Cycle time for Type 7230 is a constant 4.0 μsec.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.71 Data Transfer

Pairs of storage unit possibilities

With self: . . . . . yes.
With Film Memory: . yes.
With FH-880 Drum: . yes.

.72 Transfer Load Size

With self: . . . . . 1 to N full or partial words; N limited by storage capacity.
With Film Memory: . . 1 to 128 full or partial words.
With FH-880 Drum: . . 1 to N full words.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none.	
Invalid code:	all codes valid.	
Receipt of data:	none.	
Recording of data:	none.	
Recovery of data:	none.	
Dispatch of data:	none.	
Timing conflicts:	check	resolved automatically by priority control network.
Reference to locked area:	check	interrupt.

INTERNAL STORAGE: FILM MEMORY

§ 042.

.1 GENERAL

..11 Identity: . . . . . Film Memory. (In Type 7200 Central Computer cabinet.)

.12 Basic Use: . . . . . control and working storage.

.13 Description

Film Memory (also called Control Memory) provides 128 word locations of fast-access internal storage and gives the UNIVAC 1107 Thin-Film Memory Computer its name. Access time is 0.333 microsecond and cycle time is 0.667 microsecond; theoretically, up to 1,500,000 references per second can be made to Film Memory.

Specific functions are assigned to 63 of the 128 Film Memory locations. There are 15 index registers, 16 arithmetic registers, 32 input-output access-control words, and four registers whose specific functions are listed in Paragraph 16 below. Four locations can be used as either index or arithmetic registers, making possible some unconventional address modification operations. The remaining 65 Film Memory locations are available as fast-access working storage, but there are certain programming restrictions: Film Memory cannot be referenced by jump instructions, indirect addressing, or input-output operations, and partial-word load and store operations are restricted. The arithmetic and index registers have "two-address accessibility" in most instructions: they can be referenced either by the base operand address or by the a- or b-designator in the instruction word.

The thin-film storage medium consists of permalloy spots deposited on a thin plate by a vacuum process. Each spot represents one bit position of storage, and the direction of magnetization of the spot determines whether it is storing a 0 or a 1. Drive and sense lines are etched on Mylar sheets, attached to epoxy boards, and mounted above and below each plane of film spots. The read/restore cycle consists of reading one word of data from the selected film spots into the 36-bit Z Register, transferring it to the central processor, and then re-writing it into the same film spots from which it was read. The clear/write cycle consists of reading and discarding the data from the selected film spots, transferring new data into the Z-register, and writing it into the selected film spots. No parity checks are made.

.14 Availability: . . . . . 9 to 12 months.

.15 First Delivery: . . . . September, 1962.

.16 Reserved Storage

Purpose	Number of Locations	Octal Addresses	Locks
Index registers:	15	001-017 †	none.
Arithmetic registers:	16	014-033 †	
Input access-control:	16	040-057	
Output access-control:	16	060-077	
Real-time clock count:	1	100	
Repeat count:	1	101	
Mask word:	1	102	
Temporary storage for P:	1	103	
Unassigned:	65	000, 034-037, 105-177	

† Locations 014 through 017 can be used as either Index or Arithmetic registers.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . thin film (spots of permalloy deposited on a thin plate).

.22 Physical Dimensions

Diameter of spots: . . . 50 mils.
Thickness of spots: . . 1,000 angstroms.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . yes.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . none.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.282 Reading method: . . . . linear select.
.283 Type of access: . . . . read-out followed by rewrite.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates: . . . . up to 1,500,000 cps.
Unit of data: . . . . . one 36-bit word.
Data rate: . . . . . 1,500,000 words/sec.

§ 042.

.3 DATA CAPACITY

.31 Module and System Sizes

Identity: . . . . . standard.
Modules: . . . . . 1.
Words: . . . . . 128.
Characters: . . . . . 768.
Instructions: . . . . . not used for instruction storage.

.4 CONTROLLER: . . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: 1 access facility.

.52 Simultaneous Operations: . . . . . none.

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . . 0.333 μsec.
Cycle time: . . . . . 0.667 μsec.
For data unit of: . . . . 1 word.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.71 Data Transfer

Pairs of storage unit possibilities

With self: . . . . . yes.
With Core Memory: . yes.
With FH-880 Drum: . no.

.72 Transfer Load Size

With self: . . . . . 1 to N full words; N limited by storage capacity.
With Core Memory: . . 1 to 128 full or partial words.

.73 Effective Transfer Rate

With self: . . . . . 125,000 words/sec.
With Core Memory: . . 125,000 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none	addresses above 177_8 refer to Core Memory.
Invalid code:	all codes valid.	
Receipt of data:	none.	
Recording of data:	none.	
Dispatch of data:	none.	
Recovery of data:	none.	
Timing conflicts:	check	resolved automatically.

INTERNAL STORAGE: FH-880 DRUM

§ 043.

.1 GENERAL

.11 Identity: . . . . . Flying Head 880 Magnetic Drum.
Type 7432.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 880 Magnetic Drum is an auxiliary storage device that provides rapid random access to large quantities of data or programs in UNIVAC 1107 systems. Each drum has 880 read-write heads, each serving one track. The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the rotating drum. The flying head principle permits the use of larger drums with less critical tolerances, and the close head-to-drum spacing (0.0005 inch) permits high-density recording.

A Magnetic Drum Subsystem consists of from one to eight Flying Head 880 Magnetic Drums connected to a Drum Control and Synchronizer Unit. Each subsystem fully occupies one input-output channel. Since one of the 1107's 16 channels is required for the Control Console, a maximum of 15 Magnetic Drum Subsystems could be connected if no other peripheral equipment were required. Each drum has a storage capacity of 786,432 words of 36 bits each. Maximum potential storage capacity is therefore 6,291,456 words per subsystem and 94,371,840 words per fully expanded 1107 system.

Of the 880 tracks on each drum, 768 are grouped into 128 data bands of six tracks each. The other 112 tracks are used for parity checking, timing, reference, and as spares. Each 1107 word is converted by the Synchronizer into six 6-bit characters. The six tracks in each data band are read and recorded in parallel, and each word is stored in a six-by-six matrix of bit positions. An odd parity bit is generated for each word and recorded in a corresponding location in one of 32 parity tracks.

Each data band consists of 6,144 word locations arranged in the form of three interleaved "angular sections" of 2,048 words each. This means that any location can be accessed within one drum revolution, but only 2,048 words can be read or recorded per revolution. Drum speed is 1,800 revolutions per minute, so the average access time is 17 milliseconds. Peak data transfer rate is 60,000 words or 360,000 characters per second. From 1 to 65,535 words can be transferred in a single operation. Each drum read operation requires two instructions, two Access Words, and a Function Word. The instructions initiate the input mode and function mode

.13 Description (Contd.)

on the appropriate input-output channel. The Access Words specify the initial core storage address, the number of words to be transferred, and the address of the Function Word. The Function Word specifies the operation to be performed and the 23-bit initial drum address. Coding of a drum write operation is similar but requires a third instruction. A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired.

Checking includes a parity check to insure that each word read from the drum has odd parity, a character count to insure that each word transferred to or from the drum consists of exactly six characters, and checks for invalid drum addresses and function codes. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Computer a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 9 to 12 months.

.15 First Delivery: . . . . September, 1962.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum
Diameter: . . . . . 24 inches.
Length: . . . . . 30 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data volume per band of 6 tracks

Words: . . . . . 6,144.
Characters: . . . . . 36,864.
Instructions: . . . . . 6,144.

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.26 Bands per Physical Unit: 128.

.27 Interleaving Levels: . . 3.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically supported head per track.

.283 Type of access

Description of stage	Possible starting stage
Switch bands:	when different band is selected (or at end of a band).
Wait for specified sector:	when previously selected band is used.
Read or write 1 to 65,535 words: . . .	no.

.29 Potential Transfer Rates

.291 Peak bit rates

Cycling rates:	1,800 rpm.
Track/head speed: . .	2,265 inches/sec.
Bits/inch/track: . . .	518.
Bit rate per track: . .	1,173,270 bits/sec/track.

.292 Peak data rates

Unit of data:	word.
Conversion factor: . .	36 bits per word.
Gain factor:	6 tracks per band.
Loss factor:	3 interleaving levels.
Data rate:	60,000 words/sec, or 360,000 char/sec.
Compound data rate: .	240,000 words/sec, or 1,440,000 char/sec. †

† With four FH-880 Drum units on four different input-output channels transferring data simultaneously. Total communication rate for the 1107 system cannot exceed 250,000 words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum per Subsystem	Maximum Storage
Drum Subsystems:	1	1	15.
Drums:	1	8	120.
Words:	786,432	6,291,456	94,371,840.
Characters:	4,718,592	37,748,736	566,231,040.
Instructions:	786,432	6,291,456	94,371,840.

.32 Rules for Combining Modules: . . . . . 1 to 8 Drum Units per Magnetic Drum Subsystem; 1 to 15 Magnetic Drum Subsystems per 1107 system. Each subsystem fully occupies 1 input-output channel.

.4 CONTROLLER

.41 Identity: . . . . . FH-880 Drum Control and Synchronizer Unit. Type 7427.

.42 Connection to System

.421 On-line: . . . . . 1 to 15 controllers; 1 per Magnetic Drum Subsystem.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 8 FH-880 Drum Units.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 65,535 words.
.442 Input-output area: . . . Core Memory.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization: . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of data stacks

Stacks per drum: . . .	128.
Stacks per subsystem:	128 to 1,024.

.512 Stack movement: . . . . none.
.513 Stacks that can access any particular location: . . . . . 1.
.514 Accessible locations

By single stack: . . .	6,144.
By all stacks:	786,432 per drum. maximum of 6,291,456 per subsystem.

.515 Relationship between stacks and locations: . bits 11-17 of Function Word designate band number 0-127.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer operation per Magnetic Drum Subsystem. Total number of simultaneous drum data transfer operations may in no case exceed 4 because total system communication rate is limited to 250,000 words/sec.

.53 Access Time Parameters and Variations

.532 Variation in access time

Stage	Variation, μsec	Example, μsec
Switch bands:	0 or 134	0.
Wait for specified sector:	0 to 33,300	16,700.
Read or write:	16.3 to 1,070,000 ‡ 16.3 to 1,103,434	33,300 ‡ 50,000

‡ 16.3 μsec per word transferred; example is based on a 2,048-word transfer.

.6 CHANGEABLE STORAGE: . . . . . none.

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.7 PERFORMANCE

.71 Data Transfer

Pairs of storage units possibilities

With self: . . . . . no.
With Core Memory: . yes.
With Film Memory: . no.

.72 Transfer Load Size

With Core Memory: . . 1 to 65,535 words.

.73 Effective Transfer Rate

With Core Memory: . . 60,000 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	character count	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	character count	interrupt.
Reference to locked area:	not possible.	

Note: The type of error is indicated by bits 30-35 of the Status Word, sent to the Central Computer when the interrupt occurs. Bits 0-22 specify the drum address of the error word.

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1107 Central Computer. Type 7200.

.12 Description

The UNIVAC 1107 Central Computer is a single cabinet that houses the system's solid-state arithmetic and control circuitry and 128 word locations of Film Memory. Sixteen arithmetic registers (or "accumulators"), fifteen index registers, a seven-part instruction format, and a partial-word transfer facility provide for programming flexibility and efficient computation. While the 1107 can be programmed in a straightforward way without undue difficulty, only skilled, highly-trained programmers will be able to take full advantage of all its powerful processing facilities.

The versatile instruction repertoire includes fixed and floating point arithmetic on 36-bit binary operands (floating point representation is 27 bits plus sign for the fraction and 8 bits for the exponent). Fixed point multiplication and division can produce either integral or fractional results, depending upon the instructions used. Addition or subtraction by half-words or third-words develops dual 18-bit or triple 12-bit result fields in a single operation. Load and store operations can cause the transfer of a full word or of any half, third, or sixth of a word to or from the least significant bit positions of the specified arithmetic register. A full set of Boolean, test, and conditional jump instructions is provided. Single- and double-length shifts of up to 72 bit positions can be performed in a single 4-microsecond cycle. The block transfer instruction moves blocks of full or partial words from one area of internal storage to another. Twelve different search instructions facilitate table look-up operations. Facilities not directly provided in the 1107 instruction repertoire include editing, double precision arithmetic, decimal arithmetic, and radix conversion; generalized subroutines or complex sequences of instructions are required to accomplish these operations.

Each instruction is one word (36 bits) in length and consists of seven parts, called "designators," as shown below.

Name	f	j	a	b	h	i	u
Size (bits)	6	4	4	4	1	1	16

- The 6-bit f-designator specifies the operation to be performed.
- The 4-bit j-designator specifies partial-word operands or serves as an extension of the operation code.

.12 Description (Contd.)

- The 4-bit a-designator references one of the 16 arithmetic registers in Film Memory or specifies an input-output channel.
- The 4-bit b-designator, references one (or none) of the 15 index registers, whose contents are added to the specified operand address or literal operand.
- The 1-bit h-designator indicates whether or not the 18-bit modifier portion of the specified index register shall be incremented by the increment portion of the same index register (also 18 bits) each time the instruction is executed; this capability for automatic incrementation (or decrementation) facilitates the coding of loops.
- The 1-bit i-designator indicates whether direct or indirect addressing applies (i.e., whether the u-designator specifies the direct address of the required operand or the address of a location containing another address in a chain of indirect addresses that may be of any length).
- The 16-bit u-designator contains the base operand address, an indirect address, a shift count, or a literal operand. In the case of literal operands, the low-order 16 bits of the instruction word are interpreted as the operand itself rather than as the address of a storage location containing the operand.

The fact that the a-designator can specify the use of any of the 16 arithmetic registers in arithmetic, logical, test, load, and store operations provides a limited two-address capability. This capability can reduce program lengths and execution times by minimizing the need for temporary storage of operands in Core Memory. All instructions can be indexed, including those that specify literal operands. Furthermore, indexing and index register incrementation can be performed upon any or all addresses in a cascaded indirect address chain. Each stage of indirect addressing adds 4 microseconds to the instruction execution time.

A key factor in the computing power of the 1107 is the Film Memory (also called Control Memory), which provides 128 36-bit storage locations with an access time of 0.333 microsecond and a cycle time of 0.667 microsecond. Specific functions are assigned to certain Film Memory locations. There are 15 index registers, 16 arithmetic registers (or "accumulators"), 32 input-output Access-Control Words, a real-time clock register, a repeat count register, and a mask word register. Four locations can be designated as either index or arithmetic registers, or both, permitting some unusual and powerful address modification operations. The remaining unassigned Film Memory locations are available as fast-access storage for general use, but are subject to certain programming restrictions: Film Memory

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.12 Description (Contd.)

cannot be referenced by jump instructions, indirect addressing, or input-output operations, and partial-word load and store operations are restricted. Furthermore, instruction execution times for operands in Film Memory are no lower than for operands in Core Memory when the "alternate bank" storage allocation technique (described below) is used.

The 128 lowest-order locations of Core Memory are called "hidden" memory. Their addresses (octal 000 through 177) are the same as those of Film Memory, and they can be accessed only by indirect addressing, by jump instructions, or by input-output operations. All other instructions will refer to the correspondingly numbered Film Memory locations. The "hidden" core locations are therefore protected from overwriting by internal data transfer operations, but not from input-output operations; the converse applies to all of Film Memory. To minimize confusion between the contents of Film and "hidden" memory, the safest policy is to avoid program references to the core locations below octal address 177.

In programming the 1107, it is important to store instructions in one Core Memory bank and data in the other to take advantage of the overlapping cycles of the two core storage banks. This "alternate bank" storage allocation technique halves the effective core storage cycle time and decreases the overall execution time for most instructions by 4 microseconds. Every add, subtract, load, and store instruction takes 4 microseconds when instructions and operands are in alternate banks and 8 microseconds - or twice as long - when they are in the same bank. Processor speeds in Paragraph 785:051.4 are listed for both the "alternate bank" and "same bank" conditions. When the addressed operand is in Film Memory, the lower, "alternate bank" time always applies.

Program interrupts occur upon normal completion of an input-output operation (when requested); upon detection of an input-output, storage reference, or processor error; and whenever the contents of the real-time clock have been decremented to zero. Depending upon the cause of interruption, control is transferred to one of 74 fixed Core Memory locations. Only the contents of the instruction sequence counter can be automatically saved when an interrupt occurs, so the routine that services the interrupt condition must preserve and restore the previous contents of all the registers it uses. The interrupt facility makes multi-running possible under control of EXEC I, the 1107 Executive System, described in Section 784:191.

A 16-bit Memory Lockout Register, loaded by a special instruction, specifies the upper and lower address limits - 2,048-word increments - of the area of each Core Memory bank that is currently available for recording of data. Any write instruction with an effective address outside these permissible limits will initiate an error interrupt.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1962.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point			
Add-subtract:	automatic	binary	35 bits + sign. †
Multiply			
Short:	automatic; integer only	binary	35 bits + sign. †
Long:	automatic; integer or fractional	binary	35 bits + sign † (72-bit product).
Divide			
No remainder:	automatic; fractional only	binary	35 bits + sign. †
Remainder:	automatic; integer or fractional	binary	35 bits + sign (72-bit dividend). †
.212 Floating point			
Add-subtract:	automatic	binary	fraction: 27 bits + sign. exponent: 8 bits.
Multiply:	automatic	binary	
Divide:	automatic	binary	
.213 Boolean			
AND	automatic	binary	36 bits. †
Inclusive OR:	automatic		
Exclusive OR:	automatic		
.214 Comparison			
Numbers:	automatic		36 bits. †
Absolute:	none.		
Letters:	automatic		36 bits (6 chars). †
Mixed:	automatic		36 bits. †
Collating sequence:	see Data Code Table No. 3, Section 784:143.		

	Provision	Between	And	Size
.215 Code translation:	none.			
.216 Radix conversion	standard subroutine	binary field	BCD chars	1 to 36 bits; 3 to 13 chars.

	Provision	Comment	Size
.217 Edit format			
Alter size:	standard subroutine	in LION Input/Output Library; handles numeric data only.	1 to 36 bits before editing.
Suppress zero:			
Insert point:			
Insert spaces:			
Insert sign:			
Float character:	none.		
Protection:	none.		
Round off:	none.		
.218 Table look-up			
Equality:	automatic	look-up can be based on any bit pattern using Masked Search instructions.	36 bits. †
Less than or equal:	automatic		
Greater than:	automatic		
Within limits:	automatic		
Outside limits:	automatic		
Greatest:	none.		
Least:	none.		
.219 Others			
Add/subtract halves:	automatic		two 18-bit fields/word.
Add/subtract thirds:	automatic		three 12-bit fields/word.
Shifts:	automatic	circular, logical, or arithmetic shifts	1 or 2 words.
Block transfer:	automatic		1 to N words. †

† j-designator can specify use of the full addressed operand or any half-word (18 bits), third-word (12 bits), or sixth-word (6 bits) portion of it.

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.22 Special Cases of Operands

.221 Negative numbers:. . . one's complement.
.222 Zero:. . . . . 1 form: zero in all bit positions.
.223 Operand size determination: . . . . j-designator in instruction specifies full word (36 bits), half word (18 bits), third word (12 bits), or sixth word (6 bits) operand length in 51 instructions, including load, store, fixed point arithmetic, logical, and test instructions.

.23 Instruction Formats

.231 Instruction structure: . 1 word.
.232 Instruction layout:

Name	f	j	a	b	h	i	u
Size (bits)	6	4	4	4	1	1	16

.233 Instruction parts

Name	Purpose
f-designator:	specifies major operation code.
j-designator:	(1) specifies partial-word operands; or (2) provides expanded operation code; or (3) indicates that u is a literal rather than an address.
a-designator:	(1) references an Arithmetic Register; or (2) specifies an input-output channel. (3) serves one of several other specialized functions.
b-designator:	references an Index Register, whose contents are added to u.
h-designator:	indicates whether the specified Index Register shall be incremented or decremented.
i-designator:	indicates whether u is a direct or indirect address.
u-designator:	(1) specifies base operand address; or (2) specifies shift count; or (3) holds a literal operand.

.234 Basic address structure: . . . . . 1 + 0. (The a-designator references one of the 16 Arithmetic Registers in thin-film memory, providing a limited two-address capability in many load, store, arithmetic, logical, and test instructions.)

.235 Literals

Arithmetic:.	18 bits.
Comparisons and tests:	18 bits.
Incrementing modifiers:	18 bits.

.236 Directly addressed operands

Internal storage type	Minimum size	Maximum size	Volume accessible
Film Memory:	6 bits	1 word	128 words.
Core Memory:	6 bits	1 word	total capacity (up to 65,536 words).

.237 Address indexing
.2371 Number of methods: . 1.
.2372 Names: . . . . . indexing.
.2373 Indexing rule:. . . . . add contents of modifier portion (lower half) of specified index register to instruction address, modulo 65,536.
.2374 Index specification:. . by b-designator in the instruction to be modified.
.2375 Number of potential indexers: . . . . . 15.
.2376 Addresses which can be indexed: . . . . . operand address portion (u-designator) of all instructions, including literals.
.2377 Cumulative indexing: . none; but see Paragraph .2384.
.2378 Combined index and step:. . . . . yes; if h-designator (bit 17) is 1, add contents of increment portion of specified index register to its modifier portion after the effective operand address has been formed.
.238 Indirect addressing
.2381 Recursive: . . . . . yes.
.2382 Designation: . . . . . 1 in i-designator (bit 16) of each indirect address.
.2383 Control:. . . . . 0 in i-designator of the direct address.
.2384 Indexing with indirect addressing: . . . . . yes; indexing occurs before determination of the indirect address. Both indexing and incrementation of the index register can be specified at each stage of indirect addressing.
.239 Stepping
.2391 Specification of increment: . . . . . in most significant half of the index register.
.2392 Increment sign:. . . . + or -.
.2393 Size of increment: . . 18 bits.
.2394 End value: . . . . . zero, or any value specified in test instruction or storage location.
.2395 Combined step and test: . . . . . yes.

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.24 Special Processor Storage

.241 Category of storage	Number of locations	Size in bits	Program usage
Control register:	1	16	P-Register: holds address of next instruction.
Control register:	2	36	Program Control Registers: decode instructions (both are used in alternate-bank operation).
Control register:	3	18	W-Registers: input registers for the Index Adder.
Control register:	1	18	R-Register: output register for the Index Adder.
Control register:	1	16	Storage Class Control: decodes operand addresses.
Thin-film memory:	15 ‡	36	Index Registers.
Thin-film memory:	16 ‡	36	Arithmetic Registers.
Thin-film memory:	16	36	Input Access-Control.
Thin-film memory:	16	36	Output Access-Control.
Thin-film memory:	1	36	Real-Time Clock Count.
Thin-film memory:	1	36	Repeat Count.
Thin-film memory:	1	36	Mask Word.
Thin-film memory:	1	36	Temporary Storage for P-Register.
Thin-film memory:	65	36	Unrestricted fast access storage.

‡ Four locations may be used as either Index or Arithmetic Registers.

.242 Category of storage	Total number of locations	Physical form	Access time μsec	Cycle time, μsec
Control Registers:	8	flip-flop	?	0.167.
Film Memory:	128	ferromagnetic spots	0.333	0.667.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . 1 (P Register).

.314 Special sub-sequence counters: . . . . . none (during repeated instructions, address of next instruction is stored in Film Memory and P Register holds the Repeat Count Word).

.315 Sequence control step size: . . . . . 1 word.

.316 Accessibility to routines: . . . . . P Register contents can be stored in core storage or in an Index Register.

.317 Permanent or optional modifier: . . . . . no.

.32 Look-Ahead: . . . . . when instructions and data are stored in separate banks, the next instruction can be accessed and partially decoded during execution of the current instruction, reducing execution time by 4 μsec for each load, store, arithmetic, logical, and test instruction.

.33 Interruption

.331 Possible causes

In-out units: . . . . . see next entry.
In-out channels: . . . completion of input, output or external function operation; or input-output error.
Storage access: . . . reference to locked-out core storage area; completion of magnetic drum operation; magnetic drum error.
Processor errors: . . invalid operation, exponent underflow, exponent overflow, divide overflow.
Other: . . . . . real-time clock; external synchronization (supplementary real-time clock or master clock for a multi-processor complex).

.332 Control by routine

Individual control: . . enable or disable external interrupts on all channels or any specific channel.
Method: . . . . . special instructions.
Restriction: . . . . . central processor and core storage error interrupts cannot be locked out; no restriction on external interrupts.

.333 Operator control: . . . none.

.334 Interruption conditions: (1) interrupt enabled; and (2) not currently processing an interrupt condition.

.335 Interruption process

Disabling interruption: automatic.
Registers saved: . . . contents of P-Register (sequence counter) are saved by "return jump" instruction in destination register; other registers by program.
Destination: . . . . . one of 74 fixed locations, depending upon cause.

.336 Control methods

Determine cause: . . automatic; destination depends upon cause.
Enable interruption: . by special instruction before returning to main routine.

.34 Multi-running

.341 Method of control: . . . by EXEX I (see Section 784:191), using the interrupt facilities described above.

.342 Maximum number of programs: . . . . . limited only by hardware availability.

.343 Precedence rules: . . . see 784:191.12

.344 Program protection

Storage: . . . . . Memory Lockout Register, set by a special instruction, specifies address limits (in 2,048-word increments) of the Core Memory areas available for writing.
In-out units: . . . . . none.

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.35 Multi-sequencing: . . . practical only in multi-processor complexes.

.4 PROCESSOR SPEEDS

Conditions

I: . . . . . instructions and operands in alternate core storage banks.

II: . . . . . instructions and operands in same bank.

.41 Instruction Times in μsec

	Condition	I	II
.411	Fixed point		
	Add-subtract:	4.0	8.0.
	Multiply:	12.0	16.0.
	Divide:	31.3	35.3.
.412	Floating point		
	Add-subtract:	14.0	18.0.
	Multiply:	13.3	17.3.
	Divide:	26.7	30.7.
.413	Additional allowance for		
	Indexing:	0	0.
	Indirect addressing, per stage:	4	4.
	Re-complementing: .	0	0.
.414	Control		
	Compare †:	4 to 10	8 to 14.
	Branch:	4	4.
	Compare and branch†:	8 to 14	12 to 18.

† Times vary according to condition tested and result.

.415	Counter control		
	Step:	0	0.
	Step and test:	8	8.
.418	Shift:	4	4.

(Note: Execution time is independent of length of shift, which can be from 1 to 72 bit positions.)

.42 Processor Performance in μsec

	Condition	I	II
.421	For random addresses		
	Fixed point		
	$c = a + b$:	12	24.
	$b = a + b$:	12	24.
	Sum N items, per item:	4	8.
	$c = ab$:	20	32.
	$c = a/b$:	39.3	51.3.
	Floating point		
	$c = a + b$:	22	34.
	$b = a + b$:	22	34.
	Sum N items, per item:	14	18.
	$c = ab$:	21.3	33.3.
	$c = a/b$:	34.7	46.7.
.422	For arrays of data		
	Fixed point		
	$c_i = a_i + b_j$:	16	28.
	$b_j = a_i + b_j$:	16	28.

	Condition:	I	II
.422	For arrays of data (Contd.)		
	Fixed point (Contd.)		
	Sum N items, per item:	8	12.
	$c = c + a_i b_j$:	24	32.
	Floating point		
	$c_i = a_i + b_j$:	26	38.
	$b_j = a_i + b_j$:	26	38.
	Sum N items, per item:	18	22.
	$c = c + a_i b_j$:	35.3	43.3.
.423	Branch based on comparison		
	Numeric data:	40	60.
	Alphabetic data: . . .	40	60.
.424	Switching		
	Unchecked:	12	16.
	Checked:	28.7	44.7.
	List search:	16 + 16N	24 + 20N.
.425	Format control per character		
	Unpack:	?	
	Compose:	?	
.426	Table look-up comparison		
	For a match:	4	4.
	For least or greatest:	4.8	5.2.
	For interpolation point:	4	4.
.427	Bit indicators		
	Set bit in separate location:	8	16.
	Set bit in pattern: . .	12	24.
	Test bit in separate location:	12	16.
	Test bit in pattern: . .	16	24.
	Test AND for B bits: .	20	36.
	Test OR for B bits: . .	20	36.
.428	Moving (full words or 6, 12, or 18 bit fields)		
	1 word:	8	16.
	N words:	12 + 8N	12 + 8N.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Add/subtract overflow:	check	set indicator.
Divide overflow:	check	interrupt.
Exponent overflow:	check	interrupt.
Exponent underflow:	check	interrupt.
Zero divisor:	check	interrupt.
Invalid data:	none.	
Invalid operation:	check	interrupt.
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	none.	
Dispatch of data:	none.	
Reference to locked-out storage area:	check	interrupt.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . Control Console.

.12 Associated Units: . . . Keyboard and Printer.

.13 Description

The Control Console is the operating center of the UNIVAC 1107. It consists of a desk with a 54 by 36 inch top and ultramodern styling, featuring two pillars that reach from floor to ceiling and support a display panel at eye-level height for a seated operator. Built into the desk top are a standard typewriter keyboard and a Teletype Model 28 Page Printer. The keyboard and page printer permit direct communication between the operator and the stored programs. The console controls and displays enable the operator to:

- Start and stop execution of the stored program.
- Clear all Central Computer registers.
- Set any of 15 Selective Jump switches, which can be tested by conditional jump instructions.
- Set any of 4 Selective Stop switches, which can cause the stored program to halt.
- Select any input-output channel for initial loading of a "bootstrap" program.
- Read, set, and/or clear the contents of the P register (the instruction sequence counter).

.13 Description (Contd.)

- Initiate a manual interrupt of the computer program to permit keyboard input at any time.
- Read the setting of the Memory Lockout Register, which shows the areas of Core Memory in which writing is permitted.
- Note the occurrence of excessive temperature, low voltage, initial loading errors, peripheral equipment faults (e.g., illegal operation codes) by means of console indicators.

The contents of the arithmetic registers and index registers cannot be displayed on the console panel, and no direct means is provided for entering data into these registers or into specific Core Memory locations.

The Keyboard is a standard 4-bank typewriter keyboard that can generate the 64 basic Fieldata character codes. The console printer is the Teletype Model 28 Page Printer, which prints 1 character at a time at a peak speed of 10 characters per second. It can print the 26 alphabetic, 10 numeric, and 20 special characters of the Fieldata code and responds to the remaining 8 control codes (e.g., space and carriage return). Output is on a continuous paper roll, 8-1/2 inches wide and up to 5 inches in diameter. All data transfers between the Central Computer and the console input-output units must be programmed on a character-at-a-time basis.

INPUT-OUTPUT: CARD READER

§ 071.

.1 GENERAL

.11 Identity: . . . . . Card Reader. Type 7223.

.12 Description

The Type 7223 Card Reader reads standard 80-column cards at a peak speed of 600 cards per minute, using a conventional picker knife feed, pinch roller drive, and brush sensing system. A similar reader for 90-column cards has been announced, but it is not part of the standard product line at present and detailed specifications are not available.

One Card Reader and one Card Punch can be connected to a Card Control and Synchronizer Unit, forming a Punched Card Subsystem. Each Punched Card Subsystem fully occupies one 1107 input-output channel. The reader and punch in any subsystem can operate concurrently by time-sharing their access demands on Core Memory.

Sixteen different function codes are provided to initiate Card Reader operations. Cards can be fed without reading and read with or without feeding. Other function codes provide for stacker selection and mode selection (translated, column binary, or row binary mode). Initiation of an external interrupt upon completion of a reader operation is optional.

Comprehensive checks are made on reader operations. When any error is detected, the Card Control Unit initiates an external interrupt and transmits a Status Word indicating the type of error to the Central Computer. A bit-by-bit read verification is performed, and an illegal character check (in the translated mode only) accepts only 64 of the 4,096 possible card column codes. Other causes of error interrupts are: full stacker, empty hopper, card jam, misfeed, late stacker selection, and illegal or inappropriate function code. An inappropriate function code is one that cannot be performed because of the particular sequence of Card Reader functions that preceded it.

Upon receipt of the appropriate input Function Words, cards are fed from the input hopper, read and verified at two separate sensing stations, and sent to one of three stackers. Data read from a card is stored in card image form within the Card Control Unit. If the translated mode has been selected, each card column code is translated into a 6-bit internal code. The Channel Synchronizer assembles the 6-bit codes into 36-bit computer words, so the contents of each 80-column card occupy 13 full words and the 12 high-order bit positions of a 14th word. Standard Hollerith card coding and Fieldata internal coding will usually be used when reading in the translated mode, but any desired 12-bit to 6-bit code translation

.12 Description (Contd.)

can be performed if the translated portion of the Card Control Unit buffer storage is manually altered via the maintenance panel.

Full card images can be transferred to Core Memory without translation in either the column binary or row binary mode. In the column binary mode, the bit pattern of each group of three consecutive card columns fills one computer word. In the row binary mode, the bit pattern of each card row fills two computer words and the eight high-order bit positions of a third word. (This differs from the row binary mode used in the IBM 700 and 7000 series scientific systems, in which only 72 card columns are read and the bit pattern of each card row is stored in only two computer words.)

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1962 (with 1107).

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller friction.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . none.
.222 Sensing system: . . . . brush.

.24 Arrangement of Heads

Use of station: . . . . . reading.
Stacks: . . . . . 1.
Heads/stack: . . . . . 80.
Method of use: . . . . . reads 1 row at a time.

Use of station: . . . . . read verification.
Distance: . . . . . 1 card.
Stacks: . . . . . 1.
Heads/stack: . . . . . 80.
Method of use: . . . . . reads 1 row at a time and verifies previously read data on a bit-by-bit basis.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard 80-column cards.
.312 Phenomenon: . . . . . rectangular holes.

.32 Positional Arrangement

.321 Serial by: . . . . . 12 rows.
.322 Parallel by: . . . . . 80 columns.
.324 Track use: . . . . . all for data.
.325 Row use: . . . . . all for data.

§ 071.

.33 Coding

Translated mode:	Hollerith code as in Data Code Table No. 2, or any other column code.
Column binary mode:	full card image.
Row binary mode:	full card image.

.34 Format Compatibility: with all devices using standard 80-column card.

.35 Physical Dimensions: standard 80-column card.

.4 CONTROLLER

.41 Identity: Card Control and Synchronizer Unit. Type 7240 or 7277.

.42 Connection to System

.421 On-line: up to 15 Card Controls, 1 per Punched Card Subsystem. Each subsystem fully occupies 1 input-output channel.

.422 Off-line: none.

.43 Connection to Device

.431 Devices per controller: 1 Card Reader. Type 7240 also controls 1 150 card/min punch. Type 7277 also controls 1 300 card/min punch.

.432 Restrictions: none.

.44 Data Transfer Control

.441 Size of load: 1 card of 14 computer words in translated mode, 27 words in column binary mode, or 36 words in row binary mode.

.442 Input-output area: Core Memory.

.443 Input-output area access: each word or field-defined portion of a word.

.444 Input-output area lockout: none.

.445 Table control: none.

.446 Synchronization: automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: 1 card.

.512 Block demarcation: fixed.

.52 Input-Output Operations

.521 Input: read 1 card, with or without feeding, in translated, column binary, or row binary mode. External interrupt upon completion is optional.

.522 Output: none.

.523 Stepping: feed 1 card but do not read.

.524 Skipping: none.

.525 Marking: none.

.526 Searching: none.

.53 Code Translation: one of the following 3 modes selected by a Function Word.

Translated mode:	translate each card column code into a 6-bit internal code. Any desired codes can be manually inserted via the Card Control Unit maintenance panel.
Column binary mode:	store card image, 3 card columns per 36-bit computer word; zero-fill the 12 least significant bit positions of the 27th word.
Row binary mode:	store card image, with each card row filling 2 computer words and 8 bit positions of a third word; zero-fill the remaining 24 bit position of every third word.

.54 Format Control: mode selection only; see preceding entry (no plugboard).

.55 Control Operations

Disable:	no.
Request interrupt:	yes.
Offset card:	no.
Select stacker:	yes; 1 of 3 stackers.
Select format:	no.
Select code:	yes.

.56 Testable Conditions

Disabled:	yes.
Busy device:	no.
Nearly exhausted:	no.
Busy controller:	yes.
Hopper empty:	yes.
Stacker full:	yes.

.6 PERFORMANCE

.61 Conditions: see Paragraph .63.

.62 Speeds

.621 Nominal or peak speed: 600 cards/minute.

.622 Important parameters

Name	Value
Sensing and storing of data:	82.4 msec/card.
Dead time:	17.6 msec/card at peak speed.
Stacker select delay:	maximum of 100 msec after input instructions.

.623 Overhead: 15 clutch points per 100 msec cycle.

.624 Effective speeds: 600 cards/minute when reading continuously.

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.63 Demands on System

Component	Condition	Msec per card	Percentage
Core Memory:	translated mode	0.056	0.056.
	column binary	0.108	0.108.
	row binary	0.144	0.144.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Run:	button	reads 3 cards and stores their contents in Card Reader memory.
I/O Clear:	button (on Control Console)	clears control circuits, indicators, and Card Reader memory.
Resume:	button	restarts reader after a halt.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	1,000 cards.
Stacker:	3 stackers; 1,000 cards each.

.732 Replenishment time: . . 0.25 minute; reader does not need to be stopped.

.734 Optimum reloading period: . . . . . 1.67 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	re-read and compare	interrupt; route card to error stacker.
Input area overflow:	none.	
Invalid code:	check (in translated mode only)	interrupt.
Imperfect medium:	none.	
Timing conflicts:	check	interrupt.
Hopper empty:	check	interrupt.
Stacker full:	check	interrupt.
Card jam:	check	interrupt.

Note: The type of error is indicated by bits 30 to 35 of the Status Word, sent to the Central Computer when an interrupt occurs.

INPUT-OUTPUT: CARD PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . . Card Punch.
Type 7224 (150 cards/min).

.12 Description

The Type 7224 Card Punch punches and verifies standard 80-column cards at a peak speed of 150 cards per minute. One Card Punch and one Card Reader can be connected to a Card Control and Synchronizer Unit, forming a Punched Card Subsystem. Each subsystem fully occupies one 1107 input-output channel. The reader and punch in any subsystem can operate concurrently by time-sharing their access demands on Core Memory.

Ten different function codes are provided to initiate Card Punch operations. The function codes determine which of two stackers will be selected, which of three translation modes will be used, and whether or not an external interrupt will be initiated upon completion of the punch operation. Cards fed from the input hopper pass the following stations at one-card intervals: two read stations (which are not used in an 1107 system), the punch station, a "wait" station, and the read verification station. Cards are block-punched; i.e., all 12 rows are punched at the same time, whereas most card punches punch one row at a time. A maximum of 240 holes can be punched into any 1 card. This characteristic represents a serious limitation on the punching of full-card binary images, because any or all of the 960 positions on the card may need to be punched to represent binary "1" bits. When the binary punching capability is required, use of the 300-card-per-minute punch is recommended.

Comprehensive checks are made on Card Punch operations. When any error is detected, the Card Control Unit initiates an external interrupt and transmits a Status Word indicating the type of error to the Central Computer. All punched data is read back and verified on a bit-by-bit basis. A character validity check (in the translated mode only) can detect any of up to 12 code combinations designated as illegal codes by the user. Other causes of error interrupts are: full stacker, empty hopper, card jam, misfeed, an attempt to punch more than 240 holes into one card, and an illegal or inappropriate function code. An innappropriate function code is one that cannot be performed because of the particular sequence of Card Reader functions that preceded it.

Upon receipt of the appropriate output Function Words, the Channel Synchronizer disassembles 36-bit computer words into 6-bit character codes and transmits them to buffer storage in the Card Control Unit. If the translated mode has been selected, each 6-bit code is translated into one card column code.

.12 Description (Contd.)

The contents of 13 full computer words and the 12 high-order bit positions of a 14th word are then punched into one 80-column card. Standard Fieldata internal coding and Hollerith card coding is usually used when punching the translated mode, but any desired 6-bit to 12-bit code translation can be performed if the translate portion of the Card Control Unit buffer is manually altered via the maintenance panel.

Full card images can be transferred from Core Memory to cards without translation in either the column binary or row binary mode. However, the limitation of 240 holes per card previously noted makes it necessary to zero-fill most of the Core Memory locations whose contents are to be punched in either binary mode.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1962 (with 1107).

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller friction.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . die punch.
.222 Sensing system: . . . . brush.
.223 Common system: . . . no.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . punching.
Stacks: . . . . . 1.
Heads/stack: . . . . . 960.
Method of use: . . . . . punches 1 full card at a time.

Use of station: . . . . . reading (for verification of punching).
Distance: . . . . . 2 cards after punch station.
Stacks: . . . . . 1.
Heads/stack: . . . . . 80.
Method of use: . . . . . reads 1 row at a time.

Note: Two more read stations precede the punch station; they are not used in 1107 programming.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . standard 80-column cards.

§ 072.

.312 Phenomenon: . . . . . rectangular holes.

.32 Positional Arrangement

.321 Serial by: . . . . . 1 card for punching.
12 rows for checking.
.322 Parallel by: . . . . . 960 punch positions for punching.
80 columns for checking.
.324 Track use: . . . . . all for data.
.325 Row use: . . . . . all for data.

.33 Coding

Translated mode: . . . Hollerith code as in Data Code Table No. 2, or any other column code.
Column binary mode: . full card image.
Row binary mode: . . . full card image.

.34 Format Compatibility:. with all devices using standard 80-column cards.

.35 Physical Dimensions: . standard 80-column cards.

.4 CONTROLLER

.41 Identity: . . . . . Card Control and Synchronizer Unit. Type 7240.

.42 Connection to System

.421 On-line: . . . . . up to 15 Card Controls, 1 per Punched Card Subsystem. Each subsystem fully occupies 1 input-output channel.

.43 Connection to Device

.431 Devices per controller: 1 Card Punch and 1 Card Reader.
.432 Restrictions:. . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 card of 14 computer words in translated mode, 27 words in column binary mode, or 36 words in row binary mode.
.442 Input-output area: . . . Core Memory.
.443 Input-output area access: . . . . . each word or field-defined portion of a word.
.444 Input-output area lockout:. . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 card.
.512 Block demarcation: . . fixed.

.52 Input-Output Operations

.521 Input:. . . . . none.
.522 Output: . . . . . punch 1 card in translated, column binary, or row binary mode; advance all cards 1 station; and feed 1 card. External interrupt upon completion is optional.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . one of the following 3 modes, selected by a Function Word.
Translated mode: . . . translate each 6-bit internal code into 1 card column code. Any desired codes can be manually inserted via the Card Control Unit maintenance panel.
Column binary mode: . punch full card image, 3 card columns per 36-bit computer word.
Row binary mode: . . . punch full card image, 1 card row for every 3 computer words (2 full words and the high-order 8 bits of the third word).

.54 Format Control: . . . . mode selection only; see preceding entry (no plugboard).

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . yes.
Offset card: . . . . . no.
Select stacker: . . . . yes, 1 of 2 stackers.
Select format: . . . . . no.
Select code: . . . . . yes.

.56 Testable Conditions

Disabled:. . . . . yes.
Busy device: . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
Hopper empty: . . . . . yes.
Stacker full: . . . . . yes.

.6 PERFORMANCE

.61 Conditions:. . . . . see Paragraph .63.

.62 Speeds

.621 Nominal or peak speed: 150 cards/minute.
.622 Important parameters

Name	Value
Translate and transfer data: . . .	256.9 msec/card.
Punch:.	134.1 msec/card.

.623 Overhead: . . . . . 18 clutch points per 400 msec cycle.
.624 Effective speeds: . . . 150 cards/minute when reading continuously.

§ 072.

.63 Demands on System

Component	Condition	Msec per card	Percentage
Core Memory:	translated mode	0.056	0.014.
	column binary	0.108	0.027.
	row binary	0.144	0.036.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Run:	button	initiates punch operation.
Resume:	button	restarts punch after a halt.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	700 cards.
Stackers:	2 stackers; 850 cards each.

.732 Replenishment time: . . 0.25 minute; punch does not need to be stopped.

.734 Optimum reloading period: . . . . . 4.67 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read back and compare	interrupt; route card to error stacker.
Output block size:	fixed; no check.	
Invalid code:	check (in translated mode only)	interrupt.
Imperfect medium:	none.	
Timing conflicts:	check	interrupt.
Hopper empty:	check	interrupt.
Stacker full:	check	interrupt.
Card jam:	check	interrupt.
More than 240 holes per card:	check	interrupt.

Note: The type of error is indicated by bits 30 to 35 of the Status Word, sent to the Central Computer when an interrupt occurs.

INPUT-OUTPUT: PAPER TAPE READER

§ 075.

.1 GENERAL

.11 Identity: . . . . . Paper Tape Reader. (Part of Paper Tape Subsystem, Type 7423).

.12 Description

The Paper Tape Reader is a modified Digitronics Model B3500 reader with a peak speed of 400 characters per second. It is an integral part of the UNIVAC 1107 Paper Tape Subsystem, a single cabinet which also houses a 110 character per second punch (described in Section 784:076) and a control unit.

The reader is mounted vertically, and the tape is fed down into it from a supply reel with a tension arm reservoir. No take-up facilities are provided. Reading is performed photoelectrically by silicon photo-diodes. Tape can be read backward as well as forward, but backward movement may not exceed 12 inches (120 characters). The reader can handle tape with 5, 6, 7, or 8 data tracks and 11/16, 7/8, or 1 inch in width. Because all code translation must be programmed, any tape code can be used.

The Paper Tape Subsystem does not include a Channel Synchronizer for the assembly of characters into 1107 words. Therefore, the reader must communicate directly with the computer on a character-by-character basis. Character codes read from the tape are transferred without translation into the eight low-order bit positions of consecutive word locations in Core Memory. No automatic parity checking is provided. When a parity check is required, it must be accomplished through a program subroutine. (The 1107 has special instructions that facilitate programmed parity checking.) The standard program sequence used to read a block of data from punched tape consists of six Instruction Words, three Access-Control Words, and two Function Words.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1963.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch rollers.
.212 Reservoir: . . . . . tension arm, serving supply reel only.

.22 Sensing and Recording Systems

.221 Recording system: . . . none.
.222 Sensing system: . . . . photo-electric (silicon photo-diodes).

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . reading.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8 (plus sprocket head).
Method of use: . . . . . reads 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . paper or plastic tape.
.312 Phenomenon: . . . . . punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . row, at 10 rows/inch.
.322 Parallel by: . . . . . 5, 6, 7, or 8 data tracks at standard spacing.
.324 Track use
Data: . . . . . 5, 6, 7, or 8.
Redundancy check: . . 0 (parity check can be programmed).
Timing: . . . . . 1 (sprocket track).
Control signals: . . . 0.
Unused: . . . . . 0.
Total: . . . . . 5, 6, 7, or 8 (plus sprocket track).
.325 Row use: . . . . . all for data.

.33 Coding: . . . . . any 5-, 6-, 7-, or 8-track tape code; code translation is programmed.

.34 Format Compatibility: . with all devices using standard punched tape.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.687, 0.875, or 1.0 inch.
.352 Length: . . . . . up to 600 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . Paper Tape Control Unit. (Part of Paper Tape Subsystem, Type 7423).

.42 Connection to System

.421 On-line: . . . . . up to 15; each subsystem fully occupies one 1107 input-output channel.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 Paper Tape Reader and 1 Paper Tape Punch.
.432 Restrictions: . . . . . none.

§ 075.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 character.
.442 Input-output area: . . . low-order 8-bit positions of consecutive Core Memory locations.
.443 Input-output area access: . . . . . each word, or field-defined portion of a word.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . accomplished by standard input instruction sequence.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . limited only by tape length.
.512 Block demarcation: . . character count in Access-Control Word.

.52 Input-Output Operations

.521 Input: . . . . . feed tape forward or backward 1 row and read 1 character into the low-order 8-bit positions of a Core Memory location. (Backward tape movement may not exceed 12 inches.)
.522 Output: . . . . . none.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . by program.

.54 Format Control: . . . . by program.

.55 Control Operations

Enable: . . . . . yes; "reader on".
Disable: . . . . . yes; "reader off".
Request interrupt: . . . no.
Select format: . . . . . no.
Select code: . . . . . no.
Rewind: . . . . . no.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
Exhausted medium: . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 400 char/sec.

.622 Important parameters
Tape speed: . . . . . 40 inches/sec.
Start time: . . . . . 2.5 msec.
Stop time: . . . . . 2.5 msec.

.624 Effective speed: . . . . 400 char/sec.

.63 Demands on System

Component: . . . . . Central Computer.
Msec per char: . . . . 0.004.
or
Percentage: . . . . . 0.16.

Note: When standard input instruction sequence is used, Central Computer is occupied throughout the data transfer operation.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . tape width.
Method: . . . . . 3-position detent action of tape guides.

.72 Other Controls

Function	Form	Comment
Master Clear:	button/light	clears all error conditions and reinitiates normal communication.
Tape Fault:	button/light	clears "out-of-tape" error conditions.
Tape Load:	button/light	engages tape drive rollers and brakes.

.73 Loading and Unloading

.731 Volumes handled: . . . up to 600 feet per reel.
.732 Replenishment time: . . 1 to 2 minutes; reader needs to be stopped.
.734 Optimum reloading period: . . . . . 3 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	none†	
Input area overflow:	none.	
Invalid codes:	all codes valid.	
Exhausted medium:	check	interrupt.
Imperfect medium:	none.	
Timing conflicts:	none.	
Broken tape:	check	interrupt.

† Parity checking can be performed by the stored program, but is not incorporated into the hardware.

INPUT-OUTPUT: PAPER TAPE PUNCH

§ 076.

.1 GENERAL

.11 Identity: . . . . . Paper Tape Punch. (Part of Paper Tape Subsystem, Type 7423).

.12 Description

The Paper Tape Punch is a modified Teletype BRPE-11 punch with a peak speed of 110 characters per second. This unit is an integral part of the UNIVAC 1107 Paper Tape Subsystem, a single cabinet which also houses a 400 character per second reader (described in Section 784:075) and a control unit.

Tape is fed to the punch from a supply reel with a tension arm reservoir, but no take-up facilities are provided. The punch can handle tape with five, six, seven, or eight data tracks and of 11/16, 7/8, or 1 inch width. Because all code translation must be programmed, any tape code can be used.

The Paper Tape Subsystem does not include a Channel Synchronizer to handle the disassembly of 1107 words into individual characters. Therefore, the computer must communicate directly with the punch on a character-by-character basis. Character codes to be punched on tape are transferred without translation from the eight low-order bit positions of consecutive Core Memory locations. If a parity check is required when the tape is read, the proper parity bit for each character code must be generated by the stored program. The standard program sequence used to punch a block of data consists of seven Instruction Words, three Access-Control Words, and two Function Words.

As each punch is activated, it closes a switch which verifies that punching actually took place in that position. The pattern of holes (or "1" bits) actually punched in each tape row is then compared with the desired pattern. An invalid comparison halts the punching operation, initiates an external interrupt, and places a signal on the level-1 data line to indicate the reason for the interrupt.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket drive.
.212 Reservoir: . . . . . tension arm, serving supply reel only.

.22 Sensing and Recording Systems

.221 Recording system: . . . die punches.
.222 Sensing system: . . . . none.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . punching.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8 (plus sprocket punch).
Method of use: . . . . . punches 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . paper or plastic tape.
.312 Phenomenon: . . . . . punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . row, at 10 rows/inch.
.322 Parallel by: . . . . . 5, 6, 7, or 8 tracks at standard spacing.

.324 Track use
Data: . . . . . 5, 6, 7, or 8.
Redundancy check: . . 0 (parity check can be programmed).
Timing: . . . . . 1 (sprocket track).
Control signals: . . . 0.
Unused: . . . . . 0.
Total: . . . . . 5, 6, 7, or 8 (plus sprocket track).

.325 Row use: . . . . . all for data.

.33 Coding: . . . . . any 5-, 6-, 7-, or 8-track tape code; code translation is programmed.

.34 Format Compatibility: . with all devices using standard punched tape.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.687, 0.875, or 1.0 inch.
.352 Length: . . . . . up to 600 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . Paper Tape Control Unit. (Part of Paper Tape Subsystem, Type 7423).

.42 Connection to System

.421 On-line: . . . . . up to 15; each subsystem fully occupies one 1107 input-output channel.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 Paper Tape Reader and 1 Paper Tape Punch.
.432 Restrictions: . . . . . none.

§ 076.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 character.
.442 Input-output area: . . . low order 8 bit positions of consecutive Core Memory locations.
.443 Input-output area access: . . . . . each word, or field-defined portion of a word.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . accomplished by standard input instruction sequence.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . limited only by tape length.
.512 Block demarcation: . . character count in Access-Control Word.

.52 Input-Output Operations

.521 Input: . . . . . none.
.522 Output: . . . . . punch 1 character from the 8 low-order bit positions of a core memory location and advance tape 1 row.
.523 Stepping: . . . . . none.
.524 Skipping: . . . . . none.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . by program.

.54 Format Control: . . . . by program.

.55 Control Operations

Enable: . . . . . yes; "punch on".
Disable: . . . . . yes; "punch off".
Request interrupt: . . . no.
Select format: . . . . . no.
Select code: . . . . . no.
Rewind: . . . . . no.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
Exhausted medium: . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 110 char/sec.
.622 Important parameters
Tape speed: . . . . 11 inches/sec.
.624 Effective speed: . . . 110 char/sec.

.63 Demands on System

Component: . . . . . Central Computer.
Msec per char: . . . . 0.004.
or
Percentage: . . . . . 0.044.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . tape width.
Method: . . . . . 3-position detent action of tape guides.

.72 Other Controls

Function	Form	Comment
Master Clear:	button/light	clears all error conditions and reinitiates normal communication.
Tape Fault:	button/light	clears "out-of-tape" error conditions.
Miscompare:	button/light	clears punching error condition.
Tape Feed:	button/light	feeds tape, causing sprocket holes to be punched.

.73 Loading and Unloading

.731 Volumes handled: . . . up to 1,000 feet per reel.
.732 Replenishment time: . . 1 to 2 minutes; reader needs to be stopped.
.734 Optimum reloading period: . . . . . 5 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	none. †	
Input area overflow:	none.	
Invalid codes:	all codes valid.	
Exhausted medium:	check	interrupt.
Imperfect medium:	none.	
Timing conflicts:	none.	
Broken tape:	check	interrupt.

† Parity checking can be performed by the stored program, but is not incorporated into the hardware.

INPUT-OUTPUT: PRINTER (600 Lines/Min.)

§ 081.

.1 GENERAL

.11 Identity: . . . . . High-Speed Printer.
Model 46.
Type 7418.

.12 Description

The UNIVAC Model 46 High-Speed Printer has a peak speed of 600 single-spaced lines per minute. At an average line spacing of one inch, its effective speed is 424 lines per minute. One printer can be connected to a High-Speed Printer Control and Synchronizer Unit, forming a High-Speed Printer Subsystem. Each subsystem fully occupies one 1107 input-output channel.

The printer has a 51-character set and 128 print positions, spaced ten per inch. Vertical spacing is six lines per inch. There is no paper tape carriage control loop, so the computer program must count its way over pre-printed forms. The forms can be advanced from 0 to 63 lines prior to printing each line, at a maximum speed of 20 inches per second.

A printer Function Word, sent by the Central Computer to the control unit, initiates each print operation. The Function Word specifies the number of lines to be stepped and indicates whether or not there shall be an external interrupt upon completion of the print operation. The 128 characters to be printed, in the six-bit Fieldata code, occupy 21 full words and the 12 high-order bit positions of a 22nd word in Core Memory. If a "stop" code (binary 111111) is encountered in the data before all 128 characters have been transferred to the printer buffer, the data transfer is terminated and the remaining print positions are space-filled.

No checks for accuracy are made upon the transfer of data to the printer or the print operation itself. Although there are only 51 printable characters, all of the 64 Fieldata code combinations are valid: there are 12 different codes for "space," plus the special stop code. External interrupts are initiated upon detection of exhausted forms, exhausted ribbon, excessive temperature, improper printer selection, or an illegal Function Word.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1962 (with 1107).

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprockets.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . on-the-fly hammer strokes press paper against ribbon and engraved typewheels.
.222 Sensing system: . . . . none.

.23 Multiple Copies

.231 Maximum number: . . . original and four clear copies, using 12-pound stock with interleaved carbons.
.233 Types of master
Multilith: . . . . . yes.
Spirit: . . . . . yes.

.24 Arrangement of Heads

Use of station: . . . . . printing.
Stacks: . . . . . 1.
Heads/stack: . . . . . 128.
Method of use: . . . . . prints 1 line at a time.

.25 Range of Symbols

Numerals:	10	0 to 9.
Letters:	26	A to Z.
Special:	15	= > < - $. ; ( ) / , + * &
Alternatives:		upon special request.
FORTRAN set:		yes.
Basic COBOL set: . . .		yes, substituting ' for COBOL " .
Total:	51 and blank.	

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . continuous, fanfold, sprocket-punched stationery.
.312 Phenomenon: . . . . . printing.

.32 Positional Arrangement

.321 Serial by: . . . . . 6 lines per inch.
.322 Parallel by: . . . . . 128 print positions at 10 per inch.
.324 Track use: . . . . . all for data.
.325 Row use: . . . . . all for data.

.33 Coding: . . . . . engraved character font; Fieldata internal code as in Data Code Table No. 1, Section 784:141.

.34 Format Compatibility: . none.

§ 081.

.35 Physical Dimensions

.351 Overall width: . . . . . 4 to 27 inches by vernier.
.352 Length: . . . . . maximum of 22 inches fold-to-fold.

.4 CONTROLLER

.41 Identity: . . . . . High-Speed Printer Control and Synchronizer Unit. Type 7239.

.42 Connection to System: . up to 15 controllers, 1 per Printer Subsystem. Each subsystem fully occupies 1 input-output channel.

.43 Connection to Device

.431 Devices per controller: 1 printer.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 line of up to 128 characters (22 computer words).
.442 Input-output area: . . . Core Memory.
.443 Input-output area access: . . . . . each word or field-defined portion of a word.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 line.
.512 Block demarcation: . . fixed; 128 characters per line. (Data transfer from Core Memory is halted if a stop code consisting of six "1" bits is detected before 128 characters have been transferred; in this case, the remaining print positions are space-filled.)

.52 Input-Output Operations

.521 Input: . . . . . none.
.522 Output: . . . . . transfer up to 128 characters from Core Memory to printer buffer; advance paper 0 to 63 line spaces, and print 1 line with optional external interrupt upon completion.
.523 Stepping: . . . . . 0 to 63 line spaces forward, combined with print operation only; stepping precedes printing.
.524 Skipping: . . . . . see preceding entry; no carriage control tape.
.525 Marking: . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . . automatic.

.54 Format Control: . . . . by program (no plugboard).

.55 Control Operations

Disable: . . . . . no.
Request interrupt: . . . yes.
Select format: . . . . . no.
Select code: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
Exhausted medium: . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 600 lines/minute.
.622 Important parameters
Skipping speed: . . . . 20 inches/sec.
.624 Effective speeds: . . . $7,200/(N + 11)$ lines/minute, where N is average number of lines advanced.

.63 Demands on System

Component	msec per line	or	Percentage
Core Memory:	0.088		0.088.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method
Vertical alignment: . .	calibrated dial.
Form width:	sliding forms tractor.
Form thickness:	calibrated dial.

.72 Other Controls

Function	Form	Comment
Carriage In/Out:	2 buttons	move ribbon and type-wheel carriage in or out.
Change Ribbon:	button	winds ribbon completely onto take-up shaft.
Space Ribbon:	button	advances from 1 line space.
Clear:	button	resets controls, indicators, and flip-flops.
Computation Run:	button.	
Computation Stop:	button.	

§ 081.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Feed hopper:	12-inch stack.
Stacker:	12-inch stack.

.732 Replenish time: . . . . 1 to 2 minutes; printer needs to be stopped.

.733 Adjustment time: . . . 2 to 3 minutes.

.734 Optimum reloading period: . . . . . 41 minutes.

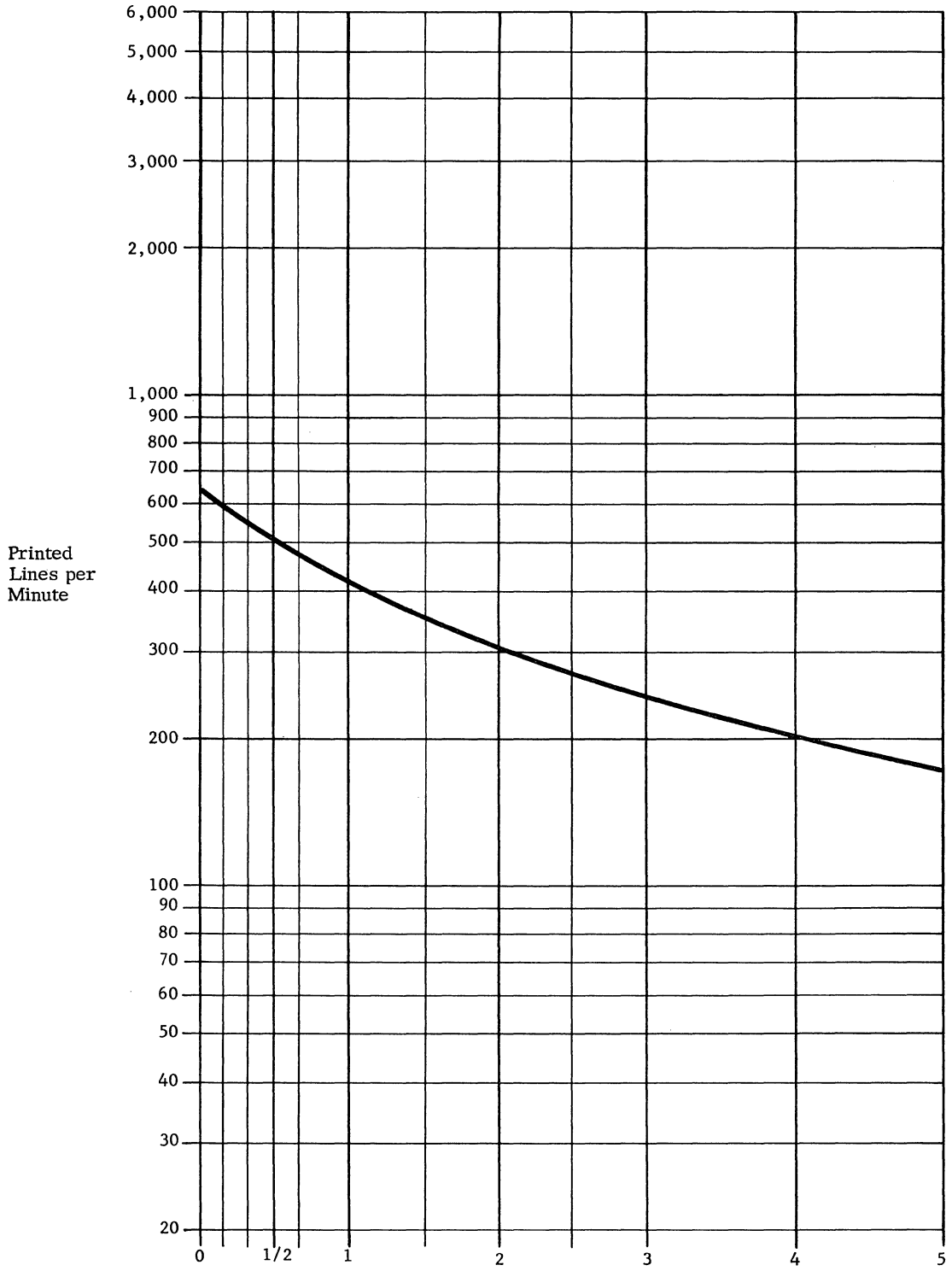
Basis: 12-inch stack of 2-part sets, 17 inches long, at 1-inch line spacing.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Output block size:	none	cut off at 128 chars.
Invalid code:	all codes valid	12 different codes produce "space".
Exhausted medium:	check	interrupt.
Exhausted ribbon:	check	interrupt.
Illegal function:	check	interrupt.
Excessive temperature:	check	interrupt.

Note: The type of error is indicated by bits 30-35 of the Status Word, sent to the Central Computer when an interrupt occurs.

EFFECTIVE SPEED
HIGH-SPEED PRINTER, TYPE 7418



INPUT-OUTPUT: UNISERVO IIA

§ 091.

.1 GENERAL

.11 Identity: . . . . . Uniservo IIA Magnetic Tape Handler. Type 7242.

.12 Description

The Uniservo IIA provides magnetic tape input-output for the UNIVAC 1107 at substantially lower speed and cost than the Uniservo IIIA and IIIC tape handlers described in the following report sections. A magnetic tape subsystem consists of 2 to 12 Uniservo IIA tape handlers connected to a Uniservo IIA Control and Synchronizer Unit and a Power Supply. Each subsystem occupies one 1107 input-output channel, and only one tape handler per subsystem can read or write at a time. A panel of dial switches is used to change the logical addresses assigned to the individual tape handlers.

Data can be recorded on either plastic-base or metallic tape, at a packing density of 125 or 250 rows per inch. (Data recorded by the Unityper keyboard-to-magnetic-tape transcriber at 50 rows per inch can be read, but the Uniservo IIA cannot record at this density.) Tape velocity is 100 inches per second, providing a peak data transfer rate of 12,500 or 25,000 characters per second, depending upon the recording density selected. Each tape row contains six data bits, one clock bit, and one parity bit, and can represent one alphameric character. Six tape rows are used to represent each 36-bit 1107 word. Block length is variable from 1 to 65,535 words. Tape width and densities are compatible with those of the Uniservo tape handlers used in the UNIVAC II, III, and Solid-State 80/90 systems, but these three systems require tape blocks to be of fixed length. There is no tape compatibility with the Uniservo IIIA or IIIC tape handlers.

A Uniservo IIA operation can be initiated by any of 36 different function codes. The function code can specify whether recording shall be at 125 or 250 rows per inch, whether reading shall be in the forward or reverse direction, and whether or not an external interrupt shall occur upon normal completion of a tape operation. Tape searching, an unusual and valuable feature, is possible in either the forward or reverse direction. The first word of each tape block is read and compared to an Identifier Word. When a match occurs, the entire block is read into Core Memory and the operation is terminated.

Each tape read operation requires two instruction words, two Access-Control Words and one Function Word in the stored program. Tape writing requires three instructions, two Access-Control Words, and one Function Word. A Status Word is transmitted from the tape control unit to the Central Computer

.12 Description (Contd.)

whenever a tape error (e.g., incorrect parity) occurs, and also upon normal completion of a tape operation when an external interrupt has been specified. Bit positions 32 through 35 of the Status Word contain a status code that can be tested to determine the reason for the interrupt and the nature of the tape error, if any has occurred. The other 32 bits of the Status Word are unused.

A row parity check is made upon tape reading, but there is no check upon recording accuracy. Any one of three amplifier gain levels can be specified when reading. A metal ring inserted into the supply reel prevents the execution of write commands; the function of this file protection device is the opposite of the "write enable" rings used in most other tape handlers, including the Uniservo IIIA and IIIC.

All tapes should be pre-tested off-line to detect and mark any flaws. Bad spots on metallic tape are marked by perforating the tape in the bad area with a special hand punch. Bad spots on plastic tape are marked by manually scraping off the oxide coating. The areas so marked are automatically skipped over during read and write operations.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . September, 1962 (with 1107).

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . single clutched capstan.
.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum column.
Capacity: . . . . . 6 feet of tape.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by magnetic write head.
.222 Sensing system: . . . . magnetic head.
.223 Common system: . . . yes; common read/write head.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . . 1 row at a time.

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.24 Arrangement of Heads (Contd.)

Use of station:	read/write.
Stacks:	1.
Heads/stack:	8.
Method of use:	1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium:	metal or plastic tape with magnetizable surface.
.312 Phenomenon:	magnetization.

.32 Positional Arrangement

.321 Serial by:	row, at 125 or 250 rows per inch. (Tape produced by a Unityper at 50 rows per inch can be read but not written).
.322 Parallel by:	8 tracks.
.324 Track use	
Data:	6.
Redundancy check:	1 (odd parity).
Timing:	1 (clock).
Control signals:	0.
Unused:	0.
Total:	8.
.325 Row use, per N-word block	
Data:	6 to 6N.
Redundancy check:	0.
Timing:	0.
Control signals:	0.
Inter-block gap:	1.05 inches.

.33 Coding:	binary image; 6 tape rows per 1107 word.
.34 Format Compatibility:	with Uniservo II and IIA units in other UNIVAC systems, and (at 50 rows/inch) with Unityper keyboard-to-magnetic tape unit.

.35 Physical Dimensions

.351 Overall width:	0.50 inch.
.352 Length	
Plastic-base tape:	2,400 feet per reel.
Metal tape:	1,500 feet per reel.

.4 CONTROLLER

.41 Identity:	Uniservo IIA Control and Synchronizer. Type 7214.

.42 Connection to System

.421 On-line:	up to 15 Control and Synchronizer units; each fully occupies 1 input-output channel.
.422 Off-line:	none.

.43 Connection to Device

.431 Devices per controller:	2 to 12.
.432 Restrictions:	none.

.44 Data Transfer Control

.441 Size of load:	1 to 65,535 words.
.442 Input-output area:	Core Memory.
.443 Input-output area access:	each word or field-defined portion of a word.
.444 Input-output area lockout:	none.
.445 Table control:	none.
.446 Synchronization:	automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block:	1 to 65,535 words.
.512 Block demarcation	
Input:	interblock gap on tape, or word count in Access-Control Word.
Output:	word count in Access-Control Word.

.52 Input-Output Operations

.521 Input:	read 1 block of data forward or backward at low, normal, or high gain, with or without external interrupt upon completion.
.522 Output:	write 1 block of data forward at 125 or 250 rows/inch, with or without external interrupt upon completion.
.523 Stepping:	none.
.524 Skipping:	automatic, across tape flaws marked in a previous edit operation.
.525 Marking:	file separator, interblock gap.
.526 Searching:	read first word (forward) or last recorded word (backward) of each block and compare it with an Identifier Word. When a match occurs, read the block.

.53 Code Translation:	none; binary images of data in internal storage are recorded on tape in an interlaced (i.e., "scrambled") pattern with clock and parity bits added.
.54 Format Control:	by program.

.55 Control Operations

Disable:	yes, following rewind with interlock.
Request interrupt:	yes.
Select format:	no.
Select code:	no.
Rewind:	yes.

§ 091.

.55 Control Operations (Contd.)

Unload:	no; not required, because tape leader remains on handler.
Terminate current operation:	yes.
Select density:	yes; 125 or 250 rows/inch.
Select amplifier gain:	yes; 3 levels.

.56 Testable Conditions

Disabled:	yes.
Busy device:	no.
Output lock:	no.
Nearly exhausted:	no.
Busy controller:	yes.
End of medium marks:	yes.
End of file:	yes.
Rewinding:	no.

.6 PERFORMANCE

.61 Conditions

I:	250 rows/inch, in stop/start mode.
II:	250 rows/inch, in continuous mode.
III:	125 rows/inch, in stop/start mode.
IV:	125 rows/inch, in continuous mode.

Note: Stop/start mode is used unless next tape function is initiated within 4 msec after last character of each block is read or written.

.62 Speeds

.621 Nominal or peak speed

I:	25,000 char/sec.
II:	25,000 char/sec.
III:	12,500 char/sec.
IV:	12,500 char/sec.

.622 Important parameters

Recording density:	125 or 250 rows/inch.
Tape speed:	100 inches/sec.
Rewind time:	4.8 minutes per reel.
Inter-block gap:	1.05 inches.
End of file gap:	4.50 inches.
Start time:	5 msec.
Stop time:	5 msec.

.623 Overhead, per block

I:	27.5 msec.
II:	10.5 msec.
III:	27.5 msec.
IV:	10.5 msec.

.624 Effective speeds

I:	25,000N/(N + 688) char/sec.
II:	25,000N/(N + 262) char/sec.
III:	12,500N/(N + 344) char/sec.
IV:	12,500N/(N + 131) char/sec.

where N is number of characters (i.e., tape rows) per block.

.63 Demands on System

Component	Condition	msec per word	or	Percentage of data transfer time
Core Memory:	I & II	0.004		1.67.
	III & IV	0.004		0.83.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment:	metal to plastic tape.
Method:	switch.

.72 Other Controls

Function	Form	Comment
Manually Run:	switch	starts or stops unit.
Rewind:	button	manual rewind.
Change Tape:	button	returns unit to system control.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity, per reel
Plastic-base tape:	2,400 feet, or 5,600,000 characters in 1,000-character blocks at 250 rows/inch.
Metal tape:	1,500 feet, or 3,400,000 characters in 1,000-character blocks at 250 rows/inch.

.732 Replenishment time: 0.5 to 1.0 minute; tape unit power needs to be turned off.

.734 Optimum reloading period

Plastic-base tape:	4.8 minutes.
Metal tape:	3.0 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Reading:	row parity check	interrupt.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	check	interrupt.
Imperfect medium:	check	skip pre-marked bad spots.
Character count:	modulo 6 check on input	interrupt.
Illegal function code:	check	interrupt.
Illegal unit address:	check	interrupt.

Note: The type of error is indicated by bits 32 through 35 of the Status Word, sent to the Central Computer when an interrupt occurs.

INPUT-OUTPUT: UNISERVO IIIA

§ 092.

.1 GENERAL

.11 Identity: . . . . . Uniservo IIIA Magnetic Tape Handler. Type 7289.

.12 Description

The Uniservo IIIA provides high speed magnetic tape input-output for the UNIVAC 1107 system. From 2 to 16 Uniservo IIIA tape handlers can be connected to a Uniservo IIIA Control and Synchronizer Unit and a Uniservo Power Supply, forming a Magnetic Tape Subsystem. Each subsystem ordinarily occupies one input-output channel, and only one tape handler per subsystem can read or write at a time. Alternatively, a dual-control synchronizer that occupies two input-output channels can be used to control each Magnetic Tape Subsystem. In this case, simultaneous read/write or read/read (but not write/write) operations involving any two tape handlers in a subsystem can occur. Other alternative models of the Control and Synchronizer permit either of two 1107 Central Computers to communicate with the tape units in a single subsystem.

Data is recorded by the "pulse phase" method at a density of 1,000 rows per inch. Nine tracks are recorded across the tape, one of which is always used as a parity track. In the standard recording format, five tape rows are used to represent each 36-bit 1107 word; the first three rows contain eight data bits each, and the last two rows of each five-row group contain only six data bits each. An optional format, selected through plugboard switching, uses six tape rows per word, with only six data bits (i.e., one alphameric character) per row. Tape velocity is 100 inches per second, providing the following peak data transfer rates:

	Standard Format (5 rows per word)	Optional Format (6 rows per word)
Rows per second:	100,000	100,000
1107 words per second:	20,000	16,667
6-bit characters per second:	120,000	100,000

An unusual and valuable feature of the Uniservo IIIA is its ability to search for a specific tape record in either the forward or reverse direction. The first data word in each block is read and compared with all or any specified portion of an Identifier Word. When a match occurs, the entire block is read into Core Memory and the search is terminated.

The pulse phase recording method represents "0" and "1" bits by the direction of change in magnetic polarity. A change from negative to positive indicates a "0", while a change from positive to negative indicates a "1." Polarity changes representing bits are recorded on the tape at 10 microsecond intervals. When two "0" bits or two "1" bits occur in adjacent rows, a "non-significant" polarity change in the reverse direction must be inserted midway between them. These non-significant polarity changes are detected but ignored by the read circuitry. Unlike most tape recording systems, the pulse phase method permits "blank" tape (i.e., tape codes representing neither "0" nor "1" bits) to be written and read.

.12 Description (Contd.)

The main advantage of the pulse phase method is that it permits self-clocking of each track on the tape. The self-clocking, in turn, makes high density recording practical by permitting automatic compensation for "skew" (i.e., the arrival of the bits comprising a tape row at their respective read heads at different times because the tape rows are not precisely parallel to the stack of read heads).

As each block of data is recorded, the control unit automatically "surrounds" it by writing a 27-row pattern (containing "1"s in all tracks) and a 3-row sentinel both before and after the data itself. The pattern and sentinel alert the reading circuits to the beginning and end of data, whether the block is read forward or backward. In addition, each normally-written block is followed by a 223-row pattern consisting of "0"s in the odd tracks only. Each block containing an error detected at recording time (e.g., incorrect parity) contains 725 additional rows of special patterns which indicate that the contents of the block shall be ignored when read. The additional overhead imposed on the reading and writing of each block by these lengthy special patterns makes the use of relatively long data blocks especially desirable in Uniservo IIIA operations.

A read-after-write row parity check permits detection of most recording errors at the time of occurrence. A "frame count" error is detected whenever the number of data rows in a block is not an integer multiple of five (or six when the optional format of six rows per word is used). Four special 9-bit registers in the control unit permit automatic compensation for skew of up to four rows (0.004 inch) in the tape being read. Excessive skew causes an error indication. Every tape recording and reading error initiates an external interrupt and causes a Status Word indicating the specific type of error to be transmitted to the Central Computer. In addition, recording errors cause the previously mentioned special patterns to be added to each incorrectly-written block.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . March, 1963.

§ 092.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan.
.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum columns.
Capacity: . . . . . approximately 5 feet.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . erase head followed by magnetic write head.
.222 Sensing system: . . . . magnetic read head.
.223 Common system: . . . yes; common read/write head.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 9.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read/write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 9.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape with magnetizable coating.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . row, at 1,000 rows per inch.
.322 Parallel by: . . . . . 9 tracks.
.324 Track use

	Standard Format	Optional Format
Data:	8 †	6.
Redundancy check: . .	1	1.
Timing:	0	0.
Control signals: . . .	0	0.
Unused:	0	2.
Total:	9	9.

† Two of the five rows used to represent each 36-bit computer word in the standard tape format contain only 6 data bits.

.325 Row use, per N-word block

	Standard Format	Optional Format
Data:	5 to 5N	6 to 6N.
Redundancy check: . .	0	0.
Timing:	0	0.
Control signals: . . .	283	283.
Inter-block gap: . . .	0.467 inch	0.467 inch.

.33 Coding: . . . . . binary image; 5 or 6 tape rows per 1107 word.

.34 Format Compatibility: . only with Uniservo IIIA units in UNIVAC III, 490, 1050, or other 1107 systems. UNIVAC III systems must be equipped with the Compatible Mode option.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.50 inch.
.352 Length: . . . . . 3,600 feet per reel, of which 3,500 feet are usable.

.4 CONTROLLER

.41 Identity: . . . . . Uniservo IIIA Control and Synchronizer.
Types 8003-08 and 8003-11.

.42 Connection to System

.421 On-line: . . . . . up to 15 Type 8003-08 Control and Synchronizer units; each fully occupies 1 input-output channel.
.422 Off-line: . . . . . none.

Note: Alternatively, the Type 8003-11 Control and Synchronizer can be used. This unit occupies 2 input-output channels and permits 2 read or 1 read and 1 write operations (but not 2 write operations) to occur simultaneously. Another alternative is the use of Control and Synchronizer models that permit either of two 1107 computers to communicate with the same group of tape units.

.43 Connection to Device

.431 Devices per controller: 2 to 16.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 65,535 words.
.442 Input-output area: . . . Core Memory.
.423 Input-output area access: . . . . . each word or field-defined portion of a word.
.444 Input-output area lockout: . . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES

.51 Blocks

.511 Size of block: . . . . . 1 to 65,535 data words, plus 283 rows of control information.
.512 Block demarcation
Input: . . . . . inter-block gap or word count in Access-Control Word.
Output: . . . . . word count in Access-Control Word.

§ 092.

.52 Input-Output Operations

.521	Input:	read 1 block of data forward or backward; or skip the block at the read head and read the next block forward. External interrupt upon completion is optional.
.522	Output:	write 1 block of data forward.
.523	Stepping:	none.
.524	Skipping:	none.
.525	Marking:	file separator, inter-block gap.
.526	Searching:	read first word (forward) or last recorded word (backward) of each block and compare it with all or an indicated portion of an Identifier Word. When a match occurs, read the block.

.53 Code Translation: . . . none; binary images of data in internal storage are recorded on tape (see Paragraph .324).

.54 Format Control: . . . . by program.

.55 Control Operations

Disable:	yes, following rewind with interlock.
Request interrupt:	yes.
Select format:	no.
Select code:	no.
Rewind:	yes.
Unload:	no; not required, because leader remains on handler.
Terminate current operation:	yes.

.56 Testable Conditions

Disabled:	yes.
Busy device:	no.
Output lock:	no.
Nearly exhausted:	no.
Busy controller:	yes.
End of medium marks:	yes.
Rewinding:	yes.
End of file:	yes.

.6 PERFORMANCE

.61 Conditions

I:	standard format; 5 tape rows per word.
II:	optional format; 6 tape rows per word.

.62 Speeds

.621	Nominal or peak speed:	100,000 rows/sec. for both conditions.
	Condition I:	20,000 words/sec. or 120,000 alphameric characters/sec.
	Condition II:	16,667 words/sec. or 100,000 alphameric characters/sec.
.622	Important parameters	
	Recording density:	1,000 rows/inch.
	Tape speed:	100 inches/sec.
	Rewind time:	maximum of 120 seconds for 3,600-foot reel.
	Inter-block gap:	0.467 inch.
	Start and stop time:	3 msec each (to within 7% of steady speed).
.623	Overhead:	7.5 msec per block.
.624	Effective speeds:	100,000N/(N + 750) rows/sec, where N is number of rows per block. (See Graph.)

.63 Demands on System

Component	Condition	msec per word	Percentage of data transfer time
Core Memory:	I	0.004	8.0
	II	0.004	6.7

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Forward:	button	sets tape for forward operation.
Backward:	button	sets tape for backward operation.
Rewind:	button	rewinds tape.
Change tape:	button	moves tape to load point.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel:	3,500 usable feet, or 26,400,000 6-bit alphameric characters at 1,000 characters per block.

.732 Replenishment time: . . 0.5 to 1.0 minute; tape unit needs to be stopped.

.734 Optimum reloading period: . . . . . 7 minutes.

§ 092.

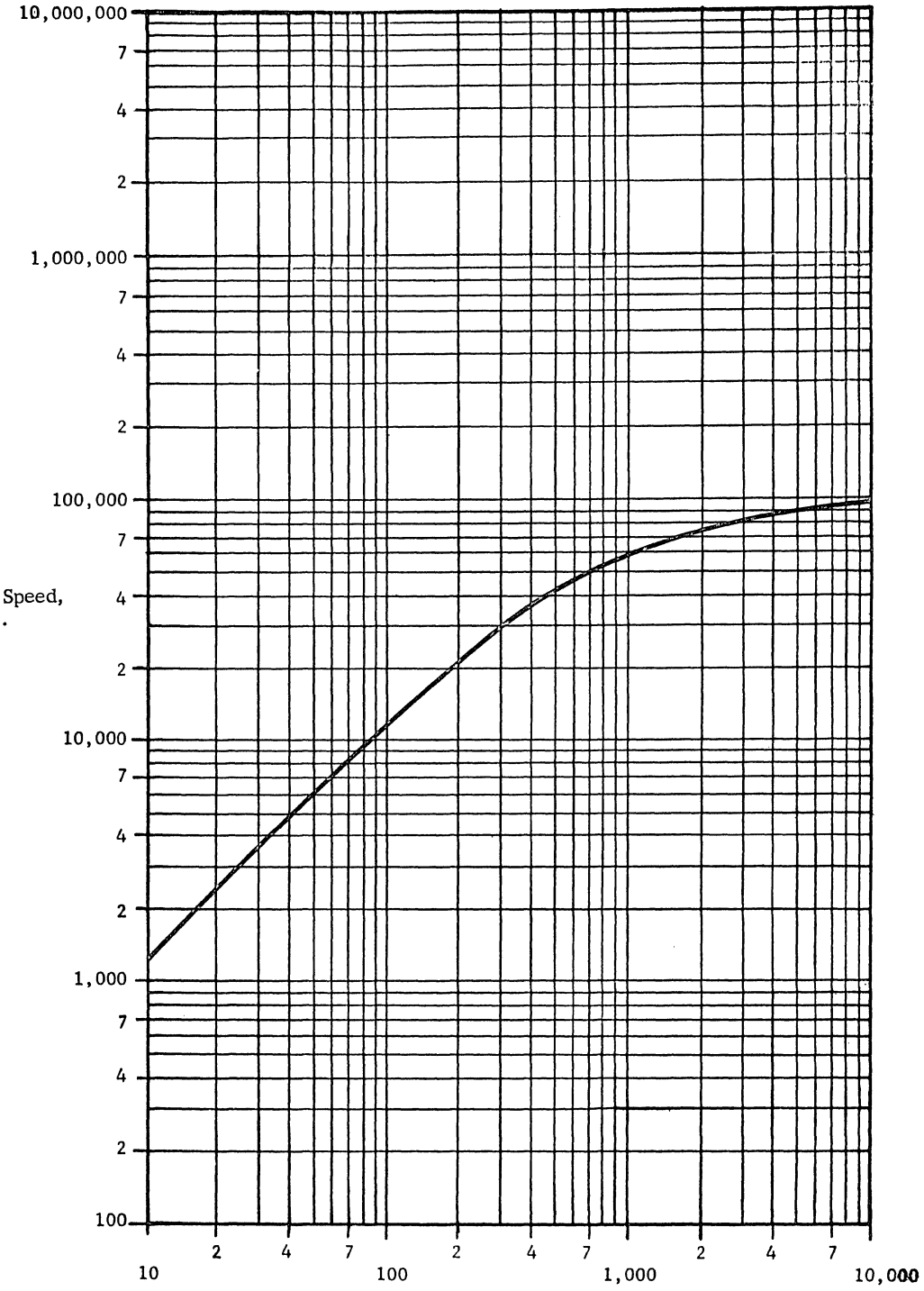
.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read-after-write row parity check	interrupt.
Reading:	row parity check	interrupt.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	check	interrupt.
Imperfect medium:	"bad spot" check	interrupt.
Timing conflicts:	synchronism check	interrupt.
Illegal function code:	check	interrupt.
Excessive skew:	check	interrupt.

Note: The type of error is indicated by bits 32 through 35 of the Status Word, sent to the Central Computer when an interrupt occurs.

§ 092.

EFFECTIVE SPEED
UNISERVO IIIA



Note: 5 or 6 tape rows per 6-character 1107 word, depending upon recording format used.

INPUT-OUTPUT: UNISERVO IIIC

§ 093.

.1 GENERAL

..11 Identity: . . . . . Uniservo IIIC Magnetic Tape Handler.
Type 7236.

.12 Description

The Uniservo IIIC provides UNIVAC 1107 systems with magnetic tape input-output in a format compatible with all tape units currently produced by IBM except the Model 7340 Hypertape Drive. From 2 to 12 Uniservo IIIC tape handlers can be connected to a Tape Adapter Cabinet, which is in turn connected to a Uniservo IIIC Control and Synchronizer Unit and a Power Supply to comprise a Compatible Tape Subsystem. Each subsystem occupies one 1107 input-output channel (there are 15 general purpose input-output channels available), and only one tape handler per subsystem can be reading or writing at any time. The logical address assigned to each tape handler can only be changed by means of a plugboard on the Tape Adapter Cabinet.

Tape speed is 112.5 inches per second. Recording density may be either 200 or 556 rows per inch, providing a peak data transfer rate of 22,500 or 62,500 characters per second. Each tape row consists of six data bits and one parity bit, and can represent one alphameric character or one-sixth of an 1107 word. As in IBM 700 and 7000 series scientific systems, reading and writing can be performed in either the binary mode (with odd parity) or the BCD mode (with even parity). Block length is variable from one word to the capacity of Core Memory. Tapes recorded at a density of 800 rows per inch by the new IBM 729V and 729VI Magnetic Tape Units cannot be read by a Uniservo IIIC tape unit.

A Uniservo IIIC operation can be initiated by any of 50 different function codes. Read and write function codes specify the recording mode (binary or BCD), the density (200 or 556 rows per inch), and whether or not an external interrupt shall occur upon normal completion of the tape operation. If a new read or write function code is received within 1.0 millisecond after the longitudinal check character of a block is read, tape movement will be continuous; otherwise, tape movement will stop after each block.

Unlike other Uniservo tape handlers, the IIIC can read and search only in the forward direction. The tape can, however, be backspaced one block or one file. In tape searching, the first word of each tape block is read and compared to an Identifier Word; when a match occurs, the entire block is read into Core Memory and the operation is terminated.

As in IBM tape units, two-gap magnetic heads are used to permit a read-after-write check on

.12 Description (Contd.)

recording. A longitudinal parity check character is written after the last data row in each block. Both longitudinal and lateral (row) parity are checked during each read and write operation. Abnormal conditions (such as parity errors, illegal function codes, and end-of-tape marks) cause external interrupts. A Status Word, sent to the Central Computer when an interrupt occurs, specifies the reason for the interrupt.

.13 Availability: . . . . . 9 to 12 months.

.14 First Delivery: . . . . March, 1963.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan and tape tension.

.212 Reservoirs
Number: . . . . . 2.
Form: . . . . . vacuum columns.
Capacity: . . . . . approx. 6 feet of tape.

.213 Feed drive: . . . . . electric motor.

.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.

.222 Sensing system: . . . . magnetic head.

.223 Common system: . . . 2-gap head provides read-after-write checking.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read.
Distance: . . . . . 0.25 inch after write head.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape with magnetizable surface.

.312 Phenomenon: . . . . . magnetization.

§ 093.

.32 Positional Arrangement

.321	Serial by:	row, at 200 or 556 per inch.
.322	Parallel by:	7 tracks.
.324	Track use	
	Data:	6.
	Redundancy check:	1 (parity).
	Timing:	0.
	Unused:	0.
	Total:	7.
.325	Row use, per N-word block	
	Data:	6 to 6N.
	Redundancy check:	1 (parity).
	Timing:	0.
	Control signals:	0.
	Unused:	0.
	Inter-block gap:	0.75 inch.
.33	Coding:	binary image, using 6 tape rows per 1107 word and odd parity; or BCD mode, using IBM 6-bit character codes and even parity.
.34	Format Compatibility:	with all IBM 700, 1400, and 7000 series systems via IBM 727, 729, and 7330 Magnetic Tape Units. Code translation will generally not be required.

.35 Physical Dimensions

.351	Overall width:	0.50 inch.
.352	Length:	2,400 feet per reel.

.4 CONTROLLER

.41	Identity:	Uniservo IIIC Control and Synchronizer. Type 7273. Uniservo IIIC Tape Adapter Cabinet. Type 7424.

.42 Connection to System

.421	On-line:	up to 15 Magnetic Tape Subsystems; each requires 1 Control and Synchronizer unit and 1 Tape Adapter Cabinet, and each fully occupies 1 input-output channel.
.422	Off-line:	none.

.43 Connection to Device

.431	Devices per controller:	2 to 12.
.432	Restrictions:	none.

.44 Data Transfer Control

.441	Size of load:	1 to 65,535 words.
.442	Input-output area:	Core Memory.
.443	Input-output area access:	each word or field-defined portion of a word.
.444	Input-output area lockout:	none.
.445	Table control:	none.
.446	Synchronization:	automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511	Size of block:	1 to 65,535 data words.
.512	Block demarcation	
	Input:	inter-block gap on tape, or word count in Access-Control Word.
	Output:	word count in Access-Control Word.

.52 Input-Output Operations

.521	Input:	read 1 block of data forward only at either 200 or 556 rows per inch and in either binary mode (odd parity) or BCD mode (even parity); external interrupt upon completion is optional.
.522	Output:	write 1 block of data forward at either 200 or 556 rows per inch and in either binary mode (odd parity) or BCD mode (even parity); external interrupt upon completion is optional.
.523	Stepping:	1 block backward (backspace). approximately 4 inches forward (to skip and erase defective tape areas).
.524	Skipping:	backspace to an end-of-file mark or to load point on tape.
.525	Marking:	end-of-file mark, inter-block gap.
.526	Searching:	read first word of each block and compare it with an Identifier Word. When a match occurs, read the block as in Paragraph .521.
.53	Code Translation:	none; binary images of data in internal storage are recorded on tape in either odd parity (binary mode) or even parity (BCD mode).
.54	Format Control:	by program.

.55 Control Operations

	Disable:	yes, following rewind with interlock.
	Request interrupt:	yes.
	Select format:	yes; binary or BCD.
	Rewind:	yes.
	Unload:	no.
	Terminate current operation:	yes.

§ 093.

.56 Testable Conditions

Disabled:	yes.
Busy device:	no.
Output lock:	yes.
Nearly exhausted:	no.
Busy controller:	yes.
End of medium marks:	yes; 14 feet from physical end.
End of file:	yes.
Rewinding:	yes.

.6 PERFORMANCE

.61 Conditions

I:	reading at 200 rows/inch.
II:	reading at 556 rows/inch.
III:	writing at 200 rows/inch.
IV:	writing at 556 rows/inch.

.62 Speeds

.621 Nominal or peak speed

I and III:	22,500 char/sec.
II and IV:	62,500 char/sec.

.622 Important parameters

Recording density:	200 or 556 rows/inch.
Tape speed:	112.5 inches/sec.
Full rewind time:	87 seconds.
Inter-block gap:	0.75 inch.
End-of-file gap:	3.7 inches.
Start time	
Read:	6.3 msec.
Write:	4.1 msec.
Stop time	
Read:	9.0 msec.
Write:	9.0 msec.

.623 Overhead †

Reading:	7.7 msec per block.
Writing:	7.7 msec per block.

.624 Effective speeds †

I:	22,500N/(N + 173) char/sec.
II:	62,500N/(N + 481) char/sec.
III:	22,500N/(N + 173) char/sec.
IV:	62,500N/(N + 481) char/sec. where N is number of characters (i.e., tape rows) per block.

† These figures are based upon continuous tape motion, since tape is not stopped between blocks in normal operation.

.63 Demands on System

Component	Condition	msec per word	Percentage of data transfer time
Core Memory:	I and III	0.004	1.50
	II and IV	0.004	4.17

.7 EXTERNAL FACILITIES

.71 Adjustments: none.

.72 Other Controls

Function	Form	Comment
Rewind and Unload:	switch/light	rewinds and positions tape.
Forward:	switch/light	sets tape to handle forward movement.
Backward:	switch/light	sets tape to handle backward movement.

.73 Loading and Unloading

.731 Volumes handled: 2,400 feet per reel; for 1,000-character blocks, 5,000,000 characters at 200 char/inch or 11,300,000 characters at 556 char/inch.

.732 Replenishment time: 0.5 to 1.0 minute; tape handler needs to be stopped.

.734 Optimum reloading period: 4 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read-after-write parity check	interrupt.
Reading:	lateral and longitudinal parity check	interrupt.
Input area overflow:	none.	
Out block size:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	check	interrupt.
Imperfect medium:	see Recording.	
Character count:	modulo 6 check	interrupt.
Illegal function code:	check	interrupt.
Illegal unit address:	check	interrupt.

Note: The type of error is indicated by bits 32 through 35 of the Status Word, sent to the Central Computer when an interrupt occurs.

SIMULTANEOUS OPERATIONS

§ 111.

.1 SPECIAL UNITS

.11 Identity: . . . . . Control and Synchronizer Units (one per peripheral subsystem; described in reports on the individual input-output units, Sections 784:071 through 784:093).

.12 Description

Sixteen input-output channels are provided for communication between the UNIVAC 1107 Central Computer and its peripheral devices. Each channel consists of an input cable and an output cable, but data flow is limited to only one direction at a time. Channel number 15 is normally reserved for the Control Console, leaving 15 input-output channels (numbered 0 through 14) available for general purpose use. Any one of the following peripheral subsystems can be connected to any one of the 15 general purpose channels via the appropriate Control and Synchronizer Unit:

- FH-880 Magnetic Drum Subsystem: 1 to 8 drums (see Section 784:043).
- Fastrand Mass Storage Subsystem: 1 to 8 storage units.
- Uniservo IIIA Magnetic Tape Subsystem: 2 to 16 tape units (see Section 784:092).
- Uniservo IIA Magnetic Tape Subsystem: 2 to 12 tape units (see Section 784:091).
- Uniservo IIIC Magnetic Tape Subsystem: 2 to 12 tape units (see Section 784:093).
- High-Speed Printer Subsystem: 1 printer (see Section 784:081).
- Punched Card Subsystem: 1 reader and 1 punch (see Sections 784:071 and 784:072).
- Paper Tape Subsystem: 1 reader and 1 punch (see Sections 784:075 and 784:076).

The Control and Synchronizer Units provide the proper interfaces between the Central Computer and the peripheral units on each channel. During output operations, the Synchronizer accepts 36-bit words from the computer and divides them into 6-bit character elements. During input operations, the Synchronizer assembles 6-bit characters from the input

.12 Description (Contd.)

device into 36-bit 1107 words. The peripheral Control Unit, which is usually in the same cabinet as the Synchronizer, directs the selected input or output device while it performs the desired function.

In general, one data transfer operation at a time can occur on each input-output channel that has a peripheral subsystem connected to it. The exceptions to this general statement are:

- The card reader and punch in a single Punched Card Subsystem can operate simultaneously by time-sharing their demands on the channel that serves them.
- An optional Dual Channel Synchronizer can be used with a Uniservo IIIA Magnetic Tape Subsystem. In this case, the subsystem occupies two input-output channels and can simultaneously control either 1 read and 1 write or 2 read operations (but not 2 write operations).
- A magnetic tape Control and Synchronizer Unit (and therefore the channel to which it is connected) is occupied throughout a tape search operation, even though no data is transferred to the Central Computer until the search has been successfully completed.

Input-output requests for access to Core Memory are automatically sequenced and controlled by a priority control network in the Central Computer. When two or more channels simultaneously attempt to communicate with Core Memory, requests to store input data are granted priority over requests to access data to produce output. Within each class, top priority is granted to the lowest-numbered channel. Therefore, the peripheral units with the higher data transfer rates are usually connected to the lower-numbered channels.

Core Memory cycle time is 4 microseconds, so the maximum potential gross data transfer rate for a UNIVAC 1107 system is 250,000 words (or 1,500,000 characters) per second. Because core storage accesses are also required for execution of the stored program and for input-output control functions, the actual gross data transfer rate will not, as a general rule, exceed 125,000 words per second. Based upon this overall restriction, the maximum number of peripheral devices that can transfer data simultaneously in any combination can be readily calculated from the following table of peak word transfer rates to and from Core Memory. (The card reader, card punch, and printer are buffered, so the tabulated word transfer rates apply to loading and unloading of their buffers and are higher than the overall transfer rates of the devices themselves.)

§ 111.

.12 Description (Contd.)

Device	Peak Transfer Rate, words/second
FH-880 Magnetic Drum	60,000
Fastrand Mass Storage Unit	25,000
Uniservo IIIA Tape Unit	20,000
Uniservo IIIC Tape Unit	10,417
Uniservo IIA Tape Unit	4,167
High-Speed Printer	4,167
Card Reader	1,400
Card Printer	1,400
Paper Tape Reader	67
Paper Tape Punch	19

The table shows, for example, that 1 FH-880 drum, 2 Uniservo IIIA tape units, 2 printers, 2 card readers, and 2 card punches could all transfer data to or from the Central Computer simultaneously; gross transfer rate in this case would be 113,934 words per second, or 91 per cent of the practical limiting rate of 125,000 words per second.

.4 RULES

Maximum of 15 peripheral subsystems, in any combination (except each Uniservo IIIA Subsystem with Dual Channel Synchronizer occupies 2 of the 15 input-output channels).

One input or output operation per Magnetic Drum Subsystem; and

One input, output, or search operation per Magnetic Tape Subsystem with Single Channel Synchronizer; and

One input and one output (or two input) operations per Uniservo IIIA Magnetic Tape Subsystem with Dual Channel Synchronizer; and

Any number of magnetic tape rewind operations; and

One input and one output operation per Punched Card Subsystem; and

One input or output operation per Paper Tape Subsystem; and

One output operation per Printer Subsystem; and

One Control Console input or output operation.

Gross data transfer rate between Core Memory and all simultaneously operating peripheral devices should not exceed 125,000 words per second.

§ 121.

INSTRUCTION LIST

Note: The following Instruction List was reproduced from the UNIVAC 1107 General Description, pages 32-35.

f	j	NAME	DESCRIPTION		EXECUTION TIME IN μ SEC. Alternate Core Banks	EXECUTION TIME IN μ SEC. Same Core Bank	MNEMONIC CODE
01	0-17	Store Positive	(A) → U		4.0	8.0	STP
02		Store Negative	− (A) → U		4.0	8.0	STN
03		Store Magnitude	|(A)| → U		4.0	8.0	STM
04		Store R_a	(R_a) → U		4.0	8.0	STR
05		Store Zero	0 → U (Clear U)		4.0	8.0	STZ
06		Store B_a	(B_a) → U		4.0	8.0	STB
10		Load Positive	(U) → A		4.0	8.0	LDP
11		Load Negative	− (U) → A		4.0	8.0	LDN
12		Load Positive Magnitude	|(U)| → A		4.0	8.0	LDM
13		Load Negative Magnitude	− |(U)| → A		4.0	8.0	LNM
14		Add	(A) + (U) → A		4.0	8.0	ADD
15		Subtract	(A) − (U) → A		4.0	8.0	SUB
16		Add Magnitude	(A) + |(U)| → A		4.0	8.0	ADM
17		Subtract Magnitude	(A) − |(U)| → A		4.0	8.0	SBM
20		Add and Load	(A) + (U) → A + 1		4.0	8.0	ADL
21		Subtract and Load	(A) − (U) → A + 1		4.0	8.0	SBL
22†		Block Transfer	$(V_1)_i \rightarrow (V_2)_i$ repeated k times. Initial V_1 address is u + $(B_b)_{17-0}$, and subsequent addresses are formed by incrementation by $(B_b)_{35-18}$. Similarly, V_2 addresses are u + $(B_a)_{17-0}$ incremented by $(B_a)_{35-18}$.		8.0	8.0	BTR
23		Load R_a	(U) → R_a		4.0	8.0	LDR
24		Add to B_a	(B_a) + (U) → B_a		4.0	8.0	ADB
25		Subtract from B_a	(B_a) − (U) → B_a		4.0	8.0	SBB
26		Load B_a Modifier Only	(U) → B_{a17-0}		4.0	8.0	LBM
27		Load B_a	(U) → B_a		4.0	8.0	LDB
30		Multiply Integer	(A) • (U) → A, A + 1		12.0	16.0	MPI
31		Multiply Single (Integer)	(A) • (U) → A		12.0	16.0	MPS
32		Multiply Fractional	(A) • (U) → A, A + 1		13.0	16.0	MPF
34		Divide Integer	(A, A + 1) ÷ (U); Quotient → A, Remainder → A + 1		31.3	35.3	DVI
35		Divide Single and Load (Fractional)	(A) ÷ (U); Quotient → A + 1, No Remainder		31.3	35.3	DVL
36		Divide Fractional	(A, A + 1) ÷ (U); Quotient → A, Remainder → A + 1		31.3	35.3	DVF
40		Selective Set	(A) → A + 1. Then set $(A + 1)_n$ for $(U)_n = 1$ i.e., (A) ⊕ (U) → A + 1		4.0	8.0	SSE
41		Selective Complement	(A) → A + 1. Then complement $(A + 1)_n$ for $(U)_n = 1$ i.e., (A) ⊕ (U) → A + 1		4.0	8.0	SCP
42		Selective Clear	(A) → A + 1. Then clear $(A + 1)_n$ for $(U)_n = 1$ i.e., (A) ⊙ (U) → A + 1		4.0	8.0	SCL
43		Selective Substitute	(A) → A + 1. Then $(U)_n \rightarrow (A + 1)_n$ for $(M)_n = 1$ i.e., (A) ⊙ (M)′ + (U) ⊙ (M) → A + 1		4.7	8.7	SSU
44		Selective Even Parity Test	If [(A) ⊙ (U)] is even parity, Skip NI	No Skip Skip	6.0 10.0	10.0 14.0	SEP
45		Selective Odd Parity Test	If [(A) ⊙ (U)] is odd parity, Skip NI	No Skip Skip	6.0 10.0	10.0 14.0	SOP
47		Test Modifier	If $(B_a)_{17-0} < (U)$, take NI; If $(B_a)_{17-0} > (U)$, Skip. In either case, $(B_a)_{17-0} + (B_a)_{35-18} \rightarrow B_{a17-0}$	No Skip Skip	4.7 8.7	8.7 12.7	TMO
50		Test Zero	Skip NI if (U) = 0	No Skip Skip	4.0 8.0	8.0 12.0	TZR
51		Test Not Zero	Skip NI if (U) ≠ 0	No Skip Skip	4.0 8.0	8.0 12.0	TNZ
52		Test Equal	Skip NI if (U) = (A)	No Skip Skip	4.0 8.0	8.0 12.0	TEQ
53		Test Not Equal	Skip NI if (U) ≠ (A)	No Skip Skip	4.0 8.0	8.0 12.0	TNE
54		Test Less Than or Equal	Skip NI if (U) ≤ (A)	No Skip Skip	4.0 8.0	8.0 12.0	TLE
55		Test Greater Than	Skip NI if (U) > (A)	No Skip Skip	4.0 8.0	8.0 12.0	TGR
56		Test Within Limits	Skip NI if (A) < (U) ≤ (A + 1) (Note: (A) < (A + 1))	No Skip Skip	4.7 8.7	8.7 12.7	TWL
57		Test Outside Limits	Skip NI if (U) ≤ (A) or (U) > (A + 1) (Note: (A) ≮ (A + 1))	No Skip Skip	4.7 8.7	8.7 12.7	TOL

†Repeat operations 62-67, 71 take 16 μ sec combined setup and termination time. The block transfer (22) takes 12 μ sec combined setup and termination time.

§ 121.

INSTRUCTION LIST (CONTD.)

f	j	NAME	DESCRIPTION		EXECUTION TIME IN μ SEC. Alternate Core Banks	EXECUTION TIME IN μ SEC. Same Core Bank	MNEMONIC CODE
60	0-17	Test Positive	Skip NI if (U) $\geq$ 0	No Skip	4.0	8.0	TPO
				Skip	8.0	12.0	
61		Test Negative	Skip NI if (U) < 0	No Skip	4.0	8.0	TNG
				Skip	8.0	12.0	
62†		Search Equal	Skip NI if $(U)_i = (A)$	No Skip	4.0	4.0	SEQ
			Repeated k times	Skip	4.0	4.0	
63†		Search Not Equal	Skip NI if $(U)_i \neq (A)$	No Skip	4.0	4.0	SNE
			Repeated k times	Skip	4.0	4.0	
64†		Search Less Than or Equal	Skip NI if $(U)_i \leq (A)$	No Skip	4.0	4.0	SLE
			Repeated k times	Skip	4.0	4.0	
65†		Search Greater Than	Skip NI if $(U)_i > (A)$	No Skip	4.0	4.0	SGR
				Skip	4.0	4.0	
66†		Search Within Limits	Skip NI if $(A) < (U)_i \leq (A + 1)$	No Skip	4.7	4.7	SWL
			(Note: $(A) < (A + 1)$)	Skip	4.7	4.7	
67†		Search Outside Limits	Skip NI if $(U)_i \leq (A)$ or $(U)_i > (A+1)$	No Skip	4.7	4.7	SOL
			(Note: $(A) < (A + 1)$)	Skip	4.7	4.7	
70		Index Jump	If $(CM)_{ja} > 0$, Jump to U	No Jump	8.0	8.0	IXJP
			$(CM)_{ja} \leq 0$, Take NI	Jump	4.0	4.0	
			Then $(CM)_{ja} - 1 \rightarrow CM_{ja}$				
			NOTE: j in this instruction serves with the a-designator to specify any one of the 128 words of Control Memory.				
71†	*						
	00	Masked Search Equal	Skip NI if $(U)_i \odot (M) = (A) \odot (M)$	No Skip	4.0	4.0	MSEQ
			Repeated k times	Skip	4.0	4.0	
	01	Masked Search Not Equal	Skip NI if $(U)_i \odot (M) \neq (A) \odot (M)$	No Skip	4.0	4.0	MSNE
			Repeated k times	Skip	4.0	4.0	
	02	Masked Search Less Than or Equal	Skip NI if $(U)_i \odot (M) \leq (A) \odot (M)$	No Skip	4.0	4.0	MSLE
			Repeated k times	Skip	4.0	4.0	
	03	Masked Search Greater Than	Skip NI if $(U)_i \odot (M) > (A) \odot (M)$	No Skip	4.0	4.0	MSGR
			Repeated k times	Skip	4.0	4.0	
	04	Masked Search Within Limits	Skip NI if $(A) \odot (M) < (U)_i \odot (M) \leq (A + 1) \odot (M)$	No Skip	4.7	4.7	MSWL
			(Note: $(A) \odot (M) < (A + 1) \odot (M)$)	Skip	4.7	4.7	
			Repeated k times				
	05	Masked Search Outside Limits	Skip NI if $(U)_i \odot (M) \leq (A)$ or $(U)_i \odot (M) > (A + 1)$	No Skip	4.7	4.7	MSOL
			(Note: $(A) \odot (M) < (A + 1) \odot (M)$)	Skip	4.7	4.7	
			Repeated k times				
72	*						
	00	Wait for Interrupt	The computer program sequence stops (i.e., P is not advanced). The wait condition is removed by an interrupt.		4.0		WAIT
	01	Return Jump	$(P) \rightarrow U_{17-0}$ and Jump to U + 1		8.0	8.0	RTJP
	02	Positive Bit Control Jump	If $(A)_{35} = 0$, Jump to U	No Jump	4.0	4.0	PBJP
			Shift (A) left one in either case	Jump	8.0	8.0	
	03	Negative Bit Control Jump	If $(A)_{35} = 1$, Jump to U	No Jump	4.0	4.0	NBJP
			Shift (A) left one in either case	Jump	8.0	8.0	
	04	Add Halves	$(A)_{17-0} + (U)_{17-0} \rightarrow A_{17-0}$		4.0	8.0	ADDH
			$(A)_{35-18} + (U)_{35-18} \rightarrow A_{35-18}$				
	05	Subtract Halves	$(A)_{17-0} - (U)_{17-0} \rightarrow A_{17-0}$		4.0	8.0	SUBH
			$(A)_{35-18} - (U)_{35-18} \rightarrow A_{35-18}$				
	06	Add Thirds	$(A)_{35-24} + (U)_{35-24} \rightarrow A_{35-24}$		4.0	8.0	ADDT
			$(A)_{23-12} + (U)_{23-12} \rightarrow A_{23-12}$				
			$(A)_{11-0} + (U)_{11-0} \rightarrow A_{11-0}$				
	07	Subtract Thirds	$(A)_{35-24} - (U)_{35-24} \rightarrow A_{35-24}$		4.0	8.0	SUBT
			$(A)_{23-12} - (U)_{23-12} \rightarrow A_{23-12}$				
			$(A)_{11-0} - (U)_{11-0} \rightarrow A_{11-0}$				
	10	Execute Remote Instruction	Execute the Instruction at U		4.0	— + Execution Time	EXRI
	11	Load Memory Lockout Register	$U_{5-0} \rightarrow$ MLR		4.0	—	LMLR
			For $U_0 = 1$ lockout 0—4095				
			$U_1 = 1$ lockout 4096—8191				
			$U_2 = 1$ lockout 8192—16383				
			$U_3 = 1$ lockout 16384—32767				
			$U_4 = 1$ lockout applies to 1st BANK				
			$U_5 = 1$ lockout applies to 2nd BANK				
73	*						
	00	Single Right Circular Shift‡	Shift (A) right U places circularly		4.0		SCSH
	01	Double Right Circular Shift	Shift (A, A + 1) right U places circularly		4.0		DCSH
	02	Single Right Logical Shift	Shift (A) right U places, end off; fill with zeros (Max. Shift = 36)		4.0		SLSH

*j serves as part of the Function Code

†Repeat operations 62-67, 71 take 16 μ sec combined setup and termination time. The block transfer (22) takes 12 μ sec combined setup and termination time.

‡Instruction execution time is independent of the number of shifts performed (e.g. a shift of 72 takes 4 microseconds). There are no memory references in the first six shift instructions, 73 00 — 73 05; consequently, the distinction between alternate core banks and the same core bank is irrelevant.

§ 121. INSTRUCTION LIST (CONTD.)

f	j	NAME	DESCRIPTION		EXECUTION TIME IN μ SEC. Alternate Core Banks	EXECUTION TIME IN μ SEC. Same Core Bank	MNEMONIC CODE
	03	Double Right Logical Shift	Shift (A, A + 1) right U places, end off; fill with zeros. (Max. Shift = 72)		4.0		DLSH
	04	Single Right Arithmetic Shift	Shift (A) right U places, end off; fill with sign bits.		4.0		SASH
	05	Double Right Arithmetic Shift	Shift (A, A + 1) right U places, end off; fill with sign bits. (Max. Shift = 72)		4.0		DASH
	06	Scale Factor Shift	(U) → A, shift A left circularly until $A_{35} \neq A_{34}$ or until A has been shifted 36 times. Store the scaled quantity in A and the number of shifts that occurred in A + 1.		6.0	10.0	SFSH
74	*						
	00	Zero Jump	Jump to U if (A) = 0	No Jump Jump	4.0 8.0	4.0 8.0	ZRJP
	01	Non-zero Jump	Jump to U if (A) ≠ 0	No Jump Jump	4.0 8.0	4.0 8.0	NZJP
	02	Positive Jump	Jump to U if (A) ≥ 0	No Jump Jump	4.0 8.0	4.0 8.0	POJP
	03	Negative Jump	Jump to U if (A) < 0	No Jump Jump	4.0 8.0	4.0 8.0	NGJP
	04	Console Selective Jump	Jump to U if A = key setting on console (1 of 15)		4.0	4.0	CSJP
	05	Selective Stop Jump	Stop if A = stop key setting on console (1 of 4), always jump to U		4.0	4.0	SSJP
	06	No Operation	Do Nothing; continue with NI		4.0	4.0	NOOP
	07	Enable All External Interrupts and Jump	Jump to U and permit interrupts to occur		4.0	4.0	EIJP
	10	Even Jump	Jump to U if $(A)_0 = 0$	No Jump Jump	4.0 8.0	4.0 8.0	EVJP
	11	Odd Jump	Jump to U if $(A)_0 = 1$	No Jump Jump	4.0 8.0	4.0 8.0	ODJP
	12	Modifier Jump	If $(B_a)_{17-0} > 0$, Jump to U If $(B_a)_{17-0} < 0$, Take NI In either case $(B_a)_{17-0} + (B_a)_{35-18} \rightarrow B_{a17-0}$	No Jump Jump	4.0 8.0	4.0 8.0	MOJP
	13	Load Modifier and Jump	(P) → $(B_a)_{17-0}$ and Jump to U		4.0	4.0	LMJP
	14	Overflow Jump	Jump to U if overflow cond. is set		4.0	4.0	OVJP
	15	No-Overflow Jump	Jump to U if overflow cond. is not set		4.0	4.0	NOJP
	16	Carry Jump	Jump to U if carry cond. is set		4.0	4.0	CYJP
	17	No-Carry Jump	Jump to U if carry cond. is not set		4.0	4.0	NCJP
75	*						
	00	Initiate Input Mode	(U) → input control word a, and initiate input mode on channel a.		4.0	8.0	IIPM
	01	Initiate Monitored Input Mode	(U) → input control word a, and initiate input mode on channel a with monitor.		4.0	8.0	IMIM
	02	Input Mode Jump	Jump to U if channel a is in the input mode.		4.0	4.0	IMJP
	03	Terminate Input Mode	Terminate input mode on channel a.		4.0	4.0	TIPM
	04	Initiate Output Mode	(U) → output control word a, and initiate output mode on channel a.		4.0	8.0	IOPM
	05	Initiate Monitored Output Mode	(U) → output control word a, and initiate output mode on channel a with monitor.		4.0	8.0	IMOM
	06	Output Mode Jump	Jump to U if channel a is in the output mode.		4.0	4.0	OMJP
	07	Terminate Output Mode	Terminate output mode on channel a.		4.0	4.0	TOPM
	10	Initiate Function Mode	(U) → output control word a, and initiate function mode on channel a.		4.0	8.0	IFNM
	11	Initiate Monitored Function Mode	(U) → output control word a, and initiate function mode on channel a with monitor.		4.0	8.0	IMFM
	12	Function Mode Jump	Jump to U if channel a is in the function mode.		4.0	4.0	FMJP
	13	Force External Transfer	Request external function or output word on channel a.		4.0	4.0	FEXT
	14	Enable All External Interrupts	All external interrupts are permitted to occur.		4.0	4.0	EAEI
	15	Disable All External Interrupts	All external interrupts are prevented from occurring.		4.0	4.0	DAEI
	16	Enable Single External Interrupt	An external interrupt on channel a is permitted to occur.		4.0	4.0	ESEI
	17	Disable Single External Interrupt	An external interrupt on channel a is prevented from occurring.		4.0	4.0	DSEI
76	*						
	00	Floating Add	(A) + (U) → A, A + 1		14.0	18.0	FLAD
	01	Floating Subtract	(A) − (U) → A, A + 1		14.0	18.0	FLSB
	02	Floating Multiply	(A) • (U) → A, A + 1		13.3	17.3	FLMP
	03	Floating Divide	(A) ÷ (U); Quotient → A Remainder → A + 1		26.7	30.7	FLDV
	04	Floating Point Unpack	Unpack (U), store mantissa in A + 1 and store the biased characteristic in A		4.0	8.0	FLUP
	05	Floating Point Normalize Pack	Normalize (A) pack with biased characteristic from (U) and store at A + 1		7.3	11.3	FLNP
	06	Floating Characteristic Difference Magnitude	Absolute value of $\lvert(A)_{34-27}\rvert - \lvert(U)_{34-27}\rvert \rightarrow A + 1$		4.0	8.0	FLCM
	07	Floating Characteristic Difference	$\lvert(A)_{34-27}\rvert - \lvert(U)_{34-27}\rvert \rightarrow A + 1$		4.0	8.0	FLCD

*j serves as part of the Function Code

§ 121. INSTRUCTION LIST (CONTD.)

GLOSSARY OF SYMBOLS AND TERMS

a	The a-designator (bits 25-22 of the instruction word). In arithmetic instructions, a designates one of the A-registers, in input-output instructions, a designates an input or output channel; in certain other instructions, a designates a B-register or an R-register.
R	Refers to a group of special registers.
M	Mask register (an R-register).
$(\ )'$	The prime on a quantity represents the one's complement of that quantity.
NI	Next Instruction.
P	Program address count in the P-register.
$\rightarrow$	Transfer the word (or words) shown at the left of the arrow to the address (or addresses) shown at the right of the arrow.
$(\ ) \odot (\ )$	The logical product, or logical AND, is defined by the table:

	0	1
0	0	0
1	0	1

$(\ ) \oplus (\ )$	The logical sum, also called the Inclusive OR:

	0	1
0	0	1
1	1	1

$(\ ) \overline{\oplus} (\ )$	The logical difference, controlled complement, add-without-carry, Exclusive OR:

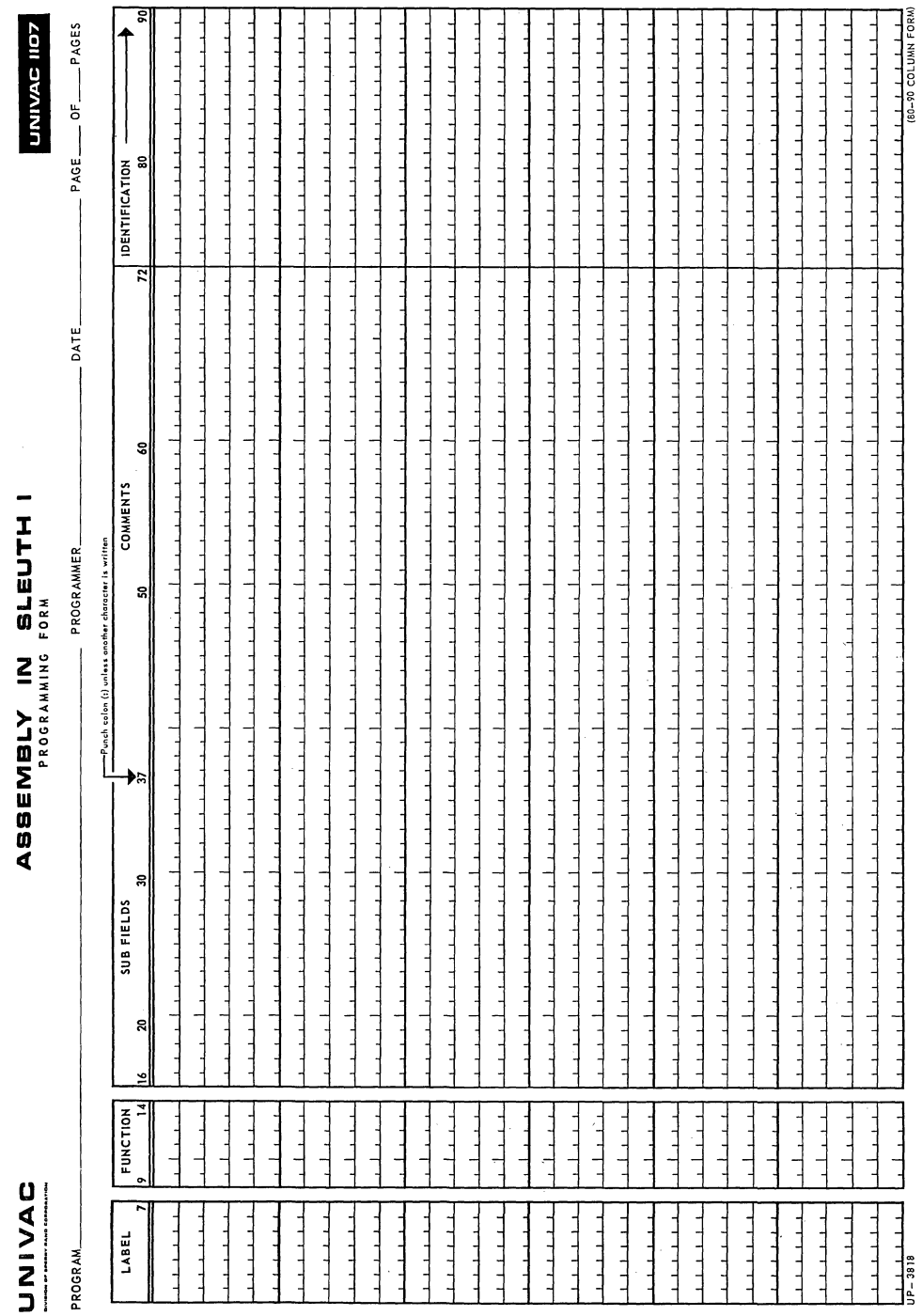
	0	1
0	0	1
1	1	0

$(\ )$	Indicates "the contents of" the address given within the parentheses.
u	The address, or base address, in the right-hand 16 bits of the instruction word.
U	The effective address of the operand to be used in the operation. It also serves as the shift count in shift instructions. $U = u + (B)_Q$ if no indirect addressing is indicated. If indirect addressing is indicated, $u + (B)_Q$ is the address at which U may be obtained.
A_n, $(U)_n$	The subscript n indicates the bit number under discussion.
$(\ )_{17\text{-}00}$	The subscript numbers represent the range of bit positions considered in the word whose address is given within the parentheses. For example: $(\ )_{\text{right half}} = (\ )_{17\text{-}00}$ $(\ )_{\text{left half}} = (\ )_{35\text{-}18}$ The bits are always numbered from right to left.
B_Q	Modifier portion of index register, $B_{17\text{-}00}$.
B_Δ	Increment portion of index register, $B_{35\text{-}18}$, used to increment the modifier B_Q.
b	b designator (bits 21-18) of the instruction word.

CODING SPECIMEN: SLEUTH I

§ 131.

.1 CODING SHEET



§ 131.

.2 SAMPLE PROBLEM

The sample problem given here will evaluate the expression

$$f(x) = x^3 + ax^2 + b\left(\frac{x^2+b}{x-5}\right) - c$$

The values of x range from 0 to 999 in steps of 1. 200 sets of random values for a, b, and c are assumed to be stored in a drum table, each set consisting of three words containing the values for a, b, and c, making the total length of the drum table equal to 600. The arrangement of the drum table is:

a_1	stored in	ABC
b_1	stored in	ABC + 1
c_1	" "	ABC + 2
a_2	" "	ABC + 3
b_2	" "	ABC + 4
c_2	" "	ABC + 5
a_3	" "	ABC + 6

etc.

The expression within parentheses $\left(\frac{x^2+b}{x-5}\right)$ will be handled as a macro instruction.

1 TAG 7	8	9 FUNCTION 14	15	SUB FIELDS 37	COMMENTS	NOTES
EFFEX		PRO		EXE	: POLYNOMIAL EVALUATION	1
XREG		EQU		$B2	:	2
		SPACE		1	:	3
				I/O DEFINITIONS		4
DRUM1		MDCH			:	5
ABC		MDT		,LGTH=600	:	6
OUTPUT		MTCH			:	7
TAPE1		MTA			:	8
		SPACE		1	:	
				DATA TABLE DEFINITIONS		
TABC		DTABLE		,LABC=3	:	9
TOUT		DTABLE		,LOUT=1000	:	10
		SPACE		1	:	
MACA		MACRO			:	11
		LDP		$A11,(1)	:	
		SUB		$A11,5,,$UOP	:	
		LDP		$A12,(1)	:	
		MPS		$A12,(1)	:	
		ADD		$A12,(2)	:	
		DVI		$A12,$A11	:	
		ENDMAC			:	
		EJECT			:	
		IBANK			:	12
START		LDB		$B5,199,,$UOP	:	13
		LDP		$Q0,REQ1	:	14
		LMJP		$B1,$X10	:	14
		LDB		$B4,999,,$UOP	:	15
		LDB		XREG,INDXWD	:	16
		STB		XREG,XLOC,,$H2	:	
		SPACE		1	:	

§ 131.

.2 SAMPLE PROBLEM (Contd.)

1 TAG 7	8	9 FUNCTION 14	15	SUB FIELDS	37	COMMENTS	NOTES
EVAL		LDP		$A5,XLOC	:		17
		MPS		$A5,$A5	:		
		"		$A5,XLOC	:		
		LDP		$A6,XLOC	:		
		MPS		$A6,$A6	:		
		"		$A6,ABC	:		
		MACA		(XLOC)(ABC+1)	:		18
		MPS		$A12,ABC+1	:		
		ADD		$A5,$A6	:		
		ADD		$A5,$A12	:		
		SUB		$A5,ABC+2	:		
		STP		$A5,TOUT,XREG*	:		19
		IXJP		$B4,EVAL-2	:		20
		LDP		$A7,PKT1+1	:		
		ADD		$A7,3,,$UOP	:		21
		STP		$A7,PKT1+1	:		21
WRITE		LDP		$QØ,REQ2	:		14
		LMJP		$B1,$XIO	:		14
		IXJP		$B5,START+1	:		
		LMJP		$B1,$END	:		22
		SPACE		1	:		
		DBANK			:		23
XLOC		W		Ø	:		
PKT1		W		Ø	:		24
		RD		ABC	:		
		I		LABC,TABC	:		
		W		Ø	:		
REQ1		H		Ø,PKT1	:		25
INDXWD		H		1,Ø	:		26
REQ2		H		Ø,PKT2	:		27

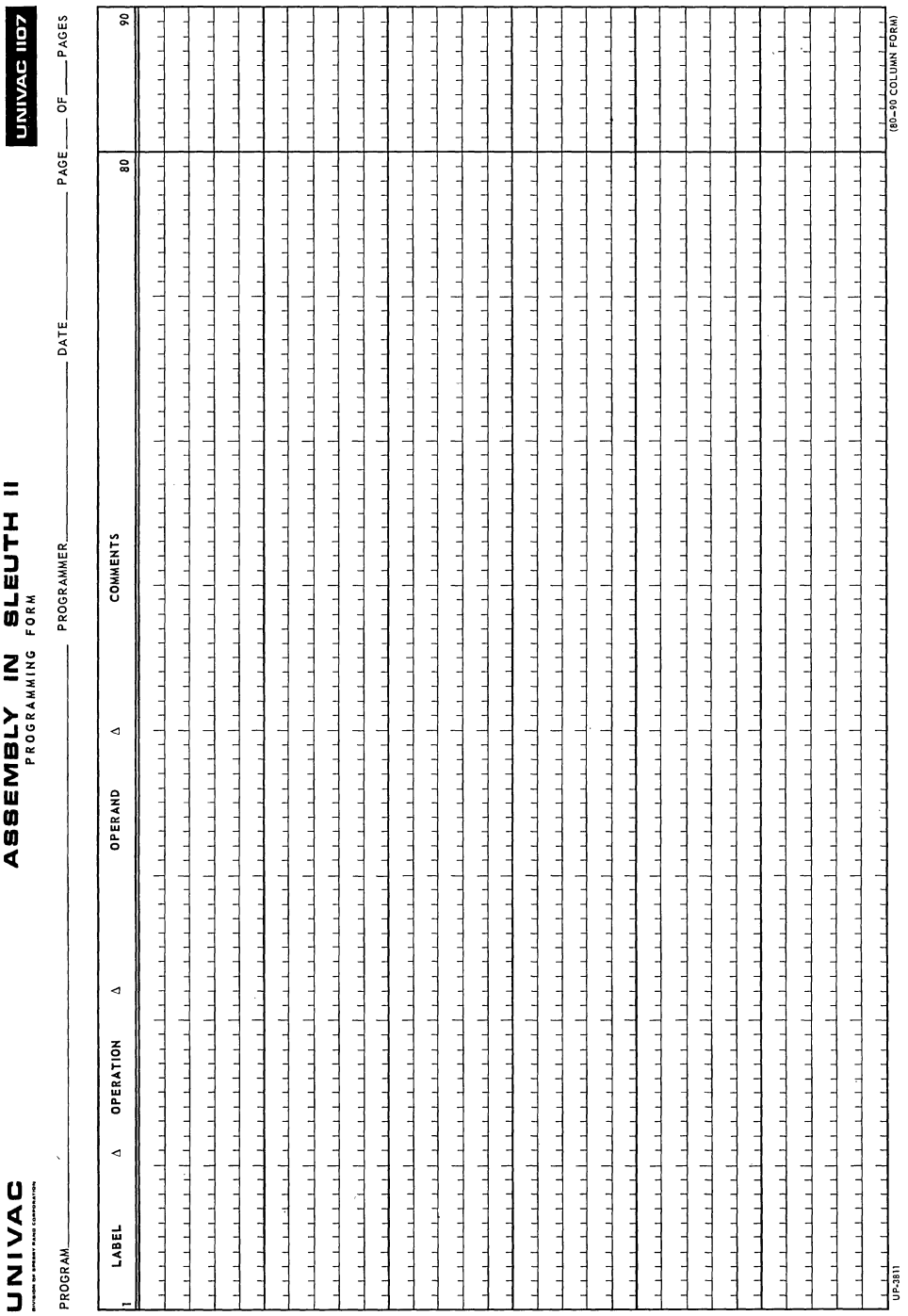
1 TAG 7	8	9 FUNCTION 14	15	SUB FIELDS	37	COMMENTS	NOTES
PKT2		W		Ø	:		28
		WT25		TAPE1	:		
		I		LOUT,TOUT	:		
		W		Ø	:		
		ENDPRO		START	:		29
					:		
					:		
					:		
					:		
					:		
					:		

Reprinted from SLEUTH I Programmer's Reference, pages 63-69.

CODING SPECIMEN: SLEUTH II

§ 132.

.1 CODING SHEET



§ 132.

.2 SAMPLE PROBLEM

The actual listing from a SLEUTH II assembly on the UNIVAC 1107 is reproduced below. It includes examples of procedure structure, nested procedures, and procedure references. The coding produced by reference to M PROC will determine the largest or smallest value in a series of values. Each value is assumed to be represented in a 36-bit signed word. On the next page is an explanation of the action taken by the assembler while processing this coding.

```
000001          000000                              RES  01000-s
000002                                         M     PROC
000003                                         MAX*  NAME 0
000004                                         MIN*  NAME 1
000005                                         M1*   PROC 0
000006                                               DO   M(0,0)=0 , TLE  M(1,1),M(I+2,1),M(I+2,2)
000007                                               DO   M(0,0)=1 , TG   M(1,1),M(I+2,1),M(I+2,2)
000008                                               LA   M(1,1),M(I+2,1),M(I+2,2)
000009                                               END
000010                                               LA   M(1,1),M(2,1),M(2,2)
000011                                         I     DO   M-3 , M1
000012                                               END
000013                  000000010000           L     EQU  010000
000014          001000  10 00 04 01 0 010000         MAX  16   L,1 L+2,1  (12)
                001001  54 00 04 01 0 010002
                001002  10 00 04 01 0 010002
                001003  54 00 04 00 0 001012
                001004  10 00 04 00 0 001012
000015          001005  10 00 04 01 0 010000         MIN  16   L,1 L+2,1  (12)
                001006  55 00 04 01 0 010002
                001007  10 00 04 01 0 010002
                001010  55 00 04 00 0 001012
                001011  10 00 04 00 0 001012
000016                  000000000000               END
                001012  000000000014
```

§ 132.

.2 SAMPLE PROBLEM (Contd.)

Line 1 sets the controlling location counter to octal 1000.

Lines 2 through 12, the body of the procedures, are temporarily stored by the assembler for later reference.

Line 13 equates L to an octal value of 10,000.

Line 14 is a reference line to PROC M, introduced above. It contains four lists. List 1 has one parameter; lists 2 and 3 each have two parameters; list 4 has one parameter, the literal 12. Coding produced by the reference to the procedure is shown to the left of the reference (addresses 001000-001004).

Line 2, the first line of M PROC, is referred to through MAX NAME 0, line 3.

Line 10, the first line of M PROC to produce coding, causes the creation of the first instruction, at address 001000. The operand entries of this instruction are determined by parameters supplied by the reference on line 14.

Line 11 references the nested procedure M1; the number of references to M1 PROC is determined by the expression M-3.

Line 5, the first line of M1 PROC, has a zero in the operand field indicating that no list is to be submitted to M1 when it is referenced.

Line 6 produces a TLE instruction (54) at address 001001, since MAX was the entry to PROC M. The counter I of the DO line (Line 11) within M PROC is used to advance the list number and thus access the appropriate parameter for use in the compare instructions.

Line 7 is skipped on this iteration, since the condition M(0,0) = 1 was not met.

Line 8 produces a LA (10) instruction at address 001002, in the same manner as line 10.

Line 9 terminates this iteration of M1 PROC.

Line 11 now references M1 PROC for the second iteration. Lines 5 through 9 will be executed as above.

Line 12 terminates M PROC. Assembly continues at.....

Line 15 is another reference to M PROC. The execution is identical except that line 6 is skipped and line 7 is executed.

Line 16 terminates the assembly, or program.

Reprinted from SLEUTH II Programmer's Guide, section III, pages 9-11.

DATA CODE TABLE NO. 1

§ 141.

.1 USE OF CODE: . . . . Fieldata Code; used for internal representation of alphameric data, High-Speed Printer, and Console Keyboard and Page Printer.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . . 2 zone bits; 32, 16.

.222 Less significant pattern: . . . . . 4 numeric bits; 8, 4, 2, 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	Master space †	K	)	0
1	Upper case †	L	–	1
2	Lower case †	M	+	2
3	Line feed †	N	<	3
4	Car. return †	O	=	4
5	Space	P	>	5
6	A	Q	&	6
7	B	R	$	7
8	C	S	*	8
9	D	T	(	9
10	E	U	" †	'
11	F	V	:	; ‡
12	G	W	? †	/
13	H	X	! †	.
14	I	Y	,	spec. †
15	J	Z	spec. †	stop ‡

† Produces "space" on High-Speed Printer.
‡ Causes cut-off when filling High-Speed Printer buffer.

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE . . . . punched cards (alphameric mode).

.2 STRUCTURE OF CODE

.21 Character Size: . . . 1 column of an 80-column card.

.23 Character Codes

UNDERPUNCH	OVERPUNCH			
	None	12	11	0
None	Space	&	–	
12				
11				
0	0	line feed †	car. return†	
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
8-2	>	+	:	'
8-3	=	.	$	,
8-4	<	)	*	(
8-5				! †
8-6	idle †	Upper case †	Lower case †	⊕ †
8-7	; †	Lower case †	? †	□ †
8-9	Master space†			

† Non-standard card codes.

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . . internal collating sequence, using Fieldata code.

.2 STRUCTURE OF CODE

In ascending sequence:

master space	)
upper case	-
lower case	+
line feed	<
carriage return	=
space	>
A	&
B	$
C	*
D	(
E	"
F	:
G	?
H	!
I	,
J	spec.
K	0
L	1
M	2
N	3
O	4
P	5
Q	6
R	7
S	8
T	9
U	'
V	;
W	/
X	.
Y	spec.
Z	stop or ‡

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . UNIVAC 1103A, 1103AS, and 1105 (no details available to date).

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

SORT/MERGE

Reference: . . . . . UNIVAC Technical Bulletin UT-2576, published May, 1962.
Record size: . . . . . limited only by available storage; variable length records can be sorted.
Block size: . . . . . variable by full words, and limited by available storage.
Key size: . . . . . maximum of 27 words plus 27 bits per key; limit of 7 such keys.
File size: . . . . . 1 reel per sort cycle; no overall limit.
Number of tape units: . 4 to 12 (up to 8 FH-880 Magnetic Drums can be used for intermediate storage when available).
Date available: . . . . . December, 1962.
Description:

SORT/MERGE is a generalized program for sorting or merging tape files into ascending or descending order. It is stored on a library tape in relocatable form and executed under control of EXEC I. Control parameters are supplied on up to nine punched cards. Twenty-five parameters are required, and others are optional. "Own coding" consisting of user-coded subroutines can be inserted to control editing prior to sorting (on the dispersion pass) or the final merge pass.

From 4 to 12 magnetic tape units can be utilized. When only four tape units are available, the unit containing the program tape must be used for intermediate storage; therefore, for efficient sorting, at least five tape units should be assigned. Up to eight FH-880 Magnetic Drums can be utilized, if available, to form long initial strings which minimize the required number of merge passes.

The Cascade Method is used to merge the strings produced by the internal sort phase into a single sequenced output file. When the input file consists of more than one tape reel, a separate "cycle," consisting of an internal sort phase followed by a cascade merge phase, must be performed upon each reel. Then the individually sorted reels are merged to form the final output. Tape dumps are automatically produced at the end of each cycle to establish restart points.

.13 Data Sorting and Merging (Contd.)

Description (Contd)

SORT II

This is a generalized routine that will operate under control of EXEC II and provide sort/merge capabilities for the SLEUTH II software package, which is being developed by Computer Sciences Corporation. No specifications for SORT II have been made available to date.

.14 Report Writing: . . . . none.

.15 Data Transcription

LION (Library of Input-Output Numerical Subroutines)

Reference: . . . . . UNIVAC Technical Bulletin UP-2581, published June, 1962.
Date available: . . . . November, 1962.
Description:

LION is a set of subroutines, called by SLEUTH I macro instructions, that perform the following functions under the control of EXEC I:

- Data transcriptions (cards to tape or drum, tape or drum to cards, and tape or drum to printer).
- Control of input-output operations on magnetic tape, drum, cards, or printer.
- Opening and closing of files and reels, including creation and checking of labels.
- Editing and format control of input-output data (including radix and mode conversions).

Note: EXEC II contains subroutines that perform most of the above functions when the SLEUTH II software package is used; see Section 784:192.

.16 File Maintenance

LIBRARIAN

Reference: . . . . . UNIVAC Technical Bulletin UP-2579, published May, 1962.
Date available: . . . . . November, 1962.
Description:

LIBRARIAN is a program library maintenance routine that operates under control of EXEC I. Using

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.16 File Maintenance (Contd.)

Description (Contd.)

input parameters on punched cards, it can create library tapes or add, delete, correct, resequence, and catalog programs on existing library tapes. The retrieval section of LIBRARIAN can be called in by the SLEUTH I Assembly System for incorporation of subroutines at assembly time.

Note: EXEC II contains built-in facilities that perform the above maintenance functions upon the library (called the "Program Complex File") when the SLEUTH II software package is used; see Section 784:192.

.17 Other

CLAMP (Controlled Loading And Modification of Programs)

Reference: . . . . . UNIVAC Technical Bulletin UP-2575, published May, 1962.
Date available: . . . . . October, 1962.
Description:

CLAMP is a loader designed to load either absolute or relocatable object programs produced by the SLEUTH I Assembly System. CLAMP can operate either under the control of EXEC I or as an independent loading routine controlled by parameters inserted through punched cards.

MIDAS (Macro Instructions for Dumping Areas of Store)

Reference: . . . . . UNIVAC General Manual UP-3846, published February, 1963.
Date available: . . . . . May, 1963.

.17 Other (Contd.)

MIDAS (Contd.)

Description:

MIDAS is a set of subroutines, called by SLEUTH I macro instructions, that provide tape dumps or printed listings of specified areas of Core or Film Memory. The MIDAS subroutines can either be incorporated into the object program at assembly time or loaded spearately at execution time under the control of EXEC I. A valuable option makes it possible to list only the initial and final contents of those locations whose contents have been altered during execution of the program being tested, thereby focusing the programmer's attention upon the potential trouble spots. Any one of five formats can be selected for the printed listing: octal, fixed or floating point decimal, alphameric (6-bit Fieldata codes), or instruction format with mnemonic operation codes.

COORDINATOR

Reference: . . . . . none published to date.
Date available: . . . . . 3rd quarter 1963.
Description:

COORDINATOR is a service routine that will partially resolve the incompatibilities between the SLEUTH I and SLEUTH II software packages by permitting object programs produced by the SLEUTH II, COBOL, and FORTRAN translators to be executed under the control of EXEC I. The three translators themselves will still operate only under the control of EXEC II. The manufacturer states that EXEC I will be expanded at a later date to control COBOL and FORTRAN compilations as well as execution of their object program.

PROCESS ORIENTED LANGUAGE: COBOL-61

§ 161.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1107 COBOL.

.12 Origin: . . . . . Computer Sciences Corporation.

.13 Reference: . . . . . UNIVAC 1107 COBOL Programmer's Guide, Publication U-2582.

.14 Description

UNIVAC 1107 COBOL is a version of COBOL-61, the most widely implemented pseudo-English common language for business applications. It represents a nearly complete implementation of Required COBOL-61 (though there are a few omissions), along with 14 COBOL electives and several useful extensions. The deficiencies of 1107 COBOL with respect to Required COBOL-61, the extensions, and the facilities of Elective COBOL-61 that have and have not been implemented are tabulated at the end of this description.

Useful extensions to the COBOL-61 language include a SORT facility, a MONITOR verb that facilitates program testing, the ability to sequence files in either ascending or descending order, and a facility that permits flexible control of the vertical format of printed output. See Paragraph .143 for more details on these extensions.

The most significant omission from the list of electives implemented for the 1107 is the COMPUTE verb. COMPUTE permits arithmetic operations to be expressed in a concise formula notation similar to that of FORTRAN, e.g.:

```
COMPUTE X = (A-B)/C
```

Without the COMPUTE verb, only one arithmetic operation can be performed in each COBOL statement, so the above formula must be expressed as:

```
SUBTRACT B FROM A GIVING T
DIVIDE C INTO T GIVING X.
```

The decision not to implement this highly useful verb is especially hard to understand in the case of a system with the speed and power of the 1107 instruction repertoire.

File and Record Descriptions and Procedure Division entries can be copied into the user's programs from the 1107 COBOL Library, but Environment Division entries cannot. Furthermore, the non-standard COPY verb of 1107 COBOL allows only single-paragraph procedures to be inserted without alteration, whereas the more flexible INCLUDE verb of Elective COBOL-61 (not implemented for the 1107) allows

.14 Description

library procedures consisting of sections, independent paragraphs, or paragraphs within sections to be inserted, with replacement of any number of names in the procedure by other names specified by the programmer.

The elective verb ENTER, as implemented for the 1107, makes it possible to enter either an independently compiled COBOL-coded subprogram or a closed subroutine in relocatable machine language form. Object programs can be segmented; but whereas Elective COBOL-61 specifies four different ways of handling segments according to their priorities, 1107 COBOL provides only two ways:

- Sections with assigned priorities of 1 through 49 will be present in Core Memory at all times.
- Sections with assigned priorities of 50 through 99 will be grouped into segments by priority number. One segment at a time will be loaded (in the order referenced) into a single Core Memory area whose size is equal to that of the largest segment.

Data items upon which arithmetic is to be performed can be represented internally in either decimal (6 bits per digit) or binary form by specifying USAGE IS COMPUTATIONAL or COMPUTATIONAL-1, Respectively. Operands can be up to 18 decimal digits or 66 binary bits in length, but SIZE must be specified in equivalent 6-bit CHARACTERS in either case. When operands are longer than 36 bits, multiple precision arithmetic must be performed. Arithmetic can be performed upon mixed COMPUTATIONAL and COMPUTATIONAL-1 items; radix conversion and point alignment will be automatically performed when necessary. None of the COBOL electives that provide for variable length items and records (e.g., the BLOCK, SIZE, and PICTURE clause options) have been implemented.

The 1107 COBOL Compiler will operate under control of the EXEC II operating system. Minimum configuration requirements are 16,384 words of core storage and 1 Flying Head 880 Magnetic Drum; magnetic tape is not required for the compilation process. Compilation is divided into six logical phases. Documentation will consist of a source program listing, diagnostic messages, and an object program listing containing symbolic instructions, octal locations, and octal machine words, with interspersed references to the source program listing. Four different types of error diagnostics are included within the translator, and they are interpreted as follows:

- Precautionary diagnostic - print warning message and continue compilation.
- Correctible error - make a reasonable attempt at correction, print explanatory message, and continue.

§ 161.

.14 Description (Contd.)

- Uncorrectible error - when a reasonable guess of the programmer's intent cannot be made, print message, reject the statement or clause, and continue.

- Destructive errors - when errors have multiplied to the point where it is probable that no more useful diagnostic information can be produced, terminate the compilation.

The main limitation on source program size is the number of cards in the source deck: a maximum of 2,000 cards in 16K systems and 4,000 cards in 32K systems. There are no specific limitations on the number of data names, procedure names, or other source program entities. When the COBOL segmentation facility is used, there are no practical limits on object program size. No information on compilation speed is yet available, but utilization of the magnetic drum instead of tape should provide relatively rapid compilation.

.141 Availability

Language: . . . . . October, 1962.
Translator: . . . . . no release date has been designated.

.142 Deficiencies with respect to Required COBOL-61

Environment Division
- SOURCE-COMPUTER, OBJECT-COMPUTER, and SPECIAL-NAMES paragraphs cannot be copied from the Library.

Data Division
- The [integer-4 TO] option of the RECORD CONTAINS clause is not permitted; there is no provision for efficient handling of variable length records; i.e., the compiler will consider all records to be the size of the largest record.

.142. Deficiencies with respect to Required COBOL-61 (Contd.)

Data Division (Contd.)

- The VALUE clause of the File Description entry can apply only to "IDENTIFICATION" or "ID," a specific item that appears in the standard label record.

Procedure Division
- The option of the PERFORM verb that permits loop control based upon a varying subscript-name has not been implemented.

.143 Extensions to COBOL-61

- A SORT facility is provided. It consists of subroutines that arrange related records in either ascending or descending sequence. Input and output procedures must be supplied by the COBOL programmer. While the functions of the 1107 SORT facility are similar to those of the SORT verb as defined in COBOL-61 Extended, the format of the required source coding is entirely different.

- A MONITOR verb provides dynamic printouts of the values of specific items as an aid to program testing and debugging.

- The operational symbol H can be used in a PICTURE clause to specify that the field is to be represented in one's complement binary form; the effect is the same as that of the clause USAGE IS COMPUTATIONAL-1.

.143 Extensions to COBOL-61 (Contd.)

- The optional clauses LINES-PER-PAGE, LINES-AT-TOP, LINES-AT-BOTTOM, and LINE-SPACING in the File Description entry provide vertical format control of printed output.

- Files can be sequenced in either ASCENDING or DESCENDING order.

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.144 COBOL-61 Electives Implemented (see 4:161.3)

Key No.	Elective	Comment
	Characters and Words	
1	Formula characters	+, -, *, /, **, =.
2	Relationship characters	=, >, <.
3	Semicolon	;, always ignored.
4	Long literals	up to 132 characters.
	File Description	
11	SEQUENCED ON	allows a list of keys to be specified, for ASCENDING or DESCENDING sequencing.
	Verbs	
24	ENTER	permits entry to independently compiled COBOL subprograms.
	Verb Options	
27	LOCK	locks rewound tapes.
30	ADVANCING	permits paper advance of the specified number of lines.
33	Operand size	up to 18 digits.
	Environment Division	
41	OBJECT-COMPUTER	includes all clauses except SEGMENT-LIMIT and ASSIGN OBJECT-PROGRAM.
46	I/O CONTROL	only the APPLY and RERUN clauses may be written.
	Identification Division	
47	DATE-COMPILED	current date will be inserted automatically.
	Special Features	
48	Library	procedures in source language can be called from the Library (but implemention is non-standard).
49	Segmentation	object programs can be segmented (but implementation is non-standard).

§ 161.

.145 COBOL-61 Electives NOT Implemented (see 4:161.3)

Key No.	Elective	Comment
	Characters and Words	
5	Figurative constants	HIGH-BOUND(S); LOW-BOUND(S).
6	Figurative constants	HIGH-VALUE(S); LOW-VALUE(S).
7	Computer-name	no alternative computer-names.
	File Description	
8	BLOCK CONTAINS	no range can be specified.
9	FILE CONTAINS	approximate file size cannot be shown.
10	Label formats	labels must be standard or omitted.
12	HASHED	hash totals cannot be created.
	Record Description	
13	Table-length	lengths of tables and arrays may not vary.
14	Item-length	variable item lengths cannot be specified.
15	BITS option	items cannot be specified in binary.
16	RANGE IS	value range of items cannot be shown.
17	RENAMES	alternative groupings of elementary items cannot be specified.
18	SIGN IS	no separate signs allowed.
19	SIZE clause option	variable item lengths cannot be specified.
20	Conditional range	a conditional value cannot be specified as a range.
21	Label handling	only standard labels (or none) may be used.
	Verbs	
22	COMPUTE	algebraic formulas may not be used.
23	DEFINE	new verbs cannot be defined.
25	INCLUDE	library subroutines cannot be called in the standard COBOL manner.
26	USE	no non-standard I/O error or label handling routines.
	Verb Options	
28	MOVE CORRESPONDING	each item in a record must be individually moved.
29	OPEN REVERSED	tapes cannot be read backward.
32	Formulas	algebraic formulas may not be used.
34	Relationship	IS UNEQUAL TO, EQUALS, and EXCEEDS are not provided.
35	Tests	IF { } IS NOT ZERO form is not provided.
36	Conditionals	no implied objects with implied subjects.
37	Compound conditionals	ANDs and ORs cannot be intermixed.
38	Complex conditionals	not permitted.
39	Conditional statements	only ON SIZE ERROR or AT END conditions may follow an imperative statement.
	Environment Division	
40	SOURCE-COMPUTER	only computer-name can be specified.
42	SPECIAL-NAMES	ACCEPT, WRITE, and DISPLAY verbs use standard hardware.
43	FILE-CONTROL	cannot be taken from library.
44	PRIORITY IS	no file priorities can be assigned for multiprogramming.
45	I/O CONTROL	cannot be taken from library.

PROCESS ORIENTED LANGUAGE: FORTRAN IV

§ 162.

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1107 FORTRAN.

.12 Origin: . . . . . Computer Sciences Corporation.

.13 Reference: . . . . . UNIVAC Publications U-3540 and U-3569.

.14 Description

No formal standard for the FORTRAN IV language exists. This report uses as a basis for comparison the language specifications for IBM 7090/7094 FORTRAN IV as contained in IBM Publication C28-6274.

The UNIVAC 1107 FORTRAN language is largely compatible with, and somewhat more powerful than, the FORTRAN IV language as implemented for the IBM 7090/7094. The restrictions and extensions of 1107 FORTRAN relative to the 7090/7094 version are listed at the end of this description. It can be seen that the restrictions will cause few problems, whereas the extensions significantly increase the power and flexibility of the FORTRAN IV language, particularly in the areas of subscripting and mixed-mode arithmetic.

A variable in 1107 FORTRAN may have up to seven subscripts, meaning that seven-dimensional arrays can be handled; 7090/7094 FORTRAN IV is limited to three dimensions. Furthermore, subscript expressions may have more complex forms in the 1107 version, though they are still limited to integer constants and variables.

The possibilities for mixed-mode arithmetic, both among the operands of an arithmetic expression and between the left and right sides of an arithmetic statement, are much broader in 1107 FORTRAN. Among the four possible types of arithmetic operands -- integer, real, double precision, and complex -- only double precision and complex values may not be freely combined.

The FORTRAN IV statements that are available in 1107 FORTRAN are listed in Paragraph .144 below. The 1107 FORTRAN Compiler maintains a reasonable degree of compatibility with the FORTRAN II language by accepting and correctly interpreting the FORTRAN II statements listed in Paragraph .145.

An even more effective means for running existing FORTRAN II programs on the 1107 is provided by the SIFT translator. SIFT was developed by the SHARE organization to translate FORTRAN II source programs into FORTRAN IV. Written in FORTRAN II, SIFT was used to translate itself into FORTRAN IV

.14 Description (Contd.)

on an IBM 7090. Then the resulting FORTRAN IV version of SIFT was successfully compiled and run on the UNIVAC 1107. Because of the availability of the SIFT translator, no FORTRAN II compiler is planned for the 1107.

The 1107 FORTRAN Compiler will operate under control of the EXEC II operating system. Minimum configuration requirements are 32,768 words of core storage and 1 Flying Head 880 Magnetic Drum. Magnetic tape is not required, and is of no advantage in compilation. Documentation produced by the compiler includes a storage allocation map and a listing of the object program instructions in both symbolic and octal form, with corresponding source statements and diagnostic messages interspersed.

Compilation speed is unusually high, primarily because of the fast-access, high-capacity storage for the translator and interim language provided by the magnetic drum. Tests performed to date indicate that, on the average, between 5,000 and 6,000 object program instructions per minute will be generated. In typical programs, an average of 3 to 3.5 machine instructions will be produced for each source program statement.

Input data for a FORTRAN IV object program arrives via the card-to-drum "symbiont" and final output is via the drum-to-tape "symbiont" (see EXEC II, Section 784:192). During the actual execution of the object program, input data is assumed to be on the drum and output data is filed on the drum. This is automatic unless the user specifies use of the magnetic tape input and output symbionts instead.

The manufacturer expects object program efficiencies to be, in general, "better than the average programmer can write in an assembly language," because of the optimizing features of the compiler.

The number of Core Memory locations required at execution time to hold the standard FORTRAN subroutines and tables are tabulated below.

Routine	Bank 1 Locations	Bank 2 Locations
Input subroutines:	383	9
Output subroutines:	482	39
FORMAT Scan subroutine:	486	-
I/O Table:	12	32
Data List Scan:	26	-

.141 Availability

Language: . . . . . August, 1962.
Translator: . . . . . currently in field test status.

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.142 Restrictions

(1) The two arithmetic expressions that are combined by a relational operator (such as .GT., for "greater than") to form a logical expression should be of the same type; otherwise, a diagnostic note will indicate that the comparison may not be meaningful. FORTRAN IV for the 7090/7094 permits REAL and DOUBLE PRECISION expressions to be combined.

(2) Octal digit values cannot be assigned to object program variables at loading time by means of the DATA statement.

.143 Extensions

(1) A variable may have up to seven subscripts, versus a maximum of three subscripts in IBM 7090/7094 FORTRAN IV.

(2) Subscripts must have the general form

$$\pm M_1 \pm M_2 \pm M_3 \ldots \pm M_i$$

where each M may be an integer constant, an integer variable, or an expression of the form

$$n * K_1 * K_2 * \ldots K_j,$$

in which n is an integer constant and each K is an integer variable. Subscripts in IBM 7090/7094 FORTRAN IV are limited to the form $n*k + n'$, where n and n′ are unsigned integer constants and k is an integer variable. Therefore, the expression I + 2*J*K - 4 is a valid subscript in 1107 FORTRAN but not in 7090/7094 FORTRAN.

(3) The PARAMETER statement assigns specified integer values to specified variables at compile time; e.g., PARAMETER I = 2 causes the integer 2 to replace I wherever it occurs in the source program. This facilitates the assignment of different values to frequently-referenced parameters in different compilations of the same program.

(4) Arithmetic operations (+, -, *, /) can be performed more freely upon operands of different types. Specifically, the following types of arithmetic operand pairs are permitted in 1107 FORTRAN but not in 7090/7094 FORTRAN IV:

REAL-INTEGER
COMPLEX-INTEGER
DOUBLE PRECISION-INTEGER

(5) In arithmetic statements, the following combinations of expressions (on the right side of the equal sign) and variables (on the left side) can be equated in 1107 FORTRAN, but not in 7090/7094 FORTRAN IV:

Variable on left	Expression on right
INTEGER	COMPLEX
REAL	COMPLEX
COMPLEX	INTEGER
COMPLEX	REAL

.143 Extensions (Contd.)

(6) The optional ABNORMAL statement permits increased optimization of object programs. Where common subexpressions occur within a statement, it is obviously desirable to evaluate each subexpression only once. Where the common subexpressions contain function references, however, there is a possibility that the function will produce different results upon successive references with the same arguments (e.g., where the function contains input statements or local variables whose values are not initialized each time the function is referenced). UNIVAC 1107 FORTRAN permits all functions that can produce different results from identical sets of arguments to be designated ABNORMAL. All common subexpressions except those that reference ABNORMAL functions are evaluated only once. When the ABNORMAL statement does not appear at all in a program, all function references are considered ABNORMAL and re-evaluated at each occurrence, as in most other FORTRAN systems.

(7) The following standard library functions are included in 1107 FORTRAN but not in 7090/7094 FORTRAN IV:

Tangent (REAL, DOUBLE PRECISION, and COMPLEX)
Arcsine (REAL and DOUBLE PRECISION)
Arccosine (REAL and DOUBLE PRECISION)
Hyperbolic Sine (REAL, DOUBLE PRECISION, and COMPLEX)
Hyperbolic Cosine (REAL, DOUBLE PRECISION, and COMPLEX)
Cube Root (REAL, DOUBLE PRECISION, and COMPLEX)

.144 UNIVAC 1107 FORTRAN Statements

ABNORMAL
ASSIGN n to i
BACKSPACE Unit
CALL s (a_1, a_2, . . . , a_n) or CALL s
COMMON/Block name/Variable names/Block name/Variable names . . .
CONTINUE
DIMENSION array 1 (parameters), array 2 (parameters) . . .
DO n i = j, k, m
END
END FILE Unit
EQUIVALENCE (Variable names), (Variable names, . . .), . . .
EXTERNAL
FORMAT (Format Specification)
FUNCTION f (a_1, a_2, . . . a_n)
GO TO m
GO TO n
GO TO i (n_1, n_2, . . . , n_m)
GO TO (transfer list), i
IF (arithmetic statement) j, k, m
IF (logical expression) FORTRAN statement
INTEGER
INTEGER FUNCTION
LOGICAL
LOGICAL FUNCTION
PARAMETER
PAUSE n (n may be omitted)

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.144 UNIVAC 1107 FORTRAN Statements (Contd.)

READ (Unit) List
READ (Unit, Format) List
REAL
REAL FUNCTION
RETURN
REWIND Unit
STOP
SUBROUTINE Name (a_1, a_2, . . . , a_n)
Variable = arithmetic expression
WRITE (Unit) List
WRITE (Unit, Format) List

.145 Acceptable FORTRAN II Statements

IF ACCUMULATOR OVERFLOW n_1, n_2
IF QUOTIENT OVERFLOW n_1, n_2
IF DIVIDE CHECK n_1, n_2
IF (SENSE LIGHT i) n_1, n_2
IF (SENSE SWITCH i) n_1, n_2
PRINT Format, List
PUNCH Format, List
Read n, List
READ INPUT TAPE i, N, List
READ TAPE i, List
SENSE LIGHT i
WRITE OUTPUT TAPE t, Format, List
WRITE TAPE t, List

MACHINE ORIENTED LANGUAGE: SLEUTH I

§ 171.

.1 GENERAL

.11 Identity: . . . . . SLEUTH I Assembly System.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corp.

.13 Reference: . . . . . UNIVAC Technical Bulletin UT-2574.

.14 Description

SLEUTH I is a symbolic assembly system and a primary component of the "SLEUTH I Package" or "A Package," one of two basic software packages for the UNIVAC 1107. The SLEUTH I Package was developed by UNIVAC's Systems Programming Department in St. Paul; its other components (EXEC I, CLAMP, Librarian, LION, MIDAS, and Sort/Merge) are described in Sections 784:151 and 784:191. There is no compatibility between the SLEUTH I and SLEUTH II assembly languages or between the components of their respective software packages.

SLEUTH I permits utilization of all the hardware facilities of the 1107, provides facilities for the definition and use of macro instructions, and produces object programs that can be multi-run under the control of the EXEC I operating system.

The SLEUTH I coding sheet provides columns for Tags (labels), Functions (operation codes), and Sub Fields. SLEUTH I (unlike SLEUTH II) uses the mnemonic operation codes shown in the Instruction List, Section 784:121. Depending upon the operation to be performed, the free-form Sub Fields column can contain a wide variety of entries, including designation of partial word operands, literal operands, direct or indirect operand addresses, arithmetic and index registers, constants, and macro instruction parameters. The facilities for generating constants in integer, fixed point, floating point, and alphameric modes make programming much easier.

Macro-instructions make possible the generation of a series of instructions or data words from a single source program line. The definitive instructions or "skeleton" for the macro can be contained in the source program or on the program library tape. All variables in the macro skeletons are coded with parameter identifiers consisting of decimal integers enclosed in parentheses. When the name of a particular macro is used as a function code in the source program, the associated parameters are substituted for the numbered parameter identifiers and the macro is assembled and inserted into the object program in straight-line fashion.

To guard against accidental duplication of symbols, source programs can be divided into sections by the SEC pseudo operation. If an address label is defined only once, it is considered universal to the entire program. If an address label is defined in more than one section, however, each definition will apply only to the particular section in which it appears. This means that no address label should be referenced in a section other than the one in which it is defined unless the coder is certain that the label is defined only once in the entire program.

.14 Description (Contd.)

Corrections to a source program are handled by preparing a separate correction deck with pseudo operation codes designating where deletions and/or additions are to be made. All source program instructions preceded by an asterisk can be deleted by a single pseudo operation in the correction deck; this facility makes it easy to remove links to trace routines and other extraneous instructions after a routine has been checked out.

The object program can be produced in any of three formats:

- AOC (Absolute Object Code) - absolute, non-relocatable binary form, ready for immediate loading and execution, with no executive system control.
- DIRECT ROC (Relative Object Code - Direct I/O) - relocatable form, ready for loading by the CLAMP Relative Load Routine. Input-Output references can be reassigned at load time, but there is no provision for executive system control.
- EXEC ROC (Relative Object Code - Executive System I/O) - relocatable form, ready for loading by EXEC I. All input-output references are symbolic, and operation must be under control of the EXEC I operating system. All input-output operations are initiated via requests to EXEC I and controlled by its standard subroutines.

SLEUTH I is a two pass assembly system. The first pass develops a dictionary of symbolic assignments and decodes a major portion of each symbolic instruction. The second pass completes the decoding, using the dictionary and the output of the first pass to produce the desired form of object program output and the assembly listing. Documentation produced by the SLEUTH I translator consists of a side-by-side listing of the source program and assembled object program instructions. Coding errors detected by the translator are identified by error codes.

.15 Publication Date: . . . . April, 1962.

.16 Translator Availability: released November, 1962.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . refer to SLEUTH I Coding Specimen, Section 784:131.

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.22 Legend

Tag:	a label; the symbolic address of a line of coding.
Function:	the operation to be performed: machine, pseudo, or macro.
Sub Fields:	describe the objective of the Function code: arithmetic register, operand address, literal operand, shift count, indirect addressing, index register, partial word designator, constant to be generated, macro parameters, etc., as required by the particular operation. Sub fields are separated by commas.

.23 Corrections: . . . . . corrections are listed on a separate input medium and merged with original source program during first translator pass.

.231 Insertions:	insert any number of lines of coding after a FOLLOW pseudo, which designates the instruction preceding the insertions.
.232 Deletions:	delete single instruction, block of instructions, or all instructions preceded by an asterisk, using DELETE pseudo.
.233 Alterations:	replace deleted instruction(s) with any number of new lines of coding following the DELETE pseudo.

.24 Special Conventions

.241 Compound address: . .	BASE ± ADJUSTMENT, where BASE is any label and ADJUSTMENT is the algebraic sum of a combination of integers and "absolute tags"; i.e., symbols representing numeric constants.
.242 Multi-addresses: . . .	most machine instructions can specify a special register in Film Memory as well as the operand address in core storage.
.243 Literals:	$UOP or $XUOP in j-field indicates that u-field contains a literal in octal or decimal integer form; alternatively, a "literal expression" in the u-field, enclosed in parentheses, can generate a floating point, fixed point, or integer constant.
.244 Special coded addresses:	$L refers to current instruction address. * designates an indirect address.

.3 LABELS

.31 General

.311 Maximum number of labels:	4,096.
.312 Common label formation rule:	yes; see Paragraph .321.
.313 Reserved labels	
For Arithmetic Registers:	$A0 to $A15.
For Index Registers: .	$B0 to $B15.
For Special Registers:	$R0 to $R15.
For Q Registers (the 4 overlapping Arithmetic and Index Registers):	$Q0 to $Q3.
.314 Other restrictions: . .	none.
.315 Designators:	initial dollar sign designates assembler-defined (reserved) labels.
.316 Synonyms permitted: .	yes; EQU pseudo.

.32 Universal Labels

.321 Labels for procedures	
Existence:	mandatory if referenced by other instructions.
Formation rule	
First character: . .	letter or numeral (dollar sign for reserved labels).
Others:	letters or numerals.
Number of characters:	1 to 6; at least 1 must be alphabetic.
.322 Labels for library routines:	same as procedures.
.323 Labels for constants: .	same as procedures.
.324 Labels for files:	same as procedures.
.325 Labels for records: . .	same as procedures.
.326 Labels for variables: .	same as procedures.

.33 Local Labels: . . . . . a program can be divided into sections by use of the SEC pseudo. The lines of coding between two SEC pseudos constitute a section. All address labels defined only once are universal to the entire program. If an address label is defined in more than one section, however, each definition will apply only to the particular section in which it appears.

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.4 DATA

.41 Constants

.411 Maximum size constants

Machine form	Coding sheet form
Integer	
Decimal:	none.
Binary (function code W):	11 decimal digits; or 12 octal digits with prefix $.
Binary half-words (code H):	6 decimal or octal digits per half-word.
Binary third-words (code T):	3 decimal or octal digits per third-word.
Binary sixth-words (code S):	2 decimal or octal digits per sixth-word.
Fixed numeric	
Decimal:	none.
Binary (code WX):	decimal value, decimal exponent, and binary scale factor (exponent and scale factor can be omitted when they are 0).
Floating numeric	
Decimal:	none.
Binary (code WF):	rational decimal value and decimal exponent (exponent can be omitted when 0).
Alphameric (code SC):	60 characters.

.412 Maximum size literals

Machine form	Coding sheet form
Integer	
Decimal:	none.
Binary:	6 decimal digits; or 6 octal digits with prefix $. See also Paragraph .411 (code W).
Fixed numeric	
Decimal:	none.
Binary:	see .411 (code WX).
Floating numeric	
Decimal:	none.
Binary:	see .411 (code WF).
Alphameric:	none.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic

Existence:	mandatory.
Number:	115.
Examples:	ADM = add magnitude. IMIM = initiate monitored input mode.
Comments:	different from SLEUTH II mnemonic codes.

.512 Absolute

Existence:	decimal or octal integer.

.52 Macro-Codes

.521 Number available

Input-output:	18 (LION macros).
Arithmetic:	0.
Math functions:	0.
Error control:	0.
Restarts:	0.

Note: Other user-defined macros can be added to the library.

.522 Examples

Simple:	SQRT (X).
Elaborate:	NFUNCT (A1) (A2) (A3) (P).

.523 New macros: can be included in program or inserted into the library in a separate run.

.53 Interludes: none.

.54 Translator Control

.541 Method of control

Allocation counter:	pseudo operations.
Label adjustment:	pseudo operations.
Annotation:	see Paragraph .544.

.542 Allocation counter

Set to absolute:	IBANK, DBANK pseudos.
Set to label:	IBANK, DBANK pseudos.
Step forward:	IBANK, DBANK pseudos.
Step backward:	IBANK, DBANK pseudos.
Reserve area:	RESV pseudo.

.543 Label adjustment

Set labels equal:	EQU pseudo.
Set absolute value:	EQU pseudo.
Clear label table:	none.

.544 Annotation

Comment phrase:	in any line of coding, following colon.
Title phrase:	PRO pseudo.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: no routines announced to date.

.62 Special Functions: no routines announced to date.

.63 Overlay Control: no routines; handled by own coding.

.64 Data Editing: handled by LION (Library of Input-Output Numerical Subroutines); see 784:151.15 and 784:171.81.

.641 Radix conversion: between decimal and binary radices, by IMGIN and IMGOUT macros.

Code translation: automatic, by hardware.

.642 Format control (by IMGOUT macro)

Zero suppression:	yes.
Size control:	yes.
Sign control:	yes.
Special characters:	insert sign and point only.

.643 Method of call: macros cause insertion of open subroutines.

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.65 Input-Output Control: . handled by LION (Library of Input-Output Numerical Subroutines).

.651 File labels: . . . . . yes.
.652 Reel labels: . . . . . yes.
.653 Blocking: . . . . . yes.
.654 Error control: . . . . . yes.
.655 Method of call: . . . . . macros cause insertion of open subroutines.

.66 Sorting: . . . . . none (but see SORT/MERGE, 784:151.13).

.67 Diagnostics

.671 Dumps: . . . . . MIDAS, a set of subroutines called by SLEUTH macros, provides listings on tape or printer of the contents of specified areas of storage in octal, decimal, floating point, alphameric, or instruction format. An option permits listing only those locations whose contents have been altered during execution of the program being tested.
.672 Tracers: . . . . . none.
.673 Snapshots: . . . . . MIDAS; see Paragraph .671.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . created and maintained by LIBRARIAN routine.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.
.723 Private: . . . . . yes.

.73 Storage Form: . . . . . magnetic tape.

.74 Varieties of Contents: . programs, subroutines.

.75 Mechanism

.751 Insertion of new item: . special library run.
.752 Language of new item: . SLEUTH I or relocatable machine code.
.753 Method of call: . . . . . LOCATE or INSERT pseudo for inclusion at assembly time.
XREF pseudo for inclusion at load time.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: . . . . . yes.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros

LION macros for Internal Format (binary) Subroutines

Code	Description
IOCON:	generates file control table for an output file.
IICON:	generates file control table for an input file.
OPNOUT:	opens an output file.
OPNIN:	opens an input file.
ITMOUT:	moves an item to an output buffer area.
ITMIN:	makes an input item available for processing.
OENREL:	closes reel on an output file.
IENREL:	closes reel on an input file.
OENFIL:	closes an output file.
IENFIL:	closes an input file.

LION macros for External Format (FIELDATA) Subroutines

Code	Description
EOCON:	generates file control table for an output file.
EICON:	generates file control table for an input file.
EOPOUT:	opens an output file.
EOPIN:	opens an input file.
IMGOUT:	converts binary fields to FIELDATA characters, forms an image suitable for output on printer or card punch, and moves it to an output buffer area.
IMGIN:	converts 80-character printer images to binary fields and makes them available for processing.
EXOEND:	closes an output file.
EXIEND:	closes an input file.

.82 Pseudos

Code	Description
PRO:	names program and defines format of object program.
ENDPRO:	signifies end of source program and defines starting address.
EQU (or =):	assigns a value to a label or relates two labels.
IBANK:	controls placement of words in the instruction area of core storage.
DBANK:	controls placement of words in the data area of core storage.
BANK:	causes following coding to be placed in next available locations in opposite bank.

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.82 Pseudos (Contd.)

Code	Description
DTABLE:	defines a data table whose size can be modified at load time.
W:	generates a 36-bit integer constant.
WF:	generates a floating point constant.
XF:	generates a fixed point scaled constant.
H:	generates two 18-bit values in a single word.
T:	generates three 12-bit values in a single word.
S:	generates six 6-bit values in a single word.
G:	generates a number of fields of specified lengths in a single word.
SC:	generates an alphameric constant of up to 60 FIELDATA characters, stored six per word.
XS3:	generates an alphameric constant of up to 60 XS-3 characters, stored six per word.
RESV:	reserves a block of words and fills them with zeros.

.82 Pseudos (Contd.)

Code	Description
MACRO:	signals start of a macro definition; i.e., the instructions which constitute the "skeleton."
ENDMAC:	signals end of a macro definition.
SWITCH:	names a console Selective Jump switch.
SPACE:	causes n blank lines in listing.
EJECT:	causes skip to top of next page in listing.
COR:	heads correction deck and names the program to be corrected.
DELETE:	causes deletion of a single instruction, a block of instructions, or all instructions preceded by *.
FOLLOW:	designates the source instruction after which insertions are to be made.
ENDCOR:	signals end of a correction deck.
XREF:	names and specifies entry points for a library subroutine to be added at load time.
INSERT:	permanently inserts library subroutine(s).
LOCATE:	calls in library subroutine(s) for a single assembly.

OPERATING ENVIRONMENT: EXEC I

§ 191.

.1 GENERAL

.11 Identity: . . . . . EXEC I.
UNIVAC 1107 Executive System.

.12 Description

EXEC I is an integrated operating system for the UNIVAC 1107. It provides the means for automatically processing a scheduled set of jobs, either serially or concurrently, with a minimum of operator intervention. EXEC I is a major component of the SLEUTH I software package; it is not directly compatible with the SLEUTH II assembly system or its associated operating system, EXEC II (Section 784:192). Object programs produced by the 1107 COBOL and FORTRAN Compilers and the SLEUTH II assembly system can be executed under the control of EXEC I through the use of COORDINATOR, described in Section 784:151.17, which provides the necessary interface. A planned extension of EXEC I will enable it to control COBOL and FORTRAN compilations as well.

EXEC I consists of a related set of subroutines that can be modified to suit the needs of specific installations. It performs the following functions:

- Schedule Maintenance - The acceptance of Job Requests from any input device and use of these requests to construct a job schedule.
- Selection - The use of information in the job schedule to select the next job to be initiated. Selection is based upon the specified priority and sequence relationships and the availability of the necessary facilities.
- Facility Assignment - The assignment of storage and peripheral devices to meet the symbolically defined requirements of each program. EXEC I maintains an up-to-date list of the status of all facilities and attempts to assign Core Memory (in 2,048-word blocks) and input-output channels for maximum overall efficiency.
- Loading - The transfer of a program from a storage medium to the operational facilities assigned to it. Loading is handled by CLAMP, the 1107 Relative Load Routine (see 784:151.17).
- Interrupts - The use of the 1107's interrupt facilities to cause entrance to subroutines that deal with processor errors. Unless error recovery routines are furnished by the user, each error interrupt will cause termination of the offending program with a storage dump.

.12 Description (Contd.)

- Input-Output - The acceptance, scheduling, and processing of all requests for input-output functions from the operating programs. Three request lists are maintained for each of the 15 input-output channels. Each request is assigned to the high, medium, or low priority list for a particular channel, as specified by the programmer. The 1107's interrupt facilities and the request lists are used to keep each channel as fully occupied as possible. Automatic recovery from input-output errors is provided where feasible.
- Switching - The provision for transfers of control between two or more programs being run at the same time. Programs are assigned to one of two Switch Lists, depending upon whether they have been classified as "I/O-limited" or "compute-limited" by the programmer. Whenever an I/O-limited program must wait for completion of an input or output operation, control is transferred to the next I/O-limited program on the list. Whenever none of the I/O-limited programs can continue, control is transferred to a compute-limited program until an external interrupt notifies EXEC I that an input-output operation has been completed and control can be returned to one of the I/O-limited programs.
- Communication - The provision for all communication between the operator and the system by means of the console keyboard and printer.
- Logging - The recording of the approximate internal processing time used by each program and the unused central processor time. This facilitates determination of the programs that should be multi-run together for maximum overall efficiency.
- Termination - The normal or abnormal termination of a program and the return of the facilities assigned to it to "available" status. Termination can be initiated by the program itself, by EXEC I, or by the operator.

.13 Availability: . . . . . December, 1962.

.14 Originator: . . . . . UNIVAC Division, Sperry Rand Corporation.

.15 Maintainer: . . . . . as above.

.16 Reference: . . . . . UNIVAC Technical Bulletin UP-2577, May, 1962.

.2 PROGRAM LOADING

.21 Source of Programs: . . specified by control cards or console type-ins.

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.211 Programs from on-line libraries:. . . . . from magnetic tape or drum libraries created and maintained by LIBRARIAN (see 784:151.16).

.212 Independent programs: from any specified input device.

.213 Data:. . . . . from any available input device, as specified in program.

.214 Master routines:. . . . EXEC I is stored on a system tape in absolute form.

.22 Library Subroutines: . subroutines required by a main program but not incorporated into it are loaded from a subroutine library tape by CLAMP (see 784:151.17).

.23 Loading Sequence: . . . Job Request cards are used to construct a job schedule. Then, based upon the specified priority and sequence relationship and equipment availability, jobs are selected, loaded, and initiated. Jobs can be added to or deleted from the schedule at any time. When a magnetic drum is available, from 50 to 130 Job Requests can be stored in a 2,000-word area reserved for the schedule.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . . must be incorporated in user's program.

.312 Occupation of working storage: . . . . . as programmed; i.e., no automatic facilities for transfer of program segments between core and drum or core and tape.

.32 Input-Output Units

.321 Initial assignment:. . . all program references to input-output devices must be symbolic; the required facilities are defined by control cards, and actual assignments are made automatically by EXEC I at loading time.

.322 Alternation: . . . . . as incorporated in user's program.

.323 Reassignment:. . . . . same as initial assignment; can release assigned facilities for use by another program.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: EXEC I controls all input-output operations and attempts to maximize utilization of the available peripheral devices.

.42 Multi-running:. . . . . number of simultaneously running programs is limited only by equipment availability. Switching techniques are described in Paragraph .12.

.43 Multi-sequencing: . . . no provisions.

.44 Errors, Checks and Action

Error	Check or Interlock	Action
Loading input error:	check	reload program.
Allocation impossible:	EXEC I checks	select another program.
In-out error - single:	interrupt	try again.
In-out error - persistent:	interrupt	type message and return to program with error indication.
Program conflicts:	?	
Arithmetic overflow:	interrupt	programmer-specified.‡
Underflow:	interrupt	programmer-specified.‡
Invalid operation:	interrupt	programmer-specified.‡
Invalid address:	check	type message and dump program.
Reference to forbidden area:	interrupt	terminate program with storage dump.

‡ If no error recovery subroutine is furnished by the programmer, the program will be terminated with a storage dump.

.45 Restarts

.451 Establishing restart points: . . . . . as incorporated in user's program, according to specified tape dump format. Restart table is produced by EXEC I at user's program request.

.452 Restarting process: . . as incorporated in user's program; or initiated under EXEC I control (using the restart table) and completed by user's program.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . hardware trace mode is available through EXEC I.

.512 Snapshots: . . . . . as incorporated in user's programs (see MIDAS, Section 784:151.17).

.52 Post Mortem: . . . . . a dump of Film Memory, all Core Memory locations assigned to the program, and other diagnostic information is produced automatically upon termination of a job

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.52 Post Mortem (Contd.): due to a non-recoverable error interrupt or upon program or operator request. The dump is written on tape for later transcription on the High-Speed Printer.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . . console printer messages, under control of EXEC I or user's program.

.612 Action required by operator: . . . . . same as .611.

.613 Reporting progress of run: . . . . . same as .611.

.62 Operator's Decisions: keyboard entries or console switch settings.

.63 Operator's Signals:

.631 Inquiry: . . . . . keyboard entries.

.632 Change of normal progress: . . . . . keyboard entries.

.7 LOGGING

.71 Operator Signals: . . . console printer.

.72 Operator Decisions: . . console printer.

.73 Run Progress: . . . . . console printer.

.74 Errors: . . . . . console printer.

.75 Running Times: . . . . console printer.

.76 Multi-running Status: console printer lists programs comprising the current "mix" before each program is initiated, for approval or rejection by the operator.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configurations: . . . . 1107 Central Computer with
16,384 Core Memory locations.
1 magnetic tape handler.
1 card reader (paper tape or drum can be used instead).
1 printer.

.812 Usable extra facilities: all.

.813 Reserved equipment: 8,192 Core Memory locations.
12 Film Memory locations.
50,000 magnetic drum locations.
Control Console.
Real-Time Clock.

.82 System Overhead

.821 Loading time: . . . . . ?

.822 Reloading frequency: resident portions of EXEC I remain in Core Memory; other portions are called in automatically as required.

.83 Program Space Available: . . . . . all of available core and drum storage except reserved areas listed in Paragraph .813.

.84 Program Loading Time: dependent upon program input device.

.85 Program Performance: EXEC I overhead is estimated by manufacturer to be about 1 to 2% of total processing time in typical multi-running applications.

OPERATING ENVIRONMENT: EXEC II

§ 192.

.1 GENERAL

.11 Identity: . . . . . EXEC II.
UNIVAC 1107 Monitor System.

.12 Description

EXEC II is being developed by Computer Sciences Corporation as an integrated operating system to control the translation and execution of programs coded in SLEUTH II, COBOL, and FORTRAN. The system is designed to achieve high utilization of the available equipment by using one or more FH-880 Magnetic Drums as high capacity back-up stores to keep the card readers, punches, and printers fully occupied without delaying execution of the main program. No facilities for true multi-running (i.e., processing several independent main programs simultaneously) are provided.

EXEC II consists of three distinct parts: a set of input-output routines, an information storage and retrieval scheme, and a set of diagnostic routines.

The input-output subroutines handle all communication between the 1107 Central Computer and its peripheral devices, under the control of a routine always found in Core Memory called the Dispatcher. All peripheral operations can be performed on-line, eliminating the need for off-line data transcription equipment. To prevent main programs from being limited by the speeds of card readers, punches, or printers, "symbiont" routines are provided which permit on-line card-to-drum, drum-to-card, and/or drum-to-printer data transcriptions to be performed concurrently with the execution of a main program. The user can design his programs to accept all input data from the drum in the form of card images in Fieldata code and transmit all output data to the drum in the form of card images or printer line images at the core-to-drum transfer rate of 60,000 words per second. The appropriate data transcription operations are automatically performed by the symbiont routines, which interrupt the user's main program as required to keep the peripheral devices operating at full speed. Magnetic tape can be used in place of the drum to provide back-up storage for the peripheral devices if desired.

Magnetic tape, drum, paper tape, and console input-output operations are handled more directly in that no back-up storage or symbiont routines are involved. A separate subroutine is provided for each type of peripheral device. The programmer must write a subroutine link accompanied by the appropriate parameters to initiate each input or output operation. Four different levels of input-output programming are available at the user's option. Input-

.12 Description (Contd.)

output errors can be handled according to standard techniques or user-coded routines.

The EXEC II information storage and retrieval system is designed to facilitate the construction of programs from their component elements, the creation and maintenance of program libraries, and the manipulation and loading of object programs. The SLEUTH II assembler and the FORTRAN and COBOL compilers are integrated into the system, and the system organization is "open-ended" so that other translators can be incorporated.

The EXEC II library of independent programs and subroutines is called the Program Complex File, or PCF. The PCF resides on the magnetic drum while in use, and the entire PCF or any of its elements can be transcribed to or from either magnetic tape or punched cards. The PCF can contain the following types of elements:

- Symbolic programs in SLEUTH II, COBOL, FORTRAN, or any other source language for which a translator has been incorporated.
- Relocatable programs produced by the SLEUTH II, COBOL, or FORTRAN translators.
- Absolute programs in non-relocatable, machine language form.
- Maps, produced by EXEC II's "Memory Allocation Processor," which define storage allocation, segmentation, and loading techniques for specific programs.
- COBOL Library entries, which can be called by the COPY verb of COBOL-61.
- Procedure definitions, which can be called by the DO directive of SLEUTH II.

By means of varied control card entries, a variety of system operations can be initiated, including compilations, assemblies, loading and execution of object programs, storage dumps after execution, insertions into the Program Complex File, and combinations of any or all of these operations. The sequence of program operations and the assignment of peripheral devices are controlled by the entries on the control cards.

Flexible control of object program segmentation is provided. The SEG operation card defines each segment and specifies, in a pseudo-algebraic language, which other segments and subsegments must occupy working storage simultaneously and which may be overlaid. A segment can be loaded into Core Memory from the drum either "manually," by means of

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.12 Description (Contd.)

an explicit program request, or "automatically," by means of a jump instruction to an entry point within a segment that is not currently loaded.

A program too large to fit into Core Memory can alternatively be handled by executing it as a series of smaller, relatively independent programs called "links," which can share a common data area in Core Memory. This technique is similar to the CHAIN function of IBM 709/7090 FORTRAN II, described in Section 408:191.

The EXEC II diagnostic routines will be designed to facilitate program testing by permitting the programmer to be highly selective in specifying the data to be dumped. Both dynamic (snapshot) dumps and postmortem dump procedures will be provided. Dump listings can be produced with the symbolic instructions intercollated with the actual Core Memory contents.

Operation of EXEC II requires an 1107 with at least 16,384 words of Core Memory, 1 FH-880 Magnetic Drum, 1 card reader, 1 card punch, and 1 printer. All available equipment can be utilized. The resident routines of EXEC II itself occupy an average of 3,000 to 3,500 Core Memory locations and a maximum of about 8,000 locations. A minimum of 80,000 words of drum storage are required for the monitor routines, the translators, and the library. Drum storage is also used to hold the absolute program to be run, the diagnostic information collected during and after execution, and input-output data for the symbiont routines.

.13 Availability: . . . . . over 90% operational and undergoing field testing as of July, 1963.

.14 Originator: . . . . . Computer Sciences Corporation.

.15 Maintainer: . . . . . UNIVAC.

.16 Reference: . . . . . Programmer's Reference Manual: UNIVAC 1107 Monitor System, January, 1963. (This is a CSC manual; final documentation will be published soon by UNIVAC.)

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . . Program Complex File (PCF) contains programs and subroutines in absolute, relocatable, or source language (SLEUTH II, COBOL, or FORTRAN) form. The PCF normally resides on the drum, but can be transcribed to or from magnetic tape or punched cards. Loading and allocation is directed by control cards.

.212 Independent programs: punched cards or magnetic tape.

.213 Data: . . . . . any available type of input device, as specified in program.

.214 Master routines: . . . . EXEC II is stored on an FH-880 Magnetic Drum. Resident routines are held in Core Memory at all times and other segments are loaded as required.

.22 Library Subroutines: . subroutines referenced in a main program but not incorporated into it are automatically loaded from the Program Complex File or the Systems Library.

.23 Loading Sequence: . . . programs are loaded and executed in the sequence in which their control cards are read; therefore, all sequencing is manually controlled.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . . program segments are defined by the SEG control card which specifies, in a pseudo algebraic language, how each segment is related to other segments and subsegments.

.312 Occupation of working storage: . . . . . a segment can be loaded into Core Memory from the drum either "manually," by an explicit program request, or "automatically," by a jump instruction to an entry point within the segment.

.32 Input-Output Units

.321 Initial assignment: . . . tape units are referenced by symbolic logical unit designations in programs. Assignment of specific physical units can be made by control cards, Keyboard entries, or subroutines.

.322 Alternation: . . . . . any number of tape units can be assigned to a specific file and switched cyclically by reference to the T$SWAP subroutine.

.323 Reassignment: . . . . . possible during a run, using the T$AGN subroutine; otherwise, same as initial assignment.

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.4 RUNNING SUPERVISION

.41 Simultaneous Working: Dispatcher routine controls all input-output operations and attempts to maximize utilization of the available peripheral devices.

.42 Multi-running: . . . . . no facilities for multi-running of independent main programs, but data transcription operations can be performed concurrently with the processing of one main program.

.43 Multi-sequencing: . . . no provisions.

.44 Errors, Checks and Action

Error	Check or Interlock	Action
Loading input error:	check	print message and offer options.
Allocation impossible:	check	print message and offer options.
In-out error - single:	checks	try again.
In-out error - persistent:	checks	jump to user-coded error routine.
Internal transfer error:	none.	
Arithmetic overflow:	check	save address of the offending instruction.
Underflow:	check	save address of the offending instruction.
Invalid operation:	check	print message and terminate run.
Invalid address:	check	print message and terminate run.
Reference to forbidden area:	check	print message and terminate run.

.45 Restarts: . . . . . no specifications published to date, but facilities will be included.

.5 PROGRAM DIAGNOSTICS: . . . . an integrated system of snapshot and post-mortem dump routines will be provided, but their specifications have not been released to date.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . . console printer messages.

.612 Action required by operator: . . . . . console printer messages.

.613 Reporting progress of run: . . . . . console printer messages.

.62 Operator's Decisions: . console keyboard entries, control cards, or console switch settings.

.63 Operator's Signals

.631 Inquiry: . . . . . console keyboard entries.

.632 Change of normal progress: . . . . . control cards must be manually resequenced or altered. Control card MSG may request decision.

.7 LOGGING: . . . . . console printer messages produced by EXEC II.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: 16,384 Core Memory locations.
1 FH-880 Magnetic Drum.
1 Card Reader.
1 Card Punch.
1 High-Speed Printer.

.812 Usable extra facilities: larger Core Memory and all available peripheral devices.

.813 Reserved equipment: . 3,000 to 8,000 words of Core Memory for resident sections of EXEC II.
at least 80,000 words of drum storage for EXEC II, processors, and library.
Film Memory locations 0, 32 through 64, and 80 through 87.
1 card channel and 1 printer channel.
Control Console.
23 machine instructions (mostly I/O instructions), which may not be used in programs to be run under EXEC II control.

.82 System Overhead

.821 Loading time: . . . . . for drum-to-core transfers: 17 msec average access time plus 0.0163 msec per word transferred.

.822 Reloading frequency: . EXEC II remains on drum; segments are loaded into Core Memory automatically as required.

.83 Program Space Available: . . . . . all of available core and drum storage except reserved areas listed in Paragraph .813.

.84 Program Loading Time: dependent upon program input device; less than 1 second when magnetic drum is used.

.85 Program Performance: EXEC II overhead is estimated to be less than 1 per cent of total processing time in typical applications.

SYSTEM PERFORMANCE

§ 201.

Generalized File Processing (784:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

Because the UNIVAC 1107 can process several independent programs at the same time through multi-running, the amount of central processor time required by each program is highly significant. The difference between the total elapsed time for a particular run and the amount of central processor time required for that run represents processor time that is potentially available to other programs. Whether or not this processor time can be efficiently utilized depends upon the system configuration, the over-all problem mix, and the effectiveness of the scheduling and operating system.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configuration VIIIB, where all four input-output files are on magnetic tape, total times for cases using both unblocked and blocked records in the detail and report files are shown by means of solid and dashed lines, respectively. Central processor time is essentially the same for all configurations, and is shown by the broken line marked "CP" on each graph. No addition has been made to the processor time to cover the overhead requirements of the operating system. As indicated in Paragraph 784:191.85, the manufacturer expects the EXEC I system to require, on the average, only 1 to 2 per cent of the total processor time.

Worksheet Data Table 1 (page 784:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for integrated Configurations VI and VIIA. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a small fraction of the total processing time. When scientific programs with limited input and output can be run simultaneously in order to utilize the remaining processor time, it may be satisfactory to operate the UNIVAC 1107 as just described. In other cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-card transcription of the report file. The curves for paired Configuration VIIIB show the time required for the all-tape main processing run in this case. The card-to-tape and tape-to-printer transcriptions will run at card reader and printer-limited speeds, and their demands on the processor will be small.

The master file record format is a mixture of alphameric and binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. (Even so, most of the central processor time is devoted to editing and radix conversion operations, using the manufacturer's standard subroutines.) A moderate degree of packing led to a record length of 18 words (or 108 6-bit characters).

SORTING (784:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the Users' Guide, Paragraph 4:200.213, using a three-way merge.

§ 201.

MATRIX INVERSION (784:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplication ($c = c + a_i b_j$) in single precision floating point (see Paragraph 784:051.422). Inversion times are shown for two cases: instructions and data in the same core storage bank, and instructions and data in alternate banks. The processor time required for a matrix inversion can be spread over a much longer total elapsed time when the inversion is multi-run with other programs that utilize the available input-output equipment. Multi-running of other programs necessarily decreases the amount of internal storage that can be allocated to the matrix inversion.

GENERALIZED MATHEMATICAL PROCESSING (784:201.4)

This problem measures over-all system performance on a simple mathematical application that involves widely varying ratios of input-to-computation-to-output volume, as described in Section 4:200.4 of the Users' Guide. As in the File Processing problem, the total elapsed time is shown by the solid lines in Graphs 784:201.414 and .415, while the central processor time is shown by the broken line marked "CP". (There is no separate "CP" line for Configuration VIIIB because the central processor time is the limiting factor in all cases, largely because of the time requirements for radix conversion of the input and output data.)

All computations are performed in single precision floating point. In Configurations VI and VIIA, input is via the on-line card reader and output is via the on-line printer. If card-to-tape and tape-to-printer transcriptions are carried out in separate runs, the time required for the all-tape main processing run can be read from the curves for paired Configuration VIIIB.

UNIVAC 1107 SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 1

Worksheet	Item		Configuration								Reference
			VI		VIIA		VIII B Files 3 & 4 Blocked		VIII B Files 3 & 4 Unblocked		
1 Input-Output-Times	Char/block	(File 1)	1,080		1,080		1,080		1,080		4:200.112
	Records/block	K (File 1)	10		10		10		10		
	msec/block	File 1= File 2	70.7		16.5		16.5		16.5		
		File 3	100.0		100.0		14.5†		8.2		
		File 4	142.0		142.0		18.5†		8.6		
	msec/switch	File 1= File 2									
		File 3									
		File 4									
	msec penalty	File 1= File 2	0.72		0.72		0.72		0.72		
		File 3	0.056		0.056		0.56		0.056		
		File 4	0.088		0.088		0.88		0.088		
2 Central Processor Times	msec/block	a1	0.08		0.08		0.08		0.08		4:200.1132
	msec/record	a2	0.12		0.12		0.12		0.12		
	msec/detail	b6	0.36		0.36		0.36		0.36		
	msec/work	b5 + b9	0.36		0.36		0.36		0.36		
	msec/report	b7 + b8	3.48		3.48		3.48		3.48		
3 Standard Problem A F = 1.0	msec/block for C.P. and dominant column.	a1	0.08		0.08		0.08		0.08		4:200.114
		a2 K	1.20		1.20		1.20		1.20		
		a3 K	42.00		42.00		42.00		42.00		
		File 1 Master In	0.72		0.72		0.72		0.72		
		File 2 Master Out	0.72		0.72		0.72		0.72		
		File 3 Details	0.56		0.56		0.56		0.56		
		File 4 Reports	0.88	1420.0	0.88	1420.0	0.88	18.5	0.88	86.0	
		Total	46.16	1420.0	46.16	1420.0	46.16	18.5	46.16	86.0	
4 Standard Problem A Space	Unit of measure	(36-bit words)									4:200.1151
		Std. routines ‡	8,192		8,192		8,192		8,192		
		Fixed	---		---		---		---		
		3 (Blocks 1 to 23)	189		189		189		189		
		6 (Blocks 24 to 48)	1,080		1,080		1,140		1,080		
		Files	792		792		1,440		792		
		Working	40		40		40		40		
		Total	10,293		10,293		11,001		10,293		

† Ten records per block in Files 3 & 4.
‡ 8,192 words are generally reserved for EXEC I.

UNIVAC 1107 SYSTEM PERFORMANCE (Contd.)

WORKSHEET DATA TABLE 2							
Worksheet	Item			Configuration			Reference
				VI & VIIA	VIIIB		
5	Fixed/Floating point			Floating	Floating		
	Unit name		input	card reader	Uniservo IIIA		
			output	Printer	Uniservo IIIA		
	Size of record		input	80 char. (1 card)	80 char.		
			output	128 char. (1 line)	128 char.		
Standard Mathematical Problem A	msec/block		input T1	100.0	8.2		4:200.413
			output T2	100.0	8.6		
	msec penalty		input T3	0.056	0.056		
			output T4	0.088	0.088		
	msec/record		T5	6.69	6.69		
	msec/5 loops		T6	1.12	1.12		
	msec/report		T7	7.52	7.52		
7	Unit name						
	Size of block						
	Records/block		B				
Standard Statistical Problem A	msec/block		T1				4:200.512
	msec penalty		T3				
	C.P.	msec/block	T5				
		msec/record	T6				
		msec/table	T7				

SYSTEM PERFORMANCE

§ 201.

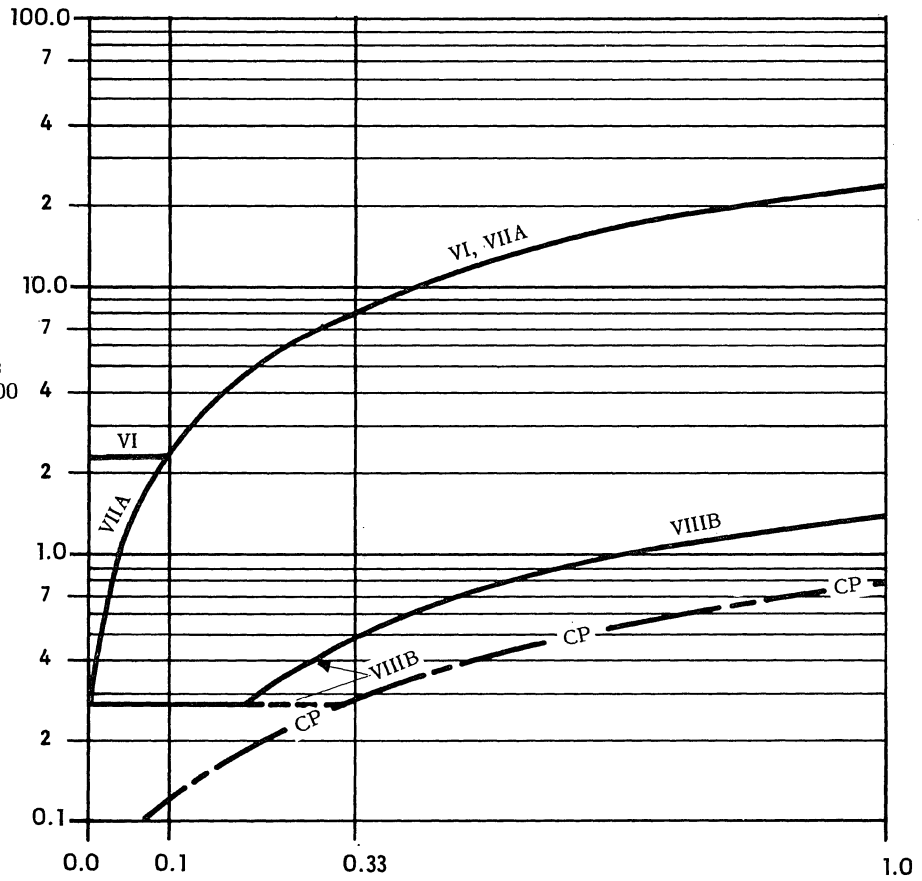
.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.
.112 Computation: . . . . . standard.
.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . . see graph below.
.115 Storage space required
Configuration VI: . . 10,300 words. *
Configuration VII A: . 10,300 words. *
Configuration VIII B (unblocked Files 3 & 4): . . . . 10,300 words. *
Configuration VIII B (blocked Files 3 & 4): . . . . 11,000 words. *

* includes 8,192 words reserved for EXEC I system.



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

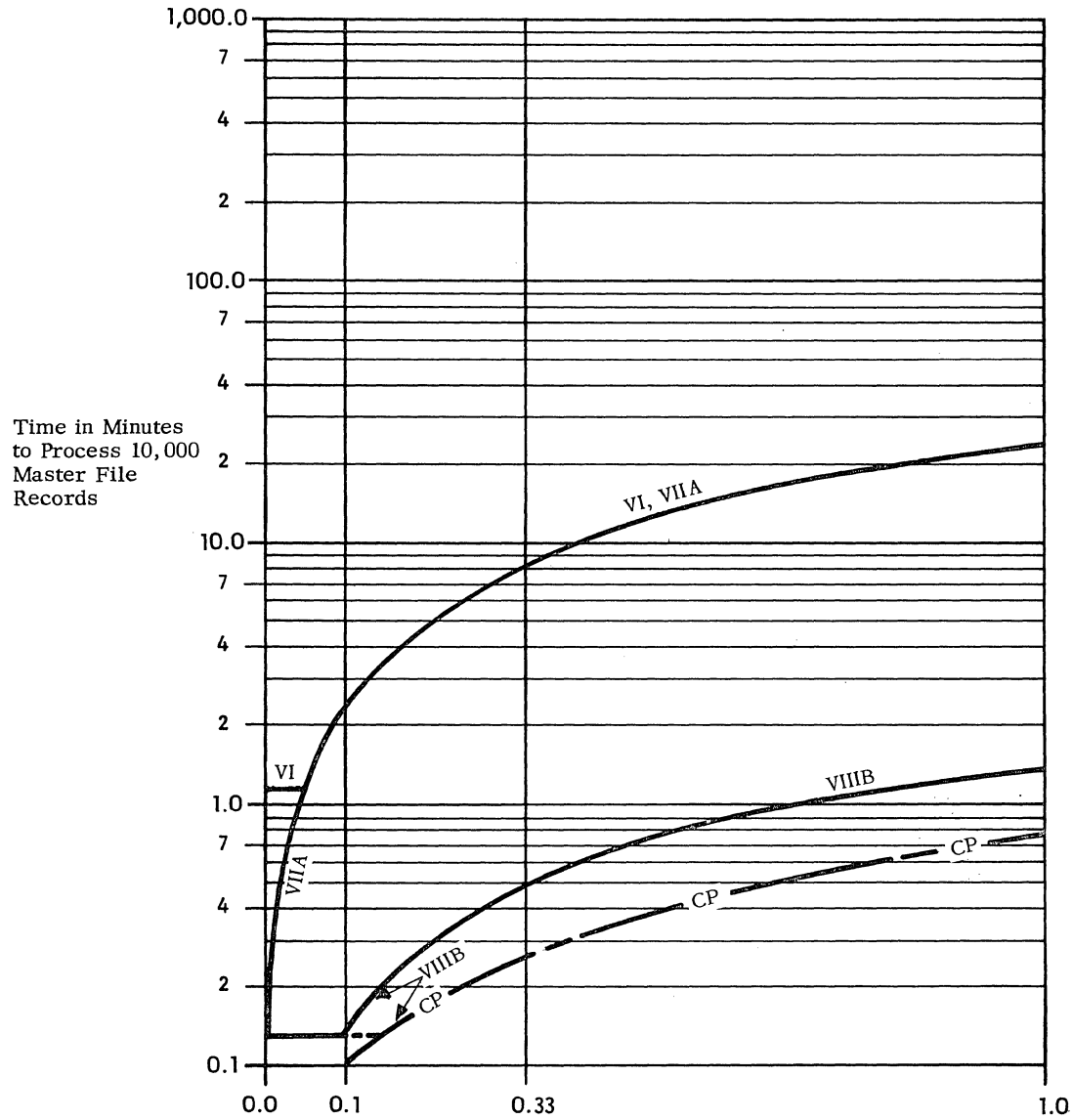
(Roman numerals denote standard System Configurations)

§ 201.

.12 Standard File Problem B

.121 Record sizes
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP — Central Processor time (all configurations)

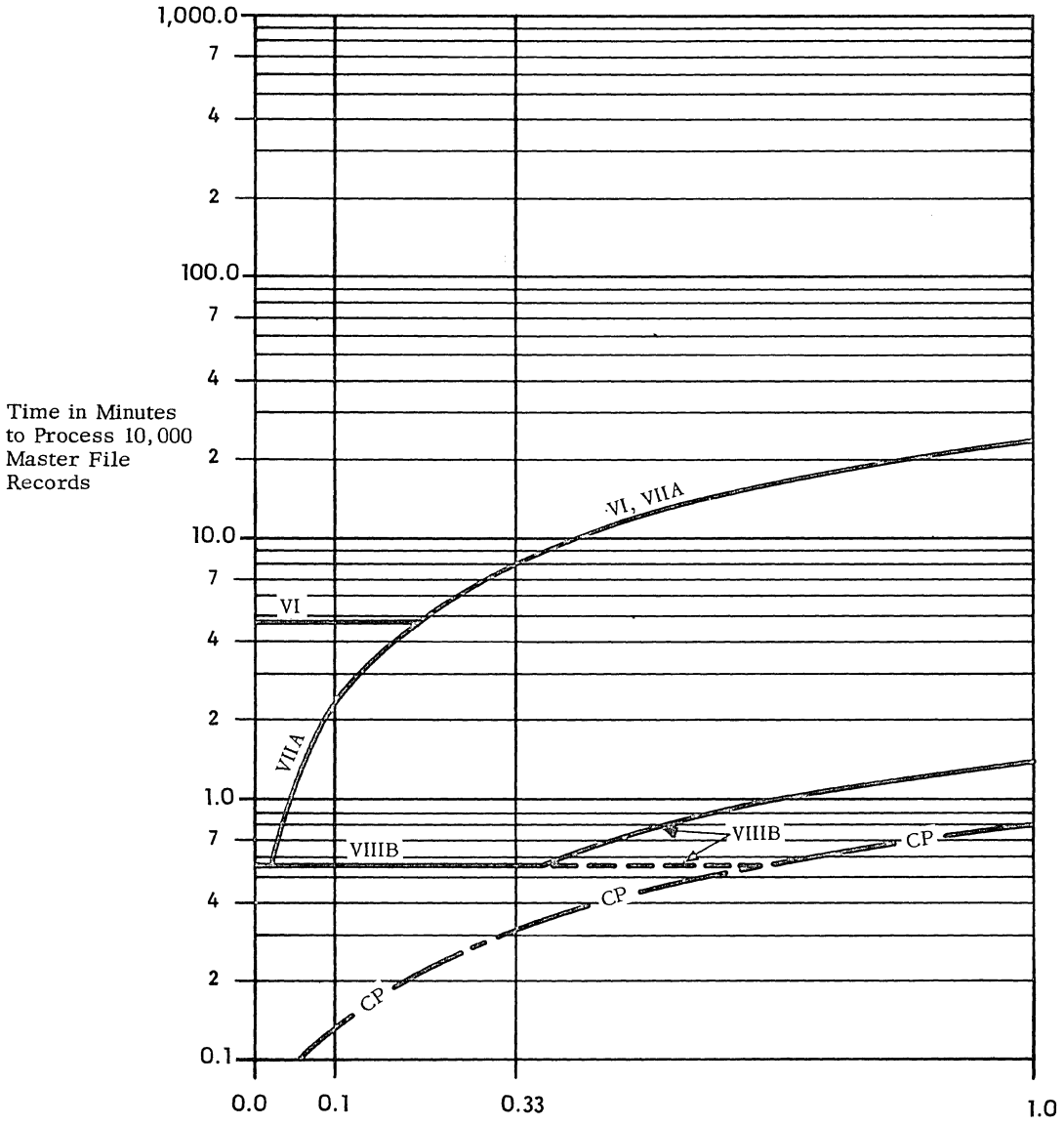
(Roman numerals denote standard System Configurations)

§ 201.

.13 Standard File Problem C

.131 Record sizes
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.



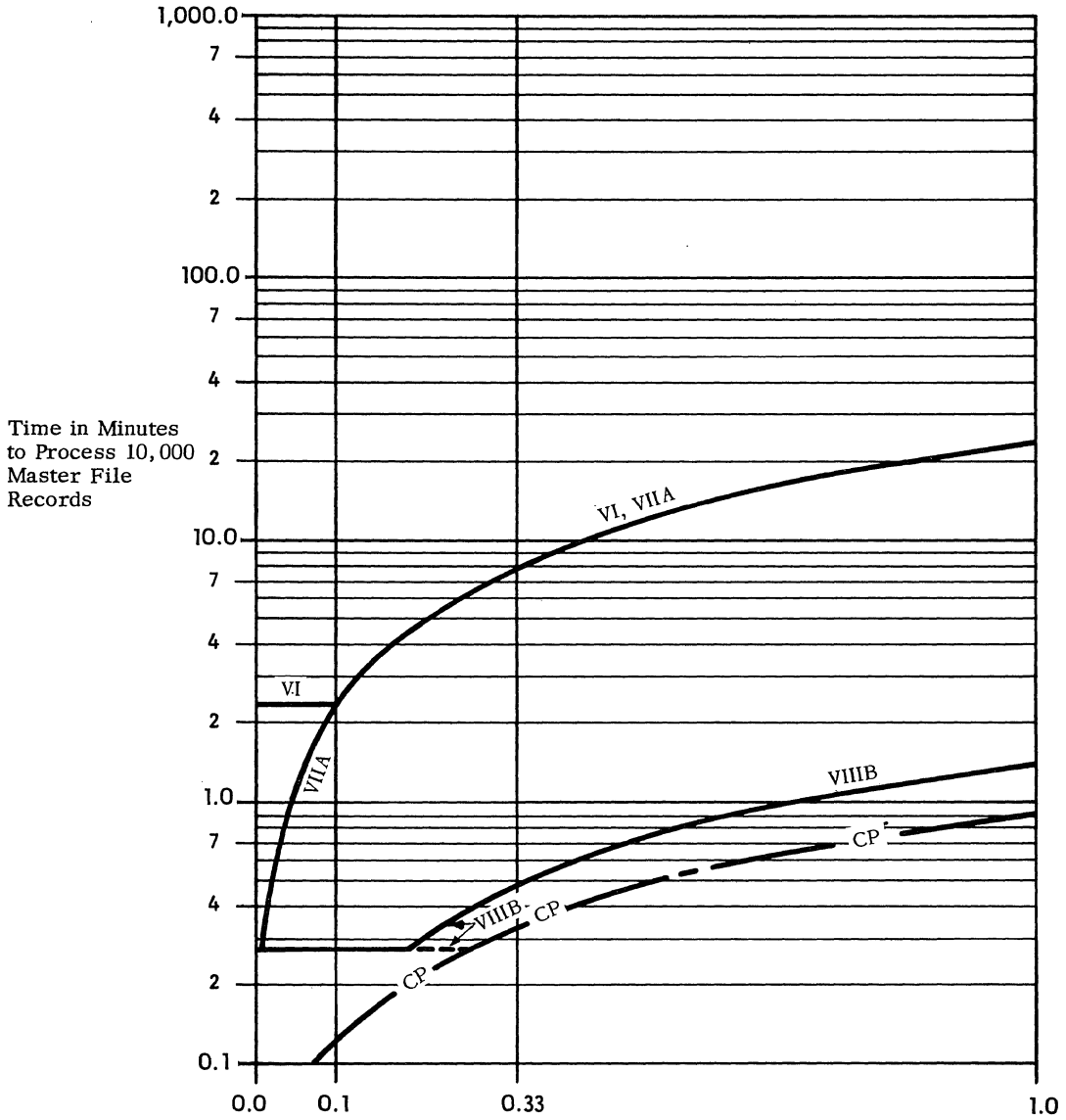
(Roman numerals denote standard System Configurations)

§ 201.

14. Standard File Problem D

.141 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations)

§ 201.

.2 SORTING

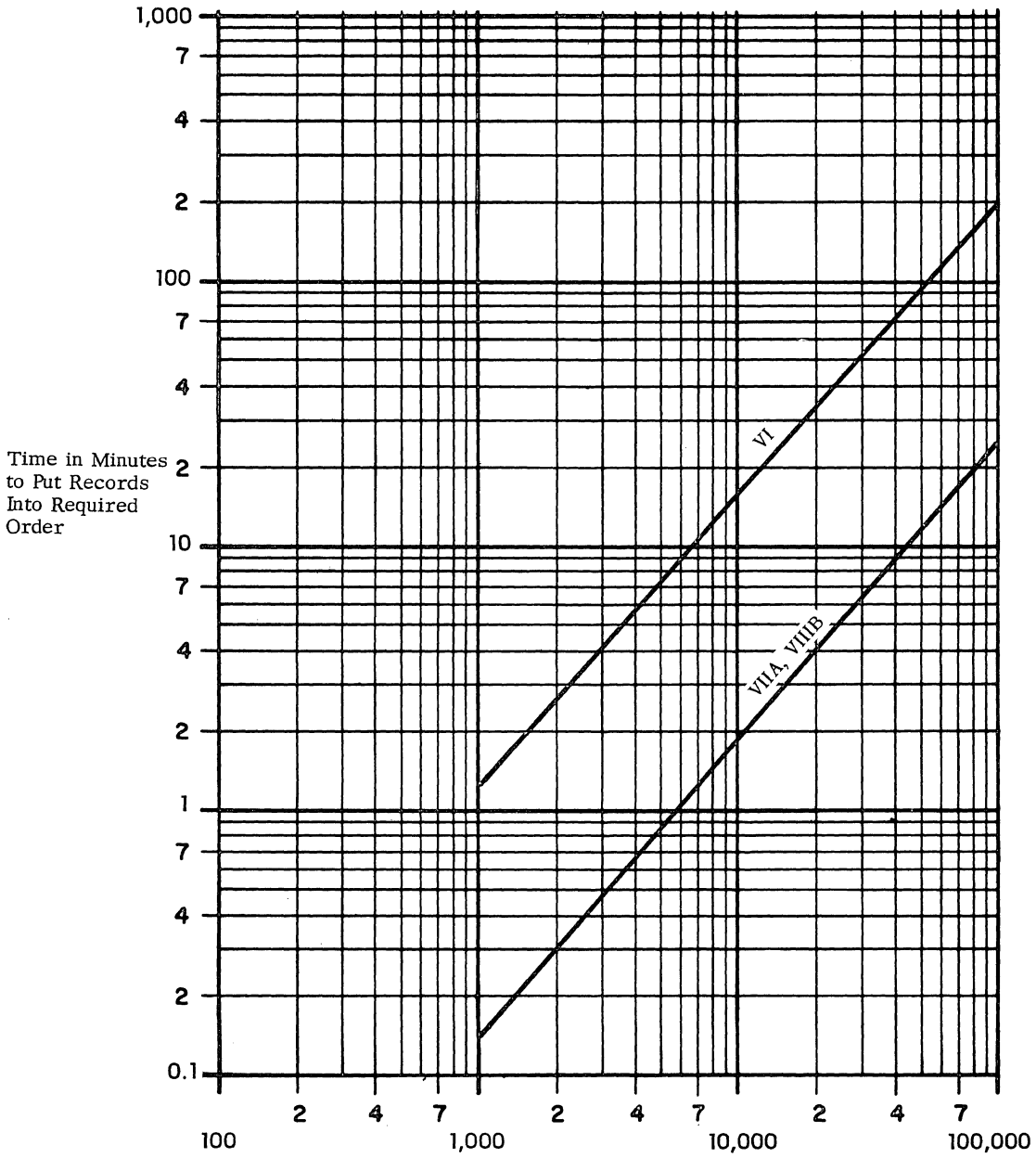
.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.

.212 Key size: . . . . . 8 characters.

.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . . see graph below, based upon 3-way merge.



§ 201.

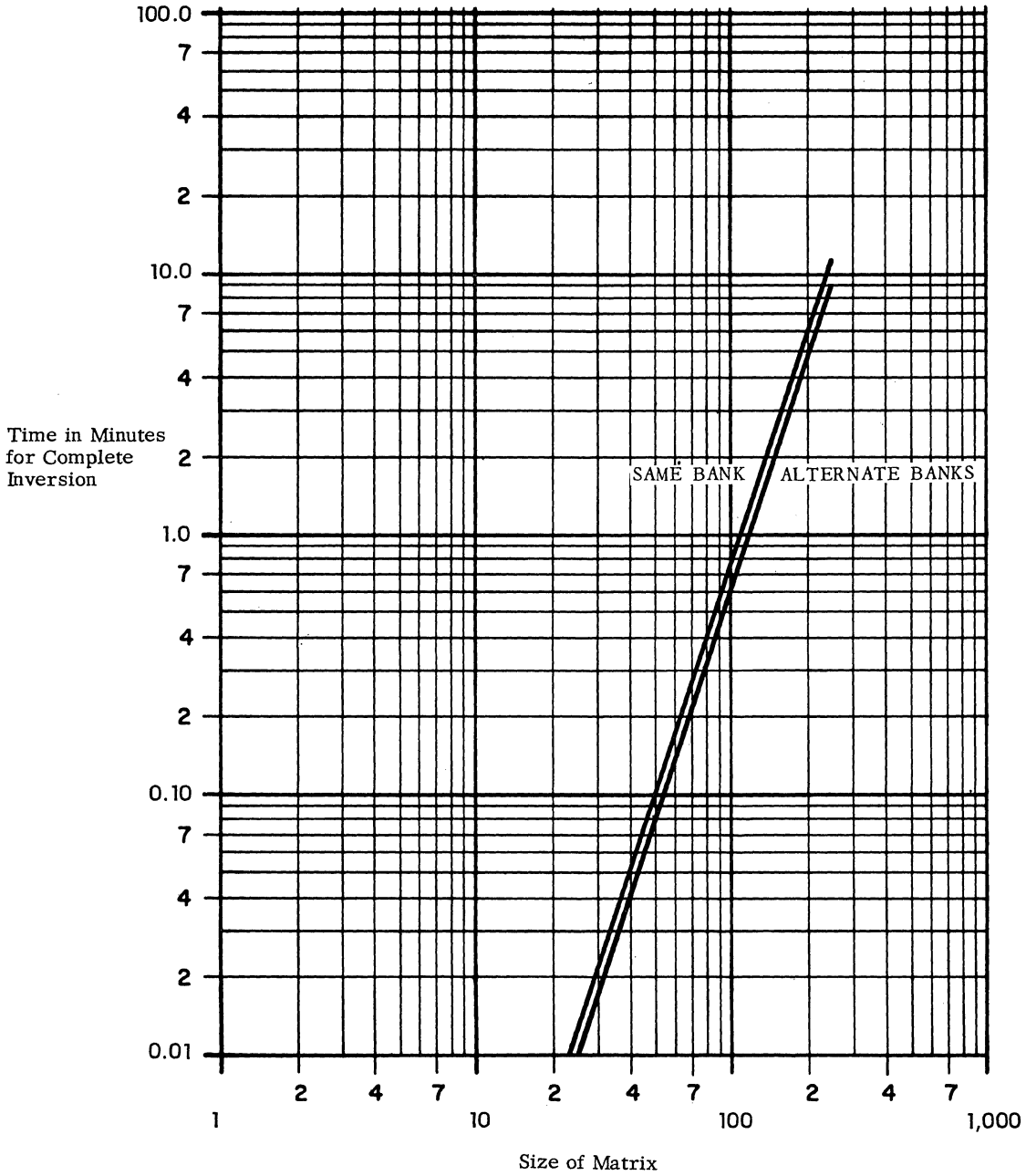
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to 8 decimal digits precision:

.312 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . . see graph below, showing times for instructions and data in the same core storage bank and in alternate banks.



§ 201.

.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

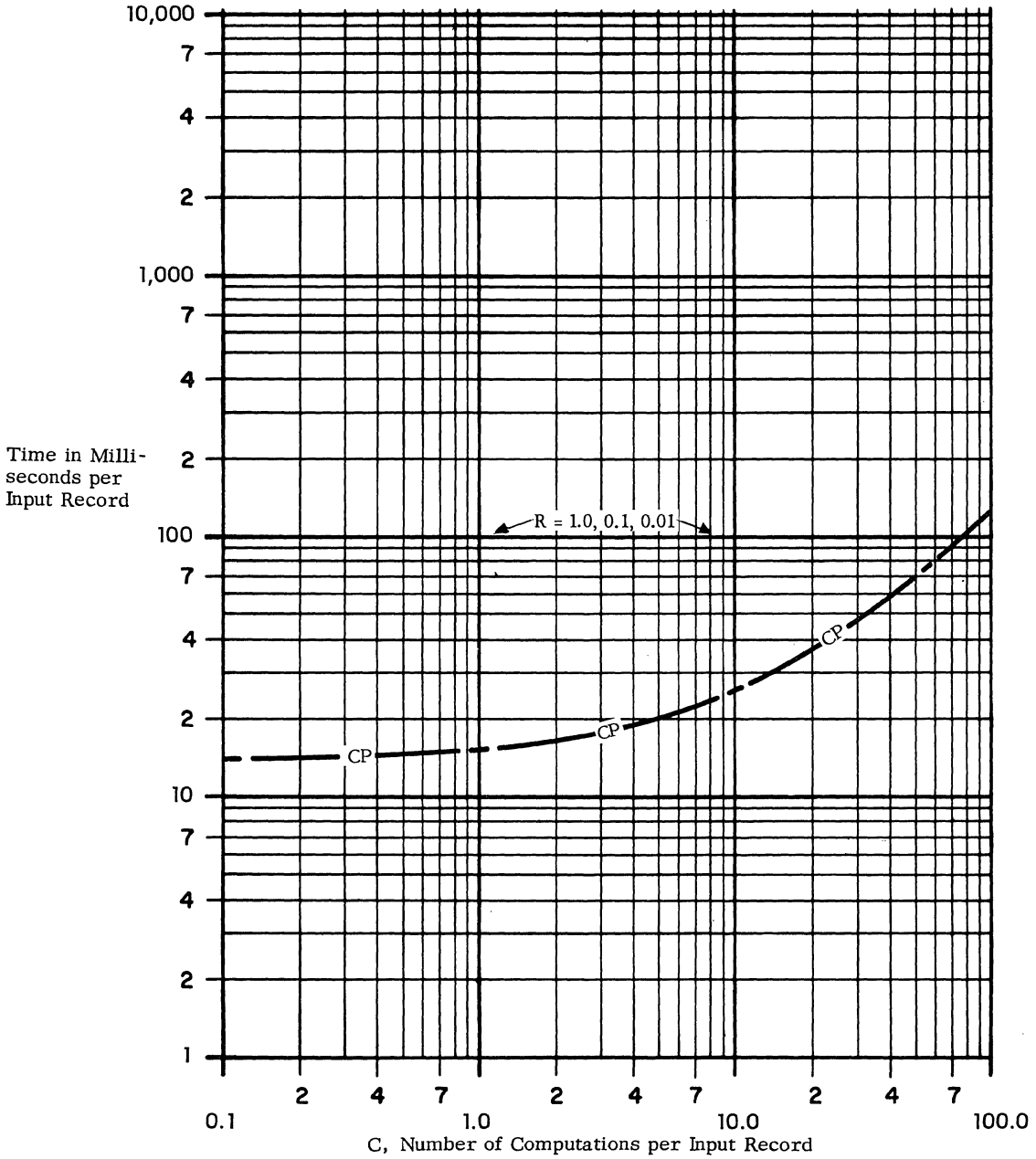
.412 Computation: . . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . . see graph below, for Standard Configurations VI and VII A. Input is via punched cards and output via on-line printer.

CONFIGURATIONS VI & VIIA; SINGLE LENGTH (8 DIGIT PRECISION); FLOATING POINT

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



LEGEND

Elapsed Time

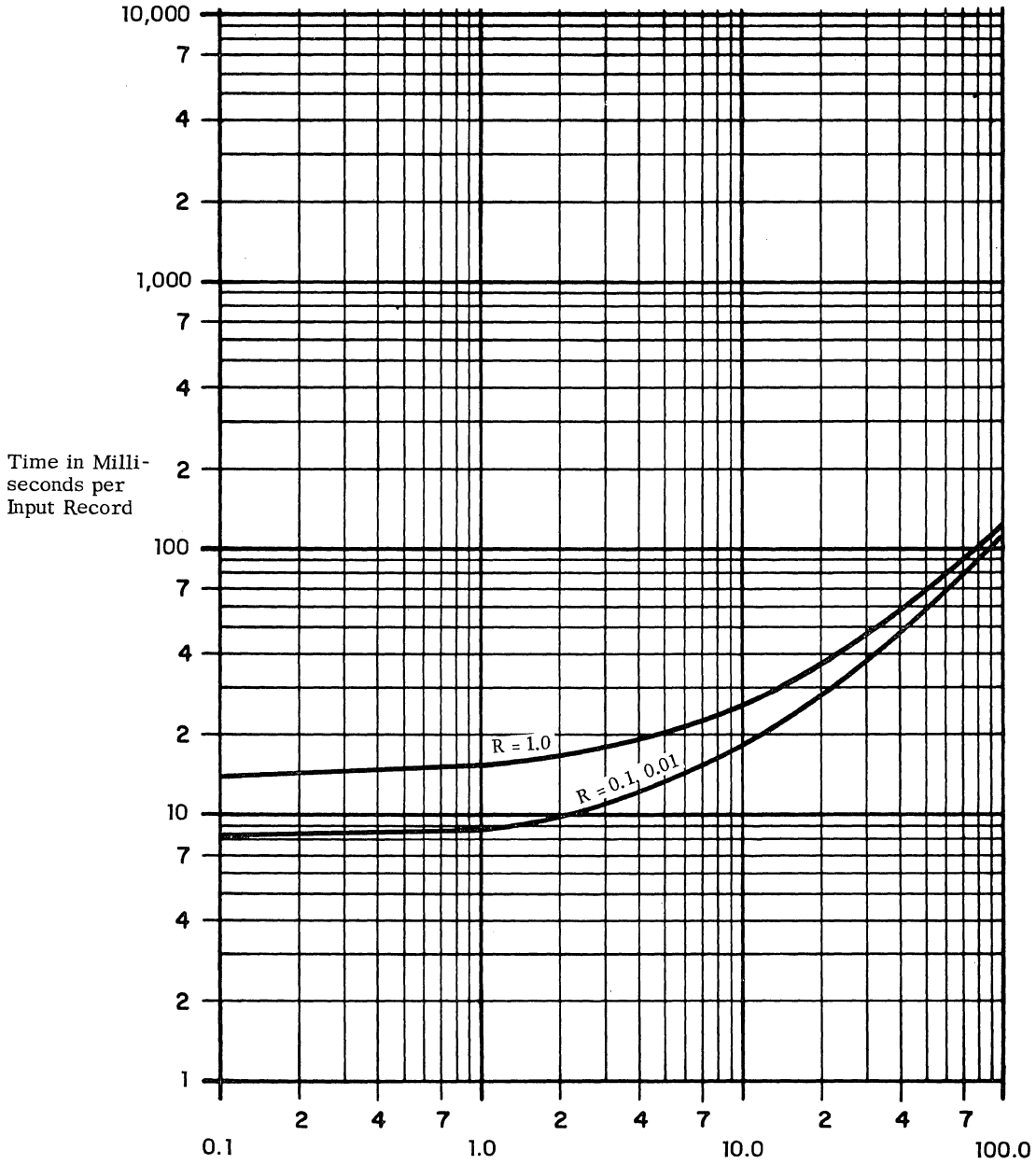
CP Central Processor time at R = 1.0

§ 201.

.415 Graph: . . . . . see graph below, for Standard Configuration VIII B. Input and output are via Uniservo III A Magnetic Tape Units.

CONFIGURATION VIIIB; SINGLE LENGTH (8 DIGIT PRECISION); FLOATING POINT

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



Note: Central Processor time equals total elapsed time in all cases for Configuration VIIIB.

UNIVAC 1107
PHYSICAL CHARACTERISTICS

UNIVAC 1107 PHYSICAL CHARACTERISTICS

IDENTITY	Unit Name		Central Computer		Power Control Cabinet	Control Console	Core Memory (16K, 1 Bank)		Core Memory (32K, 2 Bank)		Core Memory (49K, 2 Bank)		Core Memory (65K, 2 Bank)	
	Model Number		7200		---	---	7230		7232		7233		7234	
PHYSICAL	Height × Width × Depth, in.		96×74×35		96×48×35	var.×54×36	96×36×35		96×36×35		96×36×35		96×36×35	
	Weight, lbs.		1,850		800	450	1,500		1,500		1,500		1,500	
	Maximum Cable Lengths to Indicated Units, ft.		Core Memory: 25		Core Memory: 200 Central Computer: 30	Central Computer: 75								
ATMOSPHERE	Storage Ranges	Temperature, °F.												
		Humidity, %												
	Working Ranges	Temperature, °F.	←				60 to 80						→	
		Humidity, %	←				40 to 70						→	
	Heat Dissipated, BTU/hr.		13,800		600	1,400	9,600		9,600		19,200		19,200	
	Air Flow, cfm.		1,560		75	75	750		750		1,500		1,500	
	Internal Filters													
ELECTRICAL	Voltage	Nominal	208	208/120		208/120	208	208/120	208	208/120	208	208/120	208	208/120
		Tolerance	±1%	±10%		±10%	±1%	±10%	±1%	±10%	±1%	±10%	±1%	±10%
	Cycles	Nominal	384/440	60		60	384/440	60	384/440	60	384/440	60	384/440	60
		Tolerance	--	±0.5		±0.5	--	±0.5	--	±0.5	--	±0.5	--	±0.5
	Phases and Lines													
	Load KVA		3.8	1.4	---	0.49	1.8	1.6	2.1	1.6	4.0	1.6	4.2	1.6
NOTES	Where two types of power are shown for a unit, *both* are required.													

UNIVAC 1107 PHYSICAL CHARACTERISTICS (Contd.)

			Uniservo II A Tape Unit	Uniservo III A Tape Unit	Uniservo III C Tape Unit	Uniservo Control Unit	Uniservo Power Supply	Tape Adapter Cabinet	FH-880 Magnetic Drum	FH-880 Drum Control	Card Reader	Card Punch	Card Control Unit	High-Speed Printer	Printer Control Unit	Paper Tape Subsystem
IDENTITY	Unit Name		Uniservo II A Tape Unit	Uniservo III A Tape Unit	Uniservo III C Tape Unit	Uniservo Control Unit	Uniservo Power Supply	Tape Adapter Cabinet	FH-880 Magnetic Drum	FH-880 Drum Control	Card Reader	Card Punch	Card Control Unit	High-Speed Printer	Printer Control Unit	Paper Tape Subsystem
	Model Number		7242	7289	7236	7214, 8003, 7273	7290	7424	7432	7427	7223	7224, 7266	7240, 7277	7418	7239	7423
PHYSICAL	Height × Width × Depth, in.		69×31×31	63×31×30	63×31×30	96×20×35	96×66×35	63×36×30	96×54×35	96×20×35	49×51×27	53×49×27	96×20×35	53×72×32	96×20×35	96×24×35
	Weight, lbs.		745	745	745	625	2,800	800	1,300	625	750	800	625	1,613	625	800
	Maximum Cable Lengths to Indicated Units, ft.					Central Computer: 300 1st Uniservo: 80	1st Uniservo IIA: 60 1st Uniservo IIIA: 50 1st Uniservo IIIC: 50	Uniservo Power Supply: 85 Uniservo IIIC Control: 80	Drum Control: 60	Central Computer: 300	Card Control: 150	Card Control: 150	Central Computer: 300	Printer Control: 150		Central Computer: 300
ATMOSPHERE	Storage Ranges	Temperature, °F.														
		Humidity, %														
	Working Ranges	Temperature, °F.	←						60 to 80							→
		Humidity, %	←						40 to 70							→
	Heat Dissipated, BTU/hr.		7,140	7,480	7,480	2,075	10,200	2,400	5,125	1,640	3,440	4,075	2,600	12,000	2,600	3,000
	Air Flow, cfm.		300	350	350	390	2,300	600	300	390	200	200	390	500	390	300
	Internal Filters															
ELECTRICAL	Voltage	Nominal	208/120	208/120	208/120	208	208/120	208/120	208/120	208	208/120	208/120			208	208/120	208/120	208/120
		Tolerance	±10%	±10%	±10%	±1%	±10%	±10%	±10%	±1%	±10%	±10%			±1%	±1%	±1%	±1%
	Cycles	Nominal	60	60	60	384/440	60	60	60	384/440	60	384/440	60			384/440	60	60
		Tolerance	±0.5	±0.5	±0.5	--	±0.5	±0.5	±0.5	--	±0.5	--	±0.5			--	±0.5	±0.5
	Phases and Lines															
	Load KVA		2.63	2.75	2.75	0.6	0.35	3.8	1.25	0.5	2.1	0.5	0.35	---	---	0.7	3.15	---	0.4	5.2	1.5
NOTES											Power supplied by Card Control Unit.	Power supplied by Card Control Unit.		Power supplied by Printer Control Unit.		

PRICE DATA

§ 221.

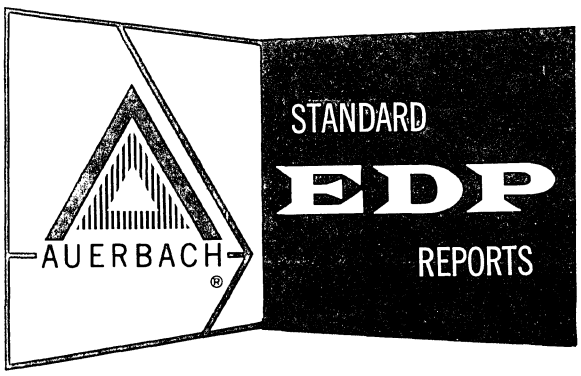
CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
Central Processor	7200	Central Computer (Includes Film Memory, Power Distribution Center, Motor Alternator, Console)	19,750	2,055	888,750
Internal Storage		Core Memory			
	7230	16,384 words - 1 bank	4,750	285	213,750
	7231	16,384 words - 2 banks	7,000	415	315,000
	7232	32,768 words - 2 banks	9,000	470	405,000
	7233	49,152 words - 2 banks	13,000	675	607,500
	7234	65,536 words - 2 banks	17,750	830	798,750
		FH-880 Magnetic Drum Subsystem			
	7432	FH-880 Drum	2,000	165	92,000
	7427	FH-880 Control & Synchronizer	1,440	165	72,000
		Fastrand Mass Storage Subsystem			
	8206	Fastrand Storage Unit	3,300	†	160,000
	7433	Fastrand Synchronizer	2,750	100	135,000
Input-Output		Uniservo IIA Subsystem			
	7242	Uniservo IIA Magnetic Tape Handler	450	95	20,000
	7214	Uniservo IIA Control & Synchronizer	1,550	130	77,500
	7290	Uniservo IIA Power Supply	550	40	25,300
		Uniservo IIIA Subsystem			
	7289	Uniservo IIIA Magnetic Tape Handler	750	155	36,500
	8003-08	Uniservo IIIA Control & Synchronizer (Single Channel)	3,800	170	182,400
	8003-11	Uniservo IIIA Control & Synchronizer (Dual Channel)	5,000	260	240,000
	7290	Uniservo IIIA Power Supply	550	40	25,330
		Uniservo IIIC Subsystem			
	7236	Uniservo IIIC Magnetic Tape Handler	800	62	38,400
	7424	Uniservo IIIC Tape Adapter Cabinet	1,000	52	48,000
	7273	Uniservo IIIC Control & Synchronizer	2,600	200	124,800
	7290	Uniservo IIIC Power Supply	550	40	25,300
		Punched Card Subsystem			
	7223	Card Reader (600 CPM)	350	75	17,500
	7224	Card Punch (150 CPM)	500	180	25,000
	7266	Card Punch (300 CPM)	1,150	295	57,500
	7240, 7277	Card Control & Synchronizer	1,850	230	83,250
		Paper Tape Subsystem (Paper tape reader, punch and control unit)	900	130	45,000
		High-Speed Printer Subsystem			
	7418	Printer (600 LPM)	500	130	25,000
	7239	Printer Control & Synchronizer (600 LPM)	1,550	140	77,500
	7400	Printer (700-922 LPM)	800	240	36,000
	7299	Printer Control & Synchronizer (700-922 LPM)	1,750	160	80,000

† $250 for first unit; $120 for each additional unit.

UNIVAC 1108

Univac

(A Division of Sperry Rand Corporation)



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UNIVAC 1108

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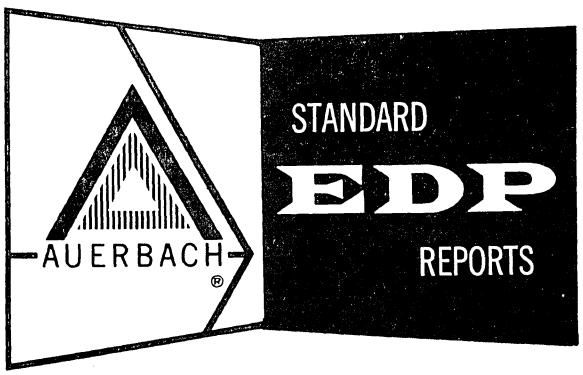

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CONTENTS

INTRODUCTION

.1 SUMMARY

The UNIVAC 1108 computer system is a large-scale data processing system, oriented toward both scientific and business applications, that features multiprogramming and multiprocessing capabilities for increased hardware utilization. Monthly rentals for typical single-processor 1108 configurations will generally fall in the $45,000 to $60,000 range. The cost of an 1108 system will typically be lower than that of an equivalent UNIVAC 1107 system — the 1108's predecessor in the UNIVAC line — despite the 1108's five-fold advantage in internal speeds. Typical multiple-processor configurations will rent for upwards of $100,000 per month.

The UNIVAC 1108 was originally announced in July 1964 as a faster, expanded version of the UNIVAC 1107 (see Computer System Report 784). Shortly afterward, UNIVAC stated that the development of multiple-processor hardware for the 1108 was under way. This hardware was first documented and described to prospective users in August 1965, but its official announcement was delayed until December 1965, when the multiple-processor version was introduced as the UNIVAC 1108-II. This, however, is only a marketing designation; the single-processor and multiple-processor versions of the 1108 use the same hardware components, and both versions are described in this report. The first single-processor 1108 system was delivered in December 1965, and the first multiple-processor configuration is expected to be delivered in the fourth quarter of 1966.

The 1108 is largely upward-compatible with the 1107, although existing 1107 programs will need to be reassembled or recompiled to run under control of the standard 1108 operating system. Most existing 1107 object programs can be run directly on an 1108 under control of a modified version of EXEC II, one of the standard operating systems for the 1107.

Chief extensions of the 1108 with respect to its predecessor, the 1107, include:

- Expanded core memory capacity — up to 262,144 36-bit words.
- Significantly faster core memory and internal processing speeds — basic cycle time is 0.75 microsecond.
- Double-precision fixed-point and floating-point arithmetic facilities.
- Greatly improved memory protection and addressing techniques.
- Provisions for I/O Controller units that can access memory independently of the Central Processor(s).
- Capability for up to five Central Processors and I/O Controllers to share a common core memory.
- Provisions for up to eight independent core memory modules.

UNIVAC has had several years of experience in multiprogramming (i.e., the capability to maintain two or more independent programs in core storage at the same time and to switch control among them to more fully utilize the hardware). This experience was gained with the UNIVAC III, 490, and 1107 computer systems. Many new features in the 1108, not found in other UNIVAC systems, are oriented toward optimizing the use of the hardware through multiprogramming.

.2 HARDWARE

.21 System Configuration

A single-processor 1108 configuration consists of one 1108 Central Processor with console and 8, 12, or 16 input-output channels; two, four, six, or eight 32,768-word modules of core memory (a maximum of 262,144 words); and peripheral subsystems as required. Tables I and II summarize the available subsystems and the number of input-output channels that each subsystem requires. The console also requires one input-output channel. In addition, up to four I/O Controller units, each having 4, 8, 12, or 16 input-output channels, can be included.

A multiprocessor (1108-II) configuration consists of up to five 1108 Central Processors and I/O Controllers in any combination; four, six, or eight 32,768-word modules of core memory (a maximum of 262,144 words); and peripheral subsystems as required. The input-output channels provided by the I/O Controllers are in addition to the Processor I/O channels.

.21 System Configuration (Contd.)

Normally, in a multiprocessor configuration, critical peripheral subsystems such as magnetic drums are connected to both an I/O Controller channel and a Processor channel to provide redundant data paths for increased reliability. Although up to five Central Processors can share the same core memory, the operating system being provided by UNIVAC for the 1108 will contain provisions for a maximum of three Processors and two I/O Controllers.

.22 Core Memory

Core memory can consist of up to 262,144 word locations in increments of 65,536 words. Each 36-bit word location can hold one instruction, one single-precision floating-point data item, from one to six fixed-point data fields, or six alphameric characters. Unlike the UNIVAC 1107, which has no checking provisions for data stored in core memory, the 1108 records a parity bit with each half-word of memory. Each 32,768-word module can be accessed independently.

The basic cycle time of the 1108's memory is 0.75 microsecond — over five times as fast as the 1107's 4-microsecond cycle. Like the 1107, the 1108 Central Processor can simultaneously access two different memory modules. If instructions and operands are stored in separate modules, the effective execution time for most instructions can be reduced by one memory cycle (0.75 microsecond). In all multiprocessor (1108-II) configurations, the physical address locations are interleaved within each pair of memory modules; the even locations are in one module and the odd locations in the other. Such interleaving reduces the frequency of conflicts when two Central Processors are executing programs which are physically located in the same memory modules.

.23 Control Memory

The 1108's Control Memory, which corresponds to the 1107's Thin-Film Memory, consists of 128 36-bit word locations. The Control Memory utilizes integrated circuits and has a cycle time of 0.125 microsecond. In the 1108, 70 of the 128 locations are reserved for use by supervisory routines; these reserved locations include a separate complete set of index registers, arithmetic registers, and control registers, as well as the Input/Output Access Control Registers. The 48 locations available to the user's program include 15 index registers, 16 arithmetic registers, and 4 control registers; the remaining 17 locations can be used by the programmer for intermediate storage. In both the reserved and user's area of Control Memory, four locations can be used as either index registers or arithmetic registers, permitting some unusual and powerful address modification operations.

.24 Central Processor

The UNIVAC 1108 Central Processor can perform fixed-point and floating-point arithmetic on one-word or two-word binary operands (although double-precision fixed-point arithmetic is limited to addition and subtraction). The 16 arithmetic registers, 15 index registers, a versatile repertoire of 7-part instructions, recursive indirect addressing, and a partial-word transfer facility permit efficient processing of most scientific problems. Commercial processing will be somewhat less efficient because the 1108, like the 1107, lacks automatic facilities for editing, decimal arithmetic, and radix conversions.

Although the 1108 uses a one-address instruction format, a limited two-address capability is provided by the fact that most instructions can specify the use of any one of the 16 arithmetic registers. The partial-word load and store instructions can transfer any half, third, or sixth of a word to or from the least significant bit positions of any arithmetic register. A wide variety of logical, shift, search, and block transfer operations can be performed. All instructions can be indexed, and each index register can be automatically incremented or decremented each time it is referenced. Indirect addresses can be "chained," and indexing can be performed upon each address in the chain. Straightforward programming of the UNIVAC 1108 is not unusually complex, but only skilled, highly-trained programmers will be able to take full advantage of the powerful optional elements offered in most instructions.

A program interrupt facility causes a transfer of control to one of 41 fixed core memory locations upon completion of an input-output operation, upon detection of a Processor or input-output error, or upon count-down to zero of the real-time clock (whose contents are decremented by 1 every millisecond). The interrupt facility permits full utilization of the Central Processor and all peripheral devices under the control of an integrated operating system that handles multiprogrammed operations.

Like other recent computer systems designed for multiprogramming, the 1108 Central Processor can operate in one of several modes which vary in the facilities they make available to the program.

In the Job Program mode, relative addressing is in effect; i.e., program addresses are modified by the contents of Basing Registers prior to all operations that require access to core memory. The upper and lower program address limits are specified by the contents of the Storage Limits Register. Any reference to the reserved set of registers in the Control Memory, any attempt to read or write into areas outside the program limits, or any

(Contd.)

.24 Central Processor (Contd.)

attempt to execute a reserved instruction results in an interrupt. The reserved instructions include loading of certain control registers and all input-output instructions. Most user's programs will be executed in the Job Program mode.

The Privileged mode is similar to the Job Program mode except that protection is provided only against writing, not against reading. Thus, programs stored in protected locations can be executed but cannot be overwritten.

In the Open mode, the complete facilities of the processor are available; there are no restrictions on the core locations that can be accessed or on the instructions that can be used, and relative addressing is not in effect. Normally, only the supervisory routines are allowed to operate in this mode.

.25 Peripheral Equipment

Three different magnetic drum units are available for use in 1108 systems. Two, the FH-432 and FH-1782, are rapid-access, word-addressable units designed to facilitate the rapid exchange of programs or routines between core storage and drum storage. One FH-432 drum subsystem with at least 786,000 words of storage is required for use of the standard operating system. The third drum storage unit, Fastrand II, is also used with several other UNIVAC computer systems. Fastrand II employs movable access mechanisms to provide somewhat slower access to much larger quantities of data than the head-per-track FH-432 and FH-1782 drums. A summary of the principal characteristics of each of these drum units is contained in Table I. Notably absent from the current UNIVAC line of random-access peripheral devices is a changeable-cartridge unit.

TABLE I: UNIVAC 1108 MAGNETIC DRUMS

Characteristic	FH-432	FH-1782	Fastrand II
Average access time, msec	4.25	17	92
Peak transfer rate, words/sec	240,000	240,000	25,625
Maximum storage per subsystem, 36-bit words	2,097,152	16,777,216	176,160,768
Maximum drum units per subsystem	9*	8*	8
Number of input-output channels per subsystem	1 or 2	1 or 2	1 or 2

* Up to 8 FH-432 and FH-1782 drum units, in any combination, can be connected to the same controller.

UNIVAC now offers only IBM-compatible magnetic tape units in the standard line of peripheral devices for the 1108. The characteristics of the Uniservo VIC and VIIIC Magnetic Tape Handlers are summarized in Table II. Both tape handlers are available in 9-track versions compatible with IBM's 2400 Series Magnetic Tape Units, as well as in the more common, IBM 729-compatible 7-track versions.

UNIVAC offers both multi-line and single-line controllers to serve as interfaces between an 1108 computer system and communications lines. The Communication Terminal Module Controller is capable of controlling up to 32 half-duplex or full-duplex narrow-band or voice-band lines. Various Communication Terminal Modules permit communications with remote terminals operating at up to 4,800 bits per second, synchronously or asynchronously, and utilizing transmission codes of up to eight levels. Up to four Communication Terminal Module Controllers can be included in a Communications Subsystem via a Scanner/Selector Unit; each Communications Subsystem fully occupies one 1108 input-output channel. All communications lines can be active simultaneously, subject to a maximum data rate of 51,000 characters per Communications Subsystem.

The Word Terminal Synchronous (WTS) and Communications Terminal Synchronous (CTS) are single-line controllers capable of controlling data communications over a single voice-band line at 2,000 or 2,400 bits per second, or over a broad-band line at 40,800 bits per second. Each Terminal fully occupies one 1108 input-output channel. The chief difference between the two Terminals is that the WTS transfers data in units of one 36-bit word between the 1108 and the controller, whereas the CTS transfers data in units of one character. With appropriate adapters or features, any of these communications controllers can operate over the public telephone network and can be equipped for unattended operation and automatic dialing.

TABLE II: UNIVAC 1108 INPUT-OUTPUT SUBSYSTEMS

Subsystem	Number of I/O Channels per Subsystem	Maximum Number of Devices per Subsystem	Peak Speed
Uniservo VIC Magnetic Tape	1 or 2	16	34,200 char/sec.
Uniservo VIIIC Magnetic Tape	1 or 2	16	96,000 char/sec.
Punched Card	1	1 reader; 1 punch	read 900 cpm; punch 300 cpm.
Printer	1	4	900 lpm.
Punched Paper Tape	1	1 reader; 1 punch	read 400 char/sec; punch 110 char/sec.
UNIVAC 1004	1	1	cards: read 615 cpm, punch 200 cpm; print 600 lpm; paper tape: read 400 char/sec, punch 110 char/sec; magnetic tape: 34,200 char/sec.
Communications (multi-line)	1	4 multiplexors, each serving up to 32 half- or full-duplex lines	4800 bits/sec per line; 51,000 char/sec total.
Communications (single-line)	1	1	40,800 bits/sec.

.25 Peripheral Equipment (Contd.)

The other peripheral devices available for use with an 1108 computer system are listed in Table II. In general, their performance is competitive but unexciting.

UNIVAC 1107 users who are installing an 1108 system can carry over the same magnetic drum and magnetic tape units they are currently using with the 1107. Specific provisions are included in the standard 1108 software for handling FH-880 Magnetic Drums and Uniservo IIA, IIIA, IIIC, and IVC Magnetic Tape Handlers, even though these 1107 peripheral units will not be actively marketed with the 1108.

.26 Simultaneous Operations

The 1108's capability for simultaneous operations is high. In addition to the overlapped operations of one or more Central Processors, all input-output channels in the Central Processors and I/O Controllers can be active simultaneously, subject to the peak data rate limitations of each channel and the associated Processor or I/O Controller. Each channel can handle a maximum of 250,000 data transfers per second; maximum capability of each Processor or I/O Controller is 1.33 million transfers per second. Most data transfers consist of one 36-bit binary word (or six 6-bit data characters), in which case each Processor or I/O Controller can handle up to 8 million characters per second. Some peripheral units, such as the Punched Paper Tape Subsystem, Communications Subsystem, and Communications Terminal Synchronous, transfer only one character per data transfer. In general, only one core storage cycle is required for each data transfer.

.3 SOFTWARE

.31 Interim Software

Prior to delivery of the full 1108 software package, as outlined in Paragraph .32, UNIVAC is supplying 1108 users with a slightly modified version of the "B" Software Package for the 1107. The principal components of this package are:

- EXEC II — an operating system designed to monitor the compilation and execution of programs, maximize utilization of the available hardware, and minimize operator intervention. The system utilizes a

(Contd.)

.31 Interim Software (Contd.)

magnetic drum as a high-capacity buffer store to keep the card readers, punches, and printers fully occupied and as a fast-access auxiliary store for program segments. An integrated set of diagnostic aids and library maintenance facilities is included. One notable characteristic of EXEC II is its lack of facilities for true multiprogramming; concurrent program execution is limited to one main program plus multiple data transcriptions.

- SLEUTH II — a symbolic assembly system, with macro-instruction facilities, that translates symbolic source programs into relocatable machine-language object programs.
- COBOL — a compiler for COBOL-61 source programs that operates under control of EXEC II. Language facilities include nearly all of Required COBOL-61 (there are a few minor deficiencies); several COBOL-61 electives (but not the very useful COMPUTE verb); a MONITOR verb (which provides dynamic printouts of the values of specified items); and a SORT facility (but not the one defined as part of Extended COBOL-61). A magnetic drum is required for COBOL compilations, but magnetic tape is not.
- FORTRAN — a compiler for FORTRAN IV source programs that operates under control of EXEC II. Language facilities are largely compatible with those of FORTRAN IV as defined for the IBM 7090/7094. FORTRAN II source programs can be converted to FORTRAN IV by means of a LIFT Translator. The FORTRAN compiler achieves high compilation speeds through use of a magnetic drum.
- SORT II — a generalized sort/merge routine that operates under control of EXEC II.

With this software, the 1108 will, in effect, perform as an 1107 which is over five times as fast internally as the original 1107, and with peripheral performance as determined by the 1108's configuration. UNIVAC states that the majority of 1107 object programs can be executed directly by an 1108 under control of the modified EXEC II system. Significant exceptions include some 1107 FORTRAN and COBOL programs, because the 1107 FORTRAN and COBOL compilers used "illegal operation code" interrupts to provide entries into certain standard functions. Such programs would not, in general, be executed properly by an 1108.

The "B" Software Package for the 1107 was developed by Computer Sciences Corporation and is serving as a foundation for the 1108 software development program. UNIVAC states that certain portions of the standard 1108 software package described below, including 1108 COBOL, 1108 FORTRAN V, and 1108 SORT/MERGE, will be capable of operation on an 1108 under control of the modified EXEC II operating system.

.32 1108 Software

The chief component of the standard software being prepared for the 1108 is the 1108 Executive System, a comprehensive operating system designed to control all activities of an 1108 installation. The software support package for the 1108 will include an assembler, compilers for COBOL, FORTRAN, and ALGOL, and several useful application programs. The scheduled delivery date for the full 1108 software package is the third quarter of 1966. Most 1108 software, with the exception of the Executive System, will be similar to, or direct extensions of, 1107 software. Programs written for an 1107 will, in general, need to be recompiled or reassembled on an 1108 in order to run under supervision of the 1108 Executive System.

The 1108 Executive System is a comprehensive group of routines designed to control all activities of an 1108 computer system, including job scheduling, hardware allocation, I/O control, and run supervision in both a multiprogramming and a multiprocessing environment. Other facilities provided by the Executive System include library facilities, I/O control, file control, automatic writing of checkpoints, and segmentation.

The Executive System is designed to recognize three types or levels of processing: real-time, demand, and batch. Real-time processing is characterized by the need for a computer response to an external event quickly enough to achieve a desired goal. Real-time processing is normally, but not exclusively, associated with data communications or process control applications where delay in obtaining computer time could result in lost data or process malfunctions. Demand processing is typified by the need for "conversation" between the computer and the user; i.e., the user will specify the execution of certain tasks dependent on the results of previously-initiated tasks. Batch processing is the normal execution of independent tasks (programs) or groups of tasks that are not highly time-dependent. The order of priority for scheduling and execution, in descending order, is real-time, demand, and batch.

.32 1108 Software (Contd.)

The principal orientation of the Executive System is toward maximizing the throughput of batch operations while providing facilities for handling useful amounts of real-time and demand processing. The type of processing is specified in the control statements initiating a run, and sometimes within each task of a run (i.e., the type of processing can vary for each task within a run).

Program areas are protected from the actions of another program (except for I/O operations) by hardware provisions, under control of the Executive. Protection of program areas from the input-output operations of other programs is accomplished through software checks.

The Executive System can be utilized on any 1108 configuration incorporating at least 786,000 words of FH-432 Magnetic Drum storage. The Executive System contains provisions for handling any 1108 configuration that includes up to three Central Processors and two I/O Controllers. The minimum resident core storage requirement is 10,000 words.

The other major items in the software support package for the 1108, which operate under control of the Executive System, include:

- 1108 Assembler — a symbolic assembly system that is virtually identical with SLEUTH II for the 1107 (see Paragraph .31), with additional mnemonics for the new 1108 instructions.
- 1108 COBOL — a compiler for programs written in COBOL-61. Language facilities include those of Required COBOL-61, except for a few minor deficiencies, and many COBOL-61 electives, including the COMPUTE verb and the extended version of the SORT verb.
- 1108 FORTRAN — a compiler for programs written in a language that UNIVAC calls "FORTRAN V." The language facilities represent significant extensions of FORTRAN IV as implemented for the 1107, including provisions to facilitate the writing and deletion of debug statements, to assign types implicitly according to the first letters of variable names, and to utilize any peripheral device (including remote terminals) for input and output. The 1108 FORTRAN V language includes, as proper subsets, all the language facilities of 1107 FORTRAN IV, IBM 7090/7094 FORTRAN IV, and the proposed A.S.A. FORTRAN language. FORTRAN II source programs can be accommodated through use of the LIFT translator; LIFT converts the source-language statements into 1107 FORTRAN IV statements, which can then be compiled by the 1108 FORTRAN V compiler. Two distinct versions of the FORTRAN V compiler will be furnished for the 1108. One is a fast, efficient compiler for batch programs. The second is a "conversational mode" compiler for servicing users at remote terminals who desire statement-by-statement program execution.
- ALGOL — a compiler for programs written in ALGOL 60. UNIVAC states that the language facilities will conform to the ACM and GAMM committee specifications.
- 1108 SORT/MERGE — a generalized subroutine used in conjunction with a series of parameter lists to produce sort programs. The complete program specifications can be entered via the control stream or incorporated as part of a larger program. Magnetic drum storage can be utilized to speed sorting.

Application packages being developed for the 1108 include linear programming, PERT/COST, APT III (for computer-assisted programming of numerically-controlled machine tools), and BEEF (an extensive series of subroutines developed by Westinghouse Electric Corporation's Baltimore Defense and Space Center to enhance FORTRAN's limited capabilities for data manipulation and to augment its capabilities as a scientific processing language).

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	36 bits	basic addressable storage unit in core storage, control registers, and FH-432 or FH-1782 drum storage.
Field:	6, 12, or 18 bits	an integral portion of a word, addressable by field definition in certain 1108 instructions.
Row (Uniservo VIC or VIIIC):	7 bits (6 data, 1 parity)	magnetic tape; holds 1 character.
Sector:	28 words	basic addressable storage unit in Fastrand drum storage.
Band:	64 sectors	Fastrand storage.

.2 DATA FORMATS

Type of Information	Representation
Instruction:	1 word.
Fixed-point binary number (short):	1 word.
Fixed-point binary number (long):	2 words.
Floating-point binary number (short):	1 word: 27-bit fraction, 8-bit exponent, and 1 sign bit.
Floating-point binary number (long):	2 words: 60-bit fraction 11-bit exponent, and 1 sign bit.
Alphameric character:	6-bit portion of a word.

SYSTEM CONFIGURATION

A UNIVAC 1108 computer system is a highly flexible system consisting of:

- Central Processor(s).
- Console(s).
- Main Memory module(s).
- Input/Output Control unit(s) (optional with a single-processor system).
- Magnetic Drum Subsystem (required by standard software).
- Various peripheral subsystems.

Central Processor

The basic 1108 Central Processor contains provisions for up to 16 input-output channels and for addressing up to 262,143 words of main (core) memory. Adapters permit multiple Central Processors to share main memory and peripheral subsystems. The basic processor includes a console; auxiliary consoles are available.

Main Memory

From one to four "banks" of main memory can be incorporated in a UNIVAC 1108 computer system. Each bank consists of two independent modules, and each module contains 32,768 36-bit words of core storage. Thus, a fully-expanded main memory would consist of eight modules (262,144 words), all of which can be accessed simultaneously. Multiple Module Access Units (MMA) allow the core storage to be shared by any combination of up to five Central Processors and Input-Output Controllers. One MMA unit is required for each bank of storage. These units provide five connections and permit up to eight modules of memory to be accessed simultaneously by multiple processors and/or Input-Output Controllers. (Each processor is capable of making two simultaneous accesses to different modules.)

Input/Output Controller

The Input/Output Controller (I/OC) is an independent wired-logic processor that provides independent data paths between up to 16 single-channel or 8 dual-channel peripheral subsystems and Main Memory via one connection of each Multiple Module Access Unit associated with Main Memory. Each Controller can be controlled by up to three 1108 Central Processors. Each I/OC contains 256 36-bit words (Index memory) for storage of the I/O control words. The Index memory is expandable to 512 words. The input/output channels provided by the I/OC are in addition to the channels provided by the basic Central Processor.

Magnetic Drum Subsystem

Use of the standard software provided for the UNIVAC 1108 requires an FH-432 Magnetic Drum Subsystem with at least 786,432 words of storage (3 drums).

Peripheral Subsystems

The peripheral subsystems available for a UNIVAC 1108 computer system are listed in Table I; the reference column defines the section within this report where additional information can be found concerning each subsystem. Each single-channel subsystem requires the full use of one input-output channel of an 1108 Central Processor or Input/Output Controller; each dual-channel subsystem requires two channels. The subsystems that can have the dual-channel capability are identified in Table I. Up to four consoles for each processor can be connectd to one input/output channel of the processor and can operate simultaneously; additional consoles for each processor can be connected via the Communication Subsystem. A peripheral subsystem can be shared among up to four Central Processors and/or Input/Output Controllers by means of a Multi-Processor Adapter (MPA). A dual-channel subsystem requires two Adapters for shared use.

Single-Processor Systems

The minimum single-processor configuration in which all components of the 1108 Executive System (see page 785:191.100) are operable includes:

- Central Processor with console and eight input/output channels;
- One bank of Main Memory (65,536 words);
- Three FH-432 Magnetic Drums (786,432 words);

(Contd.)

- Printer, card reader, and card punch (can be provided via a UNIVAC 1004 II or III); and
- Two magnetic tape units (Uniservo VIC or VIIIC).

Multiple-Processor (1108-II) Systems

The UNIVAC 1108 Executive System contains provisions for handling an 1108 multiprocessor system containing up to three 1108 Central Processors and up to two Input/Output Controllers. The minimum amount of core storage required is 131,072 words (two banks). The minimum peripheral requirements are the same as for the Single-Processor System.

UNIVAC 1107 Peripherals

All of the peripheral devices available with the UNIVAC 1107 can be used with an 1108 system. These units are not offered as a standard part of the 1108 line, but they may be carried over from a previous UNIVAC installation or obtained from UNIVAC, depending on the availability of returns. The 1108 Executive System contains specific provisions for handling the following 1107 peripheral devices: Uniservo IIA, IIIA, IIIC, and IVC Magnetic Tape Units, and FH-880 Magnetic Drum.

Standard Configurations

Standard Configurations VIIA and VIIIA (as defined in Section 4:030, System Configuration, of the Users' Guide) are shown for the UNIVAC 1108 in the following diagrams. These integrated configurations were chosen instead of the paired configurations (VIIB and VIIIB) because of the 1108's capability for multiprogramming. This capability permits data transcription runs to be carried out simultaneously with the associated main processing runs or other runs, thus providing virtually the same effective performance as when the data transcriptions are performed off-line, as in a paired configuration. (See the System Performance section, beginning on page 785:201.100.)

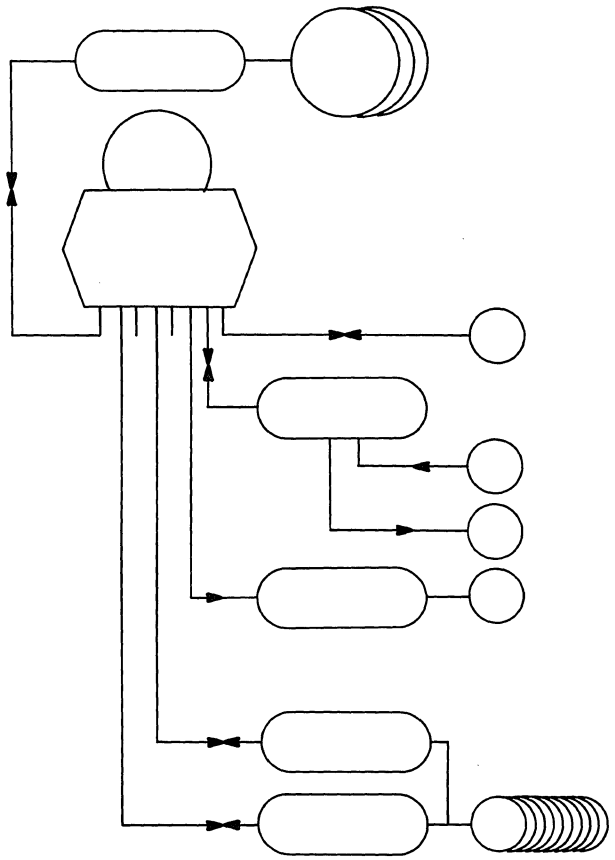
In addition, a typical multiprocessor 1108 configuration is shown on page 785:031.300. A system of this type is intended for use where large amounts of processing power and on-line file storage are required. The addition of communications equipment to this configuration would enable the central system to serve remote users.

TABLE I: UNIVAC 1108 PERIPHERAL SUBSYSTEMS

Subsystem	Reference
Punched Card Subsystem — 900 cpm (read); 300 cpm (punch)	785:071
High Speed Printer Subsystem — up to 4 printers; 700/922 lpm	785:081
Punched Paper Tape Subsystem — 400 cps (read); 110 cps (punch)	785:072
UNIVAC 1004 I, II, or III (read and punch cards, print, and read and write magnetic tape)	785:101
Single- or Dual-Channel Magnetic Tape Subsystem — 1 to 16 Uniservo VIC or VIIIC magnetic tape units; 8,500 to 96,000 char/sec	785:091
Single- or Dual-Channel Magnetic Drum Subsystem— up to 9 FH-432 drums (262,144 words/drum, 4.25 msec average access time); up to 8 FH-1732 drums (2,097,152 words/drum, 17 msec average access time); or any combination of FH-432 and FH-1782 drums not exceeding a total of 8 drums per subsystem	785:042, 785:043
Single- or Dual-Channel Mass Storage Subsystem — up to 8 Fastrand II Storage Units (22,020,096 words/unit; 92 msec average access time)	785:044
Communication Subsystem — controls up to 128 half- or full-duplex communications lines operating at up to 4,800 bits/sec	785:102
Data Communication Terminal — controls data communications over the public telephone network, a leased voice-band line, or a broad-band facility at 2,000, 2,400, or 40,800 bits/sec, respectively	785:102
Console with Keyboard and Typewriter	785:061

.1 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . . magnetic drum is required for standard software.
core memory is 220% larger.
magnetic tape is 60% faster.
printer is up to 84% faster.
card reader is 80% faster.

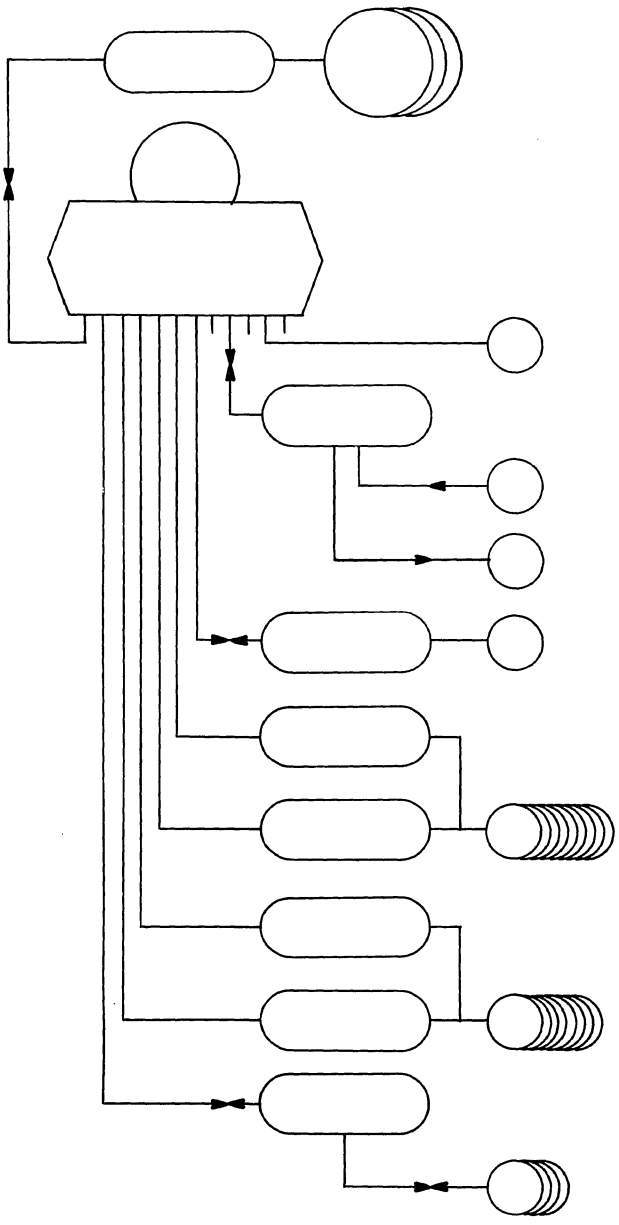


Equipment	Rental
FH-432 Magnetic Drum Subsystem (includes 3 drums and synchronizer; 786,432 words)	$ 5,000
Core Memory: 65,536 36-bit words (2 modules)	10,000
Central Processor (includes 8 I/O channels)	15,500
Console	
Card Control & Synchronizer	750
Card Reader: 900 cards/min	380
Card Punch: 300 cards/min	665
Printer & Synchronizer: 922 lines/min	1,550
Uniservo VIIIC Control & Synchronizer	1,450
Uniservo VIIIC Auxiliary Control & Synchronizer	1,450
Uniservo VIIIC 7-channel Tape Units — Simultaneous (10): 96,000 char/sec	8,500
TOTAL RENTAL:	$45,245

(Contd.)

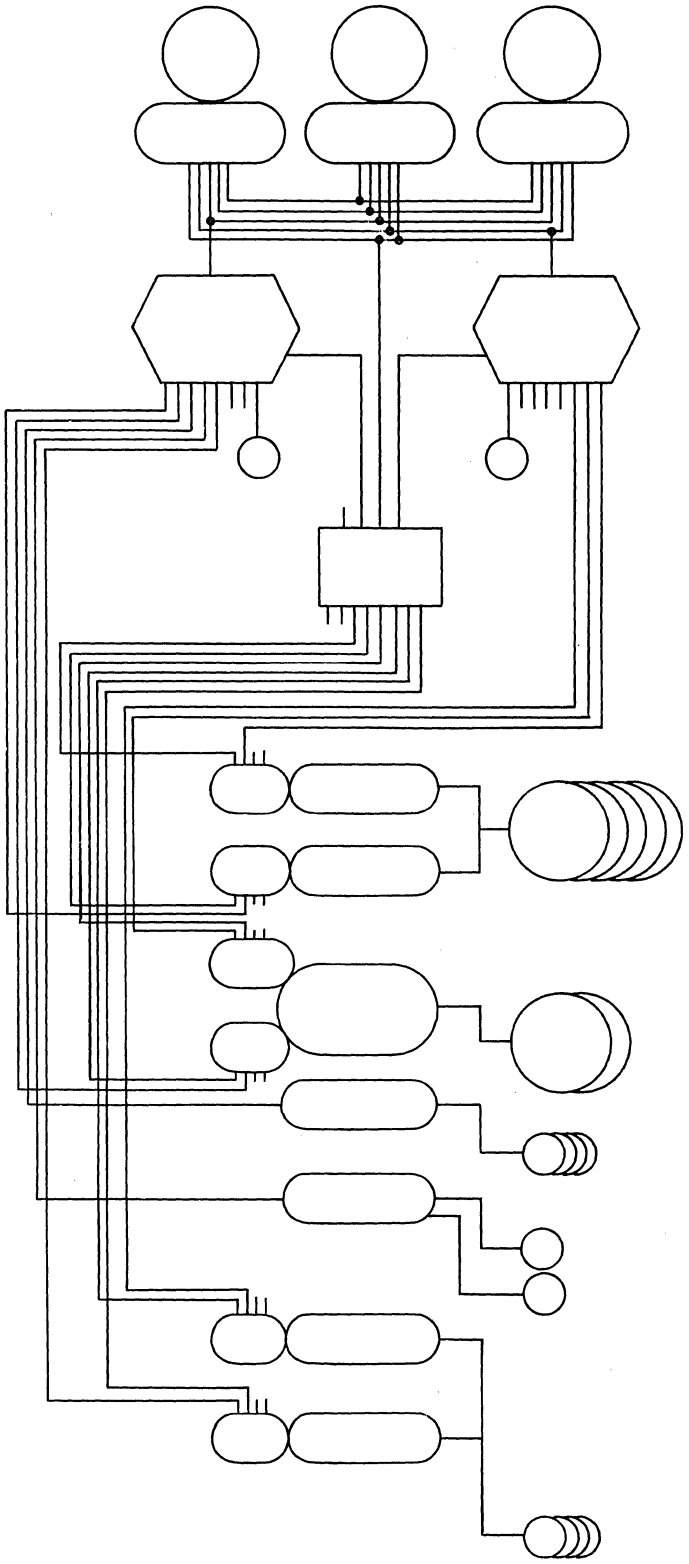
.2 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: . . . . . magnetic drum is required for standard software.
core memory is 62% larger.
magnetic tape is 20% slower.
card punch is 50% faster.



Equipment	Rental
FH-432 Magnetic Drum Subsystem (includes 3 drums and Synchronizer; 786,432 words)	$ 5,000
Core Memory: 65,536 36-bit words (2 modules)	10,000
Central Processor (includes 12 I/O channels)	16,000
Console	
Card Control & Synchronizer	750
Card Reader: 900 cards/min	380
Card Punch: 300 cards/min	665
Printer & Synchronizer: 922 lines/min	1,550
Uniservo VIIIC Control & Synchronizer, and Auxiliary Control & Synchronizer	2,900
Uniservo VIIIC 7-channel Tape Units — Simultaneous (8): 96,000 char/sec	6,800
Uniservo VIIIC Control & Synchronizer, and Auxiliary Control & Synchronizer	2,900
Uniservo VIIIC 7-channel Tape Units — Simultaneous (8): 96,000 char/sec	6,800
Uniservo VIIIC Control and Synchronizer	1,450
Uniservo VIIIC 7-channel Tape Units — Non-Simultaneous (4): 96,000 char/sec	3,200
TOTAL RENTAL:	$58,395

.3 TYPICAL MULTIPROCESSOR CONFIGURATION



Equipment	Rental
Core Memory: 196,608 words (includes 3 Multiple Module Access Units)	$32,205
Central Processors and Consoles (2)	31,000
Input/Output Controller (includes 8 input-output channels)	4,500
Magnetic Drum Subsystem (includes two Drum Control and Synchronizer Units, three FH-432 Drums: 786,432 words; two FH-1782 Drums: 4.2 million words; and two Multiple Processor Adapters)	7,835*
Fastrand Dual Channel Control and Synchronizer (includes 2 Multiple Processor Adapters)	3,235
Fastrand II Storage Unit (2): 44 million words	7,600
Printer Control and Synchronizer	NA
Printer (4): 922 lines/min	3,200
Card Control and Synchronizer	750
Card Reader: 900 cards/min	380
Card Punch: 300 cards/min	665
Uniservo VIIIC Control and Synchronizer; Uniservo VIIIC Auxiliary Control and Synchronizer (includes 2 Multiple Processor Adapters)	3,735
Uniservo VIIIC 7-channel Tape Units — Simultaneous (2): 96,000 char/sec	1,700
Uniservo VIC Master 7-channel Tape Unit — Simultaneous (1) and Slave Tape Unit (1): 34,200 char/sec	850
TOTAL RENTAL: Approximately	$100,000

* Price of FH-1782 Drums is not included because it has not been specified to date.

INTERNAL STORAGE: CORE MEMORY

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 Core Memory.

.12 Basic Use: . . . . . working storage.

.13 Description

Core Memory for the 1108 can consist of two, four, six, or eight modules of 32,768 36-bit words each. Each module is independent; i.e., in a fully-expanded memory system of eight modules, up to eight memory references can be made at the same time. One pair of memory modules is the smallest amount of core storage available. The following memory sizes are available:

Number of Modules	Word Locations
2	65,536
4*	131,072*
6	196,608
8	262,144

The cycle time is 0.75 microsecond per access of one 36-bit word. By storing instructions in one module and data in another, the effective storage cycle time can be reduced to 0.375 microsecond. This "alternate bank" storage allocation decreases the overall execution time for most instructions by 0.75 microsecond. Each 1108 memory module is functionally similar to a UNIVAC 1107 memory bank.

Each 36-bit word location can hold one instruction, one floating-point data item, from one to six fixed-point data items, or six alphameric characters. Block transfer operations from one area of Core Memory to another can transfer full words or either half (18 bits), any third (12 bits), or any sixth (6 bits) of successive word locations at a peak rate of 667,000 words per second. Successive source addresses can be N words apart and successive destination addresses M words apart, with N not necessarily equal to M.

Unlike the 1107, the 1108 contains provisions for checking the accuracy of data transfers to and from core storage. One parity bit is recorded for each half of a 36-bit word when writing and checked when reading.

As in the 1107, the 128 lowest-order locations of 1108 Core Memory are "hidden." Their addresses (000_8 through 177_8) are the same as those of Control Memory, and they can be accessed only by indirect addressing, by jump instructions, or by input-output operations. All other instructions refer to the correspondingly numbered locations in Control Memory. The "hidden" core locations are therefore protected from internal write operations, but not from input-output operations; the converse applies to all of Control Memory. To minimize confusion between the contents of Control and "hidden" memory, the safest policy is to avoid program references to the core locations below address 177_8. (See Paragraph 785:051.12 for a discussion of the Control Memory.) The "hidden" memory is normally used for "bootstrap" operations.

Two types of memory protection are provided, depending on the setting of designator bits within the Processor State Register. Memory areas not allocated to a program can be protected against writing only, or against reading, writing, and branching. The Storage Limits Register contains the upper and lower addressing limits of both the instruction area and the data area; memory can be allocated in blocks of 512 words. See Paragraph 785:051.122 for a more detailed discussion of the memory protection features of the 1108.

In a multiprocessor (1108-II) configuration, or in a single-processor configuration which also contains an I/O Controller, multiple connections to core memory are required to gain the advantages of simultaneous references to several memory modules. This capability is furnished by the Multiple Module Access Unit (MMA). An MMA enables up to five Central Processors or I/O Controllers, in any combination, to be connected to one pair of memory modules. One MMA is required for each pair of memory modules (each 65,536 words).

In a single-processor 1108 configuration containing two or four modules, memory locations are numbered sequentially within a module. In all multiprocessor 1108 configurations, and in single-processor 1108 configurations containing six or eight memory modules, memory locations are interleaved within each pair of modules on an odd and even basis. This feature reduces the memory conflicts when two processors or I/O Controllers are working in the same area of core storage. See Paragraph 785:051.122 for a more detailed discussion of the performance of multiprocessor configurations.

The 48 reserved core locations with addresses 200_8 through 247_8 are assigned for the specific purposes shown in Table I.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . December 1965.

.16 Reserved Storage

Purpose	Number of Locations	Locks
Index registers:	0*	
Arithmetic registers:	0*	
Logic registers:	0*	
Interrupt control:	48	only via programming.
"Hidden" memory:	128	protected from internal write operations.

* In Control Memory; see Section 785:051.

* Minimum memory requirement for a multiprocessor configuration (1108-II).

TABLE I: RESERVED CORE MEMORY LOCATIONS

Purpose	Number of Locations	Octal Addresses
Reserved	14	200-215
Day Clock and Interrupt	2	216-217
Input Monitor Interrupt	1	220
Output Monitor Interrupt	1	221
Function Monitor Interrupt	1	222
External Interrupt	1	223
ESI Input Monitor Interrupt	1	224
ESI Output Monitor Interrupt	1	225
Power Loss Interrupt	1	226
ESI External Interrupt	1	227
Status Word for External Interrupt	1	230
Real-Time Clock Interrupt	1	231
External Synchronous Interrupt #1, 2	2	232-233
Main Storage Parity Error, Modules #1-4	4	234-237
Control Register Parity Error	1	240
Illegal Instruction Interrupt	1	241
Executive Return Interrupt	1	242
Guard Mode Interrupt	1	243
Not Used	1	244
Floating-Point Underflow Interrupt	1	245
Floating-Point Overflow Interrupt	1	246
Divide Fault Interrupt	1	247

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.23 Storage Phenomenon: . direction of magnetization.

.29 Potential Transfer Rates

.292 Peak data rates —
Cycling rates: . . . . . up to 1,333,000 cps per module.
Unit of data: . . . . . one 36-bit word.
Gain factor: . . . . . 2 to 8 modules.
Data rate: . . . . . 1,333,000 words/sec per module.
Compound data rate: . 2,667,000 to 10,668,000 words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see table below.

.4 CONTROLLER: . . . . no separate controller.

.5 ACCESS TIMING

.52 Simultaneous Operations: . . . . . access to each module is asynchronous and independent of other modules.

.53 Access Time Parameters and Variations

.531 For uniform access (each module) —
Access time: . . . . . 0.375 μsec.
Cycle time: . . . . . 0.75 μsec.
For data unit of: . . . 1 word.

Note: When instructions are stored in one module and operands in another, effective cycle time approaches a minimum of 0.375 μsec for a pair of modules.

.7 PERFORMANCE

.72 Transfer Load Size

With self: . . . . . 1 to N full or partial words; N limited by storage capacity.

.73 Effective Transfer Rate

With self: . . . . . 667,000 words/sec (up to 4,000,000 char/sec.)

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	none.	
Invalid code:	all codes valid.	
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Timing conflicts:	check	resolved automatically by priority control network.

.31 Module and System Sizes

	Minimum* Storage			Maximum Storage
Modules:	2	4	6	8
Words:	65,536	131,072	196,608	262,144
Characters:	393,216	786,432	1,179,648	1,572,864
Instructions:	65,536	131,072	196,608	262,144

* The minumum storage required for a multiprocessor (1108-II) configuration is 131,072 words (4 modules).

INTERNAL STORAGE: FH-432 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 432 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

One of the important considerations in a multiprogramming environment is a system's ability to rapidly unload and reload individual program segments from auxiliary storage. The Flying Head 432 Magnetic Drum is an auxiliary storage device that provides the ability to load an entire 32,768-word UNIVAC 1108 memory module in approximately 140 milliseconds, including average access time. (The FH-1782 Magnetic Drum described in Section 785:043 provides a much greater on-line storage capacity than the FH-432 and can transfer data at the same peak rate, but the FH-1782 Drum has an average access time four times that of the FH-432 Drum.)

The standard operating system for the 1108 (see page 785:191.100) requires a minimum of 786,000 words of FH-432 Magnetic Drum storage (3 drums).

A Magnetic Drum subsystem consists of a single- or dual-channel controller and:

- From three to nine FH-432 Drum Units, or
- From one to eight FH-1782 Drum Units, or
- Any combination of up to eight FH-432 and FH-1782 Drum Units.

The FH-432 and FH-1782 utilize the same Drum Control and Synchronizer Unit. The dual-channel capability allows simultaneous read/read, read/write, or write/write operations on any two drum units in a subsystem.

Each FH-432 drum has a storage capacity of 262,144 36-bit words. Maximum potential storage capacity is therefore 2,359,296 words (14,155,776 characters) per subsystem. The drum revolution speed of the FH-432 is 7,100 revolutions per minute, providing an average access time of 4.25 milliseconds. The peak data transfer rate is 240,000 words per second. This rate is accomplished by reading and writing in parallel from 3 staggered bit-serial tracks. An interlace factor of 2, 4, 8, or 16 is available which reduces the data transfer rate to 120,000, 60,000, 30,000, or 15,000 words per second, respectively. There are 128 three-track bands per drum unit. The remaining 48 tracks are used for spares, for recording parity check bits, and for timing functions.

A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired.

The control logic of a Magnetic Drum Subsystem enables the program to interrogate individual drum units to determine the storage location that is currently under the read-write heads. The Drum Input/Output Handler routine can then select from the subsystem queue the data request that can be serviced most quickly. Utilization of this capability will typically increase the time required to obtain a particular block of data but will reduce the overall average access time; i.e., increase the "throughput."

A manual switch inhibits writing in the first 2,048 word locations of drum storage. Any attempt to write into this area results in an interrupt.

Checking includes a parity check to ensure that each word read from the drum has odd parity, a character count to ensure that each word transferred to or from the drum consists of exactly six characters, and checks for invalid drum addresses and function codes. Detection of any drum causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Processor a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . December 1965.

.16 Reserved Storage: . . . 48 of the 432 tracks are reserved for spares, parity, and timing functions. A manual switch allows the first 2,048 words to be protected from write operations.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter: . . . . . 10.5 inches.
Length: . . . . . 9.0 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.

.242 Data regenerated constantly: . . . . . no.

.243 Data volatile: . . . . . no.

.244 Data permanent: . . . . no.

.245 Storage changeable: . . no.

.25 Data Volume Per Band of 3 Tracks

Words: . . . . . 2,048.
Characters: . . . . . 12,288.
Instructions: . . . . . 2,048.

.26 Bands per Physical Unit: . . . . . 128.

.27 Interleaving Levels: . . 1, 2, 4, 8, or 16.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically-supported head per track.

.283 Type of access —

Description of stage	Possible starting stage
Switch bands:	when different band is selected (or at end of band).
Wait for specified sector:	when previously-selected band is used.
Read or write 1 to 65,535 words:	when rotational delay is zero.

.29 Potential Transfer Rates

.291 Peak bit rates —

Cycling rates: . . . . . 7,100 rpm.
Track/head speed: . . 3,950 inches/sec.
Bits/inch/track: . . . 687.
Bit rate per track: . . 2,880,000 bits/sec.

.292 Peak data rates —

Unit of data: . . . . . word.
Conversion factor: . . 36 bits per word.
Gain factor: . . . . . 3 tracks per band.
Loss factor: . . . . . interlace factors of 2, 4, 8, or 16 are optional.

Data rate:

Interlace option	Words/sec	Char/sec
1	240,000	1,440,000
2	120,000	720,000
4	60,000	360,000
8	30,000	180,000
16	15,000	90,000

.3 DATA CAPACITY

.31 Module and System Sizes (FH-432 Drums only)

	Minimum Storage	Maximum per Subsystem
Drums:	3	9
Words:	786,432	2,359,296
Characters:	4,718,592	14,155,776
Instructions:	786,432	2,359,296

.32 Rules for Combining Modules: . . . . . 3 to 9 FH-432 Drum Units, or 1 to 8 FH-1782 Drum Units, or 1 to 8 FH-432 and FH-1782 Drum Units (in any combination) per Magnetic Drum Subsystem.

.4 CONTROLLER

.41 Identity: . . . . . FH-432/1782 Drum Control and Synchronizer Unit, Single or Dual Channel.

.42 Connection to System: . 1 controller per Magnetic Drum Subsystem. Each subsystem fully occupies 1 or 2 input-output channels.

.43 Connection to Device: . 3 to 9 FH-432 Drum Units per controller; see also Paragraph .32.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 65,535 words.
.442 Input-output area: . . . . core memory.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization: . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads: one fixed head serves each track.

.52 Simultaneous Operations: . . . . . maximum of 1 read, write, or search operation per Single-Channel Subsystem; maximum of two read, write, or search operations (in any combination, but must occur on different drum units) per Dual-Channel Subsystem.

.53 Access Time Parameters and Variations

Stage	Variation, msec	Average, msec
Switch bands:	0 or 0.04	—
Wait for specified sector:	0 to 8.5	4.25
Read or write:	(see Paragraph .292)	

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size: . . 1 to 65,535 words.

.73 Effective Transfer Rate (with Core Memory)

Interlace option	Words/sec	Char/sec
1	237,000	1,422,000
2	120,000	720,000
4	60,000	360,000
8	30,000	180,000
16	15,000	90,000

.74 Update Cycle Rate: . . . 46.3 references/second, based on random accessing of one 84-character record; reading, updating, and writing that record; and rereading for verification of recording. An interlace option of 1 is assumed.

.75 Read-Only Reference Rate: . . . . . 217 references/second, based on random accessing of one 84-character record, with no updating or rewriting. An interlace option of 1 is assumed.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bits.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit	interrupt.
Reference to locked area:	check	interrupt.

INTERNAL STORAGE: FH-1782 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 1782 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 1782 Magnetic Drum is similar to UNIVAC's earlier FH-880 drum (Section 784:043) but offers well over twice the storage capacity. The FH-1782's greater capacity is achieved partly by an increase in the number of tracks (to 1760) and partly by an increase in the recording density (to 780 bits per inch). The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the drum rotating at 1,770 revolutions per minute.

The FH-1782 Magnetic Drum can use the same Control and Synchronizer Unit as the FH-432 Drum (see Section 785:042). The optional dual-channel capability allows simultaneous read/read, read/write, or write/write operations on any two drum units in a subsystem. A Magnetic Drum Subsystem consists of a single-channel or dual-channel controller and:

- From three to nine FH-432 Drum Units, or
- From one to eight FH-1782 Drum Units, or
- Any combination of up to eight FH-432 and FH-1782 Drum Units.

Each FH-1782 drum has a storage capacity of 2,097,152 words of 36 bits each. Maximum potential storage capacity is therefore 16,778,216 words per subsystem.

Of the 1,760 tracks on each FH-1782 drum, 1,536 are grouped into 256 data bands of six tracks each. The other 224 tracks are used for parity checking, timing, reference, and as spares. Each UNIVAC 1108 word is converted by the Synchronizer into six 6-bit characters. The six tracks in each data band are read and recorded in parallel, and each word is stored in a six-by-six matrix of bit positions. An odd parity bit is generated for each word and recorded in a corresponding location in one of 64 parity tracks.

Peak data transfer rate is 240,000 words or 1,440,000 characters per second. An interlace factor of 2, 4, 8, or 16 is available to decrease the transfer rate by the corresponding factor. From 1 to 65,535 words can be transferred in a single operation.

A general explanation of how input-output operations are handled in the 1108, including demands on the system, can be found in Section 785:111, Simultaneous Operations.

A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired.

A new function has been incorporated in the control logic of the FH-432 and FH-1782 subsystems to reduce overall storage access times. This function enables the program to interrogate a particular drum unit to determine which storage locations are currently under the read-write heads. The Drum Input-Output Handler routine can then select from the subsystem queue the data request that can be serviced fastest.

Writing can be inhibited in increments of 8,192 word locations by manual switches. Any attempt to write in a locked-out area results in an interrupt.

Checking includes a parity check to ensure that each word read from the drum has odd parity, a character count to ensure that each word transferred to or from the drum consists of exactly six characters, and checks for invalid drum addresses and function codes. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Processor a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 8 months.

.15 First Delivery: . . . third quarter 1966.

.16 Reserved Storage: . . 224 of the 1,760 tracks are reserved for spares, parity, and timing functions, and are not accessible by the programmer.
Manual switches permit protection of storage areas against write operations in increments of 8,192 words.

.2 PHYSICAL FORM

.21 Storage Medium: . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter: . . . . . 24 inches.
Length: . . . . . 36 inches.
Number on shaft: . . 1.

.23 Storage Phenomenon: magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . no.

.25 Data Volume per Band of 6 Tracks

Words: . . . . . 8,192.
Characters: . . . . . 49,152.
Instructions: . . . . . 8,192.

.26 Bands per Physical Unit: . . . . . 256.

.27 Interleaving Levels:. 1, 2, 4, 8, or 16.

.28 Access Techniques

.281 Recording method: . 1 aerodynamically-supported head per track.

.283 Type of access:. . . . word-addressable.

.29 Potential Transfer Rates

.291 Peak bit rates —

Cycling rates: . . .	1,770 rpm.
Track/head speed:.	1,850 inches/sec.
Bits/inch/track: . .	780.
Bit rate per track:.	1,440,000 bits/sec.

.292 Peak data rates —

Unit of data:	word.
Conversion factor:.	36 bits per word.
Gain factor:	6 tracks per band.
Loss factor:	interlace factors of 2, 4, 8, or 16 are optional.

Data rate:

Interlace option	Words/sec	Char/sec
1	240,000	1,440,000
2	120,000	720,000
4	60,000	360,000
8	30,000	180,000
16	15,000	90,000

.3 DATA CAPACITY

.31 Module and System Sizes (FH-1782 Drums only)

	Minimum Storage	Maximum per Subsystem
Drums:	1	8
Words:	2,097,152	16,778,216
Characters:	12,582,912	100,663,296
Instructions:	2,097,152	16,778,216

.32 Rules for Combining Modules: . . . . . 1 to 8 FH-1782 Drum Units, or 1 to 9 FH-432 Drum Units, or 1 to 8 FH-432 and FH-1782 Drum Units (in any combination) per Magnetic Drum Subsystem.

.4 CONTROLLER

.41 Identity: . . . . . FH-432/1782 Drum Control and Synchronizer Unit, Single or Dual Channel.

.42 Connection to System: 1 controller per Magnetic Drum Subsystem. Each subsystem fully occupies 1 or 2 input-output channels.

.43 Connection to Device: 1 to 8 FH-1782 Drum Units per controller; see also Paragraph .32.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 65,535 words.

.442 Input-output area:. . core memory.

.443 Input-output area access:. . . . . each word.

.444 Input-output area lockout: . . . . . none.

.445 Synchronization:. . . automatic.

.447 Table control:. . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads: . . . . . one fixed head serves each track.

.52 Simultaneous Operations: . . . . . maximum of 1 read, write, or search operation per Single-Channel Subsystem; maximum of two read, write, or search operations (in any combination, but must occur on different drum units) per Dual-Channel Subsystem.

.53 Access Time Parameters and Variations

Stage	Variation, msec	Average, msec
Switch bands:	0 or 0.04	--
Wait for specified sector:	0 to 34.0	17.0
Read or write:. . . .	(see Paragraph .292)	

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size:. 1 to 65,535 words.

.73 Effective Transfer Rate (with Core Memory)

Interlace option	Words/sec	Char/sec
1	227,000	1,362,000
2	117,000	702,000
4	59,200	355,200
8	29,800	178,800
16	15,000	90,000

.74 Update Cycle Rate: . 11.8 references/second, based on random accessing of one 84-character record; reading, updating, and writing that record; and rereading for verification of recording. An interlace option of 1 is assumed.

.75 Read-Only Reference Rate: . . . . . 58.1 references/second; based on random accessing of one 84-character record, with no updating or rewriting. An interlace option of 1 is assumed.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bits.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Reference to locked area:	check	interrupt.

Note: The type of error is indicated in the status word which is transferred to core memory when an interrupt occurs.

INTERNAL STORAGE: FASTRAND II

.1 GENERAL

.11 Identity: . . . . . Fastrand II Mass Storage Subsystem.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Fastrand II Mass Storage Subsystem provides relatively fast random access to large quantities of data stored on magnetic drums. Each Fastrand II Storage Unit has a capacity of 22,020,096 UNIVAC 1108 words (132,120,576 characters). A Fastrand II Subsystem consists of from one to eight Storage Units connected to a Single- or Dual-Channel Fastrand Control and Synchronizer Unit. One fully-expanded Fastrand II subsystem can provide on-line storage for over one billion characters of data. Average random access time to any record in Fastrand storage is 93 milliseconds.

An option is available to provide a 35-millisecond average access to 43,008 additional words. This option, called Fastband, provides an additional 24 data tracks with fixed read/write heads. Another option provides lockout protection. It consists of a key-controlled switch which, when set, will prevent the writing of data in a specified area of the drum unit on which it is installed.

Each Fastrand II Storage Unit contains two magnetic drums, which are treated as a single logical unit by the controller. There are 64 aerodynamically-supported read/write heads per Storage Unit (32 per drum). All 64 heads are connected to a common positioning mechanism and move in unison. Head positioning time varies from 30 to 86 milliseconds and averages 58 milliseconds. Drum speed is 870 revolutions per minute, so the rotational delay varies from 0 to 69 milliseconds and averages 35 milliseconds. Activation of addressing circuits requires 5 milliseconds, but this is overlapped with the other access time factors. Peak data transfer rate is 25,625 words or 153,750 characters per second.

Each of the two drums in a Fastrand II Storage Unit has 6,144 data tracks; each track is divided into 64 sectors; and each sector holds 28 36-bit UNIVAC 1108 words, recorded serially by bit. The data storage area on each drum is divided into 192 "positions," with 32 tracks per position. The 32 tracks that constitute a position are sequentially addressed but are not physically adjacent to one another; each of the 32 tracks is served by a separate read/write head, so all the data in a single position can be accessed without repositioning.

A general explanation of how input-output operations are handled in the 1108, including demands on the system, can be found in Section 784:111, Simultaneous Operations. Repositioning of the read/write heads to a different position is a separate operation from reading and writing, and repositioning can be carried out simultaneously in all Fastrand Storage Units within a subsystem.

Fastrand search operations cause the contents of a specified drum position to be searched until a bit-by-bit match is found to an Identifier Word stored in the controller. At this point a read operation is initiated. Alternative function codes permit searching every word or only the first word of each drum sector. The search operations make no demands upon the central processor or core storage until a "find" is made.

Longitudinal check characters and phase-monitoring circuits are used for error detection and correction, providing for the recovery of up to 11 bits of missed data. Other checks are made for invalid addresses, illegal function codes, timing conflicts, and sector length errors. Detection of any error causes the controller to initiate an external interrupt and send the Central Processor a Status Word indicating the type of error and (in some cases) the Fastrand location at which it occurred.

The Fastrand Mass Storage Subsystem originally announced for the UNIVAC 1107 system differs from the present Fastrand II only in having 3,072 bands per drum instead of 6,144; thus, the data capacity of each original Fastrand Storage Unit is half that of a Fastrand II Storage Unit.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . second quarter, 1964.

.16 Reserved Storage: . . none; an option permits inhibiting write operations in a specified segment of storage under the control of a key-switch.

.2 PHYSICAL FORM

.21 Storage Medium: . . drums.

.22 Physical Dimensions

.222 Drum-

Diameter:	23.8 inches.
Length:	61.2 inches, effective.
Number on shaft: . .	1.
Number per Storage Unit: . . .	2.

.23 Storage Phenomenon: magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . .	yes.
.242 Data regenerated constantly:	no.
.243 Data volatile:	no.
.244 Data permanent: . . .	no.
.245 Storage changeable: .	no.

.25 Data Volume Per Band of 1 Track

Words:	1,792.
Characters:	10,752.
Instructions:	1,792.
Sectors:	64 (33 words each).
Address tags:	1 (48 bits).

.26 Bands per Physical Unit: . . . . . 6,144 per drum.
12,288 per Storage Unit.

.27 Interleaving Levels: . none.

.28 Access Techniques

.281 Recording method: . . 64 moving heads per Storage Unit, connected to a common positioning mechanism.

.283 Type of access—

Description of stage	Possible starting stage
Move heads to specified position:	when a different position is selected.
Wait for specified sector:	when previously-selected position is used.
Read or write 1 to 65,535 words:	when rotational delay is zero.

.29 Potential Transfer Rates

.291 Peak bit rates—
Cycling rates: . . . 870 rpm.
Track/head speed: . 1,086 inches/sec.
Bits/inch/track: . . 1,000.
Bit rate per track: . 1,086,000 bits/sec/track.

.292 Peak data rates—
Unit of data: . . . . . word.
Conversion factor: . 36 bits per word.
Gain factor: . . . . . 1 track per band.
Data rate: . . . . . 25,625 words/sec (153,750 char/sec).

.3 DATA CAPACITY

.31 Module and System Sizes:

	Minimum Storage	Maximum per Subsystem
Drums (2 per unit):	2	16
Words:	22,020,596	176,160,768
Characters:	132,120,596	1,056,964,608
Instructions:	22,020,096	176,160,768

.32 Rules for Combining Modules: . . . . . 1 to 8 Storage Units per Fastrand Subsystem.

.4 CONTROLLER

.41 Identity: . . . . . Single- or Dual-Channel Fastrand Control and Synchronizer.

.42 Connection to System: 1 Control per Fastrand Subsystem. Each subsystem fully occupies 1 or 2 input-output channels.

.43 Connection to Device: 1 to 8 Fastrand Storage Units per control.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 65,535 words, beginning with the first word of a drum sector.

.442 Input-output area: . . core memory.

.443 Input-output area access: . . . . . each word.

.444 Input-output area lockout: . . . . . none.

.445 Synchronization: . . . automatic.

.447 Table control: . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks—
Stacks per Fastrand Subsystem: . . . . 64 to 512.
Stacks per storage unit: . . . . . 64.
Stacks per drum: . 32.
Stacks per yoke: . . 64.
Yokes per storage unit: . . . . . 1.

.512 Stack movement: . . all 64 stacks in a Storage Unit move in unison, to 1 of 192 discrete positions.

.513 Stacks that can access any particular location: . . . . . 1.

.514 Accessible locations:
By single stack—
With no movement: 64 sectors.
With all movement: 12,288 sectors.
By all stacks—
With no movement: 4,096 sectors per storage unit.
up to 32,768 sectors per subsystem.

.515 Relationship between stacks and locations: 6 bits of the Function Word designate head address.

.52 Simultaneous Operations: . . . . maximum of 1 data transfer or search operation per Single-Channel Fastrand Subsystem or 2 per Dual-Channel Subsystem (involving different storage units), and 1 head-positioning operation per Fastrand Storage Unit.

.53 Access Time Parameters and Variations

Stage	Variation, msec	Average, msec
Activate addressing circuits: . . .	5.0*	*
Position heads: . .	0 or 30.0 to 86.0	58.0
Wait for specified sector:	0 to 69.0	35.0
Read or write: . . .	(see Paragraph .292)	
Total:	5.0 to 155.0	93.0

*Usually overlapped with other timing factors.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size
With core memory: . 1 to 65,535 words, beginning with the first word of a drum sector.

.73 Effective Transfer Rate

From main area of Fastrand II: . . . . 24,700 words/sec (148,200 char/sec).

From Fastbands area of Fastrand II: . . 25,100 words/sec (150,600 char/sec).

(Contd.)

.74 Update Cycle Rate

From main area of Fastrand II: . . . . 4.1 references/second.
From Fastbands area of Fastrand II: . . 5.7 references/second.

Note: Both of the above rates are based on random accessing of one 168-character record (1 sector); reading, updating, and writing that record; and rereading for verification of recording.

.75 Read-Only Reference Rate

From main area of Fastrand II: . . . . 10.6 references/second.
From Fastbands area of Fastrand II: . . 27.7 references/second.

Note: Both of the above rates are based on random accessing and reading of one 168-character record (1 sector), with no updating or rewriting.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Recording of data:	record check character	
Recovery of data:	check character and phase monitoring	interrupt.
Timing conflicts:	check	interrupt.
Physical record missing:	check	interrupt.
Reference to locked area:	check	interrupt.
Sector length error:	check	interrupt.
End of position reached:	check	interrupt.

Note: The type of error is indicated by six bits of the Status Word, sent to core memory when the interrupt occurs.

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 Central Processor.

.12 Description

The UNIVAC 1108 Central Processor is a faster (over five times as fast internally) and more versatile (nearly 30 additional instructions) version of the earlier UNIVAC 1107 Central Computer, which is described on page 784:051.100. The principle extensions to the 1107's facilities include:

- Double-precision fixed-point and floating-point arithmetic,
- Additional control and shift instructions,
- Improved memory protection, and
- A set of index, arithmetic, and control registers reserved specifically for the operating system.

See page 785:131.100 for a detailed discussion of the compatibility relationships between the 1107 and the 1108.

Except for the differences mentioned above, the instruction repertoire of the 1108 is the same as that of the 1107; it includes fixed-point and floating-point arithmetic, partial-word operations, and several search instructions. As in the 1107, no provisions are included for editing, decimal arithmetic, or radix conversion; generalized subroutines or complex sequences of instructions are required to accomplish these operations.

A key factor in the computing power of the earlier 1107 is its Control Memory, which provides 128 36-bit storage locations of thin-film memory with a cycle time of 333 nanoseconds. A total of 63 locations are used to provide index registers, arithmetic registers, and control registers; the other 65 locations are available to the programmer as intermediate storage. The 1108's Control Memory utilizes integrated circuit registers with a cycle time of 125 nanoseconds and also contains 128 36-bit locations. According to UNIVAC, a survey of 1107 users indicated that the non-special-purpose locations of the Control Memory were not being used; in the 1108, therefore, 71 of the 128 locations are reserved for use by the operating system. These reserved locations include a separate set of index registers, arithmetic registers, and control registers, as well as the Input/Output Access Control Registers. Of the 47 locations available to users' programs, 31 are used to provide index, arithmetic, and control registers. In both the reserved and non-reserved areas, four locations can be used as either index or arithmetic registers, or both, permitting some unusual and powerful address modification operations.

The address modification facilities provided for the 1108 are the same as for the 1107; i.e., non-cumulative indexing with automatic incrementation or decrementation, and recursive indirect addressing with indexing possible at each level.

As in the 1107, the 128 lowest-order locations of Core Memory are "hidden." Their addresses (octal 000 through 177) are the same as those of Control Memory, and they can be accessed only by indirect addressing, by jump instructions, or by input-output operations. All other instructions will refer to the correspondingly-numbered Control Memory locations. The "hidden" core locations are therefore protected from overwriting by internal data transfer operations, but not from input-output operations; the converse applies to all of Control Memory. To minimize confusion between the contents of Control and "hidden" memory, the safest policy is to avoid program references to the core locations below octal address 177.

The instruction format of the 1108 is identical with that of the 1107. A 16-bit address specification field allows direct addressing of up to 65,536 words of storage. Addressing of the full extent of core storage - up to 262,144 words - is accomplished through the use of either the index registers (18 bits) or the basing registers (9 bits, modulo 512). There are two basing registers: the Instruction Bank Basing Register and the Data Bank Basing Register. The contents of the appropriate basing register is added to every programmed address prior to referencing core storage (unless inhibited by the setting of the Base Register Suppression bit in the Processor State Register). The basing operation is referred to as relative addressing and requires no additional time.

Like the 1107, the 1108 Central Processor can make simultaneous accesses to two memory modules. While the operand for the current instruction is being fetched from one memory module, the next instruction can be fetched from a different module. Execution of the current instruction and decoding of the next instruction can be overlapped. This process results in an effective memory cycle time of 375 nanoseconds when instructions and operands are in separate modules. If both instructions and operands are located in the same module, no overlapping can occur. The standard assembler and compilers are oriented toward automatic allocation of instructions and operands to separate modules whenever possible. Additional speed increases are possible in a multiprocessor system; see the discussion of Multiprocessing in Paragraph .122 of this report section.

Program interrupts occur upon normal completion of an input-output operation (when requested); upon detection of an input-output, storage reference, or processor error; and whenever the contents of the real-time clock have been decremented to zero. Depending upon the cause of interruption, control is transferred to one of 41 fixed core memory locations. The interrupt facility makes multiprogramming practical. Only the contents of the instruction sequence counter and the Processor State Register

.12 Description (Contd.)

are automatically saved when an interrupt occurs. The operating system routine that services the interrupt condition utilizes the reserved set of registers. If control is switched to another user's program, the previous contents of the user's set of registers must be preserved; this is accomplished by the standard operating system.

.121 Multiprogramming

Several new hardware features enhance the multiprogramming capabilities of the 1108 when compared to the already proven capabilities of the UNIVAC 1107. In a multiprogramming environment, several programs and their associated data can be in core storage at the same time. Two factors are of paramount importance: security (i.e., memory protection) and control (i.e., sequencing and switching between programs).

The 1108, like most other recent computer systems designed for multiprogramming, can operate in different modes. Certain modes make certain instructions and areas of core storage unavailable to the program. In the 1108, memory protection and operational mode are controlled by the Processor State Register and the Storage Limits Register.

The Processor State Register contains two 9-bit address basing registers, a basing-register selection register, and a number of 1-bit designators. Four of these designators are used to specify the facilities available to a program, including:

- Base register suppression - designates whether the contents of one of the basing registers will be added to program addresses prior to referencing memory.
- Control register selection - designates which of the two sets of index, arithmetic, and control registers contained in Control Memory will be used by the program.
- Guard mode - designates whether the program has access to reserved Control Memory locations or to certain reserved instructions.
- Storage protection mode - designates the type of storage protection for areas outside the boundaries of the program. In conjunction with the Guard Mode designator, protection can be against writing only; against reading, writing, or jumping; or non-existent.

The two basing registers provide relative addressing for users' programs; i.e., the contents of a basing register is added to the developed address for each instruction and each operand prior to referencing core storage. The provision of separate registers for the instruction area and for the data area aids in maintaining the instructions and data in separate memory modules to achieve maximum execution speeds. A third register within the Processor State Register designates whether the Instruction Basing Register or the Data Basing Register is to be used for a particular reference to memory. Relative addressing does not require any extra time.

The Storage Limits Register contains four 9-bit fields which specify the upper and lower program address limits for the instruction area and for the data area. Each field is counted modulo 512; i.e., each field is logically an 18-bit address specification, with the 9 low-order bits always assumed to be zero. Core storage can thus be allocated in blocks of 512 words.

The reserved instructions include:

- Loading of Processor State Register or Storage Limits Register.
- Halt instruction.
- All I/O instructions.

The 1108 Executive System (page 785:191.100) uses the designators in the Processor State Register to establish one of three modes of operation:

- Job Program Mode - In this mode relative addressing is in effect, and any attempt to read, write, or branch into areas outside the limits defined by the Storage Limits Register causes an interrupt. A reference to the reserved set of registers in the Control Memory or an attempt to execute any of the reserved instructions also results in an interrupt.
- Privileged Mode - This mode is similar to the Job Program Mode except that any location of core storage can be accessed for reading but not for writing; the other restrictions also apply. This mode allows a user's program to read, but not to alter, supervisory routines.
- Open Mode - In this mode the complete facilities of the system are available; there are no restrictions on the core storage locations accessible or on the instructions used, and relative addressing is not in effect. Normally, only the Executive System is allowed to operate in this mode.

An interrupt causes a forced transfer into the Open Mode and a branch to a specific location in core storage; the destination depends upon the cause of the interrupt. Normally, a jump is then made to a supervisory routine which services the interrupt condition.

The scheduling of jobs for processing and the switching from program to program are performed under control of the 1108 Executive System, as described in Paragraph 785:191.12.

.122 Multiprocessing

Multiple 1108 Central Processors can share the same core storage via Multiple Module Access Units (MMA). These adapters provide connections for up to five Central Processors or I/O Controllers in any combination. Multiprocessor 1108 configurations have been designated "1108-II" systems by UNIVAC.

A major factor affecting the performance of a multiprocessor configuration is its ability to handle multiple simultaneous accesses to main memory. Obviously, if only one access at a time can be made, two or more processors will be little, if any, faster than a single processor. In the 1108, this need for simultaneous memory accesses is handled by having independent memory modules (up to eight) and by interleaving the physical locations of main memory addresses. Within a cabinet of two 32,768-word memory modules, the even addresses are assigned to one module and the odd addresses to the other. Half of a program loaded into core storage will therefore be in one module, and half in the other. As in the single-processor version,

(Contd.)

.122 Multiprocessing (Contd.)

separate instruction and data areas are maintained to take advantage of the overlap feature of the processor. Thus, obtaining sequential instructions or operands requires alternate accesses to main memory - first from one module of a pair, and then the other.

Since each module is independently accessible, a second processor can access instructions or data from the even module while the first processor is accessing the odd module. In this manner, two processors can simultaneously execute two separate programs which are located in the same memory modules. If two processors attempt to access the same memory module at the same time - as when two programs both start at even locations - one processor will be delayed for one cycle. A fixed priority among the processors governs the order of precedence. After this one-cycle delay, the processors will again be in synchronization, and both processors can proceed.

A maximum of eight independent memory modules limits the maximum number of processors that can operate simultaneously in this fashion to four. In this situation, one pair of programs would be spread over one group of four modules, and a second pair of programs would be spread over the second group of four modules. The minimum 1108-II configuration of four memory modules can effectively support two processors.

The effective performance of a two-processor configuration varies with the starting locations (even or odd) of the instruction and data areas of the two tasks being executed simultaneously, and also with the frequency of instructions that require more than one memory cycle to execute. These considerations affect the frequency of potential memory conflicts between the two processors. The effective internal speed of a two-processor configuration ranges from about 1.5 to 2.0 times the speed of a single processor. The effective performance of a multiprocessor configuration including more than two processors depends on the number of memory modules in the system and the arrangement of programs in core storage. Under ideal conditions, a speed ratio of four compared to a single processor can be obtained, as outlined in preceding paragraphs.

To provide the Executive System with a means of control in a multiprocessor configuration, a special instruction allows one processor to transmit an interrupt signal to one of two other processors. Thus, the Executive System has a means of controlling the activity of each processor. See Paragraph 785:191.12 for a discussion of how the 1108 Executive System handles system operations in a multiprocessing environment.

.13 Availability. . . . . 9 months.

.14 First Delivery. . . . . December 1965.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point —			
Add-subtract:	automatic	binary	35 or 71 bits + sign.*
Multiply —			
Short:	automatic; integer only	binary	35 bits + sign.*
Long:	automatic; integer or fractional	binary	35 bits + sign (72-bit product).*
Divide			
No remainder:	automatic; fractional only	binary	35 bits + sign.*
Remainder:	automatic; integer or fractional	binary	35 bits + sign (72-bit dividend).*
.212 Floating point —			
Add-subtract:	automatic	binary	27 and 8 bits (short). 60 and 11 bits (long).
Multiply:	automatic	binary	
Divide:	automatic	binary	
.213 Boolean —			
AND	automatic	binary	36 bits.*
Inclusive OR:	automatic		
Exclusive OR:	automatic		
.214 Comparison —			
Numbers:	automatic		36 bits.*
Absolute:	none.		
Letters:	automatic		36 bits (6 chars).*
Mixed:	automatic		36 bits.*
Collating sequence:	see Data Code Table,	Section 785:141.	

* j-designator can specify use of the full addressed operand or any half-word (18 bits), third-word (12 bits), or sixth-word (6 bits) portion of it.

		Provision	Between	And	Size
.215	Code translation:	none.			
.216	Radix conversion:	standard subroutine	binary field	BCD chars	1 to 36 bits; 3 to 13 chars.

		Provision	Comment	Size
.217	Edit format —			
	Alter size:	standard subroutine	handles numeric data only.	1 to 36 bits before editing.
	Suppress zero:			
	Insert point:			
	Insert spaces:			
	Insert sign:			
	Float character:	none.		
	Protection:	none.		
	Round off:	none.		
.218	Table lookup —			
	Equality:	automatic	look-up can be based on any bit pattern using Masked Search instructions.	36 bits.*
	Less than or equal:	automatic		
	Greater than:	automatic		
	Within limits:	automatic		
	Outside limits:	automatic		
	Greatest:	none.		
	Least:	none.		
.219	Others —			
	Add/subtract halves:	automatic		two 18-bit fields/word.
	Add/subtract thirds:	automatic		three 12-bit fields/word.
	Shifts:	automatic	left or right circular, logical, or arithmetic shifts	1 or 2 words.
	Block transfer:	automatic		1 to N words.*

* j-designator can specify use of the full addressed operand or any half-word (18 bits), third-word (12 bits), or sixth-word (6 bits) portion of it.

.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement.

.222 Zero: . . . . . 1 form: zero in all bit positions.

.223 Operand size determination: . . . . specified in the instruction by the f- or j-designators or by a combination of the two.

.23 Instruction Formats

.231 Instruction structure: . 1 word.

.232 Instruction layout:

Name	f	j	a	x	h	i	u
Size (bits)	6	4	4	4	1	1	16

.233 Instruction parts —

Name	Purpose
f-designator:	specifies major operation code.
j-designator:	(1) specifies partial-word operands; or (2) provides expanded operation code; or (3) indicates that u is a literal rather than an address.
a-designator: . . .	(1) references an Arithmetic Register; or (2) specifies an input-output channel. (3) serves one of several other specialized functions.
x-designator:	references an Index Register, whose contents are added to u.
h-designator: . . .	indicates whether the specified Index Register shall be incremented or decremented.
i-designator:	indicates whether u is a direct or indirect address.
u-designator: . . .	(1) specifies base operand address; or (2) specifies shift count; or (3) holds a literal operand.

.234 Basic address structure: . . . . . 1 + 0. (The a-designator references one of the 16 Arithmetic Registers, providing a limited two-address capability in many load, store, arithmetic, logical, and test instructions.)

(Contd.)

.235 Literals —
Arithmetic: . . . . . 18 bits.
Comparisons and tests:. . . . . 18 bits.
Incrementing modifiers: . . . . . 18 bits.

.236 Directly addressed operands —

Storage type	Minimum size	Maximum size	Volume accessible
Control Memory:	6 bits	1 word	128 words.
Core Memory:	6 bits	1 word	total capacity (up to 262,144 words).

.237 Address indexing —
.2371 Number of methods: . 1
.2372 Names: . . . . . indexing.
.2373 Indexing rule:. . . . . add contents of modifier portion (lower half) of specified index register to instruction address, modulo 262,144.
.2374 Index specification . . by x-designator in the instruction to be modified.
.2375 Number of potential indexers: . . . . . 15.
.2376 Addresses which can be indexed: . . . . . operand address portion (u-designator) of all instructions, including literals.
.2377 Cumulative indexing:. none; but see Paragraph .2384.
.2378 Combined index and step:. . . . . yes; if h-designator (bit 17) is 1, add contents of increment portion of specified index register to its modifier portion after the effective operand address has been formed.

.238 Indirect addressing —
.2381 Recursive:. . . . . yes.
.2382 Designation: . . . . . 1 in i-designator (bit 16) of each indirect address.
.2383 Control: . . . . . 0 in i-designator of the direct address.
.2384 Indexing with indirect addressing: . . . . . yes; indexing occurs before determination of the indirect address. Both indexing and incrementation of the index register can be specified at each stage of indirect addressing.

.239 Stepping —
.2391 Specification of increment: . . . . . in most significant half of the index register.
.2392 Increment sign: . . . + or -.
.2393 Size of increment: . . 18 bits.
.2394 End value: . . . . . zero, or any value specified in test instruction or storage location.
.2395 Combined step and test:. . . . . yes.

.24 Special Processor Storage

.241 Category of storage	Number of locations	Size in bits	Program usage
Control register:	1	16	P-Register: holds address of next instruction.
Control register:	2	36	Program Control Registers: decode instructions (both are used in alternate-bank operation).
Control register:	3	18	W-Registers: input registers for the Index Adder.
Control register:	1	18	R-Register: output register for the Index Adder.
Control register:	1	18	Storage Class Control; decodes operand addresses.
Control register:	1	36	Storage Limits Register: holds upper and lower boundaries for instruction and data area.
Control register:	1	36	Processor State Register: holds address basing registers and control information.
Control register:	1	4	Channel Select Register: holds identity of input-output channel selected.
Control memory— Available to user programs:	15*	36	Index Registers.
	16*	36	Arithmetic Registers.
	1	36	Repeat Count.
	1	36	Mask Word.
	1	36	Temporary Storage for P-Register.
	17	36	Unrestricted storage for operands and intermediate results.
Reserved for Executive System:	16*	36	Index Registers.
	16*	36	Arithmetic Registers.
	1	36	Real-Time Clock Count.
	16	36	Input Access Control.

.241 Category of storage	Number of locations	Size in bits	Program usage
Reserved for Executive System (Contd.):	16	36	Output Access Control.
	1	36	Repeat Count.
	1	36	Mask Word.
	18	36	Unassigned.

* Four locations can be used as either Index or Arithmetic Registers.

.242 Category of storage	Total number of locations	Physical form	Access time, μsec	Cycle time, μsec
Control registers:	8	flip-flop	?	?
Control memory:	128	integrated circuit flip-flops	?	0.125

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . 1 (P-Register).

.314 Special sub-sequence counters: . . . . . none (during repeated instructions, address of next instruction is stored in Control Memory and P-Register holds the Repeat Count Word).

.315 Sequence control step size: . . . . . 1 word.

.316 Accessibility to routines: . . . . . P-Register contents can be stored in core storage or in an Index Register.

.317 Permanent or optional modifier: . . . . . no.

.32 Look-Ahead: . . . . . when instructions and data are stored in separate banks, the next instruction can be accessed and partially decoded during execution of the current instruction, reducing execution time by 0.75 μsec for each load, store, arithmetic, logical, and test instruction.

.33 Interruption

.331 Possible causes —

- In-out units: . . . . . see next entry.
- In-out channels: . . . completion of input, output, or external function operation; or input-output error.
- Storage access: . . . reference to locked-out core storage area; completion of magnetic drum operation; magnetic drum error; core storage parity error.
- Processor errors: . invalid operation, exponent underflow, exponent overflow, divide overflow.
- Other: . . . . . real-time clock; day clock; external synchronization (supplementary real-time clock or master clock for a multi-processor complex).

.332 Control by routine —

- Individual control: . . enable or disable external interrupts on all channels or any specific channel.
- Method: . . . . . special instructions.
- Restriction: . . . . . central processor and core storage error interrupts cannot be locked out; no restriction on external interrupts.

.333 Operator control: . . . none.

.334 Interruption conditions: (1) interrupt enabled; and (2) not currently processing an interrupt condition.

.335 Interruption process —

- Disabling interruption: . . . . . automatic.
- Registers saved: . . contents of P-Register (sequence counter) are saved by "return jump" instruction in destination register; Processor State Register is saved in Control Memory location 0; other registers by program.
- Destination: . . . . . one of 41 fixed locations, depending upon cause.

.336 Control methods —

- Determine cause: . . automatic; destination depends upon cause.
- Enable interruption: . by special instruction before returning to main routine.

.34 Multiprogramming

.341 Method of control: . . by Executive System (see Section 785:191), using the interrupt facilities described above.

.342 Maximum number of programs: . . . . . limited only by hardware availability.

.343 Precedence rules: . . see Paragraph 785:191.12.

.344 Program protection —

- Storage: . . . . . Storage Limits Register specifies the address limits (in 512-word increments) of the instruction and data areas in core storage which are unavailable for reading/writing/jumping or for writing only; see Paragraph .121, "Multiprogramming."

(Contd.)

.344 Program protection — Storage (Contd.)

In-out units: . . . . . under control of software; no automatic protection; see Paragraph 785:191.12.

.35 Multi-sequencing: . . . possible only in multiprocessor complexes. See Paragraph .122, "Multiprocessing."

.4 PROCESSOR SPEEDS

The times listed in this paragraph are for cases where the instructions and the operands are stored in separate memory modules. If the instructions and operands are located in the same module, the execution time of each instruction is increased by 0.75 microseconds. See Paragraph .122 for a discussion of the effective speeds of multiprocessor (1108-II) configurations.

.41 Instruction Times in Microseconds

	Short (1 word)	Long (2 words)
.411 Fixed point —		
Add-subtract:	0.75	1.625
Multiply:	2.375	-
Divide:	10.125	-
.412 Floating point —		
Add-subtract:	1.75	2.625
Multiply:	2.625	4.25
Divide:	8.25	17.25
.413 Additional allowance for —		
Indexing:	0.	
Indirect addressing, per stage:	0.75	
Re-complementing: .	0.	
.414 Control —		
Compare:	0.875 to 1.75*	
Branch:	0.75	
Compare and branch:	1.625 to 1.75*	
.415 Counter control —		
Step:	0.	
Step and test:	1.00	
.418 Shift:	0.75 (independent of length of shift).	

* Times vary according to condition tested and result.

.42 Processor Performance in Microseconds

	Short (1 word)	Long (2 words)
.421 For random addresses:		
Fixed point —		
$c = a + b$:	2.25	4.625
$b = a + b$:	2.25	4.625
Sum N items, per item:	0.75	1.625
$c = ab$:	3.875	-
$c = a/b$:	11.625	-
Floating point —		
$c = a + b$:	3.25	5.625
$b = a + b$:	3.25	5.625
Sum N items, per item:	1.75	2.625
$c = ab$:	4.125	7.25
$c = a/b$:	9.75	20.25
.422 For arrays of data:		
Fixed point —		
$c_i = a_i + b_i$:	3.75	6.125
$b_j = a_i + b_j$:	3.75	6.125
Sum N items, per item:	0.75	1.625
$c = c + a_i b_j$:	5.375	-
Floating point —		
$c_i = a_i + b_j$:	4.75	7.125
$b_j = a_i + b_j$:	4.75	7.125
Sum N items, per item:	1.75	2.625
$c = c + a_i b_j$:	6.625	9.875
.423 Branch based on comparison —		
Numeric data:	7.25	
Alphabetic data: . . .	7.25	
.424 Switching —		
Unchecked:	2.25	
Checked:	5.50	
List search:	2.25 + 3.0N	
.425 Format control, per character —		
Unpack —		
Without radix conversion: . . .	0.51	
With radix conversion: . . .	2.7	
Compose:	5.0	
.426 Table look-up, per comparison —		
For a match:	0.875	
For least or greatest:	1.325	
For interpolation point:	0.875	
.428 Moving (full words or 6, 12, or 18-bit fields) —		
1 word:	3.0	
N words:	1.5 + 1.5N	

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Add/subtract overflow:	check	set indicator.
Divide overflow:	check	interrupt.
Exponent overflow:	check	interrupt.
Exponent underflow:	check	interrupt.
Zero divisor:	check	interrupt.
Invalid data:	none.	
Invalid operation:	check	interrupt.
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Reference to locked-out storage area:	check	interrupt.

CONSOLE

.1 GENERAL

.11 Identity: . . . . . 1108 Control Console.

.12 Associated Units: . . . . Keyboard and Printer.
CRT Display.

.13 Description

.131 Single-Processor Configuration

The Control Console forms the operating center of a UNIVAC 1108 and is essentially the same console as the one provided for its predecessor, the UNIVAC 1107. It consists of a desk with a 54-by-36-inch top and ultramodern styling, featuring two pillars that reach from floor to ceiling and support a display panel at eye-level height for a seated operator. Built into the desk top are a standard typewriter keyboard and a Teletype Model 35 Page Printer. The keyboard and page printer permit direct communication between the operator and the stored programs. The console controls and displays enable the operator to:

- Start and stop execution of the stored program.
- Clear all Central Processor registers.
- Set any of 15 Selective Jump switches, which can be tested by conditional jump instructions.
- Set any of 4 Selective Stop switches, which can cause the stored program to halt.
- Select any input-output channel for initial loading of a "bootstrap" program.
- Read, set, and/or clear the contents of the P register (the instruction sequence counter).
- Initiate a manual interrupt of the computer program to permit keyboard input at any time.
- Note the occurrence of excessive temperature, low voltage, initial loading errors, and peripheral equipment faults (e.g., illegal operation codes) by means of console indicators.

The contents of the arithmetic registers and index registers cannot be displayed on the console panel, and no direct means is provided for entering data into these registers or into specific Core Memory locations.

The Keyboard is a standard 4-bank typewriter keyboard that can generate the 64 basic Fieldata character codes. The console printer is the Teletype Model 35 Page Printer, which prints 1 character at a time at a peak speed of 10 characters per second. It can print the 26 alphabetic, 10 numeric, and 20 special characters of the Fieldata code and responds to the remaining 8 control codes (e.g., space and carriage return). Output is on a continuous paper roll, 8-1/2 inches wide and up to 5 inches in diameter. All data transfers between the Central Processor and the console input-output units must be programmed on a character-at-a-time basis.

Up to four consoles can be connected to one input-output channel of a processor and can operate simultaneously. Additional consoles can be added by connecting them to input and output positions of the Communication Terminal Module Controller (see Section 785:102). The standard operating system, the 1108 Executive System, has provisions for dividing the console operations among up to five consoles.

.132 Multiprocessor Configuration (UNIVAC 1108-II)

In addition to the facilities mentioned above, a cathode-ray-tube (CRT) display device is incorporated into the Control Console for a multiprocessor 1108 system. The CRT can display up to 16 lines of up to 32 characters each. Provisions are contained in the Executive System for displaying program status messages, error messages, tape mounting requests, etc. upon requests from the operator or as a result of certain program contingencies. Often there will be more information to be displayed than can be displayed at one time on the face of the tube. In this case, the operator can request that the information be "rolled through"; i.e., the information is displayed as if on a continuous, moving roll. If the backlog of information to be displayed becomes too great, the console printer is used as a backup device.

Operator-initiated messages can be constructed and verified on the display device prior to submission to the system. The Executive System reserves one display line for this purpose at all times.

The principal advantage in using a CRT display device for console display functions is the increased ease of use and identification of current status by the operators; the display device itself "pages" through the status information. Care should be taken to ensure that sufficient information is also transferred to hard copy (console printer or a log file) to maintain adequate records of system performance and other system information.

.133 Auxiliary Communications Console

If desired, the control panel for a Communications Subsystem (see Section 785:102) can be placed in a wing added to either of the 1108 consoles described above. This panel provides power control switches and indicators for a Communications Subsystem. In addition, a lamp for each of the 64 possible input-output line positions provides a visual indication whenever that line is transmitting or receiving data.

INPUT-OUTPUT: PUNCHED CARD SUBSYSTEM

.1 GENERAL

.11 Identity: . . . . . 900-cpm Card Reader.
300-cpm Card Punch.
Card Control and Synchronizer.

.12 Description

One Card Reader and/or one Card Punch can be connected to a Card Control and Synchronizer Unit to form a Punched Card Subsystem. Each Punched Card Subsystem fully occupies one UNIVAC 1108 input-output channel. The card reader and card punch units within a Punched Card Subsystem cannot operate concurrently.

.121 Card Reader

The Card Reader used with the UNIVAC 1108 can read standard 80-column cards at a peak rate of 900 cards per minute. Significant characteristics of the Card Reader include:

- A 3,000-card input hopper.
- A 2,500-card output stacker.
- Photodiode sensing, with automatic checking of the sensory elements before each card is read.
- An infinite clutch to provide demand card reading.
- Binary card-image reading.
- Automatic translation from Hollerith code to the 6-bit UNIVAC 1108 internal code when reading in the translate mode. The Channel Synchronizer assembles the 6-bit codes into 36-bit computer words.
- Generation of an interrupt signal upon successful completion of a read operation and upon detection of an error condition or a unit not-ready condition. The read-complete interrupt can be inhibited by the program. Detected conditions, including registration check errors, parity errors, sensing element errors, unit busy, and unit not ready (off-normal) conditions, are identified in the Status Word that is transferred to memory when an interrupt is generated.

Card images can be transferred to core memory without translation in either the column binary or row binary mode. In the column binary mode, the bit pattern of each group of three consecutive card columns fills one computer word. In the row binary mode, the bit pattern of each card row fills two consecutive computer words and the 8 high-order bit positions of a third word.

The ability to initiate a card read operation at any time (due to the infinite clutch) and the relatively small demands made on the system during a read operation should permit reading speeds close to the peak speed to be achieved in most applications.

.122 Card Punch

The Card Punch used with the UNIVAC 1108 punches and verifies standard 80-column cards at a peak speed of 300 cards per minute. Among the significant characteristics of the card punch are the following:

- A 1,000-card input hopper.
- Two 850-card output stackers.
- Four separate card transport stations (two wait stations, followed by the punch station and a post-punch check station).
- A single-access-point clutch.
- Binary card-image punching (but a maximum of 240 holes can be punched per card).
- Automatic translation from internal to Hollerith code. The Channel Synchronizer disassembles each 36-bit computer word into six 6-bit characters and transmits them to buffer storage in the Card Control Unit. Each 6-bit character is then translated into one Hollerith-coded character.
- Complete card-image comparison to verify punching accuracy.
- Generation of an interrupt signal upon successful completion of a card punch operation or upon encountering an error condition or a unit not-ready condition. The read-complete signal can be inhibited by the program. Detected conditions, including punching errors and unit busy and unit not-ready conditions, are identified in the Status Word that is transferred to memory when an interrupt is generated.

INPUT-OUTPUT: PUNCHED TAPE SUBSYSTEM

.1 GENERAL

.11 Identity: . . . . . Punched Paper Tape Subsystem.

.12 Description

The Punched Paper Tape Subsystem available with the UNIVAC 1107 Computer System will also be offered for the 1108. This subsystem includes a modified Digitronics Model B 2500 reader and a modified Teletype BRPE-11 punch in the same cabinet along with a control unit. These devices are described in detail in Report Sections 784:075 and 784:076; a brief description follows.

The peak reading speed is 400 characters per second, and the peak punching speed is 110 characters per second.

The reader is mounted vertically, and the tape is fed down into it from a supply reel with a tension-arm reservoir. No take-up facilities are provided. Reading is performed photoelectrically by silicon photodiodes. Tape can be read backward as well as forward, but backward movement may not exceed 12 inches (120 characters). The reader can handle tape with five, six, seven, or eight data tracks and 11/16, 7/8, or 1 inch in width. Because all code translation must be programmed, any tape code can be used.

Tape is fed to the punch from a supply reel with a tension-arm reservoir, but no take-up facilities are provided. The punch can handle tape with five, six, seven, or eight data tracks and 11/16, 7/8, or 1 inch in width. Because all code translation must be programmed, any tape code can be used.

As each punch is activated, it closes a switch which verifies that punching actually took place in that position. The pattern of holes (or "1" bits) actually punched in each tape row is then compared with the desired pattern. An invalid comparison halts the punching operation, initiates an external interrupt, and sets a bit in the Status Word to indicate the reason for the interrupt.

The Paper Tape Subsystem does not include a Channel Synchronizer for the assembly of characters into 1108 words. Therefore, the reader must communicate directly with the computer on a character-by-character basis. Character codes read from the tape are transferred without translation into the eight low-order bit positions of consecutive word locations in core memory. No automatic parity checking is provided. When a parity check is required, it must be accomplished through a program subroutine. (The 1108 has special instructions that facilitate programmed parity checking.)

INPUT-OUTPUT: PRINTER

.1 GENERAL

.11 Identity: . . . . . High-Speed Printer.

.12 Description

A High-Speed Printer Subsystem consists of a Synchronizer/Control Unit and from one to four High-Speed Printers. A Printer Subsystem fully occupies one UNIVAC 1108 input-output channel. All printers in a subsystem can operate simultaneously.

The maximum printing speed is 700 single-spaced lines per minute utilizing the full 63-character set or 922 lines per minute utilizing any set of 41 contiguous characters. Table I shows the effective print speeds at various line spacings. The arrangement of the characters on the drum puts the alphabetics, numerics, and 5 commonly-used special symbols in one 41-character group. The 63 characters that can be printed are the 26 upper-case alphabetics, the 10 numerics, and 27 punctuation marks and other special symbols. The 64th character code is the space or blank.

The printed lines can be spaced vertically at either 6 or 8 lines per inch by manual control. Horizontal spacing is 10 characters per inch.

Paper can be advanced at a speed of 20 inches per second, under program control. There is no format control tape to facilitate the control of vertical spacing. The physical dimensions of the forms used can range from 2.75 to 21.5 inches in width. However, use of the 21.5-inch width restricts the printable portion of the form to the center 13.2 inches. Up to 5 carbons plus the original copy, having a combined thickness of up to 0.0155 inch, can be printed between ribbon changes.

Manual controls permit horizontal or vertical adjustment of up to one full character position during printer operation. Visual indicators provide information on the following conditions: power fault, power runaway, ribbon exhausted, interlock(s) open, overheating, paper exhausted, and print carriage out.

The octal character code 77 (the "not equal" symbol) acts as a stop code and defines the end of a line of print. A switch is provided to inhibit this action; a full line of 132 characters will then be transferred to the print buffer for each line of print.

TABLE I: EFFECTIVE SPEED OF 700/922-LPM PRINTER

Lines Advanced per Line Printed (6 lines per inch)	Printed Lines per Minute Using 64-Character Set	Printed Lines per Minute Using 41 Contiguous Characters
1	700	922
2	638	692
3	586	615
4	542	553
5	504	512
6 (1 inch)	472	484
12 (2 inches)	338	346
18 (3 inches)	264	264
24 (4 inches)	217	231
30 (5 inches)	183	185

INPUT-OUTPUT: UNISERVO VIC AND VIIIC TAPE UNITS

.1 GENERAL

.11 Identity: . . . . . Uniservo VIC Magnetic Tape Handler.
Uniservo VIIIC Magnetic Tape Handler.

.12 Description

The Uniservo VIC and VIIIC Tape Handlers are similar, 7-track, IBM 729-compatible units that offer data transfer rates ranging from 8,500 to 96,000 characters per second. These units can be optionally modified at the factory in order to provide 9-track recording capability for compatibility with the IBM 2400 Series tape units used with the System/360. Tape reading can be performed in either a forward or backward direction.

A Uniservo VIC Magnetic Tape Subsystem consists of a single- or dual-channel Control and Synchronizer, from 1 to 4 master units, and from 1 to 12 slave units. Each master unit contains the power supply for itself and up to three slave units. A Uniservo VIIIC Subsystem consists of a single- or dual-channel control and from 1 to 16 tape units. A separate power supply is provided for each of the VIIIC tape units. A dual-channel control requires the use of two input-output channels and allows simultaneous read/read, read/write, or write/write operations.

The economy-priced Uniservo VIC tape units provide data transfer rates of up to 34,000 characters per second; the Uniservo VIIIC tape units can transfer data at up to 96,000 characters per second. Recording density can be 200, 556, or 800 rows per inch. Each tape row consists of six data bits and one parity bit. The 9-track recording option permits eight data bits and one parity bit per row. Block length is variable from one word to 65,535 words. Error conditions are indicated by an interrupt. The type of error can be determined by testing the contents of the input-output Status word.

.13 Availability: . . . . . 9 months.

.14 First Delivery

VIC: . . . . . second quarter, 1965 (with UNIVAC 1050).
VIIIC: . . . . . December, 1965 (with UNIVAC 1108).

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan.
.212 Reservoirs —
Number: . . . . . 2.
Form: . . . . . vacuum columns.
Capacity: . . . . . approximately 2 feet of tape (Uniservo VIC) or 5 feet of tape (Uniservo VIIIC).
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sending and Recording Systems

.221 Recording system: . . . magnetic head.
.222 Sensing system: . . . . . magnetic head.
.223 Common system: . . . . 2-gap head provides read-after-write checking.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase or write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7 (9 optional).
Method of use: . . . . . 1 row at a time.

TABLE I: CHARACTERISTICS OF THE 7-TRACK UNISERVO VIC AND VIIIC MAGNETIC TAPE HANDLERS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, rows per sec	Interblock Gap Lengths			Efficiency, % (3)		Demand on Core Storage, % (4)	Full Rewind Time. minutes
				inches (5)	msec (1)	chars (2)	100-char blocks	1,000-char blocks		
VIC	42.7	200	8,500	0.75	17.5	150	40	87	0.11	3.0
		556	23,700	0.75	17.5	417	19	70	0.29	3.0
		800	34,100	0.75	17.5	600	14	62	0.43	3.0
VIIIC	120.0	200	24,000	0.75	6.0	150	40	87	0.30	1.3
		556	66,720	0.75	6.0	417	19	70	0.88	1.3
		800	96,000	0.75	6.0	600	14	62	1.2	1.3

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.
(4) One memory cycle per word is required. Memory cycle time for the UNIVAC 1108 is 0.75 μsec.
(5) The interblock gap with the optional 9-channel feature is 0.6 inches.

.24 Arrangement of Heads (Contd.)

Use of station:. . . . . read.
Distance: . . . . . 0.25 inch after write head.
Stacks:. . . . . 1.
Heads/stack:. . . . . 7 (9 optional).
Method of use:. . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium:. . . . . plastic tape with magnetizable surface.
.312 Phenomenon:. . . . . magnetization.

.32 Positional Arrangement

.321 Serial by:. . . . . 6 to N rows, at 200, 556, or 800 rows per inch; N specified by UNIVAC 1108 Access Control Word.
.322 Parallel by: . . . . . 7 tracks, standard. 9 tracks, with optional feature.

.324 Track use —

	7-Track	9-Track
Data:	6	8.
Redundancy check:	1 (parity)	1 (parity).
Timing:	0 (self-clocking)	0 (self-clocking).
Unused:	0	0.
Total:	7	9.

.325 Row use —
Data:. . . . . 6 to N.
Redundancy check:. . 1 (2 for 9-channel).
Timing: . . . . . 0.
Control signals:. . . . 0.
Unused: . . . . . 0.
Gap: . . . . . 0.75 inch (0.6 inch for 9-channel).

.33 Coding: . . . . . binary word image, using 6 tape rows per 1108 word and odd parity; or BCD mode, using IBM 6-bit character codes and even parity.

.34 Format Compatibility: with IBM 727, 729, and 7330 Magnetic Tape Units; with IBM 2400 Series tape units if 9-track option is used; with UNIVAC systems using Uniservo IIIC, IVC, or VIC tape handlers; and with other manufacturers' "IBM-compatible" tape units.

.35 Physical Dimensions

.351 Overall width:. . . . . 0.5 inch.
.352 Length: . . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity:. . . . . Uniservo VIC Control and Synchronizer.
Uniservo Auxiliary Control and Synchronizer.
Uniservo VIIIC Control and Synchronizer.
Uniservo VIIIC Auxiliary Control and Synchronizer.
Note: Both a Control and an Auxiliary Control are required for dual-channel capability.

.42 Connection to System

.421 On-line:. . . . . one magnetic tape subsystem fully occupies one or two input-output channels.
.422 Off-line:. . . . . none.

.43 Connection to Device

.431 Devices per controller —
VIC: . . . . . 1 to 4 VIC Master Tape Units per subsystem; 1 to 3 VIC Slave Tape Units per Master Tape Unit (maximum of 16 tape units).
VIIIC: . . . . . 1 to 16 VIIIC Tape Units per subsystem.
.432 Restrictions:. . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 65,535 36-bit words.
.442 Input-output areas:. . . core storage.
.443 Input-output area access: . . . . . each 36-bit word.
.444 Input-output area lockout:. . . . . none; I/O memory protection is provided by checks made by the standard operating system.
.445 Table control:. . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to 65,535 36-bit words, limited by the 15-bit counter in the Access Control Word.

.512 Block demarcation —
Input:. . . . . inter-block gap on tape or word count in Access Control Word.
Output: . . . . . word count in Access Control Word.

.52 Input-Output Operations

.521 Input:. . . . . read 1 block of data, forward or reverse, at 200, 556, or 800 rows per inch in either binary mode (odd parity) or BCD mode (even parity); external interrupt upon completion of the operation is optional.
.522 Output:. . . . . write 1 block of data forward at 200, 556, or 800 rows per inch in either binary or BCD mode; external interrupt upon completion of the operation is optional.
.523 Stepping: . . . . . 1 block backward (backspace); approximately 4 inches forward (to skip and erase defective tape areas).

(Contd.)

.524 Skipping: . . . . . backspace to an end-of-file mark or to load point of tape.
.525 Marking: . . . . . end-of-file mark, interblock gap.
.526 Searching: . . . . . read first word of each block and compare it with identifier word. When a match occurs, read the block as in Paragraph .521.

.53 Code Translation: . . . optional translation between 1108 Fieldata code (odd parity) and IBM BCD code (even parity).

.54 Format Control: . . . . by program.

.55 Control Operations

Disable: . . . . . yes (follow rewind with interlock).
Request interrupt: . . . yes.
Select format: . . . . . yes; binary or BCD.
Rewind: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Output lock: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: yes.
End of file: . . . . . yes.
Rewinding: . . . . . yes.

.6 PERFORMANCE

.62 Speeds

.621 Nominal or peak speed: . . . . . see Table I.
.622 Important parameters: see Table I.
.623 Overhead: . . . . . see Table I.
.624 Effective speeds: . . . . see Table I.

.63 Demands on System: . . see Table I.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Rewind:	switch/light	rewinds and positions tape.
Forward:	switch/light	moves tape forward.
Backward:	switch/light	moves tape backward.
Change tape:	switch/light	moves tape to load position.

.73 Loading and unloading

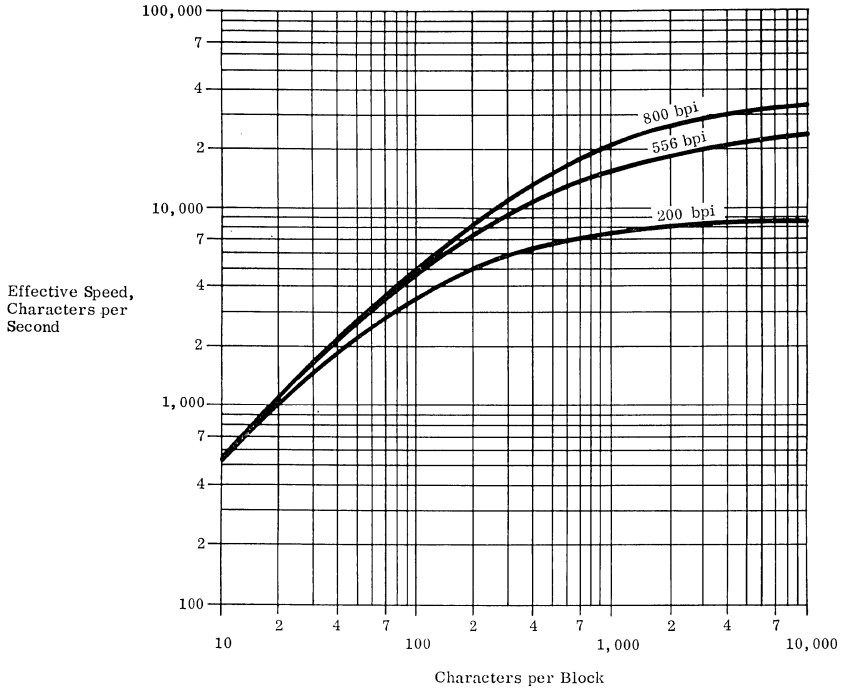
.731 Volumes handled: . . . . 2,400 feet per reel. For 1,000-character blocks: 5 million characters at 200 char/inch; 11.3 million characters at 556 char/inch; 14.4 million characters at 800 char/inch.
.732 Replenishment time: . . 0.5 to 1.0 minute.
.734 Optimum reloading period —
Uniservo VIC: . . . . . 11.2 minutes.
Uniservo VIIIC: . . . . 4 minutes.

.8 ERRORS, CHECKS, AND ACTION

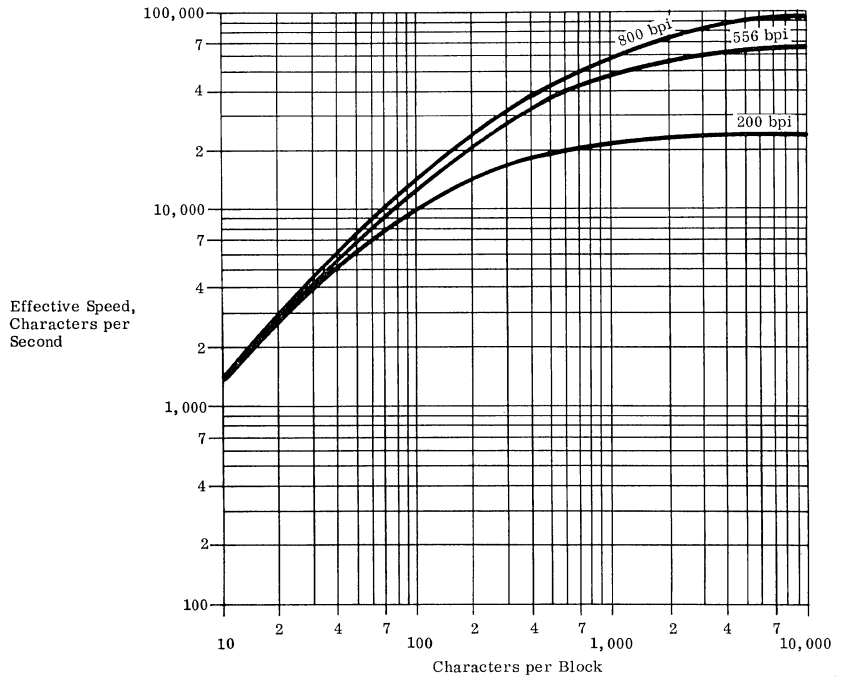
Error	Check or Interlock	Action*
Recording:	read-after-write parity check	set indicator and interrupt.
Reading:	lateral and longitudinal parity check	set indicator and interrupt.
Invalid code:	all codes are valid.	
Exhausted medium:	check	set indicator and interrupt.
Imperfect medium:	read-after-write parity check	set indicator and interrupt.
Timing conflicts:	check	set indicator and interrupt.

* Indicators are contained in the Status Word sent to core memory after an interrupt.

EFFECTIVE SPEED: UNISERVO VIC TAPE HANDLER



EFFECTIVE SPEED: UNISERVO VIIIC TAPE HANDLER



INPUT-OUTPUT: UNIVAC 1004

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 Processor; Models I, II, and III. UNIVAC 1004 Adapter.

.12 Description

The UNIVAC 1004 is a small, plugboard-programmed computer with 961 or 1,922 positions of core storage. It can be connected to a UNIVAC 1108 computer system by means of the 1004 Adapter, enabling transmission of data, in one direction at a time, between the 1108's core storage and the 1004's core storage. The 1004 can provide data editing, code translation, and similar data manipulation facilities independently of the 1108 program. All operations must be initiated by the 1108 program; i.e., the UNIVAC 1004 cannot act as an independent inquiry station for the 1108. When it is not in use as an on-line peripheral subsystem for the 1108, the UNIVAC 1004 can be used as an off-line data processor, under sole control of its plugboard wiring.

Some of the important characteristics of the 1004 are:

- Plugboard programming.
- 961 or 1,922 positions of core storage.
- 31, 47, or 62 program steps.
- 8-μsec cycle time for the 1004 Model I; 6.5-μsec cycle time for Models II and III.
- Editing and decimal arithmetic facilities.
- Maximum card reading rate of 400 or 615 cards per minute, depending upon the model.
- Maximum printing rate of 400 or 600 lines per minute, depending upon the model.
- 132 alphanumeric printing positions.
- 63-character printing set.
- Optional card punch — 200 cards per minute.
- Punched paper tape units available — 400 char/sec reading and 110 char/sec punching.
- One or two magnetic tape units can be connected: up to 33,664 characters per second at densities of 200, 556, or 800 characters per inch.

For more detailed information on the capabilities and performance of the UNIVAC 1004, see Computer System Report 770.

Data is transmitted one word at a time to or from the 1108. Except during interprocessor data transmission, the 1004 operates independently. The 1004 Subsystem requires one UNIVAC 1108 input-output channel and can operate simultaneously with all other peripheral subsystems.

INPUT-OUTPUT: DATA COMMUNICATIONS SUBSYSTEMS

.1 GENERAL

.11 Identity: . . . . . Communication Terminal Module Controller (CTMC).
Channel Scanner/Selector.
Word Terminal Synchronous (WTS).
Communication Terminal Synchronous (CTS).

.12 Description

UNIVAC offers a standard line of data communications equipment for use with UNIVAC 418, 490 Series, or 1100 Series computer systems; different interfaces are provided for connection to the various computers. Included in this line are a multiline controller capable of handling up to 32 full-duplex narrow-band or voice-band lines, and two single-line controllers capable of handling one full-duplex voice-band or broad-band line.

.121 Multiline Controller

UNIVAC has recently changed the pricing policy and nomenclature for its Standard Communications Subsystem. The Communication Multiplexor is now called the Communication Terminal Module Controller (CTMC). Four Communication Line Terminals (CLT's) are now grouped into one Communication Terminal Module (CTM). The CLT-Parallel Input and Output and CLT Automatic Dialing terminals retain the same names. Savings of up to 50% in communications equipment costs can be realized in fully-expanded subsystems containing one CTMC when compared to the previous Standard Communications Subsystem prices.

Transmission adapters are available for handling a wide range of communications facilities; see Table I. The CTMC contains 32 input and 32 output positions. The number of positions required by each adapter is specified in Table I. The Communications Subsystem is physically contained in two cabinets; one contains the power supply and communication lines interfaces, and the other contains the multiplexor, the transmission adapters, and timing clocks. The second cabinet contains space for accommodating 16 modules. Each module consists of one of the following:

- One Low-Speed CTM,
- One Medium-Speed CTM,
- One High-Speed CTM,
- One to four CLT-Automatic Dialing Adapters, or
- One module containing up to two Parallel Input Adapters and up to two Parallel Output Adapters.

One CLT-Dialing is required for each line on which the automatic dialing function is desired.

An internal clock is required for some adapters; other adapters use external timing signals from the associated data set. A maximum of six output clocks can be included within the second cabinet. All output adapters operating at the same speed can utilize the same clock, but each input adapter has its own clock. Adapters within the same module can operate at different speeds.

Although each Communications Subsystem fully occupies the input-output channel to which it is

TABLE I: TRANSMISSION ADAPTER CHARACTERISTICS

Unit	Positions Required		Code Level, (Bits/char)	Mode	Timing	Speed
	Input	Output				
Low-Speed CTM	2	2	5, 6, 7, or 8	Bit serial	Asynchronous; internal	Up to 300 bits/sec.
Medium-Speed CTM	2	2	5, 6, 7, or 8	Bit serial	Asynchronous; internal	Up to 1,600 bits/sec.
CLT-Parallel Input	1	0	Up to 8	Bit parallel	Timing signal; external	Up to 75 char/sec.
CLT-Parallel Output	0	1	Up to 8	Bit parallel	Timing signal; internal	Up to 75 char/sec.
High-Speed CTM	2	2	5, 6, 7, or 8	Bit serial	Synchronous; external	2,000 to over 5,000 bits/sec.
CLT-Dialing	0	1	4	Bit parallel	Timing signals; external	Determined by common carrier.

Note: "Asynchronous" means that start and stop bits are sent with each character to establish timing; "Synchronous" means that timing characters are sent with each message to establish timing.

.121 Multiline Controller (Contd.)

connected, up to four CTMC's can be connected to a single channel by means of a Scanner/Selector Unit. Thus, a maximum of 256 simplex lines or 128 half-duplex or full-duplex lines can be serviced by a single input-output channel.

A special communications feature, the Externally Specified Index (ESI), allows a number of communications lines to operate concurrently over a single input-output channel by providing automatic sorting of incoming data and automatic collation of outgoing data.

When the Communications Subsystem is used, one core storage location is reserved for each communication line (two for a full-duplex line). These locations contain the ESI Access Control Words. In addition, two alternating core storage buffer areas are assigned to each line. The size and locations of these buffer areas can be varied by the program.

A 15-bit code is transmitted along with each message character leaving or entering the Central Processor. This code, called the ESI, identifies the communication line and the multiplexor. The ESI references an Access Control Word, which in turn indicates the location to or from which the character is to be sent. When a buffer has been filled (or emptied), an internal interrupt occurs, and the Access Control Words are modified by the operating system to reference the alternate buffer. Incoming and outgoing data are stored two characters per 1108 word.

All Communication Line Terminals can be active simultaneously, subject to the maximum data rates of the computer and the CTMC. Messages can be transmitted or received while any other peripheral subsystem is operating and while the Central Processor is computing.

The maximum data rate of the CTMC is determined by the time required for scanning, the time required to transfer each character to the computer, and certain characteristics of the adapters. The resulting maximum allowable communications data rate for the CTMC, based on 8 bits per character (including start and stop bits, if any), when used with an 1108 is 51,000 characters per second. For other character codes, an approximate maximum character rate can be obtained by multiplying the above figure by 7N/8(N-1), where N is the total number of bits (including start and stop bits, if any) per character.

.122 Single-Line Controllers

UNIVAC offers two single-line controllers, each of which is capable of controlling communications between an 1108 computer and a remote terminal at 2,000 bits per second over the public telephone network, at 2,400 bits per second over a leased voice-band line, or at 40,800 bits per second over a leased broad-band facility such as Telpak A. These two controllers, the Word Terminal Synchronous (WTS) and the Communication Terminal Synchronous (CTS), are essentially two versions of the same unit.

Both versions transmit data serially by bit in a synchronous mode. The WTS transmits or receives 6 data bits and 1 parity bit per character; the CTS transmits or receives 5, 6, 7, or 8 data bits and 1 parity bit per character.

The WTS transfers data between itself and the computer one word (6 characters) at a time and performs both character and message parity checking. The CTS transfers data to or from the computer one character at a time and performs only character parity checking. The WTS imposes a smaller demand upon the central processor than the CTS, but is also more expensive.

Both the WTS and the CTS can be equipped for unattended answering and automatic dialing (when connected to the public telephone network).

These controllers have been used to connect a variety of UNIVAC computers with remote UNIVAC 1004 Card Processors. Each controller fully occupies one input-output channel. The maximum demand on the 1108's core memory for communications at 340 characters per second (6 data bits per character) is only 0.026 percent for the CTS and 0.004 percent for the WTS. The memory demands at other data transmission speeds are proportionate.

SIMULTANEOUS OPERATIONS

.1 GENERAL

UNIVAC 1108 computer systems possess powerful capabilities for overlapped operations. A single-processor 1108 system without Multiple Module Access Units can concurrently execute:

- One machine instruction; and
- One operand fetch if the operand is located in Control Memory or in a different memory module from the instruction being executed; and
- One positioning operation per Fastrand II Storage Unit; and
- One magnetic tape rewind operation per tape handler; and
- One input or output data transfer or search operation per I/O Channel — except for a Console Subsystem (up to four console input-output operations per subsystem), a High-Speed Printer Subsystem (up to four print operations per subsystem), and a Communications Subsystem (in which multiple lines can be active simultaneously).

In the above type of configuration, one or two core memory references can be made at the same time, depending upon the locations addressed. Overlapping of I/O data transfers is accomplished by sharing core storage cycles among the active I/O channels and the Central Processor.

A Multiple Module Access Unit (MMA) enables up to five Central Processors or I/O Controllers, in any combination, to be connected to one pair of memory modules (each module contains 32,768 words). Each memory module is independent, and any combination of modules can be accessed simultaneously. The MMA's provide the connections to allow multiple devices access to Core Memory.

The I/O Controller (I/OC) is an independent, wired-logic processor that provides functions similar to those of the I/O Control Logic section of the Central Processor, as described in Paragraph .2 of this section. The I/OC contains 256 36-bit words of Index Memory that serve the same function for the channels of the I/OC as the Input/Output Access Control Words in the Control Memory of the 1108 Central Processor. More than one Access Control Word can be associated with each I/O channel, and these Control Words can be "chained" together to provide scatter-read and gather-write capabilities. An additional 256-word module of Index Memory can be incorporated to provide additional Buffer Control Words for data communications devices.

In a single-processor 1108 configuration with Multiple Module Access Units and Input/Output Controllers, one additional simultaneous reference to core memory can be made by each I/O Controller, provided that each memory reference is to a separate memory module.

A multi-processor 1108 configuration (1108-II) requires the use of MMA's and also one or two I/O Controllers (if the standard operating system is to be used). An 1108-II configuration can concurrently execute:

- One machine instruction per processor; and
- One operand fetch per processor and one memory reference per I/O controller, subject to a maximum of one reference per memory module and eight in all; and
- The other operations listed above for the single-processor configuration.

The capability for multiple simultaneous accesses to core memory reduces the frequency of conflicts due to two or more Central Processors and/or I/O Controllers requesting access to the same memory module during the same cycle. Due to the impossibility of making optimum address assignments for every circumstance, the amount of effective overlapping will be degraded somewhat from the theoretical maximum. The amount of degradation depends on the mix of programs being executed and will vary with time.

.2 INPUT-OUTPUT

All input-output operations are handled in the same general manner. A Function Word is transmitted to a peripheral device or controller and specifies the device and the operation to be performed. The Access Control Word, located either in the Central Processor's Control Memory or in an I/O Controller's Index Memory, specifies the number of words

.2 INPUT-OUTPUT (Contd.)

to be transferred and the address to or from which the current data word is to be transferred. This address is automatically incremented, decremented, or left unchanged, depending on the setting of bits in the Access Control Word. The word count is decremented for each word transferred, and the I/O operation is terminated when the word count reaches zero. An interrupt can optionally be generated at the end of an I/O operation.

One 36-bit word of data at a time is transferred between Core Memory and any peripheral subsystem except a Punched Paper Tape Subsystem, a Communications Subsystem, Communications Terminal Synchronous Unit, and a Console I/O Typewriter. All four of these subsystems transfer one character at a time. Due to the efficiencies of using the Control Memory or Index Memory to hold the Access Control Words, each data transfer of one word or one character requires only one core storage cycle.

The overall input-output data transfer rate is limited by the capability of the I/O channels and the Central Processor or I/O Controller. Each I/O channel in either a Central Processor or an I/OC can handle up to 250,000 words or characters per second, depending on whether the transfer mode is by word or by character. The maximum combined data rate for all channels of either a processor or an I/OC is 1.33 million words or characters per second, again depending on the transfer mode.

Table I is a tabulation of the demands on core memory imposed by the various UNIVAC 1108 peripheral subsystems.

TABLE I: I/O DEMANDS ON 1108 CORE MEMORY

Peripheral Subsystem	Transfer Mode	Peak Data Transfer Rate, char/sec	Demand on Core Memory, % (1)
FH-432 Drum	word	1,440,000	18.0
FH-1782 Drum	word	1,440,000	18.0
Fastrand II Storage Unit	word	153,750	1.9
Uniservo VIIIC Tape Handler	word	96,000	1.2
Uniservo VIC Tape Handler	word	34,200	0.43
Punched Card Subsystem —			
Reading (2)	word	1,400	0.016
Punching (2)	word	1,400	0.005
Printer Subsystem (2)	word	4,167	0.025
Punched Tape Subsystem —			
Reading	character	400	0.03
Punching	character	110	0.008
Communications Subsystem	character	51,000	3.8
Word Terminal Synchronous	word	5,800	0.072
Communications Terminal Synchronous	character	5,800	0.43
Console	character	10	<0.001

(1) This column indicates the demand on the particular memory module involved in the I/O data transfer operation. In configurations with two-way memory interleaving, half of the indicated demand will apply to each of the two modules involved. If the peripheral subsystem is operating over a Central Processor channel, the memory demand will be reflected on the processor.

(2) For these devices, the peak data transfer rate is the rate at which data is transferred between the peripheral device's buffer and core memory. The indicated demands are averaged over the total cycle times when operating at peak speeds. The instantaneous demands based on the buffer transfer rates will be significantly higher.

INSTRUCTION LIST

	Instruction Code		Mnemonic	Instruction
	f	j		
	00	-	-	Illegal Code
	01	0-15	SA	Store A
	02	0-15	SN	Store Negative A
			SNA	
	03	0-15	SM	Store Magnitude A
			SMA	
	04	0-15	SR	Store R
	05	0-15	SZ	Store Zero
	06	0-15	SX	Store X
	07	-	-	Illegal Code
	10	0-17	LA	Load A
	11	0-17	LN	Load Negative A
			LNA	
	12	0-17	LM	Load Magnitude A
			LMA	
	13	0-17	LNMA	Load Negative Magnitude A
	14	0-17	AA	Add to A
	15	0-17	ANA	Add Negative A
	16	0-17	AM	Add Magnitude to A
			AMA	
	17	0-17	ANM	Add Negative Magnitude to A
			ANMA	
	20	0-17	AU	Add Upper
	21	0-17	ANU	Add Negative Upper
	22	0-17	BT	Block Transfer
	23	0-17	LR	Load R
	24	0-17	AX	Add to X
	25	0-17	ANX	Add Negative to X
	26	0-17	LXM	Load X Modifier
	27	0-17	LX	Load X
	30	0-17	MI	Multiply Integer
	31	0-17	MSI	Multiply Single Integer
	32	0-17	MF	Multiply Fractional
	33	-	-	Illegal Code
	34	0-17	DI	Divide Integer
	35	0-17	DSF	Divide Single Fractional
	36	0-17	DF	Divide Fractional
	37	-	-	Illegal Code
	40	0-17	OR	Logical OR
	41	0-17	XOR	Logical Exclusive OR
	42	0-17	AND	Logical AND
	43	0-17	MLU	Masked Load Upper
	44	0-17	TEP	Test Even Parity
	45	0-17	TOP	Test Odd Parity
**	46	0-17	LXI	Load X Increment
	47	0-17	TLEM	Test Less or Equal to Modifier
			TNGM	Test Not Greater than Modifier

	Instruction Code		Mnemonic	Instruction
	f	j		
	50	0-17	TZ	Test for Zero
	51	0-17	TNZ	Test for Non Zero
	52	0-17	TE	Test for Equal
	53	0-17	TNE	Test for Not Equal
	54	0-17	TLE	Test for Less or Equal
			TNG	Test for Not Greater
	55	0-17	TG	Test for Greater
	56	0-17	TW	Test for Within Range
	57	0-17	TNW	Test for Not Within Range
	60	0-17	TP	Test for Positive
	61	0-17	TN	Test for Negative
	62	0-17	SE	Search for Equal
	63	0-17	SNE	Search for Not Equal
	64	0-17	SLE	Search for Less or Equal
			SNG	Search for Not Greater
	65	0-17	SG	Search for Greater
	66	0-17	SW	Search for Within Range
	67	0-17	SNW	Search for Not Within Range
	70	+	JGD	Jump on Greater and Decrement
	71	00	MSE	Mask Search for Equal
	71	01	MSNE	Mask Search for Not Equal
	71	02	MSLE	Mask Search for Less or Equal
			MSNG	
			MDNH	Mask Search for Not Greater
	71	03	MSG	Mask Search for Greater
	71	04	MSW	Masked Search for Within Range
	71	05	MSNW	Masked Search for Not Within Range
**	71	06	MASL	Masked Alphanumeric Search for Less or Equal
**	71	07	MASG	Masked Alphanumeric Search for Greater
**	71	10	DA	Double Precision Fixed Point Add
**	71	11	DAN	Double Precision Fixed Point Add Negative
**	71	12	DS	Double Store A
**	71	13	DL	Double Load A
**	71	14	DLN	Double Load Negative
**	71	15	DLM	Double Load Magnitude
**	71	16	DJZ	Double Precision Zero Jump
**	71	17	DTE	Double Precision Test Equal
*	72	00		Illegal Code
	72	01	SLJ	Store Location and Jump
	72	02	JPS	Jump on Positive and Shift
	72	03	JNS	Jump on Negative and Shift
	72	04	AH	Add Halves

*These codes represent different instructions in the UNIVAC 1107 (see Section 784:121).
**These instructions are not included in the UNIVAC 1107's repertoire.

	Instruction Code f	Instruction Code j	Mnemonic	Instruction
	72	05	ANH	Add Negative Halves
	72	06	AT	Add Thirds
	72	07	ANT	Add Negative Thirds
	72	10	EX	Execute
*	72	11	ER	Executive Return
	72	12		Illegal Code
**	72	13	PAIJ	Prevent All Interrupts and Jump
**	72	14	SCN	Store Channel Number
**	72	15	LIF	Load Processor State Register
**	72	16	LSL	Load Storage Limits Register
	72	17		Illegal Code
	73	00	SSC	Single Shift Circular
	73	01	DSC	Double Shift Circular
	73	02	SSL	Single Shift Logical
	73	03	DSL	Double Shift Logical
	73	04	SSA	Single Shift Algebraic
	73	05	DSA	Double Shift Algebraic
	73	06	LSC	Load Shift and Count
**	73	07	DLSC	Double Load Shift and Count
**	73	10	LSSC	Left Single Shift Circularly
**	73	11	LDSC	Left Double Shift Circularly
**	73	12	LSSL	Left Single Shift Logical
**	73	13	LDSL	Left Double Shift Logical
**	73	14	ISI	Initiate Synchronous Interrupt
**	73	15	SIL	Select Interrupt Module
**	73	16	LCR	Load Channel Select Register
**	73	17		Illegal Code
	74	00	JZ	Jump on Zero
	74	01	JNZ	Jump on Non Zero
	74	02	JP	Jump on Positive
	74	03	JN	Jump on Negative
	74	04	JK	Jump on Keys
			J	Jump
	74	05	HKJ	Halt on Keys and Jump
			HJ	Halt and Jump
	74	06	NOP	No Operation
	74	07	AAIJ	Allow all Interrupts and Jump
	74	10	JNB	Jump on No Low Bit
	74	11	JB	Jump on Low Bit
	74	12	JMGI	Jump Modifier Greater and Increment
	74	13	LMJ	Load Modifier and Jump
	74	14	JO	Jump on Overflow
	74	15	JNO	Jump on No Overflow
	74	16	JC	Jump on Carry
	74	17	JNC	Jump on No Carry
	75	00	LIC	Load Input Channel
	75	01	LICM	Load Input Channel and Monitor
	75	02	JIC	Jump on Input Channel Busy
	75	03	DIC	Disconnect Input Channel
	75	04	LOC	Load Output Channel
	75	05	LOCM	Load Output Channel and Monitor
	75	06	JOC	Jump on Output Channel Busy
	75	07	DOC	Disconnect Output Channel
	75	10	LFC	Load Function in Channel
	75	11	LFCM	Load Function in Channel and Monitor
	75	12	JFC	Jump on Function in Channel
	75	13	AFC	Allow Function in Channel
	75	14	AACI	Allow All Channel Interrupts
	75	15	PACI	Prevent All Channel Interrupts
	76	00	FA	Floating Add
	76	01	FAN	Floating Add Negative
	76	02	FM	Floating Multiply
	76	03	FD	Floating Divide
	76	04	LUF	Load and Unpack Floating
	76	05	LCF	Load and Convert to Floating
	76	06	MCDU	Magnitude of Characteristic Difference to Upper
	76	07	CDU	Characteristic Difference to Upper
**	76	10	DFA	Double Precision Floating Add
**	76	11	DFAN	Double Precision Floating Add Negative
**	76	12	DFM	Double Precision Floating Multiply
**	76	13	DFD	Double Precision Floating Divide
**	76	14	DFU	Double Load & Unpack Floating
**	76	15	DFP	Double Load & Convert to Floating
**	76	16	FEL	Floating Expand and Load
**	76	17	FCS	Floating Compress and Store
	77	0-17		Illegal Code

*These codes represent different instructions in the UNIVAC 1107 (see Section 784:121).
**These instructions are not included in the UNIVAC 1107's repertoire.

COMPATIBILITY: WITH UNIVAC 1107

.1 GENERAL

.11 The UNIVAC 1108 is largely compatible with its slower predecessor, the UNIVAC 1107, but programs written for an 1107 will, in general, need to be reassembled or recompiled before they can be executed on an 1108 under control of the 1108 Executive System.

UNIVAC states that most 1107 object programs will run directly on an 1108 under control of the modified EXEC II operating system provided as part of the interim software package described in Paragraph 785:011.31. Significant exceptions include certain COBOL and FORTRAN programs. The 1107 compilers for these source languages use "illegal operation code" interrupts for entry into some standard functions and subroutines, such as FORTRAN double-precision and complex arithmetic functions. Such programs will have to be recompiled using 1108 compilers.

UNIVAC also states that virtually all 1107 source-language programs can be assembled or compiled on a UNIVAC 1108, utilizing the 1108 compilers, with few, if any, difficulties in compilation or execution. A special translator will be provided for converting 1107 source programs written in SLEUTH I assembly language into SLEUTH II source coding. SLEUTH II and the 1108 Assembly language use the same mnemonic operation codes, whereas SLEUTH I uses completely different mnemonics.

The major areas of incompatibility between the 1107 and the 1108 include:

- The larger core storage of the 1108. Addressing in the 1107 was performed modulo the system's memory size, which was at most 65,536 words.
- A different memory protection technique in the 1108. The 1108 utilizes basing registers in generating effective addresses. This addressing technique and other factors led to the adoption of a different relocatable coding arrangement for the 1108.
- Different control instructions and techniques in the 1108. The 1108 has a set of reserved instructions which provide increased facilities for controlling the computer. The operation codes for this set of instructions partially overlap the 1107's operation codes; i.e., in some instances a particular operation code does not have the same function in the 1107 as in the 1108. In addition, the technique for handling I/O interrupts is implemented in a different manner in the 1108, although it is functionally similar.

Control routines or programs that do not utilize the 1107 EXEC II operating system will need to be recoded. Programs utilizing "memory wrap-around" can be accommodated by setting a particular bit in the Processor State Register, which forces the 1108 to perform addressing modulo 65,536. The user may, of course, desire to recode some programs to take advantage of the increased facilities of the 1108 for performing double-precision arithmetic. A more detailed description of the new hardware features of the 1108 Central Processor can be found in Paragraph 785:051.12.

.2 CONVERSION OF DATA

.21 Punched Card Data

Existing UNIVAC 1107 punched card files can be used without modification with UNIVAC 1108 systems, provided that the punched card input-output devices for both systems use the same type of cards (i.e., 80-column or 90-column).

.22 Magnetic Tape Files

Three different, non-compatible tape formats are used in the magnetic tape units available for the 1107. If the same tape units are carried over to the 1108 system, no problems will be experienced and magnetic tape files will not have to be converted. The following table shows the compatibility relationships between the various Uniservo Tape Handlers; a model listed on the left-hand side is format-compatible only with the models listed in the corresponding group on the right-hand side.

Uniservo Model	Compatible Models
IIA	IIA
IIIA	IIIA
IIIC*, IVC, VIC (7-channel), VIIIC (7-channel)	IIIC*, IVC, VIC (7-channel), VIIIC (7-channel)
VIC (9-channel), VIIIC (9-channel)	VIC (9-channel), VIIIC (9-channel)

.23 Magnetic Drum Files

If the same 1107 Magnetic Drums are not carried over to the 1108 system, the information on the drums will need to be transferred. This can usually be done by dumping the drums onto magnetic tape and reloading the new drums from tape. In this case, see also Paragraph .22, above.

.24 Collating Sequence

The 1108's collating sequence is the same as that of the 1107.

.3 CONVERSION OF PROGRAMS

In general, all programs written for an 1107 will need to be reassembled or recompiled prior to execution on an 1108 under the 1108 operating system because of the different relocatable coding techniques used in the two systems. For the most part, no changes will be required in source programs written in FORTRAN, COBOL, or SLEUTH II

* The Uniservo IIIC Tape Handler cannot operate at 800 bits/inch.

.3 CONVERSION OF PROGRAMS (Contd.)

Assembly Language. Changes may be desirable, however, to take advantage of language extensions and added hardware capabilities. Programs coded in SLEUTH I Assembly Language will have to be recoded or translated into SLEUTH II source language coding; see Paragraph .11. User-coded control routines will need to be completely recoded due to the different control instructions and techniques in the 1108.

See Paragraph 785:011.31, in the Introduction to this report, for a discussion of the interim situation that will exist until the complete 1108 software package is delivered in the second quarter of 1966.

.4 CONVERSION OF PERSONNEL

Personnel should experience little difficulty in moving from an 1107 installation to an 1108 installation because of the great similarities in hardware, software, and operating procedures. Probably the only major difficulty will be the necessity for SLEUTH I programmers to learn a completely new set of mnemonics in order to use the 1108 Assembly Language. Of course, the additional capabilities of the 1108 hardware and software will demand more systems planning effort to obtain maximum efficiency of machine usage.

.5 OPERATING PROCEDURES

Although not identical, the operating procedures for the 1108 are similar in concept to the procedures for the 1107. Operator communications with the operating system and directives to the system are performed via a console input-output typewriter in both systems. The cathode-ray-tube visual display console used in multiprocessor (1108-II) configurations should present few difficulties for the operators.

DATA CODE TABLE

Internal Code (Octal)	Card Code	Character
00	7-8	@
01	12-5-8	[
02	11-5-8	]
03	12-7-8	#
04	11-7-8	Δ
05	(blank)	(space)
06	12-1	A
07	12-2	B
10	12-3	C
11	12-4	D
12	12-5	E
13	12-6	F
14	12-7	G
15	12-8	H
16	12-9	I
17	11-1	J
20	11-2	K
21	11-3	L
22	11-4	M
23	11-5	N
24	11-6	O
25	11-7	P
26	11-8	Q
27	11-9	R
30	0-2	S
31	0-3	T
32	0-4	U
33	0-5	V
34	0-6	W
35	0-7	X
36	0-8	Y
37	0-9	Z

Internal Code (Octal)	Card Code	Character
40	12-4-8	)
41	11	-
42	12	+
43	12-6-8	<
44	3-8	=
45	6-8	>
46	2-8	&
47	11-3-8	$
50	11-4-8	*
51	0-4-8	(
52	0-5-8	%
53	5-8	:
54	12-0	?
55	11-0	!
56	0-3-8	, (comma)
57	0-6-8	\
60	0	0
61	1	1
62	2	2
63	3	3
64	4	4
65	5	5
66	6	6
67	7	7
70	8	8
71	9	9
72	4-8	' (apostrophe)
73	11-6-8	;
74	0-1	/
75	12-3-8	.
76	0-7-8	□
77	0-2-8	≠ (or stop)

PROBLEM ORIENTED FACILITIES

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . .none.

.12 Simulation by Other Computers: . . . . . .none.

.13 Data Sorting and Merging

1108 SORT/MERGE

Reference: . . . . . .UNIVAC preliminary information.
Record size: . . . . . .limited only by available storage; variable-length records can be sorted.
Block size: . . . . . .variable by full words up to 1,000 words maximum.
Key size: . . . . . .no limit on key size; maximum of 40 keys per record.
File size: . . . . . .no limit.
Number of tape units: . . . . . .zero to all (all tape units used in the same sort must be of the same type; e.g., Uniservo VIC).
Date available: . . . . . third quarter, 1966.
Description:

The UNIVAC 1108 SORT/MERGE is a generalized subroutine which is used in conjunction with a series of parameter lists and input-output routines to produce a sort program or a sort routine within a larger program. A sort routine can be incorporated into any 1108 source-language program. The sort program is generated at load time from specifications contained in control statements in the control stream or within a program. Specifications include the number of magnetic tapes to be used (if any), the amount of core storage to be used, and the amount of magnetic drum storage to be used (if any). In general, the disordered input file and the ordered output file can be on any combination of 1108 peripheral devices. If sufficient drum storage is available, the entire sort can take place between core storage and magnetic drum storage.

Files can be sorted into either ascending or descending order. The internal collation sequence can be used, or a different one can be specified by means of a table. Key fields can be specified to be in any one of five forms, with translation occurring prior to key comparison and retranslation into the original form prior to output. The possible forms include unsigned binary, UNIVAC signed binary (1108 internal fixed-point or floating-point format), IBM signed binary (IBM 7090/7094 fixed-point format), alphanumeric, and signed decimal. If desired, a programmer can code his own comparison algorithm.

.14 Report Writing: . . . . . none

.15 Data Transcription: . . . routines for performing data transcription are included in the Executive System; see Section 785:191.

.16 File Maintenance: . . . . . routines for performing file maintenance are included in the Executive System; see Section 785:191.

.17 BEEF (Business and Engineering Enriched FORTRAN)

BEEF consists of two groups of subroutines developed by the Westinghouse Electric Corporation's Baltimore Defense and Space Center to overcome FORTRAN's limitations as a data processing language and to enhance its capabilities as a scientific processing language. These routines are available to programmers using any 1108 source language.

BEEF Data Processing Routines

This group consists of 60 subroutines primarily concerned with data manipulation. Facilities are provided for:

- Moving whole data words — 6 subroutines.
- Moving characters and fields — 5 subroutines.
- Formatting — 7 subroutines.
- Decision-making — 7 subroutines.
- Data conversion — 6 subroutines.
- Report control — 2 subroutines.
- Input-output control — 6 subroutines.
- Sorting — 1 subroutine.
- Miscellaneous, including word-field and character-field sequence comparisons — 20 subroutines.

BEEF Math-Pack

This group consists of 64 subroutines primarily concerned with numerical calculations. Facilities are provided for:

- Interpolation — 6 subroutines.
- Solution of polynomial equations — 6 subroutines.
- Differentiation — 3 subroutines.
- Matrix manipulation — 24 subroutines.
- Numerical integration — 5 subroutines.
- Solution of ordinary differential equations — 5 subroutines.

.17 BEEF (Business and Engineering Enriched FORTRAN) (Contd.)

- Solution of systems of linear and non-linear equations — 4 subroutines.
- Miscellaneous, including Fourier series, random number generation, polynomial evaluation, and evaluation of Bessel functions — 11 subroutines.

.18 Stat-Pack Routines

The Stat-Pack Routines consist of a group of 90 subroutines oriented toward statistical calculations. Facilities are provided for:

- Descriptive statistics — 30 subroutines.
- Tests on statistical parameters — 16 subroutines.
- Analysis of variance — 13 subroutines.
- Regression and correlation analysis — 3 subroutines.
- Analysis — 1 subroutine.
- Time series analysis — 11 subroutines.
- Multivariate analysis — 5 subroutines.
- Distribution functions — 10 subroutines.
- Plotting — 1 subroutine.

.19 Application Packages

.191 Linear Programming System

This package, coded in FORTRAN V and Assembly Language, provides 1108 users with a comprehensive system for evaluating many manufacturing cost and product distribution problems. Up to 2,047 rows can be accommodated, and extensive use is made of magnetic drums for intermediate storage. Computations can be made in either single- or double-precision arithmetic. Vector levels can be specified and coefficients can be modified. Long runs can be split with restart procedures. Post-optimal parametric programming or a complete tableau can be obtained. The final output includes the objective function value, optimal basis, and vector levels. The Linear Programming System is incorporated as part of the 1108 Executive System and is initiated by control statements in the control stream.

.192 APT III (Automatic Programmed Tools)

APT III is a problem-oriented language directed toward computer-assisted programming of numerically-controlled machine tools, flame cutters, drafting equipment, and similar equipment. The present APT III language was written by the Aerospace Industries Association and further developed by the Illinois Institute of Technology Research Institute. APT III as implemented for the 1108 conforms to these specifications. The output from the APT III translator is in a generalized form which is not directly applicable to any particular machine. UNIVAC states that a post-processor can be furnished, subject to negotiation, to interface with any particular machine.

.193 PERT

The UNIVAC 1108 PERT/COST system is a generalized applications program that adheres to the framework provided by the "DOD/NASA Guide to PERT/COST System Design." PERT, in general, is a technique for handling the scheduling of jobs or procedures with a large number of interrelated tasks and for identifying the "critical path" or limiting factors. As conditions change, new PERT evaluations can be made to determine the effect on the overall job. PERT/COST adds the capability for performing cost estimates and the effect on costs due to deviations from the schedule.

PROCESS ORIENTED LANGUAGE: 1108 COBOL

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 COBOL.

.12 Origin: . . . . . UNIVAC; based on the 1107 COBOL Compiler originally developed by Computer Sciences Corporation.

.13 Reference: . . . . . UNIVAC 1108 COBOL Programmer's Reference Manual, Publication UP-4048.

.14 Description

COBOL-61 is the most widely implemented pseudo-English common language for business applications. The 1108 COBOL language represents a nearly complete implementation of Required COBOL-61 (though there are a few omissions), along with many of the electives and several useful extensions. The deficiencies of 1108 COBOL with respect to Required COBOL-61, the extensions, and the facilities of Elective COBOL-61 that have and have not been implemented are tabulated at the end of this description.

Useful extensions to the COBOL-61 language include the SORT facility, a MONITOR verb that facilitates program testing, random-accessing facilities, and a facility that permits flexible control of the vertical format of printed output. A non-standard version of the Report Writer facility is also included. See Paragraph .143 for more details on these extensions. No COBOL language facilities are provided for control of data communications.

The 1108 COBOL language is an extension of the UNIVAC 1107 COBOL language, which is described in Section 784:161. The electives implemented in 1108 COBOL but not in 1107 COBOL are indicated by asterisks in the table in Paragraph .144. These electives include the COMPUTE and INCLUDE verbs, many of the verb options, and the complete range of conditionals. In addition, 1108 COBOL includes the standard implementation of the SORT verb and Library facilities. File and Record Descriptions and Procedure Division entries can be copied into the user's programs from the 1108 COBOL Library, but Environment Division entries cannot. The 1108 COBOL language does not include the SEQUENCED ON option in the File Description statement, which is implemented in 1107 COBOL.

Random (non-sequential) accessing of records stored on magnetic drums can be performed by using the standard COBOL calling sequence or, alternatively, by entering the Assembly language and working directly with the Executive System functions. Programmers who elect to use the Assembly language are responsible for the arrangement and construction of the drum files.

The elective verb ENTER, as implemented for the 1108, makes it possible to enter an independently-compiled Assembly-language, FORTRAN, COBOL, or other subprogram. Object programs can be segmented; but whereas Elective COBOL-61 specifies four different ways of handling segments according to their priorities, 1108 COBOL provides only two ways:

- Sections with assigned priorities of 1 through 49 will be present in core memory at all times.
- Sections with assigned priorities of 50 through 99 will be grouped into segments by priority number. One segment at a time will be loaded (in the order referenced) into a single core memory area whose size is equal to that of the largest segment.

Data items upon which arithmetic is to be performed can be represented internally in either decimal (6 bits per digit) or binary form by specifying USAGE IS COMPUTATIONAL or COMPUTATIONAL-1, respectively. Operands can be up to 18 decimal digits or 66 binary bits in length, but SIZE must be specified in equivalent 6-bit CHARACTERS in either case. When operands are longer than 36 bits, multiple-precision arithmetic must be performed. Arithmetic can be performed upon mixed COMPUTATIONAL and COMPUTATIONAL-1 items; radix conversion and point alignment will be performed automatically when necessary. None of the COBOL electives that provide for variable-length items and records (e.g., the BLOCK, SIZE, and PICTURE clause options) have been implemented.

The 1108 COBOL Compiler operates under control of the Executive System. COBOL programs can be compiled on any valid 1108 configuration. See Section 785:031, System Configuration, for the minimum 1108 configuration. Magnetic tape is not required for the compilation process. Compilation is divided into six logical phases. Documentation will consist of a source program listing, diagnostic messages, and an object program listing containing symbolic instructions, octal locations, and octal machine words, with interspersed references to the source program listing. Four different types of error diagnostics are included within the translator; they are interpreted as follows:

- Precautionary diagnostic - print warning message and continue compilation.
- Correctible error - make a reasonable attempt at correction, print explanatory message, and continue.
- Uncorrectible error - when a reasonable guess of the programmer's intent cannot be made, print message, reject the statement or clause, and continue.
- Destructive errors - when errors have multiplied to the point where it is probable that no more useful diagnostic information can be produced, terminate the compilation.

UNIVAC states that current tests indicate that an average compilation speed of about 4,000 to 5,000 statements per minute can be obtained. Source

..14 Description (Contd.)

program loading and object program output will be governed by the speed of the peripheral devices used. UNIVAC also states that there is no practical limit on the sizes of programs that can be compiled; additional core storage can be requested if needed during compilation.

.141 Availability

Language: . . . . . November, 1965.
Translator: . . . . . third quarter, 1966.

.142 Deficiencies with Respect to Required COBOL-61

Environment Division —

- SOURCE-COMPUTER, OBJECT-COMPUTER, and SPECIAL-NAMES paragraphs cannot be copied from the Library.

Data Division —

- The [integer-4 TO] option of the RECORD CONTAINS clause is not permitted; there is no provision for efficient handling of variable-length records; i.e., the compiler will consider all records to be the size of the largest record.
- The VALUE clause of the File Description entry can apply only to "IDENTIFICATION" or "ID," a specific item that appears in the standard label record.

.143 Extensions to COBOL-61

- The extended implementation of the SORT verb is included. This permits multiple sorts within a single program.
- A MONITOR verb provides dynamic printouts of the values of specific items as an aid to program testing and debugging.
- The operational symbol H can be used in a PICTURE clause to specify that the field is to be represented in one's complement binary form; the effect is the same as that of the clause USAGE IS COMPUTATIONAL-1.
- The optional clauses LINES-PER-PAGE, LINES-AT-TOP, LINES-AT-BOTTOM, and LINE-SPACING in the File Description entry provide vertical format control of printed output.
- A Report Writer facility is included, but its implementation is non-standard.
- Random (non-sequential) accessing of records located in magnetic drum storage is implemented with the standard COBOL calling sequence.

(Contd.)

.144 COBOL-61 Electives Implemented (see 4:161.3)

No.	Elective	Comments
	Characters and Words	
1	Formula characters	Formulas are allowed.
2	Relationship characters	The symbols < , > , = are allowed.
3	Semicolon	A semicolon is in the character set.
4	Long literals	The maximum size is 132 characters.
	File Description	
*9	FILE CONTAINS	The approximate size of the file can be shown.
	Record Description	
*20	Conditional ranges	VALUES can be ascribed to conditionals.
	Verbs	
*22	COMPUTE	Algebraic formulas may be used.
24	ENTER	Non-COBOL languages can be used in a program.
*25	INCLUDE	Library routines are available automatically.
	Verb Options	
27	LOCK	A rewound tape can be optionally locked.
*28	MOVE CORRESPONDING	Commonly named items in a group can be handled together.
*29	OPEN REVERSED	Tapes can be read backwards.
30	ADVANCING	Specific paper advance instructions can be given.
*31	STOP provisions	Special numeric coded alphabetic displays.
*32	Formulas	Algebraic formulas may be used.
33	Operand size	Operands can be up to 18 digits.
*34	Relationship	IS EQUAL TO, EQUALS, EXCEEDS relationships are allowed.
*35	Tests	IF x IS NOT ZERO test is allowed.
*36	Conditionals	Implied subjects with implied objects are allowed.
*37	Complex conditionals	ANDs and ORs may be intermixed.
*38	Complex conditionals	Nested conditionals are permitted.
*39	Conditional statements	IF, SIZE ERROR, AT END, ELSE (OTHERWISE) may follow an imperative statement.
	Environment Division	
41	OBJECT-COMPUTER	Computer description can be given.
46	I-O-CONTROL	A rerun facility is available, but the full range is not implemented.
	Identification Division	
47	DATE-COMPILED	The current date is inserted automatically.
	Special Features	
48	Library	Library facilities for the procedure division are available.
49	Segmentation	Segmentation of programs is allowed (but implementation is non-standard).

*These electives are implemented in UNIVAC 1108 COBOL, but not in UNIVAC 1107 COBOL.

.145 COBOL-61 Electives Not Implemented (see 4:161.3)

No.	Elective	Comments
	Characters and Words	
5	Figurative constants	HIGH or LOW BOUND(S) are not available.
6	Figurative constants	HIGH or LOW VALUE(S) are not available.
7	Computer-name	No alternative object computers.
	File Description	
8	BLOCK CONTAINS	No range of block sizes can be given.
10	Label formats	Labels must be standard, omitted, or completely programmed.
11	SEQUENCED ON	No key fields can be given for sequencing.
12	HASHED	Hash totals cannot be created.
	Record Description	
13	Table-length	Lengths of tables and arrays must not vary.
14	Item-length	Variable-length items cannot be specified.
15	BITS option	Items cannot be specified in binary.
16	RANGE IS	Value range of items cannot be shown.
17	RENAMES	Alternative groupings of elementary items cannot be specified.
18	SIGN IS	No separate signs allowed.
19	SIZE clause	Variable-length items cannot be specified.
21	Label handling	Only standard labels (or none) may be used.
	Verbs	
23	DEFINE	The user cannot define new verbs.
26	USE	No non-standard auxiliary I/O error-handling or label-handling routines can be inserted.
	Environment Division	
40	SOURCE-COMPUTER	No computer description can be given.
42	SPECIAL-NAMES	The status conditions of hardware devices cannot be given special names by the program.
43	FILE-CONTROL	File naming and description of desired control method cannot be taken from the library.
44	PRIORITY IS	Priorities cannot be given.
45	I-O-CONTROL	Input-output control cannot be taken from the library.
46	I-O-CONTROL	A rerun facility is available, but the full range is not implemented.

PROCESS ORIENTED LANGUAGE: FORTRAN V

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 FORTRAN V.

.12 Origin: . . . . . Computer Sciences Corporation.

.13 Reference: . . . . . UNIVAC 1108 FORTRAN V Programmer's Reference Manual, Publication UP-4060.

.14 Description

The UNIVAC 1108 FORTRAN V language is an extension of the 1107 FORTRAN IV language developed by Computer Sciences Corporation. The 1108 FORTRAN V language contains all the facilities of 1107 FORTRAN IV (see Section 784:162) and of IBM 7090/7094 FORTRAN IV (see Section 408:162); this means that any legitimate source program written in UNIVAC 1107 or IBM 7090/7094 FORTRAN IV can be compiled by the 1108 FORTRAN V compiler. UNIVAC's FORTRAN V also contains all provisions of the FORTRAN language as proposed by the X.3.4.3 FORTRAN Group of the American Standards Association and as published in the Communications of the ACM, October 1964.

The extensions of 1108 FORTRAN V relative to IBM 7090/7094 FORTRAN IV are listed in Paragraph .143; a full description of the IBM 7090/7094 FORTRAN IV language can be found in Section 408:162. These extensions significantly increase the power and flexibility of the FORTRAN language, particularly in the areas of subscripting, mixed-mode arithmetic, and debugging.

As in 1107 FORTRAN, a variable may have up to seven subscripts, meaning that seven-dimensional arrays can be handled; 7090/7094 FORTRAN IV is limited to three dimensions. Furthermore, subscript expressions may have more complex forms in the 1108 version, though they are still limited to integer constants and variables. Use of the DEFINE statement permits subscripted subscripts to any level; this capability is not usually found in FORTRAN.

The possibilities for mixed-mode arithmetic, both among the operands of an arithmetic expression and between the left and right sides of an arithmetic statement, are much broader in 1108 FORTRAN. Among the four possible types of arithmetic operands — integer, real, double-precision, and complex — only double-precision and complex values may not be freely combined.

Input and output of data for testing purposes are facilitated by the NAMELIST statement, which assigns a name to a list of variables. The name of this list can be used in an input or output statement in place of a FORTRAN specification; standard formats are used for output. The input data need not be in a fixed format or order; the variables' names and their values are both included in the input. The input-output statements inserted only for testing purposes can be preceded by a parameterized DELETE statement. The changing of a single statement, the PARAMETER statement, and recompiling will then eliminate these input-output statements from the compiled program, while enabling them to be kept in the source program for possible future testing.

The LIFT translator can be used to translate existing FORTRAN II programs into equivalent 1107 FORTRAN IV source coding, which can then be compiled by the 1108 FORTRAN V compiler.

An extensive array of FORTRAN subroutines under the name of BEEF has been developed by Westinghouse Electric Corporation to expand the business data-handling capabilities of previous UNIVAC FORTRAN languages. These subroutines are available to the 1108 FORTRAN V programmer. A summary of the facilities offered by the BEEF subroutines can be found in the Problem Oriented Facilities Section, Paragraph 785:151.17.

Compilers

Two compilers are being developed for 1108 FORTRAN V. One, the "batch" compiler, is similar to the 1107 FORTRAN compiler; UNIVAC states that it will feature multiphase compilation at high compiling speeds and will produce highly efficient coding. The second, the "conversational" compiler, is intended for use by remote users submitting programs from remote data communications terminals; it will feature statement-by-statement execution, if desired, and extensive diagnostics.

The "batch" compiler operates under control of the Executive System and can be used on any valid 1108 configuration; see Section 785:031, System Configuration. Magnetic tape units are not required and are of no advantage in compilation. Documentation produced by the batch compiler includes a storage allocation map and a listing of the object program instructions in both symbolic and octal form, with corresponding source statements and diagnostic messages interspersed. UNIVAC expects the average compilation speed to be significantly faster than that of the highly-respected 1107 FORTRAN compiler; an average speed of 4,000 to 6,000 source statements per minute has been demonstrated by UNIVAC in tests. UNIVAC expects object program efficiencies to be, in general, "better than the average programmer can write in an assembly language," because of the optimizing features of the compiler.

As in the 1107, the batch compiler expects input and output data to be stored on the drum during execution of a program. The card-to-drum and drum-to-printer "symbionts" (see Executive, Section 785:191) handle the required data transcriptions. Other input and output devices can be utilized if the programmer desires. Source program input to the batch compiler can be from any 1108 peripheral device, including remote data

.14 Description (Contd.)

communications terminals. Object code output and listings can also be to any 1108 peripheral device.

The batch compiler is not re-entrant, so a separate "copy" of the compiler program must be loaded into core storage for each FORTRAN compilation in the current mix.

The "conversational" compiler will accept input source statements from a local or remote data communications terminal and produce generated object code, results of object-program execution, diagnostic comments, or combinations of these, at the option of the remote operator. Operations with the conversational compiler are performed in the demand mode of processing (see Paragraph 785:191.12). The remote programmer/operator can call for functions or subroutines from the batch compiler. The conversational compiler is written in re-entrant coding; i.e., the compiler program is never modified during execution, so all remote conversational FORTRAN activity can utilize the same physical copy of the compiler program. Separate source code, object code, and data areas are maintained for each program.

The conversational compiler will contain extensive diagnostic facilities including traces and snapshots. Typical applications of the conversational compiler will be to use the 1108 as a fast, powerful remote "calculator" or to prepare and debug programs later to be submitted to the batch compiler. Because of the interpretive, statement-by-statement operational mode of the conversational compiler, its object code efficiency will be significantly lower than that of the batch compiler.

The FORTRAN language initially acceptable by the conversational compiler will be a proper subset of the 1108 FORTRAN V language as described in this section. The primary limitations will be: no complex or logical arithmetic, no magnetic tape input-output, no provision for binary (odd-parity) files, and input-output via remote terminals only. UNIVAC states that the conversational FORTRAN language will eventually be expanded to include all of 1108 FORTRAN V.

.141 Availability

Language:. . . . . March 1966.
Compilers —
"Batch" compiler: . . second quarter, 1966.
"Conversational"
compiler:. . . . . third quarter, 1966.

.142 Restrictions Relative to IBM 7090/7094 FORTRAN IV (See Section 408:162)

Any valid program capable of being compiled on a 7090/7094 can be compiled on an 1108 with few, if any, changes or restrictions.

.143 Extensions Relative to IBM 7090/7094 FORTRAN IV (See Section 408:162)

Note that items (1) through (7) apply to UNIVAC 1107 FORTRAN as well; items (8) through (15) are currently unique to 1108 FORTRAN V. UNIVAC states that these features will eventually be incorporated into 1107 FORTRAN, with the exception of automatic type assignment (item 15).

(1) A variable may have up to seven subscripts, versus a maximum of three subscripts in IBM 7090/7094 FORTRAN IV.

(2) Subscripts must have the general form

$$\pm M_1 \pm M_2 \pm M_3 \ldots \pm M_i,$$

where each M may be an integer constant, an integer variable, or an expression of the form

$$n * K_1 * K_2 * \ldots K_j,$$

in which n is an integer constant and each K is an integer variable. Subscripts in IBM 7090/7094 FORTRAN IV are limited to the form n*k + n', where n and n' are unsigned integer constants and k is an integer variable. Therefore, the expression I + 2*J*K - 4 is a valid subscript in 1108 FORTRAN but not in 7090/7094 FORTRAN.

(3) The PARAMETER statement assigns specified integer values or integer variables to specified variables at compile time; e.g., PARAMETER I = 2 causes the integer 2 to replace I wherever it occurs in the source program. This facilitates the assignment of different values to frequently-referenced parameters in different compilations of the same program.

(4) Arithmetic operations (+, -, *, /) can be performed more freely upon operands of different types. Specifically, the following types of arithmetic operand pairs are permitted in 1108 FORTRAN but not in 7090/7094 FORTRAN IV:

REAL-INTEGER
COMPLEX-INTEGER
DOUBLE PRECISION-INTEGER

(5) In arithmetic statements, the following combinations of expressions (on the right side of the equal sign) and variables (on the left side) can be equated in 1108 FORTRAN, but not in 7090/7094 FORTRAN IV:

Variable on left	=	Expression on right
INTEGER		COMPLEX
REAL		COMPLEX
COMPLEX		INTEGER
COMPLEX		REAL

(6) The optional ABNORMAL statement permits increased optimization of object programs. Where common subexpressions occur within a statement, it is obviously desirable to evaluate each subexpression only once. Where the common subexpressions contain function references, however, there is a possibility that the function will produce different results upon successive references with the same arguments (e.g., where the function contains input statements or local variables whose values are not initialized each time the function is referenced). UNIVAC 1108 FORTRAN permits all functions that can produce different results from identical sets of arguments to be designated ABNORMAL. All common subexpressions except those that reference ABNORMAL functions are evaluated only once. When the ABNORMAL statement does not appear at all in a program, all function references are

(Contd.)

.143 Extensions Relative to IBM 7090/7094 FORTRAN IV (Contd.)

considered ABNORMAL and re-evaluated at each occurrence, as in most other FORTRAN systems.

(7) The following standard library functions are included in 1108 FORTRAN but not in 7090/7094 FORTRAN IV:

Tangent (REAL, DOUBLE PRECISION, and COMPLEX)
Arcsine (REAL and DOUBLE PRECISION)
Arccosine (REAL and DOUBLE PRECISION)
Hyperbolic Sine (REAL, DOUBLE PRECISION, and COMPLEX)
Hyperbolic Cosine (REAL, DOUBLE PRECISION, and COMPLEX)
Hyperbolic Tangent (DOUBLE PRECISION and COMPLEX; not in 1107 FORTRAN)
Cube Root (REAL, DOUBLE PRECISION, and COMPLEX)

(8) The NAMELIST statement assigns a name to a list of variables. The NAMELIST name can then be used in place of a FORMAT specification in a READ or WRITE statement. A standard format is used for all information output in this fashion. The input data need not be in any fixed format or order; the variables' names and their values are both included in the input.

(9) The ENTRY statement allows the programmer to assign additional entry points to a function or subroutine. The order, type, or number of arguments for an entry point defined in this manner need not be the same as for the function or subroutine definition or other entry points.

(10) Normally, variables having names beginning with the letters I through N are automatically assigned the type INTEGER. Other variables not appearing in an explicit Type statement, such as DOUBLE PRECISION or COMPLEX, are assigned the type REAL. The IMPLICIT statement allows the programmer to specify types implicitly by the first letter of a variable name. For example, if the statement

```
IMPLICIT DOUBLE PRECISION (A, B)
  COMPLEX (E)
```

were included in a program, all subsequent variables having names beginning with the letter A or B would automatically be typed as DOUBLE PRECISION. Similarly, all subsequent variables having names beginning with the letter E would be typed COMPLEX. An IMPLICIT statement can be used to redefine the letter designation at any point in a program. The IMPLICIT statement overrides the beginning letter conventions of INTEGER and REAL. The type statements, such as REAL, COMPLEX or LOGICAL, however, override any assignment by an IMPLICIT statement.

(11) The INCLUDE statement causes a predefined list of statements to be included in the program. A typical use of this statement would be to repeat a long list of DIMENSION, COMMON, EQUIVALENCE, and TYPE statements in a subroutine by the use of a single INCLUDE statement.

(12) The DELETE statement directs the compiler to ignore all subsequent statements through a specified statement number. A second version of the DELETE statement makes the statement conditional upon an INTEGER variable or a PARAMETER variable (see item 2) of the value "0" or "1." Thus, DELETE statements in conjunction with a PARAMETER statement can be conveniently used to suppress object code generation for diagnostic statements without removing the diagnostic statements from the source program.

(13) The EDIT statement allows the programmer to halt source code or object code listings during compilations. Such listings are resumed when an EDIT START statement is encountered.

(14) Any peripheral device can be designated as an input or output unit in a READ or WRITE statement. In the input-output statement, the unit is identified by number. Actual peripheral assignments are made at program load time from a standard table or by control card specifications.

(15) In IBM 7090/7094 FORTRAN, different function names are required depending on the type of the argument. In 1108 FORTRAN V, a generic name can be used for the function, and the correct coding will automatically be generated for the argument presented. For example, the statement

```
VAR + COS (ABC)
```

would cause the coding for DCOS (ABC) to be generated if the argument were of type DOUBLE PRECISION, or for CCOS (ABC) if the argument were of type COMPLEX, etc.

PROCESS ORIENTED LANGUAGE: ALGOL

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 ALGOL.

.12 Origin: . . . . . Evergreen Corporation.

.13 Reference: . . . . . UNIVAC 1108 System Description, Publication UP-4046.

.14 Description

ALGOL is a computation-oriented programming language designed primarily for scientific and engineering applications. UNIVAC 1108 ALGOL conforms to the specifications arrived at jointly by the ACM Committee on Programming Languages and the GAMM Committee on Programming, as published in the Communications of the ACM, May and July, 1960. UNIVAC 1108 ALGOL extends the basic ALGOL 60 language to make use of the 1108's powerful input-output capabilities and incorporates the capability for name strings. Certain machine-dependent extensions have been made to efficiently employ the hardware capabilities of the 1108. Details of these language extensions, and of the ALGOL compiler for the 1108, have not been released to date. UNIVAC states that 1108 ALGOL will be essentially the same as 1107 ALGOL.

A full description of the ALGOL 60 language, as implemented for the Burroughs B 5500, can be found in Report Section 203:161.

.141 Availability

Because of the limited interest in ALGOL in the United States, UNIVAC has not expedited the preparation of documentation on ALGOL for the 1108. UNIVAC states, however, that both the language definition and the ALGOL compiler itself will be made available to interested users.

MACHINE ORIENTED LANGUAGE: 1108 ASSEMBLER

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 Assembler.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corporation.

.13 Reference: . . . . . not published to date.

.14 Description

The UNIVAC 1108 Assembler uses virtually the same source language as the SLEUTH II Assembler for the 1107. The chief difference is the addition of symbolic names for the additional instructions in the 1108. SLEUTH II was implemented for the 1107 by Computer Sciences Corporation and formed a part of the "B Package" software that was offered for the 1107.

The 1108 Assembler permits utilization of all the hardware facilities of the 1108, provides 14 operators that can be used to form expressions, permits the definition and use of subroutines and functions, and produces relocatable object programs that are run under the control of Executive, the operating system for the 1108 (Section 785:191).

The 1108 Assembler uses a free-form coding sheet. Fields must be written from left to right in the order Label, Operation, Operand, and Comments; and fields must be separated from one another by at least one blank column. If the operand field is blank, the line must be terminated by a period. Depending upon the particular machine instruction code in the Operation field, the Operand field may contain up to four sub-fields, separated by commas. Each sub-field may be a simple literal value, a label, or an expression formed with the "+" and "-" operators. The 14 operators listed in Paragraph .83 can be used to form complex arithmetic and/or logical expressions in any or all of the sub-fields. These sub-fields define the base operand address, the arithmetic and index registers to be used, partial-word operands, and other data required by specific instructions.

The 1108 Assembler has 11 "assembler directives." Ten are pseudo operation codes used for controlling the assembly process and defining subroutines and functions. The remaining assembler directive, DO, is a macro instruction that produces any specified value or line of coding a specified number of times. The DO macro is especially useful for subroutine linkages and function references.

The PROC pseudo specifies that the segment of coding following is a subroutine. The subroutine is stored without translation until it is referenced by a DO macro or by use of its name in the Operation field of a symbolic instruction. Then the subroutine is assembled and inserted in-line, with its formal parameters replaced by the parameters specified in the referencing instruction. The FUNC pseudo specifies that the segment of coding following is a function. When referenced, the function produces a value which is dependent upon the values of the parameters supplied to it.

Facilities for inter-program communication permit separately-assembled programs to be linked together at load time. A label followed by an asterisk is defined as an external label, which can be referenced by other programs as well as by the program in which it is defined. When an address expression consists of a label plus or minus a constant, and the label is not defined within the program, a reference to an external label is generated.

The 1108 Assembler can be used on any valid UNIVAC 1108 configuration; see Section 785:031, System Configuration, for the minimum 1108 configuration. Source program input can be accepted from any 1108 peripheral device, including remote data communications terminals. Object program output can also be to any 1108 peripheral device. The 1108 Assembler, like the other 1108 software components, utilizes magnetic drum storage for improved translation speed. The 1108 Assembler is a two-pass assembly system that is capable of assembling over 5,000 statements per minute. Actual source program input and object program output will be limited by the speed of the peripheral devices used.

.15 Publication Date: . . . . February 1966.

.16 Translator Availability: . . . . . November 1965.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . a free-form coding sheet is used, with instruction fields written from left to right in the order Label, Operation, Operand, and Comments, and separated from one another by at least one blank column.

.22 Legend

Label: . . . . . symbolic address of a line of coding or a word of data; or declaration of any one of 32 allocation counters.

Operation: . . . . . mnemonic code for the operation to be performed; a + or - indicates a constant to be generated; a space produces the address of a literal containing information specified in the remainder of the line.

Operand: . . . . . a list of expressions, separated by commas, providing the information required by the Operation Field.

Comments: . . . . . comments and line control symbols (";" for continuation, and "." for termination of an entry).

.23 Corrections: . . . . . no special provisions within the language; the Executive System (see Section 785:191) contains updating provisions.

.24 Special Conventions

.241 Compound addresses: . 14 operators available; see Paragraph .83.

.242 Multi-addresses: . . . . most machine instructions specify a special register in Control Memory as well as the operand address.

.243 Literals —
Alphameric: . . . . . enclose Fieldata character codes within apostrophes.
Octal: . . . . . precede the desired octal value with a zero.
Decimal: . . . . . decimal digits not preceded by a zero.
Floating point: . . . . . decimal value as above, with decimal point preceded and followed by at least one digit.

.244 Special coded addresses: . . . . . $ refers to current location counter; $(e) refers to location counter e, where $0 \leq e \leq 31$.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . . ?

.312 Common label formation rule: . . . . . yes; see Paragraph .321

.313 Reserved labels: . . . . use of "$" within a label should be avoided.

.314 Other restrictions: . . . mnemonic or pseudo operation codes should not be used as labels.

.315 Designators: . . . . . a label immediately followed by "*" is an externally-defined label that provides a communication link between separately-assembled programs.

.316 Synonyms permitted: . via EQU and PROC pseudos.

.32 Universal Labels

.321 Labels for procedures —
Existence: . . . . . mandatory if referenced by other instructions.
Formation rule —
First character: . . letter.
Other: . . . . . letters, numerals, or $.
Number of characters: . . . . . 1 to 6.

.322 Labels for library routines: . . . . . same as procedures.

.323 Labels for constants: . same as procedures.

.324 Labels for files: . . . . same as procedures.

.325 Labels for records: . . same as procedures.

.326 Labels for variables: . same as procedures.

.33 Local Labels: . . . . . local to PROC routine in which they appear; otherwise same as Universal Labels described in preceding paragraph.

.4 DATA

.41 Constants

.411 Maximum size constants —

Machine form	Coding sheet form
Integer —	
Binary:	up to 12 octal digits preceded by zero; or up to 11 decimal digits not preceded by a zero.
Fixed numeric:	none.
Floating numeric —	
Binary:	decimal digits with decimal point preceded and followed by at least one digit.
Alphameric:	any number of Fieldata characters enclosed by apostrophes.

.412 Maximum size literals: . . . . . same as constants, except alphameric literals may not be longer than 6 characters unless a continuation symbol is used.

.42 Working Areas

.421 Data layout —
Implied by use: . . . . no.
Specified in program: by reserving area.

.422 Data type: . . . . . implied by use.

.423 Redefinition: . . . . . yes, by EQU and RES pseudos.

.43 Input-Output Areas

.431 Data layout: . . . . . explicit layout.

.432 Data type: . . . . . not required.

.433 Copy layout: . . . . . PROC pseudo will define common statement; DO macro will cause it to be copied the specified number of times.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . . generally used.
Number: . . . . . approximately 130.
Example: . . . . . AMA = add magnitude.
LICM = load input channel and monitor.
Comment: . . . . . uses same mnemonics as 1107 SLEUTH II.

.512 Absolute —
Existence: . . . . . seldom used, but possible through use of the FORM pseudo.

.52 Macro-Codes: . . . . . one; DO generates a specific value or line of coding a specified number of times.

.53 Interludes: . . . . . none.

(Contd.)

.54 Translator Control

.541 Method of control —
Allocation counter: . . 32 counters, controlled by RES pseudo and designated by label field.
Label adjustment: . . EQU pseudo.
Annotation: . . . . . see Paragraph .544.

.542 Allocation counter —
Set to absolute: . . . . none.
Set to label: . . . . . none.
Step forward: . . . . . RES pseudo.
Step backward: . . . . RES pseudo.
Reserve area: . . . . . RES pseudo.

.543 Label adjustment —
Set labels equal: . . . EQU pseudo.
Set absolute value: . . EQU pseudo.
Clear label table: . . . none.

.544 Annotation —
Comment phrase: . . . separated from operand field by a period and a blank.
Title phrase: . . . . . preceded by a period and a blank.

.6 SPECIAL ROUTINES: . no specifications available to date. Generalized input-output and editing routines are part of the Executive System; see Section 785:191.

.7 LIBRARY FACILITIES: part of the Executive System, described in Section 785:191.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Code: . . . . . DO.
Description: . . . . . generates a specified value or line of coding a specified number of times.

.82 Pseudos ("Assembler Directives")

Code	Description
EQU:	equates a label to the value of the expression in the operand field.
RES:	increments or decrements one of 32 location counters.
FORM:	describes an arbitrary word format designed by the user.
END:	designates end of a program or procedure.
LIT:	defines a table of literals.
INFO:	transmits information from the Assembler to the Executive System.
PROC:	specifies that the following segment of coding is a subroutine, to be stored without translation until referenced by another source program instruction.
FUNC:	defines a function which generates a value when referenced.
NAME:	indicates alternate entrances to PROCedures and FUNCtions.
GO:	transfers control within a PROCedure or FUNCtion to a specific NAME pseudo.

.83 Operators: . . . . . used in operand field to form expressions representing compound addresses or data values. Note that the use of operators other than "+" or "-" to form compound addresses would result in non-relocatable coding.

Code	Description
+	arithmetic sum.
-	arithmetic difference.
*	arithmetic product.
/	arithmetic quotient.
//	covered quotient: a//b means (a + b - 1)/b.
*+	positive exponent: a*+b means $a*10^{b}$.
*-	negative exponent: a*-b means $a*10^{-b}$.
*/	shift exponent: a*/b means $a*2^{b}$ (specifies a binary shift).
++	logical sum (OR).
--	logical difference (exclusive OR).
**	logical product (AND).
=	a = b is 1 if true, 0 if false.
>	a > b is 1 if true, 0 if false.
<	a < b is 1 if true, 0 if false.

OPERATING ENVIRONMENT: EXECUTIVE SYSTEM

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1108 Executive System.

.12 Description

.121 Major Functions

The 1108 Executive System is a comprehensive group of routines designed to control all activities of an 1108 computer system, including job scheduling, hardware allocation, I/O control, and run supervision in both a multiprogramming and a multiprocessing environment. The Executive System is designed to recognize three types or levels of processing:

- Real-time processing,
- Demand processing, and
- Batch processing.

Real-time processing is characterized by the need for a computer response to an external event quickly enough to achieve a desired goal. Real-time processing is normally, but not exclusively, associated with data communications or process control applications where delay in obtaining computer time could result in lost data or process malfunctions. Demand processing is typified by the need for "conversation" between the computer and the user; i.e., the user will specify the execution of certain tasks dependent on the results of previously-initiated tasks. Batch processing is the normal execution of independent tasks (programs) or groups of tasks that are not highly time-dependent.

The principal orientation of the Executive System is toward maximizing the throughput of batch operations while providing facilities for handling useful amounts of real-time and demand processing. Input and output for the batch operations can take place either at the computer site or remotely, via data communications links. The type of processing to be performed is specified in the control statements initiating a run, or perhaps within a task of a run (i.e., the type of processing can vary for each task within a run, and can vary between real-time and batch processing within the same task).

The design of the Executive System is highly modular and allows many parameters to be specified by the installation. Sections of the Executive can be replaced by user-coded routines if desired.

The Executive System can be utilized on any 1108 configuration incorporating at least 786,000 words of FH-432 Magnetic Drum storage. The Executive System contains provisions for handling any 1108 configuration that includes up to three Central Processors and two I/O Controllers. The minimum resident core storage requirement is 10,000 words. For certain installations the residency requirements may be as high as 16,000 words or more, depending on the number of different types of peripheral devices included in the configuration and the inclusion of routines to control real-time and demand processing.

.122 Job Scheduling and Multiprogramming

In a multiprogramming environment, there are two types of scheduling: (1) allocation or reservation of facilities such as core storage, mass storage, and I/O equipment; and (2) allocation of processing time to each program in the current mix. Three modules of the Executive System are concerned with scheduling: the Coarse Scheduler, the Dynamic Allocator, and the Dispatcher.

The Coarse Scheduler interprets information from control statements taken from the "control stream", which may be entered from a card reader or other system component. The control information is used to queue jobs according to priorities. Job queues are normally held on the magnetic drum storage reserved for the Executive System. Jobs are queued on the basis of the following priority sequence:

- Real-time jobs — Multiple real-time jobs are queued within the real-time group on the basis of job priorities assigned by the programmer or operator.
- Demand jobs — Multiple demand jobs are queued within the demand group in the order of arrival to the computer.
- Batch jobs — Multiple batch jobs are queued within the batch group on the basis of job priorities assigned by the programmer or operator.

Typically, a job or run consists of a group of tasks (such as a FORTRAN compilation, execution of a previously-compiled program, etc.) that are performed serially. The Coarse Scheduler also maintains a second queue of runs in which a task has terminated and additional control card interpretation is required prior to the execution of the next task or the termination of a run (perhaps including a memory dump). The second queue is also maintained in the order of program priority.

The Dynamic Allocator accepts the highest-priority tasks from the queues maintained by the Coarse Scheduler and allocates the core storage, mass storage, and peripheral devices required to execute each task.

The Dispatcher controls switching among the programs resident in core storage on the basis of switch lists prepared by the Dynamic Allocator. The basic order of execution is listed below, in descending order:

- Interrupt queuing,
- Programs with real-time status,
- Programs with demand status,
- Programs with batch status, and

.122 Job Scheduling and Multiprogramming (Contd.)

- Other Executive functions, such as advance scheduling, program termination, logging, and accounting.

The order of execution of multiple real-time programs is based on the relative priorities of the programs. Each real-time program maintains control until it can do no further processing or until it is interrupted by a higher-priority real-time program. Typically, control is relinquished when the real-time program either completes its current task or has to wait for the completion of an input or output operation. Once in core storage, a real-time program is not moved until terminated.

Processing time is allocated to demand programs sequentially, based on the demand switch list prepared by the Dynamic Allocator. A demand program maintains control for a predetermined length of time; then control is given either to a higher-priority activity (which may be another demand program) or to the next demand program in the list. Initially, all demand programs are given the same amount of execution time and are executed with the same frequency. The Dynamic Allocator monitors the progress of each demand program and alters the demand switch list on the basis of the frequency of interaction between the computer system and the remote user. If no user action occurs after one burst of execution, the amount of time ("time-slice") per execution phase is increased for that program and its position in the switch list is depressed; the likelihood is that its frequency will be decreased. Thus, the Executive System attempts to optimize the usage of the computer by remote users in the demand mode.

Batch programs are executed in the order of the batch list prepared by the Dynamic Allocator. When a batch program is first brought into the mix, it is placed at the bottom of the list. Information about the estimated Central Processor time required and the deadline for completion of the program is contained in the control statements which initiate a run. Standard installation-set parameters are used if no other values are specified by the programmer. The time-required and deadline parameters are used by the Dynamic Allocator, along with the amount of Processor time already used, to reorder the batch list periodically. Thus, as the deadline for completion of a particular program approaches, its priority, or place in the list, is elevated, and more Processor time is allocated to it for execution. Once a batch program gains control, it remains in control until it can progress no further (typically because it is waiting for the completion of an input or output operation) or until an acitivity of higher priority can proceed.

Programs of the real-time class are allocated processing time and facilities up to the full capacity of the computer. This is necessary to ensure that no data will be lost and no malfunction caused because of a delayed response by the computer.

Time and facility division between demand programs and batch programs are governed by a parameter specified by the installation. This parameter essentially specifies the minimum proportion of Processor time that will be devoted to batch processing whenever there are more requests for batch and demand processing than the computer can satisfy. Programs having demand status can utilize only the remainder of the Processor time, even if infrequently-referenced demand programs must be moved to mass storage areas between calls for them. Demand programs can utilize more than the specified amount of time if there are insufficient batch activities to fully use the time allocated to batch processing. This arrangement is designed to prevent demand programs from monopolizing the computer at the expense of batch programs; it allows the installation management to govern the processing ratio between batch and demand activities.

Two additional control routines are used to maintain control of storage and peripheral facilities. The Facilities Inventory routine maintains a complete listing of all systems facilities, including input-output channels, peripheral devices, mass storage and core storage, along with an indication of those facilities in use and those available for assignment. The Storage Contents Control routine maintains a map of the contents of core storage in terms of the programs or routines that are currently residing in core storage, the location of each, and the areas of core storage that are available for allocation to new programs. This routine also initiates "roll-outs" of lower-priority programs or routines onto magnetic drum storage when space is required for a higher-priority routine. The Storage Contents Control routine also initiates the compacting of core storage (i.e., relocation of programs in core storage to maximize the amount of contiguous core storage space available). Compacting of storage is performed only when necessary to allow the scheduling of a job.

Protection of programs from interference by other programs is accomplished in several ways. Certain storage areas and functions are reserved for Executive System use. Hardware features prevent the accessing of reserved areas by a user program, and user programs are not permitted to execute certain instructions, such as control register modification or initiation of input-output operations. Core storage areas occupied by user programs are protected from unauthorized reading or writing by other user programs by the 1108's addressing technique. See Paragraph 785:051.12 of the Central Processor section for a more detailed description of the hardware memory protection features. A user program is protected from the input or output operations of a second user program by address limit checks carried out by the Executive System. User files are protected from unauthorized access by a security key associated with each file.

.123 Multiprocessing

In a multiprocessor (1108-II) configuration operating under control of the Executive System, all Processors are equivalent; i.e., each Processor can execute any required activity, including control or supervisory routines. In certain cases, such as initiating input or output operations on a Processor channel (as opposed to an I/O Controller channel), the operation can be performed only by a particular Processor. The same basic scheduling techniques are used as outlined in Paragraph .122,

(Contd.)

.123 Multiprocessing (Contd.)

with each Processor being assigned the highest-priority task that can proceed when that Processor completes the previously-assigned tasks. All interrupts are queued, and the Processor currently executing the lowest-priority task is assigned to process each interrupt condition.

The programmer can specify individual tasks within a program that can be performed in parallel. If more than one Processor is available at execution time, these activities may be executed in parallel on different Processors.

The Executive System contains provisions for controlling a multiprocessor configuration containing a maximum of three Processors and two I/O Controllers.

.124 I/O Control and File Control

Input-output operations are controlled either by a central routine that contains individualized routines called "Device Handlers" or by specialized routines called "Symbionts." Device Handlers are provided for controlling operations involving the following peripherals:

- Uniservo IIA, IIIA, IIIC, IVC, VIC, and VIIIC Magnetic Tape Handlers;
- Magnetic tape handlers associated with an on-line UNIVAC 1004-II;
- FH-432 and FH-1782 Magnetic Drum Units;
- Fastrand Storage Units; and
- Communications subsystems utilizing Communications Terminal Module Controllers.

The Device Handlers control all operations of the respective peripheral devices, including search operations and dual-channel operations of magnetic tape or drum units. An "Arbitrary Device Handler" is included to allow control of a non-standard peripheral device.

The Symbionts are a group of control routines designed to serve as the interfaces between magnetic drum storage (any type), where the system expects to find programs and input data and to write output data, and the primary unit record equipment such as card readers and printers. This is similar to the technique used in the EXEC II operating system for the UNIVAC 1107; its purpose is to permit main programs to proceed at drum speed rather than at the much lower speeds of the on-line card readers, card punches, printers, or other low-speed input-output devices. Symbiont-controlled data transcriptions are performed concurrently with the execution of a main program. Symbionts are provided to allow transcriptions between the drums and the following input-output devices: on-site card readers, card punches, and UNIVAC 1004's; and remote devices communicating with the 1108 computer system via a Communications Terminal Module Controller.

In some 1108 configurations (particularly ones utilizing I/O controllers), redundant data paths to the peripheral subsystems are implemented via Multiple Processor Adapters, so a given peripheral subsystem can be addressed either through a Processor channel or through an I/O Controller channel. This provides backup in case of component malfunction and permits uninterrupted operation during maintenance. Preferred paths are assigned by the installation; the Executive System provides the capability to switch to the redundant paths when notified by the operator that the preferred path is unavailable. Channel assignments for dual-channel subsystems are made by the Executive at execution time, based on availability.

The UNIVAC 1108 Executive System's File Control system is comprehensive and provides a great deal of flexibility. In general, users need not be concerned with the physical location of a file; most files are made insensitive to input-output media characteristics, with the File Control system adjusting the interface between the device and the file as necessary. The File Control system provides for files and records within files to be of virtually unlimited length. It also provides security measures to ensure that files will not be destroyed or modified by unauthorized use. The File Control system provides buffering on a block and item basis, and either sequential access or random access to information within a file. The capability for random access to a file is available at all programming levels.

Provisions are included for renaming, copying, deleting, and compacting files. After prolonged use, with many additions and deletions to a file, a large amount of space within the area allocated to the file may in fact be unused. The compacting feature allows a file to be rewritten, eliminating the unused space and returning the excess space to the system.

.125 Operator Communications

Facilities are provided for operator communications with the Executive System via a console typewriter and a cathode-ray-tube visual display device. See Section 785:061, Console, for a more detailed discussion of the console facilities provided.

.126 Other Facilities

The 1108 Executive System also contains provisions for overlay control, supervision of language translators, diagnostics, and checkpoints and restarts.

The segmentation facility, which provides overlay control, allows a user to specify the layout of his program in storage. Segments can be called either by specific loading directions within the program or automatically when referenced by another segment. Program elements in any source language can be named and treated as segments.

All software is oriented toward making all activities of an 1108 computer system operate under control of the Executive System, including language translators such as the COBOL, FORTRAN, and ALGOL compilers and the 1108 Assembler. When using the standard batch-mode compilers, users at remote terminals will typically submit complete tasks, with computer/user communication occurring at the completion of each task. Typical tasks would be to compile, to modify, or to execute a program. In addition, a "conversational mode" FORTRAN compiler will be available to permit remote users to compile and execute programs in statement-by-statement fashion. (See Paragraph 785:162.14 for additional information.) A standard interface is maintained for all language processors (translators), allowing additional

.126 Other Facilities (Contd.)

language processors to be added to the system at a future date.

The various 1108 language translators, such as the FORTRAN and COBOL compilers, maintain three sequence counters when generating object coding. Separate areas are thus designated for data, for object coding, and for a common area. When allocating core storage for the execution of a program, the Executive System attempts to assign each area to a different core memory module. The actual disposition of core storage at allocation time may not permit this, and the three program areas can be located in three, two, or even one memory module. In addition, rearrangement or compacting of core storage can alter the relative locations of the individual program areas.

Extensive diagnostic facilities are available to users for debugging programs, including conditional snapshots of core storage, a memory dump, and snapshots of specified files. Other diagnostic routines check the functioning of major system components such as core storage, Central Processors, and control registers. These diagnostic routines can be initiated either by the operator or automatically, by the Executive System itself, when there is a lull in processing activity.

Checkpoints can be initiated by the program, by the operator, or by the Executive System. When a checkpoint is initiated, the following information is written on the designated output unit: file position information, contents of all registers and other control information, contents of the user's core storage area or the part he designates, and contents of mass storage files if desired. Checkpoints can be written onto a magnetic drum or a magnetic tape unit. Restarts must be initiated by the operator.

.13 Availability: . . . . . third quarter, 1966 (Executive Control Functions).

.14 Originator: . . . . . UNIVAC.

.15 Maintainer: . . . . . UNIVAC.

.2 PROGRAM LOADING

.21 Source of Programs: . . all programs to be executed are normally maintained in random-access storage prior to allocation and loading into core storage.

.22 Library Subroutines: . held in random-access storage except for the most common I/O control routines and certain supervisory routines, which reside in core storage.

.23 Loading Sequence: . . . programs are loaded sequentially into a job stack from an external device.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . . segmentation of a program can be specified at load time by control cards or (in COBOL only) when programming.

.312 Occupation of working storage: . . . . . segments can be loaded by a programmed call or automatically when referenced by the program.

.32 Input-Output Units

.321 Initial assignment: . . . under control of the Executive System.

.322 Alternation: . . . . . as specified by individual programs.

.323 Reassignment: . . . . . system can be reconfigured by operator through control cards.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: see Paragraph .124.

.42 Multiprogramming: . . see Paragraph .122.

.43 Multi-sequencing: . . . see Paragraph .123.

(Contd.)

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Allocation impossible:	Executive check	delay processing of this program.
I/O error, single:	interrupt	reread or rewrite if possible (tape or drum); otherwise, type message and terminate task.
I/O error, persistent:	interrupt	type message and terminate task if number of errors exceeds a threshold value.
Loading input error:	same as I/O error.	
Control Register parity error:	interrupt	further interrupts are inhibited and an attempt is made to locate the faulty register and to distinguish between a recurring error and a transient error. If the error is transient, and the system is in a non-critical state, the error is ignored, the program is sent to a restart routine, or an entrance is made to an I/O error routine, depending on the register involved. A recurring error, or a transient error while the system is in a critical state, causes the system to halt, and manual instruction is necessary for restart.
Core storage parity error:	interrupt	an attempt is made to locate the faulty location and to distinguish between a transient and a recurring error. If the faulty location cannot be found, operation resumes. A transient error in a non-critical task results in the task being aborted and operation resumed. Any error in a critical task causes the system to halt. A permanent fault causes the task to be aborted and the 512-word block to be removed from available core storage.
Power failure:	interrupt	control registers and instruction counter are stored; active I/O channels are flagged.
Illegal operation:	interrupt	type message, dump registers, terminate task.
Floating-point overflow or underflow, or divide overflow:	interrupt	set results to zero and continue.
Out-of-bounds address:	interrupt	type message, dump registers, and terminate task.
Reference to forbidden area:	interrupt	type message, dump registers, and terminate task.

* The actions described are the standard ones implemented in the Executive System. Any or all of these can be replaced by user-coded routines; for example, the action in every case might be a simple halt, which would decrease the space required to hold the error routine.

.45 Restarts

.451 Establishing restart points: . . . . . checkpoints can be initiated by the program, by Executive, or by the operator. Checkpoints can be written on mass storage or magnetic tape. If on tape, checkpoints can include mass storage files. Superseded checkpoints are automatically deleted if written on mass storage.

.452 Restarting process: . . keyboard entry by operator initiates automatic restart.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . no direct provisions within the Executive System.

.512 Snapshots: . . . . . specified by control cards at program load time or by control statements within the program. Conditionals can be used to specify when a snapshot is to be taken. Specified areas of core storage, control registers, magnetic tape files, and/or mass storage areas can be written onto a diagnostic file for printing after the program has terminated.

.52 Post-Mortem: . . . . . specified by operator via a control card after program termination. Dumps can be from core storage areas only.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . . typed message on console typewriter.

.612 Action required by operator: . . . . . typed message.

.613 Reporting progress of run: . . . . . typed message.

.62 Operator's Decisions: . keyboard entries.

.63 Operator's Signals

.631 Inquiry: . . . . . keyboard entries.

.632 Change of normal progress: . . . . . a program priority change, a delay in the scheduling of a program, or removal or addition of I/O equipment can be made via keyboard entries.

.7 LOGGING

.71 Operator Signals: . . . . typed record of keyboard entries.

.72 Operator Decisions: . . typed record of keyboard entries.

.73 Run Progress: . . . . . typed messages.

.74 Errors: . . . . . typed messages.

.75 Running Times: . . . . . typed messages.

.76 Multiprogramming Status: . . . . . typed messages in response to keyboard inquiries. A summary of the backlog and a list of the programs being restrained from allocation can be requested.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . . any permitted 1108 configuration; see Section 785:031.

.812 Usable extra facilities: . . . . . all; control cards or keyboard entries are used to inform the Executive whenever there is a change in the number or type of I/O devices available.

.813 Reserved equipment: . . approximately 12,000 words of core storage and 786,000 words of magnetic drum storage. Drum storage includes space for job files and I/O buffering areas.

.82 System Overhead: . . . . operating portion remains in core storage; other portions are called in as needed; loading time depends on drum-to-core data transfer rate.

.83 Program Space Available: . . . . . all, except as noted in Paragraph .813, above.

.84 Program Loading Time: . . . . . depends on drum-to-core data transfer rate. (Time to load program initially onto drum varies with input device.)

.85 Program Performance: varies widely with hardware availability and with number and types of programs being run at the same time. UNIVAC estimates that about 50 to 100 microseconds, on the average, will be required to switch from one program to another. UNIVAC also estimates that the overall demand on the Processors due to Executive functions will typically be about 5 percent, exclusive of the time involved when swapping demand programs between magnetic drum and core storage.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (785:201.100)

These problems involve updating a master file from information in a detail file and producing a printed record of each transaction. This application, one of the most common commercial data processing jobs, is fully described in Section 4:200.1 of the Users' Guide. Standard File Problems A, B, and C show the effects of varying record sizes in the master file. Standard File Problem D increases the amount of computation performed upon each transaction. Each problem is estimated for activity factors (ratios of number of detail records to number of master records) of zero to unity. In all cases a uniform distribution of activity is assumed.

To realistically portray the performance of the UNIVAC 1108 computer in a multiprogramming mode of operation, the transaction file and the report file are assumed to be on magnetic tape. The data transcription runs necessary for card-to-tape and tape-to-printer media conversions are performed by separate programs and can be run concurrently with the main File Processing run or with other program runs. The elapsed time and Central Processor time for the data transcription runs are shown on a separate graph (785:201.150). These times are the same for blocked or unblocked tape files.

In computing the Central Processor times, instructions and operands were assumed to be placed in different core storage banks where possible, to take maximum advantage of the 1108's capability for overlapping accesses to main memory.

The master-file record format is a mixture of alphameric and binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. (Even so, much of the Central Processor time is devoted to editing and radix conversion operations.) A moderate degree of packing led to a record length of 18 words (or 108 6-bit characters).

In the graphs presenting the performance of the UNIVAC 1108 for Standard File Problems A, B, C, and D, the total time for the main processing run is shown for both blocked and unblocked detail and report files. The limiting factor for Configuration VIIA is a combination of one master-file tape and the report-file tape. Additional tape channels reduce the overall elapsed times for Configuration VIIIA, while the Central Processor times remain the same as for Configuration VIIA. In general, the controlling factor is the report-file tape at high activities and one master-file tape at low activities.

The curve representing the Central Processor times is also shown on each graph. The difference between the Central Processor time and the elapsed time for the main processing run indicates the amount of Central Processor time available for concurrently performing other tasks such as data transcriptions or other main programs. The performance of a UNIVAC 1108 system when running multiple programs simultaneously depends upon the complement of peripheral equipment and upon the input-output channel availability and usage, as well as upon the amount of Central Processor time used by each program. This System Performance section contains enough information (particularly in Worksheet Data Table I) to enable you to estimate the overall performance of a UNIVAC 1108 system for any desired mix of the standard benchmark problems.

SORTING (785:201.200)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A by the method explained in Paragraph 4:200.213 of the Users' Guide. A three-way merge is used in all system configurations for the UNIVAC 1108. The results are shown in Graph 785:201.200.

MATRIX INVERSION (785:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplications ($c = c + a_i b_j$) in single-precision floating-point (see Paragraph 785:051.422). Inversion times are shown for two cases: instructions and data in the same core storage bank, and instructions and data in alternate banks.

GENERALIZED MATHEMATICAL PROCESSING (785:201.400)

The Standard Mathematical Problem A is an application in which there is one stream of input data, a fixed computation to be performed, and one stream of output results. Two variables are introduced to demonstrate how the time for a job varies with different proportions of input, computation, and output. The factor C is used to vary the amount of computation per input record. The factor R is used to vary the ratio of input records to output records. The procedure used for the

Standard Mathematical Problem is fully described in Section 4:200.2 of the Users' Guide. Computations are performed in single-precision floating-point arithmetic, which provides the minimum 8-digit precision prescribed in the Users' Guide.

Again, because multiprogramming is featured in the UNIVAC 1108, the curves show the Central Processor time as well as total elapsed time. The performance for both Configurations VIIA and VIIIA is assessed for the multiprogramming mode of operation. Graph 785:201.400 shows the time for the main processing run, in which the input and output are on magnetic tape and in which all of the prescribed internal processing is performed (including editing and radix conversions). The table beneath the chart shows the times for the corresponding card-to-tape (input) and tape-to-printer (output) data transcription runs. The performance curves for Configurations VIIA and VIIIA are identical for the 1108 because the same magnetic tape units are employed and the additional tape channels in Configuration VIIIA are of no benefit in this problem.

WORKSHEET DATA TABLE 1

	ITEM		CONFIGURATION VIIA		VIIA (Blocked Files 3 & 4)		VIIIA		VIIIA (Blocked Files 3 & 4)		REFERENCE
1	Char/block	(File 1)	1,080		1,080		1,080		1,080		
	Records/block	K (File 1)	10		10		10		10		
	msec/block	File 1 = File 2	17.5		17.5		17.5		17.5		
		File 3	7.4		15.0*		7.4		15.0*		
		File 4	7.6		20.0*		7.6		20.0*		
Input-Output Times	msec/switch	File 1 = File 2	0		0		0		0		4:200.112
		File 3	0		0		0		0		
		File 4	0		0		0		0		
	msec penalty	File 1 = File 2	0.135		0.135		0.135		0.135		
		File 3	0.011		0.11*		0.011		0.11*		
		File 4	0.017		0.17*		0.017		0.17*		
2	msec/block	a_1	0.015		0.015		0.015		0.015		
Central Processor Times	msec/record	a_2	0.024		0.024		0.024		0.024		
	msec/detail	b_6	0.071		0.071		0.071		0.071		4:200.1132
	msec/work	$b_5 + b_9$	0.073		0.073		0.073		0.073		
	msec/report	$b_7 + b_8$	0.664		0.664		0.664		0.664		
3	msec/block for C.P. and dominant column.		C.P.	Tapes	C.P.	Tapes	C.P.	Tape	C.P.	Tape	
Standard File Problem A F = 1.0		a_1	0.015		0.015		0.015		0.015		
		a_2K	0.240		0.240		0.240		0.240		
		a_3K	8.080		8.080		8.080		8.080		
		File 1: Master In	0.135	17.5	0.135	17.5	0.135		0.135		4:200.114
		File 2: Master Out	0.135		0.135		0.135		0.135		
		File 3: Details	0.110		0.110		0.110		0.110		
		File 4: Reports	0.170	76.0	0.170	20.0	0.170	76.0	0.170	20.0	
		Total	8.885	93.5	8.885	37.5	8.885	76.0	8.885	20.0	
4	Unit of measure	(36-bit words)									
Standard File Problem A Space		Std. routines	**		**		**		**		
		Fixed	—		—		—		—		
		3(Blocks 1 to 23)	189		189		189		189		4:200.1151
		6(Blocks 24 to 48)	1,080		1,080		1,080		1,080		
		Files	792		1,440		792		1,440		
		Working	40		40		40		40		
		Total	2,101		2,749		2,101		2,749		

	ITEM		CONFIGURATION VIIA	VIIIA	REFERENCE
5	Fixed/Floating point		Floating Point	Floating Point	
Standard Mathematical Problem A	Unit name	input	Uniservo VIIIC	Uniservo VIIIC	
		output	Uniservo VIIIC	Uniservo VIIIC	
	Size of record	input	80 char.	80 char.	
		output	132 char.	132 char.	
	msec/block	input T_1	7.4	7.4	4:200.413
		output T_2	7.6	7.6	
	msec penalty	input T_3	0.011	0.011	
		output T_4	0.017	0.017	
	msec/record	T_5	1.285	1.285	
	msec/5 loops	T_6	0.194	0.194	
	msec/report	T_7	1.454	1.454	

* 10 records per block in Files 3 and 4.
** Does not include space required for resident portions of the standard operating system.

(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes —
Master file:. . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

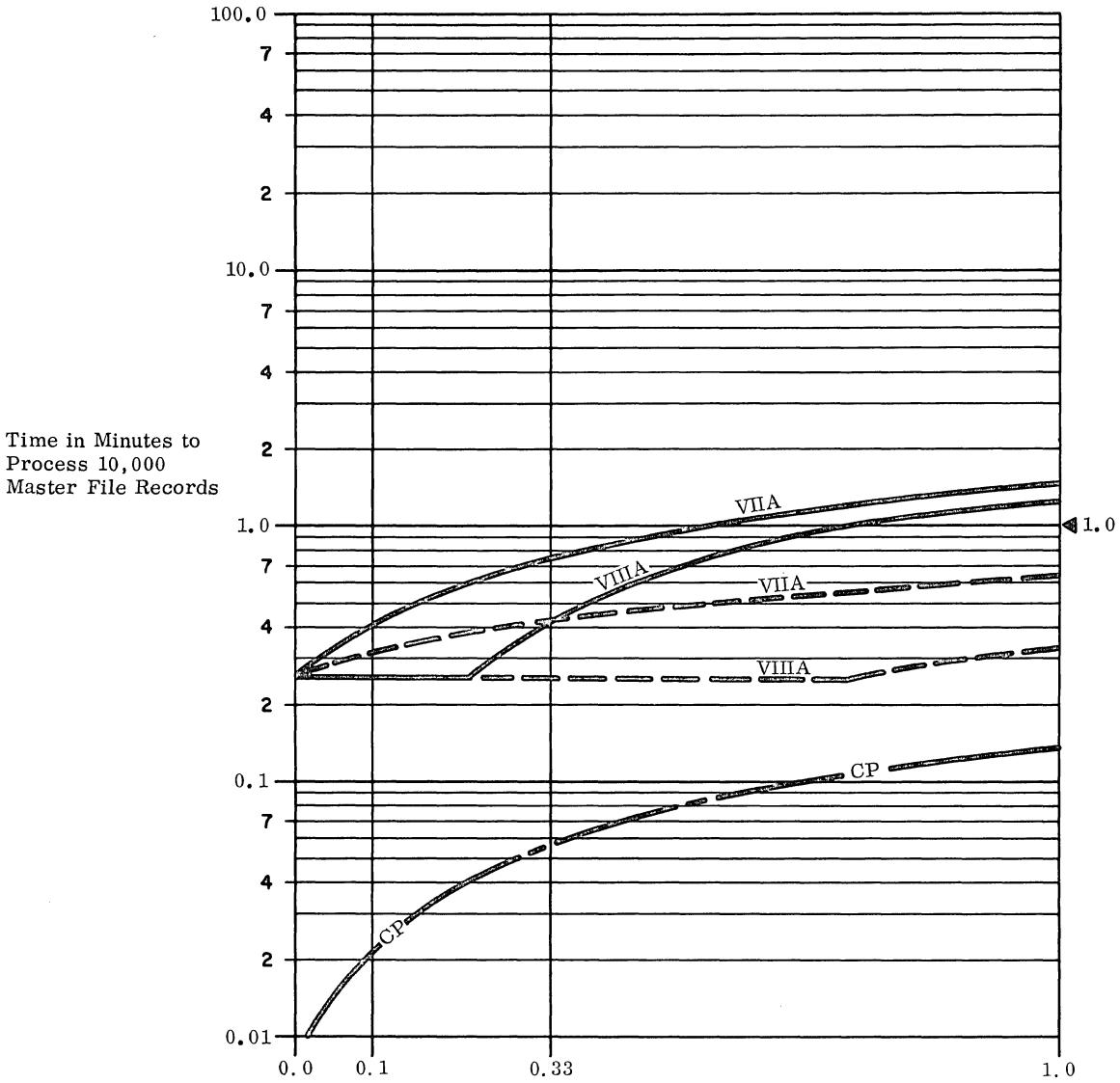
.112 Computation:. . . . . standard.

.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . . see graph below.

.115 Storage space required* —
Configurations VIIA & VIIIA: . . . . . 2,101 words.
Configurations VIIA & VIIIA (blocked Files 3 & 4): . . . . . 2,749 words.

*Does not include space required for resident portions of the standard operating system.



(Roman numerals denote standard System Configurations.)

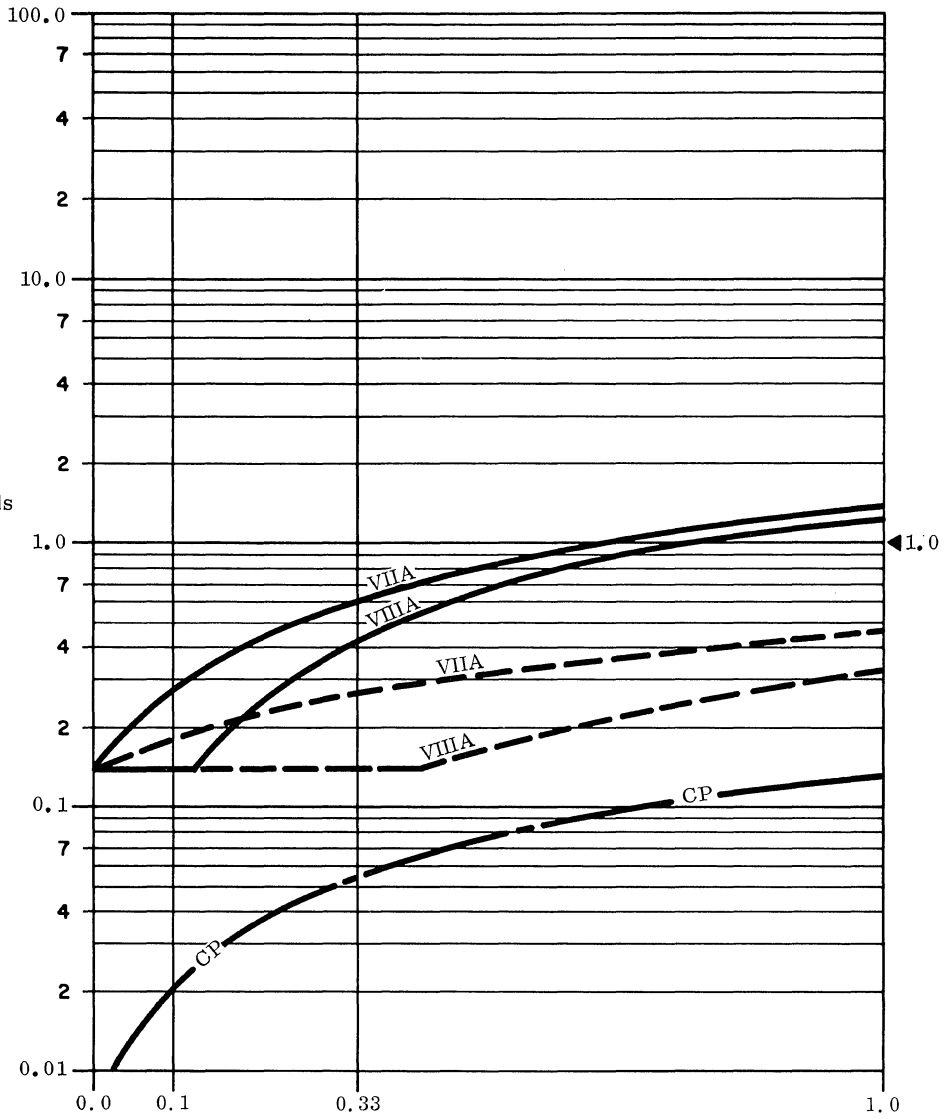
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

.12 Standard File Problem B

.121 Record sizes —
Master file:. . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

.122 Computation:. . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

LEGEND

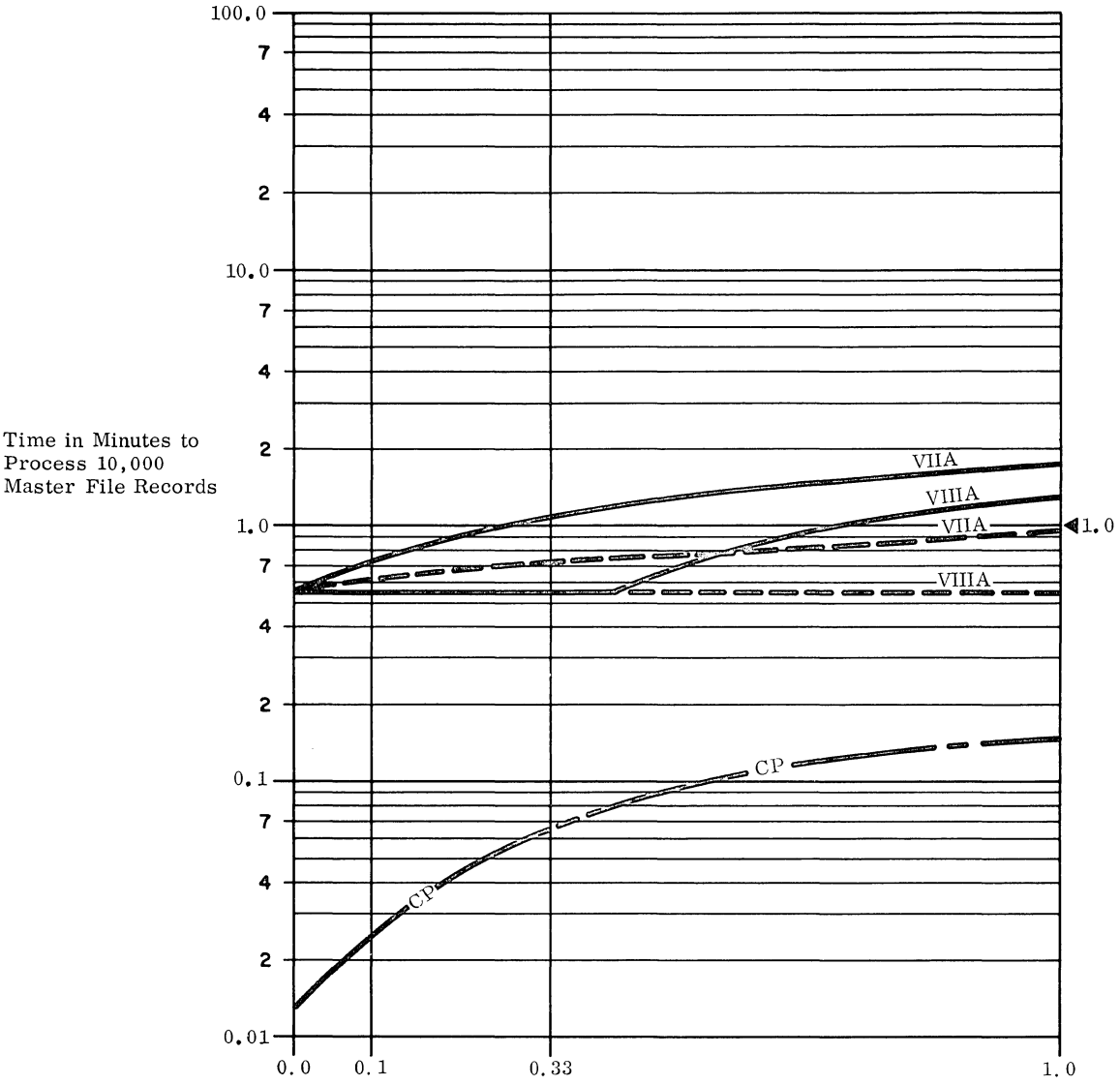
Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

(Contd.)

.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph . . . . . see graph below.



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

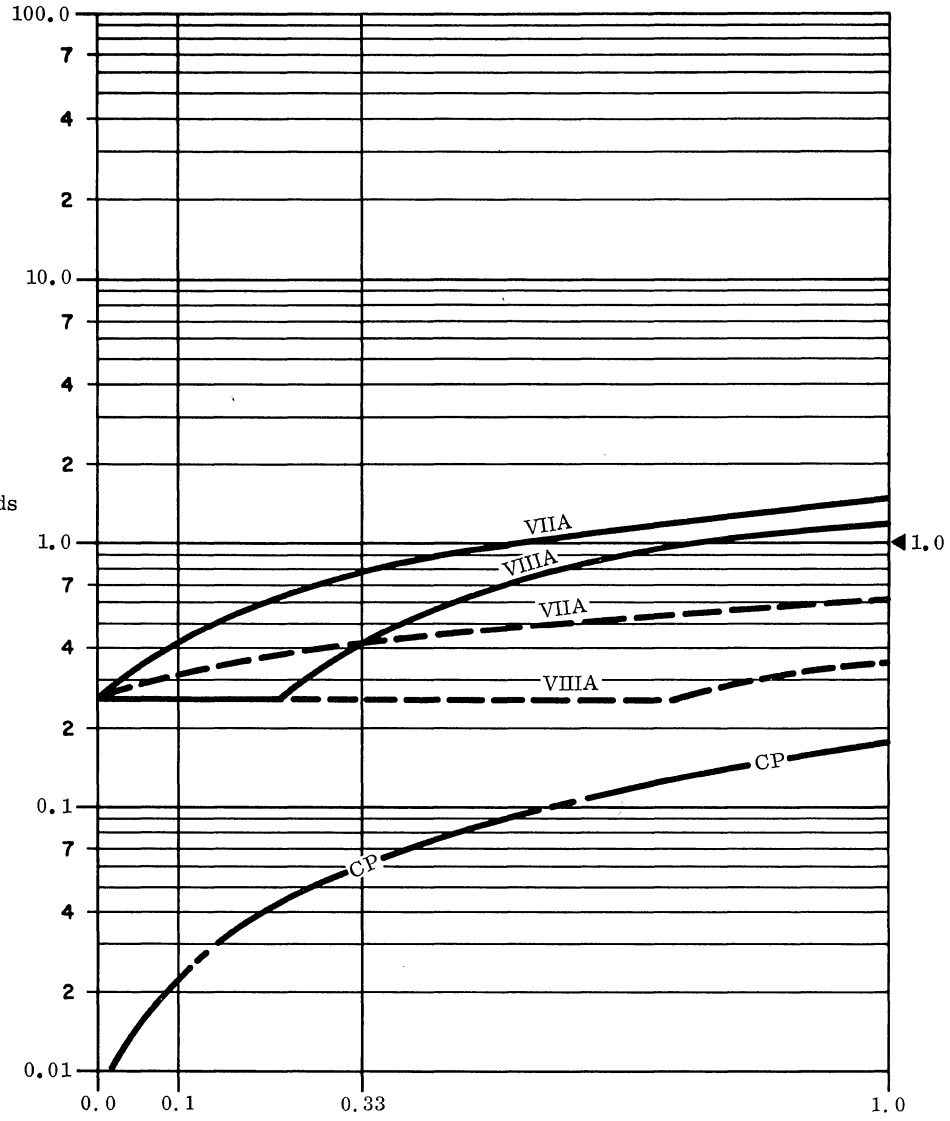
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

.14 Standard File Problem D

.141 Record sizes —
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.144 Graph: . . . . . see graph below.



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP — Central Processor time (all configurations)

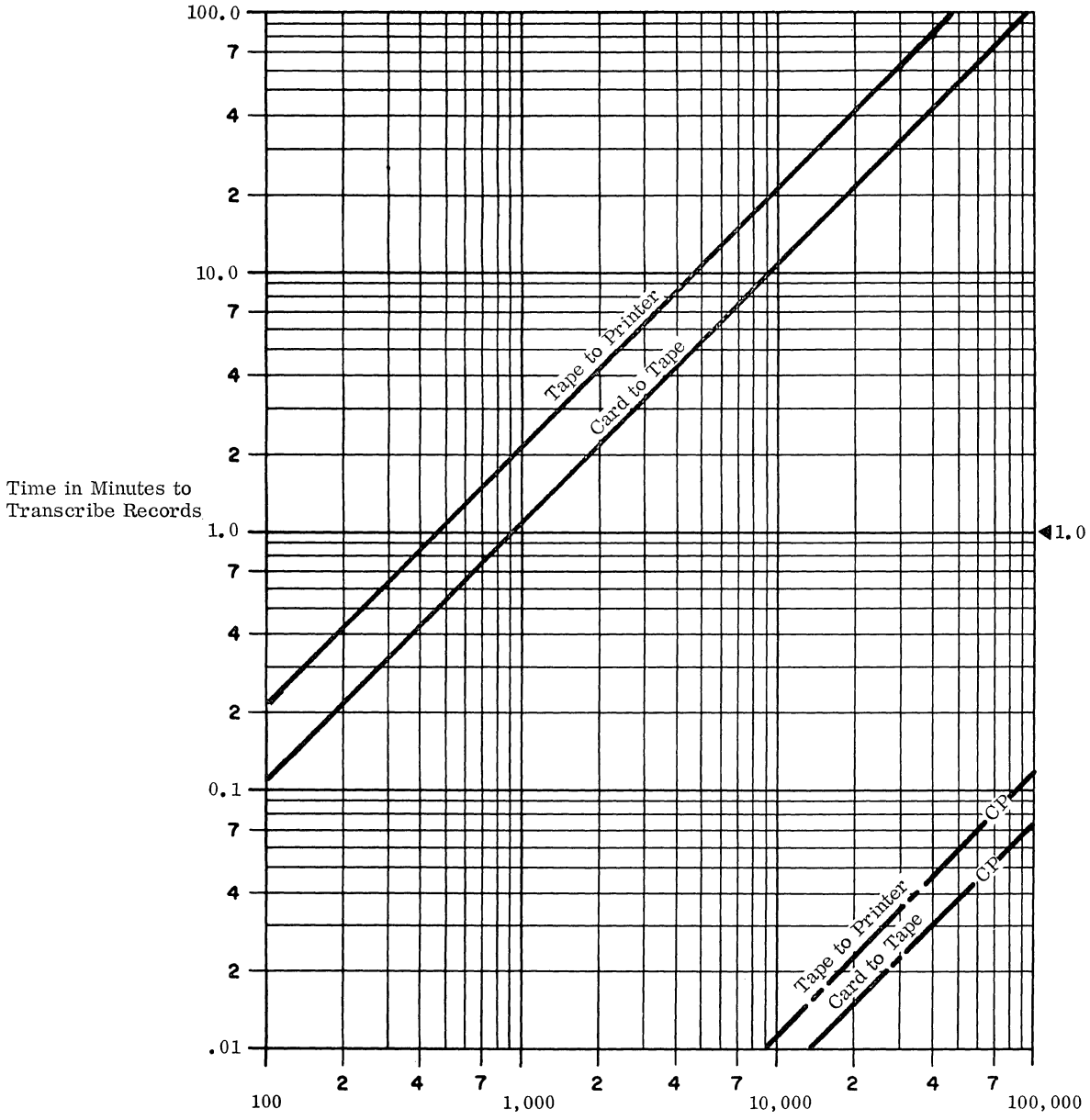
(Contd.)

.15 Data Transcription Runs for Standard File Problems

.151 Block sizes:
Detail File —
On cards: . . . . . one card.
On tape: . . . . . one card image (unblocked) or ten card images (blocked).
Report File —
On printer: . . . . . one print line.
On tape: . . . . . one print-line image (unblocked) or ten print-line images (blocked).

.153 Timing basis: . . . . . data is transcribed directly from cards to tape or tape to printer; no editing is performed other than blocking on tape (in some cases).

.154 Graph: . . . . . see graph below.



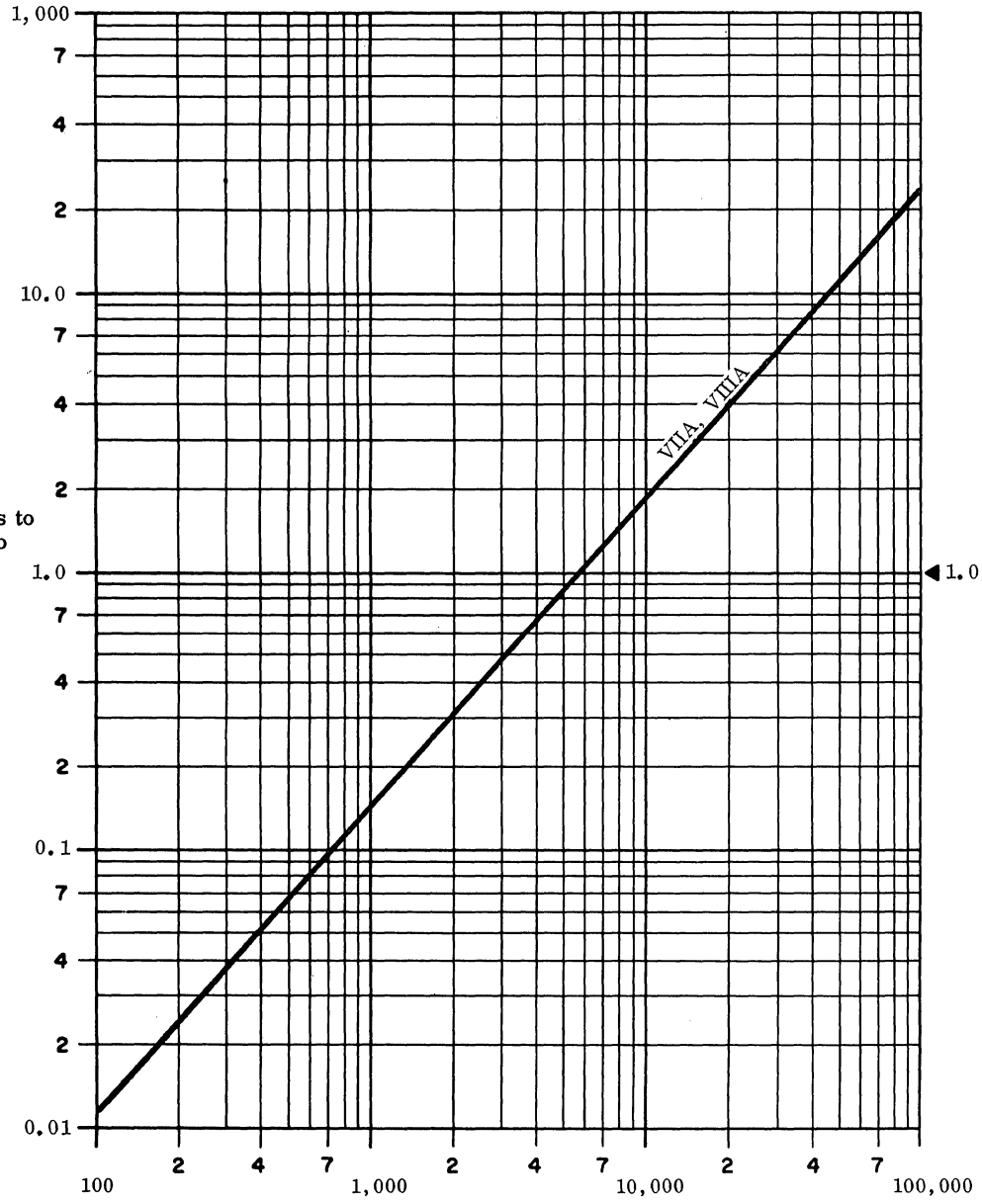
(Graph applies to Standard Configurations VIIA and VIIIA; lines marked "CP" denote Central Processor times.)

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.
.212 Key size: . . . . . 8 characters.

.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.
.214 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

(Contd.)

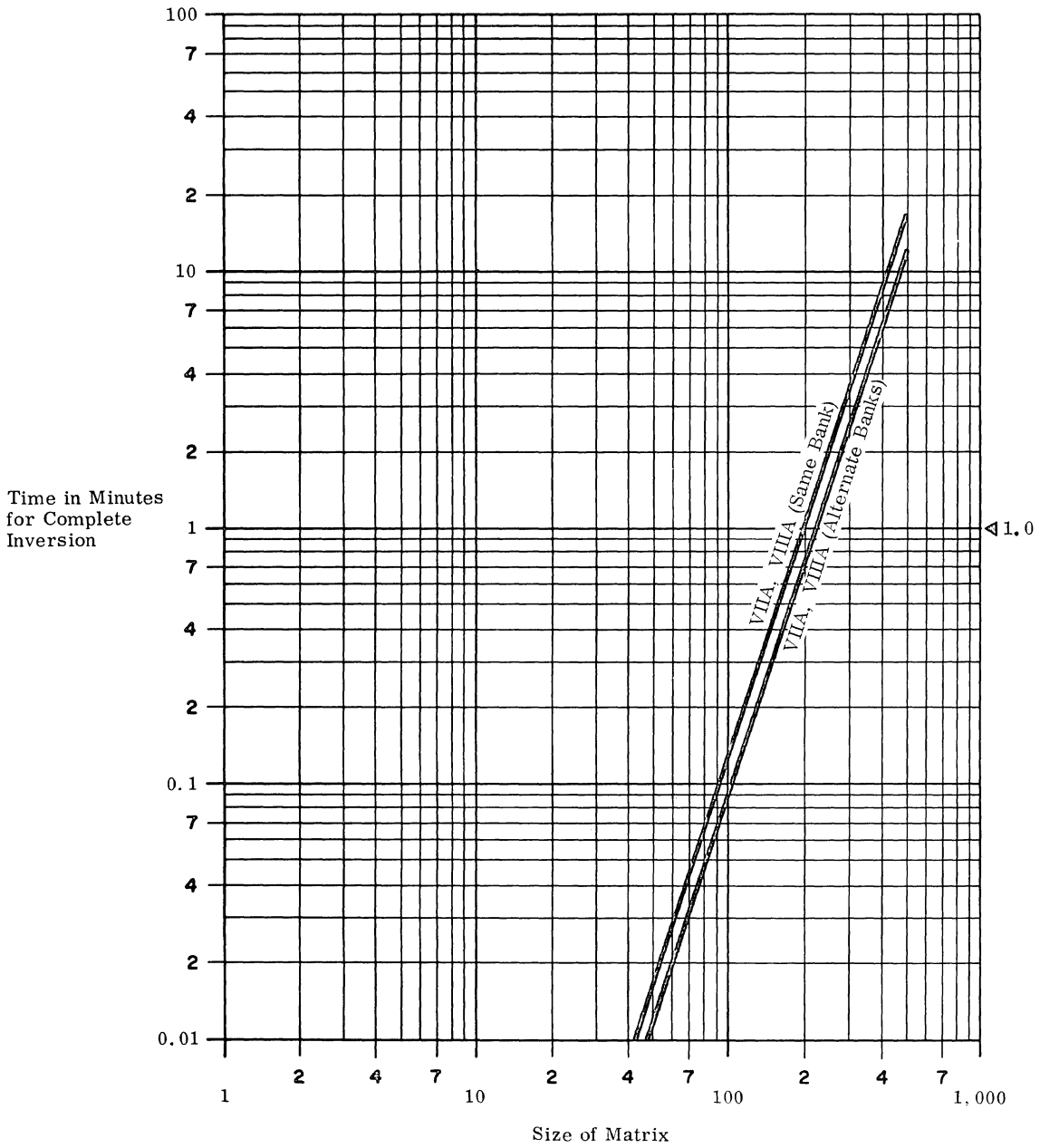
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

.4 GENERALIZED MATHEMATICAL PROCESSING

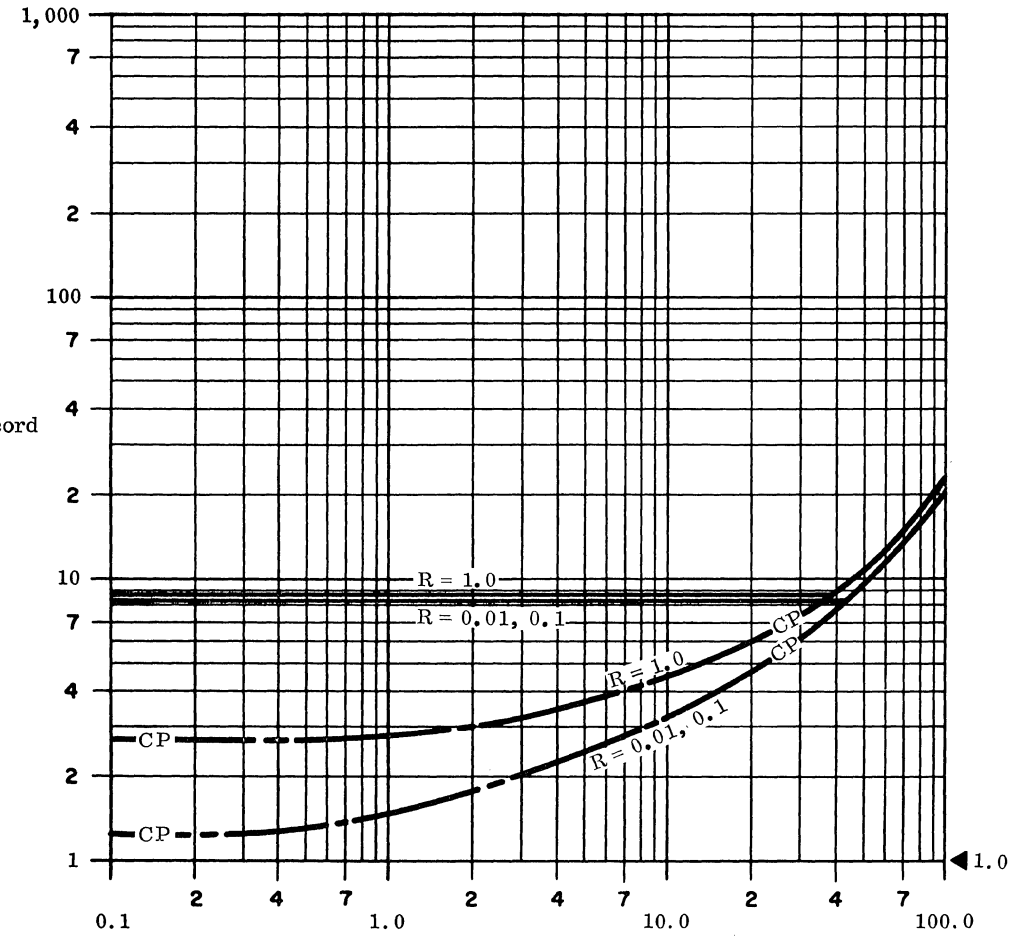
.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . 10 signed numbers; average size 5 digits, maximum size 8 digits.

.412 Computation: . . . . . 5 fifth-order polynomials, 5 divisions, and 1 square root; computation is in single-precision floating-point mode (8-digit precision).

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . . see graph below.



DATA TRANSCRIPTION RUN, CONFIGURATIONS VIIA AND VIIIA

	R = 0.01	R = 0.1	R = 1.0
Elapsed time —			
Input (card to tape)	67.	67.	67.
Output (tape to printer)	1.33	13.3	133.
Central Processor time —			
Input*	0.045	0.045	0.045
Output*	0.0007	0.007	0.069

*Does not include the time for the I/O control routines.

(Roman numerals denote standard System Configurations; R = Number of output records per input record; all times are expressed in milliseconds per input record.)

PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
1108 Central Processor	64	26	64	600	?	9,200
Memory Module (contains 32,768 words)	36	26	64	500	3.2	10,900
Console	65	37	41	600	0.7	2,400
FH-432 Drum Unit (contains two drums)	48	24	64	765	2.5	600
FH-1782 Drum Unit	64	34	64	1,700	0.85	2,000
FH-432/1782 Control	48	24	64	1,300	0.85	2,000
Fastrand II Storage Unit	122	35	64	5,150	12.5	19,500
Fastrand Control	36	26	55	650	1.0	2,800
Multiple Module Access Unit	25	26	64	450	0.65	10,500
Input/Output Controller	64	26	64	1,000	5.4	12,300
Multiple Processor Adapter	24	26	64	600	1.25	3,420
Card Reader	48.5	24	54	700	1.0	2,500
Card Punch	38	26	48	775	1.5	4,600
Card Control	20	35	64	625	3.73	2,600
High-Speed Printer	43	33	55	1,250	1.7	4,930
High-Speed Print Control —						
For 1 printer	20	35	64	625	5.95	2,600
For up to 4 printers	?	?	?	?	?	?
Punched Paper Tape Subsystem	24	35	64	800	1.0	3,000
Uniservo VIC Tape Handler (all models)	24	26	64	500	0.5	3,500
Uniservo VIC Control and Synchronizer (all models)	24	26	64	500	0.80	2,170
Uniservo VIIIC Tape Handler (all models)	27	29	64	700	2.75	5,100
Uniservo VIIIC Control and Synchronizer (all models)	24	24	64	600	0.95	2,170
Communications Subsystem Cabinet (each CTM Controller and associated equipment requires 2 cabinets)	48	26	80	2,000	5.9	6,000
Word or Communication Terminal Synchronous (WTS or CTS)	24	24	72	600	1.0	4,500

General Requirements

Temperature: . . . . . between 60°F and 80°F.
Relative humidity: . . . . . between 30% and 70%.
Power: . . . . . 240-volt, 1-phase, 60-cycle, 3-wire; or 208-volt, 3-phase, 60-cycle, 4-wire.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR		UNIVAC 1108 Central Processor (includes 8 input-output channels and Console)	15,500	2,132	651,000
		4 Additional Input-Output Channels (max. of 8 additional channels)	500	52	21,000
		Auxiliary Console (operator)	?	?	?
		Auxiliary Console (communications)	150	10	6,300
INTERNAL STORAGE		Main (Core) Memory			
		1 Bank (65,536 words)	10,000	650	420,000
		2 Banks (131,072 words)	20,000	1,200	840,000
		3 Banks (196,608 words)	30,000	1,700	1,260,000
		4 Banks (262,144 words)	40,000	2,200	1,680,000
		Multiple Module Access Unit (required for each bank when multiple Processors or I/O Controllers require access to memory)	735	50	30,870
		FH-432 Drum and Control	3,000	85	40,000
		FH-432 Drum	1,000	310	120,000
		FH-1782 Drum (prices to be announced)	?	?	?
		Fastrand Control and Synchronizer (controls up to 8 Fastrand II Units) —			
		Single Channel, Unbuffered	1,200	100	57,600
		Single Channel, Buffered	1,250	100	60,000
		Dual Channel, Unbuffered	2,400	200	115,200
		Dual Channel, Buffered	2,500	200	120,000
		Fastrand II Storage Unit	3,800	265*	184,000
		Options for Fastrand II			
		Fastband	200	22	9,000
		Write Lockout	24	3	1,125
		Search All Words (requires buffered control)	50	—	2,000
INPUT-OUTPUT		Controllers and Adapters			
		Input-Output Controller (includes 4 I/O channels)	4,000	100	168,000
		4 Additional I/O Channels (max. of 12 additional channels)	500	50	21,000
		256 Additional Words of Index Memory	750	5	31,500

* For first unit only; monthly maintenance charge for each subsequent unit is $125.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd.)		Multiple Processor Adapter (permits a peripheral subsystem to be accessed by up to 4 processors or I/O Controllers) —			
		Basic 36-bit MPA (with 2-processor capability)	435	25	18,270
		Second 36-bit MPA (with 2-processor capability)	400	20	16,800
		Third Processor Capability	30	5	1,260
		Fourth Processor Capability	50	5	2,100
		1004 Adapter **	200	20	8,000
		Punched Card			
		Card Control and Synchronizer (controls one Card Reader and one Card Punch)	750	230	33,750
		Card Reader — 900 cpm	380	100	15,200
		Card Punch — 300 cpm	665	200	26,600
		Printer			
		High-Speed Print Control and Synchronizer —			
		Controls one printer	750	160	34,275
		Controls up to four printers	?	?	?
		High Speed Printer — 700/922 lpm	800	240	36,000
		Punched Paper Tape			
		Paper Tape Reader, Punch, and Control	645	110	32,250
		Magnetic Tape			
		Uniservo VIC Tape Handler; 34,500 char/sec —			
		Master 7-Track, Non-Simultaneous (contains common circuitry for itself and up to three Slave Units)	500	125	20,000
		Master 7-Track, Simultaneous	550	125	22,000
		Slave 7-Track	300	75	12,000
		Control and Synchronizer	700	30	28,000
		Auxiliary Control and Synchronizer (required for dual-channel subsystem)	700	30	28,000
		Translate Option (translates between internal Fieldata code and BCD code; required on each control in a dual-channel subsystem)	100	5	3,600
		Uniservo VIIIC Tape Handler; 96,000 char/sec —			
		7-Track, Non-Simultaneous	800	95	36,000
		7-Track, Simultaneous	850	95	38,250
		Control and Synchronizer	1,450	105	60,900
		Auxiliary Control and Synchronizer (required for dual-channel subsystem)	1,450	105	60,900
		Translate Option (translates between internal Fieldata code and BCD code; required on each control in a dual-channel subsystem)	100	5	3,600

** For price data on the UNIVAC 1004, see Report Section 770:221.

(Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd.)		Communications Equipment			
		Communication Terminal Module Controller (controls up to 16 CTM's)	650	118	25,000
		Communication Terminal Module (CTM; provides 2 input and 2 output positions) —			
		Low speed; up to 300 bps	60	11	2,400
		Medium speed; up to 1,600 bps	75	13	3,300
		High speed; 2,000 to 4,800 bps	90	12	3,600
		CLT Automatic Dialing	20	6	900
		CLT Parallel Output	35	7	1,575
		CLT Parallel Input	35	7	1,575
		Scanner/Selector (connects up to four controllers to a single I/O channel)	800	36,000	?
		Communication Terminal Synchronous —			
		Terminal Basic Set	250	69	10,000
		Power Supply	100	28	4,000
		Synchronous Module	250	69	10,000
		Broad Band Interface	100	28	4,000
		Unattended Answering	5	—	200
		Automatic Calling	50	14	2,000
		Word Terminal Synchronous —			
		Terminal Basic Set	250	69	10,000
		Power Supply	100	28	4,000
		Synchronous Module	445	138	17,800
		Voice Band	5	—	200
		Broad Band	5	—	200
		Unattended Answering	5	—	200
		Automatic Calling	50	14	2,000

UNIVAC 418

Univac

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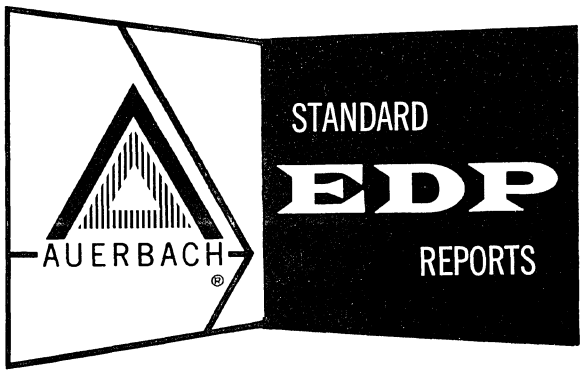

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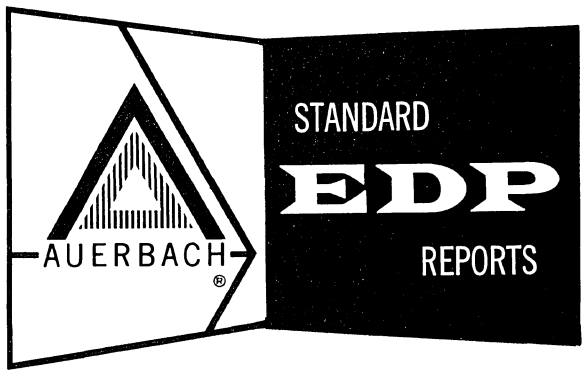

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CONTENTS

INTRODUCTION

The UNIVAC 418 is a medium-scale, solid-state computer that is oriented primarily toward real-time and message switching applications. Two central processors and associated core memories are available for use in 418 systems: the Model I and the Model II. Both models have the same set of instructions and, given the same peripheral equipment and input-output channel assignments, are completely program-compatible. The core storage cycle time is 4 microseconds for Model I and 2 microseconds for Model II.

A wide range of magnetic drum units, magnetic tape units, and communication devices permit the UNIVAC 418 to serve as a versatile message switching center. The 418 is also suited for real-time commercial applications in which it is essential or desirable to reduce the time lag between the occurrence of a transaction and the corresponding updating of one or more master files. Use of the 418 in scientific applications will generally not be economical due to its short word length (18 bits) and the absence of instructions for double-precision or floating-point arithmetic. UNIVAC 418 system rentals range from approximately $7,000 to $18,000 per month and average around $11,000.

Although UNIVAC 418 systems have been operating in customer installations since June, 1963, their general availability to commercial users was not announced until August, 1964. The 418 is closely related to the UNIVAC 1218 Military Computer. Both the 418 and the 1218 evolved from the UNIVAC CUT (Control Unit Tester), a special-purpose computer designed to test peripheral equipment for the larger UNIVAC computer systems. A modified version of the 418 serves as the central processor in the Westinghouse PRODAC 510 and 580 process control systems.

The principal characteristics that make the UNIVAC 418 system suitable for real-time or message switching applications are:

- High-capacity random access storage for master file data or messages in transit.
- A variety of magnetic tape units, which provide storage of slower access and greater capacity for use as a reference store, a journal, and intercept and overflow storage.
- Program interrupt facilities which permit concurrent processing of several levels of programs.
- Flexible communications linkages to any common carrier for two-way transmission of data between the computer and remote points.
- Two electronic chronometers, which make the system "time-conscious."

Hardware

UNIVAC 418 systems using the Model I Processor can have from 4,096 (included with the basic processor) to 16,384 word locations of 4-microsecond core storage in 4,096-word modules. Systems using the Model II Processor can have from 4,096 (included with the basic processor) to 65,536 word locations of 2-microsecond core storage in 4,096-word modules. Each core storage word contains 18 data bits and one parity bit. Each 18-bit word can hold one instruction, three alphameric characters, or an 18-bit binary data item. Thirty-two locations of core storage contain a permanently-wired "bootstrap" routine to facilitate program loading and error recovery.

The 418 Central Processor can perform a full complement of fixed-point arithmetic, Boolean, comparison, and shifting operations on 18-bit binary operands. Double-precision addition, subtraction, and shifting are also provided. The UNIVAC 418 has no automatic facilities for double-precision multiplication and division, floating-point arithmetic, decimal arithmetic, editing operations, multi-word internal transfers, or radix conversion. There are eight index registers, with instructions to step and test, increment, store, and load them. Only one of the eight index registers at a time, as selected by a separate instruction, can be used for address modification. Indirect addressing is not provided except for "Jump Indirect" instructions.

Instructions which reference core storage contain a single 12-bit address. This restricts the number of locations directly accessible at any time to one module of 4,096 words unless indexing is used. The particular module being addressed is indicated by a special register, by the Program Address Counter, or by an index register.

Average execution time for UNIVAC 418 instructions is about 4 microseconds for the Model II Central Processor and 8 microseconds for the Model I Processor. The longest instruction - Divide - requires 24 microseconds (48 microseconds for Model I), while a few instructions require as little as 2 microseconds (4 microseconds for Model I).

The program interrupt facility causes a transfer of control to one of 51 fixed core locations upon completion of an input-output operation, upon detection of an illegal operation code or input-output error, upon underflow of the Delta Clock, or upon an interrupt from the Day Clock.

The UNIVAC 418 can have 8, 12, or 16 input-output channels. If the Console keyboard-printer is used, it must be assigned to channel 0; the remaining channels are for general input-output use. Many of the standard peripheral subsystems require two channels, as indicated below. In general, each subsystem can handle one data transfer operation at a time. The maximum gross data transfer rate (or "saturation rate") for all simultaneously-operating peripheral devices ranges from 135,000 to 200,000 words per second for the Model II Central Processor, depending upon the channel requirements of the various subsystems. The gross data rate for the Model I Processor ranges from 62,500 to 100,000 words per second.

Two types of peripheral interfaces are used in the 418 system, depending upon the channel requirements of the subsystem used. Subsystems which use one input-output channel require 4 core memory cycles to transfer 18 bits (one word) of data. Subsystems using two input-output channels require 5 memory cycles to transfer 36 bits (two words) of data.

Each UNIVAC 418 peripheral subsystem can consist of any of the following groups of input-output devices and their associated control units:

- 1 Flying Head 220 Magnetic Drum. This drum stores 65,536 words with an average access time of 8.5 milliseconds. Peak data transfer rate is 7,700 words per second with an interlace factor of 4. One input-output channel is required.

- 1 to 5 Flying Head 330 Magnetic Drums. Each drum stores 262,144 words with an average access time of 8.5 milliseconds. Peak data transfer rate is 30,000 words per second with an interlace factor of 2. Interlace factors of 4, 8, or 16 can alternatively be used to achieve lower effective transfer rates. One input-output channel is required.

- 1 to 8 Flying Head 880 Magnetic Drums. Each drum stores 1,572,864 words with an average access time of 17 milliseconds. Peak data transfer rate is 60,000 words per second. Interlace factors of 2, 4, 8, or 16 can be used for lower effective transfer rates. Two input-output channels are required.

- 1 to 8 Fastrand I Mass Storage Units. Each unit has 2 drums, served by 64 movable read/write heads, and stores 22,020,096 words with an average access time of 93 milliseconds. A single Fastrand I Subsystem can store up to 528 million characters. Peak data transfer rate in UNIVAC 418 systems is 52,685 words per second with an interlace factor of 3. Interlace factors of 5, 7, and 9 can be used for lower transfer rates. Two input-output channels are required.

- 1 to 8 Fastrand II Mass Storage Units. Each unit stores 44,040,192 words; otherwise its characteristics are the same as Fastrand I.

- 2 to 12 Uniservo IIA Magnetic Tape Handlers. These units read forward or backward at a peak transfer rate of 12,500 or 25,000 rows per second. Eight tracks are recorded on 1/2-inch-wide tape at a density of 125 or 250 rows per inch, with row parity checking of read operations only. Two input-output channels are required.

- 2 to 16 Uniservo IIIA Magnetic Tape Handlers. These units read forward or backward at a peak transfer rate of 100,000 rows per second. Nine tracks are recorded on 1/2-inch-wide tape at a density of 1,000 rows per inch, with read-after-write row parity checking. Two input-output channels are required.

(Contd.)

- 2 to 12 Uniservo IIIC or IVC Magnetic Tape Handlers. These units can read forward only, at a peak transfer rate of 22,500, 62,500, or (IVC only) 90,000 rows per second. The tape format is fully compatible with the IBM 729 and 7330 Magnetic Tape Units. One input-output channel is required; two channels must be used if simultaneous read/read or read/write operations are desired. Two channels may alternatively be used to reduce central processor delays.
- 2 to 16 Uniservo VIC Magnetic Tape Handlers. These units can read forward only, at a peak transfer rate of 8,500, 24,000, or 34,000 rows per second. The tape format is fully compatible with the IBM 729 and 7330 Magnetic Tape Units. One input-output channel is required; two channels must be used if simultaneous read/read or read/write operations are desired.
- 1 High-Speed Printer. This unit uses a 63-character set and prints up to 700 alphameric lines or 922 numeric lines per minute. Two input-output channels are required.
- 1 Paper Tape Reader and 1 Paper Tape Punch. These units (housed in a single cabinet on the console desk) can read punched tape of up to 8 levels at up to 200 characters per second and punch standard 5-6-, 7-, or 8-level punched tape at 110 characters per second. One input-output channel (the same channel as used by the console keyboard-printer) is required.
- 1 UNIVAC 1004 Central Processor and associated peripherals. The 1004 provides the UNIVAC 418 with punched card input at 400 or 600 lines per minute. An optional card punch is available which punches cards at the rate of 200 per minute. The 1004 can also be equipped with magnetic tape and paper tape units. See Computer System Report 770 for full details. The 1004 subsystem requires one 418 input-output channel.
- Standard Communications Subsystem, consisting of up to 32 input and 32 output Communication Line Terminals connected to a Communication Multiplexer. These units enable the 418 to send and receive data via any common carrier at transmission rates of up to 4,800 bits per second. Two input-output channels are required.

Software

Programs which are available or currently being developed for the UNIVAC 418 can be summarized as follows:

- ART – An assembly system that translates symbolic source programs into machine language object programs in relocatable or absolute form. ART is a two-pass assembler unless a magnetic tape unit or drum is available for intermediate storage. An 8K 418 is required, with a program input and program output device, a card reader or magnetic tape unit for control input, and a 1004 printer. Assembly speed is approximately 400 lines per minute for a 12K 418-I Processor with Uniservo IIIC Tape Handlers.
- EXEC — An operating system capable of controlling four levels of programs: critical, real-time, batch, and computational, all operating concurrently. EXEC is designed to provide efficient utilization of the available system components and process scheduled jobs with a minimum of operator intervention. EXEC requires at least 1,491 words of core storage plus about 208 words per I/O handler routine. Times required to perform the EXEC functions associated with each input-output operation range from 0.52 to 1.19 milliseconds.
- FORTRAN IV — A compiler for the FORTRAN IV language has been announced, but no specifications are available to date.
- Sort/Merge — A three-phase program that utilizes the polyphase method of merge sorting with 3 to 12 Uniservo IIA or IIIC Tape Handlers or a Fastrand Mass Storage Unit. A 12K 418 is required, and additional core storage can be utilized when available.
- Utility Routines — include data transcription functions, dump and trace routines, tape and drum maintenance, and inspect and change routines.

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	18 bits + parity bit	basic addressable unit of storage in core and drum storage.
Row (Uniservo IIA):	8 bits (6 data, 1 parity, 1 sprocket)	magnetic tape; holds 1 character or 1/3 of a word.
Row (Uniservo IIIA - 100KC):	7 bits (6 data, 1 parity)	magnetic tape; holds 1 character or 1/3 of a word.
Row (Uniservo IIIA - 120KC):	9 bits (8 data, 1 parity)	magnetic tape; five rows hold two words.
Row (Uniservo IIIC, IVC, VIC):	7 bits (6 data, 1 parity)	magnetic tape; holds 1 character in IBM-compatible format.
Column:	12 positions	punched cards; usually holds 1 character.
Line:	132 positions	printer reports.
Block:	1 to N words	magnetic or punched tape.

.2 DATA FORMATS

Type of Information	Representation
Instruction:	1 word.
Fixed-point number:	1 word; 17 data bits and sign bit (or 2 words).
Alphameric character:	6 bits (internal), 1 row (tape), or 1 column (cards).
Card image (row binary):	5 words (4 with 18 bits and 1 with 8 bits) per card row; 60 consecutive words per card.
Card image (column binary):	1-1/2 card columns per word; 53-1/3 consecutive words per card.
Record:	1 to N words of logically related information.
File:	1 to N records.

SYSTEM CONFIGURATION

Every UNIVAC 418 computer system includes the following units:

- One of the following Central Processors:

  UNIVAC 418-I, with 4-μsec core storage ranging from 4,096 to 16,384 words in increments of 4,096 words; or

  UNIVAC 418-II, with 2-μsec core storage ranging from 4,096 to 65,536 words in increments of 4,096 words.

- Console Operator's Panel. A console keyboard-printer, console alarm, and day clock are available as options.

- Power Supply.

Eight input-output channels are included with the basic system. Eight more channels can be added, in increments of four, so that a fully expanded system will have sixteen input-output channels.

The following peripheral subsystems can be connected in any combination. Please refer to the Simultaneous Operations section (Page 790:111.101) of this Computer System Report for details on the capabilities for simultaneous operations of the various possible configurations.

- FH-220 Magnetic Drum Subsystem. Each subsystem has a capacity of 196,608 alphanumeric characters and an average access time of 8.5 milliseconds. The subsystem has its own Control and Synchronizer Unit and is connected to one input-output channel. See page 790:042.100 of this report for full details.

- FH-330 Magnetic Drum Subsystem. Each subsystem has a capacity of from 786,432 to 3,932,160 alphanumeric characters and an average access time of 8.5 milliseconds. The subsystem is connected via the FH-330 Drum Control and Synchronizer Unit to one input-output channel. See page 790:043.100 of this report for full details.

- FH-880 Magnetic Drum Subsystem. Each subsystem has a capacity of from 4.7 million to 37.7 million alphanumeric characters and an average access time of 17 milliseconds. The subsystem is connected via the FH-880 Drum Control and Synchronizer Unit to two input-output channels. See page 790:044.100 of this report for full details.

- Fastrand I Mass Storage Subsystem. Each subsystem has a capacity of from 66 million to 528 million alphanumeric characters and an average access time of 92 milliseconds. The subsystem is connected via the Fastrand I Control and Synchronizer Unit to two input-output channels. See page 790:045.100 of this report for full details.

- Fastrand II Mass Storage Subsystem. Each subsystem has a capacity of from 132 million to 1,056 million alphanumeric characters and an average access time of 92 milliseconds. The subsystem is connected via the Fastrand II Control and Synchronizer Unit to two input-output channels. See page 790:045.100 of this report for full details.

- Uniservo IIA Magnetic Tape Subsystem. These units operate at 12,500 or 25,000 characters per second at densities of 125 or 250 characters per inch, respectively. Two to twelve units can be connected to two I/O channels via the Uniservo IIA Control and Synchronizer Unit. One Uniservo Power Supply per 6 tape units is required. See page 790:091.100 of this report for full details.

- Uniservo IIIA Magnetic Tape Subsystem. These units operate at 100,000 or 120,000 characters per second. Recording density is 1,000 rows per inch in either case. Two to sixteen units can be connected to two input-output channels via the Uniservo IIIA Control and Synchronizer Unit. One Uniservo Power Supply per 6 tape units is required. See page 790:092.100 of this report for full details.
- Uniservo IIIC and IVC Magnetic Tape Subsystem. These units operate at 22,500, 62,500, or 90,000 (Uniservo IVC only) characters per second at densities of 200, 556, or 800 (IVC only) characters per inch, respectively. Two to twelve units can be connected to one (for read or write) or two (for simultaneous read/write or a 36-bit interface) input-output channels via the Uniservo IIIC and IVC Control and Synchronizer Unit. One Uniservo Power Supply per 6 tape units is required. See page 790:093.100 of this report for full details.
- Uniservo VIC Magnetic Tape Subsystem. This unit operates at 8,500, 23,700, or 34,200 characters per second at densities of 200, 556, or 800 characters per inch, respectively. One to four master tape units can be connected via the Uniservo VIC Control and Synchronizer Unit to one input-output channel. One to three additional tape units can be connected to each master tape unit. No additional power supply is needed. If simultaneous read/read or read/write is desired, two input-output channels must be used per subsystem. See page 790:094.100 of this report for full details.
- High-Speed Printer Subsystem. This unit is rated at 700 to 922 lines per minute. It is connected via the Printer Control and Synchronizer Unit to two input-output channels. See page 790:081.100 of this report for full details.
- Paper Tape Subsystem. This unit reads at 200 and punches at 110 rows per second; it has its own control unit and is directly connected to one input-output channel. See page 790:072.100 of this report for full details.
- Standard Communications Subsystem. One Communication Multiplexer serves up to 32 input and 32 output simplex (one-way) communication lines with a maximum transmission rate of 4,800 bits per second each. More than one Multiplexer can be used per subsystem by means of a Scanner/Selector. The subsystem is directly connected to two input-output channels. See page 790:101.100 of this report for full details.
- UNIVAC 1004 I, II, or III Subsystem. This subsystem consists of a plugboard-programmed processor and built-in peripheral units that can read cards at a peak rate of 400 or 615 cards per minute and can print at a peak rate of 400 or 600 lines per minute. An optional card punch is available which operates at 200 cards per minute. The 1004 can also be equipped with a paper tape reader and punch, and the 1004 Model III can have one or two 34KC magnetic tape units. The subsystem is connected via the 1004 Adapter Unit to one input-output channel of the 418. See page 790:071.100 of this report and Computer System Report 770 for full details about the UNIVAC 1004.

Selection of Representative System Configurations

The following standard configurations (as defined in the Users' Guide, page 4:030.100) are illustrated on the following pages:

- Configuration III; 6-Tape Business System.
- Configuration V; 6-Tape Auxiliary Storage System.
- Configuration VIIA; 10-Tape General System (Integrated).

Alternatives to the Illustrated Configurations

Configuration VIIA can be considered to be functionally equivalent to Configuration VIIB, the 10-Tape General System (Paired), if the UNIVAC 1004 is operated off-line instead of under direct control of the 418 Central Processor.

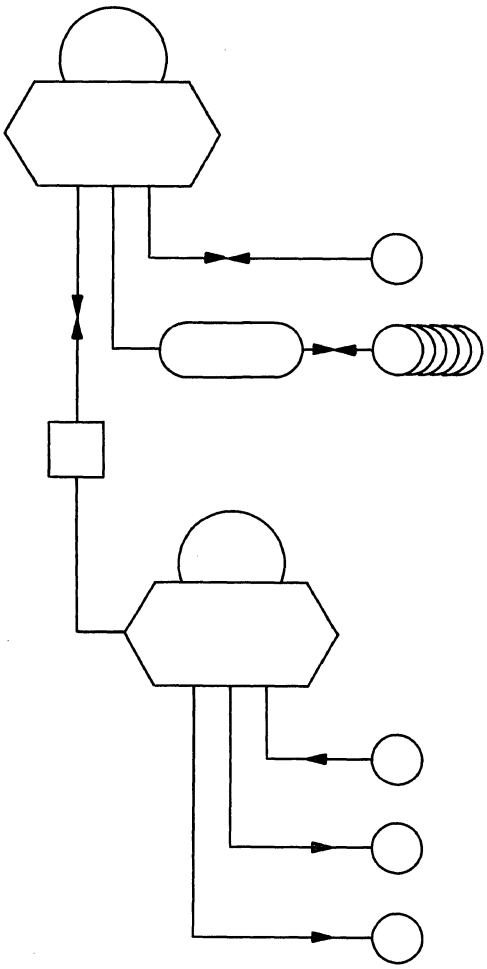
Additional Configuration Illustrated

Because the primary purpose of the UNIVAC 418 is to perform the functions of a message switching center, a Typical Communications System is illustrated on page 790:031.400.

(Contd.)

.1 6-TAPE BUSINESS SYSTEM; CONFIGURATION III

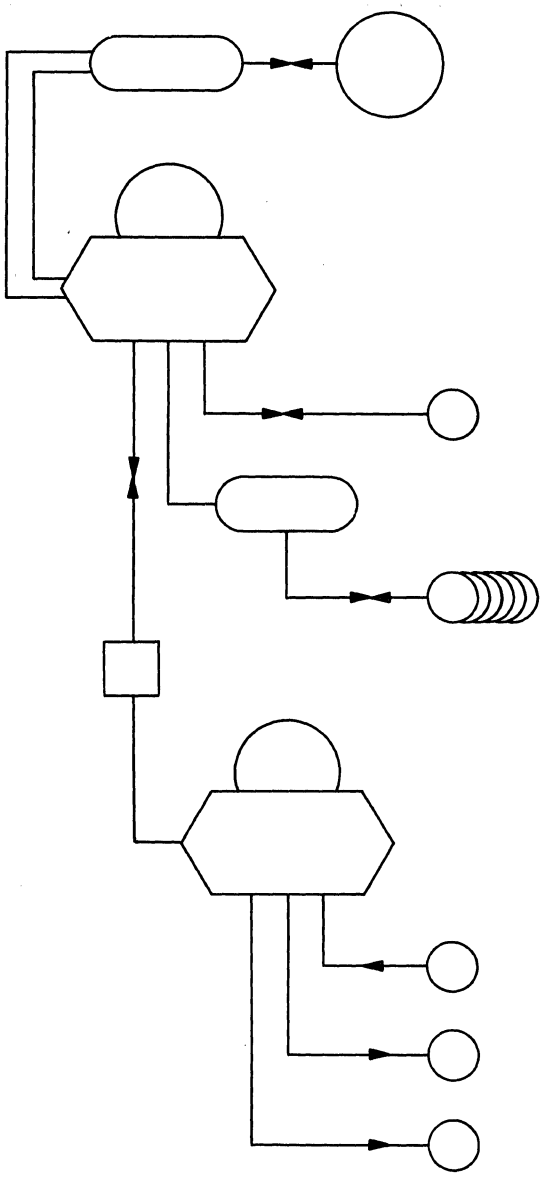
Deviations from Standard Configuration:. . . . . core storage is 40% larger.
card punch is 100% faster.
printer is 20% faster.
card reader is 20% faster.



Equipment	Rental
4,096 Additional Words of Core Storage	$ 350
UNIVAC 418-II Central Processor (2 μsec cycle time) — includes 4,096 words of Core Storage	2,050
Console (includes Keyboard-Printer)	250
Uniservo VIC Control	600
Master Uniservo VIC (2)	1,000
Additional Uniservo VIC (4): 34,200 char/sec	1,200
1004 Adapter	100
UNIVAC 1004 II Central Processor (6.5 μsec memory cycle; 961 characters of core storage)	
Includes:	1,275
Card Reader — 615 cards/minute	
Printer — 600 lines/minute	
1004 II Card Punch — 200 cards/minute	300
TOTAL RENTAL:	$7,125

.2 6-TAPE AUXILIARY STORAGE SYSTEM: CONFIGURATION V

Deviations from Standard Configuration:. . . . . auxiliary storage is 275% larger.
core storage is 40% larger.
card punch is 100% faster.
printer is 20% faster.
card reader is 20% faster.

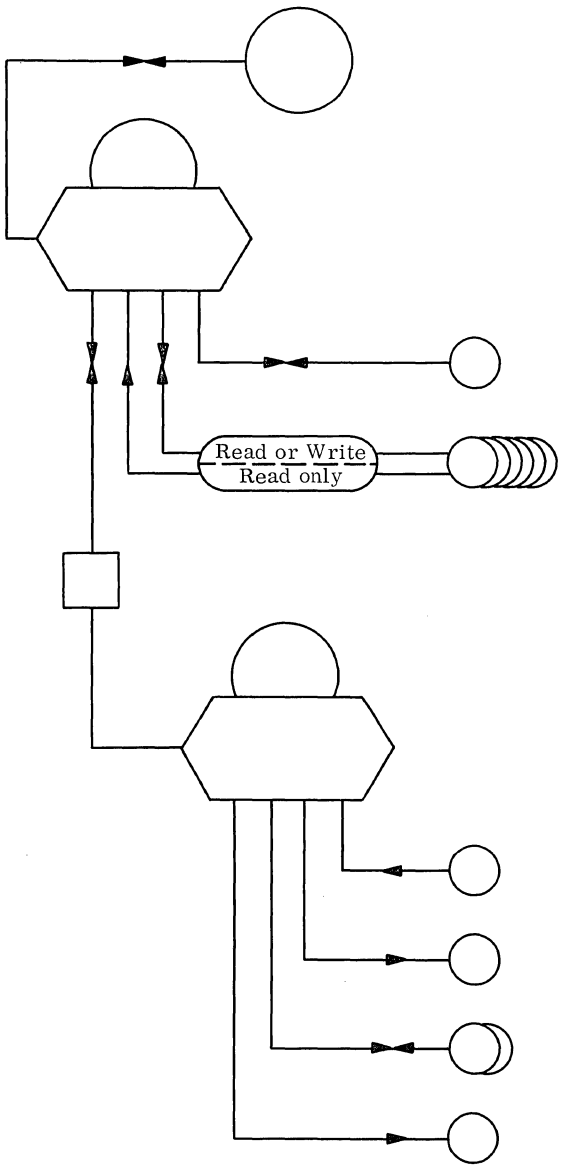


Equipment	Rental
Fastrand I Control Unit	$ 1,000
Fastrand I Storage Unit: 22,020,096 words (66 million characters)	3,300
4,096 Additional Words of Core Storage	350
UNIVAC 418-II Central Processor (2 μsec cycle time) — includes 4,096 words of Core Storage	2,050
Console (includes Keyboard-Printer)	250
Uniservo VIC Control	600
Master Uniservo VIC (2)	1,000
Additional Uniservo VIC (4): 34,200 char/sec	1,200
1004 Adapter	100
UNIVAC 1004 II Central Processor (6.5 μsec memory cycle; 961 characters of Core Storage)	
Includes:	1,275
Card Reader — 615 cards/minute	
Printer — 600 lines/minute	
1004 II Card Punch — 200 cards/minute	300
TOTAL RENTAL:	$11,425

(Contd.)

.3 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

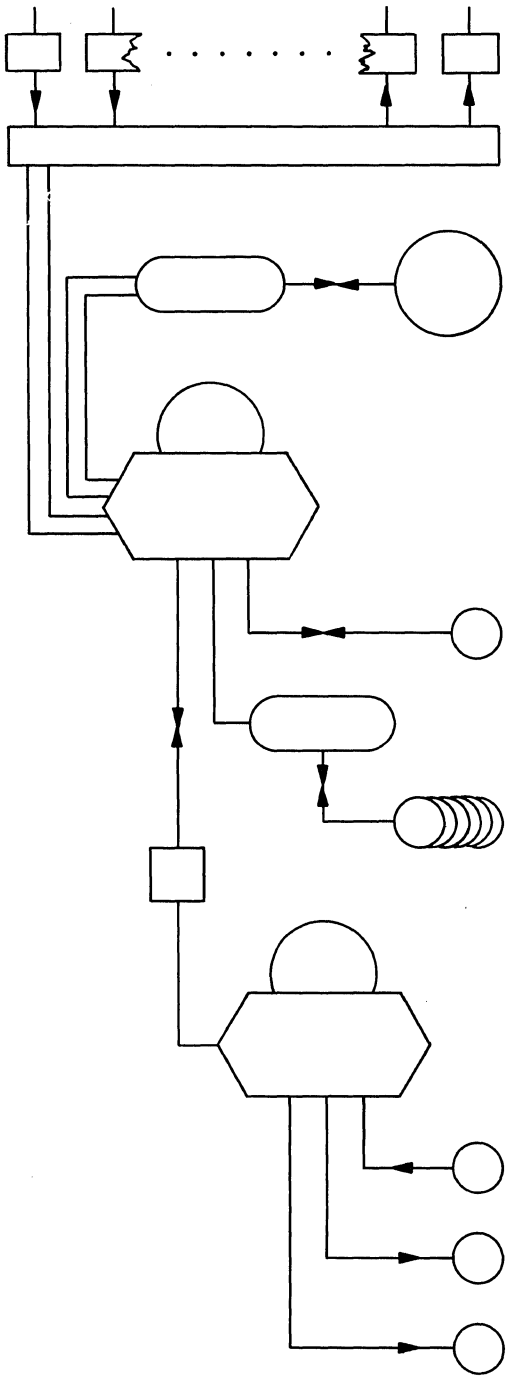
Deviations from Standard Configuration: . . . . . no floating-point hardware.
1004 system can be used on-line or off-line.
2 magnetic tapes (on 1004) are 50% slower.
card punch is 100% faster.
card reader is 20% faster.
printer is 20% faster.
drum is included to permit full use of standard software.



Equipment	Rental
FH-330 Magnetic Drum and Control and Synchronizer Unit: 786,432 alphameric characters	$ 2,000
24,576 Additional Words of Core Storage	2,100
UNIVAC 418-II Central Processor (2 μsec cycle) — includes 4,096 words of Core Storage	2,050
Console (with Keyboard-Printer)	250
Uniservo IVC Control: Dual-Channel model	1,970
Uniservo IVC Tape Units (8): 90,000 char/second*	6,400
Uniservo Power Supply (not shown)	430
800 char/inch option	200
1004 Adapter	100
UNIVAC 1004 III Processor (6.5 μsec memory cycle; 961 characters of Core Storage) Includes: 1004 Card Reader — 615 cards/minute; 1004 Printer — 600 lines/minute	1,275
1004 III Uniservo Tape Units (2) and Control: 33,664 char/sec	800
1004 III Card Punch — 200 cards/min	300
TOTAL RENTAL:	$17,875

* The standard configuration specifies 60KC tapes; the eight 90KC tape units can be rented for only $600 more and are considered a logical choice.

.4 TYPICAL COMMUNICATIONS SYSTEM



Equipment	Rental
Communication Line Terminals: up to 32 input and 32 output lines	*
Communication Multiplexer	$ 1,300
Fastrand Storage Unit & Synchronizer: 22,020,096 words	4,300
20,480 Additional Words of Core Storage	1,750
UNIVAC 418-II Central Processor (2 μsec cycle) — includes 4,096 words of Core Storage	2,050
Console (includes Keyboard-Printer)	250
Uniservo VIC Control	600
Master Uniservo VIC (2)	1,000
Additional Uniservo VIC (4): 34,200 char/sec	1,200
1004 Adapter	100
UNIVAC 1004 II Central Processor (6.5 μsec memory cycle; 961 characters of Core Storage)	
Includes:	1,275
Card Reader — 615 cards/min	
Printer — 600 lines/min	
1004 II Card Punch — 200 cards/min	300
TOTAL RENTAL:	$14,125*

* Costs of the necessary Communication Line Terminals and interface units are not included.

INTERNAL STORAGE: CORE STORAGE

.1 GENERAL

.11 Identity: . . . . . Core Storage (part of UNIVAC 418-I or 418-II Central Processor).

.12 Basic Use: . . . . . working storage.

.13 Description

UNIVAC 418 Core Storage is housed in the Central Processor cabinet and consists of one or more bays (banks) of 4,096 eighteen-bit word locations each. Two speeds of core storage are available. The 418-I Central Processor has a cycle time of 4 microseconds, while the 418-II Processor has a cycle time of 2 microseconds. The Model I Processor can use from 1 to 4 banks of storage, for a maximum capacity of 16,384 words. The Model II can use up to 16 banks, for a maximum capacity of 65,536 words of core storage. Each UNIVAC 418 word can hold one instruction, three alphanumeric characters, or a binary data item of 18 bits plus parity bit.

UNIVAC 418 instructions occupy one word each. Because of the limited number of bits per word, only 12 bits can be used for core storage addressing. Thus, only 4,096 locations can be directly referenced by any one instruction unless indexing is used. The desired core storage bank is indicated by the current setting of a Special Register, which can be changed or examined by the program. Most instructions call for the operand to be automatically modified by the Special Register. Twenty-five of the 78 instructions in the 418's repertoire can be indexed, and an indexed instruction can reference any location in core storage. No provision for multiple-word internal transfers has been made.

Core storage locations are reserved for index registers, input-output control, interrupt control, clocks, a scale factor, and (optionally) for communications multiplexing. A section of core storage contains a permanently-wired bootstrap routine which provides for input of programs ("bootstrap" operations) and automatic error recovery.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . June, 1963 (Model I).
November, 1964 (Model II).

.16 Reserved Storage

Purpose	Number of locations	Locks
Index registers:	8 (18 bits each)	none.
Arithmetic registers:	0.	
Logic registers:	0.	
I-O control:	32, 48, or 64 (optional)	none.
Interrupt control:	51, 75, or 99 (optional)	none.
Clocks:	4	none.
Bootstrap:	32	permanently wired.
Scale Factor:	1	none.
Multiplexing (optional):	8 to 128	none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes (except bootstrap).
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile:. . . . . no.
.244 Data permanent:. . . . . no.
.245 Storage changeable: . . no.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.283 Type of access: . . . . . uniform.

.29 Potential Transfer Rates

.292 Peak data rates —
Cycling rates:
Model I: . . . . . 250,000 cps.
Model II:. . . . . 500,000 cps.
Unit of data: . . . . . word.
Conversion factor: . . 18 bits and parity bit.
Data rate:
Model I: . . . . . 250,000 words/sec.
Model II:. . . . . 500,000 words/sec.
Compound data rate:
Model I: . . . . . 250,000 words/sec.
Model II:. . . . . 500,000 words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Core Memory Increment	Maximum Storage	Maximum Storage
Identity:	Basic UNIVAC 418-I or -II	UNIVAC 418-I or -II	UNIVAC 418-I	UNIVAC 418-II.
Words:	4,096	4,096	16,384	65,536.
Characters:	12,288	12,288	49,152	196,608.
Instructions:	4,096	4,096	16,384	65,536.
Modules:	1	1 each	4	16.

.32 Rules for Combining Modules

Model I Processor:. . . up to three 4,096-word increments can be added.
Model II Processor: . . up to fifteen 4,096-word increments can be added.

.4 CONTROLLER: . . . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: 1 access facility per system.

.52 Simultaneous Operations: . . . . . no facilities for interleaved accesses to independent storage banks.

.53 Access Time Parameters and Variations

.531 For uniform access —
Access time:
Model I: . . . . . 2 μsec.
Model II:. . . . . 1 μsec.
Cycle time:
Model I: . . . . . 4 μsec.
Model II:. . . . . 2 μsec.
For data unit of:. . . . 1 word.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With self: . . . . . 1 word.

.73 Effective Transfer Rate

With self —
Model I: . . . . . 62,500 words/sec.
Model II:. . . . . 125,000 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none.	
Invalid code:	check	interrupt.
Receipt of data:	check parity	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	check parity	interrupt.
Dispatch of data:	send parity bit.	
Timing conflicts:	check	resolved automatically by priority control network.

INTERNAL STORAGE: FH-220 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 220 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 220 Magnetic Drum is an economy auxiliary storage device that provides rapid random access to relatively small amounts of data or programs in UNIVAC 418 systems. Each subsystem is composed of one drum and an integrated control and synchronizer unit. A drum has 220 read-write heads, each serving one track. The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the rotating drum. The flying-head principle permits the use of larger drums with less critical tolerances, and the close head-to-drum spacing (0.0005 inch) permits high-density recording.

An FH-220 Magnetic Drum Subsystem consists of one drum and one controller and requires one input-output channel. Since a 418 can have up to 16 channels, a maximum of 16 FH-220 Magnetic Drum Subsystems could be connected if no other peripheral equipment were required. A subsystem has a storage capacity of 65,536 words. Maximum potential storage capacity is therefore 1,048,576 words per fully-expanded 418 system.

Of the 220 tracks on each drum, 128 are used for data bands of one track each. The other tracks are used for timing, reference marks, word marks, parity checking, and as spares. Data is read and recorded in bit-serial form. The FH-220 is sector-addressable. Each data track consists of four sectors, each containing 128 words. Drum speed is 3,600 revolutions per minute, so the average access time is 8.5 milliseconds. Peak data transfer rate is 7,700 words or 23,100 characters per second with the standard interlace factor of four.

Each drum read operation requires two instructions, two Buffer Control Words, and two Function Words. The instructions initiate the input buffer and external function on the appropriate input-output channel. The Buffer Control Words specify the initial and final core storage addresses. The Function Words specify the operation to be performed and the drum address. Coding of a drum write operation is similar. Drum search facilities are not provided. Writing in selected areas of the drum can be inhibited by means of manual lockout switches.

Checking includes a parity check to insure that each word read from the drum has odd parity. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Processor a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . June, 1963.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter:. . . . . 20 inches.
Thickness or length:. 28.5 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes (except locked-out areas).
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile:. . . . . no.
.244 Data permanent:. . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 1 Track

Words:. . . . . 512.
Characters:. . . . . 1,536.
Instructions: . . . . . 512.
Sectors: . . . . . 4.

.26 Bands per Physical Unit: . . . . . 128.

.27 Interleaving Levels: . . 4.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically supported head per track.
.283 Type of access —

Description of stage	Possible starting stage
Switch bands:.	when different band is selected (or at end of band).
Wait for specified sector:.	when previously selected band is used.
Read or write 1 to 512 sectors:	no.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 3,600 rpm.
Track/head speed: . . 3,780 inches/sec.
Bits/inch/track:. . . . 155.
Bit rate per track: . . 585,000 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 18 bits + parity bit per word.
Gain factor:. . . . . 1 track per band.
Loss factor: . . . . . 4 (interlace factor).
Date rate:. . . . . 7,700 words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum Storage
Drum subsystems:	1	16.
Drums:	1	16.
Words:	65,536	1,048,576.
Characters:	196,608	3,145,728.
Instructions:	65,536	1,048,576.
Sectors:	512	8,192.
Tracks:	128	2,048.

.32 Rules for Combining Modules: . . . . . one drum unit of 65,536 words per subsystem; 1 subsystem per input-output channel (a UNIVAC 418 system can have 8, 12, or 16 I/O channels).

.4 CONTROLLER

.41 Identity: . . . . . included with drum unit.

.42 Connection to System

.421 On-line: . . . . . 1 to 16 controllers; 1 per Magnetic Drum Subsystem.

.422 Off-line:. . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 FH-220 Drum Unit.
.432 Restrictions:. . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N words, beginning with the first word of a drum sector, where N is limited only by core storage capacity.
.442 Input-output area:. . . . core storage.
.443 Input-output area access:. . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization:. . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —
Stacks per drum: . . . 128.
Stacks per yoke:. . . . 16.
Yokes per module: . . 8.
.512 Stack movement: . . . . none.
.513 Stacks that can access any particular location:. . . . . 1.
.514 Accessible locations —
By single stack:. . . . 4 sectors.
By all stacks: . . . . . 512 sectors per drum.

.52 Simultaneous Operations:. . . . . none (only 1 operation at a time per FH-220 Subsystem).

.53 Access Time Parameters and Variations

.532 Variation in access time —

Stage	Variation, msec	Example, msec
Switch bands:	0 or 0.3	0.
Wait for specified sector:	0 to 16.7	8.5
Read or write:	0.13 per word	266.0*
Total:	0.13 to 17.13	274.5

*Based on a transfer of 2,048 words.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to N sectors; N is limited by core storage capacity.

.73 Effective Transfer Rate

With core storage: . . . 7,700 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none.	
Invalid function code:	none.	
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Reference to locked area:	check	interrupt.

INTERNAL STORAGE: FH-330 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 330 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 330 Magnetic Drum is an auxiliary storage device that provides rapid random access to moderately large quantities of data or programs in UNIVAC 418 systems. Each drum has 330 read-write heads, each serving one track. The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the rotating drum. The flying head principle permits the use of larger drums with less critical tolerances, and the close head-to-drum spacing (0.0005 inch) permits high-density recording.

An FH-330 Magnetic Drum Subsystem consists of from one to five Flying Head 330 Magnetic Drums connected to a Drum Control and Synchronizer Unit. Each subsystem requires one input-output channel. Since a 418 can have up to 16 channels, a maximum of 16 FH-330 Magnetic Drum Subsystems could be connected if no other peripheral equipment were required. Each drum has a storage capacity of 262,144 words of 18 bits each. Maximum potential storage capacity is therefore 1,310,720 words per subsystem and 20,971,520 words per fully-expanded 418 system.

Of the 330 tracks on each drum, 256 are used for data bands of one track each. The other 74 tracks are used for parity checking, timing, reference, and as spares. Data is read and recorded in bit-serial form. Data is transferred between an FH-330 Drum and the 418 in units of 18 bits. The Model II Central Processor is delayed 8 microseconds for each word transferred. (Delay time is 16 microseconds per word in the slower Model I Central Processor.)

Each data band consists of 1,024 word locations of three characters each. Drum speed is 3,600 revolutions per minute, so the average access time is 8.5 milliseconds. Peak data transfer rate is 30,000 words or 90,000 characters per second. An interlace factor of 2, 4, 8, or 16 is usually used in UNIVAC 418 systems, corresponding to a data rate of 30,000, 15,000, 7,500 or 3,750 words per second.

From 1 word to the capacity of core storage can be transferred in a single operation. Each drum read operation requires two instructions, two Buffer Control Words, and two Function Words. The instructions initiate the input buffer and external function on the appropriate input-output channel. The Buffer Control Words specify the initial and final core storage addresses. The Function Words specify the operation to be performed and the initial drum address. Coding of a drum write operation is similar. A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired. Writing in specified areas of the drum can be inhibited by means of manual lockout switches.

Checking includes a parity check to insure that each word read from the drum has odd parity, and checks for invalid drum addresses and function codes. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Processor a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . January, 1965.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter:. . . . . 20 inches.
Length:. . . . . 28.5 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes (except locked-out areas).

.242 Data regenerated constantly: . . . . . no.

.243 Data volatile:. . . . . no.

.244 Data permanent:. . . . . no.

.245 Storage changeable: . . no.

.25 Data Volume per Band of 1 Track

Words:. . . . . 1,024.
Characters:. . . . . 3,072.
Instructions: 1,024

.26 Bands per Physical Unit: . . . . . 256.

.27 Interleaving Levels: . . 2, 4, 8, or 16.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically supported head per track.

.283 Type of access —

Description of stage	Possible starting stage
Switch bands:.	when different band is selected (or at end of band).
Wait for specified sector:.	when previously selected band is used.
Read or write 1 to N words:	no.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 3,600 rpm.
Track/head speed: . . 3,780 inches/sec.
Bits/inch/track:. . . . 150.
Bit rate per track: . . 570,000 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 18 bits + parity bit.
Gain factor:. . . . . 1 track per band.
Loss factor: . . . . . 2, 4, 8, or 16 (interlace factor).

Data rate:

Interlace Factor	Words/sec	Char/sec
2	30,000	90,000
4	15,000	45,000
8	7,500	22,500
16	3,750	11,250

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum per Subsystem	Maximum Storage
Drum subsystems:	1	1	16.
Drums:	1	5	80.
Words:	262,144	1,310,720	20,971,520.
Characters:	786,432	3,932,160	62,914,560.
Instructions:	262,144	1,310,720	20,971,520.

.32 Rules for Combining Modules:. . . . . 1 to 5 Drum Units per Magnetic Drum Subsystem; 1 subsystem per input/output channel. A UNIVAC 418 system can have 8, 12, or 16 input/output channels.

.4 CONTROLLER

.41 Identity:. . . . . FH-330 Drum Control and Synchronizer Unit.

.42 Connection to System

.421 On-line:. . . . . 1 to 16 controllers (1 per input-output channel).
.422 Off-line:. . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 5 FH-330 Drum Units.
.432 Restrictions:. . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N words; N limited by size of core storage.
.442 Input-output area:. . . . core storage.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization:. . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of data stacks —
Stacks per drum: . . . 256.
Stacks per subsystem: . . . . . 256 to 1,280.
.512 Stack movement: . . . . none.
.513 Stacks that can access any particular location:. . . . . 1.
.514 Accessible locations —
By single stack:. . . . 1,024.
By all stacks: . . . . . 262,144 per drum. maximum of 1,131,720 per subsystem.

.52 Simultaneous Operations:. . . . . maximum of 1 data transfer operation per Magnetic Drum Subsystem.

.53 Access Time Parameters and Variations

.532 Variation in access time —

Stage	Variation, msec	Example, msec
Switch bands:.	0	0.
Wait for specified sector:.	0 to 17.0	8.5
Read or write:.	0.033 to 0.250 per word	67.6*
Total:	0.033 to 17.25	76.1

*Example is based on a 2,048-word transfer.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to N words; N is limited by size of core storage.

.73 Effective Transfer Rate

With core storage: . . . 3,750 to 30,000 words per second, depending on interlace option used.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Reference to locked area:	check	interrupt.

INTERNAL STORAGE: FH-880 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 880 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 880 Magnetic Drum is an auxiliary storage device that provides rapid random access to moderately large quantities of data or programs in UNIVAC 418 systems. Each drum has 880 read-write heads, each serving one track. The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the rotating drum. The flying head principle permits the use of larger drums with less critical tolerances, and the close head-to-drum spacing (0.0005 inch) permits high-density recording. The FH-880 provides greater storage capacity than the FH-330 but has slower access times and is more expensive.

An FH-880 Magnetic Drum Subsystem consists of from one to eight Flying Head 880 Magnetic Drums connected to a Drum Control and Synchronizer Unit. Each subsystem requires two input-output channels. Since a 418 can have a maximum of 16 channels, a maximum of 8 Magnetic Drum Subsystems could be connected if no other peripheral equipment were required. Each drum has a storage capacity of 1,572,864 words of 18 bits each. Maximum potential storage capacity is therefore 12,532,912 words per subsystem and 100,663,296 words per fully-expanded 418 system.

Of the 880 tracks on each drum, 768 are grouped into 128 data bands of six tracks each. The other 112 tracks are used for parity checking, timing, reference, and as spares. Each 418 word is converted by the Synchronizer into three 6-bit characters. The six tracks in each data band are read and recorded in parallel, and each word is stored in a three-by-six matrix of bit positions. An odd parity bit is generated for each word and recorded in a corresponding location in one of 32 parity tracks.

Data is transferred between the FH-880 and the 418 in groups of 36 bits. The Model II Central Processor is delayed 10 microseconds for every two words transferred. (Delay time for the slower Model I Central Processor is 20 microseconds per two words transferred).

Each data band consists of 12,288 word locations arranged in the form of three interleaved "angular sections" of 4,096 words each. This means that any location can be accessed within one drum revolution, but only 4,096 words can be read or recorded per revolution. Drum speed is 1,800 revolutions per minute, so the average access time is 17 milliseconds. Peak data transfer rate is 60,000 words or 180,000 characters per second, using an interlace factor of 1 (i.e., 1 drum revolution to read or write a single full angular section). Optional interlace factors of 2, 4, 8, or 16 slow down the data transfer rate by the corresponding factor.

From 1 word to the full capacity of core storage can be transferred in a single operation. Each drum read operation requires two instructions, two Buffer Control Words, and two Function Words. The instructions initiate the input buffer and external function on the appropriate input-output channel. The Buffer Control Words specify the initial and final core storage addresses. The Function Words specify the operation to be performed and the initial drum address. Coding of a drum write operation is similar. A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired.

Checking includes a parity check to insure that each word read from the drum has odd parity, and checks for invalid drum addresses and function codes. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Computer a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 9 to 12 months.

.15 First Delivery: . . . . . September 1962.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter:. . . . . 24 inches.
Length:. . . . . 30 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile:. . . . . no.
.244 Data permanent:. . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 6 Tracks

Words: . . . . . 12,288.
Characters:. . . . . 36,864.
Instructions: . . . . . 12,288.

.26 Bands per Physical Unit: . . . . . 128.

.27 Interleaving Levels: . . three interleaved "angular sections"; in addition, an optional "interlace factor" of 2, 4, 8, or 16 may be used to slow down the data transfer rate.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically supported head per track.

.283 Type of access —

Description of stage	Possible starting stage
Switch bands:.	when different band is selected (or at end of a band).
Wait for specified sector:.	when previously selected band is used.
Read or write 1 to N words:	no.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 1,800 rpm.
Track/head speed: . . 2,265 inches/sec.
Bits/inch/track:. . . . 518.
Bit rate per track: . . 1,173,270 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 18 bits per word.
Gain factor:. . . . . 6 tracks per band.
Loss factor: . . . . . 3 interleaving levels (always) times optional interlace factor of 1, 2, 4, 8, or 16.

Data rate:

Interlace Factor	Words/sec	Characters/sec
1	60,000	180,000
2	30,000	90,000
4	15,000	45,000
8	7,500	22,500
16	3,750	11,250

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum per Subsystem	Maximum Storage
Drum subsystems:	1	1	8.
Drums:	1	8	64.
Words:	1,572,864	12,582,912	100,663,296.
Characters:	4,718,592	37,748,736	301,989,888.
Instructions:	1,572,864	12,582,912	100,663,296.

.32 Rules for Combining Modules:. . . . . 1 to 8 Drum Units per Magnetic Drum Subsystem; 1 Magnetic Drum Subsystem per 2 input/output channels. A UNIVAC 418 system can have 8, 12, or 16 I/O channels.

.4 CONTROLLER

.41 Identity:. . . . . FH-880 Drum Control and Synchronizer Unit.

.42 Connection to System

.421 On-line:. . . . . 1 to 8 controllers; 1 per Magnetic Drum Subsystem.
.422 Off-line:. . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 8 FH-880 Drum Units.
.432 Restrictions:. . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N words; N is limited by size of core storage.
.442 Input-output area:. . . . core storage.
.443 Input-output area access:. . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization:. . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of data stacks —
Stacks per drum: . . . 128.
Stacks per subsystem:. . . . . 128 to 1,024.
.512 Stack movement: . . . . none.
.513 Stacks that can access any particular location:. . . . . 1.
.514 Accessible locations —
By single stack:. . . . 12,288.
By all stacks: . . . . . 1,572,864 per drum. maximum 12,582,912 per subsystem.

.52 Simultaneous Operations:. . . . . maximum of 1 data transfer operation per Magnetic Drum Subsystem.

(Contd.)

.53 Access Time Parameters and Variations

.532 Variation in access time —

Stage	Variation, msec	Example, msec
Switch bands:	0 or 0.134	0.
Wait for specified sector:	0 to 33.3	
Read or write:	0.0163 to 1,070*	33.3*
	0.0163 to 1,103	50.0

*16.3 μsec per word transferred; example is based on a 2,048-word transfer.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to N words; N is limited by size of core storage.

.73 Effective Transfer Rate

With core storage: . . . 3,750 to 60,000 words/sec, depending on the interlace option used.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit	interrupt.
Reference to locked area:	not possible.	

Note: The type of error is indicated by the Status Word, sent to the central processor when the interrupt occurs.

INTERNAL STORAGE: FASTRAND I AND II

.1 GENERAL

.11 Identity: . . . . . Fastrand I and II Mass Storage Subsystems.

.12 Basic Use: . . . . . Auxiliary storage.

.13 Description

The Fastrand Mass Storage Subsystem provides relatively fast random access to large quantities of data stored on magnetic drums. Two versions of the Fastrand Storage Unit are available. Fastrand II has twice the number of tracks per drum as Fastrand I, and therefore twice the data capacity. There is no difference in physical size or other characteristics.

Each Fastrand I Storage Unit has a capacity of 22,020,096 UNIVAC 418 words, or over 66 million characters; each Fastrand II Storage Unit, 44,040,192 words, or over 132 million characters. From one to eight storage units can be connected to a Fastrand Control and Synchronizer Unit to comprise a Fastrand Subsystem. One subsystem can be connected to any two UNIVAC 418 input-output channels. Since a 418 system can have up to 16 input-output channels, a maximum of 8 subsystems can be connected. Maximum storage capacity, therefore, ranges from 1.408 billion words or 4.224 billion characters, for systems incorporating Fastrand I, to 2.816 billion words or 8.454 billion characters for those using Fastrand II.

An option called Fastbands can be added to either type of Fastrand Storage Unit. It adds 24 tracks (258,048 characters) with 1 fixed head per track. The access time to records contained on these tracks depends only upon rotational delay and averages 35 milliseconds.

Each Fastrand Storage Unit contains two magnetic drums, which are treated as a single logical unit by the controller. There are 64 aerodynamically-supported read/write heads per Storage Unit (32 per drum). All 64 heads are connected to a common positioning mechanism and move in unison. Head positioning time varies from 30 to 86 milliseconds and averages 58 milliseconds. Drum speed is 870 revolutions per minute, so the rotational delay varies from 0 to 69 milliseconds and averages 35 milliseconds. Activation of addressing circuits requires 5 milliseconds, but this is overlapped with the other access time factors. Average random access time to any record is 93 milliseconds.

Peak data transfer rate is 52,685 words or 158,054 characters per second, using an interlace factor of 3 (i.e., 3 drum revolutions to read or write a single full track). Optional interlace factors of 5, 7, or 9 slow down the data transfer rate by the corresponding factor. The selected interlace factor applies to all Fastrand units within a subsystem and must be specified prior to delivery.

Each of the two drums in a Fastrand I Storage Unit has 3,072 data tracks, while each Fastrand II drum has 6,144 data tracks. Each track is divided into 64 sectors; and each sector holds 56 eighteen-bit UNIVAC 418 words, recorded serially by bit. The data storage area on each drum is divided into 96 (Fastrand I) or 192 (Fastrand II) "positions", with 32 tracks per position. The 32 tracks that constitute a position are sequentially addressed but are not physically adjacent to one another; each of the 32 tracks is served by a separate read/write head. Therefore, all the data in any one position (688,128 characters per Storage Unit) can be read and/or recorded without repositioning the heads. (This is analogous to the "cylinder" concept in IBM 1301 and 1311 Disk Storage.)

Every Fastrand read or write operation requires two instructions, two Function Words and two Buffer Control Words. The Function Words specify the operation to be performed and the initial drum address. The Buffer Control Words specify the core storage addresses of the first and last words to be transferred. Reading and writing must begin with the first word of the addressed sector and can continue over any number of sectors. The read or write operation is halted and an external interrupt signal is sent to the computer when: (1) the final core address specified in the Buffer Control Word is reached; (2) the end of the drum position is reached; (3) an error is detected; or (4) a "terminate" instruction is issued. Repositioning of the read/write heads to a different position is a separate operation, which can be carried out simultaneously in all the Fastrand Storage Units within a subsystem. Writing in selected areas of Fastrand storage can be inhibited by means of manual lockout switches.

Fastrand search operations cause the contents of a specified drum position to be searched until a bit-by-bit match is found to an Identifier Word stored in the controller. At this point a read operation is initiated. Alternative function codes permit searching every word or only the first two words of each drum sector. The search operations make no demands upon the central processor or core storage until a "find" is made.

Longitudinal check characters and phase-monitoring circuits are used for error detection and correction, providing for the recovery of up to 11 bits of missed data. (The form of the check characters and the technique used for error recovery are considered proprietary information.) Other checks are made for invalid addresses, illegal function codes, timing conflicts, and sector length errors. Detection of any error causes the controller to initiate an external interrupt and send the central processor a Status Word indicating the type of error and (in some cases) the Fastrand location at which it occurred.

(Contd.)

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . September, 1963 (Fastrand I).

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drums.

.22 Physical Dimensions

.222 Drum —
Diameter: . . . . . 23.8 inches.
Length: . . . . . 61.2 inches, effective.
Number on shaft: . . . 1.
Number per Storage Unit: . . . . . 2.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes (except locked-out areas).
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 1 Track

Words: . . . . . 3,584.
Characters: . . . . . 10,752.
Instructions: . . . . . 3,584.
Sectors: . . . . . 64 (56 words each).
Address tags: . . . . . 1 (48 bits).

.26 Bands per Physical Unit

Fastrand I: . . . . . 3,072 per drum.
6,144 per Storage Unit.
Fastrand II: . . . . . 6,144 per drum.
12,288 per Storage Unit.

.27 Interleaving Levels: . . 3, 5, 7, or 9 (optional; must be selected before delivery).

.28 Access Techniques

.281 Recording method: . . . 64 moving heads per Storage Unit, connected to a common positioning mechanism.

.283 Type of access —

Description of stage	Possible starting stage
Move heads to specified position:	when a different position is selected.
Wait for specified sector:	when previously selected position is used.
Read or write 1 to N words:	when rotational delay is zero.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 870 rpm.
Track/head speed: . . 1,086 inches/sec.
Bits/inch/track: . . . . 1,000.
Bit rate per track: . . 1,086,000 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 18 bits per word.
Gain factor: . . . . . 1 track per band.
Loss factor: . . . . . 3, 5, 7, or 9 interleaving levels.

Data rate:

Interlace option	Words/sec	Characters/sec
3	52,685	158,054
5	30,611	91,833
7	22,579	67,737
9	17,562	52,686

.3 DATA CAPACITY

.31 Module and System Sizes

Fastrand I	Minimum Storage	Maximum per Subsystem	Maximum Storage
Subsystems:	1	1	8
Storage Units:	1	8	64
Drums:	2	16	128
Words:	22,020,096	176×10^6	$1,408 \times 10^6$
Characters:	66,060,288	528×10^6	$4,224 \times 10^6$
Instructions:	22,020,096	176×10^6	$1,408 \times 10^6$
Sectors:	393,216	3,145,728	25,165,824.
Fastrand II			
Subsystems:	1	1	8
Storage Units:	1	8	64
Drums:	2	16	128
Words:	44,040,192	352×10^6	$2,816 \times 10^6$
Characters:	132,100,576	$1,056 \times 10^6$	$8,454 \times 10^6$
Instructions:	44,040,192	352×10^6	$2,816 \times 10^6$
Sectors:	786,432	6,291,456	50,331,648.

.32 Rules for Combining Modules: . . . . . 1 to 8 Storage Units per Fastrand Subsystem; 1 to 8 subsystems per UNIVAC 418 system. Each subsystem requires 2 input-output channels.

.4 CONTROLLER

.41 Identity: . . . . . Fastrand Control and Synchronizer.

.42 Connection to System

.421 On-Line: . . . . . 1 to 8 controllers; 1 per Fastrand Subsystem.
.422 Off-Line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 8 Fastrand Storage Units.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N words, beginning with the first word of a drum sector, where N is limited by core storage capacity.
.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization: . . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —
Stacks per Fastrand Subsystem: . . . . . 64 to 512.
Stacks per storage unit: . . . . . 64.
Stacks per drum: . . . 32.
Stacks per yoke: . . . . 64.
Yokes per storage unit: . . . . . 1.
.512 Stack movement: . . . . all 64 stacks in a Storage Unit move in unison to 1 of 96 or 192 discrete positions, depending on the model.
.513 Stacks that can access any particular location: . . . . . 1.
.514 Accessible locations:
By single stack —
With no movement: . 64 sectors.
With all movement: . 6,144 sectors.
By all stacks —
With no movement: . 4,096 sectors per storage unit.
up to 32,768 sectors per subsystem.
.515 Relationship between stacks and locations: . bits 6-11 of Lower Function Word designate head address.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer or search operation per Fastrand Subsystem, and 1 head-positioning operation per Fastrand Storage Unit.

.53 Access Time Parameters and Variations

.532 Variation in access time —

Stage	Variation, μsec	Average, μsec
Activate addressing circuits:	5,000*	*
Position heads:	0 or 30,000 to 86,000	58,000
Wait for specified sector:	0 to 69,000	35,000
Read or write:	see Para. .292	—
Total:	5,000 to 155,000	93,000

*Usually overlapped with other timing factors.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to N words, beginning with the first word of a drum sector, where N is limited only by core storage capacity.

.73 Effective Transfer Rate

With core storage —

Interlace option	Words/sec	Characters/sec
3	17,562	52,685.
5	10,204	30,611.
7	17,326	22,579.
9	5,854	17,562.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Recording of data:	record check character.	
Recovery of data:	check character and phase monitoring	interrupt.
Timing conflicts:	check	interrupt.
Physical record missing:	check	interrupt.
Reference to locked area:	check	interrupt.
Sector length error:	check	interrupt.
End of position reached:	check	interrupt.

Note: The type of error is indicated by the Status Word, sent to the central processor when the interrupt occurs.

CENTRAL PROCESSORS

.1 GENERAL

.11 Identity: . . . . . UNIVAC 418 Central Processor. Models I and II.

.12 Description

The UNIVAC 418 Central Processor consists of a single cabinet that houses the system's arithmetic and control sections, the input-output section, and core storage. The Processor is available in two models. Model I has a maximum capacity of 16,384 words of 4-microsecond core storage, while Model II can have up to 65,536 words of 2-microsecond core storage. In both models, core storage is available in 4,096-word increments.

Each UNIVAC 418 instruction is one word (18 bits) in length. Those instructions which reference core storage locations can accommodate only one 12-bit address. Thus, only 4,096 core storage locations can be directly addressed by any one instruction unless indexing is used. The particular 4,096-word module referenced is indicated by a 5-bit Special Register, by the Program Address Counter (P-register), or by the active index register, if any.

There are 78 basic instructions, 25 of which can be modified by indexing. Eight index registers are provided, but only the one specified by the Index Control Register setting can be referenced at any particular time. Indirect addressing is not provided, although "jump indirect" instructions exist. The UNIVAC 418 instruction repertoire includes a full complement of fixed-point arithmetic, Boolean, comparison, and shift operations on 18-bit binary operands. Special instructions are provided to test and increment the counters of the eight index registers or of any core location.

Facilities not provided in the instruction repertoire include floating-point arithmetic and double-precision multiply/divide (although double-precision add/subtract is available). This will generally limit high-speed computations to fixed-point 18-bit precision. However, instructions which round to single precision, scale for floating point, and test for overflow are provided.

Other facilities not included are editing, decimal arithmetic, multiword internal transfers, radix conversions, and table look-up. Generalized subroutines or complex sequences of instructions are therefore required to accomplish these important operations.

Execution time is 4 microseconds (8 microseconds in the Model I Processor) for most UNIVAC 418 instructions that reference an operand in core storage. When the operand is contained in the instruction itself (as a 12-bit literal), the execution time is generally lower. Address modification by indexing increases instruction execution times by 2 microseconds (4 microseconds in Model I). In addition, if the number of the particular index register desired is not currently contained in the Index Control Register, an extra 2 microseconds (4 microseconds in Model I) is required to load the new index register number.

Program interrupts occur upon normal completion of an input-output operation (optional), upon detection of an input-output or processor error, upon underflow of the program-settable Delta Clock, and from the Day Clock at plugboard-defined intervals. Control is transferred to one of 51 fixed locations (for an 8-channel system), depending upon the cause of interruption. Only the contents of the instruction sequence counter can be automatically saved when an interrupt occurs, so the routine that services the interrupt condition (usually EXEC) must preserve and restore the previous contents of all the registers it uses. The interrupt facility makes it possible to perform real-time operations and batch processing operations concurrently, under control of the Executive System (EXEC), described on page 790:191.100.

The UNIVAC 418 has two electronic chronometers. The Delta Clock is decremented 1,024 times per second. An interrupt is received at the end of each second, causing the clock location to be reset and the current time to be updated. An optional Day Clock is available; its function is to provide time indications in decimal representation, with or without initiating interrupts.

.13 Availability: . . . . . 9 months.

.14 First Delivery: . . . . June, 1963 (Model I). November, 1964 (Model II).

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point —			
Add-subtract:	automatic	binary	18 or 36 bits.
Multiply:			
Short:	none.		
Long:	automatic	binary	18 bits.
Divide:			
No remainder:	none.		
Remainder:	automatic	binary	18 bits.

	Operation and Variation	Provision	Radix	Size
.212	Floating point:	subroutines.		
.213	Boolean —			
	AND:	automatic	binary	18 bits.
	Inclusive OR:	automatic	binary	18 bits.
	Exclusive OR:	automatic	binary	18 bits.
	Complement:	automatic	binary	18 or 36 bits.
	Selective substitute:	automatic	binary	18 bits.
.214	Comparison —			
	Numbers:	automatic	binary	18 bits.
	Absolute:	none.		
	Letters:	automatic	binary	18 bits.
	Mixed:	automatic	binary	18 bits.
	Collating sequence:	according to binary values of character codes.		

		Provision
.215	Code translation:	none.
.216	Radix conversion:	none.
.217	Edit format —	
	Alter size:	none.
	Suppress zero:	none.
	Round off:	automatic
	Insert point:	none.
	Insert spaces:	none.
	Protection:	none.
.218	Table look-up:	none.

		Provision	Comment	Size
.219	Others —			
	Shifts:	automatic	right shifts are end off; left shifts are end around.	18 or 36 bits.
	Scale:	automatic	useful in floating-point manipulations.	36 bits.

.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement.

.222 Zero: . . . . . plus or minus zero (treated as equal in arithmetic operations).

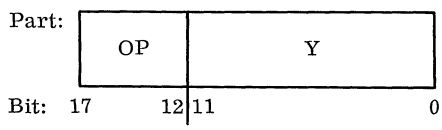
.223 Operand size determination: . . . . . implied by instruction (one or two words).

.23 Instruction Formats

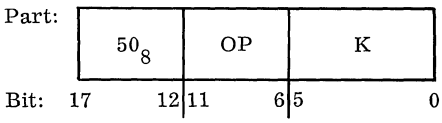
.231 Instruction structure: . . . . . 1 word; format implied by instruction operation code.

.232 Instruction layout:

Memory Reference Format



Non-Memory Reference Format (I/O, shifts, etc.)



.233 Instruction parts —

Name	Purpose
OP:	specifies operation code and indexing (if possible).
Y:	specifies a 12-bit operand address or a literal operand.
K:	specifies a shift count, channel number, or some other indicator.

.234 Basic address structure: . . . . . 1 + 0.

(Contd.)

.235 Literals —
Arithmetic: . . . . . addition only; 18 bits.
Comparisons and tests: . . . . . no.
Incrementing modifiers: . . . . . no.
.236 Directly addressed operands —
.2361 Internal storage type: . . . . . core storage.
Minimum size: . . . . 1 word.
Maximum size: . . . . 2 words.
Volume accessible: . . 4,096 words.
.2363 Increased address capacity —
Method: . . . . . modification by P-register, Special Register, and/or an index register.
Volume accessible: . a specified 4,096-word module.
.237 Address indexing —
.2371 Number of methods: . 1.
.2372 Name: . . . . . indexing.
.2373 Indexing rule: . . . . . add contents of specified index register to operand address.
.2374 Index specification: . "1" is added to octal Function Code to indicate indexing is to be performed. The index register to be used is indicated by the Index Control Register.
.2375 Number of potential indexers: . . . . . 8.
.2376 Address which can be indexed —
Type of address: . . operands of 19 instructions.
Application: . . . . . compare, arithmetic, load and store, unconditional jumps.
.2377 Cumulative indexing: . . . . . none.
.2378 Combined index and step: . . . . . none.
.238 Indirect addressing: . only by means of "jump indirect" instructions.
.239 Stepping —
.2391 Specification of increment: . . . . . implied by instruction, or contained in instruction as a literal.
.2392 Increment sign: . . . tally (-); index (+ or -).
.2393 Size of increment: . -2048 to + 2048.
.2394 End value: . . . . . implied as zero or specified in core storage.
.2395 Combined step and test: . . . . . yes.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . 1 (P-Register).
.314 Special sub-sequence counters: . . . . . none.
.315 Sequence control step size: . . . . . 1 word (2 words on skips).
.316 Accessibility to routines: . . . . . P-register contents can be stored in core storage by "Store Location Jump" instructions.
.317 Permanent or optional modifier: . . . . . no.

.32 Look-Ahead: . . . . . none.

.33 Interruption

.331 Possible causes —
In-out subsystems: . completion of input-output operation or input-output error.
Storage access: . . completion of magnetic drum operation or drum error.
Processor errors: . illegal function code.
Other: . . . . . Delta Clock underflow or Day Clock interval completion.
.332 Control by routine —
Individual control: . . can enable or prevent all interrupts, or only external interrupts, by special instructions.
Note: A program can cause an interrupt (and entrance to EXEC) by means of an illegal function code.
Method: . . . . . when an interrupt occurs, all other interrupts are disabled until they are re-enabled by a special instruction.
Restriction: . . . . . enable or disable instruction can be used only by the EXEC program.
.333 Operator control: . . . . the console typewriter can initiate an external interrupt for unsolicited type-ins.

.24 Special Processor Storage

Category of storage	Number of locations	Size in bits	Program usage
Arithmetic section:	3	18 each	arithmetic registers (AU and AL) and adder.
Control section:	1	16	Program Address Counter (P-Register).
Special Register:	1	5	indicates current 4K storage bank.
Index Control Register:	1	3	indicates current index register.

.334 Interruption conditions: . . . . . interrupt must be enabled. If in a priority routine (EXEC), the interrupt is placed in a queue and handled at a later time. If in a non-priority routine, the routine is temporarily suspended and the interrupt is then processed. If processor is idle, the interrupt is handled immediately.

.335 Interruption process —
Disabling interruption:. . . . . automatic.
Registers saved: . . . contents of P-register (sequence counter) are saved by a "Store Location and Jump" instruction in the particular interrupt location; other registers are saved by the EXEC routine.
Destination: . . . . . 3 fixed locations per I/O channel, depending on type of interrupt: input, output, or external.

.34 Multiprogramming

.341 Method of control: . . . by EXEC (see Page 790:191.100), using the interrupt facilities described above.

.342 Maximum number of programs: . . . . . limited only by hardware availability.

.343 Precedence rules: . . . see paragraph 790:191.12.

.344 Program protection —
Storage: . . . . . none.
In-out units: . . . . . only via assignment by EXEC of specific units to specific programs.

.35 Multi-sequencing: . . practical only in multi-computer complexes.

.4 PROCESSOR SPEEDS

.41 Instruction Times In Microseconds

Note: All figures given below are for the Model II Processor (2 μsec cycle). Times for the Model I Processor are exactly twice those shown.

.411 Fixed point —
Add-subtract: . . . . 4.0 (1 word); 6.0 (2 words).
Multiply: . . . . . 13.33 to 24.67
Divide: 24.0

.412 Floating point (performed by subroutines)
Add: . . . . . 203 to 218.
Subtract: . . . . . 212 to 227.
Multiply: . . . . . 290 to 345.
Divide: . . . . . 290 to 365.

.413 Additional allowance for —
Indexing: . . . . . 2.0 (+2.0 more if Index Control Register must be loaded).
Indirect addressing: 2.0 ("jump indirect" instructions only).
Re-complementing:. 0.0

.414 Control —
Compare: 4.0
Branch: 2.0
Compare and Branch: 6.0

.415 Counter control —
Step: 6.0
Step and test: 6.0
Test: 6.0

.416 Edit: . . . . . none.

.417 Convert: . . . . . none.

.418 Shift: . . . . . 2.67 + K/3, where K = number of bits shifted.

.42 Processor Performance in Microseconds

	Fixed point	Floating point
.421 For random addresses —		
$c = a + b$:	12.	273 to 288.
$b = a + b$:	12.	273 to 288.
Sum N items	4N.	257N to 272N.
$c = ab$:	27 average.	360 to 415.
$c = a/b$:	36.	360 to 435.
.422 For arrays of data —		
$c_i = a_i + b_j$:	36.	303 to 318.
$b_j = a_i + b_j$:	34.	303 to 318.
Sum N items:	12N.	269N to 284N.
$c = c + a_i b_j$:	51 average.	392 to 447.
.423 Branch based on comparison —		
Numeric data:	32.	
Alphabetic data:	32.	
.424 Switching —		
Unchecked:	14.3	
Checked:.	22.3	
List search:	14 + 18N.	
.425 Format control, per character —		
Unpack:	1.8	
Compose:	31.5 (estimate, for generalized subroutines).	
.426 Table look-up, per comparison —		
For a match:	18.	
For least or greatest:	18.4	
For interpolation point:	18.	
.427 Bit indicators —		
Set bit in pattern:	12.	
Test bit in pattern:	10.	
.428 Moving:	8 per word.	

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	set indicator.
Zero divisor (divide overflow):	check	set indicator.
Invalid data:	none.	
Invalid operation:	check	interrupt.
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	

CONSOLE

.1 GENERAL

.11 Identity: . . . . . Operator's Panel (Maintenance Panel).

.12 Associated Units: . . . . Programmer's Console. Keyboard and Printer. Paper Tape Subsystem (see page 790:072.100).

13 Description

The Operator's Panel (Figure 1) is mounted on the side of the UNIVAC 418 Central Processor cabinet and can be operated from a standing position. The panel may be used both for maintenance and for debugging and monitoring of programs. Included on the Operator's Panel are switches, lights, and buttons that enable an operator to:

- Turn the power supply on or off.
- Clear all indicators.
- Monitor and control input-output operations.
- Display or alter the contents of core storage locations and registers.
- Start or stop the execution of a program.
- Initiate an Operator Request interrupt.
- Execute single instructions or phases of an instruction (clock pulses).
- Set program-testable switches.
- Operate the console off-line.
- Initiate a bootstrap routine.
- Run a program on "slow clock" (i.e., execute an instruction every 10 seconds). This is of great value for on-line debugging.

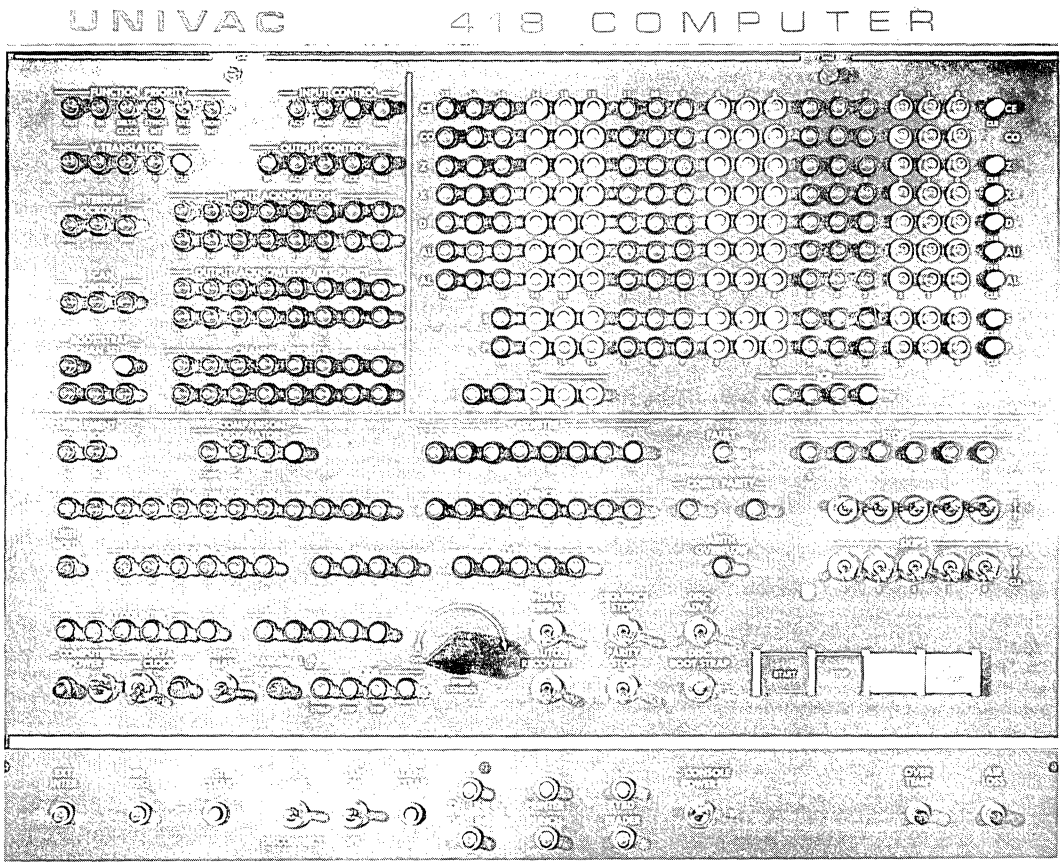


FIGURE 1: UNIVAC 418 OPERATOR'S PANEL

.13 Description (Contd.)

The Operator's Panel contains neon indicator lights which display the contents of all data registers. Each indicator light is also a push-button, facilitating modification of the contents of individual bit locations of the registers.

The Programmer's Console (Figure 2) consists of a desk with a keyboard-printer and controls for the Standard Communications Subsystem mounted on top. Options available on the console are an audible console alarm and a paper tape reader and punch (see page 790:072.100 for details).

The Keyboard is a standard typewriter keyboard that can generate the 64 basic Fieldata character codes. There are 51 keys for operator control, including alphanumeric keys, shift and shift lock keys, space bar, and return. The console Printer is the Teletype Model 35 Page Printer, which prints 1 character at a time at a peak speed of 10 characters per second. It can print 60 or 61 symbols and perform space, carriage return, and line feed functions. Vertical spacing is 6 lines per inch; horizontal spacing is 10 characters per inch. The printer will accept paper widths of up to 8.5 inches.

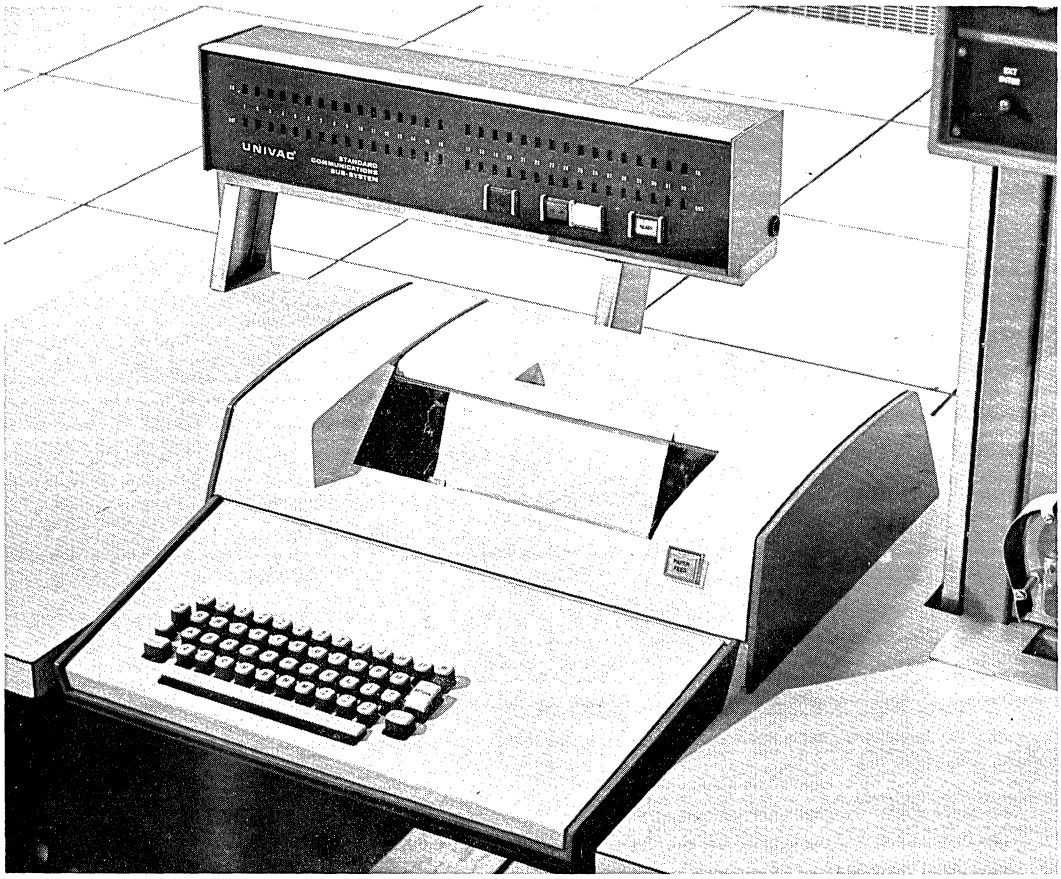


FIGURE 2: UNIVAC 418 PROGRAMMER'S CONSOLE

(Photos courtesy of UNIVAC Division, Sperry Rand Corp.)

INPUT–OUTPUT: UNIVAC 1004

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 Processor; Models I, II, and III. UNIVAC 1004 Adapter.

.12 Description

The UNIVAC 1004 is a small, plugboard-programmed computer with 961 or 1,922 positions of core storage. It can be connected to the UNIVAC 418 by means of the 1004 Adapter, enabling transmisson of data, in one direction at a time, between 418 core storage and 1004 core storage. The 1004 Subsystem provides the principal means for connecting card reading and punching equipment to a 418 system. It can also provide data editing, code translation, and similar data manipulation facilities independently of the 418 program. All operations must be initiated by the 418 program, or by the plugboard wiring under control of the 418 program; i.e., the UNIVAC 1004 cannot act as an inquiry station for the 418. When it is not in use as an on-line peripheral subsystem for the 418, the UNIVAC 1004 can be used as an off-line data processor, under sole control of its plugboard wiring.

Some of the important characteristics of the 1004 are:

- Plugboard programming.
- 961 or 1,922 positions of core storage.
- 31, 47, or 62 program steps.
- 8 μsec cycle time for the 1004 Model I; 6.5 μsec cycle time for Models II and III.
- Editing and decimal arithmetic facilities.
- Maximum card reading rate of 400 or 615 cards/minute, depending upon the model.
- Maximum printing rate of 400 or 600 lines/minute, depending upon the model.
- 132 alphanumeric printing positions.
- 63-character printing set.
- Optional card punch — 200 cards/minute.
- Punched paper tape units available — 400 char/sec reading and 110 char/sec punching.
- One or two magnetic tape units can be connected: up to 33,664 characters per second at densities of 200, 556, or 800 characters per inch.

For more detailed information on the capabilities and performance of the UNIVAC 1004, see Computer System Report 770.

A UNIVAC 1004 operation is initiated in the same way as other 418 peripheral operations. Eighteen functions are provided, including Read Card, Punch Card, Space 1 Line, etc. For functions that cause data to be transferred, a data IN or OUT instruction follows transmittal of the function code to the 1004. Output is performed without monitor interrupt. Following a data OUT, or a positioning function, an input instruction to obtain a one-word acknowledge character is performed. Error analysis, scheduling of input-output functions, and provision for simultaneity of 1004 operations are handled by the 418 Executive System (EXEC).

Data is transmitted one word at a time to or from the 418, interlocking core storage for four cycles per transmitted word. Except during interprocessor data transmission, the 1004 operates independently of the 418. The 1004 Subsystem requires one UNIVAC 418 input-output channel and can run simultaneously with all other peripherals. Since a 418 system can have a maximum of 16 channels, up to sixteen 1004 Subsystems could be connected to a UNIVAC 418 Central Processor if no other peripherals were used.

INPUT–OUTPUT: PAPER TAPE SUBSYSTEM

.1 GENERAL

.11 Identity: . . . . . Paper Tape Subsystem.

.12 Description

The UNIVAC 418 Paper Tape Subsystem reads paper tape at 200 characters per second and punches tape at 110 characters per second. The Paper Tape Subsystem does not include a Channel Synchronizer for the assembly of characters into 418 words, so the subsystem must communicate with the Central Processor on a character-by-character basis.

The subsystem is located on the Programmer's Console, and it alternates with the console in communicating with the Central Processor via Channel 0. Selection of either the Paper Tape Subsystem or the console keyboard-printer is done initially by means of a button on the operator's panel and subsequently by internal commands. The Paper Tape Subsystem requires one input-output channel (the same channel used for the Programmer's Console).

The input-output channel is used to transfer data in units of 18 bits (each unit containing only one paper tape frame and control signals). The Central Processor is delayed for 4 core storage cycles per unit of data transferred; this takes 8 microseconds per character in the Model II Processor and 16 microseconds in the Model I Processor. Reading and punching can be done concurrently; however, communication with the Central Processor by both units cannot occur at any given instant. No automatic checks for errors are made. Parity bits, when required, must be generated and/or checked by programmed routines.

Paper tape of up to eight levels plus sprocket holes can be read; 5, 6, 7, or 8 levels can be punched. Varying tape widths can be used. Oiled, opaque paper tape in roll form is recommended. Supply reels are provided on both the reader and punch units. Bins are provided for take-up.

The Paper Tape Subsystem can be used for off-line tape preparation in conjunction with the console keyboard-printer.

The paper tape reader is manufactured by Digitronics Corporation, and the punch is a Teletype BRPE unit.

INPUT–OUTPUT: PRINTER (700/922 LPM)

.1 GENERAL

.11 Identity: . . . . . High-Speed Printer.

.12 Description

This printer can print alphanumeric data at 700 single-spaced lines per minute and numeric data (0-9, +, -, space) at up to 922 lines per minute. Printing is by an on-the-fly hammer stroke which presses the ribbon and paper against an engraved drum. There are 132 printing positions, each capable of printing any of the following 64 characters:

&	H	P	X	5	/	;	△
A	I	Q	Y	6	,	>	\
B	J	R	Z	7	$	:	≠
C	K	S	0	8	+	<	@
D	L	T	1	9	(	[	%
E	M	U	2	-	'	!	#
F	N	V	3	*	)	?	⌑
G	O	W	4	.	=	]	space

Printing is on continuous, sprocket-punched stationery ranging from 4 to 22 inches in width and up to 22 inches per sheet in length. An original and up to 5 carbon copies of good quality can be produced. Vertical spacing is 6 or 8 lines per inch, as selected by the operator. Horizontal spacing is 10 characters per inch. The full 132-character print line can be placed anywhere in the print area of a form up to 16.5 inches in width. When 22-inch-wide forms are used, however, only the central 13.2-inch portion can be printed upon.

Single-line spacing requires 20 milliseconds or less, and skipping speed is 20 inches per second. The forms can be advanced from 0 to 63 lines prior to printing each line. There is no forms control loop to permit skipping to predefined points on a form, so spacing is usually controlled by software.

Controls are provided which allow the operator to shift the paper horizontally by at least one character in either direction and vertically by at least one line in either direction. These adjustments can be made while the printer is operating.

One printer can be connected to a Control and Synchronizer Unit, forming a High-Speed Printer Subsystem. Each subsystem requires 2 UNIVAC 418 input-output channels.

The Central Processor is delayed for 5 cycles for each 2 words transferred. Thus, printing one line requires 0.22 milliseconds of central processor time in the Model II Processor and 0.44 milliseconds in the Model I Processor.

TABLE I: EFFECTIVE SPEED OF 700/922 LPM PRINTER

Lines Advanced per Line Printed (6 lines per inch)	Printed Lines per Minute Using 64 Character Set	Printed Lines per Minute Using Numeric Set
1	700	922
2	638	818
3	586	735
4	542	667
5	504	611
6 (1 inch)	472	563
12 (2 inches)	338	383
18 (3 inches)	264	291
24 (4 inches)	217	234
30 (5 inches)	183	196

INPUT–OUTPUT: UNISERVO IIA

.1 GENERAL

.11 Identity: . . . . . Uniservo IIA Magnetic Tape Handler.

.12 Description

The Uniservo IIA provides magnetic tape input-output for the UNIVAC 418 at substantially lower speed and cost than the newer Uniservo IIIA, IIIC, and IVC tape handlers described in the following report sections. (The IBM-compatible Uniservo VIC Tape Handlers are slightly less expensive than the IIA's.) A Magnetic Tape Subsystem consists of 2 to 12 Uniservo IIA Tape Handlers connected to a Uniservo IIA Control and Synchronizer Unit and a Power Supply. Each subsystem occupies two 418 input-output channels, and only one tape handler per subsystem can read or write at a time. A panel of dial switches is used to change the logical addresses assigned to the individual tape handlers.

Data can be recorded on either plastic-base or metallic tape at a packing density of 125 or 250 rows per inch. (Data recorded by the Unityper keyboard-to-magnetic-tape transcriber at 50 rows per inch can be read, but the Uniservo IIA cannot record at this density.) Tape velocity is 100 inches per second, providing a peak data transfer rate of 12,500 or 25,000 characters per second, depending upon the recording density selected. Each tape row contains six data bits, one clock bit, and one parity bit, and can represent one alphameric character. Three tape rows are used to represent each 18-bit 418 word. Block length is variable. Tape width and densities are compatible with those of the Uniservo II and IIA tape handlers used in the UNIVAC II, III, 1107, 490, and Solid-State 80/90 systems. There is no tape compatibility with the Uniservo IIIA, IIIC, IVC, or VIC tape handlers.

The UNIVAC 418 can have a maximum of 16 input-output channels. Since each Uniservo IIA subsystem requires two input-output channels, up to eight subsystems could be used with a 418 if no other peripheral equipment were required.

For a more detailed description of the mechanical characteristics of the Uniservo IIA, see Section 775:091 of the UNIVAC 490 Computer System Report.

.6 PERFORMANCE

.62 Speeds

.621 Nominal or peak speed —
At 250 rows/inch:. . . 25,000 char/sec.
At 125 rows/inch:. . . 12,500 char/sec.

.622 Important parameters —
Recording density: . . 120 or 250 rows/inch.
Tape speed: . . . . . 100 inches/sec.
Rewind speed: . . . . . 100 inches/sec.
Interblock gap: . . . . 1.05 inches.
End-of-file gap:. . . . 4.50 inches.
Start time: . . . . . 5 msec.
Stop time:. . . . . 5 msec.

.623 Overhead, per block —
Start/stop mode: . . 25.5 msec.
Continuous mode:. . 10.5 msec.

.624 Effective speeds —

250 Rows/Inch
Start/stop mode: . 25,000N/ (N + 638) char/sec.
Continuous mode:. 25,000N/ (N + 262) char/sec.

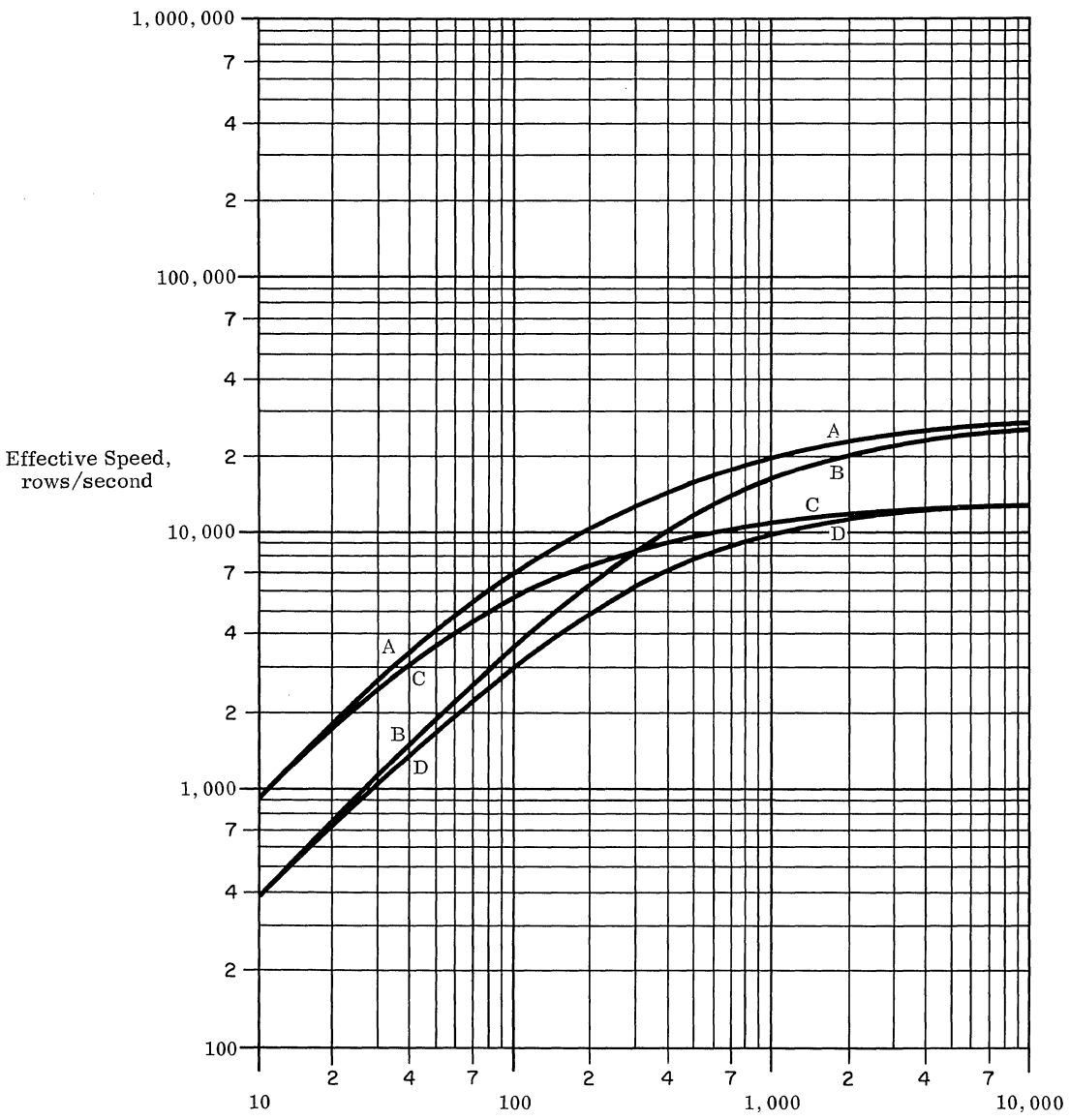
125 Rows/Inch
Start/stop mode: . 12,500N/ (N + 319) char/sec.
Continuous mode:. 12,500N/ (N + 131) char/sec. where N is the number of characters (i.e., tape rows) per block. (See graph.)

Note: The start/stop mode is used unless the next tape function is initiated within 4 msec after the last character of each block is read or written.

63 Demands on System

Component	Density, rows/inch	Msec per 2 words	Percentage of data transfer time
Central Processor, Model I:	250	0.020	8.0
	125	0.020	4.0
Central Processor, Model II:	250	0.010	4.0
	125	0.010	2.0

EFFECTIVE SPEED: UNISERVO IIA



LEGEND

Curve A — 250 rows/inch, continuous mode
Curve B — 250 rows/inch, start/stop mode
Curve C — 125 rows/inch, continuous mode
Curve D — 125 rows/inch, start/stop mode

INPUT–OUTPUT: UNISERVO IIIA

.1 GENERAL

.11 Identity: . . . . . Uniservo IIIA Magnetic Tape Handler.

.12 Description

The Uniservo IIIA provides high-speed magnetic tape input-output for the UNIVAC 418 system. From 2 to 16 Uniservo IIIA tape handlers can be connected to a Uniservo IIIA Control and Synchronizer Unit and a Uniservo Power Supply, forming a Magnetic Tape Subsystem. Each subsystem occupies two input-output channels, but only one tape handler per subsystem can read or write at a time. The UNIVAC 418 can have a maximum of 16 input-output channels. Since each Uniservo IIIA subsystem requires two input-output channels, up to eight subsystems could be used with a 418 if no other peripheral equipment were required.

Data is recorded by the "pulse phase" method at a density of 1,000 rows per inch. Nine tracks are recorded across the tape, one of which is always used as a parity track. In the standard recording format, five tape rows are used to represent two 18-bit 418 words; the first four rows contain eight data bits each, and the last row of each five-row group contains only four data bits. An optional format, selected through plugboard switching, uses three tape rows per word, with only six data bits (i.e. one alphameric character) per row. Tape velocity is 100 inches per second, providing the following peak data transfer rates:

	Standard Format (5 rows per 2 words)	Optional Format (3 rows per word)
Rows per second:	100,000	100,000
418 words per second:	40,000	33,333
6- bit characters per second:	120,000	100,000

For a more detailed description of the mechanical characteristics of the Uniservo IIIA, see Section 775:092 of the UNIVAC 490 Computer System Report.

.6 PERFORMANCE

.62 Speeds

.621 Nominal or peak speeds —

Standard format (5 tape rows per 2 words): . . . . . 40,000 words/sec or 120,000 alphameric characters/sec.

Optional format (3 tape rows per word): . . . . . 33,333 words/sec or 100,000 alphameric characters/sec.

.622 Important parameters —

Recording density: . . 1,000 rows/inch.
Tape speed:. . . . . 100 inches/sec.
Rewind speed: . . . . . 300 inches/sec.
Interblock gap:. . . . . 0.75 inch.
Start time: . . . . . 3 msec.
Stop time:. . . . . 3 msec.

.623 Overhead per block —

Start/stop mode: . . . 14.8 msec.
Continuous mode:. . . 8.2 msec.

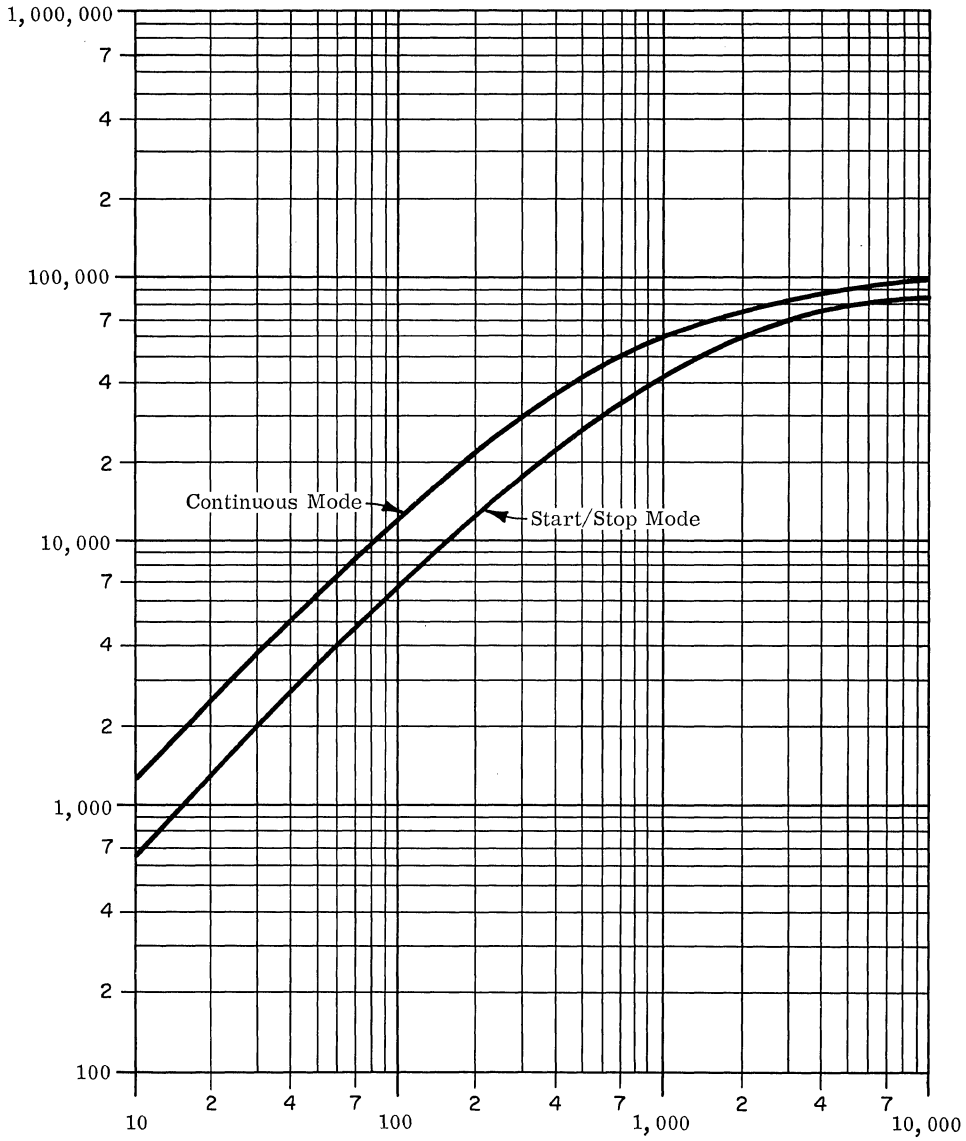
.624 Effective speeds —

Start/stop mode: . . . 100,000N/(N + 1480) rows/sec.
Continuous mode:. . . 100,000N/(N + 820) rows/sec. where N is number of rows per block. (See graph.)

.63 Demands on System

Component	Format	Msec per 2 words	Percentage of data transfer time
Central Processor, Model I:	standard	0.020	40.0
	optional	0.020	33.3
Central Processor, Model II:	standard	0.010	20.0
	optional	0.010	16.7

EFFECTIVE SPEED: UNISERVO IIIA



Note: 3 tape rows per 3-character 418 word or 5 tape rows per two 418 words, depending upon recording format.

INPUT–OUTPUT: UNISERVO IIIC AND IVC

.1 GENERAL

.11 Identity: . . . . . Uniservo IIIC and IVC Magnetic Tape Handlers.

.12 Description

The Uniservo IIIC and IVC provide UNIVAC 418 systems with magnetic tape input-output in a format compatible with all tape units currently produced by IBM except the Model 7340 Hypertape Drive and the new 2400 Series units. From 2 to 12 Uniservo IIIC or IVC Tape Handlers can be connected to a Tape Adapter Cabinet, which is in turn connected to a Uniservo IIIC or IVC Control and Synchronizer Unit and a Power Supply to comprise a Compatible Tape Subsystem.

Each subsystem ordinarily occupies one 418 input-output channel (there are up to 16 input-output channels available), and only one tape handler per subsystem can be reading or writing at any time. Alternatively, a dual-control synchronizer that requires two input-output channels can be used to control each Magnetic Tape Subsystem. In this case, simultaneous read/read or read/write (but not write/write) operations involving any two tape handlers in a subsystem can occur. The logical address assigned to each tape handler can be changed only by means of a plugboard on the Tape Adapter Cabinet.

Tape speed is 112.5 inches per second. Recording density may be either 200 or 556 rows per inch, providing a peak data transfer rate of 22,500 or 62,500 characters per second. A third recording density of 800 rows per inch is available in the IVC Tape Handler only, providing a transfer rate of 90,000 characters per second. Each tape row consists of six data bits and one parity bit, and can represent one alphameric character or one-third of a UNIVAC 418-word. As in IBM 700 and 7000 Series scientific systems, reading and writing can be performed in either the binary mode (with odd parity) or the BCD mode (with even parity). Block length is variable from one word to the capacity of core storage.

The Uniservo IIIC and IVC subsystems transfer data in units of 18 bits, regardless of whether the read/read-read/write overlap capability is used. An optional feature permits the subsystem to transfer data in units of 36 bits by using two input-output channels. This results in a reduction of central processor delay time. Another optional feature for the Uniservo IIIC and IVC is automatic code translation.

For a more detailed description of the mechanical characteristics of the Uniservo IIIC and IVC Tape Handlers, see Section 775:093 of the UNIVAC 490 Computer System Report.

.6 PERFORMANCE

.62 Speeds

.621 Nominal or peak speed —
- At 200 rows/inch: . . 22,500 char/sec.
- At 556 rows/inch: . . 62,500 char/sec.
- At 800 rows/inch: . . 90,000 char/sec.

.622 Important parameters —
- Recording density: . 200, 556, or 800 rows/inch.
- Tape speed: . . . . . 112.5 inches/sec.
- Rewind speed: . . . . 360 inches/sec.
- Interblock gap: . . . 0.75 inch.
- End-of-file gap: . . . 3.7 inches.
- Start time —
  - Read: . . . . . 6.3 msec.
  - Write: . . . . . 4.1 msec.
- Stop time —
  - Read: . . . . . 9.0 msec.
  - Write: . . . . . 9.0 msec.

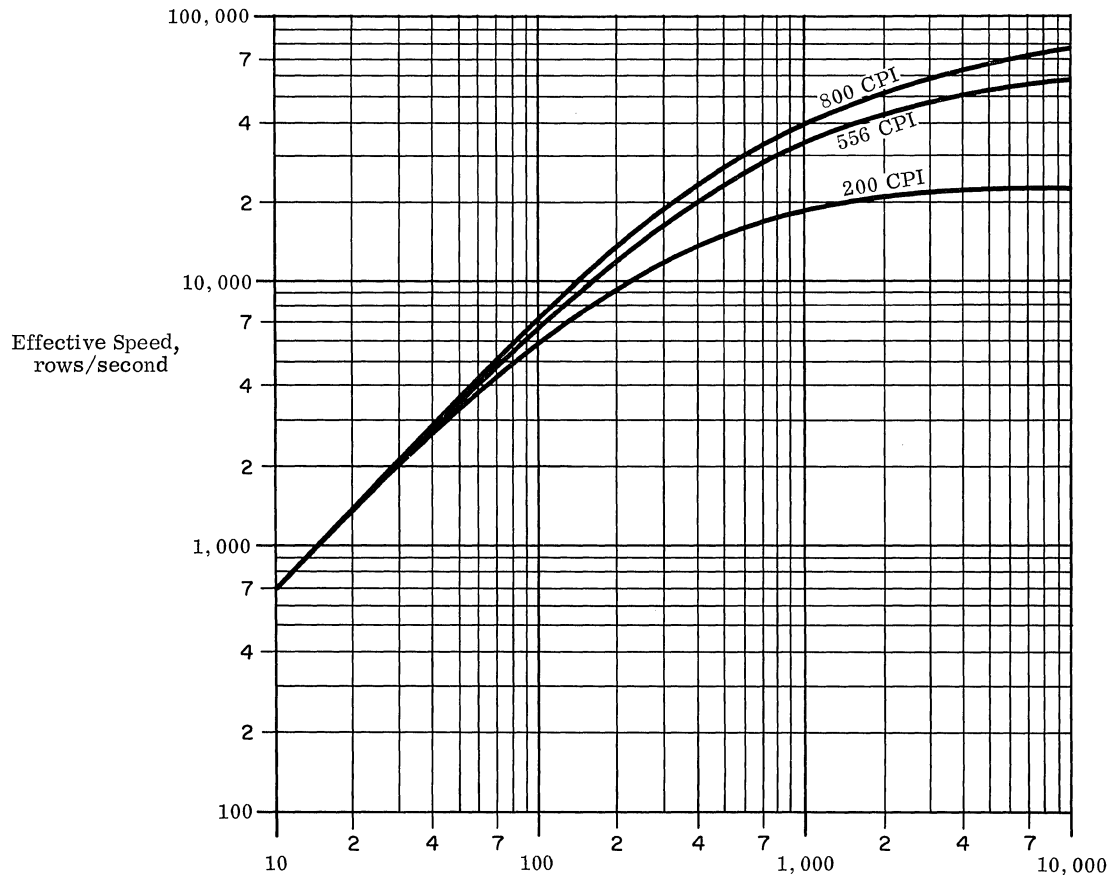
.623 Overhead (continuous mode), per block —
- Reading: . . . . . 14.2 msec.
- Writing: . . . . . 14.2 msec.

.624 Effective speeds —
- 200 rows/inch: . . . 22,500N/ (N + 319) char/sec.
- 556 rows/inch: . . . 62,500N/ (N + 887) char/sec.
- 800 rows/inch: . . . . 90,000N/ (N + 1,278) char/sec. where N is number of characters (i.e., tape rows) per block. (See graph.)

.63 Demands on System

Component	Type of interface	Density, rows/inch	msec per word	Percentage of data transfer time
Central Processor, Model I:	18 bits	200	0.016	12.2
		556	0.016	33.4
		800	0.016	48.4
	36 bits (optional)	200	0.010	7.6
		556	0.010	20.8
		800	0.010	30.4
Central Processor, Model II:	18 bits	200	0.008	6.1
		556	0.008	16.7
		800	0.008	24.2
	36 bits (optional)	200	0.005	3.8
		556	0.005	10.4
		800	0.005	15.2

EFFECTIVE SPEED: UNISERVO IIIC & IVC



Note: Effective speeds are based upon continuous operation, with no stops between blocks.

INPUT–OUTPUT: UNISERVO VIC

.1 GENERAL

.11 Identity: . . . . . Uniservo VIC Magnetic Tape Handler.

.12 Description

The Uniservo VIC Tape Handler is a new unit that is functionally similar to the Uniservo IIIC and IVC but has a substantially reduced tape speed (42.7 inches per second) and a significantly lower cost. The format of the Uniservo VIC is compatible with all currently-produced IBM magnetic tape drives except the Model 7340 Hypertape Drive and the new 2400 Series units. Automatic code conversion between UNIVAC 418 internal code and IBM 6-bit BCD code is optional, as in the Uniservo IIIC and IVC. If this feature is not installed, code conversion, when required, must be done by subroutines.

A Uniservo VIC Magnetic Tape Subsystem consists of a Synchronizer Unit, from 1 to 4 Control Units, and from 1 to 16 Uniservo VIC Magnetic Tape Handlers (1 to 4 tape handlers can be connected to each Control Unit). Each subsystem can be connected to either one or two input-output channels. The controllers are two-way units; thus, when two input-output channels are used, simultaneous read/read or read/write operations are possible involving any two tape handlers on two different controls. The Uniservo VIC Tape Handler can read only in the forward direction and cannot perform any skip or search operations.

Recording density can be either 200, 556, or 800 rows per inch, providing peak data transfer rates of 8,500, 23,700, or 34,100 characters per second, respectively. Each tape row consists of six data bits and one parity bit. Block length is variable from one word to the capacity of core storage. The External Function instruction specifies a read or write operation, the unit involved, the recording density, and whether or not an external interrupt shall occur upon successful completion of the operation. The size of a tape block is indicated by initial and final addresses in the Buffer Control Words. Error conditions are indicated by interrupts. The type of error is determined by a status code set in the Status Word.

For a detailed description of the mechanical characteristics of the Univervo VIC, see Section 777: 094 of the UNIVAC 1050 Computer System Report.

.6 PERFORMANCE

.62 Speeds

.621 Nominal or peak speed —

At 200 rows/inch: . .	8,500 char/sec.
At 556 rows/inch: . .	23,700 char/sec.
At 800 rows/inch: . .	34,100 char/sec.

.622 Important parameters —

Recording density: .	200, 556, or 800 rows/inch.
Tape speed:	42.7 inches/sec.
Full rewind time: . .	180 seconds.
Interblock gap: . . .	0.75 inch.
Start plus stop time:	24 msec.

.623 Overhead, per block: . . . . . 17.6 msec (continuous tape motion).

.624 Effective speeds —

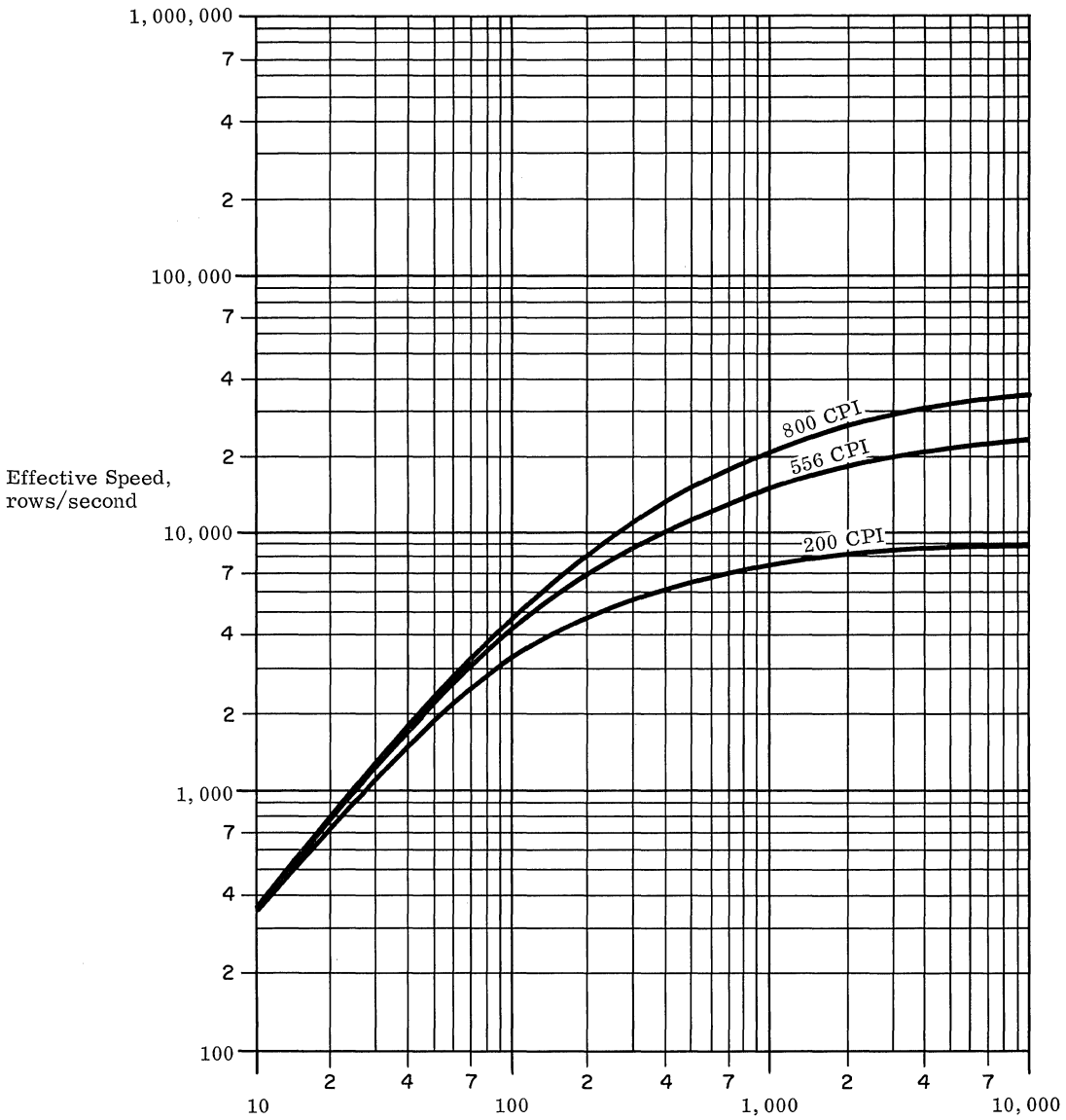
200 rows/inch: . . .	8,500N/ (N + 150) char/sec.
556 rows/inch: . . .	23,700N/ (N + 417) char/sec.
800 rows/inch: . . .	34,100N/ (N + 600) char/sec.

where N is number of characters (i.e., tape rows) per block. (See graph.)

.63 Demands on System

Component	Density, rows/inch	msec per word	Percentage of data transfer time
Central Processor, Model I:	200	0.016	4.6
	556	0.016	12.6
	800	0.016	18.4
Central Processor, Model II:	200	0.008	2.3
	556	0.008	6.3
	800	0.008	9.2

EFFECTIVE SPEED: UNISERVO VIC



Note: Effective speeds are based upon continuous operation, with no stops between blocks.

INPUT–OUTPUT: STANDARD COMMUNICATIONS SUBSYSTEM

.1 GENERAL

.11 Identity: . . . . . Standard Communications Subsystem, consisting of 1 to 64 Communication Line Terminals connected to a Communication Multiplexer.

.12 Description

The Standard Communications Subsystem enables the UNIVAC 418 to receive and transmit data via any common carrier, in any standard code of up to 8 levels, at any standard rate of transmission up to 4,800 bits per second. It can receive or transmit data via high-speed, medium-speed, or low-speed lines in any combination.

The two principal components of the Standard Communications Subsystem are the Communication Line Terminals (CLT's), which are connected directly to the communication facilities, and the Communication Multiplexer, which links up to 64 CLT's to the Central Processor. One or more Communication Multiplexers can be connected to a pair of the UNIVAC 418's input-output channels. (If necessary, more than one Communication Multiplexer can be connected to the same pair of computer input-output channels via a Scanner/Selector.)

The Standard Communications Subsystem requires two input-output channels. Data transfer is performed in the Request-Acknowledge mode. One input-output channel is used to transfer data, one word at a time. Each word holds only one data character. The second input-output channel is used to transmit the ESI (see below). The Central Processor is delayed 4 core storage cycles for each character transferred. This takes 8 microseconds per character in the Model II Central Processor and 16 microseconds in the Model I Processor.

Simultaneity

A special communications feature is the Externally Specified Index (ESI), which allows a number of communications networks to operate concurrently on a single pair of input-output channels by providing automatic sorting of incoming data and automatic collation of outgoing data. This ESI feature, which is built into the input-output logic, permits UNIVAC 490 communications peripherals to be used with the 418.

When the Standard Communications Subsystem is used, two core storage locations are reserved for each of the 64 possible communication lines. These locations contain the Buffer Control Words. In addition, two alternating core storage buffer areas are assigned to each line. The size and location of these buffer areas can be varied by the program.

A 15-bit code is transmitted along with each message character leaving or entering the Central Processor. This code, called the address ESI, identifies the Communication Line Terminal and Multiplexer and is available on the even-numbered channel of the dual channel pair. The ESI references a Buffer Control Word, which in turn indicates the location to or from which the character is to be sent. When a buffer has been filled (or emptied), an internal interrupt occurs, and the Buffer Control Words are modified by the EXEC operating system to reference the alternate buffer.

Thus, all Communication Line Terminals can be active simultaneously, with a minimum of program attention, so long as the gross data rate of all incoming and outgoing messages does not exceed 62,500 characters per second. This gross data transfer rate is determined by the length of time required for scanning and gating. In addition, messages can be transmitted or received while any other peripheral subsystem is operating and while the Central Processor is computing.

Communication Line Terminals

One CLT is required for each input line and each output line to be connected to a communication multiplexer. There are three basic types of input and output CLT's: low-speed (up to 300 bits per second), medium-speed (up to 1,600 bits per second), and high-speed (2,000 to 4,800 bits per second). The characteristics of the available CLT models are summarized in Table I.

A special type of output CLT is the CLT-Dialing, which enables the Central Processor to establish communication with a particular remote point via the common carrier's switching network. Each CLT-Dialing requires one output position on the Communication Multiplexer and is always used in conjunction with another output CLT, an input CLT, or (for two-way communication) both.

Communication Multiplexer

The Communication Multiplexer is available in five different models, capable of connecting the following maximum numbers of Communication Line Terminals to a pair of UNIVAC 418 input-output channels.

C/M-4:	2 input and 2 output CLT's
C/M-8:	4 input and 4 output CLT's
C/M-16:	8 input and 8 output CLT's
C/M-32:	16 input and 16 output CLT's
C/M-64:	32 input and 32 output CLT's.

When several CLT's simultaneously request access to core storage, the Communication Multiplexer assigns priorities and lets the Central Processor know which CLT has been granted access.

.12 Description (Contd.)

Types of Communication Service

Through the use of the appropriate Communication Line Terminals and associated common-carrier equipment, any or all of the following types of communication service can be tied into a UNIVAC 418 system:

- Private Line Teletypewriter: up to 100 words per minute; simplex, half duplex, or full duplex.
- Teletypewriter Exchange Service (TWX): 100 words per minute; half duplex.
- Direct Distance Dialing (DDD) or Wide Area Telephone Service (WATS): 1,200 to 2,000 bits per second; half duplex.
- Private Line Telephone: 2,000 bits per second and up; full or half duplex.

Optional Features

External Interrupt: With this feature, an external interrupt will occur either: (1) when an EOT code is received from an 8-level CLT, or (2) when a "no change of state" condition exists for a period varying from a minimum of one character transfer time to a maximum of 750 milliseconds, per individual asynchronous, lower speed, 5- or 8-level CLT.

TABLE I: COMMUNICATION LINE TERMINAL CHARACTERISTICS

Type No. (Input only)	Type No. (Output only)	Code Level (Bits/char)	Mode	Timing	Speed
CLT-51L	CLT-50L	5	Bit serial	Asynchronous	Up to 300 bits/sec.
CLT-81L	CLT-80L	6,7, or 8	Bit serial	Asynchronous	Up to 300 bits/sec
CLT-81M	CLT-80M	5,6,7, or 8	Bit serial	Asynchronous	Up to 1,600 bits/sec.
CLT-81P	CLT-80P	up to 8	Bit parallel	Timing Signal	Up to 75 char/sec.
CLT-81H	CLT-80H	5,6,7, or 8	Bit serial	Synchronous	2,000 to 4,800 bits/sec.
	CLT-Dialing	4	Bit parallel	Timing Signals	Determined by common carrier.

Note: "Asynchronous" means that start and stop bits are used with each character to establish timing; "Synchronous" means that timing characters are used at pre-determined intervals between data characters.

INPUT–OUTPUT: INTER–COMPUTER COUPLERS

.1 GENERAL

.11 Identity: . . . . . Inter-Computer Couplers.

418/UNIVAC III Channel Adapter.

.12 Description

The Inter-Computer Couplers permit the UNIVAC 418 to be used as a peripheral on-line subsystem for a UNIVAC 490, UNIVAC 1107/1108, UNIVAC III, or a remote UNIVAC 418. Two types of inter-computer synchronizers are available: single-channel and dual-channel. The couplers for the UNIVAC III or a remote UNIVAC 418 use a single channel to provide an 18-bit interface with the UNIVAC 418. A dual-channel, 36-bit interface coupler is required for use with a UNIVAC 1107/1108 or 490.

Maximum data transfer rates are determined by the internal speed of the slower of the two connected computers. Each computer treats the other as an input-output device. Automatic storage protection is not provided; protection is available only through software routines.

Data sent to a UNIVAC III from a 418 must be edited before transmission. Only the lower 12 bits of each 18-bit word can contain data. The upper 6 bits must be blank.

INPUT–OUTPUT: TRANSFER SWITCHING UNIT

.1 GENERAL

.11 Identity: . . . . . Transfer Switching Unit.

.12 Description

The Transfer Switching Unit permits two peripheral subsystems to share the same UNIVAC 418 input-output channel or channels. Since many 418 subsystems require two input-output channels, the 16 possible channels may be insufficient to accommodate all of the desired peripheral equipment. The Transfer Switching Unit can alleviate this restriction. Two types of units are available: single-channel and dual-channel. Switching between two subsystems is done manually. The Transfer Switching Unit also permits a peripheral subsystem to be switched between two UNIVAC 418 Central Processors, or between a 418 and a UNIVAC 490, 1107, or 1108.

SIMULTANEOUS OPERATIONS

.1 GENERAL

.11 Channel Requirements

The UNIVAC 418 Central Processor can contain 8, 12, or 16 input-output channels. Any peripheral subsystem can be connected to any input-output channel, with the exception of the Programmer's Console, which includes a keyboard-printer. If the Programmer's Console is used, it must be connected to channel 0. Two types of input-output transfers are performed in the UNIVAC 418. One type uses one input-output channel to transfer data in units of 18 bits; the second uses two input-output channels to transfer data in units of 36 bits.

The following subsystems require two input-output channels and transfer data in units of 36 bits:

- FH-880 Magnetic Drum Subsystem: 1 to 8 drums (see Section 790:044).
- Fastrand I and II Mass Storage Subsystems: 1 to 8 storage units (see Section 790:045).
- Uniservo IIA Magnetic Tape Subsystem: 2 to 12 tape units (see Section 790:091).
- Uniservo IIIA Magnetic Tape Subsystem: 2 to 16 tape units (see Section 790:092).
- High-Speed Printer Subsystem: 1 printer (see Section 790:081).

The following subsystems require one input-output channel and transfer data in units of 18 bits:

- FH-220 Magnetic Drum Subsystem: 1 drum (see Section 790:042).
- FH-330 Magnetic Drum Subsystem: 1 to 5 drums (see Section 790:043).
- Uniservo IIIC and IVC Magnetic Tape Subsystem: 2 to 12 tape units (see Section 790:093). As an optional feature, two channels can be used to transfer data in units of 36 bits.
- Uniservo VIC Magnetic Tape Subsystem: 2 to 16 tape units (see Section 790:094).
- UNIVAC 1004 Central Processor (see Section 790:071).
- Programmer's Console Keyboard-Printer (see Section 790:061).
- Paper Tape Subsystem: 1 reader and 1 punch (see Section 790:072). This subsystem uses the same channel as the Programmer's Console.

An unusual case is the Standard Communications Subsystem (SCS). This subsystem requires two channels, but only one channel is used to transfer data. The second channel transmits Externally Specified Index (ESI) characters. Central processor delay times for the SCS are the same as for devices using the 18-bit data transfer mode.

.12 Control and Synchronizer Units

The Control and Synchronizer Unit for each subsystem provides the proper interface between the central processor and the peripheral units on the input-output channel or channels. During most output operations, the synchronizer accepts one or two 18-bit words at a time from the computer and divides them into 6-bit character elements. During most input operations, the Synchronizer assembles 6-bit characters from the input device into one or two 18-bit UNIVAC 418 words at a time. The peripheral control unit, which is usually in the same cabinet as the synchronizer, directs the selected input or output device while it performs the desired function.

.13 The Input-Output Process

In general, one data transfer operation at a time can occur in each peripheral subsystem. The exceptions to this general statement are:

- An optional Dual Channel Synchronizer can be used with the Uniservo IIIC, IVC, or VIC Magnetic Tape Subsystem. In this case, the subsystem occupies two input-output channels and can simultaneously control either one read and one write operation or two read operations (but not two write operations).
- A magnetic tape or drum Control and Synchronizer Unit (and therefore the channel to which it is connected) is occupied throughout a search operation, even though no data is transferred to the central processor until the search has been successfully completed.
- When the Standard Communications Subsystem is used, the channels to which it is connected can be effectively divided into several channels of lower speed, each with its own core buffer area and interrupt control. Each Communication Line Terminal presents the address of its own particular buffer area to the central processor, permitting messages to or from several different communication lines to be transmitted concurrently under control of the Communication Multiplexer.
- Although only one data transfer operation at a time can occur between the 418 and the UNIVAC 1004 Processor, full use of the

.13 The Input-Output Process (Contd.)

simultaneity of the 1004 peripherals can be achieved through plugboard programming of the 1004 and use of its 961 characters of core storage as buffer areas for the data being read, printed, and/or punched.

Two Buffer Control Words, in fixed core storage locations, are associated with each input and each output channel. Before an input or output operation is initiated, a "Load External Function" instruction is used to inform the synchronizer of the function to be performed and provide any other necessary data. The "Data In" or "Data Out" instructions load the appropriate Buffer Control Words with the core storage addresses of the first and last words to be transferred and initiate the transfer operation. After each data word (or pair of data words in the case of the 36-bit interface) has been transferred to or from core storage, the initial address in one Buffer Control Word is automatically incremented by 1 (or 2) and compared with the terminal address in the other Buffer Control Word. The updated initial address is replaced in storage. If the comparison indicates that the data transmission has been completed, the operation is terminated and (optionally) an interrupt is initiated.

.2 DEMANDS ON THE PROCESSOR

Each data word transferred to or from core storage in the 18-bit interface mode requires 4 cycles of central processor time. This takes 8 microseconds in the Model II Processor and 16 microseconds in the Model I Processor. Each pair of words transferred in the 36-bit interface mode requires 5 cycles of central processor time; this is equivalent to 10 microseconds in the Model II Processor and 20 microseconds in Model I. (In the case of the Programmer's Console, the Paper Tape Subsystem, and the Standard Communications Subsystem, one full word is used to hold each data character.)

The maximum gross data transfer rate (or "saturation rate") for the UNIVAC 418-I system is 62,500 words (or 187,500 characters) per second in the 18-bit interface mode and 100,000 words (or 300,000 characters) per second in the 36-bit interface mode. The maximum gross data rate for the UNIVAC 418-II system is 125,000 words (or 375,000 characters) per second in the 18-bit interface mode and 200,000 words (or 600,000 characters) per second in the 36-bit interface mode. At these rates, no central processor time would be available for executing stored program instructions.

The consequences of attempting to exceed the maximum data transfer rate quoted above depend upon the particular peripheral subsystems involved and the priorities of the channels to which they are connected. (When there are simultaneous demands for access to core storage, the highest-numbered channel is served first.) The magnetic drum subsystems will attempt another data transfer during the next drum revolution, with no loss of data. The magnetic tape subsystems will generate a recoverable error condition, necessitating that the input or output operation be repeated. The probability of exceeding the maximum data transfer rate can be reduced by choosing one of the interlace options available for the Fastrand, FH-330, and FH-880 Magnetic Drums, which reduce their effective transfer rates.

.3 SIMULTANEITY RULES

A UNIVAC 418 system can simultaneously perform:

- One input, output, or search operation per Fastrand, FH-220, FH-330, or FH-880 Magnetic Drum Subsystem; and
- One positioning operation per Fastrand Storage Unit; and
- One input, output, or search operation per Magnetic Tape Subsystem with Single-Channel Synchronizer; and
- One input and one output (or two input) operations per Uniservo IIIC, IVC, or VIC Magnetic Tape Subsystem with Dual-Channel Synchronizer; and
- Any number of magnetic tape rewind operations; and
- One input or output transfer per UNIVAC 1004 Subsystem; and
- One input or output operation per Paper Tape Subsystem or one Programmer's Console input or output operation; and
- One output operation per Printer Subsystem; and
- One input or output operation per Communication Line Terminal; and
- Internal processing in the Central Processor.

The gross data transfer rate between core storage and all simultaneously operating peripheral devices cannot exceed the following values:

	Words per second	Characters per second
Model I Processor -		
18-bit interface:	62,500	187,500
36-bit interface:	100,000	300,000
Model II Processor -		
18-bit interface:	125,000	375,000
36-bit interface:	200,000	600,000

INSTRUCTION LIST

MNEMONICS		FUNCTION CODE OCTAL	μS	OPERATION	DESCRIPTION
ART	TRIM				
CL	CMAL	02	4	(AL) : (Y)	COMPARE AL
MSL	SLSU	04	4	$(Y_N) \rightarrow AL_N$ FOR $AU_N = 1$	SELECTIVE SUBSTITUTE
CLM	CMSK	06	4	L(AU) (AL) : L(AU) (Y)	COMPARE AL WITH MASK
LU	ENTAU	10	4	(Y)→ AU	LOAD AU
LL	ENTAL	12	4	(Y)→ AL	LOAD AL
AL	ADDAL	14	4	(AL) + (Y)→ AL	ADD AL
ANL	SUBAL	16	4	(AL) – (Y)→ AL	SUBTRACT FROM AL
AA	ADDA	20	6	(AU, AL) + (Y – 1, Y)→ A;Y ODD	ADD A
ANA	SUBA	22	6	(AU, AL) – (Y – 1, Y)→ A;Y ODD	SUBTRACT FROM A
M	MULAL	24	13.33–24.67	(AL) (Y)→ A	MULTIPLY AL
D	DIVA	26	24	(A) ÷ (Y)→ AL, REM→ AU	DIVIDE A
SLJI	IRJP	30*	6	P + 1→ (Y); (Y) + 1→ P	STORE LOCATION JUMP INDIRECT
LB	ENTB	32	6	(Y)→ B	LOAD B
J	JP	34*	2	Y→ P	JUMP
LBK	ENTBK	36*	4	Y→ B	LOAD B WITH CONSTANT
CY	CL	40	4	ZERO→ Y	CLEAR Y
SB	STRB	42	6	(B)→ Y	STORE B
SL	STRAL	44	4	(AL)→ Y	STORE AL
SU	STRAU	46	4	(AU)→ Y	STORE AU
* ALL ABOVE INSTRUCTIONS EXCEPT THESE ARE SR SENSITIVE. ALL ABOVE INSTRUCTIONS ARE B - MODIFIABLE (SUFFIX A "B" TO TRIM CODE PREFIX AN * TO AN ART OPERAND, OR ADD A "1" TO OCTAL)					
OR	SLSET	51	4	SET AL_N=1 FOR $(Y_N = 1)$	SELECTIVE SET
AND	SLCL	52	4	SET AL_N=0 FOR $(Y_N = 0)$	SELECTIVE CLEAR
XOR	SLCP	53	4	COMPLEMENT AL_N FOR $(Y_N) = 1$	SELECTIVE COMPLEMENT
EJI	IJPEI	54	4	(Y)→ P; ENABLE INTERRUPTS	ENABLE INTERRUPTS AND JUMP INDIRECT
JI	IJP	55	4	(Y)→ P	JUMP INDIRECT
TB	BSK	56	8	(B) = (Y), (P) + 2→ P (B) ≠ (Y), (B) + 1→ B, (P) + 1→ P	TEST B
TZ	ISK	57	6	(Y) = 0;(P) + 2→ P (Y) ≠ 0;(Y) – 1→ Y, (P) + 1→ P	TEST ZERO
LLK	ENTALK	70	2.33	Y→ AL	LOAD AL CONSTANT
ALK	ADDALK	71	2.33	(AL) + Y→ AL	ADD AL CONSTANT
SIR	STRICR	72	3	(ICR)→ $(Y)_{2\rightarrow \emptyset}$	STORE INDEX CONTROL REGISTER
JBNZ	BJP	73	6	(B) ≠ 0, (B) – 1→ B; Y→ P (B) = Ø, (P) + 1→ P	JUMP B
SAD	STRADR	74	4	$(AL)_{11\rightarrow 0} \rightarrow Y_{11\rightarrow 0}$	STORE ADDRESS
SSR	STRSR	75	4	$(SR) \rightarrow (Y)_{4\rightarrow 0}$ AND ZERO→ SR_4	STORE SEPCIAL REGISTER
SLJ	RJP	76	4	(P) + 1→ Y ; Y + 1→ P	STORE LOCATION, JUMP
JUMP INSTRUCTIONS – COMPARE DESIGNATOR NOT SET					
JUZ	JPAUZ	60	2	JUMP IF (AU) = 0	JUMP AU ZERO
JLZ	JPALZ	61	2	JUMP IF (AL) = 0	JUMP AL ZERO
JUNZ	JPAUNZ	62	2	JUMP IF (AU) ≠ 0	JUMP AU NOT ZERO
JLNZ	JPALNZ	63	2	JUMP IF (AL) ≠ 0	JUMP AL NOT ZERO
JUP	JPAUP	64	2	JUMP IF (AU) IS POSITIVE	JUMP AU POSITIVE
JLP	JPALP	65	2	JUMP IF (AL) IS POSITIVE	JUMP AL POSITIVE
JUN	JPAUNG	66	2	JUMP IF (AU) IS NEGATIVE	JUMP AU NEGATIVE
JLN	JPALNG	67	2	JUMP IF (AL) IS NEGATIVE	JUMP AL NEGATIVE

(Contd.)

JUMP INSTRUCTIONS – COMPARE DESIGNATOR SET

MNEMONICS		FUNCTION CODE			
ART	TRIM	OCTAL	μS	OPERATION	DESCRIPTION
JE	JPEQ	60 & 61	2	JUMP IF (AL) = (Y)	JUMP EQUAL
JNE	JPNOT	62 & 63	2	JUMP IF (AL) ≠ (Y)	JUMP NOT EQUAL
JNLS	JPMLEQ	64 & 65	2	JUMP IF (AL) < (Y), OR (Y) ≥ (AL)	JUMP AL GREATER
JLS	JPMGR	66 & 67	2	JUMP IF (AL) < (Y), OR (Y) > (AL)	JUMP AL LESS OR EQUAL
LIC	IN	50 11*	10	LOAD INPUT CHANNEL K	INPUT TRANSFER
LOC	OUT	50 12*	10	LOAD OUTPUT CHANNEL K	OUTPUT TRANSFER
LFC	EXF	50 13*	10	LOAD FUNCTION CHANNEL K	EXTERNAL FUNCTION
STIC	INSTP	50 15*	2	STOP INPUT ON CHANNEL K	TERMINATE INPUT
STOC	OUTSTP	50 16*	2	STOP OUTPUT ON CHANNEL K	TERMINATE OUTPUT
TIC	SKPIIN	50 21*	2.3	TEST INPUT CHANNEL K (IDLE, (P) + 2→ P)	SKIP IF INPUT CHANNEL INACTIVE
TOC	SKPOIN	50 22*	2.3	TEST OUTPUT CHANNEL K (IDLE, (P) + 2→ P)	SKIP IF OUTPUT CHANNEL INACTIVE
TFC	SKPFIN	50 23*	2.3	TEST FUNCTION CHANNEL K (YES, (P) + 2→ P)	SKIP IF FUNCTION MODE INACTIVE
OV	OUTOV	50 26*	10-12	OVERRIDE K, IF BCWT ≠ BCWI	OUTPUT OVERRIDE
AAI	RIL	50 30 &	2	ALLOW ALL INTERRUPT	REMOVE INTERRUPT LOCKOUT
		50 31	2		
AFI	RXL	50 32 &	2	ALLOW FUNCTION INTERRUPT	REMOVE EXTERNAL INTERRUPT LOCKOUT
		50 33	2		
PAI	SIL	50 34 &	2	PREVENT ALL INTERRUPT	SET INTERRUPT LOCKOUT
		50 35	2		
PFI	SXL	50 36 &	2	PREVENT FUNCTION INTERRUPT	SET EXTERNAL INTERRUPT LOCKOUT
		50 37	2		
SRU	RSHAU	50 41	2.67 + K/3	SHIFT RIGHT U } END OFF	SHIFT RIGHT AU
SRL	RSHAL	50 42	2.67 + K/3	SHIFT RIGHT L } END OFF	SHIFT RIGHT AL
SRA	RSHA	50 43	2.67 + K/3	SHIFT RIGHT A } END OFF	SHIFT RIGHT A
SCA	SF	50 44	3.17 + K/3	SCALE A; SF→ 17	SCALE A
SLU	LSHAU	50 45	2.67 + K/3	SHIFT LEFT U } END AROUND	SHIFT LEFT AU
SLL	LSHAL	50 46	2.67 + K/3	SHIFT LEFT L } END AROUND	SHIFT LEFT AL
SLA	LSHA	50 47	2.67 + K/3	SHIFT LEFT A } END AROUND	SHIFT LEFT A
TK	SKP	50 50	2.33 - 3	TEST KEY	SKIP ON KEY SETTINGS
* ABOVE INSTRUCTIONS ARE NOT FOLLOWED BY AN I/O SCAN.					
TNB	SKPNBO	50 51	2.3-3	(P) + 2→ P IF NO BORROW NEEDED & RESET	SKIP ON NO BORROW
TOF	SKPOV	50 52	2.3-3	(P) + 2→ P IF OVERFLOW OCCURRED & RESET	SKIP ON OVERFLOW
TNO	SKPNOV	50 53	2.3-3	(P) + 2→ P IF NO OVERFLOW OCCURRED	SKIP ON NO OVERFLOW
TOP	SKPODD	50 54	2.3-3	(P) + 2→ P IF ODD PARITY IN AL, MASKED BY AU	SKIP ON ODD PARITY
TEP	SKPEVN	50 55	2.3-3	(P) + 2→ P IF EVEN PARITY IN AL, MASKED BY AU	SKIP ON EVEN PARITY
SK	STOP	50 56	2.3	STOP IF KEY SET	STOP ON KEY SETTINGS
RND	RND	50 60	2.7	$(AL_{17}) \div 2^{17} + (AU) \rightarrow AL$	ROUND AU
CPL	CPAL	50 61	2.7	~ AL→ AL	COMPLEMENT AL
CPU	CPAU	50 62	2.7	~ AU→ AU	COMPLEMENT AU
CPA	CPA	50 63	2.7	~ A→ A	COMPLEMENT A
LIR	ENTICR	50 72	2	$Y_{2} \rightarrow 0 \rightarrow$ ICR	LOAD INDEX CONTROL REGISTER
LSR	ENTSR	50 73	2	$Y_{4} \rightarrow 0 \rightarrow$ SR	LOAD SPECIAL REGISTER

Y = OPERAND AS CONSTANT
( ) = CONTENTS OF REGISTER OR ADDRESS
FF = FUNCTION CODE OR OP CODE
K = BITS 5 - 0 OF INSTRUCTION
~ = OPPOSITE OF (EVERY 0→ 1, AND EVERY 1→ 0)
ICR = INDEX CONTROL REGISTER
ADD 2 μSEC TO TIME FOR INDEXING

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DATA CODE TABLE

80-Col. Card Code	Printable Characters	XS-3 Code	80-Col. Card Code	Printable Characters	XS-3 Code
12–1	A	01 0100	7	7	00 1010
12–2	B	01 0101	8	8	00 1011
12–3	C	01 0110	9	9	00 1100
12–4	D	01 0111	12	&	01 0000
12–5	E	01 1000	11	- (minus)	00 0010
12–6	F	01 1001	12–0	?	01 0011
12–7	G	01 1010	11–0	!(exclam.)	10 0011
12–8	H	01 1011	0–1	/	11 0100
12–9	I	01 1100	2–8	+	11 0011
11–1	J	10 0100	3–8	#	01 1101
11–2	K	10 0101	4–8	@	10 1110
11–3	L	10 0110	5–8	: (colon)	01 0001
11–4	M	10 0111	6–8	>	11 1110
11–5	N	10 1000	7–8	' (apos.)	10 0000
11–6	O	10 1001	12–3–8	. (period)	01 0010
11–7	P	10 1010	12–4–8	⌑	11 1101
11–8	Q	10 1011	12–5–8	[	00 1111
11–9	R	10 1100	12–6–8	<	01 1110
0–2	S	11 0101	12–7–8	=	01 1111
0–3	T	11 0110	11–3–8	$	10 0010
0–4	U	11 0111	11–4–8	*	10 0001
0–5	V	11 1000	11–5–8	]	00 0001
0–6	W	11 1001	11–6–8	;(semi-col)	00 1110
0–7	X	11 1010	11–7–8	Δ	10 1111
0–8	Y	11 1011	0–2–8	≠	11 0000
0–9	Z	11 1100	0–3–8	, (comma)	11 0010
0	0	00 0011	0–4–8	%	11 0001
1	1	00 0100	0–5–8	(	10 1101
2	2	00 0101	0–6–8	\	00 1101
3	3	00 0110	0–7–8	)	11 1111
4	4	00 0111			
5	5	00 1000	Blank	Space N.P.	00 0000
6	6	00 1001			

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PROBLEM ORIENTED FACILITIES

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . none.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

Sort/Merge

Record size: . . . . . 1,200 characters (maximum).
Block size: . . . . . 1,200 characters (maximum).
Key size: . . . . . 36 characters (up to 12 non-contiguous, non-sequential fields).
File size: . . . . . 1 output reel.
Number of tape units: . 3 to 12 (Fastrand can be used for I/O and/or external sort).
Date available:. . . . . January, 1965.
Description:

Sort/Merge is a character-oriented, object-time generator that uses a replacement-selection tournament technique for sorting and a polyphase merge. Parameters can be read on-line from the 1004 Card Reader. The user's own coding can be inserted into the first and last passes. Sort/Merge uses Uniservo IIIC or IIA Tape Handlers. A Fastrand option is available which uses a Fastrand Mass Storage Unit for external sorting, with input-output for either Fastrand or magnetic tape.

Sort/Merge requires a 12K UNIVAC 418 and runs under EXEC control. Additional core storage can be allotted when available. Six-way code translation and sequence definition are provided.

.14 Report Writing: . . . . . none.

.15 Data Transcription

418 Utility Routines

Date available:. . . . . now in use.
Description:

The following data transcription routines are currently provided:

- Uniservo IIIC Magnetic Tape to 1004 Printer — includes label check, variable-length record handling, error conditions, code conversion, tape convention checking, and paper spacing.
- Uniservo IIIC Magnetic Tape to 1004 Card Punch — includes same features as above.
- 1004 Card Reader to Uniservo IIIC Magnetic Tape — allows choice of density, block size, and file length and provides for automatic restart at a predetermined point.
- General Tape-Drum Print — prints programs or data from Uniservo IIIC Tape Handler or FH-330 Drum without special format.

Data transcription routines for all peripheral devices used by the UNIVAC 418 will, according to the manufacturer, be made available upon request by the user.

.16 File Maintenance

Tape File Maintenance (Uniservo IIIC)

Date available:. . . . . now in use.
Description:

This program provides for updating and correcting of a master file, and is run under EXEC control. Input control cards specify the options to be performed: correction of all or a portion of a file, copying of a file or portions of it onto another tape or a printer, comparison of segments of a master file with another tape, or merely positioning of a tape to a given segment. Depending on the option desired, the requirements are 1 to 3 magnetic tape units, 1004 Card Reader, console typewriter, 1004 Printer, and approximately 2,600 core storage locations.

Core and Drum Change Program (FH-330 Magnetic Drum)

Date available:. . . . . now in use.
Description:

Two versions of this program for inspecting and altering the contents of core or drum storage exist. One uses the 1004 card reader for input data; the other uses the console keyboard. Both programs operate under control of EXEC. Entries can be made in five formats: octal, Baudot, XS-3, Fieldata, or ASCII. The program automatically translates these into the codes of the card reader or console.

.17 Other

Reloadable Core and Drum Dump

Date available: . . . . . January, 1965.
Description:

This routine allows the user to dump the contents of any part of core storage or any number of tracks of an FH-330 Drum Unit onto a Uniservo IIIC tape, so that it can be retrieved by means of a wired (non-destructible) bootstrap card program.

Trace

Date available:. . . . . January, 1965.
Description:

This routine is a selective trace that prints a record of a program's progress on the 1004 Printer. Trace is compatible with the EXEC operating system. It is relocatable at load time and occupies less than 700 word locations.

PROCESS ORIENTED LANGUAGES: FORTRAN IV

.1 GENERAL

.11 Identity: . . . . . UNIVAC 418 FORTRAN IV.

.14 Description

FORTRAN IV for the UNIVAC 418 is a subset of IBM 7090/7094 FORTRAN IV. Compilation requires a 418 central processor with at least 12,288 words of core storage, an input-output keyboard and console printer, a UNIVAC 1004 card processor with printer, a card reader, and a card punch. Storage requirements for the execution of object programs will depend upon the particular program's size and data storage requirements. Object program input can be from cards, magnetic tape, and/or drum; output can be to magnetic tape, console printer, high-speed printer, cards, and/or drum. UNIVAC 418 FORTRAN IV utilizes the EXEC operating system for all input-output functions.

The UNIVAC 418 FORTRAN compiler permits the use of most of the facilities available in IBM 7090/7094 FORTRAN IV. Integer, real, and a form of double-precision constants and variables can be used, but provisions for complex and logical constants and variables have not been made. All the open and library functions offered in IBM 7090/7094 FORTRAN are included in the 418 version except those with double-precision or complex arguments. The logical operators .NOT., .AND., and .OR. are not permitted. The expressions allowed as subscripts in 418 FORTRAN IV are different from those permitted in IBM 7090/7094 FORTRAN IV. Unlike FORTRAN IV for the UNIVAC III, 418 FORTRAN IV offers no compatibility with the FORTRAN II language.

.141 Availability

Language specifications: . . . . February, 1965 (preliminary).
Compiler: . . . . . ?

.142 Restrictions Relative to IBM 7090/7094 FORTRAN IV

(1) Integer constants can be 1 to 6 digits in length, as compared to a maximum of 11 digits for 7090/7094 FORTRAN IV; double-precision constants can be up to 11 digits in length, as compared to a maximum of 17 digits for 7090/7094 FORTRAN IV. However, the size of the exponent for double-precision items in the 418 is 15 bits, as compared to 8 bits for 7090/7094 FORTRAN IV.

(2) Complex and logical constants are not permitted.

(3) The following statements are not provided:
BLOCK DATA
DATA
END FILE
EXTERNAL
PRINT
PUNCH
READ n

(4) The expressions allowed as subscripts vary from those for 7090/7094 FORTRAN IV. The following are not permitted:
V+C
V-C

(5) The logical operation symbols .NOT., .AND., and .OR. are not included.

(6) In FORMAT statements, D-specification is not permitted.

(7) No double-precision or complex functions are provided.

.143 Extensions Relative to IBM 7090/7094 FORTRAN IV

(1) The following expression types are allowed as subscripts:
V*C
V*V'±C

(2) The symbol "+" can be used for carriage control to suppress spacing before printing.

(3) The library function ASIN (arcsin) is provided.

(4) The exponent in double-precision numbers can be up to 15 bits in 418 FORTRAN IV as compared to 8 bits in 7090/7094 FORTRAN IV.

MACHINE ORIENTED LANGUAGES: ART

.1 GENERAL

.11 Identity: . . . . . ART (Assembler for Real Time).

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corp.

.14 Description

ART is a symbolic assembly system that permits utilization of all the hardware facilities of the UNIVAC 418, provides facilities for the definition and use of macro-instructions, and produces object programs that can be run in a multiprogrammed mode under the control of the EXEC operating system. The ART translator is described in detail in the following report section (page 790:181.100).

The ART coding sheet is free-form and provides space for labels, operation codes, operands, and comments. The operation codes can be in mnemonic form. The operand field consists of one or more expressions, as required by the operation code, and can be used to indicate whether indexing is to be performed. Expressions can contain a series of labels, the location counter address, octal values, alphabetics, decimal values, parameter reference forms, and/or lines of coding, connected by a large assortment of operators. Constants and literals are limited to 18 bits in size. Programmer notes are permitted.

A macro-instruction is a symbolic command which accesses an entire group of instructions. No standard macro-instructions are supplied with ART, but a powerful PROC (procedure) facility enables the user to generate his own macros. A PROC Assembler directive informs the assembler that all succeeding symbolic lines, until a corresponding END directive is reached, are not to be assembled, but retained by the assembler until they are referenced by some other portion of the symbolic program. When the PROC is referenced (or "CALLed") by one of its names, the symbolic coding associated with the PROC will then be assembled, substituting the parameters in the calling line to create object code that is custom-fitted to the current requirements. It is possible to execute a PROC at assembly time, rather than at object time. PROC's can be stored in the ART Library System and copied during the first pass of the assembler.

Input-output operation codes in the ART language are usually "privileged" (reserved for use only by the executive routine). When an input-output function is desired, the program must reference a "CALL" packet which contains the channel and function desired, an immediate return address or an address to be returned to after completion, an error address, and the Buffer Control Words. Contents of the packet can vary for the particular device and function used. The first word of the packet contains an illegal operation code. When executed, this will result in a "fault" interrupt and automatic transfer to location 00000. This location contains a "store and jump" instruction which saves the contents of the sequence counter and transfers control to EXEC. The appropriate EXEC Input-Output Handler routine is utilized to initiate and control the input or output operation.

The basic ART Assembly program requires two passes and 8,192 words of core storage. A printer is required for the program listing, and a card reader or magnetic tape for control input. The program to be assembled can be on punched cards, paper tape, magnetic tape or drum. Assembly can be accomplished in one pass if magnetic tape or a drum is available for intermediate storage. If 4,096 words of additional core storage are present, assembly can proceed under control of EXEC.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . see coding sheet, Figure 1.

.22 Legend

Label: . . . . . identifies either a symbolic line of coding or an item of data.

Operation: . . . . . contains a mnemonic machine operation code, an assembler directive, a label associated with a PROC code, or a data generating code.

Operand: . . . . . one or more expressions defining the information required by the operation field.

Comments: . . . . . if line is not to be continued, any comments for the reader can be inserted after a period.

.23 Corrections

.231 Insertions: . . . . . a line of coding is written with an operation code of INS and operand of LINE NO.

.232 Deletions: . . . . . a line of coding is written with an operation code of COR and operand of LINE NO.

.233 Alterations: . . . . . same as deletions.

UNIVAC® 418 | ASSEMBLY IN ART

PROGRAM _____ PROGRAMMER _____ DATE _____ PAGE____ OF____ PAGES

KEYPUNCH: USE UNIVAC III PUNCH COMBINATION FOR SPECIAL CHARACTERS UNLESS ALTERNATE NOTED HERE ☐

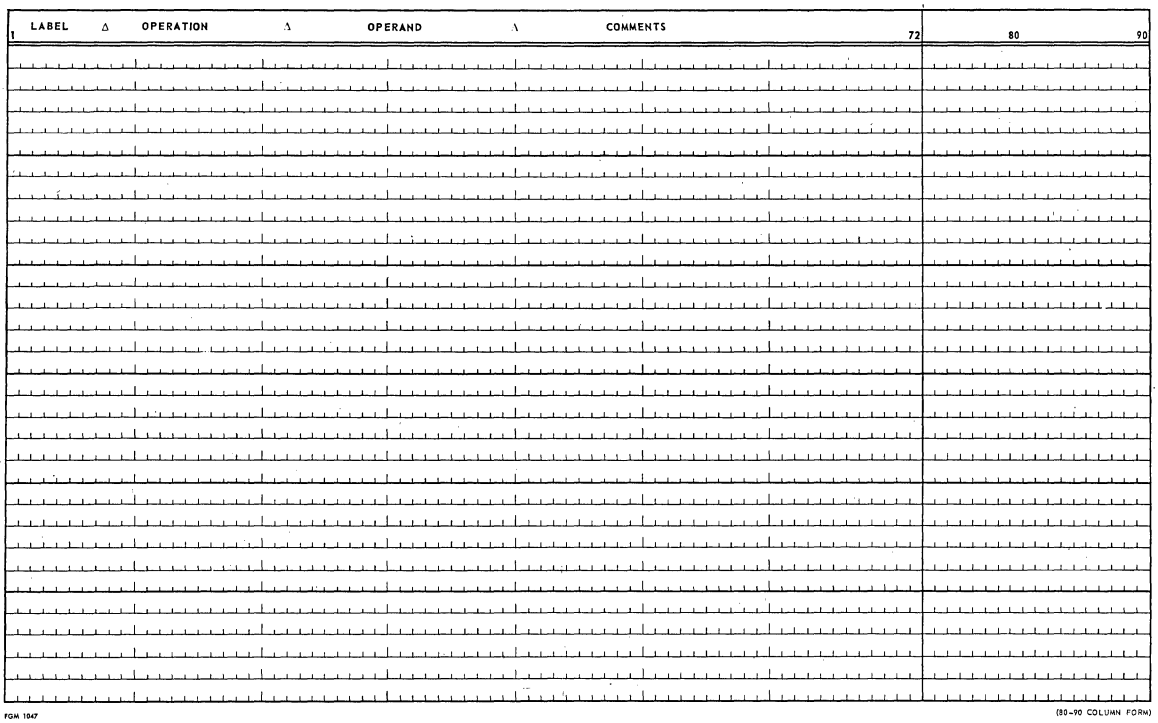


FIGURE 1: ART CODING SHEET

.24 Special Conventions

.241 Compound addresses: . a series of elementary items connected by operators: (+, -, *, /, Logical ++, --, **, Covered Quotient //, =, >, <).

.242 Multi-addresses: . . . . none.

.243 Literals: . . . . . • octal value preceded by zero.
• alphabetic characters enclosed in quotes.
• paraform enclosed in parentheses.
• line of coding enclosed in parentheses.

.244 Special coded addresses: . . . . . $ refers to current value of the location counter.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . . no practical limit (in 8K version, upper limit is approximately 900 labels).

.312 Common label formation rule: . . . . . yes.

.313 Reserved labels: . . . . none.

.314 Other restrictions: . . . none.

.315 Designators: . . . . . none.

.316 Synonyms permitted: . . yes; EQU pseudo.

.32 Universal Labels

.321 Labels for procedures —
Existence: . . . . . mandatory if referenced by another program segment.
Formation rule —
First character: . . alphabetic.
Last character: . . asterisk (*).
Others: . . . . . alphabetic or numeric; no special characters or spaces.
Number of characters: . . . . . 1 to 6 plus asterisk.

.322 Labels for library routines: . . . . . three types of labels exist, depending on the library subdivision. Labels for books are the same as for local labels. Labels for chapters are the same as for universal labels. Sentences are referenced by line number.

.323 Labels for constants: . same as procedures.

.324 Labels for files: . . . . . same as procedures. (Label for the ART library tape is its entire label block.)

(Contd.)

.325 Labels for records: . . same as procedures.
.326 Labels for variables: . same as procedures.

.33 Local Labels

.331 Region: . . . . . local to a program segment.
.332 Labels for procedures —
Existence:. . . . . mandatory if referenced by another instruction.
Formation rule —
First character:. . . alphabetic.
Others:. . . . . alphabetic or numeric; no special characters or blanks.
Number of characters:. . . . . 1 to 6 (no asterisk).
.333 Labels for library routines:. . . . . see Paragraph .322.
.334 Labels for constants: . same as procedures.
.335 Labels for files:. . . . . same as procedures.
.336 Labels for records: . . same as procedures.
.337 Labels for variables: . same as procedures.

.4 DATA

.41 Constants

.411 Maximum size constants —
Integer
Decimal:. . . . . equivalent of 18 bits.
Octal:. . . . . 6 octal digits.
Fixed numeric: . . . . no provision.
Floating numeric:. . . no provision.
Alphabetic: . . . . . 3 characters.
Alphameric: . . . . . 3 characters.
.412 Maximum size literals: same as constants.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence:. . . . . optional.
Number:. . . . . 78.
Example: . . . . . LL = Load Lower Accumulator.
Comment:. . . . . operand preceded by an asterisk indicates indexing.

.52 Macro-Codes: . . . . . PROC facility enables user to construct a macro system.
.523 New Macros:. . . . . coded with program, using PROC pseudo; can be inserted in library during same run.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter:. . pseudo-operation.
Label adjustment:. . . pseudo-operation.
Annotation: . . . . . comments portion of line of coding.
.542 Allocation counter —
Set to absolute: . . . . parameter in Executive Preamble.
Set to label:. . . . . RES.
Step forward:. . . . . RES, ODD, EVEN, SETADR.
Step backward:. . . . . RES.
Reserve area: . . . . . RES.
.543 Label adjustment —
Set labels equal:. . . . EQU pseudo.
Set absolute value: . . EQU pseudo.
Clear label table:. . . CLT, PLT, or PPLT pseudo (clears all but universal labels).
.544 Annotation —
Comment phrase:. . . comments portion at end of line of coding.
Title phrase: . . . . . ASM pseudo.
.545 Other —
SETADR: . . . . . dumps and clears literal table, and advances sequence counter.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic:. . . floating-point routines will be provided with FORTRAN compiler. (Note: fixed-point computations in ART are performed throughout in double precision (36 bits) format, with results truncated to 18 bits.)

.62 Special Functions: . . . standard math functions will be provided with FORTRAN compiler.

.63 Overlay Control: . . . . provided by EXEC routines.

.64 Data Editing

.641 Radix conversion:. . . . octal or decimal to binary.
.642 Code translation: . . . . CHAR pseudo - operation can provide translation between any two codes.
.643 Format control:. . . . . no provisions.

.65 Input-Output Control

.651 File labels:. . . . . EXEC routines.
.652 Reel labels:. . . . . EXEC routines.
.653 Blocking: . . . . . EXEC routines.
.654 Error control:. . . . . EXEC routines.
.655 Method of call:. . . . . see Section 790:191.

.66 Sorting: . . . . . see Sort/Merge, Paragraph 790:151.13.

.67 Diagnostics

.671 Dumps:. . . . . EXEC Snapdump or utility routines.
.672 Tracers:. . . . . Trace utility routine.
.673 Snapshots:. . . . . EXEC Snapdump routine.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . ART Library System.

.72 Kinds of Libraries: . . expandable master.

.73 Storage Form: . . . . . card, paper tape, magnetic tape, or drum.

.74 Varieties of Contents:. programs, macros (PROC's), and subroutines.

.75 Mechanism

.751 Insertion of new item:. part of first pass of assembler.
.752 Language of new item:. relocatable or symbolic code.
.753 Method of call:. . . . . external directives (commands preceded by an asterisk), usually from 1004 Card Reader.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist:. yes.
.763 Open-closed is optional: . . . . . no.
.764 Closed routines appear only once:. . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . . no specific macros are provided; user can create his own system using PROC pseudo-instruction and library facilities.

.82 Pseudos

Code	Description
Definitive —	
ASM:	identifies an assembly and provides data to generate an Executive preamble.
EQU:	equates a symbol with an expression.
FORM:	defines arbitrary word formats, labels these formats, and thereafter references each format by using the associated format label as an operation code in the operation field.
END:	indicates end of a program or procedure.
CHAR:	permits redefinition of the octal equivalents of alphabetic data.
CLT:	performs segment END functions and clears label table of all but external labels.
PLT:	same as CLT except that external labels are printed.
PPLT:	same as PLT; in addition, the external labels are punched.
Incremental —	
RES:	causes the value of the expression in the operand field to be added to the location counter.
SETADR:	causes all literals referred to previously to be dumped, removed from the literal table, and the location counter advanced to the value of an expression.
ODD:	sets location counter so that subsequent data will be assigned to an odd address.
EVEN:	same as ODD, but for EVEN addresses.
Repetitive —	
DO:	conditionally generates a line of coding a variable number of times.
Procedural —	
PROC:	precedes the coding of a procedure with variable parameters.
NAME:	qualifies a PROC procedure; designates entry points in a PROC.
GO:	transfers to a label specified in the operand field (used only in a PROC).

PROGRAM TRANSLATORS: ART

.1 GENERAL

.11 Identity: . . . . . ART Assembly System.

.12 Description

Operation of the ART translator requires at least 8,192 core storage locations, a card reader or magnetic tape unit for control input, a printer, an input device, and a punch, magnetic tape, or paper tape punch for loadable output. If an additional 4,096 words of core storage are available, the assembly can be run under control of the EXEC Executive System. ART is basically a two-pass assembler, but assembly can be accomplished on one pass if a drum or additional magnetic tape units are available.

Input may be from punched cards, magnetic tape, paper tape, or drum, and output of the object program may be on any of these media. Two versions of ART are available. One is designed to be run on the UNIVAC 418, and the other — ART III — on the UNIVAC III. Only the UNIVAC 418 version is described here.

The EXEC Executive System (page 790:191.100) effectively eliminates the need for detailed programming of standardized input and output functions. The programmer must use a CALL sequence and provide a packet of information for use by EXEC.

.13 Originator: . . . . . UNIVAC Division, Sperry Rand Corp.

.14 Maintainer: . . . . . as above.

.15 Availability

Preliminary version: September, 1964.
Full version: . . . . . December, 1964.

.2 INPUT

.21 Language

.211 Name: . . . . . ART assembly language (page 790:171.100).
.212 Exemptions: . . . . . none.

.22 Form

.221 Input media —
Control data: . . . . . punched cards or magnetic tape.
Program: . . . . . cards, magnetic tape, paper tape, or drum.
.222 Obligatory ordering: . . ASM directive first, then proper logical sequence of instructions, followed by END directive.
.223 Obligatory grouping: . . . no.

.23 Size Limitations

.231 Maximum number of source statements: . . not limited.
.232 Maximum size source statements: . . . . . not limited.
.233 Maximum number of labels: . . . . . variable by configuration.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . . UNIVAC 418 machine language.
.312 Language style: . . . . . machine.
.313 Output media: . . . . . punched cards, paper tape, magnetic tape, or drum.

.32 Conventions

.321 Standard inclusions: . . none.
.322 Compatible with: . . . . EXEC (Executive System). ART Library System.

.33 Documentation

Subject	Provision
Source program:	. . . . listing.
Object program:	. . . . listing (in octal).
Storage map:	. . . . . no.
Restart point list:	. . . no.
Language errors:	. . . . listing.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Pass 1: . . . . . mixing and printing (if desired) of control and library inputs, according to external directives; copying of PROC's to core; copying of labels and their values to core; output of composite input to intermediate storage.
Pass 2: . . . . . Assembling from intermediate storage; evaluating of literals and eliminating of duplicates; referencing of label table for definitions; generating of PROC's; output of object code and listing.

.42 Optional Modes

.421 Translate: . . . . . yes.
.422 Translate and run: . . . yes.

.423 Check only: . . . . . no.
.424 Patching: . . . . . yes.
.425 Updating: . . . . . no.

.43 Special Features

.431 Alter to check only: . . no.
.432 Fast unoptimized translate: . . . . . yes.
.433 Short translate on restricted program: . yes.

.44 Bulk Translating: . . . . yes, with magnetic tape or drum.

.45 Program Diagnostics: . incorporated in EXEC operating system, plus coding diagnostics on listing.

.46 Translator Library

.461 Identity: . . . . . ART Library System.
.462 User restriction: . . . . none.
.463 Form —
Storage medium: . . . card, paper tape, magnetic tape, or drum.
Organization: . . . . . topic, book, chapter, and sentence.
Format: . . . . . symbolic or relocatable (absolute code is used for Bootstrap routine only).
.464 Contents —
Routines: . . . . . closed or open.
Functions: . . . . . yes.
Data descriptions: . . yes.
PROC's (macro-instructions): . . . . . yes.
.465 Librarianship —
Insertion: . . . . . yes.
Amendment: . . . . . yes.
Call procedure: . . . . by external directive cards; if library portion is a subroutine, linking must be done by the user.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead —

Name	Space	Comment
EXEC:	1,491 words plus 208 words per I/O Handler (average)	one I/O Handler routine is required for each type of peripheral device.
Fixed locations:	160 to 256 words plus 768-word overlay area.	depends upon facilities used (i.e., number of channels and number of kinds of EXEC services).

.512 Space required for each input-output file: . . . controlled user.
.513 Approximate expansion of procedures: . . . . . one-to-one.

.52 Translation Time: . . . approximately 400 object-code lines per minute (using 418-I with 12K core, Uniservo IIIC Tape Handlers, and 1004 II Printer for on-line listing).

.53 Optimizing Data: . . . . none.

.54 Object Program Performance: . . . . . unaffected; i.e., same as hand coding.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: UNIVAC 418 Central Processor with 8,192 core locations.
card reader or tape unit for control input.
1004 Printer.
device for source program input.
device for object program output.
.612 Larger configuration advantages: . . . . . 4,096 additional core locations permit operation under EXEC control.
additional magnetic tape unit or drum permits one-pass assembly.

.62 Target Computer

.621 Minimum configuration: any UNIVAC 418 system.
.622 Usable extra facilities: all.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	check	warning is printed.
Unsequenced entries:	no check.	
Duplicate names:	check	warning is printed.
Improper format:	check	warning is printed.
Incomplete entries:	no check.	
Target computer overflow:	check	diagnostic is printed and logged on console.
Inconsistent program:	check	warning is printed.
Truncated constant (over 18 bits):	check	warning is printed.

.8 ALTERNATIVE TRANSLATORS: . . . . ART III, which assembles UNIVAC 418 programs on the UNIVAC III Computer System.

OPERATING ENVIRONMENT: EXEC

.1 GENERAL

.11 Identity: . . . . . UNIVAC 418 Executive System.
EXEC.

.12 Description

The UNIVAC 418 Executive System, EXEC, is an on-line operating system that controls, sequences, and allocates facilities for user programs operating on the UNIVAC 418. The ART Assembly System language (page 790:171.100) provides facilities for linkage and communication with EXEC. A number of utility routines are designed to operate under EXEC control.

EXEC provides for the concurrent operation of four priority levels of programs: critical, real-time, batch, and computational. All executive tasks and the input-output handlers operate at the critical level. Coding at this level is non-suspendible, but for the most part, interruptible. One or more routines may exist at the real-time level. Their main characteristic is a sensitivity to and a dependence upon communications data as primary input-output. Routines at the batch level are standard, input-output oriented programs with no direct communications connections. The computation level is reserved for those programs which are low in input-output dependency.

The following functions are performed by EXEC:

- Priority Control — Remembers the current priority level and sets it to "critical" as required; suspends the current operation when appropriate and saves the environment at that level; returns control to the suspended operation when all higher-priority requirements are satisfied.
- Interrupt Answering — Logs interrupts if unable to process them; transfers control to the proper handler routine; returns control to the place where interrupt occurred with the proper environment restored.
- Clock Control — Maintains an internal clock; provides the time and date when queried; transfers control to specified locations at specified times (or after a lapse of time) in accordance with priority.
- I/O Interface — Fills requests for input and output functions according to priority; handles interrupts; returns control with notification of status.
- Utility Services — Assigns and releases facilities (core, tape units); loads programs or segments as requested by operator or internal call, and initiates loaded runs if desired; provides logging; calls in error routines; provides debugging aids.
- SNAPDUMP — Allows dumping of the contents of specified areas of core storage.
- Expanded Repertoire System — Calls for EXEC functions by means of undefined operation codes, which cause a "fault" condition.
- Place-to-Go Scheduling — Allows the specification of an address to which control is to be transferred. Places-to-go may be scheduled "as soon as possible" by priority (four queues are kept), at a particular time, or at the end of a specified time period.

The EXEC control routines are designed to maintain an orderly flow of control and sequencing of tasks. This is done through handling of interrupts, scheduling of requests from users, and maintenance of an "outstanding task structure" which allows concurrent work at each of four different operational levels.

Three possible conditions can exist when an interrupt is received. If the processor is in an idle state, the interrupt is handled immediately. If the processor is in a suspendible mode (i.e., real-time, batch, or computational priority level), the current program is suspended, its environment is saved, and the interrupt is then handled. If a critical mode exists, a flag is set, the interrupt is counted, and control is returned to the point of interrupt. The interrupt will be handled as an outstanding task when the EXEC functions have been completed.

After most EXEC routines, control is passed to the EXEC Switcher routine which scans "outstanding work" indicators. The switcher first determines whether any unanswered interrupts exist. These are processed in the following sequence:

(1) Communications input.

(2) Communications external (optional).

(3) Communications output.

(4) Self-imposed interrupts (by EXEC).

(5) Standard peripheral interrupts (in accordance with channel priority).

If all outstanding interrupts have been processed, the Switcher routine determines whether a suspended program exists. A maximum of three

.12 Description (Contd.)

suspended programs can exist at any one time (one each at the real-time, batch, and computational levels). If one or more suspended programs are indicated, the proper environment is restored and control is transferred to the highest-priority program. If no suspended program can be found, a scan is made of the place-to-go queues. For queues (one per priority level, in "first in-first out" sequence) are searched in order, and control is transferred to the first address found. If none of the above conditions exists, there is no outstanding work, and the computer enters the idle state.

.13 Availability: . . . . . September, 1964.

.14 Originator: . . . . . UNIVAC Division, Sperry Rand Corporation.

.15 Maintainer: . . . . . as above.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . . ART Library System is usually on a drum; it can also be on magnetic tape, paper tape, or punched cards.

.212 Independent programs: . punched cards, paper tape, magnetic tape, or drum.

.213 Data: . . . . . punched cards, paper tape, magnetic tape or drum.

.214 Master routines: . . . . core storage and magnetic tape or drum.

.22 Library Subroutines: . . no automatic facilities.

.23 Loading Sequence: . . . controlled by ARLO routine (loader), using internal calls or operator type-ins.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Segmenting of routines: . . . . . by ARLO executive routine, controlled by program parameters.

.312 Occupation of working storage: . . . . . controlled by FACSERV executive routine.

.32 Input-Output Units

.321 Initial assignment: . . . controlled by FACSERV executive routine.

.322 Alternation: . . . . . as coded by user.

.323 Reassignment: . . . . . controlled by FACSERV executive routine.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: . . . . . controlled by executive I/O Handler routines.

.42 Multiprogramming: . controlled by executive routine — 4 levels of programs are permitted.

.43 Multi-sequencing: . . no provisions.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Loading input error:	check	diagnostic on console printer.
Allocation impossible:	check before loading	diagnostic on console printer.
In-out error — single:	check	diagnostic on console printer.
In-out error — persistent:	check	diagnostic on console printer.
Storage overflow:	check	diagnostic on console printer.
Invalid instructions:	check	diagnostic on console printer.
Program conflicts:	partial checks	EXEC protects itself.
Arithmetic overflow:	no check.	
Invalid operation:	hardware check	interrupt.
Improper format:	check (in most cases)	console diagnostic.
Invalid address:	check (in most cases)	console diagnostic.
Reference to forbidden area:	check (in most cases)	console diagnostic.

.45 Restarts

.451 Establishing restart points: . . . . . no automatic provision.

.452 Restarting process: . operator issues a bootstrap command which causes the EXEC routine to be loaded. EXEC initializes itself and transfers to a START routine (provided by programmer).

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . MS routine logs on console the time that an instruction at a particular address is executed; initiated by program.

(Contd.)

.512 Snapshots: . . . . . SNAPDUMP routine; can be initiated by a program, from console keyboard, or from the maintenance panel; output is on 1004 Printer or magnetic tape.

.52 Post Mortem: . . . . . SNAPDUMP routine; see preceding entry.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . . console typewriter messages.

.612 Action required by operator: . . . . . console typewriter messages.

.613 Reporting progress of run: . . . . . console typewriter messages.

.62 Operator's Decisions: . . . . . console keyboard entries.

.63 Operator's Signals

.631 Inquiry: . . . . . console keyboard entries.

.632 Change of normal progress: . . . . . console keyboard entries.

.7 LOGGING: . . . . . console typewriter messages, controlled by CONSERV executive routine.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . . 418 Central Processor with at least 1,491 words of core storage for EXEC use, plus approx. 208 words for each I/O Handler routine required.
Console keyboard-printer.
At least one of the following:
Card reader
Magnetic tape unit
Paper tape subsystem
Standard Communication Subsystem with 6-8 level Teletype ASR unit.

.812 Usable extra facilities: . . . . . additional 924 to 1,024 words of core storage and 1 tape unit or drum for automatic handling of concurrent real-time and batch programs.

.813 Reserved equipment: . . usually all of bay 0 (4,096 locations of core storage) and at least an equal amount of drum storage (user option).

.82 System Overhead: . . . approximately 30% of EXEC is always in core storage.

.83 Program Space Available: . . . . . all of available core and drum storage except reserved areas listed in Paragraph .813.

.84 Program Loading Time: . . . . . limited by speed of input device.

.85 Program Performance

Times required by EXEC to respond to an interrupt and initiate an input-output operation in the UNIVAC 418-II Processor, according to the manufacturer, are as follows:

- When the processor is busy: 1.19 msec plus time required to schedule the I/O operation.
- When the processor is idle: 0.52 msec plus time required to schedule the I/O operation.
- For communications I/O: 0.64 msec plus time required to schedule the I/O operation.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (790:201.100)

These problems involve updating a master file from information in a detail file and producing a printed record of each transaction. This application is one of the most common commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide. Standard File Problems A, B, and C show the effects of three different record sizes in the master file. Standard Problem D shows the effect of increasing the amount of computation performed upon each transaction. Each problem is estimated for activity factors (ratios of number of detail records to number of master records) of zero to unity. In all cases a uniform distribution of activity is assumed.

Because multiprogramming is a featured capability of the UNIVAC 418, the central processor time requirements are shown on all of the graphs in addition to the usual curves of elapsed time (i.e., total processing time). The difference between the curves of elapsed time and central processor time represents the amount of central processor time that is potentially available for concurrent processing of other programs. An analysis of the resulting graphs shows that in Standard Configuration III, the central processor is available to process other programs during approximately 80% of the total time required to handle the Standard File Problems.

In order to show its true potential for business data processing in more than one equipment configuration and operational mode, the UNIVAC 418's performance on the Standard File Problems has been analyzed for two different cases, as described in the following paragraphs:

(1) Conventional processing, with on-line card reading and printing during the file processing run.

(2) Multiprogrammed operation, with separate card-to-tape, processing, and tape-to-printer runs performed on the same main frame.

The ability of the UNIVAC 1004 to operate off-line with respect to the 418 permits tape-to-tape processing with off-line card-to-tape and tape-to-printer transcriptions. The graphs for the 418 in this mode of operation would be the same as those for the main Processing Run for Configuration VIIA.

CONVENTIONAL PROCESSING (CONFIGURATION III)

In Configuration III the master files are on magnetic tape. The detail file is assigned to the on-line 1004 card reader and the report file to the on-line 1004 printer. For Problems A, B, C, and D, the printer is the controlling factor at high, moderate, and low activities. The two master file tapes control at activities near zero.

MULTIPROGRAMMED OPERATION (CONFIGURATION VIIA)

In Configuration VIIA, it is assumed that file processing jobs will generally be divided into three separate runs:

(1) Card-to-tape transcription of the detail file.

(2) Main processing run, with all files on magnetic tape.

(3) Tape-to-printer transcription of the report file.

Depending upon the size of the file to be processed and the installation's other work, these three runs might be performed sequentially or concurrently. All of the prescribed processing for the Standard File Problems is performed during the main processing run; the other two runs are straightforward data transcriptions. The detail and report files are unblocked.

The graphs for Configuration VIIA (pages 790:201.116 and 790:201.145) show the time required for two distinct programs: (1) the main (tape-to-tape) Processing Run; and (2) the card-to-tape and tape-to-printer Transcription Runs, which are assumed to run in parallel.

For each program, both the total elapsed time (usually controlled by one or a combination of input-output devices) and the central processor time are shown, so that estimates of the amount of central processor time available to process other programs can easily be made.

Because of space limitations, performance in the multiprogrammed mode is shown for Standard File Problems A and D only. Problem D shows the effect of tripling the amount of computation performed in the main Processing Run; times for the Transcription Runs are unaffected.

The curves for the Transcription Runs are similar to those for Configuration III, except that the printer is the controlling factor at all activities. The controlling factors for the main Processing Run are the central processor at high and moderate activities, and the report file tape and one master file tape at low activity.

SORTING (790:201.200)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A by the method explained in Paragraph 4:200.213 of the Users' Guide. A three way merge was used in both Configurations III and VIIA. The results are shown in Graph 790:201.200. Configuration III uses the economical Uniservo VIC Tape Units without read-write overlap. The Uniservo IVC Tape Units which are used in Configuration VIIA are faster and provide read-write-compute simultaneity for significantly better performance.

Times for the standard UNIVAC 418 Sort/Merge routine are not available to date.

WORKSHEET DATA TABLE 1 (STANDARD FILE PROBLEM A)

	ITEM		CONFIGURATION III		CONFIGURATION VIIA (Main Processing Run)		REFERENCE
1 Input-Output Times	Words/block	(File 1)	340		340		
	Records/block	K (File 2)	10		10		
	msec/block	File 1 = File 2	47.5		11.3*		
		File 3	93		0.9*		
		File 4	142		1.5*		
	msec/switch	File 1 = File 2	0		0		4:200.112
		File 3	0		0		
		File 4	0		0		
	msec penalty	File 1 = File 2	2.7		2.7		
		File 3	0.22		0.22		
		File 4	0.35		0.35		
2 Central Processor Times	msec/block	a_1	0.68		0.68		
	msec/record	a_2	0.79		0.79		
	msec/detail	b6	0.34		0.34		4:200.1132
	msec/work	b5 + b9	0.56		0.56		
	msec/report	b7 + b8	19.15		19.15		
3 System Performance at F = 1.0	msec/block for C.P. and dominant I/O column.		C.P.	Printer	C.P.	Tapes	
		a_1	0.7		0.7		
		a_2 K	7.9		7.9		
		a_3 K	200.5		200.5		
		File 1 Master In	2.7		2.7		4:200.114
		File 2 Master Out	2.7		2.7	21.2	
		File 3 Details	2.2		2.2		
		File 4 Reports	3.5	1,420	3.5	123.0	
		Total	220.2	1,420	220.2	144.2	
4 Storage Space Required	Unit of measure	18-bit words					
		Std. routines	2,900		3,900		
		Fixed	160		160		
		3 (Blocks 1 to 23)	831		831		
		6 (Blocks 24 to 48)	4,086		4,086		
		Files	1,502		1,786		4:200.1151
		Working	34		34		
		Total	9 513		10,797		

* Plus start-stop time.

(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes —
Master file:. . . . . 108 characters, packed into 34 UNIVAC 418 words.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

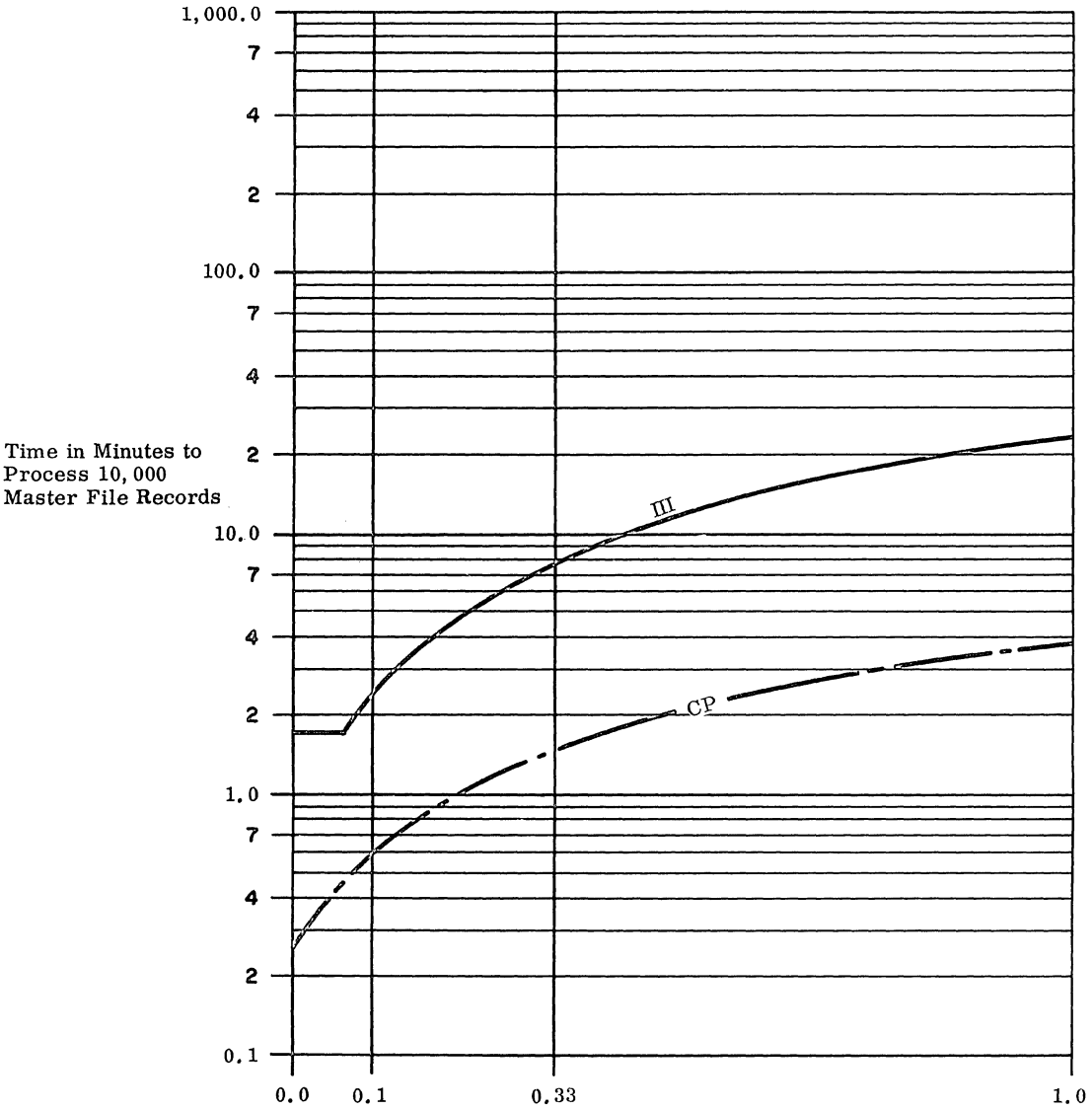
.112 Computation:. . . . . standard.

.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113; see also page 790:201.001.

.114 Storage space required —
Configuration III: . . . 9,513 words.
Configuration VIIA (multiprogrammed):. 10,797 words.

.115 Graph showing performance in conventional processing mode: . . . . . see graph below.

CONVENTIONAL PROCESSING (CONFIGURATION III)



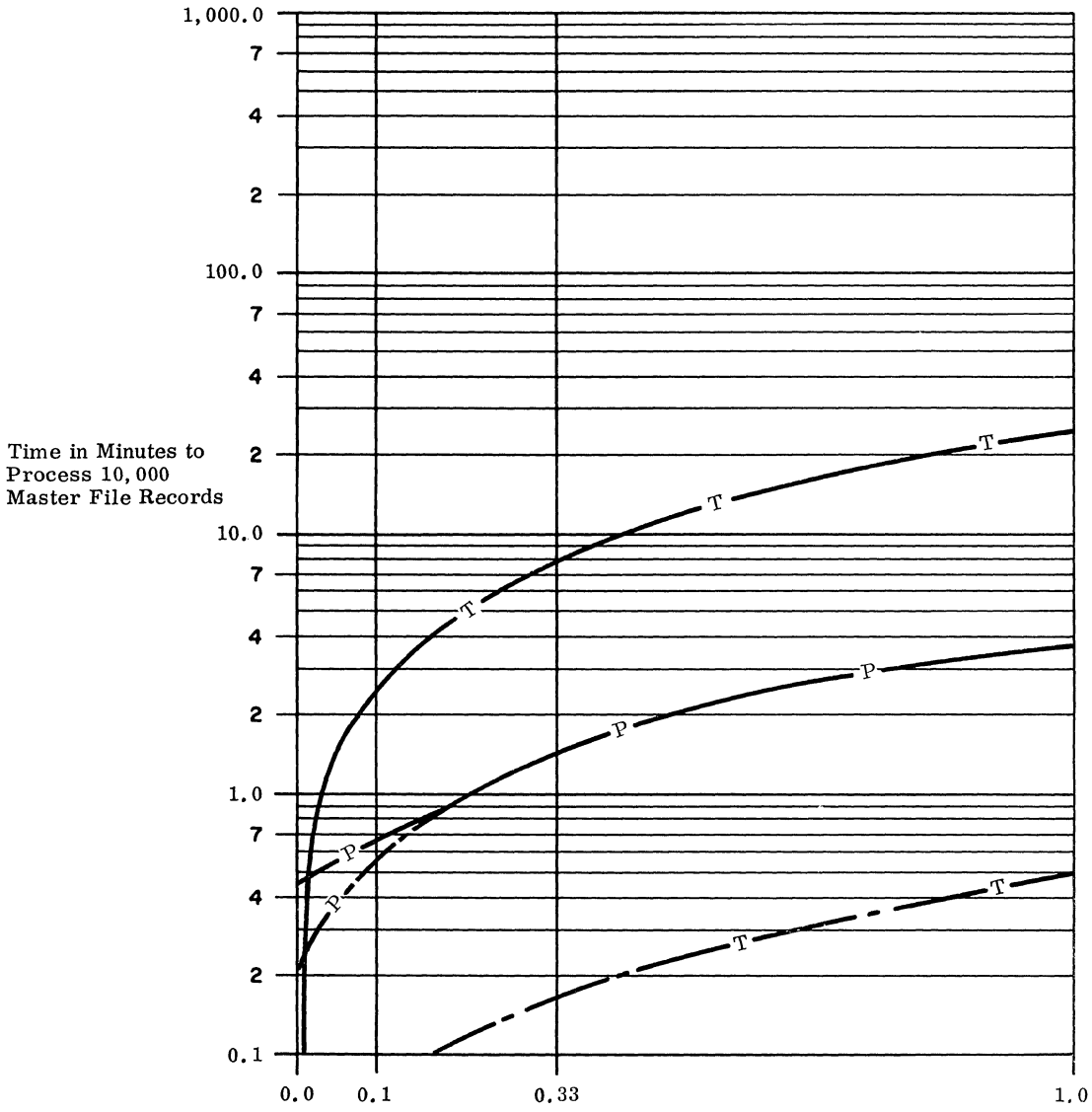
LEGEND

Elapsed time
CP Central Processor time

.11 Standard File Problem A (Contd.)

.116 Graph showing performance in a multiprogrammed environment: . . . . . see graph below.

MULTIPROGRAMMED OPERATION (CONFIGURATION VIIA)



LEGEND

P	Elapsed time for main processing run.
T	Elapsed time for data Transcription runs.
P	Central Processor time for main Processing run.
T	Central Processor time for data Transcription runs.

(See also the explanation under "Multiprogrammed Operation" on page 790:201.001.)

(Contd.)

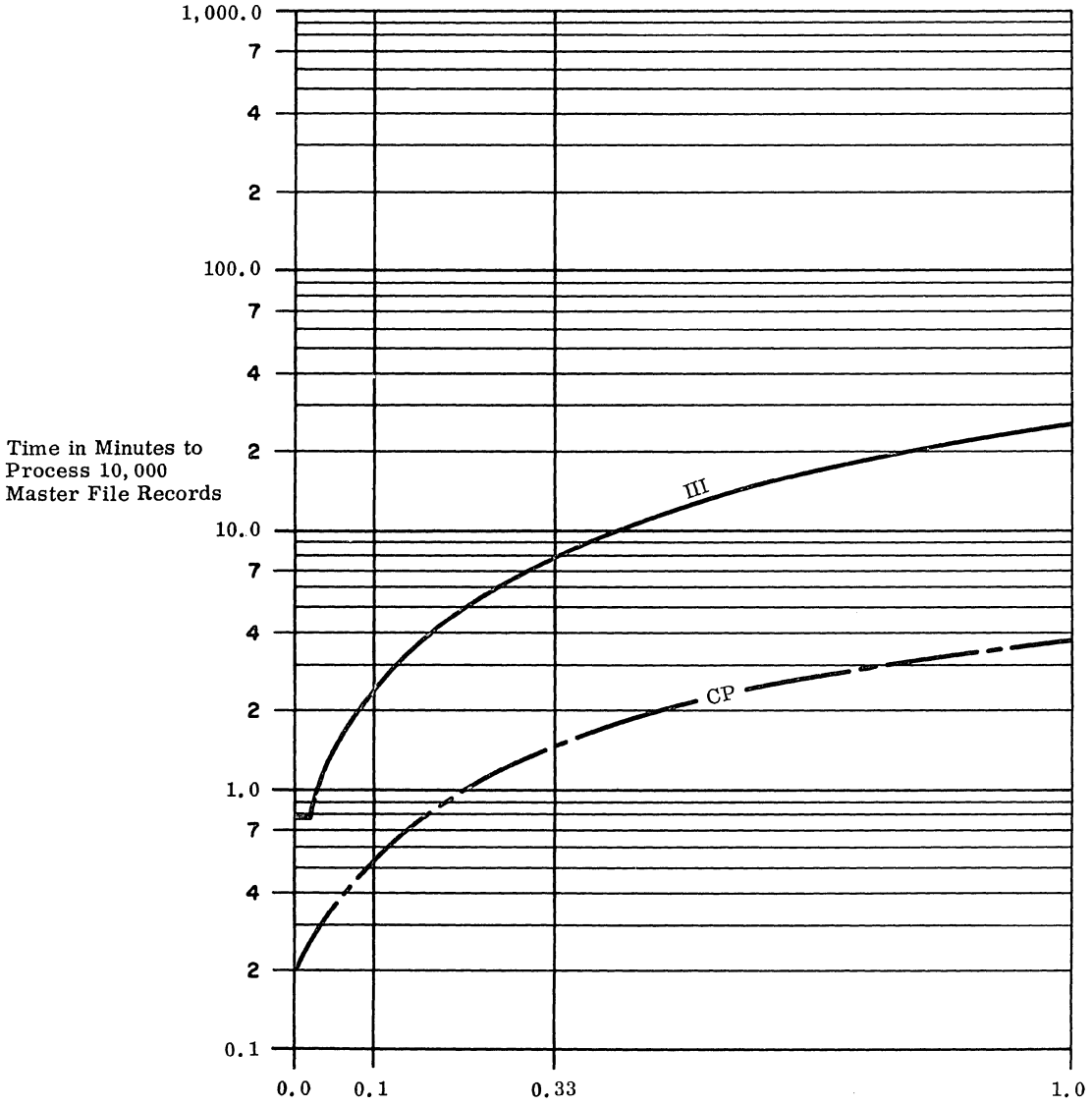
.12 Standard File Problem B

.121 Record sizes —
Master file:. . . . . 54 characters, packed into 17 UNIVAC 418 words.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.

.122 Computation:. . . . . standard.

.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.

.124 Graph: . . . . . see graph below.



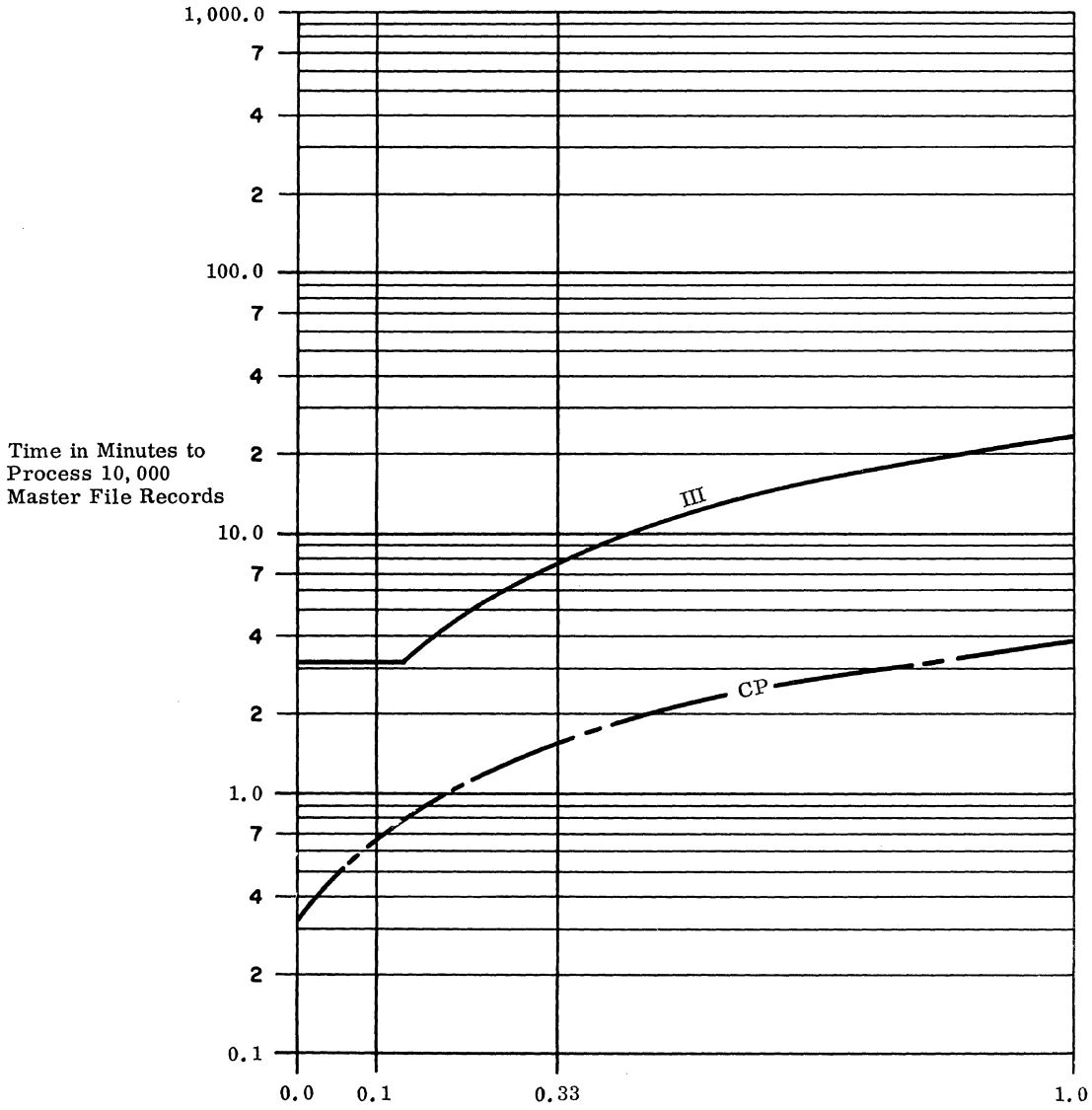
.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . 216 characters, packed into 68 UNIVAC 418 words.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.

.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13

.134 Graph: . . . . . see graph below.



(Contd.)

.14 Standard File Problem D

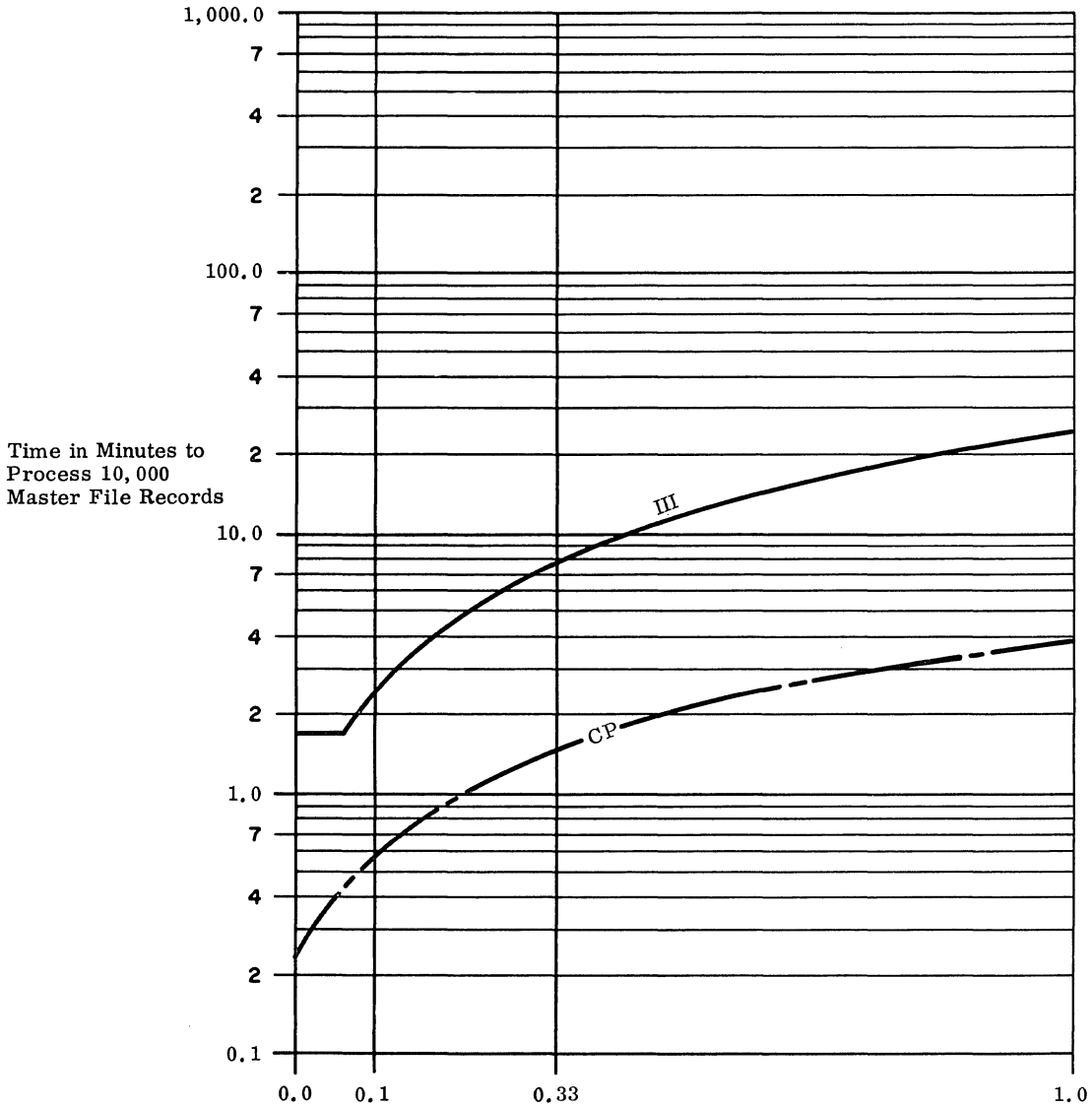
.141 Record sizes —
Master file: . . . . . 108 characters, packed into 34 UNIVAC 418 words.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.

.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14; see also page 790:201.001.

.144 Graph showing performance in conventional processing mode: . . . see graph below.

CONVENTIONAL PROCESSING (CONFIGURATION III)



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

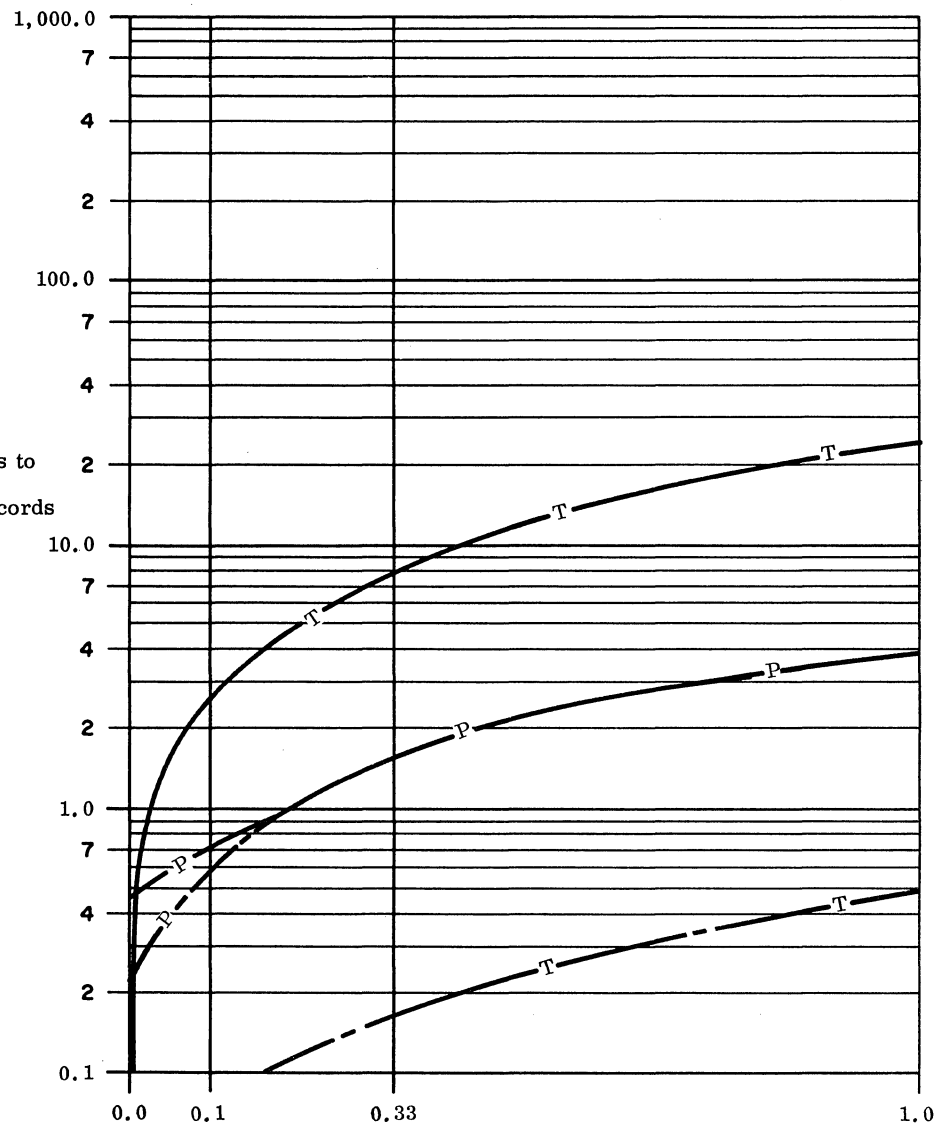
LEGEND

Elapsed time.
CP Central Processor time

.14 Standard File Problem D (Contd.)

.145 Graph showing performance in a multiprogrammed environment: . . . . . see graph below.

MULTIPROGRAMMED OPERATION (CONFIGURATION VIIA)



LEGEND

P — Elapsed time for main Processing run.
T — Elapsed time for data Transcription runs.
P — Central Processor time for main Processing run.
T — Central Processor time for data Transcription runs.

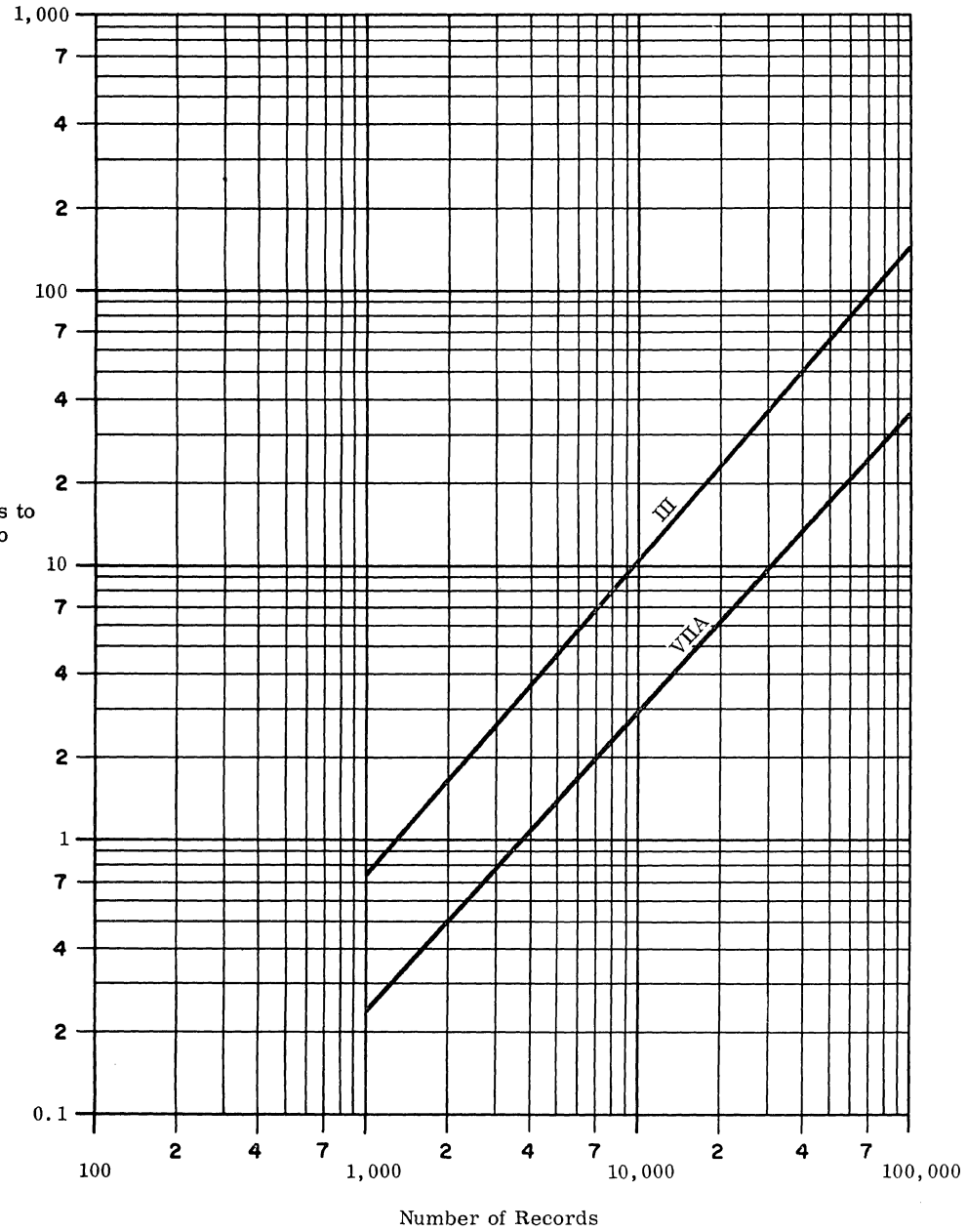
(See also the explanation under "Multiprogrammed Operation" on page 790:201.001.)

(Contd.)

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.
.212 Key size: . . . . . 8 characters.
.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.
.214 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hour
Central Processor without Console	26	88	65	1,050	2.5	6,700
Central Processor with Console	68	107	65	1,125	2.5	8,300
Standard Communication Subsystem	96	26	80	2,000	4.1	12,000
FH-330 Drum (1 drum)	48	26	64	980	7.1	3,819
FH-330 Drum (2 drums)	96	26	64	1,745	8.6	5,590
FH-330 Drum (3 drums)	96	26	64	2,060	10.1	6,372
FH-330 Drum (4 drums)	144	26	64	2,825	11.6	8,143
FH 330 Drum (5 drums)	144	26	64	3,140	13.1	8,925
1004 Processor	71	63	55	2,021	3.0	8,500
1004 Punch	42	25	49	870	1.5	3,500
Tape Adapter Cabinet	26	26	64	600	1.8	2,500
Uniservo IIIC	31	30	64	800	2.75	7,500
Uniservo IIA Synchronizer	20	35	82	600	1.56	2,075
Uniservo IIA	31	30	69	800	2.63	7,140
Uniservo IIIA Synchronizer	20	35	32	600	0.96	2,075
Uniservo IIIA	31	30	64	800	2.75	7,500
Uniservo Power Supply	24	26	64	1,200	3.0	8,200
Fastrand Synchronizer	20	35	82	600	1.56	2,075
Fastrand Drum Unit	122	35	64	5,300	7.0	19,500
FH-880 Synchronizer	20	35	82	600	1.56	1,640
FH-880 Drum	54	35	80	1,300	2.2	5,125
Printer Control	20	35	82	600	1.56	3,000
High Speed Printer	46	32	55	1,250	1.7	5,100
Paper Tape Subsystem	24	35	96	475	1.2	5,100

General Requirements

Temperature: . . . . . 60 to 80°F.
Relative Humidity: . . . . . 40 to 70%.
Power: . . . . . 120/208V, 60-cycle, 3-phase, 5-wire. Individual units may require power from Motor/Alternator, voltage-regulated power from Power Supplies, and/or unregulated power; consult UNIVAC for details.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR	UNIVAC 418-I	Central Processor (4 μsec cycle); includes 4,096 words of core storage, 8 I/O channels, and Operator's Panel.	1,950	250	70,200
		Optional Features for 418-I:			
		Additional 4,096 words of Core Memory (max. 3)	250	40	9,000
		4 Additional I/O channels (max. 16 channels total)	200	15	7,200
		Console (keyboard-printer)	250	15	9,000
		Console Alarm	25	3	900
		Day Clock	60	5	2,400
	UNIVAC 418-II	Central Processor (2 μsec cycle); includes 4,096 words of core storage and 8 I/O channels.	2,050	250	73,800
		Optional Features for 418-II:			
		Additional 4,096 words of Core Memory (max. 15)	350	40	12,600
		4 Additional I/O channels (max. 16 channels total)	200	15	7,200
		Console (keyboard-printer)	250	15	9,000
		Console Alarm	25	3	900
		Day Clock	60	5	2,400
INTERNAL STORAGE		Core Memory See Central Processor, above			
		Magnetic Drum Subsystems			
	FH-220	Drum Unit and Synchronizer (max. 1 drum)	1,000	30	36,000
	FH-330	Control and Synchronizer Unit (includes 1 Drum Unit)	2,000	155	72,000
		Additional Drum (max. 4)	1,200	80	40,000
		Dual Drum Unit (max. 2)	2,400	160	80,000
	FH-880	Control and Synchronizer Unit	2,000	165	71,000
		Drum Unit (max. 8)	1,420	165	92,000
		Fastrand Mass Storage Subsystems			
	I	Fastrand I Mass Storage Control	1,000	35	136,000
		First Mass Storage Unit	3,300	250	160,000
		Additional Units (max. 7)	3,300	120	160,000
	II	Fastrand II Mass Storage Control	1,000	35	36,000
		First Mass Storage Unit	3,800	265	184,000
		Additional Units (max. 7)	3,800	125	184,000

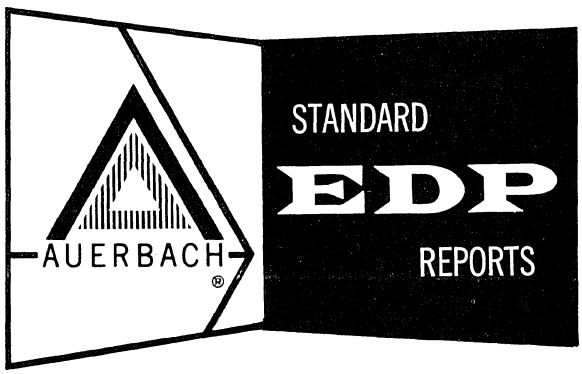
CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INTERNAL STORAGE (Contd.)		Optional Features for Fastrand:			
		Fastbands Option (24 bands)	200	22	9,000
		Write Lockout	25	3	1,125
		Dual Computer and Read-Read/ Read-Write	300	20	13,500
INPUT-OUTPUT		Uniservo Magnetic Tape Subsystems			
	IIA	IIA Tape Handler	450	95	20,000
		IIA Control & Synchronizer	1,550	130	77,500
		IIA Power Supply (for 6 tapes)	350	35	17,500
	IIIA	IIIA Tape Handler	700	155	36,500
		IIIA Control and Synchronizer	2,750	100	99,000
		IIIA Power Supply (for 6 tapes)	350	40	17,500
	IIIC & IVC	IIIC Tape Handler - 200/556 CPI	750	62	36,500
		IVC Tape Handler - 800 CPI	800	95	38,400
		Control Unit & Synchronizer - 200/556 CPI	985	85	35,460
		800 CPI option	100	5	3,600
		Read-Read/Read-Write (second data path)	985	85	35,460
		Translator	100	5	3,600
		Power Supply (for 6 tapes)	215	35	8,600
	VIC	VIC Tape Handler - 200/556/800 CPI	300	75	12,000
		Synchronizer	600	30	24,000
		Control and one tape handler	500	125	20,000
		Paper Tape Subsystem (paper tape reader, punch, and control unit)	150	25	6,000
		High-Speed Printer Subsystem			
		Printer (700-922 LPM)	800	240	36,000
		Printer Control & Synchronizer	1,750	160	80,000
		Punched Card Subsystem (See complete price list for UNIVAC 1004, page 770:221.100)			
		418/1004 Channel Adapter	100	15	4,000
		Intercomputer Couplers			
		Single Channel (418/418)	600	60	24,000
		Dual Channel (418/1107-1108 or 490)	800	60	32,000
		418/UNIVAC III Channel Adapter	450	40	14,300
		Transfer Switching Units			
		Single I/O Pair	60	4	2,700
		Dual I/O Pair	120	8	5,400
		Cabinet	50	-	2,250

For prices of Standard Communications Subsystem components, see UNIVAC 1050 Price Data section, page 777:221.103.

UNIVAC 490 SERIES

Univac

(A Division of Sperry Rand Corporation)



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UNIVAC 490 SERIES

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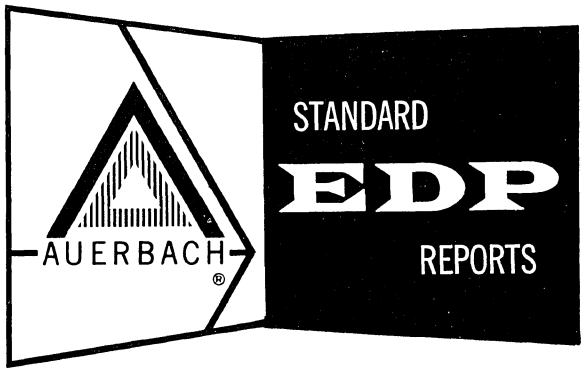

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CONTENTS

Report 801: UNIVAC 490

Report 802: UNIVAC 491/492

Report 804: UNIVAC 494

INTRODUCTION

.1 SUMMARY

The UNIVAC 490 Series consists of three recently-announced, medium-to-large-scale computer systems (the 491, 492, and 494) and one older system (the 490) which was initially delivered in December of 1961. The three newer systems, announced in June of 1965, are also known as the "UNIVAC Modular 490 Real-Time Systems."

The 490 Series is designed primarily for applications that require control based upon continuously updated records. Examples of this type of real-time application, in which it is essential or highly desirable to reduce the time lag between the occurrence of a transaction and the corresponding updating of one or more master files, include airline reservation systems, savings bank operations, production scheduling, inventory control, and order processing. Message switching is another important application. The 490 Series is also suitable for commercial applications of the more conventional batch processing type, particularly when they are run as "background" programs to use the processor time periods that would otherwise be idle between real-time transactions.

The principal characteristics that make the UNIVAC 490 Series suitable for real-time applications are:

- A variety of fast, large-capacity random-access storage units for master-file data and systems programs.
- Hardware and software facilities that permit concurrent processing (multiprogramming) of real-time and batch programs.
- Flexible data communications equipment that facilitates two-way communications between the computer and remote points.

The original UNIVAC 490 system evolved as a commercial outgrowth of UNIVAC's Defense Systems computer development work. Originally conceived as a special-purpose system for airline reservations, the 490 was later successfully applied to a wide range of other commercial applications. A major factor in enhancing the saleability and effectiveness of the 490 was the development of REX, an integrated, drum-oriented operating system capable of controlling the concurrent operation of one real-time program and one or more batch-type programs. REX is used by the majority of 490 installations, and will serve as the standard operating system for the newer UNIVAC 491 and 492 as well.

The major change in the original UNIVAC 490 system during its four-year production cycle was the introduction of an optional feature that improves its basic memory cycle time from 6 to 4.8 microseconds, with proportional increases in internal processing speeds. About 60 UNIVAC 490 systems have been delivered to date.

The three recently-announced members of the 490 Series follow the industry trend by offering significantly more performance per dollar than their predecessor. Using a typical 10-tape system (our Standard Configuration VIIA) as a basis for comparison, the original UNIVAC 490 system, with a 6-microsecond cycle time, rents for $31,270 per month. The newer UNIVAC 491, with a 4.8-microsecond cycle time, rents for $23,715 per month — a 24% reduction in rental. The UNIVAC 492 is identical to the 491 except that the 492 provides six more I/O channels at a rental increase of $1,750 per month. The powerful new UNIVAC 494, with actual and effective cycle times of 0.75 and 0.375 microseconds, respectively, rents for $32,715 per month, or only 5% more than the much slower 490. The 494 also provides an expanded instruction repertoire and improved multiprogramming capabilities. It is clear that UNIVAC's marketing strategy in announcing the three new systems is to attract new customers through the lower price tags on the 491 and 492, while retaining present customers by enabling them to trade up to the more powerful but program-compatible 494 at very modest increases in cost.

The structure of this report parallels that of our other recent reports on computer "families"; it is designed to present the facts about the 490 Series in a manner that will make it easy for you to locate the material you need, while placing proper emphasis upon the similarities and differences among the various models. This coverage consists of a general Computer System Report (behind Tab 800) which analyzes the concepts, hardware, and software that are common to all or most of the 490 Series models, plus individual Subreports (behind Tabs 801, 802, and 804) which report the characteristics and performance of the individual 490 Series processors and of computer systems based upon them.

.2 CENTRAL PROCESSORS AND CORE STORAGE

In all four of the UNIVAC 490 Series processors, each 30-bit word location in core storage can hold one instruction, one 30-bit or two 15-bit binary data items, or up to five alphameric characters. Core storage capacity can range from a minimum of 16,384 words (in all models) to a maximum of 32,768 words in the 490, 65,536 words in the 491 or 492, and 131,072 words in the 494. Parity checks upon internal operations are performed only in the 494. Cycle times and other features of the 490 Series processors and core storage units are summarized in Table I.

TABLE I: CHARACTERISTICS OF THE UNIVAC 490 SERIES PROCESSORS

Processor Model	UNIVAC 490	UNIVAC 491	UNIVAC 492	UNIVAC 494
Maximum No. of I/O Channels	14 (12 available)	8 (6 available)	14 (12 available)	24 (23 available)
Core Storage Cycle Time, μsec	6.0 (4.8 optional)	4.8	4.8	0.75 (0.375 effective)
Core Storage Capacity, 30-bit words	16,384 or 32,768	16,384 to 65,536	16,384 to 65,536	16,384 to 131,072
Core Storage Protection	No	Yes; 1,024-word increments	Yes; 1,024-word increments	Yes; 64-word increments
Core Storage Overlap	No	No	No	Yes
Core Storage Parity Checking	No	No	No	Yes
Floating-Point Arithmetic	No	No	No	Yes
Double-Precision Arithmetic	No	No	No	Yes
Decimal Arithmetic	No	No	No	Yes
Maximum I/O Data Rate, characters/second	417,000	521,000	521,000	2,747,000

Facilities common to all of the 490 Series processors include a full complement of fixed-point binary arithmetic, Boolean, comparison, and shifting operations. Facilities for editing and radix conversion, however, are conspicuously absent. Any one instruction can be automatically repeated up to 32,767 times, permitting efficient table lookup and accumulate operations. There are seven index registers, with a typical set of related instructions for loading, testing, and storing them. (The 494 has two sets of seven index registers to facilitate operating system control.)

Sixty-two basic single-address instructions are common to all of the 490 Series processors. Each of these basic instructions consists of five distinct parts: a 6-bit operation code; a 3-bit field that can specify a variety of conditions under which a skip or jump shall occur; a 3-bit field that specifies whether the operand shall be a full word, a half word, or a literal; a 3-bit index register designator; and a 15-bit field that can specify an operand address, a literal operand, or a shift count. This flexible instruction format permits numerous variations of each of the 62 basic instructions.

The UNIVAC 494 has an expanded instruction repertoire that provides a full range of double-precision arithmetic, floating-point arithmetic, decimal arithmetic, and enhanced character-handling facilities. The 47 additional instructions which are unique to the 494 exceed the capacity of the 490 Series' 6-bit operation code field, so UNIVAC uses the next 6 bits of the instruction word to specify the operation code for these additional instructions. As a result, the 47 instructions which are unique to the 494 cannot specify the use of partial-word operands or transfers of control based upon the results.

Average execution time per instruction in a basic UNIVAC 490 Processor is about 10 microseconds. The longest instruction — Divide — requires 86.4 microseconds, while a few instructions require as little as 6 microseconds. All instruction times for a 491, 492, or a 490 with the optional 4.8-microsecond memory are exactly 20 percent shorter than the times for the basic 490.

Average instruction execution time for a UNIVAC 494 system with more than 16,384 words of core storage can approach the actual cycle time of 0.75 microseconds when odd/even

(Contd.)

.2 CENTRAL PROCESSORS AND CORE STORAGE (Contd.)

memory-bank overlapping is employed. This means that the next instruction can be read from one memory bank while the processor is executing an instruction that references an operand in the other memory bank. The overlap facility can also be used to minimize access conflicts when two UNIVAC 494 processors share the same core storage.

A UNIVAC 494 system can include a maximum of three central processors, any two of which can operate simultaneously by interleaving their accesses to core memory. Total core storage capacity is limited to a maximum of 131,072 words in two banks, as in a single-processor 494 system. Thus, the UNIVAC 494's capabilities for multiprocessing are significantly less powerful than those of the recently-announced UNIVAC 1108-II system; the multiprocessing capability for the 494 is provided primarily to ensure ample growth possibilities without extensive reprogramming for users of the 490 Series.

The 490 Series processors have effective program interrupt facilities which cause a transfer of control to one of 44 to 73 fixed core locations (depending upon the model) upon completion of an I/O operation, upon detection of a processor or I/O error, or upon overflow of either the real-time clock or the day clock. Interrupts from any or all I/O channels can be enabled or disabled by means of special instructions.

Storage protection facilities, which prevent user programs from gaining unauthorized access to specified areas of core storage, are an important factor to consider in evaluating computers with multiprogramming capabilities. The original UNIVAC 490 system has no storage protection facility. The 491 and 492 contain hardware facilities that permit individual 1,024-word blocks to be guarded against unauthorized access. The 494 provides effective protection through a combination of hardware facilities and the Omega operating system. The "Guard Mode," in which user programs will normally operate, prohibits the use of input-output instructions and other instructions reserved for operating system use. Individual 64-word blocks of core storage can be protected against writing only, or against both reading and writing. Attempted violations of storage protection cause program interrupts.

The maximum number of input-output channels available for each of the 490 Series processors is indicated in Table I. In every 490, 491, and 492 system, one channel is reserved for the console and one for the real-time clock. In the 494, a single channel serves both the console and the clock. Each of the remaining channels, in general, can accommodate one peripheral subsystem and can handle one data transfer operation at a time. The gross I/O data rates for all simultaneously-operating peripheral devices are limited to the figures shown in Table I.

.3 PERIPHERAL EQUIPMENT

Probably the most noteworthy aspect of the UNIVAC 490 Series peripheral equipment is the numerous drum storage units and magnetic tape units that are available. Table II summarizes the characteristics of the three head-per-track "Flying Head" drums and the two Fastrand units. The Flying Head drums provide rapid access to moderate amounts of data, while the Fastrand units use movable access mechanisms and store larger amounts of data, but with slower access times and data transfer rates. A smaller, less expensive "Modular Fastrand" subsystem was announced along with the newer 490 Series processors, but it was withdrawn from the line later in 1965. UNIVAC's line of mass storage devices for the 490 Series still lacks a unit with interchangeable-cartridge capabilities.

TABLE II: CHARACTERISTICS OF UNIVAC 490 SERIES DRUM STORAGE UNITS

Device	FH-432 Drum	FH-880 Drum	FH-1782 Drum	Fastrand I	Fastrand II
Storage capacity, 6-bit characters per unit	1.31×10^6	3.93×10^6	10.5×10^6	65.3×10^6	130.7×10^6
Storage capacity, 6-bit characters per subsystem	11.8×10^6	31.5×10^6	83.9×10^6	519×10^6	$1,038 \times 10^6$
Average access time, msec	4.25	17	17	92	92
Data transfer rate, characters/second	240,000	60,000	240,000	25,150	25,150
Usable with 490	No	Yes	No	Yes	No
Usable with 491/492	No	Yes	No	Yes*	Yes
Usable with 494	Yes	Yes	Yes	Yes*	Yes

*Not actively marketed; available as a "compatibility option."

.3 PERIPHERAL EQUIPMENT (Contd.)

Table III summarizes the characteristics of the five magnetic tape units available for 490 Series systems. UNIVAC now encourages use of the Uniservo VIC or VIIIC tape units, which use "industry-compatible" (i.e., IBM 729-compatible) 7-track tape. Optional dual-channel controllers permit read-write simultaneity within a single Uniservo VIC or VIIIC subsystem. The other three tape units were available for the original UNIVAC 490 system, and they are still offered as "compatibility options" to postpone or eliminate the need to convert large existing tape inventories.

TABLE III: CHARACTERISTICS OF UNIVAC 490 SERIES MAGNETIC TAPE UNITS

Device	Uniservo IIA	Uniservo IIIA	Uniservo IIIC	Uniservo VIC	Uniservo VIIIC
Tape Speed, inches/second	100	100	112.5	42.7	120
Recording Density, rows/inch	125/250	1,000	200/556	200/556/800	200/556/800
Peak Data Transfer Rate, Kilo-characters/second	12.5/25.0	125	22.5/62.5	8.5/23.7/34.1	24.0/66.7/96.0
Tape Units per Controller	2 to 12	2 to 16	2 to 12	1 to 16	1 to 16
IBM 729-Compatible	No	No	Yes	Yes**	Yes**
Read Backward Capability	Yes	Yes	No	Yes	Yes
Read-After-Write Checking	No	Yes	Yes	Yes	Yes
Usable with 490	Yes	Yes	Yes	No	No
Usable with 491/492/494	Yes*	Yes*	Yes*	Yes	Yes

* Not actively marketed; available as a "compatibility option."

** Optional feature provides compatibility with the 9-track IBM 2400 Series Magnetic Tape Units used with System/360.

Other peripheral equipment available for the 490 Series systems includes the following:

- Punched Card Subsystem: Consists of one Card Control and Synchronizer, one Card Reader, and/or one Card Punch. In UNIVAC 491, 492, and 494 systems, cards are read at the rate of 800 cards per minute (or 900 cpm if only the first 72 columns of each card are read) and punched at 300 cards per minute. Reading and punching can be performed in Hollerith, row binary, or column binary mode. (UNIVAC 490 systems use a 600-cpm card reader and a 150-cpm punch.)
- Paper Tape Subsystem: Consists of a reader, punch, and control unit in a single cabinet. Maximum speeds are 400 characters per second when reading and 110 characters per second when punching. Paper tape with 5 to 8 channels can be read and punched.
- High-Speed Printer Subsystem: Consists of a Control and Synchronizer Unit and one Printer. Maximum speed is 700 alphanumeric or 922 numeric 132-character lines per minute. There are 63 printable characters.
- UNIVAC 1004 Subsystem: The 1004 is a small, plugboard-programmed computer that can be connected on-line to a 490 Series system and can perform editing and input-output functions. The 1004 can read cards at 400 or 615 cards per minute and can print at 400 or 600 lines per minute, depending upon the model. Other peripheral equipment that can be connected to the 1004 includes a 200-cpm card punch and one or two magnetic tape units.
- Data Communication Subsystem (For UNIVAC 491, 492, and 494 systems): Consists of 1 Communication Terminal Module Controller and 1 to 16 Communication Terminal Modules, each of which can control a maximum of 2 input lines and 2 output lines. Up to 64 communications lines can thus be multiplexed into a single I/O channel. This multiplexing equipment enables the computer to send and receive data via most common-carrier facilities at transmission rates of up to 4,800 bits per second. The original UNIVAC 490 system uses similar communications equipment, although its nomenclature is different and its cost is higher.

(Contd.)

.3 PERIPHERAL EQUIPMENT (Contd.)

- Data Communication Terminals: These single-line controllers can be used for data communications applications where the multiplexing capabilities of the preceding subsystem are not required. Models are available for interfacing with the public telephone network (at 2,000 bits per second), a private voice-band line (at 2,400 bits per second), or a Telpak A link (at 40,800 bits per second).

.4 SOFTWARE

The introduction of a series of new computer systems that are program-compatible with an earlier system has obvious advantages for the manufacturer as well as for the user. Software developed and perfected for the older system can be supplied with the newer systems, thereby relieving many of the pressures usually associated with the software development process.

UNIVAC 491 and 492 systems will be able to utilize all of the existing UNIVAC 490 software. When operating in the special 490-compatible mode, UNIVAC 494 systems will also be able to use the existing software, but this mode will not permit full utilization of the 494's expanded capabilities. For this reason, current software development work is being concentrated upon new facilities for the 494. Eventually, UNIVAC plans to make subset versions of the 494 software available for the 490, 491, and 492, as replacements for the software originally developed for the 490. This approach to software development has two advantages for the UNIVAC 490 user who elects to retain his present equipment: he is assured of continued maintenance of the present software, and later he will be able to use a set of completely new, improved software facilities.

.41 UNIVAC 490 Software

Programs developed for the UNIVAC 490, all of which are currently available and usable with UNIVAC 491, 492, and 494 systems as well, can be summarized as follows:

- REX — An operating system capable of controlling a single real-time program and one or more batch programs, all operating concurrently. REX is designed to provide for efficient utilization of the available system components and to process a scheduled set of jobs with a minimum of operator intervention. REX requires a magnetic drum, at least one magnetic tape unit, and an average of about 4,000 core locations.
- SPURT — An assembly system that translates symbolic source programs into machine-language object programs in relocatable or absolute form. At least four magnetic tape units are required. Facilities for user-defined macro-instructions are available only for systems that include a Fastrand or Flying Head Drum.
- COBOL — A compiler for COBOL-61 source programs that operates under control of REX and produces a SPURT-coded symbolic program as output. All of Required COBOL-61 and a number of useful electives and extensions have been implemented. A magnetic drum and at least five magnetic tape units are required for COBOL compilations.
- Sort/Merge — A generalized routine that sorts data on magnetic tape according to programmer-specified parameters. The cascade method is used for the merge passes. From 3 to 12 Uniservo tape units on a single channel can be used, and an FH-880 Drum can be used in the presort phase when available. Sorting can be performed concurrently with a real-time program, under control of REX.
- Utility Routines — A series of generalized routines to perform such functions as:

  Transcribing data from one peripheral medium to another;
  Tracing and monitoring programs;
  Maintaining program libraries on magnetic tape;
  Transcribing programs from a library tape to a Master Instruction Tape in a specified sequence.

- Library Subroutines — Sixty subroutines designed to handle frequently-encountered programming tasks such as:

  Multi-precision arithmetic on binary or Fieldata-coded items;
  Character insertion and extraction;
  Radix conversions between Fieldata and binary formats;
  Editing (zero suppression, floating dollar sign, etc.);
  File control;
  Data movement, scaling, and rounding.

.42 UNIVAC 494 Software

The software being developed especially for the UNIVAC 494 centers around a comprehensive operating system called Omega, which is scheduled for delivery in June 1966. If the term "third-generation" can be applied to software, as well as to hardware, then Omega is a true third-generation operating system. The lessons learned in implementing and applying REX, the UNIVAC 490 operating system, were used as foundations for the development of Omega. The system is modular in design, a characteristic that will make it easier for UNIVAC to "retrofit" Omega for use on 490, 491, and 492 systems in the future.

Omega is designed to control the scheduling and execution of a mix of independent real-time and batch-type programs in a multiprogramming mode. Assigned priorities and balanced utilization of the system's facilities are the governing factors. Conflicting user programs are "rolled out" of core storage and restarted when the facilities required for their continued operation again become available. Exclusive control and allocation of all system facilities by Omega allows changes in configuration and/or operating procedures without direct impact on user programs. Omega requires 4,000 to 8,000 words of core storage for its resident routines, plus at least 786,432 words of drum storage.

The collection and loading of the routines required for a particular task is facilitated by having all source-language processors produce a common form of relocatable output. An integrated test system facilitates debugging operations and permits testing of new programs concurrently with the real-time operation of other programs.

The processing of batch-type programs is facilitated by Omega's facilities for automatic job-to-job transitions, communication within and between jobs, and services such as logging and accounting. An unusual feature of the batch processing environment is Omega's ability to provide multiprogramming within an individual activity. This "Fork and Join" function allows, for example, the second pass of a sort to begin processing the initial output of the first pass while the first pass is still transcribing data. The ability for computer systems with random-access storage to perform this type of processing is not new, but including this ability as a general software option is quite novel.

The following source-language processors are being developed for use with Omega:

- COBOL — The COBOL compiler for the UNIVAC 494 is based on the language defined in the Department of Defense report, COBOL Preliminary Edition 1964. Source-language compatibility with the existing COBOL-61 compiler for the UNIVAC 490 is stressed. The new 494 compiler, however, generates a basically "straight-line" form of object coding, whereas the 490 compiler uses generalized subroutines. Compilation times, execution times, and object program memory requirements are said to be reduced by the straight-line method. Additional time will be saved by having the new compiler's output in the generalized relocatable-loader format, thereby eliminating the separate assembly phase that the 490 COBOL compiler requires. The subset version of the 494 COBOL compiler, for use with UNIVAC 490, 491, and 492 systems, will be available with the initial release in the third quarter of 1966. A minimum of four magnetic tape units and one drum are required for compilation.
- FORTRAN IV — This one-pass compiler accepts a source language based upon the A.S.A. working specifications for FORTRAN as published in the Communications of the ACM, October 1964. No complex or logical operations are provided. Object-program execution speeds will be much higher on UNIVAC 494 systems than on the other 490 Series members because of the 494's inherent speed advantage and its built-in facilities for floating-point arithmetic.
- UNIVAC 494 Assembly System — The form of the new symbolic assembly system for the UNIVAC 494 will resemble that of the SLEUTH II assembly system for the UNIVAC 1107, which features extensive macro-instruction facilities. The new system (un-named to date) will facilitate effective utilization of the 494's expanded facilities. The SPURT assembly system developed for the UNIVAC 490 will also be retained for use in 494 installations where program compatibility with the smaller 490 Series processors is considered important.

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	30 bits	basic addressable storage unit in core and drum storage.
Half-word:	15 bits	high- or low-order 15 bits of a core storage location, addressable by k-designator in most instructions.
Row: (Uniservo VIC, VIIIC)	7 bits (6 data, 1 parity)	magnetic tape; holds 1 character in IBM-compatible format.
Row: (Uniservo VIC, VIIIC with optional feature)	9 bits (8 data, 1 parity)	magnetic tape; holds 1 byte or 1/4 of a program word.
Column:	12 positions	punched cards; usually holds 1 character.
Line:	132 characters	High-Speed Printer reports.
Block:	1 to N words	magnetic or punched tape.

.2 DATA FORMATS

Type of Information	Representation
Instruction:	1 word.
Fixed-point number:	1 word; 29 data bits and sign bit (or 1 half-word).
Floating-point number — 490, 491, 492:	2 words; 28 data bits and sign for fractional part, 15 bits for exponent.
494:	2 words; 48 data bits and sign for fractional part, 11 bits for exponent.
Alphameric character:	6 bits (internal), 1 row (tape), or 1 column (cards).
Card image (row binary):	3 words (2 with 30 bits and 1 with 20 bits) per card row; 36 consecutive words per card.
Card image (column binary):	2-1/2 card columns per word; 32 consecutive words per card.
Record:	1 to N words of logically related information.
File:	1 to N records.

SYSTEM CONFIGURATION

Every UNIVAC 490 Series computer system includes a Central Processor Set consisting of the following units:

- Central Processor (see Report Sections 801:051, 802:051, and 804:051 for details).
- Power Control Cabinet.
- Motor-Alternator.
- Control Console.
- Core Memory (see Report Section 800:041 for details).

A UNIVAC 490 Series Central Processor can contain from 6 to 24 general-purpose input-output channels, depending upon the model; and, with only a few exceptions, any one of the standard 490 Series peripheral subsystems can be connected to any one of the general-purpose channels. Please refer to Report Section 800:111, Simultaneous Operations, for the details and exceptions. The standard peripheral subsystems are described in Report Sections 800:042 thru 800:045 (mass storage) and 800:071 thru 800:102 (input-output).

For diagrams and prices of UNIVAC 490 Series systems arranged in standard configurations, as defined in Section 4:030 of the Users' Guide, see the System Configuration sections of the subreports on the individual models:

INTERNAL STORAGE: PROCESSOR STORAGE

.1 GENERAL

.11 Identity: . . . . . Processor Storage for UNIVAC 490, 491, 492, and 494.

.12 Basic Use: . . . . . working storage.

.13 Description

The main core storage characteristics of the 490 Series are summarized in Table I.

Main storage is physically integrated with the Processing Unit in UNIVAC 490, 491, and 492 systems, and is housed in separate cabinets in UNIVAC 494 systems. A synchronization facility in the UNIVAC 494 allows core memory to be shared by two or three processors.

.14 Availability: . . . . . 490: discontinued.
491: 9 months.
492: 9 months.
494: 9 months.

.15 First Delivery: . . . . . 490: December 1961.
491: December 1965.
492: December 1965.
494: June 1966.

.16 Reserved Storage

	490/491/492	494
Index registers:	0	0
Arithmetic registers:	0	0
Logic registers:	0	0
I/O control:	28 words	48 words
Interrupt control:	44 words	21 words*
Clocks:	1 word	4 words

* 16 additional locations are reserved when operating in the UNIVAC 490 mode.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . no interleaving in 490, 491, or 492; dual-bank interleaving in 494 systems with 32,768 words or more.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.282 Reading method: . . . . coincident current.
.283 Type of access: . . . . . uniform; read-out followed by rewrite.

TABLE I: CHARACTERISTICS OF 490 SERIES CORE STORAGE

Capacity, 30-bit words	UNIVAC 490 Series Models			
	UNIVAC 490	UNIVAC 491	UNIVAC 492	UNIVAC 494
16,384	8188 thru 8193	8187-99	8187-93	7005-99
32,768	8194 thru 8199	8187-98	8187-92	7005-98
40,960	—	8187-97	8187-91	—
49,152	—	8187-96	8187-90	—
57,344	—	8187-95	8187-89	—
65,536	—	8187-94	8187-88	7005-97
98,304	—	—	—	7005-96
131,072	—	—	—	7005-95
Parity Check	No	No	No	Yes
Cycle Time, μsec	6.0 (4.8 opt.)	4.8	4.8	0.750*
Read Access Time, μsec	1.9	1.5	1.5	0.375
Memory Lockout	None	1024-word increments	1024-word increments	64-word increments

* The 494's effective cycle time equals its read access time (0.375 μsec) when the odd-even addressing scheme is used with the dual banks of core storage in all models except the 7005-99.

.29 Potential Transfer Rates

	UNIVAC 490	UNIVAC 491/492	UNIVAC 494
Cycling rate, words/sec:	166,667	208,333	1,333,333
Data rate, words/sec:	166,667	208,333	1,333,333
Compound data rate, words/sec:	166,667	208,333	2,666,667

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see Table I.

.32 Rules for Combining Modules: . . . . . see Table I.

.4 CONTROLLER: . . . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: . . . . . 1 access facility per processor (2 in dual-bank 494 models).

.53 Access Time Parameters and Variations

(See table below)

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With self (via Central Processor): . . . . . 1 full or half word (or 1 double word in UNIVAC 494).

.73 Effective Transfer Rate

With self (via Central Processor) —

UNIVAC 490: . . . . . 83,000 words/sec or 415,000 char/sec, using repeated "Replace" instruction.

UNIVAC 491/492: . . 104,000 words/sec or 520,000 char/sec, using repeated "Replace" instruction.

UNIVAC 494: . . . . . 444,000 words/sec or 2,222,000 char/sec, using repeated "Replace" instruction.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check*	interrupt*
Invalid code:	check	interrupt
Receipt of data:	parity check*	interrupt*
Recording of data:	record parity bit.	
Recovery of data:	parity check*	interrupt*
Dispatch of data:	send parity bit.	
Timing conflicts:	check	resolved automatically by priority control network.

* In 494 only; not checked in 490/491/492 systems.

.53 Access Time Parameters and Variations

	UNIVAC 490	UNIVAC 491/492	UNIVAC 494
Access time:	1.9 μsec	1.5 μsec	0.375 μsec
Regeneration time:	1.9 μsec	1.5 μsec	0.375 μsec
Free time used by certain instructions:	2.2 μsec	1.8 μsec	-0.375 μsec*
Cycle time:	6 μsec	4.8 μsec	0.750 μsec**
For data unit of:	1 word	1 word	1 word

* Memory overlap facility.

** Effective cycle time is 0.375 μsec in dual-bank models.

INTERNAL STORAGE: FH-880 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 880 Magnetic Drum.
Type 7304.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 880 Magnetic Drum is an auxiliary storage device that provides rapid random access to moderate quantities of data or programs in UNIVAC 490 Series systems. Each drum has 880 read-write heads, each serving one track. The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the rotating drum. The flying head principle permits the use of larger drums with less critical tolerances, and the close head-to-drum spacing (0.0005 inch) permits high-density recording.

A Magnetic Drum Subsystem consists of from one to eight Flying Head 880 Magnetic Drums connected to a Drum Control and Synchronizer Unit. Each subsystem fully occupies one input-output channel. Each drum has a storage capacity of 786,432 words of 30 bits each. Maximum potential storage capacity is therefore 6,291,456 words per subsystem. See Table I for the maximum storage per computer system.

Of the 880 tracks on each drum, 768 are grouped into 128 data bands of six tracks each. The other 112 tracks are used for parity checking, timing, reference, and as spares. Each 490 word is converted by the Synchronizer into five 6-bit characters. The six tracks in each data band are read and recorded in parallel, and each word is stored in a six-by-five matrix of bit positions. An odd parity bit is generated for each word and recorded in a corresponding location in one of 32 parity tracks.

Each data band consists of 6,144 word locations arranged in the form of three interleaved "angular sections" of 2,048 words each. This means that any location can be accessed within one drum revolution, but a maximum of 2,048 words can be read or recorded per revolution. Drum speed is 1,770 revolutions per minute, so the average access time is 17 milliseconds. Peak data transfer rate is 60,000 words or 300,000 characters per second.

From 1 to 32,767 words can be transferred in a single operation. Each drum read operation requires two instructions, a Buffer Control Word and a Function Word. The instructions initiate the input buffer and external function on the appropriate input-output channel. The Buffer Control Word specifies the initial and final core storage addresses. The Function Word specifies the operation to be performed and the 23-bit initial drum address. Coding of a drum write operation is similar. A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired.

Checking includes a parity check to insure that each word read from the drum has odd parity, a character count to insure that each word transferred to or from the drum consists of exactly five characters, and checks for invalid drum addresses and function codes. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Computer a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . December, 1961.

.16 Reserved Storage: . . . 112 of the 880 tracks are reserved for spares, parity, and timing functions.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter:. . . . . 24 inches.
Length: . . . . . 30 inches.
Number on shaft: . . . 1.

TABLE I: FH-880 DRUM MODULE AND SYSTEM SIZES

	Minimum Storage	Maximum Subsystem	490 and 492 Maximum Storage	491 Maximum Storage	494 Maximum Storage
Drum Subsystems	1	1	12	6	24
Drums	1	8	96	48	192
Words	786,432	6,291,456	75,497,472	37,748,736	150,994,944
Characters	3,932,160	31,457,280	377,487,360	188,743,680	654,974,720
Instructions	786,432	6,291,456	75,497,472	37,748,736	150,994,944

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 6 Tracks

Words: . . . . . 6,144.
Characters: . . . . . 30,720.
Instructions: . . . . . 6,144.

.26 Bands per Physical Unit: . . . . . 128.

.27 Interleaving Levels: . . 3.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically supported head per track.

.283 Type of access —

Description of stage	Possible starting stage
Switch bands:	when different band is selected (or at end of a band).
Wait for specified sector:	when previously selected band is used.
Read or write 1 to 32,767 words:	when rotational delay is is zero.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 1,800 rpm.
Track/head speed: . . 2,265 inches/sec.
Bits/inch/track: . . . 409.
Bit rate per track: . . 925,200 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 30 bits per word.
Gain factor: . . . . . 6 tracks per band.
Loss factor: . . . . . 3 interleaving levels (always) times optional interlace factor of 1, 2, 4, 8, or 16.

Data rate:

Interlace option	Words/sec	Char/sec
1	60,000	300,000
2	30,000	150,000
4	15,000	75,000
8	7,500	37,500
16	3,750	18,750

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see Table I.

.32 Rules for Combining Modules: . . . . . 1 to 8 Drum Units per Magnetic Drum Subsystem; each subsystem fully occupies 1 input-output channel.

.4 CONTROLLER

.41 Identity: . . . . . FH-880 Drum Control and Synchronizer Unit. Type 8122.

.42 Connection to System

.421 On-line: . . . . . 1 to 6, 12, or 24 controllers (see Table I); 1 controller per Magnetic Drum Subsystem.
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1 to 8 FH-880 Drum Units.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 32,767 words; 1 to 4,096 words in UNIVAC 494 systems.
.442 Input-output area: . . . Core Memory.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization: . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads: one fixed head serves each track.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer operation per Magnetic Drum Subsystem.

.53 Access Time Parameters and Variations

.532 Variation in access time —

Stage	Variation, msec	Example, msec
Switch bands:	0 or 0.134	0.
Wait for specified sector:	0 to 33.3	16.7
Read or write:	0.0163 to 1,070*	33.3*
	0.0163 to 1,103	50.0

*16.3 μsec per word transferred; example is based on a 2,048-word transfer.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to 32,767 words, beginning with the first word of a drum sector; 1 to 4,096 words in UNIVAC 494 systems.

.73 Effective Transfer Rate

With core storage: . . . 3,750 to 60,000 words/sec, depending on the interlace option used.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit	interrupt.
Reference to locked area:	not possible.	

INTERNAL STORAGE: FH-432 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 432 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

One of the important considerations in multiprogramming is a system's ability to rapidly unload and reload individual programming tasks from auxiliary storage. The Flying Head 432 Magnetic Drum is an auxiliary storage device that provides the ability to load an entire 32,768-word UNIVAC 494 memory module in approximately 140 milliseconds, including average access time.

An FH-432 Magnetic Drum Subsystem consists of from three to nine Flying Head 432 Magnetic Drums connected to a Drum Control and Synchronizer Unit. Each subsystem fully occupies one input-output channel. Each drum has a storage capacity of 262,144 30-bit words. Maximum potential storage capacity is therefore 2,359,296 words per subsystem. FH-432 Magnetic Drum Subsystems cannot be connected to UNIVAC 490, 491, or 492 systems.

The drum speed of the FH-432 is 7,100 revolutions per minute, so the average access time is 4.25 milliseconds. Peak data transfer rate is 240,000 words per second. This rate is accomplished by reading and writing in a basically bit-serial mode, but with the data "staggered" among 3 tracks at a transfer rate of 80,000 words per second per track. The 550KC channel option is required to accommodate this data rate. An interlace factor of 2, 4, 8, or 16 is available, which reduces the data transfer rate to 120,000, 60,000, 30,000, or 15,000 words per second, respectively. There are 128 three-track bands per drum unit. The remaining 48 tracks are used for spares, parity, and timing functions.

FH-432 units can be intermixed with FH-1782 units in the same subsystem to satisfy requirements for some very fast-access drum storage in combination with the larger, slower-access FH-1782 units described in Section 800:044. A new function of the control logic of the FH-432 Subsystem enables the program to interrogate individual drum units to determine the storage location that is currently under the read-write heads. The Input/Output Handler routine can then select from the subsystem queue the data request that can be serviced fastest.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . . . 3rd quarter 1966.

.16 Reserved Storage: . . . 48 of the 432 tracks are reserved for spares, parity, and timing functions.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter: . . . . . 10.5 inches.
Length: . . . . . 9.0 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 3 Tracks

Words: . . . . . 2,048.
Characters: . . . . . 10,240.
Instructions: . . . . . 2,048.

.26 Bands per Physical Unit: . . . . . 128.

.27 Interleaving Levels: . . 1, 2, 4, 8, or 16.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically-supported head per track.

.283 Type of access —

Description of stage	Possible starting stage
Switch bands:	when different band is selected (or at end of band).
Wait for specified sector:	when previously selected band is used.
Read or write 1 to 32,767 words:	when rotational delay is zero.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rate: . . . . . 7,100 rpm.
Track/head speed: . . 3,950 inches/sec.
Bits/inch/track: . . . 687.
Bit rate per track: . . 6,224,220.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 30 bits per word.
Gain factor: . . . . . 3 tracks per band.
Loss factor: . . . . . interlace factors of 2, 4, 8, or 16 are optional.

Data rate:

Interlace option	Words/sec	Char/sec
1	240,000	1,200,000
2	120,000	600,000
4	60,000	300,000
8	30,000	150,000
16	15,000	75,000

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum per Subsystem	Maximum per 494 System
Drum Subsystems:	1	1	24
Drums:	3	9	216
Words:	786,432	2,359,296	18,874,368
Characters:	3,932,160	11,796,480	94,371,840
Instructions:	786,432	2,359,296	18,874,368

.32 Rules for Combining Modules: . . . . . 3 to 9 Drum Units per Magnetic Drum Subsystem; 1 to 24 Magnetic Drum Subsystems per UNIVAC 494 system. Each subsystem occupies 1 input-output channel.

.4 CONTROLLERS

.41 Identity: . . . . . FH-432/1782 Drum Control and Synchronizer Unit. Type 6013-02.

.42 Connection to System

.421 On-line: . . . . . 1 to 24 controllers; 1 per Magnetic Drum Subsystem.

.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 3 to 9 FH-432 Drum Units.

.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 4,096 words.

.442 Input-output area: . . . Core Memory.

.443 Input-output area access: . . . . . each word.

.444 Input-output area lockout: . . . . . none.

.445 Synchronization: . . . . automatic.

.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads: one fixed head serves each track.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer operation per Magnetic Drum Subsystem.

.53 Access Time Parameters and Variations

Stage	Variation, msec	Average, msec
Switch bands:	0 or 0.04	—
Wait for specified sector:	0 to 8.5	4.25
Read or write:	see Paragraph .292	

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to 4,096 words.

.73 Effective Transfer Rate

With core storage: . . . 15,000 to 240,000 words/sec, depending on the interlace option used.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit	interrupt.
Reference to locked area:	not possible.	

Note: The type of error is indicated by the Status Word, sent to the central processor when an interrupt occurs.

INTERNAL STORAGE: FH-1782 DRUM

.1 GENERAL

.11 Identity: . . . . . Flying Head 1782 Magnetic Drum.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Flying Head 1782 Magnetic Drum is similar to the FH-880 drum (Section 800:042) but offers a storage capacity that is greater by a factor of 2.67. The FH-1782's greater capacity is achieved partly by an increase in the number of tracks (to 1760) and partly by an increase in the recording density (to 547 bits per inch). The term "Flying Head" refers to the fact that the heads are aerodynamically supported on a boundary layer of air generated by the surface friction of the drum rotating at 1,800 revolutions per minute.

An FH-1782 Magnetic Drum Subsystem consists of from one to eight Flying Head 1782 Magnetic Drums connected to a Drum Control and Synchronizer Unit. Each subsystem fully occupies one input-output channel. A maximum of 24 Magnetic Drum Subsystems could be connected to a UNIVAC 494 if no other peripheral equipment were required. Each drum has a storage capacity of 2,097,152 words of 30 bits each. Maximum potential storage capacity is therefore 16,778,216 words per subsystem and 402,677,184 words per fully-expanded 494 system. FH-1782 Drums cannot be connected to UNIVAC 490, 491, or 492 systems.

Of the 1,760 tracks on each drum, 1,536 are grouped into 256 data bands of six tracks each. The other 224 tracks are used for parity checking, timing, reference, and as spares. Each UNIVAC 494 word is converted by the Synchronizer into five 6-bit characters. The six tracks in each data band are read and recorded in parallel, and each word is stored in a six-by-five matrix of bit positions. An odd parity bit is generated for each word and recorded in a corresponding location in one of 64 parity tracks.

Peak data transfer rate is 240,000 words or 1,200,000 characters per second. An interlace factor of 2, 4, 8, or 16 is available to decrease the transfer rate by the corresponding factor. From 1 to 32,767 words can be transferred in a single operation.

Each drum read operation requires two instructions, a Buffer Control Word, and a Function Word. The instructions initiate the input buffer and external function on the appropriate input-output channel. The Buffer Control Word specifies the initial and final core storage addresses. The Function Word specifies the operation to be performed and the 23-bit initial drum address.

A drum search operation causes successive drum locations to be scanned until a bit-by-bit match is found to an Identifier Word in the stored program. At this point a read operation can be automatically initiated if desired.

A new function has been incorporated in the control logic of the FH-432 and FH-1782 subsystems to predict and reduce storage access times. This function enables the program to interrogate a particular drum unit to determine which storage locations are currently under the read-write heads. The Input-Output Handler routine can then select from the subsystem queue the data request that can be serviced fastest.

Checking includes a parity check to ensure that each word read from the drum has odd parity, a character count to ensure that each word transferred to or from the drum consists of exactly five characters, and checks for invalid drum addresses and function codes. Detection of any drum error causes the Drum Control and Synchronizer Unit to initiate an external interrupt and send the Central Processor a Status Word indicating the type of error and the drum location at which it occurred.

.14 Availability: . . . . . 12 months.

.15 First Delivery: . . . . 4th quarter 1966.

.16 Reserved Storage: . . . 224 of the 1,760 tracks are reserved for spares, parity, and timing functions.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . drum.

.22 Physical Dimensions

.222 Drum —
Diameter: . . . . . 24 inches.
Length: . . . . . 36 inches.
Number on shaft: . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.

.242 Data regenerated constantly: . . . . . no.

.243 Data volatile: . . . . . no.

.244 Data permanent: . . . . no.

.245 Storage changeable: . . no.

.25 Data Volume per Band of 6 Tracks

Words: . . . . . 16,384.
Characters: . . . . . 81,920.
Instructions: . . . . . 16,384.

.26 Bands per Physical Unit: . . . . . 256.

.27 Interleaving Levels: . . 1, 2, 4, 8, or 16.

.28 Access Techniques

.281 Recording method: . . . 1 aerodynamically supported head per track.

.283 Type of access —

Description of stage	Possible starting stage
Switch bands:	when different band is selected (or at end of a band).
Wait for specified sector:	when previously selected band is used.
Read or write 1 to 32,767 words: . . .	when rotational delay is zero.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rate: . . . . . 1,800 rpm.
Track/head speed: . . 2,265 inches/sec.
Bits/inch/track: . . . 547.
Bit rate per track: . . 1,238,955 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . . 30 bits per word.
Gain factor: . . . . . 6 tracks per band.
Loss factor: . . . . . interlace factors of 2, 4, 8, or 16 are optional.

Data rate:

Interlace option	Words/sec	Char/sec
1	240,000	1,200,000
2	120,000	600,000
4	60,000	300,000
8	30,000	150,000
16	15,000	75,000

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see table below.

.32 Rules for Combining Modules: . . . . . 1 to 8 Drum Units per Magnetic Drum Subsystem; 1 to 24 Magnetic Drum Subsystems per UNIVAC 494 system. Each subsystem fully occupies 1 input-output channel.

.4 CONTROLLER

.41 Identity: . . . . . FH-432/1782 Drum Control and Synchronizer Unit.

.42 Connection to System

.421 On-line: . . . . . 1 to 24 controllers; 1 per Magnetic Drum Subsystem.
.422 Off-line: . . . . . none.

.43 Connections to Device

.431 Devices per controller: 1 to 8 FH-1782 Drum Units.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 4,096 words.
.442 Input-output area: . . . Core Memory.
.443 Input-output area access: . . . . . each word.
.444 Input-output area lockout: . . . . . none.
.445 Synchronization: . . . . automatic.
.447 Table control: . . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads: one fixed head serves each track.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer operation per Magnetic Drum Subsystem.

.53 Access Time Parameters and Variations

Stage	Variation, msec	Average, msec
Switch bands:	0 or 0.04	—
Wait for specified sector:	0 to 34.0	17.0
Read or write:	see Paragraph .292	
Total:	5.0 to 39.0	17.0

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With Core Memory: . . 1 to 4,096 words, beginning with the first word of a drum sector.

.73 Effective Transfer Rate

With core storage: . . . 15,000 to 240,000 words/second (exclusive of 17-msec average initial access time), depending on the interlace option used; see Paragraph .292.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bits.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit	interrupt.
Reference to locked area:	not possible.	

.31 Module and System Sizes

	Minimum Storage	Maximum per Subsystem	Maximum per 494 System
Drum Subsystems:	1	1	24
Drums:	1	8	192
Words:	2,097,152	16,778,216	402,677,184
Characters:	10,485,760	83,891,080	2,013,385,920
Instructions:	2,097,152	16,778,216	402,677,184

INTERNAL STORAGE: FASTRAND II

.1 GENERAL

.11 Identity: . . . . . Fastrand II Mass Storage Subsystem. Type 6010.

.12 Basic Use: . . . . . auxiliary storage.

.13 Description

The Fastrand Mass Storage Subsystem provides relatively fast random access to large quantities of data stored on magnetic drums. Each Fastrand Storage Unit has a capacity of about 26 million UNIVAC 490 Series words or 130 million characters. A Fastrand Subsystem consists of from one to eight Storage Units connected to a Fastrand Control and Synchronizer Unit. Average random access time to any record in Fastrand storage is 93 milliseconds.

The amount of on-line random access storage provided by Fastrand II can range up to almost 25 billion characters in UNIVAC 494 systems. Table I shows the maximum capacity for each 490 Series system for which Fastrand II storage is available.

Average random access time to any record in Fastrand II storage is 93 milliseconds. An option is available to provide a 35-millisecond average access to 50,688 additional words. This option, called Fastband, provides 24 fixed read/write heads. Another option provides lockout protection; it consists of a key-controlled switch which, when set, will prevent the writing of data in a specified area of the drum unit on which it is installed.

Each Fastrand II Storage Unit contains two magnetic drums, which are treated as a single logical unit by the controller. There are 64 aerodynamically-supported read/write heads per Storage Unit (32 per drum). All 64 heads are connected to a common positioning mechanism and move in unison. Head positioning time varies from 30 to 86 milliseconds and averages 58 milliseconds. Drum speed is 870 revolutions per minute, so the rotational delay varies from 0 to 69 milliseconds and averages 35 milliseconds. Activation of addressing circuits requires 5 milliseconds, but this is overlapped with the other access time factors.

Peak data transfer rate is 25,150 words or 125,750 characters per second. Optional interlace factors of 3, 7, or 9 are available for Fastrand units used with UNIVAC 490, 491, and 492 systems. The selected interlace factor applies to all Fastrand units within a subsystem and must be specified prior to delivery.

Each of the two drums in a Fastrand II Storage Unit has 6,142 data tracks; each track is divided into 64 sectors; and each sector holds 33 30-bit UNIVAC 490 Series words, recorded serially by bit. The data storage area on each drum is divided into 192 "positions", with 32 tracks per position. The 32 tracks that constitute a position are sequentially addressed but are not physically adjacent to one another; each of the 32 tracks is served by a separate read/write head.

Every Fastrand read or write operation requires two instructions, a Function Word, and a Buffer Control Word. The Function Word specifies the

TABLE I: FASTRAND II MODULE AND SYSTEM SIZES

	Minimum Storage	Maximum per Subsystem	491 Maximum Storage	492 Maximum Storage	494 Maximum Storage.
Subsystems	1	1	6	12	24
Storage Units	1	8	48	96	192
Drums	2	16	96	192	384
Words	25,952,256	207.6×10^6	$1,246 \times 10^6$	$2,492 \times 10^6$	$4,984 \times 10^6$
Characters	129,761,280	$1,038.0 \times 10^6$	$6,228 \times 10^6$	$12,456 \times 10^6$	$24,912 \times 10^6$
Instructions	25,952,256	207.6×10^6	$1,246 \times 10^6$	$2,492 \times 10^6$	$4,984 \times 10^6$
Sectors	786,432	6,291,456	37,748,736	75,497,472	150,994,944

Note: Fastrand II was not offered for use in UNIVAC 490 Series systems; halve the 492 capacities shown here for the corresponding capacities of the Fastrand IA mass storage which is used in 490 systems.

.13 Description (Contd.)

operation to be performed and the initial drum address. The Buffer Control Word specifies the core storage addresses of the first and last words to be transferred. Reading and writing must begin with the first word of the addressed sector and can continue over any number of sectors. The read or write operation is halted and an external interrupt signal is sent to the computer when: (1) the final core address specified in the Buffer Control Word is reached; (2) the end of the drum position is reached; (3) an error is detected; or (4) a "terminate" instruction is issued. Repositioning of the read/write heads to a different position is a separate operation, which can be carried out simultaneously in all the Fastrand Storage Units within a subsystem.

Fastrand search operations cause the contents of a specified drum position to be searched until a bit-by-bit match is found to an Identifier Word stored in the controller. At this point a read operation is initiated. Alternative function codes permit searching every word or only the first word of each drum sector. The search operations make no demands upon the central processor or core storage until a "find" is made.

Longitudinal check characters and phase-monitoring circuits are used for error detection and correction, providing for the recovery of up to 11 bits of missed data. Other checks are made for invalid addresses, illegal function codes, timing conflicts, and sector length errors. Detection of any error causes the controller to initiate an external interrupt and send the central processor a Status Word indicating the type of error and (in some cases) the Fastrand location at which it occurred.

The Fastrand IA Mass Storage Subsystem originally announced for the UNIVAC 490 system differs from the present Fastrand II only in having 3,072 bands per drum instead of 6,144; thus, the data capacity of each Fastrand IA Storage Unit is half that of a Fastrand II Storage Unit.

.14 Availability: . . . . . 9 months.

.15 First Delivery: . . . 2nd quarter 1964.

.16 Reserved Storage: . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . drums.

.22 Physical Dimensions

.222 Drum —

Diameter:	23.8 inches.
Length:	61.2 inches, effective.
Number on shaft: . .	1.
Number per Storage Unit	2.

.23 Storage Phenomenon: magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . yes.

.242 Data regenerated constantly: . . . . . no.

.243 Data volatile: . . . . . no.

.244 Data permanent: . . . no.

.245 Storage changeable: . no.

.25 Data Volume per Band of 1 Track

Words:	2,112.
Characters:	10,560.
Digits:	18,374.
Instructions:	2,112.
Sectors:	64 (33 words each).
Address tags:	1 (48 bits).

.26 Bands per Physical Unit: . . . . . 6,144 per drum. 12,288 per Storage Unit.

.27 Interleaving Levels: . 1, 3, 7, or 9 (optional; must be selected before delivery).

.28 Access Techniques

.281 Recording method: . . 64 moving heads per Storage Unit, connected to a common positioning mechanism.

.283 Type of access —

Description of stage	Possible starting stage
Move heads to specified position:	when a different position is selected.
Wait for specified sector:	when previously selected position is used.
Read or write 1 to 32,767 words: .	when rotational delay is zero.

.29 Potential Transfer Rates

.291 Peak bit rates —

Cycling rates:	870 rpm.
Track/head speed: .	1,086 inches/sec.
Bits/inch/track: . .	1,000.
Bit rate per track: .	1,086,000 bits/sec/track.

.292 Peak data rates —

Unit of data:	word.
Conversion factor: .	30 bits per word.
Gain factor:	1 track per band.
Loss factor:	3, 7, or 9 interleaving levels.

Date rate:

Interlace option	Words/sec	Characters/sec
1	25,150	125,750
3	8,383	41,915
7	3,592	18,060
9	2,794	13,970

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . . see Table I.

.32 Rules for Combining Modules: . . . . . 1 to 8 Storage Units per Fastrand Subsystem. Each subsystem fully occupies 1 input-output channel.

(Contd.)

.4 CONTROLLER

.41 Identity: . . . . . Fastrand Control and Synchronizer.
Type 5009-08: single channel.
Type 5009-09: dual channel.

.42 Connection to System

.421 On-Line: . . . . . 1 to 24 controllers (see Table I); 1 per Fastrand Subsystem.

.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . 1 to 8 Fastrand Storage Units.

.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 32,767 words, beginning with the first word of a drum sector; 1 to 4,096 words in UNIVAC 494 systems.

.442 Input-output area: . Core Memory.

.443 Input-output area access: . . . . . each word.

.444 Input-output area lockout: . . . . . none.

.445 Synchronization: . . automatic.

.447 Table control: . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —
Stacks per Fastrand Subsystem: . . . . 64 to 512.
Stacks per storage unit: . . . . . 64.
Stacks per drum: . 32.
Stacks per yoke: . 64.
Yokes per storage unit: . . . . . 1.

.512 Stack movement: . . . all 64 stacks in a Storage Unit move in unison, to 1 of 192 discrete positions.

.513 Stacks that can access any particular location: . . . . . 1.

.514 Accessible locations —
By single stack —
With no movement: 64 sectors.
With all movement: 12,288 sectors.
By all stacks —
With no movement: 4,096 sectors per storage unit.
up to 32,768 sectors per subsystem.

.515 Relationship between stacks and locations: bits 6-11 of Function Word designate head address.

.52 Simultaneous Operations: . . . . . maximum of 1 data transfer or search operation per Fastrand Subsystem, and 1 head-positioning operation per Fastrand Storage Unit.

.53 Access Time Parameters and Variations

Stage	Variation, msec	Average, msec
Activate addressing circuits:	5.0*	*
Position heads:	0 or 30.0 to 86.0	58.0
Wait for specified sector:	0 to 69.0	35.0
Read or write:	See Paragraph .292	
Total:	5.0 to 155.0	93.0

* Usually overlapped with other timing factors.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With Core Memory: . 1 to 32,767 words, beginning with the first word of a drum sector; 1 to 4,096 words in UNIVAC 494 systems.

.73 Effective Transfer Rate

With Core Memory —

Interlace option	Words/sec	Characters/sec
3	10,060	50,300.
7	4,300	21,500.
9	3,360	16,800.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Invalid function code:	check	interrupt.
Recording of data:	record check character	
Recovery of data:	check character and phase monitoring	interrupt.
Timing conflicts:	check	interrupt.
Physical record missing:	check	interrupt.
Reference to locked area:	check	interrupt.
Sector length error:	check	interrupt.
End of position reached:	check	interrupt.

Note: The type of error is indicated by bits 24-29 of the Status Word, sent to the central processor when the interrupt occurs.

CENTRAL PROCESSORS

The UNIVAC 490 Series currently includes four Central Processor models: the 490, 491, 492, and 494. Although there is a great deal of similarity among the four models, there are also some significant differences, including variations in:

- Memory cycle times and instruction execution speeds.
- Instruction repertoires.
- Number of input-output channels.
- Storage protection and multiprogramming facilities.
- Checking of internal operations.

The characteristics of the 490 Series Central Processors are summarized and compared in Table I of the Introduction to this Computer System Report, Section 800:011.

Each of the UNIVAC 490 Series Central Processors is discussed in detail in the appropriate Computer System Subreport, which also provides performance details. These reports on the individual processor models can be found on the following pages:

CONSOLE

.1 GENERAL

.11 Identity: . . . . . Control Console.
Maintenance Panel.

.12 Associated Units: . . . Keyboard and Printer.

.13 Description

The Control Console is the operating center of the UNIVAC 490 Series computer systems. It consists of an alphanumeric keyboard, a character-at-a-time printer, and a control panel in a console desk 54 inches wide by 35 inches deep. The keyboard and printer permit direct two-way communication between the operator and the stored computer program. The control panel contains displays that show the status of the program in progress and switches that provide manual control. The Control Console is designed for normal system operations only; the controls and register displays used primarily in maintenance operations are located on the Central Processor Maintenance Panel (described at the end of this section). The Control Console is connected to one of the UNIVAC 490 system's input-output channels.

Lamps are provided to indicate conditions such as excessive temperature, illegal function code, Day Clock or Delta Clock fault, and program stop. The Day Clock display shows the time of day, in hours, minutes, and seconds, by means of a six-decimal-digit display. Switch indicators permit the operator to set the three Jump Switches, halt program execution, start program execution at location 0000, lock out the Console Keyboard, and disconnect the Console Printer.

The Keyboard is a standard 4-bank typewriter keyboard that can generate the 64 basic Fieldata character codes. The Console Printer is the Teletype Model 28 Page Printer, which prints 1 character at a time at a peak speed of 10 characters per second. It can print the 26 letters, 10 numerals, and 19 special symbols of the Fieldata character code, and responds to the remaining 9 control codes (space, line feed, etc.). Output is on paper from a continuous roll, 8.50 inches wide and up to 5 inches in diameter.

The Maintenance Panel on the Central Processor contains other controls and displays which are used in debugging and maintenance operations. Binary displays of the contents of the following Central Processor registers are provided: A, B1 through B7, C0, C1, P, Q, R, R' S, U, X, and Z. Functions of the Maintenance Panel controls include:

- Execution of either one program step or one clock phase (one-fourth of a cycle) each time a switch is depressed.
- Disconnection of the Real-Time Clock, the Incremental Clock, and the Automatic Recovery feature.
- Normal execution of all instructions except programmed "stop" instructions, which are ignored.

INPUT-OUTPUT: CARD READER

.1 GENERAL

.11 Identity: . . . . . Type 0706-00 Card Reader.

.12 Description

The Type 0706 Card Reader reads standard 80-column cards at the rate of 900 cards per minute, provided that the information to be read is punched in the first 72 card columns. If the entire 80 columns must be read, the reading rate drops to 800 cards per minute. The capability to read 90-column cards is available in another version of the Type 0706 Card Reader.

One card reader and/or one card punch can be connected to a Card Control and Synchronizer Unit, forming a Punched Card Subsystem. Each Punched Card Subsystem fully occupies one 490 Series input-output channel. The card reader and punch units within any subsystem can operate concurrently by sharing their access demands on Core Memory. (The UNIVAC 1004, described in Section 800:102, can serve as an alternative punched card input device for 490 Series systems.)

Significant among the characteristics of the Type 0706 Card Reader are the following:

- A 3,000-card input hopper.
- A 2,500-card output stacker.
- Photodiode punch-sensing with automatic checking of the sensory elements before each card is read.
- An "infinite clutch" to provide immediate initiation of card feeding on demand.
- Binary card-image reading.
- Automatic translation from Hollerith card code to the 6-bit 490 Series internal code when reading in the translate mode. The Channel Synchronizer assembles the 6-bit codes into 30-bit computer words.
- Generation of an interrupt signal upon successful completion of a read operation and upon detection of an error condition or a unit not-ready condition. The read-complete interrupt can be inhibited by the program.
- Setting of testable indicators upon detection of registration check errors, parity errors, sensing element errors, unit busy, and unit not ready (off-normal) conditions.

Card images can be transferred to Core Memory without translation in either the column binary or row binary mode. In the column binary mode, the bit pattern of each group of five consecutive card columns fills two computer words. In the row binary mode, the bit pattern of each card row fills two consecutive computer words and the 20 high-order bit positions of a third word.

The ability to initiate a card read operation at any time (due to the infinite clutch) and the relatively small demands made on the central processor during card input operations (see Section 800:111, Simultaneous Operations) should permit maximum-rate reading speeds to be maintained in most applications.

INPUT-OUTPUT: CARD PUNCH

.1 GENERAL

.11 Identity: . . . . . Type 0600 Card Punch.

.12 Description

The Type 0600 Card Punch punches and verifies standard 80-column cards at a peak speed of 300 cards per minute. One card punch and/or one card reader can be connected to a Card Control and Synchronizer unit, forming a Punched Card Subsystem. Each subsystem fully occupies one 490 Series input-output channel. The reader and punch in each subsystem can operate concurrently by sharing their access demands on Core Memory. A unit capable of punching 90-column cards is also available. (The UNIVAC 1004, described in Section 800:102, can serve as an alternative punched card output device for 490 Series systems.)

Among the significant characteristics of the Type 0600 card punch are the following:

- A 1,000-card input hopper.
- Two 1,000-card output stackers.
- Four separate card transport stations (2 wait stations, followed by the punch station and the Post Punch Check station).
- A single-access-point clutch.
- Binary card image punching (a maximum of 240 holes can be punched per card).
- Automatic translation from the 6-bit 490 Series internal code to Hollerith card code (only in the 80-column card punch models). The Channel Synchronizer disassembles each 30-bit computer word into five 6-bit characters and transmits them to buffer storage in the Card Control Unit. Each 6-bit character is then translated into one Hollerith-coded character.
- Post-punch hole-count checking.
- Generation of an interrupt signal upon successful completion of the card punch operation, and upon encountering an error condition or a unit not-ready condition. The read-complete signal can be inhibited by the program.
- Setting of testable indicators upon detection of parity errors, hole-count errors, and unit busy and unit not-ready conditions.

INPUT-OUTPUT: PAPER TAPE SUBSYSTEM

.1 GENERAL

.11 Identity: . . . . . Punched Paper Tape Subsystem.

.12 Description

The UNIVAC 490 Paper Tape Subsystem consists of a modified, bidirectional Digitronics B 3500 reader, a Teletype BRPE-11 high-speed punch, and associated controllers. The unit can read and punch 5, 6, 7, or 8-channel paper tape, according to operator specification. The maximum tape reading rate is 400 characters per second, and the maximum tape punching speed is 110 characters per second. Code translation is performed under program control.

For each punched character, channels 0 through 6 can be used for either data or control purposes. If the character is accompanied by an External Function Signal, the bits are assumed to provide control information. The eighth bit of each character is used exclusively for control purposes. The control information that can be provided by the eight bits of a character include the following:

Bit 0: . . . . . Read Forward
Bit 1: . . . . . Read Reverse
Bit 2: . . . . . Fault
Bit 3: . . . . . Master Clear
Bit 4: . . . . . Punch On
Bit 5: . . . . . Reader On
Bit 6: . . . . . Compare Error Clear
Bit 7: . . . . . Punch Off
Bit 8: . . . . . Reader Off.

The faults that can be sensed by the paper tape controller include:

- Unequal comparison between the punched information and the contents of the punch register.
- Tape exhausted conditions in either reader or punch.
- Lateral motion of the paper in either reader or punch.

Paper tape reading is performed photoelectrically by silicon photo-diodes. The width of the tape can be either 11/16, 7/8, or 1 inch. The tape sprocket holes, used for timing purposes, are arranged in-line, ten to an inch.

The Paper Tape Subsystem does not include a Channel Synchronizer for the assembly of characters into 490 Series words. Therefore, the Paper Tape Subsystem and the central processor must communicate directly, one character at a time. The eight-bit character codes are transferred to and from the eight low-order bit positions of consecutive core storage word locations. No automatic code translation or parity checking is provided.

INPUT-OUTPUT: PRINTER

.1 GENERAL

.11 Identity: . . . . . High-Speed Printer. Types 0751, 0755, 8121.

.12 Description

The High-Speed Printer Subsystem consists of a Channel Synchronizer/Control Unit and a high-speed printer. One output channel is required for each printer. The power supply of one subsystem can be shared by a second High-Speed Printer Subsystem. The maximum printing speed of each printer is 700 alphanumeric or 922 numeric 132-character lines per minute. Up to 63 different characters can be printed; the character set consists of the 26 upper-case alphabetics, the 10 numerics, and 27 punctuation marks and other special symbols (illustrated in Table I). The 64th character code is the space or blank.

The 63 printable characters for each position are arranged in a checkerboard pattern on the print drum. This staggered arrangement is used to obtain "ghost-free" print quality. ("Ghosting", or printing characters with the hint of a double image, is often caused by characters being horizontally aligned too closely on the drum.) The printed lines can be spaced vertically at either 6 or 8 lines per inch by a manual control. Horizontal spacing is 10 characters per inch.

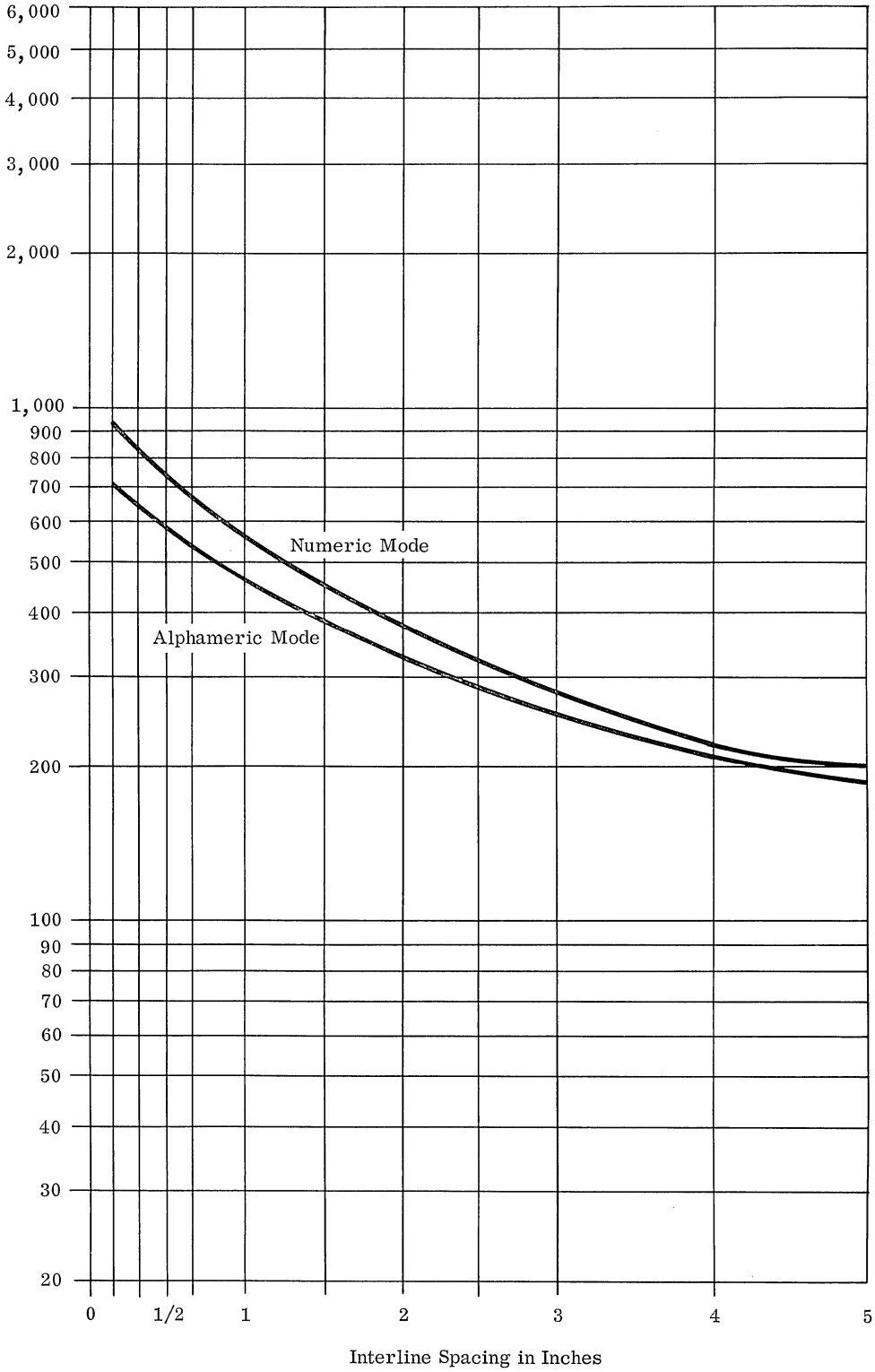
Paper can be advanced at 20 inches per second, under program control. There is no format control tape to facilitate the control of vertical spacing. The forms used can range from 2.75 to 21.5 inches in width, although use of the 21.5-inch width restricts the printable portion of the form to the center 13.2 inches. Up to 5 carbons plus the original copy, having a combined thickness of 15.5 mils, are acceptable. A maximum of 1.5 million lines can be printed between ribbon changes.

Controls provided allow an operator to adjust the forms up to one full character position, either horizontally or vertically, during printer operation. The indicators provide information on the following conditions: power fault, power runaway, ribbon exhausted, interlock(s) open, overheating, paper exhausted, and print carriage out.

TABLE I. STANDARD CHARACTER SET

Character	Printed Symbol	Character	Printed Symbol
Close Bracket	]	At the Rate of	@
Minus or Hyphen	-	Asterisk	*
Zero	0	Dollar Sign	$
One	1	Exclamation Mark	!
Two	2	J	J
Three	3	K	K
Four	4	L	L
Five	5	M	M
Six	6	N	N
Seven	7	O	O
Eight	8	P	P
Nine	9	Q	Q
Left Oblique	\	R	R
Semicolon	;	Percent	%
Open Bracket	[	Apostrophe	'
Plus	+	Delta	Δ
Colon	:	Not Equal	≠
Period	.	Open Parenthesis	(
Question Mark	?	Comma	,
A	A	Ampersand	&
B	B	Slash	/
C	C	S	S
D	D	T	T
E	E	U	U
F	F	V	V
G	G	W	W
H	H	X	X
I	I	Y	Y
Equal	=	Z	Z
Less	<	Close Parenthesis	)
Number	#	Greater	>
		Lozenge	⌑

EFFECTIVE SPEED: UNIVAC HIGH-SPEED PRINTER



INPUT-OUTPUT: UNISERVO VIC AND VIIIC TAPE UNITS

.1 GENERAL

.11 Identity: . . . . . Uniservo VIC Magnetic Tape Handler. Types 0858-00, -01, -08.

Uniservo VIIIC Magnetic Tape Handler. Types 0859-00, -02.

.12 Description

The Uniservo VIC and VIIIC Tape Handlers are 7-channel, "industry-compatible" units that offer data transfer rates ranging from 8.5 to 96 thousand characters per second. Their performance characteristics are summarized in Table I. Both units can optionally be modified at the factory to provide 9-channel recording capability for compatibility with the IBM 2400 Series tape units used with the System/360. Tape reading can be performed in either the forward or backward direction.

The Uniservo VIC Magnetic Tape Subsystem consists of a single-channel or dual-channel Control and Synchronizer, from 1 to 4 master units, and from 1 to 12 slave units. Each master unit contains the power supply for itself and up to three slave units. The Uniservo VIIIC Subsystem also offers the choice of a single-channel or dual-channel control, but provides in addition a separate power supply for each of the one to sixteen tape units that it can control. Each dual-channel control requires the use of two input-output channels to allow simultaneous read/write operations.

The economy-priced Uniservo VIC tape units provide data transfer rates of 8.5, 24, or 34KC; the Uniservo VIIIC tape units can transfer data at 24, 66.7, or 96KC, depending upon the recording density in use. Both models provide a choice of three recording densities: 200, 556, or 800 rows per inch. Each tape row consists of six data bits and one parity bit. The nine-channel recording option permits eight data bits and one parity bit to be recorded in each row. Block length is variable from one word to the capacity of core storage.

The External Function instruction specifies a read or write operation, the unit involved, the recording density, and whether or not an external interrupt shall occur upon successful completion of the operation. The size of a tape block is indicated by the initial and final addresses in the Buffer Control Words. Error conditions are indicated by an interrupt. The central processor can then determine the type of error by testing the contents of the input-output Status word.

.13 Availability: . . . . . 9 months.

.14 First Delivery: . . . . . January 1965.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . vacuum capstan.
.212 Reservoirs —
Number: . . . . . 2.
Form: . . . . . vacuum columns.
Capacity: . . . . . approximately 2 feet of tape in the Uniservo VIC and 5 feet in the VIIIC.
.213 Feed drive: . . . . . electric motor.
.214 Take-up drive: . . . . . electric motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.
.222 Sensing system: . . . . . magnetic head.
.223 Common system: . . . . 2-gap head provides read-after-write checking.

TABLE I: CHARACTERISTICS OF THE UNISERVO VIC AND VIIIC MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, chars per sec	Interblock Gap Lengths			Efficiency, % (3)		Demand on Core Storage	Full Rewind Time, minutes
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks		
VIC	42.7	200	8,500	0.75	17.5	150	40	87	(4)	3.0
		556	23,700	0.75	17.5	417	19	70	(4)	3.0
		800	34,100	0.75	17.5	600	14	62	(4)	3.0
VIIIC	120.0	200	24,000	0.75	6	150	40	87	(4)	1.3
		556	66,720	0.75	6	417	19	70	(4)	1.3
		800	96,000	0.75	6	600	14	62	(4)	1.3

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.
(4) Two memory cycles per word are required; memory cycle time for the UNIVAC 491/492 is 4.8 microseconds, while memory cycle time for the UNIVAC 494 is 0.75 microsecond.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase or write.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7 (or optionally 9).
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . read.
Distance: . . . . . 0.25 inch after write head.
Stacks: . . . . . 1.
Heads/stack: . . . . . 7 (or optionally 9).
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . plastic tape with magnetizable surface.
.312 Phenomenon: . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . . 5 to N rows, at 200, 556, or 800 rows per inch; N limited by available core storage or UNIVAC 494 Buffer Control Word.
.322 Parallel by: . . . . . 7 tracks, standard. 9 tracks, with optional feature.

.324 Track use:

Standard mode —
Data: . . . . . 6.
Redundancy check: . 1 (parity).
Timing: . . . . . 0 (self-clocking).
Unused: . . . . . 0.
Total: . . . . . 7.

With optional Nine-Track feature —
Data: . . . . . 8.
Redundancy check: . 1.
Timing: . . . . . 0 (self-clocking).
Unused: . . . . . 0.
Total: . . . . . 9.

.325 Row use —
Data: . . . . . 5 to N.
Redundancy check: .. 1.
Timing: . . . . . 0.
Control signals: . . . 0.
Unused: . . . . . 0.
Gap: . . . . . 0.75 inch.

.33 Coding: . . . . . binary word image, using 5 tape rows per 490 Series word and odd parity; or BCD mode, using IBM 6-bit character codes and even parity.

.34 Format Compatibility: . . . . . with IBM 727, 729, and 7330 Magnetic Tape Units; with IBM 2400 Series tape units when 9-track option is used; with UNIVAC systems using Uniservo IIIC, IVC, or VIC tape handlers; and with other manufacturers' "IBM compatible" tape units.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.5 inch.
.352 Length: . . . . . 2400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . . Uniservo VIC Control and Synchronizer (Type 5008-04, single-channel).

Uniservo VIC Auxiliary Control and Synchronizer (Type 5008-05, dual-channel).

Uniservo VIIIC Control and Synchronizer (Type 5008-16, single-channel).

Uniservo VIIIC Auxiliary Control and Synchronizer (Type 5008-17, dual-channel).

.42 Connection to System

.421 On-line: . . . . . maximum number of subsystems ranges from 3 (dual-channel, UNIVAC 491) to 24 (single-channel, UNIVAC 494).
.422 Off-line: . . . . . none.

.43 Connection to Device

.431 Devices per controller: 1 to 16 tape units.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 4,096 30-bit words.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . each 30-bit word.
.444 Input-output area lockout: . . . . . the 491 and 492 provide memory protection in 1,024-word blocks; the 494 provides memory protection in 64-word blocks.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to 4,096 30-bit words, limited by the 12-bit size counter in the Buffer Control Word.

.512 Block demarcation —
Input: . . . . . inter-block gap on tape, or word count in Buffer Control Word.
Output: . . . . . word count in Buffer Control Word.

(Contd.)

.52 Input-Output Operations

.521 Input: . . . . . read 1 block of data forward or reverse at 200, 556, or 800 rows per inch in either binary mode (odd parity) or BCD mode (even parity); external interrupt upon completion of operation is optional.

.522 Output: . . . . . write 1 block of data forward at 200, 556, or 800 rows per inch in either binary or BCD mode; external interrupt upon completion of operation is optional.

.523 Stepping: . . . . . 1 block backward (backspace); approximately 4 inches forward (to skip and erase defective tape areas).

.524 Skipping: . . . . . backspace to an end-of-file mark or to load point of tape.

.525 Marking: . . . . . end-of-file mark, interblock gap.

.526 Searching: . . . . . read first word of each block and compare it with identifier word; when a match occurs, read the block as in Paragraph .521.

.53 Code Translation: . . . none; binary images of data in internal storage are recorded on tape in either odd parity (binary mode) or even parity (BCD mode).

.54 Format Control: . . . . by program.

.55 Control Operations

Disable: . . . . . yes (follow rewind with interlock).
Request interrupt: . . . yes.
Select format: . . . . . yes; binary or BCD.
Rewind: . . . . . yes.
Unload: . . . . . no.

.56 Testable Conditions

Disabled: . . . . . yes.
Busy device: . . . . . yes.
Output lock: . . . . . yes.
Nearly exhausted: . . . no.
Busy controller: . . . . yes.
End of medium marks: yes.
End of file: . . . . . yes.
Rewinding: . . . . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . standard operation of Uniservo VIC and VIIIC tape units.

.62 Speeds

.621 Nominal or peak speed: see Table I.
.622 Important parameters: see Table I.
.623 Overhead: . . . . . see Table I.
.624 Effective speeds: . . . . see Table I and graphs.

.63 Demands on System: . . see Table I.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . none.

.72 Other Controls

Function	Form	Comment
Rewind:	switch/light	rewinds and positions tape.
Forward:	switch/light	moves tape forward.
Backward:	switch/light	moves tape backward.
Change tape:	switch/light	moves tape to load position

.73 Loading and Unloading

.731 Volumes handled: . . . . 2,400 feet per reel. For 1,000-character blocks: 5.0 million characters at 200 char/inch; 11.3 million characters at 556 char/inch; 14.4 million characters at 800 char/inch.

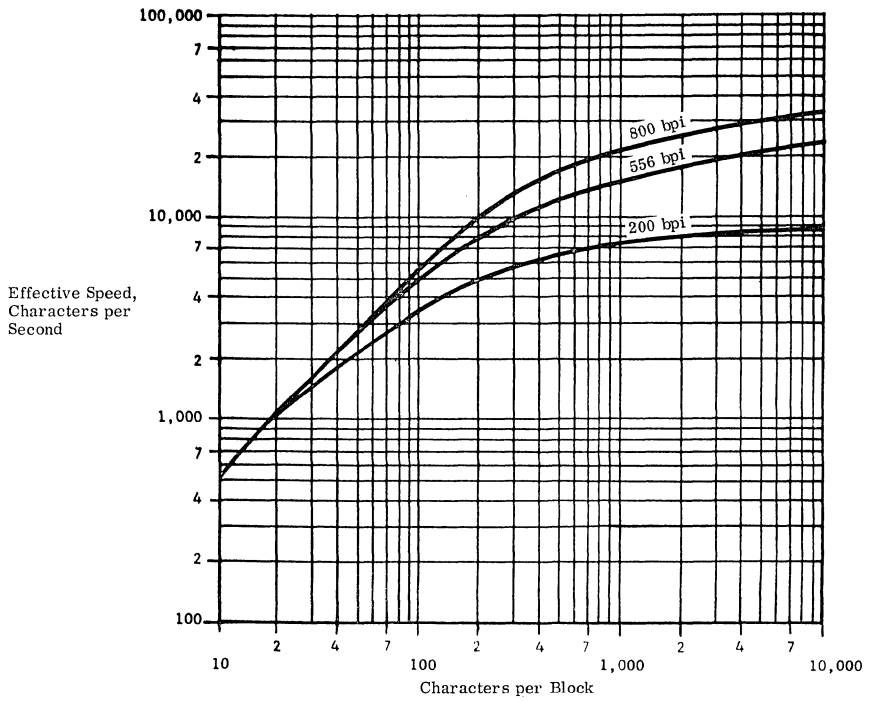
.732 Replenishment time: . . 0.5 to 1.0 minutes.

.734 Optimum reloading period —
Uniservo VIC: . . . . . 11.2 minutes.
Uniservo VIIIC: . . . . 4 minutes.

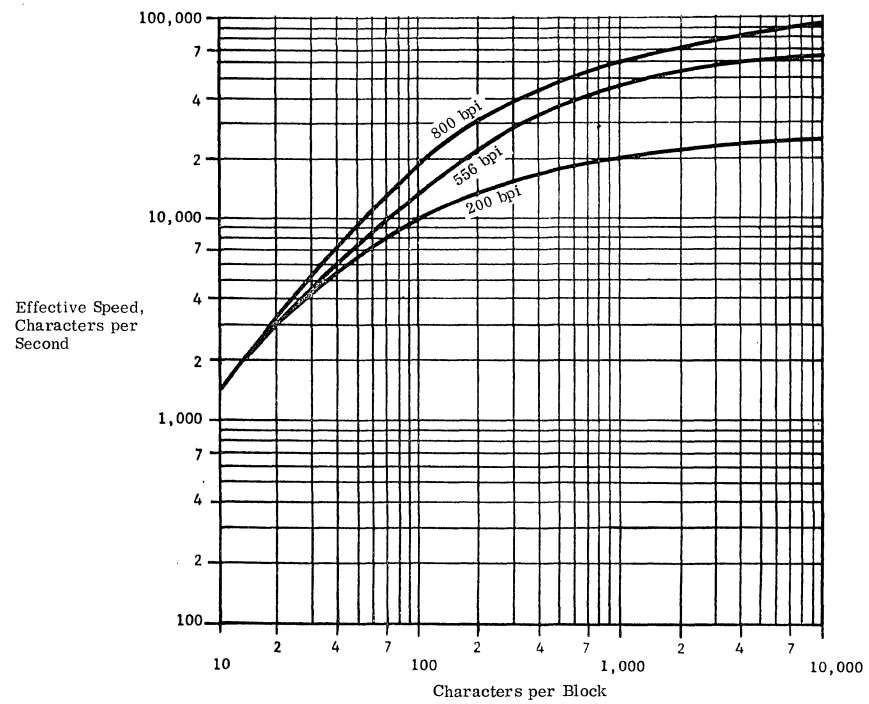
.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Recording:	read-after-write parity check	set indicator and interrupt.
Reading:	lateral and longitudinal parity check	set indicator and interrupt.
Invalid code:	all codes are valid.	
Exhausted medium:	check	set indicator and interrupt.
Imperfect medium:	read-after-write parity check	set indicator and interrupt.
Timing conflicts:	check	set indicator and interrupt.

Effective Speed:
Uniservo VIC Tape Units



Effective Speed:
Uniservo VIIIC Tape Units



INPUT-OUTPUT: UNISERVO IIA TAPE UNITS

.1 GENERAL

.11 Identity: . . . . . Uniservo IIA Magnetic Tape Handler. Type 8143.

.12 Description

The Uniservo IIA Magnetic Tape Handlers that were originally offered with the UNIVAC 490 are also available for use with the newer members of the 490 Series as "compatibility systems." The costly burden of reprogramming tape operations and converting a magnetic tape inventory can thereby be eliminated for users of UNIVAC systems dating back to the UNIVAC I.

The Uniservo IIA Subsystem consists of from 2 to 12 Uniservo IIA Tape Handlers connected to a Uniservo IIA Control and Synchronizer Unit and a Power Supply. Only one tape handler per subsystem can read or write at a time. A panel of dial switches is used to change the logical unit designations assigned to the individual tape handlers.

Data can be recorded on either plastic-base or metallic tape at a packing density of 125 or 250 rows per inch. (Data recorded by the Unityper keyboard-to-magnetic-tape transcriber at 50 rows per inch can be read, but the Uniservo IIA cannot record at this density.) Tape velocity is 100 inches per second, providing a peak data transfer rate of 12,500 or 25,000 characters per second, depending upon the recording density selected. Each tape row contains six data bits, one clock bit, and one parity bit, and can represent one alphameric character. Five tape rows are used to represent each 30-bit 490 Series word. Block length is variable. Tape width and densities are compatible with those of the Uniservo II and IIA Tape Handlers used in the UNIVAC II, III, 1107, and Solid-State 80/90 systems. There is no tape compatibility with the Uniservo IIIA, VIC, or VIIIC Tape Handlers.

.6 PERFORMANCE

.62 Speeds

.621 Nominal or peak speed —
At 250 rows/inch:. . . 25,000 char/sec.
At 125 rows/inch:. . . 12,500 char/sec.

.622 Important parameters —
Recording density: . . 120 or 250 rows/inch.
Tape speed: . . . . . 100 inches/sec.
Rewind speed: . . . . . 100 inches/sec.
Interblock gap: . . . . 1.05 inches.
End-of-file gap:. . . . 4.50 inches.
Start time: . . . . . 5 msec.
Stop time:. . . . . 5 msec.

.623 Overhead, per block —
Start/stop mode: . . . 25.5 msec.
Continuous mode:. . . 10.5 msec.

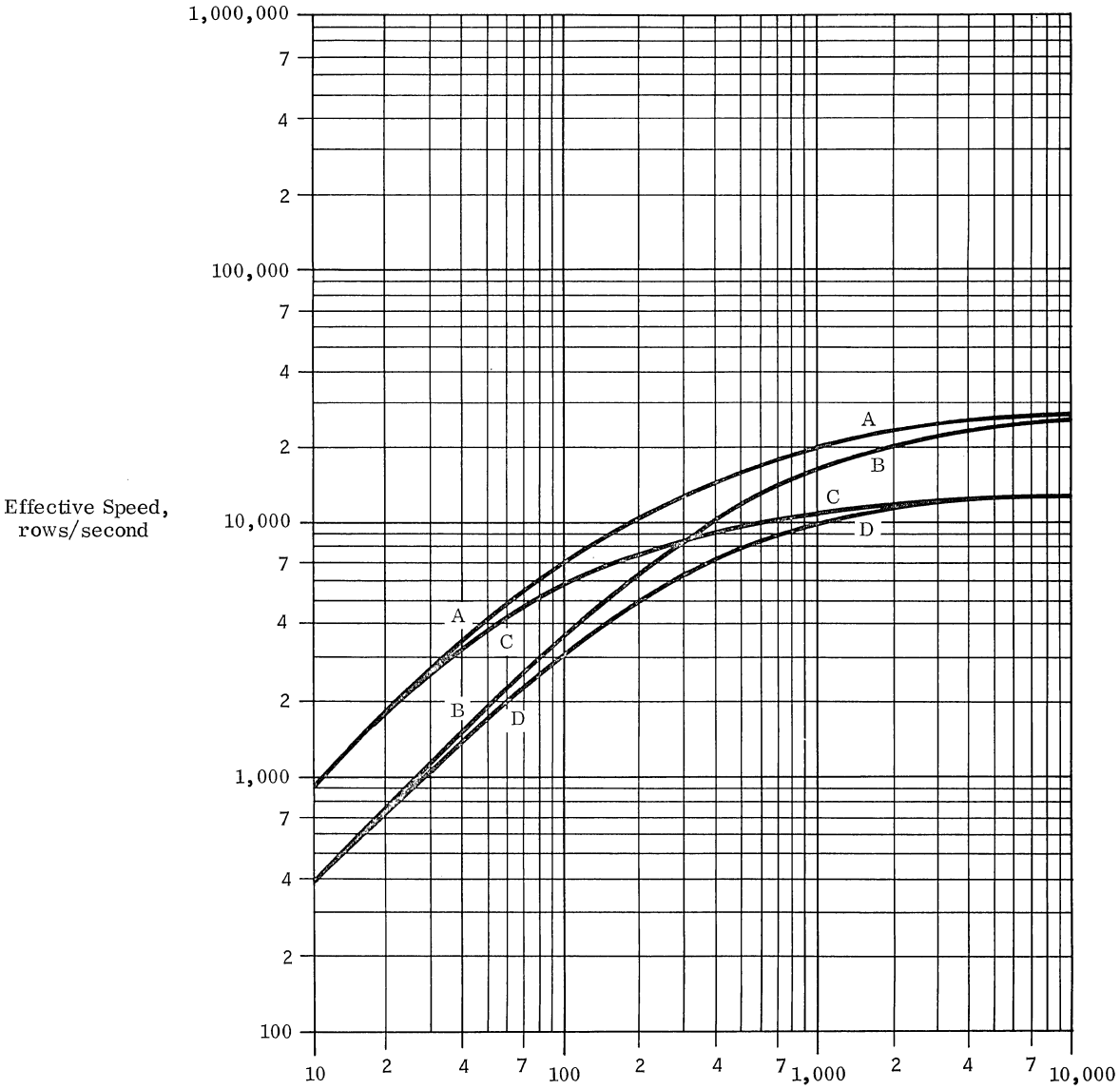
.624 Effective speeds —

250 Rows/Inch
Start/stop mode: . . 25,000N/ (N+ 638) char/sec.
Continuous mode:. . 25,000N/ (N+ 262) char/sec.

125 Rows/Inch
Start/stop mode: . . 12,500 N/ (N+ 319) char/sec.
Continuous mode:. . 12,500 N/ (N+ 131) char/sec. where N is the number of characters (i.e., tape rows) per block. (See graph.)

Note: The start/stop mode is used unless the next tape function is initiated within 4 msec after the last character of each block is read or written.

EFFECTIVE SPEED: UNISERVO IIA



Tape Rows Per Block

LEGEND

Curve A — 250 rows/inch, continuous mode
Curve B — 250 rows/inch, start/stop mode
Curve C — 125 rows/inch, continuous mode
Curve D — 125 rows/inch, start/stop mode

INPUT-OUTPUT: UNISERVO IIIA TAPE UNITS

.1 GENERAL

.11 Identity: . . . . . Uniservo IIIA Magnetic Tape Handler. Type 8011.

.12 Description

The Uniservo IIIA Magnetic Tape Handlers that were originally offered with the UNIVAC 490 are also available for use with the newer members of the 490 Series as "compatibility systems." The Uniservo IIIA, first delivered in March 1963, is currently the fastest tape unit available for use with the UNIVAC 490 Series, but it is not compatible with the tape units used with competitive computer systems. The Uniservo IIIA provides format compatibility only with other Uniservo IIIA units used with other UNIVAC computer systems, such as the 1107 and the 418.

From 2 to 16 Uniservo IIIA Tape Handlers can be connected to a Uniservo IIIA Control and Synchronizer Unit and a Uniservo Power Supply, forming a Uniservo IIIA Magnetic Tape Subsystem. Each subsystem fully occupies one input-output channel, and only one tape handler per subsystem can read or write at the same time.

Data is recorded by the "pulse phase" method at a density of 1,000 rows per inch. Nine tracks are recorded across the tape, and one is always used as a parity track. In the standard recording format, four tape rows are used to represent one 30-bit 490 Series word; the first three rows contain eight data bits each, and the last row of each four-row group contains only six data bits. An optional format, selected through plugboard switching, uses five tape rows per word, with only six data bits (i.e., one alphameric character) per row. Tape velocity is 100 inches per second, providing the following peak data transfer rates:

	Standard Format (4 rows per word)	Optional Format (5 rows per word)
Rows per second:	100,000	100,000
490 words per second:	25,000	20,000
6-bit characters per second:	125,000	100,000

.6 PERFORMANCE

.62 Speeds

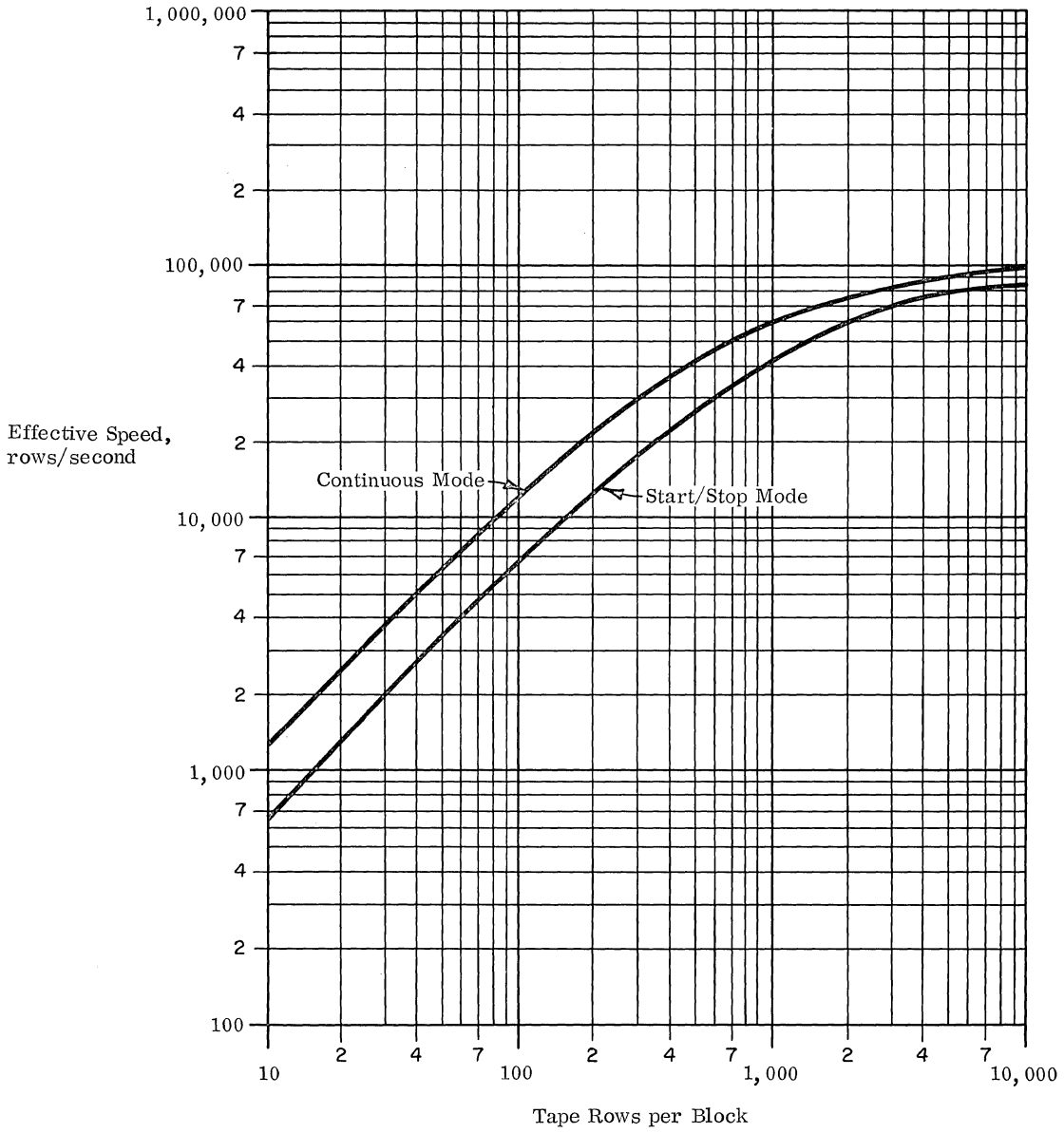
.621 Nominal or peak speeds —
Standard format (4 tape rows per word): . . . . . 25,000 words/sec or 125,000 alphameric characters/sec.
Optional format (5 tape rows per word): . . . . . 20,000 words/sec or 100,000 alphameric characters/sec.

.622 Important parameters —
Recording density: . . 1,000 rows/inch.
Tape speed: . . . . . 100 inches/sec.
Rewind speed: . . . . . 300 inches/sec.
Interblock gap: . . . . 0.75 inch.
Start time: . . . . . 3 msec.
Stop time: . . . . . 3 msec.

.623 Overhead per block: . . 7.5 msec per block.

.624 Effective speeds: . . . . 100,000N/(N+ 750) rows/sec, where N is number of rows per block. (See graph.)

EFFECTIVE SPEED: UNISERVO IIIA



Note: 4 or 5 tape rows per 5-character 490 word, depending upon recording format.

INPUT-OUTPUT: DATA COMMUNICATIONS SUBSYSTEMS

.1 GENERAL

.11 Identity: . . . . . Communication Terminal Module Controller (CTMC).
Channel Scanner/Selector.
Word Terminal Synchronous (WTS).
Communication Terminal Synchronous (CTS).

.12 Description

UNIVAC offers a standard line of data communications equipment for use with UNIVAC 418, 490 Series, or 1100 Series computer systems; different interfaces are provided for connection to the various computers. Included in this line are a multiline controller capable of handling up to 32 full-duplex narrow-band or voice-band lines, and two single-line controllers capable of handling one full-duplex voice-band or broad-band line.

.121 Multiline Controller

UNIVAC has recently changed the pricing policy and nomenclature for its Standard Communications Subsystem. The Communication Multiplexor is now called the Communication Terminal Module Controller (CTMC). Four Communication Line Terminals (CLT's) are now grouped into one Communication Terminal Module (CTM). The CLT-Parallel Input and Output and CLT Automatic Dialing terminals retain the same names. Savings of up to 50% in communications equipment costs can be realized in fully-expanded subsystems containing one CTMC when compared to the previous Standard Communications Subsystem prices.

Transmission adapters are available for handling a wide range of communications facilities; see Table I. The CTMC contains 32 input and 32 output positions. The number of positions required by each adapter is specified in Table I. The Communications Subsystem is physically contained in two cabinets; one contains the power supply and communication lines interfaces, and the other contains the multiplexor, the transmission adapters, and timing clocks. The second cabinet contains space for accommodating 16 modules. Each module consists of one of the following:

- One Low-Speed CTM,
- One Medium-Speed CTM,
- One High-Speed CTM,
- One to four CLT-Automatic Dialing Adapters, or
- One module containing up to two Parallel-Input Adapters and up to two Parallel-Output Adapters.

One CLT-Dialing is required for each line on which the automatic dialing function is desired.

An internal clock is required for some adapters; other adapters use external timing signals from the associated data set. A maximum of six output clocks can be included within the second cabinet. All output adapters operating at the same speed can utilize the same clock, but each input adapter has its own clock. Adapters within the same module can operate at different speeds.

Although each Communications Subsystem fully occupies the 490 Series input-output channel to which it is connected, up to four CTMC's can be connected to a single channel by means of a Scanner/Selector Unit. Thus, a maximum of 256 simplex lines or 128 half-duplex or full-duplex lines can be serviced by a single input/output channel.

A special communications feature, the Externally Specified Index (ESI), allows a number of communications lines to operate concurrently over a single input-output channel by providing automatic sorting of incoming data and automatic collation of outgoing data.

TABLE I: TRANSMISSION ADAPTER CHARACTERISTICS

Unit	Positions Required		Code Level (Bits/char)	Mode	Timing	Speed
	Input	Output				
Low-Speed CTM	2	2	5, 6, 7, or 8	Bit serial	Asynchronous; internal	Up to 300 bits/sec.
Medium-Speed CTM	2	2	5, 6, 7, or 8	Bit serial	Asynchronous; internal	Up to 1,600 bits/sec.
CLT-Parallel Input	1	0	Up to 8	Bit parallel	Timing signal, external	Up to 75 char/sec.
CLT-Parallel Output	0	1	Up to 8	Bit parallel	Timing signal, internal	Up to 75 char/sec.
High-Speed CTM	2	2	5, 6, 7, or 8	Bit serial	Synchronous; external	2,000 to over 5,000 bits/sec.
CLT-Dialing	0	1	4	Bit parallel	Timing signals; external	Determined by common carrier.

Note: "Asynchronous" means that start and stop bits are sent with each character to establish timing; "Synchronous" means that timing characters are sent with each message to establish timing.

.121 Multiline Controller (Contd.)

When the Communications Subsystem is used, two core storage locations are reserved for each communication line (one for input and one for output). These locations contain the Buffer Control Words. In addition, two alternating core storage buffer areas are assigned to each line. The size and locations of these buffer areas can be varied by the program.

A 15-bit code is transmitted along with each message character leaving or entering the Central Processor. This code, called the address ESI, identifies the Communication Line Terminal and Multiplexor. The ESI references a Buffer Control Word, which in turn indicates the location to or from which the character is to be sent. When a buffer has been filled (or emptied), an internal interrupt occurs, and the Buffer Control Words are modified by the operating system to reference the alternate buffer. Incoming data is stored in the upper halves of the words in the buffer area (one character per word), and outgoing data is stored in the lower halves (also one character per word). Thus, input and output buffer areas can be overlapped. Other arrangements are available on special request.

All Communication Line Terminals can be active simultaneously, subject to the maximum data rates of the computer and the CTMC. Messages can be transmitted or received while any other peripheral subsystem is operating and while the Central Processor is computing.

The maximum data rate of the CTMC is determined by the time required for scanning, the time required to transfer each character to the computer, and certain characteristics of the adapters. The resulting maximum allowable communications data rate for the CTMC, based on 8 bits per character (including start and stop bits, if any), for each of the various members of the 490 family, is as follows:

UNIVAC 490:. . . . . 19,000 char/sec.
UNIVAC 491/492:. . 22,500 char/sec.
UNIVAC 494:. . . . . 51,000 char/sec.

For other character codes, an approximate maximum character data rate can be obtained by multiplying the above figure by 8(N-1)/7N, where N is the total number of bits (including start and stop bits, if any) per character.

.122 Single-line Controllers

UNIVAC offers two single-line controllers, each of which is capable of controlling communications between a UNIVAC 490 Series computer and a remote terminal at 285 characters per second over the public telephone network, at 340 characters per second over a leased voice-band line, or at 5,800 characters per second over a leased broad-band facility such as Telpak A. These two controllers, the Word Terminal Synchronous (WTS) and the Communication Terminal Synchronous (CTS), are essentially two versions of the same unit. Both transmit data serially by bit in a synchronous mode, with a total of 7 bits per character. There are 6 data bits per character.

The WTS transfers data between the controller and the computer one word (5 characters) at a time and performs both character and message parity checking. The CTS transfers data to the computer one character at a time and performs only character parity checking. The WTS imposes a smaller demand upon the central processor than the CTS, but is also more expensive.

Both the WTS and the CTS can be equipped for unattended answering and automatic dialing (when connected to the public telephone network).

These controllers have been used to connect a variety of UNIVAC computers with remote UNIVAC 1004 Card Processors. Each controller fully occupies one input-output channel. The maximum demands on the central processor for communications at 340 characters per second are as follows:

	WTS	CTS
UNIVAC 490:.	0.07%	0.41%
UNIVAC 491/492:	0.05%	0.32%
UNIVAC 494:	0.01%	0.06%

The processor demands at other data transmission speeds are proportionate.

INPUT-OUTPUT: UNIVAC 1004

.1 GENERAL

.11 Identity: . . . . . UNIVAC 1004 Processor; Models I, II, and III. UNIVAC 1004 Adapter.

.12 Description

The UNIVAC 1004 is a small, plugboard-programmed computer with 961 or 1,922 character positions of core storage. It can be connected to a UNIVAC 490 Series computer system by means of the 1004 Adapter, enabling transmission of data, in one direction at a time, between 490 core storage and 1004 core storage. The 1004 can provide data editing, code translation, and similar data manipulation facilities independently of the 490 program. All operations must be initiated by the 490 program; i.e., the UNIVAC 1004 cannot act as an independent inquiry station for the 490 Series system. When it is not in use as an on-line peripheral subsystem for the 490, the UNIVAC 1004 can be used as an off-line data processor, under sole control of its plugboard wiring.

Some of the important characteristics of the 1004 are:

- Plugboard programming.
- 961 or 1,922 positions of core storage.
- 31, 47, or 62 program steps.
- 8 μsec cycle time for the 1004 Model I; 6.5 μsec cycle time for Models II and III.
- Editing and decimal arithmetic facilities.
- Maximum card reading rate of 400 or 615 cards/minute, depending upon the model.
- Maximum printing rate of 400 or 600 lines/minute, depending upon the model.
- 132 alphanumeric printing positions.
- 63-character printing set.
- Optional card punch — 200 cards/minute.
- Punched paper tape units available — 400 char/sec reading and 110 char/sec punching.
- One or two magnetic tape units can be connected: up to 33,664 characters per second at densities of 200, 556, or 800 characters per inch.

For more detailed information on the capabilities and performance of the UNIVAC 1004, see Computer System Report 770.

Data is transmitted one word at a time to or from the 490 systems. Except during interprocessor data transmission, the 1004 operates independently. The 1004 Subsystem requires one UNIVAC 490 Series input-output channel and can run simultaneously with all other peripheral devices.

SIMULTANEOUS OPERATIONS

1 INPUT-OUTPUT CHANNELS

The UNIVAC 490 Series Central Processors can contain 6, 12, 16, 20, or 24 general-purpose* input-output channels; the possiblities for each model are shown in Table I.

TABLE I: I/O CHANNEL POSSIBILITIES

Number of Channels*	6	12	16	20	24
UNIVAC 490	✓	✓			
UNIVAC 491	✓				
UNIVAC 492		✓			
UNIVAC 494		✓	✓	✓	✓

Each channel contains an input cable and an output cable, but data flow over the channel is, in most cases, limited to one direction at a time. Any one of the following peripheral subsystems can be connected to any one of the general-purpose channels via the appropriate Control and Synchronizer Unit (with exceptions as noted):

- FH-880 Magnetic Drum Subsystem: 1 to 8 drums (see Section 800:042).
- FH-432 Magnetic Drum Subsystem: 3 to 9 drums, on UNIVAC 494 only (see Section 800:043).
- FH-1782 Magnetic Drum Subsystem: 1 to 8 drums, on UNIVAC 494 only (see Section 800:044).
- Fastrand Mass Storage Subsystem: 1 to 8 storage units; Fastrand I on UNIVAC 490, Fastrand II on remainder (see Section 800:045).
- Uniservo IIA Magnetic Tape Subsystem: 2 to 12 tape units (see Section 800:092).
- Uniservo IIIA Magnetic Tape Subsystem: 2 to 16 tape units (see Section 800:093).
- Uniservo VIC Magnetic Tape Subsystem: up to 4 master units, each controlling up to 3 slave units; not available on UNIVAC 490 (see Section 800:091).
- Uniservo VIIIC Magnetic Tape Subsystem: up to 16 tape units; not available on UNIVAC 490 (see Section 800:091).
- High-Speed Printer Subsystem: 1 printer (see Section 800:081).
- Punched Card Subsystem: 1 reader and 1 punch (see Sections 800:071 and 800:072).
- Paper Tape Subsystem: 1 reader and 1 punch (see Section 800:075).
- Communication Terminal Module Controller (replaces the Standard Communication Subsystem for the UNIVAC 490; see Section 800:101).
- UNIVAC 1004 Processor (see Section 800:102).

* In addition to these general-purpose channels, each 490, 491, and 492 Processor includes two more channels which are reserved for computer-to-computer communications and for the console and clock. In the 494, one of the indicated channels serves both the console and the clock.

.2 CONTROL AND SYNCHRONIZER UNITS

The Control and Synchronizer Units provide the proper interfaces between the Central Computer and the peripheral units on each channel. During most output operations, the Synchronizer accepts 30-bit words from the computer and divides them into 6-bit character elements. During most input operations, the Synchronizer assembles 6-bit characters from the input device into 30-bit UNIVAC 490 words. The peripheral Control Unit, which is usually in the same cabinet as the Synchronizer, directs the selected input or output device while it performs the desired functions.

.3 SIMULTANEITY

In general, one data transfer operation at a time can occur on each input-output channel that has a peripheral subsystem connected to it. The exceptions to this general statement are as follows:

- The card reader and punch in a single Punched Card Subsystem can operate simultaneously by time-sharing their demands on the channel that services them.
- An optional Dual Channel Synchronizer can be used with all magnetic tape subsystems except the Uniservo IIA. With this option, the subsystem occupies two input-output channels and can simultaneously control either 1 read and 1 write or 2 read operations (but not 2 write operations).
- An optional Dual Channel Synchronizer can be used with Fastrand II. With this option, the subsystem occupies two input-output channels and can simultaneously control read and write operations.
- A magnetic tape or drum Control and Synchronizer Unit (and therefore the channel to which it is connected) is occupied throughout a search operation, even though no data is transferred to the Central Computer until the search has been successfully completed.
- When the Communications Subsystem is used, the channel to which it is connected can effectively be divided into several channels of

(Contd.)

.3 SIMULTANEITY (Contd.)

lower speed, each with its own core buffer area and interrupt control. Each Communication Line Terminal presents the address of its own particular buffer area to the Central Processor, permitting messages to or from several different communication lines to be transmitted concurrently under control of the Communication Controller.

.4 CONTROL OF I/O OPERATIONS

There is a Buffer Control Word in a fixed Core Memory location associated with each input and each output channel. Before an input or output operation is initiated, an "Activate Buffer" instruction must be used to initialize the appropriate Buffer Control Word. The Buffer Control Word in UNIVAC 490, 491, and 492 systems initially contains (in its low-order 15 bits and high-order 15 bits, respectively) the Core Memory addresses of the first and last words to be transferred. After each data word has been transferred to or from Core Memory, the lower half of the Buffer Control Word is automatically incremented by 1 and compared with the terminal address in the upper half. The updated Buffer Control Word is replaced in storage. If the comparison indicates that the data transmission has been completed, the operation is terminated and (optionally) an interrupt is initiated.

In the UNIVAC 494, the Buffer Control Word takes on a different form. Initially, the low-order 18 bits of the Buffer Control Word contained in the Buffer Control Register define the starting address of a buffer area. The 18 bits are required rather than 15 because of the 494's 131,072-word maximum storage capacity. The upper 12 bits are used to specify the number of core memory locations allocated to the buffer — a maximum of 4,096 words. As each data transfer between buffer and peripheral unit takes place, the 18-bit Current Address is increased by one and the 12-bit Address Count is decreased by one. When the Address Count reaches zero, the operation is terminated.

.5 MAXIMUM I/O DATA RATES

Each data word transferred to or from Core Memory requires two cycles of Central Processor time and one additional cycle of input-output logic time. When alternate input and output data transfers occur, the I/O logic cycles can be overlapped so that each one-word transfer can be accomplished within the 2-cycle time period. Table II shows the maximum total input-output rates, or "saturation rates," for the 490 Series Processors.

The consequences of attempting to exceed the maximum data transfer rates quoted above depend upon the particular peripheral subsystems involved and the priorities of the channels to which they are connected. (When there are simultaneous demands for access to Core Memory, the highest-numbered channel is served first.) The magnetic drum subsystems will attempt another data transfer during the next drum revolution, with no loss of data. The magnetic tape subsystems will generate a recoverable error condition, necessitating that the input or output operation be repeated. The probability of exceeding the maximum data transfer rate can be reduced by choosing one of the interlace options available for the Fastrand and Flying-Head magnetic drums, which reduce their effective transfer rates.

The combinations of simultaneous operations that can take place in a UNIVAC 490 Series system are limited by the number of input-output channels available, the data transfer rates of the individual devices compared with the gross input-output data rate of the Central Processor, and the amount of internal processing required. UNIVAC provides a program that tests a proposed configuration to determine all possible combinations of input-output operations that may exceed the allowable gross data transfer rates.

Figure 1 shows some of the combination possibilities in the various 490 Series systems. Horizontal lines on the chart show the maximum gross data transfer rates (input only) for the various UNIVAC 490 Series Processor Models. The vertical lines show the maximum data transfer rates of various input devices, with the effects of interlacing shown for the random-access storage devices.

TABLE II: MAXIMUM I/O DATA RATES

PROCESSOR MODEL	UNIVAC 490*	UNIVAC 491/492	UNIVAC 494
Maximum total transfer rate, input or output only —			
Words/second:	55,555	69,444	444,444
Characters/second:	277,775	347,220	2,222,220
Maximum number of instructions per second that can be executed concurrently with above I/O rate:	33,333	41,667	250,000
Maximum total transfer rate, input plus output —			
Words/second:	83,333	104,167	549,450
Characters/second:	416,665	520,833	2,747,250
Maximum number of instructions per second that can be executed concurrently with above I/O rate:	0	0	0

* With standard 6-μsec core memory.

.6 THE INPUT/OUTPUT CONTROLLER

The data rate capacities of UNIVAC 494 systems can be increased through use of the Input/Output Controller, an independent, wired-logic processor that provides:

- Independent data paths between peripheral subsystems and main core storage.
- High-speed communications capability.
- Enhanced system performance through chained buffer operations (a scatter/gather facility).
- The ability to expand the number of input-output channels available to the UNIVAC 494 system by from 4 to 16 additional channels.

The Input/Output Controller contains its own high-speed Index Memory for buffer control. The basic Index Memory provides 256 words, with an optional 256-word module providing expanded ESI (Externally-Specified Index) capabilities. Sixteen 5-bit Associative Registers are used to associate each I/O channel with a particular Index Memory location. In the Non-Chain mode of operation, a single Index Memory location is used to define the Buffer Control Word. In the alternative Chain mode, the Associative Register is used to indicate the first of a series of Buffer Control Words in Index Memory. Termination of an operation in the Chain mode is effected by recognition of an End-of-Chain code in Index Memory.

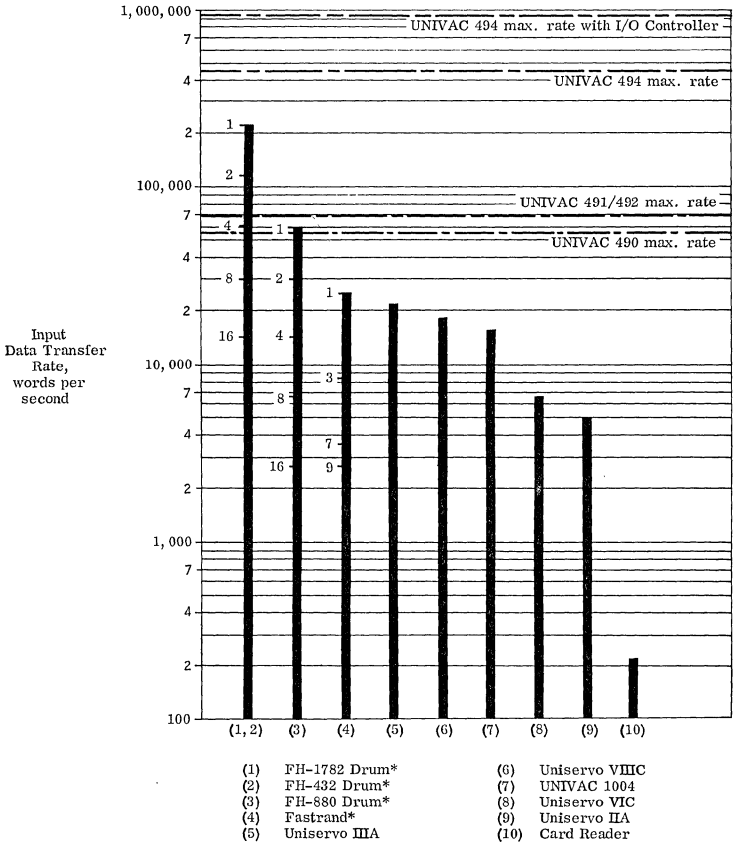


Figure 1: UNIVAC 490 Series Data Transfer Rates

INSTRUCTION LIST

Octal Code	Instruction	Description
00	Illegal	—
01	Right Shift Q	Shift Q right per Y
02	Right Shift A	Shift A right per Y
03	Right Shift A	Shift AQ right per Y
04	Compare A·Q·AQ	A:Y or Q:Y or AQ:Y
05	Left Shift Q	Shift Q left per Y
06	Left Shift A	Shift A left per Y
07	Left Shift AQ	Shift AQ left per Y
10	Enter Q	(Y) → Q
11	Enter A	(Y) → A
12	Enter B	(Y) → Bj
13	External Function	(Y) → C
14	Store Q	(Q) → Y
15	Store A	(A) → Y
16	Store B	(B)j → Y
17	Store C	(C) → Y
20	Add A	(A) + (Y) → A
21	Subtract A	(A) - (Y) → A
22	Multiply	(Q)·(Y) → AQ
23	Divide	(AQ)/(Y) → Q, R
24	Replace A+Y	(A) + (Y) → Y + A
25	Replace A-Y	(A) - (Y) → Y + A
26	Add Q	(Q) + (Y) → Q
27	Subtract Q	(Q) - (Y) → A
30	Enter Y + Q	(Y) + (Q) → A
31	Enter Y - Q	(Y) - (Q) → A
32	Store A + Q	(A) + (Q) → Y + A
33	Store A - Q	(A) - (Q) → Y + A
34	Replace Y + Q	(Y) + (Q) → Y + A
35	Replace Y - Q	(Y) - (Q) → Y + A
36	Replace Y + 1	(Y) + 1 → Y + A
37	Replace Y - 1	(Y) - 1 → Y + A
40	Enter LP (Logical Product)	L(Y)· (Q) → A
41	Add LP	L(Y) · (Q) + (A) → A
42	Subtract LP	A - L(Y)·(Q) → A
43	Compare Mask	(A) - L(Y)· (Q), sense j
44	Replace LP	L(Y)· (Q) → Y + A
45	Replace A + LP	L(Y) · (Q) + (A) → Y + A
46	Replace A - LP	(A) - L(Y) · (Q) → Y + A
47	Store LP	L(A) · (Q) → Y
50	Selective Set	Set (A)n for Yn = 1
51	Selective Complement	Complement (A)n for Yn = 1
52	Selective Clear	Clear (A)n for Yn = 1
53	Selective Substitute	(Y)n → (A)n for (Q)n = 1
54	Replace Selective Set	Set (A)n for (Y)n = 1 → Y + A
55	Replace Selective Complement	CP (A)n for (Y)n = 1 → Y + A
56	Replace Selective Clear	CL (A)n for (Y)n = 1 → Y + A
57	Replace Selective Substitute	(Y)n → An for (Q)n = 1 → Y
60	Jump — Arithmetic	(Y) → P
61	Jump — Manual	(Y) → P
62	Jump — C Active IN	If Cj active (Y) → P
63	Jump — C Active OUT	If Cj active (Y) → P
64	Return Jump — Arithmetic	(P+1) → Y, (Y+1) → P
65	Return Jump — Manual	(P+1) → Y, (Y+1) → P
66	Terminate C Input	Terminate Buffer
67	Terminate C Output	Terminate Buffer

Octal Code	Instruction	Description
70	Repeat	Repeat NI (Y) times
71	B Skip	If (B)j=Y, skip NI and CL (B)j; If (B)j≠Y, advance Bj and read NI
72	B Jump	If (B)j=0, read NI; if (B) j≠ 0, (B)j = (B)j-1 and jump to Y
73	Input C	Activate Buffer
74	Output C	Activate Buffer
75	Input C with Monitor	Activate Buffer
76	Output C with Monitor	Activate Buffer
77-00*	Illegal	—
77-01*	Floating Point Add	$(AQ)_{FP}+(Y,Y+1)_{FP} \rightarrow AQ_{FP}$
77-02*	Floating Point Subtract	$(AQ)_{FP}-(Y,Y+1)_{FP} \rightarrow AQ_{FP}$
77-03*	Floating Point Multiply	$(AQ)_{FP} \cdot (Y,Y+1)_{FP} \rightarrow AQ_{FP}$
77-05*	Floating Point Divide	$(AQ)_{FP} \div (Y,Y+1)_{FP} \rightarrow AQ_{FP}$
77-06*	Floating Point Pack	$(Y)_{EX} + (AQ)_{FXP} \rightarrow AQ_{FP}$
77-07*	Floating Point Unpack	$(AQ)_{FP} \rightarrow Y_{EX} + AQ_{FXP}$
77-10*	Decimal Test AQ	Skip per Y
77-11*	Decimal Add	$(AQ)_{D} + (Y,Y+1)_{D} \rightarrow AQ_{D}$
77-12*	Decimal Subtract	$(AQ)_{D} - (Y,Y+1)_{D} \rightarrow AQ_{D}$
77-13*	Decimal Compare	If $(AQ)_{D}=(Y,Y+1)_{D}$, Skip NI
77-14*	Decimal Complement AQ	$(AQ)_{D}' \rightarrow AQ_{D}$
77-15*	Decimal Add with Carry	$(AQ)_{D}+(Y,Y+1+C)_{D} \rightarrow AQ_{D}$
77-16*	Decimal Subtract with Carry	$(AQ)_{D}-(Y,Y+1+C)_{D} \rightarrow AQ_{D}$
77-17*	Decimal Compare Less	If $(AQ)_{D}<(Y,Y+1)_{D}$, skip NI
77-21*	Enter AQ Double Length	$(Y,Y+1) \rightarrow AQ$
77-22*	Double Precision Add	$(AQ) + (Y,Y+1) \rightarrow AQ$
77-23*	Compare AQ Equal	If (AQ)=(Y,Y+1), skip NI
77-24*	Complement AQ	$(AQ)' \rightarrow AQ$
77-25*	Double Length Store AQ	$(AQ) \rightarrow Y, Y+1$
77-26*	Double Precision Subtract	$(AQ)-(Y,Y+1) \rightarrow AQ$
77-27*	Compare AQ Less	If (AQ)<(Y,Y+1), skip NI
77-30*	Scale Factor Shift	Scale A, Count →Q
77-31*	Character Park Lower	$(Y, Y+1, Y+2, Y+3, Y+4)_{0-5} \rightarrow A$
77-32*	Character Park Upper	$(Y, Y+1, Y+2, Y+3, Y+4)_{15-20} \rightarrow A$
77-34*	Executive Return	Interrupt
77-35*	Character Unpark Lower	$(A) \rightarrow Y, Y+1, Y+2, Y+3, Y+4_{0-5}$
77-36*	Character Unpark Upper	$(A) \rightarrow Y, Y+1, Y+2, Y+3, Y+4_{15-20}$
77-37*	Execute Remote	(Y) →FØ, NI=P+1(Cond)
77-41*	Enter B1 and Jump	P→B1, Jump to Y

* All instructions that have a 77 operation code are available only with the UNIVAC 494 Central Processor.

(Contd.)

Octal Code	Instruction	Description
77-42*	Enter B2 and Jump	P →B2, Jump to Y
77-43*	Enter B3 and Jump	P →B3, Jump to Y
77-44*	Enter B4 and Jump	P →B4, Jump to Y
77-45*	Enter B5 and Jump	P →B5, Jump to Y
77-46*	Enter B6 and Jump	P →B6, Jump to Y
77-47*	Enter B7 and Jump	P →B7, Jump to Y
77-52*	Test and Set	INT if $2^{14} = 1$; NI if $2^{14} = 0$
77-53*	Masked Alphanumeric Compare	If AΘQ = YΘQ, Skip NI
77-57*	Masked Alphanumeric Compare	If AΘQ < YΘQ, Skip NI
77-61*	Enter Internal Function Register	(Y) →IFR
77-62*	Enter Program Lock-In Register	(Y) →PLR
77-65*	Store Internal Function Register	(IFR) → Y
77-66*	Enter Relative Index Register	(Y) →RIR
77-70*	Initiate Synchronous Interrupt	Send Interrupt
77-71*	Enter BW	(Y) →B1, (Y+1) →B2, (Y+2) →B3, (Y+3) →B4, (Y+4) →B5, (Y+5) →B6, (Y+6) →B7
77-72*	Store Channel Number	(I/O chan NO) →Y
77-73*	Enter Channel Select Register	(Y) →CSR
77-75*	Store BW	(B1) →Y, (B2) →Y+1, (B3) →Y+2, (B4) →Y+3, (B5) →Y+4, (B6) →Y+5, (B7) →Y+6

*All instructions that have a 77 operation code are available only with the UNIVAC 494 Central Processor.

INTERPRETATION OF SYMBOLS

A	A register
(A)	A register contents
Q	Q register
(Q)	Q register contents
AQ	the combined A and Q register
(AQ)	the combined A and Q register contents
Y	the address of an operand
(Y)	the contents of an operand address
B_j	B register contents
C	I/O Channel
n	variable bit count
P	P register contents
NI	next instruction
R	remainder
L or Θ	logical product
cl	clear
FP	Floating-point
D	Decimal
EX	Exponent
FXP	Fixed-point part
INT	interrupt
IFR	Internal Function Register
PLR	Program Lock-In Register
RIR	Relative Index Register
CSR	Channel Select Register

DATA CODE TABLE

FIELDATA	CHARACTER CODE		BAUDOT
	CONSOLE T/W	80 COL. CARD	
000000	(NO ACTION)	7-8	00000
000001	\	12-5-8	11011
000010	%	11-5-8	11111
000011	LINE FEED	12-7-8	00010
000100	CAR RET	11-7-8	01000
000101	SPACE	BLANK	00100
000110	A	12-1	L00011
000111	B	12-2	L11001
001000	C	12-3	L01110
001001	D	12-4	L01001
001010	E	12-5	L00001
001011	F	12-6	L01101
001100	G	12-7	L11010
001101	H	12-8	L10100
001110	I	12-9	L00110
001111	J	11-1	L01011
010000	K	11-2	L01111
010001	L	11-3	L10010
010010	M	11-4	L11100
010011	N	11-5	L01100
010100	O	11-6	L11000
010101	P	11-7	L10110
010110	Q	11-8	L10111
010111	R	11-9	L01010
011000	S	0-2	L00101
011001	T	0-3	L10000
011010	U	0-4	L00111
011011	V	0-5	L11110
011100	W	0-6	L10011
011101	X	0-7	L11101
011110	Y	0-8	L10101
011111	Z	0-9	L10001
100000	)	12-4-8	U10010
100001	-	11	U00011
100010	+	12	U11010
100011	<	12-6-8	NO CODE
100100	=	3-8	NO CODE
100101	>	6-8	NO CODE
100110	¬	2-8	NO CODE
100111	$	11-3-8	U01001
101000	*	11-4-8	NO CODE
101001	(	0-4-8	U01111
101010	"	0-5-8	U10001
101011	:	5-8	U01110
101100	?	12-0	U11001
101101	!	11-0	U01101
101110	COMMA	0-3-8	U01100
101111	STOP	0-6-8	NO CODE
110000	0	0	U10110
110001	1	1	U10111
110010	2	2	U10011
110011	3	3	U00001
110100	4	4	U01010
110101	5	5	U10000
110110	6	6	U10101
110111	7	7	U00111
111000	8	8	U00110
111001	9	9	U11000
111010	APOSTROPHE	4-8	U01011
111011	;	11-6-8	U11110
111100	/	0-1	U11101
111101		12-3-8	U11100
111110	□	0-7-8	NO CODE
111111	⩚	0-2-8	NO CODE

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PROBLEM ORIENTED FACILITIES

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . none.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

Sort/Merge

Reference: . . . . . UP 3809.
Record size: . . . . . 1 to 1,092 words; preset.
Block size: . . . . . 1 to 4,096 words; preset.
Key size: . . . . . any number of keys, each of any specified length.
File size: . . . . . no limit.
Number of tapes: . . . 3 to 12.
Date available: . . . . November, 1963.
Description:

The Sort/Merge routine is a three-phase program that utilizes the cascade method of merge sorting. The routine is generalized to sort data in various formats specified by the programmer in a parameter table. The priority of the sorting keys can be specified in the parameter table.

Optional features are: own code on initial input and/or last pass output from the final merge, tape swapping on input and/or final output, and restart points when program interruption is desired and when errors occur in the transfer of data.

Sort/Merge uses the executive system for loading, facility assignments, loading of the parameter table, and loading of own-code routines. Three to twelve Uniservo VIC, VIIIC, IIA, or IIIA tape units (all of one kind) are utilized. One Flying Head Magnetic Drum can be utilized, if available, for a drum presort in place of the standard tape presort.

.14 Report Writing: . . . . none.

.15 Data Transcription

PRINTAPE (Magnetic Tape to High-Speed Printer)

Reference: . . . . . UP 3807.4, UP 3805.4.
Date available: . . . . July, 1962.
Description:

This routine reads print-edited magnetic tapes and prints the records on the High-Speed Printer. Basic print editing, such as line spacing, margins, and page numbering, is permitted. The executive system is utilized for loading and for input/output requests. PRINTAPE uses approximately 1,238 words of memory and requires one High-Speed Printer and one Uniservo VIC, VIIIC, IIA, or IIIA tape unit.

CATUT (Card-to-Magnetic Tape Utility)

Reference: . . . . . UP 3807.3, UP 3805.3.
Date available: . . . . . February, 1963.
Description:

This is a generalized program to read punched cards and write the contents onto tape. CATUT may operate in a multiprogramming environment, thereby eliminating the need for off-line card-to-tape equipment. The executive system is used for loading and for I/O requests. Provision is made for optional inclusion of own coding.

CATUT requires approximately 1,614 words of core memory, one card reader, and one Uniservo VIC, VIIIC, IIA, or IIIA tape unit.

GULP (General Utility Library Program)

Reference: . . . . . UNIVAC 490 Software Note, September, 1963.
Date available: . . . . . September, 1963.
Description:

This program is an expandable library consisting of input-output routines used to transfer data from one peripheral medium to another. All possible combinations of media are permitted. Routines to handle non-standard formats can be added by the user. The program was designed to serve as a debugging aid and to perform service tasks for the executive system load program and SPURT.

GULP operates under the control of the executive system, requires approximately 1,178 words of core memory, either a card reader or a paper tape reader, one Uniservo VIC, VIIIC, IIA, or IIIA tape unit, and any other peripheral devices required to perform the desired function.

.16 File Maintenance

RMOPL II

Reference: . . . . . UP 3805.1A.
Date available: . . . . . June, 1963.
Description:

This program produces and maintains program library files of object programs. The executive is used for program loading, input-output requests, and parameter entry.

RMOPL II requires approximately 1,726 words of core memory, one card reader or paper tape reader, three Uniservo VIC, VIIIC, IIA, or IIIA tape units, and (optional) a High-Speed Printer and card punch.

RMASL

Reference: . . . . . UP 3805.6A.
Date available: . . . . . June, 1963.
Description:

This routine produces and maintains program library files in source-language form suitable as SPURT input. See RMOPL II (above) for other features.

.16 File Maintenance (Contd.)

CIMCO (Card Image Corrector)

Reference: . . . . . UP 3805.7A.
Date available: . . . . March, 1963.
Description:

This routine corrects a source-language program that is on magnetic tape in a SPURT 301 (card image) format. Corrections are punched on cards and may be replacements, additions, or deletions to the program on tape. CIMCO operates in conjunction with the executive system.

Approximately 1,332 words of memory are required, with one card reader and two Uniservo VIC, VIIIC, IIA, or IIIA tape units.

.17 Other Routines

TRACE IV (Debugging Routine)

Reference: . . . . . UP 3807.5, UP 3805.5.
Date available: . . . . October, 1962.
Description:

This program monitors the results of each instruction executed by a program operating under its control and prints a selective output on the High-Speed Printer.

The printout consists of the instruction address, the executed instruction, the operand, and the contents of the A, Q, and B registers. A printout can occur after every instruction, after jump instructions only, after instructions within a specified area, or only after execution of any instruction that modifies the contents of a specified "blood-hound address."

TRACE IV requires approximately 1,254 words of memory and one High-Speed Printer.

MITAR II

Reference: . . . . . UP 3805.2A.
Date available: . . . . February, 1962.
Description:

This routine assembles the Master Instruction Tape (MIT). REX, the operating system for the 490, 491, and 492 computer systems, is designed to process two or more independent programs concurrently. In order to do so with efficient utilization of core memory and peripheral equipment, REX must be presented with scheduling information, facility requirements, operational parameters, and the actual object code for all programs to be executed during a given processing session. The MIT contains this information.

Report Section 804:191 describes how Omega, the UNIVAC 494's operating system, performs this same function.

PROCESS ORIENTED LANGUAGE: COBOL

.1 GENERAL

.11 Identity: . . . . . UNIVAC 490 Series COBOL.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corporation.

.13 Reference: . . . . . UNIVAC 494 COBOL, Preliminary Language Specifications, August 1965.

.14 Description

The COBOL compiler for the 490 Series is being written for the UNIVAC 494, and a subset of this compiler will be used for the other 490 Series systems. The COBOL compiler written for the original UNIVAC 490 system will be replaced by this later version, which is based on the COBOL language as defined in the Department of Defense document, COBOL Preliminary Edition 1964. Any hesitation on the part of UNIVAC 490 users to change to the new compiler will no doubt be removed by compilation times estimated to be 270% to 600% faster than those of the older version. Further time savings will be realized by having the output of the new compiler in object-code form; the SPURT output of the older compiler necessitated an additional assembly phase.

Compatibility at source level with the older UNIVAC 490 compiler will be accomplished with few omissions. The major addition is the inclusion of the COMPUTE verb. The SORT verb is also new, but it will be available only in the expanded compiler for the UNIVAC 494.

A significant difference in the object coding is obtained through the use of a straight-line coding form in the new 490 Series compiler, rather than the generalized subroutines used in the older one. In this straight-line form, the coding extracted from the compiler for a specific option is shared only if this option is used more than once. Use of a different option of the same verb results in more coding being extracted. In the older version, a single generalized subroutine was used for each verb, with option variations handled by switch settings within the object coding. Unless a programmer uses a number of different options of the same verb, this new method will result in tighter and faster object coding.

The major exclusions from the UNIVAC 490 Series compiler, when compared to the standard established for the industry by the Department of Defense, are report writing and the handling of variable-length fields and records. The exclusion of variable-length data-handling facilities is understandable when the fixed word-length and non-character-oriented instruction complement of the 490 Series are considered; the use of these features by programmers unfamiliar with the characteristics of the UNIVAC 490 Series would tend to result in inefficient object programs. However, UNIVAC's decision to omit these features, rather than including the features with appropriate warnings to the programmer, is typical of the actions by the computer manufacturers that have prevented COBOL from achieving one of its major goals: the ability to provide complete inter-manufacturer program compatibility.

The UNIVAC 490 Series COBOL Compiler will operate under control of the integrated operating systems (REX for the 490, 491, and 492, and Omega for the 494). Minimum configuration requirements for the COBOL compiler are four Uniservo tape units, 16,384 words of core memory, one random-access storage device, one input device, and one output device. Compilation times will range from 400 to 600 statements per minute, depending upon length and complexity.

.141 Availability

Language: . . . . . 3rd quarter 1965 (preliminary manual).
Translator: . . . . . 3rd quarter 1966.

.142 Deficiencies with respect to Required COBOL-61

- The integer-4 option of the RECORD CONTAINS clause is not permitted; there is no provision for efficient handling of variable-length records; i.e., the compiler will consider all records to be the size of the largest record within a given file.
- The VALUE clause of the File Description entry can apply only to IDENTIFICATION, ID, or DATE-WRITTEN (Specific items that appear in the standard label record).

.143 Extensions to COBOL-61

- Files assigned to the DRUM may be designated as RANDOM or SEQUENTIAL files. Indices are used in READ and WRITE statements to reference records in RANDOM or SEQUENTIAL files.
- A complete sorting facility is available in the extended COBOL compiler for the UNIVAC 494.
- Debugging at source level is facilitated through the use of MONITOR, a verb that allows tracing of the program. An output line will be written each time a data name is modified by any procedure statement, upon entering a procedure, and upon altering a procedure.
- The compiler provides for all functions necessary for segment operation on a priority basis. The segment priorities are based on frequency of use.

.144 COBOL-61 Electives Implemented (see 4:161.3)

Key No.	Elective	Comments
	Characters and Words	
1	Formula characters	= (equals), + (plus), - (minus), * (multiplication), / (division), and ** (exponentiation) are used.
2	Relationship characters	The symbols < = > are used.
3	Semicolon	A semicolon is included in the character set.
4	Long literals	The maximum size is 128 characters.
6	Figurative constants	HIGH-VALUE(S) and LOW-VALUE(S).
7	Computer-name	An alternative is provided between the UNIVAC 494 and the UNIVAC 490 (491, 492).
	File Description	
11	SEQUENCED ON	The Sort facility is available in the UNIVAC 494 version of the compiler.
	Record Description	
15	BITS option	COMPUTATIONAL is used to specify items in binary.
18	SIGN IS	Separate signs are allowed.
20	Conditional ranges	Two ranges of VALUES for conditionals are permitted.
	Verbs	
22	COMPUTE	Algebraic formulas can be used.
24	ENTER	SPURT and FORTRAN can be used in a COBOL program.
	VERB Options	
27	LOCK	A rewound tape can be locked.
28	MOVE CORRESPONDING	Commonly-named items in a group can be handled together.
30	ADVANCING	Specific paper-advance instructions can be given.
31	STOP provisions	Special numeric-coded alphabetic displays.
32	Formulas	Algebraic formulas can be used.
33	Operand size	Up to 18 digits.
34	Relationship	IS EQUAL TO, EQUALS, EXCEEDS relationship.
35	Tests	IF ( ) IS NOT ZERO test is allowed.
36	Conditionals	Implied subjects with implied objects are allowed.
38	Complex conditionals	Nested conditionals are permitted.
39	Conditional statements	IF, SIZE ERROR, AT END, ELSE (OTHERWISE) may follow an imperative statement.
	Environment Division	
40	SOURCE-COMPUTER	UNIVAC 494 or 490 (491, 492) can be specified.
41	OBJECT-COMPUTER	UNIVAC 494 or 490 (491, 492) can be specified.
46	I-O-CONTROL	A full range of rerun techniques is available.
	Identification Division	
47	DATE-COMPILED	The current date is inserted.
	Special Features	
48	Library	Subprograms (i.e., partial programs written in COBOL, FORTRAN, or SPURT and combined by the operating system to produce a single object program) can be included in the main object program.
49	Segmentation	Segmentation of programs is allowed.

(Contd.)

.145 COBOL-61 Electives Not Implemented (see 4:161.3)

Key No.	Elective	Comments
	Characters and Words	
5	Figurative constants	HIGH-BOUNDS(S) and LOW-BOUND(S) are not permitted.
	File Description	
8	BLOCK CONTAINS	No range can be specified.
9	FILE CONTAINS	Approximate file size cannot be shown.
10	Label formats	Labels must be standard or omitted.
12	HASHED	Hash totals cannot be created.
	Record Description	
13	Table-length	Lengths of tables and arrays may not vary.
14	Item-length	Variable item lengths cannot be specified.
16	RANGE IS	Value range of items cannot be shown.
17	RENAMES	Alternative groupings of elementary items cannot be specified.
19	SIZE clause	Variable item lengths cannot be specified.
21	Label handling	Only standard labels (or none) may be used.
	Verbs	
23	DEFINE	New verbs cannot be defined.
25	USE	Standard I/O handling is required by the executive routines, particularly Omega.
	Verb Options	
29	OPEN REVERSED	The ability to read tape backward has not been implemented.
37	Complex conditionals	ANDs and ORs cannot be intermixed.
	Environment Division	
42	SPECIAL-NAMES	ACCEPT, WRITE, and DISPLAY verbs use standard hardware-names for switches.
43	FILE-CONTROL	Cannot be taken from library.
44	PRIORITY IS	No file priorities can be assigned for multiprogramming.
45	I-O-CONTROL	Cannot be taken from library.

PROCESS ORIENTED LANGUAGE: FORTRAN IV

.1 GENERAL

.11 Identity: . . . . . UNIVAC 490 Series FORTRAN IV.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corp.

.13 Reference: . . . . . UNIVAC 490 FORTRAN, August 1965.

.14 Description

Mathematical processing on the UNIVAC 490 Series computers will be facilitated by the availability of a compiler for FORTRAN IV, as specified by the ASA working specifications for the FORTRAN language published in the Communications of the ACM, October 1964. For purposes of inter-report comparison, the features of the language as implemented by UNIVAC are compared to those of IBM 7090/7094 FORTRAN IV, as described in Report Section 408:162.

The facilities most conspicuously absent from the UNIVAC 490 Series FORTRAN IV language, when compared to IBM 7090/7094 FORTRAN IV, are the LOGICAL and COMPLEX operations. Other restrictions include a maximum integer constant size of nine digits rather than eleven, a maximum integer magnitude of 2^{29} rather than 2^{35}, and a maximum of three dimensions for arrays rather than seven.

The most significant extension is the ability to use an implied DO structure in an extended DATA statement.

UNIVAC 490 Series FORTRAN is a one-pass compiler. As such, it imposes certain ordering restrictions on the source program, as indicated in Table I.

Object program running times will show wide variations between the UNIVAC 494 and the remainder of the 490 Series computers, as one would expect. In addition to its much faster basic cycle time, the 494 has built-in facilities for floating-point arithmetic, whereas the 490, 491, and 492 all require the use of subroutines.

.141 Availability

Language specifications: . . . . . August 1965.
Compiler: . . . . . June 1966.

.142 Restrictions of 490 Series FORTRAN IV Relative to IBM 7090/7094 FORTRAN IV

(1) Integer (fixed-point) values are limited to 9 decimal digits (maximum value 2^{29}), whereas FORTRAN IV for the 7090/7094 permits a maximum of 11 decimal digits (maximum value is 2^{35}).

(2) COMPLEX variables and statements are not permitted in UNIVAC 490 Series FORTRAN.

(3) The LOGICAL (true-false) capabilities of IBM 7090/7094 FORTRAN IV are not provided in UNIVAC 490 Series FORTRAN IV.

.143 Extensions of 490 Series FORTRAN IV Relative to IBM 7090/7094 FORTRAN IV

(1) A DATA statement can be extended to include an implied DO structure.

TABLE I: SOURCE PROGRAM ORDERING RESTRICTIONS

Order No.	Statement Type	Comments
1	FUNCTION	Order 1 statements are sections which are logically separate from the main program.
1	SUBROUTINE	
1	BLOCK DATA	
2	DIMENSION	
2	EQUIVALENCE	
2	COMMON	
2	REAL	These three Order 2 (or Type) statements are used to declare the type of variables, arrays, and functions as integer, real (single-precision floating-point), or double-precision.
2	INTEGER	
2	DOUBLE PRECISION	
3	DATA	The DATA statement enables the internal production of data at the time of object program loading.
4	Arithmetic Functions	For example, I = A + B. The mode to the left of the equal sign need not be identical to that to the right. Mixed-mode arithmetic (i.e., having two modes to the right of the equal sign) is not permitted.
5	Control Statements	
5	CALL	
5	Arithmetic Assignment	
5	I/O Statements	
5	FORMAT	
5	PAUSE	
5	STOP	
6	END	A blank card must follow an END statement.

MACHINE ORIENTED LANGUAGE: SPURT

.1 GENERAL

.11 Identity: . . . . . SPURT Assembly System.

.12 Origin: . . . . . UNIVAC Division, Sperry Rand Corp.

.13 Reference: . . . . . UNIVAC Technical Bulletin UT-2522.

.14 Description

SPURT is a symbolic assembly system that permits utilization of all the hardware facilities of the UNIVAC 490, 491, and 492 computer systems. SPURT can also be used with the UNIVAC 494, although an Assembler specifically designed for the 494 will also be made available. SPURT provides facilities for the definition and use of macro instructions, and produces object programs that can be multi-run under the control of the operating system.

The SPURT coding sheet has columns for Labels, Operators, and Operands and Notes. The operators (or operation codes) may be in mnemonic form and, when used with "allied operands," provide a large variety of operations. The content of the Operand column is free-form and varies according to the instruction. It may contain tags, increments, constants, extended constants, j-designators, tag modifiers, absolute addresses, designation of half-word operands, arithmetic and address modification registers, complementation of values, and literals for certain macro-instructions. Constants can be indicated in decimal or octal mode. Programmer notes are permitted.

A macro-instruction is a symbolic command which accesses an entire group of instructions. Depending upon the macro, the instructions generated may be incorporated directly into the program, or may be linked to the program as a subroutine. Addresses, parameters, or any other information needed to link the macro to the program are provided by the operands in the macro line of coding.

Corrections to a source program can be made in a separate assembly run. Deletion, replacement, and addition of operations are permitted.

Each input-output operator in a SPURT program causes the assembler to generate a return jump instruction followed by a packet of information. At run time, control is transferred to the operating system at that point, and the appropriate functional subroutine is utilized to initiate and control the input or output operation. If a real-time request or another request is being processed, the submitted request will be put into a queue. Various instruction codes are provided for operating system control.

SPURT is a six-phase assembly system. Output may be produced on paper tape, high-speed printer, and/or magnetic tape. A variety of assembly information and documentation may be requested. Coding errors detected by the translator are identified by console diagnostic and declarative messages or by error flags on the printed listing.

.15 Publication Date: . . . . March, 1962.

.16 Translator Availability: . . . . . April, 1962.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . free-form coding sheet; delimiters are used as follows:
→ Right arrow separates Label and Operator.
o Point separates Operator and Operands; also used between multiple Operands.
← Left arrow defines end of line.

.22 Legend

Label: . . . . . the symbolic address of a line of coding.
Operator: . . . . . basic function to be performed.
Operands: . . . . . define, modify, or complete the function.
Notes: . . . . . descriptive comments, printed in listings but otherwise ignored.

.23 Corrections: . . . . . correction header followed by insertions, deletions, and/or alterations.

.24 Special Conventions

.241 Compound addresses: . BASE ± ADJUSTMENT; where BASE = any label and ADJUSTMENT = a binary or decimal number and/or contents of a B register.

.242 Multi-addresses: . . . . none.

.243 Literals: . . . . . decimal or octal equivalent of a binary number (D must follow decimal); if minus, sign must appear.

.244 Special coded addresses: . . . . . (1) X preceding a tag will cause associated address to be extended when used.
(2) may indicate portion of word to be used by enclosing tag or absolute address in parentheses and preceding it by L, U, W, LX, or UX.

.244 Special coded addresses: (Contd.) . (3) may indicate complementing of a word or portion of a word by enclosing the associated tag in parentheses and preceding it by CPW, CPU, or CPL.
(4) $ means current location.

.3 LABELS

.31 General

.311 Maximum number of labels —
Procedures: . . . . . 1,730.
.312 Common label formation rule: . . . . . yes.
.313 Reserved labels —
For A-register: . . . . A.
For Q-register: . . . . Q.
For B-registers: . . . B0 through B7.
For channel numbers: C0 through C15.
.314 Other restrictions: . . . none of the symbolic operation codes may be used as a label.
.315 Designators: . . . . . none.
.316 Synonyms permitted: . yes.

.32 Universal Labels

.321 Labels for procedures —
Existence: . . . . . mandatory if referenced by other instructions (unless $ is used).
Formation rule —
First character: . . letter other than X or O.
Others: . . . . . letters or numerals; no special characters; spaces are ignored.
Number of characters: . . . . . maximum of 10.
.322 Labels for library routines: . . . . . same as procedures.
.323 Labels for constants: . same as procedures.
.324 Labels for files: . . . . same as procedures.
.325 Labels for records: . . same as procedures.
.326 Labels for variables: . same as procedures.

.33 Local Labels: . . . . . none.

.4 DATA

.41 Constants

.411 Maximum size constants —
Integer —
Decimal: . . . . . ±536870911.
Octal: . . . . . ±3777777777.
Fixed numeric —
Decimal: . . . . . no provision.
Octal: . . . . . no provision.
Floating numeric: . . no provision.
Alphameric: . . . . . no provision.
.412 Maximum size literals —
Integer: . . . . . same as constants.
Fixed numeric: . . . . no provision.
Floating numeric: . . no provision.
Alphameric: . . . . . 70 chars (used with TYPEC or TYPET macros).

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . . alternative.
Number: . . . . . 29 (many variations through "allied operands").
Example: . . . . . CL = Clear.
.512 Absolute —
Existence: . . . . . alternative (j, k, and b designators must be absolute also).
Number: . . . . . 62 (can be modified to produce over 25,000).
Example: . . . . . 01 = Shift Q Right.

.52 Macro-Codes

.521 Number available —
Input-output: . . . . . 15 (REX).
Data manipulation: . . 6.
Subroutine linkage: . . 2.
.522 Examples: . . . . . →MOVE·3·AREA2·AREA4→.
→FORM-TEXT·NOTE2·17D·THIS IS SAME AS BEFORE→.
.523 New macros: . . . . . yes; through use of SPURT User Defined Macro Assembler, incorporated into regular Assembler (available only in systems with drum storage).

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter: . . see Paragraph .542.
Label adjustment: . . pseudo operation.
Annotation: . . . . . see Paragraph .544.
.542 Allocation counter —
Set to absolute: . . . . ALLOCATION header plus direct allocation.
Set to label: . . . . . EQUALS pseudo.
Step forward: . . . . . DELETE value, REL-ALLOC header plus direct allocation.
Step backward: . . . . DELETE value.
Reserve area: . . . . . RESERVE pseudo.
.543 Label adjustment —
Set labels equal: . . . EQUALS pseudo.
Set absolute value: . . EQUALS pseudo.
Clear label table: . . . no provision; in a segmented program label table holds labels within the segment being processed plus the control segment.
.544 Annotation —
Comment phrase: . . . in any line of coding, following an arrow; COMMENT pseudo.
Title phrase: . . . . . no provision.
.545 Other —
Indirect allocation: . . U-TAG pseudo, INDR-ALLOC header, plus direct allocation (allows several different programs to access the same subroutine).

(Contd.)

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic

.611 Facilities: . . . . . inspect signs; binary multi-precision addition, subtraction, multiplication, and division; Fieldata multi-precision addition and subtraction; indexing; rounding and scaling; floating point arithmetic.

.612 Method of call: . . . . . CALL operator; Execute operator calls and sets up linkage to a closed subroutine.

.62 Special Functions

.621 Facilities: . . . . . character manipulation routines; examine, comparison, and relation routines.

.622 Method of call: . . . . . same as .612 above.

.63 Overlay Control: . . . . by own coding, using the SEGMENT and LOAD operators.

.64 Data Editing

.641 Radix conversion: . . . between Fieldata and binary.
.642 Code translation: . . . . none.
Format control —
Zero suppression: . yes.
Size control: . . . . . yes.
Sign control: . . . . . yes.
Special characters:. floating dollar sign, check protection, CR or DB, floating + or -.
.643 Method of call: . . . . . same as .612 above.

.65 Input-Output Control: . handled by File Control and operating system.

.651 File labels: . . . . . yes.
.652 Reel labels: . . . . . yes.
.653 Blocking: . . . . . yes.
.654 Error control: . . . . . yes.
.655 Method of call: . . . . . same as .612 above.

.66 Sorting: . . . . . see Sort/Merge program (800:151.13).

.67 Diagnostics: . . . . . inserted by DEBUG-AIDS header; removed by removing header and reassembling.

.671 Dumps: . . . . . DUMP-REG causes a printout of registers A, Q, and B1-B7.
DUMP-AREA causes a listed printout of all non-zero words in the specified debugging area(s).
.672 Tracers: . . . . . see 800:151.15.
.673 Snapshots: . . . . . see Paragraph .671 above.
.674 Others: . . . . . DEF-AREA defines area of the program to which debugging operations are to apply.
CORE-IMAGE provides an area in memory which will initially duplicate another area.
DRUM-IMAGE provides a drum area which will initially duplicate a program area.
TEST-IMAGE compares a program area against the corresponding core or drum image of that area.

.7 LIBRARY FACILITIES

.71 Identity: . . . . . SPURT Library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.
.723 Private: . . . . . yes.

.73 Storage Form: . . . . . magnetic tape.

.74 Varieties of Contents: . programs, directory, subroutines.

.75 Mechanism

.751 Insertion of new item: . special run: LIBRARY header with ADD-PROG.
.752 Language of new item: . format acceptable to SPURT assembler.
.753 Method of call: . . . . . CALL or EXECUTE operator.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: . . . . . yes.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Code	Description
CLEAR:	clears (fills with zeros) a number of words of an area of core memory.
ENTRY:	provides for entry into a subroutine; a manual stop may be added.
EXIT:	provides for a normal exit from a subroutine.
FD:	enters a literal into a program in Fieldata code.
FORM-TEXT:	stores alphanumeric text (converted to Fieldata code) in a buffer area for eventual printout on the on-line High-Speed Printer.
MOVE:	moves blocks of data from one area to another.
PUT:	places a single word in a designated storage address.
T-TAG:	provides a means by which an absolute channel and unit value can be placed in a word position.
REX-Associated Macros	
CKSTAT:	permits control of the sequence of operations following the submission of an I/O request.

.81 Macros (Contd.)

Code	Description
MTAPE:	request for Uniservo IIA or IIIA tape function.
CTAPE:	request for Uniservo VIC or VIIIC function.
PTAPE:	request for paper tape function.
FAST:	request for Fastrand function.
DISC:	request for disc function.
DRUM:	request for Flying Head drum function.
PRINT:	request for a print operation.
PIN:	specifies a margin format for the High-Speed Printer.
CARD:	specifies card operations.
TYPEC:	causes octal-coded content of specified storage registers to be typed by the console typewriter.
TYPET:	causes the console typewriter to type a given message.
ACCEPT:	indicates that operator is to respond to a printout by entering information via the console keyboard.
REX:	request for REX operating system action: stop or terminate run.
CONSOLE:	holds or releases the printer for exclusive use of the requesting program.
LOAD:	calls secondary segments into memory.

.82 Pseudos

Code	Description
ASSIGN:	groups several similar I/O units which are physically connected to the same channel.
MEANS:	permits a mnemonic channel name to be used in conjunction with mnemonic input-output instructions.
FACIL:	defines channels, peripheral units, and number of units required for each program.
EQUALS:	states a relation between a tag whose allocation value is unknown and a known value.
COMMENT:	indicates a notation to be presented in a listing of the program.
RESERVE:	reserves a block of memory locations in the running (object) program.
U-TAG:	provides for the expression of the value in the upper half and/or lower half of a storage word by means of a tag.
CALL:	calls programs from the library and incorporates them into a source program.
EXECUTE:	calls a closed routine from the library, places it at the end of the high-level coding, and sets up a linkage.
IGNORE:	inhibits program library extraction.
SEGMENT:	defines a secondary segment of a program.
END-SEG:	ends segmentation.
S-TAG:	defines entry points in a secondary segment.
DRUM-AREA:	reserves a relative drum area.
D-TAC:	defines certain points within a drum area.
OUTPUTS:	specifies documentation and output devices desired.

PROGRAM TRANSLATOR: SPURT

.1 GENERAL

.11 Identity: . . . . . SPURT Assembly System.

.12 Description

Operation of the SPURT translator requires at least 8,192 Core Memory locations, 4 Uniservo magnetic tape units, and the REX or Omega executive routine. Three versions of the SPURT translator are provided for UNIVAC 490 Series systems that use Uniservo IIA, IIIA, or IIIC/VIC/VIIIC tape units. Additional core storage increases efficiency by allowing the work tape buffers to be expanded. If a drum is included in the configuration, user-defined macro instructions are permitted. Larger configurations enable concurrent processing of both batch and real-time programs.

Input may be from punched cards, magnetic tape, or paper tape, and output may be produced on the high-speed printer, magnetic tape, and/or paper tape. The translator will accommodate source programs in either the SPURT Assembly language or UNIVAC 490 machine language, or a combination of the two.

The REX Executive routine (Section 800:191) effectively eliminates the need for detailed programming of standardized input and output functions. SPURT generates only the linkage instructions to REX and a packet of information for its use.

SPURT includes program diagnostic facilities. Instructions are provided to obtain core dumps and to test core images.

.13 Originator: . . . . . UNIVAC Division, Sperry Rand Corp.

.14 Maintainer: . . . . . as above.

.15 Availability: . . . . . April, 1962.

.2 INPUT

.21 Language

.211 Name: . . . . . SPURT and UNIVAC 490 Series machine language.

.212 Exemptions: . . . . . none.

.22 Form

.221 Input media: . . . . . magnetic tape, punched cards, or paper tape.

.222 Obligatory ordering: . . procedures must be in proper logical sequence.

.223 Obligatory grouping: . . no.

.23 Size Limitations

.231 Maximum number of source statements: . . not limited.

.232 Maximum size source statements: . . . . . 3 cards.

.233 Maximum number of data items: . . . . . 1,300.

.234 Other limitations —

Maximum number of ALLOCATION or REL-ALLOC items: . . . . . 1,700.

Maximum number of DEF-AREA statements: . . . . . 12.

Maximum number of CORRECT-L1 statements: . . . . . 150.

Maximum number of INDR-ALLOC statements: . . . . . 149.

Maximum number of MEANS statements: 26.

Maximum number of ADD PROG statements: . . . . . 20.

Maximum number of DRUM-AREA statements: . . . . . 16.

Maximum number of S-TAG statements: . 40.

Maximum number of ASSIGN operands: . 38.

Maximum number of SEGMENT operands: . . . . . 24.

Maximum number of programs in library: . . . . . 292.

Maximum number of macros defined: . . . 64.

Maximum number of updating actions demanded: . . . . . 192.

Maximum number of programs or keys to be listed, retrieved, or updated: 49.

Note: Sizes of the individual tables can be adjusted for a particular installation.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . . UNIVAC 490 Series machine language.

.312 Language style: . . . . . machine.

.313 Output media: . . . . . paper tape or magnetic tape; High-Speed Printer for listings.

.32 Conventions

.321 Standard inclusions: . . REX or Omega operating system.

.322 Compatible with: . . . . SPURT Library.

.33 Documentation

Subject	Provision
Source program:	listing.
Object program:	listing.
Storage map:	listing.
Restart point list:	none.
Language errors:	listing and console messages.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Phase 1: . . . . . Input — accepts source language from magnetic tape, paper tape, or cards. Processes source code to standard format on a work tape and identifies library references.

Phase 2: . . . . . Retrieval — adds any required programs from library to formatted source code.

Phase 3: . . . . . Declaration — processes declarative statements to build reference lists for translation.

Phase 4: . . . . . Translation — translates generative statements from formatted source code into machine coded instructions except for labels and tags, using reference lists produced by Phase 3.

Phase 5: . . . . . Allocation — first pass creates core table of program labels; second pass processes translation output to form object code in internal format.

Phase 6: . . . . . Output — converts source and/or object codes to the output media requested.

.42 Optional Mode

.421 Translate: . . . . . yes.
.422 Translate and run: . . . no.
.423 Check only: . . . . . no.
.424 Patching: . . . . . yes.
.425 Updating: . . . . . no.

.43 Special Features

.431 Alter to check only: . . no.
.432 Fast unoptimized translate: . . . . . access to library tape can be avoided on a correction run.
.433 Short translate on restricted program: . no.

.44 Bulk Translating: . . . . yes; Multi-Run option for magnetic tape input.

.45 Program Diagnostics: . removed by deleting DEBUG-AIDS header and reassembling.

.451 Tracers: . . . . . see 800:151.17.
.452 Snapshots: . . . . . dump operations with DEF-AREA.
.453 Dumps: . . . . . DUMP-REG, DUMP-AREA, and CORE-, DRUM-, and TEST-IMAGE operations.

.46 Translator Library

.461 Identity: . . . . . SPURT Library.
.462 User restriction: . . . . none.
.463 Form —
Storage medium: . . . magnetic tape.
Organization: . . . . . formatted source code.
.464 Contents —
Routines: . . . . . open or closed.
Functions: . . . . . no.
Data descriptions: . . no.
.465 Librarianship —
Insertion: . . . . . during special library run: ADD-PROG, INS-PROG operations.
Call procedure: . . . . CALL pseudo calls an open or closed routine. EXECUTIVE pseudo calls a closed routine and sets up a Return Jump to it.
Amendment: . . . . . DEL-PROG, RPL-PROG operations.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . . REX operating system for the 490, 491, and 492 occupies an average of 4,000 Core Memory locations.
Omega operating system for the 494 occupies between 4,000 and 8,000 Core Memory locations.
.512 Space required for each input-output file: . . . . . controlled by user.
.513 Approximate expansion of procedures: . . . . . one-to-one (except macrocodes).

.52 Translation Time

.521 Normal translating: . . approximately 500 to 600 statements per minute (Uniservo IIA) not including printing and card reading time.

.53 Optimizing Data: . . . . none.

.54 Object Program Performance: . . . . . unaffected; i.e., same as hand coding.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . . minimum of 8,192 core locations, 4 Uniservo magnetic tape units (of same type: IIA, IIIA, or IIIC, VIC, or VIIIC).
.612 Larger configuration advantages: . . . . . drum — may use programmer-defined macros.
additional tapes — reduce tape change requirements.
additional core — increased efficiency because work tape buffers are expanded.
on-line printer — allows on-line listings.
larger configurations permit concurrent processing of both batch and real-time programs.

(Contd.)

.62 Target Computer

.621 Minimum configuration: . . . . . any UNIVAC 490 Series system.

.622 Usable extra facilities: . . . . . all.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	check (card input only)	noted on listing.
Duplicate names:	check	noted on listing.
Improper format:	check	noted on listing or console.
Incomplete entries:	check	noted on listing or console.
Target computer overflow:	?	
Inconsistent program:	checks	noted on listing or console.
Unallocated tags:	check	noted on listing and equated to zero.

.8 ALTERNATIVE TRANSLATORS: . . . none.

OPERATING ENVIRONMENT: REX

.1 GENERAL

.11 Identity:. . . . . Real-Time Executive Routine.
REX.

.12 Description

The Real-Time Executive Routine (REX) is an on-line operating system that controls, sequences, and allocates facilities for user programs operating on a UNIVAC 490, 491, or 492 computer system. (The executive routine for the system, Omega, is described in Section 804:191.) The SPURT Assembly System language provides facilities for linkage and communication to REX. A group of Utility Routines is designed to operate under REX control.

REX provides a priority structure that permits one real-time program to be run concurrently with one or more batch programs. When the real-time program is processing a request, batch programs are interrupted.

The following functions are performed by REX:

- Selection and Loading — Programs to be run and their parameters are written on a Master Instruction Tape (MIT) in the order in which they are to be performed. Options are provided to run programs on demand only and to inhibit runs.
- Listing — REX maintains a queue of requests for program loading, input-output facilities, and utility functions.
- Console Control — Provides for communication between the operator and the running programs.
- Drum Control — Loads utility routines to be run as batch programs under REX control.
- Initiation — Maintains priority supervision over standard input-output requests. Priority is given to real-time program requests, while requests from batch programs are processed in the order submitted.
- Switching — Provides for sequencing the operation of programs constituting the current program mix. Top priority is always given to the real-time program. Batch programs are assigned priority ranks according to a programmer estimate of the percentage of time each program must spend awaiting completion of input-output operations. This results in programs with relatively little input-output being executed during the input-output time of higher-ranking programs. The switching routine also provides for the handling of interrupts which occurred while non-suspendible routines were operating.
- Real-Time Interrupt Analysis — Provides for entry to and exit from user-supplied subroutines.
- Input-Output Interrogation — A batch program can determine the condition of a standard input-output request by entering this routine. When a request is submitted, a program may wait for the operation to be completed or continue processing.
- Contingency Control — Provides for situations where the normal flow of a program is interrupted. A user-provided routine may be executed; or, if none is available, the program is usually suspended.

.13 Availability

FH-880 version: . . . . released in 1962.
Fastrand version: . . . December, 1963.

.14 Originator:. . . . . UNIVAC Division, Sperry Rand Corporation.

.15 Maintainer: . . . . . as above.

.16 Reference:. . . . . UNIVAC Technical Bulletin UP 2578, July, 1962.

.2 PROGRAM LOADING

.21 Source of Programs

Programs from on-line object code libraries and controlling data are stored on the Master Instruction Tape (MIT). Independent programs which will be on the drum at object time may be scheduled by entering controlling data on this tape. The MIT is generated by using the MIT Assembly routine (MITAR II), described in Paragraph 800:151.17. Parameters are stated by means of control cards, program cards, and operational parameter cards.

Loading of a program is accompanied by a console type-out describing the facilities required for the run. After the peripherals have been set up, the operator starts the program by a console type-in.

Use of the MIT is optional.

.22 Library Subroutines: . subroutines referenced in a main program but not incorporated into it are automatically loaded from magnetic tape or drum.

.23 Loading Sequence: . . . the order of programs on the MIT is specified by means of priority and string items on control cards. Certain programs may be "locked," and run only on demand. Runs may also be inhibited. These two options are controlled from the console. Up to 64 programs can be contained on one MIT.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Segmenting of routines: . . . . . as incorporated in user's program.

.312 Occupation of working storage:. . . . . controlled by REX.

(Contd.)

.32 Input-Output Units

.321 Initial assignment:. . . ASSIGN operator in SPURT assigns a unit to a channel group. Specific assignment to a channel is made by REX.

.322 Alternation: . . . . . can start new tape on another device by "START SCHEDULE FORMAT" message.

.323 Reassignment: . . . . . operator substitution.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: REX controls all input-output operations and attempts to maximize utilization of the available peripheral devices.

.42 Multiprogramming: . . one real-time program can be performed concurrently with one or more batch programs.

.43 Multi-sequencing: . . . no provisions.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Loading input error:	check	reported to operator.
Allocation impossible:	check before loading	recovery routine.
In-out error – cards:	interlock for card jam, etc.	halt program and offer options to operator.
In-out error – tape:	check	try again.
In-out error – persistent:	check	reported to responsible worker program via the status word.
Invalid operation:	hardware check	interrupt.
Program conflicts:	partial checks	REX protects itself.
Arithmetic overflow:	no check.	
Inproper format:	check	reported to originating program or operator.
Invalid address:	check	reported to requesting program.
Reference to forbidden area:	check.	

.45 Restarts

.451 Establishing restart points:. . . . . by program-initiated rerun dump (see Paragraph .52 below).

.452 Restarting process:. . after a program has been abandoned and rerun dump made, the operator can restart the program by using a "load" type-in.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . . utility program TRACE IV (800:151.17) can be used with REX.

.512 Snapshots: . . . . . INSPECT DRUM and INSPECT CORE operations, initiated by operator, provide console output for a small block of drum or core designated by the operator.
PRINT DRUM and PRINT CORE operations, initiated by operator or program, print blocks of drum or core on high-speed printer or magnetic tape (in octal or Fieldata).

.52 Post Mortem:. . . . . rerun dump, program initiated; drum will contain:
- o image of core memory area assigned to the requesting program;
- o bypass sentinel; REX facility and control information;
- o specified peripheral areas;
- o a second core image of the program and bypass sentinel.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator:. . . . . console typewriter messages.

.612 Action required by operator:. . . . . console typewriter messages.

.613 Reporting progress of run:. . . . . console typewriter messages.

.62 Operator's Decisions: console keyboard entries.

.63 Operator's Signals

.631 Inquiry:. . . . . console keyboard entries.

.632 Change of normal progress: . . . . . console keyboard entries. (program sequence is determined by MIT, but can be altered by console suspension, termination, and restart abilities. High-priority unscheduled programs can be loaded from tape or drum by "load" type-in.)

.7 LOGGING: . . . . . console typewriter messages.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . . 490, 491, or 492 Central Computer and Console.
1 magnetic tape unit.
1 Flying Head or Fastrand drum unit.
1 paper tape or card reader for automatic multi-program operation.

.812 Usable extra facilities:. . . . . larger Core Memory and all available peripheral devices.

.813 Reserved equipment: . approximately 4,000 Core Memory locations.
approximately 33,000 drum locations with 16K Core Memory, or 46,000 drum locations with 32K Core Memory.
1 magnetic tape unit.

.82 System Overhead

.821 Loading time:. . . . . 3 seconds, including operator type-in of date.

.822 Reloading frequency: . always in Core Memory.

.83 Program Space Available: . . . . . all of available core and drum storage except reserved areas listed in Paragraph .813.

.84 Program Loading Time: . . . . . limited by speed of input device.

.85 Program Performance:. . . . . an estimated 3 to 5% of the total central processor time is required for executive functions in typical multi-program operation.

SYSTEM PERFORMANCE

The overall performance of a UNIVAC 490 Series computer system naturally depends upon the user's choice of central processor model and peripheral equipment. Therefore, the performance of the UNIVAC 490 Series systems on the AUERBACH Standard EDP Reports benchmark measures of system performance has been analyzed separately for several representative configurations using each of the processor models. For performance curves, summary worksheets, and analyses of the results, please turn to the System Performance sections of the Subreports on the models of interest:

PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
UNIVAC 490, 491, 492						
Power Control Cabinet	40	35	96/64*	1,000	0.7	750
Central Processor	96	35	96/64*	1,500	Note 1	12,000
Computer Power Supply	40	35	96/64*	850	4.4	3,000
Control Console	54	35	32	400	0.5	1,350
UNIVAC 494						
Power Control Cabinet	36	35	96/64*	1,040	13.45	25,800
Central Processor	64	35	96/64*	600	Note 1	Note 1
Computer Power Supply	36	35	96/64*	900	Note 1	Note 1
Control Console	54	35	32	400	Note 1	Note 1
Core Storage	65	35	96/64*	800	Note 1	1,200
Peripherals						
FH-880 Drum	54	35	96/64*	1,300	2.2	5,125
FH-880 Drum Control	20	35	96/64*	625	0.85	1,640
FH-432 Drum	48	24	96/64*	765	2.5	600
FH-432 Drum Control	48	24	96/64*	1,300	0.85	2,000
FH-1782 Drum	64	34	96/64*	1,700	?	?
FH-1782 Drum Control	20	36	96/64*	?	?	?
Fastrand Mass Storage Unit	122	35	96/64*	5,150	12.5	19,500
Fastrand Control Unit	36	26	55	650	1.0	2,800
Uniservo IIA	31	35	96/64*	900/810	2.63	7,140
Uniservo IIA Control	20	35	96/64*	625	0.95	2,075
Uniservo IIIA	31	35	96/64*	900/810	2.75	7,480
Uniservo IIIA Control	20	35	96/64*	625	0.95	2,075
Uniservo IIIC	31	35	96/64*	900/810	2.75	7,480
Uniservo IIIC Control	31	35	96/64*	625	0.95	2,075
Tape Adapter Cabinet	35	35	96/64*	950	1.25	2,400
Uniservo Power Supply	66	35	96/64*	2,800	3.8	10,200
Uniservo VIC (control is included in first tape unit)	24	26	96/64*	500	1.9	3,500
Uniservo VIIIC	27	29	96/64*	700	2.75	5,100
Uniservo VIIIC Control	24	24	96/64*	600	0.95	2,170
Paper Tape Subsystem (includes reader, punch, and synchronizer in one cabinet)	24	35	96/64*	800	1.0	3,000
Card Reader	48.5	24	54	700	1.0	2,500
Card Punch	38	26	48	775	1.5	4,600
Card Control	20	35	96/64*	625	3.73	2,600
High Speed Printer	43	33	55	1,250	1.7	4,930
Printer Control	20	35	96/64*	625	5.95	2,600
Communication Terminal Module Controller	48	26	96/64*	2,000	5.9	6,000
Input-Output Controller	64	24	64*	1,800	5.4	12,300
Multi-Memory Adapter	?	?	?	?	?	?
Multi-Processor Adapter	?	?	?	?	?	?

* The 64-inch height is standard for the UNIVAC 491, 492 and 494 systems. The 96-inch height was standard for the UNIVAC 490 and will be available on new equipment for those users requiring it.

Note 1: Power and heat dissipation figures are included in Power Control Cabinet figure.

General Requirements

Temperature: . . . . . 60 to 80°F.
Relative humidity: . . . . . 30 to 80%.
Power: . . . . . 120/208-volt, 60-cycle or 220/380-volt, 50-cycle, 3-phase, 4-wire.

PRICE DATA

For price data on the original UNIVAC 490 computer system, which is no longer being actively marketed, please turn to Page 801:221.101.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSORS	491	The following UNIVAC 491 Processor Sets include: Processor Type 8187-02 with 8 I/O Channels; Control Console, Type 7313-00; Motor Alternator, Type 8070-01.			
	8187-99	491 Central Processor Set with 16,384 words of Core Memory	7,000	1,365	280,000
	8187-98	491 Central Processor Set with 32,768 words of Core Memory	11,000	1,390	440,000
	8187-97	491 Central Processor Set with 40,960 words of Core Memory	12,500	1,405	500,000
	8187-96	491 Central Processor Set with 49,152 words of Core Memory	13,500	1,420	540,000
	8187-95	491 Central Processor Set with 57,344 words of Core Memory	14,800	1,435	592,000
	8187-94	491 Central Processor Set with 65,536 words of Core Memory	15,500	1,450	620,000
	492	The following UNIVAC 492 Processor Sets include: Processor Type 8187-02 with 8 I/O Channels; 6 additional I/O channels, Feature F0764-00; Control Console, Type 7313-00; Motor Alternator, Type 8070-01.			
	8187-93	492 Central Processor Set with 16,384 words of Core Memory	8,750	1,455	350,000
	8187-92	492 Central Processor Set with 32,768 words of Core Memory	12,750	1,480	510,000
	8187-91	492 Central Processor Set with 40,960 words of Core Memory	14,250	1,495	570,000
	8187-90	492 Central Processor Set with 49,152 words of Core Memory	15,250	1,510	610,000
	8187-89	492 Central Processor Set with 57,344 words of Core Memory	16,550	1,525	662,000
	8187-88	492 Central Processor Set with 65,536 words of Core Memory	17,250	1,540	690,000
	3012-99	UNIVAC 494 Central Processor Set: Processor, Type 3012-00; Twelve 250KC Channels; Control Console, Type 4004-02.	9,500	1,248	399,000
		Optional Features for UNIVAC 494:			
	F0745-00	250KC Channels - Increment of 4	250	32	10,500
	F0745-01	550KC Channels - Increment of 4	550	62	23,100
	F0774-xx	Auxiliary Console	150	—	6,300

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INTERNAL STORAGE		UNIVAC 491/492 Core Memory See Central Processor listings.			
		UNIVAC 494 Core Memory			
	7005-99	16,384 words of Core Memory — Single Bank	4,500	370	189,000
	7005-98	32,768 words of Core Memory — Dual Banks	6,500	500	273,000
	7005-97	65,536 words of Core Memory — Dual Banks	11,000	700	462,000
	7005-96	98,304 words of Core Memory — Dual Banks	15,500	975	651,000
	7005-95	131,072 words of Core Memory — Dual Banks	20,000	1,250	840,000
		FH-1732 Magnetic Drum Subsystem (1)			
		(prices to be announced)	?	?	?
		FH-432 Magnetic Drum Subsystem (1)			
	F0696-00	FH-432 Drum Unit	1,000	85	40,000
	6013-02	FH-432 Drum and Control	3,000	310	120,000
		FH-880 Magnetic Drum Subsystem			
	7304-01	FH-880 Drum	2,000	165	92,000
	8103-03	FH-880 Drum Control and Synchronizer	1,420	165	71,000
		Fastrand II Control and Synchronizer			
	5009-12	Single Channel — Unbuffered	1,200	100	57,600
	5009-08	Single Channel — Buffered	1,250	100	60,000
	5009-13	Dual Channel — Unbuffered	2,400	200	115,200
	5009-09	Dual Channel — Buffered	2,500	200	120,000
	F0710-00	Search All Words — buffered control option	50	10	2,000
		Fastrand II Subsystem			
	6010-00	Fastrand II Storage Unit	3,800	265	184,000
	F0686-01	Fastrand feature	200	22	9,000
	F0688-01	Write Lockout feature	25	3	1,125
INPUT-OUTPUT		Uniservo VIC Magnetic Tape Subsystem			
	0858-00	Uniservo VIC Master 7-Channel Non-Simultaneous Unit	500	125	20,000
	0858-08	Uniservo VIC Master 7-Channel Simultaneous Unit	550	125	22,000
	0858-01	Uniservo VIC Slave 7-Channel Unit	300	75	12,000
	5008-04	Uniservo VIC Control and Synchronizer, Single-Channel	700	30	28,000
	5008-05	Uniservo VIC Auxiliary Control and Synchronizer, Dual-Channel	700	30	28,000
	F0627-04, F0627-03	Translate Options for 5008-04, -05, -16, -17	100	5	3,600

(Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd.)		Uniservo VIIIC Magnetic Tape Subsystem			
	0859-00	Uniservo VIIIC 7-Channel Non-Simultaneous Unit	800	95	36,000
	0859-02	Uniservo VIIIC 7-Channel Simultaneous Unit	850	95	38,250
	5008-16	Uniservo VIIIC Control and Synchronizer, Single-Channel	1,450	105	60,900
	5008-17	Uniservo VIIIC Control and Synchronizer, Dual-Channel	1,450	105	60,900
		High-Speed Printer Subsystem			
	0751-00	High-Speed Printer — 700/922 LPM (3)	800	240	36,000
	8120-00	High-Speed Printer Control and Synchronizer (3)	750	160	34,275
		Punched Card Subsystem			
	0706-00	Card Reader — 800/900 CPM	380	100	15,200
	0600-00	Card Punch — 300 CPM	665	295	26,600
	5010-01	Card Control and Synchronizer	750	230	33,750
	8136-00	Paper Tape Reader and Punch	645	110	32,250
	F0700-xx	Electronic Transfer Switch (2)	150	8	6,000
	2502-xx	Electronic Transfer Switch Cabinet (2)	325		13,000
	F0597-02	1004 to 491 and 492 Adapter (2)	200	20	8,000
		Communication Subsystem			
	F0900-05	Communication Terminal Module Controller	650	118	25,000
	F0901-04	Communication Terminal Module—low-speed, asynchronous, 5-8 level, 2 in, 2 out	60	11	2,400
	F0902-02	Communication Terminal Module—medium-speed, asynchronous, 5-8 level, 2 in, 2 out	75	13	3,300
	F0903-02	Communication Terminal Module—high-speed, synchronous, 5-8 level, 2 in, 2 out	90	12	3,600
	F0905-00	CLT Automatic Dialing — 1 Output	20	6	900
	F0904-00	CLT Parallel Output	35	7	1,575
	F0904-01	CLT Parallel Input	35	7	1,575
		Data Communication Terminal			
	8552-00	Data Communication Terminal Basic Set	250	?	10,000
	F0614-00	Power Supply for 8552-00,01	100	?	4,000
	F0615-00	Communication Terminal Synchronous (CTS) Module	250	?	10,000
	F0616-00	Broad-Band Interface	100	?	4,000
	F0617-00	Unattended Answering Service	5	?	200
	F0618-00	Automatic Calling	50	?	2,000
		Data Communication Terminal			
	8552-01	Data Communication Terminal Basic Set	250	?	10,000
	F0614-01	Power Supply (for Second WTS)	100	?	4,000
	F0771-01	Word Terminal Synchronous (WTS) Module	395	?	15,800
	F0772-00	Voice-Band Adapter	5	?	200
	F0772-01	Unattended Answering Service	5	?	200

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd.)	F0772-02 F0772-03	Automatic Calling Broad-Band Adapter	50 5	? ?	2,000 200
MULTI-PROCESSOR EQUIPMENT FOR 494		Input-Output Controller Basic controller with 4 I/O channels; includes cabinet and power supply	4,000	100	168,000
		Optional features: Additional I/O Channels, per increment of 4	500	50	21,000
		ESI Buffer Control, expansion from 256 to 512 words	750	5	31,000
		Multiple Module Adapter (MMA) MMA with 5 access paths; 30 bit; includes cabinet and power supply	735	50	30,870
		Multi-Processor Adapter (MPA) Basic 30-bit MPA; 2-Processor capability; includes cabinet and power supply.	435	25	18,270

(1) Available for 494 only.

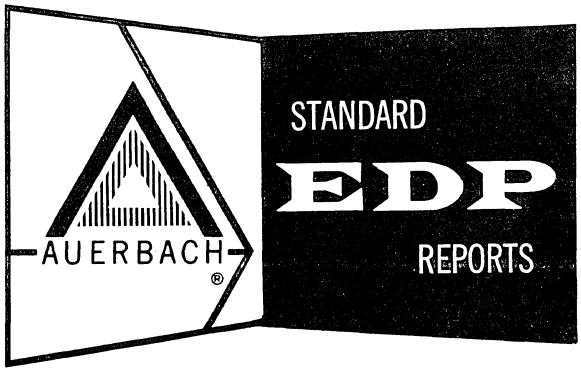
(2) Available for 491 and 492 only.

(3) The same Printer and Printer Control are offered for the 494 computer system at the same prices, but as model numbers 0755-00 and 8120-02, respectively.

UNIVAC 490

Univac

(A Division of Sperry Rand Corporation)



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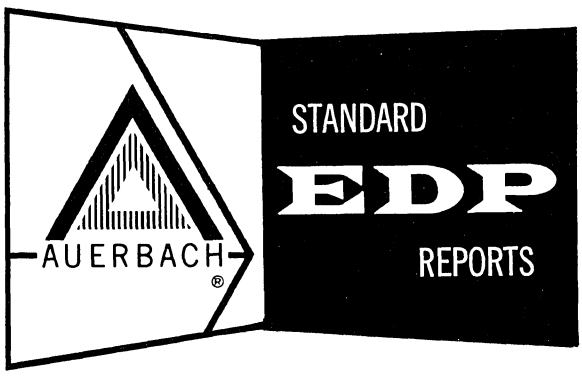

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INTRODUCTION

The UNIVAC 490 Real-Time System was announced in December 1960, and the first customer delivery was made in December 1961.

Among the characteristics of the original UNIVAC 490 system that distinguish it from the newer members of the 490 Series are the following:

- A basic core storage cycle time of 6 microseconds (or 4.8 microseconds with the optional Accelerator Package).
- Core storage capacities of 16,384 or 32,768 30-bit words.
- An instruction repertoire consisting of 62 basic instructions.*
- The absence of direct facilities for floating-point, double-precision, and decimal arithmetic.*
- The absence of a parity check on core storage operations.*
- A maximum of 14 input-output channels, 12 of which are available for general-purpose use.
- Inability to utilize some of the new, high-performance 490 Series peripheral devices, such as Fastrand II, the FH-432 and FH-1782 Drums, and the Uniservo VIC and VIIIC Magnetic Tape Handlers.

This subreport concentrates upon the characteristics and performance of the UNIVAC 490 Central Processor and systems based upon it. All general characteristics of the 490 Series hardware and software are described in Computer System Report 800: UNIVAC 490 Series — General.

The System Configuration section that follows shows the UNIVAC 490 system arranged in a number of standardized configurations according to the rules in the Users' Guide, page 4:030.120. These standardized equipment configurations form the basis for a detailed analysis of the overall System Performance of the UNIVAC 490 on our standard benchmark problems, the results of which are presented in Section 801:201.

Section 801:051 contains a detailed description of the UNIVAC 490 Central Processor, its processing facilities, and its execution times for a series of standardized tasks.

The rentals, purchase, and maintenance prices that were in effect for the UNIVAC 490 system while it was being actively marketed are listed in Section 801:221.

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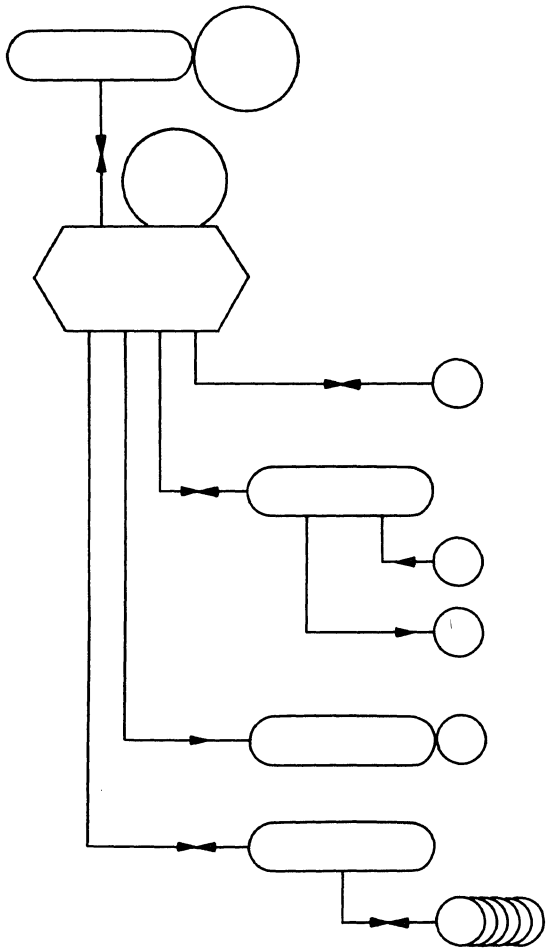
* These characteristics are shared by the newer UNIVAC 491 and 492 systems described in the following subreport.

SYSTEM CONFIGURATION

For overall configuration rules, refer to Page 800:031.100.

.1 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

Deviations from Standard Configuration: . . . . . auxiliary storage (Fastrand) is 224% larger.
core storage is 350% larger.
card punch is 50% faster.
printer is 40% faster.
2 more simultaneous non-tape data transfer operations are possible
4 more index registers.

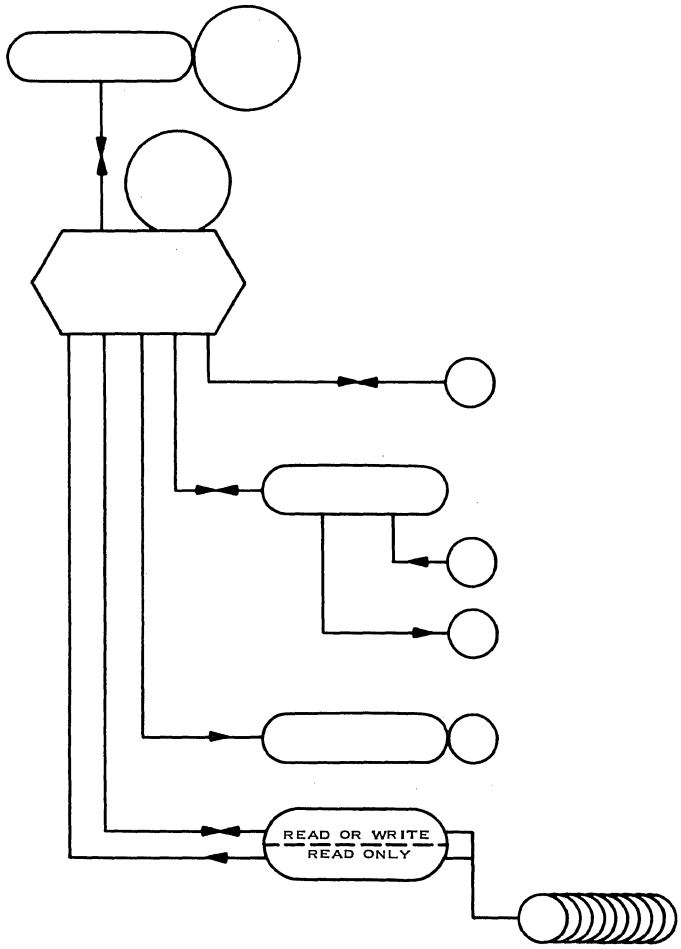


Equipment	Rental
Fastrand Storage Unit & Synchronizer: 12,976,128 words	$ 6,050
Core Memory: 16,384 words	
Central Processor	10,000
Console	
Card Control & Synchronizer	1,600
Card Reader: 600 cards/min.	350
Card Punch: 150 cards/min.	500
Printer & Synchronizer: 700/922 lines/min.	2,550
Uniservo IIA Synchronizer	1,530
Uniservo IIA Tape Units (6): 25,000 char/sec.	2,700
Uniservo Power Supply (not shown)	550
TOTAL RENTAL:	$25,830

Note: Standard Configuration III is the same as Configuration V (shown here) less Fastrand Storage Unit and Synchronizer; its rental is $19,780 per month.

.2 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

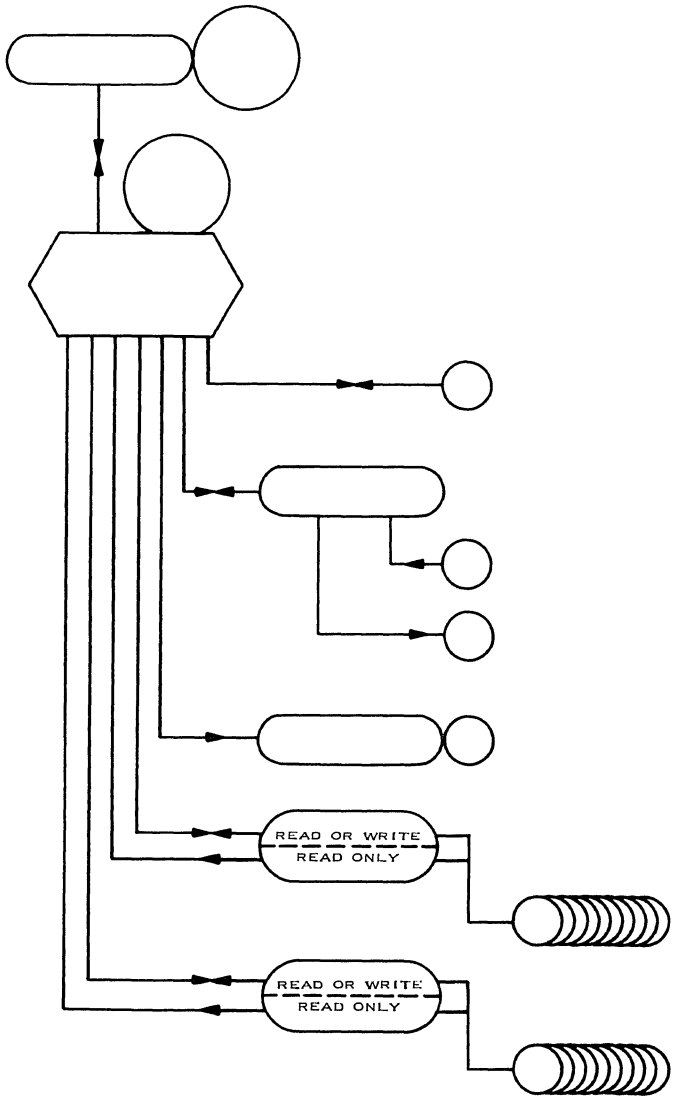
Deviations from Standard Configuration: . . . . . magnetic drum is required for use of most software systems.
core storage is 24% smaller.
magnetic tape is 108% faster.
card punch is 50% faster.
printer is 40% faster.
floating-point hardware is not available.



Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$ 3,420
Core Memory: 16,384 words	
Central Processor	10,000
Console	
Card Control & Synchronizer	1,600
Card Reader: 600 cards/min.	350
Card Punch: 150 cards/min.	500
Printer & Synchronizer: 700/922 lines/min.	2,550
Uniservo IIIA Synchronizer: dual channel model	4,800
Uniservo IIIA Tape Units (10): 125,000 char/sec.	7,500
Uniservo Power Supply (not shown)	550
TOTAL RENTAL:	$31,270

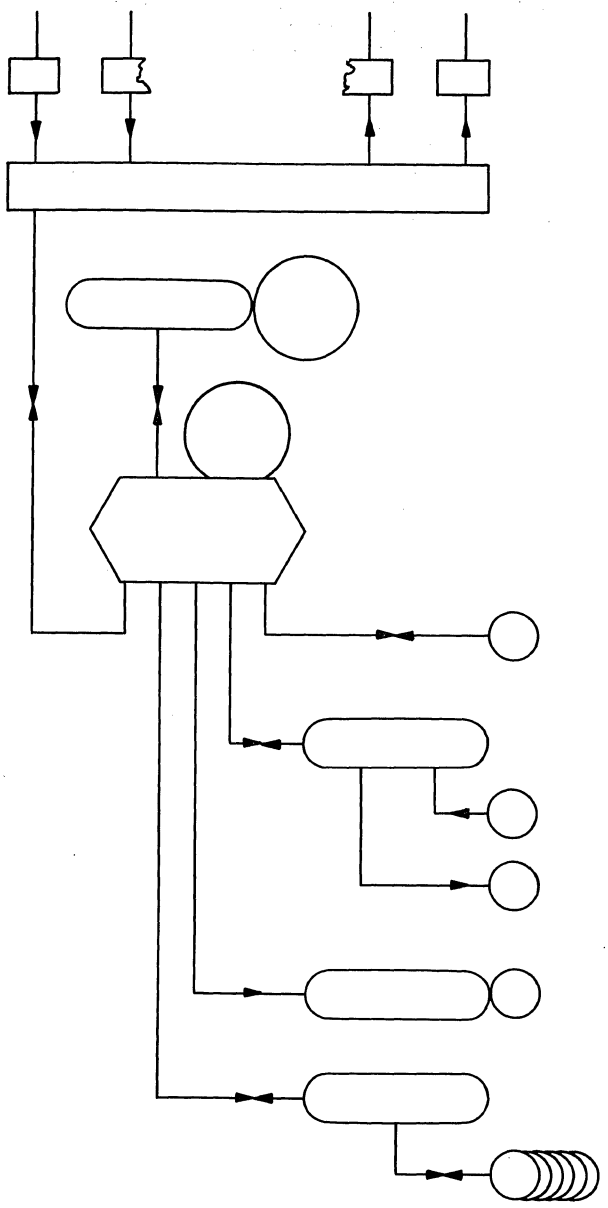
.3 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: . . . . . magnetic drum is required for use of most software systems.
core storage is 24% smaller.
magnetic tape is 108% faster.
card reader is 40% slower.
card punch is 25% slower.
printer is 20% slower.
floating-point hardware is not available.



Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$ 3,420
Core Memory: 32,768 words	14,000
Central Processor	
Console	
Card Control & Synchronizer	1,600
Card Reader: 600 cards/min.	350
Card Punch: 150 cards/min.	500
Printer & Synchronizer: 700/922 lines/min.	2,550
Uniservo IIIA Synchronizers (2): dual-channel models	9,600
Uniservo IIIA Tape Units (20): 125,000 char/sec.	15,000
Uniservo Power Supply (not shown)	1,100
TOTAL RENTAL:	$48,120

.4 TYPICAL COMMUNICATIONS SYSTEM



Equipment	Rental
Communication Line Terminals: up to 32 input and 32 output lines	*
Communication Multiplexer	$ 1,300
Fastrand Storage Unit & Synchronizer: 12,976,128 words	6,050
Core Memory: 16,384 words	10,000
Central Processor	
Console	
Card Control & Synchronizer	1,600
Card Reader: 600 cards/min.	350
Card Punch: 150 cards/min.	500
Printer & Synchronizer: 700/922 lines/min.	2,550
Uniservo IIA Synchronizer	1,530
UniservoIIA Tape Units (6): 25,000 char/sec.	2,700
Uniservo Power Supply (not shown)	550
TOTAL RENTAL:	$27,130

* Costs of the necessary Communication Line Terminals and interface units are not included.

CENTRAL PROCESSOR: UNIVAC 490

.1 GENERAL

.11 Identity: . . . . . UNIVAC 490 Central Processor. Types 8188 through 8199.

.12 Description

The Central Processor of the UNIVAC 490 computer system is a single cabinet that houses the system's solid-state arithmetic and control circuits, 16 word locations of Wired Memory, and 16,384 or 32,768 word locations of Core Memory with a cycle time of 6 microseconds. The faster, more powerful Central Processors used with the UNIVAC 491/492 and 494 systems are described in Sections 802:051 and 804:051, respectively.

Each UNIVAC 490 instruction is one word (30 bits) in length and consists of five parts called "designators," as shown below.

Designator:	f	j	k	b	y
Size (bits):	6	3	3	3	15

- The 6-bit f-designator specifies the basic operation to be performed.
- The 3-bit j-designator usually specifies the conditions under which a skip or jump will be performed (e.g., when contents of an arithmetic register are positive, negative, zero, or non-zero). It can also specify the mode for a "Repeat" instruction, or the index register to be used in a loop control instruction. (In input-output instructions, the j-designator is 4 bits long and specifies the channel to be used.)
- The 3-bit k-designator shows how the operand is to be derived from the y-designator part; e.g., the operand of a load instruction can be y itself, all or either half of the Core Memory location specified by y, or the contents of the accumulator. (In input-output instructions, the k-designator is only 2 bits long, but its function is similar.)
- The 3-bit b-designator specifies one (or none) of seven index registers, whose contents are to be added to the y-designator part to form the operand or its address.
- The 15-bit y-designator specifies the base operand address, a literal operand, or a shift count.

There are 62 basic instructions, each with up to 64 distinct variations made possible by the j- and k-designators. The j-designator in most instructions can cause a conditional skip of the next instruction, depending upon the sign of the A-register (accumulator) or Q-register after the specified operation has been performed. The k-designator in most instructions can specify whether the operand shall consist of all 30 bits or only the high-order or low-order 15 bits of the Core Memory location specified by the y-designator. Where half-word operands are specified, sign extension is optional.

The UNIVAC 490 instruction repertoire includes a full complement of fixed-point arithmetic, Boolean, comparison, and shift operations on 30-bit binary operands. Thirteen different "Replace" instructions provide many of the capabilities of two-address, "add-to-storage" processors; e.g., by means of a single instruction, the contents of the accumulator can be added to (or subtracted from) the contents of a specified Core Memory location and the result placed in both the accumulator and the specified Core Memory location. The "Repeat" instruction causes the instruction immediately following it to be executed from 0 to 32,767 times, with or without index register modification prior to each execution. The Repeat capability permits efficient table lookup operations. Special instructions are provided to load, store, test, and increment (by +1 or -1 only) the contents of the seven index registers.

Facilities not directly provided in the instruction repertoire include editing, double precision arithmetic, decimal arithmetic, floating point arithmetic, multi-word internal transfers, and radix conversions. Generalized subroutines or complex sequences of instructions are therefore required to accomplish these important operations.

Execution time is 12 microseconds for most UNIVAC 490 instructions that reference an operand in Core Memory. When the operand is contained in the instruction itself (as a 15-bit literal) or in the accumulator or Q-register, the execution time is generally lower. Address modification by indexing does not increase instruction execution times. Average execution time is about 10 microseconds per instruction.

Program interrupts occur upon normal completion of an input-output operation (optional), upon detection of an input-output or processor error, and upon overflow of the program-settable delta clock. Control is transferred to one of 44 fixed locations, depending upon the cause of interruption. Only the contents of the instruction sequence counter can be automatically saved when an interrupt occurs, so the routine that services the interrupt condition (usually REX) must preserve and restore the previous contents of all the registers it uses. The interrupt facility makes it possible to run one or more batch programs concurrently with a real-time program, under control of the Real-Time Executive Routine (REX), described in Section 800:191.

The UNIVAC 490 has three electronic chronometers. The Real-Time Clock occupies the lower half of octal location 00017, is incremented each millisecond, and recycles back to zero every 32,768 milliseconds. The Delta Clock occupies the upper half of octal location 00017, counts each mil-

.12 Description (Contd.)

lisecond, and can be set by the program to initiate an interrupt after any time interval from 1 to 32,768 milliseconds. The Day Clock is connected to one of the two "computer-to-computer" data channels, is controlled by REX, and presents the time of day (in hours and minutes) via an interrupt each minute.

.13 Availability: . . . . . discontinued.

.14 First Delivery: . . . . . December, 1961.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point —			
Add-subtract:	automatic	binary	29 bits + sign.
Multiply —			
Short:	none.		
Long:	automatic	binary	29 bits + sign (60-bit product).
Divide —			
No remainder:	none.		
Remainder:	automatic	binary	29 bits + sign (60-bit dividend).
.212 Floating point —			
Add-subtract:	subroutine	binary	fraction: 28 bits + sign. exponent: 15 bits + sign.
Multiply:	subroutine		
Divide:	subroutine		
.213 Boolean —			
AND:	automatic	binary	30 bits.
Inclusive OR:	automatic		
Exclusive OR:	automatic		
.214 Comparison —			
Numbers:	automatic		30 bits.
Letters:	automatic		30 bits (6 chars).
Mixed:	automatic		30 bits (6 chars).
Collating sequence:	see Data Code Table, Section 800:141.		

	Provision	Comment	Size
.215 Code translation:	none	performed by subroutines.	
.216 Radix conversion:	none		
.217 Edit format —			
Alter size:	none		
Suppress zero:	none		
Round off:	none		
Insert point:	none		
Insert spaces:	none		
Insert commas:	none		
Float $, +, -:	none		
Protection:	none		
.218 Table look-up —			
Equality:	none.		
Greater than:	semi-automatic through use of "Repeat" instruction		30 bits.
Less than or equal:			
Within limits:			
Greatest:	none.		
Least:	none.		

(Contd.)

	Provisions	Comment	Size
.219 Others —			
Shifts:	automatic	left shifts are circular; right shifts with sign extension	30 or 60 bits.
Add to storage:	automatic	---	29 bits + sign.
Subtract from storage:	automatic	---	29 bits + sign.
Repeat:	automatic	executes next instruction specified number of times.	

.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement.

.222 Zero: . . . . . +0 and -0 have zeros and ones, respectively, in all 30 bit positions; they are considered unequal in compare and certain arithmetic operations.

.223 Operand size determination: . . . . . k-designator in most instructions specifies full word (30 bits), upper or lower half-word (15 bits), or literal operand (15 bits).

.23 Instruction Formats

.231 Instruction structure: 1 word.

.232 Instruction layout:

Name:	f	j (or j*)	k (or k*)	b	y
Size (bits):	6	3 (or 4)	3 (or 2)	3	15

.233 Instruction parts —

Name	Purpose
f-designator	specifies operation code.
j-designator:	specifies skip or jump condition, or special register.
j*-designator (I/O instruction):	specifies input or output channel.
k-designator:	controls the procedure by which the operand is derived.
k*-designator (I/O instruction):	controls procurement and/or storing of the operand.
b-designator:	specifies 1 (or none) of 7 Index Registers, whose contents are added to y.
y-designator:	specifies an operand address or a literal operand.

.234 Basic address structure: . . . . . 1 + 0.

.235 Literals—

Arithmetic: . . . . . 15 bits (i.e., up to 32,767).

Comparisons and tests: . . . . . 15 bits.

Incrementing modifiers: . . . . . 15 bits.

.236 Directly addressed operands—

Internal storage type	Minimum size	Maximum size	Volume accessible
Core Memory:	15 bits	1 word	total capacity (16,384 or 32,768 words).
Wired Memory:	15 bits	1 word	16 words.

.237 Address indexing—

.2371 Number of methods: 1.

.2372 Name: . . . . . indexing.

.2373 Indexing rule: . . . . . add contents of specified index register to Y (low-order 15 bits of instruction word), modulo 32,768.

.2374 Index specification: by b-designator in the instruction to be modified.

.2375 Number of potential indexers: . . . . . 7.

.2376 Addresses which can be indexed: . . . operand address portion (y-designator) of all instructions, including literals.

.2377 Cumulative indexing: . . . . . none.

.2378 Combined index and step: . . . . . none.

.238 Indirect addressing: . . only by means of jump instructions.

.239 Stepping—

.2391 Specification of increment: . . . . . implied by operation code.

.2392 Increment sign: . . . . + or -.

.2393 Size of increment: . . always 1 or 2 (depending on skip conditions).

.2394 End value: . . . . . zero, or any value specified in instruction or storage location.

.2395 Combined step and test: . . . . . yes.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program usage
Register:	1	30	A-register;accumulator.
Register:	1	30	Q-register; auxiliary arithmetic register; combines with A-register to form a single 60-bit register.
Register:	1	15	P-register; holds address of next instruction.
Register:	7	15	B-registers; index registers.
Register:	1	30	X-register; arithmetic communication register.
Register:	1	15	S-register; holds storage address during storage references.
Register:	1	30	Z-register; operand buffer for storage references.
Register:	1	6	K-register; shift counter.
Register:	1	30	U-register; holds the instruction being executed.
Register:	2	30	R-registers; used for communication with index registers.
Register:	2	30	C-registers; communication buffer registers.

.242

Category of storage	Total number of locations	Physical form	Access time, μsec
Register:	19	flip-flops	overlapped with Core Memory access time.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . . 1 (P-register).

.314 Special sub-sequence counters: . . . . . none (during repeated instructions, Index Register 7 holds the repeat counter).

.315 Sequence control step size: . . . . . 1 word (2 words on skips).

.316 Accessibility to routines: . . . . . P-register contents can be stored in Core Memory by "Return Jump" instructions.

.317 Permanent or optional modifier: . . . . . no.

.32 Look-Ahead: . . . . . none.

.33 Interruption

.331 Possible causes—
- In-out units: . . . . . see next entry.
- In-out subsystems: . . completion of input-output operation or input-output error.
- Storage access: . . . . completion of magnetic drum operation or drum error.
- Processor errors: . . illegal function code.
- Other: . . . . . Delta Clock overflow; Delta Clock not updated.

.332 Control by routine—
- Individual control: . . can enable internal interrupts on any or all input-output channels by means of special input-ouput instructions. Internal interrupts occur when an input buffer is filled or an output buffer is emptied.
- Method: . . . . . when an interrupt occurs, all other non-error interrupts are disabled until they are re-enabled by a special instruction.
- Restriction: . . . . . error interrupts cannot be locked out.

.333 Operator control: . . . none.

.334 Interruption conditions: interrupt enabled.

.335 Interruption process—
- Disabling interruption: . . . . . automatic.
- Registers saved: . . . contents of P-register (sequence counter) are saved by "Return Jump" instruction; other registers by program.
- Destination: . . . . . one of 44 fixed locations, depending upon cause.

.336 Control methods—
- Determine cause: . . . automatic; destination depends upon cause.
- Enable interruption: . by special instruction contained in REX before returning to main program.

(Contd.)

.34 Multiprogramming

.341 Method of control: . . . by REX (see Section 800:191), using the interrupt facilities described above.
.342 Maximum number of programs: . . . . . limited only by hardware availability.
.343 Precedence rules: . . . see 800:191.12.
.344 Program protection—
Storage: . . . . . none.
In-outs units: . . . . . via assignment by REX of specific units to specific programs.

.35 Multi-sequencing: . . . practical only in multi-computer complexes.

.4 PROCESSOR SPEEDS

All processing times listed here are based on use of the standard 6-microsecond memory. With the optional 4.8-microsecond memory, UNIVAC 490 Processor speeds will be the same as those of the 491/492 Processors, as listed in Paragraph 802:051.4.

.41 Instruction Times in Microseconds

.411 Fixed point—
Add-subtract: . . . . . 12.0 †
Multiply: . . . . . 37.2 to 85.2
Divide: 86.4

.412 Floating point (using standard subroutines)—
Add: . . . . . 380.
Subtract: . . . . . 452.
Multiply: . . . . . 406.
Divide: . . . . . 446.

.413 Additional allowance for—
Indexing: . . . . . 0.
Indirect addressing: . 6 (jump instructions only).
Re-complementing: . . 0.

.414 Control—
Compare: . . . . . 12.0 †
Branch: 6.0
Compare and branch: 18.0 †

.415 Counter control—
Step and test: . . . . . 6.0 to 12.0
.416 Edit: . . . . . *
.417 Convert—
Decimal to binary: . . *
Binary to decimal: . . *
.418 Shift: . . . . . 7.2 to 15.6

† These times are based on use of operands in Core Memory. Times are shorter if the operand is a literal or is contained in the A- or Q-register.

* Performed by subroutines; timing data not available.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Fixed point
$c = a + b$:	36.0
$b = a + b$:	30.0
Sum N items:	12.0N
$c = ab$:	85.2
$c = a/b$:	110.4

.422 For arrays of data —

	Fixed point
$c_i = a_i + b_j$:	66.0
$b_j = a_i + b_j$:	60.0
Sum N items:	7.2N
$c = c + a_i b_j$:	121.2

.423 Branch based on comparison —
Numeric data: 81.6
Alphabetic data: . . . 81.6
.424 Switching
Unchecked: 24.0
Checked: 60.0
List search: . . . . . 33.6 + 7.2N
.425 Format control per character —
Unpack: . . . . . ?
Compose: . . . . . ?
.426 Table look-up per comparison —
For a match: 8.4
For interpolation . . point: 8.4
.427 Bit indicators —
Set bit in separate location: 24.0
Set bit in pattern: . . 30.0
Test bit in separate location: 12.0
Test bit in pattern: . 24.0
Test AND for B bits: . 48.0
Test OR for B bits: . 48.0
.428 Moving (per full word or half-word): . . . . . 12.0 (using repeated "Replace" instruction).

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	none	as programmed.
Zero divisor:	none	as programmed.
Invalid data:	none.	
Invalid operation:	check	interrupt.**
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	none.	
Dispatch of data:	none.	
Delta Clock not updated:	check	interrupt.**

** Branch to a specific location in Wired Memory occurs if Bootstrap switch is in "Automatic Recovery" position.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (801:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

Because the UNIVAC 490 can process several independent programs at the same time through multiprogramming, the amount of central processor time required by each program is highly significant. The difference (if any) between the total elapsed time for a particular run and the amount of central processor time required for that run represents processor time that is potentially available to other programs. Whether or not this processor time can be efficiently utilized depends upon the system configuration, the over-all problem mix, and the effectiveness of the scheduling and operating system.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configurations VIIA and VIIIA, where all four input-output files are on magnetic tape, total times were computed for cases using both unblocked and blocked records in the detail and report files. Central processor time is essentially the same for all configurations, and is shown by the line marked "CP" on each graph. No addition has been made to the processor time to cover the overhead requirements of the operating system.

Worksheet Data Table 1 (page 801:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for Configurations III and V. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a fraction of the total processing time. When other programs with limited input and output can be run simultaneously in order to utilize the remaining processor time, it may be satisfactory to operate the UNIVAC 490 as just described. In other cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-print transcription of the report file. The curves for Configurations VIIA and VIIIA show the time required for the all-tape main processing run. The card-to-tape and tape-to-printer transcriptions will run at card reader and printer-limited speeds, and their demands on the processor will be small. The elapsed time and central processor time for the data transcription runs are shown on a separate graph (801:201.150). It should be noted that in the case of Configurations VIIA and VIIIA, the central processor time, rather than the input-output time, is the controlling factor whether the detail and report files are blocked or unblocked.

The master file record format is a mixture of alphameric and binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. Even so, most of the central processor time is devoted to editing, radix conversion, and character manipulation operations. Packing was kept to a minimum because of the high demands it would place upon the UNIVAC 490 central processor. The resulting master file record length is 21 words (the equivalent of 105 6-bit characters).

SORTING (801:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the Users' Guide, Paragraph 4:200.213, using a three-way merge.

MATRIX INVERSION (801:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplication ($c = c + a_i b_j$) using the standard single-precision floating-point subroutines. The processor time required for a matrix inversion can be spread over a much longer total elapsed time when the inversion is multi-run with other programs that utilize the available input-output equipment. Multi-running of other programs necessarily decreases the amount of internal storage that can be allocated to the matrix inversion.

GENERALIZED MATHEMATICAL PROCESSING (801:201.4)

The standard estimating procedure outlined in the Users' Guide, Paragraph 4:200.413, was used. Computation includes 5 fifth-order polynomials, 5 divisions and 1 square root, all of which were timed using SPURT floating-point subroutines.

WORKSHEET DATA TABLE 1

	ITEM		CONFIGURATION								REFERENCE
			III, V		VIIA & VIIIA, Files 3 & 4 Blocked*			VIIA & VIIIA, Files 3 & 4 Unblocked			
1 Input-Output Times	Char/block	(File 1)	1,050		1,050			1,050			4:200.112
	Records/block	K (File 1)	10		10			10			
	msec/block	File 1 = File 2	69.5		15.9			15.9			
		File 3	100.0		13.9*			8.1			
		File 4	127.7		17.4*			8.5			
	msec/switch	File 1 = File 2	0		0			0			
		File 3	0		0			0			
		File 4	0		0			0			
	msec penalty	File 1 = File 2	3.78		3.78			3.78			
		File 3	0.29		2.88*			0.29			
		File 4	0.47		4.88*			0.47			
2 Central Processor Time	msec/block	a_1	0.22		0.22			0.22			4:200.1132
	msec/record	a_2	0.59		0.59			0.59			
	msec/detail	b_6	3.77		3.77			3.77			
	msec/work	$b_5 + b_9$	1.00		1.00			1.00			
	msec/report	$b_7 + b_8$	8.62		8.62			8.62			
3 Standard File Problem A F = 1.0	msec/block for C.P. and dominant column.		C.P.	Printer	C.P.	VIIA	VIIIA	C.P.	VIIA	VIIIA	4:200.114
		a_1	0.2		0.2			0.2			
		a_2K	5.9		5.9			5.9			
		a_3K	133.9		133.9			133.9			
		File 1: Master In	3.8		3.8	15.9		3.8	15.9		
		File 2: Master Out	3.8		3.8			3.8			
		File 3: Details	2.9		2.9			2.9			
		File 4: Reports	4.7	1,277.	4.7	17.4	17.4	4.7	85.0	85.0	
		Total	155.2	1,277.	155.2	33.3	17.4	155.2	100.9	85.0	
4 Standard File Problem A Space	Unit of measure	(30-bit words)									4:200.1151
		Std. routines	4,000**		4,000**			4,000**			
		Fixed	-		-			-			
		3(Blocks 1 to 23)	165		165			165			
		6(Blocks 24 to 48)	2,346		2,406			2,346			
		Files	924		1,680			924			
		Working	50		50			50			
		Total	7,485		8,306			7,485			

	ITEM		CONFIGURATION		REFERENCE
			III, V	VIIA, VIIIA	
5 Standard Mathematical Problem A	Fixed/Floating point		Floating (subroutines)	Floating (subroutines)	4:200.413
	Unit name	input	600-cpm reader	Uniservo IIIA	
		output	700/922-1pm printer	Uniservo IIIA	
	Size of record	input	80 char	80 char	
		output	135 char	132 char	
	msec/block	input T_1	100.0	8.1	
		output T_2	127.7	8.5	
	msec/penalty	input T_3	0.29	0.29	
		output T_4	0.47	0.47	
	msec/record	T_5	13.2	13.2	
	msec/5 loops	T_6	35.5	35.5	
	msec/report	T_7	9.1	9.1	

* 10 records per block in Files 3 (detail) and 4 (report).
** 4,000 words are generally reserved for REX.

(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes —
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

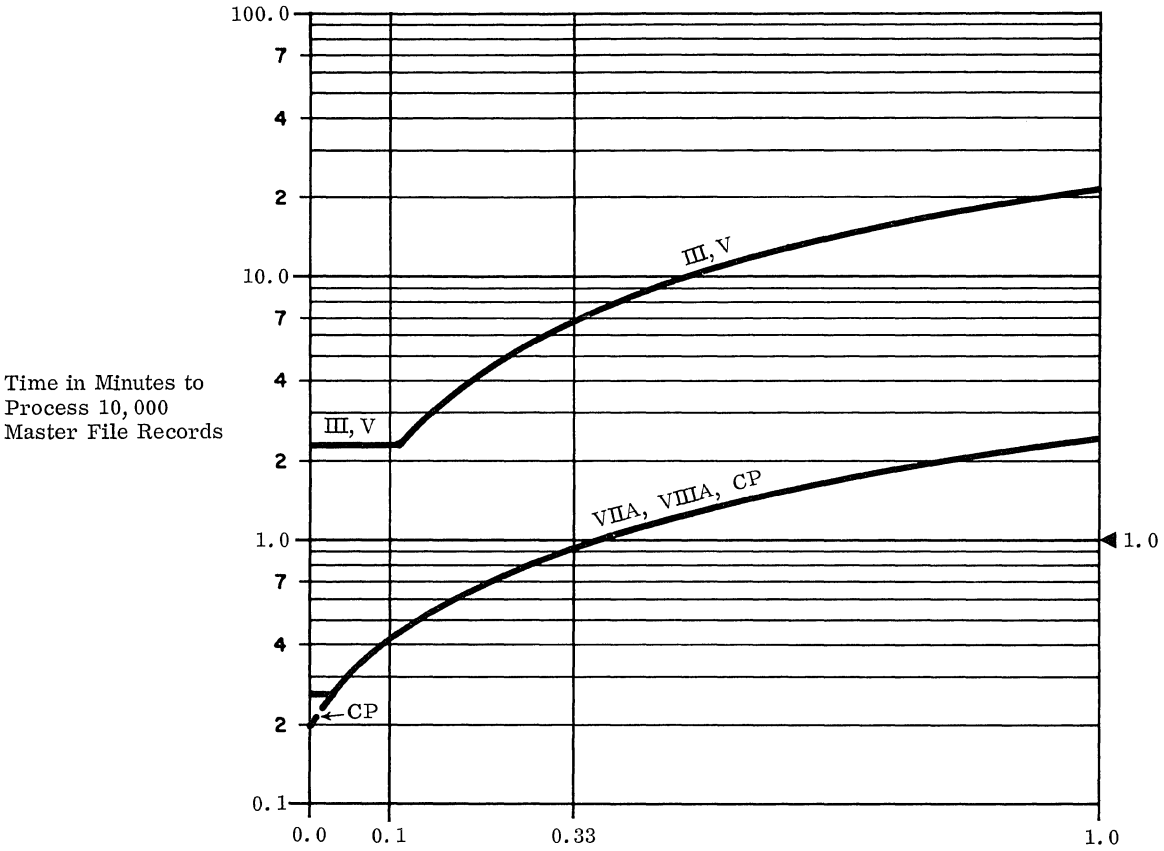
.112 Computation: . . . . . standard.

.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . . see graph below.

.115 Storage space required —
Configurations III; V: 7,500 words.*
Configurations VIIA, VIIIA (unblocked Files 3 & 4): . . . . . 7,500 words.*
Configurations VIIA, VIIIA (blocked Files 3 & 4): . . . . 8,300 words.*

* Includes 4,000 words reserved for REX system.

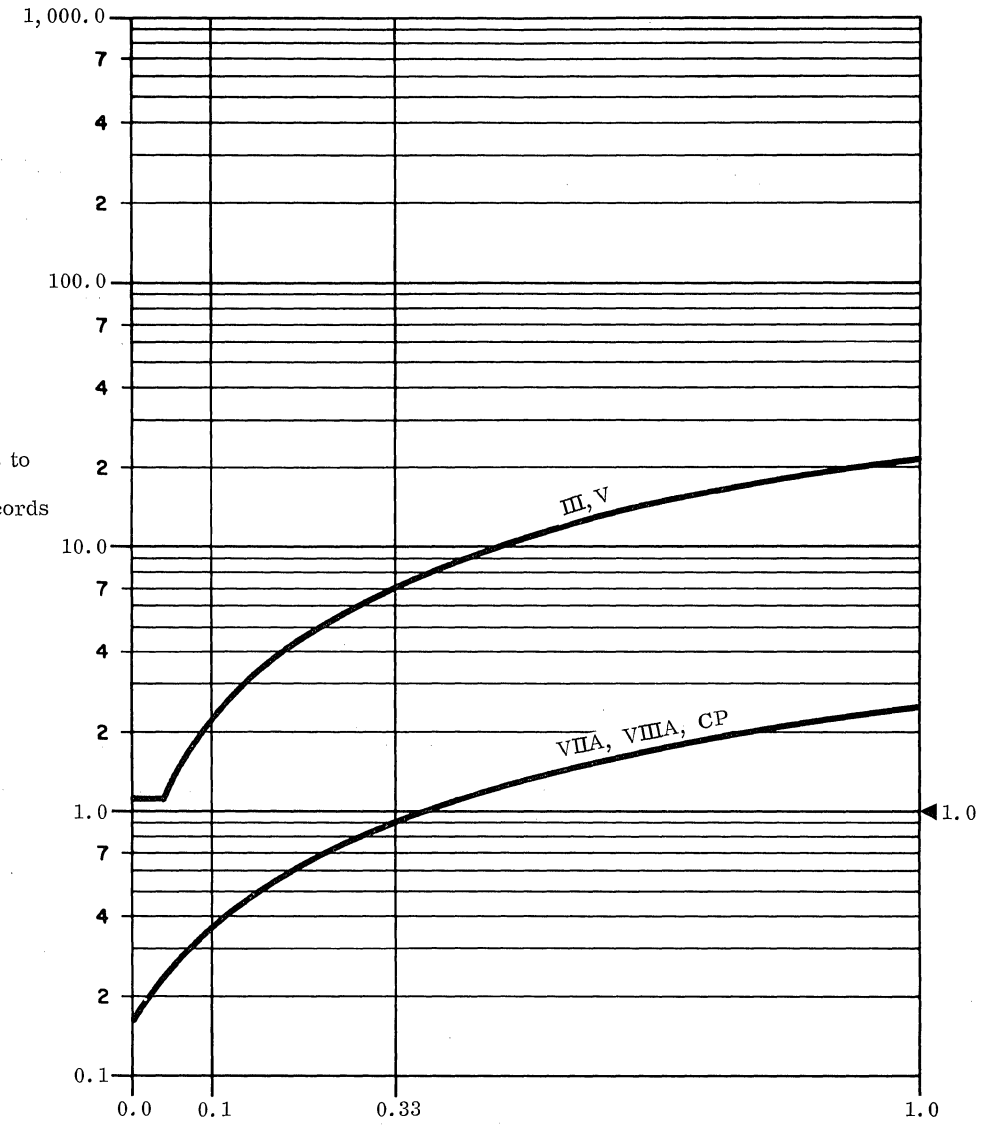


(Roman numerals denote standard System Configurations; "CP" denotes Central Processor time for all configurations.)

.12 Standard File Problem B

.121 Record sizes —
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



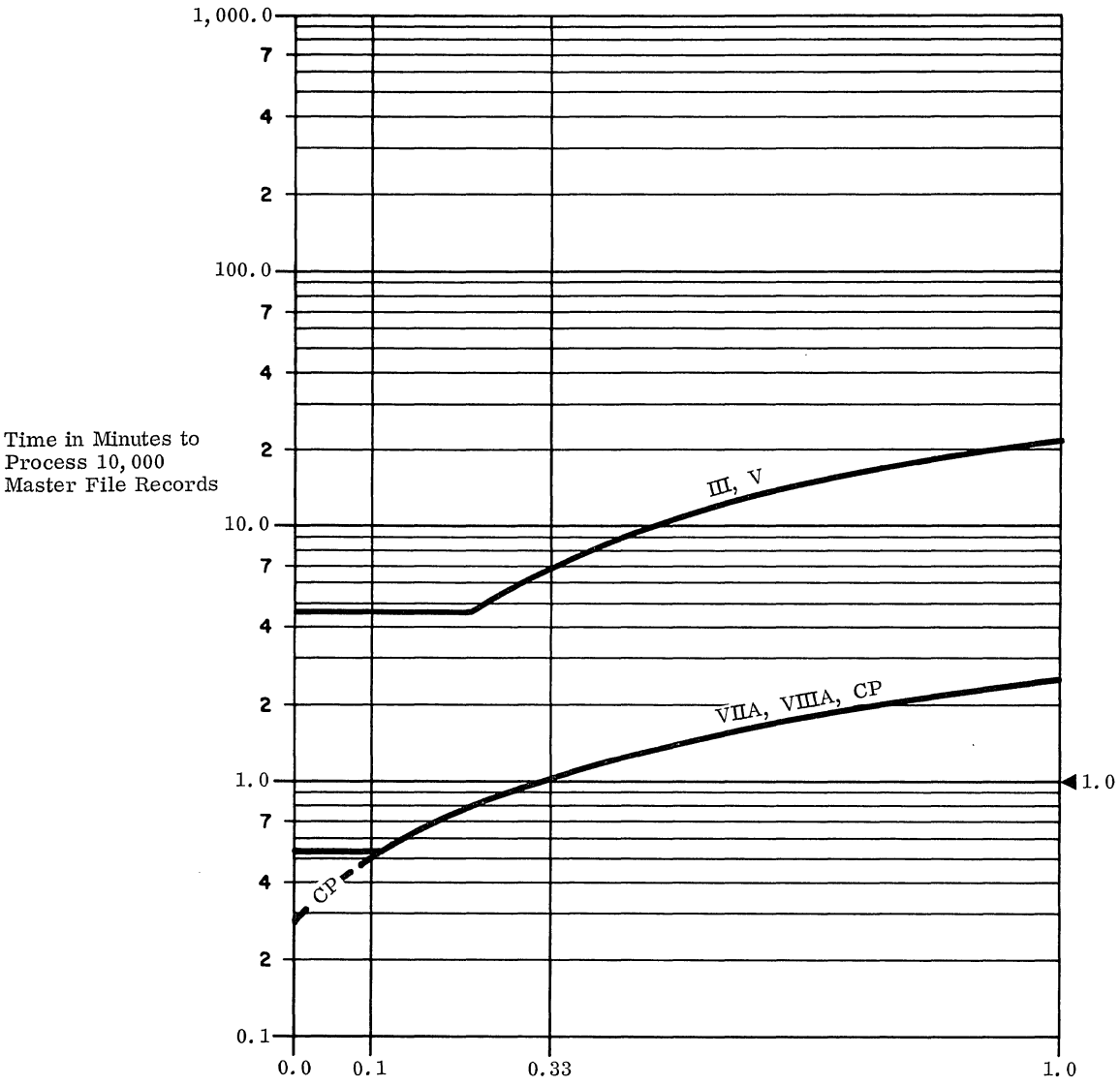
(Roman numerals denote standard System Configurations; "CP" denotes Central Processor time for all configurations.)

(Contd.)

.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.

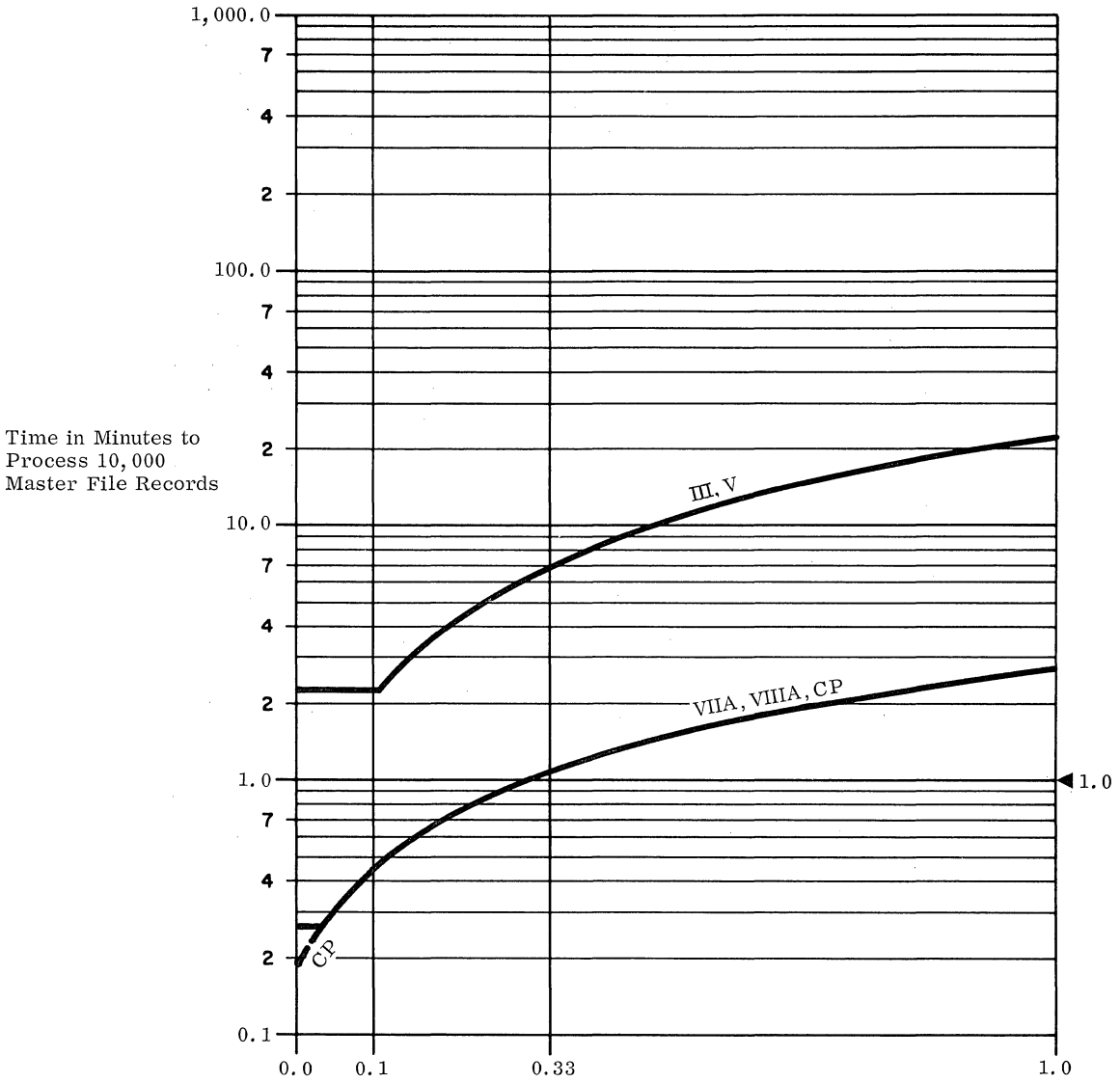


(Roman numerals denote standard System Configurations; "CP" denotes Central Processor time for all configurations.)

.14 Standard File Problem D

.141 Record sizes —
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations; "CP" denotes Central Processor time for all configurations.)

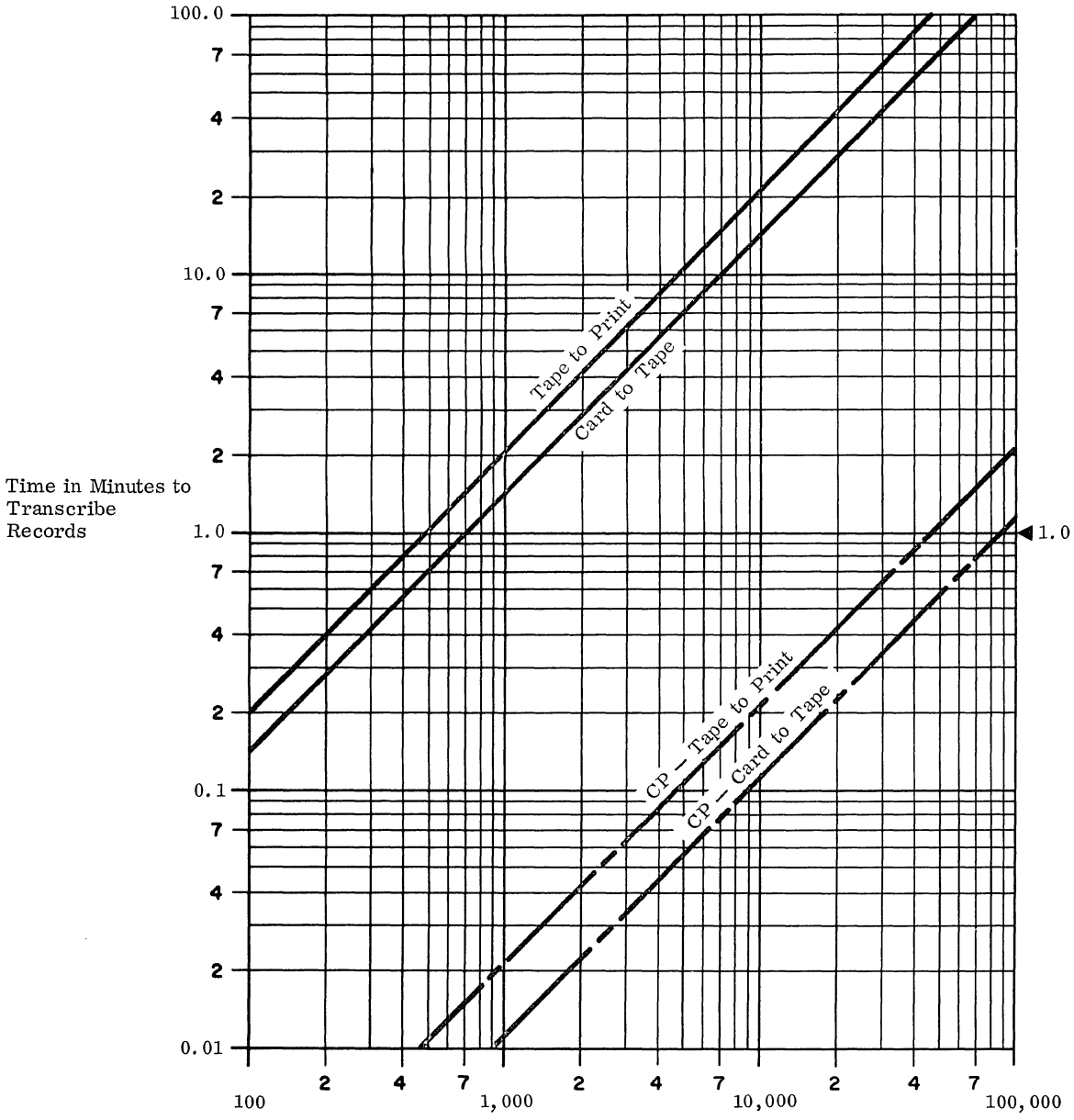
(Contd.)

.15 Data Transcription Runs for Standard File Problems

.151 Block sizes:
Detail file (on cards): one card.
Report file (on printer): . . . . . one print line.

.153 Timing basis: . . . . . data is transcribed directly from cards to tape or tape to printer; no editing is performed during these runs.

.154 Graph: . . . . . see graph below.



(Graph applies to Standard Configurations VIIA and VIIIA; curves marked "CP" denote Central Processor times.)

.2 SORTING

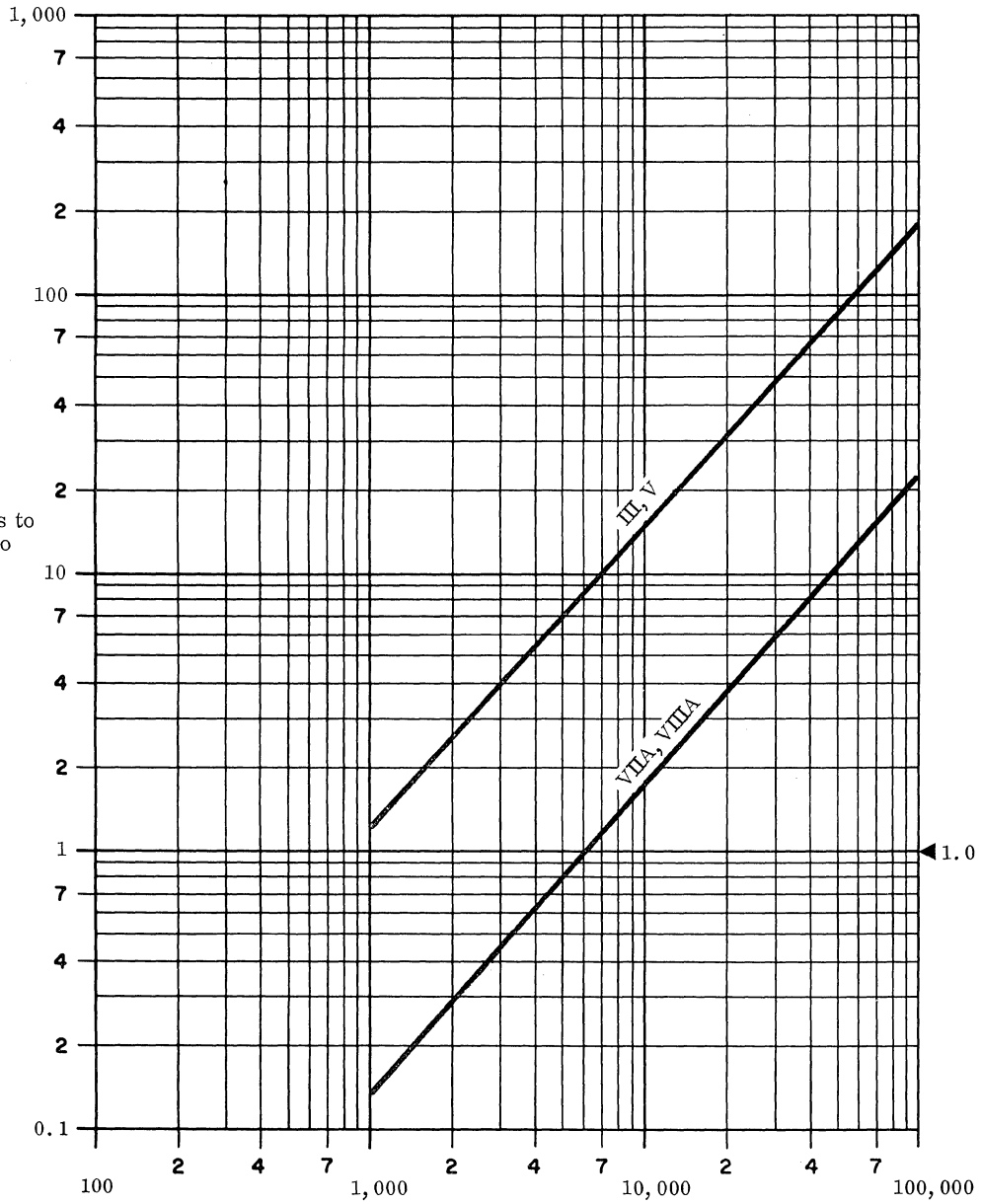
.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.

.212 Key size: . . . . . 8 characters.

.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . . see graph below, based upon 3-way merge.



Time in Minutes to Put Records into Required Order

Number of Records

(Roman numerals denote standard System Configurations.)

(Contd.)

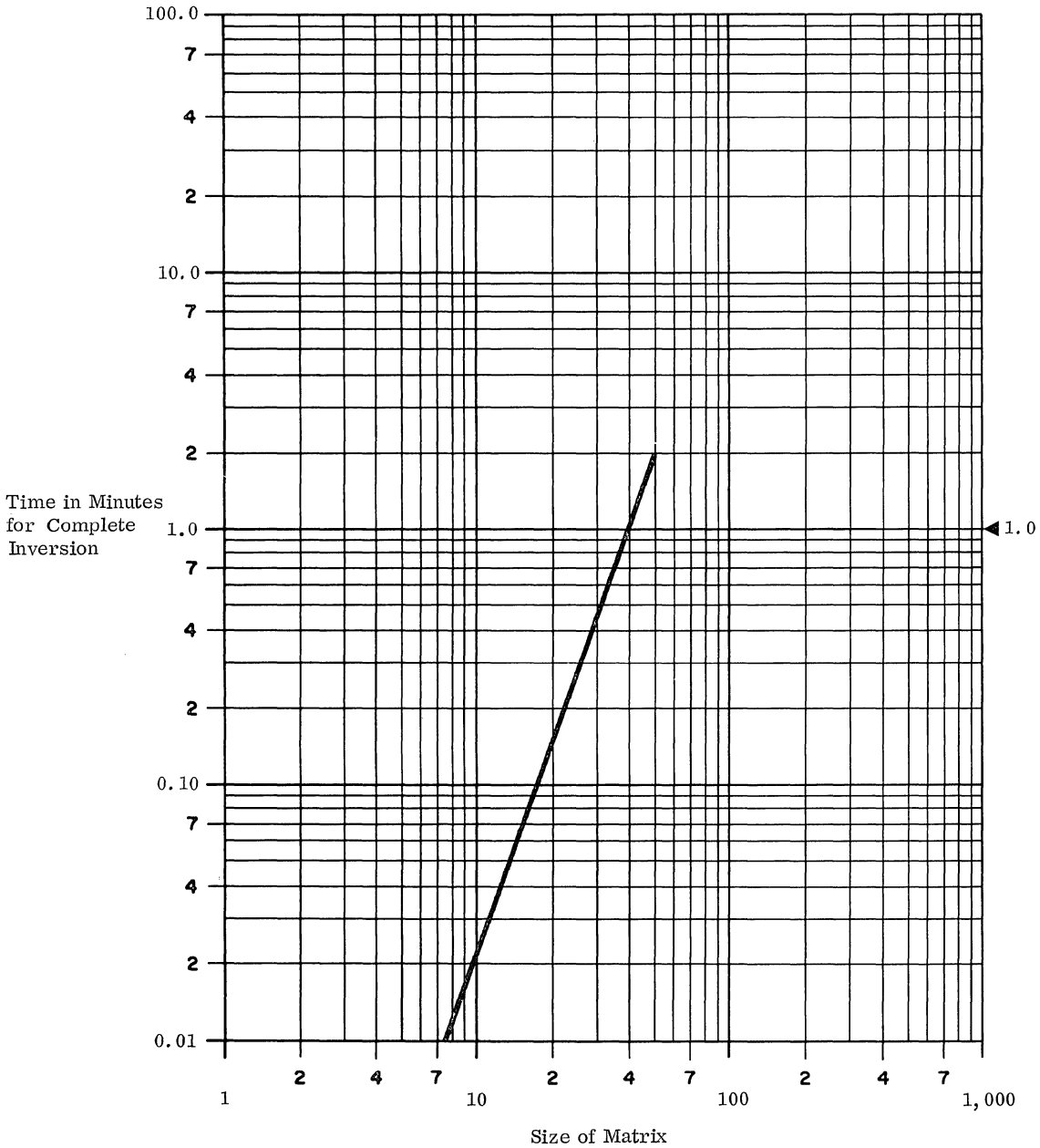
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312; times are based on standard floating-point arithmetic routines.

.313 Graph: . . . . . see graph below.



.4 GENERALIZED MATHEMATICAL PROCESSING

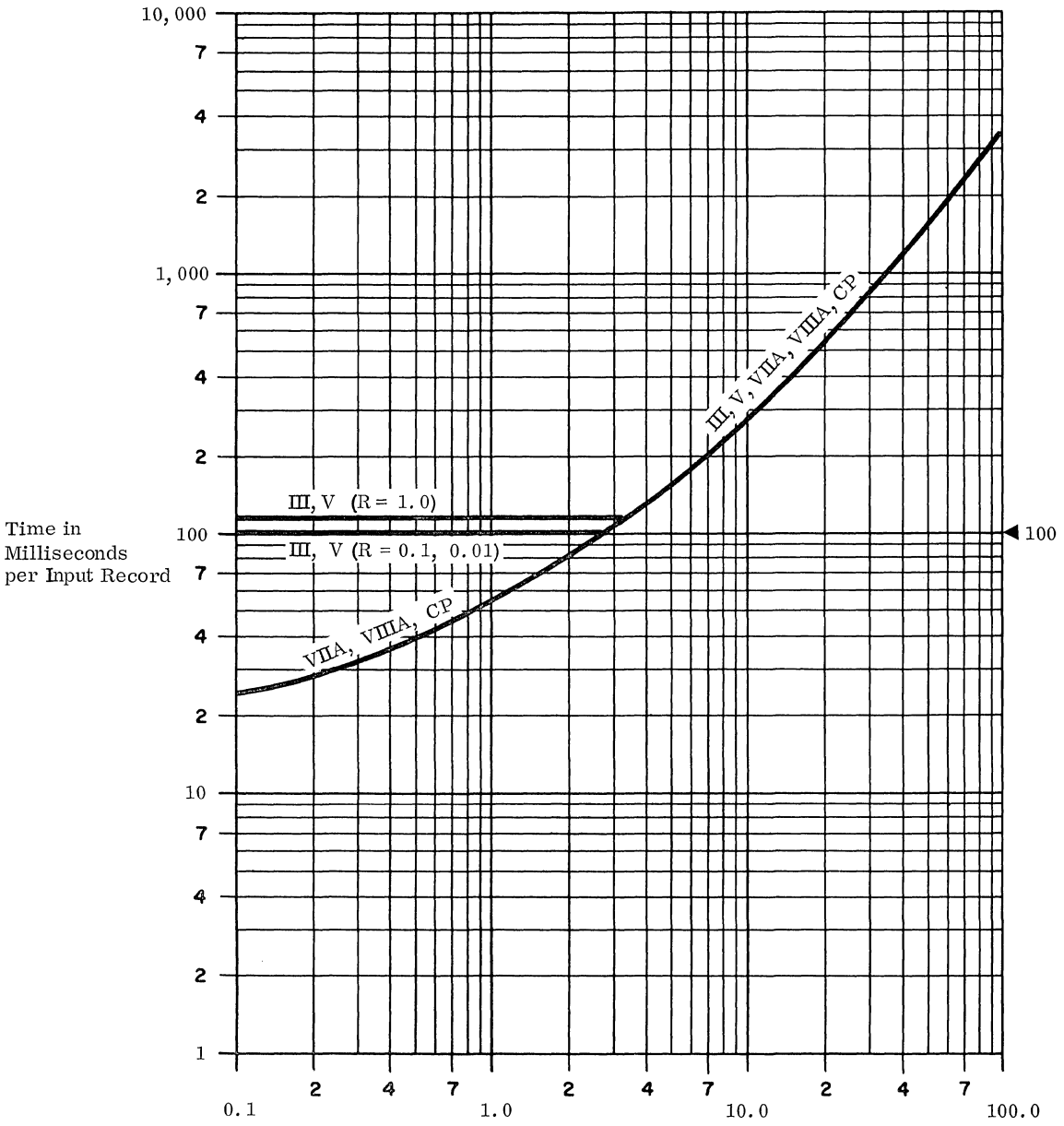
.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . 10 signed numbers; average size 5 digits, maximum size 8 digits.

.412 Computation: . . . . . 5 fifth-order polynomials, 5 divisions, and 1 square root; computation is performed in 8-digit-precision floating-point mode, using subroutines.

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations; R=number of output records per input record; curve marked "CP" shows Central Processor time.)

PRICE DATA: UNIVAC 490

UNIVAC 490 computer systems are no longer being actively marketed; the following prices were those in effect while the system was in production. For price data on the UNIVAC 491, 492, and 494 systems, please turn to Page 800:221.101.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR		UNIVAC 490 Central Processor (Including Control Console, Motor Alternator, and Power Control Cabinet)			
		With 16,384 Core Memory locations & 6 I/O Channels	9,500	1,300*	427,500
		With 16,384 Core Memory locations & 14 I/O Channels	10,000	1,365*	450,000
		With 32,768 Core Memory locations & 6 I/O Channels	13,500	1,340*	580,000
		With 32,768 Core Memory locations & 14 I/O Channels	14,000	1,390*	602,000
		4.8-Microsecond Accelerator Package			
		For 16,384 Core Memory locations	250	—	10,000
		For 32,768 Core Memory locations	500	—	20,000
INTERNAL STORAGE		Core Memory			
		See Central Processor, above			
		FH-880 Magnetic Drum Subsystem			
	8112	FH-880 Drum	2,000	165	92,000
	8122	FH-880 Control & Synchronizer	1,420	165	71,000
		Fastrand Mass Storage Subsystem			
	8206	Fastrand Storage Unit	3,300	†	160,000
	8205	Fastrand Synchronizer	2,750	100	135,000
INPUT-OUTPUT		Uniservo IIA Subsystem			
	8143	Uniservo IIA Magnetic Tape Handler	450	95	20,000
	8113	Uniservo IIA Control & Synchronizer	1,530	130	76,500
	8142	Uniservo IIA Power Supply	550	40	25,300
		Uniservo IIIA Subsystem			
	8011	Uniservo IIIA Magnetic Tape Handler	750	155	36,500
	8003-1	Uniservo IIIA Control & Synchronizer (Single Channel)	3,700	170	177,600
	8003-3, 8003-5	Uniservo IIIA Control & Synchronizer (Dual Channel)	4,800	260	230,400
	8142	Uniservo IIIA Power Supply	550	40	25,300

† $250 for first unit; $120 for each additional unit.

* Applicable only when Central Processor is used for batch processing applications; maintenance charges for real-time applications available upon request.

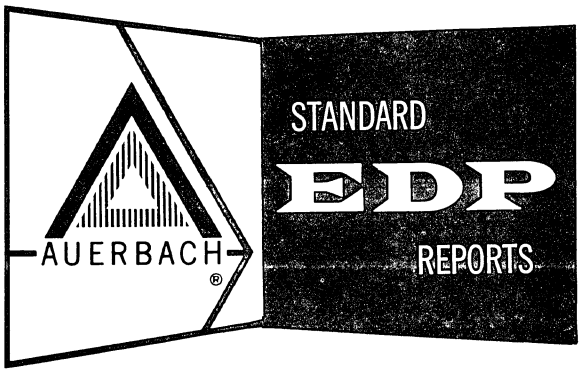
CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd.)		Uniservo IIIC Subsystem			
	8220	Uniservo IIIC Magnetic Tape Handler	800	62	38,400
	8208	Uniservo IIIC Tape Adapter Cabinet	1,000	50	48,000
	8209	Uniservo IIIC Control & Synchronizer	2,250	173	108,000
	8142	Uniservo IIIC Power Supply	550	40	25,300
		Punched Card Subsystem			
	8114	Card Reader (600 CPM)	350	75	17,500
	8124	Card Punch (150 CPM)	500	180	25,000
	8104	Card Control & Synchronizer	1,600	230	80,000
		Paper Tape Subsystem			
	8136	(Paper tape reader, punch and control unit)	645	110	32,250
		High-Speed Printer Subsystem			
	8121	Printer (700-922 LPM)	800	240	36,000
	8120-00	Printer Control & Synchronizer (700-922 LPM)	1,750	160	80,000
		Communication Line Terminals			
	CLT-50L	Low speed output (5 level)	25	#	1,125
	CLT-51L	Low speed input (5 level)	20		900
	CLT-80L	Low speed output (6, 7, 8 level)	30		1,350
	CLT-81L	Low speed input (6, 7, 8 level)	25		1,125
	CLT-80M	Medium speed output	35		1,575
	CLT-81M	Medium speed input	25		1,125
	CLT-80H	High speed output	45		2,025
	CLT-81H	High speed input	45		2,025
	CLT-80P	Parallel output	35		1,575
	CLT-81P	Parallel input	35		1,575
	CLT-Dialing	Automatic Dialing Unit	20		900
		Communication Multiplexers			
	C/M-4	For up to 4 CLTs	675	#	30,375
	C/M-8	For up to 8 CLTs	725		32,625
	C/M-16	For up to 16 CLTs	800		36,000
	C/M-32	For up to 32 CLTs	1,000		45,000
	C/M-64	For up to 64 CLTs	1,300		58,500
		Communication Scanner/Selectors			
	8150	4 Channels	800	#	36,000
	8151	8 Channels	1,000		45,000
	8152	12 Channels	1,250		56,250
	8153	16 Channels	1,500		67,500

Monthly maintenance charges will be quoted by the manufacturer upon request.

UNIVAC 491/492

Univac

(A Division of Sperry Rand Corporation)



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UNIVAC 491/492

Univac

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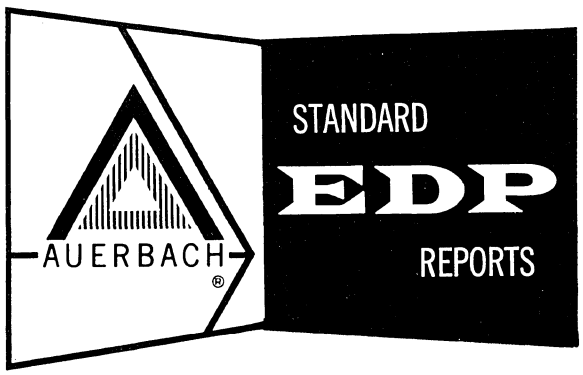

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INTRODUCTION

The UNIVAC 491 and 492 computer systems were announced in June 1965, and the first official customer delivery was made in December 1965. The 491 and 492 Central Processors differ only in the number of input-output channels (the 492 has 6 more) and in price (the 492's monthly rental is higher by $1,750).

Among the characteristics of the UNIVAC 491 and 492 systems that distinguish them from the other members of the 490 Series are the following:

- A core storage cycle time of 4.8 microseconds.
- Core storage capacities of 16,384 to 65,536 30-bit words.
- An instruction repertoire consisting of 62 basic instructions.*
- The absence of direct facilities for floating-point, double-precision, and decimal arithmetic.*
- A core storage protection facility that permits individual 1,024-word blocks to be guarded against unauthorized access.
- The absence of a parity check on core storage operations.*
- In the 491 Central Processor, a total of 8 input-ouput channels, 6 of which are available for general-purpose use.
- In the 492 Central Processor, a total of 14 input-output channels, 12 of which are available for general-purpose use.
- Inability to utilize the high-performance FH-432 and FH-1782 Magnetic Drums.*

This subreport concentrates upon the characteristics and performance of the UNIVAC 491 and 492 Central Processors and systems based upon them. All general characteristics of the 490 Series hardware and software are described in Computer System Report 800: UNIVAC 490 Series — General.

The System Configuration section that follows shows UNIVAC 491/492 systems arranged in a number of standardized configurations, according to the rules in the Users' Guide, page 4:030.120. These standardized equipment configurations form the basis for a detailed analysis of the overall System Performance of the UNIVAC 491/492 on our standard benchmark problems, the results of which are presented in Section 802:201.

Section 802:051 contains a detailed description of the UNIVAC 491/492 Central Processor, its processing facilities, and its execution times for a series of standardized tasks.

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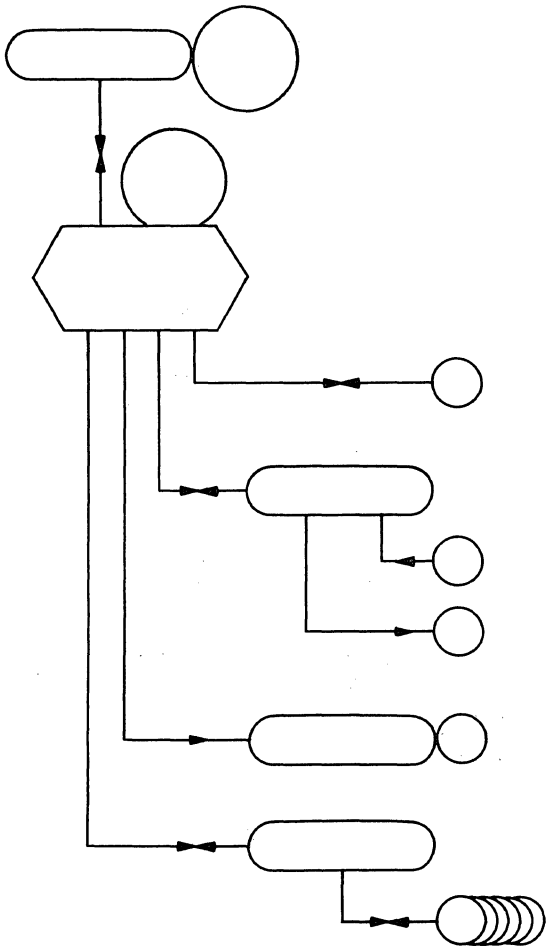
* These characteristics are shared by the original UNIVAC 490 system described in the preceding subreport.

SYSTEM CONFIGURATION

For overall configuration rules, refer to Page 800:031.100.

.1 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

Deviations from Standard Configuration: . . . . . core storage is 350% larger.
card reader is 60% faster.
card punch is 200% faster.
printer is 40% faster.
4 more index registers.
auxiliary storage (Fastrand II) is 448% larger.



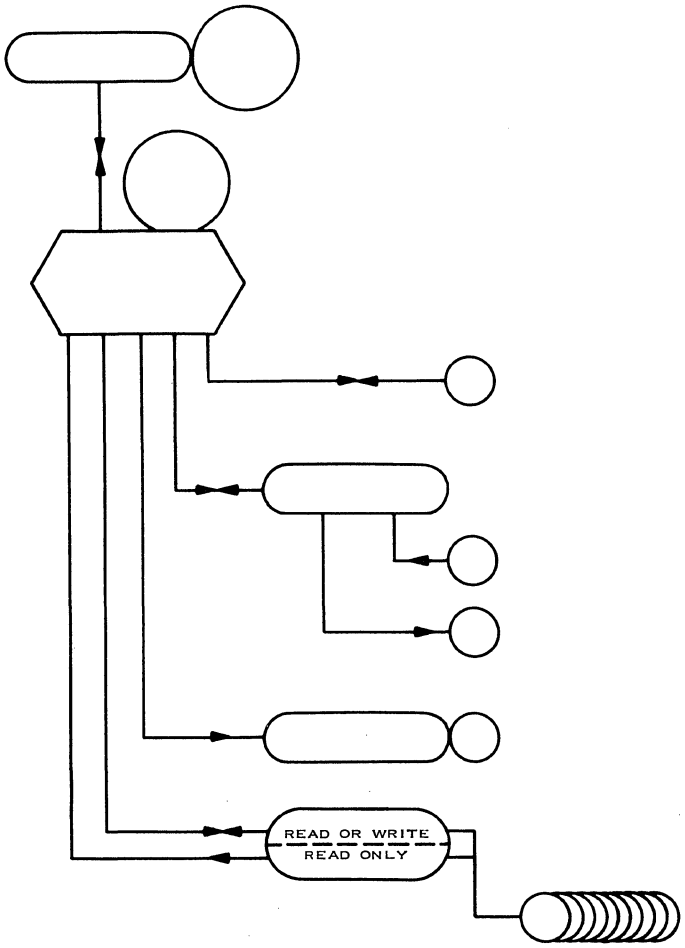
Equipment	Rental
Fastrand II Storage Unit & Synchronizer: 25,952,256 words	$ 5,000
Core Memory: 16,384 words	
Central Processor (UNIVAC 491)	7,000
Console	
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Printer & Synchronizer: 700/922 lines/min.	1,550
Uniservo VIC Auxiliary Control & Synchronizer	700
2 Uniservo Simultaneous Master Units	1,100
4 Uniservo Slave Units: 34,200 char/sec.	1,200
TOTAL RENTAL:	$18,345

Notes: 1. Standard Configuration III is the same as Configuration V (shown here) less Fastrand Storage Unit and Synchronizer; its rental is $13,345 per month.

2. Configuration V, with the addition of a Communication Terminal Module Controller and up to 16 Communication Terminal Modules, each having 2 input and 2 output lines, represents a typical 491/492 communications system. The total monthly rental of such a system — including 16 medium-speed asynchronous Communication Line Terminals — is $20,195.

.2 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . . magnetic drum is required by most software systems.
core storage is 24% smaller.
magnetic tape is 60% faster.
card reader is 60% faster.
card punch is 200% faster.
printer is 40% faster.
floating-point hardware is not available.

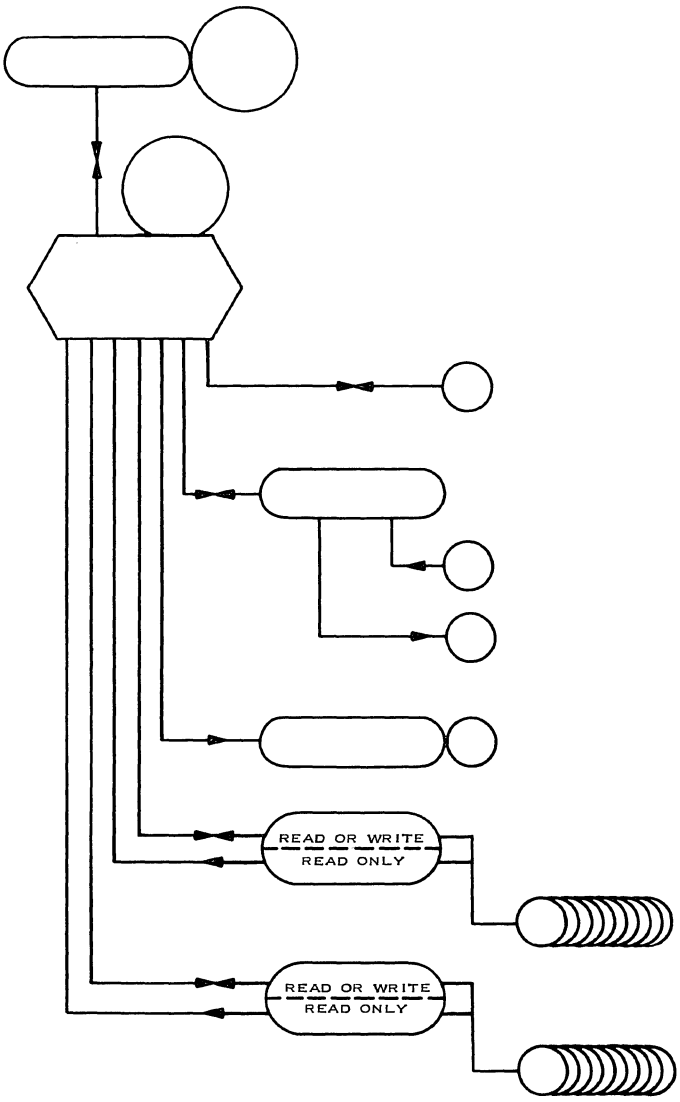


Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$ 3,420
Core Memory: 16,384 words Central Processor (UNIVAC 491) Console	7,000
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Printer & Synchronizer: 700/922 lines/min.	1,550
Uniservo VIIIC Synchronizer: dual-channel model	1,450
Uniservo VIIIC Tape Units (10): 96,000 char/sec.	8,500
TOTAL RENTAL:	$ 23,715

(Contd.)

.3 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: . . . . . magnetic drum is required by most software systems.
core storage is 14% larger.
magnetic tape is 23% slower.
printer is 20% slower.
card reader is 15% slower.
card punch is 67% faster.
floating-point hardware is not available.



Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$ 3,420
Core Memory: 49,152 words	15,250
Central Processor (UNIVAC 492)	
Console	
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Printer & Synchronizer: 700/922 lines/min.	1,550
Uniservo VIIIC Synchronizer: dual-channel model	1,450
Uniservo VIIIC Tape Units (10): 96,000 char/sec.	8,500
Uniservo VIIIC Synchronizer; dual-channel model	1,450
Uniservo VIIIC Tape Units (10): 96,000 char/sec.	8,500
TOTAL RENTAL:	$ 41,915

CENTRAL PROCESSOR: UNIVAC 491/492

.1 GENERAL

.11 Identity: . . . . . UNIVAC 491 Central Processor. UNIVAC 492 Central Processor. Types 8187-88 through 8187-99.

.12 Description

The Central Processor used with the UNIVAC 491 and 492 computer systems is a single cabinet that houses the system's solid-state arithmetic and control circuits, 16 word locations of Wired Memory, and 16,384, 32,768, or 65,536 word locations of Core Memory with a cycle time of 4.8 microseconds. The principal difference between the 491 and 492 Central Processors lies in the fact that the 492 is capable of controlling up to 12 general-purpose input-output channels, as contrasted with the 491's capability of controlling only 6 general-purpose channels. The Central Processor used with the original UNIVAC 490 computer system is described in Section 801:051; the Central Processor used with the more powerful UNIVAC 494 computer system is analyzed in Section 804:051.

Each instruction of the UNIVAC 491/492 Central Processor is one word (30 bits) in length and consists of five parts called "designators," as shown below.

Designator:	f	j	k	b	y
Size (bits):	6	3	3	3	15

- The 6-bit f-designator specifies the basic operation to be performed.
- The 3-bit j-designator usually specifies the conditions under which a skip or jump will be performed (e.g., when contents of an arithmetic register are positive, negative, zero, or nonzero). It can also specify the mode for a "Repeat" instruction, or the index register to be used in a loop control instruction. (In input-output instructions, the j-designator is 4 bits long and specifies the channel to be used.
- The 3-bit k-designator shows how the operand is to be derived from the y-designator part; e.g., the operand of a load instruction can be y itself, all or either half of the Core Memory location specified by y, or the contents of the accumulator. (In input-output instructions, the k-designator is only 2 bits long, but its function is similar.)
- The 3-bit b-designator specifies one (or none) of seven index registers, whose contents are to be added to the y-designator part to form the operand or its address.
- The 15-bit y-designator specifies the base operand address, a literal operand, or a shift count.

There are 62 basic instructions, each with up to 64 distinct variations made possible by the j- and k-designators. The j-designator in most instructions can cause a conditional skip of the next instruction, depending upon the sign of the A-register (accumulator) or Q-register after the specified operation has been performed. The k-designator in most instructions can specify whether the operand shall consist of all 30 bits or only the high-order or low-order 15 bits of the Core Memory location specified by the y-designator. Where half-word operands are specified, sign extension is optional.

The UNIVAC 491/492 instruction repertoire includes a full complement of fixed point arithmetic, Boolean, comparison, and shift operations on 30-bit binary operands. Thirteen different "Replace" instructions provide many of the capabilities of two-address, "add-to-storage" processors; e.g., by means of a single instruction, the contents of the accumulator can be added to (or subtracted from) the contents of a specified Core Memory location and the result placed in both the accumulator and the specified Core Memory location. The "Repeat" instruction causes the instruction immediately following it to be executed from 0 to 32,767 times, with or without index register modification prior to each execution. The Repeat capability permits efficient table look-up operations. Special instructions are provided to load, store, test, and increment (by +1 or -1 only) the contents of the seven index registers.

Facilities not directly provided in the instruction repertoire include editing, double precision arithmetic, decimal arithmetic, floating point arithmetic, multi-word internal transfers, and radix conversions. Generalized subroutines or complex sequences of instructions are therefore required to accomplish these important operations.

Execution time is 9.6 microseconds for most UNIVAC 491/492 instructions that reference an operand in Core Memory. When the operand is contained in the instruction itself (as a 15-bit literal) or in the accumulator or Q-register, the execution time is generally lower. Address modification by indexing does not increase instruction execution times. Average execution time is about 8 microseconds per instruction.

Program interrupts occur upon normal completion of an input-output operation (optional), upon detection of an input-output or processor error, upon attempted violation of preset memory boundaries, and upon overflow of the program-accessible delta clock. Control is transferred to one of 44 fixed locations, depending upon the cause of interruption. Only the contents of the instruction sequence counter can be automatically saved when an interrupt occurs, so the routine that services the interrupt

.12 Description (Contd.)

condition (usually REX) must preserve and restore the previous contents of all the registers it uses. The interrupt facility makes it possible to run one or more batch programs concurrently with a real-time program, under control of the Real-Time Executive Routine (REX), described in Section 800:191.

The UNIVAC 491/492 Central Processor has three electronic chronometers. The Real-Time Clock occupies the lower half of octal location 00017, is incremented each millisecond, and recycles back to zero every 32,768 milliseconds. The Delta Clock occupies the upper half of octal location 00017, counts each millisecond, and can be set by the program to initiate an interrupt after any time interval from 1 to 32,768 milliseconds. The Day Clock is connected to one of the two "computer-to-computer" data channels, is controlled by REX, and presents the time of day (in hours and minutes) via an interrupt each minute.

.13 Availability: . . . . . 9 months.

.14 First Delivery: . . . . . December, 1965.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point —			
Add-subtract:	automatic	binary	29 bits + sign.
Multiply —			
Short:	none.		
Long:	automatic	binary	29 bits + sign (60-bit product).
Divide —			
No remainder:	none.		
Remainder:	automatic	binary	29 bits + sign (60-bit dividend).
.212 Floating point —			
Add-subtract:	subroutine	binary	fraction: 28 bits + sign. exponent: 15 bits + sign.
Multiply:	subroutine		
Divide:	subroutine		
.213 Boolean —			
AND:	automatic	binary	30 bits.
Inclusive OR:	automatic		
Exclusive OR:	automatic		
.214 Comparison —			
Numbers:	automatic		30 bits.
Letters:	automatic		30 bits (6 chars).
Mixed:	automatic		30 bits (6 chars).
Collating sequence:	see Data Code Table, Section 800:141.		

	Provision	Comment	Size
.215 Code translation:	none	performed by subroutines.	
.216 Radix conversion:	none		
.217 Edit format —			
Alter size:	none		
Suppress zero:	none		
Round off:	none		
Insert point:	none		
Insert spaces:	none		
Insert commas:	none		
Float $, +, -:	none		
Protection:	none		
.218 Table look-up —			
Equality:	none.		
Greater than:	semi-automatic through use of "Repeat" instruction		30 bits.
Less than or equal:			
Within limits:			
Greatest:	none.		
Least:	none.		

(Contd.)

	Provision	Comment	Size
.219 Others —			
Shifts:	automatic	left shifts are circular; right shifts with sign extension	30 or 60 bits.
Add to storage:	automatic	---	29 bits + sign.
Subtract from storage:	automatic	---	29 bits + sign.
Repeat:	automatic	executes next instruction specified number of times.	

.22 Special Cases of Operands

.221 Negative numbers: . . one's complement.
.222 Zero: . . . . . +0 and -0 have zeros and ones, respectively, in all 30 bit positions; they are considered unequal in compare and certain arithmetic operations.
.223 Operand size determination: . . . k-designator in most instructions specifies full word (30 bits), upper or lower half-word (15 bits), or literal operand (15 bits).

.23 Instruction Formats

.231 Instruction structure: 1 word.
.232 Instruction layout:

Name:	f	j (or j*)	k (or k*)	b	y
Size (bits):	6	3(or 4)	3(or 2)	3	15

.233 Instruction parts —

Name	Purpose
f-designator:	specifies operation code.
j-designator:	specifies skip or jump condition, or special register.
j*-designator (I/O instruction):	specifies input or output channel.
k-designator:	controls the procedure by which the operand is derived.
k*-designator (I/O instruction):	controls procurement and/or storing of the operand.
b-designator:	specifies 1 (or none) of 7 Index Registers, whose contents are added to y.
y-designator:	specifies an operand address or a literal operand.

.234 Basic address structure: . . . . . 1 + 0.

.235 Literals —
Arithmetic: . . . . . 15 bits (i.e., up to 32,767).
Comparisons and tests: . . . . . 15 bits.
Incrementing modifiers: . . . . 15 bits.

.236 Directly addressed operands —

Internal storage type	Minimum size	Maximum size	Volume accessible
Core Memory:	15 bits	1 word	total capacity (16,384 or 32,768 words).
Wired Memory:	15 bits	1 word	16 words.

.237 Address indexing —
.2371 Number of methods: 1.
.2372 Name: . . . . . indexing.
.2373 Indexing rule: . . . add contents of specified index register to Y (low-order 15 bits of instruction word), modulo 32,768.
.2374 Index specification: by b-designator in the instruction to be modified.
.2375 Number of potential indexers: . . . . . 7.
.2376 Addresses which can be indexed: . operand address portion (y-designator) of all instructions, including literals.
.2377 Cumulative indexing: . . . . . none.
.2378 Combined index and step: . . . . . none.
.238 Indirect addressing: only by means of jump instructions.
.239 Stepping —
.2391 Specification of increment: . . . . implied by operation code.
.2392 Increment sign: . + or -.
.2393 Size of increment: always 1 or 2 (depending on skip conditions).
.2394 End value: . . . . . zero, or any value specified in instruction or storage location.
.2395 Combined step and test: . . . . . yes.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program usage
Register:	1	30	A-register; accumulator.
Register:	1	30	Q-register; auxiliary arithmetic register; combines with A-register to form a single 60-bit register.
Register:	1	15	P-register; holds address of next instruction.
Register:	7	15	B-registers; index registers.
Register:	1	30	X-register; arithmetic communication register.
Register:	1	15	S-register; holds storage address during storage references.
Register:	1	30	Z-register; operand buffer for storage references.
Register:	1	6	K-register; shift counter.
Register:	1	30	U-register; holds the instruction being executed.
Register:	2	30	R-registers; used for communication with index registers.
Register:	2	30	C-registers; communication buffer registers.

.242

Category of storage	Total number of locations	Physical form	Access time, μsec
Register:	19	flip-flops	overlapped with Core Memory access time.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . . 1 (P-register).

.314 Special sub-sequence counters: . . . . . none (during repeated instructions, Index Register 7 holds the repeat counter).

.315 Sequence control step size: . . . . . 1 word (2 words on skips).

.316 Accessibility to routines: . . . . . P-register contents can be stored in Core Memory by "Return Jump" instructions.

.317 Permanent or optional modifier: . . . . . no.

.32 Look-Ahead: . . . . . none.

.33 Interruption

.331 Possible causes —
In-out units: . . . . . see next entry.
In-out subsystems: . . completion of input-output operation or input-output error.
Storage access: . . . . completion of magnetic drum operation or drum error.
Processor errors: . . illegal function code.
Memory protection: . attempt to exceed memory boundaries specified for individual tasks.
Other: . . . . . Delta Clock overflow; Delta Clock not updated.

.332 Control by routine —
Individual control: . . can enable internal interrupts on any or all input-output channels by means of special input-output instructions. Internal interrupts occur when an input buffer is filled or an output buffer is emptied.
Method: . . . . . when an interrupt occurs, all other non-error interrupts are disabled until they are re-enabled by a special instruction.
Restriction: . . . . . error interrupts cannot be locked out.

.333 Operator control: . . . none.

.334 Interruption conditions: interrupt enabled.

.335 Interruption process —
Disabling interruption: . . . . . automatic.
Registers saved: . . . contents of P-register (sequence counter) are saved by "Return Jump" instruction; other registers by program.
Destination: . . . . . one of 44 fixed locations, depending upon cause.

.336 Control methods —
Determine cause: . . . automatic; destination depends upon cause.
Enable interruption: . by special instruction contained in REX before returning to main program.

(Contd.)

.34 Multiprogramming

.341 Method of control: . . . by REX (see Section 800:191), using the interrupt facilities described above.
.342 Maximum number of programs: . . . . . limited only by hardware availability.
.343 Precedence rules: . . . see 800:191.12.
.344 Program protection —
Storage: . . . . . none.
In-out units: . . . . . via assignment by REX of specific units to specific programs.

.35 Multi-sequencing: . . . practical only in multi-computer complexes.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
Add-subtract: 9.6
Multiply: . . . . . 29.8 to 68.2
Divide: 69.1
.412 Floating point (using standard subroutines) —
Add: . . . . . 304.
Subtract: . . . . . 362.
Multiply: . . . . . 325.
Divide: . . . . . 357.
.413 Additional allowance for —
Indexing: . . . . . 0.
Indirect addressing: . (jump instructions only).
Re-complementing: . . 0.
.414 Control —
Compare: 9.6
Branch: 4.8
Compare and branch: 14.4 †
.415 Counter control —
Step and test: . . . . . 4.8 to 9.6
.416 Edit* —
Zero suppress: . . . . 106.
Float dollar sign: . . . 88.
Check protection: . . . 169.
417 Convert* —
Decimal to binary: . . 702.
Binary to decimal: . . 627.
.418 Shift: . . . . . 5.8 to 12.5

* These times are based on editing/converting a four-character field.

† These times are based on use of operands in Core Memory. Times are shorter if the operand is a literal or is contained in the A- or Q-register.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Fixed point
c = a + b:	29.0
b = a + b:	24.0
Sum N items:	9.6N
c = ab:	68.2
c = a/b:	88.3

.422 For arrays of data —

	Fixed point
$c_i = a_i + b_j$:	52.8
$b_j = a_i + b_j$:	52.8
Sum N items:	5.8N
$c = c + a_i b_j$:	97.0

.423 Branch based on comparison —
Numeric data: 65.3
Alphabetic data: 65.3
.424 Switching —
Unchecked: 19.2
Checked: 48.0
List search: . . . . . 26.9 + 5.8N
425 Format control per character —
Unpack: . . . . . ?
Compose: . . . . . ?
.426 Table look-up per comparison —
For a match: 6.7
For interpolation point: 6.7
.427 Bit indicators —
Set bit in separate location: 19.2
Set bit in pattern: . . 24.0
Test bit in separate location: 9.6
Test bit in pattern: . . 19.2
Test AND for B bits: . 38.4
Test OR for B bits: . . 38.4
.428 Moving (per full word or half-word): . . . . . 9.6 (using repeated "Replace" instruction).

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	interrupt.
Zero divisor:	none	as programmed.
Invalid data:	none.	
Invalid operation:	check	interrupt.**
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	none.	
Dispatch of data:	none.	
Delta Clock not updated:	check	interrupt.**

** Branch to a specific location in Wired Memory occurs if Bootstrap switch is in "Automatic Recovery" position.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (802:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

Because the UNIVAC 491/492 systems can process several independent programs at the same time through multiprogramming, the amount of central processor time required by each program is highly significant. The difference (if any) between the total elapsed time for a particular run and the amount of central processor time required for that run represents processor time that is potentially available to other programs. Whether or not this processor time can be efficiently utilized depends upon the system configuration, the over-all problem mix, and the effectiveness of the scheduling and operating system.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configurations VIIA and VIIIA, where all four input-output files are on magnetic tape, total times were computed for cases using both unblocked and blocked records in the detail and report files. Central processor time is essentially the same for all configurations, and is shown by the line marked "CP" on each graph. No addition has been made to the processor time to cover the overhead requirements of the operating system.

Worksheet Data Table 1 (page 802:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for Configurations III and V. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a fraction of the total processing time. When other programs with limited input and output can be run simultaneously in order to utilize the remaining processor time, it may be satisfactory to operate the UNIVAC 491/492 as just described. In other cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-print transcription of the report file. The curves for Configuration VIIA and VIIIA show the time required for the all-tape main processing run. The card-to-tape and tape-to-printer transcriptions will run at card reader and printer-limited speeds, and their demands on the processor will be small. The elapsed time and central processor time for the data transcription runs are shown on a separate graph (802:201.150). It should be noted that in the case of Configurations VIIA and VIIIA, the central processor time, rather than the input-output time, may well be the controlling factor whether the detail and report files are blocked or unblocked.

The master file record format is a mixture of alphameric and binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. Even so, most of the central processor time is devoted to editing, radix conversion, and character manipulation operations. Packing was kept to a minimum because of the high demands it would place upon the UNIVAC 491/492 central processor. The resulting master file record length is 21 words (the equivalent of 105 6-bit characters).

SORTING (802:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the Users' Guide, Paragraph 4:200.213, using a three-way merge.

MATRIX INVERSION (802:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplication ($c = c + a_i b_j$) using the standard single-precision floating-point subroutines. The processor time required for a matrix inversion can be spread over a much longer total elapsed time when the inversion is multi-run with other programs that utilize the available input-output equipment. Multi-running of other programs necessarily decreases the amount of internal storage that can be allocated to the matrix inversion.

GENERALIZED MATHEMATICAL PROCESSING (802:201.4)

The standard estimating procedure outlined in the Users' Guide, Paragraph 4:200.413, was used. Computation includes 5 fifth-order polynomials, 5 divisions and 1 square root, all of which were timed using SPURT floating-point subroutines.

WORKSHEET DATA TABLE 1

	ITEM		CONFIGURATION: III, V	CONFIGURATION: VIIA & VIIIA, Files 3 & 4 Blocked*	CONFIGURATION: VIIA & VIIIA, Files 3 & 4 Unblocked	REFERENCE
1	Char/block	(File 1)	1,050	1,050	1,050	
	Records/block	K (File 1)	10	10	10	
Input-Output Times	msec/block	File 1 = File 2	48.5	19.6	19.6	4:200.112
		File 3	66.7	17.1*	9.98	
		File 4	127.7	21.4*	10.47	
	msec/switch	File 1 = File 2	0	0	0	
		File 3	0	0	0	
		File 4	0	0	0	
	msec penalty	File 1 = File 2	3.02	3.02	3.02	
		File 3	0.23	2.30*	0.23	
		File 4	0.39	3.89*	0.39	
2	msec/block	a_1	0.18	0.18	0.18	
Central Processor Times	msec/record	a_2	0.42	0.42	0.42	
	msec/detail	b_6	3.02	3.02	3.02	4:200.1132
	msec/work	$b_5 + b_9$	0.80	0.80	0.80	
	msec/report	$b_7 + b_8$	6.90	6.90	6.90	

			III, V		VIIA & VIIIA, Files 3 & 4 Blocked*			VIIA & VIIIA, Files 3 & 4 Unblocked			
3	msec/block		C.P.	Printer	C.P.	VIIA	VIIIA	C.P.	VIIA	VIIIA	
Standard File Problem A F = 1.0	for C.P. and dominant column.	a_1	0.2		0.2			0.2			
		a_2K	4.2		4.2			4.2			
		a_3K	107.1		107.1			107.1			
		File 1: Master In	3.0		3.0	19.6		3.0	19.6		4:200.114
		File 2: Master Out	3.0		3.0			3.0			
		File 3: Details	2.3		2.3			2.3			
		File 4: Reports	3.9	1,277.	3.9	21.4	21.4	3.9	104.7	104.7	
		Total	123.7	1,277.	123.7	41.0	21.4	123.7	124.3	104.7	
4	Unit of measure	(30-bit words)									
Standard File Problem A Space		Std. routines	4,000**		4,000**			4,000**			
		Fixed	–		–			–			
		3(Blocks 1 to 23)	165		165			165			
		6(Blocks 24 to 48)	2,346		2,406			2,346			4:200.1151
		Files	924		1,680			924			
		Working	50		50			50			
		Total	7,485		8,306			7,485			

	ITEM		CONFIGURATION: III, V	CONFIGURATION: VIIA, VIIIA	REFERENCE
5	Fixed/Floating point		Floating (subroutines)	Floating (subroutines)	
Standard Mathematical Problem A	Unit name	input	800/900-cpm reader	Uniservo VIIIC	
		output	700/922-lpm printer	Uniservo VIIIC	
	Size of record	input	80 char	80 char	
		output	135 char	132 char	4:200.413
	msec/block	input T_1	75.0	6.8	
		output T_2	127.7	7.4	
	msec penalty	input T_3	0.23	0.23	
		output T_4	0.39	0.39	
	msec/record	T_5	10.6	10.6	
	msec/5 loops	T_6	28.4	28.4	
	msec/report	T_7	7.3	7.3	

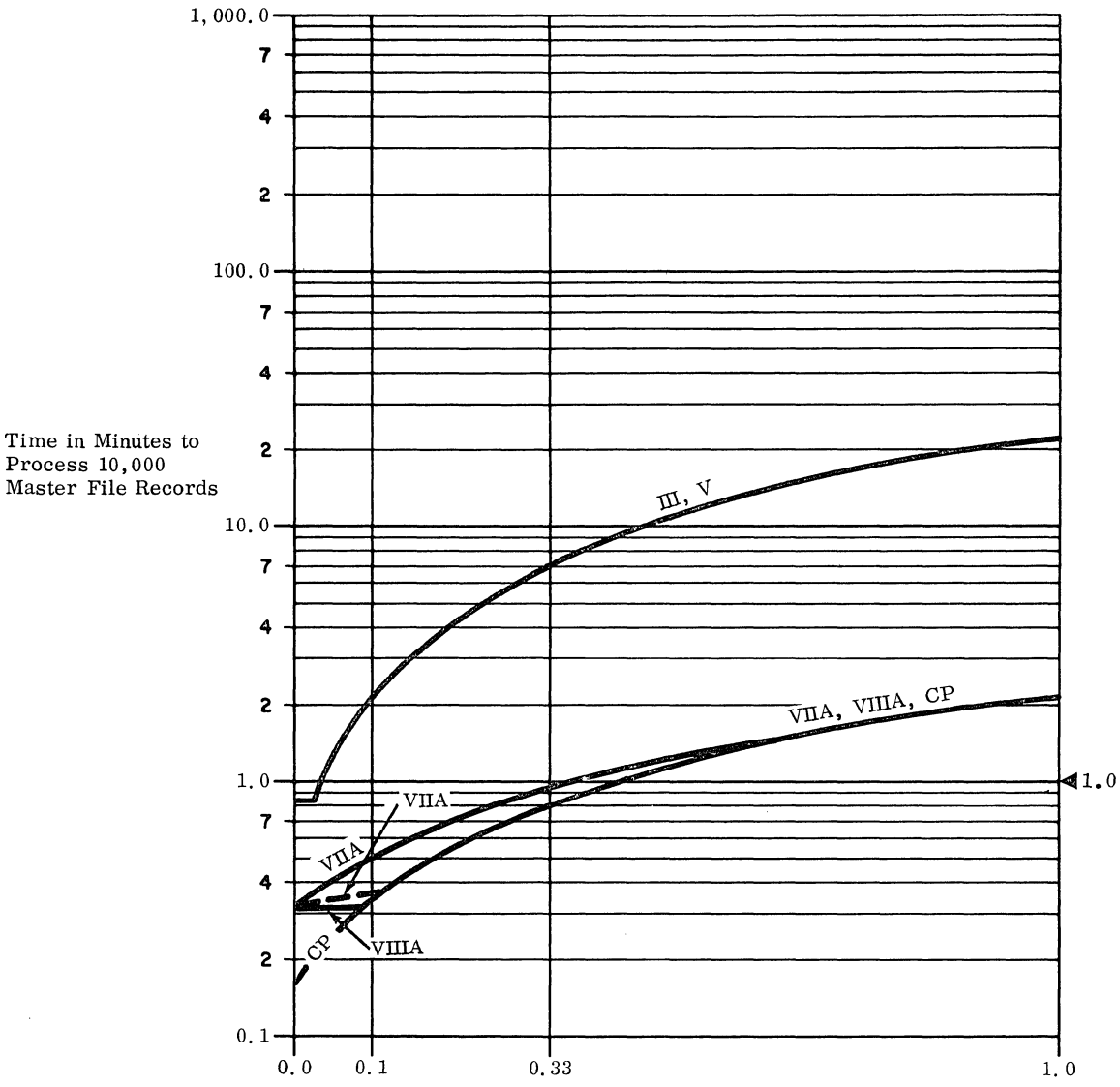
* 10 records per block in File 3 (detail) and 4 (report).
** 4,000 words are generally reserved for REX.

(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes —
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file:. . . . . 1 line.
.112 Computation:. . . . . standard.
.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.
.114 Graph: . . . . . see graph below.
.115 Storage space required —
Configurations III, V: 7,500 words.*
Configuration VIIA,
VIIIA (unblocked
Files 3 & 4): . . . . . 7,500 words.*
Configurations VIIA
and VIIIA (blocked
Files 3 & 4):. . . . . 8,300 words.*
* Includes 4,000 words reserved for REX system.



(Roman numerals denote standard System Configurations.)

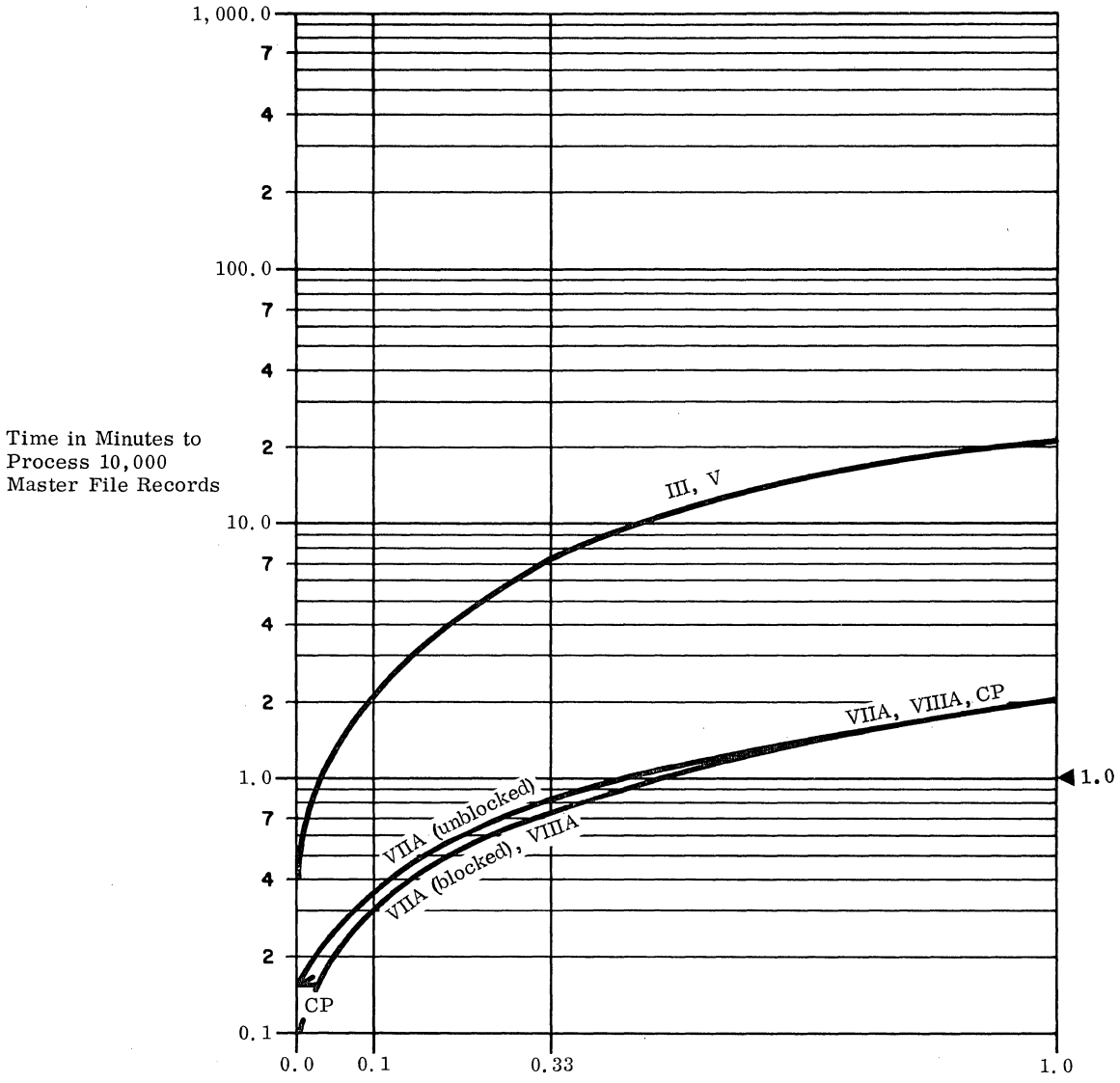
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

.12 Standard File Problem B

.121 Record sizes —
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

LEGEND

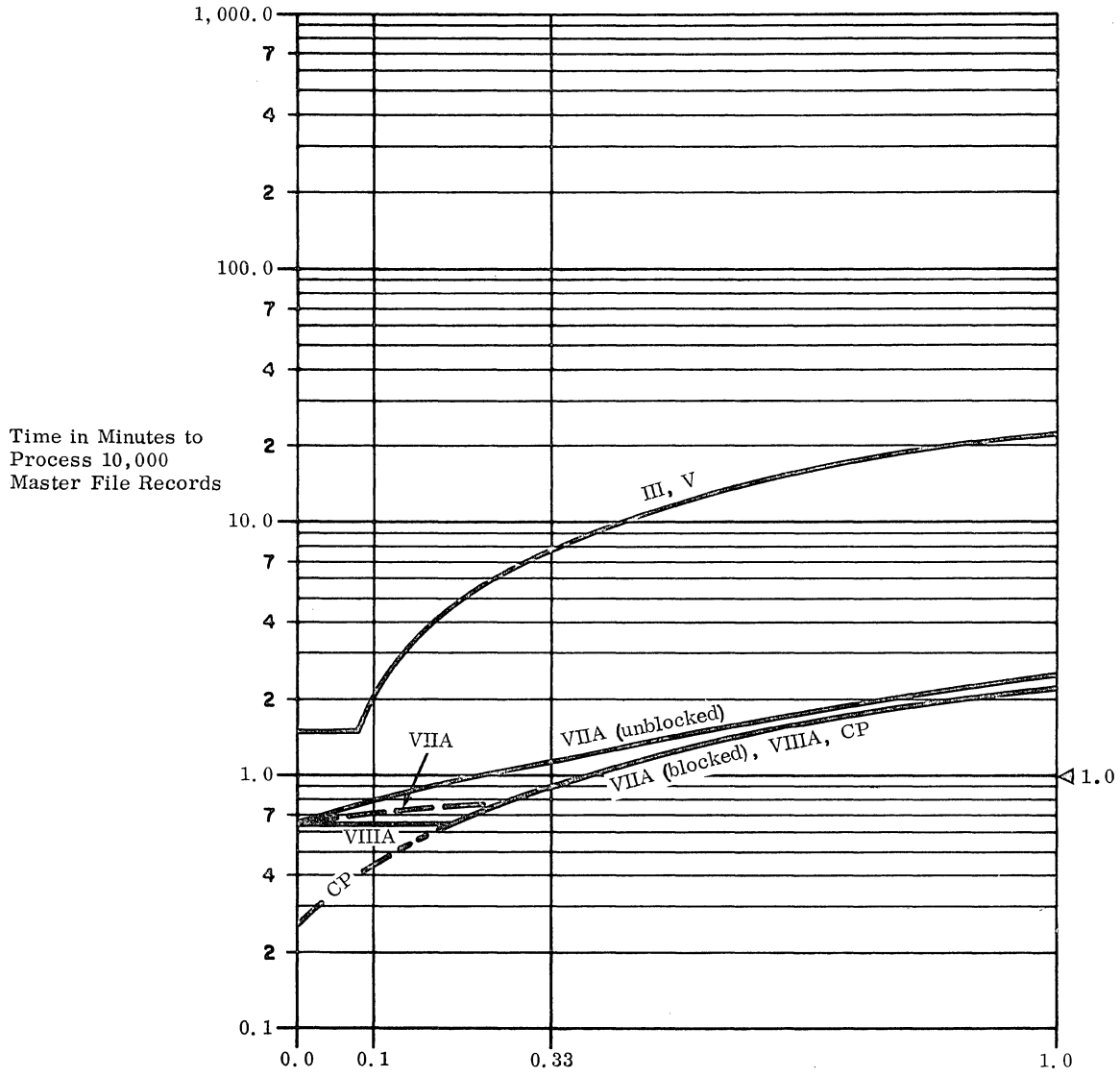
Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP — Central Processor time (all configurations)

(Contd.)

.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

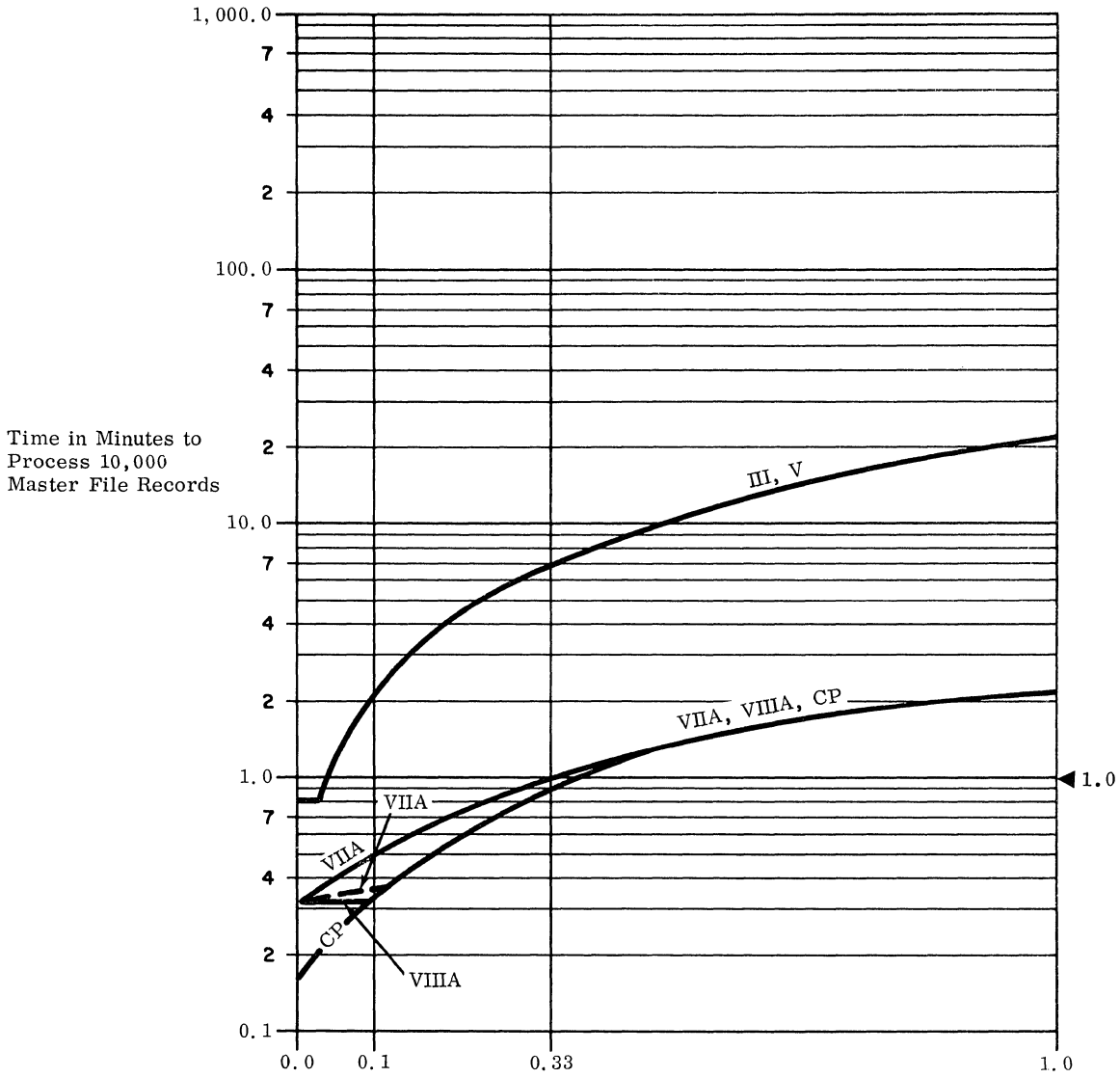
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
Central Processor time (all configurations)

.14 Standard File Problem D

.141 Record sizes –
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
Central Processor time (all configurations)

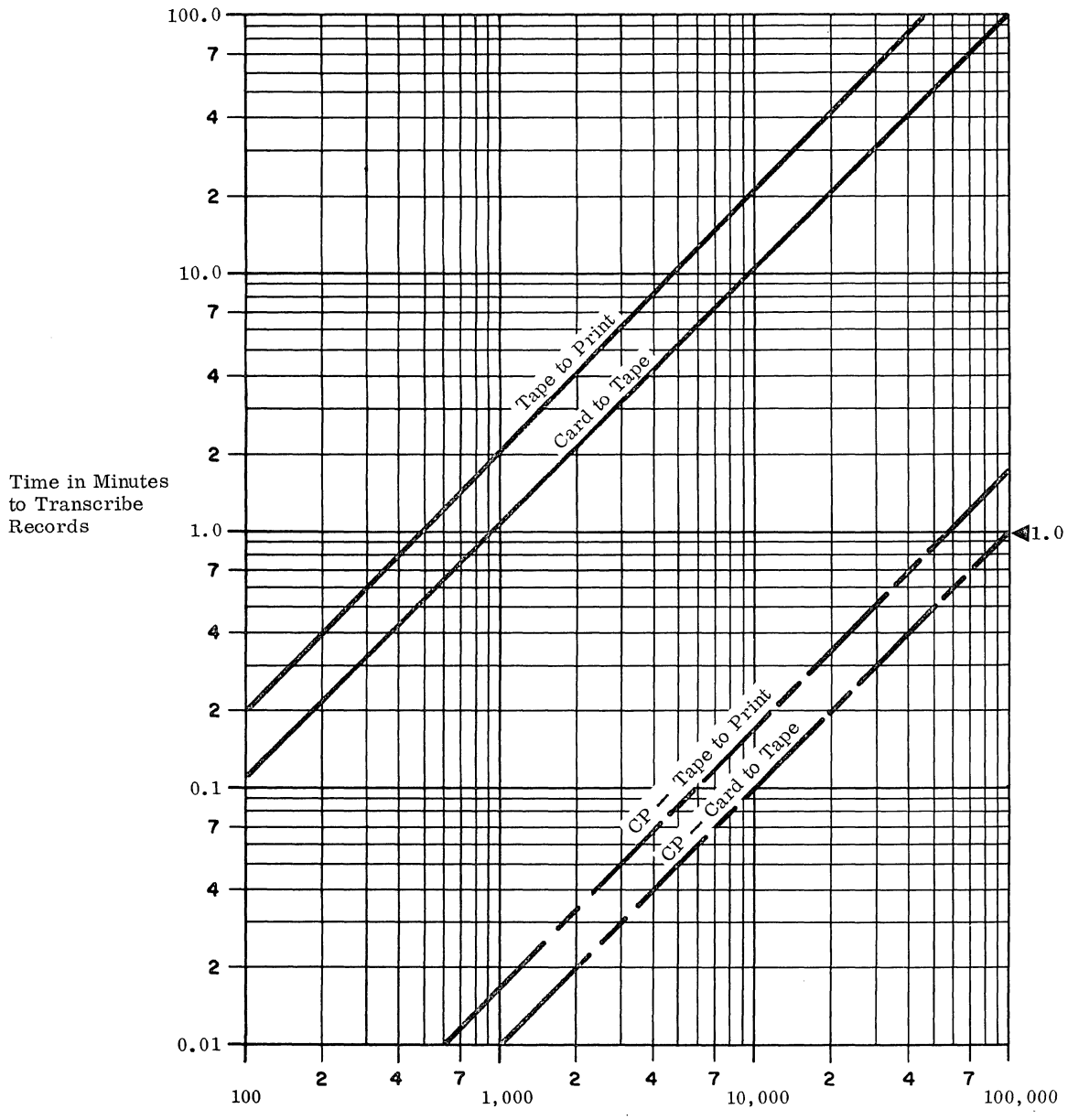
(Contd.)

.15 Data Transcription Runs for Standard File Problems

.151 Block sizes:
Detail file (on cards): one card image.
Report file (on printer):. . . . . one print line.

.153 Timing basis: . . . . . data is transcribed directly from cards to tape or tape to printer; no editing is performed during these runs.

.154 Graph: . . . . . see graph below.

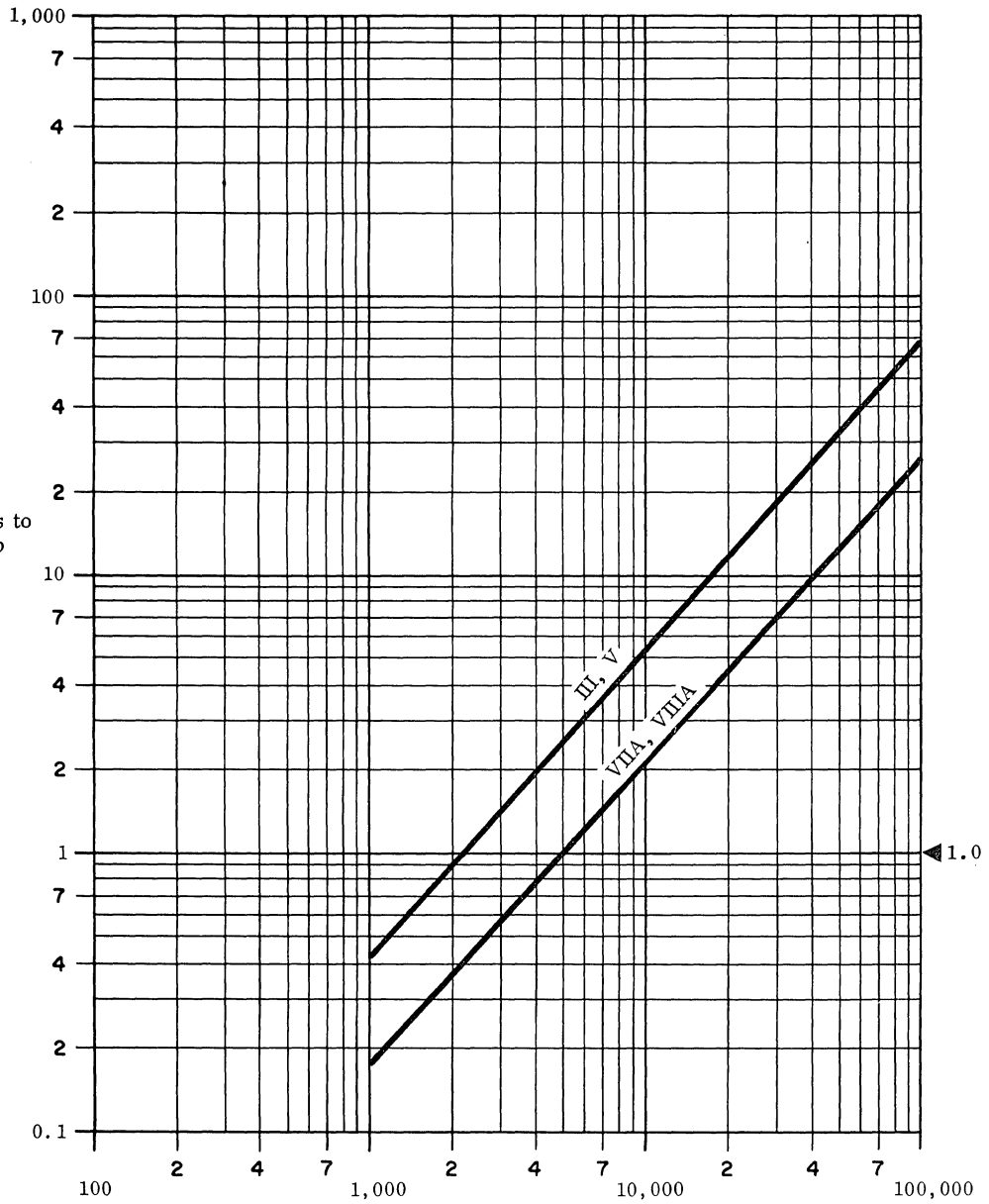


(Graph applies to Standard Configurations VIIA and VIIIA; curves marked "CP" denote Central Processor times.)

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.
.212 Key size: . . . . . 8 characters.
.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213; 3-way tape merge.
.214 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

(Contd.)

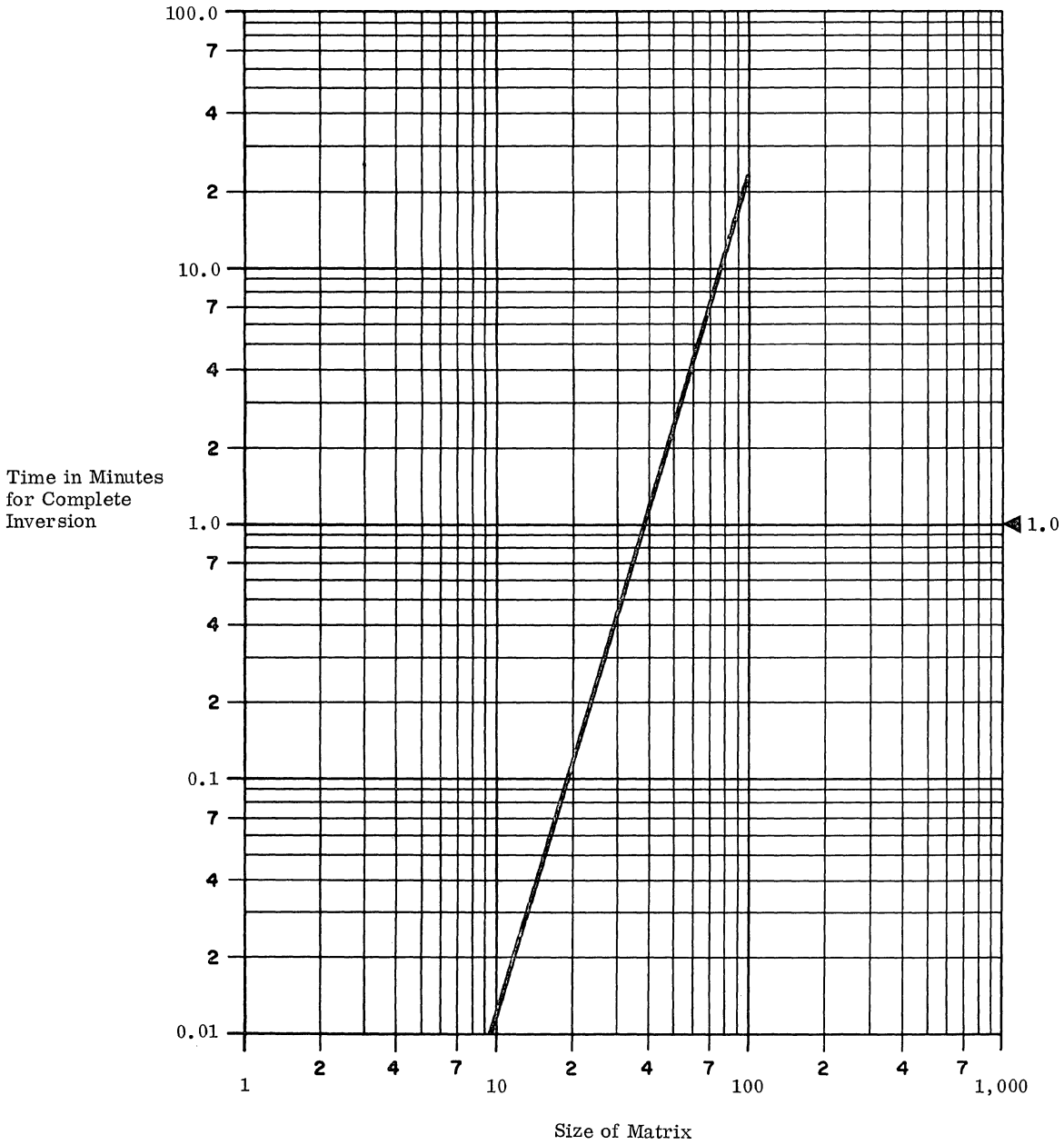
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits precision.

.312 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . . see graph below.



.4 GENERALIZED MATHEMATICAL PROCESSING

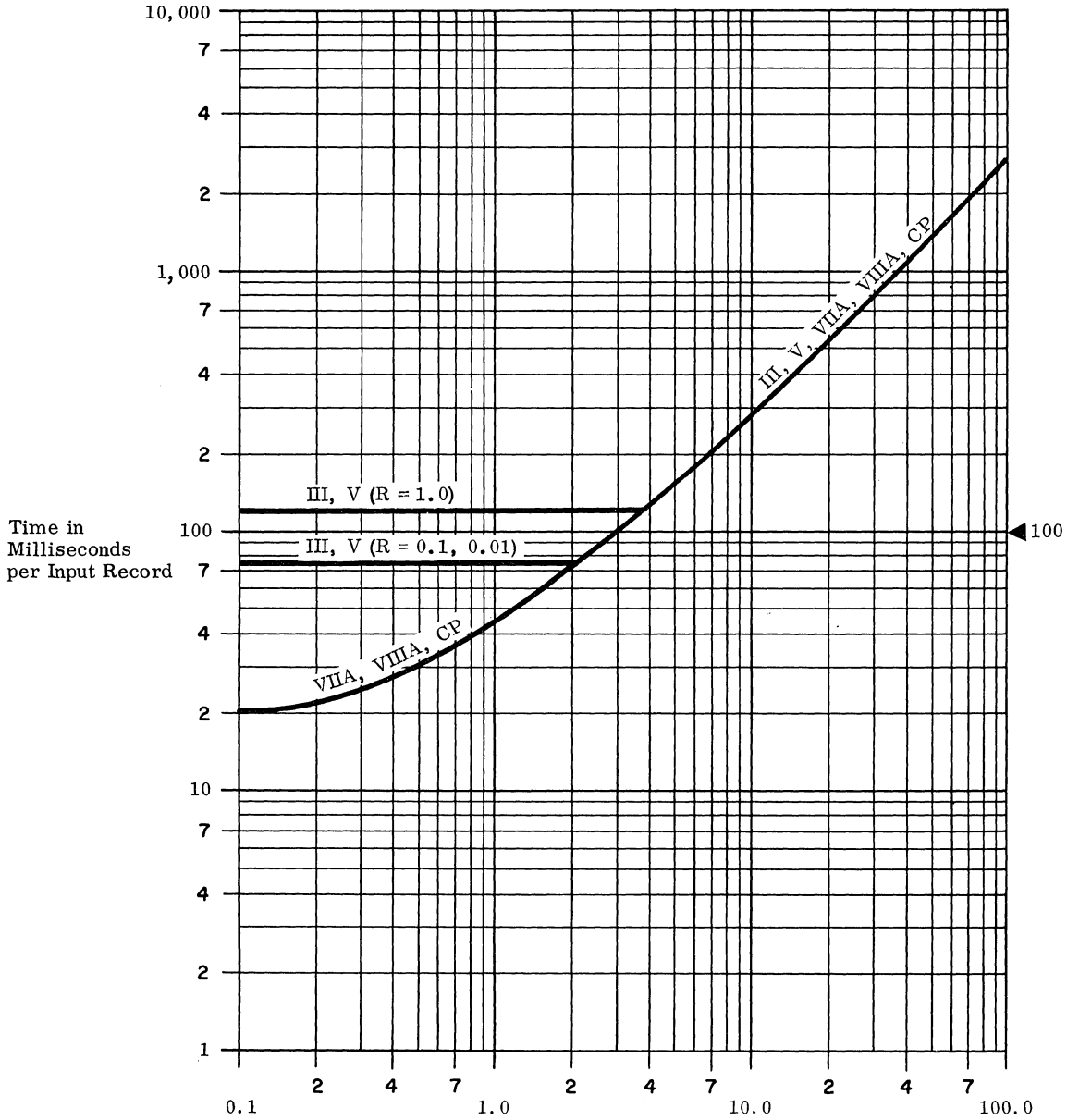
.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . 10 signed numbers; average size 5 digits, maximum size 8 digits.

.412 Computation: . . . . . 5 fifth-order polynomials, 5 divisions, and 1 square root; computation is performed in 8-digit-precision floating-point mode, using subroutines.

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations; R = number of output records per input record; curve marked "CP" shows central processor time.)

UNIVAC 494

Univac

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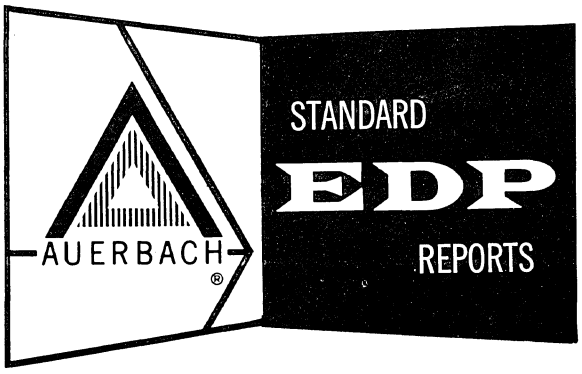

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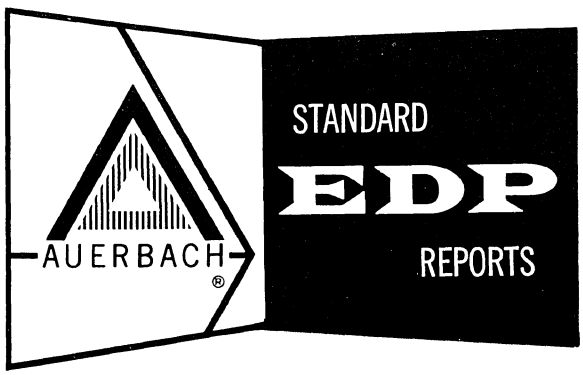

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INTRODUCTION

The UNIVAC 494 computer system was announced in June 1965, and the first customer delivery is scheduled for the second quarter of 1966.

Among the characteristics of the UNIVAC 494 system that distinguish it from the less powerful members of the 490 Series are the following:

- A basic core storage cycle time of 0.75 microsecond; an effective cycle time of 0.375 microsecond can be achieved through dual-bank overlapping of memory accesses in all models with 32,768 words or more.
- Core storage capacities of 16,384 to 131,072 30-bit words.
- An instruction repertoire consisting of 109 basic instructions (including all of the 62 instructions used in the UNIVAC 490, 491, and 492 Processors).
- Inclusion of standard facilities for floating-point, double-precision, and decimal arithmetic.
- A special 490-compatible mode that enables a 494 to execute programs written for UNIVAC 490, 491, or 492 systems without alteration.
- A core storage protection facility that permits individual 64-word blocks to be guarded against unauthorized access.
- Parity checking on all core storage operations.
- A maximum of 24 input-output channels, 23 of which are available for general-purpose use.

This subreport concentrates upon the characteristics and performance of the UNIVAC 490 Central Processor and systems based upon it. All general characteristics of the 490 Series hardware and software are described in Computer System Report 800: UNIVAC 490 Series — General.

The System Configuration section that follows shows the UNIVAC 494 system arranged in a number of standardized configurations according to the rules in the Users' Guide, page 4:030.120. A "Typical Multiprocessor Configuration" is also shown to illustrate the manner in which two or three independent Central Processors can be used in a single UNIVAC 494 installation. The standardized equipment configurations form the basis for a detailed analysis of the overall System Performance of the UNIVAC 494 on our standard benchmark problems, the results of which are presented in Section 804:201.

Section 804:051 contains a detailed description of the UNIVAC 494 Central Processor, its processing facilities, and its execution times for a series of standardized tasks.

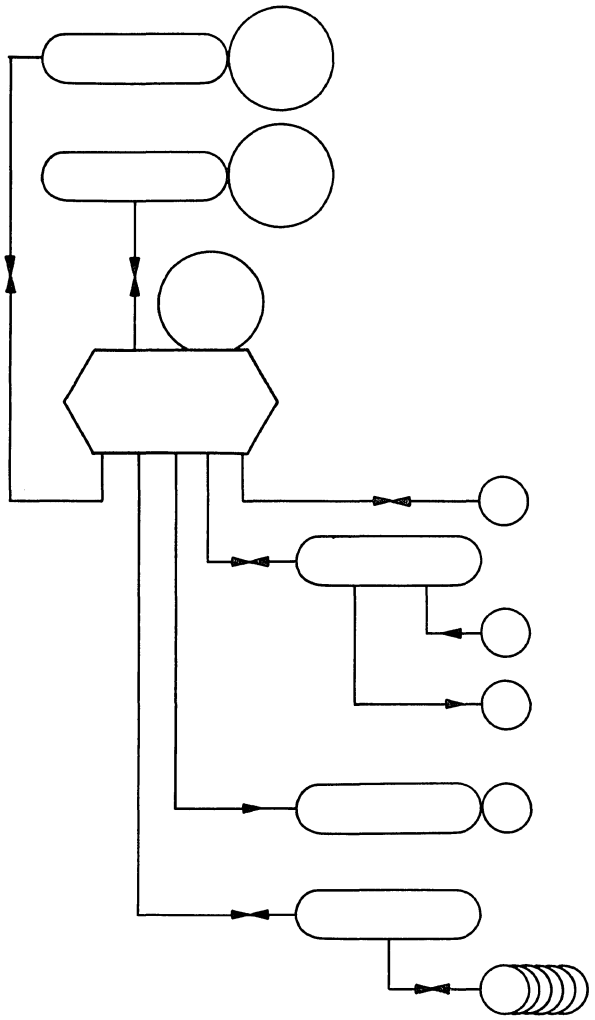
Omega, the comprehensive operating system that is being developed to take advantage of the 494's expanded hardware capabilities, is described in Section 804:191 of this subreport. All of the other UNIVAC 490 Series software is described in Report Sections 800:151 thru 800:191.

SYSTEM CONFIGURATION

For overall configuration rules, refer to Page 800:031.100.

.1 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

Deviations from Standard Configuration: . . . . . magnetic drum is required for executive system use.
auxiliary storage (Fastrand II) is 448% larger.
core storage is 8 times larger.
card reader is 60% faster.
card punch is 200% faster.
printer is 40% faster.
all input-output channels can operate concurrently.

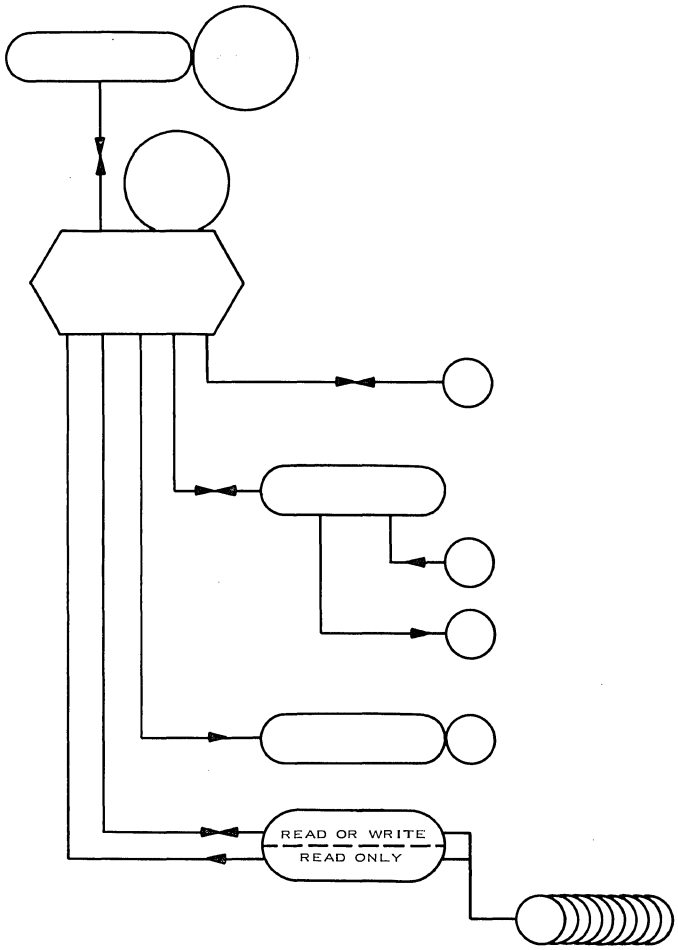


Equipment	Rental
FH-880 Drum & Synchronizer	$ 3,420
Fastrand II Storage Unit & Synchronizer: 25,952,256 words	5,250
Core Memory: 32,768 words - dual banks	6,500
Central Processor Set	9,500
Console	
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Printer & Synchronizer	1,550
Uniservo VIC Control & Synchronizer	700
2 Uniservo Simultaneous Master Units	1,100
4 Uniservo Slave Units: 34,200 char/sec.	1,200
TOTAL RENTAL:	$ 31,015

Notes:
1. Standard Configuration III is the same as Configuration V (shown here) less Fastrand II Unit and Synchronizer; its rental is $25,765 per month.
2. Configuration V, with the addition of a Communication Terminal Module Controller and up to 16 Communication Line Terminals, each having 2 input and 2 output lines, represents a typical communications system. The total monthly rental of such a system — including 16 medium-speed asynchronous Communication Line Terminals — is $32,865.

.2 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

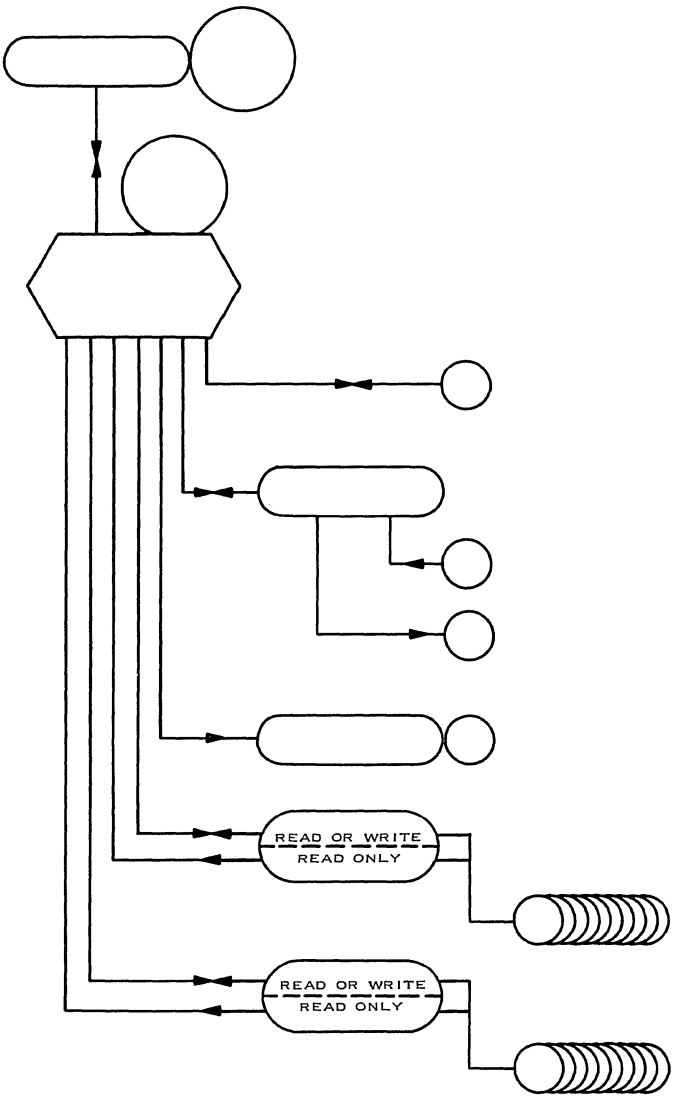
Deviations from Standard Configuration: . . . . . magnetic drum is required for executive system use.
available core storage is 50% larger.
magnetic tape is 60% faster.
card reader is 60% faster.
card punch is 200% faster.
printer is 40% faster.



Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$ 3,420
Core Memory: 32,768 words — dual banks	6,500
Central Processor Set	9,500
Console	
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Printer & Synchronizer: 700/922 lines/min.	1,550
Uniservo VIIIC Synchronizer: dual-channel model.	1,450
10 Uniservo VIIIC Tape Units: 96,000 char/sec	8,500
TOTAL RENTAL:	$ 32,715

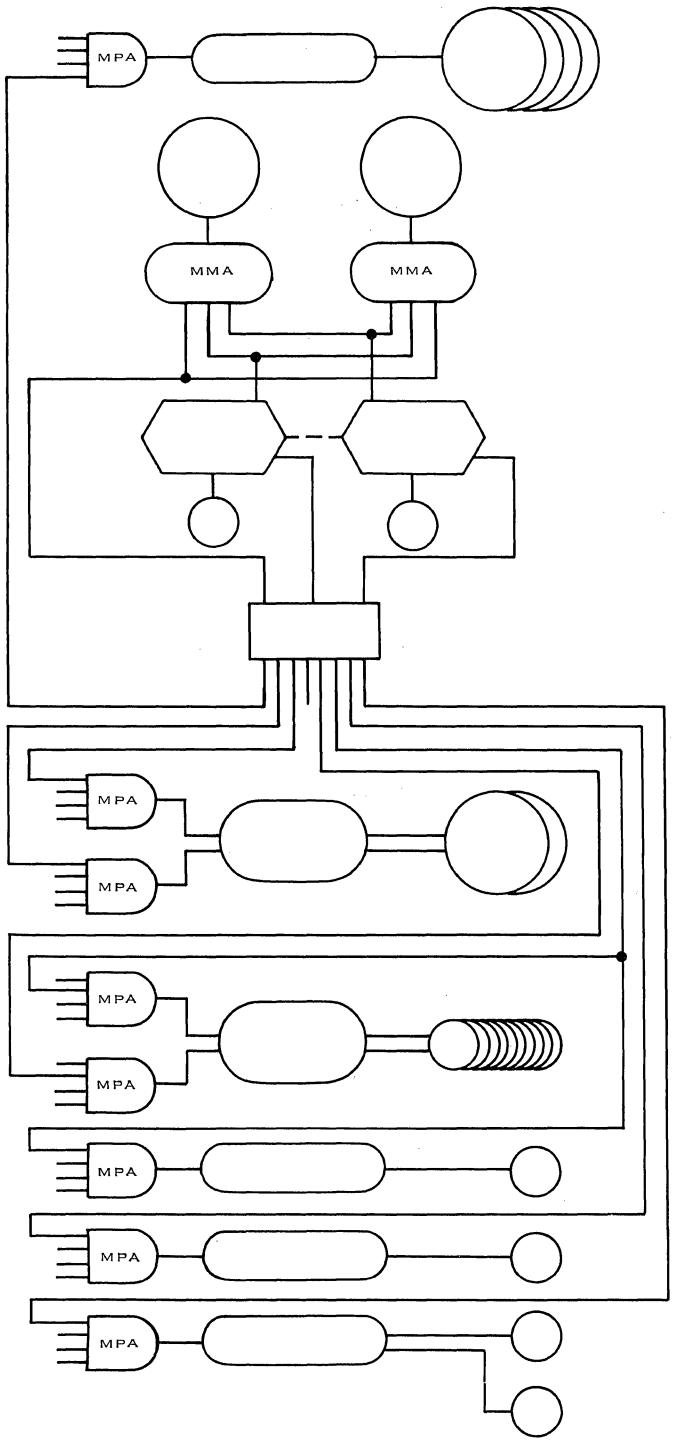
.3 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: . . . . . magnetic drum is required for executive system use.
available core storage is 50% larger.
magnetic tape is 20% slower.
printer is 30% slower.
card reader is 20% slower.
card punch is 50% faster.



Equipment	Rental
FH-880 Drum & Synchronizer: 786,432 words	$ 3,420
Core Memory: 65,536 words — dual banks	11,000
Central Processor Set	9,500
Console	
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Printer & Synchronizer 700/922 lines/min.	1,550
Uniservo VIIIC Synchronizer; dual-channel model	1,450
10 Uniservo VIIC Tape Units: 96,000 char/sec.	8,500
Uniservo VIIIC Synchronizer; dual-channel model	1,450
10 Uniservo VIIIC Tape Units: 96,000 char/sec.	8,500
TOTAL RENTAL:	$ 47,165

.4 TYPICAL MULTIPROCESSOR CONFIGURATION



Equipment	Rental
FH-432 Magnetic Drum Subsystem:	
1 Drum Control & Synchronizer Unit	$ 3,000
4 FH-432 Drum Units with total capacity of 1,048,576 words	4,000
1 Multiple Processor Adapter	435
Core Memory: 2 banks of 65,536 words per bank	20,000
2 Multiple Module Access Units	1,470
Central Processors and Consoles (2)	19,000
Input/Output Controller with 8 Channels	4,500
Fastrand Dual-Channel, Buffered Control & Synchronizer	2,500
Fastrand II Storage Units (2): 51,904,512 words	7,600
Uniservo VIIIC Control & Synchronizer; dual channel:	1,450
Uniservo VIIIC 7-Channel Tape Units (10): 96,000 char/sec.	8,500
High-Speed Printer Control & Synchronizer	750
High-Speed Printer: 700/922 lines/min.	800
High-Speed Printer Control & Synchronizer	750
High-Speed Printer: 700/922 lines/min.	800
Card Control & Synchronizer	750
Card Reader: 800/900 cards/min.	380
Card Punch: 300 cards/min.	665
Cost of Multiple Processor Adapters for above subsystems:	835
	835
	435
	435
	435
TOTAL RENTAL:	$80,325

CENTRAL PROCESSOR: UNIVAC 494

.1 GENERAL

.11 Identity: . . . . . UNIVAC 494 Central Processor. Type 3012-99.

.12 Description

The UNIVAC 494 Central Processor houses the system's solid-state arithmetic and control circuitry. Of the 109 basic instructions provided with the 494 Central Processor, 62 are common to all the central processors in the 490 Series. The 47 instructions peculiar to the UNIVAC 494 offer:

- Increased power in the arithmetic functions, including double-precision floating-point, double-precision fixed-point, and decimal arithmetic.
- Increased power in the control of multiprogramming operations.
- Several data-manipulation instructions to assist the programmer in handling data produced by or prepared for computer systems outside the 490 Series family. Specifically, the Pack and Unpack instructions and the Scale Factor Shift instruction facilitate data-handling operations. Editing and radix-conversion instructions are not directly provided.

Instruction Formats

The 30-bit instruction word format for the 62 instructions shared with the other 490 Series central processors is composed of the following elements:

- A 6-bit f-designator that specifies the basic operation to be performed.
- A 3-bit j-designator that usually specifies the conditions under which a skip or jump will be performed, such as jumping when the contents of an arithmetic register are positive, negative, zero, or non-zero. The j-designator can also specify the mode for a Repeat instruction, or the index register to be used in a loop control instruction. In input-output instructions, the j-designator is 4 bits long and specifies the data channel to be used.
- A 3-bit k-designator that specifies whether an associated operand is held in a full word or a portion of a word.
- A 3-bit b-designator that specifies one of seven index registers whose contents are to be added to the y-designator portion to form an operand or its effective address.
- A 15-bit y-designator that specifies the base operand address, a literal operand, or a shift count.

Each one of these 62 instructions can have up to 64 distinct variations, due largely to the functional flexibility of the j- and k-designators. The j-designator in most instructions can cause a conditional skip of the next instruction, depending on the sign of the A-register (accumulator) or Q-register. The k-designator in most instructions can specify whether the operand shall consist of all 30 bits or only the high-order or low-order 15 bits of the Core Memory location specified by the y-designator. When half-word operands are specified, sign extension is optional.

The 47 instructions that are peculiar to the UNIVAC 494 Central Processor utilize a different 30-bit instruction word format, as illustrated in Figure 1. These instructions share a common operation code (octal 77) and obtain their individuality only through variations in the g-designator, a 6-bit instruction part that replaces the j- and k-designators of the 62 common 490 Series instructions. Thus, the 494's instruction word is effectively shortened by 6 bits, and decreased instruction flexibility results.

Designator:	f	j	k	b	y
Size in bits:	6	3	3	3	15

Format for instructions common to all 490 Series Central Processors

Designator:	f	g	b	y
Size in bits:	6	6	3	15

Format for instructions peculiar to 494 Central Processor.

Figure 1. UNIVAC 494 Series Instruction Formats

Execution time for most UNIVAC 494 instructions, when alternate banks of core storage are accessed, is 0.75 microsecond. This time is obtained by overlapping one instruction's execution cycle with the next instruction's interpretation cycle. A description of the functions of each of these cycles follows.

Interpretation Cycle

The contents of the Program Location Counter are transferred to the 17-bit P (Program) Register and then to both core memory and the Internal Function Register (IFR). The IFR is used to facilitate user-to-executive routine jumps and returns. The instruction word is then read from the indicated address of core memory into the Instruction Register, the contents of the word are analyzed for operation and function codes, and the execution cycle is started.

Execution Cycle

The operand is determined according to the contents of the 30-bit Instruction Register. In some cases (literals), the operand is a part of the instruction word itself. In these cases, the execution cycle is reduced to placement of the operand into its proper register and then processing it as explained in Step 5 below. In other cases, the instruction word specifies the memory address of the operand. The following steps are then executed:

.12 Description (Contd.)

(1) The relative address contained in the instruction word is added to the contents of an index register, resulting in an effective address.

(2) The effective address is added to the contents of the Relative Index Register to form the absolute memory address.

(3) The absolute memory address is loaded into the Operand Address Register and checked to determine that it lies within the predetermined program boundaries.

(4) The operand is read from memory into the applicable register.

(5) The logic circuits, conditioned by timing and execution controls, process the operand, retaining the result in one of the arithmetic registers.

(6) If required by the instruction, the result is stored in a memory location specified in the instruction word.

Communication Modes

The UNIVAC 494 Central Processor uses two modes of communication with peripheral devices. The Internally Specified Index (ISI) mode is used if the I/O device is directly connected to a channel of the Central Processor. If a multiplexor device (such as a communications controller) interfaces between a channel and the I/O device, the channel operates in the Externally Specified Index (ESI) mode, as explained in Report Section 800:101.

Program Protection

Program protection can be accomplished by the UNIVAC 494 Central Processor in three ways:

- Read and Write Protection with Guard Mode. This mode of memory protection will cause a program protection interrupt if an attempt is made to read, write, or jump outside the limits set by the Program Lock-In Register. Guard Mode prohibits usage of I/O instructions or reserved executive-routine instructions in the user program.
- Write Protection with Guard Mode, allowing full freedom to read any area of memory, while protecting specified memory areas against writing and prohibiting the use of I/O and reserved instructions.
- Write Protection without Guard Mode, permitting unrestricted reading and the use of I/O and reserved instructions, while protecting specified memory areas against writing.

The 494 Central Processor can also be directed to run without any form of memory protection if this should ever be desired.

Relative Addressing

Two modes of relative addressing can be used in the 494 Central Processor. When the Dual Relative mode is used, the data addressing can be relative to the Lower Limit of the Program Lock-In Register while the instruction addressing is relative to the Relative Index Register. When the RIR Relative Index mode is used, both data and instructions must be addressed relative to the value stored in the Relative Index Register.

Multiprocessing

Two UNIVAC 494 Central Processors can share the same core storage via a Multiple Module Adapter (MMA). This adapter provides for the connection of up to three Central Processors and/or Input/Output Controllers. (The Input/Output Controller is described in Paragraph 800:111.6.) A third processor may be of value for redundancy purposes to ensure system reliability, but UNIVAC states that no timing advantage over a two-processor configuration will result.

With two processors, paired simultaneous core memory accesses can be made to the odd and even banks. Within a cabinet of two 32,768-word memory banks, the even addresses are assigned to one bank and the odd addresses to the other. A program loaded into core storage will be split, even/odd, between the two banks. Since each module is independently accessible, a second Central Processor can access instructions or data from the even bank while the first Central Processor is accessing the odd bank, and vice versa. Synchronization of the dual accesses is accomplished by delaying one processor whenever the other is executing an instruction that takes longer than the average execution period. The delayed processor is restarted as soon as simultaneous odd/even accesses can again be made.

Use of the Multiple Module Adapter currently introduces a 125-nanosecond delay upon each access to core memory, but UNIVAC indicates that this delay is likely to be reduced or eliminated in the near future.

.13 Availability: . . . . . 9 months.

.14 First Delivery: . . . . . 2nd quarter, 1966.

.2 PROCESSING FACILITIES

.21 Operations and Operands

Operation and Variation	Provision	Radix	Size
.211 Fixed point —			
Add-subtract:	automatic	binary	29 bits + sign or 59 bits + sign.
		decimal	59 bits + sign.
Multiply —			
Short:	none		
Long:	automatic	binary	29 bits + sign. (60-bit product).
Divide —			
No remainder:	none		
Remainder:	automatic	binary	29 bits + sign (60-bit dividend).

		Provision	Radix	Size
.212	Floating point —			
	Add-subtract:	automatic	binary	48 & 11 bits + sign.
	Multiply:	automatic	binary	48 & 11 bits + sign.
	Divide:	automatic	binary	48 & 11 bits + sign.
.213	Boolean —			
	AND:	automatic	binary	30 bits.
	Inclusive OR:	automatic	binary	30 bits.
	Exclusive OR:	automatic	binary	30 bits.
.214	Comparison —			
	Numbers:	automatic		30 bits.
	Letters:	automatic		30 bits.
	Mixed:	automatic		30 bits.
	Collating sequence:	see Data Code Table, Page 800:141.100.		

		Provision	Comment	Size
.215	Code translation:	none	performed by subroutines.	
.216	Radix conversion:	none	performed by subroutines.	
.217	Edit format:	none	performed by subroutines.	
.218	Table look-up —			
	Equality:	none.		
	Greater than: / Less than or equal: / Within limits:	semi-automatic through use of "Repeat" instruction.		30 bits.
	Greatest:	none.		
	Least:	none.		
.219	Others —			
	Shifts:	automatic	left shifts are circular; right shifts with sign extension.	30 or 60 bits.
	Add to storage:	automatic		29 bits + sign.
	Subtract from storage:	automatic		29 bits + sign.
	Repeat:	automatic	executes next instruction a specified number of times.	

.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement — binary. nine's complement — decimal.

.222 Zero: . . . . . +0 and -0 have zeros and ones, respectively, in all 30 bit positions; they are considered unequal in compare and certain arithmetic operations.

.223 Operand size determination:. . . . . K-designator in most instructions specifies full word (30 bits), upper or lower half-word (15 bits), or literal operand (15 bits).

.23 Instruction Formats

.231 Instruction structure:. one 30-bit word.

.232 Instruction layout: . . . see Paragraph .12.

.233 Instruction parts:. . . . see Paragraph .12.

.234 Basic address structure:. . . . . 1 + 0.

.235 Literals —
Arithmetic:. . . . . 15 bits (i.e., up to 32,767).
Comparisons and tests:. . . . . 15 bits.
Incrementing modifiers: . . . . . 15 bits.

.236 Directly addressed operands —
Internal storage type: core storage.
Minimum size: . . . . 1/2 word (15 bits).
Maximum size: . . . . 3-1/2 words (Store Index Registers).
Volume accessible: . total capacity (up to 131,072 words).

.237 Address indexing —

.2371 Number of methods: . 1.

.2372 Names:. . . . . indexing.

.2373 Indexing rule: . . . . . add contents of specified index register to y (low-order 15 bits of instruction word).

.2374 Index specification:. . by b-designator in the instruction to be modified.

.2375 Number of potential indexers: . . . . . 2 sets of 7 (one set for user routines and one for executive routine).

.2376 Addresses which can be indexed: . . . . . operand address portion (y-designator) of all instructions, including literals.

.2377 Cumulative indexing:. none.
.2378 Combined index and step: . . . . . none.
.238 Indirect addressing: . . only by means of jump instructions.
.239 Stepping —
.2391 Specification of increment: . . . . . implied by operation code.
.2392 Increment sign: . . . . + or -.
.2393 Size of increment: . . always 1 or 2 (depending on skip conditions).
.2394 End value:. . . . . zero, or any value specified in instruction or storage location.
.2395 Combined step and test: . . . . . yes.

.24 Special Processor Storage:. . . . . see Table I.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities:. . . 1 (P-register).
.314 Special sub-sequence counters: . . . . . none (during repeated instructions, the seventh Index Register holds the repeat counter).
.315 Sequence control step size:. . . . . 1 word (2 words on skips).
.316 Accessibility to routines: . . . . . P-register contents can be stored in Core Memory by "Return Jump" instructions.
.317 Permanent or optional modifier: . . . . . no.

.32 Look-Ahead:. . . . . none.

.33 Interruption

.331 Possible causes —
In-out subsystems:. . completion of input-output operation, or input-output error.
In-out controllers: . . parity error in buffer word.
Storage access: . . . . completion of magnetic drum operation, or drum operational error.
Processor errors: . . illegal function code.
memory parity error.
memory protection violation.
floating point underflow.
floating point overflow.
Other: . . . . . power loss.
day clock.
real-time clock.
data request from sending processor.
.332 Control by routine —
Individual control: . . can enable internal interrupts on any or all input-output channels by means of special input-output instructions.
Method: . . . . . when an interrupt occurs, all other non-error interrupts are disabled until they are re-enabled by a special instruction.
Restriction: . . . . . error interrupts cannot be locked out.
.333 Operator control:. . . . operator can initiate a request for an external interrupt.
.334 Interruption conditions: interrupt enabled.
.335 Interruption process —
Disabling interruption: . . . . . automatic.
Registers saved: . . . contents of P register (sequence counter) and users' index registers are saved automatically.
Destination: . . . . . one of 73 fixed locations, depending on cause of interrupt.
.336 Control methods —
Determine cause:. . . automatic; destination depends upon cause.
Enable interruption: . by special instruction contained in Omega before returning to main program.

.34 Multiprogramming

.341 Method of control: . . . by Omega (see Section 804:191).
.342 Maximum number of programs:. . . . . 64 per processor.
.343 Precedence rules: . . . see Section 804:191.12.
.344 Program protection —
Storage: . . . . . by means of program boundaries in 64-word increments.
Input-output units: . . through assignment by Omega of specific units to specific programs.

.35 Multisequencing: . . . . possible only with a multicomputer complex.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds*

		Single Memory Bank	Dual Memory Banks
.411	Fixed point —		
	Add-subtract:	1.5	0.75
	Multiply:	8.03	7.27
	Divide:.	8.03	7.27
.412	Floating point —		
	Add-subtract:	2.99	2.35
	Multiply:	12.84	12.09
	Divide:.	12.63	12.41
.413	Additional allowance for —		
	Indexing:	0	0
	Indirect addressing:	(not available)	
	Recomplementing: .	0.11	0.11
.414	Control —		
	Compare:	1.5	0.75
	Branch:	0.11	0.11
	Compare and branch:	0.21	0.21
.415	Counter control —		
	Step and test:	1.5	0.75
.416	Edit:	no instruction available.	
.417	Convert:.	no instruction available.	
.418	Shift:	1.5	0.75

* These times are based on instructions whose operands are located in core storage. Times are generally shorter if the operand is a literal or is contained in the A or Q register.

TABLE I: CENTRAL PROCESSOR REGISTERS AND THEIR CHARACTERISTICS

Number of Storage Locations	Size in Bits	Register Name	Program Usage
1	30	IFR — Internal Function Register	Captures the contents of the P register for jump instructions. Captures the relative address of a Repeat instruction and its j-designator. Determines type of program protection. Indicates overflow or carry for BCD arithmetic. Activates the proper index register sets depending on executive or user routine usage. Determines the bit capacity of the index registers. Activates the relative addressing mode.
1	15	P — Program Register	Holds address of next instruction; the Memory Select Register combines with P for determination of next address within proper storage module.
1	2	MSR — Memory Select Register	See Program Register description, above.
1	30	PLR — Program Lock-in Register	Defines the upper and lower memory limits of each program.
1	30	RIR — Relative Index Register	Used as the base program address to facilitate moving programs anywhere within memory without modification.
1	30	U — Instruction Register	Holds the instruction being executed.
1	5	IASR — Interrupt Address Storage Register	Used for channel number storage prior to exiting to executive routine.
1	5	CSR — Channel Select Register	Used to select the proper input-output device on the channel.
14	15 or 17	B_1 to B_7 — Index Registers	There are two sets of 7 index registers; one set for user programs, one set for the executive routine. The executive set can use 4 of the 7 registers in an expanded length of 17 bits to allow memory referencing of all modules. The uses of the registers include operand address modification, index codes, counters, and modifier incrementation.
48	30	BCR — Buffer Control Register	Used to control I/O transfer operations between a portion of core used as a buffer and the peripheral device. There are 24 input and 24 output buffer control registers.
1	30	X — X Register	Controls communication between arithmetic circuits and core memory.
1	30	A — Accumulator	The principal arithmetic register.
1	30	Q — Quotient Register	The secondary arithmetic register; A and Q are used in combination for double-precision and BCD arithmetic operations.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Fixed Point	Floating Point
c = a + b:	2.25	9.64
b = a + b:	2.25	9.64
Sum N items:	0.75N	15.64N
c = ab:	8.7	18.09
c = a/b:	8.7	18.41

.422 For arrays of data —

$c_i = a_i + b_j$:	5.25	15.64
$b_j = a_i + b_j$:	5.25	15.64
Sum N items:	0.75N	15.64N
$c = c + a_i b_j$:	18.53	36.20

.423 Branch based on comparison —
Numeric data: 5.25
Alphabetic data: 5.25

.424 Switching —
Unchecked: 2.25
Checked: 4.5
List search: 2.25

.425 Format control, per character —
Unpack: 5.9
Compose: 8.98

.426 Table look-up, per comparison —
For a match: 0.75 per comparison, using Repeat instruction.
For interpolation point: 0.75

.427 Bit indicators —
Set bit in separate location: 1.5
Set bit in pattern: 2.25
Test bit in separate location: 0.75
Test bit in pattern: 2.25
Test AND for B bits: 0.75
Test OR for B bits: 3.0

.428 Moving (per full or half word): 2.25 - loop.
1.5 — straight-line coding.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	interrupt.
Underflow:	check	interrupt.
Zero divisor:	—	testable by program.
Invalid data:	check	interrupt.
Invalid operation:	check	interrupt.
Invalid address:	check	interrupt.
Receipt of data:	check	interrupt.
Dispatch of data:	check	interrupt.
Power failure:	check	interrupt.
Guard Mode violation:	check	interrupt.

OPERATING ENVIRONMENT: OMEGA

.1 GENERAL

.11 Identity: . . . . . Omega Operating System.

.12 Description

Omega, the operating system announced for use with the UNIVAC 494, takes advantage of UNIVAC's several years of experience with the REX executive system presently used with the UNIVAC 490, 491, and 492 computer systems. Omega consists of a comprehensive library of programs integrated under supervisory control. It features a variety of language translators and a flexible control system for directing the basic computer operations. The operating system is modular in design, a feature that will permit future additions of language processors and control functions without affecting the performance of existing programs. This modularity will also be valuable in permitting UNIVAC to "retrofit" Omega to the UNIVAC 490, 491, and 492 systems in the future.

Basic machine requirements for Omega include 4,000 to 8,000 30-bit words of core memory and 786,432 words of auxiliary storage. The auxiliary store is used to hold in residence all active system and problem programs, and to serve as a backlog buffering device for input-output operations.

The following list of terms is used by UNIVAC in the documentation that describes the functions of Omega. A brief definition of each term is provided to assist in understanding the Omega concepts as developed by UNIVAC.

- Element — The smallest logical unit of programmed information that can be entered into the system.
- Element Library — a collection of elements, yet not necessarily a complete program.
- Activity — two elements of a single task that are capable of working concurrently.
- Task — a logical collection of elements and activities, equivalent to a program.
- Job — a series of tasks that accomplish a complete data processing function, such as demand deposit accounting.
- Primary Input Stream - a series of job control descriptions that represent the complete UNIVAC 494 scheduled workload for a given portion of the computer center's day.

All of Omega's control facilities are organized to accomplish the following operational objectives:

- Real-Time/On-Line Processing — A priority scheduling system gives the real-time, demand processing requests highest priority. Non-delayed, real-time control is facilitated by a series of hardware checks and interrupts. Programs that attempt memory boundary violations are inhibited, thus ensuring the security of the programs that share internal storage.
- Batch Processing — The operating system controls program selection and job-to-job transition to maximize the utilization of the full system configuration and to minimize the job turn-around time.
- Multiprogrammed Processing — This function is also intended to achieve optimum computer utilization. Omega's multiprogramming control facilities queue program requests, service a program for a certain time interval, and then pass control to the next competing program.

.121 Job Control: External

Omega's External Job Control system refers to the control routine and its control-card images which regulate the programs that are to be executed and the manner in which they are to be executed. After the Job Control specifications have been entered into the system, Omega assumes all further responsibility for obtaining overall concurrent operating efficiency. A description of the individual elements of the job control language follows:

- JOB — identifies the beginning of a specific job control package.
- START — symbolically names the job to be executed.
- LOAD — directs the connecting of discrete program elements to form a program capable of execution.
- GO — initiates the execution of a program.
- ASG — calls for the peripheral devices required for program execution.
- FREE — releases peripheral devices when they are no longer required for program execution.
- SWITCH — swaps one peripheral assignment for another.
- FROM — identifies an input stream from a remote terminal.
- CALL — overrides the standard action of Omega and returns the program output to the site of the input.
- FIN — signals the end of information sent to a particular device.
- LOG — supplies the system operator with information on the status of the scheduled workload.
- SOURCE — introduces corrections to the input data.

.121 Job Control: External (Contd.)

- IN, OUT, PRINT — used for Library Maintenance (see Paragraph .126 for a description of these functions).
- FOR, COB, ASM, SPURT — select and activate specific language processors (see Paragraph .128 for a listing of Omega-controlled processors).
- TEST, UTL, ELM — select and activate specific utility routines.

.122 Job Control: Internal

Omega's internal Job Control system is basically a scheduling system designed to control the flow of jobs and to maximize the use of all available equipment. Omega performs its scheduling functions by sequentially entering job decks into a job stack, and then selecting each job for processing according to preset priorities.

If sufficient core storage and peripheral devices are available, several jobs can be run concurrently in a multiprogramming environment. Individual tasks within each job are selected, and memory allocations and peripheral device assignments are made for as many tasks as possible. Upon completion of each task, the facilities which will no longer be needed for the following task of the job are surrendered. When the last task of each job is completed, post-job processes are automatically initiated to log accounting information and to return control to the next job in the stack.

The scheduling routine generally attempts to select, for concurrent execution, tasks that have counterbalancing demands for peripheral operations and pure bulk computations. Modification of this scheme can be caused by the following factors:

- Service Priority — Real-time processing can demand a precedence over all other scheduled processing. Similarly, non-production tasks, such as program tests, have low priorities.
- Response Priority — In order to obtain maximum utilization and control of the available peripheral devices, the Service Priority of specific elements within a task, such as input-output routines, can be dynamically assigned Response Priorities that will alter the task's original Service Priority. The Service Priority values assigned to any task can range from a high of 0 to a low of 17. Response Priority values range from 0 to 10. During the execution of each task, the combined Service and Response priority value is called the task's Operating Priority.
- Rotation — It is conceivable that a given task could monopolize use of a Central Processor. To prevent this situation from occurring, Omega ensures that any task that has a lower priority than that of the next queued task will not occupy the Central Processor for more than 200 milliseconds. This 200-millisecond limit can be altered by individual installations. Rotation interrupts the processing of a task for one complete turn through the processing of all other active tasks.

In addition to the program-switching caused by the 200 millisecond rotational interrupt, task interruption can also be caused by any other standard hardware interrupt (see Central Processor Section, Paragraph 804:051.33), by the completion of an executed task, or by a service request that cannot be immediately performed.

.123 Allocation Control

The function of Allocation Control is to maintain and regulate the status and availability of the computer system's assignable hardware components. Dynamic control of all available facilities is an essential element in real-time processing.

Allocation Control provides the routines to control program "roll-out" and subsequent "roll-in" when a high-priority task must usurp the facilities (I/O and core storage) of a lower-priority task. In performing a roll-out operation, Omega interrupts the program that is using the desired facilities and generates a status record sufficient to resume processing that program when the same or equivalent facilities are again available. The assigned priority of the interrupted program is automatically increased to lessen the chance of repeated pre-emption of its required facilities. Since a program's peripheral devices and memory locations are symbolically designated and then assigned at execution time according to availability, it is possible that a reinstated program will utilize facilities that are different from those that were being utilized prior to the interruption. If insufficient system facilities are available to perform the roll-out operation, the low-priority program is aborted.

Another system procedure performed by Omega's Allocation Control is called "compacting." Compacting is the process of rearranging programs and data in core storage in order to have available, at all times, the largest possible area of contiguous core storage. In order for a program to be eligible to be moved in the compacting process, it must be temporarily stable (i.e., not currently engaged in an I/O data transfer operation). Since real-time input-output operations are potentially continuous, real-time programs are not moved in the compacting process.

.124 Input-Output Control

Omega provides the centralized I/O control necessary in a multiprogramming environment, coordinating the I/O demands of concurrent users. This control is provided at three levels:

- Device Control — Omega supplies generalized input-output routines to control the operations of the available peripheral devices. User-provided parameter statements for a specific device are referred to as a "packet request." Packet requests are implemented by system control elements called "I/O handlers." The most common I/O handlers, such as Read or Write, are retained in core as permanent residents. Less frequently used handlers, such as error recovery routines, are generally held in secondary storage.
- Cooperative Control — Three input and output utility routines are provided by Omega for use by any or all of the concurrently-operating programs. These cooperative control programs can

(Contd.)

.124 Input-Output Control (Contd.)

be activated by the user by minimum parameter specifications, such as PRINT and the associated file name. The file items to be read, printed, or punched must be of fixed size, and they can be processed only sequentially.

- File Control — These routines provide automatic file handling operations at either the block or item level. A file consists of a collection of either fixed or variable items. Each variable item must contain a length field within its first word for use by the file control routines. File control will handle non-standard as well as standard file conventions in the areas of header and trailer label checking, blocking and deblocking, sequence checking, and hash totaling.

Omega's I/O control system is modular in design, permitting additional facilities to be added to it without necessitating changes in existing user programs.

.125 Logging and Accounting

Omega maintains an operational log for the collection and display of status information pertinent to each task or job and to the system as a whole. The logged accounting information includes a count of I/O requests per peripheral unit, the time period of peripheral unit assignment to each program, and the total amount of central processor time utilized in the execution of each program.

Logged hardware maintenance data includes a detailed history of various transient errors that occurred during a certain period of processing. This information is used to pinpoint certain areas of the system that require diagnostic examination. Other, non-suspect portions of the system can continue to be used during the limited system testing.

.126 System Library

The Omega library contains a table of contents that identifies each element of every program by name, version, and type, and includes any control information necessary for executing the program. The name in the table of contents is a symbolic name associated with the element at the time the program element is written. The "version" designation is used to differentiate similar elements with a program. Also, several different versions of the same program can be contained in the library system, such as a production version and a newer, untested version that includes modifications to the original.

Three logical levels of the Omega library can be referenced: the job library, the group library, and the system library. These levels represent three degrees of permanence in storing the various elements of the library, as described below.

- Job Library — A job library is created by Omega from control language statements each time a given job is executed. The function of the job library is to provide the linkage between the several tasks of each job. The Job Library is initially created by Omega's library maintenance function (IN) or by program elements that are generated or referenced during job execution. A given job library is transient and remains in the system only as long as the program is being executed, unless the library maintenance function (OUT) is called to save the current job library.
- Group Library — The group library is a compromise between the impermanence of the job library and the permanence of the system library. The group library consists of a set of job library linkage elements that can be loaded once and then shared by a series of successive jobs.
- System Library — The system library is a permanent part of the operating system and is held in random-access storage. It consists of standard subroutines, standard object programs of the manufacturer and the user, a master-file directory, and registered data files. The system library cannot be altered by Omega's standard library maintenance procedures. The question of how system library modification can be accomplished has been left unanswered to date.

.127 User Programs and Language Processors

The creation of user programs is facilitated by the provision of a group of language processors that produce a common form of object code that allows the effective merging of segments written in different source languages. Control of the various compilers and integration of the final object program is managed by Omega. Program testing is performed by an automatic system that provides dynamic control of the test and protection of any other programs that are concurrently being processed.

The language processors supplied with Omega include:

- SPURT II — a symbolic assembly language that provides inter-family source language compatibility with the other 490 Series computer systems. SPURT II is the basic 490 Series assembly language; see Report Section 800:171.
- 494 Assembler — a new assembly language designed to provide a language capable of fully utilizing the 494's improved facilities. This assembler is quite similar to the SLEUTH assembler first used on the UNIVAC 1107 computer system.
- FORTRAN IV — a language and compiler based on the A. S. A. FORTRAN specifications as defined in Communications of the ACM, October 1964; see Report Section 800:162.
- COBOL — a language and compiler based on the Department of Defense report, COBOL Preliminary Edition, 1964; see Report Section 800:161.

Other software facilities available through Omega include UNIVAC routines to perform the following functions: communications network simulation, linear programming, PERT/Cost, report program generation, and sorting and merging.

.128 Diagnostic Facilities

Omega's testing procedure can interpretively execute the program in test by using the symbol tables generated by the compilers as sources of symbolic program test points and data areas. Relative reference diagnostics are also provided for testing absolute programs that lack symbol tables. The test routines include conditional snapshot dumps, a set value procedure for either inserting program patches or setting test condition values, and postmortem dumps of core storage and/or

.128 Diagnostic Facilities (Contd.)

specifically designated logical units. Each of these functions is activated by control statements contained in the input job stream.

Programs initiated under control of Omega's test system are interpretively executed until an "end condition" occurs. The recognizable end conditions include:

- Program end-of-job;
- Program attempt to store or jump to a memory location outside its assigned limits;
- An unsolicited operator entry indicating that the program is in a loop;
- A program request for a common routine not previously defined as legal;
- Exceeding a pre-designated time limit on program execution.

An end condition will automatically result in dumping of the operational registers and writing of other descriptive diagnostics.

.129 Summary

The Omega operating system provides a comprehensive foundation for the control of sophisticated multiprogramming and multiprocessing installations with real-time capabilities. However, considerable knowledge is required of the individual who is responsible for designing such a 494 installation. He must be completely familiar with the UNIVAC 494 hardware, all phases of the operating system, and the data processing goals to be accomplished. It may be true that the skill required of this individual need be no greater than that required of a person who designs a good batch processing system; but the penalty for poor design of a large-scale, real-time 494 installation is potentially much greater than that paid for an inefficient batch processing system.

.13 Availability

For UNIVAC 494: . . . . June 1966.
For remainder of the UNIVAC 490 Series: . April 1967.

.14 Originator: . . . . . UNIVAC Division, Sperry Rand Corp.

.15 Maintainer: . . . . . UNIVAC Division, Sperry Rand Corp.

.2 PROGRAM LOADING

.21 Source of Programs: . . all programs available to the system are held in random-access storage.

.22 Library Subroutines: . . library subroutines are held in random-access storage (except for the most common I/O routines, which are held in core memory).

.23 Loading Sequence: . . . loading of programs into a job stack from an external device is performed sequentially. Execution of the tasks within the jobs is performed according to the priority of each task.

.3 HARDWARE ALLOCATION

.31 Storage: . . . . . a program occupies one contiguous area of core memory. The location of this area can be changed during the execution of the program to better accommodate other concurrently operating programs and data.

.32 Input-Output Units: . . . assignment of peripheral units is controlled by Omega as described in Paragraph .124.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: controlled by Omega.

.42 Multiprogramming: . . . controlled by Omega as described in Paragraph .122.

.43 Multiprocessing: . . . . . the UNIVAC 494 has the facility to allow up to three central processors to share core memory. Omega allows two processors to access core memory at a time (one in the odd bank, the other in the even). Task activation by either processor is based on the waiting tasks' relative priorities.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Parity error — instruction:	hardware check	interrupt, check read, log or remove from the system.
Parity error — I/O:	hardware check	interrupt, exercise and log, or remove from system.
Power failure:	hardware check	lock out interrupts, save registers, and set time delay.
Guard Mode interrupt:	hardware check	drop the offending task from further execution.
Floating-point overflow:	hardware check	set program switch, assume maximum magnitude number, and continue program.
Floating-point underflow:	hardware check	set program switch, assume zero value, and continue program.
Illegal instruction:	hardware check	drop the offending task from further execution.
I/O interrupts:	hardware check	repeat attempt and log.

(Contd.)

.45 Restarts

.451 Establishing restart points: . . . . . checkpoint facilities are provided to record the current status of a program.

.452 Restarting process: . . can be operator-initiated; in the case of a transient power failure, Omega recovers automatically.

.5 PROGRAM DIAGNOSTICS: . . . . . called as required (see Paragraph .128 for a description of Omega diagnostic facilities).

.6 OPERATOR CONTROL: . . . . . communication is provided through a console typewriter.

.7 LOGGING: . . . . . provided by Omega (see Paragraph .125).

.8 PERFORMANCE

.81 Routine Loading Time: . . . . . the speed at which a program is entered into a central processor is a function of the priority assigned to that program and the speed of the auxiliary storage device.

.82 Reserved Equipment

Core storage: . . . . . 4K to 8K words.
Auxiliary storage: . . . 786K minimum.
System input device*: . . card reader or magnetic tape unit.
System output device, primary*: . . . . . high-speed printer or magnetic tape unit.
System output device, secondary*: . . . . . card punch or magnetic tape unit.
System origin: . . . . . a tape unit is required for constructing the system library on random-access storage.
System clocks: . . . . . the day clock and internal timer are required and directly controlled by Omega. Time functions are available to the user by direct service request.
System console: . . . . . the console typewriter is permanently assigned to Omega.

.83 Running Overhead: . . . UNIVAC states that the amount of overhead time imposed by Omega is highly variable. The degree of efficiency in overall system design will directly affect the operating efficiency of Omega.

* These devices can also be used for the user's problem programs.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (804:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

Because the UNIVAC 494 can process several independent programs at the same time through multiprogramming, the amount of central processor time required by each program is highly significant. The difference (if any) between the total elapsed time for a particular run and the amount of central processor time required for that run represents processor time that is potentially available to other programs. Whether or not this processor time can be efficiently utilized depends upon the system configuration, the overall problem mix, and the effectiveness of the scheduling and operating system.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configurations VIIA and VIIIA where all four input-output files are on magnetic tape, total times were computed for cases using both unblocked and blocked records in the detail and report files. Central processor time is essentially the same for all configurations, and is shown by the line marked "CP" on each graph. No addition has been made to the processor time to cover the overhead requirements of the operating system. All processor times are for dual-bank operation (i.e., overlapped core memory accesses).

Worksheet Data Table 1 (page 804:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for Configurations III and V. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a fraction of the total processing time. When other programs with limited input and output can be run simultaneously in order to utilize the remaining processor time, it may be satisfactory to operate the UNIVAC 494 as just described. In other cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-print transcription of the report file. The curves for Configurations VIIA and VIIIA show the time required for the all-tape main processing run. The card-to-tape and tape-to-printer transcriptions will run at card reader and printer-limited speeds, and their demands on the processor will be small. The elapsed time and central processor time for the data transcription runs are shown on a separate graph (804:201.150).

The master file record format is a mixture of alphameric and binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. Even so, most of the central processor time is devoted to editing, radix conversion, and character manipulation operations. Packing was kept to a minimum because of the high demands it would place upon the UNIVAC 494 Central Processor. The resulting master file record length is 21 words (the equivalent of 105 6-bit characters).

SORTING (804:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the Users' Guide, Paragraph 4:200.213, using a three-way merge.

MATRIX INVERSION (804:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplication ($c = c + a_i b_j$) using the standard double-precision floating-point hardware. The processor time required for a matrix inversion can be spread over a much longer total elapsed time when the inversion is multi-run with other programs that utilize the available input-output equipment. Multi-running of other programs necessarily decreases the amount of internal storage that can be allocated to the matrix inversion.

GENERALIZED MATHEMATICAL PROCESSING (804:201.4)

The standard estimating procedure outlined in the Users' Guide, Paragraph 4:200.413, was used. Computation includes 5 fifth-order polynomials, 5 divisions, and 1 square root. The double-precision floating-point mode, which provides a precision of about 14 decimal digits, was used because it is the only form of floating-point arithmetic for the UNIVAC 494.

WORKSHEET DATA TABLE 1

	ITEM		CONFIGURATION								REFERENCE
			III, V		VIIA & VIIIA, Files 3 & 4 Blocked*			VIIA & VIIIA, Files 3 & 4 Unblocked			
1 Input Output Times	Char/block	(File 1)	1,050		1,050			1,050			4:200.112
	Records/block	K (File 1)	10		10			10			
	msec/block	File 1 = File 2	48.5		19.6			19.6			
		File 3	66.7		17.1*			9.98			
		File 4	127.7		21.4*			10.57			
	msec/switch	File 1 = File 2	0		0			0			
		File 3	0		0			0			
		File 4	0		0			0			
	msec penalty	File 1 = File 2	0.47		0.47			0.47			
		File 3	0.04		0.36*			0.04			
		File 4	0.06		0.61*			0.06			
2 Central Processor Times	msec/block msec/record msec/detail msec/work msec/report	a_1	0.022		0.022			0.022			4:200.1132
		a_2	0.053		0.053			0.053			
		b_6	0.377		0.377			0.377			
		$b_5 + b_9$	0.100		0.100			0.100			
		$b_7 + b_8$	0.862		0.862			0.862			
3 Standard File Problem A F = 1.0	msec/block for C.P. and dominant column.		C.P.	Printer	C.P.	VIIA	VIIIA	C.P.	VIIA	VIIIA	4:200.114
		a_1	0.022		0.022			0.022			
		a_2K	0.527		0.527			0.527			
		a_3K	13.392		13.392			13.392			
		File 1: Master In	0.047		0.047	19.6		0.047			
		File 2: Master Out	0.047		0.047			0.047			
		File 3: Details	0.036		0.036			0.036	19.06		
		File 4: Reports	0.061	1,277	0.061	21.4	21.4	0.061	104.72	104.72	
		Total	14.132	1,277	14.132	41.0	21.4	14.132	123.78	104.72	
4 Standard File Problem A Space	Unit of measure	(30-bit words)									4:200.1151
		Std. routines	4,000 (Omega)		4,000 (Omega)			4,000 (Omega)			
		Fixed	---		---			---			
		3 (Blocks 1 to 23)	165		165			165			
		6 (Blocks 24 to 48)	2,346		2,346			2,346			
		Files	924		1,680			924			
		Working	50		50			50			
		Total	7,485		8,306			7,485			

	ITEM			CONFIGURATION		REFERENCE
				III, V	VIIA, VIIIA	
Standard Mathematical Problem A	Fixed/Floating point			Floating	Floating	4:200.413
	Unit name	input		800/900-cpm reader	Uniservo VIIIC	
		output		700/922-lpm printer	Uniservo VIIIC	
	Size of record	input		80 char	80 char	
		output		135 char	132 char	
	msec/block	input	T_1	75.0	6.8	
		output	T_2	127.7	7.4	
	msec penalty	input	T_3	0.04	0.04	
		output	T_4	0.06	0.06	
	msec/record		T_5	1.045	1.045	
	msec/5 loops		T_6	0.606	0.606	
	msec/report		T_7	0.634	0.634	

*10 records per block in Files 3 (detail) and 4 (report).

(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes —
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

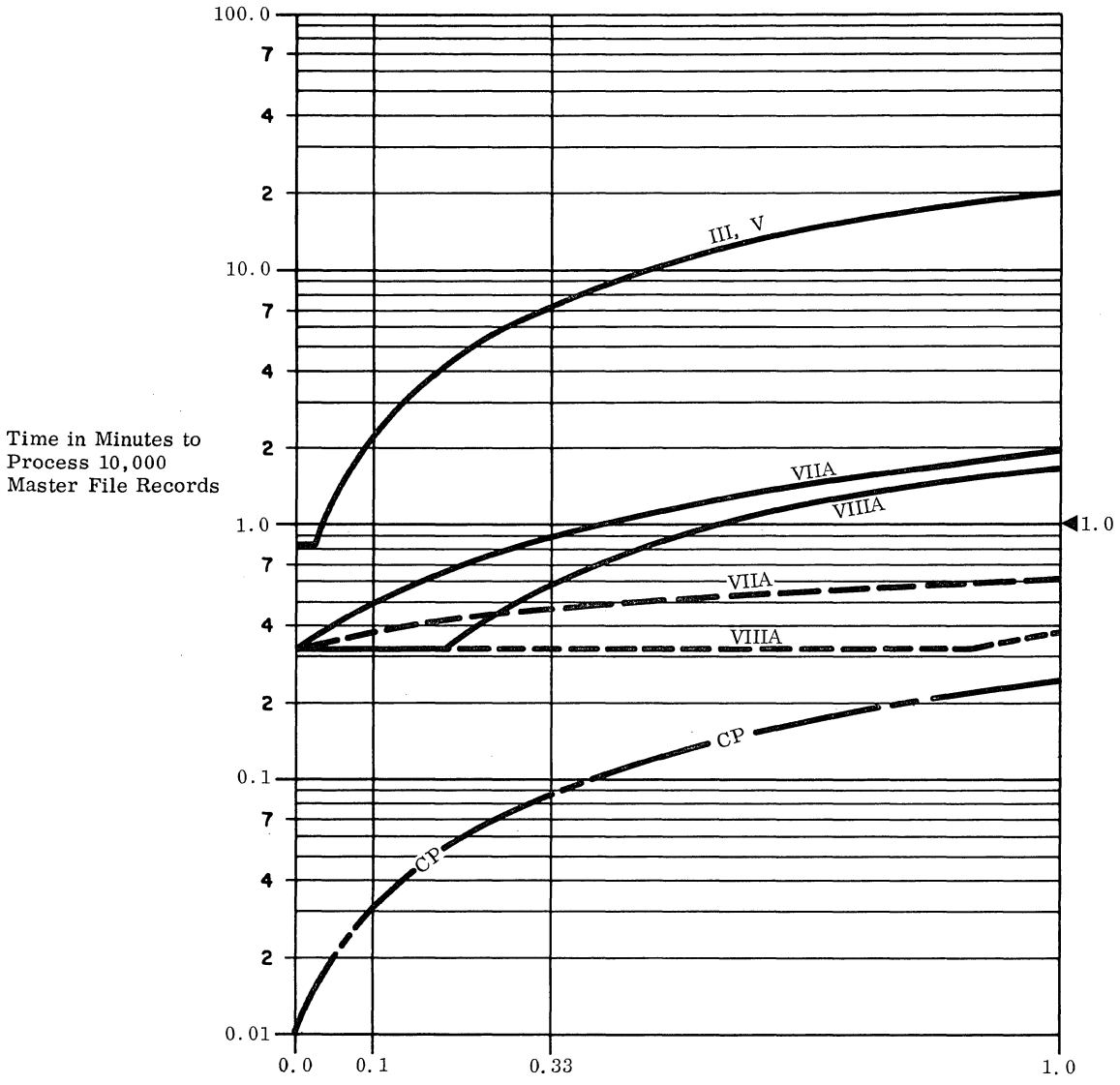
.112 Computation . . . . . standard.

.113 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.11.

.114 Graph: . . . . . see graph below.

.115 Storage space required —
Configurations III,
V: . . . . . 7,500 words.*
Configurations VIIA,
VIIIA (unblocked
Files 3 & 4): . . . . 7,500 words.*
Configurations VIIA,
VIIIA (blocked
Files 3 & 4): . . . . 8,300 words.*

*Includes 4,000 words reserved for Omega operating system.



(Roman numerals denote standard System Configurations.)

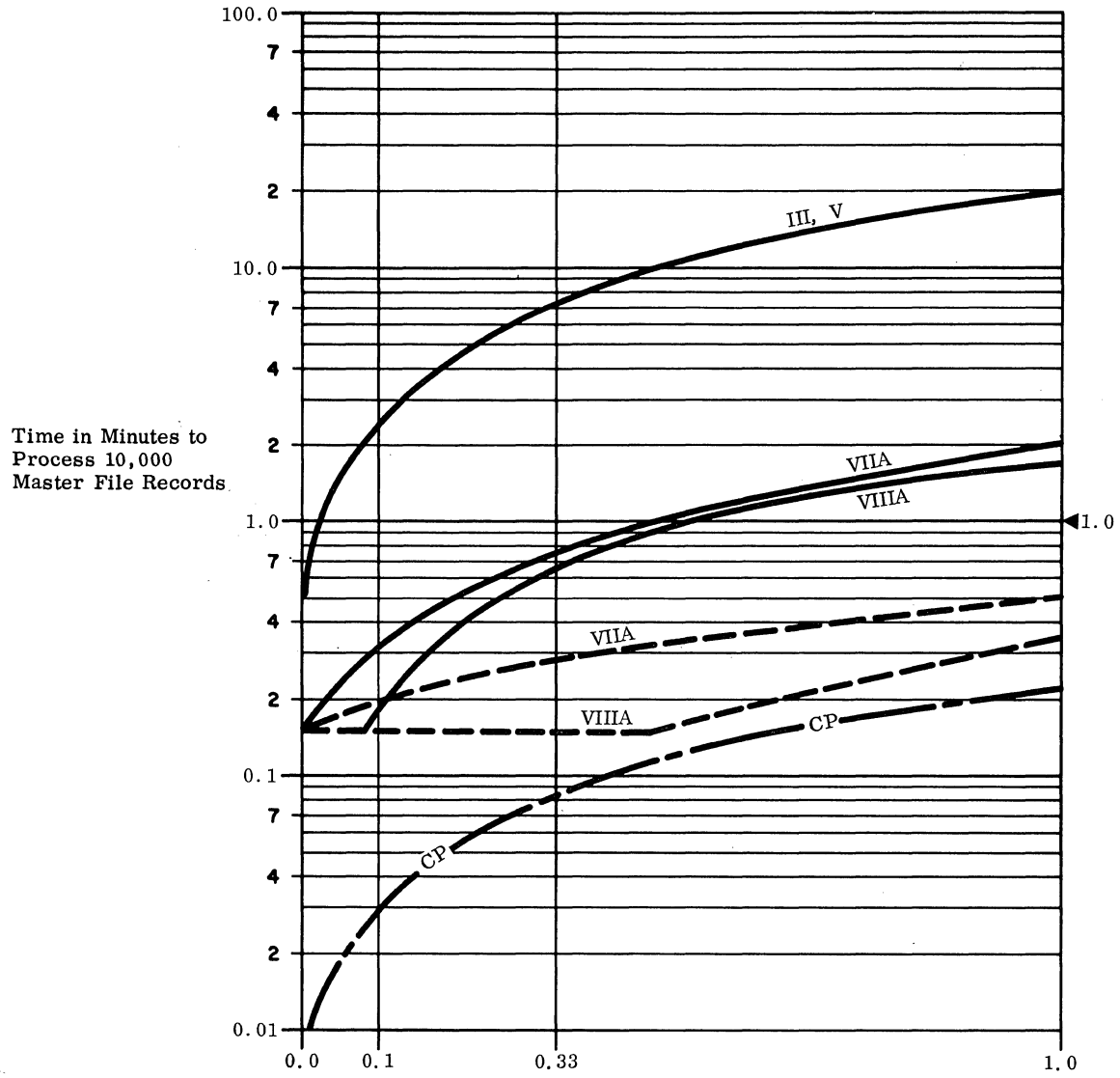
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

.12 Standard File Problem B

.121 Record sizes —
Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

LEGEND

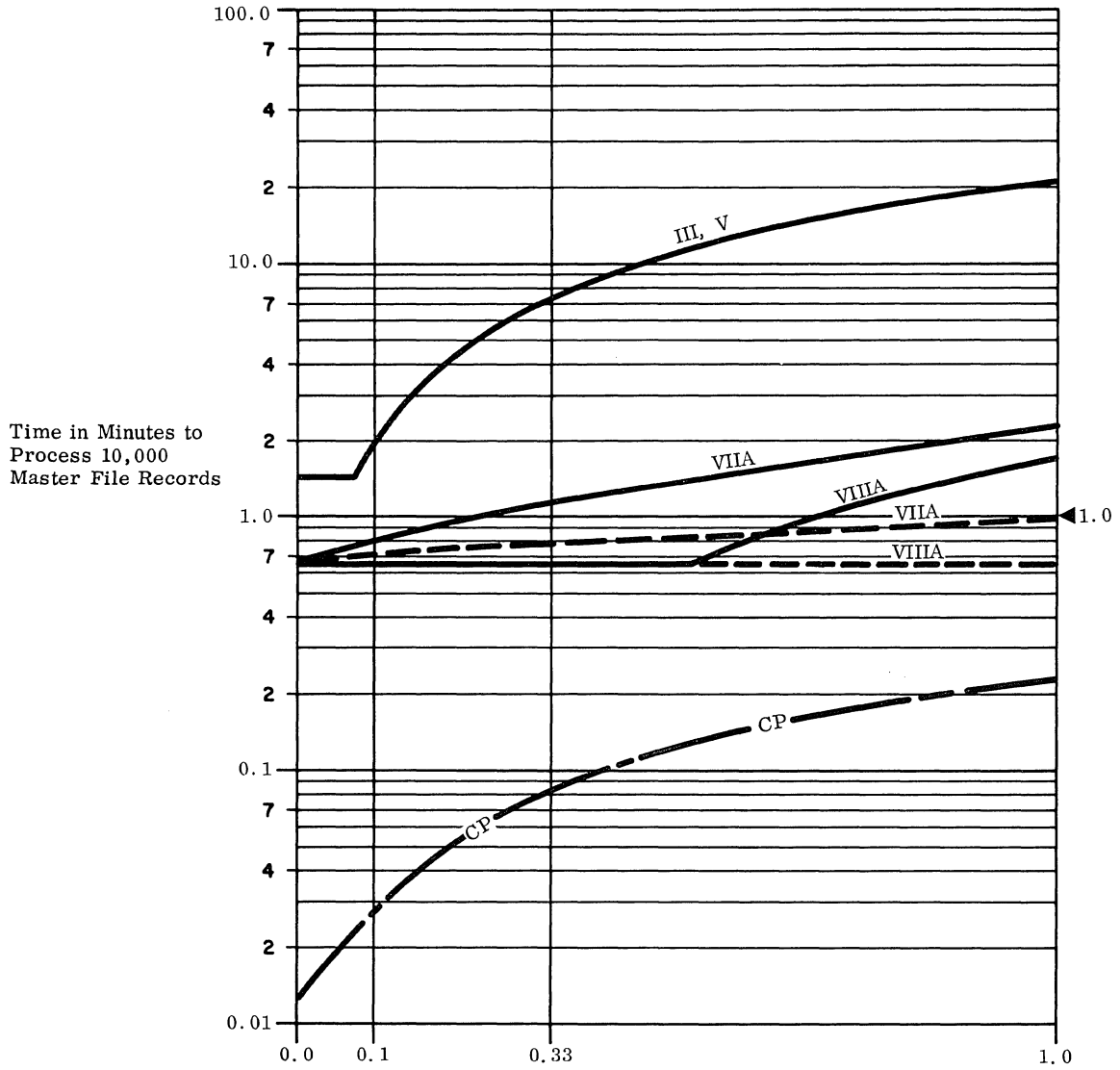
Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

(Contd.)

.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard.
.133 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

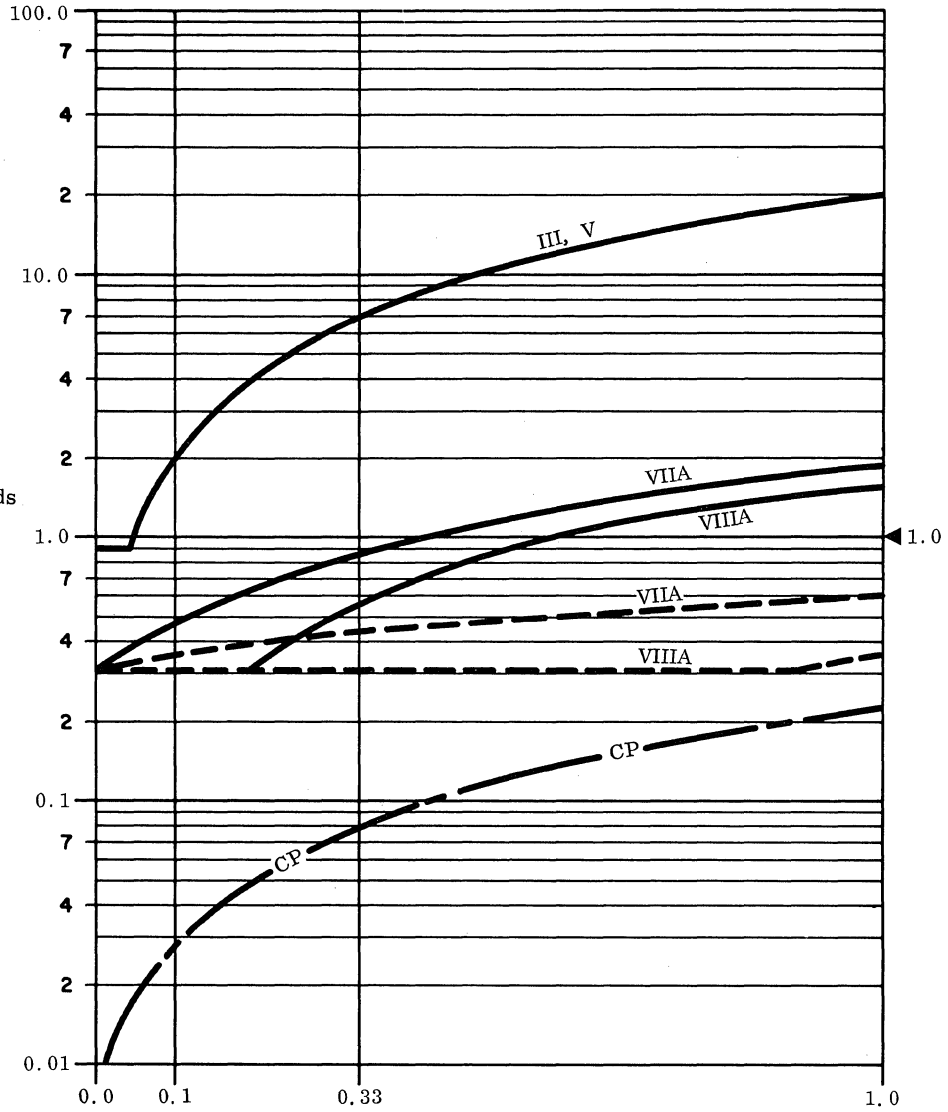
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

.14 Standard File Problem D

.141 Record sizes —
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . . see graph below.



Time in Minutes to Process 10,000 Master File Records

Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

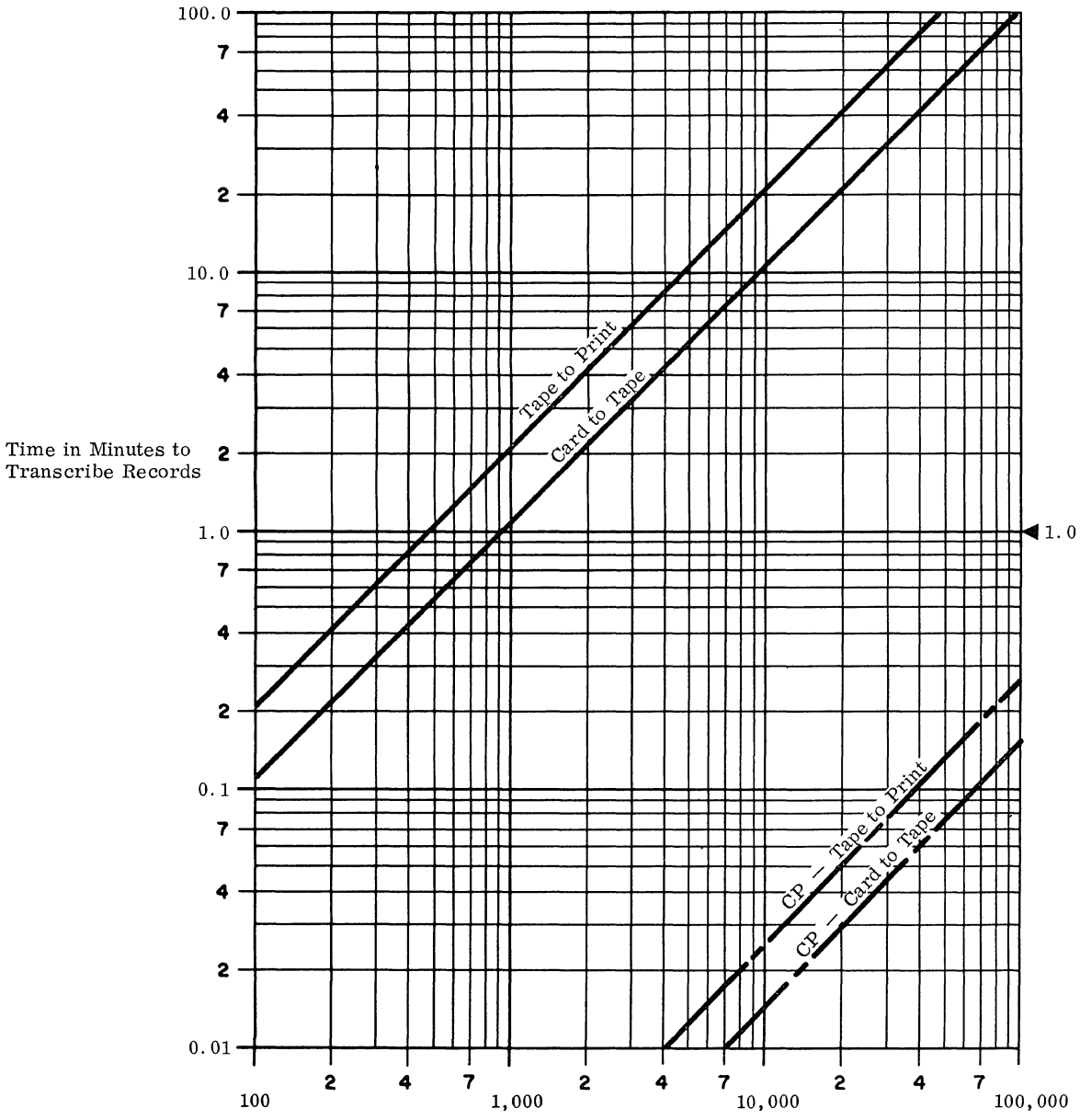
(Contd.)

.15 Data Transcription Runs for Standard File Problems

.151 Block sizes —
Detail file (on cards): . . . . . one card.
Report file (on printer): . . . . . one print line.

.153 Timing basis: . . . . . data is transcribed directly from cards to tape or tape to printer; no editing is performed during these runs.

.154 Graph: . . . . . see graph below.

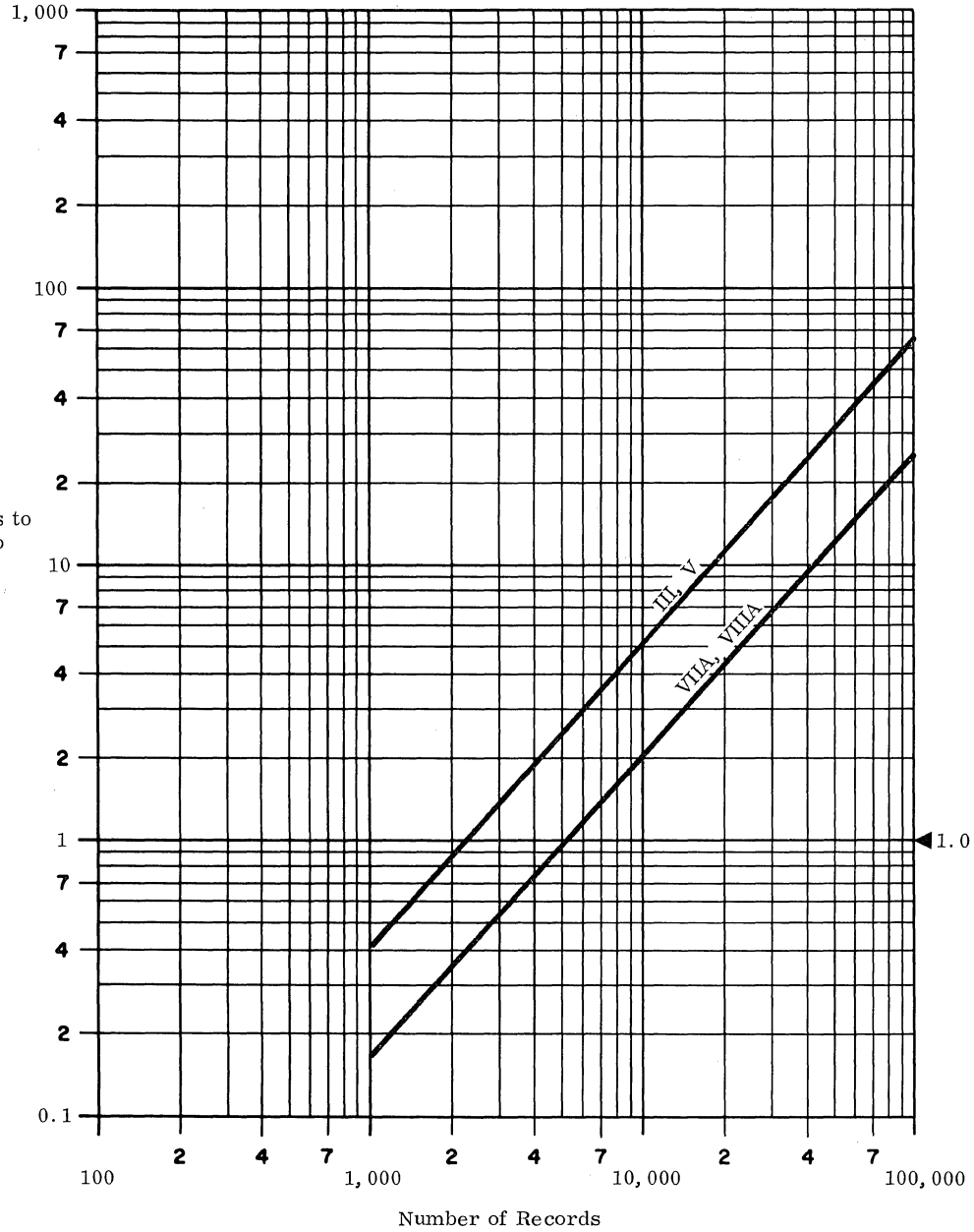


(Graph applies to Standard Configurations VIIA and VIIIA; lines marked "CP" denote Central Processor times.)

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.
.212 Key size: . . . . . 8 characters.
.213 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.213; 3-way tape merge.
.214 Graph: . . . . . see graph below.



(Roman numerals denote standard System Configurations.)

(Contd.)

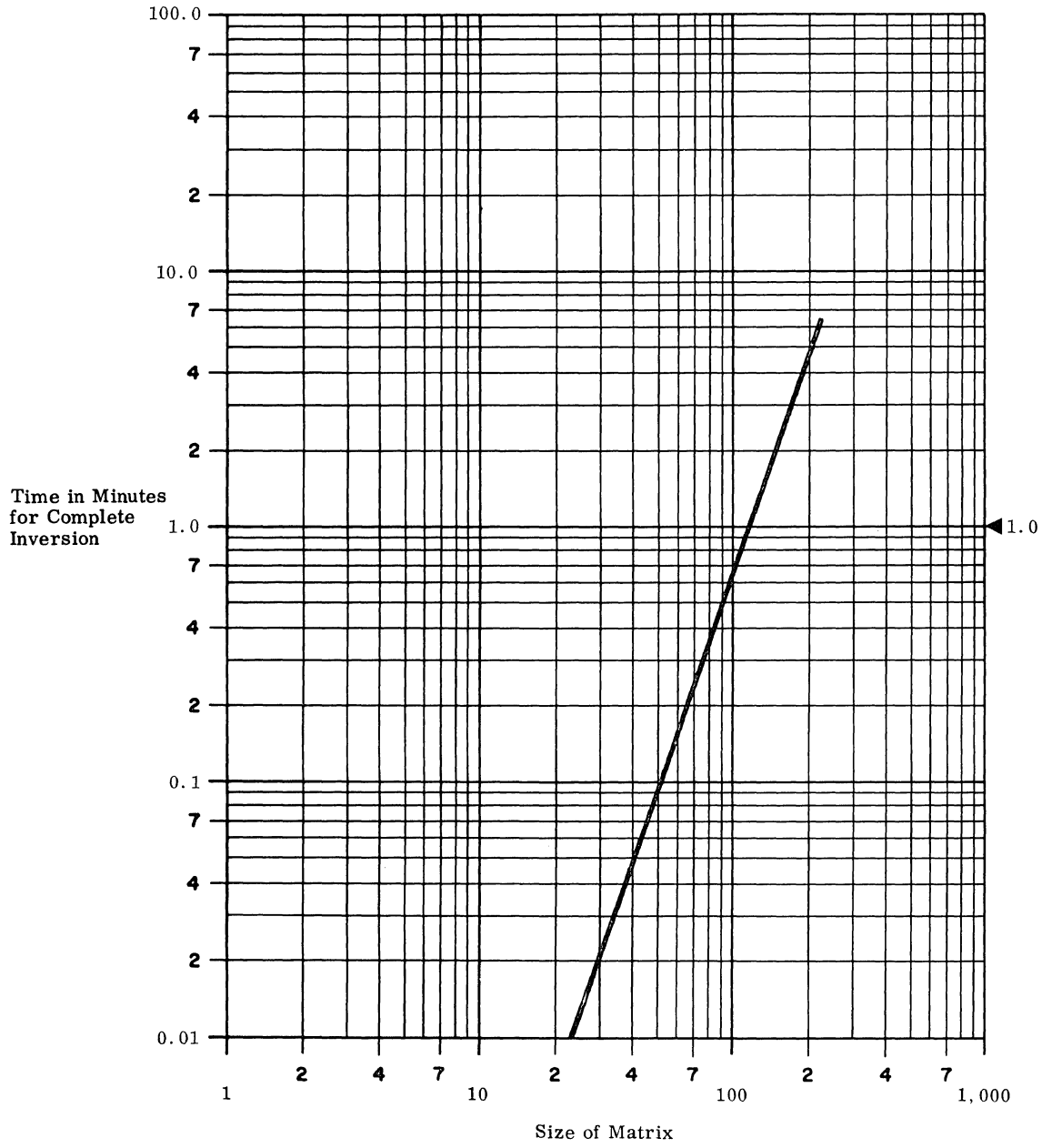
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters:. . general, non-symmetric matrices, using floating point to at least 8 decimal digits precision.

.312 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312; 14-digit-precision floating-point arithmetic is used; indicated times are for dual core memory banks; single-bank times are 18% slower.

.313 Graph: . . . . . see graph below.



.4 GENERALIZED MATHEMATICAL PROCESSING

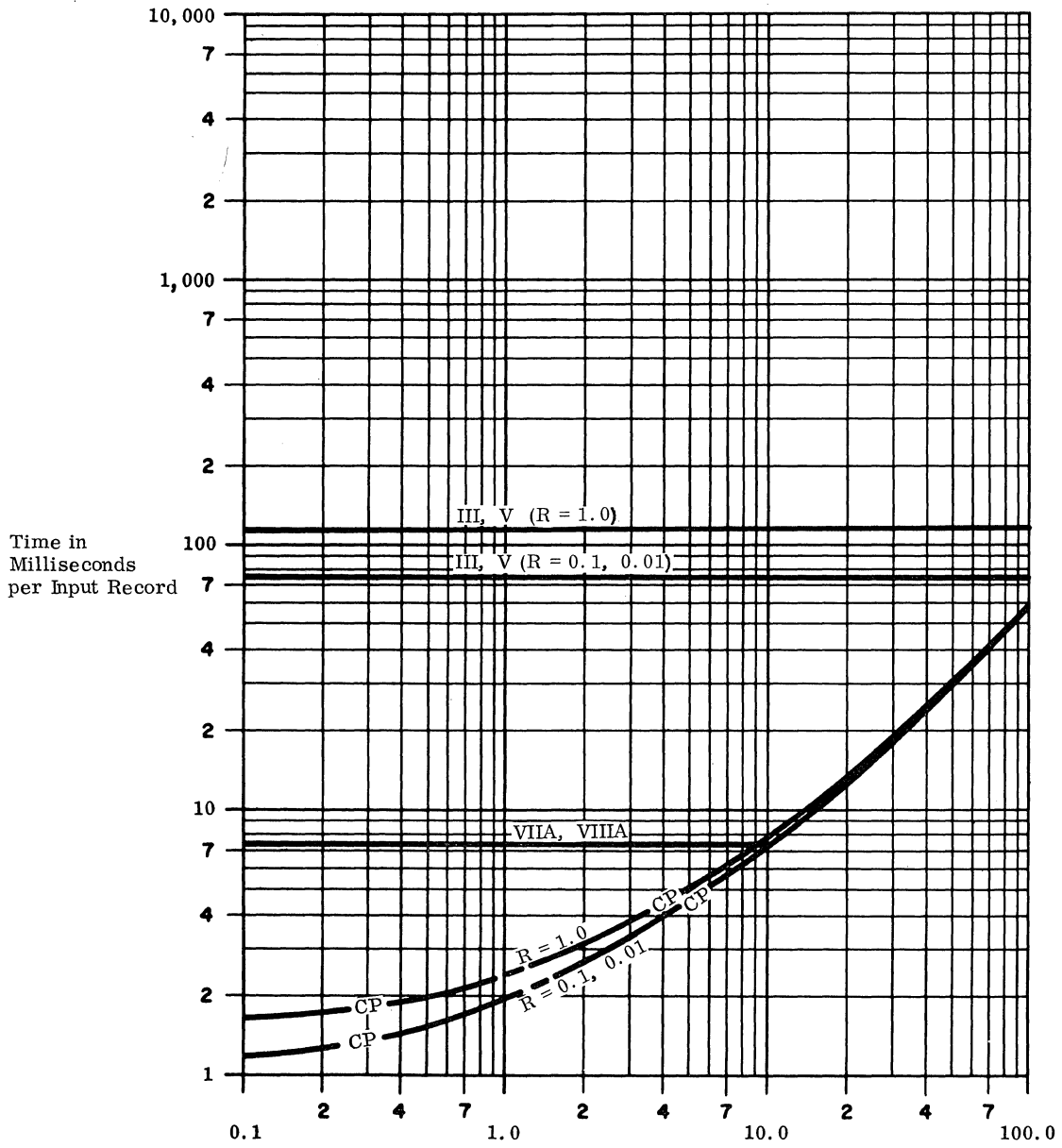
.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . 10 signed numbers; average size 5 digits, maximum size 8 digits.

.412 Computation: . . . . . 5 fifth-order polynomials, 5 divisions, and 1 square root; computation is performed in 14-digit-precision floating-point mode.

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . . see graph below.

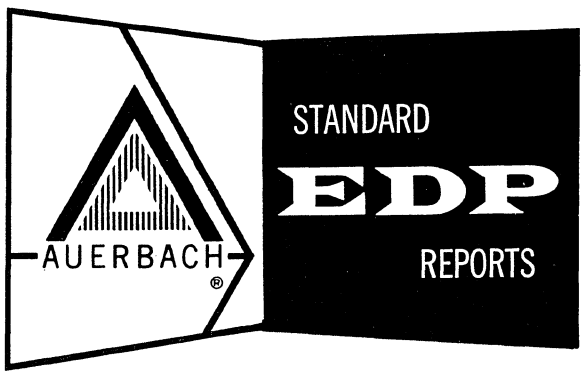


(Roman numerals denote standard System Configurations; R = number of output records per input record; curve marked "CP" shows central processor time.)

UNIVAC 9000 SERIES

Univac

(A Division of Sperry Rand Corporation)



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UNIVAC 9000 SERIES

Univac

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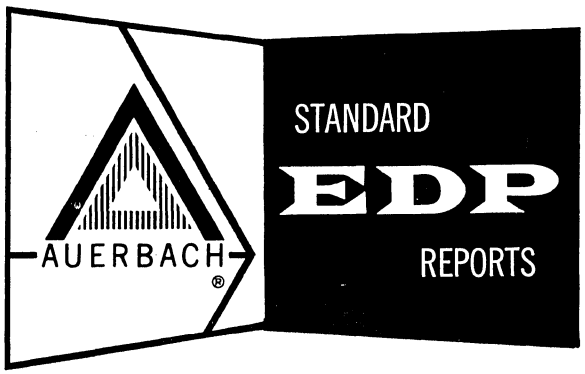

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ADVANCE REPORT: UNIVAC 9000 SERIES

.01 INTRODUCTION

The UNIVAC Division of Sperry Rand Corporation unveiled the UNIVAC 9200 and 9300, the first two members of its long-awaited 9000 Series computer family, on June 21, 1966. Although the 9200 and 9300 systems are small-scale computers designed for business applications, UNIVAC states that the 9000 Series will eventually span the small, medium, and large-scale computer market. The UNIVAC 9500, a medium-scale computer with multiprogramming and real-time capabilities, will probably be announced this Fall. Still larger models are being planned for future announcement.

The UNIVAC 9000 Series computers employ plated-wire main memories (the first commercial use of this promising storage technique) and monolithic integrated circuits. Both of these technological innovations promise improved performance, economy, and reliability. Perhaps of even greater significance to prospective buyers, however, is UNIVAC's decision to make its 9000 Series computers System/360-compatible with respect to data structure, codes, input-output media, and source-language programming. This decision by UNIVAC, which is widely regarded as the number two computer manufacturer and a leader in technology, represents a giant step toward improved communication among computers, lower reprogramming and retraining costs, lessened dependence upon a single equipment supplier, and greater standardization throughout the industry.

The UNIVAC 9200 is an internally-programmed punched card computer that provides high internal processing speeds at rock-bottom prices, although its input-output speeds are somewhat below par for third-generation equipment. The 9200 will be marketed primarily as a first step into stored-program data processing for users of punched card tabulating equipment and of UNIVAC's own highly successful, plugboard-programmed 1004 Card Processors. The 9200 will be competing with systems such as the IBM System/360 Model 20, the Honeywell 120, and the GE-115 — and it is clear that the 9200's lower cost will make it a formidable contender for this important segment of the computer market.

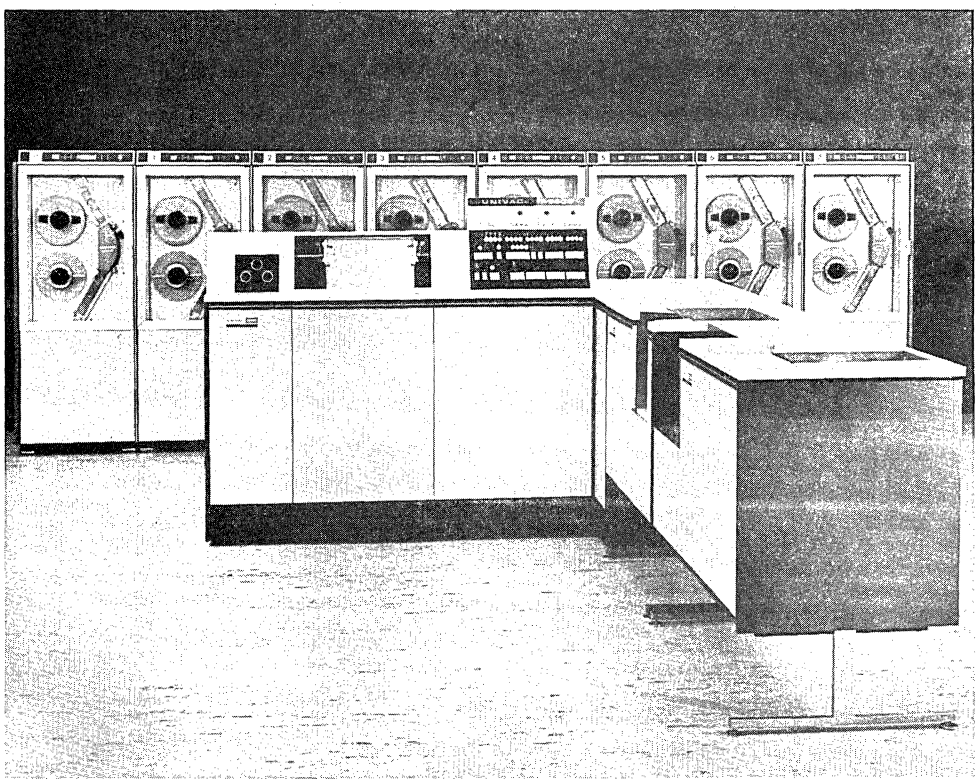

Figure 1. An 8-tape UNIVAC 9300 system.

.01 INTRODUCTION (Contd.)

A basic 9200 system, containing 8,192 bytes of plated-wire memory, 250-lpm printer, 400-cpm reader, and 75-to-200-cpm punch, can be rented for $1,040 per month or purchased for approximately $40,000. Under a 5-year lease agreement, the monthly rate drops to $925. Deliveries are scheduled to begin in June 1967.

The UNIVAC 9300 can be used either as a punched card system with higher computing and input-output speeds than the 9200 or as a low-cost magnetic tape system. It will be suitable for use as a stand-alone computer for a wide range of business applications or as a satellite computer to perform card-to-tape and tape-to-printer transcriptions for larger computer systems. The 9300's 600-nanosecond memory cycle time is the fastest in its price class. Instruction execution times are comparable to those of the more expensive IBM System/360 Model 30.

UNIVAC 9300 system rentals will range from about $1,675 to $9,300 per month, and purchase prices will range from about $63,000 to $350,000. A tape-oriented system with sort/merge capability (three tape handlers) can be rented for less than $3,000 per month. Deliveries of the 9300 are scheduled to begin in September 1967.

Because of UNIVAC's decision to introduce the two low-end models first, it is too early to evaluate the overall competitive position of the UNIVAC 9000 Series in relation to other third-generation computer families such as the IBM System/360 and the Honeywell Series 200. The limited line of peripheral equipment announced to date includes no mass storage, communications controllers, display devices, high-performance magnetic tape units, optical character readers, or punched tape equipment. The announced software facilities are more than adequate to support the small-scale 9200 and 9300 systems but represent no significant innovations in software design. Therefore, a definitive analysis of the new UNIVAC line's strengths and weaknesses in the hotly competitive general-purpose computer market must be postponed at least until UNIVAC announces the medium-scale UNIVAC 9500 and the associated peripheral equipment and software.

.02 DATA STRUCTURE

The basic unit of data storage in the UNIVAC 9000 Series, as in the IBM System/360, is the 8-bit byte, which consists of eight data bits plus (in memory) a parity bit. The eight data bits in a byte can represent one alphanumeric character, one or two decimal digits (depending upon whether the "packed" or "unpacked" format is used), or a portion of a binary field.

Bytes can be handled individually or grouped together into fields. A "halfword" is a group of two consecutive bytes, or 16 bits. Binary numbers in the UNIVAC 9200 and 9300 are represented by signed halfwords (sign plus 15 data bits). Instructions are four or six bytes (32 or 48 bits) in length.

Decimal arithmetic is performed upon 4-bit BCD digits packed two to a byte, with a sign in the rightmost four bits of the low-order byte. Decimal operands can be up to 16 bytes (31 digits and sign) in length.

.03 SYSTEM CONFIGURATION

.031 UNIVAC 9200 Configurations

The basic UNIVAC 9200 system includes a 9200 Processor with a built-in 250-lpm printer; 8K, 12K, or 16K bytes of plated-wire memory; a 400-cpm card reader; and a column card punch rated at 75 to 200 cpm. Only one of each of the basic I/O devices can be connected. Optional features available for the processor and I/O devices are described in the appropriate sections of this report.

A UNIVAC 1001 Card Controller can be connected via the optional Multiplexor I/O Channel and a 1001 Control. The Multiplexor I/O Channel can accommodate up to eight control units, but the 1001 is the only peripheral device currently offered for connection to a 9200 system in this manner.

Typical Card System; Standard Configuration I*

Equipment	Monthly Rental
1 — 9200 Processor, including 250-lpm Printer	$330
1 — Multiply/Divide/Edit feature	75
1 — 120 Print Positions feature	120
1 — 8K Wire Memory (8,192 bytes, 1.2 μsec cycle)	375
1 — 400-cpm Card Reader	135
1 — Column Card Punch (75-200 cpm)	200
Total Rental:	$1,235

* It should be noted that the 9200's printing, card reading, and card punching speeds are all significantly lower than the speeds called for by the specifications for Standard Configuration I (Section 4:030 of the Users' Guide).

(Contd.)

.032 UNIVAC 9300 Configurations

The basic UNIVAC 9300 system includes a 9300 Processor with a built-in 600-lpm printer; 8K, 12K, 16K, or 32K bytes of plated-wire memory; a 600-cpm card reader, and a column card punch rated at 75 to 200 cpm. Only one of each of the basic I/O devices can be connected.

The optional Multiplexor I/O Channel permits connection of a 1001 Card Controller, a 200-cpm Row Punch, and/or Uniservo VI C magnetic tape units. The Multiplexor Channel can accommodate up to eight control units. The 1001 Card Controller can be connected to one control-unit position via a 1001 Control. Each Uniservo VI C Control occupies one control-unit position and can control up to eight tape handlers; see Paragraph .091 for Uniservo VI C configuration details.

Typical Card System; Standard Configuration I

Equipment	Monthly Rental
1 — 9300 Processor, including 600-lpm Printer	$725
1 — Multiplexor I/O Channel (for Row Punch)	75
1 — 8K Wire Memory (8,192 bytes; 0.6 μsec cycle)	550
1 — 600-cpm Card Reader	200
1 — 200-cpm Row Punch	310
Total Rental:	$1,860

6-Tape Business System; Standard Configuration III

Equipment	Monthly Rental
1 — 9300 Processor, including 600-lpm Printer	$725
1 — Multiplexor I/O Channel	75
1 — 16K Wire Memory (16,384 bytes; 0.6 μsec cycle)	1,000
1 — 600-cpm Card Reader	200
1 — Column Card Punch (75-200 cpm)	200
1 — Uniservo VI C Magnetic Tape Subsystem (control unit, 1 master handler, and 1 slave handler)	875
1 — Uniservo VI C Master Tape Handler	500
3 — Uniservo VI C Slave Tape Handlers	900
Total Rental:	$4,475

.04 INTERNAL STORAGE

.041 Plated-Wire Memory

Probably the most significant technical innovation in the UNIVAC 9000 Series is the use of plated-wire memory for the main working storage. The plated-wire memory operates in a nondestructive readout (NDRO) mode, eliminating the need for the regenerative cycle which is required after every read operation in conventional magnetic core memories. Furthermore, most of the plated-wire manufacturing and testing operations can be carried out in continuous, automated processes. For these reasons, UNIVAC claims that its plated-wire memories can be offered with higher speeds and at lower costs than the core memories which are used in nearly all current computer systems.

The plated-wire memory is a magnetic storage device of the thin-film type. The substrate is a beryllium copper wire, 0.005 inch in diameter. The manufacturing process consists of electroplating an iron nickel alloy over an initial plating of copper. Plating is performed while the wire is in the presence of a circumferential magnetic field that is created by the passage of current through the wire itself. The wire that provides a base for the thin-film material also becomes an integral part of the read/write circuitry: it serves as the sense line during read operations and carries write current during write operations.

The UNIVAC 9200 has a memory cycle time of 1.2 microseconds per one-byte access, and memory capacities of 8,192, 12,288, and 16,384 bytes are available. The UNIVAC 9300's memory cycle time is 600 nanoseconds (0.6 microsecond) per one-byte access, and the available capacities are 8,192, 12,288, 16,384, and 32,768 bytes. Memory sizes can be increased at any time by field-installing additional modules. Every byte read from memory is checked for proper (odd) parity.

.042 Mass Storage

No mass storage devices have been announced to date for use with the 9000 Series. It is likely, however, that some of UNIVAC's existing drums, and other mass storage equipment which the company is currently developing, will be offered within the next few months.

.05 CENTRAL PROCESSORS

The UNIVAC 9200 and 9300 Processors are functionally identical; they differ only in internal speeds (the 9300 is twice as fast), in the complement of I/O devices that can be connected, and in the fact that the Multiply, Divide, and Edit facilities are extra-cost options in the 9200 and standard features in the 9300. Table I summarizes the basic characteristics and capabilities of the two systems.

TABLE I: CHARACTERISTICS OF THE UNIVAC 9200 AND 9300

SYSTEM	9200	9300
Memory cycle time, microseconds	1.2	0.6
Bytes accessed per cycle	1	1
Memory capacity, bytes	8K, 12K, or 16K	8K, 12K, 16K, or 32K
General registers	8	8
I/O control registers	8	8
Multiply, Divide, Edit instructions	Optional	Standard
Processor speeds, microseconds (signed 5-digit operands) —		
c = a + b	187.2	93.6
b = a + b	103.2	51.6
Move a to b	84.0	42.0
Compare a to b	103.2	51.6
Multiplexor I/O Channel rate, bytes/second	85,000	85,000
Card reading speed, cpm —		
Basic reader	400	600
1001 Card Controller	1000/2000	1000/2000
Card punching speed, cpm	75-200	75-200 or 200
Alphanumeric printing speed, lpm	250	600
Magnetic tape speed, bytes/second	Not available	34,160

The overall architecture of the UNIVAC 9200 and 9300 Processors is closely similar to that of the IBM System/360 processors. Perhaps the most significant differences are in the general registers, which serve as accumulators, index registers, and base address registers. Whereas System/360 Models 30 through 75 each have one set of 16 general registers, the UNIVAC 9200 and 9300 have two groups of eight registers each. Furthermore, each register has a capacity of four bytes (32 bits) in the larger System/360 models and only two bytes (16 bits) in the 9200 and 9300.

One group of eight registers in the UNIVAC processors is used solely for internal processing functions, while the other group is reserved for input-output control functions. The processing group is used whenever the processor is operating in the normal mode, called Processor Program State Control (PPSC). Whenever an interrupt occurs, the processor switches automatically to the I/O Program State Control mode (I/OPSC) and uses the input-output group of registers. This system improves processing efficiency by eliminating the need to store and then reload the contents of the general registers whenever an interrupt occurs. Conversely, programming flexibility will be somewhat restricted by the fact that only 8 general registers, rather than 16, are accessible to the programmer.

Program interrupts occur upon completion of input-output operations and upon detection of input-output or processor errors. Standard software facilities interrogate a status byte to determine the cause of the interrupt and then initiate the appropriate program action.

The UNIVAC 9200/9300 instruction repertoire (see Table II) emphasizes decimal arithmetic operations upon variable-length fields. There are three basic instruction formats, which correspond to System/360 instruction types RX, SI, and SS. Type RX instructions are four bytes in length, specify one general register and one memory location, and are used primarily for binary arithmetic and branching operations. Type SI instructions are four bytes in length, specify one memory location and an 8-bit "immediate" operand value, and are used for logical and input-output operations. Type SS instructions are six bytes in length, specify two memory locations, and are used for the variable-length operations such as decimal arithmetic, code translation, packing, unpacking, and data movement. The two-byte register-to-register (type RR) instruction format used in the System/360 is not implemented in the UNIVAC 9200 and 9300.

Operands in plated-wire memory can be addressed either directly or by means of the base-plus-displacement technique used in the System/360. If there is a 0 in the most significant bit position of an instruction halfword containing a memory address, the remaining 15 bits of the halfword are interpreted as a direct address. If the most significant bit is a 1, the "base address"

(Contd.)

.05 CENTRAL PROCESSORS (Contd.)

contained in the general register specified by the next three bits is added to the "displacement" contained in the last 12 bits of the halfword to form the required memory address.

.06 CONSOLE

The operator's console for both the 9200 and 9300 systems consists of a sloping panel located to the right of the printer in the cabinet module that houses both the processor and printer. The top row of switches on the panel permits control of system power and of the functions of the basic printer, reader, and punch. A row of display lights indicates the nature of errors and abnormal conditions. Other switches and lights on the control panel are intended primarily for use in program testing and equipment maintenance. The contents of any address in memory can be displayed and altered, and programs can be executed in step-by-step fashion.

.07 INPUT/OUTPUT; PUNCHED CARD

.071 400-cpm Card Reader

This card reader is the basic input unit for the UNIVAC 9200 system. It reads standard 80-column cards photoelectrically, in column-by-column fashion, at a peak speed of 400 cards per minute. Optional features permit short cards of either 51 or 66 columns to be fed. The input hopper holds 1200 cards and the single output stacker holds 1500 cards. Checks are made for the following conditions: hopper empty, stacker full, misfeed, card jam, improper registration, photocell malfunction, and improper parity in data transmitted to the reader. Photocell malfunctions are detected by a light/dark check at the beginning of each card cycle. Control of card reader operations occupies the 9200 Processor for less than 1 percent of each 150-millisecond card cycle.

.072 600-cpm Card Reader

This card reader is the basic input unit for the UNIVAC 9300 system. Except for its higher peak speed of 600 cards per minute, its characteristics are similar to those of the 400-cpm reader described above. Control of card reader operations occupies the 9300 Processor for only 1 millisecond of each 100-millisecond card cycle.

.073 Column Card Punch

UNIVAC's new Column Card Punch is the basic card output device for both the UNIVAC 9200 and 9300 systems. It punches standard 80-column cards in column-by-column fashion. Cards are fed from a 1200-card input hopper past an optional pre-punch read station, a wait station, and a punch station, and then into one of two 850-card stackers. Program selection of either the normal output stacker or the reject stacker is an optional feature.

Rated punching speeds range from a maximum of 200 cards per minute when only the first 14 columns of each card are punched to a minimum of 75 cards per minute when all 80 columns are punched. In all cases, control of card punch operations occupies the central processor for a maximum of 1 millisecond per card. Checks are made for the following conditions: hopper empty, stacker full, chip box full, card jam, misfeed, improper punch motion (echo check), and improper parity.

.074 200-cpm Row Card Punch

The Row Punch can be connected to a UNIVAC 9300 system via the optional Multiplexor I/O Channel. Because it punches cards in row-by-row fashion, it can maintain its rated speed of 200 cards per minute regardless of the number of columns punched per card. Standard 80-column cards are fed from a 1000-card input hopper past an optional pre-punch read station, a wait station, a punch station, and a post-punch read station used for hole-count checking purposes, and then into one of two 1000-card stackers. Program selection of either stacker is a standard capability, and error cards are automatically directed into the error stacker. Control of Row Punch operations occupies the 9300 Processor for only 2 milliseconds of each 300-millisecond card cycle.

.075 1001 Card Controller

The 1001 Card Controller, announced in May 1965, is a high-speed alphanumeric collator that can be connected to a UNIVAC 9200 or 9300 system via the optional Multiplexor I/O Channel and a 1001 Control. The 1001 has two card feeds and seven stackers. Each of the two card feeds can operate independently at up to 1000 cards per minute, and a column-by-column photoelectric read station is associated with each card feed. Thus, a UNIVAC 9200 or 9300 equipped with a 1001 (in addition to the basic 400-cpm or 600-cpm card reader) can simultaneously handle three separate card input files and can perform merging and selection operations while processing.

The 1001 also contains 256 six-bit character positions of core memory and processing capabilities such as addition, subtraction, comparison, and editing. It is externally programmed by means of a plugboard. These facilities permit the 1001 to be disconnected from the computer system and used for off-line collating, editing, sorting, or proving operations.

.08 INPUT-OUTPUT; PRINTERS

.081 250-lpm Bar Printer

The 250-lpm printer is an integral part of the UNIVAC 9200 Processor and is the only printer currently offered for use in 9200 systems; its relatively low speed is likely to be the limiting factor on system throughput in many applications. The printer uses a horizontally oscillating type-bar — the first time UNIVAC has employed this printing technique. The advantages of this technique are its simplicity, low cost, elimination of vertical misalignment, and ability to use interchangeable type-bars.

The basic model has 96 print positions and a peak speed of 250 single-spaced or double-spaced lines per minute using the standard 63-character set. Vertical spacing is 6 lines per inch, and skipping speed is 25 inches per second. Control of printer operations occupies the 9200 Processor for about 31 milliseconds of each 240-millisecond print cycle.

Optional features permit the number of print positions to be expanded from 96 to either 120 or 132. Another option — Variable Speed Printing — provides a special type-bar that enables the printer, under program control, to print lines requiring only a 16-character numeric font at 500 lines per minute and lines requiring a 48-character alphanumeric font at 250 lines per minute.

.082 600-lpm Bar Printer

The 600-lpm printer is integrated into the 9300 Processor cabinet. It, too, uses a removable, horizontally oscillating type-bar, but its peak speed, using the standard 63-character set, is 600 single- or double-spaced lines per minute. The optional Numeric Print feature provides an interchangeable 16-character type-bar that permits lines containing only the 10 numeric digits plus 6 special symbols to be printed at the rate of 1200 lines per minute. Skipping speed is 25 inches per second, and the basic 120 print positions can be expanded to a maximum of 132. Control of printing operations occupies the 9300 Processor for 31 milliseconds per line when the standard 63-character set is used, and for only 8 milliseconds per line when the optional 16-character numeric type-bar is in use.

.09 INPUT-OUTPUT; MAGNETIC TAPE

.091 Uniservo VI C Magnetic Tape Handlers

The Uniservo VI C Magnetic Tape Handlers, which have been used with most of UNIVAC's second-generation computers, are the only tape units announced to date for the UNIVAC 9300 system. The standard models for use with the 9300 use 9-track tape with a recording density of 800 bytes per inch; thus, they are compatible with the 2400 Series magnetic tape units used with the IBM System/360. The tape speed of 42.7 inches per second provides a data transfer rate of 34,160 bytes per second, and tape can be read either forward or backward. Nominal start-stop times are 16.7 milliseconds when reading and 21.7 milliseconds when writing. Rewind time is 180 seconds or less per 2400-foot reel.

Tape reading and writing is overlapped with computing, and full read/write/compute simultaneity is possible in systems that include two tape control units. Control of magnetic tape operations occupies the 9300 Processor for approximately 10 microseconds per byte, or about 33% of the total data transfer time.

The basic Uniservo VI C Magnetic Tape Subsystem consists of one 9-track control unit, one master tape handler, and one slave tape handler. Each master tape handler can control up to three slave handlers, and one control unit can accommodate a maximum of eight tape handlers (two masters and six slaves). Each control unit occupies one of the eight positions on the 9300 Processor's optional Multiplexor I/O Channel. Two control units with a total of 16 handlers represent the maximum configuration that will be supported by the 9300 software.

The Uniservo VI C subsystem is also available in a 7-track version that provides compatibility with IBM 729 tape units and with many of the older Uniservo models. Recording densities of 200, 556, or 800 characters per inch result in data transfer rates of 8,540, 23,741, or 34,160 characters per second, respectively. The optional Data Conversion feature provides automatic two-way format conversions between the 6-bit characters on tape and the 8-bit bytes in memory. A 7-track tape subsystem consists of a 7-track control unit and up to eight 7-track tape handlers, arranged in the same way as the 9-track subsystem described above. Alternatively, 7-track slave handlers can be connected to a 9-track master handler and used in a 9-track subsystem if the optional 7-track feature is added.

.10 INPUT-OUTPUT; OTHER

No communications controllers, display devices, optical or magnetic character readers, or punched tape I/O devices have been officially announced to date for use with UNIVAC 9200 or 9300 systems, although UNIVAC plans to make an expanded line of peripheral equipment available in the future. The initial line of input-output devices is oriented exclusively toward the use of punched cards and magnetic tape.

(Contd.)

.11 SIMULTANEOUS OPERATIONS

Control circuits for the basic printer, card reader, and card punch are built into the 9200 and 9300 Processors; these three basic I/O devices, as well as devices connected via the optional Multiplexor Channel, can operate simultaneously with one another and with internal processing by interleaving their demands upon the plated-wire main memory. The Multiplexor Channel's maximum data rate, when operating in the multiplex mode, is 85,000 bytes per second — fast enough to permit read/write tape simultaneity in systems that include two Uniservo VI C control units.

The demands imposed upon the processor by the various input-output devices are stated in Paragraphs .071 through .091.

.12 INSTRUCTION LIST

The UNIVAC 9200 and 9300 have the same repertoire of 35 instructions, as listed in Table II; the only differences are that the Edit, Multiply, and Divide instructions are optional in the 9200 and standard in the 9300. Most of these 35 instructions are identical with IBM System/360 instructions in format and function; the principal exceptions are the privileged and input-output instructions, which differ from those used in the System/360.

The UNIVAC 9200/9300 instruction repertoire is similar to, though not identical with, that of IBM's small-scale System/360 Model 20, and is far smaller and less comprehensive than the instruction set used in System/360 Models 30 through 75. No facilities are provided for binary multiplication and division or for floating-point arithmetic, and there are fewer variations of the basic data-handling instructions to choose from than in the System/360. Nonetheless, the limited instruction set that UNIVAC has chosen to implement should be entirely adequate for small-scale business applications — and the smaller number of instructions should make programming easier to learn and less error-prone. The UNIVAC 9500 and the larger 9000 Series models will probably contain most or all of the System/360 programming facilities, although the privileged instructions in all models of the 9000 Series will differ from their System/360 counterparts (as do those in RCA's Spectra 70 series).

.13 COMPATIBILITY

Within the 9000 Series, UNIVAC promises hardware, software, and program compatibility. The programming languages for the 9200 and 9300 are compatible subsets of the languages for the larger models, so that source-language programs written for the smaller systems will be usable on upgraded systems without reprogramming.

UNIVAC plans to make its 9000 Series computers compatible with the IBM System/360 with respect to data structure, data codes, input-output media, and source-language programming. Direct program compatibility at the machine-language level will be precluded by the differences in privileged instructions (i.e., those instructions reserved for operating system use). Therefore, reassembly or recompilation will be necessary before programs written for a System/360 can be run on a 9000 Series system, but little or no reprogramming should be required. In all of these respects, UNIVAC's plans appear to parallel the methods RCA has used for achieving compatibility between its Spectra 70 Series and the System/360.

The restricted instruction repertoires of the small-scale UNIVAC 9200 and 9300, however, will make it impractical for these systems to reassemble and execute most assembly-language programs written for the System/360 processors other than the Model 20. Only the larger, yet-to-be-announced 9000 Series systems will be able to provide real assembly-language compatibility with the System/360; and, as in all such cases, an equivalent complement of peripheral devices and storage will be required.

No hardware or software facilities to enable 9000 Series systems to execute programs written for any of the older UNIVAC computers have been announced to date.

.14 DATA CODES

The basic internal code of the UNIVAC 9000 Series is the Extended Binary-Coded Decimal Interchange Code (EBCDIC), as used in the IBM System/360. It will also be possible to perform arithmetic and comparison operations upon ASCII data, although all standard software will be EBCDIC-oriented. Compatibility with the System/360 will also be maintained in punched card and magnetic tape codes. The 8-bit byte data structure, coupled with an efficient code translation instruction, should enable 9000 Series systems to accept and manipulate most present and future character codes of up to eight bits.

.15 SOFTWARE

.151 UNIVAC 9200 Software

The card-oriented UNIVAC 9200 system will be supported by the following software facilities:

- Assembler: Translates symbolic instructions into machine instructions on a one-to-one basis. The source deck is read twice, a printed listing is produced, and a relocatable object deck is punched.

TABLE II: UNIVAC 9200/9300 INSTRUCTION REPERTOIRE

CLASS	INSTRUCTION	OP CODE	MNEMONIC	FORMAT	9300 EXECUTION TIME, MICROSECONDS(1)
BINARY	Store Halfword	40	STH	RX	20.4
	Load Halfword	48	LH	RX	20.4
	Compare Halfword	49	CH	RX	20.4
	Add Immediate	A6	AI	SI	19.2
	Add Halfword	AA	AH	RX	20.4
	Subtract Halfword	AB	SH	RX	20.4
LOGICAL	Test Under Mask	91	TM	SI	16.8 to 19.2
	Move Immediate	92	MVI	SI	16.8
	AND	94	NI	SI	16.8
	Compare Immediate	95	CLI	SI	16.8
	OR	96	OI	SI	16.8
	Halt and Proceed	A9	HPR	SI	14.4
	Move Numerics	D1	MVN	SS	16.8 + 8.4(N)
	Move Characters	D2	MVC	SS	16.8 + 8.4(N)
	AND	D4	NC	SS	16.8 + 8.4(N)
	Compare Logical	D5	CLC	SS	25.2 + 8.4(N)
	OR	D6	OC	SS	16.8 + 8.4(N)
	Translate	DC	TR	SS	16.8 + 14.4(N)
	Edit	DE	ED	SS	See Note 3.
DECIMAL	Move with Offset	F1	MVO	SS	$25.2 + 3.6(N_2) + 6(N_1)$
	Pack	F2	PACK	SS	$25.2 + 3.6(N_2) + 4.8(N_1)$
	Unpack	F3	UNPK	SS	$21.6 + 7.2(N_2) + 4.8(N_1)$
	Zero and Add	F8	ZAP	SS	$26.4 + 3.6(N_2) + 4.8(N_1)$
	Compare Decimal	F9	CP	SS	$26.4 + 3.6(N_2) + 4.8(N_1)$
	Add Decimal	FA	AP	SS	$26.4 + 3.6(N_2) + 4.8(N_1)$
	Subtract Decimal	FB	SP	SS	$26.4 + 3.6(N_2) + 4.8(N_1)$
	Multiply Decimal	FC	MP	SS	See Note 3.
	Divide Decimal	FD	DP	SS	See Note 3.
BRANCH	Branch and Link	45	BAL	RX	18
	Branch on Condition	47	BC	RX	15.6 to 18
PRIVILEGED	Store State	A0	SPSC	SI	24
	Load State	A8	LPSC	SI	18 to 24
SPECIAL	Supervisor Call	A1	SRC	SI	12
I/O	Execute I/O	A4	XIOF	SI	18 to 22.8
	Test I/O	A5	TIO	SI	18 to 22.8

(1) To determine 9200 execution times, multiply the indicated times by 2. Timing for all instructions assumes no indexing; add 3.6 microseconds for each indexing operation.

(2) N, N_1, N_2 = the number of bytes specified in the respective length fields (L + 1, L_1 + 1, or L_2 + 1).

(3) Times for the ED, MP, and DP instructions have not been specified to date; these three instructions are extra-cost options in the UNIVAC 9200 and standard equipment in the 9300.

.151 UNIVAC 9200 Series (Contd.)

- Preassembly Macro Pass: Causes generalized macro routines from a punched-card macro library to be particularized in accordance with parameters specified by the programmer in a deck of macro instructions. The particularized routines are then punched in source code for subsequent assembly.
- Report Program Generator: Accepts problem-oriented specifications defining a required report, and generates a program to produce the report. The UNIVAC RPG uses essentially the same coding forms and specifications as the IBM System/360 RPG; its principal purpose is to ease the transition from punched card tabulating to stored-program computing.
- Gangpunch Reproducer: Permits gangpunching and reproducing functions to be described in problem-oriented terms, and generates a program to perform the specified functions.

(Contd.)

.151 UNIVAC 9200 Series (Contd.)

- Subroutines: A group of standard routines to perform functions such as control of input-output operations, loading of programs, linking of separately-assembled program elements, simulation of the hardware multiply/divide and edit instructions, dumping of specified memory areas, floating-point arithmetic, and evaluation of the common mathematical functions (Mathpac).

.152 UNIVAC 9300 Software

Card-oriented UNIVAC 9300 systems will be able to utilize all of the 9200 software facilities described above.

For tape-oriented 9300 systems, the following facilities will be provided in addition to the card-oriented software:

- Tape Assembler: Functionally similar to the card Assembler, but contains a built-in macro facility and uses magnetic tape to minimize card handling; requires at least four tape units and 16,384 bytes of memory.
- Tape Report Program Generator: Functionally similar to the card RPG, but permits magnetic tape input to the object program; requires four tape units and 16,384 bytes of memory.
- Tape Input/Output Control System: Performs the housekeeping operations involved in handling magnetic tape files, so that the programmer only needs to concern himself with the processing of logical records. Tape IOCS operations are initiated by macro instructions. At least two tape units and 8,192 bytes of memory are required.
- Sort/Merge: Sorts and/or merges tape records of either fixed or variable length. Upper limits on record size, number of sort key fields, and total key size depend upon memory capacity. At least three tape units and 8,192 bytes of memory are required.
- FORTRAN IV: Converts source programs written in the A.S.A. FORTRAN IV language (with certain yet-to-be-defined extensions) into machine-language object programs. At least four tape units and 16,384 bytes of memory are required for FORTRAN compilation.
- COBOL: Translates COBOL source programs into machine-language object programs. UNIVAC states that the 9300 COBOL language is based on D.O.D. COBOL 1965 and conforms with the proposed A.S.A. COBOL language modules. The exact language facilities to be provided have not been defined to date. Six tape units and 32,768 bytes of memory are required for COBOL compilation.
- Executive: Facilitates efficient system operation by coordinating operator-computer communication, allocating memory space and peripheral devices to programs, locating programs and overlays stored on magnetic tape, handling input-output interrupts, and providing restart capabilities.

"Control stream operation" is UNIVAC's term for stacked-job processing in which one program at a time is loaded and executed in accordance with control cards entered by way of the card reader. "Concurrency" is a limited form of multiprogramming that can be employed in UNIVAC 9300 systems with sufficient memory capacity and magnetic tape units; in this mode of operation, one or more data transcription functions (card to tape, tape to printer, etc.) are performed concurrently with the execution of one main program. Control stream operation will require a 16K, 4-tape configuration, while 32K and at least 5 tape units will be required for concurrency.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	Monthly Rental 1-year lease	Monthly Rental 5-year lease	Monthly Maintenance $	Purchase $
9200 CENTRAL SYSTEM	3030-00	9200 Processor (includes 250-lpm printer with 96 print positions)	330	295	65	12,200
	F0882-00	Multiply, Divide, Edit Instructions	75	65	5	3,220
	F0869-00	Multiplexer I/O Channel	50	45	5	2,070
	F0822-00	1001 Control	40	35	5	1,610
	F0866-00	120 Print Positions	120	105	15	4,830
	F0868-01	132 Print Positions	180	160	20	7,360
	F0865-00	Variable Speed Printing	75	70	15	2,760
		Plated-Wire Memory:				
	7007-00	8,192 Bytes	375	330	30	15,870
	7007-10	12,288 Bytes	625	550	45	26,680
	7007-12	16,384 Bytes	750	660	60	31,740
9200 I/O DEVICES	0711-00	Card Reader (400 cpm)	135	120	30	4,830
	F0872-00	Short Card Feature (51-column)	40	35	10	1,380
	F0872-01	Short Card Feature (66-column)	40	35	10	1,380
	0603-04	Card Punch (75-200 cpm)	200	180	60	6,440
	F0870-00	Read/Punch Feature	75	65	15	2,760
	F0871-00	Selective Stacker Feature	10	8	—	415
	1001	Card Controller (basic model)	475	425	150	16,250
	—	1004 Interface (required on 1001 for connection to a 9200 system)	11	9	3	400
9300 CENTRAL SYSTEM	3030-02	9300 Processor (includes 600-lpm printer with 120 print positions)	725	650	150	26,500
	F0869-01	Multiplexer I/O Channel	75	65	5	3,220
	F0864-00	132 Print Positions	75	70	10	2,990
	F0867-00	High-Speed Numeric Print Feature	50	45	15	1,610
	F0822-99	1001 Control	50	45	5	2,070
		Plated-Wire Memory:				
	7007-99	8,192 Bytes	550	485	45	23,230
	7007-98	12,288 Bytes	850	750	60	36,340
	7007-97	16,384 Bytes	1,000	880	75	42,550
	7007-14	32,768 Bytes	1,800	1,580	120	77,280
9300 I/O DEVICES	0711-02	Card Reader (600 cpm)	200	180	60	6,440
	F0872-02	Short Card Feature (51-column)	40	35	10	1,380
	F0872-03	Short Card Feature (66-column)	40	35	10	1,380
	0603-04	Card Punch (75-200 cpm)	200	180	60	6,440
	F0870-00	Read/Punch Feature	75	65	15	2,760
	F0871-00	Selective Stacker Feature	10	8	—	415
	0604-00	Row Card Punch (200 cpm)	310	280	90	10,120
	F0875-00	Read/Punch Feature	150	135	45	4,830

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	Monthly Rental 1-year lease	Monthly Rental 5-year lease	Monthly Maintenance $	Purchase $
9300 I/O DEVICES (Contd.)	1001	Card Controller (basic model)	475	425	150	16,250
	—	1004 Interface (required on 1001 for connection to a 9300 system)	11	9	3	400
	0858-99	Uniservo VI C Magnetic Tape Subsystem (9-track; includes control, master handler, and 1 slave handler)	875	785	195	31,280
	F0828-00	7-Track Feature (permits 7-track handlers to be added to a 9-track subsystem)	50	45	5	2,070
	F0827-00	Data Conversion Feature	50	45	5	2,070
	0858-14	Uniservo VI C Slave Handler (9-track)	300	270	70	10,680
	0858-10	Uniservo VI C Master Handler (9-track)	500	450	115	17,700
	0858-98	Uniservo VI C Magnetic Tape Subsystem (7-track; includes control, master handler, and 1 slave handler)	875	785	195	31,280
	F0827-00	Data Conversion Feature	50	45	5	2,070
	0858-01	Uniservo VI C Slave Handler (7-track)	300	270	70	10,680
	0858-00	Uniservo VI C Master Handler (7-track)	500	450	115	17,700