MCP BASED DMA SERIAL CARD ("Livonia") REV 1.4.2 (PVT PHASE)

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1.1.2 System Overview

The "Livonia" board is a card with a full NuBus Master/Slave interface with a 68000 processor , 1/2 Mbyte of RAM (expandable to 2.5Mb), two SCC's and one Mc68450 DMA chip (4 channels) on board. It is based on Gary Martens' **MCP** Nubus interface card.
The card provides four active ports, two of which can be run at speeds greater than 19.2kbit/s. These two high speed serial ports may be configured as V.35 ports for driving 56kb/s leased line DDS (modem-like) devices, or as RS-232 ports. The configuration choice is made by the type of connecting cable used.

The 68000 can access any device on the NuBus. The DMA, EPROM, SCC's, local RAM and DTR/DSR registers and all may be accessed via Nubus. *Accesses by the DMA to the Nubus are NOT supported.*

2.1 Processor

The I/O Processor utilizes a 10MHz 68000 processor with no wait states for accesses to onboard RAM. The 10MHz clock is derived from the 10MHz NuBus clock. All access by the 68000 are implemented by a 16-bit data bus with byte mode also supported. Accesses to the SCCs are done on a byte wide basis on D0-7 (odd addresses). Accesses to the DMA may be either byte or word mode.

2.2 ROM

The 16-bit wide ROM is implemented with two 256K bit ROMS yielding a 64K byte ROM space. The ROM serves as "power-up" code for the 68000, a place for user firmware, and it also stores the NuBus ID data for the card. The ROM inserts one wait state when accessed by the onboard 68000.

To the NuBus interface, ROM appears as a full 32-bit wide device, supporting 8-bit, 16-bit and 32-bit bus reads.

2.3 RAM

The card contains 1/2 Mbyte of 16-bit wide dynamic RAM, with sockets available for a second 1/2 Mbyte (all ZIP chips). RAM is accessed by the 68000, NuBus, and the two DMA Chips (MC68450). When any device on the card is accessed via NuBus, the 68000 is locked out from all accesses. RAM starts at location 000000, with the default 1/2 Mbyte of RAM, the last RAM address is 07FFFF. When the 68000 accesses onboard RAM, no wait states are inserted. When the 68450 DMA chip accesses RAM, one wait state is inserted on write cycles, zero wait states inserted on read cycles (this is an anomaly in the DMA chip itself).

Provision is made for future 4 Mbit DRAM ZIP chips (Qty. 4) which, when combined with the 1/2 Mbyte already present would give total of 2.5 Mbyte of RAM on the card. Pin 10 of the 1Mb chip is a no connect which will be used as A9 on the 4Mb parts

To the NuBus interface, RAM appears as a full 32-bit wide device, supporting 8-bit, 16-bit and 32-bit bus operations.

2.4 NuBus Interface

The NuBus interface allows for either master or slave operation. In master mode the 68000 makes an access to the NuBus address space, and uses the NuBus ACK signal to generate DTACK and complete the cycle. Since the 68000 does not have 32 bits of address to drive the NuBus, the upper 12 address bits are generated by a "page latch", which is written with these bits by the processor prior to a Nubus cycle. In slave mode, the 68000 and DMA are tri-stated on the internal bus while the NuBus access is taking place.

Since the 68000 has an internal 16-bit bus, all bus cycles originating from the 68000 can be either 8-bit or 16-bit operations. This includes NuBus operations where the 68000 is the NuBus master, in which both 8-bit and 16-bit operations are supported.

Special hardware has been included so that 32-bit accesses coming in from NuBus will function correctly. The hardware performs two 16-bit bus operations on the 68000 bus whenever NuBus requests a 32-bit operation. As a result, the card supports 8-bit, 16-bit and 32-bit NuBus transfers. Since two bus 68000 bus cycles are required for a 32-bit NuBus operation, using a 32-bit operation when only 16-bits are required should be avoided due to the increased amount of time required for the extra 68000 bus cycle.

If the NuBus access cannot be completed, a bus error to the 68000 and DMA components are reported.

2.5 SCC Interface

Two serial communications chips (Zilog 8530 SCC) are included on the card to provide four serial ports. The SCC PCLK is supplied by a 7.3728 Mhz crystal oscillator. Receive and transmit clocks are inputs only.

Vectored interrupts from the SCC are supported in this implementation. During SCC setup, a base vector value is written to the device. After the SCC activates the interrupt line, a vector will be placed on D0-D7 corresponding to the base vector offset by the condition code of the interrupt. Possible interrupt condition codes are:

CH B Tx buffer empty
CH B External/Status Change
CH B Rx Character Available
CH B Special Rx Condition
CH A Tx buffer empty
CH A External/Status Change
CH A Rx Character Available
CH A Special Rx condition

Please see the Zilog/AMD SCC manual for further information on the SCC.

2.6 DMA Interface

The 68450 DMA chip uses a multiplexed address and data bus, with four bus transceivers connecting to the separate local buses. Addresses A0-A7 are not multiplexed, and are used to select the internal registers in the DMA component. Please see the Motorola MC68450 manual for more information on the DMA chip.

3.0 Hardware Description Details

3.1 Address Map

All operations to the card's address space, regardless of where they orginate (either from NuBus or the 68000) map into the same 24-bit address range. This 16 Mbyte space is defined as follow:

Address	Function
FF0000-FFFFFF	Read - ROM (with 2 - 256Kbit ROMs)
F00000	Write - Place 68000 in RESET
E00000-EFFFFF	Test ROM (off card)
C0000A	Read - Set Interrupt Livonia request
C00008	Read - Clear Interrupt Livonia request
C00006	Read - Set Interrupt Host request
C00004	Read - Clear Interrupt Host request
C00002	Read - Clear Timer Interrupt
C00000	Read - Clear RESET, Read Serial Status Register
C00000	Write - NuBus Extension Register
A00000-BFFFFF	NuBus
900002	DTR/LED Write only Register
900000	DSR Read only Register
600000	DMA Chip Base
500007	SCC #1 "A" Channel Data Register
500005	SCC #1 "A" Channel Command Register
500003	SCC #1 "B" Channel Data Register
500001	SCC #1 "B" Channel Command Register
400007	SCC #2 "A" Channel Data Register
400005	SCC #2 "A" Channel Command Register
400003	SCC #2 "B" Channel Data Register
400001	SCC #2 "B" Channel Command Register
100000-3FFFFF	Future RAM
07FFFF-100000	Expandable 1/2 MB RAM
000000-07FFFF	RAM (with 1/2 MB RAM)

3.2 NuBus Address Space

Access to the 32-bit NuBus address space is provided by a 12-bit addresses extension register. The most significant 12 bits of the NuBus address should be placed in this register before accessing the NuBus address space. This write-only register is located at location C00000.
In addition, A20 in the address field (not used for address calculation) is used by the hardware to perform a read-modify-write cycle. Whenever a Test-and-Set instruction is executed, A20 must be set true. A20 should be set false for all other operations.

3.3 Timer

An internal 6.5536ms timer is provided. Every 6.5536ms a level 1 interrupt occurs. This interrupt is cleared by reading location C00002. Note that if this interrupt is ignored for 6ms or more, the next interrupt may not be seen and a clock tick will be lost.

3.4 Reset

The Livonia card can be placed in latched reset by writing location F00000 (any write to FXXXXX will place the 68000 in RESET) and placed out of reset by reading C00000 (any access to CXXXXX will take the 68000 out of RESET). This latched feature is useful for software downloads to the card, where the card can be reset, downloaded to, and then brought out of reset.

The NuBus reset going active also resets the card, but does not latch the card in the reset state.

On power-on reset (NuBus reset) the first four accesses, i.e., the stack pointer and the program counter, are fetched from the first four ROM locations. Under "warm" RESET, the address and stack pointer are fetched from RAM, starting at location 000000.

Note that the start-up address vector in location 4 and 6 of the ROM must point to ROM address space (FF0000-FFFFFF) .

3.5 Interrupts

Three interrupts are provided in the basic design, one for the timer, one for the NuBus interface, and one for the I/O interface. The priorities are as follows:

Interrupt	Level
Timer	1
NuBus	2
DMA	3
not used	4
SCC #1	5
SCC #2	6

The I/O interface interrupt must remain asserted until the software resets this interrupt request.

The card can interrupt the host by reading location C00006, this interrupt is cleared by the host reading location C00004. This interrupt is generated at level 2.

The card is interrupted by the host reading location C0000A, this interrupt is cleared by the 68000 reading location C00008.

3.6 Accessing the SCCs

The SCCs appear at 68000 addresses 40000X (SCC #2) and 50000X (SCC #1), where X can be one of four values (1,3,5,7). Address bit 1 controls the Data/Command line and Address bit 2 controls the A/B channel line. The SCC decodes are listed in the memory map in section 3.1:

3.7 Serial I/O Signals

The four serial I/O channels are divided up into two high speed channels (DMA backed), channels A and B of SCC #1, which can drive full duplex 56kb/s leased lines, and two low speed channels, channels A and B of SCC #2, (fed by the 68000), each of which can drive up to 19.2kb/s full duplex.

Note: Actual speed performance of th Livonia card is highly dependent on the efficiency of the software run on it. Tests have been run which prove that the card can run individual lines at 19.2kb/s, not concurrently, without using the DMA. With DMA, tests have been run which indicate the card can do one 56Kb/s channel, and one 9.6kb/s channel concurrently. It is quite likely that the card can go much faster than these speeds, and this document will be updated as these tests are carried out.

Hereafter the channels will be referred to using the following nomenclature:
Channel A1 : DMA backed, high speed > 56Kb/s
Channel B1 : DMA backed, high speed > 56Kb/s
Channel A2 : 68K controlled, up to 19.2kb/s
Channel B2: 68K controlled, up to 19.2kb/s

3.8 Serial Status Register

The Serial Status Register is an 8-bit read only register that contains the RI and DSR inputs for the serial channels. This data is placed on data bit 8 -15 of the data bus whenever the status register is read (address 900000). The format of the register is as follows:

RIB2	D8
RIB1	D9
RIA2	D10
RIA1	D11
DSRB1	D12
DSRB2	D13
DSRA1	D14
DSRA2	D15

3.8.1 DTR Register

Because the DTR/*REQ pin on the SCC #1 is used for DMA request, the DTR signal to the modem interface is generated by a write only register and each bit is written individually based on the state of A4-A6. Once written, the four DTR lines are latched until the next write. In addition, 3 test bits are available in this register, two of which, TSTB1 an TSTB3, are used for green and red LED's, respectively.

DTR Address Map : (DTR_BASE = $900002)

DTR_BASE + 010H = DTRA1	Data bit 8 flows thru & latches
DTR_BASE + 020H = DTRA2	
DTR_BASE + 030H = DTRB1	
DTR_BASE + 040H = DTRB2	
DTR_BASE + 060H = TSTB1	Green LED
DTR_BASE + 070H = TSTB2	Non-latching
DTR_BASE + 000H = TSTB3	Red LED

3.9 Configuration

Channels 1A and 1B are the high speed channels. Channels 2A and 2B are the low speed channels, which are hardwired to meet RS-232. The two high-speed channels may be configured for the various interfaces by changing **custom** R-packs RPA15 and RPA16, which are socketed for this purpose.

Interface	RPA15	RPA16
RS-232	Removed	Removed
V.35	120 ohm	300ohm

3.10 D-62 Connector

Note: Signals in this section with prefix 232 or 422 are used here and on the schematic for notational purposes only, 232 denoting a single ended signal and 422 a differential . For example, the signals +/-422TXDA1 are attenuated and used to drive the V.35 transmit signals.

Signal	Pin #	Function
+CA1F	1	Control, +CHA1, OUTPUT
-CA1F	3	Control, -CHA1, OUTPUT
+CB1F	6	Control, +CHB1, OUTPUT
-CB1F	8	Control, -CHB1, OUTPUT
+IA1	16	INDICATION, +CHA1, INPUT
1DCDA/-IA1	44	Data Carrier Detect/ INDICATION -CHA1, INPUT
+IB1	11	INDICATION, +CHB1, INPUT
1**DCDB/-IB1**	49	Data Carrier Detect /INDICATION -CHB1, INPUT
GND_1	62	CHA1 GND
GND_2	57	CHB1 GND
GND_3	52	CHA2 GND
GND_4	47	CHB2 GND
GND_5	41	EXTRA GND
GND_6	37	EXTRA GND
232TXDA1	2	TX DATA, CHA1, SINGLE-ENDED, OUTPUT
232TXDB1	7	TX DATA, CHB1, SINGLE-ENDED, OUTPUT,
232TXDA2	12	TX DATA, CHA2, SINGLE-ENDED, OUTPUT
232TXDB2	17	TX DATA, CHB2, SINGLE-ENDED, OUTPUT
1RTSA	4	READY TO SEND, CHA1, SINGLE-ENDED, OUTPUT
1RTSB	9	READY TO SEND, CHB1, SINGLE-ENDED, OUTPUT
2RTSA	14	READY TO SEND, CHA2, SINGLE-ENDED, OUTPUT
2RTSB	19	READY TO SEND, CHB2, SINGLE-ENDED, OUTPUT
1CTSA	5	CLEAR TO SEND, CHA1, SINGLE-ENDED, INPUT

1CTSB	10	CLEAR TO SEND, CHB1, SINGLE-ENDED, INPUT
2CTSA	15	CLEAR TO SEND, CHA2, SINGLE-ENDED, INPUT
2CTSB	20	CLEAR TO SEND, CHB2, SINGLE-ENDED, INPUT
1DSRA	43	DATA SET READY, CHA1, SINGLE-ENDED, INPUT
1DSRB	48	DATA SET READY, CHB1, SINGLE-ENDED, INPUT
2DSRA	53	DATA SET READY, CHA2, SINGLE-ENDED, INPUT
2DSRB	58	DATA SET READY, CHB2, SINGLE-ENDED, INPUT
1DTRA	45	DATA TERMINAL READY, CHA1, SINGLE-ENDED, OUTPUT
1DTRB	50	DATA TERMINAL READY, CHB1, SINGLE-ENDED, OUTPUT
2DTRA	55	DATA TERMINAL READY, CHA2, SINGLE-ENDED, OUTPUT
2DTRB	60	DATA TERMINAL READY, CHB2, SINGLE-ENDED, OUTPUT
1RIA	46	RING INDICATOR, CHA1, SINGLE-ENDED, INPUT
1RIB	51	RING INDICATOR, CHB1, SINGLE-ENDED, INPUT
2RIA	56	RING INDICATOR, CHA2, SINGLE-ENDED, INPUT
2RIB	61	RING INDICATOR, CHB2, SINGLE-ENDED, INPUT
2DCDA	54	DATA CARRIER DETECT, CHA2, SINGLE-ENDED, INPUT
2DCDB	59	DATA CARRIER DETECT, CHB2, SINGLE-ENDED, INPUT
2RXCA	39	RECEIVE CLOCK, CHA2, SINGLE-ENDED, INPUT
2RXCB	40	RECEIVE CLOCK, CHB2, SINGLE-ENDED, INPUT

2TXCA	38	TRANSMIT CLOCK, CHA2, SINGLE-ENDED, INPUT
2TXCB	42	TRANSMIT CLOCK, CHB2, SINGLE-ENDED, INPUT
2RXDA	13	RECIEVE DATA, CHA2, SINGLE-ENDED, INPUT
2RXDB	18	RECEIVE DATA, CHB2, SINGLE-ENDED, INPUT
+422TXCA1	21	+ TRANSMIT CLOCK, CHA1, DIFFERENTIAL, INPUT
-422TXCA1	22	- TRANSMIT CLOCK, CHA1, DIFFERENTIAL, INPUT
+422TXCB1	29	+ TRANSMIT CLOCK, CHB1, DIFFERENTIAL, INPUT
-422TXCB1	30	- TRANSMIT CLOCK, CHB1, DIFFERENTIAL, INPUT
+422RXCA1	25	+ RECEIVE CLOCK, CHA1, DIFFERENTIAL, INPUT
-422RXCA1	26	- RECEIVE CLOCK, CHA1, DIFFERENTIAL, INPUT
+422RXCB1	33	+ RECEIVE CLOCK, CHB1, DIFFERENTIAL, INPUT
-422RXCB1	34	- RECEIVE CLOCK, CHB1, DIFFERENTIAL, INPUT
+422TXDA1	27	+ TRANSMIT DATA, CHA1, DIFFERENTIAL, OUTPUT
-422TXDA1	28	- TRANSMIT DATA, CHA1, DIFFERENTIAL, OUTPUT
+422TXDB1	35	+ TRANSMIT DATA, CHB1, DIFFERENTIAL, OUTPUT
-422TXDB1	36	- TRANSMIT DATA, CHB1, DIFFERENTIAL, OUTPUT
+422RXDA1	23	+ RECEIVE DATA, CHA1, DIFFERENTIAL, INPUT
-422RXDA1	24	- RECEIVE DATA, CHA1, DIFFERENTIAL, INPUT
+422RXDB1	31	+ RECEIVE DATA, CHB1, DIFFERENTIAL, INPUT
-422RXDB1	32	- RECEIVE DATA, CHB1, DIFFERENTIAL, INPUT

4.0 MC68450 DMA Component

The card contains one MC68450 DMA component, optimized for the 68000 bus. It provides 4 DMA channels for 2 simultatneous full duplex communications processes. The DMA channels may also be used for block memory transfers as follows:

*SCC to On-card memory and vice-versa
*On-Card to On-Card Block Memory Moves

The 68450 supports command chaining, which should prove useful in programming Datacomm protocols where pre-formed control packets such as "code violation" and "RTS" can be formed in memory and then DMA'ed out in succession without processor intervention.

4.1 DMA Interface to MCP Local Bus

The DMA component is capable of becoming a local bus master, that is, it can perform cycles out to local DRAM on the card. The DMA chip is capable of addressing the full 16 Mbyte memory space that the 68000 sees, with the exception of the NuBus space at A00000-BFFFFF. The DMA contends for control of the local RAM with the 68000 and the NuBus. Access is in a fixed priority

scheme with a bus request from either the NuBus or the DMA chips causing the 68000 to tri-state until the access by the others is finished. Note that the DMA component has priority over the NuBus, and both have priority over the 68000. *Care must be taken in programming the DMA chip to insure that it does not grab the bus for more than 25.6uSec, the NuBus timeout value.* It is recommended that the DMA chip be used in "Cycle Steal" mode, which will ensure re-arbitration. The four channels within each DMA may be programmed as fixed prioritized or in "round robin" service order.

Interrupts are handled by an interrupt acknowlege cycle, with the interrupt request line from the DMA chips tied in to a fixed priority encoder (see section 3.5).

When the DMA is operated in the polled mode (as opposed to interrupt driven), a delay of 6.7 uS (18 68020 DBRA's) must be inserted in software from the time the DMA "start" command is issued to the first poll of any internal register of the DMA chip. Note that this is longer than what Motorola advises in their errata sheet, which is 700ns. It is recommended that the DMA be used in interrupt, rather than polled mode.

4.2 Access to DMA Registers by 68000

The 68000 accesses DMA chips registers as shown in Fig. 3-1. The "base" described in the DMA chip register map is 600000 HEX.

4.3 MC68450 DMA to 8530 SCC Interface

The DMA to 8530 interface assumes the 8530 is programmed to use DTR/*REQ programmed as a transmit request line, and W/*REQ as the receive request line. The 8530 does not have a DMA acknowledge line. To the 8530 and the DTACK generation logic, a DMA access to the 8530 looks like a 68000 access.

Note that the state of the 8530 transmit buffer is reflected directly on the DTR/*REQ line *whether the transmitter is enabled or not.* This means that the transmitter must be enabled *before* the DMA channel associated with it. *It is important that when starting the DMA and SCC that the current DMA operation be aborted first, then set up the SCC, then start the DMA. Similarly, when stopping operations, abort the DMA operation first, then stop the SCC.*

The DMA to SCC interface is setup as follows:

DMA REQ0	to	RXA1_REQ
DMA REQ1	to	TXA1_REQ
DMA REQ2	to	RXB1_REQ
DMA REQ3	to	TXB1_REQ

5.0 Cabling

Two types of cables are available with the Livonia card, one is the "Hydra" cable, which offers four RS-232 connectors (DB-25) for ports 1A, 1B, 2A, 2B. Termination resistors are included in the heads 1A and 1B to meet the specification for RS-232 input impedance.

The second cable type available is a two-headed V.35 cable which has a V.35 connector on port 1A and an RS-232 (DB-25) connector on port 2B.

6.0 Performance

The Livonia board shall be capable of running one 56 Kb/s full duplex connection out of either port 1a or 1b, while at the same time operating one full duplex connection at 9600 Kb/s out of either port 2a or 2b.

7.2 **Mechanical Packaging**

The card has a standard NuBus form factor.

Each connector shall be capable of being cycled more than 100 times.

The card is not intended to be shipped in a CPU slot. It should be packaged separately.

7.3 **Environmental Specifications**

7.3.1 **Temperature**

The operating temperature shall be from +10 to +40 degrees C.
(Note that the Macintosh II can only operate to 35 degrees C).

The storage temperature range shall be from -40 to +65 degrees C.

The transit temperature range shall be from -40 to +65 degrees C.

7.3.2 **Humidity**

The operating humidity shall be from 20% - 95% non-condensing at a temperature range from +25 to +40 degrees c.

The storage humidity range is not specified.

7.3.3 **Vibration**

7.3.3.1 **Operational**

Vibration requirements while operating are not specified.

7.3.3.2 **Non-Operational**

A non-operating board shall be able to withstand the following vibration tests:

7.3.3.3 **Resonance Search**

Search of critical components within a frequency range of 3-200-3 Hz at a sinusoidal acceleration of 0.5 Gs, with a sweep rate of 1 decade/minute.

7.3.3.4 **Resonance Dwell**

Endurance tested for a total of 15 minutes per resonance frequency at a sinusoidal input of 0.5 Gs acceleration.

7.3.3.5 **Random Vibration**

Each shipping axis shall pass an endurance test for both the "truck bed" and "jet airplane" random vibration spectrum for 15 minutes each.

7.3.4 **Shock**

7.3.4.1 **Operational**

Shock requirements while operating are not specified.

7.3.4.2 **Non-Operational**

A non-operating board shall be able to withstand the following shock tests:

Bench Test

Each of the four edges shall be lifted to a height of four inches or a position 45 degrees to the horizontal, which ever is lower, and the lifted edge allowed to freely fall onto the horizontal surface. Each edge shall be tested twice.

Free Fall Drop Test

The test unit shall survive a simulated free fall drop test of a flat four inch impact on a programmable shock test system. The shock test system shall be set for a programmed shock input with a velocity change of 56 inches/second (4 inch free fall).

7.3.5 **Altitude**

The operating altitude shall be 0 to 2135 meters.

The transit altitude shall be 0 to 13000 meters.

7.3.6 **Electrostatic Discharge**

The LIVONIA card will adhere to the Apple specification drawing number 062-0302-A for hardening equipment against electrostatic discharge.

The card, when installed in a system, shall meet the following requirements:

0 kV to 7.5 kV	No errors allowed
7.5 kV to 10 kV	No more than three soft errors
10 kV to 15 kV	No catastrophic failures

A soft error is defined as a momentary interruption of normal operation, with no perceptible loss of data.

A catastrophic failure is defined as a termination of normal operations which requires repair.

7.3.7 **Mean Time Between Failure**

The card shall have a MTBF of greater than 100K power on hours.

7.4 **FCC/UL Specifications**

The unit will adhere to all the Apple specifications with regards to the limits for all radiated and conducted interference levels for class
B operation.

The unit will conform to the UL/CSA electrical specifications for safety and operation (ref. Apple drawing no. 062-0093-C).

7.5 **International Requirements: West German FTZ/VDE Requirements**

All radiated and conducted emissions from the LIVONIA unit must meet the levels specified by the West German FTZ(FCC equivalent) rules and regulations equivalent to FCC class B.

The unit will conform to the West German VDE, UL equivalent specifications for safety and operation (ref Apple drawing no. IEC 380/ VDE 0806 Equivalent).

The unit will adhere to the Apple specification for hardening equipment against electrostatic discharge (refer Apple drawing. no. 062-0302-A).

Note that these may be replaced by the new NETS standards. NETS is a new European standards body that is replacing the individual countries standards organizations.