AMCOMP

8011 Disc Memory Controller
OPERATION & MAINTENANCE MANUAL

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8011 Disc Memory Controller

OPERATION & MAINTENANCE MANUAL

AMCOMP

686 WEST MAUDE AVENUE
SUNNYVALE, CALIFORNIA 94086

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LIST OF EFFECTIVE PAGES

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PREFACE

This manual describes the AMCOMP 8011 Disc Memory Controller. The controller is used with the Data General Corporation Nova Series Computers to write data into or read data out of the AMCOMP models 8400 or 8500 Disc Memory Units.

This manual is divided into six chapters as follows:

Chapter 1 - General Information
Chapter 2 - Installation and Checkout
Chapter 3 - Operation and Interface
Chapter 4 - Theory of Operation
Chapter 5 - Maintenance
Chapter 6 - Drawings and Parts Lists

The publications listed below provide additional information. Copies of publications prepared by AMCOMP, INC. may be obtained from AMCOMP facility at 686 West Maude Avenue, Sunnyvale, California 94086.

Title	Publication Number
8400 Series Disc Memory Unit Operation and Maintenance Manual (AMCOMP, INC.)	1580009-00
8500 Series Disc Memory Unit Operation and Maintenance Manual (AMCOMP, INC.)	1580006-00
How To Use The Nova Computers System Reference Manual (Data General Corporation)	DG NM-5

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Chapter 1

GENERAL INFORMATION

GENERAL INFORMATION

1-1 INTRODUCTION

This chapter contains general information pertaining to the AMCOMP 8011 Disc Memory Controller (figure 1-1). The information in this chapter consists of a general description, a physical description and a functional description. Specifications and characteristics for the controller are listed in table 1-1 of this chapter.

1-2 GENERAL DESCRIPTION

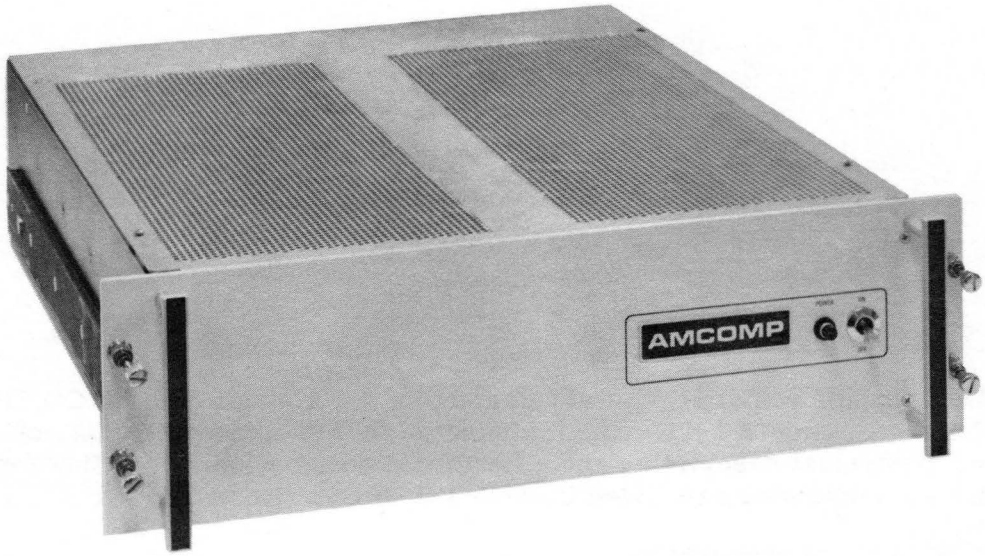
The 8011 Controller consists of a formatter assembly, an adapter board, interconnecting cables, and a diagnostic program. The formatter assembly consists of a single printed circuit (PC) board, a slide mountable chassis, and a DC power supply. The controller operates with Data General Corporation Nova Series Computers in writing data to or reading data from the disc memory units. The adapter PC board deals with Nova Computer interface functions, and the formatter PC board with AMCOMP disc memory control functions.

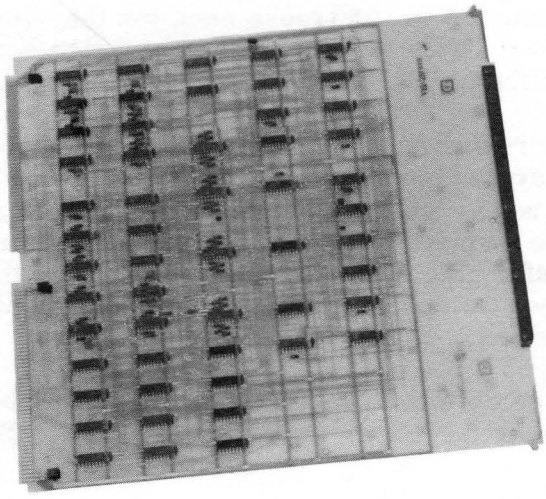
The controller can interface up to four (daisy-chain configuration) 8430 or 8530 Disc Memory Units. These disc units range from 16 to 128 tracks each for the 8400, and from 16 to 256 tracks each maximum for the 8530. The track selection and size configuration is accomplished through the power connection of "E" pins in the formatter PC board.

Each track on a disc contains 32 sectors and each sector contains 16 subsectors. Each subsector stores 16 words plus a 16-bit cyclic code word and parity bit. The 16 subsectors that comprise one sector may or may not be adjacent to each other on a track, depending upon the interlace factor wired into the formatter PC board. The subsector interlacing is used to change the average data transfer rate of the system and allowing the disc to be matched with the speed of the various Nova Computers. The formatter PC board can be wired for 1:1, 2:1, 4:1, or 8:1 interlace factors.

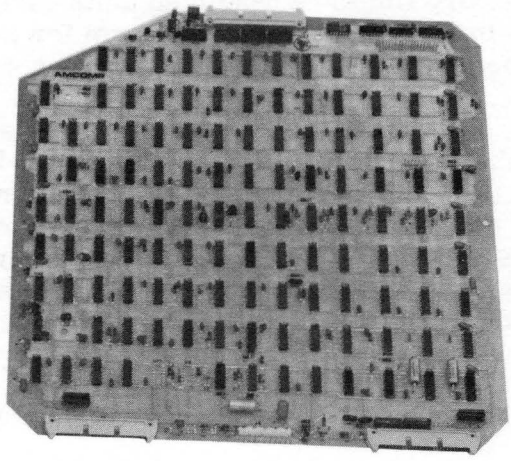
An interleaving feature, available as an option, changes the numbering scheme of the tracks and assures processor time between consecutively numbered sectors. (See paragraph 1-5.)

Error checking is provided by a 16-bit cyclic code word and an odd parity bit that are automatically written by the controller at the end of each subsector. When each subsector is read, the cyclic code and the parity bit are read and compared against the code that was generated from the previous 16 words. If the codes differ, the data error status flag is set indicating a data error.





ADAPTER BOARD



FORMATTER BOARD

Figure 1-1. 8011 Disc Memory Controller

When the 8011 Controller is providing a diagnostic mode of operation, it allows approximately one-half of its circuitry to be checked independently of the disc memory units. During this mode of operation, 16 words of data are transferred between the Nova Computer and the controller without accessing the disc memory units. Note that there must be a disc on line to run the diagnostic mode.

1-3 PHYSICAL DESCRIPTION

The formatter PC board and power supply are contained in a 19-inch rack-mount-table chassis (formatter assembly). The adapter PC board plugs into an input/output slot in the Nova Computer. (See table 1-1 for specifications and characteristics.)

TABLE 1-1. SPECIFICATIONS AND CHARACTERISTICS

Power Requirements	
Formatter Assembly	
Voltage	100, 120, 220, 240 Vac +5%, -10%
Frequency	50 or 60 Hz ± 5% single phase
Run Current	3 amps at 120 volts
Adapter Board	
Voltage	+5 Vdc (supplied by computer)
Current	4 amps (supplied by computer)
Environmental Specifications	
Operating Temperature	$0^{o}C$ to $55^{o}C$
Non-Operating Temperature	$-30^{o}C$ to $+65^{o}C$
Temperature Change	$10^{o}C$ per hour maximum
Relative Humidity (Operating)	10% to 90% without condensation
Relative Humidity (Non-Operating)	0% to 90% without condensation
Physical Characteristic	
Formatter Assembly	
Height	5.25 in. (13.34 cm.)
Width	16.88 in. (42.88 cm.)
Depth	21.00 in. (53.34 cm.)
Weight	30.00 lbs. (13.50 Kg.)

TABLE 1-1. SPECIFICATIONS AND CHARACTERISTICS (continued)

Adapter Board (plugged in computer slot)	
Height	0.5 in. (1.27 cm.)
Width	15.0 in. (38.10 cm.)
Depth	15.0 in. (38.10 cm.)

1-4 FUNCTIONAL DESCRIPTION

At the start of any operation the computer sends instructions to the controller. These instructions specify the starting core memory address, unit address, track address, and sector address. They also specify the operation to be performed (read, write, or diagnostic mode).

In addition to the instructions from the Nova Computer, the operational software can provide instruction (DOC) to allow a subsector address and subsector count to be specified.

After selection of the unit address and track address, specified in the instruction from the computer, the controller selects the disc operation contained in the computer instruction by generating either the start (READ) or pulse (WRITE) function.

If the controller is placed in the diagnostic mode, the read and write operations specified by the computer are performed only between the computer and controller. (See chapters 3 and 4 for more complete functional information.)

1-5 INTERLEAVING

Since the controller cannot process consecutively physically adjacent sectors on a track, the sectors are numbered alternately with the numbering scheme changing from one track to the next as shown in the tracks of figure 1-2. With such numbering arrangement, the program can process consecutively numbered sectors in a given track and switch to the first sector of the next track all with minimum waiting time. Thus, switching time between sectors is 2.085 milliseconds except when switching from sector 3 to sector 4 for which the time is double (2 sectors apart), i.e., 4.17 milliseconds. The interleave of figure 1-2 shows the track-sector configuration for a 3600-rpm disc unit with 4:1 interlace factor.

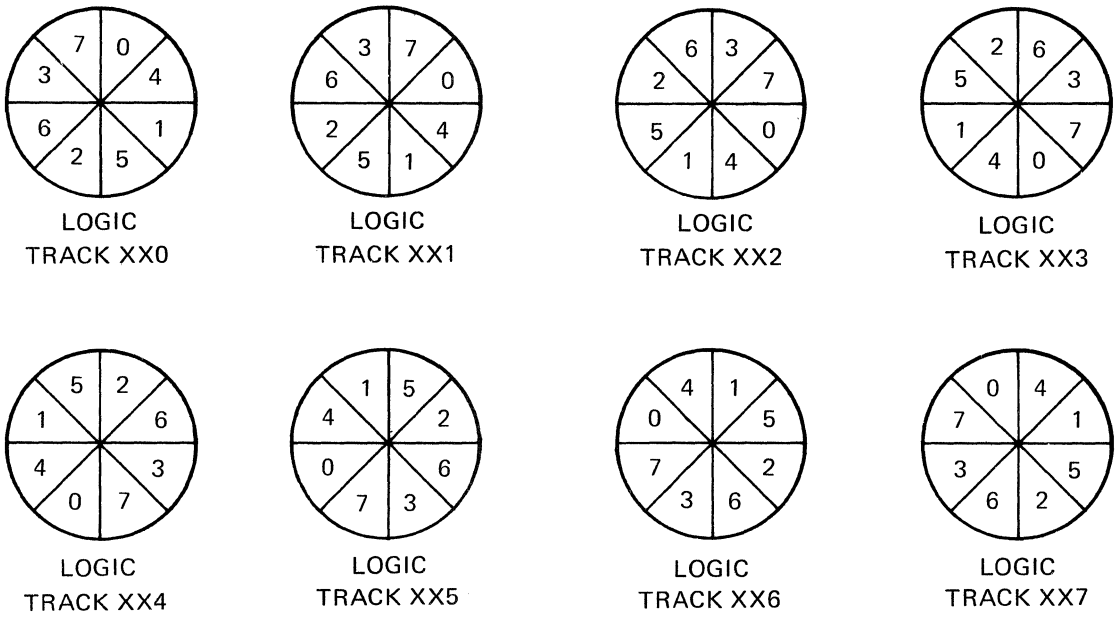


Figure 1-2. Track-Sector Configuration

Chapter 2

INSTALLATION AND CHECKOUT

INSTALLATION AND CHECKOUT

2-1 INTRODUCTION

This chapter provides installation instructions for the 8011 Disc Memory Controller. Included in this chapter are unpacking and equipment location instructions, an installation procedure, tables and diagrams, and voltage selection procedure. The installation procedure, tables and diagrams provide the following instructions:

1. Wiring and connecting the cable assemblies between the Nova Computer and the formatter assembly.

2. Installing the adapter PC board.

3. Wiring the Nova Computer backplane (cables 1060024 and 1060025).

4. Wiring the formatter PC board for the proper system configuration.

5. Wiring the disc memory units for address assignments.

6. Connecting the disc memory unit or units to the formatter assembly.

2-2 UNPACKING AND INSPECTION

The controller is shipped in a special packing case. As the equipment is unpacked, care should be exercised to prevent damage to the finished surfaces of the unit. All parts should be inspected for evidence of damage during shipment. If the packing case or any unit parts are damaged, advise the manufacturer and file a claim with the transfer company. The following procedure should be followed for unpacking and inspecting the unit:

a. Open the packing case and remove the contents. Check items removed against the shipping list to verify packing case contents. Contact AMCOMP in the event there is a shortage.

b. Remove any additional packing material and verify that the serial number of the unit corresponds to that shown on the shipping invoice.

NOTE

If reshipment of unit becomes necessary, a new packing case may be acquired from the manufacturer. The manufacturer is not responsible for damage incurred during shipment due to faulty packing.

c. Visually inspect the exterior of the unit for evidence of any physical damage that may have occurred in transit. Inspect the cover for dents or abrasions.

d. Check for broken or damaged components and broken or loose wires on connectors.

NOTE

If any damage is discovered, notify the manufacturer and the transfer company immediately. If manufacturer is not notified of the damage to the unit and damaged unit is subsequently operated may void the warranty.

2-3 EQUIPMENT LOCATION

The formatter assembly is a slide mountable chassis mounted on the cabinet together with the outer slides. The adapter PC board is installed in a selected slot within the Nova Computer chassis.

2-4 INSTALLATION PROCEDURE

A cabling diagram for a typical 8011 Disc Memory Controller is shown in figure 2-1. Tables 2-1, 2-2 and 2-3 list the signals between the adapter and formatter board, between formatter and disc memory unit, and between adapter board and Nova Computer. Install the controller as follows:

a. Select an I/O slot on the Nova Computer for installing the adapter PC board and then wire backplane connector end of CPU-A cable assembly (Part No. 1060024) to pins of electrical connector A of selected I/O slot according to wiring connections given in table 2-1.

b. Wire backplane connector end of CPU-B cable assembly (Part No. 1060025) to pins of electrical connector B of selected I/O slot in accordance with wiring connections given in table 2-1.

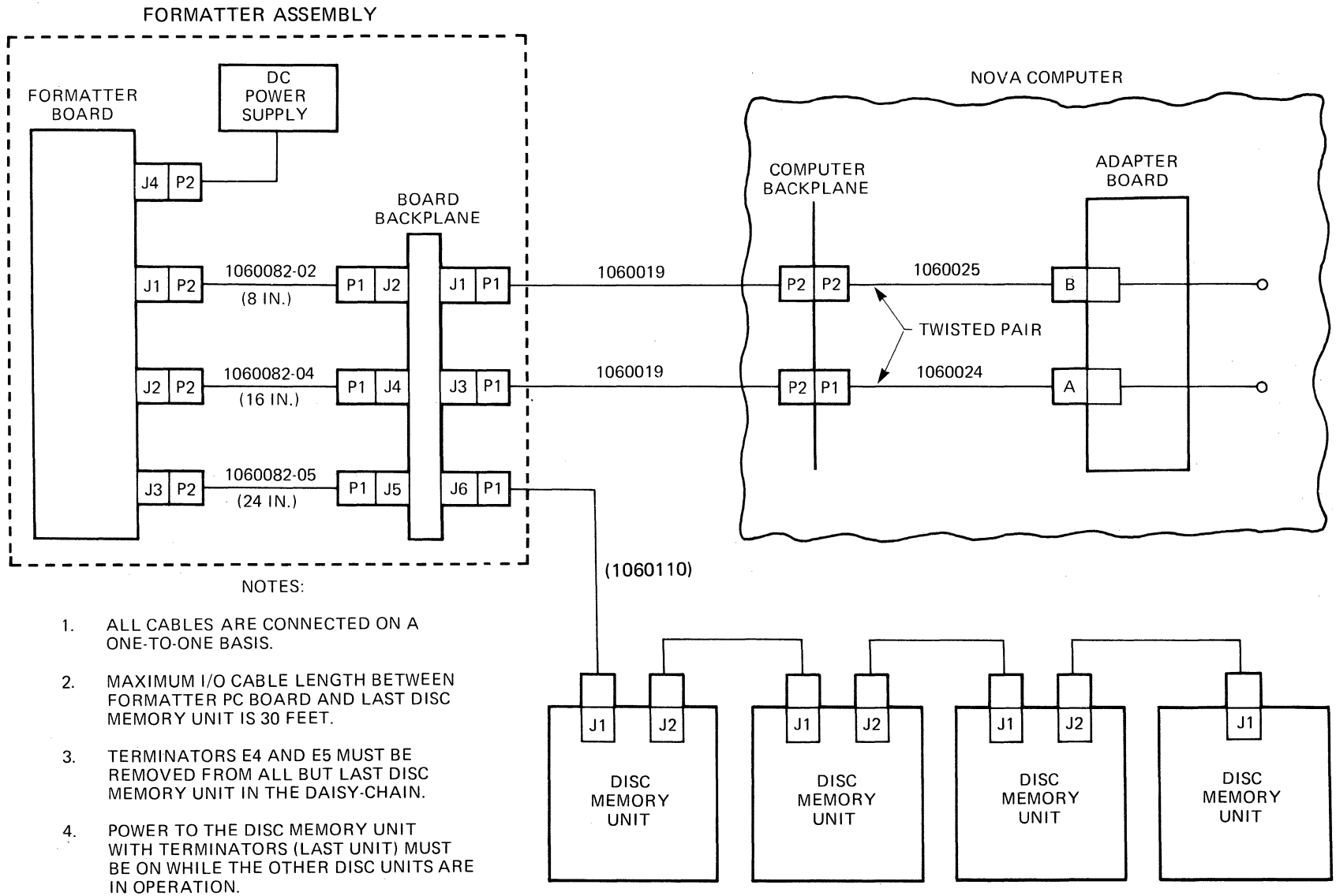
c. Install the adapter PC board in selected I/O slot.

d. Connect one of the two formatter cable assemblies (Part No. 1060019) to connector J2 on formatter PC board via backplane connector J3. Connect other end (P2) of this cable to CPU-A cable assembly (figure 2-1).

e. Connect other formatter cable assembly (Part No. 1060019) to connector J1 on formatter PC board via backplane connector J1. Connect other end (P2) of this cable assembly to CPU-B cable assembly (figure 2-1).

CAUTION

Connector J1 on formatter board (J1 on backplane) must be connected to CPU-B on computer, and connector J2 (J3 on backplane) must be connected to CPU-A on computer, or electrical damage to equipment may result.



NOTES:

1. ALL CABLES ARE CONNECTED ON A ONE-TO-ONE BASIS.
2. MAXIMUM I/O CABLE LENGTH BETWEEN FORMATTER PC BOARD AND LAST DISC MEMORY UNIT IS 30 FEET.
3. TERMINATORS E4 AND E5 MUST BE REMOVED FROM ALL BUT LAST DISC MEMORY UNIT IN THE DAISY-CHAIN.
4. POWER TO THE DISC MEMORY UNIT WITH TERMINATORS (LAST UNIT) MUST BE ON WHILE THE OTHER DISC UNITS ARE IN OPERATION.

Figure 2-1. Typical 8011 Disc Memory Controller Cabling Diagram (Daisy-Chain Configuration)

TABLE 2-1. FORMATTER/ADAPTER BOARD SIGNAL AND CONNECTOR PIN ASSIGNMENTS

SIGNAL DEFINITION	SIGNAL MNEMONIC	ORIGINATION		CONNECTOR/PIN	
		FORMATTER BOARD	ADAPTER BOARD	FORMATTER BOARD	ADAPTER BOARD
Buffer Empty	BFEMTY	X		J2-19	A-77
Buffer Full	BFFUL-	X		J2-21	A-78
Buffers	BUFFS		X	J2-39	A-90
Data Bit 00	DB00		X	J1-9	B-11
01	DB01-		X	J1-11	B-13
02	DB02-		X	J1-13	B-15
03	DB03-		X	J1-15	B-19
04	DB04-		X	J1-17	B-23
05	DB05-		X	J1-19	B-25
06	DB06-		X	J1-21	B-27
07	DB07-		X	J1-23	B-31
08	DB08-		X	J1-25	B-48
09	DB09-		X	J1-27	B-49
10	DB10-		X	J1-29	B-51
11	DB11-		X	J1-31	B-52
12	DB12-		X	J1-33	B-53
13	DB13-		X	J1-35	B-54
14	DB14-		X	J1-37	B-67
15	DB15-		X	J1-39	B-69
Data Register Arrival	DRAVL-		X	J2-43	A-92
Data Register Full	DRFUL-	X		J2-17	A-76
Data Register Set	DRSETPS-		X	J2-41	A-91
Data Bit 00	DB00-	X		J1-9	B-11
01	DB01-	X		J1-11	B-13
02	DB02-	X		J1-13	B-15
03	DB03-	X		J1-15	B-19
04	DB04-	X		J1-17	B-23
05	DB05-	X		J1-19	B-25
06	DB06-	X		J1-21	B-27
07	DB07-	X		J1-23	B-31
08	DB08-	X		J1-25	B-48
09	DB09-	X		J1-27	B-49
10	DB10-	X		J1-29	B-51
11	DB11-	X		J1-31	B-52
12	DB12-	X		J1-33	B-53
13	DB13-	X		J1-35	B-54
14	DB14-	X		J1-37	B-67
15	DB15-	X		J1-39	B-69
Data Register Full	DRFUL-	X		J2-17	A-76
Data Register Gate	DRGAT-		X	J2-23	A-79
DOC Instruction	DOCX		X	J2-31	A-86
End Error	ENDER-	X		J2-15	A-75

TABLE 2-1. FORMATTER/ADAPTER BOARD SIGNAL AND CONNECTOR PIN ASSIGNMENTS (continued)

SIGNAL DEFINITION	SIGNAL MNEMONIC	ORIGINATION		CONNECTOR/PIN	
		FORMATTER BOARD	ADAPTER BOARD	FORMATTER BOARD	ADAPTER BOARD
End Strobe	ENDSTR	X		J2-13	A-73
Initiate	INIT		X	J2-35	A-88
Read Operation	RDOP		X	J1-41	B-34
Read Sector Go	RSGO-		X	J1-43	B-38
Reset	RST		X	J2-33	A-87
Sector Continue Operation Clock	SCOPCK	X		J2-11	A-71
Status In	STATIN		X	J2-25	A-81
Subsector Address Load One-Shot	SALDS-		X	J2-29	A-85
Track/Sector Address Set	TSASET		X	J2-27	A-83
Write Operation	WROP		X	J1-45	B-40
Write Sector Go	WSGO-		X	J1-47	B-36

TABLE 2-2. FORMATTER BOARD/DISC MEMORY UNIT I/O SIGNAL AND PIN ASSIGNMENTS (CONNECTOR J3)

SIGNAL DEFINITION	SIGNAL MNEMONIC	INPUT TO FORMATTER	OUTPUT FROM FORMATTER	PIN No.
Disc Ready	DSCRDY	X		2
Return	GND			1
Head Change	HEAD CHANGE		X	32
Perm Address	PERM ADDRESS	X		17
Return	GND			18
Read	READ		X	27
Read Clock	RD CLK	X		39
Return	GND			40
Read Data	RD DATA	X		31
Sector Clock	SCLK	X		23
Return	GND			24
Sector Write	SWD		X	25
Return	GND			26
Track Address 0	TA0		X	11
1	TA1		X	10
2	TA2		X	9
3	TA3		X	8
4	TA4		X	7
5	TA5		X	6
6	TA6		X	5
7	TA7		X	4
8	TA8		X	3

TABLE 2-2. FORMATTER CARD/DISC MEMORY UNIT I/O SIGNAL AND PIN ASSIGNMENTS (CONNECTOR J3) (continued)

SIGNAL DEFINITION	SIGNAL MNEMONIC	INPUT TO FORMATTER	OUTPUT FROM FORMATTER	PIN No.
Track Origin	TO	X		21
Return	GND			22
Unit Select 0	USEL 0		X	15
1	USEL 1		X	14
2	USEL 2		X	13
3	USEL 3		X	12
Write	$\overline{\text{WRT}}$		X	29
Return	GND			30
Write Clock In	WR CLK IN		X	43
Return	GND			44
Write Clock Out	WCLK	X		47
Return	GND			48
Write Data	WR DATA		X	35
Return	GND			36

TABLE 2-3. ADAPTER BOARD/NOVA COMPUTER I/O SIGNAL AND PIN ASSIGNMENTS

SIGNAL NAME	SIGNAL MNEMONIC	INPUT TO ADAPTER	OUTPUT FROM ADAPTER	CONNECTOR/PIN
Clear	CLR	X		A-50
Data 00	DATA00	X		A-62
01	01	X		A-65
02	02	X		A-82
03	03	X		A-73
04	04	X		A-61
05	05	X		A-57
06	06	X		A-95
07	07	X		A-55
08	08	X		A-60
09	09	X		A-63
10	10	X		A-75
11	11	X		A-58
12	12	X		A-59
13	13	X		A-64
14	14	X		A-56
15	15	X		A-66
Data In A Instruction	DATIA	X		A-44
Data In B Instruction	DATIB	X		A-42
Data Out A Instruction	DATOA	X		A-58
Data Out B Instruction	DATOB	X		A-56
Data Out C Instruction	DATOC	X		A-48
Data Channel Acknowledge	DCHA-	X		A-60

TABLE 2-3. ADAPTER BOARD/NOVA COMPUTER I/O SIGNAL AND PIN ASSIGNMENTS (continued)

SIGNAL NAME	SIGNAL MNEMONIC	INPUT TO ADAPTER	OUTPUT FROM ADAPTER	CONNECTOR/PIN
Data Channel In	DCHI	X		B-37
Data Channel Mode	DCHMO-		X	B-17
Data Channel Out	DCHO	X		B-33
Data Channel Priority In	DCHPIN-	X		A-94
Data Channel Priority Out	DCHPOT-		X	A-93
Data Channel Request	DCHR-		X	B-35
Device Select 0	DS0-	X		A-72
1	DS1-	X		A-68
2	DS2-	X		A-66
3	DS3-	X		A-46
4	DS4-	X		A-62
5	DS5-	X		A-64
Interrupt Acknowledge	INTA	X		A-40
Interrupt Priority In	INTPIN-	X		A-96
Interrupt Priority Out	INTPOT-		X	A-95
Interrupt Received	INTR-		X	A-29
Input/Output Pulse	IOPLS	X		A-74
Input/Output Reset	IORST	X		A-70
Mask Out	MSKO-	X		A-38
Request Enable	RQENB-	X		B-4
Select Busy	SELB-		X	A-82
Select Done	SELD-		X	A-80
Start	STRT	X		A-52

f. Verify proper wiring of "E" pins on formatter for proper disc memory unit according to table 2-4.

g. Verify proper wiring of "E" pins on formatter board for proper sector interlace factor in accordance with tables 2-5 and 2-6.

h. Verify proper wiring of "E" pins on formatter board for proper system size in accordance with table 2-7.

i. Verify proper wiring of "E" pins on formatter board for disc unit address assignments as shown in table 2-8.

j. Verify "E" pins on formatter board for disc unit address assignments as shown in table 2-9.

k. Wire "E" pins on adapter board according to selected device address (unit is shipped for device address 20) as shown in table 2-10.

l. If daisy-chaining of disc memory units is used, remove signal line resistive terminations from PC board of each disc memory unit except from disc memory unit at end cable.

NOTE

It is recommended that disc unit address 0 be connected at the end of the daisy-chain cable assembly. This allows other disc memory units to be removed or connected without changing the system cabling.

TABLE 2-4. 8400/8500 DISC UNIT SELECTION WIRE CONNECTIONS

DISC MEMORY UNIT	STRAPPING
8400	E56 To E57 E59 To E61 E58 To E62
8500	E56 To E59 E61 To E58 E62 To E60

TABLE 2-5. SEQUENTIAL SECTOR INTERLACE WIRE CONNECTIONS

FROM	TO			
	1:1	2:1	4:1	8:1
E19	E40	E37	E32	E31
E20	E39	E40	E37	E32
E17	E34	E39	E40	E37
E18	E33	E34	E39	E40
E23	E30	E33	E34	E39
E24	E29	E30	E33	E34
E21	E31	E29	E30	E33
E22	E32	E31	E29	E30
E27	E37	E32	E31	E29

TABLE 2-6. WIRE CONNECTIONS FOR SECTOR INTERLACE WITH NOVA COMPUTER INTERLEAVING

SIGNAL	FROM	TO						
		AMCOMP COMPATIBLE				NOVA COMPATIBLE		
		1:1	2:1	4:1	8:1	1:1	2:1	4:1
LCC5	E29	E51	E51	E51	E19	E50	E50	E50
LCC4	E30	E52	E52	E52	E52	E51	E51	E51
LCC6	E31	E50	E50	E19	E20	E52	E52	E52
LCC7	E32	E49	E19	E20	E17	E23	E19	E19
LCC3	E33	E18	E23	E24	E21	E18	E23	E24
LCC2	E34	E17	E18	E23	E24	E17	E18	E23
LCC8	E37	E23	E24	E21	E22	E24	E24	E20
LCC1	E39	E20	E17	E18	E23	E20	E17	E18
LCC0	E40	E19	E20	E17	E18	E19	E20	E17
BN4	E41	E36	N/C	N/C	N/C	N/C	N/C	N/C
BN3	E42	E35	E35	N/C	N/C	E27	E27	E27
BN2	E43	E26	E26	E26	N/C	E22	E22	E22
BN1	E44	E25	E25	E25	E25	E21	E21	E21
AN4	E45	E27	N/C	N/C	N/C	N/C	N/C	N/C
AN3	E46	E22	E27	N/C	N/C	E56	E56	E56
AN2	E47	E21	E22	E27	N/C	E38	E38	E38
AN1	E48	E24	E21	E22	E27	E28	E28	E28
PUV	E53	E54	E54	E54	E54	E55	E55	E55

TABLE 2-7. 8400/8500 DISC SIZE WIRE CONNECTIONS

DISC SIZE (TRACKS)		MAXIMUM SIZE JUMPER								
8400	8500	FROM								TO
0	128	E9	E10	E11	E12	E13	E14	E15	E16	E2
16	144	E9	E10	E11	E12	E13	E14	E15		E2
32	160	E9	E10	E11	E12	E13	E14			E2
48	176	E9	E10	E11	E12	E13				E2
64	192	E9	E10	E11	E12					E2
80	208	E9	E10	E11						E2
96	224	E9	E10							E2
112	240	E9								E2

TABLE 2-8. UNIT SELECT ADDRESS WIRE CONNECTIONS

UNIT No.	FROM	TO
0	E1	E8
1	E1	E7
2	E1	E5
3	E1	E6

TABLE 2-9. HIGHEST UNIT NUMBER WIRING CONNECTIONS

HIGHEST UNIT No. ASSIGNED	TO	FROM	FROM	FROM
0	E3	E7	E6	E5
1	E3	E6	E7	
2	E3	E7		
3	NONE			

NOTE

For multiple units of different size (different number of tracks) but not exceeding two different sizes, the unit having the fewest tracks must be assigned the highest unit number.

TABLE 2-10. DEVICE ADDRESS SELECTION CONNECTIONS

ADDRESS	FROM	TO	COMMENTS
20	E1	E2	
60	E1	E3	Cut etch between E1 and E2

2-5 VOLTAGE SELECTION

Line voltages of 100, 120, 220, and 240 volts at an operating frequency of 48 to 62 Hz can be selected through a voltage selector PC board (figure 2-2) located in rear panel of the formatter chassis. To select an operating voltage perform the following steps:

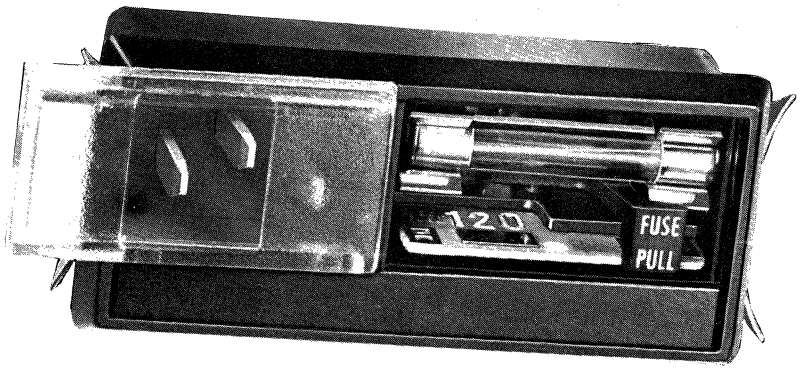
1. Open cover door and rotate fuse-pull to left.

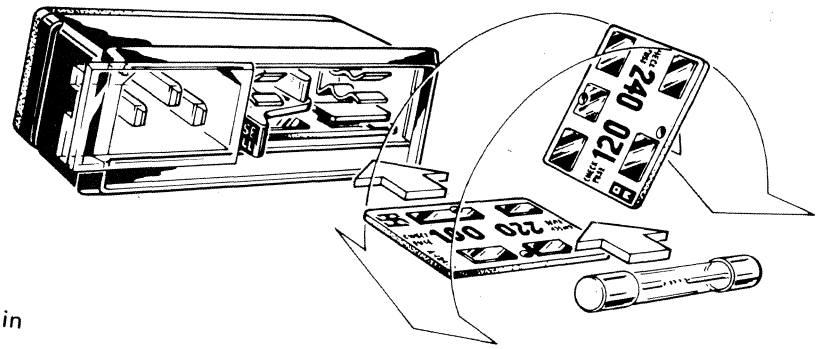
2. Select operating voltage by orienting PC board to position desired voltage on top left side. (Selected voltage should be visible when PC board is installed.)

3. Rotate fuse-pull back into normal position and re-insert fuse into holders, careful to install a fuse with correct value.

2-6 PERFORMANCE VERIFICATION

To verify program operation, refer to chapter 3, paragraph 3-10 and to User's Guide in Appendix A.





Operating voltage is shown in Connector window.

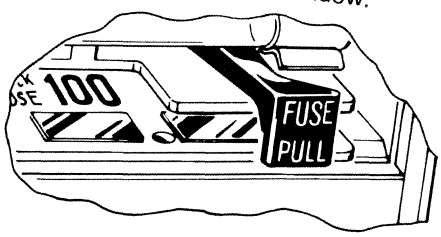


Figure 2-2. Voltage Selecting Connector

Chapter 3

OPERATION AND INTERFACE

OPERATION AND INTERFACE

3-1 INTRODUCTION

This chapter contains operation and programming considerations, interface input/output signals, and interface signal logic levels. Described in this chapter, under the above major paragraphs, are controller instructions, computer transfer instructions, loading information, and modes of operation.

The basic timing considerations, track selection requirements, write and read timing requirements, and a description of the input/output signals for the interface between the controller and the disc memory units are given in chapter 3 of the AMCOMP Operation and Maintenance Manuals for the disc memory unit.

3-2 OPERATION AND PROGRAMMING CONSIDERATIONS

The operation and programming considerations include controller instructions, computer input/output transfer instructions, automatic and non-automatic loading, and modes of operation.

3-3 CONTROLLER INSTRUCTIONS

The 8011 Disc Controller uses five of the Nova Computer I/O transfer instructions. These instructions are described in the following paragraphs.

3-4 DOA-, DSK (Data Out A-, Disc)

This instruction is as follows: Select the unit, track and sector according to the contents of ac (accumulator) bits 2 through 15 of the instruction as shown in figure 3-1, and perform the function specified by F (bits 8 and 9). The contents of F are as follows:

00 = No operation (NOP)

01 = Start (READ)

10 = CLEAR

11 = Pulse (WRITE)

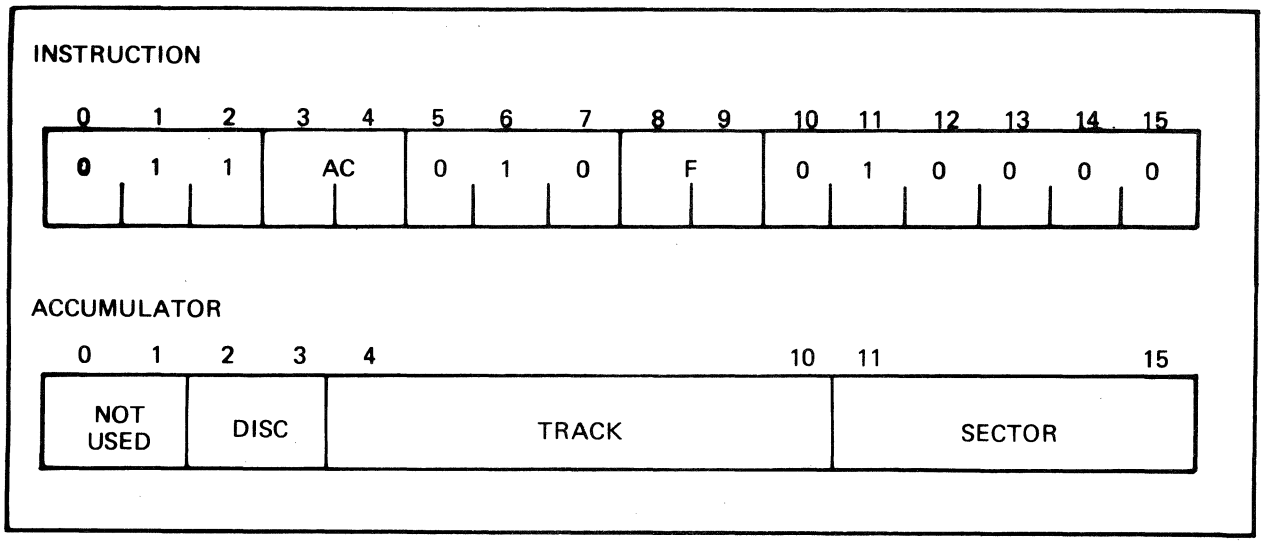


Figure 3-1. DOA-, DSK Instruction

3-5 DOB-, DSK (Data Out B-, Disc)

This instruction (figure 3-2) is as follows: Load the contents of accumulator bits 0 through 15 into the core address counter (accumulator bit 0 should be 0) and perform the function specified by F (bits 8 and 9).

NOTE

If a logical 1 bit is contained in accumulator bit 0, the controller is placed in the diagnostic move.

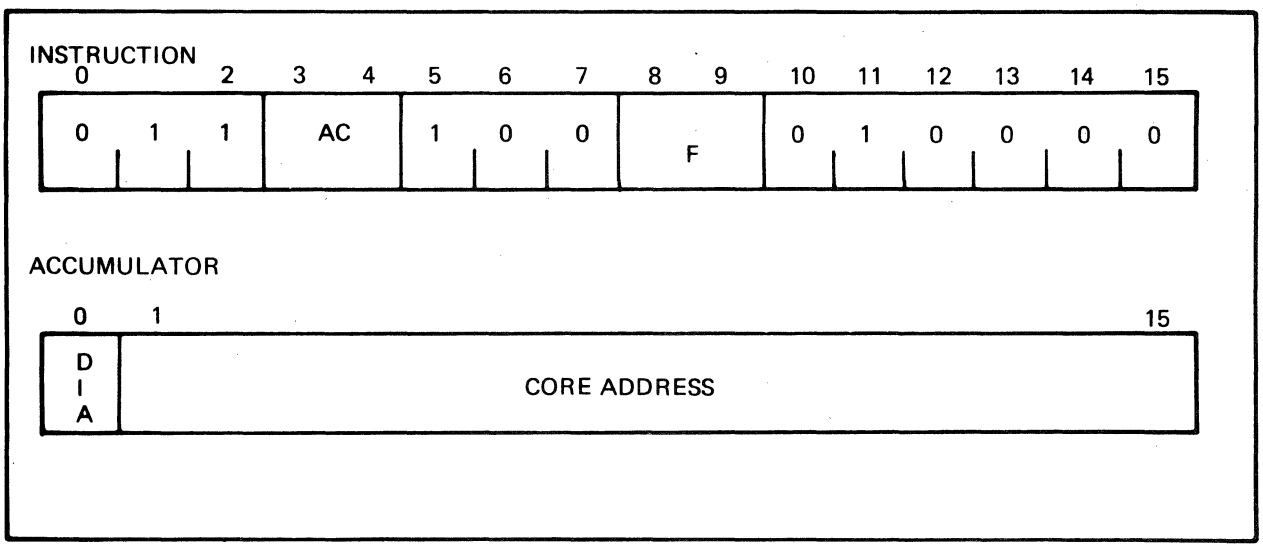


Figure 3-2. DOB-, DSK Instruction

3-6 DIA-, DSK (Data In A-, Disc)

This instruction reads the status of the disc memory system into accumulator bits 10 through 15 (figure 3-3), clears accumulator bits 0 through 9, and performs the function specified by F (bits 8 and 9). A logical 1 in bits 10 through 15 is decoded as follows:

a. Bit 10 (disc fail). The selected disc becomes not ready or the system is hung during a read or write operation (time out or ready). The setting of this bit clears Busy and sets Done, requesting an interrupt if interrupt disable is clear.

b. Bit 11 (write error). The program has specified write instruction and the selected track-sector is write-protected.

c. Bit 12 (timer error). The data channel, during read or write, has failed to respond in time to a request for access (i.e., because of preemption of the channel by faster devices).

d. Bit 13 (no such disc). The disc or track selected by the program is not available on this system. The setting of this bit clears busy and sets done, requesting an interrupt if interrupt disable is clear.

e. Bit 14 (data error). During a read operation, the cyclic check word or parity bit read from the disc differed from that computed by the controller for the data in the subsector.

f. Bit 15 (error). Bit 10, 11, 12, 13, 14 are a logical 1.

NOTE

The clear, start, or pulse function in an instruction clears all of the flags established by the setting of bits 10 through 15.

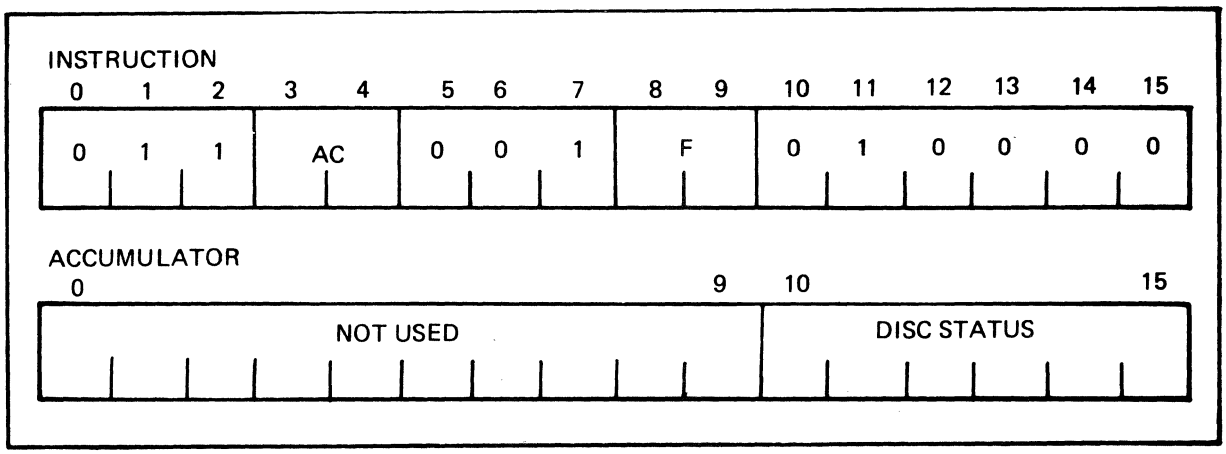


Figure 3-3. DIA-, DSK Instruction

3-7 DIB-, DSK (Data In B-, Disc)

This instruction (figure 3-4) is as follows: Read the present contents of the core address counter into accumulator bits 0 through 15. If the accumulator bit 0 is a logical 1, the unit is in the diagnostic mode. The contents of the core address counter is presented as zeros when this instruction is executed while the system is busy. This instruction can be ordinarily used for diagnostic purposes. Perform the function specified by F (bits 8 and 9).

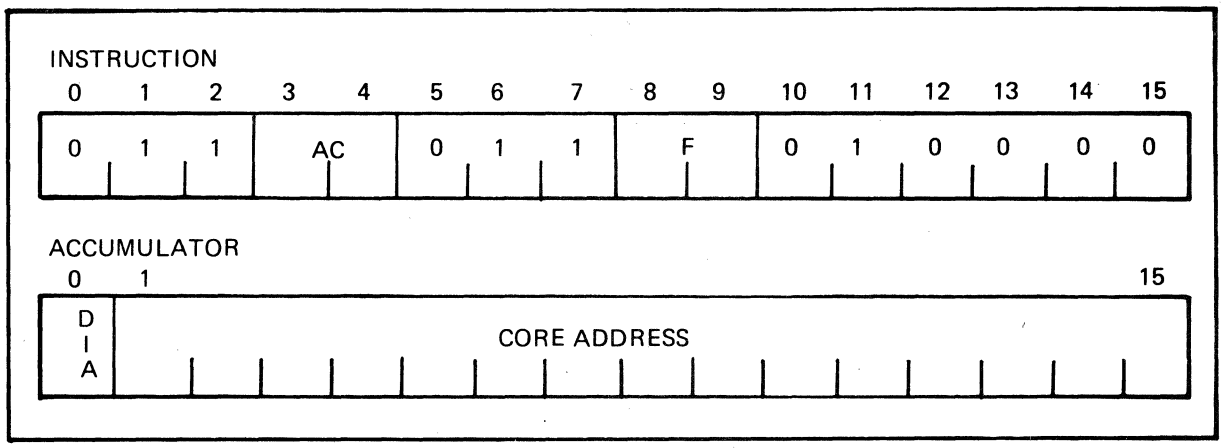


Figure 3-4. DIB-, DSK Instruction

3-8 DOC O, DSK (Data Out C , Disc)

This instruction (figure 3-5) is as follows: Select the starting subsector address according to the contents of accumulator bits 0 through 3 and perform the function specified by F in the length according to the contents of accumulator bits 4 through 15. The 12-bit number expresses the length of operation in terms of number of subsectors. It must be a number in 2's complement form. The total number of words transferred is 16 times the specified subsector number.

The DOC instruction extends the capability of the controller beyond that provided by the Data General Disc System. It allows disc addressing to the subsector level. It also allows multiple (1-4096) subsector operation. When all 12 bits of accumulator bits 4 through 15 are specified as zeros, 4096 subsectors will be operated. When the DOC instruction is not executed, the operation is performed as one sector (16 subsectors) operation with disc subsector address starting at 0, which is compatible with the Data General Fixed Head Disc System.

NOTE

If accumulator bits 4 through 15 are all high, one subsector will be transferred.

If the DOC instruction is not executed, the system will transfer only one sector (256 words) of data.

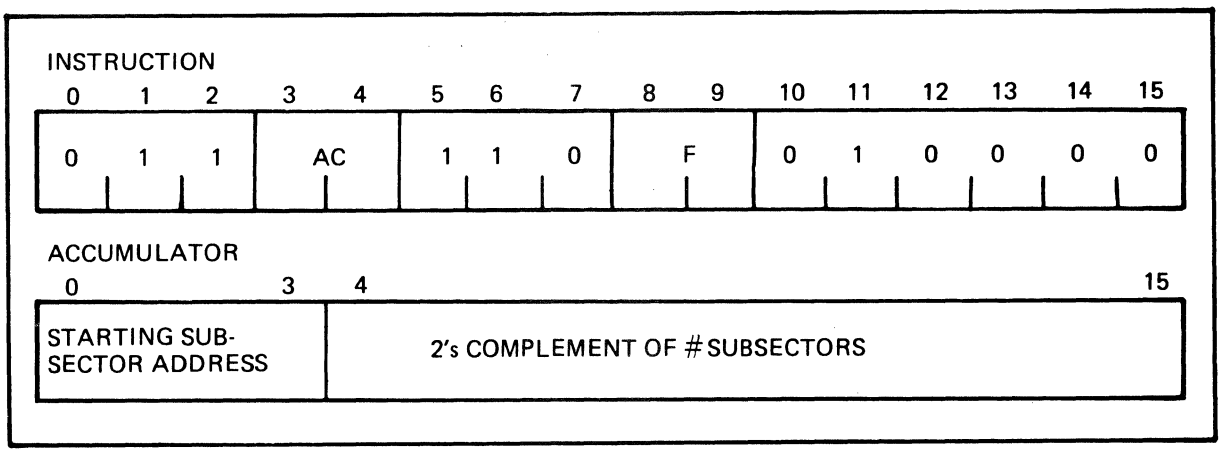


Figure 3-5. DOC 0, DSK Instruction

3-9 COMPUTER I/O TRANSFER INSTRUCTIONS

The controller has the Nova Computer device code 20, mnemonic DSK, and uses five of the computer I/O transfer instructions. The busy and done flags from the controller are sensed by bits 8 and 9 in the computer skip instructions. The busy and done flags are controlled by the clear, start or pulse function in the instruction. Interrupt disable from the controller is controlled by interrupt priority task bit 9 in the computer. When a second controller is connected to the computer, its device code is 60, mnemonic DSK. If other disc memory units are used, additional codes are assigned.

The clear function in an instruction clears the busy and done flags, and thus terminates data transfers if a track sector is currently being processed. In addition to specifying the function, start and pulse both clear the done flag and set the busy flag. Start selects the read function and pulse selects the write function. Clear, start and pulse each clear the disc memory system status flags: disc fail, write error, data late, no such disc, data error and error.

3-10 AUTOMATIC AND NON-AUTOMATIC LOADING

Ordinarily sector 0, track 0 of disc 0 is reserved for binary loader. If the loader in core is destroyed by program debugging, it can be restored from the disc. The automatic and non-automatic loading procedures are described below.

3-11 Automatic Loading

To bring the loader into memory automatically, proceed as follows:

a. Set device code 20 into DATA switches 10 through 15 at the computer console for disc operation. Set device code 10 into DATA switches for TTY with paper tape operation.

b. If a Nova 1200 or 800 Series Computer with the program load option is being used, position the RESET-STOP switch to RESET position, turn on DATA switch 0, and then position PROGRAM LOAD switch to PROGRAM LOAD position. If a Supernova Computer is being used, position RESET-

STOP switch to RESET position and then position PROGRAM LOAD-CHANNEL start switch to CHANNEL START position.

3-12 Non-Automatic Loading

To bring the loader into memory without automatic loading, proceed as follows:

a. Load bootstrap loader into upper core through the switches.

b. Load binary loader (paper tape) into reader.

c. Set RESET-STOP switch to RESET.

d. Set switches to XX7770. 007770=4K and 777770-32K.

NOTE

If using a high speed reader switch, 0 must be a "1". If using TTY, switch 0 must be a "0".

e. Switch START-CONTINUE to START. (Program will stop at location XX 7777.)

f. Load program tape into reader.

g. START-CONTINUE.

h. Reference program tape listing for starting address and operation of program.

3-13 MODES OF OPERATION

The operation to be performed (read, write, or diagnostic) is specified in the instructions sent to the controller by the Nova Computer. These instructions are the DOA and DOB.

After one read operation, no further DOB instructions need be issued if subsequent operations are to be read operations and are to access consecutive sectors in core memory. For write operations, both the DOA and DOB instructions should be given.

At the completion of each operation, the program should check the status of the disc memory system, and if the data was late or in error, the operation should be repeated. The status should not be checked before starting an operation with a disc; the status is not valid until an operation has been performed.

3-14 Write Operation

When a write operation (pulse) is specified by the instructions from the computer, the controller requests and gains control of the computer data channel and starts transferring words consecutively into a 16-word data buffer. Simultaneously, the controller searches for the sector address on the selected track by comparing the sector address with an incrementing sector counter of the disc. When the specified sector is found, data in the buffer is written on the disc into the first 16-word subsector. The writing operation is

continued until one sector (16 subsectors) of data is transferred, or the specified number of subsectors are transferred (as specified in the DOC instruction). If the DOC instruction is not executed prior to or with the generation of the I/O pulse, one sector (16 subsectors) of data is transferred. Otherwise, the number of subsectors of data transferred is the number of subsectors specified by the DOC instruction.

3-15 Read Operation

When a read operation (start) is specified by the instructions from the computer, the controller searches for the sector address on the selected disc and track by comparing the sector address with the incrementing sector counter of the disc. Data words are then transferred from the disc into the 16-word data buffer. With the first word in the data buffer, the controller then requests and gains use of the data channel for inputting data to the computer. The length of data transfer is the same as that for the write operation.

3-16 Diagnostic Mode of Operation

When the controller is in the diagnostic mode, the read or write operation specified by the computer causes data transfers to be performed only between the computer and the controller.

The controller is placed in the diagnostic mode when a logical 1 is contained in accumulator bit 0 of a DOB instruction from the computer. The controller remains in the diagnostic mode until a logical 0 is contained in accumulator bit 0 in a subsequent DOB instruction from the computer. The DOA instruction that normally specifies the disc, track and sector address is not required in the diagnostic mode. A specified pulse function in the DOB instruction causes 16 words of data to be transferred from the specified core address in the computer to the 16-word buffer in the controller. The contents of the 16-word buffer is then read back to the computer when the computer issues a DOB instruction containing a start function. The contents of the buffer is read back in the logical 1's complement form from which it was written. The diagnostic mode of operation allows 16 words of data to be transferred between the computer and controller for diagnostic purposes without accessing the disc memory.

3-17 INTERFACE INPUT/OUTPUT SIGNALS

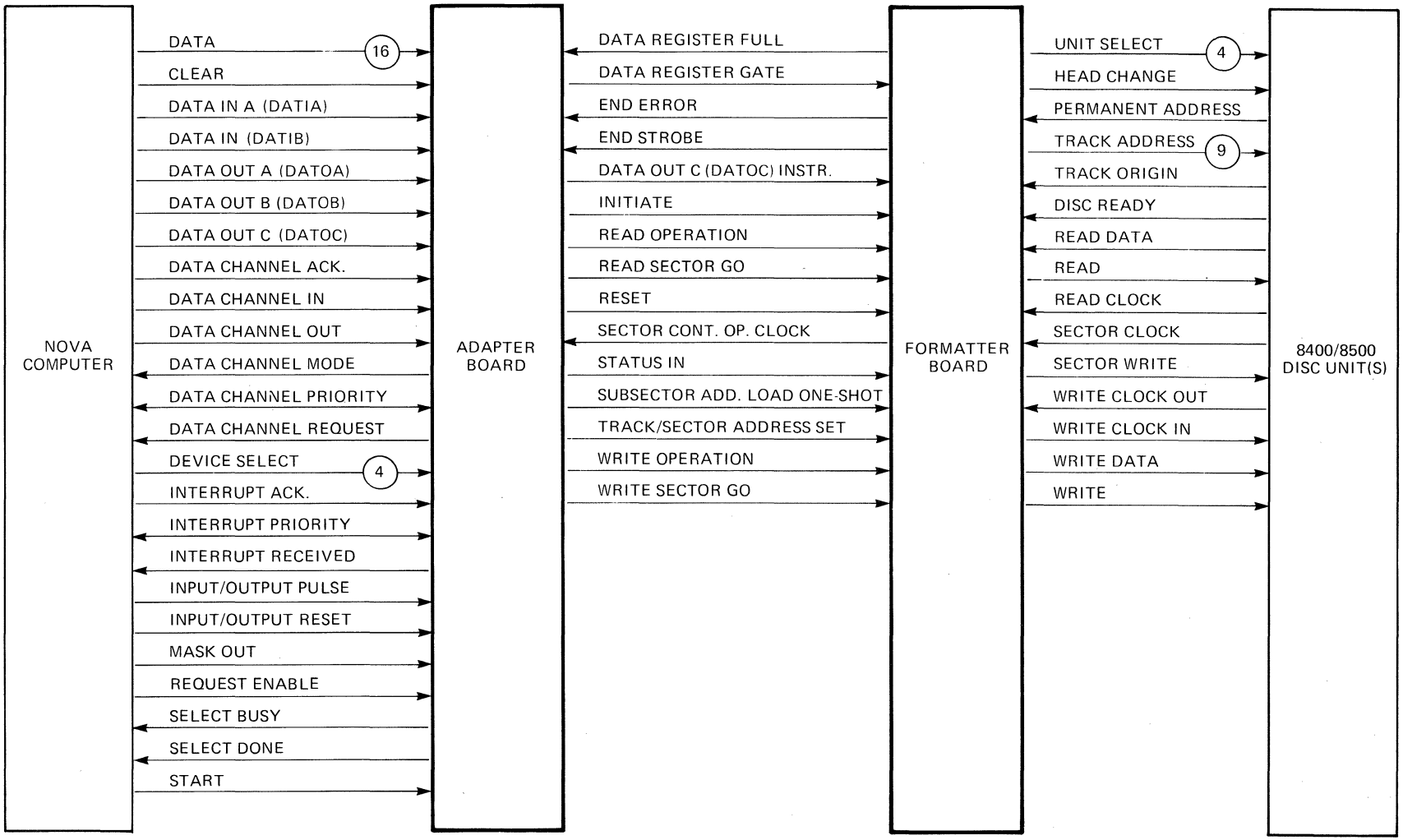
The description of the interface signals are divided into two categories: the Nova Computer to the controller and the controller to Nova Computer interface signals. Figure 3-6 contains the signals interfacing the controller (adapter and formatter boards).

3-18 NOVA COMPUTER TO CONTROLLER INTERFACE SIGNALS

The following paragraphs describe the interface signals from the Nova Computer to the 8011 Controller.

3-19 Device Selection (DS0 through DS5)

These signal lines are low in the assertive state. The processor places the device code (bits 10 through 15 of the instruction word) on these signal lines during the execution of an in-out instruction. These signal lines select one of 59 devices (codes 04 through 76) that may be connected to the I/O bus (the controller has the device code 20, mnemonic DSK). Only the selected device responds to control signals generated during the instruction.



NOTE: FOR SIGNAL MNEMONICS SEE TABLES 2-1, 2-2, AND 2-3.

Figure 3-6. Controller Interface Signals

3-20 Data (DATA 0 through DATA 15)

These signal lines are low when true and are used to transfer all data and addresses between the processor and controller.

For a programmed output, the processor places the accumulators specified by the instruction on the data lines and then generates DATOA, DATOB, or DATOC to load the data from the lines into the corresponding buffer in the controller of the disc memory system (selected device); or generates MSKO to set up the interrupt disable flags in all of the devices according to the mask on the data lines. For data channel output, the processor places the memory buffer on the data lines and generates signal DCHO to load the contents of the lines into the data register in the controller.

3-21 Data Out A (DATOA)

This signal is high when true and is generated by the processor after the accumulator signals have been placed on the data lines in a DOA instruction. DATOA is used to load the address into the unit, track and sector registers on the controller when the disc memory system is the device selected by DS0 through DS5.

3-22 Data In A (DATIA)

This signal is high when true and is generated by the processor during a DIA instruction to place the error register in the controller on the data lines when the disc memory system is the device selected by DS0 through DS5.

3-23 Data Out B (DATOB)

This signal is high when true and is generated by the processor, after accumulator data has been placed on the data lines in a DOB instruction. DATOB signal loads the data into the core memory address register in the controller when the disc memory system is the device selected by DS0 through DS5.

3-24 Data In B (DATIB)

This signal is high when true and is generated by the processor during DIB instruction. DATIB signal places the core memory address register in the controller on the data lines when the disc memory system is the device selected by DS0 through DS5.

3-25 Data Out C (DATOC)

This signal is high when true and is generated by the processor after accumulator bits have been placed on the data lines in a DOC instruction. DATOC signal loads the counter and subsector address register in the controller when the disc memory system is the device selected by DS0 through DS5.

3-26 Start (STRT)

This signal is high when true and is generated by the processor in a non-skip I/O instruction (DOA, DOB, DOC, etc.) with an S control function (bits 8 and 9 = 01). STRT signal clears done, sets busy, clears the INT REQ flip-flop, and selects a read operation in the controller when the disc memory system is the device selected by DS0 through DS5.

3-27 Clear (CLR)

This signal is high when true and is generated by the processor in a non-skip I/O instruction with a C control function (bits 8 and 9 = 10). CLR clears busy, done and INT REQ flip-flop in the controller when the disc memory system is the device selected by DS0 through DS5.

3-28 I/O Pulse (IOPLS)

This signal is high when true and is generated by the processor in a non-skip I/O instruction with a P control function (bits 8 and 9 = 11). IOPLS selects a write, clears done, sets busy, and clears the INT REQ flip-flop in the controller when the disc memory system is the device selected by DS0 through DS5.

3-29 Request Enable (RQENB)

This signal is low when true and is generated at the beginning of every memory cycle to allow all devices (including the disc memory system) on the I/O bus to request program interrupts or data channel access. In any device, RQENB sets the INT REQ flip-flop if done signal is set and interrupt disable is clear; otherwise, it clears INT REQ flip-flop. In any device connected to the data channel, RQENB sets the DCH REQ flip-flop if the DCH SYNC flip-flop is set; otherwise, it clears DCH REQ.

3-30 Interrupt Priority (INTP)

This signal is low when true and is generated by the processor for transmission serially to the device on the I/O bus. If the INT REQ flip-flop in a device is clear when the device received INTP, the signal is transmitted to the next device.

3-31 Interrupt Acknowledge (INTA)

This signal is high when true and is generated by the processor during the INTA instruction. If a device (including the disc memory system) received INTA while it is also receiving INTP and its INT REQ flip-flop is set, it places its device code on data lines 10 through 15.

3-32 Mask Out (MSKO)

This signal is low when true and is generated by the processor during the MSKO instruction after accumulator bits (data 09) have been placed on the data lines to set up the interrupt disable flags in all devices according to the mask on the lines.

3-33 Data Channel Priority (DCHP)

This signal is low when true and is generated by the processor and transmitted serially to the devices on the I/O bus. If the DCH REQ flip-flop in a device is clear when the device receives the DCHP signal, this signal is transmitted to the next device.

3-34 Data Channel Acknowledge (DCHA)

This signal is low when true and is generated by the processor at the beginning of a data channel cycle. If the controller receives DCHA while it is receiving DCHP and its DCH REQ flip-flop is set, it places the memory address to be used for data channel access on data lines 1 through 15 and sets the DCH SEL flip-flop.

3-35 Data Channel In (DCHI)

This signal is high when true and is generated by the processor for data channel input (DCHMO = logical 1) to place the data register of the controller on the data lines when the disc memory system is selected by DCHA.

3-36 Data Channel Out (DCHO)

This signal is high when true and is generated by the processor for data channel output (DCHMO = logical 0) after the word from memory or the arithmetic result has been placed on the data lines. DCHO signal loads the contents of the lines into the data register of the controller when the disc memory system is selected by DCHA.

3-37 I/O Reset (IORST)

This signal is high when true and is generated by the processor in the IORST instruction or when the console RESET switch is pressed to clear the control flip-flop in all interfaces connected to the I/O bus. This signal is also generated when power is turned on.

3-38 CONTROLLER TO NOVA COMPUTER INTERFACE SIGNALS

The following paragraphs describe the interface signals from the 8010 Controller to the Nova Computer.

3-39 Data (DATA0 through DATA15)

These signal lines are low when true and are used to transfer all data and addresses that are transferred between the processor and the controller.

For a programmed input, the processor generates DATIA or DATIB to place the error register or core memory address register in the controller on the data lines (when the disc memory system is selected by DS0 through DS5), or generates INTA to place the code of the nearest device that is requesting an interrupt on lines 10 through 15. The processor then loads the data from the lines into the accumulator selected by the instruction. To obtain an address for data channel access, the processor generates DCHA to place a memory address from the nearest device that is requesting access on lines 1 through 15 and then loads the address into the memory address register. For data channel input, the processor generates DCHI to place the data buffer of the controller on the data lines (when the disc memory system is the device being serviced), and then loads the contents of the lines into the memory buffer.

3-40 Selected Busy (SELB)

This signal is low when true and is generated by the controller (when the disc memory system is selected by DS0 through DS5) if its busy flag is set.

3-41 Selected Done (SELD)

This signal is low when true and is generated by the controller (when the disc memory system is selected by DS0 through DS5) if its done flag is set.

3-42 Interrupt Request (INTR)

This signal is low when true and is generated by any device (including the disc memory system) when its INT REQ flip-flop is set. In the disc controller the INT REQ flip-flop is set when the DONE flip-flop and INT MASK flip-flop are set.

3-43 Data Channel Request (DCHR)

This signal is low when true and is generated by any device (including the disc memory system) when its DCH REQ flip-flop is set. This informs the processor that the device is waiting for data channel access.

3-44 Data Channel Mode (DCHMO)

This signal is low when true and is generated by the controller when its DCH SEL flip-flop is set to inform the processor of the type of desired data channel cycle. For data in, this signal is low-true; for data out, the signal is high-true.

3-45 INTERFACE SIGNAL LOGIC LEVELS

The logic is either 14-pin or 16-pin dual in-line packages, with industrial operating temperatures ranging from $0^{o}C$ to $70^{o}C$. All logic circuits are constructed with TTL integrated circuit chips of the small-scale and medium-scale integration type.

The interface logic used is positive having the following levels:

Logical 1 (low-true = active low)	0 volts	nominal
	0.4 volts	maximum
Logical 0 (high-false = active high)	2.3 volts	minimum
	2.7 volts	nominal
	5.0 volts	maximum

NOTE

Internal logic levels are contained in chapter 4.

Chapter 4

THEORY OF OPERATION

THEORY OF OPERATION

4-1 INTRODUCTION

This chapter provides logic diagram information, overall theory and circuit descriptions for the 8011 Disc Memory Controller. This includes detailed circuit descriptions of the controller adapter and formatter PC (printed circuit) boards.

4-2 LOGIC DIAGRAM AND SIGNAL INFORMATION

The signals appearing on the adapter and formatter logic boards are listed in table 4-1. The signals from the adapter PC board to Nova Computer are low-true and those from Nova Computer to the adapter PC board are either low-true or high-true, depending upon the particular signal. The signals from/to disc memory unit are low-true.

The low-true signals carry a minus sign at the right end of the signal term (i.e., DSCRDY-), while the high-true signals are presented plainly (i.e., DSCRDY).

NOTE

The interface signals and their logic levels are described in chapter 3; their origin and destination are listed in the tables of chapter 2.

The controller internal logic (between adapter and formatter PC boards) is standard positive having the following levels:

Logic 0 (low) = 0 to +0.4 volts
Logic 1 (high) = 2.3 to +5.0 volts

4-3 KEY TO BASIC SYMBOLOGY

Figure 4-1 shows the gate as well as the JK and D-Type flip-flop symbols together with their truth tables.

4-4 JUMPER CONNECTIONS

The E pins on the formatter PC board are jumpered in order to achieve selection of 8400 or 8500 Disc Memory Unit, disc unit size, sequential sector interlace, sector interlace with Nova Computer interleaving and disc unit (1 through 4) selection. (See chapter 2, tables 2-4 through 2-10.

TABLE 4-1. SIGNAL DEFINITION AND MNEMONICS

Mnemonic Term	Signal Definition	Location*
Any Error	Output is negative true for any error output. This includes Read Error, Illegal Address Error, Data Transfer Error, Disc Failure Error, Write Protect Error or Ready Error.	83-2
AOVFA-	Address Over-Flow A	83-2
AOVFB-	Address Over-Flow B	83-2
AOVFE-	Address Over-Flow E	83-2
BCNT	Bit Count	83-1
BCNTO	Bit Count Zero	83-1
BCNT15	Bit Count Fifteen	83-1
FB00 - BF15	16 Word Buffer, Bit Zero through Bit Fifteen	83-3
BFEMTY-	Fuffer Empty	83-1, 27-1
BFEMTY	Buffer Empty	83-1, 83-5,27-1, 27-3
BFFUL	Buffer Full	83-1, 83-5, 27-1, 27-3
BFLD-	Buffer Load	83-5
BFLDCNR-	Buffer Load Control Register	83-1, 83-3
BFLDPS-	Buffer Load Pulse	83-3, 83-5
BFLDR	Buffer Load Register	83-1, 83-3
BFPSINH	Buffer Pulse Inhibit	83-1, 83-5
BUFFS	Buffers: Operate during diagnostic mode for 16 Word Transfers	83-5, 27-1
BUSY	Busy	27-1, 27-2
CCGNZR	Cyclic Code Not Zero Read	83-2, 83-5
CCYL, CCYL-	Cyclic Code Cycle	83-2, 83-5
CLR	Clear	27-1
DATA00-DATA15	Data Bit 00 through 15 from the Processor	27-2, 27-1
DATIA	DIA Instruction	27-1
DATIB	DIB Instruction	27-1
DATOA	DOA Instruction	27-1
DATOB	DOB Instruction	27-1
DATOC	DOC Instruction	27-1
DB00 - DB03	Data Bit 00 through Data Bit 03 from the Adapter Card	83-1, 27-2
DB00 - DB15	Data Bit 00 through Data Bit 15 from the Adapter Card	83-2, 83-3, 83-4, 27-1, 27-2
DCHA-	Data Channel Acknowledge	27-3
DCHADG-	Data Channel Acknowledge Delay Gated	27-2, 27-3
DCHBSY	Data Channel Busy	27-2, 27-3
DCHBSY	Data Channel Busy	27-2, 27-3
DCHI	Data Channel In	27-3
DCHIN-	Data Channel In Gated	27-1, 27-2, 27-3
DCHMO-	Data Channel Mode	27-3

*The first two digits refer to the last two digits of the schematic number, third digit refers to sheet number.

TABLE 4-1. SIGNAL DEFINITION AND MNEMONICS (continued)

Mnemonic Term	Signal Definition	Location*
DCHO	Data Channel Out	27-3
DCHR-	Data Channel Request	27-3
DCHPOT-	Data Channel Priority Out	27-3
DFLD	Should be BFLD (error on drawing)	83-3
DIAGM	Diagnostic Mode	27-1, 27-2
DISC FAIL	Time Out and Ready	83-2
DOA	DOA Instruction	27-1
DOCX	DOC Instruction	83-1, 27-1, 27-2
DR00 - DR15	Data Register Zero through Data Register Fifteen	83-2
DRAVL-	Data Register Arrival Generated by DCHIN-	83-5, 27-1
DRCNC	Data Register Count Control	27-1, 27-3
DRFUL	Data Register Full	83-5, 27-3
DRGAT-	Data Register Gate	83-2, 27-1
DSCRDY-	Disc Ready	83-1
DRSET	Data Register Set	83-3, 83-5
DRSETPS	Data Register Set Pulse	83-5, 27-1, 27-3
DRSETBF-	Data Register Set Buffer	83-3, 83-5
DS0 - DS5	Device Select Zero through Five	27-1
E9 - E16	Location Control Count Same as LCCO-LCC11	83-4
ENDER	End Error	83-2, 83-5, 27-1, 27-3
ENDSTR	End Strobe	83-1, 83-5, 27-1, 27-3
EOWD	End of Word	83-1
INIT-	Initiate	83-1, 83-5, 27-1
INIT-A	Initiate A	83-1, 83-3, 83-5
INIT-C	Initiate C	27-1, 27-2, 27-3
INTA	Interrupt	27-1
INTACK-	Interrupt Acknowledge	27-1, 27-2
INTPIN	Interrupt Priority In	27-1
INTPOT	Interrupt Priority Out	27-1
INTR-	Interrupt Received	27-1
IOPLS	I/O Pulse	27-1
IORST	I/O Reset	27-1
LCC0 - LCC11	Location Control Count Zero - Eleven	83-4
LCCA - LCCM	Location Control Count A - M	83-4
LSTWD	Last Word	83-1
MAIN-	Memory Address In	27-1, 27-2
MASET-	Memory Address Set	27-1, 27-2
MSKO-	Mask Out	27-1
PERM ADDRESS	Protected Memory Address	83-1
POR-	Power ON Reset	83-1
PTY	Parity Bit	83-2, 83-5
PTYCYL,		83-2, 83-4
PTYCYL-	Parity Cycle	83-5

*The first two digits refer to the last two digits of the schematic number, third digit refers to sheet number.

TABLE 4-1. SIGNAL DEFINITION AND MNEMONICS (continued)

Mnemonic Term	Signal Definition	Location*
PU	Pull Up	83-2
RD	Read	27-1, 27-3
RDDATA, RDDATA-	Read Data	83-1
RDL, RDL-	Read Latch	83-1, 83-5
RDOP	Read Operation	83-1, 83-5, 27-1 27-2, 27-3
RDSC-	Read Sync F/F	83-1
RDST-	Read Start	27-1
RQENB, RQENB-	Request Enable	27-1, 27-3
RSGOA-	Error on drawing S/B RSGO	83-1
RSGO-	Read Sector Go	83-1, 27-1
RST-	Reset	83-1, 83-4, 83-5, 27-1, 27-2
RWOP	Read/Write Operation	83-1, 83-4
SA10 - SA13	Subsector Address 0 through 3	83-1, 83-4
SALOS-	Subsector Address Load One-Shot	83-1, 83-3, 27-1, 27-2
SARST	Sector Address Reset	83-4
SARSTA	Should be SARST	83-1
SCLK	Sector Clock	83-1, 83-5
SCOPCK	Sector Continue Operation Clock	83-2, 83-5, 27-1, 27-3
SCSYN	Sector Clock Sync	83-1, 83-4
SELB	Select Busy	27-1
SELD	Select Done	27-1
SEQL, SEQL-	Sector Equal	83-1
SEQLEN	Sector Equal Enable	83-1, 83-4
SR00 - SR15	Shift Register Bit Zero - Fifteen	83-3, 83-5
SRCL	Shift Register Clock	83-1, 83-3
SRCLKW	Shift Register Clock Write	83-1, 83-5
SRLD-	Shift Register Load	83-1, 83-3, 83-5
SRLDENW-	Shift Register Load Enable Write	83-1, 83-3
SRCLKR-	Shift Register Clock Read	83-2, 83-5, 83-1
STATIN	Status In	83-2, 27-1, 27-2
STCLD-	Word Transfer Counter Load Used only with a DOC Instruction	27-1, 27-2
STRT	Start	27-1
TA0 - TA8	Track Address Zero - Eight	83-4, 83-5, 83-2
TMERRD-	Timer Error Read	83-1
TMERWR	Timer Error Write	83-1
TSASET	Track/Sector Address Set	83-1, 83-4, 27-1
UACHG-	Unit Address Changing	83-1, 83-4
USEL2	Unit Select Two	83-4
USEL1	Unit Select One	83-4
USEL3	Unit Select Three	83-4

*The first two digits refer to the last two digits of the schematic number, third digit refers to sheet number.

TABLE 4-1. SIGNAL DEFINITION AND MNEMONICS (continued)

Mnemonic Term	Signal Definition	Location*
USEL0-	Unit Select Zero	83-4
WCLK	Write Clock Out	83-1, 83-5
WCLKDI	Write Clock Out Delay	83-1, 83-5
WC0-WC3 WE0-WE3	Word Count Zero - Word Count Three	83-1
WRL, WRL-	Write Latch	83-1, 83-5
WROP	Write Operation	83-1, 83-3, 83-5, 27-1, 27-2, 27-3
WRITE-	Write	83-5, 83-6
WRSC, WRSC-	Write Sync flip-flop	83-1
WRT-	Write to Disc	83-6
WSGO, WSGO-	Write Sector Go	83-1, 27-1
WTST-	Write Start	27-1

*The first two digits refer to the last two digits of the schematic number, third digit refers to sheet number.

4-5 OVERALL SYSTEM THEORY OF OPERATION

The 8011 Disc Memory Controller is normally connected to the Nova Computer I/O bus along with other peripheral devices such as magnetic tape units, paper tape readers, line printers, etc. Each device connected to the I/O bus is assigned a device code (octal) and a mnemonic designation. The controller has device code 20 or 60 with mnemonic DSK. The computer processor selects a device by placing the device code (bits 10 through 15 of the I/O instruction word) on lines DS0 through DS5 during the execution of an I/O instruction. Only the selected device responds to the control signals generated during the instruction.

4-6 DATA-OUT AND DATA-IN TRANSFERS

For data-out transfers, the controller is selected for operation by the DOA and DOB instructions that are issued by the processor. The DATOA and DATOB signals are sent from the processor to the adapter PC board as a result of the instructions. The IOPLS signal sent from the processor to the PC board adapter, PC board causes the selected busy (SELB) signal from the adapter board to the processor to become true.

The DCHP signal is sent from the processor to the adapter board at the start of the data cycle. When the RQENB signal is sent from the processor to the adapter board, the DCHR signal to the processor becomes true.

The address information placed on the data lines as a result of the DOA instruction is sent to the unit, track and sector registers of the controller. The initial address information of the DOB instruction is sent to the core memory address register on the adapter board. The DATOA signal causes the unit, track and sector registers to be loaded, and the DATOB signal causes the core memory address register to be loaded.

The DCHA signal sent by the processor to the adapter PC board causes the DCHMO signal to the processor to go high, indicating a data-out transfer. This also causes the initial address to be read out from the core memory address register to the processor.

The sector address is applied to the sector equal detection circuit on the formatter board where it is compared with the information from the current sector location counter.

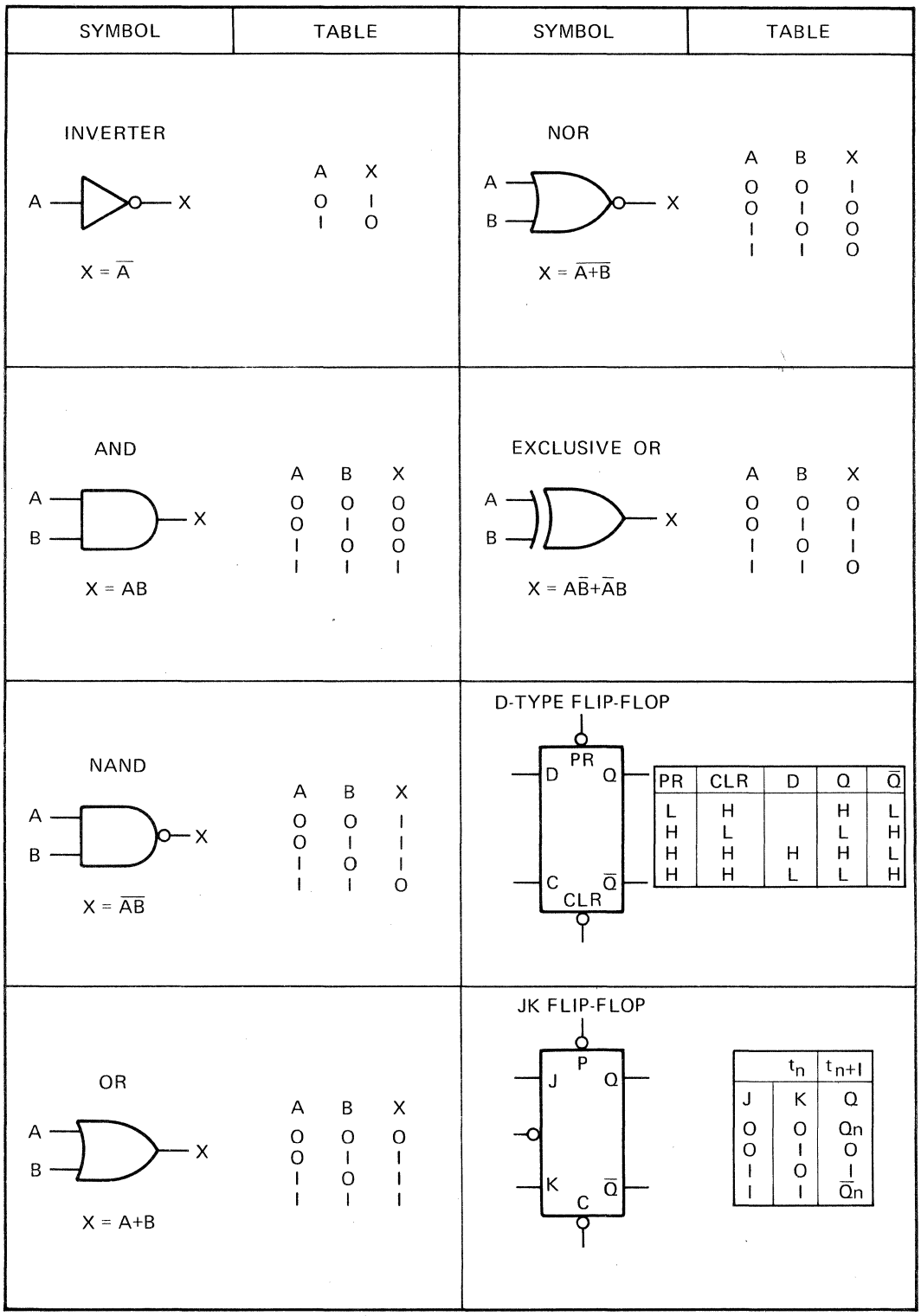


Figure 4-1. Logic Symbols

The data word from the processor is sent through the adapter board to data selectors on the formatter board. It is then transferred through these data selectors to the data register to a 16-word buffer and then to the shift register.

When the sector address applied to the sector equal detection circuit is equal to the sector address on the disc, the data is serially shifted out of the shift register and is written on the disc when the WRITE signal from the formatter board is applied to the disc unit.

At the end of the data-out transfer (256 words) when the last data word has been written, the selected done (SELD) signal from the adapter board to the processor becomes true.

For data-in transfers, the controller is selected for operation and the DOA and DOB instructions are issued by the processor. The STRT signal sent from the processor as a result of one of the instructions is applied to the adapter PC board. This causes the SELB signal to the processor to become true.

The DCHP signal is sent by the processor to the adapter board at the beginning of the data cycle. When the RQENB signal is sent from the processor, the DCHR signal to the processor becomes true. The unit, track and sector address information is loaded into the unit, track and sector registers when the DATOA signal is sent from the processor. The initial address information is loaded into the core memory address register when the DATOB signal is sent from the processor.

The sector address information is applied to the sector equal detection circuit where it is compared with the information from the current location counter. When the addresses are equal, the READ signal to the disc unit becomes true. At approximately 16-bit times later, the first bit of data is read from the disc.

The bits read from the disc are serially shifted into the shift register until a 16-bit word is formed. The data word is then transferred in parallel through the 16-word buffer to the data register through the adapter PC board where it is strobed to the processor when the DATIA signal is sent from the processor to the adapter board.

When the last (256 words) of the data-in transfer has been transferred to the processor, the SELD signal to the processor becomes true.

The preceding paragraphs pertained to sector operation. When subsector operation is used, the word transfer counter is loaded at the start of a data transfer with 12 data bits (04 through 15). These bits define the length of operation in terms of subsectors. A more detailed theory of operation for write and read operations is given in paragraphs 4-57 and 4-58.

4-7 PROGRAM INTERRUPT

When the processor uses a mask to set up the program interrupt, it executes the same sequence as for a data-out transfer, except that it generates MSKI (in place of the DATOA signal) to set up the interrupt disable flags in all devices according to the information on the data lines.

When the controller and the other devices connected to the I/O bus complete an operation, they set their don flag. At the beginning of every memory cycle, the processor generated the request enable (RQENB) signal to allow all devices on the bus to request

program interrupts or channel access. If the done flag of a device is set and its interrupt disable flag is clear, the leading edge of the RQENB pulse is used to set the INT REQ flip-flop to ensure sufficient time for the serial INTP function to be completed before the processor attempts to discover which device has priority. The processor issues INTP IN to a device only if there is no INT REQ flip-flop set in a device closer to the processor on the I/O bus. The closest device that has its INT REQ flip-flop set terminates the INTP signal.

The processor aknowledges an interrupt by generating the INTA signal. If a device receives the INTA signal while it is also receiving the INTP signal and its INT REQ flip-flop is set, it places its device code on DATA 10 through DATA 15 lines to the processor. The processor strobes the data containing the device code into the specified accumulator at the end of the INTA level.

During an interrupt, the processor can also determine which device requires service by sensing the busy or done signals. When the processor is to use the same device again after interrupt, it clears the done signal so that the device does not immediately request an interrupt when the interrupt system is reintiated and its interrupt disable signal is cleared. When the done signal is cleared, it causes the INT REQ flip-flop to be cleared. This disables the INTR signal, preventing the device from requesting an interrupt.

4-8 DATA CHANNEL REQUESTS

The sequence of events that occur during a data channel request are similar to the events that occur during an interrupt request. Each device connected to the I/O bus has a DCH SYNC flip-flop which controls the logic state of its done signal to the processor. Each device has a DCH REQ flip-flop (data channel request flip-flop) and a net for transmitting the serial priority signal to the next device. When a device receives the input DCHP signal (data channel priority) and its DCH REQ flip-flop is clear, it transmits the DCHP signal to the next device. The first device that has its DCH REQ flip-flop set terminates the DCHP signal. When this flip-flop is set, the next RQENB signal from the processor sets the DCH REQ flip-flop in the device. This causes its DCHP signal to the processor to become true. The DCH REQ flip-flop is set on the leading edge of the RQENB signal to ensure sufficient time for the serial DCHP function to be completed.

When a device is waiting for access to the data channel, the processor generates DCHA after the RQENB signal goes false in the final cycle of an instruction. The leading edge of the DCHA signal sets the DCH SEL flip-flop in the nearest device that is requesting service. This device must be receiving the input DCHP signal and have its DCH REQ flip-flop set. The device that has its DCH SEL flip-flop set places the memory address to be used for data channel acess on data lines 1 through 15 to the processor for the duration of the DCHA signal. When the DCHA signal goes false, the processor strobes the address into its memory address register.

When the DCH SEL flip-flop is set in the controller, the DCHMO signal to the processor is enabled. This signal becomes true (low) for a data-in (read) transfer and becomes true (high) for a data-out transfer (write). The DCHA signal that sets the DCH SEL flip-flop also clears the DCH SEL flip-flop in all other devices, thus preventing conflict with other cycles.

The leading edge of the DCHA signal also clears the DCH SYNC flip-flop (done flag). When the next RQENB signal is generated by the processor, the leading edge of the RQENB signal sets request flip-flops in other devices on the I/O bus while it clears

the DCH REQ flip-flop in the device previously having access to the data channel.

When the DCHA signal goes false during a data-in transfer from the controller, the processor generates the DCHI signal and the final instruction cycle is extended while the DCHI signal holds the contents of the data register of the controller on the I/O bus. When the DCHI signal becomes false, the processor strobes the data into its memory buffer and begins the next processor cycle by generating the REQ NB signal which causes the DCHR signal to the processor to go false. During the data-out (write) cycle, the processor stores the data in the addressed memory location.

When the DCHA signal goes false during a data-out transfer to the controller, the processor begins the next cycle by generating the RQENB signal which causes the DCHR signal to become false. During the data-out (write) cycle, the processor retrieves a data word from the addressed memory location and brings it into the memory buffer. The data-out cycle is completed when the processor places the contents of the memory buffer on the data lines to the controller and generates the DCHO signal to load the data word into the controller data register.

4-9 MULTIPLE REQUESTS FOR DATA CHANNEL ACCESS

If the DCH SYNC flip-flop in the device that is being serviced is clear (done signal false) at the leading edge of the RQENB signal in the data channel cycle, the RQENB signal clears the DCH REQ flip-flop in that device. However, if the DCH SYNC flip-flop is already set again (done signal true), the DCH REQ flip-flop stays set. This causes a second data channel access request to be initiated by the device. In either case, the RQENB signal sets the request flip-flops in any other device on the I/O bus that may require service.

If there is a second request from a device, the processor generates a second DCHA signal after completing whatever operations are necessary for the first data channel access. For a data-in transfer, the second DCHA signal is generated when RQENB for the second request becomes false. This occurs preceding the transfer of data. For a data-out transfer, the second DCHA signal is generated following the transfer of data. The second DCHA signal sets the DCH SEL flip-flop in all other devices. The second DCHA signal also initiates the operations necessary to prepare the third transfer of data. Multiple data channel requests occur every other RQENB.

4-10 WRITE OPERATION

A block diagram of a typical write operation is given in figure 4-2. For simplicity, the interrupt signals are not shown. The controller is selected for operation by the processor, and the DOA and DOB instructions and the DOTOA and DATOB signals are generated as a result of the instructions. The IOPLS signal, generated by the processor in accordance with the instruction, is applied to the adapter PC board and sets the WROP flip-flop. This causes the SELB (selected busy) signal to the processor to become true. The DONE flip-flop is reset by the INIT C signal at the same time that the WRIP flip-flop is set. The START signal also becomes true at this time.

The DCHP signal is generated by the processor at the start of the data cycle. When the RQENB signal is generated by the processor, the DCH REQ flip-flop is set, and the DCHR signal to the processor goes low. This also enables the DCH SEL flip-flop. The address information, placed on the data lines as a result of the DOA instruction, is applied through the processor data bus of the adapter board and through the formatter/adapter board common bus to the unit, track and sector registers on the formatter PWBA. The DOB initial address information is applied through the processor data bus to the cor memory address register on the adapter board. The unit, track and sector address information is

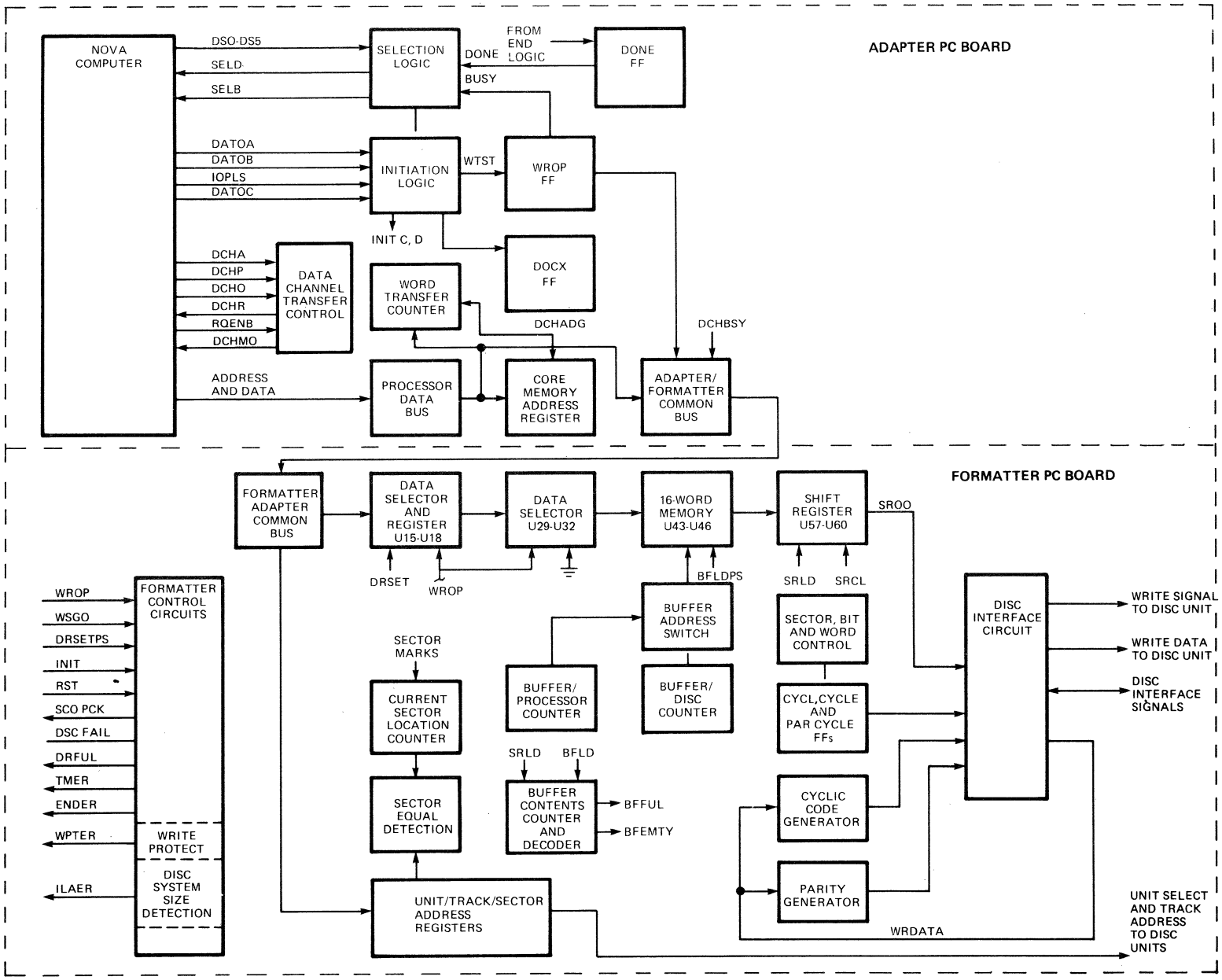


Figure 4-2. Write Operation Block Diagram

loaded into the unit, track and sector registers when the DATOA signal from the processor causes the TSASET signal to become true. The core memory address register is loaded when the DATOB signal from the processor causes the TSASET signal to become true. The core memory address register is loaded when the DATOB signal from the processor causes the MASET signal to become true. The DCHA signal generated by the processor sets the DCH SEL flip-flop. This causes the DCHADG signal to go low (true) and the DCHMO signal to the processor to go high, indicating a data-out (write) operation. The DCHADG signal is applied to the register on the data processor bus that contains the initial address from the core memory address register. This causes the initial address to be read out to the processor. The low DCHADG signal also presets the DCH BSY flip-flop, enabling data transfer.

When the DOC instruction is used for subsector operation, the subsector address is loaded into the subsector address register when the DATOC signal from the processor causes the STCLD signal to go true, presetting the DOCX flip-flop. For this operation, the contents of accumulator bits 4 through 15 are loaded into the word transfer counter. The 12-bit number expresses the length of operation in terms of numbers of subsectors. This number is a number in two's complement. The total number of words transferred is that which is specified by the subsector number.

The unit track addresses are sent to the disc memory units, and the sector n address is applied to the sector equal detection circuit where it is compared with the information from the current location counter.

The data word from the processor is applied to the data selectros and registers U15, U16, U17, and U18 through the processor data bus and the adapter/formatter PWBA common bus. During the write operation, the WROP signal is high and causes a low input to be applied to the WORD SELECT (pin 10) input. The data selectors and registers are quadruple two-input multiplexers each of which select four input DBO data lines from the formatter/adapter common bus when the WORD SELECT input is low. Each of the data selectors and registers is clocked by the inverted DRSET clock pulse which is derived from the DCHO pulse from the processor. When the data selectors and registers are clocked by the inverted DRSET clock pulse, the DBO data is transferred to data selectros U29, U30, U31, and U32.

Data selectros U29, U30 and U32 are quadruple two-line to one-line data selector/multiplexers. Since the STROBE input of all of these data selectors is connected to ground, the high WROP input to the SELECT terminal of each data selector causes its four DBO input signals to be transferred to its output. This applies the DBO data signals to the 16 word read/write memories U43, U44, U45 and U46. The read/write memories store a total of 16 words of 16 bits per word. The address signals are applied to the memories from the buffer/processor access counter through the buffer address switch. Since the MEM terminal of each memory is connected to ground, the BFLDPS signal which goes low for each word transferred during a write operation causes the four bits of DBO data at the input of each memory to be written into the 16 word memory at the address established by the buffer address signals. The words are loaded into the memories until the memories are full. With the buffer full and a sector pulse, the WSGO signal goes low. This selects the buffer disc access counter for operation through the buffer address selector switch. The first word is then read out of the memories and appears at the output in the complement form. This causes the DBO data to be transferred to the 4-bit shift registers U57, U58, U59, and U60. The DBO data is loaded into the shift registers by the low SRLD clock when the SRCL clock pulse goes high. When each word is written into the memories the buffer contents counts up. When each word is read from the memories, the counter counts down. During the write operation, the sector bit and word control logic count the number of bits written and generates control signals.

When the sector address applied to the sector equal detection circuit is equal to the selector address on the disc, the write signal flip-flop is conditioned high at the same time that the SRLD signal goes high. The loading of the first word into shift registers U57 through U60 causes the first bit (SROO) to be applied in the complimentary form to the write data logic in the disc interface circuit. This conditions the WRITE DATA flip-flop in accordance with the logical state of the bit. When the WRITE DATA flip-flop is clocked, the WRITE signal flip-flop is also clocked causing the WRITE signal to the disc memory unit to go low. The bit then appears on the write data line to the disc memory unit where it is written on the disc. Timing for the transfer to the write data line is derived from the WRITE CLOCK OUT and SECTOR CLOCK pulses from the disc memory unit.

With each positive pulse to the SRCL input, the data is shifted serially from shift register U60 toward SROO of shift register U57 until all of the 16 bits have been written on the disc. The entire process is repeated using the buffer/disc access counter to read words from the memories and the buffer/processor counter to write words into the memories until one sector (256 words of data) has been written. If the DOC instruction is used, the number of subsectors written is specified by the instruction.

At the beginning of each data channel cycle, the processor issues a DCHA pulse to the adapter PC board. The DCHADG pulses, that clock the word transfer counter, are generated by the DCHA pulses during the write operation. When each word is transferred from the processor, the counter is clocked in the count-up direction. If subsector operation is not used, the counter is programmed to count 256 words (one sector). When 256 words have been transferred, the END flip-flop is set on the adapter board. The END signal is ANDed with BFEMTY signal from the buffer contents counter and generate the ENDWEN signal that is ANDed with the WROP signal and ENDSTR one-shot when it is triggered. When the ENDSTR one-shot times out, it causes a low to high transition at the clock input of the done flip-flop. When the flip-flop is set, the selected done (SELD) signal to the processor goes low (true) and the select busy (SELB) signal goes high (false).

When subsector operation is used, accumulator bits 4 through 15 that are loaded into the word transfer counter determines the length of operation in terms of subsectors.

The DCHADG pulses, that clock the word transfer counter, also clock the core memory address counter in the upward direction. The contents of this counter can be read out to the processor as means of checking the number of words transferred or for diagnostic purposes.

At the end of each subsector, a 16-bit cyclic code word and odd parity bit are generated by the formatter PC board. The 16-bit cyclic code word is generated by a cycle code generator and shifted serially to the data interface circuit. The bits are gated to condition the WRITE DATA flip-flop (WRITE DATA signal to the disc memory unit) by the setting of the CCYL flip-flop that is set after the last word counter generates the LSTWD signal. The odd parity bit is generated by a parity bit generator and is gated to condition the WRITE DATA flip-flop when the PTYCYL flip-flop is set after the 16th bit of the cyclic code word.

4-11 ERRORS IN WRITE MODE

Write Error. When a write operation is initiated by the processor and the selected track-sector is write protected, the ENDER signal goes low (true) and the WPTER flip-flop is set. The ENDER signal sets the done flip-flop, causing the SELD (selected done) signal to the processor to go low (true). This causes the SELB (selected busy) signal to the processor to go high (false), and the INTR (interrupt request) signal to go low (true) if the INT DSB (interrupt disable) flip-flop is not set. The WPTER and WPTER- signals are applied to

the error register on the formatter/adapter PC board common bus. This sets bit 15 and error bit 11 to a logical 1.

No Such Disc. When the disc or track selected by the processor is not available on the system, the ILAER flip-flop is set, and the ENDER signal goes low (true). The ENDER signal sets the DONE flip-flop, cuasing the SELD signal to the processor to go low (true) and the SELB signal to go high (false). The true ENDER signal also causes the INTR signal to go low if the INT DSB flip-flop is not set. The ILAER and ILAER- signals are applied to the error register on the formatter/adapter board common bus. This sets bit 15 and error bit 13 to a logical 1.

Disc Fail. If the disc becomes not ready or the system is hung during the write operation, the DSC FAIL flip-flop is set. The ENDER signal goes low (true) if the system is hung. The ENDER signal sets the DONE flip-flop, cuasing the SELD signal to the processor to go low and the SELB signal to go high. The true ENDER signal also causes the INTR signal to go low (true) if the INT DSB flip-flop is not set. The DISC FAIL and DSC FAIL signals are applied to the error register formatter/adapter PWBA common bus. This sets bit 15 and the 10 error bits to a logical 1.

Data Late. When the data channel fails to respond in time to a request for access, the TMER flip-flop is set. The TMER and TMER signals are applied to the error register on the formatter/adapter board common bus. This sets bit 15 and error bit 12 to a logical 1.

The contents of the error register is read when the processor issues a DIA instruction to read the status of the disc memory system.

4-12 READ OPERATION

A block diagram of a typical read operation is given in figure 4-3. For the sake of simplicity, the interrupt signals are not shown. The 8010 Disc Memory Controller is selected for operation by the processor as described in paragraph 4-3. There are three types of read operations. These consist of read from a disc memory unit, read the status of the controller, and read the contents of the core memory address register. The theory of operation of these three types of read operations is described in paragraphs that follow.

4-13 Read From Disc Memory Unit

The DOA and DOB instructions are issued by the processor, and the STRT signal is generated as a result of one of the instructions and applied to the 8010 adapter. This sets the RDOP flip-flop while causing the START and INIT C and INIT D signals to go low. The INIT C signal resets the DONE flip-flop. The setting of the RDOP flip-flop causes the SELB signal to the processor to go low (true).

The unit, track and sector address information is loaded into the unit, track and sector registers when the DATOA signal from the processor is applied to the Nova adapter PWBA and causes the TSASET signal to go low. The core memory address register is loaded when the DATOB signal from the processor causes the MASET signal to go low.

When subsector operation is used, the subsector address is loaded into the subsector address register when the DATOC signal from the processor causes the STCLD signal to go low, presetting the DOCX flip-flop. The low STCLD signal also loads bits 4 through 15 into the word transfer counter. The 12-bit number expresses the length of the operation in terms of subsectors.

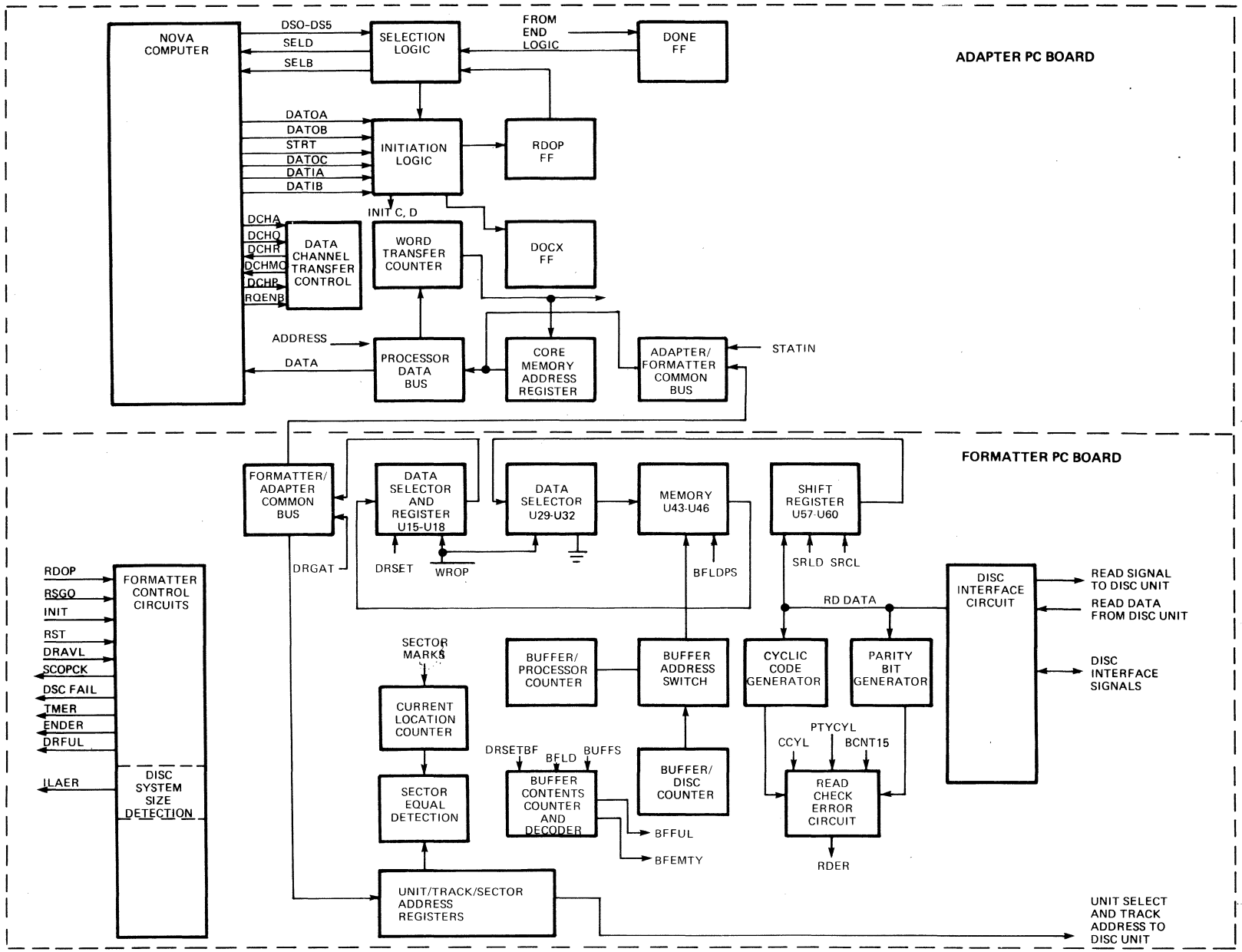


Figure 4-3. Read Operation Block Diagram

The unit select and track address information is sent to the disc memory units, and the sector address information is applied to the sector equal detection circuit where it is compared with the information from the current location counter. When the addresses are equal, the READ signal flip-flop is set and the READ signal to the disc memory unit goes low. At approximately 16 bit times later, the first bit of data is read from the disc.

The first bit of data is applied to the four-bit shift register U60. During the shift operation, the SRLD signal is held high and the first bit of data is entered into U60 when the SRCL clock pulse occurs. The serial shifting process from U57 to U57 is repeated with each clock pulse until shift registers U57 through U60 contain the first data word (16 bits) read from the disc.

During the read operation, the WROP signal is low producing a low input at the SELECT inputs of U29 through U32. This selects the SR data input lines from shift registers U57 through U60. Since the STROBE input of U29 through U32 is grounded, the SR data is transferred in parallel through data selectors U29 through U32 to the input of memories U43 through U46.

Since the MEM input of memories U43 through U46 is grounded and the BFKDR signal goes low when 16 bits are in the shift register, the low signal applied to the WRITE ENABLE input of the memories causes the SR read data to be loaded into the memories since the address is applied from the buffer/disc access counter through the selector switch. When the BFLDR pulse goes high, the buffer disc access counter is advanced, after a delay, to the next higher address.

After the first word is written in the memories, through multiplexers U29 through U32, the buffer/processor access counter is selected and reads the complement of the word from the memory. This applies the word to data selectors U15 through U18. After a delay the buffer/processor access counter is advanced when the first DRSETBF low pulse goes high.

During the read operation the WROP signal is low and causes a high input at the WORD SELECT input of U15 through U18. This selects the BF00 through BF15 inputs from memories U43 through U46. The data is clocked to the outputs of U15 through U18 DRSET pulse that is derived from the first DRSETBF pulse. This pulse is generated as a result of read, buffer registers are empty, and data register not full. The DRSETBF pulses that follow are generated as a result of the data register being emptied by the DCHI signals from the processor. This is where the RQENB, DCHR, DCHPIN and DCHMO should be. If the first DCHI signal does not arrive immediately, loading of the memories still continues. When a word is loaded into the memories, the buffer contents counter counts down. During the read operation, the sector bit and word control logic count the number of bits read and generate control signals.

The outputs from U15 through U18 are applied to the data register on the formatter/adapter PWBA common bus. During the read operation, the DRGAT signal goes low when the RDOP flip-flop is set and DATIA signal is applied from the processor. The low DRGAT signal strobes the data word through the register to the formatter/adapter board common bus. The data word passes through the formatter/adapter PWBA common bus to the data register on the processor data bus. The low DCHIN signal derived from the DCHI signal from the processor strobes the data word through the register to the processor.

The entire read process is repeated for each data word cycle code word and parity bit read from the disc. At the end of each subsector the cyclic code word and the parity bit are read and a read error check is performed. During the read operation, the core memory

address register counter and the word transfer counter are clocked by the DCHADG pulses that are derived from the DCHA pulse from the processor. At the beginning of each data channel cycle, the processor generates at DCHA pulse and applies it to the data channel transfer control circuit on the adapter board. When the length of operation is in terms of sectors, the core memory address register counter provides the count for setting the END flip-flop. The word transfer counter is advanced with each DCHA pulse until 256 words have been transferred. If the BFEMTY signal from the buffer contents counter is high when the 256 count has been reached, the END signal flip-flop is set through its preset input. The END signal is ANDed with the RDOP and DRCNC signals that are caused to be derived from the processor by DCHI signal. When the DCHI signal goes high, the resultant signal sets the DONE flip-flop, and the SELD signal to the processor then goes low.

4-14 ERRORS IN READ MODE

No Such Disc. When the disc or track selected by the processor is not available on the controller, bit 13 is set for a logical 1, SELD signal to the processor goes low, SELB signal to the processor goes high, and an interrupt request is generated by the formatter/controller logic boards in the same manner as for No Such Disc error during a write operation (paragraph 4-11).

Disc Fail. If the disc becomes not ready or the system is hung during a read operation, the DSK FAIL flip-flop is set. The DSK FAIL and DSK FAIL- signals are applied to the error register on the formatter/adapter board common bus. This sets a logical 1 bit in bit 10 of the error bits and also sets a logical 1 in bit 15. The ENDER signal goes low if the system is hung. The ENDER signal sets the DONE flip-flop causing the SELD signal to the processor to go low and the SELB signal to go high. The true ENDER signal also causes the INTR signal to go low if the INT DSB flip-flop is not set.

Data Late. When the data channel fails to respond in time to a request for access during a read operation, the TMER flip-flop is set. The TMER and TMER- signals are applied to the error register on the formatter/adapter board common bus. This sets a bit 15 and error bit 12 to a logical 1.

Data Error. If the cyclic code word or parity bit read from the disc differs from the code word and parity bit computed by the read check circuitry for the data in the subsector, the RDER flip-flop is set. The RDER and RDER- signals are applied to the error register on the formatter/adapter board common bus. This sets bit 15 and error bit 14 to a logical 1.

4-15 Read Status of Disc Memory System

The error register on the formatter/controller board common bus contains the errors (if any) from the previous operation. The six errors that the register may contain are described in paragraphs 4-11 and 4-14.

To read the status of the disc memory system, the processor issues a DIA instruction. The DATIA signal applied to the adapter PC board as a result of the instruction causes the STATIN signal to go high (true). The STATIN pulse strobes the contents of the error register through the formatter/adapter board common bus to the processor data bus. On the processor data bus, the inverted STATIN pulse strobes the error bits to the processor.

4-16 Read Contents of Core Memory Address Register

One of the data registers on the processor data bus contains the inputs from the core memory address register on the adapter PC board. The core memory address register bits from the processor. During a write or read operation, the counter is advanced by a DCHADG pulse at the beginning of each data cycle.

To read the contents of the core memory address register, the processor issues a DIB instruction. The DATIB signal, generated by the processor as a result of the instruction, is applied to the adapter board and causes the MAIN signal to go low. The MAIN signal is applied to the register on the data processor bus that contains the inputs from the core memory address register. This causes the contents of the register to be read out to the processor. If the system is busy when the DIB instruction is issued, the contents of the core memory address register is presented as logical 0's.

4-17 DIAGNOSTIC MODE

In the diagnostic mode of operation, the processor issues a DOB instruction containing a logical 1 in accumulator bit 0. This places the controller in the diagnostic mode. The processor then transfers 16 words, using the memories U43 through U46 as described in the write operation in paragraph 4-10. During the diagnostic mode of operation the buffer/processor access counter supplies addresses to the memories through the buffer address switch. The 16 words are then read back to the processor through the data selectors and registers U15 through U18 as described in the read operation of paragraph 4-12. To read the 16 words out of the memories, the write enable input is held high and since the memory enable signal is grounded, the words are read out of the memories when the address signals are applied from the buffer address switch.

4-18 ADAPTER BOARD DETAILED CIRCUIT DESCRIPTION

The following paragraphs describe the logic circuits whithin the adapter PC board of the controller. The information contained in the descriptions is taken from the schematic diagram 1940027, sheets 1 through 3.

4-19 INITIATION AND DONE CONTROL (1940027, SHEET 1)

The initiation and done control logic contains the logic for selecting the 8010 Disc Memory System for operation and the logic for the various initiation control signals from the processor. It also contains the WROP and DROP flip-flops that control the SELD- signal to the processor, the DONE flip-flop that controls the loading of the word transfer counter and subsector address register during subsector operation.

4-20 Device Selection

The DS0- through DS5- signals are applied from the processor to select the 8010 Disc Memory System for operation. To select the disc memory system, DS0- must be high, DS1 must be low, and DS2 through DS5- must be high. This code (010 000) corresponds to octal 20, the code for the disc memory system. With this code applied from the processor, the output from U41-13 goes high. This high output is applied to U15-3 and U16-13, enabling the DATIA and CLR signal gates. This output is also applied to U27-9. If neither the WROP or RDOP flip-flop is set, the input to U27-10 is high. This causes the output from U27-8 to go high. This high output is applied to U3-3, U17-5, U17-13, U17-11, U16-11 and U16-3. This enables the DATOA, DATOB, DATOC, IOPLS, STRT and SATIB signal gates.

The high output from U41-13 is also applied to U5-13 and U5-5, enabling the SELB- and SELD- signal gates.

4-21 Initiation Logic

The IOPLS signal (write operation) applied to U17-9 or the STRT signal (read operation) applied to U16-9 causes the INIT signal at U53-8 to go low, the INIT D signal at U40-12 to go high and the INIT C- signal at U48-8 to go low. The inverted INIT C signal at U48-8 resets the DONE flip-flop at U56-13 causing the SELD- signal to the processor to go high (false). The IOPLS or STRT signal also causes the START signal at U4-11 to go high. The STRT signal generates the RDST- signal that sets the read latch U55-8 and U42-10 signal circuit during a diagnostic read operation.

On the trailing edge of the IOPLS or STRT pulse, the WROP or RDOP flip-flop is set. This causes the SELB signal at U5-11 to go low (true). This signal is applied to the processor to indicate selected busy (busy flag).

During a write operation, the DATOA signal is applied to U3-5. The output at U3-6 goes low, causing the TSASET signal of driver U19-4 to go low. The TSASET- signal is used to load the unit, track and sector address registers with the address contained in the DOA instruction.

During a write operation, the DATOB signal is applied to U17-4. The output MASET- signal at U17-6 goes low. The MASET- signal is used to load the core memory address register with a starting core address contained in the DOB instruction.

When subsector operation is used, the DATOC signal is applied to U17-2 and the STCLD output at U17-12 goes low. The low STCLD output from U17-12 presets the DOCX flip-flop and the DOCXA signal at driver U22-2 goes high. The low output from U17-12 is the STCLD- signal that is applied to the word transfer counter to load bits 4 through 15 of the DOC instruction into the counter (specifying the length of operation in terms of sub-sectors). The DOCX signal at U56 is used to apply the subsector address register. The DOCX- signal and the START signal are ANDed at U59-11 and used to load the subsector address into the register.

When the status of the disc memory system is ready, the DATIA signal is applied as a result of the DIA instruction to U15-5. The output at U15-6 goes high, causing the STATIN signal at driver U19-2 to go high. The STATIN- signal strobes the contents of the error register on the formatter/adapter common bus to the processor data bus where the STATIN- signal strobes the error data to the processor.

When bits 8 and 9 (F) of the instruction contain a logical 1 (clear function) the signal is applied to U16-1. This causes the clear output at U16-12, and U27-3 to go low. This generates the INIT- signal at U53-8, the INIT-D signal at U40-12 and the INIT-C signal at U48-8. This clears the RDOP, WROP, DOCX, DONE, DCM, REQ and all other flip-flops that are cleared by the INIT signals. This also causes the SELB- signal to the processor to go false (high).

When the IORST signal is generated as a result of the instruction by the processor, or when the console RESET switch is pressed to clear all control flip-flops in all interfaces connected to the I/O bus, or at power turn on, the input to U4-9 goes high. The output from U4-8 goes low, generating the RST- signal. This also causes the output from U27-3 to go low, generating the INIT-, INIT-D and INIT-C signals. This resets all control flip-flops.

4-22 Done Control

The DONE flip-flop U56 is set at the end of a write operation or at the end of a read operation, and when a write error (write protect) occurs. No such disc error signal or disc fail error signal occurs during an operation.

At the end of a write operation, the END flip-flop is set on the Nova adapter PWBA. This causes the input to U28-1 to go high. If the BFEMTY signal from the buffer contents counter is high (memory buffer empty), the output from U28-3 goes low, causing a high input at U21-2. Since the WROP signal is high during the write operation, the input to U21-1 is high. If the ENSTR one-shot U64 has been triggered at the end of the parity cycle, the input to U21-13 goes high and the output at U21-12 goes low, enabling the DONE flip-flop input at U56-11. When the ENSTR one-shot times out, the transition from low to high at U56-11 sets the DONE flip-flop.

At the end of a read operation, the END flip-flop is set on the Nova adapter PWBA causing the input to U57-2 to go high. Since the RDOP signal is high during a read operation, the input to U57-1 is high. The DRCNC signal at U57-13 is derived from the DCHI signal from the processor. This causes the output from U57-12 to go low enabling the DONE flip-flop with a low input at its clock input U56-11. When the DCHI signal from the processor goes low (false), the transition from low to high at U56-11 sets the DONE flip-flop.

If a write protect error, no such disc error, or disc fail error occurs during an operation, the ENDER- signal at U15-10 goes low and then goes high, causing a low to high transition at the clock input U56-11 of the DONE flip-flop. This sets the DONE flip-flop.

During a diagnostic write operation, the WROP signal at U42-2 is low and the DIAGM- signal at U43-3 is low. This causes a high output from U42-1 that is applied to U55-4. When the BFFUL signal at U55-5 from the buffer condition decoder goes high at the count of 16, the output from U55-6 goes low, presetting the DONE flip-flop.

4-23 WRITE AND READ SECTOR GO LOGIC (1940027, SHEET 1)

The write sector go logic generates the WSGO- signal at the start of a write operation, and the read sector go logic generates the RSGO- signal at the start of a read operation.

The BUFFS signal to the buffer contents counter is set by a latch at the start of a diagnostic read operation, so that it programs the buffer contents counter properly for the countdown sequence.

4-24 Write Sector Go Logic

When the DIAGM signal from the core memory address register is low (not diagnostic mode) and the BFFUL- signal from the buffer condition decoder is low (memory buffer full), the inputs to U42-12 and U42-11 are low. This causes the output from U42-13 to go high. This conditions write sector go flip-flop U49 with a high input at U49-12. If the read sector go flip-flop U49 is not set, the input to U44-5 is low, and since the write sector go flip-flop is reset, the input to U44-6 is also low. This causes the output at U44-4 to go high. When the SCOS (sector clock one-shot) is triggered by the SCSYN- pulse, the SCOPCK signal goes high. The high SCOPCK signal is applied to U57-10 and also causes the write sector go flip-flop U49 to be clocked through gate U20. This causes the WSGO-

signal at U57-8 to go low (true). When the SCOS one-shot times out, the WSGO- signal at U57-8 goes high (false). The write sector go flip-flop is reset by the INIT signal at U41-8 or by the high signal at U41-9 at the end of the write operation when the END and BFEMTY signals are both high. When doing more than one write, the first WSGO is generated by WRSC (low), RDSC (low) and SCSYN (low) which generate SCOS (low); which, in turn, generates SCOPCK (high) which generates WSGO (low). Subsequent WSGO signals are generated by LSTWD (high) followed by CCYL (high), PTYCYL (high), ENDSTR (low), and SCOPCK (high) which generates WSGO (low).

4-25 Read Sector Go Logic

When the RDOP signal at U4-1 (B3) is high and the BFEMTY signal from the buffer contents counter is high, the output from U4-3 goes low. This low output is applied to U42-5. If the DIAGM signal from the core memory address register is low, the read sector go flip-flop U49 is conditioned with a high input at U49-2. If the write sector go flip-flop U49 and the read sector go flip-flop U49 are both reset, the output from U44-4 goes high. When the SCOS one-shot in the end control circuit is triggered by the SCSYN- pulse, the SCOPCK signal goes high. The high SCOPCK signal is applied to U57-4 and also causes the read sector go flip-flop to be clocked through gate U20. This causes the RSGO- signal at U57-6 to go low (true). When the SCOS one-shot times out, the RSGO signal goes high (false). The read sector go flip-flop is reset by the low signal at U20-5 at the end of the read operation. Subsequent RSGO signals are generated by LSTWD (high) followed by CCYL (high), PTYCYL (high), ENDSTR (low), and SCOPCK (high) which generates RSGO.

At the start of a diagnostic read operation, the STRT signal from the processor causes the RDST- signal at U55-10 to go low. This sets the latch composed of the two low-true NOR gates U55. This sets the input at U42-8 low. Since the input at U42-9 is low, the BUFFS signal at U42-10 goes high. This programs the buffer contents counter properly for the diagnostic read operation. During all other operations, the BUFFS signal is held low.

4-26 INTERRUPT CONTROL (1940027, SHEET 1)

The Interrupt control logic contains the interrupt mask flip-flop that allows the processor to set up priorities for the program interrupt and the INT REQ internal request flip-flop that generates the INTR- signal to the processor to request a program interrupt or channel access.

4-27 Interrupt Mask

When the processor issues a mask out instruction to set up priorities for the program interrupt, bit 9 of the accumulator bits is used as the mask bit for the 8010 Disc Controller. If the disc controller is not one of the devices having priority for the interrupt, the D09 signal applied to U62-2 of the INT MSK flip-flop is high. When the MSKO- signal is applied from the processor, the output from U2-6 goes high. This sets the INT MSK flip-flop U62, causing the input to U1-13 to go low. This disables the INTR- signal to the processor, since the INT REQ flip-flop U62-9 cannot be set by the RQENB clock pulse.

4-28 Interrupt Request

If the controller is one of the devices having priority for the interrupt, the INT MSK flip-flop is not set. This causes the input of U1-13 to be high. If the DONE flip-flop U56 is set, the input to U1-12 is also high. This conditions the INT REQ flip-flop U62 with a high input at U62-12. When the next RQENB signal is sent from the processor, the INT

REQ flip-flop is set on the leading edge of the RQENB pulse.

The INTPIN- signal from the processor is applied to U7-9. This causes a high input at U8-5. If the INT REQ flip-flop U62 is not set, the INPOT- signal at U8-6 goes high. This signal is sent to the next device connected on the I/O bus. If the INT REQ flip-flop is set, the INPOT signal at U8-6 goes low disabling priority to all other units on the I/O bus. When the INTA (interrupt acknowledge) signal is applied from the processor, the output from U1-8 goes high; this causes a high input at U53-5. If the INTPIN signal is high at U53-4 and the INT REQ flip-flop is set, the INTACK signal at U53-6 goes low. The INTACK- signal is applied to data lines DATA11 to the processor. Since data lines DATA10 and DATA12 through DATA15 are logical 1's, the device code of the disc memory system, 010,000 is sent to the processor. This identifies the disc memory system as the device requesting the interrupt.

4-29 CORE MEMORY ADDRESS REGISTER AND WORD TRANSFER COUNTER (1940027, Sheet 2)

The core memory address register is a 16-bit binary counter that is loaded with the initial starting address for the operation. During the operation, the counter is advanced by DCHADG- pulses when each word is transferred. The contents of the register are read out to the processor at the start of an operation and can be read out at other times as a means of checking the number of words transferred, or for diagnostic purposes.

4-30 Core Memory Address Register

When the DOB instruction is issued by the processor, accumulator bits 0 through 15 (D100 through D115) are applied to the core memory address register. These bits contain the initial starting address for the operation. When the DATOB signal is generated by the processor, the MASET signal goes low. This low signal is applied to pin 1 of each register and loads the 4 bits associated with that register into the register. Since registers U36 through U39 are programmable, the outputs from the registers will assume the state of the input signals. When the DCHADG- pulse is generated at the beginning of each data cycle, the input to U58-11 goes low and the output at U58-10 goes high, clocking register U38. The four registers, U36 through U38 are connected as a ripple-through binary counter. A count of 0 to 32, 768 words can be transferred.

The outputs from the core memory address register are connected to a register on the processor data bus and are read out to the processor at the beginning of an operation and incremented when the DCHADG- pluse occurs. They are also read out to the processor when the processor issues a DIB instruction. If the system is busy when the DIB instruction is issued, the contents of the core memory address register is presented as logical 0's. The setting of the most significant bit in the core memory address register sets the controller in a diagnostic mode of operation. In the diagnostic mode the 16-word buffer is read. There are no data transfers to and from the disc during the diagnostic mode.

The core memory address register is cleared by the RST- signal applied to U27-12, 13 when the IORST pulse is generated by the processor.

4-31 Word Transfer Counter

When subsector operation is used, a DOC instruction is issued by the processor. The starting subsector address is contained in accumulator bits 0 through 3. The length of operation expressed in terms of subsectors is contained in accumulator bits 4 through 15.

At the start of the operation, the START signal at U59-3 goes high when the STRT or IPOL signal is sent from the processor. This clears counters U43, U44, U46 and U48. When the DATOC signal is sent from the processor, the STCLD- signal goes low (true), presetting the DOCX flip-flop. The STCLD- signal is also applied to pin 11 of counters U44, U46 and U48. This loads data bits D04 through D15 into the counters, thereby programming the counters for the specified length of operation. The low STCLD- signal is also applied to U1-4 and causes the SALOS- signal at U1-6 to go low (true). This loads accumulator bits 0 through 3 into the subsector address register on the formatter PC board.

The programming of counters U44, U46, and U48 with bits D04 through D15 allows multiple 1 to 4096 subsectors to be operated. When bits D04 through D15 are low (accumulator bits logical 0), the length of the operation is 4096 subsectors. Since there are 16 words per subsector, 65, 536 words can be transferred.

During the operation, counter U43 is advanced with each DCHADG- pulse at the beginning of each data cycle. Since counters U43, U44, and U46 are cascaded in a ripple-through connection, the output at U48-12 goes high at the count programmed by D04 through D15. This clocks the END flip-flop U60 setting the END signal at U60-5 high.

When sector operation is used, the DOC instruction is not executed, and the word transfer counter then counts 256 words (one sector). At this count, the END flip-flop is clocked, setting the END signal at U60-5 high.

4-32 PROCESSOR DATA BUS (1940027, SHEET 2)

The processor data bus connects the adapter PC board to the computer processor. It receives the D00 through D15 signals from the processor, and according to the contents of the signals, routes them to the core memory address register; the unit, track and sector registers; the word transfer counter and subsector register; or the data selectors and registers. It also contains a register that stores the contents of the core memory address register. In addition, it contains a buffer register for the data read from the disc or the data read from the error register on the formatter/adapter common bus.

The D00 through D15 signals from the processor are each applied to an inverter (U10 through U13). When the data lines contain the disc, track and sector address given in the DOA instruction, the address information is applied through the adapter/formatter common bus to the unit, track and sector registers on the formatter PC board.

When the data lines contain the initial address information of the DOB instruction, the address information from the inverters is applied to the registers of the core memory address register.

When the data lines contain the information of the DOC instruction, the inverted D04 through D15 signals are applied to the word transfer counter, and the D00 through D03 signals are applied through the adapter/formatter common bus to the subsector register on the formatter PC board.

When the data lines contain the data to be written, the inverted data from the inverters is applied through the adapter/formatter common bus to the data selectors and registers on the formatter PC board.

The register for the outputs of the core memory address register is composed of NAND gates U23 through U26. At the start of an operation after the core memory address register has been loaded with the initial address, the first DCHADG- pulse is applied to

U14-1. This strobes the initial address from the core memory address register through the NAND gates to the data lines to the processor. When a DIB instruction is issued by the processor, the MAIN- signal at U14-2 goes low. This strobes the present contents of the core memory address through the NAND gates to the data lines to the processor.

When data is read from the disc or when the status of the disc memory system is read, the buffer composed of NAND gates U10 through U13 is used. When the DCHIN- signal at U20-9 goes low, the data is strobed through the NAND gates to the data lines in the processor.

When the status of the disc memory system is read, a DIA instruction is issued by the processor, and the contents of the error register (bits 10 through 15) on the formatter/adapter common bus is strobed by the STATIN signal through the formatter/adapter common bus to NAND gates U10 through U13. The low STATIN- signal at U20-10 strobes the contents of the error register through the NAND gates to the data lines to the processor.

The INTACK- signal at U6-11 goes low when the disc memory system has requested an interrupt and has priority. This causes a logical 1 bit on line DATA11- to the processor. Since data line D10- and data lines D12- through D15- are logical 1's (high), the code 010,000 (octal 20) identifies the disc memory system as the device requesting the interrupt.

4-33 ADAPTER/FORMATTER COMMON BUS (1940027, SHEET 2)

The adapter/formatter common bus contains a buffer that receives the D00 through D15 signals from the processor data bus and a logic circuit that provides the enabling signal for transferring the signals to the formatter/adapter common bus. The adapter/formatter common bus also receives the data read from the disc and the data read from the error register on the formatter/adapter common bus. It inverts this data and applies it to the buffer register on the processor data bus.

When the data is read from the disc, the read signals from the data selectors and registers are strobed through the fromatter/adapter common bus to the DB00- through DB15- inputs. Each input signal is terminated by resistive networks and applied to an inverter (U30, U31, U33 and U35). The inverted output signals from the inverters are applied to U10 through U13 and are strobed to the data lines to the processor by DCHIN.

When the status of the disc memory is read, the contents of the error register (bits 10 through 15, DB10- through DB15-) is strobed from the formatter/adapter common bus and processor data bus to the processor. This route is the same as for the read data signals from the formatter/adapter common bus.

4-34 DATA CHANNEL TRANSFER CONTROL (1940027, SHEET 2)

The data channel transfer control logic contains the DCH REQ, DCH SEL and DCH BSY flip-flops. The DCH REQ flip-flops controls the DCHR (data channel request) and DCHPOT (data channel priority out) output signals, and the DCH SEL flip-flop controls the DHADG transfer pulses and DCHMO (data channel mode) output signal. The DCH BSY flip-flop controls the DCH BSY (data channel busy) output signal and the gating of the input DCHI (data channel in) and DCHO (data channel out) signals that generate the DCHI- and DRSETPS signals respectively.

After the WROP (write operation) or RDOP (read operation), the data channel transfer control flip-flop is set and the input to U9-4 or U9-1 goes high. For a write

operation, the DRFUL- signal at U9-5 is set high, and for a read operation the DRFUL signal at U9-2 is set high. This causes the input to U15-1 to go high. Since the DCH BSY flip-flop is reset at this time and the END- signal is high, the inputs to U15-2 and U15-13 are high. This causes the output from U15-12 to go high, conditioning the DCH REQ flip-flop U61 with a high input at U61-2. When the RQENB- signal is applied from the processor at the beginning of the memory cycle, the output from U9-8 goes high. This sets the DCH REQ flip-flop U61-5, causing the CDHR- signal to the processor to go low (true).

The DCHPIN- signal from the processor causes a high input at U5-10. If the DCH REQ flip-flop is not set, the DCHPOT- signal at U5-8 goes low (true). This signal is transmitted to the next device connected on the computer I/O bus. If the DCH REQ flip-flop is set, the DCHPOT- signal remains false giving the controller priority. The output of U59-6 goes high, conditioning the DCH SEL flip-flop U61 with a high input at U61-12 and enabling AND gate U59 with a high input at U59-10.

When the DCHA- signal is applied from the processor at the beginning of the data channel cycle, the output from U2-8 goes high. This sets the DCH SEL flip-flop U61-9 and causes the DCADG- signal at U8-3 to go low. This signal is sent to the processor to indicate a data-out transfer. For a read operation, the RD signal at U8-1 is high, causing the DCHMO- signal to go low. This signal is sent to the processor to indicate a data-in transfer. The low DCHADG- pulse at U58-10 loads the core memory address on the processor data bus into the core memory address register. This causes the initial address to be read out to the processor. The low DCHADG- pulse is also applied to the preset input of U60-10 of the DCH BSY flip-flop U60. This sets U60-9, enabling U21-11 and U21-3. This also causes the DCH BSY signal to go high. This signal is applied to the data register logic on the adapter/formatter common bus. During a write operation this enables the register to transfer data from the processor to the data selectors and registers on the formatter PC board.

During a write operation, the DCHO signal applied from the processor causes the output from U21-6 to go low. This causes the DRSETPS- signal to go low (true). The DRSETPS- signal is applied to the buffer and data register transfer control logic on the formatter PWBA and generates the DRSET pulse that clocks the data into the data selectors and registers. When the DCHO signal goes low (false), the DCH BSY flip-flop is reset. Then the DCHA- signal for the next data word is applied from the processor and the DCHADG- signal presets the DCH BSY flip-flop. This enables gates U21 again for the next DCHO signal from the processor.

During a read operation, the DCHI signal applied from the processor causes the output from U21-8 to go low. This causes the DCHIN signal to go low (ture). The DCHIN- signal becomes the DRAVL- signal when it is applied through the adapter/formatter interface. The DRAVL- signal is applied to the buffer and data register transfer control logic on the formatter and generates the DRSET pulse that clocks the read data from the memories into the data selectors and registers. When the DCHA- signal goes low (false), the DCH BSY flip-flop is reset. When the DCHA- signal for the next data word is applied from the processor, the DCHADG- signal presets the DCH BSY flip-flop. This enables gates U21 again for the next DCHI signal from the processor.

4-35 FORMATTER BOARD DETAILED CIRCUIT DESCRIPTION

The following paragraphs describe the logic circuits within the formatter PC board of the controller. The information contained in the descriptions is taken from the schematic diagram 1940083, sheets 1 through 6.

4-36 POWER ON RESET (1940083, SHEET 1)

When +5 volts are applied to the formatter board during power turn-on the emitter-base circuit of transistor at U8 (B23) generates a negative pulse in its collector circuit. This pulse is used to reset the SEQLEN flip-flop in the sector equal detection circuit (B3). The negative pulse applied to inverter U13-9 (C4) produces a positive pulse at U13-8. This positive pulse resets the sector and subsector address registers.

4-37 READ/WRITE SECTOR CONTROL (1940083, SHEET 1)

The read/write sector control logic provides the control signals required for writing and reading of a sector on the disc.

4-38 Write Sector Control

When the WCLK clock pulse at U123-3 (C3) and the SCLK clock pulse at U123-5 are high, the SCSYN- pulse at U123-6 goes low, presetting the WRSYN flip-flop U95. At this time, the SCOS one-shot has already been triggered, causing the WSGO- signal at U34-1 to be low and the input to U49-1 to be high. The low WSGO- signal has also caused a low input at U26-1 causing a high input to U49-5. After the time delay of 120 nanoseconds, a low input is applied to U77-3, causing the SRCL signal at U77-6 to go high (refer to the Memory Buffer and Register Loading Circuit Description).

When the SCOS one-shot times out, the WSGO- signal goes high (false). At the same time, the SCSYN- signal goes high and the WCLK clock pulse resets the WRSYN flip-flop, causing a high input to be applied to U123-9. The transition from low to high of the WSGO- signal clocks the WRSC flip-flop U110-5. This applies a high input to U124-2.

When the sector address applied to the sector equal detection circuit is equal to the sector on the disc, the SEQL input to U124-13 goes high. If the PERM ADDRESS signal applied to U124-1 is high (address not locked out by disc unit write lockout switches), the WRL flip-flop U110 is conditioned with a high input at U110-12. The transition from low to high of the SCYSN- signal clocks the WRL flip-flop. This applies a high input to U123-10, U51-10, and U50-5. The high output from U110-9 is also applied to the WRITE signal flip-flop to condition it with a high input at its D input.

The SRCL signal at U77-6 goes high when the WSGOCK- signal at U49-6 goes low and goes low when the WSGO- signal goes high. The SRCLKW- pulses at U123-8 are generated by the WCLK pulses applied to U123-11. When each SRCLKW- pulse is generated at U123-8, the low input to U77-5 generates the SRCL pulse at U77-6.

The SRLD- signal at U66-6 goes low when the WSGO- signal goes low at U66-3 and goes high when the WSGO- signal goes high. The SRLDENW- signal at U51-8 goes low when 15 bits have been counted by the sector bit and word control circuit. The low input applied to U66-4 and U66-5 at this time causes the SRLD- signal to go low (refer to the Memory Buffer and Register Loading Circuit Description).

When the BFEMTY signal at U50-4 is still high after 15 SRCLKW- pulses have been counted by the sector bit and word control circuit, the inputs to U50-3, 4 and 5 are then high. This causes the TMERWR- signal at U50-6 to go low. When the next SCRCLKW- pulse occurs, the TMERWR- signal goes high. This sets the TMER flip-flop in the error circuitry, indicating a data late error (data transfer timing error) since the data from the processor did not arrive in time and caused the BFMETY signal from the buffer contents counter to remain high (memory buffer empty).

4-39 Read Sector Control

When the SCOS one-shot in the end control circuit is triggered, the RSGO- signal goes low, presetting flip-flop U53-5. This also applies a low input to U34-3 and to U26-2. After the time delay established by R16 and C28, the RSGO CK- signal at U49-8 goes low and clocks the bit and word control counter, which is loaded to a programmed count of 15 by the RSGO- signal (refer to the Sector Bit and Word Control Circuit Description).

The presetting of flip-flop U53-5 causes a low input to U90-8. When the sector address is equal to the address from the current location counter, the SEQL- signal at U90-9 goes low. This conditions the RDL flip-flop U95 with a high input at U95-12. The SCSYN- signal at U123-6 goes low when the SCLK and WCLK pulses are high, the low to high transitions at U95-11 clocks the RDL flip-flop U95, causing the RDL output at U95-9 to go high. This high output conditions the READ- signal flip-flop in the disc interface circuit with a high input at its D input. This causes the flip-flop to be set by the WCLK pulse, causing the READ- signal to the disc memory unit to go low (true).

The high RDL signal at U95-9 is also applied to U52-13. When the RCLK (read clock) pulse is applied to U52-2, the RDSC flip-flop U53 is clocked through U14-3. This causes the output from U53-6 to go high. This high output is applied to U52-10. This enables the SRCLKR- pulses at U52-8 which are generated by the RCLK- pulse applied to U52-9.

When 15 read data bits have been shifted into shift registers U57 through U60 in the buffer memory and register loading circuit, the input to U50-1, goes high, and BFLDCNR- signal output at U50-12 goes low. This causes a high input at U51-1. When 16 read data bits have been shifted into shift registers U57 through U60, all inputs to U51 are high, and the BFLDR- signal at U51-6 goes low (refer to the Memory Buffer and Register Loading Circuit Description).

The SRCLKR- pulses from U52-8 are also applied to U77-4 and generate the SRCL clock pulses during the read operation.

The BFLDR- pulse from U51-6 is also applied through inverter U22 to U50-9. If the BFFUL signal at U50-10 is still high at this time, the TMERRD- signal at U50-8 goes low. The low TMERRD- signal presets the TMER flip-flop in the error circuit, indicating a data late error (data transfer timing error), since the DCHI signal from the processor did not arrive in time and caused the BFFUL signal to remain high (memory buffer full).

4-40 Reset Circuits

The WRSC flip-flop U110 is reset when the WROP signal at U39-10 goes low, as a result of the resetting of the WROP flip-flop or when the WRL- signal goes low when the WRL flip-flop U110 is set.

The WRL flip-flop U110 and the RDL flip-flop U95 are reset when the INIT- signal at U124-9 goes low at the start of an operation, or when the WROP signal at U124-10 goes low as a result of the resetting of the RDOP or WROP flip-flop, or when the ENDSTR- signal goes low at the end of the write or read operation.

The RDSC flip-flop U53 is reset when the RDOP signal at U53-1 goes low as a result of the resetting of the RDOP flip-flop.

The WRSYN flip-flop U95 is reset when the signal at U95-1 goes low when the track origin- signal goes low.

4-41 BIT AND WORD CONTROL COUNTER (1940083, SHEET 1)

The bit and word control counter circuit counts the number of bits transferred during the write and read operations and generates the LSTWD (last word) signal for the subsector. It also provides control signals to the read/write sector control circuit and to the buffer and data register control circuit.

4-42 Write Control

When the WSGO- (D4) signal goes low, 4-bit binary counters U70 and U69 are cleared. During a write operation the RSGO- (D4) signal is high (false). Therefore, U70 and U69 are not loaded with the programmed inputs at A through D. When the WRSC flip-flop is set in the read/write sector control circuit, the low WRSC- signal presets flip-flop U53-9. This applies a high input to U69-10 (ENT) and to U54-1.

During the write operation, counters U70 and U69 are clocked by the SRCLKW- pulses applied to U55-5 which produce positive pulses at the clock input of U70 and U69. At the count of 12, the inputs to U54-2 and U54-13 go high. This applies a high input to pin 2 of flip-flop U67. The SRCLKW- pulses are also applied to U14-4 and produce positive pulses which clock the BFPSINH flip-flop U67. At the count of 13, flip-flop U67-5 is set. The low BFPSINH- signal from U67-6 is applied to the buffer and data register transfer control circuit and inhibits the generation of BFLDPS- pulses at the count of 13. At the count of 16, the BFPSINH flip-flop is conditioned with a low input at U67-2. When the next SRCLKW- pulse occurs, flip-flop U67 is reset.

At the count of 14 SRCLKW- pulses, the inputs to U54-11, 9 and 10 go high. This conditions flip-flop U67 with a high input at U67-12. When the 15th SRCLKW- pulse occurs, flip-flop U67 is set by the positive pulse from U14-6. The high EOWD signal is applied to the logic in the read/write sector control circuit (refer to the Read/Write Sector Control Circuit Description).

At the count of 16 SRCLKW- pulses, the inputs to U56-1, 2, 4 and 5 go low. This applies a high input to U55-9. Since the input to U55-10 is high during the write operation, the BDKO signal at U55-8 goes low when the SRCLKW- pulse goes high. The low BCKO- signal is applied to U65-1 and resets EOWD flip-flop U67. The low BCKO- signal is also applied to the read/write sector control circuit and causes the SRLDENW- and SRLD- signals to go high at this count.

At the count 16 BCNT15 pulses, the outputs from WC0 through WC3 go high. These outputs are applied to an AND gate in the cyclic cycle circuit and produce the LSTWD signal that conditions the CCYL flip-flop with a high input at its D input. When the LSTWD signal goes high, the input to U65-12 goes high. Since the WRL flip-flop is set in the read/write sector control circuit, the input to U65-13 is also high. This is a high output from U65-11 and a low input to U54-9 which inhibits the setting of the EOWD flip-flop U67. When the CCYL flip-flop is set in the cyclic cycle circuit after 16 more SRCLKR- pulses occur, the input to U90-2 goes high. This inhibits the setting of the EOWD flip-flop U67 until after the 16-bit cyclic code word is written.

4-43 Read Control

When the RSGO- signal goes low at the start of the read operation, the input to counter U70-9 and U69-9 goes low. When the low RSGOCK signal is applied to U55-3, counter U70 is programmed to the count of 15. When the RDSC flip-flop was preset in the read/write sector control circuit, the low RDSC- signal applied to U53-13 reset flip-flop U53. With U70 programmed to 15, the first SRCLKR- pulse applied to U55-4 resets U70 to the count of zero. This causes low inputs at U56-1, 2, 4 and 5 and a high input to U55-9. When the SRCLKR- pulse goes high (false), the BCKO- signal at U55-8 goes low. When the next SRCKLR- pulse occurs, flip-flop U53 is set. This enables counter U69 with a high input at U69-10 and also applies a high input to U54-1.

At the count of 13 SRCLKR- pulses, the output from U54-12 goes high. This conditions the BFPSINH flip-flop U67 with a high input at U67-2. When the next SRCLKR- pulse occurs, flip-flop U67 is set. The low BFPSINH- signal is applied to the buffer and data register transfer control circuit and inhibits the generation of DRSETBF- pulses at this count.

At the count of 15 SRCLKR- pulses, the output from U54-8 goes high. This high output is applied to U55-13. If the RDL flip-flop is set in the read/write sector control circuit, the EOWD flip-flop U67 is preset when the SRCLKR- pulse goes false (high). The high EOWD signal from U67-9 is applied to the read/write sector control circuit and causes the BFLDCNR- signal to go low at this point.

At the count of 16 SRCLKR- pulses, the BCN15 signal at U70-15 goes high. This signal is applied to the read/write sector control circuit and causes the BFLDR- signal to go low when the RCLK clock pulse occurs.

At the count of 17 SRCLKR- pulses, BFLDR- goes high, counter U70 is reset to zero, and the inputs to U56-1, 2, 4 and 5 go low. This causes a high input to U55-9, and the BCKO- signal at U55-8 goes low when the SRCLKR- pulse goes high (false). This applies a low input to U65-1 which resets the EOWD flip-flop U67, causing the BFLDCNR- signal in the read/write sector control circuit to go high.

At the count of 16 BCNT15 pulses, the outputs WC0 through WC3 go high. This produces the LSTWD signal in the same manner as for the write operation. After 15 more SRCLKR- pulses occur, the CCYL flip-flop is set and the input to U90-2 goes high. This inhibits the setting of the EWOD flip-flop until the 16-bit cyclic code word is read.

4-44 DISC/FORMATTER INTERFACE CIRCUIT (1940083, SHEET 1)

The disc/formatter interface logic circuit sends the unit select and track address signals to the disc memory units. It receives the track origin, read clock, write clock out, sector clock-, disc ready-, read data-, and illegal address- signals from the selected disc memory unit and returns the write clock in- signal to the selected disc memory unit.

The disc/formatter interface logic circuit also contains the logic for generating the write-, write data-, and read- signals that are sent to the selected disc memory unit.

The track origin-, sector clock-, write clock out-, read clock-, disc ready-, read data-, and illegal J3-10 per address- signals from the selected disc memory unit are applied through J3-21, J3-23, J3-47, J3-39, J3-2, J3-31 and J3-17, respectively. The signals are inverted and applied to various logic circuits as shown on the schematic.

4-45 FORMATTER/ADAPTER COMMON BUS (1940083, SHEET 2)

The formatter/adapter common bus receives the address and write data from the processor through the processor data bus. It applies the address signals to the unit, sector, subsector and track registers and the write data signals to the inputs of data selectors and registers U15 through U18. It also receives the DR00 through DR15 read signals from U15 through U18 and applies them to the processor data bus. In addition, the formatter/adapter common bus contains the 6-bit error register which provides the status of the disc memory system.

4-46 Address and Data Signals

The address signals (DB00 through DB15) and the write data signals (DB00 through DB15) are applied through electrical connector J1. Each signal line is terminated by a resistive network and applied to an inverter in its associated IC (U1 through U4). When the address given in the DOA instructions is on lines DB00 through DB15, the unit, track and sector address bits are applied to their respective address registers. For subsector operation, the subsector address contained in DB00 through DB03 is applied to a 4-bit register on the formatter/adapter interface. When the DOCX flip-flop is set in the initiation logic circuit, the subsector address bits are applied to the subsector address register U99 in the unit, track and sector address register circuit.

When the write data is on lines DB00 through DB15, the inverted data bits are each applied to their associated input on data selectros and registers U15 through U18.

During a read operation, the DB00 through DR15 input signals from U15 through U18 are applied to the register composed of U1 through U4. When the DATIA signal is applied from the processor, the DRGAT- signal at J2-J3 fall low. This strobes the read data signals to the output lines DB00- through DB15-. Output lines DB00- through DB15- route the signals to the processor via the adapter/formatter common bus and processor data bus.

4-47 Error Register

The error register is composed of gates U5 and U19. (C6) ILAER (bit 13), RDER (bit 14) and bits 10, 11, 12 and 14 cause a logical 1 in their associated bit in the register when they go high (true). Bit 15 is set to logical 1 when any of the 5 errors occur (refer to the error logic circuit description). When the DATIA signal is applied from the processor, the STATIN signal at J2-25 goes high. This strobes the contents of the error register to output lines DB10- through DB15-. Output lines DB10- through DB15- route the contents of the error register containing the disc memory system status to the processor via the adapter/formatter common bus and the processor data bus.

4-48 CYCLIC CYCLE, PARITY CYCLE, AND END CONTROL (1940083, SHEET 2)

The cyclic cycle, parity cycle, and end control logic circuit contains the CCYL flip-flop that is set when the 16-bit cyclic code word is written or read for each subsector of data, the PTYCYL flip-flop that is set when the odd parity bit is written or read for each subsector of data, and the ENDSTR one-shot that is triggered at the end of each subsector.

4-49 During Write Operation

After 240 bits (15 words) have been written in a subsector, the WC0 through WC3 signals at U68-1, 2, 4 and 5 (D8), respectively, go high. This causes the output from

U68-6 to go high, conditioning the CCYL flip-flop U63 with a high input at U63-2. This signal is the LSTWD signal. At this time, the PTYCYL- signal at U104-9 is high, since the PTYCYL flip-flop is reset. The BCNT15- signal at U104-10 is also high, since counter U70 in the sector bit and word control circuit is clocked to zero on the 240th bit count. When counter U70 again counts to 15, the BCNT15- signal at U104-10 goes low, causing the input to U77-11 to go high. When the SRCLKW- pulse for the 255th bit count goes high (false), all inputs to U77 are high. This causes a low output from U77-8 that is applied to the clock input (U63-3) of the CCYL flip-flop U68. When the SRCLKW- pulse for the 256th bit count goes low, the output from U77-8 goes high. The low to high transition at U63-3 sets the CCYL flip-flop U36. The 256th SRCLKW- pulse also clocks counter U70 to zero in the bit and word control circuit, causing the BCNT15- signal to go high and the LSTWD signal at U68-6 to go low.

The high output from U63-5 of the CCYL flip-flop U63 is applied to the disc interface logic circuit to enable the writing of the 16-bit cyclic code word and is also applied to U63-12 of the PTYCYL flip-flop U63. The low output from U63-6 is applied to the disc interface logic circuit to inhibit the writing of data at this time.

When 15 more SRCLKW- pulses have been counted by counter U70 in the bit and word control circuit, the BCNT15- signal at U104-10 goes low. This applies a high input to U77-11, causing a low input to U63-11. When the next SRCLKW- pulse occurs, the PTYCYL flip-flop U63 is set by the low to high transition at U63-11 and the CCYL flip-flop is reset by the low to high transition at U63-3.

The low output from U63-5 of the CCYL flip-flop is applied to U63-12 of the PTYCYL flip-flop U63. The high output from U63-9 is applied to the disc interface logic circuit to enable the writing of the odd party bit. The low output from U63-8 is also applied to the disc interface logic circuit to inhibit the writing of data at this time. The low output from U63-8 is also applied to U104-9, causing a high input to U77-11. This causes a low input to U63-11.

When the next SRCLKW- pulse occurs, the PTYCYL flip-flop U63 is reset by the low to high transition at U63-11. The low output from U63-9 is applied to U64. This triggers the ENDSTR one-shot U64, causing the output from U64-5 to go high and the output from U64-12 to go low. The low output from U64-12 is applied to U104-12, causing the SCOPCK signal at U104-11 to go high. The low output from U64-12 also resets the WRL flip-flop in the read/write sector control circuit, causing the WRITE- signal to be clocked high (false). The high SCOPCK signal at U104-11 is applied to the write sector GO circuit and causes the WSGO- signal to go low. After 200 nanoseconds, one-shot U64 times out, causing the SCOPCK signal to go low. This causes the WSGO- signal to go high.

The sequence described is repeated for each subsector until the end of the operation when the END signal and BFEMTY signal go high (true). This resets the WSGO flip-flop in the write sector start circuit, terminating the operation.

4-50 During Read Operation

The operation of the cyclic cycle, parity cycle, and end control logic circuit during a read operation is similar to the operation during a write operation as explained in the following paragraph.

During the read operation, the LSTWD signal goes high after 241 SRCLKR- pulses have been counted, since counter U70 in the sector bit and control circuit is loaded to a programmed 15 count at the start of the read operation. The SRCLKR- pulses at U77-9

are used in place of the SRCLKW- pulses during the read operation. When the ENDSTR one-shot U64 is triggered, the low output from U64-12 resets the RDL flip-flop in the read/write sector control circuit, causing the READ- signal to be clocked high (false). The high SCOPCK signal at U104-11 is applied to the read sector start circuit and causes the RSGO- signal to go low. After 200 nanoseconds, one-shot U64 times out, causing the SCOPCK signal to go low. This causes the RSGO- signal to go high.

The sequence is repeated for each subsector until the end of the operation when the ENDRD- signal at U57-12 in the done control circuit goes low. This resets the RSGO flip-flop in the read sector start circuit, terminating the operation.

4-51 ERROR LOGIC CIRCUIT (1940083, SHEET 2)

The error logic circuit generates 4 of the 5 error signals that are applied to the error register on the formatter/adapter common bus. These error signals include the disc fail error (bit 10), the write protect error (bit 11), the data transfer timing Error (bit 12) and the illegal address error (bit 13). The read error (bit 14) is generated by the read check error circuit. Bit 15 of the error bits is generated on the formatter/adapter common bus when any of the other errors occur.

4-52 Disc Fail Error

The DSC FAIL flip-flop U25 is set when the disc becomes not ready or when the system is hung during a write or read operation, the WRL flip-flop in the read/write sector control circuit is set when the SEQL signal goes high (true). This applies a low input to U23-4 conditioning U25 with a high input at U25-4. During a read operation, the RDL flip-flop in the read/write sector control circuit is set when the SEQL- signal goes low (true). This applies a low input to U23-4 conditioning U25 with a high input to U25-12. The DSCRDY- signal applied to U25-11 (CLOCK) goes low when the disc is ready. The DSCRDY- signal goes high if there is a loss of ac or dc power, if the dc voltages are below acceptable limits, or if the disc rotational speed is below the reliable operating range. When the DSCRDY- signal goes high, flip-flop U25 is set.

The DSC FAIL flip-flop U25 is also preset if the system is hung during a write or read operation. At the start of a write or read operation, the INIT- signal at U66-13 goes low. This causes a high to low transition at pin 1 of retriggerable TMOUT one- shot U37. This triggers U37, and the output at U37-4 goes low. This low output is applied to U66-10. Since the DSC FAIL flip-flop U25 is reset, the input to U66-9 is high. Since either the WROP (write operation) or RDOP (read operation) is set, the input to U66-11 is high, the output at U66-8 is low, and the input to U25-10 (PRESET) is high.

TMOUT one-shot U37 is a retriggerable one-shot that does not time out if it is retriggered before the time delay established by register R9 and capacitor C6 times out. Before TMOUT U37 times out, either the WSGO- signal (write operation) of the RSGO- signal (read operation) goes low, retriggering U37. The WSGO- signal at U66-2 goes low during a write operation at the start of each subsector. The RSGO- signal at U66-1 goes low during a read operation at the start of each subsector. If the WSGO- signal does not go low in time (300 nanoseconds) during a write operation, or the RSGO- signal does not go low in time (300 nanoseconds) during a read operation because the system is hung, one-shot U37 times out. This causes the input to U66-10 to go high, presetting the DSC FAIL flip-flop U25 with a low input from U22-8. This causes the DSC FAIL signal at U25-9 to go high, and the DSC FAIL- signal at U25-8 to go low.

For either cause of a disc fail error, the high output from U25-9 is applied to U19-10. The low output from U25-8 is applied to U20-9. This causes a logical 1 in 10 of the error bits and also causes a logical 1 in bit 15.

The low output from U22-8 that presets the DSC FAIL flip-flop U25 also is applied to U39-1. This causes the ENDER- signal at U124-6 to go low. This sets the DONE flip-flop, terminating the operation when the DSC FAIL- signal at U66-9 goes low and causes the ENDER- signal to go high. This causes the SELB- (selected busy) signal to the processor to go high (false). This also causes an interrupt request to be generated if the INTDSB flip-flop is reset.

4-53 Write Protect Error

The WPTER flip-flop U109 is preset when the selected track-sector is write protected. When the SCSYN- pulse goes false at the start of a subsector and the SEQL signal is high (true), the inputs to U24-9 and 10 are both high. The resulting high output from U24-8 is applied to U123-13. Since the WRSC flip-flop is set at this time, the input to U123-2 is high. The PERM ADDRESS- signal from the disc at U123-1 goes high when the selected track-sector is write protected. This causes the output from U123-12 to go low, presetting the WPTER flip-flop U109. The high output from U109-8 is applied to U20-11. This causes a logical 1 in bit 15 of the error bits.

The low output from U123-12 is also applied to U124-3. This causes the ENDER- signal at U124-6 to go low. When the SEQL signal at U24-9 goes low (false), the ENDER- signal goes high. This sets the DONE flip-flop, causes the SELB- signal to the processor to go high (false), and causes an interrupt request to be generated if the INTDSB flip-flop is reset.

4-54 Data Transfer Timing Error

The TMER flip-flop U25 is set when the processor has failed to respond in time to a request for data channel access. During a write operation, the TMERWR- signal at U25-3 (CLOCK) goes low (true) when the data from the processor does not arrive in time and causes the BFEMTY signal to remain high, indicating buffer empty (refer to the Read/Write Sector Control Circuit Description). When the TMERWR- signal goes high (false) one SRCLKW- pulse time later, the TMER flip-flop U25 is set.

During a read operation the TMERRD- signal at U25-4 goes low (true) when the processor does not generate the DCHI signal in time and causes the BFFUL signal to remain high, indicating memory buffer full. The low TMERRD- signal presets the TMER flip-flop U25. This causes the TMER signal at U25-5 to go high, and the TMER- signal at U25-6 to go low.

The high output from U25-5 is applied to U5-13 and causes a logical 1 in bit 12 of the error bits. The low output from U25-6 is applied to U21-5 and causes a logical 1 in the bit 15 of the error bits.

4-55 Illegal Address Error

The ILAER flip-flop U109 is set when the disc or track selected by the processor is not available on the system. Pin E2 is jumpered to pins E5 through E8 in accordance with the highest unit number assigned. If the disc unit selected is in the system but the track address is higher than the highest track on the disc, the inputs to U12-2 and 3 go low. This causes a high output from U12-1 and a low input to U23-13. The output at U23-11 then

goes high, causing a high input to U23-1 and U24-13 and a low input to U119-4. The low input to U119-4 inhibits the READ- signal. If the disc unit selected is not in the system, the input to U23-12 goes low, causing the high inputs to U23-1 and U24-13 and the low input to U119-4.

At the beginning of a write or read operation, the INIT-A signal goes low. This presets flip-flop U36. This causes the output from U36-5 to go high, applying a high input to U24-5. Since the RDOP signal is true (high) during both read and write operations, the input to U24-4 is also high. This causes the output from U24-6 to go high, applying a high input to U24-2. Since the ILAER flip-flop is not set at this time, the input to U24-1 is high. This causes the output at U24-3 to go high, applying a high input to U23-2. The output from U23-3 then goes low, presetting the ILAER flip-flop. The high output from U109-5 is applied to U5-10 and causes a logical 1 in bit 13 of the error bits. The low output from U109-6 if applied to U21-4 and causes a logical 1 in bit 15 of the error bits.

The low output from U23-3 is also applied to U124-4 and causes the ENDER- signal at U124-6 to go low (true). When the ENDER- signal to the processor goes high (false), and an interrupt request is generated if the INTDSB flip-flop is reset.

During a read operation, flip-flop U36 is reset at the end of the first subsector when the RDL flip-flop in the read/write sector control circuit. If the system becomes hung and an illegal address occurs, the inputs to U24-12 and 13 go high. This sets the ILAER flip-flop U109 with a high output from U24-11. This causes a logical 1 to be set in bits 10, 13, and 15 of the error bits. This also causes the DONE flip-flop to be set, the SELB- signal to the processor to go high (false), and an interrupt request to be generated if the MSKO flip-flop is reset.

4-56 MEMORY BUFFER AND REGISTER LOADING WRITE AND READ OPERATION (1940083, SHEET 3)

The memory buffer and register loading circuit consists of quadruple two-input multiplexers U15 through U18, quadruple two-line to one-line data selector/multiplexers U29 through U32 and U47, 64-bit read/write memories U43 through U46, 4-bit parallel access shift registers U57 through U60, buffer/disc access counter U61, and buffer/processor access counter U33. This circuit receives the write data from the processor, buffers it, and transfers it in serial form to the disc unit. This circuit also receives the serial read data from the disc, buffers it, and transfers it in parallel form to the processor. The timing diagram for the read and write operations appear in figures 4-4 and 4-5 respectively.

4-57 Write Operation

The DB00 through DB15 write data word from the processor is applied to the data selectors and registers U15 through U18 that are quadruple two-input multiplexers. During the write operation, the WROP signal at U34-11 is high, since the WROP flip-flop is set. This applies a low input to pin 10 (SEL A) of U15 through U18. When the DCHO signal is applied to the data channel transfer control circuit, the DRSETPS- signal goes low. This causes the DRSET signal at U34-9 to go high. This clocks U15 through U18 with a low input, and the DB00 through DB15 signals appear at the outputs of U15 through U18, since they were selected by the low input applied to each SEL A input.

The outputs from U15 through U18 are applied to the inputs of data selectors U29 through U32 that are quadruple two-line to one-line data selector/multiplexers. Since a high input is applied to the SEL input of U29 through U32 and the STR input of U29 through

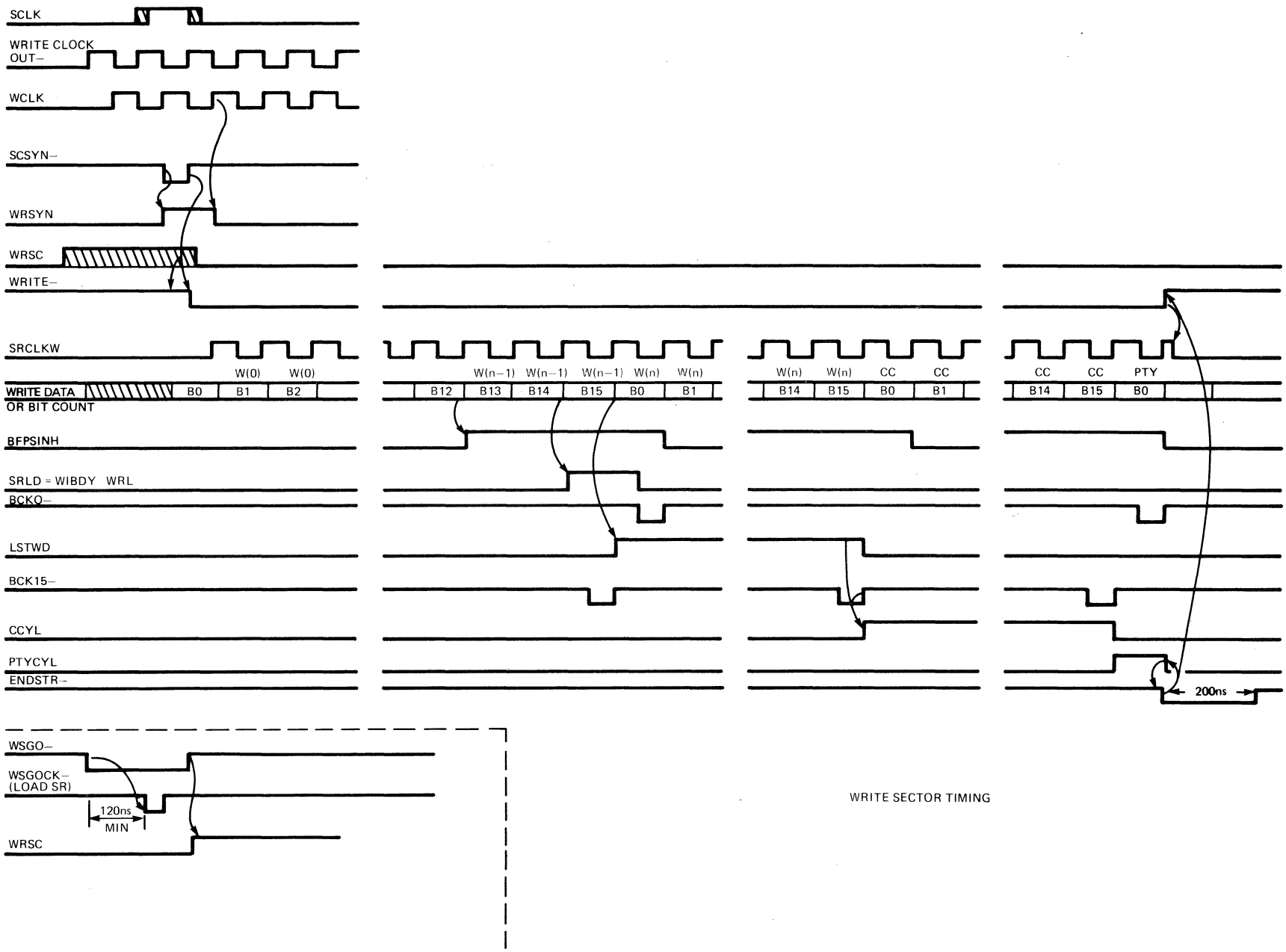


Figure 4-4. Write Subsector Timing Diagram

U32 is grounded, the inputs from U15 through U18 are selected and appear at the outputs of U29 through U32 and the inputs to memories U43 through U46.

At the start of the write operation, all inputs to NOR gate U20 are high. This causes a low output from U20-12 which is applied to the SELECT input of U47. This selects the outputs of the buffer/processor access counter U33. The BFLDPS- pulses at U48-2 occur as a result of the DCHO signals sent from the processor. This causes a low input at the write enable input of memories U43 through U46. The BFLDPS- pulses are also applied to U48-12 and clock the buffer/processor access counter U33 which is a 4-bit binary counter. When the first BFLDPS- pulse is applied, U33 is reset and the address output from U47-4, 7, 9 and 12 is 0000. When the WRITE ENABLE input of U43 through U46 goes low, the input data to the memories is written at this address. Memories U43 through U46 are 64-bit read/write memories that each store 16, 4-bit words.

The low BFLDPS- pulse applied to U48-12 clocks the 4-bit binary counter U33, and the address output from U33 advances to D001. When the next BFLDPS- pulse is applied, the input data of the next data word is written into the memories at this address. This loading process is repeated until the memory buffer is full. At this point, WSGO- signal goes low, causing the input to U47-1 (SELECT) to go high, selecting the buffer/disc access counter for operation. This also causes the SRLD- signal at the LOAD inputs of shift registers U57 through U60 to go low, and the input to U48-9 to also go low.

At this time, the 4-bit binary counter U61 is reset, and the address output from U47-4, 7, 9 and 12 goes to 0000. Since the write enable input to the memories is now high, the data stored at address 0000 is then read out of the memories in the complemented form and applied to the inputs of shift registers U57 through U60. When the SRCL clock pulse goes high after a short delay, the output data from address 0000 is loaded in parallel into the shift registers.

The low input to U61-2 goes low. When the WSGO- signal goes high, the SRLD- signal goes high. This clocks the 4-bit binary counter U61 so that the address at U47-4, 7, 9 and 12 goes to 0001.

When the SEQL signal in the sector equal detection circuit goes high (true), the WRL flip-flop in the read/write sector control circuit is set. This conditions the write signal flip-flop in the disc interface circuit with a high input at its D input. When shift registers U57 through U60 were loaded, the first bit from SR00 was applied in complemented form to the disc interface logic circuit where it conditioned the write data flip-flop in accordance with the logical state of the bit. When the WCLK pulse occurs and clocks the write data and write flip-flops, the logical state of the bit appears on the WRITE DATA- line and is written on the disc. With each SRCL pulse, the remaining bits of the first data words are shifted in the direction from U60 to U57 out of SR00 and written on the disc in their complemented form. When the last bit of the first data word has been written, the SRLD- signal goes low, and the data word from address 0001 in the memories is loaded in parallel into shift registers U57 through U60 when the SRCL clock pulse goes high. During the time that bits 0 through 11 are shifted to the disc, the next data word is written into the memories at address 0000 using the BFLDPS- signal and the buffer/processor access counter.

The SRLENW signal at U20-2 goes low at the same time that the SRLD- signal goes low, since the low SRLD- signal is generated by the low SRLENW signal. This causes the input to U47-1 to go high, selecting the buffer/disc access counter. When the SRLD- signal goes high 1-1/2 bit times later, U61 is clocked, and the output at U47-4, 7, 9 and 12 goes to 0010.

After the SRLD- signal at the LOAD inputs of shift registers U57 through U60 goes high, the SRCL pulse, which is now generated by the WCLK clock pulses, goes high and the first bit of the second word is shifted out of SR00. The process of reading the data words from the memories, loading them into shift registers, and shifting the bits serially to the disc is repeated for each word written into the memories.

During the write operation, the buffer contents counter, which is a binary count-up/count-down counter, counts up with each BFLD- signal and counts down with each SRLD- signal. The SRCLRW- pulse that generates the SRCL pulses the clock the bits out of the shift register are also applied to an 8-bit binary counter in the bit and word control counter. The counter counts up to 16 bits, 16 words and causes the LSTWD signal (for a subsector) to go true. It also provides control signals to the read/write sector control circuit during the write operation. After the LSTWD signal becomes true, the CCYL flip-flop is set after 16 more SRCLKW- pulses occur. The 16-bit cyclic code word is then written. After the 16th bit has been written, the PTYCYL flip-flop is set. The odd parity bit is then written. When the next SRCLKW- pulse occurs, the PTYCL flip-flop is reset and triggers the ENDSTR one-shot which produces the 200-nanosecond ENDSTR- pulse.

After the 16th subsector is gated the odd parity bit of the final subsector has been written, the buffer contents counter is at a count of zero and the BFEMTY signal goes high (true). The DONE flip-flop is then set (refer to the Initiation and Done Control Circuit Description). A timing diagram for the write operation appears in figure 4-4.

4-58 Read Operation

At approximately 16 bit times after the RSGO signal becomes true, the first bit data read from the disc is applied to pins 2 and 3 of shift register U60. Since the SRLD- signal is high at this time, the bit is shifted into U60 when the SRCL pulse occurs. During the read operation, the SRCL clock pulses are generated by the SRCLKR- pulses that are generated by the RCLK- pulses. The bits are shifted from U60 toward U57 until 16 bits have been shifted into the registers. When the 16 bits have been shifted into U57 through U60 the contents of the register are transferred in parallel on the SR lines to the inputs of data selectors U29 through U32. Since the WROP signal at U34-11 is low during a read operation, a low input is applied to the select inputs of U29 through U32. This selects the SR data inputs from shift registers U57 through U60. Since the strobe inputs of U29 through U32 are grounded, the SR data inputs are applied to the inputs of memories U43 through U46.

The RCLK pulse causes the SR data to be transferred from shift registers U57 through U60, and also causes the BFLDR- signal at U48-1 to go low. This causes a low input at the WRITE ENABLE inputs of memories U43 through U46. Since the BFLDCNR- signal at U20-13 goes low when 15 bits are in shift registers U57 through U60, the outputs from the buffer/disc access counter have already been selected through U47. This causes the SR data to be written into the memories at address 0000.

The low BFLDR- signal causes the outputs from counter U61 to change to 0001. During the writing of words into the memories, the buffer contents counter is advanced when each BFLDR- goes high (false). After the first BFLDR- goes high, the BFEMTY- signal goes high, enabling the DRSETBF- signal circuit in the buffer and data register transfer control logic. At this time, all inputs to U20 are high. This selects the outputs of the buffer/processor counter through U47. This causes the outputs from U47-4, 7, 9 and 12 to go to 0000. This address is applied to the memories and since the WRITE ENABLE inputs are now high, the word stored in address 0000 is read out of the memories in complemented form and applied to the input of data selectors and registers U15 through

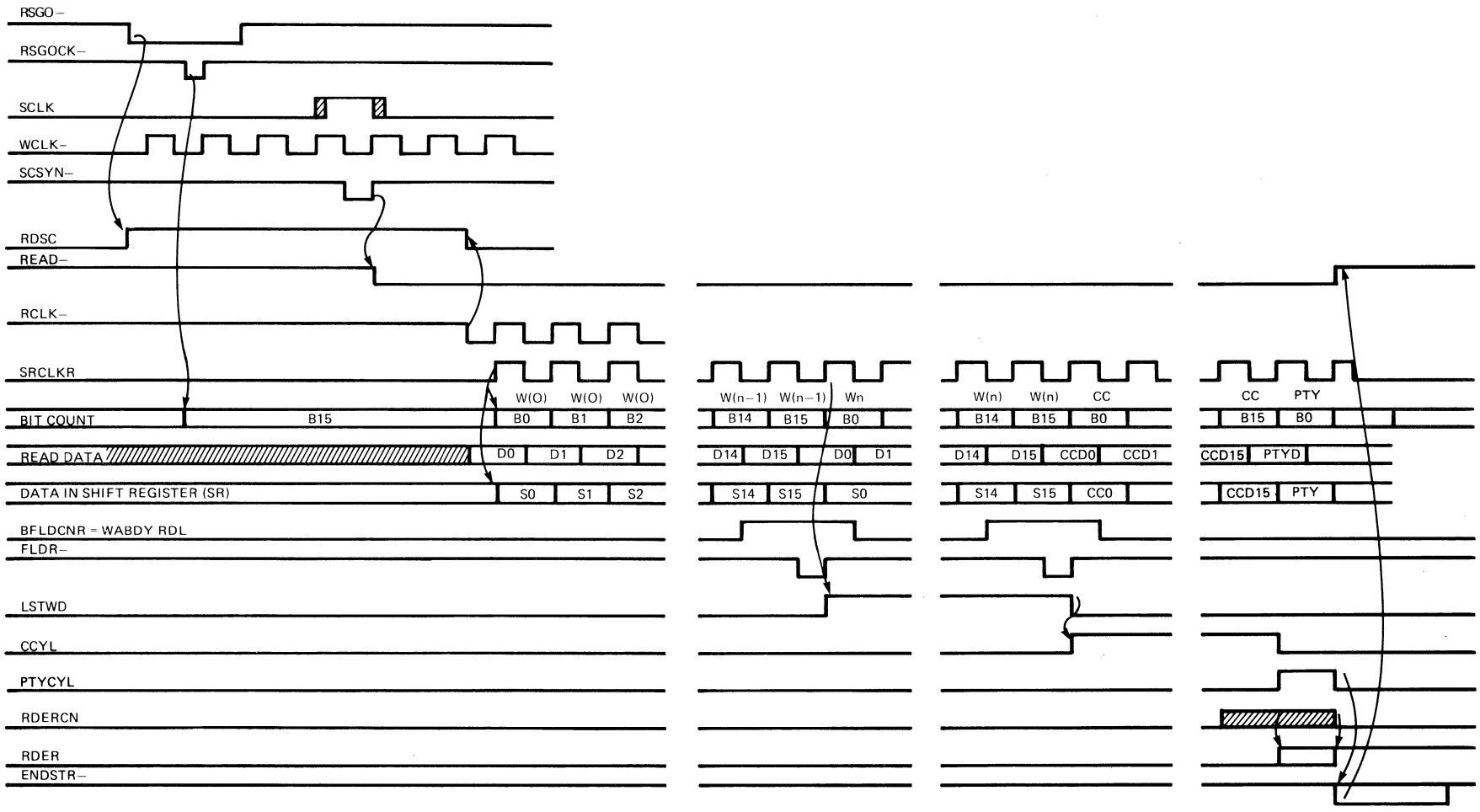


Figure 4-5. Read Subsector Timing Diagram

U18. Since the WROP signal at U34-11 is low during the read operation, the high input applied to the select A inputs of U15 through U18 causes the BF data outputs from the memories to the selected. When the first DRSETBF- pulse goes low, the DRSET pulse at U34-9 goes high clocking U15 through U18 and transferring the data to the DR lines to the processor via the formatter/adapter common bus.

The low DRSETBF- pulse applied to U48-13 causes the clocking of counter U33 and causing U33 to advance to 0001. After another data word is transferred from shift register U57 through U60 and written into address 0001 by the buffer/disc access counter, the buffer/processor access counter is again selected and the data from address 0001 is transferred to U15 through U18. If the DCHI signal does not arrive immediately, loading of the memories still continues. When the DRSETBF- pulse is generated as a result of the DCHI signal from the processor, the data from address 0001 is transferred from U15 through U18 to the processor via the formatter/adapter common bus. Counter U33 is then clocked to 0100. In this manner data is alternately transferred from the shift registers to the memories through data selectors U29 through U32 and read out of the memories until the LSTWD signal goes high (true) after 16 words have been read in the subsector. When the LSTWD signal goes true, the CCYL flip-flop is set after 16 more SRCLKR- pulses occur. The cyclic code word is then read. After the cyclic code word is read, the PTYCYL flip-flop is set. The odd parity bit is then read and the read error check is performed and, if a read error has occurred, the RDER signal is generated. However, a read error does not terminate the read operation. When the PTYCL flip-flop is reset, it triggers the ENSTR one-shot which produces the 200 nanosecond ENDSTR- pulse.

During the read operation, the buffer contents counter counts up when each BFLD- pulse goes high (false) and counts down when each DRSETBF- pulse goes high. After the odd parity bit of the final subsector has been read, the buffer contents counter is at a count of zero. The DONE flip-flop is then set (refer to the Initiation and Done Control Circuit Description).

4-59 TRACK AND SECTOR ADDRESS REGISTER LOGIC (1940083, SHEET 4)

The unit, track and sector address register logic circuit contains the registers for loading the unit, track and sector addresses contained in the DOA instruction. The circuit also contains the register loading the subsector address when the DOC instruction is used for subsector operation. In addition, the logic circuit provides the circuitry required to address a maximum of 4096 subsectors during subsector operation.

4-60 Unit Address Selection

The unit address contained in the DOA instruction from the processor (DB03 and DB02 from the formatter/adapter common bus) is applied to U71-10 and 3. When the TSASET- signal at U71-1 goes low as a result of the DATOA signal from the processor, the unit address is loaded into U71. When the disc memory unit selected has address logical 00, the inputs to U71-10 and 3 are low, and the outputs at U71-9 and 2 go low when the TSASET- signal goes low. This causes low inputs at U86-9 and 1 and high inputs to U102-12 and 13. This causes a low output from U102-3 that is applied to J3-15 and selects disc memory unit 0.

When the disc memory unit selected has the address logical 10, the input to U71-3 is low. When the STASET- signal goes low, the output at U71-9 goes high, and the output at U71-2 goes low. This causes a low output from U102-11 that is applied to J3-14 and selects disc memory unit 1.

When the disc memory unit selected has the address logical 01, the input to U71-10 is low, and the input to U71-3 is high. When the STASET- signal goes low, the input to U71-3 is high, and the output at U71-2 goes high. This applies a low input to U86-9 and a high input to U102-5. This causes a low output from U102-6 that is applied to J3-13 and selects disc memory unit 2.

When the disc memory unit selected has the address logical 11, the inputs to U71-10 and 3 are high. When the TSASET- signal goes low, the outputs at U71-9 and 2 go high. This causes high inputs to U102-9 and 10 and a low output from U102-8. This output is applied to J3-12 and selects disc memory unit 3.

The outputs to J15, J14, J13 and J12 are also applied to E pins E8, E5, E6, and E7 respectively, to configure the system in accordance with the number of disc memory units that are to be used (refer to chapter 2).

The information contained in this paragraph is applicable only when multiple memory units are "daisy-chained" in the memory system. The track and unit address register is incremented to a count of 128 (counts of 256 and 512 are selectable). This will cause the unit change flip-flop (U106) to set with TO (track origin) unit change flip-flop. The track and unit address register will be incremented from a track count of 127 to zero and increment the unit address by one. The controller waits for one TO time before looking for SEQL. If the processor changes from one unit to another, the changing of U71 pins 9 or 2 (unit address register) will pulse UACHG- resetting SEQLEN flip-flop inhibiting SEQL for one TO time. When low, the UACHG- signal resets the SEQLEN flip-flop.

4-61 Sector Address Register

The sector address contained in the DOA instruction from the processor (DB11 through DB15 from the formatter/adapter common bus) is applied to U113-15 and U74-9, 10, 1 and 15 respectively. When the TSASET- signal at U113-11 and U74-11 goes low as a result of the DATOA signal from the processor, the sector address is loaded into U113 and U74. When subsector operation is used, the SA10 through SA13 signals from the formatter/adapter PWBA interface are loaded into U99-15, 1, 10 and 9 respectively when the SALOS- signal at U99-11 goes low as a result of the DATOC signal from the processor. The initial sector or subsector address is applied to the sector equal detection circuit (refer to the Sector Equal Detection Logic Circuit Description).

Registers U99, U74 and U113 are 4-bit binary counters cascaded to count to the highest order sector address on a track. When the maximum number of subsectors are to be operated, the operation is as follows: The PTYCYL- signal at U99-5 goes low when the PTYCYL flip-flop is reset at the end of each subsector. When the PTYCYL flip-flop is reset at the end of each subsector, the PTYCYL- signal goes high. This advances counter U99 one count. When U99, U74 and U113 have counted up to the highest sector address on a track, flip-flop U76 is preset by a low output from U104-3. The high output from U76-9 is applied to U92-9. Since the input to U92-10 is high at this time, the output from U92-8 goes low when the track origin signal at U92-12 goes high at the start of the disc revolution. This clocks counter U73 to the next higher track address. When the track origin signal at U92-12 goes low, the output from U92-8 goes high. This resets flip-flop U76. In this manner, the track address register is advanced each time that the highest sector address is reached on the track being operated.

Each time that the track address register is advanced, a low input is applied to U20-4. This causes the HEAD CHANGE- signal at J3-32 to go low (true). The HEAD CHANGE- signal also becomes true at the start of the operation when the initial sector

address is loaded by the TSASET- signal. This causes a low input to U21-9, 10 and 11. When the reset function takes place, the low RST- signal applied to U20-3 also causes the HEAD CHANGE- signal to become true.

During normal operation when the DOC instruction is not used, the length of the operation is one sector (16 subsectors).

4-62 Track Address Register

The track address contained in the DOA instruction from the processor (DB04 through DB10 from the formatter/adapter common bus) is applied to U72-3, 10 and 4, and U73-11, 3, 10 and 4. When TSASET- signal at U73-1 and U72-1 goes low, as a result of the DATOA signal from the processor, the track address is loaded into U72 and U73. Registers U72 and U73 are 4-bit binary counters connected as a ripple-through counter. When the counter is advanced to the count of 127 all inputs to AND gate U75 go high. This enables flip-flop U106 with a high input at U106-12. When the track origin signal becomes false, flip-flop 106 is set, causing a low output from U75-8 which resets the SEQLEN flip-flop in the sector equal detection circuit. The initial track address loaded into U72 and U73 is sent to the disc memory unit on the TA0 through TA8 lines via electrical connector J3.

The track origin signal which sets U106 also increments the unit address when the track address is at its maximum count. Track address is dependent on the disc size when daisy-chained.

4-63 SECTOR EQUAL DETECTION LOGIC (1940083, SHEET 4)

The sector equal detection logic circuit compares the subsector and/or sector address from the subsector and sector address registers against the output count from the sector counter (current location counter). When the subsector and/or sector address is equal to the output on the sector counter, the SEQL and SEQL- signals are generated.

The sector counter is composed of 4-bit counters U127, U128 and U129 connected as a 12-bit ripple through counter. At the start of each disc revolution, the TO- (track origin) goes low (true) and resets counters U127, U128 and U129. When the TO- signal goes high (false) counters U127, U128 and U129 are cleared. The SCSYN- pulses at U116-9 go low at the beginning of each subsector of data. When each SCSYN- pulse goes high (false), counter U127 is clocked and advanced one count.

There are 16 subsectors in each of the 32 sectors on a track. The subsectors are numbered 0 through 15. The sectors in each track are numbered 0 through 31. When subsector operation is used, the DB00 through DB03 signals applied to register U99 select the subsector starting address and the DB11 through DB15 signals applied to registers U113 and U74 select the sector starting address. When sector operation is used, only the DB11 through DB15 signals are used. The outputs from regiester U99, U74 and U113 are each applied to a separate input of an exclusive OR gate, U100, U88 and U114.

The outputs from counters U127, U128 and U129 are also each applied to a separate input of an exclusive OR gate (U100, U88 and U114) through E pins E29 through E40. The E pins are wired for the required interlace factor of 1:1, 2:1, 4:1, or 8:1 (refer to chapter 2).

The following theory of operation is given for a selection of subsector 1 of sector 1 as the starting address with an interlace factor of 1:1. When counter U127 has counted 17 SCSYN- pulses, the outputs from U127-5 and U128-5 are high. The high output from

U127-5 (LCAA) is connected through E19 and E40 to pin 5 of exclusive OR gate U100. Since subsector 1 is the starting subsector address loaded into U99, the input to U100-4 is high. With high inputs at U100-5 and 4, the output from U100-6 goes low. This low output is inverted by U101, and the output at U101-10 goes high.

The high output from U128-5 (LCEE) is applied through E23 and E30 to pin 2 of exclusive OR gate U88. Since sector 1 is the starting sector address loaded into U74, the input to U88-1 is high. With high inputs at U88-2 and 1, the output at U88-3 goes low. This low output is inverted by U115, and the output at U115-4 goes high.

With high outputs now at U101-10 and U115-4, all outputs from all inverters U101 and U115 connected to U104-4 are then high. Since the SEQLEN flip-flop U76 was set when the TO (track origin) signal went high at the start of the disc revolution, the input to U104-5 is also high. This causes the SEQL- signal at U104-6 to go low, and the SEQL signal at U96-12 to go high, indicating sector equal. The SEQL and SEQL- signals are applied to the logic in the read/write sector control circuit (refer to the Read/Write Sector Control Circuit Description).

When the DSCRDY signal goes low, indicating disc not ready, or the UACHG- signal at U75-8 goes low, or the RST- signal goes low during the reset function, the SEQLEN flip-flop is reset. This inhibits the SEQL and SEQL- signals by applying a low input to U104-5.

4-64 BUFFER AND DATA REGISTER TRANSFER CONTROL (1940083, SHEET 5)

The buffer and data register transfer control logic circuit generates the BFLDPS- signals that are used to transfer data during the write operation, the DRSETBF- signals that are used to transfer data during the read operation, and the DRSET signals that are used to transfer data during both the write and read operations. It also contains the DRFUL flip-flop which controls the generation of the BFLDPS- and DRSETBF- signals and applies control signals to the data channel transfer control circuit.

4-65 During Write Operation

At the beginning of the write operation, the DRFUL flip-flop U38 is reset. When the DCHO signal from the processor is sent to the data channel transfer control circuit, the DRSETPS- signal at U14-13 and U68-13 goes low. This causes the DRSET signal at U14-11 to go high (refer to the memory buffer and register loading circuit description). This also causes the output at U68-8 to go low, applying a low input at the clock input of flip-flop U38. When the DRSETPS- signal goes high (false), flip-flop U38 is set by the low to high transition at its clock input. This enables gate U40 with a high input at U40-5. Since the memory buffer is not full at this time and the WROP flip-flop is set, the inputs to U40-2 and U40-4 are also high. This causes the output from U40-6 to go low and the input to U39-13 to go high. Since neither the cyclic cycle flip-flop or the parity cycle flip-flop is set at this time and the bit and word control counter is not between a count 13 to 16, the output from U54-6 is high. This applies a high input to U39-12. With high inputs at U39-12 and 13, flip-flop U38 is conditioned with a high input at U38-2.

Flip-flop U36 is set on the positive edge of every other WCLKD1 clock pulse applied to its clock input (pin 11). When U36 is set, the high output from U36-9 sets flip-flop U38. This causes the input to U40-1 to go high and the BFLDPS- signal at U40-12 to go low (true). The BFLDPS- signal is applied to the memory buffer and register loading circuit (refer to the Memory Buffer and Register Loading Circuit Description). The low

BFLDPS- signal is also applied to U68-9, causing a low input to the clock (U38-11) of the DRFUL flip-flop U38. When the BFDPS- signal goes high (false), the DRFUL flip-flop U38 is reset. In this manner, a BFLDPS- and a DRSET signal are generated for each DCHO signal sent from the processor. After 13 bits have been written in each word, the BFPSINH- signal at U54-4 goes low. This inhibits the BFLDPS- signal until the first bit of the next word has been written. If the memory becomes full, the BFLDPS- signal is inhibited by a low input to U40-3.

When the CCYL flip-flop is set for the writing of the cyclic code word, the input to U54-5 goes low. This inhibits the generation of the BFLDPS- signal. When the PTYCYL flip-flop is set for the writing of the parity bit, the input to U54-5 again goes low. This inhibits the generation of the BFLDPS- signal. Finally, when the ENDSTR one shot is triggered at the end of the subsector, the low input to U54-3 inhibits the BFLDPS- signal until the ENDSTR one-shot times out.

4-66 During Read Operation

At the beginning of the read operation, the DRFUL flip-flop, U38, is reset. This causes a high input to U52-5. Since the RDOP flip-flop is set, the input to U52-3 is high. After 16 bits are in shift registers U57 through U60, the BFLD- signal is generated. When the BFLD- signal goes high, the buffer contents counter counts up one count. This causes the BFEMTY- signal at U52-4 to go high and the output from U53-6 to go low. This causes a high input to U39-13. Since neither the CCYL or PTYCYL flip-flops are set at this time, the bit and word control counter has not counted to 13 and the ENDSTR one-shot has not been triggered, the output from U54-6 is high and the input to U39-12 is high. With high inputs at U39-12 and 13, flip-flop is conditioned with a high input at U38-2. When flip-flop U36 is set, the high output from U36-9 sets flip-flop U38, and the output from U38-5 goes high. This high output is applied to U40-9. When the WCLKD1 clock pulse goes low, the DRSETBF- signal at U40-8 goes low. The DDSETBF- signal is applied to the memory buffer and register loading circuit (refer to the Memory Buffer and Register Loading Circuit Description).

The low DRSETBF- signal is also applied to U68-10 and U14-12. The low input to U14-12 causes the DRSET signal at U14-11 to go high (refer to the Memory Buffer and Register Loading Circuit Description). The low input to U68-10 causes the output from U68-8 to go low. This applies a low input to the clock input (pin 11) of the DRFUL flip-flop U38. When the DRSETBF- signal goes high (false), the low to high transition at U38-11 sets the DRFUL flip-flop U38.

When the DCHI signal is sent from the processor, the DRAVL- signal at U68-12 goes low. This causes a low input to U38-11. When the DRAVL- signal goes high (false), the low to high transition at U38-11 resets the DRFUL flip-flop U38. Another DRSETBF- signal is then generated in the manner previously described.

When each DRAVL- signal is applied to U68-12, a DRSETBF- signal is generated. When the sector bit and word control counter has counted to 14 bits, the input of U54-4 goes low, inhibiting the DRSETBF- signal until the second bit of the next word. When the CCYL flip-flop is set for the reading of the parity bit, the input to U54-5 goes low. This again inhibits the generation of the DRSETBF- signal. Finally, when the ENDSTR one-shot is triggered at the end of the subsector, the low input to U54-3 inhibits the DRSETBF- signal until the ENDSTR one-shot times out.

4-67 BUFFER CONTENTS COUNTER AND BUFFER CONDITION DECODER (1940083, SHEET 5)

The buffer contents counter is composed of 4-bit up/down binary counters U42 and U41 and associated logic circuitry connected as a 5-bit up/down binary counter. The counter counts up one count when each data word is written into memory buffers U43 through U46 and counts down one count when each word is read out of memory buffers U43 through U46. The buffer condition decoder is composed of U12-13 and U13-12. The buffer condition decoder detects a full condition memory buffers U43 through U46 by decoding the outputs from the counter logic.

4-68 During Write Operation

At the beginning of the write operation, counter U42 is loaded to a programmed 15 count by the low INIT-A signal applied to U42-11. Since the BUFFS signal at U41-15 is high only the diagnostic read mode, counter U41 is programmed to zero by the INIT-A signal applied to U41-11.

The BLDF- signal applied to U6-13 goes low when each word is written into memory buffers U43 through U46. When the BFLD- signal goes false U42-5 goes high. This causes U42 to count up one count (reset to zero count), since the input at U42-4 is high at this time. Since the carry from U42-12 was applied to U41-5 when counter U42 was programmed to 15, the output from U41-3 goes high when U42 counts up. The output from U41-3 is inverted by U13 and applied to U12-12 and to various control circuits on the Nova adapter BWBA and formatter PWBA. As additional words are written into the memory buffers, counter U42 is advanced when each BFLD- pulse goes high. When the WSGO- signal goes low, the SRLD signal goes low, and the first word is read out of the memory buffers and loaded in parallel into shift registers U57 through U60.

When the SRLD- signal at U65-4 goes low to high it applies a high input to U42-4. Since the input to U42-5 is high at this time, counter U42 counts down one count. Another word is then written into the memory buffers, and counter U42 counts up one count as previously described. The next word is then then transferred to the shift registers, and counter U42 counts down one count as previously described. This sequence continues until only one word is left to be read out from the memory buffers. At this point, counter U42 has counted down to zero, and the borrow output from U42-13 is applied to U41-4. When the next SRLD- pulse goes high (false), counter U42 outputs go to the count of 15, and counter U41 output U41-3 goes low. Since the BFEMTY- signal is U41-3, the BFEMTY- signal is then low and the BFEMTY signal at U13-10 is then high, indicating buffer empty.

4-69 Buffer Condition Decoder

Whem memory buffers U43 through U46 are full (contain 16 words), the full condition is detected by the buffer condition decoder composed of NAND gate U12 and inverter U13. When the buffer contents counter has counted up to 16, the outputs from U42-3, 2, 6 and 7 go high and the output from U41-3 is high. This caused the outputs from U28-6 and U13-10 to go low. These low outputs are applied to U12-11 and U12-12 respectively. This causes the BFFUL signal at U12-13 to go high and the BFFUL- signal at U12-2 to go low, indicating a buffer full condition. The BFFUL and BFFUL- signals are applied to various control circuits on the Nova adapter PWBA and formatter PWBA.

4-70 During Read Operation

During a read operation, counters U42 and U41 operate in a similar manner to their operation during a write operation, except that the DRSETBF- signal at U65-5 is used for the count-down function instead of the SRLD- signal at U65-4. The BFLD- signal at U6-13 is also used for the count-up function during a read operation. As each word is read from the disc and written into memory buffers U43 and U46, counter U42 is advanced one count when the BFLD- pulse goes high (false). As each word is read out of the buffer memories and transferred to the processor, counter U42 counts down one count when the DRSETBF- signal goes high. The final count down of the buffer contents counter is the same as during a write operation.

4-71 During Diagnostic Read Operation

At the start of a diagnostic read operation, the BUFFS signal at U41-15 goes high. When the INIT-A signal is applied to U42-11 and U41-11, counter U42 is loaded to a programmed 15 count and counter U41 is loaded to a programmed 1. This is required because a diagnostic read operation may be performed without a preceding diagnostic write operation, since the readout from memory buffers U43 through U46 is non-destructive. In this case the buffer contents counter would be in the empty condition with the output from U41-3 low. Loading counters U41 to a programmed 1 count places the buffer contents counter in the full condition.

4-72 CYCLIC CODE GENERATOR, PARITY BIT GENERATOR AND READ CHECK ERROR CIRCUITS (1940083, SHEET 5)

The cyclic code generator generates the 16-bit cyclic code word that is written at the end of each subsector of data. The parity bit generator generates the odd parity bit that is written after the cyclic code word at the end of each subsector of data.

When the cyclic code word and the odd parity bit are read at the end of each subsector, they are compared against a cyclic code word and odd parity bit that is generated by the cyclic code generator and parity bit generator for the 16 words of data that have been read. If the cyclic code words or odd parity bits differ, the RDER (read error) signal is generated by the read check error circuit.

4-73 During Write Operation

At the start of each subsector, the SCLK signal at U80-9 and U80-10 (A20) goes high. This causes the output from U80-8 to go low, presetting the PTY flip-flop U79 and clearing shift registers U84, U97 and U82 and flip-flops U94 and U93.

When the subsector and/or sector address is equal to the outputs from the sector counter (current location counter), the WRL flip-flop is set in the read/write sector control circuit. This causes the WRL signal at U112-4 (C20) to go high. The WR DATA signal at U112-5 goes high each time a logical 1 bit is written and goes low each time a logical 0 bit is written.

The output from U112-6 is applied to U98-2 and to U90-1. The output from U98-3 is determined by the logical state of the signal at U112-4 and the state (set or reset) of flip-flop U93-9. The output from U98-3 is applied to pins 2 and 3 of 4-bit shift register U84 and to exclusive OR gates U98. The output from U98-8 conditions U94-12 with a high or low input, depending upon the state of flip-flop U94-5 and the output from U98-3. The

output from U98-11 conditions U93-12 with a high or low input, depending upon the state of flip-flop U93-5 and the output from U98-3.

The three shift registers U84, U97 and U82 (A20, B20) and the four flip-flops U94 and U93 (A19) are clocked by the trailing edge of the SRCLKW- pulses applied from U80-11. The inputs to shift register U84 are shifted in the direction from QA toward QD with each SRCLKW- pulse. The output from QD (U84-12) is a complemented output that is applied to exclusive OR gate U98-5. The output from U98-6 depends upon the logical state of the signal at U112-5 and the logical state of the output from U84-12. Shift registers U97 and U82 also shift in the direction from QA toward QD with each SRCLKW- pulse and provide complemented outputs at QD.

When the last data word is written, the CCYL flip-flop in Sheet 2 (C8) is set. The 16 bits of the cyclic code word are then written, shifting the bits in a direction from QA to QD in U84 (sheet 5, B20) toward flip-flop U93-9 (CCG16). Each time that flip-flop U93-9 is set, the CCG16- output from U93-8 goes low. This writes a logical 1 bit in the cyclic code word, since the CCG16- signal is applied to the AND/OR invert circuit that conditions the write data- signal flip-flop. Each time the flip-flop U93-9 is reset, a logical 0 bit is written in the cyclic code word.

The parity flip-flop U79 (A19) changes state with each logical 1 bit (high input) applied to U112-5. If there was an odd number of logical 1 bits written in the subsector (including the cyclic code word), flip-flop U79 will be in the reset state when the parity bit is to be written (after the PTYCYL flip-flop is set in the cyclic cycle, parity cycle, and end control circuit in sheet 5). This causes a logical 0 to be written (odd parity) since the low PTY- output from U79-6 is applied to the AND/OR invert circuit that conditions the write data- signal flip-flop. The cyclic code word has the characteristic that if an even number of ligical 1 data bits are written in the subsector it will have odd parity and if an odd number of logical 1 bits are written in the subsector it will have an even parity.

4-74 <u>During Read Operation And Read Check Error</u>

During a read operation, the RDL signal at U112 (C20) goes high when the RDL flip-flop is set in the read/write sector control circuit. The RD DATA signal at U112-3 goes high when each logical 1 bit is read from the disc. The operation of the circuit is the same as during a write operation, except that the SRCLKR- pulses at U80-13 are used in place of the SRCLKW- pulses at U80-12 (A20).

When the last data word is read in the subsector, the CCYL in sheet 2 (CB) flip-flop is set. The cyclic code word is then read. If the cyclic code word generated by the cyclic code generator for the data bits read in the subsector is the same as the cyclic code word read from the disc, the outputs from U83-6, U83-8, and U81-6 are high and the CCGNZR signal at U92-6 goes low. If any of the outputs are low, the CCGNZR signal at U92-6 goes high. This output is applied to U77-13 (sheet 2, D8). Since the BCNT15 signal at U77-2 (D8) and the CCYL signal at U77-1 are high at this time, flip-flop U79 is conditioned with a high input of U 79-12. When the SRCLKR- pulse occurs, flip-flop U79 is set. This causes the RDER signal at U79-9 to go high, indicating a CRC error (D6). The RDER signal is applied to the error register on the formatter/adapter common bus and causes a logical 1 in bit 15 of the error bits.

When the PTYCYL flip-flop (C8) is set, the input to U78-4 goes high. If the PTY flip-flop U79 (A18) is set at this time, the input of U78-5 (D8) is high. This conditions flip-flop U79 with a high input to U79-12 (D7). When the SRCLKR- (D8) pulse occurs, flip-flop U79 is set. This causes the RDER signal at U79-9 to go high indicating a parity error,

since the PTY signal at U78-5 (D8) should have been low if an odd number of logical 1 bits were read in the subsector.

In either case of a read check error, the low output from U79-8 (D7) is applied to U79-9 and inhibits any additional clocking of flip-flop U79.

4-75 Disc Interface Signals

The WRITE flip-flop U122 (B17) is conditioned with a high input at U122-2 when the WRITE flip-flop is set in the read/write sector control circuit (C2). This occurs when the sector address is equal to the outputs from the sector counter in the sector equal detection circuit and causes the SEQL signal to go high (true). At this time the WRL- signal at U108-1 and 13 (B18) goes low. Since the CCYL and PTYL flip-flops are reset at this time, three of the four inputs to NOR gate U108 of AND/OR invert gates U108 are low. If the SR00 signal at U108-4 is low, the output from U108-8 goes high, conditioning flip-flop U122 with a high input at U122-12. If a SR00 signal at U108-4 is high, the output from 108-8 goes low, coditioning flip-flop U122 with a high input at U122-12. The WRITE flip-flop U122 is reset by either the power on reset ($\overline{\text{POR}}$) signal from sheet 6 or initiate A (INIT-A) signal from the adapter board. When the WCLK signal occurs, it causes the output from U122-5 to go high, causing the $\overline{\text{WRITE}}$ signal to go low. This is used in power cycling feature contained in the description of sheet 6. Depending upon the logical state of the signal at U108-4, the write data- signal at J3-35 goes either low or high.

During the writing of the cyclic code word, the CCYL signal at U108-3 goes high, and the CCYL signal at U108-5 goes low. This again produces low inputs at three of the four inputs to NOR gate U108. Depending upon the logical state of the CCG16 signal at U108-2, the write data- signal goes either low or high.

When the odd parity bit is written, the PTYCYL signal at U108-10 goes high. This again produces low inputs at three of the four inputs to NOR gate U108. Depending upon the logical state of the PTY- signal at U108-9, the write data- signal goes either low or high when the WCLK clock pulse occurs.

The READ flip-flop U106 is conditioned with a high input at U106-2 when the RDL flip-flop is set in the read/write sector control circuit. This occurs when the sector address is equal to the outputs from the sector counter in the sector equal detection circuit and causes the SEQL- signal to go true (low). When the WCLK clock pulse occurs, flip-flop U106 is set. This causes the input to U19-5 to go high. If the address for the read operation is legal, the input to U19-4 is high. This causes the read- signal to the disc memory unit at J3-27 to go low (true).

4-76 POWER CYCLING (1940083, SHEET 6)

If there is a power loss the voltage is detected early enough so that a protective action is taken before the circuit elements lose their normal bias voltage. This is done through power on reset ($\overline{\text{POR}}$) signal (B22) and $\overline{\text{WRITE}}$ signal (B17).

When power on reset ($\overline{\text{POR}}$) signal detects a voltage of less than 4.2 volts over 50 ± 10 μsec, it resets the disc WRITE flip-flop U122 (B17). The output $\overline{\text{WRITE}}$ causes the $\overline{\text{Q}}$7 (D23) to clamp on the write circuit and force it to its nonactive state. When the voltage source becomes greater than 4.50 volts for over 100 ± 30 msec, the write circuit is enabled.

Chapter 5

MAINTENANCE

MAINTENANCE

5-1 INTRODUCTION

This chapter provides troubleshooting procedures confined in replacing the PC boards and/or the power supply.

5-2 TROUBLESHOOTING TOOLS

The tools needed for such limited troubleshooting are as follows:

1. Digital volt-ohmmeter.
2. Standard field service tool kit

5-3 TROUBLESHOOTING PROCEDURES

If all equipment external to the controller are functioning properly, the following outline is used to isolate a malfunction via board level of maintenance.

a. Verify that all cables are connected according to figure 2-1. Make sure that cable connectors are properly seated.

b. Verify that the adapter board is plugged into the Nova computer I/O slot.

c. Verify that the power switch on the assembly formatter assembly front panel is in the ON position and that the fuse located at the rear of the chassis is installed and functioning.

d. Remove top cover from formatter assembly chassis. With the volt-ohmmeter, check for +5 volts at the J4-5 on the formatter PC board. Voltage should be:

5 volts $\pm$ 1% (with J4 connected)

If voltage is not within the above values, make the adjustment according to the following step.

e. Remove formatter PC board hold-down clamp by removing two screws. Rotate the front of the hinged PC board upward. The adjustment pot can be accessed through the round hole located inside the chassis in the back right-hand corner. If power supply cannot be adjusted according to specification,

it must be replaced according to paragraph 5-4 and the defective power supply routed for repair.

f. If the malfunction is not isolated by the steps above, replace the formatter PC board and run diagnostics to check it out. If problem persists, replace adapter PC board. Again run diagnostics. If a defective board is found, route it for repair. If problem remains, the malfunction is likely located in the external equipment or in defective cable.

5-4 POWER SUPPLY REMOVAL AND REPLACEMENT

The following steps may be used in order to remove and replace the power supply.

a. Remove both top and bottom chassis covers from formatter assembly.

b. Unplug J4 connector from formatter PC board.

c. Unplug both J1 and J2 connectors located in power supply.

d. Remove four screws from bottom of chassis to free power supply.

e. Remove power supply from chassis and route for repair.

f. Reverse above steps to install new power supply.

g. Check new power supply according to the procedure described in step d of paragraph 5-3.

Chapter 6

DRAWINGS AND PARTS LISTS

DRAWINGS AND PARTS LISTS

6-1 INTRODUCTION

This chapter contains the drawings required to maintain the 8011 Disc Memory Controller. A list of replaceable parts is also included.

6-2 DRAWINGS

Table 6-1 lists the drawings contained in this chapter. These are assembly schematic and wiring diagrams. The partial drawing tree in figure 6-1 shows the order in which the drawings apply to the controller.

TABLE 6-1. CONTROLLER DRAWINGS

DRAWING No.	DRAWING TITLE
1040027	Adapter PC Board Assembly
1940027	Adapter PC Board Schematic
1040083	Formatter PC Board Assembly
1940083	Formatter PC Board Schematic
1020129	Formatter Assy
1940080	Connector Interface Board
1940081	Connector Interface Board
1930025	System Interconnect Diagram
1060019	Cable Assembly
1060024	CPU A Cable Assembly
1060025	CPU B Cable Assembly
1020093	Rear Panel Assembly
1930003	Power Supply Wiring Diagram

6-3 PARTS LIST

A list of replaceable parts for the adapter and formatter PC boards is given in table 6-2.

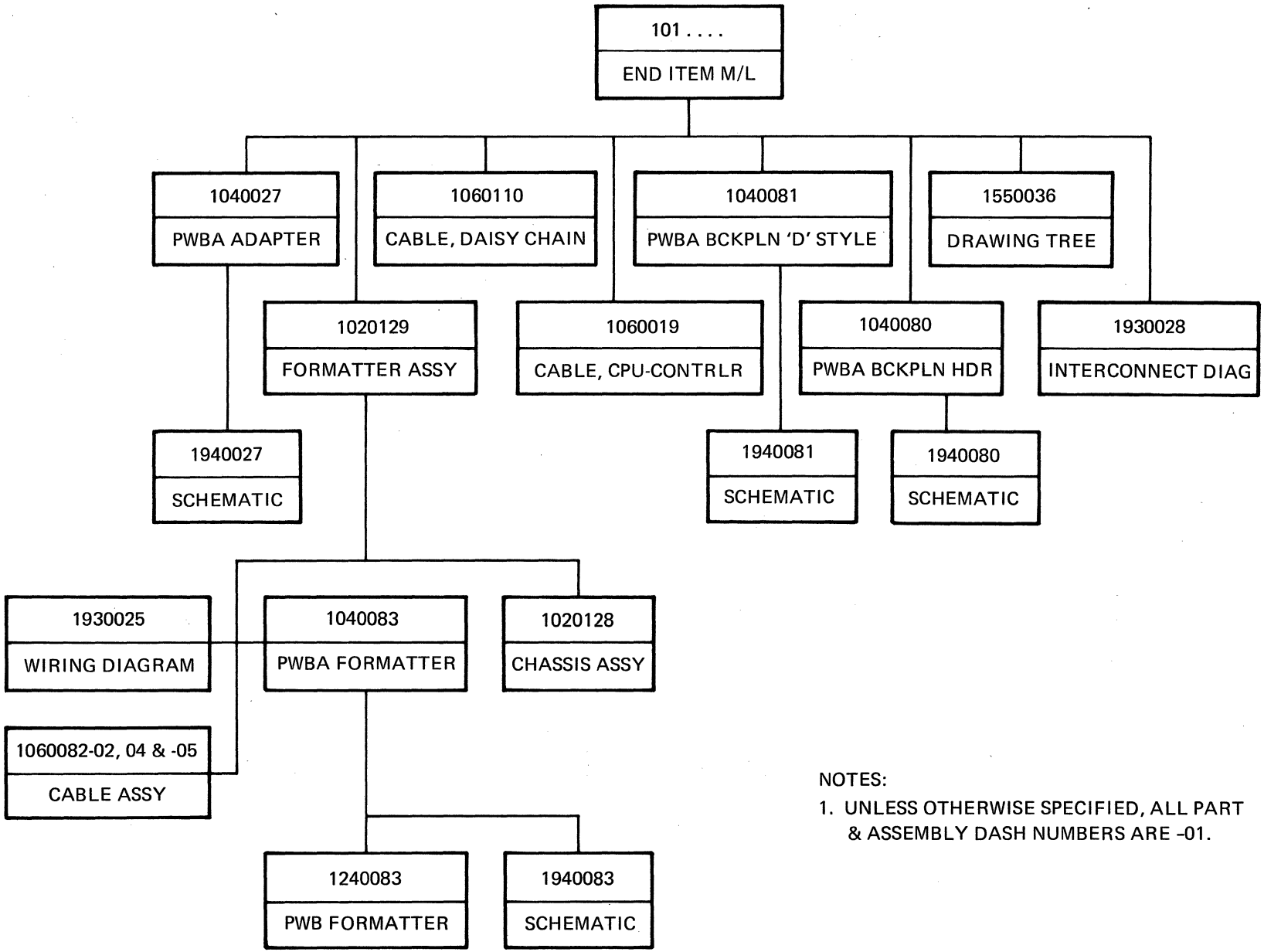


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Figure 6-1. 8011 Disc Memory Controller Drawing Tree (Partial)

TABLE 6-2. REPLACEABLE PARTS LIST

AMCOMP PART No.	DESCRIPTION/LOCATION	QUANTITY
	ADAPTER PC BOARD COMPONENTS	
1040027	Adapter PC Board Assembly	1
04122221-01	Res. Fxd, 220 ohms, $\frac{1}{4}$ w, 5%/R7, R8, R11, R13, R16, R17, R19, R24, R33, R36, R37, R39, R41, R44, R46, R47, R49, R52, R54, R55, R57, R60, R62, R63, R65, R68, R70, R72, R76, R80	30
04122331-01	Res. Fxd. 330 ohms, $\frac{1}{4}$ w, 5%/R6, R9, R10, R14, R15, R18, R20, R23, R34, R35, R40, R38, R42, R43, R45, R48, R50, R51, R53, R58, R59, R56, R61, R64, R66, R67, R69, R71, R75, R79	30
04122102-01	Res. Fxd., 1K ohms, $\frac{1}{4}$ w, 5%/R1, R2, R3, R4, R5, R12, R21, R22, R25, R26, R27, R28, R29, R30, R31, R32, R73, R74, R77, R78, R81	21
01400101-27	Cap. Fxd., Cer., 100 pf, 100v, 10%/C1 through C15	15
01400106-01	Cap. Fxd., Cer, .01 μf/C18 through C71	54
01383201-01	Cap. Fxd., Mica 200 pf, 500v, 5%/C16	1
01400109-21	Cap. Fxd., Mold Cer. 470 pf, 200v, 5%/C17	1
01200104-03	Cap. Fxd., Tant. 15 μf, 10v, 20%/C72 through C77	6
03201101-01	I.C., 14 pins, 7400/U2, U4, U9, U28, U55	5
03201142-01	I.C., 14 pins, 7402/U41, U42	2
03201109-01	I.C., 14 pins, 7410/U3, U16, U17, U21, U53, U57	6
03201123-01	I.C., 14 pins, 7474/U49, U54, U56, U60, U61, U62	6
03201104-01	I.C., 14 pins, 7404/U7, U18, U40, U53	4
03201118-01	I.C., 14 pins, 7473/U14	1
03201134-01	I.C., 16 pins, 74193/U43, U44, U46, U48	4
03201111-01	I.C., 14 pins, 74H11/U15	1
03201108-01	I.C., 14 pins, 7408/U1, U20, U27, U59	4
03201119-01	I.C., 14 pins, 7438/U5, U8, U23, U24, U25, U26	6
03201128-01	I.C., 14 pins, 74197/U36, U37, U38, U39	4
03201114-01	I.C., 14 pins, 7417/U6, U19, U22	3
03100111-02	I.C., 16 pins, 75138/U30, U31, U33, U35	4
03201138-01	I.C., 16 pins, DS8838/U10, U11, U12, U13	4
	FORMATTER PC BOARD COMPONENTS	
1040083	Formatter PC Board Assembly	1
07100898-40	Connector, 50-pin/J1, J2, J3	3

TABLE 6-2. REPLACEABLE PARTS LIST (continued)

AMCOMP PART No.	DESCRIPTION/LOCATION	QUANTITY
	FORMATTER PC BOARD COMPONENTS (continued)	
47080101-01	Header Assembly, 10-pin, right angle/J4	1
04122100-01	Res., 10 ohms, $\frac{1}{4}$ w, 5%/R91	1
04122220-01	Res., 22 ohms, $\frac{1}{4}$ w, 5%/R69	1
04122101-01	Res., 100 ohms, $\frac{1}{4}$ w, 5%/R1	1
04122151-01	Res., 150 ohms, $\frac{1}{4}$ w, 5%/R2, R17, R21, R37, R68, R81	6
04122221-01	Res., 220 ohms, $\frac{1}{4}$ w, 5%/R46, R53, R72, R75, R92	5
04122271-01	Res., 270 ohms, $\frac{1}{4}$ w, 5%/R79	1
04122331-01	Res., 330 ohms, $\frac{1}{4}$ w, 5%/R45, R52	2
04122471-01	Res., 470 ohms, $\frac{1}{4}$ w, 5%/R67	1
04122511-01	Res., 510 ohms, $\frac{1}{4}$ w, 5%/R11, R14, R23 through R31, R34, R35, R36, R43, R56	18
04122561-01	Res., 560 ohms, $\frac{1}{4}$ w, 5%/R71, R78, R88, R90	4
04122621-01	Res., 620 ohms, $\frac{1}{4}$ w, 5%/R83	1
04122102-01	Res., 1K ohms, $\frac{1}{4}$ w, 5%/R6, R7, R15, R18, R19, R33	27
04122122-01	Res., 2.2K ohms, $\frac{1}{4}$ w, 5%/R74, R76, R89, R96	4
04122222-01	Res., 2.2K ohms, $\frac{1}{4}$ w, 5%/R74, R76, R89, R96	4
04122272-01	Res., 2.7K ohms, $\frac{1}{4}$ w, 5%/R98	1
04122472-01	Res., 4.7K ohms, $\frac{1}{4}$ w, 5%/R87, R93, R94	3
04122510-01	Res., 51 ohms, $\frac{1}{4}$ w, 5%/R69	1
04122622-01	Res., 6.2K ohms, $\frac{1}{4}$ w, 5%/R10	1
04122822-01	Res., 8.2K ohms, $\frac{1}{4}$ w, 5%/R16, R40, R41	3
04122103-01	Res., 10K ohms, $\frac{1}{4}$ w, 5%/R82	1
04122123-01	Res., 12K ohms, $\frac{1}{4}$ w, 5%/R85	1
04122393-01	Res., 39K ohms, $\frac{1}{4}$ w, 5%/R9	1
04122623-01	Res., 62K ohms, $\frac{1}{4}$ w, 5%/R73	1
04444502-01	Res., Variable, 5K/R70	1
04551331-01	Res., Net Dip, 330/RN2, RN5, RN7, RN9, RN11, RN13, RN15, RN3	8
04551221-01	Res., Net Dip, 220/RN1, RN4, RN6, RN8, RN10, RN12, RN14, RN16	8
02100914-03	Diode, IN914B/CR1-CR3, CR5-CR10	9
02100102-01	Diode, IN4454/CR4	1
05100104-01	Transistor, 2N3646/Q5-Q8	4
01383101-01	Cap., 100 pf, 500v, 5%/C59, C60, C28	3
01400109-16	Cap., 180 pf, 200v/C131	1
01383221-01	Cap., 220 pf, 500v, 5%/C33, C40, C57	3
01383201-01	Cap., 200 pf, 500v, 5%/C1, C2	2
01400101-52	Cap., 1000 pf/C19, C72	2
01400106-01	Cap., .01 μf, 16v/C8-C14, C17, C18, C20-C26,	94

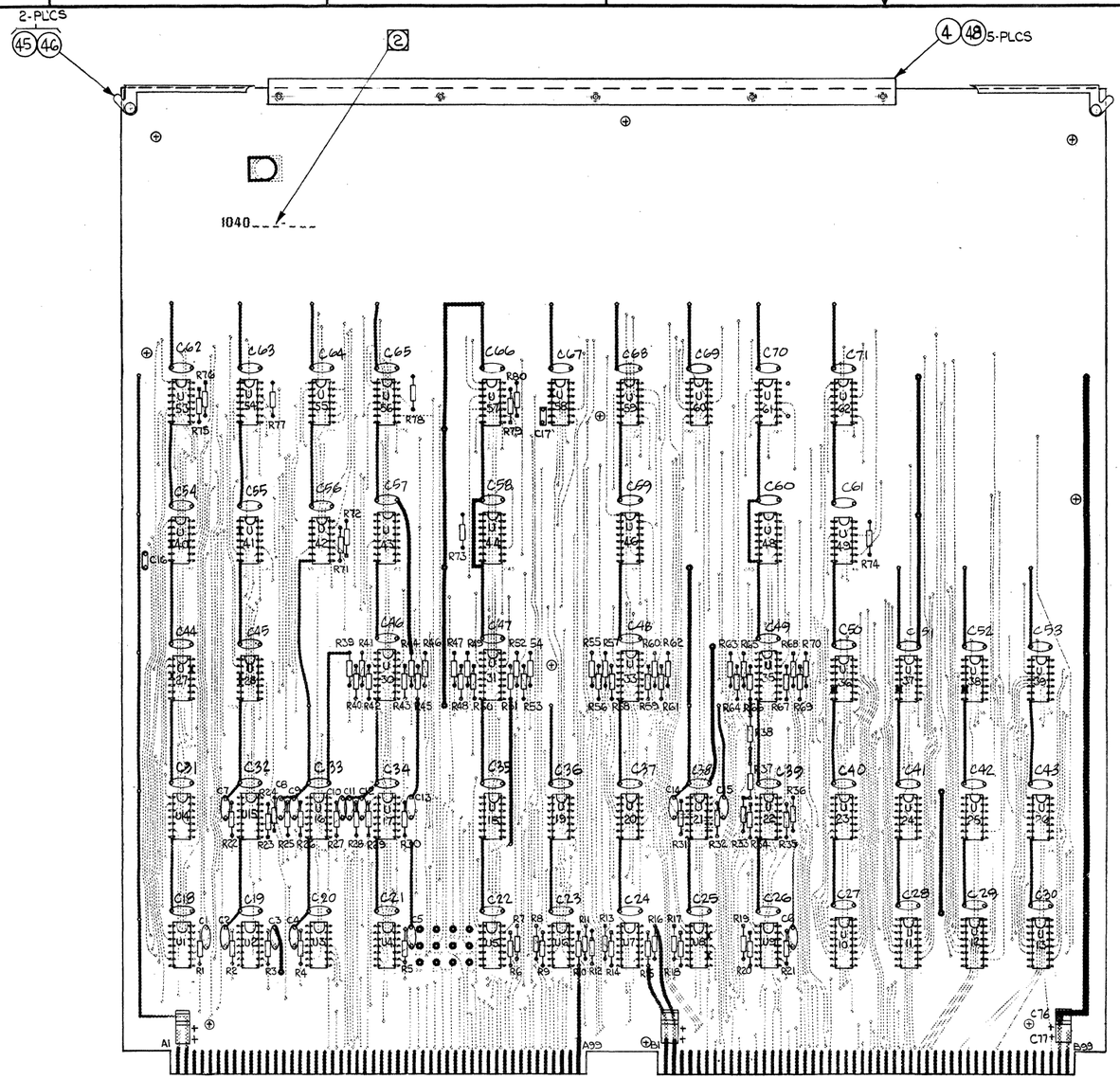
TABLE 6-2. REPLACEABLE PARTS LIST (continued)

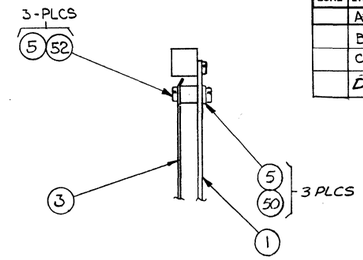
AMCOMP PART No.	DESCRIPTION/LOCATION	QUANTITY
	FORMATTER PC BOARD COMPONENTS (continued)	
	C30-C32, C34-C39, C43-C50, C53, C54, C55, C56, C58, C61, C62, C63, C64, C65, C68, C69, C70, C71, C73-C81, C84-C95, C98-C108, C111-C125	
01200102-17	Cap., 2.2 μf, 20v/C128	1
01200104-04	Cap., 22 μf/C6	1
01225226-01	Cap., 22 μf, 15v, 20%/C7, C15, C16, C27, C29, C41, C42, C51, C52, C66, C67, C82, C83, C96, C97, C109, C110	17
01200103-31	Cap., 33 μf, 35v/C132	1
01200102-37	Cap., 100 μf, 20v/C129, C130	2
01225107-01	Cap., 100 μf, 20v/C3	1
03201101-01	I.C., 14 pins, 7400/U78	1
03201142-01	I.C., 14 pins, 7402/U12, U90	2
03201130-01	I.C., 16 pins, 7445/U117	1
03201123-01	I.C., 14 pins, 7474/U25, U36, U53, U76, U79, U106, U122	7
03201102-01	I.C., 14 pins, 74H00/U14, U23, U104	3
03201104-01	I.C., 14 pins, 7404/U13, U22, U34, U86, U96, U116	6
03201120-01	I.C., 14 pins, 74H51/U112	1
03201110-01	I.C., 14 pins, 74H10/U20, U40, U50, U52, U55, U77, U123	7
03201105-01	I.C., 14 pins, 74H04/U105, U118, U119	3
03201107-01	I.C., 14 pins, 7405/U35, U101, U115	3
03201118-01	I.C., 14 pins, 7437/U80	1
03201124-01	I.C., 14 pins, 74H74/U38, U63, U67, U93, U94, U95, U109, U110	8
03201112-01	I.C., 14 pins, 7413/U49	1
03201134-01	I.C., 16 pins, 74193/U4, U42, U74, U99, U113	5
03201111-01	I.C., 14 pins, 74H11/U21, U54, U66, U75, U124	5
03201116-01	I.C., 14 pins, 74H21/U68, U87	2
03201108-01	I.C., 14 pins, 7408/U24, U39, U48, U65, U85	5
03201121-01	I.C., 14 pins, 74H54/U108	1
03201133-01	I.C., 16 pins, 74161/U33, U69, U70, U61	4
03201139-01	I.C., 16 pins, 74123/U37, U64	2
03201122-01	I.C., 14 pins, 74H20/U28, U92	2
03201140-01	I.C., 16 pins, 7489/U43, U44, U45, U46	4
03201125-01	I.C., 14 pins, 7486/U88, U100, U114	3
03201143-01	I.C., 16 pins, 74157/U29, U30, U31, U32, U47	5
03201117-01	I.C., 14 pins, 7425/U56, U81, U83	3
03201119-01	I.C., 14 pins, 7438/U5, U19, U26, U102, U107, U120, U121	7
03201128-01	I.C., 14 pins, 74197/U71, U72, U73, U127, U128, U129	6
03201113-01	I.C., 14 pins, 7416/U7	1

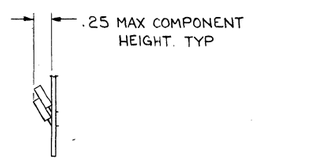
TABLE 6-2. REPLACEABLE PARTS LIST (continued)

AMCOMP PART No.	DESCRIPTION/LOCATION	QUANTITY
	FORMATTER PC BOARD COMPONENTS (continued)	
03201114-01	I.C., 14 pins, 7417/U6, U11, U62, U103	4
03201115-01	I.C., 14 pins, 74S20/U51	
03201126-01	I.C., 14 pins, 74S86/U89, U91, U98	3
03100111-02	I.C., 16 pins, 75138/U1, U2, U3, U4	4
03201144-01	I.C., 16 pins, 74195/U57, U58, U59, U60, U82, U84, U97	7
03201150-01	I.C., 16 pins, 74283/U130	1
03201135-01	I.C., 16 pins, 74298/U15, U16, U17, U18	4
03000102-01	I.C., 14 pins, 3046/U8	1
47210002-01	Wire-Wrap Pin/E1-E62	

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	PRE-PROD RELEASE 8010-06	8/4/75	MG.
	B	SEE EO 8203, 8224	9/1/75	MG.
	C	SEE EO 8288, 8321	11/8/74	MG.
	D	REVISED PER EO 50122	8/24/76	MG







NOTES:

1. WORKMANSHIP SHALL COMPLY WITH QA100000-00
2. IDENTIFY WITH APPROPRIATE ASSY PART NO. AND M/L REV PER 1550010.
3. MAXIMUM COMPONENT LEAD PROTRUSION ON CIRCUIT SIDE OF BOARD SHALL BE .060

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

1040027-02	WITH CP
1040027-01	WITHOUT CP
PART NO.	CONFIGURATION

TABULATION BLOCK

NOTICE

THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

8010	END ITEM
USED ON	NEXT ASSY.

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX±, .XXX±, ANGLES —

MATERIAL —

FINISH —

SIGNATURE		DATE
DFT.	K. Quinn	8/8/75
CHK.	J. Mowers	8/8/75
APP.	J. Bingham	9/11/75
APP.		

DATA DISC INCORPORATED

TITLE
ADAPTER PWBA

SIZE	DRAWING NO.	REV.
D	1040027	D
SCALE 1/1	PROJ. NO.	SHEET 1 OF

ZONE	LTR	REVISIONS DESCRIPTION		
	C	SEE ECO 3244		
	D	SEE ECO 3337		
	E	SEE ECO 50995		

INITIATION AND DONE CONTROL

INTERRUPT CONTROL

READ SECTOR GO

WRITE SECTOR GO

REF DESIGNATION	
HIGHEST USED	NOT USED
C77	—
E3	—
R81	—
U62	U29, U32, U34, U45, U47, U50, U51, U52

(5) UNIT SHIPPED FOR DEVICE ADDRESS =20
FOR DEVICE ADDRESS 60 CUT TRACE FROM E2 TO E1 AND ADD JUMPER FROM E3 TO E1.

4. "–" INDICATES LOW TRUE LOGIC TERM.
3. "X" INDICATES OPEN COLLECTOR OUTPUT
2. ALL CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTORS ARE IN OHMS 1/4W 5%.

NOTES:

MODEL 8010	N/A	DATA DISC
TOLERANCES UNLESS OTHERWISE SPECIFIED: DO NOT SCALE DRAWING. DECIMALS XX ±.01, XXX ±.005. ANGLES ±1°. MATERIAL:	ENGINEER	DIAGRAM LOGIC ADAPTOR BOARD
	CHECKED	
	DRAFTSMAN 11-3-75	SIZE E — DRAWING NO. 1940027 E — SCALE — — SHEET 1 OF 3

REVISIONS		
ZONE	LTR	DESCRIPTION
E		SEE SHEET 1

(B11)(B1) DCHIN-

(C1) STATIN- 7437 U14

(D4) BUSY-

(C12) DCHBSY 7437 U14

(B1)(D12) WRDP

(D4) MAIN-

(C1) SALOS-

(C1) DOCX-

(D4) START

(C4) STCLD-

(B4) END

(D12) RDDP

(B4) BFEMTY

(C12)(D4) INIT-C

(D12) END-

(C12) DCHADG-

(D4) RST-

(C4) MASET-

ADAPTER / FORMATTER COMMON BUS

R54 220 / R53 330	U31	75138	DBI15- (69)
R46 220 / R45 330	U30	75138	DBI14- (67)
R41 220 / R42 330	U30	75138	DBI13- (54)
R60 220 / R59 330	U33	75138	DBI12- (53)
R65 220 / R66 330	U35	75138	DBI11- (52)
R62 220 / R61 330	U33	75138	DBI10- (51)
R44 220 / R43 330	U30	75138	DBI09- (49)
R57 220 / R58 330	U33	75138	DBI08- (48)
R39 220 / R40 330	U30	75138	DBI07- (31)
R70 220 / R69 330	U35	75138	DBI06- (27)
R68 220 / R67 330	U35	75138	DBI05- (25)
R52 220 / R51 330	U31	75138	DBI04- (23)
R55 220 / R56 330	U33	75138	DBI03- (19)
R63 220 / R64 330	U35	75138	DBI02- (15)
R47 220 / R48 330	U31	75138	DBI01- (13)
R49 220 / R50 330	U31	75138	DBI00- (11)

+5V

C17 = 470PF

FIF

PU (R81)

R73 1K

WORD TRANSFER COUNTER

PROCESSOR DATA BUS

CORE MEMORY ADDRESS REGISTER

DATA 15-	(66)
DATA 14-	(56)
DATA 13-	(64)
DATA 12-	(59)
DATA 11-	(58)
DATA 10-	(75)
DATA 09-	(63)
DATA 08-	(60)
DATA 07-	(55)
DATA 06-	(95)
DATA 05-	(57)
DATA 04-	(61)
DATA 03-	(73)
DATA 02-	(82)
DATA 01-	(65)
DATA 00-	(62)

INTACK- (A4)

DIAGM (31)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWINGS
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS XX ± — XXX ± —
ANGLES ±
MATERIAL:

ENGINEER
CHECKED
DRAFTSMAN Richard 11-3-75

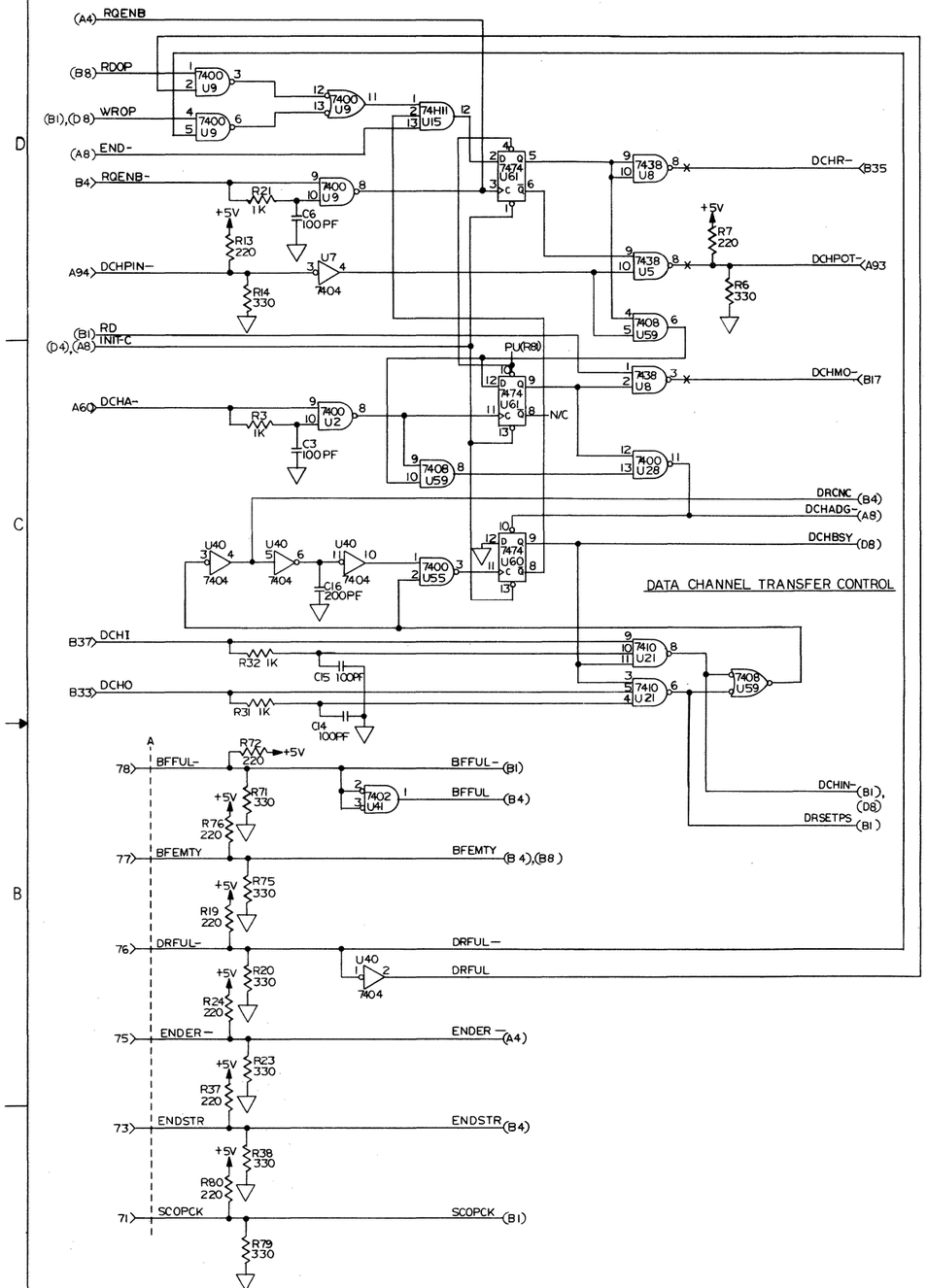
DATA DISC

DIAGRAM LOGIC
ADAPTOR BOARD

SIZE E | DRAWING NO. 1940027 | E

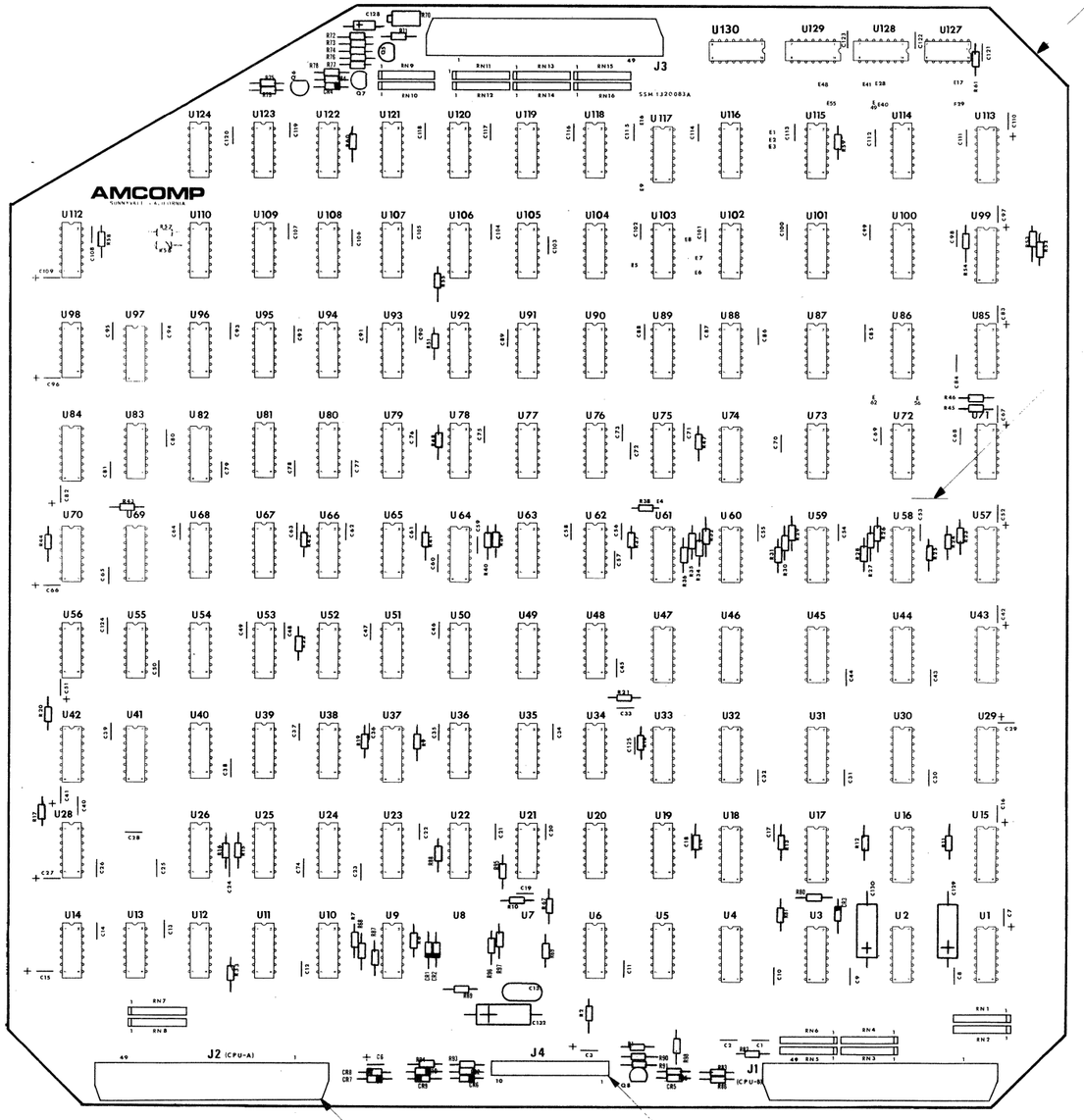
SCALE —

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	E	SEE SHEET 1		



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWINGS TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMALS .X ±— .XX ±— ANGLES ±— MATERIAL:		ENGINEER CHECKED DRAFTSMAN 11-4-75	DATA DISC DIAGRAM LOGIC ADAPTOR BOARD SIZE E · DRAWING NO. 1940027 · REV. E SCALE — · SHEET 3 OF 3

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE / BOM-13	1/17	



NOTES

1. IDENTIFY WITH M/L DASH NO. AND APPROPRIATE M/L REV PER 1550010.
2. MAXIMUM COMPONENT LEAD PROTRUSION ON CIRCUIT SIDE OF BOARD SHALL BE .06.
3. FOR SCHEMATIC DIAGRAM SEE DWG NO. 1940083.
4. SQUARE PAD DENOTES EMITTER OF TRANSISTOR.
5. WORKMANSHIP SHALL COMPLY WITH QA-100000-00.

(5)(3)

(3) REMOVE PIN 6 FROM CONNECTOR

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

USED ON	NEXT ASSY.
8010B	END ITEM

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX=± .XXX=±
ANGLES

MATERIAL: SEE M/L

FINISH

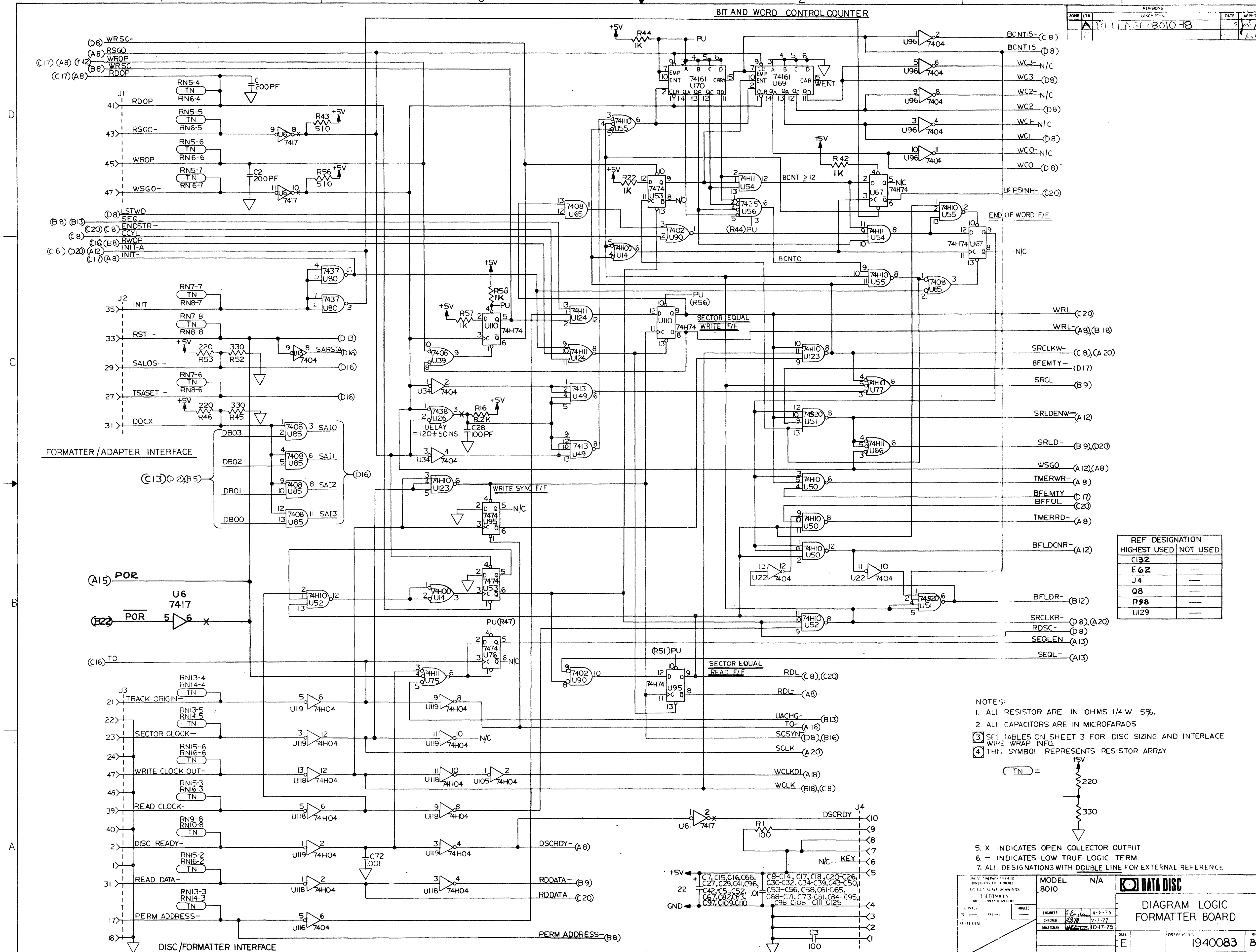
SIGNATURE		DATE
DFT.	Ron Bateman	1/20/77
CHK.	J.D.M.	2-7-77
APP.		2/8/77
APP.		

AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
ASSEMBLY- PRINTED WIRING BOARD
FORMATTER BOARD

SIZE	DRAWING NO.	REV.
D	1040083	A

SCALE 1/1 | PROJ. NO. 1620-00 | SHEET 1 OF 1



REF DESIGNATION	
HIGHEST USED	NOT USED
C132	—
E62	—
J4	—
Q8	—
R98	—
U129	—

NOTES:
1. ALL RESISTOR ARE IN OHMS 1/4 W 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. SEE TABLES ON SHEET 3 FOR DISC SIZING AND INTERLACE WIRE WRAP INFO.
4. THIS SYMBOL REPRESENTS RESISTOR ARRAY.
5. X INDICATES OPEN COLLECTOR OUTPUT
6. – INDICATES LOW TRUE LOGIC TERM.
7. ALL DESIGNATIONS WITH DOUBLE LINE FOR EXTERNAL REFERENCE

MODEL 8010 N/A

DATA DISC

DIAGRAM LOGIC FORMATTER BOARD

SIZE E 1940083 REV B

SHEET 1 OF 6

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE / APPROVED
		SEE SHEET 1	

READ ERROR

CRCC, PARITY AND SECTOR END CONTROL

ILLEGAL ADDRESS ERROR

TIME OUT O/S

DISC FAILURE DURING OPERATION

DATA TRANSFER ERROR

WRITE PROTECT ERROR

ANY ERROR

READ ERROR (CRC & PARITY)

ILLEGAL ADDRESS ERROR

TIMER ERROR (MODULAITY)

WRITE PROTECT ERROR

DISC FAIL (TIME OUT & READY)

FORMATTER ADAPTER COMMON BUS

READ F/F

PU R60

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DO NOT SCALE DRAWING. TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMALS .XX ±.01, .XXX ±.005, ANGLES ±	DATA DISC
MATERIAL:	DIAGRAM, LOGIC, FORMATTER BOARD
ENGINEER	
CHECKED	
DRAFTSMAN 10-17-75	
SIZE E	DRAWING NO. 1940083 REV B
SCALE —	SHEET 2 OF 6

REVISIONS		
ZONE	LTR	DESCRIPTION
		SEE SHEET 1

DATA REGISTER

16 WORD BUFFER

SHIFT REGISTER

(C17),(D4) WROP — U34 7404

(C17) DRSET — U34 7404

(D20) FLD- — U34 7404

(C4),(B5),(C13) DB00 DB01 DB02 DB03 — BF00- BF01- BF02- BF03- (D10) — U15 74298 — DR00 DR01 DR02 DR03 (B6)

(D9) SR00 SR01 SR02 SR03 — U29 74157 SEL — U43 7489 — +5V R25 510, R24 510, R23 510, R11 510 — BF00- BF01- BF02- BF03- (D12) — U57 74195 — SR00 SR01 SR02 SR03 (D11)

SR00 (B18)

(B13),(B5) DB04 DB05 DB06 DB07 — BF04- BF05- BF06- BF07- (C10) — U16 74298 — DR04 DR05 DR06 DR07 (B6)

(C9) SR04 SR05 SR06 SR07 — U30 74157 SEL — U44 7489 — +5V R28 510, R27 510, R26 510, R12 510 — BF04- BF05- BF06- BF07- (C12) — U58 74195 — SR04 SR05 SR06 SR07 (C11)

(C5) DB08 DB09 DB10 DB11 — BF08- BF09- BF10- BF11- (C10) — U17 74298 — DR08 DR09 DR10 DR11 (C6)

(C12),(C5)

(C9) SR08 SR09 SR10 SR11 — U31 74157 SEL — U45 7489 — +5V R31 510, R30 510, R29 510, R13 510 — BF08- BF09- BF10 BF11 (C12) — U59 74195 — SR08 SR09 SR10 SR11 (C11)

(D16),(D5) DB12 DB13 DB14 DB15 — BF12- BF13- BF14- BF15- (B10) — U18 74298 — DR12 DR13 DR14 DR15 (D6)

(B9) SR12 SR13 SR14 SR15 — U32 74157 SEL — U46 7489 — +5V R36 510, R34 510, R35 510, R14 510 — BF12- BF13- BF14 BF15 (B12) — U60 74195 — +5V R32 1K — SR12 SR13 SR14 SR15 (B11)

SRCL (C1)

SRLD- (C1)

RDDATA- (A3)

(B1) BFLDR-

(C17) BFLDPS- — U48 7408

+5V PU(R39) R37 150 — U62 7417 — C57 220PF — PU (R39)

BUFFER/DISC ACCESS COUNTER

U61 74161 — CLK ENP ENT LD CLR — QA QB QC QD

+5V R18 1K — +5V R21 150

(D20) DRSETBF- — U48 7408 — U62 7417 — C33 220PF

U33 74161 — CLK ENP ENT LD CLR — QA QB QC QD

U47 74157 SELCT STR — 1A 2A 3A 4A — 1B 2B 3B 4B

(C4) INIT-A

(A8),(C1) WSGO-

(C1) SRLDENW-

(B1) BFLDCNR- — U20 74H10

BUFFER/PROCESSOR ACCESS COUNTER

INTERLACE TABLE

FROM	AMCOMP FORMATT 1/1	2/1	4/1	8/1	NOVA FORMATT 1/1	2/1	4/1	8/1
E19 TO	E40	E37	E32	E31	E40	E37	E32	E53
E20 ▲	E39	E40	E37	E32	E39	E40	E37	E32
E17	E34	E39	E40	E37	E34	E39	E40	E37
E18	E33	E34	E39	E40	E33	E34	E39	E40
E23	E30	E33	E34	E39	E42	E33	E34	E39
E24	E29	E30	E33	E34	E51	E48	E33	E34
E21	E31	E29	E30	E33	E43	E44	E48	E33
E22 ▼	E32	E31	E29	E30	E32	E53	E44	E48
E27 TO	E37	E32	E31	E29	E37	E32	E53	E44
E45	NO CONNECTION				E30	E30	E30	E30
E41	▲		▲		E29	E29	E29	E29
E49					E31	E31	E31	E31
E50					E55	E55	E55	E55
E46					E55	E55	E55	E55
E42					E55	E55	E55	E55
E51					E55	E55	E55	E55
E43					E25	E25	E25	E25
E47	▼		▼		E38	E38	E38	E38
E52	NO CONNECTION				E28	E28	E28	E28

STRAPPING

8400	8500
E56 TO E57	E56 TO E59
E59 TO E61	E61 TO E58
E58 TO E62	E62 TO E60

[3]

DISC SIZE 8400	8500		MAX SIZE JUMPER TO	FROM
0	128	TRACK	E2	E9 E10 E11 E12 E13 E14 E15 E16
16	144		▲	▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲
32	160			E14
48	176			E13
64	192			E12
80	208			E11
96	224			E10
112	240	TRACK	E2	E9

[3]

HIGHEST UNIT NO. ASSIGNED	ILLEGAL UNIT JUMPER TO	FROM
0	E3	E7 E6 E5
1	E3	E6 E7
2	E3	E7
3	NONE	

UNIT NO.	UNIT SELECT JUMPER TO	FROM
0	E8	E1
1	E7	E1
2	E5	E1
3	E6	E1

[3]

NOTE: FOR MULTIPLE UNITS OF DIFFERENT SIZE (IE NUMBER OF TRACKS AND ONLY TWO DIFFERENT SIZES) THE UNIT HAVING FEWEST TRACKS MUST BE ASSIGNED HIGHEST UNIT NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWINGS
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS .XX ±.— .XXX ±.— ANGLES ±—
MATERIAL:
ENGINEER
CHECKED
DRAFTSMAN 10-17-75

DATA DISC

DIAGRAM LOGIC FORMATTER BOARD

SIZE E | DRAWING NO. 1940083 | REV B

SCALE — | SHT 3 OF 6

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SECTOR ADDRESS REGISTER

TRACK AND UNIT ADDRESS REGISTER

DISC SIZE MAX TRACK

UNIT CHANGE F/F

SECTOR COUNTER DISC

HEAD CHANGE

16 TRACKS
32 TRACKS
64 TRACKS
128 TRACKS
256 TRACKS

TO DISCS

DRAWN	
CHECKED	
ENGINEER	
DRAFTSMAN	10-17-75

DATA DISC

DIAGRAM LOGIC FORMATTER BOARD

SIZE	DRAWING NO.	REV
E	1940083	B

SCALE — SHEET 4 OF 6

20 19 18 17

BUFFER CONTENTS COUNTER

BUFFER AND DR TRANSFER CONTROL

CYCLIC CODE GENERATOR

PARITY BIT GENERATOR

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(A12),(C4) INIT-A
(A12) DRSETBF-
(C1) SRLD-
(D12) BFLD-
J2 39 BUFFS
41 DRSETPS-
43 DRAVL-
(B1) BFFUL
(D16),(C8) PTYCYL-
(C8),(D4) ENDSTR-
(D1) BFPSINH-
(C8) CCYL
(C8),(B2) RDL
(A2) RDDATA
(C1) WRL
(A2) SCLK
(B1),(D8) SRCLKR-
(C8),(C1) SRCLKW-

BUFFER FULL--
BUFFER EMPTY
BUFFER FULL
USED DURNING READ
USED DURING WRITE
INTR CLK F/F
BUFFER CONDITION DECODER
PUV (P.U.)

BFEMTY- (C1)
BFEMTY (B1)
J2
BFFUL- 21
BFEMTY 19
DRFUL- 17
(C8) ENDSTR 15
(C8) ENDSTR 13
(D8) SCOPCK 11
INIT- (C4),(B8)
DRSET (D12)
BFLDPS- (B12)
WRQP (D12),(D4),(A12)
RDQP (D4),(A8)

(C8),(A2) WCLK
(A8),(C1) WRL-
(D9) SROO
(C8) CCYL-
(C8) PTYCLY
(D13) (A16) TA0 TA1 TA2 TA3
(A2) WCLKDI
PU(R60)
J3
WRITE- 29
N/C 30
WRITE DATA 35 36
TRACK ADDRESS 0- 11
TRACK ADDRESS 1- 10
TRACK ADDRESS 2- 9
TRACK ADDRESS 3- 8
TO DISC
SECTOR WRITE- 25
WRITE CLOCK IN- 26 43 44

CCGNZR (D8)
PTY (D8)
PU(R44)
PU R64
PU R44
PU R48
PU R60
PUV R48
+5V
R20 1K
R17 150
R2 150
C40 220PF
R10 62K
C19 .001
R51 1K
R60 1K
R67 470
RN7-5 TN RN8-5
RN7-4 TN RN8-4
RN7-3 TN RN8-3
RN9-7 TN RN10-7
RN12-5 TN RN11-5
RN11-4 TN RN12-4
RN11-3 TN RN12-3
RN11-2 TN RN12-2
RN13-7 TN RN14-7
RN15-4 TN RN16-4

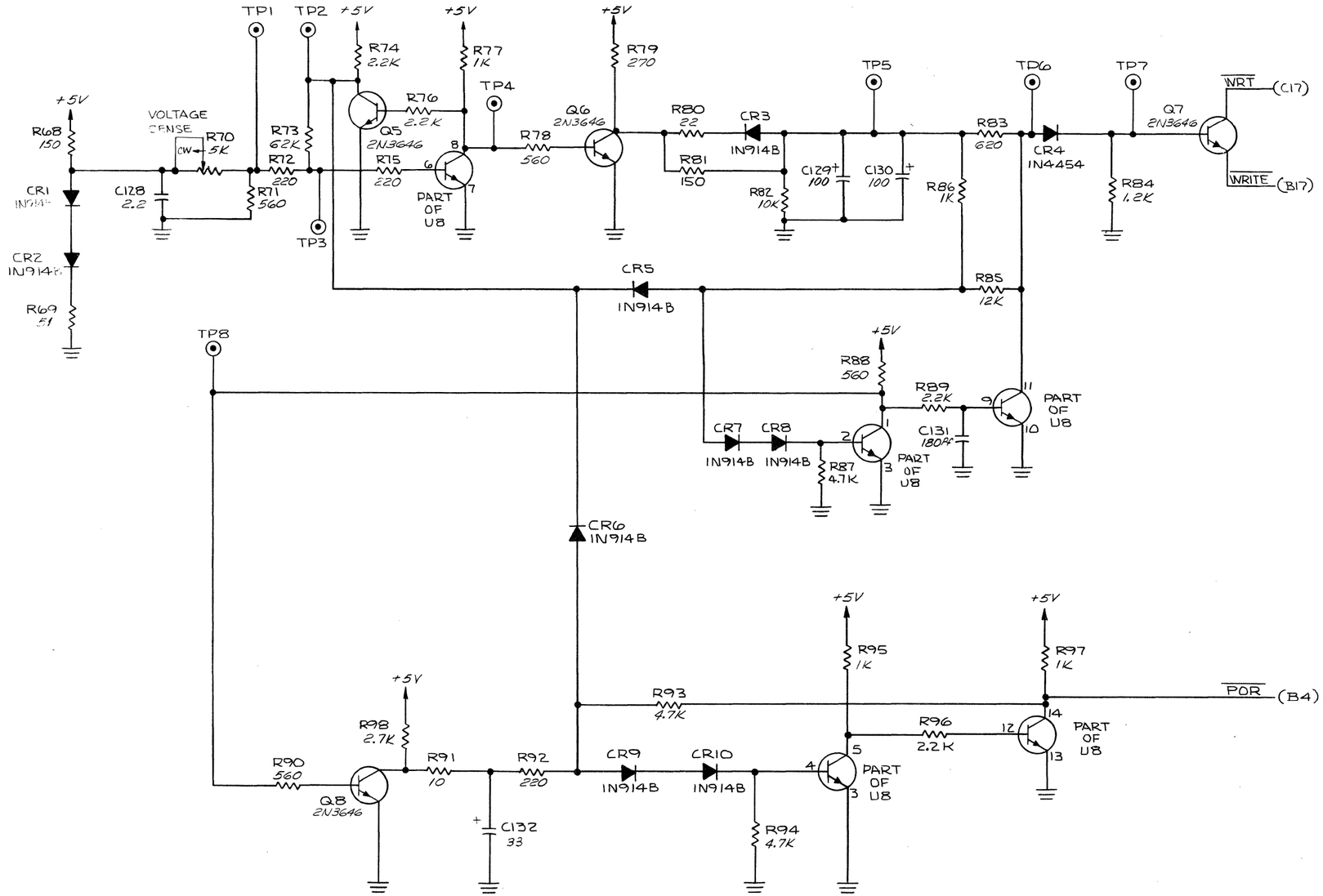
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWINGS
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS .XX .XXX ANGLES
MATERIAL:
ENGINEER
CHECKED
DRAFTSMAN 10-17-75

DATA DISC

DIAGRAM LOGIC FORMATTER BOARD

SIZE E | DRAWING NO. 1940083 | REV. B
SCALE — | SHEET 5 OF 6

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	B	SEE SHT 1		



QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

USED ON | NEXT ASSY. | APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX=± .XXX=± | ANGLES
MATERIAL
FINISH

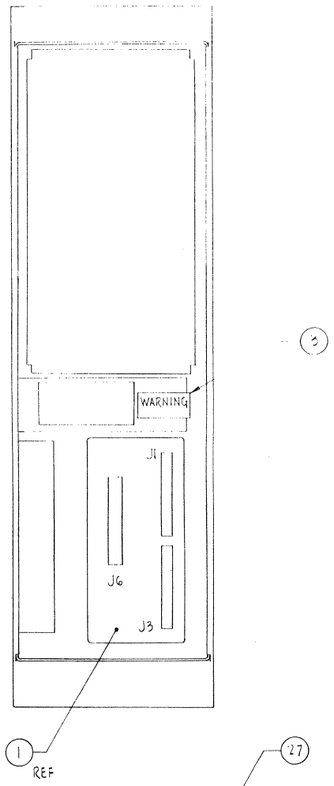
SIGNATURE	DATE
DFT.	
CHK.	
APP.	
APP.	

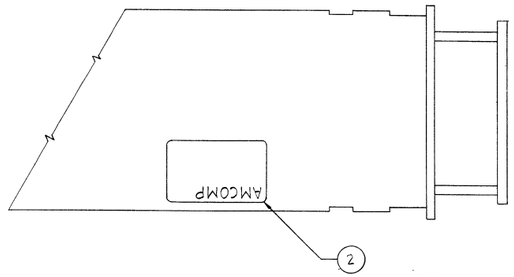
AMCOMP
SUNNYVALE, CALIFORNIA

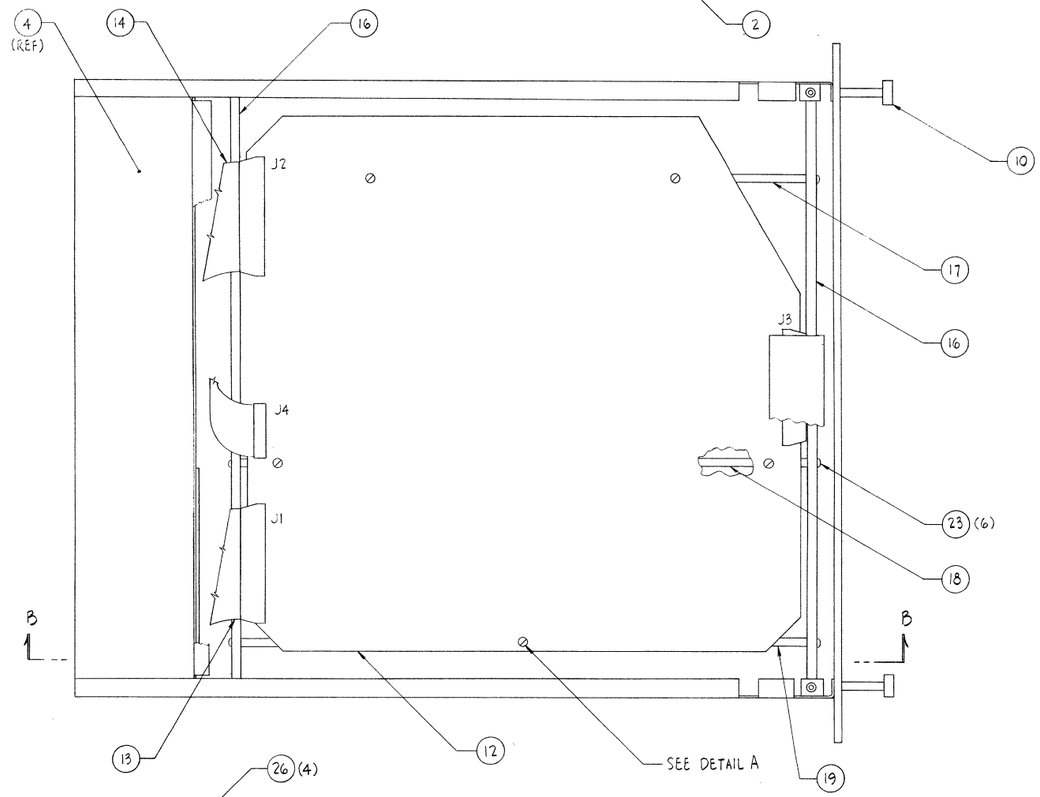
TITLE
DIAGRAM LOGIC
FORMATTER BOARD

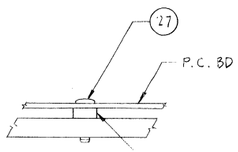
SIZE D | DRAWING NO. 1940083 | REV. B
SCALE ——— | PROJ. NO. 16'CCO | SHEET 6 OF 6

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE/3019-13	12-17	JAC

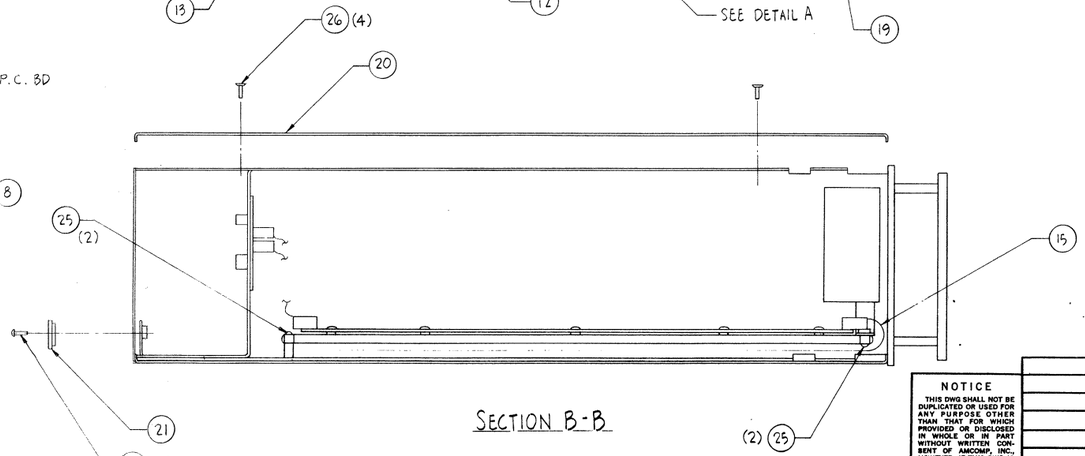








DETAIL A TYP 5 PLCS
SCALE 1/1



SECTION B-B

NOTES

1. THIS ASSEMBLY SHALL BE IDENTIFIED BY ITS M/L NO. 1020129-01 PER 1550010.
2. WORKMANSHIP TO COMPLY WITH QA 100000-00.

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

USED ON	NEXT ASSY.
8010B	END ITEM

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX±, .XXX±, ANGLES
MATERIAL
FINISH

	SIGNATURE	DATE
DFT.	Carl Nielsen	12-10-76
CHK.	J. St. Mascis	12-21-76
APP.		2/8/77
APP.	JAC	

AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
CONTROLLER ASSEMBLY

SIZE	DRAWING NO.	REV.
D	1020129	A

SCALE 1/2 | PROJ. NO. 1620-00 | SHEET 1 OF 1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE		

J1		J2
1		1
2		2
3		3
4		4
5		5
6		6
7		7
8		8
9	DB00-	9
10		10
11	DB01-	11
12		12
13	DB02-	13
14		14
15	DB03-	15
16		16
17	DB04-	17
18		18
19	DB05-	19
20		20
21	DB06-	21
22		22
23	DB07-	23
24		24
25	DB08-	25
26		26
27	DB09-	27
28		28
29	DB10-	29
30		30
31	DB11-	31
32		32
33	DB12-	33
34		34
35	DB13-	35
36		36
37	DB14-	37
38		38
39	DB15-	39
40		40
41	RDOP	41
42		42
43	RSGO-	43
44		44
45	WROPA	45
46		46
47	WSGO-	47
48		48
49		49
50		50

J3		J4
1		1
2		2
3		3
4		4
5		5
6		6
7		7
8		8
9		9
10		10
11	SCOPCK-	11
12		12
13	ENDSTR-	13
14		14
15	ENDER	15
16		16
17	DRFUL-	17
18		18
19	BFEMTY	19
20		20
21	BFFUL	21
22		22
23	DRGAT-	23
24		24
25		25
26		26
27	TSASET-	27
28		28
29	SALOS-	29
30		30
31	DOCX	31
32		32
33	RST-	33
34		34
35	INIT	35
36		36
37		37
38		38
39	BUFFS	39
40		40
41	DRSETPS-	41
42		42
43	DRAYL-	43
44		44
45		45
46		46
47		47
48		48
49		49
50		50

J5		J6
1	GND	1
2	DISC READY-	2
3	TRACK ADDRESS 8-	3
4	TRACK ADDRESS 7-	4
5	TRACK ADDRESS 6-	5
6	TRACK ADDRESS 5-	6
7	TRACK ADDRESS 4-	7
8	TRACK ADDRESS 3-	8
9	TRACK ADDRESS 2-	9
10	TRACK ADDRESS 1-	10
11	TRACK ADDRESS 0-	11
12	USEL 3-	12
13	USEL 2-	13
14	USEL 1-	14
15	USEL 0-	15
16		16
17	PERM ADDRESS-	17
18	GND	18
19		19
20		20
21	TRACK ORIGIN-	21
22	GND	22
23	SECTOR CLOCK-	23
24	GND	24
25	SECTOR WRITE-	25
26	GND	26
27	READ	27
28	GND	28
29	WRITE-	29
30	GND	30
31	READ DATA-	31
32		32
33		33
34		34
35	WRITE DATA	35
36	GND	36
37		37
38		38
39	READ CLOCK-	39
40	GND	40
41		41
42		42
43	WRITE CLOCK IN-	43
44	GND	44
45		45
46		46
47	WRITE CLOCK OUT-	47
48	GND	48
49		49
50		50

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

NOTICE

THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC., HOWEVER; IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

8010B	1040080
USED ON	NEXT ASSY.

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX±, .XXX±, ANGLES

MATERIAL

FINISH

	SIGNATURE	DATE
DFT.	Ron Bateman	12 1 76
CHK.		
APP.	Joel	4/8/77
APP.		

AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
SCHEMATIC DIA-POWER WIRING BD
CONNECTOR INTERFACE BD

SIZE	DRAWING NO.	REV.
D	1940080	A

SCALE —— PROJ. NO. [illegible] SHEET 1 OF 1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE / 8010-B	2/77	JE NG

J1		J2
1		1
2		2
3		3
4		4
5		5
6		6
7		7
8	DB00-	8
9		9
10	DB01-	10
11		11
12	DB02-	12
13		13
14	DB03-	14
15		15
16	DB04-	16
17		17
18	DB05-	18
19		19
20	DB06-	20
21		21
22	DB07-	22
23		23
24	DB08-	24
25		25
26	DB09-	26
27		27
28	DB10-	28
29		29
30	DB11-	30
31		31
32	DB12-	32
33		33
34	DB13-	34
35		35
36	DB14-	36
37		37
38	DB15-	38
39		39
40	RDOP	40
41		41
42	RSGO-	42
43		43
44	WROPA	44
45		45
46	WSGO-	46
47		47
48		48
49		49
50		50

J3		J4
1		1
2		2
3		3
4		4
5		5
6		6
7		7
8		8
9		9
10		10
11	SCOPCK-	11
12		12
13	ENDSTR-	13
14		14
15	ENDER	15
16		16
17	DRFUL-	17
18		18
19	BFEMTY	19
20		20
21	BFFUL	21
22		22
23	DRGAT-	23
24		24
25		25
26		26
27	TSASET-	27
28		28
29	SALOS-	29
30		30
31	DOCX	31
32		32
33	RST-	33
34		34
35	INIT	35
36		36
37		37
38		38
39	BUFFS	39
40		40
41	DRSETPS-	41
42		42
43	DRAYL-	43
44		44
45		45
46		46
47		47
48		48
49		49
50		50

J5		J6
1		1
2		18
3		34
4	TRACK ADDRESS 7-	35
5	TRACK ADDRESS 6-	2
6	TRACK ADDRESS 5-	19
7	TRACK ADDRESS 4-	3
8	TRACK ADDRESS 3-	20
9	TRACK ADDRESS 2-	36
10	TRACK ADDRESS 1-	37
11	TRACK ADDRESS 0-	4
12	USEL 3	21
13	USEL 2	5
14	USEL 1	22
15	USEL 0-	38
16		39
17		6
18		23
19		7
20		24
21	TRACK ORIGIN-	40
22	GND	41
23	SECTOR CLOCK-	8
24	GND	25
25	SECTOR WRITE-	9
26	GND	26
27	READ	42
28	GND	43
29	WRITE-	10
30	GND	27
31	READ DATA-	11
32		28
33		
34		
35	WRITE DATA	12
36	GND	29
37		
38		
39	READ CLOCK-	46
40	GND	47
41		14
42		31
43	WRITE CLOCK IN-	15
44	GND	32
45		
46		
47	WRITE CLOCK OUT-	16
48	GND	33
49		17
50		50

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

8010B	1040081
USED ON	NEXT ASSY.

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX=±, .XXX=± | ANGLES
MATERIAL
FINISH

SIGNATURE		DATE
DFT.	RON BATEMAN	12 2 76
CHK.		
APP.	Joe	2/4/77
APP.		

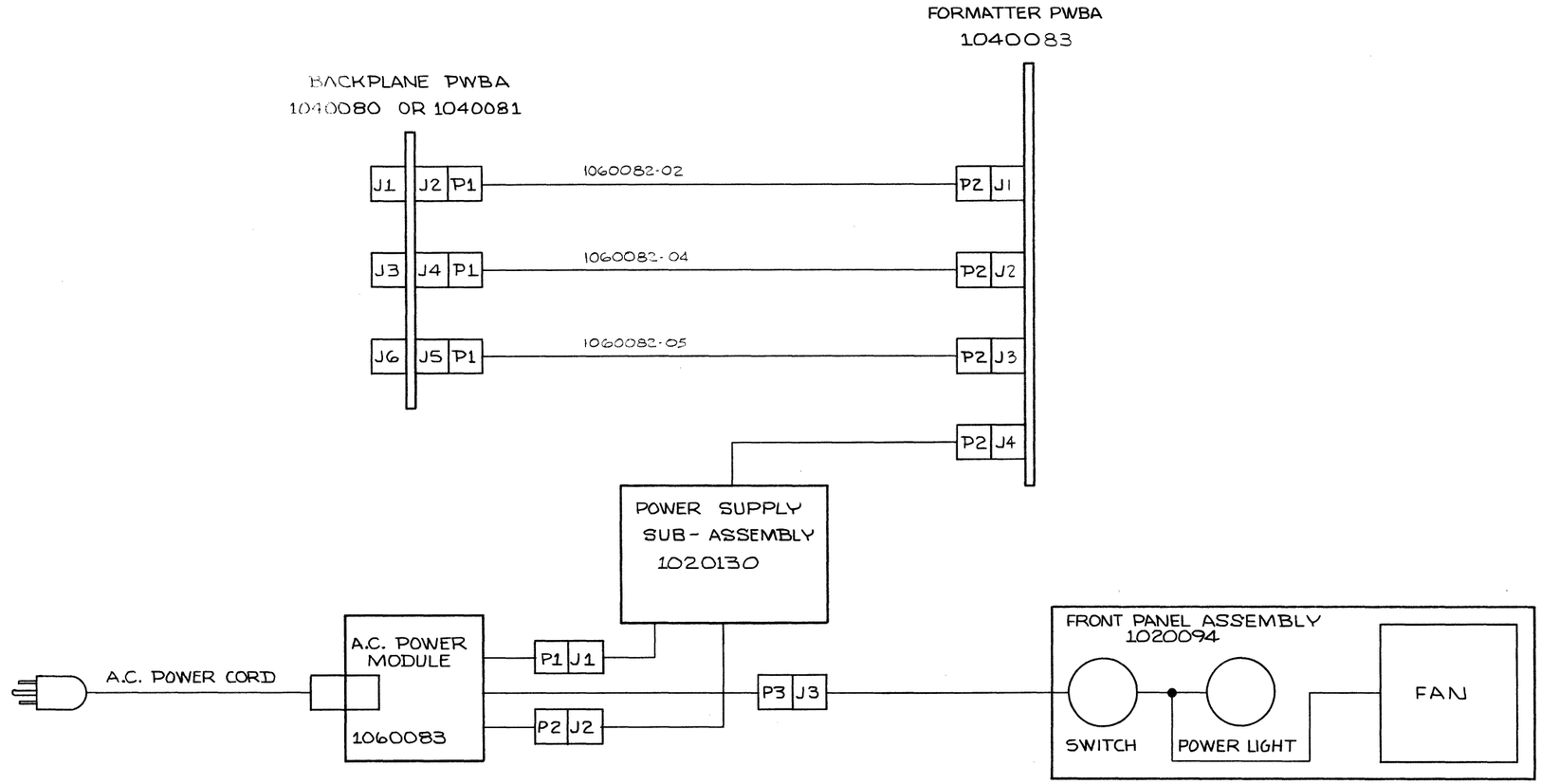
AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
SCHEMATIC DIA-POWER WIRING BD
"D" CONNECTOR INTERFACE BOARD

SIZE	DRAWING NO.	REV.
D	1940081	A

SCALE ——— | PROJ. NO. 1620-00 | SHEET 1 OF 1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE/3[illegible]	4/11/77	[illegible]



QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

USED ON	NEXT ASSY.
8010B	END ITEM

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX±, .XXX±, ANGLES
MATERIAL
FINISH

	SIGNATURE	DATE
DFT.	Ron Bateman	12 8 76
CHK.		
APP.	[illegible]	2/2/77
APP.		

AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
SYSTEM INTERCONNECT DIAGRAM
8010 B

SIZE	DRAWING NO.	REV.
D	1930025	A

SCALE NONE | PROJ. NO. 1620-00 | SHEET 1 OF 1

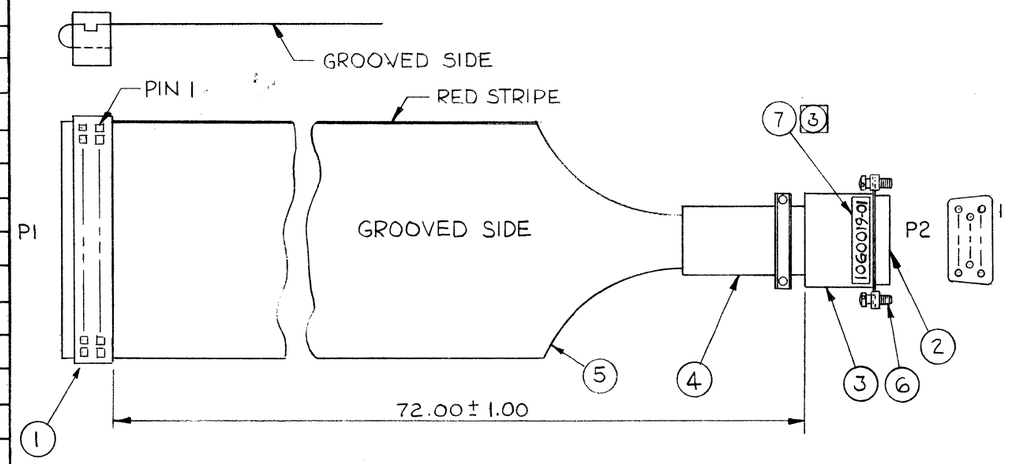
WIRE LEAD LIST

ITEM REQD FROM LM	WIRE GAGE COND	NO.	FROM STA	FROM COMP	FROM PIN	TO STA	TO COMP	TO PIN	REMARKS	FUNCTION

NOTES:

1. CONNECT AS FOLLOWS: P1/1 TO P2/1 ETC. THRU P1/50 TO P2/50
2. WORKMANSHIP SHALL COMPLY WITH QA100000-00
3. IDENTIFY WITH ASSY NO 1060019-01 & REV.

RELEASE LEVEL = ENGR □ LIMITED □ PROD			
REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	PRE-PROD. REL/3400-22	[illegible]	[illegible]
B	SEE EO 8177	[illegible]	[illegible]



NO.	PART NO.	DESCRIPTION	REF DES	MFR	PART NO.	CODE IDENT	QTY REQD
7	229-168	LABEL, ADHESIVE BACK					1
6	089-054	LOCK SCREW ASSY					2
5	195-533	CABLE, FLAT, 50 CONDUCT.					A/R
4	087-900	BOOT, TELESCOPING					1
3	089-053	SHELL, JUNCTION					1
2	089-052	CONNECTOR, 50 PIN	P2				1
1	089-829	CONNECTOR, 50 PIN	P1				1

LIST OF MATERIAL

1020019	8010
1020018	DDS
N/A	USED ON
APPLICATION	

UNLESS NOTED: DIMENSIONS ARE IN IN. & INCLUDE FIN. CHEMICAL OR PLATED. TOL ± .XX .XXX FRAC. — — —. DO NOT SCALE DWG

SIGNATURE		DATE
DWN	[signature]	4/29/75
CHK		[illegible]
ENG	[signature]	[illegible]
APPD	[signature]	[illegible]

MATL —

FIN —

DATA DISC INCORPORATED Palo Alto, Calif.

TITLE: CABLE ASSY, CPU CONTROLLER

SIZE	CODE IDENT	DWG NO.	REV
C		1060019	B

SCALE 1/1 X000346 SHEET 1 OF 1

PRINTED ON DIEPO NO. 1000H
D.D.I. 117

WIRE LEAD LIST

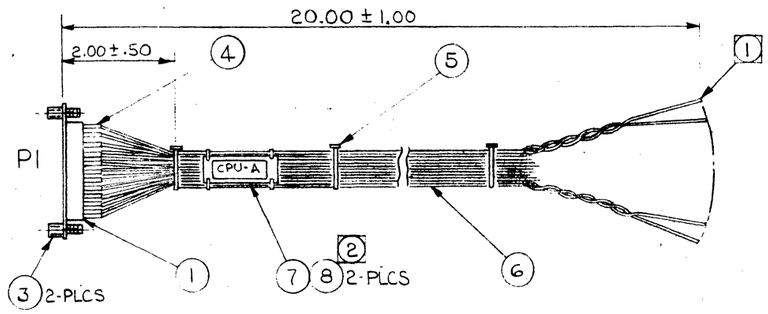
ITEM FROM	REQD	LM	WIRE GAGE COND	NO.	FROM STA	FROM COMP	FROM PIN	TO STA	TO COMP	TO PIN	REMARKS	FUNCTION
						P1	9		MARKER	69	YEL T.P	(CCYL-)
							10		GND		BLU	
							11		MARKER	71	YEL T.P	(SCDPCK)
							12		GND		BLU	
							13		MARKER	73	YEL TP	(ENDSTR)
							14		GND		BLU	
							15		MARKER	75	YEL TP	(ENDER)
							16		GND		BLU	
							17		MARKER	76	YEL TP	(DRFUL-)
							18		GND		BLU	
							19		MARKER	77	YEL TP	(BFEMTY)
							20		GND		BLU	
							21		MARKER	78	YEL TP	(BFFUL)
							22		GND		BLU	
							23		MARKER	79	YEL TP	(DRGAT-)
							24		GND		BLU	
							25		MARKER	81	YEL TP	(STATIN)
							26		GND		BLU	
							27		MARKER	83	YEL TP	(TSASET-)
							28		GND		BLU	
							29		MARKER	85	YEL TP	(SALOS-)
							30		GND		BLU	
							31		MARKER	86	YEL TP	(DOCX)
							32		GND		BLU	
							33		MARKER	87	YEL TP	(RST-)
							34		GND		BLU	
							35		MARKER	88	YEL TP	(INIT)
							36		GND		BLU	
							37		MARKER	89	YEL TP	(SPARE)
							38		GND		BLU	
							39		MARKER	90	YEL TP	(BUFFS)
							40		GND		BLU	
							41		MARKER	91	YEL TP	(DRSETPS-)
							42		GND		BLU	
							43		MARKER	92	YEL TP	DRAVL -
							44		GND		BLU	
							45		MARKER	61	YEL TP	SPARE
						P1	46		GND		BLU	

NOTES:
1. ATTACH WIRE MARKER TO SIGNAL END (YELLOW WIRE), OF EACH TWISTED PAIR, AS PER WIRE LEAD LIST.
2. TYPE IN CHARACTERS AS SHOWN.
3. WORKMANSHIP SHALL COMPLY WITH QA100000-00
4. IDENTIFY WITH ASSY NO. 1060024-01 & LATEST REV THIS DWG.

RELEASE LEVEL = ENGR ☐ LIMITED ☐ PROD ☐

REVISIONS

LTR	DESCRIPTION	DATE	APPD
A	PRE-PROD REL. 8010-02	3-3-75	



NO.	PART NO.	DESCRIPTION	REF DES	MFR	PART NO.	CODE IDENT	QTY REQD
8	229-176	MARKER PLATE, CABLE IDENT					2
7	229-168	LABEL, SELF ADHESIVE					1
6	192-027	WIRE, SOLID, T/PR. 26G, BLU/YEL					A/R
5	075-002	TIE WRAP					A/R
4	192-201	TUBING, SHRINK					A/R
3	089-207	SCREW JACK, FEMALE					2
2							
1	089-055	CONNECTOR, 50 PIN	P1				1

LIST OF MATERIAL

NOTICE

THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC., HOWEVER; IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

10200019	8010
N/A	USED ON
APPLICATION	

UNLESS NOTED DIMENSIONS ARE IN IN. & INCLUDE FIN. CHEMICAL OR PLATED
TOL .XX .XXX FRAC.
DO NOT SCALE DWG

	SIGNATURE	DATE
DWN	R. Simpson	3/6/75
CHK		
ENG	W. S. Gibb	3/6/75
APPD	W. S. Gibb	3/6/75

MATL —
FIN —

DATA DISC INCORPORATED Palo Alto, Calif.

TITLE CABLE ASSY, CPU 'A'

SIZE C | CODE IDENT | DWG NO. 1060024

SCALE 1/2 | SHEET 1 OF 1

PRINTED ON DIEPO NO. 1000H
D.D.I. 117

A 1-82

WIRE LEAD LIST

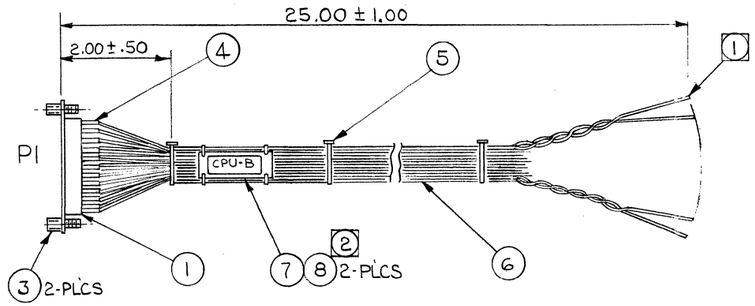
ITEM REQD FROM LM	WIRE GAGE COND	NO.	FROM STA	FROM COMP	FROM PIN	TO STA	TO COMP	TO PIN	REMARKS	FUNCTION
				P1	7		MARKER	6	YEL TP	SPARE
					8		GND		BLU	
					9		MARKER	11	YEL TP	DB00-
					10		GND		BLU	
					11		MARKER	13	YEL TP	DB01-
					12		GND		BLU	
					13		MARKER	15	YEL TP	DB02-
					14		GND		BLU	
					15		MARKER	19	YEL TP	DB03-
					16		GND		BLU	
					17		MARKER	23	YEL TP	DB04-
					18		GND		BLU	
					19		MARKER	25	YEL TP	DB05-
					20		GND		BLU	
					21		MARKER	27	YEL TP	DB06-
					22		GND		BLU	
					23		MARKER	31	YEL TP	DB07-
					24		GND		BLU	
					25		MARKER	48	YEL TP	DB08-
					26		GND		BLU	
					27		MARKER	49	YEL TP	DB09-
					28		GND		BLU	
					29		MARKER	51	YEL TP	DB10-
					30		GND		BLU	
					31		MARKER	52	YEL TP	DB11-
					32		GND		BLU	
					33		MARKER	53	YEL TP	DB12-
					34		GND		BLU	
					35		MARKER	54	YEL TP	DB13-
					36		GND		BLU	
					37		MARKER	67	YEL TP	DB14-
					38		GND		BLU	
					39		MARKER	69	YEL TP	DB15-
					40		GND		BLU	
					41		MARKER	34	YEL TP	RDOP
					42		GND		BLU	
					43		MARKER	38	YEL TP	RSGO-
				P1	44		GND		BLU	

NOTES:
1. ATTACH WIRE MARKER TO SIGNAL END (YELLOW WIRE), OF EACH TWISTED PAIR, AS PER WIRE LEAD LIST.
2. TYPE IN CHARACTERS AS SHOWN.
3. WORKMANSHIP SHALL COMPLY WITH QA100000-00
4. IDENTIFY WITH ASSY NO. 1060025-01 & LATEST REV THIS DWG.

RELEASE LEVEL = ENGR ☐ LIMITED ☐ PROD ☐

REVISIONS

LTR	DESCRIPTION	DATE	APPD
A	PRE-PROD REL. 8010-02	3/3/75	



NO.	PART NO.	DESCRIPTION	REF DES	MFR	PART NO.	CODE IDENT	QTY REQD
8	229-176	MARKER PLATE, CABLE IDENT					2
7	229-168	LABEL, SELF ADHESIVE					1
6	192-027	WIRE, SOLID, T/PR, 26G, BLU/YEL					A/R
5	075-002	TIE WRAP					A/R
4	192-201	TUBING, SHRINK					A/R
3	089-207	SCREW JACK, FEMALE					2
2							
1	089-055	CONNECTOR, 50 PIN	P1				1

LIST OF MATERIAL

NOTICE

THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC., HOWEVER: IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

UNLESS NOTED	SIGNATURE	DATE
DIMENSIONS ARE IN IN. & INCLUDE FIN. CHEMICAL OR PLATED	DWN R. Simpson	3/6/75
	CHK	
TOL ± .XX .XXX FRAC. — — —	ENG [illegible]	3/6/75
DO NOT SCALE DWG	APPD [illegible]	3/6/75

1020019 8010
N/A USED ON APPLICATION

MATL —

FIN —

DATA DISC INCORPORATED Palo Alto, Calif.

TITLE CABLE ASSY, CPU 'B'

SIZE C | CODE IDENT | DWG NO. 1060025

SCALE 1/2 | SHEET 1 OF 2

PRINTED ON DIEPO NO. 1000H
D.D.I. 117

WIRE LEAD LIST

ITEM REQD FROM LM	WIRE GAGE COND	NO.	FROM STA	FROM COMP	FROM PIN	TO STA	TO COMP	TO PIN	REMARKS	FUNCTION
				P1	45		MARKER	40	YEL TP	WROP
					46		GND		BLU	
					47		MARKER	36	YEL TP	WSGO-
					48		GND		BLU	

RELEASE LEVEL = ENGR ☐ LIMITED ☐ PROD ☐			
REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	SEE SHT 1	—	—

NO.	PART NO.	DESCRIPTION	REF DES	MFR	PART NO.	CODE IDENT	QTY REQD

LIST OF MATERIAL

N/A USED ON APPLICATION

UNLESS NOTED
DIMENSIONS ARE IN IN. & INCLUDE FIN. CHEMICAL OR PLATED
TOL ± .XX — .XXX — FRAC. —
DO NOT SCALE DWG

SIGNATURE	DATE
DWN	
CHK	
ENG	
APPD	

MATL —
FIN —

DATA DISC INCORPORATED Palo Alto, Calif.

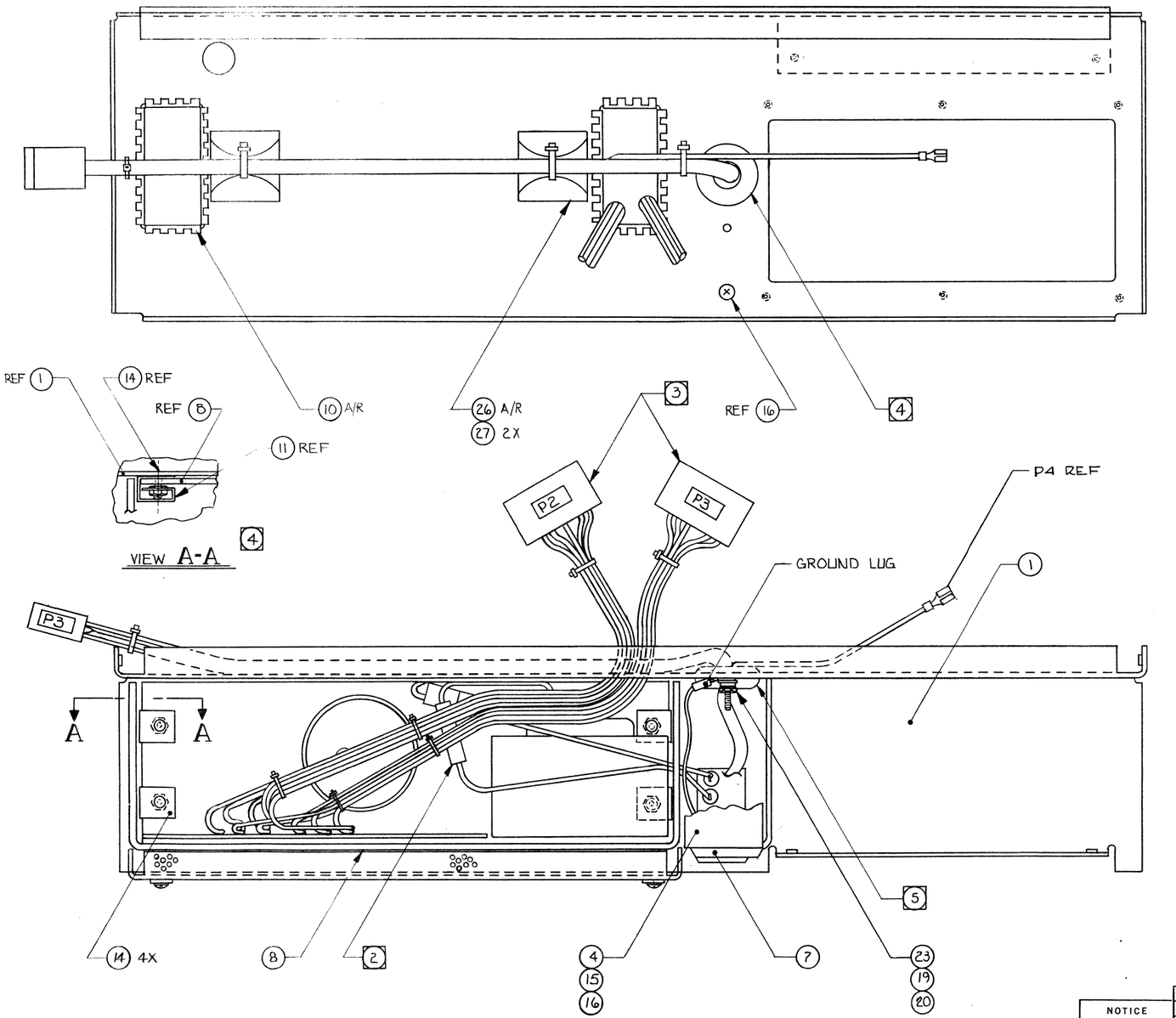
TITLE — CABLE ASSY, CPU 'B'

SIZE C | CODE IDENT | DWG NO. 1060025

SCALE — | SHEET 2 OF 2

PRINTED ON DIEPO NO. 1000H
D.D.I. 117

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A			
	B	SEE ECO 50245		
	C	SEE ECO 50271		



4. ROUTE HARNESS AND CONNECTOR (P3) THRU .75 DIA. CUTOUT THEN FIT GROMMET INTO CUTOUT IN ITEM 1 AS SHOWN.

3. ROUTE HARNESS AND CONNECTORS P2 & P3 THRU 1.0" x 2.0" CUTOUT IN ITEM 1 AS SHOWN.

2. ROUTE HARNESS AND CONNECTOR P1 & P2 THRU UPPER SLOT IN ITEM 8 AS SHOWN AND CONNECT P1 & P2 WITH J1 & J2 RESPECTIVELY.

1. IDENTIFY WITH ASSY PART NO. 1020093-02 AND CURRENT M/L REVISION PER 1550010.

NOTES:

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

8020	1020095
USED ON	NEXT ASSY.

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS XX± — XXX± — ANGLES —

MATERIAL

FINISH

SIGNATURE	DATE
DFT. James A. Peterson	4/30/76
CHK. W. Rivas	4/30/76
APP.	7-7-76
APP.	

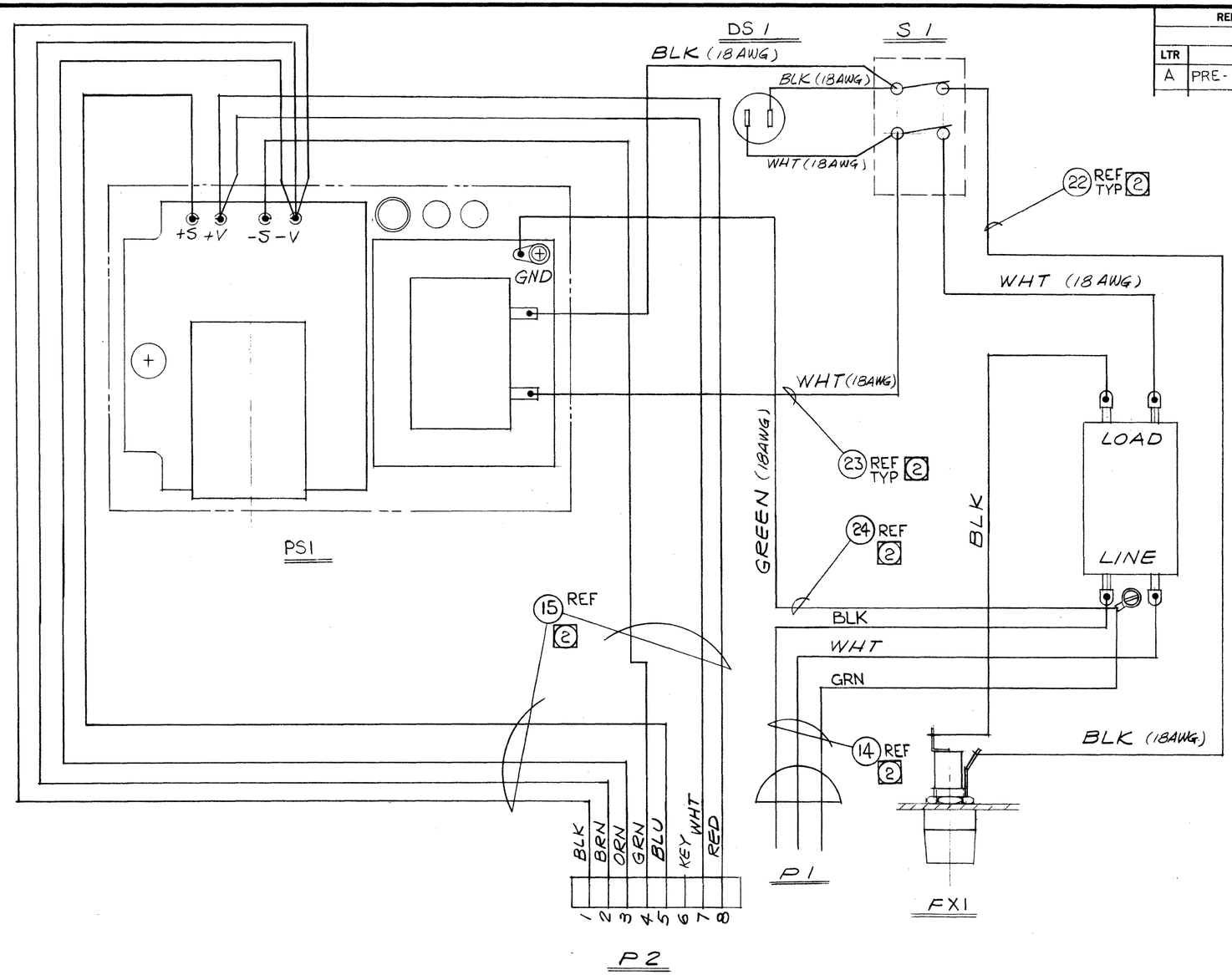
DATA DISC INCORPORATED

TITLE
PANEL ASSY, REAR

SIZE	DRAWING NO.	REV.
D	1020093	C

SCALE 1/1 | PROJ. NO. | SHEET 1 OF 1

RELEASE LEVEL = ENGR ☐ LIMITED ☐ PROD ☐			
REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	PRE-PROD. REL 8010-02	3/13/75	



2 ITEMS ARE AS LISTED ON DWG & M/L 1020020.

1 REMOVE JUMPER BETWEEN +S AND +V ; -S AND -V PRIOR TO ASSEMBLY.

NOTES:

NO	PART NO	DESCRIPTION	REF DES	MFR	PART NO	CODE IDENT
QTY REQD	LIST OF MATERIAL					

UNLESS NOTED	SIGNATURE	DATE
DIMENSIONS ARE IN IN. & INCLUDE FIN, CHEMICAL OR PLATED	DWN E. WONG	8-29-74
TOL ± XX .— XXX .— ANG .—	CHK E.W	12-18-74
DO NOT SCALE DWG	ENG [illegible]	3-5-75
	APPD [illegible]	3-14-75

1020020 8010

N/A USED ON APPLICATION

MATL —

FIN —

DATA DISC INCORPORATED SUNNYVALE CALIF

TITLE WIRING DIAGRAM-POWER SUPPLY

SIZE C | CODE IDENT | DWG NO. 1930003

SCALE ~ | X00035[illegible]-00 | SHEET 1 OF 1

PRINTED ON DIEPO NO. 10004-10 CLEARPRINT FADE-OUT 7-68

APPENDIX A

USER'S GUIDE

FOR

8010 DISC MEMORY SYSTEM DIAGNOSTIC PROGRAM

USER'S GUIDE FOR 8010 DISC MEMORY

SYSTEM DIAGNOSTIC PROGRAM

A-1 INTRODUCTION

The 8010 Disc System Diagnostic Program is a maintenance program designed to test the AMCOMP 8010 Disc Memory System. Minimum machine requirements include a standard Nova processor with 8K of read/write memory, an AMCOMP 8010 Disc Memory System, and a teletype. Sufficient flexibility has been designed into this program to allow a wide range of disc system testing. The user may choose test functions as widely varied as looping on single bit exercises suitable for scope loops, to large scale data transfer and verification. The program consists of five different tests and numerous options. Combinations of these tests and options are selectable from the Nova's front panel data switches and the teletype such that the user may never have to directly alter the processor's memory.

A-2 LOADING AND STARTING

The medium of the AMCOMP 8010 Disc System Diagnostic Program load module is paper tape. This paper tape may be loaded from either the teletype or a high speed paper tape reader. In either case the program will be loaded using the Data General Binary Loader program which is loaded by the Data General Bootstrap Loader. The Data General Nova Processor User's Guide should be referred to for a complete description of these loaders. Once the program is successfully loaded it may be started by executing location 2. This may be accomplished by setting all the data switches except switch 14, which must be up, downward, then engaging the STOP, RESET and START switches in turn. The program will respond by prompting the user for the disc system device address by printing on the teletype the message:

8010 DISC SYSTEM TEST PROGRAM
TYPE 2 DIGIT DISK DEVICE CODE (20 OR 60)

The user should respond to this promptly by entering the disc system device address on the teletype. A response must always be 2 digits since the program waits for the second digit. A response other than 20 or 60 will cause the second half of the above message to be repeated. An improper response, i.e., a 60 for a system with a device address of 20 or vice versa, will cause multiple errors when executing test 1 of this program and the error message SOFTWARE TIMEOUT when executing any other test. Once the device code has been accepted by the program the message SET DATA SWITCHES-CONTINUE is printed on the teletype. In response to this message the user should select the desired options by manipulating the Nova's front panel data switches then depressing the CONTINUE switch which is also located on the Nova's front panel.

A-3 SWITCH FUNCTION AND SETTING

All 16 of the Nova's front panel data switches are used in this program. The switches are active (1) in their up position, and inactive (0) when depressed. Their assignments are as follows:

SWITCH

0	= Print instructions/Abort current test
1	= Halt on error
2	= Print test 4 cycle count
3	= Loop on selected test

4, 5, 6	Test selection
0 0 0	Tests 1 thru 4
0 0 1	Test 1 discrete controller tests
0 1 0	Test 2 diagnostic mode test
0 1 1	Test 3 sizing test
1 0 0	Data transfer (sector) test
1 0 1	Data transfer (subsector) test
1 1 0	Tests 1, 2 and 4
1 1 1	Tests 2 and 4

7	= Read only
8	= Write only
9	= Data error print inhibit
10	= Status error print inhibit
11	= End of test and test ID print inhibit
12	= 2 Reads per write inhibit

13, 14, 15	Select data pattern
0 0 0	Use all data patterns
0 0 1	Use random pattern
0 1 0	Use incrementing pattern
0 1 1	Use track/sector as pattern
1 0 0	Use worst case pattern (16142)
1 0 1	Use all ones
1 1 0	Use all zeroes
1 1 1	User selected pattern

SWITCH 0

The program instructions are printed if and when the program finds switch 0 to be in the up position when the CONTINUE switch has been depressed after the program has printed SET DATA SWITCHES - CONTINUE. These instructions are almost identical to the above description of the switch functions. In order to actually exercise any of the tests of this program the user must depress switch 0. If in the course of actually running any of the tests available in this program switch 0 is found to be set, the test being run will be aborted and the message SET DATA SWITCHES - CONTINUE will be printed. At this time the user may reselect the desired options, then restart the program by depressing CONTINUE.

SWITCH 1

If an error such as discrete test error, status error, data error, or software timeout error occurs during the running of any of the tests available in this program, and the program finds switch 1 to be set, the program will halt. This feature is useful when hardware conditions demand that the software does nothing to cover up a problem once a spurious hardware anomaly has been detected.

SWITCH 2

When, during the running of any of the tests of this program switch 2 is found to be set, the program will print the cycle count. The cycle count is set to zero at the start of the program (when the program prints SET DATA SWITCHES - CONTINUE) and incremented at the end of Test 4.

SWITCH 3

This switch may be used to cause the program to repeatedly execute a single test or a sub-test. As the program starts any of the tests, it determines whether switch 3 is set. If the switch is found to be set the program will demand the test dependent looping parameters from the user. If switch 3 is found to be set as test 1 is started, the program will print the message LOOP ON RNT# on the teletype. The user may then enter on the teletype a number, ranging from 1 to 53, corresponding to the desired test routine number. The program will then repeatedly execute only this desired sub-test for as long as switch 3 remains set. If switch 3 is found to be set when test 2 or test 3 is started, the program will execute repeatedly the particular test without a prompt message. If switch 3 is found to be set as test 4 is started the program will prompt the user with the message START SECTOR. The user should then enter on the teletype the disc system disc/track/sector address (in octal) where the user desires test 4 to start its exercise. Next the program prompts the user with the message END SECTOR to which the user responds with the disc system disc/track/sector address (in octal) where he desires test 4 to end its exercise. The acceptable range of addresses is from a single sector (the desired start and end addresses are the identical) to all the sectors of the disc system. If switch 3 is found to be set when test 5 is started the program will again prompt the user with the messages START SECTOR then END SECTOR then START SUB SECTOR then END SUB SECTOR then NO. OF SUB SECTORS. To each of these messages the user must respond with the desired value. The acceptable range of values is from a single sub sector to the entire disc system. The number of sub sectors refers to the number of sub sectors that will be transferred per transfer and may be any value from 1 to 20 octal.

SWITCHES 4, 5, and 6

The user sets these switches to select the desired test or tests as detailed above. These switches are examined by the program when it is started (when the program has printed SET DATA SWITCHES - CONTINUE) and at the end of each test that is being looped on.

SWITCH 7

When set this switch causes the program to enter a read-only mode. This switch is ignored by tests 1 and 3. The user must ensure that the data read and the data expected to be read are identical; otherwise continuous data errors will result. The disc system should be written with a specific data pattern before read-only mode. This pattern should be the same with the one data was entered if data compare validity is desired by the user.

SWITCH 8

When set this switch causes the program to enter a write-only mode. This switch is ignored by tests 1 and 3.

SWITCH 9

This switch is examined by the program only once a data compare error has occurred. If the switch is found to be set no teletype print of the error condition is made. Otherwise a printout results as detailed as that in the error messages section of this manual.

SWITCH 10

This switch is examined by the program only once a status error has been detected by the program. No teletype print of the error is made if this switch is found to be set. Otherwise a printout results as detailed as that in the error messages section of this manual.

SWITCH 11

When set this switch inhibits the test identification and end of test messages that would otherwise be printed on the teletype as each test is started or completed.

SWITCH 12

The setting of this switch causes the program to issue only one read command to the disc system for each write command. With this switch reset, two read commands are issued for each write.

SWITCHES 13, 14 and 15

The setting of these switches determines the data pattern, as detailed above, used for the data transfer tests. These switches are ignored by tests 1 and 3, and while a data transfer cycle is in progress, i.e., while the program is in the process of writing or reading the disc, the pattern will not be changed even though the user alters the setting of these data switches.

A-4 TEST DESCRIPTIONS

TEST 1 - DISCRETE CONTROLLER TESTS

Test 1 is composed of a series of 43 very short, basic tests which exercise control and status bits between the CPU and the disc system controller. Interrupts are forced and acknowledged and the core location counter is written to and read back. No actual data is transferred.

TEST 2 - CPU TO CONTROLLER DATA PATH TEST

Test 2 writes 16 words of data to the controller in diagnostic mode then reads that data back and compares it to what was written. The data is read back complemented so the program must recomplement it before the actual compare is done. All data patterns may be used by this test.

TEST 3 - DISC SYSTEM SIZING TEST

Test 3 determines the size of the disc system and verifies that the sizing options have been properly strapped in the hardware. The program does this by writing to the first sector of a track of the disc system and examining the status returned by the system after the write. If the status indicates that the track just written to is write-protected, an appropriate error message is printed. The program attempts to write to all four discs in the system and prints the last valid address or a NO DISC MESSAGE for each disc. Once the last valid address has been determined for a disc and that address is found to be less than the maximum address of a disc, the program will continue to write to the remaining possible tracks of that disc ensuring that all these writes raise the NO-SUCH-DISC status bit, otherwise an error message is printed.

TEST 4 - DATA TRANSFER SECTOR

Test 4 writes to the entire disc system, or to the portion of the disc system selected by the user through the looping option and the current data pattern, one sector at a time. When the write is completed the portion of the disc system that was written to is read and the data is compared to what was written. Each sector is read twice unless data switch 12 is set.

TEST 5 - DATA TRANSFER SUBSECTOR

Test 5 writes to the entire disc system, or the portion of the disc system selected by the user through the looping option and the current data pattern, one subsector at a time. When the write is completed the portion of the disc system that was written to is read and the data is compared to what was written. Each subsector is read twice unless data switch 12 is set. If the user chooses to exercise the looping option of test 5, the user must also select the number of subsectors that will be written or read on each data transfer.

A-5 DATA PATTERNS

ZEROES

The zeroes pattern consists of words of data with all data bits reset.

ONES

The ones pattern consists of words of data with all data bits set.

WORST CASE

The worst case pattern consists of words containing the pattern 16142 octal.

TRACK/SECTOR

The track/sector pattern consists of words of data containing the disc system address of where that pattern will be written.

INCREMENTING

The incrementing pattern consists of words of data each of which is incremented by one from the preceding word. The first word is zero, the next 1, and the next 2,

up to a maximum depending on the size of the portion of the disc system being written to. Once the data word is incremented to where it contains all ones, the next data word will again be all zeroes.

RANDOM

The random pattern consists of words of data with bits unpredictably set or reset. The pattern is generated from a one word seed which is manipulated to form a data word. The next data word uses the last data word as the seed. This method allows the same "random" pattern to be generated repeatedly if that were desired. Ordinarily the program will alter the seed word on each pass ensuring a new and different random pattern.

A-6 ERROR MESSAGES

The program prints 2 main types of error messages: status errors and data compare errors. The format for status error is as follows:

STER SS D TTT SS XXX CY

This is a status error message. The STER indicates that a status error occurred. The SS is the actual status the program received in octal. The D TTT SS indicate the disc system address at which the error occurred. D is the disc number, TTT is the track and SS is the sector. The XXX is the cycle count the program was on when the error occurred. The CY identifies the cycle count which is printed only when the program is executing test 4.

N:RD- PPPPPP WT- PPPPPP ADRS: D TTT SS WWW XXX CY

This format is a data compare error. The N is either a 1 or a 2 indicating whether the error occurred on the first or second read. RD- PPPPPP represents the data that was read in octal, WT- PPPPPP represents the data that was written, the expected data. The D TTT SS represent the disc system address as it does for status errors. The WWW is the word position in the sector or subsector in octal where the error was detected. The XXX CY again represents the cycle count which is printed only when the program is executing test 4.

The format of test 1 errors is as follows:

ER# NNN

This is the format of test 1 error. The NNN corresponds to the number of the sub-test that detected the error.

Test 3 will print the message SIZING ERROR if on any particular disc attempting to write to a track address greater than the last valid address does not result in a NO SUCH DISC status.

The error message SOFTWARE TIMEOUT is recorded whenever DONE is not asserted by the disc system approximately 2/3 of second after an I/O instruction causing data transfer, has been issued to it.

Test 1 Sub-Test Detailed Descriptions

The 43 sub-tests that make up Test 1 are identified by their run sequence number in octal.

Sub-Test 01

This sub-test selects device 0 via a SKPBZ instruction. An error indicates that the disc controller is asserting BUSY when it should not.

Sub-Test 02

This sub-test selects device 0 via a SKPDZ instruction. An error indicates that the disc controller is asserting DONE when it should not.

Sub-Test 03

This sub-test clears the disc controller with a NIOC instruction, does an I/O reset via an IORST instruction then checks to see if the disc controller is busy. An error indicates that the disc controller BUSY signal is asserted when it should not be.

Sub-Test 04

This sub-test clears the disc controller with a NIOC instruction, does an I/O reset via an IORST instruction and then checks to see if the disc controller is done. An error indicates that the disc controller DONE signal is asserted when it should not be.

Sub-Test 05

This sub-test issues a NIO instruction to the disc controller then checks to see if BUSY signal is asserted. An error condition indicates that BUSY was asserted without a "S" or "P" pulse.

Sub-Test 06

This sub-test issues a "P" pulse via a NIOP instruction to device 0. It then checks to see if the disc controller asserts BUSY signal. An error condition indicates that the disc controller asserted BUSY in response to a "P" pulse to a device not the disc.

Sub-Test 07

This sub-test issues a "S" pulse via a NIOS instruction to device 0. It then checks to see if the disc controller asserts BUSY signal. An error condition indicates that the disc controller asserted BUSY in response to an "S" pulse to a device not the disc.

Sub-Test 10

This sub-test sets the disc BUSY signal via an NIOP instruction to the disc. It then issues a clear via an NIOC instruction to the disc and issues an IORST. An error condition indicates that the disc BUSY signal failed to clear from neither a "C" pulse nor a I/O reset.

Sub-Test 11

This sub-test sets the disc BUSY signal via an NIOP instruction to the disc and issues an IORST. An error condition indicates that the disc BUSY signal failed to clear from an I/O reset.

Sub-Test 12

This sub-test sets the disc BUSY signal via an NIOP instruction to the disc and issues a clear via an NIOC instruction to the disc. An error condition indicates that the disc BUSY signal failed to clear from a "C" pulse.

Sub-Test 13

This sub-test sets the disc BUSY signal via a DOBP instruction to the disc. An error condition indicates that BUSY failed to set.

Sub-Test 14

This sub-test sets the disc BUSY signal via a DOBS instruction to the disc. The disc is then reset via an NIOC instruction. An error condition indicates that BUSY failed to set.

Sub-Test 15

This sub-test sets the disc BUSY signal via a DOBP instruction to the disc. The disc is then issued an NIO instruction without a "C" pulse. An error condition indicates that the disc was cleared via a NIO instruction without a "C" pulse.

Sub-Test 16

This sub-test sets the disc BUSY signal via a DOBP instruction to the disc. A NIOC instruction is then issued to device 0. An error condition indicates that disc BUSY signal was cleared via an NIOC instruction to a device other than the disc.

Sub-Test 17

This sub-test enables the CPU interrupt system and issues an interrupt acknowledge instruction to which no device should respond. An error condition indicates that an interrupt occurred without the disc DONE signal being set.

Sub-Test 20

This sub-test disables all device interrupts by issuing a MSKO instruction with an argument of all ones. The CPU interrupt system is then enabled which it would be unless an interrupt occurred. An error condition indicates that an interrupt occurred although all device interrupts, including the disc, are disabled.

Sub-Test 21

This sub-test repeats a portion of sub-test 20 by enabling the CPU interrupt system testing to see if an interrupt has occurred. An error condition indicates that the disc interrupt request remained set after the IORST instruction, which is part of every sub test, was issued.

Sub-Test 22

This sub-test issues an interrupt acknowledge instruction. An error condition indicates that the disc responded to the interrupt acknowledge without the disc interrupt request being set.

Sub-Test 23

This sub-test loads the core location counter with all zeroes. An IORST instruction is then issued and the CLC is read back via a DIB instruction. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 24

This sub-test loads the core location counter with all ones. An IORST instruction is then issued and the CLC is read back via a DIB instruction. An error condition indicates that something other than all ones was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 25

This sub-test loads the core location counter with all zeroes, then reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 26

This sub-test loads the core location counter with all zeroes, then loads it with an octal 010421 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (010421).

Sub-Test 27

This sub-test loads the core location counter with all zeroes, then loads it with an octal 021042 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (021042).

Sub-Test 30

This sub-test loads the core location counter with all zeroes, then loads it with an octal 042104 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (042104).

Sub-Test 31

This sub-test loads the core location counter with all zeroes, then loads it with an octal 104210 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (104210).

Sub-Test 32

This sub-test loads the core location counter with all ones, then reads it back. An error condition indicates that something other than all ones was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 33

This sub-test loads the core location counter with all ones and issues a "P" pulse. It then attempts to read back the equivalent of the CLC of device 0. An error condition indicates that data was read back from the CLC when the disc was not selected.

Sub-Test 34

This sub-test loads the core location counter with all ones and issues a "S" pulse. It then attempts to read back the equivalent of the CLC of device 0. An error condition indicates that data was read back from the CLC when the disc was not selected.

Sub-Test 35

This sub-test issues an instruction to load the core location counter with all ones to the CPU as the device. The CLC of the disc is then read back. An error condition indicates that the disc accepted the data (loaded the CLC) when it was not selected.

Sub-Test 36

This sub-test write all ones to the disc core location counter. It then reads the disc CLC back and ANDs that data with an octal 377. An error condition indicates that bits 8 - 15 were not read back correctly.

Sub-Test 37

This sub-test write all ones to the disc core location counter. It then reads the disc CLC back and ANDs that data with an octal 377 and complements it. An error condition indicates that bits 1 - 7 were not read back correctly.

Sub-Test 40

This sub-test loads the core location counter with all ones, then reads it back. An error condition indicates that something other than all ones was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 41

This sub-test selects disc 0, track 0, sector 0 via a DOAP instruction to the disc. The status of the disc system is then read via a DIA instruction. An error condition indicates that the NO-SUCH-Disc status bit (bit 13) was set.

Sub-Test 42

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read. An error condition indicates that the WRITE-ERROR bit (bit 11) was set.

Sub-Test 43

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read via a DIAC instruction which clears the status. An error condition indicates that the WRITE-ERROR bit (bit 11) remained set.

Sub-Test 44

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read via a DIAC instruction which clears the status. An error condition indicates that the ERROR bit (bit 15) remained set.

Sub-Test 45

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read via a DIAC instruction which clears the status. An error condition indicates that the DATA-LATE bit (bit 12) remained set.

Sub-Test 46

This sub-test issues a write command to the disc via a DOBP instruction. It then issues a DIC instruction to device 0. An error condition indicates that a DIC to a device other than the disc produced a response from the disc system.

Sub-Test 49

This sub-test issues a write command to the disc system. It then issues a NIOC to device 21 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 21.

Sub-Test 50

This sub-test issues a write command to the disc system. It then issues a NIOC to device 22 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 22.

Sub-Test 51

This sub-test issues a write command to the disc system. It then issues a NIOC to device 24 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 24.

Sub-Test 52

This sub-test issues a write command to the disc system. It then issues a NIOC to device 30 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 30.

Sub-Test 53

This sub-test is designed to assure that the CLC register is capable of counting. A maximum length (65536 words) write is unitiated from memory location zero. This should cause the CLC to be set to a logical zero, then incremented until it overflows, resulting in its being set to a zero. An error condition indicates that the contents of the

CLC that were read back after the write command had set DONE, was something other than zero. AC0 contains the starting memory location; AC1 contains the status of the disc system after the write; AC2 contains the contents of the CLC after the write; and AC3 contains what was output in the DOC instruction.

Sub-Test 54

This sub-test also assures that the CLC register is capable of counting. The above test (53) expects the setting of the CLC to be the same before and after the write command. This sub-test is executed since a completely non-incrementing CLC would produce the same results. In this sub-test only 65520 words are written from memory location zero. This will cause the CLC to set to an octal 77760 after the write command. An error condition indicates that the contents of the CLC that were read back after the write command had set DONE, was something other than 77760. AC0 contains the expected contents of the CLC; AC1 contains the status of the disc system after the write; AC2 contains the contents of the CLC after the write; and AC3 contains what was output in the DOC instruction.

A-7 DISC CONTROL DIAGNOSTIC

The following pages contain the software diagnostic program for the 8011 Disc Memory Controller.

```
                ;                TYPE 8011  DISK CONTROL DIAGNOSTIC
                ;
                ;1        ABSTRACT
                ;
                ;            TYPE 8011 DISK CONTROL DIAGNOSTIC IS A
                ;            MAINTENANCE PROGRAM DESIGNED TO TEST THE
                ;            TYPE 8010 DISK MEMORY SYSTEM
                ;
                ;2.       MACHINE REQUIREMENTS
                ;
                ;2.1          STANDARD NOVA PROCESSOR
                ;2.2          4K READ/WRITE MEMORY
                ;2.3          DATA DISC 8010 DISC MEMORY SYSTEM
                ;             TELETYPE
                ;
                ;3.       SWITCH SETTINGS
                ;
                ;            SWITCH 0(1)          =PRINT INSTRUCTIONS/ABORT CURRENT TEST
                ;
                ;        HALT / LOOP OPTIONS
                ;
                ;            SWITCH 1(1)          =HALT ON ERROR
                ;            SWITCH 2(1)          =PRINT CYCLE COUNT
                ;            SWITCH 3(1)          =LOOP ON SELECTED TEST
                ;
                ;        TEST SELECTION
                ;
                ;            SWITCH 4(1)          =SELECT TEST
                ;            SWITCH 5(1)          =SELECT TEST
                ;            SWITCH 6(1)          =SELECT TEST
                ;
                ;            4,  5,  6
                ;
                ;            0   0   0       TESTS 1 THRU 4
                ;            0   0   1       TEST 1  DISCRETE CONTROLLER TESTS
                ;            0   1   0       TEST 2  DIAGNOSTIC MODE TEST
                ;            0   1   1       TEST 3  SIZE TEST
                ;            1   0   0       TEST 4  DATA TRANSFER (SECTOR)
                ;            1   0   1       TEST 5  DATA TRANSFER (SUB-SECTOR)
                ;            1   1   0       TESTS 1, 2 AND 4
                ;            1   1   1       TESTS 2 AND 4
                ;
                ;
                ;
                ;            SWITCH 7(1)          =READ-ONLY
                ;            SWITCH 8(1)          =WRITE-ONLY
                ;
                ;            SWITCH 9(1)          =DATA ERROR PRINT INHIBIT
                ;            SWITCH 10(1)         =STATUS ERROR PRINT INHIBIT
                ;            SWITCH 11(1)         =END OF TEST AND TEST ID PRINT INHIBIT
                ;
                ;            SWITCH 12(1)         =2 READS PER WRITE
                ;
                ;            SWITCH 13(1)         =SELECT THE DATA PATTERN
                ;            SWITCH 14(1)         =SELECT THE DATA PATTERN
                ;            SWITCH 15(1)         =SELECT THE DATA PATTERN
                ;
                ;            13,14,15
```

```
                ;
                ;            0  0  0            =USE ALL DATA PATTERNS
                ;            0  0  1            =USE RANDOM PATTERN
                ;            0  1  0            =USE INCREMENTING PATTERN
                ;            0  1  1            =USE TRACK/SECTOR ID PATTERN
                ;            1  0  0            =USE WORST CASE PATTERN
                ;            1  0  1            =USE ALL ONES PATTERN
                ;            1  1  0            =USE ALL ZEROES PATTERN
                ;            1  1  1            =USER SELECTABLE PATTERN
                ;
                ;
                ;
                ;4.      OPERATING PROCEDURE
                ;
                ;4.1        LOAD THE PROGRAM VIA THE BINARY LOADER
                ;
                ;
                ;4.2        GET SWITCHES TO 000002
                ;4.3        PRESS RESET
                ;4.4        PRESS START
                ;
                ;4.5        THE PROGRAM WILL IDENTIFY ITSELF ON THE TELETYPE
                ;          AND REQUEST THE DISK DEVICE CODE TO WHICH A 20 OR
                ;4.6        60 MUST BE ENTERED TO INDICATE THE DISC MEMORY
                ;          SYSTEM TO BE TESTED.  THE PROGRAM WILL NEXT REQUEST
                ;          THAT THE DATA SWITCHES BE SET TO THEIR DESIRED SETTINGS
                ;          THEN HALT.  THE USER SHOULD THEN SET THE DATA SWITCHES
                ;          AND DEPRESS CONTINUE.
                ;
                ;4.7        THE PROGRAM WILL RUN UNTIL MANUALLY STOPPED
                ;          OR AN ERROR IS DETECTED. AT THE END OF EACH
                ;          TEST THE MESSAGE "END OF TEST" IS PRINTED.
                ;
                ;5.      PROGRAM OUTPUT/ERROR DESCRIPTION
                ;5.1        IF A MALFUNCTION IS DETECTED THE PROGRAM
                ;          WILL, DEPENDING ON THE SWITCH SETTING, PRINT
                ;          AN ERROR MESSAGE, HALT, CONTINUE, OR LOOP ON
                ;          THE ERROR.
                ;
                ;6.      PROGRAM DESCRIPTION/THEORY OF OPERATION
                ;
                ;          TEST 1 IS MADE UP OF 43 TEST STEPS WHICH TEST
                ;          THE SETTING AND RESETTING OF THE CONTROLLER STATUS
                ;          BITS UNDER VARIOUS CONDITIONS. NO DATA TRANSFER
                ;          TAKES PLACE.
                ;
                ;          TEST 2 TESTS DIAGNOSTIC MODE. DATA IS TRANSFERRRED FROM
                ;          THE CPU TO THE CONTROLLER AND READ BACK IMMEDIATELY.
                ;          NO DATA TRANSFER TAKES PLACE BETWEEN THE CONTROLLER
                ;          AND THE DISC.
                ;
                ;          TEST 3 DETERMINES THE SIZE AND THE WRITE PROTECTED TRACKS
                ;          OF THE DISC. THE FIRST SECTOR OF EACH TRACK IS WRITTEN TO
                ;          AND THE STATUS OF THE DISC SYSTEM IMMEDIATELY AFTER EACH
                ;          WRITE IS READ AND EXAMINED.
                ;
                ;          TEST 4 TRANSFERS DATA TO AND FROM THE DISC ON A SECTOR
                ;          BY SECTOR BASIS.
```

```
 1                      ;
 2                      ;           TEST 5 TRANSFERS DATA TO AND FROM THE DISC ON A SUB-SECTOR
 3                      ;           BASIS BY USING THE DOC INSTRUCTIONS.
 4                      ;
 5                      ;
 6                      ;7.       RESTRICTIONS/MISC
 7                      ;
 8                      ;7.1         WHEN THE DIAGNOSTIC IS RUNNING NO OTHER
 9                      ;            CONTROL MAY REQUEST THE DISK DRIVE.
10                      ;7.2         THE DISK DRIVE LOGIC MUST RESPOND TO
11                      ;            SELECTING OF DRIVE 0.
12
13              000002  .LOC 2
14   00002 102401               SUB 0,0,SKP
15   00003 102000               ADC 0,0          ;HIGH SPEED CHANNEL
16   00004 040072               STA 0,CHAN
17   00005 002006               JMP @.+1
18   00006 000400               DIAG
19              000050  .LOC 50
20              000020  .DUSR DSK=  020
21              010000  .DUSR IBUF = 10000
22              014000  .DUSR OBUF = 14000
23   00050 000000       PASS:    0
24   00051 000000       TINRET:  0
25   00052 000000       LOADR:   0
26   00053 000000       WDCTR:   0
27   00054 000000       DRET:    0
28   00055 000000       DEVICE:  0
29   00056 000000       MSAV:    0
30   00057 000144       C144:    144
31   00060 000012       C12:     12
32   00061 004520       XXITR:   ITR
33   00062 000543       FIRST:   T01      ;FAB FOR PROGRAM
34   00063 003007       LAST:    ECODE    ;MODIFICATION
35                      ;
36   00064 005630       ICRLF:   CRLF
37   00065 005505       IMESS:   MESS
38   00066 004216       TYPIN:   DCODE
39   00067 004500       SETUP:   ENTER
40   00070 004531       LOOP:    CYCLE
41   00071 004544       ER:      ERR
42              006071  EHALT=JSR         @ER
43                      ;
44   00072 000000       CHAN:    0
45   00073 040000       C40K:    40000
46   00074 010421       C0104:   010421
47   00075 021042       C0210:   021042
48   00076 042104       C0421:   042104
49   00077 104210       C1042:   104210
50   00100 000004       C4:      4
51   00101 140000       C140K:   140000
52   00102 000200       C200:    200
53   00103 000054       C54:     54
54   00104 000010       C10:     10
55   00105 177766       M12:     -12
56   00106 177762       M16:     -16
57   00107 002000       C2000:   2000
58   00110 000001       C1:      1
```

```
 1   00111 000002  C2:       2
 2   00112 000005  C5:        5
 3   00113 000006  C6:        6
 4   00114 000007  C7:        7
 5   00115 177760  M20:      -20
 6   00116 000003  C3:        3
 7   00117 077000  C77K:     77000
 8   00120 000020  C20:       20
 9   00121 000070  C70:       70
10   00122 177720  CM60:     -60
11   00123 000060  C60:       60
12   00124 160020  C1600:    160020
13   00125 060020  C0600:    060020
14   00126 000077  C77:       77
15   00127 177717  C1777:    177717
16   00130 073673  C7367:    073673
17   00131 000044  C44:      44
18   00132 000177  C177:      177
19   00133 000100  C100:      100
20   00134 177777  M1:       -1
21                 ;
22                 ;         DATA SWITCHES
23                 ;
24   00135 100000  PRINS:    100000
25   00136 040000  ERHLTS:    40000
26   00137 020000  LPERS:     20000
27   00140 010000  LPTST:     10000
28   00141 004000  MOD1S:      4000
29   00142 002000  MOD2S:      2000
30   00143 001000  MOD3S:      1000
31   00144 000400  RDONLY:      400
32   00145 000200  WRONLY:      200
33   00146 000100  DERIN:       100
34   00147 000040  STERIN:       40
35   00150 000020  EOCIN:        20
36   00151 000010  RD2WR:        10
37   00152 000004  DPAT1:         4
38   00153 000002  DPAT2:         2
39   00154 000001  DPAT3:         1
40   00155 000007  DPALL:         7
41   00156 007000  MODAL:      7000
42                 ;
43                 ;         STATUS BITS
44                 ;
45   00157 000001  ERROR:   1
46   00160 000002  DAERR:   2
47   00161 000004  NSDIS:   4
48   00162 000010  DALAT:   10
49   00163 000020  WRERR:   20
50   00164 000040  DSFAL:   40
51                 ;
52   00165 000000  ERNO:     0        ;ERROR NUMBER
53   00166 000000  MODE:     0        ;CURRENT MODE
54   00167 014000  IOBUF:    OBUF
55   00170 010000  IIBUF:    IBUF
56   00171 000000  TRKAD:    0
57   00172 000000  LOWSEC:   0
58   00173 000377  HISEC:    377
```

```
 1   00174 000377  MXSEC:    377
 2   00175 000000  LOWSSC:   0
 3   00176 000017  HISSC:    17
 4   00177 000000  NSSC:    0
 5   00200 000000  WRK1:    0
 6   00201 000000  CURSEC:   0
 7   00202 000000  IEDIA:    0
 8   00203 004334  ISTER:    STAER
 9   00204 000000  STERS:    0
10   00205 000000  STTS:    0
11   00206 005527  IPDEC:    PDEC
12   00207 005524  IPOCT:    POCT
13   00210 005601  ICHAR:    CHAR
14   00211 005653  ITYPE:    TYPE
15   00212 004773  ICOMP:   COMP
16   00213 004611  IPTRN:   PATRN
17   00214 000404  ISTRT:   STRT
18   00215 000001  CURPT:   1
19   00216 000000  SSEED:   0
20   00217 000000  CSEED:   0
21   00220 004310  IT4IN:   T4IN
22   00221 000466  ITTBL:   TTBL
23   00222 100000  DMBIT:   100000   ; DIAGNOSTIC MODE BIT
24   00223 004625  IPTBL:   PATBL
25   00224 004146  IIMOD:   IMODE
26   00225 004134  IEOC2:   EDIAG
27   00226 000000  LSSEC:   0
28   00227 000000  HSSEC:   0
29   00230 005422  IINTB:   INTB
30   00231 000000  INPTR:   0
31   00232 005376  IPINS:   PINS
32   00233 000000  PATE:    0
33   00234 000000  PATES:   0
34   00235 002747  IM5:     M5CTS
35   00236 007777  SSONE:   7777
36   00237 010000  SSINC:   10000
37   00240 002371  IMD5:    MOD5B
38   00241 002420  IMW5:    M5WLP
39   00242 000000  T4CY:    0
40   00243 005323  IPCNT:   PCNT
41   00244 005334  IPCT2:   PCT2
42   00245 005037  ICONW:   CONW
43   00246 000000  INCE:    0
44   00247 005267  IONE:    ONEM
45   00250 000000  SELPT:   0
46   00251 001577  IDSC0:   DSC0
47   00252 000000  DSK6:    0
48   00253 002055  IM4:     M4CTS
49   00254 002631  IM5A:    MOD5LP
50   00255 002737  IM5C:    M5CFP
51   00256 001506  IM3:     MOD3C
52   00257 000000  MOD3T:   0
53   00260 001543  IM3P:    M3P
54   00261 000000  SWFLG:   0
55   00262 002557  IM52:    M52
56   00263 002721  IM5W:    MOD5W
57   00264 002745  IM5AD:   M5AD
58   00265 030000  DMSK:    30000
```

```
 1   00266 004000   TMSK1:   4000
 2   00267 003400   TMSK2:   3400
 3   00270 000340   TMSK3:   340
 4   00271 000030   SMSK1:   30
 5   00272 000007   SMSK2:   7
 6   00273 000240   CBLK:    240
 7   00274 000300   PMSK1:   300
 8   00275 000070   PMSK2:   70
 9   00276 000007   PMSK3:   7
10   00277 002510   IM5R:    MOD5R
11   00300 002575   IM5Q:    M5Q
12   00301 005460   IWLP:    WLP
13   00302 000000   WCNTR:   0
14   00303 000000   CRTN:    0
15   00304 000000   POSS:    0
16   00305 000000   CCNTR:   0
17   00306 000000   RWFLG:   0
18   00307 000000   ERCN:    0
19   00310 000000   STARS:   0
20   00311 004373   ISTP:    STP
21   00312 005354   IPRT:    PRT
22   00313 077760   T54C:    77760
23   00314 000055   C55:     55
24                  ;
25                  ;
26                  ;
27         000377   .LOC 377
28                  ;
29   00377 000005   ERC5:    5       ; NO. OF CONSEQUTIVE COMPARE ERROR THAT WILL BE PRINTED
30                  ;
```

```
 1
 2                      ;
 3                      ;
 4                      ;       START OF DIAGNOSTIC
 5                      ;
 6                      ;
 7   00400 006064   DIAG:    JSR     @ICRLF  ;RHW DIAGNOSTIC
 8   00401 006065            JSR     @IMESS  ;TELL OPERATOR TO
 9   00402 003741            LOCKIT  ;LOCK DISK DRIVE.
10   00403 006066            JSR     @TYPIN
11                      ;
12   00404 102400   STRT:    SUB     0,0
13   00405 040250            STA     0,SELPT
14   00406 040050            STA     0,PASS
15   00407 040166            STA     0,MODE
16   00410 040242            STA     0,T4CY
17   00411 040165            STA     0,ERNO
18   00412 040233            STA     0,PATE
19   00413 101400            INC     0,0     ; FORM A ONE
20   00414 040215            STA     0,CURPT ;
21   00415 006064            JSR     @ICRLF  ; CARRIAGE
22   00416 006065            JSR     @IMESS  ; MESSAGE
23   00417 003102            SSWM1
24   00420 063077            HALT            ; WAIT FOR SWITCHES TO BE SET
25   00421 074477            READS   3       ; READ THE DATA SWITCHES
26   00422 030135            LDA     2,PRINS ; GET THE PRINT SWITCH
27   00423 173404            AND     3,2,SZR ; MASK WITH SWITCHES
28   00424 000402            JMP     .+2
29   00425 002225            JMP     @IEOC2  ; START A TEST
30                      ;
31                      ;       PRINT THE INSTRUCTIONS
32                      ;
33   00426 006232            JSR     @IPINS  ; PRINT THE INSTRUCTIONS
34   00427 000755            JMP     STRT
35                      ;
36                      ;
37   00430 074477   MODE1:   READS   3       ; READ THE DATA SWITCHES
38   00431 030150            LDA     2,EOCIN ; PRINT INHIBIT
39   00432 173404            AND     3,2,SZR ; MASK THE SWTCHES
40   00433 000407            JMP     M1B     ; YES  NO ID PRINT
41                      ;
42   00434 006064            JSR     @ICRLF
43   00435 006065            JSR     @IMESS
44   00436 004006            MOD1M
45   00437 034110            LDA     3,C1    ; GET A ONE
46   00440 054166            STA     3,MODE  ; SET CURRENT MODE
47   00441 074477            READS   3       ; READ THE DATA SWITCHES
48   00442 030140   M1B:     LDA     2,LPTST ; GET LOOP ON TEST BIT
49   00443 074477            READS   3
50   00444 173405            AND     3,2,SNR
51   00445 000476            JMP     T01
52                      ;
53   00446 006064   M1A:     JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
54   00447 006065            JSR     @IMESS  ; MESSAGE
55   00450 004104            TNOM
56   00451 152400            SUB     2,2,    ; GET TWO DIGITS
57   00452 006220            JSR     @IT4IN  ; READ THE TTY
58   00453 000773            JMP     M1A     ; ERROR
```

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```
 1   00454 024314          LDA     1,C55    ; GET MAX TEST NO.
 2   00455 132433          SUBZ#   1,2,SNC
 3   00456 000770          JMP     M1A
 4   00457 150400          NEG     2,2      ; DECREMENT COUNT
 5   00460 150000          COM     2,2
 6   00461 050165          STA     2,ERNO   ; SET POTENTIAL ERROR NUMBER
 7   00462 151400          INC     2,2
 8   00463 024221          LDA     1,ITTBL  ; ADDRESS OF TEST TABLE
 9   00464 133000          ADD     1,2      ; ADD TO ENTERED NUMBER
10   00465 003000          JMP     @0,2     ; JUMP TO DESIRED TEST
11                 ;
12   00466 000446  TTBL:   M1A
13   00467 000543          T01
14   00470 000552          T02
15   00471 000556          T03
16   00472 000564          T04
17   00473 000572          T05
18   00474 000577          T06
19   00475 000604          T07
20   00476 000611          T10
21   00477 000620          T11
22   00500 000626          T12
23   00501 000634          T13
24   00502 000642          T14
25   00503 000654          T15
26   00504 000663          T16
27   00505 000674          T17
28   00506 000704          T20
29   00507 000714          T21
30   00510 000722          T22
31   00511 000727          T23
32   00512 000737          T24
33   00513 000747          T25
34   00514 000756          T26
35   00515 000770          T27
36   00516 001002          T30
37   00517 001014          T31
38   00520 001026          T32
39   00521 001035          T33
40   00522 001044          T34
41   00523 001054          T35
42   00524 001063          T36
43   00525 001073          T37
44   00526 001105          T40
45   00527 001114          T41
46   00530 001126          T42
47   00531 001140          T43
48   00532 001152          T44
49   00533 001162          T45
50   00534 001172          T46
51   00535 001205          T47
52   00536 001214          T50
53   00537 001223          T51
54   00540 001232          T52
55   00541 001241          T53
56   00542 001255          T54
57                 ;
58                 ;
```

```
 1  00543 101000  T01:    MOV     0,0
 2  00544 102400          SUB     0,0       ; FORM A ZERO
 3  00545 040165          STA     0,ERNO    ; RESET ERROR NUMBER
 4
 5
 6  00546 006067          JSR     @SETUP    ; SELECT DEVICE ZERO, TEST FOR NOT BUSY
 7  00547 063500          SKPBZ   0         ; IF EHALT THE CONTROLLER IS ASSERTING
 8  00550 006071          EHALT             ; BUSY AND SHOULD NOT BE.
 9  00551 006070          JSR     @LOOP     ;
10
11  00552 006067  T02:    JSR     @SETUP    ; SAME AS TEST 01 TESTING
12  00553 063700          SKPDZ   0         ; DONE INSTEAD OF BUSY
13  00554 006071          EHALT             ;
14  00555 006070          JSR     @LOOP     ;
15
16  00556 006067  T03:    JSR     @SETUP    ;DISK BUSY FLOP STUCK (1).
17  00557 060220          NIOC    DSK       ;
18  00560 062677          IORST             ;DISK BUSY (1), ASSERTED
19  00561 063520          SKPBZ   DSK       ;WITHOUT DISK BUSY.
20  00562 006071          EHALT
21  00563 006070          JSR     @LOOP
22
23  00564 006067  T04:    JSR     @SETUP    ;DISK DONE FLOP STUCK (1)
24  00565 060220          NIOC    DSK       ;
25  00566 062677          IORST             ;DISK DONE (1), ASSERTED
26  00567 063720          SKPDZ   DSK       ;WITHOUT DISK DONE.
27  00570 006071          EHALT
28  00571 006070          JSR     @LOOP
29
30  00572 006067  T05:    JSR     @SETUP    ;SELECTING THE DISK
31  00573 060020          NIO     DSK       ;WITHOUT A "S" OR "C" PULSE
32  00574 063520          SKPBZ   DSK       ;SET DISK BUSY
33  00575 006071          EHALT             ;
34  00576 006070          JSR     @LOOP     ;
35
36  00577 006067  T06:    JSR     @SETUP    ;A "P" PULSE TO A
37  00600 060300          NIOP    0         ;DEVICE NOT THE DISK
38  00601 063520          SKPBZ   DSK       ;SET DISK BUSY.
39  00602 006071          EHALT             ;
40  00603 006070          JSR     @LOOP
41
42  00604 006067  T07:    JSR     @SETUP    ;A "S" PULSE TO A
43  00605 060100          NIOS    0         ;DEVICE NOT THE DISK
44  00606 063520          SKPBZ   DSK       ;SET DISK BUSY.
45  00607 006071          EHALT
46  00610 006070          JSR     @LOOP
47
48  00611 006067  T10:    JSR     @SETUP    ;DISK BUSY FLOP FAILED
49  00612 060320          NIOP    DSK       ;TO CLEAR VIA A "C"
50  00613 060220          NIOC    DSK       ;PULSE OR I/O RESET.
51  00614 062677          IORST
52  00615 063520          SKPBZ   DSK
53  00616 006071          EHALT
54  00617 006070          JSR     @LOOP
55
56  00620 006067  T11:    JSR     @SETUP    ;DISK BUSY FLOP FAILED
57  00621 060320          NIOP    DSK       ;TO CLEAR VIA A I/O RESET.
58  00622 062677          IORST
```

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PAGE  10
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 1   00623 063520           SKPBZ   DSK
 2   00624 006071           EHALT
 3   00625 006070           JSR     @LOOP
 4
 5   00626 006067  T12:     JSR     @SETUP  ;DISK BUSY FLOP FAILED
 6   00627 060320           NIOP    DSK     ;TO CLEAR VIA A "C"
 7   00630 060220           NIOC    DSK     ;PULSE.
 8   00631 063520           SKPBZ   DSK
 9   00632 006071           EHALT
10   00633 006070           JSR     @LOOP
11
12   00634 006067  T13:     JSR     @SETUP  ;A "P" PULSE FAILED
13   00635 020170           LDA     0,IIBUF ;TO SET DISK BUSY FLOP.
14   00636 062320           DOBP    0,DSK
15   00637 063420           SKPBN   DSK
16   00640 006071           EHALT
17   00641 006070           JSR     @LOOP
18
19   00642 006067  T14:     JSR     @SETUP  ;A "S" PULSE FAILED
20   00643 020170           LDA     0,IIBUF ;TO SET DISK BUSY FLOP.
21   00644 126400           SUB     1,1
22   00645 062120           DOBS    0,DSK
23   00646 063520           SKPBZ   DSK
24   00647 126000           ADC     1,1
25   00650 060220           NIOC    DSK
26   00651 125005           MOV     1,1,SNR
27   00652 006071           EHALT
28   00653 006070           JSR     @LOOP
29
30   00654 006067  T15:     JSR     @SETUP  ;THE DSK BUSY FLOP
31   00655 020170           LDA     0,IIBUF ;WAS CLEARED VIA A
32   00656 062320           DOBP    0,DSK   ;"NIO" INSTRUCTION WITH-
33   00657 060020           NIO     DSK     ;OUT A "C" PULSE.
34   00660 063420           SKPBN   DSK
35   00661 006071           EHALT
36   00662 006070           JSR     @LOOP
37
38   00663 006067  T16:     JSR     @SETUP  ;THE DSK BUSY FLOP
39   00664 020170           LDA     0,IIBUF ;WAS CLEARED VIA A
40   00665 062320           DOBP    0,DSK   ;"C" PULSE WITHOUT
41   00666 060200           NIOC    0       ;THE DISK BEING SELECTED.
42   00667 063420           SKPBN   DSK
43   00670 006071           EHALT
44   00671 006070           JSR     @LOOP
45
46   00672 102620           SUBZR   0,0     ;SET LOCATION
47   00673 040001           STA     0,1     ;FOR INTERRUPTS
48
49   00674 006067  T17:     JSR     @SETUP  ;A INTERRUPT OCCURED
50   00675 060177           NIOS    CPU     ;WITHOUT DSK DONE FLOP
51   00676 061477           INTA    0       ;BEING SET.
52   00677 101004           MOV     0,0,SZR
53   00700 000403           JMP     .+3
54   00701 063477           SKPBN   CPU
55   00702 006071           EHALT
56   00703 006070           JSR     @LOOP
57
58   00704 006067  T20:     JSR     @SETUP  ;THE DKS INT REQ
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```
 1   00705 102000           ADC     0,0       ;FLOP IS SET.
 2   00706 062077           MSKO    0
 3   00707 060177           NIOS    CPU
 4   00710 101000           MOV     0,0
 5   00711 063477           SKPBN   CPU
 6   00712 006071           EHALT
 7   00713 006070           JSR     @LOOP
 8
 9   00714 006067  T21:      JSR     @SETUP   ;THE DSK INT REQ
10   00715 060177           NIOS    CPU      ;FLOP IS SET.
11   00716 101000           MOV     0,0
12   00717 063477           SKPBN   CPU
13   00720 006071           EHALT
14   00721 006070           JSR     @LOOP
15
16   00722 006067  T22:      JSR     @SETUP   ;THE DSK INT REQ FLOP
17   00723 061477           INTA    0        ;IS NOT SET. YET INTA
18   00724 101004           MOV     0,0,SZR  ;READS BACK A BYTE.
19   00725 006071           EHALT
20   00726 006070           JSR     @LOOP
21
22   00727 006067  T23:      JSR     @SETUP   ;THE CORE LOCATION COUNTER
23   00730 126400           SUB     1,1      ;(CLC) WAS LOADED TO 0
24   00731 066020           DOB     1,DSK    ;THEN RESET VIA IORST.
25   00732 062677           IORST            ;DIB   READ BITS BACK.
26   00733 061420           DIB     0,DSK    ;CHECK AC0 FOR READ
27   00734 101004           MOV     0,0,SZR  ;CHECK AC1 FOR WRITTEN
28   00735 006071           EHALT
29   00736 006070           JSR     @LOOP
30
31   00737 006067  T24:      JSR     @SETUP   ;THE CORE LOCATION COUNTER
32   00740 126220           ADCZR   1,1      ;(CLC) WAS LOADED WITH
33   00741 066020           DOB     1,DSK    ;ALL BITS. THEN CLEARED
34   00742 062677           IORST            ;VIA A I/O RESET PULSE.
35   00743 061420           DIB     0,DSK    ;CHECK AC0 FOR READ
36   00744 101004           MOV     0,0,SZR  ;CHECK AC1 FOR WRITTEN
37   00745 006071           EHALT
38   00746 006070           JSR     @LOOP
39
40   00747 006067  T25:      JSR     @SETUP   ;LOAD THE CLC REGISTER
41   00750 126400           SUB     1,1      ;WITH ZEROS. CHECK VIA
42   00751 066020           DOB     1,DSK    ;A DIB INSTRUCTION.
43   00752 061420           DIB     0,DSK    ;ANY BIT SET IN AC0  IS
44   00753 101004           MOV     0,0,SZR  ;IN ERROR.
45   00754 006071           EHALT
46   00755 006070           JSR     @LOOP
47
48   00756 006067  T26:      JSR     @SETUP   ;LOAD THE CLC REGISTER
49   00757 102400           SUB     0,0      ;MAGIC TEST 1#
50   00760 062020           DOB     0,DSK
51   00761 024074           LDA     1,C0104  ;#010421
52   00762 066020           DOB     1,DSK    ; AC1 WRITTEN
53   00763 062020           DOB     0,DSK    ; AC0 READ
54   00764 061420           DIB     0,DSK
55   00765 101004           MOV     0,0,SZR
56   00766 006071           EHALT
57   00767 006070           JSR     @LOOP
58
```

```
 1   00770 006067  T27:    JSR     @SETUP  ;LOAD THE CLC REGISTER
 2   00771 102400          SUB     0,0     ;MAGIC TEST 2#
 3   00772 062020          DOB     0,DSK
 4   00773 024075          LDA     1,C0210 ;#021042
 5   00774 066020          DOB     1,DSK   ; AC1 WRITTEN
 6   00775 062020          DOB     0,DSK   ; AC0 READ
 7   00776 061420          DIB     0,DSK
 8   00777 101004          MOV     0,0,SZR
 9   01000 006071          EHALT
10   01001 006070          JSR     @LOOP
11
12   01002 006067  T30:    JSR     @SETUP  ;LOAD THE CLC REGISTER
13   01003 102400          SUB     0,0     ;MAGIC TEST 3#
14   01004 062020          DOB     0,DSK
15   01005 024076          LDA     1,C0421 ;#042104
16   01006 066020          DOB     1,DSK   ; AC 1 WRITTEN
17   01007 062020          DOB     0,DSK   ; AC0 READ
18   01010 061420          DIB     0,DSK
19   01011 101004          MOV     0,0,SZR
20   01012 006071          EHALT
21   01013 006070          JSR     @LOOP
22
23   01014 006067  T31:    JSR     @SETUP  ;LOAD THE CLC REGISTER
24   01015 102400          SUB     0,0     ;MAGIC TEST 4#
25   01016 062020          DOB     0,DSK
26   01017 024077          LDA     1,C1042 ;#104210
27   01020 066020          DOB     1,DSK   ; AC 1 WRITTEN
28   01021 062020          DOB     0,DSK   ; AC0 READ
29   01022 061420          DIB     0,DSK
30   01023 101004          MOV     0,0,SZR
31   01024 006071          EHALT
32   01025 006070          JSR     @LOOP
33
34   01026 006067  T32:    JSR     @SETUP  ;LOAD CLC WITH
35   01027 126000          ADC     1,1     ;ALL ONES AND TRY
36   01030 066020          DOB     1,DSK   ;TO READ SOME BACK.
37   01031 061420          DIB     0,DSK   ;AC1 WRITTEN
38   01032 101005          MOV     0,0,SNR ; AC0 READ
39   01033 006071          EHALT
40   01034 006070          JSR     @LOOP
41
42   01035 006067  T33:    JSR     @SETUP  ;DSK DATIB ASSERTED
43   01036 102220          ADCZR   0,0     ;WITHOUT DSK SELECT.
44   01037 062320          DOBP    0,DSK
45   01040 065400          DIB     1,0
46   01041 106415          SUB#    0,1,SNR
47   01042 006071          EHALT
48   01043 006070          JSR     @LOOP
49
50   01044 006067  T34:    JSR     @SETUP  ;DSK DATOB ASSERTED
51   01045 126220          ADCZR   1,1     ;WITHOUT DSK SELECT
52   01046 066120          DOBS    1,DSK   ;AC 1 WRITTEN
53   01047 061400          DIB     0,0     ;AC 0 READ
54   01050 060220          NIOC    DSK
55   01051 106415          SUB#    0,1,SNR
56   01052 006071          EHALT
57   01053 006070          JSR     @LOOP
58
```

```
 1  01054 006067  T35:    JSR     @SETUP  ;DSK DATOB ASSERTED
 2  01055 126220          ADCZR   1,1     ;WITHOUT DSK SELECT
 3  01056 066077          DOB     1,CPU   ;AC 1 WRITTEN
 4  01057 061420          DIB     0,DSK   ;AC 0 READ
 5  01060 106415          SUB#    0,1,SNR
 6  01061 006071          EHALT
 7  01062 006070          JSR     @LOOP
 8
 9  01063 006067  T36:    JSR     @SETUP  ;THE CLC REGISTER FAILED
10  01064 102000          ADC     0,0     ;TO READ BACK BITS
11  01065 062020          DOB     0,DSK   ;8-15.
12  01066 061420          DIB     0,DSK
13  01067 024406          LDA     1,XX377
14  01070 123415          AND#    1,0,SNR
15  01071 006071          EHALT
16  01072 006070          JSR     @LOOP
17
18  01073 006067  T37:    JSR     @SETUP  ;THE CLC REGISTER FAILED
19  01074 102001          ADC     0,0,SKP ;TO READ BACK BITS 1-7
20  01075 000377  XX377:  377
21  01076 062020          DOB     0,DSK
22  01077 061420          DIB     0,DSK
23  01100 024775          LDA     1,XX377
24  01101 124000          COM     1,1
25  01102 123415          AND#    1,0,SNR
26  01103 006071          EHALT
27  01104 006070          JSR     @LOOP
28
29  01105 006067  T40:    JSR     @SETUP  ;LOAD CLC WITH ALL
30  01106 126000          ADC     1,1     ;ONES, CHECK THEM AS
31  01107 066020          DOB     1,DSK   ;READ BACK.
32  01110 061420          DIB     0,DSK   ; AC1 WRITTEN
33  01111 104014          COM#    0,1,SZR ; AC0 READ
34  01112 006071          EHALT
35  01113 006070          JSR     @LOOP
36
37  01114 006067  T41:    JSR     @SETUP  ;DISK SELECT ERROR IS  SET
38  01115 102400          SUB     0,0     ;SELECTING DISC 0.
39  01116 061320          DOAP    0,DSK   ;TRACK 0, SECTOR 0.
40  01117 063520          SKPBZ   DSK     ;SET NO-SUCH-DISC BIT
41  01120 000777          JMP     .-1
42  01121 060420          DIA     0,DSK
43  01122 024100          LDA     1,C4
44  01123 107414          AND#    0,1,SZR
45  01124 006071          EHALT
46  01125 006070          JSR     @LOOP
47
48  01126 006067  T42:    JSR     @SETUP  ;WRITE LOCK STATUS
49  01127 020117          LDA     0,C77K  ; IS SET WITHOUT WRITE COMMAND
50  01130 062120          DOBS    0,DSK
51  01131 063520          SKPBZ   DSK
52  01132 000777          JMP     .-1
53  01133 060420          DIA     0,DSK
54  01134 024120          LDA     1,C20
55  01135 107414          AND#    0,1,SZR
56  01136 006071          EHALT
57  01137 006070          JSR     @LOOP
58
```

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PAGE  14
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  1   01140 006067  T43:    JSR     @SETUP  ;WRITE LOCK STATUS
  2   01141 020117          LDA     0,C77K  ;SHOULD NOT SET ON
  3   01142 062120          DOBS    0,DSK   ;A READ OPERATION.
  4   01143 063520          SKPBZ   DSK
  5   01144 000777          JMP     .-1
  6   01145 060620          DIAC    0,DSK
  7   01146 024120          LDA     1,C20
  8   01147 107414          AND#    0,1,SZR
  9   01150 006071          EHALT
 10   01151 006070          JSR     @LOOP
 11
 12   01152 006067  T44:    JSR     @SETUP  ;DISK DATA ERROR BIT
 13   01153 020101          LDA     0,C140K ;IS SET.
 14   01154 062120          DOBS    0,DSK
 15   01155 060620          DIAC    0,DSK
 16   01156 105220          MOVZR   0,1
 17   01157 125202          MOVR    1,1,SZC
 18   01160 006071          EHALT
 19   01161 006070          JSR     @LOOP
 20
 21   01162 006067  T45:    JSR     @SETUP  ;DISK DCH LATE ERROR
 22   01163 020101          LDA     0,C140K ;BIT IS SET.
 23   01164 062120          DOBS    0,DSK
 24   01165 060620          DIAC    0,DSK
 25   01166 024104          LDA     1,C10
 26   01167 107414          AND#    0,1,SZR
 27   01170 006071          EHALT
 28   01171 006070          JSR     @LOOP
 29
 30   01172 006067  T46:    JSR     @SETUP  ;COMMAND IS WRITE
 31   01173 102620          SUBZR   0,0     ;MAINT MODE. THIS TEST
 32   01174 062320          DOBP    0,DSK   ;INSURES THAT A DIC
 33   01175 076400          DIC     3,0     ;INSTRUCTION TO A DEVICE
 34   01176 101000          MOV     0,0     ;OTHER THAN THE DISK
 35   01177 076400          DIC     3,0     ;WILL NOT PRODUCE
 36   01200 060420          DIA     0,DSK   ;(DSK DATIC) 4 MAINTENANCE
 37   01201 024102          LDA     1,C200  ;FEATURE OF THE DISK.
 38   01202 107414          AND#    0,1,SZR
 39   01203 006071          EHALT
 40   01204 006070          JSR     @LOOP
 41
 42   01205 006067  T47:    JSR     @SETUP  ;CHECK DEVICE SELECTION
 43   01206 102620          SUBZR   0,0
 44   01207 062320          DOBP    0,DSK
 45   01210 060221          NIOC    21
 46   01211 063420          SKPBN   DSK
 47   01212 006071          EHALT
 48   01213 006070          JSR     @LOOP
 49
 50   01214 006067  T50:    JSR     @SETUP  ;CHECK DEVICE SELECTION
 51   01215 102620          SUBZR   0,0
 52   01216 062320          DOBP    0,DSK
 53   01217 060222          NIOC    22
 54   01220 063420          SKPBN   DSK
 55   01221 006071          EHALT
 56   01222 006070          JSR     @LOOP
 57
 58   01223 006067  T51:    JSR     @SETUP  ;CHECK DEVICE SELECTION
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 1  01224 102620          SUBZR   0,0
 2  01225 062320          DOBP    0,DSK
 3  01226 060224          NIOC    24
 4  01227 063420          SKPBN   DSK
 5  01230 006071          EHALT
 6  01231 006070          JSR     @LOOP
 7
 8  01232 006067  T52:     JSR     @SETUP  ;CHECK DEVICE SELECTION
 9  01233 102620          SUBZR   0,0
10  01234 062320          DOBP    0,DSK
11  01235 060230          NIOC    30
12  01236 063420          SKPBN   DSK
13  01237 006071          EHALT
14  01240 006070          JSR     @LOOP
15
16  01241 006067  T53:     JSR     @SETUP  ; CHECK THAT CLC REGISTER CAN INCREMENT
17  01242 176400          SUB     3,3     ; FORM A ZERO
18  01243 102400          SUB     0,0     ;
19  01244 062020          DOB     0,DSK   ; CORE ADDRESS ZERO
20  01245 077320          DOCP    3,DSK   ; DOC OF ZERO MEANS WRITE 65K WORDS
21  01246 063620          SKPDN   DSK     ; WAIT FOR DONE
22  01247 000777          JMP     .-1
23                ;
24  01250 064420          DIA     1,DSK   ; GET DISC STATUS
25  01251 071420          DIB     2,DSK   ; GET THE CLC REGISTER
26  01252 151004          MOV     2,2,SZR ; ZERO IMPLIES CLC WRAPPED ALL AROUND IS OK
27  01253 006071          EHALT           ; ON ERROR AC 0 CONTAINS CORE ADDRESS OF WRITE
28                                        ; START. AC1 CONTAINS DISC SYSTEM STATUS. AC2
29                                        ; CONTAINS THE CLC REGISTER CONTENTS AFTER THE WRITE.
30                                        ; AC3 CONTAINS INITIAL CLC CONTENTS.
31  01254 006070          JSR     @LOOP
32                ;
33  01255 006067  T54:     JSR     @SETUP  ; CHECK THAT CLC CAN INCREMENT
34  01256 034110          LDA     3,C1    ; GET A ONE
35  01257 102400          SUB     0,0     ; FORM A ZERO
36  01260 062020          DOB     0,DSK   ; USE MEMORY ADDRESS OF ZERO
37  01261 077320          DOCP    3,DSK   ; DOC OF 1  WRITES LOTS
38  01262 063620          SKPDN   DSK     ; WAIT FOR DONE
39  01263 000777          JMP     .-1
40                ;
41  01264 064420          DIA     1,DSK   ; GET DISC STATUS
42  01265 071420          DIB     2,DSK   ; GET THE CLC
43  01266 020313          LDA     0,T54C  ; GET THE EXPECTED CLC CONTENTS
44  01267 112434          SUBZ#   0,2,SZR ; COMPARE TO ACTUAL
45  01270 006071          EHALT           ; ON ERROR AC0 CONTAINS EXPECTED CLC CONTENTS
46                                        ; AC1 CONTAINS DISC SYSTEM STATUS
47                                        ; AC2 CONTAINS CLC CONTENTS
48                                        ; AC3 CONTAINS DOC OUTPUT REGISTER
49  01271 006070          JSR     @LOOP
50                ;
51  01272 074477          READS   3       ; READ THE DATA SWITCHES
52  01273 030150          LDA     2,EOCIN ; INHIBIT EOT PRINT BIT
53  01274 173404          AND     3,2,SZR ; SEE IF SET
54  01275 000404          JMP     T100!   ; YES  NO PRINT
55                ;
56  01276 006064          JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
57  01277 006065          JSR     @IMESS  ; MESSAGE
58  01300 003735          IPASS
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 1  01301 002401  T1OUT:  JMP      @.+1
 2  01302 004134          EDIAG
```

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 1
 2                  ;
 3                  ;
 4                  ;       TEST 2 HANDLER
 5                  ;
 6                  ; 1. GENERATE 16 HALFWORD PATTERN IN OBUF
 7                  ; 2. SEND DOB OF OBUF PLUS BIT 0 + PULSE    TO WRITE TO CONTROLLER
 8                  ; 3. SEND DOB OF IBUF PLUS BIT 0 + START    TO READ FROM CONTROLLER
 9                  ; 4. COMPLEMENT IBUF
10                  ; 5. COMPARE IBUF, OBUF
11                  ; (USE LOC. 20 AUTO
12                  ;
13  01303 034111    MODE2:  LDA     3,C2    ; GET A TWO
14  01304 054166            STA     3,MODE  ; SET CURRENT MODE
15  01305 176400            SUB     3,3     ; FORM A ZERO
16  01306 054500            STA     3,M22   ; RESET 1-2 READ FLAG
17  01307 054261            STA     3,SWFLG ; ALLOW PATTERN CHANGE
18  01310 054246            STA     3,INCE  ; INITIALIZE INCREMENTING PATTERN
19  01311 034216            LDA     3,SSEED ; GET INITIAL SEED
20  01312 054217            STA     3,CSEED ; INITIALIZE SEED
21  01313 034110            LDA     3,C1    ; GET A ONE
22  01314 054215            STA     3,CURPT ; INITIALIZE PATTERN
23  01315 074477            READS   3       ; READ THE DATA SWITCHES
24  01316 030150            LDA     2,EOCIN ; PRINT INHIBIT BIT
25  01317 173404            AND     3,2,SZR ; MASK SWITCHES
26  01320 000404            JMP     M2B
27                  ;
28  01321 006064            JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
29  01322 006065            JSR     @IMESS  ; MESSAGE
30  01323 004023            MOD2M
31  01324 006213    M2B:    JSR     @IPTRN  ;GENERATE PATTERN
32  01325 000020    C16:    20              ;OF 16 WORDS
33  01326 014000            OBUF            ;IN OUTPUT BUFFER
34  01327 000000            0               ; TRACK ADDRESS
35
36  01330 074477    MOD2B:  READS   3       ; READ THE DATA SWITCHES
37  01331 030144            LDA     2,RDONLY ; READ ONLY BIT
38  01332 173404            AND     3,2,SZR ; MASK THE SWITCHES
39  01333 000421            JMP     M2RD    ;
40                  ;
41  01334 030134            LDA     2,M1    ; TIME OUT VALUE
42  01335 050302            STA     2,WCNTR ; SET COUNTER
43  01336 152400            SUB     2,2     ; FORM A ZERO
44  01337 050306            STA     2,RWFLG ; INDICATE WRITE
45  01340 020167            LDA     0,IOBUF ;ADDRESS OF OUTPUT BUFFER
46  01341 024222            LDA     1,DMBIT ;
47  01342 044261            STA     1,SWFLG ; INHIBIT PATTERN CHANGE
48  01343 123000            ADD     1,0     ;
49  01344 062320            DOBP    0,DSK   ;WRITE TO CNTRL
50  01345 063620            SKPDN   DSK     ; WAIT FOR DONE
51  01346 006301            JSR     @IWLP
52                  ;
53  01347 074477            READS   3
54  01350 030145            LDA     2,WRONLY ; GET WRITE ONLY BIT
55  01351 173400            AND     3,2     ; MASK WITH SWITCHES
56  01352 151004            MOV     2,2,SZR ; SEE IF SET
57  01353 000755            JMP     MOD2B
58
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 1  01354 102400  M2RD:   SUB     0,0      ; FORM A ZERO
 2  01355 040246          STA     0,INCE   ; INITIALIZE INCREMENT
 3  01356 101400          INC     0,0      ; FORM A ONE
 4  01357 040306          STA     0,RWFLG  ; INDICATE READ
 5  01360 020216          LDA     0,SSEED  ; INITIAL SEED
 6  01361 040217          STA     0,CSEED  ; INITIALIZE SEED
 7  01362 020170          LDA     0,IIBUF  ;ADDRESS OF INPUT BUFFER
 8  01363 024222          LDA     1,DMBIT  ;
 9  01364 123000          ADD     1,0      ;
10  01365 062120          DOBS    0,DSK    ;READ FROM CNTROLLER
11
12  01366 030115          LDA     2,M20    ;MINUS 16
13  01367 034170          LDA     3,IIBUF  ;ADDRESS OF INPUT BUFFER
14  01370 174400          NEG     3,3      ; DECREMENT
15  01371 174000          COM     3,3
16  01372 054020          STA     3,20     ;SET POINTERS
17  01373 054021          STA     3,21     ;SET POINTERS
18  01374 022020   CMP:    LDA     0,@20    ;GET WORD
19  01375 100000          COM     0,0      ;COMPLEMENT
20  01376 042021          STA     0,@21    ;STORE IT BACK
21  01377 151404          INC     2,2,SZR
22  01400 000774          JMP     CMP
23  01401 006212          JSR     @ICOMP
24  01402 000020          20
25  01403 014000          OBUF
26  01404 010000          IBUF
27  01405 000000          0
28  01406 000000  M22:     0
29                        ;
30  01407 074477          READS   3        ; READ THE DATA SWITCHES
31  01410 030151          LDA     2,RD2WR  ; SEE IF NOT 2 READS PER WRITE
32  01411 173405          AND     3,2,SNR  ;
33  01412 000432          JMP     M2CRD    ; SECOND READ
34  01413 030135  M2C:     LDA     2,PRINS  ; ABORT TEST BIT
35  01414 173404          AND     3,2,SZR  ; MASK SWITCHES
36  01415 002214          JMP     @ISTRT   ; GO TO BEGINNIG
37                        ;
38  01416 030137          LDA     2,LPERS  ; PRINT CYCLE COUNT SWITCH
39  01417 173404          AND     3,2,SZR  ; SEE IF SET
40  01420 006244          JSR     @IPCT2   ; YES  PRINT CYCLE COUNT
41  01421 074477          READS   3
42  01422 030140          LDA     2,LPTST  ; GET LOOP ON TEST BIT
43  01423 173404          AND     3,2,SZR  ; MASK SWITCHES
44  01424 000440          JMP     M2B2     ; YES  LOOP
45
46  01425 030155          LDA     2,DPALL  ; MASK OF PATTERN DATA SWITCHES
47  01426 173405          AND     3,2,SNR  ; SEE IF 0 SELECTED
48  01427 000425          JMP     P2NX     ; YES DO ALL PATTERNS
49                        ;
50  01430 030150  M2EXT:   LDA     2,EOCIN  ; END OF TEST PRINT INHIBIT ?
51  01431 173404          AND     3,2,SZR  ; SEE IF SET
52  01432 000404          JMP     M2OUT    ; YES
53                        ;
54  01433 006064          JSR     @ICRLF   ; CARRIAGE RETURN
55  01434 006065          JSR     @IMESS   ; MESSAGE
56  01435 003735          IPASS
57                        ;
58  01436 020217  M2OUT:   LDA     0,CSEED  ; GET CURRENT SEED
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 1  01437 040216           STA     0,SSEED ; USE AS INITIAL SEED
 2  01440 102400           SUB     0,0     ; FORM A ZERO
 3  01441 040261           STA     0,SWFLG ; ALLOW PATTERN CHANGE
 4  01442 002401           JMP     @.+1
 5  01443 004134           EDIAG
 6                  ;
 7  01444 020742  M2CRD:   LDA     0,M22   ; SECOND READ FLAG
 8  01445 101004           MOV     0,0,SZR ; SEE IF SET
 9  01446 000403           JMP     M2C2    ; YES
10  01447 010737           ISZ     M22     ; OTHERWISE SET IT
11  01450 000704           JMP     M2RD    ; DO SECOND READ
12  01451 102400  M2C2:    SUB     0,0     ; FORM A ZERO
13  01452 040734           STA     0,M22   ; RESET SECOND READ FLAG
14  01453 000740           JMP     M2C     ; CONTINUE TEST
15                  ;
16  01454 102400  P2NX:    SUB     0,0     ; FORM A ZERO
17  01455 040233           STA     0,PATF  ; RESET PATTERN PER TRACK SWITCH
18  01456 040261           STA     0,SWFLG ; RESET PATTERN CHANGE INHIBIT
19  01457 020215           LDA     0,CURPT ; GET THE CURRENT PATTERN CODE
20  01460 024110           LDA     1,C1    ; GET A ONE
21  01461 106404           SUB     0,1,SZR ; SEE IF CODE EQUAL 1
22  01462 000642  P2NX2:   JMP     M2B     ; NO  DO TEST WITH NEXT PATTERN
23  01463 000745           JMP     M2EXT   ; YES ALL DONE
24                  ;
25  01464 020217  M2B2:    LDA     0,CSEED ; GET THE CURRENT SEED
26  01465 040216           STA     0,SSEED ; USE AS INITIAL SEED
27  01466 102400           SUB     0,0     ; FORM A ZERO
28  01467 040261           STA     0,SWFLG ; ALLOW PATTERN CHANGE
29  01470 000772           JMP     P2NX2
```

```
                        ;
                        ;       TEST3 HANDLER
                        ;
                        ;       SIZE THE DISC
                        ;
                        ; 1. WRITES THE FIRST SECTOR OF EACH TRACK
                        ; 2. IGNORES DATA ERRORS
                        ; 3. EXAMINES BIT 10 TO SEE IF DIC PRESENT
                        ; 3. EXAMINES BIT 11 TO DETERMINE WRITE PROTECTED TRACKS
                        ; 4. WHEN BIT 13 SETS ASSUMES LAST WRITE WAS TO LAST TRACK ON DISC
                        ;
01471 034116  MODE3:    LDA     3,C3    ; GET A THREE
01472 054166            STA     3,MODE  ; SET CURRENT MODE
01473 074477            READS   3       ; READ THE DATA SWITCHES
01474 030150            LDA     2,EOCIN ; PRINT INHIBIT BIT
01475 173404            AND     3,2,SZR ; MASK THE SWITCHS
01476 000404            JMP     M3B
                        ;
01477 006064            JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
01500 006065            JSR     @IMESS  ; MESSAGE
01501 004042            MOD3M
01502 020167  M3B:      LDA     0,IOBUF ; GET BUFFER ADDRESS
01503 126400            SUB     1,1     ; START WITH 0
01504 044257            STA     1,MOD3T ; INITIALIZE TRACK ADDRESS
01505 044477            STA     1,DSKN  ; INITIALIZE DISC NUMBER
01506 030134  MOD3C:    LDA     2,M1    ; TIME OUT VALUE
01507 050302            STA     2,WCNTR ; SET COUNTER
01510 152400            SUB     2,2     ; FORM A ZERO
01511 050306            STA     2,RWFLG ; INDICATE WRITE
01512 065020            DOA     1,DSK   ; SET SECT ADDRESS
01513 062320            DOBP    0,DSK   ; SET BUFFER ADDRESS  AND WRITE TO DISC
01514 063620            SKPDN   DSK     ; WAIT FOR DONE
01515 006301            JSR     @IWLP   ;
                        ;
01516 070420            DIA     2,DSK   ; READ THE STATUS
01517 050204            STA     2,STERS ; SAVE THE STATUS
01520 044205            STA     1,STTS  ; T/S FOE STATUS ROUTINE
01521 034164            LDA     3,DSFAL ; GET DISC FAIL BIT
01522 157405            AND     2,3,SNR ;
01523 000403            JMP     M30
01524 006203            JSR     @ISTER  ; PRINT STATUS
01525 000572            JMP     M3H     ; GO TO NEXT TRACK
                        ;
01526 034161  M30:      LDA     3,NSDIS ; GET NO SUCH DISC BIT
01527 157404            AND     2,3,SZR ; AND TO STATUS
01530 000467            JMP     MOD3B   ;
01531 034163            LDA     3,WRERR ; GET A WRITE ERROR BIT
01532 157404            AND     2,3,SZR ; MASK STATUS
01533 000576            JMP     MOD3D   ; YES REPORT IT
                        ;
01534 074477            READS   3       ; READ THE DATA SWITCHES
01535 030135            LDA     2,PRINS ; GET THE ABORT BIT
01536 173404            AND     3,2,SZR ; MASK TO SWITCHES
01537 002214            JMP     @ISTRT
01540 030137            LDA     2,LPERS ; PRINT CYCLE COUNT SWITCH
01541 173404            AND     3,2,SZR ; SEE IF SET
01542 006244            JSR     @IPCT2  ; PRINT CYCLE COUNT
```

```
 1                      ;
 2  01543 034432  M3P:    LDA     3,M3INC ; GET SECTOR ADDRESS INCREMENT
 3  01544 167000          ADD     3,1
 4  01545 044257          STA     1,MOD3T ; SAVE      CURRENT TRACK ADDRESS
 5  01546 020436          LDA     0,DSKN  ; GET CURRENT DISC NUMBER
 6  01547 034251          LDA     3,IDSC0 ; ADDRESS OF DISC TABLE
 7  01550 117000          ADD     0,3     ; FORM POINTER INTO TABLE
 8  01551 021400          LDA     0,0,3   ; GET CURRENT DISC CODE
 9  01552 131000          MOV     1,2     ; CURRENT ADDRESS
10  01553 034427          LDA     3,DSC3  ; MASK OF DSC BITS
11  01554 173400          AND     3,2     ; MASK TO CURRENT DISC
12  01555 112415          SUB#    0,2,SNR ; SEE IF INCREMENTED PAST CURRENT DISC
13  01556 000730          JMP     MOD3C   ; NO  CONTINUE TO NEXT TRACK
14  01557 000444          JMP     M3N     ; YES PRINT LAST ADDRESS MESSAGE
15                      ;
16                      ;
17  01560 074477  M3G:    READS   3       ; READ THE DATA SWITCHES
18  01561 030150          LDA     2,EOCIN ; END OF TEST PRINT INHIBIT ?
19  01562 173404          AND     3,2,SZR ; SEE IF SET
20  01563 000405          JMP     M3OUT   ; YES
21                      ;
22  01564 006064          JSR     @ICRLF  ; CARRAGE RETURN LINE FEED
23  01565 006065          JSR     @IMESS  ; MESSAGE
24  01566 003735          IPASS
25
26  01567 074477          READS   3       ; READ THE DATA SWITCHES
27  01570 030140  M3OUT:  LDA     2,LPTST ; GET LOOP ON TEST BIT
28  01571 173404          AND     3,2,SZR ; MASK SWITCHES
29  01572 000710          JMP     M3B     ; YES  LOOP
30
31  01573 002401          JMP     @.+1
32  01574 004134          EDIAG
33                      ;
34  01575 000040  M3INC:  40
35  01576 007777  TSMSK:  7777
36                      ;
37  01577 000000  DSC0:   0
38  01600 010000  DSC1:   10000
39  01601 020000  DSC2:   20000
40  01602 030000  DSC3:   30000
41                      ;
42  01603 010000  DSINC:  10000
43  01604 000000  DSKN:   0
44  01605 042240  DSKM:   .TXTE   ! DISC  !
45  01606 051711
46  01607 120303
47  01610 000240
48  01611 047240  NODSM:  .TXTE   ! NO DISC  !
49  01612 120317
50  01613 144504
51  01614 141523
52  01615 120240
53  01616 000000
54                      ;
55  01617 044257  MOD3B:  STA     1,MOD3T ; SAVE CURRENT ADDRESS
56  01620 020756          LDA     0,TSMSK ; MASK FOR TRACK AND SECTOR
57  01621 107415          AND#    0,1,SNR ; SEE IF ANYTHING THIS DISC
58  01622 000526          JMP     M3E     ; NOTHING
```

```
                        ;
01623 124400  M3N:      NEG     1,1
01624 124000            COM     1,1     ; FORM LAST VALID ADDRESS
01625 044257            STA     1,MOD3T ; SAVE ADDRESS
01626 044174            STA     1,MXSEC ; SET MAXIMUM SECTOR
01627 074477            READS   3       ; READ DATA SWITCHES
01630 030150            LDA     2,EOCIN
01631 173404            AND     3,2,SZR ; SEE IF SET
01632 000416            JMP     M3C
01633 006064            JSR     @ICRLF  ; CARRIAGE RETURN, LINE FEED
01634 006065            JSR     @IMESS  ; PRINT MESSAGE
01635 003723            LASTV
01636 024257            LDA     1,MOD3T ; GET SAVED ADDRESS
01637 034737            LDA     3,TSMSK ; TRACK SECTOR MASK
01640 167400            AND     3,1     ; MASK OUT DISC ADDRESS
01641 006207            JSR     @IPOCT  ; PRINT ADDRESS
01642 006065  M3K:      JSR     @IMESS  ; MESSAGE
01643 001605            DSKM
01644 030123            LDA     2,C60   ; ASCII ZERO
01645 020737            LDA     0,DSKN  ; CURRENT DISC
01646 143000            ADD     2,0     ; FORM DISC NO. IN ASCII
01647 006210            JSR     @ICHAR  ; PRINT IT
                        ;
01650 024257  M3C:      LDA     1,MOD3T ; GET LAST ADDRESS
01651 034725            LDA     3,TSMSK ; MAX TRACK PER DISC
01652 167400            AND     3,1     ; MASK TO TRACK/SECTOR
01653 166415            SUB#    3,1,SNR ; SEE IF MAX FOR THIS DISC
01654 000443            JMP     M3H     ; YES GO TO NEXT DISC
01655 024257            LDA     1,MOD3T
01656 125400            INC     1,1     ; OTHERWISE GO TO NEXT TRACK OF THIS DISC
01657 020716            LDA     0,M3INC ; GET TRACK INCREMENT
01660 107000            ADD     0,1     ; SET FOR NEXT TRACK
01661 020167            LDA     0,IOBUF ; BUFFER ADDRESS
01662 030134  M3I:      LDA     2,M1    ; TIME OUT VALUE
01663 050302            STA     2,WCNTR ; SET COUNTER
01664 152400            SUB     2,2     ; FORM A ZERO
01665 050306            STA     2,RWFLG ; INDICATE WRITE
01666 065020            DOA     1,DSK   ; SET SECTOR ADDRESS
01667 062320            DOBP    0,DSK   ; SET BUFFER ADDRESS AND WRITE TO DISK
01670 063620            SKPDN   DSK     ; WAIT FOR DONE
01671 006301            JSR     @IWLP
                        ;
01672 070420            DIA     2,DSK   ; GET DISK SYSTEM STATUS
01673 050204            STA     2,STERS ; SAVE THE STATUS
01674 044205            STA     1,STTS  ; SAVE T/S FOR STATUS ROUTINE
01675 034164            LDA     3,DSFAL ; GET THE DISK FAIL BIT
01676 173404            AND     3,2,SZR ; SEE IF SET
01677 006203            JSR     @ISTER  ; YES PRINT ERROR
01700 030204            LDA     2,STERS ; RESTORE STATUS
01701 034161            LDA     3,NSDIS ; GET NO SUCH DISC BIT
01702 173405            AND     3,2,SNR ; SHOULD BE SET
01703 000464            JMP     M3J     ; OTHERWISE ERROR
                        ;
01704 034671            LDA     3,M3INC ; ADDRESS INCREMENT
01705 167000            ADD     3,1     ; FORM NEXT TRACK ADDRESS
01706 020676            LDA     0,DSKN  ; GET THE CURRENT DISC NUMBER
01707 034251            LDA     3,IDSC0 ; ADDRESS OF TABLE
01710 117000            ADD     0,3     ; FORM POINTER INTO TABLE
```

```
 1  01711 021400          LDA     0,0,3   ; GET CURRENT DISC CODE
 2  01712 131000          MOV     1,2     ; CURRENT ADDRESS
 3  01713 034667          LDA     3,DSC3  ; DISC BITS IN ADDRESS
 4  01714 173400          AND     3,2     ; MASK ADDRESS TO DISC
 5  01715 112405          SUB     0,2,SNR ; SEE IF STILL EQUAL
 6  01716 000744          JMP     M3I     ; DO NEXT TRACK THIS DISC
 7
 8  01717 010665  M3H:    ISZ     DSKN    ; INCREMENT CURRENT DISC NO.
 9  01720 030664          LDA     2,DSKN  ; GET CURRENT DISC NO.
10  01721 034100          LDA     3,C4    ; GET A FOUR
11  01722 156415          SUB#    2,3,SNR ; WHEN FOUR WE ARE DONE
12  01723 000635          JMP     M3G     ; OTHERWISE CONTINUE
13  01724 034251          LDA     3,IDSC0 ; ADDRESS OF TABLE
14  01725 157000          ADD     2,3     ; FORM OINTER INTO TABLE
15  01726 025400          LDA     1,0,3   ; GET NEXT DISC ADDRESS
16  01727 044257          STA     1,MOD3T ; SAVE CURRENT ADDRESS
17  01730 002256  M3L:    JMP     @IM3
18                        ;
19                        ;
20  01731 024257  MOD3D:  LDA     1,MOD3T ; GET THE CURRENT TRACK ADDRESS
21  01732 074477          READS   3       ; READ THE DATA SWITCHES
22  01733 030135          LDA     2,PRINS ; ABORT BIT
23  01734 173404          AND     3,2,SZR ; SEE IF SET
24  01735 002214          JMP     @ISTRT  ; TO THE BEGINNING
25  01736 030150          LDA     2,EOCIN ; SEE IF INHIBIT SET
26  01737 173404          AND     3,2,SZR ;
27  01740 000770          JMP     M3L     ; CONTINUE
28  01741 006064          JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
29  01742 006065          JSR     @IMESS  ; MESSAGE
30  01743 003065          WPROM
31  01744 024257          LDA     1,MOD3T ; CURRENT TRACK/SECTOR ADDRESS
32  01745 006207          JSR     @IPOCT  ; PRINT IT
33  01746 024257          LDA     1,MOD3T ; CURRENT TRACK/SECTOR
34  01747 002260          JMP     @IM3P
35                        ;
36  01750 074477  M3E:    READS   3       ; READ THE DATA SWITCHES
37  01751 030135          LDA     2,PRINS ; ABORT BIT
38  01752 173404          AND     3,2,SZR ; SEE IF SET
39  01753 002214          JMP     @ISTRT  ; TO THE BEGINNING
40  01754 030150          LDA     2,EOCIN ; PRINT INHIBITED ?
41  01755 173404          AND     3,2,SZR ; SEE IF SET
42  01756 000741          JMP     M3H     ; IF INHIBITED JUST CONTINUE
43                        ;
44  01757 006064          JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
45  01760 006065          JSR     @IMESS  ; MESSAGE
46  01761 001611          NODSM
47  01762 030123  M3M:    LDA     2,C60   ; ASCII ZER
48  01763 020621          LDA     0,DSKN  ; CURRENT DISC NO.
49  01764 143000          ADD     2,0     ; FORM ASCCI DISC NO.
50  01765 006210          JSR     @ICHAR  ; PRINT IT
51  01766 000731          JMP     M3H
52                        ;
53  01767 074477  M3J:    READS   3       ; GET DATA SWITCHES
54  01770 030135          LDA     2,PRINS ; ABORT BIT
55  01771 173404          AND     3,2,SZR ; SEE IF SET
56  01772 002214          JMP     @ISTRT  ; TO THE BEGINNING
57  01773 030150          LDA     2,EOCIN ; INHIBIT ERROR PRINT
58  01774 173404          AND     3,2,SZR ; SEE IF SET
```

```
 1  01775 000722          JMP     M3H     ; DO NEXT DISC
 2  01776 006064          JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
 3  01777 006065          JSR     @IMESS  ; MESSAGE
 4  02000 002004          SZERM           ; SIZING ERROR
 5  02001 006065          JSR     @IMESS  ; PRINT DISC
 6  02002 001605          DSKM
 7  02003 000757          JMP     M3M     ; DISC NUMBER
 8                  ;
 9  02004 144523  SZERM:  .TXTE   !SIZING ERROR  !
10  02005 144532
11  02006 043516
12  02007 142640
13  02010 151322
14  02011 151317
15  02012 120240
16  02013 000000
17
```

```
 1
 2                      ;
 3                      ;       TEST 4  DATA TRANSFER SECTORS
 4                      ;
 5                      ;
 6  02014 034100  MODE4:  LDA     3,C4     ; GET A FOUR
 7  02015 054166          STA     3,MODE   ; SET CURRENT MODE
 8  02016 176400          SUB     3,3      ; FORM A ZERO
 9  02017 054261          STA     3,SWFLG  ; RESET PATTERN SELECT INHIBIT
10  02020 054246          STA     3,INCE   ; ZERO INCREMENT START
11  02021 054536          STA     3,DSKAD+1 ; RESET 1-2 READ FLAG
12  02022 034110          LDA     3,C1     ; GET A ONE
13  02023 054215          STA     3,CURPT  ; INITIAL PATTERN
14  02024 074477          READS   3        ; READ THE DATA SWITCHES
15  02025 030150          LDA     2,EOCIN  ; PRINT INHIBIT BIT
16  02026 173404          AND     3,2,SZR  ; MASK THE SWITCHES
17  02027 000404          JMP     M4B
18                      ;
19  02030 006064          JSR     @ICRLF   ; CARRIAGE RETURN LINE FEED
20  02031 006065          JSR     @IMESS   ; MESSAGE
21  02032 004052          MOD4M
22  02033 074477  M4B:    READS   3        ; READ THE DATA SWITCHES
23  02034 030140          LDA     2,LPTST  ; SEE IF LOOP ON TEST IS SET
24  02035 173404          AND     3,2,SZR  ; MASK THE SWITCH SETTING
25  02036 000543          JMP     MOD4LP   ; YES GO LOOP
26                      ;
27  02037 020174          LDA     0,MXSEC  ; GET MAX SECTOR ADDRESS
28  02040 040173          STA     0,HISEC  ; SET END TEST ADDRESS
29  02041 102400          SUB     0,0      ; FORM A ZERO
30  02042 040172          STA     0,LOWSEC ; SET LOW SECTOR ADDRESS
31  02043 040412          STA     0,M4CTS  ;
32  02044 074477  MOD4A:  READS   3        ; READ DATA SWITCHES
33  02045 030144          LDA     2,RDONLY ; GET THE READ ONLY BIT
34  02046 173404          AND     3,2,SZR  ; MASK TO SWITCH SETTING
35  02047 000455          JMP     MOD4R    ; YES DO READ ONLY
36                      ;
37  02050 030217          LDA     2,CSEED  ; GET CURRENT SEED
38  02051 050216          STA     2,SSEED  ; USE AS INITIAL SEED
39                      ;
40                      ;
41  02052 006213  MOD4B:  JSR     @IPTRN   ; GENERATE TEST PATTERN
42  02053 000400          400              ; NO. OF WORDS
43  02054 014000          OBUF             ; OUT BUFFER
44  02055 000000  M4CTS:  0                ; CURRENT TRACK/SECTOR ADDRESS
45                      ;
46  02056 024777          LDA     1,M4CTS  ; GET THE START SECTOR ADDRESS
47  02057 020134  M4WLP:  LDA     0,M1     ; TIME OUT VALUE
48  02060 040302          STA     0,WCNTR  ; SET COUNTER
49  02061 102400          SUB     0,0      ; FORM A ZERO
50  02062 040306          STA     0,RWFLG  ; INDICATE WRITE
51  02063 065020          DOA     1,DSK    ; SEND IT TO THE CONTROLLER
52  02064 044771          STA     1,M4CTS  ; SAVE CURRENT ADDRESS
53  02065 030167          LDA     2,IOBUF  ; BUFFER ADDRESS
54  02066 050261          STA     2,SWFLG  ; NO MORE PATTERN CHANGE
55  02067 072320          DOBP    2,DSK    ; START WRITE
56  02070 063620          SKPDN   DSK      ; WAIT FOR DONE
57  02071 006301          JSR     @IWLP
58                      ;
```

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 1   02072 060420           DIA     0,DSK    ; READ THE STATUS
 2   02073 040204           STA     0,STERS  ; SAVE STATUS
 3   02074 044205           STA     1,STTS   ; SAVE T/S FOR STATUS ROUTINE
 4   02075 030157           LDA     2,ERROR  ; GET THE ERROR BIT
 5   02076 113404           AND     0,2,SZR  ; MASK THE STATUS
 6   02077 006203           JSR     @ISTER   ; STATUS ERROR
 7                    ;
 8   02100 074477           READS   3        ; READ THE DATA SWITCHES
 9   02101 030135           LDA     2,PRINS  ; GET THE ABORT BIT
10   02102 173404           AND     3,2,SZR  ; MASK TO SWITCHES
11   02103 002214           JMP     @ISTRT
12   02104 030137           LDA     2,LPERS  ; PRINT CYCLE COUNT SWITCH
13   02105 173404           AND     3,2,SZR  ; SEE IF SET
14   02106 006244           JSR     @IPCT2
15   02107 074477           READS   3
16                    ;
17   02110 010745           ISZ     M4CTS    ; GET CURRENT ADDRESS
18   02111 024744           LDA     1,M4CTS  ; INCREMENT TRACK/SECTOR ADDRESS
19   02112 030173           LDA     2,HISEC  ; GET MAX TRACK/SECTOR
20   02113 132423           SUBZ    1,2,SNC  ; SUBTRACT CURRENT
21   02114 000405           JMP     M4N
22                    ;
23   02115 020233           LDA     0,PATE   ; SEE IF PATTERN PER TRACK SET
24   02116 101005           MOV     0,0,SNR  ; SEE IF SET
25   02117 000740           JMP     M4WLP    ; GENERATE NEXT PATTERN
26   02120 000732           JMP     MOD4B    ; DO NEXT WRITE
27                    ;
28   02121 030145  M4N:     LDA     2,WRONLY ; GET THE WRITE ONLY BIT
29   02122 173404           AND     3,2,SZR  ; MASK THE SWITCH SETTING
30   02123 000505           JMP     MOD4W    ; YES DO WRITE ONLY
31
32                    ;
33                    ;      WRITES COMPLETED DO READS
34                    ;
35   02124 126400  MOD4R:   SUB     1,1      ; FORM A ZERO
36   02125 044246           STA     1,INCE   ; ZERO INCREMENT START
37   02126 024216           LDA     1,SSEED  ; INITIAL SEED
38   02127 044217           STA     1,CSEED  ; SET CURRENT SEED
39   02130 024172           LDA     1,LOWSEC ; GET START TRACK/SECTOR ADDRESS
40   02131 020134  M4RLP:   LDA     0,M1     ; TIME OUT VALUE
41   02132 040302           STA     0,WCNTR  ; SET COUNTER
42   02133 020110           LDA     0,C1     ; GET A ONE
43   02134 040306           STA     0,RWFLG  ; INDICATE READ
44   02135 065020           DOA     1,DSK    ; SEND IT TO CONTROLLER
45   02136 044420           STA     1,DSKAD  ; SAVE CURRENT ADDRESS
46   02137 030170           LDA     2,IIBUF  ; INPUT BUFFER
47   02140 072120           DOBS    2,DSK    ; READ THE SECTOR
48   02141 063620           SKPDN   DSK      ; WAIT FOR DONE
49   02142 006301           JSR     @IWLP
50                    ;
51   02143 060420           DIA     0,DSK    ; READ THE STATUS
52   02144 040204           STA     0,STERS  ; SAVE STATUS
53   02145 044205           STA     1,STTS   ; SAVE T/S FOR STATUS ROUTINE
54   02146 030157           LDA     2,ERROR  ; GET THE ERROR BIT
55   02147 113400           AND     0,2      ; MASK THE STATUS
56   02150 151004           MOV     2,2,SZR  ; SEE IF ERROR BIT SET
57   02151 006203           JSR     @ISTER   ; STATUS ERROR
58                    ;
```

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 1  02152 006212          JSR     @ICOMP   ; COMPARE DATA
 2  02153 000400          400              ; NO. OF WORDS
 3  02154 014000          OBUF             ; DATA WRITTEN
 4  02155 010000          IBUF             ; DATA READ
 5  02156 000000  DSKAD:  0                ; CURRENT TRACK/SECTOR
 6  02157 000000          0                ; FIRST/SECOND FLAG
 7                ;
 8                ;
 9  02160 074477          READS   3        ; READ THE DATA SWITCHES
10  02161 030135          LDA     2,PRINS  ; GET THE ABORT BIT
11  02162 173404          AND     3,2,SZR  ; MASK TO SWITCHES
12  02163 002214          JMP     @ISTRT
13  02164 030137          LDA     2,LPERS  ; PRINT CYCLE COUNT
14  02165 173404          AND     3,2,SZR  ; SEE IF SET
15  02166 006244          JSR     @IPCT2   ; PRINT CYCLE COUNT
16  02167 074477          READS   3
17                ;
18  02170 030151          LDA     2,RD2WR  ; 2 READS PER WRITE BIT
19  02171 173405          AND     3,2,SNR  ; MASK SWITCHES
20  02172 000464          JMP     CSRD     ; SECOND READ
21                ;
22  02173 024763  M4NX:   LDA     1,DSKAD  ; GET THE LAST READ TRACK/SECTOR
23  02174 125400          INC     1,1      ; INCREMENT ADDRESS
24  02175 030173          LDA     2,HISEC  ; GET THE MAX TRACK/SECTOR
25  02176 132423          SUBZ    1,2,SNC  ; SEE IF EQUAL
26  02177 000430          JMP     MOD4D
27                ;
28  02200 000731          JMP     M4RLP    ; READ NEXT SECTOR
29                ;
30                ;       GET THE LOOP PARAMETERS
31                ;
32  02201 006064  MOD4LP: JSR     @ICRLF   ; CARRIAGE RETURN LINE FEED
33  02202 006065          JSR     @IMESS   ; MESSAGE
34  02203 003010          SECP
35  02204 152400          SUB     2,2      ; GET  CHARACTERS
36  02205 006220          JSR     @IT4IN   ; READ THE TELETYPE
37  02206 000773          JMP     MOD4LP   ; ERROR
38  02207 050172          STA     2,LOWSEC  ; SET THE START SECTOR ADDRESS
39  02210 050645          STA     2,M4CTS
40                ;
41  02211 006064  M4M:    JSR     @ICRLF   ; CARRIAGE RETURN LINE FEED
42  02212 006065          JSR     @IMESS   ; MESSAGE
43  02213 003020          ESCP
44  02214 152400          SUB     2,2      ; GET CHARACTERS
45  02215 006220          JSR     @IT4IN   ; READ THE TELETYPE
46  02216 000773          JMP     M4M      ; ERROR
47  02217 050173          STA     2,HISEC  ; SET END SECTOR ADDRESS
48  02220 024172          LDA     1,LOWSEC ; GET THE LOW
49  02221 146415          SUB#    2,1,SNR  ; SEE IF HI EQUALS LOW
50  02222 000622          JMP     MOD4A    ; YES ITS OK
51  02223 146412          SUB#    2,1,SZC  ; OTHERWISE HI MUST BE GRATER
52  02224 000755          JMP     MOD4LP   ; IF NOT  TRY AGAIN
53  02225 000457          JMP     M4P
54                ;
55  02226 000616  M4O:    JMP     MOD4A    ; LINKAGE
56                ;
57                ;
58                ;       READS COMPLETED FIND WHAT TO DO NEXT
```

```
 1                      ;
 2  02227 074477  MOD4D:  READS   3         ; READ THE DATA SWITCHES
 3                      ;
 4  02230 030140  MOD4W:  LDA     2,LPTST  ; CHECK FOR LOOP ON TEST
 5  02231 173404          AND     3,2,SZR  ; MASK TO DATA SWITCHES
 6  02232 000452          JMP     M4P      ; YESS   REPEAT THE TEST
 7                      ;
 8  02233 074477          READS   3        ; READ THE DATA SWITCHES
 9  02234 030155          LDA     2,DPALL  ; MASK OF PATTERN SELECT SWITCHES
10  02235 173405          AND     3,2,SNR  ; SEE IF ALL PATTERNS SELECTED
11  02236 000437          JMP     P4NX     ; YES
12                      ;
13  02237 074477  M4EXT:  READS   3        ; READ DATA SWITCHES
14  02240 030150          LDA     2,EOCIN  ; END OF TEST PRINT INHIBIT ?
15  02241 173404          AND     3,2,SZR  ; SEE IF SET
16  02242 000406          JMP     M4OUT    ; YES
17  02243 006064          JSR     @ICRLF   ; CARRIAGE RETURN LINE FEED
18  02244 006065          JSR     @IMESS   ; MESSAGE
19  02245 003735          IPASS
20  02246 006243          JSR     @IPCNT
21                      ;
22  02247 074477          READS   3        ; READ THE DATA SWITCHES
23  02250 030135  M4OUT:  LDA     2,PRINS  ; GET THE ABORT BIT
24  02251 173404          AND     3,2,SZR  ; MASK TO SWITCHES
25  02252 002214          JMP     @ISTRT
26                      ;
27  02253 010242          ISZ     T4CY     ; INCREMENT CYCLE COUNT
28  02254 002401          JMP     @.+1
29  02255 004134          EDIAG
30                      ;
31  02256 024700  CSRD:   LDA     1,DSKAD  ; GET CURRENT ADDRESS
32  02257 030700          LDA     2,DSKAD+1 ; GET SECOND READ FLAH
33  02260 151004          MOV     2,2,SZR  ; SEE IF SET
34  02261 000407          JMP     CSRD2    ; YES
35  02262 010675          ISZ     DSKAD+1  ; SET SECOND READ FLAG
36  02263 034233          LDA     3,PATE   ; GET PATTERN PER TRACK SWITCH
37  02264 054234          STA     3,PATES  ; SAVE IT
38  02265 176400          SUB     3,3      ; FORM A ZERO
39  02266 054233          STA     3,PATE   ; RESET PATE FOR SECOND READ
40  02267 000642          JMP     M4RLP    ; DO THE SECOND READ
41  02270 152400  CSRD2:  SUB     2,2      ; FORM A ZERO
42  02271 050666          STA     2,DSKAD+1 ; RESET SECOND READ FLAG
43  02272 034234          LDA     3,PATES  ; GET THE SAVED PATE
44  02273 054233          STA     3,PATE   ;
45  02274 000677          JMP     M4NX
46                      ;
47  02275 102400  P4NX:   SUB     0,0      ; FORM A ZERO
48  02276 040233          STA     0,PATE   ; RESET PATTERN PER TRACK SWITCH
49  02277 040261          STA     0,SWFLG  ; ALLOW PATTERN CHANGE
50  02300 020215          LDA     0,CURPT  ; GET CURRENT PATTERN CODE
51  02301 024110          LDA     1,C1     ; GET A ONE
52  02302 106405          SUB     0,1,SNR  ; SEE IF A ONE
53  02303 000734          JMP     M4EXT    ; YESS ALL DONE
54  02304 020172  M4P:    LDA     0,LOWSEC ; GET START SECTOR
55  02305 042253          STA     0,@IM4   ; USE AS CURRENT SECTOR
56  02306 102400          SUB     0,0      ; FORM A ZERO
57  02307 040246          STA     0,INCE   ; START INCREMENT WITH ZERO
58  02310 040261          STA     0,SWFLG  ; ALLOW PATTERN CHANGE
```

```
 1   02311 040233          STA     0,PATE  ; RESET PATTERN PER TRACK
 2   02312 020216          LDA     0,SSEED ; GET INITIAL SEED
 3   02313 040217          STA     0,CSEED ; USE AS CURRENT SEED
 4   02314 000712          JMP     M4D
```

```
 1
 2                  ;
 3                  ;
 4                  ;        TEST 5  DATA TRANSFER SUB SECTORS
 5                  ;
 6  02315 173000  M5AA:   ADD     3,2      ; FORM SUS SECTOR DECREMENT
 7  02316 124400          NEG     1,1      ; DECREMENT COUNT
 8  02317 124000          COM     1,1
 9  02320 000444          JMP     M5AC
10                  ;
11  02321 034112  MODE5:  LDA     3,C5     ; GET A FIVE
12  02322 054166          STA     3,MODE   ; SET CURRENT MODE
13  02323 176400          SUB     3,3      ; FORM A ZERO
14  02324 054261          STA     3,SWFLG  ; RESET SELECT PATTERN INHIBIT
15  02325 054246          STA     3,INCE   ; START INCREMENT WITH ZERO
16  02326 056262          STA     3,@IM52  ; RESET 1-2 READ FLAG
17  02327 034110          LDA     3,C1     ; GET A ONE
18  02330 054215          STA     3,CURPT  ; CURRENT PATTERN CODE
19  02331 054177          STA     3,NSSC   ; DEFAULT NO. OF SUB SECTORS
20  02332 074477          READS   3        ; READ THE DATA SWITCHES
21  02333 030150          LDA     2,EOCIN  ; PRINT INHIBIT BT
22  02334 173404          AND     3,2,SZR  ; MASK THE SWITCHES
23  02335 000404          JMP     M5B
24                  ;
25  02336 006064          JSR     @ICRLF   ; CARRIAGE RETURN LINE FEED
26  02337 006065          JSR     @IMESS   ; MESSAGE
27  02340 004066          MOD5M
28                  ;
29  02341 074477  M5B:    READS   3        ; READ THE DATA SWITCHES
30  02342 030140          LDA     2,LPTST  ; SEE IF LOOP ON TEST IS SET
31  02343 173404          AND     3,2,SZR  ; MASK THE SWITCH SETTING
32  02344 002254          JMP     @IM5A    ; YES GO LOOP
33                  ;
34  02345 020174          LDA     0,MXSEC  ; GET MAX SETOR ADDRESS
35  02346 040173          STA     0,HISEC  ; SET END OF TEST ADDRESS
36  02347 020176          LDA     0,HISSC  ; GET MAX SUB SECTOR
37  02350 040227          STA     0,HSSEC  ; SET END
38  02351 102400          SUB     0,0      ; FORM A ZERO
39  02352 040172          STA     0,LOWSEC ; SET START TEST ADDRESS
40  02353 040226          STA     0,LSSEC  ; SET START SUB SECTOR
41  02354 024172  MOD5A:  LDA     1,LOWSEC ; GET START SECTOR
42  02355 046235          STA     1,@IM5
43  02356 044425          STA     1,M5CT
44  02357 024177          LDA     1,NSSC   ; NUMBER OF SUB SECTOR
45  02360 124400          NEG     1,1      ; DECREMENT IT
46  02361 124000          COM     1,1
47  02362 034120          LDA     3,C20    ; WORD COUNT INCREMENT
48  02363 030120          LDA     2,C20    ; BASIC WORD COUNT
49  02364 125004  M5AC:   MOV     1,1,SZR  ; SEE IF ZERO YET
50  02365 000730          JMP     M5AA     ; NO
51  02366 050413          STA     2,MODA
52  02367 050564          STA     2,M5AB   ; SET WORD COUNT
53  02370 052264          STA     2,@IM5AD
54                  ;
55  02371 074477  MOD5B:  READS   3
56  02372 030144          LDA     2,RDONLY ; GET THE READ ONLY BIT
57  02373 173400          AND     3,2      ; MASK TO SWITCH SETTING
58  02374 151004          MOV     2,2,SZR  ; SEE IF SET
```

```
 1  02375 000513          JMP     MOD5R   ; YES DO READ ONLY
 2                ;
 3  02376 030217          LDA     2,CSEED ; GET CURRENT SEED
 4  02377 050216          STA     2,SSEED ; USE AS INITIAL SEED
 5                ;
 6                ;
 7  02400 006213          JSR     @IPTRN  ; GENERATE TEST PATTERN
 8  02401 000020  MODA:   20              ; NO. OF WORDS
 9  02402 014000          OBUF            ; OUT BUFFER
10  02403 000000  M5CT:   0               ; CURRENT TRACK/SECTOR ADDRESS
11                ;
12  02404 024172  M5WA:   LDA     1,LOWSEC  ; GET THE START SECTOR ADDRESS
13  02405 030236          LDA     2,SSONE ; INITIAL SUB SECTOR ADDRESS
14  02406 050261          STA     2,SWFLG ; NO MORE PATTERN CHANGE
15  02407 034226          LDA     3,LSSEC ; GET THE START SUB SECTOR
16  02410 020177          LDA     0,NSSC  ; NUMBER OF SUB SECTORS
17  02411 100400          NEG     0,0     ; DECREMENT
18  02412 100000          COM     0,0
19  02413 112400          SUB     0,2     ;
20  02414 175320          MOVZS   3,3     ; SHIFT TO HI BYTE
21  02415 177120          ADDZL   3,3     ; SHIFT 2 MORE BITS
22  02416 177120          ADDZL   3,3     ; SHIFT 2 MORE BITS
23  02417 173000          ADD     3,2     ; FORM START SUB SECTOR ADDRESS
24                ;
25  02420 020134  M5WLP:  LDA     0,M1    ; TIME OUT VALUE
26  02421 040302          STA     0,WCNTR ; SET COUNTER
27  02422 102400          SUB     0,0     ; FORM A ZERO
28  02423 040306          STA     0,RWFLG ; INDICATE WRITE
29  02424 065020          DOA     1,DSK   ; SEND IT TO THE CONTROLLER
30  02425 034167          LDA     3,IOBUF ; BUFFER ADDRESS
31  02426 076020          DOB     3,DSK   ; START WRITE
32  02427 073320          DOCP    2,DSK   ; WRITE A SUB SECTOR
33  02430 063620          SKPDN   DSK     ; WAIT FOR DONE
34  02431 006301          JSR     @IWLP
35                ;
36  02432 060420          DIA     0,DSK   ; READ THE STATUS
37  02433 040204          STA     0,STERS ;
38  02434 044205          STA     1,STTS  ; SAVE T/S FOR STATUS ROUTINE
39  02435 034157          LDA     3,ERROR ; GET THE ERROR BIT
40  02436 117400          AND     0,3     ; MASK THE STATUS
41  02437 175004          MOV     3,3,SZR ; SEE IF ERROR BIT SET
42  02440 006203          JSR     @ISTER  ; STAUS ERROR
43                ;
44  02441 074477          READS   3       ; READ THE DATA SWITCHES
45  02442 020135          LDA     0,PRINS ; GET THE ABORT BIT
46  02443 163404          AND     3,0,SZR ; MASK TO SWITCHES
47  02444 002214          JMP     @ISTRT
48                ;
49  02445 030137          LDA     2,LPERS ; PRINT CYCLE COUNT ?
50  02446 173404          AND     3,2,SZR ; SEE IF SET
51  02447 006244          JSR     @IPCT2  ; PRINT CYCLE COUNT
52                ;
53  02450 020177          LDA     0,NSSC  ; GET NO. OF SUB SECTORS
54  02451 040200          STA     0,WRK1  ; SAVE IT
55  02452 102400          SUB     0,0     ; FORM A ZERO
56  02453 034237          LDA     3,SSINC ; SUB SECTOR INCREMENT
57  02454 163000  AD:     ADD     3,0     ;
58  02455 014200          DSZ     WRK1    ; DECREMENT COUNT
```

```
    02456 000776            JMP     AD      ; REPEAT
                    ;
    02457 113022            ADDZ    0,2,SZC ;
    02460 000411            JMP     M5L     ;
    02461 034227            LDA     3,HSSEC ; GET MAX SUB SECTOR
    02462 175320            MOVZS   3,3     ; SHIFT TO HI BYTE
    02463 177120            ADDZL   3,3     ; SHIFT 2 MORE BITS
    02464 177120            ADDZL   3,3     ; SHIFT 2 MORE BITS
    02465 020236            LDA     0,SSONE ; ONE SUB SECTOR
    02466 117000            ADD     0,3     ; FORM MAX SUB SECTOR ADDRESS
    02467 156422            SUBZ    2,3,SZC ; SEE IF MAX YET
    02470 002255            JMP     @IM5C
                    ;
    02471 125400  M5L:      INC     1,1     ; INCREMENT TRACK/SECTOR ADDRESS
    02472 030236            LDA     2,SSONE ; RESET SUB SECTOR ADDRESS
    02473 034226            LDA     3,LSSEC ; GET THE START SUB SECTOR
    02474 175320            MOVZS   3,3     ; SHIFT TO HI BYTE
    02475 177120            ADDZL   3,3     ; SHIFT 2 MORE BITS
    02476 177120            ADDZL   3,3     ; SHIFT 2 MORE BITS
    02477 173000            ADD     3,2     ; FORM START SUB SECTOR ADDRESS
    02500 020173            LDA     0,HISEC ; GET MAX TRACK/SECTOR
    02501 101400            INC     0,0
    02502 122424            SUBZ    1,0,SZR ; SUBTRACT CURRENT
    02503 002255            JMP     @IM5C
                    ;
    02504 074477            READS   3       ; READ DATA SWITCHES
    02505 030145            LDA     2,WRONLY ; GET THE WRITE ONLY BIT
    02506 173404            AND     3,2,SZR ; MASK THE SWITCH SETTING
    02507 002263            JMP     @IM5W   ; YES DO WRITE ONLY
                    ;
                    ;       WRITES COMPLETED DO READS
                    ;
    02510 126400  MOD5R:    SUB     1,1     ; FORM A ZERO
    02511 044246            STA     1,INCE  ; START INCREMENT WITH ZERO
    02512 024216            LDA     1,SSEED ; INITIAL SEED
    02513 044217            STA     1,CSEED ; USE AS CURRENT SEED
    02514 024172            LDA     1,LOWSEC ; GET START TRACK/SECTOR ADDRESS
    02515 030236            LDA     2,SSONE ; INITIAL SUB SECTOR ADDRESS
    02516 034226            LDA     3,LSSEC ; GET THE START SUB SECTOR
    02517 020177            LDA     0,NSSC  ; NUMBER OF SUB SECTORS
    02520 100400            NEG     0,0     ; DECREMTNIT
    02521 100000            COM     0,0
    02522 112400            SUB     0,2
    02523 175320            MOVZS   3,3     ; SHIFT TO HI BYTE
    02524 177120            ADDZL   3,3     ; SHIFT 2 MORE BITS
    02525 177120            ADDZL   3,3     ; SHIFT 2 MORE BITS
    02526 173000            ADD     3,2     ; FORM START SUB SECTOR ADDRESS
                    ;
    02527 020134  M5RLP:    LDA     0,M1    ; TIME OUT VALUE
    02530 040302            STA     0,WCNTR ; SET COUNTER
    02531 020110            LDA     0,C1    ; GET A ONE
    02532 040306            STA     0,RWFLG ; INDICATE READ
    02533 065020            DOA     1,DSK   ; SEND IT TO CONTROLLER
    02534 034170            LDA     3,IIBUF ; INPUT BUFFER
    02535 076020            DOB     3,DSK   ; READ THE SECTOR
    02536 073120            DOCS    2,DSK
    02537 063620            SKPDN   DSK     ; WAIT FOR DONE
    02540 006301            JSR     @IWLP
```

```
 1                      ;
 2   02541 060420               DIA     0,DSK    ; READ THE STATUS
 3   02542 040204               STA     0,STERS  ; SAVE STATUS
 4   02543 044205               STA     1,STTS   ; SAVE T/S FOR STAUS ROUTINE
 5   02544 034157               LDA     3,ERROR  ; GET THE ERROR BIT
 6   02545 117400               AND     0,3      ; MASK THE STATUS
 7   02546 175004               MOV     3,3,SZR  ; SEE IF ERROR BIT SET
 8   02547 006203               JSR     @ISTER   ; STATUS ERROR
 9                      ;
10   02550 044406               STA     1,DSK5   ; SAVE  CURRENT TRACK/SECTOR
11   02551 050252               STA     2,DSK6   ; SAVE CURRENT SUB SECTOR
12   02552 006212               JSR     @ICOMP   ; COMPARE DATA
13   02553 000020   M5AB:       20               ; NO. OF WORDS
14   02554 014000               OBUF             ; DATA WRITTEN
15   02555 010000               IBUF             ; DATA READ
16   02556 000000   DSK5 :      0                ; CURRENT TRACK/SECTOR
17   02557 000000   M52:        0                ; FIRST/SECOND FLAG
18                      ;
19                      ;
20   02560 074477               READS   3        ; READ THE DATA SWITCHES
21   02561 030135               LDA     2,PRINS  ; GET THE ABORT BIT
22   02562 173404               AND     3,2,SZR  ; MASK TO SWITCHES
23   02563 002214               JMP     @ISTRT
24                      ;
25   02564 030137               LDA     2,LPERS  ; PRINT CYCLE COUNT ?
26   02565 173404               AND     3,2,SZR  ; SEE IF SET
27   02566 006244               JSR     @IPCT2   ; PRINT CYCLE COUNT
28   02567 074477               READS   3
29                      ;
30   02570 024766               LDA     1,DSK5   ; RESTORE SECTOR ADDRESS
31   02571 030252               LDA     2,DSK6   ; RESTOR SUB SECTOR
32   02572 020151               LDA     0,RD2WR  ; 2 READS PER WRITE
33   02573 163405               AND     3,0,SNR  ; SEE IF SET
34   02574 000557               JMP     M5S      ; DO SECOND READ
35                      ;
36   02575 020177   M5Q:        LDA     0,NSSC   ; NO. OF    SUB SECTOR
37   02576 040200               STA     0,WRK1   ; SAVE IT
38   02577 102400               SUB     0,0      ; FORM A ZERO
39   02600 034237               LDA     3,SSINC  ; SUB SECTOR INCREMENT
40   02601 163000               ADD     3,0      ;
41   02602 014200               DSZ     WRK1     ; DECREMENT COUNT
42   02603 000776               JMP     .-2
43                      ;
44   02604 113022               ADDZ    0,2,SZC  ;
45   02605 000411               JMP     M5M      ;
46   02606 034227               LDA     3,HSSEC  ; GET MAX SUB SECTOR
47   02607 175320               MOVZS   3,3      ; SHIFT TO HI BYTE
48   02610 177120               ADDZL   3,3      ; SHIFT 2 MORE BITS
49   02611 177120               ADDZL   3,3      ; SHIFT 2 MORE BITS
50   02612 020236               LDA     0,SSONE  ; ONE SUB SECTOR
51   02613 117000               ADD     0,3      ; FORM MAX SUB SECTOR ADDRESS
52   02614 156422               SUBZ    2,3,SZC  ; SEE IF MAX YET
53   02615 000712               JMP     M5RLP
54                      ;
55   02616 034173   M5M:        LDA     3,HISEC  ; GET THE MAX TRACK/SECTOR
56   02617 136425               SUBZ    1,3,SNR  ; SEE IF EQUAL
57   02620 000500               JMP     MOD5D
58                      ;
```

```
 1  02621 125400  M5R:     INC      1,1      ; INCREMENT CURRENT TRACK/SECTOR
 2  02622 030236           LDA      2,SSONE  ; INITIAL SUB SECTOR ADDRESS
 3  02623 034226           LDA      3,LSSEC  ; GET THE START SUB SECTOR
 4  02624 175320           MOVZS    3,3      ; SHIFT TO HI BYTE
 5  02625 177120           ADDZL    3,3      ; SHIFT 2 MORE BITS
 6  02626 177120           ADDZL    3,3      ; SHIFT 2 MORE BITS
 7  02627 173000           ADD      3,2      ; FORM START SUB SECTOR ADDRESS
 8  02630 000677  M5V:     JMP      M5RLP    ; READ NEXT SECTOR
 9                        ;
10                        ;        GET THE LOOP PARAMETERS
11                        ;
12  02631 006064  MOD5LP: JSR      @ICRLF   ; CARRIAGE RETURN LINE FEED
13  02632 006065           JSR      @IMESS   ; MESSAGE
14  02633 003010           SECP
15  02634 152400           SUB      2,2      ; GET  CHARACTERS
16  02635 006220           JSR      @IT4IN   ; READ THE TELETYPE
17  02636 000773           JMP      MOD5LP   ; ERROR
18  02637 050172           STA      2,LOWSEC  ; SET THE START SECTOR ADDRESS
19                        ;
20  02640 006064  M5O:     JSR      @ICRLF   ; CARRIAGE RETURN LINE FEED
21  02641 006065           JSR      @IMESS   ; MESSAGE
22  02642 003020           ESCP
23  02643 152400           SUB      2,2      ; GET  CHARACTERS
24  02644 006220           JSR      @IT4IN   ; READ THE TELETYPE
25  02645 000773           JMP      M5O      ; ERROR
26  02646 024172           LDA      1,LOWSEC ; GET LOW SECTOR ADDRESS
27  02647 146415           SUB#     2,1,SNR  ; SEE IF EQUAL
28  02650 000403           JMP      M5U      ; EQUAL IS OK
29  02651 146432           SUBZ#    2,1,SZC   ; HI SEC SHOULD BE GREATER
30  02652 000757           JMP      MOD5LP   ; OTHERWISE TRY AGAIN
31  02653 050173  M5U:     STA      2,HISEC  ; SET END SECTOR ADDRESS
32                        ;
33  02654 006064  M5K:     JSR      @ICRLF   ; CARRIAGE RETURN LINE FEED
34  02655 006065           JSR      @IMESS   ; MESSAGE
35  02656 003027           SSECP
36  02657 152400           SUB      2,2      ; GET  CHARACTERS
37  02660 006220           JSR      @IT4IN   ; READ TTY
38  02661 000773           JMP      M5K      ; ERROR
39  02662 050226           STA      2,LSSEC  ; SET START SUB SECTOR
40                        ;
41  02663 006064  M5N:     JSR      @ICRLF   ; CARRIAGE RETURN LINE FEED
42  02664 006065           JSR      @IMESS   ; MESSAGE
43  02665 003041           SESCP
44  02666 152400           SUB      2,2      ; GET CHARACTERS
45  02667 006220           JSR      @IT4IN   ; READ THE TTY
46  02670 000773           JMP      M5N      ; ERROR
47  02671 024226           LDA      1,LSSEC  ; GET LOW SUB SECTOR
48  02672 146415           SUB#     2,1,SNR  ; SEE IF EQUAL
49  02673 000403           JMP      M5P      ; EQUAL OK
50  02674 146432           SUBZ#    2,1,SZC  ; HI MUST BE GREATER
51  02675 000757           JMP      M5K
52  02676 024176  M5P:     LDA      1,HISSC  ; GET MAX SUB SECTOR
53  02677 146433           SUBZ#    2,1,SNC  ; SEE IF PAST MAX
54  02700 000754           JMP      M5K      ; YES
55  02701 050227           STA      2,HSSEC  ; SET END SUB SECTOR
56                        ;
57  02702 006064  M5Z:     JSR      @ICRLF   ; CARRIAGE RETURN LINE FEED
58  02703 006065           JSR      @IMESS   ; MESSAGE
```

```
 1  02704 003052          NSSCM             ; NO SUB SECTORS MESSAGE
 2  02705 152400          SUB     2,2       ; GET CHARACTERS
 3  02706 006220          JSR     @IT4IN    ; READ TTY
 4  02707 000773          JMP     M5Z       ; TRY AGAIN IF ERROR
 5  02710 151005          MOV     2,2,SNR   ; SEE IF ZERO
 6  02711 000720          JMP     MOD5LP    ; RESET ALL ON ZERO
 7  02712 024120          LDA     1,C20     ; MAX SUB SECTOR
 8  02713 146433          SUBZ#   2,1,SNC   ; SEE IF GRATER
 9  02714 000766          JMP     M5Z       ; YES  NO  GGOOD
10  02715 050177          STA     2,NSSC    ; SET NO OF SUB SECTORS
11  02716 002401          JMP     @.+1
12  02717 002354          MOD5A
13                  ;
14                  ;       READS COMPLETED FIND WHAT TO DO NEXT
15                  ;
16  02720 074477  MOD5D:  READS   3         ; READ THE DATA SWITCHES
17                  ;
18  02721 030140  MOD5W:  LDA     2,LPTST   ; CHECK FOR LOOP ON TEST
19  02722 173404          AND     3,2,SZR   ; MASK TO DATA SWITCHES
20  02723 000455          JMP     M5Y       ; YESS   REPEAT THE TEST
21                  ;
22  02724 030155          LDA     2,DPALL   ; MASK TO PATTERN SELECT DATA SWITCHES
23  02725 173404          AND     3,2,SZR   ; SEE IF ALL PATTERNS SELECTED
24  02726 000443          JMP     P5NX      ; YES
25                  ;
26  02727 030150  M5EXT:  LDA     2,EOCIN   ; END OF TEST PRINT INHIBIT ?
27  02730 173404          AND     3,2,SZR   ; SEE IF SE
28  02731 000770          JMP     MOD5W     ; YES
29                  ;
30  02732 006064          JSR     @ICRLF    ; CARRIAGE RETURN LINE FEED
31  02733 006065          JSR     @IMESS    ; MESSAGE
32  02734 003735          IPASS
33                  ;
34  02735 002401          JMP     @.+1
35  02736 004134          EDIAG
36                  ;
37  02737 034233  M5CFP:  LDA     3,PATE    ; GET PATTERN PER SECTOR FLAG
38  02740 175005          MOV     3,3,SNR   ; SEE IF SET
39  02741 002241          JMP     @IMW5     ; NO
40  02742 044614          STA     1,DSK5    ; SAVE AC 1
41  02743 050252          STA     2,DSK6    ; SAVE AC 2
42                  ;
43  02744 006213          JSR     @IPTRN    ; GENERATE THE PATTERN
44  02745 000020  M5AD:   20
45  02746 014000          OBUF
46  02747 000000  M5CTS:  0
47                  ;
48  02750 024606          LDA     1,DSK5    ; RESTORE AC 1
49  02751 030252          LDA     2,DSK6    ; RESTORE AC 2
50  02752 002241          JMP     @IMW5
51                  ;
52                  ;       ROUTINE TO CHECK FOR SECOND READ
53                  ;
54  02753 022262  M5S:    LDA     0,@IM52   ; SECOND READ FLAG
55  02754 101004          MOV     0,0,SZR   ; SEE IF SET
56  02755 000407          JMP     M5T       ; IS SET
57  02756 012262          ISZ     @IM52     ; OTHERWISE SET THE FLAG
58  02757 020233          LDA     0,PATE    ; GET THE PATTERN PR TRACK SWITCH
```

```
 1  02760 040234           STA     0,PATES ; SAVE IT
 2  02761 102400           SUB     0,0     ; FORM A ZERO
 3  02762 040233           STA     0,PATE  ; RESET PATTERN PER TRACK FOR SECOND READ
 4  02763 000645           JMP     M5V     ; DO THE SECOND READ
 5                         ;
 6  02764 020234  M5T:     LDA     0,PATES ; GET THE PATTERN SWITCH
 7  02765 040233           STA     0,PATE
 8  02766 102400           SUB     0,0     ; FORM A ZERO
 9  02767 042262           STA     0,@IM52 ; RESET SECOND READ FLAG
10  02770 002300           JMP     @IM5Q   ; READ NEXT SUB SECTOR
11                         ;
12  02771 102400  P5NX:    SUB     0,0     ; FORM A ZERO
13  02772 040233           STA     0,PATE  ; RESET PATTERN PER TRACK SWITCH
14  02773 040261           STA     0,SWFLG ; ALLOW PATTERN CHANGE
15  02774 020215           LDA     0,CURPT ; GET CURRENT PATTERN CODE
16  02775 024110           LDA     1,C1    ; GET A ONE
17  02776 106405           SUB     0,1,SNR ; SEE IF DONE
18  02777 000730           JMP     M5EXT   ; YES
19  03000 102400  M5Y:     SUB     0,0     ; FORM A ZERO
20  03001 040246           STA     0,INCE  ; START INCREMENTING WITH ZERO
21  03002 040261           STA     0,SWFLG ; ALLOW PATTERN CHANGE
22  03003 040233           STA     0,PATE  ; RESET PATTERN PER TRACK
23  03004 020216           LDA     0,SSEED ; GET INITIAL SEED
24  03005 040217           STA     0,CSEED ; USE AS CURRENT SEED
25  03006 002240           JMP     @IMD5
26                         ;
27                         ;
28  03007 000000  ECODE:   0
29        000010           .RDX 8
30  03010 152123  SECP:    .TXTE !START SECTOR  !
31  03011 151101
32  03012 120324
33  03013 142523
34  03014 152303
35  03015 151317
36  03016 120240
37  03017 000000
38
39  03020 047305  ESCP:    .TXTE !END SECTOR  !
40  03021 120104
41  03022 142523
42  03023 152303
43  03024 151317
44  03025 120240
45  03026 000000
46
47  03027 152123  SSECP:   .TXTE !START SUB SECTOR  !
48  03030 151101
49  03031 120324
50  03032 052523
51  03033 120102
52  03034 142523
53  03035 152303
54  03036 151317
55  03037 120240
56  03040 000000
57
58  03041 047305  SESCP:   .TXTE !END SUB SECTOR  !
```

```
 1   03042 120104
 2   03043 052523
 3   03044 120102
 4   03045 142523
 5   03046 152303
 6   03047 151317
 7   03050 120240
 8   03051 000000
 9
10   03052 147516  NSSCM:  .TXTE !NO. OF SUB SECTORS   !
11   03053 120056
12   03054 143317
13   03055 051640
14   03056 041125
15   03057 051640
16   03060 141705
17   03061 147724
18   03062 051722
19   03063 120240
20   03064 000240
21
22   03065 151327  WPROM:  .TXTE !WRITE PROTECT ADDRESS   !
23   03066 152311
24   03067 120305
25   03070 151120
26   03071 152317
27   03072 141705
28   03073 120324
29   03074 042101
30   03075 151104
31   03076 051705
32   03077 120123
33   03100 120240
34   03101 000000
35
36   03102 142523  SSWM1:  .TXTE !SET DATA SWITCHES - CONTINUE !
37   03103 120324
38   03104 040504
39   03105 040724
40   03106 051640
41   03107 144727
42   03110 141724
43   03111 142510
44   03112 120123
45   03113 120055
46   03114 147703
47   03115 152116
48   03116 047311
49   03117 142525
50   03120 000240
51
52
53   03121 040504  INST1:  .TXTE !DATA SWITCHES !
54   03122 040724
55   03123 051640
56   03124 144727
57   03125 141724
58   03126 142510
```

```
 1   03127 120123
 2   03130 000000
 3
 4   03131 120060  INST2:   .TXTE !0 ABORTS TEST !
 5   03132 041101
 6   03133 151317
 7   03134 051724
 8   03135 152240
 9   03136 051705
10   03137 120324
11   03140 000000
12
13   03141 120261  INST3:   .TXTE !1 HALT ON ERROR !
14   03142 040510
15   03143 152314
16   03144 147640
17   03145 120116
18   03146 151305
19   03147 147722
20   03150 120322
21   03151 000000
22
23   03152 120262  INST4:   .TXTE !2 PRINT CYCLE COUNT !
24   03153 151120
25   03154 047311
26   03155 120324
27   03156 054703
28   03157 146303
29   03160 120305
30   03161 147703
31   03162 047125
32   03163 120324
33   03164 000000
34
35   03165 120063  INST5:   .TXTE !3 LOOP ON TEST !
36   03166 147714
37   03167 050317
38   03170 147640
39   03171 120116
40   03172 142724
41   03173 152123
42   03174 000240
43
44   03175 126264  INST6:   .TXTE !4, 5, 6, SELECT TEST !
45   03176 032640
46   03177 120254
47   03200 126066
48   03201 051640
49   03202 146305
50   03203 141705
51   03204 120324
52   03205 142724
53   03206 152123
54   03207 000240
55
56   03210 120060  INST7:   .TXTE !0 0 0 => TESTS 1 THRU 4 !
57   03211 120060
58   03212 120060
```

```
 1  03213 137275
 2  03214 152240
 3  03215 051705
 4  03216 051724
 5  03217 130640
 6  03220 152240
 7  03221 151110
 8  03222 120125
 9  03223 120264
10  03224 000000
11
12  03225 120060  INST8:  .TXTE !0 0 1 => TEST 1 DISCRETE CONTROLLER TESTS !
13  03226 120060
14  03227 120261
15  03230 137275
16  03231 152240
17  03232 051705
18  03233 120324
19  03234 120261
20  03235 144504
21  03236 141523
22  03237 142722
23  03240 142724
24  03241 141640
25  03242 047317
26  03243 151324
27  03244 146317
28  03245 142714
29  03246 120322
30  03247 142724
31  03250 152123
32  03251 120123
33  03252 000000
34
35  03253 120060  INST9:  .TXTE !0 1 0 => TEST 2 DIAGNOSTIC MODE !
36  03254 120261
37  03255 120060
38  03256 137275
39  03257 152240
40  03260 051705
41  03261 120324
42  03262 120262
43  03263 144504
44  03264 043501
45  03265 147516
46  03266 152123
47  03267 141711
48  03270 046640
49  03271 042317
50  03272 120305
51  03273 000000
52
53  03274 120060  INSTA:  .TXTE !0 1 1 => TEST 3 SIZE/WRITE PROTECT !
54  03275 120261
55  03276 120261
56  03277 137275
57  03300 152240
58  03301 051705
```

```
 1   03302 120324
 2   03303 120063
 3   03304 144523
 4   03305 142532
 5   03306 153657
 6   03307 144722
 7   03310 142724
 8   03311 050240
 9   03312 147722
10   03313 142724
11   03314 152303
12   03315 000240
13
14   03316 120261   INSTB:   .TXTE !1 0 0 => TEST 4 DATA TRANSFER (SECTOR) !
15   03317 120060
16   03320 120060
17   03321 137275
18   03322 152240
19   03323 051705
20   03324 120324
21   03325 120264
22   03326 040504
23   03327 040724
24   03330 152240
25   03331 040722
26   03332 051516
27   03333 142706
28   03334 120322
29   03335 051450
30   03336 141705
31   03337 147724
32   03340 124722
33   03341 000240
34
35   03342 120261   INSTC:   .TXTE !1 0 1 => TEST 5 DATA TRANSFER (SUB SECTOR) !
36   03343 120060
37   03344 120261
38   03345 137275
39   03346 152240
40   03347 051705
41   03350 120324
42   03351 120065
43   03352 040504
44   03353 040724
45   03354 152240
46   03355 040722
47   03356 051516
48   03357 142706
49   03360 120322
50   03361 051450
51   03362 041125
52   03363 051640
53   03364 141705
54   03365 147724
55   03366 124722
56   03367 000240
57
58   03370 120261   INSTD:   .TXTE !1 1 0 => TESTS 1, 2 AND 4 !
```

```
 1   03371 120261
 2   03372 120060
 3   03373 137275
 4   03374 152240
 5   03375 051705
 6   03376 051724
 7   03377 130640
 8   03400 120254
 9   03401 120262
10   03402 047101
11   03403 120104
12   03404 120264
13   03405 000000
14
15   03406 120261  INSTE:  .TXTE !1 1 1 => TESTS 2 AND 4 !
16   03407 120261
17   03410 120261
18   03411 137275
19   03412 152240
20   03413 051705
21   03414 051724
22   03415 131240
23   03416 040640
24   03417 042116
25   03420 132240
26   03421 000240
27
28   03422 120267  INSTF:  .TXTE !7 READ ONLY !
29   03423 142722
30   03424 042101
31   03425 147640
32   03426 146116
33   03427 120131
34   03430 000000
35
36   03431 120270  INSTG:  .TXTE !8 WRITE ONLY !
37   03432 151327
38   03433 152311
39   03434 120305
40   03435 047317
41   03436 054714
42   03437 000240
43
44   03440 120071  INSTH:  .TXTE !9 INHIBIT DATA ERROR PRINT !
45   03441 047311
46   03442 144510
47   03443 144502
48   03444 120324
49   03445 040504
50   03446 040724
51   03447 142640
52   03450 151322
53   03451 151317
54   03452 050240
55   03453 144722
56   03454 152116
57   03455 000240
58
```

```
 1   03456 030261   INSTI:   .TXTE !10 INHIBIT STATUS ERROR PRINT !
 2   03457 144640
 3   03460 044116
 4   03461 041311
 5   03462 152311
 6   03463 051640
 7   03464 040724
 8   03465 052724
 9   03466 120123
10   03467 151305
11   03470 147722
12   03471 120322
13   03472 151120
14   03473 047311
15   03474 120324
16   03475 000000
17
18   03476 130661   INSTJ:   .TXTE !11 INHIBIT END OF TEST PRINT ! /
19   03477 144640
20   03500 044116
21   03501 041311
22   03502 152311
23   03503 142640
24   03504 042116
25   03505 147640
26   03506 120306
27   03507 142724
28   03510 152123
29   03511 050240
30   03512 144722
31   03513 152116
32   03514 000240
33
34   03515 131261   INSTK:   .TXTE !12 TWO READS PER WRITE INHIBIT !
35   03516 152240
36   03517 147727
37   03520 151240
38   03521 040705
39   03522 051504
40   03523 050240
41   03524 151305
42   03525 153640
43   03526 144722
44   03527 142724
45   03530 144640
46   03531 044116
47   03532 041311
48   03533 152311
49   03534 000240
50
51   03535 031661   INSTL:   .TXTE !13, 14, 15 SELECT DATA PATTERN !
52   03536 120254
53   03537 132261
54   03540 120254
55   03541 032661
56   03542 051640
57   03543 146305
58   03544 141705
```

```
 1  03545 120324
 2  03546 040504
 3  03547 040724
 4  03550 050240
 5  03551 152101
 6  03552 142724
 7  03553 047322
 8  03554 000240
 9
10  03555 030240  INSTM:  .TXTE ! 0   0   0 => ALL PATTERNS !
11  03556 120240
12  03557 030240
13  03560 120240
14  03561 030240
15  03562 136640
16  03563 120276
17  03564 146101
18  03565 120314
19  03566 040520
20  03567 152324
21  03570 151305
22  03571 051516
23  03572 000240
24
25  03573 030240  INSTN:  .TXTE ! 0   0   1 => RANDOM !
26  03574 120240
27  03575 030240
28  03576 120240
29  03577 130640
30  03600 136640
31  03601 120276
32  03602 040722
33  03603 042116
34  03604 046717
35  03605 000240
36
37  03606 030240  INSTO:  .TXTE ! 0   1   0 => INCREMENTING !
38  03607 120240
39  03610 130640
40  03611 120240
41  03612 030240
42  03613 136640
43  03614 120276
44  03615 047311
45  03616 151303
46  03617 046705
47  03620 047305
48  03621 144724
49  03622 043516
50  03623 000240
51
52  03624 030240  INSTP:  .TXTE ! 0   1   1 => TRACK/SECTOR ID !
53  03625 120240
54  03626 130640
55  03627 120240
56  03630 130640
57  03631 136640
58  03632 120276
```

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 1   03633 151324
 2   03634 141501
 3   03635 127513
 4   03636 142523
 5   03637 152303
 6   03640 151317
 7   03641 144640
 8   03642 120104
 9   03643 000000
10
11   03644 130640  INSTQ:  .TXTE ! 1   0   0 => WORST CASE !
12   03645 120240
13   03646 030240
14   03647 120240
15   03650 030240
16   03651 136640
17   03652 120276
18   03653 147727
19   03654 051722
20   03655 120324
21   03656 040703
22   03657 142523
23   03660 000240
24
25   03661 130640  INSTR:  .TXTE ! 1   0   1 => ONES !
26   03662 120240
27   03663 030240
28   03664 120240
29   03665 130640
30   03666 136640
31   03667 120276
32   03670 047317
33   03671 051705
34   03672 000240
35
36   03673 130640  INSTS:  .TXTE ! 1   1   0 => ZEROES !
37   03674 120240
38   03675 130640
39   03676 120240
40   03677 030240
41   03700 136640
42   03701 120276
43   03702 142532
44   03703 147722
45   03704 051705
46   03705 000240
47
48   03706 130640  INSTT:  .TXTE ! 1   1   1 => SELECTABLE !
49   03707 120240
50   03710 130640
51   03711 120240
52   03712 130640
53   03713 136640
54   03714 120276
55   03715 142523
56   03716 142714
57   03717 152303
58   03720 041101
```

```
 1  03721 142714
 2  03722 000240
 3
 4                        ;
 5  03723 040714  LASTV:  .TXTE !LAST VALID ADDRESS !
 6  03724 152123
 7  03725 053240
 8  03726 146101
 9  03727 042311
10  03730 040640
11  03731 042104
12  03732 142722
13  03733 051523
14  03734 000240
15
16                        ;
17  03735 026705  IPASS:  .TXTE !E-O-T !
18  03736 026717
19  03737 120324
20  03740 000000
21
22  03741 030270  LOCKIT: .TXTE !8010 DISC SYSTEM TEST PROGRAM !
23  03742 030261
24  03743 042240
25  03744 051711
26  03745 120303
27  03746 054523
28  03747 152123
29  03750 046705
30  03751 152240
31  03752 051705
32  03753 120324
33  03754 151120
34  03755 043717
35  03756 040722
36  03757 120115
37  03760 000000
38
39  03761 054724  DEVNUM: .TXTE !TYPE 2 DIGIT DISK DEVICE CODE (20 OR 60)!
40  03762 142520
41  03763 131240
42  03764 042240
43  03765 043711
44  03766 152311
45  03767 042240
46  03770 051711
47  03771 120113
48  03772 142504
49  03773 144526
50  03774 142703
51  03775 141640
52  03776 042317
53  03777 120305
54  04000 131050
55  04001 120060
56  04002 151317
57  04003 033240
58  04004 124460
```

```
 1  04005 000000
 2
 3
 4  04006 144504  MOD1M:   .TXTE !DISCRETE CONTROLLER TESTS!
 5  04007 141523
 6  04010 142722
 7  04011 142724
 8  04012 141640
 9  04013 047317
10  04014 151324
11  04015 146317
12  04016 142714
13  04017 120322
14  04020 142724
15  04021 152123
16  04022 000123
17
18  04023 050303  MOD2M:   .TXTE !CPU-CONTROLLER DATA PATH TEST!
19  04024 026525
20  04025 147703
21  04026 152116
22  04027 147722
23  04030 146314
24  04031 151305
25  04032 042240
26  04033 152101
27  04034 120101
28  04035 040520
29  04036 044324
30  04037 152240
31  04040 051705
32  04041 000324
33
34  04042 144504  MOD3M:   .TXTE !DISC SIZE TEST!
35  04043 141523
36  04044 051640
37  04045 055311
38  04046 120305
39  04047 142724
40  04050 152123
41  04051 000000
42
43  04052 040504  MOD4M:   .TXTE !DATA PATH TEST (SECTOR)!
44  04053 040724
45  04054 050240
46  04055 152101
47  04056 120110
48  04057 142724
49  04060 152123
50  04061 024240
51  04062 142523
52  04063 152303
53  04064 151317
54  04065 000251
55
56  04066 040504  MOD5M:   .TXTE !DATA PATH TEST (SUB-SECTOR)!
57  04067 040724
58  04070 050240
```

```
 1  04071 152101
 2  04072 120110
 3  04073 142724
 4  04074 152123
 5  04075 024240
 6  04076 052523
 7  04077 026502
 8  04100 142523
 9  04101 152303
10  04102 151317
11  04103 000251
12
13  04104 147714  TNOM:   .TXTE !LOOP ON RNT # !
14  04105 050317
15  04106 147640
16  04107 120116
17  04110 047322
18  04111 120324
19  04112 120243
20  04113 000000
21
22  04114 047305  EPSM:   .TXTE !END OF CYCLE !
23  04115 120104
24  04116 143317
25  04117 141640
26  04120 141531
27  04121 142714
28  04122 000240
29
30  04123 147523  TMSG:   .TXTE !SOFTWARE TIMEOUT !
31  04124 152306
32  04125 040727
33  04126 142722
34  04127 152240
35  04130 046711
36  04131 147705
37  04132 152125
38  04133 000240
39
40
41  04134 024166  EDIAG:  LDA     1,MODE
42  04135 101000  EOC2:   MOV     0,0       ;ITERATE TEST.
43  04136 030156          LDA     2,MODAL   ;ALL MODE SWITCHES
44  04137 074477          READS   3         ;READ THE DATA SWITHCES
45  04140 173400          AND     3,2       ;SEE WHICH RE SET
46  04141 151320          MOVZS   2,2       ; SWAP BYTES
47  04142 151220          MOVZR   2,2       ; SHIFT BITS TO LOW ORDER
48  04143 024224  EOC4:   LDA     1,IIMOD   ; ADDRESS OF MODE TABLE
49  04144 133000          ADD     1,2       ; FORM POINTER INTO TABLE
50  04145 003000          JMP     @0,2      ; JUMP TO CURRENT MODE
51
52  04146 004156  IMODE:  MODE0             ; TESTS 1 THRU 4
53  04147 000430          MODE1             ; TEST 1
54  04150 001303          MODE2             ; TEST 2
55  04151 001471          MODE3             ; TEST 3
56  04152 002014          MODE4             ; TEST 4
57  04153 002321          MODE5             ; TEST 5
58  04154 004167          MODE6             ; TESTS 1, 2 AND 4
```

```
 1   04155 004206           MODE7            ; TESTS 2 AND 4
 2                    ;
 3                    ;
 4   04156 010166   MODE0:  ISZ      MODE     ; INCREMENT MODE
 5   04157 030166           LDA      2,MODE   ; GET THE MODE
 6   04160 024112           LDA      1,C5     ; MAX TEST NO.
 7   04161 132432           SUBZ#    1,2,SZC  ; SEE IF GREATER THAN MAX
 8   04162 000402           JMP      EPMS     ; YES  END OF PASS
 9   04163 000760           JMP      EOC4
10                    ;
11   04164 152400   EPMS:   SUB      2,2      ; GET A ZERO
12   04165 050166           STA      2,MODE   ; SET MODE
13   04166 000755           JMP      EOC4     ;
14                    ;
15   04167 030166   MODE6:  LDA      2,MODE   ; GET CURRENT MODE
16   04170 020110           LDA      0,C1     ; GET A ONE
17   04171 024111           LDA      1,C2     ; GET A TWO
18   04172 034100           LDA      3,C4     ; GET A FOUR
19   04173 112415           SUB#     0,2,SNR  ; SEE IF CURRENTLY 1
20   04174 000405           JMP      M6A      ; YES
21   04175 132415           SUB#     1,2,SNR  ; SEE IF CURRENTLY 2
22   04176 000406           JMP      M6B      ; YES
23   04177 111000           MOV      0,2      ; OTHERWISE MUST BE FOUR
24   04200 000402           JMP      M6C      ; SET TO 1
25                    ;
26   04201 151400   M6A:    INC      2,2      ; FORM A TWO
27   04202 050166   M6C:    STA      2,MODE   ; SET NEXT MODE
28   04203 000740           JMP      EOC4     ; GO TO NEXT TEST
29                    ;
30   04204 133000   M6B:    ADD      1,2      ; FORM A FOUR
31   04205 000775           JMP      M6C
32                    ;
33   04206 030166   MODE7:  LDA      2,MODE   ; GET THE CURRENT MODE
34   04207 024111           LDA      1,C2     ; GET A TWO
35   04210 132415           SUB#     1,2,SNR  ; SEE IF CURRENLY 2
36   04211 000403           JMP      M7A
37   04212 030111           LDA      2,C2     ; GET A TWO
38   04213 000767           JMP      M6C      ; GO TO TEST
39   04214 030100   M7A:    LDA      2,C4     ; GET A FOUR
40   04215 000765           JMP      M6C      ; GO TO TEST
41
42   04216 054054   DCODE:  STA      3,DRET   ;SET THE I/O INST
43   04217 062677           IORST             ;DEVICE CODES.
44   04220 006064           JSR      @ICRLF
45   04221 006065           JSR      @IMESS
46   04222 003761           DEVNUM
47   04223 030107           LDA      2,C2000
48
49   04224 004450   SHFL:   JSR      TIN      ;TYPE INPUT
50   04225 034121           LDA      3,C70
51   04226 116032           ADCZ#    0,3,SZC
52   04227 034122           LDA      3,CM60
53   04230 117046           ADDO     0,3,SEZ
54   04231 000767           JMP      DCODE+2  ;NOT A DIGIT
55   04232 151120           MOVZL    2,2
56   04233 153120           ADDZL    2,2
57   04234 173003           ADD      3,2,SNC  ;ASSEMBLE 2 DIGITS
58   04235 000767           JMP      SHFL
```

```
 1  04236 024120           LDA     1,C20
 2  04237 020123           LDA     0,C60
 3  04240 146414           SUB#    2,1,SZR
 4  04241 142415           SUB#    2,0,SNR
 5  04242 101011           MOV#    0,0,SKP
 6  04243 000755           JMP     DCODE+2
 7  04244 050055           STA     2,DEVICE
 8
 9  04245 030062  DEVCD:    LDA     2,FIRST ;MODIFY I/O INST
10  04246 021000           LDA     0,0,2   ;BETWEEN FIRST
11  04247 024124           LDA     1,C1600         ;AND LAST.
12  04250 123400           AND     1,0
13  04251 024125           LDA     1,C0600
14  04252 106414           SUB#    0,1,SZR
15  04253 000414           JMP     DEV1    ;NOT I/O
16  04254 021000           LDA     0,0,2
17  04255 024126           LDA     1,C77
18  04256 123400           AND     1,0
19  04257 106415           SUB#    0,1,SNR
20  04260 000407           JMP     DEV1    ;CPU INST
21  04261 021000           LDA     0,0,2
22  04262 024127           LDA     1,C1777700
23  04263 123400           AND     1,0
24  04264 024055           LDA     1,DEVICE
25  04265 123000           ADD     1,0
26  04266 041000           STA     0,0,2
27
28  04267 151400  DEV1:     INC     2,2
29  04270 020063           LDA     0,LAST
30  04271 112414           SUB#    0,2,SZR
31  04272 000754           JMP     DEVCD+1
32  04273 002054           JMP     @DRET
33
34  04274 054051  TIN:      STA     3,TINRET;TYPE INPUT
35  04275 063610           SKPDN   TTI
36  04276 000777           JMP     .-1
37  04277 063511           SKPBZ   TTO
38  04300 000777           JMP     .-1
39  04301 060610           DIAC    0,TTI
40  04302 061111           DOAS    0,TTO
41  04303 034132           LDA     3,C177
42  04304 163400           AND     3,0
43  04305 063511           SKPBZ   TTO
44  04306 000777           JMP     .-1
45  04307 002051           JMP     @TINRET
46                ;
47                ;
48                ;       ROUTINE TO READ SOME DIGITS FORM TELETYPE
49                ;
50                ;
51  04310 054422  T4IN:     STA     3,TRET  ; SAVE RETURN ADDRESS
52  04311 062677           IORST           ; RESET THE WORLD
53  04312 004762  SH4FL:    JSR     TIN     ; GET A CHARACTER
54  04313 034121           LDA     3,C70   ; MASK
55  04314 116032           ADCZ#   0,3,SZC ; ???
56  04315 034122           LDA     3,CM60  ;
57  04316 117046           ADDO    0,3,SEZ ; ???
58  04317 000407           JMP     T4IM    ; NOT A DIGIT
```

```
 1   04320 151120           MOVZL   2,2
 2   04321 153120           ADDZL   2,2       ; SHIFT
 3   04322 173003           ADD     3,2,SNC   ; ASSEMBLE DIGIT
 4   04323 000767           JMP     SH4FL     ; GET NEXT DIGIT
 5                  ;
 6   04324 010406 T4OUT:    ISZ     TRET      ; FORM NO ERROR RETURN ADDRESS
 7   04325 002405           JMP     @TRET     ; RETURN
 8                  ;
 9   04326 034405 T4IM:     LDA     3,CR      ; CARRIAGE RETURN CHARACTER
10   04327 116404           SUB     0,3,SZR   ; SEE IF LAST CHAR A CR
11   04330 002402           JMP     @TRET     ; NO  MUST BE ERROR
12   04331 000773           JMP     T4OUT     ; OTHERWISE NORMAL EXIT
13                  ;
14   04332 000000 TRET:     0
15   04333 000015 CR:       15
```

```
 1
 2                          ;
 3                          ;
 4                          ;
 5                          ;       ROUTINE TO PRINT STATUS ERROR
 6                          ;
 7  04334 054310  STAER:    STA     3,STARS ; SAVE RETURN REGISTER
 8  04335 044526            STA     1,SAVE1 ; SAVE AC 1
 9  04336 050526            STA     2,SAVE2 ; SAVE AC 2
10  04337 074477            READS   3       ; READ DATA SWITCHES
11  04340 030147            LDA     2,STERIN ; STATUS ERROR PRINT INHIBIT BIT
12  04341 173404            AND     3,2,SZR ; MASK THE SWITCHES
13  04342 000516            JMP     SRTN    ; NO PRINT SO RETURN
14                          ;
15  04343 006064            JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
16  04344 006065            JSR     @IMESS  ; MESSAGE
17  04345 004467            STERM
18                          ;
19  04346 020306            LDA     0,RWFLG ; GET THE READ/WRITE FLAG
20  04347 101005            MOV     0,0,SNR ; SEE IF SET
21  04350 000404            JMP     PWT     ; NO INDICATES WRITE
22                          ;
23  04351 006065            JSR     @IMESS  ; PRINT MESSAGE
24  04352 004472            SRDM            ; RD
25                          ;
26  04353 000403            JMP     STER2
27                          ;
28  04354 006065  PWT:      JSR     @IMESS  ; MESSAGE
29  04355 004475            SWTM            ; WT
30                          ;
31  04356 030123  STER2:    LDA     2,C60   ; GET AN ASCII 0
32  04357 020204            LDA     0,STERS ; GET THE STATUS
33  04360 024505            LDA     1,STMK1 ; FIRST CHARACTER MASK
34  04361 123620            ANDZR   1,0     ; MASK TO STATUS
35  04362 101220            MOVZR   0,0     ; SHIFT
36  04363 101220            MOVZR   0,0     ; SHIFT TO LOW ORDER
37  04364 143000            ADD     2,0     ; FORM ASCII CHARACTER
38  04365 006210            JSR     @ICHAR  ; PRINT THE CHARACTER
39  04366 020204            LDA     0,STERS ; RELOAD STATUS
40  04367 024477            LDA     1,STMK2 ; MASK FOR SECOND CHARACTER
41  04370 123400            AND     1,0     ; ISOLATE 2ND CHARACTER BITS
42  04371 143000            ADD     2,0     ; FORM ASCII CHARACTER
43  04372 006210            JSR     @ICHAR  ; PRINT THE CHARACTER
44                          ;
45                          ;       PRINT DISC NO.
46                          ;
47  04373 020273  STP:      LDA     0,CBLK  ; ASCII BLANK
48  04374 006210            JSR     @ICHAR  ; PRINT IT
49  04375 030123            LDA     2,C60   ; ASCII 0
50  04376 020205            LDA     0,STTS  ; GET SAVE T/S
51  04377 024265            LDA     1,DMSK  ; MASK TO DISC NO. BITS
52  04400 123700            ANDS    1,0     ; MASK IT
53  04401 101220            MOVZR   0,0     ; SHIFT
54  04402 101220            MOVZR   0,0     ; SHIFT
55  04403 101220            MOVZR   0,0     ; SHIFT
56  04404 101220            MOVZR   0,0     ; SHIFT
57  04405 143000            ADD     2,0     ; FORM ASCII
58  04406 006210            JSR     @ICHAR  ; PRINT IT
```

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 1   04407 020273           LDA     0,CBLK  ; ASCII BLANK
 2   04410 006210           JSR     @ICHAR  ; PRINT IT
 3                  ;
 4                  ;       PRINT TRACK
 5                  ;
 6   04411 020205           LDA     0,STTS  ; GET THE SAVE T/S
 7   04412 024266           LDA     1,TMSK1 ; MASK TO HI CHAACTER
 8   04413 123700           ANDS    1,0     ; AND IT TO MASK
 9   04414 101220           MOVZR   0,0     ; SHIFT IT
10   04415 101220           MOVZR   0,0     ; SHIFT
11   04416 101220           MOVZR   0,0     ; SHIFT
12   04417 143000           ADD     2,0     ; FORM ASCII
13   04420 006210           JSR     @ICHAR  ; PRINT IT
14                 ;
15   04421 020205           LDA     0,STTS  ; GET THE SAVE T/S
16   04422 024267           LDA     1,TMSK2 ; MASK FOR SECOND CHARACTER
17   04423 123700           ANDS    1,0     ; MASK
18   04424 143000           ADD     2,0     ; FORM ASCII
19   04425 006210           JSR     @ICHAR  ; PRINT IT
20                 ;
21   04426 020205           LDA     0,STTS  ; GET THE SAVE T/S
22   04427 024270           LDA     1,TMSK3 ; MASK TO LO CHARACTER
23   04430 123620           ANDZR   1,0     ; MASK
24   04431 101220           MOVZR   0,0     ; SHIFT
25   04432 101220           MOVZR   0,0     ; SHIFT
26   04433 101220           MOVZR   0,0     ; SHIFT
27   04434 101220           MOVZR   0,0     ; SHIFT
28   04435 143000           ADD     2,0     ; FORM ASCII
29   04436 006210           JSR     @ICHAR  ; PRINT IT
30   04437 020273           LDA     0,CBLK  ; ASCII BLANK
31   04440 006210           JSR     @ICHAR  ; PRINT IT
32                 ;
33                 ;       PRINT SECTOR
34                 ;
35   04441 020205           LDA     0,STTS  ; GET SAVE T/S
36   04442 024271           LDA     1,SMSK1 ; SECTOR MASK
37   04443 123620           ANDZR   1,0     ; MASK
38   04444 101220           MOVZR   0,0     ; SHIFT
39   04445 101220           MOVZR   0,0     ; SHIFT
40   04446 143000           ADD     2,0     ; FORM ASCII
41   04447 006210           JSR     @ICHAR  ; PRINT IT
42                 ;
43   04450 020205           LDA     0,STTS  ; GET SAVED T/S
44   04451 024272           LDA     1,SMSK2 ; SECTOR MASK
45   04452 123400           AND     1,0     ; MASK
46   04453 143000           ADD     2,0     : FORM ASCII
47   04454 006210           JSR     @ICHAR  ; PRINT IT
48   04455 020273           LDA     0,CBLK  ; ASCII BLANK
49   04456 006210           JSR     @ICHAR  ; PRINT IT
50                 ;
51   04457 006243           JSR     @IPCNT  ; PRINT CYCLE COUNT
52                 ;
53   04460 024403  SRTN:    LDA     1,SAVE1 ; RESTORE AC 1
54   04461 030403           LDA     2,SAVE2 ; RESTORE 2
55   04462 002310           JMP     @STARS  ; RETURN
56                 ;
57   04463 000000  SAVE1:   0
58   04464 000000  SAVE2:   0
```

```
PAGE  53
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 1   04465 000070  STMK1:   70
 2   04466 000007  STMK2:   7
 3                 ;
 4   04467 152123  STERM:   .TXTE !STER !
 5   04470 151305
 6   04471 000240
 7
 8   04472 151240  SRDM:    .TXTE ! RD  !
 9   04473 120104
10   04474 000240
11
12   04475 153640  SWTM:    .TXTE ! WT  !
13   04476 120324
14   04477 000240
15
16                 ;
17   04500 054430  ENTER:   STA     3,LOOPR ;LOOP ITERATE RETURN
18   04501 074477           READS   3       ; READ THE DATA SWITCHES
19   04502 030135           LDA     2,PRINS ; TEST ABORT SWITCH
20   04503 173404           AND     3,2,SZR ; MASK SWITCHES
21   04504 002214           JMP     @ISTRT  ; ABORT
22   04505 030137           LDA     2,LPERS ; PRINT CYCLE COUNT
23   04506 173404           AND     3,2,SZR ; SEE IF SET
24   04507 006244           JSR     @IPCT2  ; PRINT CYCLE COUNT
25   04510 034410           LDA     3,ITR   ;THIS ROUTINE INITALIZES
26   04511 054410           STA     3,ITRCT ;EACH TEST
27   04512 010165           ISZ     ERNO    ;INCREMENT ERROR NUMBER
28   04513 176400           SUB     3,3
29   04514 054406           STA     3,ESWIT
30   04515 054406           STA     3,ERRCT
31   04516 062677           IORST           ;I/O RESET
32   04517 002411           JMP     @LOOPR
33
34   04520 000144  ITR:     144
35   04521 000000  ITRCT:   0
36   04522 000000  ESWIT:   0
37   04523 000000  ERRCT:   0
38   04524 000000  RETURN:  0
39   04525 000000  SAV2:    0
40   04526 000000  SAV1:    0
41   04527 000000  SAV0:    0
42   04530 000000  LOOPR:   0
43
44   04531 054773  CYCLE:   STA     3,RETURN;END OF TEST ITERATION
45   04532 050773           STA     2,SAV2  ;ROUTINE
46   04533 074477           READS   3
47   04534 062677           IORST           ;I/O RESET
48   04535 030135           LDA     2,PRINS ; ABORT SET ?
49   04536 173404           AND     3,2,SZR ; MASK SWITCHES
50   04537 002214           JMP     @ISTRT
51   04540 030140           LDA     2,LPTST ; SEE IF LOOP ON TEST
52   04541 173404           AND     3,2,SZR ; MASK SWITCHES
53   04542 002766           JMP     @LOOPR  ;(1)*LOOP ROUTINE
54   04543 002761           JMP     @RETURN ;(0)*PROCEED TO NEXT TEST
55
56   04544 054760  ERR:     STA     3,RETURN          ;ERROR SUBROUTINE
57   04545 050760           STA     2,SAV2
58   04546 044760           STA     1,SAV1
```

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 1  04547 040760           STA     0,SAV0
 2  04550 000407           JMP     ERR1
 3  04551 030754 ERET:     LDA     2,SAV2  ;RESTORE ACS
 4  04552 024754           LDA     1,SAV1
 5  04553 020754           LDA     0,SAV0
 6  04554 010747 ERHRT:    ISZ     ERRCT   ;COUNT
 7  04555 101000           MOV     0,0     ;ERRORS. I/O RESET
 8  04556 002746           JMP     @RETURN ;EXIT
 9
10  04557 034745 ERR1:     LDA     3,RETURN;ERROR. C(3)=PC
11  04560 054742           STA     3,ESWIT
12  04561 074477           READS   3
13  04562 030146           LDA     2,DERIN ; PRINT INHIBIT BIT
14  04563 173405           AND     3,2,SNR ; MASK
15  04564 004406           JSR     EPRINT  ; PRINT THE ERROR
16  04565 074477           READS   3
17  04566 030136           LDA     2,ERHLTS ; HALT ON ERROR BIT
18  04567 173404           AND     3,2,SZR  ; MASK SWITCHES
19  04570 000411           JMP     ERR3
20  04571 000760           JMP     ERET
21
22  04572 054730 EPRINT:   STA     3,ESWIT ;ERROR MESSAGE PRINTER
23  04573 006064           JSR     @ICRLF  ;PRINT CARRIAGE
24  04574 006065           JSR     @IMESS  ;AND HEADER
25  04575 004606           HEADER
26  04576 024165           LDA     1,ERNO
27  04577 006207           JSR     @IPOCT  ;NO.OF ERROR
28  04600 002722           JMP     @ESWIT  ;RETURN TO CALL
29                     ;
30  04601 020726 ERR3:     LDA     0,SAV0  ; RESTORE AC 0
31  04602 024724           LDA     1,SAV1  ; RESTORE AC 1
32  04603 030722           LDA     2,SAV2  ;  RESTORE AC 2
33  04604 063077           HALT
34  04605 000747           JMP     ERHRT   ; RETURN
35                     ;
36  04606 151305 HEADER:   .TXTE   !ER* !
37  04607 120243
38  04610 000000
39
```

```
 1
 2                      ;
 3                      ; ROUTINE TO GENERATE DATA PATTERN
 4                      ; CALLING SEQUENCE:
 5                      ;       JSR     @IPATRN
 6                      ;       DC      NUMBER OF WORDS
 7                      ;       DC      ADDRESS OF BUFFER
 8                      ;       DC      CURRENT TRACK/SECTOR ADDRESS
 9                      ;       DC      FIRST/SECOND READ FLAG
10                      ;
11                      ; EXAMINE DATA SWITCHES 13,14,15 TO DETERMINE THE PATTERN.
12                      ; PATTERNS ARE:
13                      ;       13, 14, 15
14                      ;        0   0   0      ALL PATTENS
15                      ;        0   0   1      RANDOM
16                      ;        0   1   0      INCREMENTING
17                      ;        0   1   1      TRACK/SECTOR ID
18                      ;        1   0   0      WORST CASE
19                      ;        1   0   1      ONES
20                      ;        1   1   0      ZEROES
21                      ;        1   1   1      SELECTABLE
22                      ;
23  04611 054552  PATRN:  STA     3,PRTN  ;SAVE RETURN
24  04612 034261          LDA     3,SWFLG ; SEE IF PATTERN CHANGE IS INHIBITED
25  04613 175004          MOV     3,3,SZR
26  04614 000407          JMP     PCUR    ; YES
27                      ;
28  04615 074477          READS   3       ;GET DATA SWITCHES
29  04616 030155          LDA     2,DPALL
30  04617 173400          AND     3,2     ;MASK DP SWITCHES
31  04620 024223  PAT4:   LDA     1,IPTBL ; ADDRESS OF PATTERN HANDLERS TABLE
32  04621 133000          ADD     1,2     ; ADD TO SWITCHES
33  04622 003000          JMP     @0,2    ; JUMP
34                      ;
35                      ;
36  04623 030215  PCUR:   LDA     2,CURPT ; GET CURRENT PATTERN CODE
37  04624 000774          JMP     PAT4    ; USE IT
38                      ;
39                      ;
40  04625 004635  PATBL:  ALPAT
41  04626 004707          RANPAT
42  04627 004670          INCPAT
43  04630 004735          IDPAT
44  04631 004731          WCPAT
45  04632 004650          ONEPAT
46  04633 004664          ZERPAT
47  04634 004744          SLPAT
48                      ;
49                      ;
50  04635 020233  ALPAT:  LDA     0,PATE  ; GET PATTERN PER SECTOR FLAG
51  04636 101004          MOV     0,0,SZR ; SEE IF SET
52  04637 000405          JMP     ALP2    ; IF SET  REPEAT PATTERN
53  04640 014215          DSZ     CURPT   ;DECREMEN CURRENT PATTERNS
54  04641 000403          JMP     ALP2
55  04642 020113          LDA     0,C6    ;GET A SIX
56  04643 040215          STA     0,CURPT
57  04644 030215  ALP2:   LDA     2,CURPT
58  04645 024223          LDA     1,IPTBL ; ADDRESS OF PATTERN HANLERS TABLE
```

```
 1  04646 133000           ADD     1,2      ; ADD TO SWITCH SETTING
 2  04647 003000           JMP     @0,2
 3                ;
 4  04650 020112  ONEPAT:  LDA     0,C5     ; GET A ONE
 5  04651 040215           STA     0,CURPT  ; SET CURRENT PATTERN
 6  04652 020134           LDA     0,M1     ;GET A ONE
 7  04653 034510  PAT1:    LDA     3,PRTN
 8  04654 025400           LDA     1,0,3    ; GET THE NUMBER OF WORDS
 9  04655 044505           STA     1,CNTR   ; SAVE IT
10  04656 031401           LDA     2,1,3    ; GET THE BUFFER ADDRESS
11  04657 041000  PAT2:    STA     0,0,2    ; STORE IN BUFFER
12  04660 151400           INC     2,2      ; INCREMENT BUFFER POINTER
13  04661 014501           DSZ     CNTR     ; DECREMENT COUNTR
14  04662 000775           JMP     PAT2     ;
15  04663 001403           JMP     3,3      ; RETURN
16                ;
17  04664 020113  ZERPAT:  LDA     0,C6     ; GET A TWO
18  04665 040215           STA     0,CURPT  ; SET CURRENT PATTERN
19  04666 102400           SUB     0,0      ; GET A ZERO
20  04667 000764           JMP     PAT1     ; STORE IN BUFFER
21                ;
22  04670 020111  INCPAT:  LDA     0,C2     ; GET A THREE
23  04671 040215           STA     0,CURPT  ; SET CURRENT PATTERN
24  04672 040233           STA     0,PATE   ; SET PATTERN PER TRACK
25  04673 020246           LDA     0,INCE   ; START W ZERO
26  04674 034467           LDA     3,PRTN
27  04675 025400           LDA     1,0,3    ; GET # OF WORDS
28  04676 031401           LDA     2,1,3    ; GET BUFFER ADDRESS
29  04677 044463           STA     1,CNTR   ; SET THE COUNTER
30                ;
31  04700 041000  INC2:    STA     0,0,2    ; STORE PATTERN
32  04701 101400           INC     0,0      ; INCREMEN PATTERN
33  04702 151400           INC     2,2      ; INCREMEN STORE POINTER
34  04703 014457           DSZ     CNTR     ; DECREMEN COUNTER
35  04704 000774           JMP     INC2
36  04705 040246           STA     0,INCE   ; SAVE LAST PATTERN
37  04706 001403           JMP     3,3      ; RETURN
38                ;
39  04707 020110  RANPAT:  LDA     0,C1     ; GET A FOUR
40  04710 040215           STA     0,CURPT  ; SET CURRENT PATTERN
41  04711 040233           STA     0,PATE   ; SET PATTERN PER TRACK
42  04712 034451           LDA     3,PRTN
43  04713 025400           LDA     1,0,3    ; GET # OF WORDS
44  04714 031401           LDA     2,1,3    ; GET BUFFER ADDRESS
45  04715 044445           STA     1,CNTR   ; SET COUNTER
46  04716 010217           ISZ     CSEED    ; INCREMENT CURRENT SEED
47  04717 000401           JMP     .+1
48  04720 020217           LDA     0,CSEED  ; GET CURRENT SEED
49                ;
50  04721 105120  RANP2:   MOVZL   0,1      ; MANIPULATE SEED
51  04722 127120           ADDZL   1,1
52  04723 123120           ADDZL   1,0
53  04724 041000           STA     0,0,2    ; STORE PATTERN
54  04725 151400           INC     2,2      ; INCREMENT BUFFER POINTER
55  04726 014434           DSZ     CNTR     ; DECREMENT COUNTER
56  04727 000772           JMP     RANP2
57  04730 001403           JMP     3,3      ; RETURN
58                ;
```

```
 1  04731 020100  WCPAT:  LDA     0,C4     ; GET A FIVE
 2  04732 040215         STA     0,CURPT  ; SET CURRENT PATTERN
 3  04733 020431         LDA     0,WCPT   ; GET WC PATTERN
 4  04734 000717         JMP     PAT1
 5                 ;
 6  04735 020116  IDPAT:  LDA     0,C3     ; GET A SIX
 7  04736 040215         STA     0,CURPT  ; SET CURRENT PATTERN
 8  04737 034424         LDA     3,PRTN   ; GET POINTER
 9  04740 021402         LDA     0,2,3    ; GET CURRENT TRACK/SECTOR
10  04741 024110         LDA     1,C1     ; GET A ONE
11  04742 044233         STA     1,PATE   ; SET PATTERN PER SECTOR SWITCH
12  04743 000710         JMP     PAT1
13                ;
14  04744 020114  SLPAT:  LDA     0,C7     ; GET A SEVEN
15  04745 040215         STA     0,CURPT  ; SET CURRENT PATTERN
16  04746 020250         LDA     0,SELPT  ; SEE IF PATTERN SELECTED
17  04747 101004         MOV     0,0,SZR  ;
18  04750 000703         JMP     PAT1
19  04751 006064         JSR     @ICRLF   ; CARRIAGE RETURN LINE FEED
20  04752 006065         JSR     @IMESS   ; MESSAGE
21  04753 004765         SLPM
22  04754 152400         SUB     2,2      ; GET SOME CHARACTERS
23  04755 006220         JSR     @IT4IN   ; READ THE TTY
24  04756 000766         JMP     SLPAT    ; ERROR
25  04757 050250         STA     2,SELPT  ; SAVE THE PATTERN
26  04760 141000         MOV     2,0      ;
27  04761 000672         JMP     PAT1
28                ;
29                ;
30  04762 000000  CNTR:   0
31  04763 000000  PRTN:   0
32  04764 016142  WCPT:   16142
33  04765 040520  SLPM:   .TXTE   !PATTERN ? !
34  04766 152324
35  04767 151305
36  04770 120116
37  04771 120077
38  04772 000000
```

```
                        ;
                        ;
                        ;       ROUTINE TO COMPARE DATA PATTERN
                        ;
                        ;       CALLING SEQUENCE:
                        ;
                        ;       JSR     @ICOMP
                        ;       DC      NUMBER OF WORDS
                        ;       DC      OBUF            WRITE BUFFER ADDRESS
                        ;       DC      IBUF            READ BUFFER ADDRESS
                        ;       DC      TRACK/SECTOR    CURRENT TRACK/SECTOR
                        ;       DC      FIRST/SECOND    0 => FIRST READ, 1 => SECOND READ
                        ;
                        ;
04773 054303  COMP:     STA     3,CRTN  ; SAVE RETURN REGISTER
04774 020377            LDA     0,ERC5  ; CONSEQUTIVE ERROR COUNTER
04775 040307            STA     0,ERCN  ; SET COUNTER
04776 020233            LDA     0,PATE  ; GET THE PATTERN PER SECTOR SWITCH
04777 101005            MOV     0,0,SNR ; SEE IF SET
05000 000414            JMP     COMB    ; NO
                        ;
05001 021400            LDA     0,0,3   ; GET NUMBER OF WORDS
05002 040406            STA     0,NWC   ; SET AS CALLING SEQUENCE
05003 021401            LDA     0,1,3   ; GET THE BUFFER ADDRESS
05004 040405            STA     0,BAC   ; SET IN CALLING SEQUENCE
05005 021403            LDA     0,3,3   ; GET THE SECTOR ADDRESS
05006 040404            STA     0,TAC   ; SET IN CALLING SEQUENCE
                        ;
05007 006213            JSR     @IPTRN  ; GENERATE THE PATTERN
05010 000000  NWC:      0               ; WORD COUNT
05011 000000  BAC:      0               ; BUFFER ADDRESS
05012 000000  TAC:      0               ; SECTOR ADDRESS
                        ;
05013 034303            LDA     3,CRTN
05014 102400  COMB:     SUB     0,0     ; FORM A ZERO
05015 040304            STA     0,POSS  ; INITIALIZE POSITION
05016 101400            INC     0,0     ;
05017 031401            LDA     2,1,3   ; GET THE WRITE BUFFER ADDRESS
05020 112400            SUB     0,2     ; DECREMENT
05021 050020            STA     2,20    ; SET AUTO INDEX REGISTER
05022 031402            LDA     2,2,3   ; GET THE READ BUFFER ADDRESS
05023 112400            SUB     0,2     ; DECREMENT
05024 050021            STA     2,21    ; SET AUTO INDEX REGISTER
05025 031400            LDA     2,0,3   ; GET THE NUMBER OF WORDS
05026 050305            STA     2,CCNTR ; SET THE COUNTER
                        ;
05027 022020  CLOP:     LDA     0,@20   ; GET A WORD FROM WRITE BUFFER
05030 026021            LDA     1,@21   ; GET A WORD FROM READ BUFFER
05031 131000            MOV     1,2     ; SAVE
05032 106400            SUB     0,1     ; COMPARE THE WORDS
05033 125004            MOV     1,1,SZR ; SAME ?
05034 000410            JMP     CERR    ; NO
05035 034377            LDA     3,ERC5  ; CONSEQUTIVE ERROR COUNT
05036 054307            STA     3,ERCN  ; SET COUNTER
05037 010304  CONW:     ISZ     POSS    ; INCREMENT POSITION
05040 014305            DSZ     CCNTR   ; OTHERWISE DECREMENT COUNTER
05041 000766            JMP     CLOP    ; GET THE NEXT WORD
```

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 1   05042 034303           LDA     3,CRTN  ; GET RETURN ADDRESS
 2   05043 001405           JMP     5,3     ; RETURN
 3                  ;
 4                  ;
 5   05044 030146   CERR:   LDA     2,DERIN ; DATA ERROR PRINT INHIBIT BIT
 6   05045 074477           READS   3       ; READ THE DATA SWITCHES
 7   05046 173404           AND     3,2,SZR ; MASK THE BITS
 8   05047 000770           JMP     CONW    ; IF SET NO PRINT
 9   05050 030135           LDA     2,PRINS ; SEE IF ABORT SET
10   05051 173404           AND     3,2,SZR ;
11   05052 002214           JMP     @ISTRT  ; YES ABORT
12   05053 014307           DSZ     ERCN    ; DECREMENT CONSEQ. ERROR COUNT
13   05054 000402           JMP     .+2     ; PRINT ERROR
14   05055 000762           JMP     CONW    ; DONT PRINT ERROR
15   05056 006064           JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
16   05057 034303           LDA     3,CRTN  ; GET POINTER
17   05060 021404           LDA     0,4,3   ; FIRST/SECOND FLAG
18   05061 024123           LDA     1,C60   ; ASCII ZERO
19   05062 125400           INC     1,1     ;
20   05063 123000           ADD     1,0     ; FORM ASCII CHARACTER
21   05064 006210           JSR     @ICHAR  ; PRINT THE FLAG
22   05065 006065           JSR     @IMESS  ; MESSAGE
23   05066 005254           CERM
24                  ;
25   05067 030021           LDA     2,21    ;GET THE BUFFER POINTER
26   05070 025000           LDA     1,0,2   ; GET WORD FORM BUFFER
27   05071 050021           STA     2,21    ; RESET INDEX
28   05072 006207           JSR     @IPOCT  ; PRINT THE WORD
29   05073 006065           JSR     @IMESS  ; MESSAGE
30   05074 005264           EXPM
31   05075 030020           LDA     2,20    ; WRITE BUFFER POINTER
32   05076 025000           LDA     1,0,2   ; GET WORD FROM BUFFER
33   05077 050020           STA     2,20    ; RESET INDEX
34   05100 006207           JSR     @IPOCT  ; PRINT THE WORD
35   05101 006065           JSR     @IMESS  ; MESSAGE
36   05102 005257           ADRM
37                  ;
38                  ;       PRINT DISC
39                  ;
40   05103 030123           LDA     2,C60   ; GET ASCII ZERO
41   05104 034303           LDA     3,CRTN  ; POINTER
42   05105 021403           LDA     0,3,3   ; TRACK/SECTOR
43   05106 024265           LDA     1,DMSK  ; MASK TO DISC BITS
44   05107 123700           ANDS    1,0     ; MASK TO T/S
45   05110 101220           MOVZR   0,0     ; SHIFT BITS
46   05111 101220           MOVZR   0,0     ; SHIFT BITS
47   05112 101220           MOVZR   0,0     ; SHIFT BITS
48   05113 101220           MOVZR   0,0     ; SHIFT BITS
49   05114 143000           ADD     2,0     ; FORM ASCII
50   05115 006210           JSR     @ICHAR  ; PRINT DISC NO.
51   05116 020273           LDA     0,CBLK  ; A SPACE
52   05117 006210           JSR     @ICHAR  ; PRINT IT
53                  ;
54                  ;       PRINT TRACK
55                  ;
56   05120 034303           LDA     3,CRTN  ; GET PINTER
57   05121 021403           LDA     0,3,3   ; GET THE TRACK/SECTOR
58   05122 024266           LDA     1,TMSK1 ; MASK TO FIRST CHARACTER
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 1   05123 123700           ANDS    1,0     ; MSK ADDRESSS
 2   05124 101220           MOVZR   0,0     ; SHIFT
 3   05125 101220           MOVZR   0,0     ; SHIFT
 4   05126 101220           MOVZR   0,0     ; SHIFT
 5   05127 143000           ADD     2,0     ; FORM ASCII
 6   05130 006210           JSR     @ICHAR  ; PRINT FIRST CHARACTER
 7                    ;
 8   05131 034303           LDA     3,CRTN  ; RESTORE POINTER
 9   05132 021403           LDA     0,3,3   ; GET TRACK/SECTOR
10   05133 024267           LDA     1,TMSK2 ; MASK TO SECOND CHARACTER
11   05134 123700           ANDS    1,0     ; MASK TO ADDRESS
12   05135 143000           ADD     2,0     ; FORM ASCII
13   05136 006210           JSR     @ICHAR  ; PRINT SECOND CHARACTER
14                    ;
15   05137 034303           LDA     3,CRTN  ; RESTORE POINTER
16   05140 021403           LDA     0,3,3   ; GET TRACK/SECTOR
17   05141 024270           LDA     1,TMSK3 ; GET MASK
18   05142 123620           ANDZR   1,0     ; MASK TO ADDRESS
19   05143 101220           MOVZR   0,0     ; SHIFT
20   05144 101220           MOVZR   0,0     ; SHIFT
21   05145 101220           MOVZR   0,0     ; SHIFT
22   05146 101220           MOVZR   0,0     ; SHIFT
23   05147 143000           ADD     2,0     ; FORM ASCII
24   05150 006210           JSR     @ICHAR  ; PRINT THE THIRD CHARACTER
25   05151 020273           LDA     0,CBLK  ; SPACE
26   05152 006210           JSR     @ICHAR  ; PRINT IT
27                    ;
28                    ;      PRINT THE SECTOR
29                    ;
30   05153 034303           LDA     3,CRTN  ; RESTOR POINTER
31   05154 021403           LDA     0,3,3   ; GET TRACK/SECTOR
32   05155 024271           LDA     1,SMSK1 ; MASK
33   05156 123620           ANDZR   1,0     ; MASK TRACK ADDRESS
34   05157 101220           MOVZR   0,0     ; SHIFT
35   05160 101220           MOVZR   0,0     ; SHIFT
36   05161 143000           ADD     2,0     ; FORM ASCII
37   05162 006210           JSR     @ICHAR  ; PRINT THE CHARACTER
38                    ;
39   05163 034303           LDA     3,CRTN  ; RESTORE POINTER
40   05164 021403           LDA     0,3,3   ; GET THE TRACK/SECTOR ADDRESS
41   05165 024272           LDA     1,SMSK2 ; MASK TO SECOND CHARACTER
42   05166 123400           AND     1,0
43   05167 143000           ADD     2,0     ; FORM ASCII
44   05170 006210           JSR     @ICHAR  ; PRINT THE CHARACTER
45   05171 020273           LDA     0,CBLK  ; SPACE
46   05172 006210           JSR     @ICHAR  ; PRINT IT
47                    ;
48                    ;      PRINT THE POSITION IN BUFFER
49                    ;
50   05173 020304           LDA     0,POSS  ; GET THE POSITION
51   05174 024274           LDA     1,PMSK1 ; MASK TO FIRST CHARACTER
52   05175 123520           ANDZL   1,0     ; MASK
53   05176 101120           MOVZL   0,0     ; SHIFT
54   05177 101320           MOVZS   0,0     ; SHIFT
55   05200 143000           ADD     2,0     ; FORM ASCII
56   05201 006210           JSR     @ICHAR  ; PRINT THE FIRST CHARACTER
57                    ;
58   05202 020304           LDA     0,POSS  ; GET THE POSITION
```

```
 1   05203 024275           LDA     1,PMSK2 ; MASK TO SECOND CHARACTER
 2   05204 123620           ANDZR   1,0     ; MASK
 3   05205 101220           MOVZR   0,0     ; SHIFT
 4   05206 101220           MOVZR   0,0     ; SHIFT
 5   05207 143000           ADD     2,0     ; FORM ASCII
 6   05210 006210           JSR     @ICHAR  ; PRINT THE SECOND CHARACTER
 7                  ;
 8   05211 020304           LDA     0,POSS  ; GET THE POSITION
 9   05212 024276           LDA     1,PMSK3 ; MASK TO THIRD CHARACTER
10   05213 123400           AND     1,0
11   05214 143000           ADD     2,0     ; FORM ASCII
12   05215 006210           JSR     @ICHAR  ; PRINT THE CHARACTER
13   05216 020273           LDA     0,CBLK  ; SPACE
14   05217 006210           JSR     @ICHAR  ; PRINT IT
15                  ;
16                  ;
17                  ;       PRINT PATTERN
18                  ;
19   05220 020215           LDA     0,CURPT ; GET CURENT PATTERN CODE
20   05221 100400           NEG     0,0     ; NEG IT
21   05222 100000           COM     0,0     ; DECREMENT PATTERN CODE
22   05223 103120           ADDZL   0,0     ; MULTIPLY BY FOUR
23   05224 024247           LDA     1,IONE  ; ADDRESS OF TABLE
24   05225 123000           ADD     1,0     ; FORM ADDRESS OF MESSAGE
25   05226 040402           STA     0,MSAD  ; STORE MESSAGE POINTER
26   05227 006065           JSR     @IMESS  ; MESSAGE
27   05230 000000  MSAD:    0
28                  ;
29                  ;       PRINT CYCLE COUNT IF TEST 4
30                  ;
31   05231 020166           LDA     0,MODE  ; GET THE CURRENT MODE
32   05232 024100           LDA     1,C4    ; SEE IF TEST 4
33   05233 122405           SUB     1,0,SNR ;
34   05234 006243           JSR     @IPCNT  ; PRINT CYCLE COUNT
35                  ;
36   05235 074477           READS   3       ; READ THE DATA SWITCHES
37   05236 030136           LDA     2,ERHLTS ; HALT ON ERROR SET ?
38   05237 173405           AND     3,2,SNR ;
39   05240 002245           JMP     @ICONW
40                  ;
41   05241 034021           LDA     3,21    ; GET BUFFER POINTER
42   05242 021400           LDA     0,0,3   ; GET WORD FROM BUFFER FOR DISPLAY
43   05243 054021           STA     3,21    ; RESET INDEX
44   05244 034020           LDA     3,20    ; GET WRITE BUFFER POINTER
45   05245 025400           LDA     1,0,3   ; GET WORD FOR DISPLAY
46   05246 054020           STA     3,20    ; RESET INDEX
47   05247 030304           LDA     2,POSS  ; POSITION
48   05250 034303           LDA     3,CRTN  ; GET POINTER
49   05251 035403           LDA     3,3,3   ; TRACK/SECTOR FOR DISPLAY
50   05252 063077           HALT
51   05253 002245           JMP     @ICONW  ; CONTINUE
52                  ;
53                  ;
54   05254 151072  CERM:    .TXTE   !:RD- !
55   05255 026504
56   05256 000240
57
58   05257 040640  ADRM:    .TXTE   ! ADRS:  !
```

```
 1  05260 151104
 2  05261 035123
 3  05262 120240
 4  05263 000000
 5
 6  05264 153640  EXPM:   .TXTE   ! WT- !
 7  05265 026724
 8  05266 000240
 9
10                ;
11  05267 120240  ONEM:   .TXTE   !  RAN !
12  05270 040722
13  05271 120116
14  05272 000000
15
16  05273 120240  ZERM:   .TXTE   !  INC !
17  05274 047311
18  05275 120303
19  05276 000000
20
21  05277 120240  SECM:   .TXTE   !  SEC !
22  05300 142523
23  05301 120303
24  05302 000000
25
26  05303 120240  INCM:   .TXTE   !  WOR !
27  05304 147727
28  05305 120322
29  05306 000000
30
31  05307 120240  RANM:   .TXTE   !  ONE !
32  05310 047317
33  05311 120305
34  05312 000000
35
36  05313 120240  WORM:   .TXTE   !  ZER !
37  05314 142532
38  05315 120322
39  05316 000000
40
41  05317 120240  SELM:   .TXTE   !  SEL !
42  05320 142523
43  05321 120314
44  05322 000000
45
46                ;
47                ;
48  05323 054446  PCNT:   STA      3,PCRTN ; SAVE RETURN ADDRESS
49  05324 024242          LDA      1,T4CY  ; GET THE COUNT
50  05325 006206          JSR      @IPDEC  ; PRINT IT
51  05326 006065          JSR      @IMESS  ; MESSAGE
52  05327 005331          CYM
53  05330 002441          JMP      @PCRTN  ; RETURN
54                ;
55  05331 141640  CYM:    .TXTE   ! CY  !
56  05332 120131
57  05333 000240
58
```

```
 1                      ;
 2  05334 054436  PCT2:    STA     3,P2RTN ; SAVE RETURN
 3  05335 040436           STA     0,P0S
 4  05336 044436           STA     1,P1S
 5  05337 050436           STA     2,P2S
 6  05340 006064           JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
 7                      ;
 8  05341 020306           LDA     0,RWFLG ; GET THE READ/WRITE FLAG
 9  05342 101005           MOV     0,0,SNR ; 0 FOR WRITE
10  05343 000404           JMP     PWT2    ; WRITE MESSAGE
11  05344 006065           JSR     @IMESS  ; MESSAGE
12  05345 004472           SRDM
13  05346 000403           JMP     PCT3    ; CONTINUE
14                      ;
15  05347 006065  PWT2:    JSR     @IMESS  ; MESSAGE
16  05350 004475           SWTM
17                      ;
18  05351 020312  PCT3:    LDA     0,IPRT  ; CONTINUE ADDRESS
19  05352 040310           STA     0,STARS ; PRINT RETURN
20  05353 002311           JMP     @ISTP   ; PRINT ADDRESS
21                      ;
22                      ;       PRINT PATTERN
23                      ;
24  05354 020215  PRT:     LDA     0,CURPT ; GET CURENT PATTERN CODE
25  05355 100400           NEG     0,0     ; NEG IT
26  05356 100000           COM     0,0     ; DECREMENT PATTERN CODE
27  05357 103120           ADDZL   0,0     ; MULTIPLY BY FOUR
28  05360 024247           LDA     1,IONE  ; ADDRESS OF TABLE
29  05361 123000           ADD     1,0     ; FORM ADDRESS OF MESSAGE
30  05362 040402           STA     0,MSAD2 ; STORE MESSAGE POINTER
31  05363 006065           JSR     @IMESS  ; MESSAGE
32  05364 000000  MSAD2:   0
33  05365 020406           LDA     0,P0S
34  05366 024406           LDA     1,P1S
35  05367 030406           LDA     2,P2S
36  05370 002402           JMP     @P2RTN  ; RETURN
37                      ;
38  05371 000000  PCRTN:   0
39  05372 000000  P2RTN:   0
40  05373 000000  P0S:     0
41  05374 000000  P1S:     0
42  05375 000000  P2S:     0
43                      ;
44                      ;
45                      ;       ROUTINE TO PRINT INSTRUCTIONS
46                      ;
47  05376 054423  PINS:    STA     3,PIRTN ; SAVE RETURN ADDRESS
48  05377 126400           SUB     1,1     ; FORM A ZERO
49  05400 044231           STA     1,INPTR ; INITIALIZE TABLE POINTER
50  05401 006064  PINLP:   JSR     @ICRLF  ; CARRIAGE RETURN LINE FEED
51  05402 030135           LDA     2,PRINS ; GET THE ABORT BIT
52  05403 074477           READS   3       ; READ THE DATA SWITCHES
53  05404 173405           AND     3,2,SNR ; MASK SWITCHES
54  05405 002414           JMP     @PIRTN  ; RETURN
55  05406 024231           LDA     1,INPTR ; GET TABLE POINTER
56  05407 030230           LDA     2,IINTB ; ADDRESS OF TABLE
57  05410 133000           ADD     1,2     ; FORM POINTER INTO TABLE
58  05411 025000           LDA     1,0,2   ; GET CURRENT MESSAGE ADDRESS
```

```
 1  05412 135005           MOV     1,3,SNR ; ZERO IS END OF TABLE
 2  05413 002406           JMP     @PIRTN  ; RETURN
 3  05414 044402           STA     1,.+2   ; STORE AS CALL
 4  05415 006065           JSR     @IMESS  ; MESSAGE
 5  05416 000000           0
 6  05417 010231           ISZ     INPTR   ; INCREMENT TABLE POINTER
 7  05420 000761           JMP     PINLP
 8                  ;
 9  05421 000000   PIRTN:  0
10                  ;
11  05422 003121   INTB:   INST1
12  05423 003131           INST2
13  05424 003141           INST3
14  05425 003152           INST4
15  05426 003165           INST5
16  05427 003175           INST6
17  05430 003210           INST7
18  05431 003225           INST8
19  05432 003253           INST9
20  05433 003274           INSTA
21  05434 003316           INSTB
22  05435 003342           INSTC
23  05436 003370           INSTD
24  05437 003406           INSTE
25  05440 003422           INSTF
26  05441 003431           INSTG
27  05442 003440           INSTH
28  05443 003456           INSTI
29  05444 003476           INSTJ
30  05445 003515           INSTK
31  05446 003535           INSTL
32  05447 003555           INSTM
33  05450 003573           INSTN
34  05451 003606           INSTO
35  05452 003624           INSTP
36  05453 003644           INSTQ
37  05454 003661           INSTR
38  05455 003673           INSTS
39  05456 003706           INSTT
40  05457 000000           0       ; END OF TABLE
41                  ;
42                  ;
43                  ;
44                  ;       SOFTWARE TIMER ROUTINE
45                  ;
46                  ;
47  05460 014302   WLP:     DSZ     WCNTR   ; DECREMENT COUNTER
48  05461 001776           JMP     -2,3    ; RETURN IF NOT ZERO
49                  ;
50  05462 040417           STA     0,RSW0  ; SAVE 0
51  05463 044417           STA     1,RSW1  ; SAVE 1
52  05464 050417           STA     2,RSW2  ; SAVE 2
53  05465 054417           STA     3,WRTN  ; SAVE RETURN
54  05466 074477           READS   3
55  05467 030150           LDA     2,EOCIN ; SEE IF PRINT INHIBITED
56  05470 173404           AND     3,2,SZR
57  05471 000404           JMP     WLP2    ; YES
58                  ;
```

```
 1   05472 006064           JSR     @ICRLF  ; OTHERWISE TIMEOUT OCCURRED
 2   05473 006065           JSR     @IMESS  ; MESSAGE
 3   05474 004123           TMSG
 4                  ;
 5   05475 020404   WLP2:   LDA     0,RSW0  ; RESTORE 0
 6   05476 024404           LDA     1,RSW1  ; RESTORE 1
 7   05477 030404           LDA     2,RSW2  ; RESTORE 2
 8   05500 002404           JMP     @WRTN   ; RETURN
 9                  ;
10   05501 000000   RSW0:   0
11   05502 000000   RSW1:   0
12   05503 000000   RSW2:   0
13   05504 000000   WRTN:   0
14                  ;
15                  ;TTO NON INTERRUPT PACKAGE
16                  ;"MESS" PRINTS ASCII MESSAGES AS SPECIFIED BY ASSEMBLER
17                  ;"CHAR" PRINTS ASCII CHARACTRO, C(0)R, C(0)L MUST BE 0
18                  ;WILL RETURN +2 IF C(0)R=0, CORRECTS THE PARITY, 33 SIMULATE
19                  ;"TYPE" PRINTS C(0)R, MUST HAVE PROPER PARITY, RETURN IS
20                  ;TO CALL+1, REPLACE THIS ROUTINE WITH INTERRUPT TYPE IF DESIRED.
21                  ;"CRLF" PRINTS A CARRIAGE RETURN
22                  ;"POCT" PRINTS C(1) IN OCTAL FOLLOWED BY A TAB
23                  ;"PDEC" PRINTS C(1) IN DECIMAL, LEADING ZEROS SUPPRESSED.
24                  ;FOLLOWED BY A TAB.
25
26   05505 054545   MESS:   STA     3,MESSR ;PRINT A TEXT MESSAGE
27   05506 010544           ISZ     MESSR
28   05507 031400           LDA     2,0,3   ;C(2) POINTS TO MESSAGE
29   05510 024541           LDA     1,C377  ;A 8 BIT MASK
30   05511 021000           LDA     0,0,2   ;C(2)=DATA WORD
31   05512 125112           MOVL#   1,1,SZC
32   05513 123701           ANDS    1,0,SKP
33   05514 123401           AND     1,0,SKP ;C(0)=DATA CHARACTOR RIGHT
34   05515 151400           INC     2,2     ;INC TO NEXT WORD
35   05516 124000           COM     1,1     ;FLIP MASK
36   05517 004462           JSR     CHAR    ;PRINT
37   05520 000771           JMP     MESS+4  ;ANOTHER
38   05521 002531           JMP     @MESSR  ;LAST
39
40   05522 020525   ZOCT:   LDA     0,CH240
41   05523 101001           MOV     0,0,SKP
42
43   05524 020123   POCT:   LDA     0,C60
44   05525 030433           LDA     2,OCTAB ;PRINT C(1) IN OCTAL
45   05526 000403           JMP     .+3
46   05527 030441   PDEC:   LDA     2,DECTB ;PRINT C(1) IN DECIMAL
47   05530 020517           LDA     0,CH240 ;SUPPRESS LEADING ZEROS
48   05531 054447           STA     3,RADRET;BOTH ENTRYS PRINT NUMBER
49   05532 040445           STA     0,ZSUPP ;THEN TAB TO NEXT POSITION
50   05533 050401           STA     2,.+1
51   05534 000000   DECOCT: 0               ;A"LDA 2,TABLE" INSTRUCTION
52   05535 010777           ISZ     .-1
53   05536 034442           LDA     3,RADRET;SETUP "TAB" AT END
54   05537 020503           LDA     0,CHTAB
55   05540 151005           MOV     2,2,SNR ;IF TABLE ENTRY=0
56   05541 000440           JMP     CHAR    ;EXIT WITH TAB
57   05542 034435           LDA     3,ZSUPP ;ZEROS SUPPRESS STUF
58   05543 102400           SUB     0,0
```

```
 1  05544 146512  DECOT:  SUBL#   2,1,SZC
 2  05545 000405         JMP     DECP
 3  05546 146400         SUB     2,1       ;FORM THE DIGIT
 4  05547 034123         LDA     3,C60
 5  05550 101400         INC     0,0
 6  05551 000773         JMP     DECOT
 7  05552 151225  DECP:   MOVZR   2,2,SNR
 8  05553 034123         LDA     3,C60
 9  05554 054423         STA     3,ZSUPP   ;C(0)=DIGIT
10  05555 163000         ADD     3,0       ;MAKE ADCII
11  05556 004423         JSR     CHAR      ;PRINT
12  05557 000755         JMP     DECOCT    ;GET NEXT DIGIT
13
14  05560 030425  OCTAB:  LDA     2,.+1+.-DECOCT
15  05561 100000         100000
16  05562 010000         10000
17  05563 001000         1000
18  05564 000100         100
19  05565 000010         10
20  05566 000001         1
21  05567 000000         0
22
23  05570 030435  DECTB:  LDA     2,.+1+.-DECOCT
24        000012  .RDX 10
25  05571 023420         10000
26  05572 001750         1000
27  05573 000144         100
28  05574 000012         10
29  05575 000001         1
30  05576 000000         0
31        000010  .RDX 8
32
33  05577 000000  ZSUPP:  0
34  05600 000000  RADRET: 0
35
36  05601 054442  CHAR:   STA     3,CHRET   ;PRINT C(0) RIGHT
37  05602 101305         MOVS    0,0,SNR   ;RETURN +2 IF NULL
38  05603 001401         JMP     1,3
39  05604 040440         STA     0,CHSAV
40  05605 176000         ADC     3,3       ;COMPUTE THE PARITY
41  05606 117000         ADD     0,3
42  05607 163404         AND     3,0,SZR
43  05610 000775         JMP     .-3
44  05611 176660         SUBCR   3,3       ;COMBIND PARITY WITH CHAR
45  05612 020432         LDA     0,CHSAV
46  05613 163300         ADDS    3,0
47
48  05614 034426  CHAR1:  LDA     3,CHTAB   ;IS THIS A TAB
49  05615 116405         SUB     0,3,SNR
50  05616 000403         JMP     .+3       ;YES
51  05617 004434         JSR     TYPE      ;NO PRINT IT
52  05620 002423         JMP     @CHRET    ;EXIT
53
54  05621 020424         LDA     0,CHORZ   ;SIMULATE A TAB
55  05622 034424         LDA     3,CHARZ   ;VIA 1 TO 8 SPACES
56  05623 117405         AND     0,3,SNR
57  05624 002417         JMP     @CHRET
58  05625 020422         LDA     0,CH240
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 1  05626 004425           JSR     TYPE
 2  05627 000772           JMP     .-6
 3
 4  05630 054420  CRLF:    STA     3,CRLFR :SAVE RETURN
 5  05631 020410           LDA     0,C215
 6  05632 004747           JSR     CHAR    ;PRINT CHARRIAGE AND LF
 7  05633 020405           LDA     0,C212
 8  05634 004745           JSR     CHAR
 9  05635 102400           SUB     0,0
10  05636 040407           STA     0,CHORZ :CLEAR MORZ POSITION
11  05637 002411           JMP     @CRLFR  ;EXIT
12
13  05640 000212  C212:    212
14  05641 000215  C215:    215
15  05642 000001  CHTAB:   1
16  05643 000000  CHRET:   0
17  05644 000000  CHSAV:   0
18  05645 000000  CHORZ:   0
19  05646 000007  CHARZ:   7
20  05647 000240  CH240:   240
21  05650 000000  CRLFR:   0
22  05651 000377  C377:    377
23  05652 000000  MESSR:   0
24  05653 054406  TYPE:    STA     3,TYPRET;TYPE THE C(0)R IF
25  05654 010771           ISZ     CHORZ
26  05655 063511           SKPBZ   TTO
27  05656 000777           JMP     .-1
28  05657 061111           DOAS    0,TTO
29  05660 002401           JMP     @TYPRET
30  05661 000000  TYPRET:  0
31                .END
```

SYMBOL	VALUE	DEFINED	REFERENCES						
AD	002454	31:57	32:01						
ADRM	005257	61:58	59:36						
ALP2	004644	55:57	55:52	55:54					
ALPAT	004635	55:50	55:40						
BAC	005011	58:32	58:26						
C0210	000075	3:47	12:04						
C0421	000076	3:48	12:15						
C0600	000125	4:13	49:13						
C1	000110	3:58	7:45	15:34	17:21	19:20	25:12	26:42	28:51
			30:17	32:51	36:16	48:16	56:39	57:10	
C10	000104	3:54	14:25						
C100	000133	4:19							
C1042	000077	3:49	12:26						
C12	000060	3:31							
C140K	000101	3:51	14:13	14:22					
C144	000057	3:30							
C16	001325	17:32							
C1600	000124	4:12	49:11						
C177	000132	4:18	49:41						
C1777	000127	4:15	49:22						
C2	000111	4:01	17:13	48:17	48:34	48:37	56:22		
C20	000120	4:08	13:54	14:07	30:47	30:48	35:07	49:01	
C200	000102	3:52	14:37						
C2000	000107	3:57	48:47						
C212	005640	67:13	67:07						
C215	005641	67:14	67:05						
C3	000116	4:06	20:13	57:06					
C377	005651	67:22	65:29						
C4	000100	3:50	13:43	23:10	25:06	48:18	48:39	57:01	61:32
C40K	000073	3:45							
C44	000131	4:17							
C5	000112	4:02	30:11	48:06	56:04				
C54	000103	3:53							
C55	000314	6:23	8:01						
C6	000113	4:03	55:55	56:17					
C60	000123	4:11	22:19	23:47	49:02	51:31	51:49	59:18	59:40
			65:43	66:04	66:08				
C7	000114	4:04	57:14						
C70	000121	4:09	48:50	49:54					
C7367	000130	4:16							
C77	000126	4:14	49:17						
C77K	000117	4:07	13:49	14:02					
CBLK	000273	6:06	51:47	52:01	52:30	52:48	59:51	60:25	60:45
			61:13						
CCNTR	000305	6:16	58:46	58:57					
CERM	005254	61:54	59:23						
CERR	005044	59:05	58:53						
CH240	005647	67:20	65:40	65:47	66:58				
CHAN	000072	3:44	3:16						
CHAR	005601	66:36	5:13	65:36	65:56	66:11	67:06	67:08	
CHAR1	005614	66:48							
CHAR2	005646	67:19	66:55						
CHORZ	005645	67:18	66:54	67:10	67:25				
CHRET	005643	67:16	66:36	66:52	66:57				
CHSAV	005644	67:17	66:39	66:45					

SYMBOL	VALUE	DEFINED	REFERENCES						
CHTAB	005F42	67:15	65:54	66:48					
CLOP	005027	58:48	58:58						
CM60	000132	4:10	48:52	49:56					
CMP	001774	18:18	18:22						
CNTR	004762	57:30	56:09	56:13	56:29	56:34	56:45	56:55	
CO104	000074	3:46	11:51						
COMB	005014	58:36	58:21						
COMP	004773	58:16	5:15						
CONW	005037	58:56	5:42	59:08	59:14				
CR	004335	50:15	50:09						
CRLF	005630	67:04	3:36						
CRLFR	005650	67:21	67:04	67:11					
CRTN	000303	6:14	58:16	58:35	59:01	59:16	59:41	59:56	60:08
			60:15	60:30	60:39	61:48			
CSEED	000217	5:20	17:20	18:06	18:58	19:25	25:37	26:38	29:03
			31:03	32:36	36:24	56:46	56:48		
CSRD	002256	28:31	27:20						
CSRD2	002270	28:41	28:34						
CURPT	000215	5:18	7:20	17:22	19:19	25:13	28:50	30:18	36:15
			55:36	55:53	55:56	55:57	56:05	56:18	56:23
			56:40	57:02	57:07	57:15	61:19	63:24	
CURSE	000201	5:06							
CYCLE	004531	53:44	3:40						
CYM	005331	62:55	62:52						
DAERR	000160	4:46							
DALAT	000162	4:48							
DCODE	004216	48:42	3:38	48:54	49:06				
DECOC	005534	65:51	66:12	66:14	66:23				
DECOT	005544	66:01	66:06						
DECP	005552	66:07	66:02						
DECTB	005570	66:23	65:46						
DERIN	000146	4:33	54:13	59:05					
DEV1	004267	49:28	49:15	49:20					
DEVCD	004245	49:09	49:31						
DEVIC	000055	3:28	49:07	49:24					
DEVNU	005761	45:39	48:46						
DIAG	000400	7:07	3:18						
DMBIT	000222	5:23	17:46	18:08					
DMSK	000265	5:58	51:51	59:43					
DPALL	000155	4:40	18:46	28:09	35:22	55:29			
DPAT1	000152	4:37							
DPAT2	000153	4:38							
DPAT3	000154	4:39							
DRET	000054	3:27	48:42	49:32					
DSC0	001577	21:37	5:46						
DSC1	001600	21:38							
DSC2	001601	21:39							
DSC3	001602	21:40	21:10	23:03					
DSFAL	000164	4:50	20:39	22:46					
DSINC	001603	21:42							
DSK5	002556	33:16	33:10	33:16	33:30	35:40	35:48		
DSK6	000252	5:47	33:11	33:31	35:41	35:49			
DSKAD	002156	27:05	25:11	26:45	27:22	28:31	28:32	28:35	28:42
DSKM	001605	21:44	22:18	24:06					
DSKN	001604	21:43	20:26	21:05	22:20	22:56	23:08	23:09	23:48

SYMBOL	VALUE	DEFINED	REFERENCES						
ECODE	003007	36:28	3:34						
EDIAG	004134	47:41	5:26	16:02	19:05	21:32	28:29	35:35	
EHALT	006071	3:42	9:08	9:13	9:20	9:27	9:33	9:39	9:45
			9:53	10:02	10:09	10:16	10:27	10:35	10:43
			10:55	11:06	11:13	11:19	11:28	11:37	11:45
			11:56	12:09	12:20	12:31	12:39	12:47	12:56
			13:06	13:15	13:26	13:34	13:45	13:56	14:09
			14:18	14:27	14:39	14:47	14:55	15:05	15:13
			15:27	15:45					
ENTER	004500	53:17	3:39						
EOC2	004135	47:42							
EOC4	004143	47:48	48:09	48:13	48:28				
EOCIN	000150	4:35	7:38	15:52	17:24	18:50	20:16	21:18	22:07
			23:25	23:40	23:57	25:15	28:14	30:21	35:26
			64:55						
EPMS	004164	48:11	48:08						
EPRIN	004572	54:22	54:15						
EPSM	004114	47:22							
ER	000071	3:41	3:42						
ERC5	000377	6:29	58:17	58:54					
ERCN	000307	6:18	58:18	58:55	59:12				
ERET	004551	54:03	54:20						
ERHLT	000136	4:25	54:17	61:37					
ERHRT	004554	54:06	54:34						
ERNO	000165	4:52	7:17	8:06	9:03	53:27	54:26		
ERR	004544	53:56	3:41						
ERR1	004557	54:10	54:02						
ERR3	004601	54:30	54:19						
ERRCT	004523	53:37	53:30	54:06					
ERROR	000157	4:45	26:04	26:54	31:39	33:05			
ESCP	003020	36:39	27:43	34:22					
ESWIT	004522	53:36	53:29	54:11	54:22	54:28			
EXPM	005264	62:06	59:30						
FIRST	000062	3:33	49:09						
HEADE	004606	54:36	54:25						
HISEC	000173	4:58	25:28	26:19	27:24	27:47	30:35	32:21	33:55
			34:31						
HISSC	000176	5:03	30:36	34:52					
HSSEC	000227	5:28	30:37	32:05	33:46	34:55			
ICHAR	000210	5:13	22:22	23:50	51:38	51:43	51:48	51:58	52:02
			52:13	52:19	52:29	52:31	52:41	52:47	52:49
			59:21	59:50	59:52	60:06	60:13	60:24	60:26
			60:37	60:44	60:46	60:56	61:06	61:12	61:14
ICOMP	000212	5:15	18:23	27:01	33:12				
ICONW	000245	5:42	61:39	61:51					
ICRLF	000064	3:36	7:07	7:21	7:42	7:53	15:56	17:28	18:54
			20:20	21:22	22:10	23:28	23:44	24:02	25:19
			27:32	27:41	28:17	30:25	34:12	34:20	34:33
			34:41	34:57	35:30	48:44	51:15	54:23	57:19
			59:15	63:06	63:50	65:01			
IDPAT	004735	57:06	55:43						
IDSC0	000251	5:46	21:06	22:57	23:13				
IEDIA	000202	5:07							
IEOC2	000225	5:26	7:29						
IIBUF	000170	4:55	10:13	10:20	10:31	10:39	18:07	18:13	26:46

SYMBOL	VALUE	DEFINED	REFERENCES						
			32:54						
IIMOD	000224	5:25	47:48						
IINTB	000230	5:29	63:56						
IM3	000256	5:51	23:17						
IM3P	000260	5:53	23:34						
IM4	000253	5:48	28:55						
IM5	000235	5:34	30:42						
IM52	000262	5:55	30:16	35:54	35:57	36:09			
IM5A	000254	5:49	30:32						
IM5AD	000264	5:57	30:53						
IM5D	000255	5:50	32:12	32:24					
IM5O	000300	6:11	36:10						
IM5P	000277	6:10							
IM5U	000263	5:56	32:29						
IMD5	000240	5:37	36:25						
IMES	000065	3:37	7:08	7:22	7:43	7:54	15:57	17:29	18:55
			20:21	21:23	22:11	22:17	23:29	23:45	24:03
			24:05	25:20	27:33	27:42	28:18	30:26	34:13
			34:21	34:34	34:42	34:58	35:31	48:45	51:16
			51:23	51:28	54:24	57:20	59:22	59:29	59:35
			61:26	62:51	63:11	63:15	63:31	64:04	65:02
IMODE	004146	47:52	5:25						
IMUS	000241	5:38	35:39	35:50					
INC2	004700	56:31	56:35						
INCE	000246	5:43	17:18	18:02	25:10	26:36	28:57	30:15	32:34
			36:20	56:25	56:36				
INCM	005303	62:26							
INCPA	004670	56:22	55:42						
INPTP	000231	5:30	63:49	63:55	64:06				
INST1	003121	37:53	64:11						
INST2	003131	38:04	64:12						
INST3	003141	38:13	64:13						
INST4	003152	38:23	64:14						
INST5	003165	38:35	64:15						
INST6	003175	38:44	64:16						
INST7	003210	38:56	64:17						
INST8	003225	39:12	64:18						
INST9	003253	39:35	64:19						
INSTA	003274	39:53	64:20						
INSTB	003316	40:14	64:21						
INSTC	003342	40:35	64:22						
INSTD	003370	40:58	64:23						
INSTE	003406	41:15	64:24						
INSTF	003422	41:28	64:25						
INSTG	003431	41:36	64:26						
INSTH	003440	41:44	64:27						
INSTI	003456	42:01	64:28						
INSTJ	003476	42:18	64:29						
INSTK	003515	42:34	64:30						
INSTL	003535	42:51	64:31						
INSTM	003555	43:10	64:32						
INSTN	003573	43:25	64:33						
INSTO	003606	43:37	64:34						
INSTP	003624	43:52	64:35						
INSTQ	003644	44:11	64:36						

SYMBOL	VALUE	DEFINED	REFERENCES					
M2C	001413	18:34	19:14					
M2C2	001451	19:12	19:09					
M2CRD	001444	19:07	18:33					
M2EXT	001430	18:50	19:23					
M2OUT	001436	18:58	18:52					
M2RD	001354	18:01	17:39	19:11				
M3B	001502	20:23	20:18	21:29				
M3C	001650	22:24	22:09					
M3E	001750	23:36	21:58					
M3G	001560	21:17	23:12					
M3H	001717	23:08	20:43	22:28	23:42	23:51	24:01	
M3I	001662	22:34	23:06					
M3INC	001575	21:34	21:02	22:31	22:54			
M3J	001767	23:53	22:52					
M3K	001642	22:17						
M3L	001730	23:17	23:27					
M3M	001762	23:47	24:07					
M3N	001623	22:02	21:14					
M3O	001526	20:45	20:41					
M3OUT	001570	21:27	21:20					
M3P	001543	21:02	5:53					
M4B	002033	25:22	25:17					
M4CTS	002055	25:44	5:48	25:31	25:46	25:52	26:17	26:18	27:39
M4EXT	002237	28:13	28:53					
M4M	002211	27:41	27:46					
M4N	002121	26:28	26:21					
M4NX	002173	27:22	28:45					
M4O	002226	27:55	29:04					
M4OUT	002250	28:23	28:16					
M4P	002304	28:54	27:53	28:06				
M4RLP	002131	26:40	27:28	28:40				
M4WLP	002057	25:47	26:25					
M52	002557	33:17	5:55					
M5AA	002315	30:06	30:50					
M5AB	002553	33:13	30:52					
M5AC	002364	30:49	30:09					
M5AD	002745	35:44	5:57					
M5B	002341	30:29	30:23					
M5CFP	002737	35:37	5:50					
M5CT	002403	31:10	30:43					
M5CTS	002747	35:46	5:34					
M5EXT	002727	35:26	36:18					
M5K	002654	34:33	34:38	34:51	34:54			
M5L	002471	32:14	32:04					
M5M	002616	33:55	33:45					
M5N	002663	34:41	34:46					
M5O	002640	34:20	34:25					
M5P	002676	34:52	34:49					
M5Q	002575	33:36	6:11					
M5R	002621	34:01						
M5RLP	002527	32:49	33:53	34:08				
M5S	002753	35:54	33:34					
M5T	002764	36:06	35:56					
M5U	002653	34:31	34:28					
M5V	002630	34:08	36:04					

SYMBOL	VALUE	DEFINED	REFERENCES						
INSTR	003661	44:25	64:37						
INSTS	003673	44:36	64:38						
INSTT	003706	44:48	64:39						
INTB	005422	64:11	5:29						
IOBUF	000167	4:54	17:45	20:23	22:33	25:53	31:30		
IONE	000247	5:44	61:23	63:28					
IPASS	003735	45:17	15:58	18:56	21:24	28:19	35:32		
IPCNT	000243	5:40	28:20	52:51	61:34				
IPCT2	000244	5:41	18:40	20:58	26:14	27:15	31:51	33:27	53:24
IPDEC	000206	5:11	62:50						
IPINS	000232	5:31	7:33						
IPOCT	000207	5:12	22:16	23:32	54:27	59:28	59:34		
IPRT	000312	6:21	63:18						
IPTBL	000223	5:24	55:31	55:58					
IPTRN	000213	5:16	17:31	25:41	31:07	35:43	58:30		
ISTEP	000203	5:08	20:42	22:48	26:06	26:57	31:42	33:08	
ISTP	000311	6:20	63:20						
ISTRT	000214	5:17	18:36	20:55	23:24	23:39	23:56	26:11	27:12
			28:25	31:47	33:23	53:21	53:50	59:11	
IT4IN	000220	5:21	7:57	27:36	27:45	34:16	34:24	34:37	34:45
			35:03	57:23					
ITR	004520	53:34	3:32	53:25					
ITRCT	004521	53:35	53:26						
ITTBL	000221	5:22	8:08						
ITYPE	000211	5:14							
IWLP	000301	6:12	17:51	20:34	22:41	25:57	26:49	31:34	32:58
LAST	000063	3:34	49:29						
LASTV	003723	45:05	22:12						
LOADR	000052	3:25							
LOCKI	003741	45:22	7:09						
LOOP	000070	3:40	9:09	9:14	9:21	9:28	9:34	9:40	9:46
			9:54	10:03	10:10	10:17	10:28	10:36	10:44
			10:56	11:07	11:14	11:20	11:29	11:38	11:46
			11:57	12:10	12:21	12:32	12:40	12:48	12:57
			13:07	13:16	13:27	13:35	13:46	13:57	14:10
			14:19	14:28	14:40	14:48	14:56	15:06	15:14
			15:31	15:49					
LOOPR	004530	53:42	53:17	53:32	53:53				
LOWSE	000172	4:57	25:30	26:39	27:38	27:48	28:54	30:39	30:41
			31:12	32:37	34:18	34:26			
LOWSS	000175	5:02							
LPERS	000137	4:26	18:38	20:56	26:12	27:13	31:49	33:25	53:22
LPTST	000140	4:27	7:48	18:42	21:27	25:23	28:04	30:30	35:18
			53:51						
LSSEC	000226	5:27	30:40	31:15	32:16	32:39	34:03	34:39	34:47
M1	000134	4:20	17:41	20:27	22:34	25:47	26:40	31:25	32:49
			56:06						
M12	000105	3:55							
M16	000106	3:56							
M1A	000446	7:53	7:58	8:03	8:12				
M1B	000442	7:48	7:40						
M20	000115	4:05	18:12						
M22	001406	18:28	17:16	19:07	19:10	19:13			
M2B	001324	17:31	17:26	19:22					
M2B2	001464	19:25	18:44						

SYMBOL	VALUE	DEFINED	REFERENCES						
M5WA	002404	31:12							
M5WLP	002420	31:25	5:38						
M5Y	003000	36:19	35:20						
M5Z	002702	34:57	35:04	35:09					
M6A	004201	48:26	48:20						
M6B	004204	48:30	48:22						
M6C	004202	48:27	48:24	48:31	48:38	48:40			
M7A	004214	48:39	48:36						
MESS	005505	65:26	3:37	65:37					
MESSR	005652	67:23	65:26	65:27	65:38				
MOD1M	004006	46:04	7:44						
MOD1S	000141	4:28							
MOD2B	001330	17:36	17:57						
MOD2M	004023	46:18	17:30						
MOD2S	000142	4:29							
MOD3B	001617	21:55	20:47						
MOD3C	001506	20:27	5:51	21:13					
MOD3D	001731	23:20	20:50						
MOD3M	004042	46:34	20:22						
MOD3S	000143	4:30							
MOD3T	000257	5:52	20:25	21:04	21:55	22:04	22:13	22:24	22:29
			23:16	23:20	23:31	23:33			
MOD4A	002044	25:32	27:50	27:55					
MOD4B	002052	25:41	26:26						
MOD4D	002227	28:02	27:26						
MOD4L	002201	27:32	25:25	27:37	27:52				
MOD4M	004052	46:43	25:21						
MOD4R	002124	26:35	25:35						
MOD4W	002230	28:04	26:30						
MOD5A	002354	30:41	35:12						
MOD5B	002371	30:55	5:37						
MOD5D	002720	35:16	33:57						
MOD5L	002631	34:12	5:49	34:17	34:30	35:06			
MOD5M	004066	46:56	30:27						
MOD5R	002510	32:33	6:10	31:01					
MOD5W	002721	35:18	5:56	35:28					
MODA	002401	31:08	30:51						
MODAL	000156	4:41	47:43						
MODE	000166	4:53	7:15	7:46	17:14	20:14	25:07	30:12	47:41
			48:04	48:05	48:12	48:15	48:27	48:33	61:31
MODE0	004156	48:04	47:52						
MODE1	000430	7:37	47:53						
MODE2	001303	17:13	47:54						
MODE3	001471	20:13	47:55						
MODE4	002014	25:06	47:56						
MODE5	002321	30:11	47:57						
MODE6	004167	48:15	47:58						
MODE7	004206	48:33	48:01						
MSAD	005230	61:27	61:25						
MSAD2	005364	63:32	63:30						
MSAV	000056	3:29							
MXSEC	000174	5:01	22:05	25:27	30:34				
NODSM	001611	21:48	23:46						
NSDIS	000161	4:47	20:45	22:50					
NSSC	000177	5:04	30:19	30:44	31:16	31:53	32:40	33:36	35:10

SYMBOL	VALUE	DEFINED	REFERENCES						
NSSCM	003052	37:10	35:01						
NWC	005010	58:31	58:24						
OCTAB	005560	66:14	65:44						
ONEM	005267	62:11	5:44						
ONEPA	004650	56:04	55:45						
P0S	005373	63:40	63:03	63:33					
P1S	005374	63:41	63:04	63:34					
P2NX	001454	19:16	18:48						
P2NX2	001462	19:22	19:29						
P2RTN	005372	63:39	63:02	63:36					
P2S	005375	63:42	63:05	63:35					
P4NX	002275	28:47	28:11						
P5NX	002771	36:12	35:24						
PASS	000050	3:23	7:14						
PAT1	004653	56:07	56:20	57:04	57:12	57:18	57:27		
PAT2	004657	56:11	56:14						
PAT4	004620	55:31	55:37						
PATBL	004625	55:40	5:24						
PATE	000233	5:32	7:18	19:17	26:23	28:36	28:39	28:44	28:48
			29:01	35:37	35:58	36:03	36:07	36:13	36:22
			55:50	56:24	56:41	57:11	58:19		
PATES	000234	5:33	28:37	28:43	36:01	36:06			
PATRN	004611	55:23	5:16						
PCNT	005323	62:48	5:40						
PCRTN	005371	63:38	62:48	62:53					
PCT2	005334	63:02	5:41						
PCT3	005351	63:18	63:13						
PCUR	004623	55:36	55:26						
PDEC	005527	65:46	5:11						
PINLP	005401	63:50	64:07						
PINS	005376	63:47	5:31						
PIRTN	005421	64:09	63:47	63:54	64:02				
PMSK1	000274	6:07	60:51						
PMSK2	000275	6:08	61:01						
PMSK3	000276	6:09	61:09						
POCT	005524	65:43	5:12						
POSS	000304	6:15	58:37	58:56	60:50	60:58	61:08	61:47	
PRINS	000135	4:24	7:26	18:34	20:53	23:22	23:37	23:54	26:09
			27:10	28:23	31:45	33:21	53:19	53:48	59:09
			63:51						
PRT	005354	63:24	6:21						
PRTN	004763	57:31	55:23	56:07	56:26	56:42	57:08		
PWT	004354	51:28	51:21						
PWT2	005347	63:15	63:10						
RADRE	005600	66:34	65:48	65:53					
RANM	005307	62:31							
RANP2	004721	56:50	56:56						
RANPA	004707	56:39	55:41						
RD2WR	000151	4:36	18:31	27:18	33:32				
RDONL	000144	4:31	17:37	25:33	30:56				
RETUR	004524	53:38	53:44	53:54	53:56	54:08	54:10		
RSW0	005501	65:10	64:50	65:05					
RSW1	005502	65:11	64:51	65:06					
RSW2	005503	65:12	64:52	65:07					
RWFLG	000306	6:17	17:44	18:04	20:30	22:37	25:50	26:43	31:28

SYMBOL	VALUE	DEFINED	REFERENCES						
			32:52	51:19	63:08				
SAV0	004527	53:41	54:01	54:05	54:30				
SAV1	004526	53:40	53:58	54:04	54:31				
SAV2	004525	53:39	53:45	53:57	54:03	54:32			
SAVE1	004463	52:57	51:08	52:53					
SAVE2	004464	52:58	51:09	52:54					
SECM	005277	62:21							
SECP	003010	36:30	27:34	34:14					
SELM	005317	62:41							
SELPT	000250	5:45	7:13	57:16	57:25				
SESCP	003041	36:58	34:43						
SETUP	000067	3:39	9:06	9:11	9:16	9:23	9:30	9:36	9:42
			9:48	9:56	10:05	10:12	10:19	10:30	10:38
			10:49	10:58	11:09	11:16	11:22	11:31	11:40
			11:48	12:01	12:12	12:23	12:34	12:42	12:50
			13:01	13:09	13:18	13:29	13:37	13:48	14:01
			14:12	14:21	14:30	14:42	14:50	14:58	15:08
			15:16	15:33					
SH4FL	004312	49:53	50:04						
SHFL	004224	48:49	48:58						
SLPAT	004744	57:14	55:47	57:24					
SLPM	004765	57:33	57:21						
SMSK1	000271	6:04	52:36	60:32					
SMSK2	000272	6:05	52:44	60:41					
SRDM	004472	53:08	51:24	63:12					
SRTN	004460	52:53	51:13						
SSECP	003027	36:47	34:35						
SSEED	000216	5:19	17:19	18:05	19:01	19:26	25:38	26:37	29:02
			31:04	32:35	36:23				
SSINC	000237	5:36	31:56	33:39					
SSONE	000236	5:35	31:13	32:09	32:15	32:38	33:50	34:02	
SSWM1	003102	37:36	7:23						
STAER	004334	51:07	5:08						
STARS	000310	6:19	51:07	52:55	63:19				
STER2	004356	51:31	51:26						
STERI	000147	4:34	51:11						
STERM	004467	53:04	51:17						
STERS	000204	5:09	20:37	22:44	22:49	26:02	26:52	31:37	33:03
			51:32	51:39					
STMK1	004465	53:01	51:33						
STMK2	004466	53:02	51:40						
STP	004373	51:47	6:20						
STRT	000404	7:12	5:17	7:34					
STTS	000205	5:10	20:38	22:45	26:03	26:53	31:38	33:04	51:50
			52:06	52:15	52:21	52:35	52:43		
SWFLG	000261	5:54	17:17	17:47	19:03	19:18	19:28	25:09	25:54
			28:49	28:58	30:14	31:14	36:14	36:21	55:24
SWTM	004475	53:12	51:29	63:16					
SZERM	002004	24:09	24:04						
T01	000543	9:01	3:33	7:51	8:13				
T02	000552	9:11	8:14						
T03	000556	9:16	8:15						
T04	000564	9:23	8:16						
T05	000572	9:30	8:17						
T06	000577	9:36	8:18						

SYMBOL	VALUE	DEFINED	REFERENCES			
T07	000604	9:42	8:19			
T10	000611	9:48	8:20			
T11	000620	9:56	8:21			
T12	000626	10:05	8:22			
T13	000634	10:12	8:23			
T14	000642	10:19	8:24			
T15	000654	10:30	8:25			
T16	000663	10:38	8:26			
T17	000674	10:49	8:27			
T1OUT	001301	16:01	15:54			
T20	000704	10:58	8:28			
T21	000714	11:09	8:29			
T22	000722	11:16	8:30			
T23	000727	11:22	8:31			
T24	000737	11:31	8:32			
T25	000747	11:40	8:33			
T26	000756	11:48	8:34			
T27	000770	12:01	8:35			
T30	001002	12:12	8:36			
T31	001014	12:23	8:37			
T32	001026	12:34	8:38			
T33	001035	12:42	8:39			
T34	001044	12:50	8:40			
T35	001054	13:01	8:41			
T36	001063	13:09	8:42			
T37	001073	13:18	8:43			
T40	001105	13:29	8:44			
T41	001114	13:37	8:45			
T42	001126	13:48	8:46			
T43	001140	14:01	8:47			
T44	001152	14:12	8:48			
T45	001162	14:21	8:49			
T46	001172	14:30	8:50			
T47	001205	14:42	8:51			
T4CY	000242	5:39	7:16	28:27	62:49	
T4IM	004326	50:09	49:58			
T4IN	004310	49:51	5:21			
T4OUT	004324	50:06	50:12			
T50	001214	14:50	8:52			
T51	001223	14:58	8:53			
T52	001232	15:08	8:54			
T53	001241	15:16	8:55			
T54	001255	15:33	8:56			
T54C	000313	6:22	15:43			
TAC	005012	58:33	58:28			
TIN	004274	49:34	48:49	49:53		
TINRE	000051	3:24	49:34	49:45		
TMSG	004123	47:30	65:03			
TMSK1	000266	6:01	52:07	59:58		
TMSK2	000267	6:02	52:16	60:10		
TMSK3	000270	6:03	52:22	60:17		
TNOM	004104	47:13	7:55			
TRET	004332	50:14	49:51	50:06	50:07	50:11
TRKAD	000171	4:56				
TSMSK	001576	21:35	21:56	22:14	22:25	

SYMBOL	VALUE	DEFINED	REFERENCES						
TTBL	000466	8:12	5:22						
TYPE	005653	67:24	5:14	66:51	67:01				
TYPIN	000066	3:38	7:10						
TYPRE	005661	67:30	67:24	67:29					
WCNTR	000302	6:13	17:42	20:28	22:35	25:48	26:41	31:26	32:50
			64:47						
WCPAT	004731	57:01	55:44						
WCPT	004764	57:32	57:03						
WDCTR	000053	3:26							
WLP	005460	64:47	6:12						
WLP2	005475	65:05	64:57						
WORM	005313	62:36							
WPROM	003065	37:22	23:30						
WRERR	000163	4:49	20:48						
WRK1	000200	5:05	31:54	31:58	33:37	33:41			
WRONL	000145	4:32	17:54	26:28	32:27				
WRTN	005504	65:13	64:53	65:08					
XX377	001075	13:20	13:13	13:23					
XXITR	000061	3:32							
ZERM	005273	62:16							
ZERPA	004664	56:17	55:46						
ZOCT	005522	65:40							
ZSUPP	005577	66:33	65:49	65:57	66:09				

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