PART 2

ALTOS COMPUTER SYSTEMS
8500 CENTRAL PROCESSING UNIT PCB
HARD DISK CONTROLLER PCB
TAPE CONTROLLER PCB
I/O PORT ASSIGNMENTS
SCHEMATICS

Table of Contents

PART TWO

SCHEMATICS

LIST OF FIGURES

LIST OF TABLES

1. 8500 CENTRAL PROCESSING UNIT PRINTED CIRCUIT BOARD AND THE EIGHT-INCH HARD DISK CONTROLLER BOARD.

The following two sections are dedicated to a detailed discussion of the 8500 CPU PCB and the eight-inch hard disk controller PCB. Most of the information contained in these sections are for user reference only.

2. THE 8500 CPU PRINTED CIRCUIT BOARD (PCB).

Most of the data contained in this Section is for inrormation purposes only as the operating system handles the operations discussed herein. The 8500 CPU PCB has the capability of supporting up to four floppy disk drives and up to two eight-inch hard disks. Figure 2-1 is a matrix map of the 8500 PCB.

2.1 Memory.

The 8500 PCB Memory bank switching allows selection of the bank the DMA will access independently of tne bank selected for access by the CPU. Thus, the CPU may be operating in one memory bank when the DMA interrupts to read from or write to another memory bank. This requires two more bits (UN3 and UN4) at port 25.

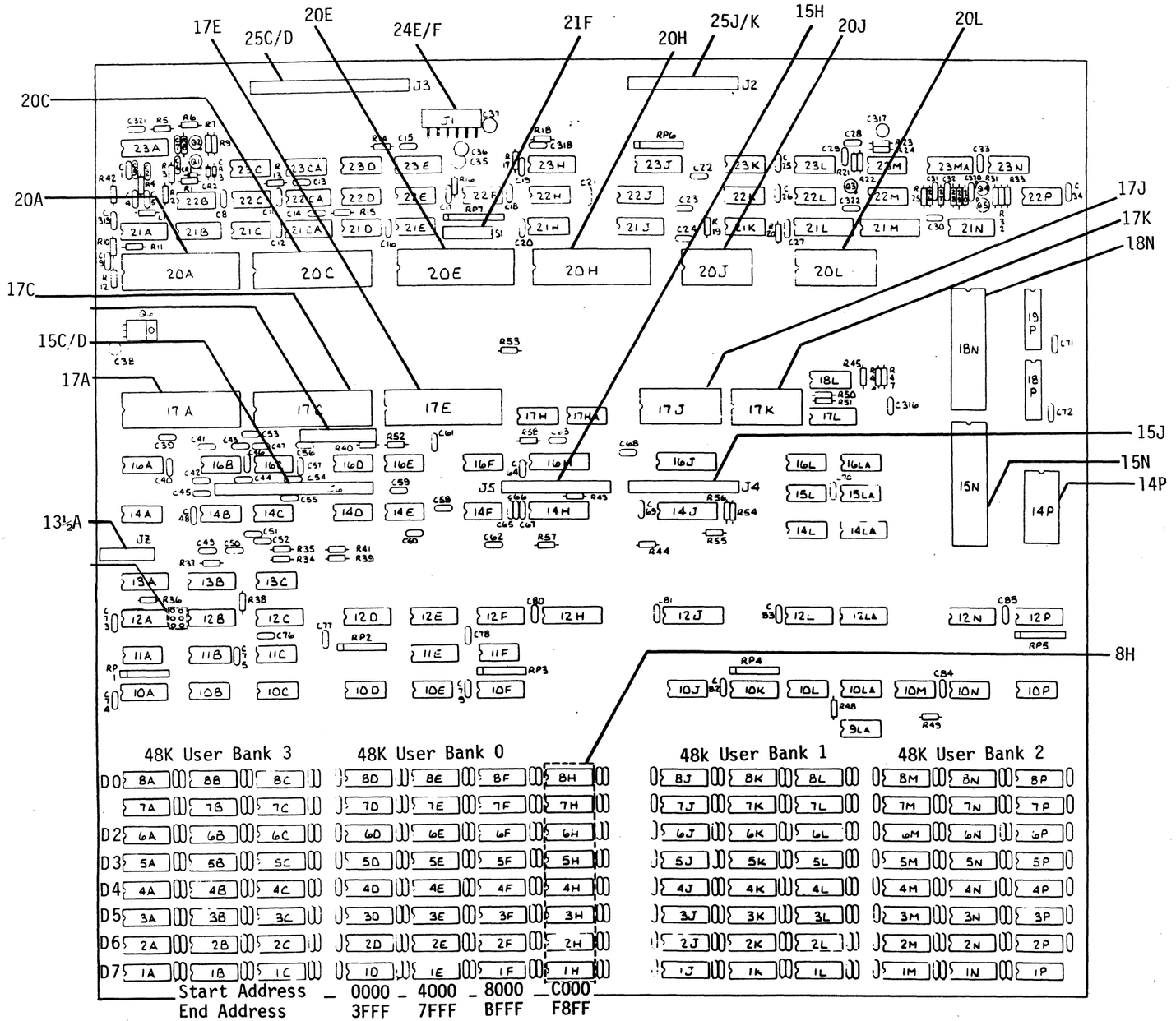
The ability to swap the fixed 16K address space from high-order memory to low-order memory has been facilitated by a pair of jumpers (S21 and S22), on the PCB at matrix positions 12A/B. This jumper allows the user to configure the system for OASIS, CP/M or MP/M operating systems. The write protect function operates on the common memory only, independently of whether common memory is pinned to be in high-order or low-order space.

2.2 Tne Hard Disk Controller (HDC).

The hard disk controller is a separate PCB that attaches, piggyback, onto the right side mother board. Tnis allows different types of disk drives to be used. Currently, the hard disk controller that will mount on the 8500 board is the for the soft-sectored drives suchas the SA1000.

2.3 Floppy Disk Controller (FDC).

When double-sided floppy disk drives are installed, they are pinned for accessability as one logical drive with two heads via the side-select control line.



Matrix Position	Purpose
12A/B	Operating System Selection Jumper Block
13 1/2A	High Speed Serial Connector
17A	SIO IC Console #4, Printer #2
15C/D	RS232 Connector to Rear Panel
16 1/2C/D	High Speed Networking Jumper Block
17C	SIO IC Consoles #2 and #3
20A	FDC IC 1797
20C	FDC PIO IC
17E	SIO IC Console #1, Printer #1
25C/D	FDC Connector
20E	PIP IC Memory Bank Select
24E/F	Power Connector
21F	S1 System Configuration Block
20H	PIO IC Parallel Printer
25J/K	Parallel Printer Port
15H	MTU Connector
20J	AMD 9511 FPP
20L	CTC IC
17J	Address Decoder IC
17K	CTC IC
18N	Z80
15J	HDC Connector
15N	DMA IC
14P	EPROM IC
8H	16K Ram Common Bank

Figure 2-1. 8500 CPU PCB Matrix Map.

2.3 --Continued.

When switching from one floppy drive to another, it is necessary to force unloading of the head-load signal. This insures that, when the newly selected drive is READ from or WRITTEN to, the head load delay one-shot in the controller circuit will be triggered and delay sufficiently for the head of the newly selected drive to settle. This is done by doing a SEEK with the head load flag bit set to unload the head at the beginning.

The FDC IC chip has been changed from the FD1791 to the FD1797. The 1797 IC chip is able to read to some single-density diskettes that the 1791 cannot.

Bit 1 on the 1797 establishes which side is being compared; bit 3 dynamically alters the code for the sector length field (This is done in conjunction with the sector length byte in the header). Thus, the side select bit changes from bit 3 to bit 1, and the option not to compare is not available. To maintain compatibility with the present sector length field code, bit 3 should be set to bit 1.

The 1797 has an output that can be used to control the side-select line to the disk drive. This happens automatically as determined by bit 1 in the READ and WRITE commands. However, the CPU board is wired to use bit 5 out of the PIO at B7 to do this selection. If necessary, the signal from the 1797 can be used to control side select by cutting a trace and installing a jumper at S25.

2.4 Magnetic Tape Unit Controller.

The magnetic tape controller is a separate PCB that attaches, piggyback, onto the left side of the 8500 board. It currently controls a Data Electronics Inc., (DEI) funnel drive.

2.5 I/O Port Assignments for the 8500 PCB.

Table 2-1 lists the I/O port assignments with their corresponding schematic reference and functions. Table 2-2 lists the bit assignments for the I/O port.

Table 2-1. I/O Port Assignments for the 8500 PCB

PORT NUMBER	SCHEMATIC REFERENCE	FUNCTION
00-03	Y0 (DMA)	Initialize DMA.
04	Y1 (FD1797)	Input drive/controller status. Output command.
05	(Floppy disk)	Input/output track number.
06		Input/output sector number.
07		Input data. Output data when WRITING to the disk and the desired track number prior to doing a SEEK.
08	Y2 (PIO-CH A)	Input interrupts from FDC and from HDC. Output floppy disk drive select, and recording density.
09	Y2 (PIO-CH B)	Input END from 9511A, DISK CHANGE, CPU board type and two-sided (TS) signal from floppy disk drive. Out put MR to FDC chip.
0A	Y2 (PIO-CH A)	Initialize channel A.
0B	Y2 (PIO-CH B)	Initialize channel B.
0C	Y3 (CTC-CH 0)	Baud rate generator for console number 1 at JX.
0D	Y3 (CTC-CH 1)	not used.
0E	Y3 (CTC-CH 2)	Baud rate generator for printer number 1 at JT.
0F	Y3 (CTC-CH 3)	Used to count index pulses of the floppy disk drive.
10	Y4 (PIO-CH A)	Parallel port I/O at J2 (normally used in I/O mode).
11	Y4 (PIO-CH B)	Parallel port I/O at J2 (normally used for data in an I/O mode).
12	Y4 (PIO-CH A)	Initialize channel A.
13	Y4 (PIO-CH B)	Initialize channel B.
14-17	Y5 (IPL)	An output to any of these ports turns off the PROM after initial program load (IPL).
18	Y6 (9511)	Input/output data from the 9511's stack.
19	"	Input status, output commands to/from the 9511.
1A	"	Same as 18.
1B	"	Same as 19.

Table 2-1. Continued

PORT NUMBER	SCHEMATIC REFERENCE	FUNCTION
1C	Y7 (DART-CH A)	Input/output data to I/O port at JX (normally Console #1). Input status of channel A. Output commands to CH A.
1E	Y7 (DART-CH B)	Input/output data to I/O port at JT (normally printer number 1).
1F	"	Input status of channel B. Output commands to CH B.
20	Y8 (Hard Disk)	Output drive and head number to HDC.
21	"	Output sector number and old cylinder number to the HDC; also input and output data to or from the hard disk via the DMA.
22	"	Output new cylinder number to the controller.
23	"	Output commands to the controller. Input status of the controller.
24	Y9 (PIO-CH A)	Input configuration of CPU and controllers.
25	Y9 (PIO-CH B)	Input nothing. Output memory write protect bit and memory bank select bits.
26	Y9 (PIO-CH A)	Initialize channel A.
27	Y9 (PIO-CH B)	Initialize channel B.
28	Y10 (SIO-CH A)	Input/output data to I/O port at JV (normally printer nummber 2 but on the 8500 is reconfigurable as a bisync modem port).
29	"	Input status of channel A. Output commands to CH A.
2A	Y10 (SIO-CH B)	Input/output data to I/O port at JZ (normally console number 4).
2B	"	Input status of channel B. Output commands to CH B.
2C	Y11 (SIO-CH A)	Input/output data to I/O port at JY (normally console number 2). Input/Output data to network port JW
2D	"	Input status of channel A. Output commands to CH A.

Table 2-1. Continued.

2E	Y11 (SIO-CH B)	Input/output data to I/O port at JU (normally console number 3).
2F	"	Input status of channel B. Output commands to CH B.
30	Y12 (CTC-CH 0)	Baud rate clock for console # 2 at JY.
31	Y12 (CTC-CH 1)	Baud rate clock for consoles # 3 and #4 at JU and JZ.
32	Y12 (CTC-CH 2)	Baud rate clock for printer number 2 at JV.
33	Y12 (CTC-CH 3)	Real time clock generator for time slicing the usage of the processor.

Kill Clock on MP/MII + 10 output 21 to 33H

Table 2-2. Bit Assignments, Input/Output Signals for I/O Ports

PORT # SCH. REF.	BIT #	DESCRIPTION
00-03 (DMA)		(See Zilog DMA Manual)
04-07 (FD1797)		(See the applicable Western Digital data sheet).
08 Y2 (PIO-CH A)	7	INTERRUPT input from the HDC.
	6	INTERRUPTinput from the FDC chip.
	5	DRIVE SELECT 4 to select drive D. 0=unselected, 1=selected. Select only one drive at a time.
	4	DRIVE SELECT 3 to select drive C.
	3	DRIVE SELECT 2 to select drive B.
	2	DRIVE SELECT 1 to select drive A.
	1	HLD input from the floppy disk controller chip to indicate when the head is loaded. 0=not loaded; 1=loaded.
	0	DDEN output to set the recording mode. 0=single density, 1=double density.
09 Y2 (PIO-CH B)	7	TWO-SIDED (TS) input from the floppy disk drive. 0=single-sided diskette, 1=two-sided diskette.
	6	Input (hardwired) to indicate the type of PCB. 0=8500..
	5	Side select output to the floppy disk drives (unless SSO on the controller chip is used). 0=side 0 selected, 1=side 1 selected.
	4	Not connected.
	3	Not connected.
	2	DISK CHANGE input from the floppy disk drive. (See the disk drive spec sheet for details).
	1	(master reset) (/MR)output to the floppy disk controller chip. Normally a 1, take 50 seconds to reset.
	0	END, input from the 9511A to indicate the completion of a calculation.
OA		(See Zilog PIO Manual)
OB		(See Zilog PIO Manual)

Table 2-2. Continued.

ØC Y3 (CTC-CH Ø)	In Out	2 Mhz. Baud rate for channel A of the DART that outputs to JX (normally console number 1).
ØD Y3(CTC-CH 1)	In Out	2 Mhz. Not attached.
ØE Y3 (CTC-CH 2)	In Out	2Mhz. Baud rate for channel B of the DART that outputs to JT (normally printer number 1).
ØF Y3 (CTC-CH 3	In Out	Index pulses from the selected floppy diskk drives. (None).
1Ø Y4 (PIO-CH A)	7 6 5 4 3 2 1 Ø	(Unnamed) normally an input from printer to PIO SELECT " BUSY " PAPER EMPTY " FAULT " CNTL normally an output to the printer. INPUT PRIME " DATA STROBE "
11 Y4 (PIO-CH B)	7 6 5 4 3 2 1 Ø	DATA 7 normally an output to the printer. DATA 6 " DATA 5 " DATA 4 " DATA 3 " DATA 2 " DATA 1 " DATA Ø "
12-13 Y4 (PIO-CH A)		(See Zilog PIO Manua).
14-17 Y5 (IPL)		An output to any of these ports turns off the PROM after initial program load (IPL)
18,19 Y6 (9511A) 1A Y6 (9511A) 1B Y6 (9511A)		(See the AMD9511A specification sheet). Same as 18 Same as 19

Table 2-2. Continued.

1C Y7 (DART-CH A)		(Refer to the Zilog Manual)
1D Y7 (DART CH A)		(Refer to the Zilog Manual)
1E Y7 (DART-CH B)		(Refer To Zilog Manual)
1F YA (DART-CH B)		(Refer to Zilog Manual)
20-23 Y8 (Hard disk)		(See the HARD DISK interface specifi-
24 Y9 (PIO-CH A)		All bits have yet to be assigned. They will be pinned to indicate the type(s) of controllers attached to the CPU board.
25 Y9 (PIO-CH B)	7	UN4, MSB of a two bit nibble that sets the bank of memory that DMA accesses.
	6	UN3, LSB of the above nibble.
	5	WRITE PROTECT, output to the hardware to prevent writing into the upper 16K of memory space. 0=not protected, 1=write protected.
	4	UN2, MSB of a two bit nibble that sets the bank of memory that the CPU accesses.
	3	UN1, LSB of the above nibble.
	2	Unassigned.
	1	Unassigned.
	0	Unassigned.
26, 27		(Refer to the Zilog Manual)
28 (SIO-CH A) 28 to 2B		Console # 4
2A Y10 (SIO-CH B)		Printer #2
2B		(Refer to the Zilog Manual)
2C (SIO-CH A) 2C to 2F		Console # 2
2D		(Refer to the Zilog Manual)
2E Y11 (SIO-CH B)		Network 1

Table 2-2. Continued.

30 Y12 (CTC-CH 0)	In Out	2Mhz. Baud rate for channel A of the SIO that outputs to JY (normally console number 2).
31 Y12 (CTC-CH 1)	In Out	2Mhz. Baud rate for channel B of the SIO that outputs to JU and channel B of the SIO that outputs to JZ (normally consoles 3 and 4).
32 Y12 (CTC-CH 2)	In Out	2Mhz. Baud rate for channel A of the SIO that outputs to JV (normally printer number 2).
33 Y12 (CTC-CH 3)	In Out	2Mhz. (none).

2.6 Z80 Interrupt Daisy Chain.

On the Z80 interrupt chain the SIOs are at the bottom of the chain so they can return from interrupt by a command rather than by RETI instruction which ripples down the daisy chain. See Table 2-3 for the interrupt daisy chain sequence.

Table 2-3. Interrupt Daisy Chain

Top of chain	YO	DMA
	Y2	PIO (Hard disk, Floppy disk and 9511 interrupts)
	Y4	PIO (user's port)
	Y3	CTC (Baud rates and timer)
	Y12	CTC (baud rates and real time clock)
	Y7	SIO (console 1 and Printer 1)
	Y10	SIO (printer 2 and Console 4)
Bottom of Chain	Y11	SIO (Consoles 2 and 3)

2.7 ALTOS Interface Connector Wiring.

Table 2-4 lists the pin connections of the device connectors on the rear of the ACS8000 computer. All of the console connectors are Serial I/O devices as is the serial printer jack. The auxiliary printer connector is a Parallel I/O device available to the user.

Table 2-5 lists the Parallel I/O Pin connectors.

Table 2-4. Serial I/O Connector

Pin	Use
1	Chassis Ground
2	Transmitted Data
3	Received Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	Signal Ground
20	Data Terminal Ready*

*All ALTOS CP/M, MP/M and ADX system diskettes require pin 20 (Data Terminal Ready) handshaking.

Other pins are not used. Request to Send (pin 4) and Clear to Send (pin 5) are not normally implemented. Jumpers on the Printed Circuit board allow their conection. Pin 8 is tied high through a resistor. Contact ALTOS for instructions for activating Request to Send or Clear to Send.

Table 2-5. Parallel I/O Connector

Pin	Use
1	Data Source
2	Data Ø
3	Data 3
4	Data 1
5	Data 6
6	Data 7
7	Acknowledge
8	Busy
9	Data 2
1Ø	Data 4
11	Data 5
12	Control
13	Select
14	+5 Volts
15	Paper Empty
16	-12 Volts
17	Input Prime
18	Floating
19	Floating
26	Unassigned
34	Fault
35	Unassigned
36	+12 Volts

All of the remaining pins are ground

3. ALTOS EIGHT INCH HARD DISK CONTROLLER, MTU CONTROLLER, AND THE SHUGART EIGHT-INCH SOFT-SECTORED DRIVE.

Most of the data contained in this Section is for information purposes only, as the operating system handles the operations discussed herein. This section discusses the ALTOS eight-inch hard disk controller, the MTU controller, and the specifications for the Shugart eight-inch soft sectored drive. For further information on the Shugart eight-inch soft-sectored drive, refer to the SA1000 Fixed Disk Drive Service Manual.

3.1 Eight-inch Hard Disk Controller.

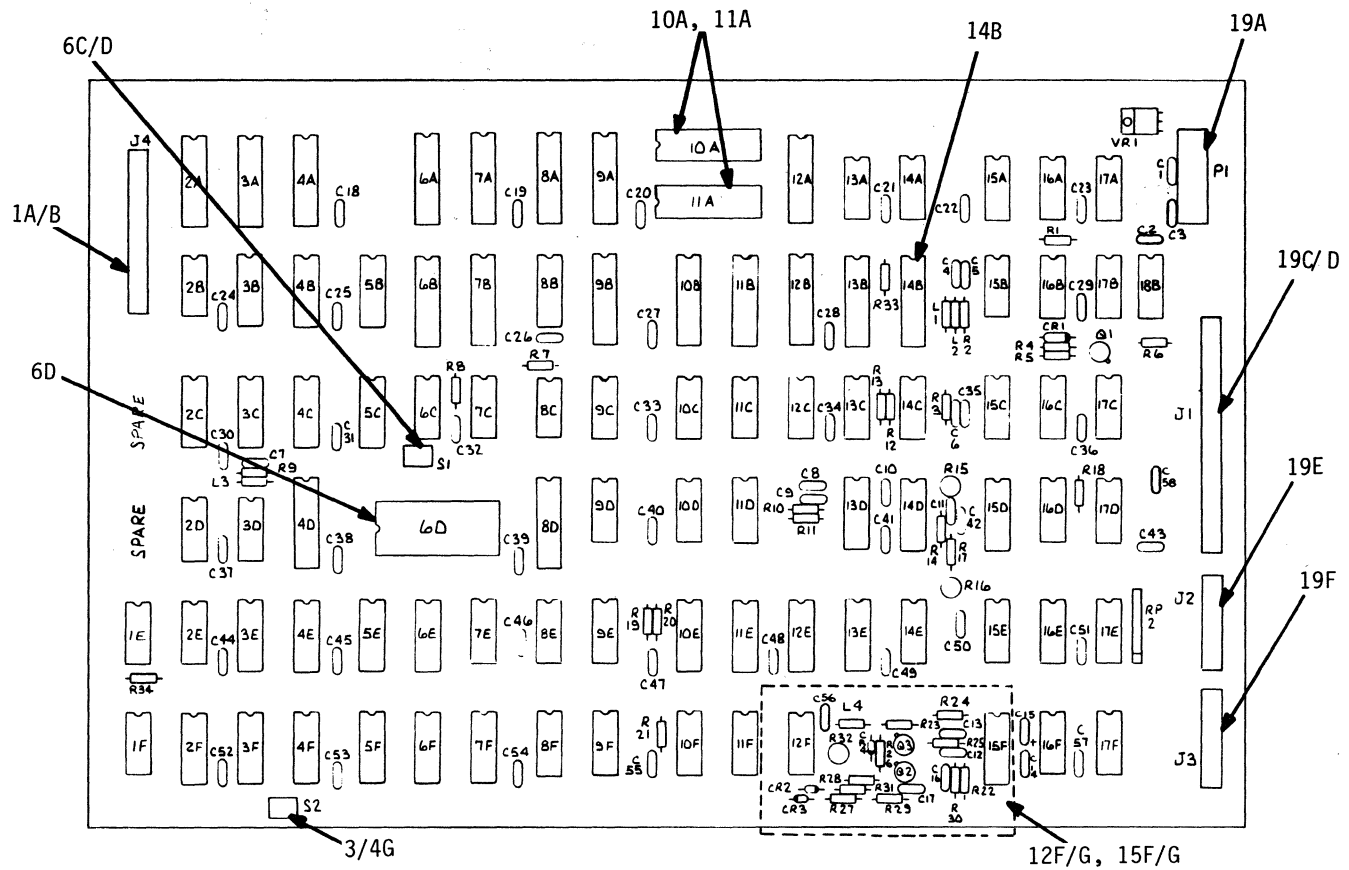
See Figure 3-1 for a diagram of the eight-inch hard disk controller matrix map. Jumper S1 on the controller must be set to coincide with the type of hard disk in the system. This must be set to S for the Shugart drive. This jumper determines the cylinder number, 128, at which write precompensation takes place. See Figures 3-2a, b, c, d and e for connector and pin assignments for the eight-inch hard disk controller.

Data is stored on the disks in blocks or sectors of 256 bytes (not programmable), identified by cylinder, head and sector numbers. The addresss for each sector is previously written (by a FORMAT command) ahead of the data field. When reading from or writing to the disk, this address is read and verified. A correct match must be found for the address and its check bytes before the sector can be written to or read from.

The general procedure to read or write data is to first position the heads over the desired cylinder via a SEEK command, load the head and sector numbers into the appropriate ports, and finally, issue a READ or WRITE command. When the correct sector is found, the data is transferred between disk and system memory under control of the DMA by way of a FIFO buffer. The controller is addressed by way of four I/O ports (020H-023H). Table 3-1 lists the four ports and their corresponding read and write addresses.

Table 3-1. Addresses

Port	Read	Write
020H	X	Drive and head numbers
021H	Data	Old cylinder number (in two bytes), sector number and data
022H	X	New cylinder number in two bytes
023H	Status	Commands



6D	FPLA
1A/B	J4 CPU Interface
6C/D	S1 Precomp Block
10A, 11A	FIFO Buffers
14B	Programmable Array Logic (PAL)
19A	P1 Power
19C/D	J1 50-Pin Daisy Cahin Cable
19E	J2 20-Pin Radial Cable Drive 1
19F	J3 20-Pin Radial Cable Drive 2
12F/G, 15F/G	PLO Circuitry
3/4G	S2 Sector Size Configuration Block

Figure 3-1. Eight-Inch HDC Controller Board Matrix Map.

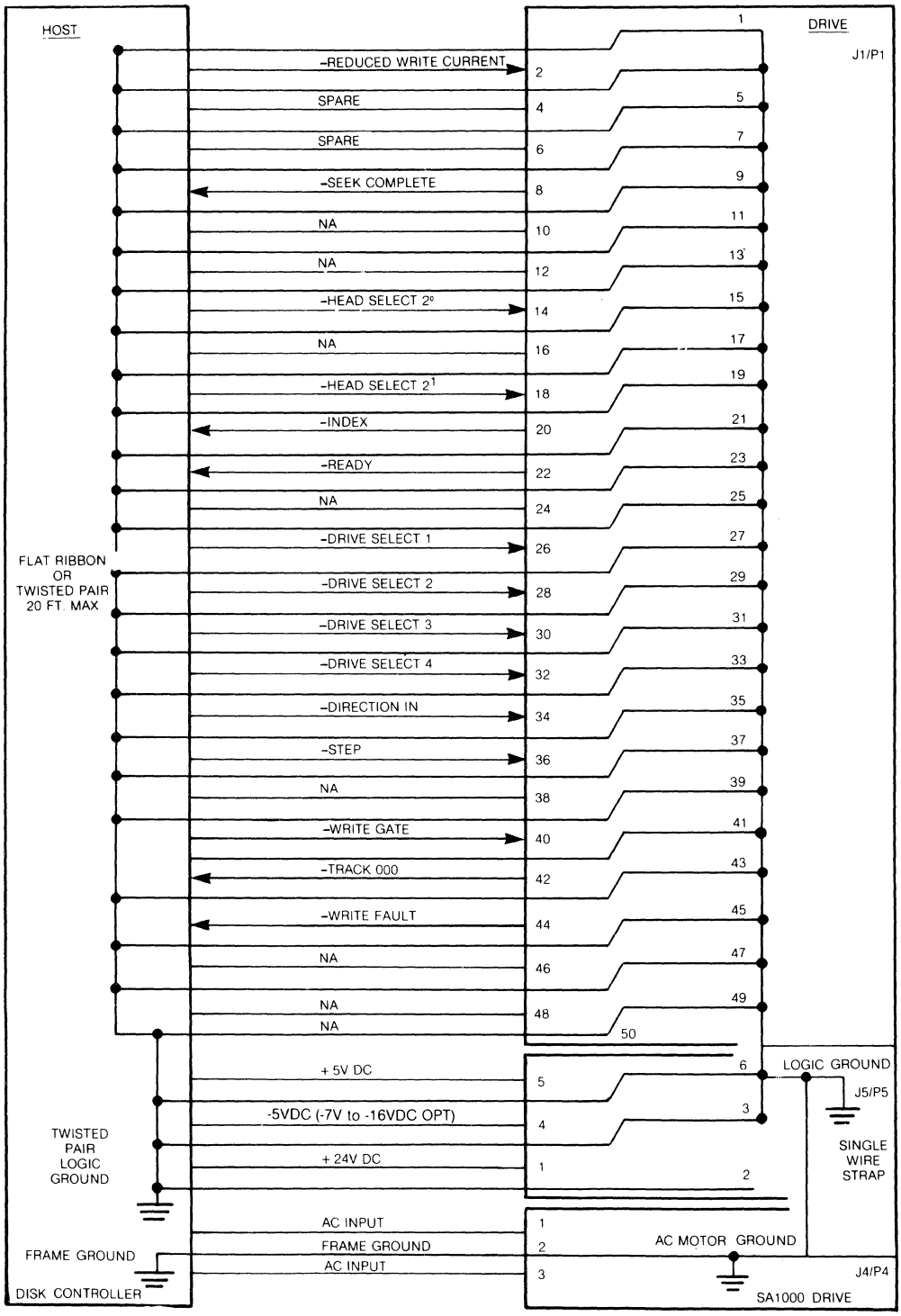


Figure 3-2a. 50-Pin Daisy Chain Connector for the 8-inch Hard Disk Controller

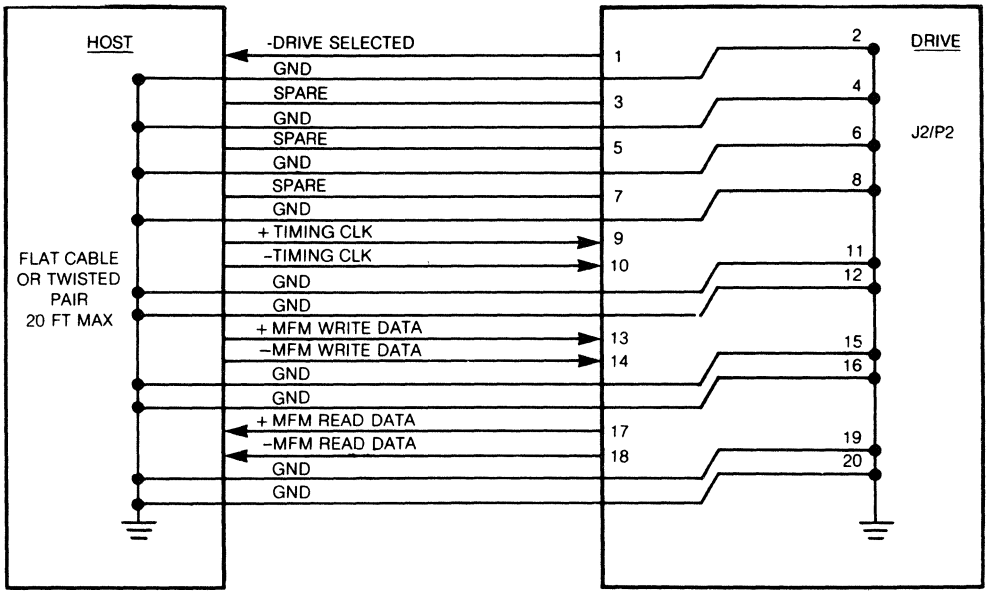


Figure 3-2b. 20-Pin Radial Connector to Drive 1

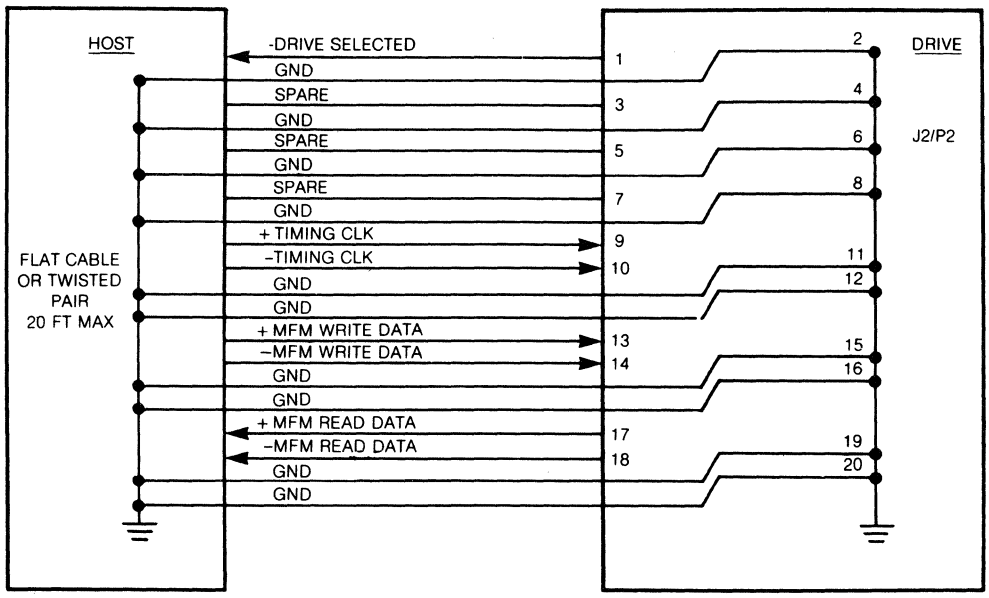


Figure 3-2c. 20-Pin radial connector to Drive 2

1	Ground
2	INT (interrupt), output to CPU, goes true at completion of a command
3	(not used)
4	/HDWR, output from controller, negative AND of controllers' address (Y8) and /IOWR, used to control transceivers on the CPU PCB
5	/Y15 (not used by this controller)
6	Ground
7	/HDRD, output from controller, negative AND of controllers' address (Y8) and /IORD, used to control transceivers on the CPU PCB
8	/MR RESET from CPU
9	Ground
10	/IORD, input to controller, negative AND of /RD and /IORQ
11	DIOB3
12	DIOB7 (MSB of bidirectional data bus)
13	DIOB2
14	Ground
15	DIOB1
16	DIOB6
17	Ground
18	/IOWR, input to controller, negative AND of /WR and /IORQ
19	/HDWAIT, output (not used by this controller)
20	DIOB5
21	DIOB4
22	Ground
23	DIOBØ, (LSB of bidirectional data bus)
24	ABØ, input, (LSB of CPU's address bus
25	Ground
26	AB1, input
27	/RDMA, (ready DMA), output from controller to start and pace transfer of data
28	/BUSAKB, (bus acknowledge output bit), input from CPU, true-to-false transition is used by controller to recognize completion of a data transfer
29	System clock
30	Ground
31	/Y8, input to controller, used with ABØ and AB1 to address the controller
32	/RDB (CPU/DMA read signal), output from controller to properly position the RDMA signal (i.e., early in a transfer cycle)
33	Ground
34	1Mhz input from CPU

Figure 3-2d. 34-Pin CPU-to-Controller Interconnect Cable

1	Ø	Volts
2	Ø	Volts
3	-12	Volts
4	+5	Volts
5	+5	Volts
6	+12	Volts (not used by this controller)

Figure 3-2e. Power Connector P1

3.1.1 Commands/Command Ports.

Port Ø23H is the command port when writing and the status port when reading. There are seven commands that may properly be issued. These commands, when issued, cause associated circuity functions. Table 3-2 contains the Commands and associated bit number.

COMMAND	FUNCTION
NULL	Quiescent state
RESET	Initializes the controller circuit. A reset is done automatically at power on and is not normally required thereafter.
RECAL	Positions the heads over track zero. This must be done for each drive following power on before any disk access is attempted and thereafter as part of the error recovery routine. A recal requires about 18 msec/cylinder for a maximum time of approximately 4 seconds.
SEEK	Moves the heads from the programmed "old cylinder" to the programmed "new cylinder".
READ	Reads the addressed sector from the disk.
WRITE	Writes to the addressed sector to the disk.

3.1.1 --Continued.

FORMAT — Formats an entire track. (This consists of writing out the address or header for each sector on the specified track by cylinder and head.)

Table 3-2. Commands (Port 023H)

Command	bit number								Hex
	7	6	5	4	3	2	1	0	
NULL	0	0	0	0	0	0	0	0	00
READ	0	0	0	0	X	0	0	1	01
WRITE	0	0	0	0	X	0	1	0	02
FORMAT	0	0	0	0	X	1	0	0	04
SEEK	0	0	0	1	X	0	0	0	10
RECAL	0	0	1	0	X	0	0	0	20
RESET	1	0	0	0	X	0	0	0	80

3.1.1 --Continued.

No more than one command may be issued at one time. For all the commands except NULL and RESET, when the command has been completed, the controller will issue an interrupt (via the PIO at port 008H bit 7). Following the interrupt, the status port is read to clear the status register via the clearing all status latches and to permit subsubsequent interrupts. If more than one command is outstanding (i.e., a second command issued before the status register is cleared), both commands will be aborted.

3.1.2 Status/Status Port.

The status byte, also on port 023H, reports on the status of the drive or controller. The status byte should be read at the completion of every operation. Table 3-3 lists the bits of the Status Byte and their meaning.

3.1.2 --Continued.

STATUS BYTE	DESCRIPTION
READY	Indicates that the selected drive has power and is up to speed. No operation will take place until a drive is selected and ready is true. Normally being READY indicates that the drive is ready to be read from or written to but a special case exists with this Shugart drive: **upon being powered on these drives require a two minute stabilization time before they should be read from or written to. Unfortunately, READY will go true before these two minutes are up (in about five seconds) and does not allow for this warm-up time.**
WRITE FAULT	Indicates a disk error during writing. To clear a write fault, the selected drive must be de-selected then re-selected.
CRC ERROR	Indicates that either the header or data field read off the disk was in error. If the operation was a write, the error occurred while reading the header and the sector was not written to. If the operation was a read, then the error could have occurred in either the header or data field. If it occurred in the header, the operation was aborted and the data field was not read. If it occurred in the data field, the data was transferred before the error was detected.
RECORD NOT FOUND (RNF)	During a READ or WRITE operation the specified header was not found in four revolutions of the disk. This may be caused by a seek error or incorrectly specified head or sector. RNF During a read may also indicate that the data sync field (00, A1 or F8) was not found even after the header was located. This is most likely caused by trying to read a sector that had been formatted, but before it was written to.

BAD SECTOR	The sector to be read or written was previously specified as a bad sector. A sector is flagged as bad during disk initialization with a 1 at bit 3 of the header byte. Good sectors have a Ø at bit 3.
TASK COMPLETE	The requested command was carried out or aborted. Analysis of the status byte will show whether or not the operation was aborted.
BUSY	The controller is in the process of carrying out an operation. BUSY is a Ø at the completion of an operation.

Table 3-3. Status byte (Port 023H)

Bit	Mnenomic	Meaning
7	RDY	Selected drive is ready
6	WR FLT	Write fault (from drive)
5	(none)	
4	CRC ERR	CRC error encountered
3	RNF	Record not found
2	BD SECT	Bad sector encountered
1	TC	Task complete
0	BUSY	Busy

3.1.3 PORTS 022H, 020H and 021H

Port 022H is used for writing the new cylinder number. This is entered in two consecutive bytes, the low order eight bits first, then the high order three bits.

Cylinder Bytes	Bits							
Least significant	7	6	5	4	3	2	1	0
Most significant	X	X	X	X	X	A	9	8

Port 021H has the following three functions:

a. Before doing a SEEK the old cylinder is entered (in two bytes as for new cylinder).

b. Before doing a READ or WRITE, the sector number is entered into this port,

c. When data is being transferred between disk and memory, it is done through port 021H.

Port 020H is used for selecting the drive and head to be used. The heads are selectable in a binary sequence (limited by the number of heads on the drive). One or the other but not both drives can be selected. Table 3-4 contains the drive-head byte bit numbers, names and their functions.

Table 3-4. Drive/head byte (Port 020H)

Bit	Name	Function
7	HS3	Head select bit 3
6	HS2	Head select bit 2
5	HS1*	Head select bit 1
4	HS0*	Head select bit 0
3		(none)
2		(none)
1	DS2	Drive select 2
0	DS1	Drive select 1

*Table 3-5. Head Select

Head Select Bits HS1	HS2	Head Number Selected SA1004
0	0	0
0	1	1
1	0	2
1	1	3

3.2 Formatting.

Since the SA1000 drive is soft-sectored, an entire track must be formatted at one time to maintain the proper timing relationship among the sectors. The heads must be positioned to the desired cylinder using the SEEK command. Then a header image consisting of four bytes, an 0FEH, cylinder number, head number, and sector number must be placed in memory and written out to the disk by the DMA. This is done as each sector arrives under its head during one rotation of the disk. The cylinder number in the header must agree with the cylinder on which the heads are positioned. The head number must agree with the selected head. The sector;number does not have to correspond to any system, allowing for staggering of the sectors if required.Tne DMA must be programmed for a four-byte continuous transfer. Table 3-6 lists and describes the byte header image.

Table 3-6. Header Image

Byte	Description
Sync	ØFEH
Cylinder	Low-order bits (7-Ø) of the cylinder number
Head	Head bits (3-Ø) in the top four bits, a bad sector flag at bit 3, and high order cylinder bits (A-8) at the bottom three bits
Sector	Sector number in hex

The FORMAT command must be issued to write a header. When that header has been written, an interrupt is generated. Then the header image must be updated to the next sector number (only the sector numbers change down the track), and a new FORMAT command issued before the next sector arrives at the head (464 μseconds for a 256-byte sector). The program must also keep count ot the number of sectors that have been formatted and stop issuing the FORMAT command when the last command for that track has been written. Wnen the interrupt occurs following the writing of the last sector's header, the status must be read and when the next interrupt occurs, the track is completely formatted and another command may be issued. (Following the next to last interrupt, a dummy or null command may be issued if necessary).

To format the entire disk the above procedure must be repeated for each head of each cylinder.

256 and 512 byte sector sizes are provided for. One track will accomodate 31 sectors at 256 bytes or 17 sectors at 512 bytes. Sector size is determined by jumper S2 on the controller. Two jumpers are used. Both must be in either the 256 or the 512 byte position.

The controller fills in every byte of the data field with Ø4EH while formatting. Following the formatting of a track, any attempt to read a sector on that track that has not been specifically written to will result in a RECORD NOT FOUND (RNF) since the sync bytes will be missing for these sectors. Each sector must subsequently be written to with some other data, (e.g., ØE5H to initialize the sector for CP/M or MP/M. Any data stored on a track is destroyed when that track is formatted.

3.2 --Continued.

The sequence of sectors on a track is under control of the formatting program. Physically adjacent sectors should not be read or written sequentially, because the data is transferred between disk and main memory under DMA control. System memory, composed of dynamic RAM, requires periodic clocking to maintain its data. This refresh is normally done by the CPU, but when the DMA is active, the CPU's refresh cycles are held off. To allow the memory to be properly refreshed, the CPU must regain control and generate the refresh cycles.

Soft sectoring the drive prevents performance of a specific READ ID command since the location of the sector on a track is unknown. When READING or WRITING, a sector is located by reading all the headers encountered along the track until the correct header is found. In a READ command, when the correct header is found, the header bytes are read off the disk and transferred into memory. As a diagnostic this verifies that the data read was from the specified sector.

3.3 Reading or Writing a Sector.

Assuming the drive has been properly initialized following power on by selecting and RECALing the drive, SEEK the desired cylinder loading the old cylinder number at port Ø21H (following a RECAL this would be ØØØH), loading the new cylinder number at port Ø22H, then issuing a SEEK command. An interrupt will occur when the head has arrived at the new cylinder and settled down (no additional head settle time is required).

To write or read a sector the sector must first be found. The controller does this by comparing the header images (written on the disk during formatting) as they pass under the head, to the bytes programmed into ports Ø20H-Ø22H (Ø20H has the head number, Ø21H has the sector number and Ø22H has the new cylinder number). The sector register gets written-over by data during a write. Before the next read or write command the sector number must be reissued to port Ø21H. Also, in switching between drives, even if a seek is not necessay, port Ø22H must be reloaded with the new cylinder number.

3.3.1 Reading a Sector.

To read a sector follow the procedure below:

a. Prepare a buffer area in main memory, to which the data from disk can be placed.

3.3.1 --Continued.

b. Program the DMA to transfer the desired number of bytes, either 256 or 512 for WRITE, or 259 or 515 for READ, from the controller's I/O port, Ø21H, to the buffer in memory using the CONTINUOUS mode and standard memory, and I/O timing (to properly pace the FIFO). When doing a READ, three additional bytes of header information that precede the data, cylinder, head/drive and sector are read off the disk. Just as they are written out during formatting. Along with 256 or 512 bytes of data these three bytes must be transferred by the DMA. There are also two bytes of CRC that follow the data. These may be transferred but it is not a requirement. Also, the DMA transfers one more byte than programmed for. Thus, the number of bytes the DMA is programmed to transfer will end up being two or four bytes longer than the sector length.

c. Load the address, cylinder, head/drive and sector, of the sector to be read. The cylinder number should already be correct from having done a SEEK.

d. Load the head number to port Ø2ØH without changing the drive number (they share the same byte).

e. Load the sector number at port Ø21H. A 2Ø-μsecond delay is required between selecting a drive or a head and issuing a read or write command, but the inherent programming delays normally take care of this.

f. Issue the READ command. When the drive/controller locates the desired sector, the controller signals the DMA and the data transfer is carried out by the DMA directly into memory. When the transfer is complete, the controller generates another interrupt and clears out the READ command. The status register must then be read. If a RNF is indicated, the data was not transferred to memory. If a CRC ERR for BAD SECTOR is indicated, the data was transferred but its accuracy is questionable.

3.3.2 Writing a Sector.

To write to a sector follow the procedure given below:

a. Fill the buffer area with data to be written to the disk. The header and CRC bytes are provided by the hardware, so only the data bytes must be transferred by the DMA.

3.3.2 --Continued.

b. Read the status register. If a RNF, CRC ERR, or BAD SECTOR is indicated, the data was not written to the disk. When writing, all the sync bytes are provided by the controller (in contrast with the technique used for the SA4000 which required a sync byte ahead of the data). However, when FORMATTING the drive, a sync byte of 0FEH must precede the header bytes.

3.4 Controller Responses.

It a command is issued before a drive is ready or selected, the controller will wait until the selected drive is ready before carrying out the operation. An interrupt is generated when the operation is completed.

Pressing RESET does not generate an interrupt; neither does selecting or deselecting a drive.

Reading from, and writing to the disk cannot be done by the CPU because of the high data rate. Except for some diagnostic tests, the data must be transferred by the DMA.

To prevent extraneous writes to the disk when the power goes off, the controller has a sensing circuit that deselects the drives when the +5v supply falls below +4.5V. This circuit does not, however, guarantee that data being written to a sector will be retained if power goes off. To insure data retention, power down the system only when no writing is being done to the disk.

3.5 Shugart Eight-inch Soft-sectored drive.

a. Logical Drives E and F are associated with the first hard disk. Drive E has a formatted capacity of approximately 8 Mbytes. Drive F has a formatted capacity of approximately 500 Kbytes.

b. Logical Drives G and H are associated with the second hard disk. Drive G has a formatted capacity of Approximately 8 Mbytes. Drive H has a formatted capacity of approximately 500 Kbytes.

Table 3-7. DISK DRIVE SPECIFICATIONS

Nominal track capacity	10416 bytes
Min track capacity (-3% speed)	10102 bytes
Formatted capacity (at 512 bytes)	8,912,896 bytes
Transfer Rate	230 nsec/bit 1.84 μsec/byte
Access Time	
Track to track	19 ms
Average	70 ms
Maximum	150 ms
Average latency	9.6 ms

Table 3-8. Format for Soft-sectored eight-inch Hard Disk

Start at: Index Pulse	Character(s) Written	
16	4E	
14	ØØ	Repeated 17 times for 512 byte
1	A1*	sectors when the
1	FE	cylinder is
1	[cylinder no.]	formatted
1	[head no.]	
1	[sector no.]	
2	[CRC character]	
1Ø	ØØ	
12	ØØ	
1	A1*	
1	F8	Written out when
512	[Data character]	a sector is written to
2	[CRC character]	
3	ØØ	
15	4E	
	<or>	
(as required)	4E	
Stop at: until sub-sequent Index pulse		

* Character written with one missing clock pulse.

3.6 Magnetic Tape Controller.

Figure 3-3 is the MTU Controller Matrix Map. Table 3-9 lists the signal-pin connections for the cable from the MTU Controller to the DEI tape drive.

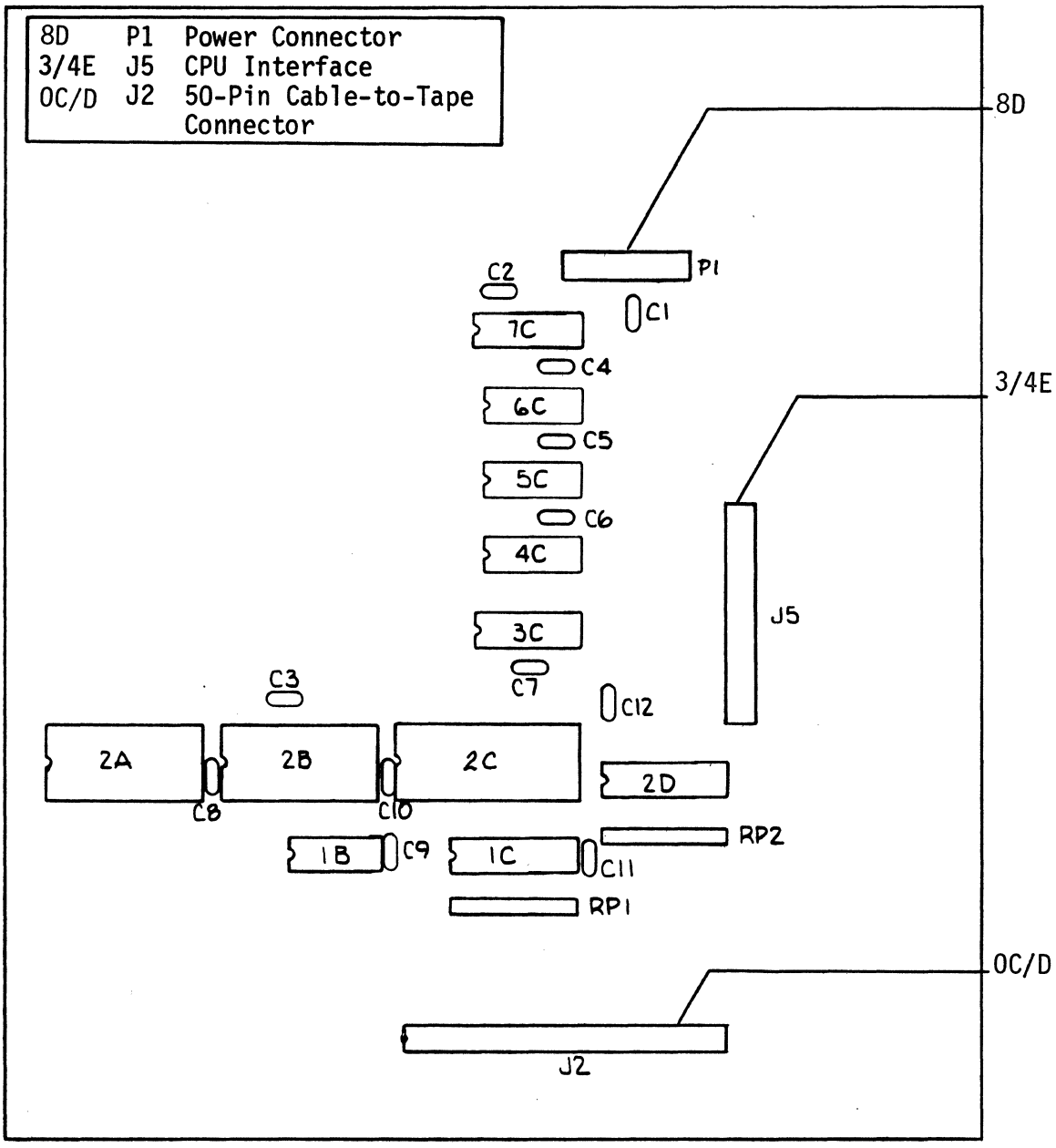


Figure 3-3. MTU Controller Board Matarix Map

Table 3-9. MTU Controller to DEI Drive Signal Pin Assignments

PIN #	SIGNAL	FROM	COMMENTS
2	SLD-	Drive	Selected
4	RDY-	Drive	Ready
6	WND-	Drive	Write Enabled
8	FLG-	Drive	Flag
10	LPS-	Drive	Load Point Sensed
12	FUP-	Drive	File Unprotected
14	BSY-	Drive	Busy
16	EWS-	Drive	Early Warning Sensed
18	RWD-	Controller	Rewind
20	REV-	Controller	Reverse
22	FWD-	Controller	Forward
24	HSP-	Controller	High Speed
26	WEN-	Controller	Write Enable
28	SL1-	Controller	Unit Select 2^0
30	SL2-	Controller	Unit Select 2^1
32	SL4-	Controller	Unit Select 2^2
34	SLG-	Controller	Select Gate
36	RNZ-	Drive	Read NRZ Data
38	RDS-	Drive	Read Data Strobe
40	DAD-	Drive	Data Detected
42	WDE-	Controller	Write Data Enabled
44	WNZ-	Controller	Write NRZ Data
46	TR2-	Controller	Track Select 2^1
48	WDS-	Drive	Write Data Strobe
50	TR1-	Controller	Track Select 2^0

NOTE: 1) All odd numbered pins are returns.

2) Mating connector: 3M Part Number 3425-3000 or equivalent.

8500 CPU PCB SCHEMATICS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	PROTOTYPE		
B	REVISED BD.		
C	REVISED BD. 1ST RUN	1/13/81	E.G.
D	REVISED P.C. 2ND RUN	2/10/81	C.N.
E	ECO # 0007	4/9/81	C.N.
F	ECO # 7330	9/14/81	E.G.
G	SEE SHEET 1	11/1/81	E.G.

S8 TP RD
S2 RAMRD
S8 HDRD
S5 GTRD
S5,2,8 DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
17Hø
LS20
S26 JUMPER
19P
LS241
S27 JUMPER
18P
LS241
+5
C71 .1uf
C72 .1uf
NMI
S5 WAIT
BUSRQ
INT
S2 2Ø
23L
8MHz
OSL
LS14
23Mø
S163
2MHz S4,6,5
1 MHz S7
½ MHz S7
R26 1K
TTL 58
C32 200pf
C31 200pf
R28 2.7K
R27 2.7K
R25 680
R29 4.7
Q4 2N3904
R31 10K
R30 120
Q5 2N3906
R32 10
C320 .1
C33 .1
R45 4.7
R46 4.7
R47 4.7
RØ
R53 39Ω
S4,5,8 MR RESET
S6 MASTER RESET
S4
R24 100uf
R23 2.7K
C317 100uf
S5 IPLW
22P LS74
PR CLR
LS00
22M
IOWR
S5
23N
LS32
AB12
S2 MEMRD
IPL S2
14P
2716
S29
OR CE
Z80A CPU
18N
S4,6 DØ
D1
D2
D3
D4
D5
D6
D7
Z80A DMA
15N
BUSRQ
BUSAK
M1
IORQ
MREQ
RD
WR
INT
SDMA
+5V
IEI
IEO
S4,6 AØ
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
12 La 8T97
14 La 8T97
12N 8T97
21N 8T97
ABIØ S3
AB9
AB8
AB7
AB6
AB5
AB15
AB14
AB13
AB12
AB11
AB4
AB3
AB2
AB1
ABØ
M1B
RFSHB
RDB
WRB
MREQB
IORQB
BUSAKB
HALTB N/W
RD
WR
MREQ
IORQ
BUSAK
R33 10K
21K LS32
RDB
IORQL
S5
WRB
IORD
S5
AB2
AB3
AB4
AB5
AB6
AB7
LS154 17K
YØ
Y1 S6
Y2 S6
Y3 S4
Y4 S4
Y5
Y6 S6
Y7 S4
Y8 S8
Y9 S6
Y10 S5
Y11 S5
Y12 S5
Y13
Y14 S8
Y15
Q3 2N3906
R21 1K
C28 .1uf
R22 1K
23M 74LS14
MR RESET
R44 1K
R43 2K
17Hø LS20
DRQ S6
RDMA S8
TPDMA S8
SIORDY S5
C316 .1uf

SPARE GATES

23N	LS32	2SP
21K	LS32	2SP
10N	574	1SP
12B	LS175	2SP
12A	S139	1SP
10M	LS00	1SP
22L	LS32	1SP
22K	LS02	1SP
23K	LS00	2SP
16La	LS04	3SP
15La	LS32	1SP
16L	LS02	1SP
14L	LS08	1SP
13C	LS74	1SP
21H	LS02	3SP
22C	LS32	3SP

NOTE: "S" INDICATES SHEET NUMBER

TOLERANCES UNLESS OTHERWISE SPECIFIED			ALTOS COMPUTER SYSTEMS
FRACTIONS ±	DEC ±	ANGLES ±	SCHEMATIC CPU P.C. BD.
APPROVALS		DATE	
DRAWN C.N.		1/26/81	
CHECKED			SCALE — SIZE D DRAWING NO. 005-1243-001
			DO NOT SCALE DRAWING SHEET 1 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

BANK 3 | BANK Φ | COM | BANK 1 | BANK 2

1A 1B 1C 1D 1E 1F 1H 1J 1K 1L 1M 1N 1P
2A 2B 2C 2D 2E 2F 2H 2J 2K 2L 2M 2N 2P
3A 3B 3C 3D 3E 3F 3H 3J 3K 3L 3M 3N 3P
4A 4B 4C 4D 4E 4F 4H 4J 4K 4L 4M 4N 4P
5A 5B 5C 5D 5E 5F 5H 5J 5K 5L 5M 5N 5P
6A 6B 6C 6D 6E 6F 6H 6J 6K 6L 6M 6N 6P
7A 7B 7C 7D 7E 7F 7H 7J 7K 7L 7M 7N 7P
8A 8B 8C 8D 8E 8F 8H 8J 8K 8L 8M 8N 8P

DIN 2 14 DOUT

+5 C81 .1uf
LS244 12J
DB7 DB6 DB5 DB4

+5 C80 .1uf
LS244 12H
DB3 DB2 DB1 DBØ

RAMRD S1
MEMRD S1
RDB S1
MREQB S1
AB12 S1
IPL S1
WRB S1
PICK
BUSAKB S1
WPRT S6

+5 C82 .1uf
DS3678 10K
WRITE 1
WRITE Ø
WRITE 3
WRITE 2
RP4 +5V

LS00 LS02 LS32

S3 ADMUX
S1 MREQ
S1 RFSHB
S1 MREQB
2Ø
M1B
Ø
S1 AB14
S1 AB15
+5 R49 1K
10La 574 CLR
10N 574 CLR
LS375 12B
LS139 12A
LS157 12E
S6 UN1
S6 UN2
S6 UN3
S6 UN4
BUSAKB
PICK
+5 R48 2K
+5 C74 .1uf
+5 C79 .1uf
DS3678 10A
DS3678 10F
RP1 RP3
10J 10B 10E
LS04

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

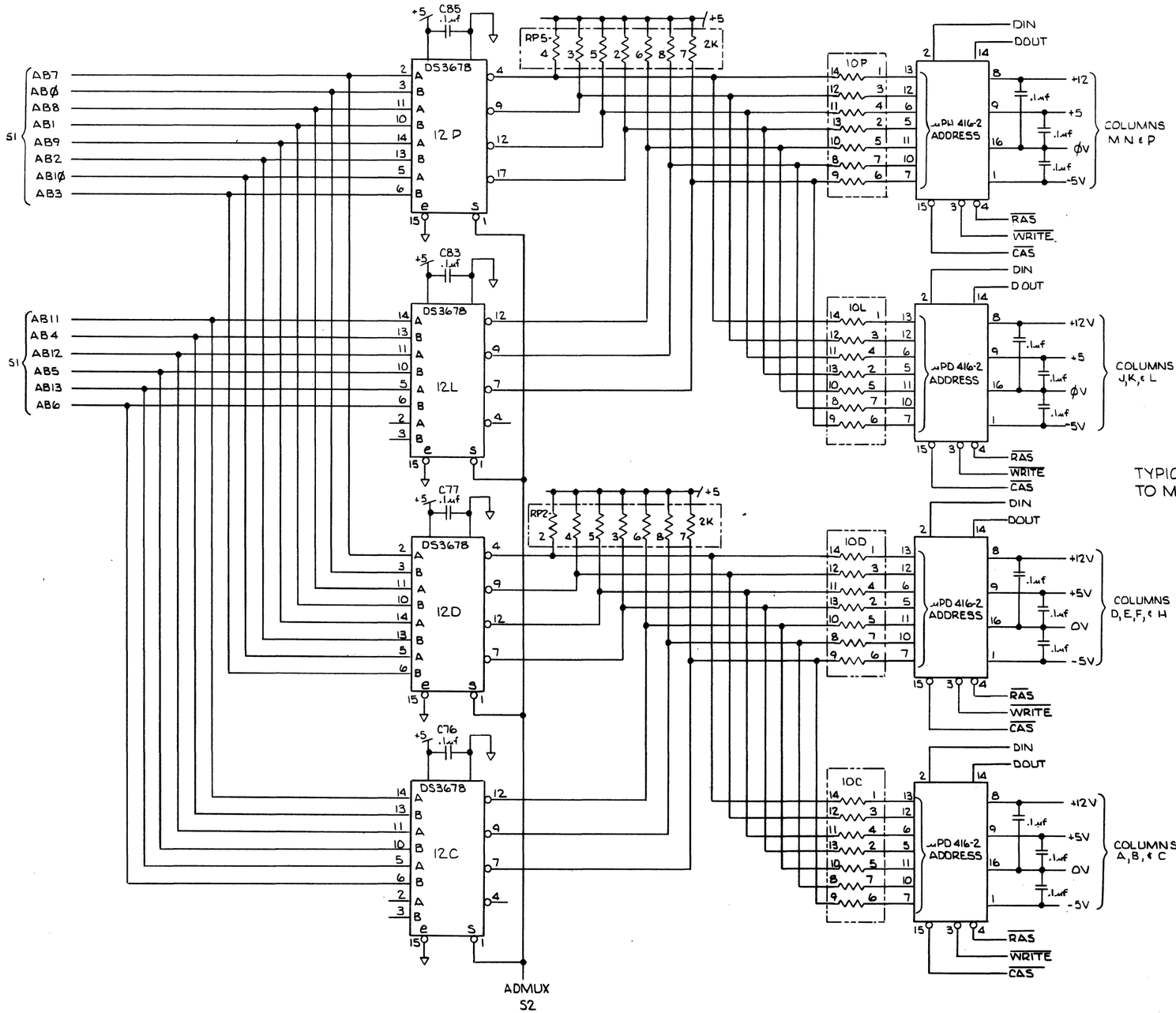
ALTOS COMPUTER SYSTEMS

APPROVALS	DATE
DRAWN C.R.	1/30/81
CHECKED	

SCALE —— SIZE D DRAWING NO. 625-11243-001 4

DO NOT SCALE DRAWING SHEET 2 of 8

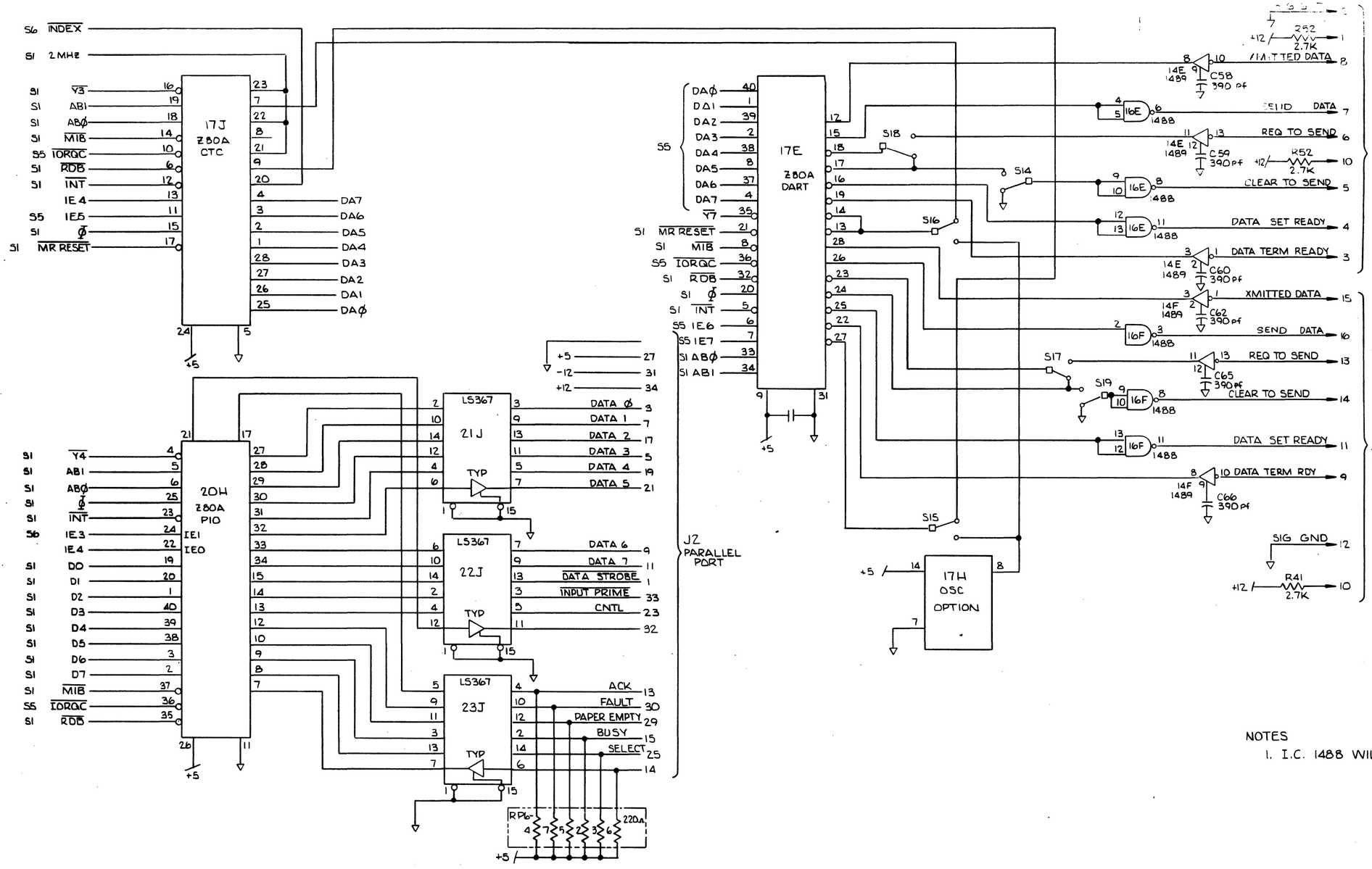
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TYPICAL CONNECTIONS
TO MEMORY CHIP

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		ALTOS COMPUTER SYSTEMS	
APPROVALS	DATE		
DRAWN C. R.	11/21/81		
CHECKED		SCALE —	SIZE D DRAWING NO. 625-11293-001 4
		DO NOT SCALE DRAWING	SHEET 3 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES

1. I.C. 1488 WILL HAVE PIN 1 TO -12 AND PIN 14 TO +12

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	ALTOS COMPUTER SYSTEMS		
APPROVALS	DATE		
DRAWN G.R.	1/12/81		
CHECKED		SCALE —	SIZE D
		DRAWING NO. 625-11293-001	4
		DO NOT SCALE DRAWING	SHEET 4 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

S1 2.MHz

DA7 DA6 DA5 DA4 DA3 DA2 DA1 DAØ

DBØ DB1 DB2 DB3 DB4 DB5 DB6 DB7

+5 C27 .1uf

21L LS241

S2 JUMPER

+5 C30 .1uf

21M LS241

S3 JUMPER

11E 74LS 193

2Ø

13C LS74

R38 10K

20L Z80A CTC

YI2 ABØ ABI MIB IORQ RDB Ø MR RESET INT IE5 IE6

S1 GTRD

LS02 16L

LS21 15L

LS08 14L

YI0 S1 LS08

YI1 S1

YI2 S1

YI3 S1

IORD

MIB S1

IORQC

IE4 S4

S1 IPLW

S6 PAUSE

S1 IORQB

LS32 15La

LS04 16La

DN/UP LD 17L LS191

S1 MIB

S1 Ø

WAIT S1

IORQC S1,4,6

S8 EXT WAIT

DAØ DA1 DA2 DA3 DA4 DA5 DA6 DA7 S1 YI1 S1 MR RESET S1 MIB S1 IORQC S1 RDB S1 RØ S1 INT IE5 S1 ABØ S1 ABI S1 SIORDY

17C Z80A SIO/0 W/RDVA

C56 .1uf

TxDA RxDA RxCA TxCA RTS CTS DCD DTR

S11 S12

17A Z80A SIO/0

S4 IE7 IE8 S1 ABØ S1 ABI

C39 .1uf

BDRT

S8 S9 S10 S5 S6 S7

AM26LS32 AM26LS531 LS31

S20 R36 200Ω S28 S23 R37 200Ω S24

DATA + DATA - CLOCK + CLOCK-

J W NET 1

SIG GND

XMITTED DATA RECEIVED DATA REQ TO SEND CLEAR TO SEND IO DATA TERM RDY DATA SET RDY

R39 2.7K C52 390pf C51 390pf C55 390pf

J6 TO JY CONSOLE #2

IO XMITTED DATA RECEIVED DATA REQ TO SEND CLEAR TO SEND DATA TERM RDY DATA SET READY SIG GND

C57 390pf C53 390pf C47 390pf R40 2.7K

J6 TO JU CONSOLE #3

C54 390pf C43 390pf C41 390pf

REQ TO SEND CLR TO SEND XMITTED DATA RECEIVED DATA DATA SET RDY DATA TERM RDY

C44 390pf C42 390pf R34 2.7K

J6 TO JV PRINTER #2

C50 390pf C45 390pf C49 390pf R35 2.7K

J6 TO JZ CONSOLE #4

TOLERANCES UNLESS OTHERWISE SPECIFIED			ALTOS COMPUTER SYSTEMS		
FRACTIONS DEC ANGLES					
± ± ±					
APPROVALS	DATE				
DRAWN C.M.R.	1/29/81				
CHECKED		SCALE ——	SIZE D	DRAWING NO. 625-11293-001	49
		DO NOT SCALE DRAWING		SHEET 5 OF 8	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	ALTOS COMPUTER SYSTEMS		
APPROVALS	DATE		
DRAWN C.R.	1/20/81		
CHECKED		SCALE ——	SIZE D
		DRAWING NO. 6Z5-11243-001	
		DO NOT SCALE DRAWING	SHEET 6 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

S6 $\overline{VFOE}$

S1 ½MHz

S1 1 MHz

S6 $\overline{RAW\ READ}$

CLK A

CLK B

S6 DDEN

$\overline{RCLK}$ S6

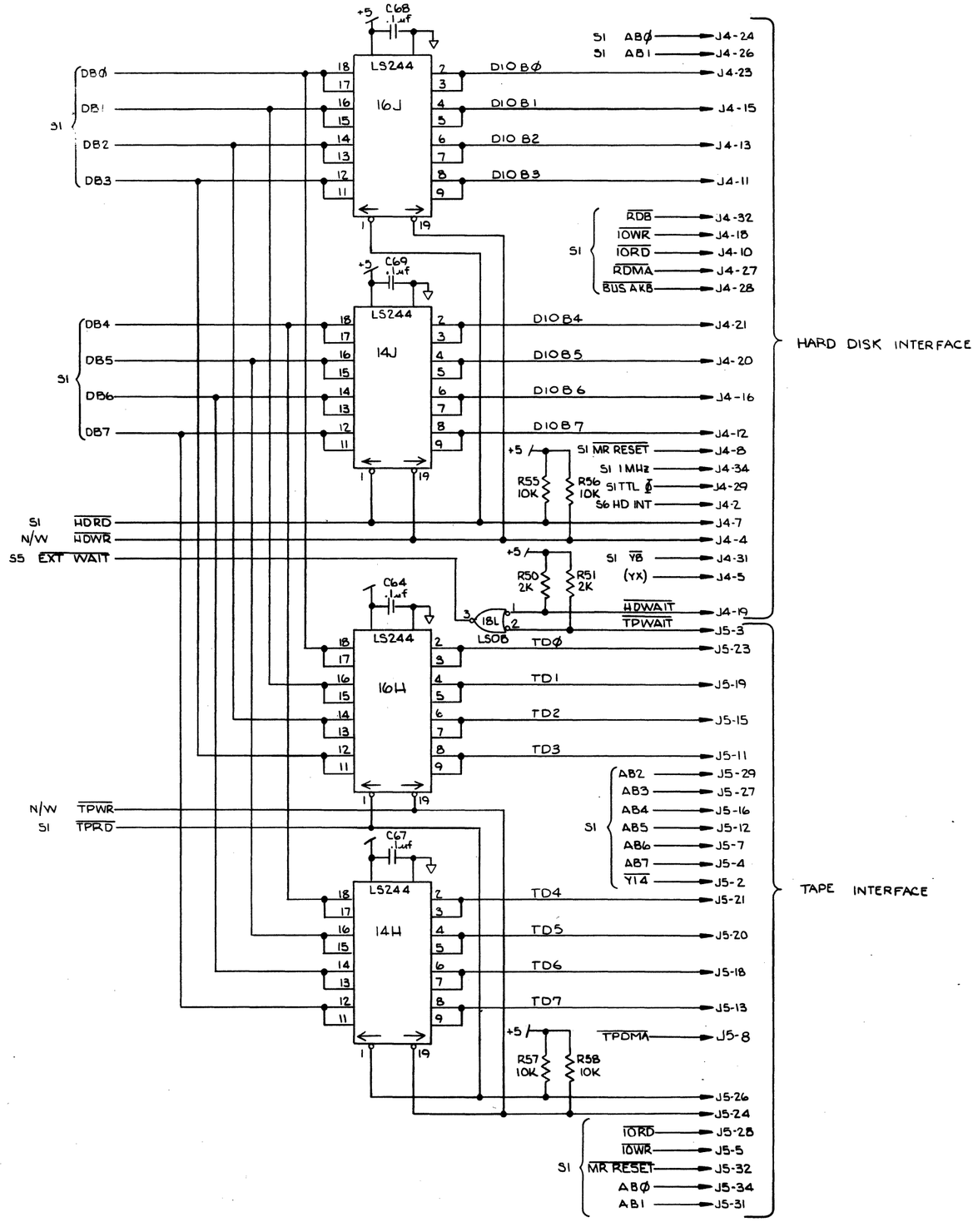
CLK A (FM)

CLK B (MFM)

$\overline{RD\ DATA}$ S6

TOLERANCES UNLESS OTHERWISE SPECIFIED			ALTOS COMPUTER SYSTEMS
FRACTIONS ±	DEC ±	ANGLES ±	
APPROVALS	DATE		
DRAWN C.M.	3/81		
CHECKED		SCALE —	SIZE D DRAWING NO. 8105-11243-001 G
		DO NOT SCALE DRAWING	SHEET 7 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED			ALTOS COMPUTER SYSTEMS		
FRACTIONS ±	DEC ±	ANGLES ±			
APPROVALS	DATE				
DRAWN C.R.	1/20/81				
CHECKED			SCALE —	SIZE D	DRAWING NO. 625-11283-001
			DO NOT SCALE DRAWING		SHEET 3 of 5

EIGHT-INCH HARD DISK CONTROLLER SCHEMATICS

DWG. NO.	SH	REV.
625-11125-001	1	2

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

O87
O86
O85
O84
O83
O82
O81
O80

LS244 2A

LS244 3A

J4-23 DIOB-0
J4-15 DIOB-1
J4-13 DIOB-2
J4-11 DIOB-3
J4-21 DIOB-4
J4-20 DIOB-5
J4-16 DIOB-6
J4-12 DIOB-7
J4-7 HDRD

J4-10 IORD
J4-31 Y8
J4-18 IOWR
LS14

J4-24 AB0
J4-26 AB1
J4-4 HDWR
LS04

IC ½ LS139

9 LD DR/HD
10 LD SECT/OLD CYL/ DATA
11 LD NEW CYL
12 LD COMMAND

TOP
STAT

1B0
1B1
1B2
1B3
1B4
1B5
1B6
1B7

NHRD

LS273 9A

ENREF OSC
SEEK
RECAL
12 REZERO
9 RESET HD
HDRDY
BADB

LS273 8D

RD
WR
FRM
SEN REF OSC
SHDRDY
DMA BSY
MR FIFO
STBZ
CLR CMD REG
PLO CLK B

LS273 8A

RST

LS374 7A

COMP SECT

LS273 6A

LS374 6B

SEEK
COMP CYL

LS74 6C

PL

CB0 1 2 3 4 5 6 7

LS244 7B

e1 e2

COMP HD

LS85 5C
LS85 4C
LS85 3C

A=B

STEP IN

LS191 5B
LS191 4B
LS191 3B

STEP

LS273 4A

1B0
1B1
1B2
1B3
1B4
1B5
1B6
1B7

Q
S
S1B
S1A

R7 4.7K

LS00

EN COMP

7438

DS1 J1-26
DS2 J1-28
HS0 J1-14
-HS1 J1-18
-HS2 J1-4
-HS3 J1-
REZERO J1-6
UNSAFE J1-46 CLEAR

R8 4.7K

S288 8B 'SBP2' (#10572)

CB0
CB1
CB2
CB3
CB4
CB5
CB6
CB7

E0
E1
E2
ENSBP

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION 'SPECIFICATION	ITEM
								3
								2
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √

TOLERANCE
DIMENSIONAL: X ± 1; XX ± .030 ±1°; XXX ± .010
ANGLES
HOLE SIZE: 0-500 ± .003; 500-1000 ± .004; 1.000-1.499 ± .005
BEND RADIUS
FINISH

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	DATE 10-25-81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSUR	

ALTOS COMPUTER SYSTEMS

TITLE: SCHEMATIC 8" CONTROLLER VERSION 2

SCALE	SIZE	PART NUMBER	REV
—	D	625-11125-001	2

CODE — SHEET 1 OF 5

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1216

DWG. NO. 625-11125-001 | SH 2 | REV 2

REVISIONS

DESCRIPTION	DATE	APPROVED

J4-Z INT

OB0 OB1 OB2 OB3 OB4 OB5 OB6 OB7

12A LS244

4 TASK COMPLETE
6 BAD SECT
8 REC NOT FOUND
17 CRC ERR
15
13 WR FAULT
11 RDY

STAT

17A LS14 — 14A LS02 — WORR

15B — 16E LS74 (CLK D PR CLR Q)

SC — 16C LS08 — 16A LS74 (PR D Q CLR Q)

REZERO — 16D LS32

CLRC — 16A LS74 (PR D Q CLR Q)

PLO CLK A — 15A LS08

15B LS04 — L2 22 mh — R2 470Ω — C5 30 pf

CLR STATUS — 16C LS08 — CLR CMD REG — RST

RESET HD — 14A LS02

J4-8 MR RESET — 15B LS04

HD READY

SC — 15C LS00 — 14A LS02

READY — 15C LS00

SEEK — 16D LS32

RDY — 16E LS74 (PR D Q CLR Q)

RECAL — 17F LS00

TRK Ø — 17F LS00 — 17F LS00

A=B — 17F LS00 — 16C LS08

16D LS32

STEP IN — 16F LS74 (PR D Q CLR Q)

STEP — 15B LS04

15E LS193 (CPU CPD PL Q1 Q2 Q3 MR D0 D1 D2 D3)

J4-34 1 MHZ

MFM WRITE DATA — 17C 75110

TIMING CLK — 17D 75110

RIB 1K

RP1 18E — 47Ω

17E — MFM DATA 1

17E — MFM DATA 2

MFM DATA — 14E LS00 — 17E 75107A — 17E 75107A

17B LS14 — -DRIVE 1 SELECTED

17B LS14 — -DRIVE 2 SELECTED

IMK — 17A LS14 — -INDEX

READY — 17A LS14 — -READY

TRK Ø — 17B LS14 — -TRACK Ø

SC — 17A LS14 — -SEEK COMP

WRITE FAULT — 17B LS14 — -WRITE FAULT

16B 7438 — -DIRECTION IN

16B 7438 — -STEP

R1 4.7K — EN COMP — 16B 7438 — -REDUCED WRITE CURRENT

WR GATE — 16B 7438 — -WRITE GATE

R5 75Ω — R4 1K — Q1 2N3906 — CR1 IN7474 (3.6V ± 5%) — R6 510Ω

RPAC 18B — 220/330

J2-13 J2-14 MFM WRITE DATA
J2-9 J2-10 TIMING CLK
J3-13 J3-14 MFM WRITE DATA
J3-9 J3-10 TIMING CLK
J2-17 J2-18 MFM DATA 1
J3-17 J3-18 MFM DATA 2

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								3
								2
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √
TOLERANCE
DIMENSIONAL X ± .1 ANGLES XX ± .020 ±1° XXX ± .010
HOLE SIZE 0-.300 ± .003 .300-.999 ± .004 1.000-1.499 ± .005
BEND RADIUS
FINISH

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

DRAWN CK Ramaswamy — DATE 10-25-81
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSUR

ALTOS COMPUTER SYSTEMS

TITLE SCHEMATIC 8" CONTROLLER VERSION 2

SCALE — | SIZE D | PART NUMBER 625-11125-001 | REV 2

CODE | SHEET 2 OF 5

1:45

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A14216

625-11125-001 3 2

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

LS175 1D 14 Q 13 — LS175 1D 10 Q D 12

MR FIFO
WR
FRM
BAOB
J4-28 BUSAKB
DMARQ
J4-27 RDMA
S3
J4-29 Ø
J4-32 RDB
TOP
PL

2E LS74 PR CLR Q D

2D LS04 — 3D LS02 — 10D LS00

L3 22 mh — R9 470Ω — C7 30 pf

P1-1 P1-2 P1-3 P1-4 P1-5 P1-6
+5 +12
C2 10uf
VR1 LM320 -12 -5
C3 10uf — C1 10uf

NRZ CLK
IB0 IB1 IB2 IB3 IB4 IB5 IB6 IB7

9403 11A — 9403 10A
PL TTS IES OES TOS TOP DO D1 D2 D3 D4 D5 CPSI MR IRF ORE CPSO EO Q0 Q1 Q2 Q3 Q4 Q5

OB7 OB6 OB5 OB4 OB3 OB2 OB1 OBØ

LS299 13B — 25LS2521 12B — 25LS2521 10B
IN SR SL G1 G2 A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 OUT

NRZ DATA
CB Ø CB 1 CB 2 CB 3 CB 4 CB 5 CB 6 CB 7
EØ — 15A — LSØ8 BSF
B MATCH
COMP HD — 9C LSØ8
PLO CLK A
ENCPST

S02 11C
ENCPCRC — S02 11C

S51 10C — WRITE DATA
LS04 2D
S51 10C — S02 11C — CWE
9401 9D — PR CRC
WR GATE — LS04 15B
SEN CRC CHK
LSØØ 10D
CLR STATUS
11D LS74 PR CLR
PLO CLK A
CRC ERR
EN CPSO — S02 11C

								3
								2
								1
-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √
TOLERANCE
DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ±1°; XXX ± .010
HOLE SIZE: 0-.199 ± .003; .200-.999 ± .004; 1.000-1.499 ± .005
BEND RADIUS
FINISH

DRAWN — DATE
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSUR

DASH NO. | NUMBER | NEXT ASSEMBLY | QTY

ALTOS COMPUTER SYSTEMS

TITLE: SCHEMATIC 8" CONTROLLER VERSION 2

SCALE	SIZE	PART NUMBER	REV
—	D	625-11125-001	2

CODE — SHEET 3 OF 5

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A14218

8 7 6 5 4 3 2 1

625-11125-001 | 4 | 2

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

PLO CLK B
B MATCH
STB Z
DMA BUSY
BAD SECT
CRC ERR
SHD RDY
IP
WR
RD
FRM
EN CRC CHK
CLRC
R35 4.7K
RST
BAD SECT
BSF
PLO CLK B
IMK
STATE Ø
CLR STATUS
COMP CYL
PLA 825100 6D (#11158)
INCREMENT
JUMP
LOAD COUNTER
CLRS
CLRC
EN BAD SECT CHK
WORR
LS32
LS00
LS08
LS74 8F
LS74 8E
LS191 8F
RECORD NOT FOUND
LS163 6F
LS163 7F
S288 4E CP22 (#10574)
S288 5E CP12 (#10573)
S288 6E "JAP 2" (#10575)
S288 3E CLP 3 (#11157)
CWE
COMP CYL
COMP HD
COMP SECT
ENCPCRC
EN REF OSC
EN SBP
EN CP50
EN CP51
EØ
E1
E2
R34 4.7K
S2
256
512
LS273 4D
EN CRC CHK
EØ
IMK
SEN CRC CHK
PRCRC
EN SYNC DET
SEØ
WR GATE
STATE Ø
IP
DMARQ
PLO CLK B
EN
R FIFO
NHRD
LOAD COUNTER
LS163 2F
LS163 3F
LS163 4F
LS163 5F
SI

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			3
			2
			1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √
TOLERANCE
DIMENSIONAL: X ± .1 ANGLES; XX ± .030 .5°; XXX ± .010
HOLE SIZE: 0-.599 ± .003; .600-.999 ± .004; 1.000-1.499 ± .005
BEND RADIUS

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

FINISH

DRAWN: Thompson 10-25-81
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSUR

ALTOS COMPUTER SYSTEMS

TITLE: SCHEMATIC 8" CONTROLLER VERSION 2

SCALE: — SIZE: D PART NUMBER: 625-11125-001 REV: 2

CODE: SHEET 4 OF 5

BISHOP GRAPHICS/ACCUPRESS REORDER NO A14216

DWG. NO.	SH.	REV.
625-11125-001	5	2

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

SYNC FIELD DETECTOR

R14 1K 1% R15 500Ω C10 30pf 14D 96S02 57.5ns CLR

MFM DATA

VPU 1

R21 R20

VPU 2 VPU 1

R17 1K 1% R16 500Ω C11 330pf 13D 278ns 96S02 CLR

VPU 1

EN SYNC DET

11D LS74 PR CLR

LS193 13E CEP CET PE CU CLR TC

TBZ

14E S00

R11 1.15K 1% C8 5% 100pf 103ns 14D 96S02 CLR

MFMRD

9E OSC 8.68 MHZ K1115

10F S74 PR CLR

15D LS393 CLR

TIMING CLK

SEN REF OSC

7E LS00

9F S51

VPU 2

12F S74 PR CLR

R32 5K R28 100K C16 100pf 5% R30 680Ω C17 .01uf 5%

PHASE LOCKED OSCILLATOR

CR3 IN4148 R27 3.92K 1%

L4 22uh C15 47uf / 6V

R23 1K 1% C14 .1uf R24 1K 1% R22 4.7K

CR2 IN4148 R31 3.92K R29 100Ω Q2 ZN2222 Q3 2N2222 R26 20K CR4 IN4148

11F S00

15F S124 FC CEXT CEXT RNG EN OUT

C12 30 pf 5%

R25 10K 1% C13 .1uf

PHASE COMPARATOR

2 PLO

VPU 2

SEØ

13A LS74 PR CLR D Q

SET PHASE OF PLO

VPU 1

10E S112 PR CLR J K

11E S112

12E S112

NRZ DATA

MFM TO NRZ DECORDER (DATA SEPARATOR)

PLO CLK A

A1 BYTE

VPU-2

VPU 3

R19

ENPL

S1

CB Ø CB 1 CB 2 CB 3 CB 4 CB 5 CB 6 CB 7

9B LS299 SI SO CLR G1 G2 SR SL QH

R33 4.7K

NRZ TO MFM ENCODER

14B PAL 16R4 (# 10571)

EARLY NORM LATE MFM OUT EN

S04

13C S64

10E S112

11F S112

12E S112

NRZ CLK

R10 1K 1% C9 100pf 13D 96S02 100ns CLR

PLO CLK B

PLO CLK A

WRITE DATA

WR GATE

EN COMP

R12 180Ω R13 240Ω

20 DELAY

12C

WR GATE

MFM WR DATA

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								3
								2
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √

TOLERANCE

DIMENSIONAL X ± .1 ANGLES XX ± .020 ±1° XXX ± .010

HOLE SIZE 0-599 ± .003 600-999 ± .004 1.000-1.499 ± .005

BEND RADIUS

FINISH

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSUR	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

ALTOS COMPUTER SYSTEMS

TITLE: SCHEMATIC 8" CONTROLLER VERSION 2

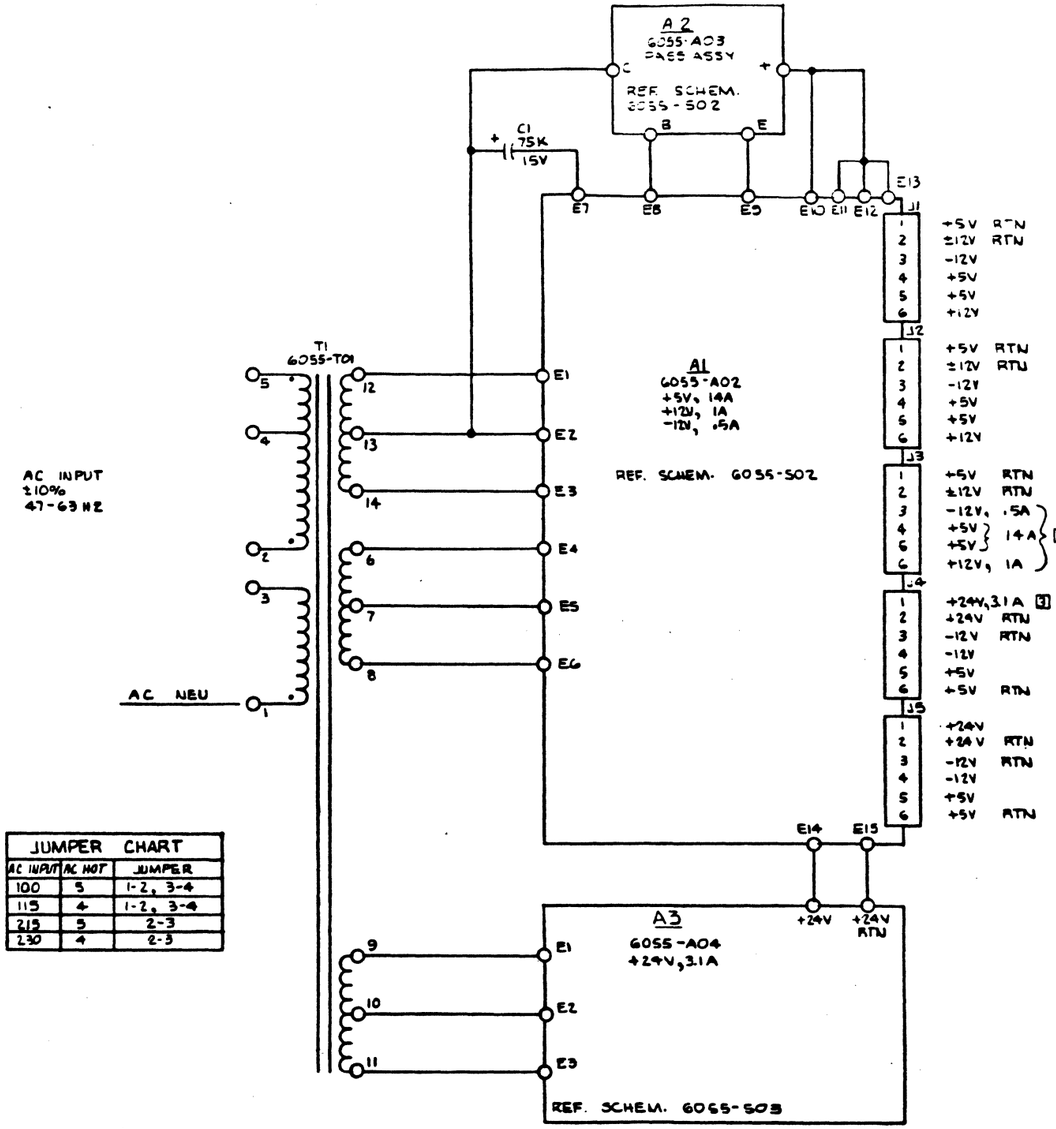
SCALE	SIZE	PART NUMBER	REV
~	D	625-11125-001	2

CODE SHEET 5 OF 5

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A14218

XENTEK POWER SUPPLY SCHEMATICS

REVISIONS				
REV	BY	DESCRIPTION	APPR	DATE
A	BE	INITIAL RELEASE	E	1-6-80



JUMPER CHART		
AC INPUT	AC HOT	JUMPER
100	5	1-2, 3-4
115	4	1-2, 3-4
215	5	2-3
230	4	2-3

3 TOTAL CURRENT SUPPLIED BY ALL CONNECTORS.
2. ALL CAPACITANCE VALUES IN MICROFARADS
1. REF. DOCUMENTS: 6055-801, 6055-502, 6055-503

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQ'D	DESCRIPTION	PART NO.	MATERIAL	MANUFACTURER	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRAC. ±1/32 DEC. .XX ±.05 .XXX ±.010 ANGLES ±1/2°

SIGNATURES	DATES
DWN. [illegible]	12-18-80
CHK.	
DSGN.	
ENGR. A. Hightower	12/19/80
APPR. A. Peterson	12/19/80

MATERIAL:
FINISH:

PROPRIETARY NOTICE
ALL PATENT OR OTHER PROPRIETARY RIGHTS PERTAINING TO THE ITEMS SOLD HEREUNDER SHALL REMAIN THE SOLE PROPERTY OF XENTEK INCORPORATED EXCEPT THAT THE PURCHASER SHALL HAVE THE RIGHT TO USE SUCH ITEMS FOR THE INTENDED PURPOSE

DO NOT SCALE DWG

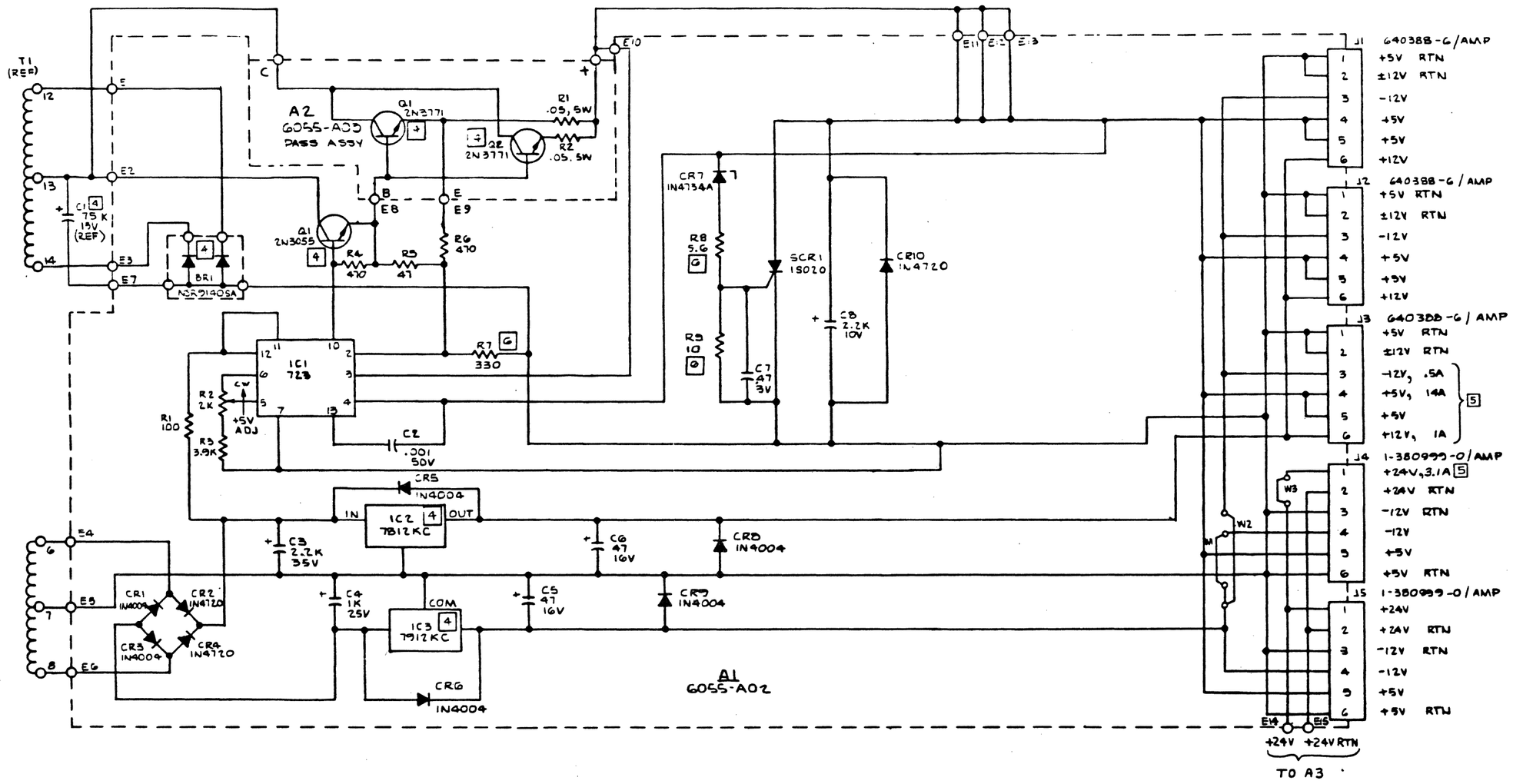
XENTEK INCORPORATED
San Marcos, California

TITLE
POWER SUPPLY SCHEMATIC
(ALTOS COMP)

CODE IDENT	SIZE	DWG NO.	REV.
53279	D	6055-S01	A

SCALE: NONE | WEIGHT: ~ | SHEET 1 OF 1

REVISIONS				
REV.	BY	DESCRIPTION	APPR.	DATE
-	DZ	INITIAL RELEASE	[illegible]	[illegible]
A	DZ	REVISED. ADDED CONNECTORS J1-J5	[illegible]	[illegible]



6055-S02 | A

QTY REQ'D	DESCRIPTION	PART NO.	MATERIAL	MANUFACTURER	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRAC. ±1/32 DEC. .XX ±.02 .XXX ±.010 ANGLES ±1/2°

SIGNATURES	DATES
DWN. B Zielke	10-6-80
CHK.	
DSGN.	
ENGR. A. Peterson	10 OCT
APPR. A. Peterson	80

MATERIAL:
FINISH:

PROPRIETARY NOTICE
ALL PATENT OR OTHER PROPRIETARY RIGHTS PERTAINING TO THE ITEMS SOLD HEREUNDER SHALL REMAIN THE SOLE PROPERTY OF XENTEK INCORPORATED EXCEPT THAT THE PURCHASER SHALL HAVE THE RIGHT TO USE SUCH ITEMS FOR THEIR INTENDED PURPOSE
DO NOT SCALE DWG

XENTEK INCORPORATED
San Marcos, California

TITLE
REGULATOR SCHEMATIC (ALTOS COMPUTER)

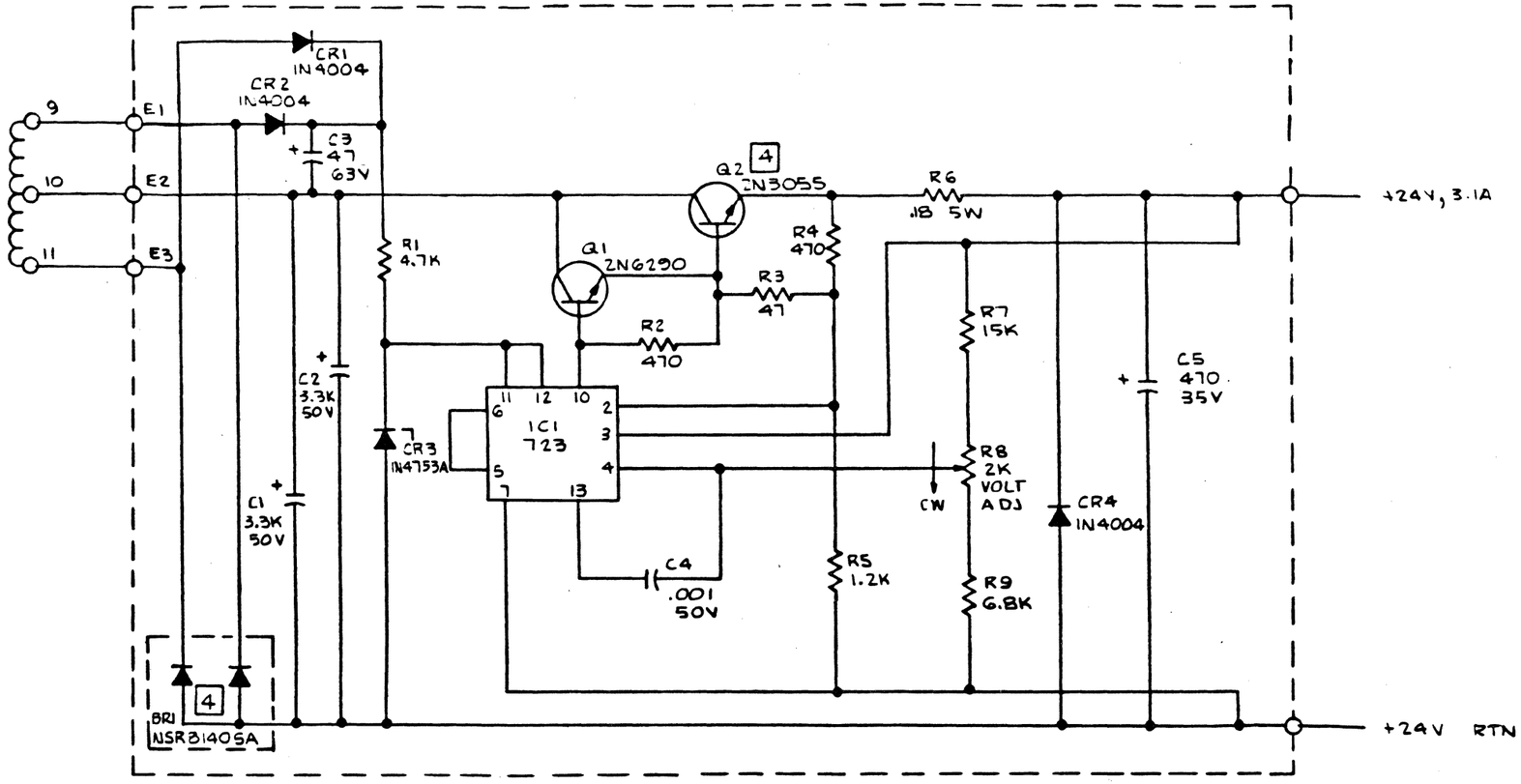
CODE IDENT	SIZE	DWG. NO.	REV.
53279	D	6055-S02	A

SCALE: NONE | WEIGHT: ~ | SHEET 1 OF 1

[6] COMPONENT TEST SELECT
[5] TOTAL CURRENT SUPPLIED BY ALL CONNECTORS.
[4] COMPONENT MOUNTED ON HEATSINK OR CHASSIS.
3. ALL RESISTANCE VALUES IN OHMS ±5% 1/2W.
2. ALL CAPACITANCE VALUES IN MICROFARADS.
1. REF. DOCUMENTS: 6055-B02, 6055-B03, 6055-S01.

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS			
REV.	BY	DESCRIPTION	APPR. DATE
NC	BZ	INITIAL RELEASE	



4. COMPONENT MOUNTED ON HEATSINK
3. ALL RESISTANCE VALUES IN OHMS ±5%, 1/2W.
2. ALL CAPACITANCE VALUES IN MICROFARADS.
1. REF. DOCUMENTS: 6055-B04, 6055-S01.

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQ'D	DESCRIPTION	PART NO.	MATERIAL	MANUFACTURER	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
FRAC. ±1/32 DEC. .XX ±.02 .XXX ±.010 ANGLES ±1/2°

MATERIAL:

FINISH:

SIGNATURES	DATES
DWN.	2-5-80
CHK.	
DSGN.	
ENGR.	18
APPR.	31

DO NOT SCALE DWG.

XENTEK INCORPORATED
San Marcos, California

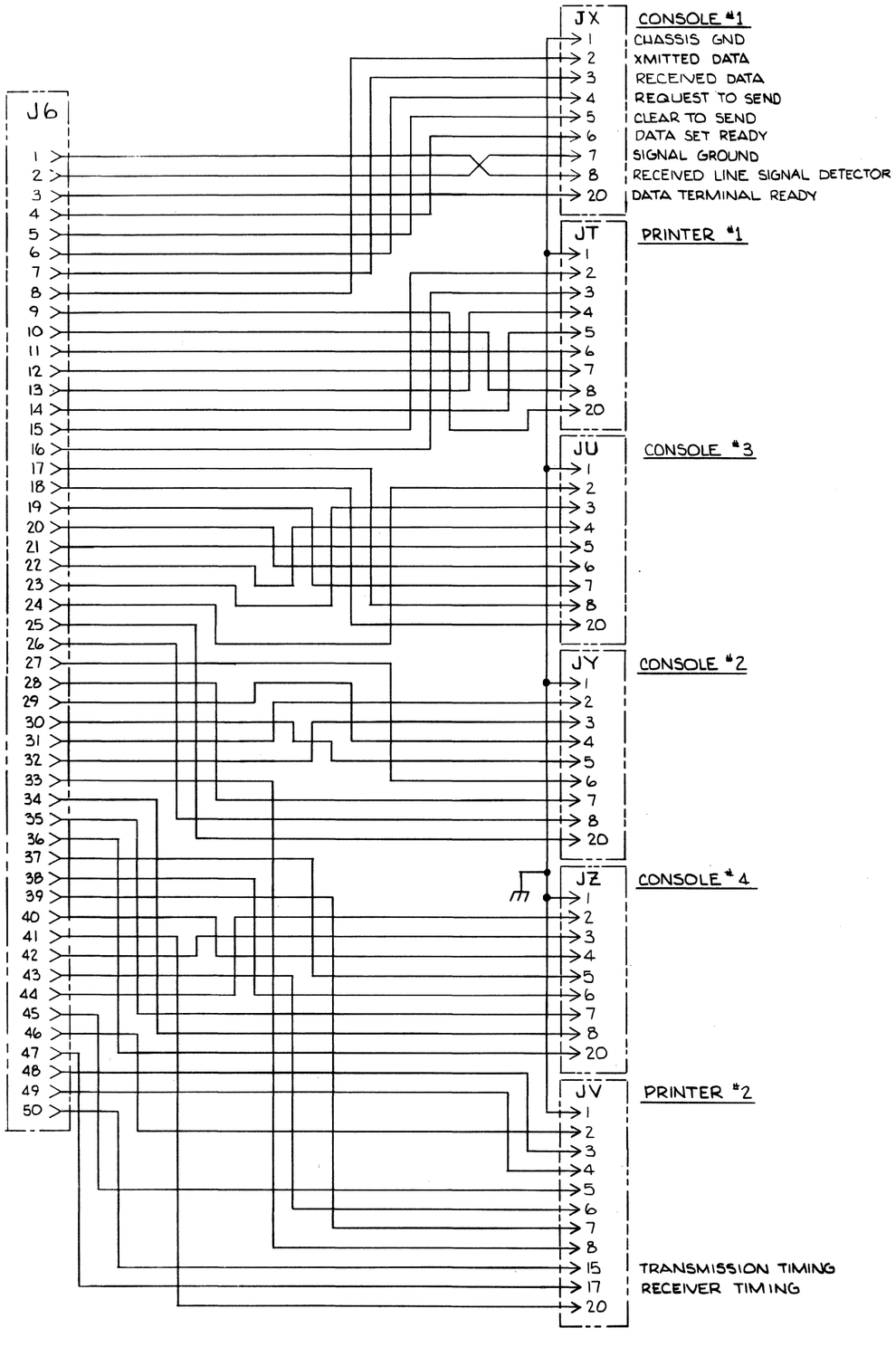
TITLE
REGULATOR SCHEMATIC
(ALTOS)

CODE IDENT	SIZE	DWG. NO.	REV.
53279	C	6055-S03	NC

SCALE: NONE WEIGHT: ~ SHEET 1 OF 1

6055-S03 NC

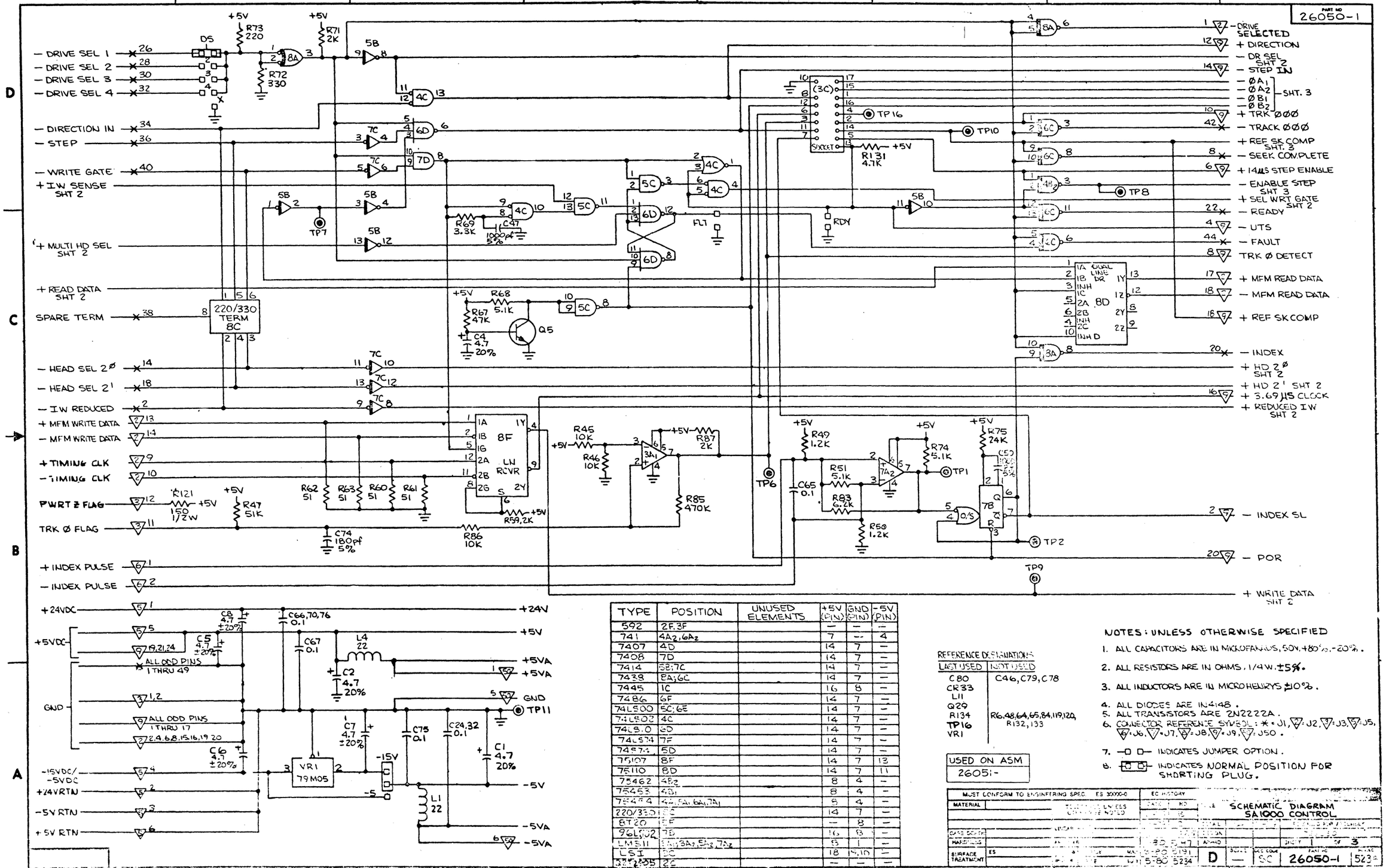
REAR PANEL I/O PCB SCHEMATIC



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	ALTOS COMPUTERS
APPROVALS / DATE	SCHEMATIC, I/O PCB
DRAWN M.SCHMELZER	SCALE ~ / SIZE D / DRAWING NO. 8500-0016 A
CHECKED	DO NOT SCALE DRAWING / SHEET 1 OF 1

SHUGART SA1000 SCHEMATICS



TYPE	POSITION	UNUSED ELEMENTS	+5V (PIN)	GND (PIN)	-5V (PIN)
592	2F,3F		—	—	—
741	4A2,6A2		7	—	4
7407	4D		14	7	—
7408	7D		14	7	—
7414	5B;7C		14	7	—
7438	8A;6C		14	7	—
7445	1C		16	8	—
7486	6F		14	7	—
74LS00	5C;6E		14	7	—
74LS02	4C		14	7	—
74LS.0	6D		14	7	—
74LS74	7F		14	7	—
7497..	5D		14	7	—
75107	8F		14	7	13
75110	8D		14	7	11
75462	4B2		8	4	—
75463	4B1		8	4	—
7545.4	4A1,5A1,6A1,7A1		5	4	—
220/330	8C		14	7	—
8T20	8E		—	8	—
96LS02	7B		16	8	—
LM311	5A1;3A2,5A2,7A2		5	1	—
LSI	8C		18	9,10	—
555	2C		—	—	—

REFERENCE DESIGNATIONS

LAST USED	NOT USED
C80	C46,C79,C78
CR33	
L11	
Q29	
R134	R6,48,64,65,84,119,120, R132,133
TP16	
VR1	

USED ON ASM
2605i-

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80%, -20%.
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
3. ALL INDUCTORS ARE IN MICROHENRYS ±10%.
4. ALL DIODES ARE IN4148.
5. ALL TRANSISTORS ARE 2N2222A.
6. CONNECTOR REFERENCE SYMBOL: * = J1, 2 = J2, 3 = J3, 5 = J5, 6 = J6, 7 = J7, 8 = J8, 9 = J9, 50 = J50.
7. —□ D— INDICATES JUMPER OPTION.
8. INDICATES NORMAL POSITION FOR SHORTING PLUG.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0

EC HISTORY

SCHEMATIC DIAGRAM SA1000 CONTROL

SIZE	CODE IDENT NO	PART NO	REV
D	SC	26050-1	523

SCALE — SHEET 1 OF 3

PART NO 26050-1

+HD 2^8 SHT 1
+HD 2^1 SHT 1
-DR SEL SHT 1
IC BCD/DEC
+24V
L5 22
R32 240
R28 10K
R29 10K
R30 10K
R31 10K
C33 0.1
R26 100
Q11 2N2907A
C3 4.7 80%
C34 0.1
R27 390
2C
CR15 IN5248B 5.1V
R39 4.7K
R38 1K
R25 430
C9 1.0
R66 2K
+5V
R70 2K
R41 3K
R40 430
R23 274 1/8W 1%
R24 274 1/8W 1%
R22 909 1/8W 1%
R35 68
R36 68
R43 2K
R44 6.2K
+SEL WRT GATE SHT 1
Q6
CR17
CR16
R42 510
R34 2.2K
R33 2.2K
R37 4.7K
+WRITE DATA SHT 1
+REDUCE IW SHT 1
5D
4D
R21 10K
R20 10K
-5VA
CR13
+HEAD Ø
-HEAD Ø
+HEAD 1
-HEAD 1
+HEAD 2
-HEAD 2
+HEAD 3
-HEAD 3
CR8
CR7
CR6
CR5
CR4
CR3
CR2
CR1
CR14
CR9
CR10
+5VA
C30 0.1
Q2
R2 5.1K
R7 2K
CR12
C31 0.1
CR11
TP12
R4 2K
R3 5.1K
R1 430
Q1
C29 0.1
R5 10
C73 .047 50V ±10%
C28 0.1
R8 453 1/8W 1%
L8 10
L9 15
R9 453 1/8W 1%
L6 10
L7 15
C27 120pf 50V 5%
C26 18pf 50V 5%
Q4
C23 .01 10%
R14 1K
R15 1K
R10 909 1/8W 1%
R11 1K
R12 1K
C25 .01 10%
Q3
C21 0.1
R13 36
C20 0.01 10%
C19 0.01 10%
C18 0.1
C22 100pf 50V 5%
L10 56
L11 56
TP3
TP4
TP14
R17 768 1/8W 1%
R16 768 1/8W 1%
R18 2K
C16 18pf
R19 5.1K
C17 0.1
L3 22
L2 22
C15 0.1
C32 15pf 50V 5%
+LINEAR (TP1)
-LINEAR (TP2)
+MULTI HEAD SEL SHT 1
-HEAD C.T. Ø
-HEAD C.T. 1
-HEAD C.T. 2
-HEAD C.T. 3
+I'W SENSE SHT 1
R58 2K
R56 2K
R57 2K
R134, 1K
6F
6E
7B
7F
TP5
+READ DATA SHT 1

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR
CASE DEPTH
HARDNESS
SURFACE TREATMENT
EC HISTORY
DATE
NO
TITLE SCHEMATIC DIAGRAM SA1000 CONTROL
DETAIL
DESIGN
APPRO
RELEASED FOR ASSEMBLY
SIZE D
SCALE —
SHEET 2 OF 3
PART NO SC 26050-1 5234

PART NO 26050-1

-ØA2 (23)
-ØA2 SHT 1
-ØA1 (22)
-ØA1 SHT 1
-ØB1 (25)
-ØB1 SHT 1
-ØB2 (26)
-ØB2 SHT 1
-ENABLE STEP SHT 1
+REF SK COMP SHT 1

+5V
+24V
-5V

Q29 TIP34
R100 510
C77 4.7 20%
R128 39 1/2W
R52 2K
CR22 IN5625
CR33 IN4003
Q16 TIP32
R103 510
R104 1K
Q14 2N2907A
R115 180
R116 180
R112 510
Q21 TIP32
Q17 TIP31
R125 51 1/2W
CR31 IN4003
CR29 IN4003
Q22 TIP32
R111 510
Q18 TIP31
R107 51K
R91 510
Q10
R126 39 1/2W
Q27 TIP33
R90 510
CR19
CR18
CR30 IN4003
CR28 IN4003
R124 51 1/2W
Q9
R93 510
Q28 TIP33
R127 39 1/2W
R92 510
R53 10 K
R94 200
R89 510
C64 1200pf 5%
R54 10K
R117 0.4 3W 1%
TP15
R88 330
C11 1.0
C60 0.1
C59 0.1
R79 4.3k
R80 510
CR2 0.1
C51 0.1
CR23 IN5625
CR32 IN4003
Q15 TIP32
R101 510
R102 1K
Q13 2N2907A
R113 180
R114 180
R110 510
Q23 TIP32
Q19 TIP31
R123 51 1/2W
CR27 IN4003
CR25 IN4003
Q24 TIP32
R109 510
Q20 TIP31
R108 5.1K
R97 510
Q8
R129 39 1/2W
Q26 TIP33
R96 510
CR21
CR20
CR26 IN4003
CR24 IN4003
R122 51 1/2W
Q7
R99 510
Q25 TIP33
R130 39 1/2W
R98 510
R55 10 K
R95 200
R105 510
C55 1200pf 5%
R82 10K
R118 0.4 3W 1%
R106 330
C10 1.0
C63 0.1
C61 0.1
R81 2K
Q12 2N2907A
R78 510
R76 510
R77 5.6K
C62 0.1

10 (3) A1
9 (3) A1
8 (3) A2
7 (3) A2
6 (3) B2
5 (3) B2
4 (3) B1
3 (3) B1

MUST CONFORM TO ENGINEERING SPEC.	ES 30000-0
MATERIAL	
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	ES
TOLERANCE UNLESS OTHERWISE NOTED	LINEAR .X ±; .XX ±; .XXX ±; ANGULAR ±; FINISH OUTSIDE MAX; FINISH INSIDE MAX
EC HISTORY	DATE
TITLE	SCHEMATIC DIAGRAM SA1000 CONTROL
DETAIL	RELEASED FOR ASSEMBLY
DESIGN	
APPRO	
SIZE	D
SCALE	—
DOC CODE	SC
PART NO	26050-1
REV	5234
SHEET	3 OF 3

PART NO 26045-2

+ DIRECTION IN
- STEP IN
- POR
+ 3.69 µs CLOCK
+ TRK Ø DETECT
- INDEX SL
+ REF SK COMP
+ 14.45 STEP ENABLE
+ TRK ØØØ
- UTS (RDY)
- Ø B1
- Ø B2
- Ø A2
- Ø A1
+5V
TP1
TP5
R1 R2 R3 R4 R5 R6 R11
1A 1B 1C 1D 1E 2A 2B 2C 2D 2E 2F 3A 3B 3C 3D 3E 3F 4A 4B 4E 4F 5A 5B 5E 5F

C2-C13 .1µf
C1 4.7µf ±20%
+5V
GND
19, 21 & 24
1-17 ODD
TP 2, 3

REFERENCE DESIGNATION	
LAST USED	NOT USED
C13	
R11	
TP5	TP4

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GRD (PIN)
7400	3C 4F		14	7
7402	3D		14	7
7404	2D	2D, 2D2	14	7
7409	2C		14	7
7432	1A, 4E	1A2	14	7
7474	2A 1C 3E, 5F	5F2	16	8
7485	4A		16	8
74156	2F		16	8
74157	3B		16	8
74161	1C		16	8
74191	3A, 2E		16	8
74153	4B, 5E		16	8
CD4012B	5A 1B 2B 1E 2E		14	14
82S23	3B		16	8

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE 2K OHMS, ¼ W, 5%.
2. ALL CAPACITORS ARE AXIAL LEAD, 0.1 µf, 50V, +80-20%
3. 74 LS SERIES IC'S MAY BE USED.
4. IC., PROM, PAMP CNTL.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO	TITLE SCHEMATIC DIAGRAM STEPPER LOGIC.
	LINEAR ± XX / ± XXX			DETAIL — RELEASED FOR ASSEMBLY
CASE DEPTH	ANGULAR ±			APPRO — SHEET 1 OF 1
HARDNESS				SCALE — DOC CODE SC PART NO. 26045-2 REV
SURFACE TREATMENT ES	CORNERS & EDGES OUTSIDE MAX. / INSIDE MAX.			D

DISK CONTROLLER EIGHT INCH SCHEMATICS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	PROTOTYPE		
B	REDRAWN & REVISED 1ST RUN	2/3/81	

OB7
OB6
OB5
OB4
OB3
OB2
OB1
OBØ

LS244 2A

J4-23 DIOB Ø
J4-15 DIOB 1
J4-13 DIOB 2
J4-11 DIOB 3
J4-21 DIOB 4
J4-20 DIOB 5
J4-16 DIOB 6
J4-12 DIOB 7

LS244 3A

J4-7 HDRD
J4-10 IORD
J4-31 YB
J4-18 IOWR

LS32 2B
LS32 2B

2C ½LS139
LD DR/HD
LD SECT/OLD CYL / DATA
LD NEW CYL
LD COMMAND

J4-24 ABØ
J4-26 AB1
J4-4 HDWR

2C ½LS139
TOP
STAT

LS04 2D

1BØ
1B1
1B2
1B3
1B4
1B5
1B6
1B7

LS273 9A
EN REF OSC
SEEK HDRDY
RECAL BADB
REZERO
RESET HD

LS273 8D
RD
WR
FRM
SEN REF OSC
SWDRDY
DMA BSY
IP
STBZ
IMK
TBZ
CLR CMD REG
PLO CLK B

LS273 8A
RST

LS374 7A
COMP SECT

LS273 6A

LS374 6B

SEEK
COMP CYL
14A LS02

LS244 7B
CBØ 1 2 3 4 5 6 CB7

PR LS74 6C

EN COMP
S1

LS585 5C
LS585 4C
LS585 3C
A=B
STEP IN

LS191 5B
LS191 4B
LS191 3B
COMP HD
STEP

R7 4.7K
R8 4.7K

7438 8C
-DS1 J1-26
-DS2 J1-28
-HSØ J1-14
-HS1 J1-18
-HS2 J1-4
-HS3 J1-
-REZERO J1-6

S288 8B 'SBP2'
CBØ CB1 CB2 CB3 CB4 CB5 CB6 CB7
EØ E1 E2
ENSBP

LS273 4A
1BØ 1B1 1B2 1B3 1B4 1B5 1B6 1B7

PL

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		ALTOS COMPUTER SYSTEMS	
APPROVALS	DATE	DISK CONTROLLER 8"	
DRAWING CR	2/3/81		
CHECKED		SCALE —	SIZE D DRAWING NO. 8500-0021 B
		DO NOT SCALE DRAWING	SHEET 1 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

J4-2 INT

OBØ
OB1
OB2
OB3
OB4
OB5
OB6
OB7

12A LS244

BUSY
TASK COMPLETE
BAD SECT
RECORD NOT FOUND
CRC ERR
WRITE FAULT
RDY

STAT

R3 470Ω
C6 30pf
L1 22uh

15B LS04

15C LS00

RESET HD
J4-8 MR RESET
HD RDY

14A LS02

16C LS08

SC
RDY
SEEK
RECAL
TRK Ø
A=B
STEP IN
STEP
J4-34 1 MHZ

15C LS00
16D LS32
17F LS00

16A LS74 — SC
16A LS74 — SCLRC
16E LS74
16F LS74

15E LS193

REZERO

16C LS08
16D LS32

15B LS04
15A LS08

L2 22uh
R2 470Ω
C5 30pf

CLR STATUS
CLR CMD REG
RST

MFM WRITE DATA
TIMING CLK

17C 75110
17D 75110

J2-13 J2-14 MFM WRITE DATA
J2-9 J2-10 TIMING CLK
J3-13 J3-14 MFM WRITE DATA
J3-9 J3-10 TIMING CLK

RP2 18E 47Ω

17E
J2-17 J2-18 MFM DATA 1
J3-17 J3-18 MFM DATA 2

MFM DATA
14E S00
17E 75107A

17B LS14

J2-1 -DRIVE 1 SELECTED
J3-1 -DRIVE 2 SELECTED
IMK — J1-20 -INDEX
RDY — J1-22 -READY
TRK Ø — J1-42 -TRACK Ø
SC — J1-8 -SEEK COMP
WRITE FAULT — J1-44 -WRITE FAULT

16B 7438

J1-34 -DIRECTION IN
J1-36 -STEP
J1-2 -REDUCED WRITE CURRENT
J1-40 -WRITE GATE

R1 4.7K
EN COMP
WR GATE

R5 75Ω
R4 1K
Q1 2N3906
CR1 IN7474 (3.6V ±5%)
R6 510Ω

220/330 RPAC 18B

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		ALTOS COMPUTER SYSTEM	
APPROVALS	DATE	DISK CONTROLLER 8"	
DRAWN CR	2/5/81		
CHECKED		SCALE —	SIZE D DRAWING NO. 8500-0021
		DO NOT SCALE DRAWING	SHEET 2 of 5

8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

NRZ DATA
NRZ CLK
MR FIFO
WR
FRM
BAOB
J4-28 BUSAKB
DMARQ
J4-27 RDMA
J4-29 Φ
J4-32 RDB
TOP
PL
RD
WR GATE
B MATCH
PLO CLK A
ENCPSI
ENCPCRC
WRITE DATA
CWE
PR CRC
SEN CRC CHK
CLR STATUS
PLO CLK A
CRC ERR
EN CPSO
COMP HD
BSF
EΦ
P1-1
P1-2
P1-3
P1-4
P1-5
P1-6
+5
+12
-12
-5
VR1
LM320
C1 10uf
C2 10uf
C3 10uf
L3 22uh
R9 470Ω
C7 30pf
1BΦ
1B1
1B2
1B3
1B4
1B5
1B6
1B7
OB7
OB6
OB5
OB4
OB3
OB2
OB1
OBΦ
CBΦ
CB1
CB2
CB3
CB4
CB5
CB6
CB7
13B LS299
12B 25LS2521
11B LS299
10B 25LS2521
11A 9403
10A 9403
6C LS74
2E LS74
2E LS74
11D LS74
9D 9401
3D LS02
2D LS04
1E LS00
10D LS00
15A LS08
9C LS08
11C S02
15B LS04
10C S51
11C S02

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	ALTOS COMPUTER SYSTEMS		
APPROVALS	DATE	DISK CONTROLLER 8"	
DRAWN CR	2/3/81		
CHECKED		SCALE —	SIZE D
		DRAWING NO. 8500-0021	B
		DO NOT SCALE DRAWING	SHEET 3 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

PLO CLK B

PLA 82S100 6D
I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14 I15
F0 F1 F2 F3 F4 F5 F6 F7

B MATCH
STBZ
DMA BSY
BAD SECT
CRC ERR
SHD RDY
IP
WR
RD
FRM
CZ 20

1F LS32 (IDER26)

F0 → 18 INCREMENT
F1 → 17 JUMP
F2 → 16 LOAD COUNTER
F3 → 15 CLRS
F4 → 13 CLRC
F5 → 12 EN BAD SECT CHK
F6 → 11 BUSY
F7 → 10
19

EN CRC CHK
CLRC

LS163 6F: T=10, P=7, A=3, B=4, C=5, D=6, CLR=1, LD=9, RC=15, QA=14, QB=13, QC=12, QD=11

LS163 7F: T=10, P=7, A=3, B=4, C=5, D=6, CLR=1, LD=9, Q1=14

S288 4E CP22: 10 11 12 13 14 15 CE → 1 2 3 4 5 6 7 9
CWE

S288 5E CP12: 10 11 12 13 14 15 CE → 1 2 3 4 5 6 7 9
COMP CYL
COMP HD
COMP SECT
ENCPCRC
EN REF OSC
EN SBP
EN CPSO
EN CPS1

LS273 4D: D=8 7 18 4 3 14 13, CLR=11, Q=16 9 6 19 5 2 15 12
EN CRC CHK
CLRC
SEN CRC CHK
PRCRC
EN SYNC DET
SCLRC
WR GATE
STATE Ø
MR FIFO
DMARQ

PLO CLK B
ENPL
LOAD COUNTER

LS163 2F: T=10, P=7, A=3, B=4, C=5, D=6, LD=9, CLR=1, TC=2, QC=12
1F LS32 (10, 8, 5) → 1F LS32 (4, 6, 5) → 1E LS00 (4, 6) → S1

LS163 3F: T=10, P=7, A=3, B=4, C=5, D=6, LD=9, CLR=1, TC=2
LS163 4F: T=10, P=7, A=3, B=4, C=5, D=6, LD=9, CLR=1, TC=2
LS163 5F: T=10, P=7, A=3, B=4, C=5, D=6, LD=9, CLR=1, TC=2

RST
BAD SECT
BSF
PLO CLK B

9C LS08 (2, 1, 3)
7E LS00 (2, 1, 3)
8E LS74 (D=12, CLR=13, Q=9, PR=11, Q̄=8)
8E LS74 (D=2, PR=4, Q=5, CLR=3, Q̄=6, 1)
RECORD NOT FOUND

IMK
STATE Ø
CLR STATUS
COMP CYL

LS191 8F: D/U=5, EN=4, LD=11, A=15, B=1, C=10, D=9, QA=13, QB=12, QC=6, QD=7, CLK=14
9C LS08 (5, 4, 6)
7E LS00 (12, 13, 11)

S288 6E "JAP2": 10 11 12 13 14 15 CE → 1 2 3 4 5 6 7 9
Eø
E1
E2

S288 3E "CLP2": 10 11 12 13 14 15 CE → 1 2 3 4 5 6 7 9

1E LS00 (1, 2, 3)
R34 4.7K
S2: 1 2 3 → 6 5 4
256
512

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		ALTOS COMPUTER SYSTEMS
APPROVALS	DATE	DISK CONTROLLER #8
DRAWN CR	5/9/81	
CHECKED		SCALE —— SIZE D DRAWING NO. 8500-0021 B
		DO NOT SCALE DRAWING SHEET 4 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

9E OSC 8.68 MHz K1115

2WRCLK

10F S74

15D LS163

TIMING CLK

SYNC FIELD DETECTOR

R14 1K 1% R15 500Ω C10 30pf

14D 96502 57.5ns

MFM DATA

11D LS74

TBZ

VPU1

R21 R20 VPU2 VPU1

R17 1K 1% R16 500Ω C11 330pf

14D 278ns 96502

LS193 13E

103ns 13D 96502

R11 1.15K 1% C8 5% 100pf

EN SYNC DET

MFMRD

SEN REF OSC

7E LS00

9F 551

12F S74

CR3 IN4148 R27 3.92K 1% R28 100K R32 5K

PHASE LOCKED OSCILLATOR

C17 .01μf 5% C16 100pf 5% R30 680Ω R23 1K 1% C14 .1μf R24 1K 1% L4 22μh C15 47μf/6V R22 4.7K

CR2 IN4148 R31 3.92K 1% R29 100Ω 2N2222 Q2 Q3 2N2222 R26 20K CR4 IN4148

15F S124 FC CEXT RNG EN OUT C12 30pf 5% C13 .1μf R25 10K 1%

PHASE COMPARATOR

2 PLO

11F LS00

E∅

PLO CLK A

13A LS74

16E LS74

A1 BYTE

SET PHASE OF PLO

10E S112

11E S112

12E S112

NRZ DATA

MFM TO NRZ DECORDER (DATA SEPARATOR)

VPU3 R19

NRZ CLK

ENPL SI CB∅ CB1 CB2 CB3 CB4 CB5 CB6 CB7

9B LS299 R33 4.7K

WRITE DATA

WR GATE

EN COMP

NRZ TO MFM ENCODER

14B PAL 16R4

EARLY NORM LATE MFM OUT

13C S64

R12 180Ω R13 240Ω

20 DELAY 12C

R10 1K 1% C9 100pf 5%

13D 96502 100ns

14E LS00

PLO CLK B

PLO CLK A

WR GATE

MFM WRITE DATA

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		ALTOS COMPUTER SYSTEMS	
APPROVALS	DATE	DISK CONTROLLER 8"	
DRAWN CR	2/3/81		
CHECKED		SCALE —	SIZE D DRAWING NO. 8500-0021 B
		DO NOT SCALE DRAWING	SHEET 5 OF 5

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