
Computer Products, Inc.

Revision B
INTERFACE GUIDE
FOR

# LSI-50 CONTROLLER

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Revision B
**INTERFACE GUIDE**
**FOR**

# LSI-50 CONTROLLER


**ALLOY COMPUTER PRODUCTS, INC.**
Corporate Headquarters, Framingham, Massachusetts

ALLOY COMPUTER PRODUCTS was founded in 1979 to service the computer industry's needs to interface large system types of peripherals to mini, micro and personal computers.

ALLOY designs and manufactures complete computer systems, tape and disk subsystems, and tape and disk controllers for many computers.

ALLOY sells and services its equipment through a worldwide dealer and distribution network.

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The hardware and software product, and revision codes printed alongside the date indicates the version and update level of the product at the time the manual edition or update was issued. Many product updates and fixes do not require manual changes, and conversely manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

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|---|---|---|
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| DP-8000 | LSI-50 | PC-SLAVE/16 |
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| DZ-80 | OSBU | QICTIP |
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| IDS-412 | PC-CARD | TMB-1 |
| IDS-PC | PC-DISK | TRS-232 |
| IDX-506 | PC-PLUS | TS-100 |
| IDXS-100 | PC-QICTAPE | TZ-80 |
| IDXS-PC | PC-QT2 | XS-100 |

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**Summary:** The LSI-50 is a DEC LSI-11 compatible controller integrating the NEW 55 ips CDC Streaming tape drives. Unlike most "Streamer" integrations, the LSI-50 provides File-Oriented Backup/Restore operations under Standard DEC Utilities i.e. PIP, FILEX, BRU, DUP, COPY, DSC, and PRESERVE at "Streaming" Speeds.

A 32 K-byte "relaxation" buffer on the controller allows overlapped I/O with Disk activity without requiring specialized programming. Dynamic logical Record sizes of up to 16K Bytes are allowed.

Configured as single Quad size controller and requiring only 5 volts @ 2.2 amps, it easily fits into the smallest of systems, yet provides an upgrade path through 22-bit addressing to support the largest of systems. Functionally emulating the DEC TM-11 Tape System, except for "destructive" reverse-space commands, it not only provides Backup, but also serves as "spooling" storage or "program-load". Because the CDC Streamer is error-transparent and writes bidirectionally to 11 tracks, it will eliminate the normal OS problems associated with soft errors and rewind timeout between tracks.

More importantly, a full 44 Megabytes are stored on each 450 foot cartridge unlike the typical 4.5 Mb at 512 byte record lengths with conventional stop-start Tape Systems. The typical transfer rate under the DEC Utilities is 3 Mb/min.

# I. INTRODUCTION

The LSI-50 product is designed to interface the Digital Equipment Corporation's LSI-11 computer to the CDC 1/4" Cartridge Streamer. To the user and the LSI-11, the interface responds just as you would expect a standard 9-track tape drive interface, since it emulates that command set, but through the intelligence of the on-board 8085 microprocessor, converts the data into a form suitable for streaming, with a minimum amount of start/stop action. This technique allows very efficient throughput of system functions such as disk backup, multiple file copy, and mass storage.

# II. PROGRAMMING SUMMARY

The typical sequence used in initiating any tape operation would include programming the peripheral registers (i.e. Byte Record Count, DMA address counter) first, and then issuing the command. Each of the usable registers and their bit-positional significance are listed below.

## 1. MAG TAPE STATUS REGISTER - 772520

The factory pre-wired address of this register is 772520 (octal). It is a read-only register. At any time during a tape operation, this register will reflect the current status of the controller. The individual bits represent the following information:

BIT 15 - ERROR: Set as a result of any of the following conditions:

1. Any write command to a drive whose Write Lock bit is set.
2. Any command to a drive whose Select Remote bit is clear.
3. The setting of any of bits 8 - 14 in the Mag Tape Status.

BIT 14 - END OF FILE: Set to indicate that a File Mark was detected.

BIT 13 - UNUSED:

BIT 12 - HARD ERROR: Set to indicate any unrecoverable tape errors.

BIT 11 - BUS GRANT LATE: Set to indicate that a DMA request was not granted within 10 microseconds, thus running the risk of losing data due to the lack of memory refresh on either the controller or the LSI-11.

BIT 10 - END OF TAPE: Set to indicate that the physical end of tape was sensed by the controller. The only allowable commands during this condition are rewind or space reverse.

BIT 9 - RECORD LENGTH ERROR: Set during a read operation where the record read exceeded the size specified by the LSI-11.

BIT 8 - BAD TAPE ERROR: Set to indicate that the tape cartridge installed is incapable of reliable data storage.

BIT 7 - UNUSED:

BIT 6 - SELECT REMOTE: Set to indicate that the addressed tape drive is on-line, has been selected and has a tape cartridge installed.

BIT 5 - BEGINNING OF TAPE: Set when the addressed tape drive is positioned at the physical beginning of tape.

BIT 4 - UNUSED:

BIT 3 - UNUSED:

BIT 2 - WRITE LOCK: Set when the addressed tape unit's write protect switch is set to the "protect" state. No write commands will be honored in this condition.

BIT 1 - REWIND STATUS: Set to indicate that the addressed drive is currently in the process of rewinding to the beginning of tape.

BIT 0 - TAPE UNIT READY: Set when the selected drive is in the proper state to receive and execute valid tape commands.

## 2. MAG TAPE COMMAND REGISTER - 772522

The factory prewired address of this register is 772522 (octal). The following list defines the respective bit positions used in this register:

BIT 15 - ERROR: Set to indicate an error condition which is defined by the error bits in the status register. Cleared by an INIT or a GO command to the controller.

BIT 14 - UNUSED:

BIT 13 - UNUSED:

BIT 12 - POWER CLEAR: This bit set indicates that the controller should perform a power up sequence.

BIT 11 - UNUSED:

BIT 10 - UNUSED:

BIT 9 - UNUSED:

BIT 8 - UNUSED:

BIT 7 - CONTROLLER READY: Cleared on GO command and set when operation specified has been completed.

BIT 6 - INTERRUPT ENABLE: When set, allows interrupt to occur upon successful completion of an operation or notification of an error condition.

BIT 5 - EXTENDED ADDRESS: Corresponds to the bus signal BDAL17L and indicates that DMA operations to or from the LSI-11 are to address extended memory.

BIT 4 - EXTENDED ADDRESS: Same as BIT 5 but corresponds to bus signal BDAL16L.

BIT 3,2,1 - FUNCTION BITS: These three bits, along with the GO bit will initiate a tape operation defined by the following table:

| BIT 3 | BIT 2 | BIT 1 | |
|---|---|---|---|
| 0 | 0 | 0 | OFF LINE |
| 0 | 0 | 1 | READ |
| 0 | 1 | 0 | WRITE |
| 0 | 1 | 1 | WRITE EOF |
| 1 | 0 | 0 | SPACE FORWARD |
| 1 | 0 | 1 | SPACE REVERSE |
| 1 | 1 | 0 | ILLEGAL |
| 1 | 1 | 1 | REWIND |

BIT 0 - GO: When set begins the operation defined by the function bits.

### 3. BYTE RECORD COUNTER - 772524

This register is factory prewired to address 772524 (octal). The purpose of this register is twofold: when used during a read or write operation, this register is loaded with the 2's complement of the number of bytes to be read or written. When used during a space forward or a space reverse operation it is loaded with the 2's complement of the number of blocks to be spaced. The register is incremented for every byte transferred or block spaced. Operation will be complete when the count reaches 0, or in "space operations" when a FILE MARK, BOT, or EOT is encountered.

### 4. MEMORY ADDRESS REGISTER - 772526

This register is factory prewired to address 772526 (octal). It is loaded with the starting address of the data buffer from or to which the controller will transfer data. It is incremented by 1 for each byte of data transferred and if an overflow occurs, then will increment the extended address bit counter and continue to count from 0.

### 5. EXTENDED MEMORY ADDRESS REGISTER - 772534
(22 bit addressing)

| | |
|---|---|
| BIT - 8 | BDA18L |
| BIT - 9 | BDA19 |
| BIT - 10 | BDA20 |
| BIT - 11 | BDA21 |

NOTE: These bits are write only.

### 6. INTERRUPT VECTOR - 224

The Interrupt Vector is factory prewired to location 224 (octal) for the LSI-11.

## III. INSTALLATION INSTRUCTIONS

The LSI-50 is a standard quad height interface card which plugs directly into the Q-BUS backplane. The user should note that both interrupt and DMA daisy-chain signals must be properly propagated for use on the board, and no blank slots may exist above the LSI-50, unless occupied with the appropriate bus propagation cards.

The CDC tape drive may be supplied in a stand-alone chassis (ALLOY #TMC-1C) with all necessary cabling provided. Once the interface card is installed in the computer, the 8' 34 conductor ribbon cable from the drive should be plugged into the interface card's P1, being sure to observe the proper cable polarity. The supplied cable is marked with a contrasting color line to designate pin 1, and the controller board's pin 1 is clearly marked on the board's silk screen printing.

## IV. INITIAL SYSTEM CHECKOUT

Once power is applied to the system, the user should perform some preliminary functional checks to ensure proper installation of the controller board. By following the sequence below, the user will be able to verify the ability to address the control board and access the internal registers.

Momentarily depress the HALT switch, or hit the BREAK key on the system console to enter the Console ODT mode on the LSI-11. To see that the board is actively responding to its address on the bus, type '772520/' on the console. The controller should respond by outputting the contents of its Mag Tape Status Register, which will be displayed on the video. By then typing three successive 'LINE-FEED' keys, the other three register's contents will be displayed.

Tape movement may be initiated by depositing the number '7' in location 772522, which will cause the drive to write a file mark to tape. The user may then deposit the number '17' in the same location in order to cause the drive to rewind and reposition itself at BOT.

If these tests can be satisfactorily performed, then the user may proceed to boot his system as he normally would. If the above tests fail, it is recommended that the user review the installation instructions to be sure he has properly installed all cabling and has power applied to the tape drive.

## V. POWER REQUIREMENTS

The LSI-50 requires the following voltage at the current indicated:

+5 VOLTS D.C. @ 2.50 AMPS MAXIMUM
*
+12 VOLTS D.C. @ 0.05 AMPS MAXIMUM
* used only on/P config.

## VI. DRIVE INDICATOR LIGHTS

The LED indicators on the front panel of the tape drive have the following meanings:

LOAD/UNLOAD - Indicates a cartridge can be inserted or removed without interrupting the device function in progress.

DATA CHECK - Indicates that excessive read or write errors have been detected. It is recommended that the magnetic head be cleaned to maintain Read/Write performance. Successive data checks may indicate a defective cartridge.

DEVICE - Indicates that microcode has detected a fault within the drive hardware and the device is not operational.

## VII. PROGRAMMING NOTES

### A). USER CONSIDERATIONS

The LSI-50 storage medium is an 1/4 inch streaming tape drive based on the CDC Cartridge Streamer. While the LSI-50 attempts to functionally emulate an LSI-11 magnetic tape unit (TM11, TS03 or TU45),there are inherent differences between the devices making a complete emulation impossible. These differences are:

1. Only forward tape motion is supported. Excepting a rewind command, the tape cannot be backspaced to reposition the tape at the beginning of a previously read / written record. In support of some of the DEC utilities, logical backspaces are performed over the limited amount of data in the LSI-50's internal buffer.

2. Data may only be written to the beginning of tape or at end of data. End of data defines the point on the tape that the previous write operation terminated data transfer. This means that data written on tape may not be overwritten, excepting write data request from the beginning of tape (BOT).

## B). RT-11 UTILITY SUPPORT

The LSI-50 supports all RT-11 utilities that perform transfers with magnetic tape devices (MT:). A synopsis of the more significant tape transfer utility commands is:

**COPY/DEV xx: MT:**

copy device 'xx:' to MT: (backup device)

**COPY/DEV MT: xx:**

copy device MT: to 'xx:' (restore device)

**COPY file MT:/POS:-1**

copy file to MT:. MT: must have been previously initialized, however files may be added to the end of the tape. The POS:-1 switch specifies that the tape is not to be rewound between file transfers. Note, the POS:x use of the switch can not be used to overwrite a file of tape.

**COPY MT:file file**

copy file from MT: written in the copy file mode to a file on a system device.

**DIR MT:**

list the directory on the MT:

**INIT MT:**

initialize MT:. Tapes must be initialized before copy file commands are issued. The copy device command does not require initialized tapes.

**Miscellaneous Notes**

1. RT-11 FILEX does not support MT:.
2. The SQUEEZE command does not support MT:.
3. File output cannot be assigned to MT:
4. Copy file will operate the tape in start/stop mode. There is too much overhead in the PIP utility to maintain streaming.

## C). RSX-11M UTILITY SUPPORT

The LSI-50/MT device is supported by the following RSX-11M utilities:

1. BRU (Backup and Restore Utility)
2. DSC (Disk Save and Compress Utility)
3. FLX (File Transfer Utility)

As a convenience, a brief description of the command syntaxes follows. For more detailed information consult the RSX-11M Utilities manual.

**BRU/MOU/REW/VER/BAC:xxx dd: MT:**

backup device 'dd:' onto MT:. /MOU specifies device 'dd:' is currently mounted and is ommitted if the volume is not mounted. /REW specifies the transfer is to start at the beginning of tape. /VER specifies the copy is to be verified at completion. /BAC:xxx the name of the save-set. Save-set naming allows the user to recover individual files, should the need arise.

Note, while more than 1 save-set may be backed up onto the MT:, only the first save-set may be verified.

**BRU/MOU/REW/VER/BAC:xxx MT: dd:**

restore device 'dd:' from MT:. See above notes.

**DSC MT0:/RW/VE=dd:**

backup device 'dd:' onto MT:. /RW specifies the transfer to start at the beginning of tape. /VE specifies the copy is to be verified at completion.

Note, if the DSC task image is invoked, the device to be backed up must be dismounted.

Note, if the standalone DSC system is invoked 'BOODSCS8', the first command must be to establish the MT vector address:

MT:/VEC=224

**DSC dd:=MT0:/RW/VE**

restore device 'dd:' from MT:. See above notes.

**FLX MT:/Z**

Initialize the directory of MT: for FLX file transfers.

**FLX MT:/DO=file/RS**

copy specified file(s) in Files-11 format onto the MT in DOS format.

**FLX file/RS=MT:file/DO**

copy specified file(s) from MT: in DOS format to files in Files-11 format on the system device.

**FLX MT:/LI**

list the directory of MT:

**Miscellaneous Notes**

1. The LSI-50 does not support the PIP utility program or general Files-11 directory routines. This means data may not be redirected or assigned to the MT device.

2. The LSI-50 will support multiple save sets under BRU, but not under DSC.

## UNIX/ZENIX UTILITY SUPPORT

The LSI-50 will support all UNIX tape utilities, including DD, DUMP, TP, and TAR. Some examples of their uses are listed below.

**DD IF=(FILENAME) OF=/DEV/(N)RMT0 COUNT=X**

This will transfer X number of blocks from filename to the magtape, and will not rewind the drive to BOT on completion if the N prefix is added to the drive specification. The restore function works with the reversed filespecs:

**DD IF =/DEV/(N)RMT0 OF=(FILENAME) COUNT=X**

Using the TAR utility is as follows:

**TAR XFB/DEV/(N)RMT0 (bs) (FILENAME)**

This command sequence will restore Filename (or all if no filename is specified) from tape to disk. The 'bs' designates the blocking factor to be used. Again, the 'N' prefix will cause the drive to <u>not</u> rewind to BOT if added.

For further information on UNIX Tape Utilities, consult your UNIX user's manual.

## VIII. SYSTEM ARCHITECTURE

The system consists primarily of three distinct sections: the on-board processor and memory, the interface to the CDC tape drive, and the LSI-11 interface. Contained within each section are components which allow each to transfer data to and from a common bus, all under the control of the 8085 microprocessor. Also, data transfer is achieved by means of the 8257 DMA controller so as to maintain the maximum speed within the constraints of the individual systems.

Referring to Figure 1. we can see that each entity (CDC or LSI) has a path to read or write from the on-board memory via the DMA controller. We will now proceed to see how the data flow from computer to tape and vice versa is actually performed, by examining the protocol required by each unit.

Assuming, for reasons of simplicity, that we wish to perform the transfer of a single block of 512 8-bit bytes of data from the LSI-11 to the CDC tape. The LSI-11 initiates the transfer by first transferring its own pertinent data to the controller. The first 16-bit word of information that it sends to the controller is the number of bytes to be fetched from its memory. The second word contains the starting address at which that data is stored. It will then issue the command to the controller to proceed with the transfer. Since the data will be moved from the LSI-11 memory by DMA techniques and is operating in an interrupt driven environment, it has no further need to monitor the operation, assuming that an interrupt to a specific location will be performed upon either successful completion, or an error condition. At this time the 8085 takes over complete control of the transfer set-up.

First, the 8085 fetches the number of bytes to be transferred. This parameter will be used in setting up the 8257 DMA chip. It also programs the 8257 with the address within its own memory space to which the data must be transferred. It will then signal the DMA controller to begin its programmed transfer, also awaiting an interrupt signalling either completion or error condition.

During the time the block is being transferred, both the 8085 and the LSI-11 are free to perform other tasks, since the DMA between the devices is operated on a 'cycle-stealing basis', requiring neither CPU's intervention.

Upon successful completion of its task, the 8257 will interrupt the 8085. The 8085 will then proceed to program another channel within the same DMA controller in preparation to transfer the block of data, which now resides within the 8085's memory, on to the tape drive. The same byte count and address information are programmed as before, but a unique set of logic will control the hand-shaking between the devices.

Again, once this transfer is initiated, the CPU will be notified via an interrupt upon completion of the task. Once this interrupt has been received, the 8085 stores the status of the tape drive in a register which the LSI-11 will access to ensure proper tape operation, and the 8085 forces an interrupt to occur on the LSI-11 control lines.

Data transfer in the opposite direction, tape to LSI-11, is simply performed in the reverse sequence, although the LSI-11 must still initiate the transfer as before.

## IX. FUNCTIONAL DESCRIPTION

### 1. 8085 MICROPROCESSOR, EPROM, AND MEMORY

On power-up of the LSI-11, or upon depressing the BOOT switch, the LSI-11 bus signal BINITL is asserted, in turn asserting INIT0* on the controller. This signal clears the signals ERR*, CUR*, and REQH. It also asserts the RESET input to the 8085, which in turn asserts its RESET to clear the 8257. Once the signal BINITL is de-asserted the 8085 will perform a restart to location 0000H. There it will begin the firmware initialization sequence, clearing memory, rewinding the CDC tape drive and adjusting internal pointers. Once this is completed, the 8085 will loop through a routine which waits for a command to be sent from the LSI-11.

Addresses 0000H through 07FFH are reserved for the EPROM which is read only memory in which resides the firmware. Address 1000H through 4FFFH are for the read/write RAM's. Address 0800H through 0FFFH are reserved for possible future EPROM addition.

The 8085 uses multiple interrupt inputs in order to be informed of external events. The signal RST55H informs the CPU that the controller has just received a command from the LSI-11. RST65H tells it that the 2651 is requesting service. The signal RST75H flags the completion of a DMA transfer, by either the 8257 or the DEC interface logic. The 8085 will sense the signal OLD via its SID line to see if an off-line dump is being requested.

## 2. 8257 DMA CONTROLLER

The 8257 is used to control the transfer of data from RAM to either the CDC tape drive or the LSI-11. It can be programmed by the 8085 via I/O commands to ports 10H through 18H, inclusive. A DMA transfer is initiated by any one of the DREQ0-3 lines going to a high state, once that channel has been enabled by the 8085. Upon sensing that request, the 8257 requests the use of the system bus by asserting HRQ. The CPU, once it has completed any instruction in process, will honor the request by asserting its HLDA. The 8257 then outputs the address to be accessed and signals the requesting device to proceed by asserting the appropriate DACK0-3*. It will then assert either MEMR* or MEMW*, depending upon which direction the transfer must take place, and wait until the signal READY is asserted, this being the method by which all the DMA's are synchronized. Once READY is asserted it will de-assert its MEMR* or MEMW*, its DACK*, and its HRQ. It will then remain idle until a new DREQ becomes asserted. After the 8257 outputs the address to the system bus, it decrements its internal byte counter and increments its internal address counter. If the result of decrementing the byte counter is zero, then during that cycle the 8257 will set its signal TC in order to notify the 8085 that the programmed transfer was completed.

## 3. LSI-11 INTERFACE AND REGISTERS

In order to minimize the parts count, the DEC Chipkit set was incorporated to realize the LSI-11 bus interface. This set includes four bi-directional four-bit buffers for driving and receiving the Data and Address lines, one register decoder, one interrupt control, two dual 8-bit register/counters for byte count and address generation, and one DMA bus controller. The BDAL buffers have jumper selectable inputs for coding the device address of the controller, as well as jumper selectable inputs for coding the interrupt address. When the address on the BDAL lines is equal to the address jumpers, each chip will generate the signal MATCHH, which in conjunction with the signal BSYNCL will cause the register decoder to set one of the signals SEL0L, SEL2L, SEL4L, or SEL6L, depending on the state of the BDAL1 and BDAL2 lines. These signals select one of four registers.

SEL0L selects the Mag Tape Status Gate, SEL2L selects the Mag Tape Command Register, SEL4L selects the Byte Record Counter, and SEL6L selects the DMA Address Register. The Status Register is a read-only register, the Command Register is a read/write register, and the Byte Record and Address registers are read/write registers.

## 4. CDC TAPE DRIVE INTERFACE

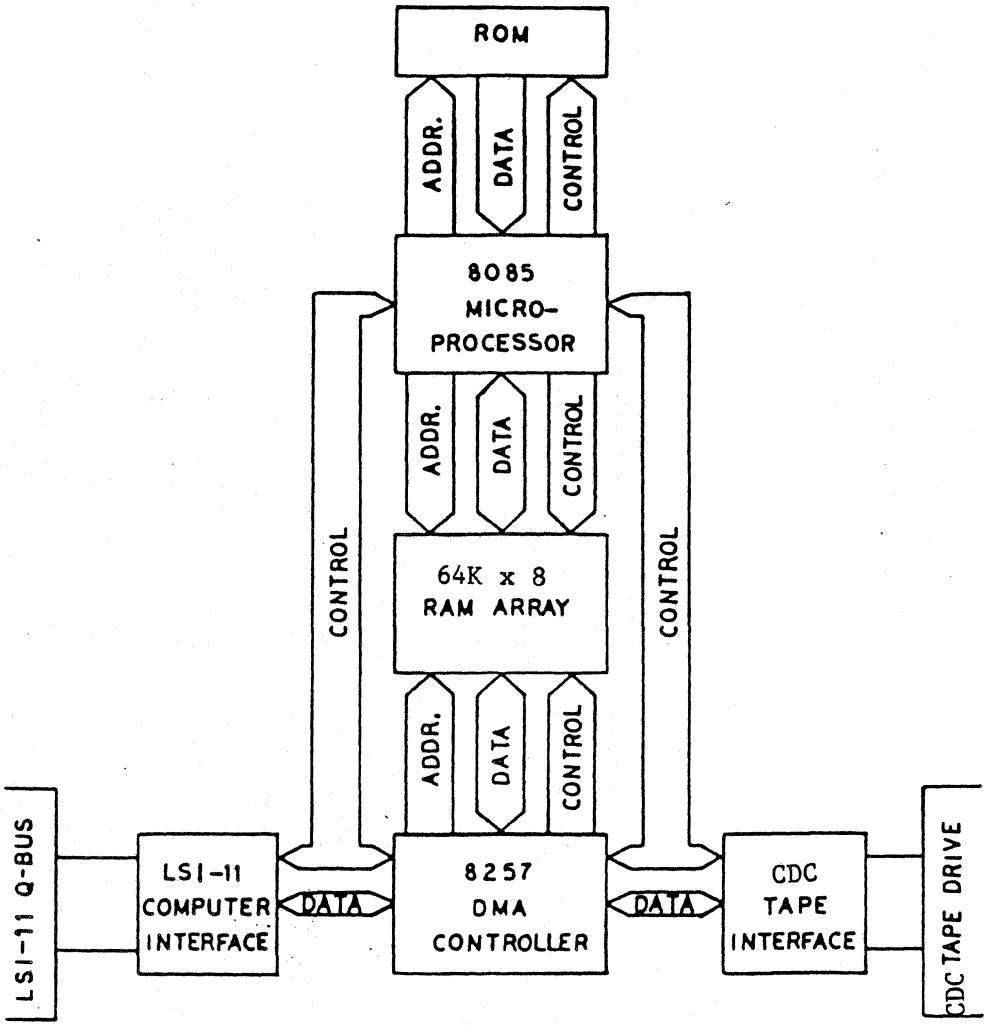
The CDC interface consists of three sections:

1. The command register, which contains the unit select bits and the command bits.

2. The drive status register.

3. The data register which is a bi-directional tri-state gate. DMA handshaking between the drive and the 8085 is performed by the two signals DRY* (from the drive) and DSB* (generated by the 8085). When the tape drive has data available to be read, it will assert DRY*, which will generate the signal DREQ2. If enabled, the DMA channel will proceed to perform a DMA cycle. In transfers from the RAM to tape, the signal DSB will be asserted, and will remain until the drive responds with DRY*.

**FIGURE 1. -(Simplified Block Diagram)**



DWG NO ADI00159 | SH 1 OF 1 | REV G

EJECTOR "L"

EJECTOR "R"

ROLL PIN (2 PLACES)

ROLL PIN (2 PLACES)

LED1

P1

2

34
33

M79 M80 M81 M82 M83 M84 M85 M86 M87 M88 M89

R12 R30 R10 R4 R29 R17 R22 R28 R7 R14 R25 R9 R6 R8 R11

C27 C28 C26 C22 C23 C24 C25

M63 M64 M65 M66 M67 M68 M69 M70 M71 M72 M73 M74 M75 M76 M77 M78

M49 M50 M51 M52 M53 M54 M55 M56 M57 M58 M59 M60 M61 M62

M35 M36 M37 M38 M39 M40 M41 M42 M43 M44 M45 M46 M47 M48

C21 C31 C3

CL2

C19 C18 C20

M19 M20 M21 M22 M23 M24 M25 M26 M27 M28 M29 M30 M31 M32 M33 M18

R18 R19 R24

R26 R27 M6 CL1 M7 M8 M9 M10 M11 M12 M13

C29 C30

M14 M15 M16 M17 M5

C12 C16 C17

A8 10 9 A11 13 12 V8

A5 7 6 V7 6 5

A2 4 3 V4 3 2

M1 M2 M3 M4

C11 C13 C14 C15

C1 C2 R15 R23 R20

DA1 CA1 BA1 AA1



ALLOY ENGINEERING COMPANY

Scale —

Date

COMPUTER PRODUCTS DIVISION

Drawn CL. B.

Revised

Title LSI-50

Approved D. Epstein

Dwg No ADI00159

Rev G

DRAWING SIZE B

DWG NO SD100159 SH 1 of 6 REV C

## REVISIONS

| | | | |
|---|---|---|---|
| A | RELEASED AS DRAWN | | |
| B | ARTWORK LAYOUT REDONE | 11-18-82 | MJC |
| C | REMARK LED (SILKSCREEN ONLY)<br>CHANGED M75 FROM 74LS136 TO 74LS173<br>REMOVED: M68-15 FROM M70-19<br>M56-10 FROM M68-10<br>M56-12 FROM GND<br>R8 FROM VCC<br>ADDED: M69-15 TO M70-19<br>M56-10 TO M68-11<br>M80-9 TO M76-11<br>M25-9,10 TO M18-2 TO M21-4,5<br>R8 TO GND<br>M75-13 TO M70-9<br>M75-14 TO M63-7<br>M62-2 TO M41-8<br>M39-11 TO M74-7<br>M87-12 TO M40-15 | | |
| D | REMOVED: M63-11 FROM M80-5<br>M79-8 FROM M80-15<br>ADDED: M24-13 TO M24-14 (VCC)<br>LOGIC CORRECTION(SCHEMATIC ONLY) | 9/15/83 | MJC |
| E | ECO NO. 0159-01 | 3-18-83 | MJC |
| F | ECO NO. 0159-02 | 7-11-83 | MJC |
| G | ECO NO. 0159-03 | 12-19-83 | MJC |

## NOTES :

1. UNLESS SPECIFIED:
   A. ALL RESISTOR VALUES ARE IN OHMS AND ARE ¼ W ± 5%
   B. ALL CAPACITOR VALUES ARE IN MICROFARADS
2. CPU SIGNALS ARE NOT DESIGNATED WITH COORDINATES



ALLOY ENGINEERING COMPANY

Date 12-15-81 | COMPUTER PRODUCTS DIVISION | drawn | revised

Title LSI-50

Approved | DWG NO SD100159 | REV G

BRUNING 44-1313-30116

ERR*
M52
74LS244
LED
+5V
CL.2
5.0688
74LS04
X2*
M66
BDMA(3A6)
WB F/F(6B6)
8085
CPU
X1
SID
READY
RESET
B-INT
(1A6)
TXEMT
(6A5)
INT 5.5
(4A3)
RST 5.5
RST 6.5
RST 7.5
INT 7.5
WC2
(1C4)
M53
74LS27
TRAP
INTR
TCLR
(3B8)
DACK 2 G
(6C7)
HOLD
HLDA
CLK
M35
ADØ
AD1
AD2
AD3
AD4
AD5
AD6
AD7
ALE
ALE*
(3C4)
74LS373
M36
AØ
A1
A2
A3
A4
A5
A6
A7
A15
A14
A13
A12
A11
A10
A9
A8
RD
WR
I/OM
SI
SOD
RAM CTRL
(3C2)
R8 1K
ENBR
(3B4)
CLK*
M51
74LS240
ENB BUS
(4C4)
BADD G
(5A2)
RESET*
(5C2)
IOSEL*
M50
74LS257
SELB
R10 2K
R9 2K
RAM CTRL(3C2)
SELOR(3B4)
ADDINC*(4B6)
IO OR(3C8)
IO OR(3C8)
SELOR(3B4)
MRD(3C4)
MEMWR*
(3C1)
AEN*
M51
74LS240
SYNC OR(5B6)
ALE*
(3C4)
74LS373
M49
DMAC
8257
CLK
RESET
HLDA
HRQ
AEN
MEMR*
I/OR*
MEMW*
I/OW*
READY
TC
DREQ Ø
DREQ 1
DREQ 2
DREQ 3
M6
CE
DO
D1
D2
D3
D4
D5
D6
D7
ADSTB
DACKØ
DACK 1
DACK 2
DACK 3
DMA REQ
(5B5)
BRPLYL(3B1)
DACKØ*
(3C6)
M26
74LS11
DACKØ1OR*
DACK Ø1 OR
(1A5)
DACKI2
(2D3)
RDY OR
M25
74LS10
RPLY*
(4D2)
DSB*
(2D2)
DRY*
(6B7)
DREQ2G
(6C7)
SYNR2
M25
74LS10
+5VO
TAPE G*
IWGATE
(6D7)
ALE*
(3C3)
M67
74LS10
T-BUF(6A8)
TAPEDAT*
(6A8)
DACK 2 G (6C7)
DSB*
DACKI2
(3C4)
DMAC
(2A3)
M67
74LS10
M51
74LS240
RDY OR(2A6)
DSB G*(6B4)
M52
74LS244
A4*
M51
74LS240
ADDINC*
(4B7)



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I/ORW*
74LS138
M69
A0 A1 A2
0 RDY*(6A4)
1 MTCHB*(1C3)
2 MTCLB*(1B3)
3 CB*(6D1)
4 MTSLB*(3A5)
5
6 ADREQ(4B8)
7 INGATE(5A8)
G1 G2A G2B

IOSEL*4 (2B4)
IOSEL*2 (2C4)
IO OR
M67
74LS10

DACK0* (2A3)
M22
74LS04
MEMWR* (3C1)

MTSHB*
74LS374
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
1D 2D 3D 4D 5D 6D 7D 8D
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
D8 D9 D10 D11 D12 D13 D14 D15
CLK OC
M41

A13 A14 A15
M20
74LS10

M23
74LS11

A12
M22
74LS04
M23
74LS11

M65
74LS27

M22
74LS04

RAM CTRL
M5
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13
AL0 AL1 AL2 AL3 AL4 AL5 AL6 AL7
AH0 AH1 AH2 AH3 AH4 AH5 AH6 AH7
CS WR RD
8203
CUT0 CUT1 CUT2 CUT3 CUT4 CUT5 CUT6 CUT7
RAS CAS WE REFRQ SACK XACK
64K BO
RA0 RA1 RA2 RA3 RA4 RA5 RA6 RA7
RAS CAS WE
REFRQ(5C1)
REFRQ(5C2)
RAMSEL (3B3)
X0 X1
20MHZ CL1
R 27 1K
R26 680Ω
CPU(2C6)
IOSEL*1 (2C4)

74LS10
M20
MRD
IOSEL*3 (2B4)
CPU (2C6)
DMAC (2B3)
ALE*
M65
74LS27
TAPEG* (2D2)
ENABH (1A4)

RAM SEL
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
G0 G1 G2 G3 G4 G5 G6 G7
D0 D1 D2 D3 D4 D5 D6 D7
RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7
CK OC
M19
74LS373

MEMWR*
M21
74LS27
DACK0* (3C5)

BMEMWR*
M21
74LS27
DMAC* (2A3)
BRPLYL
M21
74LS27
RPLY* (4D2)

DSB* (2D3)
RSEL
M20
74LS10
REFRQ (5C2)

+5V
SELOR
IOSEL*3 (2B4)
IOSEL*1 (2C4)
M54
74LS10
M24
74LS74
CPU (2B6)
ENB BUS (4D4)
ENBR

2716
M37
CE
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7

MTSLB*
74LS374
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
1D 2D 3D 4D 5D 6D 7D 8D
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
NC RWS WRL SWDN CH BOT SELR NXM
D1 D2 D3 D4 D5 D6 D7
CLK OC
M39
I/ORW*4 (3C7)

INT 5.5 (4A3)
MTS
M74
74LS173
C
1D 1Q
CK
ENB G1 ENB G2
OCM OCN
D0

+5V
R6 2K
DMAC (2B6)
DACK 0/1 OR (1A4)
TCLR
M57
74LS11
PR D Q CK CLR
M62
74LS74
AD0

B-PROL (1B6)
B-PROL (1B5)
MTG
M78
74LS02
M60
74LS04

DIRG
PR D Q CK CLR
M62
74LS74
AD1
SELDIR 1 (1A3)
SELDIR (1C3)
R6 2K
+5V

WC2 (1C4)
CLREQ*
M53
74LS27
INIT* (4A7)
+5V0
R20 220 330
+5V
E3 E1 E2
BWTBT (4C3)

BDMGIL AR2
BDMGOL AS2
B-INT(1A5)
BDMRI ANI
BDOUT*(4C2)
BDIN*(4C2)
BWTBT(4C3)
ENBW(1A2)
BSYNC*(4D3)
SYNC OR(5B6)
RPLY(4D2)
BMDGI L
BMDGOL
INIT L
BDMR L
DOUT H
DIN H
MASTER H
TSYNC H
RSYNC H
RPLY H
REQ H
DATIN L
DATIO L
CTN 4 H
DATNL L
CLK H
TMOUT H
ADREN H
E18 DC010
M48
BDMA
X2*(2C8)
BADD G (5A3)
R11 1K
+5V
C3 1000 PF
WB F/F (6B6)
WC1, WC2 (1B5)
M78
74LS02
M61
74LS27
REC
M60
74LS04
B-BUF1 (1D6)

BRPLY (1B7)
XMT OR
M61
74LS27
XMTB
M60
74LS04
B-BUF1 (1D5)
B-PROL (1B5)
INWD
M60
74LS04
REC OR
M61
74LS27
B-INT (1A6)



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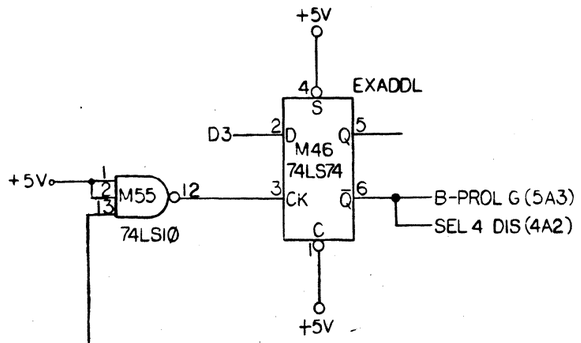


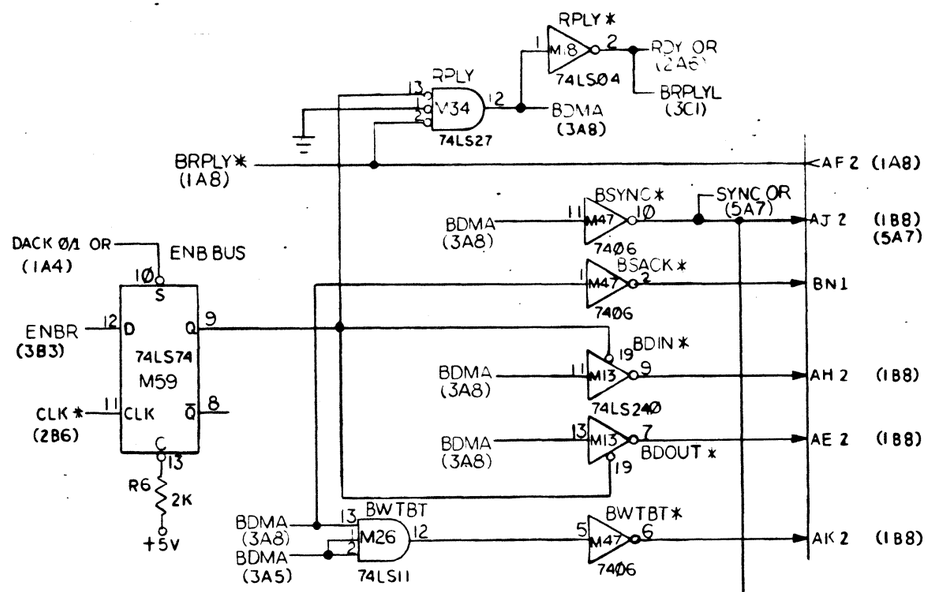


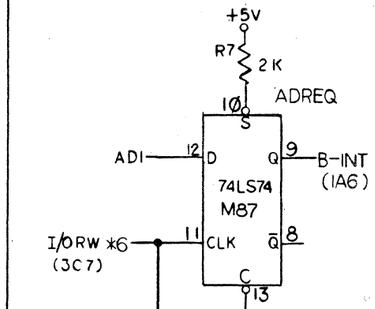


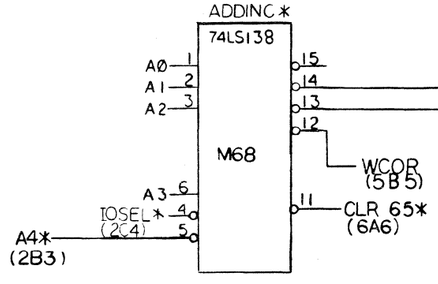


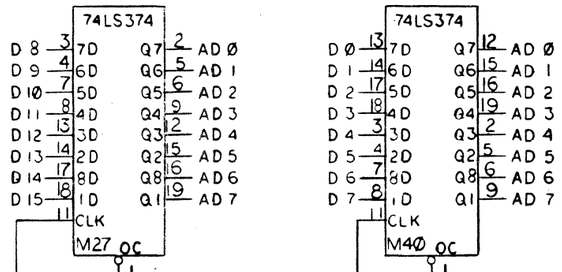


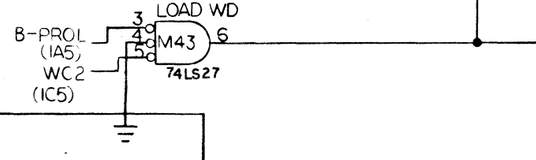


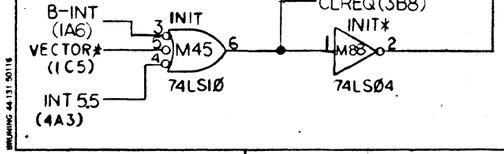


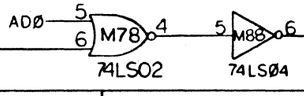


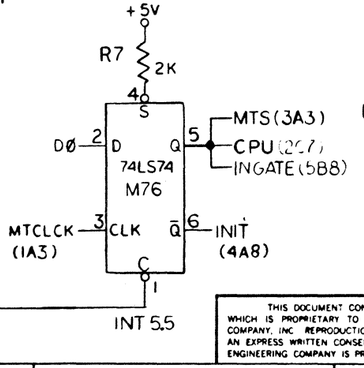


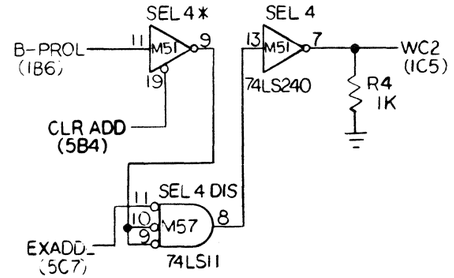




ALLOY ENGINEERING COMPANY 26

Scale — | Drawn —
Date 12-15-81 | COMPUTER PRODUCTS DIVISION | Revised —
Title LSI-50
Approved | Dwg No SD100159 | Rev G

DRAWING 44151-50116

+5V
R25 2K
EXT ADD
D4
D5
74LS161
CLK
LOAD
M77 CLR
EXT ADD G (5B3)
EXT ADD G (5A3)
ADREN*
WC1 (1B5)
74LS04
B-PROL (1B5)
74LS367
D5
D4
74LS240
AC1 BDAL 16
ADI BDAL17
74LS374
ADD SHIFT 1
R14 2K
MTCLCK (1A3)
74Ø6
ADD SHIFT 2
WC2 (1C4)
M38 OC
INWDL
74LS02
74LSØ4
74LS374
D8-15L
MTCHCK (1C2)
M42 OC
WCOR
ADDINC* (4B6)
74LSIØ
WC1 (1B5)
CLR ADD
DI2
74LS74 M58
SEL4* (4B2)
10 DMA REQ
DMAC (2A4)
DACKØ OR (1A4)
MTCHCK (1C3)
SEL6B (1A4)
B-INT (1A6)
INT55 (4A3)
INGATE
74LSI73
IORW*6 (3C7)
M75
AEN* (2B3)
BRPLY* (1A8)
BSYNC* (4D1)
SYNC OR
4LSIØ
BDMA (3A8)
CM2
CN2
CR2
CS2
C1 50 uf 12 VDC
C7 50 uf 12 VDC
C11—C31 CAPACITORS .1 uf @ 100 VDC
GND
P3 3;10
P4 3;10
AJ 1
AM 1
AT 1
BJ 1
BM 1
BT 1
CJ 1
CM 1
CT 1
DJ 1
DM 1
DT 1
AC 2
BC 2
CC 2
DC 2
74LS10
74LS10
REFRQ
RSEL (3B4)
RAMCTRL (SACK) (3C1)
M65
74LS27
RAM CTRL(REFRQ) (3D1)
RESET *
RESET (2B6)
M22
74LSØ4
M26
74LS11
+5V
4164
RAØ
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RAS
CAS
WE
M15 M16 M2 M3 M1 M17 M14 M4
ADØ RDØ
AD1 RD1
AD2 RD2
AD3 RD3
AD4 RD4
AD5 RD5
AD6 RD6
AD7 RD7
+5V
22 BADD
BDAL 8
BDAL 9
BDAL 10
BDAL 11
M44
74LS569
BC1
BD1
BE1
BF1
EXT ADD G
EXT ADD(5C6)
EXT ADD(5C5)
WC 2(1C4)
74LSIØ
B-PROL G
B-PROL(1A6)
EXADDL(4C7)
B-PROL(1B6)
M43
74LS27
BADD G
BDMA (3A6)
RESET (2B6)
BV 1
DV 1
AA 2
BA 2
CA 2
DA 2
+5V

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ALLOY ENGINEERING COMPANY
Scale
Date 12-15-81
COMPUTER PRODUCTS DIVISION
Drawn
Revised
Title LSI-50
Approved
SD100159 Rev G

BRUNING 44-131-30116

R30 2K +5V
AD5
TAPE G * (5C2)
IWGATE
M81
74LS74
B-INT (1A6)
CB*(6C1)
CLRG*F/F (6C3)
CLRGATE*
M57
74LS11
CLRWG* (6B6)
DREQ2G*
M64
74LSIØ
SYNR 2 (2A5)
SPC
BDONE
ADØ AD1 AD2 AD3 AD4 AD5 AD6 AD7
CLK
DOUT
M63
WDIØØ
-Ø5
DCLK EN
SPC*(6C4)
DMAC(2B8)
DACK 2 G
M79
CLRWG*
M83
CLRGATE* (6D7)
DACKI2 (2B3)
R22 1K +5VO
WDIØØ-Ø7
M73
NRZ
CLK
BDONE
BCLR
M53
74LS27
DRY*
M88
74LS04
SYNR 2 (2A5)
T-BUF
74LS244
M72
ADØ AD1 AD2 AD3 AD4 AD5 AD6 AD7
+5VO
TAPE G* (2D1)
TAPEDAT*
M56
74LS11
RGATE* (6C2)
IRGATE*
M86
74LSIØ
+5V
R7 2K
M76
IDCLK*
R29 1K
TXEMT
M85
CPU RST 6.5H
CB*(6C1)
ADDINC*(4B6)
CLR 6 5*
BDMA (3A6)
X2* (2C8)
WB F/F
M82
DSB* (2D2)
DSBG*
M79
R17-5
M8Ø
74LS244
M7Ø
74LS24Ø
P1
23
15
21
R7 2K
CLRG*F/F
M87
CLRGATE* (6D8)
M88
74LSØ4
I/ORW3* (3C7)
CB*
M71
74LS374
AD Ø AD 1 AD 2 AD 3 AD 4 AD 5 AD 6 AD 7
CK
25 29 33 31
CLRGATE* (6D8)
CLR 6 5* (6 A6)
R17 220/330
RGATE*
IRGATE* (6A8)
SPC*
M66
74LS04
SPC (6C8)
I/ORWØ* (3C7)
R12 220
74LS244
B-INT (1A6)
ICACKG
M56
74LS11
M84
74LS74
RDY*
ADØ AD1 AD2 AD7
P1-27

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Date 8-20-82
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Title LSI-50
Approved
Dwg No SDIØØ159 Rev G

DRAWING 44-131-30110

{# P100181A - TMC-1C (CDC) }

{# - PART # -- DESCRIPTION -QTY.- REF.DESIG.}

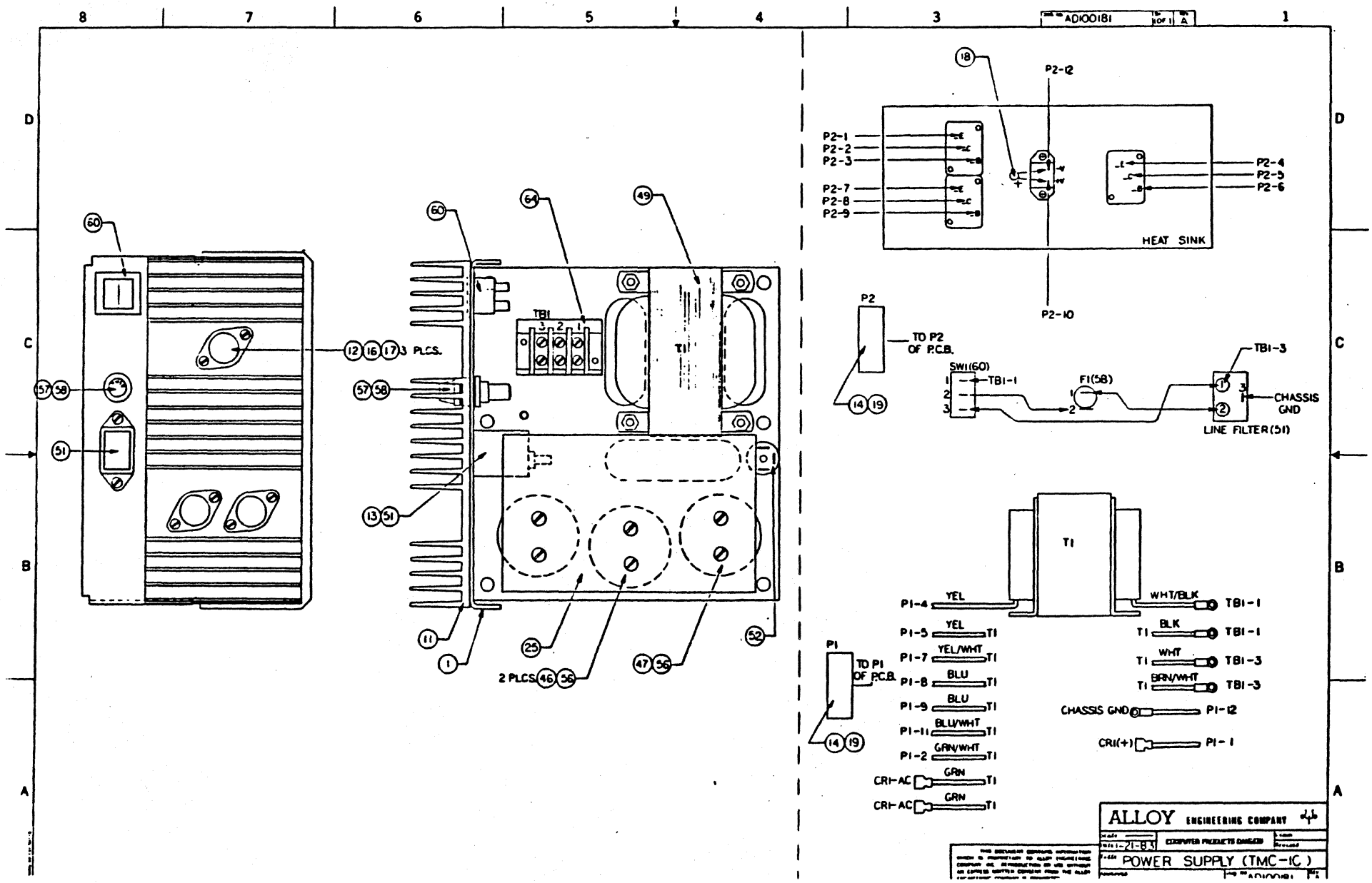
| | | | | |
|---|---|---|---|---|
| 1 | A#PP100182A | PART NOT ON FILE | 1 | CHASSIS P/S TMC-1C |
| 2 | A#PP100183A | PART NOT ON FILE | 1 | CASE TMC-1C |
| 3 | A#PP100184A | PART NOT ON FILE | 1 | COVER TMC-1C |
| 4 | REF | | 0 | |
| 5 | HW8FOOT | #8 RUBBER FOOT | 4 | |
| 6 | C-ITEM | RUBBER EXTRUSION | 50 | |
| 7 | C-ITEM | #8 FLAT WASHER | 2 | |
| 8 | C-ITEM | 8-32X1/2(100C SK)FH | 6 | |
| 9 | C-ITEM | SCR.8-32X3/8 BUT.HD | 4 | |
| 10 | REF | | 0 | |
| 11 | A#PP100001B | PS-15.224 HEATSINK | 1 | HEAT SINK |
| 12 | HW601143051674 | TRANSISTOR INSULATOR | 3 | |
| 13 | DHL-12-OV-5 | 5 VOLT OVP. MODULE | 1 | |
| 14 | CN09507121 | CRIMP TYPE CONN. 12 POS. | 2 | P1,P2 |
| 15 | HW4876(MK) | MOUNTING KIT | 3 | |
| 16 | HW8909NB(TC) | TRANSISTOR COVER | 3 | |
| 17 | TR2N5875 | TRANSISTOR | 3 | |
| 18 | CF1MF@35V | CAPACITOR 1UFD @ 35V | 1 | |
| 19 | C-ITEM | CRIMP PIN(MOLEX) | 24 | |
| 20 | C-ITEM | #18 AWG WIRE(RED) | 50 | |
| 21 | C-ITEM | #18 AWG WIRE(WHT) | 50 | |
| 22 | C-ITEM | #18 AWG WIRE(BLK) | 50 | |
| 23 | C-ITEM | SCR.6-32X5/16" | 2 | |
| 24 | REF | | 0 | |
| 25 | A#PB100002C | P15.224 REGULATOR CARD | 1 | P.C.B. |
| 26 | C-ITEM | TEST PT.(TP1;TPG) | 2 | |
| 27 | CFTE-1305 | CAPACITOR 20 UFD @ 50V | 2 | |
| 28 | DI1N5624 | DIODE | 4 | |
| 29 | RF10W.1 | RESISTOR FIXED | 1 | |
| 30 | RF10W.2 | RESISTOR FIXED | 2 | |
| 31 | RF.25W100 | RESISTOR FIXED | 1 | |
| 32 | RF.25W270 | RESISTOR FIXED | 2 | |
| 33 | RF.5W47 | RESISTOR FIXED | 3 | |
| 34 | RV100 | RESISTOR VARIABLE | 1 | |
| 35 | CF.1@100 | CAPACITOR .1UFD @ 100 | 1 | |
| 36 | VRLM317KC | VOLTAGE REGULATOR VAR. | 1 | |
| 37 | VR7824UC | VOLTAGE REGULATOR +24 | 2 | |
| 38 | TRTIP32 | TRANSISTOR | 4 | |
| 39 | CN10182032 | TRANSISTOR SOCKET | 7 | |
| 40 | CN09601121 | CONNECTOR 12 POS. | 3 | |
| 41 | CN09523061 | CONNECTOR RT ANGLE 6 POS. | 1 | |
| 42 | CN09601061 | CONNECTOR 6 POS. LOCKING | 1 | |
| 43 | CFTE-1133 | CAPACITOR 50 UFD @ 12V | 1 | |
| 44 | C-ITEM | NYLON RIVET | 7 | |
| 45 | REF | | 0 | |
| 46 | CF36D602G050BB2A | CAPACITOR 6000 @ 50V | 2 | |
| 47 | CF36D213G015BB2A | CAPACITOR 21000 @ 15V | 1 | |
| 48 | A#PP100017A | STANDOFF PC CARD | 1 | |
| 49 | A#PP100007C | PS-15.224 TRANSFORMER RWK | 1 | |
| 50 | C-ITEM | CARD GUIDE PCB | 50 | |
| 51 | CS6AMP | AC LINE FILTER 6 AMP | 1 | |
| 52 | DIPKC05F | DIODE | 1 | |
| 53 | C-ITEM | 10-32X1/4 SCREW | 6 | |
| 54 | HW.250(QD) | QUICK DISCONNECT | 7 | |
| 55 | HW.250(RL) | RING LUG | 2 | |

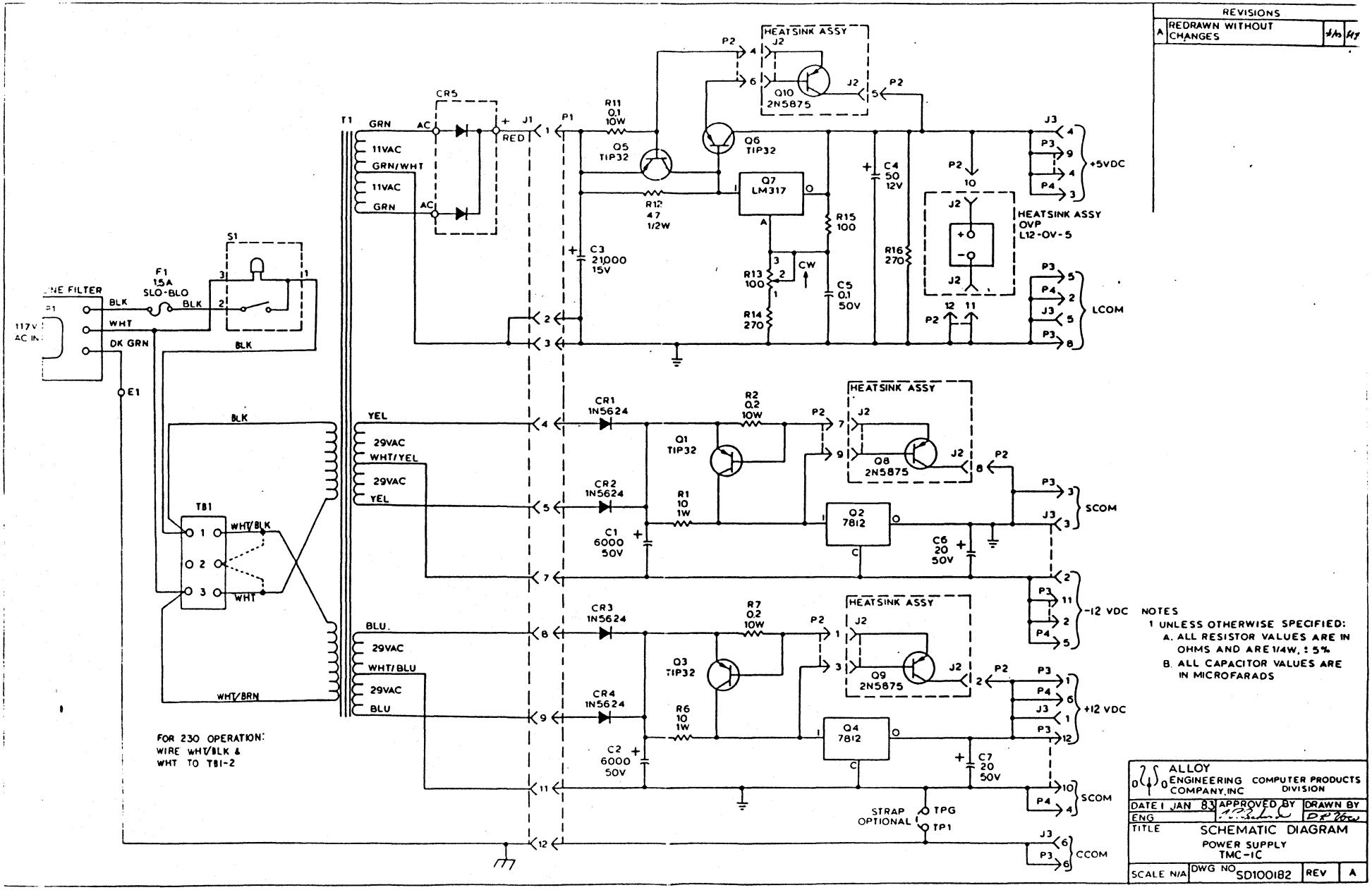
{PARTS LIST RUN - 01/18/83}
{# P100181A - TMC-1C (CDC) }

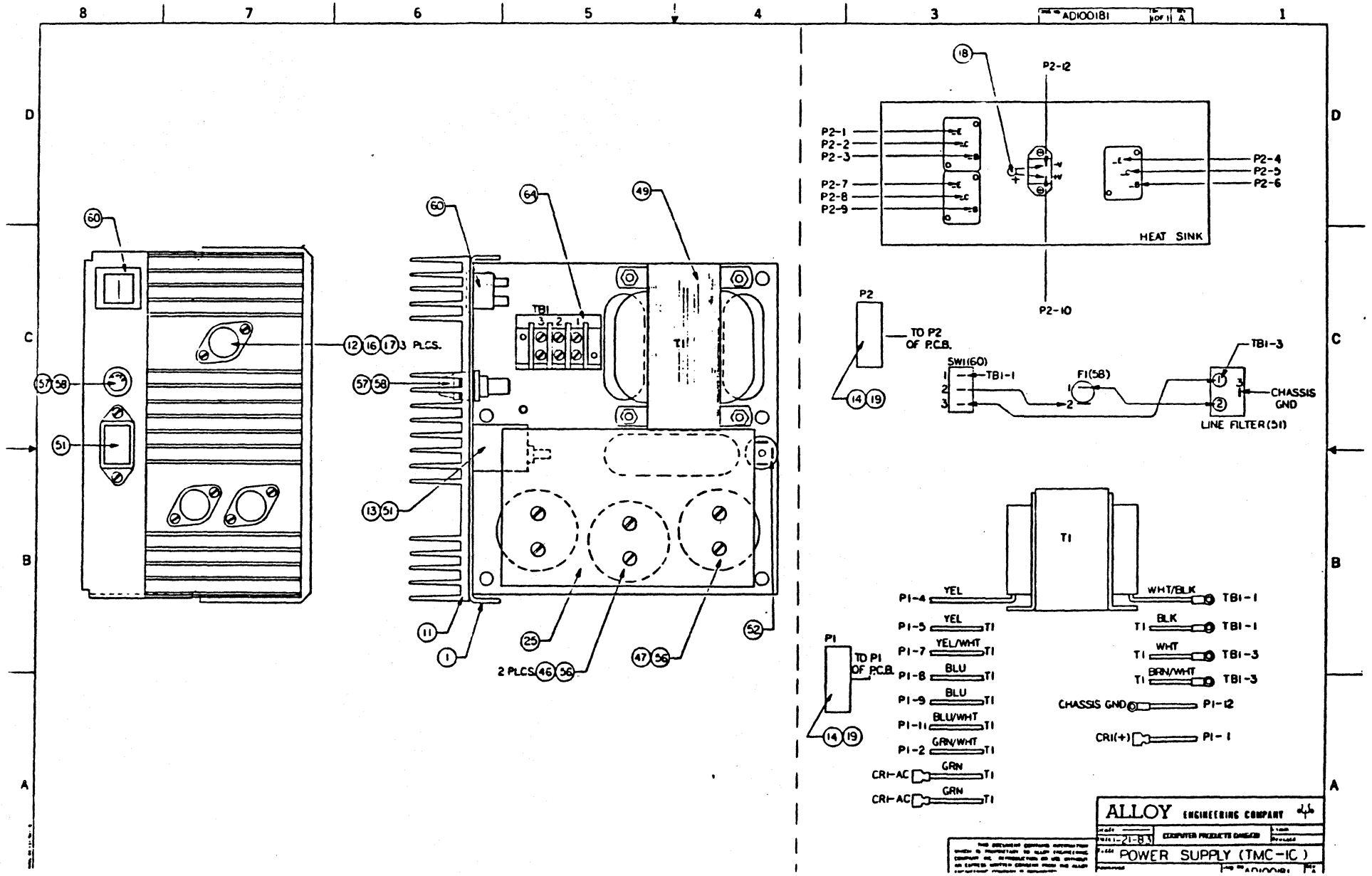
{# - PART # -- DESCRIPTION -QTY.- REF.DESIG.}

| | | | | |
|---|---|---|---|---|
| 56 | HW4586-48(CM) | CAPACITOR CLAMP | 3 | |
| 57 | HW31302.5(FUSE) | 2.5 AMP FUSE | 1 | |
| 58 | HW342022(FH) | FUSE HOLDER | 1 | |
| 59 | LCBELD17250 | MOLDED LINE CORD | 1 | |
| 60 | SW260012E | DBL POLE SGL THROW SW | 1 | SWITCH ON/OFF |
| 61 | C-ITEM | 6-32 KEP NUT | 12 | |
| 62 | C-ITEM | 8-32 KEP NUT | 7 | |
| 63 | HW0380250(CC) | CABLE CLAMP | 1 | |
| 64 | HW3POS(TB) | TERMINAL BLOCK | 1 | |
| 65 | C-ITEM | SCREW 4-40X1/2 | 2 | |
| 66 | C-ITEM | 4-40 KEP NUT | 2 | |
| 67 | C-ITEM | SCREW 6-32X1/2" | 3 | |
| 68 | C-ITEM | SCREW 8-32X1/2" | 8 | |
| 69 | C-ITEM | #18 AWG WIRE | 200 | |
| 70 | CN1-480702-0 | PART NOT ON FILE | 1 | CONN.PRIME DRIVE |
| 71 | HW350547-1 | PART NOT ON FILE | 4 | AMP CR.PIN(PRIME) |
| 72 | CN09507061 | CRIMP TYPE CONN. 6 POS. | 1 | P4 |
| 73 | REF | | 0 | |
| 74 | REF | | 0 | |

ASSEMBLY HOURS --- .5
TEST HOURS ------- .5


8
7
6
5
4
3
1
A
B
C
D
AD100181
60
64
49
TB1
T1
12 16 17 3 PLCS.
57 58
51
13 51
11
1
25
2 PLCS 46 56
47 56
52
18
P2-12
P2-1
P2-2
P2-3
P2-7
P2-8
P2-9
P2-4
P2-5
P2-6
HEAT SINK
P2-10
P2
TO P2 OF P.C.B.
14 19
SW1(60)
TB1-1
F1(5B)
TB1-3
CHASSIS GND
LINE FILTER(51)
P1
TO P1 OF P.C.B.
P1-4 YEL
P1-5 YEL
P1-7 YEL/WHT
P1-8 BLU
P1-9 BLU
P1-11 BLU/WHT
P1-2 GRN/WHT
CR1-AC GRN
CR1-AC GRN
WHT/BLK TB1-1
BLK TB1-1
WHT TB1-3
BRN/WHT TB1-3
CHASSIS GND P1-12
CR1(+) P1-1
ALLOY ENGINEERING COMPANY
COMPUTER PRODUCTS DIVISION
DATE 1-21-83
POWER SUPPLY (TMC-IC)


REVISIONS
A REDRAWN WITHOUT CHANGES
T1
CR5
S1
F1 1.5A SLO-BLO
LINE FILTER
117V AC IN
BLK
WHT
DK GRN
E1
GRN
11VAC
GRN/WHT
11VAC
GRN
AC
RED
J1
P1
R11 0.1 10W
Q5 TIP32
Q6 TIP32
HEATSINK ASSY
Q10 2N5875
R12 47 1/2W
Q7 LM317
R15 100
R13 100 CW
R14 270
C3 21000 15V
C4 50 12V
C5 0.1 50V
R16 270
HEATSINK ASSY OVP L12-OV-5
+5VDC
LCOM
YEL
29VAC
WHT/YEL
29VAC
YEL
CR1 1N5624
CR2 1N5624
R2 0.2 10W
Q1 TIP32
Q8 2N5875
R1 10 1W
C1 6000 50V
Q2 7812
C6 20 50V
SCOM
-12 VDC
BLU.
29VAC
WHT/BLU
29VAC
BLU
CR3 1N5624
CR4 1N5624
R7 0.2 10W
Q3 TIP32
Q9 2N5875
R6 10 1W
C2 6000 50V
Q4 7812
C7 20 50V
+12 VDC
SCOM
STRAP OPTIONAL
TPG
TP1
CCOM
TB1
WHT/BLK
WHT
WHT/BRN
FOR 230 OPERATION:
WIRE WHT/BLK &
WHT TO TB1-2
NOTES
1 UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4W, ± 5%
B. ALL CAPACITOR VALUES ARE IN MICROFARADS
ALLOY ENGINEERING COMPANY, INC COMPUTER PRODUCTS DIVISION
DATE 1 JAN 83
APPROVED BY
DRAWN BY
ENG
TITLE SCHEMATIC DIAGRAM
POWER SUPPLY
TMC-1C
SCALE N/A
DWG NO SD100182
REV A


ADI00181
HEAT SINK
P2-1
P2-2
P2-3
P2-7
P2-8
P2-9
P2-4
P2-5
P2-6
P2-12
P2-10
P2
TO P2 OF P.C.B.
SWI(60)
TBI-1
FI(58)
TBI-3
CHASSIS GND
LINE FILTER(51)
TBI
TI
12 16 17 3 PLCS.
2 PLCS.
P1
TO P1 OF P.C.B.
P1-4 YEL
P1-5 YEL
P1-7 YEL/WHT
P1-8 BLU
P1-9 BLU
P1-11 BLU/WHT
P1-2 GRN/WHT
CRI-AC GRN
CRI-AC GRN
WHT/BLK TBI-1
BLK TBI-1
WHT TBI-3
BRN/WHT TBI-3
CHASSIS GND P1-12
CRI(+) P1-1
ALLOY ENGINEERING COMPANY
POWER SUPPLY (TMC-IC)

ALLOY

Computer Products

A Division of Alloy Engineering Company, Inc.

# STANDARD TERMS & CONDITIONS

1. **GENERAL** - An order constitutes a contract between **Alloy-CPD** and the Buyer when accepted in writing by **Alloy-CPD** at its home office as shown on the face hereof. A contract resulting from the acceptance of an order may be cancelled or altered by the Buyer only if agreed to in writing by **Alloy-CPD** at its home office subject to payment of associated charges necessary to protect **Alloy-CPD** from loss. Any of the terms or provisions of the Buyer's order which are in any way inconsistent with or in addition to the terms and conditions contained herein shall not be binding on either party unless expressly accepted in writing by its authorized representatives.

2. **DELIVERY** - Shipping dates are based upon prompt receipt of all necessary documents from the Buyer. Shipments are scheduled after acceptance of an order in accordance with the Buyer's requirements. Unless specifically stated to the contrary, however, where existing priorities and schedules prevent strict compliance with requested delivery dates, orders are entered as close as possible to the requested date and the Buyer is advised of the actual shipping schedule. **Alloy-CPD** shall not be liable for delays in delivery or other default by reason of any occurrence or contingency beyond its reasonable control, nor shall it be liable for any special or consequential damages caused by any delay in delivery or failure to manufacture or deliver.

3. **PRICES** - **Alloy-CPD** certifies that the prices contained herein are as favorable to the Buyer as those extended to any other customer in effect on the date of this document for substantially similar items and quantities under similar conditions. The prices stated are exclusive of any federal, state, municipal or other government tax now or hereinafter imposed upon the production, storage, sale, transportation or use of the products described herein. Such taxes applied directly to the sale hereunder shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide a tax exemption certificate acceptable to the taxing authorities. Note: On sales outside the U.S., all required import duties, licenses & fees shall be payable by the Buyer in addition to the stated prices.

4. **PAYMENT** - Unless otherwise specifically stated to the contrary, the terms of payment shall be **NET - 30 DAYS** from the date of shipment of the hardware. In case of partial shipments, pro-rata payments shall become due on each shipment. On overdue accounts, a finance charge shall be charged and payable at the rate of two percent per month on the amount of the unpaid balance. **Alloy-CPD** may require full or partial payment in advance if, in its judgement, the financial condition of the Buyer at any time prior to shipment so warrants.

5. **WARRANTY** - See attached **Limited Warranty** statement.

6. **CHANGES** - By mutual agreement the order may be suspended or changes may be made in quantity, designs, specifications, place of delivery, methods of shipment and packaging. If any such change causes an increase or decrease in the price of the equipment or in the time required for performance, **Alloy-CPD** shall promptly notify the Buyer and assert its claim within thirty days from the date the change is agreed upon, and an equitable adjustment shall be made. In any event, changes shall not be binding upon nor be put into effect by either party unless confirmed in writing by its appropriate representative.

7. **TERMINATION** - The Buyer may terminate work under this Agreement, either in whole or in part. Notice of termination under this paragraph must be submitted by the Buyer, in writing, sixty days in advance of its effective date. During that final sixty days, deliveries shall continue in accordance with the existing delivery schedule. Where special equipment or services are involved, the Buyer shall be responsible for all related work in process; however, **Alloy-CPD** shall take all reasonable steps to mitigate damages immediately upon receipt of said termination notice and shall notify subcontractors to do likewise.

8. **PROPRIETARY INFORMATION** - All proprietary information which is specifically designated as such, disclosed by either party to the other in connection with this order, shall be used solely for installation, operation, maintenance and support of equipment furnished under this order only and shall be protected by the recipient from disclosure to others with the same degree of care as that which is accorded to its own proprietary information. Information will not be subject to this provision if it is or becomes a matter of public knowledge without the fault of the recipient party, if it was a matter of written record in the recipient party's files prior to disclosure to it by the other party, if it was or is received by the recipient party from a third person under circumstances permitting its disclosure or its disclosure is required by any United States Governmental Agency.

9. **PATENT PROTECTION** - **Alloy-CPD** shall undertake at its own expense, the defense of any suit or proceeding brought against the Buyer in so far as such suit or proceeding is based upon a claim that any equipment made to **Alloy-CPD** design and furnished hereunder constitutes an infringement of any patent of the United States, on condition that the Buyer promptly notifies **Alloy-CPD** in writing of such suits or threats thereof and cooperates by giving **Alloy-CPD** any requested authorization, information and assistance for the defense of same. The foregoing shall not apply in instances in which normally non-infringing **Alloy-CPD** equipment is rendered infringing by the Buyer's alteration, combination with other equipment, or use of said equipment. The sole obligation of **Alloy-CPD** shall be full compliance with this clause.

10. **APPLICABLE REGULATIONS** - **Alloy-CPD** certifies that it complies with the requirements of the Fair Labor Standards Act of 1938 as amended, the Walsh-Healy Public Contacts Act and Equal Opportunity Employment as defined in Executive Order Number 11246.

If the Buyer's order is placed as a subcontract under a United States Government prime contract, only those clauses of the Armed Service Procurement Regulation that are required by Federal law are hereby incorporated by this reference, except as a representation contained or incorporated herein shall be construed as a representation that **Alloy-CPD** offers its standard products on a cost reimbursement basis or that **Alloy-CPD** makes any representation regarding the cost of standard products.

11. **ENFORCEABILITY** - No delay or failure of either party in exercising any right hereunder and no partial or single exercise hereof shall be deemed to constitute the waiver of such right or any other rights hereunder.

If any provisions of this Agreement shall become inoperative or unenforceable as applied in any particular case or becomes in conflict with any other provisions hereof, such circumstances shall not have the effect of rendering the provisions in question invalid, inoperative or unenforceable in any other case or circumstances. The invalidity of any one or more phrases, sentences, clauses or sections in this Agreement contained shall not affect the remaining portion of this Agreement or any part thereof.

12. **AGREEMENT** - This Agreement supersedes and cancels all prior agreements, if any, by the parties hereto and constitutes the entire understanding between the parties with respect to the subject matter hereof. Any assignment of this Agreement, or any of the rights hereunder by the Buyer shall be void without written consent of **Alloy-CPD.** All disputes and controversies arising out of the performance of this Agreement shall be settled by arbitration, at the American Arbitration Association in Boston, Mass. in accordance with the laws of the Commonwealth of Massachusetts.

# LIMITED WARRANTY

**ALLOY ENGINEERING COMPANY, INC., Computer Products Division (Alloy-CPD),** in recognition of its responsibility to provide quality products, components, and workmanship, warrants each product it manufactures and each part and component thereof installed by **Alloy-CPD** (except those excluded by Para. 4 below) to be free from defects in material and workmanship for a period of **120 DAYS** after shipment. This warranty is subject to the terms and conditions below:

1. **WARRANTOR** - This warranty is granted by Alloy Engineering Company, Inc., 12 Mercer Road, Natick, MA 01760 [Telephone (617) 655-3900 or TWX: 710-346-0394]

2. **PARTIES TO WHOM WARRANTY IS INTENDED** - This warranty shall extend to any owner and to any person to whom the warranted system is transferred during the duration of this warranty.

3. **PARTS AND COMPONENTS COVERED** - All parts and components of the warranted system manufactured and/or installed by **Alloy-CPD** are covered by this warranty, except those parts and components excluded by Para. 4 below.

4. **PARTS AND COMPONENTS NOT COVERED** - The following components are not covered by this warranty: (a) any part or component that shall have been subject to abnormal electrical or mechanical abuse, negligence or accident (as determined by **Alloy-CPD**); (b) any part or component that shall have deteriorated from ordinary wear and tear, such as paint; (c) expendable items that would normally be replaced within the warranty period, such as Magnetic Tapes and Cartridges.

5. **PROCEDURE FOR OBTAINING PERFORMANCE UNDER THIS WARRANTY** - In order to qualify under this warranty, the owner must notify **Alloy-CPD** within ten days after discovery of the defect and receive authorization by **Alloy-CPD** to return the defective system or component to **Alloy-CPD.** Upon receipt of such system or component, if it is found not to be defective in material or workmanship, **Alloy-CPD** shall notify the owner of the fact and request instructions for its return to the owner. All cost of transporting the system or component to and from **Alloy-CPD** shall be paid by the owner.

6. **REMEDY** - If, within the duration of this warranty, a system or component covered by this warranty is returned to **Alloy-CPD** and proves to be defective in material or workmanship, **Alloy-CPD** shall (at its option) repair or replace the defective item at its expense. Replacement of a defective component pursuant to this warranty shall be warranted for the remainder of the warranty period applicable to the replaced component. After the expiration of this warranty, a system or component return to **Alloy-CPD** will be repaired and returned at a cost commensurate with the parts and labor required; in no case will this charge exceed one hundred dollars ($100.00) without prior notification and approval of the owner.

7. **DESIGN CHANGES** - **Alloy-CPD** reserves the right to make changes in the design or material of its products without incurring any obligation to incorporate such changes in any product previously manufactured. From time to time, however, **Alloy-CPD** will issue Applications Notes to its customers to notify them of product improvements which may be retrofitted at the option of the customer.

8. **EXCLUSIONS AND DISCLAIMERS** - This warranty does not extend to normal preventative maintenance procedures, nor to any defect due to negligence of others, failure to operate or maintain the system in accordance with instructions furnished, electrical or mechanical abuse, accidents, alterations, or ordinary wear and tear. This warranty and the remedy provided herein are exclusive and expressly in lieu of all other warranties expressed or implied either in fact or by operations of law, statutory or otherwise, including warranties or merchantability or fitness for use. Under no circumstances will **Alloy-CPD** assume liability for special, consequential, or punitive damages arising from or in any way connected with use of its products.