FUTUREBUS+ GETS READY IN BUSCON'S BACKROOM

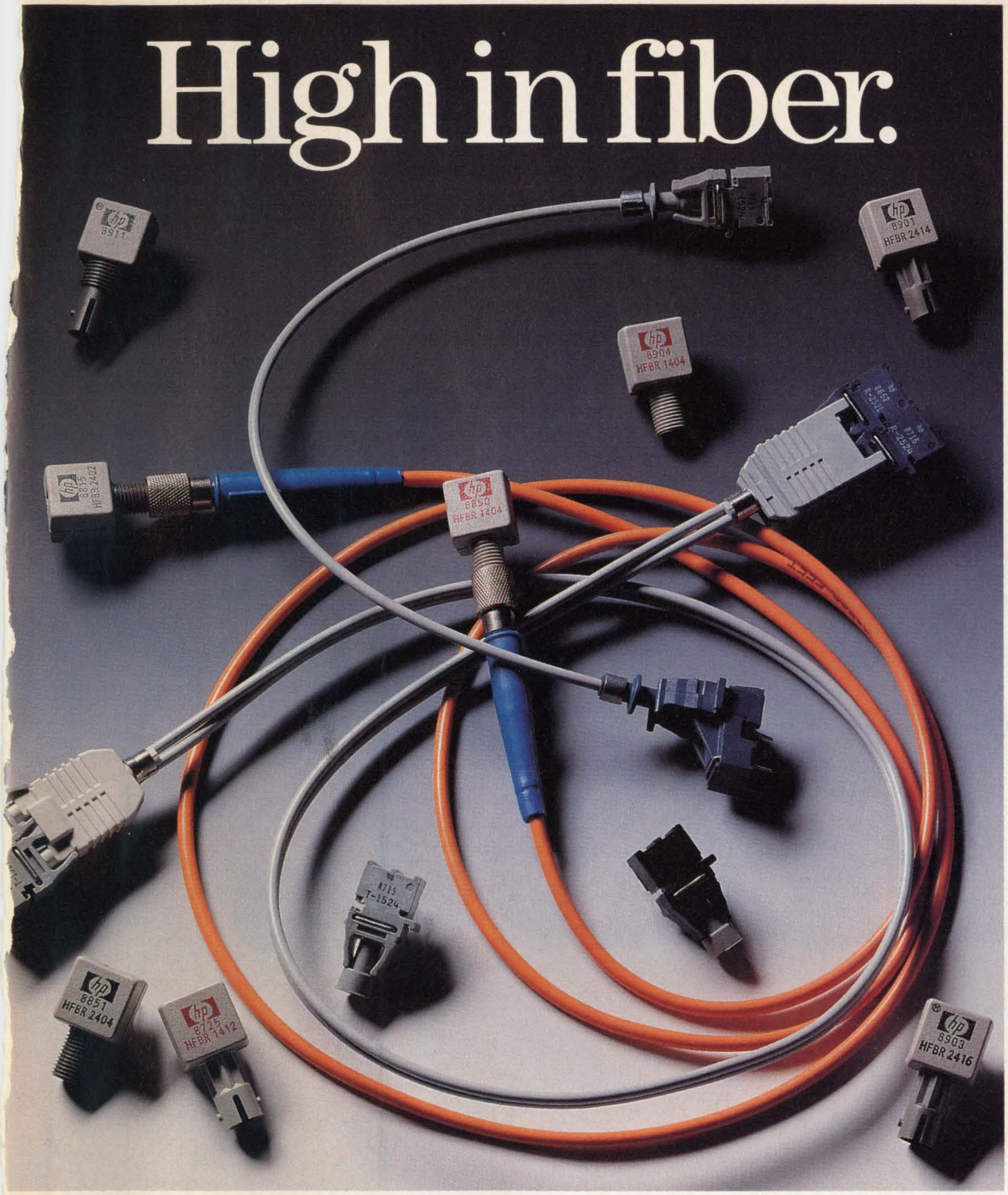
EMBEDDED CONTROLLER RUNS INSTRUCTIONS IN PARALLEL

ELECTRONIC DESIGN

A PENTON PUBLICATION U.S. $5.00 SEPTEMBER 14, 1989

DIGITIZE WIDEBAND AUDIO WITH A DUAL 18-BIT ADC CHIP

SPECIAL REPORT: OP AMPS GROW IN VARIETY



At HP, we've got all the fiber-optic components you need. And all at a price that's good for your health.

Our HBFR-0400 family of 820 nm fiber-optic transmitters and receivers provides cost-effective fiber-optic links of up to 4Km. With no assembly time.

The 125 MHz analog receiver is designed for high-speed data links, providing data rates of up to 150MBd. And its wide dynamic range is compatible with the IEEE 802.3 FOIRL standard.

The transmitters are specified with four types of fiber and are designed for high-speed transmission, such as with TAXIchip links.

Both the transmitter and receiver are compatible with popular ST and SMA connectors.

HP's HFBR-0501 Versatile Link family includes a complete line of 665 nm fiber-optic transmitters, receivers, connectors and cable. All designed to provide you with a low-cost solution.

Our wide range of plastic cable and connector options includes simplex, duplex, latching and non-latching. Which offers you a cost-effective alternative to copper wire while it provides design flexibility.

Best of all, they're from HP. So you're always assured of HP's commitment to excellence in service, support and reliability.

For a free information package describing our full line of fiber-optic solutions, call **1-800-752-0900, ext. 219R.** It's the best way to get your fiber.

There is a better way.

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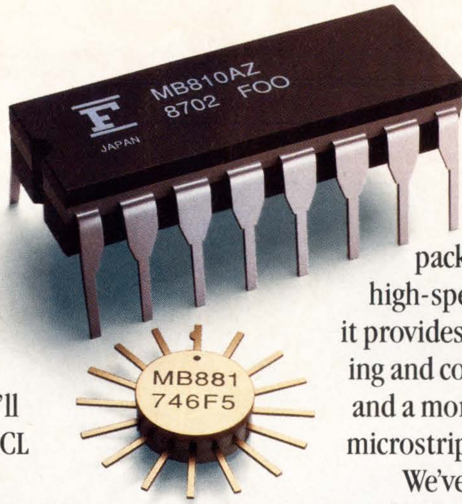
CIRCLE 26

Going fast.

Introducing ultra high-speed ECL logic packaged to meet your needs.



If the race belongs to the swift, then you're in fast company with Fujitsu Microelectronics. Because we'll give you all the high-speed ECL logic you need to win.

Whether you choose the 3GHz MB880 series, the 1.5GHz MB810 series, or our complementary 1-2.5GHz master slice series, the E128H, E32 and E128, you get the fastest UHECL logic available. And you get it packaged to go. Because it's on the shelf now.

You can even mix and match the MB880 and MB810 discrete logic series with the E128H, E32 and E128 master slice series for optimum system performance and cost.

Take the 3GHz MB880 discrete logic series and associated 2.5GHz E128 UHECL master slice array, for example. They were designed for ultra high-performance systems where speed is an absolute must.

Which makes them ideal for fiber-optics, telecommunications, video-graphics processing and high-speed computing applications.

When it comes to packaging for ultra-speed performance, we've got the MB880 and the master slice series all wrapped up in a compact, circular, ceramic flat package with radial leads.

This unique package is designed for ultra high-speed applications. And it provides you with easier mounting and cooling, lower crosstalk and a more efficient interface to microstrip transmission lines.

We've even made it easy for you to check out our incredibly fast ECL process speeds for yourself. Our optional ECL test kit provides you with hardware to check out the performance of the circular ceramic flatpackage devices.

The 1.5GHz MB810 discrete logic series and 1.0GHz E128H and E32 master slice series are designed for use in high-speed test equipment, instrumentation and general logic applications. And they're conventionally packaged in 16-pin cerdip and ceramic flat-packs to provide performance at a lower cost.

What's more, you don't have to worry about compatibility, either. Because the MB880 and MB810 discrete logic series, and the E128H, E32 and E128 master slice array series are logic-level compatible with ECL 10K and 10KH series.

Best of all, they're from Fujitsu Microelectronics. The partner you can count on. Now and in the future. Providing you with the edge you need to always stay ahead.

If you'd like to know more about the UHECL series, call 800/642-7616. We'll show you how to fall in with a fast crowd.

FUJITSU

Every step of the way.℠

FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
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CIRCLE 27

SEPTEMBER 14, 1989 VOL. 37, NO. 19

ELECTRONIC DESIGN

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

Cover illustration by Jim Kinstrey

COMING NEXT ISSUE
- Special Report on DSP
- Latest developments in designing high-speed pc boards
- Special Reference Section: Interconnections & Packaging

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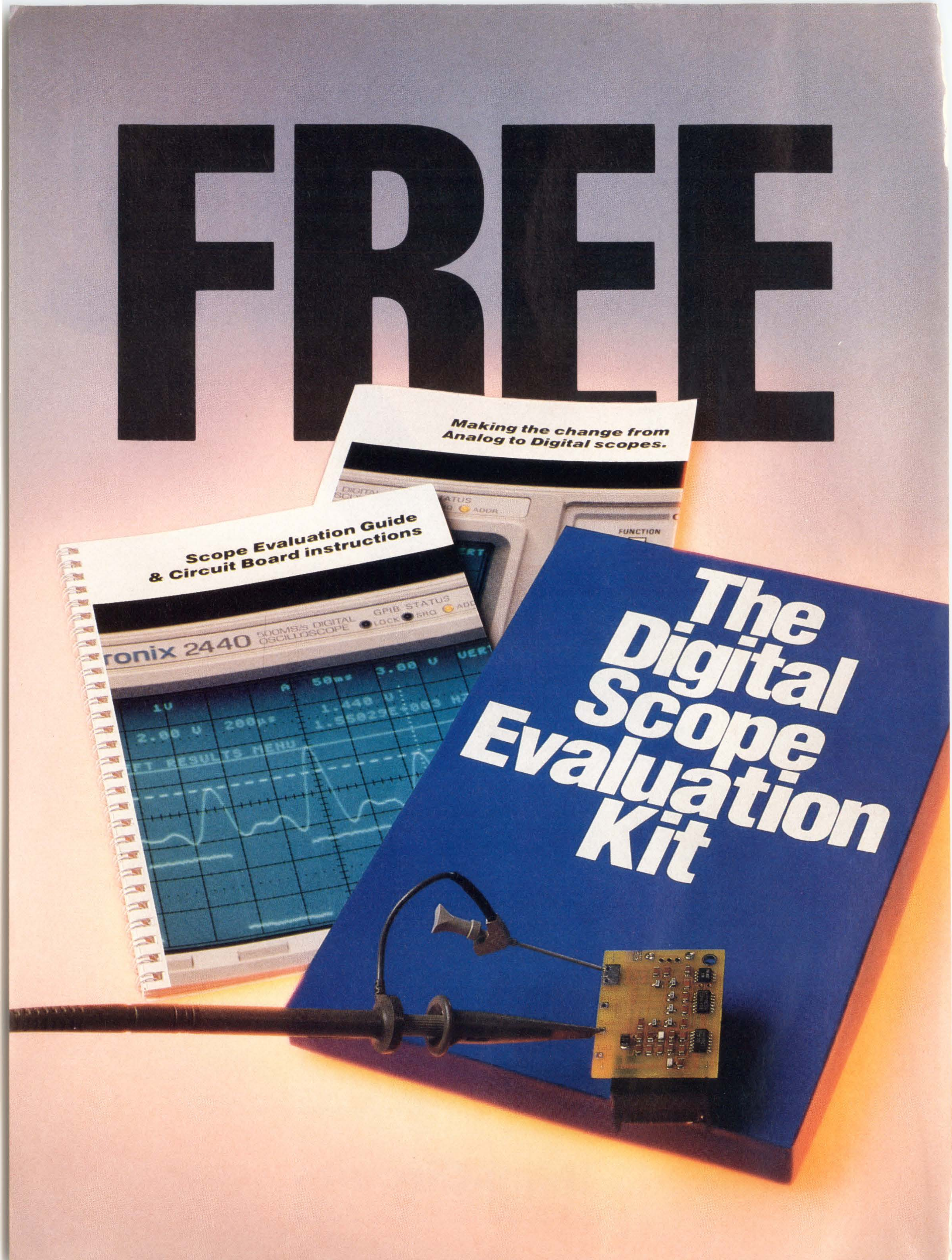
FREE
Making the change from Analog to Digital scopes.
Scope Evaluation Guide & Circuit Board instructions
The Digital Scope Evaluation Kit

Who was the second person

Captain James Fitzgerald was the second person to break the sound barrier at Muroc Dry Lake, on February 24, 1948.

to break the sound barrier?

Someone worked every bit as hard as Chuck Yeager and came in second. The sad truth is, no matter how fast you go, getting there second isn't fast enough.

The same holds true in the marketplace.

That's why AMD concentrates on complete design solutions that cut product development time. So your product won't be obsolete before it's shipped.

Take our 32-bit RISC microprocessor, the 29K.™ At 17 MIPS, it's at the heart of some of the fastest, most powerful equipment now being built.

And everything you need to get to work is here. Today. From silicon to tools for hardware and software development. From AMD or any of 40 Fusion29K™ partners.

Which makes it easy for you to go out and get your share of the profits before anyone else gets off the ground.

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Or take AMD and fly to market.

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CIRCLE 30

THE SHOCKLEY-ROSE SYNDROME

Sometimes, you can take self-confidence too far. In recent weeks we have been reminded of this by two events: the lifetime ban from baseball placed on Pete Rose, and the death of transistor co-inventor William Shockley. Both men needed an abundance of self-confidence to accomplish what they did in their respective fields. Consistently hitting a baseball requires extreme confidence in one's ability, as does applying emerging principles of solid-state physics to a new class of electronic devices. Though Rose and Shockley might both make excellent role models in their fields, each one also took his self-assurance slightly beyond what's proper.

In Rose's case, his arrogance in flouting the rules of baseball is an extrapolation of his supreme self-assurance in his athletic skills. Similarly, Shockley was blessed with great intelligence and keen scientific analytical ability, but he also crossed the line when he stepped away from his knowledge of semiconductor physics and entered the realm of genetics. It's unfortunate that both giants of their respective fields will be remembered not only for their herculean achievements but also for their lapses.

If what we've read is true, Rose wasn't blessed with an outstanding amount of natural talent, but he developed his skill through intense practice—taking hundreds of ground balls a day in fielding practice, hours of extra batting practice, and the like. And he continued practicing his profession long after the time when others couldn't keep pace with the hot new rookie phenoms who sought to take the jobs of older players. Most over-40 engineers can identify with such dedication to the profession, as well as the problems of having to outperform new graduates with a more modern engineering education. Consequently, as a role model, Rose is in some ways a better example for engineers to follow than Shockley was.

Of course, semiconductor technology is one of the cornerstones of the electronics industry. And we all owe a big debt to William Shockley. Let's simply remember him as a pioneer whose work at Bell Laboratories has made life better for all of us.

Stephen E. Scrupski
Editor-in-Chief

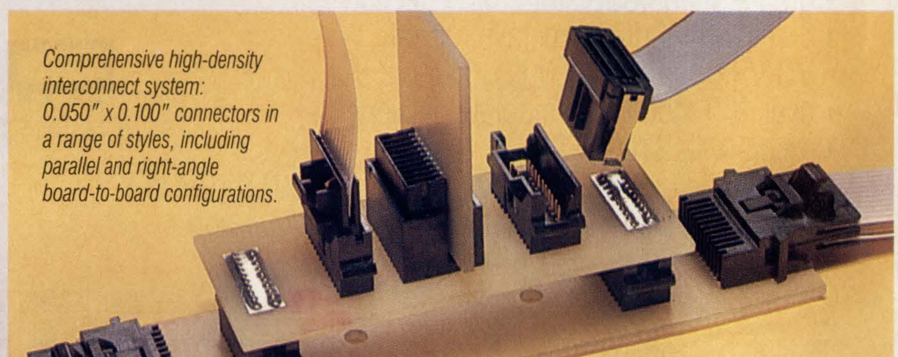
An idea this small

This is the AMPMODU System 50 connector.

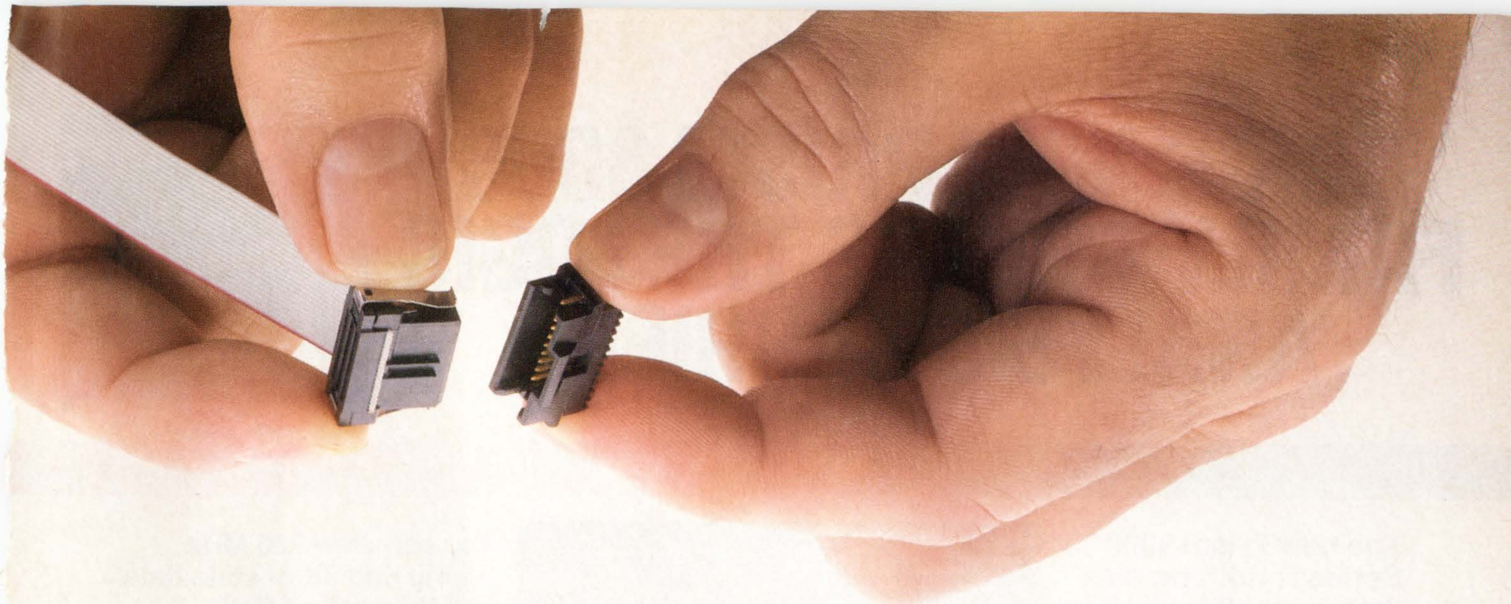
Definitely worth getting close enough for a good look.

It comes in a comprehensive system. Everything you need for a 0.050″ x 0.100″ grid. Board-to-board, stacking, or mother/daughter. FFC to board. 0.050″ CL flex etched circuitry to board. 0.025″ CL ribbon cable to board.

Special design innovations (such as putting the latch hardware on the *cable* side) shrink our System 50 line to the least board space of any connector in this class. Even 0.050″ x 0.050″ types.

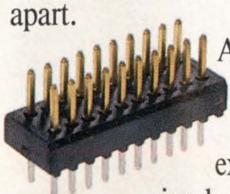


Comprehensive high-density interconnect system: 0.050″ x 0.100″ connectors in a range of styles, including parallel and right-angle board-to-board configurations.



is no small idea.

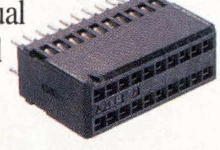
Example: 2x25 position shrouded headers occupy 1.5″ x 0.284″ of board surface. And parallel boards mount with inside faces a mere 0.450″ apart.



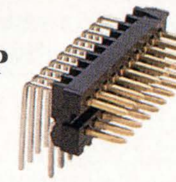
Along with density, you also get the productivity you expect from AMP: simple mass termination, robotic handling features, high-temp housings, selective gold plating.

And of course, outstanding quality and reliability.

AMPMODU System 50 connectors are available in selected sizes of 4 through 30 single row positions, 8 through 100 in dual row, with shrouded or unshrouded headers. With all those variations, you could do almost anything your design requires.



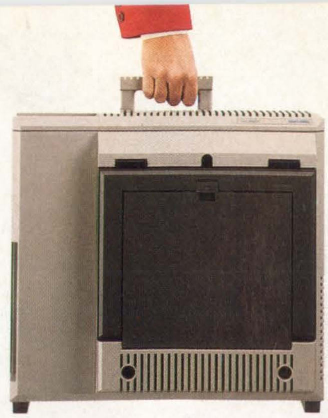
Which is our whole idea.



Call the AMP Information Center at 1-800-522-6752 to ask about our AMPMODU System 50 line. For characterized backplane assemblies, contact AMP Packaging Systems Inc., P.O. Box 9400, Austin, Texas 78766, (512) 244-5100, or your AMP Sales Engineer. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP **Interconnecting ideas**

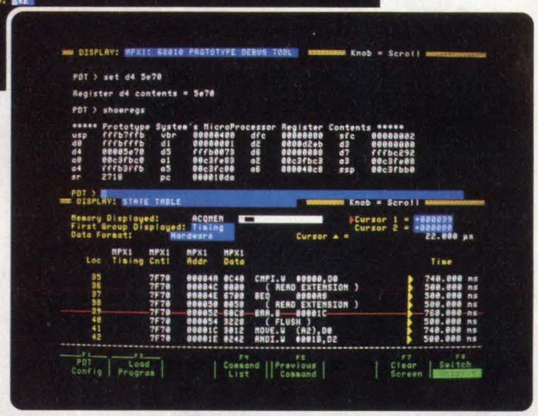
CIRCLE 32



TEK'S NEW PRISM 3000 FAMILY BREAKS THE LOGIC ANALYSIS BARRIER.

The new Prism 3000 Series is nothing less than a breakthrough in the evolution of logic analysis: once you see what it can do, you may scarcely imagine doing without it.

Now digital designers and integrators can start with all the speed, channels and memory depth they need — without tradeoffs. They can mix-and-match tools for their specific needs, including 8, 16 and 32-bit microprocessor debug modules brimming with features never before possible in a logic analyzer. They can add other modules, such as for high-speed timing and waveform analysis, later.



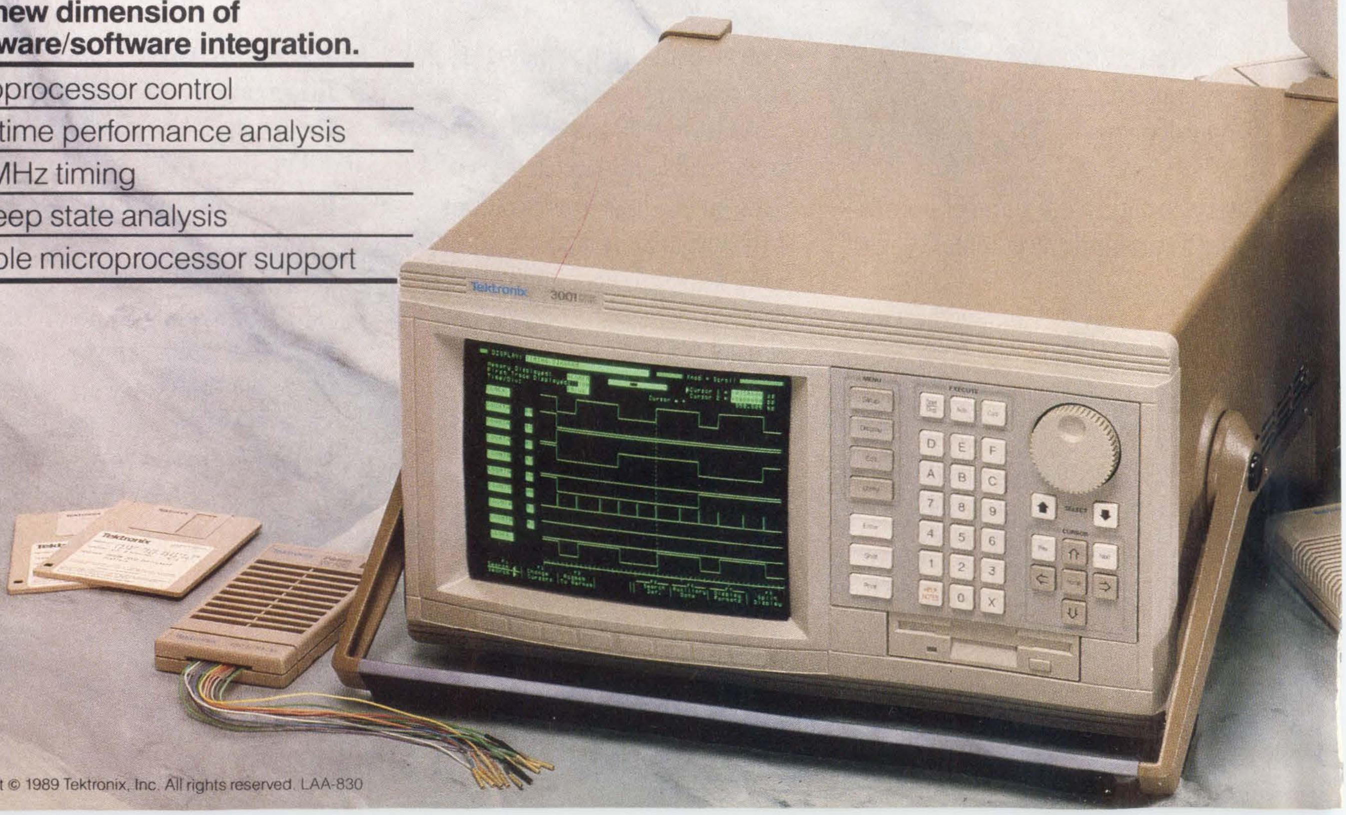
(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.

You can view 200 MHz timing and 8K of state data per channel, all time-correlated and integrated on the same display.

Observe data from multiple microprocessors or time-bases simultaneously. Set up

The new dimension of hardware/software integration.

- Microprocessor control
- Real-time performance analysis
- 200 MHz timing
- 8K deep state analysis
- Multiple microprocessor support



The Prism 3002P configuration features a slide-away keyboard and a 640x400 flat panel display that folds against the mainframe when not in use.

state and timing sections to cross-trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

Push beyond microprocessor observation into emulator-like microprocessor *control*.

With its unprecedented Prototype Debug Tool, Prism is the first logic analyzer to let you set breakpoints, patch registers and memory, restart the system, and more—without an emulator's intrusiveness (or the long wait for new emulator availability).

Use real-time performance analysis to get a true, non-statistical view of system performance.

Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

Choose from a stand-alone version, expandable mainframe-and-monitor, even a portable model with fold-up flat panel screen.

Features like auto-load, split-screen displays, smooth scrolling, automatic timestamping and on-line help notes make Prism refreshingly simple to learn and use.

Complete front panel controls are included on the Prism keyboard, enabling users to move easily from one Prism mainframe to another.

The clincher? You can step into this new generation of logic analyzers at prices starting at $8600.

Call 1-800-426-2200 for our free video demo and literature packet. Prism breaks so much new ground and offers so much to build on, you owe yourself a look. For a hands-on introduction, call your Tek sales engineer soon.

Tektronix
COMMITTED TO EXCELLENCE

CIRCLE 33

TESTING: TALKING A BETTER GAME

JOHN NOVELLINO
TEST & MEASUREMENT EDITOR

An encouraging trend is developing in the test-and-measurement industry—people are starting to talk to each other. Discussions are being held among instrument manufacturers as well as between manufacturers and users. And these aren't just the off-hand comments made at trade shows or during sales pitches—they're formal, useful talks that are positively affecting the way test-and-measurement people do their jobs.

First came the VXIbus standard for instruments on a card. The U.S. Air Force had asked the Modular Automated Test Equipment users group to write an open standard for its own use, but five manufacturers instead decided to develop a standard for both military and commercial users. The standard was completed in 1987, and several development systems and instrument modules were available within the next few months. At ATE & Instrumentation East in June, at least a dozen booths displayed VXIbus products.

Next came an update to the venerable IEEE-488 standard for the general-purpose interface bus, published in June, 1988. Document IEEE-488.2 simplified instrument programming and control by creating a layer of communications protocols and formats. Interestingly, an earlier attempt at standardizing codes and formats, IEEE-728, didn't go over well when it was published in 1981. This time around, though, the ink was hardly dry on 488.2 before people were talking about the possibility of standardized higher-level, device-based commands—an IEEE-488.3.

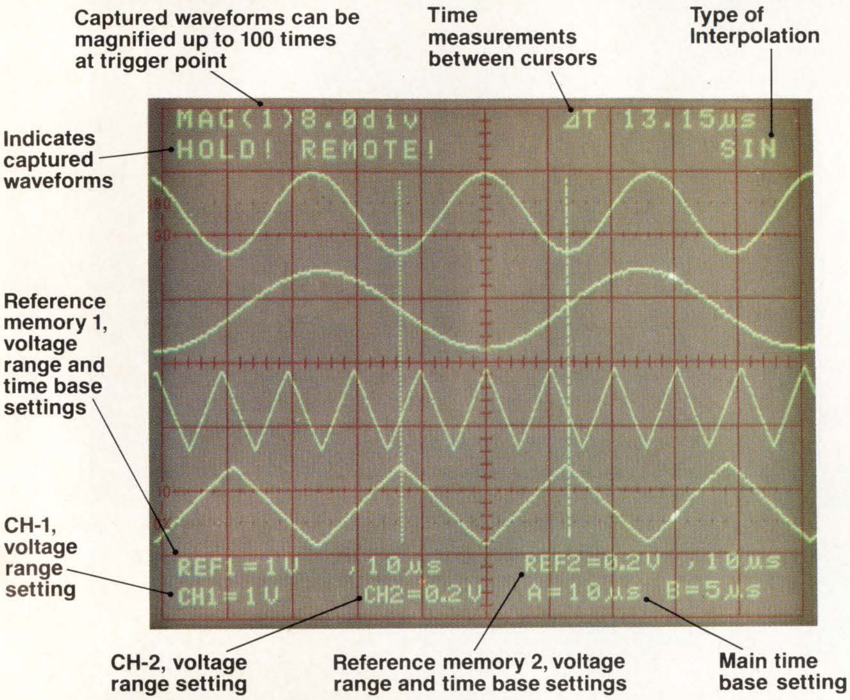
An eager volunteer in the battle for standardization is Hewlett-Packard. Last month, the Palo Alto-based company opened its test-and-measurement systems language (TMSL) to the public. The language uses one command to perform a specific function, regardless of the type of instrument or model. Hewlett-Packard, whose HP Instrument Bus served as the basis for IEEE-488 in 1975, believes that TMSL would make an excellent 488.3. In fact, the company is actively seeking an organization willing to manage the adoption of the language as a standard.

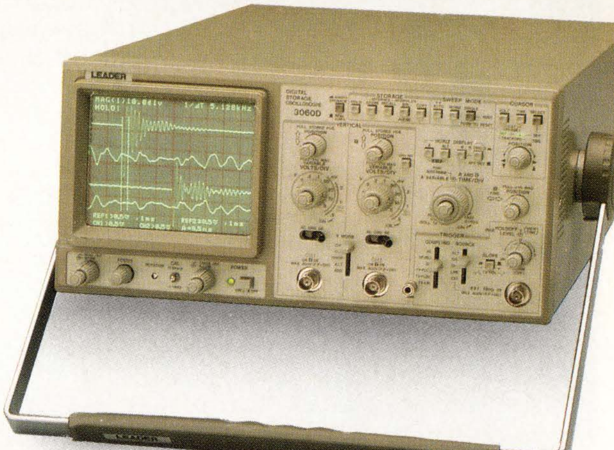
Talks between test-equipment manufacturers and users are also starting to bear fruit. At the International Test Conference in Washington last month, Integrated Measurement Systems Inc. introduced a scan test module for its Logic Master XL series of ASIC test-and-verification systems. Much of the product definition work on the new module resulted from the efforts of the Scan Technical Advisory Group (ScanTAG), which IMS formed with key users in August, 1988 to address scan-test issues. The company also participated in the Joint Test Action Group (JTAG), sent out detailed questionnaires to important users, and conducted one-on-one meetings with customers.

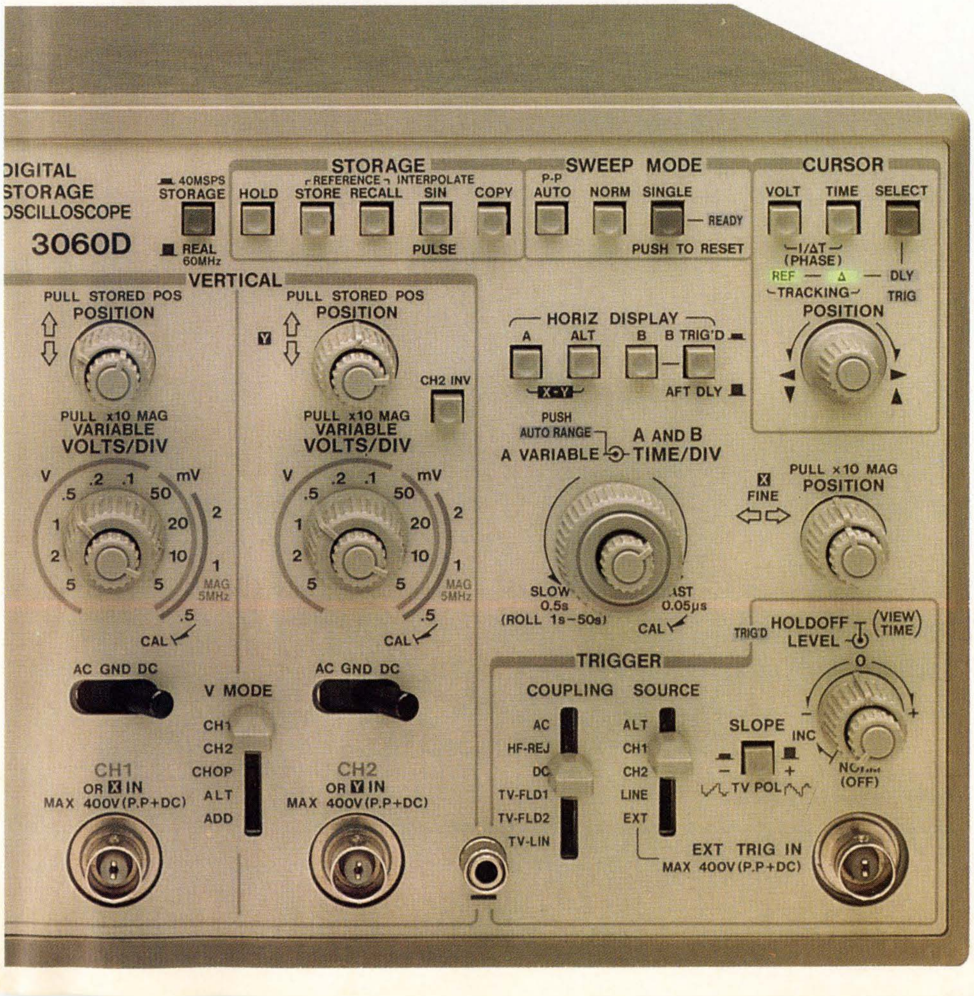
IMS learned that users want a system that supports a number of design-for-testability scan techniques besides that in the JTAG IEEE P1149.1 proposed standard. Consequently, the module also accommodates scan path, scan set, random-access scan, boundary scan, and level-sensitive scan design. Other ScanTAG contributions were the need for optimal serial/parallel memory depth and for ways to convert test data into meaningful and easy-to-use information.

It's easy to see how this trend will help test-equipment users do a better job less expensively. R&D costs too much to spend the effort on proprietary buses and test languages to perform standard functions. Instead, manufacturers should compete on the basis of what functions their equipment can perform and with what accuracy, resolution, speed, and so forth.

LEADER







New full-time digital storage oscilloscope grabs fast events!

Perfect for freezing fast and slow events, the Model 3060D performs as a 40MS/s digital storage oscilloscope and 60-MHz real-time scope.

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Expand captured waveforms up to 100 times and interpolate them; store four waveforms in the 2k word/2-channel memory for immediate or later evaluation, and send fully documented waveforms to a plotter.

Plus, calibrated delay sweep, pre-trigger functions, p-p auto triggering, sine and pulse interpolation, autoranging time base . . . etc. And for computer control, GPIB is standard.

The 3060D is backed by a TWO-YEAR WARRANTY, and factory service depots on both coasts.

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For Product Information Circle 34
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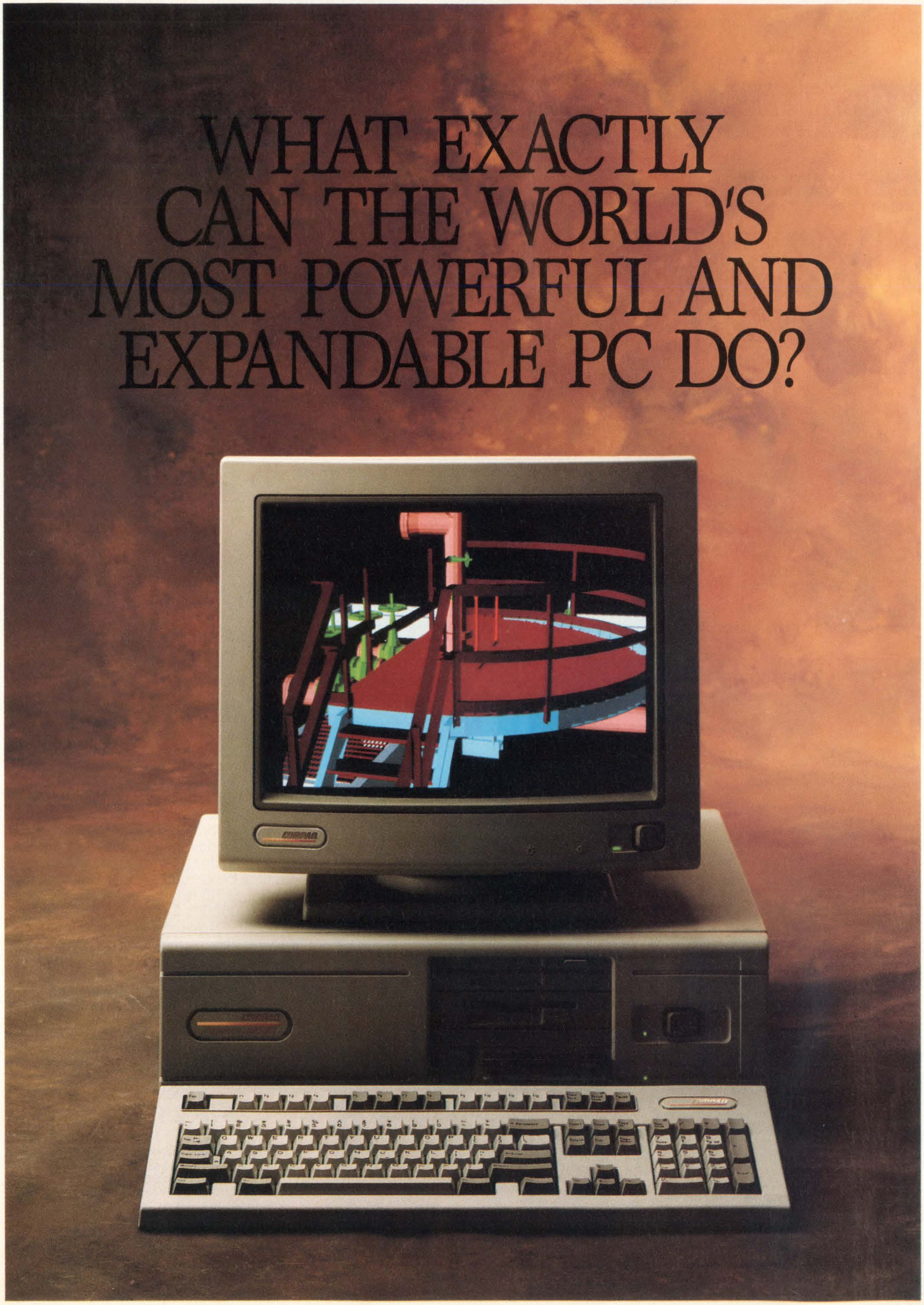
WHAT EXACTLY
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EXPANDABLE PC DO?

INTRODUCING THE COMPAQ DESKPRO 386/33 PERSONAL COMPUTER.

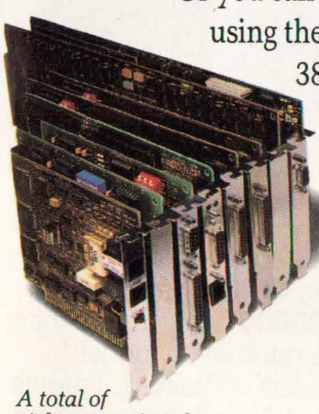
Never before has so much performance, expandability and storage been put into one desktop PC. And never before has one PC been capable of so much.

ANYTHING IT WANTS.

Inside its new system unit, you'll find that our engineers have redesigned just about every component to deliver a minicomputer level of power with unmatched PC flexibility.

So you can use it as a stand-alone PC, putting its power to work on the most demanding CAD/CAE, financial analysis, database management and personal productivity applications.

Or you can spread the power around, using the COMPAQ DESKPRO 386/33 as the driving force for a network or multiuser system.



A total of eight expansion slots let you customize the system to your needs by expanding memory and choosing from thousands of industry-standard expansion boards.

At the heart of the system is the Intel 386™ microprocessor. Running at a blazing 33 MHz, it works in concert with a series of technological advancements. Like a 33-MHz cache memory controller with 64K of high-speed static RAM. Interleaved memory architecture. And the exclusive COMPAQ Flexible Advanced Systems Architecture.

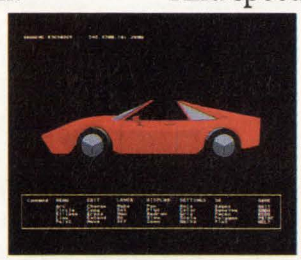
This high-performance combination delivers a 35% performance improvement in CPU-intensive applications over 25-MHz 386 cache-based PC's.

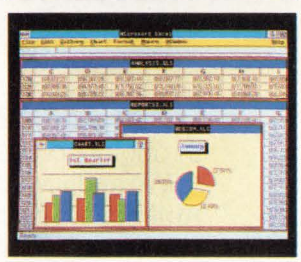
Or said another way, nothing will slow you down. No matter what you want to do. You can expand the 2 MB of standard RAM up to 16 MB using the high-speed 32-bit slot. That leaves up to *six* industry-standard slots free to customize the system to the demands of the application you're using.

If your job is particularly demanding, you can use up to five high-performance internal storage devices to hold up to 1.3 *gigabytes* of data. And if that's not enough, bring total system storage to 2.6 gigabytes with the optional COMPAQ Fixed Disk Expansion Unit.

There's more. You can run MS-DOS®, MS® OS/2, Microsoft® Windows/386 and the XENIX® and UNIX® operating systems. Access memory over 640K under DOS with the COMPAQ Expanded Memory Manager that supports Lotus/Intel®/Microsoft (LIM) 4.0. And speed through calculations with 33-MHz Intel 387™ and Weitek 3167 coprocessor options.

Built-in interfaces make it easy to connect pointing devices, printers, plotters or other peripherals without using an expansion slot.





High-speed VGA graphics are built in. And for greater graphics capabilities, add the optional COMPAQ Advanced Graphics 1024 Board.

All the new advancements engineered into the COMPAQ DESKPRO 386/33 deliver an unmatched level of power, expandability and storage. To do anything you want.

To find out more, please call 1-800-231-0900, Operator 97. In Canada, 1-800-263-5868, Operator 97. We'll send you a free brochure and give you the location of your nearest Authorized COMPAQ Computer Dealer.

COMPAQ

It simply works better®

GENERAL DYNAMICS LAND SYSTEMS

Generations from now, when today's state-of-the-art fighting systems have taken their place in armament history books, today's Abbott power supplies will still be operating reliably.

Outfitted for Enhanced Reliability, for example, our new 60 Watt triple-output switching DC-DC converter achieves an MTBF rating up to 600,000 hours; more than 68 years. A single-output model is rated even longer.*

Yet this compact package is fully self contained. It meets the tough EMI limits of MIL-STD-461C. And the punishing environmental specs of MIL-STD-810C and MIL-S-901C.

While the BC60 is brand new, this is no "developmental" power supply. Its topology is identical to our field proven BC100 and BC200 models. Its design integrity is verified through rigorous ESS testing.

We're delivering power supplies for projects critical to America's defense, including MILSTAR, the EH101 helicopter, the TOW missile, INEWS and the F/A-18 Hornet.

For a copy of our 1988 Military Power Supply Product Guide, write us at 2721 S. La Cienega Boulevard, Los Angeles, CA 90034. (800) 556-1234 XT9; CA (800) 441-2345 XT9.

*MTBF FIGURES CALCULATED PER MIL-HDBK-217E GROUND.

Our power supply is built to outlast the tank.

Versatile new 60 Watt switcher measures 5 x 4 x 1.5 inches. Provides outputs of 5, 12, 15, 24 or 28 V dc, from inputs of 18 to 36 V dc. Operating temperature from − 55°C to + 100°C. Overvoltage protection & short circuit protection standard.

abbott

WHEN RELIABILITY IS IMPERATIVE.™

CIRCLE 60

INSTRUMENT CRT CAPTURES PICOSECOND PULSES

An oscilloscope tube from the Components Division of Philips N.V., claims to capture nonrepetitive, narrow pulses faster than any other oscilloscope tube in the world. Developed at the company's Paris research labs, the D3-120KA/N boasts a bandwidth of 7 GHz, compared with 3 GHz for existing ultra-fast CRTs. The result is a giant leap forward in single-shot electronic imaging. The high bandwidth makes the tube suitable for applications in high-speed digital communications, particle physics, and high-power laser research. The 7-GHz bandwidth corresponds to a 50-ps pulse rise time. The bandwidth comes from the tube's vertical-deflection system, which consists of a tiny helix line. The horizontal-deflection system, which is built around a symmetrical meander line, has a 3-GHz bandwidth. As a result, fast deflection signals of linear, sinusoidal, or mixed types can be used. For timing, the D3-120KA/N uses 100-ps marking pulses, which can be superimposed on the signal by an independent deflection system. JG

2-A TRIAC-OPTOCOUPLER HANDLES RECORD POWER

Representing a virtual powerhouse in the triac-optocoupler field, the IL428 from Siemens AG handles 2 A—almost ten times the current-handling capability of conventional couplers. According to the company, this ability makes the chip the most powerful triac-optocoupler to date. Developed at Siemens Components Inc.'s Optoelectronics Division, Cupertino, Calif., the coupler comes in a new single-in-line package that needs no cooling, even for 2-A operation at up to 55°C. It consists of a GaAs infrared light-emitting diode optically coupled to a photo-triac. The photo-triac is so sensitive that control currents of less than 8 mA will switch the 2-A maximum current, and for resistive, inductive, and capacitive loads of 120 V, 230 V, and 380 V. Besides having applications in semiconductor relays, industrial controls, office equipment, and consumer electronics, the coupler opens up new applications for current switching in line-powered systems. JG

ASIC TEST APPROACH CLEARS HURDLES

Roadblocks on the path from simulation to test can often hinder successful ASIC designs. These obstacles include logic simulation; incorporation of tester-specific limitations, which means knowing what stimulus will be produced; and simulation verification and translation. The DesignTest approach offered by NCR, Ft. Collins, Colo., contains several key elements that team up to clear these hurdles. A central database contains complete and consistent data for both the design and test environments. A high-level simulation language adds portability across popular simulators, and built-in tester knowledge increases tester compatibility. Because an expected device response is included, the verification can also be performed at several stages within the design cycle. A paper on the DesignTest approach is one of many concerning all aspects of ASICs to be presented at the Second Annual IEEE ASIC Seminar and Exhibit in Rochester, N.Y., September 25 to 28. RN

MODULAR ARCHITECTURE CRAFTS CUSTOM BOARDS

Creating custom versions of standard board families can run up high nonrecurring engineering charges. A better way to create application-specific boards is to have a "base" board with a minimal set of functions, a local bus, and optional peripheral modules. The Corebus architecture from Heurikon, Madison, Wis., consists of a CPU bus extension and optional plug-over modules. The local bus isn't easy to design: It must be fast enough to support a high-bandwidth link between the base board and the modules, yet flexible enough to satisfy the requirements of a broad range of memory and peripheral devices. Heurikon's Corebus is a standard 50-MHz, synchronous extension of a CPU card's internal bus that burst-transfer up to 200 Mbytes/s. In addition, it supplies flexible, multimaster arbitration and is compatible with both RISC and CISC processors. For board customization, application-specific options like specialized memory, DMA, Ethernet, and graphics are added through Corebus modules. LG

8051 MICROCONTROLLER RUNS FROM 1.5-V SOURCE

Thanks to a low-power, self-aligned CMOS process technology, power-saving operating modes, and specific design measures, engineers at Philips International N.V., Eindhoven, the Netherlands, have readied an 8051-based microcontroller that works from supplies as low as 1.5 V. Philips claims that this operating voltage is the lowest for any microcontroller to date. The PCF84C410 opens up many new markets for one-cell-battery applications, including pocket telephones and portable telecom equipment (cordless and cellular phones, facsimile systems, and answering machines). The device also fits general-purpose jobs in instrumentation, industrial control, intelligent computer peripherals, portable consumer products, and smart cards. The 16-MHz controller typically draws 1 mA from a 3-V supply at a 3.58-MHz clock frequency. Its idle- and power-down modes cut current drain to 0.5 mA and 1 μA, respectively. The chip's own oscillator circuits work down to 32 kHz. With external oscillators, the controller operates down to dc, which means the clock can be turned off. When it's turned back on, the 84C410 resumes the operation it was performing. The result is even lower current drain because the controller lies dormant until the clock stream resumes. JG

NETWORK AND CPU GET SEPARATE MEMORY

The Full Throughput (FXP) architecture that CMC, Santa Barbara, Calif., uses in its network-interface processors allocates separate memory locations for host and interface processors. This improves network speed by eliminating competition for resources. With memory dedicated for programs, the CPU's instructions are executed from a private memory instead of a common one. Only the host can access the program memory directly, so it doesn't compete with network or VMEbus controllers for processing time. In addition, while most other products use plain DRAM, the FXP architecture uses video DRAM as global data memory. Video RAM gives users two ways to access data memory: the DRAM port and the sequential-access-memory (SAM) port, which has 32-bit parallel access at 800 Mbits/s. Examples of computer systems that can benefit from the FXP architecture include 3D workstations, such as those available from Silicon Graphics. The architecture will be the basis for many future CMC products, including the company's fiber-distributed data interface (FDDI) line. LG

MULTIPLE WRITE LINES SIMPLIFY BYTE PARITY

To check byte-wide parity, computer designers usually add bit-wide memories to long words formed with 4- or 8-bit-wide RAMs. But because each byte-parity bit needs its own write-control line, 32-bit word lengths need four separate bit-wide chips. Now, however, a 64k-by-4-bit static RAM from Motorola Semiconductor Inc., Austin, Texas, offers four write-control lines, eliminating the need for four separate chips. The four asynchronous lines make it possible to write to each bit position individually: Each bit's write cycle is completed only if its own strobe line is asserted within the specified setup time after a rising clock edge. Conversely, write cycles can be aborted by negating the write line before the clock goes low. Surrounding the forthcoming chip's 64k-by-4-bit core are positive-edge-triggered registers on address and synchronous-write enable lines. The synchronous design keeps data access down to 20 ns and cycle time to 25 ns. Such short access times let the novel RAM keep pace with a high-speed memory system. DB

CIRCUITS MEETING PEEKS AT TOMORROW'S ICS

The 4th annual IEEE Bipolar Circuits and Technology Meeting in Minneapolis, Minn. this month will give a glimpse of what the next few years should see in fast, wideband analog and digital ICs. Topics to be discussed include 30-GHz f_T transistors in silicon ECL, rather than GaAs; a liquid-cooled ECL gate array; 200-GHz f_T GaAs heterojunction bipolar transistors (HBTs); 10-bit 40- to 60-MHz a-d converters; a wideband JFET-input op amp with lower noise than most bipolar-junction-transistor (BJT) input op amps; trade-offs needed to run silicon BJTs at 70K; and a handful of complementary and biCMOS processes yielding 13-GHz npn transistors and 5-GHz pnps. The meeting will be held at the Marriott Hotel in Minneapolis on Sept. 18 and 19. For last minute registration call the conference office at (612) 934-5082. FG

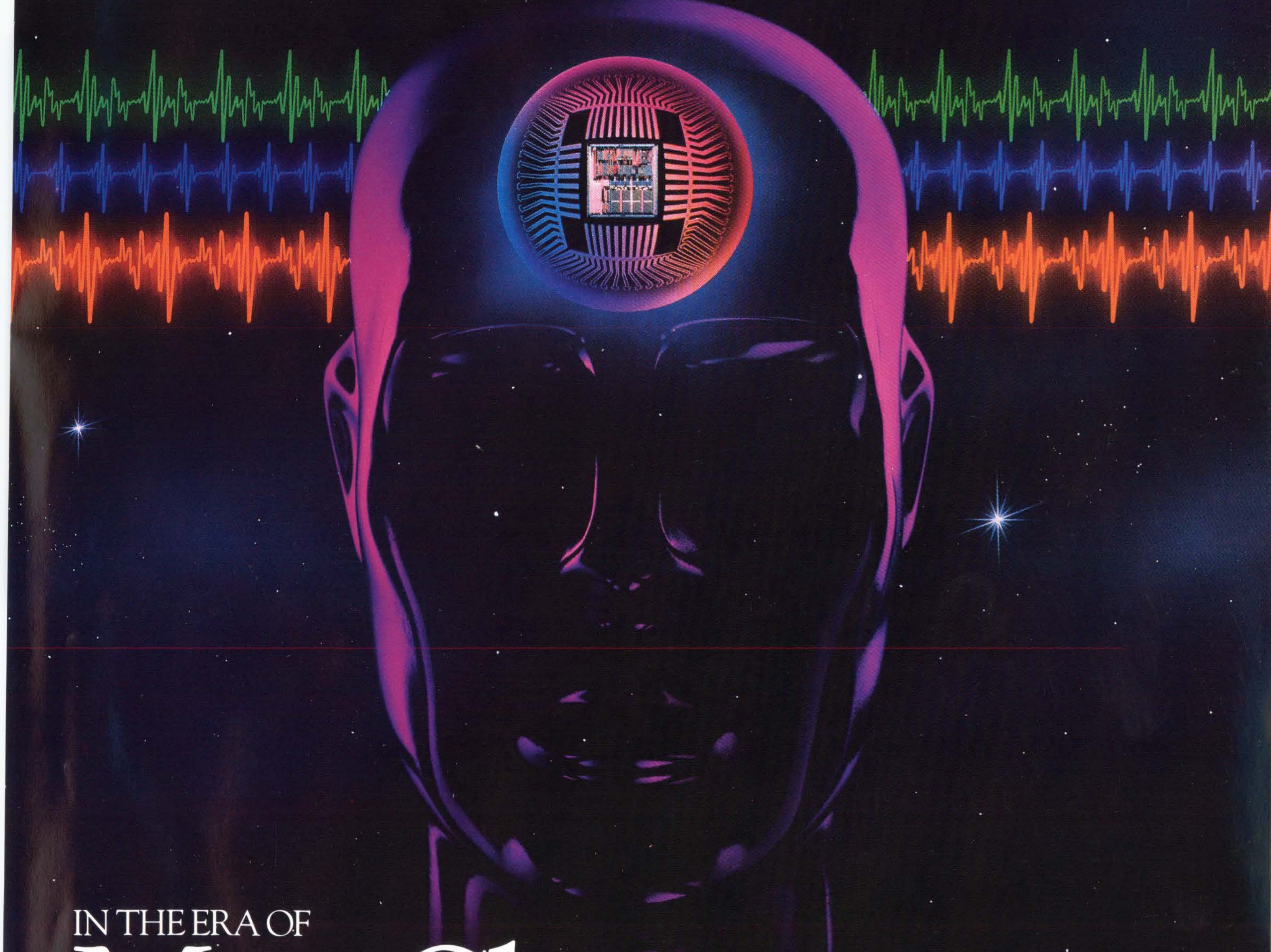
BETA TESTING BEGINS FOR GRAPHICS BENCHMARK

Software for a picture-level benchmark (PLB) that will compare the performance of workstation graphics is now in beta test and will be released in early 1990. The benchmark is the fruit of efforts by the Graphics Performance Characterization (GPC) group and 11 companies working under the supervision of the National Computer Graphics Association (NCGA) (ELECTRONIC DESIGN, *Feb. 9, p. 22)*. The NCGA plans to release the PLB source code to the public in March, 1990, so that any hardware vendor can port the code to its platform. Users will port geometry from their graphics applications to PLB software through a Benchmark Interface Format (BIF), which is based on a superset of elements from the Programmer's Hierarchical Interactive Graphics Standard (PHIGS+). The application can then be run for performance comparison on any hardware that supports the PLB program. BIF specifications are available from the NCGA for a nominal fee. Future plans for the GPC group include software that will grade graphics, windowing, I/O operations, and operating-systems. LG

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

New ways to link digital brains to advanced analog worlds

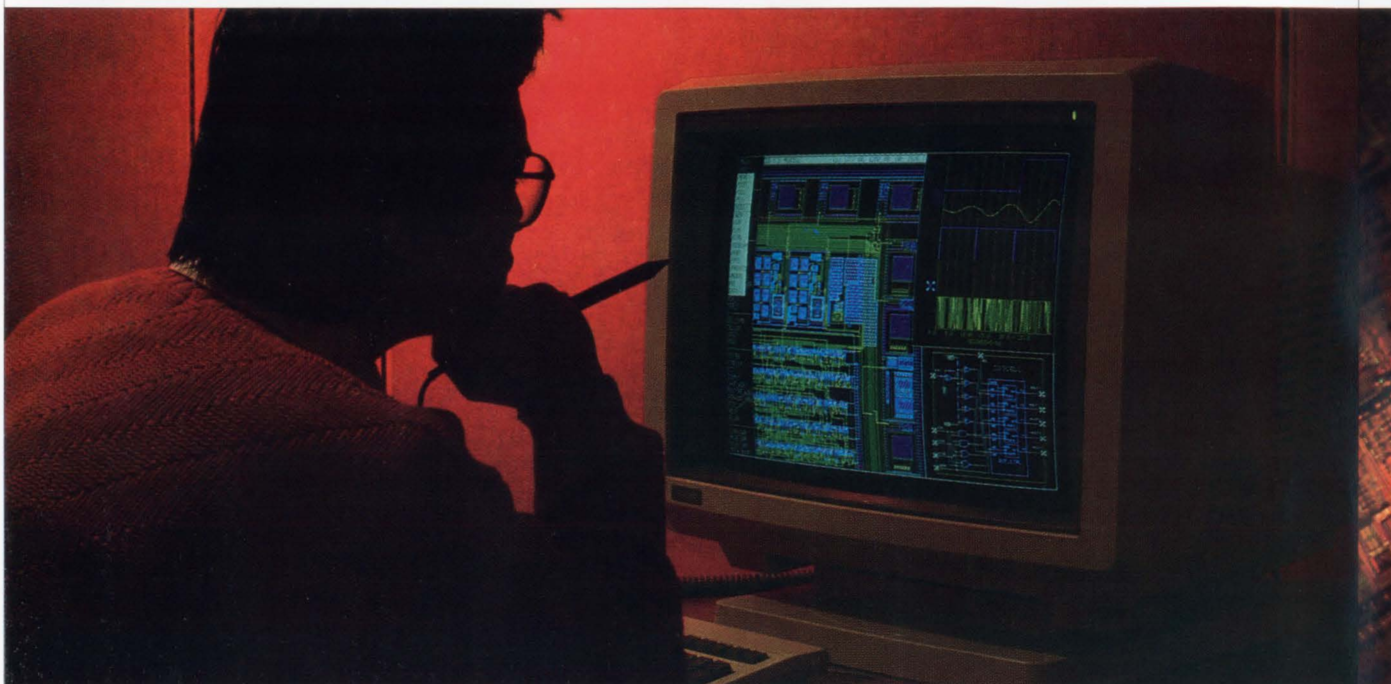


IN THE ERA OF

MegaChip□ TECHNOLOGIES

Next-generation analog: Advanced Linear ICs

A new breed of linear chips, born of leadership processing at Texas Instruments, can help you design superperformance systems.



Sophisticated design and simulation tools shorten development cycles of TI's Advanced Linear ICs, helping you get to market faster. By using these tools, TI can offer as standard circuits many designs that previously would have had to have been customized.

The human brain has separate but dependent left and right sides. Similarly, an electronic "brain" or system has separate but dependent parts, one digital, one analog. Designers accustomed to the spectacular performance gains made in digital chips are now demanding comparable improvements in analog devices so that both parts of their systems can function to full potential. Leading the analog evolution: Advanced Linear circuits from Texas Instruments.

These new chips are called *advanced* for one or more reasons. They are more highly integrated than ever before, often combining digital and analog functions on a single chip. They offer higher performance and greater flexibility. They are often the result of advanced processing that may merge two or more technologies.

Better parameters from better processing

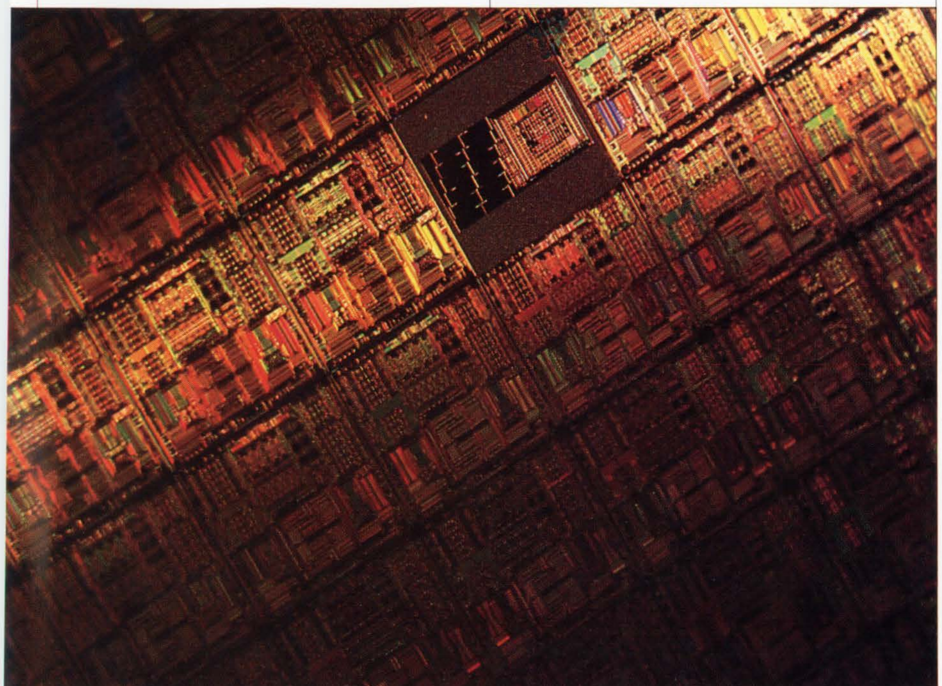
Because advanced analog system requirements for performance and flexibility vary greatly, a single workhorse technology typically can't do the job any longer. Nor can creative circuit designs alone. We at TI are convinced the key to driving the linear evolution lies in the excellence of our processing technologies.

TI is committed to developing and implementing a range of leadership wafer-fabrication processes (*see descriptions on back page*). The result: TI's Advanced Linear devices are already helping system designers link digital brains to advanced analog worlds more efficiently and with greater ease in many applications. Here are a few examples.

Advanced Linear: Displaying greater brilliance

Out of our pacesetting LinEPIC™ processing comes our high-performance Color Video Palette, operating at 125 MHz with a very high-resolution 1024 x 1024 pixel count. Because of one-micron CMOS processing, power consumption is reduced more than 40% compared to other CMOS implementations. Additionally, the device is pack-

...the key to driving the linear evolution lies in the excellence of processing technologies.



High-density Analog Interface Circuit chips demonstrate the greater integration achieved by TI's innovative linear processing technologies. These DSP interfaces allow you to alter circuit configuration under software control without external adjustments.

aged in reliable, economical plastic.

LinEPIC has also produced such high-speed, high-density interface chips as our Flash A/D and our Video DAC for use in graphics displays, imaging systems, monitors, and cameras. Both devices require about five times less power than bipolar equivalents.

Advanced Linear: Intelligent power for every car

Chips fabricated with our Power DMOS-based BIDFET™ processing are replacing electromechanical relays in many automotive applications, such as driving headlamps and motors. Power BIDFET allows us to minimize power loss in the switch and add high-complexity logic functions.

Multi-EPI bipolar processing, a very cost-effective technology, is used to produce chips having inherent reverse battery protection and high operating voltages. Such chips are ideal for use in automotive antilock braking systems, electronic transmissions, and active suspension systems.

Either technology can produce devices with low-side drive, high-side drive, or H-bridge configurations.

In the future, these developments may lead to multiplexed systems for cars, replacing bulky wiring harnesses.

Advanced Linear: Enhancing modems and facsimiles

TI's dual driver/receiver is a good example of the integration achieved with advanced processing technologies. LinBiCMOS™ processing has enabled us to put the drivers and receivers needed for RS-232 voltage levels on the same chip with the charge pump required to generate the necessary split rails from a single 5-V supply. You eliminate external power supplies and get a device that's easier to design with—it is available in our LinASIC™ cell library for integration with digital ASICs.

A new family of Analog Interface Circuits (AICs) is emerging from our Advanced LinCMOS™ processing. The voice-band AICs, designed for modems and fax equipment, combine high-performance analog functions—14-bit A/D and D/A converters and switched capacitor filters—with digital functions such as control circuitry, program registers, and DSP interface. The usual clutter of resistors, capacitors, and pots is eliminated.

High-speed AICs are available for use in servo controllers and hard-disk-drive applications.

These AICs are also high-performance members of our LinASIC standard-cell library. Based on TI's proven digital ASIC methodologies, the LinASIC library has allowed us to develop complex, semicustom chips in as little as 16 weeks.

Advanced Linear: Boosting instrumentation accuracy

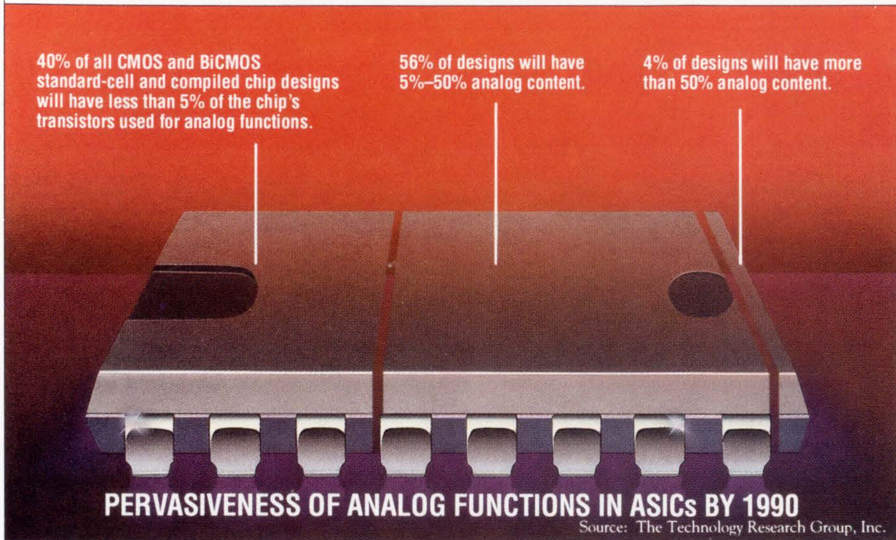
Even one of the most basic analog building blocks, the operational amplifier, is benefiting from TI's Advanced Linear technologies. Our Excalibur op amp family combines low power consumption with a 5X speed improvement while retaining low offset voltages. Offset-voltage drift has been cut from 300 μV to 60 μV to reduce your calibration, test, and measurement expenses.

For high-accuracy applications, Advanced LinCMOS is making possible Chopper Stabilized Op Amps with chopping frequencies 10 times higher than previously available (10 kHz). Noise levels are the lowest on the market.

The evolution in analog devices has only begun. Dramatic progress lies ahead throughout the 1990s. As the Advanced Linear leader, Texas Instruments is pledged to remain at the forefront, supplying you with new ways to link digital brains to advanced analog worlds.

For suggestions on choosing a linear supplier, turn the page.

A PERSPECTIVE ON ANALOG SYSTEM DESIGN



Circuits combining analog functions with digital logic will soon be widespread in ASIC chip designs. TI is taking a leadership role with the development of its LinASIC methodology.

Checkpoints for choosing an analog supplier in the 1990s.

Questions and answers with Tom Engibous, Vice President, Semiconductor Group, and Manager, Linear Products, Texas Instruments Incorporated.

Q. What is the first thing to look for in choosing a linear supplier?

A. Product performance is definitely the first priority. Our customers are asking for ever-increasing linear device performance. At TI, we believe creative circuit designs alone won't meet the challenge. Advanced process technologies—note the plural—are becoming the keys to success in linear device performance of the '90s.

Q. What else should a designer look for?

A. Whether or not the supplier has experience with digital as well as analog devices. These two worlds are merging (*see chart above*). Functions once performed by analog are now done digitally, and a growing percentage of our Advanced Linear devices combines analog and digital circuitry on one chip.

At TI, we've leveraged our 30 years of digital expertise into the development of our Advanced Linear products and processing with highly satisfactory success. This has been especially noticeable with our LinASIC methodology.

Q. Do you expect ASICs to play a major role in your linear future?

A. Very definitely, as they already do today. Cell-based designs will be the rule in both user-specified functions and highly integrated standard products. Digital ASIC methodologies are also the key to cutting system design cycles. As our digital experience proves, suppliers who have advanced process technologies and fast, accurate design-automation tools will be the best equipped to deliver single-chip solutions.

Today, we have customers doing their own LinASIC designs using our advanced processes and design-automation tools.

Q. What role does manufacturing capability play in picking a supplier?

A. It is always a factor, and the need for efficient worldwide manufacturing facilities such as TI has in place will become even more important. Today's semiconductor market is global in nature. You can't serve worldwide customers from a single plant—you have to be "multilocal." This is particularly true with ASICs.

Q. Any other important factors?

A. Yes, I'd suggest that, in choosing a linear supplier, the designer find one he can live with for a long time. Close supplier-customer relationships are essential to the development of products that will provide the highest performance and lowest cost systems.

TI's Leadership Linear Processing Technologies

LinBiCMOS—Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC—One-micron CMOS double-level metal, double-level polysilicon technology which adds highly integrated, high-speed analog to the high-performance digital EPIC process.

Advanced LinCMOS—An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET—Merges standard linear bipolar, CMOS, and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar—A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 40%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur—A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing the most stable op amp performance available today.

Our just-published *Advanced Linear Circuits* brochure examines more fully the changes taking place in analog system design and their impact on linear devices. The brochure also describes TI's leadership processing technologies and explains the performance improvements that result. **For your copy, call 1-800-232-3200, ext. 3407, today.**

TEXAS INSTRUMENTS

NEWS

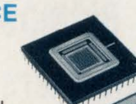
ILC DATA DEVICE CORPORATION

SEPTEMBER 1989

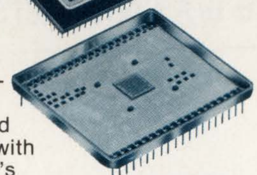
ABOUT SYNCHRO-CONVERSION • A/D & D/A CONVERSION • 1553 BUS DEVICES • POWER & CUSTOM HYBRIDS

All You'll Ever Need In 1553!

MONOLITHIC BC/RTU/MT PROVIDES COMPLETE 1553 BUS TO SUBSYSTEM INTERFACE



BUS-65612

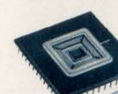


BUS-65610

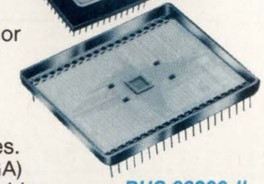
The BUS-65610 (and BUS-65612 PGA) is a complete dual-redundant Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor Terminal (MT). This small 1.9" x 2.1" hybrid contains 2 encoder/decoders; 2 bit processors; BC, RTU, and MT protocol; and complete interface logic. When used with a low power transceiver, such as DDC's BUS-63125, and (optionally) the BUS-66300 II Interface Unit, the BUS-65610 provides a complete intelligent MIL-STD-1553B interface. The BUS-65610 hybrid and BUS-65612 PGA version are available screened to MIL-STD-883.

FOR SALES CONTACT CIRCLE 40 FOR LITERATURE CIRCLE 41

MONOLITHIC 1553 TO CPU INTERFACE HYBRID OR PGA REDUCES CPU OVERHEAD



BUS-66312



BUS-66300 II

DDC's BUS-66300 II Interface Unit simplifies interfacing the MIL-STD-1553 terminal to a MIL-STD-1750 or other standard microprocessor. This small 2.1" x 1.9" 78-pin hybrid frees the host CPU by assuming terminal control, data transfer timing/control, and response handling responsibilities. The BUS-66300 II (and BUS-66312 PGA) manages up to 64K x 16 of RAM, provides double buffering and uses standard control and memory I/O. When matched with a DDC intelligent Terminal Unit, the BUS-66300 II completes a truly stand-alone, bit-mapped 1553 interface. (Available screened to MIL-STD-883).

FOR SALES CONTACT CIRCLE 46 FOR LITERATURE CIRCLE 47

1553B RTU/BC/MT MODULE FOR GRiD™ 1530 LAPTOP

BUS-65555

The BUS-65555 plug-in expansion module offers full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the GRiDcase 1520, 1530, and 1535 laptop XT/AT compatible computers. It's software controls operation as a 1553 Remote Terminal Unit (RT), Bus Controller (BC), or Bus Monitor (MT) and is fully compliant with MIL-STD-1553B. Small size, high performance, low power requirement, and low cost make the BUS-65555 and GRiDcase combination an excellent choice for dynamic simulation in the lab or for flight line applications.

TM GRiD and GRiDCASE are a registered trademark of GRiD SYSTEMS CORPORATION.

FOR SALES CONTACT CIRCLE 42 FOR LITERATURE CIRCLE 43

IBM PC® CARD PROVIDES 1553 TEST/SIMULATION

BUS-65517

The BUS-65517 integrated, single-slot IBM-PC card and software provide a complete MIL-STD-1553 development package. Utilizing 2 on-board processors, the BUS-65517 requires little PC processing power to simulate up to 31 Remote Terminal Units, an assignable Bus Controller, an intelligent Monitor (event-triggerable command reconstruction), error injection/detection, and a MIL-STD-1553 port. User-friendly, intuitive menus and graphics (color or monochrome) provide integrated development, emulation, and analysis (IDEA) capabilities without lengthy training. The BUS-65517's Real Time Display provides complete real-time information.

® IBM PC is a registered trademark of International Business Machines Corporation.

FOR SALES CONTACT CIRCLE 48 FOR LITERATURE CIRCLE 49

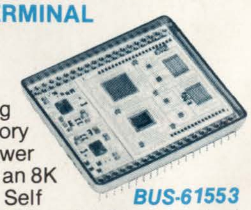
LOW COST 1553B REMOTE TERMINAL HYBRID

BUS-65142

The new, low cost BUS-65142 MIL-STD-1553B Dual Redundant Remote Terminal Hybrid features a single chip CMOS/SOS monolithic RTU protocol and Bipolar low power Mark II transceivers. It supports 13 mode codes for dual redundant operation and performs continuous on-line wraparound self-test. The BUS-65142 has radiation tolerance to Tactical Levels as well as excellent Single Event Upset tolerance. Incorporating small size (1.9" x 2.1") with low power, high reliability, and low cost makes this ideal for most MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

FOR SALES CONTACT CIRCLE 44 FOR LITERATURE CIRCLE 45

1553 INTEGRATED BC/RT/MT TERMINAL



BUS-61553

The BUS-61553 is an Advanced Integrated MUX (AIM) Hybrid which minimizes CPU overhead by assuming host interface maintenance and memory management. It contains dual low power transceivers, complete protocol logic, an 8K x 16 shared RAM, on-line and off-line Self Test, is compatible with MIL-STD-1750 and other standard CPUs, and is SEAFAC Tested. It comes as a 2.1 x 1.9 x 0.25" (DDIP) or a 2.2 x 1.6 x 0.17" (Flatpack). Also available as a single +5V only supply. MIL DWG TO BE ANNOUNCED.

FOR SALES CONTACT CIRCLE 50 FOR LITERATURE CIRCLE 51

FOR ADDITIONAL PRODUCT INFORMATION CONTACT DATA BUS APPLICATIONS 1-800-DDC-1772.

ILC DATA DEVICE CORPORATION

HEADQUARTERS AND MAIN PLANT: ILC Data Device Corporation, 105 Wilbur Place, Bohemia, N.Y. 11716, (516) 567-5600, TLX-310-685-2203, FAX: (516) 567-7358
WEST COAST (CA.): WOODLAND HILLS, (818) 992-1772, FAX: (818) 887-1372; SAN JOSE, (408) 236-3260, FAX: (408) 244-9767; GARDEN GROVE, (714) 895-9777
WASHINGTON, D.C. AREA: (703) 893-7989, FAX: (703) 893-7954
NORTHERN NEW JERSEY: (201) 785-1734, TLX: 130-332
MASSACHUSETTS: (617) 341-4422 or 3128, FAX: (617) 344-1040
JAPAN: (03) 814-7688, FAX: (03) 814-7689
UNITED KINGDOM: 635-40158, TLX: 851-848826; **FRANCE:** (1) 4-333-5888, TLX: 842-630609
WEST GERMANY: (08191) 3105, TLX: 841-527128; **SWEDEN:** 8-920-635, TLX: 854-10952

Transputer Modules Ease Parallel Processing

Engineers can build a parallel computer that delivers about 100 MIPS and 12 MFLOPS on a standard VMEbus card for less than $10,000 and in the time it takes to plug eight small modules into a board. Moreover, the modules can be mixed and matched to achieve various processor, memory, digital-signal processing, peripheral and graphics controller, and I/O-interface combinations. Designers can tailor the optimum embedded or standalone processor based on a range of standard-bus system boards, such as a PC XT/AT, PS/2, GPIB, Futurebus, or VXI.

This system extends beyond a set of parts for breadboarding prototypes. It includes more than 40 fully engineered modules and motherboards intended for full-production runs. Known as the IQ System, the modules from Inmos Ltd., Bristol, U.K., are now being produced and they will be formally introduced on September 12 at Buscon East in Boston.

The intention of the IQ Systems Division is to offer a catalog of modules and motherboards that will help designers build complete systems. Ian Pearson, Inmos' newly appointed director of Systems Products, divides system functions into seven layers, each defined as a class of functionality.

The first layer assumes that a system needs to communicate with other systems. The IQ first-layer modules will then connect with various local-area networks. The first modules to be included in this category are Ethernet controllers. Modules that can drive 20-m, 20-Mbit/s Transputer serial-communications links are currently under development. Next will come modules to connect with high-speed, fiber-optic networks.

Within a system, second-layer modules will encompass what Pearson describes as "general-purpose I/O modules." These will offer interfaces to such standards as RS-232-C and IEEE-488 (GPIB), as well as analog-to-digital conversion and other functions.

Processors—the third layer in Inmos' strategy—are next. They consist of a series of computing modules, including 16- and 32-bit integer and floating-point scalar processors and vector processors. All modules in this category will contain memory.

Peripheral controllers and interfaces, such as graphics modules and controllers to drive the standard SCSI interface, define the fourth layer. This is followed by a more advanced set of application-specific modules, which constitute the fifth layer.

As an example, Pearson cites a module containing an Inmos A121 image-compression chip. This device compresses dynamic video information, reducing the bandwidth needed to send high-definition moving images, and then decompresses them on reception.

According to Pearson, a module that employs this device could be teamed with others to build a high-capacity video store. The subsystem would compress signals for storage on various media, and then decompress them for subsequent processing and display.

Up to this level, individual modules conform to a credit-card-sized layout adopted as the basic standard. Because of the Transputer's architecture, modules need just 16 pins to communicate with the outside world. In fact, the Transputer was designed from the outset to be totally self-contained, incorporating such functions as local-memory management, clock generation, and synchronization.

In addition, though its internal structure uses either a 16- or 32-bit bus, depending on the part number, all external communication with other Transputers and peripherals apart from local memory is carried out with a fast serial link. Each Transputer has four such links that transmit data from 10 to 20 Mbits/s. These links are designed for direct connection to other Transputers. Consequently, any Transputer can be linked to the other four.

Furthermore, each module needs just four pins for the Transputer links. Others are used for power supply, ground, clock, and system services. This arrangement eases motherboard design, which is the sixth level in Pearson's system-architecture model. Motherboards contain little else than circuitry, which is required to deliver the proper signals to a particular system bus, and two rows of sockets to receive the modules' pins.

The other motherboard device is an Inmos C004 crossbar switch, a 32-by-32 matrix that sets up the motherboard configuration. The switch serves as a programmable and reconfigurable patch panel for the Transputer communications links.

Pearson also maintains that system design is eased by the Transputer's external clock requirements. Though the T800-G25S Transputer operates with an on-chip 25-MHz clock, it requires only a 5-MHz input. And 5 MHz doesn't require difficult pc-board fabrication or layout techniques.

If designers don't know exactly how much computing power is needed for a particular application when using the IQ System's modules, a modular system can be built by picking and choosing from other various modules.

"While most people are on a steep learning curve concerning parallel computing, we can introduce them to the shallow end of the pool," says Pearson. "For $5000, they can get a respectable system to gain experience and then add modules and motherboards until they get it right. They don't have to invest $50,000 or more just to experiment."

Prices of the IQ TRAM and motherboards vary with function. The VME motherboard costs around $2000; a module with a 12.5-MIPS T800, 2 Mbytes of dynamic RAM, and 128 kbytes of static RAM costs goes for about $1000. A 100-MIPS VME board made up of eight modules is $10,000.

PETER FLETCHER

EXPERT SOFTWARE ANALYZES CIRCUITS, EMBEDS TEST LOGIC

By helping designers pin down and solve testability problems, a program developed at the Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, promises to produce more testable chips and systems without requiring designers to be versed in test techniques.

The Testability Insertion Guidance Expert System—Tiger for short—assesses a circuit's testability and design-for-test (DFT) aspects early in its design cycle. Using "what-if" techniques, it evaluates various trade-offs of DFT solutions, and then helps embed the necessary logic.

The program builds on a testable-design expert system first proposed in 1985 by Magdy Abadir as a PhD thesis at the University of Southern California. Abadir now manages MCC's Tiger project.

Within the program are mechanisms for analyzing the accessibility of various design components. It identifies the characteristics of various data-flow paths using functional and structural design information. Designs are subdivided by the software into blocks referred to as kernels. Each kernel can be independently tested by exploiting functional, architectural, and structural partitioning to come up with the best way or ways to test the design. Data-flow paths uncovered by an accessibility analysis give insight into the design's bottlenecks and point to locations that require partitioning.

Thanks to the software's expert knowledge, more than one approach can be used to evaluate each kernel. According to Abadir, Tiger might suggest 50 possible test solutions with five possible techniques. Each is ranked and scored, and then the numbers are normalized and weighed against such factors as test time, chip area, pin count, fault coverage, performance degradation, software cost and code generation, and so forth.

The design goals and constraints, which are specified by the user, are used by Tiger to dynamically adjust the weights of the solution-ranking process as it searches for a feasible design that satisfies the testability goals without violating the design constraints.

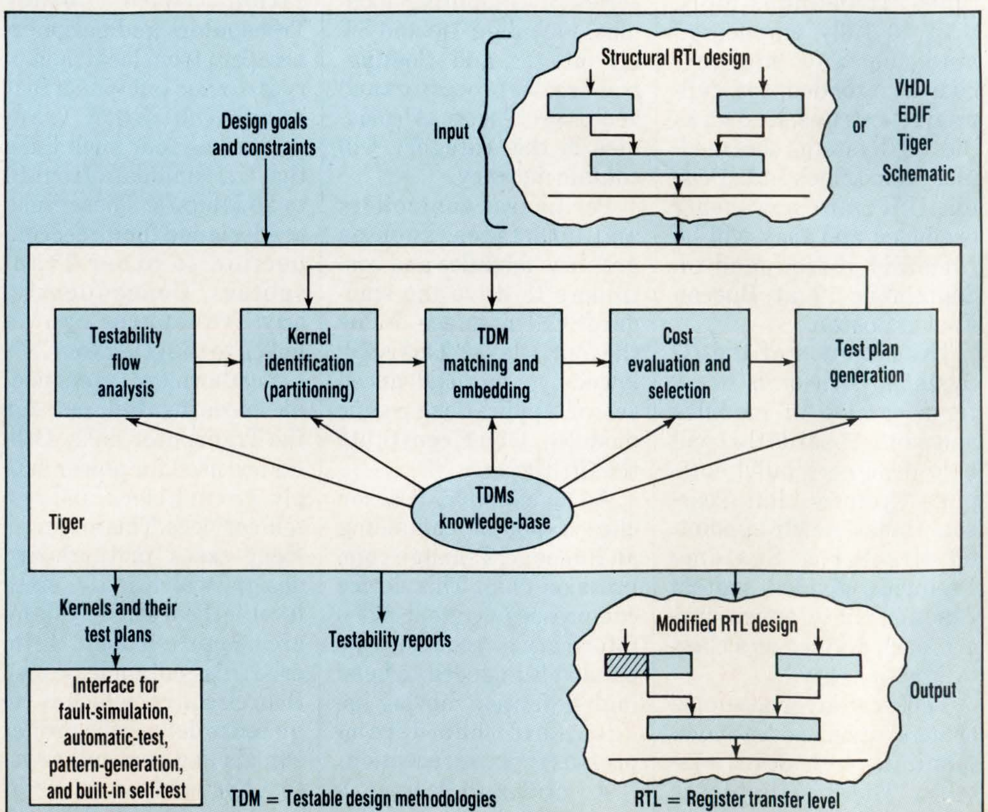
Taking matters further, the software helps compose test plans associated with the embedded solutions. Those plans contain the information required by the test-generation routines. Also, the plans describe the necessary on-chip test controller, which can be synthesized either as an individual module or as part of an existing controller.

Tiger can accept a hardware description at several levels. At the highest level, it can accept a register-transfer logic description or a model defined in a hardware-description language such as VHDL, or a circuit-description file such as EDIF. Net lists from some popular schematic-capture packages can also be input as the design nears completion. The Tiger program ties into fault-coverage estimators, test-pattern generators, fault simulators, and other analysis tools that help designers wring out a circuit.

After analysis, the final logic synthesis can be performed manually or automatically. Trials on circuits with from 1000 to 27,000 gates yielded computation speeds for Tiger of as little as 3 seconds to about 120 seconds (using a Sun 3/60 workstation with 8 Mbytes of RAM). Only a 4% area penalty was incurred by embedded test circuitry in the 27,000-gate chip. The software selected a combination of built-in self-test and scan techniques.

Though the software is already available to MCC's CAD-program participants, MCC isn't sure when it might reach the commercial market.

DAVE BURSKY



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FUTUREBUS WORK GROUPS CLOSE IN ON FINAL SPEC

THEY'RE MEETING AT BUSCON, WHICH ALSO FEATURES KEY VME, MULTIBUS, AND STD BUS INTROS.

LAWRENCE CURRAN

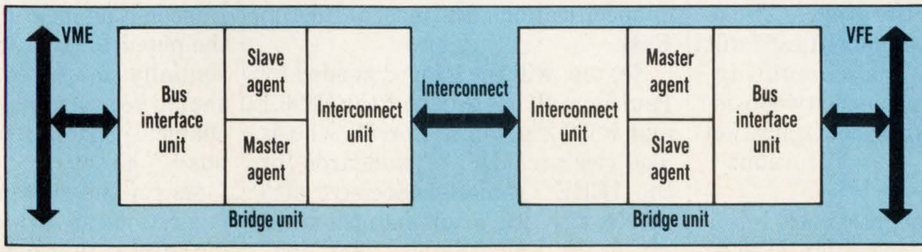
Most of the throngs of engineers attending the Buscon East show this week won't be aware of the backroom committee activity aimed at honing the specifications for Futurebus+. More likely, they'll focus on the exhibits and some key new product announcements intended to make some of today's buses—Multibus II, the VMEbus, and the STD bus—more effective until Futurebus+ becomes widely used in tomorrow's computers.

Buscon East, which takes place at the Royal Plaza Trade Center, Marlborough, Mass., Sept. 12–14, will see IEEE working groups gathered together to bring the specifications for their respective Futurebus+ projects closer to final form. The timetable calls for the Futurebus+ specification to become an IEEE standard by September, 1990. The logical layer (P896.1) of the Futurebus+ specification was essentially completed in July. Still to be finished are elements of the systems layer (P896.2), physical layer (P896.3), and system configuration layer (P896.4).

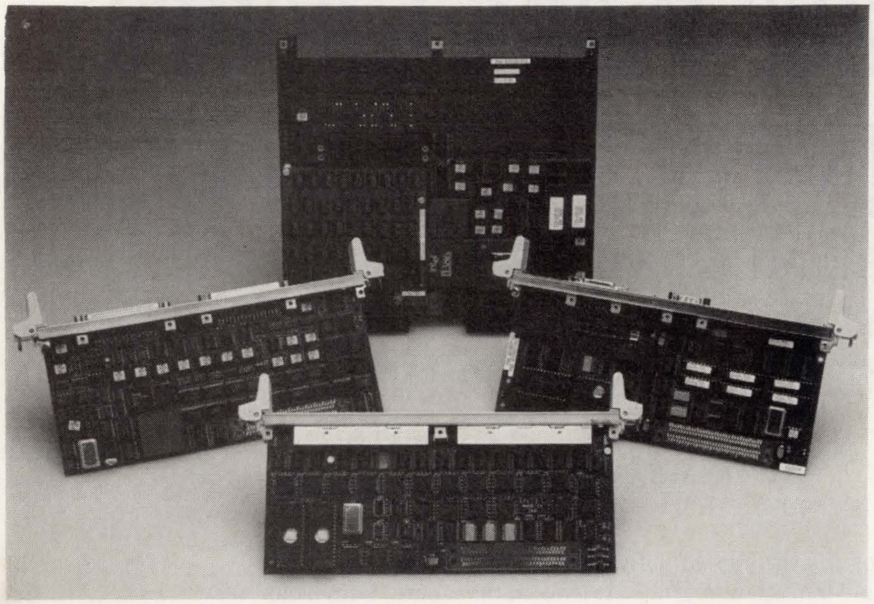
At the same time, numerous new products introduced at the show make it easier for designers to get more mileage out of today's bus structures, and to bridge the gap between 16- and 32-bit systems as well as the coming generations of Futurebus+ systems. Among the hottest developments at the show, RISC-based single-board computers will be introduced by Force Computers and Heurikon.

Futurebus+, which encompasses an advanced bus architecture intended to serve into the late 1990s, will accommodate high-performance computers—including those to be implemented with the RISC wave of microprocessors needing higher-performance buses—whose data will range in width from 32 to 256 bits. In contrast, most of today's computers are at 32 bits or less. One of the bus's main appeals is that systems built to the specification will transfer data internally substantially faster than today's systems do, with near-term transfer rates of 200 Mbytes/s within systems.

Later on, speeds as great as 400 Mbytes/s will be possible when semi-



1. A VME-TO-VFE BRIDGE shows logic required to interface between the two buses.



2. INTEL'S MIX EXTENSION for Multibus II uses a baseboard and one to three stackable modules.

conductor transceiver technology catches up with the Futurebus. Those numbers compare with about 40 Mbytes/s as the best possible with VMEbus systems, for example. The IEEE working groups have met just about monthly this year to sharpen the specifications for both Futurebus+ and bridges that link currently used buses with the coming Futurebus generations.

Late last year, working groups planning the Futurebus, the Rugged Bus, and the Next Generation Architecture (NGA) of the VMEbus, came to an important agreement: Each would back Futurebus+ as the structure most appropriate for high-performance, 32-to-256-bit computers (ELECTRONIC DESIGN, *Feb. 9, p. 31)*.

The IEEE Computer Society-sponsored Futurebus and Rugged Bus committees merged and are incorporating Rugged Bus needs into the Futurebus specification. Those needs include accommodating fault tolerance, real-time computing, maintainability, and security considerations in the system configuration layer (P896.4) of the Futurebus+ specification.

At the same time, the VME International Trade Association (VITA) selected the Futurebus as its basis for the VMEbus' so-called Next Generation Architecture. VITA then worked to hammer out a VME-to-Futurebus bridge specification.

Achieving an agreement among these working groups about a common hardware bus architecture was a major milestone. Paul Cook, chairman of the IEEE P896.3 and P896.4 working groups, noted that having Futurebus as a single hardware interface means that the industry can create common hardware modules for it, "just as Unix enables software modules to be created for a common software interface."

Cook is a member of the technical staff at Ameritech Services Inc.'s Applied Technology and Development Organization, Schaumburg, Ill. His two P896 working groups, which are tasked with incorporating the former Rugged Bus needs into the Futurebus+ specification, as well as working out the physical layer specifications, will meet at Buscon East.

So, too, will the groups headed by Paul Borrill, chairman of the P896.1 and P896.2 groups. Borrill, who is also vice president of standards for the IEEE Computer Society, also carries the title of distinguished engineer at Sun Microsystems Inc., Mountain View, Calif., where he manages the S-bus architecture and development group.

Borrill is pleased that the 896.1 group handling the logical layer produced a draft Futurebus+ specification on schedule in July after reviewing the suggested revisions and comments that surfaced at the June meetings. He points out that provisions of the original 896.2 systems layer were incorporated into 896.1, and that a new 896.2 task will determine what is now called the profile and physical layer of the Futurebus+ specification.

The new group is addressing such considerations as board sizes and connector configurations. Eventually, this part of the specification may include, for example, a large industrial-size board, a smaller workstation board, and a ruggedized board for military applications.

Recent developments that are under consideration by Cook's 896.3 working group include a proposal from Hewlett-Packard that a desktop-computer-sized board that supports both an EISA bus and a 64-bit Futurebus+ be included as one of the Futurebus mechanical standards. Another proposed mechanical standard would have pure metric packaging and metric connectors for use in Europe, which is expected to go fully metric in 1992. The current Eurocard format is a mixed English-metric system.

In response to those proposals, the 896.3 working group recommended to the IEEE Computer Society's Microprocessor Standards Committee that study groups be created to investigate the need for those suggested standards. These study activities may later necessitate new project authorizations from the committee and some reorganization of 896.3.

Cook says that after this week's Buscon East meetings, he hopes that the physical layer (896.3) draft is essentially completed. "The document should be at a point where it's the mechanical specification for Futurebus+," he says.

As for the systems configuration layer, Cook says that the 896.4 working group will continue writing a draft at this week's Buscon East meeting. The draft will specify how to use boards that meet the provisions of 896.1 and 896.2, and which boards accommodate fault-tolerant and real-time computing, as well as maintainability and security considerations. The draft will be circulated for official working group ballot and comments at a December meeting.

Putting it all together, Borrill notes that he plans to have an overall IEEE Computer Society Futurebus+ draft document ready by October. For six months, this document would be available for public comment by interested parties.

Borrill points out that the International Standards Organization, like the IEEE, requires a six-month comment period for its standards, and that this period for the Futurebus+ specification for both organizations coincides. He looks forward to having the Futurebus+ specification as an approved IEEE standard next September. But achieving this will be no small feat, considering how large the working group meetings have become. "Just about every major company is sending representatives to our meetings," Borrill says, "but we've got top-notch people in the groups, and they've remained essentially on schedule." He expects 32-bit system designers to hop on the Futurebus in the next two years; 64- and 128-bit Futurebus architectures should follow, beginning in 1991.

Bridging The Gap

Wayne Fischer, director of marketing at Force Computers Inc., Campbell, Calif., is keenly interested in the eventual Futurebus+ provisions, but his near-term attention is focused on how today's VMEbus-based systems will link to Futurebus when it arrives. Toward that end, Fischer is chairing a working group charged with coming up with a bridge specification that will enable a hardware/software migration path from VME to the Futurebus.

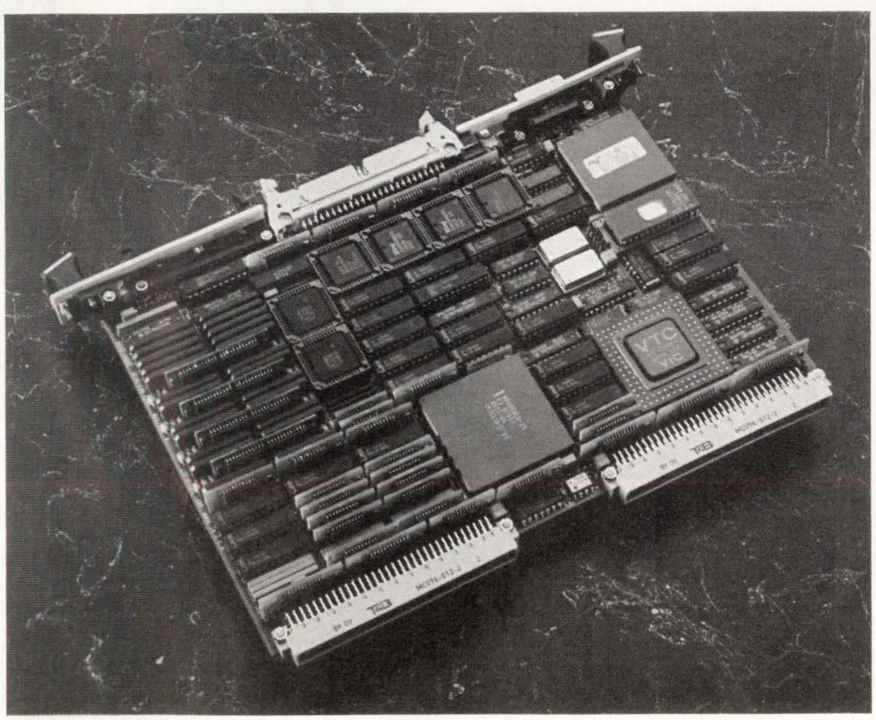
The effort is called the VME-to-VME Futurebus+ Extended (VFE) bus bridge; the IEEE working group is P1014.2. In addition to offering a migration path, such a bridge will also accommodate the coexistence of two bus architectures in the same system, so that the VME segments might handle I/O functions, for example *(Fig. 1)*.

Fischer points out that the VME-to-VFE bridge is best understood in the context of a local-area network. "Both VMEbus and VFE can be considered as high-speed, parallel LANs in which a variety of CPUs, memory, and I/O boards can be plugged into the backplane," he says. Each board becomes a communication node on its respective backplane.

As a result, when two different systems—each with a different kind of backplane and associated protocols—must talk to each other, a mechanical and electrical bridge must be established to enable the movement of information between them. "The networking community calls this a gateway," Fischer explains, "but in both the Futurebus+ and VFE Bridge working groups, it was mutually decided to use the term 'bridge' to encompass the total activity of specifying the interface between the two buses."

Besides promoting easy migration to VFE (Futurebus+) systems and coexistence of these two buses in one system, there are other goals for the VFE bridge specification. It's also intended to help the VMEbus be used as a secondary bus for I/O operations in VFE systems. Furthermore, the bridge specification should make it possible for software to reach into the other buses for I/O and memory accesses while executing on either the VMEbus or VFE.

Fischer says that the assumption is that the bridge will be implemented as two boards *(Fig. 2)*. His group was to complete the definition of the interface between the two buses by the end of last month. He hopes to have a final version of the bridge specification for the Oct. 30 meeting of the Futurebus+ working groups.



3. HEURIKON'S SINGLE-BOARD COMPUTER is the first to use the Intel 960 RISC microprocessor.

Product Introductions

Although systems are being designed for Futurebus+ ahead of the specification's completion, the effects of this new bus architecture won't be widely felt for several years. In the meantime, both board and device vendors continue to find ways to extend some of today's bus architectures, to improve the performance of systems implemented on those buses, or to make it simpler to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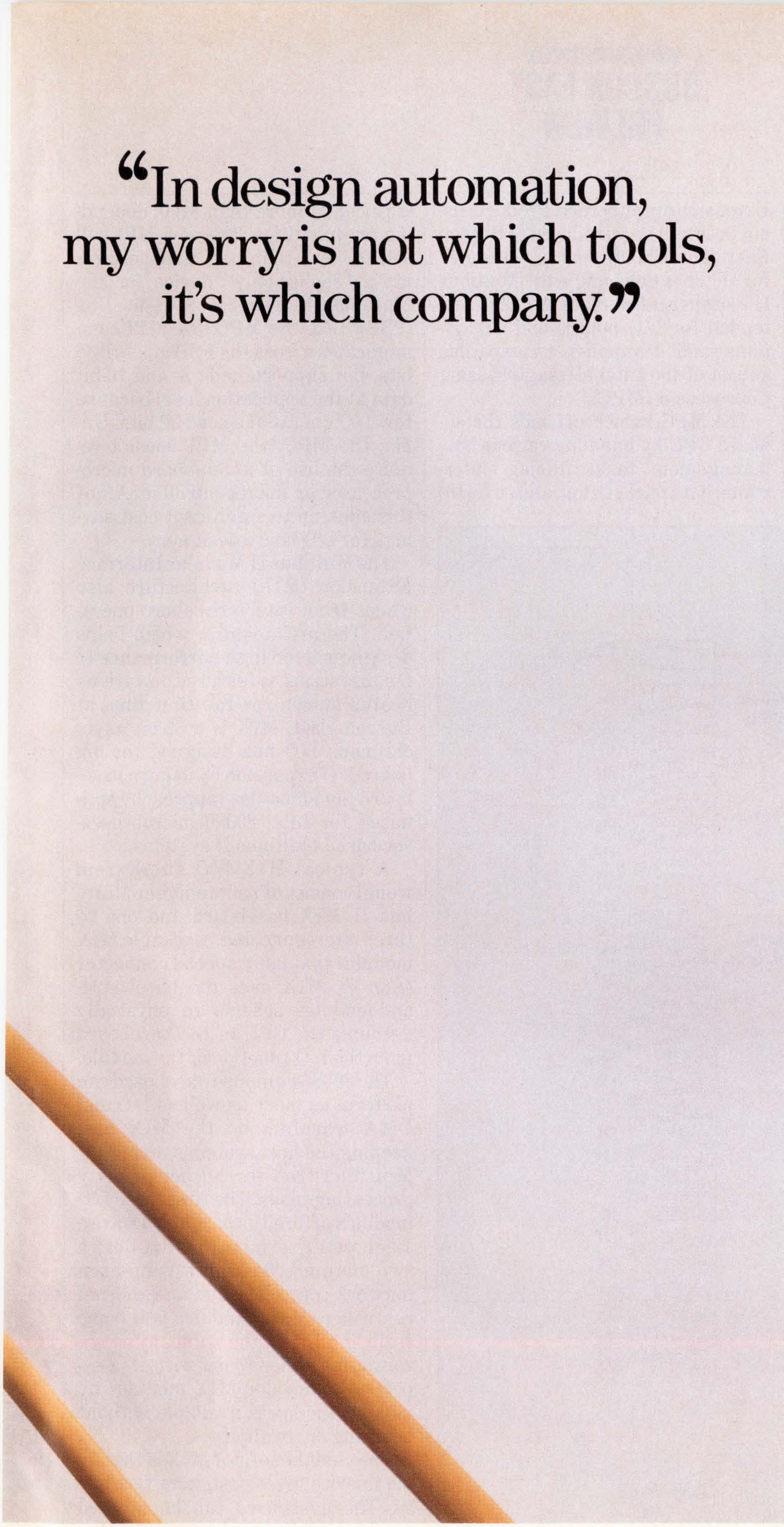

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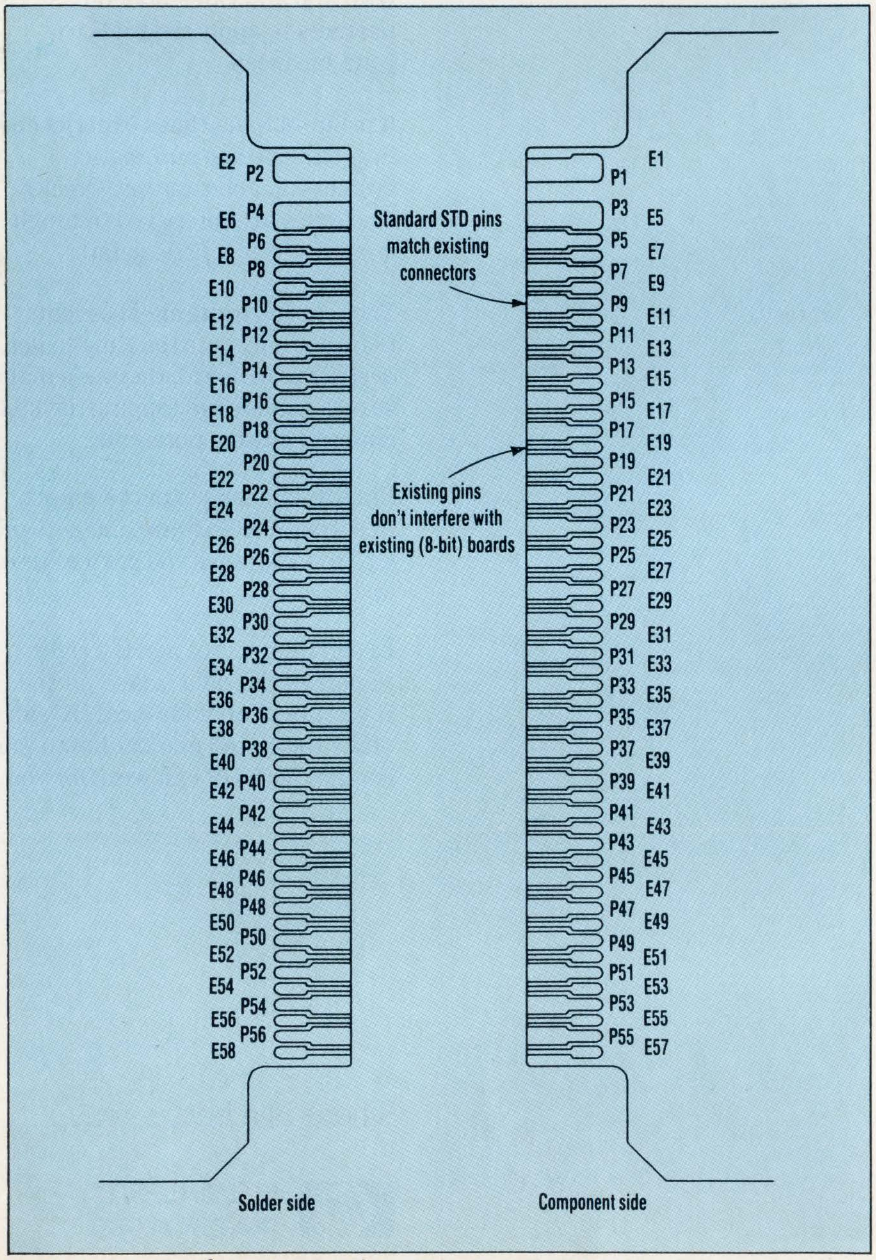
interface with some of those buses.

Several of the products bowing at Buscon East are intended to help designers achieve those ends. Some of the companies unveiling products or making other significant announcements are Concurrent Technologies, Force Computers, Heurikon, Intel, WinSystems, and Ziatech.

Intel's OEM Modular Systems Operation, Hillsboro, Ore., has two new Multibus II developments: an interface device and a Modular Interface Extension architecture. Products using both will be introduced at Buscon East. The CMOS device, scheduled for October delivery, is the Multibus II Peripheral Interface (MPI). It's intended for I/O boards and subsystems, and it supplies a compatible subset of the Intel Message Passing Coprocessor (MPC).

The MPC, which offloads the on-board CPU by handling various bus-management tasks (timing, interrupts, data packetizing, and so forth) is priced at more than $100, depending on quantities. The new MPI will sell for less than half that because it's a "replier-only" device for the Multibus II Parallel System Bus (PSB). Like the MPC, the MPI communicates across the PSB at a full 32 bits, but supports only 8- and 16-bit data at the application level because few I/O operations need 32 bits. Unlike the MPC, the MPI doesn't require the use of an on-board microprocessor or microcontroller. All of this adds up to significant cost savings for I/O board designers.



4. ZIATECH'S CONNECTOR CONFIGURATION is associated with the company's proposed STD 32 specification.

The Multibus II Modular Interface Extension (MIX) architecture also comes from Intel's Hillsboro operation. The architecture, which helps designers build high-performance I/O subsystems, is featured on various boards shown for the first time at Buscon East. MIX is a 32-bit asynchronous I/O bus designed for on-board I/O expansion by using a baseboard-plus-modules approach optimized for Intel 80386 microprocessor-based Multibus II systems.

A typical MIX I/O subsystem would consist of an intelligent Multibus II MIX baseboard and one to three interconnected, stackable MIX modules that use a special connector *(Fig. 3)*. MIX uses the baseboard-and-modules scheme to physically decouple the CPU of the baseboard from the I/O function of the module.

The 80386-equipped baseboard can perform memory as well as I/O and DMA transfers on the MIX bus, keeping the host system's main 386/Multibus free for higher-priority processing tasks. The first three I/O modules offered as part of MIX are a 12-channel terminal controller; a two-channel, 64-kbit/s wide-area network controller; and an Ethernet controller. More modules will come from Intel, and the company is encouraging other firms with I/O expertise to develop MIX modules by making the specs available without licensing or royalty fees.

The chief benefit of MIX is that its modularity gives designers flexibility. The baseboard can be tailored quickly because of the various interchangeable I/O modules that are available.

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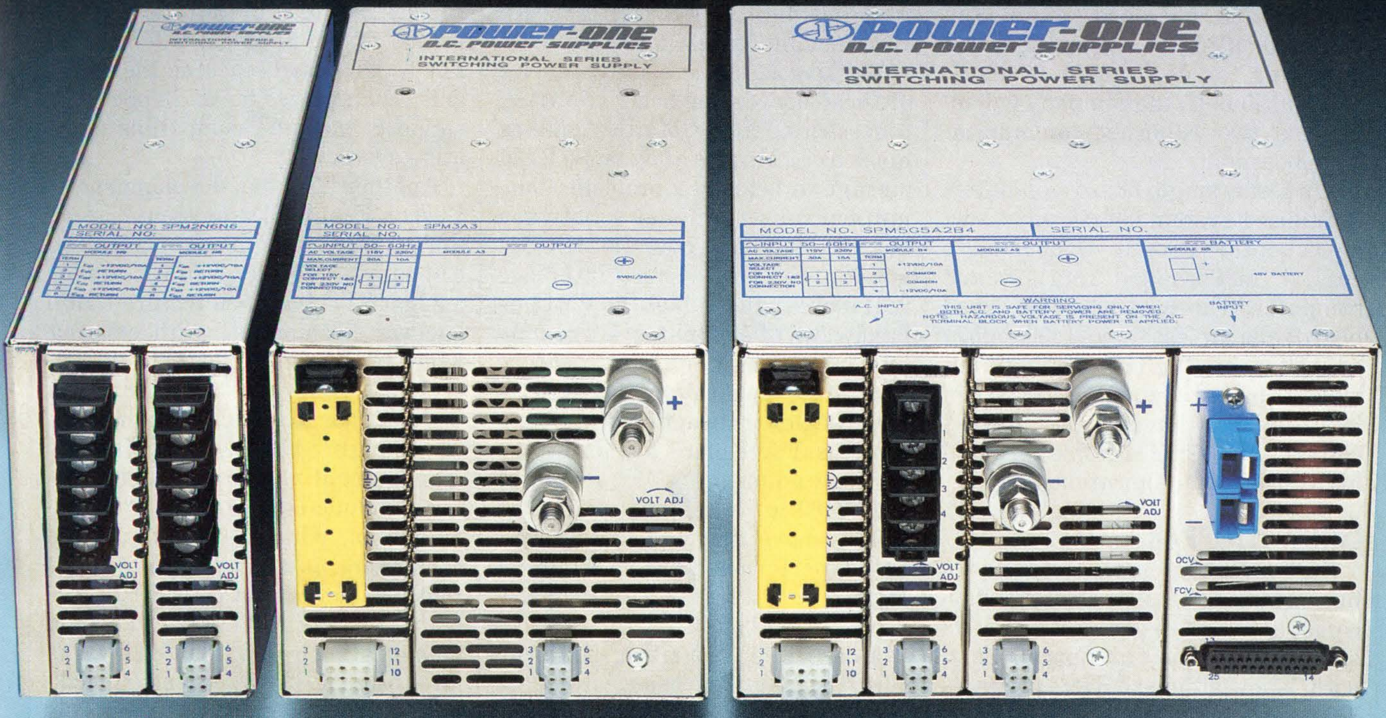

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BUSCON EAST PREVIEW

Other Multibus developments at Buscon East come from Concurrent Technologies, Champaign, Ill., in the form of boards using the Intel 80386 and 80386SX microprocessors. One is the CP1386/16X, a single-board computer for Multibus I systems. For Multibus II, the company will introduce two Ethernet communications boards.

With the single-board computer, Multibus I system users gain a lower-cost alternative to Concurrent's earlier 80386-based single-board computer. The new 80386SX-based board sells for less than $1900 each in quantities of 100. The existing unit, which is priced at about $3500 each in lots of 100, is intended for process control, industrial automation, and high-speed communications.

Show Stoppers

Still a leading high-performance bus until and even after Futurebus+ comes along, the VMEbus will get its share of attention at Buscon East, with "show-stopper" RISC products from Force Computers and Heurikon Corp. Force made will make a splash with a Motorola 88000 RISC-based single-board computer family, while Heurikon will unwrap the first board-level computer to feature Intel's 66-MIPS RISC microprocessor, the 960, which was officially introduced on Sept. 12.

Force believes that its CPU-8X family with up to 340 MIPS per card cage thrusts the company into the domain served by multiprocessing systems. That's achieved by closely coupling 10 pairs of boards, with each pair delivering 34 MIPS.

Three boards make up the series: The CPU-80 contains a 20-MHz 88100 RISC CPU and two 88200 cache memory management units (CMMU), as well as 4 Mbytes of shared dynamic RAM. The board supports the VMEbus interface and also has a SCSI disk-drive interface. The CPU-81 is identical to the CPU-80, except that it replaces the SCSI interface with a VME Subsystem Bus (VSB) interface. VSB represents a local bus that can be used for I/O expansion.

The CPU-82 acts as a "dyadic" or closely-coupled companion processor to either of the other two. It has an 88100 CPU, two or three 88200 CMMUs, 8 Mbytes of shared dynamic RAM, and a VSB interface. An Ethernet interface is optional.

Working in tandem, a dyadic pair of these boards can bring two RISC processors, five CMMUs, and as much as 12 Mbytes of dynamic RAM storage to bear on a problem. Communications to memory between boards takes place over the MBUS, a 100-Mbyte/s interboard interface that more than doubles the VMEbus bandwidth of 40 Mbytes/s. The family is intended for high-end, real-time computing applications, as well as large-scale, transaction-processing systems. Force plans to improve the series by adding a 25-MHz version of the 88100 in the second quarter of 1990, a move that will boost single-board performance from 17 to 21 MIPS—or to 420 MIPS for 10 dyadic pairs in a card cage.

Meanwhile, Heurikon, Madison, Wis., will impress show attendees with the HK80/V960E, a VMEbus single-board computer believed to be the first product to incorporate Intel's 960CA 32-bit RISC microprocessor *(Fig. 4)*. The board offers peak performance of 66 native MIPS and 30 VAX MIPS. Heurikon claims that at its $2795 price, the board offers the best price/performance ratio of any RISC or CISC single-board computer on the market. It's intended for real-time applications, including intelligent I/O, communications, embedded control, and image processing. The 40-MHz 960 chip includes a 1-kbyte instruction cache, 1 kbyte of static data RAM, and a four-channel 32-bit DMA controller.

A product billed as the first 20-MHz single-board computer for the STD bus will be shown for the first time by WinSystems, Arlington, Texas. The MCM286AT-20-2M is a 16-bit board that the company says is the fastest 80286 CPU board for that bus. WinSystems' previous 286-based STD product, introduced a year ago at Buscon, runs at 16 MHz. That board—the STD-AT—offers performance that's 19 times better than an IBM PC/XT, as measured by the Norton SI benchmark. In contrast, the new board runs 23 times faster than the XT on the same benchmark. It all adds up to the new board's ability to top the performance of the IBM PS/2 Model 80. The $1995 board features the Chips and Technologies Neat ChipSet and supports most AT-compatible operating systems.

Another STD bus development at Buscon East will come from Ziatech Corp., San Luis Obispo, Calif. The company produced specifications for a 32-bit STD bus architecture that's backward-compatible with existing 8-bit standards. Called STD 32, Ziatech will offer the specifications without charge to the STD community through STDMG, the STD Bus Management Group. The specifications include edge-connector tab dimensions, which match available connectors, as well as the use of pins that don't interfere with existing 8-bit boards. With STD 32, users could plug existing 8- and 16-bit STD cards into the STD-32 bus extension backplane. They could also plug new STD-32 bus extension cards into the backplane of existing 8- and 16-bit STD bus systems.

Ziatech undertook development of STD 32 after the firm's market research indicated that system designers would stay with the STD bus if they were assured that it offered a growth path to 32 bits. One 16-bit STD specification was proposed to STDMG but has not yet been accepted. STD 32 would leapfrog to 32 bits, but also accommodate 16-bit designs with a growth path.

Rob Davidson, Ziatech product manager, says that refinements are still needed before STD 32 can be put into production. "But in conversations with suppliers of connectors and other portions of STD technology, we've determined that every specification is producible," he says. Ziatech is already developing products using the new architecture.☐

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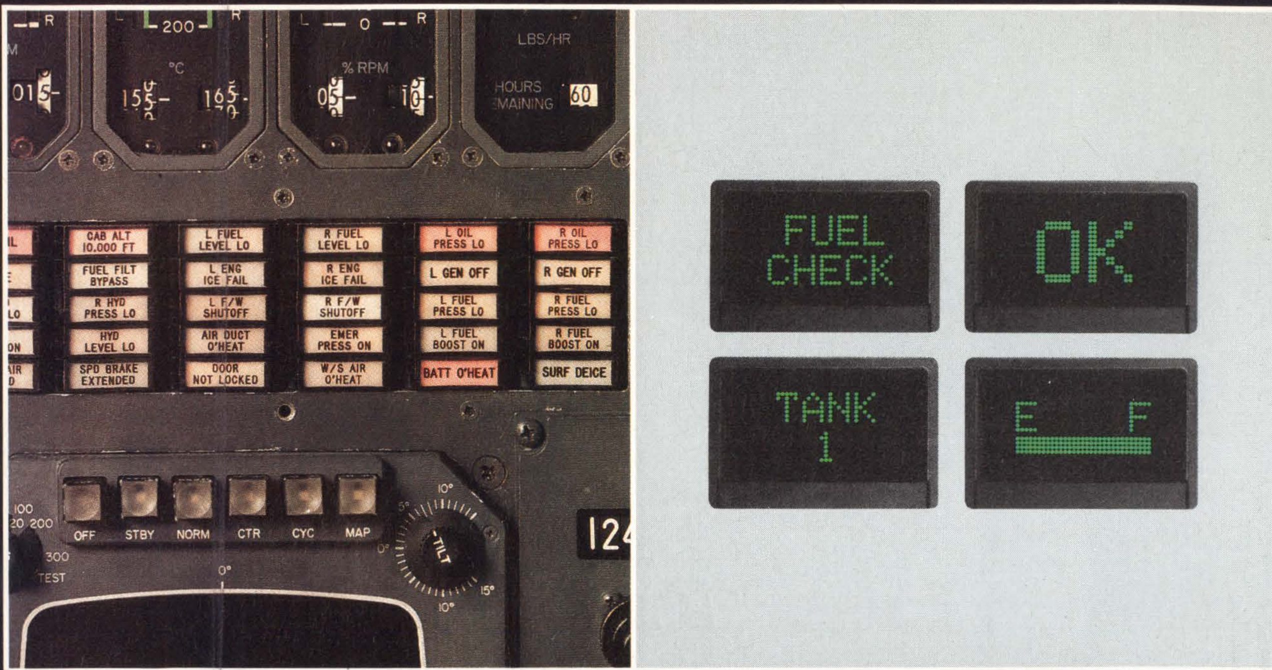
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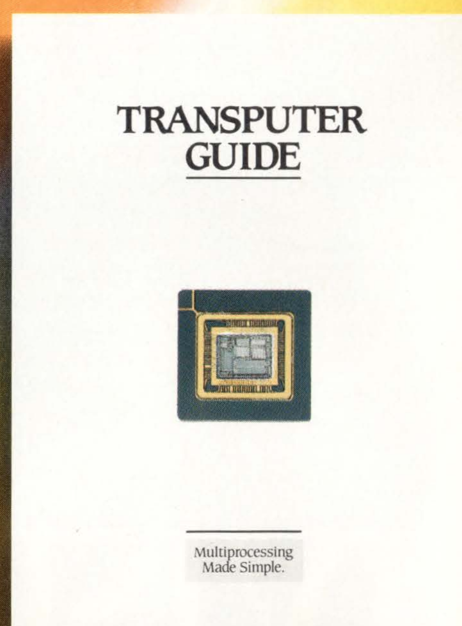

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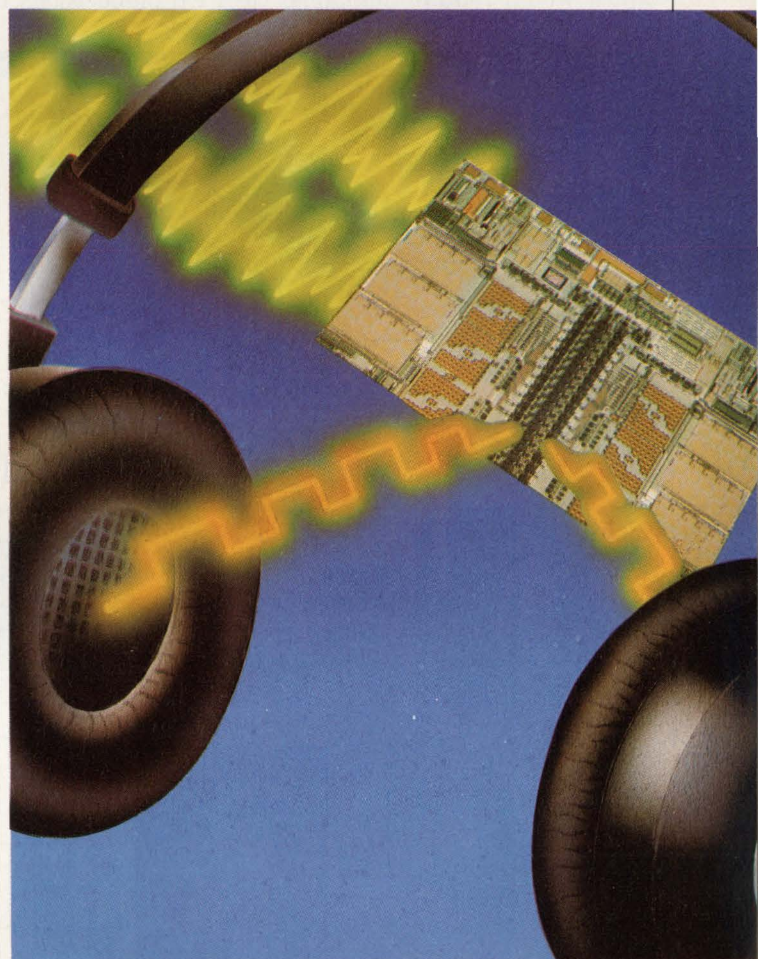


When designing mixed analog-digital systems, large numbers of dc-to-audio-band analog channels must be digitized to at least 14-bit accuracy. Now there's the PCM1705P, the first monolithic a-d converter with more than 16-bit resolution that can handle signals of more than a few hertz. Available from Burr-Brown, it runs at 200 kHz and gives 14-bit, no-missing-code accuracy for under $14. In addition, two of these converters are contained on one chip.

The PCM1705P, a dual 18-bit CMOS a-d converter, was developed for high-end consumer digital-audio applications and is currently specified for only those jobs. When oversampling 20 kHz audio by a factor of four at 192 kHz, total harmonic distortion plus noise runs a maximum of –92 dB. It's used in digital- audio tape (DAT) player/recorders and various consumer applications, which include the front end of stereo systems that employ digital-signal processors for special effects, and digitizing stereo audio for video recorders (camcorders).

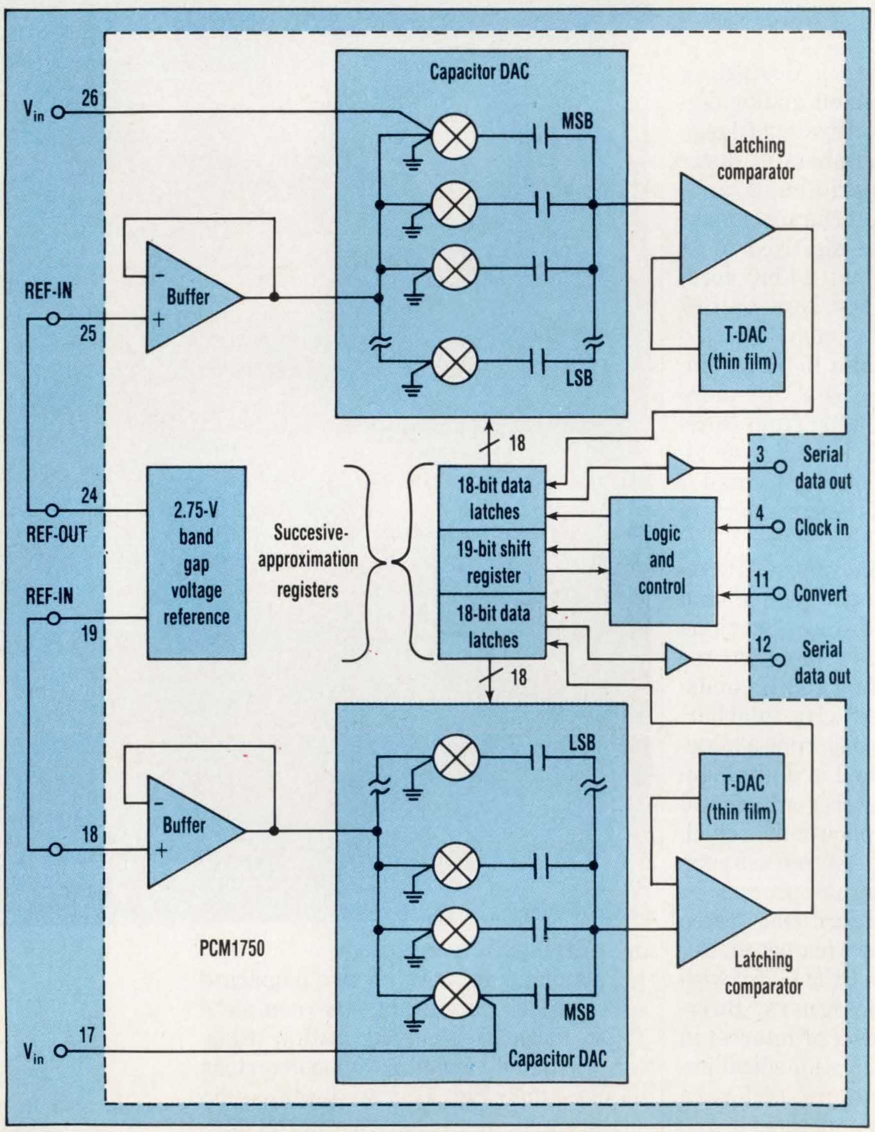
After discussing the PCM1705P with traditional system designers, Burr-Brown found a high level of interest in many applications, such as medical imaging, telecommunications, and various systems with DSPs at their heart. For instance, in virtually any DSP application the processor can up the a-d converter's signal-to-noise (S/N) ratio by 9 or 10 dB just by averaging.

This machine, with its two disparate sets of specifications, has two complete 18-bit, successive-approximation register, switched-capacitor a-d converters on one chip *(Fig. 1)*. The digital-audio requirement demands two serial outputs that minimize die size and conveniently put the chip into a reasonably-sized 28-pin DIP (imagine working with

36 output lines from a 64-pin package). Some system designers may still employ parallel outputs, but most of them try to cut the number of bus lines on a board. In addition, if you need the data in parallel form, registers (which are usually inexpensive) can be used. The serial bits are clocked out by the master clock, with each bit available one clock cycle after a bit decision.

The converter pair employs a classic, binary weighted, switched-capacitor architecture to minimize chip size (160 by 160 mils). Segmentation, which would require additional capacitors, isn't employed. Like most a-d converters using switched capacitors, the architecture offers inherent sampling. Moreover, because the two converters run in synch, designers can simultaneously sample two dynamic signals. Typical jitter (aperture uncertainty) is just 50 ps, translating into a full-power bandwidth of 25 kHz, and an equivalent noise between channels of just 20 μV.

Running in synch also ensures that the digital switching noise from one converter doesn't pollute the sampling of the signal, or effect critical bit-decisions by the auto-zeroed comparator in the other converter. In the stereo application, minimum noise is crucial in reaching the –92 dB signal-to-noise ratio. The simultaneous sampling eliminates the phasing error found in systems that alternately sample and convert one channel and then the other.



1. SWITCHED-CAPACITOR TECHNOLOGY and a successive-approximation architecture are employed by Burr-Brown's PCM1750 dual 18-bit a-d converter to achieve a 92-dB signal-to-noise ratio while sampling a 20-kHz signal at 200,000 kHz.

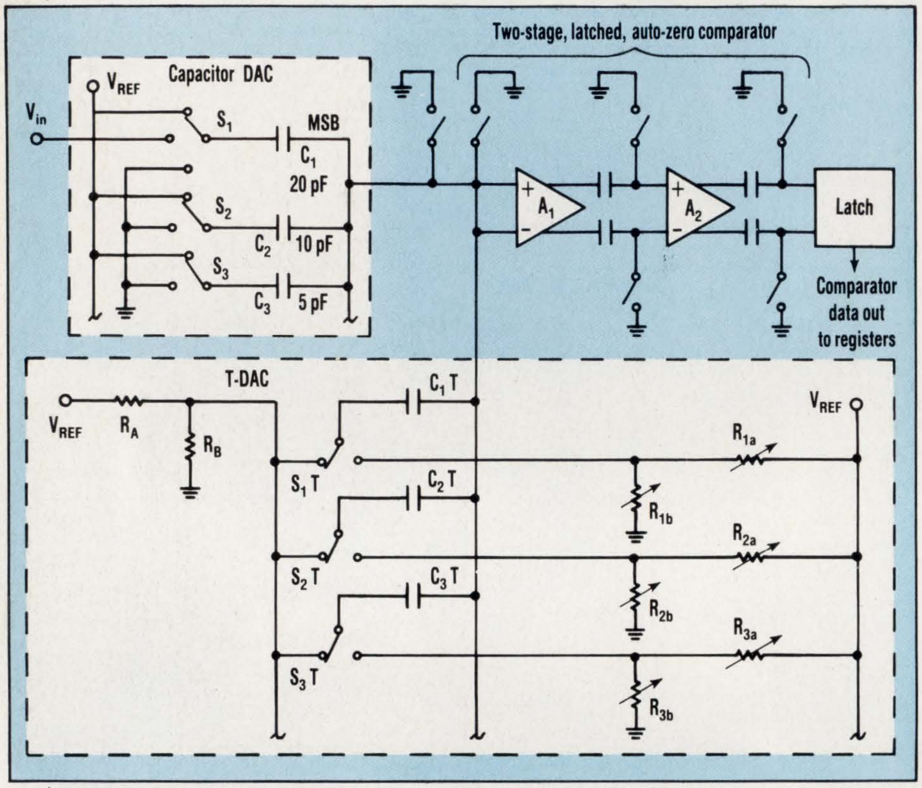
The chip also has it's own 2.75-V voltage reference, with separate fast-settling buffer amplifiers driving each of the capacitor d-a converters. The reference employs a low-noise band-gap circuit, but the circuit isn't low-drift. Consequently, the resulting gain temperature coefficient of the two converters can be as great as 250 ppm/°C. Gain accuracy at 25°C runs a maximum of ±5%.

An internal reference is fine for audio applications, but it doesn't always suffice for other applications where greater precision is needed. By using the REF-Out and REF-In pins that are supplied for each channel, a higher-precision reference can be used. Because the reference voltage to the d-a converter determines the maximum value of the input signal (±2.75 V), changing its value alters the full-scale input voltage.

Burr-Brown is currently only supplying typical (but conservative) specifications for non-audio applications. However, accurate characterization for more traditional applications is underway. As noted, basic accuracy (no missing codes) is 14 bits, while differential nonlinearity (DNL) and integral nonlinearity run ±0.002% and ±0.003% of full scale, respectively. Power consumption, which is important to all potential users, is just 300 mW maximum for the PCM1705P; 28 mA from a +5-V rail; and a mere 13 mA from a –5-V rail.

There are diverse nonconsumer applications for the PCM1750. Today, the front end of a typical, multichannel, medical imaging system consists of an expensive, true 16-bit a-d converter with a throughput rate in the neighborhood of 500 kHz. Between the converter and the signals lie signal-conditioning circuitry for each channel, a high-speed analog multiplexer, and a high-speed, 16-bit-accurate, sample-and-hold amplifier (or often a buffer amplifier or a sam-

COVER: DUAL 18-BIT ADC IC



2. THE PCM1750 DUAL 18-BIT a-d converter employs trimming or T-DACs that use laser-trimmed thin-film resistors to trim its 18-bit switched-capacitor d-a converter.

ple-and-hold amplifier per channel ahead of the multiplexer). Switching to one-half of a PCM1750P per channel (though only 14 bits accurate) can actually produce a better image, and in some applications, a lower-cost system. Eliminating the multiplexer and sampling amplifier(s) significantly reduces timing jitter, resulting in nearly 1 bit less blur in the image.

Telecommunications applications range from digital-cellular telephones to echo cancellation in high-end (V.32, 9600-baud) modems. Both represent forms of DSP applications. The extra (14-bit) resolution and accuracy eliminate the need for compression and/or gain-ranging circuits. The processor only uses the bits it needs. Low-cost instruments or systems that can run a fast Fourier transform on signals from dc to over 20 kHz represent another DSP system application. Often employed for vibration analysis, they're finding their way into engine test laboratories (both internal-combustion and jet engines). For example, by continually examining the spectra of a diesel locomotive engine, the system can determine when to perform a major overhaul.

The PCM1750 is created on Burr-Brown's 3-μm, p-well, CMOS process, which builds stable, low on-resistance analog switches and precision, polysilicon-oxide-polysilicon capacitors. It also has two layers of metal, and builds laser-trimmable nichrome film resistors. In each converter, the capacitors are used in the two-stage, auto-zeroed, latched comparator; the main capacitor a-d converter; and in a trimming d-a converters. The resistors are used exclusively in the trimming d-a converters.

Polysilicon plate capacitors have stability and matching characteristics equal to or superior to other precision components, such as thin-film resistors. On a well-controlled process, ratio matching typically runs 0.1%, which is a respectable number for an untrimmed component. Even more impressive, the capacitors ratio-track over temperature to about 0.1 ppm/°C; drift overtime is similar.

Achieving a DNL error of better than 1 least-significant bit (at 18 bits) requires ratio matching of the "more significant bits" to better than 0.001%, or 100 times better than the process offers. Therefore, some form of calibration of the "upper bits" is mandatory. On the other hand, ratio tracking over temperature is so superb that DNL changes less than 1 LSB at 18 bits over a 50°C temperature change. As a result, factory calibration rather than field (on-chip) calibration or trimming makes sense, further reducing die size, power, and cost.

Both converters, which are trimmed at the wafer-probing stage with their own on-chip, T-DACs, are built with polysilicon capacitors and thin-film resistors *(Fig. 2)*. Instead of changing the capacitor's value, (ELECTRONIC DESIGN, Feb. 9, p. 26), the reference value is changed.

This is how it works for one bit: Switch S_1T (in the T-DAC) switches one plate of capacitor C_1T between two different voltage levels; a "reference" level is set by a fixed divider formed by R_A and R_B; and a correction level is set by laser trimming the divider formed by R_{1a} and R_{1b}. The difference between these two voltages is coupled by C_1T to the comparator's minus input to generate a correction voltage for bit 1. The correction voltage changes a reference level for bit 1 at the minus input to the comparator. If C_1 is too large, the correction voltage is raised; if it's too small, the voltage is lowered.□

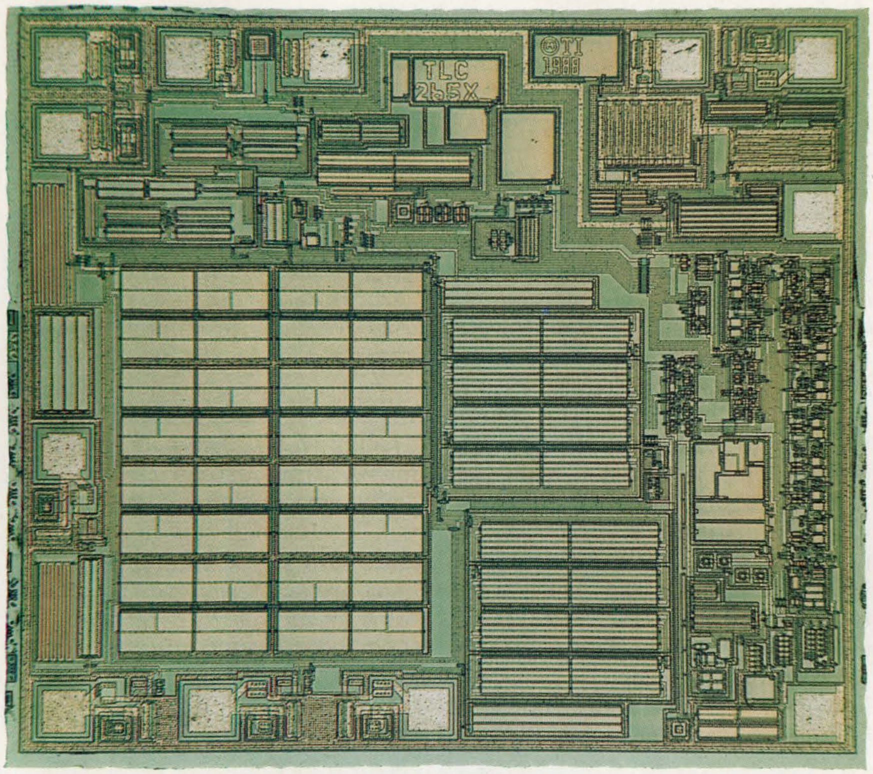
PRICE AND AVAILABILITY

The Burr-Brown PCM1750 dual 18-bit a-d converter, in a 28-pin double-width plastic DIP, goes for $26.90 in quantities of 1000. Small quantities are available from stock.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; Randy Skinner, (602) 746-7270.

CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	556
MODERATELY	557
SLIGHTLY	558



PICKING IC OP AMPS: IT'S NO LONGER EASY

WITH IMPROVED PROCESS AND CIRCUIT DESIGN, IC OP AMPS CHALLENGE RIVALS.

FRANK GOODENOUGH

Over the last few years, the IC op-amp jungle has come to resemble the Amazonian rain forest in the number and diversity of its species. This diversity stems from advanced processing and trimming techniques coming on-stream. Op-amp chip designers have had a field day defining and designing new families of op amps with greater performance—at lower prices. Developments continue, with each new design from each company optimizing one or more of the 40 plus performance specifications carried by every quality op amp.

Continued developments in junction-isolated-complementary-bipolar (JICB) and CMOS processes are the driving forces behind the op-amp explosion. Complementary bipolar processes build fast vertical npn transistors and fast vertical pnp transistors rather than slow lateral pnps, such as the ±15-V, standard, analog, bipolar process. TTL and ECL processes usually don't even build pnp transistors.

Both JICB and CMOS processes demand different design techniques or architectures. Furthermore, skilled designers have taken existing analog and digital bipolar and MOS processes and stretched the performance of the op amps built on them to new highs through innovative circuit techniques. While complementary processes of all types have made linear IC design simpler, op amp designers have taken full advantage of the processes to offer price-performance peaks.

Because of their process and architectural differences, members of each new op-amp family tend to be different from members of all the other families—it matters little that they're from the same company. In contrast, virtually all IC op amps that were bought a few years ago, with the exception of chopper-stabilized and dielectrically isolated (DI) devices, were built on essentially identical bipolar processes with very similar designs. Most op amps, such as the 741, 324, and 355, and logic ICs were multiple-sourced with identical specifications. But today, we find a multitude of models representing an impressive array of processes and designs. In fact, designers can find devices from processes as disparate as standard bipolar and CMOS aimed at the same application. With few exceptions, nothing is standard from one new op amp to another except for their basic pinouts.

PRODUCT PERMUTATIONS

General-purpose IC op amps (unity-gain stable devices for which speed or bandwidth aren't prime specifications) range from less than \$0.25 each to more than \$25. Their guaranteed maximum offset voltages go from less than 15 μV to more than 15 mV. Offset voltage (V_{OS}) drift spans a similar two decades. Bias current (I_B) sweeps a far greater savanna, from less than 100 fAs to hundreds of nAs—a ratio of 10,000,000 to one. In addition, the temperature coefficient (TC) of these static specifications can differ radically from device to device.

Dynamic specifications are just as diverse as static specifications. Open-loop gain (A_{OL}) runs from 40 to 140 dB, unity-gain bandwidths run from hertz to gigahertz, minimum supply voltages span from 1 V to 12 V or more, and quiescent currents vary from 15 μA to over 15 mA. Other widely varying specifications, each important for many applications, include common-mode and power-supply rejection ratios, common-mode voltage range, settling time, full-power bandwidth and slew rate, distortion, and phase and gain margin. Moreover, most of these specifications aren't only a function of temperature, they're are also a function of supply voltage and load impedance—the test conditions for the specification. Change any one of the conditions and it's often a whole new ball game. For example, some of the low-supply-voltage op amps have higher offset voltages at low supply voltages rather than at high supply voltages.

To further exacerbate the IC op amp inflation, the "big three" (National Semiconductor, Motorola, and Texas Instruments) and others are bringing out each new device in single, dual, and quad versions; in three temperature ranges; and often in one or more performance grades. Finally, op-amp package types extend from TO-8 cans and plastic or ceramic DIPs to nearly any surface-mounted design.

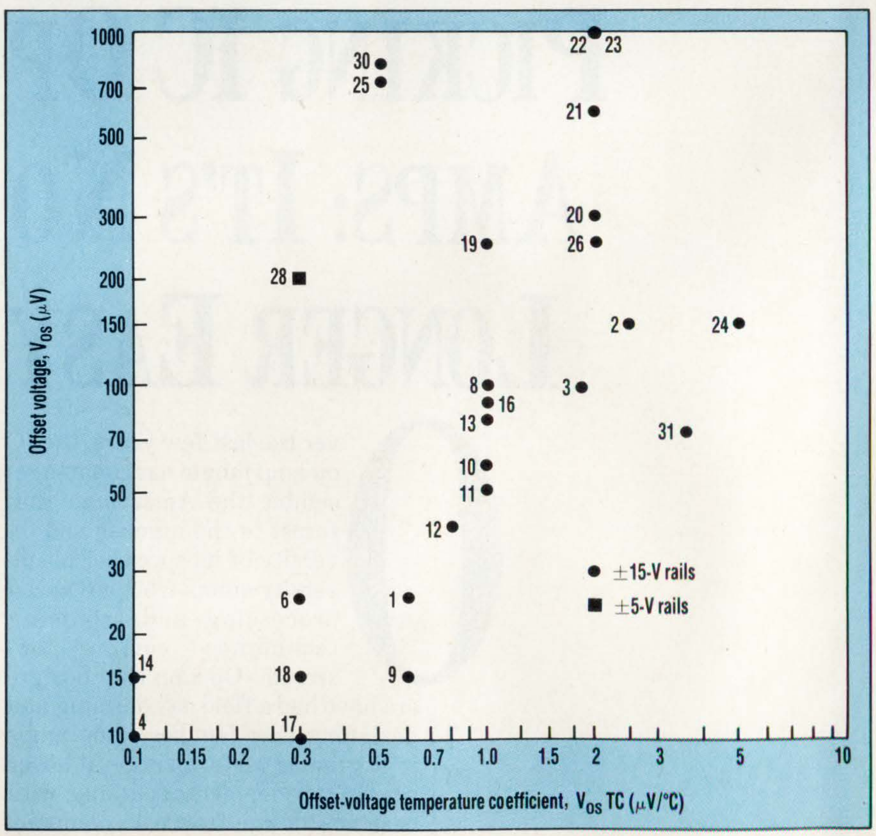
And if product proliferation is a problem for designers, consider what it must be like for manufacturers. One Motorola op-amp family, the MC33071, has 42 models. However, several of Motorola's latest families have just two or four. One Analog Devices' op amp, the ultra-low-drift AD707, has 18 models in single-op-amp versions. A dual version, the AD708, adds nine more. Raytheon's ultra-low-drift RC4077/4277 has 26 models (5 duals). Precision Monolithics (PMI), however, has kept its ultra-low entry, the OP-177, to 11 models—there are no duals yet.

Precision (non-chopper-stabilized) low-offset-voltage and low-offset-voltage-drift op amps generally run off ±15-V supply rails with several exceptions *(Fig. 1)*. They have offset drifts of less than 3 μV/°C and offset voltages at 25°C below 300 μV. The best come in at 0.1 μV/°C and 10 μV. Note that all specifications for individual devices are guaranteed maximums or minimums unless noted as typical (t) in Table 2.

Op amps that operate with 10 V or less between their supply pins (half with 3 V or less) and need a quiescent current (I_Q) equal to or less than 300 μA. Some operate from as low as 3 V drawing 15 μA. There are even 1-V units drawing just 270 μA *(Fig. 2)*.

High-speed op amps will be covered in a second report early next year; however, some high-speed op amps are scattered over the charts *(for another look at IC op amps, see* ELECTRONIC DESIGN, *May 14, 1987, p. 39; Sept. 3, 1987, p. 81; and Feb. 4, 1988, p.127)*.

Today, process advancements are



1. PICK THE PRECISION **op amp you need from this chart (numbers refer to devices listed in Table 1). First, select the maximum offset drift you can stand along the horizontal axis, then go vertically into the chart until you reach the maximum initial offset voltage. Finally, pick up additional data about your selection in the Table 1.**

as important to the vitality of an analog IC supplier as published papers are to a professor. While much attention is given to the move toward JICB processes due to their speed, more designers will probably use op amps from one or more of the new silicon-gate CMOS processes.

Of the five companies marketing op amps built on these JICB processes (Analog Devices, AT&T, National Semiconductor, PMI, and TI), only TI has used the process to build low-power (230-μA I_Q) general-purpose devices. The op amps are members of the recently announced TLE2021/22/24 device family *(see opening figure and Tables 1 and 2, items 20 and 21)*. Moreover, their fast pnp input stage ensures single-supply operation (common-mode voltage can include the minus rail). They also appear to be the fastest single-supply op amps, and the fastest with a supply current below 500 μA.

Although a dual, single-supply op amp swinging 75 V across a 1000-Ω load is hardly general purpose, AT&T's LB1013AD comes close to the TI TLE2022 in many of its specifications. Operating with 85 V between its supply pins, the AT&T part will run off as little as 5 V; supply current runs a total of 1.1 mA (550 μA/op amp). The LB1031AD goes for $5.25 each in hundreds.

TLE20xx op amps can't touch the best precision op amps found in the lower left quadrant of figure 1. The BC grade with a guaranteed maximum offset voltage of 200 mV and a typical drift of 2 mV/+C certainly puts them in the precision class. Moreover, its offset voltage over temperature (including the military range) is a maximum of 300 mV. Consequently, your maximum expected error can be known even if the drift specification is given as typical. These specifications are for operation from one 5-V rail, which results in the low quiescent current. When operating from split 15-V supplies, I_Q increases by 70 mA—but maximum offset voltage drops in half. And, as might be expected, dynamic specifications improve: Open-loop gain improves by 10 dB.

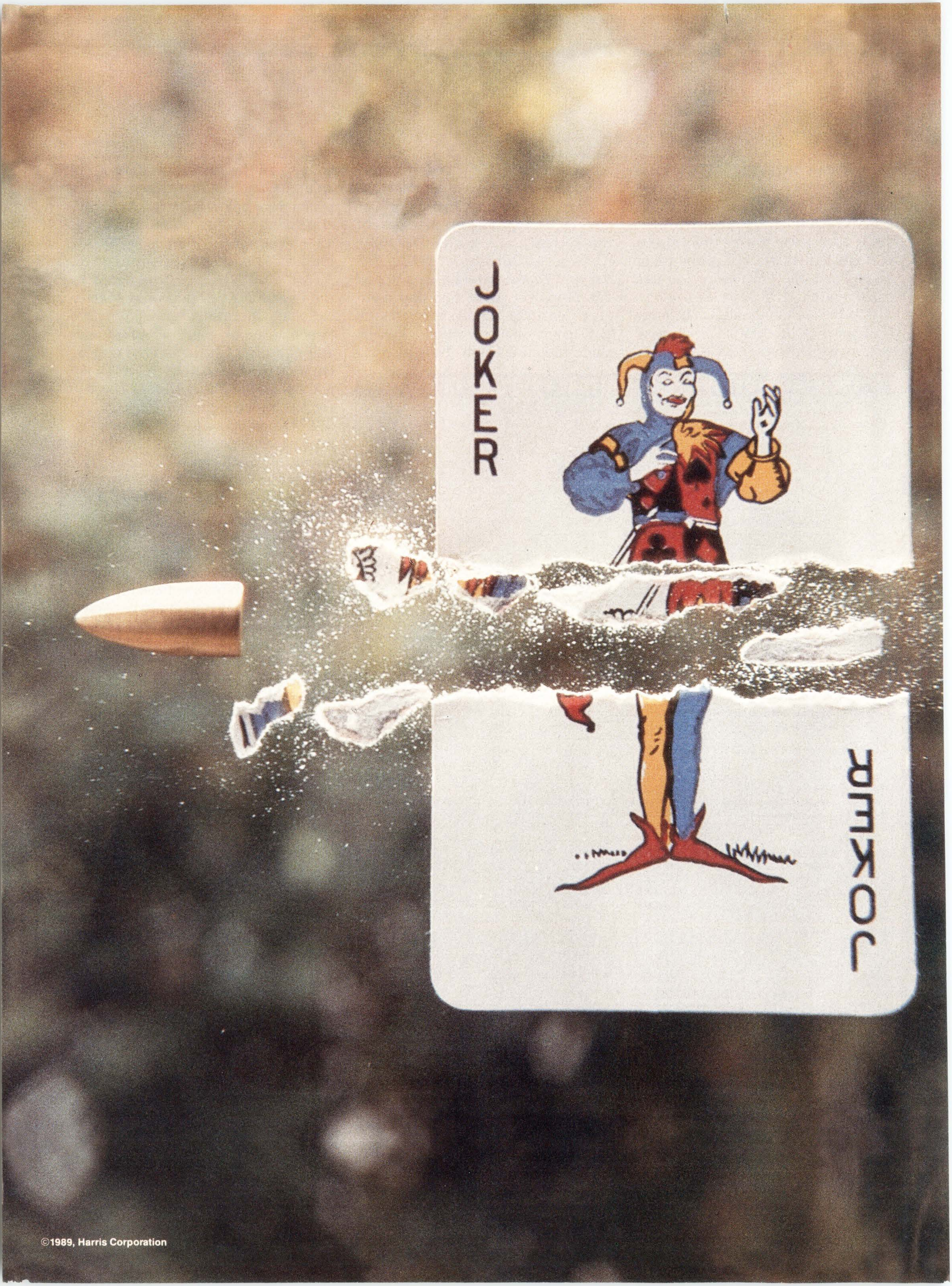
Interestingly, two more CB op amps make figure 1, Analog Devices' AD844D and AD846B *(Table 1, items 24 and 31)*. While employing a current-feedback design and aimed at speed, they still come in with an OP-07 class specification. Because the op amps current-feedback devices, their open-loop gain is expressed in megohms. Consequently they are not displayed for simplicity.

Other Strokes

Harris, which has DICB as its longtime trademark for its high-speed devices, recently entered the fray with a pair of precision devices, the single HA-5177 and the single/dual HA-5121/5122. The former has the lowest offset drift of the CB op amps, the latter is the fastest precision op amp that's not using current feedback *(Table 1, items 16a and*

TABLE 1: 15-V LOW-OFFSET-VOLTAGE PRECISION OP AMPS

No.	Company	Model	Unit price (100s)	Open-loop gain (dB)	Comments
1a	Precision Monolithics	OP-07A	$12.65	110	
1b	Precision Monolithics	OP-27E	$3.53	120	
1c	Burr-Brown	OPA27E	$6.80	120	
1d	Harris Semiconductor	HA-5127A	$6.75	120	
2a	Precision Monolithics	OP-07D	$1.20	101	
2b	National Semiconductor	LM607C	$0.93	123	
3a	Precision Monolithics	OP-27G	$1.54	117	
3b	National Semiconductor	LM627C	$1.13	132	
3c	Burr-Brown	OPA27G	$3.00	117	
4a	Precision Monolithics	OP-177E	$14.95	134	
4b	Raytheon Semiconductor	4077B	$14.21	134	
5a	Precision Monolithics	OP-177G	$1.00	126	
5b	Raytheon Semiconductor	RC4097F	$2.45	116	
6a	Precision Monolithics	OP-77E	$3.00	134	
6b	Precision Monolithics	OP-50E	$8.10	140	
6c	National Semiconductor	LM627A	$4.53	134	
6d	Linear Technology	LT1007AC	$5.00	137	
6e	Linear Technology	LT1012AC	$6.50	110	
6f	Raytheon Semiconductor	RC4097E	$3.65	120	
6g	National Semiconductor	LM607AC	$2.60	134	
7	Precision Monolithics	OP-77G	$1.25	126	
8a	Precision Monolithics	OP-50F	$6.00	138	I_0 = 50 mA
8b	Burr-Brown	OPA21E	$6.70	120	I_Q = 230 mA
8c	Burr-Brown	OPA627B	$15.80	110	I_B = 20 pA
9a	Linear Technology	LT1001AM	$3.40	113	
9b	Raytheon Semiconductor	LT1001AM	$27.00	113	
10a	Linear Technology	LT1001C	$1.35	112	I_B = 150 pA
10b	Linear Technology	LT1007C	$3.70	134	
10c	Raytheon Semiconductor	·LT1001C	$1.16	112	I_B = 150 pA
10	National Semiconductor	LM607BC	$1.20	126	
11	Linear Technology	LT1012C	$2.75	106	
12	Linear Technology	LT1028AC	$7.55	137	Low noise
13	Linear Technology	LT1028C	$4.95	134	
14	Analog Devices	AD707C	$16.00	138	
15a	Analog Devices	AD707J	$1.25	130	
15b	Raytheon Semiconductor	RC4077B	$14.21	120	
16a	Harris Semiconductor	HA-5177	$4.73	126	
16b	Raytheon Semiconductor	RC4077F	$1.37	126	
17a	Raytheon Semiconductor	RC4077E	$2.63	134	
17b	Maxim	MAX400E	$7.62	114	
18a	Raytheon Semiconductor	RC4097A	$21.00	120	
18b	Maxim	MAX400C	$6.00	114	
19	Burr-Brown	OPA111BM	$12.65	120	I_B = 1 pA
20	Texas Instruments	TLE2021AC	$2.56	110	
21	Texas Instruments	TLE2021C	$1.76	110	
22	Motorola Semiconductor	MC33078	$1.05	90	Dual
23	Motorola Semiconductor	MC33077	$1.91	104	Dual
24	Analog Devices	AD844B	$7.00	NA	Current feedback
25	Harris Semiconductor	HA-5221	$6.68	106	
26	Burr-Brown	OPA627A	$7.50	104	
27	Motorola Semiconductor	MC33272	NA	94	
28	Texas Instruments	TLC2201B	$7.49	104	I_B = 1 pA
29	Linear Technology	LT1077C	$1.65	NA	
30	Texas Instruments	TL031AC	$1.15	74	
31	Analog Devices	AD846B	$7.45	NA	Current feedback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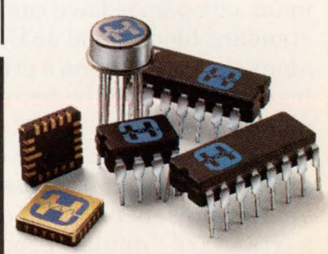
KEY FEATURE		HA-5221	HA-2410	HA-5177	HA-5134	HA-5170	HA-5147A
Max Offset Voltage	μV	700	200	25	100	300	25
Settling Time	μSec	1.5	2.0	14.0	13.0	1.0	0.4
Offset Drift	μV/°C	0.5	3.0	0.1	0.3	2.0	0.2
Gain	V/μV	2.5	5.0	30.0	3.0	0.6	1.8
Noise	nV/Hz	3.4	6.0	3.8	7.0	10.0	3.0
Slew Rate	V/μSec	20.0	8.0	0.8	7.0	8.0	35.0
Bandwidth	MHz	35.0	8.0	1.4	4.0	8.0	10
Supply Current	mA	8.0	4.0	1.2	6.5	1.9	3.0
Packages	LCC	•	•	•	•	•	
	Cerdip	•	•	•	•	•	•
	TO-99			•		•	

All specs typical.



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25). In most applications, V_{OS} TC or maximum V_{OS} over temperature is more important than initial V_{OS}—and that's where the HA-5177 shines.

Harris isn't alone with precision DICB op amps. Burr-Brown's upcoming OPA627B *(Fig. 1, center)* has a V_{OS} of 100 μV and a TC of 1 μV/°C *(Table 1, item 8c)*. It's also fast, and it includes JFETs on the input that give it a bias current of 20 pA, putting it in a class with Burr-Brown's OPA111 and the Harris HA-5180-5. Both of these are 1-pA-bias-current chips aimed at electrometer applications where femtoampere bias currents aren't needed. Comparable to virtually all Harris op amps, the HA-5180 employs their DICB process; however, the OPA111 is built on an earlier Burr-Brown process. While employing DI, the OPA111's pnps are laterals *(Table 1, item 19)*.

Elantec and Sipex are also building op amps on DICB processes, but both have limited their product lines to speedy devices. Furthermore, a JFET input device is expected from TI's complementary process in the near future. The TI chip will claim a mix of specifications for general-purpose JFET op amps that were previously unavailable.

Don't give up on the well-proven, standard bipolar processes yet. They dominate today's ultra-precision devices, such as the PMI OP-177E, with just 10 μV of V_{OS} and 0.1-μV/°C drift, *(Table 1, item 4)*. In addition, 20 other devices boast offsets equal to or below 50 μV with TCs at or below 1 μV/°C. Many of them are available as duals, and some can be found as quads. A quick look at both tables indicates that innovative designers at many companies have come up with standard bipolar and JFET-input op amps that compete on a price-performance basis with the newer complementary units.

Eight op amp families developed at Motorola over the past several years represent excellent designs on a standard bipolar process. The newer families also contain members that are excellent examples of what can be done with advanced trimming techniques. The newest also show one company's effort to slash product proliferation. As a reminder, both TI and National have bipolar and JFET-input op amp families containing devices with similar levels of performance.

"To Boldly Go..."

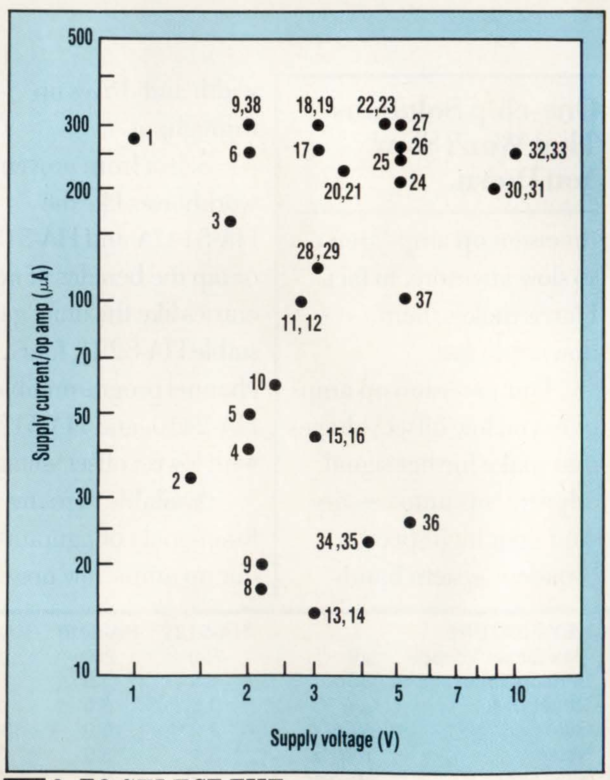
Op amps in Motorola's families range widely in performance—from low-power, single-supply all-bipolar devices to high-speed JFET-input units. All the bipolar-input devices run from one supply. The families have dual and quad versions; some also come as singles. The bipolar-input families include the single-version MC33171 units with low power of 250 μA, a 1.6-V/μs slew rate, and V_{OS} of 4.5 mV; and the MC33071 with an 8-V/μs slew rate and V_{OS} of 3 mV. Both feature a V_{OS} TC of 10 μV/°C. In dual bipolar-input families, there are the MC33078, MC33077, and MC33272 with slew rates of 5, 8, and 10 V/μs, and a V_{OS} of 2, 1, and 1 mV, respectively. All three families have a V_{OS} IC of 2 μV/°C.

In JFET-input, single-version families, there's the high-speed MC34081 family with slew rates up to 20 V/μs, I_B of 200 μA, V_{OS} of 0.5 mV, and V_{OS} TC of 10 μV/°C. Then there's the MC33181 family with a low bias current I_B of 100 μA, a 7-V/μs slew rate, V_{OS} of 2 mV, and V_{OS} TC of 10 μV/°C. Also included is the MC33282 JFET-input dual-input family with a 7-V/μs slew rate, V_{OS} of 2 mV, V_{OS} TC of 5 μV/°C, and I_B of 200 μA.

An all-npn output stage, common to these eight op amp families, gives them their speed-power product that's in a class with many CB devices. This technique dominates Motorola's op amps. Linear Technology (LTC) uses it in its LT1028 and PMI uses it in its OP-50, which features a V_{OS} of 25 μV, a V_{OS} TC of 0.3 μV/°C, and puts out 50 mA.

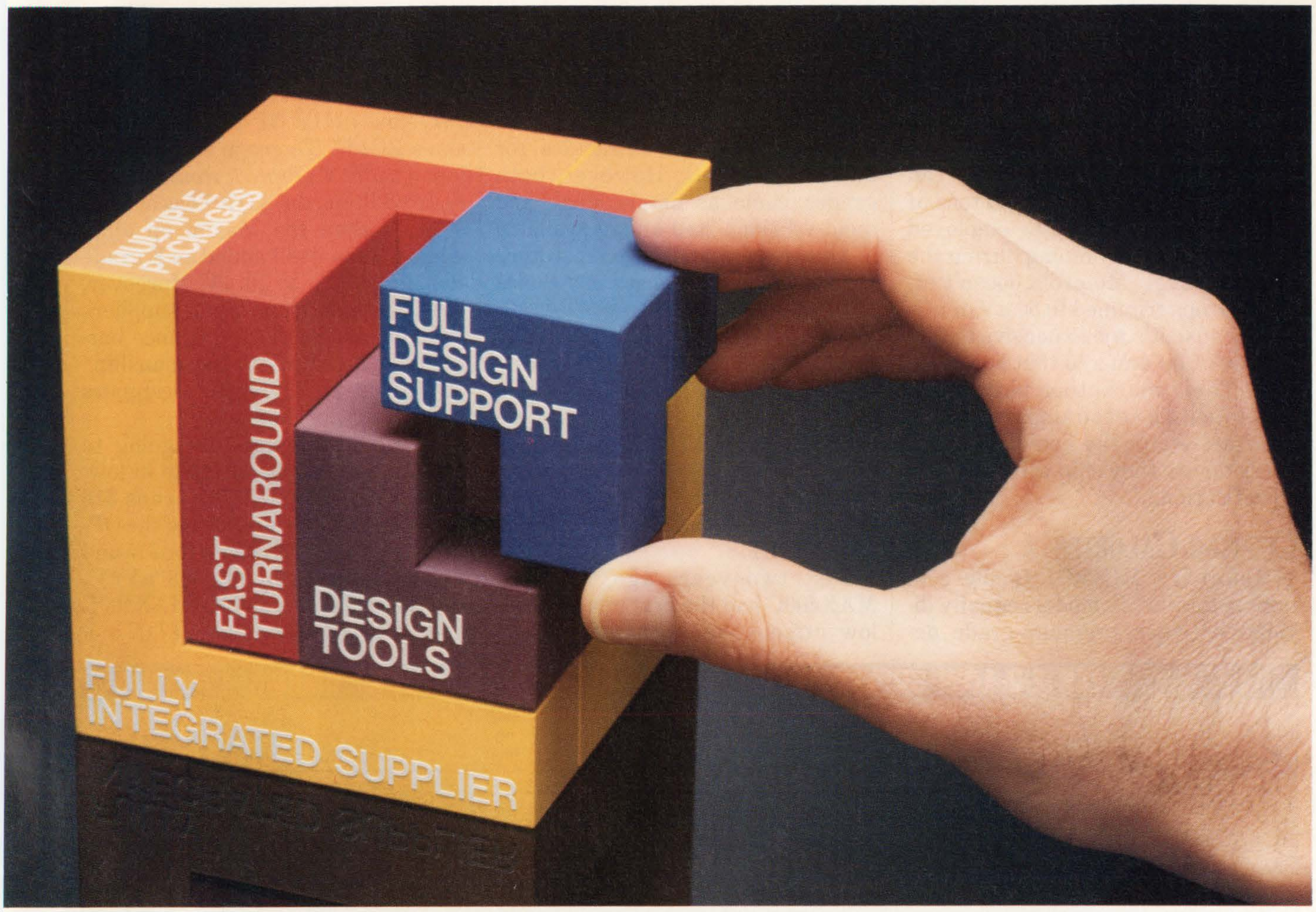
The secret behind any producible IC op amp with an offset voltage below a few millivolts is good control of the process and a superior production trimming technique. Analog Devices specializes in laser trimming thin-film resistors, while most of the others employ some variation of zener zapping—the blowing of on-chip zener diodes to cut fixed resistors in or out of the circuit. Both techniques must be used before packaging. However, stress induced during molding can cause permanent changes in offset voltage. Zapping can be done after packaging but it requires extra pins.

Motorola developed a technique that makes in-package trimming



2. TO SELECT THE low-supply-voltage or quiescent-current op amp, you need to first choose your maximum supply voltage from the horizontal axis (numbers refer to devices listed in Table 2). Then go vertically into the chart until you reach your maximum allowable supply current. Finally, get other data about your choice in Table 2.

The Analog ASIC Solution



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[1] SPICE developed by University of California

CIRCLE 9

possible by passing pulses of current through on-chip resistors via paths from signal pins to the power pins. Called "zipper-trimming" because the resistors look like zippers, it can rapidly trim offsets to within tens of microvolts. It can also be employed for prepackage trimming during the probing stage. Motorola doesn't offer op amps trimmed to 50 μV of offset because it's too expensive to test zillions of op amps to that specification. Their marketing philosophy says to sell a lot of op amps with 1 mV of offset—with the knowledge that every device they ship will meet that specification.

CUTTING CALORIES

Motorola's MC33071 family contains a total of 42 models equally divided between premium-grade devices with initial maximum offsets of 3 mV, and non-premium-grade units with maximum offsets of 5 mV. All other specifications are identical for all other models. However, both grades come as single, dual, and quad versions, and all are available in the three standard temperature ranges. Each also comes in a choice of three packages.

The more recent MC34081 family dropped to 26 models, again equally divided between premium and non-premium devices. Finally, if designers want an MC33077, they can have it any form as long as it's a dual version for the extended-industrial-temperature range and it's in an SO-8 or an 8-pin DIP.

Just two years ago, Maxim's MAX400C had the best mix of ultra-low offset-voltage and offset-drift devices, with a V_{OS} of 15 μV and a V_{OS} TC of 0.3 μV/°C *(Table 1, item 18)*. Now PMI's OP-177 and Raytheon's RC4077B come in at 10 μV and just 0.1 μV/°C *(Table 1, items 4a and b)*. In addition, the AD707 has a lower V_{OS} TC than the Maxim op amp, while Maxim itself added an E grade that drops V_{OS} to 10 μV. Moreover, other devices from other suppliers have encroached into this once barren field. Is this just "specsmanship" or is there a difference? Designers will have to decide.

To start, designers are going to have to pay for the ultimate in low-drift devices. The AD707C runs $16 each in quantities of 100, and the OP-177E and the RC4077B go for $15 and $14.21, respectively. At 0.3 μV/°C, the RC4097A, MAX400C, MAX400E and RC4077E cost $21, $6, $7.62 and

TABLE 2: LOW-SUPPLY-VOLTAGE LOW-QUIESCENT-CURRENT OP AMPS

No.	Company	Model	Single supply	Min. rail voltage (V)	Max, I_Q (mA)	Unit price (100s)	I_B (max)	V_{OS} (mV/C)
1	Genum	GC810	Y	1	270	$1.49	160 nA	2 (t)
2	Texas Instruments	TLC1078 (d)	Y	1.4	34	$2.31	0.6 pA (t)	1 (t)
3	Signetics	NE5230	Y	1.8	160	$1.00	60 nA	5
4	Advanced Linear Devices	ALD1706A	Y	2	40	$4.34	30 pA	7 (t)
5	Advanced Linear Devices	ALD1706G	Y	2	50	$1.89	50 pA	10 (t)
6	Advanced Linear Devices	ALD1701A	Y	2	250	$3.97	30 pA	7 (t)
7	Advanced Linear Devices	ALD1701G	Y	2	300	$1.55	50 pA	10 (t)
8	Linear Technology Corp.	LT1178AC (d)	Y	2.2	17	$5.15	8 nA	1.8
9	Linear Technology Corp.	LT1178C (d)	Y	2.2	20	$2.80	10 nA	2.5
10	Linear Technology Corp.	LT1077C	Y	2.3	60	$1.65	10 nA	0.4
11	Linear Technology Corp.	LT1006AC	Y	2.7	100 pA	$2.80	15 nA	1.3
12	Linear Technology Corp.	LT1006C	Y	2.7	100 pA	$1.60	25 nA	1.8
13	Precision Monolithics Inc.	OP-90E	Y	3	15	$6.50	15 nA	NA
14	Precision Monolithics Inc.	OP-90G	Y	3	15	$1.65	25 nA	NA
15	Texas Instruments	TLC27L7C	Y	3	42	$1.18	0.6 pA (t)	1.1 (t)
16	Texas Instruments	TLC27L2C	Y	3	42	$0.57	0.6 pA (t)	1.1 (t)
17	Motorola	MC331171	Y	3	250	$1.34	0.1 mA	10 (t)
18	Texas Instruments	TLC27M7C (d)	Y	3	280	$1.18	0.6 pA (t)	1.7 (t)
19	Texas Instruments	TLC27M2C (d)	Y	3	280	$0.57	0.6 pA (t)	1.7 (t)
20	Texas Instruments	TLE2021AC	Y	3.2	230	$2.56	50 nA	2 (t)
21	Texas Instruments	TLE2021C	Y	3.2	230	$1.76	50 nA	2 (t)
22	Precision Monolithics Inc.	OP-80E	Y	4.5	300	NA	250 fA	30 (t)
23	Precision Monolithics Inc.	OP-80G	Y	4.5	300	$1.95	2 pA	30 (t)
24	Burr-Brown	OPA21E	N	5	210	$6.70	40 nA	1
25	Precision Monolithics Inc.	OP-21E	N	5	230	$6.35	0.1 mA	1
26	Burr-Brown	OPA211G	N	5	250	$3.30	75 nA	5
27	Precision Monolithics Inc.	OP-21G	N	5	300	$1.88	0.15 mA	5
28	National	LPC662AI d	Y	3	120	NA	0.1 pA (t)	1.3 (t)
29	National	LPC662I d	Y	3	120	$0.90	0.1 pA (t)	1.3 (t)
30	Analog Device Inc.	AD548C	N	9	200	$4.95	10 pA	2
31	Analog Device Inc.	AD548J	N	9	200	$0.75	20 pA	20
32	Texas Instruments	TL031AC	N	10	250	$1.15	100 pA	25
33	Texas Instruments	TL031C	N	10	250	$0.48	100 pA	7 (t)
34	Texas Instruments	TLE2021BC	Y	4	230	$2.56	50 nA	2 (t)
35	Texas Instruments	TLE2021C	Y	4	230	$1.76	50 nA	2 (t)
36	Motorola	MC34181	N	5	250	$0.79	100 pA	10 (t)
37	Harris	CA5130A	Y	5	100	$1.39	10 pA	NA
38	Harris	CA3420A	Y	2	300 t	$2.81	0.02 pA	4

d = dual t = typical

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VTC
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$2.63 each, respectively.

Open-loop gains, mandatory for high-precision circuits running at high gain, range from 114 to 134 dB: The low value (114 dB) is sufficient for all but the most critical circuit; the $2.63 unit hits 126 dB. Early precision op amps had open-loop gains of about 100 dB, but the gain nonlinearity of many was poor. The result was nonlinear errors or distortion in wide-dynamic-range signals, particularly when driving low-impedance loads. Though unspecified, most current designs have eliminated the problem—both PMI and Analog Devices show typical gain nonlinearity plots (in any case, be cautious of precision op amps with open-loop gains much below 120 dB). Bias currents of all units are similar in the 1-to-2-nA region. Maximum voltage noise between 0.1 and 10 Hz runs 0.35 μVpk-pk for the AD707, and 0.6 μVpk-pk for the RC4077 and Maxim units.

There are a half-dozen others to consider when in the market for this breed of op amp: the PMI OP-77E, National's LM627A and LM607AC, Linear Technology's LT1007AC and LT1012AC, Raytheon's RC4097E, and PMI's OP-50E. All have offset TCs of 0.5 μV/°C and 25 μV of offset. Prices range from $3 to $6.50, except for the $8 OP-50E. The OP-50E can put out 50 mA and has open-loop gain of 140 dB, but it's only stable at closed-loop gains of five or above. In a 14-pin hermetic DIP, the fast OP-50E shuts down when the die reaches 165°C.

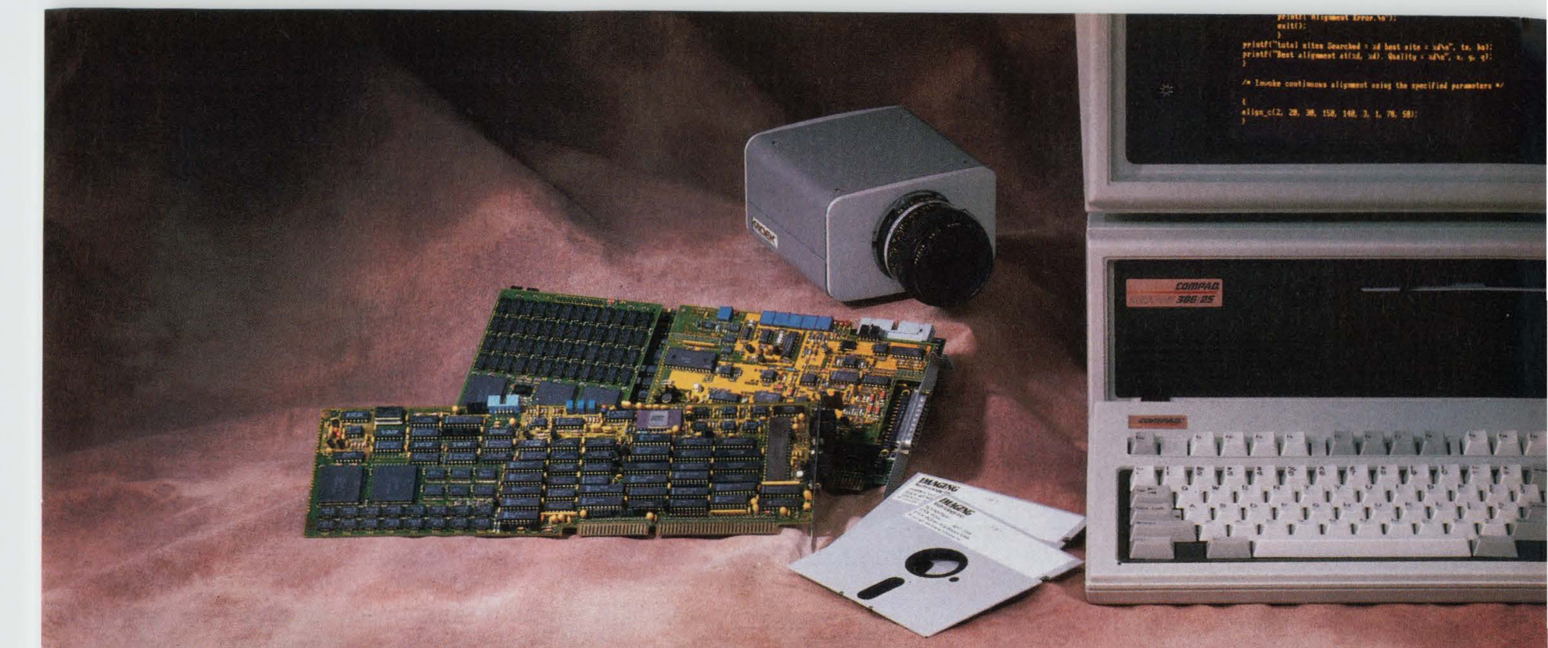
An anomaly lies in 0.5-μV/°C 200-μV—the TI TLC2201BC, which is located in a square *(Fig. 1 and Table 1, item 28)*. It's the only device on the figure that can't handle ±15-V rails. It's a CMOS op amp that outperforms many bipolars, albeit with an offset voltage that's specified as typical. And with a bias current of 1 pA (again typical), it beats out the JFETs, OPA111BM, and OPA627A *(items 19 and 8c)* and its drift is lower than the JFET OPA627B *(Table 1, item 26)*.

When looking at the voltage noise of the low-bias-current devices, it's important to consider the ultra-low drift units: They usually have impressive noise specifications. From 0.1 to 10 Hz, voltage noise of the OPA111, OPA627, and TLC2201BC runs 2.5, 2.5, and 0.5 μVpk-pk typical, respectively. Their respective spot noise at 10 Hz runs 60, 60, and 25 nV/$\sqrt{\text{Hz}}$. At 10 Hz, the voltage noise of LTC's LT1028 (the lowest voltage-noise IC op amp) is 1.7 nV/$\sqrt{\text{Hz}}$, and that of the AD707 is 13 nV/$\sqrt{\text{Hz}}$.

How did a TI designer take a process infamous for building noisy op amps (CMOS) and come up with a device that could challenge some of the best bipolars and beat out the lowest-noise JFETs? It took close work between circuit design, layout, and process engineering. In any process, low-noise input stages are obtained by using big transistors—in CMOS, they must be gargantuan. In fact, the input devices take up 45% of the die *(see opening figure)*. The largest block in the lower left corner forms two p-channel MOSFETs, and the two large blocks to their right form two n-channel MOSFETs.

The move to CMOS IC op amps, begun by TI in 1983, appears to be gaining momentum. The second-generation field now has six players: TI, National, Advanced Linear Devices, Maxim, and PMI—all of them with proprietary product lines—and SGS-Thomson, which second-sources the TI devices.

There are a myriad of driving forces behind the move to CMOS and various reasons for its apparent success. One reason is the advantages



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CIRCLE 11

CMOS offers: low cost, low power-supply voltage, high density, a good power-speed product, and inherent sub-picoampere bias currents that turn a CMOS op amp into a poor-man's electrometer op amp. Furthermore, CMOS op amps can operate from one supply and deliver a virtual rail-to-rail output swing. Finally, analog system designers are now ready to give up split ±15-V rails.

Essentially all of the CMOS op amps announced over the past few years can be classified as low-power, low-supply-voltage types. The lone exception is the previously described low-noise TLC2201, which needs 1.5 mA from the rails *(Table 2)*. With bias currents that peak at 50 pA and offset that drifts below 15 μV/°C, all of these CMOS op amps would make a low-bias-current list. While they can't take 30 V between their supply pins, they work well from ±5-V supplies—most only need about 3 V.

National's LPC662I, at just \$0.90, has a typical bias current of just 40 fA. It runs off 3 V and needs only 120 μA from one lithium cell *(Table 2, item 29)*. Bias current is typical because designers can't test for that kind of current in production and sell it for \$0.90.

Another interesting micropower op amp, the all-bipolar dual LT1178AC, is a true precision device with a V_{OS} of 70 μV and a V_{OS} TC of 1.8 μV/°C. It needs just 17 μA of supply current per op amp from a 2.2-V battery *(Table 2, item 9)*. As with all LTC single-supply op amps, its output swings to within a few millivolts of ground while sinking current, without the need for a pull-down resistor that draws power when sourcing current. The Advanced Linear Devices CMOS op amps and Signetics' bipolar NE5230 both offer a unique feature that's made possible by a complementary input stage: The common-mode voltage can include both supply rails *(Table 2, items 3 through 7)*.□

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83C751, 87C751

SYSTEM SPECIFICATION

Host
IBM PC/XT/AT, PS/2 or compatible.
Minimum 512K of RAM.
Monochrome, color or enhanced graphic display.

External Box
The emulator boards can be installed in an external box with serial communication to PC.

Languages supported
Third party assemblers, PL/M, Pascal and C compilers.

Source level debugging
Window for source level debugging. Single Step or Line Step with breakpoints marked directly in the code.

In-line Assembler and Disassembler
Full instruction set and symbols supported.

Symbolic Support
Full symbolic debugging and type checking. Same symbols can be used in different modules.

File formats Supported
Intel HEX/OBJ/OMF/SYM, Motorola S1, Avocet, Introl IAR, HMI SYM, AD2500, American Automation, Relms.

Real time Emulation
Full speed emulation (max 20 MHz EMUL 51, 3,3 MHz EMUL 68) No wait states and no intrusion on memory, stack, I/O or interrupt pins.

Emulation Memory
EMUL51: 64 K XDATA and 64 K CODE.
EMUL 68: 64 K

Memory Mapping
Mappable in 4 K pages.
Write protected areas supported in EMUL 68.

Macros
Test session automation and macro command definition. IF/ELSE, REPEAT/WHILE structures.

Debug Session Logging
Record emulation session and all setups to a file.

Breakpoints
64 K program breakpoints.
64 K data read and write breakpoints.

Break on external signal.
Break on direct access to internal bit or byte memory.
Conditional breakpoints.
Break on internal contents (not real time).

Single Stepping
Single or multiple instruction stepping. Line stepping in high level languages.

Execution timer
Resolution down to clock cycles.

Real Time Trace Memory (optional)
16 K deep by 48 bits wide.
Trace address, data, ports, control signals, time stamp and maximum of 18 external signals.

Trace Filter
20 qualifiers for filter tracing.
Post view filtering can record up to 15 frames after a match.

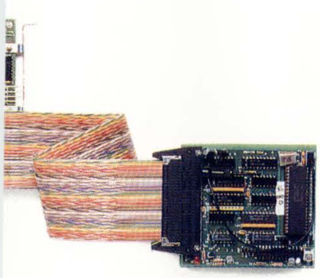
Trace Trigger
Two multiple trigger qualifiers with trigger on combinations of the qualifiers. Sequential and boolean combinations. Loop counter. Trigger can be modified without stopping emulation.

Trigger Breakpoint
The 48 bit trace trigger qualifiers can be used to define complex breakpoints also on program execution.

Trace Display
Display trace in disassembled symbolic or binary/hex form. Display can be saved to a file. Trace can be started, stopped and displayed independent of program execution.

Trace Time Stamp
Time stamp can be used to display execution time or time from last frame.

Program Performance Analyzer
Histogram and statistical information of program execution in real time.



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BUILD A WIDE-BUS TEST AND DEVELOPMENT SYSTEM

DESIGNERS FACE UNIQUE CONSTRAINTS WHEN USING OFF-THE-SHELF SCSI PROTOCOL CHIPS IN SCSI-2 SYSTEMS.

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MARK S. GORDON
Digital Finesse Inc., 355 W. Olive Ave., Suite 105, Sunnyvale, CA 94086; (408) 737-9156.

One of the key improvements in the proposed SCSI-2 standard is a wider data bus—16- and 32-bit capability in addition to the current SCSI standard's 8-bit data width. But the way that data is sent—over two cables that don't need synchronization—leads to potential problems in debugging new designs. One solution to these problems is a test-and-development system that displays bus phases, data-bus and control-line content, and timing information. With such a system, designers wouldn't need to decode ones and zeros to understand what's happening on the bus. Instead, they could concentrate on *why* a condition occurs rather than how to test for it.

Such SCSI test-and-development systems are usually based on protocol chips specifically designed to interface with the SCSI bus. These devices contain state machines that automatically handle all bus phases and the accompanying data transfers. The protocol chips currently available, however, were designed to conform with the SCSI-1 standard. To build a SCSI-2 test system with these devices, designers must add hardware and software that support the features embodied in SCSI 2.

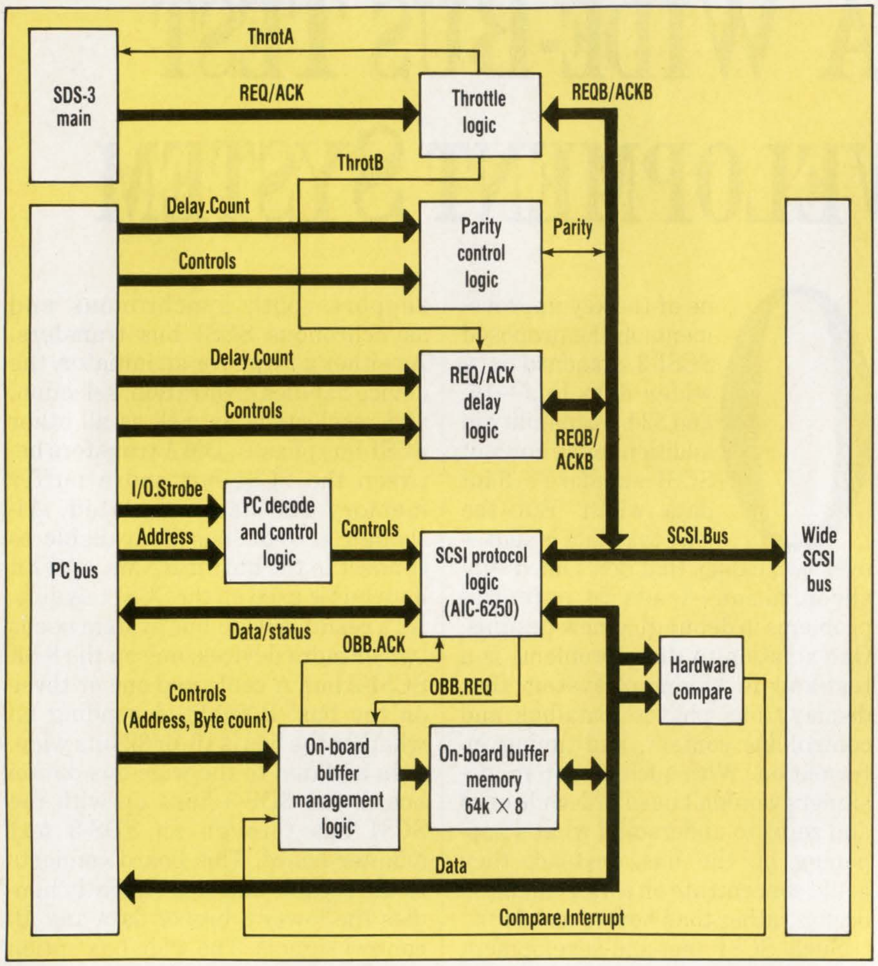
A board that adds wide-bus capability to the Adaptec SDS-3 SCSI test and development system illustrates some of the problems SCSI-2 system designers must face. The wide-bus option board, as it's called, employs the Adaptec AIC-6250 SCSI protocol chip. The system consists of cards that plug into an IBM PC/XT, AT, or compatible, and the software to control the cards.

The 6250, a high-performance SCSI interface protocol controller, supports both synchronous and asynchronous SCSI bus transfers. As either a target or an initiator, the device handles arbitration, selection, and reselection, as well as all other SCSI-bus phases. DMA transfers between the SCSI bus and a buffer memory are accommodated. Although a 16-bit bus is available to connect to the buffer RAMs, an 8-bit data bus is used on the SCSI bus side. As a result, a wide-bus system needs two or more devices, one on the 8-bit SCSI-2 bus A cable and one or three on the bus' B cable, depending on whether the bus is 16- or 32-bits wide.

In addition to the wide-bus option board, the SDS-3 links up with the SCSI bus through an SDS-3 test adapter board. This board connects to the A cable and consequently handles the lower 8 bits of data and all control signals. The wide-bus option board connects to the B cable and to the test adapter board. The design example that's discussed has a 16-bit bus, so only one 6250 is needed on each board. The example also exclusively covers the wide-bus option board design.

ON-BOARD MEMORY

Besides the AIC-6250, the wide-bus option board holds an on-board data buffer (OBB memory), which stores up to 64 kbytes of data coming from or going to the SCSI bus *(Fig. 1).* Fast DMA logic (OBB management logic) automatically performs the handshake on the OBB memory bus. This circuitry also ensures that the OBB on the wide-bus option board and the OBB on the test adapter board are synchronized so that they can transfer the correct number of bytes and locate these bytes in the buffer properly. The address and control signals from the PC bus transmit to the OBB through the



1. THOUGH THE AIC-6250 SCSI protocol chip was designed to conform to the original SCSI specification, designers can use the device in systems for the proposed SCSI-2 standard, such as this SDS-3 wide-bus option board.

OBB management logic.

The hardware compare block contains circuitry that compares data at high speeds. This capability makes possible on-the-fly comparisons of data that's written to a device on the SCSI bus. It works by comparing what's stored in the OBB with data that's read back from the bus (which is only compared, not stored). This feature is particularly useful when large volumes of data are transferred, making visual comparison inefficient.

The parity control logic makes controlled parity generation possible. If enabled, it generates parity for writes to the SCSI bus and checks parity on reads from the bus. With this parity logic, users can also force a parity error after from 1 to 256 byte transfers.

Because it resides on the PC bus, the board also has PC decode and control logic, which is contained in a PAL16R4, a register-type programmable logic array *(Fig. 2)*. Proper synchronization is ensured by clocking the array with the same 20-MHz on-board oscillator that the 6250 uses. The PAL translates PC bus address and control lines $\overline{IOW}$, $\overline{IOR}$, and AD_4, and address decoder output $\overline{BDSEL}$ to the $\overline{WR}$, $\overline{RD}$, ALE, and CS control lines required by the 6250.

The board has 32 (decimal) addresses: 16 for the 6250's internal registers and 16 for other logic. AD_4 chooses between the two sets, and the $\overline{BDSEL}$ line supplies access to any of the 32 locations.

Two three-state buffers, $TSBUF_1$ and $TSBUF_2$, isolate the address bus lines from the multiplexed address/data bus lines, PD_{7-0}, of the 6250. Three more three-state buffers ($TSBUF_3$, $TSINV_1$, and $TSINV_2$) connect the $\overline{\text{SCSI.I/O}}$, $\overline{\text{Pseudo.C/D}}$, and $\overline{\text{Pseudo.BSY}}$ lines to the device.

ADAPTING TO SCSI-2

The $\overline{\text{Pseudo.C/D}}$ and $\overline{\text{Pseudo.BSY}}$ signals are needed because the 6250 is a SCSI-1 type device working in a SCSI-2 wide-bus system. This is because the 6250 is designed to handle all of the SCSI bus phases, expecting to see them occur in a particular order. Because all control signals are transmitted on the A cable, the 6250 on the adapter board monitors and handles the phases that these signals specify.

On the other hand, the 6250 on the wide-bus option board handles only B cable data transactions, so it doesn't see BSY, SEL, or any of the phase lines carried on the A cable. The $\overline{\text{Pseudo.BSY}}$ and $\overline{\text{Pseudo.C/D}}$ signals make the 6250 on the wide-bus option board believe that those SCSI-bus phases preceding the data phase are complete.

As a result, the 6250 on the B cable can arbitrate, select (or reselect), watch for a response to its selection (or reselection), and detect phases other than the data phase (a command, status, or message phase) so it can properly proceed to and from the SCSI data phase. Control software that's part of the SDS-3 manages the Pseudo.BSY and Pseudo.C/D signals.

It must be remembered that the BSY, SEL, and phase control lines (C/D, I/O, and MSG) of the 6250 on the wide-bus option board aren't actually connected and this device doesn't control or respond to bus phases. The 6250 on the SDS-3 test adapter board handles bus phases.

A look at the arbitration and selection/reselection phases shows how the process works. Acting as an initiator, the 6250 on the wide-bus option board believes it's commencing arbitration when bit 6 in its interrupt mask register 0 is set to 1. The initiator raises SEL (if arbitration is won), drops BSY, and waits for the target to respond to being selected by raising BSY.

The SDS-3 control software responds when the SCSI SEL signal appears by polling SCSI signal register 09 on the 6250—this determines when BSY is dropped. It then raises the Pseudo.BSY signal at the appropriate time. This particular action fools the 6250 into believing that a SCSI target responded.

No Handshake Needed

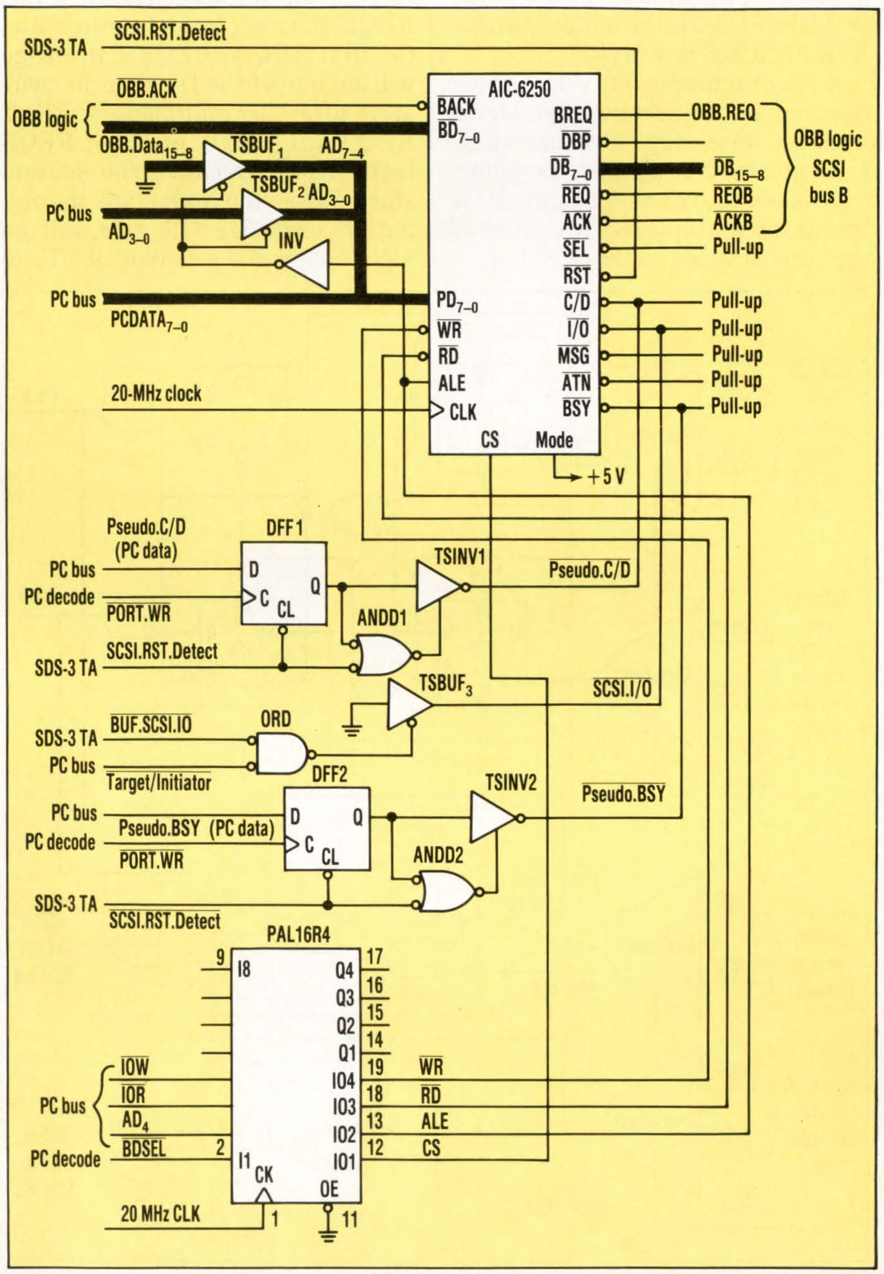
The control software then asserts the Pseudo.C/D signal to simulate a change to command phase by a target. The 6250 matches this new phase, which is reflected in the SCSI C/D bit (bit 7 of the device's SCSI signal register 09). Next, the control software drops Pseudo.C/D , forcing a change in value of the SCSI C/D bit. Note that a handshake isn't needed for the 6250 to proceed to the SCSI data phase.

Similarly, when the board acts as a target, the control software watches for SEL being raised and BSY being dropped, then asserts and deasserts the Pseudo.BSY signal. This action makes the 6250 believe that it successfully completed the arbitration and reselection phases and gained control of the SCSI bus by asserting BSY. As a target, the 6250 can be switched to the command phase by writing SCSI signal register 09, bit 7. Data phase is entered when this bit is deasserted. This series of actions places the device in the data phase so that it can transfer data properly. The SCSI control signals are different for a target and an initiator, so the Target/Initiator signal is required to differentiate between the two roles.

The SCSI.I/O signal (a buffered version of the SCSI bus I/O signal) forces the 6250 to see the data phase direction (in or out) on the SCSI bus. The SCSI.RST.Detect signal resets the 6250 and then deasserts the Pseudo.BSY and Pseudo.C/D signals when a reset occurs on the SCSI bus.

As noted, the proposed SCSI-2 standard doesn't supply synchronized data transfers on the A and B cables. In the case of a 16-bit data bus, even bytes (0, 2, 4, and so on) pass along the A cable, and odd bytes (1, 3, 5, and so on) along the B cable. If the cables are of different lengths, which is permitted by the proposed standard, skewed transfers can occur. For instance, bytes 0, 2, and 4 may pass along the A cable before the transfer of byte 1 is completed on the B cable.

A buffer, however, must hold the bytes in their proper order (0, 1, 2, and so forth), even though that may differ from the order of receipt if transfers on one cable operate faster than those on the other. Consequently, unsynchronized cables can make it difficult to debug firmware that, for example, moves data into a disk buffer on reads. If the system enforces the synchronization of the two cables—a process called throttling—designers can turn the synchronization on and off to determine if skewed transfers cause improperly ordered buffers.



2. A PROGRAMMABLE LOGIC ARRAY, the PAL16R4, translates PC bus address and control lines into the control signals required by the SCSI protocol chip.

Fortunately, SCSI 2 includes separate REQ and ACK lines on each cable to accommodate possible different cable lengths. Therefore, it's conceptually easy to throttle transfers on either the A or B cable so that they're within one byte of each other.

To enforce synchronization, a throttle logic circuit generates two signals, ThrotA and ThrotB, that delay the appropriate $\overline{\mathrm{REQ}}$ or $\overline{\mathrm{ACK}}$ signal *(Fig. 3)*. If the SDS-3 is the target, either $\overline{\mathrm{REQ}}$ or $\overline{\mathrm{REQB}}$ is delayed, depending on which cable leads the other. If the SDS-3 is the initiator, either $\overline{\mathrm{ACK}}$ or $\overline{\mathrm{ACKB}}$ is delayed.

A set of multiplexers select either the request or acknowledge signal lines as necessary. Because these are negative true signals, the falling edge is the active one. The signals entering the multiplexers are inverted versions of those on the SCSI bus.

Four D flip-flops then determine which line (A or B) leads the other by more than one active edge. The Throttle signals pass through AND-OR logic that delays assertion on the SCSI bus of the appropriate handshake signal from the 6250 until it's less than one active edge ahead of its counterpart.

Throttling Action

For example, assume that the SDS-3 is the target and is therefore responsible for asserting REQ and REQB. Starting from the reset state, the first REQ or REQB active edge will set one of the flip-flops immediately after the multiplexers: FF_1 if REQ leads REQB, or FF_2 if REQB leads REQ. Because the system started from the reset state, the output of exclusive OR gate will go high, causing the output of FF_3 to also go high. This output, combined with the enclusive OR gate's output, activates the ThrotA signal.

ThrotA, in turn, is an input to the AND-OR circuit that throttles the A cable. Working as a latch, this circuit waits until the current handshake transaction is completed, which occurs when $\overline{\mathrm{REQ}}$ in the example goes high or inactive. This high signal combines with the high ThrotA to drive DelayA high, preventing $\overline{\mathrm{REQ}}$ from being asserted at the OR gate's output.

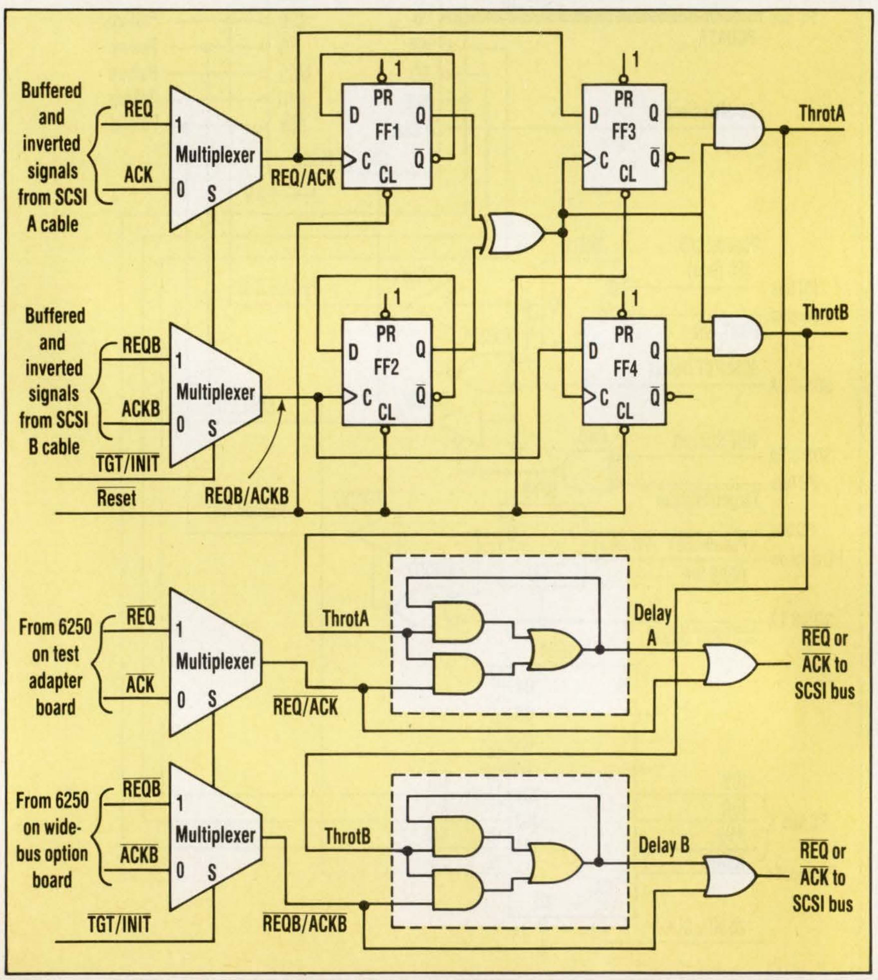
Because DelayA is fed back into the AND-OR network, the circuit is latched until ThrotA goes low, regardless of the state of $\overline{\mathrm{REQ}}$. And ThrotA can't go low or inactive until an active edge occurs on the REQB line. The result is the desired throttling: $\overline{\mathrm{REQ}}$ can't have two active edges without an intervening active $\overline{\mathrm{REQB}}$ edge.

When the next $\overline{\mathrm{REQB}}$ edge does occur, it triggers flip-flop FF_2. The exclusive OR gate's output then goes low and negates ThrotA. With ThrotA negated, another $\overline{\mathrm{REQ}}$ edge can be gated onto the SCSI bus, making it possible for another data transfer on the A cable.

A similar series of events occurs if the $\overline{\mathrm{REQB}}$ signal attempts to precede the $\overline{\mathrm{REQ}}$ signal by more than one active edge. In that case, the ThrotB signal is activated and the B cable transfer throttled. The same situation applies if the SDS-3 is the initiator. The only difference between these situations is that the $\overline{\mathrm{ACK}}$ or $\overline{\mathrm{ACKB}}$ signal is throttled.

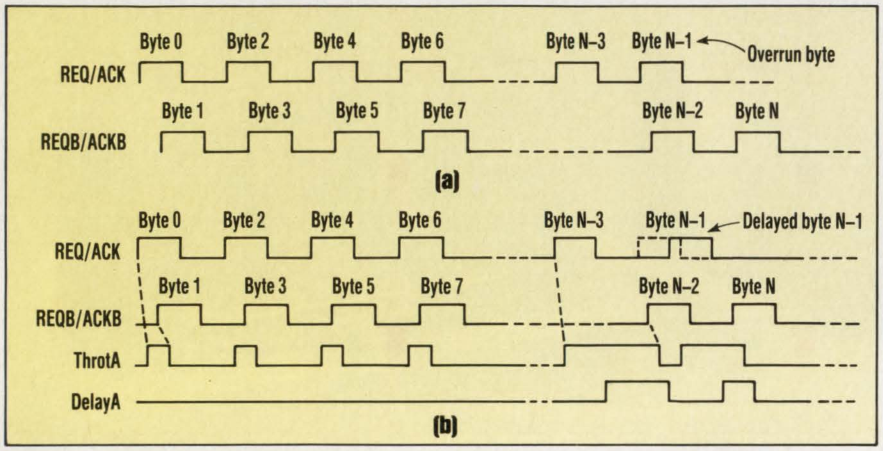
By blocking another REQ active edge generation, this technique prevents more data transfers from occurring. As a result, the REQ/ACK handshaking ensures that transfers occur in lock step. This method is used only with asynchronous SCSI transfers.

The affect of throttling is easily seen on a set of typical REQ/ACK signal timing diagrams. With the throttling circuit disabled, byte N–1 is an "overrun byte," which means that its transfer begins before the transfer of byte N–2 begins *(Fig. 4a)*. Debugging this situation can be difficult.



3. BY ADDING THROTTLING LOGIC on the wide-bus board, designers can synchronize A and B cable operation for easier debugging of SCSI 2 designs.

With the throttling circuit working, the active edges of the REQ/ACK and REQB/ACKB signals control the state of ThrotA. The ThrotA and DelayA signals delay the byte N–1 transfer *(Fig. 4b)*. ThrotA goes high when the REQ/ACK signal associated with byte N–3 goes high. DelayA goes high when REQ/ACK goes in active. The DelayA signal prevents the REQ/ACK signal, gated onto the SCSI bus by the OR gate in the throttling circuit, from going active until the next active edge of REQB/ACKB arrives. That next active edge of REQB/ACKB causes ThrotA to go low, which forces DelayA low.□

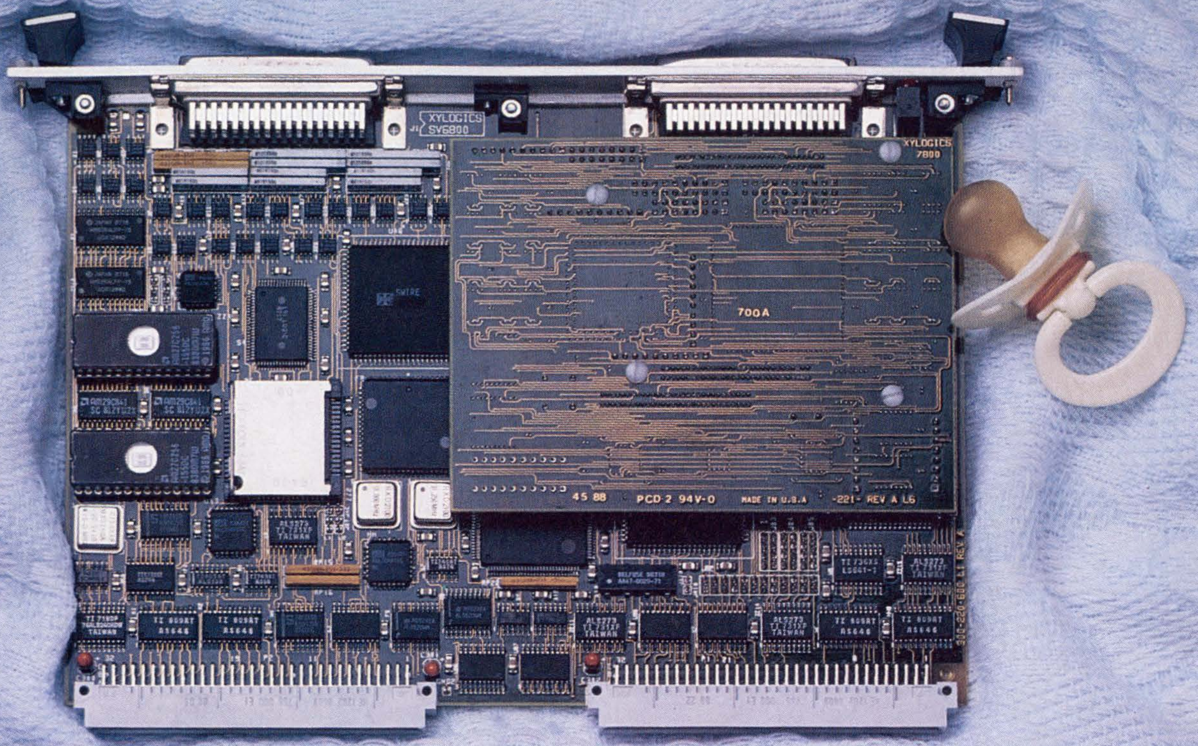


4. WITH THE THROTTLING FEATURE OFF, the transfer of byte N-1 may begin before the transfer of N-2 (a). Enabling the throttling circuit makes it possible for the REQ/ACK lines to control the Throttle and Delay signals in a way that delays the transmission of N-1 until N-2 begins transmitting (b).

Michael Nguyen, an engineer in the Development System Operations group at Adaptec, previously developed hardware at Link Flight Simulation.

Mark S. Gordon, founder and president of Digital Finesse, a consulting-management company, designed ICs at Zilog and helped found Verticom Inc.

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546



Develop And Verify Circuits In Two Weeks With CAD On A PC/AT.

CAD Shortens Design Cycle For RLL2,7 Coder

The total development effort, from design to working unit, for a fairly complex VLSI device can take just several weeks with schematic-capture and simulation tools, plus automatic-placement-and-routing software. A semicustom design, however, could take up to eight months, and a full custom design may consume years. An illustration of a computer-aided design-to-device cycle is the development of an RLL2,7-coding circuit for an optical-disk-interface encoder/decoder intended for high-density storage.

Less than two weeks of design effort went into developing and verifying the coding circuit on an IBM PC/AT. The schematic-design tools from OrCad Systems Corp. (OrCad/SDT III), together with Advanced Micro Devices' supported logic-cell-array (LCA) libraries, supplied the design software. Similarly, OrCad's verification and simulation tools (OrCad/VST) and the AMD PGA simulator-interface library offered unit-delay and full timing-delay simulation *(see "Logic cell arrays")*.

After partitioning the design with the software's auto-logic reduction and partitioning program (XNF2LCA) and routing with automatic-placement-and-routing (APR) software (AmPGA23), the circuit was temporarily hardwired in an Am3020 logic-cell-array (LCA) device for final checking. XACT editor software was also used to manually route some of the wiring nets that couldn't be APR routed.

The LCA device's primary advantage is fast turn-around design time—an advantage also extendible to other applications where time-to-market is critical. The RLL2,7-coding circuit was subsequently programmed into a larger Am3020 LCA device for full hardware verification. Finally, it was transferred into a still larger AM3090 as part of the entire optical-disk encoder/decoder system.

The encoding circuit in the LCA converts serially clocked nonreturn-to-zero (NRZ) digital data—the data format used inside most computers—into an RLL2,7 data stream for write operations to the disk. During data-read operations, the circuit converts the RLL2,7 coded data back to NRZ data. In addition to coding and decoding, the circuit checks for code-length violations of the

CHRISTOPHER JAY AND THY-HIEN LE
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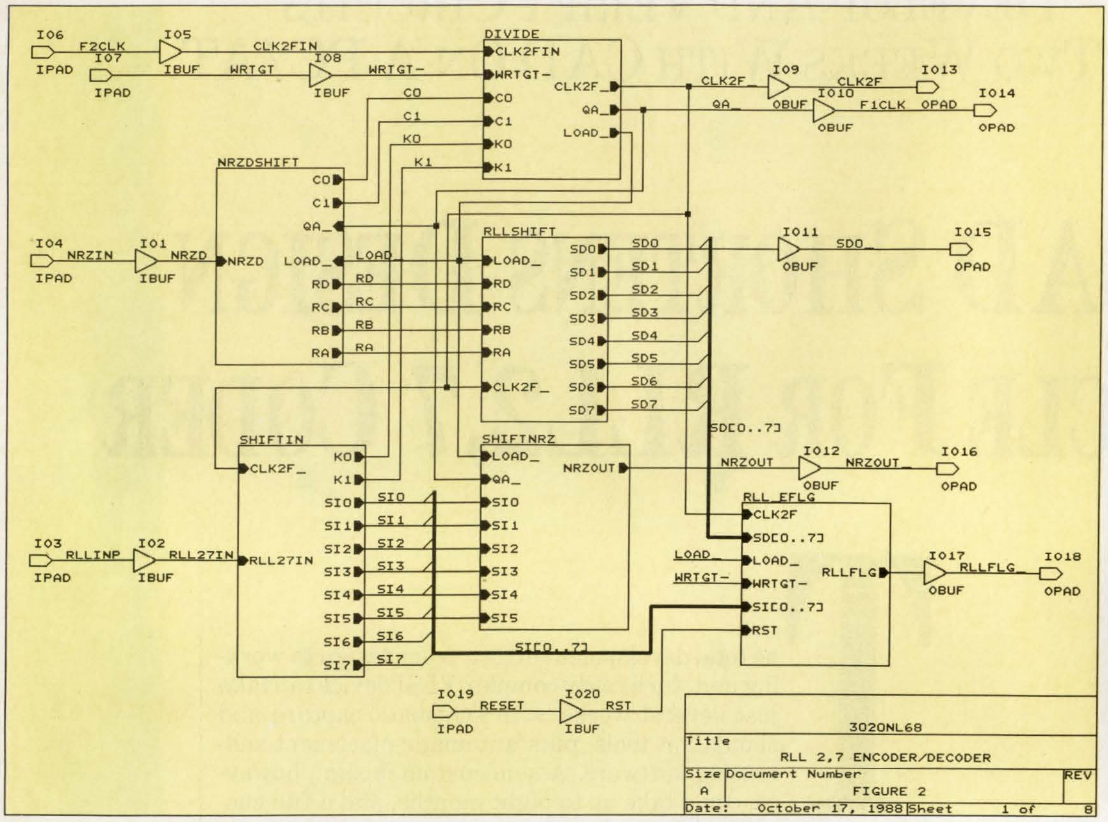
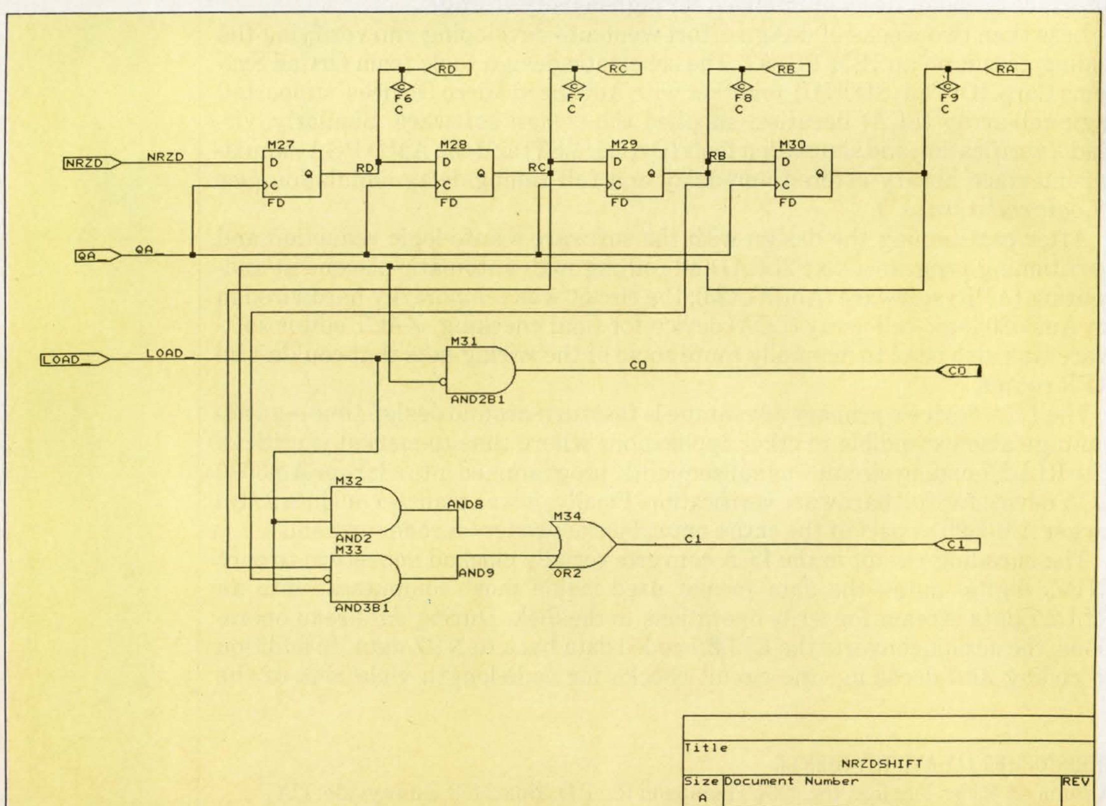
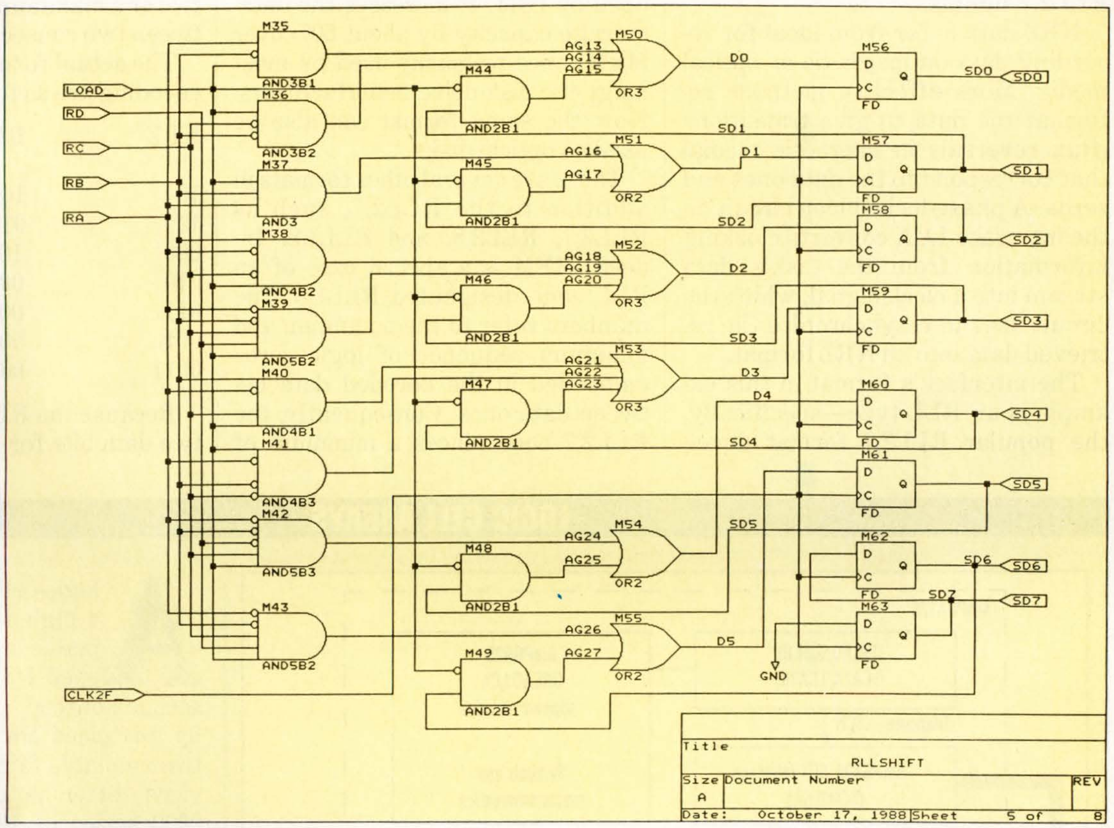


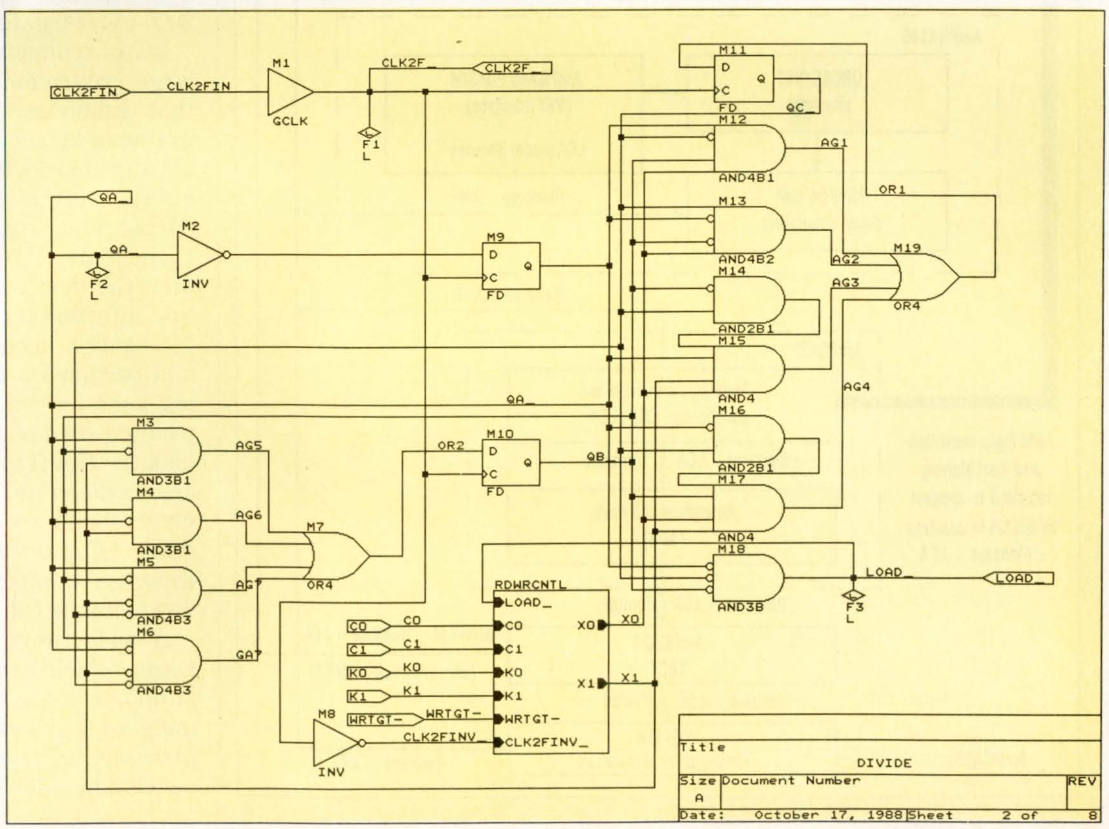
1. CREATED with OrCad/SDT III on a PC/AT, the overall block diagram of the RLL2,7 encoder/decoder is a hierarchical design. Each of its six blocks fit on separate sheets at a lower hierarchical level.



2. THE 4-BIT shift register in the NRZDSHIFT circuit receives serial NRZ data from the host computer.



3. THE RA through RD signals feed into the RLLSHIFT circuit.



4. RLLSHIFT register loading takes place at a zero count of the counter in the Divide circuit.

CAD FOR RLL2,7

RLL2,7 signals.

NRZ data is far from ideal for recording data on magnetic or optical media. More effective methods reformat the data to give transitions (flux reversals in magnetic media) that correspond to the data ones and zeros. A phase-locked loop circuit on the interface LCA converts clocking information from the disk's data stream into a clock signal, which the circuit uses to resynchronize the retrieved data into an NRZ format.

The interface's format in this example is an RLL type—specifically, the popular RLL2,7 format developed by IBM. It increases the data-storage capacity by about 50% over MFM, once primarily used by most magnetic disk-drive manufacturers. Now the same format can also be used on optical disks.

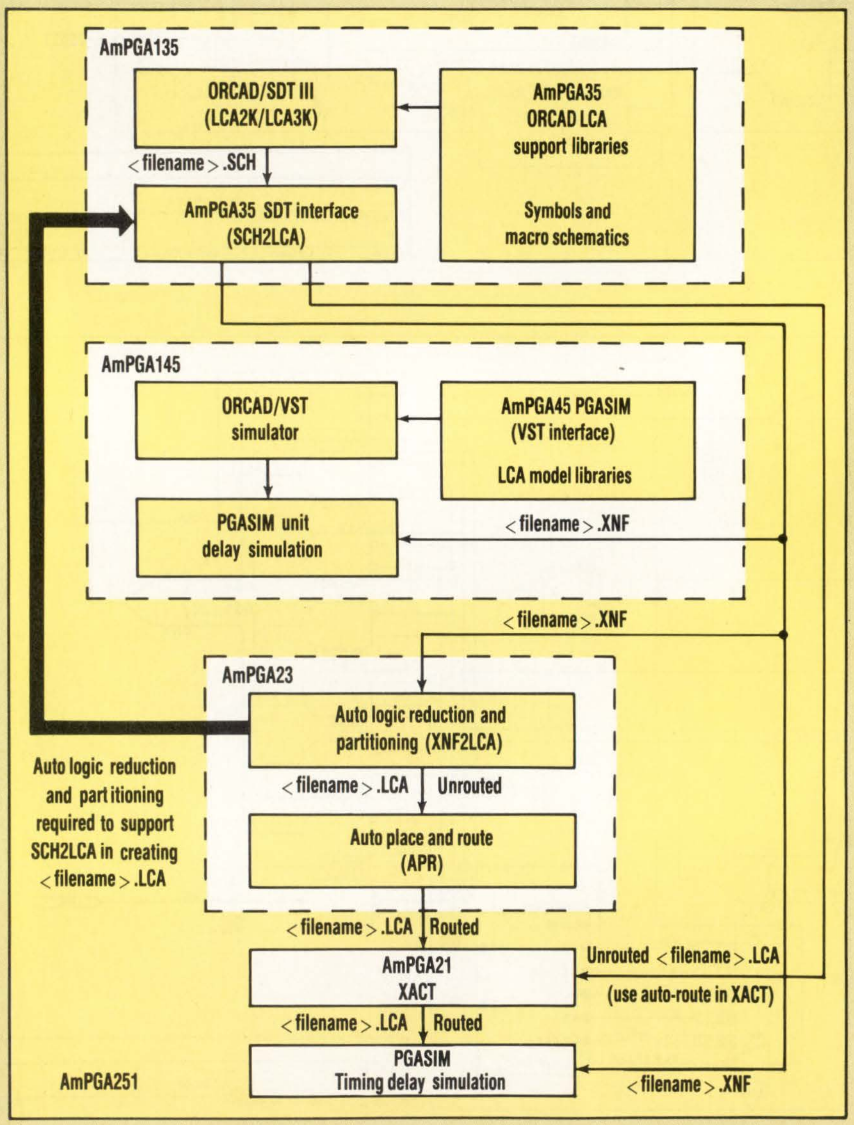
There are several other formats in addition to the RLL2,7, such as RLL2,7, RLL2,8, and RLL1,8. Indeed, MFM is a special case of an RLL code designated RLL1,3. The numbers refer to the maximum and minimum sequence of logic zeros embedded in the encoded data between data ones. Consequently, the RLL2,7 code places a minimum of two or a maximum of seven zeros between two consecutive ones.

The actual formatting rules of the encoding are as follows:

NRZ	RLL	Shifts
10	1000	4
11	0100	4
000	100100	6
010	001000	6
011	000100	6
0010	00001000	8
0011	00100100	8

Because the RLL2,7 code supplies two data bits for each NRZ data bit,

LOGIC CELL ARRAYS



A logic-cell array (LCA) is a high-density programmable logic circuit developed by Xilinx Inc. and second-sourced by Advanced Micro Devices. The two available families of LCA devices differ in complexity—the 2000 series of 1200-to-1800 gate equivalency and the recently introduced 3000 series that offers 2000-to-9000 gate complexity.

LCA architecture is based on a large programmable RAM array that subdivides into three programmable sections: configurable logic blocks (CLBs), programmable input/output blocks (IOBs), and programmable interconnections. Upon power application, the device reads configuration information from a nonvolatile source, such as an EPROM, and becomes a functional working logic unit in 17 to 80 ms, depending on device type and complexity. Configuration data can also come serially from a microprocessor, a serial EPROM, another LCA device, or a PC/AT through a specially designed downloading cable.

A wide range of design software, which runs on a PC/AT, supports logic array programming so that designers can complete and fully test a design in the development lab *(see the figure)*.

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CIRCLE 4

shift registers for RLL2,7 data must have twice the clock rate of NRZ data. Accordingly, the encoder/decoder circuit needs two synchronous clock signals: CLCKF2 and QA.

The overall block diagram of the RLL2,7 encoder/decoder in the AM3020 LCA, created with OrCad/SDT III on an IBM PC/AT, is a hierarchical design *(Fig. 1)*. Each of its six blocks fit on separate sheets at a lower hierarchical level. OrCad offers two design-entry methods: flat file and hierarchical. Unless the design can fit on one sheet, the software doesn't support the flat-file structure.

For easy identification, the sheets have the following labels: NRZDSHIFT, RLLSHIFT, SHIFTIN, RDWRCNTL, RLL_EFLG, SHIFTNRZ, and DIVIDE. The 4-bit shift register in the NRZDSHIFT circuit receives serial NRZ data (NRZIN) from the host computer *(Fig. 2)*. Shift-register outputs RA, RB, RC, and RD (where RA is from the last register in the 4-bit chain) drive a sum-of-products decoder circuit, which generates condition signals C0 and C1. The RA through RD signals also feed into the RLLSHIFT circuit *(Fig. 3)*.

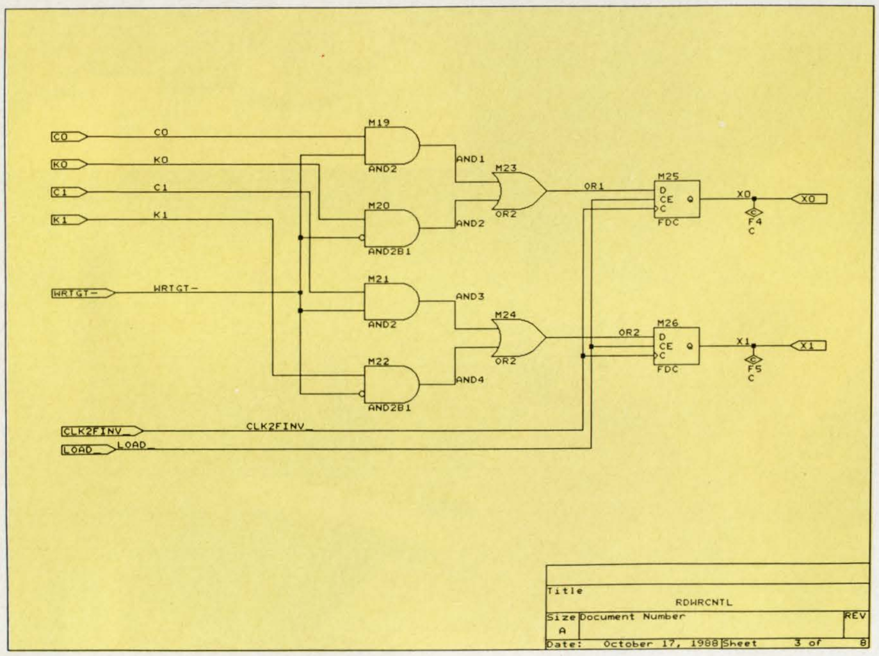
Then, within the RLLSHIFT circuit, the signals drive the six register inputs of the 8-bit shift-register chain—SD0 through SD7. Loading the RLLSHIFT registers takes place at a zero count of the counter in the DIVIDE circuit *(Fig. 4)*.

The C0 and C1 condition signals load into a 2-bit register in the DIVIDE circuit's RDWRCNTL section and control its counter *(Fig. 5)*. Depending on the state of C0 and C1, the counter counts through one of the following three sequences: 0 to 3, 0 to 5, or 0 to 7. In this method, the Divide circuit generates the four, six, or eight shift cycles consistent with the code combinations in the encoding-rule table.

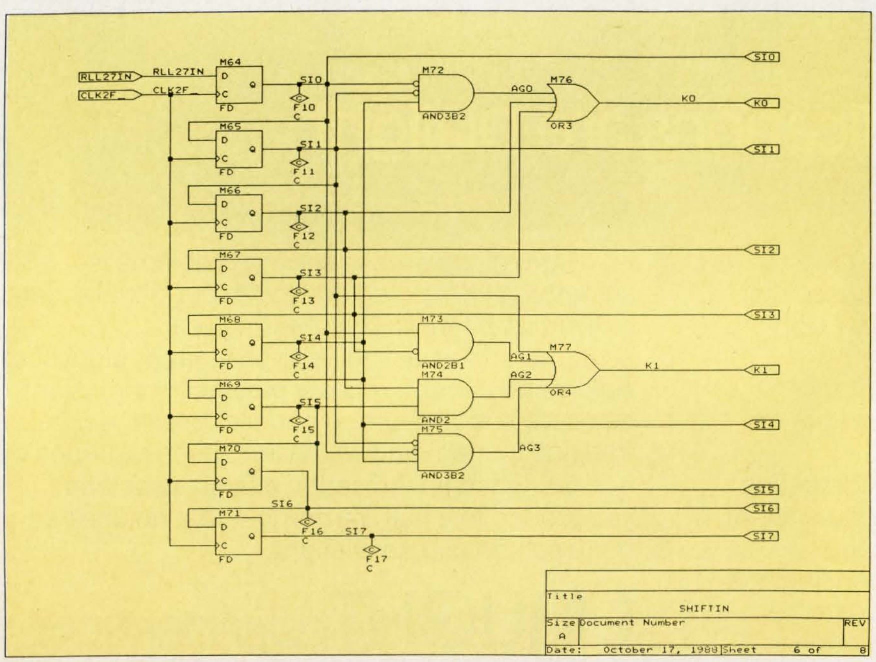
For example, if the data was 0011 from RA, RB, RC, and RD of the NRZDSHIFT register, then the Divide circuit would deliver a count of 0 through 7 to clock out the RLL2,7 data stream 00100100.

Accordingly, the RLL2,7 output bits must occur at twice the rate of NRZ input bits. The clock frequency (F2CLK) for shifting the RLL data is twice the clock frequency (QA) for shifting the NRZ data into the NRZDSHIFT register.

With the signal on the $\overline{\text{WRTGT}}$ line enabled, condition signals C0 and C1 pass through to lines OR1 and OR2 into flip-flop inputs that load when the $\overline{\text{LOAD}}$ signal is active—that is, when the Divide circuit counter contains a count of zero. The CLK2FINV clock signal strobes the condition signals into these flip-flops. When the counter's contents



5. THE C0 AND C1 condition signals load into a 2-bit register in the Divide circuit's RDWRCNTL section and control its counter.



6. THE SHIFTIN CIRCUIT generates the K0 and K1 control signals.

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CIRCLE 5

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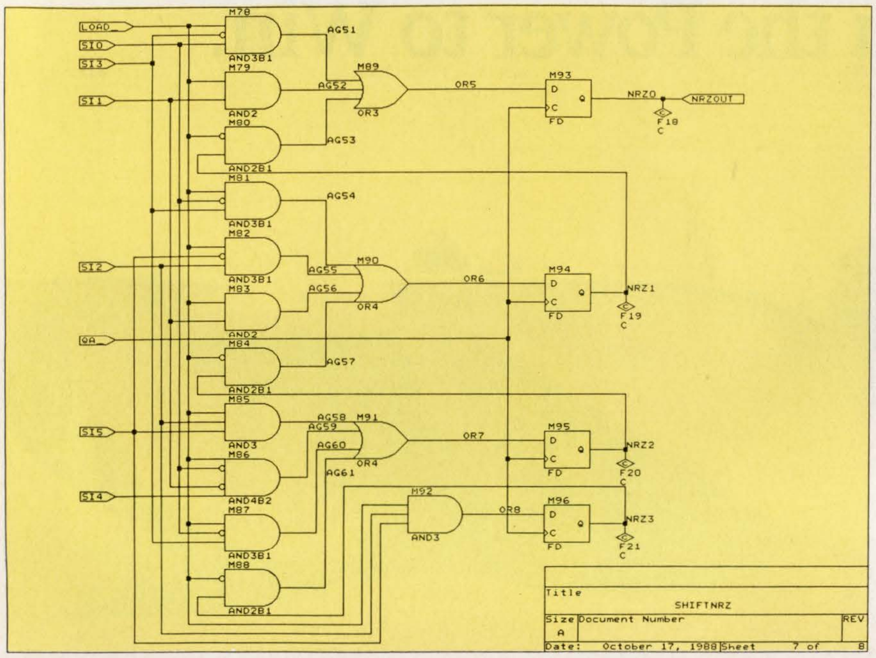


7. WITH AN ACTIVE $\overline{\text{LOAD}}$ signal, the SHIFTNRZ register's sum-of-products circuit decodes the RLL2,7 data signal to generate registered outputs NRZ0–3.

reach a count of three, the condition signals cause the counter either to reset, count to five and reset, or count to seven and reset. The same counter serves both read and write operations and the $\overline{\text{WRTGT}}$ input selects either the C0 and C1 pair of signals or the K0 and K1 pair. The SHIFTIN circuit generates the K0 and K1 control signals *(Fig. 6)*.

The decoding philosophy for the SHIFTIN's register's contents—using combinatorial logic and loading up a second register file with 4 bits of NRZ data—is the same for both the decoder and encoder. Consequently, the SHIFTIN circuit also decodes the RLL2,7 data output from the disk. The CLK2F signal clocks the encoded RLL27IN data into the first register of an 8-bit shift register. As in the NRZDSHIFT circuit, a sum-of-products circuit decodes the shift register's contents to supply the condition signals K0 and K1. The first six registers in the shift-register chain generate the sum-of-products. Just as the C0 and C1 signals control the count sequence in the write operations, K0 and K1 control the counter's behavior during a read.

The total set of conditions for selecting the three counting sequences are as follows:

To shift out RLL2,7 data:

$\overline{\text{WRTGT}}$	C0	C1	K0	K1	Count
H	L	H	X	X	0–3
H	H	L	X	X	0–5
H	H	H	X	X	0–7

To shift in NRZ data:

L	X	X	L	H	0–3
L	X	X	H	L	0–5
L	X	X	H	H	0–7

(Note: An input code of C0 = C1 = K0 = K1 = 0 gives a count of 0 to 3, but it's a redundant code in the design.)

With an active $\overline{\text{LOAD}}$ signal, the SHIFTIN register's sum-of-products circuit decodes the RLL2,7 data signal to generate registered outputs NRZ0, NRZ1, NRZ2, and NRZ3 *(Fig. 7)*. When $\overline{\text{LOAD}}$ is inactive, the NRZ data shifts through the register file at a rate synchronized to $\overline{\text{QA}}$, half the CLK2FIN rate. Furthermore, the condition-code registers decode the same count sequence 0 to 3, 0 to 5, and 0 to 7, depending on the contents of the data shifted into the RLL input register. The same counter can encode and decode because read and write operations are mutually exclusive.

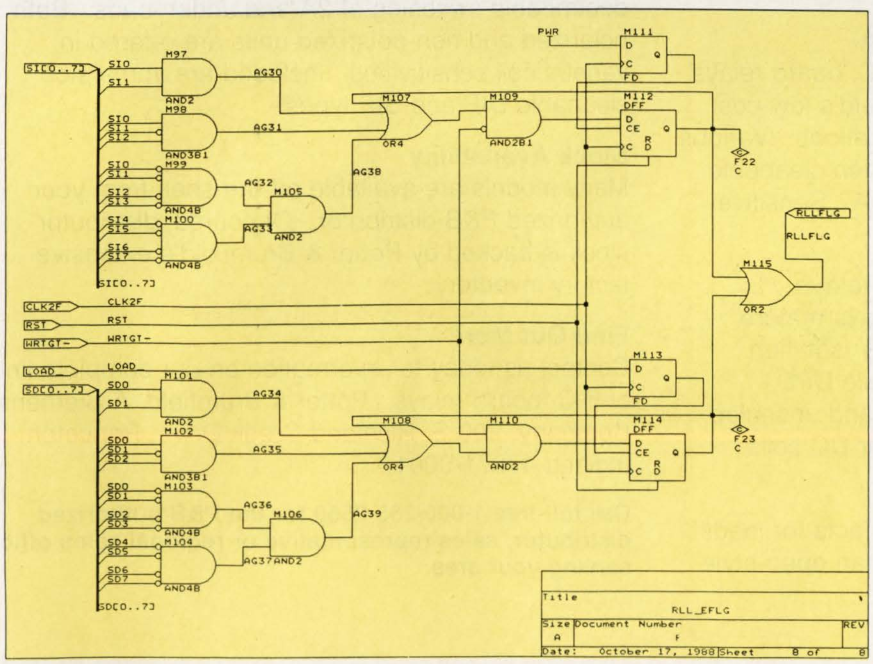
After decoding, the SHIFTIN circuit passes the data to the host system as either a 4-bit, 6-bit, or 8-bit data stream. For a 4-bit count, registered outputs NRZ0 and NRZ1 load with the decoded data and shift through the register file to the NRZOUT output. For a 6-bit count, NRZ0, NRZ1, and NRZ2 load and shift to the output, and for an 8-bit count NRZ0, NRZ1, NRZ2, and NRZ3 load and shift.

Moreover, the RLL_EFLG circuit detects corrupted RLL2,7 data *(Fig. 8)*. A $\overline{\text{WRITEGT}}$ command sets up the RLL_EFLG circuit in accordance with the condition code that controls the counter's behavior for writing or reading operations. When low, the $\overline{\text{WRITEGT}}$ signal selects the NRZ-to-RLL2,7 encoder condition-control signals C0 and C1; when high, the RLL2,7-to-NRZ condition-control signals K0 and K1 are selected. Only the specific cases of one zero, no zeros, or more than seven zeros between two consecutive logic ones in the data stream set registers and supply an error flag (RLLFLG) until cleared by the host system.

The OrCad/VST is a menu-driven simulator with a stimulus editor that makes it possible to initialize signals, and generate pulse signals and repetitive clocks cycles to drive a design's inputs in a PC/AT environment. An input signal can be added, deleted, or edited from the stimulus file. VCC and GND signals in this file represent high and low signal inputs, respectively. The trace editor controls the display of signal waveforms.

By invoking PGASIM (a program written by AMD), an external net list or LCA file can be translated into the OrCad verification and simulation tool's (OrCad/VST) net list and delay back-annotation files to run the simulation. The PGASIM menu offers either a unit-delay or timing-delay simulation. To check the design's logic functioning exclusively requires unit-delay simulation, which needs just the external net list file as an input source. Timing simulation, however, requires the routed timing parameters available from the LCA

CAD FOR RLL2,7



8. THE RLL_EFLG CIRCUIT detects corrupted RLL2,7 data and supplies an error flag (RLLFLG) until cleared by the host system.

file. It can be done at the configurable logic-block level, which needs only the support of the routed-LCA file, or at the gate level, which requires both the routed-LCA file and the unrouted external net-list file.☐

Christopher Jay is currently applications manager at Waferscale Integration. Prior to joining WSI, he worked at AMD as application manager for the LCA products. He holds a BSEE from the University of Essex.

Thy-Hien Le, a senior applications engineer working in AMD's Programmable Gate Array Division, has a BSEE from Santa Clara University.

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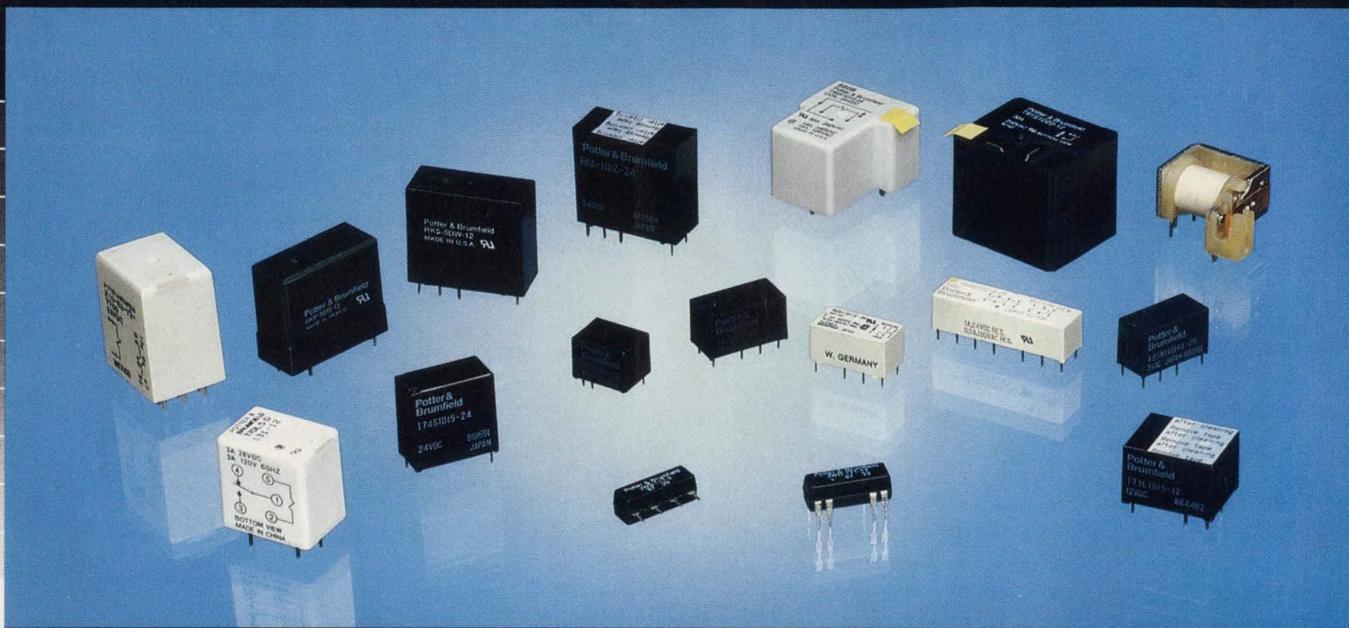

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A POPULAR EMBEDDED CONTROL PROCESSOR PRESENTS NEW OPPORTUNITIES FOR PERSONAL COMPUTER COMPATIBILITY.

BRING PC COMPATIBILITY TO THE INTEL 80C186

Many equipment manufacturers are considering moving the PC architecture from desktop to traditional embedded processor applications. There's a wide range of potential uses: consumer electronic devices, point-of-sale terminals, vending machines, industrial controllers. The architecture can also be used in such diverse areas as medical instrumentation, telecommunication systems, and electronic testing and measuring *(see "PC architecture for embedded systems")*.

However, the 80186 (or 80C186), the most popular embedded 16-bit processor, isn't fully PC compatible. Until now, designers were forced to use either the less powerful 8080/8086 processor or the more complex, costly 80286 (or even the 80386). With the new VG-501/502 chip set, the popular embedded-system processor can now take full advantage of the PC's architecture with true PC compatibility. Simultaneously, the chip set supplies a substantially reduced component count and lower power consumption than the 80286/386 microprocessors, and also better performance than the 8088/8086 microprocessors.

The 80186 includes many peripheral components found in the PC, such as a direct-memory-access (DMA) controller, programmable-interrupt controller, programmable timers, clock generator, bus controller, and wait-state generator. Nevertheless, although the CPU is fully PC compatible, the architecture of the peripherals on the 80186 chip is different *(Table 1)*.

PC architecture requires four DMA channels as supplied by the 8237 DMA controller. The 80186 only offers two, and they aren't 8237 compatible. The 8237 also uses a 16-bit address register and a 16-bit counter register for each channel. The 80186 has the same 16-bit counter register but uses 20-bit source and destination registers for

TABLE 1. 80186 vs. PC ARCHITECTURE

Feature	80186	PC
DMA	Two channels proprietary	Four channels (8237)
Timers	Two proprietary timers	Three timers (8253)
Interrupts	Single-level internal vector	Eight-level (8259A) external vector
Bus Cntrl	None	8288
Refresh	Internal (C186 only)	DMA channel 0

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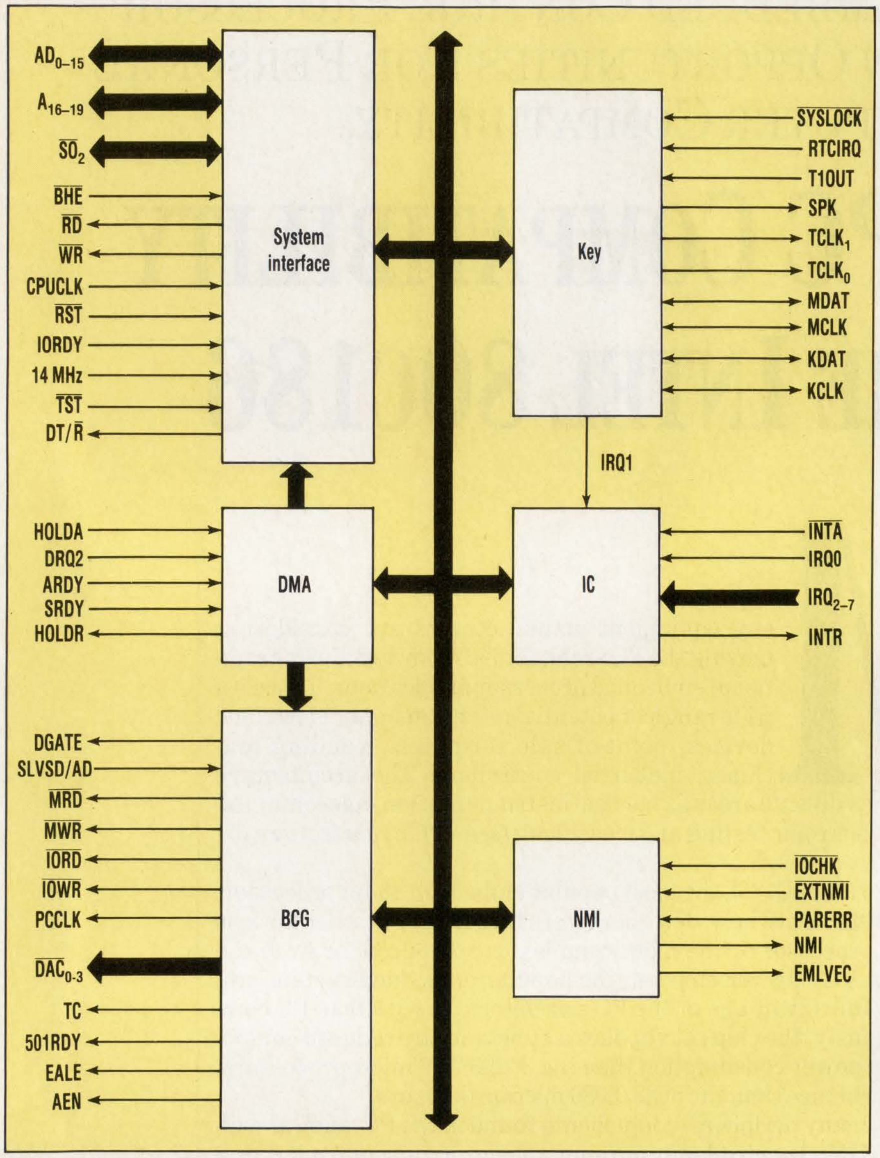
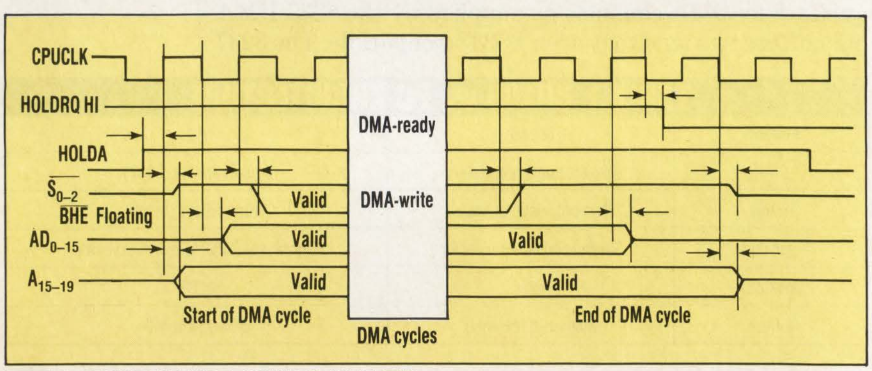


1. THE NEW VG-501/502 chip set lets the popular 80C186 take full advantage of the PC's architecture with true PC compatibility. The VG-501 chip acts as an external eight channel interrupt controller that is functionally compatible with the Intel 8259A.



2. WHEN THE CONTROLLER in the VG-501 is ready to do a DMA transfer, it issues a Hold-Request signal. Once the 80186 releases the bus and returns a Hold-Acknowledge signal, the VG-501 becomes a bus master and can perform the DMA activity.

DMA. In addition, the 8237 generates TC and DACK signals when DMA is complete; the 80186 doesn't.

Also, where the PC uses the eight-level 8259 priority-interrupt-controller chip, the interrupt controller integrated in the 80186 offers little more than one 8086 type of interrupt facility in the mode of operation closest to the PC. Consequently, for the 80186, the full capability of the 8259 must be externally duplicated. Furthermore, the two timers on the 80186 set up in different ways than the three timers on the 8253 timer chip used for the PC. A third timer must be added externally.

A Compatible 80186

Two critical elements bring PC compatibility to the 80186. The first element is extra hardware that supplements the on-board 80186 peripherals to match the configuration of the PC. Secondly, there's intercepting (trapping) and converting (if necessary) the way PC application software and hardware access peripheral components. If the PC application software is well behaved and performs all peripheral accesses through the BIOS, a special PC-compatible BIOS for the 80186 is all that is required to access the hardware with appropriate commands. But problems arise when ill behaved programs bypass the BIOS and go directly to the hardware to access the peripherals.

The PC software makers are notorious for supplying programs that wring every possible bit of performance from PCs by directly interfacing the hardware. Nevertheless, some early PC suppliers tried to supplement the 80186 hardware and use a special PC BIOS to hide the hardware differences. The few PC products released to the market that used this approach with the 80186 failed.

Fortunately, the PC architecture makes it possible to define a precise list of all possible incompatible peripheral accesses. Because the PC accesses peripherals with I/O addresses, hardware can be used to intercept the critical I/O addresses for correction *(Table 2)*. Accordingly, a hardware-based trapping mechanism in the VG-501/502 chip set saves the state of the machine in a FIFO register. It also delivers a nonmaskable interrupt (NMI) signal to the 80186 processor. Upon receiving this signal, the processor executes a short interrupt-service routine, which interrogates the FIFO register to determine the type of CPU cycle that was in progress.

Upon identifying the cycle type, the NMI-interrupt routine passes control to specific customized routines in the 80186's special BIOS. The special BIOS procedures extracts the parameters of the operation in progress. The BIOS then executes a functionally equivalent operation for the trapped command in a manner acceptable to the 80186/501/502 configuration. Afterwards, control returns to the application program. Using the NMI to trap doesn't affect the normal PC use of NMI for parity-error reporting.

Though this sequence may seem complex and slow, few instructions are needed to trap and execute an equivalent operation. Moreover, the chip-set hardware reduces the required software. Less than 1% of the overhead is used when the code is executed to correct peripheral setup. A typical operation takes less than 40 μs. Furthermore, because most PC applications employ relatively few peripheral accesses, overall performance degradation is barely noticeable.

TABLE 2. CRITICAL I/O ADDRESS FOR PERIPHERAL ACCESSES

Peripheral	I/O Address
Interrupt	20
Interrupt	21
DMA	00-0F
DMA Page	80-83
Timer	40-43
Model 30 RTC	B0-BF, E0-EF

Given the ability to detect and correct all accesses to the peripherals either through the BIOS or directly to the hardware, the next step is adding the necessary supplemental hardware to configure 80186 systems as a PC. This hardware is divided into three areas: interrupt control, DMA control, and timers.

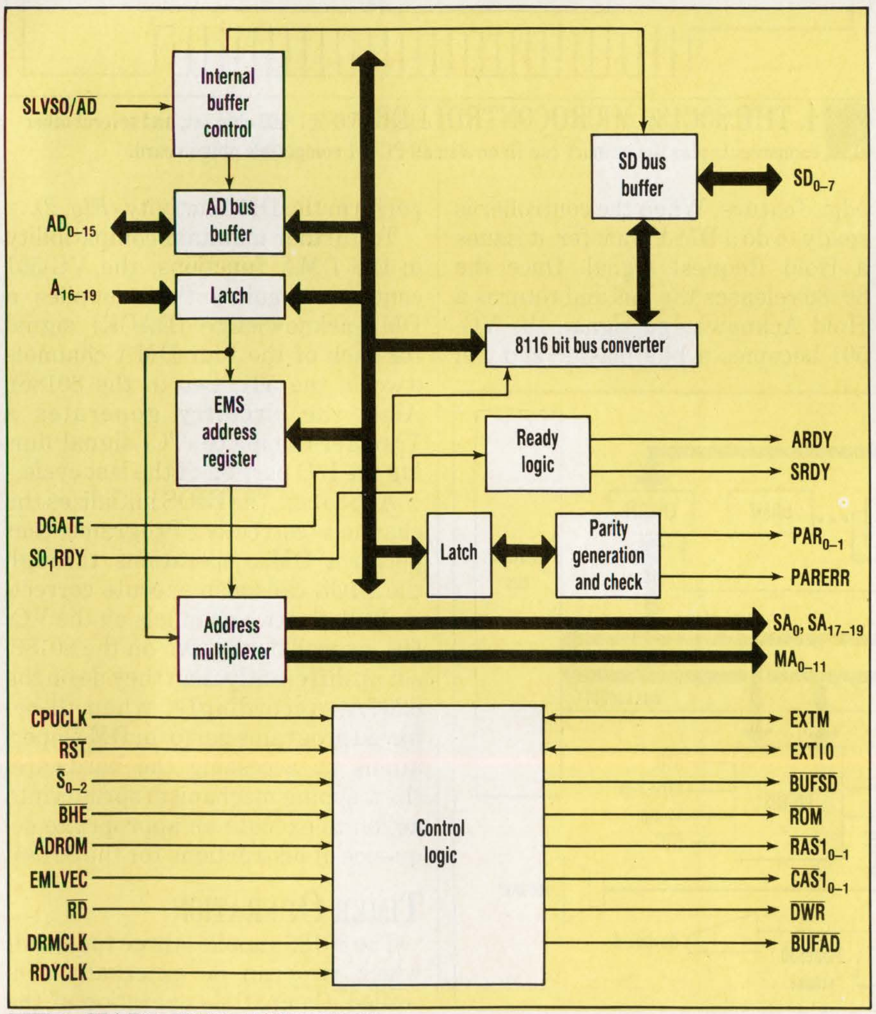
Interrupt Controller

The 80186 internal interrupt controller operates in several modes. All but one force the use of fixed, internal interrupt vectors. The VG-501 chip acts as an external eight-channel interrupt controller, which is functionally compatible with the Intel 8259A *(Fig. 1)*. The 80186 then operates in a mode functionally equivalent to the 8088/8086 interrupt system. Accordingly, the VG-501 typically receives interrupts intended for the 8259A in a PC-compatible system.

The VG-501 passes those interrupts on to the 80186, which is in a cascade mode. The 80186 doesn't generate internal interrupt vectors in the cascade mode, but it uses external vectors generated by the 8259A-like circuit contained in the VG-501. Of course, the 80186 requires proper initialization to enter this mode.

Seven of the VG-501 interrupt-controller channels (numbers 0 and 2 through 7) are externally accessible, and the remaining channel (number 1) connects to the VG-501's internal keyboard-mouse controller. The interrupt controller's output connects to the 80186's INT0 pin.

When the 80186 receives the interrupt, it carries out an Interrupt-Acknowledge (INTACK) cycle absorbed by the VG-501, which responds externally the same way as the 8259A. Consequently, PC-type software interrupt routines execute



3. HARDWARE SUPPORT for extended memory is built into the VG-502 chip, making it possible for transparent access to a memory space of 32 Mbytes.

without change.

Although the interrupt controller in the VG-501/80186 functions identically with the 8259A in the PC, the VG501 interrupt controller is initialized differently. Ill-behaved programs, which attempt to access the interrupt controller directly through I/O address 20 and 21, are trapped in the hardware and corrected through the NMI structure. The BIOS handles the initialization at boot up in a normal fashion. Also, the application program, which interrogates or alters the interrupt controller operation by calls to the BIOS, operates in a normal fashion.

DMA CONTROLLER

The 80186 supplies two independent DMA channels, yet the PC architecture calls for four. Therefore, to make the 80186 PC compatible, the VG-501 chip includes the two additional channels. One channel transfers floppy-disk data, and is programmable in a single transfer mode compatible with the 8237A. The second channel serves refresh cycles. Though nonprogrammable, it's functionally compatible with channel 0 of the 8237A in the single transfer mode.

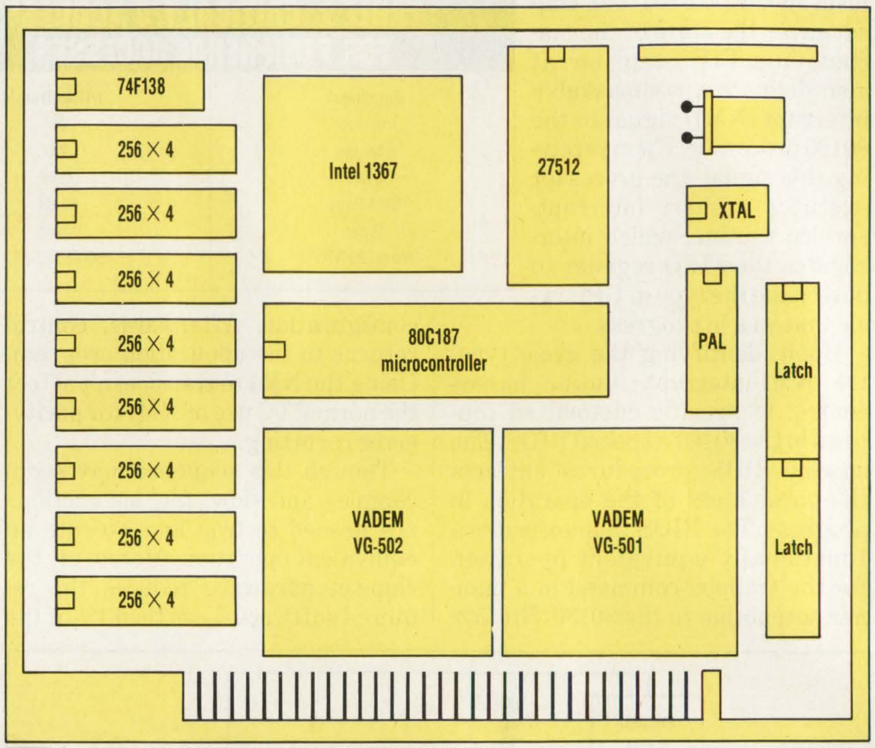
The VG-501's DMA controller uses the 80186 Hold Request/Acknowledge feature. When the controller is ready to do a DMA transfer, it issues a Hold Request signal. Once the 80186 releases the bus and returns a Hold Acknowledge signal, the VG-501 becomes a bus master and can perform the DMA activity *(Fig. 2)*.

To further maintain compatibility in the DMA functions, the VG-501 contains circuitry that supplies a DMA-acknowledge (DACK) signal for each of the four DMA channels (two in the 501, two in the 80186). Also, the circuitry generates a Transfer-Complete (TC) signal during the I/O portion of the last cycle.

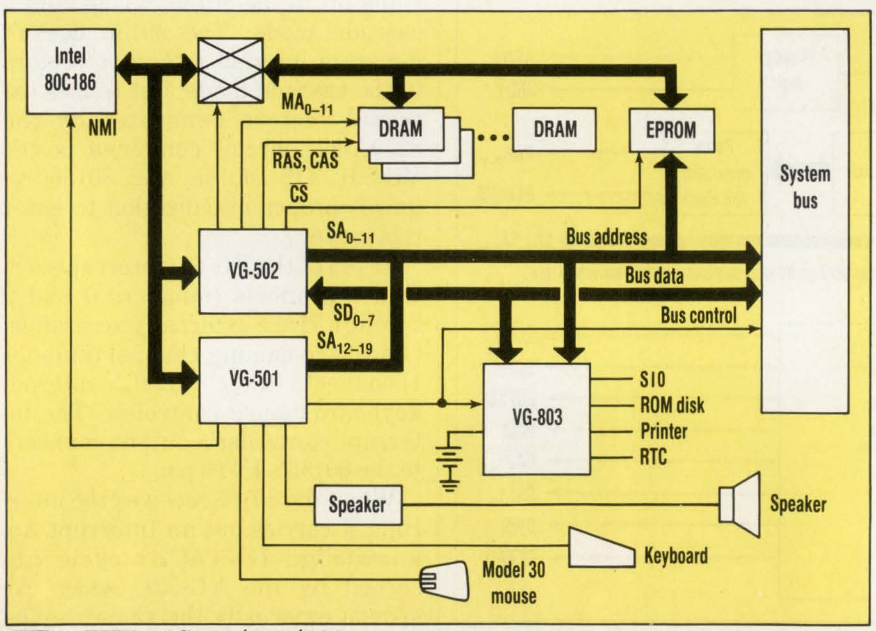
At boot up, the BIOS initializes the channels correctly. Programs that perform DMA operations through the BIOS calls also execute correctly. Still, the two channels on the VG-501, as well as the two on the 80186, set up differently than they do on the 8237A. Accordingly, when ill-behaved programs perform DMA operations by accessing the hardware, the trapping mechanism springs into action to execute an appropriate sequence of instructions for the 80186.

TIMER OPERATION

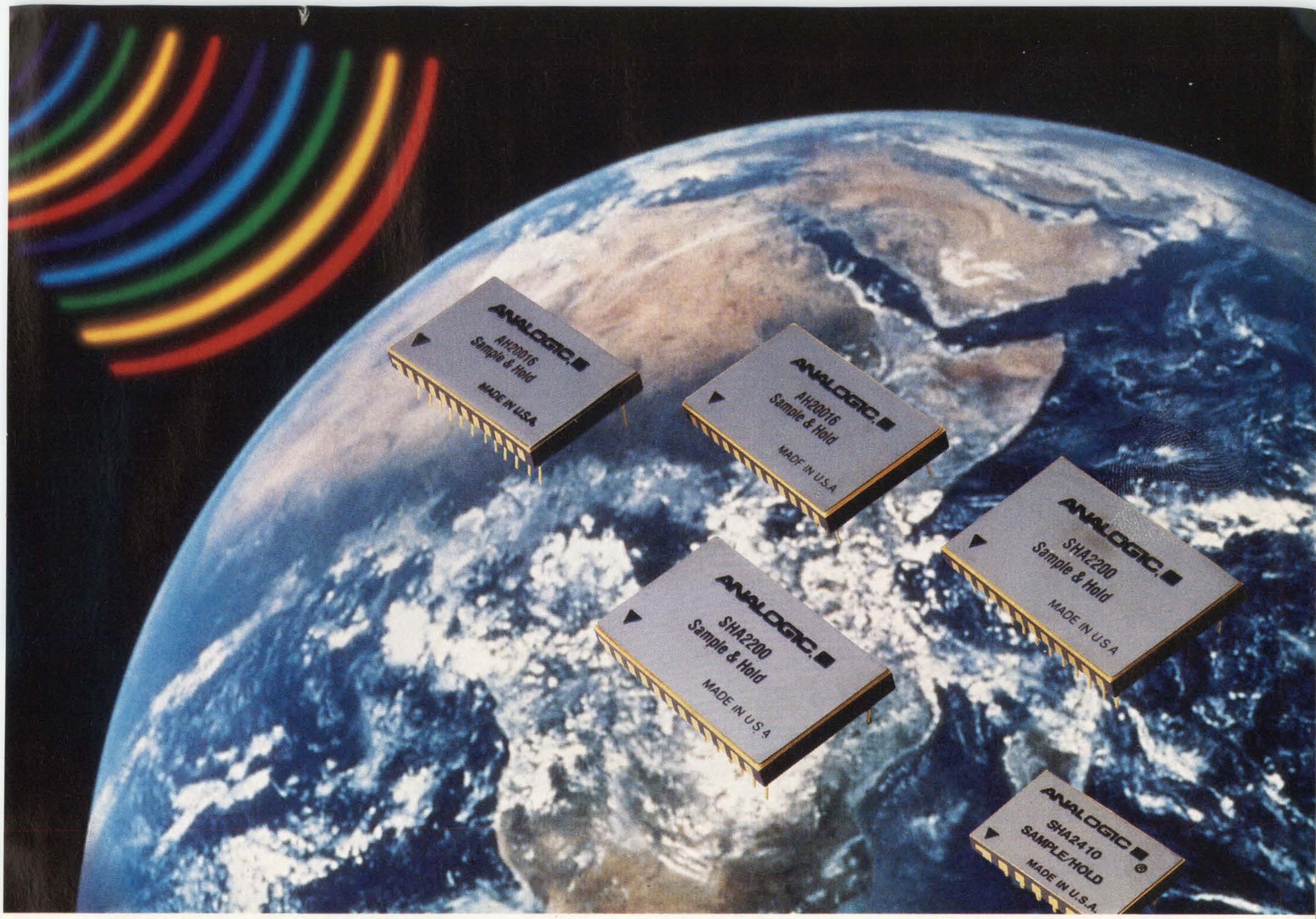
The 80186 supplies three timers, of which two can be externally controlled. Compatible operation of the on-board 80186 timers was perhaps the most challenging problem. The



4. THE 80C186 MICROCONTROLLER, VG-501/502 chip set, and several other components plus the memory can fit on a small PC/XT compatible plug-in card.



5. THE 80C186/501/502 chip combination can also serve in a PS/2 Model 30 compatible system.



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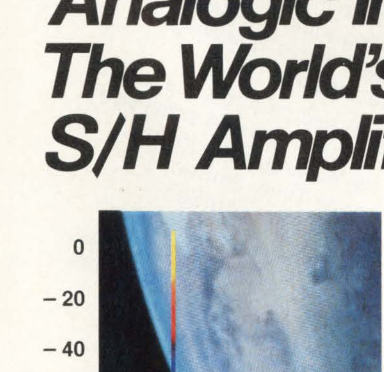

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code sequences that set up the 80186's timers differ from the 8253's timers used in the PC. As with the DMA, the BIOS handles initialization of the 80186 timers at boot up. Consequently, well-behaved programs that access the timers through BIOS calls operate correctly. Again, the NMI-trapping logic corrects the access to the timer hardware from ill-behaved PC applications that access the timer hardware directly. This underscores the importance of trapping-logic performance for the timers.

The 80186 timer channel 0 handles the system clock—the equivalent of the PC timer channel 0, and the 80186 timer channel 1 handles the speaker clock—the equivalent of the PC timer channel 2. The VG-501 supplies the inputs for these 80186 timer channels 0 and 1 by dividing the system's 14-MHz clock by 12. PC timer channel 1 normally serves as the refresh timer, a function handled completely within the VG-501.

Full control over the PC BIOS is a key element for successfully implementing an 80186-based PC. A standard off-the-shelf PC BIOS won't give the appropriate

PC ARCHITECTURE FOR EMBEDDED SYSTEMS

PC architecture isn't an obvious choice for embedded systems. PCs are generally associated with the MSDOS operating system and floppy or hard-disk drive usage. Embedded systems, however, are usually ROM based and diskless. Also, PCs don't require fast interrupt response times for handling external events. Furthermore, PC applications are single-threaded and generally deal with only one task at a time. PCs contain few elements to increase the reliability or maintainability of the system.

Nevertheless, the PC architecture isn't as bad a choice for embedded systems as it might appear. ROMable code can be written for PCs. New chip sets, BIOS developments enable existing PC applications to be based in ROM (or EPROM), whether or not the application was originally written for ROM. This capability even extends to DOS. The PC's interrupt architecture and response times are adequate for all but the most performance-intensive data gathering and control applications, and the higher speed processors now available for the PC architecture supply coverage of several of these applications.

Furthermore, a host of software companies now offer real-time multitasking operating systems for the PC architecture. They're either DOS compatible, run together with DOS, or take over the system completely. The fundamental underlying standard is the well-known PC architecture.

Because it's known that PC architecture deficiencies can be addressed for embedded applications, what are the advantages of the PC architecture? The most overwhelming gain may be the great wealth of off-the-shelf PC software and

CIRCLE 14

hardware.

Many portions of an embedded system can be purchased directly, as opposed to developed from scratch. This reduces time to market, which usually translates to higher prices, better margins, and a greater market share for the resulting product. Other factors that affect time to market include the availability of PC-compatible solutions at the box, board, and chip level. Board-level PC-compatible solutions are available for various popular bus architectures, such as the Multibus, VME, S-100, STD, and Eurocard, as well as the PC Bus. Such vendors as Ampro make a small form-factor busless single-board PC.

Even at the chip level, designs are simpler than ever due to the highly integrated chip sets available from various vendors. Embedded software can be prototyped on the ubiquitous desktop PCs before committing to EPROM for the embedded system prototyping.

Other factors favoring the PC architecture are the pricing for PC-compatible boards and chip sets that are driven by the high volume of PC sales themselves. These 10-million plus units per year bring down the manufacturing cost for PC-compatible components. Finally, the increasing attention on portable and laptop PCs is driving higher levels of integration for PC components, shrinking the size of PC implementations, and reducing power consumption to new low levels.

peripheral initialization for the 80186 and the necessary trapping code. Therefore, a special BIOS for the 80186 is needed. Without extensive PC-BIOS experience, the system designer would do best to steer clear of this task. The 80186 PC BIOS from Vadem designed to work with the VG-501/502 chip set offers full IBM PC/XT and PS/2 Model-30 compatibility.

Once the architectural approach to supplying PC compatibility with the 80186 is clear, the most difficult task is to supply adequate system performance. At initialization during boot up, and for well-behaved programs, the VG-501/502 chips' performance doesn't differ from the standard PC architecture. Ironically, those programs that access hardware directly to increase performance are the ones that impact the overhead of the trapping logic. With the timers integrated on the 80186, this is most difficult area of trapping logic.

Moreover, timer performance is most critical at slow processor-clock speeds, because the time to execute trapping code is most significant at this point. The timer adjustment for the trapping code must include the time consumed by the trapping logic, the decode logic, and the setup code. But the timers may not supply the accurate fine resolution needed at slow processor clock speeds with this VG-501/502 and 80186 approach. This problem has most impact on some game program sound effects.

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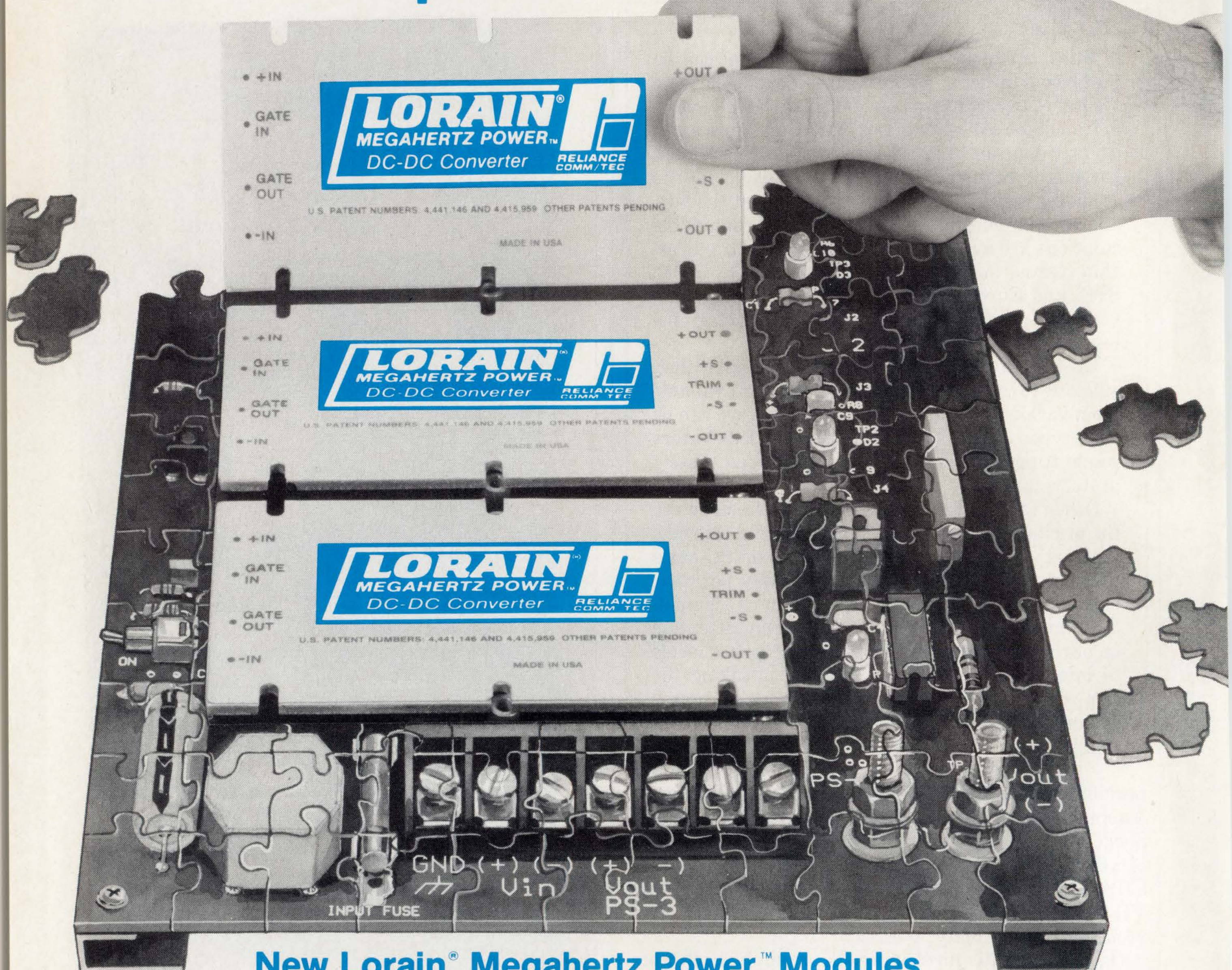

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PC-COMPATIBLE 80C186

Nevertheless, it hasn't affected the correct operation of any of the hundreds of PC application programs tested to date.

In addition to the timer problem, the memory controller offered several special challenges. First, the 80C186 can operate at speeds up to 16 MHz. No other PC/XT or PS/2 Model-30 compatible processor performs at that level. While higher performance systems built around the 80286 and 80386 require 80 ns or faster dynamic RAMs, use of such expensive DRAMs with a lower cost microcontroller, such as the 80186, would defeat one purpose in selecting the 80186. Consequently, the VG-501/502 chip set highly optimizes the memory controller to work at 16 MHz, with zero wait states and DRAMs operating at 100 ns. Furthermore, the memory controller can support either 256-kbits, 1-Mbit, or 4-Mbits DRAMs in either the by-1 or by-4 configurations.

Finally, the original PC architecture systems are based on an addressable memory space of 1 Mbyte. In the DOS-compatible environment, only 640-kbytes of this space was available to application programs. Many current embedded systems seek to go beyond this 640-kbyte limitation and find the traditional DOS environment constraining. The PC system designers have evolved several extended-memory alternatives to solve the problem. The most recent, and perhaps the most popular, is the LIM (Lotus, Intel, Microsoft) standard known as EMS 4.0. Hardware support for this extended memory standard is built into the VG-502 chip, making it possible for transparent access to an extended-memory space of 32 Mbytes *(Fig. 3)*.

Accordingly, the task of supplying a full solution for 80186 usage in embedded PC-compatible systems is only slightly more difficult than supplying it for the 8086. The 80186, VG-501/502 chip set, and a few other components plus the memory can fit on a small PC/XT compatible plug-in card *(Fig.4)*. Similarly, this chip combination can serve in a PS/2 Model 30 compatible system *(Fig. 5)*. The remaining tasks are for design engineers working on embedded systems to evaluate the opportunities presented by PC compatibility for the processor, which has proven to be the most popular for embedded control applications.☐

Paul Rosenfeld, Vadem's chief operating officer, has an extensive background in systems and component marketing, including seven years at Intel Corp. He holds a BA in Math from the University of California, Berkeley.

Ralph Woodard, a design engineer at Vadem, has experience both as an electronic technician and engineer. He is currently designing ASICs for PC compatible systems.

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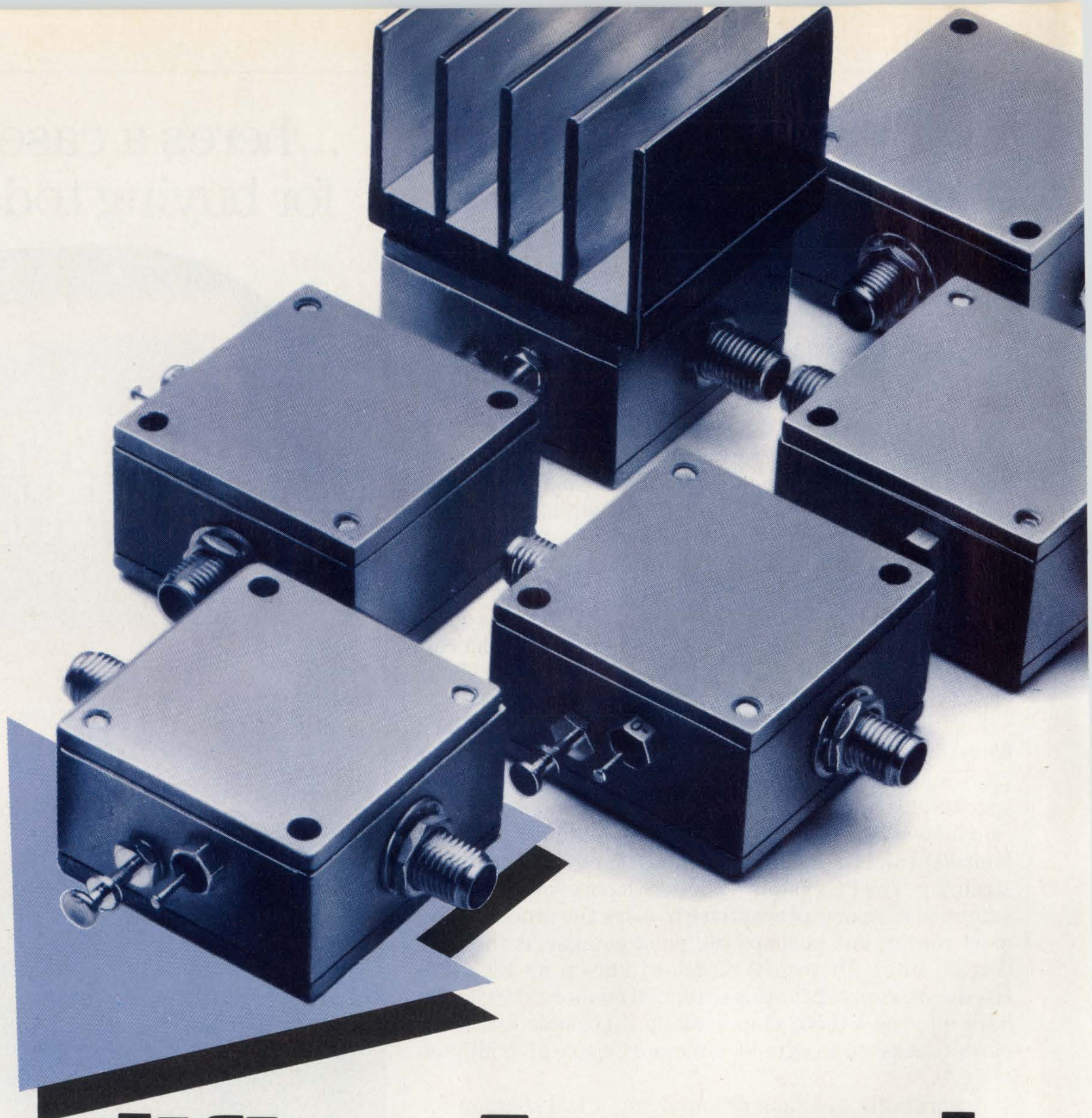
MODERATELY	548
SLIGHTLY	549



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ZFL-1000H	10-1000	28	+20	5.0	219.00
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ZFL-1000VH	10-1000	20	+26	4.5	229.00
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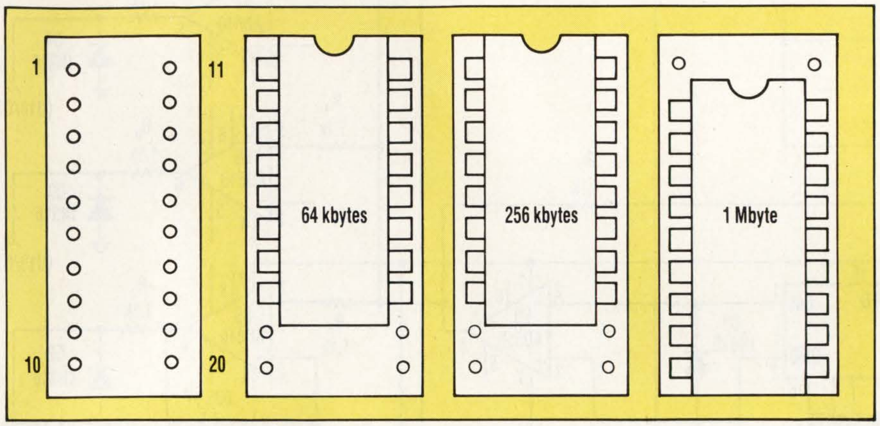
CIRCLE

521 UPGRADE WITH 1-MBYTE DRAMS

DON MACADAM
Annulus Technical Industries Inc., P.O. Box 7407, 1296 Osprey Dr., Ancaster, Ontario, Canada L9G 4G4; (416) 648-8100.



A 64- OR 256-KBYTE DRAM sits in the upper portion of a 20-pin socket, while a 1-Mbyte part is placed in the socket's lower section.

Today's designers are more apt to upgrade dynamic RAMs because they're less expensive. Upgrading is an easy task with 16-, 64-, and 256-kbyte DRAMs, which come packaged in 16-pin DIPs and have compatible pinouts. Unfortunately, 1-Mbyte chips are packed in 18-pin DIPs and have an entirely different pinout configuration.

One solution to this problem is to use a high density switch to reconfigure the source and destination of the pc-board traces between the DRAM array and the rest of a system. In an array of 32 DRAMs, organized as four banks of eight chips each, there are 41 traces to be reconfigured between the array and the rest of a system.

The problem is further simplified with 20-pin IC sockets that offer the maximum number of matches between the 16- and 18-pin formats. When the array is populated with 64- or 256-kbyte DRAMs, the parts are seated in the upper portion of the sockets. 1-Mbyte parts, however, are seated in the lower position *(see the figure)*.

In this arrangement, only 21 circuit traces must be reconfigured. When the high density switch is in its "A" position, signals are sent to the IC sockets in the pattern required by 64- and 256-kbyte DRAMs. But when placed in its "B" position, signals are presented in the 1-Mbyte DRAM pattern.□

IFD WINNERS

April 27, 1989

Jeff Barrow, Craven Hilton, and Frances Lucas, Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. His idea: *"Eliminate Oscillator From A Loop."*

May 11, 1989

Michael A. Wyatt, Space and Strategic Avionics Div., Honeywell Inc., 13350 U.S. Hwy. 19 South, Clearwater, FL 34624-7290. His idea: *"Phase Meter Uses Just Two Chips."*

May 25, 1989

Warren Schultz, Motorola, SPS, 5005 E. McDowell Rd., Phoenix, AZ 50008. His idea: *"Drive Brush Motors With Brushless IC."*

CIRCLE

522 STEP DRIVER DELIVERS 0.1 TO 9 A

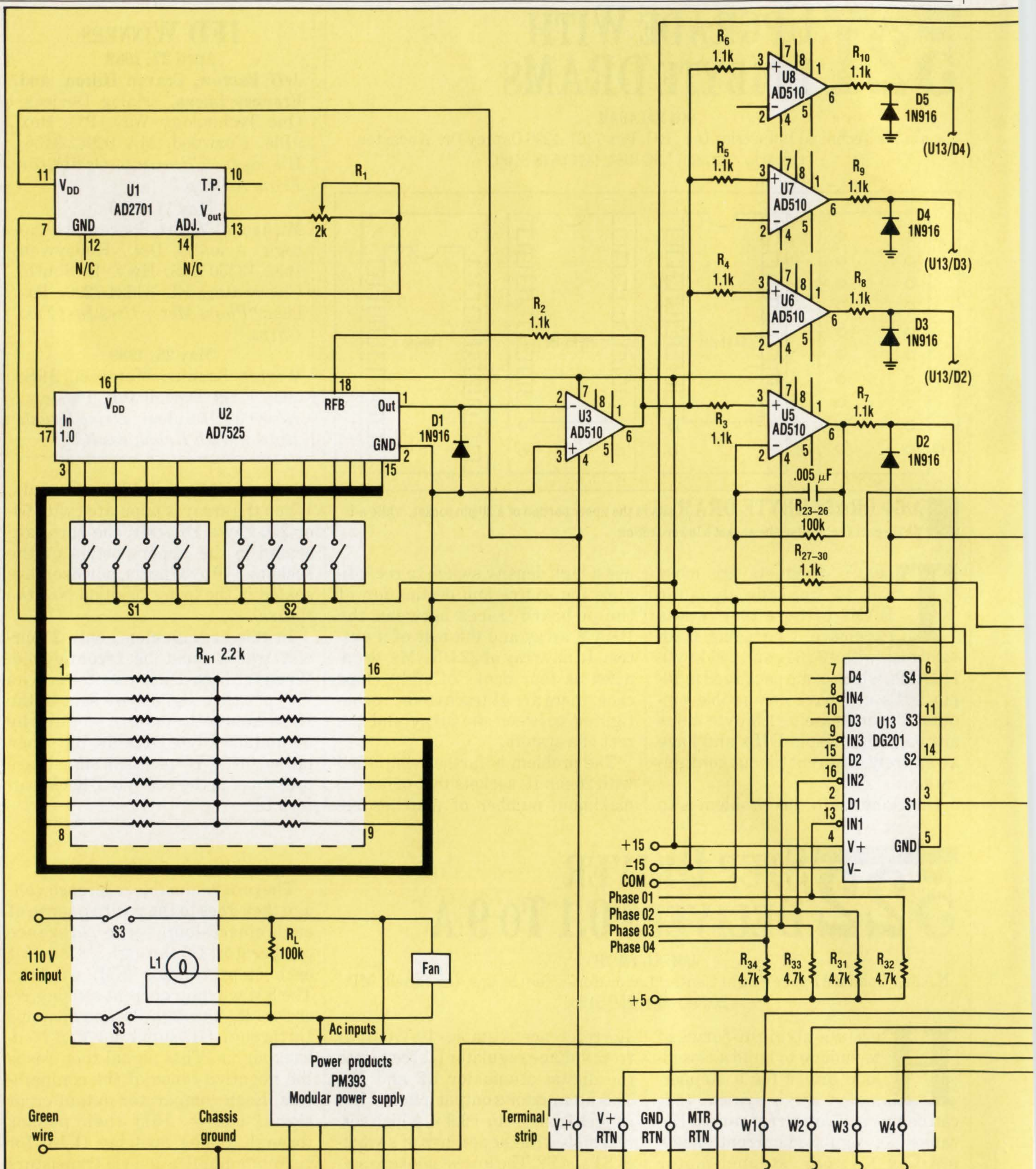
JAMES C. SMITH
NASA/Goddard Space Flight Center, Laboratories for Oceans, Greenbelt, MD 20771; (301) 286-5185.

Here's a straight-forward technique to build a closed-loop driver for a stepper-motor servo system that can deliver a wide current range. The range is a regulated current of 100-mA-to-9.9-A per stepper-motor phase *(see the figure)*.

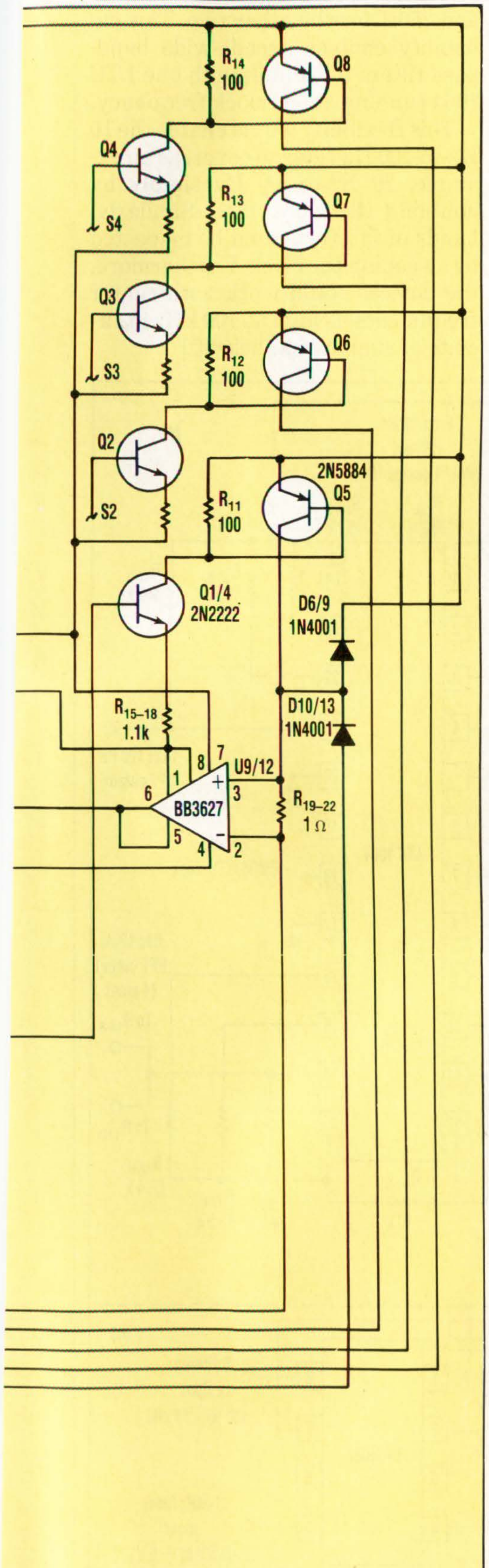
Components U1, U2, U3, and thumbwheel switches (TWS) S1 and S2 establish a programmable voltage reference. A stable –10-V output from voltage regulator U1 feeds into the digital attenuator U2 and U3. This attenuator's output (pin 6 of U3) ranges from 0.0 to +9.9 V, which corresponds with the settings of switches S1 and S2. The lowest nonzero setting is 0.1 V. Adjusting R_1 to establish the desired programmable output-voltage relationship between the TWS settings and the output voltage range calibrates this function.

The programmable reference voltage then goes to the positive sense of each closed-loop servo reference comparator, U5 through U8, one for each stepper-motor (SM) winding. The SM winding current-sensing resistors R_{19} through R_{22} and op amps U9 through U12 supply a 1-V/A feedback signal. That signal then feeds the negative sense of the comparators. Each comparator output-error signal (Av = 101) then passes through analog switches (U13) for current amplification via transistors Q1 through Q4 and Q5 through Q8.

Servo-loop control adjusts the current through each SM winding to equal the programmable output-ref-



THE OUTPUT RANGE of this stepper-motor's drive circuit is a regulated current of 100 mA to 9.9 A per phase.



erence voltage (1 A/V). Consequently, the TWS settings correspond to the desired SM winding control current value range of 0.1 mA to 9.9 A.

The analog switches (U13) supply correct phases for the closed-loop servo operation. In other words, when the appropriate SM phase signal is active, it closes the corresponding analog switch to complete the servo-loop feedback path and to establish the programmed drive current in the SM winding. When the SM phase signal is inactive, the analog switch is open and the closed-loop control servo becomes disconnected. This condition doesn't offer drive current to the emitters of Q5 through Q8. The voltage rating of Q1 through Q8 limits the maximum value of V+. S1 and S2 determine the maximum current supplied to the motor, and the subsequent control servo regulates the current.□

CIRCLE 523

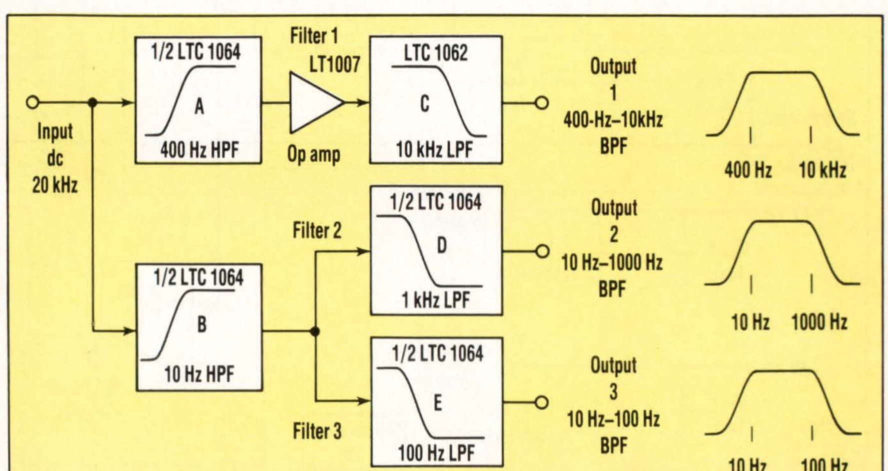
Switch-Cap ICs Filter Transducers

RICH MARKELL
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.

Sophisticated filter-system designs frequently need expensive printed-circuit boards that are replete with op amps and precision capacitors. Digital filters require fewer yet more expensive devices and a great deal of software. But help is on the way with advances in switched-capacitor filters that make the design of elegant filter systems cheaper, easier to operate, and much smaller. Determining resistor values for setting the filter frequency is the chief design problem with switched-capacitor filters. It's a minor problem, though, after considering the advantages.

Signals covering a dc-to-10 kHz range into a typical switched-capacitor system for filtering transducers can be divided into three bandpass-frequency areas *(Fig. 1)*. Filter 1 is a 400 Hz-to-10 kHz filter with a passband noise of 200 μVrms; filter 2 is a 10 Hz-to-100 Hz filter with a passband noise of 500 μVrms; and filter 3 is a 10 Hz-to-1 kHz filter with a passband noise of 390 μVrms. All of the bandpass outputs have 1-dB ripple in the passband.

This implementation uses two LTC 1064s and one LTC 1062 switched-capacitor ICs, and one LT 1007 op amp *(Fig. 2)*. The LTC 1064s are quad switched-capacitor filters that can implement up to 8th-order filters. Filters 2 and 3 consist of one half of a four-section LTC1064 —a 10-Hz



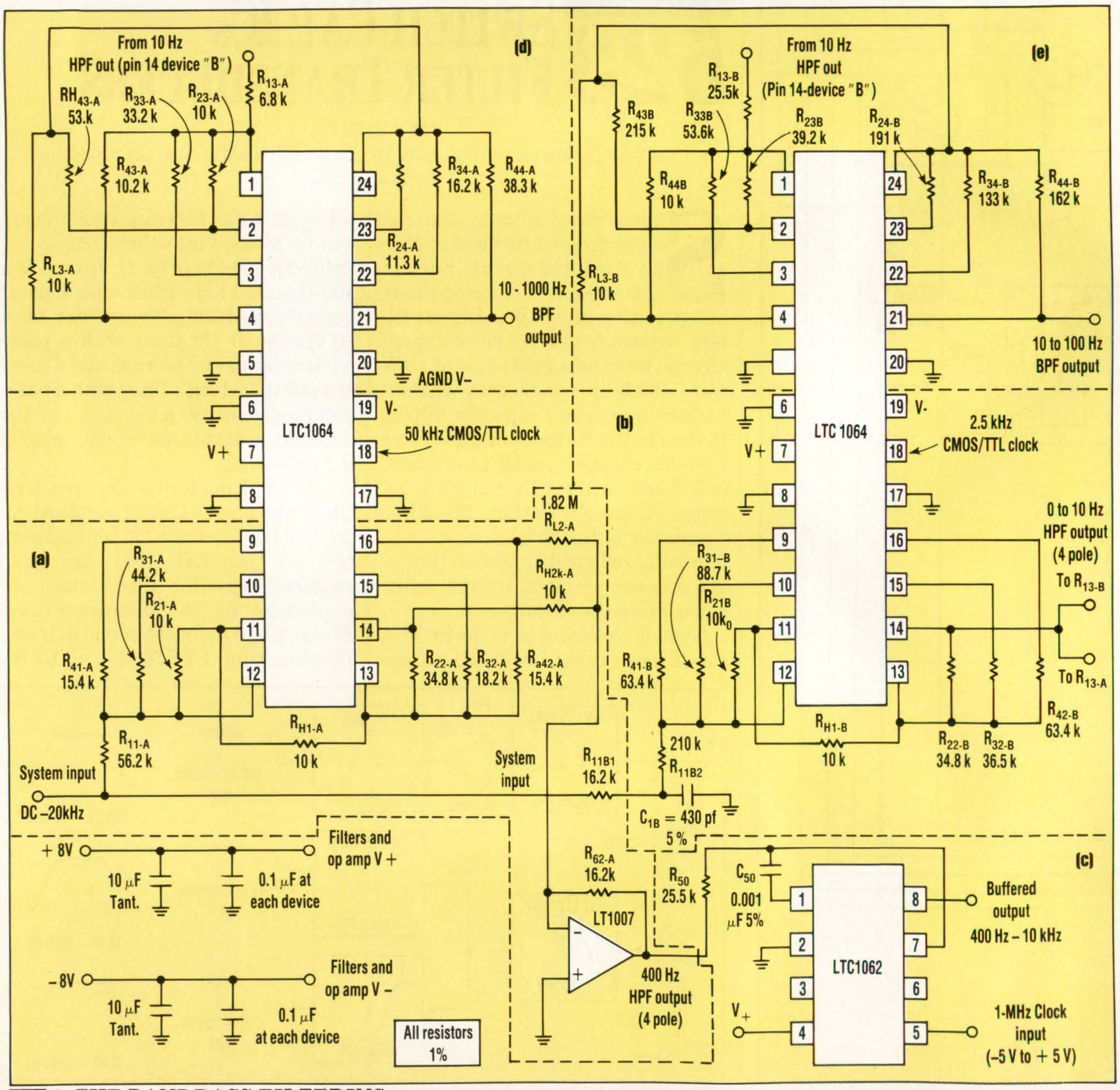
1. SIGNALS covering a dc-to-kHz range are split into three bandpass-frequency areas.

high-pass 4th-order elliptic filter—that feeds two separate low-pass 4th-order elliptic filters each made with half of an LTC1064. One cuts off at 100 Hz, the other at 1 kHz. In filter 1, a 400-Hz high-pass 4th-order elliptic filter feeds a 5th-order low-pass Butterworth filter set at 10 kHz.

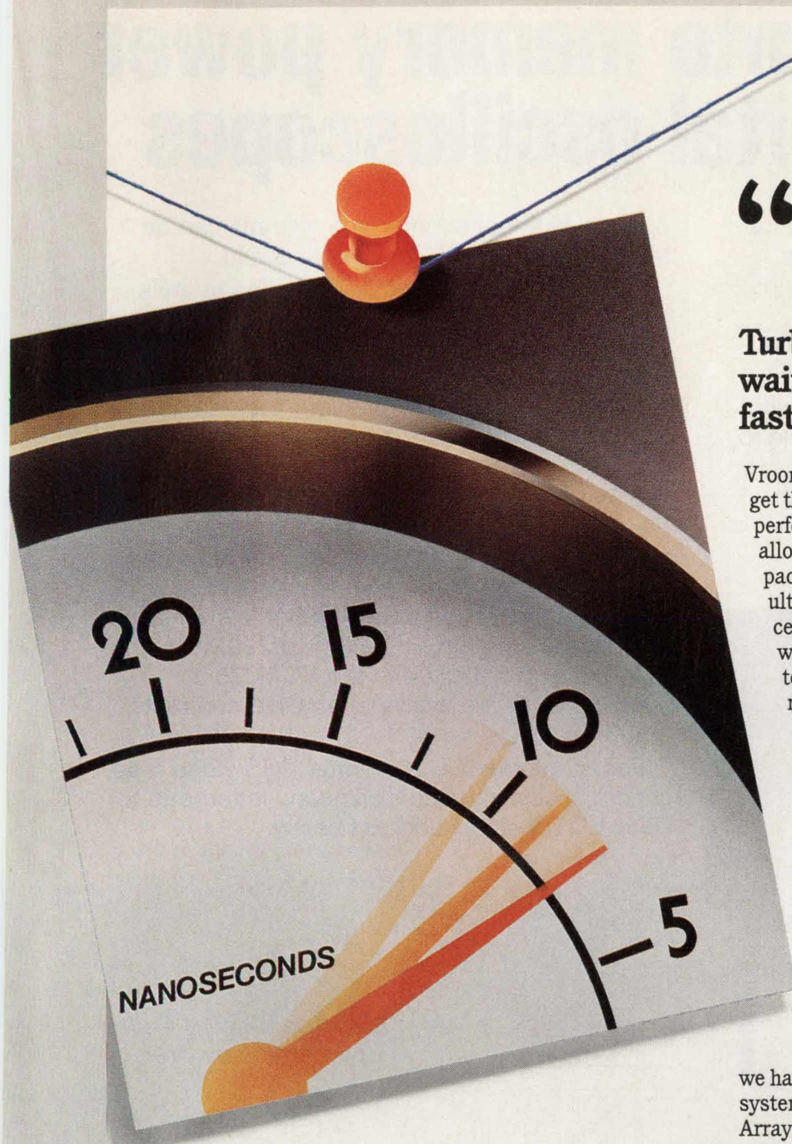
Resistors R_{11A} to R_{H2A}, with R_{G2A} and the LT1007 op amp, implement the 400-Hz high-pass filter in device A. Resistors R_{13A} to R_{44A}, also in device A, implement the 1-kHz low-pass filter. In Device B, resistors R_{11B1} to R_{42B} implement the 10-Hz high-pass filter, and resistors R_{13B} through R_{44B} implement the 100-Hz low-pass filter. Lastly, R_{50} and C_{50} program the LTC 1062 for 10 kHz.

The LTC 1064 devices make it possible for two sections to operate in a 100:1 clock-to-center frequency mode while two others run in a 50:1 mode. Thus, resistor programming can change the clock-to-center frequency range to 25:1 for two sections and 250:1 for the other two. This capability enables decade-wide bandpass filters to be built with one LTC 1064 running at one clock frequency.

This flexibility would enable the 10 Hz-to-100 Hz filter to cover, as an example, 20 Hz-to-200 Hz simply by doubling the clock rate. Similarly, bands of interest could be inspected by sweeping the clock. Furthermore, the devices could work with center frequencies as high as 100 kHz in circuits of similar simplicity.□



2. THE BANDPASS FILTERING system uses two LTC 1064 and one LTC 1062 switched-capacitor ICs, and one LT 1007 op amp.



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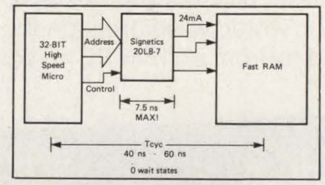

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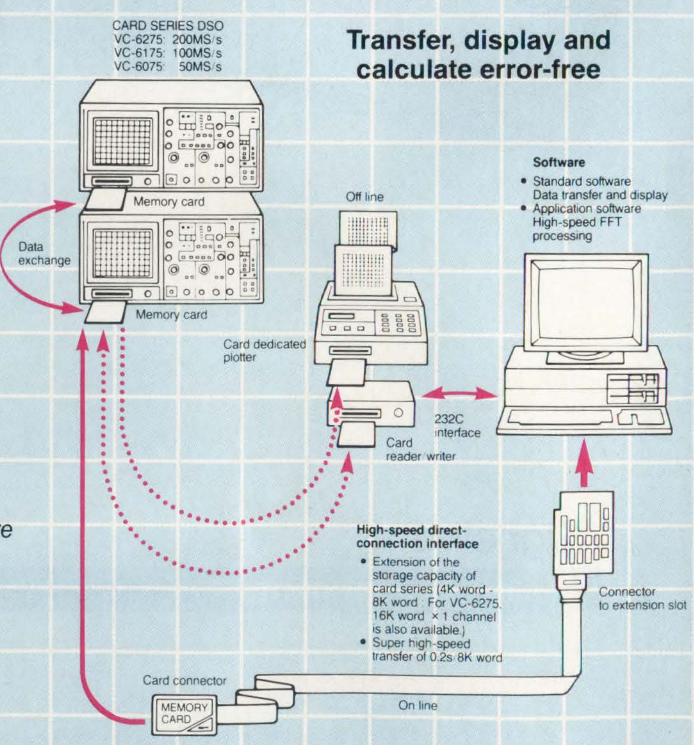

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CIRCLE 56

OP AMPS IMPROVE IN PRICE-PERFORMANCE

A joint development-manufacturing-marketing agreement between Maxim, Sunnyvale, Calif., and VTC (a subsidiary of Control Data), Bloomington, Minn., should result in future innovations in high-speed, wide-bandwidth IC op amps, comparators, digital-to-analog converters, and analog-to-digital converters. Initially, Maxim will broaden the linear marketing base of VTC's current line of high-speed op amps and comparators. Down the road, new products will take advantage of both Maxim's design expertise and VTC's process technology. This technology is a complementary, $\pm$5-V process that builds npn transistors with a cutoff frequency of 6 GHz; the cutoff frequency of the pnps runs 1.2 GHz. These transistors in turn build IC op amps, such as the VTC VA708 (Maxim's MAX 408) that slew at 90 V/μS (minimum), which translates to a full-power bandwidth of 4.8 MHz. And the op amps settle in 200 ns (maximum) to 0.1% for a 2-V step. Moreover, they can drive 50-Ω loads. Dual and quad versions are also available. Contact Jerry Thimsen at VTC, (612) 851-5200, or Brian Gillings at Maxim, (408) 737-7600. FG **CIRCLE 301**

WIDE-BAND OP AMPS COME IN TINY SO-8 PACKAGE . . .

Comlinear, Fort Collins, Colo., will introduce all of its wideband IC op amps and buffers in small-outline packages. The first three devices, in SO-8s, are the 200-MHz (3-dB bandwidth at a gain of 2) CLC400, the 150-MHz CLC401 (3-dB bandwidth at a gain of 20), and the closed-loop unity-gain buffer, the 730-MHz CLC110 (3-dB bandwidth). All settle to 0.02% in under 15 ns for a 2-V output step. The combination of small size, low cost ($9.25 each in 1000s), and low power (150 mW) makes them attractive for high-volume commercial applications. Call Scott Evans, (303) 226-0500. FG **CIRCLE 302**

. . . ANOTHER SPORTS PRECISION, LOW NOISE

The OP-61 fast precision op amp from Precision Monolithics Inc., Santa Clara, Calif., has a typical gain-bandwidth product of 200 MHz, and at a frequency of 1 MHz, it's stable at gains of 10 or above. With that kind of ac performance, the premium OP-61A still offers a maximum offset voltage of just 500 μV and maximum offset drift of 5 μV/°C. Input-voltage noise at 1 kHz is typically a low 3.4 nV/$\sqrt{\text{Hz}}$. And it will typically settle a 10-V output step in under 330 ns. PMI is offering the model free to designers doing Spice simulation. In quantities of 100, the extended industrial-grade units start at $4.25 each. Small quantities are in stock. Contact Al Neves, (408) 562-7181. FG **CIRCLE 303**

8-BIT CPU CHIPS FEATURE EMBEDDED FOCUS

Zilog is still updating its Z80 microprocessor family, putting microcontroller-like features on the CPU chip. The latest implementation adds 2 kbytes of static RAM and a clock generator. As a result, time-critical data or instructions held in the new Z84C50 chip's static memory can be accessed with no wait states. This enables the processor to execute even faster than if the memory was off the chip. The new on-chip clock generator gives the processor four operating modes to save power: There are run and stop modes and two intermediate idle modes—one stops the clock and CPU; another stops the CPU but keeps the clock running. Contact Jim Magill, (408) 370-8000. DB **CIRCLE 304**

NETWORK SOFTWARE ENDS MEMORY CONFLICTS

Users can run large, memory-hungry applications while still accessing network data with the VM/386 NetPak from IGC, Santa Clara, Calif. The software overcomes the 640-kbyte RAM limitation encountered with most computers. VM/386 NetPak extends IGC's VM/386 multitasking program for 80386-based computers. With the software, users can run multiple DOS applications simultaneously and access network data and peripherals from any one of those applications. Data is accessed from the file server without the need to first download it to a local hard disk. Each application runs on a virtual machine that contains DOS and compatible programs. To overcome the 640-kbyte memory limitation, users can load all network drivers into one virtual machine, while applications are loaded into their own virtual machines. Networks supported by the software include IBM Token Ring, Novell, and 3COM. Requiring a 80386-based computer running VM/386, NetPak costs $150 and is shipping now. Contact Steve Rogaway, (408) 986-8373. LG **CIRCLE 305**

I/O BOARD BOOSTS PROCESSING POWER

The ZT 8832 I/O control processor (ICP) board from Ziatech Corp., San Luis Obispo, Calif., modularly increases the processing power of an STD bus-based system. One or more ICP boards can be added to a STD-bus system in a multiprocessing configuration to handle real-time I/O tasks and to offload the main processor. The number of ICP boards in a system is only limited by the number of slots available in the card cage. The board is a surface-mounted, V40-based computer. Its features include 800 kbytes of memory, a numeric data-processor socket, two serial ports, three parallel ports, and an SBX expansion socket. Software support for the board includes a DOS Multiprocessing Extension (DOS EXP) program, which is an operating and development environment for multiple ZT 8832 boards running DOS-based software. The control processor is available now for $785 in single quantities. The DOS MPX development software costs $650. Quantity discounts are available. Call (805) 541-0488. LG **CIRCLE 306**

FIBER-OPTIC ETHERNET HOOKS DIRECTLY TO PC

Most fiber-optic Ethernet local-area networks require costly external transceivers and interfaces to connect with personal computers. But the FiberStar Ethernet network from Zenith Electronics Corp., Glenview, Ill., has a transceiver right on the PC adapter card, so the fiber network connects directly into the computer. The FiberStar Z-LAN10F network is the newest addition to Zenith's Z-LAN product line. It transmits data at 10 Mbits/s with 100% collision detection, and spans 4 km on one network without magnetic or radio interference. FiberStar conforms to IEEE 802.3 Ethernet standards. The Z-LAN10F system consists of an Ethernet adapter card that fits in any PC/XT/AT or compatible-bus computer, a FiberStar hub coupler that connects 8 or 14 devices, and an external transceiver with an Attachment Unit Interface (AUI) that connects the system with other Ethernet networks. Prices for the interface card, 8-port hub, 14-port hub, and external AUI transceiver are $895, $4175, $5975, and $595, respectively. Delivery is 90 days after receipt of order. Contact Robert Dranter, (312) 391-8000. LG **CIRCLE 307**

GRAPHICS OPTION BOOSTS SPEED BY UP TO 500%

The 4G graphics board from Tektronix Inc., Wilsonville, Ore., accelerates the graphics speed of the Tektronix XD88 workstation by 500%. Redraw rates top 1 million 2D and 3D vectors/s and 65,000 shaded polygons/s. This performance increase results from a pipelined design, a separate clipping engine that runs at 13 million operations/s, and more bit-slice and transform engines. XD88 workstations equipped with the upgrade easily handle large databases for scientific visualization, molecular modeling, and animation. Because the board is transparent to application software, users need not recompile or relink existing programs. Tek 4230 Series netstations and 4330 Series workstations can also be upgraded. The 4G board, which ships this month, costs $6000 as an installed option in a XD88 workstation; $8000 when purchased with a Tek 4230/4330 Series netstation or as an upgrade for any compatible Tektronix graphics system. Call (800) 225-5434. LG **CIRCLE 308**

DUAL OP AMP RUNS OFF JUST 2 V; 40 μA TOTAL

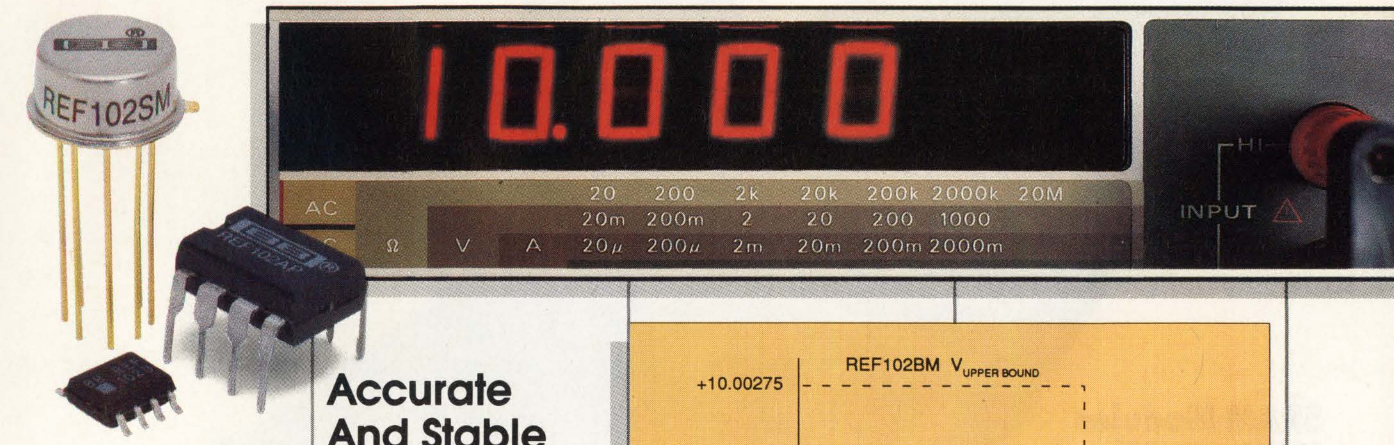
A true micropower op amp, the ALD2706, from Advanced Linear Devices, Sunnyvale, Calif., runs off a mere 2 V (or ±1 V). Moreover, this dual CMOS chip typically needs only 20 μA for each op amp (40 μA total). Maximum supply voltage is 12 V, making possible reliable operation from split ±5 V rails. In addition, a complementary p-channel/n-channel input stage allows the common-mode voltage to include both rails. Bias current typically runs 1 pA. Open-loop gain typically runs 100 dB—if driving at least 1 MΩ—but is still over 90 dB when driving 10 kΩ. Running off ±2.5-V rails, unity-gain bandwidth is 400 kHz; off ±1V rails, 300 kHz. Slew rate is 0.17 V/μs for either. With ±2.5-V supplies and driving 100 kΩ, the op amp's outputs will typically swing from 0.1 to 4.9 V. The ALD2706 comes in three grades with offset voltages of 2, 5, and 10 mV. In quantities of 100, the 10 mV device starts at $3.84 each. Call Mike O'Neal, (408) 720-8737. FG **CIRCLE 309**

40-FA ELECTROMETER COSTS UNDER $1

A dual CMOS IC op amp delivers micropower operation and femtoampere bias currents at the dramatically low cost of under $1—op amps with this performance have cost $15 to $25 each in the past. The LPC662 from National Semiconductor, Santa Clara, Calif., has a typical bias current of 40 fA (guaranteed minimum bias current is 20 pA). Of course, no one can afford to sell an IC for under $1 and still test for 90 fA. Bias current is actually checked at maximum temperature (either 85° or 125°C) and the room temperature value is calculated (bias current about doubles every 10°C.) The ultra-low bias current goes with an offset voltage and an offset temperature coefficient of 3 mV and 1.3 μV/°C coupled with one 5-V supply operation while drawing less than 60 μA per op amp. When driving a 5000-Ω load from a 5-V rail, the output typically swings from 0.04 to 4.94 V (a swing from 0.15 to 4.85 V is guaranteed). In quantities of 100, prices range from $0.90 to $1.95 each. Small quantities are available from stock. Call Bettina Briz, (408) 721-2274. FG **CIRCLE 310**

EDITED BY CLIFFORD METH

New 10.000V Reference Lowers The Price Of Precision



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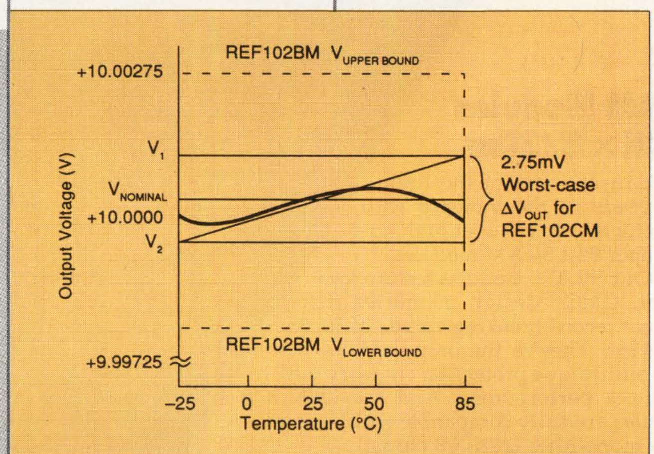

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CIRCLE 37

Large Libraries Plus Tight Tool Integration Equals Simple Analog And Digital ASIC Design.

Modify Chip Components To Fully Customize ICs

Richard Nass

Designers can hurdle the ASIC design obstacle course by switching to the Fastrack, a new system from Harris Semiconductor that eliminates the numerous stumbling blocks incurred when designing an ASIC from scratch. Now designers can leap over the task of integrating available toolsets, jumping from workstation to workstation, and figuring out just which direction to proceed in.

Fastrack was developed with a combination of libraries from Harris and GE Solid State, a result of Harris' recent acquisition of the GE division. The libraries contain bipolar and CMOS analog circuits and CMOS digital circuits.

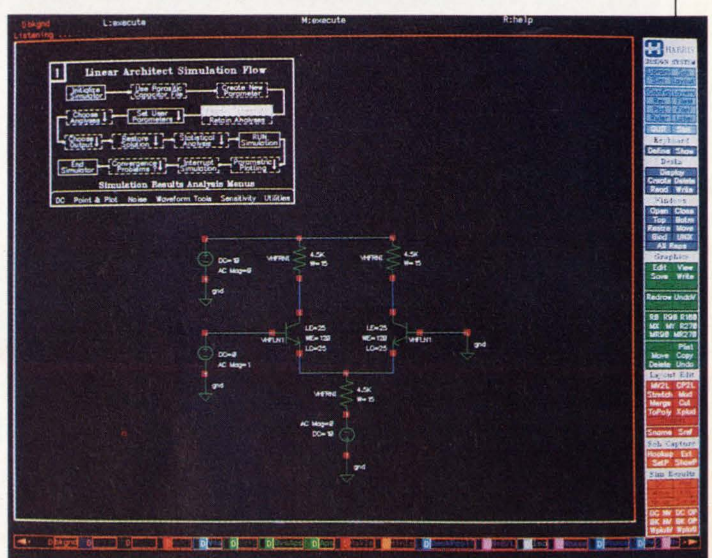
The system takes advantage of the Cadence framework. Its open architecture allows the best available CAE tools to be integrated. These tools were developed by Harris and other third-party software suppliers. The open architecture could also integrate system simulation with IC simulation tools.

Another advantage of the Cadence framework is a unified database, which keeps a design's physical and electrical representations in one database. This simplifies the user interface and allows all phases of the design to be completed on the same workstation.

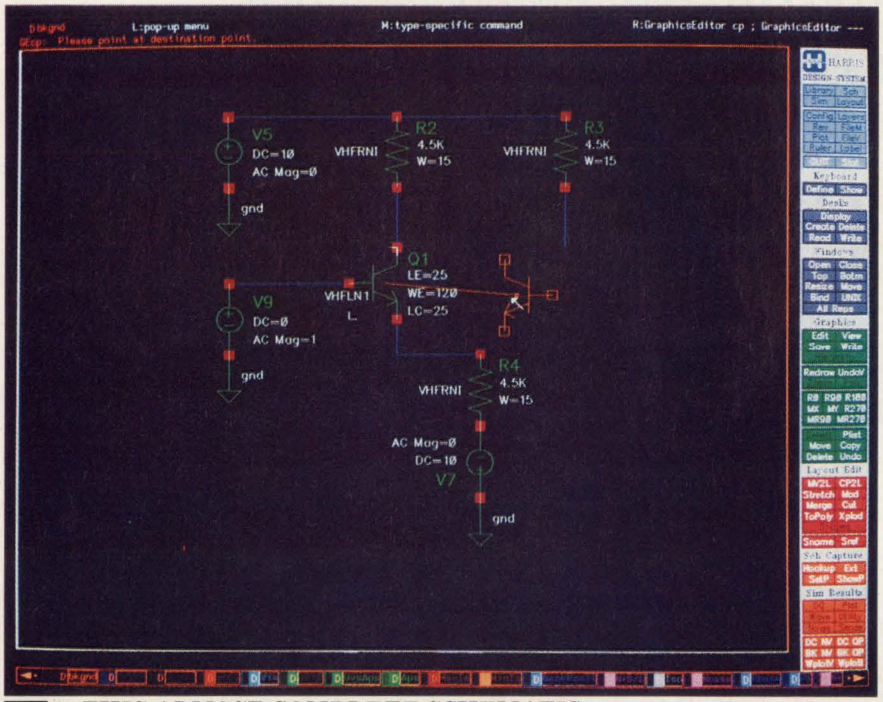
The tools support complete front-to-back design. The mouse-driven menus, windows, and on-screen help force users to go in the right direction along a step-by-step path—even first-time users will find it simple to operate *(Fig. 1)*. Moreover, error-prone tasks, such as generating a net list from a schematic, are automated with one command.

Most analog designers associate transistor-level design with the painstaking task of defining diffusion regions and interconnects within the ground-rule boundaries of a process. But designing transistors using Harris' Device Design, one of the Fastrack tools, can remedy some of that headache. The library has npn and pnp transistors optimized for specific applications, such as low noise, high current, or low collector resistance.

Once analog designers choose a device, four circuit parameters must be entered: minimum collector voltage, maximum emitter current, maximum

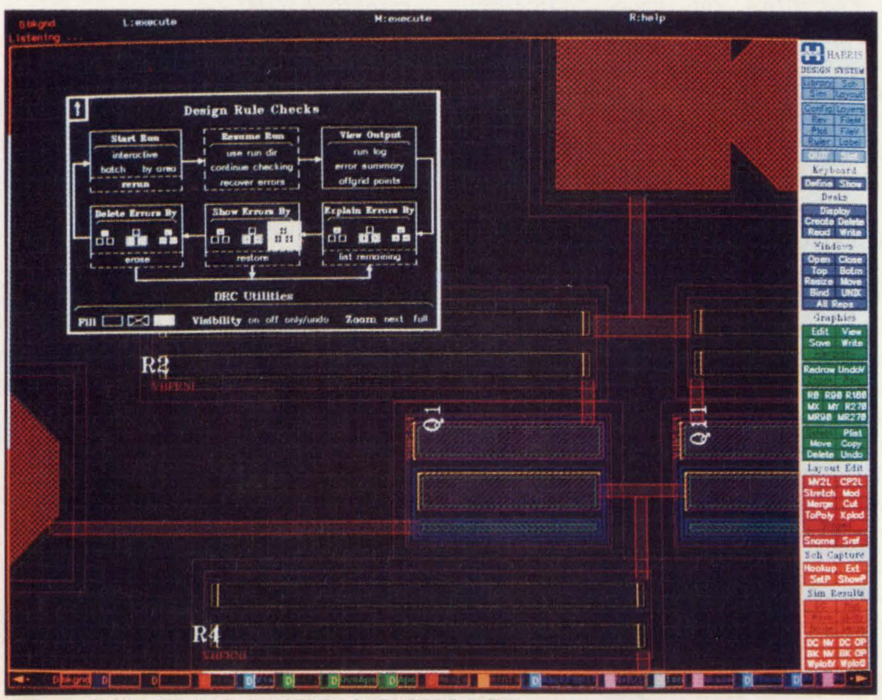


1. AFTER THE SCHEMATIC entry is complete, the design flow menu prompts users to the next step in the sequence.



2. THIS ALMOST-COMPLETE SCHEMATIC **shows all the devices with their parameters. A wire-entry tool is now used to interconnect the devices.**

operating temperature, and the condition to be optimized for (low noise, matched emitter resistance, etc.). By doing this, designers create a custom device made to their own specifications, rather than using a "prefab" model. Given this information and a prior knowledge of the process layout ground rules, the Device Design runs a device simulation to determine the transistor dimensions that comes up with custom-device geometries for each design.



3. ONCE THE LAYOUT IS COMPLETE, **the Design Rule Checker goes through its list of over 900 rules to be certain that none were violated.**

A Spice circuit file, or net list, is next created by the Readin Schematic. This schematic-capture tool eliminates manually entering the file. From this point, a preliminary electrical simulation can be run to make sure there aren't any problems with circuit performance. Users can next proceed to the physical design.

Harris' Slice (Simulation Language with Integrated Circuit Emphasis), the circuit simulator used by Fastrack, is an interactive, high-level programming language. It contains over 50 built-in mathematical functions and uses various simple high-level commands. These commands can perform ac, dc, transient, sensitivity, noise, and Monte Carlo analyses. The results of these analyses can be displayed in textual or graphical form. An interactive keyboard makes it easy for users to do complex calculations involving node voltages and branch currents. By simply pointing to a transistor node, users can obtain the operating conditions and model parameter values.

Three tools are used in the physical-design stage. First, the Automatic Device Generator, or Autogen, lays out the "correct-by-construction" device—a device that meets all of the electrical ground rules, such as minimum spaces between devices or minimum sizes for isolation. The second tool is the Automatic Preplacement tool, which preplaces the devices as they appear on the schematic *(Fig. 2)*. Because this may not be the optimal layout as far as thermal or parasitic effects are concerned, alternate layouts can be attempted. In this case, some interactive layout tools can be used to assist designers, such as the Graphics Editor.

Certain features of the system are included to make it as error-free as possible. The system prompts designers to enter a needed parameter when it's required. By using multiple windows, designers can simultaneously view the circuit schematic, the physical layout, and a frequency response. Plots, histograms, and scatter plots can be created on-screen or sent to a plotter at different points in the design process.

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CIRCLE 59

After the placement is set, the routing is done manually using the third tool—the Graphics Editor. Routing is aided by highlighting the nodes to be connected, and further simplified by generating hierarchical symbols and multiple windows. During this process, any device modification is automatically back-annotated into the original schematic.

The final step is the physical-design verification, which also involves three tools. The Design Rules Check verifies the adherence of over 900 process and assembly ground-rule checks *(Fig. 3)*. This check can be run in either a batch or interactive mode and can encompass either the entire circuit or a specified area.

The Layout Versus Schematic tool ensures that the electrical net list conforms to the extraction from the physical layout. The Layout Parasitic Extractor tool draws out any non-negligible parasitic capacitance or resistance from the interconnects and back-annotates the parasitics into the circuit file for resimulation.

The analog processes take advantage of dielectric isolation (DI) which eliminates parasitics that cause latchup or a reduction in speed. In addition, leakage currents become negligible even at high temperatures. These factors also make circuit simulations more accurate.

With the DI process, vertical pnp transistors can react almost as quickly as the npns. In other words, the pnps can be used in the same signal path as the npns. Previously, designers had to pull out their bag of tricks to find a way to achieve the same result without using the pnps. Furthermore, the DI process supports JFETs and laser-trimmable Nichrome thin-film resistors. There are two complementary DI processes, one for high frequency, and one for very-high frequency (VHF). The high-frequency process is 40 V compared to the VHF's 20 V. An npn VHF transistor has an f_T of 1.2 GHz, while a pnp transistor from the same process has an f_T of 1.0 MHz.□

PRICE AND AVAILABILITY

The Fastrack system is currently available on Sun 3 and Sun 4 workstations. Volume shipments will begin in the fourth quarter of this year. The Fastrack starts at \$20,000 for the digital front-end tools; complete analog systems sell for \$100,000.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; (407) 724-3739. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	562
MODERATELY	563
SLIGHTLY	564

PARALLELISM INCREASES PROCESSOR SPEED

PARALLEL INSTRUCTION DECODING AND MULTIPLE EXECUTION UNITS PERFORM UP TO THREE MULTIPLE INSTRUCTIONS PER CYCLE TO YIELD 66 MIPS.

LISA GUNN

Generating higher speeds for processors is getting harder as conventional architectures and process technologies are pushed to the limit. But designers at Intel Corp. tackled this formidable task by incorporating parallelism—a technique that executes several instructions at once—into the newest member of their 80960 family of embedded processors, the i960CA. The inclusion of parallelism into the i960CA boosts performance three to five times while the processor remains software compatible.

The i960CA, a 32-bit reduced-instruction-set computer (RISC) processor optimized for data control, consists of numerous peripheral support functions built around the C-series core. Intel is also offering many i960CA support products *(see "In support of a fast processor," p. 122)*.

The C-series core implements the 80960 core RISC architecture, which is optimized for embedded-control applications. The core executes a sustained speed of 66 native MIPS, a speed that it owes to several innovative features that work together to issue and execute instructions in parallel *(see the figure)*. These features include parallel instruction decoding, which can initiate two to three instructions in every clock cycle. Multiple, independent execution units perform overlapped instructions, and a multiport register file enables multiple registers to be accessed simultaneously. Register and resource scoreboarding manage the parallel execution, while a branch look-ahead feature makes it possible for branches to execute in parallel with other instructions. Other factors contributing to the chip's high speed are the 33-MHz internal clock, the on-chip register cache, wide internal buses, the efficient instruction pipeline, and the numerous single-cycle instructions.

At 66 native MIPS, Intel claims that this device is the fastest embedded controller and the fastest microprocessor on the market today. Moreover, Intel says that the i960CA has the highest degree of parallelism of any single-chip integer device. Applications that can benefit from the processor's extremely fast data-handling ability include communications systems, such as network controllers and file servers, and office equipment, such as laser printers and scanners.

PARALLEL DECODING

Parallel instruction decoding is done by the instruction sequencer, which also handles prefetching and issuing instructions in parallel. The instruction decoder's task is simplified because of the machine-level instruction format. The instruction decoder basically supplies the pipe sequencer with enough instructions to maximize performance.

The parallel instruction sequencer fetches from the internal cache microcoded ROM and the queue. It also manages the instruction-prefetch requests. The pipe sequencer examines up to four instructions each clock cycle, and performs parallel decoding of up to three of them.

The pipe sequencer manages the parallel instruction flow and the parallel issuing of instructions; the core maintains three parallel pipelines. Parallel instructions are issued to the register (REG), memory (MEM), or control (CTRL) portions of the architecture. The pipelines can maintain two instructions per clock cycle at sustained execution.

The branch and condition branch instructions are executed by the instruction sequencer. Parallel branching, or branch look-ahead, is a pipe sequencer feature that attempts to execute a parallel branch before the branch condition is stable. If the attempt fails, the processor has time to abort the branch and redirect program flow. This redirection takes one to two clock cycles once the new target is cached.

The execute stage of the pipeline is handled by the execution units. Instruction execution typically takes only one clock cycle. However, some instructions, such as multiply, take multiple clock cycles.

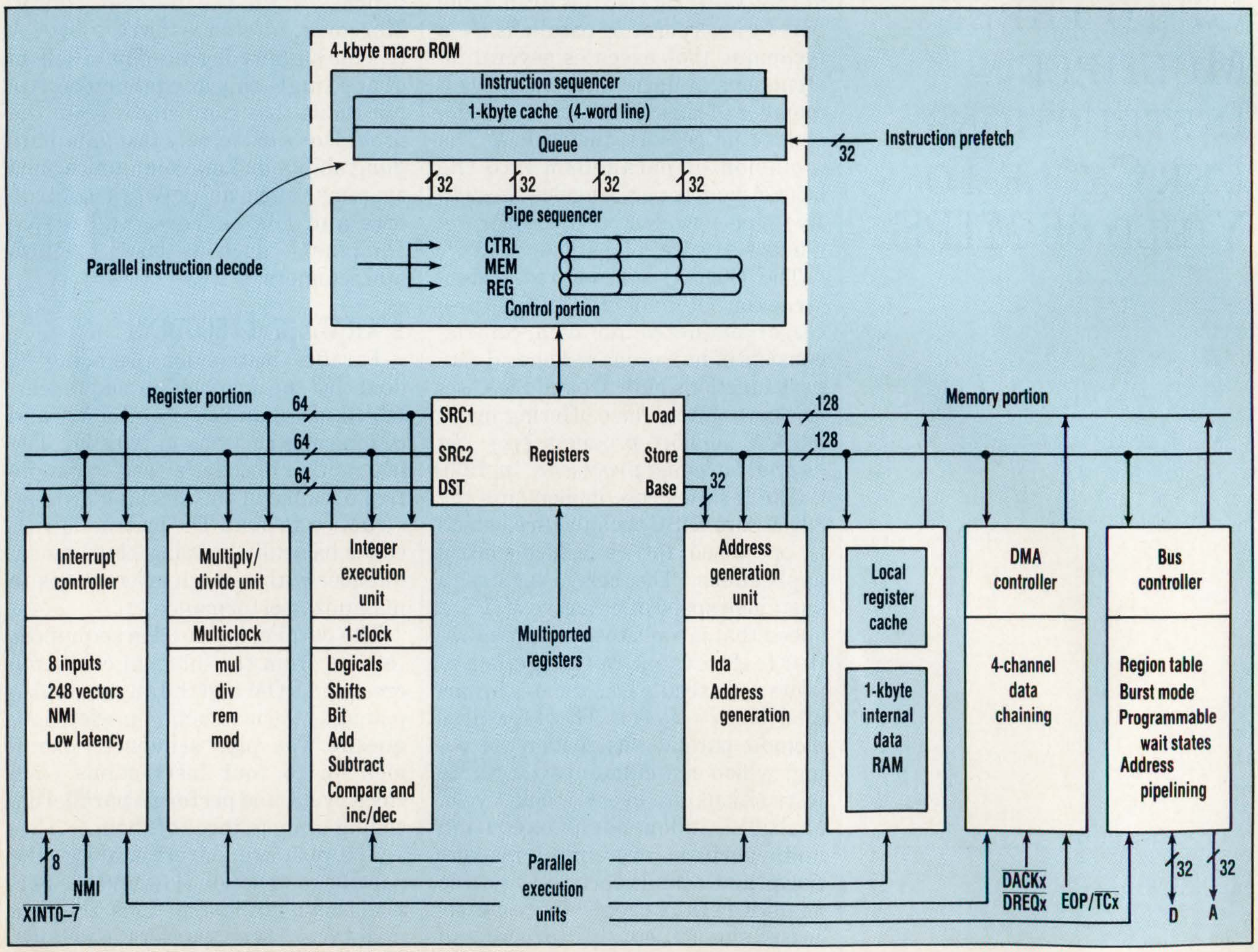
All execution units operate in parallel. The multiply and divide unit, the address-generation unit, and the integer-execution unit make up the CPU core architecture. Execution units unique to the i960CA include the interrupt controller, bus controller, and DMA controller.

The register file and the wide data paths between the register file and the execution units reduce many potential internal bottlenecks. With the 128-bit internal buses, it's possible to move the contents of four 32-bit registers in one clock cycle.

Resource scoreboarding manages instructions that are issued to the execution units. An internal instruction cache decouples the instruction stream from the external bus, which minimizes the external-bus bottlenecks. The two-way set-associative cache has a 1-kbyte by 4-word line size. Loops in the cache can execute at a sustained rate of two instructions per clock.

Another part of the i960CA implementation is a six-port register file that eliminates contention for register-set access by the independent execution units. One REG-format, one MEM-format, and one address-calculation instruction can read register operands simultaneously. Results from a REG and MEM coprocessor can be written to the register file concurrently.

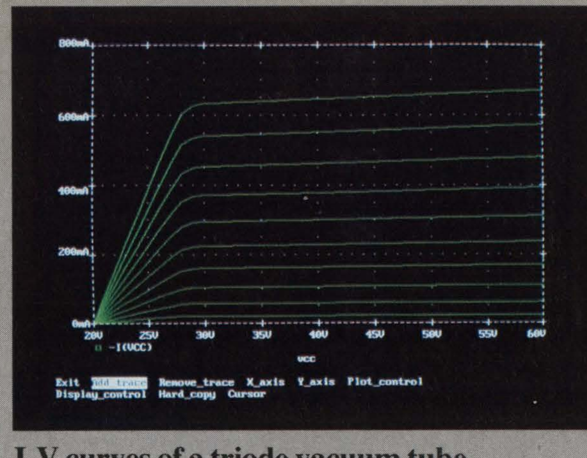
The local register cache and data RAM are located internally on the processor's MEM-bus portion. These two units are actually part of the same on-chip memory array. The local register cache supports fast calls and returns for context switching.



PARALLEL INSTRUCTION EXECUTION gives the i960CA processor its high speed of 66 MIPS. Divided into three portions, the chip is made of a C-series core in addition to interrupt-, DMA-, and bus-controller units.

PSpice

The Standard for Circuit Simulation



I-V curves of a triode vacuum tube

Analog Behavioral Modeling

The Analog Behavioral Modeling option for PSpice allows one to describe analog components, or entire circuit blocks, using a formula or a look-up table. For linear blocks, the description can be either a Laplace transform or a table of frequency response. Once defined, PSpice can simulate circuits including such blocks.

The ability to model entire blocks of circuitry is a powerful aid in designing a system from the top down. A functional block can be described by its behavior without worrying about how that function will be implemented. Later, the block can be replaced by the actual circuitry.

Another application is the modeling of electronic components which are not built into PSpice. The photo above shows an example of simulating the DC characteristics of a 3/2-power-law device.

Since its introduction over five years ago, MicroSim's PSpice has more copies sold than all other commercial Spice programs combined. Here are some of the features which have made PSpice so popular:

- Standard parts libraries of over 2200 analog models: diodes, bipolar transistors, small-signal JFET's, power MOSFET's, opamps, voltage comparators, transformer cores, and opto-couplers.
- GaAs MESFET devices, BSIM MOS model.
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

Besides Analog Behavioral Modeling, these other PSpice options are also available:

- **Digital Simulation**, which allows one to simulate mixed analog/digital circuits with feedback between the analog and digital sections.
- **Monte Carlo** analysis to calculate the effect of parameter tolerances on circuit performance. This includes statistical, sensitivity, and worst case analyses.
- **The Probe** "software oscilloscope" provides an interactive viewing environment for simulation results (see photo above).
- **The Parts** parameter extraction program, allowing one to extract a device's model parameters from data sheet information.

PSpice is available on these computers:

- The PC family, including the PS/2, running DOS, Protected Mode DOS, or OS/2.
- The Macintosh II.
- The Sun 3, Sun 4, and SPARCstation families.
- The Apollo DN3000 and DN4000 workstations.
- The VAX/VMS family, including the MicroVAX.

Each copy of PSpice comes with our extensive product support. Our technical staff has over 100 years of experience in CAD/CAE and our software is supported by the engineers who wrote it. With PSpice, expert assistance is only a phone call away.

For our free information packet, including a PSpice demo diskette, call us **toll free** at (800) 826-8603 or, in California, (714) 770-3022. Find out for yourself why PSpice is the standard in circuit simulation.

MicroSim Corporation **20 Fairbanks • Irvine, CA 92718 USA • Telex 265154 SPICE UR**

CIRCLE 61

EMBEDDED PROCESSOR

IN SUPPORT OF A FAST PROCESSOR

It's not enough to offer fast silicon these days: Customers also need support products in the form of development tools and external hardware. Intel Corp. addresses this need with a collection of products designed with the i960CA embedded RISC processor.

Development tools are important for getting maximum performance from an embedded processor. Intel's suite of development tools, for use in 80960-based systems design, include an in-circuit emulator, a system generator to set up data structures, and a software-execution vehicle for architecture evaluation and running a benchmark. Also included is a software debugger, a simulator, a macro assembler, and a C compiler. All the tools run on DOS-based PC/AT systems, and some also operate with VAX, MicroVAX, and Sun-3 systems.

Intel also offers hardware designed specifically for 80960-based designs. Though EPROMS generally can't keep up with 32-bit speed, a new 1-Mbit EPROM utilizes a burst interface to give near zero-wait-state operation. The 27960 EPROM device supports the specific requirements of the 80960 processor family. A 85C960 function-specific programmable-logic device (PLD) is also being introduced. The burst-mode memory PLD supplies address decoding and wait-state and ready generation.

Moreover, some of Intel's previously announced products support 80960-based designs. Its 85C508 PLD is a programmable address decoder with an on-board latch. With a maximum delay time of 7.5 ns, the PLD speeds the microprocessor-to-memory interface. The 82596 family of 32-bit local-area-network coprocessors operates independently of the i960CA system processor, which frees the system bus. The coprocessor transmits data at 100% of both the system- and serial-bus bandwidths.

The entire local register set is saved or restored in only four clock cycles. The on-chip RAM is available for frequently-accessed program data.

Exclusive features of the i960CA processor are the multimode bus, internal DMA, and interrupt controllers. The bus controller reads at 132 Mbytes/s and writes at 106 Mbytes/s. The processor has demultiplexed, 32-bit address and data buses. Loads, stores, and instruction fetches are queued by the bus controller.

The DMA controller is tightly coupled to the core. DMA transfers execute simultaneously with users' programs because core resources are shared between the program and the DMA operation. Quad-transfer modes can exploit the processor's burst mode.

Up to 248 interrupts from external sources are handled by the interrupt controller. It boasts a typical latency of less than 750 ns, an average time for a high-end RISC processor. The interrupt unit, a REG coprocessor, performs hardware-interrupt detection and priority mapping independently of the core.☐

PRICE AND AVAILABILITY

Samples of the i960CA embedded processor are available, with volume production scheduled for the fourth quarter of this year. The chip comes packaged in a 168-lead ceramic pin-grid array. In quantities of 1000, the 16-, 25-, and 33-MHz versions of the processor cost $273, $303, and $379, respectively.

Intel Corp., 5000 W. Chandler Blvd., Chandler, AZ 85226; (602) 554-8051. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

INTERNAL MASS STORAGE ENHANCES FAST DIGITAL SCOPE

JOHN NOVELLINO

As signal-analysis tasks grow in complexity, personal computers become an important adjunct to the oscilloscope. Recognizing this synergy, LeCroy Corp. designed the 7200 Precision Digital Oscilloscope not only as a high-performance scope, but also to be easy to use and program with PCs.

With a 1-GHz sampling rate, 400-MHz bandwidth, and 50-ksample acquisition memory, the model 7200 ranks high among digital scopes. The instrument accepts two model 7242 plug-in units, which contain the digitizing circuitry. Each plug-in offers the full 1-GHz, 8-bit-resolution sampling rate on two channels. As a result, the user can upgrade from two to four channels without losing performance. The large waveform memory lets users maintain the scope's maximum digitizing rate on slower timebase settings.

Additionally, the 7200 contains a 3.5-in. floppy drive and a hard disk. This internal mass-storage capability makes the scope easier to use. The MS-DOS floppy drive eliminates the need for GPIB programming and special instrument drivers to transfer data to a PC for analysis. Also, because front-panel settings can be stored on floppy disks, operators can maintain a file of frequently used set-ups.

On the hard disk, users store waveforms and front-panel set-ups. An on-line help manual and the 7200-series programs and operating system are also stored there. The hard disk is activated by the scope's Record Trace mode, which time-stamps each new screen of waveforms and stores it in a 2-Msample buffer.

The buffer holds any combination of waveforms adding up to 2 Msamples—for example, 1000 waveforms with 2000 points each. Storing the unit's operating system on the hard disk means that upgrades in module technology can be handled through the floppy disk rather than firmware changes.

The 7200 does have GPIB and RS-232-C ports, however, and users can program the instrument through them. Bus commands can set up the unit, control its cursors, and read out data. The scope transfers waveform data blocks at up to 600 kbytes/s over the GPIB.

TRIGGER CAPABILITIES

LeCroy's Smart Trigger capability includes edge, logic, glitch, interval, and tv triggering, singly or in combination. For example, a user can capture a particular data or address condition in a microprocessor-based system by setting logic-threshold levels for the inputs and logic conditions to trigger on. Pulse-width triggering lets users find a dropout glitch in a clock signal or a missing bit during a disk-drive read. The scope will even wait for a specified number of events before triggering.

Up to eight waveforms can be displayed at once, and the scope can perform more than 20 mathematical functions on all displayed signals simultaneously. Or, the analysis functions can be chained so that 16 cascaded calculations can be made on one signal. To speed calculations and maintain near-real-time updates, both the mainframe and plug-in module contain microprocessors.

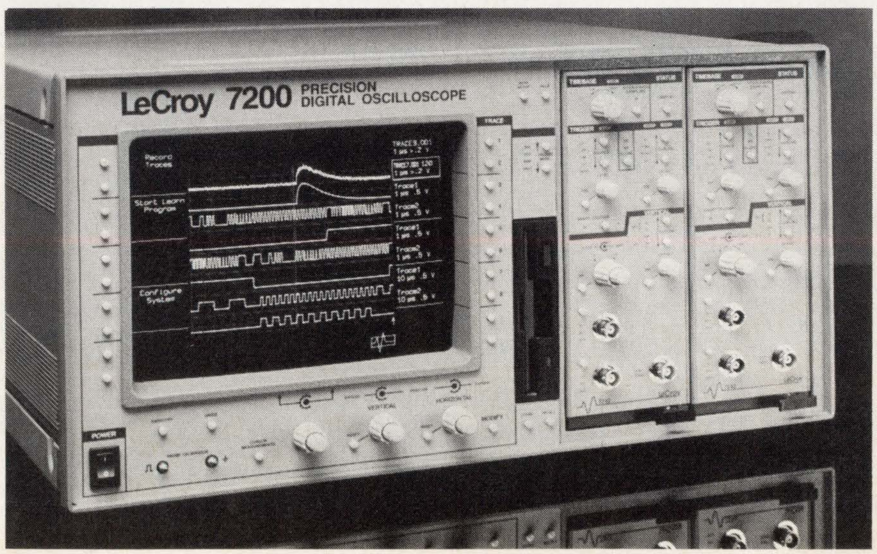
Time-domain functions include automatic readout and statistical analysis of more than 40 pulse characteristics, X-Y plots, waveform math, and signal averaging. On single waveforms, the scope determines absolute value, square, square root, log, antilog, integral, derivative, 1/X, smoothing, averaging, and maximum/minimum. Multiple-waveform math includes sum, difference, multiply, and divide. The user can select the scientific units and define labels so the readouts are in the desired format.

In the frequency domain, the 7200 can calculate 100- to 50,000-point fast-Fourier transforms and inverse FFTs. Displays include phase, magnitude, power spectrum, cross spectrum, and other functions. The amplitude, frequency, and phase of the fundamental and harmonics are automatically read out.

The 7200 oscilloscope mainframe costs $16,000, and the 7242 two-channel digitizing plug-in costs $16,900. Delivery is in eight to 10 weeks after receipt of order.

LeCroy Corp., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (800) 553-2769.

CIRCLE 311



MIXED-SIGNAL VERIFICATION SYSTEM BOASTS APPLICATIONS FLEXIBILITY

Featuring a low-noise system for distribution of analog signals, the Logic Master XL Mixed-Signal Verification System from Integrated Measurement Systems has the flexibility to perform prototype verification, device characterization, and even low-volume production testing. In addition to 176 digital-I/O channels operating at 60 or 100 MHz, the system includes 16 analog-I/O channels.

The distribution system's low-noise environment smooths out the signal noise and crosstalk problems inherent in mixed-signal ICs. The tester also has a mixed-signal switching matrix and mixed-signal fixturing that isolates analog and digital signals at the device under test to eliminate distortion. As a result, users can connect GPIB analog instruments to the fixturing to create a customized test set.

Designers can develop and execute tests interactively using the windowing environment. The interactive capability is helpful for making critical measurements during prototype verification. But the system can also execute automatic tests when the designer wants to collect data on a large sampling of devices during characterization or low-volume production testing.

Prices for the Logic Master XL Mixed-Signal Verification System start at $120,000, depending on configuration. Upgrades for existing Logic Master XL systems start at $60,000.

Integrated Measurement Systems Inc., 9525 SW Gemini Dr., Beaverton, OR 97005; (503) 626-7117. **CIRCLE 312**

JOHN NOVELLINO

64-PIN PRODUCTION TESTER FEATURES BIG-SYSTEM PERFORMANCE

Although most ICs being developed these days have relatively low pin counts, many are taking advantage of the new fast device technologies. Designers who must test these fast ICs no longer need to use large, expensive VLSI testers just to get the needed speed. For such applications, Tektronix' Semiconductor Test Systems Division has introduced the LT-1201.

The LT-1201 can be configured with two 64-pin test heads, each capable of multisite (parallel) testing. With this scheme, the system can work with dual or quad handlers for high-volume production testing. Retaining the performance of Tektronix' 256-pin LT-1001, the smaller unit handles 100-MHz test speeds, creates 16 timing sets, and has an operating voltage range of –2.5 to +7.5 V. Throughput is enhanced by the inclusion of one parametric measurement unit for each eight I/O pins.

With its 100-MHz speed, the LT-1201 can test advanced CMOS logic and CMOS TTL-compatible ICs, as well as fast TTL and ECL logic families. The unit's 290-ps edge-placement accuracy allows tighter guard bands for increased yields.

Critical to the system's performance and reliability is its second-generation IC pin electronics. Three VLSI ASICs house the system's drivers, timing generators, active loads, front-end pin support circuitry, and analog- and digital-comparator circuitry. The result is a dramatically lower parts count for each pin card, which in turn lowers the test head's operating temperatures and minimizes thermal drift.

The LT-1201 starts at $290,000 for a 32-pin system capable of testing two devices simultaneously. A typical 64-pin, one-head system costs $370,000.

Tektronix Inc., Semiconductor Test Systems, P.O. Box 4600, MS-94-441, Beaverton, OR 97076; Alan Whiteside, (503) 629-1035.

CIRCLE 313

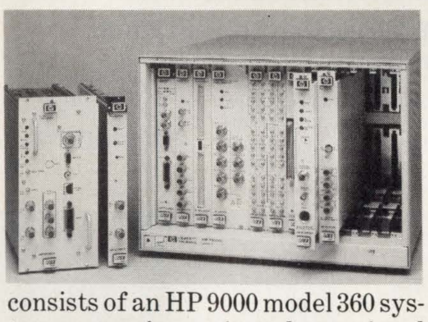
JOHN NOVELLINO

B- AND C-SIZE MODULES GIVE VXIBUS LINE PERFORMANCE FLEXIBILITY

A line of VXIbus products from Hewlett-Packard includes both B- and C-size modules, affording users a wide performance range. The HP 75000 family contains mainframes and controllers in both sizes, as well as instrument and switching modules.

The products are part of HP's measurement-system architecture, which includes software-development tools, controllers, HP-IB (GPIB) instruments, and the VXIbus, as well as modular measurement-system products that connect to a user's device under test. As part of this architecture, the HP 75000 series products share a common user interface, HP's interactive test generator, and a common command set, the HP test-systems language.

Modules available include digital multimeters, counters, a function generator, a power meter, multiplexers, a digital-to-analog converter, a 16-channel form-C switch, and a 4-by-4 relay matrix. A C-size controller



consists of an HP 9000 model 360 system-processing unit and associated I/O interfaces. The B-size mainframe contains a Motorola 68000-based controller that handles VXI slot-0 and resource-manager duties.

Most HP 75000 Series B and Series C products can be ordered now with an estimated delivery of eight to 15 weeks after receipt of order. The HP E1416A power meter, HP E1440A function/sweep generator, and HP E1480A V/360 controller will be available for order December 1.

Hewlett-Packard Co., 1920 Embarcadero Rd., Palo Alto, CA 94303; (800) 752-0900. **CIRCLE 314**

JOHN NOVELLINO

PROGRAMMABLE POWER SUPPLIES' TIMING MODE EASES STRESS-TESTING TASKS

Designed mainly for ATE users, the PPS series of programmable power supplies features an internal-timer program that eases stress-analysis testing, component testing, and evaluation of modules such as voltage-controlled oscillators. In addition, GPIB capability is built into each model.

Both research and development and bench-top applications benefit from the PPS supplies' versatility. The units offer full rated power from 100 to 1000 W for a wide range of test capabilities. Their modes of operation include ΔV, ΔT, and manual.

An important feature of the units is the ability to use their internal memory to store up to 200 preprogrammed voltage and current levels. These can then be stepped through

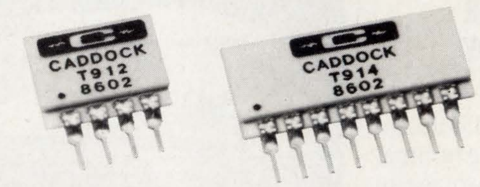
automatically without need for an external computer or controller. For instance, the supply can be programmed, for specified intervals, to deliver 24 V dc at 1 A, then go to 26.4 V dc (+10%) at 1 A, return to 24 V, switch to 21.6 V dc (–10%), and return again to 24 V.

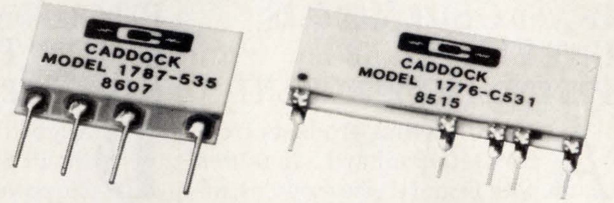
The PPS series programmable power supplies start at $995. Delivery is from stock.

Beckman Industrial Corp., 3883 Ruffin Rd., San Diego, CA 92123-1898; (619) 495-3200. **CIRCLE 315**

DAVID MALINIAK

CADDOCK's Precision and Ultra-Precision Resistor Networks provide a designer's choice of performance that will optimize solutions in precision analog circuit designs.





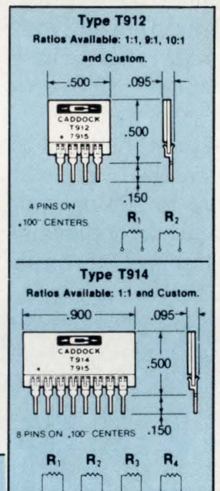
Precision and Ultra-Precision Resistor 'Pairs' and 'Quads' deliver a selection of Ratio Tolerance to as tight as ±0.01% and Ratio Temperature Coefficient to 2 PPM/°C combined with exceptional long-term stability.

Standard Type T912 and T914 Precision and Ultra-Precision Resistor Networks.

Standard models of the Type T912/T914 Precision and Ultra-Precision Resistor Networks combine all of these performance characteristics:

- **Absolute Tolerance:** 0.1% for all resistors.
- **Ratio Tolerances:** 0.1%, 0.05%, 0.02% and 0.01%
- **Ratio Temperature Coefficients:** from 10 PPM/°C to 2 PPM/°C.
- **Absolute Temperature Coefficient:** 25 PPM/°C from 0°C to +70°C.
- **Ratio Stability of Resistance at Full Load for 2000 Hours:** within 0.01%.
- **Shelf Life Stability of Ratio for Six Months:** within 0.005%.

The standard part number below provides a selection of over 500 in-production models of Type T912/T914 precision and ultra-precision 'pairs' and 'quads':



T912 - A 10K - 010 - 10

Model Number:

Ratio Code Letter:
A - T912 with $R_1 = 10R_2$ (Example: 1K - 10K)
B - T912 with $R_1 = 9R_2$ (Example: 1K - 9K)
No Letter - T912 with $R_1 = R_2$
No Letter - T914 with $R_1 = R_2 = R_3 = R_4$

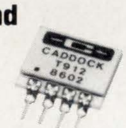
Standard Resistance Values (R_2):

1K	10K	40K	200K	500K
2K	20K	50K	250K	1 Meg.
5K	25K	100K	400K	

Ratio Tolerance:
-100 = 0.1% -020 = 0.02%
-050 = 0.05% -010 = 0.01%

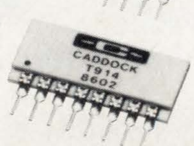
Ratio Temperature Track: (0°C to +70°C)
-10 = 10PPM/°C -05 = 5PPM/°C
-02 = 2PPM/°C

Custom Type T912 and T914 Precision and Ultra-Precision Resistor Networks.



Custom models of these precision 'pairs' and 'quads' can include these special performance features:

- **Resistance Values:** from 1K to 2 Megohms with maximum ratios of 250-to-1.
- **Absolute TC:** as low as 15 PPM/°C.
- **Ratio TC:** as low as 2 PPM/°C.



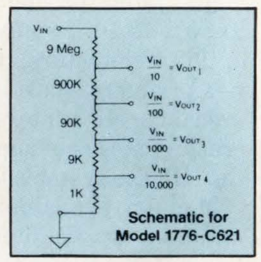
- **For Type T912/T914 data, circle Number 201.**

Precision Decade Resistor Voltage Dividers and Current Shunt Resistor Networks deliver many optimum combinations of precision and temperature coefficient performance for high accuracy range-switching circuitry.

Standard Type 1776 Precision Decade Resistor Voltage Divider Networks.

The Type 1776 Precision Decade Resistor Voltage Dividers provide a family of networks that includes 3, 4 and 5-decade voltage dividers with ratios from 10:1 to 10,000:1. Standard performance includes a wide range of specifications in particular combinations that meet the most often requested requirements.

- **Absolute Tolerances:** from 0.25% to 0.1%.
- **Ratio Tolerances:** 0.25%, 0.1% or 0.05%.
- **Absolute TC:** from 50 PPM/°C to 25 PPM/°C.
- **Ratio TC:** from 50 PPM/°C to 5 PPM/°C.
- **Voltage Coefficient:** As low as 0.02 PPM/Volt.

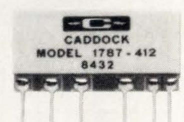


Schematic for Model 1776-C621

With 36 standard models to choose from, each circuit designer can specify the exact levels of performance required by each application.

- **For Type 1776 data, circle Number 202.**

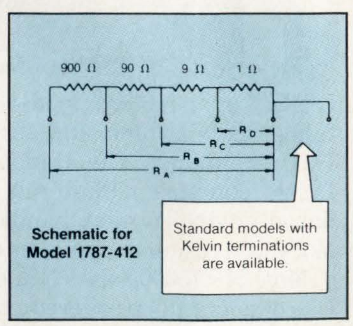
Standard Type 1787 Precision Current Shunt Resistor Networks.



The Type 1787 Current Shunt Resistor Networks achieve the combination of performance requirements necessary to meet the demands of precision current measurement circuits, including laboratory and bench-type instrumentation:

- **Resistance Values:** 1 ohm, 10 ohms, 100 ohms and 1000 ohms.
- **Absolute Tolerances:** 0.25%, 0.1% or 0.05%.
- **Absolute TCs:** 100 PPM/°C, 80 PPM/°C or 50 PPM/°C.

There are now 12 standard models of the Type 1787 Current Shunt Resistor Networks available for 3 and 4-decade applications, and prototype quantities of many models are normally available from factory stock.



Schematic for Model 1787-412

- **For Type 1787 data, circle Number 203.**

Caddock's new 28-page General Catalog describes over 200 models of both standard and custom precision and ultra-precision resistors and resistor networks. For your personal copy, call or write our main offices at -

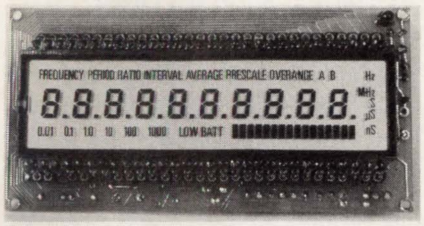
Caddock Electronics, Inc., 1717 Chicago Avenue, Riverside, California 92507 • Phone (714) 788-1700 • TWX: 910-332-6108

CADDOCK

HIGH PERFORMANCE FILM RESISTORS

CIRCLE 80

COUNTER MODULE SPANS 0.1 HZ TO 150 MHZ



A 10-digit universal counter-timer in a digital panel-meter configuration offersperformance equivalent to that of a laboratory counter. The UTC 150 has a direct frequency response from 0.1 Hz to over 150 MHz with up to 9 digits of resolution per second. Its dimensions of just 1.8 by 3.55 by 0.6 in. make it suitable for use in custom instrumentation, as well as digital panel meters. The unit offers such measurement functions as frequency, period, period average, time interval, time interval average, ratio, prescale, overrange. It also features a 16-segment bar graph and a high-accuracy (1-ppm) 10-MHz crystal time base with a calibration adjustment trimmer. In single quantities, the UTC 150 sells for $225; $149 in hundreds.

Optoelectronics Inc., 5821 N.E. 14th Ave., Fort Lauderdale, FL 33334; (800) 327-5912 or (305) 771-2050. **CIRCLE 332**

CLIPS PERMIT TESTS ON SOLDERED PLCCS

With the Adapt-A-Clip line of test accessories, users can run emulation and test programs on soldered PLCC devices. The adapters clip onto the outside of the soldered PLCC and present the emulator or testing device with alternate pinouts, such as as PGA, DIP, LCC, and others, for easy insertion of male emulator pods. The device-specific clips can be manufactured to adapt to any of the popular PLCCs currently available. They can also be custom ordered to transform one device into another by permitting different pinout configurations.

Emulation Technology, 2368B Walsh Ave., Bldg. D, Santa Clara, CA 95051; (408) 982-0660. **CIRCLE 361**

UNIT DETECTS AC WITHOUT CONTACT

Nonintrusive testing for the presence of 110 to 480 V ac is performed by a pocket-sized instrument called the Volt Stick. The unit distinguishes between live and neutral wires without having to contact the wire or its insulation. It operates by detecting the electric-field created by the 60-Hz cycle in alternating current. The instrument can detect single- and three-phase circuitry, as well as return loops. When the tip of the Volt Stick is within 1/8 in. of the wire insulation, it glows brightly indicating the presence of voltage. Current flow isn't needed for operation. The device costs $24.98.

MBD International Inc., P.O. Box 870596, Dallas, TX 75287; (214) 250-6424. **CIRCLE 333**

PATTERN GENERATOR COVERS MANY STANDARDS

In addition to color pattern-generation capabilities that meet TV standards worldwide, the PM 5518 TXI offers full remote control via an IEEE-488 interface. It supports such standards as NTSC, PAL, and SECAM, as well as PAL N and M standards used in South America. What's more, the instrument permits simple user selection among standards. Over 70 test patterns and carrier frequencies between 32 and 900 MHz can be selected by direct entry on a numeric keyboard or over the 488 bus. Special test patterns are available to meet the changing requirements of NTSC and PAL, including a 250-kHz multiburst and a demodulator pattern. The PM 5518 TXI pattern generator sells for $5150 and has an eight-week delivery time.

John Fluke Manufacturing Co. Inc., P.O. Box C-9090, Everett, WA 98206; (800) 443-5853. **CIRCLE 334**

RISC-BASED WORKSTATIONS AND SERVERS SET NEW PRICE-PERFORMANCE LEVELS

In the scramble to deliver the best performance for the lowest price, the DECstation 2100 workstation and the DECsystem 5400 and 5800 represent Digital Equipment Corp.'s latest effort. The machines deliver from 10.4 to 36 MIPS, thanks to CPUs based on the R2000 and R3000 processors from Mips Computer Systems Inc.

The workstation delivers the 10.4 MIPS of integer throughput and 2.7 MFLOPS of floating-point computer power while running the R2000 chip set at 12.5 MHz. At $7950 for a monochrome system, the DECstation 2100 represents the lowest-priced RISC-based Unix workstation.

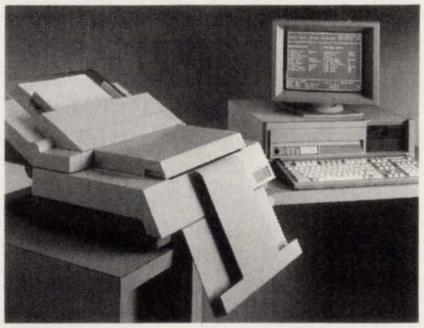
The basic workstation configuration includes 8 Mbytes of RAM and a video subsystem that displays 1024 by 864 pixels (monochrome or eight color planes) on a 15- or 19-in. monitor. The system's SCSI port accepts up to seven SCSI-compatible peripherals. Optional SCSI peripherals from DEC include 332- or 104-Mbyte disk drives (the RZ55 or RZ23), a 95-Mbyte SCSI tape drive (TZK50), and a 600-Mbyte CD ROM drive. Both thick and thin Ethernet ports are included as are serial and parallel ports, a keyboard, and a mouse.

The more general-purpose DECsystem 5400 incorporates the DEC Q-bus interface for peripheral and I/O expansion and the higher-performance R3000 chip set. The system delivers 16.6 MIPS and has a starting price of $49,900. DEC's top-of-the-line RISC-based system, the 5800 series computers, are powered by the R3000 CPU. These come in either a single- or dual-processor configuration, and are dubbed the 5810 and 5820, respectively. The 5810 cranks out 18.7 MIPS of computing power, while the 5820 ups the ante to 36 MIPS. These systems start at about $100,000.

Digital Equipment Corp., Four Results Way, Box 1022, Marlborough, MA 01752-9122; (508) 467-5111. **CIRCLE 316**

DAVE BURSKY

HIGH-VOLUME TEXT AND GRAPHICS SCANNER CONVERTS FILES TO CALS STANDARD



Thousands of type styles and sizes can be read by Xerox Imaging Systems' top-of-the-line Kurzweil K-5100 scanning system. The K-5100 heavy-duty scanner and 50-page automatic document feeder work with a PC/XT/AT or compatible in high-volume text and graphics scanning applications. In addition, a bundled system with special application software converts scanned documents to the Federal computer-aided acquisition and logistics support (CALS) standard output.

The K-5100 system uses Kurzweil's artificial-intelligence-based intelligent character recognition. It can read text created by typesetters, laser printers, typewriters, photocopiers, fine-line fonts, and draft-quality dot-matrix printers. Using the system's interactive text-verification feature, the user helps the system learn to recognize special symbols, and difficult characters found in poorer-quality documents. The learned characters can be stored and recalled as needed to expedite future recognition sessions.

The system features recognition spooling, which means that documents can be scanned as images and recognized for text at a later time.

The K-5100 scanning system is available now at a price of $17,950. An 5100 upgrade kit for K-5000 systems costs $3000. The K-5100 CALS-conversion system is also shipping now for $22,950.

Xerox Imaging Systems Inc., 1215 Terra Bella Ave., Mountain View, CA 94043; (415) 965-7900. **CIRCLE 317**

LISA GUNN

SECURE COMPUTERS OPTIMIZED FOR NETWORK APPLICATIONS

Extra security and remote-management capabilities are featured in the WGS series, an extension to AT&T's 6386 family of 80386-based computer systems. The machines gain their remote capabilities running under Unix System V/386 release 3.2.2 for distributed networking applications. All are PC-AT-bus compatible and run MS-DOS, OS/2 or Unix operating systems. Additionally, the systems support AT&T's Simul-task 386 software as well as the X-window and Microsoft Windows/386 utilities.

Besides the usual keyboard lockswitch, all of the systems have a software-based password-protection scheme to keep unauthorized users out of the system or network. The server models also have a lockable cover that secures the openings for removable media (floppy disks or tape).

The low-end 6386/SX WGS base machine comes with the 80386SX processor and 2 Mbytes of RAM on the motherboard (expandable to 8 Mbytes). All other peripheral support is found on the motherboard as well. This includes super-VGA video (800 by 600 pixels, 16 colors) and floppy-disk controllers, real-time clock, controllers for the 101-key keyboard and a mouse, hard-disk drive interface, two serial ports, and one parallel port. The higher-performance 6386/25 uses the 32-bit 80386DX, doubles the RAM to 4 Mbytes, and adds a 64-kbyte cache.

At the top of the line is the 6386E/33, an ESDI-based floor-standing system, and the 6386E/33 Model S, an SCSI-based version of the same system. Running at 33 MHz, they come with either a 135- or 300-Mbyte ESDI or SCSI disk drive and 125-Mbyte tape drive as standard equipment. Prices start at $2995 for the 6386/SX WGS and surpass $15,000 for the 6386E/33 systems.

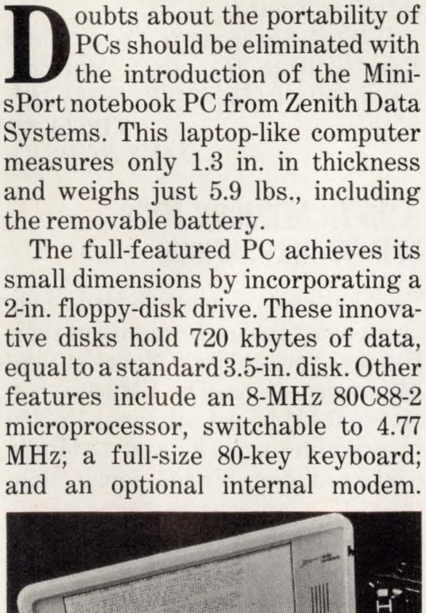
AT&T Computer Systems, 1 Speedwell Ave., Morristown, NJ 07960; (800) 247-1212. **CIRCLE 318**

DAVE BURSKY

NOTEBOOK PC IS JUST OVER 1 IN. THICK AND WEIGHS UNDER 6 LBS.

Doubts about the portability of PCs should be eliminated with the introduction of the MinisPort notebook PC from Zenith Data Systems. This laptop-like computer measures only 1.3 in. in thickness and weighs just 5.9 lbs., including the removable battery.

The full-featured PC achieves its small dimensions by incorporating a 2-in. floppy-disk drive. These innovative disks hold 720 kbytes of data, equal to a standard 3.5-in. disk. Other features include an 8-MHz 80C88-2 microprocessor, switchable to 4.77 MHz; a full-size 80-key keyboard; and an optional internal modem.



Also, MS-DOS 3.3 is permanently stored in the system's 832 kbytes of ROM.

The MinisPort contains a silicon disk that can store and retrieve data much faster than a standard hard disk. This disk can be expanded up from 360 kbytes to 1.36 Mbytes with an optional upgrade package.

A 25-line-by-80-character DayBright liquid-crystal screen combines the technologies of transmissive-backlit displays with reflective displays. The 9-1/2-in.-diagonal screen is illuminated by ambient light in normal lighting conditions and by an adjustable electroluminescent backlight in a dark or dimly-lit setting.

MinisPort's nickel-cadmium battery can operate for a minimum of three hours and recharges in four to six hours. The computer comes with serial and parallel ports in addition to an external floppy-drive and an external color-monitor port.

Two versions are available. Model 1 contains 1 Mbyte of RAM and sells for $1999 while Model 2 contains 2 Mbytes of RAM and costs $2299. This version also contains the upgraded silicon disk. The optional modem costs $199.

Zenith Data Systems, 1000 Milwaukee Ave., Glenview, IL 60025; (800) 553-0331. **CIRCLE 319**

RICHARD NASS

PC LINK, MEMORY CARDS EXPAND ORGANIZER'S USES

Applications for Sharp Electronic's hand-held electronic organizer—the Wizard—are increased with a computer link that transfers data from the organizer to a PC, and vice versa. The Organizer Link includes all the hardware and software (3.5-in. or 5.25-in. floppy diskettes) needed for file exchange between the Wizard and an IBM-compatible PC. The link hardware includes a level converter, an interface cable, and an ac adaptor. In addition, the electronic organizer's memory can be expanded with removable 32- and 64-kbyte RAM cards. The Organizer Link retails for $149.99. The suggested retail prices for the 32-kbyte and 64-kbyte RAM cards are $79.99 and $129.99, respectively.

Sharp Electronics Corp., Sharp Plaza, Mahwah, NJ 07430; (201) 529-9542. **CIRCLE 335**

UPGRADED MICROVAX SYSTEMS DOUBLE TO TRIPLE CPU THROUGHPUT

Delivering throughput improvements of from 1.85 to 2.8 times that of earlier VAX-compatible systems, the VAX 6000 Model 400, the MicroVAX 3100 workstation, and VAXserver 3100 bring the performance levels of Digital Equipment's latest systems to new highs. In the large-systems area, the VAX 6000 series gains two models. The 210 is a relatively low-priced (from $129,000) entry-level multiuser system with a throughput of 2.8 times that of the VAX-11/780. The more powerful Model 400 delivers about 36 times the throughput of the original 11/780 and starts at $239,000.

Now in development is a vector processor with 63 new instructions that can be used with the MicroVAX CPU cards to accelerate array computations in the Model 400. Up to four CPUs can be installed in the Model 400, and one or two of the CPU cards can be replaced with vector-processor cards.

For cost-conscious VAX users, DEC also offers a low-cost workstation and server: the MicroVAX 3100 and VAXserver 3100, respectively. These systems deliver 2.5 times the throughput of the older MicroVAX 2000 and VAXserver 2000 systems. The server's starting price of $6680 even undercuts IBM Corp.'s PS/2 Model 80 PC. The 3100 Model 10 low-end workstation configuration, which costs $8480, adds to the base system a 104-Mbyte hard disk drive, a 1.4-Mbyte 3.5-in. floppy drive, and a five-user VMS operating-system software license.

Digital Equipment Corp., Four Results Way, Box 1022, Marlborough, MA 01752-9122; (508) 467-5111. **CIRCLE 320**

DAVE BURSKY

ADD-IN MEMORY FITS HP WORKSTATIONS

Two low-cost memory boards help users boost the performance of their Hewlett-Packard 9000 Model 340 and 360 workstations. The EM340 is a 4-Mbyte RAM board, while the EM360 is available in 4-, 8-, and 12-Mbyte configurations. Priced lower than their HP counterparts, these memory products are of particular benefit to HP users who are entering the Unix environment. The boards are completely compatible with any HP memory installed in the computer and come with an extended five-year warranty.

Infotek Systems, 1045 S. East St., Anaheim, CA 92815; (714) 956-9300. **CIRCLE 359**

FAST, LOW-NOISE JFET OP AMPS DON'T DRIFT; BIAS CURRENT RUNS 20 PA

A pair of JFET-input IC op amps, Burr-Brown's OPA627 and OPA637, boast a mix of precision and speed not available until now. The devices are built on a dielectrically isolated (DI) complementary process that builds fast vertical pnps as well as fast npn transistors. They offer the lowest noise of any JFET-input op amp.

The OPA627 is unity-gain stable with a typical unity-gain bandwidth of 16 MHz. The decompensated OPA637 has a typical gain-bandwidth product of 80 MHz at a gain of 5, which is its minimum stable gain. All other specifications match.

The rest of the specifications are minimums or maximums unless noted typical (t). For the B and A grades, slew rates run 45 and 40 V/μs, respectively. Both devices offer a settling time of 600 ns (t) to 0.01 % for a 10-V output step. Open-loop gain is 110 dB for the B grade and 104 dB for the A. With their bias currents of just 5 pA for the B grade and 50 pA for the A grade, these op amps are just right for high-speed sample-and-hold amplifiers and current-to-voltage converters.

But if a fast, low-offset-voltage op amp is called for, these chips fill the bill. Offset voltage for the B and A grades runs 100 and 500 μV, respectively, while offset drift is 1 and 1.2 (t) μV/°C. Now for noise: between 0.1 and 10 Hz, voltage noise of the B-grade is just 2.5 μV pk-pk, with a similar typical value for the A-grade. At 1 and 10 kHz B-grade voltage noise runs 6 nV/$\sqrt{\text{Hz}}$.

Although both speed and low-noise operation demand current, these op amps draw no more than 7 mA from their $\pm$15-V supply rails. Nonetheless, they can typically put out 30 mA. In quantities of 100, the A-grade OPA627/637AP costs \$7.50 each and the B-grade goes for \$15. Delivery is from stock.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; Bruce Trump, (602) 746-7347. **CIRCLE 321**

FRANK GOODENOUGH

SINGLE, DUAL, AND QUAD OP AMPS OFFER HIGH SPEED AT LOW POWER

With typical unity-gain bandwidths of 2 MHz and slew rates of 0.9 V/μs, the TLE2021 single, TLE2022 dual, and TLE2024 quad op amps provide a three-to-five-times improvement over other premium op amps, yet dissipate no more power. The devices operate from a single supply of 4 to 40 V, or a split supply, and have a common-mode input-voltage range that includes the negative rail. Each device incorporates phase-reversal circuitry to eliminate unexpected changes in output states when one of the inputs goes below the negative-supply rail.

The amplifiers' current consumption—230 μA maximum at 5 V—changes only 44 μA over the full military temperature range at a typical rate of 0.08 μA/°C. Texas Instruments credits this stable current consumption over the devices' operating-temperature range to its Excalibur process characteristics and advances in operational-amplifier circuit design.

These new op amps are the first devices TI has fabricated using the Excalibur process, a complementary bipolar technology that incorporates isolated vertical-pnp transistors. According to the company, the Excalibur process is the first high-volume manufacturing technology to combine these high-performance pnp transistors with p-channel JFETs, super-beta npn transistors, and metal-nitride-polysilicon capacitors.

The single, dual and quad op amps are characterized for operation over commercial, industrial, and military temperature ranges. Devices come in five package types: plastic and ceramic DIPs, small-outline packages, leadless chip carriers, and metal cans. MIL-STD-883C, Class B versions are planned for later this year. Prices begin at \$1.76 in quantities of 1000. Delivery is from stock.

Texas Instruments Inc., P. O. Box 809066, Dallas, TX 75380-9066; (800) 232-3200, Ext. 700. **CIRCLE 322**

JON CAMPBELL

NEW PRODUCTS
ANALOG

PRECISION SINGLE AND DUAL WIDEBAND OP AMPS SPORT LOW NOISE AND DRIFT

With a unity-gain bandwidth of 35 MHz and a gain-bandwidth product of 100 MHz (below 100 kHz), the Harris HA-5221 single and HA-5222 dual op amps offer a mix of low noise, low offset voltage, and low drift combined with high output drive and open-loop gain. Moreover, the dual devices are as good as the singles. These unity-gain-stable op amps slew at 15 V/μs, representing a full-power bandwidth of 238 kHz. Settling time for a 10-V output step to 0.01% is typically 1.5 μs, and settling to 0.1% runs about 0.4 μs. Closed-loop gain for both specs is –1.

Offset voltage is less than 750 μV and offset drift is less than 0.5 μV/°C. Offset-voltage match between the two channels of the dual amplifier is within a maximum of 750 μV at 25°C, and twice that over the operating-temperature range. Common-mode rejection ratio is a minimum of 100 dB at 25°C.

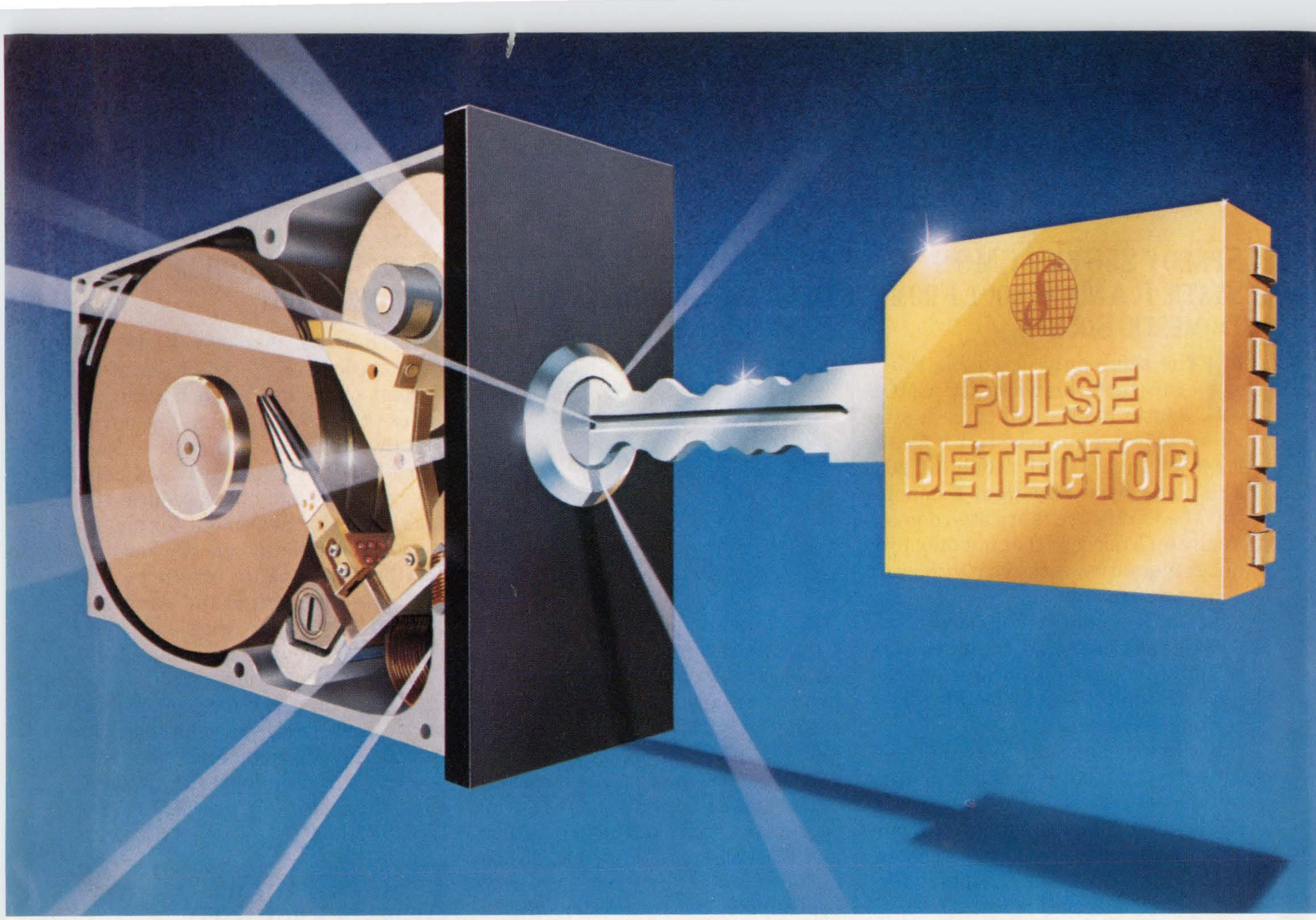
Input-voltage noise from 0.1 to 10 Hz is a maximum of 0.37 μV pk-pk; spot-voltage noise at 1 kHz is 4.5 nV/$\sqrt{}$Hz and is just over twice that at 10 Hz. Total harmonic distortion plus noise, a specification vital for high-performance audio applications, is less than 0.005%. The op amps are tested at a closed-loop gain of 10 with an output swing of 5 V rms and a 600-Ω load. Test frequency is 1000 Hz.

Open-loop gain is a minimum of 106 dB while putting ±10 V across 1000 Ω. However, the chips can put that voltage across 200 Ω, often eliminating the need for an additional buffer amplifier. On the dual HA-5222, channel separation at 10 kHz is typically 110 dB.

The chips draw a maximum of 11 mA/op amp from split ±15-V rails. In quantities of 100, unit prices for the HA-5521 start at $6.68. The prices for the HA-5222 start at $11.14. Delivery is from stock.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; Wes Kilgore, (407) 729-5310. **CIRCLE 323**

FRANK GOODENOUGH



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silicon systems®

CIRCLE 70

SPEEDY 256-KBIT CMOS STATIC RAMS SPROUT FROM DOMESTIC SOURCE

The seemingly insatiable thirst for fast, high-density CMOS static RAMs will come a step closer to being quenched with the release of the PDM41 family of 256-kbit chips from Paradigm Technology. The RAMs are fabricated domestically on a process that not only produces memories with access times as short as 20 ns, but also results in the industry's smallest chip areas for 256-kbit devices. Also, the chips easily slip into small-outline J-lead, 300-mil DIP, and 28- or 32-lead leadless ceramic packages.

Six chips make up the family—a 256k-by-1, a 32k-by-8, and four 64k-by-4 devices. Besides the 20-ns chips, 25-, 35-, and 45-ns versions are available for operation over the commercial temperature range. Military versions have access times of 25, 35, 45 and 55 ns. All operate from a 5-V supply and consume about 400 mW when active and 400 µW during standby. Low-power versions shave the active power by 50 mW and cut the standby power to just 100 µW.

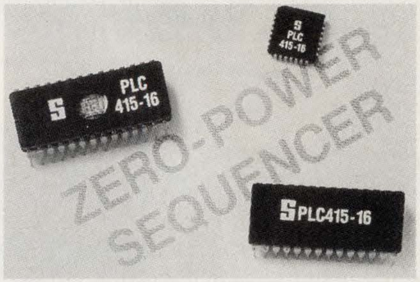
Four 64k-by-4 versions are being readied—the PDM41258, 41298, 41251, and 41252. The first uses the standard multiplexed data input and output lines and has a Chip Enable input. The 41298 adds an Output Enable line while the 41251 and 52 have separate data inputs and outputs but have only the Chip Select line. On the PDM41251, the outputs track the inputs during a write operation; on the 41252, the outputs go to a high-impedance state during a write. The PDM41257 is the 256k-by-1 memory, while the 41256 is organized as 32k-by-8.

Prices for the 20- and 25-ns options of PDM41258 are $147.05 and $113.12, respectively, for ceramic-DIP versions in quantities of 100. Samples are available now for the 41258; all others can be had in October.

Paradigm Technology Inc., 71 Vista Montana, San Jose, CA 95134; (408) 954-0500 **CIRCLE 324**

DAVE BURSKY

PROGRAMMABLE SEQUENCER DELIVERS SUPERSET OF PLS105, 405 FEATURES



Although it drops right into the sockets now holding the popular bipolar PLS105 and 405 programmable logic sequencers, Signetics' CMOS PLC415-16 sequencer packs more features and consumes less power. The 28-pin circuit crams in 17 inputs, eight buried registers, eight output registers, and 68 AND product terms. It also includes a standby mode that trims operating power from its 300-mW active level to just 2.5 mW. In comparison, the bipolar chips consume more than twice the active power and have no reduced-power standby mode. The bipolar chips, however, run at more than double the clock frequency of the new CMOS chip.

Besides all the features of the PLS105 and 405, the 415 has programmable asynchronous initialization and output-enable functions that can be controlled from the internal AND array or from an external source. As a result, the state machine implemented in the array can be asynchronously initialized to start in any desired pattern.

Because the chip carries multiple clock inputs, more than one Mealy-type state machine can be implemented on a chip. The programmable elements of the PLS415-16 use UV EPROM memory cells, and when sold in windowed packages, the sequencer can be erased and reprogrammed. Prices range from $12 to $15 in quantities of 1000, depending on packaging.

Signetics Co., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; (408) 991-2000. **CIRCLE 325**

DAVE BURSKY

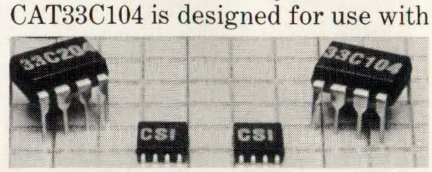
FAST SRAM MODULE STORES 1 MBIT

Housed in a 32-pin 600-mil DIP, a 1-Mbit static RAM module is one of the fastest of its kind, offering access times of 30, 35, and 40 ns. The device is fully compatible with future monolithic 128k-by-8-bit static RAM chips to prevent design obsolescence. It is also a direct replacement for similar products currently on the market. Unlike comparable products, the part uses a more rigid and less costly printed circuit board that lends itself to stringent industrial applications. A built-in protection circuit using both high- and low-frequency filter capacitors further enhances the module's performance.

Micron Technology Inc., 2805 E. Columbia Rd., Boise, ID 83706; (208) 383-4000. **CIRCLE 336**

4-KBIT EEPROMS OPERATE FROM 3 V

Organized at the user's option as 256 by 16 bits or 512 by 8 bits, two CMOS EEPROMs can be operated and programmed with a 3-V supply. The 4-kbit devices, designated the CAT33C104 and CAT33C204, require only two 1.5-V batteries, making them ideal solutions for a wide range of low-power, battery-backed applications. Each provides a serial interface, can endure 10,000 erase-write cycles per bit, and retains data for a minimum of 10 years. The CAT33C104 is designed for use with



the COPS family of microcontrollers or other standard microprocessors such as the 8048 or 8051. It is Microwire-compatible and provides software data polling. Packaging options include 8-pin plastic DIPs and small-outline configurations. In quantities of 100, the commercial DIP version of either device sells for $5.54.

Catalyst Semiconductor Inc., 2231 Calle De Luna, Santa Clara, CA 95054; (408) 748-7700. **CIRCLE 337**

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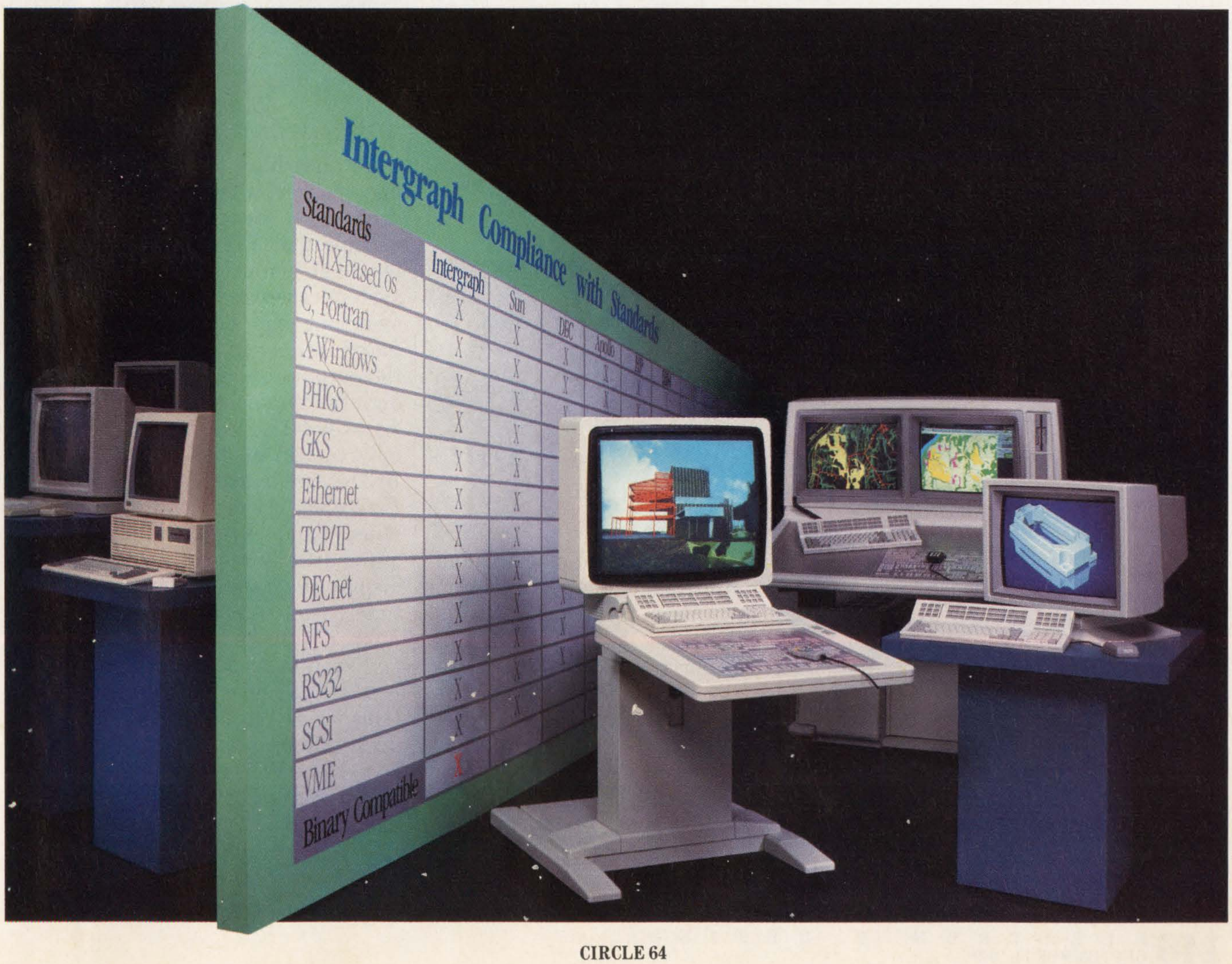


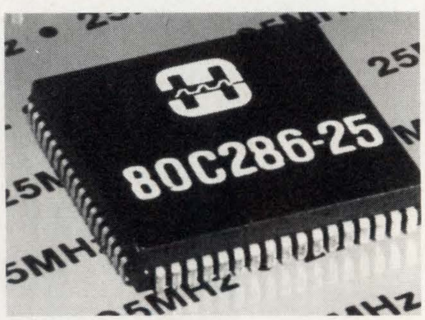
CIRCLE 64

LOGIC DEVICES ARE FAST, LOW-POWER

Three CMOS PEEL (programmable electrically erasable logic) devices rival the speeds of comparable bipolar parts while offering the additional benefits of reprogrammability and low power consumption. The 24-pin 22CV10 and 20CG10 operate at 25 ns and consume just 55 mA and 45 mA, respectively, in standby mode. The 20-pin 18CV8-15 runs at 15 ns and consumes 90 mA on standby. Fabricated in CMOS, all three devices provide up to 12 independently programmable input-output macro cells, enabling them to emulate most 24-pin or 20-pin bipolar PLDs. The 22CV10 has 132 product terms and up to 22 inputs and 10 I/O pins. The 20CG10 has 92 product terms, up to 22 inputs, and 10 I/O pins. The 18CV8-15 offers 74 product terms, up to 18 inputs, and 8 I/O pins. In lots of 1000, prices are as follows: the 22CV10 costs \$7; the 20CG10, \$4.50; and the 18CV8-15, \$5.

Gould AMI, 2300 Buckskin Rd., Pocatello, ID 83201; (208) 234-2796. **CIRCLE 338**

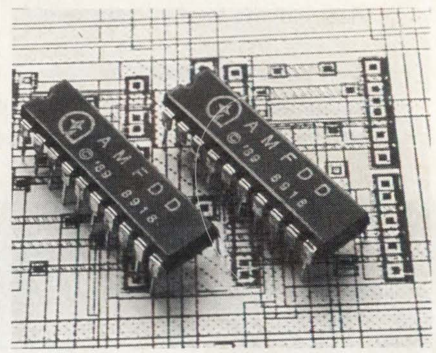
MIL MICROCONTROLLER HAS EXPANDED I/O



The 83C451 is one of the first mil-standard expanded input-output microcontrollers currently available. The single-chip device adds three 8-bit I/O ports and four I/O control lines. It reduces the requirement for external I/O ports, allowing for more inputs and outputs without having to add external hardware. The I/O central line facilitates interprocessor communication. Offered in two reduced-power modes, the 83C451 has full functional power dissipation of 1.25 mW (at 12 MHz, 6 V) in the active mode. In the idle mode, power dissipation is reduced to 25 mW (12 MHz, 6 V), and is cut still further to 250 μW in power-down mode. The processor can use the same software and code as earlier versions that had fewer I/O pins. Packaging options include 64-pin ceramic DIPs and 68-pin LLCCs. The DIP price is \$125 in lots of 100 units. Shipments are from stock.

Signetics Co., 811 E. Arques Ave., Sunnyvale, CA 94088; (408) 991-2000. **CIRCLE 339**

CHIP DRIVES PC CLOCK DISPLAY



With one chip, the Frequency Display Driver (FDD), designers can drive seven segmentLEDs used to indicate the CPU operating speed in personal computers with multiple system-clock frequencies. The auto-switching chip is a reference source-gated frequency and pulse counter, the output of which can drive a two-digit floating-point display unit from 0.1 to 39 MHz. The display unit need only consist of two common anode LEDs, two resistor packs, and an FDD chip. The display driver continuously samples the system clock and automatically reconfigures itself to display the correct frequency at all times. Thus, it eliminates the use of jumper settings to set the high and low system frequencies. The latter method also does not address situations where there are more than two operating frequencies on the system board. The FDD comes in a standard 20-pin plastic DIP and sells for \$4.95 in lots of 100.

Amax Applied Technology Inc., 3001-A W. Mission Rd., Alhambra, CA 91803; (818) 300-8828. **CIRCLE 340**

REAL-TIME OPERATING SYSTEM SUPPORTS RISC AND CISC PROCESSORS

A real-time operating and development environment that supports a wide range of Intel and Motorola RISC and CISC microprocessors is now available with the introduction of OS-9000, from Microware Systems Corp. The OS-9000 operating system, of which 95% is written in C to maximize portability, is upwardly compatible with the company's popular OS-9 operating system.

Initially, the operating system will support Motorola's 68020, 68030, and 68040, as well as Intel's 80386. Support for the Intel 80486, Motorola's 88000, and a variety of other RISC processors and will be available early next year. Also planned for early 1990 is support for ISDN as well as a variety of loosely- and tightly-coupled VMEbus multiprocessor architectures.

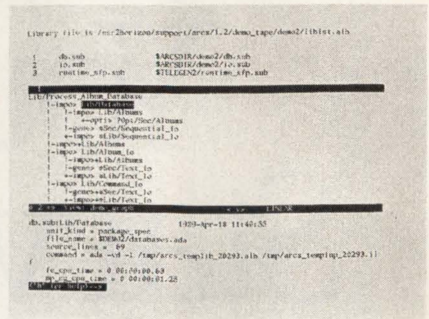
Among OS-9000's more powerful features is its scalable, modular architecture. By selecting appropriate kernel, file-management, utility, and development modules, designers can take advantage of an assortment of operating-system configurations from a standalone kernel that can reside in ROM to a full-blown multiuser development system. In addition, it can run on networks, using Ethernet, Arcnet, and serial communications with TCP/IP and SLDC protocols. Users can also build their own library functions if they want to add to the existing library.

The operating system is available immediately in both industrial and professional versions. The industrial version includes the real-time kernel, interprocess communication, and console managers. In OEM quantities, it sells for $350. The professional version starts at $650, also in OEM quantities. This version adds disk and tape support, over 70 utility commands, and a C compiler to the industrial package.

Microware Systems Corp., 1900 N.W. 114th St., Des Moines, IA 50322; (512) 224-1929. **CIRCLE 326**

RICHARD NASS

PROGRAMMING ENVIRONMENT LINKS MIDDLE- TO BACK-END ADA DEVELOPMENT TOOLS



TeleArcs, a programming environment for the TeleGen2 Ada Compilation System, tightly integrates the Ada-sensitive tools needed for the detailed design, development, and test stages of the software lifecycle. TeleArcs, from TeleSoft AB, runs with the TeleGen2 Ada program library, using its inherent database facilities to accumulate information about the user software. It lets the developer view, access, and maintain the software at many different levels.

The toolset consists of an Ada language editor, an Ada library with browsing capabilities, a program debugger, and interactive cross-referencing features. With the browsing feature, users can view program units and import certain relationships.

The interactive system emphasizes its user-friendliness. For example, if the programmer changes a particular variable, TeleSoft will let him know what else must be changed to maintain the correct syntax. This enables quick and easy changes to the software. The user can also customize this interface.

The built-in editor processes the code with syntax checking, error feedback, Ada code formatting, and hierarchical text presentation.

Available for the VAX/VMS and Sun-3 platforms, prices range from $4500 to $37,500, depending on configuration.

TeleSoft AB, 5959 Cornerstone Court West, San Diego, CA 92121; (619) 547-2700. **CIRCLE 327**

RICHARD NASS

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NEW PRODUCTS

SOFTWARE

Program For Macintosh Analyzes Images

A software package provides powerful image processing when used with the QuickCapture frame grabber board and a Macintosh II. The Image Analyst program measures areas within an image, analyzes shapes, counts objects, and measures angles and distances. It also filters images to enhance them and analyzes the gray level content of images by performing histograms. Image Analyst supports all QuickCapture functions, including its 256 gray levels and 1:1 pixel aspect ratio. Its powerful functions are accessed with the standard Macintosh interface of pull-down menus, windows, and icons. Image Analyst sells for \$1995; the QuickCapture board is priced at \$1595.

Data Translation, 100 Locke Dr., Marlboro, MA 01752; (508) 481-3700. **CIRCLE 341**

Math Software Breaks 640-kbyte RAM Barrier

The latest version of PC-Matlab, an interactive software package for scientific and engineering numeric computation, breaks the 640-kbyte memory barrier for 80286-based personal computers. Version 3.5 runs in PC AT protected mode to support up to 15 Mbytes of installed extended memory. It also provides new functions for digital signal processing, filter design and analysis, and spectral analysis. Additional functions introduced in PC-Matlab V3.5 include solution of ordinary differential equations and systems of nonlinear equations, numerical function integration, unconstrained nonlinear optimization, complete elliptic integral of the first kind, Jacobi elliptic functions, and other numeric techniques. The interpreter itself has been optimized to perform scalar operations 2 to 10 times faster than the previous version of PC-Matlab. It is available immediately and sells for \$695.

Math Works Inc., 21 Eliot St., South Natick, MA 01760; (508) 653-1415. **CIRCLE 342**

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Kit P206 $100

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Kit P205 $75

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CIRCLE 71

80386SX-BASED EMBEDDED PCS RUN DOS SOFTWARE IN A VMEBUS FORM FACTOR

Users can run their PC software in a rugged VMEbus system with a family of embedded-PC products from Radix Microsystems. Applications targeted for the EPC-3 family include a controlling computer or a human-interface computer embedded within automated equipment, medical systems, and test equipment.

The EPC-3 family includes the 80386SX-based CPU board, disks, and an assortment of expansion modules. High-density packaging made it possible to squeeze the entire CPU into one VME slot. The CPU board handles all the functions of an ordinary PC, and includes up to 4 Mbytes of dynamic RAM, an optional math coprocessor, serial and parallel I/O ports, a keyboard interface, and a VGA controller.

Thanks to an EPC-module sub-bus structure called the EXM bus, two expansion modules can fit in each VMEbus slot. EPC-3 expansion modules include four options for mass storage: a VMEbus 40-Mbyte hard disk and 3.5-in. floppy drive, a local-area-network interface with software for diskless operation, a solid-state disk for harsh environments, and an external disk interface.

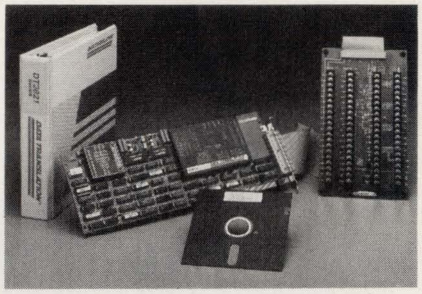
Software support is available for embedded-PC system development. The EPConnect 3.0 software includes programs for high-level hardware system configuration, system test, and system debug, as well as run-time programs.

With 1 Mbyte of dynamic RAM, the EPC-3 CPU costs $2595. The EXP-MS mass-storage module, the EXM-1 Ethernet module, and the EXM-3 disk interface for external drives cost $850, $380, and $260, respectively. The 1-Mbyte solid-state disk is $590 and the EPConnect 3.0 software is $300. All prices are in quantities of 100 and all products are available now.

Radix MicroSystems Inc., 19545 NW Von Neumann Dr., Beaverton, OR 97006; (503) 690-1229. **CIRCLE 328**

LISA GUNN

DATA-I/O BOARD SIMULTANEOUSLY SAMPLES MULTIPLE INPUTS



The DT2829 data-I/O board from Data Translation makes it possible to sample several inputs at the same time with great precision. Sampling multiple inputs at one time is important to designers who need to simultaneously analyze multiple responses to a single stimulus despite rapid signal changes.

The PC/AT-compatible board combines simultaneous inputs, high resolution, and 30-kHz analog-digital throughput. It can measure eight different sensors, transducers, or other analog signals within ±20 ns of one another, and it's capable of 16-bit resolution. According to the company, designers can get 10 to 100 times greater accuracy, far greater dynamic range, and higher throughput than with previous PC/AT products that sample simultaneously.

To assure that the DT2829 delivers its full rated accuracy, the analog-to-digital converter features a highly stable voltage reference and a circuit that automatically calibrates the board each time it's powered up. Users sample multiple signals simultaneously by employing eight onboard sample-and-hold circuits. By supplying a separate sample-and-hold front end for each input, a "snapshot" can be taken of incoming dynamic signals from up to eight sensors at once.

The board's 16-bit precision means that input signals are sampled with extremely high accuracy (±0.006% of full-scale reading).

The DT2829 board costs $2995. Delivery is in 5 days.

Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752-1192; (508) 481-3700. **CIRCLE 329**

CLIFFORD METH

DSP CARD PROVIDES QUALITY AUDIO I/O

A digital signal processing card for the IBM PC provides dual-channel professional-audio-quality analog I/O, as well as advanced digital I/O. The DSP-56's two 16-bit input channels permit simultaneous sampling of full audio bandwidth stereo signals with software-selectable sampling rates of up to 100 kHz per channel. Crystal-generated audio standard rates of 32, 44.1, and 50 kHz are also provided. For applications requiring higher sampling, the DSP-56 can acquire a single channel at up to 400 kHz while maintaining 12 bits of precision. The board employs Motorola's DSP56001, a 24-bit, 10.25-MIPS DSP chip, and the DSP56ADC16 sigma-delta oversampling analog-to-digital converter. In addition, a pair of ninth-order elliptic reconstruction filters are included. It is priced at $2995.

Ariel Corp., 433 River Rd., Highland Park, NJ 08904; (201) 249-2900. **CIRCLE 343**

BOARD SYNCHRONIZES PC TO ATOMIC CLOCK

By decoding time information from WWV and WWVH radio signals transmitted by the National Institute of Science and Technology (NIST), the Computer Time Standard, or CTS-10, provides reliable, traceable, and accurate time for IBM PCs and compatibles. These signals are synchronized to the NIST atomic standard, allowing any CTS-10-equipped PC to incorporate the correct time. It automatically accommodates daylight-saving time, leap years, leap seconds, and other anomalies. The plug-in board also permits time zone selection, 12- or 24-hour formats, adjustable on-screen display, and color selection. The CTS-10 works on any PC running DOS 2.10 or higher. It plugs directly into the PC and maintains the PC clock. Single unit pricing, including software, is under $200.

Coordinated Time Link, 921 Bluebonnet, Sunnyvale, CA 94086; (408) 738-2862. **CIRCLE 344**

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We've just packed a lot of CMOS memory into a single 32-pin DIP. You can now have 1 megabit (128Kx8) or 2 megabit (256Kx8) in SRAM or EEPROM with industrial or military temperatures. Our new high-density hybrid memories give you a choice. You'll also find that they'll lower your costs, save you board space, and conserve power, too.

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Want more? The EEPROMs offer a 10 Year Data Retention after write, and automatic page write option with internal address and data latches for up to 512 bytes, and 1 to 64 bytes/pages, up to 8 pages. Page write only 3.0mSec/page. And, there's data polling for end of write detection, and hardware and software data protection, too. Read access time is 150nSec.

The SRAMs include data retention with voltages down to 2.0 volts, read/write cycle compatibility with almost all microprocessors, and read access and write cycle times of 120nSec.

If 1 or 2 Megabit isn't enough, our 4 Megabit (512x8) will be out soon in the same 32-pin DIP. We also offer a range of access times down to speeds less than 50nSec, and memory capacities into the terabit region. Or, if you want to talk about products like a complex single-package system, a supercomputer array, or a totally defined multi-package management information system, give us a call. Your design or ours, we'll make it happen.

CERTIFIED TO MIL-STD-1772

CIRCLE 66

White Technology, Inc.

A wholly owned subsidiary of Bowmar Instrument Corporation

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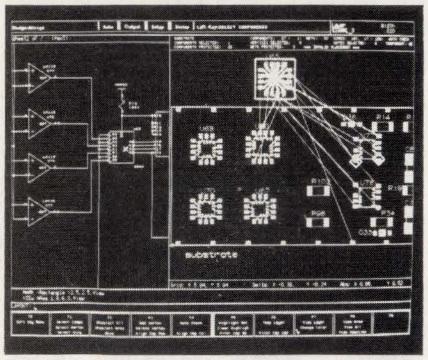
AUTOMATED MULTILAYER-BOARD DESIGNS NOW INCLUDE HYBRID CIRCUITS



Hybrids are found in almost every aspect of electronic circuitry. They are seen in computers, automobiles, and in the aerospace, military, ATE, and medical industries. For this reason, Mentor Graphics, Beaverton, Ore., has developed the Hybrid Station, a fully automated system for the design of thick-film hybrid circuits. This includes single-layer, multilayer, and cofired ceramic boards.

Because the Hybrid Station is fully integrated with Mentor's set of electronic-design-automation tools, engineers can design and simulate an entire system containing hybrids within one environment. The tools offer schematic entry, simulation, thermal analysis, packaging, and post-layout functions.

Some unique features of the tools include blind, buried, and staggered vias, automatic resistor generation, chip and wire bonding, up to 255 process layers, and dielectric checking.

Shipment of the Hybrid Station will begin in October for Apollo DN3500, DN4500, and DN10000 platforms. Pricing begins at $102,000.

Mentor Graphics Corp., 8500 S.W. Creekside Pl., Beaverton, OR 97005; (503) 626-7000. **CIRCLE 330**

RICHARD NASS

SIMULATOR HANDLES 65,000 EVENTS/S

Version 1.2 of the OrCAD/VST PC-based logic simulation package is capable of performing 65,000 events/s running on a 20-MHz 80386 machine. Other enhancements to the simulator include a 20% increase in library parts (bringing the total device count to 1750) and more efficient tracing of internal and logic nodes. OrCAD/VST can also work with OrCAD's simulation modeling program, OrCAD/MOD. This optional product accepts an industry-standard Jedec file and allows VST to simulate multiple PLDs within the design environment. VST is priced at $995, with free updates to all registered users of VST 1.1 under warranty.

OrCAD Systems Corp., 1049 S.W. Baseline St., Suite 500, Hillsboro, OR 97123; (503) 640-9488.

CIRCLE 360

CHIP LINKS DATA-COMMUNICATION EQUIPMENT TO T1, CEPT ISDN LINES

An efficient, cost-effective means of connecting data-communication equipment to either domestic T1 (1.544 Mbits/s) or European CEPT (2.048 Mbits/s) transmission facilities for ISDN service is now available from AT&T Microelectronics. The T7115 synchronous protocol data-formatter IC serves as the ISDN primary-rate interface in various hardware, such as front-end processors, host computers, PBXs, T1 multiplexers, cluster controllers, and high-end workstations.

The chip can be used in any application where many high-level data-link-control (HDLC) channels must be terminated. According to the company, the chip is the only one of its kind that enables ISDN-network operators or T1-multiplexer vendors to dynamically allocate the amount of bandwidth to customers, depending on their needs. As a result, equipment vendors can easily implement and offer fractional and full T1 capability.

All HDLC functions are performed by the chip, including the generation and checking of flags, CRC, and abort and idle codes. These functions are provided for 24- or 32-time-slot transmissions modes.

In addition, the device offers full memory management and DMA capability for each —active channel, of which there can be 32. Multiple receive and transmit packets are queued in separate linked lists for each channel, which relieves much of the overhead on the resident CPU. This eases implementation of the upper layers of the Open System Interconnect protocol stack.

The T7115 IC comes in a 68-lead plastic leaded chip carrier. It costs $75 each in small volumes and $55 each in lots of 10,000. Small lots are delivered from stock.

AT&T Microelectronics, Dept. 52AL330240, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447. **CIRCLE 331**

DAVID MALINIAK

MODEM COMPRESSES DATA THREE-TO-ONE

In addition to CCITT V.25 bis and V.42 capabilities, the MultiModem 224EH7 provides users with MNP Class 7 data compression. When operating in the V.42 MNP mode, 3:1 data compression can be achieved. The 2400-bps modem performs V.25 bis dialing and V.42 error correction. By combining MNP Class 7 data compression with MNP Class 4 error correction (part of V.42), accurate data throughput is increased dramatically. MNP Class 7 data compression adds a run-length encoding technique to the compression algorithm that takes into account the recurrences of character sequences in transmissions and adjusts the code accordingly. This technique is similar to what the proposed V.42 bis standard will eventually incorporate, but is available now in the 224EH7.

Multi-Tech Systems Inc., 2205 Woodale Dr., Mounds View, MN 55112; (612) 785-3500. **CIRCLE 345**

TWO-SPEED MODEM PLUGS INTO PS/2

Designed for the IBM PS/2, a plug-in board combines the functions of three separate boards: a 2400-bps Bell-201-compatible synchronous modem, a 4800-bps Bell-208-compatible synchronous modem, and an SDLC communication adapter supporting multiple SNA protocols. With the AdaptModem/2 Model 4800, users can dial up host mainframes and other PCs or PS/2s which have either 201- or 208-compatible modems. The dual-speed modem eliminates the need to install two separate modems, as well as an SDLC board. It can be used with Network Software Associates' AdaptSNA software to achieve PS/2-to-host connectivity across all major SNA protocols. The board carries a price tag of $1195; software ranges from $245 to $785.

Network Software Associates Inc., 39 Argonaut, Laguna Hills, CA 92656; (714) 768-4013.

CIRCLE 346

High-Definition Graphics ICs Get Mil-Spec Rating

Five graphics ICs from **Brooktree Corp.** (San Diego, Calif.) now comply with MIL-STD-883C specifications. Included in the new monolithic CMOS offerings are two video d-a converters, two RAM d-a converters, and a clock generator. The two video d-a converters are the 30-MHz, triple 8-bit Bt101/883 and the 50-MHz, single 8-bit Bt102/883. Both devices have pipelined operation with extremely low differential and integral linearity-error levels. The two RAM d-a converters are the Bt453/883 40-MHz, 256-by-24 color palette and the Bt458/883 125-MHz, 256-by-24 color palette. These pipelined products support up to 259 simultaneous colors from a 16.8-million color palette. The Bt438/883 125-MHz clock-generator chip is designed for the RAM d-a converters. **CIRCLE 347**

ASIC Design Tools Run on DEC Workstations

The Modular Design Environment (MDE) software from **LSI Logic** (Milpitas, CA) now runs on Digital Equipment Corp.'s RISC-based workstations. The MDE is a set of software tools used to design ASICs, from system definition, architectural design, and design implementation to chip verification. The tools ease the design of array- and cell-based ASICs ranging from single, low gate-count devices to complex, multi-ASIC systems. The price per node starts at $35,000.

CIRCLE 348

CAE/CAD Tools Merge in OEM Agreement

Thanks to an agreement with EDA Systems Inc., **Harris Scientific Calculations Division** (Fishers, N.Y.) is now incorporating EDA's framework software into its integrated automation toolset for printed circuit board design. With it, Harris SC can offer a common design and data-base environment for its schematic capture and simulation tools as well as its Scicards layout, thermal analysis, and drafting and documentation tools. The company also made an agreement with Viewlogic Systems Inc. to sell Workview Series I and II design capture and simulation software. Viewdraw, a design capture system, and Viewsim/SD, a simulation tool for mixed analog and digital circuits, have been integrated with the Harris Scicards system for pcb layout.

CIRCLE 349

FOR LAMBDA CIRCLE 131 →

DATA BOOK DESCRIBES 883B ANALOG ICs

Containing over 500 pages of technical information, Burr-Brown's *Military Products Data Book, Vol. 1,* provides a look at the company's broad line of 883B, SMD, and DESC (Defense Electronics Supply Center) analog microcircuits. Devices are offered in both packaged and die forms and include more than 80 high-performance op amps, power amps, data converters, multiplexers, instrumentation amps, multipliers, and voltage-to-frequency converters. The book also describes the company's DESC-certified facilities, monolithic and hybrid process flows, and quality assurance programs.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (800) 548-6132 or (602) 746-1111. **CIRCLE 350**

SELECTOR GUIDE LISTS PROGRAMMABLE DEVICES

Updated quarterly, Logical Devices' *Spring 1989 Master Device List* features over 2000 programmable devices organized by manufacturer and device architecture. The 50-page booklet supplies information on device technology, including number of pins, array size, and voltage. Additionally, the listing specifies the Logical Devices' programmer that supports each device (or if future support is planned). The selection guide can also be obtained on 5-1/4-in. disks.

Logical Devices Inc., 1201 N.W. 65th Pl., Fort Lauderdale, FL 33309; (800) EE1-PROM or (305) 491-7404. **CIRCLE 351**

GLOSSARY DEFINES VISION, IMAGING TERMS

A 19-page glossary of microcomputer vision and imaging terms provides nearly 230 definitions. These include such areas as image capture, manipulation and analysis, microcomputer systems, and imaging software.

MetraByte Corp., 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000. **CIRCLE 352**

DETECTION AND SENSING COMPONENTS

A 14-page brochure provides an overview of Baumer Electric's line of electric sensors. It discusses the company's latest detection techniques and sensing solutions, including photoelectric sensors, incremental and absolute encoders, electronic and electromechanical switches, and inductive proximity sensors.

Baumer Electric Ltd., 122 Spring St., Southington, CT 06489; (203) 621-2121. **CIRCLE 353**

NON-CONTACT VIDEO INSPECTION SYSTEM

A full-color brochure presents the capabilities, benefits, and complete specifications of the Videoscope 3-D, a non-contacting video inspection system. Using system diagrams, inspection software menus, and other informative visuals, the literature outlines how the Videoscope addrsses the dimensional inspection and flaw-detection requirements of quality control, manufacturing, production, and design departments. The vision system provides fully automatic measurements with accuracies from ± 0.0002 to ± 0.000001 in. and greater in a fraction of the time required with manual methods.

Videometrix Inc., an Agfa-Matrix Co., 5321 Sterling Center Dr., Westlake Village, CA 91361; (818) 707-0423. **CIRCLE 354**

COAXIAL CABLE SELECTION GUIDE

A brochure presents a line of coaxial cables engineered in a wide selection of materials, sizes, and shieldings. The cables are available in many configurations, including fiber-optic types and special hybrid LAN cables which include both fiber and copper components. All products are UL-listed and classified to conform to the National Electric Code for installation in air-handling plenums without conduit.

NEK Cable Inc., 2150 Fifth Ave., Ronkonkoma, NY 11779; (516) 588-0200. **CIRCLE 355**

IDC INTERCONNECTS ARE MILITARY-QUALIFIED

Military designers can now refer to a single catalog when specifying 3M military-qualified IDC components. The 35-page document lists components qualified under MIL-C-83505 and MIL-C-49055. The latter addresses round conductor flat cable used for IDC systems, while the former is the military specification for insulation displacement sockets and headers. All components appear on the qualified parts list. Cross references of military part numbers and national stock numbers are included.

3M, Department 89-57, P.O. Box 2963, Cedar Rapids, IA 52402; (512) 984-6708. **CIRCLE 356**

PIN AND SOCKET POWER CONNECTORS

A 24-page handbook on pin and socket connectors serves as a guide to choosing the right power connector for the application at hand. The booklet covers such factors as current rating, connector, wire, and circuit size, operating voltage, and materials and plating. Power connectors are cataloged along with their associated crimp tooling.

Molex Inc., 2222 Wellington Ct., Lisle, IL 60532; (312) 969-4550. **CIRCLE 357**

COAX INTERCONNECTS AND COMPONENTS

Technical data and pricing on more than 2000 standard items is provided in this informative catalog (#1989a) of coaxial cable, switches, adapters, detectors, connectors, attenuators, terminations, and cable assemblies. The document also covers twinax adapters and connectors, as well as amplifiers, breakouts, cutting and stripping tools, programmable attenuators, push-button attenuators, and waveguide adapters. New products include adapters and connectors that utilize 3.5-mm, 7-mm, HN, N, SMB, SC, and SMA formats.

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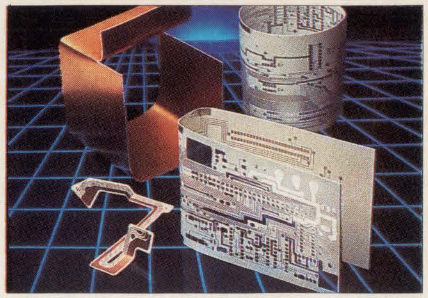

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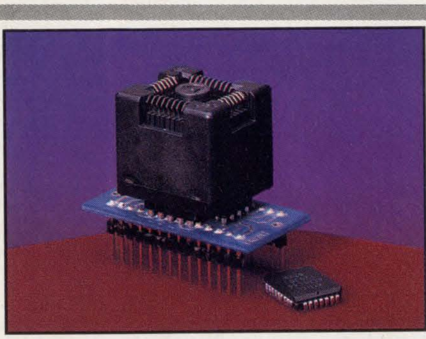

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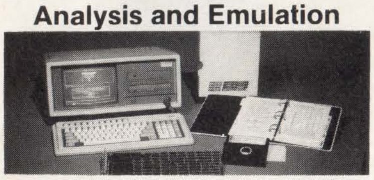

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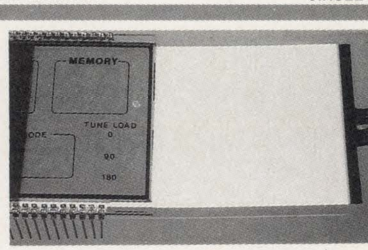

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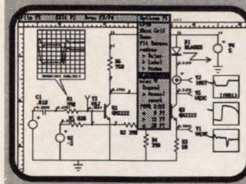

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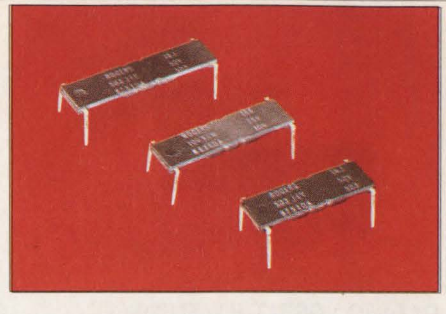

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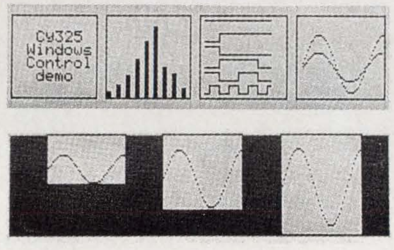

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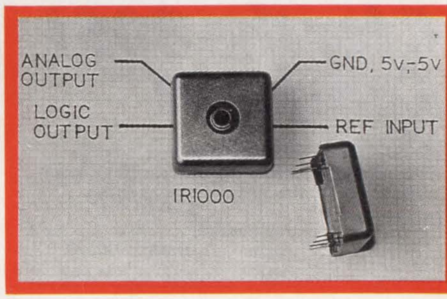

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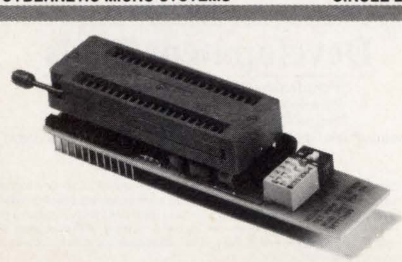

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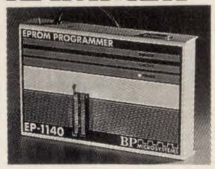

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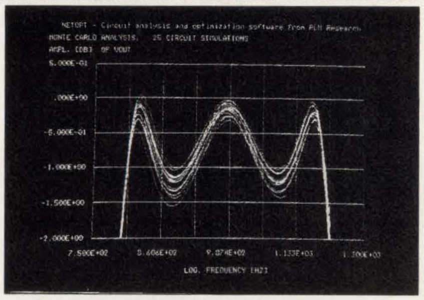

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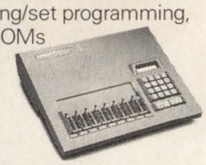

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UPCOMING MEETINGS

SEPTEMBER

1989 ASIC Seminar and Exhibit, September 25-28. Rochester Riverside Convention Center, Rochester, NY. William Bush, 2530 Parker Rd., Palmyra, NY 14522; (716) 244-5830.

Autotestcon '89, September 25-28. Philadelphia, PA. Fred Liguori, Autotestcon '89, P.O. Box 1185, Browns Mills, NJ 08015; (201) 323-2842.

Advanced Composites Conference and Exposition, September 26-28. Hyatt Regency, Dearborn, MI. ASM International, (216) 338-5151.

21st International SAMPE Technical Conference, September 26-28. Atlantic City, NJ. Holly Barnett, R.L. Couch Public Relations, (714) 474-9111.

OCTOBER

IEEE International Conference on Computer Design (ICCD '89), October 2-4. Hyatt Regency, Cambridge, MA. Gail Clanton, Computer Society of the IEEE, (202) 371-1013.

CAM-I's 18th Annual International Conference, October 2-4. Royal Sonesta Hotel, New Orleans, LA. Roger Lewis, CAM-I, 1250 E. Copeland Rd., Ste. 500, Arlington, TX 76011; (817) 860-1654.

Electronic Imaging East '89, October 2-5. Hynes Convention Center, Boston, MA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-3976.

4th Annual PC EXPO, October 3-5. McCormick Place North, Chicago, IL. PC Expo, 385 Sylvan Ave., P.O. Box 1026, Englewood Cliffs, NJ 07632; (201) 569-4147.

IEEE 1989 Ultrasonics Symposium, October 3-6. Montreal, Quebec, Canada. Narendra Batra, Naval Research Laboratory, Washington, D.C. 20375; (202) 767-3505.

FASTEC '89 Conference and Exposition, October 4-5. Sheraton CentrePark Hotel, Arlington, TX. Carol Anderson, Society of Manufacturing Engineers (SME), One SME Dr., P.O. Box 930, Dearborn, MI 48121-0930; (313) 271-1500.

1989 Quality In Electronics (QIE), October 5-7. Red Lion Inn, San Jose, CA. Dawn Onalfo, 1989 QIE Conference, P.O. Box 33015, San Jose, CA 95152; (408) 742-2472.

1989 Linear Applications Seminar, October 16. Red Lion Inn, Bellevue, WA. Dianne Sheppard, National Semiconductor, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052. For additional dates and locations: (408) 721-5000 or (800) 548-4529.

SCAN-TECH '89 International Show and Seminar, October 16-19. New San Jose Convention Center, San Jose, CA. Donald Anderson, Automatic Identification Manufacturers (AIM USA), 1326 Freeport Rd., Pittsburgh, PA 15238; (800) 338-0206 or (412) 963-8588.

Northcon/89, October 17-19. Portland Memorial Coliseum, Portland, OR. Natalie Perlin, Northcon/89, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

Supercomputing World Conference, October 17-20. San Francisco Civic Center, San Francisco, CA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (800) 223-7126 or (617) 232-3976.

International Society for Hybrid Microelectronics (ISHM '89), October 24-26. Baltimore Convention Center, Baltimore, MD. ISHM, P.O. Box 2698, Reston, VA 22090; (703) 471-0066 or (800) 232-4746.

NOVEMBER

DEXPO West '89, November 7-9. Disneyland Hotel, Anaheim, CA. Exposconsul International Inc., 3 Independence Way, Prineton, NJ 08540; (609) 987-9400.

Wescon '89, November 14-16. Moscone Convention Center, San Francisco, CA. Alexes Razevich, IEEE, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

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Isolation(dB)	typ.	min.	typ.	min.
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100-1500MHz	40	28	40	30
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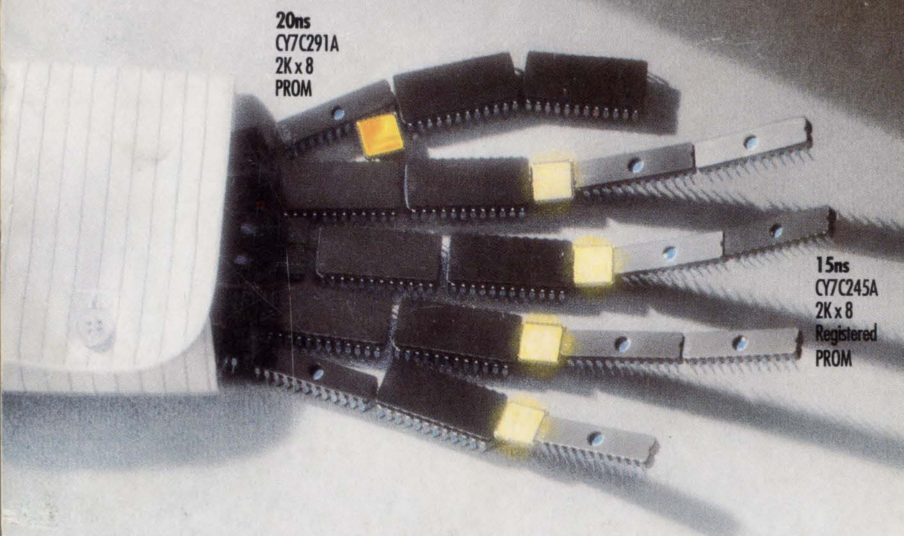

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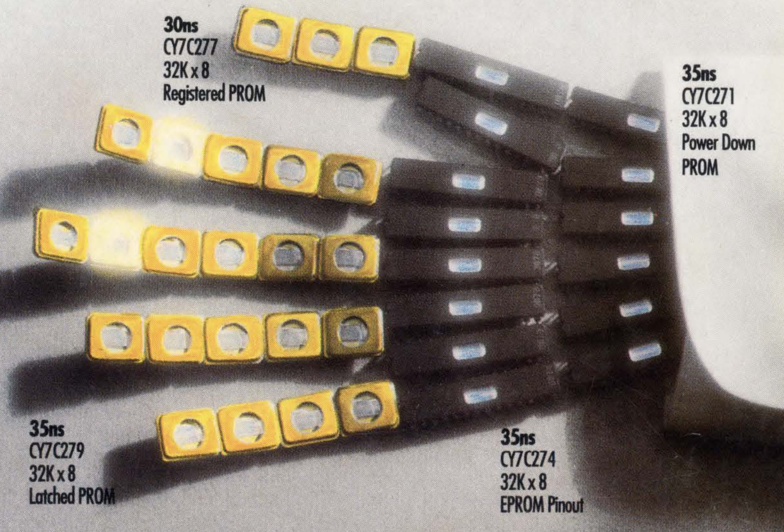

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