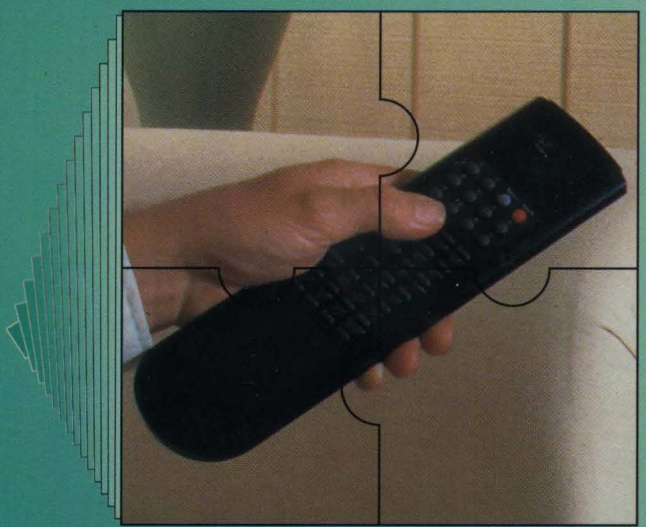
ZiLOG

Infrared Remote Controllers



Includes Specifications and Application Notes for the following parts:

Z86L06	Z86L71
Z86L29	Z86L72
Z86L70	Z86E72

Product Specifications Databook

ZiLOG
Infrared Remote Controllers
Databook

Zilog Infrared Remote Controllers (ZIRC™)

Includes Specifications for the following parts:

- **Z86L06**
- **Z86L29**
- **Z86L70/L71/L72/E72**

Databook

ZIRC™ DATABOOK

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INTRODUCTION

Zilog's Focus on the Hand-Held IR Remote Market
Provides Leading Edge Technology
For Your Entire Product Portfolio.

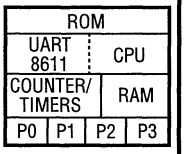
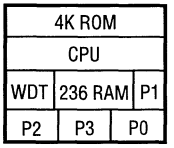
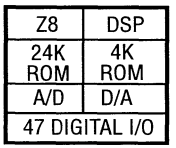
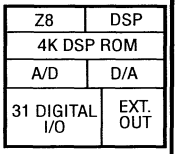
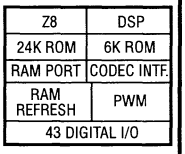
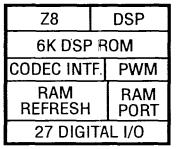
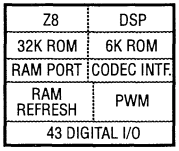
Zilog's low voltage microcontrollers are perfect for all hand-held, battery operated applications where up to 8 MHz operation at 2 volts is required. Regardless of whether your product is low-end, medium range or high-end, Zilog has an IR controller for your application.

Z86L06 Low Voltage CMOS Z8® CCP™ Consumer Controller Processor
The Z86L06 is a 1K ROM MCU, offered in an 18-pin DIP or SOIC package. The device can operate at 2 volts while maintaining 8 MHz functionality. Watch-dog timer, power-on reset, wake-up circuitry, and sleep mode provide the absolute minimum in external circuitry in your application.

Z86L29 6K Infrared Remote (IR) Controller
The Z86L29 is a 6K ROM MCU, offered in an 18-pin DIP or SOIC package. The device can operate at 2 volts while maintaining 8 MHz functionality. As on the Z86L06, watch-dog timer, power-on reset, wake-up circuitry, and sleep mode provide the absolute minimum in external circuitry in your application.

Z86L70/L71/L72/E72 Zilog Infrared Remote Controller Family (ZIRC™)
The Z86L70/71 provides 2K/8K ROM, respectively. The Z86L71 is an 8K ROM MCU, similar to the Z86L29, but with patented counter/timer circuitry which automates the generation and reception of complex pulse/signals used in all types of IR remote control applications.

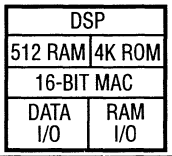
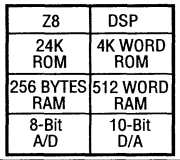
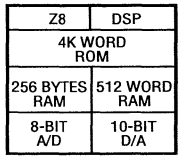
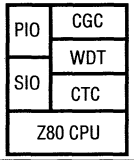
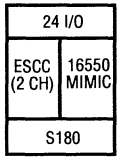
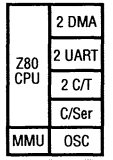
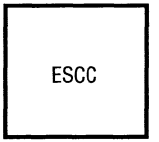
Z86L72 Zilog IR Controller
The Z86L72 provides 16K ROM and is similar to the Z86L71, but with 768 bytes of RAM to store learned codes or data from the receive section of the counter/timers. The Z86L72 is an OTP version for development and small scale production.

Block Diagram							
Part #	**Z08600/Z08611**	**Z86C30/E30 Z86C40/E40**	**Z89C65**	**Z89C66**	**Z89C67**	**Z89C68**	**Z89C69**
Description	Z8® NMOS (CCP™) 8600 = 2K ROM 8611 = 4K ROM	Z8® Consumer Controller Processor (CCP™) with 4K ROM C30 = 28-pin C40 = 40-pin E30/E40 = OTP version	Telephone Answering Controller with DSP LPC voice synthesis and DTMF detection	Telephone Answering Controller with DSP LPC voice synthesis and DTMF detection and external ROM/RAM interface	Telephone Answering Controller with digital voice encode and decode DTMF detection and full memory control interface	Telephone Answering Controller with digital voice encode and decode DTMF detection and external ROM/RAM interface	Telephone Answering Controller with digital voice encode and decode DTMF detection and full memory control interface
Process/Speed	NMOS 8,12 MHz	CMOS 12 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 20 MHz
Features	2K/4K ROM 128 Bytes RAM 22/32 I/O lines On-chip oscillator 2 Counter/Timers 6 vectored, priority interrupts UART (Z8611)	4K ROM, 236 RAM 2 Standby Modes 2 Counter/Timers ROM Protect RAM Protect 4 Ports (86C40/E40) 3 Ports (86C30/E30) Brown-Out Protection 2 Analog Comparators Low EMI Watch-Dog Timer Auto Power-On Reset Low Power option	Z8® Controller 24K ROM 16-bit DSP 4K Word ROM 8-bit A/D with AGC DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available 47 I/O Pins	Z8® Controller 16-bit DSP 4K Word ROM 8-bit A/D with AGC DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available External ROM/RAM capability 31 I/O Pins	Z8® Controller 24K ROM 16-bit DSP 6K Word ROM DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available ARAM/DRAM/ROM Controller & Interface Dual Codec Interface 43 I/O	Z8® Controller 64K ROM (external) 16-bit DSP, 6K word ROM DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available ARAM/DRAM control/ interface External ROM/RAM Dual Codec Interface 27 I/O	Z8® Controller 32K ROM 16-bit DSP 6K Word ROM DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available ARAM/DRAM/ROM Controller & Interface Dual Codec Interface 43 I/O
Package	28-pin DIP 40-pin DIP 44-pin PLCC	28-pin DIP 40-pin DIP 44-pin PLCC, QFP	68-pin PLCC	68-pin PLCC	84-pin PLCC	84-pin PLCC	84-pin PLCC
Application	Low cost tape board TAD	Window Control Wiper Control Sunroof Control Security Systems TAD	Fully featured cassette answering machines with voice prompts and DTMF signaling	General-Purpose DSP applications in TAD and other high-performance 1-tape voice processors	Voice Processing, DSP applications in tapeless TAD and other high-performance 1-tape voice processors	Voice Processing, DSP applications in tapeless TAD and other high-performance 1-tape voice processors	Voice Processing, DSP applications in tapeless TAD and other high-performance 1-tape voice processors

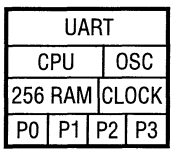
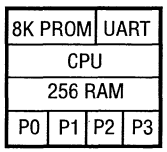
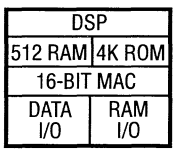
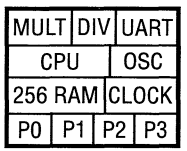
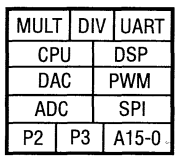
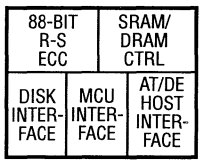
ZiLOG Video Products — Superintegration™ Products Guide

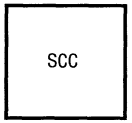
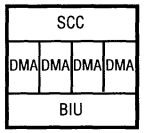
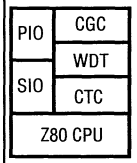
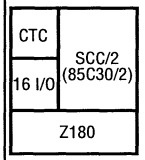
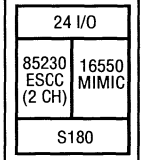
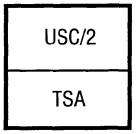
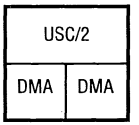
	TV Controller			IR Controller		Cable TV	
Block Diagram	8K ROM / 4K CHAR ROM / Z8 CPU | RAM / OSD / 13 PWM | TIMER WDT | 5 PORTS	6K ROM / 3K CHAR ROM / Z8 CPU | RAM / OSD / 7 PWM | TIMER WDT | 3 PORTS	CHAR ROM / COMMAND INTERPRETER / ANALOG SYNC/DATA SLICER | OSD CTRL	1K/6K ROM / Z8 CPU / WDT | 124 RAM / P2 | P3	2K/8K/16K ROM / Z8 CPU / WDT | 128,256, 768 RAM / P0 | P1 | P2 | P3	4K ROM / CPU / WDT | 236 RAM | P1 / P2 | P3 | P0	16K ROM | UART / CPU | 236 RAM / P0 | P1 | P2 / P3 | P4 | P5 | P6
Part #	**Z86C27/127/97**	**Z86227**	**Z86128**	**Z86L06/L29**	**Z86L70/71/72** (Q193)	**Z86C40/E40**	**Z86C61/62**
Description	Z8® Digital Television Controller MCU with logic functions needed for Television Controller, VCRs and Cable	Standard DTC features with reduced ROM, RAM, PWM outputs for greater economy	Line 21 Controller (L21C™) for Closed Caption Television	18-pin Z8® Consumer Controller Processor (CCP™) low-voltage and low-current battery operation 1K-6K ROM	Z8® (CCP™) low-voltage parts that have more ROM, RAM and special Counter/Timers for automated output drive capabilities	Z8® Consumer Controller Processor (CCP™) with 4K ROM (C40) E40 = OTP version	Z8® MCU with Expanded I/O's and 16K ROM
Process/Speed	CMOS 4 MHz	CMOS 4 MHz	CMOS 12 MHz	Low Voltage CMOS 8 MHz	Low Voltage CMOS 8 MHz	CMOS 12 MHz	CMOS 16, 20 MHz
Features	Z8/DTC Architecture 8K ROM, 256-byte RAM 160x7-bit video RAM On-Screen Display (OSD) video controller Programmable color, size, position attributes 13 PWMs for D/A conversion 128-character set 4Kx6-bit char. Gen. ROM Watch-Dog Timer (WDT) Brown-Out Protection 5 Ports/36 pins 2 Standby Modes Low EMI Mode	Z8/DTC Architecture 6K ROM, 256-byte RAM 120x7-bit video RAM OSD on board Programmable color, size, position attributes 7 PWMs 96-character set 3Kx6-bit character generator ROM Watch-Dog Timer (WDT) Brown-Out Protection 3 Ports/20 pins 2 Standby Modes Low EMI Mode	Conforms to FCC Line 21 format Parallel or serial modes Stand-alone operation On-board data sync and slicer On-board character generator - Color - Blinking - Italic - Underline	Z8® Architecture 1K ROM & 6K ROM Watch-Dog Timer 2 Analog Comparators with output option 2 Standby Modes 2 Counter/Timers Auto Power-On Reset 2 volt operation RC OSC option Low Noise option Brown-Out Protection High current drivers (2, 4)	Z8® Architecture 2K/8K/16K ROM Watch-Dog Timer 2 Analog Comparators with output option 2 Standby Modes 2 Enhanced Counter/Timers, Auto Pulse Reception/Generation Auto Power-On Reset 2 volt operation RC OSC option Brown-Out Protection High current drivers (4)	4K ROM, 236 RAM 2 Standby Modes 2 Counter/Timers ROM Protect RAM Protect 4 Ports Brown-Out Protection 2 Analog Comparators Low EMI Watch-Dog Timer Auto Power-On Reset Low Power option	16K ROM Full duplex UART 2 Standby Modes (STOP and HALT) 2 Counter/Timers ROM Protect option RAM Protect option Pin compatible to Z86C21 C61 = 4 Ports C62 = 7 Ports
Package	64-pin DIP 52-pin active (127)	40-pin DIP	18-pin DIP	18-pin DIP 18-pin SOIC	20-pin DIP (L71), 18-pin DIP, SOIC (L70) 40,44-pin DIP, PLCC, QFP (L72)	40-pin DIP	40-pin DIP (C61) 44-pin PLCC,QFP (C61) 68-pin PLCC (C62)
Application	Low-end Television Cable/Satellite Receiver	Low-end Television Cable/Satellite Receiver	TVs, VCRs, Decoders	I.R. Controller Portable battery operations	I.R. Controller Portable battery operations	Window Control Wiper Control Sunroof Control Security Systems TAD	Cable Television Remote Control Security

Fax/Modem Superintegration™ Products Guide

	Data Pump	Single Chip		Controllers			
Block Diagram							
Part #	**Z89C00**	**Z89120**	**Z89920**	**Z84C15**	**Z80182**	**Z80180**	**Z85230**
Description	16-Bit Digital Signal Processor	Zilog Modem/Fax Controller (ZMFC)	Zilog Modem/Fax Controller (ZMFC)	IPC/EIPC Controller	Zilog Intelligent Peripheral (ZIP™)	High-performance Z80® CPU with peripherals	Enhanced Serial Com. Controller
Process/Speed	CMOS 10, 15 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 6, 10,16 MHz	CMOS 16, 20 MHz	6, 8, 10, 16*, 20* *Z8S180 only	CMOS 8, 10,16, 20 MHz
Features	16-bit Mac 75 ns 2 data RAMs (256 words each) 4K word ROM 64Kx16 Ext. ROM 16-bit I/O Port 74 instructions Most single cycle Two conditional branch inputs, two user outputs Library of software macros available zero overhead pointers	Z8® controller with 24 Kbyte ROM 16-bit DSP with 4K word ROM 8-bit A/D 10-bit D/A (PWM) Library of software macros available 47 I/O pins Two comparators Independent Z8® and DSP Operations Power-Down Mode	Z8 w/64K external memory DSP w/4K word ROM 8-bit A/D 10-bit D/A Library of macros 47 I/O pins Two comparators Independent Z8® and DSP Operations Power-Down Mode	Z80® CPU, SIO, CTC WDT, CGC The Z80 Family in one device Power-On Reset Two chip selects 32-bit CRC WSG EV mode[1] 3 and 5 Volt Version	Complete Static Version of Z180™ plus ESCC (2 channels of Z85230) 16550 MIMIC 24 Parallel I/O Emulation Modes[1]	Enhanced Z80® CPU MMU 1 Mbyte 2 DMAs 2 UARTs with BRGs C/Serial I/O Port Oscillator Z8S180 includes: Pwr dwn, Prgmble EMI, divide-by-one clock option	Full dual-channel SCC plus deeper FIFOs: 4 bytes on Tx 8 bytes on Rx DPLL counter per channel Software compatible to SCC
Package	68-pin PLCC 60-pin VQFP	68-pin PLCC	68-pin PLCC	100-pin QFP 100-pin VQFP	100-pin QFP 100-pin VQFP	64-pin DIP 68-pin PLCC 80-pin QFP	40-pin DIP 44-pin PLCC
Other Applications	16-bit General-Purpose DSP TMS 32010/20/25 applications	Multimedia-Audio Voicemail Speech Storage and Transmission Modems FAXes, Sonabouys	Multimedia-Audio Voicemail Speech Storage and Transmission Modems FAXes, Sonabouys	Intelligent peripheral controllers Modems	General-Purpose Embedded Control Modem, Fax, Data Communications	Embedded Control	General-Purpose datacom. High performance SCC software compatible upgrade

Mass Storage Superintegration™ Products Guide

Block Diagram						
Part #	**Z86C91/Z8691**	**Z86E21**	**Z89C00**	**Z86C93**	**Z86C95**	**Z86018**
Description	ROMless Z8®	Z8® 8K OTP	16-Bit Digital Signal Processor	Enhanced Z8®	Enhanced Z8® with DSP	Zilog Datapath Controller (ZDPC)
Process/Speed	CMOS 16 MHz (C91) NMOS 12 MHz (91)	CMOS 12, 16 MHz	CMOS 10, 15 MHz	CMOS 20, 25 MHz	CMOS 24 MHz	CMOS 40 MHz
Features	Full duplex UART 2 Standby Modes (STOP and HALT) 2x8 bit Counter/Timer	8K OTP ROM 256 Byte RAM Full-duplex UART 2 Standby Modes (STOP and HALT) 2 Counter/Timers ROM Protect option RAM Protect option Low EMI option	16-bit Mac 75 ns 2 data RAMs (256 words each) 4K word ROM 64Kx16 Ext. ROM 16-bit I/O Port 74 instructions Most single cycle Two conditional branch inputs, two user outputs Library of software macros available zero overhead pointers	16x16 Multiply 1.7 µs 32x16 Divide 2.0 µs Full duplex UART 2 Standby Modes (STOP and HALT) 3 16-bit Counter/Timers Pin compatible to Z86C91 (PDIP)	8 channel 8-bit ADC, 8-bit DAC 16-bit Multiply/Divide Full duplex UART SPI (Serial Peripheral Interface) 3 Standby Modes (STOP/HALT/PAUSE) Pulse Width Modulator 3x16-bit timer 16-bit DSP slave processor 83 ns Mult./Accum.	Full track read Automatic data transfer (Point & Go®) 88-bit Reed Solomon ECC "on the fly" Full AT/IDE bus interface 64 KB SRAM buffer 1 MB DRAM buffer Split data field support 100-pin VQFP package JTAG boundary scan option Up to 8 KB buffer RAM reserved for MCU
Package	40-pin DIP 44-pin PLCC 44-pin QFP	40-pin DIP 44-pin PLCC 44-pin QFP	68-pin PLCC 60-pin VQFP	40-pin DIP 44-pin PLCC 44-pin QFP 48-pin VQFP	80-pin QFP 84-pin PLCC 100-pin VQFP	100-pin VQFP 100-pin QFP
Application	Disk Drives Modems Tape Drives	Software Debug Z8® prototyping Z8® production runs Card Reader	Disk Drives Tape Drives Servo Control Motor Control	Disk Drives Tape Drives Modems	Disk Drives Tape Drives Servo Control Motor Control	Hard Disk Drives

Block Diagram									
Part #	**Z8030/Z80C30 Z8530/Z85C30**	**Z85230/Z80230 Z85233***	**Z16C35**	**Z84C15**	**Z80181**	**Z80182**	**Z16C30**	**Z16C33**	**Z16C32**
Description	Serial Com. Controller	Enhanced Serial Com. Controller	Integrated Serial Com. Controller	Intelligent Peripheral Controller	Smart Access Controller	Zilog Intelligent Peripheral	Universal Serial Controller	Mono-channel Universal Serial Controller	Integrated Universal Serial Controller
Process/ Speed/ Clock Data Rate	NMOS: 4, 6, 8 MHZ CMOS: 8,10 16 MHz 2, 2.5, 4 Mb/s	CMOS: 10, 16 20 MHz 2.5, 4.0, 5.0 Mb/s	CMOS: 10, 16 MHz 2.5, 4.0 Mb/s	CMOS 6, 10,16 MHz	10, 12.5	CMOS 16, 20 MHz	CMOS: 20 MHz CPU Bus 10 Mb/s 20 Mb/s	CMOS: 10 MHz CPU Bus 10 Mb/s	CMOS:20 MHz CPU Bus 16 Mb/s 20 Mb/s
Features	Two independent full-duplex channels Enhanced DMA support: 10x19 status FIFO 14-bit byte counter NRZ/NRZI/FM	Full dual-channel SCC plus deeper FIFOs: 4 bytes on Tx 8 bytes on Rx DPLL counter per channel Software compatible to SCC *One channel of Z85230	Full dual-channel SCC plus 4 DMA controllers and a bus interface unit	Z80® CPU, SIO, CTC WDT, CGC The Z80 Family in one device Power-On Reset Two chip selects 32-bit CRC WSG EV mode[1] 3 and 5 Volt Version	Complete Z180™ plus SCC/2 CTC 16 I/O lines Emulation Mode[1]	Complete Static version of Z180 plus ESCC (2 channels of 85230) 16550 MIMIC 24 Parallel I/O Emulation Mode[1]	Two dual-channel 32-byte receive & transmit FIFOs 16-bit bus B/W: 18.2 Mb/s 2 BRGs per channel Flexible 8/16-bit bus interface	Single-channel (half of USC™) plus Time Slot Assigner functions for ISDN	Single-channel (half of USC) plus two DMA controllers Array chained and linked-list modes with ring buffer support
Package	40-pin DIP 44-pin CERDIP 44-pin PLCC	40-pin DIP 44-pin PLCC *44-pin QFP (85233)	68-pin PLCC	100-pin QFP 100-pin VQFP	100-pin QFP	100-pin QFP 100-pin VQFP	68-pin PLCC	68-pin PLCC	68-pin PLCC
Application	General-Purpose datacom.	General-Purpose datacom. High performance SCC software	High performance datacom. SCC upgrades	Intelligent peripheral controllers Modems	Intelligent peripheral controllers Printers, Faxes, Modems, Terminals	General-Purpose Embedded Control Modem, Fax, Data Communications	General-Purpose high-end datacom. Ethernet HDLC X.25 Frame Relay	General-Purpose high-end datacom. Ethernet HDLC X.25 Frame Relay	General-Purpose high-end datacom. Ethernet HDLC X.25 Frame Relay

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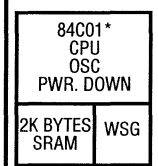
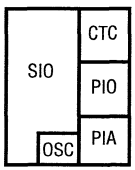
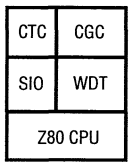
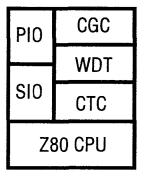
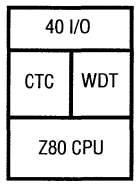
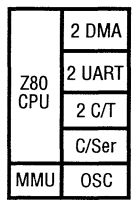
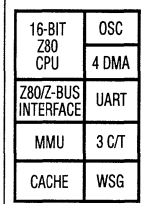
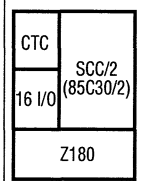
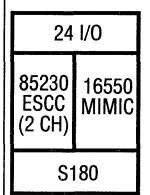
Z80® Embedded Controllers Superintegration™ Products Guide

	Z84C50	Z84C90	Z84013/C13	Z84015/C15	Z84011/C11	Z80180/S180	Z80280	Z80181	Z80182
Block Diagram									
Part #									
Description	Z80/84C01 with 2K SRAM	Killer I/O (3 Z80 peripherals)	Intelligent Peripheral Controller	Intelligent Peripheral Controller	Parallel I/O Controller	High-performance Z80® CPU with peripherals	16-bit Z80® code compatible CPU with peripherals	Smart Access Controller	Zilog Intelligent Peripheral
Speed MHz	10	8, 10, 12.5	6, 10	6, 10, 16	6, 10	6, 8, 10, 16*, 20* *Z8S180 only	10, 12	10, 12.5	16, 20
Features	Z80® CPU 2 Kbytes SRAM WSG Oscillator Pin compatible with Z84C00 DIP & PLCC EV mode[1] *84C01 is available as a separate part	SIO, PIO, CTC plus 8 I/O lines	Z80® CPU, SIO, CTC WDT, CGC, WSG, Power-On Reset 2 chip selects EV mode[1]	Z80® CPU, SIO, CTC WDT, CGC The Z80 Family in one device Power-On Reset Two chip selects 32-bit CRC WSG EV mode[1]	Z80® CPU, CTC, WDT 40 I/O lines bit programmable Power-On Reset EV mode[1]	Enhanced Z80 CPU MMU 1 Mbyte 2 DMAs 2 UARTs with BRGs C/Serial I/O Port Oscillator Z8S180 includes; Pwr dwn, Prgmble EMI, divide-by-one clock option	16-bit code compatible Z80® CPU Three stage pipeline MMU 16 Mbyte CACHE 256 byte Inst. & Data Peripherals 4 DMAs, UART, 3 16-bit C/T, WSG Z80/Z-BUS® interface	Complete Z180 plus SCC/2 CTC 16 I/O lines Emulation Mode[1]	Complete Static Version of Z180™ plus ESCC (2 channels of Z85230) 16550 MIMIC 24 Parallel I/O Emulation Modes[1]
Package	40-pin DIP 44-pin PLCC 44-pin QFP	84-pin PLCC	84-pin PLCC	100-pin QFP 100-pin VQFP	100-pin QFP	64-pin DIP 68-pin PLCC 80-pin QFP	68-pin PLCC	100-pin QFP	100-pin QFP 100-pin VQFP
Application	Embedded Controllers	General-purpose peripheral that can be used with Z80 and other CPU's	Intelligent datacom controllers	Intelligent peripheral controllers Modems	Intelligent parallel-I/O controllers Industrial display terminals	Embedded Control	Embedded Control Terminals Printers	Intelligent peripheral controllers Printers, Faxes, Modems, Terminals	General-Purpose Embedded Control Modem, Fax, Data Communications

[1] Allows use of existing development systems.

	Z8036 Z8536	Z32H00	Z5380 Z53C80	Z85C80
Description	Counter/Timer & parallel I/O Unit (CIO)	Hyperstone Enhanced Fast Instruction Set Computer (EFISC) Embedded (RISC) Processor	Small Computer System Interface (SCSI)	Serial Communication Controller and Small Computer System Interface
Process/ Speed	NMOS 4,6 MHz	CMOS 25 MHz	CMOS Z5380: 1.5 MB/s Z53C80: 3.0 MB/s	CMOS SCC - 10, 16 MHz SCSI - 3.0 MB/s
Features	Three 16-bit Counter/Timers, Three I/O ports with bit catching, pattern matching interrupts and handshake I/O	32-bit MPU 4 Gbytes address space 19 global and 64 local registers of 32 bits each 128 bytes instruction cache 1.2μ CMOS 42 mm^2 die	ANSI X3.131-1986 Direct SCSI bus interface On-board 48 mA drivers Normal or Block mode DMA transfers Bus interface, target and initiator	Full dual-channel SCC plus SCSI sharing databus and read/write functions
Package	40-pin PDIP 44-pin PLCC	144-pin PGA 132-pin QFP	Z5380: 40-pin DIP 44-pin PLCC Z53C80: 48-pin DIP 44-pin PLCC	68-pin PLCC
Application	General-Purpose Counter/Timers and I/O system designs	Embedded high-performance industrial controller Workstations	Bus host adapters, formatters, host ports	AppleTalk® networking SCSI disk drives

[2] Software and hardware compatible with discrete devices.

Z86L06

LOW VOLTAGE CMOS Z8® CCP™ CONSUMER CONTROLLER PROCESSOR

FEATURES

- 8-Bit CMOS Microcontroller
- 18-Pin DIP and 18-Pin SOIC Packages
- Low Cost
- 2.0V to 3.6V Operating Range
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines (Three with Comparator Inputs)
- 1 Kbyte of ROM
- 124 Bytes of RAM
- Four Expanded Registers (File Control Registers)
- Two Programmable 8-Bit Counter/Timers
- Two 6-Bit Programmable Prescalers
- Six Vectored, Priority Interrupts from Five Different Sources
- Clock Speed 8 MHz @ 2.0V
- Watch-Dog/Power-On-Reset Timer
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Low EMI Noise Mode
- From 0°C to +70°C Operating Temperature
- ROM Protect

GENERAL DESCRIPTION

The Z86L06 low voltage CCP (Consumer Controller Processor) is a member of the Z8 single-chip microcontroller family with 1 Kbyte of ROM, and 124 bytes of general-purpose RAM. The device is packaged in an 18-pin DIP and 18-pin SOIC, and is manufactured in low voltage CMOS technology. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion, along with low cost and low power consumption. Now with the low voltage process, this same processor may operate down to 2.0V.

The Z86L06 architecture is based on Zilog's 8-bit microcontroller core with the addition of an Expanded Register File which allows access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many consumer, industrial, automotive, and advanced scientific applications.

The device applications demand powerful I/O capabilities. The CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of general-purpose registers, two I/O port registers, and 15 control and status registers. The Expanded Register File consists of three control registers.

With powerful peripheral features such as on-board comparators, counter/timers, and watch-dog timer, the Z86L06 meets the needs for most sophisticated controller applications (Figure 1).

GENERAL DESCRIPTION (Continued)

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

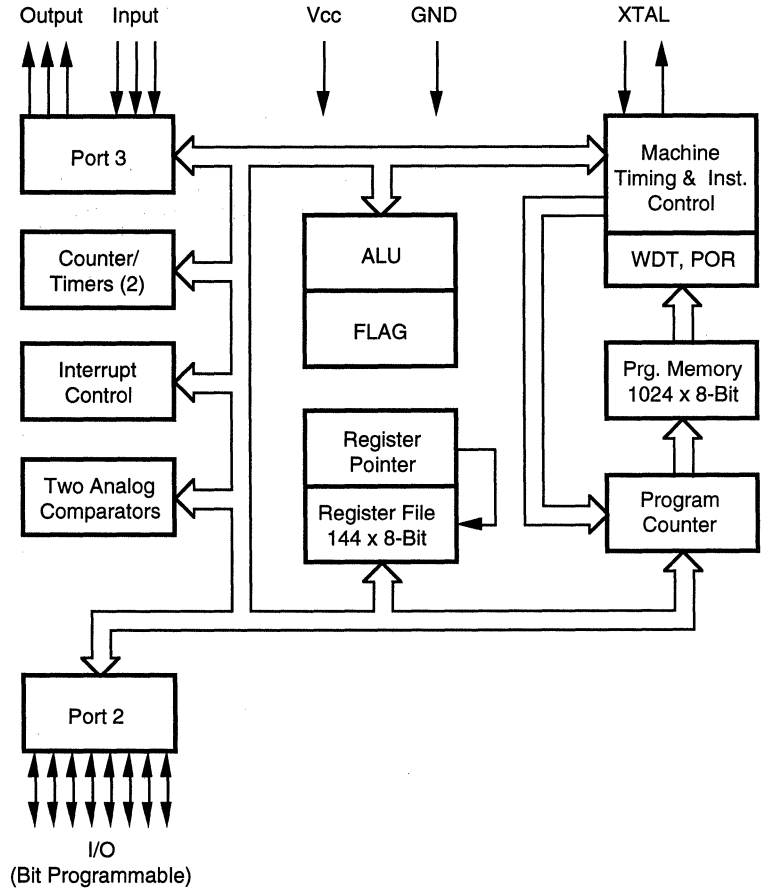


Figure 1. Z86L06 Functional Block Diagram

PIN DESCRIPTION

Table 1. 18-Pin DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-P27	Port 2, pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-P33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-P36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-P23	Port 2, pins 0, 1, 2, 3	In/Output

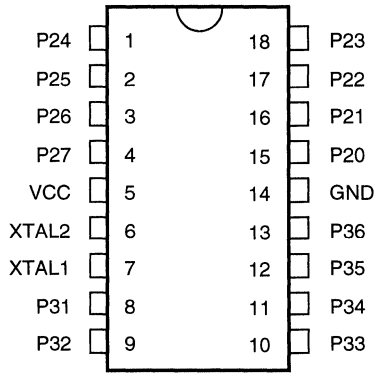


Figure 2. DIP and SOIC Pin Configuration

PIN FUNCTIONS

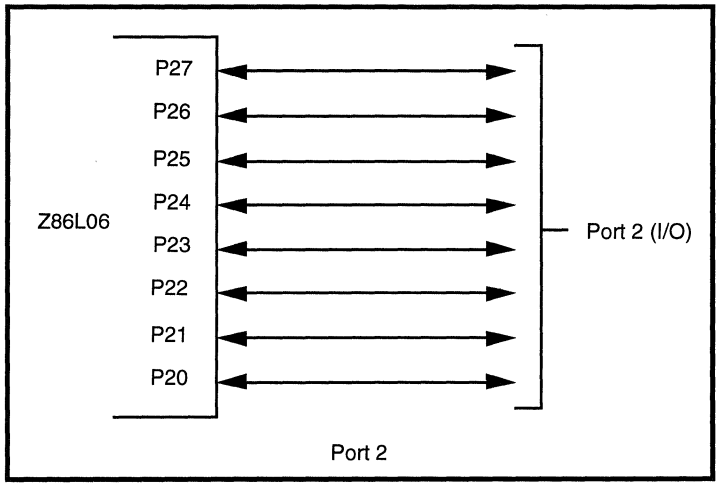
XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2. (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 3).

Port 3 (P36-P31). Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P33-P31) and three fixed outputs (P36-P34). Pins P31, P32, and P33 are standard CMOS inputs and pins P34, P35, and P36 are push-pull outputs. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (bit 1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer1 is made through P31 (T_{IN}) and P36 (T_{OUT}). (Figures 4 and 5).

PIN FUNCTIONS (Continued)



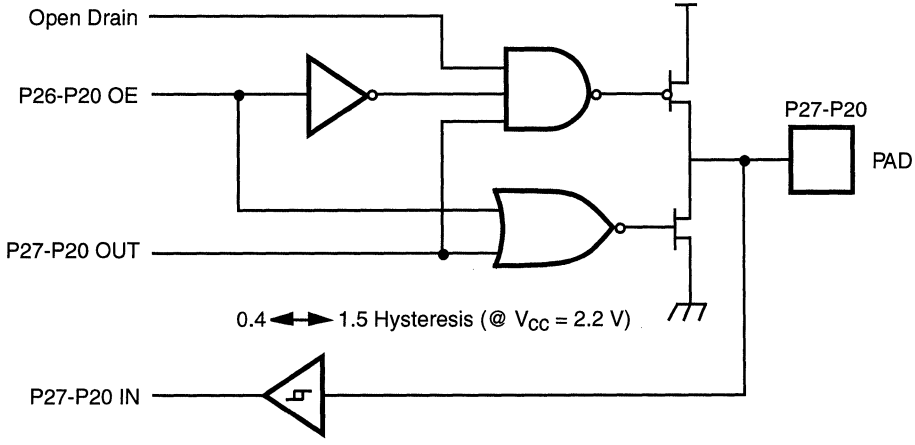
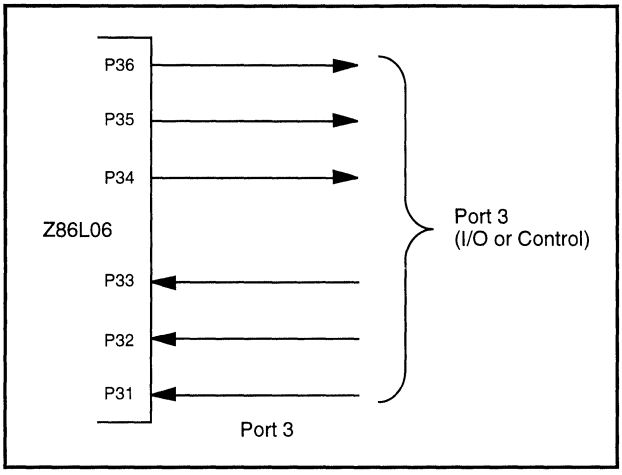


Figure 3. Port 2 Configuration



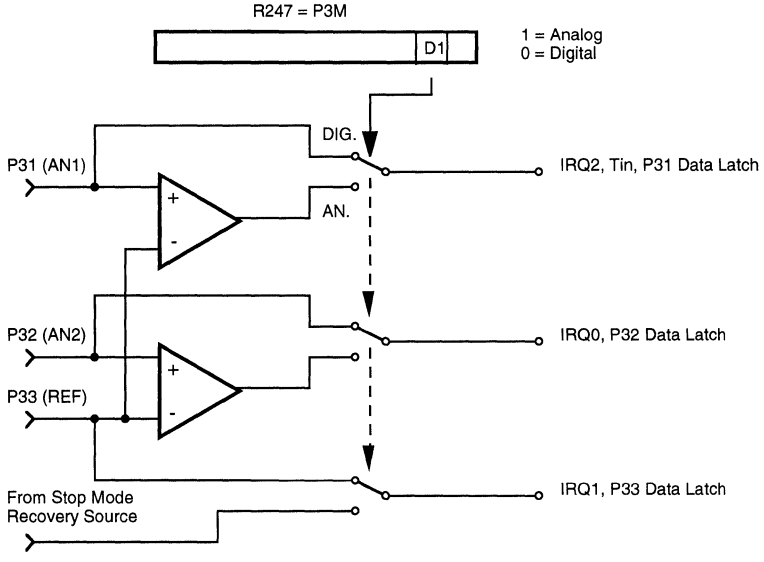


Figure 4. Port 3 Configuration

PIN FUNCTIONS (Continued)

Port Configuration Register (PCON). The Port Configuration Register (PCON) configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 6). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35 (Figure 5), and a 0 releases the Port to its standard I/O configuration. Bits 5 and 6 of this register configure Ports 2 and 3, respectively, for low EMI operation. A 1 in these locations configures the port for standard operation, and a 0 configures the port for low EMI operation. Finally, bit 7 of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. Note that the PCON Register is reset upon the occurrence of a Stop-Mode Recovery, any WDT Reset, and Power-On Reset.

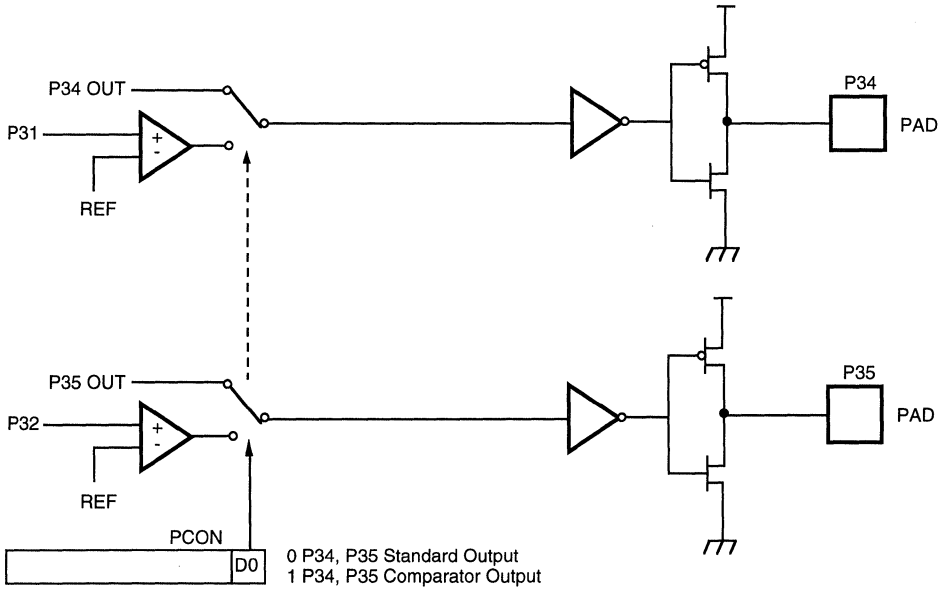
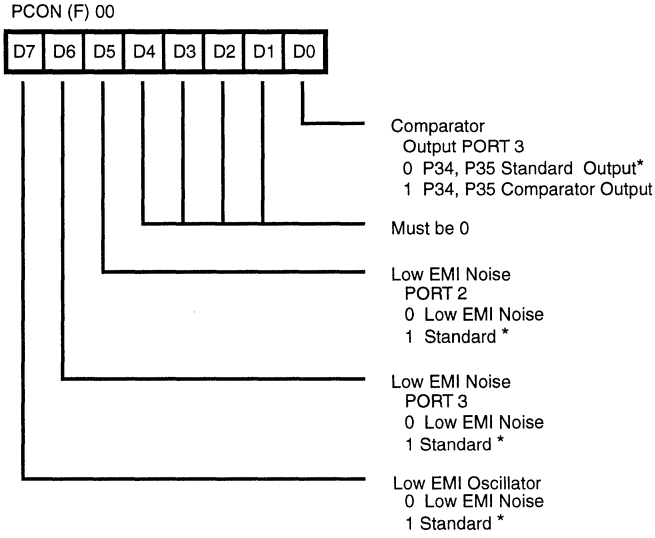


Figure 5. Port 3 Configuration

Low EMI Option. The Z86L06 can be programmed to operate in a low EMI emission mode by the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- Low current consumption during the HALT mode.
- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 800 Ohms (typical).
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz (250 ns cycle time).

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. The internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 source (Figure 6).



* Default setting from Stop-Mode Recovery, Power-On Reset, and any WDT Reset.

Figure 6. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION

The Z86L06 CCP is based on Zilog's core which incorporates special functions to enhance the Z8® MCU's application in consumer, automotive, industrial, scientific research, and advanced technologies applications.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery source

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. Z86L06 can address up to 1 Kbyte of internal program memory (Figure 7). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 13 to 1023 consist of on-chip, mask-programmed ROM.

ROM Protect. The 1 Kbyte of Program Memory is mask programmable. A ROM protect feature will prevent dumping of the ROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 8). These register groups are known as the ERF (Expanded Register File). Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 9). Three system configuration registers reside in the Expanded Register File address space in Bank F. The rest of the Expanded Register addressing space is not physically implemented, and is open for future expansion. To write to the ERF, the upper nibble of the RP must be zero. To write to the rest of the register file, the lower nibble must be zero.

Note: When using Zilog's Cross Assembler version 2.1 or earlier, use theLD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

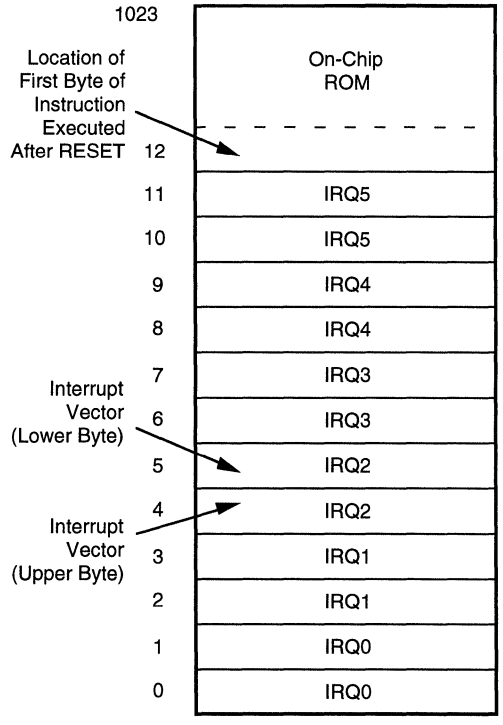


Figure 7. Program Memory Map

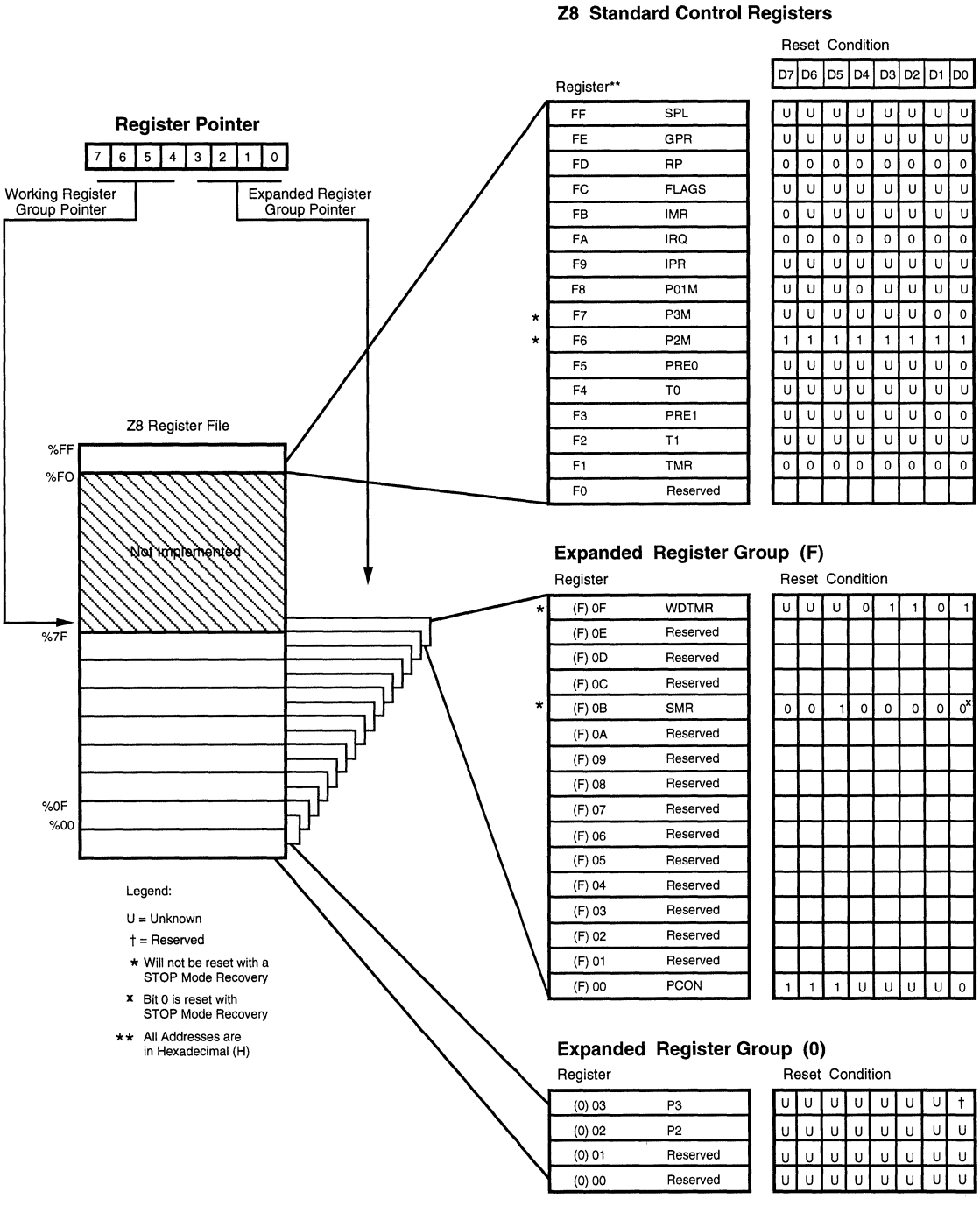
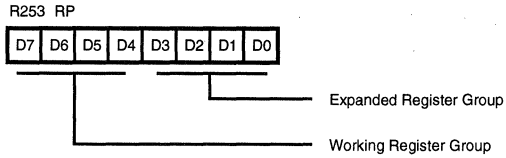


Figure 8. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)



Note: Default Setting After Reset = 00000000

Figure 9. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 124 general purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 8). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 10). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed through working registers and indirect addressing modes.

Caution: D4 of Control Register P01M (R251) must be 0. If the Z86L06 is emulated by Z86C90, D4 of P01M has to change to 0 before submission to ROM code.

GPR. The Z86L06 has one extra general purpose register located at FEH (R254).

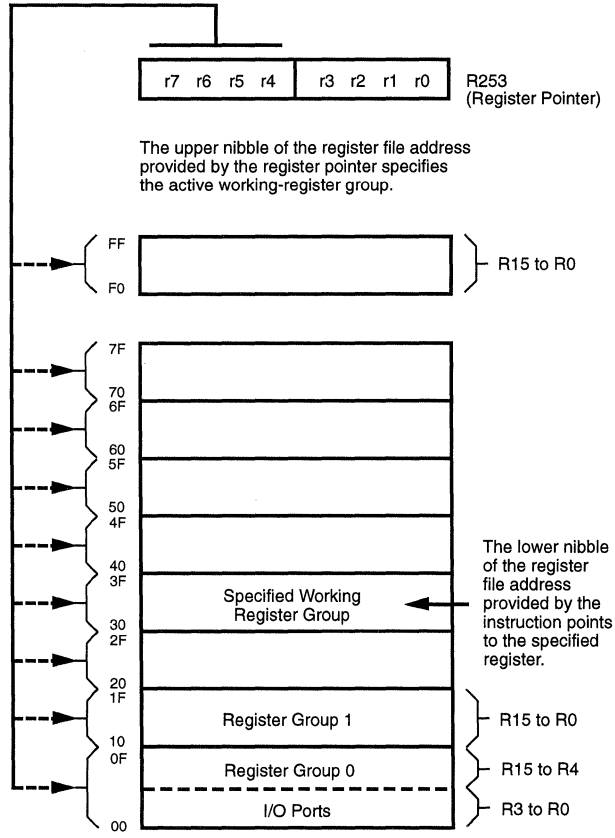


Figure 10. Register Pointer

Stack. The Z86L06 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T1-T0), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 11).

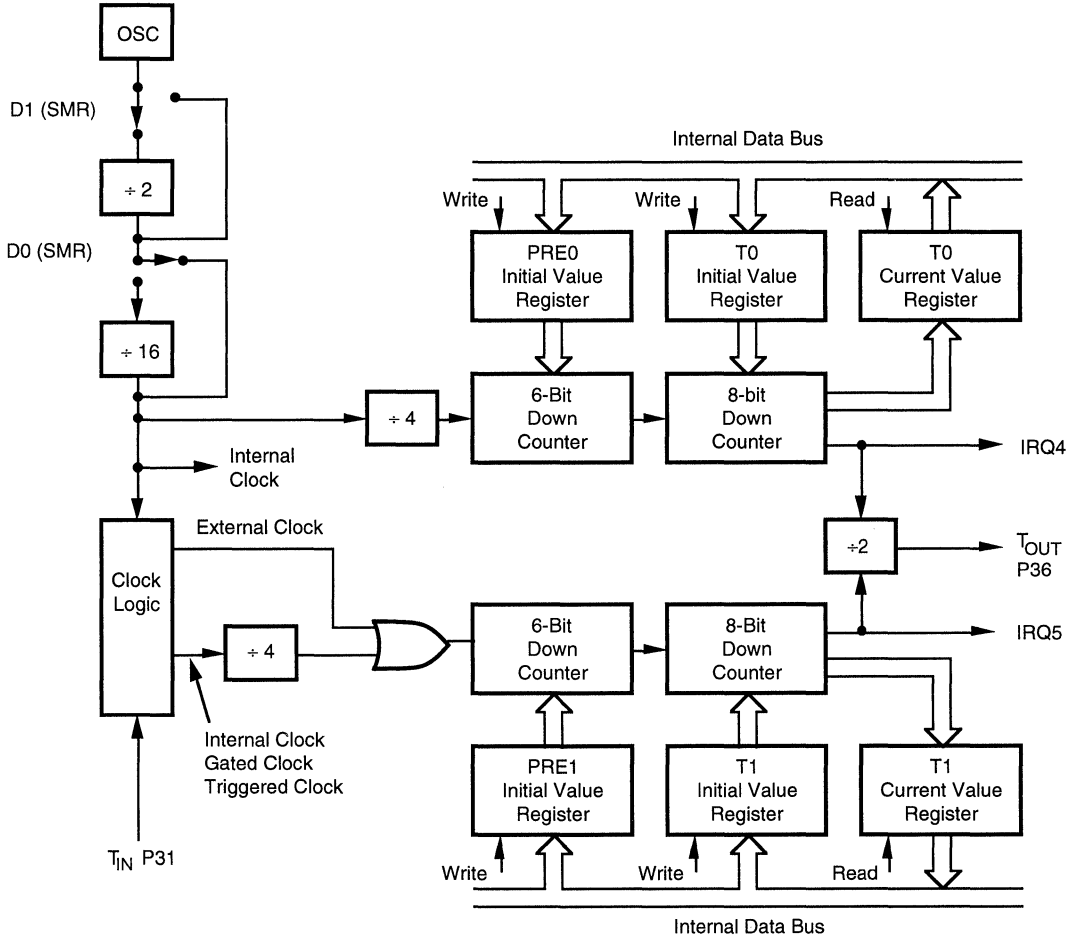


Figure 11. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z86L06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows; three sources are claimed by Port 3 lines P33-P31, two sources in the counter/timers, and one source by software. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

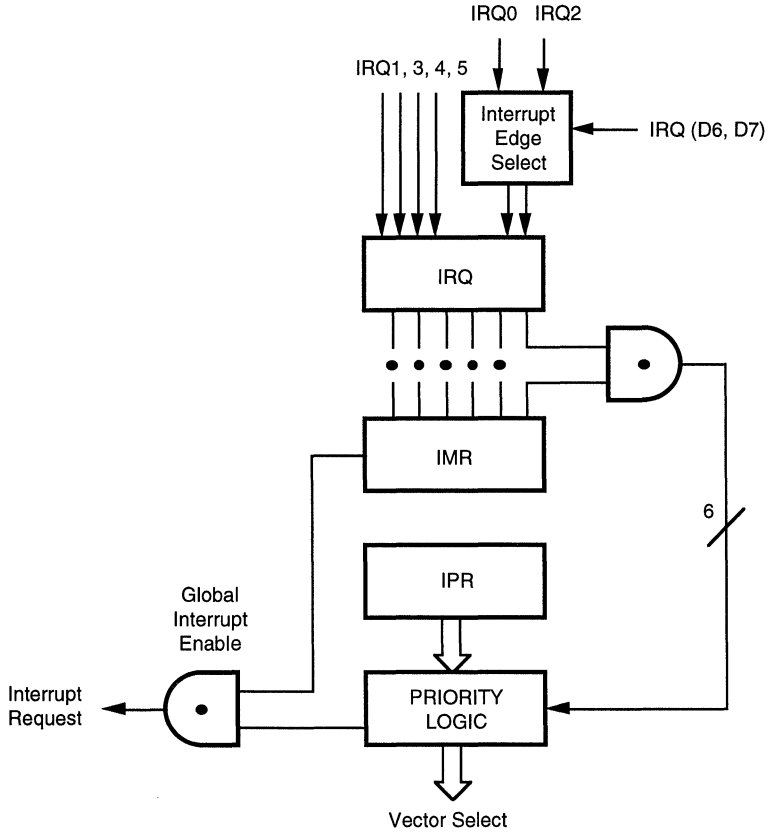


Figure 12. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	IRQ2, T_{IN}	4, 5	External (P31), Rising Falling Edge Triggered
IRQ3		6, 7	Software Generated
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs services. IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register).

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the Interrupt Edge Select are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86L06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 4 MHz or 8 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal is connected across XTAL1 and XTAL2 using the supplier's recommended capacitors (normally C1 = C2 is more than or equal to 22 pF) from each pin to V_{SS} (pin 14) of Z86L06. The RC oscillator option is mask-programmable, to be selected by the customer at the time the ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to V_{SS} (pin 14) of Z86L06 (Figure 13).

FUNCTIONAL DESCRIPTION (Continued)

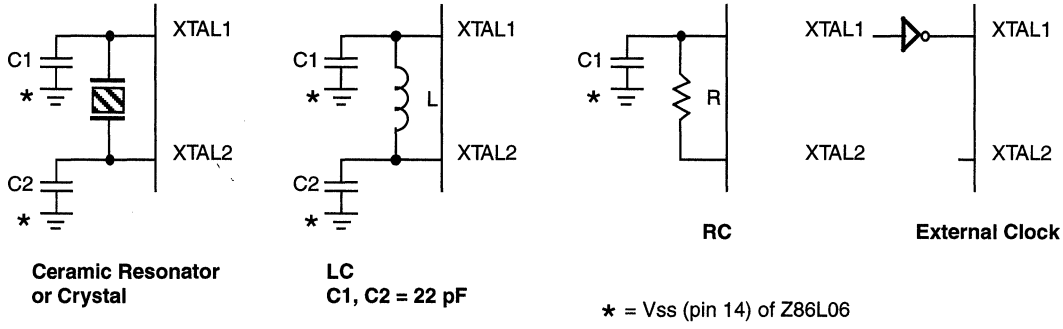


Figure 13. Oscillator Configuration

A special feature has been incorporated into the Z86L06. In low EMI noise mode (bit 7 of PCON register = 0) with the RC option selected, the oscillator is targeted to consume considerably less I_{CC} current at frequencies of 10 kHz or less.

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the Power-On Reset timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR = 1)
- WDT Time-Out

The POR time is 4 ms minimum at V_{CC} = 3.6V. Bit 5 of the STOP mode register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 15 µA (typical) or less. The STOP mode is terminated by a RESET of either WDT time-out, POR, or SMR recovery. This causes the processor to restart the application program at address 000CH.

Note: The crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF    NOP     ; clear the pipeline
6F    STOP    ; enter STOP mode
              or
FF    NOP     ; clear the pipeline
7F    HALT    ; enter HALT mode
```

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 14). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the Stop-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK.

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic). Note that bit 0 (D0) is reset from WDT time out, POR, or SMR recovery.

XTAL Clock divide-by-2 (D1). This bit determines whether the XTAL clock is divided by two or one. When this bit is set to 1, the SCLK/TCLK is equal to the XTAL clock. This option can work together with the low EMI options in PCON register to reduce the EMI noise. Maximum frequency is 4 MHz when divide-by-one selection is active.

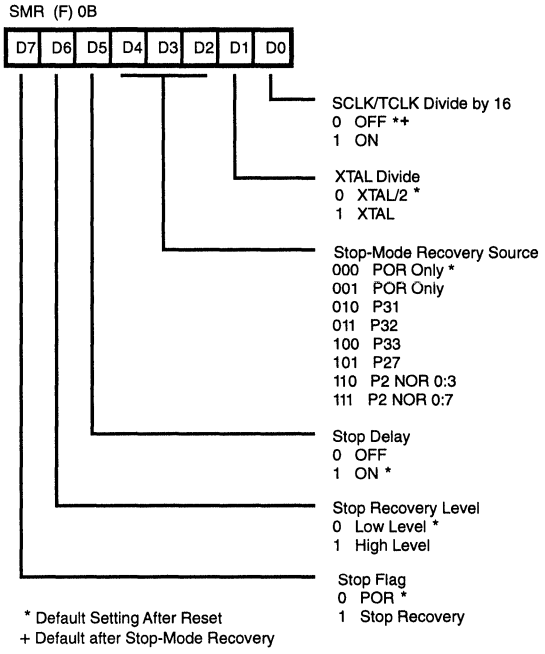


Figure 14. Stop-Mode Recovery Register (Write Only, except bit 7)

FUNCTIONAL DESCRIPTION (Continued)

Stop-Mode Recovery Source (D4-D2). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 15 and Table 4).

Table 4. Stop-Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2, bits 0-3
1	1	1	Logical NOR of Port 2, bits 0-7

P33-P31 cannot wake up from STOP mode if the input lines are configured as analog inputs. Note: These other Stop-Mode Recovery sources have to be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

Stop-Mode Recovery Delay Select (D5). This bit disables the 4 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1.

STOP Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR (Figure 14).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is READ only. It is used to distinguish between a cold or warm start.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and retriggered on subsequent executions of the WDT instruction. The timer circuit is driven by an on-board RC oscillator or external clock source.

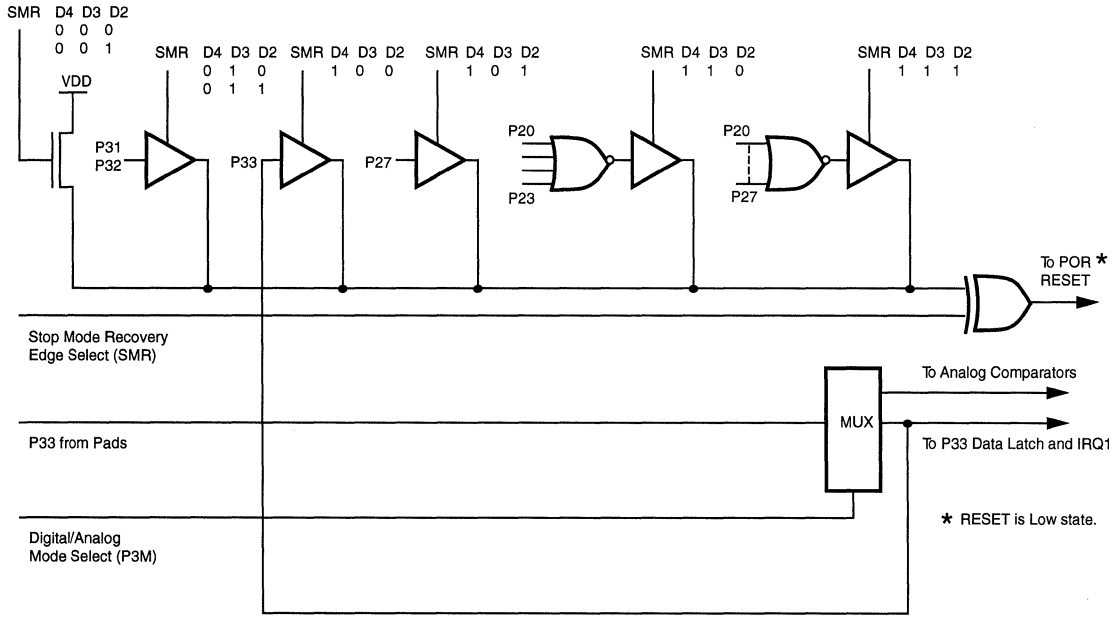


Figure 15. Stop-Mode Recovery Source

The POR clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 16). This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery (Figure 17). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH. It is organized as follows:

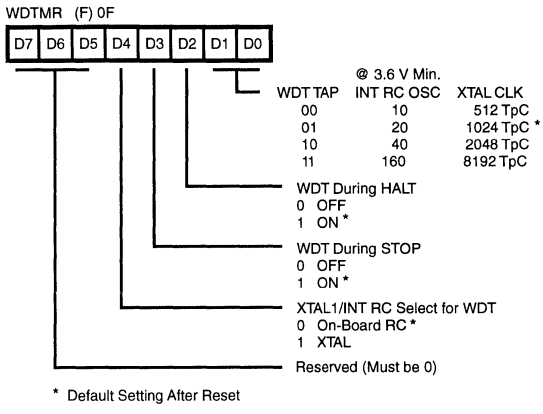


Figure 16. Watch-Dog Timer Mode Register (Write Only)

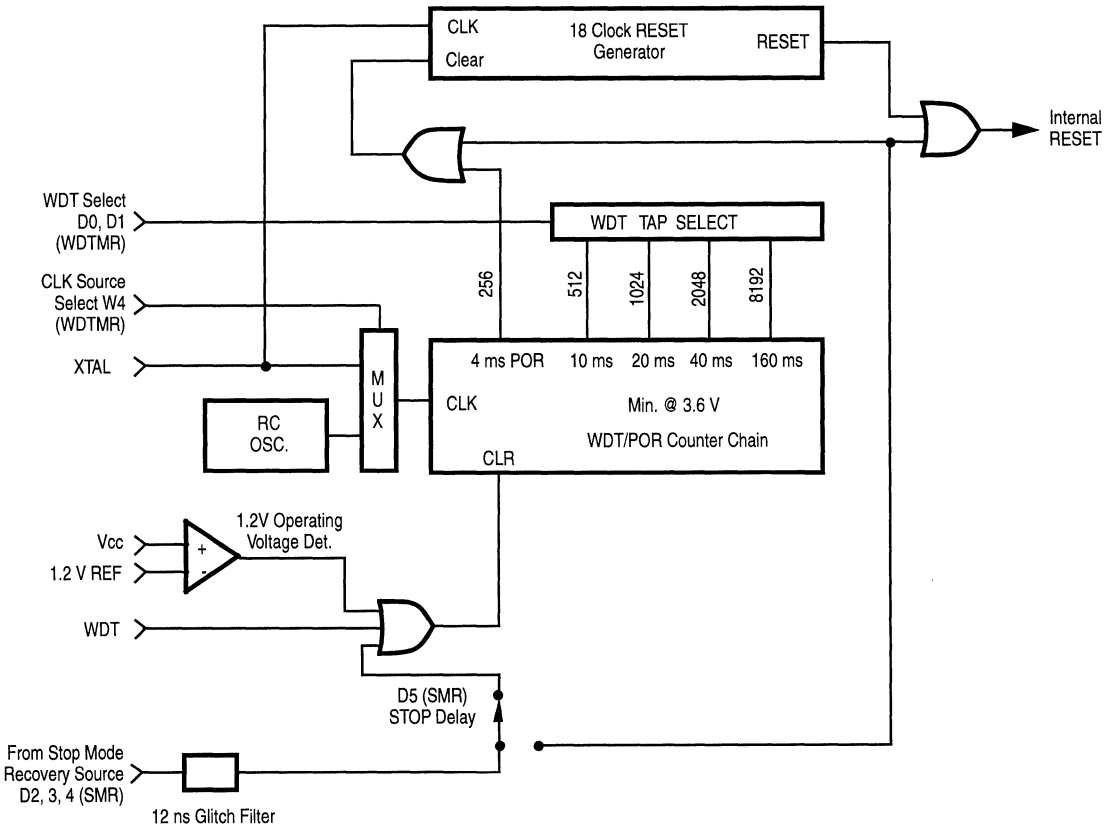


Figure 17. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

WDT Time Select (D1, D0). Selects the WDT time-out period. It is configured as shown in Table 5 (Min. @ 3.6V).

Table 5. WDT Time Select

D1	D0	Time-out of internal RC OSC	Time-out of XTAL clock
0	0	10 ms min	512TpC
0	1	20 ms min	1024TpC
1	0	40 ms min	2048TpC
1	1	160 ms min	8192TpC

Notes:
The default on a WDT initiated RESET is 20 ms.
The minimum time shown is for V_{CC} @ 3.6V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode.

Note: WDT instructions affect the Z (Zero), S (Sign), and V (Overflow) flags.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 1.2V).

ROM Protect. ROM Protect is mask-programmable. It is selected by the customer at the time the ROM code is submitted. **The selection of ROM Protect disables the LDC and LDCI instructions.**

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	°C
T_A	Oper Ambient Temp	†		°C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 18).

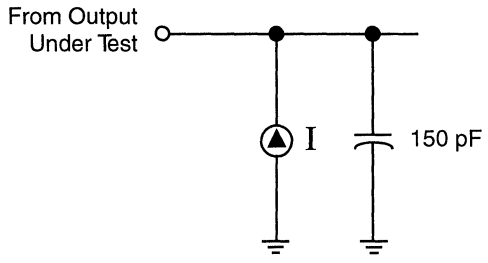


Figure 18. Test Load Configuration

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [2]	T_A = 0°C to +70°C Min	Max	Typical [7] @ +25°C	Units	Conditions	Notes
	Max Input Voltage	2.0V	V_{SS}–0.3	V_{CC}+0.3		V		
		3.6V	V_{SS}–0.3	V_{CC}+0.3		V		
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC}+0.3	0.9	V	Driven by External Clock Generator	
		3.6V	0.9 V_{CC}	V_{CC}+0.3	2.0	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS}–0.3	0.1 V_{CC}	0.9	V	Driven by External Clock Generator	
		3.6V	V_{SS}–0.3	0.1 V_{CC}	1.8	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage Port 2	2.0V	0.9 V_{CC}	V_{CC}+0.3	1.2	V		
		3.6V	0.9 V_{CC}	V_{CC}+0.3	1.9	V		
V_{IH}	Input High Voltage Port 3	2.0V	0.7 V_{CC}	V_{CC}+0.3	0.9	V		
		3.6V	0.7 V_{CC}	V_{CC}+0.3	1.9	V		
V_{IL}	Input Low Voltage Port 2	2.0V	V_{SS}–0.3	0.1 V_{CC}	0.6	V		
		3.6V	V_{SS}–0.3	0.1 V_{CC}	1.2	V		
V_{IL}	Input Low Voltage Port 3	2.0V	V_{SS}–0.3	0.2 V_{CC}	0.9	V		
		3.6V	V_{SS}–0.3	0.2 V_{CC}	1.7	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC}–0.4		1.9	V	I_{OH} = 500 µA	[6]
		3.6V	V_{CC}–0.4		3.5	V	I_{OH} = 500 µA	[6]
V_{OH}	Output High Voltage Low EMI Mode	2.0V	V_{CC}–0.4		1.9	V	I_{OH} = –125 µA	
		3.6V	V_{CC}–0.4		3.5	V	I_{OH} = –125 µA	
V_{OL}	Output Low Voltage Low EM Mode	2.0V		0.4	0.1	V	I_{OL} = 250 µA	
		3.6V		0.4	0.04	V	I_{OL} = 250 µA	
V_{OL1}	Output Low Voltage	2.0V		0.4	0.1	V	I_{OL} = 1.0 mA	[6]
		3.6V		0.4	0.04	V	I_{OL} = 1.0 mA	[6]
V_{OL2}	Output Low Voltage	2.0V		1.0	0.5	V	I_{OL} = 3 mA, 3 Pin Max	[6]
		3.6V		1.0	0.3	V	I_{OL} = 3 mA, 3 Pin Max	[6]
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	6	mV		
		3.6V		25	6	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	2.0V	–1.0	1.0	.001	µA	V_{IN} = 0V, V_{CC}	[8]
		3.6V	–1.0	1.0	.001	µA	V_{IN} = 0V, V_{CC}	[8]
I_{OL}	Output Leakage	2.0V	–1.0	1.0	.001	µA	V_{IN} = 0V, V_{CC}	
		3.6V	–1.0	1.0	.001	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		6	1.2	mA	@ 8 MHz	[3,4] [9] [10]
		3.6V		11.0	6	mA	@ 8 MHz	[3,4] [9] [10]

Sym	Parameter	V_{CC} Note [2]	T_A = 0°C to +70°C Min	Max	Typical @ + 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	2.0V		2.0	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 8 MHz	[3,4] [9] [10]
		3.6V		4	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 8 MHz	[3,4] [9] [10]
		2.0V		1.0	0.4	mA	Clock Divide by 16 @ 8 MHz	[3,4] [9] [10]
		3.6V		3.0	1.0	mA	Clock Divide by 16 @ 8 MHz	[3,4] [9] [10]
I_{CC2}	Standby Current	2.0V		15	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[5]
		3.6V		15	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[5]
		2.0V		115	30	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[5] [9]
		3.6V		350	180	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[5] [9]
V_{ICR}	Comparator Input Common Mode Voltage Range			V_{CC} -1.5V				

Notes:
[1] V_{SS} = 0V = GND
[2] V_{CC} range 3.6V to 2.0V
[3] All outputs unloaded, I/O pins floating, inputs at rail.
[4] $C_{L1} = C_{L2}$ = 47 pF
[5] Same as note [4] except inputs at V_{CC}
[6] STD MODE (not low noise)
[7] Typical are at V_{CC} = 3.6V and 2.0V.
[8] Input bias currents for comparator inputs P31, P32, P33.
[9] Internal on-board RC is driving WDT.
[10] System clock is external XTAL frequency divided by 2.

AC ELECTRICAL CHARACTERISTICS

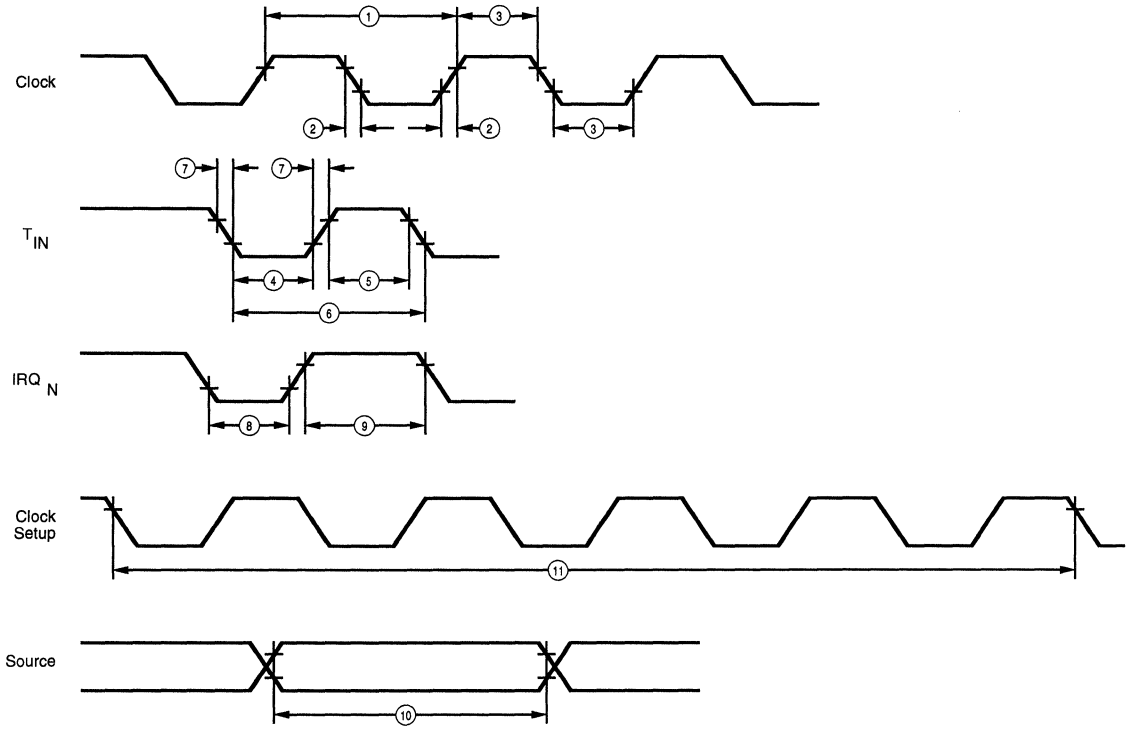


Figure 19. Additional Timing

AC ELECTRICAL CHARACTERISTICS
(Reference Additional Timing)

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	125	DC	ns	[1] [7]
			3.6V	125	DC	ns	[1] [7]
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	[1]
			3.6V		25	ns	[1]
3	TwC	Input Clock Width	2.0V	37		ns	[1] [7]
			3.6V	37		ns	[1] [7]
4	TwTinL	Timer Input Low Width	2.0V	250		ns	[1] [7]
			3.6V	250		ns	[1] [7]
5	TwTinH	Timer Input High Width	2.2V	5TpC			[1] [7]
			3.6V	5TpC			[1] [7]
6	TpTin	Timer Input Period	2.0V	8TpC			[1] [7]
			3.6V	8TpC			[1] [7]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	2.0V		100	ns	[1]
			3.6V		100	ns	[1]
8	TwIL	Int. Request Input Low Time	2.0V	100		ns	[1,2]
			3.6V	70		ns	[1,2]
9	TwIH	Int. Request Input High Time	2.0V	5TpC			[1,2] [7]
			3.6V	5TpC			[1,2] [7]
10	Twsm	Stop-Mode Recovery Width Spec	2.0V	70		ns	
			3.6V	70		ns	
11	Tost	Oscillator Start-up Time	2.0V	5TpC			Reg.
			3.6V	5TpC		ns	[4] [7]
12	Twdt	Watch-Dog Timer Refresh Time	2.0V	30	150		[5]
			3.6V	10	40	ms	D0 = 0 [6] D1 = 0 [6]
			2.0V	60	300	ms	D0 = 1 [6]
			3.6V	20	80	ms	D1 = 0 [6]
			2.0V	120	600	ms	D0 = 0 [6]
			3.6V	40	160	ms	D1 = 1 [6]
			2.0V	480	2400	ms	D0 = 1 [6]
			3.6V	160	610	ms	D1 = 1 [6]
13	T_{POR}	Power On Reset Time	2.0V	15	75	ms	[5]
			3.6V	4	20	ms	D0 = 0 [6]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33)
[3] V_{CC} range 3.6V to 2.0V
[4] SMR-D5 = 0
[5] Reg. WDTMR
[6] Internal RC Oscillator only.
[7] System clock is XTAL frequency divided by 2.

EXPANDED REGISTER FILE CONTROL REGISTERS

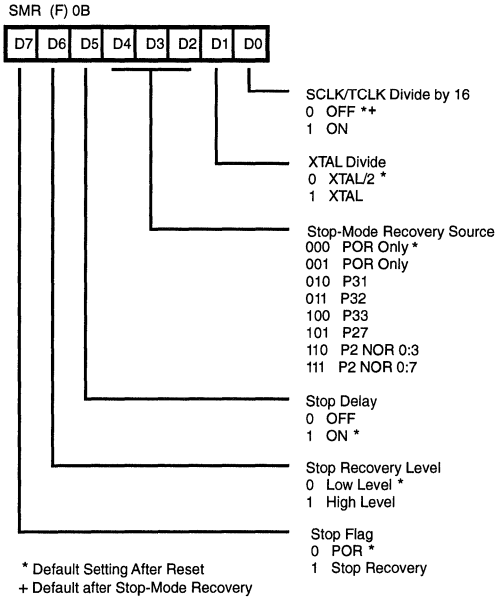


Figure 20. Stop-Mode Recovery Register (Write Only, except bit 7)

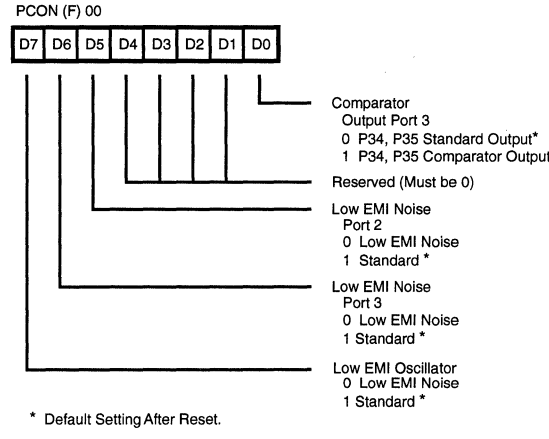


Figure 22. Port Control Register (Write Only)

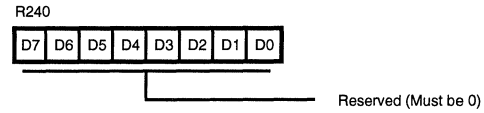


Figure 23. Reserved

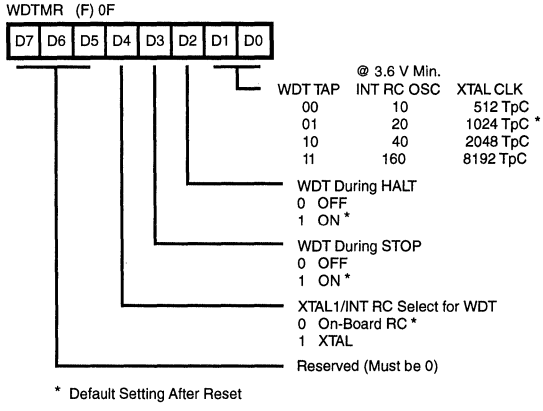


Figure 21. Watch-Dog Timer Mode Register (Write Only)

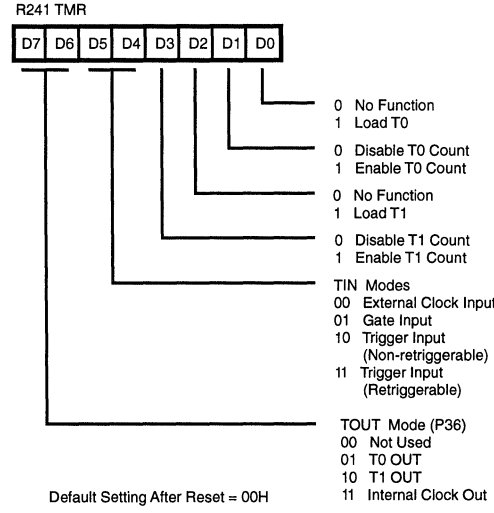


Figure 24. Timer Mode Register (F1H: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS

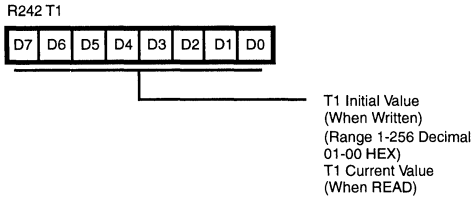


Figure 25. Counter/Timer1 Register (F2H: Read/Write)

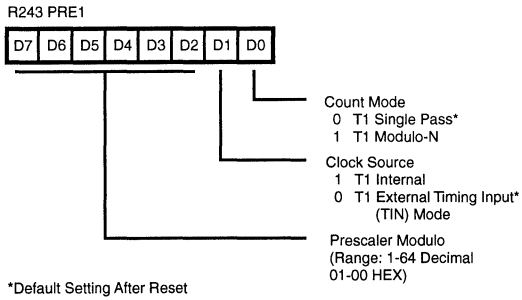


Figure 26. Prescaler 1 Register (F3H: Write Only)

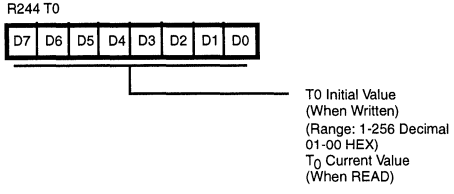


Figure 27. Counter/Timer0 Register (F4H: Read/Write)

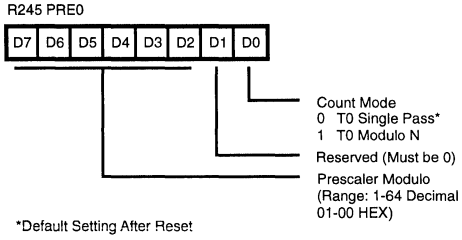


Figure 28. Prescaler 0 Register (F5H: Write Only)

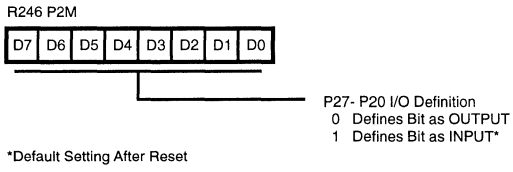


Figure 29. Port 2 Mode Register (F6H: Write Only)

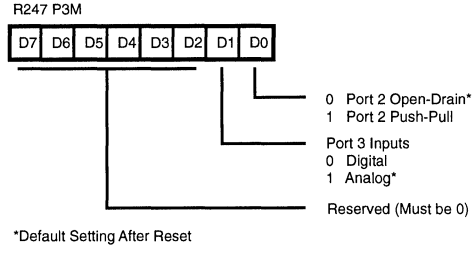


Figure 30. Port 3 Mode Register (F7H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

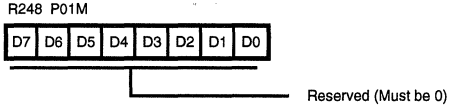


Figure 31. Port 0 and 1 Mode Register

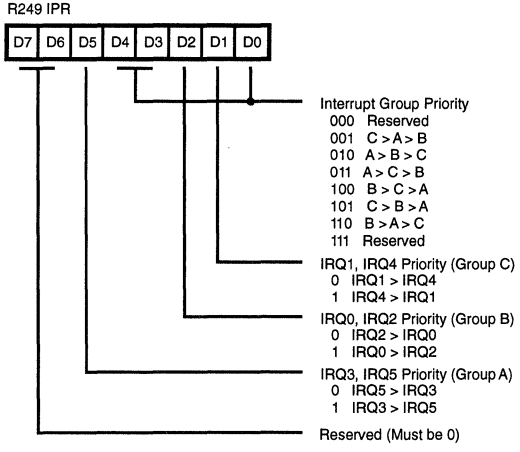


Figure 32. Interrupt Priority Register (F9H: Write Only)

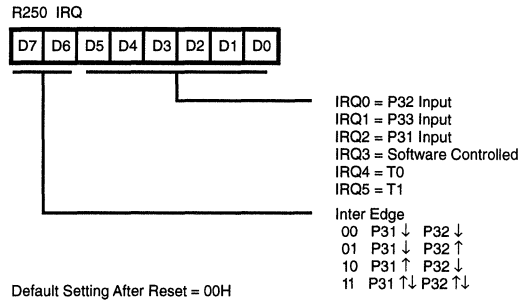


Figure 33. Interrupt Request Register (FAH: Read/Write)

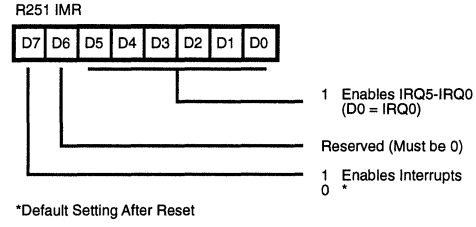


Figure 34. Interrupt Mask Register (FBH: Read/Write)

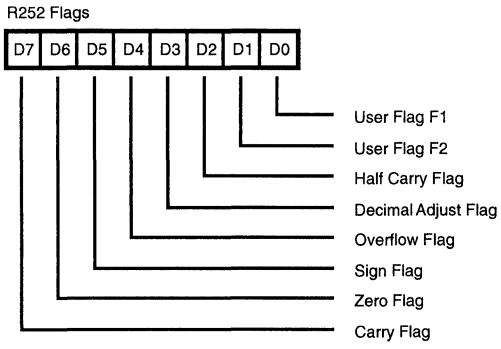


Figure 35. Flag Register (FCH: Read/Write)

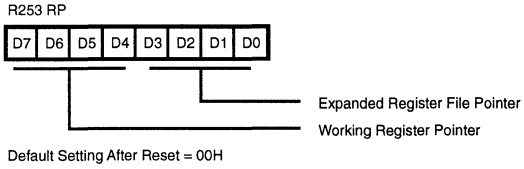


Figure 36. Register Pointer (FDH: Read/Write)

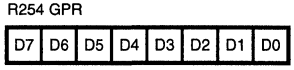


Figure 37. General Purpose Register (FEH: Read/Write)

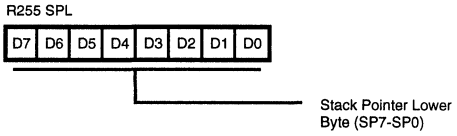


Figure 38. Stack Pointer (FFH: Read/Write)

1

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

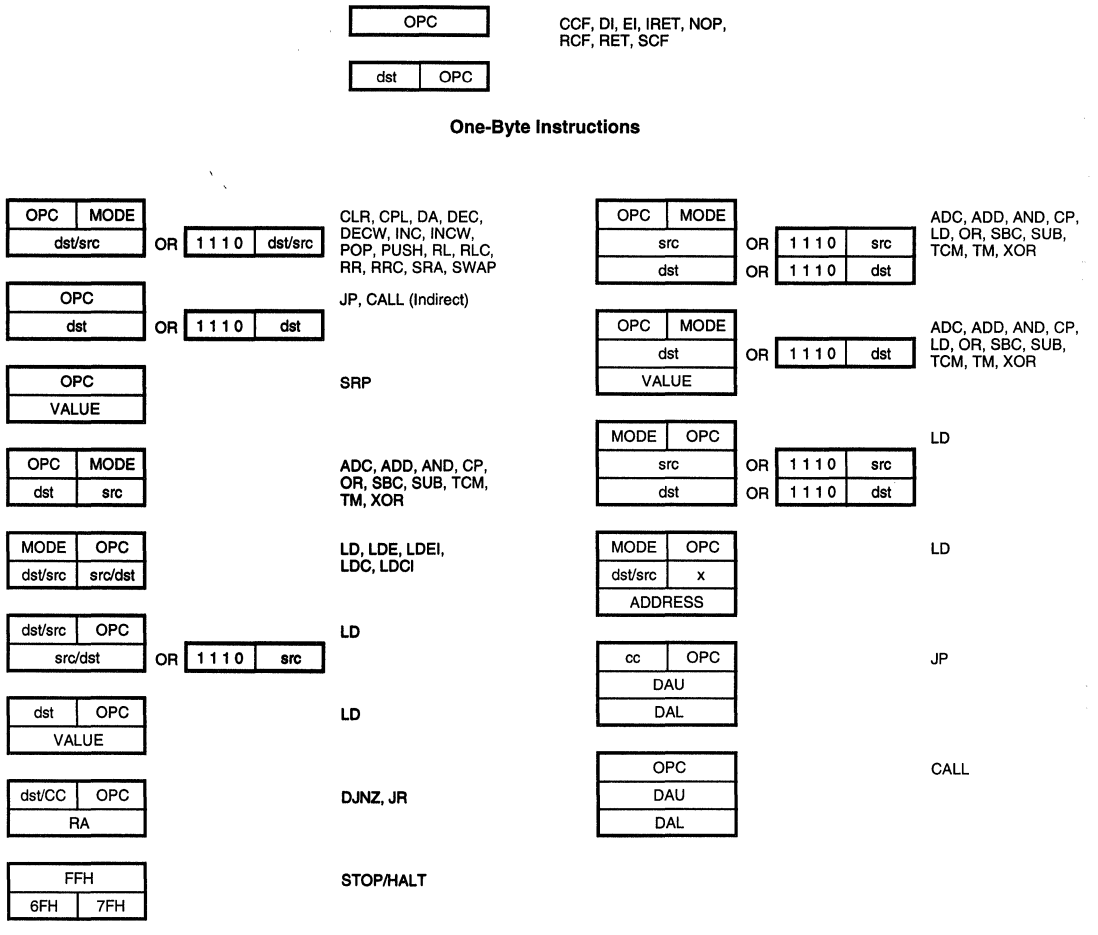
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

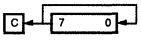
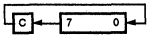
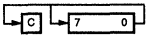
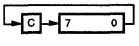
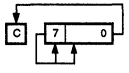
refers to bit 7 of the destination operand.

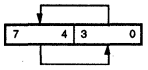
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr ←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

1

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
OR dst, src dst←dst OR src	†		4[ ]	-	[	[	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src	R IR		70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im		31	-	-	-	-	-	-
STOP			6F	1	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

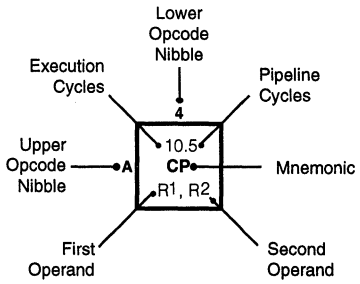
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



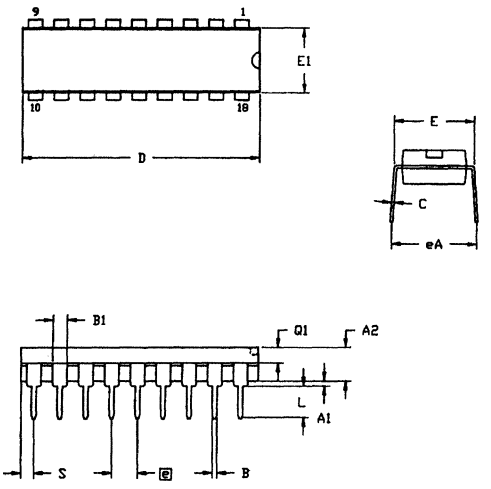
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

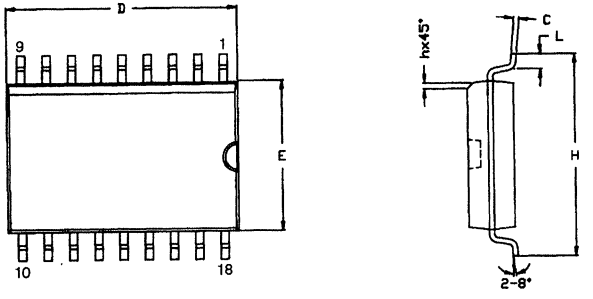
PACKAGE INFORMATION

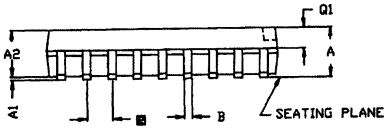


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86L06

	8 MHz
18-Pin DIP	**18-Pin SIOC**
Z86L0608PSC	Z86L0608SSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
S = Plastic SOIC (Small Outline Integrated Circuit)

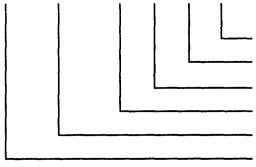
Temperature
S = 0°C to + 70°C

Speed
8 = 8 MHz

Environmental
C = Plastic Standard

Example:

Z 86L06 08 P S C is an 86L06, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Environmental Flow
Temperature
Package
Speed
Product Number
Zilog Prefix

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Z86L29

6K INFRARED (IR) REMOTE CONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- Available in 18-Pin DIP and SOIC Packages
- Low Cost
- 2.0V to 3.6V Operating Range
- Low Power Consumption - 18 mW (Typical)
- Four High-Current Outputs at 2V
  - 7 mA Source (1)
  - 10 mA Sink (3)
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines (Two with Comparator Inputs)
- All Digital Inputs are CMOS Level
- 6 Kbytes of ROM
- 125 Bytes of RAM
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers
- 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Five Different Sources
- Clock Speed 8 MHz
- Brown-Out Protection
- Watch-Dog/Power-On Reset Timer
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86L29 IR Controller is a low voltage Consumer Controller Processor (CCP™) ideal for IR remote applications which introduces a new level of sophistication to single-chip architecture. The Z86L29 is a member of the Z8® single-chip microcontroller family with 6 Kbytes of ROM, and 125 bytes of RAM. The device is available in an 18-pin DIP and 18-pin SOIC package, and is CMOS compatible. Zilog's Z86L29 CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86L29 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many industrial, automotive, hand held, battery operated, and advanced scientific applications.

For device applications that demand powerful I/O capabilities, the CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 125 bytes of general-purpose registers, two I/O Port registers, and 14 Control and Status registers. The Expanded Register File consists of three control registers.

To unburden the program from coping with real-time problems such as counting/timing and input/output data communication, the Z86L29 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators that can process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

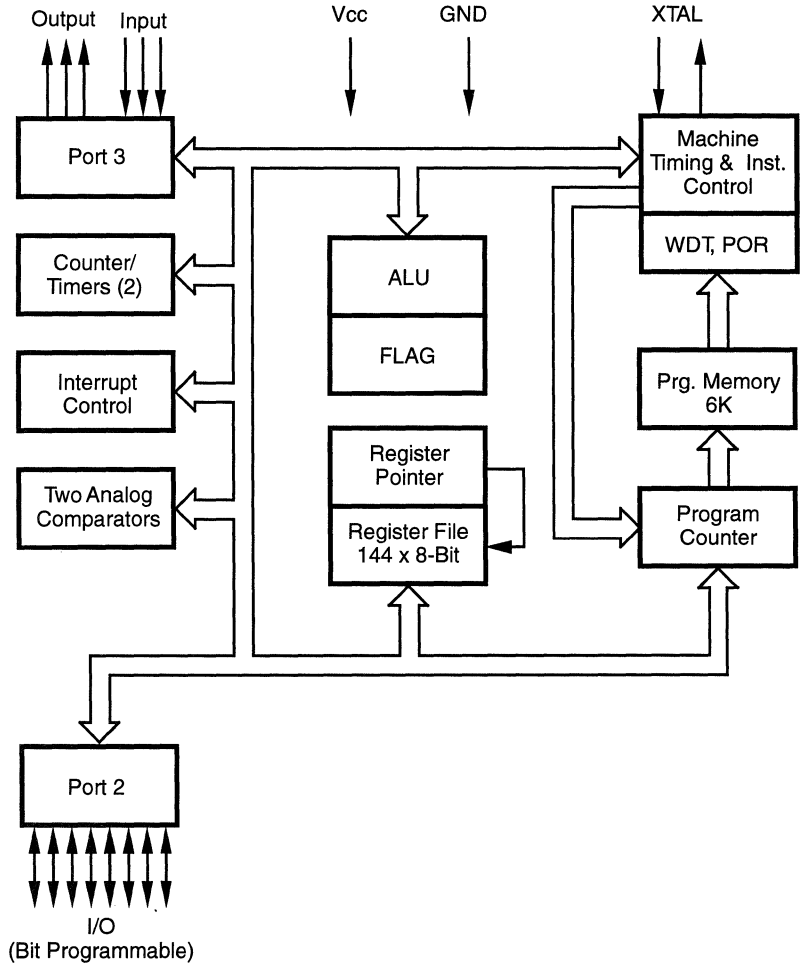

Figure 1. Functional Block Diagram

PIN DESCRIPTION

Table 1. DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-P27	Port 2, pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-P33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-P36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-P23	Port 2, pins 0, 1, 2, 3	In/Output

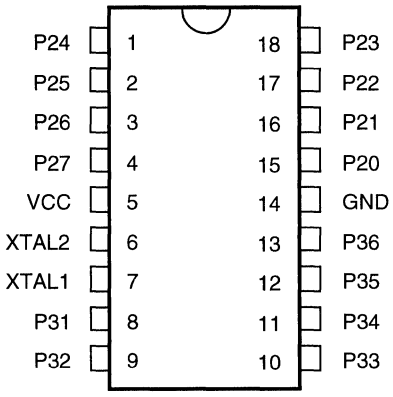

Figure 2. 18-Pin DIP and SOIC Configuration

PIN FUNCTIONS

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 3).

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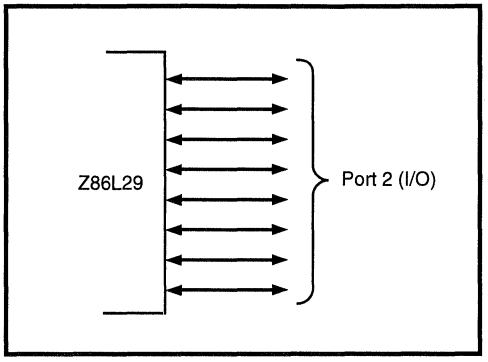
PIN FUNCTIONS (Continued)



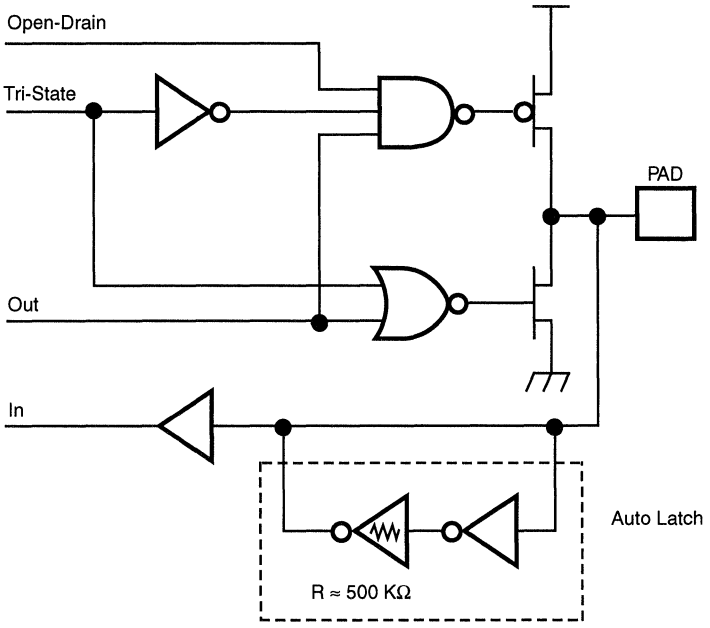
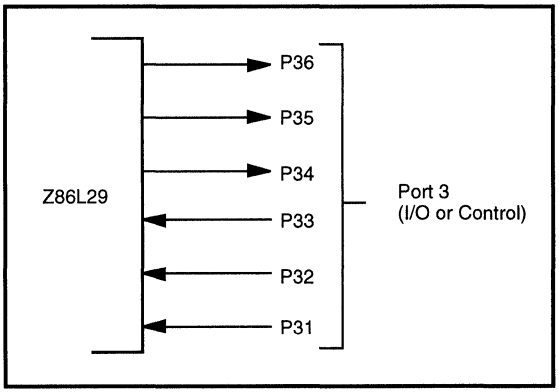


Figure 3. Port 2 Configuration

Port 3 (P36-P31). Port 3 is a 6-bit, CMOS-compatible port with three fixed input and three fixed output lines. These six lines consist of three fixed input (P33-P31) and three fixed output port (P36-P34) lines. P31, P32 and P33 are standard CMOS inputs, and P34, P35 may be programmed as either push-pull or open-drain (Figure 5). P36 is a push-pull output. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (bit 1). P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer1 is made through P31 (T_{IN}) and P36 (T_{OUT}), (Figure 4).



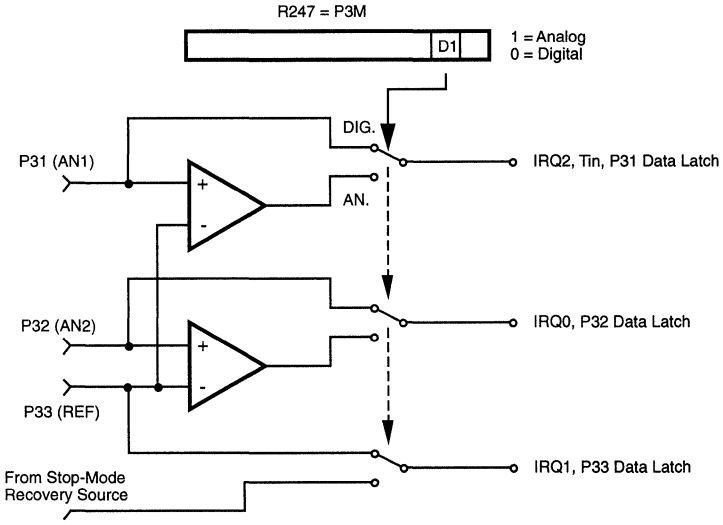


Figure 4. Port 3 Comparator Configuration

PIN FUNCTIONS (Continued)

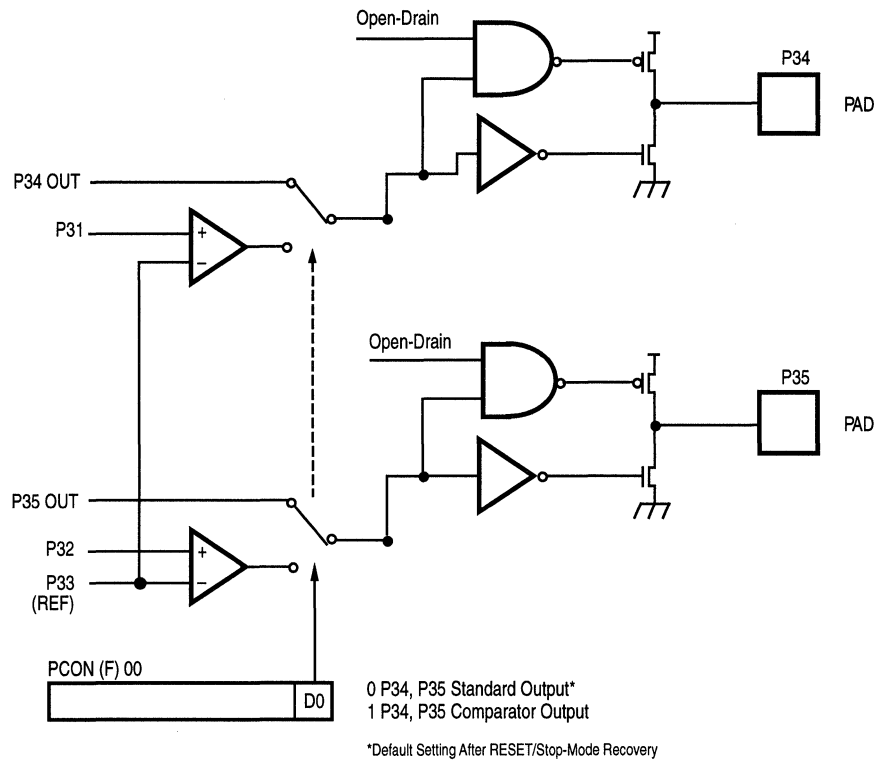


Figure 5. Port 3 I/O Configuration

Comparator Inputs. Port 3, P31 and P32 each have a comparator front end. The comparator reference voltage, P33 , is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. The internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources can be used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 source (Figure 14). Comparator outputs may be programmed to be outputted on P34 and P35 through the PCON register (Figures 5 and 16).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

FUNCTIONAL DESCRIPTION

The Z86L29 CCP is based upon Zilog's core which incorporates special functions to enhance the Z8 MCU's application in industrial, scientific research, and advanced technologies applications.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection (Brown-Out Protection)

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. The Z86L29 can address up to 6 Kbytes of internal program memory, respectively (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 6144 consists of on-chip mask-programmed ROM.

The 6 Kbytes of program memory is mask programmable. A ROM Protect feature will prevent "dumping" of the ROM contents from Program Memory by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space, R0 through R15, is implemented as 16 groups of 16 registers per group (Figure 7). These register groups are known as the ERF (Expanded Register File). Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 8). Three system configuration registers reside in the Expanded Register File address space at Bank F. The rest of the Expanded Register addressing space is not physically implemented and is open for future expansion.

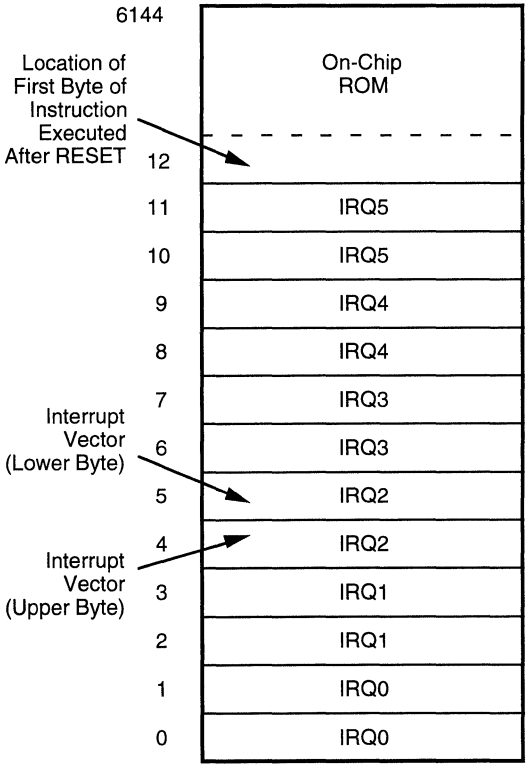


Figure 6. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

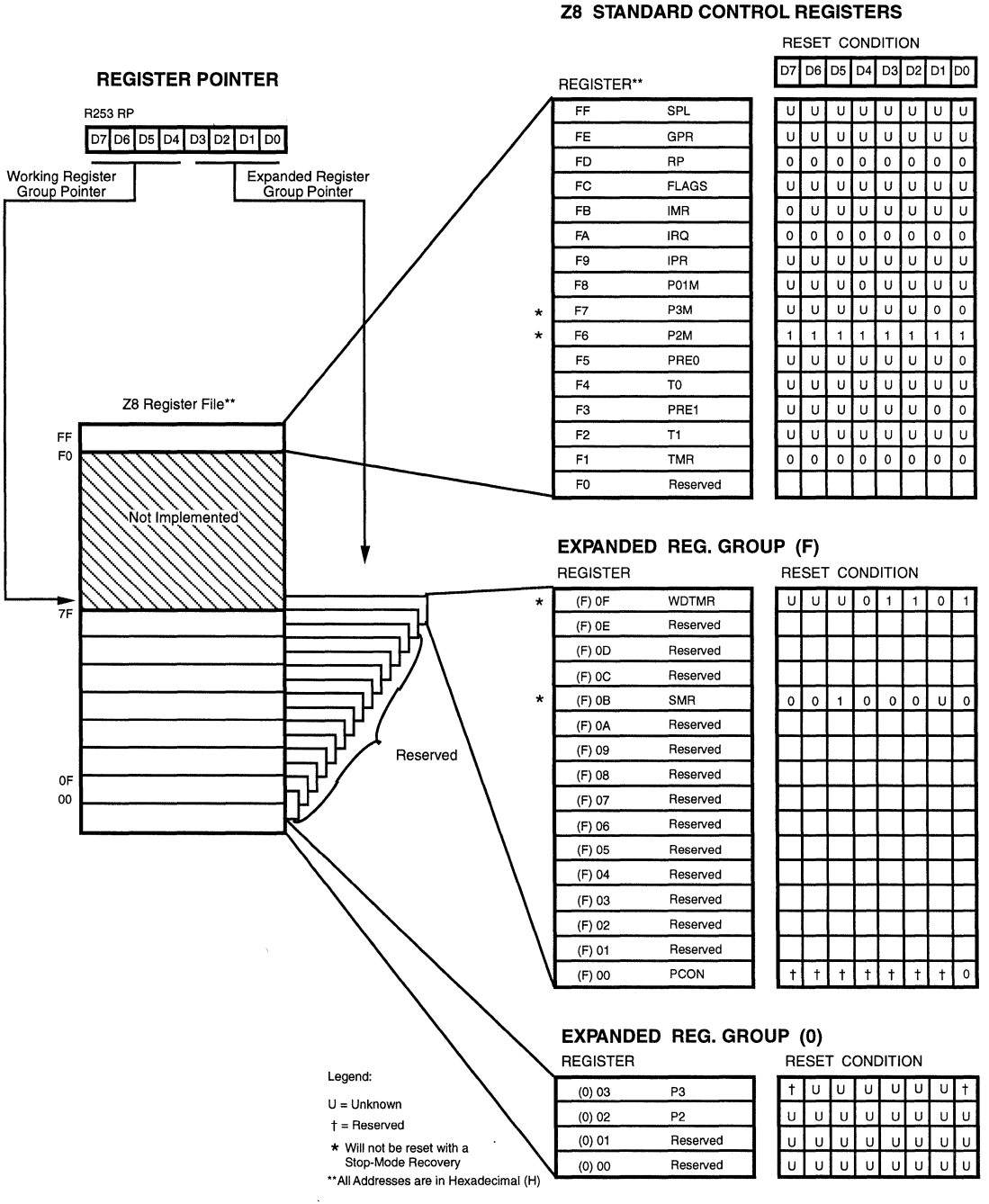


Figure 7. Expanded Register File Architecture

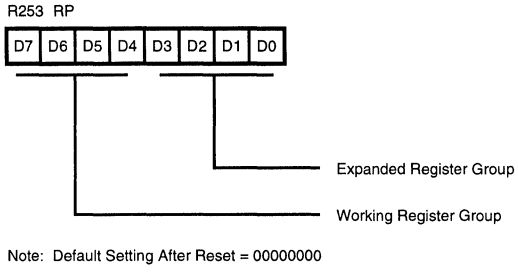


Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 125 general-purpose registers, and 14 control and status registers, and two system configuration registers in the Expanded Register Group (Figure 7). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Caution: D4 of Control Register P01M (R251) must be 0. If the Z86L29 is emulated by Z86C90, D4 of P01M has to change to 0 before submission to ROM code.

Note: The Z86L29 has one extra general-purpose register located at FEH (R254).

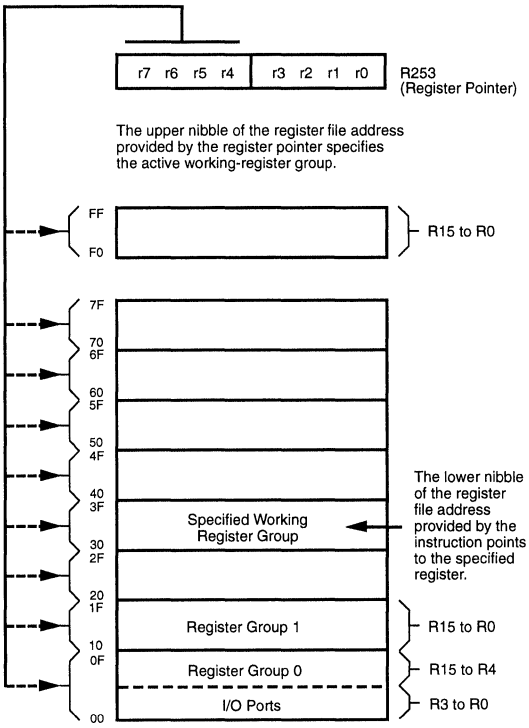


Figure 9. Register Pointer

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FUNCTIONAL DESCRIPTION (Continued)

Stack. The Z86L29 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 125 general-purpose registers.

Counter/Timers. There are two 8-bit programmable Counter/Timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 10).

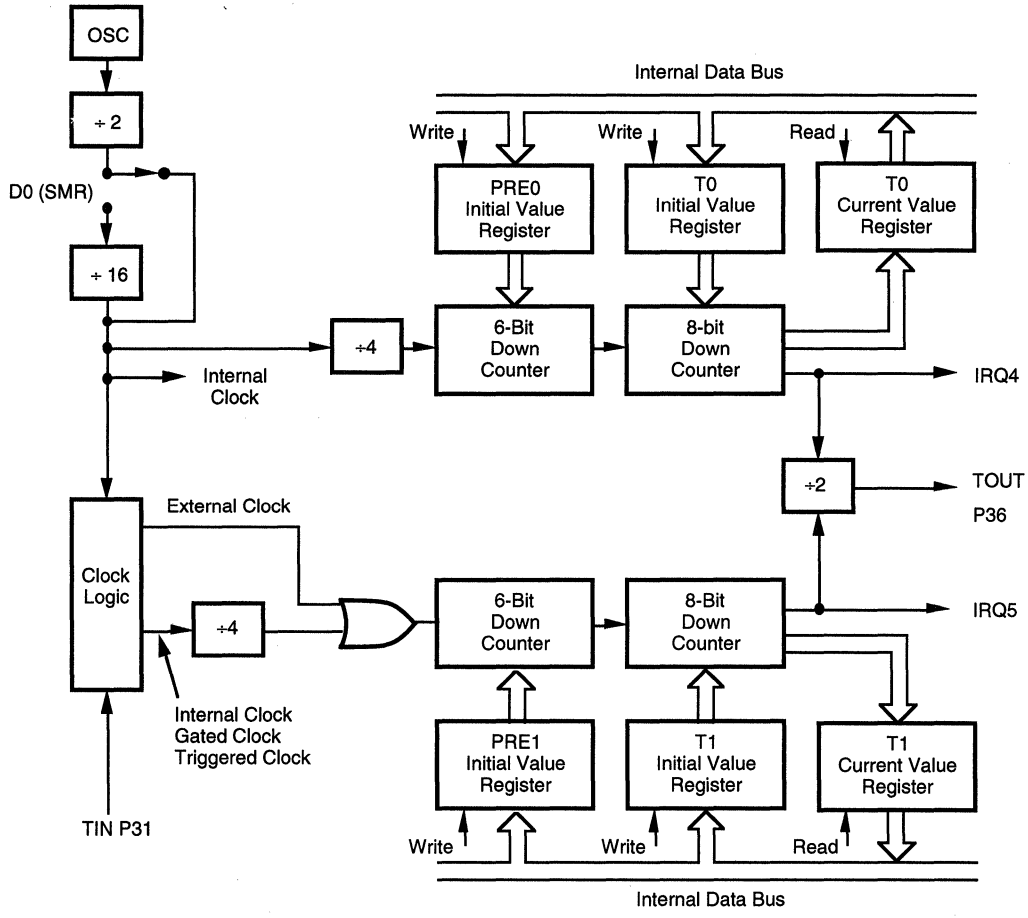


Figure 10. Counter/Timer Block Diagram

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock, divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or not-retriggerable, or as a gate input for the internal clock. Port 3, line P36, serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The Counter/Timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z86L29 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; three sources are claimed by Port 3, lines P31-P33, two sources in Counter/Timers, and one source from software. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 2).

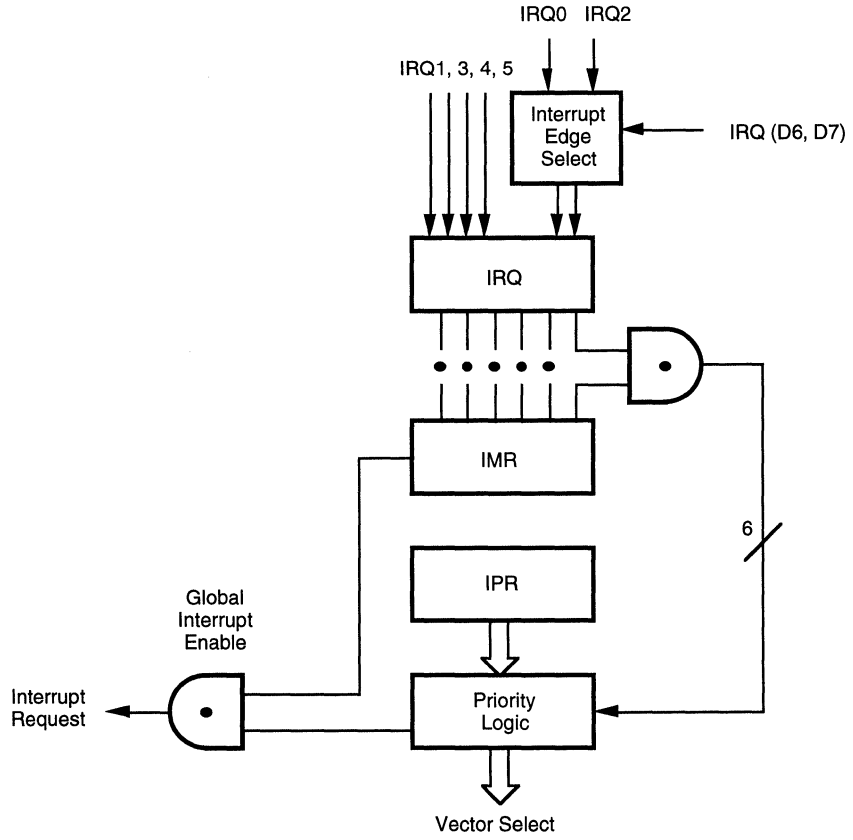


Figure 11. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	IRQ0	0, 1	External (P32), ↑ ↓ Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), ↓ Edge Triggered
IRQ2	IRQ2, T_{IN}	4, 5	External (P31), ↑ ↓ Edge Triggered
IRQ3		6, 7	Software Generated Only
IRQ4	T0	8, 9	Internal (T0)
IRQ5	T1	10, 11	Internal (T1)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L29 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs services. IRQ3 has no hardware source, but can be invoked by software (write to IRQ3 Register).

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

The programming bits for the Interrupt Edge Select are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

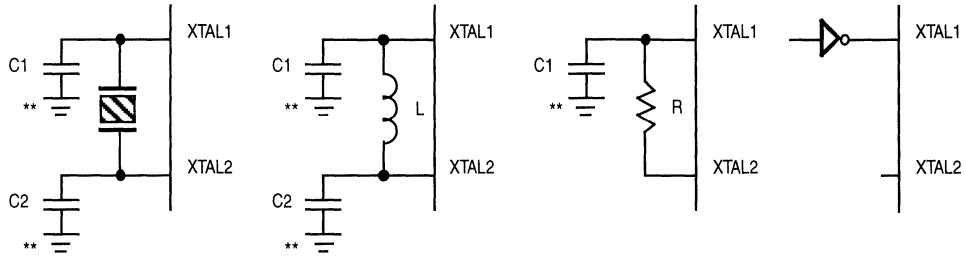
Clock. The Z86L29 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz max, with a series resistance (RS) less than, or equal, to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the supplier's recommended capacitor values from each pin to pin 14 (GND). The RC oscillator option is mask-programmable, to be selected by the customer at the time the ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12).

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator, or by the XTAL oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK Status
2. Stop-Mode Recovery (If D5 of SMR = 1)
3. WDT Time-Out
4. Low Voltage Detection (Brown-Out Protection)

The POR time is a minimum of 5 ms at V_{CC} of 3.6V. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).



* Preliminary Value Including Pin Parasitics
** Pin 14 GND

Figure 12. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The Counter/Timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 13). All bits are write only except bit 7 which is Read only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the Stop-Mode Recovery signal. If the XTAL1 is used as a source to drive the POR counter, then the Stop-Mode Recovery time is XTAL/256. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP mode is terminated by a Reset (V_{BO}, WDT timeout, POR,) or SMR recovery. This causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode

             or

FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
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FUNCTIONAL DESCRIPTION (Continued)

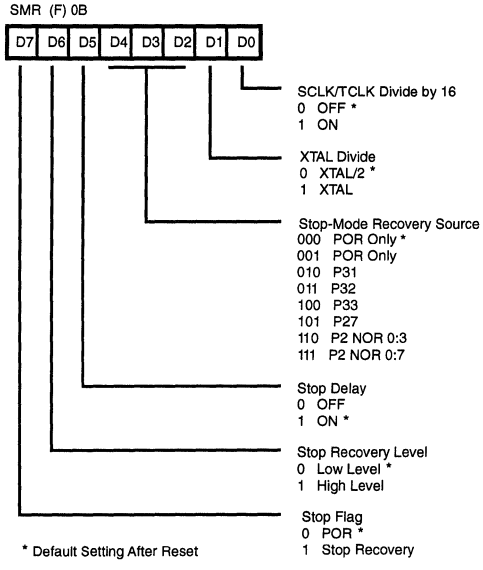


Figure 13. Stop-Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the Counter/Timers and interrupt logic).

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 14 and Table 4).

Table 4. Stop Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2, bits 0-3
1	1	1	Logical NOR of Port 2, bits 0-7

P33-P31 cannot wake up from STOP mode if the input lines are configured as analog input.

Stop-Mode Recovery Delay Select (D5). This bit disables the minimum 5 ms (V_{CC} at 3.6V) RESET delay after Stop-Mode Recovery. The default condition of this bit is 1.

Stop-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP mode. A zero indicates low level recovery. The default is 0 on POR (Figure 14).

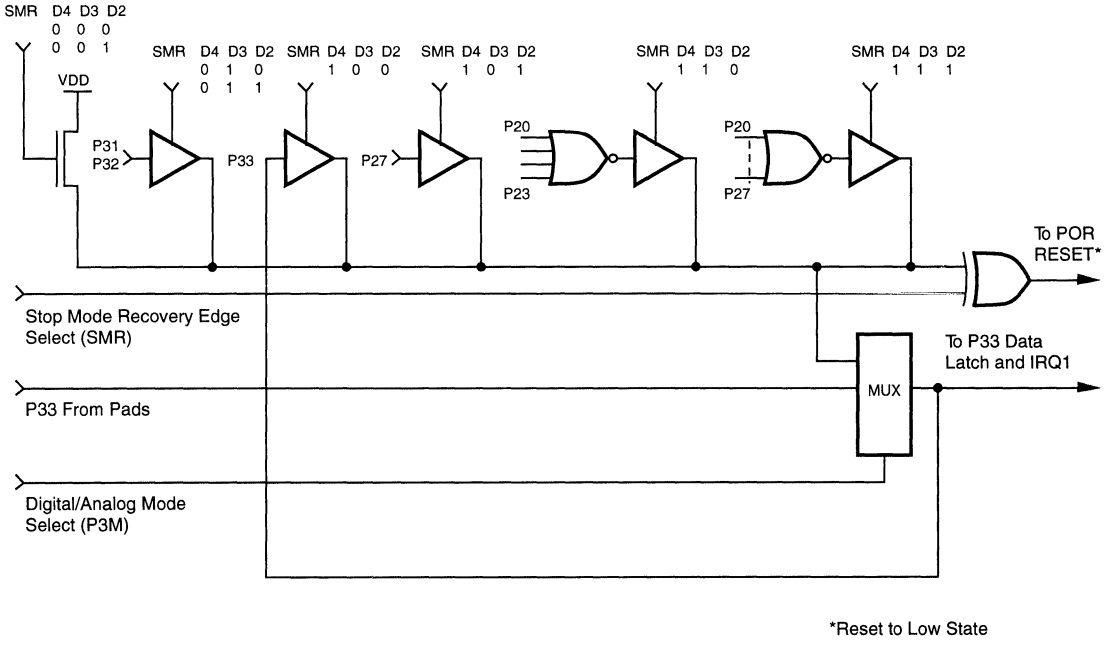


Figure 14. STOP Mode Recovery Source

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is active High, and is zero (cold) on POR/WDT RESET. This bit is a READ only. It is used to distinguish between a cold or warm start.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that will reset the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and retriggered on subsequent executions of the WDT instruction. The timer circuit is driven by an on-board RC oscillator or external XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 15). This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a Stop-Mode Recovery (Figure 17). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:

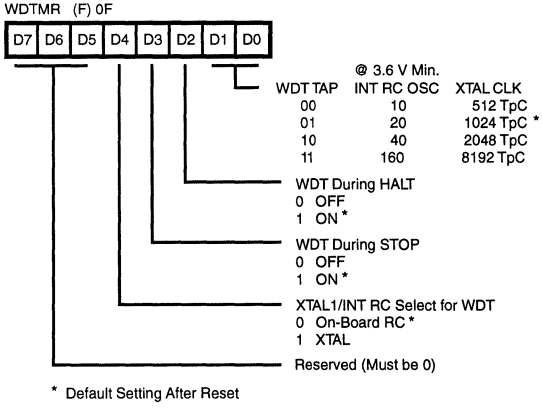
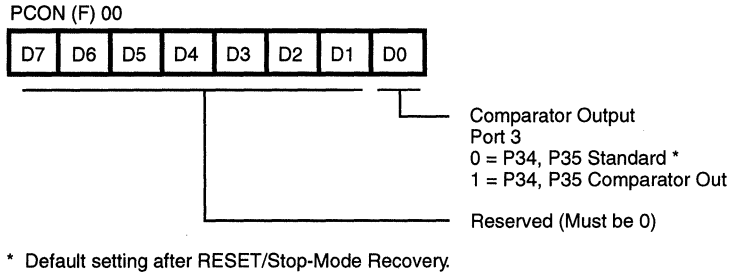


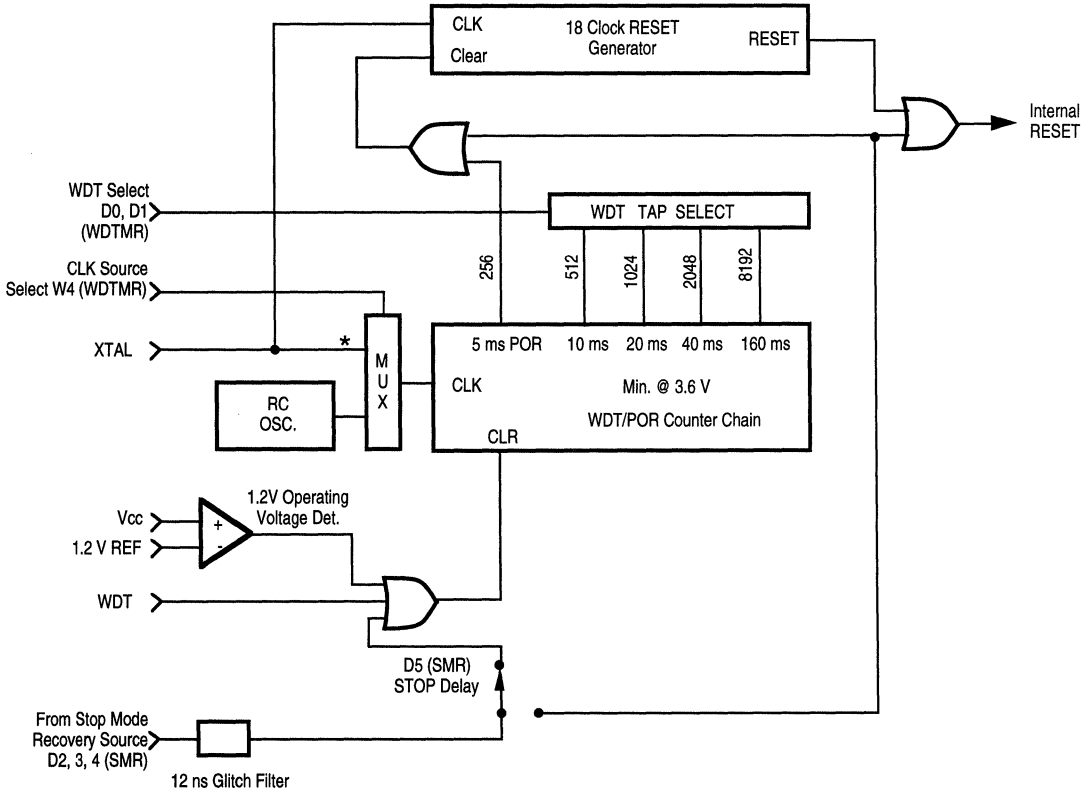
Figure 15. Watch-Dog Timer Mode Register

FUNCTIONAL DESCRIPTION (Continued)



* Default setting after RESET/Stop-Mode Recovery.

Figure 16. Port Control Register



*Run mode and stop mode only.

Figure 17. Resets and WDT

WDT Time Select (D1, D0). Selects the WDT time period. It is configured as shown in Table 5.

Table 5. WDT Time Select

D1	D0	Timeout Period (On-Board RC) Clock Source	XTAL1 Clock Source
0	0	10 ms min	512TpC
0	1	20 ms min	1024TpC
1	0	40 ms min	2048TpC
1	1	160 ms min	8192TpC

Notes:
TcP = XTAL clock cycle. The default on a WDT initiated RESET is 20 ms. The minimum time shown is for V_{CC} at 3.6V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

On-Board Power-On Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal on-board RC oscillator.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 2.0V at 25°C).

Brown-Out Protection (V_{BO}). The device will function normally at or above 2.0V under all conditions. For V_{CC} below 2.0V, the device will either function normally or the device RESET will be globally activated by the brown-out circuit. The actual brown-out trip point is a function of temperature and process parameters (Figure 18).

ROM Protect. ROM Protect is mask-programmable. It is selected by the customer at the time the ROM code is submitted. **The selection of ROM Protect will disable the LDC and LDCI instructions.**

2

FUNCTIONAL DESCRIPTION (Continued)

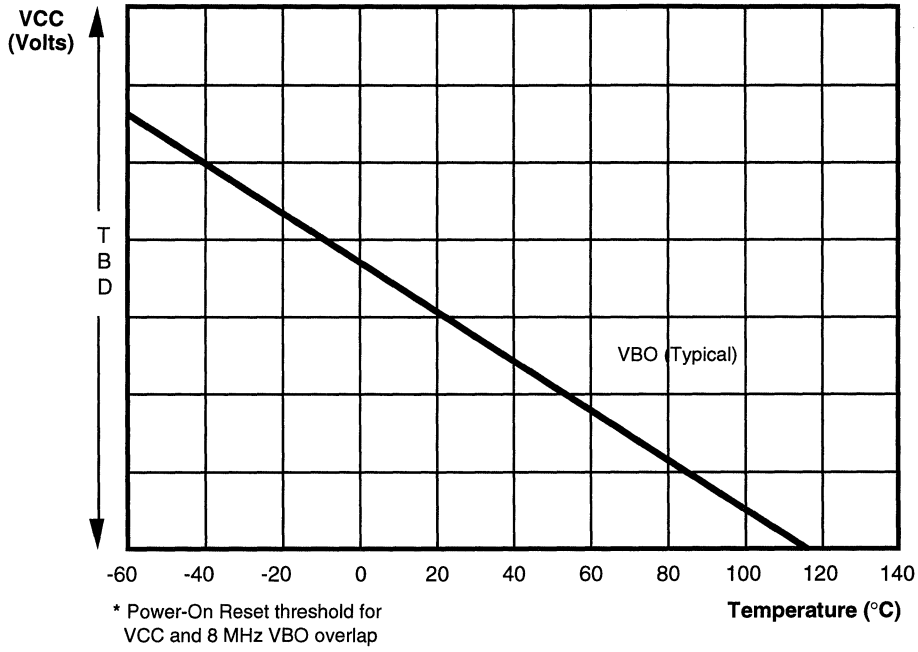


Figure 18. Typical Z86L29 V_{BO} Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage *	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†		C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 19).

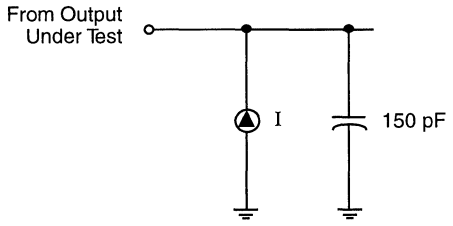


Figure 19. Test Load Configuration

2

DC ELECTRICAL CHARACTERISTICS
Z86L29

Sym	Parameter	V_{CC} Note [2]	T_A = 0°C to +55°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	2.0V	V_{CC} 0.9	V_{CC}+0.3		V	Driven by External Clock Generator	
		3.6V	V_{CC} 0.9	V_{CC}+0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS}–0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.6V	V_{SS}–0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	V_{CC} 0.9	V_{CC}+0.3	—	V		
		3.6V	V_{CC} 0.9	V_{CC}+0.3	1.3	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS}–0.3	0.2 V_{CC}	—	V		
		3.6V	V_{SS}–0.3	0.2 V_{CC}	1.3	V		
V_{OH}	Output High Voltage	2.0V	V_{CC}–0.4		1.8	V	I_{OH} = –0.5 mA	
		3.6V	V_{CC}–0.4		3.5	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage Port 3 (P36)	2.0V	1.5			V	I_{OH} = –7 mA @ 25°C	
		3.6V	1.5			V	I_{OH} = –7 mA @ 25°C	
V_{OL1}	Output Low Voltage	2.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		3.6V		0.4	0.1	V	I_{OL} = 4.0 mA	
V_{OL1a}	Output Low Voltage Port 2 (P20,21,22)	2.0V		0.4	0.2	V	I_{OL} = 10 mA @ 25°C	[6]
		3.6V		0.4	0.1	V	I_{OL} = 10 mA @ 25°C	[6]
V_{OL2}	Output Low Voltage	2.0V		0.8	0.3	V	I_{OL} = 2.0 mA 3 Pin Maximum	[7]
		3.6V		0.8	0.5	V	I_{OL} = 8.0mA 3 Pin Maximum	[7]
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.6V		25	10	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.6V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.6V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		6	2	mA	@ 8 MHz	[3,4]
		3.6V		11	5	mA	@ 8 MHz	[3,4]
V_{ICR}	Comparator Input Common Mode Voltage Range	2.0V	0	V_{CC}–1.5		V		
		3.6V	0	V_{CC}–1.5		V		

Sym	Parameter	V_{CC} Note [2]	T_A = 0°C to +55°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	2.0V		3.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[3, 4]
		3.6V		4	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[3, 4]
		2.0V		1.4	0.6	mA	Clock Divide-by-16 @ 8 MHz	[3, 4]
		3.6V		3.0	2.0	mA	Clock Divide-by-16 @ 8 MHz	[3, 4]
I_{CC2}	Standby Current	2.0V		15	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[5]
		3.6V		15	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[5]
		2.0V		TBD	TBD	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[5]
		3.6V		TBD	TBD	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[5]
I_{ALL}	Auto Latch Low Current	2.0V		6.0	3.0	µA	$0V < V_{IN} < V_{CC}$	
		3.6V		8.0	4.0	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	2.0V		–4.0	–2.0	µA	$0V < V_{IN} < V_{CC}$	
		3.6V		–6.0	–3.0	µA	$0V < V_{IN} < V_{CC}$	
T_{POR}	Power-On Reset	2.0V	15	75	—	ms		
		3.6V	5	20	—	ms		
V_{BO}	V_{CC} Brown-Out Voltage			2.1		V		

Notes:
[1] V_{SS} = 0V = GND
[2] V_{CC} is 2.0V to 3.6V.
[3] All outputs unloaded, I/O pins floating, inputs at rail.
[4] $C_{L1} = C_{L2}$ = 100 pF
[5] Same as Note [3] except inputs at V_{CC}.
[6] One output at a time.
[7] For Port 2, pins 3, 4, 5,6, 7, Port 3

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AC ELECTRICAL CHARACTERISTICS

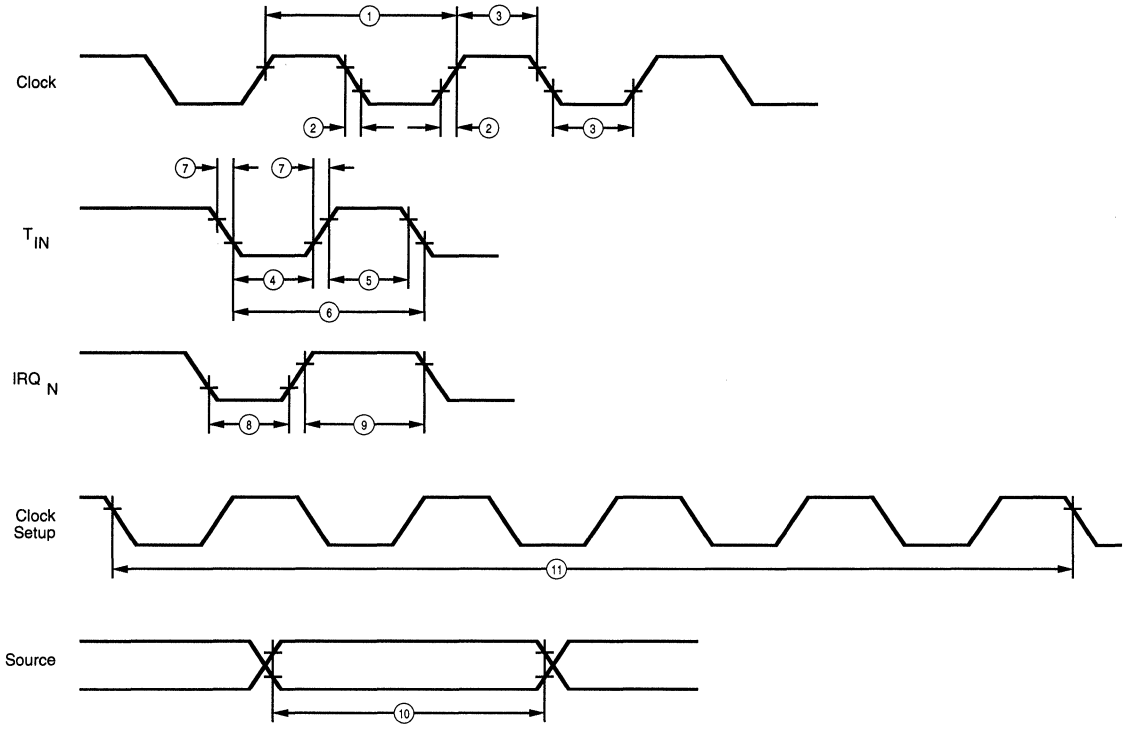

Figure 20. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Z86L29

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +55°C 8 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	125	100,000	ns	[1]
			3.6V	125	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	[1]
			3.6V		25	ns	[1]
3	TwC	Input Clock Width	2.0V	37		ns	[1]
			3.6V	37		ns	[1]
4	TwTinL	Timer Input Low Width	2.0V	250		ns	[1]
			3.6V	250		ns	[1]
5	TwTinH	Timer Input High Width	2.0V	5TpC			[1]
			3.6V	5TpC			[1]

AC ELECTRICAL CHARACTERISTICS (Continued)
Z86L29

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +55°C 8 MHz Min	Max	Units Units	Notes Notes
6	TpTin	Timer Input Period	2.0V	8TpC			[1]
			3.6V	8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	2.0V		100	ns	[1]
			3.6V		100	ns	[1]
8	TwIL	Interrupt Request Input Low Time	2.0V	100		ns	[1, 2]
			3.6V	100		ns	[1, 2]
9	TwIH	Interrupt Request Input High Time	2.0V	5TpC			[1, 2]
			3.6V	5TpC			[1, 2]
10	Twsm	Stop-Mode Recovery Width Spec	2.0V	70		ns	
			3.6V	70		ns	
11	Tost	Oscillator Startup Time	2.0V		5TpC		Reg. [4]
			3.6V		5TpC		
12	Twdt	Watch-Dog Timer Refresh Time	2.0V	30	150		[5]
			3.6V	10	40	ms	D0 = 0 [6] D1 = 0 [6]
			2.0V	60	300	ms	D0 = 0 [6]
			3.6V	20	80	ms	D1 = 1 [6]
			2.0V	120	600	ms	D0 = 0 [6]
			3.6V	40	160	ms	D1 = 1 [6]
			2.0V	480	2400	ms	D0 = 1 [6]
			3.6V	160	610	ms	D1 = 1 [6]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)
[3] V_{CC} is 2.0V to 3.6V
[4] SMR – D5 = 0
[5] Register WDTMR
[6] Internal RC Oscillator only

EXPANDED REGISTER FILE CONTROL REGISTERS

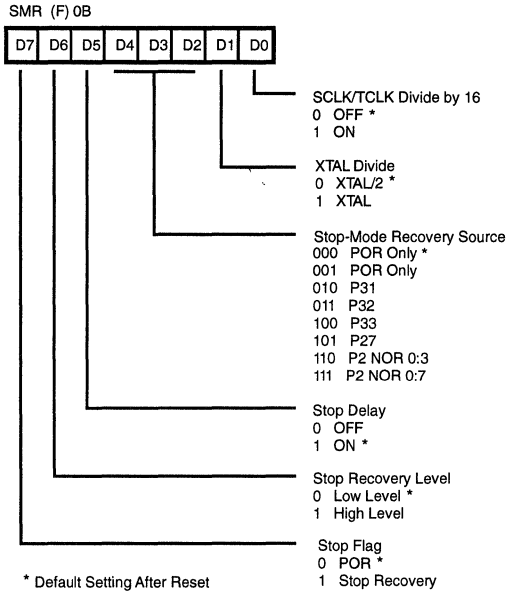

Figure 21. Stop-Mode Recovery Register ((F) 0BH: Read Only)

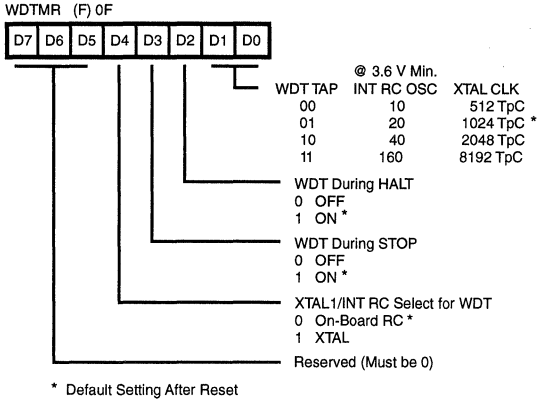

Figure 22. Watch-Dog Timer Mode Register ((F) 0FH: Write Only)

Z8 CONTROL REGISTER DIAGRAMS

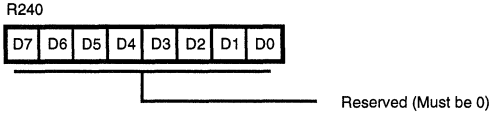

Figure 23. Reserved (F0H)

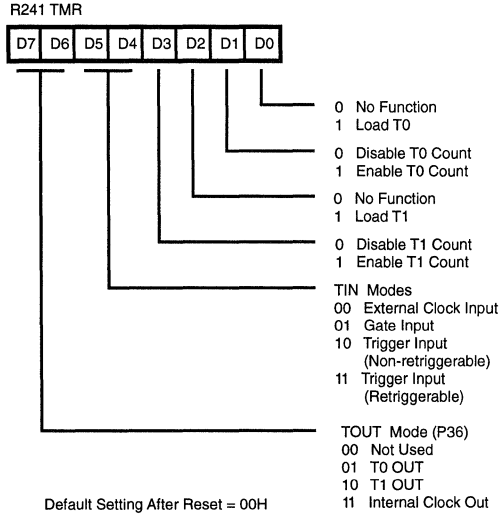

Figure 24. Timer Mode Register (F1H: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

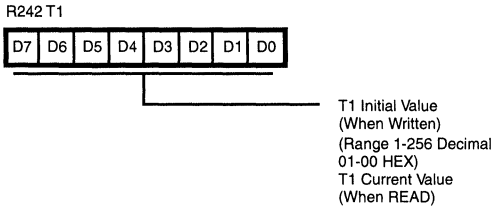

Figure 25. Counter/Timer1 Register (F2H: Read/Write)

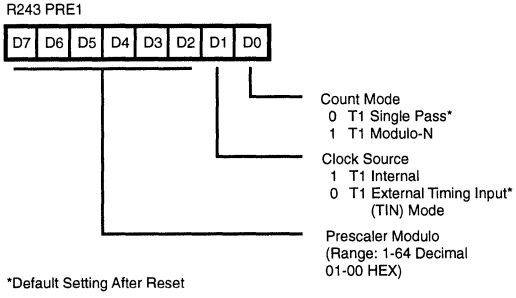

Figure 26. Prescaler 1 Register (F3H: Write Only)

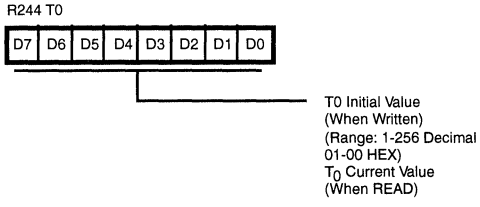

Figure 27. Counter/Timer0 Register (F4H: Read/Write)

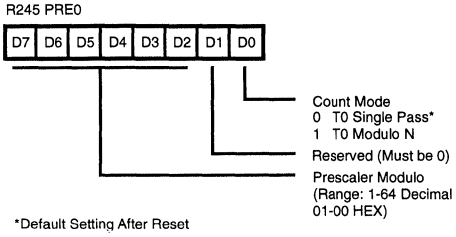

Figure 28. Prescaler 0 Register (F5H: Write Only)

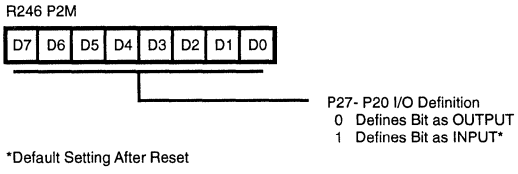

Figure 29. Port 2 Mode Register (F6H: Write Only)

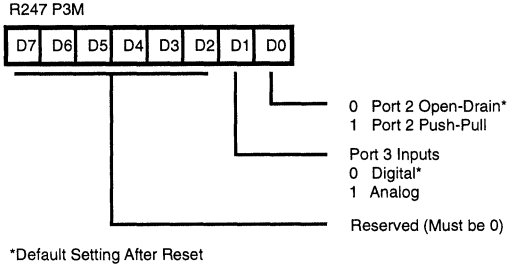

Figure 30. Port 3 Mode Register (F7H: Write Only)

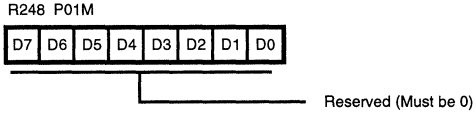

Figure 31. Port 0 and 1 Mode Register

Z8 CONTROL REGISTER DIAGRAMS (Continued)

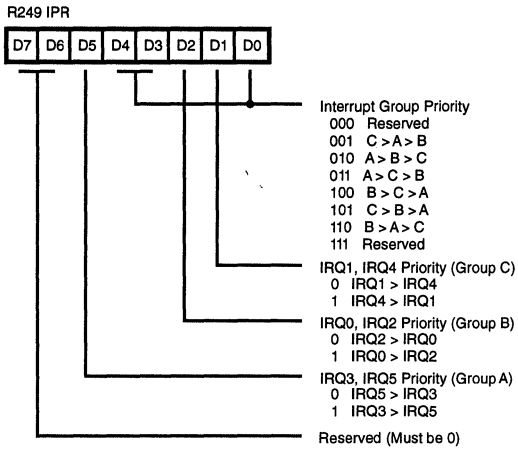

Figure 32. Interrupt Priority Register (F9H: Write Only)

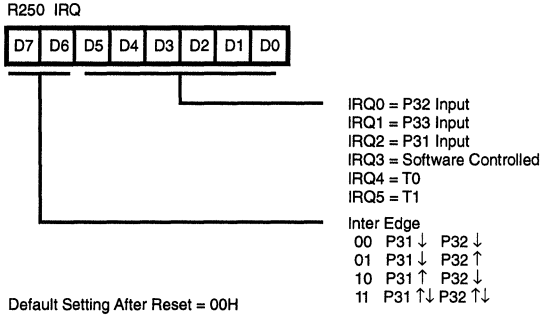

Figure 33. Interrupt Request Register (FAH: Read/Write)

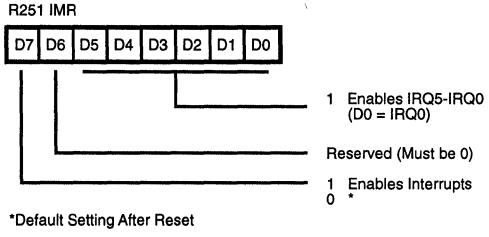

Figure 34. Interrupt Mask Register (FBH: Read/Write)

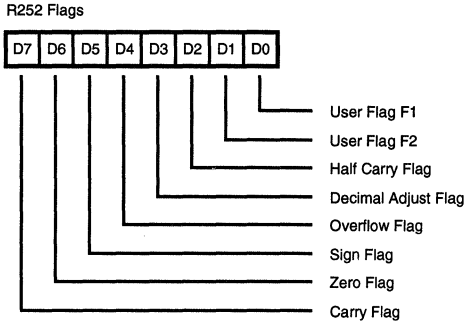

Figure 35. Flag Register (FCH: Read/Write)

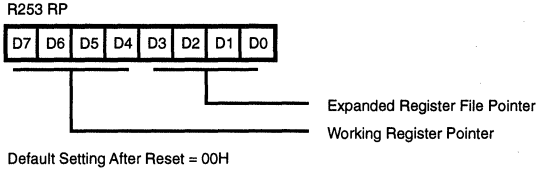

Figure 36. Register Pointer (FDH: Read/Write)

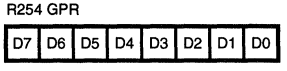

Figure 37. General Purpose Register (FEH: Read/Write)

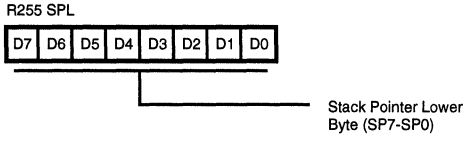

Figure 38. Stack Pointer (FFH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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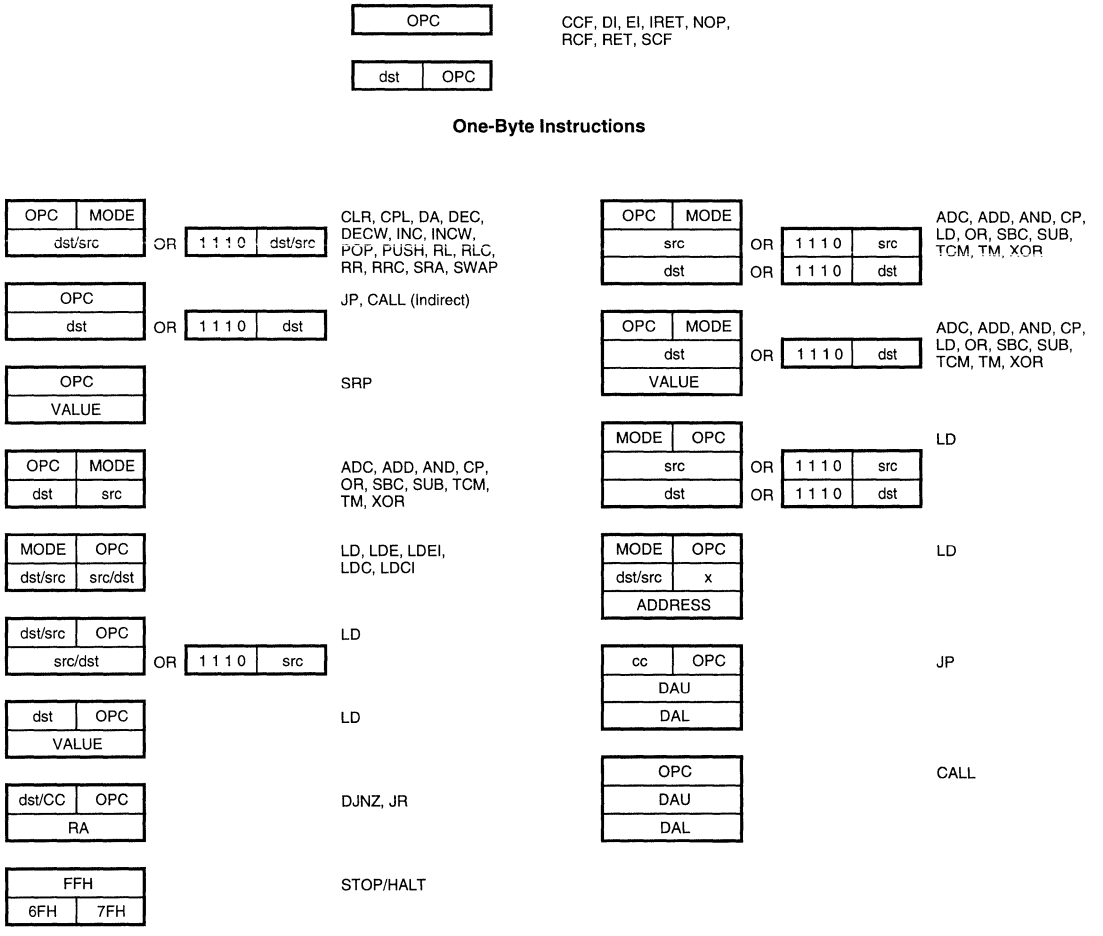
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less Than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

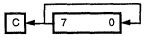
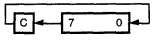
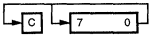
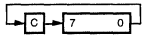
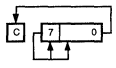
dst (7)

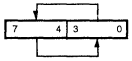
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

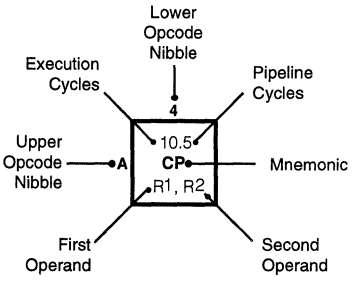
Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

2

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



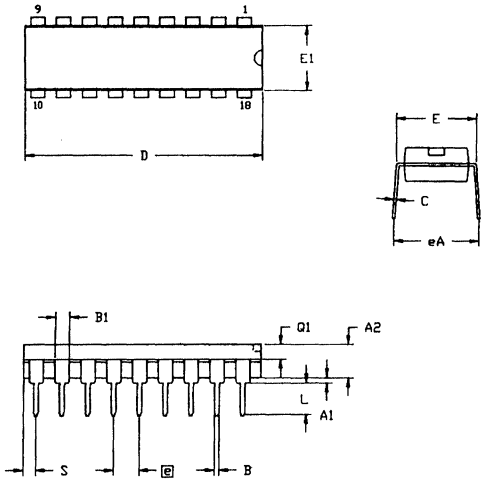
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

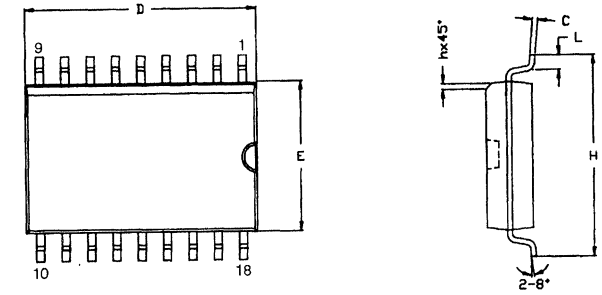
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86L29

8 MHz	8 MHz
18-Pin DIP	18-Pin Plastic SOIC
Z86L2908PSC	Z86L2908SSS

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
S = Plastic SOIC

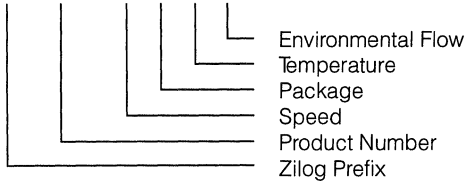
Temperature
S = 0°C to +55°C

Speed
8 = 8 MHz

Environmental
C = Plastic Standard

Example:

Z 86L29 08 P S C is an Z89L29, 8 MHz, DIP, 0°C to +55°C, Plastic Standard Flow



Z86L70/L71/L72/E72

ZILOG INFRARED REMOTE CONTROLLER FAMILY (ZIRC™)

FEATURES

- 8-Bit CMOS Microcontroller
- ROM/Package Options:
  - Z86L70 2K ROM, 128 RAM, 18-Pin SOIC/DIP
  - Z86L71 8K ROM, 256 RAM, 20-Pin DIP
  - Z86L72 16K ROM, 768 RAM, 40-Pin DIP or 44-Pin PLCC/QFP
  - Z86E72 16K OTP, 768 RAM 40-Pin DIP or 44-Pin PLCC/QFP (3V)
- 2.0V to 3.9V Operating Range (8.0 MHz)
- Low Power Consumption - 40 mW (Typical)
- Two Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
- All Digital Inputs are CMOS Levels
- 768 Bytes of RAM (748 General-Purpose) Z86L72/E72 Versions
- 256 Bytes of RAM (236 General-Purpose) for Z86L71 Version
- 128 Bytes of RAM, (124 for General-Purpose) Z86L70 Version
- Expanded Register File Control Registers
- Automatic External ROM Access Beyond 16K (Z86L72/E72 Versions)
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Low Voltage Detection and Protection
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
  - All Eight Port 2 Bits at One Time or Not

3

GENERAL DESCRIPTION

The ZIRC™ (Z86L7X) family of IR (Infrared) CCP™ (Consumer Controller Processor) Controllers are ROM-based members of the Z8® single-chip microcontroller family with 768/256/128 bytes of general-purpose RAM. The only differentiating factor between the three versions (Z86L70/71/72) is the availability of RAM, ROM, and package options. The ZIRC™ family of ROM devices (L72/E72 versions) offers the use of external memory which enables this Z8 microcontroller to be used where code flexibility is required. Zilog's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with low cost and low power consumption.

GENERAL DESCRIPTION (Continued)

The Z86L7X architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

CCP™ applications demand powerful I/O capabilities. The Z86L7X family fulfills this with three package options in which the L72/E72 version provides 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory. The lower pin count version reduces the I/O count as shown in the pin descriptions while maintaining hardware and software compatibility, thereby providing the user a wide spectrum of I/O options without major rework/changes when migrating to different family versions.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Register File is composed of 768/256/128 bytes of RAM. It includes four I/O port registers, ten control and status registers, and the rest are general purpose registers. The Expanded Register File consists of three register groups.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

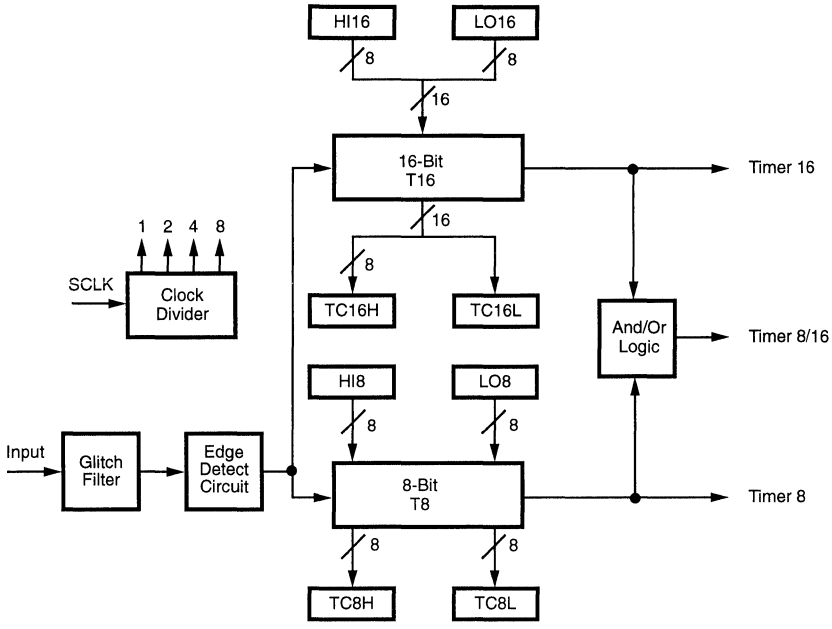


Figure 1. Counter/Timer Block Diagram

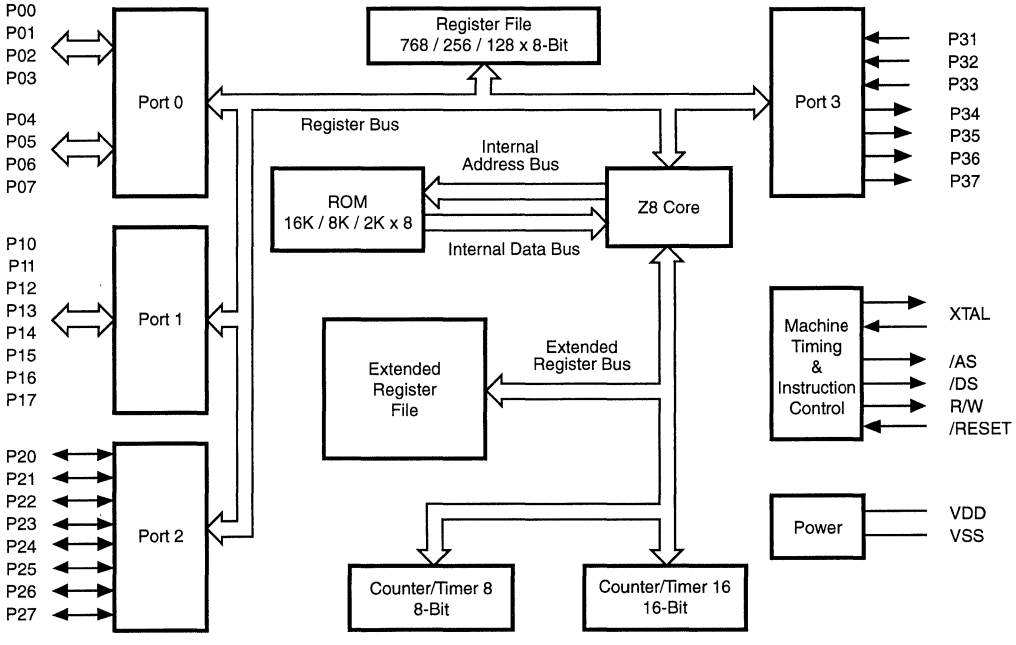


Figure 2. Functional Block Diagram

3

PIN DESCRIPTION

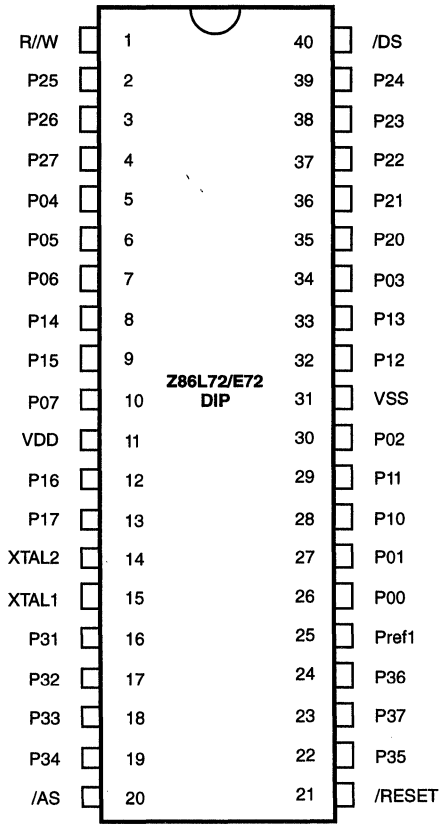


Figure 3. 40-Pin DIP Pin Assignments

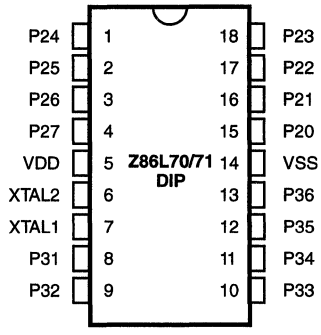


Figure 4. 18-Pin DIP Pin Assignments

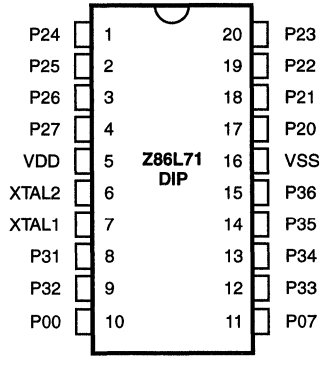


Figure 5. 20-Pin DIP Pin Assignments

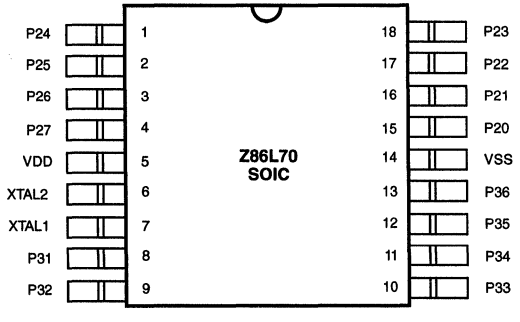


Figure 6. 18-Pin SOIC Pin Assignments

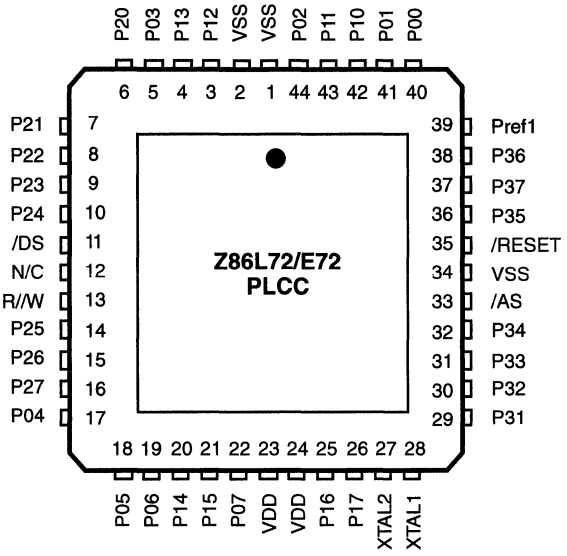


Figure 7. 44-Pin PLCC Pin Assignments

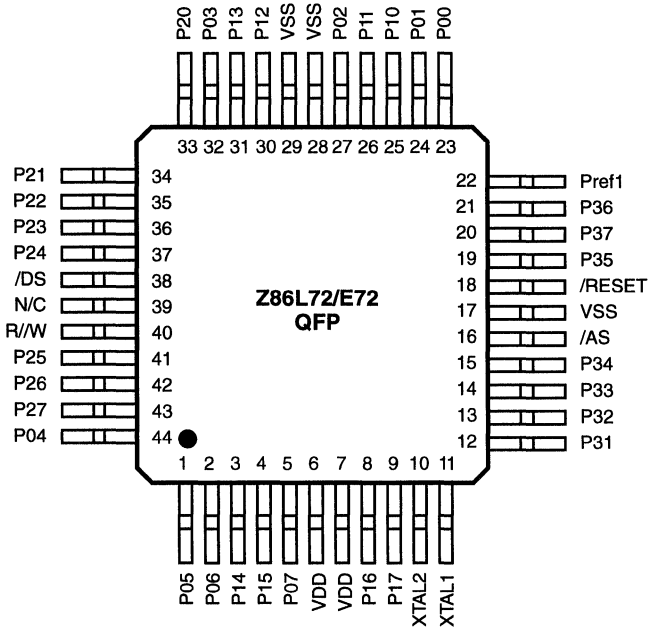


Figure 8. 44-Pin QFP Pin Assignments

3

PIN DESCRIPTION (Continued)

Table 1. Pin Identification

20-Pin DIP#	40-Pin DIP#	18-Pin DIP & SOIC#	44-Pin PLCC#	44-Pin QFP#	Symbol	Direction	Description
10	26		40	23	P00	Input/Output	Port 0 is Nibble Programmable.
	27		41	24	P01	Input/Output	Port 0 can be configured as
	30		44	27	P02	Input/Output	A15-A8 external program
	34		5	32	P03	Input/Output	ROM Address Bus.
	5		17	44	P04	Input/Output	
	6		18	1	P05	Input/Output	
	7		19	2	P06	Input/Output	
11	10		22	5	P07	Input/Output	
	28		42	25	P10	Input/Output	Port 1 is byte programmable.
	29		43	26	P11	Input/Output	Port 1 can be configured as
	32		3	30	P12	Input/Output	multiplexed A7-A0/D7-D0
	33		4	31	P13	Input/Output	external program ROM
	8		20	3	P14	Input/Output	Address/Data Bus.
	9		21	4	P15	Input/Output	
	12		25	8	P16	Input/Output	
	13		26	9	P17	Input/Output	
17	35	15	6	33	P20	Input/Output	Port 2 pins are individually
18	36	16	7	34	P21	Input/Output	configurable as input or output.
19	37	17	8	35	P22	Input/Output	
20	38	18	9	36	P23	Input/Output	
1	39	1	10	37	P24	Input/Output	
2	2	2	14	41	P25	Input/Output	
3	3	3	15	42	P26	Input/Output	
4	4	4	16	43	P27	Input/Output	
8	16	8	29	12	P31	Input	IRQ2/Modulator input
9	17	9	30	13	P32	Input	IRQ0
12	18	10	31	14	P33	Input	IRQ1
13	19	11	32	15	P34	Output	T8 output
14	22	12	36	19	P35	Output	T16 output
15	24	13	38	21	P36	Output	T8/T16 output
	23		37	20	P37	Output	
	20		33	16	/AS	Output	Address Strobe
	40		11	38	/DS	Output	Data Strobe
	1		13	40	R/W	Output	Read/Write
	21		35	18	/RESET	Input	Reset
7	15	7	28	11	XTAL1	Input	Crystal, Oscillator Clock
6	14	6	27	10	XTAL2	Output	Crystal, Oscillator Clock
5	11	5	23, 24	6, 7	V_{DD}		Power Supply
16	31	14	1, 2, 34	17, 28, 29	V_{SS}		Ground
	25		39	22	Pref1	Input	Comparator 1 Reference
			12	39	N/C		Not Connected

FUNCTIONAL DESCRIPTION

/DS *(Output, active Low).* Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS *(Output, active Low).* Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/W *Read/Write* (output, write Low). The R/W signal is Low when the CCP is writing to the external program or data memory.

Port 0 *(P07-P00).* Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R/W (Figure 9).

An optional 200 kOhms pull-up is available in a mask option on P00 and P07 only.

FUNCTIONAL DESCRIPTION (Continued)

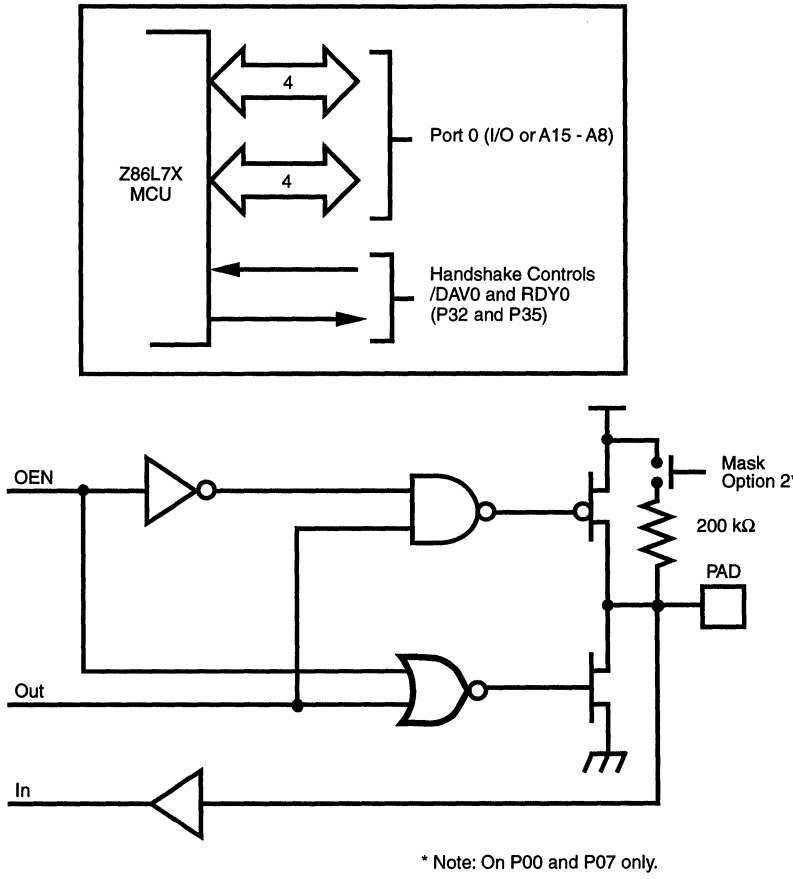


Figure 9. Port 0 Configuration

Port 1 *(P17-P10).* Port 1 is a multiplexed Address (A7-A0) and Data (D7-D0), CMOS compatible port. Port 1 is dedicated to the Zilog ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (/AS) and Data Strobe (/DS) lines, and by the Read/Write (R/W) and Data Memory (/DM) control lines. Data memory read/write operations are done through this port (Figure 10). If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the Z86L7X to share common resources in multiprocessor and DMA applications.

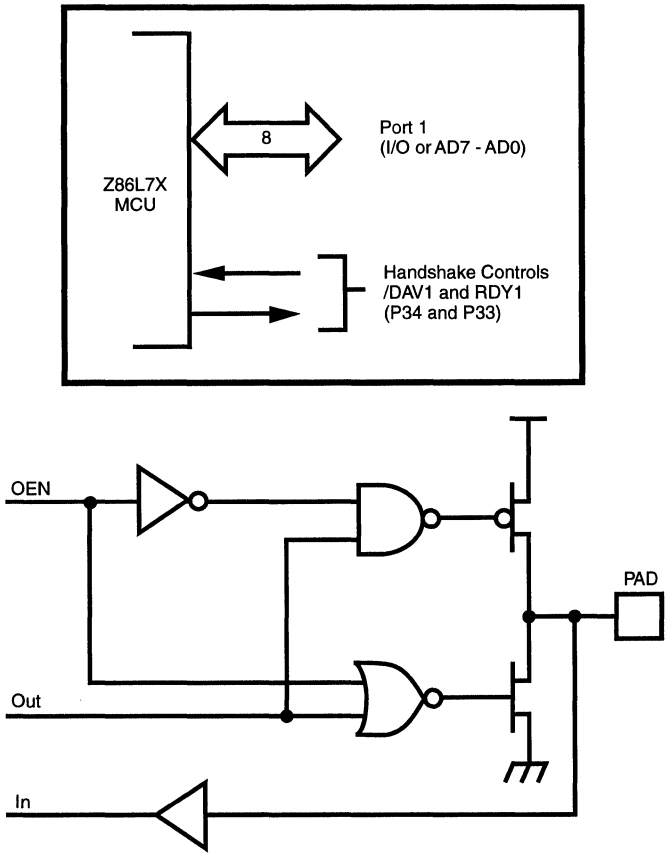


Figure 10. Port 1 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Port 2 *(P27-P20).* Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 kOhms (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 may be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2 (Figure 11). The CCP wakes up with the eight bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input OR and an AND gate which can be used to wake up the part (Figure 38). P20 can be programmed to access the edge selection circuitry (Figure 20).

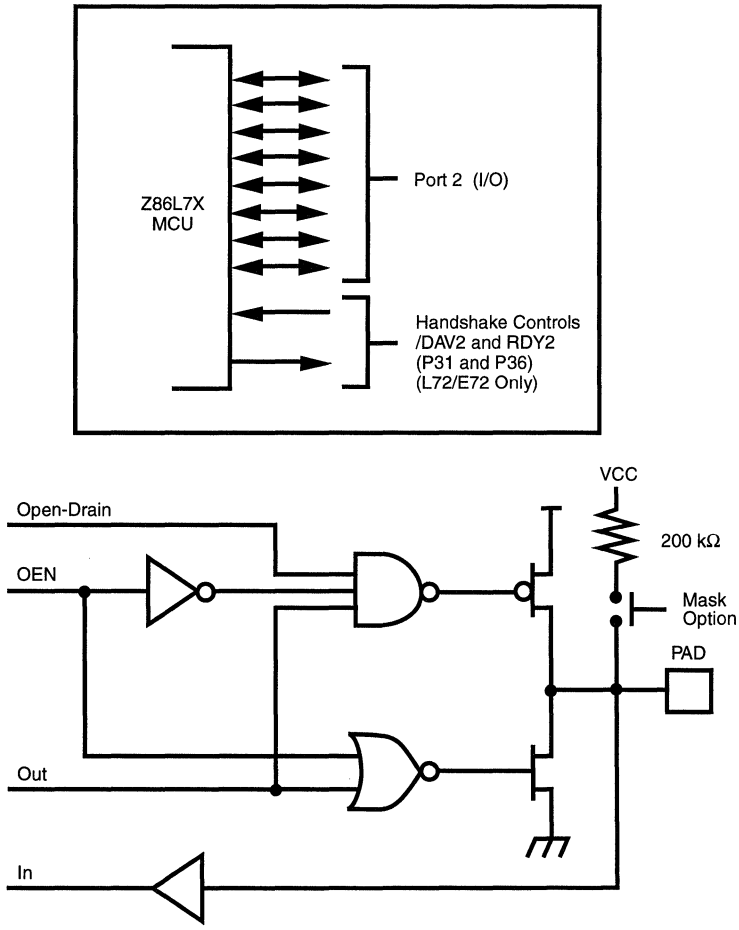


Figure 11. Port 2 Configuration

Port 3 *(P37-P31).* Port 3 is a 7-bit, CMOS compatible three fixed input and four fixed output port. Port 3 consists of three fixed input (P33-P31) and four fixed output (P37-P34), and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the edge detection circuit is through P31 or P20. Handshake lines Ports 0, 1, and 2 are available on P31 through P36. Pref2 (P33) will be in common to both comparators for versions L70 and L71 and separate for versions L72 and E72.

Port 3 provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); Data Memory Select (/DM) (Table 4).

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5-D4 of CTRI, bit 0 of CTR0 and bit 0 of CTR2.

Table 4. Pin Assignments

Pin	I/O	C/T	Comp.	Int.	P0 HS	P1 HS	P2 HS	Ext
Pref1	IN		RF1					
P31	IN	ISP	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		RF2	IRQ1		D/R		
P34	OUT	T8	A01		R/D			DM
P35	OUT	T16		R/D				
P36	OUT	T8/16					R/D	
P37	OUT		A02					
P00	I/O							

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Comparator Inputs. Port 3, P31 and P32 all have a comparator front end. The comparator reference voltages are on P33 and Pref1. The internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources can be used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 for P33 (Figure 13).

Comparator Outputs. These may be programmed to be outputted on P34 and P37 through the PCON register (Figure 12).

/RESET *(Input, active Low).* Initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line should be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the L7X that will not allow an external reset to occur.

FUNCTIONAL DESCRIPTION (Continued)

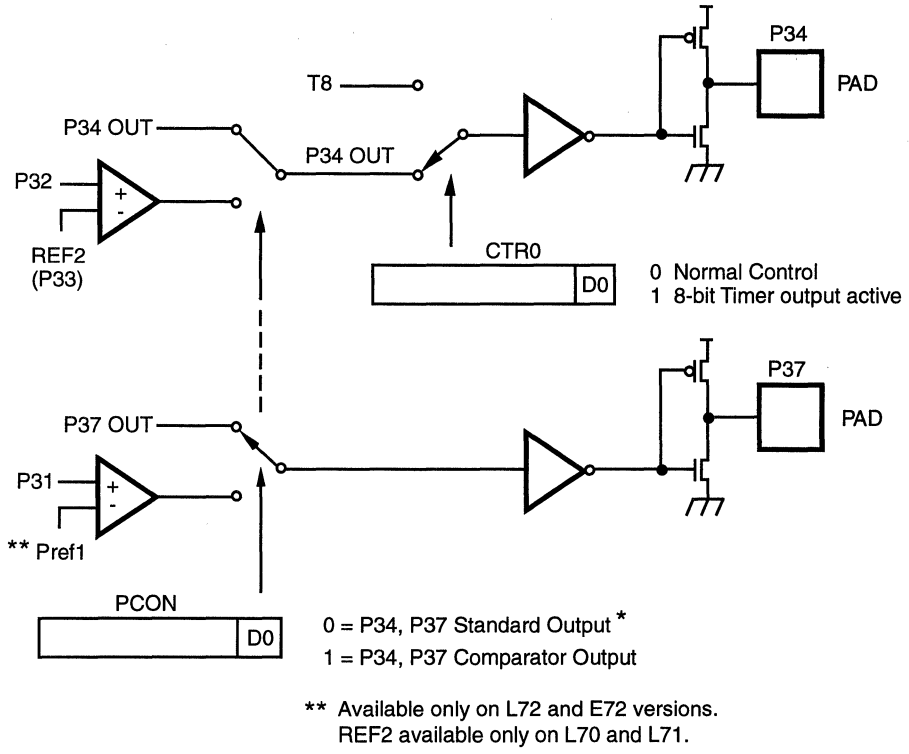


Figure 12. Port 3 Configuration

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86L7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms. The Z86L7X does not reset WDTMR, SMR, P2M, or P3M registers on a Stop-Mode Recovery operation.

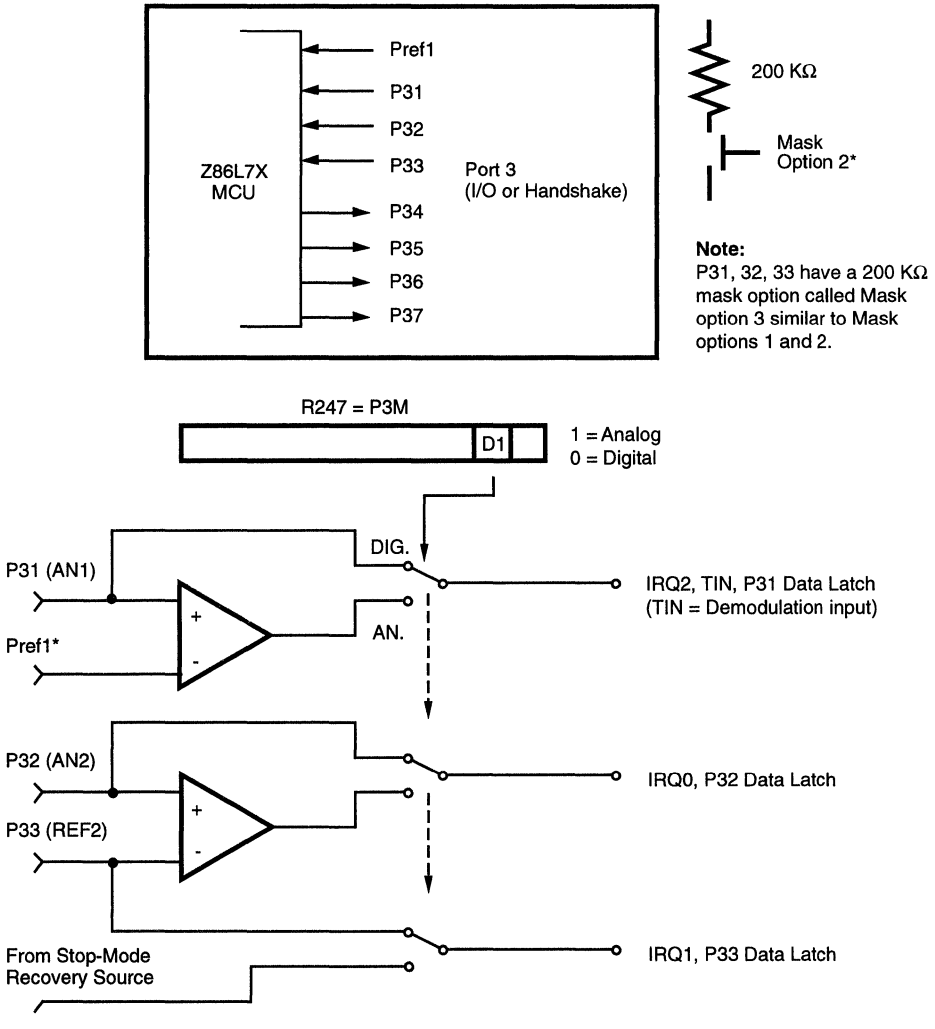


Figure 13. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

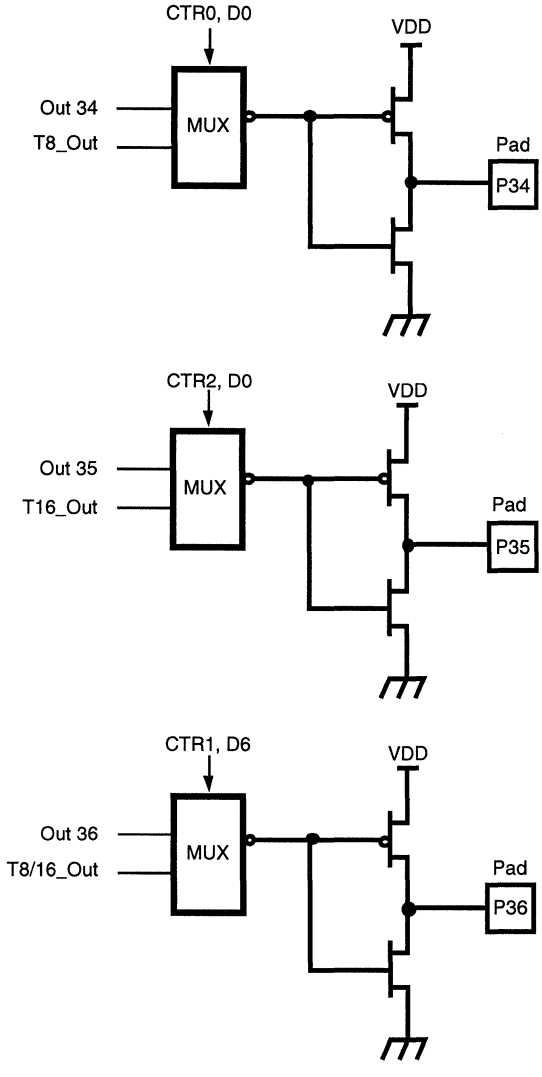


Figure 14. Port 3 Configuration

The Z8 CCP incorporates special functions to enhance the Z8's functionality in consumer and battery operated applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection
- External Reset (Z86L72 and E72 only)

Program Memory. The Z86L7X addresses up to 2K, 8K, and 16 Kbytes of internal program memory, with the remainder being external memory (Figure 15). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses 12 to 2K, 8K, or 16K (dependent on version) consist of on-chip mask-programmed ROM. At addresses 16K and greater, the Z86L72/E72 executes external program memory fetches (refer to external memory timing specifications).

RAM. The Z86L72 and Z86E72 versions have 768-byte RAM. 256 of them are in the register file. The other 512 bytes are mapped into the External ROM address between 65023 through 65535.

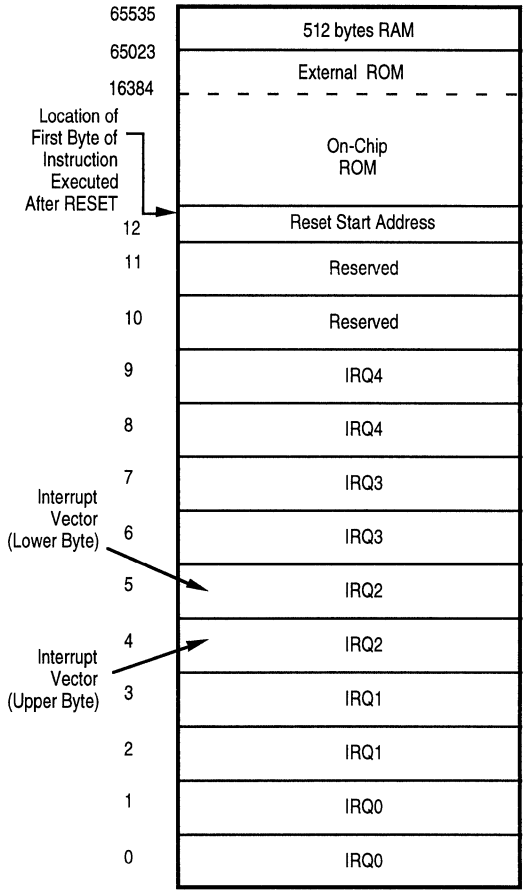


Figure 15. Program Memory Map

3

FUNCTIONAL DESCRIPTION (Continued)

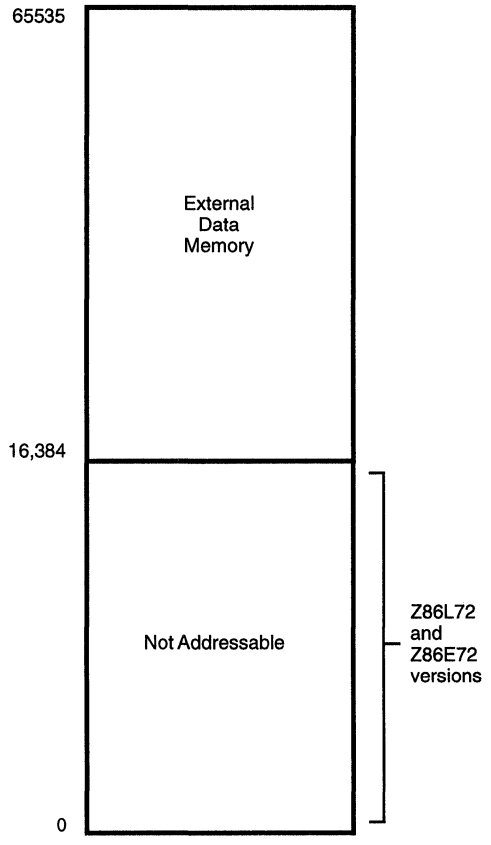


Figure 16. Data Memory Map

External Data Memory *(/DM).* The Z86L7X addresses up to 48K, 56K, or 62 Kbytes of external data memory beginning at location 000CH (Figure 16). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 17).

The upper nibble of the register pointer (Figure 19) selects which group of 16 bytes in the register file, out of the full 256, will be accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86L70/71/72, Banks F and D are implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86L71: (See Figure 17)

R253 RP = 00H
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0DH
R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD    RP, #0DH     Select ERF D for access and
                   register Bank 0 as
                   the working register group
LD    R0,#xx       access CTRL0
LD    1, #xx       access CTRL1
LD    RP, #7DH     Select expanded register group
                   (ERF) group D for access and
                   register Bank 7 as the working
                   register bank
LD    R1, 2        CTRL2 → register 71H
```

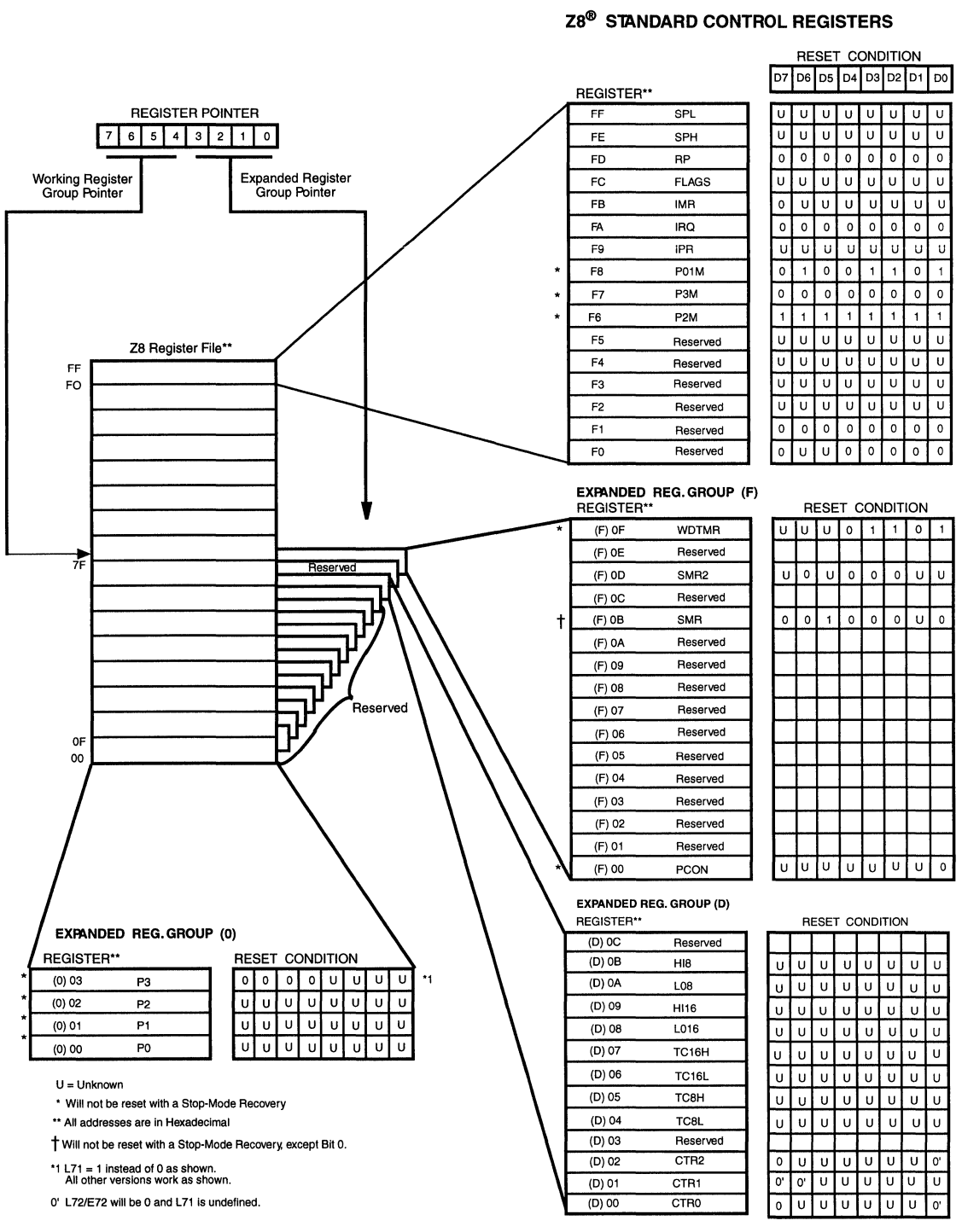


Figure 17. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

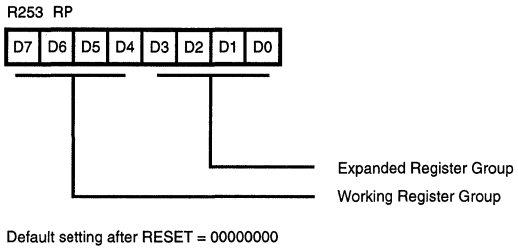


Figure 18. Register Pointer Register

Register File. The register file consists of four I/O port registers, 124, 256, or 768 general-purpose registers with 15 control and status registers (R3-R0, R239-R4, and R255-R240, respectively), plus three Expanded Register Groups (0, D, and F) which reside in the expanded register group. Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 19). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Register Bank E0-EF is only accessed through working registers and indirect addressing modes.

Stack. The Z86L7X external data memory or the internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the general-purpose registers (R4-R112/239/748). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH will be loaded into Port 0 whenever the internal stack is accessed.

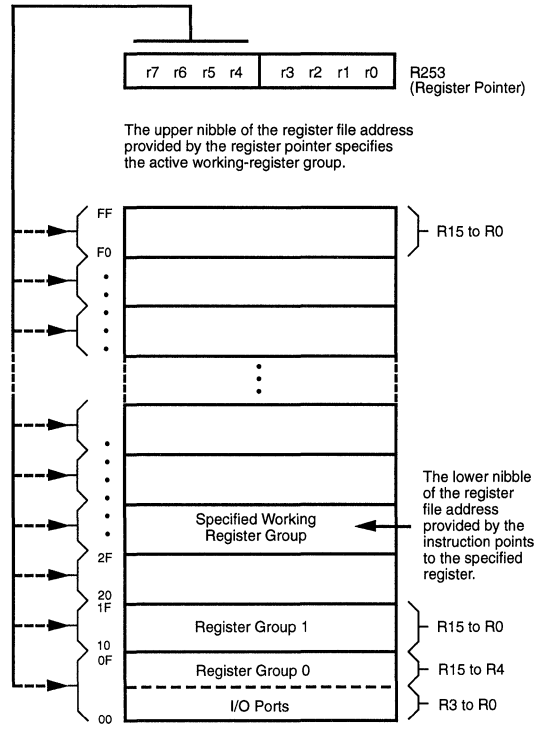


Figure 19. Register Pointer

COUNTER/TIMER REGISTER DESCRIPTION

Expanded Register Group D			
(D)%0C	Reserved	(D)%05	TC8H
(D)%0B	HI8	(D)%04	TC8L
(D)%0A	LO8	(D)%03	Reserved
(D)%09	HI16	(D)%02	CTR2
(D)%08	LO16	(D)%01	CTR1
(D)%07	TC16H	(D)%00	CTR0
(D)%06	TC16L		

Register Description

HI8(D)%0B: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Field	Bit Position		Value	Description
T8_Capture_HI	76543210	R		Captured Data
		W		No Effect

L08(D)%0A: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Field	Bit Position		Value	Description
T8_Capture_L0	76543210	R		Captured Data
		W		No Effect

HI16(D)%09: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Value	Description
T16_Capture_HI	76543210	R		Captured Data
		W		No Effect

L016(D)%08: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Value	Description
T16_Capture_LO	76543210	R		Captured Data
		W		No Effect

COUNTER/TIMER REGISTER DESCRIPTION (Continued)

TC16H(D)%07: Counter/Timer2 MS-Byte Hold Register.

Field	Bit Position		Value	Description
T16_Data_HI	76543210	R/W		Data

TC16L(D)%06: Counter/Timer2 LS-Byte Hold Register.

Field	Bit Position		Value	Description
T16_Data_LO	76543210	R/W		Data

TC8H(D)%05: Counter/Timer8 High Hold Register.

Field	Bit Position		Value	Description
T8_Level_HI	76543210	R/W		Data

TC8L(D)%04: Counter/Timer8 Low Hold Register.

Field	Bit Position		Value	Description
T8_Level_LO	76543210	R/W		Data

CTR0 (D)00: Counter/Timer8 Control Register.

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0*	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0	P34 as Port Output
			1	T8 Output on P34

Notes:
* Indicates the value upon Power-On Reset.

CTR0: Counter/Timer8 Control Register Description

T8 Enable. This field enables T8 when set (written) to 1.

Single/Modulo-N. When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to1 (single pass), the counter stops when the terminal count is reached.

Time-Out. This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to this location. **This is the only way to reset this status condition, therefore, care should be taken to reset this bit prior to using/enabling the counter/timers.**

Note:
Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers will be ORed or ANDed with the designated value and then written back into the registers. Example: When the status of bit 5 is 1, a reset condition will occur.

T8 Clock. Defines the frequency of the input signal to T8.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask. Set this bit to allow interrupt when T8 has a time out.

P34_Out. This bit defines whether P34 is used as a normal output pin or the T8 output.

COUNTER/TIMER REGISTER DESCRIPTION (Continued)

CTR1(D)%01: Controls the functions in common with the T8 and T16.

Field	Bit Position		Value	Description
Mode	7-------	R/W	0	Transmit Mode
			1	Demodulation Mode
P36_Out/	-6------	R/W		Transmit Mode
Demodulator_Input			0	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/	--54----	R/W		Transmit Mode
Edge _Detect			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	----32--	R/W		Transmit Mode
Glitch_Filter			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	16 SCLK Cycle
Initial_T8_Out/	------1-			Transmit Mode
Rising_Edge		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	-------0			Transmit Mode
Falling _Edge		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 1

CTR1 Register Description

Mode. If it is 0, the Counter/Timers are in the transmit mode, otherwise they are in the demodulation mode.

P36_Out/Demodulator_Input. In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect. In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter. In Transmit Mode, this field defines whether T8 and T16 are in the "Ping-Pong" mode or in independent normal operation mode. Setting this field to "Normal Operation Mode" terminates the "Ping-Pong Mode" operation. When set to 1, $\overline{T16}$ is immediately functional and can cause interrupts. The output is forced to a 0. When set to 11, T16 is immediately forced to a 1.

In Demodulation Mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_Out/Rising_Edge. In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge. In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2).

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

COUNTER/TIMER REGISTER DESCRIPTION (Continued)

CTR2 (D)%02: Counter/Timer16 Control Register.

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Submode	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P35_Out	-------0	R/W	0	P35 as Port Output
			1	T16 Output on P35

Notes:
* Indicates the value upon Power-On Reset.

CTR2 Description

T16_Enable. This field enables T16 when set to 1.

Single/Modulo-N. In Transmit Mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0 , T16 captures and reloads on detection of all the edges; when set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode.

Time_Out. This bit is set when T16 times out (terminal count reached). In order to reset it, a 1 should be written to this location.

T16_Clock. Defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask. Set this bit to allow interrupt when T16 times out.

P35_Out. This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2(F)%0D: Stop-Mode Recovery Register 2.

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0* 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000* 001 010 011 100 101 110 111	A. POR Only B. NAND of P23-P20 C. NAND or P27-P20 D. NOR of P33-P33 E. NAND of P33-P31 F. NOR of P33-P31, P00,P07 G. NAND of P33-P31,P00,P07 H. NAND of P33-P31,P22-P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Indicates the value upon Power-On Reset.

Port pins configured as outputs are ignored as an SMR2 recover source. For example, if NAND of P23-P20 is selected as the recover source and P20 is configured as output, then P20 is ignored as a recover source. The effective recover source in this case is NAND of P23-P21.

FUNCTIONAL DESCRIPTION (Continued)
Counter/Timer Functional Blocks

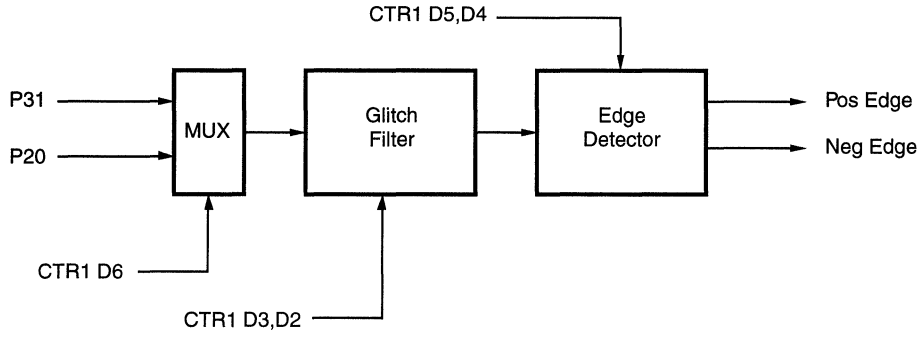


Figure 20. Glitch Filter Circuitry

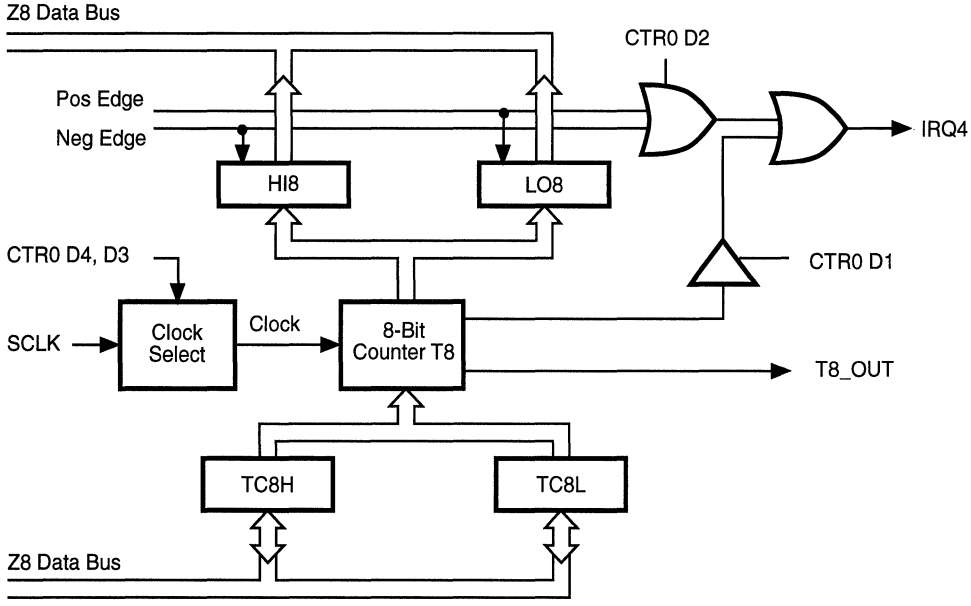


Figure 21. 8-bit Counter/Timer Circuits

Input Circuit

The edge detector monitors the input signal on P31 or P21. Based on CTR1 D5-D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal which have a width less than specified (CTR1 D3, D2) are filtered out.

T8 Transmit Mode

When T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded, otherwise TC8H is loaded into the counter. In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1) (Figure 22). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5) and generates an interrupt if enabled (CTR0 D1) (Figure 23). This completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. ***An initial count of 1 is not allowed (a non-function will occur).*** An initial count of 0 will cause TC8 to count from 0 to %FF to %FE (Note, % is used for hexadecimal values). Transition from 0 to %FF is not a time-out condition.

Note:
Using the same instructions for stopping the counter/timers and setting the status bits is not recommended. Two successive commands, first stopping the counter/timers, then resetting the status bits is necessary. This is required because it takes one counter/timer clock interval for the initiated event to actually occur.

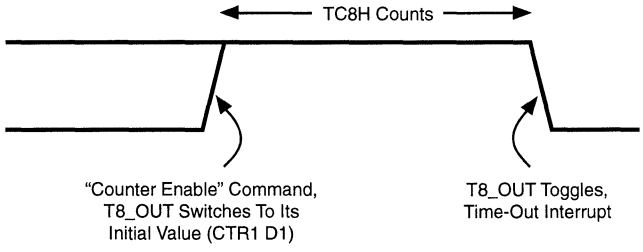


Figure 22. T8_OUT in Single-Pass Mode

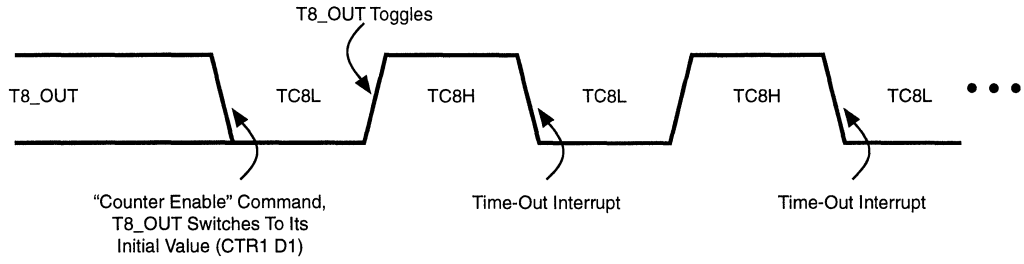


Figure 23. T8_OUT in Modulo-N Mode

FUNCTIONAL DESCRIPTION (Continued)

T8 Demodulation Mode

The user should program TC8L and TC8H to %FF. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8, if negative edge, HI8. One of the edge detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with %FF and starts counting again. Should T8 reach 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from %FF (Figure 24).

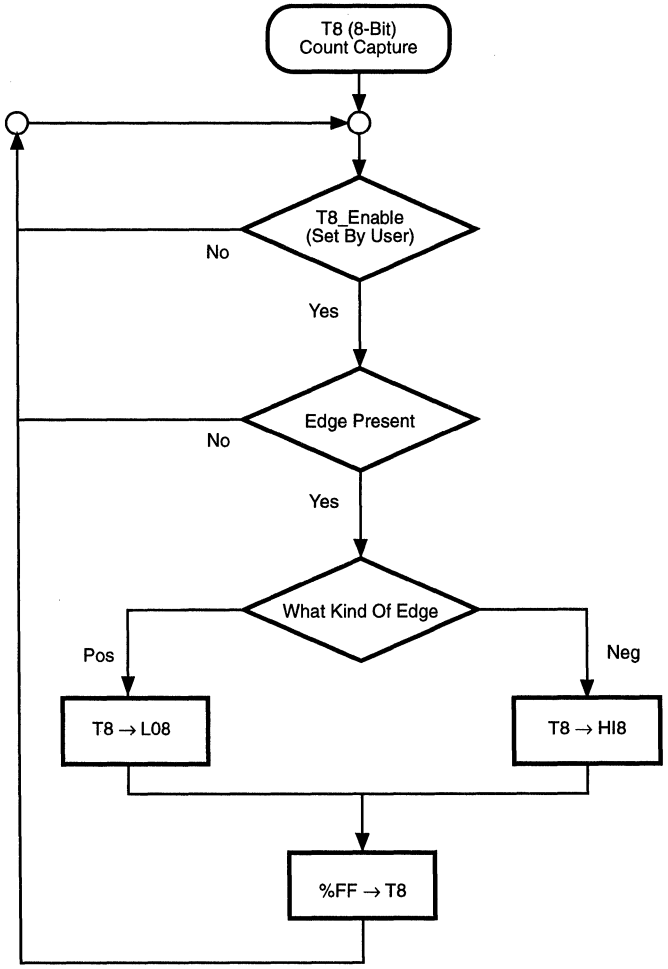


Figure 24. Demodulation Mode Count Capture Flowchart

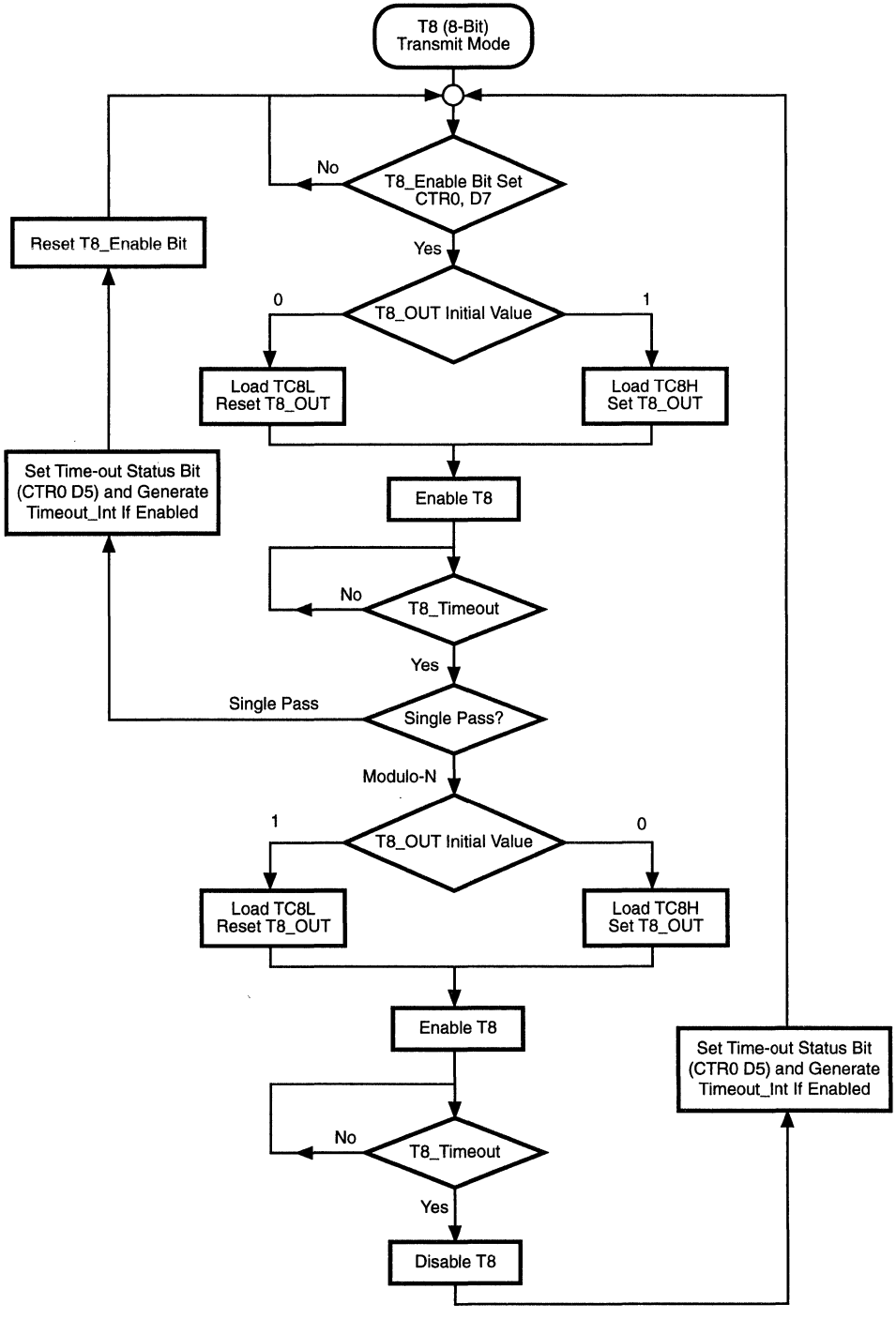


Figure 25. Transmit Mode Flowchart

FUNCTIONAL DESCRIPTION (Continued)

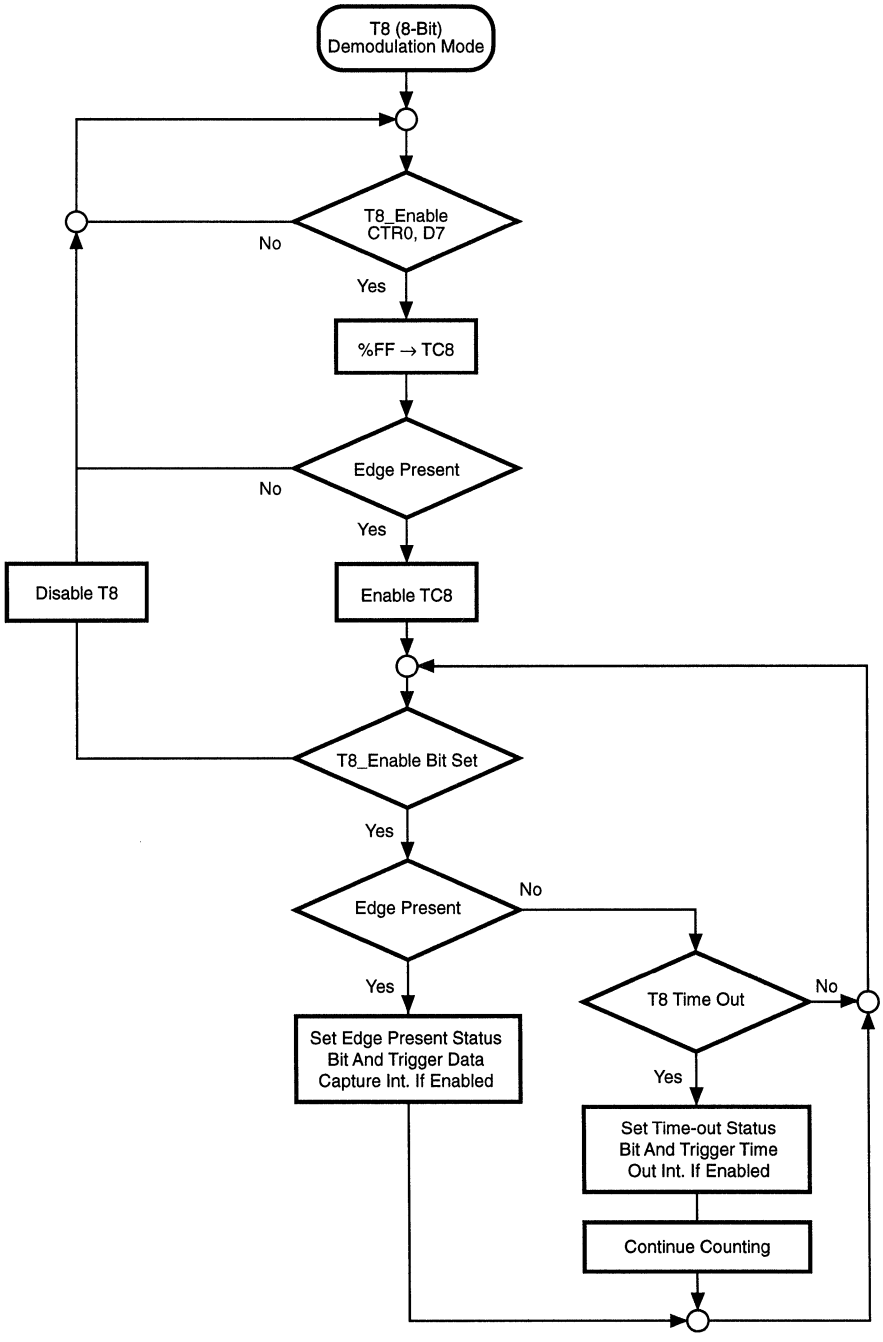


Figure 26. Demodulation Mode Flowchart

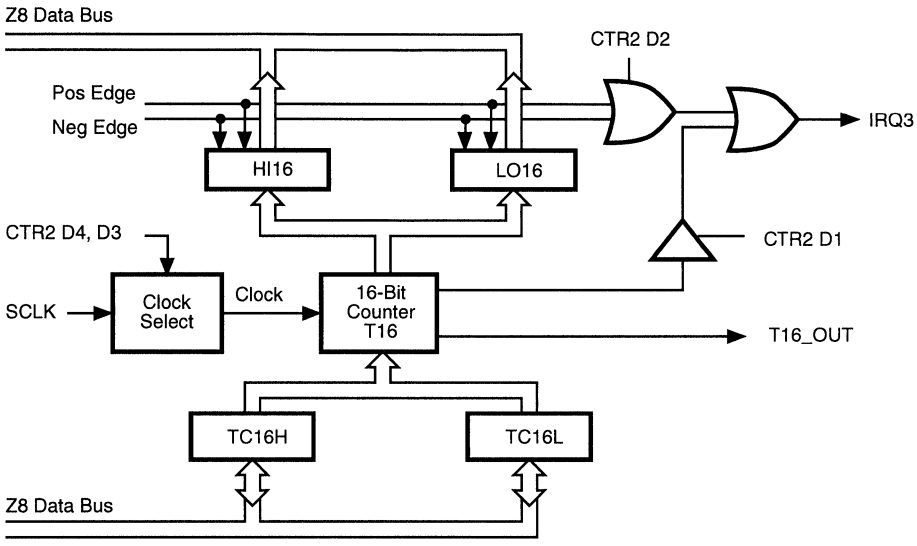


Figure 27. 16-bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 when not enabled is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. The user can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set. Note that global interrupts will override this function as described in the interrupts section. If T16 is in Single-Pass Mode, it is stopped at this point. If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 will cause T16 to count from 0 to %FF FF to %FFFE. Transition from 0 to %FFFF is not a time-out condition.

FUNCTIONAL DESCRIPTION (Continued)

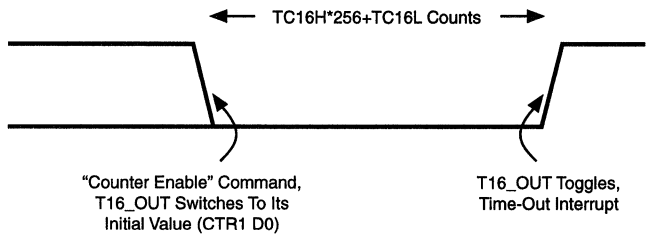


Figure 28. T16_OUT in Single-Pass Mode

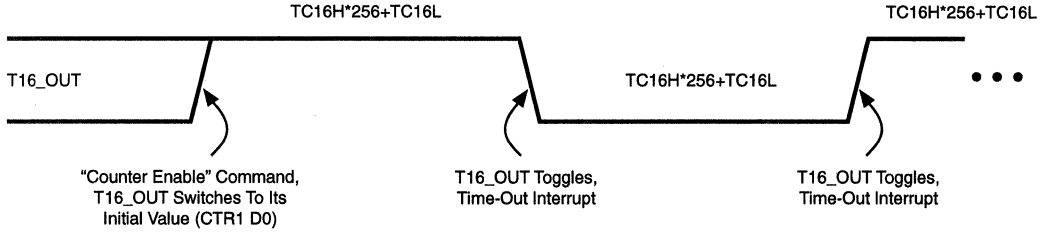


Figure 29. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to %FF. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, T16 captures HI16 and LO16 and then reloads.

If D6 of CTR2 is 0: When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1 D1, D0) is set and an interrupt is generated if enabled (CTR2 D2). T16 is loaded with %FFFF and starts again.

If D6 of CTR2 is 1: T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 will cause T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 will capture and reload on the next edge (rising, falling, or both depending on CTR1 D5, D4) but continue to ignore subsequent edges.

Should T16 reach 0, it continues counting from %FFFF; meanwhile, a status bit (CTR2 D5) is set and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6) and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. The user can begin the operation by enabling either T8 or T16 (CTR0 D1 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T0_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T2_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note:

Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function. Disable the counter/timers, then reset the status flags prior to instituting this operation.

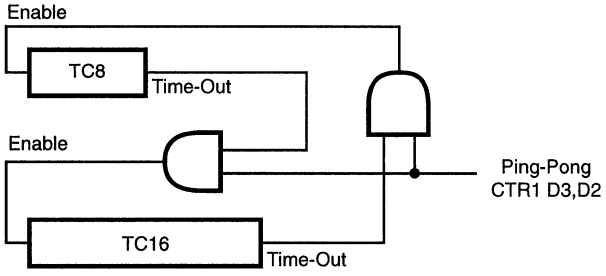


Figure 30. Ping-Pong Mode

To Initiate Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) will be cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) will be set every time the counter/timers reach the terminal count.

3

FUNCTIONAL DESCRIPTION (Continued)

To Terminate Ping-Pong Mode

Change Transmit Mode to Normal Mode (CTR1 D2, D3). Notice that Ping-Pong Mode is not actually stopped until one of the timer/counter's time-out. Before the actual termination of Png-Pong Mode, the user should not change the value of CTR0 or CTR2, except for resetting the time-out status bit. Here is an example for terminating Ping-Pong Mode safely:

```
        or      CTR0,#%20           ;reset T8 time-out status bit
loop_a:
        tm      CTR0,#%20
        jr      z,loop_a            ;wait until T8 times-out

        ld      CTR1,#00000000b     ;change to Normal Mode

        or      CTR2,#%20           ;reset T16 time-out status bit
loop_b:
        tm      CTR2,#%20
        jr      z,loop_b            ;wait until T16 times-out

                                    ;now Ping-Pong Mode is actually
        ld      CTR0,#00100000b     ;terminated and user can re-program T8
        ld      CTR2,#00100000b     ;and T16
```

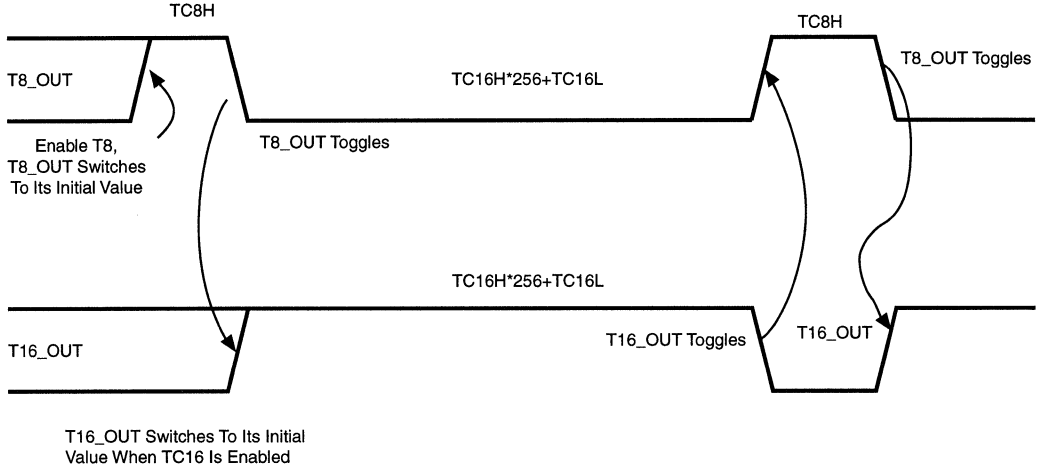


Figure 31. T8_OUT and T16_OUT in Ping-Pong Mode

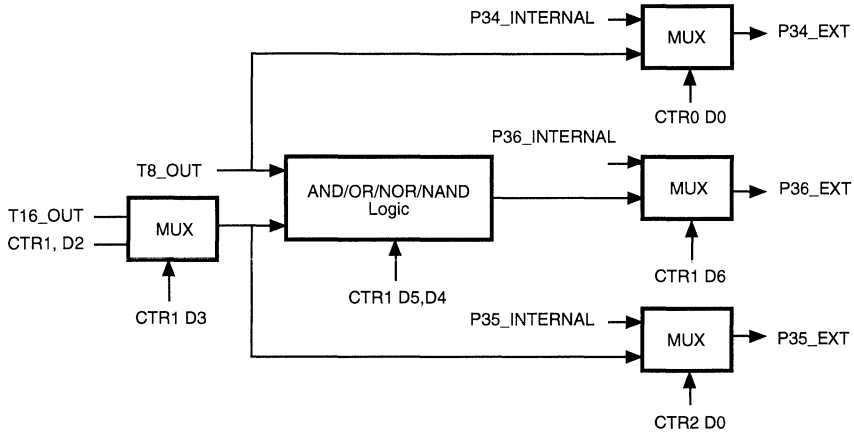


Figure 32. Output Circuit

Interrupts. The Z86L7X has five different interrupts. The interrupts are maskable and prioritized (Figure 33). The five sources are divided as follows: three sources are claimed by Port 3 lines P33-P31, the remaining two by the counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

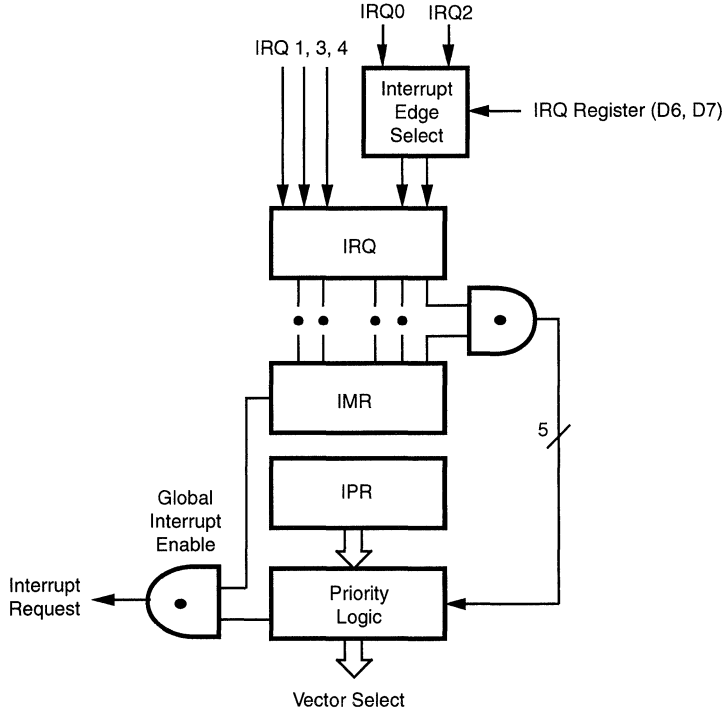


Figure 33. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L7X interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 6.

Table 6. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86L7X on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86L7X on-chip oscillator may be driven with a low cost RC network or other suitable external clock source.

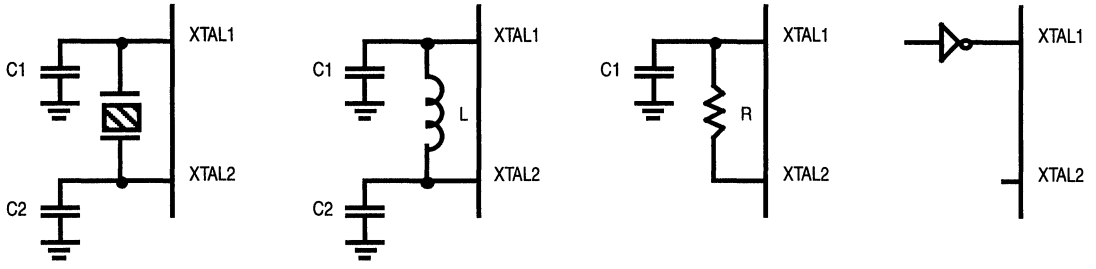
The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 34).

Power-On Reset *(POR).* A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT Time-Out.

The POR time is a nominal 5 ms. Bit 7 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, LC oscillators).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

* Preliminary value including pin parasitics

LC
C1, C2 = 22 pF

L = 130 µH *
f = 3 MHz *

RC
@ 3V VCC (TYP)

C1 = 33 pF *
R = 1K *

External Clock

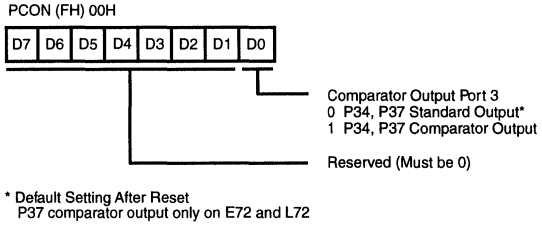
Figure 34. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. STOP mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF    NOP     ; clear the pipeline
6F    STOP    ; enter STOP mode
              or
FF    NOP     ; clear the pipeline
7F    HALT    ; enter HALT mode
```

Port Configuration Register *(PCON).* The PCON register configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00 (Figure 35).



* Default Setting After Reset
P37 comparator output only on E72 and L72

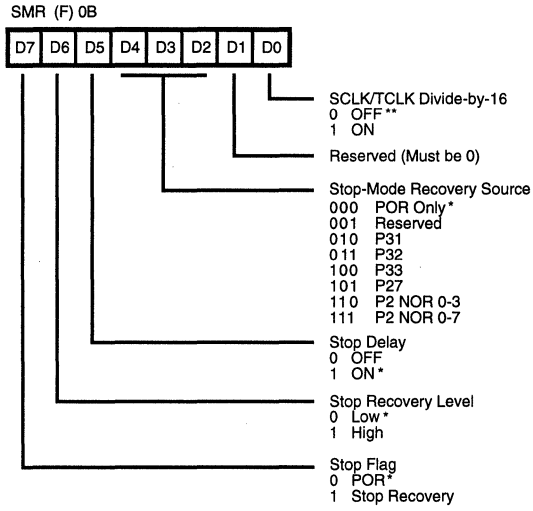
Figure 35. Port Configuration Register (PCON) (Write Only)

3

FUNCTIONAL DESCRIPTION (Continued)

Comparator Output Port 3 *(D0).* Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Stop-Mode Recovery Register *(SMR).* This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 36). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



* Default Setting After Reset
** Default Setting After Reset and Stop-Mode Recovery

Figure 36. Stop-Mode Recovery Register

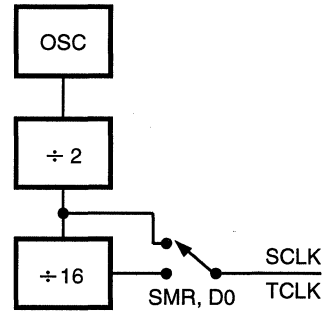


Figure 37. SCLK Circuit

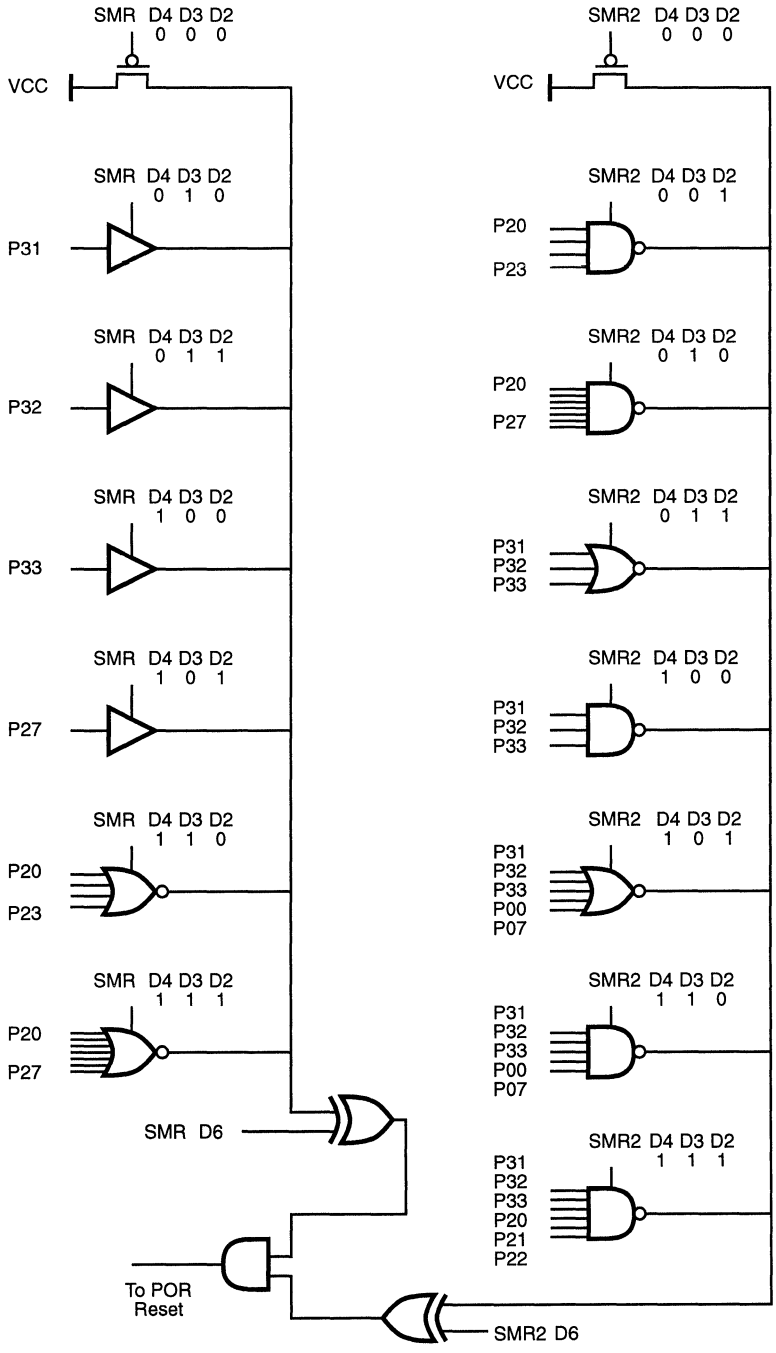


Figure 38. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select *(D0).* D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

Stop-Mode Recovery Source *(D2, D3, and D4).* These three bits of the SMR specify the wake up source of the STOP recovery (Figure 38 and Table 7).

Table 7. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note:
Any Port 2 bit defined as an output will drive the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to SMR2 register for other recover sources.

Stop-Mode Recovery Delay Select *(D5).* This bit, if High, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the "fast" wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Edge Select *(D6).* A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86L7X from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start *(D7).* This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device will be reset by POR/WDT Reset. A 1 in this bit (warm) indicates that the device awakens by a SMR source. This is a READ only bit.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 39). This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 40). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:

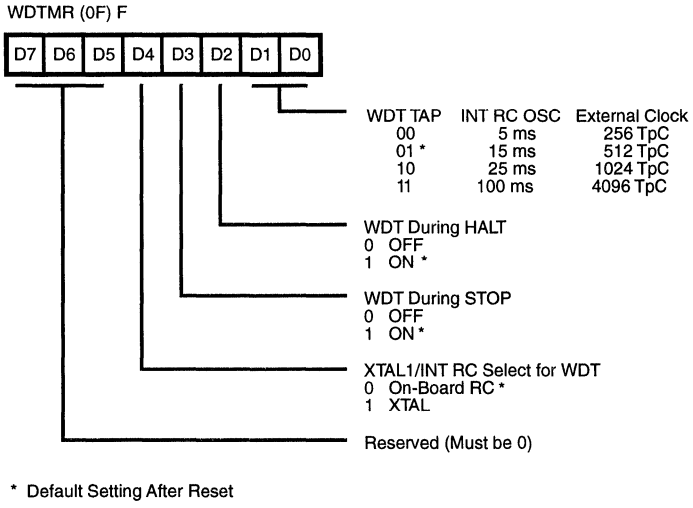


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select *(D0, D1).* Selects the WDT time period. It is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle.
The default on reset is 15 ms.
See Figures 28 to 29 for details.

WDTMR During HALT *(D2).* This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP *(D3).* This bit determines whether or not the WDT is active during STOP mode. Since the XTAL clock is stopped during STOP mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT *(D4).* This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

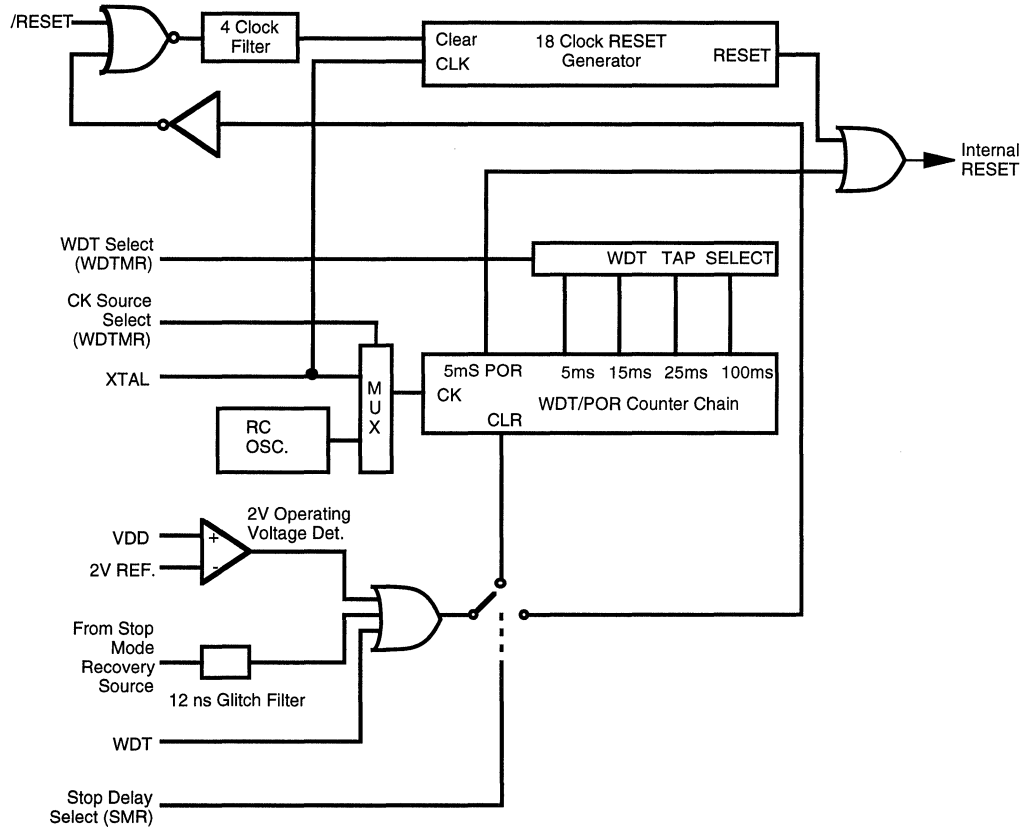


Figure 40. Resets and WDT

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{BO} (Low Voltage). The minimum operating voltage varies with the temperature and operating frequency, while V_{BO} varies with temperature only.

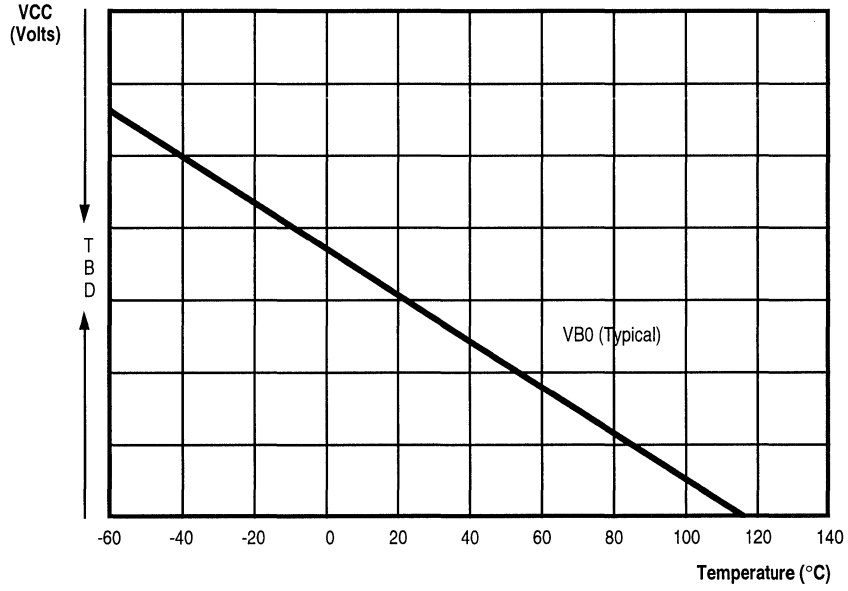
The Low Voltage trip voltage (V_{BO}) is less than 2.1V under the following conditions:

Maximum (V_{BO}) Conditions:

T_A = –0°C, +55°C Internal clock frequency equal to or less than 4.0 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device functions normally at or above 2.0V under all conditions. Below 2.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point V_{BO} is reached, below which reset is globally driven. The device is guaranteed to function normally at supply voltages above the V_{BO} trip point for the temperatures and operating frequencies in maximum V_{BO} conditions. The actual V_{BO} trip point is a function of temperature and process parameters (Figure 41).



* Power-on Reset threshold for VCC and 8.0 MHz VBO overlap

Figure 41. Typical Z86L7X Low Voltage Voltage vs Temperature at 8 MHz

3

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 42).

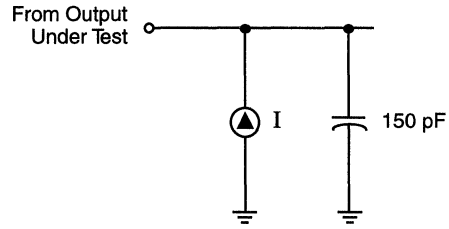


Figure 42. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS

Sym	Parameter	V_{CC}	T_A = 0°C to +55°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
	Max Input Voltage	2.0V		7		V	I_{IN} 250 µA	
		3.9V		7		V	I_{IN} 250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	1.3	V		
		3.9V	0.7 V_{CC}	V_{CC} + 0.3	2.5	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		3.9V	V_{CC} – 0.4		3.7	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36)	2.0V	0.7 V_{CC}			V	I_{OH} = –7 mA	
		3.9V	0.7 V_{CC}			V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		3.9V		0.4	0.1	V	I_{OL} = <4.0 mA	
V_{OL2}	Output Low Voltage	2.0V		0.8	0.3	V	I_{OL} = 2.0 mA 3 Pin Max	
		3.9V		0.8	0.5	V	I_{OL} = 8.0 mA 3 Pin Max	
V_{OL2}	Output Low Voltage (P20-P22, P36 and P00)	2.0V		0.8	0.3	V	I_{OL} = 10 mA	[9]
		3.9V		0.8	0.5	V	I_{OL} = 10 mA 2 O/P only	
V_{RH}	Reset Input High Voltage	2.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		3.9V	0.8 V_{CC}	V_{CC}	3.0	V		
V_{RI}	Reset Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5			
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9			
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
I_{IL}	Input Leakage	2.0V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	2.0V		–45	–20	µA		
		3.9V		–55	–30	µA		
I_{CC}	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	[4, 5]
		3.9V		15	10	mA	@ 8.0 MHz	[4, 5]

3

DC CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +55°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
I_{CC1}	Standby Current	2.0V		3	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8.0 MHz	[4,5]
		3.9V		5	4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8.0 MHz	[4,5]
		2.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
		3.9V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
I_{CC2}	Standby Current	2.0V		8	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,8]
		3.9V		10	3	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,8]
		2.0V		500	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,8]
		3.9V		800	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,8]
T_{POR}	Power-On Reset	2.0V	15	75	13	ms		
		3.9V	5	20	7	ms		
V_{BO}	V_{CC} Brown-Out Voltage			2.15	1.7	V	8 MHz max Ext. CLK Freq.	[7]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Frequency
Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
External Clock Drive	0.3 mA	5	mA	8.0 MHz

[2] GND = 0V
[3] 2.0V to 3.9V
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{BO} increases as the temperature decreases.
[8] Oscillator stopped.
[9] Two outputs at a time, independent to other outputs.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

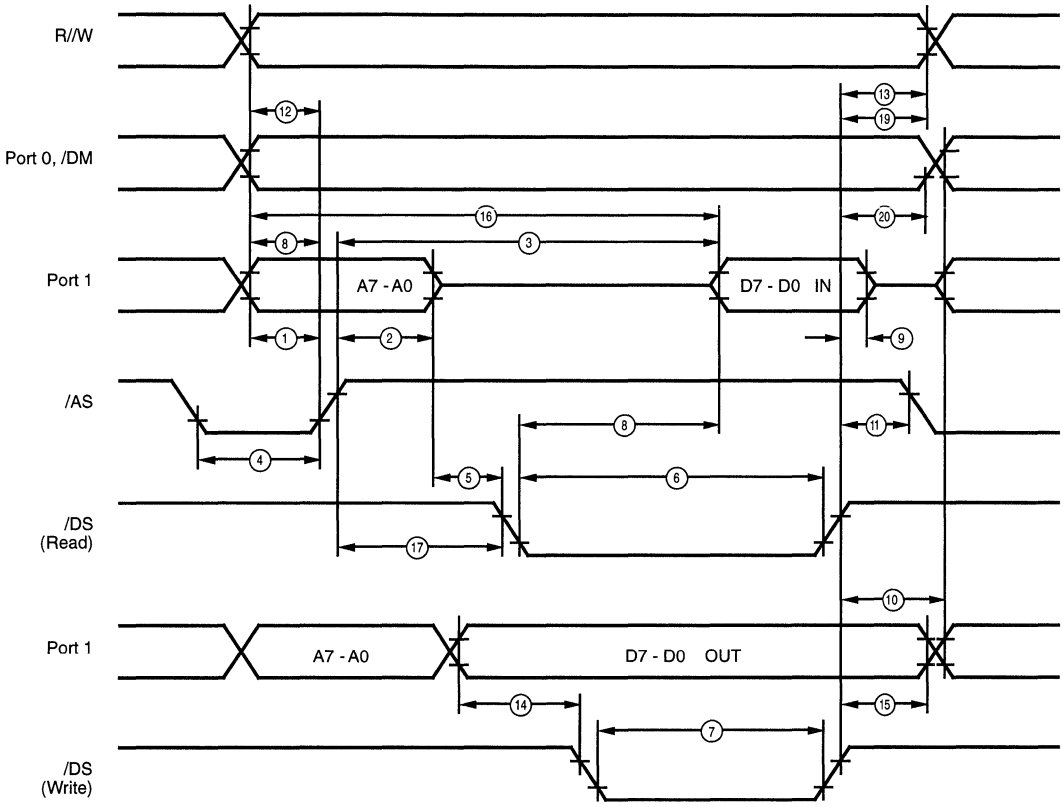


Figure 43. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No.	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to	2.0V	55		ns	[2]
		/AS Rising Delay	3.9V	55		ns	
2	TdAS(A)	/AS Rising to Address	2.0V	70		ns	[2]
		Float Delay	3.9V	70		ns	
3	TdAS(DR)	/AS Rising to Read	2.0V		400	ns	[1, 2]
		Data Required Valid	3.9V		400	ns	
4	TwAS	/AS Low Width	2.0V	80		ns	[2]
			3.9V	80		ns	
5	Td	Address Float to	2.0V	0		ns	
		/DS Falling	3.9V	0		ns	
6	TwDSR	/DS (Read) Low Width	2.0V	300		ns	[1, 2]
			3.9V	300		ns	
7	TwDSW	/DS (Write) Low Width	2.0V	165		ns	[1, 2]
			3.9V	165		ns	
8	TdDSR(DR)	/DS Falling to Read	2.0V		260	ns	[1, 2]
		Data Required Valid	3.9V		260	ns	
9	ThDR(DS)	Read Data to	2.0V	0		ns	[2]
		/DS Rising Hold Time	3.9V	0		ns	
10	TdDS(A)	/DS Rising to Address	2.0V	85		ns	[2]
		Active Delay	3.9V	95		ns	
11	TdDS(AS)	/DS Rising to /AS	2.0V	60		ns	[2]
		Falling Delay	3.9V	70		ns	
12	TdR/W(AS)	R//W Valid to /AS	2.0V	70		ns	[2]
		Rising Delay	3.9V	70		ns	
13	TdDS(R/W)	/DS Rising to	2.0V	70		ns	[2]
		R//W Not Valid	3.9V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS	2.0V	80		ns	[2]
		Falling (Write) Delay	3.9V	80		ns	
15	TdDS(DW)	/DS Rising to Write	2.0V	70		ns	[2]
		Data Not Valid Delay	3.9V	80		ns	
16	TdA(DR)	Address Valid to Read	2.0V		475	ns	[1, 2]
		Data Required Valid	3.9V		475	ns	
17	TdAS(DS)	/AS Rising to	2.0V	100		ns	[2]
		/DS Falling Delay	3.9V	100		ns	
18	TdDM(AS)	/DM Valid to /AS	2.0V	55		ns	[2]
		Falling Delay	3.9V	55		ns	
19	TdDS(DM)	/DS Rise to	2.0V			ns	
		/DM Valid Delay	3.9V			ns	
20	ThDS(A)	/DS Rise to Address	2.0V			ns	
		Valid Hold Time	3.9V			ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] 2.0V to 3.9V

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram

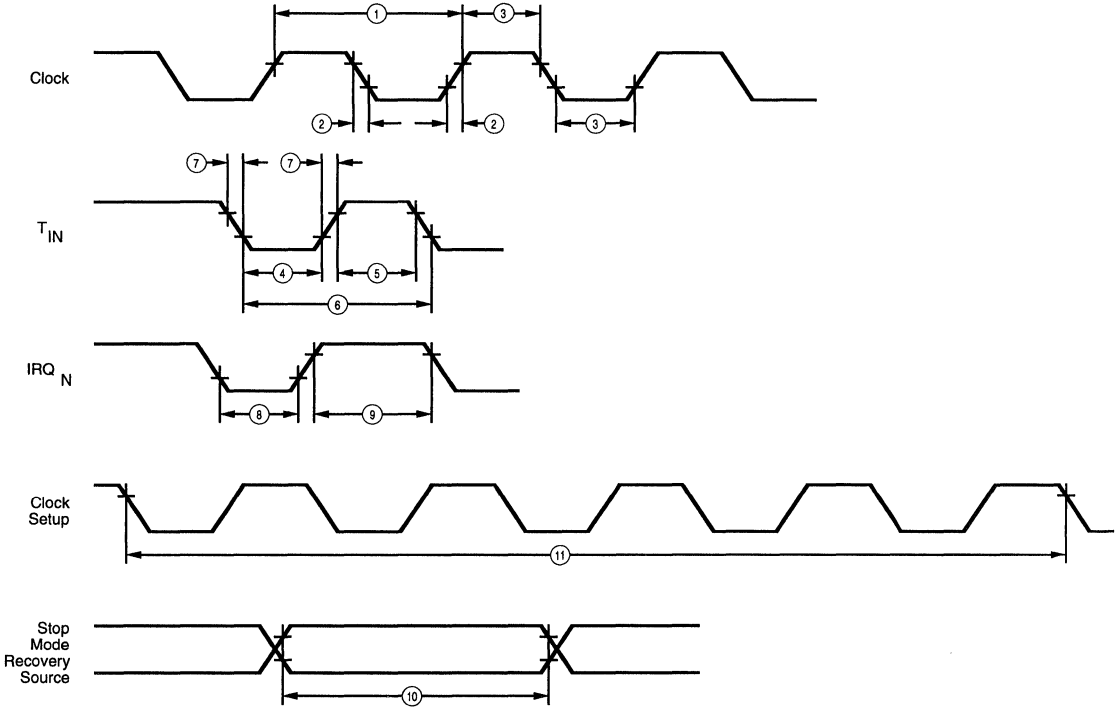


Figure 44. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +55°C 8.0 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	121	100000	ns	[1]
			3.9V	121	100000	ns	[1]
2	TrC,TfC	Clock Input Rise	2.0V		25	ns	[1]
		and Fall Times	3.9V		25	ns	[1]
3	TwC	Input Clock Width	2.0V	37		ns	[1]
			3.9V	37		ns	[1]
4	TwTinL	Timer Input	2.0V	100		ns	[1]
		Low Width	3.9V	70		ns	[1]
5	TwTinH	Timer Input	2.0V	3TpC			[1]
		High Width	3.9V	3TpC			[1]
6	TpTin	Timer Input Period	2.0V	8TpC			[1]
			3.9V	8TpC			[1]
7	TrTin,TfTin	Timer Input Rise	2.0V		100	ns	[1]
		and Fall Timers	3.9V		100	ns	[1]
8A	TwIL	Interrupt Request	2.0V	100		ns	[1, 2]
		Low Time	3.9V	70		ns	[1, 2]
8B	TwIL	Int. Request	2.0V	3TpC			[1, 3]
		Low Time	3.9V	3TpC			[1, 3]
9	TwIH	Interrupt Request	2.0V	3TpC			[1, 2]
		Input High Time	3.9V	3TpC			[1, 2]
10	Twsm	Stop-Mode Recovery	2.0V	12		ns	
		Width Spec	3.9V	12		ns	
			2.0V	5TpC			[7]
			3.9V	5TpC			[8]
11	Tost	Oscillator	2.0V		5TpC		[4]
		Startup Time	3.9V		5TpC		[4]
12	Twdt	Watch-Dog Timer	2.0V	10		ms	D0 = 0 [5]
		Delay Time	3.9V	5		ms	D1 = 0 [5]
			2.0V	30		ms	D0 = 1 [5]
			3.9V	15		ms	D1 = 0 [5]
			2.0V	50		ms	D0 = 0 [5]
			3.9V	25		ms	D1 = 1 [5]
			2.0V	200		ms	D0 = 1 [5]
			3.9V	100		ms	D1 = 1 [5]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0
[5] Reg. WDTMR
[6] 2.0V to 3.9V
[7] Reg. SMR – D5 = 0
[8] Reg. SMR – D5 = 1

AC CHARACTERISTICS

Handshake Timing Diagrams

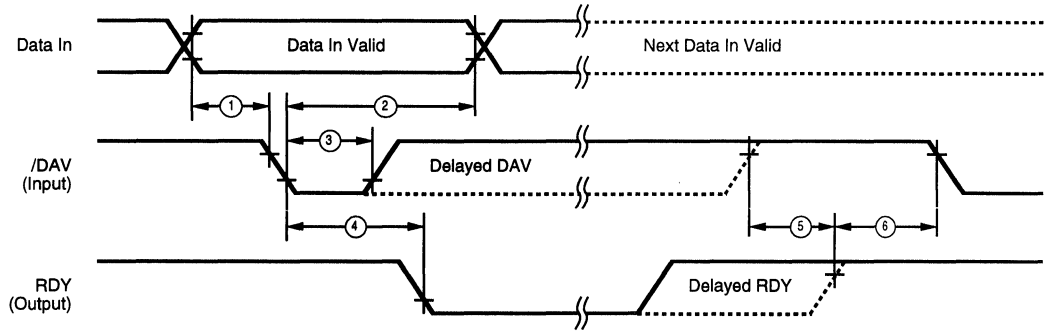


Figure 45. Input Handshake Timing

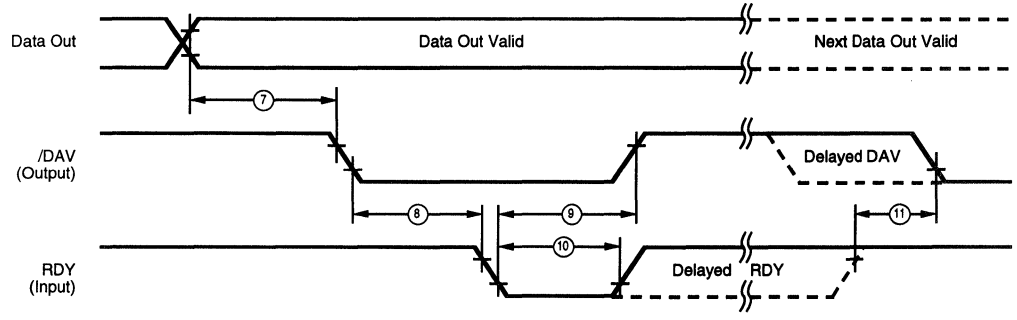


Figure 46. Output Handshake Timing

3

AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +55°C 8.0 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	160		IN
			3.9V	115		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	2.0V		160	IN
		Falling Delay	3.9V		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	2.0V		120	IN
		Falling Delay	3.9V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV	2.0V	0		IN
		Falling Delay	3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV	2.0V	63		OUT
		Falling Delay	3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY	2.0V	0		OUT
		Falling Delay	3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	2.0V		160	OUT
		Rising Delay	3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	2.0V		110	OUT
		Falling Delay	3.9V		80	OUT

Note:
[3] 2.0V to 3.9V

EXPANDED REGISTER FILE CONTROL REGISTERS (0D)

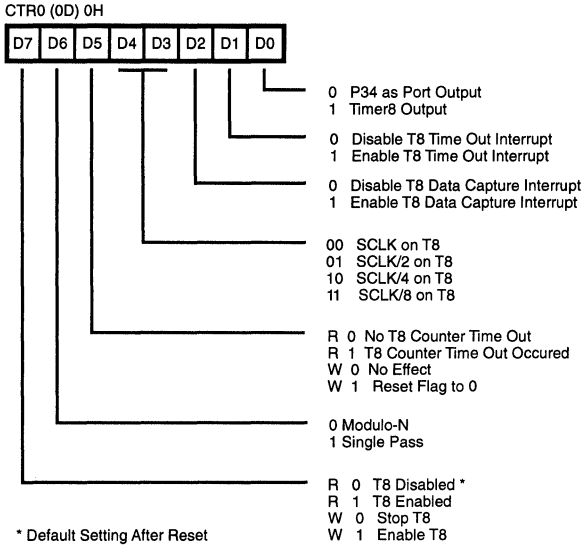
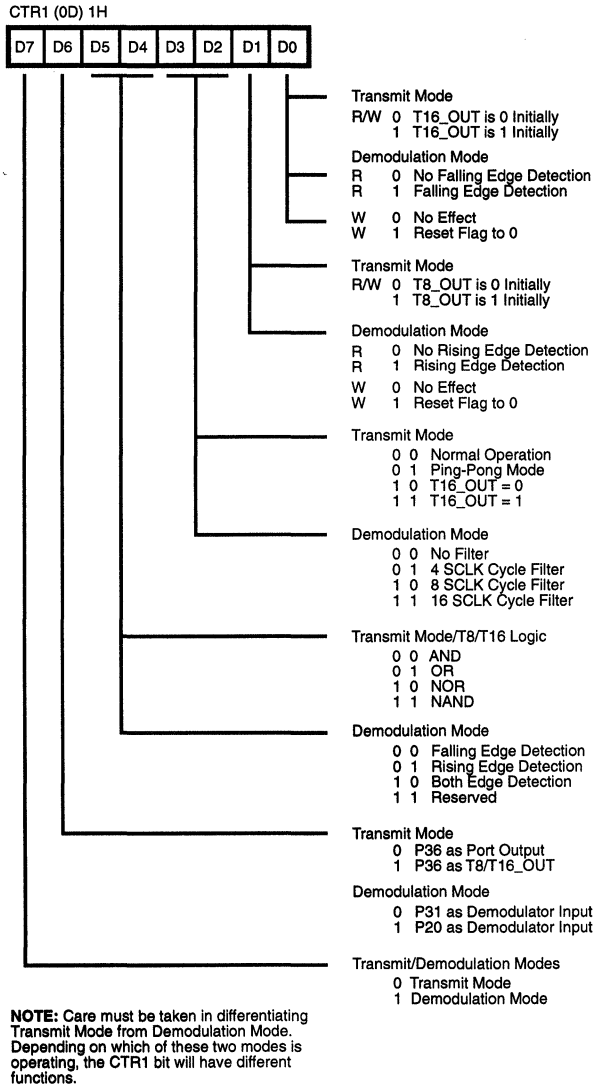


Figure 47. TC8 Control Register ((0D) 0H: Read/Write Accept Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0D) (Continued)



NOTE: Care must be taken in differentiating Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit will have different functions.

Figure 48. T8 and T16 Common Control Functions ((0D) 1H: Read/Write)

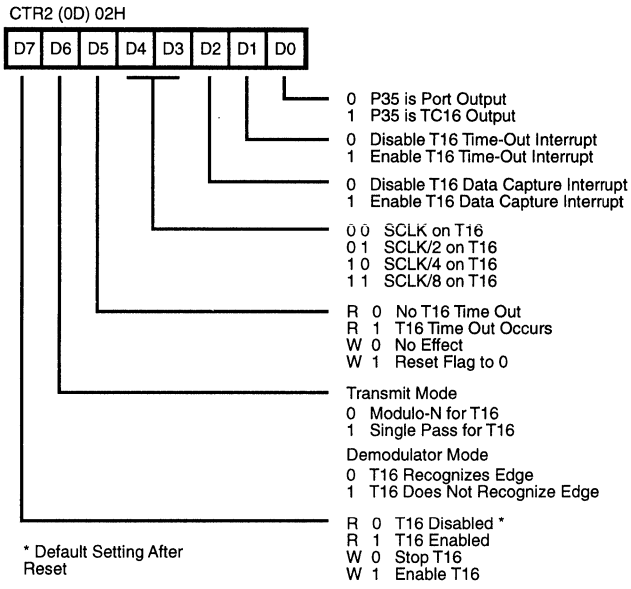
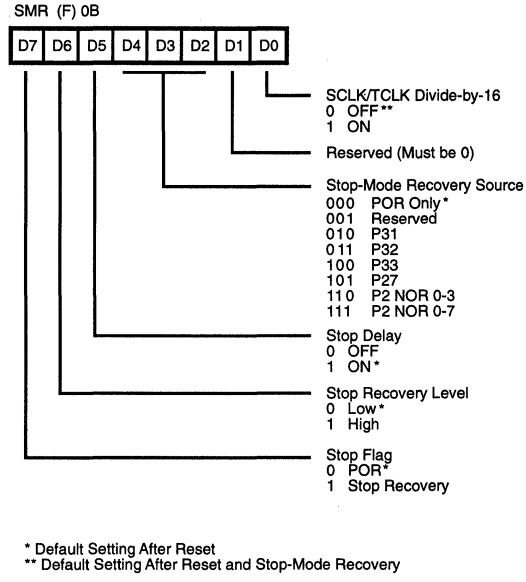


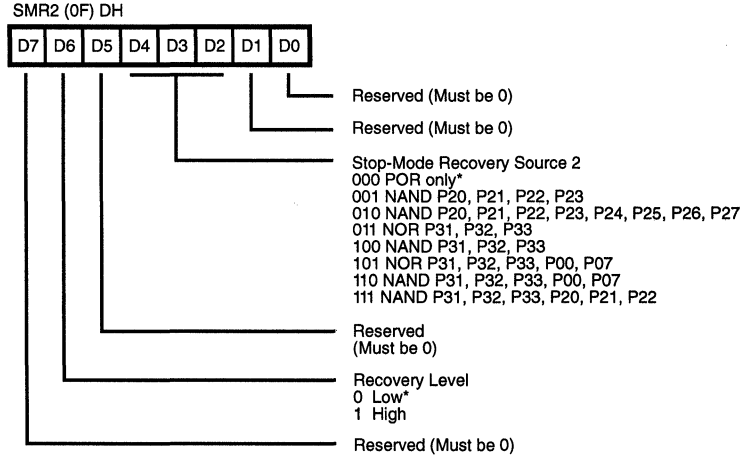
Figure 49. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0F)



* Default Setting After Reset
** Default Setting After Reset and Stop-Mode Recovery

Figure 50. Stop-Mode Recovery Register ((F)0BH: D6-D0 = Write Only, D7 = Read Only)



Note: If used in conjunction with SMR, either of the two specified events will cause a Stop-Mode Recovery.

*Default Setting After Reset

Figure 51. Stop-Mode Recovery Register 2 ((0F) DH: D2-DH, D6 Write Only)

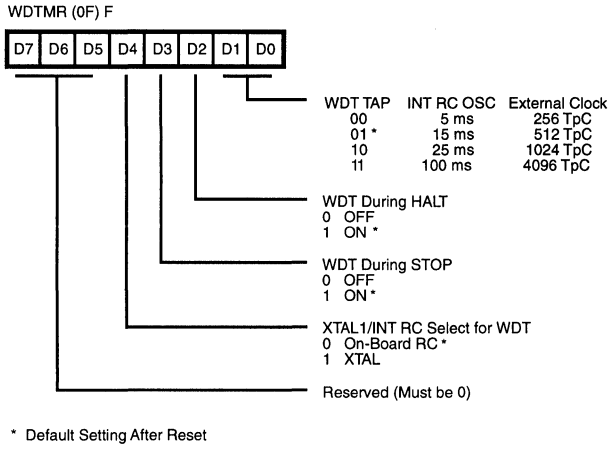


Figure 52. Watch-Dog Timer Mode Register ((F) 0FH: Write Only)

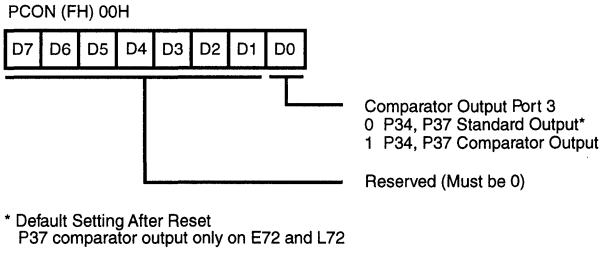
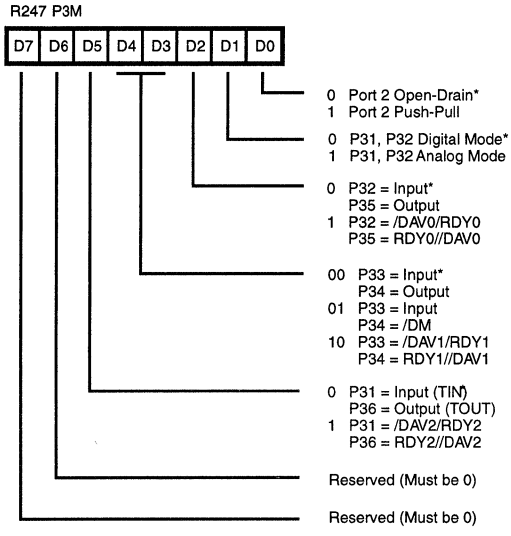


Figure 53. Port Configuration Register (PCON) ((0F) 0H: Write Only)

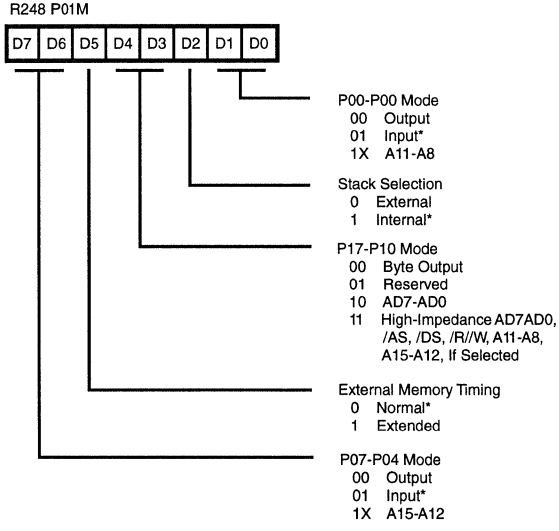
3

Z8 STANDARD CONTROL REGISTER DIAGRAMS



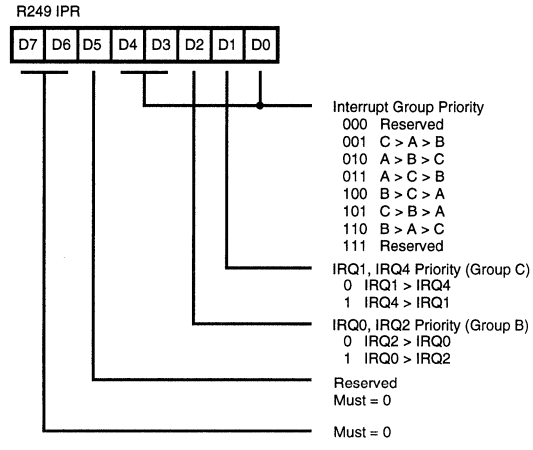
* Default Setting After Reset

Figure 54. Port 3 Mode Register (F7H:Write Only)



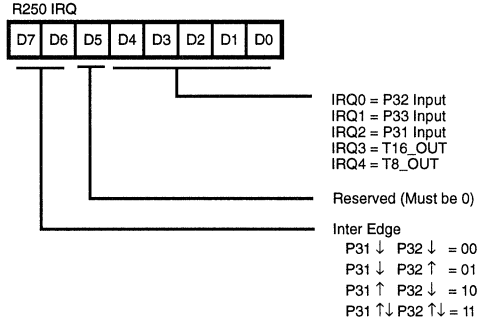
* Default Settingt After Reset.
Note: Only P00 and P07 are Available on Z86L71.

Figure 55. Port 0 and 1 Mode Register (F8H: Write Only)



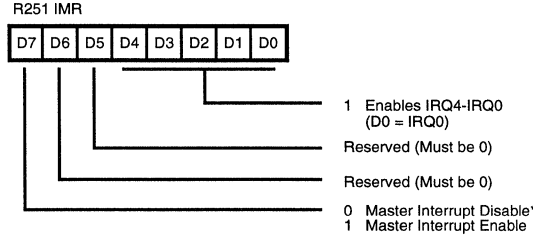
*Group A only has IRQ3 within it

Figure 56. Interrupt Priority Registers ((0)F9H:Write Only)



Default Setting After Reset = 0000 0000

Figure 57. Interrupt Request Register ((0)FAH:Read/Write)



* Default Setting After Reset

Figure 58. Interrupt Mask Register ((0)FBH:Read/Write)

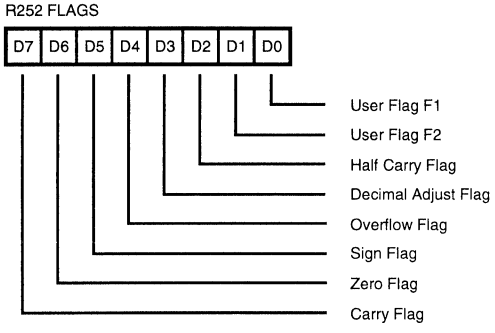


Figure 59. Flag Register ((0)FCH:Read/Write)

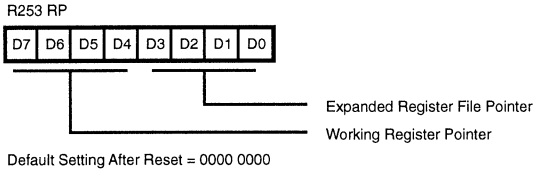


Figure 60. Register Pointer ((0)FDH:Read/Write)

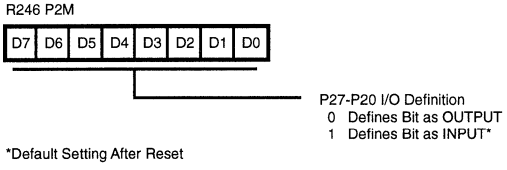


Figure 61. Port 2 Mode Register (F6H:Write Only)

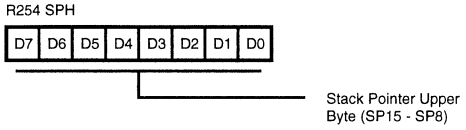


Figure 62. Stack Pointer High ((0)FEH:Read/Write)

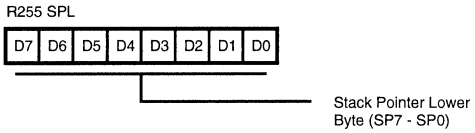


Figure 63. Stack Pointer Low ((0)FFH:Read/Write)

3

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

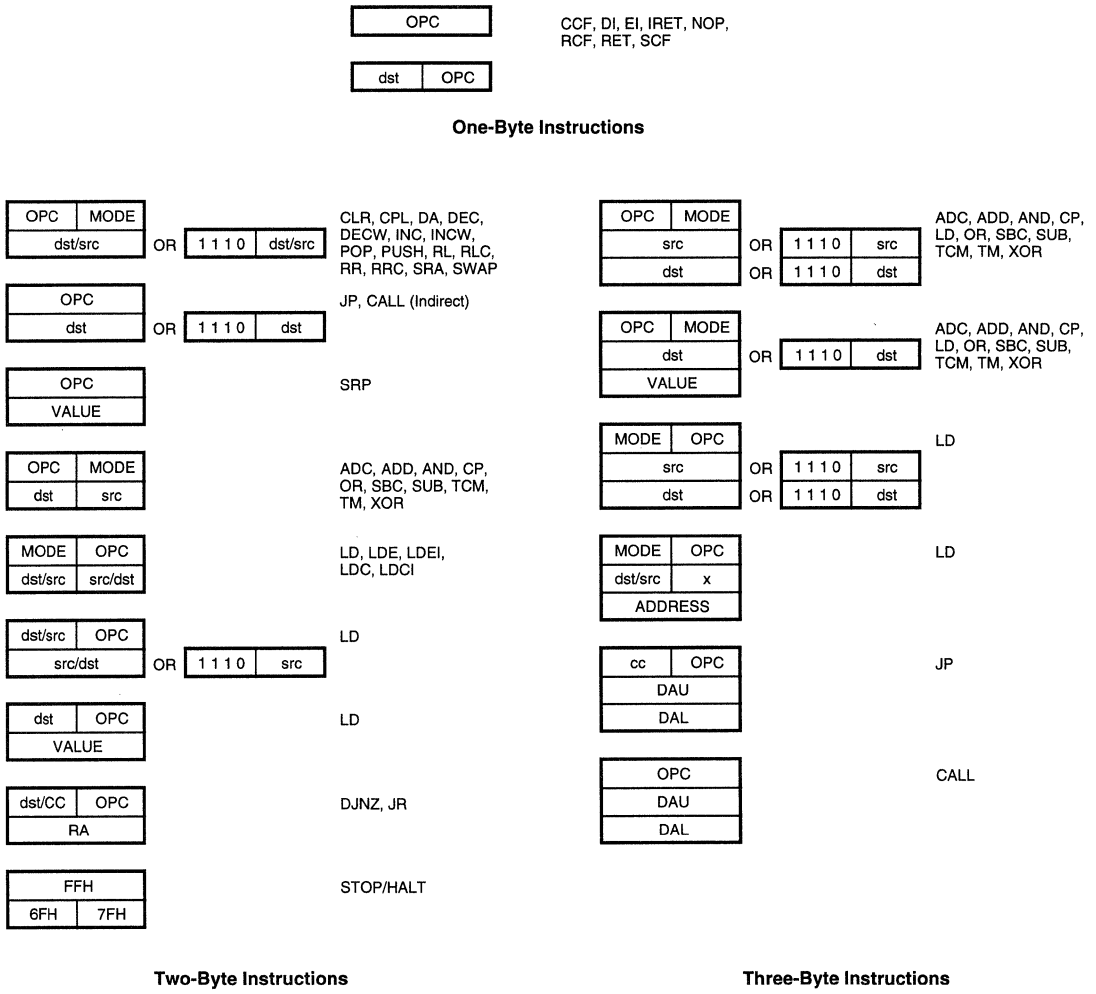
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

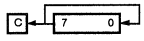
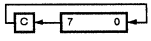
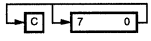
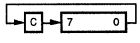
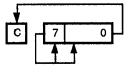
INSTRUCTION SUMMARY (Continued)

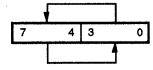
Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R IR IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r Irr	Irr r	C2 D2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir Irr	Irr Ir	C3 D3	-	-	-	-	-	-
LDE dst, src dst←src	r Irr	Irr Ir	82 92	-	-	-	-	-	-
LDEI dst, src dst←src r←r + 1;rr←rr + 1	Ir Irr	Irr Ir	83 93	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

3

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP − 1; @SP←src	R IR		70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im		31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

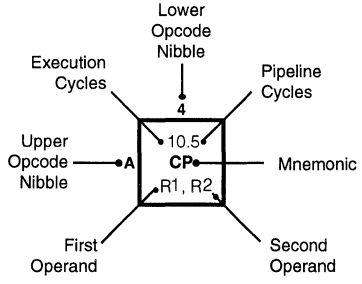
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



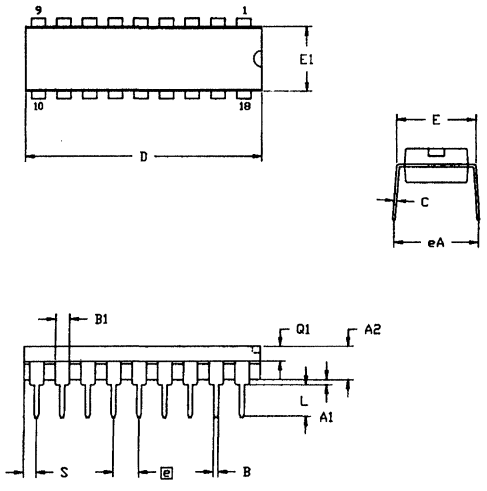
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

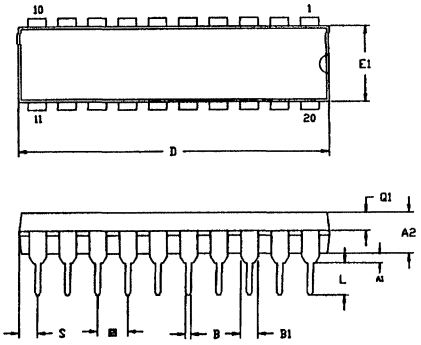
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

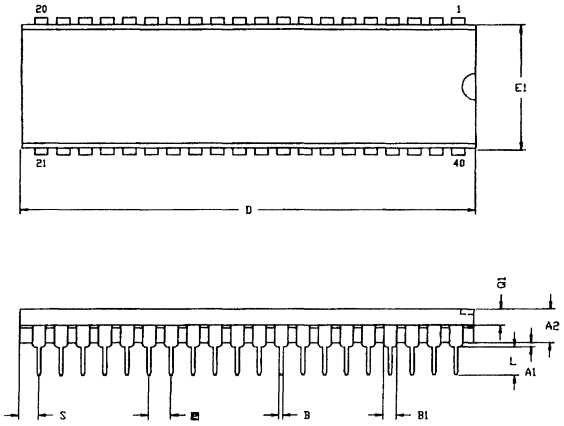
18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	-	.015	-
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

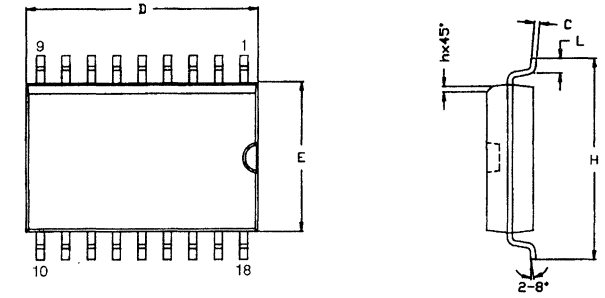
20-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram



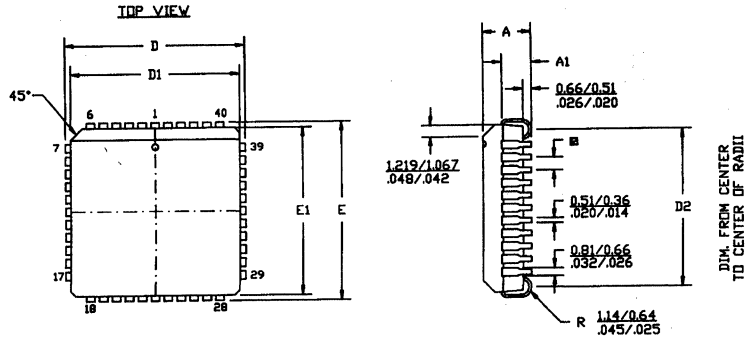
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

3

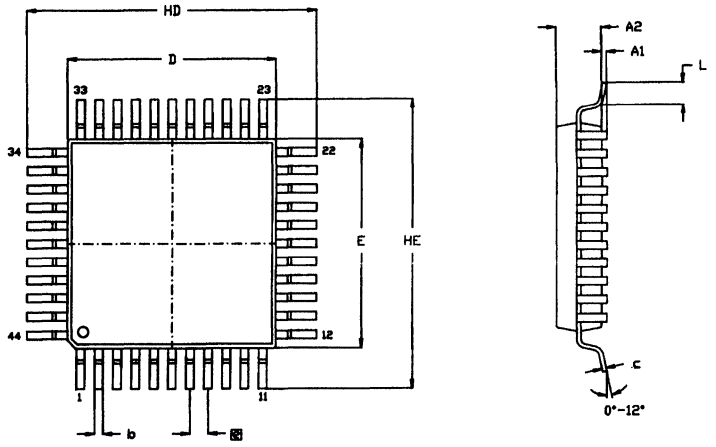
PACKAGE INFORMATION (Continued)



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10mm / .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86L70/71/72 and Z86E72

8.0 MHz

18-pin DIP	20-pin DIP	40-pin DIP
Z86L70PSC	Z86L71PSC	Z86L72PSC
		Z86E72PSC
18-pin SOIC	**44-pin PLCC**	**44-pin QFP**
Z86L70SSC	Z86L72VSC	Z86L72FSC
	Z86E72VSC	Z86E72FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

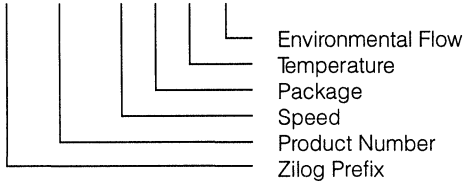
Package
P = Plastic DIP
F = Plastic Quad Flat Pack
V = Plastic Chip Carrier
S = Small Outline I.C.

Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speed
08 = 8.0 MHz

Environmental
C = Plastic Standard

Example:
Z 86L71 08 P S C is a Z86L70, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



BEYOND THE 3 VOLT LIMIT

Consumer applications designs have become more space and power conscious than ever before. Understanding the issues of long battery life and compact size — with no loss of functionality — is critical to the marketplace.

INTRODUCTION

Spurred on by the growing popularity of portable computing and the power-efficient operation these machines demand, microprocessors working down to 3V have become an ongoing area of interest in today's electronics industry. Unfortunately, reducing the operating voltage to a semiconductor such as a microprocessor limits its ability to operate at high speeds — the faster the computer, the better. Recently introduced IBM-compatible PCs at 5V operate at up to 66 MHz, while portables operating off batteries at 3V are barely able to achieve 20 to 25 MHz operation. Why? Blame the physics of a transistor: as the voltage drops, the gain of the transistors is reduced, directly affecting the speed with which it can operate. The lower the voltage, the slower things go. However, while high-speed low-voltage computers are unlikely, there is a whole host of electronic applications which demand speed, albeit not the blazing speeds of computers, making it feasible to move beyond the 3V limit.

BELOW 3V: WHERE AND WHY

Many electronic products in common use have frequency requirements far below those of portable computers in the 8 MHz and below range. The electronic watch on your wrist, infrared remote controls for televisions, VCRs and stereo systems; wireless motion and sound detectors in security systems; pagers; even the toys our children play with are all ideal examples of products requiring small size, long life, and low frequency operation. Together, these products make up a substantial part of the consumer electronics marketplace. Although many of these designs presently rely on devices operating in the 3V-5V range, they are ideal candidates for even lower voltage devices. This application note will address some of the issues involved in using microcontrollers operating in the 2V range, touch upon applications where this lower voltage approach is a good fit, and propose some solutions.

One case in point is the hand-held IR remote control. The demand from the end-user is to control more functions from an ever-smaller unit, preferably one in which the batteries need not be replaced frequently. Use of two AA or AAA cells is therefore ideal from the standpoint of size, cost and performance. Since these cells occupy less space than, for instance, three or four AAs, this opens up an opportunity for the designer to create a smaller form and fit in the packaging, or to incorporate additional features in the same form factor. In terms of battery life, operation at the 2V level also allows 80% of the two AA batteries' life-span to be used: a substantial increase compared to their life at 3V operation (see Figure 1). Additionally, as the voltage drops power consumption drops as well, thereby extending battery life even further.

The traditional tradeoff to obtain lower power consumption at lower voltages has been a reduction in performance (see Figure 2). Recent 2V introductions at Zilog, however, have incorporated special feature sets which provide optimal results at these lower voltages while maintaining the expected functionality. Two of which (see Figure 2), are special power-down modes. Should the processor not need to be fully functional at full speed, the user may choose one of the sleep modes and save a large amount of current consumption. The user need only calculate the amount of time spent while operating at full speed and asleep to calculate the overall battery life and then tradeoff the required frequency to pick the best power consumption.

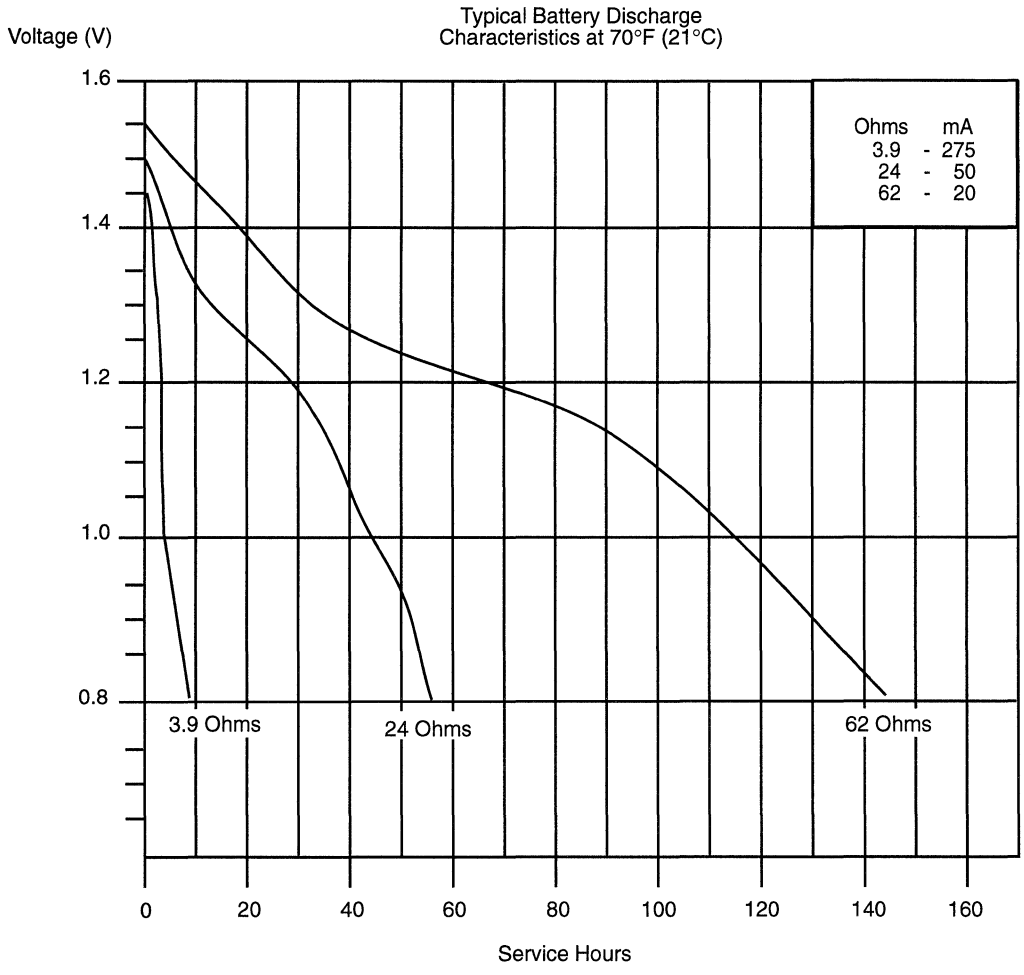


Figure 1. Typical Battery Discharge

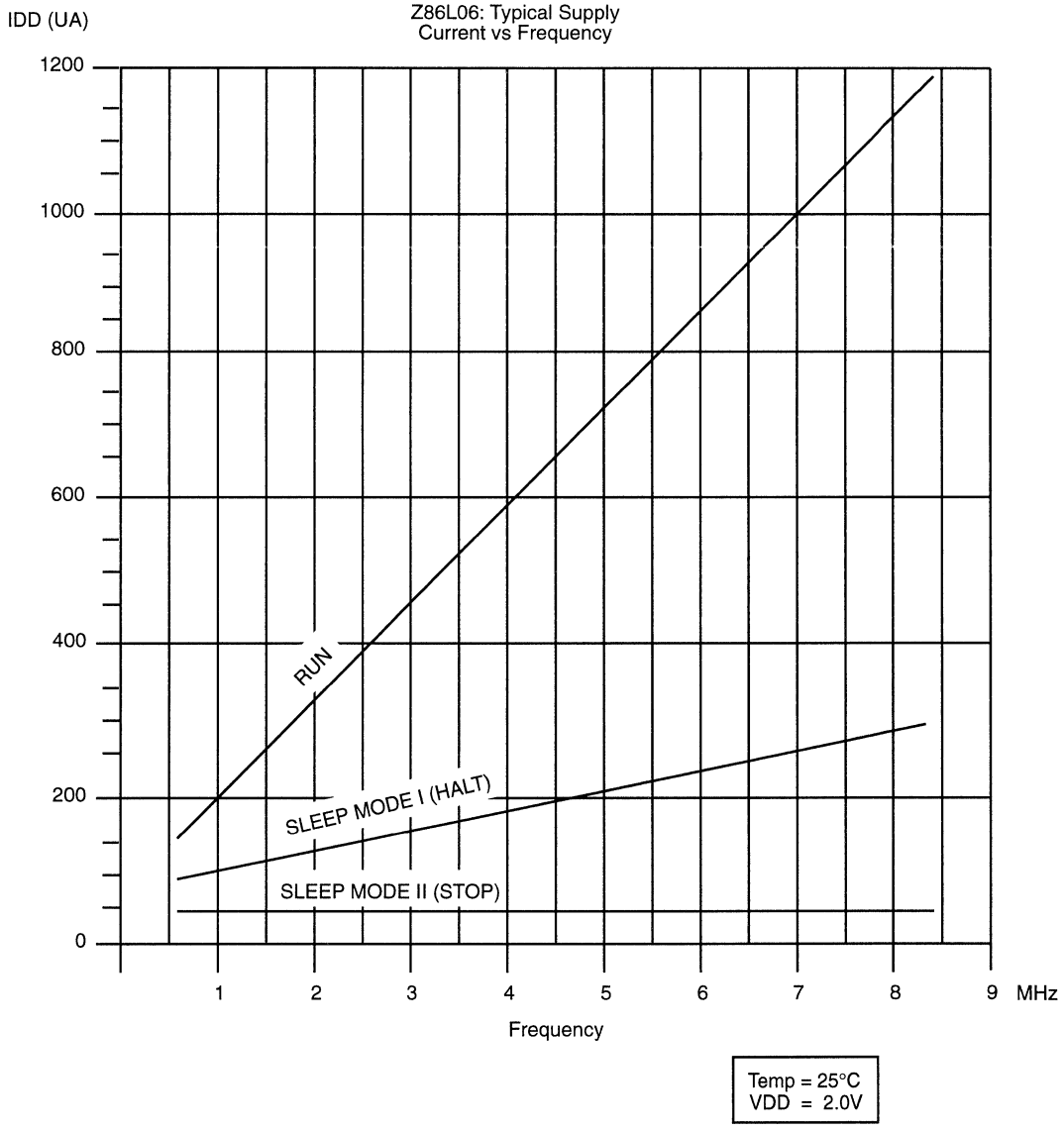


Figure 2. Typical Supply Current vs Frequency

4

PITFALLS AND SOLUTIONS

Semiconductors operating below 2V are not new, as can be witnessed by digital watches running at 1.5V, but they are very narrow in usage and very specific in function. The digital watch clock chip is useful for little else. General-purpose semiconductors such as processors and peripherals are nearly non-existent below 3V. This means that the 2V device used in hand-held electronics is forced to do all the required functions. CPU, RAM, ROM , and I/O functions all must reside within the microcontroller if the elimination of 5V peripherals is to be achieved.

High-frequency performance is a key issue. Lower frequencies, as we've seen, have usually accompanied low voltage parts. However, maintaining a 8 MHz frequency, which is more than sufficient for most battery operated, small-format products, is quite possible. Zilog's CMOS process has yielded two microcontrollers — Z86L06 and Z86L29 — which maintain 8 MHz functionality at 2V while maintaining highly efficient current consumption. For instance, the RUN current of the Z86L06 is very low: less than 1.2 mA at full speed. Only the 4 MHz operation is needed, therefore, only 600 mA is used. The two parts shown differ primarily in ROM size (1K ROM vs 6K ROM, respectively), and both have become popular choices for security and infrared remote applications.

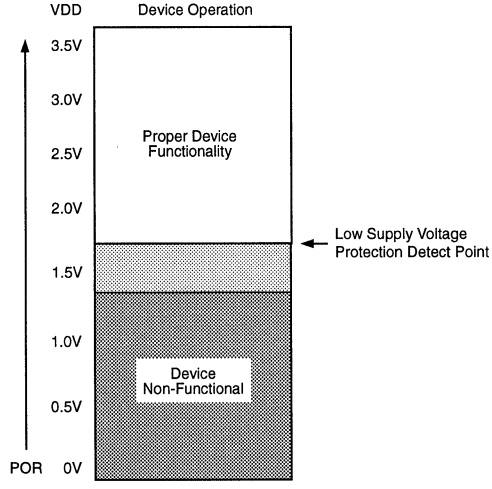


Figure 3. MCU Device Operation vs Supply Voltage

RE-INVENTING THE POWER-ON RESET (POR)

As batteries grow old, the resultant voltage they produce drops. Care must be taken to maintain safe, proper operation and avoid "brownouts" through low voltage protection techniques. Special analog circuitry with glitch filtering on-board Zilog's 2V microcontrollers detects low voltage conditions (i.e., below 2V) and holds the MCU microcontroller in a safe known reset state. Upon restoration of proper (2V or higher) voltage, the circuit will release and allow normal operation. This kind of excursion below 2V is common in battery-operated applications. For example, when you remove the batteries in an infrared remote, the unit is in a "sleep" condition, consuming almost no power. The residual charge from those batteries may be maintained within the system from minutes to hours, slowly discharging further and further below 2V. It is unlikely, when the batteries are actually replaced, that the discharge will drop sufficiently close to zero to activate the power-on circuitry. Low voltage protection, in such cases, serves much the same "reset" function (see Figure 4). Without this circuit, it is possible for any microcontroller to go into an unknown state of operation, and the power-on circuit, whether internal or external, will not work. This may preclude it from operating properly upon restoring the batteries. Unfortunately, this problem may not be found until years later when the unit's batteries finally need replacing. Only a special low voltage sense and protection circuit will do the job!

Many battery-operated applications require the absolute minimum of components — in many cases a 2V MCU may be the only IC in the system. This is one reason for Zilog's development of an on-board POR (Power-On Reset) circuit. No external circuit is required: simply apply power to the MCU and these devices will come up in normal operating condition. This circuit is very closely connected with the low voltage protection already described, so as to ensure safe operation in nearly all conditions.

Even these precautions, however, do not cover every loophole, so a Watch-Dog Timer (WDT) is an important component of these Zilog devices. This special timer is dedicated, separately from the other two counter/timers on-board, to watching over the software operation running on the MCU. It even operates from a separate on-board RC oscillator to ensure WDT functionality. If for any reason the software strays outside the bounds of normal operation, the WDT is there, and will timeout and reset the MCU.

Let's again take the infrared remote as an example. Suppose you press the volume button and hold it "on" for a few seconds. The IR remote begins sending this motion to your TV. However, in the middle of this process you accidentally knock the remote against a table. This — or, any of a number of interruptions such as a static discharge or voltage drop causes the MCU to jump into undefined code space and hang up in a do-nothing loop. The WDT continues to clock along. Since the MCU is not operating normally, it never reset the WDT prior to timeout (see Figure 3); therefore, a WDT timeout now occurs, resetting the MCU to normal operation which detects the volume button and sends the appropriate information. This process is completely undetectable to you: all you sense are the changes to the TV that you required.

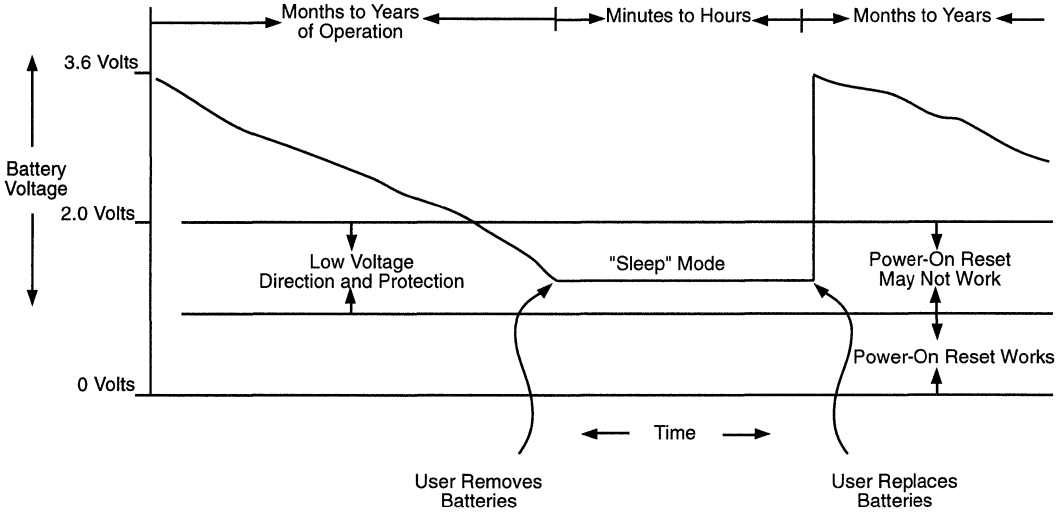


Figure 4. Low Voltage Detection and Protection

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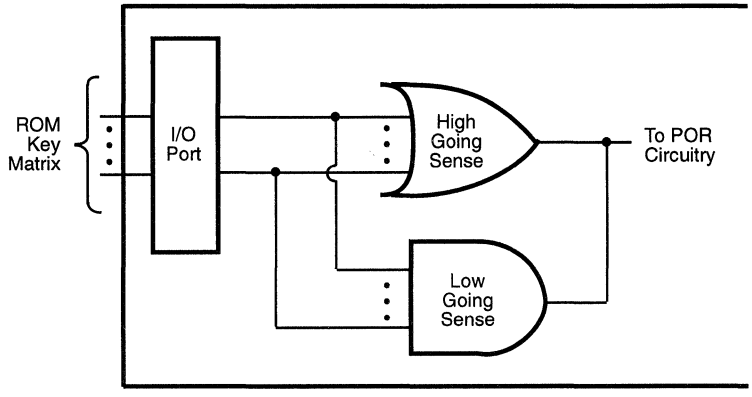
TO WORK OR NOT TO WORK

A final, crucial concern relates to battery life. Even a low voltage device, if continuously active, will create a significant power drain. Many products using such devices, however, do not require continuous operation. An IR remote need be active only when you press a key, for example; or a security motion detector may only actively scan the area at intervals which will give the perceived equivalent of continuous operation, but at the level of milliseconds or seconds. In these cases, the availability of a Sleep Mode (see Figure 2), which consumes very low power while holding the chip in a stand-by condition, makes possible significant improvements in total average power consumption. The Zilog microcontrollers incorporate special inputs which, upon a change in state, will automatically "wake" the device and allow it to perform its system functions (see Figure 5). For example, the infrared remote on your coffee table is "sleeping" until you pick it up and press the button. This sends a signal to Port 2 of the Zilog IC, which "wakes" it up in order to signal your TV to turn on. Thereafter, it returns to the "sleep" mode, saving your battery for months or even years of future operation.



Any high-going or low-going change on the I/O port triggers the on-board POR circuitry.

Figure 5. Wake Up Capability On-Board the IC

IT'S AN ANALOG WORLD

Ultimately, no matter how hard we try to avoid it, controller applications are forced to interface with the real world. This, in the hand-held battery operated electronic world, usually involves voltage sensing, analog to digital conversion, digital to analog conversion, or all the above. The combination of a PWM output through a voltage integrator and two on-board analog comparators (Figure 6) can be used for these purposes. At 2V operation, these comparators are limited but will be sufficient for simple voltage level sensing and A/D conversions. Optimaliy, a resistor and capacitor should be used as a voltage integrator. The MCU can generate a Pulse Width Modulated (PWM) signal into the voltage integrator, resulting in a voltage level which is submitted to the on-board comparators' reference inputs. When the external voltage being sensed reaches the reference voltage, an interrupt is generated to the MCU. Since the MCU knows that the associated PWM output signal equates to a given reference voltage, it recognizes the level just reached by the external voltage.

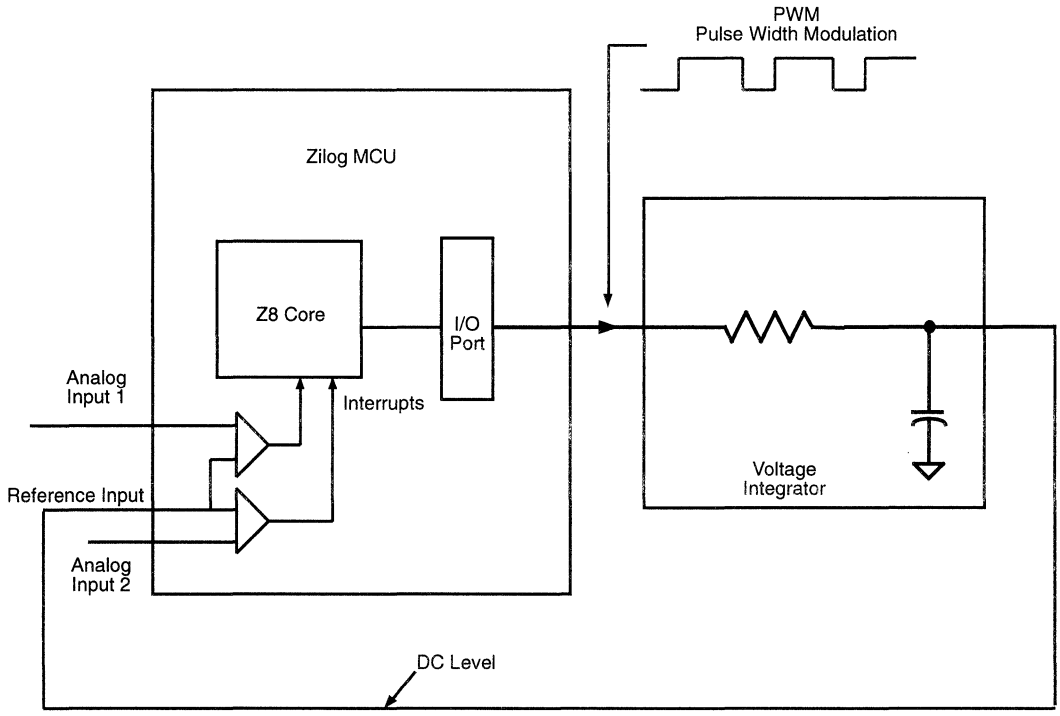


Figure 6. On-Board Comparators

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CONCLUSION

Advances like these, which make the performance of 2V parts comparable to (and, in some cases, better than) that of 3V or even 5V parts, makes them a viable alternative for many applications, and a key to future developments which will depend on low voltage/high-performance characteristics. The remote control unit of the future, for instance, will be designed for bi-directional communications and have the potential to access nearly any appliance or electronic device in the typical household. Spread spectrum technology has the potential to open up a much broader personal communications arena, where items like telephones and personal locator devices will eventually be linked in a wireless environment—low voltage microcontrollers will be a crucial component in these as well as many other hand-held electronics. And products currently in the development stage will incorporate features like automatic pulse generation and reception of infrared remote signals, special high-current outputs, and much more, all of which Zilog expects to address in the short term.

These recent advances in 2V CMOS processes, allowing 2V MCUs which maintain high frequency, 8 MHz operation, and integrated systems functions lay the groundwork for successive developments in low voltage applications. A variety of support capabilities and features are being created to ensure safe, reliable operation at 2V for consumer electronics applications requiring (as more and more of them do) the absolute minimum of external components. In the months to come you can expect to see more and more capabilities included in devices operating not just at 3V, but below. Stay tuned.

The traditional tradeoff to obtain lower power consumption at lower voltages has been a reduction in performance. Recent 2V introductions, however, have incorporated special feature sets which provide optimal results at these lower voltages while maintaining the expected functionality.

Z86L7X00ZEM
PRODUCT SPECIFICATION

SUPPORTED DEVICES: Z86L70, Z86L71, Z86L72, Z86E72

DESCRIPTION

The Z86L7X00ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The emulator provides emulation for Zilog's IR Controllers (ZIRC™) family. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware and/or software product.

Data entering and program debugging are performed by the monitor ROM and the Host Package which communicates through a RS-232C serial interface with a fixed 19200 baud rate. The user program can be downloaded directly from the host computer through the RS-232C connector and may then be executed using various debugging commands in the monitor. The ICEBOX can be connected to a serial port COM1 or COM2 of the host computer (IBM® 286, 386 or 486 compatible).

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed: 16 MHz

Power Requirements

+5 Vdc @ 1.5A

Dimensions

Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface

RS-232C @ 19200 baud

KIT CONTENTS

Z86L7X Emulator

Z8® Emulation Base Board

CMOS Z86C9120PSC
8K X 8 EPROM (Programmed with Debug Monitor)
EPM5128 EPLD
32K X 8 Static RAM
Three 64K X 4 Static RAM
RS-232C Interface
Reset Swtich

Z86L7X Emulation Daughter Board

Z86C5020GSE Z8 ICE Chip
Three EPM5128 EPLD
2K X 8 Static RAM
40-pin ZIF OTP Socket
80/40 Pin Target Connector
100-pin HP-16500 Interface Board Connector

Cables

12", 20-Pin DIP Emulation Cable
12", 40-Pin DIP Emulation Cable
15", Power Cable with Banana Plugs
60", DB 25 RS-232C Cable

Software (IBM®-PC Platform)

Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link Loader
GUI Host Package

Documentation

Z8® ICEBOX™ User's Manual
Z86L7X User's Manual Supplement
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User's Guide
Registration Card

ORDERING INFORMATION

Part No: Z86L71X00ZEM

LITERATURE GUIDE

Z8®/SUPER8™ MICROCONTROLLER FAMILY

Databooks	Part No	Unit Cost
Z8 Microcontrollers Databook (includes the following documents)	**DC-8275-04**	**5.00**

Z8 CMOS Microcontrollers

Z86C00/C10/C20 MCU OTP Product Specification
Z86C06 Z8 CCP™ Preliminary Product Specification
Z86C08 8-Bit MCU Product Specification
Z86E08 Z8 OTP MCU Product Specification
Z86C09/19 Z8 CCP Product Specification
Z86E19 Z8 OTP MCU Advance Information Specification
Z86C11 Z8 MCU Product Specification
Z86C12 Z8 ICE Product Specification
Z86C21 Z8 MCU Product Specification
Z86E21/Z86E22 OTP Product Specification
Z86C30 Z8 CCP Product Specification
Z86E30 Z8 OTP CCP Product Specification
Z86C40 Z8 CCP Product Specification
Z86E40 Z8 OTP CCP Product Specification
Z86C27/97 Z8 DTC™ Product Specification
Z86127 Low-Cost Digital Television Controller Adv. Info. Spec.
Z86C50 Z8 CCP ICE Advance Information Specification
Z86C61 Z8 MCU Advance Information Specification
Z86C62 Z8 MCU Advance Information Specification
Z86C89/C90 CMOS Z8 CCP Product Specification
Z86C91 Z8 ROMless MCU Product Specification
Z86C93 Z8 ROMless MCU Preliminary Product Specification
Z86C94 Z8 ROMless MCU Product Specification
Z86C96 Z8 ROMless MCU Advance Information Specification
Z88C00 CMOS Super8 MCU Advance Information Specification

Z8 NMOS Microcontrollers

Z8600 Z8 MCU Product Specification
Z8601/03/11/13 Z8 MCU Product Specification
Z8602 8-Bit Keyboard Controller Preliminary Product Spec.
Z8604 8-Bit MCU Product Specification
Z8612 Z8 ICE Product Specification
Z8671 Z8 MCU With BASIC/Debug Interpreter Product Spec.
Z8681/82 Z8 MCU ROMless Product Specification
Z8691 Z8 MCU ROMless Product Specification
Z8800/01/20/22 Super8 ROMless/ROM Product Specification

Peripheral Products

Z86128 Closed-Captioned Controller Adv. Info. Specification
Z765A Floppy Disk Controller Product Specification
Z5380 SCSI Product Specification
Z53C80 SCSI Advance Information Specification

Z8 Application Notes and Technical Articles

Zilog Family On-Chip Oscillator Design
Z86E21 Z8 Low Cost Thermal Printer
Z8 Applications for I/O Port Expansions
Z86C09/19 Low Cost Z8 MCU Emulator
Z8602 Controls A 101/102 PC/Keyboard
The Z8 MCU Dual Analog Comparator
The Z8 MCU In Telephone Answering Systems
Z8 Subroutine Library
A Comparison of MCU Units
Z86xx Interrupt Request Registers
Z8 Family Framing
A Programmer's Guide to the Z8 MCU
Memory Space and Register Organization

Super8 Application Notes and Technical Articles

Getting Started with the Zilog Super8
Polled Async Serial Operations with the Super8
Using the Super8 Interrupt Driven Communications
Using the Super8 Serial Port with DMA
Generating Sine Waves with Super8
Generating DTMF Tones with Super8
A Simple Serial Parallel Converter Using the Super8

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Zilog Quality and Reliability Report
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L

Z8®/SUPER8™ MICROCONTROLLER FAMILY (Continued)

Databooks	Part No	Unit Cost
Digital Signal Processor Databook (includes the following documents) Z89C00 16-Bit Digital Signal Processor Preliminary Product Specification Z89C00 DSP Application Note "Understanding Q15 Two's Complement Fractional Multiplication" Z89120, Z89920 (ROMless) 16-Bit Mixed Signal Processor Preliminary Product Specification Z89121, Z89921 (ROMless) 16-Bit Mixed Signal Processor Preliminary Product Specification Z89320 16-Bit Digital Signal Processor Preliminary Product Specification Z89321 16-Bit Digital Signal Processor Advance Information Specification	DC-8299-01	3.00
Telephone Answering Device Databook (includes the following documents) Z89C65, Z89C66 (ROMless) Dual Processor T.A.M. Controller Preliminary Product Specification Z89C67, Z89C68 (ROMless) Dual Processor Tapeless T.A.M. Controller Preliminary Product Specification	DC-8300-01	3.00
Infrared Remote (IR) Control Databook (includes the following documents) Z86L06 Low Voltage CMOS Consumer Controller Processor Preliminary Product Specification Z86L29 6K Infrared (IR) Remote (ZIRC™) Controller Advance Information Specification Z86L70/L71/L72, Z86E72 Zilog IR (ZIRC™) CCP™ Controller Family Preliminary Product Specification	DC-8301-01	3.00

Z8 Product Specifications, Technical Manuals and Users Guides	Part No	Unit Cost
Z86E23 CMOS Z8 OTP Microcontroller Preliminary Product Specification	DC-2598-00	N/C
Z86C27/97 Z8 DTC™ Product Specification and Addendum	DC-2561-01	N/C
Z86127 Low-Cost Digital Television Controller Preliminary Product Specification	DC-2574-00	N/C
Z86227 40-Pin Low-Cost Digital Television Controller Preliminary Product Specification and Addendum	DC-3002-00	N/C
Z86C61/62/96 CMOS Z8 Microcontroller Preliminary Product Specification	DC-2587-00	N/C
Z86C93 CMOS Z8 ROMless Microcontroller Product Specification	DC-2508-03	N/C
Z88C00 CMOS Super8 ROMless Microcontroller Preliminary Product Specification	DC-2551-00	N/C
Z8614 NMOS Z8 8-Bit MCU Keyboard Controller Preliminary Product Specification	DC-2576-00	N/C
Z86128 Closed-Captioned Controller Preliminary Product Specification and Addendum	DC-2570-01	N/C
Z86017 PCMCIA Adaptor Chip Advance Information Specification	DC-2643-0A	N/C
Z8 OTP CMOS One-Time-Programmable Microcontrollers Addendum	DC-2614-AA	N/C
asm S8 Super8/Z8 Cross Assembler User's Guide	DC-8267-05	3.00
Z8 Microcontrollers Technical Manual	DC-8291-02	5.00
Z86018 Preliminary User's Manual	DC-8296-00	N/C
Digital TV Controller User's Manual	DC-8284-01	3.00
Z89C00 16-Bit Digital Signal Processor User's Manual	DC-8294-01	3.00

Z8 Application Notes	Part No	Unit Cost
Z8602 Controls A 101/102 PC/Keyboard	DC-2601-01	N/C
The Z8 MCU Dual Analog Comparator	DC-2516-01	N/C
Z8 Applications for I/O Port Expansions	DC-2539-01	N/C
Z86E21 Z8 Low Cost Thermal Printer	DC-2541-01	N/C
Zilog Family On-Chip Oscillator Design	DC-2496-01	N/C
Using the Zilog Z86C06 SPI Bus	DC-2584-01	N/C
Interfacing LCDs to the Z8	DC-2592-01	N/C
X-10 Compatible Infrared (IR) Remote Control	DC-2591-01	N/C
Z86C17 In-Mouse Applications	DC-3001-01	N/C
Z86C40/E40 MCU Applications Evaluation Board	DC-2604-01	N/C
Z86C08/C17 Controls A Scrolling LED Message Display	DC-2605-01	N/C
Z86C95 Hard Disk Controller Flash EPROM Interface	DC-2639-01	N/C
Timekeeping with Z8; DTMF Tone Generation; Serial Communication Using the CCP Software UART	DC-2645-01	N/C

Z80®/Z8000® CLASSIC FAMILY OF PRODUCTS

Z80®/Z180™/Z280®/Z8000® and Datacom Family	Part No	Unit Cost
Volume I Databook	**DC-2610-01**	**5.00**

Microprocessors and Peripherals

Discrete Z80® Family

Z8400/C00 NMOS/CMOS Z80® CPU Product Specification
Z8410/C10 NMOS/CMOS Z80 DMA Product Specification
Z8420/C20 NMOS/CMOS Z80 PIO Product Specification
Z8430/C30 NMOS/CMOS Z80 CTC Product Specification
Z8440/Z84C40 NMOS/CMOS Z80 SIO Product Specification

Embedded Controllers

Z84C01 Z80 CPU with CGC Product Specification
Z84C50 RAM80™ Preliminary Product Specification
Z8470 Z80 DART Product Specification
Z84C90 CMOS Z80 KIO™ Product Specification
Z84011/C11 PIO Parallel I/O Product Specification
Z84013/015 Z84C13/C15 IPC/EIPC™ Product Specification
Z80180/Z8S180 Z180 MPU Product Specification
Z80181 ZIO™ Controller Product Specification
Z280™ MPU Preliminary Product Specification

Serial Communications Controllers

Z8030/Z8530 Z-BUS® SCC Product Specification
Z80C30/Z85C30 SCC Product Specification
Z85230 ESCC™ Product Specification
Z80230 Z-BUS ESCC Product Specification
Z16C35 ISCC™ Product Specification
Z5380 SCSI Product Specification
Z53C80 SCSI Product Specification
Z85C80 SCSI/SCC Product Specification
Z16C30 USC™ Product Specification
Z16C32 IUSC™ Product Specification
Z16C33 MUSC™ Product Specification
Z16C50 DDPLL™ Product Specification

Technical Articles

Z80 Questions and Answers
Z180 Questions and Answers
SCC Questions and Answers
ESCC Questions and Answers
ISCC Questions and Answers

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Superintegration Products Guide
Support Product Summary
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Z80®/Z180™/Z280®/Z8000® and Datacom Family	Part No	Unit Cost
Volume II Databook	**DC-2622-01**	**5.00**

Microprocessors and Peripherals

Application Notes

Z80® Family Interrupt Structure
Using the Z80® SIO with SDLC
Using the Z80® SIO In Asynchronous Communications
Binary Synchronous Communication Using the Z80® SIO
Serial Communication with the Z80A DART
Interfacing 8500 Peripherals to the Z80®
Serial Clock Generation Using the Z8536 CIO
Timing in an Interrupt-Based System with the Z80® CTC
A Z80-Based System Using the DMA with the SIO
Interfacing the Z8500 Peripherals to the 68000
Z180™ Break Detection
The Z180™ Interfaced with the SCC at 10 MHz
Technical Considerations When Implementing LocalTalk Link Access Protocol
Using the Z84C11/C13/C15 in Place of the Z84011/013/015
Using SCC with Z8000 in SDLC Protocol
SCC in Binary Synchronous Communications
On-Chip Oscillator Design
Interfacing Z80® CPUs to the Z8500 Peripheral Family
Boost Your System Performance Using The Zilog ESCC™
Design a Serial Board to Handle Multiple Protocols
Using the Z16C30 USC Universal Serial Controller
Datacommunications IUSC/MUSC Time Slot Assigner
Integrating Serial Data and SCSI Peripheral Control on One Chip
A Fast Z80® Embedded Controller
Using the Zilog Datacom Family with the 80186 CPU

Questions and Answers

Z80® Questions and Answers
Z180™ Questions and Answers
SCC Questions and Answers
ESCC Questions and Answers
ISCC Questions and Answers

Additional Information

Classic Family
Datacom Products
Literature Guide

Z80/Z180/Z280 Product Specifications, Technical Manuals and Users Guides	Part No	Unit Cost
Z80 CPU Central Processing Unit Technical Manual	DC-0029-05	3.00
Z80 Family Programmer's Reference Guide	DC-0012-04	3.00
Z80 DMA Direct Memory Access Technical Manual	DC-2013-A0	3.00
Z80 PIO Parallel Input/Output Technical Manual	DC-0008-03	3.00
Z80 CTC Counter/Timer Circuit Technical Manual	DC-0036-03	3.00
Z80 SIO Serial I/O Technical Manual	DC-3033-01	3.00
Z80180 Z180 MPU Microprocessor Unit Technical Manual	DC-8276-04	3.00
Z280 MPU Microprocessor Unit Technical Manual	DC-8224-03	3.00
Z80180/Z8S180 Z180 Microprocessor Product Specification	DC-2609-03	N/C
Z80182 Zilog Intelligent Peripheral (ZIP™)	DC-2616-03	N/C
Z380 Preliminary Product Specification	DC-3003-02	N/C

Z80/Z180/Z280 Application Notes	Part No	Unit Cost
Z180/SCC™ Serial Communications Controller Interface at 10 MHz	DC-2521-02	N/C
Z80 Using the 84C11/C13/C15 in place of the 84011/013/015	DC-2499-02	N/C
A Fast Z80 Embedded Controller	DC-2578-01	N/C

Z8000® MICROPROCESSOR FAMILY

Z8000 Product Specifications, Technical Manuals and Users Guides	Part No	Unit Cost
Z8000 CPU Central Processing Unit Technical Manual	DC-2010-06	3.00
SCC Serial Communication Controller User's Manual	DC-8293-02	3.00
Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel Input/Output Technical Manual	DC-2091-02	3.00
Z8038 Z8000 Z-FIO FIFO Input/Output Interface Technical Manual	DC-2051-01	3.00
Z8000 CPU Central Processing Unit Programmer's Pocket Guide	DC-0122-03	3.00
Z85233 EMSCC Enhanced Mono Serial Communication Controller Preliminary Product Specification	DC-2590-00	N/C
Z85C80 SCSCI™ Serial Communication and Small Computer Interface Preliminary Product Specification	DC-2534-02	N/C
Z16C30 USC Universal Serial Controller Preliminary Technical Manual	DC-8280-02	3.00
Z16C33 CMOS USC/MUSC™ Universal Serial Controller Technical Manual	DC-8285-02	3.00
Z16C32 IUSC™ Integrated Universal Serial Controller Product Specification	DC-2600-00	N/C
Z16C32 IUSC Integrated Universal Serial Controller Product Specification Addendum	DC-2600-00A	N/C
Z16C32 IUSC Integrated Universal Serial Controller Technical Manual	DC-8292-03	3.00
Z16C35 ISCC Integrated Serial Communication Controller Technical Manual	DC-8286-01	3.00
Z16C35 ISCC Integrated Serial Communication Controller Addendum	DC-8286-01A	N/C
Z53C80 Small Computer System Interface (SCSI) Product Specification	DC-2575-01	N/C
Z80230 Z-BUS® ESCC Enhanced Serial Communication Controller Preliminary Product Specification	DC-2603-01	N/C

Z8000 Application Notes	Part No	Unit Cost
Z16C30 Using the USC in Military Applications	DC-2536-01	N/C
Datacom IUSC/MUSC Time Slot Assigner	DC-2497-02	N/C
Datacom Evaluation Board Using The Zilog Family With The 80186 CPU	DC-2560-03	N/C
Boost Your System Performance Using the Zilog ESCC Controller	DC-2555-02	N/C
Z16C30 USC - Design a Serial Board for Multiple Protocols	DC-2554-01	N/C
Using a SCSI Port for Generalized I/O	DC-2608-01	N/C

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Military Specifications	Part No	Unit Cost
Z8681 ROMless Microcomputer Military Product Specification	DC-2392-02	N/C
Z8001/8002 Military Z8000 CPU Central Processing Unit Military Product Specification	DC-2342-03	N/C
Z8581 Military CGC Clock Generator and Controller Military Product Specification	DC-2346-01	N/C
Z8030 Military Z8000 Z-SCC Serial Communications Controller Military Product Specification	DC-2388-02	N/C
Z8530 Military SCC Serial Communications Controller Military Product Specification	DC-2397-02	N/C
Z8036 Military Z8000 Z-CIO Counter/Timer Controller and Parallel I/O Military Electrical Specification	DC-2389-01	N/C
Z8038/8538 Military FIO FIFO Input/Output Interface Unit Military Product Specification	DC-2463-02	N/C
Z8536 Military CIO Counter/Timer Controller and Parallel I/O Military Electrical Specification	DC-2396-01	N/C
Z8400 Military Z80 CPU Central Processing Unit Military Electrical Specification	DC-2351-02	N/C
Z8420 Military PIO Parallel Input/Output Controller Military Product Specification	DC-2384-02	N/C
Z8430 Military CTC Counter/Timer Circuit Military Electrical Specification	DC-2385-01	N/C
Z8440/1/2/4 Z80 SIO Serial Input/Output Controller Military Product Specification	DC-2386-02	N/C
Z80C30/85C30 Military CMOS SCC Serial Communications Controller Military Product Specification	DC-2478-02	N/C
Z84C00 CMOS Z80 CPU Central Processing Unit Military Product Specification	DC-2441-02	N/C
Z84C20 CMOS Z80 PIO Parallel Input/Output Military Product Specification	DC-2384-02	N/C
Z84C30 CMOS Z80 CTC Counter/Timer Circuit Military Product Specification	DC-2481-01	N/C
Z84C40/1/2/4 CMOS Z80 SIO Serial Input/Output Military Product Specification	DC-2482-01	N/C
Z16C30 CMOS USC Universal Serial Controller Military Preliminary Product Specification	DC-2531-01	N/C
Z80180 Z180 MPU Microprocessor Unit Military Product Specification	DC-2538-01	N/C
Z84C90 CMOS KIO Serial/Parallel/Counter Timer Preliminary Military Product Specification	DC-2502-00	N/C
Z85230 ESCC Enhanced Serial Communication Controller Military Product Specification	DC-2595-00	N/C

GENERAL LITERATURE

Catalogs, Handbooks and Users Guides	Part No	Unit Cost
Superintegration Shortform Catalog 1992	DC-5472-11	N/C
Superintegration Products Guide	DC-5499-07	N/C
ZIA™ 3.3-5.5V Matched Chip Set for AT Hard Disk Drives Datasheet	DC-5556-01	N/C
ZIA ZIA00ZCO Disk Drive Development Kit Datasheet	DC-5593-01	N/C
Zilog Hard Disk Controllers - Z86C93/C95 Datasheet	DC-5560-01	N/C
Zilog Infrared (IR) Controllers - ZIRC™ Datasheet	DC-5558-01	N/C
Zilog Intelligent Peripheral Controller - ZIP™ Z80182 Datasheet	DC-5525-01	N/C
Zilog Digital Signal Processing - Z89320 Datasheet	DC-5547-01	N/C
Zilog Datacommunications Brochure	DC-5519-00	N/C
Zilog Digital Signal Processing Brochure	DC-5536-02	N/C
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Zilog Television/Video Controllers Datasheet	DC-5567-01	N/C
Zilog TAD Controllers - Z89C65/C67/C69 Datasheet	DC-5561-01	N/C
Quality and Reliability Report	DC-2475-11	N/C
The Handling and Storage of Surface Mount Devices User's Guide	DC-5500-02	N/C
Universal Object File Utilities User's Guide	DC-8236-04	3.00
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Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056

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Zilog, Inc.
210 East Hacienda Ave.
Campbell, CA 95008-6600
408-370-8000
FAX 408-370-8056