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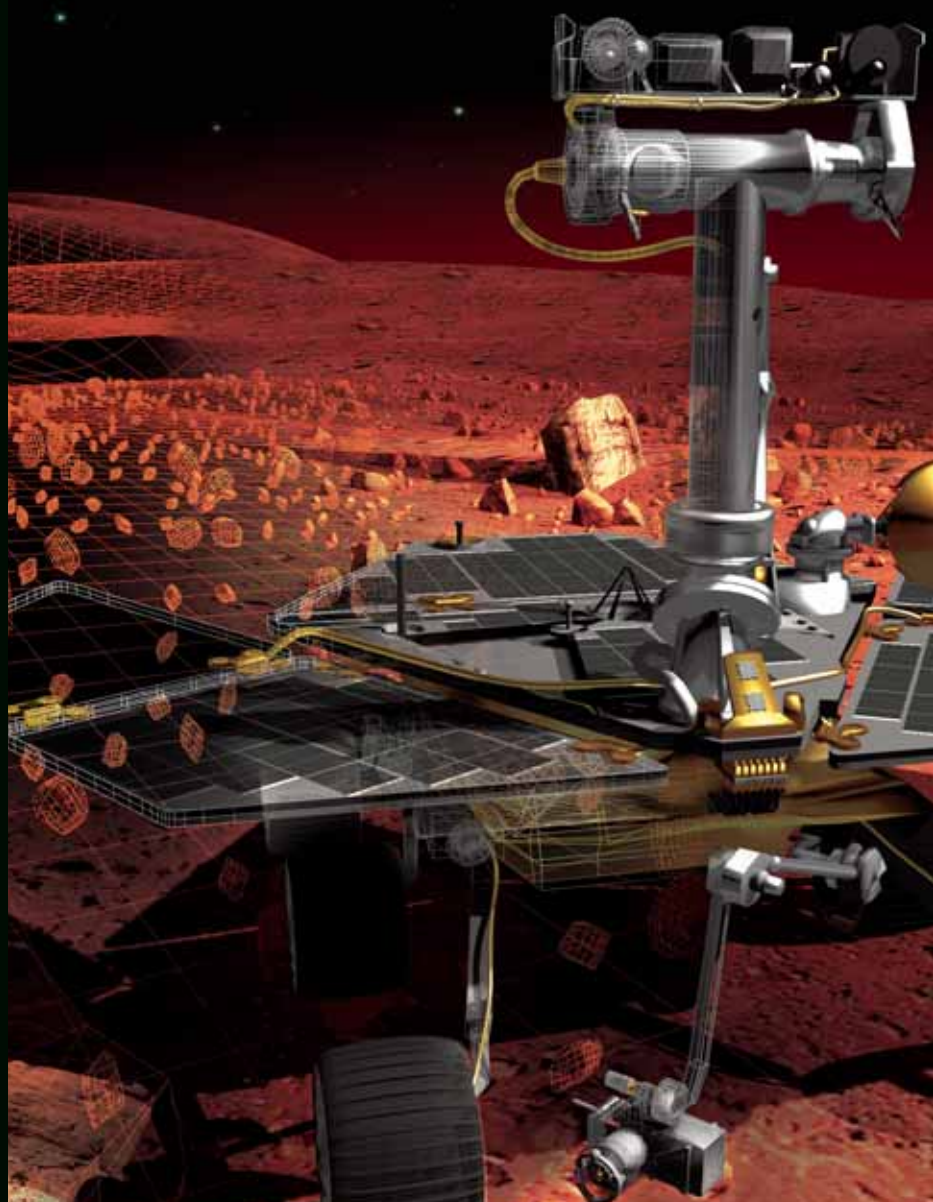

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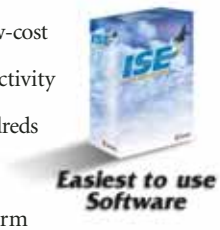


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# Thank You for Making Xilinx Number One

Ever have one of those days where you're working hard, nose to the grindstone, striving to make sure your latest project is on time and on target; and then suddenly out of nowhere, you overhear someone complimenting your efforts? It's not a comment that you solicited, but independently you find out that all of your hard work is recognized as the best among your peers and you're headed in the right direction.

CMP Media LLC, the parent company of *EETimes*, just dropped quite a few kudos on the Xilinx doorstep. Most of you know that every year CMP conducts a PCB and IC electronic design tool industry survey to sample the engineering community's view on design tool providers. This year, at the 2004 Design Automation Conference, CMP announced the results of their first FPGA vendor survey.

The ratings are striking. In 21 out of 22 categories measuring everything from best pre-sales support to brand and tool awareness, from most ethical company to customer loyalty, FPGA designers chose Xilinx as the top FPGA vendor. We received the highest rankings in best after-sales support, best documentation, current technology leader, technology leader in three years, clear vision of the future, best integration with other vendors' tools, well-managed company, and more.

We were also able to hear the industry concerns. Respondents cited the accuracy and integrity of FPGA tools as their biggest design issue, followed closely by functional verification, timing closure, and the ability of those tools to easily handle complex designs. They also said that the majority of their design time was spent in place and route, synthesis, and HDL simulation, followed by timing analysis and floorplanning. One-third of the respondents also use formal verification, while almost half regularly use signal integrity and C language system-level tools.

On behalf of all of the employees at Xilinx, thank you. We hear you loud and clear. Our primary goal is to put a programmable device in every piece of electronic equipment over the next 10 years. It's nice to hear that we're on the right path to get there.

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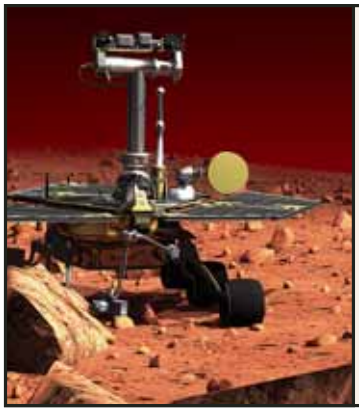

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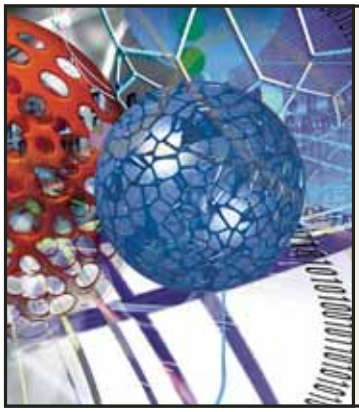

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# Preparing for a Bright Future

The economy is improving and most analysts predict that the semiconductor industry will grow for the next two years. Here's what I see ahead for Xilinx.



by Wim Roelandts
CEO, Xilinx, Inc.

We recently emerged from a three-year recession that was one of the longest and deepest in our history, yet things are getting better. The semiconductor industry typically moves in a two-year cycle, unless it is influenced by events such as the 9/11 tragedy. Therefore, after two years of growth, an overbuilding of capacity will likely occur, with another market correction in 2006. This is a normal and predictable cycle; it's the way our industry usually works.

These capacity-driven recessions tend to be shallow and short – the last one was in 1996 and lasted about 18 months. For Xilinx® during that period, we had a few negative growth quarters, with an overall 1% growth.

The market recovery is still fragile, driven primarily by the U.S. and China. And not all of the industries that we deal with are yet in recovery, which I think is good because it helps us maintain a steady growth pattern as they begin to improve later in the year.

Overall, Xilinx is in an extremely good position – our business processes, our manufacturing technology, our circuit innovation, and our software are poised to take full advantage of the current market conditions.

### The Growing Asian Markets

A significant and quickly growing segment of our business comes from the Japanese and Asia-Pacific markets – our business there is now more than three times higher than it was just four years ago. This comes both from systems that are designed and manufactured there as well as from manufacturing outsourced from other countries. Plus, Japanese business is starting to expand and is beginning to help drive the world economy forward.

I believe our business in Asia will continue to grow over the years to come. We see a big shift taking place, driven primarily by the next big trend in our industry – digital consumer electronics. The core of this business will be in Asia, and we are putting a lot of our resources there to help meet the demand. We recently began staffing a facility in Singapore that will eventually house more than 200 employees.

### Beating Moore's Law

Semiconductor technology typically follows Moore's Law, which states that every two years the number of transistors that can be fabricated on a chip will double – this law has held true for many years. As we approach finer and finer process geometries, moving from 130 nm to 90 nm and down to 65 nm, it becomes increasingly difficult to manufacture devices. Xilinx is leading the industry in the development and use of these advanced technologies, which means that we are often the first to solve difficult process problems – that's both the good and the bad news. We usually get to market first with the most advanced manufacturing processes, but we also put a lot of effort into getting it right.

We also have a strategy for significantly improving performance through innovative architectural designs – the best example is our new Virtex-4™ family. In fact, most of our performance improvements in the Virtex-4 family come from circuit enhancements. The Virtex-4 ASMBL architecture allows us to create devices that are optimized for specific applications, providing just the features and performance that are needed at the lowest possible cost. As you can see, our innovation is not just in CMOS technology – we are way ahead of our competition in both device manufacturing technology and architecture.

### Reducing Design Costs with IP

Our marketplace is changing rapidly, and our customers must operate differently today than they did four years ago. Their own customers are much more cost-conscious, and thus they are much more worried about return on investments. Our customers have fewer engineers because of the recession, so they demand more from us – it's one of the reasons why we are increasing our investments in IP and cores. Because cores allow us to provide a more complete solution, our customers have to do less work to produce more and better designs. And they want to buy cores from Xilinx because they want to have the assurance of ongoing long-term support. We are in fact increasing our investments in IP and cores to meet the increasing demand. We already have many more cores than our competitors, and thus we are very well positioned to take advantage of these trends.

### Xilinx Strategy for the Future

Here are some of the long-term objectives that define our strategy for the next five to 10 years.

#### Setting the Standard

We will continue to set the standard for how to manage a high-tech company. I think we have already done a phenomenal job – we're admired as a company that manages its people well, treats its people well, and at the same time is innovative and wins in the market. And of course, the core of our culture is innovation. We want to continue to bring new technologies, new circuitries, new innovative marketing programs, and new channels of distribution. This will continue to be the core of our strategy because it's what makes Xilinx excel in everything we do.

#### Leading Manufacturing Technology

We will continue to reduce our manufacturing costs. We made a lot of progress in the last year and now we need to move on to the next step. My intention is to make sure that all of our organizations are focused on low-cost, high-volume capabilities. The consumer electronics and automotive industries require us to reduce costs and ramp production faster than ever before. We will continue to innovate with-

Programmable logic is indeed taking over; it is becoming mainstream and finding new markets where it's never been used before.

### Going Mainstream

Eight years ago, when I joined Xilinx, I said that we will put a programmable chip in every system, and it's now becoming a reality. Our ability to shrink our products into smaller and smaller geometries at lower costs, coupled with the recession (which means that many of our customers can no longer afford the high costs of designing and building ASICs) is moving more and more of our customers to take full advantage of the many benefits of programmable logic.

Market forces, combined with our low-cost technology advances, are driving programmable logic into the mainstream – our devices are now used in all types of products and the trend continues to grow. Over the next two or three years, when these new designs go into production, our business will expand significantly. Programmable logic is indeed taking over; it is becoming mainstream and finding new markets where it's never been used before.

**For the next 10 years, we want to extend our brand and establish Xilinx as a global leader, recognized not only by the engineering community but also by the financial community.**

in all of our organizations to achieve this ongoing objective. For programmable logic to achieve its full potential in mainstream electronics, we must become even more efficient and productive – and we will.

Yet, while we continue to develop more high-volume strategies and products, we will continue to lead the high-end, high-performance market that has traditionally been the core of our business. We are doing a phenomenal job with our Virtex product line, with 70% to 80% market share, and that will continue as well.

**Creating Partnerships**

Partnerships are a key strategy that allow us to focus on what we do best while allowing other companies to provide the products and services they do best – we call it our Partner Ecosystem. We will continue to build strong partnerships not only with our suppliers but with our customers as well.

We want to engage our customers early in their design process so that we can provide the best possible service and support throughout their entire design and manufacturing cycle. This requires a broad range of services from a number of ecosystem partners, and that requires a well coordinated and comprehensive approach. We have been successful with our partnership program in the past and we intend to strengthen it by making it easier for our customer partners – and our technology partners – to work more closely together for the benefit of all.

**Expanding Our Markets**

We are already the leader in programmable logic technology, and now it's time for us to become a leader in all programmable technology, including DSP and embedded processing. Our technology already provides significant advantages in these areas, and it's time for us to capitalize on these strengths. We want to be the champion of programmability because we are the only company that can provide the advantages of programmable logic, high-performance DSP, and embedded processing all on one device.

We are the largest company in programmable logic, with 50% market segment share. However, the embedded processor market and the DSP markets also offer significant market opportunity.

**Brand Recognition**

Xilinx is already well respected and recognized in our marketplace, and we will continue to build our brand worldwide. Our success in the first 10 years was based on two innovations: FPGAs and fabless manufacturing. When we started in 1985, neither of these ideas was credible. Only the Xilinx founders believed they would work. Yet we made them possible and we made them credible.

Our second 10 years were based on two things: becoming the technology leader in our industry and establishing a unique business culture that fosters innovation. In that we have also been very successful.

For the next 10 years, we want to extend our brand and establish Xilinx as a global leader, recognized not only by the engineering community but also by the financial community. We want to be recognized not only for our innovative culture but also for our financial stability, management depth, the global reach and diversity of our products, and by the brand name we create.

**Going Global**

We will continue to expand globally and place our resources close to the markets they serve. If 20% of our business is in Asia, we will strive to place 20% of our resources there because we want to be close to our customers and understand their needs. That's why we opened up a new factory headquarters in Singapore and a new design center in India. We want to have a presence in Asia just like we have in Europe and the United States.

**Conclusion**

Innovation remains the core of Xilinx. I believe innovation is the only thing that matters because if you innovate, there is no competition. That's the reason why we have gained market share every single year in the last six years.

As you can see I'm very excited about our current situation, and I'm even more excited about our future.

# FPGAs on Mars

Xilinx FPGAs have transitioned from a flight ASIC prototyping platform to playing integral roles in the Mars Exploration Rover Mission.

by David Ratter
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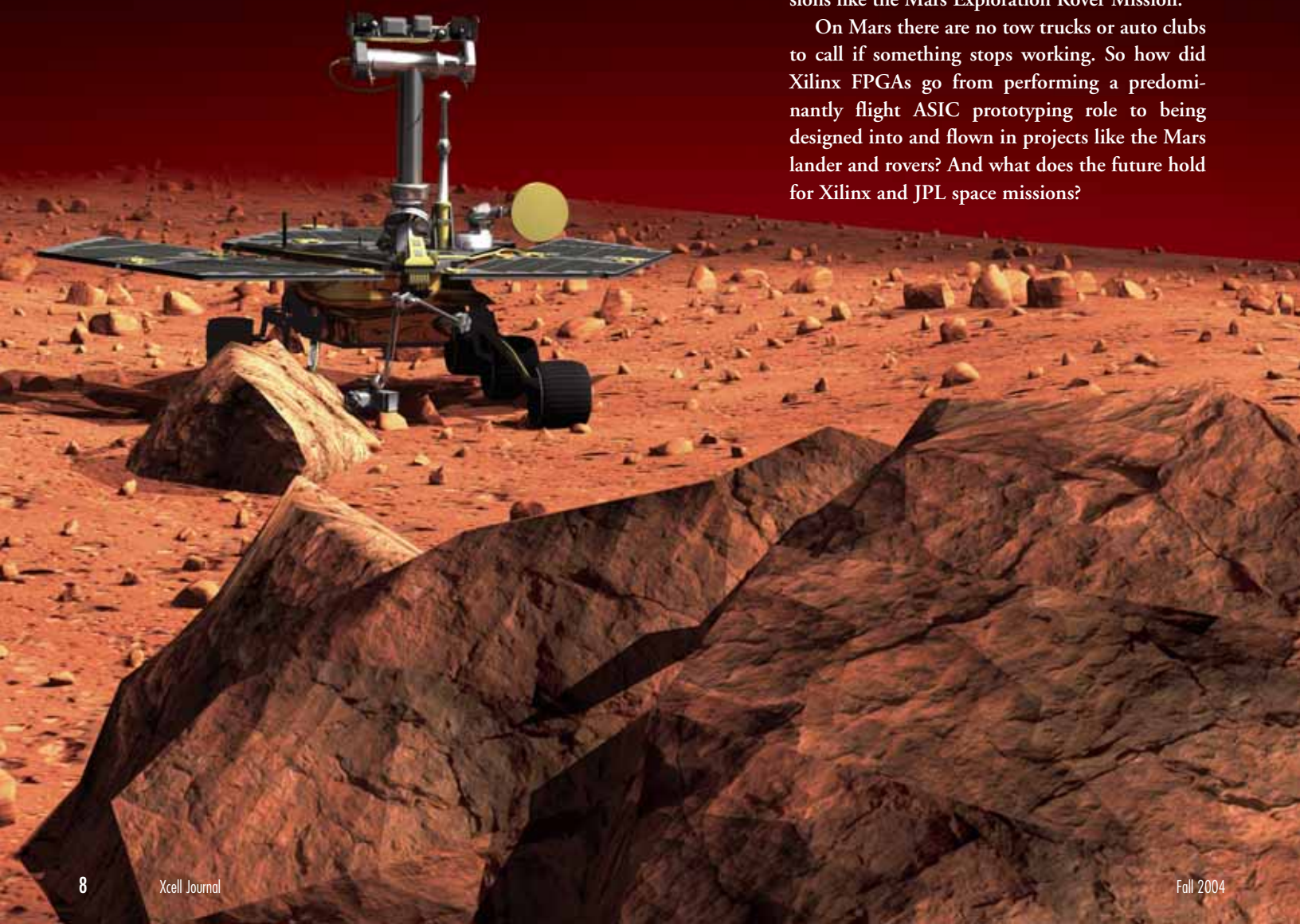
**Selecting the correct components for any engineering project can be a critical and difficult choice. This is clearly true for engineers at the Jet Propulsion Laboratory (JPL) when they must select components used on high-stakes flight projects, and especially important on high-profile missions like the Mars Exploration Rover Mission.**

**On Mars there are no tow trucks or auto clubs to call if something stops working. So how did Xilinx FPGAs go from performing a predominantly flight ASIC prototyping role to being designed into and flown in projects like the Mars lander and rovers? And what does the future hold for Xilinx and JPL space missions?**



The needs of JPL's design engineers were the main driving force behind the paradigm shift from ASIC prototype to flight-qualified part, as were the Xilinx testing, processing, and manufacturing flows for its radiation-tolerant FPGAs. Engineering needs demand meeting mission requirements, both from a functional/performance viewpoint and a time-to-working-product viewpoint. Xilinx FPGAs provide inherent design advantages to meet those needs: high gate densities, rich on-board architectural features, large I/O counts with multiple I/O standards, and the ability to be reprogrammed at any time.

The second reason for the transition was JPL's qualification of Xilinx radiation-tolerant FPGAs into more and more flight situations.

The net results of these efforts can easily be seen on the Mars Exploration Rovers. Inside of each rover (named Discovery and Spirit), two Virtex ™ XQVR1000s served as the main brains that controlled the motors. Four Xilinx XQR4062XL devices in the 4000XL family controlled the Mars lander pyrotechnics, crucial to the successful multi-phase descent and landing procedure. Also evident, although not as visible, are the increasing number of future flight missions that JPL engineers are designing with Xilinx radiation-tolerant FPGAs.

In this article, we'll briefly document the parts qualification and design steps, along with the past, present, and future of FPGA-based flight opportunities at JPL.

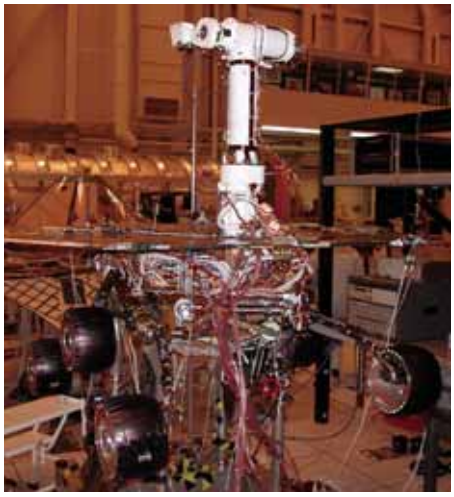
## Flight Considerations

There are three steps that must be accomplished before any part can be used in a flight application for JPL. The first is a general flight approval for a part. The second can be referred to as mission-specific approval. The third is additional design requirements for flight-based semiconductors.

### General Flight Approvals

JPL must give general flight approval before any part can be used for a flight application. This process requires that the manufacturer perform numerous additional processing, testing, and quality steps over and above the normal commercial processing steps.

JPL also meticulously examines device statistical and quality data that is constantly updated by the semiconductor manufacturers. They also examine additional parameters in this phase, including temperature considerations and packaging materials as well as semiconductor characteristics (for example, are there voids or contaminants that in zero gravity could migrate and cause failures?). Only after JPL engineers have conducted exhaustive research and analysis do they approve parts for flight use.



JPL Radiation Effects Group scientists work directly with Xilinx to unify and continually improve the testing, processing, and manufacturing steps used for Xilinx radiation-tolerant parts. This close customer/manufacturer relationship has resulted in a much superior radiation-tolerant product from Xilinx, and for JPL, a high-reliability manufacturing process gives them the utmost confidence.

### Specific Flight Approvals

Even after a part or parts has general flight approval, it still must receive mission-specific flight approval. Mission-specific approval is exactly what the term implies: JPL scientists and engineers review the mission-specific environments that the parts will encounter. This includes a detailed risk assessment.

JPL takes into account all aspects of the flight to predict what the part(s) will face during the mission's lifetime. Some of these parameters might include the number of temperature cycles, total ionizing dose, and predicted rate of radiation exposure. It is possible that parts with general flight approval will not get mission-specific flight approval.

### Specific Flight Design Considerations

Only after a part has met the above two criteria can it be used in a flight mission. The design process entails incorporating space-specific flight design requirements that include, but are not limited to, the following single-event phenomena:

- Single-event latch-up (SEL)
- Single-event upsets (SEU)
- Single-event transients (SET)
- Single-event functional interrupts (SEFIs)

In the case of Xilinx radiation-tolerant FPGAs, all single-event phenomena are taken into account either through the radiation-tolerant manufacturing and processing steps or through well-documented design practices:

- The epitaxial layer of Xilinx radiation-tolerant FPGAs eliminates SELs.
- Triple-mode redundancy (commonly referred to as TMR) mitigates SEUs and SETs.
- "Scrubbing," or reprogramming the FGPA, takes care of SEFIs and the accumulation of SEUs.

Let's discuss the latter two design features in more detail.

In simple terms, a design with TMR requires three sets of key logic elements, with a voting structure that allows only the majority decision to propagate through the circuit. The theory is that statistically you are going to get an SEU over some time period. When this upset occurs, it will disrupt a single element (net, route, or bit). When this happens and the element it disrupts is being used, the other two "correct" elements will have the correct value; thus, the correct value will be passed out of the circuit. This is especially important in circuits that use feedback, such as counters and state machines.

Numerous approaches can be taken with respect to scrubbing, from simply reprogramming the FPGA to partial reconfiguration. The simplest method of scrubbing is to completely reprogram the FPGA at some periodic rate (typically 1/10 the calculated upset rate).

For example, if an SEU will occur once every 10 days, then you would reprogram the FPGA every day. However, when you reprogram the FPGA it is not operational during that reprogram time (on the order of micro to milliseconds). For situations that cannot tolerate that type of interruption, partial reconfiguration is available. This technique allows the FPGA to be reprogrammed while still operational.

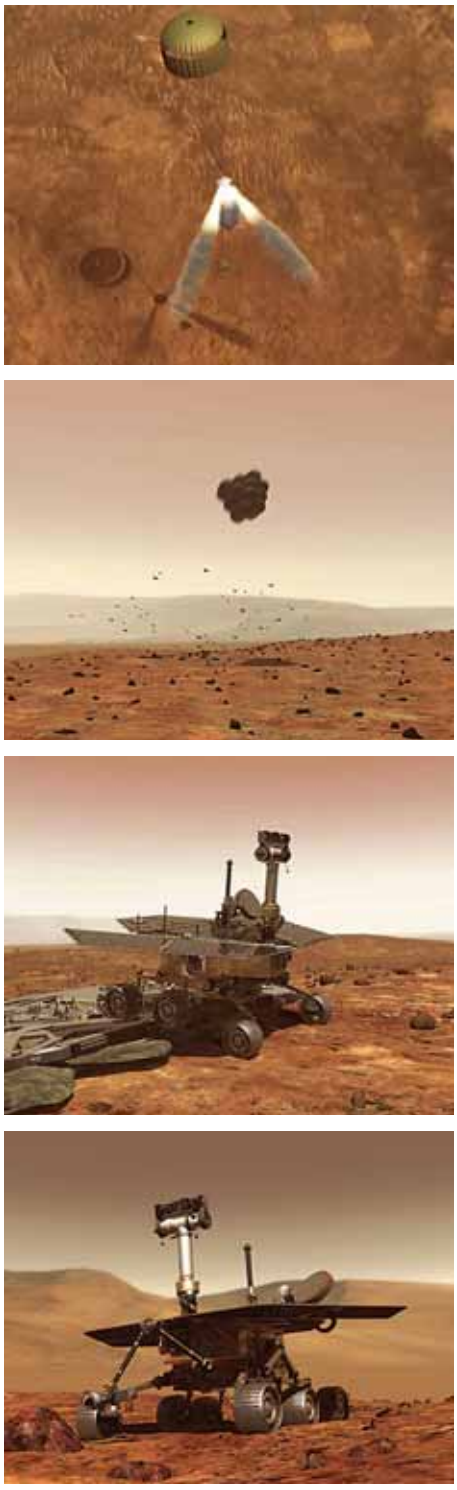
### The Past

Although the both the Discovery and Spirit rovers are still on the surface of Mars and active, they were launched in June and July 2003 and landed on Mars in January 2004. This means, obviously, that the engineering was completed in the past.

As stated earlier, the Mars Exploration Rovers used XQVR1000 devices and the lander used XQR4062XLs. The XQR4062XLs were used during the descent and landing of the rovers on the surface of Mars, while the XQVR1000s were used to control all of the brushed DC and stepper motors for the wheels, steering, antennas, camera, and other instruments on the rovers themselves.

Both the XQR4062XL and XQVR1000 designs used TMR for SEU and SET mitigation as well as scrubbing. JPL engineers achieved TMR in their designs by analyzing the design for feedback nets and other low-level design details (as detailed in Xilinx application note XAPP197), and then inserted or replaced logic with TMR library elements. After the designs were functionally implemented, the engineers went back through the design and inserted the TMR logic where necessary and made other space-specific design changes.

Due to the critical nature of the XQR4062XL's role, FPGA redundancy was utilized to mitigate all single-event phenomena. The scrubbing technique employed was a complete reconfiguration.



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When an upset condition was detected, the FPGA in question was completely reprogrammed, while the redundant FPGAs remained functional. On the other hand, because of its non-time critical nature, when a fault condition was detected on one of the XQVR1000s, the rover was temporarily halted, the FPGA was reprogrammed, and the rover went back on its merry way.

All of the mitigation techniques on the Mars Exploration Rovers worked exactly as designed by JPL engineers. During the seven-month voyage from Earth to Mars, the Xilinx radiation-tolerant FPGAs on the lander were "left on." During that time JPL collected data of interest, including the upset rate. The upset rates predicted for the FPGAs by JPL matched almost exactly the actual upset rates observed. Also, the upset detection and mitigation techniques implemented on the FPGAs performed their functions flawlessly and allowed for robust and reliable operation.

### The Present

JPL is currently working on flight designs with both Virtex-II™, the latest Xilinx radiation-tolerant family, as well as Virtex radiation-tolerant FPGAs. These new missions will fly in the next two to five years and are becoming more and more sophisticated in both mission electronic requirements and design implementation. These current projects more fully utilize the FPGA's inherent benefits.

JPL is particularly interested in the ability to update or revise designs while the spacecraft is either in flight to its final destination or already there. This will allow engineers to implement algorithm enhancements after the spacecraft has left Earth, enabling them to constantly improve design performance during a long mission timeline. This, coupled with partial reconfiguration, will allow an FPGA-based design to have one portion of its design upgraded while the rest of the design remains completely operational.

There have been some breakthroughs in the area of single event mitigation and correction. Xilinx, in partnership with Sandia Labs, recently produced a TMR tool that

will XTMR a design. The XTMR tool takes in a synthesized netlist, analyzes it, and applies the appropriate TMR measures and space-specific design modifications to produce a final XTMR netlist. Not only does this guarantee a much more robust TMR design, it also takes what used to take an engineer days or weeks to perform and reduces the process to a matter of minutes.

### The Future

Who knows that the future has in store? The new missions have more demanding requirements: more speed and more integration, with an ongoing goal of less space and less weight. On the Xilinx front, each subsequent family of radiation-tolerant FPGAs (like Virtex-II Pro™ devices) will provide more integration, more architectural features, and more capabilities.

The need for more integration, speed, and reduced space and weight goes hand in hand with continually improving radiation-tolerant FPGAs. Xilinx advances in FPGA technology and the improvements in radiation testing and processing made possible by their relationship with JPL come together to spell success.

### Conclusion

The collaborative efforts between JPL, the Xilinx aerospace and defense team, and local support (provided by the manufacturer's representative, Norcomp SC, and Nu Horizons Electronics Distribution) helped pave the way for Xilinx to go from a predominantly ASIC prototyping role to become key components in the successful design and implementation of the Mars Exploration Rovers.

Current JPL flight projects that will launch in the years to come are already being designed using the latest Virtex and Virtex-II Xilinx high-reliability FPGAs. And the continual release of bigger, faster, and better Xilinx radiation-tolerant families means that with Xilinx and JPL, not even the sky is the limit.

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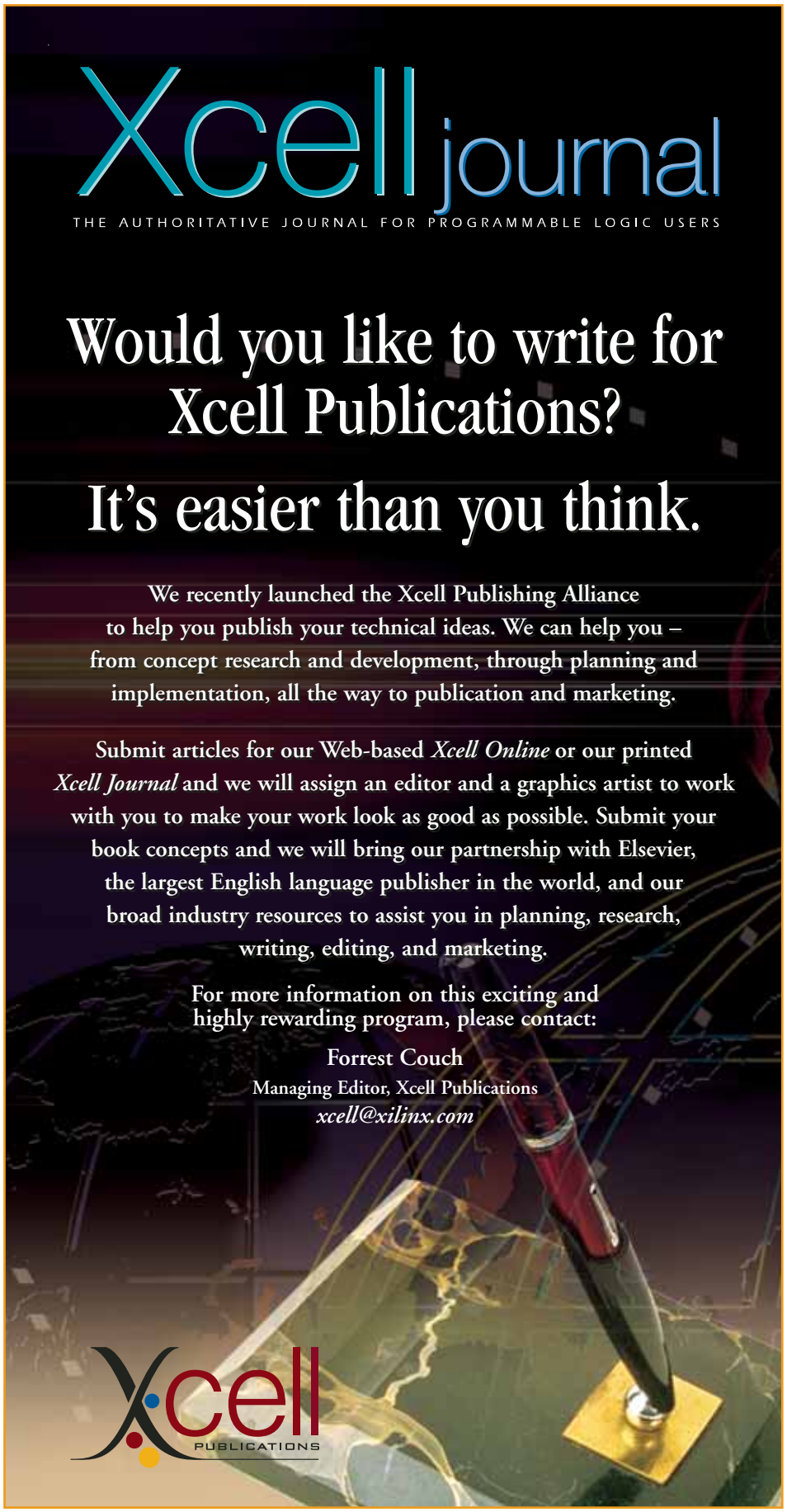

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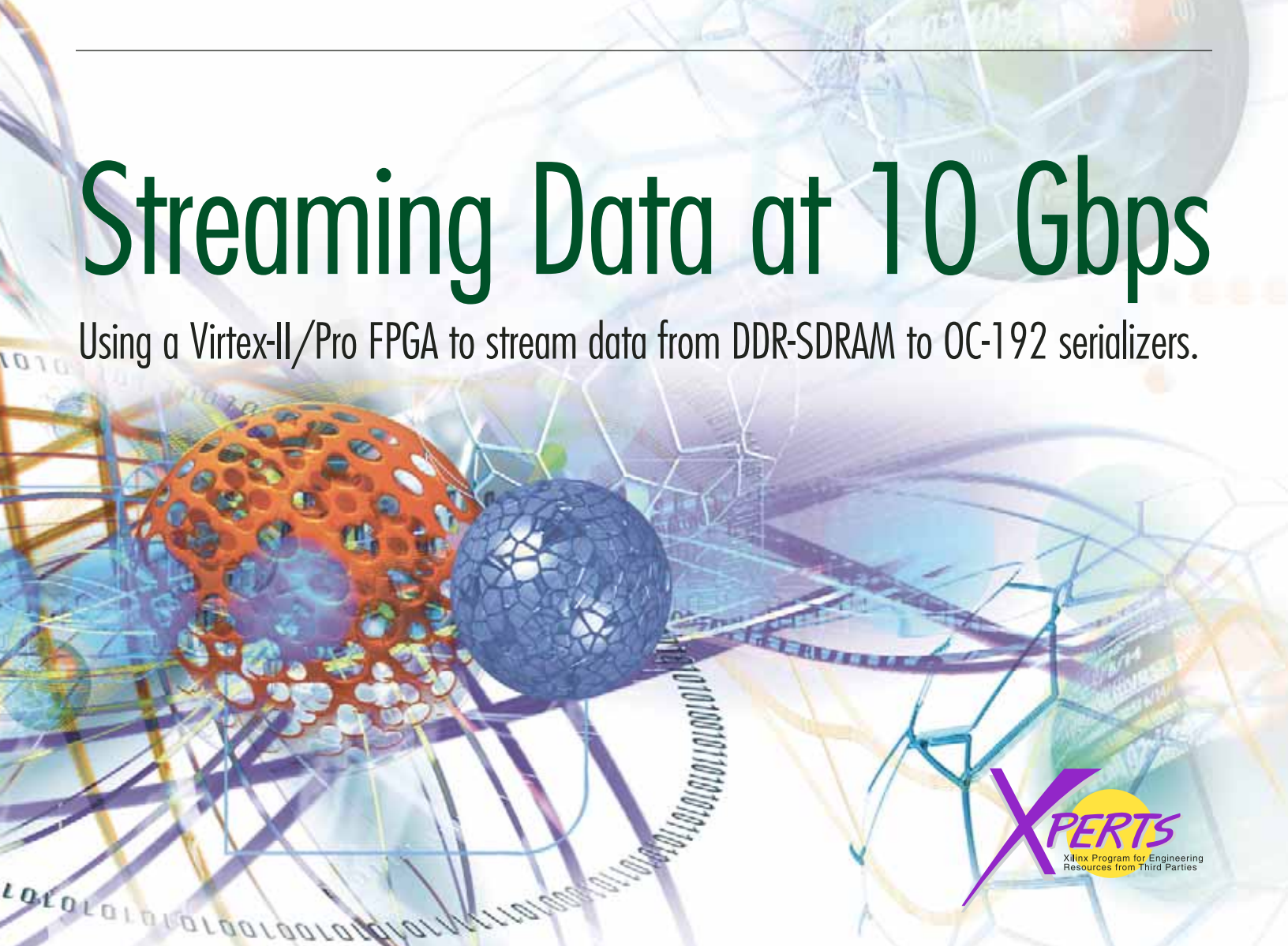
# Streaming Data at 10 Gbps

## Using a Virtex-II/Pro FPGA to stream data from DDR-SDRAM to OC-192 serializers.




by David Banas
President
Tao of Digital, Inc.
*dbanas@taoofdigital.com*

You'd like to use DDR-SDRAM as the storage medium for OC-192 test pattern generation to dramatically increase the length of patterns available to you. However, when you take the standard approach to architecting this interface and attempt implementation in a FPGA, you find that the FIFO read clock enable signals don't meet the timing requirements. Your project budget can't afford an ASIC. How can you get around this issue and make the FPGA work as the needed interface?

Fortunately, the Xilinx® digital clock manager (DCM) provides the answer. As long as you've got sufficient global clock resources available, you can use the DCM's quadrature-phase outputs to clock the outputs of the four FIFO groups directly. This eliminates the need for clock enable signals in the 320 MHz clock domain and yields a design that will achieve timing closure at that speed.

### Standard Architecture

Figure 1 shows the standard architecture used to design a streaming data interface between DDR-SDRAM and OC-192 serializers. All of the design blocks shown in this figure, with the exception of the FIFO/MUX controller, are available as directly instantiated elements (the DDR flip-flop), Xilinx CORE Generator™ modules (MUX *x* and FIFO *n*), or Xilinx-provided reference designs (DDR-SDRAM controller).

### DDR-SDRAM Controller

The DDR-SDRAM controller is a modified Xilinx-provided reference design. I modified it to provide a continuously streaming mode of operation. The controller provides the necessary address and control signals for driving a standard PC-1600/2100 DDR-SDRAM module and also converts the data bus from a 64-bit DDR mode to a 128-bit SDR mode to facilitate a simpler clocking scheme inside the FPGA.

The controller stops fetching data from memory and disables the write enable signal to the FIFOs when it detects that FIFO_0's high watermark signal has gone active (not shown in Figure 1).

The frequency of clock 1 is 100 MHz, yielding a burst data rate of 12.8 Gbps. This data rate is 28% higher than that required by the serializer, leaving room for overhead tasks such as DRAM refresh.

### FIFOs

The eight FIFO blocks represent standard, asynchronous FIFO elements generated using the CORE Generator tool. The FIFOs serve a dual purpose. First, they provide elastic buffering between two asynchronous clock domains. Second, they work in conjunction with the MUX *x* and FIFO/MUX controller blocks to provide

the data bus width reduction. This is necessary to convert from the 128-bit data bus presented by the DDR-SDRAM controller to the 16-bit data bus required by typical OC-192 serializers. I will explain this functionality in more detail.

### MUXs

The two multiplexer blocks represent standard 4-to-1 synchronous 16-bit bus multiplexers also generated using the CORE Generator tool.

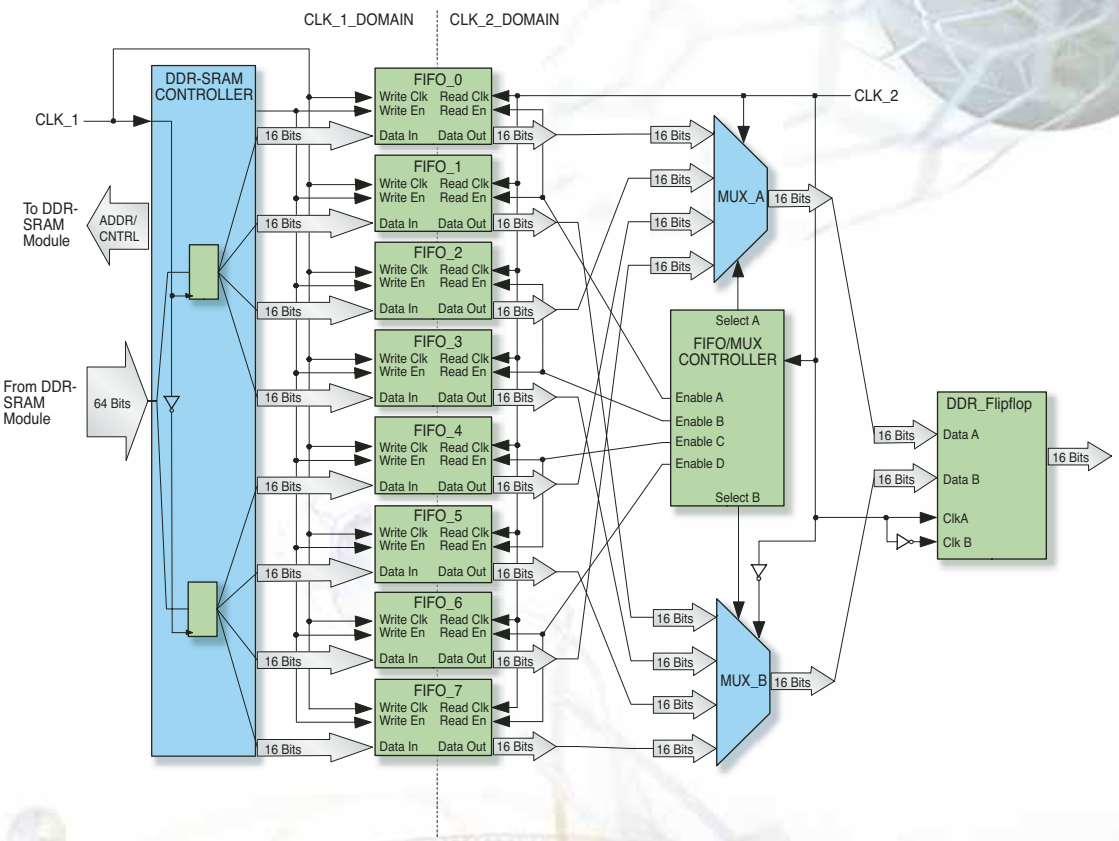



*Figure 1 – Standard architecture*

### DDR Flip-flop

The DDR flip-flop is a directly instantiated element of the Virtex-II™/Pro™ architecture. Its two inputs are multiplexed onto its single output through successive clocking at both clock edges. In this way, the data A input is clocked through to data out at the rising edge of the clock, while data B is clocked through at the falling edge.

### FIFO/MUX Controller

The FIFO/MUX controller is the only fully custom element in the architecture (also shown in Figure 1). Its operation is straightforward and you can easily understand it by looking at the timing diagram of Figure 2.

Note that while the signals generated by the FIFO/MUX controller are not explicitly shown in the timing diagram, their behavior is implicitly depicted there. For instance, the outputs of FIFOs 0 and 1 only change when the enable A signal from the FIFO/MUX controller is active.

Likewise, whenever a multiplexer output changes, it is the respective select X signal from the FIFO/MUX controller that dictates which of the multiplexer's four inputs gets clocked through to its output.

## Timing Discussion

As mentioned previously, Figure 2 depicts a timing diagram that describes the dynamic behavior of the architecture shown in Figure 1. The clock signal shown is clock 2 from Figure 1. (The clock 1 domain does not contain any novel design features.)

The clock period "T" is 3.125 ns (1/[320 MHz]). The numbers identifying the various data intervals correspond to the index of a particular 16-bit word in a sequence of data, which is at least 24 16-bit words in length. The FIFO outputs are updated once every four clock cycles in quadrature succession, as shown in the timing diagram.

The two multiplexers select from among the four FIFO groups in the same succession. However, a delay is imposed on the multiplexer selection sequence such that the FIFO outputs are allowed three clock cycles to propagate to the multiplexer inputs before being selected, as shown.

By designing this way, I can apply a multi-cycle delay constraint to the FIFO outputs and thus ease the task of the place and route engine. This is very helpful when designing in a 320 MHz clock domain. The DDR flip-flop selects from among its two inputs in standard fashion, as shown. The result is a 640 Mword/s data stream at the output, yielding a data rate to the serializer of 10.24 Gbps.

## Implementation Results

Up to this point, the proposed architecture appears to satisfy the design requirements. However, when I tried to implement this approach in a XC2V1000-6BG575 part, I couldn't get the propagation delays of the FIFO read clock enable signals under the 3.125 ns period constraint imposed by the 320 MHz clock. Therefore, I came up with the following modification to the basic architecture (Figure 3), which resulted in successful timing closure.

## Modification Description

In the modified architecture shown in Figure 3, I eliminated the clock 1 domain section of the design, as it is irrelevant to

the discussion. The only design block that changed in the modified architecture is the FIFO/MUX controller; all other design blocks remain unchanged.

Instead of generating clock-enable signals, the controller block generates four 80 MHz clocks in a quadrature phase arrangement. This is very easy to accomplish when designing for the Xilinx Virtex-II/Pro architecture, as the DCMs in that architecture have quadrature phase outputs. All I had to do was divide down the 320 MHz clock by a factor of four, using an additional DCM, to generate the original 80 MHz clock signal.

When I apply these quadrature-phased 80 MHz clocks directly to the four FIFO groups, respectively – without using any clock enable signals – the data at all FIFO outputs is exactly as required by the original architecture. You can see this fairly easily by envisioning these four clocks overlaid atop the four FIFO *n*/*n* signals in the timing diagram of Figure 2.

Notice that the rising edges of the four clocks line up perfectly with the changes in the outputs of the four FIFO groups. You no longer need to use clock enables to govern the FIFO read clocking and have, therefore, eliminated the one group of signals that failed to achieve timing closure. Of course, you must have two additional DCMs and five additional global clock buffers available to make use of this approach.

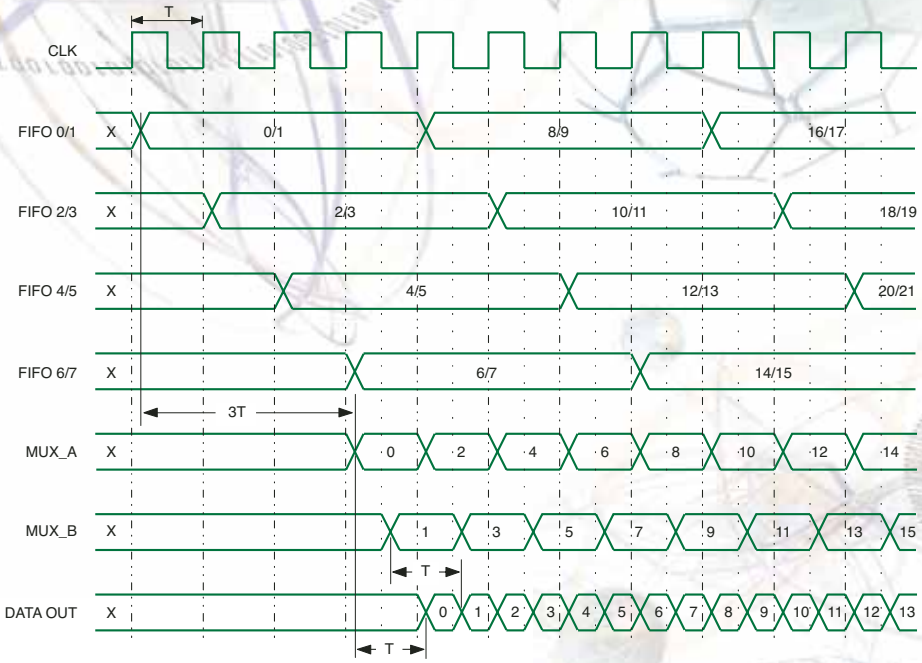



*Figure 2 – Output data timing*

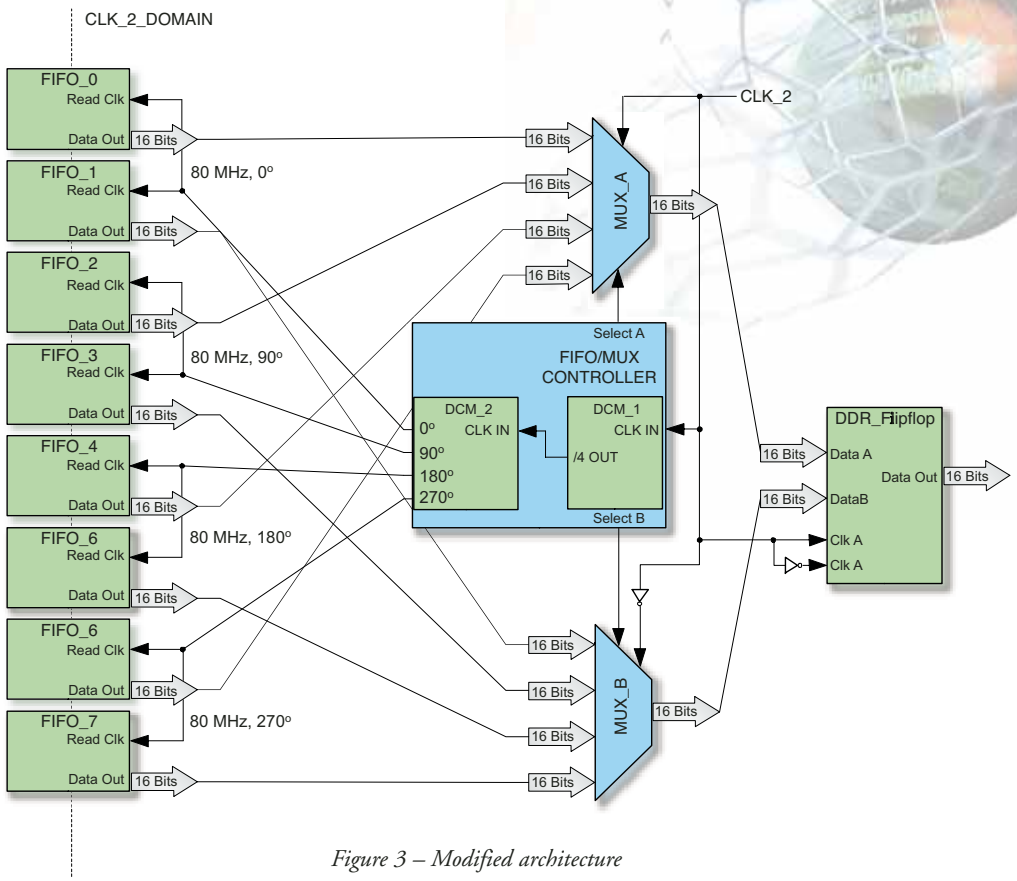



*Figure 3 – Modified architecture*

## Conclusion

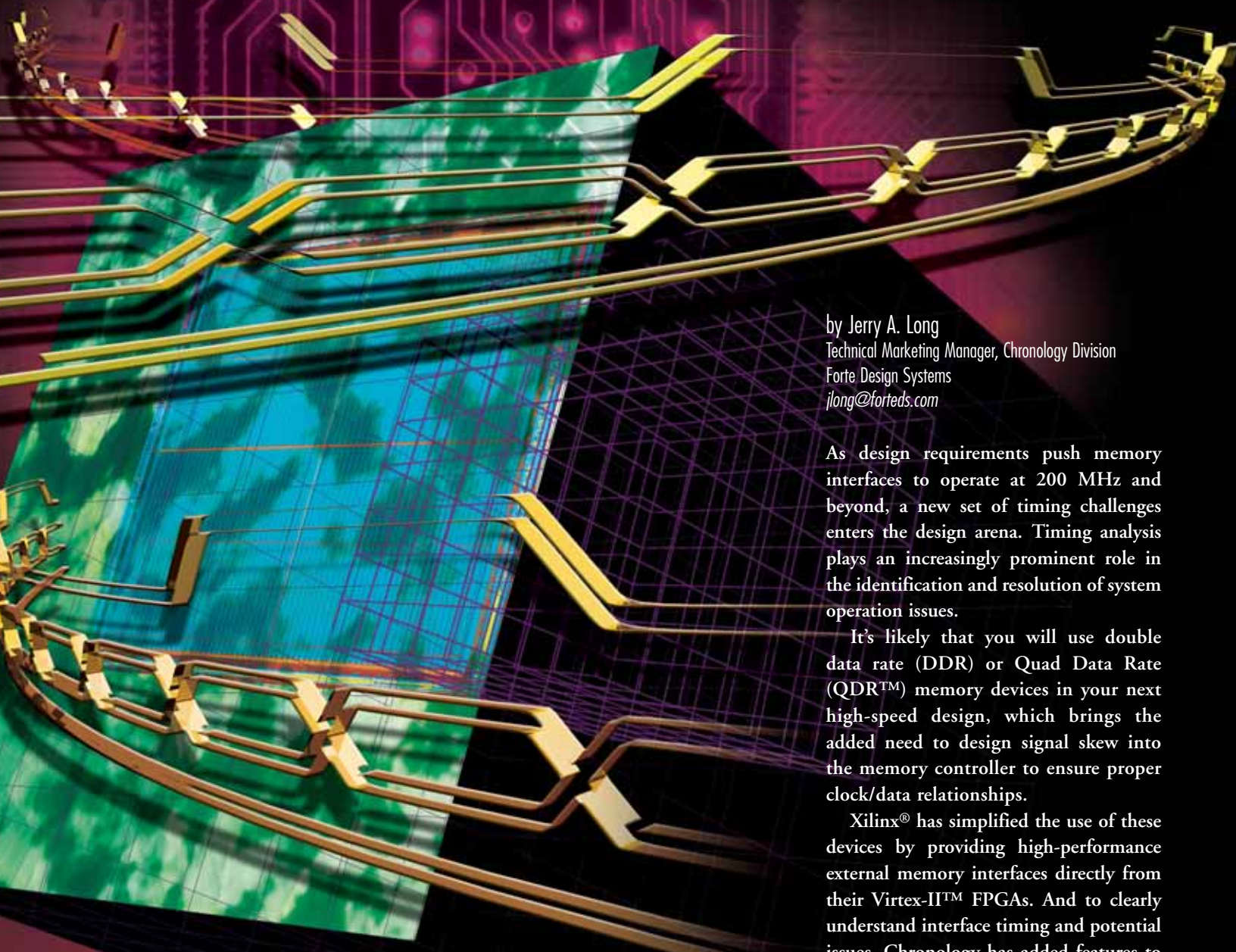
By taking advantage of the design technique presented here, OC-192 test pattern generation hardware designers can avail themselves of the low cost and large capacity of standard DDR-SDRAM modules, thereby making possible the use of extremely long test patterns or automated testing with many shorter patterns, all without incurring the cost of ASIC design and production.

The technique presented here will also find applicability in the area of direct digital synthesis (DDS) of arbitrary waveforms, where a high-speed digital waveform is used, in conjunction with PWM or Sigma/Delta modulation and subsequent low-pass filtering, to produce arbitrary waveforms with great precision and repeatability.

If you have any questions or suggestions, please contact me, David Banas, at (415) 846-5837, or e-mail at *dbanas@taoofdigital.com.* Σ

# Control Your QDR Designs

## A step-by-step guide to solving QDR memory data capture challenges with Virtex-II FPGAs.



by Jerry A. Long
Technical Marketing Manager, Chronology Division
Forte Design Systems
*jlong@forteds.com*

**As design requirements push memory interfaces to operate at 200 MHz and beyond, a new set of timing challenges enters the design arena. Timing analysis plays an increasingly prominent role in the identification and resolution of system operation issues.**

**It's likely that you will use double data rate (DDR) or Quad Data Rate (QDR™) memory devices in your next high-speed design, which brings the added need to design signal skew into the memory controller to ensure proper clock/data relationships.**

**Xilinx® has simplified the use of these devices by providing high-performance external memory interfaces directly from their Virtex-II™ FPGAs. And to clearly understand interface timing and potential issues, Chronology has added features to its TimingDesigner® tool to streamline the exchange of critical timing data with the Xilinx ISE software suite.**

TimingDesigner generates place and route constraints, allowing direct use of post-place-and-route timing information to verify desired FPGA interface operation. You can accurately determine the proper clock/data relationship for your DDR/QDR memory interface design, export the information as constraint data into ISE, and automatically get visual verification of design success.

For the purposes of this design guide, we'll use a QDR SRAM device to illustrate a source-synchronous interface design. Stepping through the design flow, we implemented a QDR memory controller in a Xilinx X2V50 Virtex-II Pro™ FPGA with a focus on the interface signals required for a read operation, utilizing a 133 MHz master clock. The memory device is a Micron™ 18 Mb QDR II four-word burst SRAM (MT54W1MH18J).

The features and principles outlined here are not necessarily unique to high-speed memory design. TimingDesigner's robust timing diagram-based analysis features, coupled with its Xilinx-specific import/export capabilities, allow a level of integration that can be applied to any timing-critical design interface for Xilinx FPGAs.

## QDR Interface Timing Requirements

QDR SRAM devices have unique timing requirements for successful read operations. In order to guarantee accurate data capture, QDR devices require the capture clock to be center-aligned within the valid data window. For source-synchronous designs, this means shifting the optional-use echo data clock supplied by the QDR device.

### Center Alignment of Capture Clock Edges

Proper timing for read operations of QDR SRAM interface designs requires you to center-align the edges of the capture clock within the valid window of the data bus for accurate data capture, as shown in Figure 1. This is because most SRAM devices typically have a positive setup and a positive hold requirement, and both are roughly the same value. So it makes sense to center the clock edge within the data valid window to maximize the safety margin for latching data. To accomplish this, the memory controller must skew the capture clock.

For source-synchronous capture of read data from a QDR device, you must use the optional echo clock signals (typically CQ and CQ#) provided from the QDR device. With the Virtex-II Pro family of FPGAs, skewing this clock is easily accomplished using one of the digital clock managers (DCM). However, the amount of phase shift necessary to achieve a safe margin is an unknown, given the external PCB skew effects on both the incoming data and its associated clock, as well as the associated routing delays encountered within the FPGA fabric. TimingDesigner will help us to accurately determine this phase shift value.

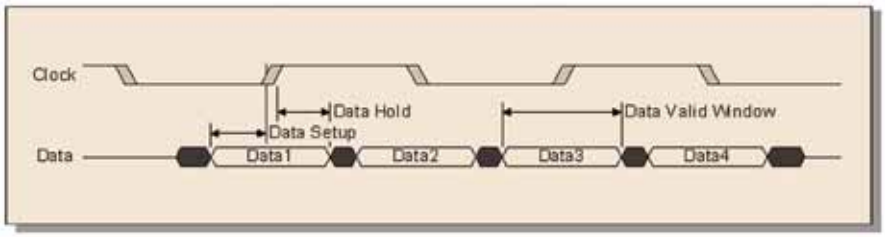



*Figure 1 – Illustration of center-aligned clock/data relationship*

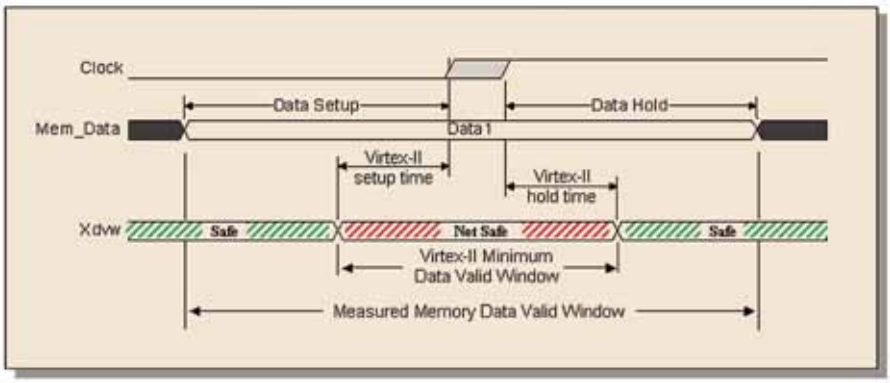



*Figure 2 – Center alignment of device minimum data valid window*

## Capturing Read Data in Virtex-II Pro Devices

You can skew (or delay) the clock signal by using PCB trace delay techniques, or by designing clock delay into the memory controller design. Because PCB trace delay techniques aren't very flexible, it makes more sense to use the incidental PCB trace delay coupled with internal FPGA routing delay and use the Virtex-II Pro DCM element as the "adjustable" component for phase shift within the FPGA memory controller design.

Typically, memory manufacturers recommend center alignment of the clock/data relationship to ensure that various temperature effects the design may encounter (or other unforeseen influences) won't cause an excessive amount of drift in signal position during the read operation and result in a violation of the setup or hold time requirement of the receiving register. In theory, a center-aligned clock edge will maximize the setup and hold times for most devices, allowing sufficient safety margins for signal drift.

However, some devices, like the Virtex II-Pro device, have a negative hold time requirement, which simply means that data can transition to the next value before the clock edge that latches it. In effect, this characteristic places the clock edge to the right (delayed) of the data transition. So for these devices, if you center-align the capture clock within the actual data valid window, you may be satisfying the setup/hold requirements of the device, but the safety margin achieved will be greater for the hold requirement than for setup.

The ideal solution is to provide a maximum safety margin for both the setup and hold requirements of a device, which translates to "balancing" these margins. This provides equal amounts of safety for both, as illustrated in Figure 2.

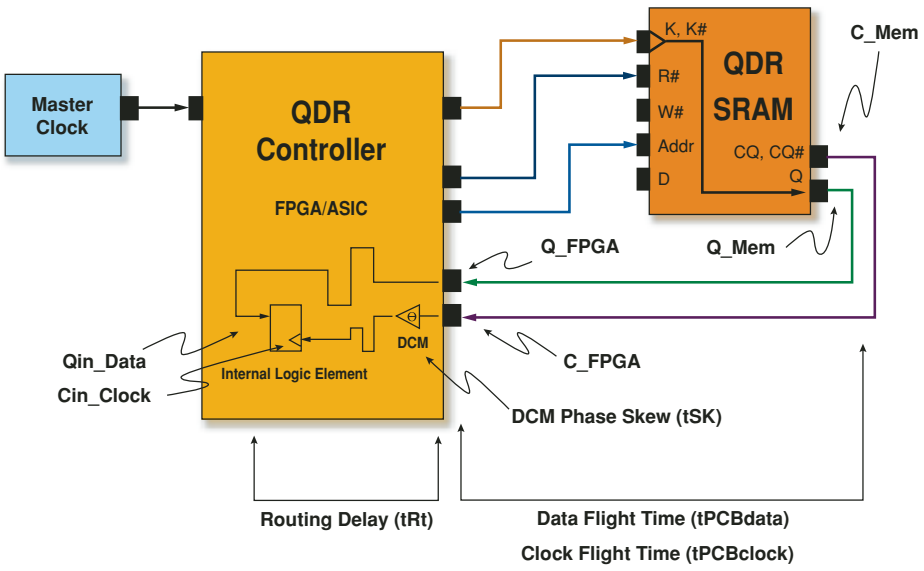



*Figure 3 – Illustration of signal delay paths for QDR read operation*

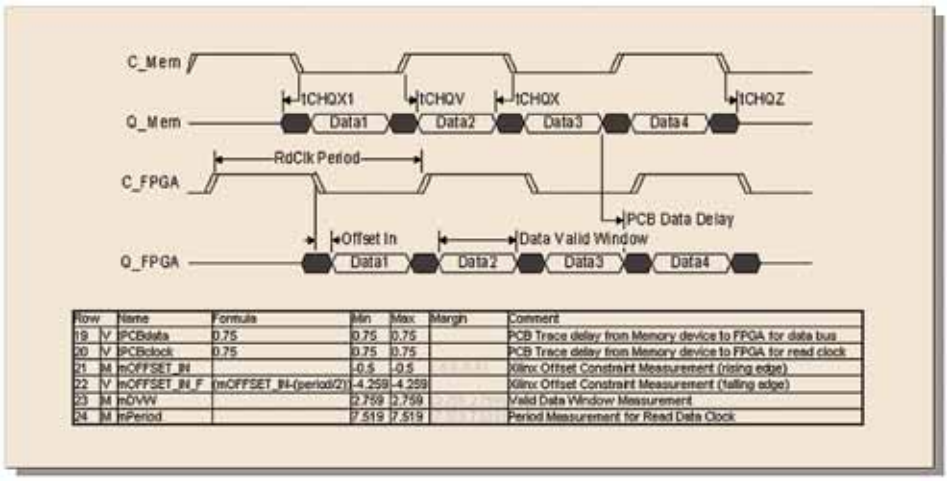
To accomplish this balance, you must determine the minimum data valid window for the receiving device, and center that window within the actual data valid window provided from the memory device, given your design parameters. Using the minimum setup and hold characteristics of the receiving device, determine a minimum "safe" data valid window with the following formula:

Min Data Valid Window = Min Setup + Min Hold

Because the placement of the resulting minimum data valid window is tied to the placement of the clock signal, skewing the clock will effectively skew the minimum data valid window. As indicated in Figure 2, as long as the data bus transitions outside of the receiver's minimum data valid window, safe data capture is ensured.

### Determining the Clock/Data Relationship

To determine the required clock skew, you create a timing diagram illustrating the clock/data relationship of a read operation for the QDR device based on the actual read timing diagrams acquired directly from the memory device's data sheet. To be more descriptive of the signal relationships in the diagram, name the read data clock signal *C_Mem* and the data bus signal *Q_Mem* to reflect the signals as they appear at the pins of the memory device.




| Row | | Name | Formula | Min | Max | Margin | Comment |
|---|---|---|---|---|---|---|---|
| 19 | V | tPCBdata | 0.75 | 0.75 | 0.75 | | PCB Trace delay from Memory device to FPGA for data bus |
| 20 | V | tPCBclock | 0.75 | 0.75 | 0.75 | | PCB Trace delay from Memory device to FPGA for read clock |
| 21 | M | mOFFSET_IN | | -0.5 | -0.5 | | Xilinx Offset Constraint Measurement (rising edge) |
| 22 | V | mOFFSET_IN_F | (mOFFSET_IN-(period/2)) | -4.259 | -4.259 | | Xilinx Offset Constraint Measurement (falling edge) |
| 23 | M | mDVW | | 2.759 | 2.759 | | Valid Data Window Measurement |
| 24 | M | mPeriod | | 7.519 | 7.519 | | Period Measurement for Read Data Clock |

*Figure 4 – Clock/data timing diagram of QDR read operation*

To model those same signals as they appear at the pins of the FPGA, after their accumulated flight path delay from the QDR device, create the signals *C_FPGA* and *Q_FPGA*. Figure 3 is a block diagram illustrating the signal path relationships just described.

The resulting QDR memory read diagram is displayed in Figure 4. The data bus represents the transition period necessary for all elements of the data bus between valid data words. The PCB trace delay accumulated by both data and clock is represented with separate variables: *tPCBdata* for the delay associated with the data signal and *tPCBclock* for the delay associated with the clock. This allows you to easily vary the values and see the effect on the design results.

### Creating Constraints with TimingDesigner

Knowing the timing relationship of an external clock and its associated data as it arrives at the pins of the FPGA provides a unique advantage for accurate data capture and design success. The Xilinx timing constraint *OFFSET* is used along with its associated keywords to provide initial timing information to ISE, so that proper placement of data capture elements and their associated routing delays will be adequate for the design. As illustrated in Figure 5, TimingDesigner provides direct dynamic access to any measurement within a timing diagram for generation of a place and route constraint file (UCF).

For this design example, you need to measure the offset for the data (*Q_FPGA*) and clock (*C_FPGA*) signals, and the duration of the valid data window at the pins of the FPGA controller. This can be done directly from the timing diagram using TimingDesigner measurements, as indicated in Figure 4. You'll also need the read data clock period measurement.

### Generating Constraint Information

TimingDesigner's Dynamic Text dialog box offers a way to reference timing diagram measurements from within a vendor's specific timing constraint syntax. Using ISE's *OFFSET* timing constraint syntax, you reference the measured offset values in

the Dynamic Text dialog box to assemble constraints for transfer into the ISE constraints file. The syntax for this design example is illustrated below:

```
OFFSET = IN %mOFFSET_IN.min VALID %mDVW.min ns BEFORE "rd_clk" TIMEGRP RdClkRisingFFs;
OFFSET = IN %mOFFSET_IN_F.min VALID %mDVW.min ns BEFORE "rd_clk" TIMEGRP RdClkFallingFFs;
```

The *VALID* keyword is for specifying the duration of the incoming data valid window, and is used for hold time calculations in ISE. The signal *rd_clk* is the pin name in the design code associated with the *C_FPGA* clock signal in the timing diagram. Notice that two offset specifications must be declared – one for the rising clock edge and one for the falling clock edge – because this is a dual-data rate read operation. Also notice the "%" syntax that indicates dynamic text access of measured values in the timing diagram.

The Dynamic Text dialog box will resolve the dynamically referenced measurements and allow direct transfer of the information into the UCF constraints file. Once the UCF file has been assembled, execute a place and route in the ISE tool set.

**Determining Routing Delays**

For this design example, ISE placed the read data capture registers into the I/O blocks of the Virtex-II Pro devices, because they capture data from the input pads and have a common clock and reset signal. This is a default setting for ISE's mapping process and is appropriate for this design example.

As the I/O blocks have only one routing path for input data signals, the TRACE report includes this data path delay in the setup and hold requirements of the I/O block registers. However, the clock signal has several possible paths from the input pad to the capture register, and this design example uses a path through the DCM element for phase shift control. So you must determine the routing and element delays for the clock path to achieve proper phase shifting of the clock.

A TRACE analysis report is generated in verbose mode to get the needed timing information. This report is limited to 16 paths per constraint (the data bus is 16 bits). Briefly look at the report and make note of the worst-case setup path for the data bus in preparation for import into the timing diagram.

To import the desired TRACE analysis report information (saved as a TWX file) into TimingDesigner, map the worst-case setup path identified earlier to the associated waveform in the diagram (*Q_FPGA*), and then import the information to create variables for the routing and element delays. Mapping the FPGA ports guides TimingDesigner to the desired signal information, and allows for automatic updates of existing variables if successive place and route executions are necessary.

**Visualization at the Capture Register**

After importing the timing results, create another clock signal (*Cin_FPGA*) to represent the clock characteristics at the data capture register. You then add the setup and hold requirements obtained in the TRACE report import as TimingDesigner constraints on the data signal relative to the register clock, as shown in Figure 6.

Notice that the indicated setup and hold margin results from the diagram match the slack values from the initial TRACE timing report, and indicate that the setup paths are failing by about 2 ns, but the hold time paths have more than enough margin. You need to shift the clock so that both the setup and hold time measurements are met with roughly the same margin.

**Take Control of Your Design**

After initial place and route is complete, you can generate a timing report using the TRACE timing analysis tool within ISE, and import that into the timing diagram. This will allow you to determine the actual routing delays so that you can specify the necessary phase shift for the read clock. You then enter the phase shift attribute into ISE, execute a final place and route, and generate a timing report. When complete, you then re-import the timing report to gauge how well the constraints were met.

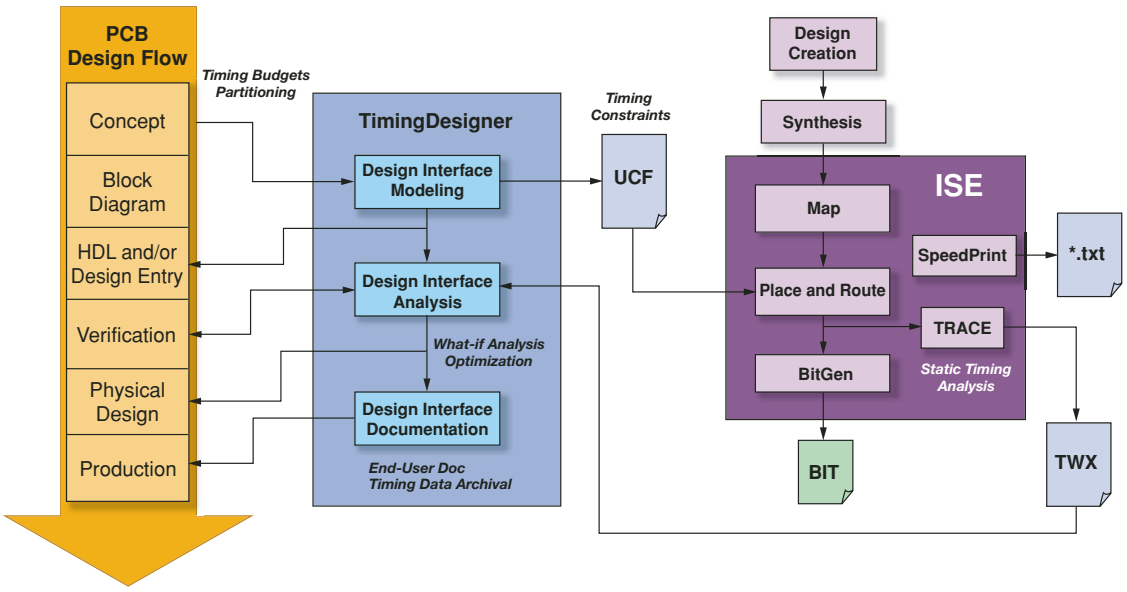



*Figure 5 – TimingDesigner offers an intuitive interface to ISE's design flow.*

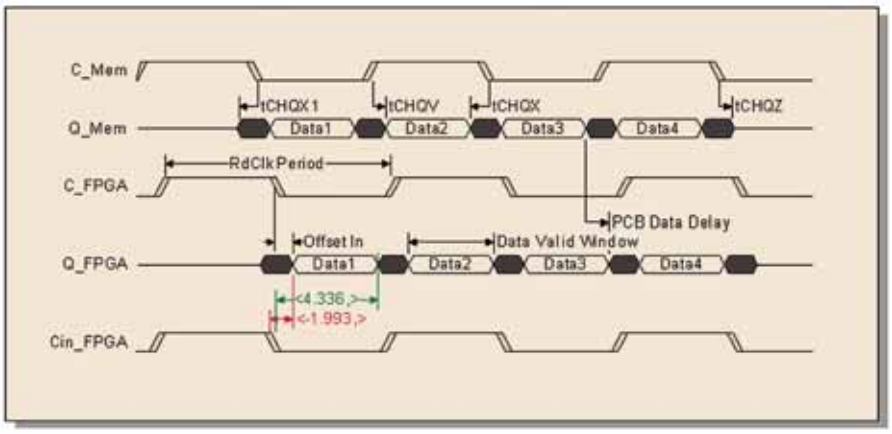



*Figure 6 – Setup and hold of data capture register after initial placement*

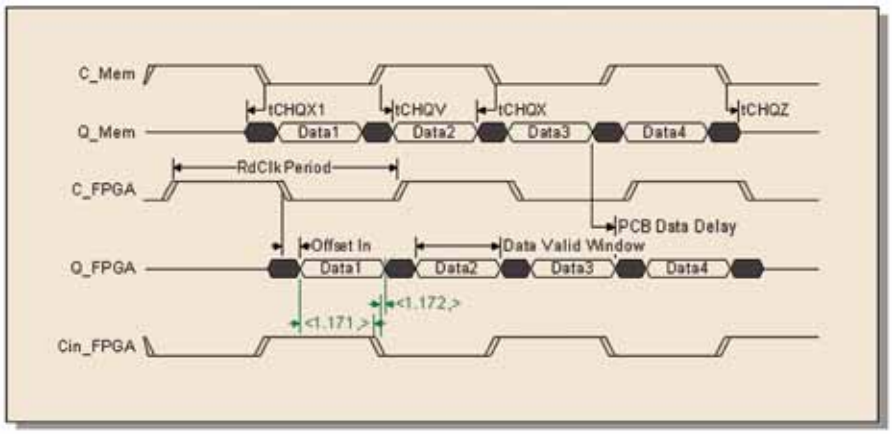



*Figure 7 – Balanced setup and hold of data capture register*

**Making Adjustments**

Using the imported information obtained from the TRACE timing analysis report and the measured values from our timing diagram, you can obtain the attribute value for the necessary DCM phase shift (see sidebar, "Balancing the Data Valid Window"). For this example, the attribute value was determined to be 108, for a shift of 3.165 ns. You then enter this value into the ISE tool flow, and execute a second place and route to shift the clock and properly balance the setup/hold margins.

**Verifying the Results**

Re-importing the new post-place-and-route timing report using the previous import settings will automatically update all of the necessary values, and correctly re-position the register clock signal (*Cin_FPGA*). This is illustrated in Figure 7. Examination of these timing results shows that the setup and hold requirements for a read data capture in the design are now balanced with respect to margin (slack), giving the safest possible result for any unforeseen signal drift.

**Conclusion**

Using TimingDesigner together with Xilinx Virtex-II Pro devices allows optimal safety margins for setup and hold requirements, which are necessary for accurate data exchange with a QDR SRAM memory controller.

By following a design process that combines the use of TimingDesigner timing diagrams and ISE's post-place-and-route timing reports, you can create an accurate analysis of your design's critical timing relationships. Using timing diagrams, you can account for PCB trace delays and other external factors that will affect the signal relationship at the pins of your FPGA device.

ISE's TRACE timing analyzer provides timing reports that give you details on the route delays and constraint requirements of your FGPA device. Together, these tools allow you to accurately capture and exchange critical interface timing information, and allow visual verification that your design will perform as desired.

To learn more about TimingDesigner and the Chronology Division of Forte Design Systems, please visit *www.timingdesigner.com.*

## Balancing the Data Valid Window

You can determine the amount of DCM-generated phase shift needed for the clock signal to balance the data window using the following procedure:

1. Subtract the minimum data valid window for the Virtex-II Pro device from the design's actual data valid window, and divide that result by two. This accounts for the difference between the two valid data windows (DlyDVW).

   DlyDVW = (DVWactual – DVW_VIImin) / 2

2. Subtract the offset measurement made at the pins of the FPGA device from the required setup time for the capture registers, to account for device setup requirements (DlyRelSU).

   DlyRelSU = IOBsu – OFFSET

3. Determine total clock path delay from the TRACE timing report (Xtcd).

   Xtcd = <from TRACE report>

4. Add up the necessary delays (values obtained in 1 and 2 above), and subtract the total clock path delay (value from 3 above).

   Clk_offset = (DlyDVW + DlyRelSU) – Xtcd

5. Finally, determine the correct ISE attribute value to control DCM phase shift with the formula:

   phase shift attribute =
   (Clk_offset/Clk_period)*256

# Celebrating 20 Years of Partnership

## Turning an industry cliché into a successful business model.

*VP of Worldwide Marketing Sandeep Vij in the Xilinx Hall of Patents*

by Xilinx Staff

**"Partnership" might possibly be the most overused word in the high-technology industry. But at Xilinx®, it transcends cliché as a foundation principle behind the company's highly successful business model since its inception.**

**Today, the Xilinx way of thinking reflects a rare mindset about the value of an interconnected ecosystem of like-minded companies and the benefits such an approach can bring to Xilinx, its customers, and to the partners themselves.**

**To say that Xilinx was founded on the Spirit of Partnership is no overstatement. In the original 1984 business plan, the second bullet under the "strategy" section (after the primary strategy point of "maximizing our strength in product architecture and design") articulated the idea to partner with complementary suppliers. The Xilinx founders thought that through an extreme focus on a few core competencies, Xilinx could deliver highly differentiated products and drive technology innovation forward.**

**Most notably at the outset was the need for a manufacturing partner. The founders fundamentally believed that there was no need to fund such a capability in-house – a radical concept in the era of "real men own fabs." (The average price tag for a fab at the time was $300 million, about one-tenth of today's going rate, but still a hefty investment for a startup company in 1984.)**

## ...Programmable logic technology is an excellent means for manufacturers to characterize new processes...

Company founder Bernie Vonderschmitt leveraged past relationships and his solid reputation for fair play to negotiate a manufacturing deal with Japanese giant Seiko, which agreed to allow Xilinx-designed chips to be produced in its fabs. Sealed with only a handshake, Xilinx had its first partner and the industry had a new model – the fabless semiconductor company.

In short order Xilinx signed up another critical partner as its first distributor, because the founders viewed the sales process as they did manufacturing: essential, yes, but not necessarily something the company needed to "own." As with Seiko, the distribution agreement was built on mutual trust and a benefit to both sides – a benefit that could be measured beyond just dollars and cents.

Since then, Xilinx has formed partnerships with a wide range of other suppliers in the semiconductor supply chain, all guided by a consistent principle.

"When we look at forming a partnership, the first question we ask is 'what's in it for you?'" Xilinx CEO Wim Roelandts says, explaining a philosophy that may seem counterintuitive to the traditional approach. "It really should be weighted 51-49 in the partner's favor. They need to get something out of it, as much – if not more – than we do."

Such an approach has helped Xilinx assemble critical components to fill the "solution gap" in its offerings, allowing it to focus on developing the core technology for which it has gained the deserved reputation of a world-class innovator. It has also made Xilinx one of the most respected companies in all of high technology and a favorite among complementary suppliers both large and small.

"For us, a partnership is more than a financial transaction or relationship. It really is about shared goals and ways of thinking," says Sandeep Vij, vice president of worldwide marketing at Xilinx. "Yes, we use partnerships to maintain our own focus and we know it doesn't make sense economically for us to invest in all areas. But it comes down to results – our partnerships are aimed at making breakthroughs that allow our customers to scale new heights."

### Manufacturing Partnerships

Manufacturing still represents the most substantial of the Xilinx partnering strategies, if only because of the cost of today's modern fabrication facility. Xilinx has emerged as one of only a small handful of semiconductor companies that truly "pushes the envelope" when it comes to implementing new technology processes. Recently, it became the first company to ship a production device based on 90 nm process geometries, considered the leading edge of expertise. It also is among the leaders in the use of 300 mm wafers to produce its chips. Both manufacturing achievements allow Xilinx to reach new price/performance milestones with its products and further distance itself from its competitors.

Although such advances are enabled by choosing the right type of company to partner with (for manufacturing, Xilinx partners with UMC™ and IBM™), Xilinx itself is a key contributor to driving manufacturing advancements. The company has more than 100 engineers on-site at UMC, for example, working in tandem with their R&D teams. And because of the "regular" nature of its structure, programmable logic technology is an excellent means for manufacturers to characterize new processes, as UMC has done with its last several generations of new process nodes. But perhaps the secret ingredient is mindset.

"Our partners must share our view on risk-taking. They must be willing to engage in joint risk-taking and be willing to try new things. It is the only way to stay on top of leading-edge technology, to truly innovate," says B.C. Ooi, Xilinx vice president of operations and the man responsible for seeing that Xilinx products stay on the leading edge. "Programmable technology requires the smallest geometries and advanced processes – and we must be a leader in those areas. We are willing to invest to be able to achieve such things as producing the world's largest dies, to be first to 90 nm. And our partners must be, too."

Ooi also points out that because Xilinx is a mission-critical supplier to its customers, its partners must share that sense of urgency and flexibility. "They have to be able to scale with us," he says of an increasingly valuable asset in the cyclical semiconductor industry.

Vincent Tong, vice president of product technology, agrees, adding that the number-one criterion for a Xilinx partner is to be a "technology leader.

"We can't afford to partner with companies that aren't leaders in what they are doing. Three or four years ago, when it came to manufacturing, you could kind of throw a design over the wall. Today we need to be engaged tightly with our partners to drive technology forward. We have more than 80 process engineers and we don't even own a fab," he says, underscoring the commitment level of Xilinx even in areas in which it chooses to partner.

Through its partnership strategy in manufacturing, Xilinx is already pushing into areas beyond the current state-of-the-art, including joint development work in 75 and 65 nm process geometries.

### The Link to the Customer

As with manufacturing, Xilinx made the decision early on that it would work with partners to sell and distribute its products (notably, field support of those products was always viewed as a critical internal function).

"It was a decision borne out of necessity and practicality," explains Vice President of Sales Steve Haynes, who's been with the company for nearly 20 years. "We knew that as a company we needed to focus on what we do best – design, technology, innovation. We needed a ready-made channel to

Today, Xilinx counts some 250 complementary technology and service providers in its "ecosystem" of companies that help it deliver the most robust solutions in the industry.

get our technology in the hands of the customers. There were, and still are, firms that bring an expertise and reach that we couldn't or didn't want to develop ourselves."

Today Xilinx uses a network of close to 30 partners to deliver its products to customers around the world. Some are broadline distributors who sell complementary technology to round out the use of programmable logic. Others are regional or vertical market specialists. In most cases, Xilinx is the most significant product line they represent, and in all cases the relationship is based on mutual trust and shared values.

"When a customer looks at a rep [resentative], they are looking at Xilinx. We have to be on the same page in all facets of the relationship. We have to know them as well as we know ourselves," says Haynes.

Haynes and his team meet regularly with sales partners to align their goals and strategies, and make sure the company's products are being represented consistently with the "Xilinx Way."

The formula is surely working, as Xilinx sales and customer satisfaction metrics show. But it's a constantly evolving process, as Haynes well knows. "Good partnerships evolve. Our channel looks a lot different than it did 20 years ago. It's like being in a marriage – you have to work at it."

### Comprehensive Solutions

The design and use of programmable logic has become an increasingly complex process. In the early days of Xilinx, third-party design tools were just coming to market as the EDA industry took shape, and commercial IP cores were almost non-existent. Today, they, along with a set of other capabilities, are essential to developing multi-million gate, multi-function systems on chip (SoCs). Thus, the Xilinx partnership model has expanded significantly to include technology partners who can round out the core offering.

"Today's markets call for a complete solution, which includes the FPGA and a full set of components and tools," says Senior Manager of Strategic Relationships Jasbinder Bhoot, who oversees all of the partnership programs at Xilinx. "Xilinx has been successfully delivering for years the best FPGA products in the industry. Now, together with our partners, we have a focused emphasis on providing comprehensive solutions to our customers. We seek out and collaborate with best-in-class companies to complement our product offerings with EDA tools, IP, design services, reference designs and manufacturing kits."

Xilinx partners must share our sense of business integrity and win-win philosophy. "We are fairly selective in who we work with. Yes, they must bring a best-of-breed offering, and yes, it must make economic sense for both sides. But these are the companies with whom we will be on the front lines with our customers, so we have to be in synch on many different levels," explains Bhoot.

Bhoot and his team use well-defined metrics to gauge how effective each and every partnership is for Xilinx and its customers. And they are constantly on the lookout for new areas to develop partnerships and make Xilinx technology more accessible and complete.

Today, Xilinx counts some 250 complementary technology and service providers in its "ecosystem" of companies that help it deliver the most robust solutions in the industry. From industry leaders such as IBM™, Cadence™, Mentor Graphics®, Synopsys™, Synplicity™ and Wind River™ to specialized experts in key areas, Xilinx partnerships provide maximum breadth and depth of technology offerings.

*Jasbinder Bhoot, Senior Manager of Strategic Relationships*

Among the areas in which Xilinx partners are:

- **Intellectual property cores.** Xilinx works closely with independent third-party core developers to produce a broad selection of industry-standard solutions, deemed AllianceCORE™, dedicated for use in and optimized for Xilinx programmable logic.

- **Design tools.** Xilinx's AllianceEDA partners are among the tool leaders for each step in the design process, including such critical areas as high-level design, synthesis, logic verification, and complete PCB design. Xilinx and its partners develop the methodologies and tool flows that help make programmable logic users productive and well positioned to take full advantage of Xilinx devices.

- **Design services.** Xperts are a global network of certified design experts trained to take full advantage of the features present in the Xilinx Platform FPGAs, software, and IP cores. When customers need design expertise, they can access a sophisticated resource database and quickly identify design consultants in their own regions.

- **Embedded development tools.** Xilinx AllianceEmbedded partners are experts in the field of embedded systems – inclusive of compiler, debugger, IDE, and trace/visibility tools – as well as RTOS requirements. They support the Xilinx commitment to deliver high-performance, cost-effective embedded processor-based solutions.

- **Reference designs.** Xilinx teams up with industry-leading semiconductor vendors to develop reference designs for accelerating its customers' product and system time to market.

### The Spirit of Partnership

Xilinx has developed a successful formula for delivering a steady stream of innovation and technology firsts to the market in its first 20 years. Its partnership approach is an essential element of that formula, and although no one intends to alter the basic strategy, the technology industry mandates that change is a constant.

"Xilinx is in a much different position as a company now than when we first started 20 years ago," Roelandts says. "Resource-wise we could consider doing more things ourselves. But we know that the key to our success has been our focus. That has enabled our innovation, which is why we are a leader. In that respect, partnerships make even more sense, especially as the world gets more complicated. Our challenge is to continue to develop the right set of relationships with companies that share our vision and make sure we all derive a benefit. We will not waver on the basic principles that guide our partnership strategy, but we will keep the process dynamic to address new market needs and conditions."

So don't expect to see Xilinx building its own fab in the next 20 years. But thanks to is unique Spirit of Partnership, it's a safe bet that Xilinx and its partners will continue to set the standard for innovation and best business practices in the semiconductor industry. Σ

Xilinx has developed a successful formula for delivering a steady stream of innovation and technology firsts to the market in its first 20 years.

# Author! Author!

## Turn your terrific idea into a technical tome through the Xcell Publishing Alliance.

by Clive "Max" Maxfield
President
TechBites Interactive
*max@techbites.com*

When reading a technical book, you may sometimes find yourself muttering, "Ha! The author is a complete and utter idiot! I could have done a better job than that!"

Or you may be working on an interesting project – or have just developed a novel solution to some problem – when you suddenly think, "I could write a really cool book about this!"

That initial flush of enthusiasm soon cools, however, when you start to mull over things in a little more detail, realizing that you don't actually have a clue where to start. Is there a market for such a book? What should it cover? Who will create the graphics? How will you find a publisher for your masterpiece?

Given these imponderables, it usually doesn't take long before you've talked yourself out of becoming an author. This is unfortunate, because there may be a lot of potential readers out there who could really benefit from your expertise. And of course, being known as an author can only enhance your career prospects and make your family and friends very proud.

## The Xcell Publishing Alliance is designed to help you take your magnum opus from initial concept, through planning and implementation, all the way to publication, fame, and glory.

To assist authors-to-be (like yourself?), Xilinx® has created an innovative new program called the Xcell Publishing Alliance. The program is designed to help you take your magnum opus from initial concept, through planning and implementation, all the way to publication, fame, and glory.

In fact, as I pen these words, I'm basking in the glow of having just received the author copies of my latest book, "The Design Warrior's Guide to FPGAs: Devices, Tools, and Flows." This book was made possible in large part by Xilinx and Mentor Graphics®, both of whom provided me with access to a wide variety of experts and information sources. Thus, in this article I thought I'd walk you through the process of creating a book – using "The Design Warrior's Guide" as an example – and then discuss what Xilinx can do to help you create your very own tour de force.

### Topical Questions

The very first thing you have to decide on is a topic. What exactly would you like to write about? There's little point in spending vast amounts of precious time and effort creating a book that no one actually wants to read.

I've been fortunate in this regard, because I've tended to write books on topics that interest me and that I would like to read myself. Happily, the folks who read my books seem to enjoy them also. For example, my very first effort – "Bebop to the Boolean Boogie: An Unconventional Guide to Electronics" – was recently re-released in its second edition due to popular demand.

Looking back, I realized that most of my tomes were introductory in nature, so the time seemed right to focus on a particular topic in more depth. FPGAs have become phenomenally powerful and sophisticated in recent years. Today's FPGA devices can be used to implement extremely large and complex functions that previously could be realized only using ASICs, and thus an increasing number of design engineers are starting to use the little rascals. When I began to look around, however, there seemed to be a dearth of useful material in this arena.

### Readership to Shore

Once you've decided on your topic, you will have to flesh it out into an outline, and eventually grow it into a full-blown proposed contents list. An integral part of this process is to decide who your audience is, because the type of information you will cover will typically vary depending on whether you are talking to engineering gurus or novices.

I personally dislike reading books that talk down to me as though I am the village idiot. But equally, I'm less than enamored by books that try to impress me with the author's brilliance, or those that require me to return to college just to wend my weary way through the first chapter.

In the case of "The Design Warrior's Guide to FPGAs," I wanted to address the needs of an unusually wide audience, including students, sales and marketing professionals in the EDA arena, and full-blown engineers. For this reason, I devoted the first section of the book to fundamental concepts such as:

- What are FPGAs and why are they of interest?
- Underlying technologies, such as anti-fuses, flash memory, and SRAM cells
- Alternative architectures and concepts
- Different programming techniques
- Who are the various players in the FPGA space?

I felt that this background information would be useful to less-technical readers, while techno-weenies could leap directly into the more challenging middle section of the book. Among many other topics, this section takes an in-depth look at:

- FPGA versus ASIC design styles
- Schematic-based design flows (yes, they are still used to support legacy designs)
- HDL-based design flows
- Silicon virtual prototyping for FPGAs
- C/C++-based design flows
- DSP-based design flows
- Embedded processor-based design flows
- Modular and incremental design
- High-speed design
- Migrating ASIC designs to FPGAs, and vice versa

One thing I recall from my college days is that despite having scores of textbooks, I was unable to find the fact I was looking for in any of them. For this reason, "The Design Warrior's Guide" includes a third section boasting a host of peripheral topics, including:

- Choosing the right device
- Gigabit serial interfaces
- Reconfigurable computing
- Field programmable node arrays (FPNAs)
- Independent design tools
- Creating a design flow based on open-source tools

Just looking at the above lists makes my eyes water, because I well remember the research and effort that went into fleshing

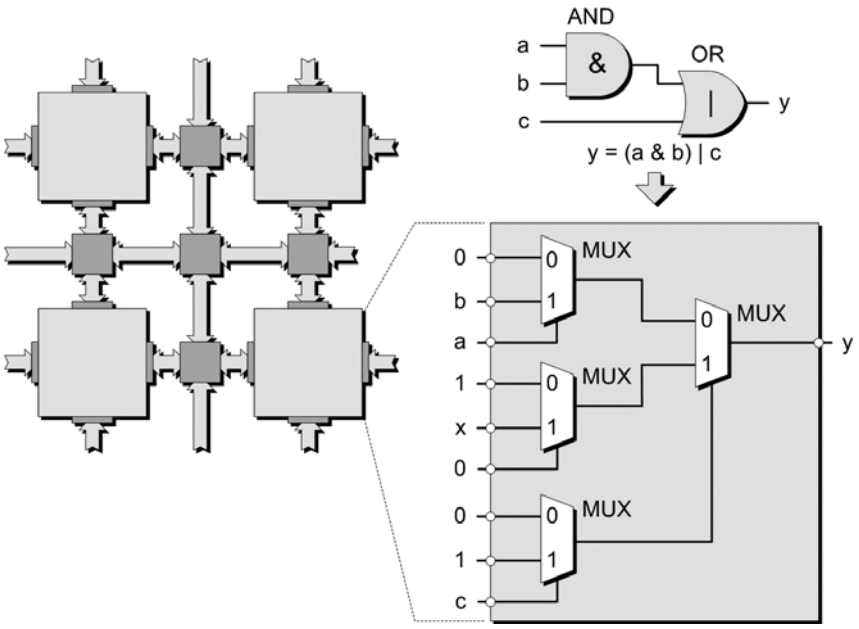



*Figure 1 – An example figure created in Visio.*

out these topics when I finally got around to writing the book.

### In Style

Yet another point to ponder before you leap into the fray is the style you intend to use. To a large extent this will be determined by your target audience, but it will also be strongly influenced by your personality.

I soon become disgruntled when reading boring books. Unfortunately, this seems to cover the vast majority of technical books out there (although there are a few notable exceptions). It's almost as though someone sent out a memo saying, "Whatever you do, don't make engineering books interesting – otherwise all sorts of folks might decide to read them."

Fortunately, I didn't receive this memo, so I don't feel bound to follow it. As a simple rule of thumb, I tend to write the sort of book that I personally would like to read. Thus, I use a somewhat informal, chatty style – much like this article – and I also like to include nuggets of trivia and tidbits of information, such as "Where did this come from?" or "Why do we do things this way rather than that?"

Furthermore, in my later books I've started to include little pronunciation notes as sidebar items for technical acronyms and terms. I do this because if you mispronounce a word when talking to someone in the industry, you immediately brand yourself as an outsider. Some engineers have been known to scoff at me for this, but I've received many e-mails from less-technical readers that say, "Only the other day you saved me from a potentially embarrassing situation."

### Yes, There's More

At some stage, of course, you are going to have to actually put pen to paper (or fingers to keyboard). Writing a book-length project isn't easy. You may start off full of vim and enthusiasm, but as you approach the middle of the project things seem to slow down and become increasingly difficult – much like wading through molasses. And then, suddenly, you'll find that you've crested the brow of the hill and are racing down the other side towards the finish line.

Another consideration is creating graphics. I personally go by the adage that "a picture is worth a thousand words," so I festoon my writings with graphics wherever I can. For technical books and white papers, I tend to use line art created in Microsoft™ Visio™, an incredibly useful and easy-to-use tool. As an example, consider a sample illustration from "The Design Warrior's Guide" (Figure 1), which reflects a simple multiplexer-based FPGA architecture. Logic gates are not usually shown with gray fills and shadows, but I think it looks more interesting – and it's my book.

Another consideration is finding someone to help you proofread and copyedit your work and to offer suggestions as to presentation and style. Although many editors can discourse for hours on the many and varied uses of the apostrophe, the loathsome split infinitive, and parallel sentence structure, actually finding one who has a clue what you are talking about technology-wise can be somewhat taxing.

And last, but certainly not least, once you've finally finished, you will need to find a publisher who can take your masterpiece, lay it out, print it, distribute it, and promote it far and wide.

### The Xcell Publishing Alliance

All of the above may seem a little overwhelming at first, but things aren't as daunting as they appear. The idea behind the Xcell Publishing Alliance is to help folks write books on FPGA-related topics, where said "folks" may range from individual engineers to small engineering houses to large Xilinx partner companies.

One key point to note is that it is not the purpose of the Xcell Publishing Alliance program to flood the market with Xilinx-centric books. The guys and gals at Xilinx aren't stupid, and they know that the last thing engineers need is for technical books to mutate into marketing brochures halfway through. The only criteria are for the books to address FPGA-related issues and to be generally useful to a wide audience.

How can Xilinx help you create the book of your dreams? Well, in the case of partner companies, Xilinx can put you in touch with authors (like me) who can write the book on your behalf; they can help you decide on the contents; and they can facilitate your relationship with a publisher.

## . . . After your book rolls off the printing presses, you could pen an article on it for the *Xcell Journal*.

For individual authors or small engineering houses who wish to write and publish a book, the Xcell Publishing Alliance can help in the following ways:

- Consulting with you on the topic, outline, and eventual contents list
- Providing access to the appropriate technical and marketing employees, both at Xilinx and their partner companies
- Facilitating access to industry insiders such as technical experts, editors, and analysts
- Helping to create any figures, diagrams, and cover art
- Proofreading and copyediting your manuscript (or finding someone who can)
- Providing access to a publishing house
- Helping you market, promote, and publicize your book

Xilinx has recently committed to a partnership with Elsevier, whom I'm informed is the largest English language publisher in the world.

And as for to helping you market, promote, and publicize your book, Xilinx can be a powerhouse working on your behalf. For example, in addition to their inside contacts at the various industry magazines, soon after your book rolls off the printing presses, you could pen an article on it for the *Xcell Journal*.

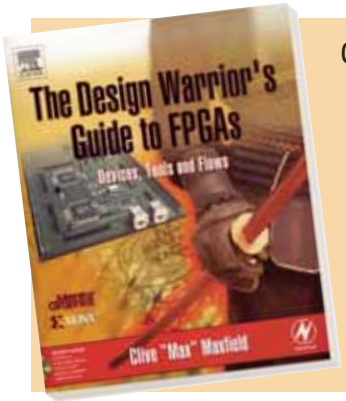
After all, since it is published quarterly in five languages, distributed in 114 countries, and directly targeted to more than 50,000 programmable digital design users, the *Xcell Journal* can carry a huge amount of weight. And let's not forget the advantages of any publicity for yourself and your company (see the info blurb on my company, for example).

### Conclusion

Writing a book is much harder than most people imagine, and there will be moments that you rue the day you ever had the idea for such a project. It's also true that the chances of ever getting rich from a technical book are laughably slight.

On the bright side, however, the feeling you get when holding the first copy of your baby when it comes back from the publisher is absolutely fantastic. Be prepared to run around with a silly "aw shucks" grin on your face. And don't discount the fact that having a book in print is a wonderful way to market yourself, open doors, reinforce your career, and enhance your future employment prospects.

Embarking on a project like this is a major task, but the chances of your success will be far greater if you have the support of the Xcell Publishing Alliance. For more information about this exciting new program, please send an e-mail to *xcell@xilinx.com*.




Clive "Max" Maxfield is president of TechBites Interactive Inc. (*www.techbites.com*). A marketing consultancy, TechBites specializes in servicing high-technology companies, ranging from small "Fred-in-a-shed" startups all the way to the "big boys" in EDA. The services provided by TechBites include logo creation, corporate/product branding, marketing plans, web design and development, collateral design and production, technical and creative writing, technical translation, and digitizing.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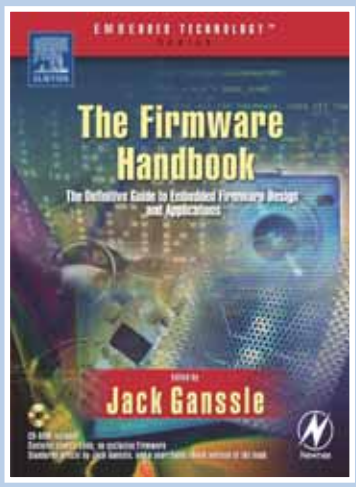


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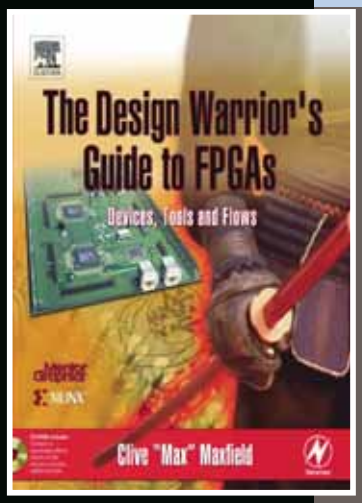


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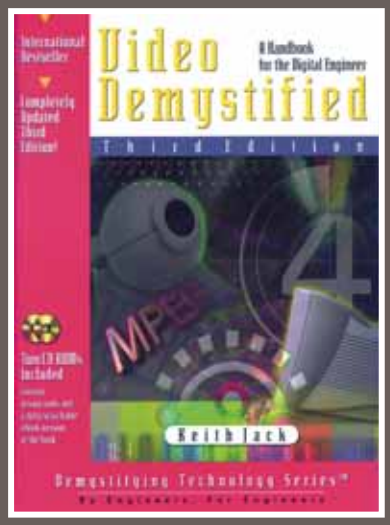


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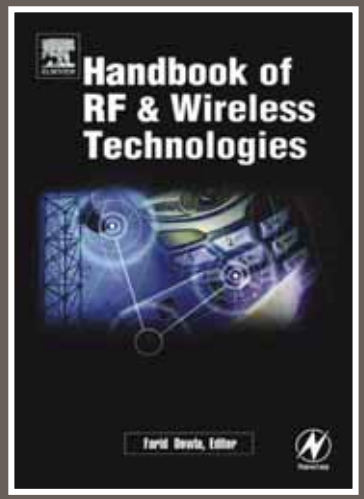


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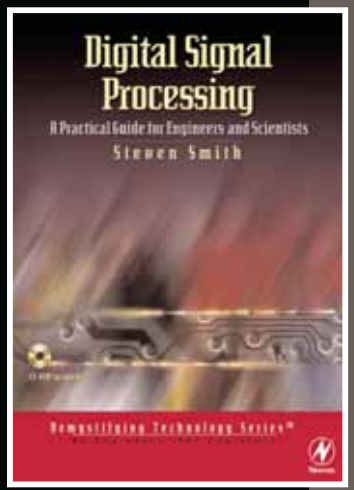


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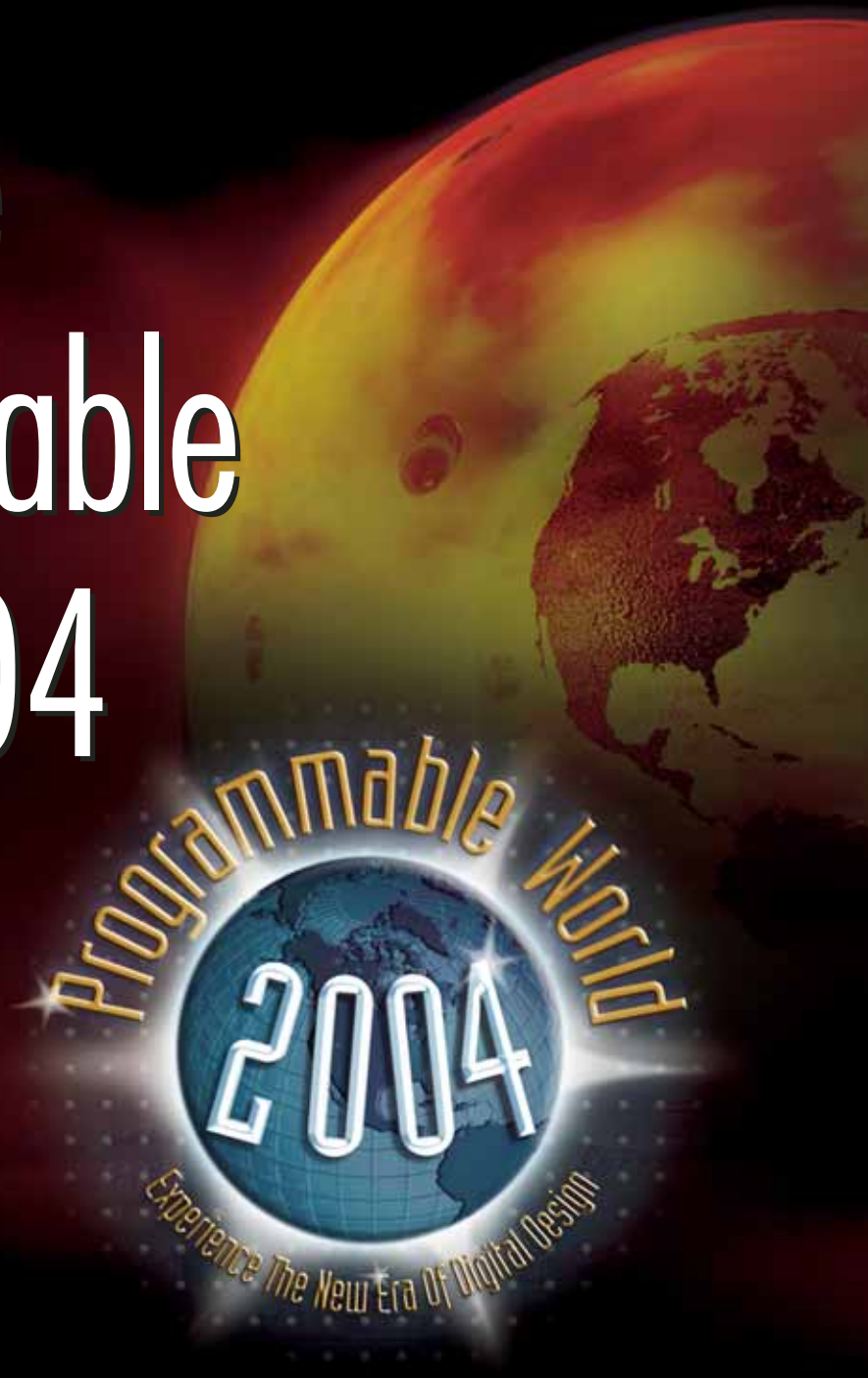
# Experience Programmable World 2004

## Xilinx and fellow technology leaders offer one-day workshops to showcase the "state-of-the-art" in programmable digital design.




by Jim Cairns
Director of Corporate Solutions Marketing
Xilinx, Inc.
*jim.cairns@xilinx.com*

Making your products and subsystems competitive in performance, features, and cost requires constant awareness of new leading-edge programmable technologies. Making your designing as productive as possible requires steady learning of leading application solutions, tools, and techniques.

Beginning this October (see Table 1), Programmable World 2004 brings together thousands of engineers and system architects for an action-packed day of learning and networking around the most exciting new programmable technology in the world: the Virtex-4™ solution from Xilinx®.

Last year's Programmable World 2003 workshops packed new technical content from the vast Xilinx partner ecosystem and its leading expert users into a highly productive day-long training event in 20 cities around the world. Xilinx and fellow industry leaders such as Agilent™, IBM™, Intel™, The MathWorks, Mentor Graphics®, Texas Instruments™, and Wind River™ led engineers through workshop tracks covering DSP, embedded processing, high-speed connectivity, and system logic design.

Workshop attendees received a 556-page workbook filled with direction on key solutions to the most pressing design and verification issues facing hardware engineers, ASIC designers, system engineers and architects, and embedded software developers in getting products to market quickly and competitively.

At Programmable World 2004, Xilinx and its partners will showcase the new Virtex-4 solution in each of four digital "domains" – DSP, processor, connectivity, and logic – with a full-day track dedicated to each.

**DSP Track**

Learn about the amazing price reductions, power improvements, and performance acceleration that Virtex-4 solutions will bring to your video and digital communications applications and algorithms. See the latest enhancements to the industry's easiest end-to-end tool flow for designing, verifying, and debugging, from design entry in MathWorks tools to real-time Xilinx hardware in-the-loop.

This track will include reference designs and other real-life examples to help you get the most out of your communications and video designs.

**Connectivity Track**

Preview the newest high-speed serial technology that enables data rates as high as 11 Gbps with impeccable signal integrity chip-to-chip, across backplanes and even box-to-box. Share techniques for minimizing error rates, board cost, and system cost for your connectivity applications. Anticipate and understand potential signal integrity issues early in your design cycle and apply the latest streamlined methodologies to proactively prevent signal integrity issues.

This track will cover the use of Xilinx RocketIO™ models in high-speed PCB simulations as well as analyzing and simulating GHz signal paths for via- and surface-mounted components in PCB design. You'll see how signal integrity analysis is used to reduce overshoot, ringing, cross talk, timing margins, inter-symbol interference, and radiated emissions. Instructors will show HSPICE™ correlation, eye diagrams, signal pre-emphasis, and S-parameter connector models using simulation tools. You'll also work on predicting performance using a combination of electromagnetic field simulation and circuit and system simulation, and on optimization of interconnect and transitions used for high-performance PCB designs.

**Processor Track**

Walk through the comprehensive Virtex-4 embedded processing solution, from the PicoBlaze™ 8-bit microcontroller reference design, 32-bit MicroBlaze™ soft processor implementation, the enhanced on-chip PowerPC™ processor, and the UltraController solution that uses the embedded PowerPC. Delve into design tools from Wind River, MontaVista Software™, and Mentor Graphics/ATI and learn about the latest Virtex-4 RTOS support.

Mix and match the latest combinations of:

- Virtex-4 silicon architecture
- 32-bit RISC processor cores and peripherals
- Third-party RTOS support
- Intelligent design tools
- Integrated hardware/software debug platforms
- Development boards
- Reference designs
- Board support packages
- Design services
- Technical support from Xilinx and industry-leading partners

See how the newest Xilinx Embedded Development Kit with the Platform Studio IDE automates and accelerates the development process, allowing hardware and software designers alike to design, debug, and boot a processor platform easily in timeframes never before possible.

**Logic Track**

See how the latest design and debug tools from Xilinx, Synplicity™, Mentor Graphics, and Agilent help leverage the blazing fast Virtex-4 logic fabric and features. Learn the latest design techniques for the fastest performance, shortest design times, and lowest project costs. Work through FPGA physical synthesis for highest quality of results; high-speed memory interface design using real-time debug to slash verification times; and bench-top testing to verify signals in real time.

You'll experience much beyond the intensive workshop sessions at Programmable World 2004. Technical demos will show how Virtex-4 solutions and partner offerings can help you solve real-world engineering problems faster and easier.

"Ask the Experts" opportunities bring you together with leading technologists from Xilinx to discuss how their products, services, and applications support can address your specific architecture and engineering challenges. Interactive networking sessions will allow you to share best practices and trends with other engineers and architects.

**Conclusion**

Programmable World 2004 packs hundreds of new programmable digital innovations and techniques into a single day of intense learning that you will not want to miss. For more information, or to register for the Programmable World workshop in a location near you, visit *www.xilinx.com/pw2004/*.

**Programmable World 2004 Dates and Locations**

**October 2004**
Paris, France
Munich, Germany
Milan, Italy
Stockholm, Sweden
San Diego, California
San Jose, California

**November 2004**
Raleigh, North Carolina
Dallas, Texas
Boston, Massachusetts
Baltimore, Maryland
Orlando, Florida
Chicago, Illinois
Ottawa, Ontario, Canada
Shanghai, China
Shenzhen, China
Hsinchu, Taiwan
Seoul, Korea
Yokohama, Japan
Osaka, Japan

**December 2004**
Tel Aviv, Israel

*Table 1 – Programmable World 2004 schedule*

# Managing Partial Dynamic Reconfiguration in Virtex-II Pro FPGAs

## Adapted methodology and tools available from RECONF2 make partial dynamic reconfiguration in Xilinx devices a reality.

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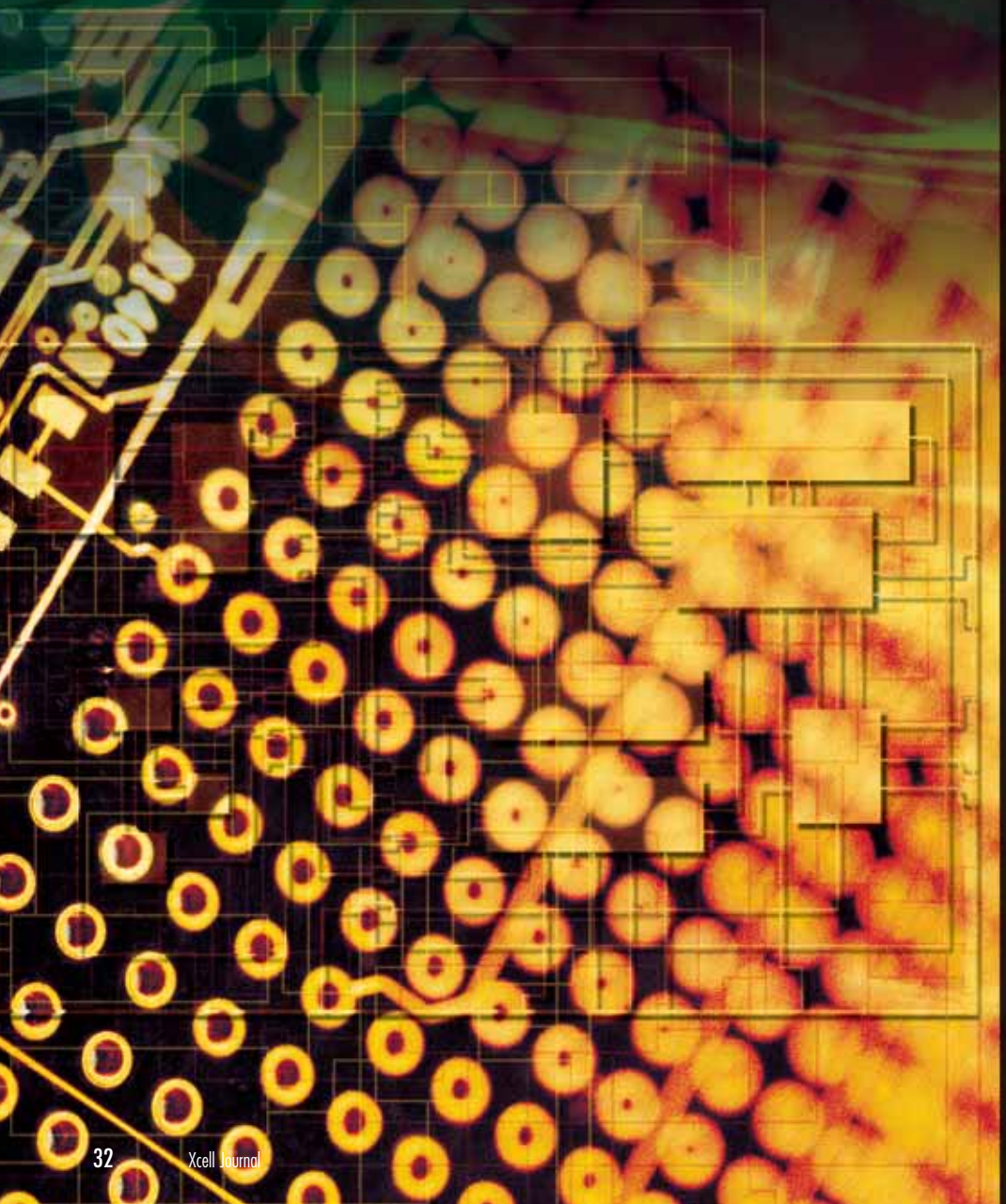


This article reports the work currently being done in the European Union (EU) R&D project "Design Methodology and Environment for Dynamic RECONFigurable FPGA," whose short name is RECONF2 (see *www.cordis.lu/en/home.htm* for more details on EU-funded research projects). Targeting designers, this project aims to ease the access to changing the configuration of part of an FPGA design while the circuit is running. Xilinx® already offers this technology, but the lack of a simple methodology and appropriate tools is a major limitation to its implementation.

Therefore, the partners of this project (both academic and industrial) defined a complete and validated methodology, along with the required front-end tools, addressing the complete design flow: dynamic partitioning, control of the dynamic behavior, and dynamic verifications. Tools covering all of the specifics related to dynamic reconfiguration are fully compatible with the standard design flow (a clear request from our industrial partners). Also, neither the methodology nor the tools are dedicated to a particular application domain and are thus suitable for any embedded application, especially real-time ones.

Many advantages exist in using this technique, including the ability to change the behavior of a system while it still running to adapt it to an externally changing environment.

In this article, two of the project partners – MBDA France and Deltatec – will demonstrate these benefits through a short presentation of the methodological flow, as well as citing one example.

### Adapted Design Flow

The goal of the RECONF2 project is to build a set of partial bitstreams representing different features, so as to partially reconfigure the FPGA with those bitstreams when needed under the control of the FPGA itself or through the use of an external controller. To reduce the difficulty in managing such a dynamically reconfigured application and to provide a reliable implementation, the academic partners developed a set of tools and associated methodologies addressing the following issues:

- Automatic or manual partitioning of a conventional design
- Specification of the dynamic constraints
- Verification of the dynamic implementation through dynamic simulations at major steps of the design flow
- Automatic generation of the configuration controller core for VHDL or C implementation
- Dynamic floorplanning management and guidelines for modular back-end implementation

The resulting adapted design flow shown in Figure 1 is based on both standard and RECONF2-specific CAD tools. The input of the design flow is a conventional VHDL static description of the application. You can also provide multiple descriptions of a given VHDL entity to enable dynamic switching between two architectures sharing the same interfaces and area on the FPGA.

We have enriched the "classical" design flow with three major steps: partitioning of the design code, verification of the dynamic behavior, and generation of the configuration controller.

### Partitioning the Application

Based on the knowledge of the design architecture and the use of each sub-module in time, you can indicate which part of the feature to dynamically load, and under which conditions. You can also specify data management constraints to retain some internal states of the application after unloading and reloading the corresponding dynamic module.

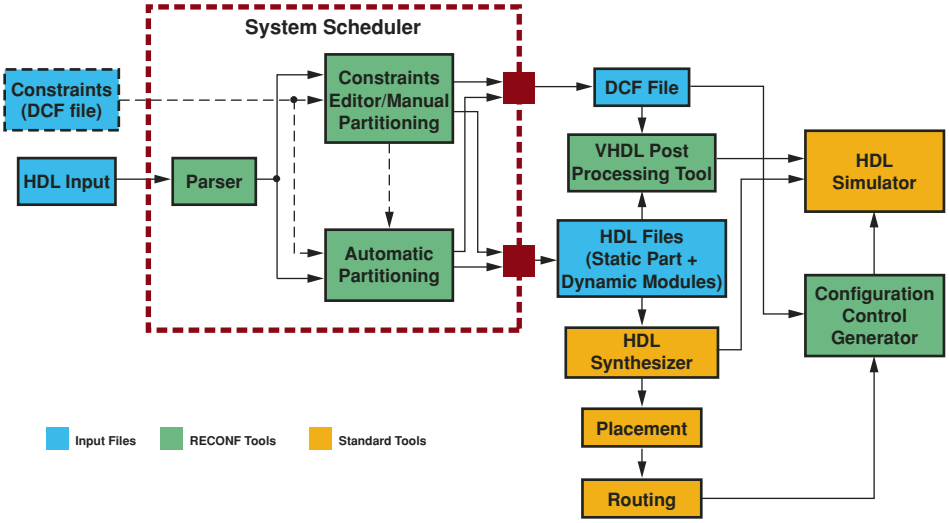



*Figure 1 – Adapted design flow*

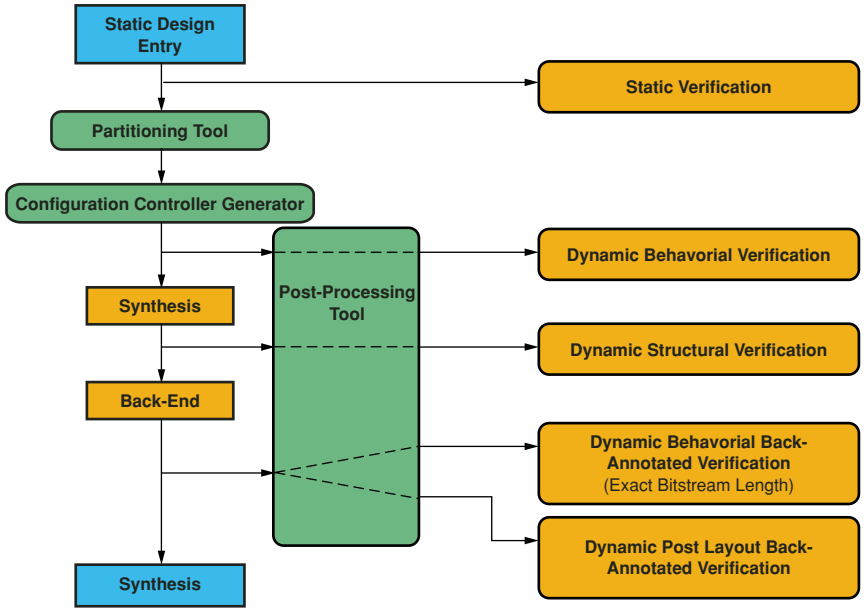



*Figure 2 – Dynamic verification flow*

By identifying portions of the design in the code at instance level, VHDL process, or VHDL assignment, you can make the dynamic specification flexible and independent of the application coding style. The outputs of this partitioning task are:

- A VHDL entity and architecture set corresponding to an identified dynamic module and containing the relevant HDL code.
- A dynamic constraint file (.dcf) that contains the definition of each module (in terms of content) and the associated constraints for loading and unloading them. You can also specify dynamic relations between two dynamic modules, making them share the same area of the FPGA or by declaring them mutually exclusive in time.
- A VHDL entity and architecture set corresponding to the static part of the final implementation. This part includes all primary design instances on which no dynamic constraints have been applied. These instances will remain permanently inside the FPGA.

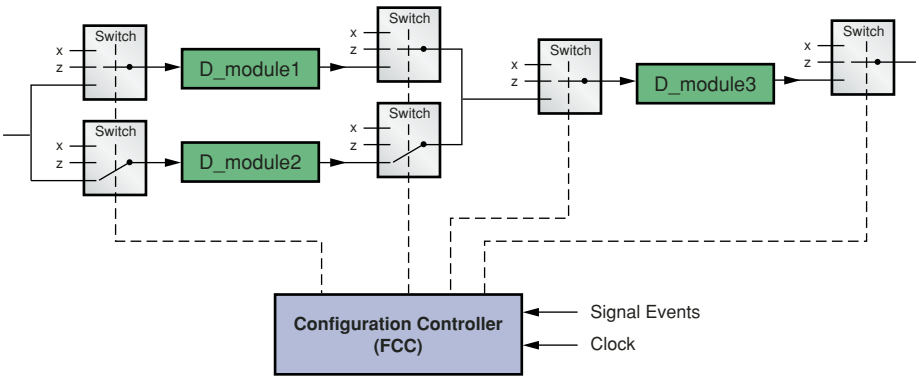



*Figure 3 – Switch insertion for dynamic simulation*

**Verifying the Dynamic Implementation**

Implementing such dynamic reconfiguration mechanisms must be checked – and with standard simulation tools. To be able to do so, we had to adapt the classical verification flow to verify the dynamic behavior of the design and the coherence of dynamic constraints applied to and the use of the design during simulation (Figure 2). As a result, you can perform this dynamic verification with behavioral, post-synthesis, or post-layout VHDL netlists.

Simply enter a partitioned database to the post-processing tool, which generates an equivalent VHDL description of the dynamic design that you can simulate under standard static VHDL simulators. The unloading of each dynamic module is modeled by a wrapper that isolates the inputs and outputs of each dynamic module from the rest of the design according to relevant dynamic constraints (Figure 3). When a dynamic module is not present inside the device, its outputs generate "X" or "Z" states to the rest of the design.

The post-processing tool also automatically generates two VHDL configuration controller cores:

- The functional configuration controller (FCC) is used during dynamic behavioral simulation. The FCC controls isolation switches by detecting events inside the application, according to the .dcf constraints. To assist with the verification process, the FCC can also issue different warnings each time a dynamic module is requested in violation of exclusivity rules defined in the .dcf.
- The physical configuration controller (PCC) is a synthesizable version of the FCC and is mapped as a static part of the FPGA. As with the FCC, it detects the loading and unloading conditions according to the .dcf and manages the dynamic reconfiguration of the FPGA by reading bistreams in storage memories and rewriting the FPGA's configuration. The PCC also provides an interface to monitor the reconfiguration process for hardware debugging purposes.

For dynamic behavioral verification, you can enter an estimation of the bitstream lengths into the post-processing tool to take into account reconfiguration delays. After layout, you can replace them with accurate ones, while a back-annotated VHDL netlist can replace the VHDL-partitioned code to obtain accurate vital verifications.

**Placement and Routing**

You would synthesize the static part of the design and the VHDL code of each dynamic module separately to obtain separate electronic design interchange format (EDIF) netlists. You can then use the Xilinx modular back-end flow to place and route each module and to generate the associated bitstream, resulting in a typical floor plan (shown in Figure 4).

In the scope of the RECONF2 project, the industrial partners extensively tested these tools and methodologies through various applications, including video processing, complex state machines, automatically adaptive portable equipment, and fault-tolerant aerospace applications.

## An Implementation Example

Figure 5 shows a complete video effects console architecture using two effects generators (A and B); their outputs feed a transition mixer. Channel A feeds the live output while the operator sets up the second (Channel B) for a new effect, visible through the preview output.

When ready, the operator selects a transition scheme such as "wipe" or "fade" and swaps the live and preview outputs (typically using a T-bar). Effects generators select their inputs from several external video sources or feedback channels implemented in an SDRAM-based frame store.

The challenging part of this application is the building of a RECONF2-based implementation with uninterrupted outputs.

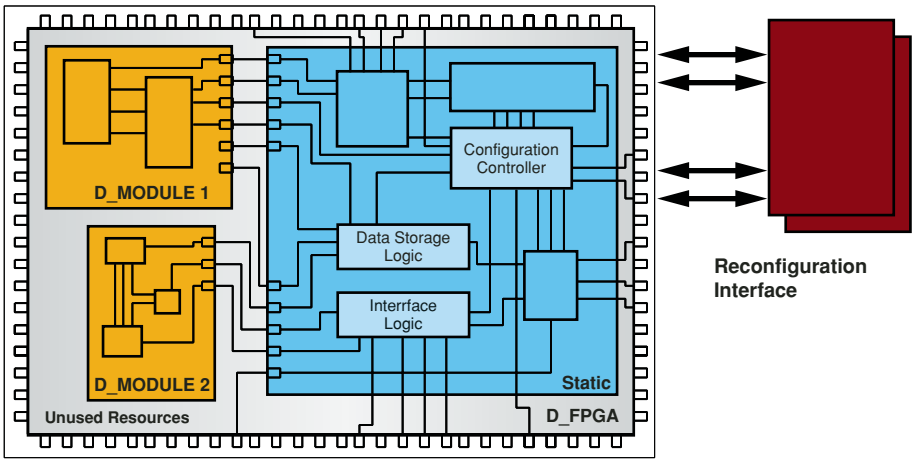



*Figure 4 -Typical layout*

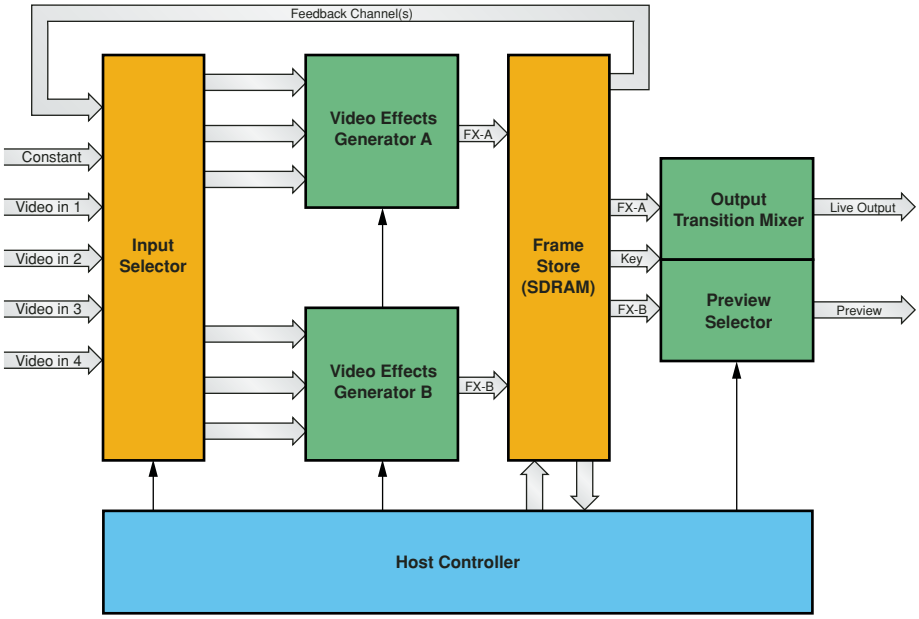



*Figure 5 – Video effects console*

We designed a dedicated hardware development platform based on a Virtex-II™ XC2V3000 device with a 64-bit PCI adapter board (see Figure 6), taking into account the specific constraints of the Xilinx partial reconfiguration design flow and providing the required flexibility for an evaluation environment.

### Dynamic Architecture of the Design

Based on Figure 5, we partitioned the design into three processing modules (sharing the same footprint), applied in sequence to every field/frame. Each effects generator also supports a collection of effects, possibly changing from frame to frame, implemented as separate exclusive modules.

1. Compute effects A output
2. Compute effects B output
3. Compute mixer output

This implies saving intermediate and final results, while reconfiguring the module for the next operation. An SDRAM memory pool provides this buffering capability. Also, the processing must run at three times the video speed so that total processing time remains unchanged.

In a reconfigurable design, there is always a trade-off between the processing time and reconfiguration time of a dynamic module. This means that one dynamic module must process a "significant amount" of data before being replaced to meet the real-time constraints.

In our real-time video application, a common data unit is one field/frame to be processed in 20/40 ms – compared with the ~25 ms needed to configure the full XC2V3000 device via its Select Map interface.

Figure 8 shows the architecture used for dynamically reconfigurable processing, while Figure 7 shows the corresponding layout. We instantiated field buffers on the input and output side. Although the SDI input/output pixel rate is 13.5 MHz, pixel processing can run much faster, at 50 MHz, for instance.

Figure 9 shows typical phase alternating line (PAL)-interlaced video timing. Without buffering, dynamic module reconfiguration must occur within the blanking interval (1.57 ms), while processing (at 13.5 MHz) fills the entire active video interval (18.43 ms).

With the field buffers and 50 MHz pro-

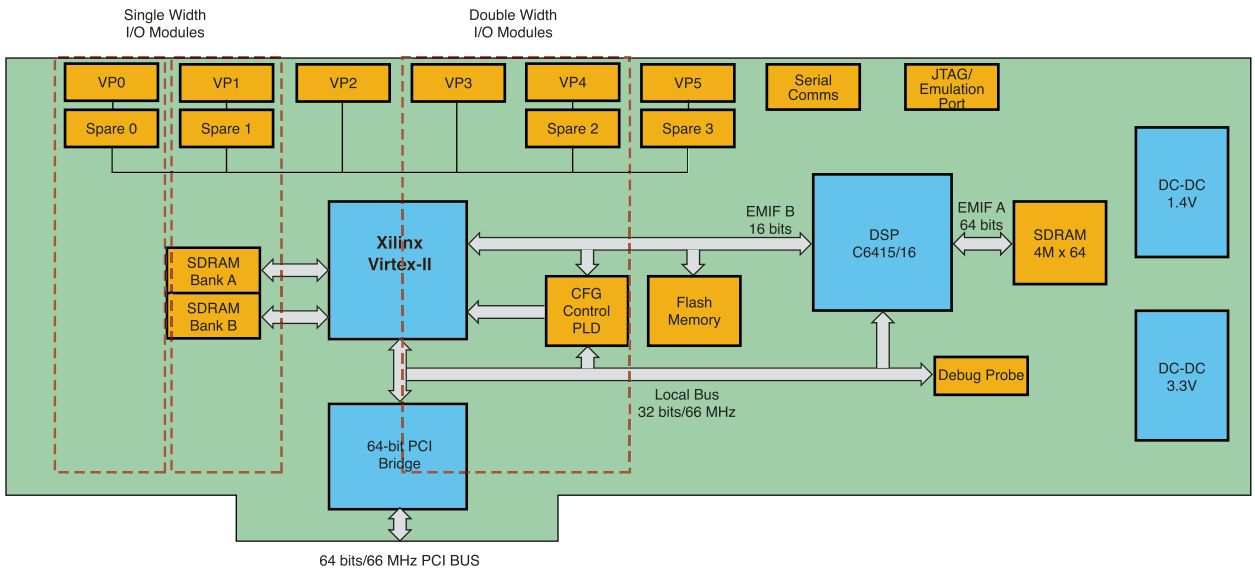



*Figure 6 – Hardware development platform*

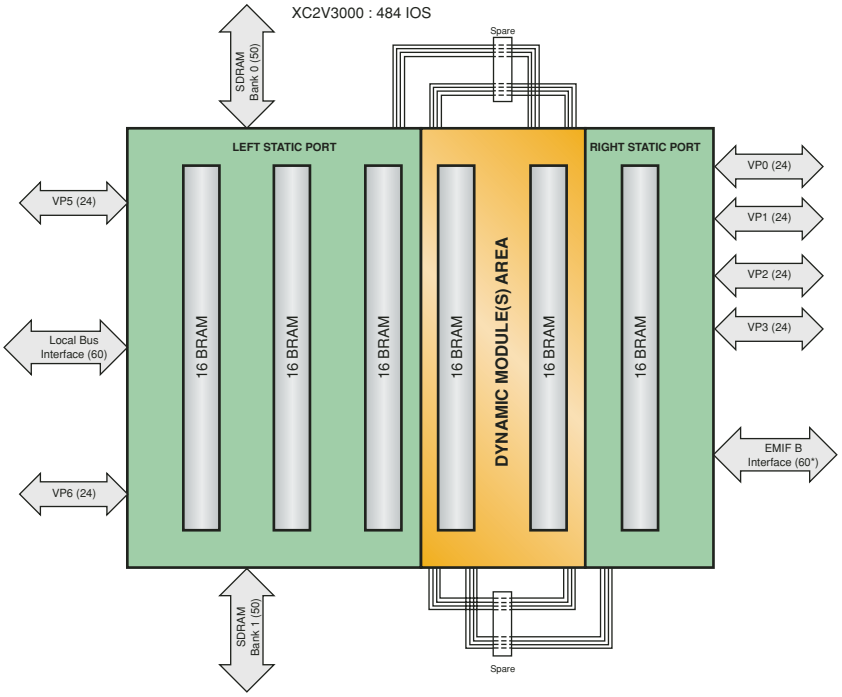



*Figure 7 – XC2V3000 layout with VP 0.3 as generic video input ports, VP 5 and 6 as generic video output ports*

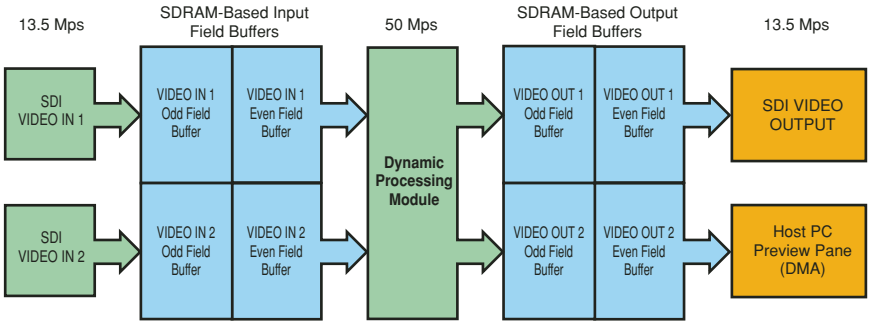



*Figure 8 – Field double buffering*

cessing, we obtain timing (as in Figure 9B) with 16 ms allocated to reconfiguration and 4 ms for video processing. Two processing steps can be interleaved (as in Figure 9C): 6 ms remain available for dynamic module reconfiguration.

Applying the same reasoning to frame buffering (2 fields → 40 ms), we double the available time for reconfiguration (as in Figure 9D).

The RECONF2 tools and flow will help investigate these trade-offs.

Figure 10 shows the manual partitioning tool GUI, with the input VHDL design in the left window. The partitioned design appears in the right window. A simple drag-and-drop assigns chunks of logic to one particular module. Scheduling constraints (load/unload and frame) are then entered for each module.

Our design lends itself by nature to manual partitioning: one particular effect is always applied to a full video field/frame. Each effect is implemented as an independent dynamic module.

The configuration controller generator analyzes the partitioned design and its constraint file to produce:

- An FCC for simulation purposes
- A PCC for implementation in hardware (VDHL code) or software (C code)

To evaluate as many features of the tools as possible, we chose to support both configuration controller schemes and tested them on our hardware development platform. Nonetheless, our preferred solution was a software configuration under the control of an on-board DSP because of critical real-time issues; we optimized the platform accordingly.

The Xilinx Partial Reconfiguration Design Flow, based on the modular design available within ISE 6.2 software, is used to produce one global bitstream for startup and several partial bitstreams for the different dynamic modules. See Xilinx application note XAPP290 for a detailed description of this flow.

One benefit of the RECONF2 approach for this video console application is obvious: we can add as many new video effects (such as video enhancement filters), fitting in the reserved dynamic module space without the need for additional FPGA resources. This effectively increases the "functional density" of the FPGA.

A further increase comes from executing several processing steps (effects A, B, and transition) within a single video field/frame duration, as previously explained. This is very similar to the traditional "parallel vs. serial" arithmetic trade-off, and makes a great deal of sense given the extraordinary progression of FPGA performance over the last several years.

One less obvious advantage exists thanks to this partitioned approach: simultaneously supporting all of the functions results in unneeded complexity that may adversely impact the design's performance. The operating model is also more complex for the control application. Smaller, dedicated modules will run faster and need less operating parameters, making them more manageable objects.

In the example presented, we see the reconfiguration time as a clear limitation. This time is directly linked to the dynamic module size and to other FPGA parameters. We are currently trying to implement a dynamic module "caching": two dynamic modules slots are reserved, and one module is reloaded while the other is processing, and vice versa. Reconfiguration time is completely "hidden," at the cost of FPGA space.

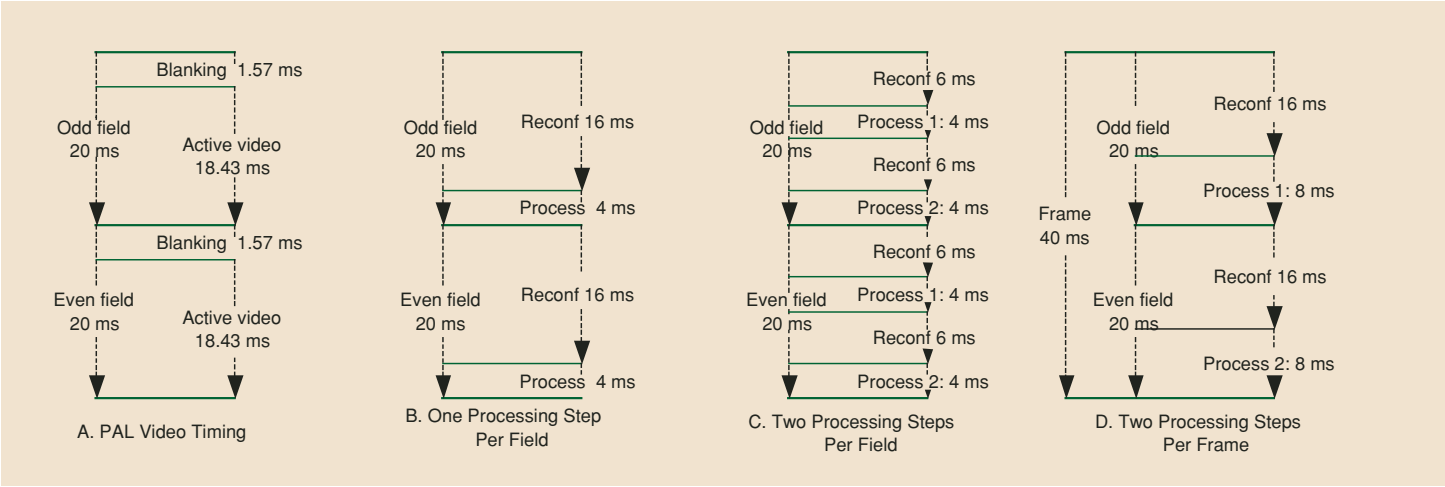



*Figure 9 – Video frame and operations timing*

## Conclusion

Most of the specific tasks required by partial dynamic reconfiguration are handled by a complete methodology and associated tools. These have been designed to be fully compatible with the ones used for classic Xilinx FPGA implementation. Furthermore, our approach is usable with any technology compatible with dynamic re-configuration.

The academic partners developed the method and tools according to specifications that take into account industrial constraints, such as:

- Compatibility with standard tools such as simulators and synthesizers
- Usability with any technology compatible with dynamic re-configuration, in particular with Xilinx technology and back-end tools

The academic partners have made the tools and methods available to the industrial partners, who are currently testing them for complex circuit design, thus ensuring ease of use and efficiency.

MBDA France will then be able to take full advantage of this technology in deeply embedded on-board computers, characterized by small volumes and low power dissipation.

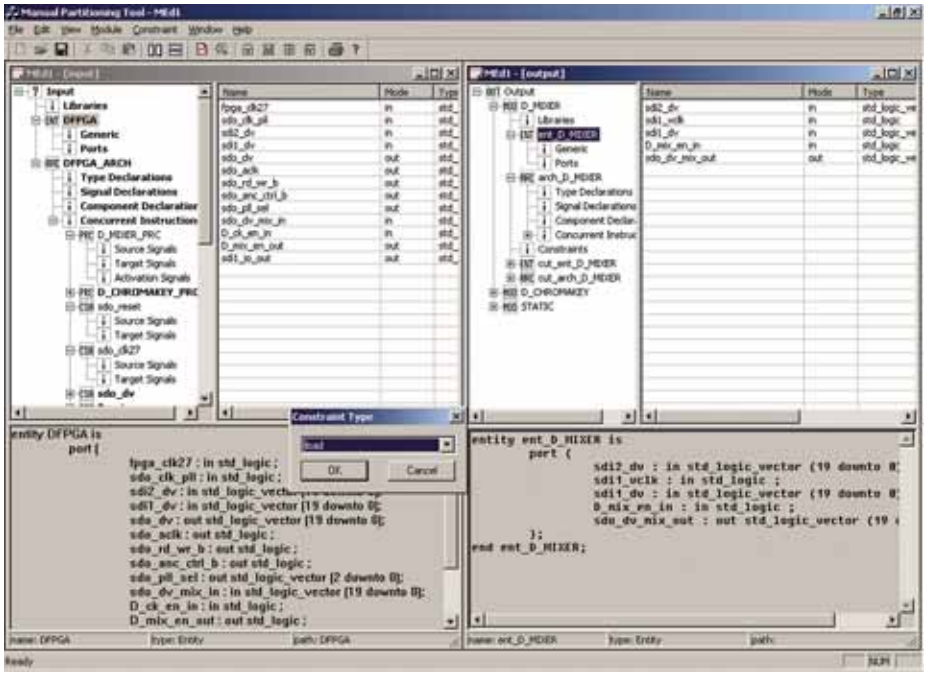


*Figure 10 – Manual partitioning tool*

Deltatec develops digital imaging products for multimedia, industrial/medical, and professional broadcast markets. Upcoming video applications will require more and more versatility. High-definition television (HDTV) applications must tackle multiple formats (resolution, frame rate, interlaced/progressive scan) as well as converge with the computer graphics world. Simultaneous support for all existing formats/functions may rapidly become a nightmare and even hamper feasibility because of cost or performance issues (for example, an HDTV pixel rate of 75 MHz, almost a six-fold increase over standard digital television [SDTV]).

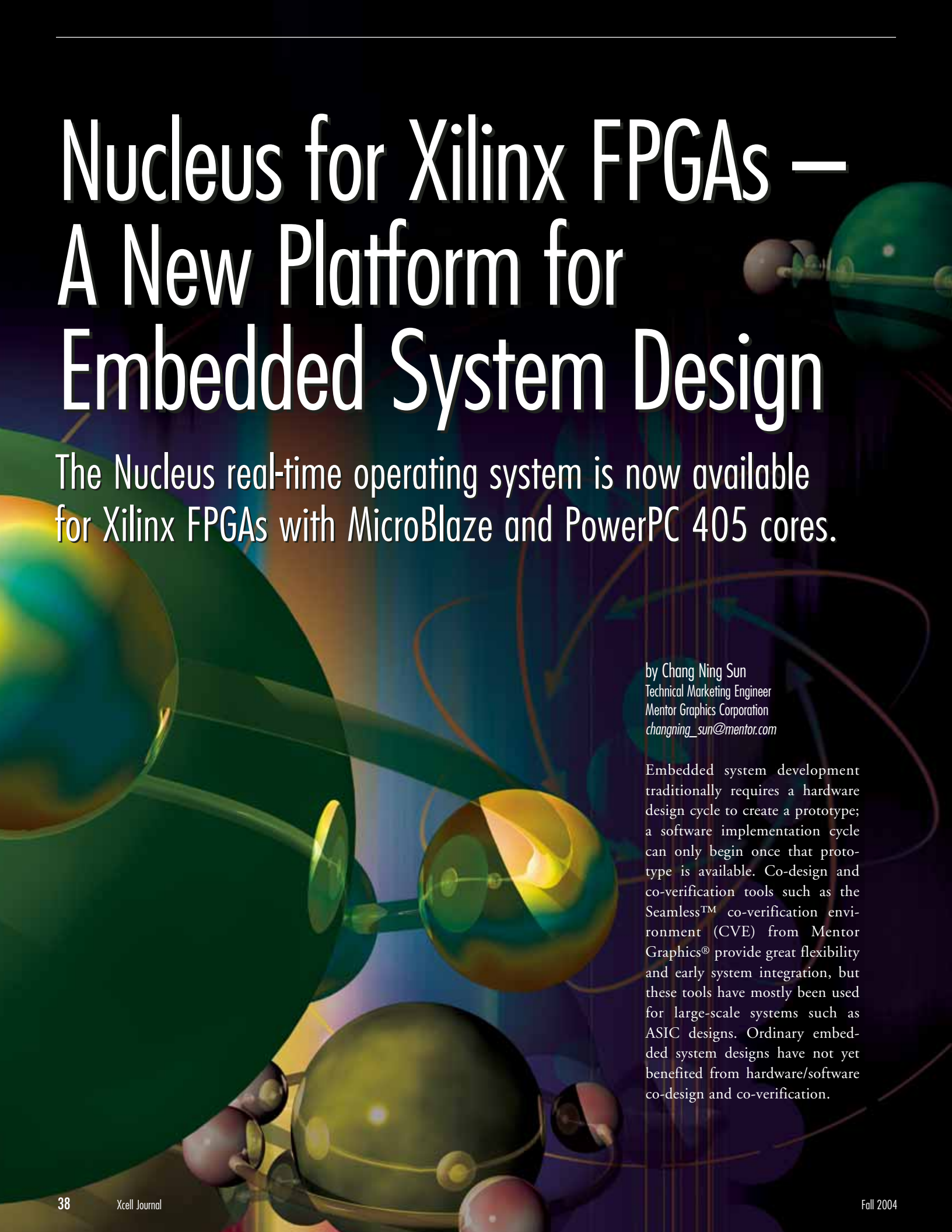
The RECONF2 tools and methodology circumvent these problems, as only the required function blocks are loaded at any particular instant:

- FPGA size (and cost) remains acceptable, while keeping the same integration level.
- Smaller, less generic, optimized function modules more easily reach performance goals.

At this time, the methodology and tools are accessible to our project partners and could be extended to other third parties, such as tool suppliers for distribution and support in order to enable a larger access to this technology. For more information on the RECONF2 project, visit *www.reconf.org*.

# Nucleus for Xilinx FPGAs — A New Platform for Embedded System Design

## The Nucleus real-time operating system is now available for Xilinx FPGAs with MicroBlaze and PowerPC 405 cores.



by Chang Ning Sun
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Embedded system development traditionally requires a hardware design cycle to create a prototype; a software implementation cycle can only begin once that prototype is available. Co-design and co-verification tools such as the Seamless™ co-verification environment (CVE) from Mentor Graphics® provide great flexibility and early system integration, but these tools have mostly been used for large-scale systems such as ASIC designs. Ordinary embedded system designs have not yet benefited from hardware/software co-design and co-verification.

In recent years, innovations in FPGA technology have shifted the use of these devices from supporting logic to forming a central part of the embedded system. With their high logic density and high performance, modern FPGAs allow you to implement almost an entire embedded hardware system in a single FPGA device.

Xilinx® Spartan-II™, Spartan-3™, and Virtex-II™ Platform FPGAs (combined with the MicroBlaze™ soft processor core) and Virtex-II Pro™ Platform FPGAs (combined with the PowerPC™ 405 hard processor core) offer new hardware platforms and facilitate new methodologies in embedded system design.

The Nucleus™ real-time operating system (RTOS) from Accelerated Technology (Mentor Graphics' Embedded Systems Division) fully supports Xilinx Platform FPGAs. Together with our FPGA design flow and Seamless CVE tools, the Nucleus RTOS is a complete hardware/software co-design and co-verification environment.

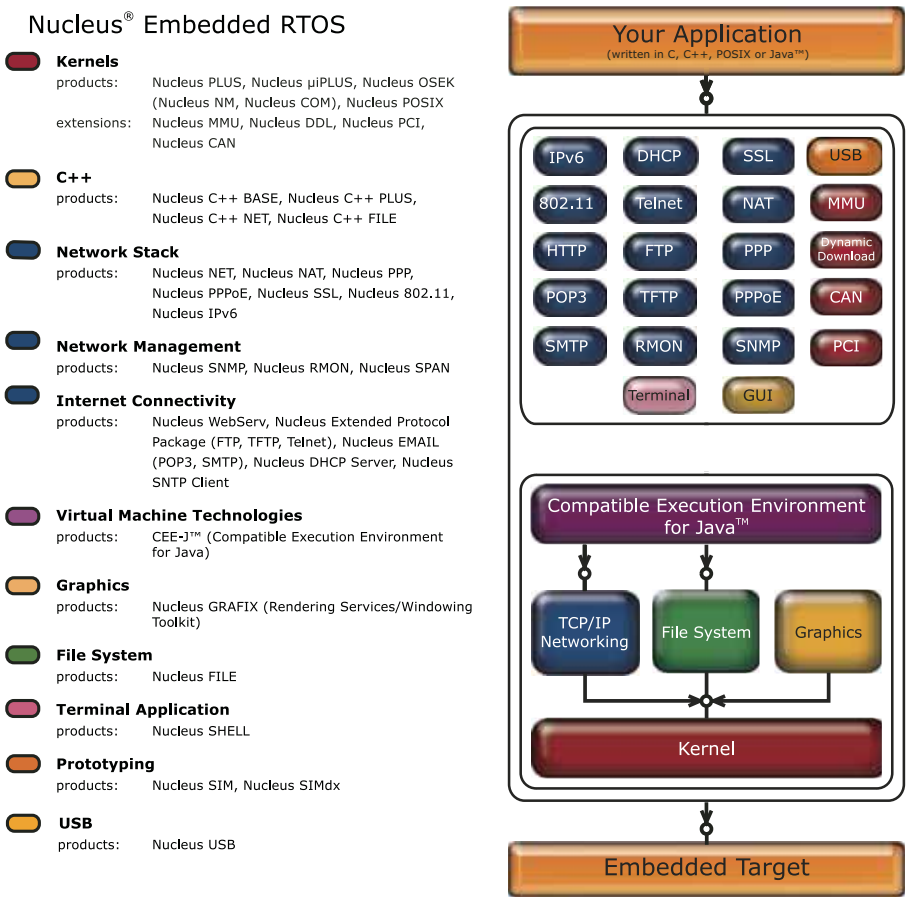


*Figure 1 - Nucleus system architecture*

## The Nucleus RTOS

Very few embedded software developers start their development on bare hardware; most choose a commercial embedded RTOS like Nucleus as the base environment and develop their applications on top of the operating system.

Generally, an RTOS provides a multi-tasking kernel and middleware components such as a TCP/IP stack, file system, or USB stack. Application developers build their application software by using the system services provided by the RTOS kernel and the middleware components. A number of commercial RTOSs are available: some have hard real-time kernels, some have extensive middleware support, and some have good development tools. The Nucleus RTOS has all of these features from a single vendor.

Figure 1 shows the Nucleus system architecture.

### Nucleus PLUS

Nucleus PLUS, a fully preemptive and scalable kernel suitable for hard real-time applications, is designed specifically for embedded systems. It has a very small footprint; the kernel itself can be as small as 15-20 kB.

All Nucleus kernel functions are provided as libraries, so only the required kernel functionality is linked with the application code in the final image. Nucleus PLUS provides complete multi-tasking kernel functions, including task management, inter-task communication, inter-task synchronization, memory management (MMU), and timer management. Recently, we added a dynamic download library (DDL) into Nucleus PLUS to allow dynamic downloading and allocation of system modules.

### Nucleus Middleware

The middleware available for an RTOS has become an important factor when selecting a commercial RTOS for a particular application. As embedded applications become increasingly more complicated, application developers find implementing industry standards like TCP/IP, WiFi, USB, and MPEG more difficult. These standards are often implemented as middleware components and provided together with the RTOS.

The Nucleus RTOS has an extensive library of middleware support (Table 1), which covers every vertical market of the embedded industry. Nucleus NET utilizes a zero-copy mechanism for transferring data between user memory space and the TCP/IP stack, which significantly improves data transmission efficiency and reduces dynamic memory allocation.

Nucleus software fully supports the POSIX standard for software portability. POSIX interface libraries are available for all Nucleus middleware components.

### Nucleus Device Drivers

The Nucleus RTOS has an extensive list of off-the-shelf device drivers. When you select a new hardware IP or peripheral to use in your design, the driver source code may already be available. If not, a driver template lets you easily develop a functional driver.

## Nucleus software has proven to be a robust RTOS and has been widely used in every vertical market of the embedded industry…

Mentor Graphics will continue to add device drivers to the Nucleus library for new hardware IP blocks for Xilinx FPGAs as well as for third parties, such as its own IP Division.

**Nucleus Development Tools**

The Nucleus RTOS has the most integrated development environment (IDE) in the industry. Combined with our Microtec compiler tools, the codelab embedded development environment (EDE) and XRAY debuggers provide a complete software design flow, from compilation to debugging.

Our C/C++ source-level debuggers support both run-mode and freeze mode debugging with complete Nucleus kernel awareness. The XRAY debugger supports both homogeneous and heterogeneous multi-core debugging, and a wide range of processors and DSPs.

In addition to the Microtec compilers, the EDE, IDE, and debuggers are also integrated with many third-party compiler tools such as GNU.

For system-on-chip (SoC) users, integration of the Nucleus RTOS and XRAY debugger with other products in the Mentor Graphics lineup (such as Seamless CVE for hardware/software co-verification) offer a complete hardware/software co-design and co-verification platform.

**Royalty-Free with Source Code**

The royalty-free with source code business model of the Nucleus RTOS, combined with the high scalability and small footprint architecture, provides great value to customers developing large-volume products such as cell phones, PDAs, and cameras. A single up-front license fee covers all production rights for a single product using Nucleus software, with no additional royalty fees and no need to track shipment numbers.

Nucleus software has proven to be a robust RTOS and has been widely used in every vertical market of the embedded industry, including consumer electronics, telecom, defense/aerospace, automotive, and telematics.

| Nucleus Product | Function |
|---|---|
| Nucleus NET | Complete embedded TCP/IP stack |
| Nucleus Extended Protocols | Telnet, FTP, TFTP, Embedded Shell |
| Nucleus SNMP version 1,2,3 | Network management protocols |
| Nucleus RMON (1-9 groups) | Network remote monitoring protocols |
| Nucleus Residential Gateway | NET, PPP, PPPoE, DHCP server |
| Nucleus WebServ | Embedded HTTPD web server |
| Nucleus EMAIL | POP3 and SMTP |
| Nucleus FILE | MS DOS compatible file system |
| Nucleus GRAFIX | Graphics-rendering engine with windowing toolkit |
| Nucleus USB | Complete USB stack for USB specifications 1.1, 2.0, and OTG |
| Nucleus 802.11 STA (WiFi) | 802.11b and 802.11g protocol stack |
| Nucleus IPv6 | IP version 6 protocol stack |
| CEE-J Java VM for Nucleus | CLDC, MIDP, Embedded Java, and Personal Java |

*Table 1 - Primary Nucleus middleware components*

**Nucleus for Xilinx FPGAs**

The scalable and configurable nature of Nucleus products, combined with the flexibility and versatility of FPGAs, provides great potential for hardware/software co-design, co-verification, and early integration of your software and hardware projects.

**Nucleus for MicroBlaze**

The MicroBlaze soft processor core features a Harvard-style RISC architecture with 32-bit instruction and data buses. A MicroBlaze soft core can be programmed into Spartan-II, Spartan-3, or Virtex-II Platform FPGAs.

Nucleus software fully supports the Xilinx MicroBlaze soft processor core with GNU compiler tool and GDB debugger.

**Nucleus for Virtex-II Pro FPGAs/PowerPC 405**

Many embedded system developers are already familiar with the PowerPC 405 processor. Xilinx Virtex-II Pro FPGAs provide fully configurable hardware platforms with the PowerPC 405 hard processor core.

Nucleus software fully supports Virtex-II Pro FPGAs with the PowerPC 405 hard core, providing a Microtec PowerPC compiler and XRAY kernel-aware debugger, as well as GNU compiler tools and GDB debugger.

**FPGA Reference Design for Nucleus Software**

To give embedded system developers a quick start with Nucleus software for Xilinx FPGAs, we worked with Xilinx and Memec™ Insight to develop reference designs for running Nucleus software. Each reference design is a sample FPGA hardware configuration based on a Memec Insight FPGA development board.

You can build and implement all of the reference designs into the FPGA device by

using Xilinx EDK and ISE software. For each reference design, we provide a Limited Version (LV) of our Nucleus software, including the Nucleus PLUS kernel and the relevant middleware (such as Nucleus NET) to help you evaluate Nucleus software with the FPGA.

The LV version of Nucleus software functions exactly the same as a full version, but is provided as binary only and runs for a limited time. Currently, we have FPGA reference designs for the following Memec Insight boards:

- Spartan-IIE LC MicroBlaze development board
- Spartan-3 LC MicroBlaze development board
- Spartan-3 MB MicroBlaze development board
- Virtex-II MB MicroBlaze development board
- Virtex-II Pro PowerPC development board

We have also created a website (*www.acceleratedtechnology.com/xilinx*) to support Nucleus software for Xilinx FPGAs, where you can download FPGA reference designs and Nucleus software updates.

**FPGA Design Flow**

The FPGA reference designs for the Nucleus RTOS can be used as your starting point to build a custom FPGA-based hardware platform. All of the reference designs are provided as Xilinx Platform Studio (XPS) projects, so you can directly open these projects in XPS and edit, build, and implement the design with Xilinx EDK and ISE software. Typically, building a Nucleus system using an FPGA and configurable cores involves the following:

- Configuring a hardware platform with FPGA, processor core, hardware IP, and memory
- Building the design with EDK/ISE software to generate an FPGA bitstream
- Building software libraries with EDK to generate low-level device driver code
- Developing Nucleus device drivers and Nucleus applications
- Programming the FPGA device
- Downloading Nucleus into the FPGA hardware board

Once you have reached this point, you can start evaluating your Nucleus software and begin debugging your application.

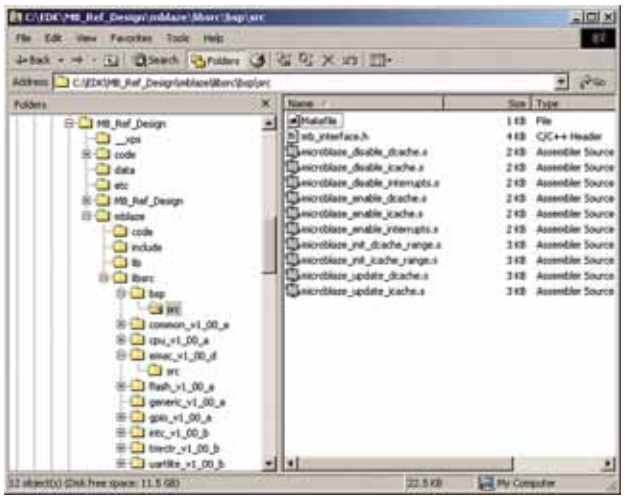

*Figure 2 - Xilinx EDK-generated source code directories*

Xilinx EDK and ISE software provide a complete environment for configuring and implementing an FPGA-based hardware platform. At the same time, EDK also generates software libraries and C header files for the hardware design. These libraries provide basic processor boot-up code and low-level hardware IP device driver function code. These low-level functions can be treated as a "BIOS" layer for Nucleus.

Figure 2 shows the source code directories generated by EDK in an XPS project. You will find one subdirectory for each piece of hardware IP, such as "emac_v1_00_d" for Ethernet and "uartlite_v1_00_b" for UART. Each subdirectory contains the driver code for that hardware IP. These driver functions are included with the hardware IP from the vendor and have been integrated into the EDK installation.

Nucleus software provides an OS adaptation layer that is an interface layer between the EDK-generated "BIOS" function layer and the Nucleus high-level device drivers. This OS adaptation layer serves as a hardware abstraction layer, which will significantly simplify the Nucleus device driver porting over FPGA-based hardware platforms.

**Nucleus Software Debugging**

Both MicroBlaze soft-core and PowerPC 405 hard-core designs provide a standard JTAG debug interface. So after implementing the hardware design in the FPGA, you can take full advantage of our JTAG-based codellab EDE or XRAY debugger to facilitate application debugging. Both codellab and XRAY have complete Nucleus kernel awareness, which can help you analyze complex real-time behaviors in a multi-tasking system.

**Co-Design and Co-Verification**

As we mentioned earlier, Nucleus software provides a viable platform for hardware/software co-design and co-verification. As one of the only EDA companies with an embedded software focus, Mentor Graphics' Nucleus RTOS and XRAY debugger are fully integrated with our Seamless hardware/software co-verification software platform.

The combination of the Nucleus RTOS and Seamless co-verification tool provides you with one of the most comprehensive hardware/software co-design and co-verification tools possible.

## Conclusion

Embedded systems are becoming increasingly complicated. To meet the challenge, integrated solutions including hardware/software co-design and co-verification are required. FPGAs with configurable processor cores bring a new, innovative approach to modern embedded system designs and open the door to hardware/software co-design and co-verification.

Nucleus software for FPGAs can significantly accelerate your hardware/software development cycle and improve your hardware/software integration quality. For more information, please visit *www.acceleratedtechnology.com.* Σ

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# Implement an Embedded System with FPGAs

## Merging the processor capability onto the FPGA on board can boost system performance and lower overall system cost.

by Zulfiqar Ali Zamindar
Field Application Engineer
Nu Horizons Electronics Corp.
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Xilinx® FPGAs have been a great platform for control logic and system interfaces for years, but have been missing the processor capabilities fulfilled by external processors in every application. Today's complex systems require a large amount of memory, a super fast microprocessor, a digital signal processor, and a variety of system interfaces to communicate with other chips, systems, and backplanes.

Every system has an external processor and memory component that delays system performance and increases system component cost. Once you've integrated both, you can then concentrate on making your system faster and eliminate performance bottlenecks.

Many companies have focused their efforts on developing the system-on-chip concept by adding feature sets to bring additional functionality to single silicon. These customized ASICs have become a very costly solution in today's competitive and time-to-market landscape.

FPGA technology has come a long way in recent years by increasing a large number of intellectual properties to reduce the cost of silicon development in various markets. This was accomplished by optimizing architecture, leading process technology, and adding both soft and hard embedded processor cores.

Some of the applications for embedded processors are infotainment systems in automotives, security systems in storage and networking markets, high-speed data analysis by data warehouse, and system monitoring in various applications. Having a processor inside an FPGA is the perfect design innovation for these types of applications; a programmable system-on-chip in the FPGA will not only support changing IP standards but can also quickly adapt to newly defined programmable systems for new markets.

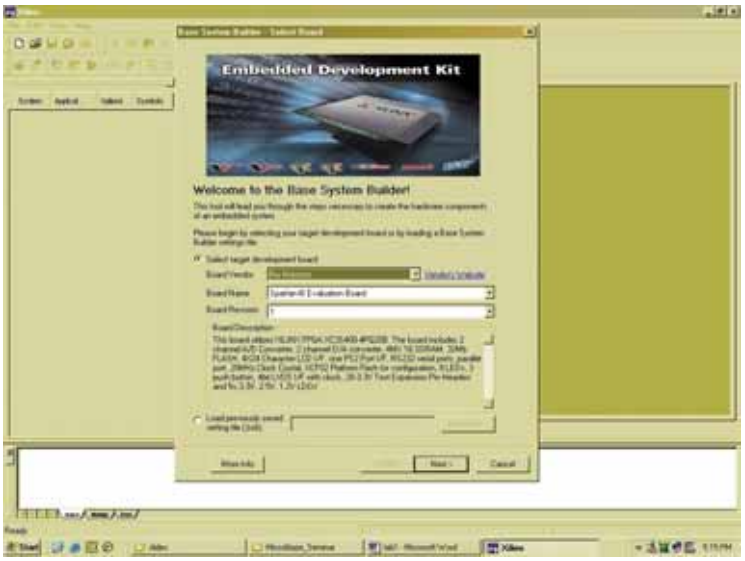



*Figure 1 – BSB flow*

## Embedded Development Kit

Xilinx expanded the features within its FPGAs by adding embedded IBM™ PowerPC™ 405 processors in its Virtex-II Pro™ devices and MicroBlaze™ soft processors in both the Virtex™ and Spartan™ architectures. This is just another step towards innovation, similar to embedded block memory, block multipliers, clock management, and multiple high-speed I/O circuitries.

Time to market still remains critical to all companies developing both hardware and software for a system. With the Embedded Development Kit (EDK) from Xilinx, you can simultaneously create both hardware and software designs and generate a system file with just a few tool clicks. The tool allows you to create block-based processor systems with many widely used peripherals like Ethernet MAC, GPIO, SDRAM Controller, UART, and IIC, all in one silicon.

With EDK v6.2 (Figure 1), the base system builder (BSB) wizard allows you to select any board from Xilinx and its distributors and connect the processor to any board component with just a few clicks. It also creates a simple software application in C that you can expand and customize.

The EDK tool also comes with a GNU-based compiler/debugger, allowing you to compile and debug within the same GUI used to develop the hardware system. The library generator (LibGen) in EDK creates all of the libraries, drivers, executables, and link files for the processor design.

Initial support for the board support package (BSP) includes Wind River Systems' vxWorks™ for PowerPC-based embedded designs and the Xilinx microkernel for MicroBlaze-based designs.

EDK v6.2 has automated the memory addressing capabilities of all of the selected design peripherals. It also has the capacity to bring developed cores into the tools environment, adding them to the processor or peripheral bus. For example, you can create a core in System Generator for DSP and bring a finite impulse response (FIR) filter or other IP into your processor-based design.

EDK is fully capable of running ISE tools in the background with a built-in feature called XFLOW, achieved by a command-line script file. This flow can synthesize, place, route, and generate hardware configuration files; compile and execute multiple software codes; generate libraries for code; and merge firmware to hardware files for downloading to a target board. All of this is achieved by just a few clicks in the EDK software.

EDK v6.2 also allows you to add ChipScope Pro™ cores during the design process to debug your design in hardware. You can add ICON, ILA, and IBA cores the same way that you can add user or Xilinx IP. Once you have downloaded the design into a target board, you can open the logic analyzer to trigger signals and view the wave form to debug your systems.

With ChipScope Pro 6.2 software, a powerful virtual I/O core has been added, which you can use as a DIP switch or LED to simulate signals and view outputs.

## The Nu Horizons Spartan-3 Board

Xilinx and its distributors have several boards for prototyping or emulating a processor-based system. A low-cost and widely adaptable prototyping platform from Nu Horizons is the Spartan-3™ development board (HW-AFX-SP3-400-DB).

NuHorizons recognizes the importance of prototyping platforms for its customers, as well as entering into new markets where Spartan-3 allows us to increase market share. The board (Figure 2) comprises the following:

- Xilinx 3S400-4PQ208C Spartan-3 device
- 4 x 24 character LCD
- LED
- Push button
- Oscillator with PLL
- RS232-C interface
- A/D and D/A converter
- Flash memory
- SDRAM memory
- JTAG configuration header for programming
- Test point headers for debugging device

This fully loaded Spartan-3 development board includes all the features necessary to prototype a MicroBlaze-based embedded system design. The board comes with the Xilinx WebPACK™ version of

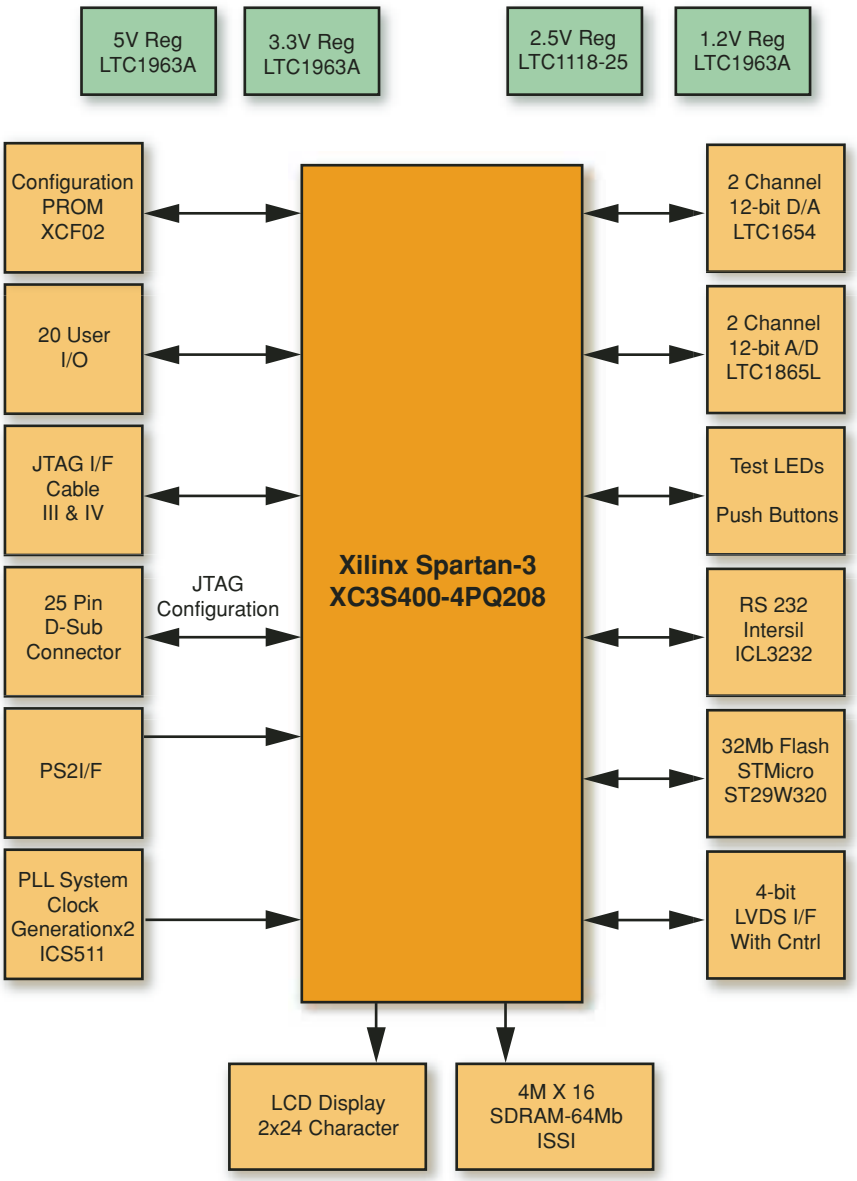



*Figure 2 – Spartan-3S400 board block diagram*

ISE tools, design files, user's manual, and documentation. The option of getting the board bundled with ChipScope Pro and EDK software is also available.

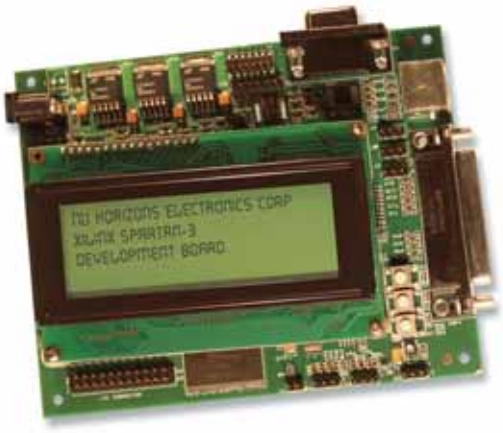
The Spartan-3 board comes with a simple display controller design that uses the MicroBlaze core, a few GPIOs, RS232, and a JTAG interface designed in EDK. The BSB flow makes it very easy to target the Nu Horizons board in EDK and generate an embedded design with the MicroBlaze processor in a few clicks. With the GNU debugger and ChipScope Pro software, you can debug a design within the same GUI environment.

Besides the MicroBlaze core, the Spartan-3 platform is a great tool in which to implement the Xilinx PicoBlaze™ 8-bit soft controller reference design. Nu Horizons field application engineers have written several designs covering memory controllers, embedded processors, hardware-in-the-loop with digital signal processing (DSP), and system monitor design using analog-to-digital (ADC) and digital-to-analog converters (DAC) on the board. ADC and DAC are very powerful attributes of our low-cost board, and two of the many competitive board features.

The Nu Horizons Spartan-3 board also supports Shift-Right Technologies' free open-source eXtreme Minimal Kernel (XMK). XMK is a 100% free, preemptive multi-threaded RTOS for microcontrollers. XMK's primary design goal is to be extremely small without sacrificing performance or functionality.

XMK's minimal footprint makes it ideal for running an 8-bit microcontroller, while its feature content makes it an excellent choice for 16-bit and 32-bit microcontrollers.

uIP is one of the several free TCP/IP stacks integrated into the XMK operating system. The uIP TCP/IP stack makes it possible to connect to a TCP/IP network without sacrificing interoperability or RFC-standard compliance.



## Conclusion

The era of creating embedded designs in FPGAs is here. With tools like EDK, anyone can implement a powerful system-on-chip design within days.

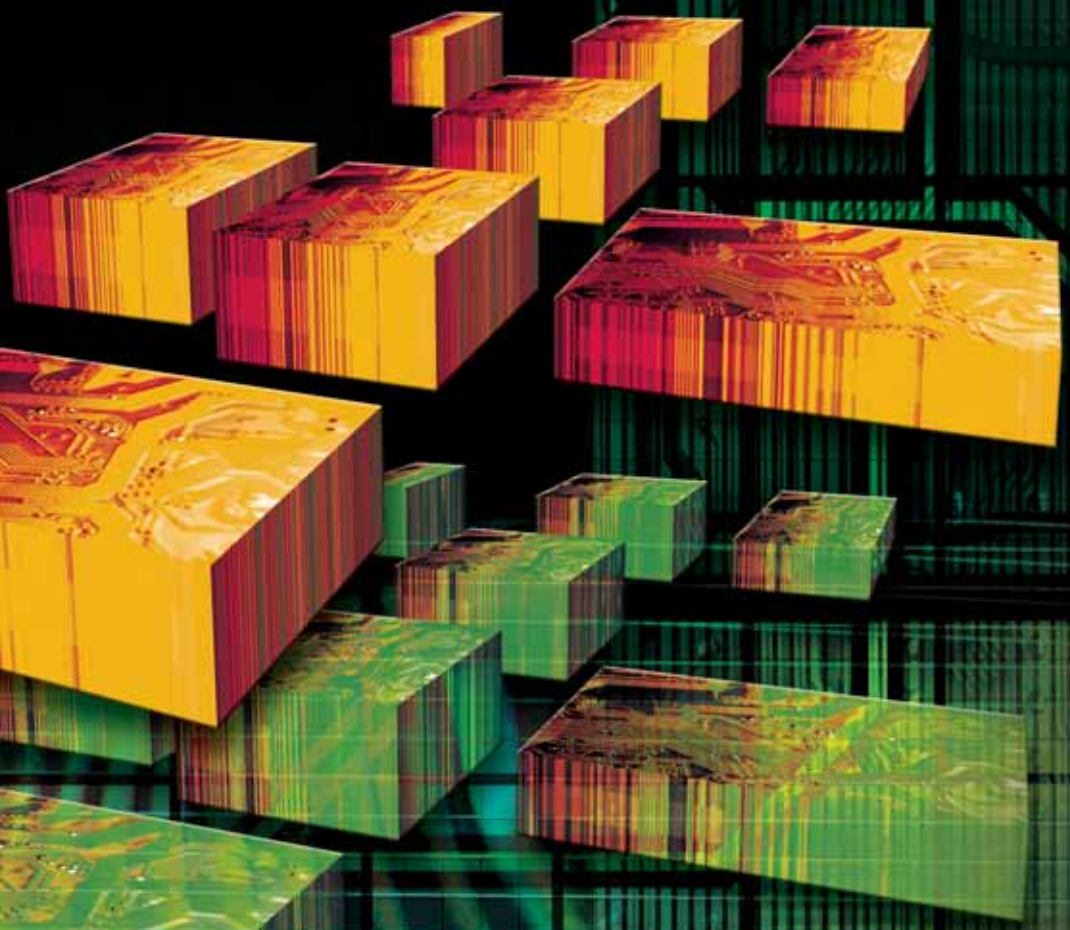
The Spartan-3 board from Nu Horizons is a perfect solution for prototyping logic and embedded processing in Xilinx FPGAs. The board has all of the interfaces necessary to create an embedded system design.

Nu Horizons is also in the process of releasing a Spartan-3 (3S1500) platform board for those who need higher density logic, more memory, and a high-performance interface for video and imaging applications.

All of the designs and related documentation for the Spartan-3 board are available on the Nu Horizons website at *www.nuhorizons.com/products/xilinx/spartan3/development-board.html.*

# Algorithmic C Synthesis Optimizes ESL Design Flows

## Using pure, untimed algorithmic C dramatically speeds implementation and increases design flexibility when compared to other C-based flows.



by Shawn McCloud
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Mentor Graphics Corporation
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**High-end electronic design flows have traditionally included the creation of Verilog™/VHDL representations by hand. These manual methods were effective in the past, but the algorithms used in many of today's new designs are so complex that traditional design practices are now inadequate.**

**Meanwhile, FPGAs are increasingly attractive because companies can avoid time-consuming, exorbitant mask re-spins and other risks associated with ASICs. The emergence of multimillion-gate, 1,000+ pin, "ASIC-like" devices incorporating embedded processors and innovative memory architectures calls for a system-level approach to programmable logic design.**

**FPGAs have already moved beyond their traditional applications into new domains such as digital signal processing (DSP). Unfortunately, creating register transfer level (RTL) implementations for high-end FPGAs can become as error-prone and time-consuming as when targeting an ASIC, thereby negating much of their inherent value.**

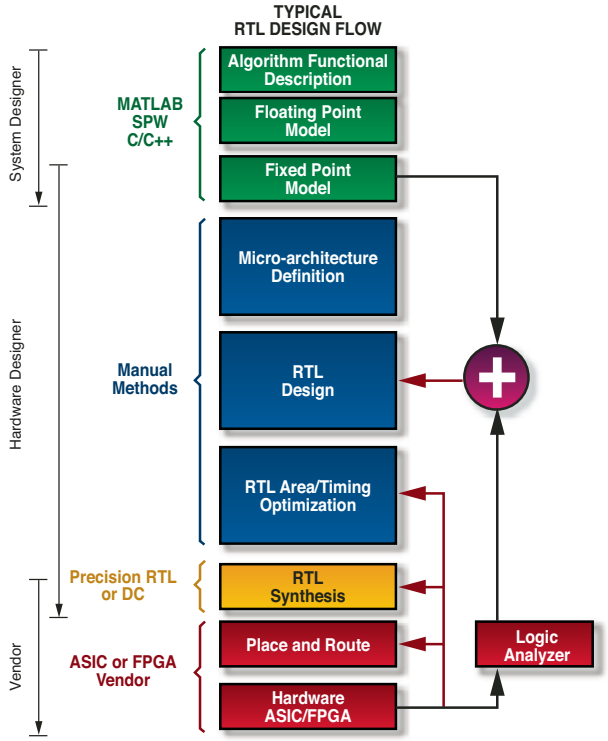


*Figure 1 – The manual, iterative methods used in conventional RTL flows no longer work for today's complex designs.*

You can now prevent these problems by adopting a design flow based on the simulation and synthesis of C representations. By using pure untimed C++ to describe functional intent, your design teams can move up to a far more productive abstraction level for designing hardware, thus reducing implementation efforts by as much as 20 times while creating a more repeatable and reliable design flow.

An important outcome of this approach is that you can produce designs of better quality than traditional RTL methods by identifying fundamentally superior micro-architectural solutions.

In this article, we'll examine the conventional design flow and its associated problems, and highlight some alternative approaches to hardware design based on the use of C/C++, comparing the pros and cons of SystemC™ and the pure, untimed C++ used by Mentor Graphics® Catapult™ C Synthesis tool.

## Traditional Design Flow

Many high-end designs in the communications or video/image processing industries are typically based on extremely complex algorithms. The first step in a conventional design flow involves modeling and proving the design functionality at the algorithmic level of abstraction, using tools such as MATLAB™ from The MathWorks or plain C/C++ modeling.

MATLAB is good for initial algorithm proof-of-concept and validation, although many design teams also develop C/C++ models to facilitate high-speed system-level verification beyond what MATLAB can provide. For subsequent discussion, we'll use the term "untimed" to represent those algorithms written either in MATLAB or pure ANSI C/C++.

Based on project requirements, system architects then partition the design into blocks to be implemented either in hardware or software. For the hardware blocks, a floating-point algorithm represents the functionality. Next, either the system or hardware designer quantizes the floating-point algorithm into an integral or fixed-point algorithm. These fixed-point algorithms are represented in MATLAB, Simulink™, or untimed C++ using bit-accurate types (SystemC 2.0). After validating the fixed-point algorithm, the hardware designer starts the long and tedious manual process of creating Verilog or VHDL for the RTL abstraction. This process can be divided into three distinct phases:

- **Micro-Architecture Definition.** Decide on the structure of the data path, control, and interfaces. Typically done on paper or perhaps a Microsoft™ Excel™ spreadsheet. The resulting micro-architecture has a significant impact on the overall speed/area of the hardware. Designs can easily swing by 10 times in area or performance based on the decisions made.
- **RTL Design.** Manually write the RTL to represent the defined micro-architecture.
- **RTL Area/Timing Optimization.** Iterate through RTL synthesis to meet design goals.

In some cases, the hardware engineers manually translate the floating-point untimed algorithm into bit-accurate RTL, either Verilog or VHDL. This RTL is subsequently synthesized into a gate-level netlist using traditional RTL synthesis technology (Figure 1).

The main problems associated with this traditional flow are:

- **Functional Intent.** A significant conceptual and representational divide exists between the system architects working with untimed algorithms and the hardware designers working with the timed RTL in VHDL/Verilog. As a result, the original design intent specified by the system architect is easily misinterpreted, causing functional errors in the end product. In addition, it is relatively easy to implement and evaluate specification changes in the untimed algorithm, but very painful and time-consuming to subsequently fold these changes into the RTL. This is a serious consideration in wireless applications, because broadcast standards and protocols constantly evolve and change.
- **Meeting Requirements.** Predicting design performance (area, delay, power) is difficult until RTL is done. Therefore, system-level partitioning and the resulting block-level design goals are inaccurate at best. Many system-level timing closure problems are directly related to poor macro-architectural choices and unrealistic goals placed on the hardware engineer designing the hardware blocks.
- **Design Complexity.** Because the untimed algorithmic domain and RTL domain are dissimilar, the manual translation from untimed algorithms to RTL is prolonged and error-prone. In addition, RTL uses technology-dependent coding styles and "hard-codes" the micro-architecture. Evaluating alternative implementations

## Any ideal flow should be based on industry-standard ANSI C/C++, the language of choice for software and system-level modeling for many years.

is impractical because modifying and re-verifying RTL to perform a series of "what-if" analyses of alternate micro-architecture implementations is too lengthy to be practical. Such evaluations may include performing certain operations in parallel versus sequentially; pipelining portions of the design versus non-pipelining; or sharing common resources. Because of the amount of time involved, design teams are limited to the number of evaluations they can perform, which can result in a non-optimal implementation. The complexity of high-end, compute-intensive applications exemplifies the difficulties associated with traditional hand-coded RTL.

- **RTL Reuse.** Using the same RTL for an ASIC and FPGA implies that the ASIC implementation is sub-optimal due to inherent FPGA performance limitations. Conversely, users can realize performance goals in an FPGA through massive parallelism; however, this parallelism may not be necessary for an ASIC. This makes it extremely difficult, if not impossible, to re-target a complex RTL design to create a tuned representation for the technology node. Finally, because RTL hard-codes the micro-architecture, using the same RTL for a 10 MHz application (for example) versus a high-performance 400 MHz application will result in sub-optimal hardware.

- **Functional Verification.** Using traditional logic simulation to verify a large design represented in RTL is computationally expensive and extremely slow.

The most important challenge facing the designer is that all of the implementation "intelligence" associated with the design is hard-coded into the RTL, which therefore becomes rigid and implementation-specific.

### Next-Generation C-based Flow

An examination of the conventional flow reveals three stages:

- Untimed algorithm evaluation in MATLAB or C/C++, including quantization and integral/fixed-point analysis
- Algorithm (untimed) to RTL (timed) translation, including verification and "what-if" implementation analysis
- RTL to gate-level netlist using industry-standard RTL synthesis

The front-end untimed algorithm evaluations and the back-end RTL-to-netlist synthesis are both well known and efficient. The bottleneck is the manual creation of the RTL, including performing "what-if" evaluations, implementing specification changes, and verifying the RTL.

Any ideal flow should be based on industry-standard ANSI C/C++, the language of choice for software and system-level modeling for many years. The pure, untimed C/C++ written by system designers is an excellent source for creating hardware because it is void of implementation details. This maximizes flexibility to the synthesis tool and provides a source that is "liquid" – capable of targeting ASICs, FPGAs, highly compact small solutions, and highly parallel fast solutions. Translation from MATLAB to C/C++ is still manual, but because these domains are conceptually very close, the translation is relatively quick and easy.

The untimed C/C++ adds significant value by providing much faster simulation than the MATLAB Simulink environment, and is thus ideally suited for system-level validation. Following verification, the C representation is used to automatically generate RTL, which in turn is subsequently used to drive existing RTL synthesis technology (Figure 2).

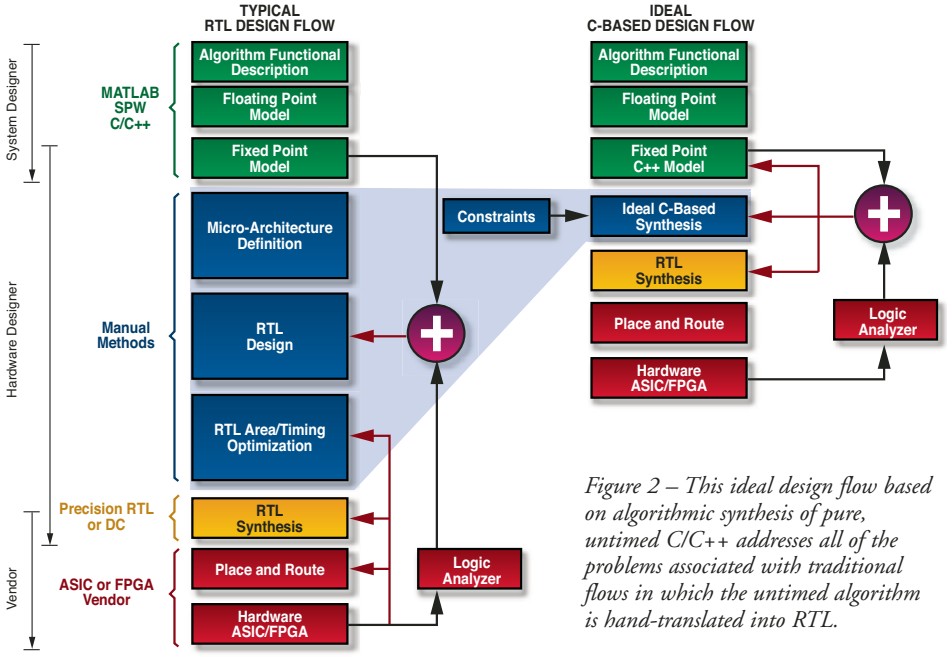


*Figure 2 – This ideal design flow based on algorithmic synthesis of pure, untimed C/C++ addresses all of the problems associated with traditional flows in which the untimed algorithm is hand-translated into RTL.*

With this flow, you can synthesize the untimed C/C++ directly into a gate-level netlist. However, generating the intermediate RTL provides a timed "comfort zone" for existing flows by allowing you to validate the implementation decisions made by the C synthesis tool.

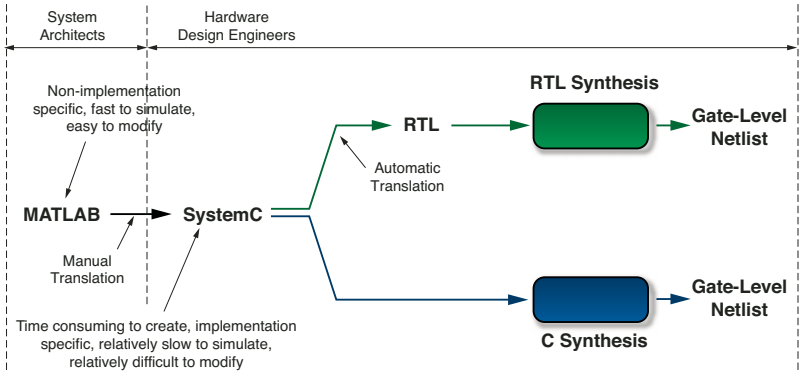


*Figure 3 – To make a SystemC representation suitable for RTL generation or direct C synthesis, you would need to write it at nearly the same level of abstraction as hand-translated RTL.*

Furthermore, RTL is a useful point to "stitch" the various functional blocks together. Large portions of today's designs exist as IP blocks represented at the RTL level of abstraction. This means that RTL is a useful point in the design flow for integrating and verifying the entire hardware system. Your design teams can thus take full advantage of existing, mature, and robust RTL design tools such as test insertion or power analysis.

The ideal flow based on algorithmic synthesis of pure, untimed C/C++ addresses all of the traditional bottlenecks:

- **Functional Intent.** Almost no conceptual gap exists because system architects and hardware designers use the same untimed C/C++ source. Their worlds are connected for the first time. Moreover, it eliminates any chance of misinterpretation by the hardware designer, thereby reducing errors and improving overall reliability. The new flow also easily accommodates design specification changes.
- **Meeting Requirements.** Algorithmic C synthesis provides accurate metrics up front, shortening lengthy RTL synthesis runtimes and manual RTL optimization. You can leverage these metrics to make system-level macro-architecture partitioning decisions, thus creating a design that is better architected to meet system performance.
- **Design Complexity.** You can address the design complexity issue by using algorithmic C synthesis to thoroughly explore any highly complex design space. C is fast and efficient to create and verify, providing additional benefits around system-level validation and integration. RTL uses technology-dependent coding styles and hard-codes the micro-architecture. Using the ideal flow, evaluating alternative implementations is fast and efficient. You can modify and re-verify C to effectively perform a series of "what-if" evaluations of alternative algorithms. Thus, your design teams are not limited by the number of evaluations they can perform, which results in an optimal implementation.
- **RTL Reuse.** A key feature of this ideal flow is that the C representation is completely abstracted from the final implementation. Therefore, as opposed to embedding implementation "intelligence" into the C representation, designers can instead use such intelligence to drive the C to the RTL implementation through a series of "soft" constraints. In turn, this means that they can easily re-target the same C representation for different micro-architectures and ASIC/FPGA implementations.
- **Functional Verification.** Verifying C is fast and efficient. A pure untimed C representation will simulate as much as 10,000 times faster than an equivalent RTL representation (the larger the design, the faster C is compared to its RTL counterpart).

Let's examine alternatives to hardware design based on the use of C/C++. These include SystemC and the synthesizable subset of pure untimed C++ used by the Mentor Graphics Catapult C Synthesis tool.

## SystemC-Based Flow

Two main SystemC-based design flows exist: both require the untimed algorithm representation to be manually translated into its SystemC counterpart. Following verification via simulation, you can automatically translate the SystemC representation into an RTL equivalent for use with existing synthesis technology. Alternatively, you can directly synthesize the SystemC representation into a gate-level netlist (Figure 3).

Because it was specifically created to represent hardware, SystemC is equipped with hardware-centric data types, including integral and fixed-point entities with rounding and overflow modes. SystemC also includes system-level simulation capabilities, including support for abstract data transactions. Although powerful, SystemC is an extremely complex language. Moreover, the pseudo-timed constructs required for SystemC synthesis and simulation are foreign to both system-level and hardware designers.

One advantage of SystemC is that it simulates as much as 100 times faster than an equivalent RTL representation specified at the same level of abstraction. However, to make a SystemC representation suitable for RTL generation or direct C synthesis, designers would need to write it at nearly the same level of abstraction as hand-translated RTL, which largely negates the advantages of using it in the first place.

Even worse, all of the implementation "intelligence" associated with the design has to be hard-coded into the SystemC representation, which therefore becomes implementation-specific. This means that a SystemC representation intended for an FPGA is not suitable for a subsequent ASIC realization, and vice versa. Finally, it is not possible to re-target the SystemC representation to a compact or highly parallel solution because the micro-architecture is hard-coded.

Another SystemC approach "wraps" the untimed C++ algorithm in a timed interface. This approach may have some advantages in system-level integration; however, the resulting source is now pseudo-timed and hard-coded to the hardware interface. Therefore, the notion of interface exploration is not practical.

For example, targeting the C source to a streaming I/O model versus a single-port memory implies re-coding the interface wrapper (difficult and time consuming). In addition, the source is no longer the pure, untimed C++ description already validated and proven by the system designer. Thus, any interface changes will require re-verification and possibly introduce foreign coding concepts to the pure C++ representation.

Finally, the degree of interface detail is extremely critical. Too much information stifles the behavioral synthesis tool and results in sub-optimal designs. Too little means the tool doesn't have the minimum information needed to synthesize the design, resulting in functional errors.

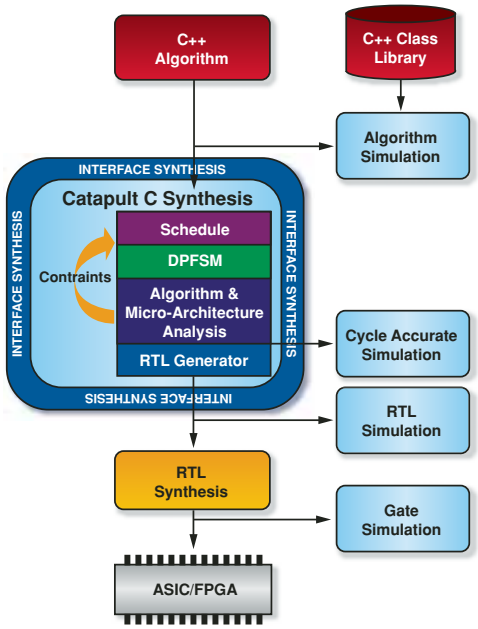


*Figure 4 – The Catapult C tool's "what if" analysis allows complete, interactive exploration of the micro-architecture and interface design space, yielding high-performance hardware that rivals hand-coded design quality.*

## Catapult C-Based Flow

As noted previously, the most significant problem with existing C-based design flows is that the implementation "intelligence" associated with the design has to be hard-coded into the C representation, which then becomes implementation-specific. This is the key differentiator of the Catapult C-based design flow from Mentor Graphics. In this flow, the C code is very close to what a system designer would write to model functional behavior without any preconceived hardware implementation or target device architecture in mind.

As opposed to adding "intelligence" to the source code (thereby locking it into a target implementation), all of the intelligence is provided by controlling the Catapult C engine itself (Figure 4).

Catapult C uses industry-standard C++ source code augmented with SystemC data types that allow specific bit-widths to be associated with variables and constants. An advantage is that many companies already create an untimed C/C++ representation of their designs for algorithmic validation. They do this because a pure C representation is easy and compact to write and simulates 100 to 10,000 times faster than an equivalent RTL representation.

The only modification typically required to use this model with Catapult C is to add a single pragma to the source code to indicate the top of the functional portion of the design – anything conceptually above this point is considered part of the test bench.

Another Catapult C advantage is its intuitive interface. Once the tool has read the source code, you can immediately perform micro-architecture tradeoffs and evaluate their effects in terms of size and speed. Catapult C easily associates ports with registers or RAM blocks. It identifies constructs like loops and allows you to specify – on an individual basis – whether they should be unrolled, partially unrolled, or left alone. You can also specify if you wish to perform resource sharing on specific entities, pipeline loops, and other constructs.

All of these evaluations are done within a few seconds or minutes depending on design size. Catapult C then reports total size/area and latency in terms of clock cycles or input-to-output delays (or throughput time/cycles in the case of pipelined designs). You can name, save, and reuse any of these "what-if" scenarios. It would be almost impossible to perform these tradeoffs in a timely manner using a conventional hand-coded RTL-based flow.

More importantly, the fact that the C source code used by Catapult C is not required to contain any implementation "intelligence" – and that all such intelligence is supplied by controlling the Catapult C engine itself – means that your design teams

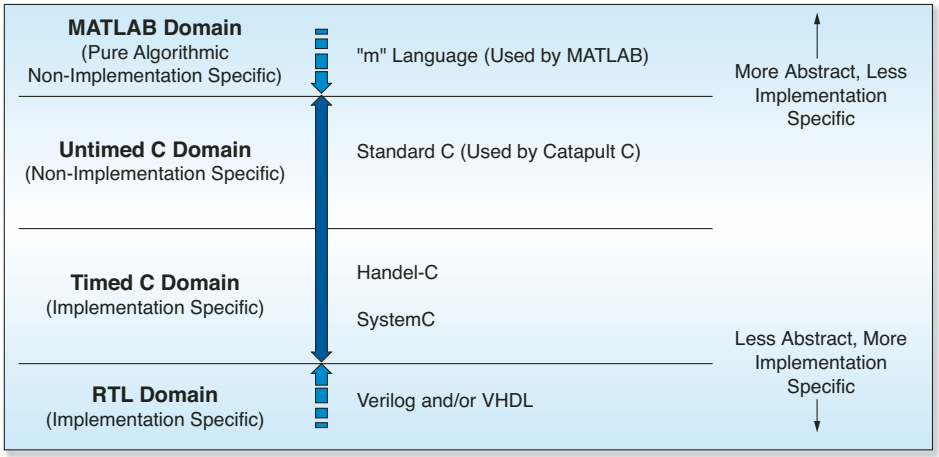


*Figure 5 – The Catapult C-based design flow supports a higher level of synthesis abstraction, speeding implementation time and increasing design flexibility when compared to other C-based flows.*

can easily re-target the same source code to alternative micro-architectures and different implementation technologies.

### Conclusion

The fundamental difference between the various C-based design flows is the level of synthesis abstraction they support (Figure 5). SystemC offers significant system-level simulation capabilities, but its synthesizable subset is at a lower abstraction level, so modification to the source drives the results.

This lack of synthesis abstraction causes the SystemC representations to be implementation-specific. This makes them difficult to create and modify, and significantly reduces their flexibility with regard to performing "what-if" evaluations and re-targeting them toward alternative implementation technologies.

By comparison, Catapult C employs models represented in standard C++ and supports a high level of synthesis abstraction. Because they are not implementation-specific, Catapult C models are compact and can thus be easily created and modified.

By means of the Catapult C engine itself, you can quickly perform "what-if" evaluations and re-target the design toward alternative implementation technologies.

The end result is that the Catapult C-based design flow dramatically speeds implementation, improves design flow reliability, and increases design flexibility when compared to other C-based flows or traditional hand-coded RTL methods.

Catapult C Synthesis has already been instrumental in many successful tapeouts from major hardware design companies worldwide. The mature, second-generation algorithmic synthesis environment unites two distinct domains – system-level design and hardware design – and when combined with Mentor Graphics ModelSim™ simulation tools, lays the foundation for next-generation electronic system level (ESL) design.

To learn more about how Catapult C Synthesis can address your hardware design needs, call Mentor Graphics to schedule a complete product demonstration, or visit our website for the latest product news and case studies at *www.mentor.com/c-design.*


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# Design Tool Performance that Lowers Your Costs

## ISE software includes advanced capabilities that slash design and verification times, getting you to design closure faster.

by Lee Hansen
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The Xilinx® Integrated Software Environment (ISE 6) is the current version of our industry-leading logic design tools, focused on delivering the highest performance available in PLD design. That leading-edge performance can help you get the highest quality of results available, and it can also significantly contribute to lowering design time and costs.

ISE 6 is packed with features designed to streamline the design flow, with technology such as:

- Timing-driven map – an ISE mapper option that helps pack more design into your highly utilized device
- ASIC-to-FPGA transition tools
- A spectrum of high-density design options built into ISE

ISE 6 can help eliminate engineering bottlenecks while delivering the fastest push-button performance available in programmable logic design.

### Lower Potential Device Costs

Introduced in September 2003, ISE 6 adds a new timing-driven map option that helps get better design utilization for your FPGA device, particularly if the device is already more than 90% utilized. Timing-driven map is a next-generation enhancement to ISE physical synthesis, and combines

placement with logic slice packing for Virtex-II™, Virtex-II Pro™, and Spartan-3™ devices to improve placement quality for "unrelated logic."

In recent benchmarks, timing-driven map was tested on large, highly-utilized designs that contained tight timing constraints, versus the standard map and place and route flow. Results varied based on many factors in the design, yet timing-driven map showed an average 30% better overall logic placement.

This advantage gives Xilinx ISE 6 customers the potential to stay in their chosen device, even if utilization is pushing 90% or higher, when competing tools would have already forced the design into a larger and thus more expensive device. The timing-driven map option is included free with all configurations of ISE 6.

### Streamlining ASIC-to-FPGA Transitions

The last few years have seen a steep decline in the number of ASIC design starts, and a good number of those projects have moved to Xilinx FPGAs for their logic delivery medium. Helping those project engineers transition from ASIC design flows with advanced support has been a priority for ISE development: thus, a number of tools are available to help.

Starting at the front of the design flow, you can use many of your existing ASIC code-checking tools to verify your HDL source. Xilinx has created a set of Xilinx FPGA-specific libraries for Synopsys™ LEDA VHDL and Verilog™ "linting" tools. The libraries are free to registered Synopsys users, and you can use them to configure your existing LEDA checker. They contain critical coding-style rules that help ensure HDL source quality and optimize implementation for the target FPGA.

ISE place and route tools also help you ensure efficient implementation. The place and route tools results offer interactive suggestions on how you can change your HDL code to reduce design size and implementation results. These suggestions help make more efficient use of FPGA resources and save overall design space.

The ISE design flow also supports technology that some ASIC designers have already invested in for verification. For example, formal verification is a technology that saw initial adoption in the ASIC design space. This structural equivalency comparison technique can drastically speed up verification time, and is often seen as an alternative to more traditional HDL simulation methods, particularly for higher density designs. These same tools also work with ISE FPGA-based designs, so if you're using Synopsys Formality™ or Verplex Conformal LEC, you can use formal equivalency checking on your Xilinx FPGA design as well.

### High-Density Design Techniques

You can also slash design times and project costs by using the high-density design options built into ISE. Free to all Xilinx users and included with ISE, these options can lead to faster timing closure and faster implementation times.

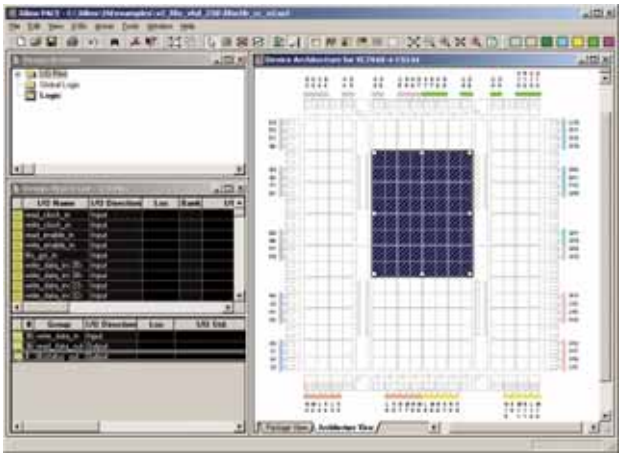

*Figure 1 – The pin assignment and constraints editor (PACE)*

**Area Mapping and Floorplanning**

ISE includes two floorplanning options: PACE (Pin Assignment and Constraints Editor – shown in Figure 1), and ISE Floorplanner. Also, PlanAhead™, the high-level floorplanning tool, is now an optional, separately purchased Xilinx design tool offering through the recent acquisition of Hier Design, integrating directly to the ISE design flow.

These tools let you group logic together and associate those groups to an area on the target FPGA. Area mapping is a fast way to keep critical sections of the design together, associate HDL together by source such as purchased IP, or to efficiently reuse HDL from an earlier project. Good floorplanning can help achieve faster timing closure and optimize design performance.

**Incremental Design**

ISE also contains Incremental Design, a technology that can slash re-implementation time by as much as 75%. Incremental Design uses a design floorplan as the starting point. The design is then implemented or passed through the synthesis and place and route cycle. If subsequent modifications are required, Incremental Design updates only the area affected by the change, leaving the other completed design areas intact and dramatically shortening the re-implementation cycle. Incremental Design is useful during the verification phase, where debug and design changes are most commonly encountered.

**Modular Design**

Modular Design is another option included in ISE supporting the team design environment. Modular Design lets team managers divide a high-density design up into "modules." Each design team can then use the entire suite of ISE design tools to complete their module independently. Modular Design deploys a "divide and conquer" strategy to high-density designs, letting teams operate efficiently in parallel, finishing the overall project faster.

### Conclusion

High-performance ISE technology isn't only about getting the fastest clock speed in your design. The advanced technology built into ISE 6 also can cut your design and verification times, slash project costs, and offer potentially lower device savings in the long run. Upgrade your designs to ISE 6, or download the evaluation version of ISE by visiting *www.xilinx.com/ise_eval*. Σ

# The Need for Speed

## Exploit ChipScope Pro to debug your high-performance designs.

by Brent Przybus
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Xilinx, Inc.
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Most of us have been there: our initial performance requirement has been increased to accommodate a new external memory interface or incorporate pre-processing now required because of an ASIC flaw. The innate flexibility of FPGAs makes them the perfect solution to address these last-minute changes and additions. But adding new capabilities is often much easier than debugging them when things no longer work.

Fortunately, Xilinx® provides a solution. ChipScope Pro™ tools enable you to place logic analysis, bus analysis, and even virtual input and output cores directly into your FPGA design and perform real-time debug and verification.

Although ChipScope Pro cores are optimized for size and performance and can run as fast as 200 MHz in Virtex-II Pro™ FPGAs, this is often not enough. Plus, adding these cores to a design may prevent it from meeting specified timing. For designs operating between 85 MHz and 150 MHz and using less than 80% of the available FPGA resources, ChipScope Pro tools can provide the easy visibility and access needed to debug and verify your designs.

For designs exceeding 150 MHz and/or using more than 80% of FPGA resources, techniques exist that allow you to use ChipScope Pro tools without impacting FPGA design performance.

In this article, we'll describe three techniques to get the most performance out of ChipScope Pro cores, gain access and visibility to debug your design, and still meet FPGA design performance.

### ChipScope Pro Debug Methodology

The easiest way to ensure that ChipScope Pro tools will not impact your design performance is to plan in advance. ChipScope Pro cores are no different that any other IP in your design – they also use logic and block RAM. By adopting a ChipScope Pro debug methodology in advance, determining what signals you would like to access for debug, and how many samples you will need to observe, you will have the best chance of meeting design performance.

The following checklist will help you meet your debug performance goals:

- Decide which signals you want to observe. This is similar to deciding which signals you are going to route out to a test header on your board. The difference is that you place virtual test headers directly within your design. And for those designs requiring more than one core, ChipScope Pro tools allow you to include as many as 15 ILA cores in a single design.
- Define how many trigger ports you need based on how you might want to trigger on different groups of signals. Consider attaching similar signals (such as individual address signals) into the same trigger port while attaching unrelated signals (such as control and data signals) to separate trigger ports. Not only will the separate trigger ports make it easier for you to create trigger conditions, but by using multiple smaller trigger ports, you might find that it is easier for the implementation tools to pack, place, and route your design.

- Decide which signals are to be used as triggers and which signals are to be captured as data. You can conserve device resources by being careful to capture only the signals you need to debug your design. Although ChipScope Pro tools provide many of the familiar trigger capabilities found in expensive benchtop logic analyzers (such as multiple trigger ports and complex trigger sequencing), you should always be aware that many of these features consume additional device resources.
- Determine the number of samples you need to observe. To do this, determine the time over which you anticipate needing to view data and divide this by the system clock rate. As many as 16,384 samples of data storage are available using on-chip block RAM. If you need more storage, you can use multiple debug cores or you can use the ChipScope Pro-enabled Agilent™ FPGA dynamic probing solution, which allows you to store internally probed signal data directly on an external Agilent logic analyzer.
- Decide how you are going to get data off-chip. Start with a JTAG port and Agilent trace port. You can use the JTAG port for configuration, hardware debug, and software debug. The Agilent trace port provides the flexibility to interface to the Agilent 16900 series logic analyzer with FPGA dynamic probing technology. You will probably already have JTAG set up on your board for FPGA configuration. The Agilent trace port uses between four and 128 user I/O pins that tie directly to a Mictor™ or Agilent soft-touch probe pad connector. Instructions for laying out these connectors are included in the Agilent data sheet, available at *www.xilinx.com/chipscopepro/*.
- Use the core generator to define the ILA cores to the specifications you have defined in the previous steps. The ChipScope Pro core generator will produce embeddable EDIF netlists and HDL component instance templates that you can incorporate into your HDL design. If your design has already been synthesized, you can use the ChipScope Pro core inserter to add ChipScope Pro cores to a design by selecting which nets and signals you want to view.

By defining a debug and verification methodology in advance, you have accounted for the logic, block RAM, and routing resources needed – and minimized the chances of ChipScope Pro cores impacting your design timing.

### Techniques to Achieve Performance

What if you have not planned for debug? Let's say your design is running at close to 200 MHz and something is not functioning correctly. When you add a ChipScope Pro ILA core to view signals in the faulty logic, the design fails to meet your timing requirements. Here are some techniques that can help:

- Reduce the size and complexity of your trigger ports and corresponding match units. Start with a basic trigger type, with a width as narrow as possible. For example, an 8-bit basic match unit will consume a fraction of the logic of a 36-bit range-type match unit.
- Use "trigger same as data." By selecting trigger same as data, you reduce the number of loads on the instrumented design nets from two to one.
- Avoid critical paths. Understand the critical paths within your design and avoid instrumenting them if at all possible.
- Watch what you instrument. Avoid instrumenting combinatorial logic, which may cause the new logic implementation to split into multiple slices. Whenever possible, try to instrument the outputs of flip-flops instead.
- Apply area constraints to ChipScope Pro cores. Bound the inner logic of a ChipScope Pro core and allow the outer flip-flops to float. A tighter fit may result in higher performance of the ILA core while allowing the outer flip-flops to be placed close to the instrumented design nets.
- Properly constrain your design. Run "trce -a" to report unconstrained nets within your design. Apply timing constraints where needed and use a constrained system clock net to drive any ChipScope Pro cores.
- Disable RPMs. Sometimes allowing the ChipScope Pro core logic to float – particularly the flops that make up the cores – enables you to better fit ChipScope Pro cores within any available logic.

### When All Else Fails ...

If you've tried all of these techniques and your design still doesn't meet timing, or if the tools seem to choke on timing, try this advanced technique. Guide filing uses your non-instrumented design netlist as a guide for routing in ChipScope Pro cores. Although this technique does not guarantee that timing will be met, it can work in some cases.

The steps to guide filing are:

1. Synthesize your design.vhd into design.ngc using your chosen synthesis tool (substitute design.edf for design.ngc, if you are not using the xst synthesis tool).
2. Translate your design.ngc into design.ngd using ngdbuild.
3. Map your design.ngd into design_map.ncd using the map tool.
4. Place and route your design._map.ncd to design_par.ncd using the par tool.

Now add ChipScope Pro cores to this design by following these steps:

5. Copy the design.ngc to design_debug.ngc.
6. Insert ChipScope Pro cores into design_debug.ngc using the ChipScope Pro core inserter tool.
7. Translate design_debug.ngc into design_debug.ngd using ngdbuild.

8. Map design_debug.ngd into design_debug_map.ncd using a -gm (guide mode) option, specifying your original design_map.ncd as the guide file. You will have the option of specifying exact, incremental, or leveraged guide modes. Start with exact; it may take a little longer to compile, but will probably deliver the best results. If that doesn't work, or if you would like a better result, try the leveraged option. This option allows logic in your design to be moved if it will benefit placement of the new ChipScope Pro cores.

9. Place and route design_debug_map.ncd into design_debug_par.ncd using a -gf (guide file) option and specifying your original design_par.ncd as the guide file. Use the same -gm guide mode option (exact, incremental, or leveraged) that you used in step 8.

10. Convert design_debug_par.ncd into a bitstream called design_debug_par.bit and use the ChipScope Pro analyzer to configure and debug your FPGA design.

After steps 8 and 9, you will receive tool messages stating that a percentage of the net names in the design have changed. This represents the new ChipScope Pro logic added to your design.

If after performing these steps your instrumented design is still not meeting timing, you may want to go back to step 2 in your original design and try to allocate an area region for ChipScope Pro cores. Then repeat the remaining steps.

## Conclusion

In this article, we've shown you techniques for debugging high-speed FPGA designs using ChipScope Pro tools. No design is the same and sometimes more advanced techniques are required. If you have techniques that have worked for you and you'd like to share them, or if you need help in implementing any of the techniques described, please send an e-mail to *chipscope_pro@xilinx.com.*


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# Lower Your PCB Manufacturing Costs

## By choosing an FPGA with the right features, you can reduce your PCB manufacturing costs and even EMI levels.

by Suhel Dhanani
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Lowering total system costs is the key goal when developing high-volume/low-cost systems. Although many system designers carefully select components with the lowest unit cost, they often ignore the actual cost of manufacturing the PCB.

However, with careful design considerations, you can achieve the same functionality and performance within a smaller PCB, using fewer layers and sometimes with less components.

Some of the newer low-cost FPGAs, such as Xilinx® Spartan-3™ devices, now include a host of features that can reduce the number of on-board components and interconnect traces, enhance signal integrity, and reduce system electromagnetic interference (EMI) noise levels, essentially enabling you to significantly lower your system costs.

### Reducing PCB Size and Complexity

The most obvious way to reduce the cost of any PCB is to make it smaller and have fewer layers. By reducing the total board area and using fewer layers (four instead of six, for example), you can cut down on the manufacturing expense.

For a typical 4" x 6" board, going from six to four layers can reduce the cost by anywhere from $2 to $4 per board. When you calculate the total savings based on the quantity of boards manufactured, this could be a substantial amount.

Another factor that influences the manufacturing cost of a PCB is EMI noise compliance. In cases where EMI is an issue, you need to design for the lowest possible EMI level, because trying to retrofit the PCB to meet EMI compliance can result in expensive redesign, re-layout, or shielding.

Good design techniques such as maintaining optimum signal integrity, having fewer traces running lower voltage levels, and distributing slower clocks on board can all help reduce the overall EMI level.

By using features found in Spartan-3

FPGAs, you can reduce total PCB manufacturing costs by optimizing the area and number of layers and minimize total EMI noise levels.

## Spartan-3 Features

### Digitally Controlled Impedance

One of the key features provided by Spartan-3 devices is digitally controlled impedance (DCI). This allows you to not only (potentially) eliminate most external resistors, but also design for optimum signal integrity.

DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variations in the ambient temperature, supply voltage, and manufacturing process. This feature is available for most popular I/O standards, including LVCMOS, LVDS, SSTL, HSTL, and GTL.

Figure 1 illustrates how the DCI feature can eliminate external resistors normally used for termination. Not only does this feature allow you to tune the output driver impedance – thereby optimizing signal integrity – but it also reduces the total number of components on board, with the resultant benefits in reliability, manufacturability, procurement costs, board area, and routability.

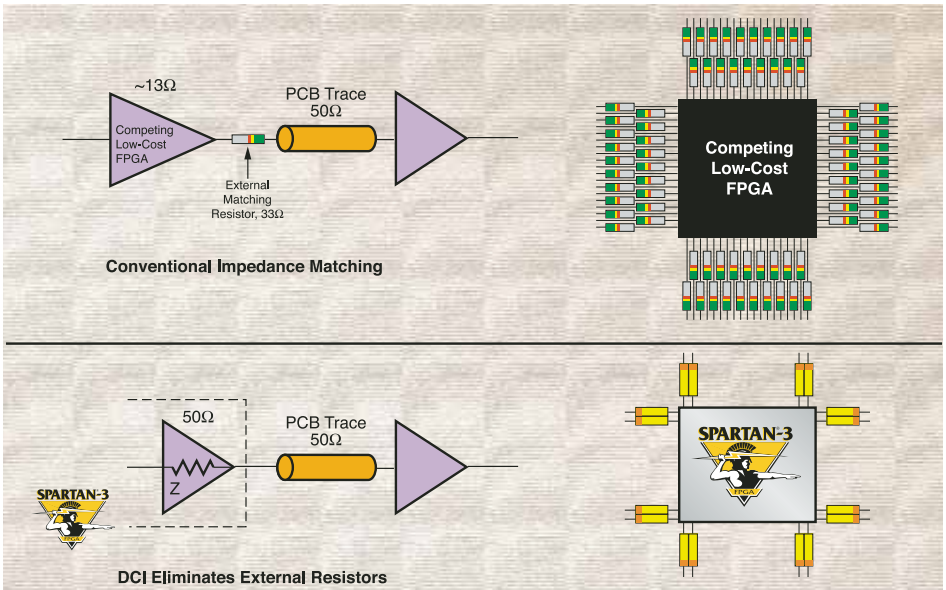



*Figure 1 – Spartan-3 DCI feature eliminates the need for external matching resistors.*

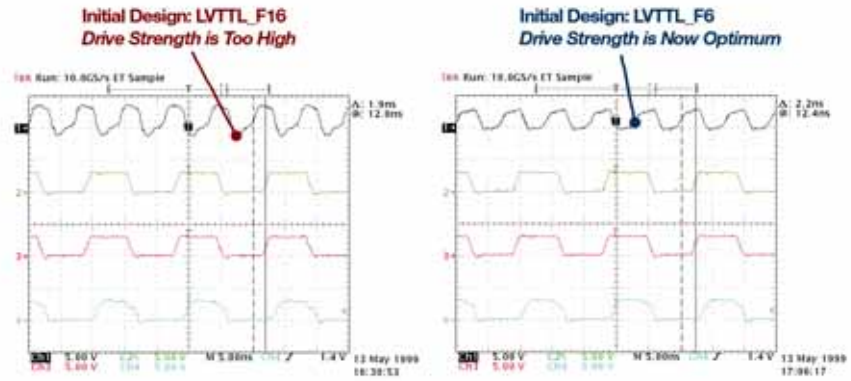



*Figure 2 – Drive strength can be adjusted by loading an updated bitstream.*

### Drive Strength and Slew Rate Control

Another Spartan-3 feature is the ability to adjust the output drive strength and slew rate of the output drivers. Two options, fast and slow, control the output slew rate. You can select as many as seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. (These options are available when using one of the LVCMOS or LVTTL standards.)

Choosing the appropriate drive strength level is yet another means to minimize bus transients and optimize board signal integrity, as shown in Figure 2.

These adjustments can be made by merely updating the device bitstream and require no board re-layout. Thus, you can continue optimizing the drive strengths long after the board has been laid out.

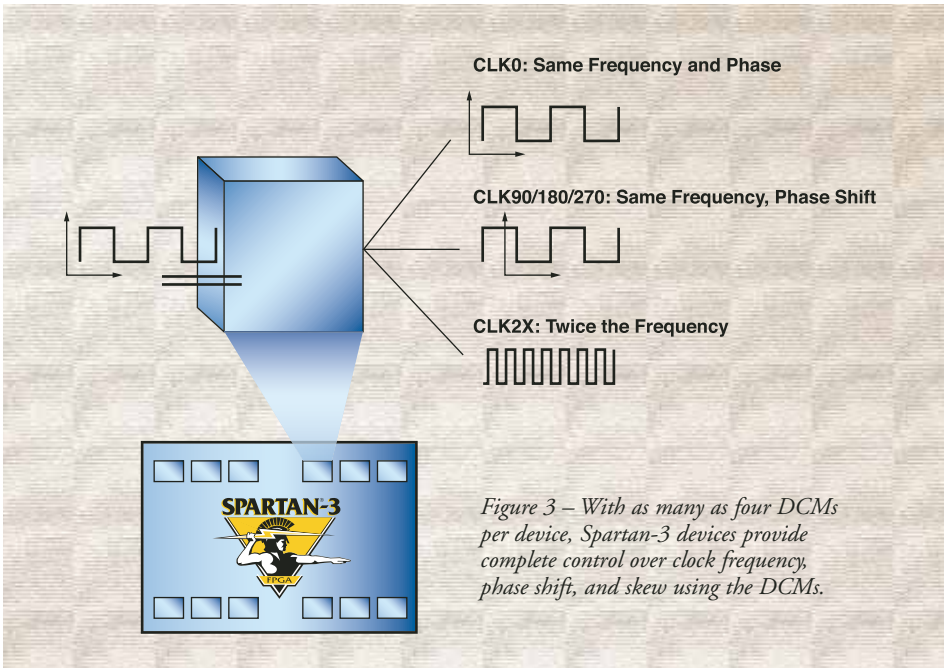



*Figure 3 – With as many as four DCMs per device, Spartan-3 devices provide complete control over clock frequency, phase shift, and skew using the DCMs.*

### On-Chip DCMs

All Spartan-3 devices have multiple high-performance digital clock managers (DCMs). Each DCM allows clock skew elimination, clock multiplication, clock division, and reconstruction, as well as phase shifting.

Although you can use the DCMs to eliminate the need for external clock management devices, they also allow you to run a slower clock on board (using the internal clock multiplication feature) and run fewer clock traces on board (using the clock reconstruction feature), as shown in Figure 3.

Using these features simplifies the layout of high-speed PCBs and can lower overall EMI levels by allowing you to run fewer and slower clocks traces across the board.

### On-Chip Voltage and I/O Standard Translation

All I/Os in Spartan-3 devices are allocated between eight banks, as shown in Figure 4. Each I/O bank has an independent $V_{REF}$ line.

The I/Os support most of the popular single-ended I/O standards such as LVTTL, LVCMOS, SSTL, HSTL, GTL, as well as differential I/O standards such as LVDS and RSDS. Because each I/O bank can independently support a different I/O standard and a different $V_{CCO}$, this feature lets you implement voltage translators and I/O standard translators within the FPGA, eliminating the need for external components. Fewer components translates to smaller PCB and lower system costs.

*Figure 4 – With eight independent I/O banks and support for multiple I/O standards, Spartan-3 devices eliminate the need for external voltage or I/O translators.*

### Comprehensive Support for Differential Signaling

The Spartan-3 family is the only low-cost FPGA family whose I/Os support LVDS transmission without the need for external resistors. This popular standard is widely used for high-speed chip-to-chip communication because of its higher noise immunity, lower EMI, and higher performance.

Because LVDS is a low swing standard (~350 mV) with a slower slew rate (1V/ns), it exhibits lower EMI. And because it is a differential I/O standard, it has better noise immunity. LVDS allows for very high data transfer rates (622 Mbps in the Spartan-3 architecture), enabling fewer pins to transfer large amounts of data serially.

| | Standard | Output $V_{CCO}$ | Input $V_{REF}$ |
|---|---|---|---|
| Single Ended | LVTTL | 3.3V | -- |
| | LVCMOS 33 | 3.3V | -- |
| | LVCMOS 25 | 2.5V | -- |
| | LVCMOS 18 | 1.8V | -- |
| | LVCMOS 15 | 1.5V | -- |
| | LVCMOS 12 | 1.2V | -- |
| | PCI 32/64 bit 33MHz | 3.0V | -- |
| | SS TL2 Class I | 2.5V | 1.25V |
| | SS TL2 Class II | 2.5V | 1.25V |
| | SS TL18 Class I | 1.8V | 0.9V |
| | HSTL Class I | 1.5V | 0.75V |
| | HSTL Class III | 1.5V | 0.9V |
| | HSTL18 Class I | 1.8V | 0.9V |
| | HSTL18 Class II | 1.8V | 0.9V |
| | HSTL18 Class III | 1.8V | 1.1V |
| | GTL | -- | 0.8V |
| | GTL+ | -- | 1.0V |
| Differential | LVDS2.5 | 2.5V | -- |
| | Bus LVDS2.5 | 2.5V | -- |
| | LVDS_ext2.5 | 2.5V | -- |
| | RSDS | 2.5V | -- |
| | LDT2.5 | 2.5V | -- |
| | LVPECL | 2.5V | -- |

All of the device package combinations of Spartan-3 support LVDS. This means that you can choose low-cost QFP packages as well as higher pin-count BGA packages.

Figure 5 illustrates how competing low-cost FPGAs require three external resistors for each LVDS transmit channel. Spartan-3 LVDS transmitters do not require the use of an external resistor network because the I/O buffers were designed to support low swing differential signaling.

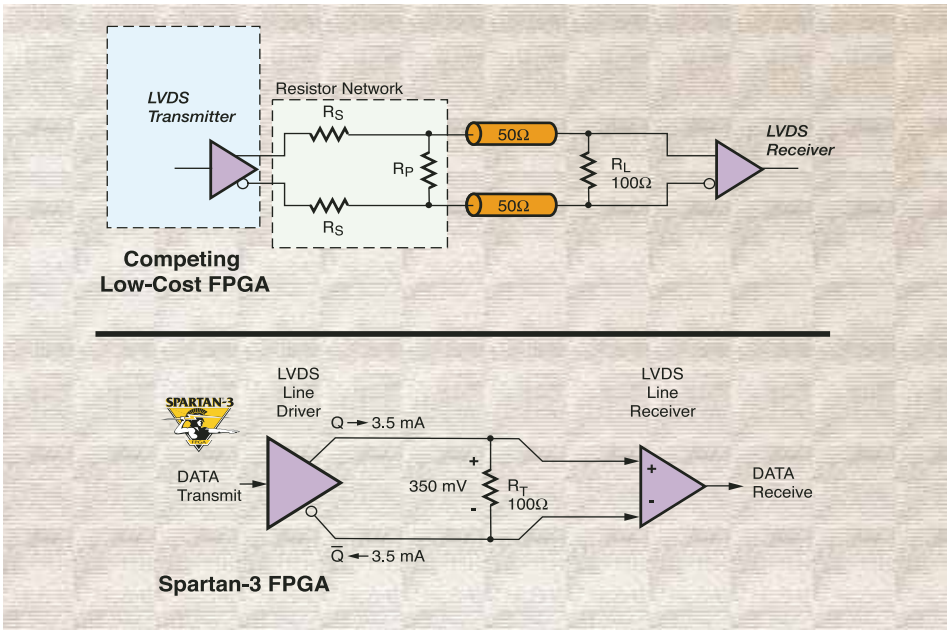



*Figure 5 – Spartan-3 I/Os are designed to transmit LVDS signals without the need for external resistors.*

### Conclusion

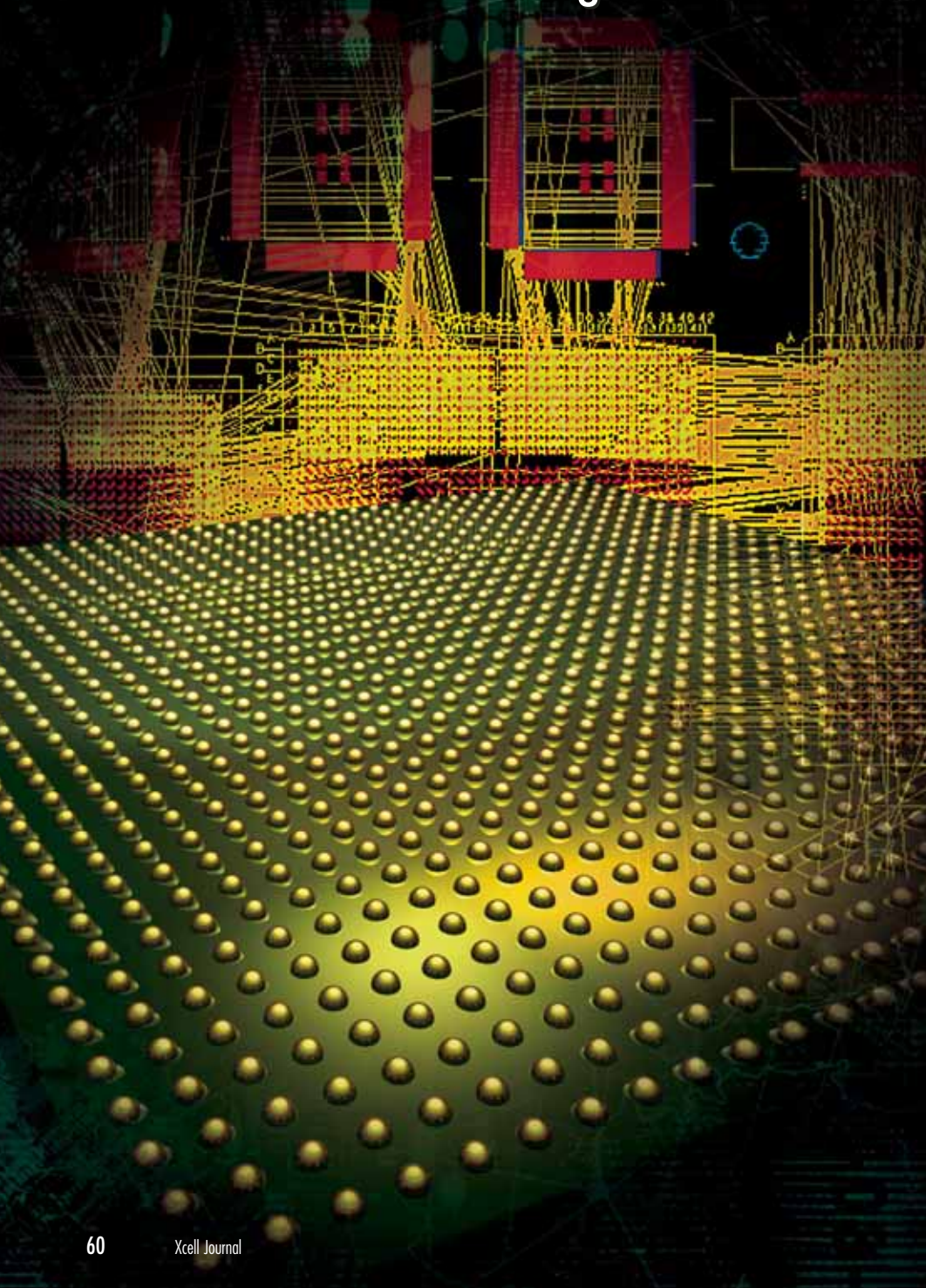
Using the many features available with Spartan-3 FPGAs allows you to eliminate external components such as resistors, voltage translators, level shifters, and even external clock management devices. This not only increases board reliability and eases manufacturing costs, but also reduces the size of the board and may in some cases reduce the number of layers required for routing, potentially lowering total system costs.

If EMI compliance is a concern, there are many features within Spartan-3 devices that improve signal integrity, allow for fewer traces, and enable low swing I/O signaling – all of which contribute to lower the EMI level of the system.

For more information on Spartan-3 features and how these features can help you reduce your system cost, visit *www.xilinx.com/spartan3/*.

# Plan FPGA Signal Assignments and Optimize PCB Routability

## Eliminate or reduce design iterations with DesignF/X.



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**Managing signal assignment of high-pin-count FPGAs, especially in multi-FPGA designs, is a growing problem. As most hardware managers will attest, this problem manifests itself in three ways.**

**First, the number of communication channels interfacing with a typical FPGA makes I/O assignment a cognitive challenge for logic designers to balance. These cognitive challenges include the handling of:**

- **Key constraints imposed by each channel, including voltage, signal strength, termination, and data versus clock skew.**
- **FPGA signal assignment constraints, such as I/O banking and simultaneous switching output rule sets.**

Second, because of an excessive number of wire crossings, layout engineers may find it physically impossible to route their designs with the specified stackup and PCB design rule checks (DRCs). The only option is to increase both the number of signal routing layers and via count. However, this will result in reduced signal quality and may drive up the manufacturing cost substantially.

Third, most of today's EDA tools focus on solving the above issues for a single device, and have little or no knowledge of other system devices or their connections. The end result is a sub-optimal pinout that has been assigned without knowledge of the system. If you are a logic designer, you know it is likely that the pinout will need several refinements because of required negotiations between you, the hardware engineer, and SI engineer.

This time-consuming process is further exacerbated as system complexity increases, along with the need for precision change control and the resulting process management overhead. Figure 1 shows one of many complex design configurations.

Design F/X directly addresses these three core system design issues by:

- Significantly reducing the need to memorize I/O banking rules. DesignF/X provides an automated signal assignment optimization process and keeps you informed of DRC rules and requirements associated with your selected I/O standards.
- Providing system-level optimization of the signal assignment for one or more FPGAs and their associated devices in a PCB environment, while honoring the design rules. This optimization will result in the highest PCB routability, enabling you to reduce your design iterations and focus on core design.

## Design F/X and Existing Design Flows

DesignF/X is easy to learn and even easier to integrate into your existing design flow. Figure 2 highlights a typical DesignF/X flow on the right, compared to today's time-consuming and error-prone iterative process on the left.

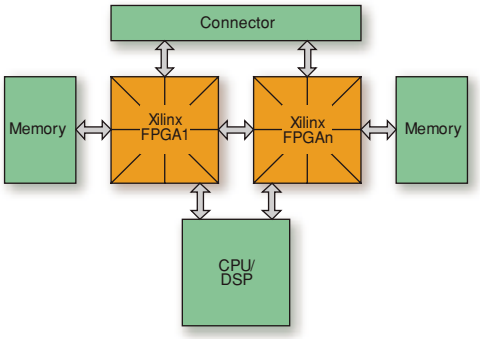


*Figure 1 – A typical multi-FPGA system design*

We argue that the traditional design flow is a lengthy and error-prone process because:

- Several manual entry points exist, including HDL, signal assignment spreadsheets, schematic symbols, schematics, package drawings, and constraint information.
- There is no tool to validate data from package to component to netlist. For example, neither the schematic nor the netlist have knowledge of the package, yet package knowledge is required for proper validation.
- The back annotation process is often broken because required FPGA updates and attributes are not automatically passed completely through to the board tools for more efficient routing and planning.
- Generally, several iterations are required to get the correct FPGA pinout based on negotiations between layout engineers and FPGA designers.

DesignF/X eliminates these issues by allowing end-to-end design with verified

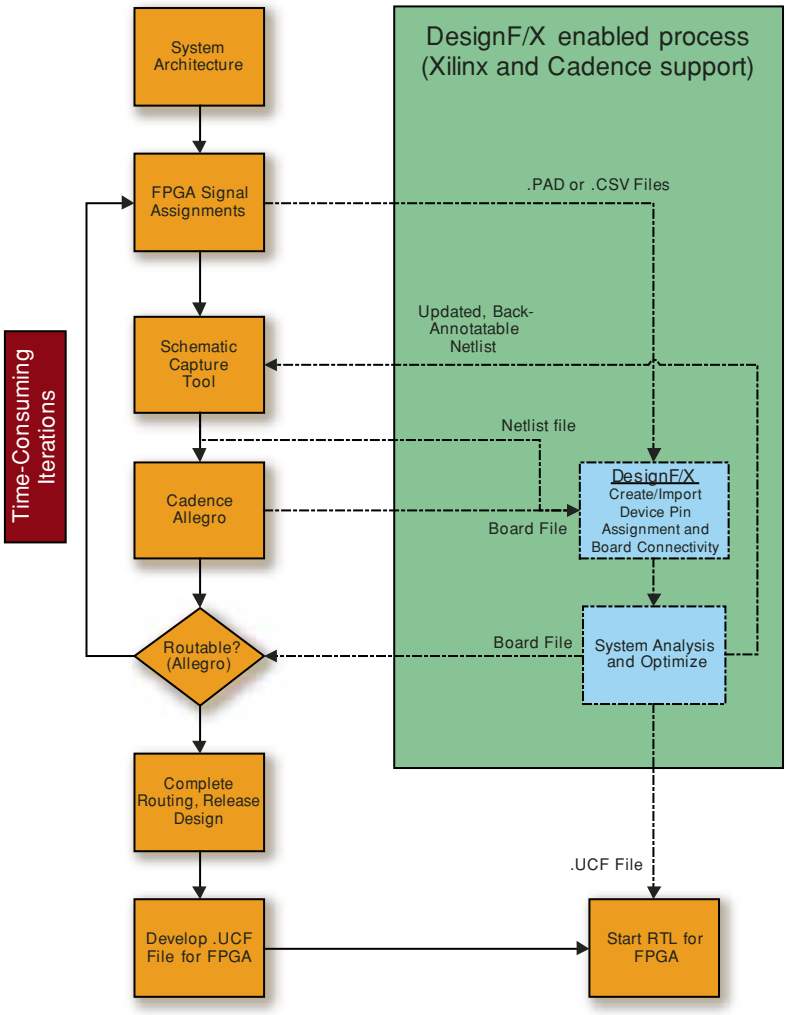


*Figure 2 – DesignF/X flow as it relates to overall PCB design flow*

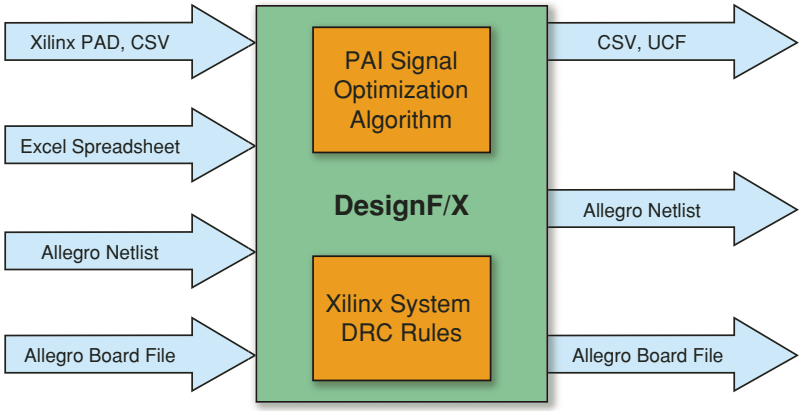


*Figure 3 – DesignF/X I/O capabilities*

data inputs and correct-by-design FPGA pinouts that are optimized at the system level for best routability.

You need not interrupt your current design flow, because DesignF/X provides several vector points at which you can analyze your design. DesignF/X also provides the I/O capabilities shown in Figure 3.

Only two successive steps are required to get an optimized design in a single iteration:

1. Create or import device pin assignment and board connectivity.
2. Analyze and optimize your configurable devices for the best possible routability while honoring Xilinx FPGA design rules.

### Signal Assignment Planning

DesignF/X is built around Xilinx parts and their associated design rules. As of June 2004, DesignF/X supports the following capabilities:

- I/O banking DRCs (voltage, I/O standards, and on-chip termination are checked for intra-bank compatibility)
- Automatic reservation of Vref, VRP, and VRN pins when necessary, based on the selected I/O standard
- Automated recognition and handling of differential pairs, including swapping signals as a pair where legal during optimization

### Usage Model

The first step is to select a Xilinx-specific device (see Figure 4). After you select your package, you may import a Xilinx .pad or .csv file, or you can start with no file inputs. In either case, you can use the signal assignment spreadsheet shown in Figure 5 to:

- Assign signals to pins and create signal groups and buses
- Apply I/O standards and mark specific pins as fixed if you do not want them considered for optimization

Each time you change a signal's I/O standard, location, or pin type (direction), DesignF/X will respond with a DRC for compliance with Xilinx-specific rules.

The screen shot for Figure 6 was generated after changing the I/O standard of two buses within the same bank. The output screen is interactive and shows which pins are causing the DRC error. A key ease-of-use feature shown is the way a number of related errors are summarized into one line.

After you have finished assigning signals, DesignF/X will perform one last DRC. If the DRC passes, you will be allowed to use the part for analysis and optimization on the "virtual PCB" screen. You can also rapidly generate a .ucf file for use in your Xilinx ISE environment for a rapid place and route check.

### Signal Assignment for Optimal PCB Routing

Once you have all your programmable devices described and pin assignments defined, you can choose to import your connectivity information using a netlist file, or, if you do not have a netlist, use a table to define connectivity. Once connectivity information is defined, you can place your components on the "virtual PCB" and optimize them.

*Figure 4 – Select Xilinx device or define new device screen*

*Figure 5 – Signal assignment screen*

*Figure 6 – DRC interactive screen*

As a PCB designer you probably want to optimize your devices at the system level for the best possible routing early in the design phase – before completion of the FPGA place and route – while maintaining compliance to fundamental Xilinx DRCs on the I/O side. This will help you:

- Reduce PCB wire crossings, which directly correlates to reduced via counts, potentially reduced layer counts, and faster routes that enable early route studies for more what-if analyses
- Reduce SI complications and generate higher quality signals, also from reduced wire crossings and via counts (vias can result in stubs at high speed that are detrimental to edge rates)

## Summary of Results

Recently, a major semiconductor/systems client was in the process of developing a new system with two Xilinx Virtex-II™ devices of 1,704 pins each and a third at 1,152 pins, combined with a custom processor.

The client faced the following challenges:

- A team co-located in three different cross-country cities: the FPGA engineer, the hardware engineer, and the layout engineers were each located in different cities.
- The fast-paced design reached layout, but the PCB board was not routable.
- Obviously, any changes made to get the PCB board to route needed to comply with the rules of the Xilinx devices.

Instead of investing several man-weeks to fly all of the engineers to one location and attempt to fix the problem by hand, they called on DesignF/X to provide the following solution:

- The FPGA engineer sent the necessary Xilinx .pad files to the hardware engineer.
- The layout engineers sent the Cadence Allegro board file to the hardware engineer.
- The hardware engineer imported all files into DesignF/X and the PCB was optimizing within hours.
- The hardware engineer then output the updated Cadence Allegro board file and the updated Xilinx .ucf files and sent them back to the appropriate engineers.
- The FPGA engineer confirmed that the new pinouts for the Xilinx parts did not violate any Xilinx rules and signed off on the update.

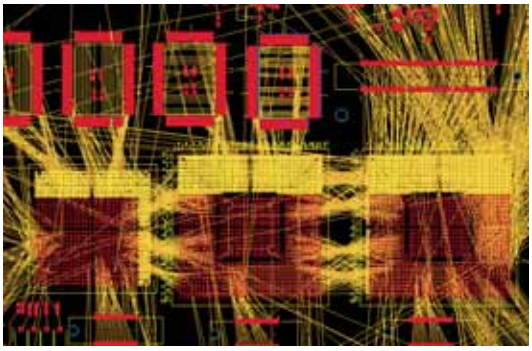

*Figure 7a*

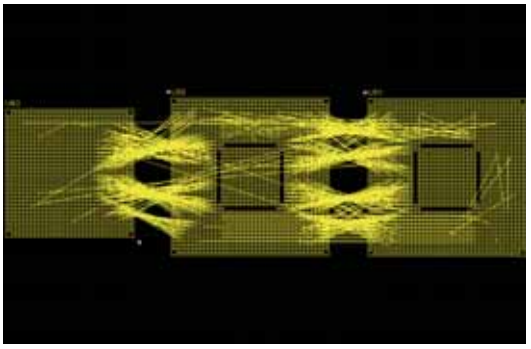

*Figure 7b*

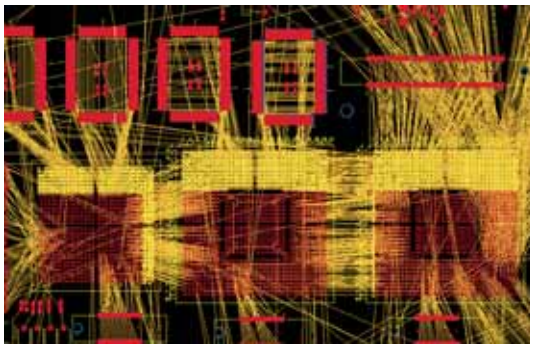

*Figure 7c*

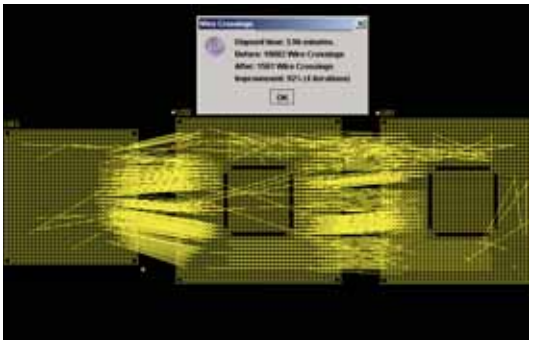

*Figure 7d*

*Figure 7 – PCB before and after optimization, shown in Cadence Allegro and DesignF/X*

| Problem Viewed in Cadence Allegro | Problem Viewed in DesignF/X |
|---|---|
| Before Optimization | 19,002 Wire Crossings |
| Figure 7a | Figure 7b |
| After Optimization (< 10 Minutes) | 1501 Wire Crossings (92% Improvement) |
| Figure 7c | Figure 7d |

*For the full account of this example application, visit* www.prodacc.com.

- The layout engineers successfully routed the PCB board and back-annotated the changes to the Cadence OrCAD schematic.

The entire process took days instead of weeks. Figure 7 shows the layout of the three Xilinx FPGAs before and after DesignF/X optimization. This design was not routable for a given PCB layer count until DesignF/X optimized the pinouts of the three FPGAs.

## Conclusion

Whether you are a logic designer, a hardware engineer, a PCB layout engineer, an engineering manager, or an FAE, you are likely facing one or more of the issues mentioned in this article with complex designs.

To learn about the latest DesignF/X features, visit the Product Acceleration website at *www.prodacc.com*. To schedule a DesignF/X demonstration, please send an e-mail to *sales@prodacc.com* or call (408) 551-0882.

Product Acceleration is a member of the Cadence Connections program and the Xilinx EDA Alliance Program. We are committed to the best solutions possible for complex FPGA design implementation integrated with the Cadence Allegro Platform and Xilinx ISE software.

# Next-Generation Data Transport over Metro Area Networks

## The Xilinx GFP core enables efficient transport of LAN/SAN protocols over SONET-based networks.

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SONET networks are ubiquitous in the telecommunications industry for transporting both voice and data over long distances. Standard protocols have targeted the underlying transport layer, including ATM for voice and data and HDLC or PPP for data transfer. However, each of these protocols introduces bandwidth inefficiencies, as none were developed specifically to address data transport over SONET/SDH networks.

Additionally, telecom carriers are motivated to increase revenues by diversifying the types of client traffic transported across their networks and optimizing their bandwidth utilization. This includes capturing new market sectors such as storage area networks (SAN – utilizing Fibre Channel) and emerging video on demand (utilizing DVB-ASI). In this case, Fibre Channel and DVB represent two specific types of client traffic or client data as defined by these data network protocols.

The Generic Framing Procedure (GFP) is the first encapsulation mechanism capable of addressing this wide range of data transport applications by supporting a suite of client network protocols (summarized in Table 1). GFP was introduced by the International Telecommunication Union (ITU) as recommendation G.7041/Y.1303, and provides a flexible, efficient mapping of various protocols onto a transport network.

In this article, we'll describe a flexible suite of networking solutions that address the needs of systems vendors deploying metro equipment to provide these services. Xilinx® supports applications ranging from

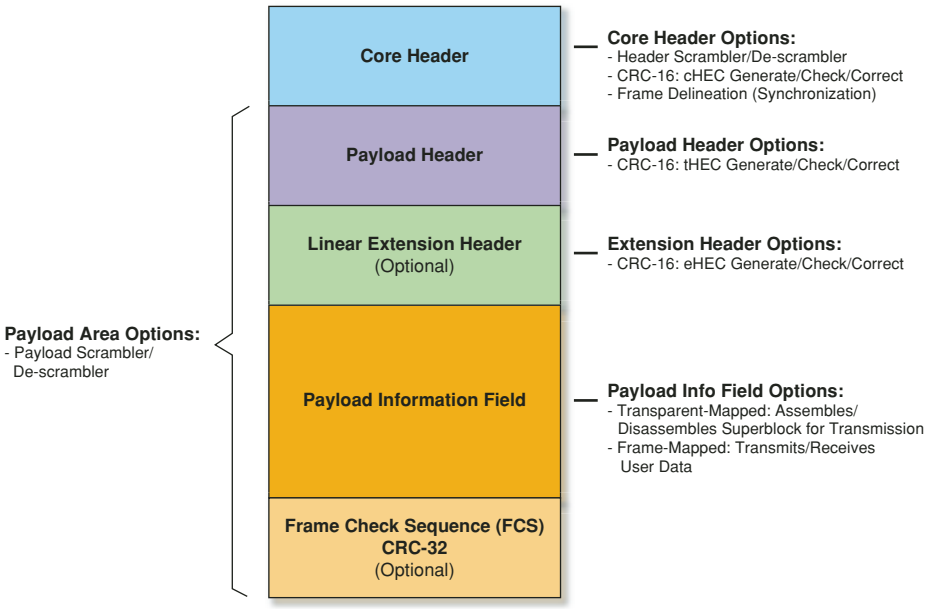


*Figure 1 – GFP core options for frame processing*

a completely integrated client adaptation with Virtex-II Pro™ devices to low-cost protocol encapsulation with Spartan-3™ FPGAs. The multi-client protocol support in Virtex-II Pro and Virtex-II Pro X high-speed RocketIO™ transceivers enables seamless communication with protocols operating at up to 10.3125 Gbps. Coupling this technology with the embedded PowerPC™ processor enables not only client adaptation, but also real-time control and processing capabilities within a single FPGA.

| FRAME MAP PROTOCOLS | TRANSPARENT MAP PROTOCOLS |
|---|---|
| Ethernet | Fibre Channel |
| PPP | Gigabit Ethernet |
| RPR (IEEE 802.17) | ESCON |
| FC-BBW | DVB ASI |
| Multiple-Access Protocol Over SDH (MAPOS) | FICON |
| | Asynchronous FC |

*Table 1 – Client network protocols supported by GFP*

Implemented on these platforms and combined with a suite of additional Xilinx intellectual property, the new GFP core provides a fully configurable way to implement custom solutions that can dynamically adapt in a rapidly changing environment.

## The GFP Specification

The GFP uses an octet-based stream of data that maps directly into an octet-synchronous stream, such as synchronous optical network/synchronous digital hierarchy (SONET/SDH). GFP frames are scrambled to ensure DC balance and running disparity, and they are delineated by using a length field within the core header, as shown in Figure 1.

Because the start and end of the frame is embedded within the GFP stream, synchronization of the two GFP end-points must first occur to ensure that data can be transmitted. Synchronization at an individual end-point is achieved by the detection of a correct CRC over the core header, then using the length field to point to the start of the following frame. Once this process is successfully repeated a programmable number of times, the GFP stream is synchronized, and data can be transmitted.

Some aspects of the GFP protocol are common to all implementations. This includes options such as frame delineation and synchronization; CRC insertion/detection/correction; and scrambling.

In addition to the common aspects of the GFP protocol, client-specific functions are required to handle unique differences in protocol mapping. This includes options specific to the two types of client data mapping: frame-mapped (GFP-F) and transparent-mapped (GFP-T). Table 1 lists all of the GFP-F and GFP-T protocols supported in the G.7041 specification.

GFP-F supports variable-sized packet lengths of framed data, where one client frame (such as an Ethernet frame) maps directly into one GFP-F frame. This requires a media access controller (MAC) in the system to terminate the Layer 2 protocol. In Ethernet, for example, an Ethernet MAC removes the preamble and start of frame delimiter, checks the CRC, and passes the Ethernet frame to the GFP end-point for encapsulation.

GFP-T supports fixed-sized packet lengths and transports block-coded constant rate bitstreams (such as Fibre Channel, Ethernet, or ESCON/SBCON). This generates a GFP frame that encapsulates block-coded data, which contains the client protocol 8B10B data and control (symbols) that are mapped to 64B65B block codes.

The transparent-mapped protocol does not require that application buffers complete frames before transmission. Instead, both data and control symbols are accumulated. Eight 8B/10B symbols (plus a flag bit) are combined to create a 64B/65B block code. This block code will include both data words and control characters.

Eight 64B/65B block codes are then combined to create superblocks (65 bytes of data + CRC16). Multiple superblocks are combined to create the GFP payload, where the number of superblocks per frame is protocol-specific (95 for Gigabit Ethernet and 13 for Fibre Channel). GFP-T does not require MAC functionality, as it is notionally transparent to the protocol transmitted.

The selection of GFP-F versus GFP-T depends on the application and system requirements. GFP-F provides bandwidth

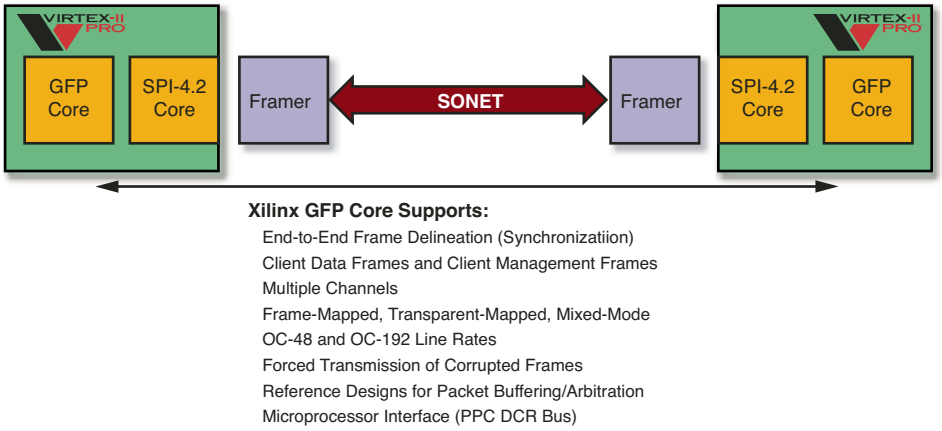


*Figure 2 – Features supported by the Xilinx GFP IP core, enabling system solutions*

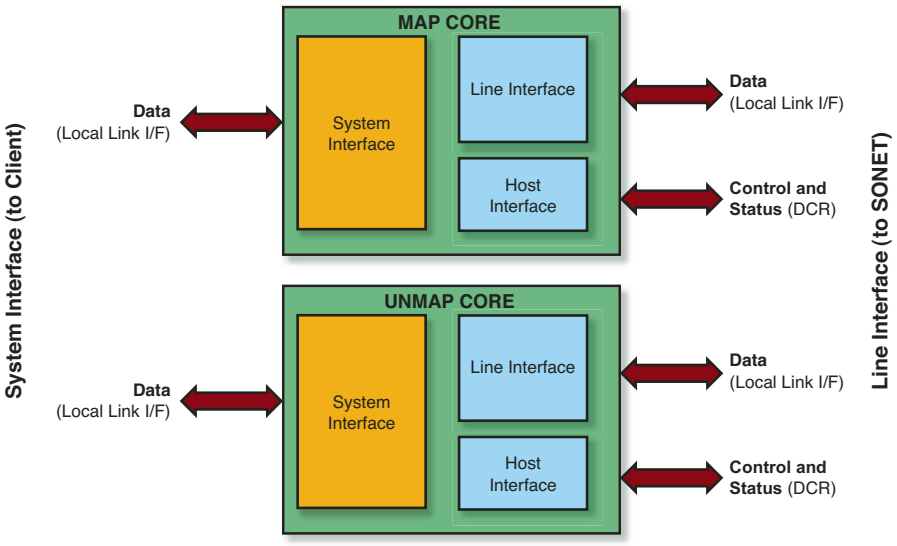


*Figure 3 – Block diagram of GFP IP MAP and UNMAP core interfaces*

efficiency by ensuring that only actual data is transmitted, whereas GFP-T transmits all information including data, framing codes, preamble, and idles.

GFP-F incurs higher latency through the system, because complete frames must be buffered before transmission. This may imply the use of external memory, depending on the system.

GFP-T does not require complete frame transmission, and therefore can achieve lower system latencies. In practice, transmission over long distances will incur a latency (due to the medium) that requires additional functionality in the client adaptation layer to ensure that the protocols' latency requirements are met. This is called "spoofing" and is critical for some client protocols, such as Fibre Channel, where strict latency requirements exist.

## Xilinx GFP Core

Xilinx offers a GFP IP core solution that supports all of these protocols and fully implements the G.7041/Y.1303 specification defined by the ITU-T. This includes system-level capability of end-to-end frame delineation, support for both client management and data frames, and configuration of frame or transparent mapping on a per-channel basis. In addition to supporting all of the features specified by G.7041, the Xilinx solution also provides options to facilitate system-level integration and debugging.

With the Xilinx CORE Generator™ tool, you can easily configure the GFP core to support your system requirements, selecting one of three operating modes: frame-mapped, transparent-mapped, or mixed mode. Mixed mode enables you to specify on a per-channel basis whether the channel is frame- or transparent-mapped. You can also change the mode through the GFP host interface.

The core also provides optional support for linear extension headers, which can be configured for as many as 10 unique channels. You can select an optional generic host interface that enables you to modify the control and status registers in real time. Some of the key system features of the GFP core are highlighted in Figure 2.

Using the CORE Generator system, you can fully customize the behavior of the core. A specific configuration determines how the core processes frames and also determines the resources required for implementation. The composition of a frame and the options provided are illustrated in Figure 1.

The GFP core is split into a MAP core and an UNMAP core, as illustrated in Figure 3. The MAP core receives client network protocol data (such as Ethernet) on the system interface, encapsulates this data, and transmits the resulting frames on the line interface (such as SONET).

The UNMAP core does the same process in reverse, receiving encapsulated data on the line interface and de-mapping the frames to extract client network protocol data, which is in turn transmitted on the system interface. The GFP core utilizes the Xilinx LocalLink interface standard on the line and client interfaces for direct connection to other cores and reference designs.

In frame-mapped mode, the client supplies the MAP core's system interface with a complete data frame, which is then transmitted without pause. In the transparent mapped mode, the MAP core automatically handles underflow by inserting pad words into the frame so that the client does not have to provide uninterrupted frames of data.

Each core has a host interface (a PowerPC™ device control register [DCR]

bus) that provides access to a bank of control and status registers. If you only require the default control signals, you can configure the core without status registers to reduce the number of resources.

### Xilinx Complete Solutions

Xilinx provides a complete and versatile solution that allows you to configure the FPGA for your system needs. A myriad of applications exist for GFP, and the architecture and requirements of the system will drive any given set of requirements.

For example, if you are utilizing a framer that is GFP-aware, you can configure the GFP core to enhance the framer by supporting options that the framer does not. Common examples of this include channelization using the linear extension header, or transparent map mode.

If the application is using a framer that is not GFP-aware, you can configure the GFP core to perform all GFP functionality, including frame delineation and synchronization, CRC, and scrambling. Using CORE Generator software enables you to specifically craft the implementation that meets your requirements, and thus minimize the resource utilization of the FPGA.

In addition to the GFP core, other Xilinx solutions enable the implementation of a complete system to transfer Ethernet or Fibre Channel over SONET. Some of these additional solutions are illustrated in Figure 4 and described below:

- Configurable PCS (CPCS) Xilinx application note XAPP739 demonstrates how to utilize Virtex-II Pro MGTs by providing a configurable PCS for a suite of protocols (FC [1G, 2G], ESCON/SBCON, and GE). It dynamically controls the PCS mode on each port, using the PowerPC and scales to support as many as eight channels in both transparent and frame map modes.
- The System Packet Interface level 4 phase 2 (SPI-4.2) IP solution provides a fully compliant core to address the data path connectivity between POS (Packet Over SONET) physical layer devices and link layer devices in networking and communications systems. The SPI-4.2 core offers support for a resource-optimized OC-48 (2.5 Gbps) interface and a high-performance (greater than 14 Gbps) interface to connect network processors with OC-192 framers and mappers, as well as gigabit and 10 Gigabit Ethernet data-link MACs.
- The 1GE MAC IP core solution provides a half- and full-duplex 1 Gbps MAC controller designed to IEEE 802.3-2002. The MAC core performs the link function of the Gigabit Ethernet standard. The core can interface to an off-chip PHY using the core's gigabit media independent interface (GMII). Alternatively, it can be delivered with an integrated 1000BASE-X PCS with a ten-bit interface (TBI), or a 1000BASE-X PCS and PMA using the integrated RocketIO transceiver in Virtex-II Pro devices.
- The buffer manager reference design demonstrates how to interface to external DDR-RAM to buffer data on a per-channel basis.
- The Fibre Channel reference design demonstrates some of the specific requirements for transmitting Fibre Channel over a SONET/SDH network outside of the GFP specification. This includes an example flow control mechanism that address the latency-sensitive Fibre Channel requirements.
- Xilinx reference design XAPP695 demonstrates an example sub-system integration in Virtex-II Pro devices for a multi-channel Gigabit Ethernet to SPI-4.2, complete with PowerPC control plane. This topic was covered in the Summer 2004 issue of the *Xcell Journal*, in the article, "Ethernet Aggregation of GFP Framing in Virtex-II Pro." The design does not include the core described here.

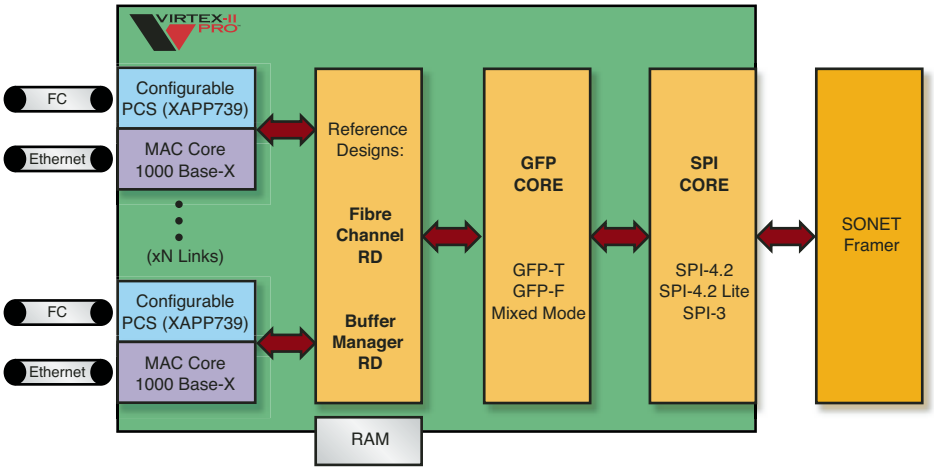


*Figure 4 – A GFP application example of Ethernet over SONET and FC over SONET*

### Conclusion

The Virtex-II Pro family of FPGAs provides a powerful, flexible platform for implementing networking solutions. The high-speed serial MGTs and PowerPC, combined with proven IP cores and reference designs, provide pre-verified solutions for managing and transporting a wide variety of data protocols.

The ITU-T GFP specification provides a flexible and efficient mapping of these data protocols onto a transport network. Using Xilinx Virtex-II Pro FPGAs combined with the GFP core, you can quickly and reliably apply this new technology to your SONET/SDH systems and implement a solution crafted to address your specific system requirements. For more information, visit *www.xilinx.com/products/design_resources/conn_central/index.htm.* Σ

# Designing Next-Generation Wireless Systems

An FPGA-centric approach using XtremeDSP and serial RapidIO solutions.

by Narinder Lall
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Xilinx, Inc.
*narinder.lall@xilinx.com*

The demands of next-generation wireless infrastructures require system designers to address not only processing bottlenecks but connectivity bottlenecks. Xilinx® FPGAs provide the ideal mix of high-performance DSP to handle the most demanding chip-rate and radio algorithms and serial MGTs, addressing high-speed connectivity and interoperability challenges.

Tomorrow's wireless infrastructure equipment designers will face an increase in algorithmic complexity and data rate brought on by the convergence of data, video, and voice. Solutions based on discrete devices such as microprocessors, DSPs, and transceivers provide tremendous headaches related to interoperability and latency, and can quickly drive up both cost and power per channel.

An FPGA-centric approach that combines Xilinx high-performance DSP capability and serial RapidIO™ (SRIO) will help alleviate some of these system performance bottlenecks and provide an integrated solution that better meets economic and energy constraints. In addition, an FPGA-centric approach allows you the flexibility to recover from mistakes and make hardware changes even after system deployment, thereby reducing overall design risk.

## The DSP Industry Embraces SRIO

Figure 1 shows that in the late 1990s, GSM systems that provided voice communications only supported terminal data rates below 10 kbps. In contrast, W-CDMA systems, which started rolling out in 2002, needed to support voice, data, and video, and hence used 2 Mbps data rates. Future systems such as W-CDMA (HSDPA) and CDMA2000 (1xEV-DO and DV) will use data rates greater than 2 Mbps.

Designers have implemented ASICs – and more increasingly FPGAs – in wireless systems to handle digital radio (modulation/demodulation, DDC/DUC) and high-chip-rate processing. FPGAs exploit parallel processing techniques through hard-wired embedded multipliers and provide you with the flexibility to make algorithmic changes even after system deployment, saving millions in maintenance or field upgrade costs.

Second, the need to transport such high information packets presents new connectivity challenges. Traditional buses are fast running out of bandwidth. Wide parallel buses are becoming too complicated to design and increasingly difficult to scale. As serial I/O technology begins to mature, wireless infrastructure equipment designers are looking towards system interconnect architectures based on MGTs to handle their transport problems. This gives rise to potential chip-to-chip and board-to-board interoperability headaches for system designers.

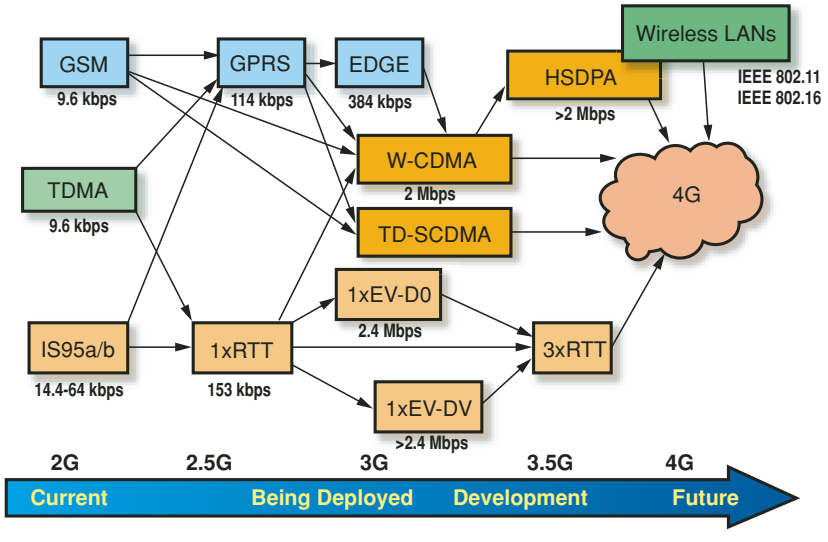



*Figure 1 – Mobile technology roadmap*

What is encouraging is that leading DSP IC suppliers that supply chip-rate and symbol-rate processing solutions (such as Texas Instruments™, Motorola™, and Xilinx) are at the forefront of the SRIO revolution and are keen to address connectivity and interoperability challenges in next-generation wireless infrastructure systems.

DSP processor vendors are projected not to start sampling products for some time, but as a system designer, you can start your development today using Xilinx Virtex-II Pro™ FPGAs, which incorporate high-performance DSP capability, SRIO connectivity, and even control functions through embedded PowerPC™ 405 processors.

As chip-rate processors, FPGAs provide an ideal complement to DSP processors, which have traditionally been used for lower sample- and symbol-rate processing.

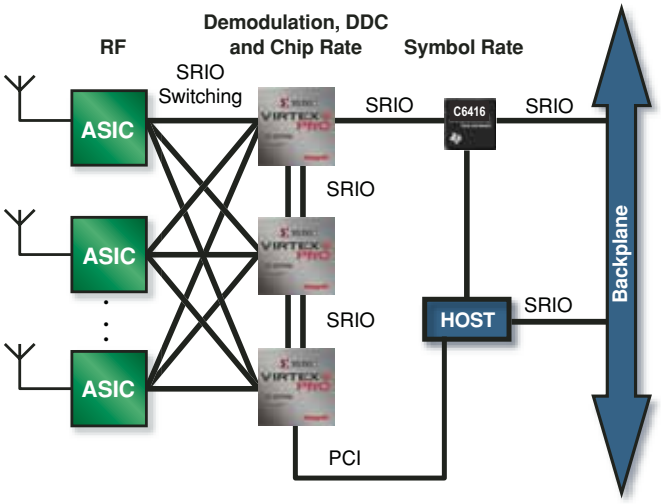



*Figure 2 – Serial RapidIO usage example in wireless infrastructure*

## SRIO Benefits Using Virtex-II Pro FPGAs

Serial RapidIO technology using Virtex-II Pro FPGAs provides a number of benefits to wireless infrastructure equipment designers:

- High-performance throughput provides the necessary bandwidth to cope with next-generation data transport needs.
- Lower complexity software and an ability to complete peer-to-peer transactions simplifies systems. In addition, it also provides a well-defined mechanism for congestion control.
- A flexible, low-risk solution offers scalable bandwidth options for future demands and fast time to market.
- With many DSP and other system IC (microprocessor, ASIC) vendors committing to SRIO, designers will have architectural flexibility. Virtex-II Pro FPGAs can provide interoperability security.
- Lower system cost through the use of a small silicon footprint and high bandwidth efficiency.

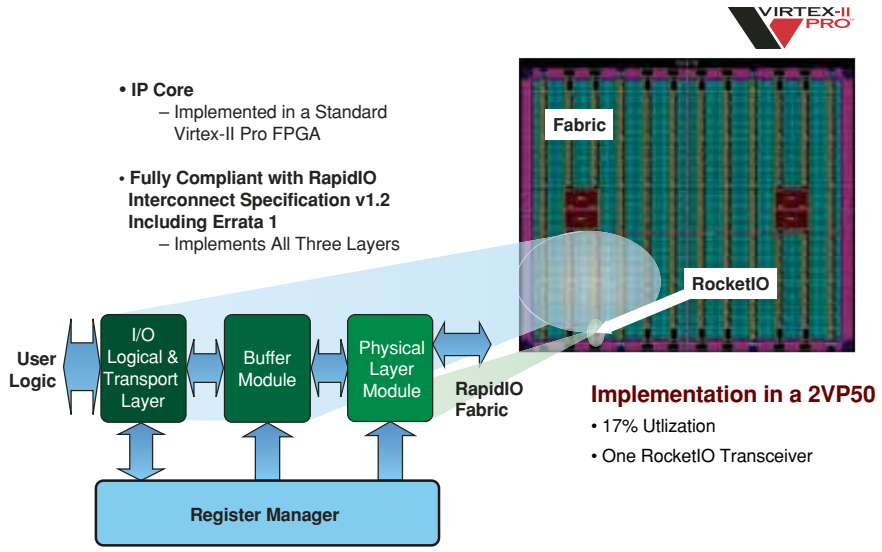



*Figure 3 – Xilinx Serial RapidIO endpoint*

## Combining Xilinx XtremeDSP and SRIO Technology

The availability of SRIO-based ASICs, FPGAs, and DSPs gives you a number of options for implementing your wireless infrastructure systems. One such implementation could use a Virtex-II Pro FPGA solely as a central switch between chip and symbol-rate devices.

A more integrated option (shown in Figure 2), based on distributing the switching to multiple Virtex-II Pro devices that can also handle high-performance DSP for multi-channel radio and chip-rate processing, provides a more integrated, cost-effective approach.

Xilinx high-performance DSP capability lies at the heart of much of today's second- and third-generation wireless infrastructure equipment. In addition to hundreds of 18 x 18 embedded multipliers for implementing custom algorithms, you can also use Xilinx DSP IP cores for demanding functions such as digital up/down conversion and forward error correction (such as 3GPP2 TCC, TPC decoding, and Viterbi decoding). You can find out more about the Xilinx XtremeDSP™ solution by visiting *www.xilinx.com/dsp/*.

## Conclusion

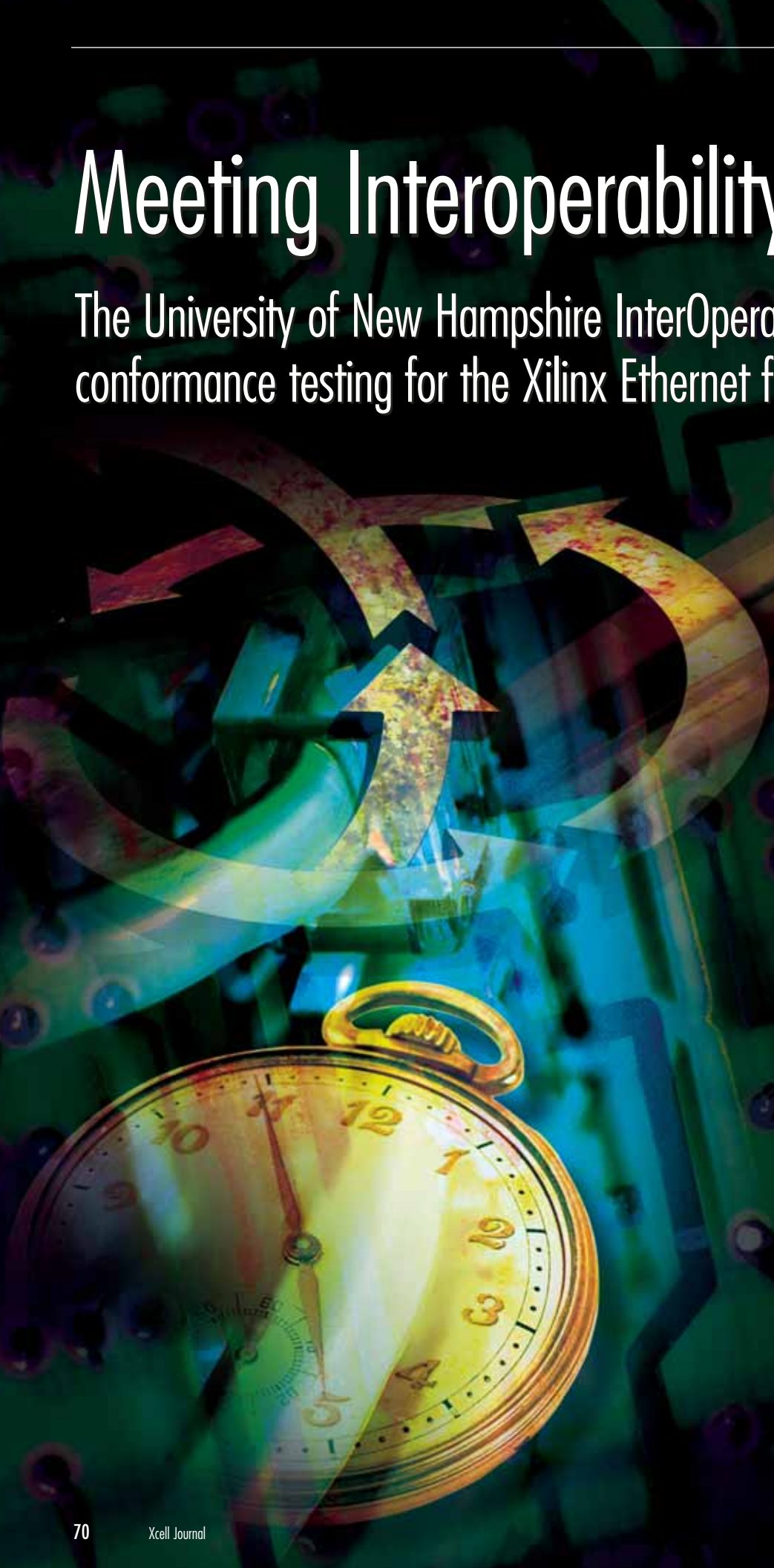
With the addition of SRIO technology, Xilinx Virtex-II Pro FPGAs provide system designers with another means to further enhance system throughput, lower cost-per-channel, and retain the flexibility of an FPGA-centric solution.

Figure 3 shows that the Xilinx Serial RapidIO IP core provides a complete endpoint solution comprising transport, logical, and physical layers, and also complies with Revision 1.2 of the specification, including Errata 1. It supports all recovery mechanisms: packet retry, stomp, link request, and CRC.

For more information on the Xilinx Serial RapidIO core, visit *www.xilinx.com/rapidio/*.

# Meeting Interoperability Standards

## The University of New Hampshire InterOperability Lab completes conformance testing for the Xilinx Ethernet family.



by Sam Sanyal
Solutions Marketing Manager
Xilinx, Inc.
*sam.sanyal@xilinx.com*

**Conformance tests are one of the most important items for embedded platforms like the Xilinx® Virtex™ and Spartan™ family of FPGAs. As these platforms are built on multiple building blocks, using standards-based technology that is independently tested addresses key issues such as accelerated time to market and interoperability. Getting Xilinx products tested also demonstrates our commitment to the technology.**

**Xilinx is the first FPGA vendor in the industry to meet the University of New Hampshire (UNH) IEEE 802.3 standard for Xilinx 10/100, 1 Gbps, and 10 Gbps MAC conformance tests. The UNH InterOperability Lab (IOL) tests are key in establishing our product line, winning designs, and building customer confidence.**

**Adhering to standards and undergoing testing by reputable organizations like the UNH IOL ensures interoperability between systems, networks, and applications. Because enterprises have the flexibility to choose best-in-class solutions, conformance testing fosters competition and innovation between solution providers.**

A successful UNH conformance test is a confidence builder that ensures project success in the shortest possible development time.

### Why UNH IOL Conformance?

The UNH IOL has the longest history of fostering interoperability and conformance in connectivity technologies. Through their independent testing methodology and relationships with major corporations and industry engineers, numerous companies have refined their technologies and extended their products' compatibility.

Specification standards are established in the hope that products from different vendors can interoperate with each other; for example, that two Ethernet cards purchased from two different vendors will communicate. This enables you to choose the system that best meets your needs for each application.

In the past, some vendors made claims of interoperability that were not quite achieved. However, this is not the case anymore; a number of vendors have successfully tested interoperability together at the UNH IOL. The limitations are better addressed through their tests.

A successful UNH conformance test is a confidence builder that ensures project success in the shortest possible development time.

The UNH IOL features:

- A neutral environment. A win-win situation for everyone involved, neutrality is achieved by using standard test beds, methodologies, and tools.
- Industry involvement. The IOL's participation in various trade associations and standards organizations keeps the lab appraised of the latest developments in technology. In turn, the IOL effects positive change in standards organizations by providing technical contributions, editorial assistance, verification, and feedback during standards development.
- Enhanced image and visibility. The UNH IOL testing consortium's relationship with industry leaders (Cisco Systems™, Broadcom™, Cadence™, Dell™, HP™, Conexant™, Brocade™, and 3Com™) works as an indirect advertising tool for your products.
- Excellence in testing services. Through industry-recognized standardized and custom test suites, expertise, advanced testing facilities and equipment, open and widely reviewed testing procedures for both conformance and interoperability testing creates confidence in your product with plug-and-play capability in a heterogeneous network.

### Test Routines

Many more tests are available from the UNH IOL, but the tests listed here were performed on Xilinx devices.

**Tests Configuration for 10/100**

MAC conformance testing included the following test suites:

- Collision Detect/Enforcement Test (Half Duplex)
- Collision Detection Timing Sensitivity Test (Half Duplex)
- Late Collision Detection Test (Half Duplex Only)
- Retransmission Attempt Limit Test (Half Duplex Only)
- Collision Backoff Algorithm (Half Duplex Only)
- No Collision Test (Full Duplex Only)
- FCS Error Test
- Alignment Error Test
- Fragment/Runt Test
- Large Frame Test
- Jabber Frame Test
- Received Preamble Test
- Start of Frame Delimiter Test
- Frame Length Test
- Minimum Received Inter-Frame Gap
- Transmit Preamble Test
- Minimum Transmitted Inter-Frame Gap
- Defer to Carrier Sense While Frame Waiting
- Deference after Collision
- Do Not Defer Test (Full Duplex)

Flow control conformance testing included the following test suites:

- Receive PAUSE Frame with Zero pause_time
- Receive PAUSE Frame with Non-Zero pause_time
- Resume Transmission
- Discard Invalid PAUSE Frames
- Receive JUMBO MAC Control PAUSE Frames
- Receive RUNT MAC Control PAUSE Frames
- Receive MAC Control PAUSE Frames with Incorrect CRC
- PAUSE Frame Transmission

PCS conformance testing included the following test suites:

- End of Stream Delimiter Test
- Invalid Data Symbol Test
- False Carrier Detect

Figure 1 shows a block diagram of the test setup of an Insight Virtex-II™ (DS-BD-V2MB1000) board with a P160 communications module (DS-BD-MBEXF1).

**Tests Configuration for 1 Gbps**

The Figure 2 block diagram of the test design based on the ML320 platform makes use of the PowerPC™ processor in Virtex-II Pro™ devices as well as an inter-

nally developed asynchronous FIFO and with firmware developed in C.

MAC conformance testing included the following nine test suites:

- Frame with FCS Errors
- Fragments and Runts
- Transmit Proper SFD and Preamble
- Receive Variable Preamble
- Does Not Defer
- No Collisions
- No Extension
- No Bursting
- Transmission of Minimum Inter-Frame Gap

Flow control conformance testing included the following five test suites:

- Receive PAUSE Frame with Zero pause_time
- Receive PAUSE Frame with Non-Zero pause_time
- Resume Transmission
- Receive PAUSE Frames of Incorrect Size
- PAUSE Frame Transmission

The UNH IOL also performed PCS, Auto-Negotiation, and Point-to-Point Interoperability tests.

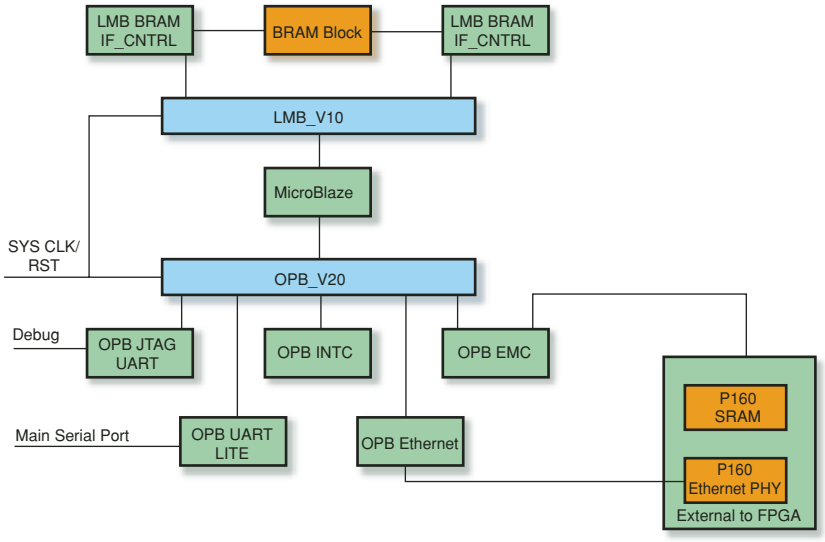



*Figure 1 – Tests Configuration for 10/100*

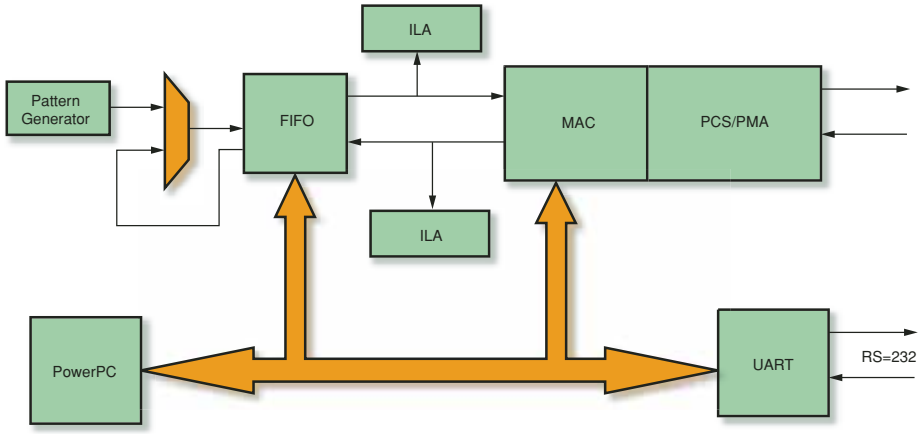



*Figure 2 – Tests Configuration for 1 Gbps*

**Tests Configuration for 10 Gbps**

The UNH IOL performs MAC tests on the frame reception and frame transmission. The frame reception tests cover MAC operations specific to reception of frames, designed to verify that the device under test (DUT) properly receives valid frames, discards frames with errors, and reports these errors if possible. The test setup was done according to the block diagram shown in Figure 3.

The UNH IOL performed these specific tests on the Xilinx DUT:

- Frames Greater than Max Frame Size
- Frames with Length Errors
- Receive All Frame Sizes 64-1518 (or 1,522) Bytes

The frame transmission tests cover MAC operations specific to the transmission of MAC frames, designed to verify that the DUT transmits properly formed MAC frames.

They also performed these specific tests on the DUT:

- Transmit Proper Length within the Length/Type Field
- Compute and Transmit Proper CRC
- Transmission of Minimum Inter-Frame Gap

Figure 3 shows the setup used throughout the testing process. An arbitrary waveform generator (AWG) is used to generate the required clock signals. A PC communicated with the testing station using National Instruments'™ LabView software, to download firmware for the DUT and access Xilinx ChipScope™ embedded logic analyzers.

The XGMII interface of the DUT was used to provide access below the MAC layer in all test cases. Using multiple ChipScope embedded logic analyzers for bus monitoring and a transmit frame generator module obtained access above the MAC layer.

Reconciliation sublayer tests are designed to verify that the DUT reacts properly to the receipt of data, both valid and invalid, at the reconciliation sublayer.

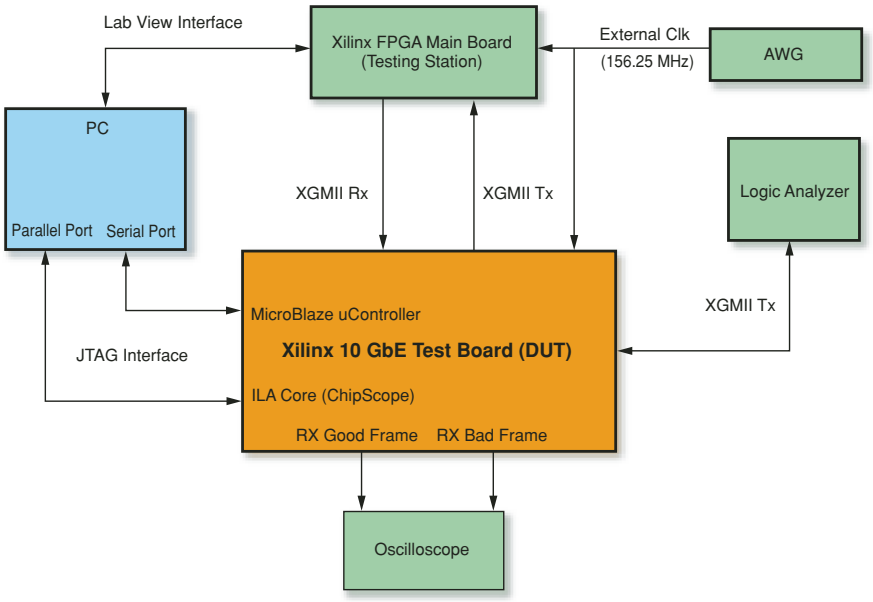



*Figure 3 – Tests Configuration for 10 Gbps*

The UNH IOL performed these specific tests on the DUT:

- Start Control Character Creation and Alignment
- Reception of Start Control Character
- Reception of Preamble and SFD
- Reception of Terminate Control Character
- Assertion of DATA_VALID_STATUS
- Reception of /E/ during DATA_VALID_STATUS
- Continuous Reception of Fault Sequences
- Reception of Identical Fault Sequences
- Reception of Non-Identical Fault Sequences
- Setting of col_cnt

## The Value Proposition

Xilinx is the industry's only FPGA vendor that has its complete Ethernet IP product family neutrally tested to IEEE 802.3 standards conformance and interoperability. These tests on the Ethernet IP product family of 10/100, 1 Gbps, and 10 Gbps speeds ensure the following value proposition:

- Proven interoperability with industry-standard equipment
- Reduced hardware testing burden for customers
- First-time design success and seamless operation (such as plug-and-play)

This invaluable approval builds customer confidence with low risk and accelerated time to market, while conformance testing also shows the company's commitment to quality.

## Conclusion

Understanding interoperability is the key to market acceptance and opportunity. Interoperability means plug-and-play operation that works within your environment and application, independent of who provided the product.

The UNH IOL Consortium acts as an extension of research and development labs, helping members test their products for conformance to industry standards and interoperability between devices from different manufacturers.

Xilinx is the only FPGA vendor to successfully bring the complete Ethernet solution to the market with the certification of the UNH IOL. With proven interoperability, you can confidently built a system for first-time design success, meet your design goals, and accelerate time to market instead of worrying about the underlying infrastructure.

For more information, visit *www.xilinx.com/systemio/interop.index.htm.*

# Xilinx Events and Tradeshows

**Xilinx participates in numerous trade shows and events throughout the year. This is a perfect opportunity to meet our silicon and software experts, ask questions, see demonstrations of new products and technologies, and hear other customers' success stories with Xilinx products.For more information and the most up-to-date schedule, visit *www.xilinx.com/events/*.**

## Worldwide Events Schedule

### North America

| | |
|---|---|
| July 20-21 | Nuclear and Space Radiation Effects Conference (NSREC) Atlanta, GA |
| September 14 | Mentor Graphics EDA Tech Forum Ottawa, ON |
| September 14-15 | Embedded Systems Conference Boston, MA |
| September 27-30 | Global Signal Processing Expo (GSPx) Santa Clara, CA |
| October 18 | Mentor Graphics EDA Tech Forum San Jose, CA |
| October 18-20 | Convergence Detroit, MI |

### Europe

| | |
|---|---|
| 17 July | Mentor Graphics EDA Tech Forum Munich, Germany |
| 6 October | Mentor Graphics EDA Tech Forum Reading, UK |
| 20 October | Boundary-scan Design For Test (DFT) European Seminar Series Frankfurt, Germany |

### Asia Pacific

| | |
|---|---|
| 13 August | Mentor Graphics EDA Tech Forum Shanghai, China |
| 16 August | Mentor Graphics EDA Tech Forum Beijing, China |
| 18 August | Mentor Graphics EDA Tech Forum Singapore |
| 20 August | Mentor Graphics EDA Tech Forum Bangalore, India |
| 24 August | Mentor Graphics EDA Tech Forum Hsin Chu, Taiwan |
| 2 September | Mentor Graphics EDA Tech Forum Seoul, South Korea |

### Japan

| | |
|---|---|
| 26-27 August | Mentor Graphics EDA Tech Forum Tokyo |
| 31 August | Mentor Graphics EDA Tech Forum Kyoto |

# Xilinx Partner Yellow Pages

## Xilinx Alliance EDA Members and Products

**AccelChip**
*www.accelchip.com*
High-level synthesis tools that read MATLAB and output RTL

**Alatek**
*www.alatek.com*
Hardware acceleration (HES)

**Altium**
*www.altium.com/nexar/*
Low cost, system level tool for targeting Spartan™ series FPGAs

**Ansoft**
*www.ansoft.com*
High-frequency products for system analysis, circuit design, and electromagnetic simulation (Ansoft Designer™, HFSS™)

**Apache Design**
*www.apache-da.com*
HSPICE®-compatible simulator using actual S-parameter data (NSPICE) for Virtex-II Pro™ MGT-based PCB design

**Aptix**
*www.aptix.com*
ASIC emulation (Prototype Studio™)

**Atrenta**
*www.atrenta.com/partners/index.htm#xilinx*
RTL Linter technology for Virtex™-II and Virtex-II Pro FPGAs (SpyGlass®)

**Auspy**
*www.auspy.com*
FPGA partition (APS II) and ASIC emulation (ACE Compiler)

**Cadence Design Systems**
*www.cadence.com*
Virtex-II Pro MGT support for high-speed PCB design (Allegro® PCB SI); NCSim family for FPGA design simulation; NC-Protect support for Xilinx EDK IPs

**Celoxica**
*www.celoxica.com*
C-level design creation, compilation, and verification for Virtex-II™ and Virtex-II Pro FPGAs

**Endeavor**
*www.endeav.com*
Co-verification for Virtex-II Pro (CoSimple™)

**EVE**
*www.eve-team.com*
RTL-level simulator accelerator (ZEBU)

**Forte Design**
*www.forteds.com*
HLL compiler to RTL (Cynthesizer); timing specification and analysis tool (TimingDesigner)

**MAGMA**
*www.magma-da.com*
Architecture-specific synthesis and layout optimization for Virtex-II series FPGAs (PALACE™ and Blast FPGA™)

**The MathWorks**
*www.mathworks.com*
System-level design tools for FPGA and processor-based signal processing systems

**Mentor Graphics**
*www.mentor.com*
Virtex-II Pro MGT support for high-speed PCB design (HyperLynx™, ICX™, Tau™); complete FPGA design flow using the ModelSim® family of simulators and Precision® RTL and Precision Physical synthesis; Seamless® co-verification support for Virtex-II Pro; FPGA symbol generation for fast PCB design iterations for Virtex-II and Virtex-II Pro FPGAs (IO Designer)

**Novilit**
*www.novilit.com*
Design partitioning using ISE EDK (AnyWare) for Virtex-II and Virtex-II Pro FPGAs

**Product Acceleration Inc.**
*www.prodacc.com*
FPGA symbol generation (LiveComponent™); automated pin assignment optimization for PCB layer and via count control (DesignF/X)

**Simucad**
*www.simucad.com*
Verilog simulator for FPGAs (Silos)

**Synopsys**
*www.synopsys.com*
Virtex-II Pro multi-gigabit transceiver support for high-speed PCB design (HSPICE); DC FPGA RTL synthesis for Virtex series and Spartan-3™ family FPGAs; VCS™(MX)/Scirocco™(MX) simulators; Formality® formal verification, LEDA® RTL linter, and PrimeTime™ static timing analysis

**Synplicity**
*www.synplicity.com*
RTL synthesis (Synplify®), RTL level debugger (Identify™), physical synthesis (Amplify®), and ASIC prototyping (Certify®) for Xilinx FPGAs

**Impulse C**
*www.impulsec.com*
C language hardware/software co-development tool for Xilinx FPGAs (CoDeveloper™)

**Summit Design**
*www.summit-design.com*
Capture and verify designs in C/C++ or SystemC (Visual Elite™)

**ProDesign**
*www.uchipit.com/ce/index.htm*
FPGA prototyping system (CHIPit™)

# Xilinx AllianceCORE Third-Party IP Providers and Products

**4i2i Communications Ltd.**
*www.4i2i.com*
Video coding, modems (OFDM), error correction

**Amirix Systems, Inc.**
*www.amirix.com*
Embedded systems

**Amphion Semiconductor, Ltd.**
*www.amphion.com*
DSP, wireless communications, and multimedia cores

**Avnet Design Services**
*www.ads.avnet.com*
Strong-ARM to PCI bridge, SDRAM controller

**Barco-Silex**
*www.barco-silex.com*
DSP cores, with a specialization in image-audio applications

**Calyptech Design Services**
*www.calyptech.com*
Packet over SONET, ATM, xDSL

**CAST, Inc.**
*www.cast-inc.com*
General-purpose IP for processors, peripherals, multimedia, networking, encryption, serial communications, and bus interfaces

**Crossbow Technologies, Inc.**
*www.crossbowip.com*
System Interconnect IP for on-chip and chip-to-chip multiprocessing

**Deltatec S.A.**
*www.deltatec.be/*
IP and services for digital imaging, DSP, multimedia, PCI, and datacom

**Derivation Systems, Inc.**
*www.derivation.com*
IP cores for high-assurance hardware/software applications and embedded systems products; 32-bit Java processor core

**Digital Communications Technologies, Ltd.**
*www.dctl.com*
Embedded Java solutions

**Digital Core Design**
*www.dcd.pl*
Microprocessor, microcontroller, floating point, and serial communication controller cores

**Dolphin Integration**
*www.dolphin-integration.com*
Bus interface, processor, peripheral, and DSP cores; EDA software

**Duma Video, Inc.**
*www.dumavideo.com*
Digital video, AES/EBU audio, MPEG and DCT cores; real-time MPEG-2 HD and SD compression

**eInfochips Pvt. Ltd.**
*www.einfochips.com*
PCI, USB, 80186, multimedia, and wireless cores

**Eureka Technology**
*www.eurekatech.com*
Silicon-proven IP for CPU interface, PCI, PCMCIA, memory control, and other peripheral functions for SoC designs

**GDA Technologies, Inc.**
*www.gdatech.com*
Hypertransport, PCI, Ethernet, design services

**HCL Technologies, Ltd.**
*www.hcltechnologies.com*
IT services and product engineering companies with a focus on technology and R&D outsourcing

**Helion Technology Limited**
*www.heliontech.com*
Encryption and DSP algorithms; design services

**iCoding Technology, Inc.**
*www.icoding.com*
Turbo Code-related error correction products including system design

**Intelliga Integrated Design, Ltd.**
*www.intelliga.co.uk*
Digital automotive networks, embedded serial communications, microcontroller design

**Loarant Corporation**
*www.loarant.com*
Proprietary 16-bit RISC CPU; embedded system design

**MEET Ltd.**
*www.meet-electronics.com*
IP cores dedicated to industrial servo motor control

**Memec Design**
*www.memeccore.com*
Peripheral, bus interfaces, encryption and communications cores

**ModelWare, Inc.**
*www.modelware.com*
Datacom/telecom cores including ATM, HDLC, POS, IMA, UTOPIA, and bridges

**NewLogic Technologies AG**
*www.newlogic.com*
Cores for wireless applications including Bluetooth and 802.11

**Northwest Logic**
*www.nwlogic.com*
Networking, digital video, embedded computing

**Paxonet Communications, Inc.**
*www.paxonet.com*
Solutions for interworking metro networking technologies to SONET

**Pentek, Inc.**
*www.pentek.com*
FPGA IP cores including FFTs, digital receivers, and pulse compressions algorithms; DSP, data acquisition, software radio boards, and system solutions

**Phystream Ltd.**
*www.phystream.com*
Integrated hardware/software data processing systems, transmission (PDH, SDH, SONET), ATM, frame relay, LAN (Ethernet, FDDI), multiservice, wireless protocols

**Pinpoint Solutions, Inc.**
*www.asic-design.com*
Standards-based telecom and datacom IP; video

**QinetiQ Limited**
*www.quixilica.com*
Floating point cores, FPU for MicroBlaze™

**RealFast Intellectual Property AB**
*www.realfast.se*
Real-time systems and RTOS; operating system cores

**Robert Bosch GmbH**
*www.can.bosch.com*
Automotive; CAN

**Roman-Jones, Inc.**
*www.roman-jones.com*
Design services: data acquisition, microprocessors (embedded and off-chip), automotive, PCI, analog design, DSP, video

**SoC Solutions, LLC**
*www.socsolutions.com*
Embedded µP and software; networking, wireless, audio, GPS and handheld; peripheral cores

**SysOnChip, Inc.**
*www.sysonchip.co.kr/*
IP and products for CDMA cellular/PCS/WLL modem, FEC and Bluetooth

**Tensilica, Inc.**
*www.tensilica.com*
Configurable processors cores and development tools

**TurboConcept**
*www.turboconcept.com*
Turbo code forward error correction solutions

**Xylon d.o.o.**
*www.logicbricks.com*
Human-machine interfaces and industrial communication controllers; video

**Zuken, Inc.**
*www.zuken.co.jp/soc/*
PCI2.2,10/100 Ethernet and Gigabit Ethernet cores

## Reference Design Partners

The Xilinx Reference Design Alliance Program builds partnerships with industry-leading semiconductor manufacturers to develop reference designs for accelerating our customer's product and system time to market. The goal is to build a library of high-quality, multicomponent system-level reference designs in the areas of networking, communications, image and video processing, DSP, and emerging technologies and markets.

**Agere Systems**
*www.agere.com*

**AMCC**
*www.amcc.com*

**Analog Devices**
*www.analog.com*

**Bay MicroSystems**
*www.baymicrosystems.com*

**BitBlitz Communications**
*www.bitblitz.com*

**Broadcom Corp.**
*www.broadcom.com*

**Centillium**
*www.centillium.com*

**Cypress Semiconductor**
*www.cypress.com*

**IBM Microelectronics**
*www.ibm.com/us/*

**IDT**
*www.idt.com*

**Ignis Optics**
*www.ignis-optics.com*

**Infineon Technologies AG**
*www.infineontechnologies.com*

**Intel Corporation**
*developer.intel.com/design/network/*

**Intrinsity**
*www.intrinsity.com/home.htm*

**Micron Technology**
*www.micron.com*

**Motorola**
*www.motorola.com*

**National Semiconductor Corporation**
*www.national.com*

**NetLogic Microsystems, Inc.**
*www.netlogicmicro.com*

**Octasic Semiconductor**
*www.octasic.com*

**PMC-Sierra Inc.**
*www.pmc-sierra.com/index.html*

**Samsung Semiconductor, Inc.**
*www.usa.samsungsemi.com*

**SiberCore Technologies**
*www.sibercore.com*

**Texas Instruments**
*www.ti.com*

**TransSwitch Coporation**
*www.transwitch.com/index_flash.jsp*

**Vitesse**
*www.vitesse.com*

**ZettaCom**
*www.zettacom.com*

## XPERTS Partners

**3T BV**
*www.3T.nl/*
Design services; measurement instruments; fail-safe controlling; medical equipment, communication, and computer peripherals

**Accent S.r.l.**
*www.Accent.it/*
Complex FPGAs; SoCs; PowerPCs™; IP platforms; software, PCB, and IC foundry services, from concept to silicon

**ADI Engineering**
*www.adiengineering.com*
Reference designs; custom designs; design services focused on Intel IXA and XScale™

**Advanced Electronic Designs, Inc.**
*www.aedbozeman.com*
Design services and manufacturing support; hardware and software design for embedded systems

**Advanced Principles Group, Inc.**
*www.advancedprinciples.com*
Design services and consulting; software algorithm acceleration and application-specific computing systems

**Alpha Data**
*www.alpha-data.com*
PCI/PMC/CPCI FPGA boards; embedded applications using HDL or System Generator methodologies

**AMIRIX Systems Inc.**
*www.amirix.com*
Design services for electronic product realization; high-performance digital boards; programmable logic; embedded software

**Andraka Consulting Group, Inc.**
*www.andraka.com*
Exclusively FPGAs for DSP since 1994; applications include radar, sonar, digital communications, imaging, and video

**Array Electronics**
*www.array-electronics.de/*
SoC/FPGA/PCB designs in telecom, industrial, and DSPs; concepts; verification; prototypes; cores

**Avnet Design Services**
*www.ads.avnet.com*
Embedded processing FPGA design services; Virtex-II Pro; high-speed SERDES; IP core integration; timing closure; RLDRAM; RapidIO™

**Baranti Group Inc.**
*www.baranti.com*
Award-winning design/manufacturing firm; expertise in digital video, FPGAs

**Barco Silex**
*www.barco-silex.com*
Total solutions consisting of IP, FPGA, and board design

**Benchmark Electronics Inc.**
*www.bench.com*
EMS/JDM team; product design, support, introduction, and launch into volume production

**Birger Engineering, Inc.**
*www.birger.com*
Development of algorithms, electronics, and systems for digital imaging

**BitSim AB**
*www.bitsim.com*
Design services; DSP, video, 3G, and WLAN designs; high-speed prototyping boards

**Bottom Line Technologies Inc.**
*www.bltinc.com*
FPGA, product, and system design services; networking; data communications; telecommunications; video; PCI; signal processing; defense; aerospace

**CES Design Services @ Siemens Program and System Engineering**
*www.ces-designservices.com*
Platform-oriented SoC/FPGA/PCB and firmware design in telecom, industrial, and video processing; customized solutions; concept; verification; prototypes

**CG-CoreEl Programmable Solutions P. Ltd.**
*www.cg-coreel.com*
Design services; telecom, networking, and processor IP and designs; turnkey FPGA; RTL design/validation

**Chess iT/Embedded**
*www.chess.nl/*
Embedded hardware and software design of products and services at the chip, board, and system level

**Colorado Electronic Product Design, Inc.**
*www.cepdinc.com*
Designing embedded systems with FPGAs for DSP; interfaces for medical, consumer, aerospace, and military

**Comit Systems, Inc.**
*www.comit.com*
High-end FPGA/SoC design services, including the integration of customer-developed and third-party IP

**ControlNet India Pvt Ltd.**
*www.controlnetindia.com*
ASIC/SoC Analog/RF FPGA design services; IP development; domains: Ethernet, IEEE1394, USB, security, PCI, WLAN, Infiniband

**Convergent Design LLC**
*www.convergent-design.com*
Audio/video design for professional/consumer products

**DATA Respons ASA**
*www.datarespons.com*
Professional design and development services for embedded hardware/software solutions; FPGA/digital hardware application specialists

**Deltatec International Inc.**
*www.deltatec.be/*
Design services; digital imaging applications; broadcast video, image processing, and image synthesis

**Digicom Answers Pty. Ltd.**
*www.fpga.com.au/*
Design services; experienced FPGA resources; design-on-demand; pre-design advice; reviews and problem solving

**Digital Design Corporation (DDC)**
*www.digidescorp.com*
Design services and products; image processing; video; communications; DSP; audio; automotive; controls; interfaces

**Dillon Engineering, Inc.**
*www.dilloneng.com*
Design services; FPGA-based DSP algorithms; high-bandwidth, real-time digital signal and image processing applications

**DRS Tactical Systems West Inc. (formally Catalina Research)**
*www.catalinaresearch.com*
Design services; FPGAs for DSP, including the manufacturer of Virtex reconfigurable computing boards

**Eden Networks, Inc.**
*www.edennetworks.com*
Turnkey design services; telecom and networking designs (Ethernet, SONET, ATM, VoIP)

**Edgewood Technologies, LLC**
*www.edgewoodtechnologies.com*
Design services; FPGAs for telecom, DSP, embedded processors

**Enea Data AB**
*www.enea.se/*
Telecommunication, data communication, DSP, RTOS, automotive, defense, high-reliability, and consumer electronics design

**Enterpoint Ltd.**
*www.enterpoint.co.uk/*
Design services; development boards; video, telecommunications, military, and high-speed design

**ESD Inc.**
*www.esdnet.com*
Design services; FPGAs for embedded systems, software/hardware design, PCB layout

**Evatronix S.A.**
*www.evatronix.pl/*
Design services; FPGA design (Virtex, Virtex-E, Spartan-II); embedded systems; SoC and SoPC designs

**Evermore Systems Inc.**
*www.evermoresystems.com*
Design services; FPGA designs for communications, audio/video, wireless, and home networking

**ExaLinx**
*www.exalinx.com*
Design services; ASIC emulation for high-speed communications and wireless applications; reference designs

**Fidus Systems Inc.**
*www.fidus.ca/*
Design services; FPGAs; communications; video; DSP; interface conversions; ASIC verification; hardware; PCB layout; software; SI/EMC

**First Principles Technology, Inc.**
*www.fptek.com*
Design/assembly/test services; FPGA + PCB + DSP/processor + system; imaging; video; test; satellite telecom; control

**Flexibilis Oy**
*www.flexibilis.com*
IP development; FPGA design services; Linux™ device drivers

**Flextronics Design**
*www.flextronics.com/design/*
Complete product design and development services for high-speed communications; reconfigurable computing; imaging; audio/video; military

**GDA Technologies, Inc.**
*www.gdatech.com*
A leading services company focused on designing systems, SoC, ASIC, FPGA, and IP

**HCL Technologies**
*www.hcltech.com*
High-speed board, ASIC, and FPGA design and verification services in avionics, medical, networking/telecom, and consumer electronics

**Helion Technology Limited**
*www.heliontech.com*
Design services and IP for FPGA with a focus on data security, wireless, and DSP

**IDERS Inc.**
*www.iders.ca/*
Contract electronic engineering and EMS resource, providing complete product cycles ranging from specifications to production

**Image Technology Laboratory Corporation**
*www.gazogiken.co.jp/*
Design services; FPGAs for image processing; design tools: EDK, System Generator, and Forge

**Innovative Computer Technology**
*ictconn.com*
Digital, analog, Xilinx FPGA, and software design solutions for customers in a wide variety of industries throughout the United States

**iWave Systems Technologies Private Ltd.**
*www.iwavesystems.com*
Embedded hardware and software design; board design; FPGA and ASIC development services

**Liewenthal Electronics Ltd.**
*www.liewenthal.ee/*
Embedded systems design services; development of software and hardware including Virtex and Spartan FPGAs

**Logic Product Development**
*www.logicpd.com*
Full-service product development, including industrial design, mechanical, electrical, and software engineering

**M&M Consulting**
*hellman@mmcons.com*
Design services; imaging; video and audio designs; high-density ASIC emulation

**Memec Design**
*www.memecdesign.com/xilinx*
Focused on FPGA design for Xilinx technology, we have completed more than 1,300 designs worldwide

**Memondo Graphics**
*www.memondo.com*
Implementation of digital signal processing, communications, and image processing solutions and algorithms over Xilinx FPGAs

**Mikrokrets AS**
*www.mikrokrets.no/*
FPGA development comprising telecommunication, network communications, and embedded systems; PCB development

**Millogic Ltd.**
*www.millogic.com*
Design services and synthesizable cores; expertise in PCI, video, imaging, DSP, compression, ASIC verification, and communications

**Milstar Inc.**
*www.milstar.co.il/*
Design services and manufacturers (industrial and military specs); DSP; communication; video; audio; high-speed boards

**Misarc srl - Agrate**
*www.misarc.com*
Design services and manufacturers; telecommunications; SoC development; test equipment boards using FPGA solutions

**Multi Video Designs**
*www.mvd-fpga.com*
Design services; DSP for video, telecommuications; SoC with Virtex-II/Pro and Spartan (PowerPC/MicroBlaze); Xilinx training

**Multiple Access Communications Ltd.**
*www.macltd.com*
Design services; products and consultancy; DSP for wireless communications

**Nallatech**
*www.nallatech.com*
Embedded reconfigurable computers for high-performance applications in DSP, imaging, and defense; Xilinx Diamond XPERTS

**NetModule AG**
*www.netmodule.ch/*
Design services for system design; FPGA applications in telecommunication systems and medical electronics

**NetQuest Corporation**
*www.netquestcorp.com*
Turnkey engineering design and production services in advanced high-speed embedded communications

**North Pole Engineering Inc.**
*www.northpoleengineering.com*
Hardware and software design services for FPGA, ASIC, and embedded systems

**Northwest Logic**
*www.nwlogic.com*
PCI, PCI-X, and SDRAM controller IP; high-end FPGA design services

**NovTech Engineering**
*www.novtech.com*
Board-level and IP cores; turnkey design services; imaging; communication; PCI cores; encryption

**NUVATION**
*www.nuvation.com*
Design services; imaging and communications for defense/security, medical, consumer, and datacom/telecom markets

**Plextek Ltd.**
*www.plextek.com*
Design services; FPGA, DSP, radio, microwave, and microprocessor technologies for defense and communications

**POLAR-Design**
*www.polar-design.de/*
High-end FPGA design for telecom, networking, and DSP applications

**Polybus Systems Corporation**
*www.polybus.com*
Test patterns; customizable in-system FPGA test patterns; design services; networking and communications

**Presco, Inc.**
*www.prescoinc.com*
Twenty-five years of experience in custom electronics design/manufacturing for high-performance image processing, data communications, inkjet

**Productivity Engineering GmbH**
*www.pe-gmbh.com*
Design services; PCI design; microprocessor cores; obsolete component replacements; ASIC prototyping

**Programall Technologies Inc.**
*www.ProgramallTechnologies.com*
Design services; embedded systems targeting Virtex, Spartan, Virtex-II, and Virtex-II Pro FPGAs

**R&D Consulting**
*972-9-7673074*
FPGA development; video; imaging; graphics; DSP; communications

**Rapid Prototypes, Inc.**
*www.fpga.com*
Design services; high-performance reconfigurable FPGA applications requiring maximum speed or density using physical design principles

**RDLABS**
*www.rdlabs.com*
FPGA/ASIC design; wireless communications; 802.11b/a IP cores; MATLAB, Sysgen, ModelSim; instruments HP1661A, HP8594E, HP54520A

**RightHand Technologies, Inc.**
*www.righthandtech.com*
Design services; Virtex-II Pro FPGAs, boards, and software for video gaming, storage, medical, and wireless

**Rising Edge Technology Inc.**
*www.risingedgetech.com*
Complete design solutions from the ground up; FPGA interface designs

**Riverside Machines Ltd.**
*www.riverside-machines.com*
Design services and project management; DSP, wireless, network, and processor development; Verilog™, VHDL, SystemC™, Specman

**Roke Manor Research**
*www.roke.co.uk/*
Design services; IP, ATM, DSP, imaging, radar, and control solutions for FPGAs

**Roman-Jones, Inc.**
*www.roman-jones.com*
Design services; FPGAs for embedded microprocessors; PCI; DSP; low-cost 8051 softcore

**Sapphire Computers, Inc.**
*drudolf@voyager.net*
Engineering design consulting; high-speed digital and FPGA design

**Siemens AG, Electronic Design House**
*www.eda-services.com*
Design services; system-on-chip; ASICs; FPGAs; IPs; DSPs; boards; EMC; embedded software; prototypes

**Silicon & Software Systems Ltd. (S3)**
*www.s3group.com*
World-class electronics design company uniquely combining IC, FPGA, software, and hardware design expertise

**Silicon Interfaces America Inc.**
*www.siliconinterfaces.com*
Design services; develops IP in areas of networking, wireless, optical, datacom, interconnect, and microcontrollers

**Silicon System Solutions P/L**
*www.silicon-systems.com*
Design services; FPGAs for very high-speed applications including communications and DSP applications

**Siscad S.p.A.**
*www.siscad.it/*
Xilinx FPGA design services; IP development and integration

**Smart Logic, Inc.**
*www.smart-logic.com*
Design services; FPGAs for rapid prototyping including imaging, compression, and real-time control

**SoleNet, Inc.**
*www.solenet.net*
FPGA, board, and system designs for wireless, telecommunications, consumer, and reference design applications

**so-logic electronic consulting**
*www.so-logic.net*
Embedded systems (PowerPC, MicroBlaze); system-level design (Forge, System Generator, Handel-C); Xilinx training centers (Austria, Eastern Europe)

**Styrex AB**
*www.styrex.se/*
Design services for embedded systems; programmable logic; hardware development; microprocessor programming

**Synopsys Professional Services**
*www.synopsys.com*
Design services to solve your design challenges in system-level design, RTL design, and physical design

**Syntera AB**
*www.syntera.se/*
Design services; FPGAs for radar, digital communications, telecom automotive, aerospace, and DSP

**Tao of Digital, Inc.**
*www.taoofdigital.com*
High-speed, large-gate-count SoC designs using IP cores for maximum modularity and efficiency

**Technolution B.V.**
*www.technolution.nl/*
Innovative hardware and software solutions

**Tezzaron Semiconductor**
*www.tezzaron.com*
Design services for portable computing, networking, and embedded systems

**Thales Airborne Systems**
*www.thalesgroup.com/airbornesystems/*
Provider and integrator with high expertise in FPGA design for radars, DSP, and communications

**TietoEnator R&D Services AB**
*www.tietoenator.com*
European design services for telecom, industrial IT, and automotive; Xilinx exclusive training provider in Scandinavia

**V-Integration**
*www.V-Integration.com*
Providing first-pass success in complex FPGA designs; applications include imaging, communications, and interface design

**Williams Consulting, Inc.**
*chipw@wciatl.com*
Embedded systems hardware and software; video; MPEG; control

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See these AllianceEmbedded members for information about the following products (contact Xilinx for Wind River Xilinx Edition products):

**Accelerated Technology® Division of Mentor Graphics**
*www.acceleratedtechnology.com*
Nucleus® RTOS support for Xilinx MicroBlaze 32-bit soft processor cores

**Avnet Design Services single board computers**
*www.em.avnet.com/home/*
ADS Xilinx Virtex-II Pro Evaluation Kit

**Corelis Inc.**
*www.corelis.com*
CodeRunner JTAG debugger support for Virtex-II Pro embedded PowerPC

**Express Logic**
*www.expresslogic.com*
ThreadX® RTOS support for Xilinx MicroBlaze 32-bit soft processor

**Green Hills Software**
*www.ghs.com*
MULTI® debugger support for Virtex-II Pro embedded PowerPC; Green Hills™ Optimizing C Compiler support for Virtex-II Pro embedded PowerPC

**MEMEC Design single board computers**
*www.insight-electronics.com/virtex2pro/*
Virtex series system boards

**Micrium Technologies Corp.**
*www.ucos-ii.com*
µC/OS-II RTOS support for Xilinx MicroBlaze 32-bit soft processor core

**Mind NV**
*www.mind.be/v2p/ecos*
Mind NV eCos RTOS support for Virtex-II Pro embedded PowerPC

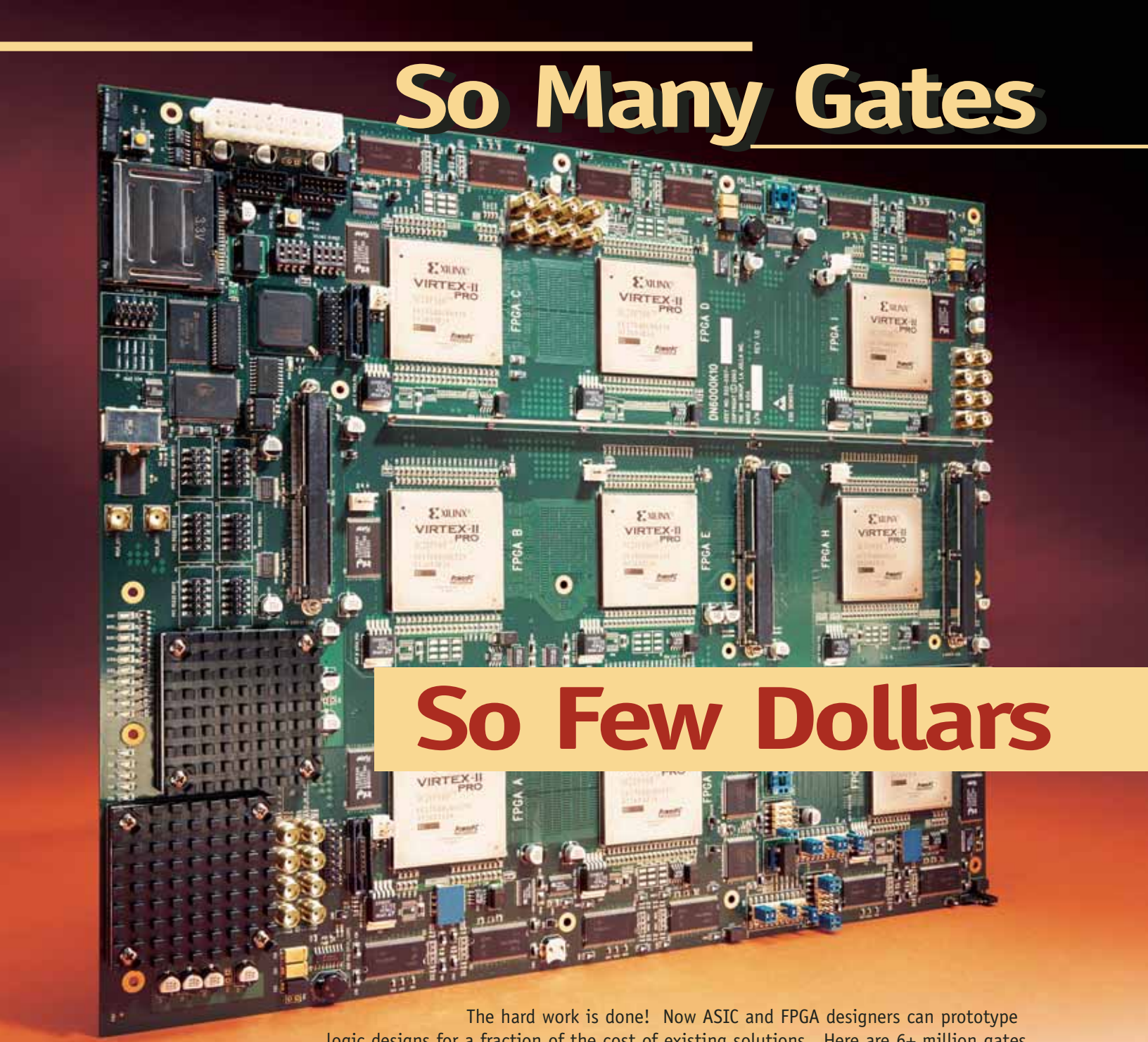
**MontaVista Software**
*www.mvista.com*
MontaVista® Linux® Professional Edition subscription support for Virtex-II Pro embedded PowerPC

**Nohau Corporation**
*www.nohau.com*
EMUL-MicroBlaze-PC debugger support for Xilinx MicroBlaze 32-bit soft processor

**QNX Software**
*www.qnx.com*
QNX® Neutrino® RTOS support for Virtex-II Pro embedded PowerPC

**Wind River Systems**
*www.windriver.com*
VxWorks® RTOS support for Virtex-II Pro embedded PowerPC; Diab™ Xilinx Edition (XE) C/C++ Compiler; SingleStep™ Xilinx Edition debugger; visionPROBE II Xilinx Edition; visionICE II Emulator; visionTRACE Emulator

# So Many Gates




# So Few Dollars

The hard work is done! Now ASIC and FPGA designers can prototype logic designs for a fraction of the cost of existing solutions. Here are 6+ million gates (measured the ASIC way) on an easy to use, stand-alone, USB2.0-hosted board (a PCI/PCI-X interface is coming soon). The DN6000k10 supports up to 9, 2vp100 VirtexII-Pro FPGA's, with an incredible amount of FPGA to FPGA interconnect for easy logic partitioning. FPGA's are interconnected with rocket I/O's, enabling the movement of data between them at 100's of GB/s. In addition to 6M+ gates, the DN6000k10 also packs on-board:

- 2 PowerPC cores per FPGA (400MHz)
- Up to 8MB embedded RAM, 444, 18x18 multipliers — per FPGA
- 12 external 133MHz 32M x 16 DDR SDRAM's, 5 4Mx16 FLASH
- 480+ connections for daughter card and logic analyzer interfaces

Configuration is fast, easy, and robust using a SmartMedia-based FLASH card or, via the USB interface. Every tool, utility, driver, and support application that The Dini Group could imagine you might need is included. Please contact us for complete specifications, we are eager to show you how our hard work can make you job easier.

The DiNI Group

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XILINX®
The Programmable Logic Company℠

# Xilinx Virtex™-II Series FPGAs

http://www.xilinx.com/devices/

## Product Selection Matrix

| | | | | CLB Resources | | | | Memory Resources | | | DSP | Clock Resources | | I/O Features | | | | Speed | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Virtex-II Series EasyPath Solutions (see note 4) | System Gates (see note 1) | CLB Array (Row x Col) | Number of Slices | Logic Cells (see note 2) | CLB Flip-Flops | Max. Distributed RAM Bits (kbits) | # 18 kbits Block RAM | Total Block RAM (kbits) | # 18x18 Dedicated Multipliers | DCM Frequency (min/max) | # DCM Blocks (see note 3) | Digitally Controlled Impedance | Maximum Differential I/O Pairs | Maximum I/O | I/O Standards | Commercial Speed Grades (slowest to fastest) | Industrial Speed Grades (slowest to fastest) | Configuration Memory (Bits) | RocketIO™ Transceiver Blocks (3.125 Gbps) | RocketIO™ X Transceiver Blocks (10.3125 Gbps) | PowerPC™ Processor Blocks | EasyPath |
| | **Virtex-II Pro Family – 1.5 Volt** | | | | | | | | | | | | | | | | | | | | | | | |
| Platform FPGAs | XC2VP2 | | * | 16 x 22 | 1,408 | 3,168 | 2816 | 44 | 12 | 216 | 12 | 24/420 | 4 | YES | 100 | 204 | LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVPECL-25, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, LVTTL, LVCMOS33, PCI-X, PCI66, GTL, GTL+, HSTL I (1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2I, SSTL2II, SSTL18 I, SSTL18 II | -5 -6 -7 | -5 -6 | 1.3M | 4 | | 0 | |
| | XC2VP4 | | * | 40 x 22 | 3,008 | 6,768 | 6,016 | 94 | 28 | 504 | 28 | 24/420 | 4 | YES | 172 | 348 | | -5 -6 -7 | -5 -6 | 3.0M | 4 | | 1 | |
| | XC2VP7 | | * | 40 x 34 | 4,928 | 11,088 | 9,856 | 154 | 44 | 792 | 44 | 24/420 | 4 | YES | 196 | 396 | | -5 -6 -7 | -5 -6 | 4.4M | 8 | | 1 | |
| | XC2VP20 | | * | 56 x 46 | 9,280 | 20,880 | 18,560 | 290 | 88 | 1,584 | 88 | 24/420 | 8 | YES | 276 | 564 | | -5 -6 -7 | -5 -6 | 8.2M | 8 | | 2 | |
| VIRTEX-II PRO | XC2VP30 | XCE2VP30 | * | 80 x 46 | 13,696 | 30,816 | 27,392 | 428 | 136 | 2448 | 136 | 24/420 | 8 | YES | 372 | 644 | | -5 -6 -7 | -5 -6 | 11.3M | 8 | | 2 | ✔ |
| | XC2VP40 | XCE2VP40 | * | 88 x 58 | 19,392 | 43,632 | 38,784 | 606 | 192 | 3,456 | 192 | 24/420 | 8 | YES | 396 | 804 | | -5 -6 -7 | -5 -6 | 15.5M | 0 or 12 | | 2 | ✔ |
| | XC2VP50 | XCE2VP50 | * | 88 x 70 | 23,616 | 53,136 | 47,232 | 738 | 232 | 4,176 | 232 | 24/420 | 8 | YES | 420 | 852 | | -5 -6 -7 | -5 -6 | 19.0M | 0 or 16 | | 2 | ✔ |
| | XC2VP70 | XCE2VP70 | * | 104 x 82 | 33,088 | 74,448 | 66,176 | 1,034 | 328 | 5,904 | 328 | 24/420 | 8 | YES | 492 | 996 | | -5 -6 -7 | -5 -6 | 25.6M | 16 or 20 | | 2 | ✔ |
| | XC2VP100 | XCE2VP100 | * | 120 x 94 | 44,096 | 99,216 | 88,192 | 1,378 | 444 | 7,992 | 444 | 24/420 | 12 | YES | 572 | 1,164 | | -5 -6 -7 | -5 -6 | 33.5M | 0 or 20 | | 2 | ✔ |
| | **Virtex-II Pro X Family – 1.5 Volt** | | | | | | | | | | | | | | | | | | | | | | | |
| VIRTEX-II PRO X | XC2VPX20 | | * | 56 x 46 | 9,792 | 22,032 | 19,584 | 306 | 88 | 1584 | 88 | 24/420 | 8 | YES | 276 | 552 | Same as above | -5 -6 -7 | TBD | 8.05M | 0 | 8 | 1 | |
| | XC2VPX70 | XCE2VPX70 | * | 104 x 82 | 33,088 | 74,448 | 66,176 | 1034 | 308 | 5544 | 308 | 24/420 | 8 | YES | 492 | 992 | Same as above | -5 -6 -7 | TBD | 25.60M | 0 | 20 | 2 | ✔ |
| | **Virtex-II Family – 1.5 Volt** | | | | | | | | | | | | | | | | | | | | | | | |
| VIRTEX-II | XC2V40 | | 40K | 8 x 8 | 256 | 576 | 512 | 8 | 4 | 72 | 4 | 24/420 | 4 | YES | 44 | 88 | LDT-25, LVPECL-33, LVDS-33, LVDS-25, LVDSEXT-33, LVDSEXT-25, BLVDS-25, ULVDS-25, LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I, HSTL II, HSTL III, HSTL IV, SSTL2I, SSTL2II, SSTL3 I, SSTL3 II, AGP, AGP-2X | -4 -5 -6 | -4 -5 | 0.4M | – | – | – | |
| | XC2V80 | | 80K | 16 x 8 | 512 | 1,152 | 1,024 | 16 | 8 | 144 | 8 | 24/420 | 4 | YES | 60 | 120 | | -4 -5 -6 | -4 -5 | 0.6M | – | – | – | |
| | XC2V250 | | 250K | 24 x 16 | 1,536 | 3,456 | 3,072 | 48 | 24 | 432 | 24 | 24/420 | 8 | YES | 100 | 200 | | -4 -5 -6 | -4 -5 | 1.7M | – | – | – | |
| | XC2V500 | | 500K | 32 x 24 | 3,072 | 6,912 | 6,144 | 96 | 32 | 576 | 32 | 24/420 | 8 | YES | 132 | 264 | | -4 -5 -6 | -4 -5 | 2.8M | – | – | – | |
| | XC2V1000 | | 1M | 40 x 32 | 5,120 | 11,520 | 10,240 | 160 | 40 | 720 | 40 | 24/420 | 8 | YES | 216 | 432 | | -4 -5 -6 | -4 -5 | 4.1M | – | – | – | |
| | XC2V1500 | | 1.5M | 48 x 40 | 7,680 | 17,280 | 15,360 | 240 | 48 | 864 | 48 | 24/420 | 8 | YES | 264 | 528 | | -4 -5 -6 | -4 -5 | 5.7M | – | – | – | |
| | XC2V2000 | | 2M | 56 x 48 | 10,752 | 24,192 | 21,504 | 336 | 56 | 1,008 | 56 | 24/420 | 8 | YES | 312 | 624 | | -4 -5 -6 | -4 -5 | 7.5M | – | – | – | |
| | XC2V3000 | XCE2V3000 | 3M | 64 x 56 | 14,336 | 32,256 | 28,672 | 448 | 96 | 1,728 | 96 | 24/420 | 12 | YES | 360 | 720 | | -4 -5 -6 | -4 -5 | 10.5M | – | – | – | ✔ |
| | XC2V4000 | XCE2V4000 | 4M | 80 x 72 | 23,040 | 51,840 | 46,080 | 720 | 120 | 2,160 | 120 | 24/420 | 12 | YES | 456 | 912 | | -4 -5 -6 | -4 -5 | 15.7M | – | – | – | ✔ |
| | XC2V6000 | XCE2V6000 | 6M | 96 x 88 | 33,792 | 76,032 | 67,584 | 1,056 | 144 | 2,592 | 144 | 24/420 | 12 | YES | 552 | 1,104 | | -4 -5 -6 | -4 -5 | 21.9M | – | – | – | ✔ |
| | XC2V8000 | XCE2V8000 | 8M | 112 x 104 | 46,592 | 104,882 | 93,184 | 1,456 | 168 | 3,024 | 168 | 24/420 | 12 | YES | 554 | 1,108 | | -4 -5 | -4 -5 | 29.1M | – | – | – | ✔ |

* Logic cell counts are a more meaningful measurement of density for the Virtex-II Pro family since system gate count does not take into consideration the benefits of the immersed special blocks such as PowerPC processors and multi-gigabit transceivers.

**Notes:** 1. System Gates include 20-30% of CLBs used as RAM 2. Logic cell = One 4-Input Look Up Table (LUT) + Flip Flop + Carry Logic. 3. DCM = Digital Clock Management 4. Virtex-II Series EasyPath solution available to provide a no risk, no effort cost reduction path for volume production

**Important: Verify all data in this document with the device data sheets found at http://www.xilinx.com/partinfo/databook.htm**

XILINX®
The Programmable Logic Company℠

# Xilinx Virtex™-II Series FPGAs

http://www.xilinx.com/devices/

## Xilinx Virtex-II Series FPGAs and RocketPHY Physical Layer Transceivers

| | | Virtex-II Pro (1.5V) | | | | | | | | | Virtex-II Pro X (1.5V) | | Virtex-II (1.5V) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | XC2VP2 | XC2VP4 | XC2VP7 | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 | XC2VP70 | XC2VP100 | XC2VPX20 | XC2VPX70 | XC2V40 | XC2V80 | XC2V250 | XC2V500 | XC2V1000 | XC2V1500 | XC2V2000 | XC2V3000 | XC2V4000 | XC2V6000 | XC2V8000 |
| Pins[3] | Area | 204 | 348 | 396 | 564 | 692 | 804 | 852 | 996 | 1164 | 552 | 992 | 88 | 120 | 200 | 264 | 432 | 528 | 624 | 720 | 912 | 1104 | 1108 |
| **Chip Scale Packages (CS) – wire-bond chip-scale BGA (0.8 mm ball spacing)** | | | | | | | | | | | | | | | | | | | | | | |
| 144 | 12 x 12 mm | | | | | | | | | | | | 88 | 92 | 92 | | | | | | | | |
| **BGA Packages (BG) – wire-bond standard BGA (1.27 mm ball spacing)** | | | | | | | | | | | | | | | | | | | | | | |
| 575 | 31 x 31 mm | | | | | | | | | | | | | | | | 328 | 392 | 408 | | | | |
| 728 | 35 x 35 mm | | | | | | | | | | | | | | | | | | | 516 | | | |
| **FGA Packages (FG) – wire-bond fine-pitch BGA (1.0 mm ball spacing)** | | | | | | | | | | | | | | | | | | | | | | |
| 256 | 17 x 17 mm | 140 | 140 | | | | | | | | | | 88 | 120 | 172 | 172 | 172 | | | | | | |
| 456[4] | 23 x 23 mm | 156 | 248 | 248 | | | | | | | | | | | 200 | 264 | 324 | | | | | | |
| 676[4] | 27 x 27 mm | | | | 404 | 416 | 416 | | | | | | | | | | | 392 | 456 | 484 | | | |
| **FFA Packages (FF) – flip-chip fine-pitch BGA (1.0 mm ball spacing)** | | | | | | | | | | | | | | | | | | | | | | |
| 672 | 27 x 27 mm | 204 | 348 | 396 | | | | | | | | | | | | | | | | | | | |
| 896[5] | 31 x 31 mm | | | 396 | 556 | 556 | | | | | 552 | | | | | | 432 | 528 | 624 | | | | |
| 1152[5] | 35 x 35 mm | | | | 564 | 644 | 692 | 692 | | | | | | | | | | | | 720 | 824 | 824 | 824 |
| 1148[6] | 35 x 35 mm | | | | | | 804 | 812 | | | | | | | | | | | | | | | |
| 1517 | 40 x 40 mm | | | | | | | 852 | 964 | | | | | | | | | | | | 912 | 1104 | 1108 |
| 1704 | 42.5 x 42.5 mm | | | | | | | | 996 | 1040 | | 992 | | | | | | | | | | | |
| 1696[6] | 42.5 x 42.5 mm | | | | | | | | | 1164 | | | | | | | | | | | | | |
| **BFA Packages (BF) – flip-chip fine-pitch BGA (1.27 mm ball spacing)** | | | | | | | | | | | | | | | | | | | | | | |
| 957 | 40 x 40 mm | | | | | | | | | | | | | | | | | | 624 | 684 | 684 | 684 | |

**Notes:** 1. Numbers in table indicate maximum number of user I/Os.
2. The number of I/Os for RocketIO MGTs are not included in this table.
3. Within the same family, all devices in a particular package are pin-out (footprint) compatible.
4. Virtex-II packages FG456 and FG676 are also footprint compatible.
5. Virtex-II packages FF896 and FF1152 are also footprint compatible.
6. RocketIO unavailable in this package.

Pb-free solutions are available. For more information about Pb-free solutions visit www.xilinx.com/pbfree.

| | Transceiver Blocks | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | RocketIO (3.125Gbps) | | | | | | | | | RocketIO X (10Gbps) | |
| Package | XC2VP2 | XC2VP4 | XC2VP7 | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 | XC2VP70 | XC2VP100 | XC2VPX20 | XC2VPX70 |
| FG256 | 4 | 4 | | | | | | | | | |
| FG456 | 4 | 4 | 8 | | | | | | | | |
| FG676 | | | | 8 | 8 | 8 | | | | | |
| FG672 | 4 | 4 | 8 | | | | | | | | |
| FF896 | | | 8 | 8 | 8 | | | | | 8 | |
| FF1152 | | | | 8 | 8 | 12 | 16 | | | | |
| FF1148[6] | | | | | | 0 | 0 | | | | |
| FF1517 | | | | | | | 16 | 16 | | | |
| FF1704 | | | | | | | | 20 | 20 | | 20 |
| FF1696[6] | | | | | | | | | 0 | | |

RocketPHY

| | RocketPHY Family of 10Gbps Physical Layer Transceivers | | | | | | |
|---|---|---|---|---|---|---|---|
| Device | SONET OC-192 SDH STM - 64 | G . 709 | 10G ETHERNET | 10G FIBRE CHANNEL | Applications | Parallel Interface | Package |
| XGC1120 - Ultra MSA | √ | √ | √ | √ | MSA Modules XFP Transceivers, SONET/SDH transmission systems, OTN system w/FEC, fiber optic test equipment | XSBI SFI-4 | FT256 |
| XGC1121 - 10G SONET/SDH | √ | | | | XFP Transceivers, SONET/SDH – based transmission systems, fiber optic test equipment | SFI-4 | FT256 |
| XGC1320 - 10GE/10GFC | | | √ | √ | XFP Transceivers, data transmission equipment, NICs, test equipment, edge routers, storage area networks | XSBI | FT256 |

For more information about the RocketPHY family, visit www.xilinx.com/rocketphy

**Important: Verify all data in this document with the device data sheets found at http://www.xilinx.com/partinfo/databook.htm**

## Product Selection Matrix

| | | CLB Resources | | | | Memory Resources | | | DSP | CLK Resources | | | | I/O Features | | | | Speed | | PROM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | System Gates (see note 1) | CLB Array (Row x Col) | Number of Slices | Logic Cells (see note 2 ) | CLB Flip-Flops | Max. Distributed RAM Bits | # Block RAM | Block RAM (bits) | Dedicated Multipliers | DCM Frequency (min/max) | # DCMs | Frequency Synthesis | Phase Shift | Digitally Controlled Impedance | Number of Differential I/O Pairs | Maximum I/O | I/O Standards | Commercial Speed Grades (slowest to fastest) | Industrial Speed Grades (slowest to fastest) | Configuration Memory (Bits) |
| **Spartan-3 Family – 1.2 Volt (see note 3)** | | | | | | | | | | | | | | | | | | | | |
| **XC3S50** | 50K | 16 x 12 | 768 | 1,728 | 1,536 | 12K | 4 | 72K | 4 | 24/330 | 2 | YES | YES | YES | 56 | 124 | Single-ended LVTTL, LVCMOS3.3/2.5/1.8/ 1.5/1.2, PCI 3.3V – 32/64-bit 33MHz, SSTL2 Class I & II, SSTL18 Class I, HSTL Class I, III, HSTL1.8 Class I, II & III, GTL, GTL+<br><br>Differential LVDS2.5, Bus LVDS2.5, Ultra LVDS2.5, LVDS_ext2.5, RSDS, LDT2.5, LVPECL | -4 -5 | -4 | .4M |
| **XC3S200** | 200K | 24 x 20 | 1,920 | 4,320 | 3,840 | 30K | 12 | 216K | 12 | 24/330 | 4 | YES | YES | YES | 76 | 173 | | -4 -5 | -4 | 1.0M |
| **XC3S400** | 400K | 32 x 28 | 3,584 | 8,064 | 7,168 | 56K | 16 | 288K | 16 | 24/330 | 4 | YES | YES | YES | 116 | 264 | | -4 -5 | -4 | 1.7M |
| **XC3S1000** | 1000K | 48 x 40 | 7,680 | 17,280 | 15,360 | 120K | 24 | 432K | 24 | 24/330 | 4 | YES | YES | YES | 175 | 391 | | -4 -5 | -4 | 3.2M |
| **XC3S1500** | 1500K | 64 x 52 | 13,312 | 29,952 | 26,624 | 208K | 32 | 576K | 32 | 24/330 | 4 | YES | YES | YES | 221 | 487 | | -4 -5 | -4 | 5.2M |
| **XC3S2000** | 2000K | 80 x 64 | 20,480 | 46,080 | 40,960 | 320K | 40 | 720K | 40 | 24/330 | 4 | YES | YES | YES | 270 | 565 | | -4 -5 | -4 | 7.7M |
| **XC3S4000** | 4000K | 96 x 72 | 27,648 | 62,208 | 55,296 | 432K | 96 | 1,728K | 96 | 24/330 | 4 | YES | YES | YES | 312 | 712 | | -4 -5 | -4 | 11.3M |
| **XC3S5000** | 5000K | 104 x 80 | 33,280 | 74,880 | 66,560 | 520K | 104 | 1,872K | 104 | 24/330 | 4 | YES | YES | YES | 344 | 784 | | -4 -5 | -4 | 13.3M |

**Note:** 1. System Gates include 20-30% of CLBs used as RAMs
2. For Spartan-3, a Logic Cell is defined as a 4-input LUT + flip-flop
3. Automotive Q-Grade Solutions for Spartan-3 will be available 2H2004.

**Important: Verify all data in this document with the device data sheets found at http://www.xilinx.com/partinfo/databook.htm**

XILINX®
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# Xilinx Spartan™ Series FPGAs

http://www.xilinx.com/devices/

## Product Selection Matrix

| | | CLB Resources | | | | Memory Resources | | | CLK Resources | | | | I/O Features | | | Speed | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | System Gates (see note 1) | CLB Array (Row x Col) | Number of Slices | Logic Cells (see notes 2 and 3) | CLB Flip-Flops | Max. Distributed RAM Bits | # Block RAM | Block RAM (bits) | DLL Frequency (min/max) | # DLL's | Frequency Synthesis | Phase Shift | Number of Differential I/O Pairs | Maximum I/O | I/O Standards | Commercial Speed Grades (slowest to fastest) | Industrial Speed Grade (slowest to fastest) | Automotive Q-Grade Speed Grade | Configuration Memory (Bits) | Automotive Q-Grade Solutions (see note 4) |
| **Spartan-IIE Family – 1.8 Volt** | | | | | | | | | | | | | | | | | | | | |
| XC2S50E | 50K | 16 x 24 | 768 | 1,728 | 1,536 | 24K | 8 | 32K | 25/320 | 4 | YES | YES | 83 | 182 | LVTTL,LVCMOS2, LVCMOS18, PCI33, PCI66, GTL, GTL+, HSTL I, HSTL III, HSTL IV, SSTL3 I, SSTL3 II, SSTL2 I, SSTL2 II, AGP-2X, CTT, LVDS, BLVDS, LVPECL | -6 -7 | -6 | -6 | 0.6M | ✔ |
| XC2S100E | 100K | 20 x 30 | 1,200 | 2,700 | 2,400 | 37K | 10 | 40K | 25/320 | 4 | YES | YES | 86 | 202 | | -6 -7 | -6 | -6 | 0.9M | ✔ |
| XC2S150E | 150K | 24 x 36 | 1,728 | 3,888 | 3,456 | 54K | 12 | 48K | 25/320 | 4 | YES | YES | 114 | 265 | | -6 -7 | -6 | -6 | 1.1M | ✔ |
| XC2S200E | 200K | 28 x 42 | 2,352 | 5,292 | 4,704 | 73K | 14 | 56K | 25/320 | 4 | YES | YES | 120 | 289 | | -6 -7 | -6 | -6 | 1.4M | ✔ |
| XC2S300E | 300K | 32 x 48 | 3,072 | 6,912 | 6,144 | 96K | 16 | 64K | 25/320 | 4 | YES | YES | 120 | 329 | | -6 -7 | -6 | -6 | 1.9M | ✔ |
| XC2S400E | 400K | 40 x 60 | 4,800 | 10,800 | 9,600 | 150K | 40 | 160K | 25/320 | 4 | YES | YES | 172 | 410 | | -6 -7 | -6 | -6 | 2.7M | ✔ |
| XC2S600E | 600K | 48 x 72 | 6,912 | 15,552 | 13,824 | 216K | 72 | 288K | 25/320 | 4 | YES | YES | 205 | 514 | | -6 -7 | -6 | -6 | 4.0M | ✔ |
| **Spartan-II Family – 2.5 Volt** | | | | | | | | | | | | | | | | | | | | |
| XC2S15 | 15K | 8 x 12 | 192 | 432 | 384 | 6K | 4 | 16K | 25/200 | 4 | YES | YES | NA | 86 | LVTTL, LVCMOS2, PCI33 (3.3V & 5V), PCI66 (3.3V), GTL, GTL+, HSTL I, HSTL III, HSTL IV, SSTL3 I, SSTL3 II, SSTL2 I, SSTL2 II, AGP-2X, CTT | -5 -6 | -5 | -5 | 0.2M | ✔ |
| XC2S30 | 30K | 12 x 18 | 432 | 972 | 864 | 13.5K | 6 | 24K | 25/200 | 4 | YES | YES | NA | 92 | | -5 -6 | -5 | -5 | 0.4M | ✔ |
| XC2S50 | 50K | 16 x 24 | 768 | 1,728 | 1,536 | 24K | 8 | 32K | 25/200 | 4 | YES | YES | NA | 176 | | -5 -6 | -5 | -5 | 0.6M | ✔ |
| XC2S100 | 100K | 20 x 30 | 1,200 | 2,700 | 2,400 | 37.5K | 10 | 40K | 25/200 | 4 | YES | YES | NA | 176 | | -5 -6 | -5 | -5 | 0.8M | ✔ |
| XC2S150 | 150K | 24 x 36 | 1,728 | 3,888 | 3,456 | 54K | 12 | 48K | 25/200 | 4 | YES | YES | NA | 260 | | -5 -6 | -5 | -5 | 1.1M | ✔ |
| XC2S200 | 200K | 28 x 42 | 2,352 | 5,292 | 4,704 | 73.5K | 14 | 56K | 25/200 | 4 | YES | YES | NA | 284 | | -5 -6 | -5 | -5 | 1.4M | ✔ |
| **Spartan-XL Family – 3.3 Volt** | | | | | | | | | | | | | | | | | | | | |
| XCS05XL | 5K | 10 x 10 | 100 | 238 | 200 | 3.1K | NA | NA | NA | NA | NA | NA | NA | 77 | | -4 -5 | -4 | -4 | 0.05M | ✔ |
| XCS10XL | 10K | 14 x 14 | 196 | 466 | 392 | 6.1K | NA | NA | NA | NA | NA | NA | NA | 112 | | -4 -5 | -4 | -4 | 0.09M | ✔ |
| XCS20XL | 20K | 20 x 20 | 400 | 950 | 800 | 12.5K | NA | NA | NA | NA | NA | NA | NA | 160 | | -4 -5 | -4 | -4 | 0.18M | ✔ |
| XCS30XL | 30K | 24 x 24 | 576 | 1,368 | 1,152 | 18.0K | NA | NA | NA | NA | NA | NA | NA | 192 | | -4 -5 | -4 | -4 | 0.25M | ✔ |
| XCS40XL | 40K | 28 x 28 | 784 | 1,862 | 1,568 | 24.5K | NA | NA | NA | NA | NA | NA | NA | 205 | | -4 -5 | -4 | -4 | 0.33M | ✔ |

**Note:** 1. System Gates include 20-30% of CLBs used as RAM
2. Logic cell = (1) 4 Input (LUT) and a register
3. For Spartan-IIE/II/XL, a Logic Cell is defined as a 4-input LUT + a register
4. Automotive Q-Grade Solutions are qualified to -40°C to +125°C junction temperature for FPGAs. Q-Grade products for Spartan-3 will be available 2H2004

**Important: Verify all data in this document with the device data sheets found at http://www.xilinx.com/partinfo/databook.htm**

## Package Options and User I/O[1]

| | | Spartan-3 (1.2V) | | | | | | | | | Spartan-IIE (1.8V) | | | | | | | | Spartan-II (2.5V) | | | | | | Spartan-XL (3.3V) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | XC3S50 | XC3S200 | XC3S400 | XC3S1000 | XC3S1500 | XC3S2000 | XC3S4000 | XC3S5000 | | XC2S50E | XC2S100E | XC2S150E | XC2S200E | XC2S300E | XC2S400E | XC2S600E | XC2S15 | XC2S30 | XC2S50 | XC2S100 | XC2S150 | XC2S200 | XCS05XL | XCS10XL | XCS20XL | XCS30XL | XCS40XL |
| Pins | Area[2] | I/O's | 124 | 173 | 264 | 391 | 487 | 565 | 712 | 784 | I/O's | 182 | 202 | 265 | 289 | 329 | 410 | 514 | 86 | 92 | 176 | 176 | 260 | 284 | 77 | 112 | 160 | 192 | 192 |
| PQFP Packages (PQ) – wire-bond plastic QFP (0.5mm lead spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 208 | 30.6 x 30.6 mm | | 124 | 141 | 141 | | | | | | | 146 | 146 | 146 | 146 | 146 | | | | | 140 | 140 | 140 | 140 | | | 160 | 169 | 169 |
| 240 | 34.6 x 34.6 mm | | | | | | | | | | | | | | | | | | | | | | | | | | | 192 | 192 |
| VQFP Packages (VQ) – very thin TQFP (0.5mm lead spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 | 16.0 x 16.0 mm | | 63 | 63 | | | | | | | | | | | | | | | 60 | 60 | | | | | 77 | 77 | 77 | 77 | |
| TQFP Packages (TQ) – thin QFP (0.5mm lead spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 144 | 22.0 x 22.0 mm | | 97 | 97 | 97 | | | | | | | 102 | 102 | | | | | | 86 | 92 | 92 | 92 | | | | 112 | 113 | 113 | |
| Chip Scale Packages (CS) – wire-bond chip-scale BGA (0.8 mm ball spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 144 | 12 x 12 mm | | | | | | | | | | | | | | | | | | | 92 | | | | | | | | | |
| FGA Packages (FT) – wire-bond fine-pitch thin BGA (1.0 mm ball spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | 17 x 17 mm | | | 173 | 173 | 173 | | | | | | 182 | 182 | 182 | 182 | 182 | 182 | | | | | | | | | | | | |
| FGA Packages (FG) – wire-bond fine-pitch BGA (1.0 mm ball spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | 17 x 17 mm | | | | | | | | | | | | | | | | | | | | 176 | 176 | 176 | 176 | | | | | |
| 320 | 19 x 19 mm | | | | 221 | 221 | 221 | | | | | | | | | | | | | | | | | | | | | | |
| 456 | 23 x 23 mm | | | | 264 | 333 | 333 | | | | | | 202 | 265 | 289 | 329 | 329 | 329 | | | | | 260 | 284 | | | | | |
| 676 | 27 x 27 mm | | | | | 391 | 487 | 489 | | | | | | | | | 410 | 514 | | | | | | | | | | | |
| 900 | 31 x 31 mm | | | | | | | 565 | 633 | 633 | | | | | | | | | | | | | | | | | | | |
| 1156 | 35 x 35 mm | | | | | | | | 712 | 784 | | | | | | | | | | | | | | | | | | | |
| BGA Packages (BG) – wire-bond standard BGA (1.27 mm ball spacing) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 256 | 27 x 27 mm | | | | | | | | | | | | | | | | | | | | | | | | | | | 192 | 205 |

**Note 1:** Numbers in table indicate maximum number of user I/Os
**Note 2:** Area dimensions for lead-frame products are inclusive of the leads.

Automotive products are highlighted: -40C to +125C junction temperature for FPGAs.
Automotive Q-Grade products will be available in Spartan-3 family 2H2004.
For more information on IQ Solutions please visit **http://www.xilinx.com/automotive**

Xilinx IQ Solutions for Automotive Intelligence

Pb-free solutions are available. For more information about Pb-free solutions visit www.xilinx.com/pbfree.

**Important: Verify all data in this document with the device data sheets found at http://www.xilinx.com/partinfo/databook.htm**

## Product Selection Matrix – CoolRunner™ Series

| | | System Gates | Macrocells | Product Terms per Macrocell | Input Voltage Compatible | Output Voltage Compatible | I/O Features: Maximum I/O | I/O Features: I/O Banking | Speed: Min. Pin-to-pin Logic Delay (ns) | Speed: Commercial Speed Grades (fastest to slowest) | Speed: Industrial Speed Grades (fastest to slowest) | Speed: IQ Speed Grade | Clocking: Global Clocks | Clocking: Product Term Clocks per Function Block |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **CoolRunner-II Family – 1.8 Volt** | | | | | | | | | | | | | |
| CoolRunner-II | XC2C32 | 750 | 32 | 40 | 1.5/1.8/2.5/3.3 | 1.5/1.8/2.5/3.3 | 33 | 1 | 3 | -3 -4 -6 | -6 | -6 | 3 | 17 |
| | XC2C64 | 1500 | 64 | 40 | 1.5/1.8/2.5/3.3 | 1.5/1.8/2.5/3.3 | 64 | 1 | 4 | -4 -5 -7 | -7 | -7 | 3 | 17 |
| | XC2C128 | 3000 | 128 | 40 | 1.5/1.8/2.5/3.3 | 1.5/1.8/2.5/3.3 | 100 | 2 | 4.5 | -4 -6 -7 | -7 | -7 | 3 | 17 |
| | XC2C256 | 6000 | 256 | 40 | 1.5/1.8/2.5/3.3 | 1.5/1.8/2.5/3.3 | 184 | 2 | 5 | -5 -6 -7 | -7 | -7 | 3 | 17 |
| | XC2C384 | 9000 | 384 | 40 | 1.5/1.8/2.5/3.3 | 1.5/1.8/2.5/3.3 | 240 | 4 | 6 | -6 -7 -10 | -10 | -10 | 3 | 17 |
| | XC2C512 | 12000 | 512 | 40 | 1.5/1.8/2.5/3.3 | 1.5/1.8/2.5/3.3 | 270 | 4 | 6 | -6 -7 -10 | -10 | -10 | 3 | 17 |
| | **CoolRunner XPLA3 Family – 3.3 Volt** | | | | | | | | | | | | | |
| CoolRunner XPLA3 | XCR3032XL | 750 | 32 | 48 | 3.3/5 | 3.3 | 36 | | 5 | -5 -7 -10 | -7 -10 | -10 | 4 | 16 |
| | XCR3064XL | 1500 | 64 | 48 | 3.3/5 | 3.3 | 68 | | 6 | -6 -7 -10 | -7 -10 | -10 | 4 | 16 |
| | XCR3128XL | 3000 | 128 | 48 | 3.3/5 | 3.3 | 108 | | 6 | -6 -7 -10 | -7 -10 | -10 | 4 | 16 |
| | XCR3256XL | 6000 | 256 | 48 | 3.3/5 | 3.3 | 164 | | 7.5 | -7 -10 -12 | -10 -12 | -12 | 4 | 16 |
| | XCR3384XL | 9000 | 384 | 48 | 3.3/5 | 3.3 | 220 | | 7.5 | -7 -10 -12 | -10 -12 | -12 | 4 | 16 |
| | XCR3512XL | 12000 | 512 | 48 | 3.3/5 | 3.3 | 260 | | 7.5 | -7 -10 -12 | -10 -12 | -12 | 4 | 16 |

## Package Options and User I/O

| Pins | Area[1] | CoolRunner-II: XC2C32 | XC2C64 | XC2C128 | XC2C256 | XC2C384 | XC2C512 | CoolRunner XPLA3: XCR3032XL | XCR3064XL | XCR3128XL | XCR3256XL | XCR3384XL | XCR3512XL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PLCC Packages (PC) – wire-bond plastic chip carrier (1.27mm lead spacing) | | | | | | | | | | | | | |
| 44 | 17.5 x 17.5 mm | 33 | 33 | | | | | 36 | 36 | | | | |
| PQFP Packages (PQ) – wire-bond plastic QFP (0.5mm lead spacing) | | | | | | | | | | | | | |
| 208 | 30.6 x 30.6 mm | | | | 173 | 173 | 173 | | | | 164 | 172 | 180 |
| VQFP Packages (VQ) – very thin TQFP (0.5mm lead spacing) | | | | | | | | | | | | | |
| 44 | 12.0 x 12.0 mm | 33 | 33 | | | | | 36 | 36 | | | | |
| 100 | 16.0 x 16.0 mm | | 64 | 80 | 80 | | | | 68 | 84 | | | |
| TQFP Packages (TQ) – thin QFP (0.5mm lead spacing) | | | | | | | | | | | | | |
| 144 | 22.0 x 22.0 mm | | | 100 | 118 | 118 | | | | 108 | 120 | 118* | |
| Chip Scale Packages (CP) – wire-bond chip-scale BGA (0.5 mm ball spacing) | | | | | | | | | | | | | |
| 56 | 6 x 6 mm | 33 | 45 | | | | | | 48 | | | | |
| 132 | 8 x 8 mm | | | 100 | 106 | | | | | | | | |
| Chip Scale Packages (CS) – wire-bond chip-scale BGA (0.8 mm ball spacing) | | | | | | | | | | | | | |
| 48 | 7 x 7 mm | | | | | | | 36 | 40 | | | | |
| 144 | 12 x 12 mm | | | | | | | | | 108 | | | |
| 280 | 16 x 16 mm | | | | | | | | | | 164 | | |
| FGA Packages (FT) – wire-bond fine-pitch thin BGA (1.0 mm ball spacing) | | | | | | | | | | | | | |
| 256 | 17 x 17 mm | | | | 184 | 212 | 212 | | | | 164 | 212 | 212 |
| FBGA Packages (FG) – wire-bond Fine-line BGA (1.0 mm ball spacing) | | | | | | | | | | | | | |
| 324 | 23 x 23 mm | | | | | 240 | 270 | | | | | 220 | 260 |

* JTAG pins and port enable are not pin compatible in this package for this member of the family

Note 1: Area dimensions for lead-frame products are inclusive of the leads.

Automotive products are highlighted: -40C to +125C ambient temperature for CPLDs

Xilinx IQ Solutions for Automotive Intelligence

## Product Selection Matrix – 9500 Series

| | System Gates | Macrocells | Product Terms per Macrocell | Input Voltage Compatible | Output Voltage Compatible | I/O Features: Maximum I/O | I/O Features: I/O Banking | Speed: Min. Pin-to-pin Logic Delay (ns) | Speed: Commercial Speed Grades (fastest to slowest) | Speed: Industrial Speed Grades (fastest to slowest) | Speed: IQ Speed Grade | Clocking: Global Clocks | Clocking: Product Term Clocks per Function Block |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **XC9500XV Family – 2.5 Volt** | | | | | | | | | | | | | |
| XC9536XV | 800 | 36 | 90 | 2.5/3.3 | 1.8/2.5/3.3 | 36 | 1 | 5 | -5 -7 | -7 | NA | 3 | 18 |
| XC9572XV | 1600 | 72 | 90 | 2.5/3.3 | 1.8/2.5/3.3 | 72 | 1 | 5 | -5 -7 | -7 | NA | 3 | 18 |
| XC95144XV | 3200 | 144 | 90 | 2.5/3.3 | 1.8/2.5/3.3 | 117 | 2 | 5 | -5 -7 | -7 | NA | 3 | 18 |
| XC95288XV | 6400 | 288 | 90 | 2.5/3.3 | 1.8/2.5/3.3 | 192 | 4 | 6 | -6 -7 -10 | -7 -10 | NA | 3 | 18 |
| **XC9500XL Family – 3.3 Volt** | | | | | | | | | | | | | |
| XC9536XL | 800 | 36 | 90 | 2.5/3.3/5 | 2.5/3.3 | 36 | | 5 | -5 -7 -10 | -7 -10 | -10 | 3 | 18 |
| XC9572XL | 1600 | 72 | 90 | 2.5/3.3/5 | 2.5/3.3 | 72 | | 5 | -5 -7 -10 | -7 -10 | -10 | 3 | 18 |
| XC95144XL | 3200 | 144 | 90 | 2.5/3.3/5 | 2.5/3.3 | 117 | | 5 | -5 -7 -10 | -7 -10 | NA | 3 | 18 |
| XC95288XL | 6400 | 288 | 90 | 2.5/3.3/5 | 2.5/3.3 | 192 | | 6 | -6 -7 -10 | -7 -10 | NA | 3 | 18 |
| **XC9500 Family – 5 Volt** | | | | | | | | | | | | | |
| XC9536 | 800 | 36 | 90 | | 5 | 36 | | 10 | -5 -6 -10 -15 | -7 -10 -15 | -15 | 3 | 18 |
| XC9572 | 1600 | 72 | 90 | 5 | 5 | 72 | | 10 | -7 -10 -15 | -10 -15 | -15 | 3 | 18 |
| XC95108 | 2400 | 108 | 90 | 5 | 5 | 108 | | 10 | -7 -10 -15 -20 | -7 -10 -15 -20 | NA | 3 | 18 |
| XC95144 | 3200 | 144 | 90 | 5 | 5 | 133 | | 10 | -7 -10 -15 | -10 -15 | NA | 3 | 18 |
| XC95216 | 4800 | 216 | 90 | 5 | 5 | 166 | | 10 | -10 -15 -20 | -10 -15 -20 | NA | 3 | 18 |
| XC95288 | 6400 | 288 | 90 | 5 | 5 | 192 | | 10 | -10 -15 -20 | -15 -20 | NA | 3 | 18 |

Pb-free solutions are available. For more information about Pb-free solutions visit www.xilinx.com/pbfree.

## Package Options and User I/O

| Pins | Area[1] | XC9500XV: XC9536XV | XC9572XV | XC95144XV | XC95288XV | XC9500XL: XC9536XL | XC9572XL | XC95144XL | XC95288XL | XC9500: XC9536 | XC9572 | XC95108 | XC95144 | XC95216 | XC95288 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PLCC Packages (PC) – wire-bond plastic chip carrier (1.27mm lead spacing)** | | | | | | | | | | | | | | | |
| 44 | 17.5 x 17.5 mm | 34 | 34 | | | 34 | 34 | | | 34 | 34 | | | | |
| 84 | 30.2 x 30.2 mm | | | | | | | | | | 69 | 69 | | | |
| **PQFP Packages (PQ) – wire-bond plastic QFP (0.5mm lead spacing)** | | | | | | | | | | | | | | | |
| 100 | 23.3 x 17.2 mm | | | | | | | | | | 72 | 81 | 81 | | |
| 160 | 31.2 x 31.2 mm | | | | | | | | | | | 108 | 133 | 133 | 168 |
| 208 | 30.6 x 30.6 mm | | | | 168 | | | | 168 | | | | | 166 | 168 |
| **VQFP Packages (VQ) – very thin TQFP (0.5mm lead spacing)** | | | | | | | | | | | | | | | |
| 44 | 12.0 x 12.0 mm | 34 | 34 | | | 34 | 34 | | | 34 | | | | | |
| 64 | 12.0 x 12.0 mm | | | | | 36 | 52 | | | | | | | | |
| **TQFP Packages (TQ) – thin QFP (0.5mm lead spacing)** | | | | | | | | | | | | | | | |
| 100 | 16.0 x 16.0 mm | | 72 | 81 | | | 72 | 81 | | | 72 | 81 | 81 | | |
| 144 | 22.0 x 22.0 mm | | | 117 | 117 | | | 117 | 117 | | | | | | |
| **Chip Scale Packages (CP) – wire-bond chip-scale BGA (0.5 mm ball spacing)** | | | | | | | | | | | | | | | |
| 56 | 6 x 6 mm | | | | | | | | | | | | | | |
| 132 | 8 x 8 mm | | | | | | | | | | | | | | |
| **Chip Scale Packages (CS) – wire-bond chip-scale BGA (0.8 mm ball spacing)** | | | | | | | | | | | | | | | |
| 48 | 7 x 7 mm | 36 | 38 | | | 36 | 38 | | | 34 | | | | | |
| 144 | 12 x 12 mm | | | 117 | | | | 117 | | | | | | | |
| 280 | 16 x 16 mm | | | | 192 | | | | 192 | | | | | | |
| **BGA Packages (BG) – wire-bond standard BGA (1.27 mm ball spacing)** | | | | | | | | | | | | | | | |
| 256 | 27 x 27 mm | | | | | | | | 192 | | | | | | |
| 352 | 35.0 x 35.0 mm | | | | | | | | 192 | | | | | 166 | 192 |
| **FGA Packages (FT) – wire-bond fine-pitch thin BGA (1.0 mm ball spacing)** | | | | | | | | | | | | | | | |
| 256 | 17 x 17 mm | | | | | | | | | | | | | | |
| **FBGA Packages (FG) – wire-bond Fine-line BGA (1.0 mm ball spacing)** | | | | | | | | | | | | | | | |
| 256 | 17 x 17 mm | | | | 192 | | | | 192 | | | | | | |
| 324 | 23 x 23 mm | | | | | | | | | | | | | | |

Note 1: Area dimensions for lead-frame products are inclusive of the leads.

Automotive products are highlighted: -40C to +125C ambient temperature for CPLDs

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# Xilinx Defense and Aerospace

http://www.xilinx.com/devices

## Aerospace & Defense FPGAs

| | | Device | SMD | Core Voltage | Slices (1) | MULTs | BRAM bits | Configuration bits | Clock DLLs/DCMs | Max I/Os | Manufacturing Grades | Packages | Total Ionizing Dose (krad) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Defense QPRO FPGAs | QPro Virtex-II | XQ2V1000 | 5962-02529 | 1.5V | 5120 | 40 | 720K | 3987K | 8 | 328 | N | FG456, BG575 | — |
| | | XQ2V3000 | 5962-02530 | 1.5V | 14336 | 96 | 1728K | 10248K | 12 | 516 | N, M, B | BG728, CG717 (2) | — |
| | | XQ2V6000 | 5962-02531 | 1.5V | 33792 | 144 | 2592K | 21337K | 12 | 824 | M | CF1144 (3) | — |
| | QPro Virtex-E | XQV600E | None | 1.8V | 6912 | — | 288K | 3869K | 8 | 316 | N | BG432 | — |
| | | XQV1000E | None | 1.8V | 12288 | — | 384K | 6433K | 8 | 404 | M, N | BG560, CG560 (4) | — |
| | | XQV2000E | None | 1.8V | 19200 | — | 640K | 9922K | 8 | 804 | N | BG560, FG1156 | — |
| | QPro Virtex | XQV100 | None | 2.5V | 1200 | — | 40K | 763K | 4 | 180 | M, N | PQ240, BG256, CB228 (5) | — |
| | | XQV300 | 5962-99572 | 2.5V | 3072 | — | 64K | 1711K | 4 | 316 | M, N, B | PQ240, BG352, BG432, CB228 | — |
| | | XQV600 | 5962-99573 | 2.5V | 6912 | — | 96K | 3523K | 4 | 316 | M, N, B | HQ240, BG432, CB228 | — |
| | | XQV1000 | 5962-99574 | 2.5V | 12288 | — | 128K | 5984K | 4 | 404 | M, N, B | BG560, CG560 | — |
| Aerospace QPRO-R Radiation Tolerant FPGAs | QPro-R Virtex-II | XQR2V1000 | 5962R02529 | 1.5V | 5120 | 40 | 720K | 3987K | 8 | 328 | R | FG456, BG575 | 200 |
| | | XQR2V3000 | 5962R02530 | 1.5V | 14336 | 96 | 1728K | 10248K | 12 | 516 | R, M, V | BG728, CG717 (2) | 200 |
| | | XQR2V6000 | 5962R02531 | 1.5V | 33792 | 144 | 2592K | 21337K | 12 | 824 | H | CF1144 (3) | 200 |
| | QPro-R Virtex | XQVR300 | 5962R9957201 | 2.5V | 3072 | — | 64K | 1711K | 4 | 162 | M, V, B | CB228 | 100 |
| | | XQVR600 | 5962R9957301 | 2.5V | 6912 | — | 96K | 3523K | 4 | 162 | M, V, B | CB228 | 100 |
| | | XQVR1000 | 5962R9957401 | 2.5V | 12288 | — | 128K | 5984K | 4 | 404 | M, V, B | CG560 (4) | 100 |

**Notes:**
(1) Each slice contains two 4-input LUTs, two flip-flops, carry logic and other features.
(2) The BG728 and CG717 packages are footprint / pin compatible
(3) The CF1144 and FF1152 packages are footprint / pin compatible
(4) The CG560 and BG560 packages are footprint / pin compatible
(5) The HQ240 and the PQ240 packages are footprint / pin compatible

## Manufacturing Grades

http://www.xilinx.com/products/milaero/rpt003.pdf

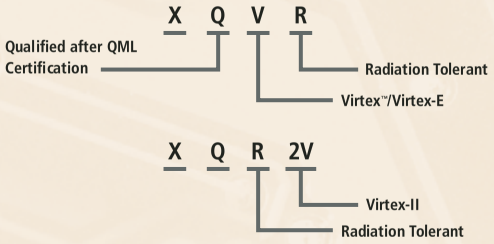
| Grade | Description | Temperature |
|---|---|---|
| V | QPRO-Plus Radiation Tolerant Military Ceramic | Tc = -55C to +125C |
| H | QPRO-FCC Flip-Chip Radiation Tolerant Ceramic | Tj = -55C to +125C |
| R | QPRO-Plus PEM Radiation Tolerant PEM Military Plastic | Tj = -55C to +125C |
| B | SMD Radiation Tolerant and Non-RT SMD Military Ceramic | Tc = -55C to +125C |
| N | Military Plastic | Tj = -55C to +125C |
| M | Military Ceramic | Tc = -55C to +125C |
| I | Industrial Plastic or Ceramic | Tc = -40C to +100C |

## Aerospace & Defense Configuration PROMs

| | | Device | SMD | Core Voltage (1) | Storage Bits | Manufacturing Grades | Packages (2) | Guaranteed Total Ionizing Dose (krad) |
|---|---|---|---|---|---|---|---|---|
| Defense QPRO Configuration PROMs | QPro PROMs | XQ1701L | 5962-99514 | 5V | 1M | M, N | CC44, SO20 | — |
| | | XQ17016 | None | 3.3V | 16M | M, N | CC44, VQ44 | — |
| | | XQ18V04 | None | 3.3V | 16M | M, N | VQ44 | — |
| Aerospace QPRO-R Radiation Tolerant Configuration PROMs | QPro-R PROMs | XQ1701L | TBD | 3.3V | 1M | M, V | CC44 | 50 |
| | | XQR17V16 | TBD | 3.3V | 16M | M, V, R | CC44, VQ44 | 50 |
| | | XQR18V04 | None | 3.3V | 4M | M, V | CC44 | 30/10 (3) |

**Notes:**
(1) Xilinx Configuration PROMs have adjustable IO voltages for compatiblity with all Xilinx FPGAs
(2) The CC44, VQ44, and PC44 packages are footprint / pin compatible
(3) 18V04 TID is 10krads for reprogramming circuitry; 30 krads for data retention

## Device Nomenclatures



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# Xilinx Configuration Storage Solutions

http://www.xilinx.com/configsolns

## Product Selection and Package Option Matrix

### Platform Flash Device Cross Reference

| Platform Flash | PROM Solution |
|---|---|
| **Spartan-3** | |
| XC3S50 | XCF01S |
| XC3S200 | XCF01S |
| XC3S400 | XCF02S |
| XC3S1000 | XCF04S |
| XC3S1500 | XCF08P |
| XC3S2000 | XCF08P |
| XC3S4000 | XCF16P |
| XC3S5000 | XCF16P |
| **Spartan-IIE** | |
| XC2S50E | XCF01S |
| XC2S100E | XCF01S |
| XC2S150E | XCF02S |
| XC2S200E | XCF02S |
| XC2S300E | XCF02S |
| XC2S400E | XCF04S |
| XC2S600E | XCF04S |
| **Spartan-II** | |
| XC2S15 | XCF01S |
| XC2S30 | XCF01S |
| XC2S50 | XCF01S |
| XC2S100 | XCF01S |
| XC2S150 | XCF01S |
| XC2S200 | XCF02S |
| **Spartan-XL** | |
| XCS05XL | XCF01S |
| XCS10XL | XCF01S |
| XCS20XL | XCF01S |
| XCS30XL | XCF01S |
| XCS40XL | XCF01S |

| Platform Flash | PROM Solution |
|---|---|
| **Virtex-II Pro** | |
| XC2VP2 | XCF02S |
| XC2VP4 | XCF04S |
| XC2VP7 | XCF08P |
| XC2VP20 | XCF08P |
| XC2VP30 | XCF16P |
| XC2VP40 | XCF16P |
| XC2VP50 | XCF32P |
| XC2VP70 | XCF32P |
| XC2VP100 | XCF32P* |
| XC2VP125 | XCF32P** |
| **Virtex-II** | |
| XC2V40 | XCF01S |
| XC2V80 | XCF01S |
| XC2V250 | XCF02S |
| XC2V500 | XCF04S |
| XC2V1000 | XCF04S |
| XC2V1500 | XCF08P |
| XC2V2000 | XCF08P |
| XC2V3000 | XCF16P |
| XC2V4000 | XCF16P |
| XC2V6000 | XCF32P |
| XC2V8000 | XCF32P |

* assumes bitstream compression is used (XCF32P + XCF01S without compression).
** assumes bitstream compression is used (XCF32P + XCF16P without compression).

**Note:** For information regarding legacy PROMs, visit **http://www.xilinx.com/legacyproms**

### Platform Flash Family Features and Packages

| | XCF01S | XCF02S | XCF04S | XCF08P | XCF16P | XCF32P |
|---|---|---|---|---|---|---|
| Density | 1Mb | 2Mb | 4Mb | 8Mb | 16Mb | 32Mb |
| JTAG Prog | Y | Y | Y | Y | Y | Y |
| Serial Configuration | Y | Y | Y | Y | Y | Y |
| SelectMap Configuration | | | | Y | Y | Y |
| Compression | | | | Y | Y | Y |
| Design Rev | | | | Y | Y | Y |
| VCC (V) | 3.3 | 3.3 | 3.3 | 1.8 | 1.8 | 1.8 |
| VCCO (V) | 1.8 – 3.3 | 1.8 – 3.3 | 1.8 – 3.3 | 1.5 – 3.3 | 1.5 – 3.3 | 1.5 – 3.3 |
| VCCJ (V) | 1.8 – 3.3 | 1.8 – 3.3 | 1.8 – 3.3 | 1.5 – 3.3 | 1.5 – 3.3 | 1.5 – 3.3 |
| Clock (MHz) | 33 | 33 | 33 | 40 | 40 | 40 |
| Package | VO20 | VO20 | VO20 | FS48 | FS48 | FS48 |
| | | | | VO48 | VO48 | VO48 |

For multiple FPGA Configuration and for designs utilizing system level features, use SystemACE™.

| SystemACE | Memory Density | Number of Components | Min Board Space | Compression | FPGA Config. Mode | Multiple Designs | Software Storage | Removable | IRL Hooks | Max Config. Speed | Non-Volatile Media |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SystemACE CF | Up to 8 Gbit | 2 | 25 cm² | No | JTAG | Unlimited | Yes | Yes | Yes | 30 Mbit/sec | CompactFlash |
| SystemACE SC | 16 Mbit 32 Mbit 64 Mbit | 3 | Custom | Yes | SelectMAP (up to 4 FPGA) Slave-Serial (up to 8 FPGA chains) | Up to 8 | No | No | Yes | 152 Mbit/sec | AMD Flash Memory |

Pb-free solutions are available. For more information about Pb-free solutions visit www.xilinx.com/pbfree.

**Important: Verify all data in this document with the device data sheets found at http://www.xilinx.com/partinfo/databook.htm**

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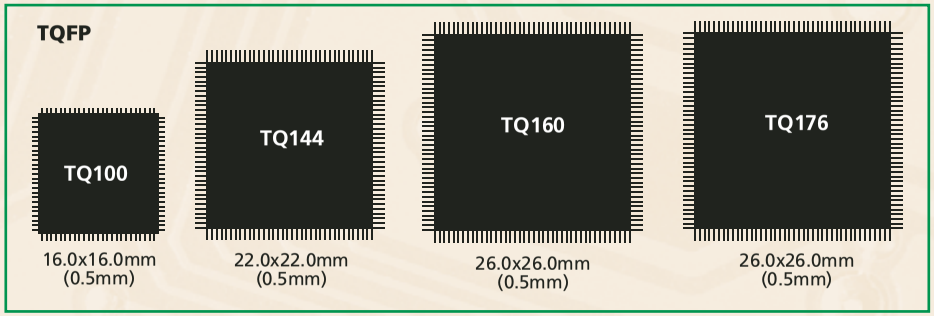
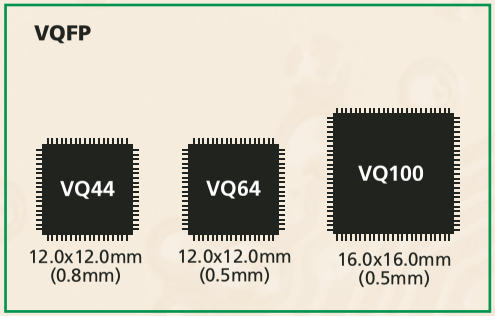
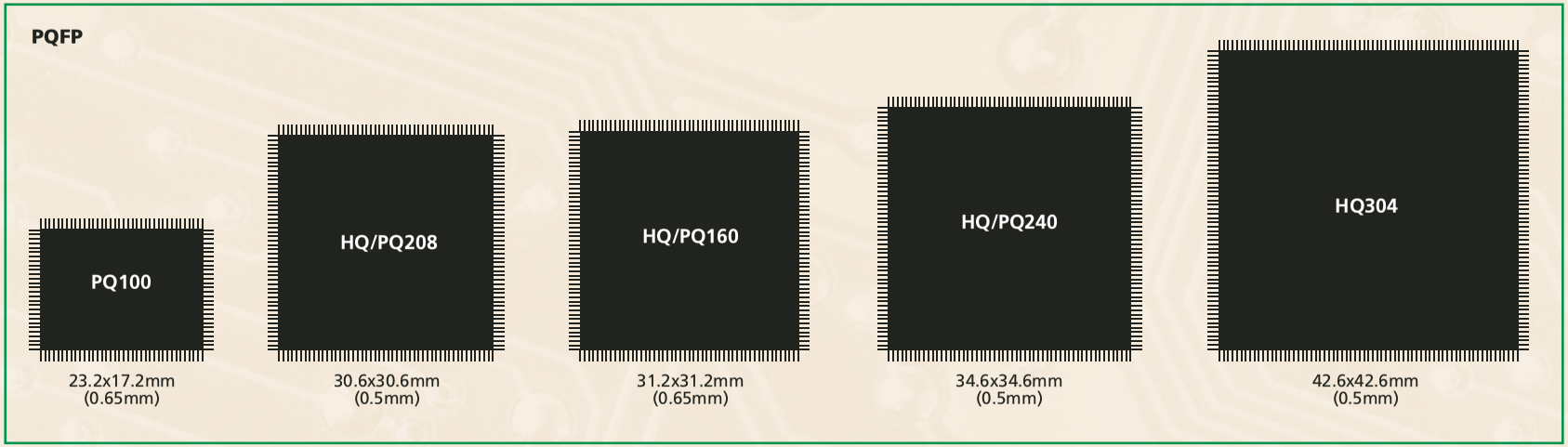
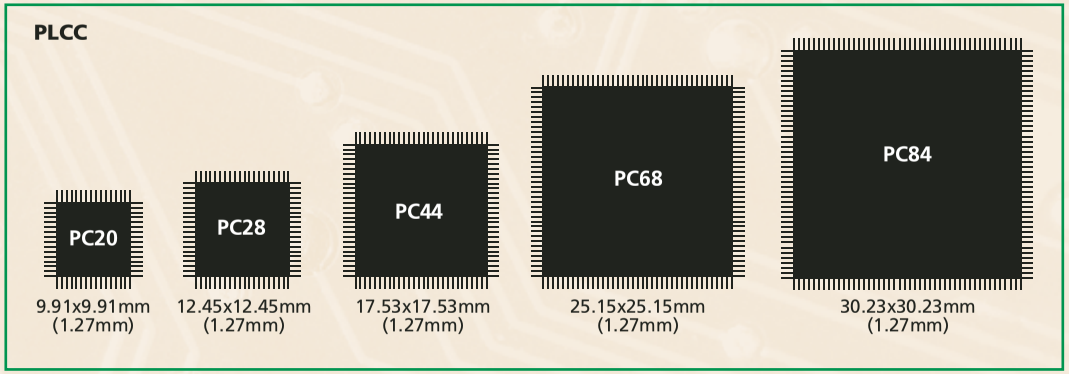
# Xilinx Packaging

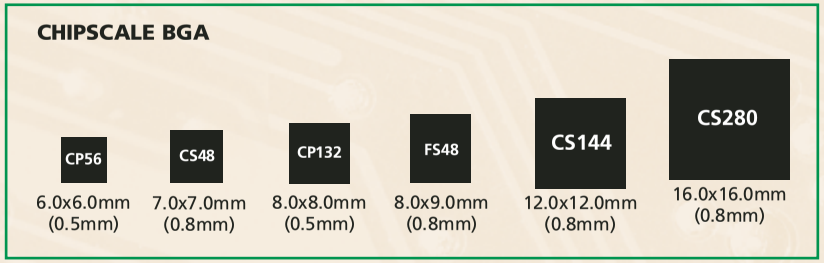
http://www.xilinx.com/packaging




**Note:** 1. Package outlines shown are actual size.
2. For lead-frame packages, dimensions (D & E) shown are inclusive of leads. Dimensions in parentheses represent package pitch.

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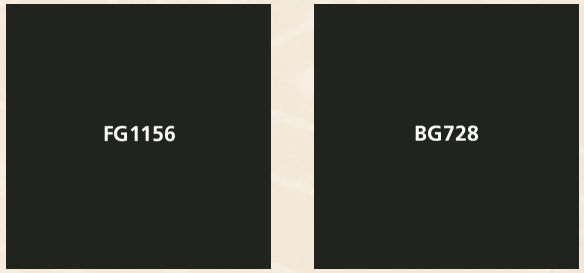
# Xilinx Packaging

http://www.xilinx.com/packaging

## PLASTIC OVERMOLDED BGA (CAVITY UP)

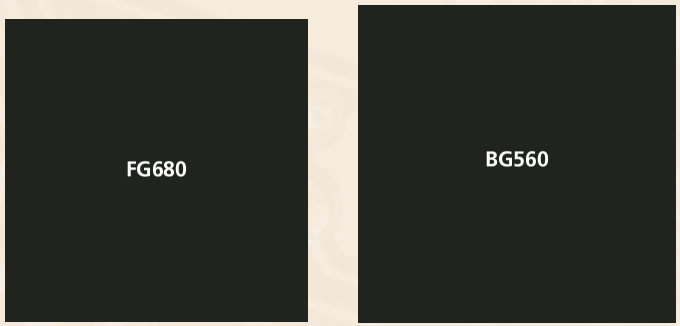
17.0x17.0mm (1.0mm) | 17.0x17.0mm (1.0mm) | 19.0x19.0mm (1.0mm) | 23.0x23.0mm (1.0mm) | 23.0x23.0mm (1.0mm) | 27.0x27.0mm (1.0mm) | 27.0x27.0mm (1.27mm) | 31.0x31.0mm (1.27mm) | 31.0x31.0mm (1.0mm)

## PLASTIC OVERMOLDED BGA (CAVITY UP) CONTINUED




35.0x35.0mm (1.0mm) | 35.0x35.0mm (1.27mm)

## METAL BGA (CAVITY DOWN)




40.0x40.0mm (1.0mm) | 42.5x42.5mm (1.27mm)

**Note:** 1. Package outlines shown are actual size.
2. Dimesions referenced in parenthesis represent package pitch.

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# Xilinx Packaging

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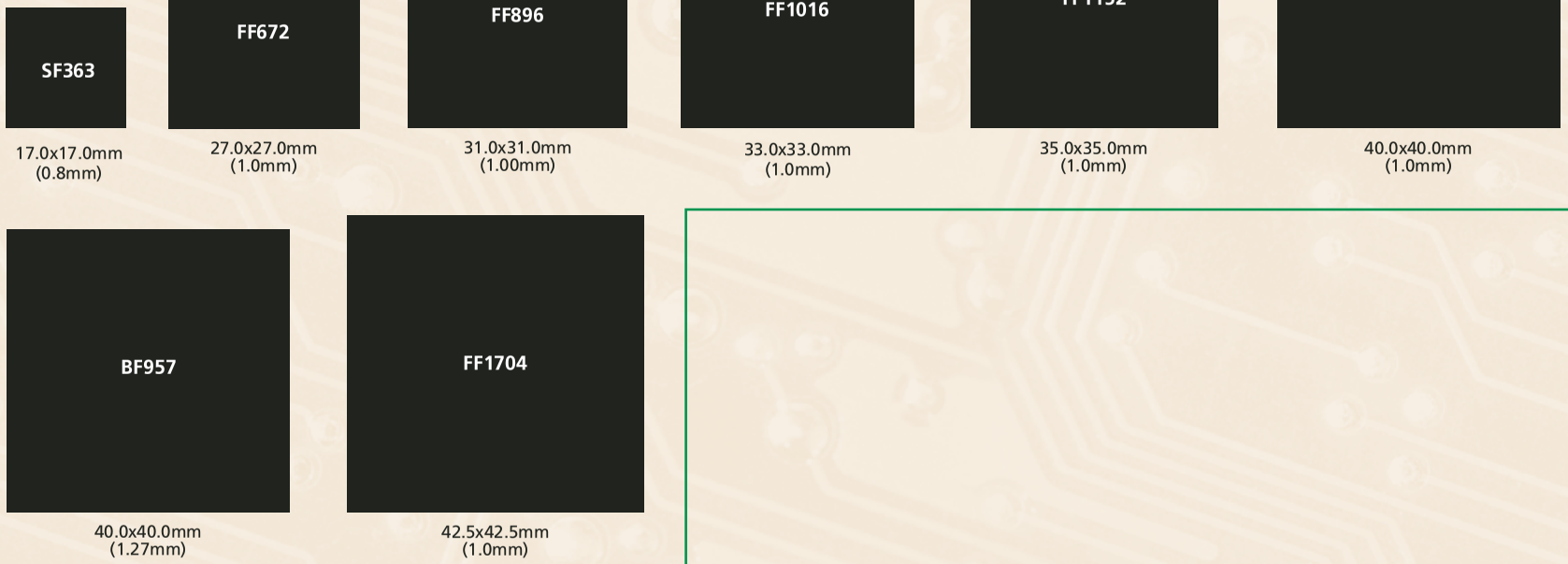
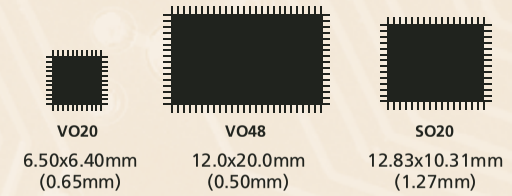
## FLIP-CHIP BGA




## TSOP/TSSOP/SOIC



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# Xilinx Software – ISE 6.2i

http://www.xilinx.com/ise

| | Feature | *ISE WebPACK™* | *ISE BaseX* | *ISE Foundation* | *ISE Alliance* |
|---|---|---|---|---|---|
| **Devices** | Virtex™ Series | **Virtex-E:** V50E -V300E<br>**Virtex-II:** 2V40 - 2V250<br>**Virtex-II Pro:** 2VP2 | **Virtex:** V50 - V600<br>**Virtex-E:** V50E - V600E<br>**Virtex-II:** 2V40 - 2V500<br>**Virtex-II Pro:** 2VP2, 2VP4, 2VP7 | ALL | ALL |
| | Spartan™ Series | **SpartanII/IIE:** ALL (except XC2S400E and XC2S600E)<br>**Spartan-3:** 3S50, 3S200, 3S400 | **Spartan-II/IIE:** ALL<br>**Spartan-3:** 3S50, 3S200, 3S400 | **Spartan-II/IIE:** ALL<br>**Spartan-3:** ALL | **Spartan-II/IIE:** ALL<br>**Spartan-3:** ALL |
| | CoolRunner™ XPLA3<br>CoolRunner-II | ALL | ALL | ALL | ALL |
| | XC9500 Series | ALL | ALL | ALL | ALL |
| **Design Entry** | Schematic Editor | Yes | MS Windows and Linux only | MS Windows and Linux only | No |
| | HDL Editor | Yes | Yes | Yes | Yes |
| | State Diagram Editor | Yes | MS Windows only | MS Windows only | MS Windows only |
| | CORE Generator System | No | Yes | Yes | Yes |
| | PACE (Pinout and Area Constraint Editor) | Yes | Yes | Yes | Yes |
| | Architecture Wizards<br>DCM - Digital Clock Management<br>MGT - Multi-Gigabit Transcievers | Yes | Yes | Yes | Yes |
| | 3rd Party RTL Checker Support | Yes | Yes | Yes | Yes |
| | Xilinx System Generator for DSP | No | Sold as an Option | Sold as an Option | Sold as an Option |
| **Embedded System Design** | Xilinx Embedded Development Kit (EDK) | No | Sold as an Option | Sold as an Option | Sold as an Option |
| | WindRiver Xilinx Edition Development Tools<br>Diab C/C++ Compiler<br>SingleStep Debugger<br>visionPROBE II target connection | No | Sold as an Option | Sold as an Option | Sold as an Option |
| **Synthesis** | Xilinx Synthesis Technology (XST) | Yes | Yes | Yes | No |
| | Synplicity Synplify/Pro | Integrated Interface | Integrated Interface (MS Windows only) | Integrated Interface (MS Windows only) | Integrated Interface (MS Windows only) |
| | Synplicity Amplify Physical Synthesis Support | Yes | Yes | Yes | Yes |
| | Mentor Graphics Leonardo Spectrum | Integrated Interface | Integrated Interface | Integrated Interface | Integrated Interface |
| | Mentor Graphics Precision RTL | EDIF only | EDIF only | EDIF only | EDIF only |
| | Synopsys FPGA Compiler II | EDIF Interface | EDIF Interface | EDIF Interface | EDIF Interface |
| | ABEL | CPLD | CPLD (MS Windows only) | CPLD (MS Windows only) | CPLD (MS Windows only) |

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# Xilinx Software – ISE 6.2i

http://www.xilinx.com/ise

| | Feature | *ISE WebPACK™* | *ISE BaseX* | *ISE Foundation* | *ISE Alliance* |
|---|---|---|---|---|---|
| **Implementation** | FloorPlanner | Yes | Yes | Yes | Yes |
| | Constraints Editor | Yes | Yes | Yes | Yes |
| | Timing Driven Place & Route | Yes | Yes | Yes | Yes |
| | Modular Design | No | Yes | Yes | Yes |
| | Timing Improvement Wizard | Yes | Yes | Yes | Yes |
| **Programming** | iMPACT | Yes | Yes | Yes | Yes |
| | System ACE Configuration Manager | Yes | Yes | Yes | Yes |
| **Board Level Integration** | IBIS Models | Yes | Yes | Yes | Yes |
| | STAMP Models | Yes | Yes | Yes | Yes |
| | HSPICE Models* | Yes | Yes | Yes | Yes |
| **Verification** | ChipScope™ Pro | Sold as an Option | Sold as an Option | Sold as an Option | Sold as an Option |
| | HDL Bencher™ | Yes | MS Windows only | MS Windows only | MS Windows only |
| | ModelSim® Xilinx Edition (MXE II) | ModelSim XE II Starter** | ModelSim XE II Starter** | ModelSim XE II Starter** | ModelSim XE II Starter** |
| | Static Timing Analyzer | Yes | Yes | Yes | Yes |
| | FPGA Editor with Probe | No | Yes | Yes | Yes |
| | ChipViewer | Yes | Yes | Yes | Yes |
| | XPower (Power Analysis) | Yes | Yes | Yes | Yes |
| | 3rd Party Equivalency Checking Support | Yes | Yes | Yes | Yes |
| | SMARTModels for PPC and RocketIO | No | Yes | Yes | Yes |
| | 3rd Party Simulator Support | Yes | Yes | Yes | Yes |
| **Platforms** | | PC (MS Windows 2000/MS Windows XP) | PC (MS Windows 2000/MS Windows XP), Linux | PC (MS Windows 2000/MS Windows XP), Sun Solaris, Linux | PC(MS Windows 2000/MS Windows XP), Sun Solaris, Linux |
| **IP/CORE** | For more information on the complete list of Xilinx IP products, visit the Xilinx IP Center at http://www.xilinx.com/ipcenter | | | | |

*HSPICE Models available at the Xilinx Design Tools Center at www.xilinx.com/ise.
**MXE II supports the simulation of designs up to 1 million system gates and is sold as an option.

For more information, visit the Xilinx Design Tools Center at www.xilinx.com/ise

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# Xilinx On Board – Development Reference Boards

http://www.xilinx.com/board_search

| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Spartan-3** | | | | |
| ADS-S3-MB-EVL400 | Spartan-3 Evaluation Kit w/MicroBlaze and Communications/ Memory Module | Avnet Design Services | XC3S400 | Networking, telecommunication, data communication, embedded and consumer markets |
| ADS-XLX-SP3-EVL1500 | Spartan-3 Evaluation Kit with 3S1500 device | Avnet Design Services | XC3S1500-4FG676 | Very cost effective Spartan-3 evaluation platform; allows experimentation with the advanced features of the Spartan-3 1500 device |
| ADS-XLX-SP3-EVL400 | Spartan-3 Evaluation Kit with 3S400 device | Avnet Design Services | XC3S400 | Very cost effective Spartan-3 evaluation platform; allows experimentation with the advanced features of the Spartan-3 400 device |
| DS-KIT-3SLC400* | Spartan-3 LC Development Kit | Insight (Memec) | XC3S400-4PQ208 | General purpose Spartan-3 development platform |
| DS-KIT-3SLC400-BAS | Spartan-3 LC Development Kit w/ISE Foundation and JTAG Cable | Insight (Memec) | XC3S400-4PQ208 | General purpose Spartan-3 development platform |
| DS-KIT-3SLC400-PAK* | Spartan-3 LC Development Kit w/ WebPACK CD and JTAG Cable | Insight (Memec) | XC3S400-4PQ208 | General purpose Spartan-3 development platform |
| DS-KIT-3SMB1500* | Spartan-3 MB 3S1500 Development Kit | Insight (Memec) | XC3S1500-4FG676 | General purpose Spartan-3 development platform |
| DS-KIT-3SMB1500-ISE | Spartan-3 MB 3S1500 Development Kit w/ISE Foundation and JTAG Cable | Insight (Memec) | XC3S1500-4FG676 | General purpose Spartan-3 development platform |
| DS-KIT-MB-3SLC400 | Spartan-3 MicroBlaze Development Kit | Insight (Memec) | XC3S400-4FG676 | Embedded microprocessor |
| DS-KIT-MB-3SMB1500 | Spartan-3 MicroBlaze Development Kit | Insight (Memec) | XC3S1500-4FG676 | Embedded microprocessor |
| HW-AFX-SP3-1500-DB | NuHo 3S1500 Development Board | NuHorizons | XC3S1500 | Prototyping, Microblaze Soft Processor Development, DSP, Industrial Systems, Data Communications / Telecommunications |
| HW-AFX-SP3-400-DB | NuHo 3S400 Development Board | NuHorizons | XC3S400-4PQ208C | Prototyping, Microblaze Soft Processor Development, DSP, Industrial Systems, Data Communications / Telecommunications |
| **Spartan-IIE** | | | | |
| ADS-S2E-US2-SOL | Xilinx & Cypress USB 2.0 to SCSI System Solution Kit | Avnet Design Services | XC2S300E-PQ208 | Complete solution for interfacing a SCSI drive to a host computer using Universal Serial Bus Specification Revision 2.0 - provides the designer with a Windows ready USB 2.0 to SCSI demonstration design |
| ADS-SP2E-MB-EVL | Spartan-IIE Evaluation Kit w/MicroBlaze & Communications/ Memory Module | Avnet Design Services | XC2S200E | Prototyping, Digital Video, Multimedia, Telecom/Datacom |
| ADS-XLX-SP2E-EVL | Spartan-IIE Evaluation Kit | Avnet Design Services | XC2S200E-6FT256C | Prototyping, Telecom/Datacom |
| DS-KIT-MB-S2E3LC | Spartan-IIE MicroBlaze Kit | Insight (Memec) | Spartan-IIE | Embedded microprocessor |
| DS-KIT-MB-S2E6LC | Spartan-IIE MicroBlaze Kit | Insight (Memec) | Spartan-IIE | Embedded microprocessor |
| DS-KIT-S2E3LC* | Spartan-IIE LC 2S300E Development Kit | Insight (Memec) | XC2S300E-6FG456C | General purpose Spartan-3 development platform |
| DS-KIT-S2E3LC-ISE-BAS | Spartan-IIE LC Development Kit w/ISE BaseX | Insight (Memec) | XC2S300E-6FG456C | |
| DS-KIT-S2E6LC* | Spartan-IIE LC 2S600E Development Kit | Insight (Memec) | XC2S600E-6FG456C | |
| DS-KIT-S2E6LC-ISE-BAS | Spartan-IIE LC 2S600E Development Kit w/ISE BaseX | Insight (Memec) | XC2S600E-6FG456C | |
| iDEV2 | CAN, LIN and TTCAN Development Platform and Starter Kit | Intelliga Integrated Design, Ltd. | XC2S300E | Automotive, Industrial |
| HW-AFX-DIGI-2S200E | Spartan-IIE Development Board | NuHorizons | XC2S200E | Prototyping, DSP, Multimedia, Reconfigurable Computing |

* Insight Products: Append -EURO to part number for international kits (ex. DS-KIT-2SLC100-EURO); Power Supply not included in -EURO kits

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# Xilinx On Board – Development Reference Boards

http://www.xilinx.com/board_search

| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Spartan-II** | | | | |
| ADS-SP2-MB-EVL | Spartan-II Evaluation Kit w/MicroBlaze & Communications/ Memory Module | Avnet Design Services | XC2S150-5PQ208 | Networking, telecommunication, data communication, embedded and consumer markets |
| ADS-XLX-SP2-EVL | Spartan-II Evaluation Kit | Avnet Design Services | XC2S150-5PQ208 | Very cost effective evaluation and prototyping platform to develop and test designs that are targeted to the Xilinx Spartan-II FPGA family - helps shorten and simplify the design cycle |
| 2D Fabric Board | 2D Fabric Evaluation and Demo Board | Crossbow Technologies, Inc. | XC2S150 | Multi-processing system development; Networking, wireless basestations, VoP gateways |
| DS-KIT-2S100* | Spartan-II 100 Development Kit | Insight (Memec) | XC2S100 | DSP, Digital Video, IP-Based Systems, Image Processing |
| DS-KIT-2S200* | Spartan-II PCI 2S200 Development Kit | Insight (Memec) | XC2S200-6FG456C | DSP, Digital Video, IP-Based Systems, Image Processing, PCI, Reconfigurable Computing |
| DS-KIT-2S200-ISE-BAS | Spartan-II PCI 2S200 Development Kit w/ISE BaseX and JTAG Cable | Insight (Memec) | XC2S200-6FG456C | DSP, Digital Video, IP-Based Systems, Image Processing, PCI, Reconfigurable Computing |
| DS-KIT-2S200-PAK* | Spartan-II PCI 2S200 Development Kit w/WebPACK CD and JTAG Cable | Insight (Memec) | XC2S200-6FG456C | DSP, Digital Video, IP-Based Systems, Image Processing, PCI, Reconfigurable Computing |
| DS-KIT-2SLC100* | Spartan-II LC 2S100 Development Kit | Insight (Memec) | XC2S100-5PQ208C | General purpose Spartan-II development platform |
| DS-KIT-2SLC100-ISE-BAS | Spartan-II LC 2S100 Development Kit w/ISE BaseX and JTAG Cable | Insight (Memec) | XC2S100-5PQ208C | General purpose Spartan-II development platform |
| DS-KIT-2SLC100-PAK* | Spartan-II LC 2S100 Development Kit w/WebPACK CD and JTAG Cable | Insight (Memec) | XC2S100-5PQ208C | General purpose Spartan-II development platform |
| DS-KIT-MBLAZE-S2 | Spartan-II MicroBlaze Kit | Insight (Memec) | Spartan-II | Embedded microprocessor |
| DS-KIT-PCI32S-200 | Spartan-II 200 PCI Development Kit w/Xilinx Single Project PCI325 License | Insight (Memec) | XC2S200 | DSP, Digital Video, Image Processing, PCI, Reconfigurable Computing |
| RT-DAC4/PCI-D-OMNI | Digital OMNI Board | INTECO | XC2S100, XC2S150, XC2S50 | ASIC Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/ Deserialization, Telecom / Datacom, Telematics, VoIP |
| RT-DAC4/PCI-OMNI | OMNI Board | INTECO | XC2S100, XC2S150, XC2S50 | ASIC Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/ Deserialization, Telecom / Datacom, Telematics, VoIP |
| MicroEngine V | CPU + FPGA (Virtex/Spartan-II) MicroEngine Cards | Intrinsyc, Inc. | Spartan-II | Embedded Systems |
| NPE565-M | Spartan-II Power-PC Engine | North Pole Engineering | XC2S200 | Prototyping, DSP, Embedded System, Industrial Automotive, Reconfigurable Computing |
| NV-FPSD-001 | FPGA SDRAM Controller Evaluation Board | Novtech | XC2S50 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/Deserialization, Telecom / Datacom, Telematics, VoIP |
| SPCMUSB-EVL | USB 2.0 Mass Storage Class Reference Design | Specsoft Consulting, Inc. | XC2S200 | Prototyping, Data Storage, Embedded System, IP-Based Systems |
| SPCVUSB-EVL | USB 2.0 Video Class Reference Design | Specsoft Consulting, Inc. | XC2S200 | Prototyping, Data Transmission & Manipulation, Embedded System, IP-Based Systems |

* Insight Products: Append -EURO to part number for international kits (ex. DS-KIT-2SLC100-EURO); Power Supply not included in -EURO kits

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II Pro** | | | | |
| ADM-XPL | Reconfigurable Computer Based on Virtex-II Pro | Alpha Data | XC2VP7, XC2VP20 | DSP, Reconfigurable Computing , Image Processing , ASIC Prototyping |
| PCI Platform | Virtex-II Pro PCI Platform FPGA Development Board | Amirix Systems, Inc. | XC2VP7,XC2VP20, XC2VP30 | Networking (SAN, VoIP, Bridges), Communications, DSP, Image Processing, Industrial Controls, Instrumentation, test and measurement |
| ADS-XLX-V2PRO-DEVP20-6 | Virtex-II Pro Development Kit w/XC2VP20, -6 speed grade | Avnet Design Services | XC2VP20 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Navigation, PCI, Reconfigurable Computing, Serial / Deserialization |
| ADS-XLX-V2PRO-DEVP30-6 | Virtex-II Pro Development Kit w/XC2VP30, -6 speed grade | Avnet Design Services | XC2VP30 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Navigation, PCI, Reconfigurable Computing, Serial / Deserialization |
| ADS-XLX-V2PRO-DEVP7-5 | Virtex-II Pro Development Kit w/Xc2VP7, -5 speed grade | Avnet Design Services | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Navigation, PCI, Reconfigurable Computing, Serial / Deserialization |
| ADS-XLX-V2PRO-DEVP7-6 | Virtex-II Pro Development Kit w/Xc2VP7, -6 speed grade | Avnet Design Services | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Navigation, PCI, Reconfigurable Computing, Serial / Deserialization |
| ADS-XLX-V2PRO-EVLP7-5 | Virtex-II Pro Evaluation Kit w/Xc2VP7, -5 speed grade | Avnet Design Services | XC2VP7 | Very cost effective evaluation and prototyping platform to develop and test designs targeted to the Virtex-II Pro device |
| ADS-XLX-V2PRO-EVLP7-6 | Virtex-II Pro Evaluation Kit w/Xc2VP7, -6 speed grade | Avnet Design Services | XC2VP7 | Very cost effective evaluation and prototyping platform to develop and test designs targeted to the Virtex-II Pro device |
| V2PRO Kit | Virtex-II Pro™ Development Kit | Avnet Design Services | XC2VP7, XC2VP20, SC2VP30 | Packet switching; network security; SAN, servers and super computers; video computing/ transmission; High-speed serial interfaces |
| D6PC | Danube 6-PaC | BittWare, Inc. | XC2VP20 | DSP, Data Transmission & Manipulation, Embedded System, Image Processing, Multimedia, Reconfigurable Computing, Telecom/Datacom |
| DN6000K10S | DN6000K10S ASIC Prototyping Engine | DINI Group | XC2VP125, XC2VP70 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/Deserialization, Datacom / Telecom, Telematics, VoIP |
| DS-KIT-2VP20FF1152* | Virtex-II Pro FF1152 P20 Development Kit | Insight (Memec) | XC2VP20 in FF1152 | |
| DS-KIT-2VP30FF1152* | Virtex-II Pro FF1152 P30 Development Kit | Insight (Memec) | XC2VP30 in FF1152 | |
| DS-KIT-2VP4FF672* | Virtex-II Pro FF672 P4 Development Kit | Insight (Memec) | XC2VP4 in FF672 | |
| DS-KIT-2VP4FG456* | Virtex-II Pro P4 FG456 Development Kit | Insight (Memec) | XC2VP4 in FG456 | DSP, Digital Video, Embedded System, IP-Based Systems, Image Processing |
| DS-KIT-2VP7FF672* | Virtex-II Pro FF672 P7 Development Kit - EURO | Insight (Memec) | XC2VP7 in FF672 | |
| DS-KIT-2VP7FG456* | Virtex-II Pro P7 FG456 Development Kit | Insight (Memec) | XC2VP7 in FG456 | DSP, Digital Video, Embedded System, IP-Based Systems, Image Processing |
| BenPRO-2VP7-6 | BenPRO | Nallatech | XC2VP7-XC2VP20 | Data Networks & Digital Signal processing, Embedded System, Telecom |
| SMT387 | Disk Storage Module | Sundance Multiprocessor Co. | XC2VP20 | DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Encryption Devices, Image Processing, Reconfigurable Computing |
| TB-V2P-20-MGT | Virtex-II Pro Rocket I/O Evaluation Board | Tokyo Electron Device Limited | XC2VP20-6FF896 | Prototyping, DSP, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Reconfigurable Computing, Serial / Deserialization |
| TB-V2P-30-MGT | Virtex-II Pro Rocket I/O Evaluation Board | Tokyo Electron Device Limited | XC2VP30-6FF896 | Prototyping, DSP, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Reconfigurable Computing, Serial / Deserialization |

* Insight Products: Append -EURO to part number for international kits (ex. DS-KIT-2SLC100-EURO); Power Supply not included in -EURO kits. For Virtex-II Pro, 2VP40 and 2VP50 boards are available upon customer request.

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# Xilinx On Board – Development Reference Boards

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II Pro** | | | | |
| TB-V2P-7-MGT | Virtex-II Pro Rocket I/O Evaluation Board | Tokyo Electron Device Limited | XC2VP7-6FF896 | Prototyping, DSP, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Reconfigurable Computing, Serial / Deserialization |
| XSP-016 | Virtex-II Pro PowerPC&MicroBlaze Evaluation Board | Tokyo Electron Device Limited | XC2VP7-5FG456 | Prototyping, DSP, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Reconfigurable Computing |
| DO-V2P-ML300-EC | Virtex-II Pro ML300 Evaluation Platform- EC version | Xilinx Online Store | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serialization / Deserialization, Telecom |
| DO-V2P-ML300-UK | Virtex-II Pro ML300 Evaluation Platform- UK version | Xilinx Online Store | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serialization / Deserialization, Telecom |
| DO-V2P-ML300-USA | Virtex-II Pro ML300 Evaluation Platform- US version | Xilinx Online Store | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serialization / Deserialization, Telecom / Datacom, Telematics, VoIP |
| DO-V2P-ML300-WRS-EC | Virtex-II Pro ML300 Evaluation Platform with WindRiver tools - EC version | Xilinx Online Store | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serialization / Deserialization, Telecom |
| DO-V2P-ML300-WRS-UK | Virtex-II Pro ML300 Evaluation Platform with WindRiver tools - UK version | Xilinx Online Store | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serialization / Deserialization, Telecom |
| DO-V2P-ML300-WRS-USA | Virtex-II Pro ML300 Evaluation Platform with WindRiver tools - US version | Xilinx Online Store | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serialization / Deserialization, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-FF1152-300 | Virtex-II Pro Proto Board | Xilinx Online Store | XC2VP20, XC2VP30, XC2VP40, XC2VP50 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Navigation, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-FF672-300 | Virtex-II Pro Proto Board | Xilinx Online Store | XC2VP2, XC2VP4, XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Navigation, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-FG456-300 | Virtex-II Pro Proto Board | Xilinx Online Store | XC2VP2, XC2VP4, XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Navigation, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-SMA-HSSDC2 | SMA To HSSDC2 Conversion Module | Xilinx Online Store | Supports boards with SMA connectors | |
| HW-AFX-SMA-RJ45 | SMA To RJ45 Conversion Module | Xilinx Online Store | Supports boards with SMA connectors | |
| HW-AFX-SMA-SATA | SMA To SATA Conversion Module | Xilinx Online Store | Supports boards with SMA connectors | |
| HW-AFX-SMA-SFP | SMA To SFP Conversion Module | Xilinx Online Store | Supports boards with SMA connectors | |
| DO-V2P-ML300-USA | Virtex-II Pro ML300 Evaluation Platform- US version | Xilinx Sales Offices | XC2VP7 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Procesing, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, Telematics, VoIP |
| HW-V2PRO-XLVDS | Virtex-II Pro XLVDS | Xilinx Sales Offices | XC2VP20 | Data Transmission & Manipulation, Embedded System, Encryption Devices, IP-Based Systems, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, Test Equipment |

* Insight Products: Append -EURO to part number for international kits (ex. DS-KIT-2SLC100-EURO); Power Supply not included in -EURO kits

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# Xilinx On Board – Development Reference Boards

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II** | | | | |
| ADM-XPL/2VP7-5 | ADM-XPL | Alpha Data | XC2V1000, XC2VP20, XC2VP7 | Prototyping, DSP, Image Processing, Reconfigurable Computing |
| ADM-XRC-II | ADM-XRC-II | Alpha Data | XC2V3000, XC2V4000, XC2V6000, XC2V8000 | Prototyping, Compression, DSP, Encryption, Reconfigurable COmputing, Software Radio, Video / Image Processing, XML processing |
| ADS-V2-MB-DEV4000XP | Virtex-II XC2V4000XP Development Kit with MicroBlaze | Avnet Design Services | XC2V4000 | Prototyping. Data Transmission & Manipulation, Highend DSP, IP-Based Systems, PCI |
| ADS-V2-MB-DEV6000XP | Virtex-II XC2V6000 Development Kit with MicroBlaze | Avnet Design Services | XC2V6000 | Prototyping. Data Transmission & Manipulation, Highend DSP, IP-Based Systems, PCI |
| ADS-XLX-MB-DEV1500 | Virtex-II XC2V1500 Development Kit with MicroBlaze | Avnet Design Services | XC2V1500 | Prototyping, Data Transmission & Manipulation, High End DSP, IP-based Systems, PCI |
| ADS-XLX-MB-DEV4000 | Virtex-II XC2V4000 Development Kit with MicroBlaze | Avnet Design Services | XC2V4000 | Prototyping, Data Transmission & Manipulation, High End DSP, IP-based Systems, PCI |
| ADS-XLX-PMC-IRL PMC IRL | Reference Design Kit | Avnet Design Services | XC2V1000-4FG456C/FF896C | Consumer, Industrial, IRL, PAVE, Telecom/Datacom, Telecommunications |
| ADS-XLX-V2-DEV1500 | Virtex-II Development Kit w/XC2V1500 device | Avnet Design Services | XC2V1500 | Complete hardware environment to develop, prototype, and test designs targeted to the Virtex-II FPGA family |
| ADS-XLX-V2-DEV4000 | Virtex-II XC2V4000 Development Kit w/XC2V4000 device | Avnet Design Services | XC2V4000 | Prototyping, Data Transmission & Manipulation, High End DSP, IP-based Systems, PCI |
| ADS-XLX-V2-DEV4000XP | Virtex-II XC2V4000XP Development Kit w/high-current power supply | Avnet Design Services | XC2V4000 | Prototyping. Data Transmission & Manipulation, Highend DSP, IP-Based Systems, PCI |
| ADS-XLX-V2-DEV6000XP | Virtex-II XC2V6000 Development Kit w/high-current power supply | Avnet Design Services | XC2V6000 | Prototyping. Data Transmission & Manipulation, Highend DSP, IP-Based Systems, PCI |
| ADS-XLX-V2-EVL1000 | Virtex-II XC2V1000 Evaluation Kit | Avnet Design Services | XC2V1000-4FG256 | Prototyping, Data Transmission & Manipulation, High End DSP, IP-based Systems |
| ADS-XLX-XV2-EVL | Virtex-II High-Speed Evaluation Kit | Avnet Design Services | XC2V40 | Data Transmission & Manipulation, DSP |
| BCPM | Barracuda-PMC+ | BittWare, Inc. | XC2V1000 | DSP, Data Transmission & Manipulation, Embedded System, Image Processing, Multimedia, Reconfigurable Computing, Telecom/Datacom |
| RFPM | Reef-PMC+ | BittWare, Inc. | XC2V1000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/Deserialization, Datacom / Telecom, Telematics, VoIP |
| RMPM | Remora-PMC+ | BittWare, Inc. | XC2V1000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/Deserialization, Datacom / Telecom, Telematics, VoIP |
| CYL2T0201-DVK | MetroLink2T-2 Link Layer Evaluation Board | Cypress Semiconductor Corporation | XC2V2000 | Data Transmission & Manipulation, IP-Based Systems, Telecom / Datacom |
| PF3100 | PC/104-Plus Reconfigurable Module Board (PF3100) | Derivation Systems, Inc. | XC2V1000, FG256 | Internet appliance, industrial control |
| DN3000K10 | DN3000K10 ASIC Prototyping Engine | DINI Group | XC2V4000, XC2V6000, XC2V8000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/Deserialization, Telecom/ Datacom, Telematics, VoIP |
| DN3000k10 | DN3000k10 | DINI Group | XC2V4000, XC2V6000, XC2V8000 | Prototyping, Algorithmic Acceleration, Logic Emulation, PCI / PCI-X, Reconfigurable Computing |
| CHM2-VME-604-SZ | Chameleon II VME Reconfigurable Computing Board | DRS Tactical Systems West, Inc. | XC2V6000 | Prototyping, DSP, IP-Based Systems, Image Processing, Reconfigurable Computing, Telecom / Datacom, Telematics |
| APB-2V1000 | Virtex-II Prototyping Board for 2V1000 | ErSt Electronics | XC2V1000 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II** | | | | |
| APB-2V1500 | Virtex-II Prototyping Board for 2V1500 | ErSt Electronics | XC2V1500 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |
| APB-2V2000 | Virtex-II Prototyping Board for 2V2000 | ErSt Electronics | XC2V2000 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |
| APB-2V3000 | Virtex-II Prototyping Board for 2V3000 | ErSt Electronics | XC2V3000 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |
| APB-2V4000 | Virtex-II Prototyping Board for 2V4000 | ErSt Electronics | XC2V4000 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |
| APB-2V6000 | Virtex-II Prototyping Board for 2V6000 | ErSt Electronics | XC2V6000 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |
| APB-2V8000 | Virtex-II Prototyping Board for 2V8000 | ErSt Electronics | XC2V8000 | Prototyping, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Serial / Deserialization, Telecom / Datacom, VoIP |
| GVA-300 | DSP Hardware Accelerator, Virtex-II (GVA-300) | GV & Associates, Inc. | XC2V1500-4, 2000-4 or 3000-4 | DSP |
| GVA-325 | DSP Hardware Accelerator, Virtex-II (GVA-325) | GV & Associates, Inc. | XC2V1500-4, 2000-4 or 3000-4 | DSP |
| GVA-350 | DSP Hardware Accelerator, Virtex-II (GVA-350) | GV & Associates, Inc. | XC2V4000-4, 6000-4 or 8000-4 | DSP |
| DS-KIT-MBLAZE-V2 | Virtex-II MicroBlaze Kit | Insight (Memec) | Virtex-II | Embedded microprocessor |
| DS-KIT-V2LC1000* | Virtex-II LC1000 | Insight (Memec) | XC2V1000 | Digital Video, Image Processing, Telecom / Datacom |
| DS-KIT-V2LC1000-ISE | Virtex-II LC1000 w/ISE Foundation and JTAG Cable | Insight (Memec) | XC2V1000 | Digital Video, Image Processing, Telecom / Datacom |
| DS-KIT-V2MB1000* | Virtex-II MB 2V1000 Development Kit | Insight (Memec) | XC2V1000-4FG456C | DSP, Digital Video, Embedded System, Image Processing, Reconfigurable Computing, Telecom / Datacom, |
| DS-KIT-V2MB1000-ISE | Virtex-II MB 2V1000 Development Kit w/ISE Foundation and JTAG Cable | Insight (Memec) | XC2V1000-4FG456C | DSP, Digital Video, Embedded System, Image Processing, Reconfigurable Computing, Telecom / Datacom, |
| MicroEngine V-II | CPU + FPGA (Virtex-II) MicroEngine Cards | Intrinsyc, Inc. | Virtex-II | Embedded Systems |
| ASPE-1000 | Advanced Signal Processing Engine (ASPE) | Multiple Access Communications | XC2V1000 | DSP, Reconfigurable Computing, Telecom / Datacom |
| BenADDA-2V250-4-xx | BenADDA | Nallatech | XC2V250 - XC2V6000 | Infrared Processing, Mobile Communications Systems, Multi-channel, Multi-mode receivers, Wideband Cable Systems |
| BenBLUE-II-2V4000-4-01 | BenBLUE-II | Nallatech | XC2V4000 - XC2V8000 | ASIC Prototyping, Image Processing, Reconfigurable Computing, Software Defined Radio Data Processing |
| BenDATA-DD-2V3000 | BenDATA-DD | Nallatech | XC2V3000-XC2V8000 | Data Transmission & Manipulation, Image Processing |
| BenDATA-WS-2V4000-4-01 | BenDATA-WS | Nallatech | XC2V4000 - XC2V8000 | Image Processing |
| 42-055-01 | SONET / SDH ATM-POS Board | NetQuest Corporation | XC2V4000 | Data Transmission & Manipulation, Embedded System, IP-Based Systems, Multimedia, Telecom / Datacom |

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II** | | | | |
| 42-059-01 | Gigabit IP Content Processor Board | NetQuest Corporation | XC2V4000 | Data Transmission & Manipulation, Embedded System, IP-Based Systems, Multimedia, Telecom / Datacom |
| 42-060-01 | SONET / SDH / PDH Groomer Board | NetQuest Corporation | XC2V3000 | Data Transmission & Manipulation, Embedded System, IP-Based Systems, Multimedia, Telecom / Datacom |
| XL9000 | XL 9000 Multi-Port Camera Link PCI Frame Grabber | Novtech | XC2V2000 (can be substituted by XC2V2000-XC2V8000) | Data Storage, Data Transmission & Manipulation, Digital Video, Image Processing |
| GR-PCI-XC2V | LEON PCI Virtex II Development Board | Pender Electronic Design | XC2V3000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Low power designs, Multimedia, Navigation, PCI, Reconfigurable Computing, Serial/Deserialization, Telecom / Datacom, Telematics, VoIP |
| JockoBoard | JockoBoard SOC Virtex-II Prototyping Platform | RealFast Operating Systems AB | XC2V1000 | Embedded Systems |
| 600-00422 | PRO-3100 Virtex-II FPGA Processing Engine | Spectrum Signal Processing | XC2V3000, XC2V6000 | DSP, Data Transmission & Manipulation, Reconfigurable Computing |
| 650-00075 | ePMC-8120 | Spectrum Signal Processing | XC2V6000 | DSP, Data transmission & Manipulation, Reconfigurable Computing |
| SMT351-G | Memory Module 351-G | Sundance Multiprocessor Co. | XC2V1000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Communications, Digital Radio Receivers, General Data Logging, IF Radar Sampling, Multi-Channel Receivers, Spectrum Analysers |
| SMT351-M | Memory Module 351-M | Sundance Multiprocessor Co. | XC2V1000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Communications, Digital Radio Receivers, General Data Logging, IF Radar Sampling, Multi-Channel Receivers, Spectrum Analysers |
| SMT365E | DSP Module | Sundance Multiprocessor Co. | XC2V6000 | Image Processing, Industrial, Medical, Telecomunications |
| SMT398-1000-4-Z1 | FPGA Module 1000-4-Z1 | Sundance Multiprocessor Co. | XC2V1000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Communications, Digital Radio Receivers, General Data Logging, IF Radar Sampling, Imaging, Multi-Channel Receivers, Spectrum Analysers |
| SMT398-2000-4-Z1 | FPGA Module 2000-4-Z1 | Sundance Multiprocessor Co. | XC2V2000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Communications, Digital Radio Receivers, General Data Logging, IF Radar Sampling, Imaging, Multi-Channel Receivers, Spectrum Analysers |
| SMT398-3000-4-Z4-Q2 | FPGA Module 3000-4-Z4-Q2 | Sundance Multiprocessor Co. | XC2V3000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Communications, Digital Radio Receivers, General Data Logging, IF Radar Sampling, Imaging, Multi-Channel Receivers, Spectrum Analysers |
| SMT398-8000-4-Z4-Q2 | FPGA Module 8000-4-Z4-Q2 | Sundance Multiprocessor Co. | XC2V8000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Communications, Digital Radio Receivers, General Data Logging, IF Radar Sampling, Imaging, Multi-Channel Receivers, Spectrum Analysers |
| SMT370 | Dual Channel A/D and D/A Module | Sundance Multiprocessor Technology Ltd. | XC2V1000 | Base Band Radar Sampling, Cellular / PCS Base Stations, Digital Radio Receivers, General Data Logging and I/O Control, IF Radar Sampling, Instrumentation, Multi-Channel Receivers, Sonar, Spectrum Analysers |
| XT2000-X | XTENSA Microprocessor Emulation Kit (XT2000-X) | Tensilica, Inc. | XC2V6000-4 | Prototyping, Embedded Systems |
| DO-V2000-MLTA | Virtex-II Multimedia Board | Xilinx Online Store | XC2V2000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded Microprocessor, Embedded System, IP-Based Systems, Image Processing, Multimedia, Reconfigurable Computing, Telecom / Datacom, VoIP |

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II** | | | | |
| HW-AFX-FF1152-200 | FF1152-200 Proto Board | Xilinx Online Store | XC2V3000, XC2V4000, XC2V6000, XC2V8000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded System, Multimedia, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-FG256-200 | FG256-200 Proto Board | Xilinx Online Store | XC2V1000, XC2V250, XC2V40, XC2V500, XC2V80 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded System, Multimedia, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-FG456-200 | FG456 Virtex-II Proto Board | Xilinx Online Store | XC2V1000, XC2V250, XC2V500 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded System, IP-Based Systems, Multimedia, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-FG676-200 | FG676 Virtex-II Proto Board | Xilinx Online Store | XC2V1500, XC2V2000, XC2V3000 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Embedded System, IP-Based Systems, Multimedia, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| DO-DI-DSP-DK2 | XtremeDSP Development Kit | Xilinx Online Store | 2V3000 | High Performance DSP |
| DO-DI-DSP-DK2-SG | XtremeDSP Development Kit + System Generator for DSP | Xilinx Online Store | 2V3000 | Hardware in the loop from Simulink using System Generator software and high performance DSP board |
| **Virtex and Virtex-E** | | | | |
| ADS-VE-MB-DEV | Virtex-E Development Kit w/MicroBlaze | Avnet Design Services | XCV1000E | Networking, telecommunication, data communication, embedded and consumer markets |
| ADS-VE-MB-EVL | Virtex-E Evaluation Kit w/MicroBlaze | Avnet Design Services | XCV100E | Networking, telecommunication, data communication, embedded and consumer markets |
| ADS-XLX-VE-DEV | Virtex-E Development Kit | Avnet Design Services | XCV1000E | Communications, Embeddd Control, LAN Routers, LAN Switch, Networking, WAN Access, xDSL Equipment |
| ADS-XLX-VE-EVL | Virtex-E Evaluation Kit | Avnet Design Services | XCV100E | Very cost effective evaluation and prototyping platform to develop and test designs targeted to the Virtex-E device |
| DN2000k10 | DN2000k10 | DINI Group | XCV1000, XCV1000E, XCV1600E, XCV2000E | Prototyping, Algorithmic Acceleration, Logic Emulation, PCI / PCI-X |
| GVA-290 | DSP Hardware Accelerator, Virtex-E (GVA-290) | GV & Associates, Inc. | 2-XCV1000E, 1600E or 2000E's | DSP |
| BenADIC-2000E | BenADIC | Nallatech | XCV2000E, XCV600E | Multichannel Data Acquisition & Software Radio, Phased Array Radar, Smart Antenna Arrays |
| BenERA-1000E-6-A | BenERA | Nallatech | XCV1000E-XCV2000E | Communications & Real-Time systems, DSP, Image Processing, Reconfigurable Computing |
| BenFAD-2000E | BenFAD | Nallatech | XCV2000E | Broadband wireless/satellite communications, Data Acquisition/signal analysis systems |
| 42-047-01 | SONET / SDH POS PCI NIC Card | NetQuest Corporation | XCV600 | Data Transmission & Manipulation, IP-Based Systems, Multimedia, Telecom / Datacom |
| 42-053-01 | SONET / SDH ATM PCI NIC Card | NetQuest Corporation | XCV600 | Data Transmission & Manipulation, IP-Based Systems, Multimedia, Telecom / Datacom |
| HW-AFX-BG352-100 | BG352-100 Proto Board | Xilinx Online Store | XCV150, XCV200, XCV300 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-BG432-100 | BG432-100 Proto Board | Xilinx Online Store | XCV300/E, XCV400/E, XCV600/E, XCV800 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **Virtex-II** | | | | |
| HW-AFX-BG560-100 | BG560-100 Proto Board | Xilinx Online Store | XCV1000/E, XCV1600E, XCV2000E, XCV400/E, XC405E, XCV600/E, XCV800, XCV812E | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-PQ240-100 | PQ240-100 Proto Board | Xilinx Online Store | XCV100, XCV150, XCV200, XCV300, XCV50 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| HW-AFX-PQ240-110 | PQ240-110 Proto Board | Xilinx Online Store | XCV100, XCV150, XCV200, XCV300, XCV50 | Prototyping, DSP, Data Storage, Data Transmission & Manipulation, Digital Video, Embedded System, IP-Based Systems, Image Processing, Multimedia, Navigation, PCI, Reconfigurable Computing, Telecom / Datacom, Telematics, VoIP |
| **RocketPHY** | | | | |
| HWK-RPHY2XFP-1 | RocketPHY XFP Kit | Xilinx Sales Offices | XGC1120 10G Ultra MSA | Data Storage, Data Storage (10 Gigabit Fibre Channel), Data Transmission & Manipulation, Datacom (10 Gigabit Ethernet), Serial / Deserialization, Telecom (Sonet OC-192 / FEC), Telecom / Datacom |
| HWK-RPHY2XFP-M | RocketPHY XFP Kit with XFP Module | Xilinx Sales Offices | XGC1120 10G Ultra MSA | Data Storage, Data Storage (10 Gigabit Fibre Channel), Data Transmission & Manipulation, Datacom (10 Gigabit Ethernet), Serial / Deserialization, Telecom (Sonet OC-192 / FEC), Telecom / Datacom |
| HWK-RPHY-DVLP | RocketPHY Development Kit | Xilinx Sales Offices | XC2VP20, XGC1120 10G Ultra MSA | Data Storage, Data Storage (10 Gigabit Fibre Channel), Data Transmission & Manipulation, Datacom (10 Gigabit Ethernet), Encryption Devices, Routers, Serial / Deserialization, Telecom (Sonet OC-192 / FEC), Telecom / Datacom, Test Equipment |
| **CoolRunner-II** | | | | |
| ADS-XLX-CR2-EVL | CoolRunner-II Evaluation Kit | Avnet Design Services | XC2C256-VQ100 | Low power designs |
| Digilab-XC2 | Digilent CoolRunner-II Development Board | Digilent | XC2C256 | Low power designs, Telecom / Datacom |
| DS-KIT-2C256* | CoolRunner-II Development Kit | Insight (Memec) | XC2C256 | Low power designs |
| DS-KIT-2C256-PAK* | CoolRunner-II Development Kit w/WebPACK CD and JTAG Cable | Insight (Memec) | XC2C256 | Low power designs |
| MXCK-100-003 | Mechatronics CoolRunner-II Prototyping Board | Mechatronics Test Equipment | XC2C64 | Embedded System, Low power designs |
| HW-AFX-COOL2-256MC | CoolRunner-II Evaluation Board | NuHorizons | XC2C256 | Low power designs |

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| Board Part Number | Board Description | Supplier | Xilinx Device Support | Application |
|---|---|---|---|---|
| **CoolRunner XPLA3** | | | | |
| ADS-XLX-X3-EVL | XPLA3 Evaluation Kit | Avnet Design Services | XCR3256XL | Low power designs |
| XCR | Digilab CoolRunner Development Board | Digilent | XCR3064XL | Low power designs |
| ET-XCR | Emulation Technology XCR Development Board | Emulation Technology, Inc. | XCR3064XL | Low power designs |
| DS-KIT-XPLA3 | CoolRunner XPLA3 Development Kit | Insight (Memec) | XCR3256XL | Low power designs |
| DS-KIT-XPLA3-PAK | CoolRunner XPLA3 Development Kit w/WebPACK CD and JTAG Cable | Insight (Memec) | XCR3256XL | Low power designs |
| MXCK-100-002 | Mechatronics CoolRunner Development Board | Mechatronics Test Equipment | XCR3064XL, XCR3128XL | Low power designs |
| HW-AFX-DIGI-XCR3064XL | Digilab XCR board | NuHorizons | XCR3064XL | Low power designs |
| **XC9500 Series** | | | | |
| PBX-84 | PBX84 Xilinx Prototyping Board | AL Williams | XC95108, XC9572 | Embedded System |
| DB-CPLD-PQ | ASICentrum XC9500 Development Kit | ASICentrum | XC9572 | Embedded System |
| XC95 | Digilab XC9500 Development Board | Digilent | XC95108 | Embedded System |
| XCR-DEV-BRD | XCR Development Board | Digilent | XC95108, XCR3064XL | Automotive, Navigation, Telematics |
| DS-KIT-95XL* | XC9572XL Development Kit | Insight (Memec) | XC9572XL-10VQ64 | Low power designs |
| DS-KIT-95XL-PAK* | XC9572XL Development Kit w/WebPACK CD and JTAG Cable | Insight (Memec) | XC9572XL-10VQ64 | General purpose Spartan-II development platform |
| DS-KIT-95XL-PAK* | XC95144XV Development Kit w/WebPACK CD and JTAG Cable | Insight (Memec) | XC95144XV-10TQ144C | Low power designs |
| DS-KIT-95XV* | XC95144XV Development Kit | Insight (Memec) | XC95144XV-10TQ144C | Low power designs |
| 84-0050 | LogicFlex | JK Microsystems, Inc | XC9572XL | DSP, Data Storage, Data Transmission & Manipulation, Embedded Microprocessor, Embedded System, IP-Based Systems, Low power designs, Serial / Deserialization, Telecom / Datacom |
| MXCK-044-001 | CPLD Junior Board | Mechatronics | XC9536, XC9572 | Everything, Datacom |
| MXCK-084-004 | CPLD Prototyping Board | Mechatronics | XC9572, XC95144 | Telecom, industrial controls, instrumentations, etc. |
| MP1000TX | Gigabit Ethernet Phy Prototyping Board | Metanetworks | XC95144XL | Data Transmission & Manipulation, Telecom / Datacom |
| SBX2 | SBX2 Systronix | Systronix | XC9572 | Embedded System |
| LogiCRAFT | LogiCRAFT Evaluation System | Xylon d.o.o. | XCV95144-VQ100, XC9572-VQ64; XC2S150-BG256 on ICU daughtercard | Automotive, Industrial, Human-Machine Interfaces |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| **Audio, Video & Image Processing** | | | | | | | |
| Burst Locked PLL (BURST_PLL) | Pinpoint Solutions, Inc. | | V-II | V-E | S3 | S-IIE | |
| Color Space Converter, RGB2YCrCb (CSC) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| Huffman Decoder (HUFFD) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| JPEG Fast Codec (JPEG_FAST_C) | CAST, Inc. | V-IIP | V-II | V-E | S3 | | |
| JPEG, 2000 Decoder (BA111JPEG2000D) | Barco-Silex | V-IIP | V-II | | S3 | | |
| JPEG, 2000 Encoder (BA112JPEG2000E) | Barco-Silex | V-IIP | V-II | | S3 | | |
| JPEG, 2000 Encoder (JPEG2K_E) | CAST, Inc. | V-IIP | V-II | V-E | | | |
| JPEG, Fast color image decoder (FASTJPEG_C DECODER) | Barco-Silex | | V-II | V-E | | | |
| JPEG, Fast Decoder (JPEG_FAST_D) | CAST, Inc. | V-IIP | V-II | V-E | | S-IIE | |
| JPEG, Fast Encoder (JPEG_FAST_E) | CAST, Inc. | V-IIP | V-II | V-E | | | |
| JPEG, Fast gray scale image decoder (FASTJPEG_BW DECODER) | Barco-Silex | | V-II | V-E | | | |
| JPEG, Motion Codec V1.0 (CS6190) | Amphion Semiconductor, Ltd. | | V-II | V-E | | | |
| JPEG, Motion Decoder (CS6150) | Amphion Semiconductor, Ltd. | | V-II | V-E | | | |
| JPEG, Motion Encoder (CS6100) | Amphion Semiconductor, Ltd. | | V-II | V-E | | | |
| Longitudinal Time Code Generator | Deltatec S.A. | V-IIP | V-II | | S3 | S-IIE | |
| Motion JPEG Decoder (JPEG Decoder) | 4i2i Communications Ltd. | V-IIP | V-II | V-E | S3 | S-IIE | |
| Motion JPEG Encoder (JPEG Encoder) | 4i2i Communications Ltd. | V-IIP | V-II | V-E | S3 | S-IIE | |
| MPEG-2 Decoder (CS6651) | Amphion Semiconductor, Ltd. | V-IIP | V-II | | | | |
| MPEG-2 HDTV I & P Encoder (DV1 HDTV) | Duma Video, Inc. | | V-II | | | | |
| MPEG-2 SDTV I & P Encoder (DV1 SDTV) | Duma Video, Inc. | | V-II | | | | |
| MPEG-4 Video Compression Decoder | 4i2i Communications Ltd. | V-IIP | V-II | | S3 | | |
| MPEG-4 Video Compression Encoder | 4i2i Communications Ltd. | V-IIP | V-II | | S3 | | |
| NTSC Color Separator (NTSC-COSEP) | Pinpoint Solutions, Inc. | | V-II | V-E | S3 | S-IIE | |
| **Communication & Networking** | | | | | | | |
| 3G FEC Package | Xilinx | | V-II | V-E | | | |
| 8b/10b Decoder | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| 8b/10b Encoder | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| ADPCM, 1024 Channel Simplex (CS4190) | Amphion Semiconductor, Ltd. | | V-II | | | | |
| ADPCM, 256 Channel Simplex (CS4130) | Amphion Semiconductor, Ltd. | | V-II | V-E | | | |
| ADPCM, 512 Channel Duplex (CS4180) | Amphion Semiconductor, Ltd. | | V-II | | | | |
| ADPCM, 768 Channel | Amphion Semiconductor, Ltd. | | V-II | | | | |
| AES Decryption Family (CS5200) | Amphion Semiconductor, Ltd. | | V-II | V-E | | | S-II |
| AES Encryption | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| AES Encryption Family (CS5200) | Amphion Semiconductor, Ltd. | | V-II | V-E | | | S-II |
| AES Standard Encryptor/Decryptor | Helion Technology Limited | V-IIP | V-II | V-E | S3 | S-IIE | |
| AES Tiny Encryptor/Decryptor | Helion Technology Limited | V-IIP | V-II | V-E | S3 | S-IIE | |
| ATM Adaptation Layer 5 (AAL5) | ModelWare, Inc. | | V-II | | S3 | | |
| ATM Adaption Layer 1 (AAL1) | ModelWare, Inc. | | V-II | V-E | | | |
| ATM Cell Processor (CC200) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| ATM Utopia Level 2 Master and Slave w/OPB Interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| AWGN - Additive White Gaussian Noise | Xilinx | V-IIP | V-II | | | | |
| Bluetooth Baseband Processor (BOOST Lite) | NewLogic Technologies AG | | V-II | | | | |
| Convolutional Encoder | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| CRC-32 for 10 Gbps OC192 systems (CORE-CRC-128) | Calyptech Design Services | | | | S3 | | |
| CRC-32 for 40 Gbps OC-768 systems (CORE-CRC-256) | Calyptech Design Services | V-IIP | V-II | | | | |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| Dataflow Processor (phyCore) | Phystream Ltd. | V-IIP | | 0 | | | 0 |
| DES and DES3 Encryption Engine (MC-XIL-DES) | Memec Design | | V-II | V-E | | S-IIE | S-II |
| DES Encryption | CAST, Inc. | | V-II | V-E | | | S-II |
| DES3 AMBA Platform | SoC Solutions, LLC | V-IIP | V-II | | S3 | S-IIE | |
| DES3 Encryption | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| DVB Satellite Modulator (MC-XIL-DVBMOD) | Memec Design | | V-II | V-E | | | S-II |
| Email Trigger | Amirix Systems, Inc. | V-IIP | | | | | |
| Ethernet 1000BASE-X PCS/PMA | Xilinx | V-IIP | | | | | |
| Ethernet MAC, 1 Gigabit (CC281) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Ethernet MAC, 1 Gigabit Half/Full duplex with GMII or 1000BASE-X PCS/PMA | Xilinx | V-IIP | V-II | V-E | | S-IIE | |
| Ethernet MAC, 10 Gigabit Full Duplex with XGMII or XAUI | Xilinx | V-IIP | V-II | | | | |
| Ethernet MAC, 10/100 | Hitachi ULSI Systems Co., Ltd. | | | | | | |
| Ethernet MAC, 10/100 | Zuken, Inc. | | V-II | V-E | | | |
| Ethernet MAC, 10/100 (CC271) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Ethernet MAC, 10/100 (MAC) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| Ethernet MAC, 10G (CC410) | Paxonet Communications, Inc. | | V-II | | | | |
| Ethernet MAC, 10G (XGEMAC) | GDA Technologies, Inc. | V-IIP | V-II | | | | |
| Ethernet MAC, 1Gigabit (MAC-1G) | CAST, Inc. | V-IIP | V-II | | | | |
| Ethernet PCS, 10G (CC411) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Ethernet PCS, 10G (MC-XIL-10GEPCS) | Memec Design | | V-II | | | | |
| Framer, 1.25 Gb/s GFP (CC224) | Paxonet Communications, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| Framer, 2.5 Gb/s GFP (CC226) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, 8-Bit Multilchannel GFP (CC225) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, 8-Bit Transparent GFP (CC124) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, E1 (CC303) | Paxonet Communications, Inc. | V-IIP | V-II | | | S-IIE | |
| Framer, OC12 (CC351) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, OC192/10 GB/s GFP (CC327) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, OTU2 (CC481) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, STS192/STM64 (CC314) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, STS48 (CC352) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Framer, T1 (CC302) | Paxonet Communications, Inc. | V-IIP | V-II | | | S-IIE | |
| Framer/Digital Wrapper, STS48 OTN (CC381) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| G.709 Compliant FEC Core (CC345) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| HDLC, Single-Channel (MC-XIL-HDLC) | Memec Design | V-IIP | V-II | | S3 | | |
| HyperTransport Cave 16-Bit | GDA Technologies, Inc. | V-IIP | V-II | | | | |
| Interleaver/De-interleaver | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Inverse Multiplexer for ATM (IMA) | ModelWare, Inc. | | V-II | V-E | | | |
| Mapper, E1 (CC333) | Paxonet Communications, Inc. | V-IIP | V-II | | | S-IIE | |
| MD5 Message Digest Algorithm | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| Modular Exponentiation Accelerator (MODEXP1) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| Multi Rate Performance Monitor | Calyptech Design Services | V-IIP | V-II | | S3 | | |
| Network Processor Forum Streaming Interface (NPSI) | ModelWare, Inc. | | | | | | |
| Packet Processor (CC318) | Paxonet Communications, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| Path Processor, OC12c (CC321) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Path Processor, STS192/STM64 (CC324) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| Path Processor, STS-48/STM-16 (CC322) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| Reed Solomon Decoder | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Reed Solomon Decoder (MC-XIL-RSDEC) | Memec Design | | V-II | | | S-IIE | S-II |
| Reed Solomon Encoder | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Reed Solomon Encoder (MC-XIL-RSENC) | Memec Design | | V-II | | | S-IIE | S-II |
| SDLC Controller (SDLC) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| SHA-1 Encryption Processor | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| SONET Performance Monitor (HCLT_SONETPM) | HCL Technologies, Ltd. | | V-II | | | | |
| SPI 4.2 Interface (CC401) | Paxonet Communications, Inc. | V-IIP | V-II | | | | |
| SPI-3 (POS-PHY L3) Link Layer Interface, 1-Ch | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| SPI-3 (POS-PHY L3) Link Layer Interface, 2-Ch | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| SPI-3 (POS-PHY L3) Link Layer Interface, 4-Ch | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| SPI-3 (POS-PHY L3) Link Layer Interface, Multi-Channel | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| SPI-3 (POS-PHY L3) Physical Layer Interface | Xilinx | | | V-E | | | |
| SPI-4.1 (Flexbus 4) Interface Core, 1-Channel | Xilinx | | V-II | | | | |
| SPI-4.1 (Flexbus 4) Interface Core, 4-Channel | Xilinx | | V-II | | | | |
| SPI-4.2 (POS-PHY L4) Multi-Channel Interface | Xilinx | V-IIP | V-II | | | | |
| SPI-4.2 (POS-PHY L4) to SPI-4.1 (Flexbus 4) Bridge | Xilinx | | V-II | | | | |
| SPI-4.2 (POS-PHY L4) to XGMII (10GE MAC) Bridge | Xilinx | | V-II | | | | |
| SPI-4.2 Lite (POS_PHY L4) | Xilinx | | V-II | | S-3 | | |
| System Packet Interface Level 4 Phase 2 (HCLT_SPI4-2) | HCL Technologies, Ltd. | V-IIP | V-II | | | | |
| TDM Timeswitch | Calyptech Design Services | V-IIP | V-II | | S3 | S-IIE | |
| Turbo Decoder, 3GPP | SysOnChip, Inc. | | V-II | V-E | | | |
| Turbo Decoder, 3GPP (S3000) | iCoding Technology, Inc. | | V-II | V-E | | S-IIE | |
| Turbo Decoder, Convolutional, 3GPP Compliant | Xilinx | | V-II | V-E | | | |
| Turbo Decoder, Convolutional, 3GPP2/CDMA2000 | Xilinx | V-IIP | V-II | | S-3 | | |
| Turbo Decoder, DVB-RCS (S2000) | iCoding Technology, Inc. | | V-II | V-E | | | |
| Turbo Decoder, DVB-RCS (TC1000) | TurboConcept | | V-II | V-E | | | |
| Turbo Decoder, Product Code | Xilinx | V-IIP | V-II | | S-3 | | |
| Turbo Encoder, Convolutional, 3GPP Compliant | Xilinx | | V-II | V-E | | | |
| Turbo Encoder, Convolutional, 3GPP2/CDMA2000 | Xilinx | V-IIP | V-II | | S-3 | | |
| Turbo Encoder, DVB-RCS (S2001) | iCoding Technology, Inc. | | V-II | V-E | | | |
| Turbo Encoder, Product Code | Xilinx | V-IIP | V-II | | S-3 | | |
| Turbo Product Code Decoder, 160 Mbps (TC3404) | TurboConcept | | V-II | V-E | | | |
| Turbo Product Code Decoder, 25 Mbps (TC3000) | TurboConcept | | V-II | V-E | | | |
| Turbo Product Code Decoder, 30 Mbps (TC3401) | TurboConcept | | | V-E | | S-IIE | |
| Viterbi Decoder, General Purpose | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Viterbi Decoder, IEEE 802-compatible | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| XAPP 289: Common Switch Interface CSIX-L1 Reference Design | Xilinx | V-IIP | V-II | | | | |
| XAUI | Xilinx | V-IIP | | | | | |
| **Digital Signal Processing** | | | | | | | |
| Bit Correlator | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| Cascaded Integrator Comb (CIC) Filter | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| CORDIC | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Digital Down Converter (DDC) | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| Digital Down Converter, High-Speed Wideband (4954-422) | Pentek, Inc. | V-IIP | V-II | | | | |

**Visit the Xilinx IP Center for more details at *www.xilinx.com/ipcenter***

| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| Digital Down Converter, Wideband (4954-421) | Pentek, Inc. | V-IIP | V-II | | | | |
| Digital Up Converter (DUC) | Xilinx | V-IIP | V-II | | S-3 | | |
| Direct Digital Synthesizer (DDS) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Discrete Cosine Transform (eDCT) | eInfochips Pvt. Ltd. | | V-II | V-E | | S-IIE | S-II |
| Discrete Cosine Transform, 2D Inverse (IDCT) | CAST, Inc. | | V-II | V-E | | | S-II |
| Discrete Cosine Transform, Combined 2D Forward/Inverse (DCT_FI) | CAST, Inc. | | V-II | V-E | | | S-II |
| Discrete Cosine Transform, Forward 2D (DCT) | CAST, Inc. | | V-II | V-E | | | S-II |
| Discrete Cosine Transform, forward/inverse 2D (DCT/IDCT 2D) | Barco-Silex | | V-II | V-E | | | S-II |
| Discrete Wavelet Transform (BA113FDWT) | Barco-Silex | V-IIP | V-II | | S3 | S-IIE | |
| Discrete Wavelet Transform, Combined 2D Forward/Inverse (RC_2DDWT) | CAST, Inc. | | V-II | V-E | | | S-II |
| Discrete Wavelet Transform, Inverse (BA114IDWT) | Barco-Silex | V-IIP | V-II | | S3 | S-IIE | |
| Discrete Wavelet Transform, Line-based programmable forward (LB_2DFDWT) | CAST, Inc. | | V-II | V-E | | | S-II |
| DOCSIS ITU-T J.83 Modulator | Xilinx | V-IIP | V-II | | S-3 | | |
| Fast Fourier Transform | Xilinx | V-IIP | V-II | | S-3 | | |
| FFT/IFFT for Virtex-II, 1024-Point Complex | Xilinx | | V-II | | | | |
| FFT/IFFT for Virtex-II, 16-Point Complex | Xilinx | | V-II | | | | |
| FFT/IFFT for Virtex-II, 256-Point Complex | Xilinx | | V-II | | | | |
| FFT/IFFT for Virtex-II, 64-Point Complex | Xilinx | | V-II | | | | |
| FFT/IFFT, 1024-Point Complex | Xilinx | | | V-E | | | |
| FFT/IFFT, 16-Point Complex | Xilinx | | V-II | V-E | | | |
| FFT/IFFT, 256-Point Complex | Xilinx | | V-II | V-E | | | |
| FFT/IFFT, 32-Point Complex | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| FFT/IFFT, 64-, 256-, 1024-Point Complex | Xilinx | V-IIP | V-II | | S-3 | | |
| FFT/IFFT, 64-Point Complex | Xilinx | | | V-E | | | |
| FIR Filter using DPRAM | eInfochips Pvt. Ltd. | | V-II | V-E | | S-IIE | S-II |
| FIR Filter, Distributed Arithmetic (DA) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| FIR Filter, MAC | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| FIR Filter, Parallel Distributed Arithmetic | eInfochips Pvt. Ltd. | | V-II | V-E | | S-IIE | S-II |
| LFSR, Linear Feedback Shift Register | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Radar Pulse Compression (4954-440) | Pentek, Inc. | V-IIP | V-II | | | | |
| TMS32025 DSP Processor (C32025) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| TMS32025TX Digital Signal Processor (C32025TX) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| **Math Function** | | | | | | | |
| Accumulator | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Adder Subtracter | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Divider, Pipelined | Xilinx | | V-II | V-E | | S-IIE | S-II |
| Floating Point Adder (DFPADD) | Digital Core Design | | V-II | | | | S-II |
| Floating Point Comparator (DFPCOMP) | Digital Core Design | | V-II | | | | S-II |
| Floating Point Divider (DFPDIV) | Digital Core Design | | V-II | | | | S-II |
| Floating Point Multiplier (DFPMUL) | Digital Core Design | | V-II | V-E | | | S-II |
| Floating Point Square Root Operator (DFPSQRT) | Digital Core Design | | V-II | V-E | | | S-II |
| Floating Point to Integer Converter (DFP2INT) | Digital Core Design | | V-II | | | | S-II |
| Integer to Floating Point Converter (DINT2FP) | Digital Core Design | | V-II | | | | S-II |
| Multiply Accumulator (MAC) | Xilinx | V-IIP | V-II | | S-3 | S-IIE | S-II |
| Multiply Generator | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Sine Cosine Look Up Table | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| Twos Complementer | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| **Memories & Storage Element** | | | | | | | |
| Block Memory, Dual-Port | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Block Memory, Single-Port | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Content Addressable Memory (CAM) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Distributed Memory | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| FIFO, Asynchronous | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| FIFO, Synchronous | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| RLDRAM Memory Controller | Avnet Design Services | | V-II | | | | |
| SDRAM Controller, DDR (EP525) | Eureka Technology | V-IIP | V-II | | S3 | S-IIE | |
| SDRAM Controller, DDR (MC-XIL-SDRAMDDR) | Memec Design | | V-II | V-E | | | S-II |
| SDRAM Controller, DDR (NW) | Northwest Logic | V-IIP | V-II | | S3 | S-IIE | |
| SDRAM Controller, SDR (NW) | Northwest Logic | V-IIP | V-II | | S3 | S-IIE | |
| **Microprocessor, Controller & Peripheral** | | | | | | | |
| 1 Gigabit Ethernet MAC w/PLB interface | Xilinx | V-IIP | | | | | |
| 10/100 Ethernet MAC Lite w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| 10/100 Ethernet MAC w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| 10/100 Ethernet MAC w/PLB interface | Xilinx | V-IIP | | | | | |
| 16450 UART (H16450) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| 16450 UART w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| 16450 UART w/PLB interface | Xilinx | V-IIP | | | | | |
| 16450 UART w/Synchronous Interface (H16450S) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| 16550 UART w/FIFOs & synch interface (H16550S) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| 16550 UART w/FIFOs (H16550) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| 16550 UART w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| 16550 UART w/PLB interface | Xilinx | V-IIP | | | | | |
| 2910A Microprogram Controller (C2910A) | CAST, Inc. | V-IIP | V-II | | S3 | | |
| 2D Multiprocessing Interface Fabric (2D-fabric402C) | Crossbow Technologies, Inc. | V-IIP | V-II | | | S-IIE | S-II |
| 68000 Compatible Microprocessor (C68000) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| 80186 Compatible Microprocessor (e80186) | eInfochips Pvt. Ltd. | | V-II | | | | |
| 8051 Base Compatible Microcontroller (DR8051BASE) | Digital Core Design | | V-II | | | | S-II |
| 8051 Compatible Microcontroller (C8051) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | S-II |
| 8051 Compatible Microcontroller (FLIP8051 Thunder) | Dolphin Integration | V-IIP | V-II | | | S-IIE | |
| 8051 High-speed 8-bit RISC Microcontroller (R80515) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| 8051 Microcontroller, PicoBlaze Emulated (PB8051-MX/TF) | Roman-Jones, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| 8051 RISC Microcontroller (DR8051) | Digital Core Design | | V-II | | | | S-II |
| 8052 Compatible Microcontroller (DR8052EX) | Digital Core Design | | V-II | | | | S-II |
| 80530 8-bit Microcontroller (D80530) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| 80C51 Compatible RISC Microcontroller (R8051) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| 8237 Programmable DMA Controller (C8237) | CAST, Inc. | | V-II | V-E | | | S-II |
| 8250 UART (H8250) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| 8254 Programmable Interval Timer/Counter (C8254) | CAST, Inc. | | V-II | V-E | | | S-II |
| 8254 Programmable Interval Timer/Counter (e8254) | eInfochips Pvt. Ltd. | | V-II | | | | S-II |
| 8255 Programmable I/O Controller (e8255) | eInfochips Pvt. Ltd. | | V-II | | | | S-II |
| 8259A Programmable Interrupt Controller (C8259A) | CAST, Inc. | | V-II | V-E | | | S-II |
| Arbiter and Bus Structure w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| Arbiter and Bus Structure w/PLB interface | Xilinx | V-IIP | | | | | |
| ATM Utopia Level 2 Master and Slave w/OPB Interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| ATM Utopia Level 2 Master and Slave w/PLB Interface | Xilinx | V-IIP | | | | | |
| BRAM Controller w/LMB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| BRAM Controller w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| BRAM Controller w/PLB interface | Xilinx | V-IIP | | | | | |
| BSP Generator (SW only) | Xilinx | V-IIP | | | | | |
| Compact Video Controller (logiCVC) | Xylon d.o.o. | | V-II | | | | S-II |
| CRT Controller (C6845) | CAST, Inc. | | V-II | V-E | | S-IIE | S-II |
| DCR Bus Structure | Xilinx | V-IIP | | | | | |
| Direct Memory Access Controller (CZ80DMA) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| External Memory Controller (EMC) w/OPB interface (Includes support for Flash, SRAM, ZBT, System ACE) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| External Memory Controller (EMC) w/PLB interface (Includes support for Flash, SRAM, ZBT, System ACE) | Xilinx | V-IIP | | | | | |
| FPU for Microblaze (Quixilica) | QinetiQ Limited | V-IIP | V-II | | | | |
| GPIO w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| HDLC Controller (Multi (256) Channel) w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| HDLC Controller (Single Channel) w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| IIC w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Internet Appliance (socPiP-1A_Platform) | SoC Solutions, LLC | | V-II | V-E | | | |
| Interrupt Controller (IntC) w/DCR interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| Interrupt Controller (IntC) w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| IPIF Address Decode w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| IPIF DMA w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| IPIF Interrupt Controller w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| IPIF Master/Slave Attachment w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| IPIF Read/Write Packet FIFO w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| IPIF Scatter/Gather w/OPB interface | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| IPIF Slave Attachment w/PLB interface | Xilinx | V-IIP | | | | | |
| Java Processor, 32-bit (Lightfoot) | Digital Communications Technologies, Ltd. | | V-II | | | | S-II |
| Java Processor, Configurable (LavaCORE) | Derivation Systems, Inc. | | V-II | | | | |
| JTAG UART w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Memory Test Utility (SW only) | Xilinx | V-IIP | | | | | |
| MicroBlaze Soft RISC Processor | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| MicroBlaze Source Code | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| MIPS system controller (ES500) | Eureka Technology | | V-II | V-E | | | |
| ML300 VxWorks BSP (SW only) | Xilinx | V-IIP | | | | | |
| Motor Controller - 3 phase (MLCA_4) | MEET Ltd. | | | | | S-IIE | S-II |
| OPB2DCR Bridge | Xilinx | V-IIP | | | | | |
| OPB2OPB Bridge (Lite) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| OPB2PCI Full Bridge (32/33) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| OPB2PLB Bridge | Xilinx | V-IIP | | | | | |
| Operating System Accelerator (Sierra S16) | RealFast Intellectual Property AB | | V-II | | | S-IIE | S-II |
| PIC125x Fast RISC Microcontroller (DFPIC125X) | Digital Core Design | | V-II | | | | S-II |
| PIC1655x Fast RISC Microcontroller (DFPIC1655X) | Digital Core Design | | V-II | | | | S-II |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| PIC165X Compatible Microcontroller (C165X) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| PIC165x Fast RISC Microcontroller (DFPIC165X) | Digital Core Design | | V-II | V-E | | | S-II |
| PIC16C55X Compatible RISC Microcontroller (C1655x) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| PicoBlaze UG129: PicoBlaze 8-bit Microcontroller for Spartan-3, Virtex-II, and Virtex-II Pro Devices) - REFERENCE DESIGN | Xilinx | V-IIP | V-II | | S-3 | | |
| PicoBlaze (XAPP 213: PicoBlaze 8-bit Microcontroller for Virtex-E and Spartan-II/E Devices) - REFERENCE DESIGN | Xilinx | | | V-E | | S-IIE | S-II |
| PicoBlaze (XAPP 627: PicoBlaze 8-bit Microcontroller for Virtex-II and Virtex-II Pro Devices) - REFERENCE DESIGN | Xilinx | V-IIP | V-II | | | | |
| PLB2OPB Bridge | Xilinx | V-IIP | | | | | |
| PowerPC Bus Master (EP201) | Eureka Technology | V-IIP | V-II | | S3 | S-IIE | |
| PowerPC Bus Slave (EP100) | Eureka Technology | V-IIP | V-II | | S3 | S-IIE | |
| RISC Processor, 16-bit Proprietary (AX1610) | Loarant Corporation | V-IIP | V-II | | S3 | S-IIE | |
| SDRAM Controller w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| SDRAM Controller w/PLB interface | Xilinx | V-IIP | | | | | |
| SPI Master and Slave w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| SwifTraxTM Rapid Development System | SoC Solutions, LLC | V-IIP | V-II | | S3 | S-IIE | |
| Systems Reset Module | Xilinx | V-IIP | | | | | |
| Timebase/Watch Dog Timer (WDT) w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| Timer/Counter w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| UART Lite w/OPB interface | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| UART, Generic Compact (MC-XIL-UART) | Memec Design | V-IIP | V-II | | S3 | | |
| UltraController Solution: A lightweight PowerPC Microcontroller (XAPP672) - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| VxWorks Board Support Package (BSP) | Xilinx | V-IIP | | | | | |
| XTENSA-V Configurable 32-bit Microprocessor | Tensilica, Inc. | | V-II | | | | |
| Z80 Compatible Microprocessor (CZ80CPU) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| Z80 Compatible Programmable Counter/Timer (CZ80CTC) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| Z80 Intelligent Peripheral Controller (CZ80PSC) | CAST, Inc. | | | | | | |
| Z80 Peripheral I/O Controller (CZ80PIO) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| Z80 Serial I/O Controller (CZ80SIO) | CAST, Inc. | V-IIP | V-II | V-E | | S-IIE | |
| **Standard Bus Interface** | | | | | | | |
| Advanced Switching Endpoint Core | Xilinx | V-IIP | | | | | |
| CAN 2.0 B Compatible Network Controller (LogiCAN) | Xylon d.o.o. | V-IIP | V-II | | S3 | S-IIE | |
| CAN 2.0B Bus Controller (iCAN) | Intelliga Integrated Design, Ltd. | V-IIP | V-II | V-E | S3 | S-IIE | |
| CAN Bus Controller (MC-XIL-OPB-XCAN) | Memec Design | V-IIP | V-II | V-E | S3 | S-IIE | S-II |
| CAN Bus Controller 2.0B | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| CAN Bus Controller with 32 Mail Boxes | Robert Bosch GmbH | V-IIP | V-II | | S3 | S-IIE | |
| HyperTransport Cave, 8-bit | GDA Technologies, Inc. | V-IIP | V-II | | | | |
| HyperTransport Single-Ended Slave Core | Xilinx | V-IIP | V-II | | | | |
| I2C Bus Controller (I2C) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| I2C Bus Controller Master (DI2CM) | Digital Core Design | | V-II | V-E | | | S-II |
| I2C Bus Controller Slave (DI2CS) | Digital Core Design | | V-II | V-E | | | S-II |
| I2C Bus Controller Slave Base (DI2CSB) | Digital Core Design | | V-II | V-E | | | S-II |
| I2C Two-Wire Serial Interface Master-Only (MC-XIL-TWSIMO) | Memec Design | | V-II | V-E | | S-IIE | S-II |
| I2C Two-Wire Serial Interface Master-Slave (MC-XIL-TWSIMS) | Memec Design | | V-II | V-E | | S-IIE | S-II |
| LIN - Local Interconnect Network Bus Controller (iLIN) | Intelliga Integrated Design, Ltd. | V-IIP | V-II | V-E | S3 | S-IIE | |

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| Function | Vendor Name | Virtex-II Pro | Virtex-II | Virtex-E | Spartan-3 | Spartan-IIE | Spartan-II |
|---|---|---|---|---|---|---|---|
| LIN Controller | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| PCI 32-bit Master Interface (PCI-M32) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| PCI 32-Bit Multifunction Target Interface (PCI-TMF) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| PCI 32-bit Target Interface (PCI-T32) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| PCI 64-bit/66-MHz master/target interface (EC240) | Eureka Technology | | V-II | V-E | | | |
| PCI Express Endpoint Core | Xilinx | V-IIP | | | | | |
| PCI Host Bridge (EP430) | Eureka Technology | | V-II | V-E | | | |
| PCI Host Bridge (PCI-HB) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| PCI, 64-bit Master Interface (PCI-M64) | CAST, Inc. | V-IIP | V-II | | | S-IIE | |
| PCI, 64-bit Target Interface (PCI-T64) | CAST, Inc. | V-IIP | V-II | | | S-IIE | |
| PCI32 Interface Design Kit (DO-DI-PCI32-DKT) | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| PCI32 Interface, IP Only (DO-DI-PCI32-IP) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| PCI32 Single-Use License for Spartan (DO-DI-PCI32-SP) | Xilinx | | | | S-3 | S-IIE | S-II |
| PCI64 & PCI32, IP Only (DO-DI-PCI-AL) | Xilinx | V-IIP | V-II | V-E | S-3 | S-IIE | S-II |
| PCI64 Interface Design Kit (DO-DI-PCI64-DKT) | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| PCI64 Interface, IP Only (DO-DI-PCI64-IP) | Xilinx | V-IIP | V-II | V-E | | S-IIE | S-II |
| PCI-PCI Bridge (EP440) | Eureka Technology | V-IIP | V-II | | S3 | S-IIE | |
| PCI-X 64/133 Interface for Virtex-II (DO-DI-PCIX64-VE). Includes PCI 64 bit interface at 33 MHz | Xilinx | V-IIP | V-II | | | | |
| PCI-X 64/66 Interface for Virtex-E (DO-DI-PCIX64-VE). Includes PCI 64 bit interface at 33 MHz | Xilinx | | | VE | | | |
| PCI-X Arbiter | SoC Solutions, LLC | V-IIP | V-II | V-E | | S-IIE | |
| PCI-X Interface (NWL PCI-X) | Northwest Logic | V-IIP | V-II | 0 | 0 | 0 | 0 |
| RapidIO 8-bit port LP-LVDS Phy Layer (DO-DI-RIO8-PHY) | Xilinx | V-IIP | V-II | | | | |
| RapidIO Logical (I/O) and Transport Layer (DO-DI-RIO8-LOG) | Xilinx | V-IIP | V-II | | | | |
| RapidIO Phy Layer to PLB Bridge reference design - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| Serial Protocol Interface Slave (SPI Slave) | CAST, Inc. | | V-II | V-E | | S-IIE | |
| Two-Wire Serial Interface - I2C (MC-XIL-TWSI) | Memec Design | V-IIP | V-II | V-E | S3 | S-IIE | S-II |
| USB 1.1 Function Controller (CUSB) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| USB 2.0 Function Controller (CUSB2) | CAST, Inc. | V-IIP | V-II | V-E | S3 | S-IIE | |
| USB Function Controller with On-Chip Peripheral Bus (CUSB_OPB) | CAST, Inc. | V-IIP | V-II | | S3 | S-IIE | |
| XAPP653: Virtex-II Pro/Spartan-3 3.3V PCI Reference Design - REFERENCE DESIGN | Xilinx | V-IIP | | | S-3 | | |
| **Backplanes and Gigabit Serial I/O** | | | | | | | |
| Aurora 201, 401and 804 Designs - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| WP160: Emulating External SERDES Devices with Embedded RocketIO Transceivers - WHITE PAPER | Xilinx | V-IIP | | | | | |
| XAPP 649: SONET Rate Conversion in Virtex-II Pro Devices - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| XAPP 651: SONET and OTN Scramblers/Descramblers - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| XAPP 652: Word Alignment and SONET/SDH Framing - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| XAPP660: Partial Reconfiguration of RocketIO Attributes using PPC405 core (DCR Bus) - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| XAPP661: RocketIO Transceiver Bit-Error Rate Tester (BERT) - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |
| XAPP662: Partial Reconfig. of RocketIO Attributes using PPC405 core (PLB or OPB bus) + RocketIO Transceiver Bit-Error Rate Tester (BERT) - REFERENCE DESIGN | Xilinx | V-IIP | | | | | |

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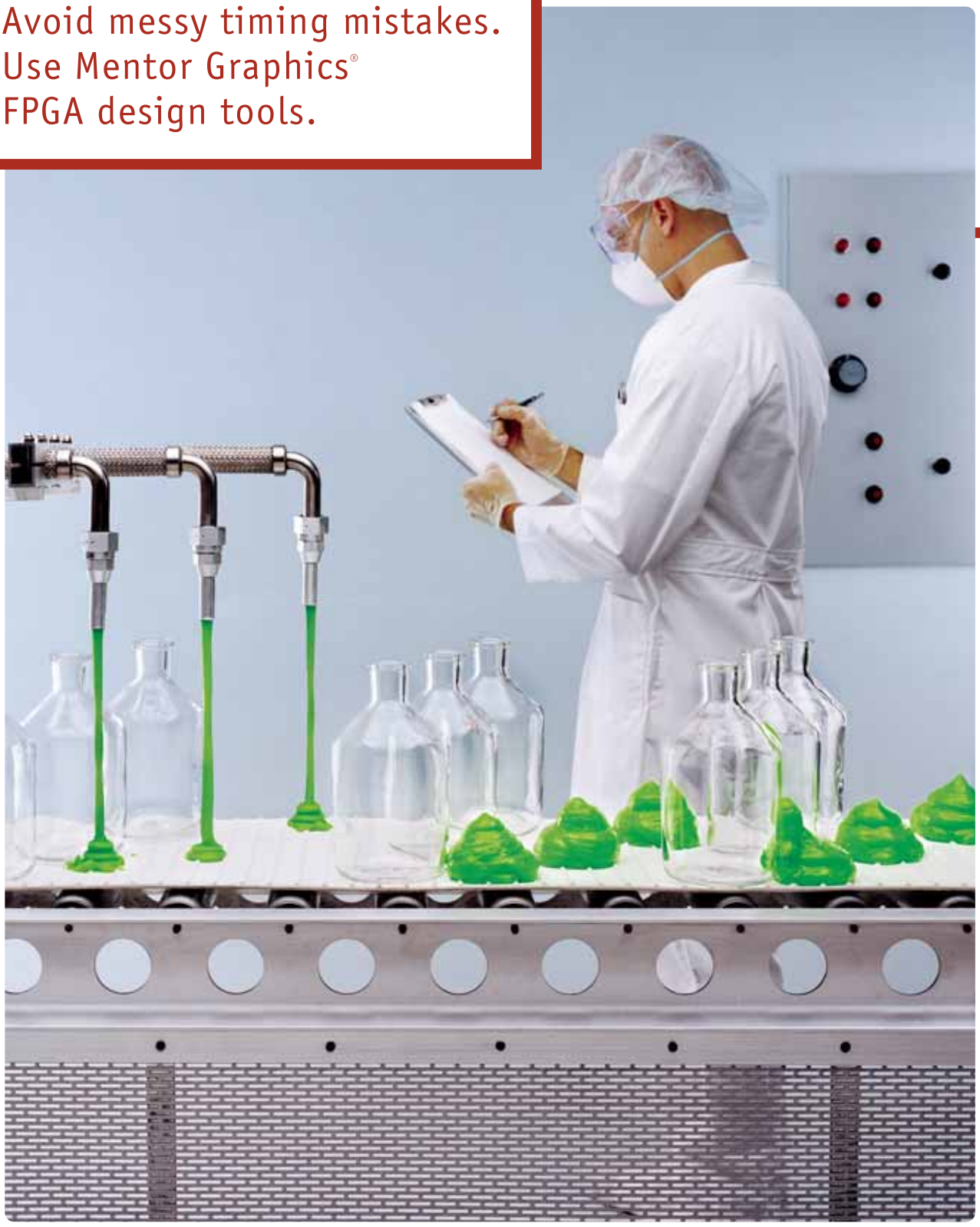

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