XCELL

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XILINX®

The Programmable Logic Company℠

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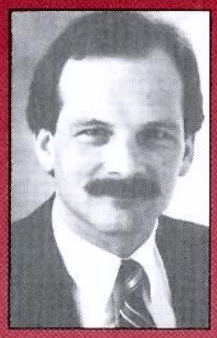
GENERAL FEATURES



Meet New Xilinx COO & President Curt Wozniak

Most recently from Sun Microsystems, new President and Chief Operating Officer Curt Wozniak brings a customer's perspective to the day-to-day running of Xilinx...

See Page 3

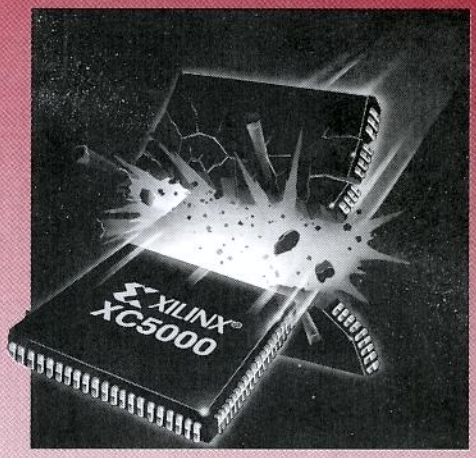
PRODUCT INFORMATION

New Product:

The XC5000 FPGA Family

Xilinx introduces the most cost-effective, high-density FPGA ever...

See Page 14



DESIGN TIPS & HINTS

MEMBER PCI LOCAL BUS SPECIAL INTEREST GROUP

A PCI Primer

What is it about the new PCI bus standard that has generated so much interest? ***Find out on page 25***

XACT-Performance Update

Three stories discuss the latest developments in the XACT-Performance™ development software:

- Using XACT-Performance, *see page 29*
- XACT-Performance Trade-Offs, *see page 30*
- Setting Requirements in a Constraints File, *see page 32*

Examining The Process

By BRADLY FAWCETT ◆ Editor

Since their introduction in the mid-1980s, most FPGAs and EPLDs have been fabricated using industry-standard, two-layer-metal CMOS process technologies. The use of standard processes has allowed programmable logic vendors to benefit from the industry's latest process improvements while ensuring an adequate supply of products at a reasonable cost. Process improvements have played a major role in creating greater FPGA density and performance and lower component costs.

The most obvious example of process technology improvement has been the continued migration to smaller and smaller device geometries. Where the first FPGA, the XC2064, was originally fabricated with 2.0 µ technology, FPGA vendors today are aggressively adopting 0.6 and 0.5 µ processes for high-volume manufacturing. However, the basic underlying technology has remained the same - two metal layers for interconnect and CMOS transistors for logic, with a nominal 5 volts for V_{CC}.

> *"These advances in process technology will lead to better programmable logic devices in several different ways."*

More fundamental changes will soon overtake us. To continue the semiconductor scaling trend and meet the demand for higher integration and reduced power consumption, the semiconductor industry has started the transition to a 3.3 volt standard. New processing techniques now allow for additional metal layers. More esoteric improvements, such as better intermetal dielectrics, are leading to improved circuit performance as well as lower die costs.

These advances in process technology will lead to better programmable logic devices in several different ways. First, these process improvements will be applied to current EPLD and FPGA architectures, resulting in faster, denser, and lower-cost versions of current product families. For example, consider the effect of three-layer-metal technology on current FPGA devices. With traditional two-layer-metal processes, an FPGA's interconnect channels must be placed "between" logic cells on the die. The first layer of metal is used for the fixed routing within the logic and programming cells. The second layer typically is used for the programmable interconnect between logic cells. However, the programming elements for the routing switches are formed in the silicon (just like the transistors that make up the logic), and, where programmable routing channels have to cross, the first layer of metal must be used also. Thus, much of the interconnect must be placed between the logic cells. With three layers of metal, the second and third layers can be used to implement the programmable interconnect channels without interfering with the first layer of metal, allowing more of the interconnect to reside "above" the logic. Thus, the same number of "usable gates" can be placed on a smaller die with resultant lower costs. We are in the process of generating new layouts and masks for our SRAM-

Continued on page 7

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Xilinx Welcomes New President and Chief Operating Officer Curt Wozniak

Curt Wozniak joined Xilinx in early August as our new President and Chief Operating Officer. Bernie Vonderschmitt remains Chief Executive Officer and Chairman of the Board of Directors.

Curt joins Xilinx after a 10-year tenure at Sun Microsystems, starting as Director of Manufacturing in early 1984. He later became Vice President and General Manager of the Education Products Division, and then Vice President of the Desktop and Graphics Development Division. In 1991, Curt was promoted to Vice President of Engineering of Sun Microsystems Computer Corporation (SMCC), Sun's largest subsidiary, where he had responsibility for engineering operations in Silicon Valley, Boston, Research Triangle and Tokyo. He became Vice President of Worldwide Marketing for SMCC in 1993.

Prior to Sun, Curt was a production engineering manager at Hewlett Packard (1982-1984) and held several positions with General Motors (1973-1982). He earned an M.B.A. degree from Stanford University in 1980 and holds a B.S.M.E. from the General Motors Institute of Technology.

Curt's thoughts about his new position:

I am very excited to have joined Xilinx. Through its first 10 years, Xilinx has established itself as the leader of the programmable logic market. I am impressed with its leadership products, great customer base and outstanding workforce.

> *"All of the basic technology factors point to the growing use of programmable logic."*

While Xilinx has become a substantial company, there is still incredible growth ahead. All of the basic technology factors point to the growing use of programmable logic as a major part of system design. The basic technology trends of semiconductors, the growing power of PCs and workstations to handle complex design tasks, and the incredible value of user-programmability all point in this direction. In addition, from my own experience running a large engineering group, system designers are continually under pressure for faster development, the ability to respond to changes, and lower budgets. Those are the **real** problems that Xilinx solves.

Engineers in growing numbers are understanding the value that high-density programmable logic offers and incorporating it in their systems. As the density of programmable logic devices continues to increase, designs are getting larger and more complex. As a result, system designers face the challenge of learning new tools and methodologies to effectively deal with increasing design complexity and shrinking development cycles. High-level design languages, logic synthesis, behavioral modeling and system-level simulation are among the tools and techniques that will become commonplace over the next few years.

In a previous issue of *XCELL*, Bernie Vonderschmitt predicted FPGAs with

Continued on page 4

XILINX®

GUEST EDITORIAL

Continued from page 3

more than 150,000 gates and 250 MHz system clock rates by the year 2000. We will be challenged to deliver all that power to the design community. We need to continually drive the ability of the tools to take advantage of all the capabilities of the silicon. Our tools must become easier to use, more powerful and interface to the other CAE tools that our users employ to complete their system designs.

In my short time at Xilinx, I have been extremely impressed by the employees, the loyalty of our customer base, and the new product portfolio we are developing. The technologies that we will be bringing to the market over the next few years will be truly exciting. Higher density, faster speed, additional architectural choices, and, of course, lower costs are all coming. Xilinx will aggressively push our product line on all of these fronts. To make this happen, we are investing in R&D at a 13 percent annual rate.

The growth that we are facing would challenge any company. This is where I hope to bring the experience I gained at Sun to bear. During my 10 years, Sun grew from 272 people and $15 million in revenue to 13,000 people and $4.8 billion in revenue. During that time, I was fortunate to be involved in some of the crucial decisions that every growing company faces. I managed manufacturing, engineering and marketing. I was a Xilinx customer. I've experienced the challenges our users face in getting their products to the market.

This brings me to my philosophy for success and growth. There are three ingredients that I think are key. First, treat your customers and partners like gold. Second, hire great people and give them the power and responsibility to succeed. Make sure they are having fun. Third, keep tight control of the business fundamentals. Revenue, costs, assets, and, of course, profits must be managed tightly. It all sounds pretty simple, but doing all three as well as Xilinx has done for the past 10 years is unusual. I hope to continue that tradition as we move into our second decade.

I am very interested in hearing from our customers. Please let me know your comments and ideas. I can't promise to answer each one, but I do promise to read every one. You can e-mail me at curt.wozniak@xilinx.com, or write me at 2100 Logic Drive, San Jose, CA 95124 or FAX me at 408-559-7114. ◆

FINANCIAL REPORT

Record Quarterly Revenues Once Again

Xilinx sales revenues for the second fiscal quarter (ending Sept. 30, 1994) rose to a record $79.5 million, an increase of 5.8 percent from the previous quarter and 32 percent from the same quarter one year ago. In all but two of the quarters since the first product shipments in late 1985, Xilinx revenues have increased compared to the previous quarter.

Domestic sales were particularly strong this past quarter, and European sales also rose. International sales accounted for 30 percent of total revenues for the quarter.

After a 20 percent increase from the previous quarter, XC4000 family revenues surpassed those of the XC3000 family for the first time. Revenues from the high-speed XC3100 family also rose sharply, with 19 percent growth from last quarter. ◆

EPLD Technology Crucial for Meeting Board Space Constraints

Soon, airline passengers may have their own personal telephone and video services available on a "per seat" basis, thanks to technology being developed by Summa Four Inc. (Manchester, NH), with an assist from Xilinx EPLDs.

The challenge for designers at Summa Four was to condense existing technology into a form suitable for use in commercial airliners. Of course, minimizing size, power consumption and cost were all major considerations.

The design supports multiple E1 digital trunk interfaces using multiple microprocessors and their memory subsystems. Both audio and video data transported on the trunks is encoded in an 8-bit format; for example, voice information is encoded using Pulse Code Modulation (PCM).

Early in the project, Summa Four recognized that high-density programmable logic would be required to consolidate the "glue logic" in the design in order to meet stringent board space and power constraints. The XC7272A EPLD was chosen, largely due to the availability of easy PAL-to-EPLD conversion software. Summa Four design engineer Brian Vaillancourt noted that excellent technical and sales support were key to selecting Xilinx as a component supplier.

One XC7272A EPLD device consolidated logic previously implemented in three 39V18 GALs, one 16V8 GAL, and some SSI glue logic. The EPLD is used for two main functions, intersystems communication control and PCM control.

EPLD Functions

The first task involves control of a proprietary asynchronous message protocol. Incoming signals are registered for use by a communications protocol state machine; the availability of input registers separate from the macrocell registers facilitates this task. In some cases, incoming signals were double-registered to avoid potential metastability problems and to counteract bus noise.

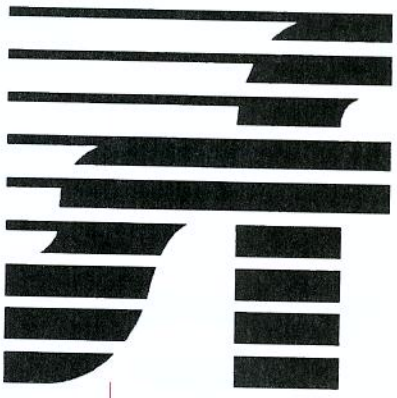
PCM control is implemented with counters and state machines. This circuitry involves shared busses, and makes extensive use of the EPLD's output enable capabilities. The flexibility of controlling output enables from macrocell outputs or UIM® (Universal Interconnect Matrix) generated states was crucial for this implementation. The EPLD also holds the logic for providing frame synchronization information to the framer circuit.

Design Process

The design was developed using Xilinx XEPLD and Prolink software on a 80486-based PC. The design was entered entirely in Boolean equations, including the conversion of existing PAL design files.

The 100% routability of the UIM proved instrumental in meeting tight development schedules. This capability allowed for significant design changes after the printed circuit board was completed. These changes included generating new function block inputs required for a state machine, and new UIM-generated clocks for use in specific "node" equations.

As Mr. Vaillancourt notes, "The PCB was extremely dense. I generated spreadsheets to monitor tenths of square inches of space on the board. We had to make it fit. Xilinx EPLDs gave us the integration we needed, without which the design would not have been possible." Since the successful completion of this design, Xilinx EPLDs have been chosen for other projects at Summa Four. ◆



Summa Four

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	PART NUMBER
Corporate		
Product description & selection guide	Overview of entire Xilinx product line & services	#0010130-04
PCI-compliance packet	Technical information to assist designers in understanding the PCI bus and the use of Xilinx devices in PCI applications	#500620
The total cost of ownership: Xilinx FPGAs vs. traditional ASICs	White paper	#0010223-01
EPLDs		
XEPLD 5.1 EPLD development software overview	Features & benefits	#0010224-01
Development Systems		
Designing Xilinx FPGAs and EPLDs with Xilinx ABEL	Features & benefits	#0010116-03
Third-party solutions status	Current listing of Xilinx-compatible design kits from third-party Alliance (EDA) and Syndicate (synthesis) vendors	#0010106-03
Training		
On-site training course overview	Features and benefits of holding a Xilinx training class at your facility	#0010225-01

For a complete list, please contact your sales representative or see XCELL Issue #10.

Applications Notes

A vast array of Application Notes are available to help you design with Xilinx products. An application note can assist with a specific design or just provide ideas to spur your imagination. Many of the application notes include schematic or design files to help you get started. XNotes, a variation of an application note, are provided for users interested in learning more about a specific market or application.

Chapter 8 of the Xilinx Programmable Logic Data Book includes about 40 application notes with topics ranging from binary counters to 2-dimensional convolution filters. Several additional applications notes have recently been published; a list of all of the application notes and XNotes that are currently available as separate documents is given below.

FPGAs	A C-Cube CL550 motion JPEG codec design	#0010228-01
	FPGA configuration guidelines	#0010229-01
EPLDs	A zero-wait-state synchronous DRAM controller for the Pentium processor	#0010217-01
	Designing flexible PCI interfaces with Xilinx EPLDs	#0010216-01
	Designing with the XC7318 and XC7336	#0010218-01
	VME data acquisition interface and control in an XC7000 EPLD	#0010227-01
	Using Xilinx EPLDs in Mixed Voltage Systems	#0010183-02
	AMD MACH to Xilinx XC7000 EPLD Design Conversion Process	#0010187-01
Development Systems	XACT 5.0 guided tour	#0010222-01
Packaging	Footprint compatibility guide	#0010223-01
XNotes	Speed PCMCIA Modem Design with FPGAs	#100490-02
	FPGAs in the PC Card Market	#100460
	Incorporating CIS into XC4000 PCMCIA Designs	#100491
	Low Voltage Systems	#0010166
	A Fast Scalable Switch Matrix in an FPGA	#0010195-01
	The Peripheral Component Interconnect Bus	#0010210-01

Continued from page 2

based FPGA families that will use three-layer-metal processes in this manner, starting with the XC4000 family.

More dramatic advances in the capabilities of programmable logic devices will result as new device architectures are crafted that fully exploit the latest fabrication techniques. For example, the transition from two-layer to three-layer metal processes alters the logic vs. routing tradeoffs for FPGA architectures. The new Xilinx XC5000 FPGA family (see page 14) features the first FPGA architecture optimized for three-layer-metal CMOS process technologies, resulting in the lowest cost-per-gate of any FPGA family. The upcoming XC8100 FPGA family, scheduled for introduction in 1995, is based on a unique metal-to-metal antifuse programming element that puts the programmable routing switches, as well as the routing itself, in the metal layers above the silicon.

The continuing evolution of complex, submicron fabrication processes provides some challenges and opportunities for further increasing programmable logic performance. For example, consider the capacitance of the metal segments that make up the interconnect in FPGAs. Although the area capacitance decreases quadratically with decreasing gate length, the fringing capacitance increases, and could dominate in deep sub-micron processes. Thus, transistors with stronger current drive capability may be needed at the block outputs to charge the interconnect lines faster.

Fortunately, research techniques for designing new process technologies and transistor structures also are rapidly improving. The technology development group at Xilinx now applies Technology CAD process and device simulation tools (from Silvaco Inc.) running on a Sun workstation to the transistor development process. The Technology CAD simulation results closely resemble the operation of actual devices, providing a "virtual fab." Experiments that would require up to two months in a fabrication facility can now be simulated within days.

In summary, programmable logic is readily adaptable to the low-voltage, sub-half-micron, multi-metal-layer semiconductor fabrication technologies of the near future. Continued dramatic improvements to the capabilities of high-density programmable logic devices can be expected. Xilinx is firmly committed to the development of new process technologies for programmable logic, both by working closely with our foundry partners in the development and deployment of process advances, and by applying our knowledge and experience in programmable logic architectures to exploit those advances to the fullest. ◆

TRAINING COURSE NEWS

Customer-Site Classes

Xilinx training courses are offered in more than 50 locations worldwide. If you need help getting up-to-speed on Xilinx products, check out a training class in your area. For even greater convenience, we can bring the class to your facility. This eliminates all travel costs, and the course can focus more on your specific areas of interest.

Advanced Training

In addition to the three-day introductory classes, Xilinx offers one-day Advanced Training sessions. Advanced Training covers design tips and design methodologies that can help you get greater performance from your Xilinx designs. Advanced sessions are targeted at users who have experience with Xilinx products, but want to get more involved in the details of designing for the Xilinx architecture and controlling the implementation. Advanced Training can be brought to your facility. ***For information on classes, call your Xilinx representative or the Training Registrar at 408-879-5090.*** ◆

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - NOVEMBER 1994

Company	Product Name	Version	Function	Vendor Interface Name	FPGA Support	EPLD Support	X-BLOX Support
Acugen	ATGEN		Automatic Test Generation	LCA2ICT	✓		
ALDEC	Susie-Xilinx	6.12	Simulation	SusieXNF	✓		
	Active-Xilinx		Schematic Entry/Simulation		✓	✓	
Altium	P-CAD	6.0	Schematic Entry	PC-Xilinx	2K,3K		
Aptix	Explorer	2.0	Emulator	Axess 2.0	✓	✓	✓
Cadence (Valid)	Concept	1.7	Schematic Entry	Xilinx Front End	✓		✓
	Rapidsim	4.10	Simulation	Xilinx Front End	✓		
	Composer	4.3	Schematic Entry	Xilinx Front End	✓		✓
	Verilog	2.0.5	Simulation	Xilinx Front End	✓		
Capilano	DesignWorks	3.1	Schematic Entry/Simulation	XDK-1	✓		
Compass	Asic Navigator		Schematic Entry	Xilinx Design Kit	3K,4K		
	QSim		Simulation				
	X-Syn		Synthesis				✓
CV (Prime)	Design Entry	2.0	Schematic Entry	Xilinx Kit	✓		
Data I/O	ABEL	6.0	Synthesis	Xilinx Fitter	✓	✓	
	Synario	2.0	Schematic Entry	Xilinx Fitter	✓	✓	
EPS	SIMETRI	2.0	Simulation	XNF2SIM	✓	✓	
Exemplar Logic	CORE	2.0	Synthesis	FS-001	✓		✓
Flynn Systems	FS-ATG	2.6	Automatic Test Generation	FS-High Density	✓	✓	
IBM-EDA	BooleDozer		Synthesis		✓		
IKOS	2800/2900	5.02	Simulation	Xilinx Tool Kit	✓		
	Voyager	1.2	Simulation	Xilinx Tool Kit	✓		
Intergraph	ACE Plus	12.0	Schematic Entry	AdvanSIM & Veribest			
				Xilinx FPGA Design Kit	✓	Q4	✓
	AdvanSIM 1076	12.0	Simulation	AdvanSIM " " "	✓	Q4	✓
	VeriBest Design Systems	12.1	Schematic Entry/Simulation	VeriBest Design Kit	✓	Q4	✓
	Synovation	12.0	Synthesis	SynLibs	✓	Q4	
	PLDSyn	12.0	Schematic Entry/ Synthesis/Simulation		✓	✓	
ISDATA	LOG/iC	3.4	Synthesis	Xilinx Design Kit	✓		
IST	ASYL+		Synthesis/Partitioning		✓		
Logic Modeling (Synopsys Division)	Smart Model Library		Simulation Models	(In Library)	✓	✓	
	LM1200		Hardware Modeler	Xilinx Logic Module	✓		
Logical Devices	CUPL	4.5	Synthesis	Xilinx Fitter	✓	✓	
Mentor Graphics	QuickSim II	8.2_5	Simulation	Call Xilinx	✓	✓	✓
	Design Architect	8.2_5	Schematic Entry	Call Xilinx	✓	✓	✓
	Autologic	8.2_5	Synthesis	Xilinx Synthesis Library	✓		
MINC	PLDesigner-XL	3.0	Synthesis	Xilinx Design Module	✓		
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2K,3K		
Nishimura	G-DRAW	5.0	Schematic Entry	GDL2XNF	✓		
	G-LOG	4.03	Simulation	XNF2GDL	✓		
OrCAD	SDT 386+	1.1	Schematic Entry	Call Xilinx	✓	✓	✓
	VST 386+	1.2	Simulation	Call Xilinx	✓	✓	✓
	PLD 386+	2.0	Synthesis	Call OrCAD	✓		
Protel	Advanced Schematic	2.2	Schematic Entry		✓	✓	
Quad Design (Viewlogic Division)	Motive	3.4 Plus	Timing Analysis	XNF2MTV	✓		
Simucad	Silos III	94.2	Simulation	Included	✓		
Sophia Systems	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓	Q4	✓
Synopsys	FPGA Compiler	3.2	Synthesis	Call Xilinx	3K,4K	Q4	✓
	Design Compiler	3.2	Synthesis	Call Xilinx	3K,4K	Q4	✓
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓		
Topdown Design	V-BAK	1.0	XNF to VHDL translator	XNF interface	✓		
VEDA	System Hilo	4.3	Simulation	Xilinx Tool Kit	✓		
Viewlogic	ViewDraw	4.1.3a	Schematic Entry	Call Xilinx	✓	✓	✓
	ViewSim	4.1.3a	Simulation	Call Xilinx	✓	✓	✓
	ViewSynthesis	2.3	Synthesis	Call Xilinx	✓	✓	✓

ALLIANCE PROGRAM - PLATFORMS & CONTACTS

Company	Contact Name	Platform				Phone Number
		PC	Sun	Apollo	HP	
Acugen	Peter de Bruyn Kops					603-881-8821
ALDEC	Ron Williams	✓				702-293-2271
Altium	Ray Turner	✓	✓			408-534-4148
Aptix	Wolfgang Hoeflich		✓		✓	408-428-6200
Cadence	Itzhak Shapira		✓		✓	408-428-5739
Capilano	Chris Dewhurst	✓		Macintosh		604-522-6200
Compass	Mahendra Jain		✓	✓	✓	408-434-7950
CV (Prime)	Kevin O'Leary		✓			617-275-1800
Data I/O	Jay Gould	✓	✓			206-881-6444
EPS	Michael Massa	✓	✓			617-487-9959
Exemplar Logic	Michiel Ligthart	✓	✓		✓	510-849-0937
Flynn Systems	Mike Jingozian	✓				603-891-1111
IBM-EDA	John Orfitelli			RS6000		914-433-9073
IKOS	Brad Roberts		✓	✓	✓	408-255-4567
Intergraph	Vince Mazur		✓			303-581-2301
ISDATA	Peter Bauer	✓	✓		✓	+49-721-751087
IST	Peter Robinson	✓	✓		✓	510-736-2302
Logic Modeling *(Synopsys Division)*	Laura Horsey	✓	✓	✓	✓	503-531-2271
Logical Devices	Joleen Rasmussen	✓				305-428-6868
Mentor Graphics	Steve Eichenlaub		✓	✓	✓	503-685-1559
MINC	Lynne Dolan	✓	✓		✓	719-590-1155
Minelec		✓				+32-02-4603175
Nishimura	Robert Bartels	✓	✓		✓	415-398-1669
OrCAD	Jim Plymale	✓				503-671-9500
Protel	Matthew Schwaiger	✓	✓			408-243-8143
Quad Design *(Viewlogic Division)*	Vern Potter	✓	✓	✓	✓	805-988-8250
Simucad	John Williamson	✓	✓			510-487-9700
Sophia Systems	Terry Wilfley	✓	✓		✓	415-813-4762
Synopsys	Lynn Fiance		✓	✓	✓	415-694-4102
Teradyne	Phil McAuliffe	✓	✓			617-422-3677
VEDA	Anne Crow		✓		✓	+44-329-82-2240
ViewLogic	Meredith Luckewicz	✓	✓		✓	508-480-0881

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. ◆

Feb. 12 - 14, 1995
1995 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays
Monterey, California

Mar. 6 - 9, 1995
The European Design and Test Conference 1995 (EDAC-ETC-EUROASIC)
Paris, France

Mar. 29 - 31, 1995
PCI '95 - The PCI Bus Industry Conference
Santa Clara, California

For further information about any of these conferences, contact Kathleen Pizzo (Tel: 408-879-5377 Fax: 408-879-4780).

COMPONENT AVAILABILITY CHART - NOVEMBER 1994

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003	XC4005	XC4006	XC4008	XC4010	XC4010D	XC4013	XC4013D	XC4025	XC4002A	XC4003A	XC4004A	XC4005A	XC4003H	XC4005H	XCZ36	XCZ22	XCZ36A	XCZ22A	XCZ318	XCZ336	XCZ354	XCZ372	XCZ3108	XCZ3144
44	PLASTIC LCC	PC44	◆	◆				◆				◆										◆																			◆		◆		◆	◆	◆			
	PLASTIC QFP	PQ44																																													◆	◆				
	CERAMIC LCC	WC44																																									◆		◆			◆	◆			
48	PLASTIC DIP	PD48	◆																																																		
64	PLASTIC VQFP	VQ64		◆	◆	◆						◆					◆																																					
68	PLASTIC LCC	PC68	◆	◆	◆		◆	◆			◆	◆										◆	◆																						◆		◆			◆	◆			
	CERAMIC LCC	WC68																																										◆		◆			◆	◆			
	CERAMIC PGA	PG68	◆																																																		
84	PLASTIC LCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆		◆	◆	◆	◆	◆					◆	◆	◆	◆			◆		◆				◆	◆		
	CERAMIC LCC	WC84																																										◆		◆				◆	◆		
	CERAMIC PGA	PG84		◆			◆	◆	◆		◆	◆	◆									◆	◆	◆																					◆		◆							
100	CERAMIC QFP	CQ100				◆		◆																																													
	PLASTIC PQFP	PQ100				◆	◆	◆			◆	◆	◆									◆	◆	◆			◆											◆	◆												◆	◆		
	PLASTIC TQFP	TQ100		◆			◆	◆														◆	◆																														
	PLASTIC VQFP	VQ100			◆							◆	◆			◆	◆					◆	◆															◆	◆														
	TOP BRZ. CQFP	CB100				◆		◆			◆		◆									◆		◆															◆														
120	CERAMIC PGA	PG120																									◆									◆	◆	◆														
132	PLASTIC PGA	PP132						◆	◆			◆	◆										◆	◆																														
	CERAMIC PGA	PG132						◆	◆			◆	◆										◆	◆																														
144	PLASTIC TQFP	TQ144										◆	◆					◆	◆				◆	◆																				◆	◆								
	CERAMIC PGA	PG144																																																		◆	
156	CERAMIC PGA	PG156																										◆	◆																◆								
160	PLASTIC PQFP	PQ160							◆	◆			◆	◆										◆	◆	◆		◆	◆	◆	◆	◆	◆	N	N	◆		◆	◆											◆	N
164	CERAMIC QFP	CQ164								◆																																										
	TOP BRZ. CQFP	CB164								◆				◆											◆	N		◆																									
175	PLASTIC PGA	PP175								◆				◆											◆	◆																												
	CERAMIC PGA	PG175								◆				◆											◆	◆																												
176	PLASTIC TQFP	TQ176												◆						◆					◆																												
184	CERAMIC PGA	PG184																																																			
191	CERAMIC PGA	PG191																												◆	◆													◆								
196	TOP BRZ. CQFP	CB196																													◆																				
208	PLASTIC PQFP	PQ208								◆				◆											◆	◆				◆	◆	◆	◆	N	◆	N								◆	◆							
	METAL MQFP	MQ208																												◆	◆	N	◆																		
223	CERAMIC PGA	PG223																							◆								◆		N								◆								
225	PLASTIC BGA	BG225																													◆	N	◆	N																◆	N
228	TOP BRZ. CQFP	CB228																															N																		
240	PLASTIC PQFP	PQ240																															◆	N									◆								
	METAL MQFP	MQ240																															◆		◆								◆								
299	CERAMIC PGA	PG299																																	◆																

◆ = Product currently shipping or planned N = New since last XCELL

XILINX RELEASED SOFTWARE STATUS - NOVEMBER 1994

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform				Last Update
					PC1 *6.2*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS									
CORE FPGA	XC2,3,4K Support	Core Implementation	DS-502-xxx	5.00	5.02	5.02	1.42	5.02	09/94
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	5.00	5.02	5.02		5.02	09/94
Mentor[1]	V7.00	I/F and Libraries	DS-343-xxx	4.10			4.20		07/94
Mentor[1]	V8.2_5	I/F and Libraries	DS-344-xxx	1.10		5.00	1.10	5.00	07/94
OrCAD[2]		I/F and Libraries	DS-35-xxx	4.23	5.00				07/94
Synopsys[1]		I/F and Libraries	DS-401-xxx	3.01A		3.01B	3.01B	3.01B	08/94
Viewlogic[2]	ViewDraw	I/F and Libraries	DS-390-xxx	4.15	5.00				07/94
Viewlogic[2]	ViewSim	I/F and Libraries	DS-290-xxx	4.15	5.00				07/94
Viewlogic[2]		I/F and Libraries	DS-391-xxx	4.15	5.00	5.1		5.1	07/94
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	4.30	5.00	5.00			07/94
X-BLOX[1]		Module Generation & Opt.	DS-380-xxx	1.04	5.00	5.00	1.04	5.00	07/94
XILINX PACKAGES									
Mentor 8	Standard		DS-MN8-STD-xxx	5.00		5.02	1.10	5.02	09/94
OrCAD	Base		DS-OR-BAS-xxx	5.0	5.02				09/94
OrCAD	Standard		DS-OR-STD-xxx	1.10	5.02				09/94
Synopsys	Standard		DS-SY-STD-xxx	1.10		2.00	2.00	2.00	08/94
Viewlogic	Base		DS-VL-BAS-xxx	5.00	5.02				09/94
Viewlogic	Standard		DS-VL-STD-xxx	1.20	5.02	5.02		5.02	09/94
Viewlogic/S	Base		DS-VLS-BAS-xxx	5.0	5.02				09/94
Viewlogic/S	Standard		DS-VLS-STD-xxx	5.00	5.02				09/94
Viewlogic/S	Extended[3]		DS-VLS-EXT-xxx	5.00	5.02				09/94
XILINX HARDWARE									
Device Pgmr.	Prom. Pgmr.		HW-112 (XPP)	3.31	5.00	5.00			06/94
Device Pgmr.	EPLD/Prom. Pgmr.		HW-120 (Prolink)	3.14	5.00				06/94
THIRD PARTY PRODUCTION SOFTWARE VERSIONS									
Cadence	Composer	Schematic Entry	N/A	4.2.2		4.30		4.30	N/A
Cadence	Verilog	Simulation	N/A	1.7BP		2.0.5		2.0.5	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.60		1.7		1.7	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	3.0BP		4.10		4.10	N/A
Mentor	NETED	Schematic Entry	N/A				7.XX		N/A
Mentor	QuickSim	Simulation	N/A				7.XX		N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2_5		8.4	8.4	8.4	N/A
Mentor	QuickSim II	Simulation	N/A	8.2_5		8.4	8.4	8.4	N/A
OrCAD	SDT 386+	Schematic Entry	N/A		1.10				N/A
OrCAD	VST 386+	Simulation	N/A	1.10	1.20				N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.01a		3.1b	3.1b	3.1b	N/A
Viewlogic	ViewDraw	Schematic Entry	N/A		4.1.3a	5.1		5.1	N/A
Viewlogic	ViewSim	Simulation	N/A		4.1.3a	5.3		5.3	N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A		6.0	6.0			N/A
Data I/O	Synario	Entry and Simulation	N/A		2.0				N/A

NOTE: [1]FPGA Only [2]FPGA and EPLD [3]Includes ViewSynthesis v2.3.1

Programmer Support for Xilinx XC7200 EPLDs — November 1994

Vendor	Model	7236	7236A	7272	7272A	PC44	PC68	PC84	PG84	Comments
Advin Systems	Pilot-U40 Pilot-U84	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	USA-84 USA-84	USA-84 USA-84	USA-84 USA-84	 AM-XC84G	
B&C Microsystems	Proteus	V3.6j	V3.6j	V3.7h	V3.7h	AMUPLC84	AMUPLC84	AMUPLC84		
BP Microsystems	BP-1200	v2.32	v2.32	v2.34	v2.34	SM44P	SM68P or SM84UP	SM84P or SM84UP	SM84UGA	
DATA I/O	UniSite 2900 3900 AutoSite	v4.3 V3.4* v2.1 V2.4*	v4.6* V3.4* V2.4* V2.4*	v4.5 v3.3* v2.3 v2.3	v4.5** v3.3** v2.3** v2.3**	USBASE-PLCC PPI-0243 3900-PLCC PLCC-44-1	USBASE-PLCC PPI-0246 3900-PLCC PLCC-68-1	USBASE-PLCC PPI-0208 3900-PLCC PLCC-84-1		*7236A=PPI-0243 **7272A=PPI-0246 (PC68) **7272A=PPI-0247 (PC84)
Deus Ex Machina	XPGM	V1.00	V1.00	V1.00	V1.00	1	2	3		
Elan Digital Systems	6000 APS	K2.04	K2.04	K2.06	K2.06	PDi84	PDi84	PDi84		
Hi-Lo Systems Research	All-03A All-07	V3.01 V3.01	V3.01 V3.01	V3.00 V3.00	V3.00 V3.00	ADP-XC7236-PL44 PAC-PLCC44	ADP-XC7272-PL68 PAC-PLCC68	ADP-XC7272QPI-84		
ICE Technology Ltd.	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00		S 11/94 S 11/94 S 11/94 S 11/94	S 11/94 S 11/94 S 11/94 S 11/94					
Logical Devices	ALLPRO-88 ALLPRO-88XR XPRO-1	2.2 1.35 1.01	P 4Q94 P 4Q94 1.01	2.2 1.35 1.01	P 4Q94 P 4Q94 1.01	C C MODXP1-44L	C C MODXP1-68L	C C MODXP1-84L	 MODXP1-84G	
MQP Electronics	SYSTEM 2000 PINMASTER 48	P 1Q95 P 1Q95	P 1Q95 P 1Q95	P 1Q95 P 1Q95	P 1Q95 P 1Q95	MP1 Universal Socket	MP1 Universal Socket	MP1 Universal Socket	Universal programmer	
Stag	Eclipse	P 4Q94	P 4Q94	P 4Q94	P 4Q94	EPU84P+	EPU84P+	EPU84P+		
SMS	Expert Optima Multisyte	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1		
System General	TURPRO-1 TURPRO-1 F\X	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	P44 P44	P68 P68	P84 P84		
Tribal Microsystems	TUP-300 TUP-400 FLEX-700	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	TUP-7236 TUP-7236 TUP-7236	TUP-7272 TUP-7272 PAC-PLCC68			PAC-PLCC 44
Xeltek	SUPERPRO SUPERPRO II	1.7C 1.7C	2.2 2.2	2.1 2.1	2.1 2.1	XXC7236-44PL/40D XXC7236-44PL/40D	XXC7272-68PL/68D XXC7272-68PL/68D	XXC7272-84PL/84D XXC7272-84PL/84D		
Xilinx	HW-120	V3.14	V3.14	V3.14	V3.14	HW-120-PC44	HW-120-PC68	HW-120-PC84	HW-120-PG84	

Programmer Support for Xilinx XC7300 EPLDs — November 1994

Vendor	Model	7318	7336	7354	7372	73108	73144	PC44	PC68	PC84	PQ44	PQ100	PQ160	PG184	BG225
Advin Systems	PILOT-U84	10.78B	10.78B	10.78B	10.78B	S 11/94	P 1Q95	USA-84	USA-84	USA-84		AM-XC100Q	AM-XC160Q		
B&C Microsystems	Proteus	3.7k	3.7k	3.7k	P 11/94	3.7k	P 1Q95	C	C	C					
BP Microsystems	BP-1200	V3.01	V3.01	V3.01				SM44P	Special Adapter	Special Adapter		Special Adapter		Special Adapter	Special Adapter
DATA I/O	2900 3900 UniSite AutoSite	V3.5 V2.5 V4.7 V4.7	V3.5 V2.5 V4.7 V4.7	V3.5 V2.5 V4.7 V4.7	BBS BBS BBS BBS	BBS BBS BBS BBS	P 1Q95 P 1Q95 P 1Q95 P 1Q95	2900-PLCC 3900-PLCC USBASE-PLCC PLCC-44-1	3900-PLCC USBASE-PLCC PLCC-68-1	3900-PLCC USBASE-PLCC PLCC-84-1					
Deus Ex Machina	XPGM	V1.00	V1.00	V1.10	P 11/94	V1.00	P 1Q95	5	6 (13 for 7372)	7					
Elan	6000 APS	P 11/94	P 11/94	P 11/94	P 11/94	P 11/94	P 1Q95	C							
Hi-Lo Systems Research	All-03A All-07	V3.04 V3.02	V3.04 V3.02	V3.04 V3.02	P 1/95 V3.01	V3.00 V3.00	P 1Q95 P 1Q95	PAC-PLCC44	PAC-PLCC68						
ICE Technology, Ltd.	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	S 11/94 S 11/94 S 11/94 S 11/94	S 11/94 S 11/94 S 11/94 S 11/94	P 1Q95 P 1Q95 P 1Q95 P 1Q95	AD-7336-PLCC-44 AD-7336-PLCC-44 AD-7336-PLCC-44 AD-7336-PLCC-44	AD-7354-PLCC-68 AD-7354-PLCC-68 AD-7354-PLCC-68 AD-7354-PLCC-68	AD-73108-PLCC-84 AD-73108-PLCC-84 AD-73108-PLCC-84 AD-73108-PLCC-84					
Logical Devices	ALLPRO-88 ALLPRO-88XR XPRO-1	P 4Q94 P 4Q94 1.01	P 4Q94 P 4Q94 1.01	P 4Q94 P 4Q94 1.01	P 4Q94 P 4Q94 1.01	P 4Q94 P 4Q94 1.01	P 2Q95 P 2Q95 P 1Q95	C C MODXP1-5444L	C C MODXP1-5468L	C C MODXP1-108L			MODXP1-160Q	MODXP1-184G	MODXP1-108B
MQP Electronics	SYSTEM 2000 PINMASTER 48	P 1Q95 P 1Q95	P 1Q95 P 1Q95	P 1Q95 P 1Q95	P 1Q95 P 1Q95	P 1Q95 P 1Q95	P 2Q95 P 2Q95	MP1 Universal Socket	MP1 Universal Socket	MP1 Universal Socket					
SMS	EXPERT	P 12/94	P 12/94	P 12/94	P 12/94	P 12/94	P 1Q95	TOP1	TOP1	TOP1					
Stag	ECLIPSE	4.10.31	4.10.31	4.10.31	4.10.31	4.10.31	P 1Q95								
System General	TURPRO-1	V2.2	V2.2	V2.2	V2.2	V2.2	P 1Q95	C							
Tribal Microsystems	ALL-07	V3.02	V3.02	V3.02	V3.01	V3.00	P 1Q95	PAC-PLCC44	PAC-PLCC68						
Xeltek	SUPERPRO SUPERPRO II	2.1 2.1	2.1 2.1	2.1 2.1	P 4Q94 P 4Q94	P 4Q94 P 4Q94	P 1Q95 P 1Q95	XXC7354-44PL/40D XXC7354-44PL/40D	XXC7354-68PL/40D XXC7354-68PL/40D						
Xilinx	HW-120	V5.00	V5.00	V5.00	V5.00	V5.00	P 4Q94	HW126-PC44	HW126-PC68	HW126-PC84			HW126-PQ160	HW126-PG184	HW126-BG225

C = Currently Supported (no version number) P = Planned Release S = Scheduled Release

Programmer Support for Xilinx XC1700 Serial Proms — November 1994

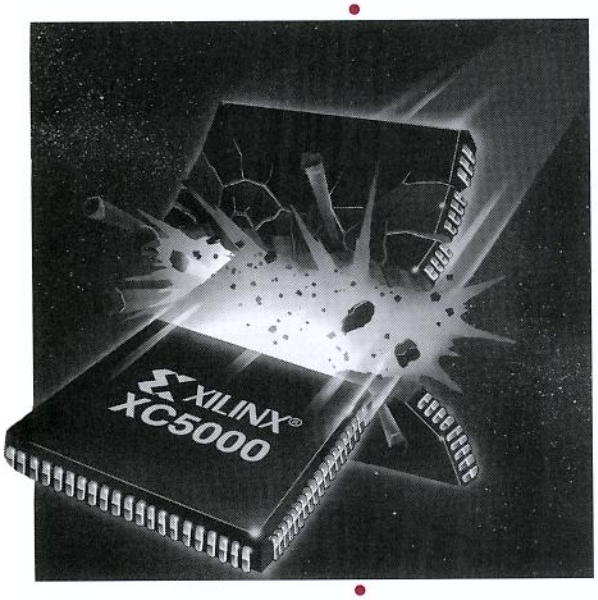
VENDOR	MODEL	1736A	1765	17128	17XXD	17XXL	17128D/ 17256D	DIP8	PC20	SO8
Advantech	PC-UPROG	V1.80	V1.80	V2.1	V2.0			X		
Advin Systems	PILOT-U24	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX-20	SO-8
	PILOT-U28	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-U32	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-U40	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-U84	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-142	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
	PILOT-143	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
	PILOT-144	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
	PILOT-145	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
AVAL	PECKER-50			C	C			X		
	PKW5100			C	C			X		
B&C Microsystems	Proteus-UP40	V3.4E	V3.4E	V3.4E	V3.5F	V3.7F	V3.7L	X	AMUPLC84	
BP Microsystems	CP-1128	C	C	V2.17*	V2.21C*	V2.34*	S 11/94	FH28A	FH28A + 3rd Party	FH28A + 3rd Party
	EP-1140	C	C	V2.17	V2.21C	V2.34	S 11/94	FH40A	FH40A + 3rd Party	FH40A + 3rd Party
	BP-1200	C	C	V2.17	V2.21C	V2.34	S 11/94	SM48D	SM20P or SM84UP	3rd Party
BYTEK	135H-FT/U	V42	V42					MTA		
	MTK-1000	V42	V42					MTA		
	MTK-2000	V42	V42					MTA		
	MTK-4000	V42	V42					MTA		
DATA I/O	UniSite/Site 40/48	V3.0	V4.0	V4.1	V4.1	V4.6	BBS	X	USBASE-PLCC	USBASE-SOIC
	UniSite/ChipSite	V3.4	V4.0	V4.1	V4.1	V4.6	BBS	X	USBASE-PLCC	USBASE-SOIC
	UniSite/PinSite	V3.4	V4.0	V4.1	V4.1	V4.6	BBS	X	USBASE-PLCC	USBASE-SOIC
	2900	V1.5	V2.1	V2.2	V2.2	V3.4	BBS	X	2900-PLCC	2900-SOIC
	3900	V1.0	V1.5	V1.6	V1.6	V2.4	BBS	0101	3900-PLCC	3900-SOIC
	AutoSite	V1.1	V1.5	V1.6	V1.6	V2.4	BBS	DIP-300-1	PLCC-20-2	
	UniPak 2B	V23	V24					351B120D		
	ChipLab	V1.1	V1.0	V1.0	V1.0	V1.1	V2.0	X		080801S300
Deus Ex Machina	XPGM			V1.00	V1.00	V1.00	V1.10	0	3rd Party	3rd Party
Elan Digital Systems	3000-145	C	C	C				A116		
	5000-145	C	C	C				A116		
	6000 APS	K2.01	K2.01	K2.02	K2.01	K2.10	K2.13	X	uPD184	
Hi-Lo Systems Research	ALL-03A	V3.30	V3.30	V3.30	V3.30	V3.30	S 11/94	X	CNV-PLCC-XC1736	CVN-SOP-NDIP16
	ALL-07	V3.30	V3.30	V3.30	V3.30	V3.30	S 11/94	PAC-DIP40	PAC-PLCC44	
ICE Technology, Ltd.	Micromaster 1000/1000E	V1.1	V1.5	V3.00	V3.00		V3.00	X	AD-1736/65-20	
	Speedmaster 1000/1000E	V1.1	V1.5	V3.00	V3.00		V3.00	X	AD-1736/65-20	
	Micromaster LV			V3.00	V3.00	V3.00	V3.00	X		
	LV40 Portable			S 1/95	S 1/95	S 1/95	S 1/95	X		
	Speedmaster LV			V3.00	V3.00	V3.00	V3.00	X		
Link Computer Graphics	CLK-3100	C	C	V4.1	V4.13			X1736	PLCC-17XX	
Logical Devices	ALLPRO-40	2.2	2.2					X	OPTPLC-208	OPTSOI-080
	ALLPRO-88	2.2	2.2	2.3	2.3			X		OPTSOI-080
	ALLPRO-88XR	1.1	1.0	2.3	1.3			X		OPTSOI-080
	CHIPMASTER 3000	2.0	2.0	2.1	2.0			X	OPTPLC-208	OPTSOI-080
	CHIPMASTER 5000	1.15	1.15					X	OPTPLC-208	OPTSOI-080
	XPRO-1	1.01	1.01	1.01	1.01	1.01		MODXLN-173	MODXLN-173	MODXLN-173
MQP Electronics	MODEL 200	C	C	6.45	6.45	6.45	6.46	AD13A-16		
	SYSTEM 2000 (Gang)			P 11/94	P 11/94	P 11/94	P 11/94	MP6		
	SYSTEM 2000			1Q95	1Q95	1Q95	1Q95	MP1		
	PINMASTER 48			1Q95	1Q95	1Q95	1Q95	X		
Micro Pross	ROM 5000 B	C	C	V1.70	V1.70			Mu 40		
	ROM 3000 U	C	C	V3.60	V3.60					
Red Square	IQ-180	C	C		V8.2					
	IQ-280	C	C		V8.2					
	Univriter 40	C	C		V8.2					
	Chipmaster 5000	C	C		V8.2					
Retnel Systems	ZAP-A-PAL	C	C		V3.8J			Module #36		
SMS	Expert	B/93	B/93	A/94	A/94	A1/94	S 12/94	TOP40DIP	TOP1PLC or	
	Optima	B/93	B/93	A/94	A/94	A1/94	S 12/94	"	TOP3PLC/TOP3PLC	
	Multisyte				A/94			"	"	
	Plus48	B/93	B/93	A/94	A/94	A1/94	S 12/94			
	Sprint Plus	B/93	B/93	A/94						
STAG	Eclipse	10.76C	10.76C	4.4	2.2	4.3	4.10.31	EPU48D	EPU84P	
	Quasar			10.76C	10.76C	10.76C		X	AMPLCC20	
Sunrise	T-10	C	C		V3.13			X		
System General	TURPRO-1	C	C	V2.14	V2.01	V2.12	S 11/94	DIP-Adapter	P20-Adapter	
	Turpro-1 F\X	C	C	V2.14	V2.01	V2.12	S 11/94	DIP-Adapter	P20-Adapter	
	APRO	C	C	V2.14	V2.01	V2.12	S 11/94	X	X	
Tribal Microsystems	TUP-300	C	C	V3.31	V3.31	V3.37C	S 11/94	X	CNV-PLCC-XC1736	
	TUP-400	C	C	V3.31	V3.31	V3.37C	S 11/94	X	"	
	FLEX-700	C	C	V3.31	V3.31	V3.37C	S 11/94	X	"	
Xeltek	SuperPRO	1.5B	1.5B	1.7C	1.7D	1.8	P 4Q94	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
	SuperPRO II	1.5B	1.5B	1.7C	1.7D	1.8	P 4Q94	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
Xilinx	HW112	C	C	V3.11	V3.31	V3.31	V5.0.0	X	HW-112-PC20	HW-112-SO8
	HW120	V5.00	V5.00	V5.00	V5.00	V5.00		HW-120-PRM	HW-120-PRM	HW-120-PRM

C = Currently Supported, P = Planned, S = Scheduled Release Date, X=Package Supported

Introducing the XC5000 Family

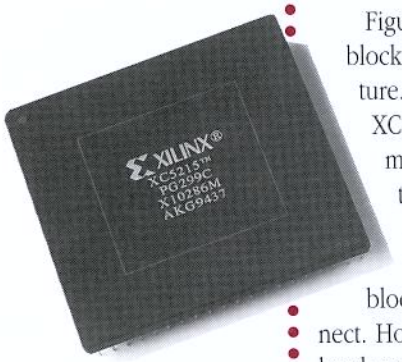
Today's Gate Array

Building on the experiences gained with the first three generations of SRAM-based FPGA devices, the new XC5000 family features the first FPGA architecture specifically optimized for three-layer-metal, sub-micron CMOS process technology. The result is a dramatic decrease in the "cost-per-gate" for FPGAs. The XC5000 family is targeted at low-end gate array users (< 20K gates, < 40 MHz), who can now gain the convenience and time-to-market benefits of FPGAs at a total cost that is competitive with traditional ASICs. The architecture also was designed to allow the placement and routing of designs using the proven automated design tools of the XACT® Development System.



XC5000 Architectural Overview

Figure 1 illustrates the basic building blocks of the XC5000 FPGA architecture. As with previous generations, the XC5000 architecture uses static memory cells to hold its configuration data, and includes programmable Input/Output Blocks (IOBs), programmable logic blocks, and programmable interconnect. However, the logic blocks and their local routing resources are uniquely combined into flexible structures named VersaBlocks™. The VersaBlocks, in turn, are interconnected through a General Routing Matrix (GRM). The VersaBlock-GRM structure facilitates the fast, local assembly of logic functions, effectively implementing user designs in a hierarchical fashion. Incremental routing resources are provided around the edge of the logic array. This interface between the IOBs and the core logic is called the VersaRing™, and increases user flexibility in the assignment of I/O pins.



The resources of each VersaBlock include a powerful and flexible configurable logic block (CLB) surrounded by a set of local routing resources (Figure 2). As in past generations, combinational functions are implemented using memory-lookup tables (LUTs) and dedicated registers provide storage functions within each CLB. Local interconnections include feedback paths from the CLB's outputs to its inputs, direct connections to neighboring CLBs, and a rich set of connections to the General Routing Matrix.

Each XC5000 CLB, in turn, contains four logic cells (labeled LC0 through LC3 in Figure 2), where each cell contains a 4-input function generator, a register, and control logic (Figure 3). The control logic in the CLB allows the function generators to be cascaded to implement carry chains or wide functions. Registers can be configured as edge-triggered master-slave flip-flops or level-sensitive latches, with optional clock inversion, clock enable, and asynchronous clear functions. The function generators can be bypassed to reach a register, allowing the function generators and registers to be used independently where desired. This increases utilization and allows the placement algorithms greater freedom during design implementation.

In previous-generation architectures, the programmable interconnect resources ran "between" the logic blocks of the FPGA's array on the physical layout of the silicon die. With three-layer metal process technology, much of the interconnect can be placed "on top" of the logic blocks. This

XILINX®

gives rise to the concept of a VersaBlock - a tile that consists of the CLB's logic plus the multiplexers, switches, and local routing paths that control the connections to that CLB's inputs and outputs. This tile is replicated throughout the matrix, with a fixed pattern of interconnection to the General Routing Matrix (GRM).

The General Routing Matrix (GRM) includes a rich amount and variety of routing resources chosen to allow efficient automatic routing. Advanced simulation tools were used to determine the optimal level of routing resources required to implement designs efficiently. The automated place and route tools take advantage of a hierarchy of routing resources, choosing the most appropriate interconnect type for a given connection. Available routing channels in the GRM include single-length lines, double-length lines, long lines, and global networks.

Altogether, the XC5000 architecture contains five levels of interconnect hierarchy: the single-length, double length, and long/global lines of the GRM, and the direct connects and local feedback paths of the VersaBlock. This hierarchy of resources takes advantage of the 'locality' of logic in typical designs; logic functions that are heavily interconnected can be placed in nearby CLBs and use the Versablocks' direct connections. The GRM resources are now dedicated to interconnecting large pieces of logic rather than small ones. This combination of symmetrical fine-grained and course-grained elements maximizes logic utilization and takes advantage of three-layer metal technology.

The I/O block primarily consists of an input and output buffer. Registers in adjacent CLBs can be used to register or latch incoming or outgoing data. The XC5000 I/O block contains all the features expected of a high-performance FPGA, including programmable TTL or CMOS input voltage thresholds, optional three-state controls for the output buffer, programmable polarity for the input, output, and enable signals, slew rate controls, and optional pull-up and pull-down resistors. Also, several nanoseconds of delay optionally can be included on the input path. This feature eliminates data hold times for incoming data that must be latched in a nearby CLB; the delay on the input path compensates for the delay on a clock signal that must first pass through a global clock buffer before arriving at the same CLB. Each output buffer is capable of sinking 4 mA.

The VersaRing contains extra routing and switches located around the periphery of the VersaBlock matrix. These incremental routing resources eliminate one of the traditional trade-offs facing FPGA designers: high logic utilization versus pin assignment flexibility. The XC5000 architecture decouples the I/O from the core logic, giving users significantly increased "pin-locking" flexibility.

XC5000 Family Products

Table 1 shows the first three planned members of the XC5000 family. These three devices address the low-end of the gate array market, which centers about 10,000 gates. HardWire versions are in development.

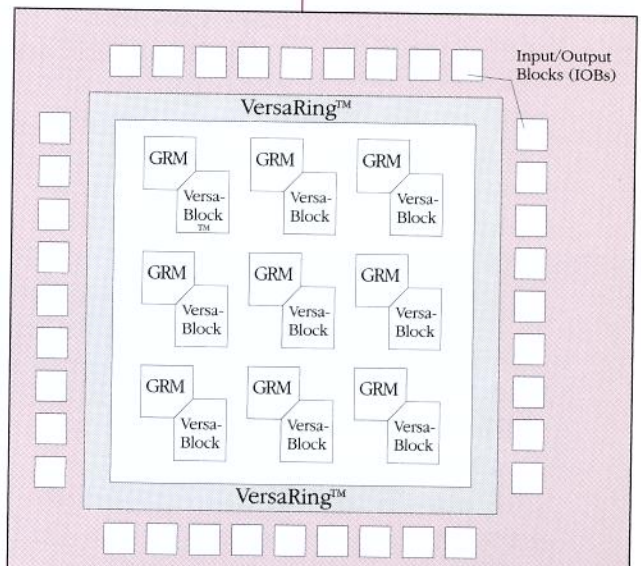


Figure 1: The XC5000 architecture consists of a matrix of VersaBlocks, a perimeter of I/O blocks and a General Routing Matrix.

Design tool support is incorporated into the XACT Development System; XACT software support for the XC5000 family will be provided free-of-charge to all in-warranty users. The XC5000 architecture is supported by the same set of implementation tools as the XC4000 family, including PPR (the auto-

XC5000

Continued from the previous page

mated partition, place, and route program, including XACT-Performance timing controls), the Unified Library (for schematic entry), the X-BLOX™ module generators, and the XDelay static timing analyzer.

Table 1: Initial XC5200 FPGA Family Members

Device	XC5206	XC5210	XC5215
Estimated usable gates	6,000	10,000	15,000
VersaBlock matrix	14 x 14	18 x 18	22 x 22
Total CLBs	196	324	484
Total Flip-Flops	784	1,296	1,936
Total IOBs	148	192	244

The XC5000 initially will support system clock rates up to 40 MHz for most applications. Relative to the XC4000, performance will lag by approximately one speed grade (-7/-6/-5). Higher speed devices will result from migrations to finer-geometry processes in the future. The XC4000 and XC3100A families remain the best FPGAs for even higher-performance applications.

The XC5000 family devices are footprint-compatible with XC4000 devices in the same package types; all the control pins, configuration pins, and power pins are in the same locations. No board relayout is required to plug an XC5000 device into an XC4000 socket, or vice-versa. The design, of course, would need to be re-routed in the newly-selected architecture.

Engineering samples of the XC5206 and XC5210 (-7/-6 speed grade, PLCC packages) will be available in early 1995, with production scheduled for the second quarter. Pre-production software with Viewlogic and Mentor Graphics interfaces for the Sun and PC platforms will be available to selected users in the first quarter of 1995, with the production release in the second quarter. Available packages will include PLCCs (plastic leaded chip carriers), PQFPs (plastic quad flat packs), PGAs (pin grid arrays), and BGAs (ball grid arrays). Projected volume pricing for the XC5210-7 in the first half of 1995 is $39 (PLCC packaging).

In summary, the XC5000 is the first FPGA family designed "from the ground up" specifically for three-layer metal CMOS fabrication processes. By combining a three-layer metal, 0.6 µ process technology with the new XC5000 architecture, Xilinx has achieved a technology breakthrough that delivers dramatically lower prices for high-density programmable logic. ◆

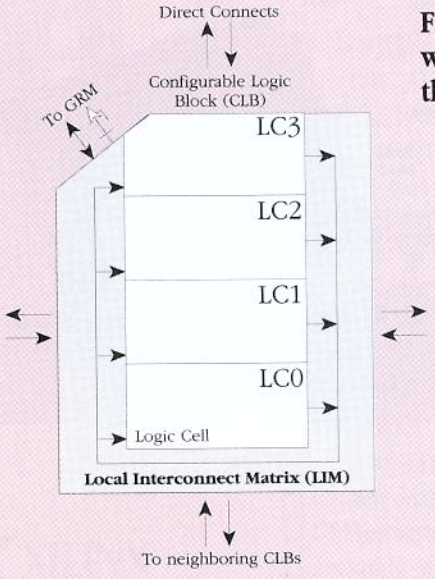


Figure 2: The VersaBlock includes a Configurable Logic Block with four logic cells, local routing resources and connections to the General Routing Matrix

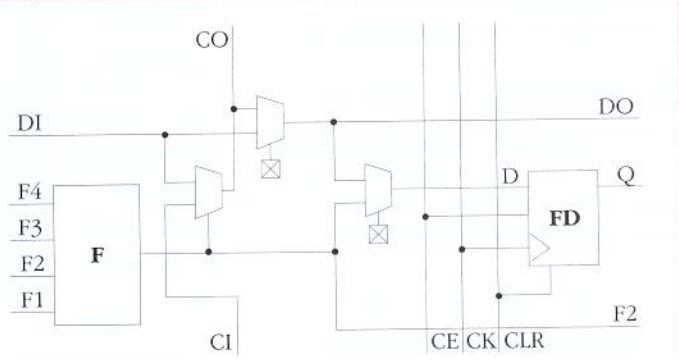


Figure 3: The basic logic cell.

High-Performance XC3100A-2 Update

The XC3100A-2 is the ultimate FPGA solution for high-performance applications. This new speed grade is 20% faster than previous versions (see XCELL #13, page 13). With an average PREP benchmark speed of 85 MHz, the XC3100A-2 is the fastest FPGA available today.

Five family members, ranging from the XC3130A to the XC3195A are in full production; packaging options include the PC84, VQ100, PQ160, PG175, and PP175 packages. Furthermore, prices for the XC3100A-2 devices were lowered by 20% in October. This combination of low price and high performance makes the XC3100A family the optimal FPGA for high-performance applications. The XC3100A-2 speed file is available on the Xilinx Technical Bulletin Board, and will be included in the upcoming XACT v5.1 update. Please contact your local Xilinx sales representative for specific pricing and availability information.

The XC3100A-2 devices also are the first FPGAs to be fully PCI compliant. (For more information, contact the Literature Hotline at 1-800-231-3386 and request the PCI Compliance Packet.) ◆

New 144-Macrocell EPLD is 100% PCI Compliant

Xilinx is proud to introduce the largest device in the high-performance XC7300 EPLD family: the XC73144. The XC73144 is a 144-macrocell device offering a pin-to-pin propagation delay of 7.5 ns and a system clock speed of 105 MHz. As the largest member of the XC7300 series incorporating the advanced Dual-Block architecture, the XC73144 contains four Fast Function Blocks (FFBs) and 12 High Density Function Blocks (HDFBs). The blocks are connected by a Universal Interconnect Matrix (UIM®) that provides 100% routing and 100% utilization of device resources, allowing a designer to lock down his pins through multiple design iterations.

PCI Compliant

The XC73144 is an extremely attractive device to implement PCI designs. A full PCI master-slave design can fit into a single XC73144 and provide **100% compliance** with all electrical and performance requirements of the PCI specification — including 3V/5V interface, high drive capability and all speed metrics. This is the only EPLD in the industry which can provide the performance needed for 100% PCI compliance along with sufficient logic resources to implement PCI designs on a single device.

Easy-to-Use Development Software

The XC73144 is supported by the XEPLD Rev. 5.1 suite of design tools. Using these tools, a design can be described and targeted for the XC73144 with push-button ease. Furthermore, Xilinx provides an extensive offering of interfaces to the industry's most popular synthesis and schematic design software, allowing the designer to remain in his favorite tool environment. XEPLD Rev. 5.1 efficiently optimizes XC73144 designs by automatically invoking all architectural features. In fact, the actual details of the architecture can remain completely invisible to the user. Once design entry and fitting is completed, the software generates a Static Timing Report to verify timing performance on all paths *(see related article, page 34)*.

Programming Support

Data I/O, Logical Devices, and BP Microsystems are among the numerous third party vendors who will support programming for the XC73144. For quick and convenient prototyping, Xilinx also offers the HW130 programmer, a system developed by Xilinx to support all of its programmable products.

The XC73144 will begin sampling in PQ160 packages by January, 1995 and production volumes will follow in February. A plastic 225-pin BGA (ball grid array) package will be available four weeks later, and a windowed 225-pin BGA in April.

Please contact your local Xilinx sales representative for further information. ◆

One Million Devices... And Counting

In October, cumulative shipments of XC4000 family FPGA devices exceeded 1 million units. Since its introduction in 1990, the XC4000 family has grown to include fifteen base family members and has been used by over 3000 customers worldwide. Meanwhile, price reductions, feature enhancements, and software improvements are expanding the range of applications addressed by the XC4000's broad product family, and shipments continue to accelerate.

The historic 1 millionth unit was shipped to Oki Electric in Japan. Oki Electric's application exemplifies the inherent power and flexibility of the XC4000 architecture. The XC4000 FPGA is employed in a new telecommunications system; Oki Electric's engineers estimate that use of the XC4000 device allowed them to complete the project in one-fifth the time required for a conventional ASIC approach.

A recent example of the expanding scope of the XC4000 family is the "D" series. This series offers the expansive feature set - except for user RAM - and range of packaging options of the base XC4000 family, but with dramatically lower costs. The newest member of the XC4000 family, the XC4013D has now entered production. (Please contact your local Xilinx sales representative for pricing and availability.) ◆

World's Highest-Density Military PLD

Xilinx recently announced the industry's highest-density military programmable logic device. The XC4013 FPGA is fully compliant with MIL-STD-883B, and gives designers of high-reliability systems new options to reduce cost, weight, and space requirements, while improving system performance and reliability. The XC4013 provides more than 13,000 usable gates and 192 user I/O pins, making it an ideal alternative to gate arrays and full custom ASICs. Xilinx also announced the availability of MIL-STD-883 compliant versions of the XC4003A, the lowest cost high-reliability member of the Xilinx XC4000 family.

"Defense, aerospace and military designers are always eager for the highest-density PLDs available."

"Defense, aerospace and military designers are always eager for the highest-density PLDs available", notes Mitch Richman, product line manager for Xilinx Hi-Rel Products. "With the introduction of the new low price XC4003A and the XC4013 at a record setting 13,000 gates, designers can now take advantage of the benefits of FPGAs in a broader range of applications at a significantly lower cost."

The XC4003A and XC4013 are the latest additions to the Xilinx XC4000 Hi-Rel family, which also includes the XC4005 and XC4010. All Xilinx XC4000 products include unique on-chip system features such as built-in JTAG test circuitry, wide decoders, on-chip RAM, internal tri-state busses and fast carry logic. These features optimize system integration and make the XC4000 family an ideal solution for high-reliability applications where high density, light weight and board space requirements are critical. The in-system reprogrammability of Xilinx FPGAs also provides additional capability and flexibility.

Xilinx is the industry leader in high-reliability PLDs and was the first supplier of full MIL-STD-883 FPGAs. Offering the broadest line of high-reliability PLDs, including erasable programmable logic devices (EPLDs) and FPGAs, Xilinx Hi-Rel products are used in hundreds of military, defense and aerospace programs. Besides MIL-STD-883 versions, SMD (Standard Military Drawing) versions of most products also are available. ◆

New High-Speed Serial PROMs

The XC1700 family of Serial Configuration PROMs has been extended with the addition of the XC17128D and the XC17256D products. These devices are built with our proven, high-reliability EPROM technology, and are designed to mate perfectly with Xilinx SRAM-based FPGA families. The XC17128D device holds 131,072 bits of data, and the XC17256D holds 262,144 bits of data. A single XC17256D PROM can be used to completely configure any Xilinx FPGA up to the XC4013, and multiple PROMs can be cascaded to support multiple FPGAs and/or multiple configurations. These new devices provide significant benefits, including:

- Higher speed: > 12.5 MHz serial access rate
- Low standby current: 50 µA max
- Improved ESD protection

The new XC17128D and XC17256D serial PROMs are available in commercial, industrial and military temperature grades. In addition to the 8-pin DIP and 20-pin PLCC packages, these parts are also available in the new VO8 package, allowing for maximum memory density with minimum space requirements. *(See related story below).*

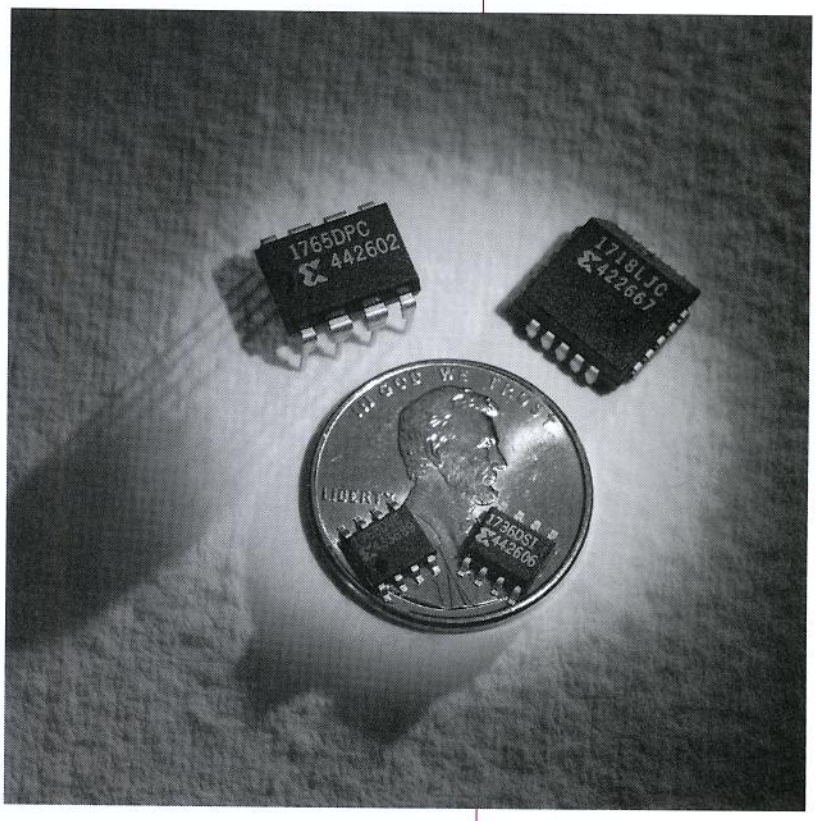
The XC17128D replaces the existing XC17128, and is fully form, fit and system compatible with the XC17128. Migrating to the XC17128D requires only an updated programming algorithm from your programmer vendor.

The XC17256D and XC17128D are in production and shipping now. The Xilinx Serial Configuration PROM is the easiest way to configure your Xilinx FPGA, and with the addition of these new devices, that job is made easier than ever. ◆

New VO8 Package for Serial PROMS

The XC1700 family of Serial Configuration PROMs is now available in the new VO8 package. This new package is only 1/2 the length, 1/2 the width, and 1/4 the height of the standard 8-pin DIP package. It matches the footprint of the existing SO8 package, but is over 30% thinner. PROMs in the new VO8 package are a perfect match for Xilinx FPGAs in VQ packages. Combined, they are the ideal solution for applications with stringent space or weight constraints, such as PCMCIA cards.

The full density range of the XC1700 Serial PROM family is available in the VO8 package, from the XC1718D to the high-density XC17256D. Please contact your local Xilinx sales representative for price, availability, and sample requests. ◆



Xilinx Serial PROMs are available in DIP, PLCC, SO8 and VO8 packages.

XACT 5.1 Enhancement and Update Release

XACT 5.1 adds a number of improvements to the successful XACT 5.0 release. XACT 5.1 updates the full software suite, including FPGA and EPLD implementation tools and third-party interfaces. The XACT 5.1 release includes a limited set of new features, speed grade file updates, and package file updates, as well as solving several problems identified in the XACT 5.0 software.

New features for FPGA development include the following:

- PPR execution times are reduced an average of 30%, through the adjustment of default parameters. However, run times are design dependent, and a few users may not experience this decrease.
- RPM placement using constraints files is allowed.
- Partial constraints for TBUFs and LOCs are allowed.
- Several problems, particularly with the "guide" option and XABEL are fixed.

(For a description of the new features in the EPLD software, please see the article at right)

This article is not intended to be a comprehensive listing of the contents of XACT 5.1; as always, please refer to the release notes contained in the update package.

For the PC, Sun, and HP700 platforms, XACT 5.1 update shipments will begin in December and be completed by the end of January, 1995. Updates will be shipped on CD-ROM media only. However, 3.5" floppy disks are available free of charge for this release, but must be ordered separately; a coupon that can be returned in order to receive 3.5" floppy disks is enclosed in the update package. Apollo, DEC Alpha, and RS6000 users will be updated a month or two later; the media will be tape. ◆

New or Updated Speed and Package Files in XACT 5.1

DEVICE	PACKAGES	SPEEDS
XC73144	BG225, PQ160	-7, -10, -12, -15
XC73108	PQ100	-7
XC7372	PQ100	-7
XC7354		-7
XC7336	PQ44	-5
XC7318	PQ44	-5
XC31xxA		-2
XC3130A	VQ64	-5, -4, -3, -2
XC3164A	TQ144	-5, -4, -3, -2
XC4010D	PQ208, BG225	-6, -5
XC4013	PQ160, PQ208, PQ240	-6, -5, -4
XC4013D	PQ160	-6, -5

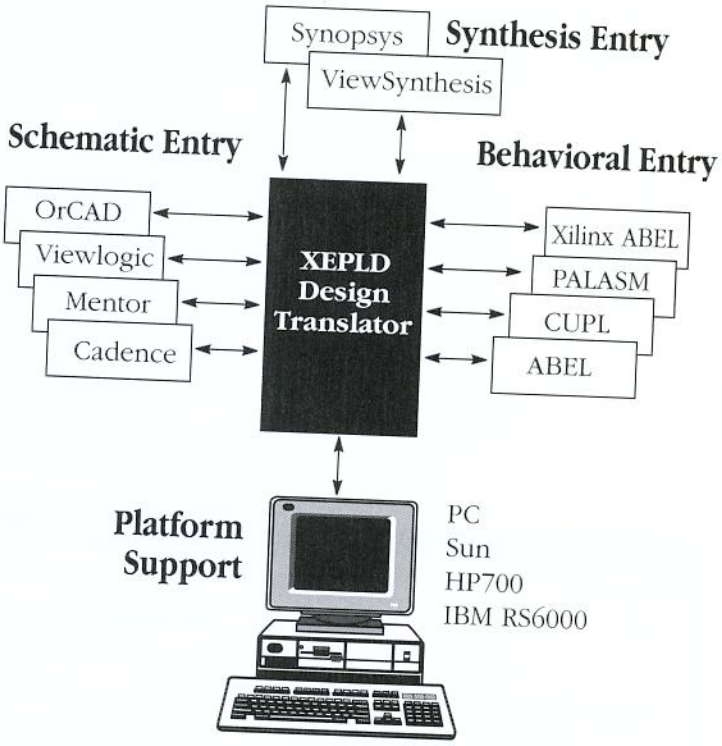
XEPLD v5.1 Advanced EPLD Development Software

XEPLD 5.1, Xilinx's latest EPLD development software, expands on the capabilities of version 5.0 by adding more third-party software support, more behavioral design flexibility and a new Static Timing Report for design verification.

Both new and advanced users will find their productivity increased. New users will find XEPLD 5.1 easy-to-learn and easy-to-use. Automatic optimization features ensure the performance and efficiency of new users' designs. Advanced users can control the optimization and fine-tune every aspect of their designs.

Supported third-party software includes schematic editors and simulators from OrCAD, Viewlogic, Mentor and Cadence. For behavioral design entry, industry-standard PLD compilers such as ABEL, CUPL and PALASM are supported. Synopsys and ViewSynthesis support also have been added.

The PC version is now available for $89.95. ◆



NEW FEATURES

VHDL and Verilog HDL Synthesis Support — Third-party software support has expanded to include two new tools: Synopsys and ViewSynthesis. Both tools support behavioral design synthesis using the VHDL language; Synopsys also supports the Verilog HDL language. Both tools offer functional and timing simulation of synthesized designs.

Static Timing Report — A new XEPLD translator report gives you precise timing information for your fitted design:

- Combinatorial pad-to-pad delays
- Setup-to-clock times
- Clock-to-output delays
- Cycle time

You can use this information instead of or in addition to timing simulation.

Vector Notation and Nested Parentheses in PLUSASM — PLUSASM now supports vector notation and nested parentheses, which add tremendous flexibility to how you can enter designs in a behavioral environment.

Explicit Placement of Logic in the UIM® — the SMARTswitch™ feature of the XEPLD software automatically uses the inherent logic capability of the UIM whenever possible to reduce macrocell requirements and increase speed. Now you can explicitly place logic in the UIM to fine-tune logic optimization.

XACT 5.1 Ends the "Floppy Shuffle"

With XACT® 5.1, targeted for release in 4Q94, Xilinx PC software products, including updates, will be delivered only on CD-ROM media (with the exception of the individual EPLD Core product: DS-550-PC1).

Current in-warranty floppy disk customers will be able to request 3.5" media supplements free of charge by returning a card included with your update. But why not make the move to CD-ROM now? Think of all the time you'll save.

With future releases, 3.5" media will be available only at an additional charge, so now is the time to get your drive. Drives are cheaper than ever and it's easy to justify a CD-ROM drive purchase; CD-ROM technology saves time and money in the following ways:

- **Simpler and Faster Software Installation** — Don't waste time feeding up to 60 floppies into your PC. CD-ROM software installation is quick and easy, saving man-hours of your time.
- **Lower Support Costs** — With your next support renewal, your support costs will be less than they were with floppy disk media. With the savings you get, the drive can practically pay for itself.
- **Simple Software Management** — All software for each platform comes on just one disk, ensuring software version compatibility. With CD-ROM, it's also simple to archive and retrieve your design environment.

"With future releases, 3.5" media will be available only at an additional charge, so now is the time to get your drive."

- **New Product Evaluations** — With XACT 5.1, any user with a Xilinx key can evaluate Xilinx X-BLOX™ and XABEL™ products. Fifty trial invocations are allowed. Unlimited use of these products can be fully authorized over the telephone upon purchase.
- **Latest Application Notes** — Xilinx application notes with design files are on the CD to help you incorporate expert techniques into your own designs.
- **(Future) Execute XACT on PC Directly from CD** — With future updates, you will be able to execute PC software directly from the CD, saving hard disk space and installation time.
- **(Future) On-line Documentation** — Also in the future, Xilinx documentation will be on-line with full searching capabilities, permitting fast access to the information you want.

Plus, owning a CD-ROM drive will give you access not only to the latest Xilinx features, but to thousands of other CD-ROM distributed applications as well. CD-ROM makes sense.

Xilinx CD-ROM media meets ISO 9660 standards, making it compatible with most standard CD-ROM drives.

To purchase a CD-ROM drive, contact your local dealer. In the U.S., CD-ROM drives can be purchased from your local Xilinx distributor; orders can be placed over the telephone. ◆

Flow Manager and Improved Synthesis in PRO Series 6.0 available 1Q95

Xilinx will begin to ship the PRO Series Windows software from Viewlogic to all in-warranty Viewlogic customers in 1Q95. All new customers will automatically receive PRO Series 6.0.

What is PRO Series 6.0?

PRO Series 6.0 is Windows 3.1 based software that includes all the tools in Workview 4.1 in a Windows environment. These tools are:

- PROcapture- schematic entry
- PROsim- simulation
- PROwave - waveform entry and display
- PROsynthesis - VHDL simulation

PRO Series 6.0 Features

The new features in PRO Series 6.0 include:

- PRO Series Flow Manager with Xilinx software integration
- PROsynthesis 3.0 (DS-VLS-EXT-PC1 package only)
- Two-button mouse support
- Windows tool bar
- Tool Tips
- Windows menus
- Window tiling - multiple open windows

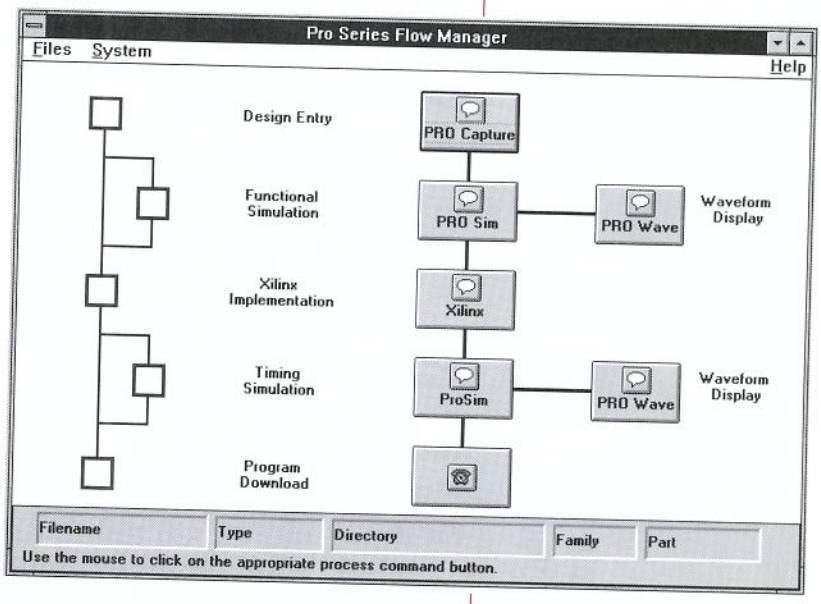
PRO Series Flow Manager

The PRO Series Flow Manager manages the design flow for both schematic and synthesis design entry. Xilinx worked with Viewlogic to integrate the Xilinx implementation software into the PRO Series Flow Manager. The result is an easy to use flow that automatically invokes all the necessary tools without ever having to leave the PRO Series environment. Moreover, the Xilinx software is accessed through a set of specially designed GUIs that simplify the specification of options. The Flow Manager supports all the Xilinx EPLDs and FPGAs.

PROsynthesis 3.0

A new version of the Viewlogic synthesis tool will be released 1Q95, PROsynthesis 3.0. This version has many Xilinx specific features that increase utilization by 22% over the previous version. The following Xilinx specific features are included in this release:

- CLB Mapping for the XC3000 and XC4000 Xilinx FPGAs
- XACT-Performance support
- Library support for the XC7000 and XC8000 families
- Improved optimization algorithms



All Xilinx customers with Viewlogic Stand-alone Extended packages will be updated with PROsynthesis 3.0. This version is also available from Viewlogic as ViewSynth/FPGA v3.0.

Viewlogic gave Xilinx a sneak preview of PROsynthesis v 3.1. Benchmark results showed improvements of 46% over the current version of PROsynthesis v2.3.1. This version will be available 2Q95. ◆

Cadence Scores High on XACT 5.0 Solution

Cadence recently completed beta testing of the new Xilinx solution that incorporates XACT 5.0. The new software is included in this quarter's release of the Cadence system.

The Xilinx solution was redesigned from the ground up. Considerable effort was spent in understanding the steps a user takes in developing a system that includes Xilinx FPGAs/EPLDs. The end result is a solution that allows a user to enter the design description in an HDL (Verilog or VHDL), schematic, or a mixture of both, implement it in FPGAs, and obtain all the information needed for board-level verification.

"The graphical representation of each step easily guides the user through the design process. Options for each step are selected from easily explained forms."

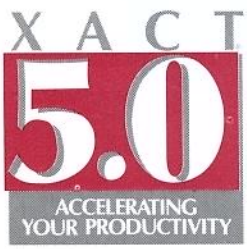
During the beta test period, several partners (including Acuson, Mistibushi, Motorola, and Thomson) worked closely with Cadence to ensure that the product was configured correctly for the system designer. The beta sites were impressed with the methodology, quality, and usability of the solution.

Features of the new release include:

- **Direct translation of netlists:** Netlist creation for XNF and Verilog is now a single processing step, eliminating the need to translate to EDIF first. This makes the process faster, and eliminates problems involved with mapping signal names across multiple netlists.
- **Synthesis support:** As designs become more complex, synthesis plays a larger role in design entry. The interface is constructed so that the user can synthesize all or part of the design and still use the same process flow. A new, oprtimized synthesis engine yields high quality results.
- **On-line documentation:** Design groups often share one or two copies of the XACT documentation. Over time, manuals may be misplaced or lost. Cadence has integrated all the XACT documentation into Openbook so that each user has access to an on-line copy of the manuals.
- **Icon-driven design flow:** New users often find themselves overwhelmed by the process flow for designing with FPGAs. The graphical representation of each step easily guides the user through the design process. Options for each step are selected from easily explained forms.
- **Processing of multiple FPGAs:** Board designs usually include several FPGAs. Incremental changes on a board typically include moving a block of logic from one FPGA to another. The interface can process multiple FPGAs, generating XNF files for the changed schematic sheets, and calling XMAKE with the guide option for each device — all with a single command.

All Cadence users will receive the new solution as part of the Cadence 9404 CD-ROM release.

To request an early copy, contact Jim Young, Cadence
(Tel: 408-944-7734
E-mail: jimby@cadence.com). ◆



A PCI Bus Primer

A personal computer system bus moves microprocessor data to and from peripherals such as disk drives, monitors and printers. The most successful of these have been the 16-bit Industry Standard Architecture (ISA) bus established by IBM for the "AT-class" PC, and its 32-bit successor, the Extended Industry Standard Architecture (EISA).

The capabilities of new high-speed microprocessors such as Intel's Pentium processor and the high data-throughput requirements of applications such as graphics and video processing have quickly exceeded the data transfer capabilities of these standard system busses. To avoid data transfer bottlenecks on the system bus, many computer systems now include a direct path between the processor and its high-speed peripherals, bypassing the main system bus. Because the main system bus is needed to support existing add-in cards, systems now often contain a hierarchy of busses.

New terminology describing this bus hierarchy has evolved. The "system bus" is the main backplane of the system with connector slots for add-in cards; examples include the ISA, EISA, MCA (Micro Channel Architecture), and PCMCIA busses.

A "local bus," on the other hand, is a direct component-to-component interface between processors and high-speed peripherals. Local busses are designed to bypass the system bus and rush data to and from high-speed peripherals resident with the CPU on the motherboard.

A "mezzanine bus" is a local bus that runs through a connector slot, establishing a motherboard-daughterboard relationship. Interfaces between the various busses are referred to as "bridges."

Figure 1 illustrates a typical example; a local bus connects the processor to high-speed graphics and disk controllers resident on the motherboard, with bridges connecting to other busses.

The specifications of the popular Peripheral Component Interconnect bus (PCI) is controlled by the PCI Special Interest Group (PCI SIG), although it was originally defined by Intel. Xilinx is an active member of the PCI SIG. Actually, PCI is not a true local bus, in that it connects to the processor via a bridge.

The PCI SIG has defined various connector slot specifications to form PCI-based mezzanine busses. A system bus definition is in place, with up to three add-in card slots per system. The market for PCI-compatible components and boards is poised for explosive growth, with endorsements from many major PC and workstation manufacturers.

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

PCI Electrical Specifications

The goal of the PCI bus is to provide high data throughput on a well-defined, lightly loaded, short bus using technology compatible with today's mainstream IC manufacturing processes. It supports a maximum transfer rate of 33 MHz over a 32- or 64-bit data path (33 MHz transfers of 32-bit data = 132 MBytes/second).

The PCI bus is complex and functions differently from other busses. It is unterminated, operating on the principle of reflective wave signaling. The output impedance of a device driving the bus is roughly matched to the

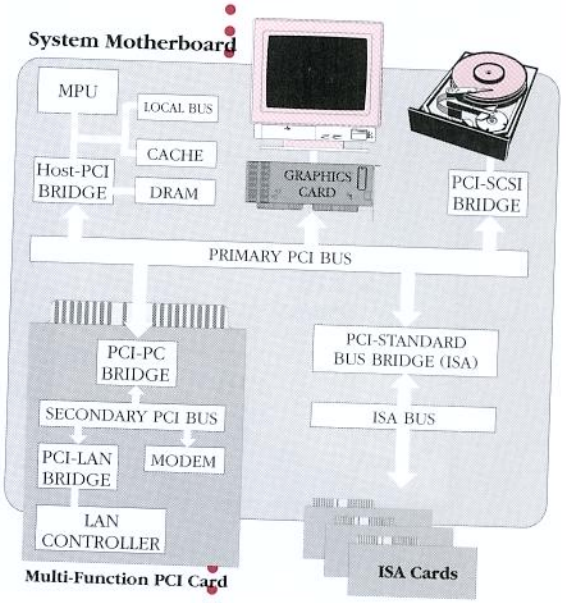


Figure 1: PCI System Block Diagram

XILINX®

PCI PRIMER

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characteristic impedance of the bus (a transmission line). The initial output signal, therefore, has half amplitude. This signal travels to the end of the non-terminated bus, and gets reflected back towards the source to become a full-amplitude signal. During the round-trip time, a level may exist on the bus that is between a legal logic one and zero, lasting longest for the receiver that is located closest to the driver. In order to achieve 33 MHz, the round-trip delay must be limited to 10 ns, limiting the physical length and allowable capacitive loading of the bus.

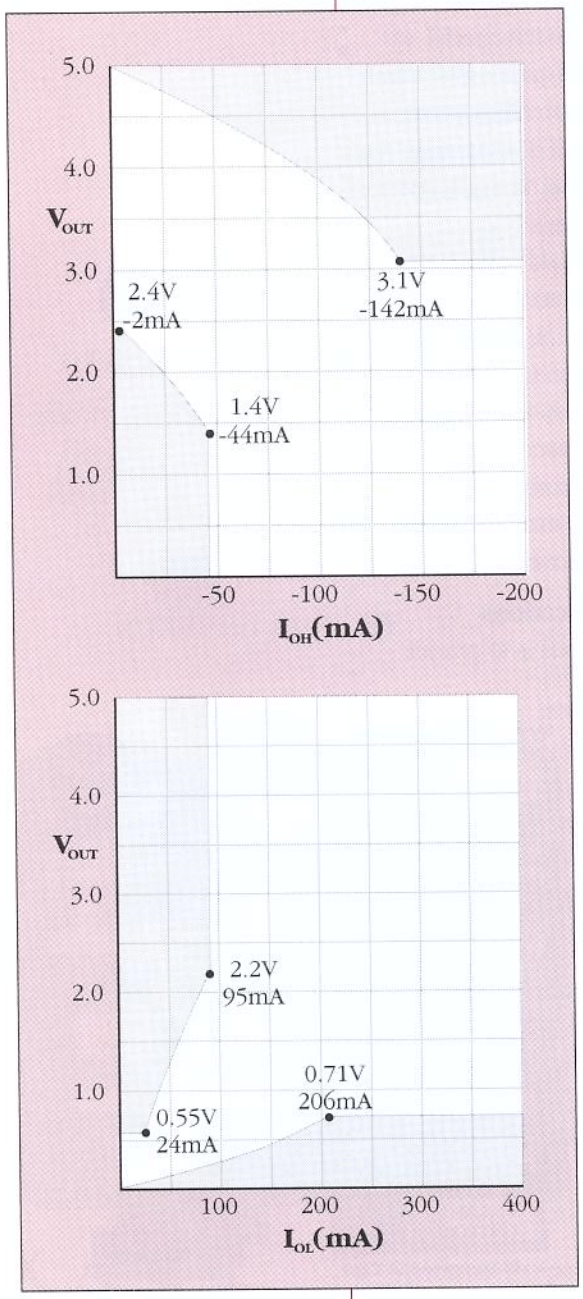


Figure 2: 5V PCI Output I/V Curve Limits

This scheme demands strict control of device drive characteristics. The driver must have an output impedance in both the High and Low states that is roughly the same as the characteristic impedance of the driven bus. When that condition is met, the outgoing signal has half amplitude, and the returning signal is absorbed without any further ringing or reflection. *(See the 1994 Xilinx Data Book, page 9-28.)*

Thus, unlike traditional bus specifications, PCI defines AC switching characteristics as well as DC parametrics. In other words, as well as specifying I/O sink and source limits at logic 0 and 1, PCI also includes specifications for sink and source switching currents across the transition from one logic level to another. These are specified as regions and specific points on a current vs. voltage graph (or "I/V curve"); Figure 2 shows the I/V curve limits for the 5 volt signaling environment. A device is considered compliant if its I/V curve does not cut into a shaded region. (The curves are drawn in an unorthodox way — voltage as a function of current, while IC manufacturers generally show current as a function of voltage — but the intent is clear.)

The PCI standard includes specifications for both 5 V and 3.3 V signaling environments to provide for "quick and easy transition from 5 V to 3.3 V component technology." PCI subsystems can be 5 V only, 3.3 V only, or universal (both). A keyed connector scheme prevents damage to single voltage cards.

PCI I/O requirements are stringent. Table 1 summarizes four key parameters. These parameters relate to bussed signals, and are more stringent than the point-to-point timing specifications. The 30 ns clock period allocates 11 ns for the output driver, 10 ns for the round-trip bus propagation delay, 2 ns for potential clock skew, and 7 ns for input set-up time.

Sym.	Parameter	PCI Limit
T_{SU}	Input Set-up Time	7 ns
T_{H}	Input Hold Time	0 ns
T_{VAL}	Clock to Valid data out	$2\text{ ns} \le T_{VAL} \le 11\text{ ns}$
T_{ON}	Float to Active delay	$2\text{ ns} \le T_{ON} \le T_{VAL}$

Table 1: Key I/O Timing Parameters

Bus loading must be strictly controlled in order to maintain performance. Rule-of-thumb guidelines for PCI allow 10 electrical loads on the bus. A direct silicon interface counts as one load; add-in cards count as two. Each add-in card edge-connector finger can attach to only one device pin of no more than 10 pF, except for the CLOCK pin which can be 12 pF. Exceeding any of these load limits requires a PCI-PCI bridge for a fully compliant system.

The PCI SIG has published the *PCI Compliance Checklist* of parameters that both system and component suppliers must adhere to in order to claim compliance. It includes a *Component Electrical Checklist* of 52 Component Electrical (CE) items for integrated circuits. They are grouped into sections, not all of which necessarily apply to every device.

- CE1-17: *5V Signaling* - DC characteristics for 5V signaling environments.
- CE18-34: *3.3V Signaling* - DC characteristics for 3.3V signaling environments.
- CE35-38: *Loading and Device Protection* - Pin capacitance and ESD protection.
- CE39-50: *Timing Specification* - Clock, AC and timing parameters.
- CE51-52: *64-Bit Components* - 64-bit architecture-specific issues.

It is important to review this checklist for any device that will connect directly to the PCI bus. By responding to the appropriate items in this checklist, a vendor demonstrates he has done the minimum amount of work required in order to claim compliance. Inability to furnish a response to this checklist is sufficient reason to question both familiarity with the PCI specification and any claims of compliance. However, while meeting the checklist criteria is necessary, it does not in itself guarantee PCI compliance. Full system-level compliance typically is verified by actually building a board and testing it. Also, models available from Logic Modeling Corp. (a division of Synopsys) have been sanctioned by the PCI SIG for testing a design for compliance.

PCI and Programmable Logic

Traditionally, I/O interfacing and control has been the most popular application of programmable logic in computer systems; this trend is expected to continue for PCI-based applications. With high-density programmable logic, the computer bus-to-I/O interface can be implemented on the same programmable device as the customized I/O control logic, providing for a high integration level and all the resulting benefits, including high performance, small size, and low power consumption. Other popular applications include PCI-to-standard bus bridges and PCI-to-PCI bridges.

While many programmable devices can claim some measure of "PCI-compatibility," complete compliance to the PCI electrical signaling specifications is a difficult goal. For programmable logic to be compliant, it must have robust output drivers and be able to meet the stringent timing requirements set forth in the specification. Some programmable devices come very close, but don't quite meet the specification. Manufacturers of those products like to use terms like "PCI-compatible" or "PCI-friendly", but in order to be fully compliant, programmable logic devices must meet all the specifications included in the *PCI Compliance Checklist*, as a minimum.

"Meeting the checklist criteria is necessary, it does not in itself guarantee PCI compliance. Full system-level compliance typically is verified by actually building a board and testing it."

The determinate timing of most EPLDs makes it a fairly straightforward task to examine the device's AC timing parameters in the data sheet and determine if that device meets the PCI timing specifications.

Determining an FPGA's compliance to these specifications is more difficult. The clock-to-output and three-state enable-to-output timing specifications are particularly problematic in FPGA-based designs, where global buffer and interconnect delays as well as logic delays must be taken into account.

A clock-to-output valid delay of under 11 ns is difficult to guarantee in large FPGA devices, where it may take 6 to 8 ns to distribute the global clock signal to every flip-flop on the chip. Remember, the PCI standard specifies pin-to-pin timing, so the clock-to-output valid delay typically would include the delay in inputting the clock signal, bringing it to the

PCI PRIMER

Continued from previous page

FPGA's global clock buffer, routing the clock to the relevant I/O or logic block, and the delay through the output buffer driving the register's output signal to the external pin. Currently, Xilinx is the only FPGA manufacturer that includes these types of pin-to-pin timing parameters in FPGA data sheets *(for example, see page 2-51 of the 1994 Xilinx Data Book for the XC4000 pin-to-pin timing);* inclusion in the data sheet means that these parameters are measured and tested in each device and guaranteed by Xilinx.

Keeping clock-to-output active (after three-state) delays under 11 ns also is difficult to meet in architectures where the output enable signal must be driven from internal logic and not from a dedicated flip-flop. Fortunately, a design "trick" can alleviate this problem; the output enable line can be driven active on the clock edge one-half bus cycle before the actual data transfer.

The maximum input set-up time is 7 ns, and the hold time must be zero. The combination of these two parameters also can be problematic in programmable logic devices. Internal to the device, flip-flops typically have short 2 to 5 ns set-up times and zero hold time. But these internal parameters are defined with respect to an internal clock; the PCI standard specifies pin-to-pin timing with respect to the system clock. The internal clock inevitably is delayed with respect to the signal being input on the clock pin. Thus, any delays on the clock signal between the external pin and the internal flip-flop must be subtracted from the internally specified set-up and hold time values. Without special precautions, the set-up time becomes either very short — which is good — or it becomes negative — which is unacceptable. The hold time moves in the same direction, inevitably violating the PCI specification. The only way to be compliant is either to reduce on-chip clock distribution delay to nearly nothing (an impossible goal) or to compensate for the clock delay by deliberately delaying the data input signals. This is what the XC3000 and XC3100 families offer as a standard feature, and the XC4000 family offers as a programmable option. Other FPGA manufacturers do not offer this feature; they have to compensate for the clock delay with vaguely specified data routing delays. The lack of minimum delay specifications or information about on-chip delay tracking make this a dangerous gamble for the designer.

> *"Unlike traditional bus specifications, PCI defines AC switching characteristics as well as DC parameters."*

Limiting the capacitive load at each card to 10 pF means that each signal can be connected to only one device pin. Data sheets often list an input capacitance of 15 pF, but this higher value only applies to ceramic packages where the multi-layer construction increases pin capacitance.

As described in *XCELL* issue 14, the XC7300 EPLD family is the first Complex PLD family that is fully-compliant with the PCI specification. *(Also see page 17 in this issue for a related article.)* An application note entitled "Designing Flexible PCI interfaces with Xilinx EPLDs" also is available. Fully-compliant Xilinx FPGAs include the XC3100A family (-2 speed grade) and some members of the XC4000 family (in certain situations). The *Component Electrical Checklist* has been completed for the XC7300 EPLD family and the XC3100A FPGA family and submitted to the PCI SIG. An article about PCI-compliant FPGAs is planned for the next issue of *XCELL.*

For more details regarding the PCI specification, contact the PCI Special Interest Group:

PCI Special Interest Group
M/S HF3-15A
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
Tel: 503-696-2000 ◆

Using XACT-Performance

A major feature of XACT 5.0® is XACT-Performance™, which permits designers to specify the maximum allowable delay between user-defined end-points. Prior to version 5.0, only less-precise "path-type" timing requirements could be specified.

The point-to-point control of XACT-Performance 5.0 can be accomplished in two simple steps:

1. Identify and define groups of related path end-points, using TNMs or TIMEGRPs.
2. Specify path delay from one group to another, using the from:group1:to:group2 syntax.

End-point specifications are the only way to assign timing requirements on paths that start or end at RAMs or input latches.

Defining End-points

To refer to a group of flip-flops, input latches, IOB pads, or RAMs, use the corresponding key words: FFS, LATCHES, PADS, RAMS. Alternatively, an TNM (timing name) identifier can be assigned to a group of specific symbols (e.g. 8 flip-flops in a 8-bit counter), creating an arbitrary group:

```
TNM=group or
   TNM=[predefined_group]:group
```

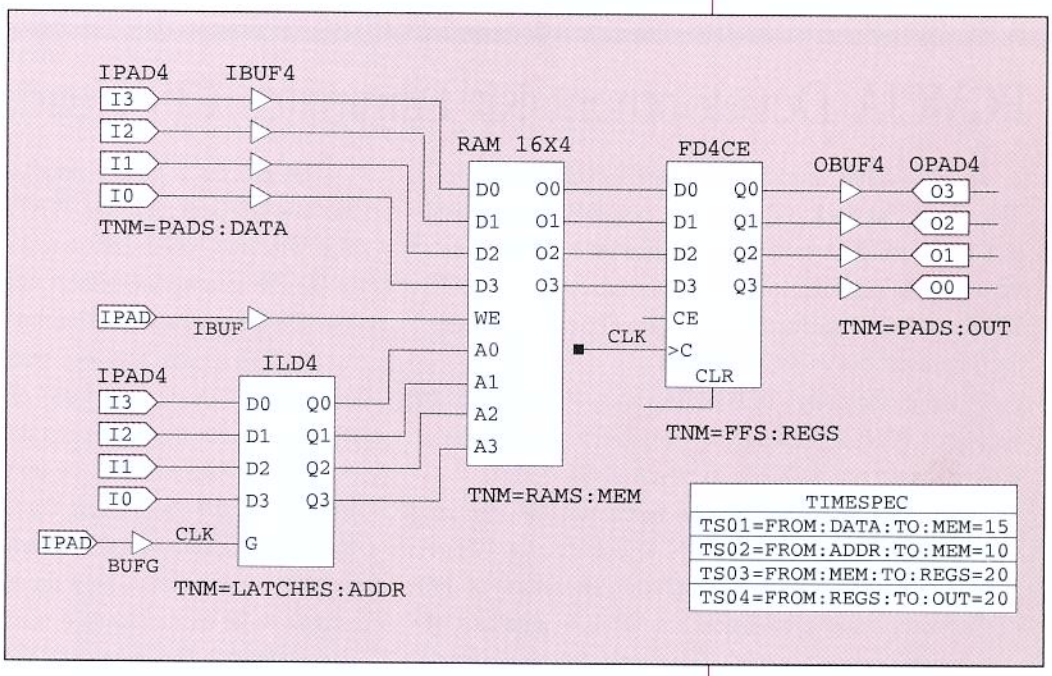
Additional groups that are combinations of existing TNM groups can also be defined with the TIMEGRP symbols. Together the predefined groups (FFS, LATCHES, etc.) and your TNM/TIMEGRP groups can be used as the end-points for the Timespec "from-to" timing specifications.

From-To Statement Syntax

To specify timing requirements between specific end-points, use the following syntax within the TIMESPEC primitive on the schematic:

```
TSidentifier=
   FROM:group1:TO:group2=delay
```

The parameters group1 and group2 must be the predefined groups, previously created TNM identifiers, or groups defined in TIMEGRP symbols. The delay parameter defines the maximum delay for the attribute. Nanoseconds are the default units for specifying delay time in TS attributes. Alternatively, you can place TS attributes containing the from-to statements in the PPR constraint file *(see related article on page 32)*.



The above example illustrates the basic methodology of specifying timing constraints in a schematic design. For more detailed information regarding XACT-Performance 5.0, please consult the XACT-Performance section of the XACT Reference Guide and the XACT-Performance and Xdelay Tutorial in your Viewlogic/Mentor/Orcad Interface User Guide. ◆

XACT-Performance™ Makes

A central feature of the Xilinx XACT® Development System is XACT-Performance™. Using XACT-Performance, the designer annotates the logic design with timing specifications that not only convey the speed objectives, but also enable the software to make intelligent trade-offs when allocating FPGA resources.

The following simple example illustrates a typical resource-allocation trade-off. Prior to XACT-Performance, the software would have made a pre-programmed choice, or the user would have had to control the routing manually. With XACT-Performance, the appropriate choice is made automatically.

Application Note XAPP023, *Accelerating Loadable Counters in XC4000*, describes a 32-bit counter that is divided into 10- and 22-bit sections (*1994 Xilinx Programmable Logic Data Book*, page 8-82). When the less significant 10 bits reach their terminal count value, an enable signal (CEP) is generated that enables the more significant bits of the counter for one clock cycle. This enable signal is in the critical path, and it is, therefore, connected in parallel to the clock-enable pins of all the more significant flip-flops.

Figure 1 shows portions of an XC4000 Configurable Logic Block (CLB). The flip-flop Clock Enables (EC) can be reached

PCMCIA Development Kit Eliminates CIS Headaches

In 1992, Xilinx introduced the first FPGA products in Thin Quad Flat Packs (TQFPs) and began supplying products to the PCMCIA card market. Since then, Xilinx has expanded its portfolio to include more than 20 devices in TQFP and VQFP packages, and Xilinx FPGAs have been used in numerous PCMCIA designs.

To aid in the design of PCMCIA cards, Mobile Media Inc. supplies a PCMCIA Prototyping Card and a "CIS Generator" product based on the Xilinx XC3042A FPGA device.

The PCMCIA standard requires that a variable amount of memory be included on each card to hold the Card Information Structure (CIS). The CIS informs the system of the card's function and capabilities. The CIS is a linked list of data frames known as tuples. Each tuple describes some aspect of the card's functionality. For example, a PCMCIA memory card would have tuples describing the memory type, size, organization, address range, and similar data.

One of the biggest problem designers face today is the design and implementation of the Card Information Structure (CIS). Many PCMCIA designers today assemble the tuple information "by hand," a painstaking and error-prone process. Verification that the CIS is constructed correctly involves placing the tuples in memory on a card and testing the card with various Card and Socket Services for compatibility and correctness.

This process is greatly simplified with Mobile Media's CIS Generator and PCMCIA Prototyping Card. The Windows-based CIS Generator turns construction of the CIS information into a push-button operation. The CIS Generator is a CIS entry and synthesis tool for PCMCIA tuples. The user selects the card's attributes from menus and icons on the screen, and the binary code for the tuples is automatically generated.

This CIS data can then be downloaded into memory on the Prototyping Card. The control logic for the card can be implemented in the FPGA. This flexible combination allows the logic and tuple information to be easily changed while experimenting with different approaches and verifying the final design. The Prototyping Card can be inserted into various host sockets for testing prior to committing to the final design.

Mobile Media manufacturers and markets a complete line of PCMCIA products. Both the CIS Generator and PCMCIA Prototyping Card are available from:

Mobile Media Inc.
1977 O'Toole Ave., Suite B-207
San Jose, CA 95131
Tel: 408-428-0310 • Fax: 408-428-0379 ◆

Right Trade-Offs

through any of the four CLB control pins, C_1, C_2, C_3 or C_4. One of these control pins resides on each side of the CLB.

Since the counter sections exploit the dedicated carry logic, they are organized in CLB columns. Consequently, CEP is best routed on a vertical Longline connected to C_1 or C_3.

The counter also has an asynchronous clear that uses the Set/Reset pins of all the flip-flops. Like EC, the flip-flop Set/Resets (SR) are reached via the CLB control pins, and like CEP, the Clear signal is, therefore, best routed on a vertical Longline. This situation leads to competition for the C_1 and C_3 pins.

Two solutions are shown in Figure 2. In Figure 2a, a single Longline is used for Clear. This runs between the two CLB columns, and conveniently connects to the CLBs on either side. The CEP Longline also connects to its column of CLBs, but it is on the wrong side of the column, away from its source, resulting in unnecessary delay. CEP cannot be efficiently routed between the columns, since the C_1 pins are already used for Clear.

In the second solution, Figure 2b, CEP is routed between the columns and uses the C_1 pins. With this routing, the counter is slightly faster because of the shorter CEP path. The speed is achieved, however, at the expense of using two Longlines for Clear, one of which might be needed for other purposes.

Which solution is better? Neither. Both are good; each has its advantages and disadvantages. The choice depends entirely upon the performance requirements of the design. Every time this counter design is used and a timing specification is included, XACT-Performance will automatically make the appropriate trade-off.

This is a fairly trivial example. It does, however, illustrate how XACT-Performance timing specifications enable the software to expend additional resources only when they are needed, conserving them for other uses when they are not. In a full design, the trade-offs are much more complex, and making these trade-offs intelligently is essential if the FPGA resources are to be used effectively. ◆

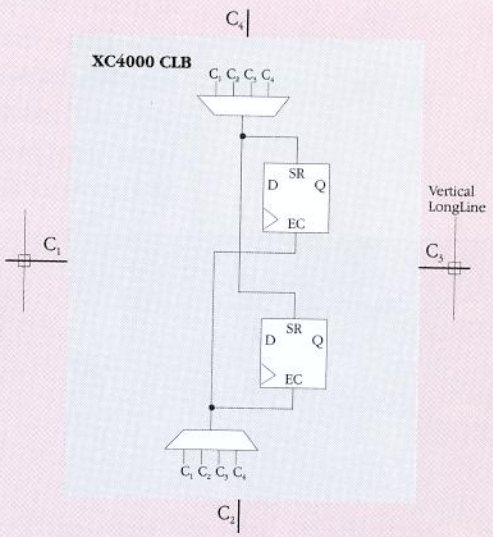


Figure 1: XC4000 CLB Control Pins

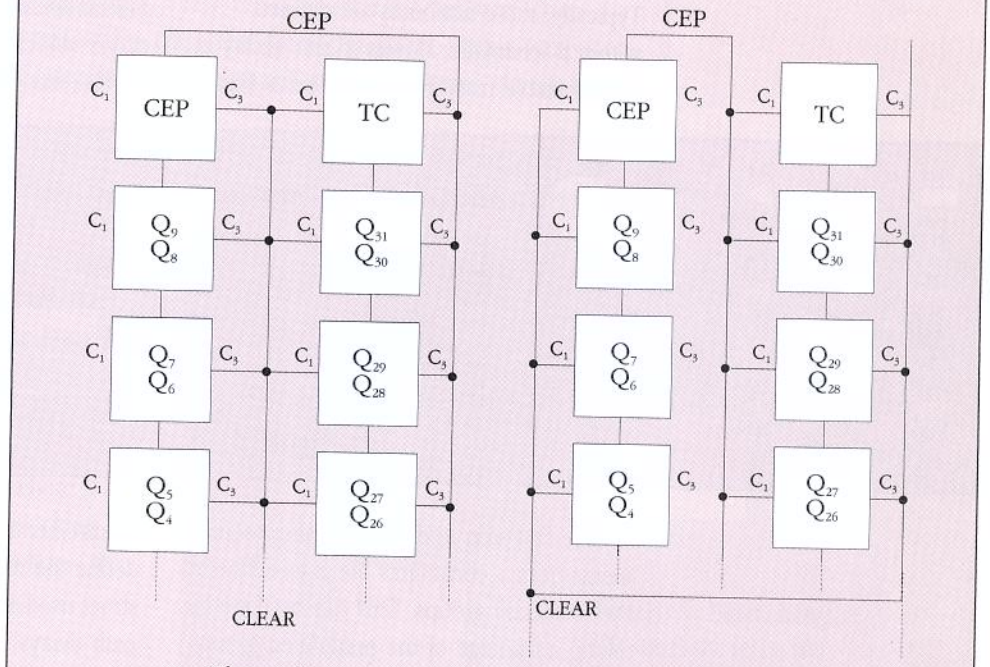


Figure 2a **Figure 2a**

Two Routing Schemes

Setting Performance Requirements in a Constraints File

XACT-Performance™ 5.0 allows users to specify very precise timing requirements for a design. Using the "point-to-point" approach, users define a start point, an end point, and the delay requirement between the two points. Valid points can be any one of the predefined groups, FFS, PADS, LATCHES, or RAMS. Additionally, users can define arbitrary groups within a predefined group by tagging symbols with TNM (pronounced *tee-name*) attributes. Once all the necessary groups are defined, timing requirements between groups can be specified by defining a TS attribute. Typically, these attributes are defined within a schematic. However, this ability is also available from a text constraints file.

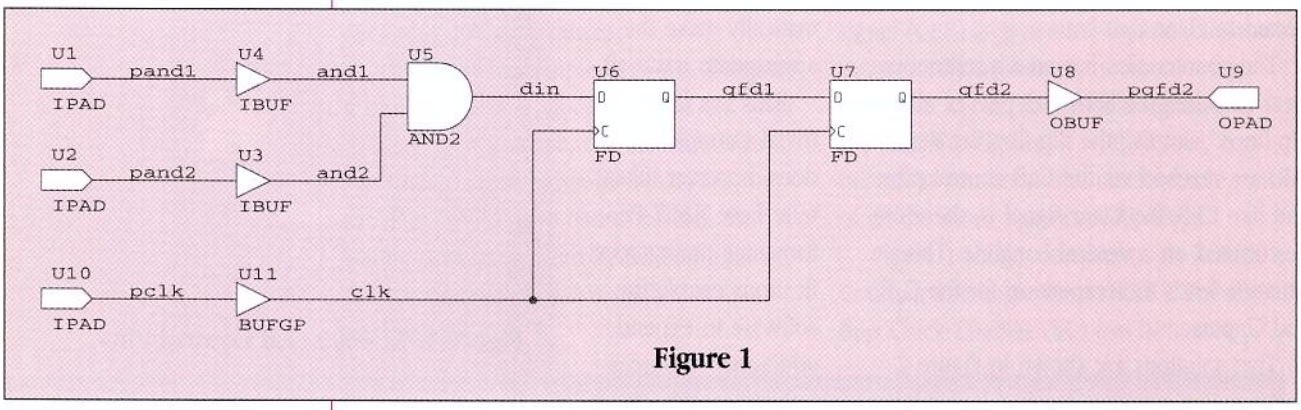


Figure 1

The first step in defining timing requirements from a constraints file is to define all the necessary groups. This can be done by taking advantage of the predefined groups and knowledge of the net names connected to the symbols' output. The construct used in a constraints file to define a new group is:

```
TIMEGRP=
"newgroup=existing_group(net_
name_pattern)";
```

where *newgroup* is the name of the group being defined, *existing_group* is a defined group (user defined or predefined), and *net_name_pattern* is a string to identify the output net names attached to the desired symbols. *net_name_pattern* may contain asterisks (*) to represent any character string and question marks (?) to represent a single character. *net_name_pattern* must account for the full hierarchical net name either explicitly or via wildcards.

The second step in defining timing requirements from a constraints file is to define the required path delays. The construct used in a constraints file to define path delays is:

```
TIMESPEC=
"TSid=FROM:group1:
  TO:group2=delay";
```

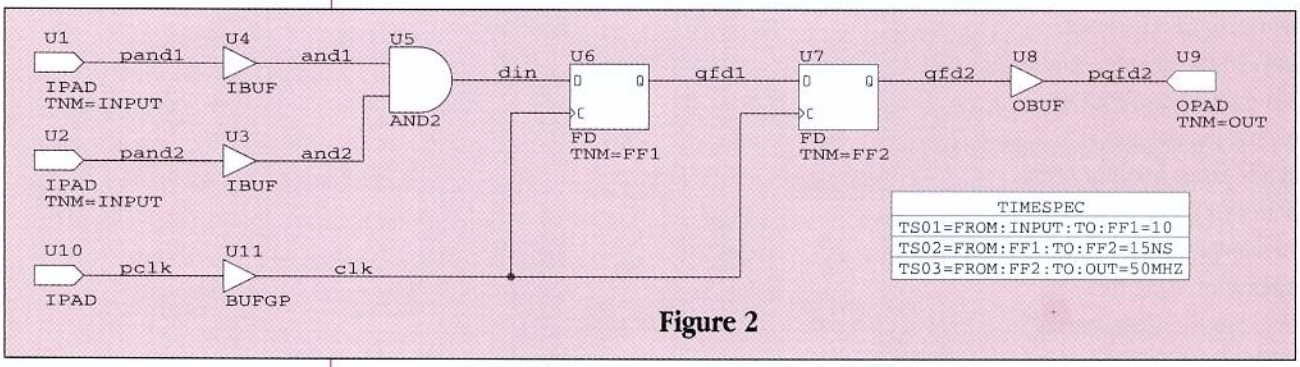


Figure 2

where **TS***id* is a unique timespec identifier, *group1* is the start point, *group2* is the end point, and *delay* is the required maximum path delay. Nanoseconds are the default units for *delay*, but users may specify NS (nanoseconds), MHZ (megahertz), US (microseconds), or KHZ (kilohertz).

After the constraints file has been created, the information can be pulled into the design by running XNFPREP on the flattened design netlist (design.XFF). XNFPREP will add the information to the output design netlist (design.XTF or design.XTG). Figure 1 is a sample schematic without any timing requirements specified. When Figure 1 is processed with the constraints file at right, it is equivalent to processing the schematic of Figure 2 which contains timing requirements.

```
TIMEGRP="INPUT=PADS(PAN*)";
# assign IPADs U1 and U2 to group INPUT
TIMEGRP="FF1=FFS(QFD1)";
# assign FD U6 to group FF1
TIMEGRP="FF2=FFS(?FD2)";
# assign FD U7 to group FF2
TIMEGRP="OUT=PADS(?QF*)";
# assign OPAD U9 to group OUT
TIMESPEC="TS01=FROM:INPUT:TO:FF1=10";
# define 10ns max delay between INPUT and FF1
TIMESPEC="TS02=FROM:FF1:TO:FF2=15NS";
# define 15ns max delay between FF1 and FF2
TIMESPEC="TS03=FROM:FF2:TO:OUT=50MHZ";
# define 50MHZ max delay between FF2 and OUT
```

For further details about XACT-Performance, please refer to the XACT 5.0 Reference Guide, Vol. 1, page 1-69. ◆

Clock Enables for Output Flip-Flops

Xilinx XC3000 and XC4000 family FPGAs have dedicated output flip-flops located in the peripheral Input/Output Blocks (IOBs). These flip-flops offer the fastest clock-to-output delay for data that is routed off the chip. The pin-to-pin global clock-to-output delay is fully characterized and guaranteed. The output flip-flops, however, do not have clock-enable controls.

The circuit in Figure 1 uses half of an adjacent CLB to emulate the clock enable function in the IOB output flip-flop. The clock-enable function is provided without affecting the output flip-flop performance.

While the clock is enabled (EN High), the multiplexer routes data to both the output flip-flop and the CLB flip-flop. When the clock is disabled, the multiplexer creates a hold loop around the CLB flip-flop and its data is retained. This captured data is also routed to the output flip-flop, where it is continually clocked in, thus mimicking a hold function in the output flip-flop. ◆

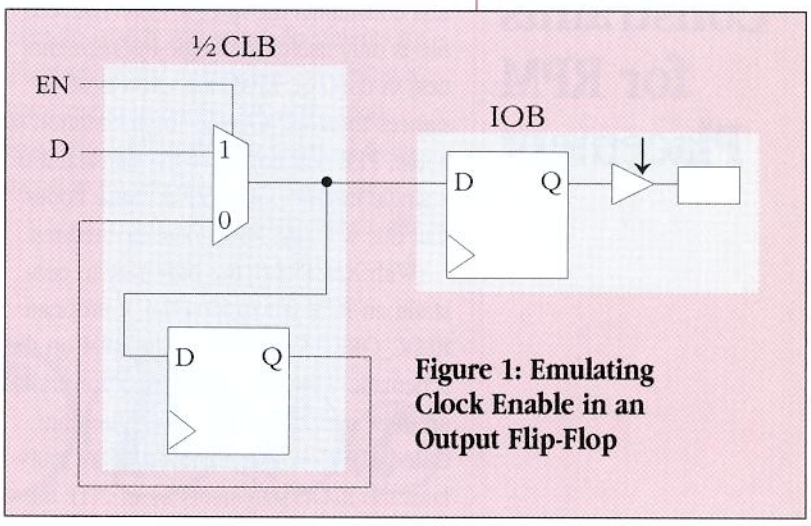


Figure 1: Emulating Clock Enable in an Output Flip-Flop

Timing Report for EPLDs Now Available

The new Static Timing Report Generator available in XEPLD 5.1 makes verification of Xilinx EPLD designs easier than ever by providing complete timing analysis.

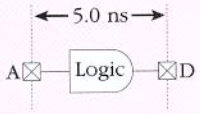
Enter the command TIMERPT after a design has been completed and a worst-case timing report will be calculated and printed in an easy-to-interpret format for:

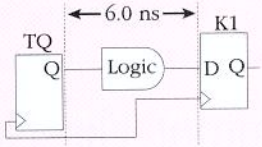
- pad-to-pad delays
- setup-to-clock timing
- clock-to-output delays
- cycle time and max. clock frequency

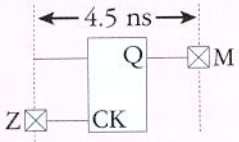
A stand-alone development tool for Xilinx EPLDs, XEPLD 5.1 can be used with a variety of third-party tools for schematic entry and timing simulation *(see page 21).*

For more information, contact your Xilinx representative or call the Xilinx hot line at 1-800-255-7778. ◆

```
XEPLD, Version 5.1                                          Xilinx Inc.
                                  Timing Report

Circuit name:  fast1
Target Device: 7336-5PC44                  Report Date:   9-5-94, 22:19:44

Slowest Combinatorial Pad-to-Pad          8.5 nsec (Worst Case)
Slowest Setup-to-Clock at the pads        7.0 nsec (Worst Case)
Slowest Clock-to-Output (pad-to-pad)      4.5 nsec (Worst Case)

Summary of Combinatorial Pad-to-Pad Delays
(In Best to Worst Order)
From       To         Delay (nsec)
A          D          5.0
. . .

Summary of Setup-to-Clock at the Pads (In Best to Worst Order)
Data       Clock      Delay (nsec)
Y          F          3.5
. . .

Summary of Cycle Time Delays
(In Best to Worst Order)
(See .map file for signal names)
From       To         Delay (nsec)
TQ         K1         6.0
. . .

Summary of Clock Pad-to-Output Pad Delays
(In Best to Worst Order)
Clock      Output     Delay (nsec)
Z          M          4.5
```







Text Constraints for RPM Placement

Relationally placed macros (RPMs) cannot be constrained through the .CST text constraints file in PPR v5.0. The .CST file is only useful for single-instance entities; in contrast, RPMs are clusters of instances threaded together by a common set name. PPR will not allow the constraint of a single instance of an RPM in the hopes that this will also lock down its brethren.

With XACT® 5.0, the only way to constrain an RPM is to attach the appropriate RLOC_ORIGIN attribute to the RPM on the schematic. However, text-based constraints are now supported by a utility program called RPMCon. The RPMCon utility translates the RLOC statements in an .XTF file into LOC statements (location constraints) according to a list of user-specified instructions.

The RPMCon program may be downloaded from the BBS by accessing rpmcon.zip (PC), rpmconsp.zip (SPARC), or rpmconhp.zip (HP700). (Please note that this program was developed for the convenience of Xilinx users by the Technical Support staff; it is not supported or tested like a production software product.)

Upcoming PPR v5.1 will include the functionality of RPMCon with slight syntactical differences. PPR 5.1 will also support the equivalent RLOC_RANGE constraint, which RPMCon does not handle. ◆

New Automated Systems for Technical Support

Doing large-scale digital design is rarely easy and sooner or later almost everyone needs support from their vendor. Xilinx Technical Support recognizes that time spent waiting for the vendor to send a document or relay information about already-solved problems is frustrating, and that vendor support can make the difference in meeting a schedule or not.

To help our users get the information they need, Xilinx is installing systems that allow access to information 24-hours-a-day via fax, e-mail and the Internet. The systems are summarized below.

E-MAIL: XDOCS

XDOCS is an automated e-mail-based document retrieval system that allows users to search the technical support database to access software and hardware debugging hints, application notes, and similar technical information. Graphics files such as package drawings are available in postscript form. XDOCS allows Xilinx users to share their Xilinx design experience in an organized way — by submitting records to be added to XDOCS, and thereby making them available to be read by other users once they have been reviewed by Xilinx application engineers. The system provides a way to send a comment to Xilinx on any subject — these comments are then distributed to the appropriate personnel within Xilinx.

The XDOCS system is accessed by sending an e-mail to xdocs@xilinx.com and placing the word "help" at the beginning of the subject line or an e-mail body line. XDOCS commands include:

HELP
Get complete, detailed XDOCS help file.

SEARCH
Search the XDOCS data using keywords.

SUBMIT
Submit information to be added to XDOCS.

COMMENT
Send comments about Xilinx to us — your unfettered feedback path to Xilinx.

SUBSCRIBE
Subscribe to XDOCS mailing list — receive updates of additions to the XDOCS database automatically via e-mail.

After your first e-mail, instructions on the use of the XDOCs system will be sent to you via return e-mail. Please remember, this is an automated system; if you need to send mail to a hotline engineer, send it to: hotline@xilinx.com.

FAX: XFACTS

XFACTS is similar to XDOCS. It allows users to search and select documents by telephoning the system and traversing a voice menu using the phone keypad. First, you request that an index of documents in a specific area — application

Continued on page 37

The Technical Support Bulletin Board

Looking for sample applications you can use in your designs, or a utility to split your PROM file? Do you have the latest updates on speeds and package files? Looking for another route to have that Technical Support question answered? Need to send a problem design to a Xilinx engineer? Then you're about to discover an often overlooked resource that can save you valuable time and effort, the Xilinx Technical Bulletin Board System (BBS)!

Our Technical Support Bulletin Board is a unique resource among the many avenues a Xilinx user can take to get help and information on Xilinx products. It provides 24-hour access to several file areas for general product information, helpful example designs, time-saving utilities, and the latest software updates.

During business hours, technical questions received on the bulletin board are regularly monitored by our technical support engineers, providing an alternative to the Hotline.

How would you like to have that after hours technical question ready for us to answer first thing in the morning? And what if you're running into a troublesome design problem that just can't be expressed over the phone? Upload it! Our engineers will put you back on track with solutions and suggestions.

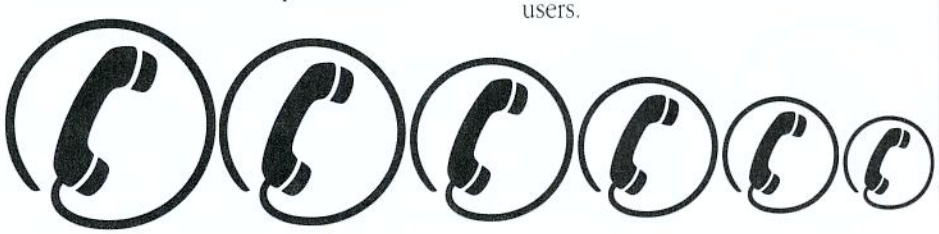
Convenient File Areas

Need immediate information, updates, utilities, or examples? The bulletin board's files are organized into separate areas for convenient access according to interest.

- **General Information** — This area contains general information regarding Xilinx software and components. One of the popular entries in this area is a monthly updated listing of available Xilinx literature. Also, here is where you find public domain archive utilities to simplify file transfers to and from the BBS.

General Information is accessible to all users, even those calling for the first time. The following areas require security access that can be obtained by completing a new user questionnaire.

- **Software Help** — Look in this area to find the newest package and speeds files. You will also find software patches and help files for common software problems.
- **CXC** — This area contains many useful utility programs written by Xilinx engineers and users. If you have a specialty application in mind, we may already have a program that does it for you! Also, if you wrote a utility you're proud of, feel free to share it with the rest of the Xilinx user base. Just be sure to leave a note telling us how to use it.
- **XAPP** — This area has example applications and notes. Most of these correspond to the XAPP notes in Chapter 8 of the *1994 Programmable Logic Data Book*. Included are macros in Viewlogic, Orcad, and X-ABEL formats that can be used in your design or serve as useful examples.
- **Download** — Here is where you receive personal files posted for you by our support staff by prior arrangement.
- **Upload** — This area is reserved for customer uploads. All designs uploaded here are kept in strict confidentiality and are not accessible to other BBS users.



- **User/Xilinx FAE Mailbox** — Need to send a file to your local Xilinx field applications engineer? Just join the User/Xilinx FAE Mailbox Conference by typing "J" at the menu prompt prior to uploading your file. Files uploaded to this conference are immediately available to the intended recipient. All you need to do is let your recipient know the exact name of the file you sent. Similarly, you can download files uploaded by your FAE. Want to leave a message for Xilinx Technical Support? Simply type "C" to leave a comment for the Sysop. Messages are checked three times a day and are forwarded to Xilinx Technical Support engineers who will either answer with a message or call you, depending on the urgency of the request.

Need to have your design looked at by a Xilinx engineer? Simply upload your schematic files and, if you haven't already, notify the Technical Hotline. A Xilinx Technical Support engineer will be assigned to offer expert assistance.

The Xilinx BBS currently runs on a 50-MHz 486 PC connected by modem to three phone lines, two of which support up to 14.4 Kbaud and a third supporting up to 9600 Kbaud.

The BBS is running the latest version of PCBoard software with on-line help and a simple, easy to use menu system. All popular file transfer protocols are supported.

We are currently exploring new ways to make the Xilinx Technical Bulletin Board as useful a resource as possible. Got any ideas you'd like to share? Comments or suggestions are always appreciated.

If you haven't tried the Technical Support Bulletin Board already, you may be missing out on valuable information and resources. Dial in now to register as a new user or to discover what you may have missed before! ◆

The Xilinx Technical Support Bulletin Board:

(24 hours/7 days) (408) 559-9327

NEW TECHNICAL SUPPORT SERVICES — CONTINUED FROM PAGE 35

notes, hardware information, place and route information, etc. — be faxed to you. The list will include a listing of document descriptions with associated key numbers that you can use to order specific faxes by calling the system again later. The XFACTS system should be available by the end of the year.

INTERNET

Xilinx now has a server on the World Wide Web (http://www.xilinx.com). Internet access will allow operations such as using ftp to transfer files to and from Xilinx and similar operations.

Look for formal announcements of XFACTS and other services on the Internet/WWW site as they become available. ◆

Summary of Technical Support Services:

Customer Support Hotline: *8:00 a.m. - 5:00 p.m. Pacific time*	**800-255-7778** *Hrs:*
Customer Support Fax Number: *Avail: 24 hrs/day-7 days/week*	**408-879-4442**
Electronic Technical Bulletin Board: *Avail: 24 hrs/day-7 days/week*	**408-559-9327**
Internet E-mail Address:	**hotline@xilinx.com**
XDOCs E-mail Address:	**xdocs@xilinx.com**
Customer Service*: *ask for customer service*	**408-559-7778**

** Call for software updates, authorization codes, documentation updates, etc.*

General - FPGA

Q: I have received a v5.0 Base package (ViewLogic or OrCAD, DS-xx-BAS-PC1-3). However, I get the following error message whenver I try to invoke PPR:

```
***Error [EXPIRE:INOPERABLE]
This version of the ppr program
has a built-in expiration date.
The mechanisms used to ...
```

What should I do?

A: We have shipped an XACT v5.0.1 update to all of our Base Package customers. However, if you have not received the update, you may either download PPR_EMUL.ZIP (for 386s without co-processors) or PPR_MATH.ZIP (for 386s with co-processors or 486s) from the Bulletin Board or contact Technical Support to get the update.

Q: I have recently converted several hard macros in my design to Relationally Placed Macros (RPMs) so that I can use XACT 5.0 software. I also previously used a constraints file to control the placement of the hard macros. However, I now receive the following error message when executing PPR:

```
***PPR: ERROR 5812:
Constraint file instance '<hard-
macro-name>' could not be
matched to a constrainable
instance in the net list.
```

What is happening?

A: Unlike hard macros, RPMs cannot be constrained in a CST file with PPR v5.0. The only way to constrain an RPM with production software is to place the appropriate RLOC_ORIGIN attribute on the RPM within the schematic. However, we have created a utility program called RPMCon that translates RLOCs in an XTF file into LOCs according to a list of user-specified instructions. *Please see the article entitled "Text Constraints for RPM Placement" on page 34.*

Q: While running XNFBA v5.0 during XSimMake processing, I receive an error message similar to the following:

```
***Error 301: Delay 1.2 on PIN O
of AND is not annotated.
```

What does this mean? What do I do?

A: Error 301 indicates that one of your net delays from the post-routed LCA file is not being properly back-annotated. There are a few unusual cases where this occurs, affecting only a small percentage of designs. If your design falls into this category, please contact Technical Support for further assistance.

Q: I recently installed the XACT v5.0.2 update, but XDM is still version 5.0. Did the update fail?

A: No. Only a few executable programs were updated, so most version numbers won't change. The main focus was to fix some errant data files and add the new EPLD Timing Report Generator and package files.

Q: I have an XC3000A (or XC3000L) design that uses the old library components (not the Unified Library). I have recently upgraded to XACT 5.0 and would like to use XACT-Performance for this XC3000A design. Can I do this?

A: Yes. XACT-Performance is not supported by the APR program. Prior to the XACT 5.0 release, XACT-Performance was available only for the XC4000 family. With XACT 5.0, XC3000A and XC3000L designs are routed with PPR and now are supported by XACT-Performance. However, only designs that use the Unified Library were targeted to support XACT-Performance. You can use XACT-Performance with the old libraries by creating your own Timespec and Timegroup symbols. The easiest way to accomplish this is to copy the Timespec and Timegroup symbols from

the Unified Library into the primary directory. Next, edit the two symbols and remove the LIBVER attributes; this is needed to avoid a "mixed library" message from XNFPrep. Now, you can place and use these symbols in your design. Remember that you now must use PPR instead of APR.

Other FPGA Helpful Hints

- **Carry Logic**—Included in the XC4000 library you can find a little-known symbol called "CY4MODE". This symbol is a chart of all 42 recognized carry logic modes along with the names of their associated symbols. You may wish to temporarily instantiate this symbol onto your schematic as a quick reference.
- **BGA Package files**—The 4010 and 4013 Ball Grid Array (BGA) package files initially shipped with XACT 5.0 are incorrect. You can find the corrected files in XC4KB225.ZIP on the BBS. After you have unzipped the files, you should copy them into the \XACT\DATA directory.

General - EPLD

Q: If a device has more than one VCCIO pin, can some be tied to 3.3 V and others to 5 V?

A: No. All VCCIO pins must be tied to the same voltage level.

Q: When designing with PLUSASM, can I specify a default clock signal?

A: Yes. If a registered equation does not have a clock specified, the XEPLD software automatically uses the first signal declared as a FASTCLOCK as the default clock.

Mentor Graphics

Q: While running GEN_SCH8, v5.0, I receive the following error message:

```
ERROR: Bad status 79502001 from
ddp_setup_pin_scan
Sheet/Symbol diagram is closed
GEN_SCH8: ERROR 386: Error
found in check_status.
```

Why is this happening and what should I do?

A: This problem occurs in very large designs or designs that contain a large number of XBLOX modules. In both cases, many power and ground connections are needed. If a power or ground symbol is the last symbol written on a schematic page, then the error occurs. GEN_SCH8 will not write the symbol to the page before closing it and opening a new page. *Contact Technical Support for assistance if you encounter this problem.*

OrCAD

Q: What is the meaning of the following error message in SDT2XNF v5.0?

```
***DS35-SDT-ERROR-016:
Failed to open the file ".inf"
for reading.
```

A: First, note that the name of the file is missing; only the ".inf" extension is given. The most likely cause is that a sheet symbol has a name longer than eight characters. Since the filename limit for DOS is eight characters, SDT2XNF cannot locate the file and issues this error message. Check your schematic for overly long sheet names.

Synopsys Helpful Hint

Synopsys' FPGA Compiler, by default, will write partitioning information into the XNF file. However, our tests and user feedback indicate that better results usually can be achieved by allowing PPR to perform its own partitioning. We recommend that you disable FPGA Compiler's ability to partition logic into BLKNMs; to achieve this, type in the following command after "replace_fpga" but before saving the file as an XNF file:

```
set_attribute design
"xnfout_use_blknames" -type
boolean FALSE
```

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FAX in Your Comments and Suggestions

To: Brad Fawcett, *XCELL* Editor **Xilinx Inc. FAX**: 408-879-4676

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NAME _____

COMPANY _____

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CITY/STATE/ZIP _____

PHONE _____

❑ **I'm interested in having my company's design featured in a future edition of XCELL as a Customer Feature.**

Comments and Suggestions: _____

From the employees of Xilinx to our customers, sales representatives and distributors:

Best Wishes For a Joyful Holiday and A Happy New Year!

Please use this form to FAX in your comments and suggestions, or to request an addition to the XCELL mailing list. Please feel free to make copies of this form for your colleagues.

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