W83194BR-K8

WINBOND

CLOCK GENERATOR FOR AMD K8 SYSTEM SERIES CHIPSETS

Publication Release Date: December 27, 2004
Revision 1.0

Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	6/8/93	0.5	n.a.	All of the versions before 0.50 are for internal use.
2		12/27/04	1.0	1.0	Update on Web
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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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1. GENERAL DESCRIPTION

The W83194BR-K8 is a Clock Synthesizer meets AMD ATHLON 64 and OPTERON Processors series chipset. W83194BR-K8 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, HT66 and PCI clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-K8 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides +/-0.5% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

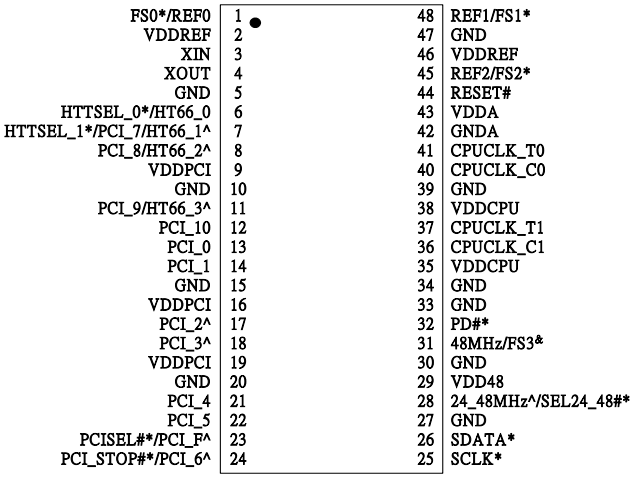
The W83194BR-K8 also has watchdog time and reset out pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-K8 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

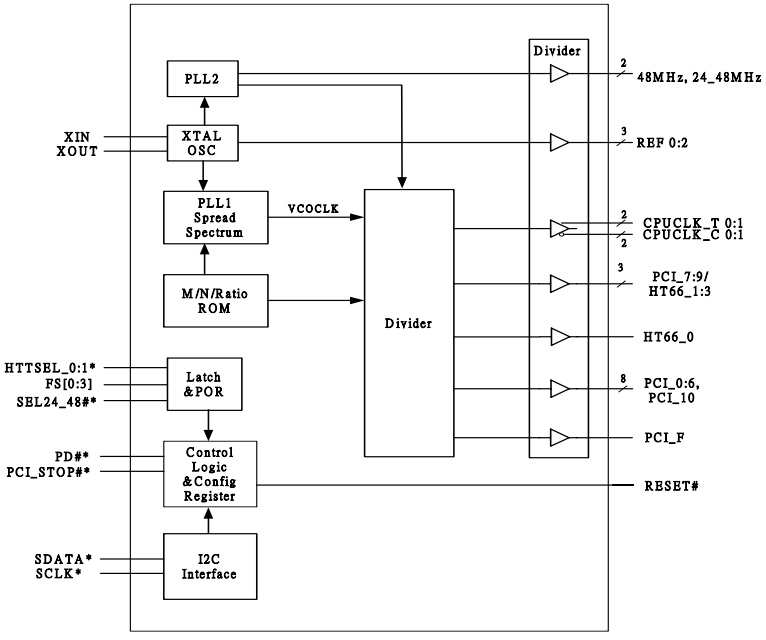
- 2 pairs push-pull differential clock for CPU and Chipset
- 3 selectable PCI/HT66 clock outputs
- 1 HT66 clock output
- 9 PCI synchronous clocks, 1 free running
- 1 48MHz clock outputs
- 1 24_48MHz for I/O chip, default 24MHz
- 3 REF 14.318MHz clock outputs
- I^2C 2-Wire serial interface supports block and byte mode read/write
- Step-less frequency programming
- Smooth frequency switch with selections from 100 to 309MHz
- Programmable clock outputs Slew rate control and Skew control
- +/- 0.5% center type spread spectrum in table mode
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch dog timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION



#: Active low
^. Output has 2X drive strength
*: Internal pull up resistor 120KΩ to VDD
&: Internal Pull-down resistor 120KΩ to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{td120k}	Latch input pin and internal 120KΩ pull down
IN_{tp120k}	Latch input pin and internal 120KΩ pull up
OUT	Output
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain
OD	Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
3	XIN	IN	Crystal input with internal loading capacitors and feedback resistors.
4	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors.

5.2 CPU, PCI/HT66, PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
41, 37, 40, 36	CPUCLK_T 0:1 CPUCLK_C 0:1	OUT	3.3V push-pull differential clock outputs for CPU and Chipset.
6	HT66_0	OUT	3.3V HT 66 MHz output clock
	HTTSEL_0*	INtp120k	Latched input at initial power up for PCI/HT66 selecting the output frequency clocks. This is internal 120KΩ pull up.
7	PCI_7/ HT66_1^	OUT	3.3V PCI 33MHz or HT 66MHz(default) output clock select by HTTSEL [0:1] output has 2X drive strength
	HTTSEL_1*	INtp120k	Latched input at initial power up for PCI/HT66 selecting the output frequency clocks. This is internal 120KΩ pull up.
8,11	PCI_8:9/ HT66 _2:3^	OUT	3.3V PCI 33MHz(default) or HT 66 MHz output clocks select by HTTSEL [0:1] outputs has 2X drive strength
13, 14, 17, 18, 21, 22,12	PCI_0:5 PCI_10	OUT	3.3V PCI clock outputs, the pin 17,18 PCI [2:3] outputs has 2X drive strength

CPU, PCI/HT66, PCI Clock Outputs, continued

PIN	PIN NAME	TYPE	DESCRIPTION
23	PCI_F^	OUT	3.3V Free-Run PCI clock output, 2X drive strength, not affected by PCI_STOP#.
	PCISEL#*	IN_{tp120k}	Latched input at initial power up for pin 24 PCI_STOP/PCI_6 selecting the output, This is internal 120KΩ pull up, when PCISEL# = 0 pin24 is PCI_6^, = 1 pin 24 is PCI_STOP#(default)
24	PCI_6^	OUT	3.3V PCI clock outputs, 2X drive strength.
	PCI_STOP#*	IN_{tp120k}	Input pin, Stops all PCI clock besides, when input low, This is internal 120KΩ pull up (default).

5.3 Fixed Frequency Outputs and Function Control pin

PIN	PIN NAME	TYPE	DESCRIPTION
1	REF0	OUT	14.318MHz output.
	FS0*	IN_{tp120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up.
48	REF1	OUT	14.318MHz output.
	FS1*	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up.
45	REF2	OUT	14.318MHz clock output.
	FS2*	IN_{tp120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up.
28	24_48MHz^	OUT	24 or 48MHz clock output, 2X drive strength.
	SEL24_48#*	IN_{tp120k}	Latched input for 24_48MHz at initial power up selecting the output frequency clocks. This is internal 120KΩ pull up, 1 = 24 MHz (default), 0= 48MHz.
31	48MHz	OUT	48MHz clock output.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down.
32	PD#*	IN_{tp120k}	Low active Input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. This is internal 120KΩ pull up.
44	RESET#	OD	System reset signal when the watchdog is time out. This pin will generate 250mS low signal when watchdog timer is timeout.

5.4 I²C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
26	SDATA*	I/OD	Serial data of I²C 2-wire control interface with internal pull-up resistor.
25	SCLK*	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

5.5 Power an GND Pins

PIN	PIN NAME	DESCRIPTION
2,46	VDDREF	3.3V power supply for REF.
9,16,19	VDDPCI	3.3V power supply for PCI.
29	VDD48	3.3V power supply for 48MHz.
35,38	VDDCPU	3.3V power supply for CPU.
43	VDDA	3.3V power supply analog core.
42	GNDA	Ground pin for analog core.
5, 10, 15, 20, 27, 30, 33, 34, 39, 47	GND	Ground pin for 3.3V.

5.6 HTTSEL table

HTTSEL_0	HTTSEL_1	PCI_7/HT66_1(PIN7)	PCI_8/HT66_2(PIN8)	PC_9I/HT66_3(PIN11)
0	0	HT66_1	HT66_2	PCI_9
0	1	HT66_1	HT66_2	HT66_3
1	0	PCI_7	PCI_8	PCI_9
1	1	HT66_1	PCI_8	PCI_9

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	HT66 (MHZ)	PCI (MHz)
0	0	0	0	0	100.9	67.2	33.6
0	0	0	0	1	133.9	66.9	33.4
0	0	0	1	0	168.0	67.2	33.6
0	0	0	1	1	202.0	67.3	33.6
0	0	1	0	0	100.2	66.8	33.4
0	0	1	0	1	133.5	66.7	33.3
0	0	1	1	0	166.7	66.6	33.3
0	0	1	1	1	200.4	66.8	33.4
0	1	0	0	0	150.0	60.0	30.0
0	1	0	0	1	180.0	60.0	30.0
0	1	0	1	0	210.0	70.0	35.0
0	1	0	1	1	240.0	60.0	30.0
0	1	1	0	0	270.0	67.5	33.7
0	1	1	0	1	233.3	66.6	33.3
0	1	1	1	0	266.6	66.6	33.3
0	1	1	1	1	300.0	75.0	37.5
1	0	0	0	0	100.0	66.6	33.3
1	0	0	0	1	133.3	66.6	33.3
1	0	0	1	0	166.6	66.6	33.3
1	0	0	1	1	200.0	66.6	33.3
1	0	1	0	0	103.0	68.6	34.3
1	0	1	0	1	137.3	68.6	34.3
1	0	1	1	0	171.6	68.6	34.3
1	0	1	1	1	206.0	68.6	34.3
1	1	0	0	0	154.5	61.8	30.9
1	1	0	0	1	185.4	61.8	30.9
1	1	0	1	0	216.3	72.1	36.0
1	1	0	1	1	247.2	61.8	30.9
1	1	1	0	0	278.1	69.5	34.7
1	1	1	0	1	240.3	68.6	34.3
1	1	1	1	0	274.6	68.6	34.3
1	1	1	1	1	309.0	77.2	38.6

7. I²C CONTROL AND STATUS REGISTERS

(The register No. Is increased by 1 if use byte data read/write protocol)

7.1 Register 0: Frequency Select Register (Default = 38H)

BIT	NAME	PWD	DESCRIPTION
7	SSEL 4	0	Software frequency table selection through I²C
6	SSEL 3	0	
5	SSEL 2	1	
4	SSEL 1	1	
3	SSEL 0	1	
2	EN_SSEL		Enable software table selection FS [4:0]. 0 = Hardware table setting. 1 = Software table setting through Bit7~3.
1	EN_SPSP	0	Enable spread spectrum mode under clock output. 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable
0	EN_SAFE_FREQ	0	After watchdog timeout 0 = Reload the hardware FS [4:0] latched pins setting. 1 = Reload the desirable frequency table selection defined at Reg-5 Bit 4~0.

7.2 Register 1: CPU & PCI_F Clock Control (1 = Enable, 0 = Stopped) & FS0~FS3 latch Register

BIT	NAME	PWD	DESCRIPTION
7	PCI_FEN	1	Pin 23 PCI_F output control
6	CPUCLKEN1	1	Pin 37,36 CPUCLK_T1/C1 output control
5	CPUCLKEN0	1	Pin 41,40 CPUCLK_T0/C0 output control
4	FS4	0	Fix in low level
3	FS3&	X	Power on latched value of FS3 pin 31.
2	FS2*	X	Power on latched value of FS2 pin 45.
1	FS1*	X	Power on latched value of FS1 pin 48.
0	FS0*	X	Power on latched value of FS0 pin 1.

7.3 Register 2: PCI Clock Register (1 = Enable, 0 = Stopped)

BIT	NAME	PWD	DESCRIPTION
7	PCI_6EN	1	Pin 24 PCI_6 output control
6	PCI_10EN	1	Pin 12 PCI_10 output control
5	PCI_5EN	1	Pin 22 PCI_5 output control
4	PCI_4EN	1	Pin 21 PCI_4 output control
3	PCI_3EN	1	Pin 18 PCI_3 output control
2	PCI_2EN	1	Pin 17 PCI_2 output control
1	PCI_1EN	1	Pin 14 PCI_1 output control
0	PCI_0EN	1	Pin 13 PCI_0 output control

7.4 Register 3: HT66, REF Clock Register (1 = Enable, 0 = Stopped)

BIT	NAME	PWD	DESCRIPTION
7	-	1	Reserved for Winbond internal use, don't modify it
6	REF2EN	1	Pin 45 REF2 output control
5	REF1EN	1	Pin 48 REF1 output control
4	REF0EN	1	Pin 1 REF0 output control
3	HT66_0EN	1	Pin 6 HT66_0 output control
2	HT66_3EN	1	Pin 11 PCI_9/HT66_3 output control
1	HT66_2EN	1	Pin 8 PCI_8/HT66_2 output control
0	HT66_1EN	1	Pin 7 PCI_7/HT66_1 output control

7.5 Register 4: 24_48MHz Control Register (1 = Enable, 0 = Stopped)

BIT	NAME	PWD	DESCRIPTION
7	SEL_24	X	Pin 28 SEL24 _48 MHz output selection 1: 24 MHz (default), 0: 48 MHz. Default value depend on latched value of SEL24_48# pin duration power on reset.
6	24_48MEN	1	Pin 28 24_48MHz output control
5	48EN	1	Pin 31 48MHz output control
4	HTTSEL_0*	X	Pin 6 Power on latched value of HTTSEL_0* pin.
3	HTTSEL_1*	X	Pin 7 Power on latched value of HTTSEL_1* pin.
2	PCISEL#*	X	Pin 23 Power on latched value of PCISEL#* pin.
1	-	0	Reserved for Winbond internal use, don't modify it
0	-	0	Reserved for Winbond internal use, don't modify it

7.6 Register 5: Watchdog Control Register

BIT	NAME	PWD	DESCRIPTION
7	-	0	Reserved for Winbond internal use, don't modify it
6	EN_WD	0	1: Enable Watchdog Timer. 0: Disable Watchdog Timer. During timer count down the bit read back to 1. If count to zero, this bit read back to 0.
5	WD_TIMEOUT	0	Read Back only. Timeout Flag. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.
4	SAF_FREQ 4	0	These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1.
3	SAF_FREQ 3	0	
2	SAF_FREQ 2	0	
1	SAF_FREQ 1	0	
0	SAF_FREQ 0	0	

7.7 Register 6: Watchdog Timer Register

BIT	NAME	PWD	DESCRIPTION
7	WD_TIME [7]	0	Watchdog timeout time. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If the watchdog timer is start, this register will be down count. Read this register will return a down count value.
6	WD_TIME [6]	0	
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	
0	WD_TIME [0]	0	

7.8 Register 7: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N<8>	X	Programmable N divisor value. Bit 7 ~0 are defined in the Register 8.
6	M<6>	X	Programmable M divisor value.
5	M>5>	X	
4	M<4>	X	
3	M<3>	X	
2	M<2>	X	
1	M<1>	X	
0	M<0>	X	

7.9 Register 8: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	X	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 7, bit 9~11 is defined in register 10 bit 3~5.
6	N_DIV [6]	X	
5	N_DIV [5]	X	
4	N_DIV [4]	X	
3	N_DIV [3]	X	
2	N_DIV [2]	X	
1	N_DIV [1]	X	
0	N_DIV [0]	X	

Note: about N value bit 9~11description only for Winbond internal and BOIS program use; the release version please reserved this description.

7.10 Register 9: Spread Spectrum Programming Register

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3.
6	SP_UP [2]	0	Spread Spectrum Up Counter bit 2.
5	SP_UP [1]	0	Spread Spectrum Up Counter bit 1.
4	SP_UP [0]	1	Spread Spectrum Up Counter bit 0
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3
2	SP_DOWN [2]	1	Spread Spectrum Down Counter bit 2
1	SP_DOWN [1]	1	Spread Spectrum Down Counter bit 1
0	SP_DOWN [0]	1	Spread Spectrum Down Counter bit 0

7.11 Register 10: Divisor and Step-less Enable and Skew Control Register

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: using frequency table 1: using M/N register to program all type clock frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**. Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg9 - bit 7).
6	Reserved	0	Reserved.
5	N<11>	0	Programmable N divisor bit 11,10,9. Setting these bits prior to enable M/N programming method.
4	N<10>	X	
3	N<9>	X	
2	KVAL<2>	X	Define the CPU/HT66/PCI divider ratio Refer to Table-1
1	KVAL<1>	X	
0	KVAL<0>	X	

Note: This Byte 3:5 only for Winbond internal and BOIS program use; the release version please reserved this byte.

Table-1 CPU, HT66, PCI divider ratio selection Table

KVAL2~KVAL0	CPU	HT66	PCI
000	2	5	10
001	2	6	12
010	2	7	14
011	2	8	16
100	4	6	12
101	4	8	16
110	4	10	20
111	3	6	12

7.12 Register 11: Spread Spectrum Programming Register

BIT	NAME	PWD	DESCRIPTION
7	SPSP1	1	Spread Spectrum type select. 00 : Down 1% 01 : Down 0.5% 10 : Center 1% 11 : Center 0.5%
6	SPSP0	1	
5	SPCNT [5]	0	Spread Spectrum Programmable time, the resolution is 280ns The frequency of Spread Spectrum is 33KHz.
4	SPCNT [4]	0	
3	SPCNT [3]	1	
2	SPCNT [2]	0	
1	SPCNT [1]	1	
0	SPCNT [0]	0	

Note: This Byte 0:5 only for Winbond internal and BOIS program use; the release version please reserved this byte.

7.13 Register 12: SKEW Control Register

BIT	NAME	PWD	DESCRIPTION
7	CPU_PCI_SKEW [2]	1	CPU to PCI skew control
6	CPU_PCI_SKEW [1]	0	
5	CPU_PCI_SKEW [0]	0	
4	Reserved	0	Reserved
3	FIX_HT66_PCI	0	0: normal mode, 1: fix mode
2	CPU_HT66_SKEW [2]	1	CPU to PCI_HT66 skew control.
1	CPU_HT66_SKEW [1]	0	
0	CPU_HT66_SKEW [0]	0	

7.14 Register 13: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-K8 (BA5846).
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	0	Winbond Chip ID.
4	CHPI_ID [4]	0	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	1	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	0	Winbond Chip ID.

7.15 Register 14: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	MAS_ID [1]	0	Winbond Master-Chip ID.
6	MAS_ID [0]	1	Winbond Master-Chip ID.
5	SUB_ID [1]	0	Winbond Sub-Chip ID.
4	SUB_ID [0]	1	Winbond Sub-Chip ID.
3	MAS_VER_ID [1]	0	Winbond Master's Version ID.
2	MAS_VER_ID [0]	1	Winbond Master's Version ID.
1	SUB_VER_ID [1]	0	Winbond Sub's Version ID.
0	SUB_VER_ID [0]	1	Winbond Sub's Version ID.

Note: The Register 15:17 slew rate control select bit fit value Please fellow below table.

S2	S1	Slew rate status
0	0	Weak
0	1	Normal
1	0	Strong
1	1	More Strong

7.16 Register 15: REF & PCI Output Slew-Rate Control

BIT	NAME	PWD	DESCRIPTION
7	REF_S1	0	REF Pin 1, 48, 45 output slew rate control bit.
6	REF_S2	0	This slew rate status default is Weak
5	PCIA_S1	1	PCI Pin 12, 13, 14, 21, 22 output slew rate control bit.
4	PCIA_S2	0	This slew rate status default is normal
3	PCIB_S1	0	PCI Pin 17, 18, 24 output slew rate control bit.
2	PCIB_S2	1	This slew rate status default is strong
1	PCIF_S1	0	PCI Pin 23 output slew rate control bit.
0	PCIF_S2	1	This slew rate status default is strong

7.17 Register 16: HT66 & 24_48MHz Slew-Rate Control

BIT	NAME	PWD	DESCRIPTION
7	HT66_0_S1	1	HT66_0 Pin 6 output slew rate control bit.
6	HT66_0_S2	0	This slew rate status default is normal
5	HT66_12_S1	0	HT66_1:2 Pin 7, 8 output slew rate control bit.
4	HT66_12_S2	1	This slew rate status default is strong
3	HT66_3_S1	0	HT66_3 Pin 11 output slew rate control bit.
2	HT66_3_S2	1	This slew rate status default is strong
1	P24M_S1	0	24_48MHz Pin 28 output slew rate control bit.
0	P24M_S2	1	This slew rate status default is strong

7.18 Register 17: Slew Rate Control

BIT	NAME	PWD	DESCRIPTION
7	P48M_S1	1	48MHz Pin 31 output slew rate control bit.
6	P48M_S2	0	This slew rate status default is Normal
5	CPU_S1	1	CPU Pin 36,37,40,41 output slew rate control bit.
4	CPU_S2	0	This slew rate status default is Normal
3	IVAL<3>	1	Charge pump current selection
2	IVAL<2>	X	Charge pump current selection
1	IVAL<1>	X	Charge pump current selection
0	IVAL<0>	X	Charge pump current selection

Note: This Byte 0:3 only for Winbond internal and BOIS program use; the release version please reserved this byte.

7.19 Register 18: M, N Time & Type Control

BIT	NAME	PWD	DESCRIPTION
7	N_Time<2>	0	M/N mode N value change time control
6	N_Time<1>	1	
5	N_Time<0>	0	
4	M_Time<2>	1	M/N mode M value change time control
3	M_Time<1>	1	
2	M_Time<0>	0	
1	Reserved	1	Reserved for Winbond internal use, don't modify it
0	Reserved	1	Reserved for Winbond internal use, don't modify it

Note: This Byte only for Winbond internal and BOIS program use, the release version please reserved this byte.

M_Time<2:0> or N_Time<2:0>	M_Divider or N_Divider timing counter
000	6.152us
001	12.304us
010	24.608us
011	49.216us
100	98.432us
101	196.864us
110	393.728us
111	787.456us

7.20 Register 80: Winbond Test Register 1

BIT	NAME	PWD	DESCRIPTION
7:0	TEST_REG1	00h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.
7	TESTKEY <3>	0	TESTKEY [3:0] is filled 4'b 1011 to enter test mode
6	TESTKEY <2>	0	
5	TESTKEY <1>	0	
4	TESTKEY <0>	0	
3	TESTMODE <3>	0	TESTMODE [3:0] is filled 4'b1000 ➔ WD test mode TESTMODE [3:0] is filled 4'b0001 ➔ force REF Clock to 0 & other output clock to 0 TESTMODE [3:0] is filled 4'b001X ➔ force REF Clock to 1 & other output clock to 0
2	TESTMODE <2>	0	
1	TESTMODE <1>	0	
0	TESTMODE <0>	0	

7.21 Register 81: Winbond Test Register 2

BIT	NAME	PWD	DESCRIPTION
7:0	TEST_REG2	00h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.
7	Iref_test0	0	Iref_test0
6	EN_CD3	1	EN_CD3
5	EN_HTT7	1	EN_HTT7
4	EN_HTT10	1	EN_HTT10
3	EN_CK7	1	EN_CK7
2	TESTSP	0	TESTSP
1	TSTSPCLK	0	TSTSPCLK
0	Tri-state	0	Tri-state all output if set 1

7.22 Register 82: Winbond Test Register 3

BIT	NAME	PWD	DESCRIPTION
7:0	TEST_REG3	00h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.
7	Reserved	0	Reserved
6	Reserved	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	Reserved	0	Reserved

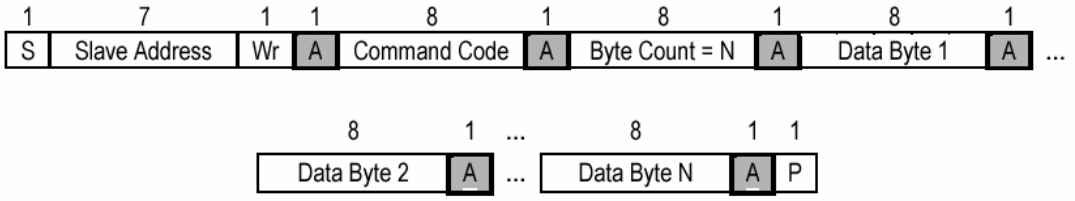
Note: The Byte 80:82 only for Winbond internal use, in release version please reserved this byte.

8. ACCESS INTERFACE

The W83194BR-K8 provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-K8 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.

Block Read and Block Write Protocol

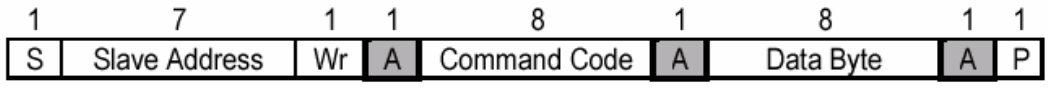
8.1 Block Write Protocol



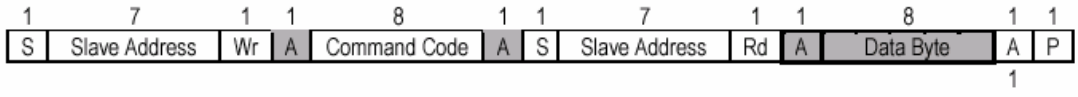
8.2 Block Read Protocol

In block mode, the command code must filled 00H

8.3 Byte Write Protocol



8.4 Byte Read Protocol



9. SPECIFICATIONS

9.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDDREF =VDDA=VDDCPU=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Cl=10pF

PARAMETER	SYM.	MIN.	MAX.	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		300	mA	CPU = 100 to 309 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group Timing Clock

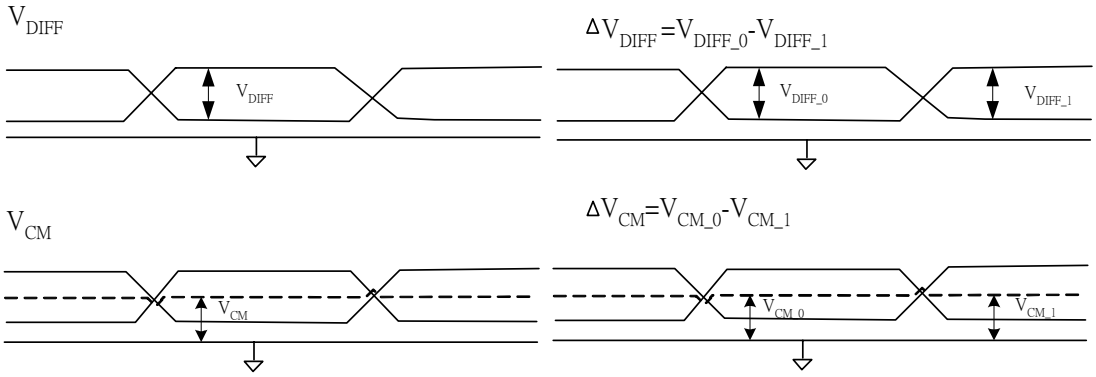
VDDREF =VDDA=VDDCPU=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
CPU to CPU Skew			250	ps	Crossing point for CPUT rising edge
CPU to PCI Skew			500	ps	Crossing point for CPUT rising edge and 1.5V for PCI clocks
CPU to HT66 Skew			500	Ps	Crossing point for CPUT rising edge and 1.5V for HT66 clocks
PCI to PCI Skew			500	ps	Measured between rising at 1.5V
PCI to HT66 Skew			500	ps	Measured between rising at 1.5V
HT66 to HT66 Skew			500	ps	Measured between rising at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured between rising at 1.5V
REF to REF Skew			500	ps	Measured between rising at 1.5V

9.4 CPU Electrical Characteristics

VDDA=VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF,

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Rise Edge Rate	2		10	V/ns	Measured at CPU test load. 0V± 400mV (differential measurement)
Fall Edge Rate	2		10	V/ns	Measured at CPU test load. 0V± 400mV (differential measurement)
V_{DIFF}: Differential Voltage (Single ended)	0.4	1.25	2.3	V	Measured at CPU test load. (Single ended measurement)
ΔV_{DIFF}: Change in V_{DIFF_DC} Magnitude	-150		+150	mV	Measured at CPU test load. (Single ended measurement)
V_{CM}: Common Mode Voltage	1.05	1.25	1.45	V	Measured at CPU test load. (Single ended measurement)
ΔV_{CM}: Change Common Voltage	-200		+200	mV	Measured at CPU test load. (Single ended measurement)
Duty Cycle	45	50	53	%	Measure at the differential crossing point
Cycle to Cycle Jitter		100	200	ps	Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.
Frequency Stabilization from Power-up (cold start)	0		3	ms	Measured from full supply voltage



9.5 HT66 Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,

PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
Rise Edge Rate	1	4	V/ns	Measured from 20% to 60%
Fall Edge Rate	1	4	V/ns	Measured from 20% to 60%
Cycle to Cycle jitter		250	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.6 PCI Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	1	4	V/ns	Measured from 20% to 60%
Fall Edge Rate	1	4	V/ns	Measured from 20% to 60%
Cycle to Cycle jitter		250	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Fall Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Cycle to Cycle jitter		500	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 REF Electrical Characteristics

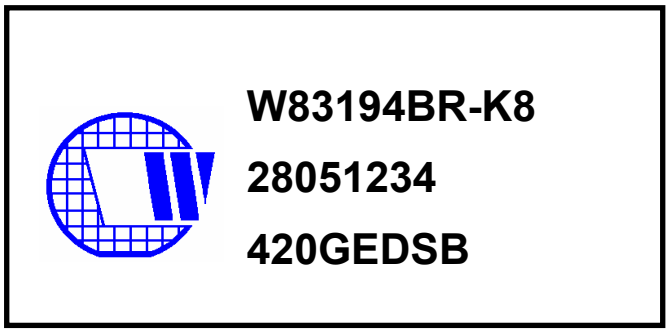
VDDREF= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,

PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
Rise Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Fall Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Cycle to Cycle jitter		1000	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-K8	48 PIN SSOP	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-K8

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 420 G E D SA

420: packages made in '2004, week 20

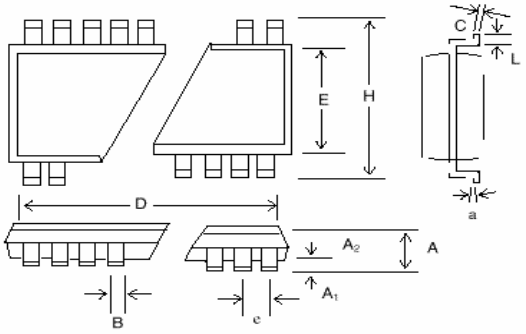
G: assembly house ID; O means OSE, G means GR

E: Internal use code

D: IC revision

SA: mask version

12. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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