1. PRODUCT DESCRIPTION

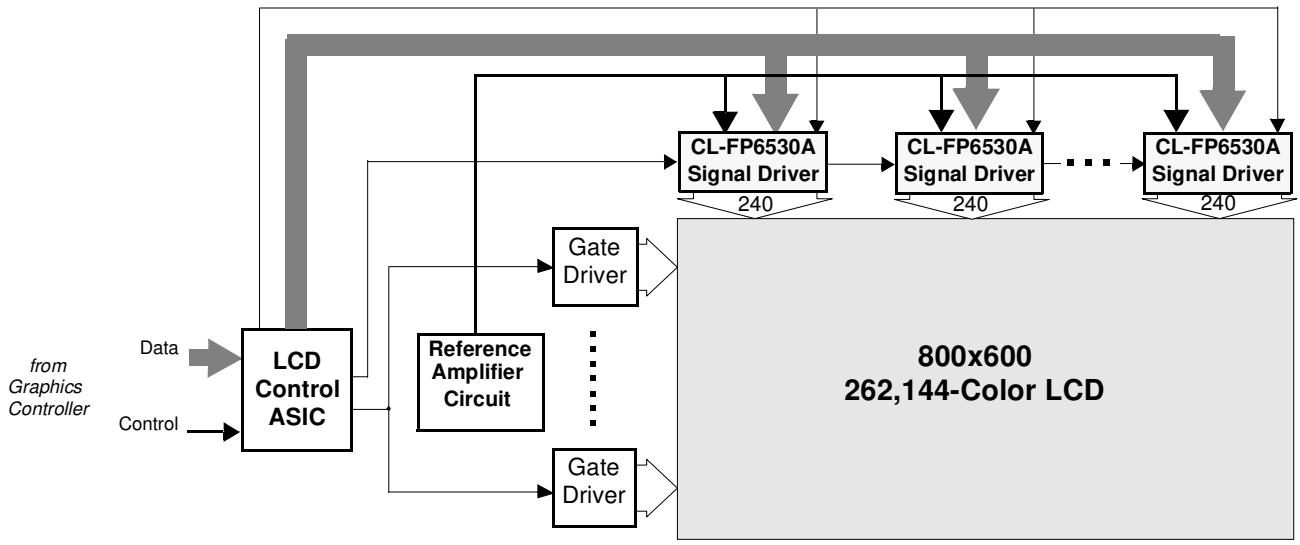
The WFP6530B is a 6-bit, 240-channel signal driver designed for SVGA chip-on-glass (COG) TFT-LCDs. The WFP6530B's minimum form factor and optimized COG layout permit the design of high-display-quality, low-power 6-bit TFT-LCD's with minimum bezel area.

The WFP6530B's internal architecture includes a resistor-string DAC with the value of the individual resistor segments weighted to reduce signal driver power dissipation by as much as 20% to 40% when compared to non-weighted resistor string DAC architectures..

COG Signal Driver

240-Channel, 6-Bit Signal Driver for TFT-LCD COG Applications

The WFP6530B silicon is Rev. K of the WFP6540 die. The Rev. K die has 10 additional dummy pads compared to Revs. A-H.



2. FEATURES & BENEFITS

Features	Benefits
• Full Color Display	• 64 gray scales per primary color • 262,144 (256K) color palette
• High Speed Operation • 65 MHz (**3.3 V** and 5.0V logic supply)	• Support for wide range of color LCD resolutions • Single driver bank supports up to 1024 x 768
• Minimum Form Factor • 17.06 mm x 1.30 mm • 70 μm output pitch • 675 μm ± 25 μm chip thickness	• Minimum Bezel Size
• High Integration • 240 output voltage channels • Bi-directional shift register	• Minimizes external components and circuitry • 10 drivers for 800x600 color LCDs • Easy re-configuration from backlit operation to over-head projector (OHP) operation
• Data Inversion Feature	• Data inversion capability enables a complete internal solution for Vcom modulation by data inversion. • Allows implementation of data transition reduction schemes.
• Low-power operation • Logic Supply: 3.3 V ± 0.3 or 5.0 V ± 0.5 • Analog Supply: 3.3 V ± 0.3 to 5.0 V ± 0.5 • Automatic standby function	• Extends battery-based operation • Low power and EMI from 3.3 V operation • Minimum dynamic-power dissipation
• Excellent Output Uniformity	• Output Error (max) ± 0.15 LSB
• Weighted R-String: See Figure 2-1 & Table 2-1	• Reduces Power Dissipation 20-40% or more. • Reduces dc current drive requirements of external reference amplifiers

- Rseg Value
  - Internal weighted R-String for low power operation (see Table 2-1 and Figure 2-1).

Table 2-1: Weighted R_{SEG} Values (ignoring bus resistance)

R-Segment	Proportion	Value
V7 ~ V8 (V55~V63)	2x	40Ω,40Ω,40Ω,40Ω,40Ω,40Ω,40Ω,40Ω
V6 ~V7	1.2x	24 Ω X 8
V5 ~V6	1x	20 Ω X 8
V4 ~V5	1x	20 Ω X 8
V3 ~V4	1x	20 Ω X 8
V2 ~V3	1x	20 Ω X 8
V1 ~V2	1.2x	24 Ω X 8
V0 ~V1 (V00~V07)	1.75x	40Ω, 40Ω 40Ω, 40Ω, 40Ω, 40Ω, 40Ω

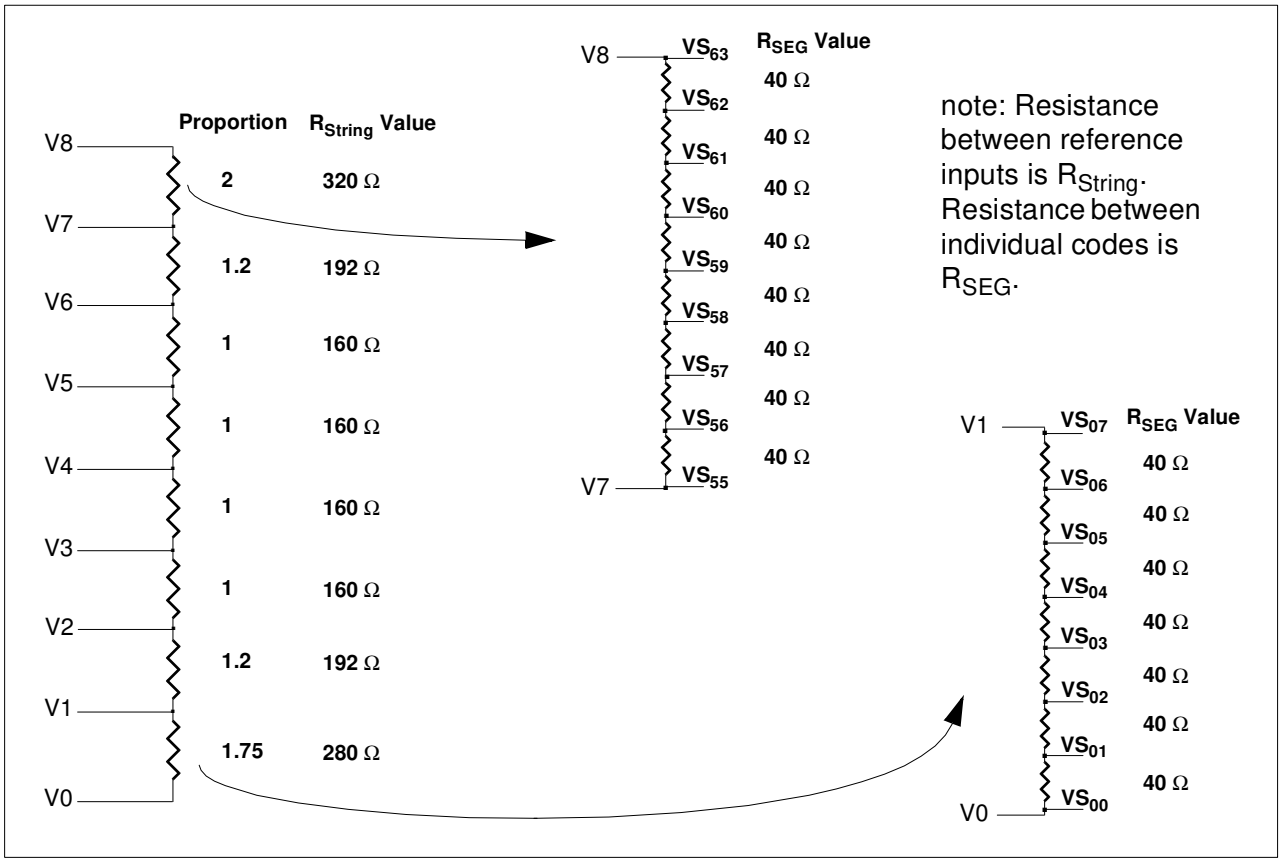
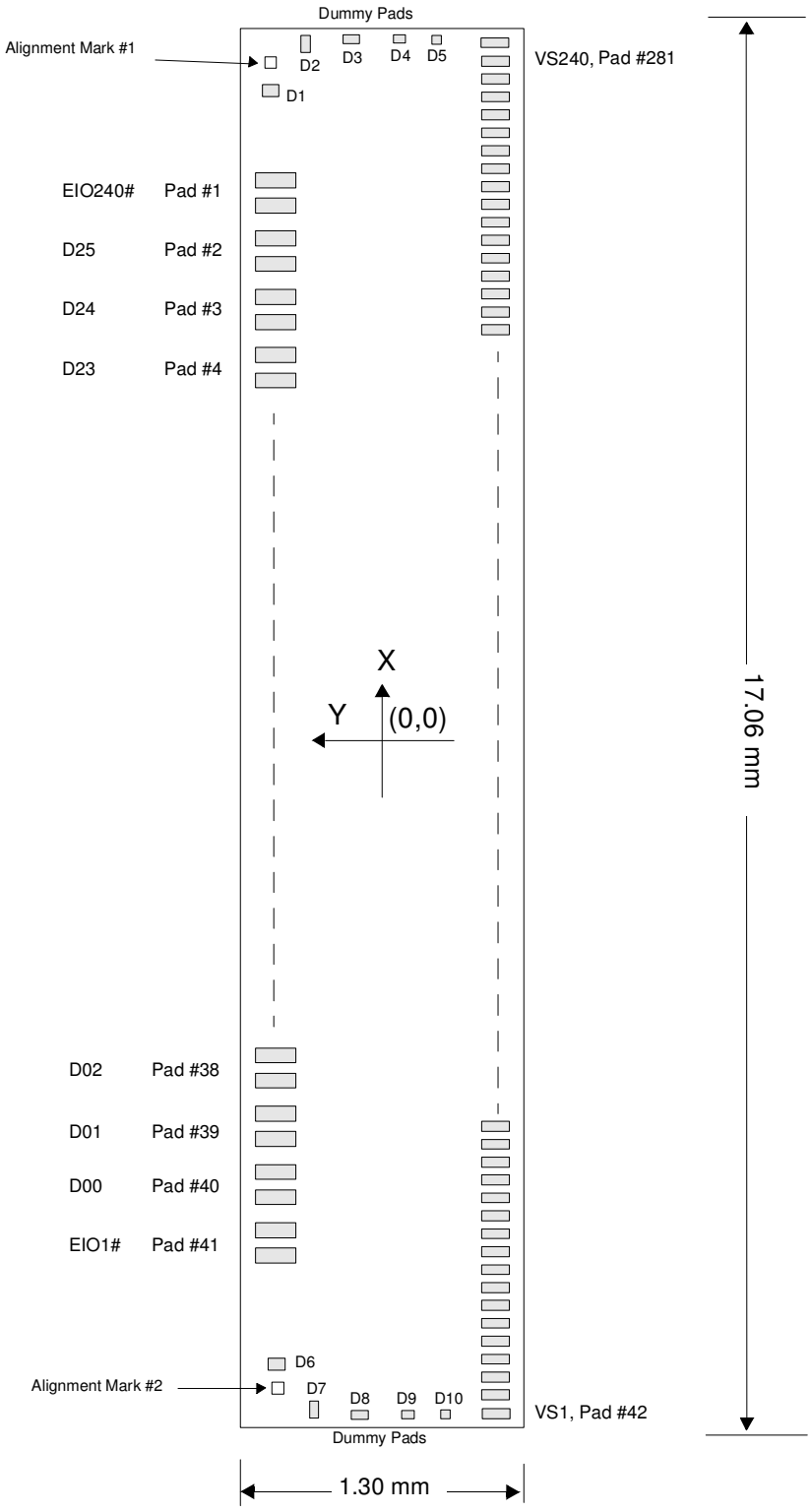


Figure 2-1: Weighted R-String Detail

3. WFP6530B DIMENSIONS & SPECIFICATIONS

3.1. DIE DIMENSIONS



3.2. Bump Specifications

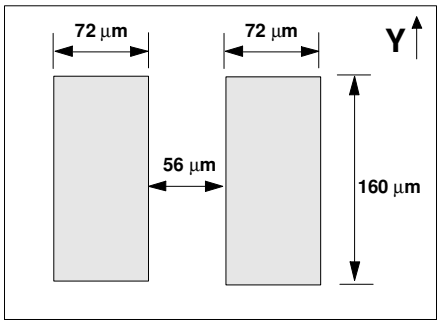


Figure 3-2: Split Input Pad Bump

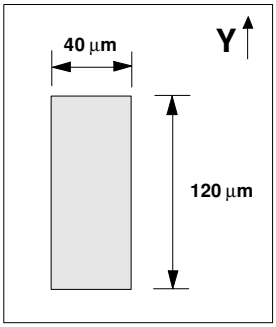


Figure 3-3: Output Pad Bump

Table 3–1. Dummy Bump Sizes

Name	Pad #	Size (Y by X) µm	Name	Pad #	Size (Y by X) µm
D5,D10	282,291	50 by 50	D2,D7	285,288	100 by 40
D4,D9	283,290	50 by 70	D1,D6	286,291	60 by 100
D3,D8	284,289	50 by 100			

- Bump Height: 15 µm ± 2 µm
- Bump Dimple: less than 2 µm (see Figure 3-5)
- Bump Material: Gold
- Bump Hardness: 30 HV ~ 80 HV,
- Bump Shape: Tapered wall, 80° ± 5 angle to plane of top of die

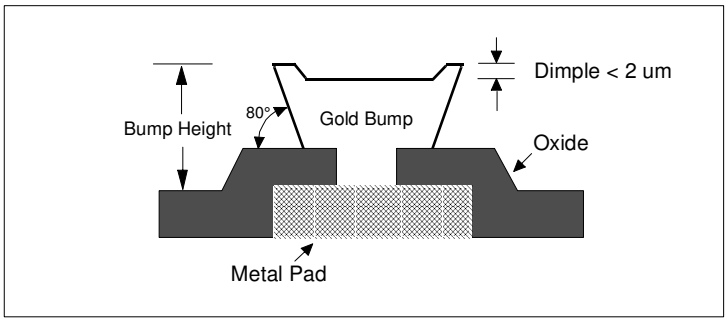


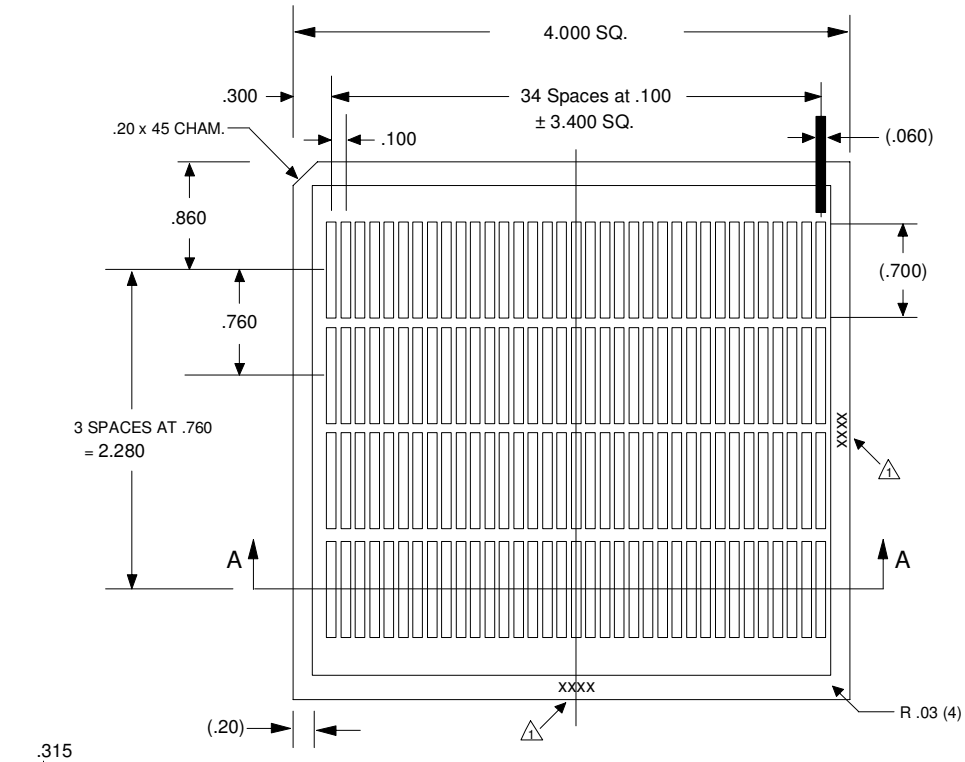
Figure 3-5: Bump Specification Definitions

3.3. Alignment Mark Coordinates

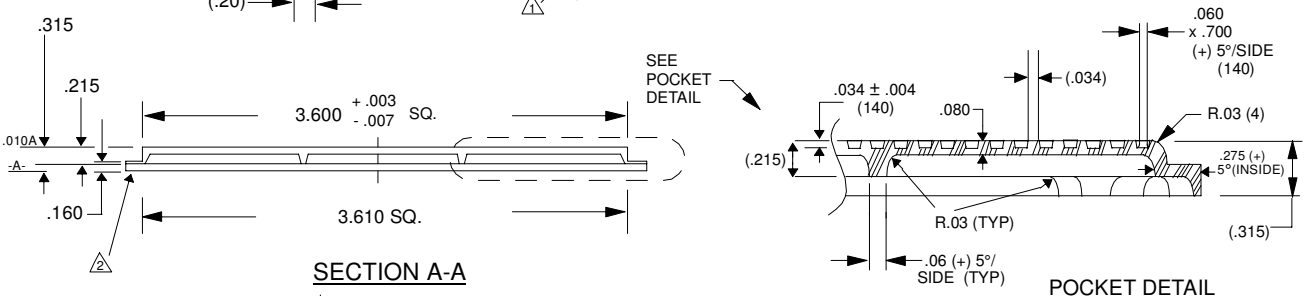
Coordinates		
Mark	X	Y
#1	8305.0	414.3
#2	-8305.0	414.3

Each mark is
50 µm by 50µm

3.4. DIE DIMENSIONSWaffle Pack Specification

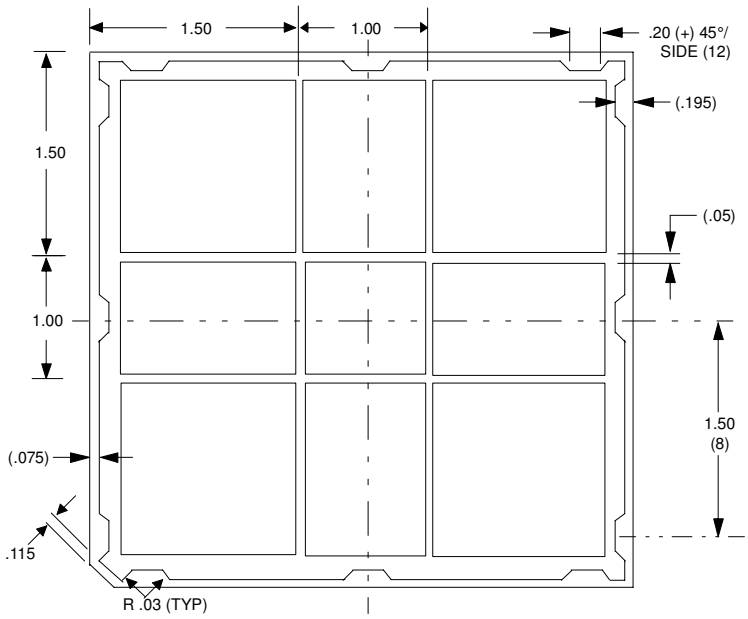


Capacity = 136 die



SECTION A-A

POCKET DETAIL



1. ENGRAVING TO BE .08 CHAR. X .01 WIDE X .002 RAISED. CENTER ON ℄
2. KNOCKOUTS NOT TO EXCEED .003 PAD
3. MATERIAL: ABS, Tan Static Protective ABS ChipSentry© ,Stat-PRO©400 -Build Tool to .006 IN./IN. SHRINK.

-66C02	ChipSentry©
-74DXX	Stat-PRO©400
Mat. Code	Mtr. & Engrvng

Tolerances Unless Otherwise Specified	Description: 4" CHIP TRAY - 140 rect. pockets
xx [.x] ± .01 [.3]	Part No.: H44-xxxx-XXXX
xxx [.xx] ± .005 [.13]	Material: SEE NOTE 3
xxxx [.xxx] ± .0005 [.013]	Drawing No.: V005-531
∠ ± 1/2°	DIMENSIONS IN INCHES [MILLIMETERS]

4. PAD INFORMATION
Input Bond Pad Coordinates

Pad #	Signal	x Coordinate (in μm)	y Coordinate (in μm)
1.1	EIO240#	7744.00	439.30
1.2	EIO240#	7616.00	439.30
2.1	D_{25}	7424.00	439.30
2.2	D_{25}	7296.00	439.30
3.1	D_{24}	7104.00	439.30
3.2	D_{24}	6976.00	439.30
4.1	D_{23}	6784.00	439.30
4.2	D_{23}	6656.00	439.30
5.1	D_{22}	6464.00	439.30
5.2	D_{22}	6336.00	439.30
6.1	D_{21}	6144.00	439.30
6.2	D_{21}	6016.00	439.30
7.1	D_{20}	5824.00	439.30
7.2	D_{20}	5696.00	439.30
8.1	D_{15}	5504.00	439.30
8.2	D_{15}	5376.00	439.30
9.1	LD240_1	5184.00	439.30
9.2	LD240_1	5056.00	439.30
10.1	V_0	4544.00	439.30
10.2	V_0	4416.00	439.30
11.1	V_8	3904.00	439.30
11.2	V_8	3776.00	439.30
12.1	Reserved	3584.00	439.30
12.2	Reserved	3456.00	439.30
13.1	D_{14}	3264.00	439.30
13.2	D_{14}	3136.00	439.30
14.1	D_{13}	2944.00	439.30
14.2	D_{13}	2816.00	439.30
15.1	DCLK	2624.00	439.30
15.2	DCLK	2496.00	439.30
16.1	V_{DDD}	2304.00	439.30
16.2	V_{DDD}	2176.00	439.30
17.1	V_{DDA}	1984.00	439.30
17.2	V_{DDA}	1856.00	439.30
18.1	V_7	1344.00	439.30
18.2	V_7	1216.00	439.30
19.1	V_2	704.00	439.30
19.2	V_2	576.00	439.30
20.1	V_5	384.00	439.30
20.2	V_5	256.00	439.30
21.1	V_4	64.00	439.30
21.2	V_4	-64.00	439.30
22.1	V_3	-256.00	439.30
22.2	V_3	-384.00	439.30
23.1	V_6	-576.00	439.30
23.2	V_6	-704.00	439.30
24.1	V_1	-1216.00	439.30
24.2	V_1	-1344.00	439.30
25.1	A_{GND}	-1856.00	439.30
25.2	A_{GND}	-1984.00	439.30
26.1	D_{GND}	-2176.00	439.30
26.2	D_{GND}	-2304.00	439.30
27.1	D_{12}	-2496.00	439.30
27.2	D_{12}	-2624.00	439.30
28.1	D_{11}	-2816.00	439.30
28.2	D_{11}	-2944.00	439.30
29.1	D_{10}	-3136.00	439.30
29.2	D_{10}	-3264.00	439.30
30.1	CLAMP#	-3456.00	439.30
30.2	CLAMP#	-3584.00	439.30
31.1	V_8	-3776.00	439.30
31.2	V_8	-3904.00	439.30

Table 4-1: WFP6530B Input Bond Pad Coordinates

Pad #	Signal	x Coordinate (in μm)	y Coordinate (in μm)
32.1	V_0	-4416.00	439.30
32.2	V_0	-4544.00	439.30
33.1	DATA_INV	-5056.00	439.30
33.1	DATA_INV	-5184.00	439.30
34.1	LP	-5376.00	439.30
34.2	LP	-5504.00	439.30
35.1	D_{05}	-5696.00	439.30
35.2	D_{05}	-5824.00	439.30
36.1	D_{04}	-6016.00	439.30
36.2	D_{04}	-6144.00	439.30
37.1	D_{03}	-6336.00	439.30
37.2	D_{03}	-6464.00	439.30
38.1	D_{02}	-6656.00	439.30
38.2	D_{02}	-6784.00	439.30
39.1	D_{01}	-6976.00	439.30
39.2	D_{01}	-7104.00	439.30
40.1	D_{00}	-7296.00	439.30
40.2	D_{00}	-7424.00	439.30
41.1	EIO1#	-7616.00	439.30
41.2	EIO1#	-7744.00	439.30

Table 4-1: WFP6530B Input Bond Pad Coordinates

4.1. Output Bond Pad Coordinate

Pad #	Signal	X (μm)	Y (μm)
42	VS1	-8365.0	-463.4
43	VS2	-8295.0	-463.4
44	VS3	-8225.0	-463.4
45	VS4	-8155.0	-463.4
46	VS5	-8085.0	-463.4
47	VS6	-8015.0	-463.4
48	VS7	-7945.0	-463.4
49	VS8	-7875.0	-463.4
50	VS9	-7805.0	-463.4
51	VS10	-7735.0	-463.4
52	VS11	-7665.0	-463.4
53	VS12	-7595.0	-463.4
54	VS13	-7525.0	-463.4
55	VS14	-7455.0	-463.4
56	VS15	-7385.0	-463.4
57	VS16	-7315.0	-463.4
58	VS17	-7245.0	-463.4
59	VS18	-7175.0	-463.4
60	VS19	-7105.0	-463.4
61	VS20	-7035.0	-463.4
62	VS21	-6965.0	-463.4
63	VS22	-6895.0	-463.4
64	VS23	-6825.0	-463.4
65	VS24	-6755.0	-463.4
66	VS25	-6685.0	-463.4
67	VS26	-6615.0	-463.4
68	VS27	-6545.0	-463.4
69	VS28	-6475.0	-463.4
70	VS29	-6405.0	-463.4
71	VS30	-6335.0	-463.4
72	VS31	-6265.0	-463.4
73	VS32	-6195.0	-463.4
74	VS33	-6125.0	-463.4
75	VS34	-6055.0	-463.4
76	VS35	-5985.0	-463.4
77	VS36	-5915.0	-463.4

Table 4-2:

Pad #	Signal	X (μm)	Y (μm)
78	VS37	-5845.0	-463.4
79	VS38	-5775.0	-463.4
80	VS39	-5705.0	-463.4
81	VS40	-5635.0	-463.4
82	VS41	-5565.0	-463.4
83	VS42	-5495.0	-463.4
84	VS43	-5425.0	-463.4
85	VS44	-5355.0	-463.4
86	VS45	-5285.0	-463.4
87	VS46	-5215.0	-463.4
88	VS47	-5145.0	-463.4
89	VS48	-5075.0	-463.4
90	VS49	-5005.0	-463.4
91	VS50	-4935.0	-463.4
92	VS51	-4865.0	-463.4
93	VS52	-4795.0	-463.4
94	VS53	-4725.0	-463.4
95	VS54	-4655.0	-463.4
96	VS55	-4585.0	-463.4
97	VS56	-4515.0	-463.4
98	VS57	-4445.0	-463.4
99	VS58	-4375.0	-463.4
100	VS59	-4305.0	-463.4
101	VS60	-4235.0	-463.4
102	VS61	-4165.0	-463.4
103	VS62	-4095.0	-463.4
104	VS63	-4025.0	-463.4
105	VS64	-3955.0	-463.4
106	VS65	-3885.0	-463.4
107	VS66	-3815.0	-463.4
108	VS67	-3745.0	-463.4
109	VS68	-3675.0	-463.4
110	VS69	-3605.0	-463.4
111	VS70	-3535.0	-463.4
112	VS71	-3465.0	-463.4
113	VS72	-3395.0	-463.4
114	VS73	-3325.0	-463.4
115	VS74	-3255.0	-463.4

Table 4-2:

Pad #	Signal	X (μm)	Y (μm)	Pad #	Signal	X (μm)	Y (μm)
116	VS75	-3185.0	-463.4	154	VS113	-525.0	-463.4
117	VS76	-3115.0	-463.4	155	VS114	-455.0	-463.4
118	VS77	-3045.0	-463.4	156	VS115	-385.0	-463.4
119	VS78	-2975.0	-463.4	157	VS116	-315.0	-463.4
120	VS79	-2905.0	-463.4	158	VS117	-245.0	-463.4
121	VS80	-2835.0	-463.4	159	VS118	-175.0	-463.4
122	VS81	-2765.0	-463.4	160	VS119	-105.0	-463.4
123	VS82	-2695.0	-463.4	161	VS120	-35.0	-463.4
124	VS83	-2625.0	-463.4	162	VS121	35.0	-463.4
125	VS84	-2555.0	-463.4	163	VS122	105.0	-463.4
126	VS85	-2485.0	-463.4	164	VS123	175.0	-463.4
127	VS86	-2415.0	-463.4	165	VS124	245.0	-463.4
128	VS87	-2345.0	-463.4	166	VS125	315.0	-463.4
129	VS88	-2275.0	-463.4	167	VS126	385.0	-463.4
130	VS89	-2205.0	-463.4	168	VS127	455.0	-463.4
131	VS90	-2135.0	-463.4	169	VS128	525.0	-463.4
132	VS91	-2065.0	-463.4	170	VS129	595.0	-463.4
133	VS92	-1995.0	-463.4	171	VS130	665.0	-463.4
134	VS93	-1925.0	-463.4	172	VS131	735.0	-463.4
135	VS94	-1855.0	-463.4	173	VS132	805.0	-463.4
136	VS95	-1785.0	-463.4	174	VS133	875.0	-463.4
137	VS96	-1715.0	-463.4	175	VS134	945.0	-463.4
138	VS97	-1645.0	-463.4	176	VS135	1015.0	-463.4
139	VS98	-1575.0	-463.4	177	VS136	1085.0	-463.4
140	VS99	-1505.0	-463.4	178	VS137	1155.0	-463.4
141	VS100	-1435.0	-463.4	179	VS138	1225.0	-463.4
142	VS101	-1365.0	-463.4	180	VS139	1295.0	-463.4
143	VS102	-1295.0	-463.4	181	VS140	1365.0	-463.4
144	VS103	-1225.0	-463.4	182	VS141	1435.0	-463.4
145	VS104	-1155.0	-463.4	183	VS142	1505.0	-463.4
146	VS105	-1085.0	-463.4	184	VS143	1575.0	-463.4
147	VS106	-1015.0	-463.4	185	VS144	1645.0	-463.4
148	VS107	-945.0	-463.4	186	VS145	1715.0	-463.4
149	VS108	-875.0	-463.4	187	VS146	1785.0	-463.4
150	VS109	-805.0	-463.4	188	VS147	1855.0	-463.4
151	VS110	-735.0	-463.4	189	VS148	1925.0	-463.4
152	VS111	-665.0	-463.4	190	VS149	1995.0	-463.4
153	VS112	-595.0	-463.4	191	VS150	2065.0	-463.4

Table 4-2: **Table 4-2:**

Pad #	Signal	X (μm)	Y (μm)
192	VS151	2135.0	-463.4
193	VS152	2205.0	-463.4
194	VS153	2275.0	-463.4
195	VS154	2345.0	-463.4
196	VS155	2415.0	-463.4
197	VS156	2485.0	-463.4
198	VS157	2555.0	-463.4
199	VS158	2625.0	-463.4
200	VS159	2695.0	-463.4
201	VS160	2765.0	-463.4
202	VS161	2835.0	-463.4
203	VS162	2905.0	-463.4
204	VS163	2975.0	-463.4
205	VS164	3045.0	-463.4
206	VS165	3115.0	-463.4
207	VS166	3185.0	-463.4
208	VS167	3255.0	-463.4
209	VS168	3325.0	-463.4
210	VS169	3395.0	-463.4
211	VS170	3465.0	-463.4
212	VS171	3535.0	-463.4
213	VS172	3605.0	-463.4
214	VS173	3675.0	-463.4
215	VS174	3745.0	-463.4
216	VS175	3815.0	-463.4
217	VS176	3885.0	-463.4
218	VS177	3955.0	-463.4
219	VS178	4025.0	-463.4
220	VS179	4095.0	-463.4
221	VS180	4165.0	-463.4
222	VS181	4235.0	-463.4
223	VS182	4305.0	-463.4
224	VS183	4375.0	-463.4
225	VS184	4445.0	-463.4
226	VS185	4515.0	-463.4
227	VS186	4585.0	-463.4
228	VS187	4655.0	-463.4
229	VS188	4725.0	-463.4

Table 4-2:

Pad #	Signal	X (μm)	Y (μm)
230	VS189	4795.0	-463.4
231	VS190	4865.0	-463.4
232	VS191	4935.0	-463.4
233	VS192	5005.0	-463.4
234	VS193	5075.0	-463.4
235	VS194	5145.0	-463.4
236	VS195	5215.0	-463.4
237	VS196	5285.0	-463.4
238	VS197	5355.0	-463.4
239	VS198	5425.0	-463.4
240	VS199	5495.0	-463.4
241	VS200	5565.0	-463.4
242	VS201	5635.0	-463.4
243	VS202	5705.0	-463.4
244	VS203	5775.0	-463.4
245	VS204	5845.0	-463.4
246	VS205	5915.0	-463.4
247	VS206	5985.0	-463.4
248	VS207	6055.0	-463.4
249	VS208	6125.0	-463.4
250	VS209	6195.0	-463.4
251	VS210	6265.0	-463.4
252	VS211	6335.0	-463.4
253	VS212	6405.0	-463.4
254	VS213	6475.0	-463.4
255	VS214	6545.0	-463.4
256	VS215	6615.0	-463.4
257	VS216	6685.0	-463.4
258	VS217	6755.0	-463.4
259	VS218	6825.0	-463.4
260	VS219	6895.0	-463.4
261	VS220	6965.0	-463.4
262	VS221	7035.0	-463.4
263	VS222	7105.0	-463.4
264	VS223	7175.0	-463.4
265	VS224	7245.0	-463.4
266	VS225	7315.0	-463.4
267	VS226	7385.0	-463.4

Table 4-2:

Pad #	Signal	X (μm)	Y (μm)
268	VS227	7455.0	-463.4
269	VS228	7525.0	-463.4
270	VS229	7595.0	-463.4
271	VS230	7665.0	-463.4
272	VS231	7735.0	-463.4
273	VS232	7805.0	-463.4
274	VS233	7875.0	-463.4
275	VS234	7945.0	-463.4
276	VS235	8015.0	-463.4
277	VS236	8085.0	-463.4
278	VS237	8155.0	-463.4
279	VS238	8225.0	-463.4
280	VS239	8295.0	-463.4
281	VS240	8365.0	-463.4
282	D5	8367.2	-204.6
283	D4	8367.2	-34.6
284	D3	8367.2	115.4
285	D2	8330.0	309.3
286	D1	8190.0	439.3
287	D6	-8190.0	439.3
288	D7	-8330.0	309.3
289	D8	-8367.2	115.4
290	D9	-8367.2	-34.6
291	D10	-8367.2	-204.6

Table 4-2:

5. DETAILED PAD DESCRIPTIONS

The following abbreviations are used for pad types in the following sections: (I) input; (O) output; (I/O) Input/Output, (#) active 'low' signal.

Name	Number	Type	Description
LD240_1	9	I	**LOAD DIRECTION:** Controls the direction in which the data is loaded into the Input Register: When LD240_1 = '0', data is loaded from Channel V_{S1} to V_{S240}. When LD240_1 = '1', data is loaded from Channel V_{S240} to V_{S1}.
EIO1#, EIO240#	41,1	I/O	**ENABLE IN/OUT**: The EIO1# and EIO240# active 'low' signals initiate the loading of data into the Input Register of the WFP6530B. When one of the EIOx# pads is configured as an input, the other is configured as an output, with the direction determined by the LD240_1 input (see Table 5-1). The EIOx# output pads are designed to be connected to the EIOx# input pads of adjacent devices to allow a series of drivers to operate sequentially. When a 'low' is applied to the EIOx# pin configured as an input on the first device in the series, data is loaded from the three sets of 6-bit Data Inputs into the first three 6-bit Input-Register locations. On subsequent transitions of the DCLK, data continues to be loaded into the remaining 6-bit Input-Register locations. When the register is full (240 words), the EIOx# pin configured as an output goes 'low', enabling the next driver. The data load sequence is summarized in Table 5-1, Figure 5-1 and Figure 5-2.

Table 5-1: Input/Output Selection for EIO1# and EIO240#

LD240_1 Input	EIO1#, EIO240# Functionality		Data Loading Sequence
	EIO1#	EIO240#	
'0'	Input	Output	Channel 1 to 240
'1'	Output	Input	Channel 240 to 1

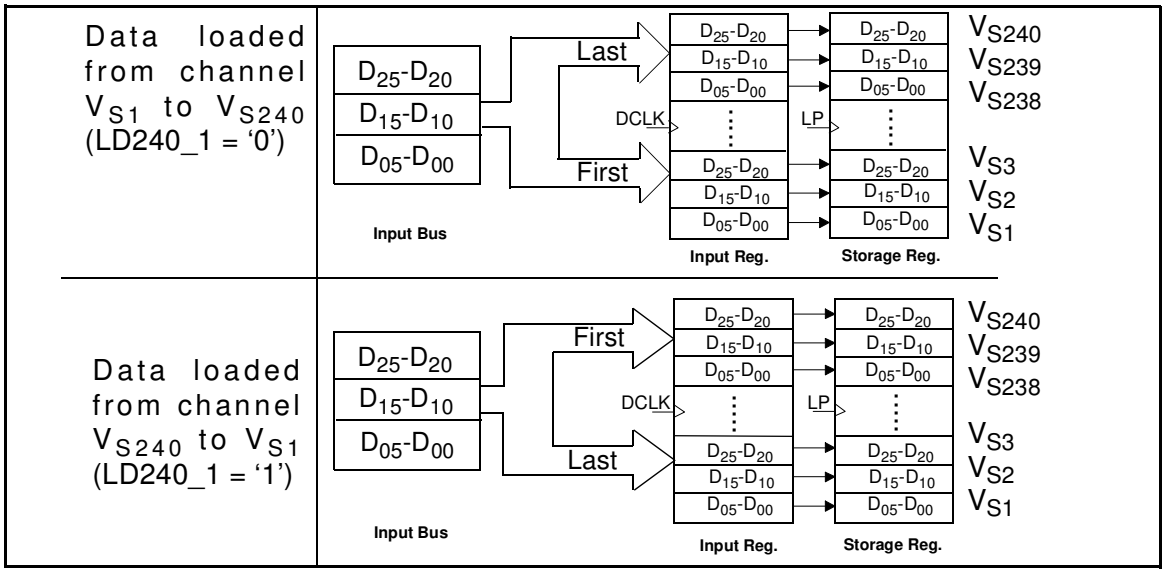


Figure 5–1. Display Data Sampling and Output Direction

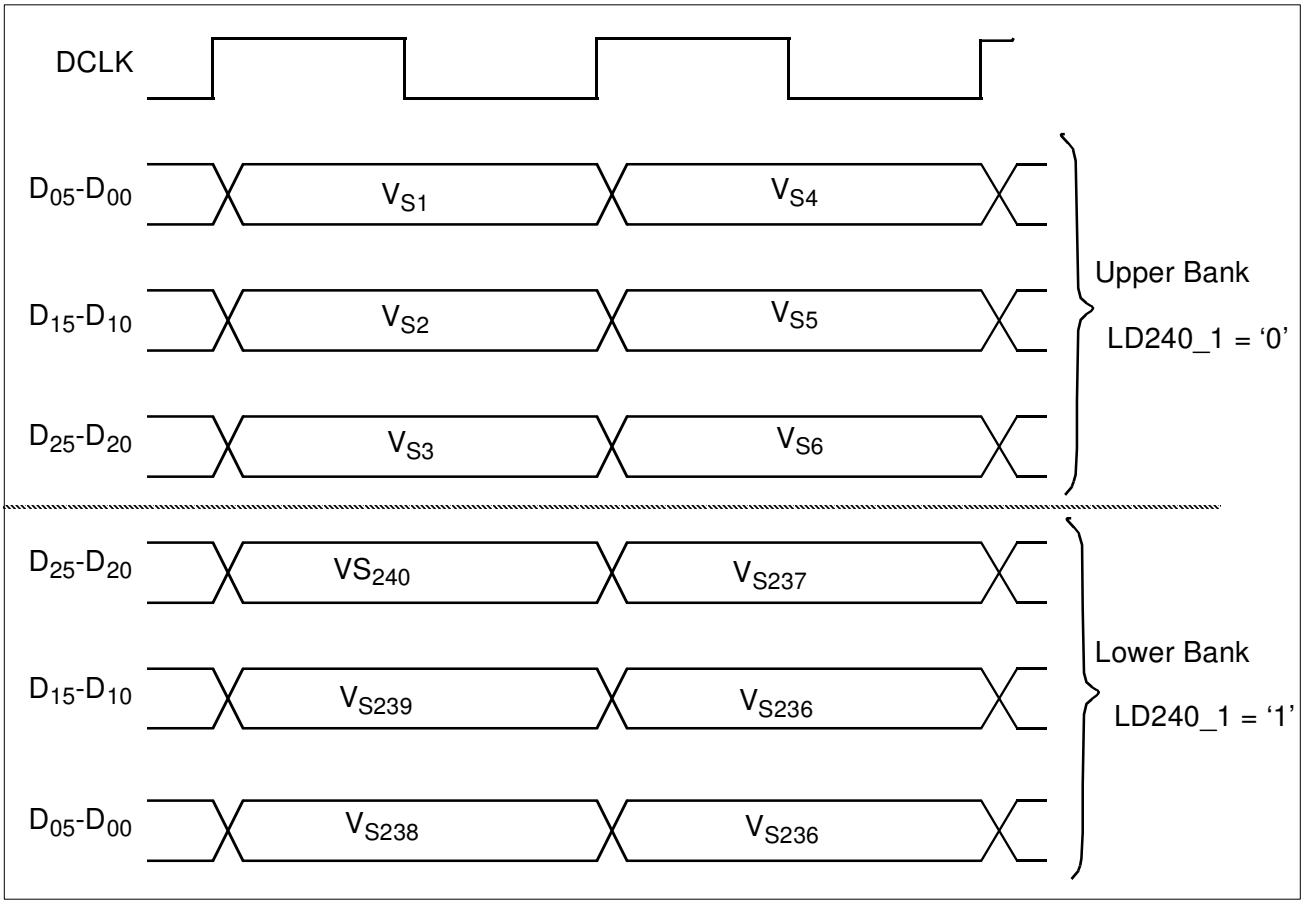


Figure 5–2. Display Data Channel Assignment and Output Sequence

Name	Number	Type	Description (*Cont.*)
V_{S1}-V_{S240}	42-282	O	**VOLTAGE OUTPUTS**: These outputs drive all 240 pixel inputs of the LCD simultaneously after the high-to-low transition of LP. Outputs are high impedance while LP is high.
D_{05}-D_{00} D_{15}-D_{10} D_{25}-D_{20}	35-40 8,13,14,27-29 2-7	I	**DATA**: The Data inputs consist of 6-bit words for each of three channels. At the falling edge of DCLK, three 6-bit words for three adjacent channels are loaded in parallel. Each data bit is represented as Dij where: i = 2-0 indicates the channel j = 5-0 indicates the significance of the bit in each word. D_{i5} indicates the MSB and D_{i0} indicates the LSB of the input word.
LP	34	I	**Latch Pulse**: When LP is asserted, the data is transferred from the Input Register into the Storage Register, and the selected analog voltages drive the LCD. Also, the EIOx# output is reset to the 'high' level.
DCLK	15	I	**DATA CLOCK**: Data is loaded into the input registers on the high-to-low transition of DCLK for 2xCLK= low and on both rising and falling edges of DCLK for 2xCLK = high.
CLAMP#	30	I	**CLAMP**: The CLAMP# input controls the active pulldown devices which are present on the DCLK and D_{00}-D_{25} inputs. When the CLAMP# signal drives low, these clamp devices connect DCLK and D_{00}-D_{25} to the WFP6530B's GND through a low impedance. **The CLAMP# pin should be connected to V_{DDD} in applications where level shifting is not used (i.e. when V_{COM} modulation is employed).**
V_{DDD}	16	I	**DIGITAL SUPPLY VOLTAGE**: Either 3.3 V or 5.0 V should be provided on this pin to supply digital power to the device.
V_{DDA}	17	I	**ANALOG SUPPLY VOLTAGE**: Up to 5.0 V should be provided on this pin to supply analog power to the device.
V_8 V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	11,31 18 23 20 21 22 19 24 10,32	I	**REFERENCE ANALOG VOLTAGE INPUTS:** These nine inputs are used to supply the adjustable-reference voltage inputs to the resistive-string DAC to provide the transmissivity-voltage response required for each type of LCD. Note: both V_8 pads must be connected to each other and to the same potential; also, both V_0 pads must be . connected to each other and to the same potential
A_{GND}	25	I	**ANALOG GROUND**
D_{GND}	26	I	**DIGITAL GROUND**

DATA_INV	33	I	**DATA INVERSION**: The data inversion input signal, when logic high, enables inversion of the input display data (D_{ij}). This pad should be tied “low” if data inversion is not used. See Figure 7-1 and 7-6 for timing information for this signal.
2xCLK	12	I	**2xCLK**: When logic high, the 2xCLK input enables sampling of input display data (D_{ij}) on both rising and falling edges of the DCLK input (see Figure 7-2). When logic low, input display data is sampled on the falling edge of DCLK only (see Figure 7-1).

Table 5-2: Input Data vs. Output Voltage

MSB	Display Data				LSB	Refer. Voltage	Output Voltage
D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0	0	0	0	V_0, V_0	V_0
0	0	0	0	0	1	V_0, V_1	$V_0 + 1/7 \times (V_1 - V_0)$
0	0	0	0	1	0	V_0, V_1	$V_0 + 2/7 \times (V_1 - V_0)$
0	0	0	0	1	1	V_0, V_1	$V_0 + 3/7 \times (V_1 - V_0)$
0	0	0	1	0	0	V_0, V_1	$V_0 + 4/7 \times (V_1 - V_0)$
0	0	0	1	0	1	V_0, V_1	$V_0 + 5/7 \times (V_1 - V_0)$
0	0	0	1	1	0	V_0, V_1	$V_0 + 6/7x (V_1 - V_0)$
0	0	0	1	1	1	V_0, V_1	V_1
0	0	1	0	0	0	V_1, V_2	$V_1 + 1/8 \times (V_2 - V_1)$
0	0	1	0	0	1	V_1, V_2	$V_1 + 2/8 \times (V_2 - V_1)$
0	0	1	0	1	0	V_1, V_2	$V_1 + 3/8 \times (V_2 - V_1)$
0	0	1	0	1	1	V_1, V_2	$V_1 + 4/8 \times (V_2 - V_1)$
0	0	1	1	0	0	V_1, V_2	$V_1 + 5/8 \times (V_2 - V_1)$
0	0	1	1	0	1	V_1, V_2	$V_1 + 6/8 \times (V_2 - V_1)$
0	0	1	1	1	0	V_1, V_2	$V_1 + 7/8 \times (V_2 - V_1)$
0	0	1	1	1	1	V_1, V_2	V_2
0	1	0	0	0	0	V_2, V_3	$V_2 + 1/8 \times (V_3 - V_2)$
0	1	0	0	0	1	V_2, V_3	$V_2 + 2/8 \times (V_3 - V_2)$
0	1	0	0	1	0	V_2, V_3	$V_2 + 3/8 \times (V_3 - V_2)$
0	1	0	0	1	1	V_2, V_3	$V_2 + 4/8 \times (V_3 - V_2)$
0	1	0	1	0	0	V_2, V_3	$V_2 + 5/8 \times (V_3 - V_2)$
0	1	0	1	0	1	V_2, V_3	$V_2 + 6/8 \times (V_3 - V_2)$
0	1	0	1	1	0	V_2, V_3	$V_2 + 7/8 \times (V_3 - V_2)$
0	1	0	1	1	1	V_2, V_3	V_3
0	1	1	0	0	0	V_3, V_4	$V_3 + 1/8 \times (V_4 - V_3)$
0	1	1	0	0	1	V_3, V_4	$V_3 + 2/8 \times (V_4 - V_3)$
0	1	1	0	1	0	V_3, V_4	$V_3 + 3/8 \times (V_4 - V_3)$
0	1	1	0	1	1	V_3, V_4	$V_3 + 4/8 \times (V_4 - V_3)$
0	1	1	1	0	0	V_3, V_4	$V_3 + 5/8 \times (V_4 - V_3)$
0	1	1	1	0	1	V_3, V_4	$V_3 + 6/8 \times (V_4 - V_3)$
0	1	1	1	1	0	V_3, V_4	$V_3 + 7/8 \times (V_4 - V_3)$
0	1	1	1	1	1	V_3, V_4	V_4
1	0	0	0	0	0	V_4, V_5	$V_4 + 1/8 \times (V_5 - V_4)$
1	0	0	0	0	1	V_4, V_5	$V_4 + 2/8 \times (V_5 - V_4)$
1	0	0	0	1	0	V_4, V_5	$V_4 + 3/8 \times (V_5 - V_4)$
1	0	0	0	1	1	V_4, V_5	$V_4 + 4/8 \times (V_5 - V_4)$
1	0	0	1	0	0	V_4, V_5	$V_4 + 5/8 \times (V_5 - V_4)$
1	0	0	1	0	1	V_4, V_5	$V_4 + 6/8 \times (V_5 - V_4)$
1	0	0	1	1	0	V_4, V_5	$V_4 + 7/8 \times (V_5 - V_4)$
1	0	0	1	1	1	V_4, V_5	V_5
1	0	1	0	0	0	V_5, V_6	$V_5 + 1/8 \times (V_6 - V_5)$
1	0	1	0	0	1	V_5, V_6	$V_5 + 2/8 \times (V_6 - V_5)$
1	0	1	0	1	0	V_5, V_6	$V_5 + 3/8 \times (V_6 - V_5)$
1	0	1	0	1	1	V_5, V_6	$V_5 + 4/8 \times (V_6 - V_5)$
1	0	1	1	0	0	V_5, V_6	$V_5 + 5/8 \times (V_6 - V_5)$
1	0	1	1	0	1	V_5, V_6	$V_5 + 6/8 \times (V_6 - V_5)$
1	0	1	1	1	0	V_5, V_6	$V_5 + 7/8 \times (V_6 - V_5)$
1	0	1	1	1	1	V_5, V_6	V_6
1	1	0	0	0	0	V_6, V_7	$V_6 + 1/8 \times (V_7 - V_6)$
1	1	0	0	0	1	V_6, V_7	$V_6 \times 2/8 \times (V_7 - V_6)$
1	1	0	0	1	0	V_6, V_7	$V_6 + 3/8 \times (V_7 - V_6)$
1	1	0	0	1	1	V_6, V_7	$V_6 + 4/8 X (V_7 - V_6)$
1	1	0	1	0	0	V_6, V_7	$V_6 + 5/8 \times (V_7 - V_6)$
1	1	0	1	0	1	V_6, V_7	$V_6 + 6/8 \times (V_7 - V_6)$
1	1	0	1	1	0	V_6, V_7	$V_6 + 7/8 \times (V_7 - V_6)$
1	1	0	1	1	1	V_6, V_7	V_7
1	1	1	0	0	0	V_7, V_8	$V_7 + 1/8 \times (V_8 - V_7)$
1	1	1	0	0	1	V_7, V_8	$V_7 + 2/8 \times (V_8 - V_7)$
1	1	1	0	1	0	V_7, V_8	$V_7 + 3/8 \times (V_8 - V_7)$
1	1	1	0	1	1	V_7, V_8	$V_7 + 4/8 \times (V_8 - V_7)$
1	1	1	1	0	0	V_7, V_8	$V_7 + 5/8 \times (V_8 - V_7)$
1	1	1	1	0	1	V_7, V_8	$V_7 + 6/8 \times (V_8 - V_7)$
1	1	1	1	1	0	V_7, V_8	$V_7 + 7/8 \times (V_8 - V_7)$
1	1	1	1	1	1	V_7, V_8	V_8

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DDD}	Digital Power Supply Voltage	-0.3	smaller of 6.0 or V_{DDA}	Volts	1,2,4
V_{DDA}	Analog Power Supply Voltage	-0.3	6.0	Volts	1,2,4
V_8 - V_0	Analog Reference Voltage Inputs	-0.3	V_{DDA} + 0.3	Volts	1,2
VS240-V_{S1}	Output Voltage	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{IN}	Voltage on any Digital Input	-0.3	V_{DDD} + 0.3	Volts	1,2,3
P_D	Operating Power Dissipation		300	mW	
T_A	Operating Temperature (Ambient Temperature under bias)	-10	85	°C	1
T_{STR}	Storage Temperature	-20	85	°C	1

NOTES: 1) Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicat ed in the operational ratings of this specification is not implied. Exposure to absolute maxi mum rating conditions for extended periods may affect system reliability.

2) All voltages are with respect to ground (GND) unless otherwise noted.

3) For D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, DCLK, LP, CLAMP#, EIO1#, EIO240# and LD240_1 input pads.

4) **V_{DDA} must be greater than or equal to V_{DDD} for proper circuit operation**. For this reason, V_{DDA} should be powered on first (or at the same time as V_{DDD}). Also, V_{DDD} should be powered off first, or at same time as V_{DDA}.

6.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDD}	Digital Supply Voltage	3.0 4.5	3.3 5.0	3.6 5.5	Volts Volts	1 1
V_{DDA}	Analog Supply Voltage	4.5	5.0	5.5	Volts	1
T_A	Ambient Temperature	0	25	70	°C	
V_8 - V_0	Analog Reference Voltage	0		V_{DDA}	Volts	1, 2
I_{REF}	Analog Reference Current			20	mA	

NOTES: 1) All voltages are with respect to ground (GND) unless otherwise noted.
2) Case I: $V_{DDA} \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0$
Case II: $V_{DDA} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8$

6.3 DC Characteristics (Preliminary data – subject to change)

V_{DDA} = 5 V ± 0.5 V, T_A = 25° C, unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions	Note
V_S	Analog Output Voltage				VDDA-0.03	Volts		1
V_{ST}	Analog Output Transition Band				$\|V_8-V_0\|$	Volts		
V_{ERR}	Analog Output Error Voltage		-0.15		+0.15	LSB		2
V_{IH}	Logic Input high Voltage		$0.8V_{DDD}$			Volts		3
V_{IL}	Logic Input low Voltage				$0.2V_{DDD}$	Volts		3
V_{OH}	Logic Output high Voltage		V_{DDD} - 0.4			Volts	I_{OH} = - 0.4 mA	4
V_{OL}	Logic Output low Voltage				0.4	Volts	I_{OL} = 0.4 mA	4
I_{QR}	Reference Quiescent Current		2.8	3.1	3.4	mA		5
I_{DDA}	Analog Supply Current				400	µA	V_{DDA} = 5.0 V	6
I_{DDD}	Digital-Supply Current (active)			3.8 6.4	7 10	mA mA	V_{DDD} = 3.3 V V_{DDD} = 5.0 V	6
I_{DDD}	Digital-Supply Current (Stand-by)			80 200	400 600	µA µA	V_{DDD} = 3.3 V V_{DDD} = 5.0 V	7
I_{IN}	Input Leakage Current		-5		+5	µA	$0 < V_{IN} < V_{DDD}$	
C_{IN}	Input Capacitance				5	pF		
R_{String}	String Resistance	V0-V1	213	304	395	Ω		
		V1-V2	151	216	281			
		V2-V3	129	184	239			
		V3-V4	129	184	239			
		V4-V5	129	184	239			
		V5-V6	129	184	239			
		V6-V7	151	216	281			
		V7-V8	241	344	447			
R_{OUT}	Output Resistance							
	V0-V1 (at code 3)				24.5	kΩ		8
	V1-V2 (at code 11)				18.1			
	V2-V3 (at code 19)				15.6			
	V3-V4 (at code 27)				15.6			
	V4-V5 (at code 35)				15.6			
	V5-V6 (at code 43)				15.6			
	V6-V7 (at code 51)				18.1			
	V7-V8 (at code 59)				28.1			

NOTES: 1) See Table 5-2 for digital code-Voltage relationship.

2) For all codes. Error is difference between measured voltage & Table 5-2 value.

NOTES: **cont'd**

3) DCLK, LP, CLAMP#, D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, EIO1#, EIO240#, and LD240_1 inputs
4) EIO1# and EIO240# outputs
5) Quiescent current between V_0 and V_8 with $|V_0-V_8|$ = 5.0 V and all other references floating
6) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is loading ,100% of data lines toggle each DCLK cycle
7) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is not loading,100% of data lines toggle each DCLK cycle.
8) Effective output resistance at output with highest resistance when all outputs drive the same code. See Figure 6-5.

6.4 AC Characteristics (V_{DDD} = 3.3 V ± 0.3 V) – (Preliminary data – subject to change)

See Figures 7-2 and 7-3 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min	Typical	Max	Units	Note
f_{CLK}	Guaranteed DCLK frequency	65			MHz	
t_{CLK}	DCLK period	15.4			ns	
t_{2xCLK}	DCLK period (2xCLK mode)	30.8			ns	
t_1	DCLK high pulse width	6			ns	
t_2	DCLK low pulse width	6			ns	
t_3	DCLK, LP rise time			10	ns	
t_4	DCLK, LP fall time			10	ns	
t_5	Data, DATA_INV setup time to DCLK Falling Edge	4			ns	
t_6	Data, DATA_INV hold time from DCLK Falling Edge	8			ns	
t_7	LP high pulse width	50			ns	2
t_8	Enable-In setup time to DCLK	4			ns	
t_9	Enable-Out low delay from DCLK			10	ns	1
t_{10}	DCLK low LP high	50			ns	
t_{11}	LP low to DCLK high	50			ns	
t_{12}	Data, DATA_INV setup time to DCLK Rising Edge	4			ns	
t_{13}	Data, DATA_INV hold time from DCLK Rising Edge	8			ns	

NOTES: 1) C_{LOAD} = 15 pF (See Figure 7-4)

2) LP width should not be wider than necessary since outputs don't drive to the next value until LP is low.

6.5 AC Characteristics (V_{DDD} = 5.0 V ± 0.5 V) – (Preliminary data – subject to change)

See Figures 7-2 and 7-3 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min	Typical	Max	Units	Note
f_{CLK}	Guaranteed DCLK frequency	65			MHz	
t_{CLK}	DCLK period	15.4			ns	
t_{2xCLK}	DCLK period (2xLCK mode)	30.8			ns	
t_1	DCLK high pulse width	6			ns	
t_2	DCLK low pulse width	6			ns	
t_3	DCLK, LP rise time			10	ns	
t_4	DCLK, LP fall time			10	ns	
t_5	Data, DATA_INV setup time to DCLK Falling Edge	4			ns	
t_6	Data, DATA_INV hold time from DCLK Falling Edge	8			ns	
t_7	LP high pulse width	40			ns	2
t_8	Enable-In setup time to DCLK	4			ns	
t_9	Enable-Out low delay from DCLK			10	ns	1
t_{10}	DCLK low to LP high	40			ns	
t_{11}	LP low to DCLK high	40			ns	
t_{12}	Data, DATA_INV setup time to DCLK Rising Edge	4			ns	
t_{13}	Data, DATA_INV hold time from DCLK Rising Edge	8			ns	

NOTES: 1) C_{LOAD} = 15 pF (See Figure 7-4).

2) LP width should not be wider than necessary since outputs don't drive to the next value until LP is low.

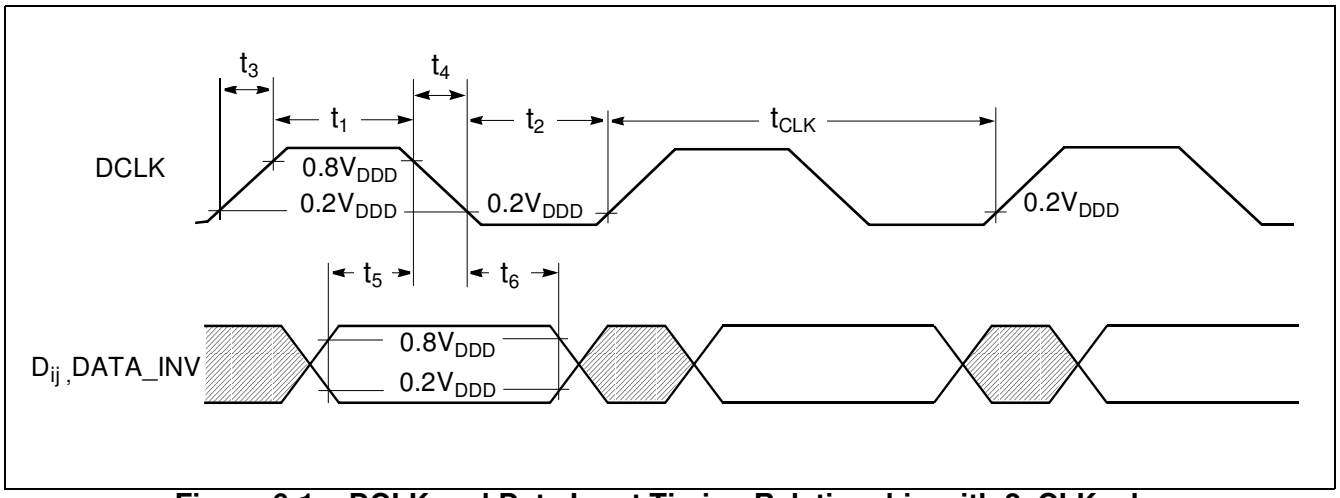


Figure 6-1: DCLK and Data Input Timing Relationship with 2xCLK = low

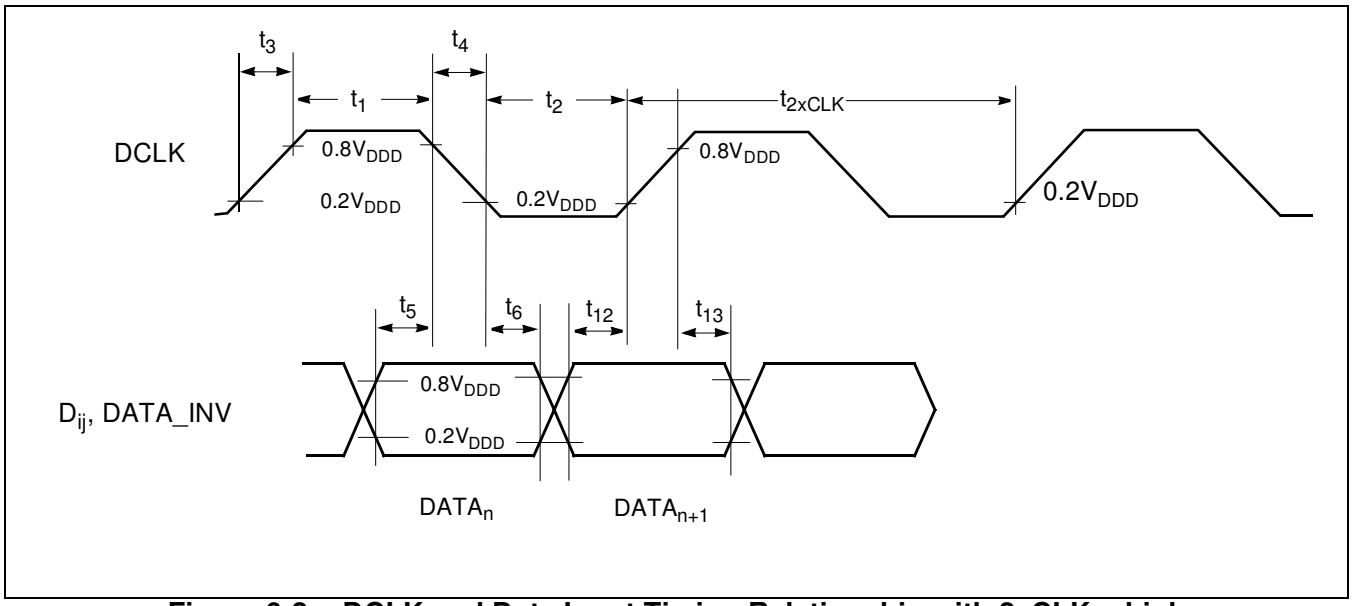


Figure 6-2: DCLK and Data Input Timing Relationship with 2xCLK = high

Note: When 2xCLK = high, the first rising edge of DCLK after LP falling edge clocks in the first display data word

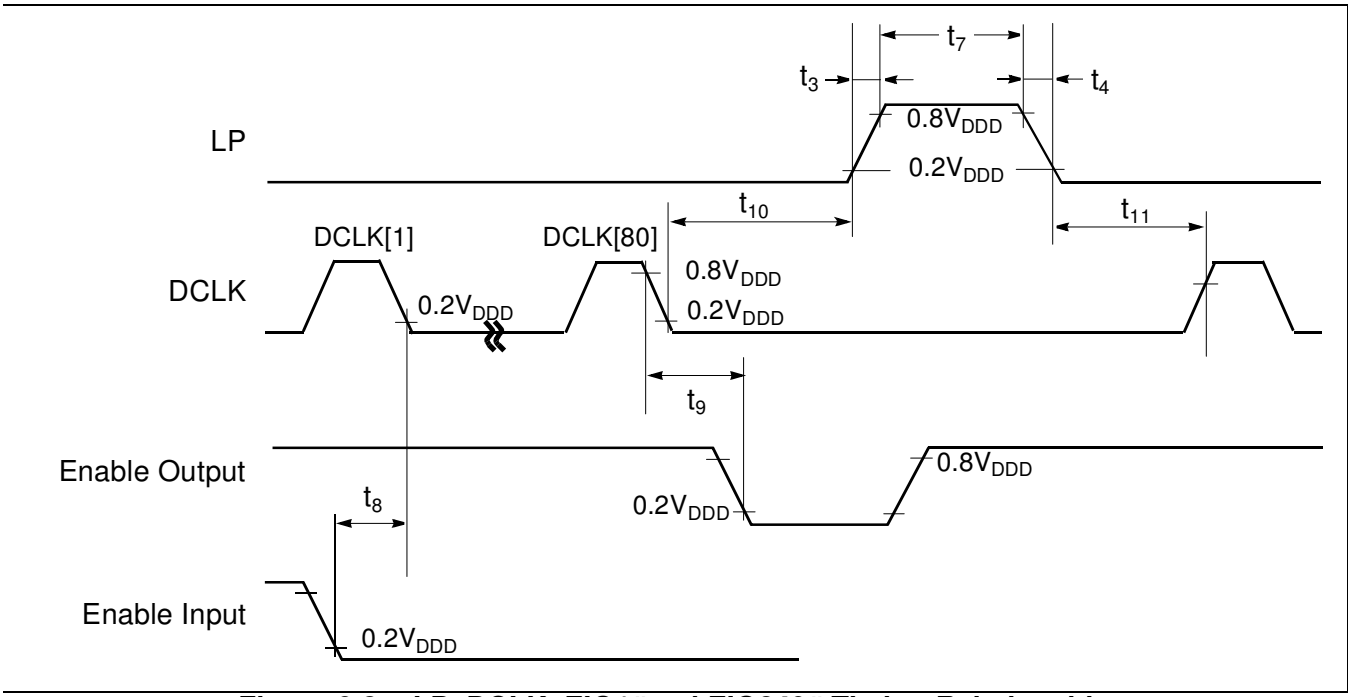


Figure 6-3: LP, DCLK, EIO1#and EIO240# Timing Relationship

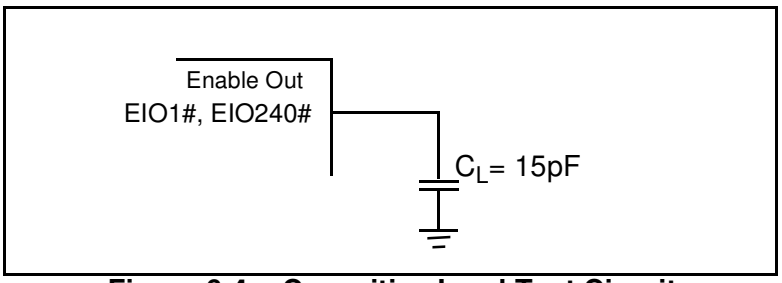


Figure 6-4: Capacitive Load Test Circuit

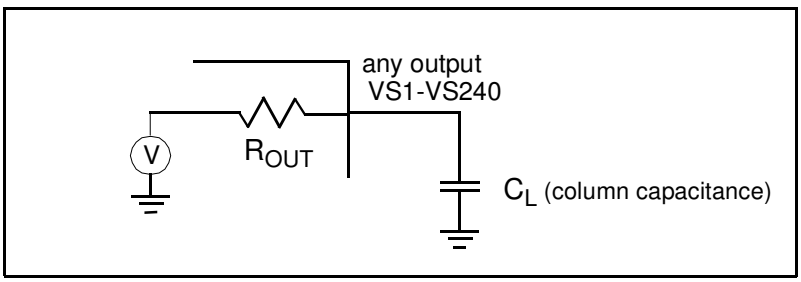


Figure 6-5: R_{OUT} Definition

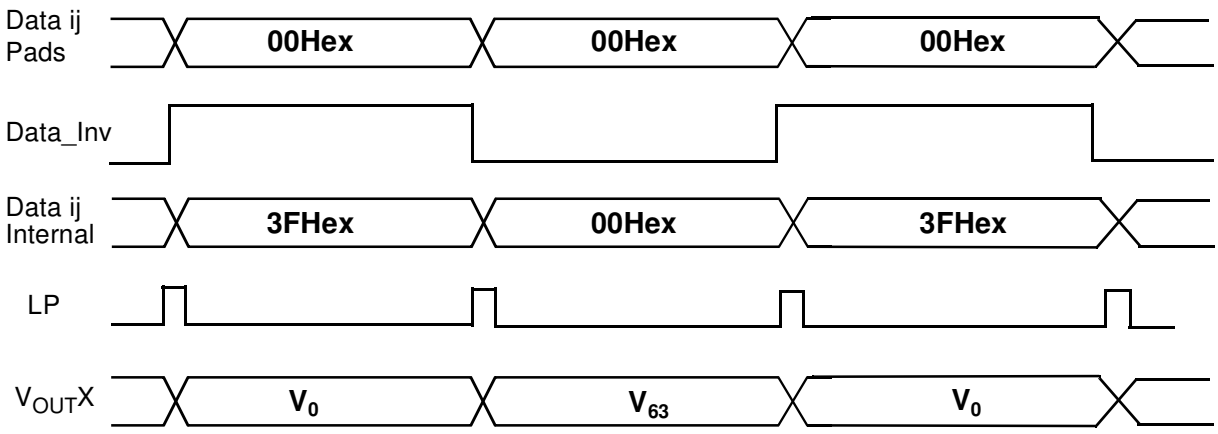


Figure 6-6: Data Inversion Example

Updates from Previous Version

Date of Issue	Page	Description
Feb. 18, 1996	2,4	Die Size Corrected
	4	Bump Height Spec Corrected
	3	Resistor String Values in Table 2-1 & Figure 2-1
	21	Voltage-Code table reflect new r-string val
	30	R_{String},R_{OUT}, I_{QR}
	30	V_{ERR} spec and Note 2
	32-34	Add t_{2xCLK} spec for 2xCLK mode

Updates from Previous Version

Date of Issue	Page	Description
Oct. 8, 1996	2,4	Change die size
	5	Change max bump hardness to 80 HV
	4,5,11	Decription of additional dummy bumps D1-D14
	25	Replace Figure 6-5 to show definition of R_{OUT}.