



VT83C572

PCI TO USB CONTROLLER

Preliminary Release 0.65
DATE : JAN.uly 1023, 19976

VIA TECHNOLOGIES, INC.

PRELIMINARY DOCUMENT RELEASE

The material in this document supersedes all previous documentation issued for any of the products included herein. Please contact VIA Technologies for the latest documentation.

Copyright Notice:

Copyright © 1995, 1996 Via Technologies Incorporated. Printed in Taiwan. ALL RIGHTS RESERVED.

No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise without the prior written permission of Via Technologies Incorporated.

Windows 95™ and Plug and Play™ are registered trademarks of Microsoft Corp.
PCI™ is a registered trademark of the PCI Special Interest Group.
All trademarks are the properties of their respective owners.

Disclaimer Notice:

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable to the publication date of this document. However, VIA Technologies assumes no responsibility for any errors in this document. Furthermore, VIA Technologies assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

Offices:

5020 Brandin Court
Fremont, CA 94538
USA

Tel: (510) 683-3300
Fax: (510) 683-3301

8th Floor, No. 533
Chung-Cheng Rd., Hsin-Tien
Taipei, Taiwan ROC

Tel: (886-2) 218-5452
Fax: (886-2) 218-5453

VIA VT83C572 PCI TO USB CONTROLLER

FEATURES

*** Universal Serial Bus Interface**

- USB specification v.1.0 compatible
- Intel UHCI (Universal Host Controller Interface) v.1.1 register compatible
- Legacy keyboard and PS2 mouse support
- Root hub and two down stream function ports
- Integrated physical layer transceivers
- Normal and low power operating mode
- Operable in both USB-aware (Windows-95 and NT) and USB legacy BIOS support
- Inter-operable with major USB peripherals

*** PCI Interface**

- PCI specification v.2.1 compliant
- Supports advanced PCI commands
- Multi-level data FIFOs with full scatter and gather capabilities

*** 0.5um high speed low power CMOS process**

*** Single chip 100-pin PQFP device**

VT83C572 CONFIGURATION REGISTERS

The VT83C572 PCI to USB controller is fully compatible with the UHCI specification v.1.1. There are two sets of software accessible registers -- PCI configuration registers and USB I/O registers. The USB I/O registers are defined in the UHCI v.1.1 specification.

PCI Configuration Registers

Offset	Function
1-0	Vendor ID : 1106h (read only)
3-2	Device ID : 3038h (read only)
5-4	Command Register
	bit 15-8: reserved
	bit 7: Address stepping, default: enabled
	bit 6-5: reserved
	bit 4: Memory write and invalidate, default: disabled
	bit 3: Fixed at 0 (special cycles)

- bit 2: Bus master, default: disabled
- bit 1: Memory space, default: disabled
- bit 0: I/O space, default: disabled

- 7-6 Status Register
 - bit 15: reserved
 - bit 14: Signaled system error
 - bit 13: Received master abort
 - bit 12: Received target abort
 - bit 11: Signaled target abort
 - bit 10-9: DEVSEL# timing: fixed at 01 (medium)
 - bit 8-0: reserved

- 08 Revision ID.

- B-9 Class Code Register: Fixed at 0C0300h to indicate the USB Controller

- 0C Cache Line Size Default: 00h

- 0D Latency Timer Default: 16h

- 0E Header Type = 00h (read only)

- 0F BIST Fixed at 00

- 23-20 Base address for **UHCI v1.1** compliant USB IO Registers
 - bit 31-16: reserved
 - bit 15-5: Port address for the base USB IO Registers, corresponding to AD[15:5]
 - bit 4-0: 00001b

- 3C Interrupt Line

- 3D Interrupt Pin, Default = 01h

- 3E-3F reserved

- 40 Misc. Control Register 1
 - bit 7: PCI Memory Command Option
 - 0 - Support Memory Read Line, Memory Read Multiple, Memory Write and Invalidate
 - 1 - Only support Memory Read, Memory Write Commands
 - bit 6: Babble Option
 - 0 - Automatically disable babbled port when EOF babble occurs.
 - 1 - Don't disable babbled port.
 - bit 5: PCI Parity Check Option
 - 0 - Disable PERR generation
 - 1 - Enable parity check and PERR generation
 - bit 4: reserved
 - bit 3: USB Data Length Option
 - 0 - Support TD length up to 1280.
 - 1 - Support TD length up to 1023.
 - bit 2: USB Power Management
 - 0 - Disable USB power management
 - 1 - Enable USB power management
 - bit 1: DMA Option
 - 0 - 16DW burst access
 - 1 - 8DW burst access

- bit 0: PCI Wait State
 - 0 - Zero wait
 - 1 - One wait

- 41 Misc. Control Register 2
 - bit7-3: reserved
 - bit 2: Trap Option
 - 0 - Set trap 60/64 status bits without checking enable bits.
 - 1 - Set trap 60/64 status bits only when trap 60/64 enable bits are set.
 - bit 1: A20gate Pass Through Option
 - 0 - Pass through A20GATE command sequence defined in UHCI.
 - 1 - Don pass through Write I/O port 64
 - bit 0: reserved

- 42-5F reserved

- 60 Serial Bus Release Number fixed at 10h

- C0-C1 Legacy Support Register (compliant with **UHCI v1.1** specification)
Default=2000h

USB I/O Registers (UHCI v1.1 Compliant)

Offset	Function
1-0	USB Command
3-2	USB Status
5-4	USB Interrupt Enable
7-6	Frame Number
B-8	Frame List Base Address
0C	Start Of Frame Modify
11-10	Port 1 Status/Control
13-12	Port 2 Status/Control

VT83C572 PIN DESCRIPTION

Signal Name	Pin No.	I/O	Signal Description
PCI Bus Interface			
AD[31:0]	98-100, 1-5, 9-14, 17-19, 31, 32, 34-36, 38, 39, 41, 42, 44-47, 49, 50	B	PCI Address/Data Bus: The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE#[3:0]	7, 20, 33, 40	B	Command/Byte Enable..
IDSEL	8	I	Initialization Device Select.
FRAME#	21	B	PCI Bus Frame Indicator.
IRDY#	22	B	Initiator Ready Indicator.
TRDY#	23	B	Target Ready.
DEVSEL#	24	B	Device Select.
STOP#	26	B	Stop Indicator.
PAR	30	B	Parity.
PERR#	27	B	PCI Bus Parity Error.
SERR#	28	I	System Error.
LOCK#	29	B	PCI Bus Lock.
REQ#	97	O	PCI bus request to the bus arbiter.
GNT#	96	I	PCI bus grant from the bus arbiter.
INTA #	95	I	PCI Interrupt Request.
PCLK	93	I	PCI Bus Clock.
PCIRST#	92	O	PCI Reset: An active low reset signal for the PCI bus.
Universal Serial Bus Interface			
SD0+	88	B	USB Port 0 Data
SD0-	89	B	USB Port 0 Data
SD1+	84	B	USB Port 1 Data
SD1-	85	B	USB Port 1 Data
X1	71	I	USB Clock input, connected to 48Mhz oscillator or crystal input.
X2	70	O	USB 48Mhz crystal connection. Leave unconnected if oscillator is used.
<u>OC1#</u>	<u>52</u>	<u>I</u>	<u>Overcurrent detection pin of port 1, tie to high if no external detection circuit.</u>
<u>OC0#</u>	<u>53</u>	<u>I</u>	<u>Overcurrent detection pin of port 0, tie to high if no external detection circuit.</u>
<u>PWRON1#</u>	<u>56</u>	<u>O</u>	<u>USB bus power switch of port 1, normal low</u>
<u>PWRON0#</u>	<u>57</u>	<u>O</u>	<u>USB bus power switch of port 0, normal low</u>
CPU Interface			
SMI#	51	O	System Management Interrupt to the processor for legacy keyboard and mouse support.
Power and Ground			
VDD	6, 16, 43, 54, 63, 73, 82, 90, 94	I	Power Supply of 4.5 to 5.5V.
VSS	15, 25, 37, 48, 55, 69, 72, 83, 91	I	Ground

VDDA	87	I	USB Differential Output Power Source
VSSA	86	I	USB Differential Output Ground

VT83C572 PIN OUT IN NUMERICAL ORDER

No. No.

Pin	Pin Name No.	Pin	Pin Name No.	Pin	Pin Name No.	Pin	Pin Name
1	AD28	31	AD14	51	SMI#	81	NC
2	AD27	32	AD13	52	OC1#NC	82	VDD
3	AD26	33	CBE1#	53	OC0#NC	83	VSS
4	AD25	34	AD12	54	VDD	84	SD1+
5	AD24	35	AD11	55	VSS	85	SD1-
6	VDD	36	AD10	56	PWRON1#NC	86	VSSA
7	CBE3#	37	VSS	57	PWRON0#NC	87	VDDA
8	IDSEL	38	AD9	58	NC	88	SD0+
9	AD23	39	AD8	59	NC	89	SD0-
10	AD22	40	CBE0#	60	NC	90	VDD
11	AD21	41	AD7	61	NC	91	VSS
12	AD20	42	AD6	62	NC	92	PCIRST#
13	AD19	43	VDD	63	VDD	93	PCLK
14	AD18	44	AD5	64	NC	94	VDD
15	VSS	45	AD4	65	NC	95	INTA#
16	VDD	46	AD3	66	NC	96	GNT#
17	AD17	47	AD2	67	NC	97	REQ#
18	AD16	48	VSS	68	NC	98	AD31
19	AD15	49	AD1	69	VSS	99	AD30
20	CBE2#	50	AD0	70	X2	100	AD29
21	FRAME#			71	X1		
22	IRDY#			72	VSS		
23	TRDY#			73	VDD		
24	DEVSEL#			74	NC		
25	VSS			75	NC		
26	STOP#			76	NC		
27	PERR#			77	NC		
28	SERR#			78	NC		
29	LOCK#			79	NC		
30	PAR			80	NC		

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	°C
Storage temperature	-55	125	°C
Input voltage	-0.5	5.5	Voltage
Output voltage ($V_{DD} = 5V$)	-0.5	5.5	Voltage
Output voltage ($V_{DD} = 3.1 - 3.6V$)	-0.5	$V_{DD} + 0.5$	Voltage

Note :

Stress above these listed cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA=0-70°C, $V_{DD}=5V\pm 5\%$, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low voltage	-.50	0.8	V	
VIH	Input high voltage	2.0	$V_{DD}+0.5$	V	
VOL	Output low voltage	-	0.45	V	$I_{OL}=4.0mA$
VOH	Output high voltage	2.4	-	V	$I_{OH}=-1.0mA$
IIL	Input leakage current	-	+/-10	uA	$0 < V_{IN} < V_{DD}$
IOZ	Tristate leakage current	-	+/-20	uA	$0.45 < V_{OUT} < V_{DD}$
ICC	Power supply current	-	80	mA	

100-PIN PLASTIC RECTANGULAR FLAT PACKAGE

