TelCom

TelCom Semiconductor, Inc.

1995 DATA BOOK

Mixed Signal

Power Management

Smart Sensors

- Mixed Signal
- Power Management
- Smart Sensors

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Life Support Policy

TelCom products are not authorized for use as critical components in life-support devices or systems, without the express written approval of the president of TelCom Semiconductor, Inc.

TelCom Semiconductor reserves the right to make changes in the circuitry and specifications of its devices and advises its customers to obtain the latest version of relevant information.

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TelCom Semiconductor serves a broad market spectrum of customers with a focus on analog components for commercial, high volume, standard product applications. Our product direction includes proprietary and commodity integrated circuits in high performance mixed-signal, power management and smart sensor devices.

TelCom's core business is in mixed-signal products. This family consists of multiple precision signal processing products including: display and system A/D converters, V/F and F/V converters, precision Op-Amps and voltage references. Characteristics of this family are low power, cost effectiveness, precision, and high noise rejection/ reduction.

TelCom's growth and flagship product line is power management integrated circuits. Included in this family are DC-to-DC converters, voltage detectors, low dropout voltage regulators and power MOSFET motor and PIN drivers. These devices interface to a wide range of voltage levels to directly drive motors, power MOSFETs, IGBTs, bipolar transistors and inductive loads.

TelCom's emerging smart sensor family includes solid-state thermal management and battery charger control ICs. Our solid-state temperature sensors protect sensitive components such as microprocessors, power supplies, motor drives, and laser diodes from thermal runaway, and control temperature in process control applications. TelCom's battery charger control ICs are designed for fast charging of one to ten NiCad or NIMH batteries.

TelCom Semiconductor is committed to delivering products which meet or exceed the quality and reliability expectations of our customers. TelCom Semiconductor's product assurance programs ensure compliance to customer driven quality requirements and provide for continuous improvement.

PRODUCT PORTFOLIO

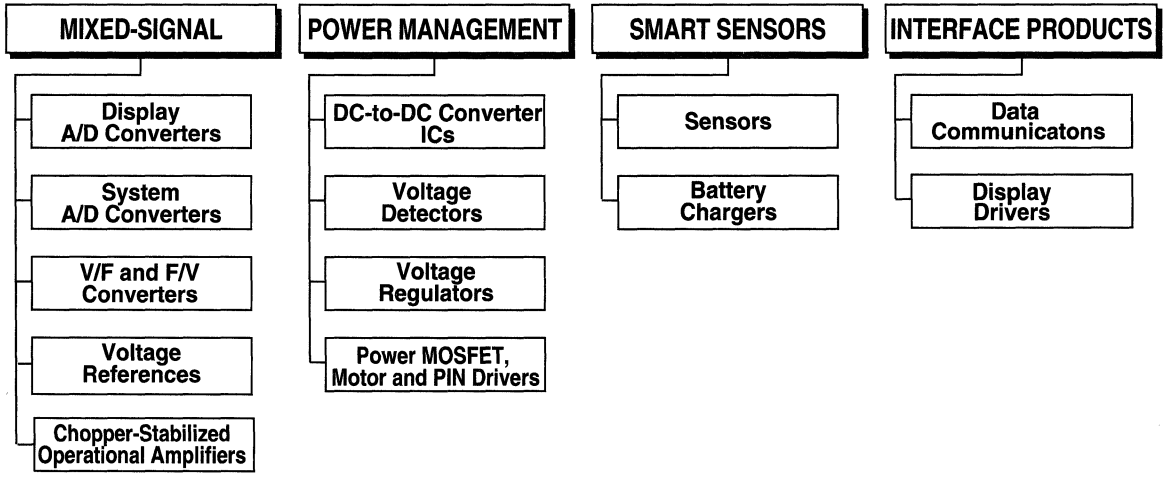


Table of Contents

ORDERING INFORMATION

1. **Order Entry**
   Orders for products contained herein should be directed to the appropriate TelCom representative or distributor. Please contact TelCom Semiconductor, 1300 Terra Bella Avenue, Mountain View, California 94039, phone: 1-800-888-9966 for a referral.

2. **Ordering Information**
   Each Item must be ordered using the complete part number exactly as listed on the data sheet.

3. **Part Number Explanation**
   For all TelCom Semiconductor voltage detectors, regulators and non-charge pump DC/DC converters:

ORDERING INFORMATION

PART CODE **TC XX XX XX XX X X X XXX**

TelCom Semiconductor Device

Product Part Number

Variation / Option

Output Voltage, or Detect Voltage (if applicable)

Extra feature Code and/or Tolerance

Operating Temperature Range:
E: Extended Range (– 40°C to +85°C)

Package Type (see listing page 1-9 and specific data sheet)

Number of package pins (see listing page 1-9 and specific data sheet)

Taping Direction:
713: Right Taping, 723: Left Taping, No Suffix: TO-92 Bulk

For all other TelCom Semiconductor devices:

ORDERING INFORMATION

PART CODE **TC XXXXXX X X X X XXX**

TelCom Semiconductor Device

Product Part Number (2 to 6 characters, see specific data sheet)

Electrical Performance
Grade Option (if applicable)
A: } Test selection criteria, see specific data sheet
B: }
R: Reverse pin layout

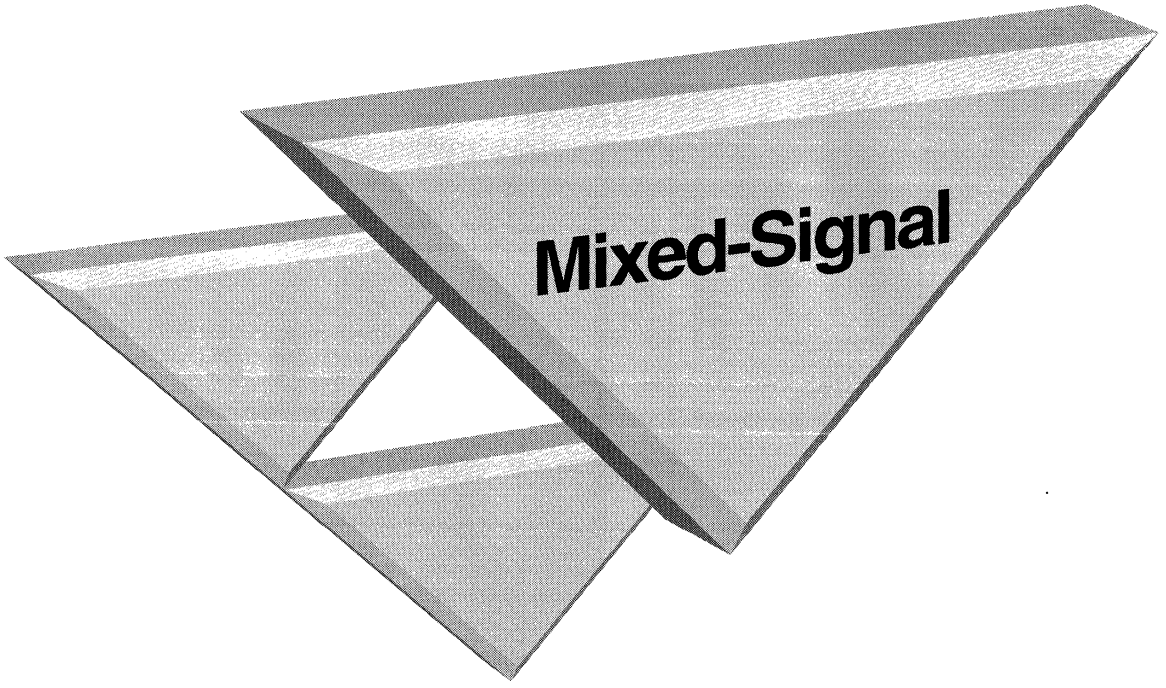
Operating Temperature Range:
C: Commercial Range (0°C to +70°C)
E: Extended Range (– 40°C to +85°C)
I: Industrial Range (– 25°C to +85°C)
M: Military Range (– 55°C to +125°C)

Package Type (see listing page 1-9 and specific data sheet)

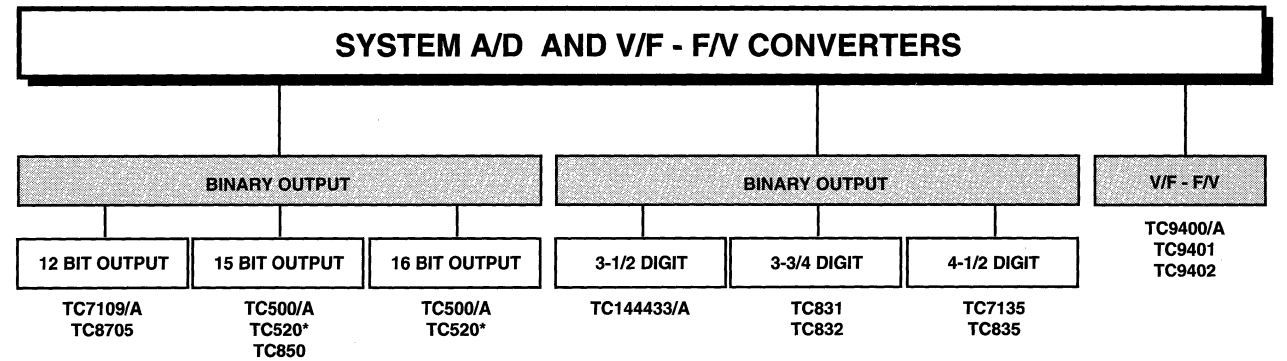
Number of Package Pins (see listing page 1-9 and specific data sheet)

Taping Direction:
713: Right Taping, 723: Left Taping, No Suffix: TO-92 Bulk

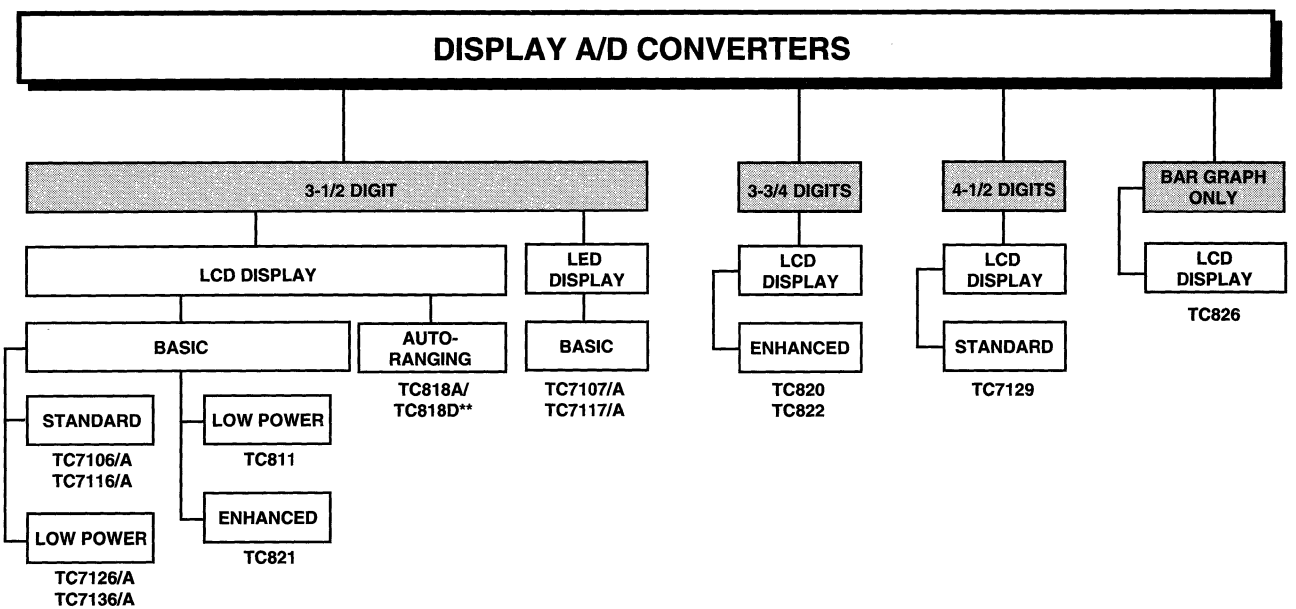
Package Type	Number of Package Pins
A TO-220	**A** 8
B Plastic Flat Pack	**B** 3
C SOT-23	**C** 3 (Pin 2 connected to case)
D SOT-223	**D** 14
F Gullwing DIP	**E** 16
G TO-18	**G** 24
H Side-Brazed CerDIP	**H** 6
J CerDIP	**I** 28
K Plastic Gullwing Quad Flat Package	**L** 40
L Plastic Leaded Chip Carrier (PLCC)	**M** 2
M SOT-89	**N** 18
O Plastic 'SO' Surface Mount	**P** 20
P Plastic DIP	**Q** 60
R TO-52	**S** 68
Y Dice	**T** 5
Z TO-92	**U** 64
	W 44
	Z 80



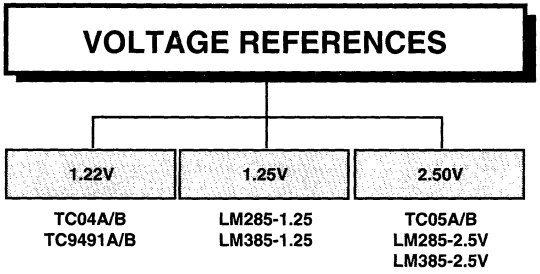
- Display A/D Converters
- System A/D Converters
- V/F and F/V Converters
- Voltage References
- Chopper-Stabilized Operational Amplifiers

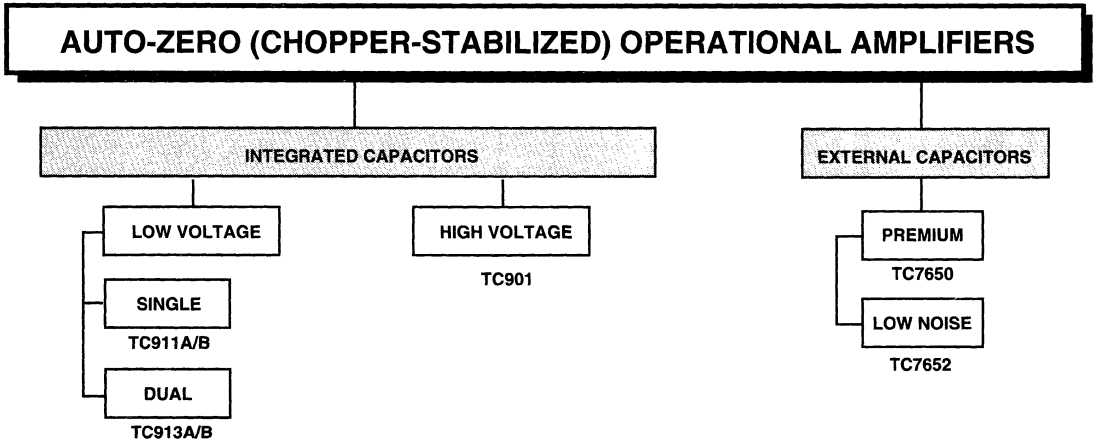


*OPTIONAL CONTROLLER CHIP FOR TC500/A



**OPTIONAL LCD DRIVER


VOLTAGE REFERENCES
1.22V
1.25V
2.50V
TC04A/B
TC9491A/B
LM285-1.25
LM385-1.25
TC05A/B
LM285-2.5V
LM385-2.5V


AUTO-ZERO (CHOPPER-STABILIZED) OPERATIONAL AMPLIFIERS
INTEGRATED CAPACITORS
EXTERNAL CAPACITORS
LOW VOLTAGE
HIGH VOLTAGE
TC901
SINGLE
TC911A/B
DUAL
TC913A/B
PREMIUM
TC7650
LOW NOISE
TC7652

3-1/2 DIGIT A/D CONVERTER WITH HOLD AND DIFFERENTIAL REFERENCE INPUTS

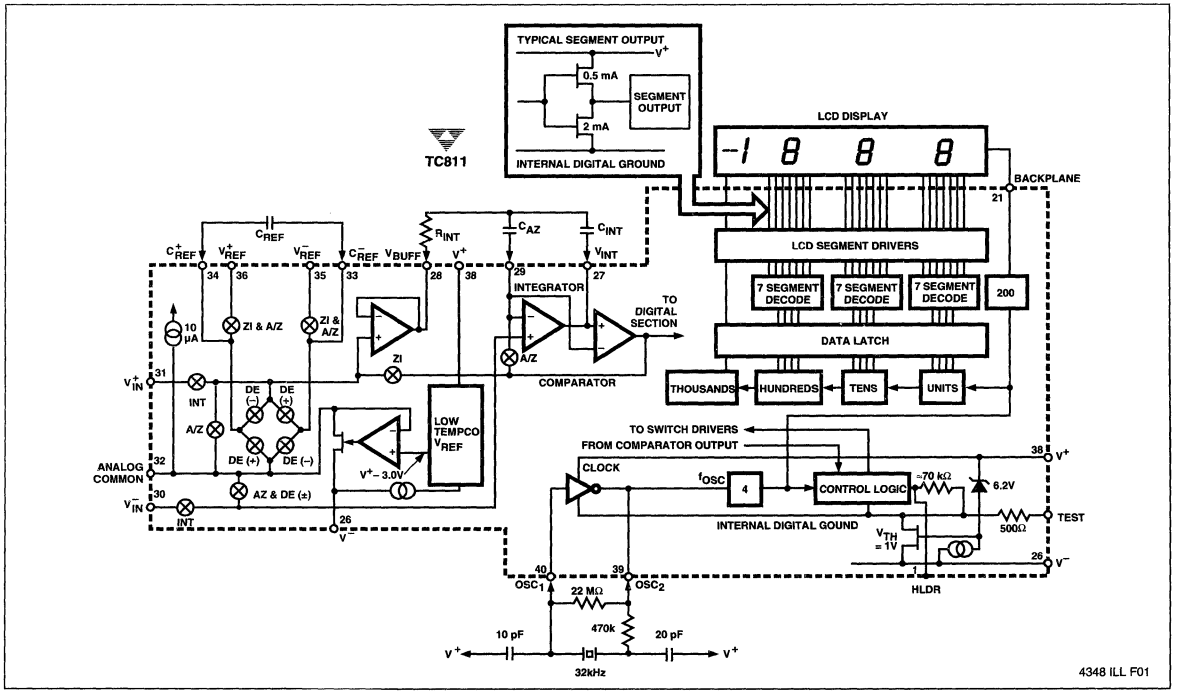
FEATURES

- Differential Reference Input
- Display Hold Function
- Fast Over-Range Recovery, Guaranteed Next Reading Accuracy
- Low Temperature Drift Internal Reference 35 ppm/°C (Typ)
- Guaranteed Zero Reading With Zero Input
- Low Noise ..... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- High Impedance Differential Input
- Low Input Leakage Current ..... 1 pA Typ
  10 pA Max
- Direct LCD Drive—No External Components
- Precision Null Detection with True Polarity at Zero
- Crystal Clock Oscillator
- Available in DIP, Compact Flat Package or PLCC
- Convenient 9V Battery Operation with Low Power Dissipation (600µA Typical, 1mW Maximum)

TYPICAL APPLICATIONS

- Thermometry
- Digital Meters
  - — Voltage/Current/Power
  - — pH Measurement
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity
  - — Humidity
  - — Position
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Digital Scales
- Process Monitors
- Gaussometers
- Photometers

FUNCTIONAL BLOCK DIAGRAM



TC811

GENERAL DESCRIPTION

The TC811 is a low power, 3-1/2 digit, LCD display analog-to-digital converter. This device incorporates both a display hold feature and differential reference inputs. A crystal oscillator, which only requires two pins, permits added features while retaining a 40-pin package. An additional feature is an "Integrator Output Zero" phase which guarantees rapid input overrange recovery.

The TC811 display hold (HLDR) function can be used to "freeze" the LCD display. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The TC811 also includes a differential reference for easy ratiometric measurements. Circuits which use the 7106/26/36 can easily be upgraded to include the hold function with the TC811.

The TC811 has an improved internal zener reference voltage circuit which maintains the Analog Common temperature drift to 35ppm/°C (typical) and 75ppm/°C (maximum). This represents an improvement of two to four times over similar 3-1/2 digit converters, eliminating the need for a costly, space consuming external reference source.

The TC811 limits linearity error to less than one count on both the 200mV and the 2.00V full-scale ranges. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1pA leakage currents and a $10^{12}\Omega$ input impedance. The $15\mu V_{p-p}$ noise performance guarantees a "rock solid" reading. The Auto Zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TC811 incorporates all the active devices for a 3-1/2 digit analog to digital converter to directly drive an LCD display. Onboard oscillator, precision voltage reference and display segment and backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution (0.05%) indicating meter requires only a TC811, an LCD display, five resistors, six capacitors, a crystal, and a 9V battery. Compact, hand held multimeter designs benefit from the TelCom Semiconductor small footprint package option.

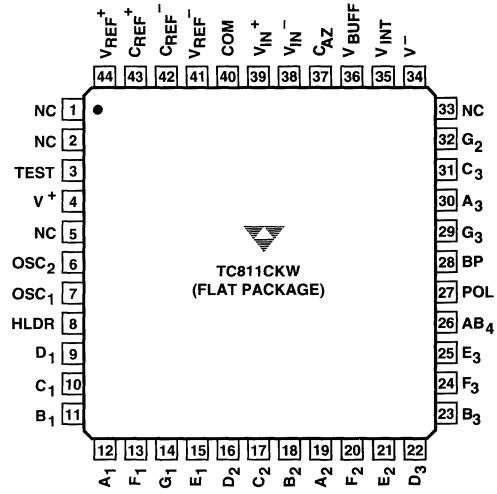
The TC811 uses a dual slope conversion technique which will reject interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400Hz line frequency signals are present.

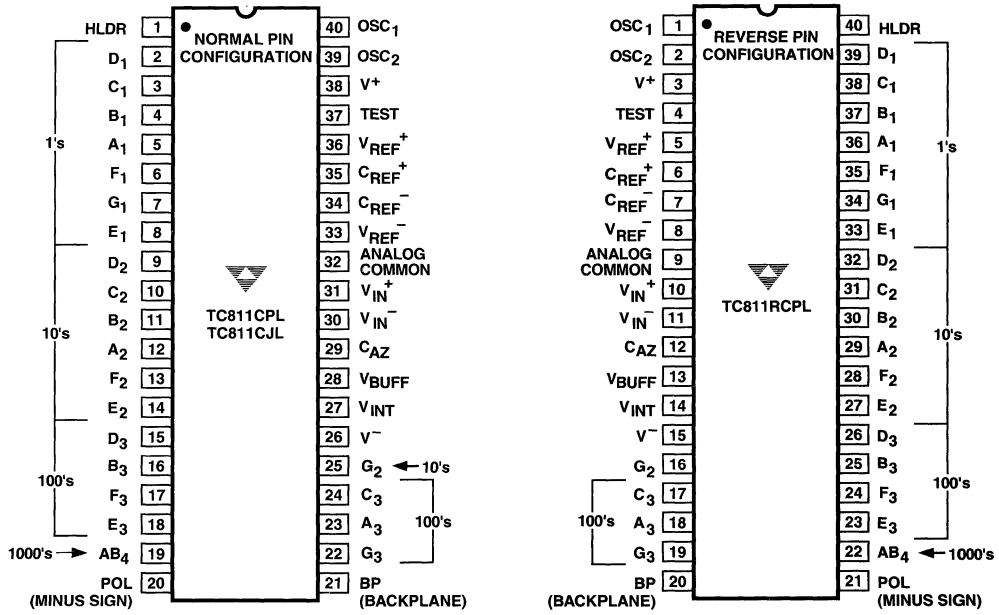
ORDERING INFORMATION

Part No.	Package	Temperature Range	V_{REF} TempCo
TC811CPL	40-Pin Plastic	0° to 70°C	75 ppm/°C Max
TC811RCPL[1]	40-Pin Plastic	0° to 70°C	75 ppm/°C Max
TC811CKW	44-Pin Flat	0° to +70°C	75 ppm/°C Max

NOTES: 1. Reversed pin-out

PIN CONFIGURATIONS





NC = NO INTERNAL CONNECTION

4348 ILL F02

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V+ to V–) 15V
Analog Input voltage (Either Input)[1] ..... V+ to V–
Reference Input Voltage ..... V+ to V–
Clock Input ..... TEST to V+
Power Dissipation[2]
CerDIP Package (J) ..... 1000 mW
Plastic Package (P, K) ..... 800 mW
Plastic Leaded Chip Carrier (L) ..... 800 mW

Operating Temperature Range
Commercial Package (C) ..... 0°C to +70°C
Industrial Package (I) ..... – 25°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (soldering, 60 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{Supply} = 9V, f_{CLOCK} = 32.768kHz, and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
—	Zero Input Reading	V_{IN} = 0V V_{FS} = 200mV	– 000.0	±000.0	+000.0	Digital Reading
—	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
NL	Linearity Error	V_{FS} = 200mV or 2.000V	– 1	±0.2	+1	Counts
E_R	Roll Over Error	V_{IN}– = V_{IN}+ ≈ 200mV	– 1	±0.2	+1	Counts
e_N	Noise	V_{IN} = 0V, V_{FS} = 200mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection	V_{CM} = ±1V, V_{IN} = 0V, V_{FS} = 200mV	—	50	—	µV/V
TC_{SF}	Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0°C ≤ T_A ≤ 70°C (ext. V_{REF} tc = 0ppm)	—	1	5	ppm/°C
Analog Common Section						
V_{CTC}	Analog Common Temperature Coefficient	250KΩ from V+ to Analog Common 0°C ≤ T_A ≤ 70°C "C" Commercial "I" Industrial	 — —	 35 35	 75 100	 ppm/°C ppm/°C
V_C	Analog Common Voltage	250KΩ from V+ to Analog Common	2.7	3.05	3.35	Volts
Hold Pin Input Section						
	Input Resistance	Pin 1 to Pin 37	—	70	—	kΩ
V_{IL}	Input Low Voltage	Pin 1	—	—	Test +1.5	V
V_{IH}	Input High Voltage	Pin 1	V+ – 1.5	—	—	V
LCD Drive Section[3]						
V_{SD}	LCD Segment Drive Voltage	V+ to V– = 9V	4	5	6	V_{P-P}
V_{SD}	LCD Backplane Drive Voltage	V+ to V– = 9V	4	5	6	V_{P-P}
Power Supply						
I_{SUP}	Power Supply Current	V_{IN} = 0V, V+ to V– = 9V				
		f_{OSC} = 16kHz	—	70	100	µA
		f_{OSC} = 48kHz	—	90	125	µA

NOTES: 1. Input voltages may exceed supply voltages when input current is limited to100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to a printed circuit board.
3. Backplane drive is in phase with the segment drive for "segment off" 180° out of phase for "segment on." Frequency is 20 times the conversion rate. Average DC component is less than 50mV.

PIN DESCRIPTION

40-Pin DIP	Name	Function
1	HLDR	Hold pin, logic 1 holds present display reading
2	D_1	Activates the D section of the units display
3	C_1	Activates the C section of the units display
4	B_1	Activates the B section of the units display
5	A_1	Activates the A section of the units display
6	F_1	Activates the F section of the units display
7	G_1	Activates the G section of the units display
8	E_1	Activates the E section of the units display
9	D_2	Activates the D section of the tens display
10	C_2	Activates the C section of the tens display
11	B_2	Activates the B section of the tens display
12	A_2	Activates the A section of the tens display
13	F_2	Activates the F section of the tens display
14	E_2	Activates the E section of the tens display
15	D_3	Activates the D section of the hundreds display
16	B_3	Activates the B section of the hundreds display
17	F_3	Activates the F section of the hundreds display
18	E_3	Activates the E section of the hundreds display
19	AB_4	Activates both halves of the 1 in the thousands display
20	POL	Activates the negative polarity display
21	BP	Backplane drive output
22	G_3	Activates the G section of the hundreds display
23	A_3	Activates the A section of the hundreds display
24	C_3	Activates the C section of the hundreds display
25	G_2	Activates the G section of the tens display
26	V–	Negative power supply voltage
27	V_{INT}	Integrator output, connection for C_{INT}
28	V_{BUFF}	Buffer output, connection for R_{INT}
29	C_{AZ}	Integrator input, connection for C_{AZ}
30	V_{IN}–	Analog input low
31	V_{IN}+	Analog input high
32	COM	Analog Common: Internal zero reference
33	V_{REF}–	Reference input low
34	C_{REF}–	Negative connection for reference capacitor
35	C_{REF}+	Positive connection for reference capacitor
36	V_{REF}+	Reference input high
37	TEST	All LCD segment test when pulled high (V^+)
38	V+	Positive power supply voltage
39	OSC_2	Crystal oscillator output
40	OSC_1	Crystal oscillator input

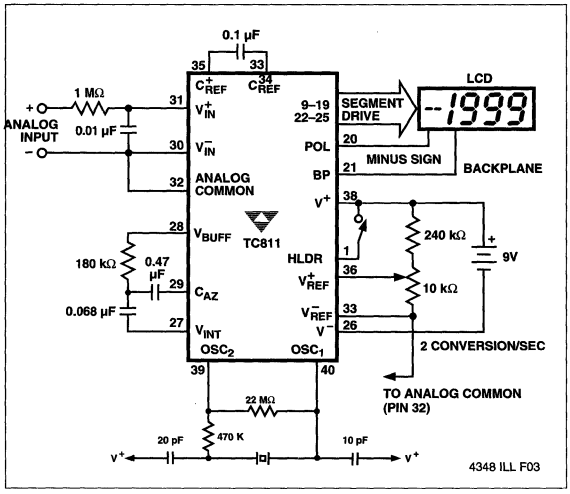


Figure 1 Typical Operating Circuit

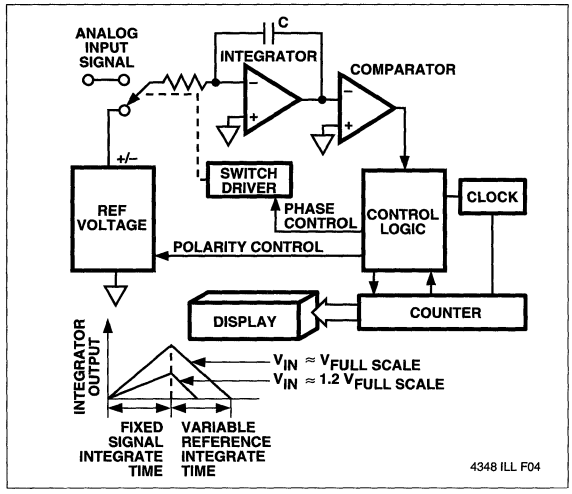


Figure 2 Basic Dual Slope Converter

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

(All Pin Designations Refer to 40-Pin DIP Package)

The TC811 is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid the user in following the detailed TC811 theory of operation following this section. A conventional dual slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Fig 2, the unknown input signal to be converted is integrated from zero for a fixed time period (T_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

V_{REF} = Reference voltage
t_{INT} = Integration Time
t_{DEINT} = Deintegration Time

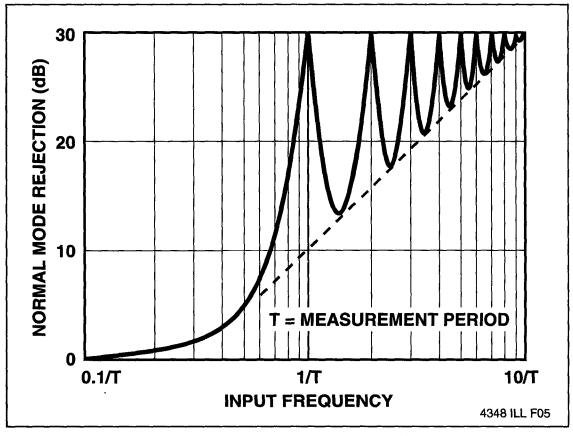


Figure 3 Normal-Mode Rejection of Dual Slope Converter

For a constant V_{INT}:

$$V_{IN} = V_{REF}\left[\frac{t_{DEINT}}{t_{INT}}\right]$$

Accuracy in a dual slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integration ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated. (see Fig 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.

THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC811 design incorporates an "Integrator Output Zero" cycle and an "Auto Zero" cycle. These additional cycles ensure the integrator starts at 0V (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator Output Zero Cycle
(2) Auto Zero Cycle
(3) Signal Integrate Cycle
(4) Reference Deintegrate Cycle

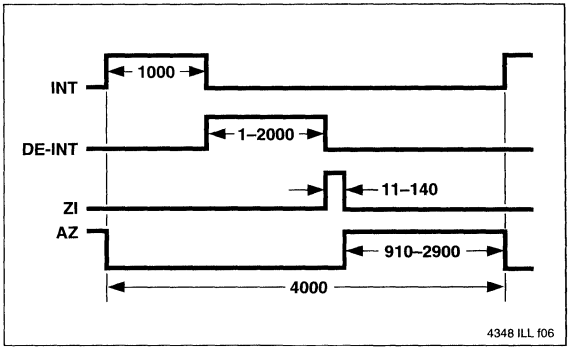


Figure 4a Conversion Timing During Normal Operation

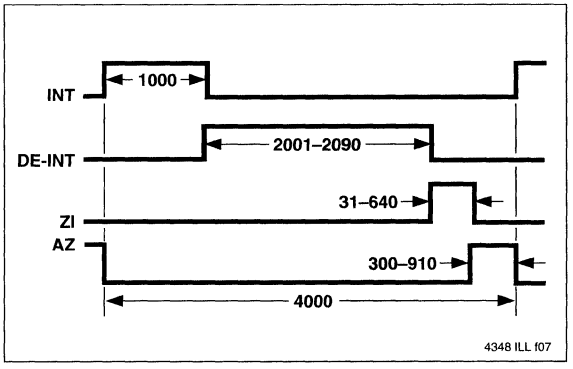


Figure 4b Conversion Timing During Overrange Operation

Integrator Output Zero Cycle

This phase guarantees that the integrator output is at zero volts before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an over-range conversion. The duration of this phase is variable, being a function of the number of counts (clock cycles) required for deintegration.

The Integrator Output Zero cycle will last from 11 to 140 counts for non-over-range conversions and from 31 to 640 counts for over-range conversions.

Auto Zero Cycle

During the Auto Zero cycle, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0V ref.) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero cycle residual is typically 10 to 15μV.

The Auto Zero duration is from 910 to 2,900 counts for non-over-range conversions and from 300 to 910 counts for over-range conversions.

Signal Integration Cycle

Upon completion of the Auto Zero cycle, the Auto Zero loop is opened and the internal differential inputs connect to $V_{IN}+$ and $V_{IN}-$. The differential input signal is then integrated for a fixed time period which, in the TC811 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{INT} = \frac{4000}{f_{OSC}}$$

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground).

If the converter and measured system do not share the same power supply common, as in battery powered applications, $V_{IN}-$ should be tied to Analog Common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Cycle

The reference capacitor, which was charged during the Auto Zero cycle, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration cycle:

$$T_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed Is:

$$\text{Digital Count} = 1000\ \frac{V_{IN}+ - V_{IN}-}{V_{REF}}$$

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

1) Auto Zero: 300 to 2900 Counts
2) Signal Integrate: 1000 Counts

This time period is fixed. The integration period is:

$$T_{INT} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

Where f_{OSC} is the crystal oscillator frequency.

3) Reference Integrate: 0 to 2000 Counts
4) Integrator Output Zero: 11 to 640 Counts

The TC811 can replace the ICL7106/26/36 in circuits which require both the hold function and a differential reference. The TC811 offers a greatly improved internal reference temperature coefficient, which can often eliminate the need for an external reference. Some minor component changes are required to upgrade existing designs, reduce power dissipation, and improve the overall performance. (see Oscillator Components)

Digital Section

The TC811 contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment of "OFF". An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If $V_{IN}+$ and $V_{IN}-$ are reversed then this indicator would reverse.

TEST Function (TEST)

On the TC811, when TEST is pulled to a logical "HIGH", all segments are turned "ON". The display will read "-1888". During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

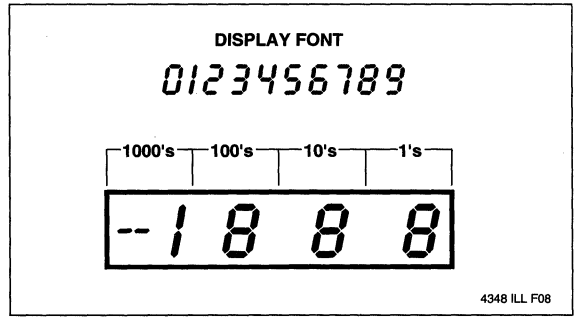


Figure 5 Display FONT and Segment Assignment

HOLD Reading Input (HLDR)

When HLDR is at a logic "HI" the latch will not be updated. Conversions will continue but will not be updated until HLDR is returned to "LOW". To continuously update the display, connect HLDR to ground or leave it open. This input is CMOS compatible and has an internal resistance of 70KΩ (typical) tied to TEST.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The value of the Auto Zero capacitor (C_{AZ}) has some influence on system noise. A 0.47µF capacitor is recommended for 200mV full-scale applications where 1LSB is 100µV. A 0.10µF capacitor should be used for 2.0V full-scale applications. A capacitor with low dielectric absorption (Mylar) is required.

Reference Voltage Capacitor -C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1µF capacitor is typical. If the application requires a sensitivity of 200mV full-scale, increase C_{REF} to 1.0µF. Rollover error will be held to less than 1/2 count. A good quality, low leakage capacitor, such as Mylar, should be used.

Integrating Capacitor - C_{INT}

CINT should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±2V integrator output swing is optimum when the analog input is near full-scale. For 2 or 2.5 reading/second (f_{OSC} = 32kHz or 40kHz) and V_{FS} = 200mV, a .068µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing. An exact expression for C_{INT} is :

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where:
f_{OSC} = Clock frequency at Pin 39
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor -R_{INT}

The input buffer amplifier and integrator are designed with class A output stages which have idling currents of 6µA. The integrator and buffer can supply 1µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200mV full-scale, R_{INT} should be about 180kΩ. A 2.0V full-scale requires abut 1.8MΩ.

Oscillator Components

The internal oscillator has been designed to operate with a quartz crystal, such as the Statek CX-1V series. Such crystals are very small and are available in a variety of standard frequencies. Note that f_{OSC} is divided by four to generate the TC811 internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of ac-line noise pickup, a 40kHz crystal should be used. This frequency will yield an integration period of 100ms and will reject both 50Hz and 60Hz noise. For prototyping or cost-sensitive applications a 32.768kHz watch crystal can be used, and will produce about 25dB of line-noise rejection. Other crystal frequencies, from 16kHz to 48kHz, can also be used.

Pins 39 and 40 make up the oscillator section of the TC811. Figures 6a and 6b show some typical conversion rate component values.

The LCD backplane frequency is derived by dividing the oscillator frequency by 800. Capacitive loading of the LCD may compromise display performance if the oscillator is run much over 48KHz.

Reference Voltage (V_{REF})

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

In some applications a scale factor other than unity may exist, such as between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400mV for 2000lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

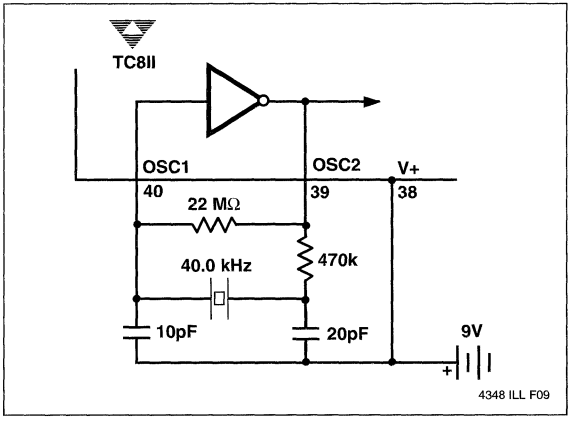


Figure 6a TC811 Oscillator

Oscillator Freq. (kHz)	Full-Scale Voltage (V_{FS})			
	200mV		2.0V	
	RINT	CINT	RINT	CINT
32.768	180k	0.068µF	1.8M	0.068µF
40	150k	0.068µF	1.5M	0.068µF

Figure 6b

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}+ (Pin 31), V_{IN}– (Pin 30))

The TC811 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V+ – 1.0 to V– + 1.5V. Common-mode voltages are removed from the system when the TC811 operates from a battery or floating power source (isolated from measured system) and V_{IN}– is connected to Analog Common. (see Fig 8)

In systems where common-mode voltages exist, the 86dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 8). For such applications the integrator output swing can be reduced below the recommended 2.0V full-scale swing. The integrator output will swing within 0.3V of V+ or V– without increased linearity error.

Reference (V_{REF}+ (Pin 36), V_{REF}– (Pin 33))

Unlike the ICL7116, the TC811 has a differential reference as well as the "hold" function. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors. The TC811 is ideally suited to applications in handheld multimeters, panel meters, and portable instrumentation. The reference voltage can be generated anywhere within the V+ to V– power supply range.

To prevent rollover type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1µF capacitor is a typical value.

The TC811 offers a significantly improved Analog Common temperature coefficient. This provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of Analog Common is typically 35ppm/°C.

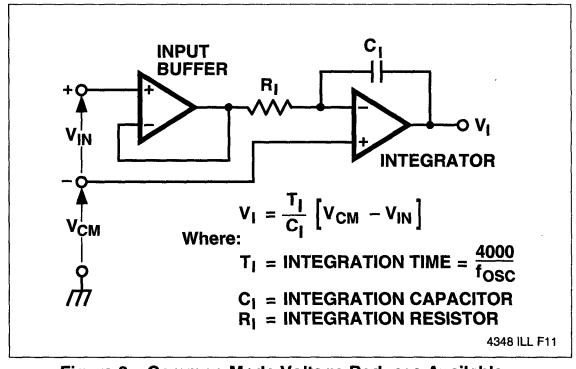


Figure 8 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

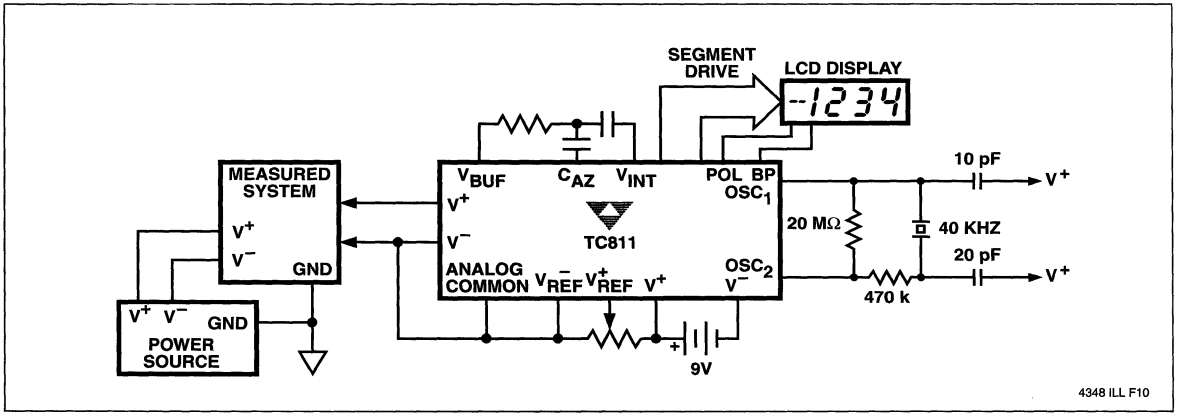


Figure 7 Common-Mode Voltage Removed in Battery Operation With V_{IN}– = Analog Common

Analog Common (Pin 32)

The Analog Common pin is set at a voltage potential approximately 3.0V below V+. This potential is guaranteed to be between 2.70V and 3.35V below V+. Analog common is tied internally to an N channel FET capable of sinking 100μA. This FET will hold the common line at 3.0V below V+ should an external load attempt to pull the common line toward V+. Analog common source current is limited to 1μA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V+ – 3.0V).

The TC811 connects the internal V_{IN}+ and V_{IN}– inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}– is connected to Analog Common. If V_{IN}– is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}– are usually connected, removing common-mode voltage concerns. In systems where V_{IN}– is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}–.

The Analog Common pin serves to set the analog section reference or common point. The TC811 is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC811 power source. The Analog Common potential of V+ – 3.0V gives a 7V end of battery life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage (V+ – V– > 7.0V), Analog Common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TC811 reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See TC811 Internal Voltage Reference discussion.

TEST (Pin 37)

The TEST pin potential is 5V less the V+. TEST may be used as the negative power supply connection when interfacing the TC811 to external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500Ω resistor. The TEST pin may be used to sink up to 1mA. See the applications section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled "HIGH" (V+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes, because when TEST is pulled to V+, the LCD Segments are impressed with a DC voltage which may cause damage to the LCD.

APPLICATIONS INFORMATION

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin. The TEST pin potential is approximately 5V below V+.

Internal Voltage Reference

The TC811 Analog Common voltage temperature stability has been significantly improved. This improved device can be used to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed, however, noise performance will be improved by increasing C_{AZ} (See Auto Zero Capacitor section). Fig 10 shows Analog Common supplying the necessary voltage reference for the TC811.

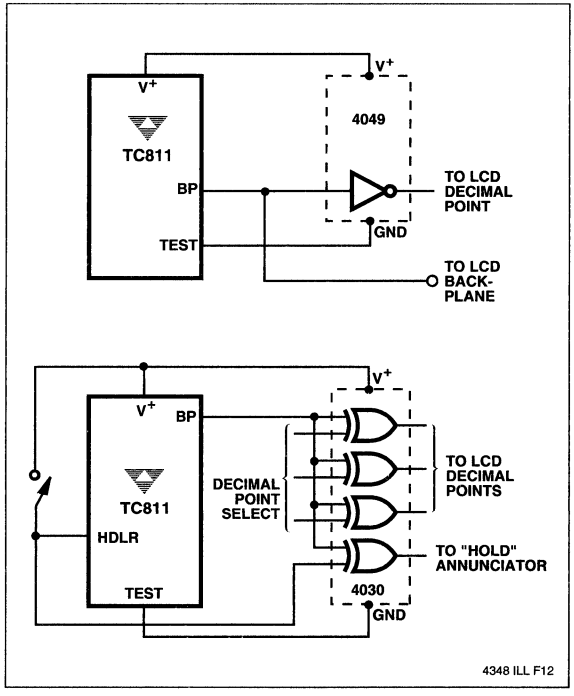


Figure 9 Display Annunciator Drivers

Liquid Crystal Display Sources

Several LCD manufactures supply standard LCD displays to interface with the TC811 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
EPSON	3415 Kashikawa St., Torrence, CA 90505 212-534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Oscillator Crystal Source

Manufacturer	Address/Phone	Representative Part Numbers
STATEK	512 N-Main Orange, CA 92668 714-639-7810	CX-1V 40.0

Ratiometric Resistance Measurements

The TC811 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 11). The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

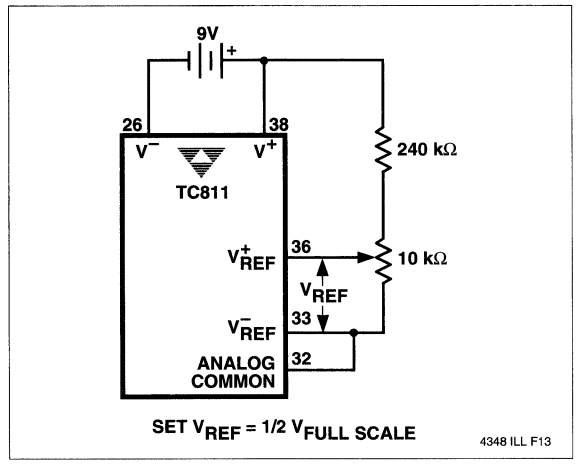


Figure 10 TC811 Internal Voltage Reference Connection

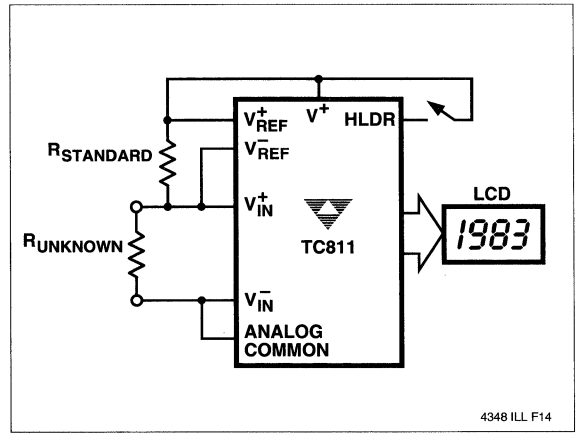


Figure 11 Low Parts Count Ratio Metric Resistance Measurement

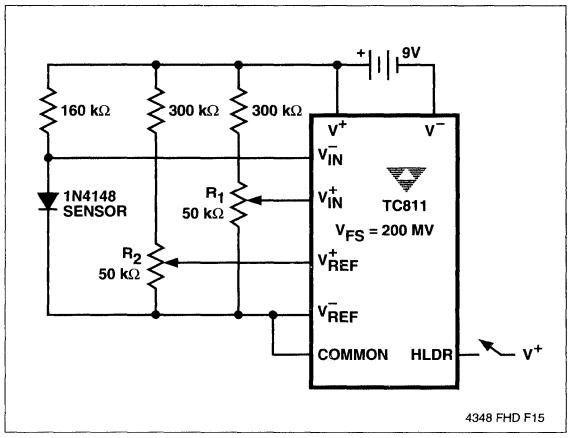
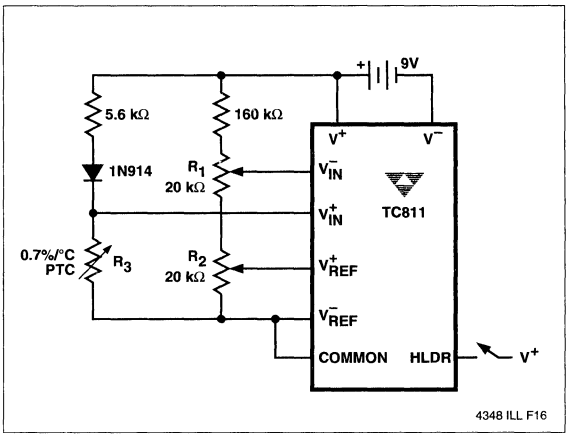


Figure 12 Temperature Sensor

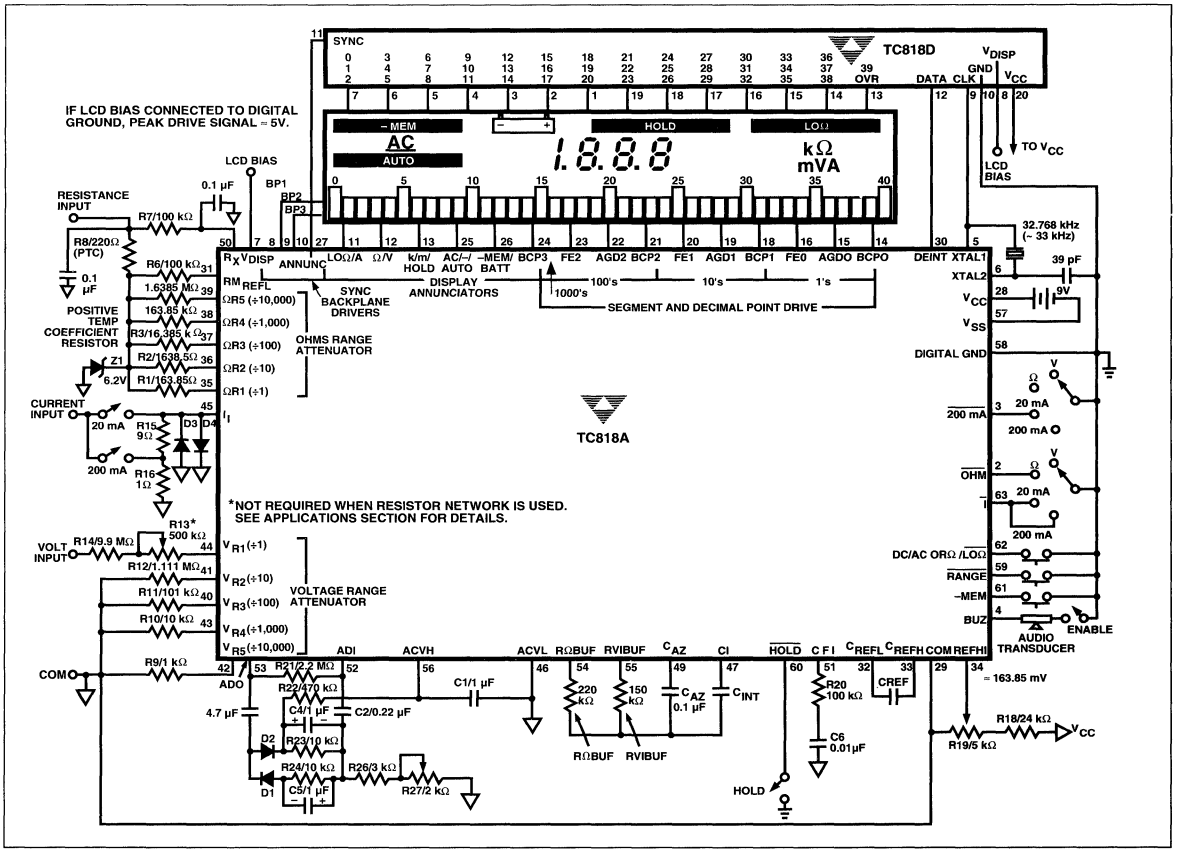


AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS

FEATURES

- 3-1/2 Digit Numeric Plus 40-Segment Bar-Graph LCD Drivers
- Annunciator Outputs Permit Customizing of LCD
- 2-Chip Set, Surface-Mounted
  - — 64-Pin Flat Package
  - — 20-Pin Small Outline (SO)
- Auto-Range Operation for AC and DC Voltage and Resistance Measurements
- Two User-Selected AC/DC Current Ranges ..... 20 mA and 200 mA
- 22 Operating Ranges
  - — 9 DC/AC Voltage
  - — 4 AC/DC Current
  - — 9 Resistance and Low-Power Ohms
- Display Hold Function
- 3-1/2 Digit Resolution in Auto-Range Mode 1/2000
- Extended Resolution in Manual Range Mode 1/3000
- Memory Mode for Relative Measurements ..... ±5% F.S.
- Internal AC-to-DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits, Bar-Graphs, and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Low-Drift Internal Reference ..... 75 ppm/°C
- 9V Battery Operation ..... 10 mW
- Low Battery Detection and LCD Annunciator

FUNCTIONAL BLOCK DIAGRAM



AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS

GENERAL DESCRIPTION

The TC818 is a 2-chip integrating analog-to-digital converter (ADC) with 3-1/2 digit numeric and 40-segment bar-graph LCD drivers, automatic ranging, and single 9V battery operation. The TC818 chip set (consisting of the TC818A and TC818D), combines the precision of a numeric display with the quick recognition of a bar-graph. The numeric display is driven by the TC818A, which also includes the ADC. The bar-graph display is driven by the TC818D.

The 40-segment bar-graph display provides "quick-look" perception of amplitude. Recognizing trends is also easier with a bar-graph, making TC818 based instruments valuable in nulling, tuning, calibration, and similar applications. On the other hand, the numeric display provides 0.05% resolution and a full set of annunciators that spell out the TC818's many operating modes.

Automatic range selection is provided for both voltage (DC and AC) and ohms (high and low power) measurements. Expensive and bulky mechanical range switches are not required. Five full-scale ranges are available, with automatic selection of external volt/ohm attenuators over a 1 to 10,000 range. Two current ranges, 20 mA and 200 mA, can be manually selected. The auto-range feature can be bypassed, allowing input attenuator selection through a single line input.

During manual mode operation, resolution is extended to 3000 counts full-scale. Extended resolution is also available during 2000 kΩ and 2000V full-scale auto-range operation. The extended range operation is indicated by a flashing 1 MSD and by the fully-extended bar-graph.

The TC818 includes an AC-to-DC converter for AC voltage and current measurements. Only external diodes/resistors/capacitors are required. Other features include a memory mode, low-battery detection, display $\overline{\text{HOLD}}$ input, and continuity buzzer driver.

The 3-1/2 digit numeric display includes a full set of annunciators. Decimal points are adjusted as automatic or manual range changes occur, and voltage, current, and ohms operating modes are displayed. Additional annunciators are activated for manual, auto, memory, $\overline{\text{HOLD}}$, AC, low-power ohms, and low-battery conditions.

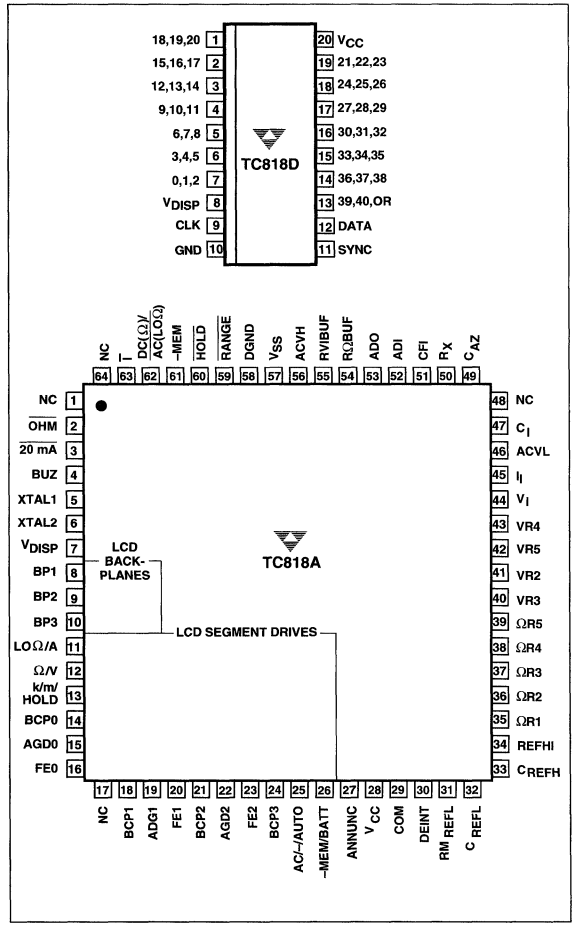
The TC818 is available in a surface-mounted chip set, with the TC818A in a 64-pin flat package and the TC818D in a 20-pin small outline (SO) package. Combining numeric and bar-graph display drivers, single 9V battery operation, internal range switching, and compact surface mounting, the TC818 is ideal for advanced portable instruments.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC818ACBU	64-Pin Plastic Quad Flat Package	0°C to +70°C
TC818ADCOP*	20-Pin SO	0°C to +70°C

*** CONTACT FACTORY FOR AVAILABILITY**

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS *

TC818A

Supply Voltage ..... +15V
Analog Input Voltage ..... V_{CC} to V_{SS}
Reference Input Voltage ..... V_{CC} to V_{SS}
Voltage at Pin 43 ..... Common ±0.7V
Power Dissipation ..... 800 mW

TC818D

Supply Voltage ..... +6V
Digital Input Voltage ..... V_{CC} to GND
Power Dissipation ..... 500 mW

Both Devices

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 9V, T_A = +25°C, Figure 1 Test Circuit

Symbol	Parameter	Test Conditions	TC818A Min	TC818A Typ	TC818A Max	Unit
	Zero Input Reading	200 mV Range Without 10 MΩ Resistor 200 mV Range With 10 MΩ Resistor 20 mA and 200 mA Range	–0000 –0001 –0000	0000 — 0000	+0000 +0001 +0000	Digital Reading
RE	Roll-Over Error	200 mV Range Without 10 MΩ Resistor 200 mV Range With 10 MΩ Resistor 20 mA and 200 mA Range	— — —	— — —	±1 ±3 ±1	Counts
NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
I_{IN}	Input Leakage Current		—	—	10	pA
e_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{P-P}
	AC Frequency Response	±1% Error ±5% Error	— —	40 to 500 40 to 2000	— —	Hz
	Open Circuit Voltage for Ohm Measurements	Excludes 200Ω Range	—	570	660	mV
	Open Circuit Voltage for $\overline{LO}$ Ohm Measurements	Excludes 200Ω Range	—	285	350	mV
V_{COM}	Analog Common Voltage	(V_{CC} – V_{COM})	2.8	3	3.3	V
V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
		Display Multiplex Rate	—	100	—	Hz
V_{IL}	Low Logic Input	$\overline{20mA}$, AC, I, $\overline{LO\Omega}$, HOLD Range, –MEM, Ohms (Relative to DIGITAL GND, Pin 55)	—	—	1	V
	Logic 1 Pull-Up	$\overline{20\ mA}$, AC, I, $\overline{LO\Omega}$, HOLD Range, –MEM, Ohms (Relative to DIGITAL GND, Pin 55)	—	25	—	µA
V_{OL}	Low Logic Output	ANNUNC, DEINT; I_L = 100 µA	—	DGND+0.1	—	V
V_{OH}	High Logic Output	ANNUNC, DEINT; I_L = 100 µA	—	V_{CC}–0.1	—	V
	Buzzer Driver Frequency		—	4	—	kHz
	Low Battery Flag Voltage	V_{CC} to V_{SS}	6.3	6.6	7	V
	Operating Supply Current		—	0.8	1.5	mA

ELECTRICAL CHARACTERISTICS: V_{CC} = 5V, GND = 0V, T_A = +25°C

Symbol	Parameter	Test Conditions	TC818D Min	TC818D Typ	TC818D Max	Unit
V_{IH}	High Logic Input		2.5	—	—	V
V_{IL}	Low Logic Input		—	—	1	V
I_{IL}	Logic Input Current	$V_{CC} \geq V_{IN} \geq$ GND	—	0.01	10	nA
	Display Multiplex Rate		—	100	—	Hz
	Operating Supply Current		—	40	100	µA

TC818A PIN DESCRIPTION

Pin No. (Plastic Quad Flat Package)	Symbol	Description
2	$\overline{OHM}$	Logic input. "0" (digital ground) for resistance measurement.
3	$\overline{20\ mA}$	Logic Input. "0" (digital ground) for 20 mA full-scale current measurement.
4	BUZ	Buzzer. Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A noncontinuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
5	XTAL1	32.768 kHz crystal connection and clock output to drive TC818D.
6	XTAL2	32.768 kHz crystal connection.
7	V_{DISP}	Sets peak LCD drive signal: $V_P = V_{CC} = V_{DISP}$. V_{DISP} may also be used to compensate for temperature variation of LCD crystal threshold voltage.
8	BP1	LCD backplane #1.
9	BP2	LCD backplane #2.
10	BP3	LCD backplane #3.
11	LOΩ/A	LCD annunciator segment drive for low ohms resistance measurement and current measurement.
12	Ω/V	LCD annunciator segment drive for resistance measurement and voltage measurement.
13	k/m/HOLD	LCD annunciator segment drive for k ("kilo-Ohms"), m ("milli-Amps" and "milli-Volts") and HOLD mode.
14	BCP0 (Ones Digit)	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD).
15	ADG0	LCD segment drive for "a," "g," "d" segments of LSD.
16	FE0	LCD segment drive for "f" and "e" segments of LSD.
18	BCP1	LCD segment drive for "b," "c" segments and decimal point of second LSD.
19	ADG1	LCD segment drive for "a," "g," "d" segments of second LSD.
20	FE1	LCD segment drive for "f" and "e" segments of second LSD.
21	BCP2	LCD segment drive for "b," "c" segments and decimal point of third LSD (hundreds digit).
22	ADG2	LCD segment drive for "a," "g," "d" segments of third LSD.
23	FE2	LCD segment drive for "f" and "e" segments of third LSD.
24	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (thousands digit).
25	AC/–/AUTO	LCD annunciator segment drive for AC measurements, polarity, and auto-range operation.
26	–MEM/BATT	LCD annunciator segment drive for low-battery indication and memory (relative measurement).
27	ANNUNC	Square-wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off. ANNUNC is also used to synchronize the TC818A and TC818D backplanes.
28	V_{CC}	Positive battery supply connection.
29	COM	Analog circuit ground reference point. Nominally 3V below V_{CC}.
30	DEINT	Deintegrate output. Transmits the A/D conversion result to the bar-graph LCD driver. (See text.)
31	RM_{REFL}	Ratiometric (resistance measurement) reference low voltage.
32	C_{REFL}	Reference capacitor negative terminal, C_{REF} = 0.1 µF.
33	C_{REFH}	Reference capacitor positive terminal, C_{REF} = 0.1 µF.
34	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
35	ΩR1	Standard resistor connection for 200Ω full-scale.
36	ΩR2	Standard resistor connection for 2000Ω full-scale.
37	ΩR3	Standard resistor connection for 20 kΩ full-scale.
38	ΩR4	Standard resistor connection for 200 kΩ full-scale.

TC818A PIN DESCRIPTION (Cont.)

Pin No. (Plastic Quad Flat Package)	Symbol	Description
39	ΩR5	Standard resistor connection for 2000 kΩ full-scale.
40	VR3	Voltage measurement ÷100 attenuator.
41	VR2	Voltage measurement ÷10 attenuator.
42	VR5	Voltage measurement ÷10,000 attenuator.
43	VR4	Voltage measurement ÷1000 attenuator.
44	V_I	Unknown voltage input ÷ attenuator.
45	I_I	Unknown current input.
46	ACVL	Low output of AC-to-DC converter.
47	C_I	Integrator capacitor connection. Nominally 0.1 µF. (Must have low dielectric absorption. Polypropylene dielectric suggested.)
49	C_{AZ}	Auto-zero capacitor connection. Nominally 0.1 µF.
50	R_X	Unknown resistance input.
51	CFI	Input filter connection.
52	ADI	Negative input of internal AC-to-DC operational amplifier.
53	ADO	Output of internal AC-to-DC operational amplifier.
54	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Nominally 220 kΩ.
55	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Nominally 150 kΩ.
56	ACVH	Positive output of AC-to-DC converter.
57	V_{SS}	Negative supply connection. Connect to negative terminal of 9V battery.
58	DGND	Internal logic digital ground. Ground connection for the TC818D, and the logic "0" level. Nominally 4.7V below V_{CC}.
59	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
60	$\overline{\text{HOLD}}$	Input to hold display. Connect to DGND to "freeze" display.
61	–MEM	Input to enter memory measurement mode for relative measurements. The two LSDs are stored and subtracted from future measurements.
62	DC (Ω)/ AC ($\overline{\text{LO}}\Omega$)	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
63	$\overline{\text{I}}$	Input to select measurement. Connect to logic "0" (digital ground) for current measurement.

* NOTE: Pins 1, 7, 48, 64 = No Connection

TC818D PIN DESCRIPTION

Pin No. (20-Pin SO)	Symbol	Description
1	18, 19, 20	Segments 18, 19, 20 of LCD.
2	15, 16, 17	Segments 15, 16, 17 of LCD.
3	12, 13, 14	Segments 12, 13, 14 of LCD.
4	9, 10, 11	Segments 9, 10, 11 of LCD.
5	6, 7, 8	Segments 6, 7, 8 of LCD.
6	3, 4, 5	Segments 3, 4, 5 of LCD.
7	0, 1, 2	Segments 0, 1, 2 of LCD.
8	V_{DISP}	Sets peak LCD voltage drive level. Connect to V_{DISP} of TC818A, or to GND of TC818D.
9	CLK	Clock input. Connect to XTAL1 output of TC818A.
10	GND	Digital ground. Connect to DGND of TC818A.
11	SYNC	Display SYNC input. Synchronizes backplanes of the TC818A and TC818D. Connect to ANNUNC output of TC818A.
12	DATA	Data input. Pulses at the CLK input are counted while DATA is logic HIGH. Connect to DEINT output of TC818A.
13	39, 40, OR	Segments 39, 40 and overrange of LCD.
14	36, 37, 38	Segments 36, 37, 38 of LCD.
15	33, 34, 35	Segments 33, 34, 35 of LCD.
16	30, 31, 32	Segments 30, 31, 32 of LCD.
17	27, 28, 29	Segments 27, 28, 29 of LCD.
18	24, 25, 26	Segments 24, 25, 26 of LCD.
19	21, 22, 23	Segments 21, 22, 23 of LCD.
20	V_{CC}	Power supply input. Connect to V_{CC} of TC818A.

THEORY OF OPERATION

(All Pin Designations Refer to 64-Pin Plastic Quad Flat Package)

The TC818 consists of two CMOS integrated circuits. The TC818A incorporates an auto-ranging ADC and drivers for a 3-1/2 digit LCD, while the TC818D provides data formatting and drivers for a 40-segment bar-graph display. Both integrated circuits are required to form a complete measurement system.

During each A/D conversion cycle, data is transferred from the TC818A to the TC818D. Therefore, the bar-graph display will track the numeric (3-1/2 digit) display. The exact relationship between numeric display counts and bar-graph segments displayed is shown in Table I. Both displays are updated at the same rate. When the TC818A is in its extended resolution mode (3000 counts, maximum), the bar-graph will display all 40 bars continuously.

Analog-to-Digital Converter (ADC)

The TC818A includes an integrating ADC with auto-ranging resolution of 2000 counts and manual range resolution of 3000 counts. Figure 1 shows a simplified schematic of the analog section. In auto-ranging mode, internal logic will adjust the input voltage or ohms attenuators so that measurements will always be made in the appropriate range. Measurement ranges, logic control inputs, 3-1/2 digit LCD formatting, and other features are identical to the TC815 auto-ranging A/D converter. However, the TC818A is not pin-compatible with, and is not a replacement for, the TC815.

A display annunciator output (ANNUNC) can be used to customize the LCD. ANNUNC is a square wave at the backplane frequency. Connecting an annunciator segment to the ANNUNC driver turns the segment on; connecting the segment to its backplane turns it off.

Bar-Graph Driver

The TC818D includes a counter and data latch, clock divider, and triplex LCD bar-graph formatting and display functions. A block diagram of the TC818D and connections between the TC818A and TC818D is shown in Figure 2. The TC818D does not require a separate power supply, since it is powered from V_{CC} and digital ground of the TC818A.

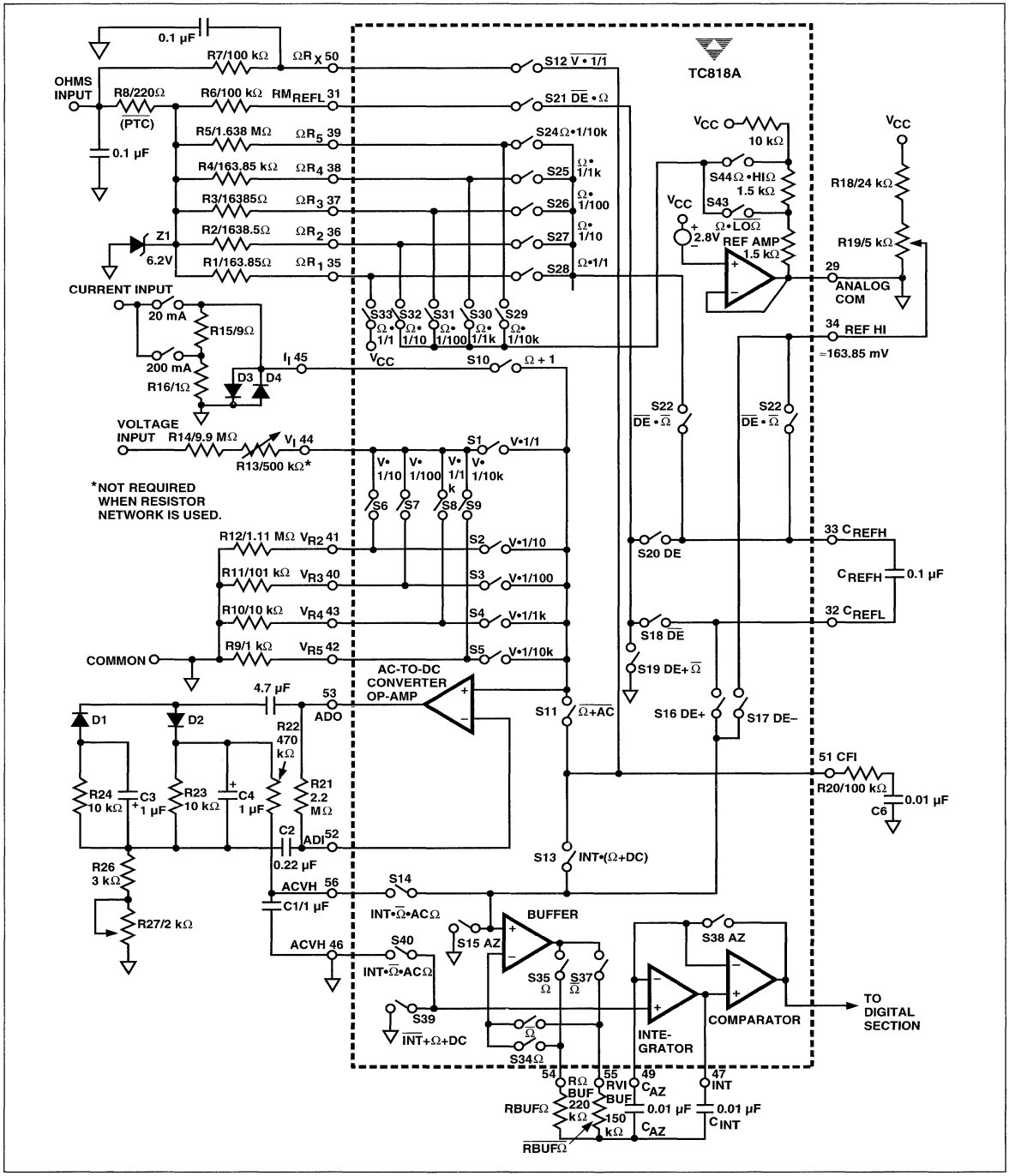


Figure 1 TC818A Analog Section

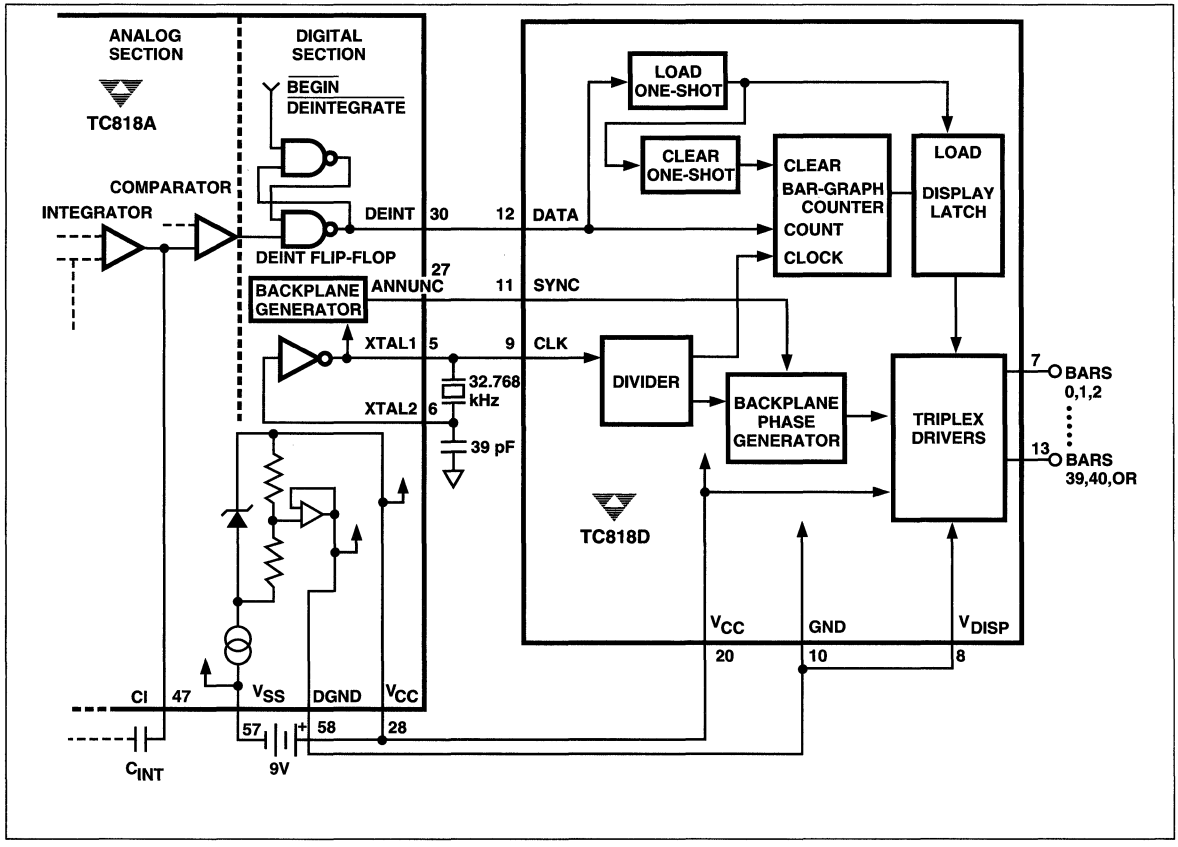


Figure 2 Interface Between TC818A and TC818D

When the TC818D DATA input goes to a logic high, pulses are counted at the CLK input. A clock divider scales clock pulses so that the number of LCD bar-graph segments is proportional to the numeric display (see Table I).

When the DATA input goes low, the counter contents are transferred to a display latch. Then the bar-graph counter is reset to zero in preparation for the next A/D conversion cycle.

The CLK input is also divided to produce the triplex LCD drivers. The backplane and segment driver waveforms are the same voltage levels as the TC818A. However, the TC818D segment driver waveforms are less complicated than those of the TC818A, because adjacent bar-graph segments are either on or off.

The SYNC input permits synchronizing display backplanes. By connecting the ANNUNC output of the TC818A to the SYNC input of the TC818D, the two sets of LCD drivers will be synchronized. This feature permits the use of an LCD with only one set of backplane drivers and saves three pin connections to the display.

LCD backplane and segment drive voltages are set by the voltage between V_{CC} and V_{DISP} pins. In most cases, V_{DISP} will be connected to GND and the LCD drive voltage will be about 5V. If V_{DISP} is not connected to GND, then V_{DISP} of the TC818D must be connected to V_{DISP} of the TC818A.

Data Transfer

Analog conversion results are transferred from the TC818A to the TC818D via two pins, DEINT and XTAL1. DEINT is a TC818A output with a pulse width proportional to the analog voltage being measured. DEINT goes to a logic HIGH at the beginning of the TC818A deintegrate cycle, and goes LOW at the comparator zero-crossing (end of conversion).

Timing of the DEINT pulse width is derived from the TC818A's XTAL1 output, which provides a 32.768 kHz clock. The number of clock pulses occurring while DEINT is high determines the number of bar-graph segments displayed. The relationship between numeric display counts and bar-graph segments is shown in Table I.

Resistance, Voltage, Current Measurement Selection

The TC818 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{OHM}$ (pin 2) and $\overline{I}$ (pin 63) input controls are normally pulled internally to V_{CC}.

By tying these pins to DGND (pin 58), the TC818 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table II.

Table I. TC818A Numeric Display vs TC818D Bar-Graph Segments

Numeric Reading	Bar-Graph Segments
0–24	0
25–74	1
75–124	2
•	•
•	•
•	•
((50*N)–25) to ((50*N)+24) (where $1 \leq N \leq 40$)	N
•	•
•	•
•	•
1975–2024*	40
>2024*	OVR

*Readings >1999 will only occur in manual or expanded resolution modes.

Table II. TC818 Measurement Selection Logic

Function Select Pin		
$\overline{OHM}$ (Pin 2)	$\overline{I}$ (Pin 63)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground 1 = Floating or Tied to V_{CC}

NOTES: 1. $\overline{OHM}$ and $\overline{I}$ are normally pulled internally high to V_{CC} (pin 28). This is considered a logic "1".
2. Logic "0" is the potential at digital ground (pin 58).

Resistance Measurements — Ohms and Low Power Ohms

The TC818 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TC818 low-power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode, the $\Omega/\overline{LO\Omega}$ (pin 62) input selects the low-power ohms measurement mode. For low-power ohms measurements, $\Omega/\overline{LO\Omega}$ (pin 62) is momentarily brought LOW to digital ground potential. The TC818 sets up for a low-power ohms measurement with a maximum open circuit probe voltage of 0.35V above analog common. In the low-power ohms mode, an LCD annunciator, $\overline{LO\Omega}$, will be activated. On power-up, the low-power ohms mode is not active.

If the manual operating mode has been selected, toggling $\Omega/\overline{LO\Omega}$ resets the TC818 back to auto-range mode. In manual mode, the decision to make a normal or low-power ohms measurement should be made before selecting the desired range.

The low-power ohms measurement is not available on the 200Ω full-scale range. Open-circuit voltage on this range is below 2.8V.

The standard resistance values are listed in Table III.

Table III. Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low-Power Ohms Mode
200Ω	163.85Ω (R1)	No
2000Ω	1638.5Ω (R2)	Yes
20 kΩ	16,385Ω (R3)	Yes
200 kΩ	163,850Ω (R4)	Yes
2000 kΩ	1,638,500Ω (R5)	Yes

R8, a positive temperature coefficient resistor, and the 6.2V zener, Z1, provide input voltage protection during ohms measurement.

Ratiometric Resistance Measurements

The TC818 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to pins 35 through 39. A low-power ohms mode may be selected on all but the 200Ω full-scale range. The low-power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 is a detailed block diagram of the TC818 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance, R_X. Figure 4 shows that the conversion accuracy relies only on the accuracy of the external standard resistors.

Normally, the required accuracy of the standard resistances will be dictated by the accuracy specifications of the user's end product. Table IV gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table IV. Reference Resistors

Full-Scale Range (Ω)	Reference Resistor	Ω/Count
200	163.85	0.1
2k	1638.5	1
20k	16385	10
200k	163,850	100
2M	1,638,500	1000

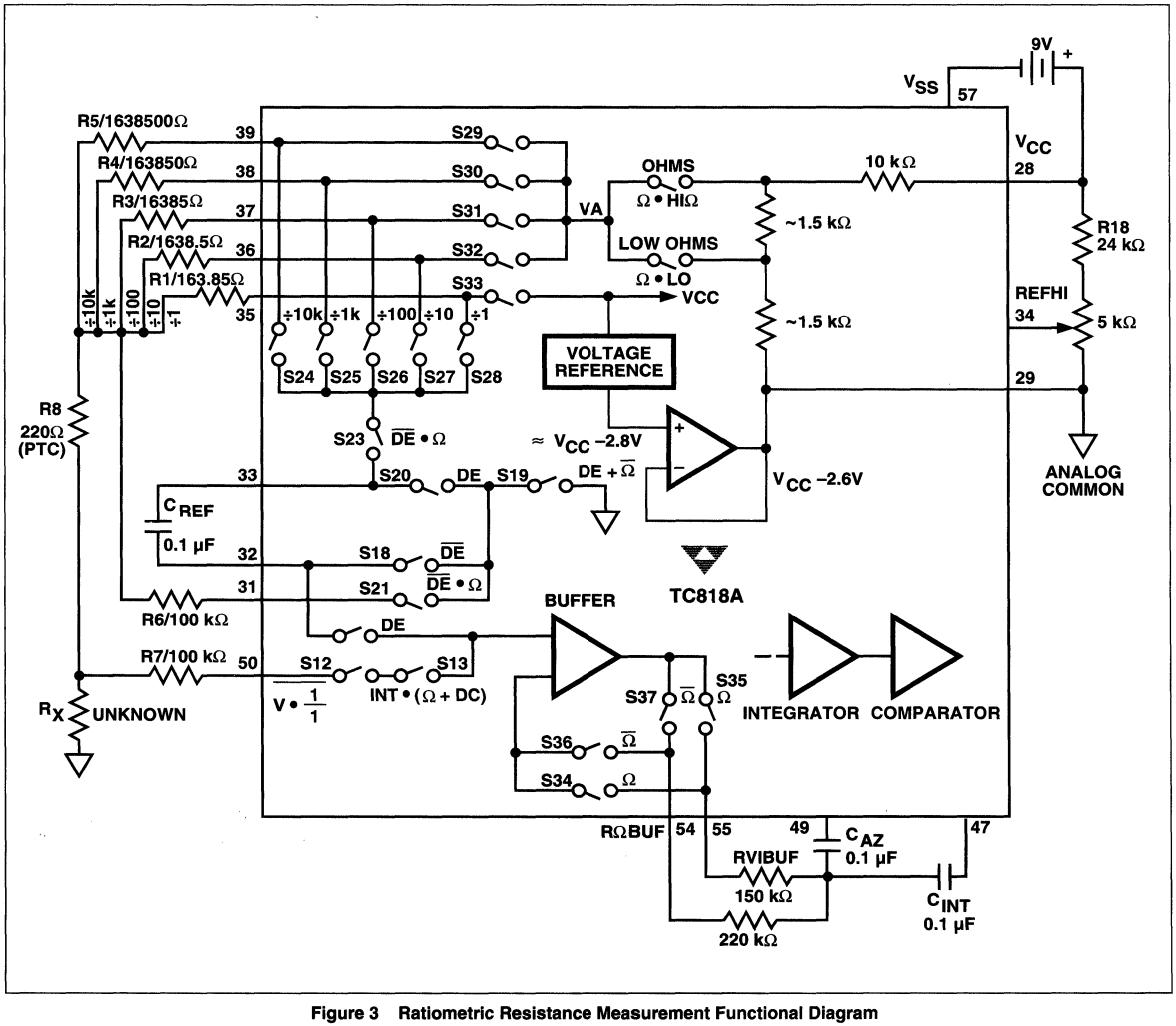
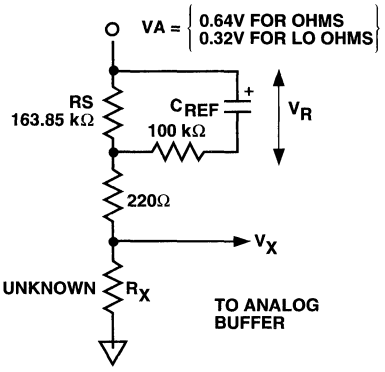


Figure 3 Ratiometric Resistance Measurement Functional Diagram



Example: 200 kΩ Full-Scale Measurement

(a) $V_R = \frac{163.85\ k\Omega}{163.85 + 220 + R_X} \times 0.64$

(b) $V_X = \frac{R_X}{163.85\ k\Omega + 220\Omega + R_X} \times 0.64$

(c) "Ramp-Up Voltage" = "Ramp-Down Voltage"

$$\therefore \frac{V_X}{R_I C_I} \times t_I = \frac{V_R}{R_I C_I} t_{DE}$$

where:

R_I = Integrating Resistor, t_I = Integrate Time

C_I = Integrating Capacitor, t_{DE} = Deintegrate Time

(d) $R_X = 163.85 \left(\frac{t_{DE}}{t_I} \right)$

Independent of R_I, C_I or internal voltage reference.

Figure 4 Resistance Measurement Accuracy Set by External Standard Resistor

Voltage Measurement

Resistive dividers are automatically changed to provide in-range readings for 200 mV to 2000V full-scale readings (Figure 1). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9–R12. The divider leg resistors give a 200 mV signal at V_I (pin 44) for full-scale voltages from 200 mV to 2000V.

For applications that do not require a 10 MΩ input impedance, the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

Current Measurement

The TC818 measures current only under manual range operation. The two user-selectable, full-scale ranges are 20 mA and 200 mA. Select the current measurement mode by holding the I input (pin 63) LOW at digital ground potential. The $\overline{OHM}$ input (pin 2) is left floating or tied to the positive supply.

Two ranges are possible. The 200 mA full-scale range is selected by connecting the $\overline{20\ mA}$ input (pin 3) to digital ground. If left floating, the 200 mA full-scale range is selected.

External current-to-voltage conversion resistors are used at the current input (I_I, pin 45). For 20 mA measurements, a 10Ω resistor is used. The 200 mA range requires a 1Ω resistor. Full scale is 200 mV

Printed circuit board trace resistance between analog common and R16 must be minimized. In the 200 mA range, for example, a 0.05Ω trace resistance causes a 5% current-to-voltage conversion error at I_I (pin 45).

The extended resolution measurement option operates during current measurements.

To minimize roll-over error, the potential difference between ANALOG COM (pin 29) and system common must be minimized.

AC-to-DC Measurements

In voltage and current measurements, the TC818 can be configured for AC measurements. An on-chip operational amplifier and external rectifier components perform the AC-to-DC conversion.

When power is first applied, the TC818 enters the DC measurement mode. For AC measurements (current or voltage), AC/DC (pin 62) is momentarily brought LOW to digital ground potential; the TC818 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling AC/DC to LOW again returns the TC818 to DC operation.

If manual operating mode has been selected, toggling AC/DC resets the TC818 back to auto-range mode. In manual mode operation, AC or DC should be selected first, then the desired range.

The minimum AC full-scale voltage range is 2V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 200 mA full-scale ranges.

Conversion Timing

The TC818 uses the conventional dual-slope integrating conversion technique with an added phase that automatically eliminates zero offset errors. The TC818 gives a zero reading with a 0V input.

This device is designed to operate with a low-cost, readily-available 32.768 kHz crystal. It serves as a time-base oscillator crystal in many digital clocks. (See external crystal sources, page 18.)

The external clock is divided by two. The internal clock frequency is 16.348 kHz, giving a clock period of 61.04 µs. The total conversion — auto-zero phase, signal integrate, and reference deintegrate — requires 8000 clock periods (or 488.3 ms). There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods (or 100 ms), giving a rejection of 50/60 Hz AC line noise.

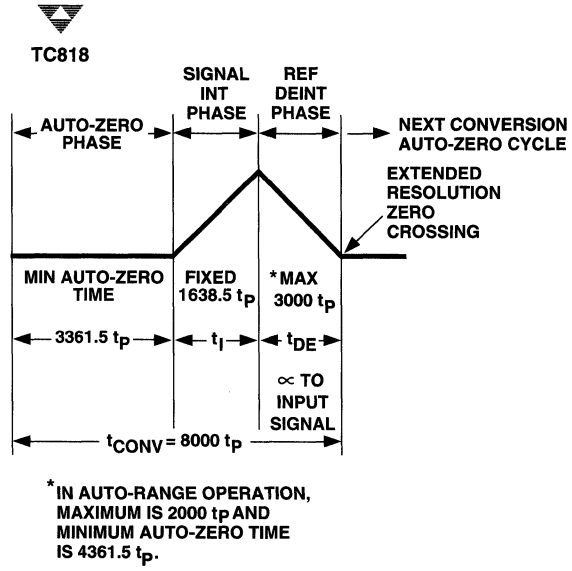
The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods (or 183.1 ms) during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode, the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 5 shows the basic TC818 timing relationships.

Manual Range Selection

The TC818's voltage and resistance auto-ranging feature can be disabled by momentarily bringing $\overline{\text{RANGE}}$ (pin 59) to digital ground potential (pin 58). When the change from auto to manual ranging occurs, the first manual range selected is the last range in the auto-ranging mode.

The TC818's power-up circuit initially selects auto-range operation. Once the manual-range option is entered, range changes are made by momentarily grounding the $\overline{\text{RANGE}}$ control input. The TC818 remains in the manual-range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, $\Omega/\overline{\text{LO}\Omega}$) changes, causing the TC818 to return to auto-ranging operation.



External Crystal = 32.768 kHz

Internal Clock Period = t_P = 2/32.768 = 61.04 µs

Total Conversion Time = t_{CONV} = 8000 (t_P)
= 488.3 ms ≈ 2 conv/sec

Integration Time = t_I = 1638.5 (t_P) = 100 ms

Maximum Reference Deintegrate Time
= t_{DE} = 3000 (t_P) = 183.1 ms (manual, extended resolution)
= 2000 (t_P) = 122.1 ms (auto-range)

Minimum Auto-Zero Time
= (8000–3000–1638.5)
(t_P) = 205.1 ms (manual, extended resolution)
= (8000–2000–1638.5)
(t_P) = 266.2 ms (auto-range)

Figure 5 Basic TC818 Conversion Timing

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Figure 6 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

When operated in the manual-range mode, the TC818 extends resolution by 50% for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only in the 2000 kΩ and 2000V ranges during auto-range operation.

In the extended resolution operating mode, readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally. The bar-graph LCD will be fully extended.

An input overrange condition causes the most significant digit (MSD) to blink and sets the three least significant digits (LSDs) to display "000." The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual- and auto-range operations.

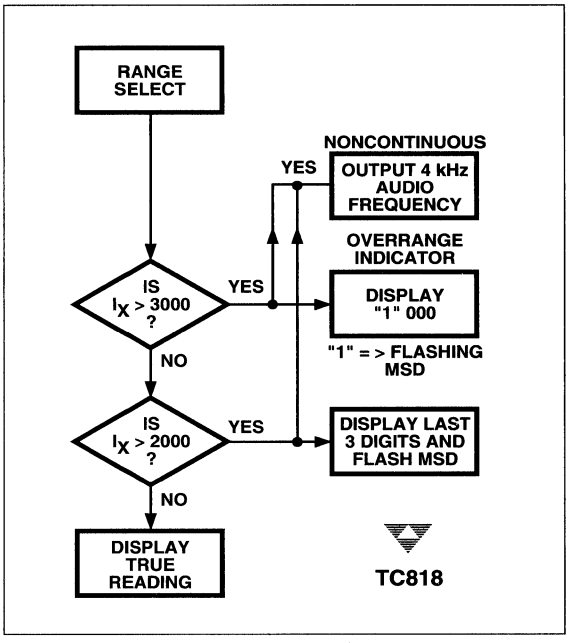


Figure 7 Manual Range Selection; Current Measurement

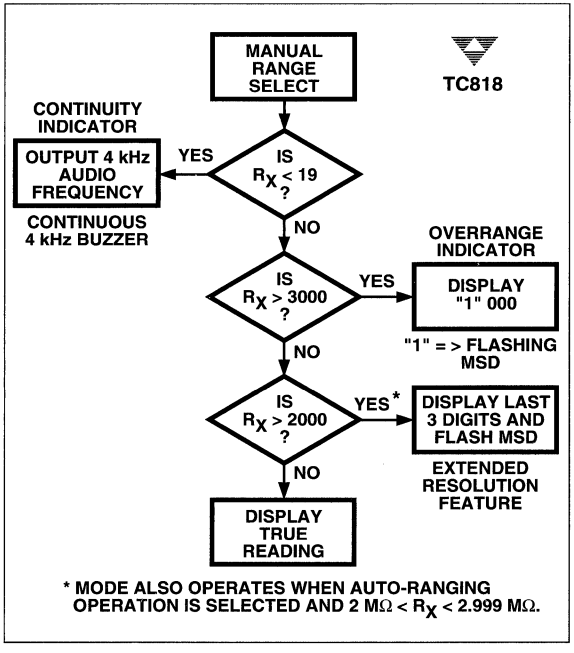


Figure 6 Manual Range Selection; Resistance Measurement

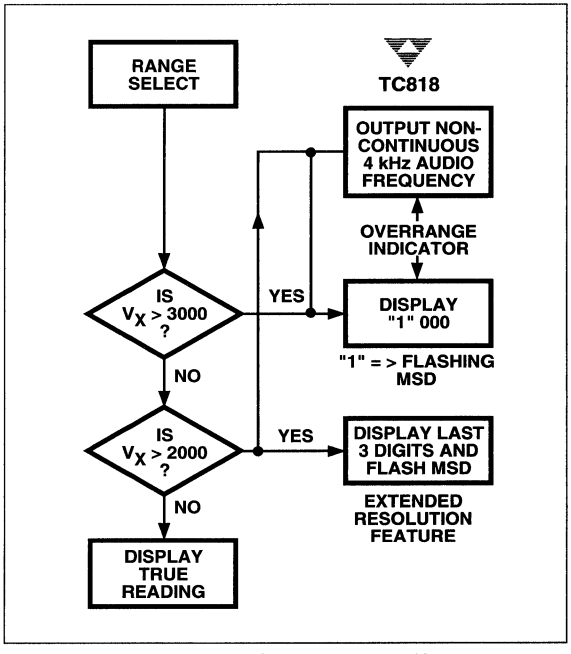


Figure 8 Manual Range Selection; Voltage Measurement

For resistance measurements, the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

–MEM Operating Mode

Bringing –MEM (Pin 61) momentarily LOW configures the "–MEM" operating mode. The –MEM LCD annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤ 99) displayed at the time MEM is LOW. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

A few examples clarify operation:

Example 1: *In Auto-Ranging*

R_I (N) = 18.21 kΩ (20 kΩ Range) ≥ Display 18.21 kΩ
MEM ≥ Store 0.21 kΩ

R_I (N + 1) = 19.87 kΩ (20 kΩ Range)
≥ Display 19.87 – 0.21 = 19.66 kΩ

R_I (N + 2) = 22.65 kΩ (200 kΩ Range)
≥ Display 22.7 kΩ and MEM Disappears

Example 2: *In Fixed Range 200Ω Full Scale*

R_I (N) = 18.2Ω ≥ Display 18.2Ω
MEM ≥ Store 8.2Ω

R_I (N + 1) = 36.7Ω
≥ Display 36.7 – 8.2 = 28.5Ω

R_I (N + 2) = 5.8Ω
≥ Display 5.8 – 8.2 = –2.4Ω*

*Will display minus resistance if following input is less than offset stored at fixed range.

Example 3: *In Fixed Range 20V Full Scale*

V_I (N) = 0.51V ≥ Display 0.51V
MEM ≥ Store 0.51V

V_I (N + 1) = 3.68V
≥ Display 3.68 – 0.51 = 3.17V

V_I (N + 2) = 0.23V
≥ Display 0.23 – 0.51 = –0.28V

V_I (N + 3) = –5.21V
≥ Display –5.21 – 0.51 = –5.72V

On power-up the, –MEM mode is not active. Once the –MEM is entered, bringing MEM to LOW again returns the TC818 to normal operation.

The –MEM mode is also cancelled whenever the measurement type (resistance, voltage, current, AC/DC, Ω/$\overline{LO\Omega}$) or range is changed. The LCD –MEM annunciator will be OFF in normal operation.

In auto-range operation, if the following input signal cannot be converted on the same range as the stored value, the –MEM mode is cancelled. The LCD annunciator is turned OFF.

The –MEM operating mode can be very useful in resistance measurements where lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied, the TC818 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option (AC/DC, Ω/$\overline{LO\Omega}$).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to V_{CC} (pin 28) and V_{SS} (pin 57) clamp the input voltage. The external 10 MΩ input resistance (see R14 and R13, Functional Diagram) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full scale (count reading <180), the next most sensitive range is selected.

An overrange voltage input condition is flagged, whenever the internal count exceeds 2000, by activating the buzzer output (pin 4). This 4 kHz signal can directly drive a piezoelectric acoustic transducer. An out-of-range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (see Figure 15).

During voltage auto-range operation, the extended resolution feature operates on the 2000V range only. (See extended resolution operating mode discussion.)

The resistance auto-range selection procedure is shown in Figure 10. The 200Ω range is the first range selected unless the low ohms resistance measurement option is selected. In low ohms operation, the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180, the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation, a continuous 4 kHz signal is output at BUZ (pin 4). An overrange input does not activate the buzzer.

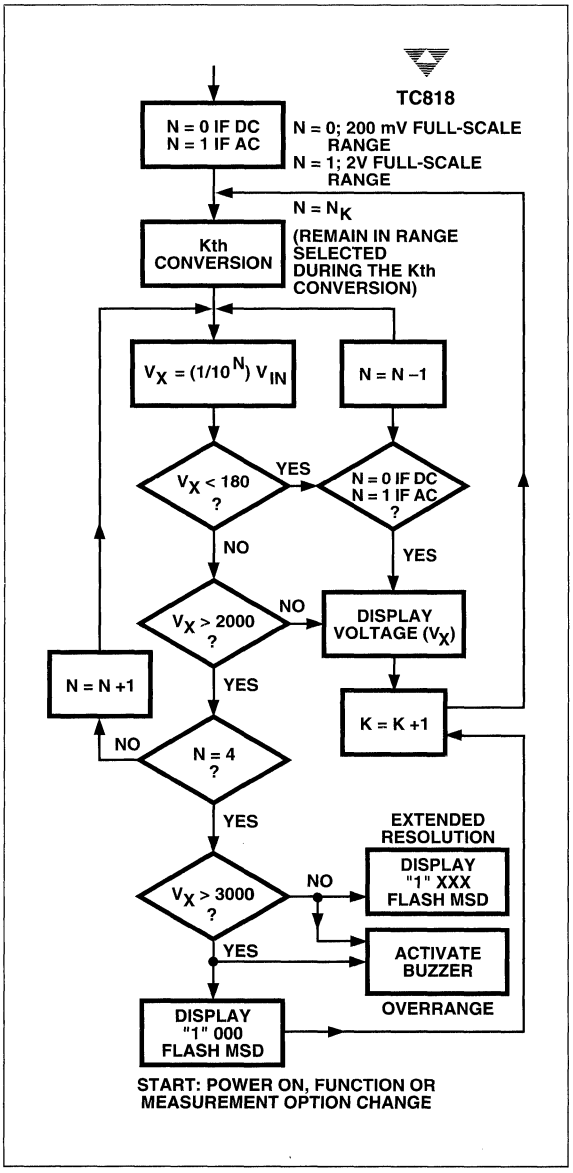


Figure 9 Auto-Range Operation; Voltage Measurement

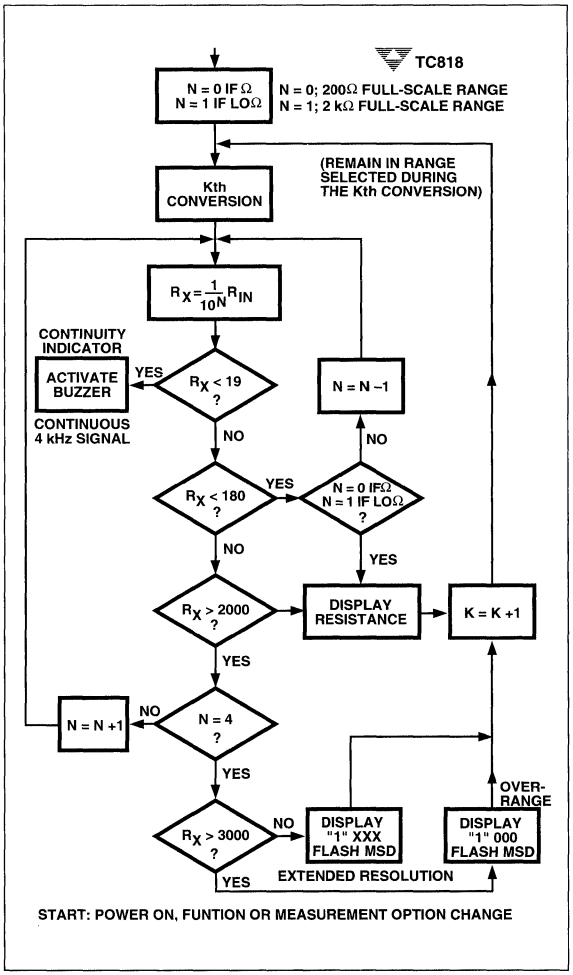


Figure 10 Auto-Range Operation; Resistance Measurement

Out-of-range input conditions are displayed by a blinking MSD with the three LSDs set to "000," and by the fully extended bar-graph.

The extended resolution feature operates only on the 200 kΩ and 2000V full-scale ranges during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three LSDs display data normally.

Low-Battery Detection Circuit

The TC818 contains a low-battery detector. When the 9V battery supply has been depleted to a 7V nominal value, the LCD low-battery annunciator is activated.

The low-battery detector is shown in Figure 11. The low-battery annunciator is guaranteed to remain OFF with the battery supply greater than 7V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3V.

Triplex Liquid Crystal Display (LCD) Drive

The TC818 directly drives a triplexed LCD using 1/3 bias drive. All numeric data, decimal point, polarity, and function annunciator drive signals are developed by the TC818A. The bar-graph data are sent to the TC818D. A direct connection to a triplex LCD is possible without external drive electronics. Standard and custom LCDs are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component, for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is:

$V_{CC} - V_{DISP}$

For example, if V_{DISP} is set at a potential 3V below V_{CC}, the peak drive signal is:

$V_P = V_{CC} - V_{DISP} = 3V$

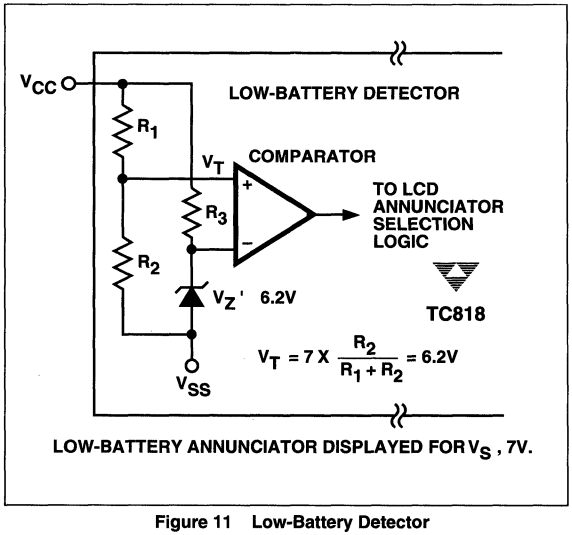


Figure 11 Low-Battery Detector

An "OFF" LCD segment has an RMS voltage of $V_P/3$ across it or 1V. An "ON" segment has a 0.63 V_P signal across it or 1.92V for $V_{CC} - V_{DISP} = 3V$.

Since the V_{DISP} pin is available, the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing V_P signal across it or 1.92V for $V_{CC} - V_{DISP} = 3V$.

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a –5 to –20 mV/°C temperature coefficient can be applied to V_{DISP} to accommodate the liquid crystal temperature operating characteristics, if necessary.

The TC818A and TC818D internally generate two intermediate LCD drive potentials (V_H and V_L) from resistive dividers (Figure 12) between V_{CC} and V_{DISP}. The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground, $V_P \approx 5V$.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting waveforms for "ON" and "OFF" RMS voltage levels across a selected numeric LCD element.

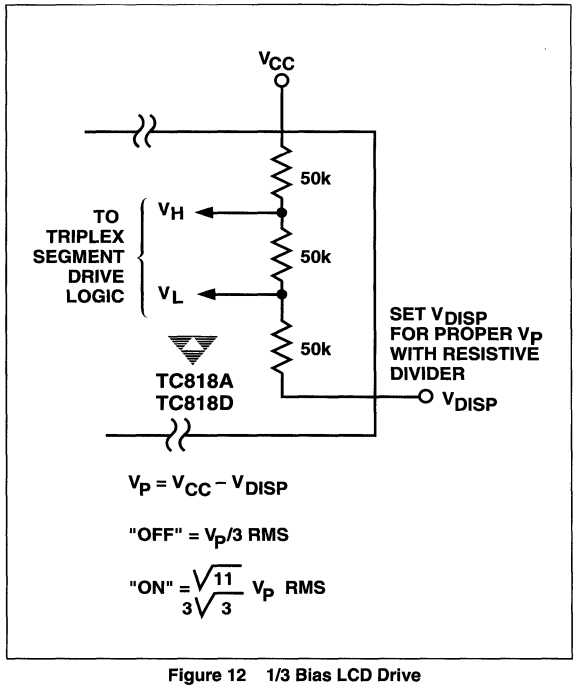


Figure 12 1/3 Bias LCD Drive

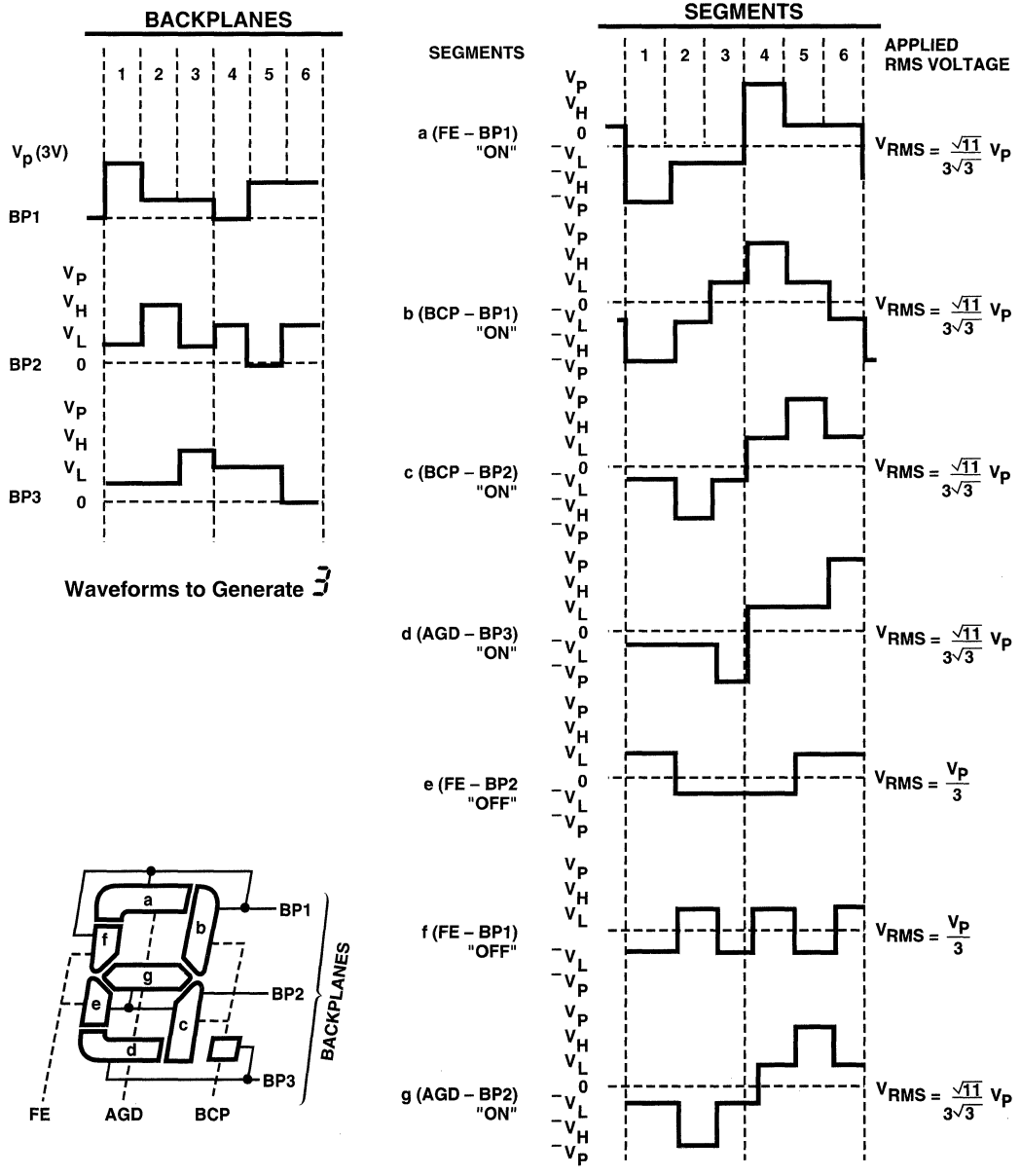


Figure 13 Triplex LCD Drive Waveforms

Liquid Crystal Displays (LCDs)

Most users design their own custom LCD. However, for prototyping purposes, a standard display is available from Varitronix, Ltd. The prototype display configuration is shown in Figure 14.

- Varitronix Ltd.
  9/F Liven House, 61-63, King Yip Street
  Kwun Tjong, Hong Kong
  Tel: 3-410286
  Telex: 36643 VTRAX HX
  FAX: 852-3-439555

  Part No. VIM-328-DP

- USA Office:
  VL Electronics Inc.
  3171 Los Feliz Blvd, #303
  Los Angeles, CA 0039
  Tel: (213) 738-8700

External Crystal

The TC818 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 ms (≈2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

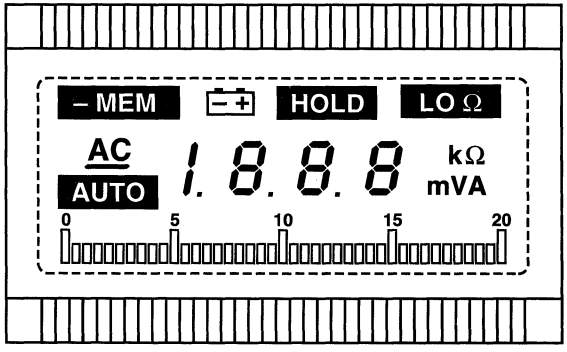
Several crystal sources exist. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  Telex: 67-8394

- Daiwa Sinku Corporation
  1389, Shinzaike – AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211

- International Piezo LTD
  24-26 Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HZ
  Tel: 3-3501151

Contact manufacturer for full specifications.



PAD	BP1	BP2	BP3	PAD	BP1	BP2	BP3
1	—	—	SCALE	19	—	—	BP3
2	X0	X1	X2	20	—	BP2	—
3	X5	X4	X3	21	BP1	—	—
4	X6	X7	X8	22	—	LOΩ	A
5	X11	X10	X9	23	—	Ω	V
6	X12	X13	X14	24	HOLD	k	m
7	X17	X16	X15	25	4B	4C	—
8	X18	X19	X20	26	4A	4G	4D
9	X23	X22	X21	27	4F	4E	—
10	X24	X25	X26	28	3B	3C	3P
11	X29	X28	X27	29	3A	3G	3D
12	X30	X31	X32	30	3F	3E	—
13	X35	X34	X33	31	2B	2C	2P
14	X36	X37	X38	32	2A	2G	2D
15	—	X40	X39	33	2A	2G	2D
16	BP1	—	—	34	1B	1C	1P
17	—	BP2	—	35	Z	–MEM	—
18	—	—	BP3	36	AC	y	AUTO

Figure 14 Typical LCD Configuration, TC818 Triplex

"Buzzer" Drive Signal

The BUZ output (pin 4) will drive a piezoelectric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement, a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a noncontinuous 4 kHz signal at the BUZ output. The LCD most significant digit also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The BUZ output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from V_{CC} (pin 28) to DGND (pin 58). The signal is at V_{CC} when not active.

The BUZ output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance), or measurement option (AC/DC, Ω/$\overline{\text{LO}\Omega}$), also activates the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.

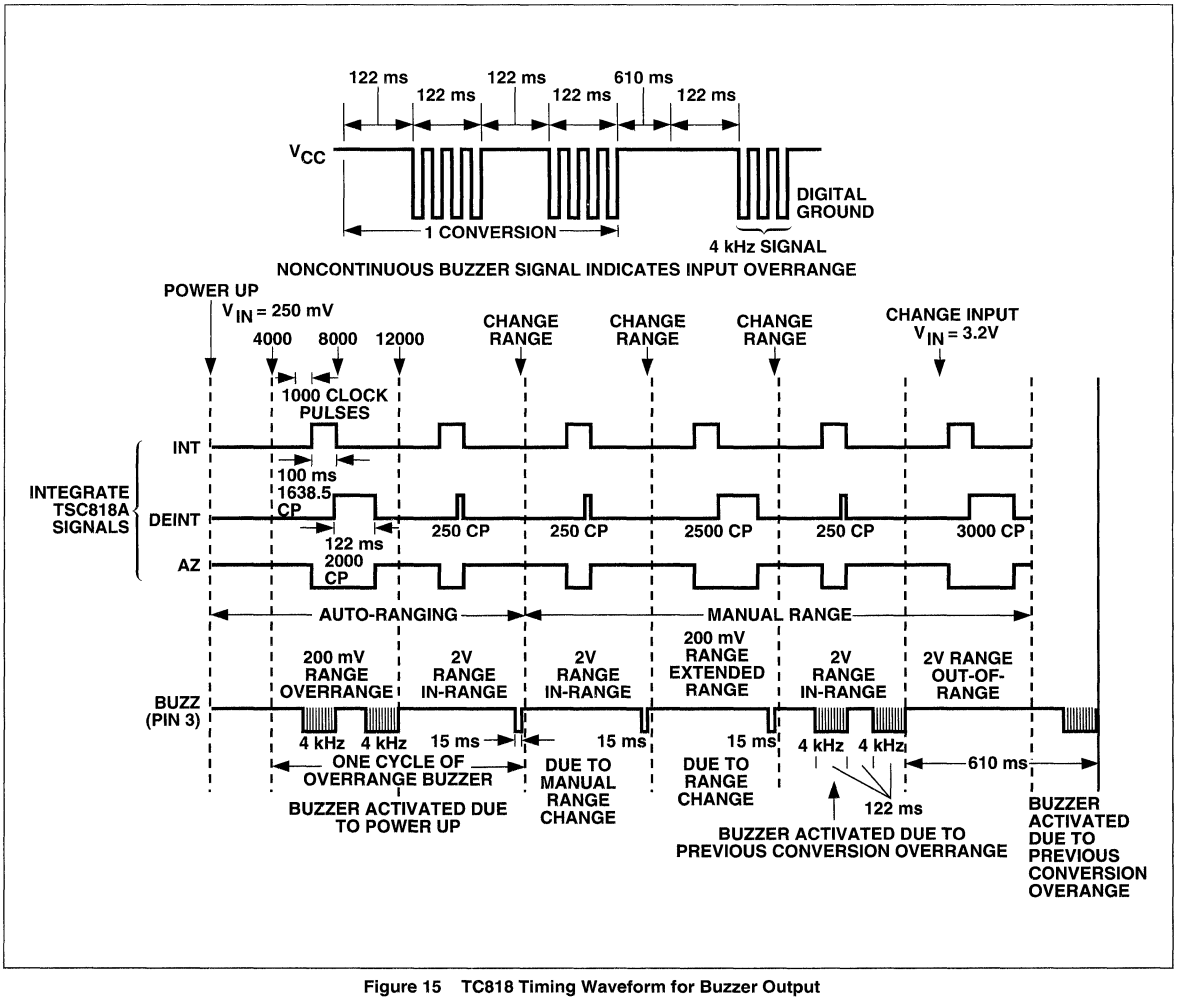


Figure 15 TC818 Timing Waveform for Buzzer Output

Vendors for piezoelectric audio transducers are:

- Gulton Industries
  Piezo Products Division
  212 Durham Avenue
  Metuchen, New Jersey 08840
  (201) 548-2800
  Typical P/Ns: 102-95NS, 101-FB-00
- Taiyo Yuden (USA) Inc.
  Arlington Center
  714 West Algonquin Road
  Arlington Heights, Illinois 60005
  Typical P/Ns: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TC818 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range, as shown in Table V.

Table V. Decimal Point Selection

Full-Scale Range	1 * 9 DP3	* 9 DP2	* 9 DP1
2000V, 2000 kΩ	OFF	OFF	OFF
200V, 200 kΩ	OFF	OFF	ON
20V, 20 kΩ	OFF	ON	OFF
2V, 2 kΩ	ON	OFF	OFF
200V, 200Ω	OFF	OFF	ON
200 mV, 200Ω	OFF	OFF	ON
20 mA	OFF	ON	OFF
200 mA	OFF	OFF	ON

AC-to-DC Converter Operational Amplifier

The TC818 contains an on-chip operational amplifier that may be connected as a rectifier for AC-to-DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/μs
- Unity-Gain Bandwidth: 0.4 MHz
- Open-Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) ±1.5V (Referenced to Analog Common)

When the AC measurement option is selected, the input buffer receives an input signal through switch S14 rather than switch S11 (see Figure 1). With external circuits, the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection

Integration Resistor Selection

The TC818 automatically selects one of two external integration resistors. RVIBUF (pin 55) is selected for voltage and current measurement. RΩBUF (pin 54) is selected for resistance measurements.

RVIBUF Selection (Pin 55)

In auto-range operation, the TC818 operates with a 200 mV maximum full-scale potential at V_I (pin 44). Resistive dividers at VR2 (pin 41), VR3 (pin 40), VR4 (pin 43), and VR5 (pin 42) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode, the extended operating mode is activated giving a 300 mV full-scale potential at V_I (pin 44).

The integrator output swing should be maximized, but saturations must be avoided. The integrator will swing within 0.45V of V_{CC} (pin 28) and 0.5V of V_{SS} (pin 57) without saturating. A ±2V swing is suggested. The value of RVIBUF is easily calculated, assuming a worst-case extended resolution input signal:

$$RVIBUF = \frac{V_{MAX}\ (t_I)}{V_{INT}\ (C_I)} \approx 150\ k\Omega$$

where:

V_{INT} = Integrator swing = ±2V
t_I = Integration time = 100 ms
C_I = Integration capacitor = 0.1 μF
V_{MAX} = Maximum input at V_I = 300 mV

RWBUF Selection (Pin 51)

In ratiometric resistance measurements, the signal at R_X (pin 50) is always positive with respect to analog common. The integrator swings negative.

The worst-case integrator swing is for the 200Ω range with the manual, extended resolution option.

The input voltage, V_X (pin 50) is easily calculated (Figure 16):

$$R\Omega BUF = \frac{(V_{CC} - V_{ANCOM})\ R_X}{(R_X + R_S + R_1 + R_S)} = 0.63V$$

where:

V_{ANCOM} = Potential at analog common ≈ 2.7V
R_S = 220Ω
R_I = 163.85Ω
R_X = 300Ω
R_S = Internal switch 33 resistance ≈ 600Ω

For a 3.1V integrator swing, the value of RΩBUF is easily calculated:

$$R\Omega BUF = \frac{(V_X\ Max)\ (t_I)}{C_I\ (V_{INT})} \approx 220\ k\Omega$$

where:

V_{INT} = Integrator swing = 3.1V
t_I = Integration time = 100 ms
C_I = Integration capacitor = 0.1 µF
R_X Max = 300Ω
V_X Max = 700 mV

With a low battery voltage of 6.6V, analog common will be approximately 3.6V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply, a 3.1V swing will set the integrator output to 0.5V above the negative supply.

Capacitors — C_{INT}, C_{AZ} and C_{REF}

The integration capacitor, C_{INT}, must have low dielectric absorption. A 0.1 µF polypropylene capacitor is suggested. The auto-zero capacitor, C_{AZ}, and reference capacitor, C_{REF}, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

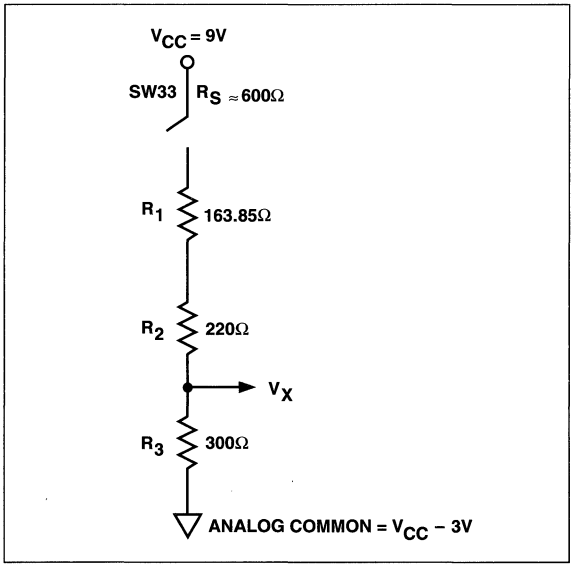


Figure 16 RΩBUF Calculation (200Ω Manual Operation)

Reference Voltage Adjustment

The TC818 contains a low temperature drift internal voltage reference. The analog common potential (pin 29) is established by this reference. Maximum drift is a low 75 ppm/°C. Analog common is designed to be approximately 2.6V below V_{CC} (pin 28). A resistive divider (R18/R19, Functional Diagram) sets the TC818 reference input voltage (REFHI, pin 34) to approximately 163.85 mV.

With an input voltage near full scale on the 200 mV range, R19 is adjusted for the proper reading.

Display Hold Feature

The LCD will not be updated when $\overline{HOLD}$ (pin 60) is connected to GND (pin 58). Conversions are made, but the display is not updated. A $\overline{HOLD}$ mode LCD annunciator is activated when $\overline{HOLD}$ is low.

The LCD $\overline{HOLD}$ annunciator is activated through the triplex LCD driver signal at pin 13.

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

- Nepenthe Distribution
  2471 East Bayshore, Suite 520
  Palo Alto, CA 94303
  (415) 856-9332
  TWX: 910-373-2060
  "CBQ" Socket, Part No. IC51-064-042

Resistive Ladder Networks

Resistor attenuator networks for voltage and resistance measurements are available from:

- Caddock Electronics
  1717 Chicago Avenue
  Riverside, CA 92507
  Tel: (714) 788-1700
  TWX: 910-332-6108

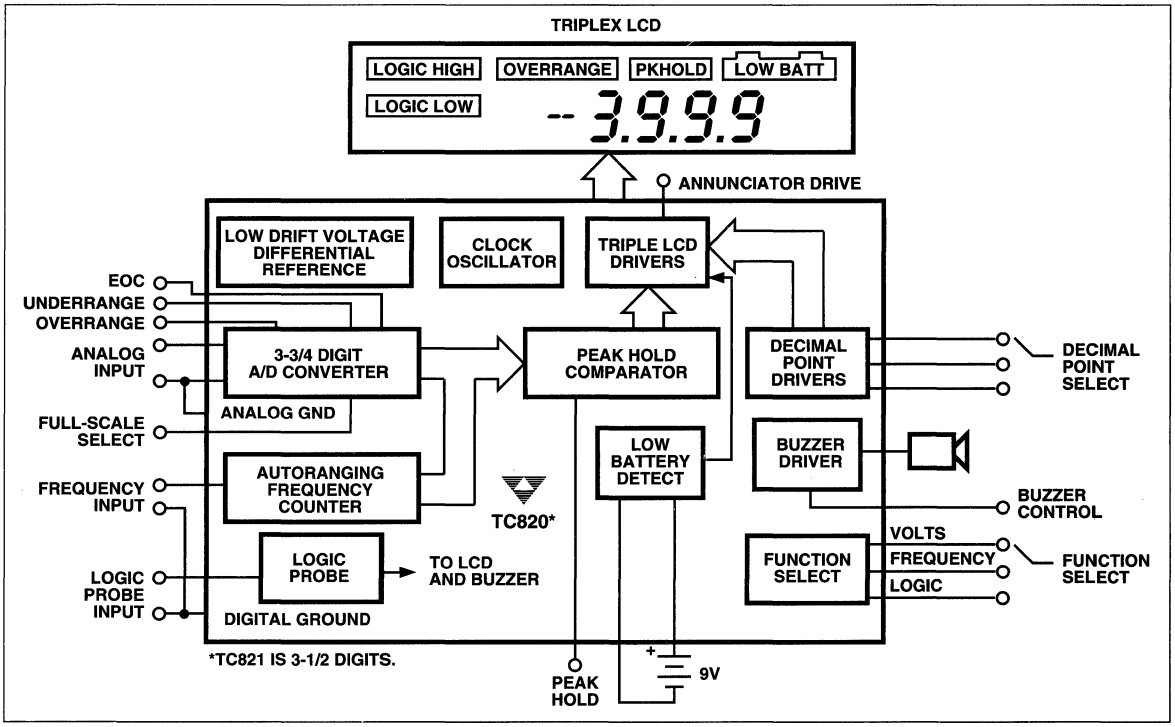
Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T1794-204-1

DISPLAY A/D CONVERTERS WITH FREQUENCY COUNTER AND LOGIC PROBE

FEATURES

- Multiple-Function Measurement System
  - — Analog-to-Digital Converter
  - — Frequency Counter
  - — Logic Probe
- Frequency Counter
  - — Measures Input Frequency to 4 MHz
  - — Auto-Ranging Over Four-Decade Range
- Logic Probe Inputs
  - — Two LCD Annunciators
  - — Buzzer Drive
- Peak Reading Hold With LCD Annunciator
- 3-3/4 Digit (3999 Maximum) Resolution (TC820)
- 3-1/2 Digit (1999 Maximum) Resolution (TC821)
- Low Noise A/D Converter
  - — Differential Inputs, 1 pA Bias Current
  - — Differential Reference for Ratiometric Ohms
  - — On-Chip Voltage Reference, 50 ppm/°C Drift
- No External LCD Drivers Required
  - — Full 3-3/4 Digit Display
  - — Displays "OL" for Input Overrange
  - — Three Decimal Point and Polarity Drivers
  - — LCD Annunciator Drive
  - — Adjustable LCD Drive Voltage
- Low Battery Detect With LCD Annunciator
- On-Chip Buzzer Driver and Control Input
- Control Input Changes Full Scale Range by 10:1
- Data Hold Input
- Underrange and Overrange Outputs
- Multiple Package Options
  - — 40-Pin DIP
  - — 44-Pin Flat Package or PLCC

SIMPLIFIED BLOCK DIAGRAM



TC820 (3-3/4 DIGIT)
TC821 (3-1/2 DIGIT)

GENERAL DESCRIPTION

The TC820 is a 3-3/4 digit measurement system combining an integrating analog-to-digital converter, frequency counter, and logic level tester in a single package. The TC820 supersedes the TC7106 in new designs by improving performance and reducing system cost. The TC820 adds features that are difficult, expensive, or impossible to provide with older A/D converters (see the competitive evaluation). The high level of integration permits TC820-based instruments to deliver higher performance and more features, while actually reducing parts count.

Fabricated in low-power CMOS, the TC820 directly drives a 3-3/4 digit (3999 maximum) LCD. The TC821 includes all features of the TC820, but with a resolution of 3-1/2 digits (1999 maximum).

With a maximum range of 3999 counts, the TC820 provides 10 times greater resolution in the 200 mV to 400 mV range than traditional 3-1/2 digit meters. An auto-zero cycle guarantees a zero reading with a 0V input. CMOS processing reduces analog input bias current to only 1 pA. Rollover error, the difference in readings for equal magnitude but opposite polarity input signals, is less than ±1 count. Differential reference inputs permit ratiometric measurements for ohms or bridge transducer applications.

The TC820's frequency counter option simplifies design of an instrument well-suited to both analog and digital troubleshooting: voltage, current, and resistance measurements, plus precise frequency measurements to 4 MHz (higher frequencies can be measured with an external prescaler), and a simple logic probe. The frequency counter will automatically adjust its range to match the input frequency, over a four-decade range.

Two logic level measurement inputs permit a TC820-based meter to function as a logic probe. When combined with external level shifters, the TC820 will display logic levels on the LCD and also turn on a piezoelectric buzzer when the measured logic level is low.

Other TC 820 features simplify instrument design and reduce parts count. On-chip decimal point drivers are included, as is a low battery detection annunciator. A piezoelectric buzzer can be controlled with an external switch or by the logic probe inputs. Two oscillator options are provided: A crystal can be used if high accuracy frequency measurements are desired, or a simple RC option can be used for low-end instruments.

A "peak reading hold" input allows the TC820 to retain the highest A/D or frequency reading. This feature is useful in measuring motor starting current, maximum temperature, and similar applications.

A family of instruments can be created with the TC821 and TC820. No additional design effort is required to create instruments with 3-1/2 and 3-3/4 digit resolution. The TC821 can also reduce parts count in existing high-end 7106-type designs.

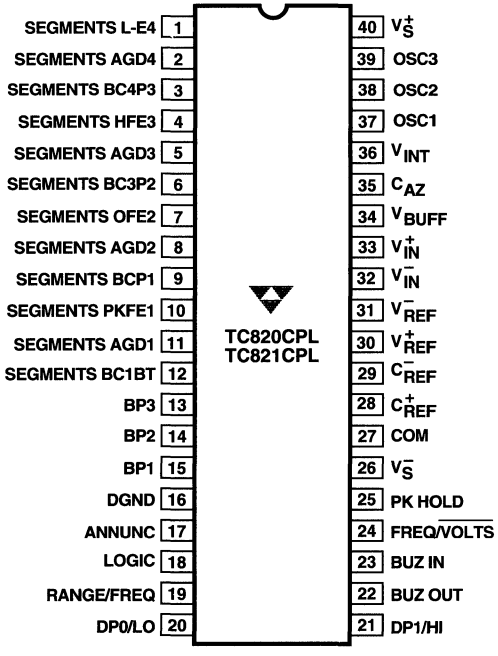
The TC820 and TC821 operate from a single 9V battery, with typical power of 10 mW. Packages include a 40-pin DIP, 44-pin plastic flat package, and 44-pin PLCC.

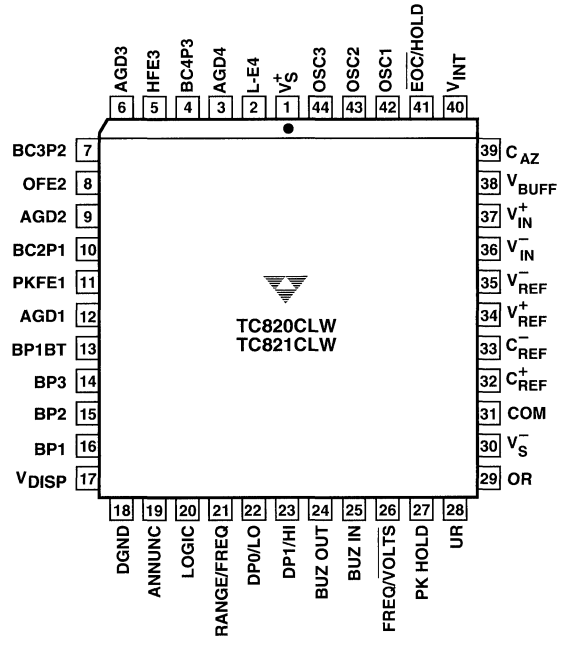
COMPETITIVE EVALUATION

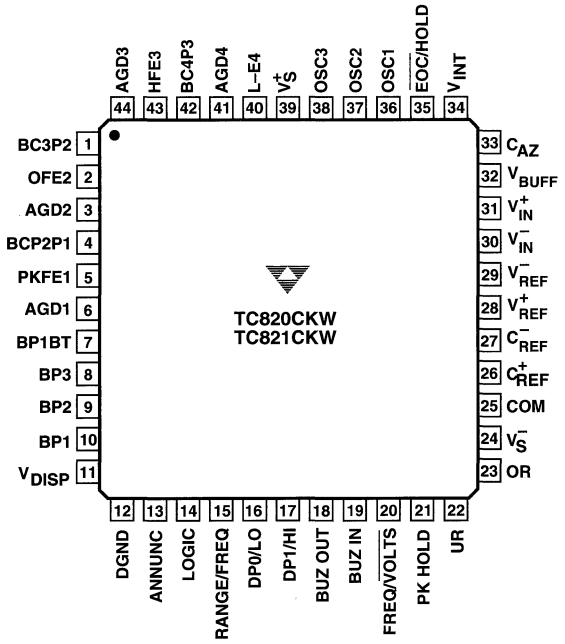
Features Comparison	TC820	7106
3-3/4 Digit Resolution	Yes	No
Auto-Ranging Frequency Counter	Yes	No
Logic Probe	Yes	No
Decimal Point Drive	Yes	No
Peak Reading Hold (Frequency or Voltage)	Yes	No
Display Hold	Yes	No
Simple 10:1 Range Change	Yes	No
Buzzer Drive	Yes	No
Low Battery Detection With Annunciator	Yes	No
Overrange Detection With Annunciator	Yes	No
Low Drift Reference	Yes	No
Underrange/Overrange Logic Output	Yes	No
Input Overload Display	"OL"	"1"
LCD Annunciator Driver	Yes	No
LCD Drive Type	Triplexed	Direct
LCD Pin Connections	15	24
LCD Elements	36	23

2

PIN CONFIGURATIONS







ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage (V_S^+ to GND) 15V
Analog Input Voltage (Either Input) (Note 1) .... V_S^+ to V_S^-
Reference Input Voltage (Either Input) ..... V_S^+ to V_S^-
Digital Inputs ..... V_S^+ to DGND
V_{DISP} ..... V_S^+ to DGND –0.3V
Power Dissipation, Plastic Package (Note 2) ..... 800 mW
Operating Temperature Range
"C" Devices ..... 0°C to +70°C
"E" Devices ..... – 40°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Static-sensitive devices. Unused devices should be stored in conductive material to protect against static discharge and static fields

NOTES:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 9V, T_A = 25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV (V_{FS} = 200 mV for TC821)	– 000	±000	+000	Digital Reading
RE	Roll-Over Error	V_{IN} = ±390 mV Full-Scale = 400 mV (V_{IN} = ±190 mV, V_{FS} = 200 mV for TC821)	– 1	±0.2	+1	Counts
NL	Nonlinearity (Maximum Deviation From Best Straight Line Fit)	Full-Scale = 400 mV (V_{FS} = 200 mV for TC821)	– 1	±0.2	+1	Count
	Ratiometric Reading	V_{IN} = V_{REF}, TC820 V_{IN} = V_{REF}, TC821	1999 999	1999/2000 999/1000	2000 1000	Digital Reading
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 400 mV (V_{FS} = 200 mV for TC820)	—	50	—	µV/V
VCMR	Common-Mode Voltage Range	Input High, Input Low	V_S^- + 1.5	—	V_S^+ – 1	V
e_N	Noise (P-P Value Not Exceeded 95% of Time)	V_{IN} = 0V Full-Scale = 400 mV (V_{FS} = 200 mV for TC820)	—	15	—	µV
I_{IN}	Input Leakage Current	V_{IN} = 0V T_A = 25°C 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	— — —	1 20 100	10 — —	pA
V_{COM}	Analog Common Voltage	25 kΩ Between Common and V_S^+ (V_S^+ – V_{COM})	3.15	3.3	3.45	V
V_{CTC}	Common Voltage Temperature Coefficient	25 kΩ Between Common and V_S^+ 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	— —	35 50	50 —	ppm/°C
TC_{ZS}	Zero Reading Drift	V_{IN} = 0V 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	—	0.2 1	—	µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 399 mV (V_{IN} = 199 mV for TC821) 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C Ext Ref = 0 ppm/°C	— —	1 5	5 —	ppm/°C

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Supply Current	V_{IN} = 0V	—	1	1.5	mA
	Peak-to-Peak Backplane Drive Voltage	V_S = 9V V_{DISP} = DGND	4.5	4.7	5.3	V
	Buzzer Frequency	f_{OSC} = 40 kHz	—	5	—	kHz
	Counter Timebase Period	f_{OSC} = 40 kHz	—	1	—	Second
	Low Battery Flag Voltage	V_S^+ to V_S^-	6.7	7	7.3	V
V_{IL}	Input Low Voltage		—	—	DGND + 1.5	V
V_{IH}	Input High Voltage		$V_S^+ - 1.5$	—	—	V
V_{OL}	Output Low Voltage, UR, OR Outputs	I_L = 50 µA	—	—	DGND + 0.4	V
V_{OL}	Output High Voltage, UR, OR Outputs	I_L = 50 µA	$V_S^+ - 1.5$	—	—	V
	Control Pin Pull-Down Current	$V_{IN} = V_S^+$	—	5	—	µA

PIN DESCRIPTION

Pin No. (40-Pin Package)	Pin No. (44-Pin Flat Package)	Symbol	Description
1	40	L-E4	LCD segment driver for L ("logic LOW"), polarity, and "e" segment of most significant digit (MSD).
2	41	AGD4	LCD segment drive for "a," "g," and "d" segments of MSD.
3	42	BC4P3	LCD segment drive for "b" and "c" segments of MSD and decimal point 3.
4	43	HFE3	LCD segment drive for H ("logic HIGH"), and "f" and "e" segments of third LSD.
5	44	AGD3	LCD segment drive for "a," "g," and "d" segments of third LSD.
6	1	BC3P2	LCD segment drive for "b" and "c" segments of third LSD and decimal point 2.
7	2	OFE2	LCD segment drive for "overrange," and "f" and "e" segments of second LSD.
8	3	AGD2	LCD segment drive for "a," "g," and "d" segments of second LSD.
9	4	BC2P1	LCD segment drive for "b " and "c" segments of second LSD and decimal point 1.
10	5	PKFE1	LCD segment drive for "hold peak reading," and "f" and "e" segments of LSD.
11	6	AGD1	LCD segment drive for "a," "g," and "d" segments of LSD.
12	7	BC1BT	LCD segment drive for "b" and "c" segments of LSD and "low battery."
13	8	BP3	LCD backplane #3.
14	9	BP2	LCD backplane #2.
15	10	BP1	LCD backplane #1.
—	11	V_{DISP}	Sets peak LCD drive signal: $V_{PEAK} = (V_S^+) - V_{DISP}$. V_{DISP} may also be used to compensate for temperature variation of LCD crystal threshold voltage.
16	12	DGND	Internal logic digital ground, the logic "0" level. Nominally 4.7V below V_S^+.
17	13	ANNUNC	Square-wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin Package)	Pin No. (44-Pin Flat Package)	Symbol	Description
18	14	LOGIC	Logic mode control input. When connected to V_S^+, the converter is in logic mode. The LCD displays "OL" and the decimal point inputs control the HIGH and LOW annunciators. When the "low" annunciator is on, the buzzer will also be on. When unconnected or connected to DGND, the TC820 is in the voltage/frequency measurement mode. This pin has a 5 µA internal pull-down to DGND.
19	15	RANGE/ FREQ	Dual-purpose input. In range mode, when connected to V_S^+, the integration time will be 200 counts instead of 2000 counts (100 instead of 1000 counts for TC821), and the LCD will display the analog input divided by 10. (See text for limitation with TC820.) In frequency mode, this pin is the frequency input. A digital signal applied to this pin will be measured with a 1-second time base. There is an internal 5 µA pull-down to DGND.
20	16	DP0/LO	Dual-purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to V_S^+ will turn on the "low" LCD segment. There is an internal 5 µA pull-down to DGND in volts mode only. Decimal point logic: DP1 DP0 Decimal Point Selected 0 0 None 0 1 DP1 1 0 DP2 1 1 DP3
21	17	DP1/HI	Dual-purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to V_S^+ will turn on the "high" LCD segment. There is an internal 5 µA pull-down to DGND in volts mode only.
22	18	BUZOUT	Buzzer output. Audio frequency, 5 kHz, output which drives a piezoelectric buzzer.
23	19	BUZIN	Buzzer control input. Connecting BUZIN to V_S^+ turns the buzzer on. BUZIN is logically ORed (internally) with the "logic level low" input. There is an internal 5 µA pull-down to DGND.
24	20	FREQ/ $\overline{\text{VOLTS}}$	Voltage or frequency measurement select input. When unconnected, or connected to DGND, the A/D converter function is active. When connected to V_S^+, the frequency counter function is active. This pin has an internal 5 µA pull-down to DGND.
25	21	PKHOLD	Peak hold input. When connected to V_S^+, the converter will only update the display if a new conversion value is greater than the preceding value. Thus, the peak reading will be stored and held indefinitely. When unconnected, or connected to DGND, the converter will operate normally. This pin has an internal 5 µA pull-down to DGND.
	22	UR	Underrange output. This output will be HIGH when the digital reading is 380 counts or less (≤180 counts for TC821).
	23	OR	Overrange output. This output will be HIGH when the analog signal input is greater than full scale. The LCD will display "OL" when the input is overranged.
26	24	V_S^-	Negative supply connection. Connect to negative terminal of 9V battery.
27	25	COM	Analog circuit ground reference point. Nominally 3.3V below V_S^+.
28	26	C_{REF}^+	Positive connection for reference capacitor.
29	27	C_{REF}^-	Negative connection for reference capacitor.
30	28	V_{REF}^+	High differential reference input connection.
31	29	V_{REF}^-	Low differential reference input connection.
32	30	V_{IN}^-	Low analog input signal connection.

2

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin Package)	Pin No. (44-Pin Flat Package)	Symbol	Description
33	31	V_{IN}^+	High analog input signal connection.
34	32	V_{BUFF}	Buffer output. Connect to integration resistor.
35	33	C_{AZ}	Auto-zero capacitor connection.
36	34	V_{INT}	Integrator output. Connect to integration capacitor.
	35	$\overline{EOC}$/ HOLD	Bidirectional pin. Pulses low (i.e., from V_S^+ to DGND) at the end of each conversion. If connected to V_S^+, conversions will continue, but the display is not updated.
37	36	OSC1	Crystal oscillator (input) connection.
38	37	OSC2	Crystal oscillator (output) connection.
39	38	OSC3	RC oscillator connection.
40	39	V_S^+	Positive power supply connection, typically 9V.

ORDERING INFORMATION

Surface-Mount Devices

Part No.	Resolution	Package	Temperature Range
TC820CKW	3-3/4 Digits	44-Pin Plastic Flat Package	0°C to +70°C
TC820CLW	3-3/4 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	0°C to +70°C
TC820EKW	3-3/4 Digits	44-Pin Plastic Flat Package	–40°C to +85°C
TC820ELW	3-3/4 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	–40°C to +85°C
TC821CKW	3-1/2 Digits	44-Pin Plastic Flat Package	0°C to +70°C
TC821CLW	3-1/2 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	0°C to +70°C
TC821EKW	3-1/2 Digits	44-Pin Plastic Flat Package	–40°C to +85°C
TC821ELW	3-1/2 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	–40°C to +85°C

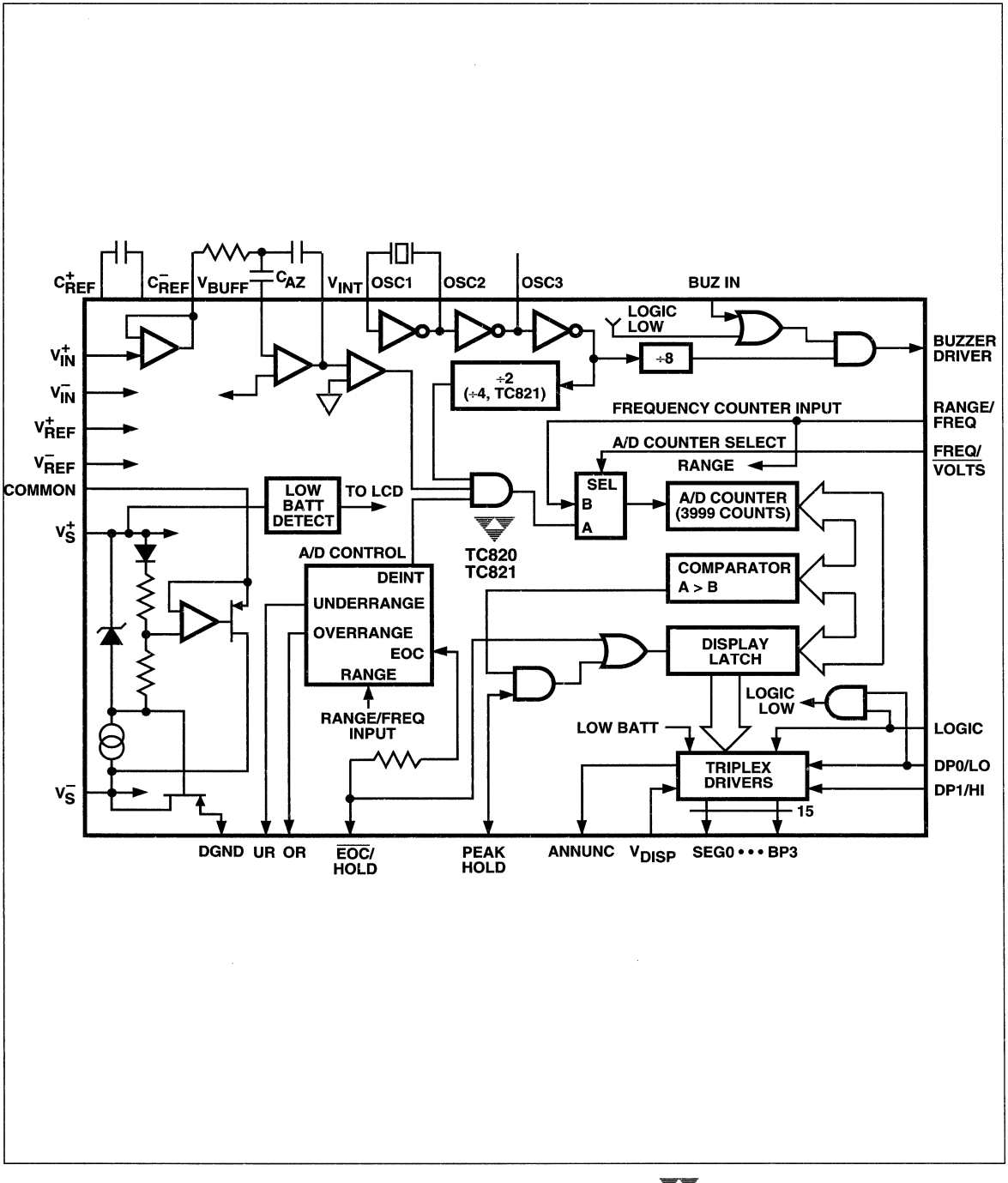
40-Pin DIPs

Part No.	Resolution	Temperature Range
TC820CPL	3-3/4 Digits	0°C to +70°C
TC820EPL	3-3/4 Digits	–40°C to +85°C
TC821CPL	3-1/2 Digits	0°C to +70°C
TC821EPL	3-1/2 Digits	–40°C to +85°C

TC820/TC821 Comparison

Feature	Device TC820	TC821
Resolution	3-3/4 Digits	3-1/2 Digits
All Other Features (Counter, Logic, etc.)	Yes	Yes

FUNCTIONAL BLOCK DIAGRAM



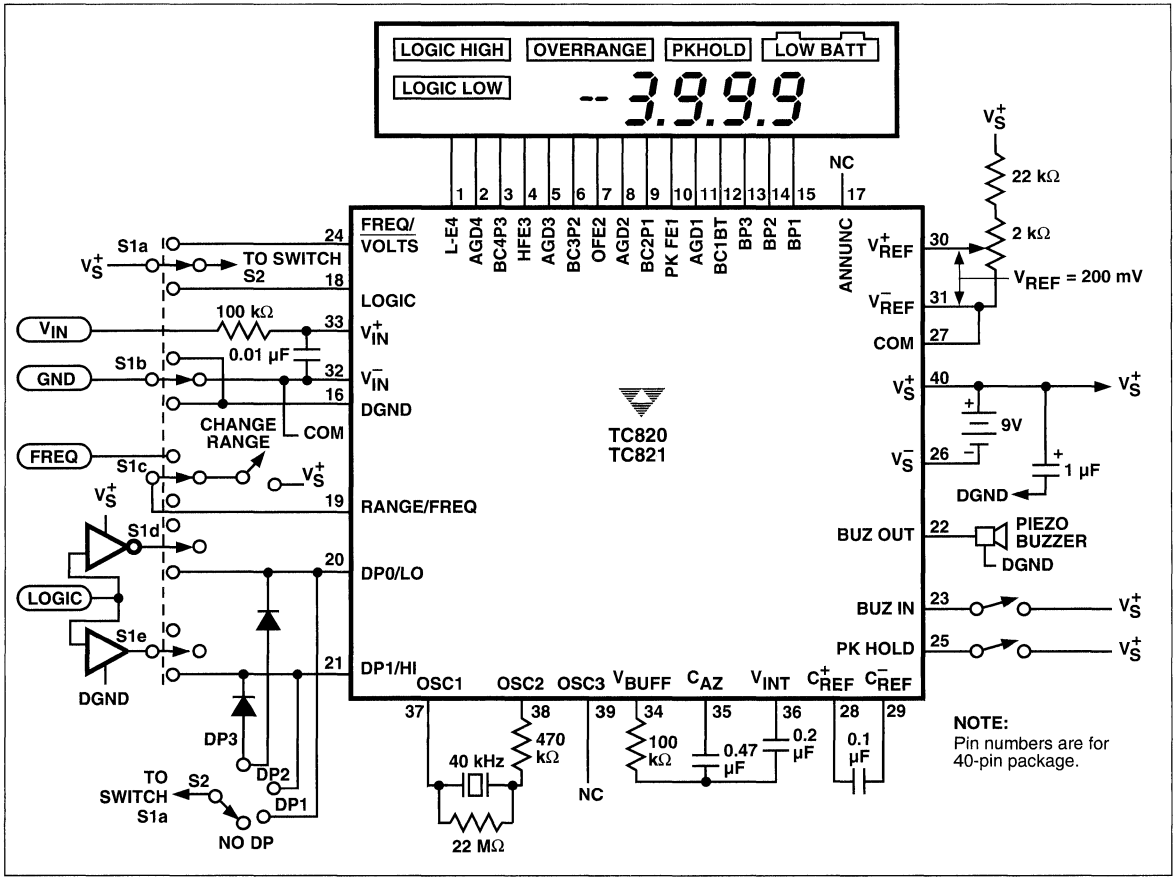


Figure 1. Typical Operating Circuit

FEATURES

The TC820 and TC821 combine the features of an analog-to-digital converter (ADC), frequency counter, and logic probe, in a single CMOS-integrated circuit. All of the TC820 features are shown graphically in the functional diagram. With on-chip voltage reference and LCD drive circuitry, the TC820 simplifies the design of multi-mode measurement instruments.

The TC820 has a resolution of 3-3/4 digits (3999 maximum), while the TC821 has a resolution of 3-1/2 digits (1999 maximum). The features of both converters are the same, so that both 3-3/4 digit and 3-1/2 digit designs can be produced with only one PC board design. The differences between the TC820 and the TC821 primarily affect system timing, and are noted in the appropriate sections of the data sheet.

GENERAL THEORY OF OPERATION

Dual-Slope conversion Principles

The TC820 analog-to-digital converter operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC820 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input Signal Integration
(2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated

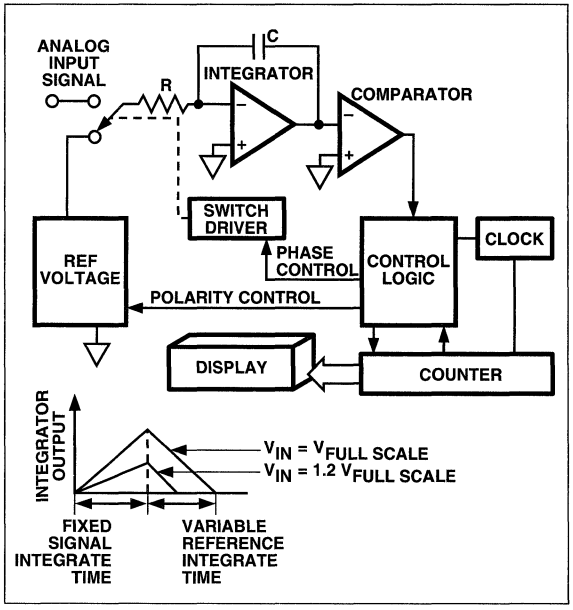


Figure 2. Basic Dual-Slope Converter

conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

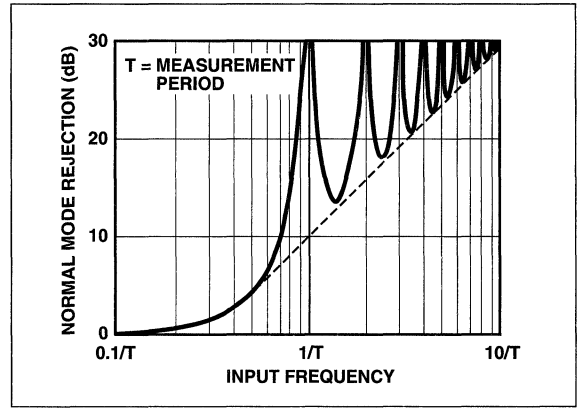


Figure 3. Normal-Mode Rejection of Dual-Slope Converter

until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where: V_{REF} = Reference voltage
t_{INT} = Integration time
t_{DEINT} = Deintegration time

For a constant t_{INT}:

$$V_{IN} = V_{REF} \times \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large

TC820 THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC820 design incorporates a "zero integrator output" phase and an "auto-zero" phase. These additional phases ensure that the integrator starts at 0V (even after a severe overrange conversion), and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Zero Integrator Output
(2) Auto-Zero
(3) Signal Integrate
(4) Reference Deintegrate

Zero Integrator Output Phase

This phase guarantees that the integrator output is at 0V before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an overrange conversion. The duration of this phase is 500 counts plus the unused deintegrate counts, for both the TC820 and TC821.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches, and the internal nodes are shorted to Analog Common (0V ref) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The auto-zero phase residual is typically 10 μV to 15 μV. The auto-zero duration is 1500 counts (750 counts for TC821).

Signal Integration Phase

Upon completion of the auto-zero phase, the auto-zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period, which is 2000 counts (4000 clock periods) in the TC820, and 1000 counts (4000 clock periods) in the TC821. The externally-set clock frequency is divided by two (TC820) or four (TC821) before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

Note that for the same clock frequency, the TC820 and TC821 have the same signal integration time. Therefore, the noise rejection performance of the two converters will be the same.

The differential input voltage must be within the device's common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, as in battery-powered applications, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection that is limited only by device noise and auto-zero residual offsets.

Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the auto-zero phase, is connected to the input of the integrating amplifier. The internal sign logic ensures the polarity of the reference voltage is always connected in the phase opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase:

$$t_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC820 is:

$$\text{Digital Count} = 2000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

For the TC821, the digital reading displayed is:

$$\text{Digital Count} = 1000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

System Timing

The oscillator frequency is divided by 2 (4 for TC821) prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 8000 (4000) counts or 16000 (16000) clock pulses. The 8000 (4000) count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

Conversion Phase	TC820	TC821	Units
1) Auto-Zero:	1500	500	Counts
2) Signal Integrate:[1,2]	2000	1000	Counts
3) Reference Integrate:	1 to 4001	1 to 2001	Counts
4) Integrator Output Zero:	499 to 4499	499 to 2499	Counts

NOTES: 1. This time period is fixed. The integration period for the TC820 is:

$$t_{INT\ (TC820)} = \frac{4000}{f_{OSC}} = 2000 \text{ counts}$$

For the TC821, the integration period is:

$$t_{INT\ (TC821)} = \frac{4000}{f_{OSC}} = 1000 \text{ counts}$$

where f_{OSC} is the clock oscillator frequency.

2. Times shown are the RANGE/FREQ at logic low (normal operation). When RANGE/FREQ is logic high, signal integrate times are 200 counts for TC820 and 100 counts for TC821. See "10:1 Range Change" section.

Input Overrange

When the analog input is greater than full scale, the LCD will display "OL" and the "OVERRANGE" LCD annunciator will be on.

Peak Reading Hold

The TC820 provides the capability of holding the highest (or peak) reading. Connecting the PK HOLD input to V_S^+ enables the peak hold feature. At the end of each

conversion the contents of the TC820 counter is compared to the contents of the display register. If the new reading is higher than the reading being displayed, the higher reading is transferred to the display register. A "higher" reading is defined as the reading with the higher absolute value.

The peak reading is held in the display register so the reading will not "droop" or slowly decay with time. The held reading will be retained until a higher reading occurs, the PK HOLD input is disconnected from V_S^+, or power is removed.

The peak signal to be measured must be present during the TC820 signal integrate period. The TC820 does not perform transient peak detection of the analog input signal. However, in many cases, such as measuring temperature or electric motor starting current, the TC820 "acquisition time" will not be a limitation. If true peak detection is required, a simple circuit will suffice. See the applications section for details.

The peak reading function is also available when the TC820 is in the frequency counter mode. The counter auto-ranging feature is disabled when peak reading hold is selected.

10:1 Range Change

The analog input full-scale range can be changed with the RANGE/FREQ input. Normally, RANGE/FREQ is held low by an internal pulldown. Connecting this pin to V_S^+ will increase the full-scale voltage by a factor of 10. No external component changes are required.

The RANGE/FREQ input operates by changing the integrate period. When RANGE/FREQ is connected to V_S^+, the signal integration phase of the conversion is reduced by a factor of 10 (i.e., from 2000 counts to 200 counts).

For the TC821 (3-1/2 digit) ADC, the RANGE/FREQ input can be used to select between 200 mV and 2V full scale. For the TC820, however, the 10:1 range change will result in ±4V full scale. This full-scale range will exceed the common-mode range of the input buffer when operating from a 9V battery. If range changing is required for the TC820, a higher supply voltage can be provided or the input voltage can be divided by 2 externally.

Frequency Counter

In addition to serving as an analog-to-digital converter, the TC820 internal counter can also function as a frequency counter (Figure 4). In the counter mode, pulses at the RANGE/FREQ input will be counted and displayed.

The frequency counter derives its time base from the clock oscillator. The counter time base is:

$$t_{COUNT} = \frac{f_{OSC}}{40{,}000}$$

Thus, the counter will operate with a 1-second time base when a 40 kHz oscillator is used. The frequency counter accuracy is determined by the oscillator accuracy. For accurate frequency measurements, a crystal oscillator is recommended.

The frequency counter will automatically select the proper range. Auto-range operation extends over four decades, from 3.999 kHz to 3.999 MHz (1.999 kHz to 1.999 MHz for TC821). Decimal points are set automatically in the frequency mode (Figure 5).

The logic switching levels of the RANGE/FREQ input are CMOS levels. For best counter operation, an external buffer is recommended. See the applications section for details.

Logic Probe

The TC820 can also function as a simple logic probe (Figure 6). This mode is selected when the LOGIC input is high. Two dual-purpose pins, which normally control the decimal points, are used as logic inputs. Connecting either input to a logic high level will turn on the corresponding LCD annunciator. When the "low" annunciator is on the buzzer will be on. As with the frequency counter input, external level shifters/buffers are recommended for the logic probe inputs.

When the logic probe function is selected while FREQ/$\overline{\text{VOLTS}}$ is low (A/D mode), the ADC will remain in the auto-zero mode. The LCD will read "OL" and all decimal points will be off (Figure 7).

If the logic probe is active while FREQ/$\overline{\text{VOLTS}}$ is high (counter mode), the frequency counter will continue to operate. The display will read "OL" but the decimal points will be visible. If the logic probe input is also connected to the RANGE/FREQ input, bringing the LOGIC input low will immediately display the frequency at the logic probe input.

Analog Pin Functional Description

Differential Signal Inputs (V_{IN}^+), (V_{IN}^-)

The TC820 is designed with true differential inputs, and accepts input signals within the input stage common-mode voltage (V_{CM}) range. The typical range is $V_S^+ - 1V$ to $V_S^- + 1.5V$. Common-mode voltages are removed from the system when the TC820 operates from a battery or floating power source (isolated from measured system) and V_S^- is connected to analog common. (See Figure 8.)

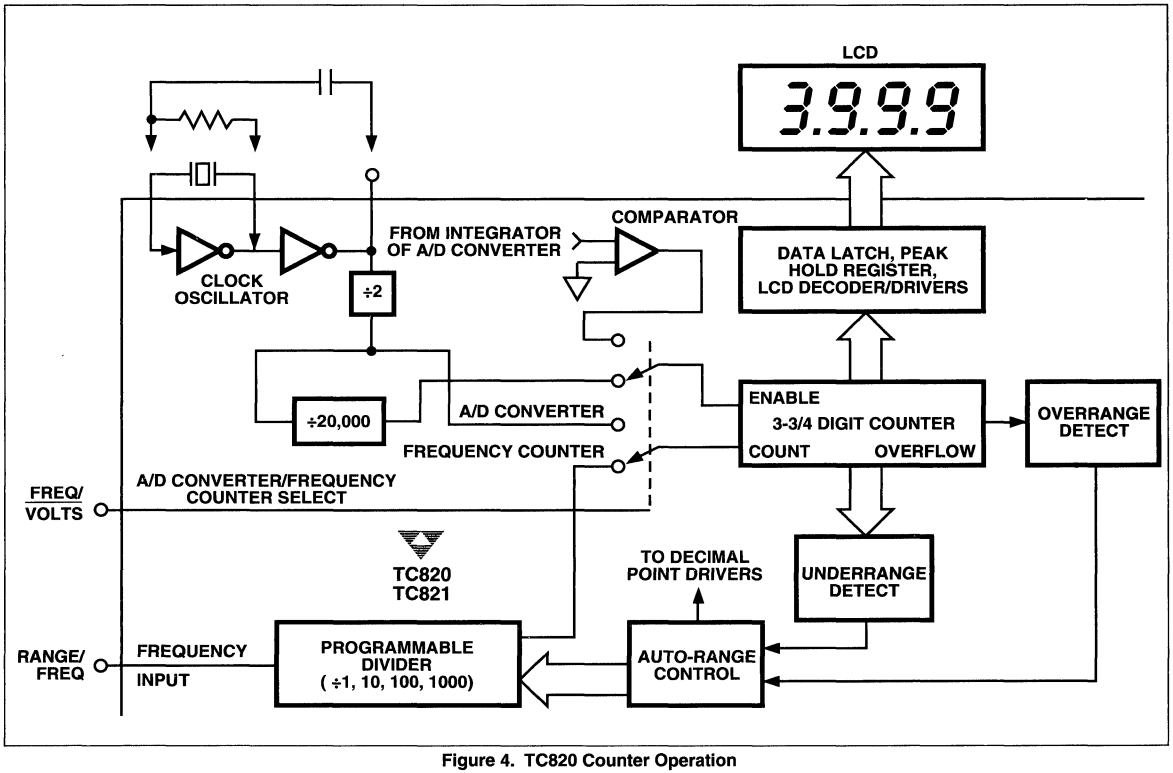
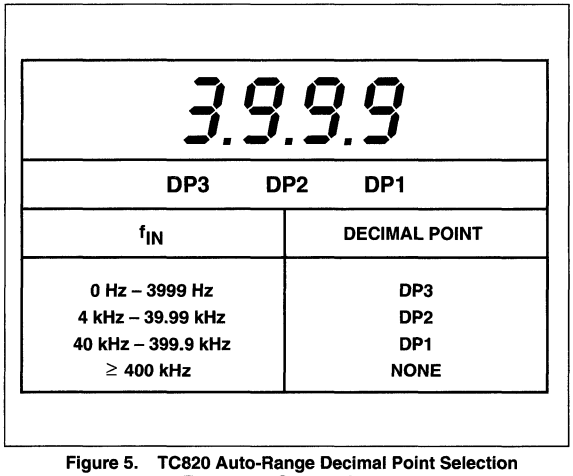


Figure 4. TC820 Counter Operation



f_{IN}	DECIMAL POINT
0 Hz – 3999 Hz	DP3
4 kHz – 39.99 kHz	DP2
40 kHz – 399.9 kHz	DP1
≥ 400 kHz	NONE

Figure 5. TC820 Auto-Range Decimal Point Selection vs Frequency Counter Input

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large, positive V_{CM} exists in conjunction with a full-scale, negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 9). For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

Reference (V_S^+, V_S^-)

The TC820 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors, such as load cells and temperature sensors.

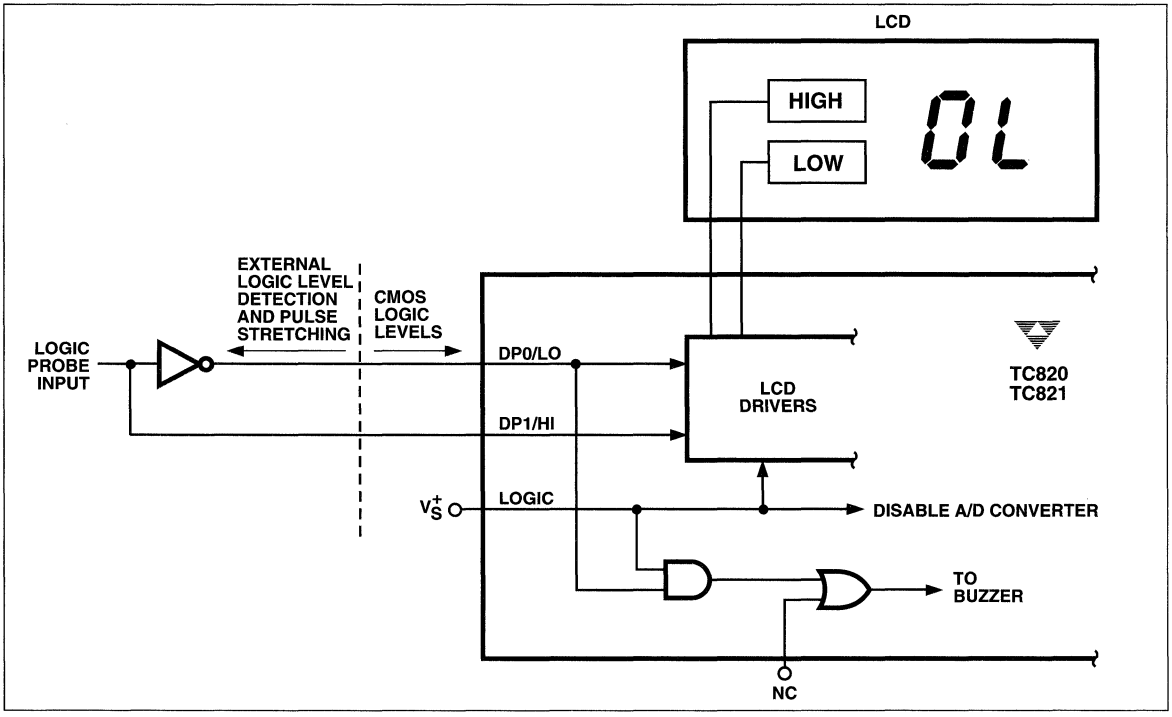


Figure 6. Logic Probe Simplified Schematic

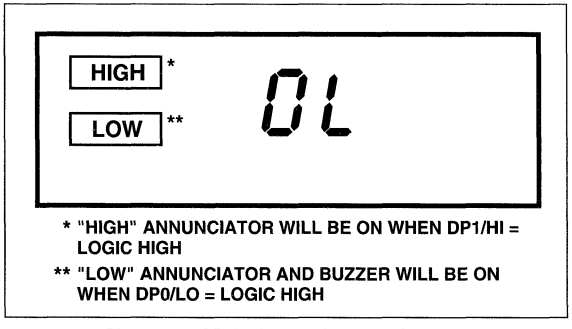


Figure 7. LCD During Logic Probe Operation

To prevent roll-over-type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1 µF capacitor is typical.

The TC820 offers a significantly improved analog common temperature coefficient, providing a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C.

Analog Common

The analog common pin is set at a voltage potential approximately 3.3V below V_S^+. This potential is guaranteed to be between 3.15V and 3.45V below V_S^+. Analog common is tied internally to an N-channel FET capable of sinking 3 mA. This FET will hold the common line at 3.3V below V_S^+ should be an external load attempt to pull the common line toward V_S^+. Analog common source current is limited to 12 µA, and is therefore easily pulled to a more negative voltage (i.e., below $V_S^+ - 3.3V$).

The TC820 connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery-powered applications, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TC820 is specifically designed to operate from a battery or in any measurement

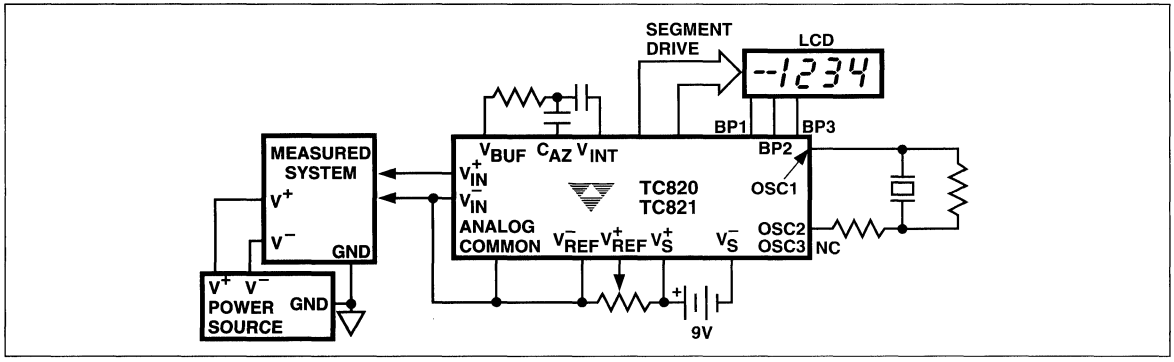


Figure 8. Common-Mode Voltage Removed in Battery Operation With V_{IN}^- = Analog Common

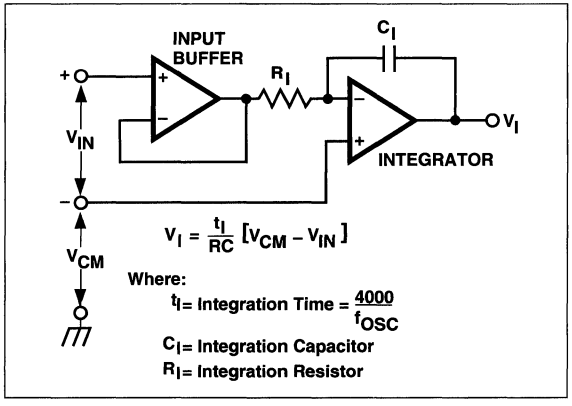


Figure 9. Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

system where input signals are not referenced (float) with respect to the TC820 power source. The analog common potential of V_S^+ –3.3V gives a 7V end-of-battery-life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage ($V_S^+ - V_S^-$ > 7V), analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°C). This potential can be used to generate the TC820 reference voltage. An external voltage reference will be unnecessary in most cases, because of the 35 ppm/°C temperature coefficient. See the applications section for details.

Function Control Input Pin Functional Description

The TC820 operating modes are selected with the function control inputs. The control input truth table is shown in Table I. The high logic threshold is ≥V_S^+–1.5V and the low logic level is ∂ DGND +1.5V.

Table I. TC820 Control Input Truth Table

Logic Input			
FREQ/$\overline{\text{VOLTS}}$	RANGE/FREQ	LOGIC	TC820/821 Function
X	X	1	Logic Probe
0	0	0	A/D Converter, $V_{FULL\ SCALE} = 2 \times V_{REF}$
0	1	0	A/D Converter, $V_{FULL\ SCALE} = 20 \times V_{REF}$
1	Frequency Counter Input	0	Frequency Counter

NOTES: 1. Logic "0" = DGND
2. Logic "1" = V_S^+

FREQ/$\overline{\text{VOLTS}}$

This input determines whether the TC820 is in the analog-to-digital conversion mode or in the frequency counter mode. When FREQ/VOLTS is connected to V_S^+, the TC820 will measure frequency at the RANGE/FREQ input. When unconnected, or connected to DGND, the TC820 will operate as an analog-to-digital converter. This input has an internal 5 µA pull-down to DGND.

LOGIC

The LOGIC input is used to activate the logic probe function. When connected to V_S^+, the TC820 will enter the logic probe mode. The LCD will show "OL" and all decimal points will be off. The decimal point inputs directly control "high" and "low" display annunciators. When LOGIC is unconnected, or connected to DGND, the TC820 will perform analog-to-digital or frequency measurements as selected by the FREQ/$\overline{\text{VOLTS}}$ input. The LOGIC input has an internal 5 µA pull-down to DGND.

RANGE/FREQ

The function of this dual-purpose pin is determined by the FREQ/$\overline{\text{VOLTS}}$ input. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_S^+, RANGE/FREQ is the input for the frequency counter function. Pulses at this input are counted with a time base equal to f_{OSC}/40,000. Since this input has CMOS input levels (V_S^+ –1.5V and DGND +1.5V), an external buffer is recommended.

When the TC820 analog-to-digital converter function is selected, connecting RANGE/FREQ to V_S^+ will divide the integration time by 10. Therefore, the RANGE/FREQ input can be used to perform a 10:1 range change without changing external components.

DP0/LO, DP1/HI

The function of these dual-purpose pins is determined by the LOGIC input. When the TC820 is in the analog-to-digital converter mode, these inputs control the LCD decimal points. The decimal point truth table is shown in Table II. These inputs have internal 5 µA pull-downs to DGND when the voltage/frequency measurement mode is active.

Table II. TC820 Decimal Point Truth Table

Decimal Point Inputs		
DP1	DP0	LCD
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

Connecting the LOGIC input to V_S^+ places the TC820 in the logic probe mode. In this mode, the DP0/LO and DP1/HI inputs control the LCD "low" and "high" annunciators directly. When DP1/HI is connected to V_S^+, the "high" annunciator will turn on. When DP0/LO is connected to V_S^+, the "low" annunciator and the buzzer will turn on. The internal pull-downs on these pins are disabled when the logic probe function is selected.

These inputs have CMOS logic switching thresholds. For optimum performance as a logic probe, external level shifters are recommended. See the applications section for details.

BUZ IN

This input controls the TC820 on-chip buzzer driver. Connecting BUZ IN to V_S^+ will turn the buzzer on. There is an external pull-down to DGND. BUZ IN can be used with external circuitry to provide additional functions, such as a fast, audible continuity indication.

Additional Features

The TC820 and TC821 are available in 40-pin and 44-pin packages. Several additional features are available in the 44-pin package.

$\overline{\text{EOC}}$/HOLD

$\overline{\text{EOC}}$/HOLD is a dual-purpose, bidirectional pin. As an output, this pin goes low for 10 clock cycles at the end of each conversion. This pulse latches the conversion data into the display driver section of the TC820.

$\overline{\text{EOC}}$/HOLD can be used to hold (or "freeze") the display. Connecting this pin to V_S^+ inhibits the display update process. Conversions will continue, but the display will not change. $\overline{\text{EOC}}$/HOLD will hold the display reading for either analog-to-digital or frequency measurements.

The input/output structure of the $\overline{\text{EOC}}$/HOLD pin is shown in Figure 10. The output drive current is only a few microamps, so $\overline{\text{EOC}}$/HOLD can easily be overdriven by an open-collector logic gate, as well as a FET, bipolar transistor, or mechanical switch. When used as an output, $\overline{\text{EOC}}$/HOLD will have a slow rise and fall time due to the limited output current drive. A CMOS Schmitt trigger buffer is recommended.

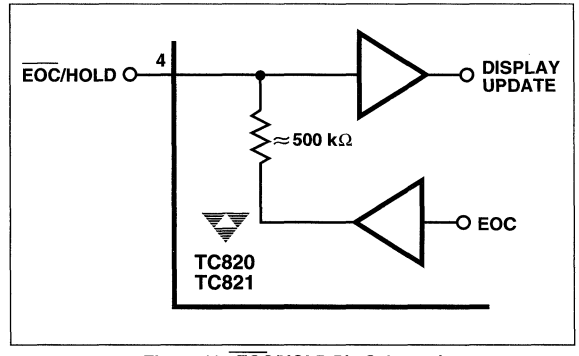


Figure 10. $\overline{\text{EOC}}$/HOLD Pin Schematic

Overrange (OR), Underrange (UR)

The OR output will be high when the analog input signal is greater than full scale (3999 counts for TC820 and 1999 counts for TC821). The UR output will be high when the display reading is 380 counts or less (∂ 180 counts for TC821).

The OR and UR outputs can be used to provide an autoranging meter function. By logically ANDing these outputs with the inverted $\overline{\text{EOC}}$/HOLD output, a single pulse will be generated each time an underranged or overranged conversion occurs (Figure 11).

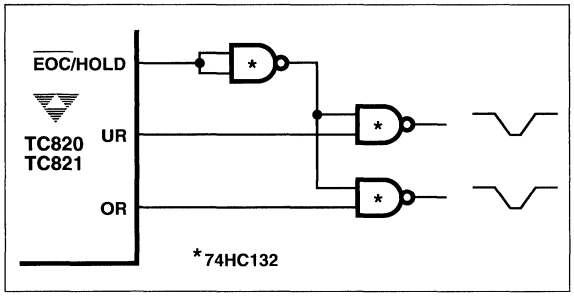


Figure 11. Generating Underrange and Overrange Pulses

V_{DISP}

The V_{DISP} input sets the peak-to-peak LCD drive voltage. In the 40-pin package, V_{DISP} is connected internally to DGND, providing a typical LCD drive voltage of 5 V_{P-P}. The 44-pin package includes a separate V_{DISP} input for applications requiring a variable or temperature-compensated LCD drive voltage. See the applications information for suggested circuits.

APPLICATIONS INFORMATION

Power Supplies

The TC820 is designed to operate from a single power supply such as a 9V battery (Figure 12). The converter will operate over a range of 7V to 15V. For battery operation, analog common (COM) provides a common-mode bias voltage (see analog common discussion in the theory of operation section). However, measurements cannot be referenced to battery ground. To do so will exceed the negative common-mode voltage limit.

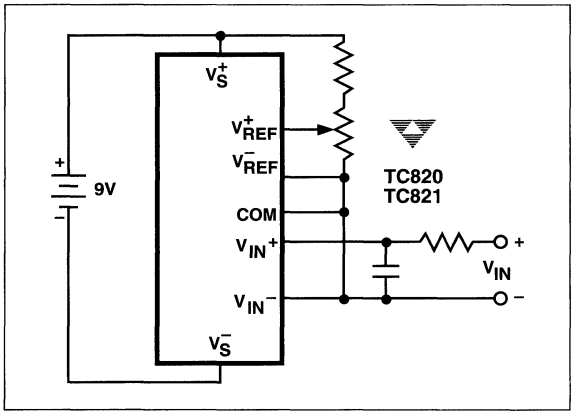


Figure 12. Powering the TC820/821 From a Single 9V Battery

A battery with voltage between 3.5V and 7V can be used to power the TC820, when used with a voltage doubler, as shown in Figure 13. The voltage doubler uses the TC7660 and two external capacitors. With this configuration measurements can be referenced either to Analog Common or to battery ground.

Digital Ground (DGND)

Digital ground is generated from an internal zener diode (Figure 14). The voltage between V_S^+ and DGND is the internal supply voltage for the digital section of the TC820. DGND will sink a minimum of 3 mA.

DGND establishes the low logic level reference for the TC820 mode select inputs, and for the frequency and logic probe inputs. The DGND pin can be used as the negative supply for external logic gates, such as the logic probe buffers. To ensure correct counter operation at high frequency, connect a 1 µF capacitor from DGND to V_S^+.

DGND also provides the drive voltage for the LCD. The TC820 40-pin package internally connects the LCD V_{DISP} pin to DGND, and provides an LCD drive voltage of about 5 V_{P-P}. In the 44-pin package, connecting the V_{DISP} pin to DGND will provide a 5V LCD drive voltage.

Digital Input Logic Levels

Logic levels for the TC820 digital inputs are referenced to V_S^+ and DGND. The high-level threshold is V_S^+ –1.5V and the low logic level is DGND +1.5V. In most cases,

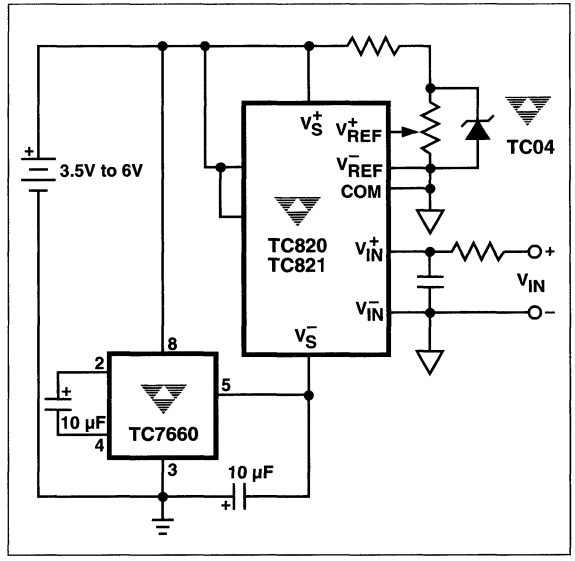


Figure 13. Powering the TC820/821 From a Low-Voltage Battery

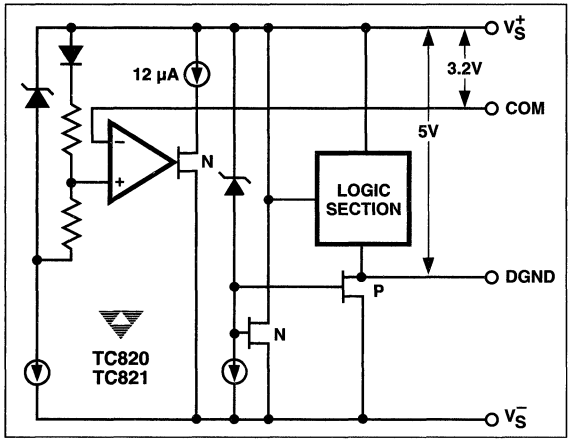


Figure 14. DGND and COM Outputs

digital inputs will be connected directly to V_S^+ with a mechanical switch. CMOS gates can also be used to control the logic inputs, as shown in the logic probe inputs section.

Clock Oscillator

The TC820 oscillator can be controlled with either a crystal or with an inexpensive resistor-capacitor combination. The crystal circuit, shown in Figure 15, is recommended when high accuracy is required in the frequency counter mode. The 40 kHz crystal is a standard frequency for ultrasonic alarms, and will provide a 1-second time base for the counter or 2.5 analog-to-digital conversions per second. Consult the crystal manufacturer for detailed applications information.

Where low cost is important, the R-C circuit of Figure 16 can be used. The frequency of this circuit will be approximately:

$$f_{OSC} = \frac{0.3}{RC}$$

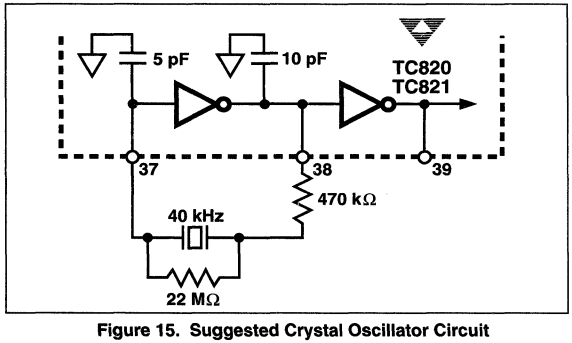


Figure 15. Suggested Crystal Oscillator Circuit

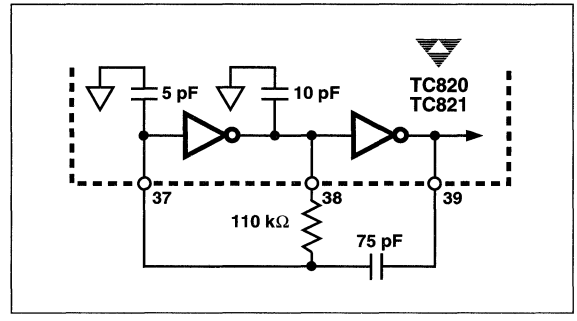


Figure 16. R-C Oscillator Circuit

Typical values are R = 10 kΩ and C = 68 pF. The resistor value should be ≥100 kΩ. For accurate frequency measurement, an R-C oscillator frequency of 40 kHz is required.

System Timing

All system timing is derived from the clock oscillator. The clock oscillator is divided by 2 (4 for TC821) prior to clocking the A/D counters. The clock is also divided by 8 to drive the buzzer, by 240 to generate the LCD backplane frequency, and by 40,000 for the frequency counter time base. A simplified diagram of the system clock is shown in Figure 17.

Component Value Selection

Auto Zero Capacitor — C_{AZ}

The value of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A 0.47 µF capacitor is recommended; a low dielectric absorption capacitor (Mylar) is required.

Reference Voltage Capacitor — C_{REF}

The reference voltage capacitor used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is typical. A good quality, low leakage capacitor (such as Mylar) should be used.

Integrating Capacitor — C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case, a ±2V integrator output swing is optimum when the analog input is near full scale. For 2.5 readings/second (f_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.22 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing. An exact

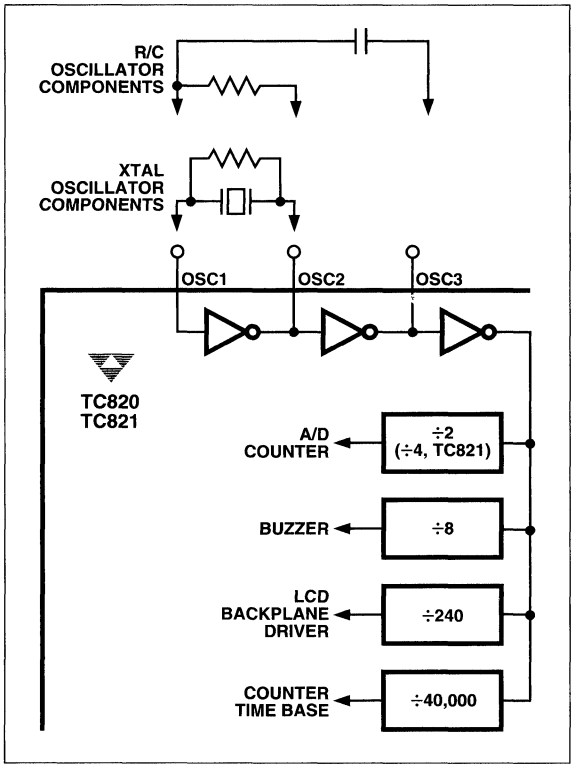


Figure 17. System Clock Generation

expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where: f_{OSC} = Clock frequency
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor — R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 40 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 400 mV full scale, R_{INT} should be about 100 kΩ.

Reference Voltage Selection

A full-scale reading (4000 counts for TC820 and 2000 counts for TC821) requires the input signal be twice the reference voltage.

Table III. Reference Voltage Selection

Full-Scale Input Voltage (V_{FS}) (Note 1)	TC820		TC821	
	V_{REF}	Resolution	V_{REF}	Resolution
200 mV	Note 2		100 mV	100 µV
400 mV	200 mV	100 µV	200 mV	200 µV
1V	500 mV	250 µV	500 mV	500 µV
2V (Notes 3, 4)	1V	500 µV	1V	1 mV

NOTES:
1. TC820/821 in A/D converter mode, RANGE/FREQ = logic low.
2. Not recommended.
3. V_{FS} > 2V may exceed the input common mode range. See "10:1 Range Change" section.
4. Full-scale voltage values are not limited to the values shown. For example, TC820 V_{FS} can be any value from 400 mV to 2V.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 800 mV for 4000 lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 400 mV. This permits the transducer input to be used directly.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference voltage. This potential is stable whenever the supply potential is greater than approximately 7V. The low-battery detection circuit and analog common operate from the same internal reference. This ensures that the low-battery annunciator will turn on at the time the internal reference begins to lose regulation.

The TC820 can also operate with an external reference. Figure 18 shows internal and external reference applications.

Ratiometric Resistance Measurements

The TC820 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 19). The voltage developed across the unknown is applied to the input and voltages across the known resistor

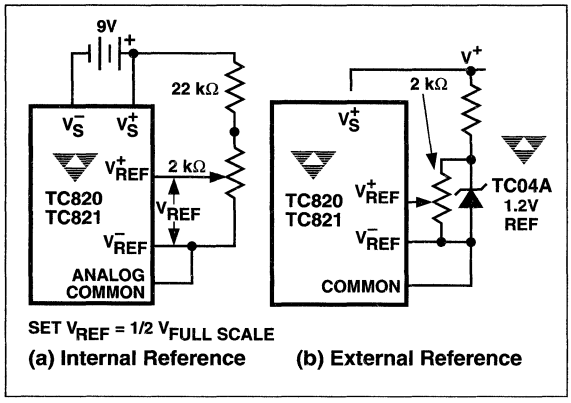


Figure 18. Reference Voltage Connections

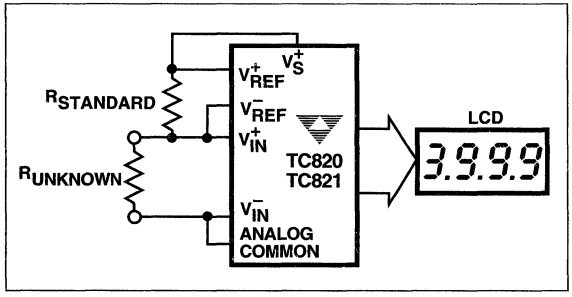


Figure 19. Low Parts Count Ratiometric Resistance Measurement

applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000 (1000 for TC821). The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 2000$$

The display will overrange for values of $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

Buffering the FREQ Input

When the FREQ/$\overline{\text{VOLTS}}$ input is high and the LOGIC input is low, the TC820 will count pulses at the RANGE/FREQ input. The time base will be $f_{OSC}/40{,}000$, or 1 second with a 40 kHz clock. The signal to be measured should swing from V_S^+ to DGND. The RANGE/FREQ input has CMOS input levels without hysteresis. For best results, especially with low-frequency sine-wave inputs, an external buffer with hysteresis should be added. A typical circuit is shown in Figure 20.

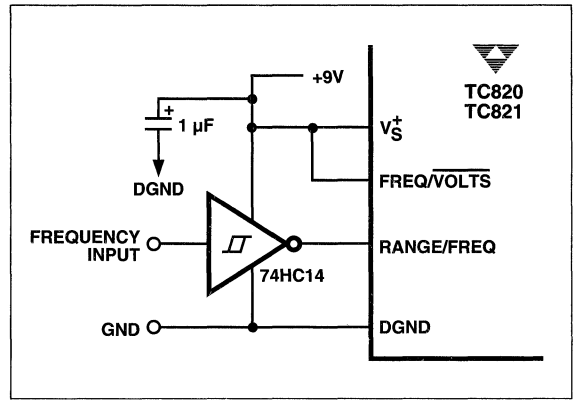


Figure 20. Frequency Counter External Buffer

Logic Probe Inputs

The DP0/LO and DP1/HI inputs provide the logic probe inputs when the LOGIC input is high. Driving either DP0/LO or DP1/HI to a logic high will turn on the appropriate LCD annunciator. When DP0/LO is high, the buzzer will be on.

To provide a "single input" logic probe function, external buffers should be used. A simple circuit is shown in Figure 21. This circuit will turn the appropriate annunicator on for high and low level inputs.

If carefully controlled logic thresholds are required, a window comparator can be used. Figure 22 shows a typical circuit. This circuit will turn on the high or low annunciators when the logic thresholds are exceeded, but the resistors connected from DP0/LO and DP1/HI to DGND will turn both annunciators off when the logic probe is unconnected.

The TC820 logic inputs are not latched internally, so pulses of short duration will usually be difficult or impossible

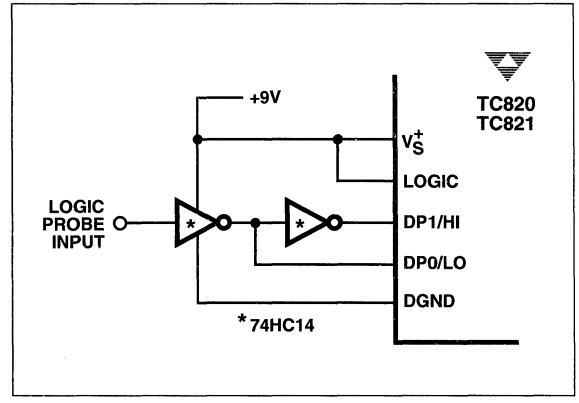
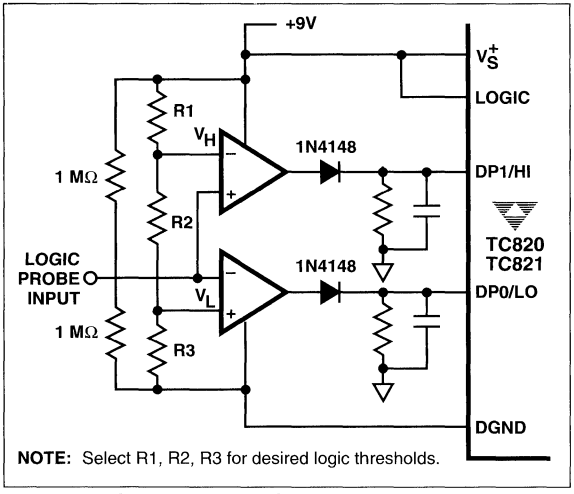


Figure 21. Simple External Logic Probe Buffer



NOTE: Select R1, R2, R3 for desired logic thresholds.

Figure 22. Window Comparator Logic Probe

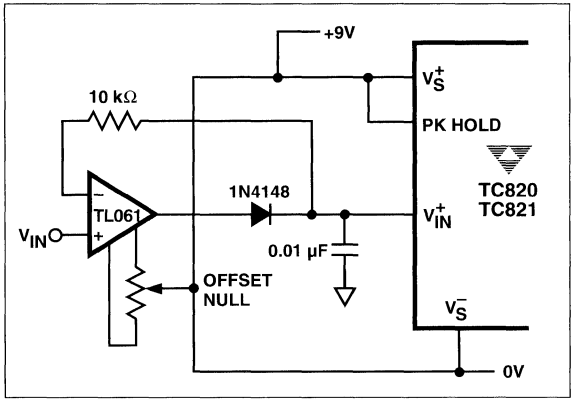


Figure 23. External Peak Detector

to see. To display short pulses properly, the input pulse should be "stretched." The circuit of Figure 22 shows capacitors added across the input pull-down resistors to stretch the input pulse and permit viewing short-duration input pulses.

External Peak Detection

The TC820 will hold the highest A/D conversion or frequency reading indefinitely when the PK HOLD input is connected to V_S^+. However, the analog peak input must be present during the A/D converter's signal integrate period. For slowly changing signals, such as temperature, the peak reading will be properly converted and held.

If rapidly changing analog signals must be held, an external peak detector should be added. An inexpensive circuit can be made from an op-amp and a few discrete components, as shown in Figure 23. The droop rate of the external peak detector should be adjusted so that the held voltage will not decay below the desired accuracy level during the converter's 400 ms conversion time.

Liquid Crystal Display (LCD)

The TC820 drives a triplex (multiplexed 3:1) LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for overrange, peak hold, high and low logic levels, and low battery. Table IV shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 240.

Backplane waveforms are shown in Figure 24. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

Other display output lines have waveforms that vary depending on the displays values. Figure 25 shows a set of waveforms for the a, g, d outputs of one digit for several combinations of "on" segments.

Table IV. LCD Backplane and Segment Assignments

40-Pin DIP Pin No.	44-Pin Flat Pkg Pin No.	LCD Display Pin No.	BP1	BP2	BP3
1	40	3	LOW	"—"	E4
2	41	4	A4	G4	D4
3	42	5	B4	C4	DP3
4	43	6	HIGH	F3	E3
5	44	7	A3	G3	D3
6	1	8	B3	C3	DP2
7	2	9	OVER	F2	E2
8	3	10	A2	G2	D2
9	4	11	B2	C2	DP1
10	5	12	PEAK	F1	E1
11	6	13	A1	G1	D1
12	7	14	B1	C1	BATT
13	8	2,16*	—	—	BP3
14	9	1	—	BP2	—
15	10	15	BP1	—	—

*Connect both pins 2 and 16 of LCD to TC820 BP3 output.

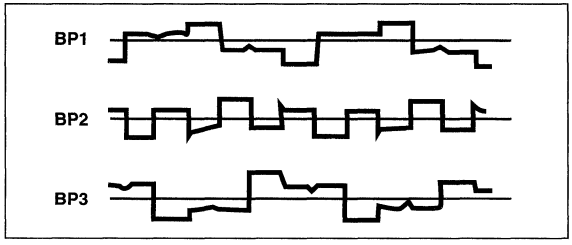


Figure 24. Backplane Waveforms

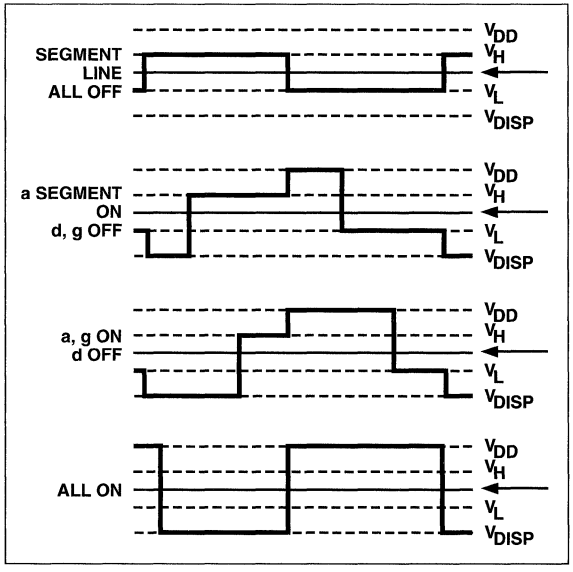


Figure 25. Typical Display Output Waveforms

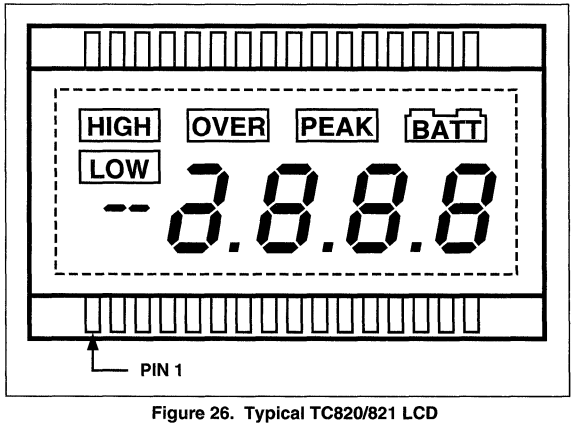


Figure 26. Typical TC820/821 LCD

LCD Source

Although most users will design their own custom LCD, a standard display for the TC820 (Figure 26), Part No. ST-1355-M1, is available from:

Crystaloid (USA)
Crystaloid Electronics
P.O. Box 628
5282 Hudson Dr.
Hudson, OH 44238
Phone: (216) 655-2429
Fax: (216) 655-2176

Crystaloid (Europe)
Rep France
102, rue des Nouvelles
F92150 Suresnes
France
Phone: 33-1-42 04 29 25
Fax: 33-1-45 06 46 99

This display can also be used with the TC821.

Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 167 Hz when f_{OSC} = 40 kHz). The peak-to-peak amplitude is equal to ($V_S^+ - V_{DISP}$). Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

LCD Drive Voltage (V_{DISP})

The peak-to-peak LCD drive voltage is equal to ($V_S^+ - V_{DISP}$). In the 40-pin dual-in-line package (DIP), V_{DISP} is internally connected to DGND, providing a typical LCD drive voltage of 5 V_{P-P}.

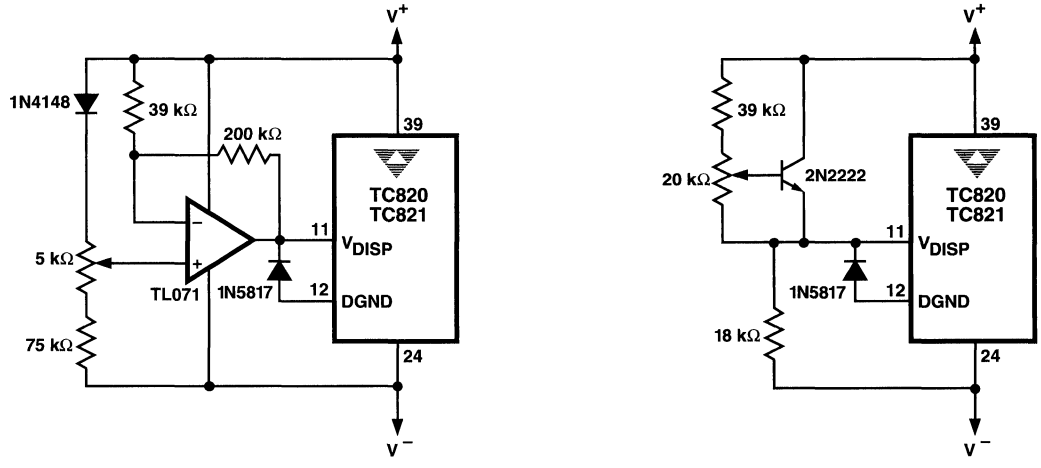
For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. In this case, the TC820 44-pin package provides a pin connection for V_{DISP}. Figure 27 shows TC820 circuits that can be adjusted to give a temperature compensation of about 10 mV/°C between V_S^+ and V_{DISP}. The diode between GND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed 0.3V below GND.

Crystal Source

Two sources of the 40 kHz crystal are:

Statek Corp
512 N. Main St
Orange, CA 92668
Phone: (714) 639-7810
Fax: (714) 997-1256
Part #: CX-1V-40.0

SPK Electronics
2F-1, No. 312, Sec 4,
Jen Ai Rd
Taipei, Taiwan R.O.C.
Phone: (02) 754-2677
Fax: 886-2-708-4124
Part#: QRT-38-40.0 kHz



NOTE: Pin numbers shown are for 44-pin flat package.

Figure 27. Temperature-Compensating Circuits

3-3/4 DIGIT LCD ANALOG TO DIGITAL CONVERTER

FEATURES

- 3-3/4 Digit (3999 maximum) Resolution
- 3V Battery Operation
  - — On-Chip DC-to-DC Converter
- Low Power Operation
  - — Supply Current 400 μA Typical
- Differential Signal Inputs
- Differential Reference Inputs
- LCD with Triplexed drive
  - — 3 Decimal Points
  - — LCD Annunciator Driver Output
  - — Low-battery and Hold Annunciators
- Op-amp for AC-to-DC Converter
- Display HOLD with LCD Annunciator
- Low-battery Detect with LCD Annunciator
- On-chip Band-gap Reference
- Crystal Oscillator

ORDERING INFORMATION

Part No.	44-Pin PFP	44-Pin PLCC	40-Pin PDIP	Temperature Range
TC822CKW	X			0°C to +70°C
TC822CLW		X		0°C to +70°C
TC822CPL			X	0°C to +70°C

GENERAL DESCRIPTION

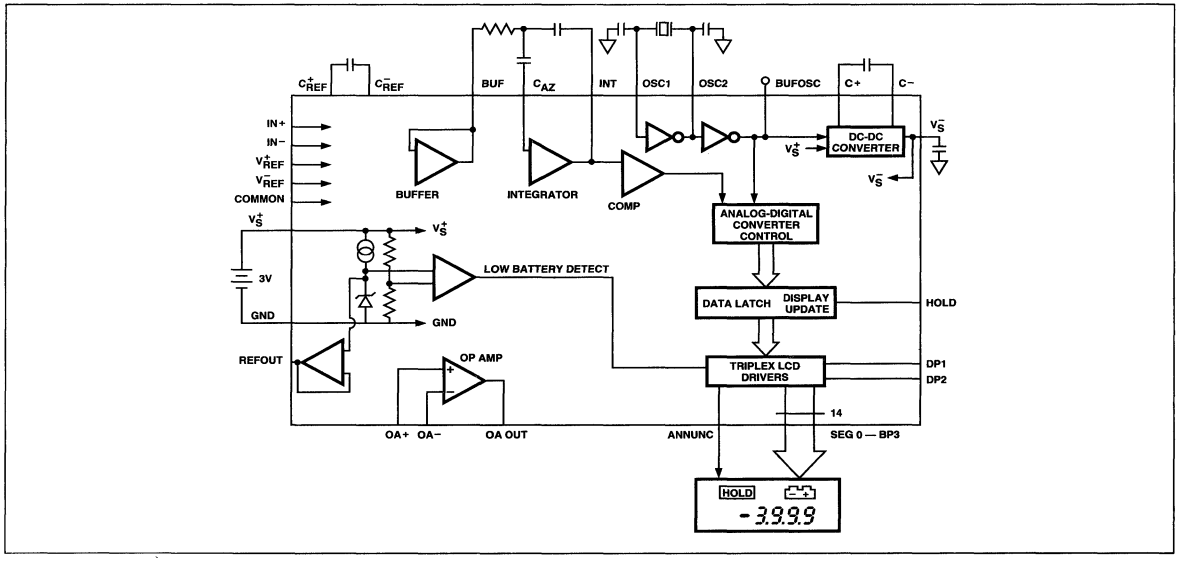
The TC822 is a 3-3/4 digit LCD analog-to-digital converter which operates from a single 3V battery. All active components necessary to construct a 0.025% resolution measurement system are included on the TC822. Only external resistors and capacitors, an LCD and a 3V battery are required.

The TC822 includes features which must be added externally with ADCs such as the 7106. LCD decimal point drivers, low-battery detection, and data hold function with LCD annunciator are all on chip. No external exclusive-OR gates are required. An operational amplifier, which can be used for an AC-to-DC converter or resistance measurement current source, is also included.

Differential signal inputs with 1 pA leakage simplify system design. Differential reference inputs permit ratiometric measurements, while retaining the data HOLD function. Either the internal 1.3V band-gap reference or an external reference can be used.

The TC822 LCD drive includes 3-3/4 digits, decimal points, and HOLD and low-battery annunciators. The triplexed LCD requires only 14 interconnects, which increases reliability and simplifies mechanical design.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S^+ to GND) ..... +4.7V
Analog Input Voltage (either input) ..... V_S^+ to V_S^- (Note 1)
Reference Input Voltage (either input) ..... V_S^+ to V_S^-
Op Amp Input Voltage (either input) ..... V_S^+ to V_S^-
Digital Inputs ..... V_S^+ to GND
Power Dissipation, Plastic Package ..... 800 mW
Operating Temperature Range
C Devices ..... 0°C to +70°C
E Devices ..... - 40°C to +85°C
Storage Temperature Range ..... - 65°C to +150°C
Lead Soldering Temperature (10 sec) ..... +300°C

NOTES:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.
4. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

ELECTRICAL CHARACTERISTICS: V_S = 3.0 V, T_A = 25° C, Figure 1 Test Circuit

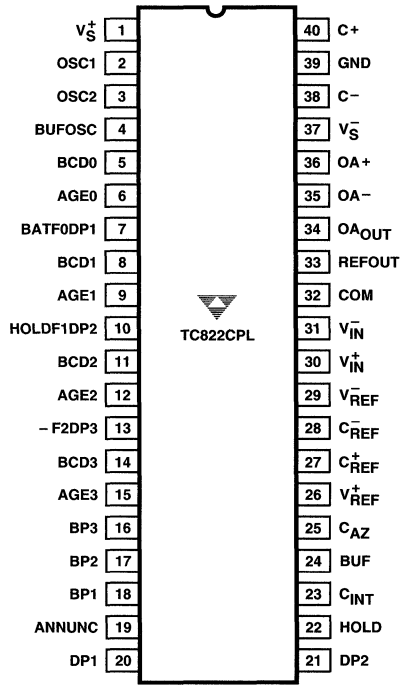
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
	Zero Input Reading	V_{IN} = 0.0V Full-Scale = 400 mV	– 0000	0000	+0000	Digital Reading
RE	Roll-Over Error	V_{IN} = ±390 mV Full-Scale = 400 mV	– 1	±0.2	+1	Counts
NL	Non-Linearity (Max Deviation from Best Straight Line Fit)	Full-Scale = 400 mV	– 1	±0.2	+1	Count
	Ratiometric Reading	$V_{IN} = V_{REF}$	1999	1999/ 2000	2000	Digital Reading
E_N	Noise (p-p value not exceeded 95% of time)	V_{IN} = 0.0V Full-Scale = 400 mV	—	15	—	µV
I_{IN}	Input Leakage Current	V_{IN}= 0.0 V T_A = 25°C 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	 — — —	 — 20 100	 10 100 250	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±0.2V, V_{IN} = 0.0 V Full-Scale= 400 mV	—	50	—	µV/V
V_{CMR}	Common-Mode Voltage Range	Input High, Input Low V_{IN} = 0.0V, Full-Scale = 400 mV	GND – 0.5	—	GND +0.5	V
TC_{ZS}	Zero Reading Drift	V_{IN} = 0.0V 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C Ext. Ref. 0 ppm/°C	 — —	 0.2 1	 — —	µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 399 mV 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C Ext. Ref. 0 ppm/°C	 — —	 ±1 ±5	 ±5 ±25	ppm/°C
	Input Voltage Range	V_{IN}^+, V_{IN}^- Normal Mode + Common-Mode Voltage	GND –0.5	—	GND +0.5	V

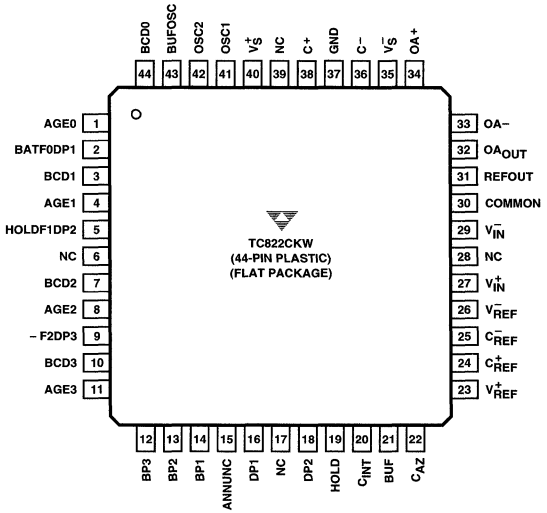
ELECTRICAL CHARACTERISTICS (Cont.): V_S = 3.0 V, T_A = 25° C, Figure 1 Test Circuit

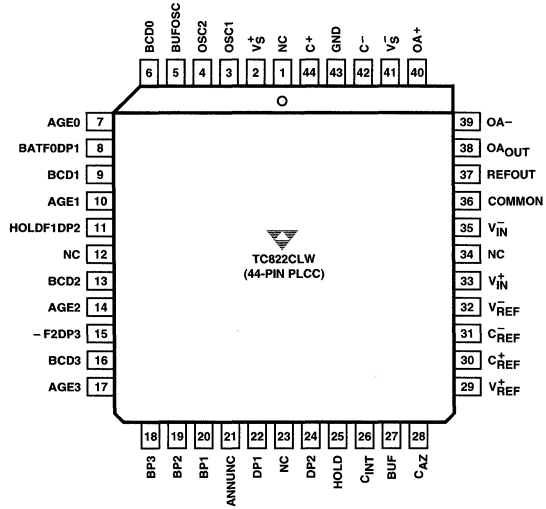
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Reference						
V_{REF}	Reference Voltage	I_L = 25 µA (V_{REF} - GND)	1.25	1.3	1.45	V
TCV_{REF}	Reference Voltage Temperature Coefficient	0°C ≤ T_A ≤ +70°C	—	50	—	ppm/°C
Op-Amp						
V_{IOA}	Op-Amp Input Offset Voltage	V_S = 3V	—	±10	—	mV
	Op-Amp Input Voltage Range		—	±2	—	V
	Op-Amp Unity Gain Frequency		—	0.6	—	MHz
	Op-Amp Output Voltage Swing	R_L = 100 kΩ to GND	—	±2.5	—	V
	Op-Amp Slew Rate	R_L = 100 kΩ to GND, CL = 50 pF	—	1	—	V/µs
Digital						
V_{IL}	Input Low Voltage	DP1, DP2, HOLD	—	—	GND +0.5	V
V_{IH}	Input High Voltage	DP1, DP2, HOLD	V_S^+ – 0.5	—	—	V
	Control Pin Pulldown Current	V_{IN} = V_S^+	—	3	—	µA
	LCD Drive Voltage	2V ≤ V_S^+ ≤ 4V	3.1	3.2	3.3	V p-p
Power Supply						
I_S	Supply Current	V_{IN} = 0.0V V_S^+ =3.0 V	—	400	600	µA
	Supply Operating Voltage Range	V_S^+ to GND	2	—	4	V
	Low-Battery Flag Voltage	V_S^+ to GND	2.15	2.25	2.45	V

TC822

PIN CONFIGURATIONS







PRELIMINARY PIN DESCRIPTION AND FUNCTION, TC822 3-3/4 DIGIT A-D CONVERTER, 3V OPERATION

Pin No. (40-Pin Package)	Symbol	Description
1	V_S^+	Positive battery supply connection. Typically 3V.
2	OSC1	Oscillator connection.
3	OSC2	Oscillator connection.
4	BUFOSC	Buffered oscillator output.
5	BCD0	LCD segment drive for 'b', 'c', and 'd' segments of least significant digit (LSD).
6	AGE0	LCD segment drive for 'a', 'g', and 'e' segments of LSD.
7	BATF0DP1	LCD segment drive for LOW-BATTERY, 'f' segment of LSD, and decimal point 1.
8	BCD1	LCD segment drive for 'b', 'c', and 'd' segments of 2nd LSD.
9	AGE1	LCD segment drive for 'a', 'g', and 'e' segments of 2nd LSD.
10	HOLDF1DP2	LCD segment drive for 'data hold', 'f' segment of 2nd LSD, and decimal point 2.
11	BCD2	LCD segment drive for 'b', 'c', and 'd' segments of 3rd LSD.
12	AGE2	LCD segment drive for 'a', 'g', and 'e' segments of 3rd LSD.
13	–F2DP3	LCD segment drive for 'polarity', 'f' segment of 3rd LSD, and decimal point 3.
14	BCD3	LCD segment drive for 'b', 'c', and 'd' segments of most significant digit (MSD).
15	AGE3	LCD segment drive for 'a', 'g', and 'e' segments of MSD.
16	BP3	LCD backplane #3.
17	BP2	LCD backplane #2.
18	BP1	LCD backplane #1.
19	ANNUNC	Square wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.
20	DP1	Decimal Point select input.
21	DP2	Decimal Point select input.
22	HOLD	Hold input. Connecting this pin to V_S^+ will 'freeze' the LCD.
23	C_{INT}	Integrator output. Connect to integration capacitor.
24	BUF	Buffer output. Connect to integration resistor.
25	C_{AZ}	Autozero capacitor connection.
26	V_{REF}^+	High differential reference input connection.
27	C_{REF}^+	Positive connection for reference capacitor.
28	C_{REF}^-	Negative connection for reference capacitor.
29	V_{REF}^-	Low differential reference input connection.
30	V_{IN}^+	High analog input signal connection.
31	V_{IN}^-	Low analog input signal connection.
32	COM	Analog circuit ground reference point.
33	REFOUT	Output of 1.3V voltage reference.
34	OA_{OUT}	Output of uncommitted operational amplifier.
35	OA-	Inverting input of uncommitted operational amplifier.
36	OA+	Noninverting input of uncommitted operational amplifier.
37	V_S^-	Output of DC-to-DC converter. Connect a 1 µF capacitor from this pin to power ground.
38	C–	Capacitor connection for DC-to-DC converter.
39	GND	Power ground.
40	C+	Capacitor connection for DC-to-DC converter.

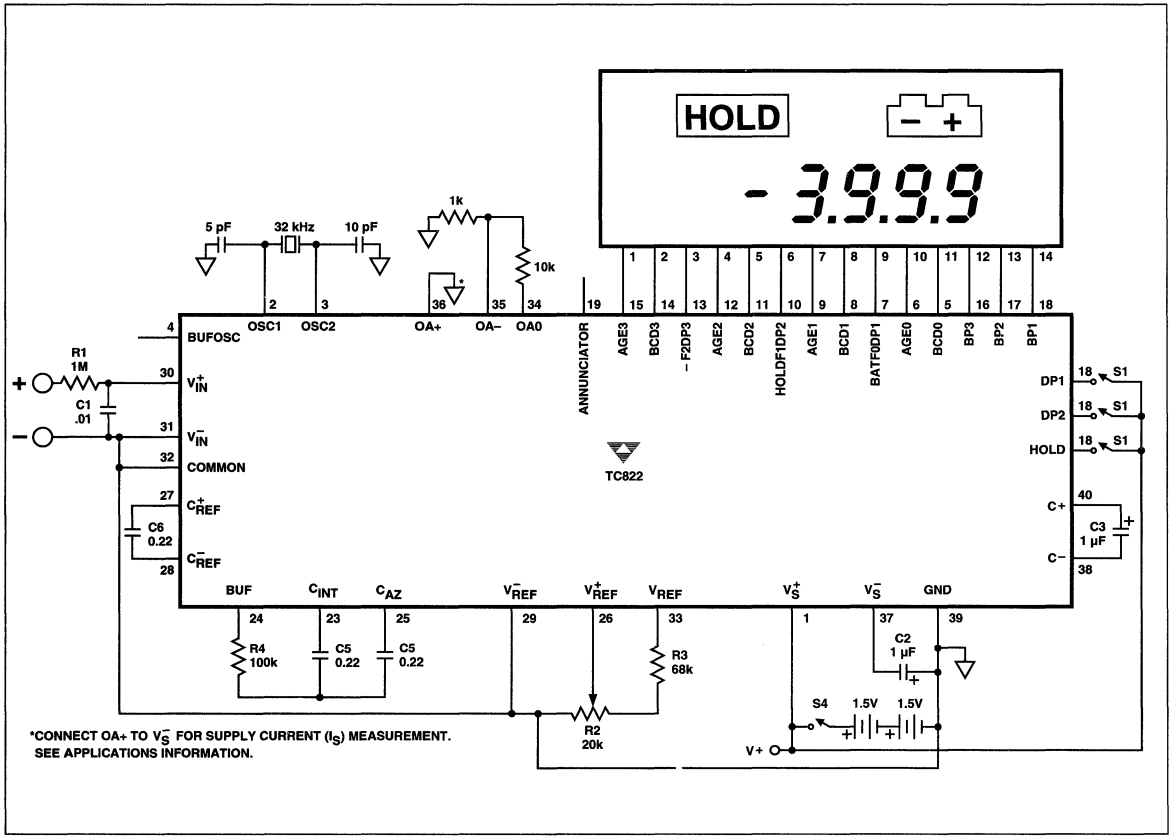


Figure 1 Test Circuit

FEATURES

The TC822 is a high-resolution analog-to-digital converter which include all of the active components required to build a typical digital multimeter or other measurement instrument. The on-chip op-amp can be configured as a sensor amplifier, AC-to-DC converter, or resistance measurement current source. The LCD includes decimal points, low-battery detection, and data hold annunciators. A DC-to-DC converter permits operation from a single 3V battery. With on-chip voltage reference and LCD drive circuitry, the TC822 simplifies the design of multi-mode measurement instruments.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC822 ADC operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC822 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (t_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

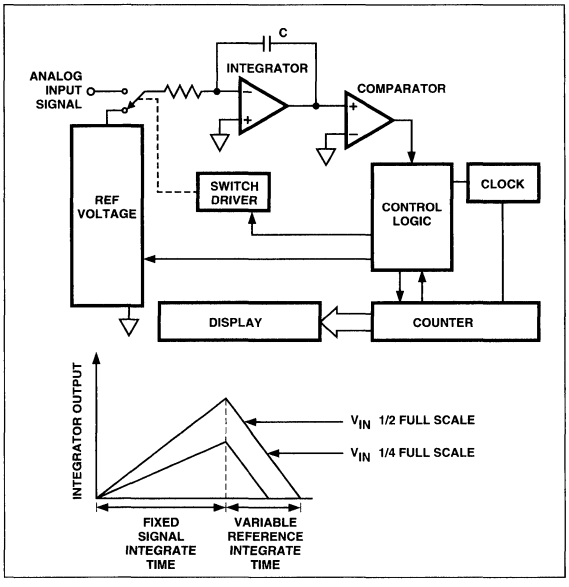


Figure 2 Basic Dual-Slope Converter

In a simple dual-slope converter, a complete conversion requires the integrator output to 'ramp-up' from zero and 'ramp-down' back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}(t)dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where: V_{REF} = Reference Voltage
t_{INT} = Integration Time
t_{DEINT} = Deintegration Time

For a constant T_{INT}:

$$V_{IN} = V_{REF} \bullet \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (see Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

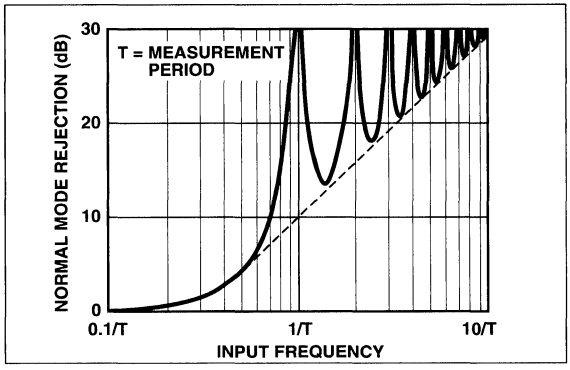


Figure 3 Normal-Mode Rejection of Dual-Slope Converter

TC822 ADC THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC822 design incorporates a 'Zero Integrator Output' phase and an 'Auto Zero' phase. These additional phases ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

1) Zero Integrator Output Phase
2) Auto Zero Phase
3) Signal Integrate Phase
4) Reference Deintegrate Phase

Zero Integrator Output Phase

This phase guarantees that the integrator output is at zero volts after an overrange input occurs. Thus, the next reading after an overranged reading will be correct. The ZI phase duration varies from 0 to 600 counts.

Auto Zero Phase

During the Auto Zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0 volt ref) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero phase residual is typically 10 to 15 μV. The Auto Zero duration is 1600 counts, plus the ZI counts if an overrange did not occur, plus

unused deintegration counts. Thus, the AZ phase can occupy from 1600 to 6000 counts.

Signal Integration Phase

Upon completion of the Auto Zero phase, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period, which in the TC822 is 2000 counts (4000 clock periods). The externally set clock frequency is divided by two before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

Polarity is determined at the end of signal integration phase. The sign bit is a 'true polarity' indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the Auto Zero phase, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (t_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase:

$$T_{DEINT} = \frac{R_{INT} * C_{INT} * V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC822 is:

$$\text{Digital Count} = 2000 * \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

ADC System Timing

The oscillator frequency is divided by 2 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 8000 counts or 16000 clock pulses. The 8000 count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

Conversion Phase	TC822	
1) Auto Zero	1600 to 5999	Counts
2) Signal Integrate*	2000	Counts
3) Reference Integrate	1 to 4000	Counts
4) Integrator Output Zero	0 to 400	Counts

* This time period is fixed. The integration period for the TC822 is:

$$T_{INT} = \frac{4000}{f_{OSC}} = 2000 \text{ Counts}$$

where f_{OSC} is the clock oscillator frequency.

ANALOG PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+, V_{IN}^-)

The TC822 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The maximum input voltage range, which includes normal-mode + common-mode signals, is ±0.5V.

Common-mode voltages are removed from the system when V_{IN}^- is connected to Analog Common. The TC822's on-chip DC-to-DC converter eliminates most common-mode difficulties and permits measurements where measurement and power grounds cannot be isolated. (see Figure 4)

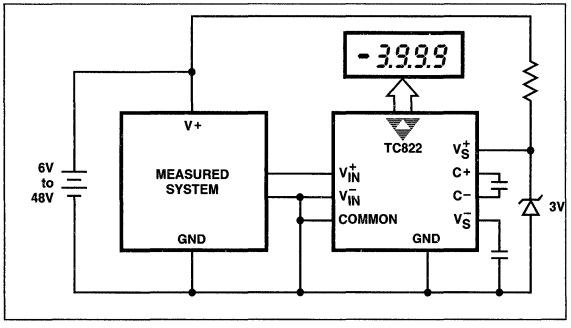


Figure 4 DC-to-DC Converter Permits Ground Referenced Measurements

Common-mode voltages with respect to power GND do, however, affect the integrator output level. The user must be particularly careful that the integrator does not saturate when at minimum battery voltage. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 5). For such applications the integrator output swing can be reduced below the recommended 1.5V full-scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

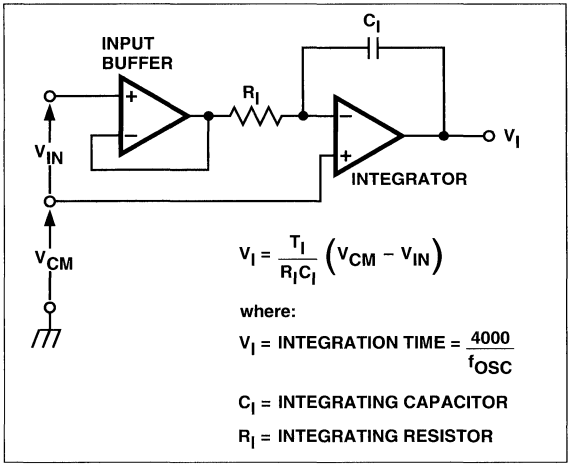


Figure 5 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Reference Inputs (V_{REF}^+, V_{REF}^-)

The TC822 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors.

Reference Output (REFOUT)

This pin is the buffered output of the internal CMOS band-gap reference. The output voltage is typically 1.3V above power GND, with a load current of 25 µA. The temperature coefficient of REFOUT is typically 50 ppm/°C.

Analog Common

The TC822 connects the internal V_{IN}^+ and V_{IN}^- inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}^- is connected to Analog Common. If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

The Analog Common pin serves to set the analog section reference or common point. The TC822 is specifically designed to operate from a battery or in any measurement system where input signals are referenced to the TC822 power source, so Analog Common is normally connected to power GND.

DIGITAL PIN FUNCTIONAL DESCRIPTION

DP1, DP2

These inputs control the LCD decimal points. The decimal point truth table is shown in Table 1. These inputs have internal 3 µA pulldowns to DGND.

Table 1 TC822 Decimal Point Truth Table

Decimal Point Inputs DP2	DP1	LCD
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

Hold

HOLD can be used to hold or 'freeze' the display. Connecting this pin to V_S^+ inhibits the display update process. Conversions will continue, but the display will not change.

APPLICATIONS INFORMATION

Power Supplies

The TC822 is designed to operate from a 3V battery, but will operate over a range of 2.0 to 4.0V. An on-chip DC-to-DC converter converts the +3V supply to –3V, which permits bipolar input voltages to be converted. Measurements are referenced to battery ground, so that the TC822 is ideal for applications such as measuring battery voltage, battery charging current, etc.

Op-Amp Power Supply Current

The Op-Amp of the TC822 has a low-distortion class A output, which is biased at 100 µA. To reduce supply current when the op-amp is not being used, connect the non-inverting input to V_S^-, as shown in Figures 6 and 11. When the op-amp is used, supply current will increase by about 200 µA.

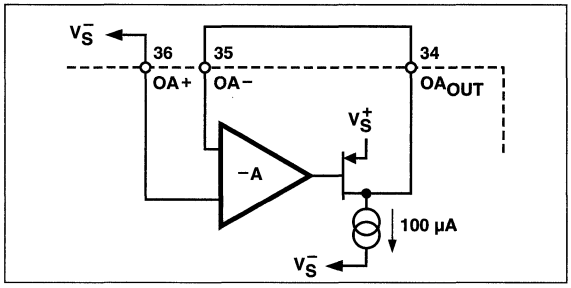


Figure 6 Simplified Op-Amp Output Schematic

Clock Oscillator

The crystal oscillator circuit is shown in Figure 7. An inexpensive 32.768 kHz watch crystal gives about 27 dB noise rejection at 60 Hz, while a 40 kHz crystal (used in ultrasonic alarms) will almost totally reject 50 and 60 Hz noise.

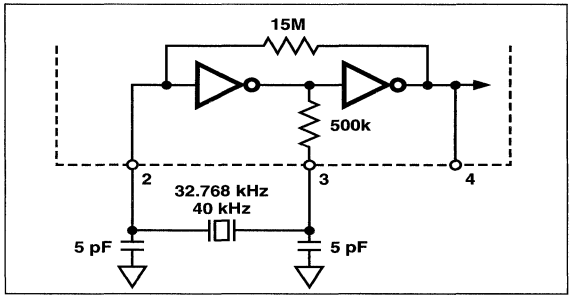


Figure 7 Crystal Oscillator Circuit

System Clock

All system timing is derived from the clock oscillator. The clock oscillator is divided by two prior to clocking the A/D counters. The clock is also divided by 4 to drive the DC-to-DC converter, and by 768 to generate the LCD backplane frequency. A simplified diagram of the system clock is shown in Figure 8.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The size of the Auto Zero capacitor (C_{AZ}) has some effect on system noise. A 0.22 µF capacitor is recommended. A capacitor with low dielectric absorption (polyester) is required.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate

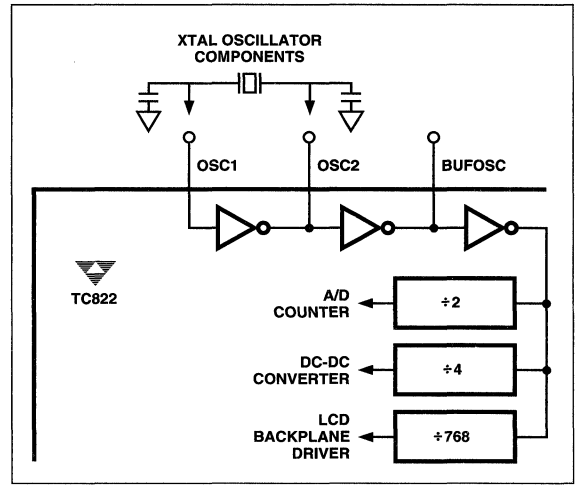


Figure 8 System Clock Generation

cycle is stored on C_{REF}. A 0.22 µF capacitor is typical. A good quality, low leakage capacitor, such as polyester, should be used.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±1.5 V integrator output swing is optimum when the analog input is near full-scale. For 2.5 readings / second (f_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.27 µF value is suggested. For a 32.768 kHz crystal, use 0.22 µF. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±1.5V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT} \bullet R_{INT} \bullet f_{OSC}}$$

where: f_{OSC} = Clock frequency
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 5 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive

region but not so large that printed circuit board leakage currents induce errors. For a 400 mV full-scale, R_{INT} should be about 100 kΩ.

Reference Voltage Selection

A full scale reading (4000 counts for TC822) requires that the input signal be twice the reference voltage. For example, a 400 mV full scale TC822 requires a reference voltage of 200 mV.

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 500 mV for 4000 lb/in^2. Rather than dividing the input voltage by 1.25, the reference voltage should be set to 250 mV. This permits the transducer input to be used directly. For best results, full scale voltage should be limited to 500 mV.

The TC822 can also operate with an external reference. Figure 9 shows internal and external reference applications.

Ratiometric Resistance Measurements

The TC822 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 10). The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \cdot 2000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$

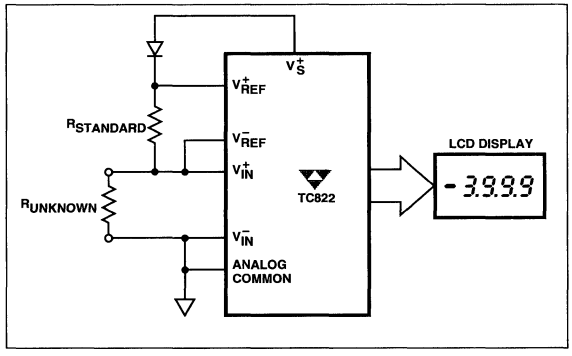


Figure 10 Low Parts Count Ratiometric Resistance Measurement

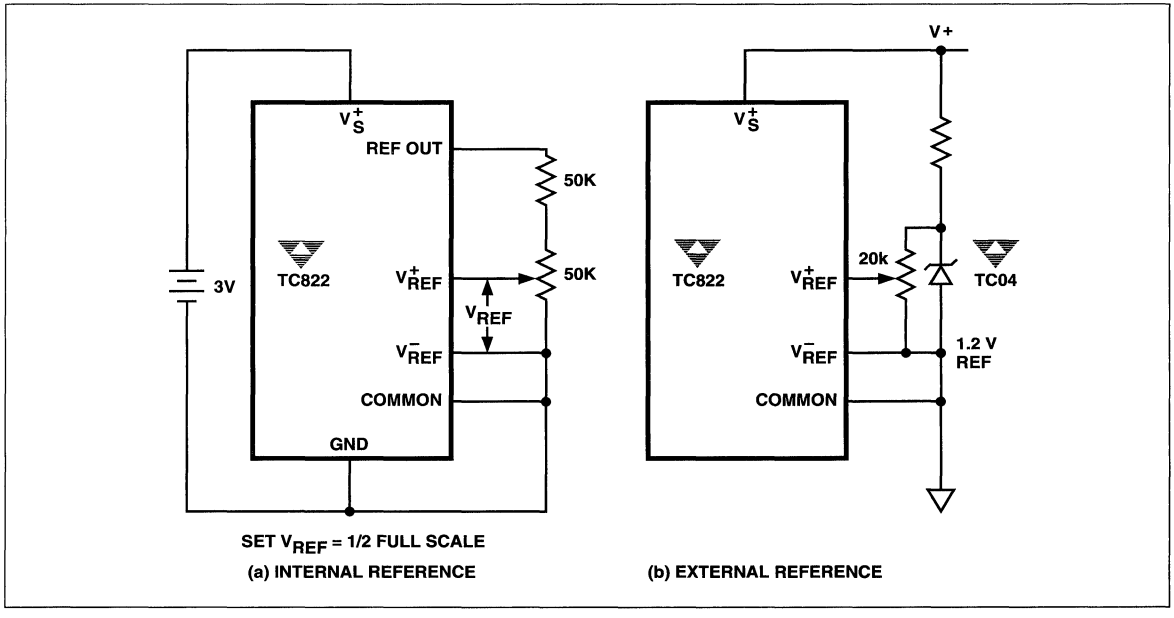


Figure 9 Internal and External Reference Applications

TC822

AC-to-DC Converter

The on-chip Op amp of the TC822 can be combined with external components to convert an AC voltage into a DC voltage. Figure 11 shows a typical circuit.

LCD

The TC822 drives a triplex (multiplexed 3:1) liquid crystal display with three backplanes. The LCD includes decimal points, polarity sign, and annunciators for data hold and low-battery. Table 2 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 768.

Table 2 LCD Pin Assignment, TC822

Pin	COM1	COM2	COM3
1	COM1	—	—
2	—	COM2	—
3	—	—	COM3
4	B0	C0	D0
5	A0	G0	E0
6	BATTERY	F0	P1
7	B1	C1	D1
8	A1	G1	E1
9	HOLD	F1	P2
10	B2	C2	D2
11	A2	G2	E2
12	Y	F2	P3
13	B3	C3	D3
14	A3	G3	E3
15	—	—	—
16	—	—	—
17	—	—	—
18	—	—	—

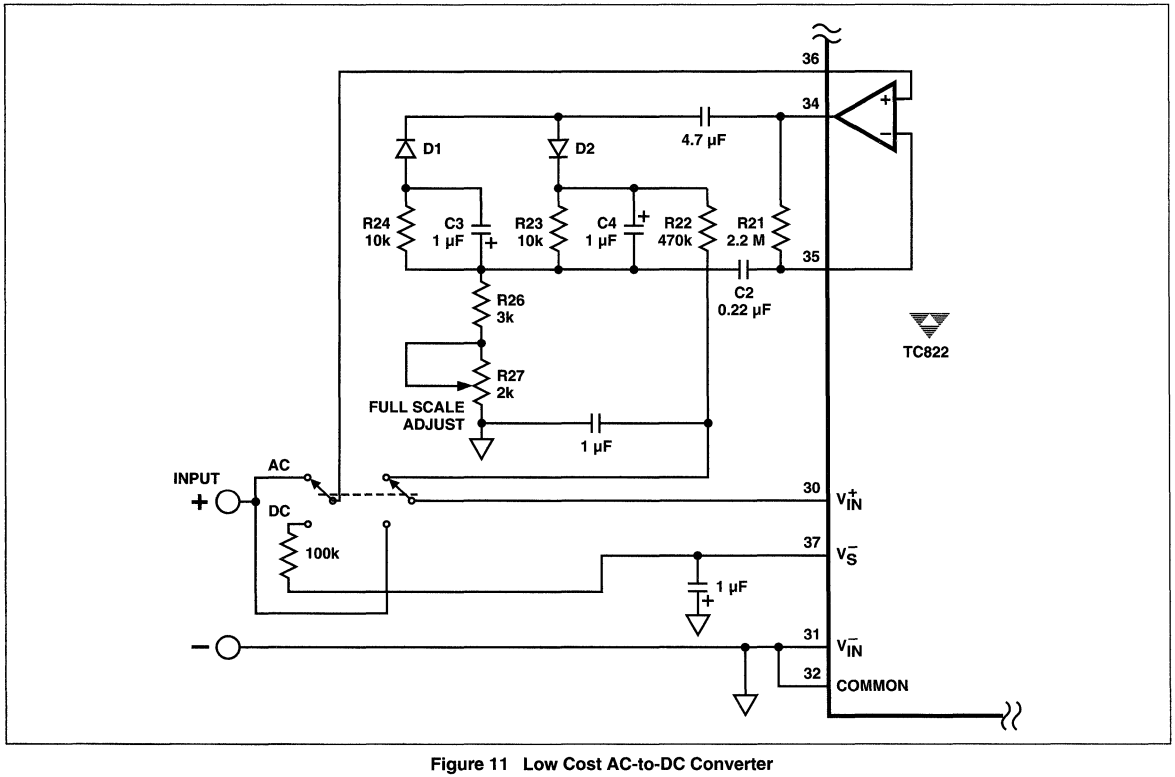


Figure 11 Low Cost AC-to-DC Converter

Backplanes waveforms are shown in Figure 12. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

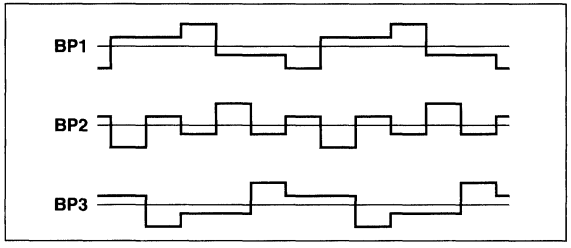


Figure 12 Backplane Waveforms

Other display output lines have waveforms that vary depending on the displays values. Figure 13 shows a set of waveforms for the AGE outputs of one digit for several combinations of 'on' segments.

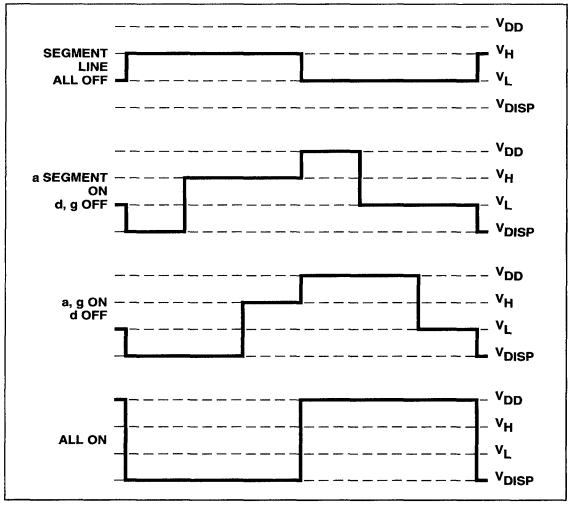


Figure 13 Typical Display Output Waveforms

LCD Source

Although most users will design their own custom LCD, a standard display for the TC822 is available. Figure 14 shows a display, part No. VIM428-DP, available from Varitronix.

Varitronix (USA)
VL Electronics
3171 Los Feliz Blvd
Suite 303
Los Angeles, CA 90039
Tel: (312) 661-8883
FAX: (213) 663-3711
Part No.:jg VIM428-DP

Varitronix
9/F Liven House
61-63 King Yip Street
Kwun Tjong
Hong Kong
Tel: 3-410286
FAX: 3-439555

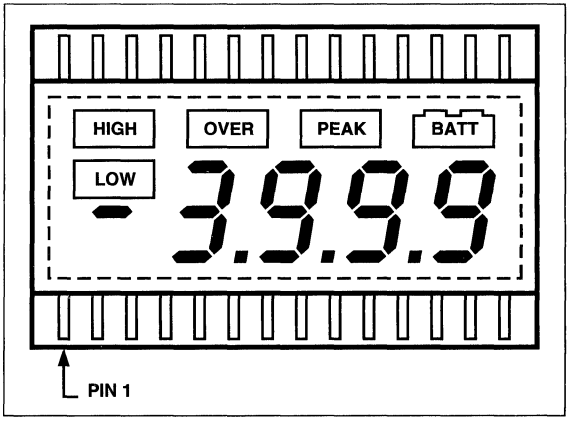


Figure 14 Typical TC822 LCD

Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 52 Hz when f_{OSC} = 40 kHZ). The peak-to-peak amplitude is the same as the backplane and segment driver outputs. Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

LCD Drive Voltage

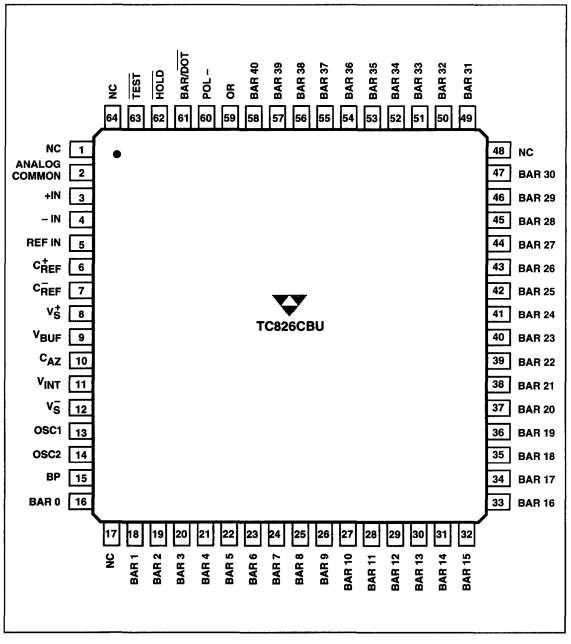
The peak-to-peak LCD drive voltage is typically 3.2 Vpp. This voltage will remain stable until the battery voltage falls below the point where the low-battery flag turns on (about 2.1V).

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

FEATURES

- **Bipolar A/D Conversion**
- **2.5% Resolution**
- **Direct LCD Display Drive**
- **'Thermometer' Bar or Dot Display**
- **40 Data Segments Plus Zero**
- **Overrange Plus Polarity Indication**
- **Precision On–Chip Reference ..... 35 ppm/°C**
- **Differential Analog Input**
- **Low Input Leakage ..... 10 pA**
- **Display Flashes on Overrange**
- **Display Hold Mode**
- **Auto–Zero Cycle Eliminates Zero Adjust Potentiometer**
- **9V Battery Operation**
- **Low Power Consumption ..... 1.1 mW**
- **20 mV to 2.0 V Full–Scale Operation**
- **Non–Multiplexed LCD Drive for Maximum Viewing Angle**

PIN CONFIGURATION



GENERAL DESCRIPTION

In many applications a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TC826 is a complete analog–to–digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full–scale differential input voltage range extends from 20 mV to 2V. The TC826 sensitivity is 500 μv. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design required only 125 μA from a 9V battery. In +5V systems a TC7660 DC to DC converter can supply the –5V supply. The differential analog input leakage is a low 10 pA.

Two display formats are possible. The BAR mode display is like a 'thermometer' scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto–zero phase maximizes noise immunity and eliminates zero–scale adjustment potentiometers. Zero–scale drift is a low 5 μV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TC826 prototyping work.

ORDERING INFORMATION

Part No.	Package	Temperature
TC826CBU	64–Pin Plastic Quad Flat Package	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(1) ..... V+ to V–
Package Power Dissipation
Flat Package ..... 500 mW
Operating Temperature
'C' Devices ..... 0°C to +70°C
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

unless otherwise stated V_S = 9V; ROSC = 430 kΩ; T_A = 25°C; Full–Scale = 20 mV.

No.	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
1	—	Zero Input	V_{IN} = 0.0V	– 0	±0	+0	Display
2	—	Zero Reading Drift	V_{IN} = 0.0V 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
3	NL	Linearity Error	Max Deviation From Best Straight Line	– 1	0.5	+1	Count
4	R/O	Rollover Error	$-V_{IN} = +V_{IN}$	– 1	0	+1	Count
5	EN	Noise	V_{IN} = 0V	—	60	—	μV_{P-P}
6	ILK	Input Leakage Current	V_{IN} = 0V	—	10	20	pA
7	CMRR	Common–Mode Rejection Ratio	VCM = ±1V V_{IN} = 0V	—	50	—	µV/V
8	—	Scale Factor Temperature Coefficient	0 ≤ T_A ≤ 70°C External Ref. Temperature Coefficient = 0 ppm/°C	—	1	—	ppm/°C
9	VCTC	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ 70°C	—	35	100	ppm/°C
10	V_{COM}	Analog Common Voltage	250 kΩ Between Common and V_S^+	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V_{P-P}
12	VBD	LCD Backplane Drive Voltage		4	5	6	V_{P-P}
13	I_{DD}	Power Supply Current		—	125	175	µA

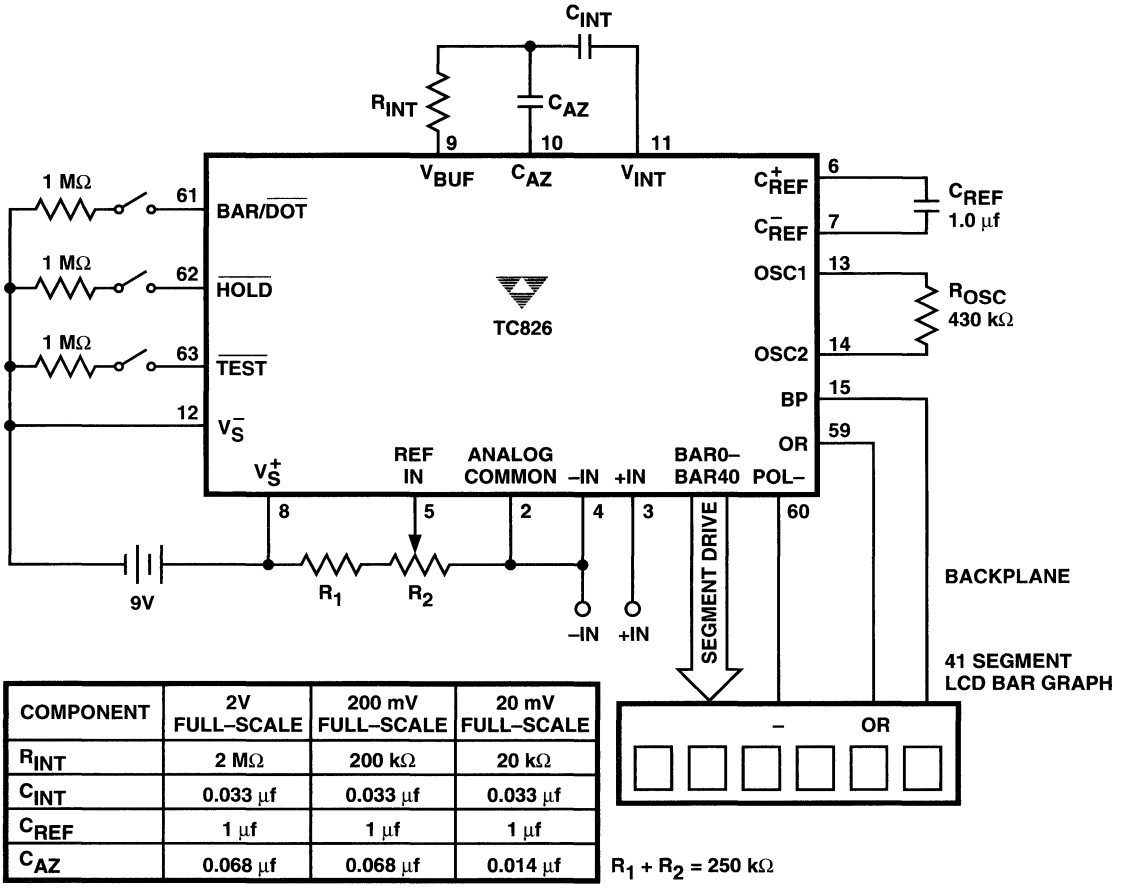
NOTES:
1. Input voltages may exceed the supply voltages when the input current is limited to 100 µA.
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
3. Backplane drive is in phase with segment drive for 'off' segment and 180°C out of phase for 'on' segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, and 60 should be connected through 1 MΩ series resistors to V_S^- for logic 0.

TC826 PIN DESCRIPTION

Pin No. (Plastic Quad Flat Package)	Symbol	Description
1	NC	
2	Analog Common	Establishes the internal analog ground point. Analog common is set to 2.9V below the positive supply by an internal zener reference circuit. The voltage difference between VS+ and analog-common can be used to supply the TC826 voltage reference input at REF IN (Pin 5).
3	+IN	Positive analog signal input.
4	-IN	Negative analog signal input.
5	REF IN	Reference voltage positive input. Measured relative to analog-common. REF IN ≈ Full-Scale/2.
6	CREF +	Reference capacitor connection.
7	CREF -	Reference capacitor connection.
8	VS+	Positive supply terminal.
9	VBUF	Buffer output. Integration resistor connection.
10	CAZ	Negative comparator input. Auto-zero capacitor connection.
11	VINT	Integrator output. Integration capacitor connection.
12	VS-	Negative supply terminal.
13	OSC1	Oscillator resistor (ROSC) connection.
14	OSC2	Oscillator resistor (ROSC) connection.
15	BP	LCD Backplane driver.
16	BAR 0	LCD Segment driver: Bar 0
17	NC	
18	BAR 1	Bar 1
19	2	2
20	3	3
21	4	4
22	5	5
23	6	6
24	7	7
25	8	8
26	9	9
27	10	10
28	11	11
29	12	12
30	13	13
31	14	14
32	15	15
33	16	16
34	17	17
35	18	18
36	19	19
37	20	20
38	21	21
39	22	22
40	23	23

TC826 PIN DESCRIPTION (Cont.)

Pin No. (Plastic Quad Flat Package)	Symbol	Description
41	BAR 24	LCD Segment driver: Bar 24
42	25	25
43	26	26
44	27	27
45	28	28
46	29	29
47	30	30
48	NC	
49	31	31
50	32	32
51	33	33
52	34	34
53	35	35
54	36	36
55	37	37
56	38	38
57	39	39
58	40	40
59	OR	LCD segment driver that indicated input out–of–range condition.
60	POL–	LCD segment driver that indicates input signal is negative.
61	BAR / $\overline{\text{DOT}}$	Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to V_S^- through 1MΩ resistor for Dot format.
62	$\overline{\text{HOLD}}$	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_S^- through 1MΩ series resistor for HOLD mode operation.
63	$\overline{\text{TEST}}$	Input logic signal. Sets TC826 to BAR display mode. Bar 0 to 40, plus OR flash on and off. The POL– LCD driver is on. Pulled high internally to inactive state. Connect to V_S^- with 1 MΩ series resistor to activate.
64	NC	



COMPONENT	2V FULL-SCALE	200 mV FULL-SCALE	20 mV FULL-SCALE
R_{INT}	2 MΩ	200 kΩ	20 kΩ
C_{INT}	0.033 µf	0.033 µf	0.033 µf
C_{REF}	1 µf	1 µf	1 µf
C_{AZ}	0.068 µf	0.068 µf	0.014 µf

$R_1 + R_2 = 250$ kΩ

Figure 1 Typical TC826 Circuit Connection

DUAL SLOPE CONVERSION PRINCIPLES

The TC826 is a dual slope, integrating analog–to–digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (TSI). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (TRI). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to 'ramp–up' and 'ramp–down'.

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

Where:
V_R = Reference Voltage
V_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}: $V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3.)

The TC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

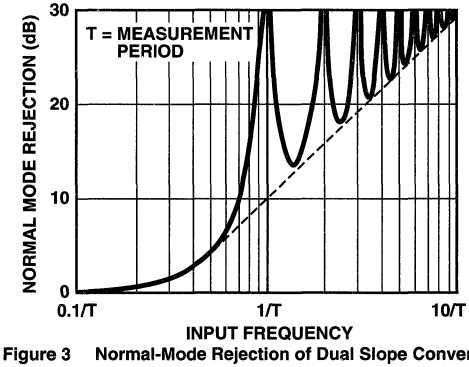


Figure 3 Normal-Mode Rejection of Dual Slope Converter

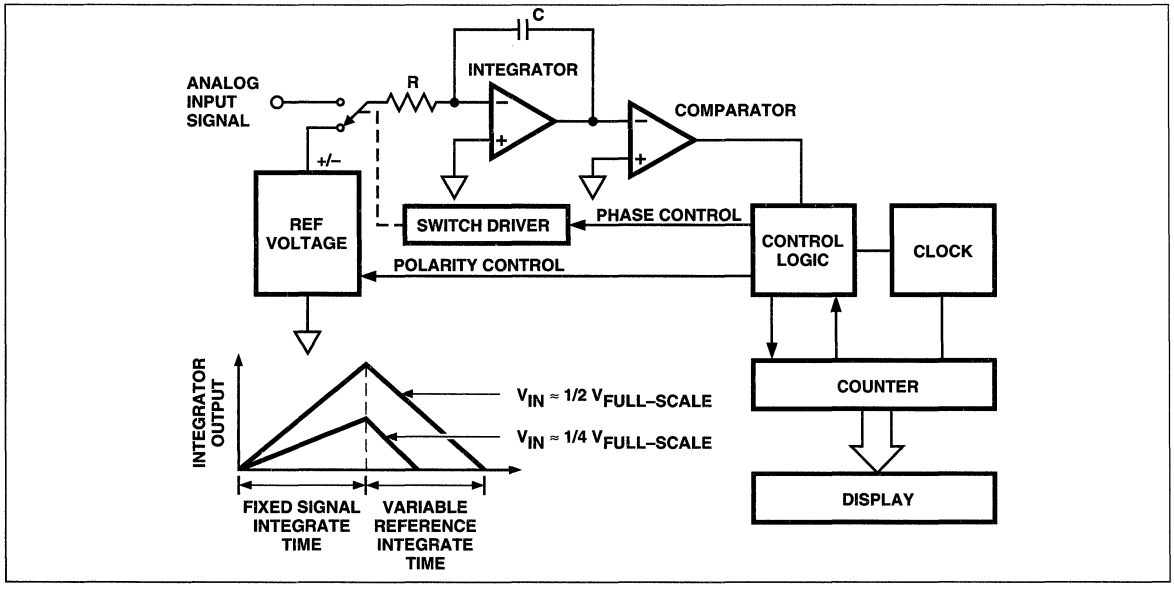


Figure 2 Basic Dual Slope Converter

THEORY OF OPERATION

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above, the TC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference cycle. (Figures 4 and 5.)

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and –IN. The differential input signal is integrated for a fixed time period. The TC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is divided by 32 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

Where:

F_{OSC} = External Clock Frequency

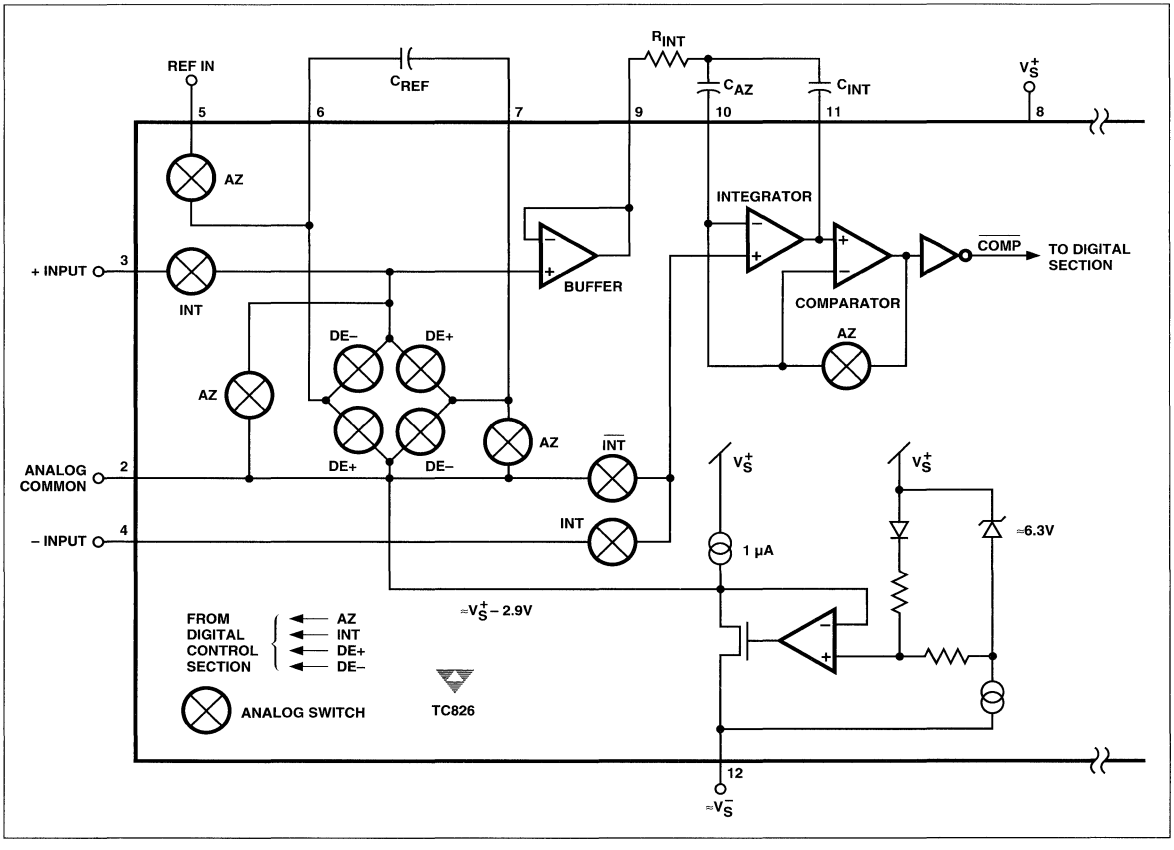


Figure 4 TC826 Analog Section

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, –IN should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. –IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

$$20 = \frac{V_{IN}}{V_{REF}}$$

System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
  For signals less than full-scale the auto-zero is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

$$T_{SI} = 20 \left| \frac{32}{F_{OSC}} \right|$$

  Where F_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 5) and Analog-Common (Pin 2).

Required Full-Scale Voltage	V_{REF}
20 mV	10 mV
2V	1V

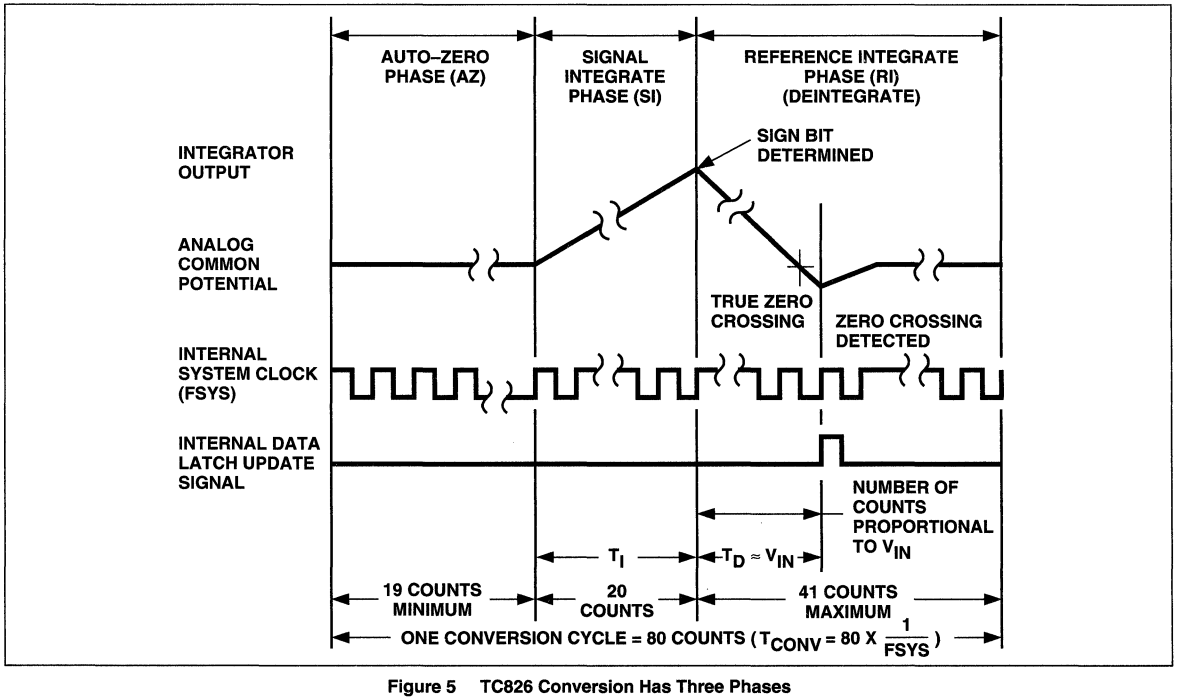


Figure 5 TC826 Conversion Has Three Phases

The internal voltage reference potential availabe at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired refer to Figure 6.

The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

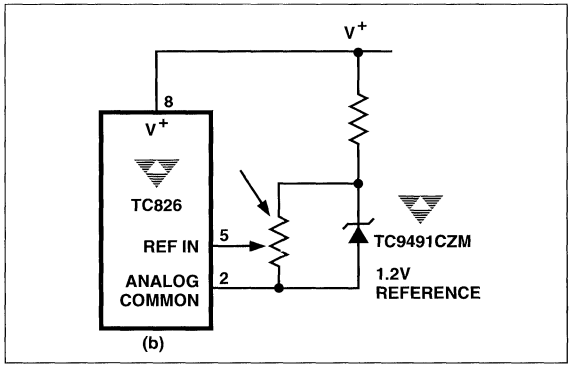


Figure 6 External Reference

Components Value Selection

Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1 μA drive current with minimal linearity error. RINT is easily calculated for a 1 μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{VFS}{1 \times 10^{-6}}$$

Where VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4V of V_S^+ or V_S^- without saturating.

The integrating capacitor is easily calculated:

$$CINT = \frac{VFS}{RINT}\left(\frac{640}{FOSC \times VINT}\right)$$

Where : VINT = Integrator Swing
FOSC = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

CAZ should be 2–3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14 μF to 0.068 μF are satisfactory.

Reference Capacitor (CREF)

A 1 μF capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1 Suggested Component Values

Component	2V Full-Scale $V_{REF} \approx 1V$	200 mV Full-Scale $V_{REF} \approx 100$ mV	20 mV Full-Scale $V_{REF} \approx 10$ mV
R_{INT}	2 MΩ	200 kΩ	20 kΩ
C_{INT}	0.033 μF	0.033 μF	0.033 μF
C_{REF}	1 μF	1 μF	1 μF
C_{AZ}	0.068 μF	0.068 μF	0.14 μF
R_{OSC}	430 kΩ	430 kΩ	430 kΩ

NOTES: Approximately 5 conversions/second.

Differential Signal Inputs

The TC826 is designed with true differential inputs and accepts input signals within the input stage common–mode voltage range (VCM). The typical range is $V^+ -1$ to $V^- +1V$. Common–mode voltages are removed from the system when the TC826 operates from a battery or floating power source (Isolated from measured system) and –IN is connected to analog–common (V_{COM}).

In systems where common–mode rejection ratio minimizes error. Common–mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full–scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2V full–scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

Digital Section

The TC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430 kΩ $_{OSC}$ gets the backplane frequency to approximately 55 Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is 'OFF'. An out–of–phase segment drive signal causes the segment to be 'ON' or

visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment drive, –POL, is 'ON' for negative analog inputs. If +IN and –IN are reversed this indicator would reverse. The TC826 transfer function is shown in Figure 7.

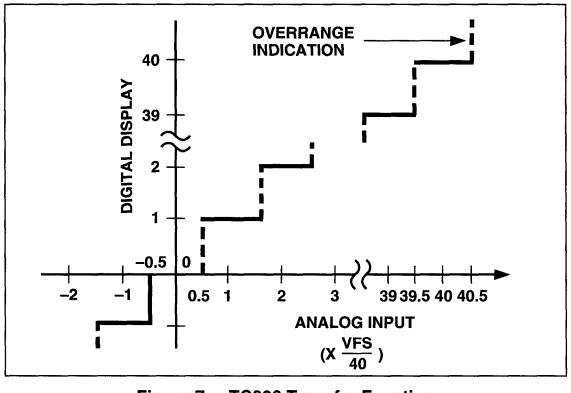


Figure 7 TC826 Transfer Function

BAR / $\overline{\text{DOT}}$ Input (Pin 61)

The BAR / $\overline{\text{DOT}}$ input allows the user to select the display format. The TC826 powers up in the BAR mode. Select the DOT display format by connecting BAR / $\overline{\text{DOT}}$ to the negative supply (Pin 12) through a 1 MΩ resistor.

$\overline{\text{HOLD}}$ Input (Pin 62)

The TC826 data output latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 12) through a 1 MΩ resistor. The LCD display continuously displays the previous conversion results.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

$\overline{\text{TEST}}$ Input (Pin 63)

The TC826 enters a test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 12). The connection must be made through a 1 MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annunciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL–) segment will be on but not flashing

Overrange Display Operation (OR, Pin 59)

An out–of–range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 59) becoming active.

In the BAR display format the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is on fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR flashes and all other data segment drivers are off.

Polarity Indication (POL–Pin 60)

The TC826 converts and displays data for positive and negative input signals. The POL–LCD segment driver (Pin 60) is active for negative signals.

Oscillator Operation

The TC826 external oscillator frequency, FOSC, is set by resistor ROSC connected between pins 13 and 14. The oscillator frequency vs. resistance curve is shown in Figure 8.

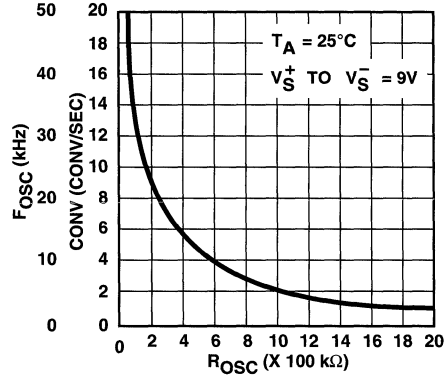


Figure 8 Oscillator Frequency vs. ROSC

FOSC is divided by 32 to provide an internal system clock, FYSY. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320.

The internal oscillator may be bypassed by driving OSCI (Pin 13) with an external signal generator. OSC2 (Pin 14) should be left unconnected.

The oscillator should swing from V_S^+ to V_S^- in single supply operation (Figure 9). In dual supply operation the signal should swing from power supply ground to V_S^+.

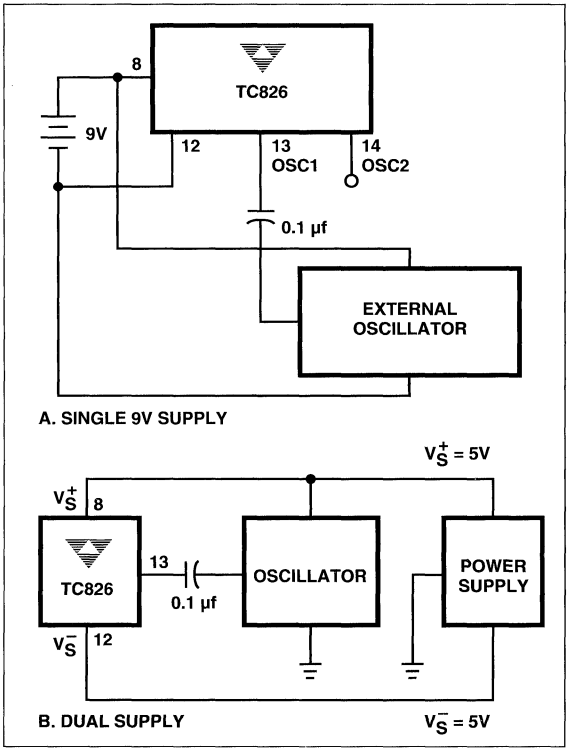


Figure 9 External Oscillator Connection

LCD Display Format

The input signal can be displayed in two formats (Figure 10). The BAR / $\overline{\text{DOT}}$ input (Pin 61) selects the format. The TC826 measurement cycle operates identically for either mode.

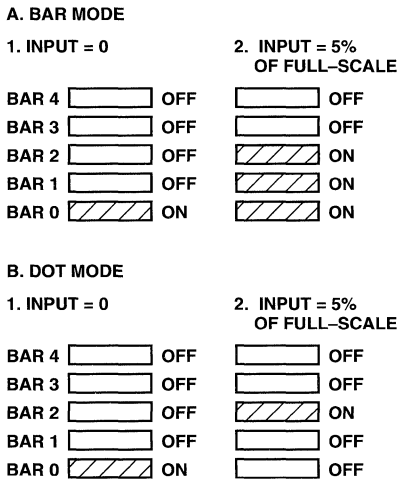


Figure 10 Display Option Formats

BAR Format

The TC826 power-ups in the BAR mode. BAR / $\overline{\text{DOT}}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equaling the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR / $\overline{\text{DOT}}$ to V_S^- through a 1 MΩ resistor the DOT mode is selected. Only the BAR LCD segment equaling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or 'needle' applications.

LCD DISPLAYS

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TC826 LCD display is available from Varitronix.

Varitronix Ltd.
9/F Linen House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Telex: 36643 VTRAX HX

USA Office:
VL Electronics Inc.
3161 Los Feliz Blvd., Suite 303
Los Angeles, CA 90039
Tel: 213/661-8883
Telex: 821554

- Part No.: VBG412-1 (Pin Connectors)
- Part No.: VBG412-2 (Elastomer Connectors)

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
Tel: 203/838-7509

- Part No. 5040: 50 segment circular display with 3 digit numeric scale.
- Part No. 5020: 50 segment linear display.

LCD BACKPLANE DRIVER (PIN 15)

Additional drive electronics is not required to interface the TC826 to an LCD display. The TC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$FBP = FOSC/256$$

Figure 11 gives typical backplane driver rise/fall time vs. backplane capacitance.

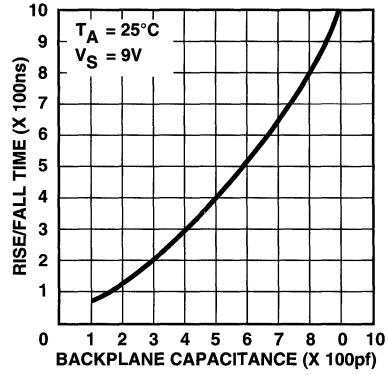


Figure 11 Backplane Driver Rise/Fall Time vs. Capacitance

FLAT PACKAGE SOCKET

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
Tel: 415/856-9332
Telex: 910/373-2060

'BQ' Socket Part No.: IC51-064-042 BQ

3-1/2 DIGIT A/D CONVERTER

FEATURES

- **Internal Reference with Low Temperature Drift**
  TC7106/7 ..... 80 ppm/°C Typical
  TC7106A/7A ..... 20 ppm/°C Typical
- **Drives LCD (TC7106) or LED (TC7107) Display Directly**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise for Stable Display**
- **Auto-Zero Cycle Eliminates Need for Zero Adjustment**
- **True Polarity Indication for Precision Null Applications**
- **Convenient 9 V Battery Operation (TC7106A)**
- **High Impedance CMOS Differential Inputs .... $10^{12}\Omega$**
- **Differential Reference Inputs Simplify Ratiometric Measurements**
- **Low Power Operation ..... 10 mW**

ORDERING INFORMATION

PART CODE **TC710X X X XXX**

6 = LCD
7 = LED

A or blank*

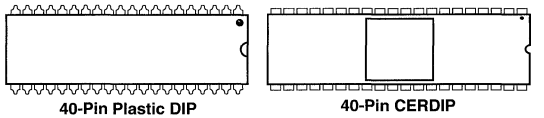
R (reversed pins) or blank (CPL pkg only)

* "A" parts have an improved reference TC

Package Code (see below):

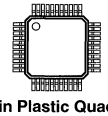
Package Code	Package	Pin Layout	Temperature Range
CPL	40-Pin PDIP	Normal	0°C to +70°C
IPL	40-Pin PDIP	Normal	– 25°C to +85°C
IJL	40-Pin CerDIP	Normal	– 25°C to +85°C
CKW	44-Pin PQFP	Formed Leads	0°C to +70°C
CLW	44-Pin PLCC	—	0°C to +70°C

AVAILABLE PACKAGES



40-Pin Plastic DIP

40-Pin CERDIP



44-Pin Plastic Quad Flat Package Formed Leads

44-Pin Plastic Chip Carrier PLCC

GENERAL DESCRIPTION

The TC7106A and TC7107A 3-1/2 digit direct-display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device has a precision reference with a 20 ppm/°C max temperature coefficient. This represents a 4 to 7 times improvement over similar 3-1/2 digit converters. Existing 7106 and 7107 based systems may be upgraded without changing external passive component values. The TC7107A drives common anode light emitting diode (LED) displays directly with 8 mA per segment. A low-cost, high-resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7106A low power drain and 9 V battery operation make it suitable for portable applications.

The TC7106A/TC7107A reduces linearity error to less than 1 count. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero-volts input.

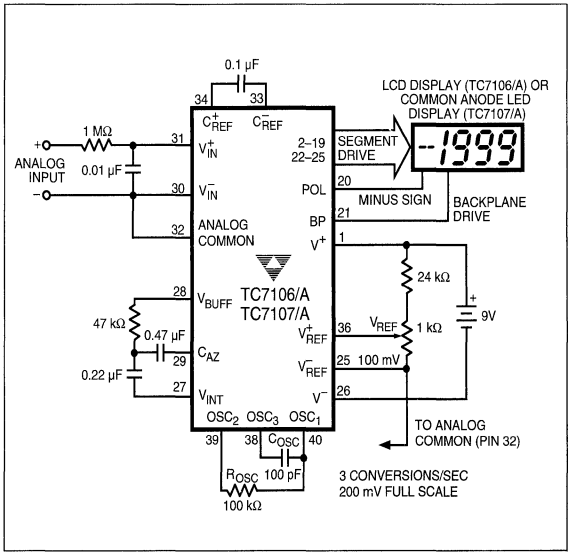


Figure 1 TC7106/A/7/A Typical Operating Circuit

TC7106/7106A
TC7107/7107A

ABSOLUTE MAXIMUM RATINGS*

TC7106A

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
- CerDIP Package ..... 1000 mW
- Plastic Package ..... 800 mW

Operating Temperature
- "C" Devices ..... 0°C to +70°C
- "I" Devices ..... – 25°C to +85°C

Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

TC7107A

Supply Voltage
- V+ ..... +6 V
- V– ..... –9 V

Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V+
Power Dissipation (Note 2)
- CerDIP Package ..... 1000 mW
- Plastic Package ..... 800 mW

Operating Temperature
- "C" Devices ..... 0°C to +70°C
- "I" Devices ..... – 25°C to +85°C

Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Conditions	TC7106/A & TC7107/A Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	– 000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \cong$ 200 mV	– 1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	– 1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk – Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C	—	0.2	1	µV/°C
	V_{IN} = 0 V "I" Device = –25°C to +85°C	—	1.0	2	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm°C)	—	1	5	ppm/°C
	V_{IN} = 199.0 mV "I" Device = –25°C to +85°C	—	—	20	ppm/°C
Supply Current (Does Not Include LED Current For TC7107/A)	V_{IN} = 0	—	0.8	1.8	mA

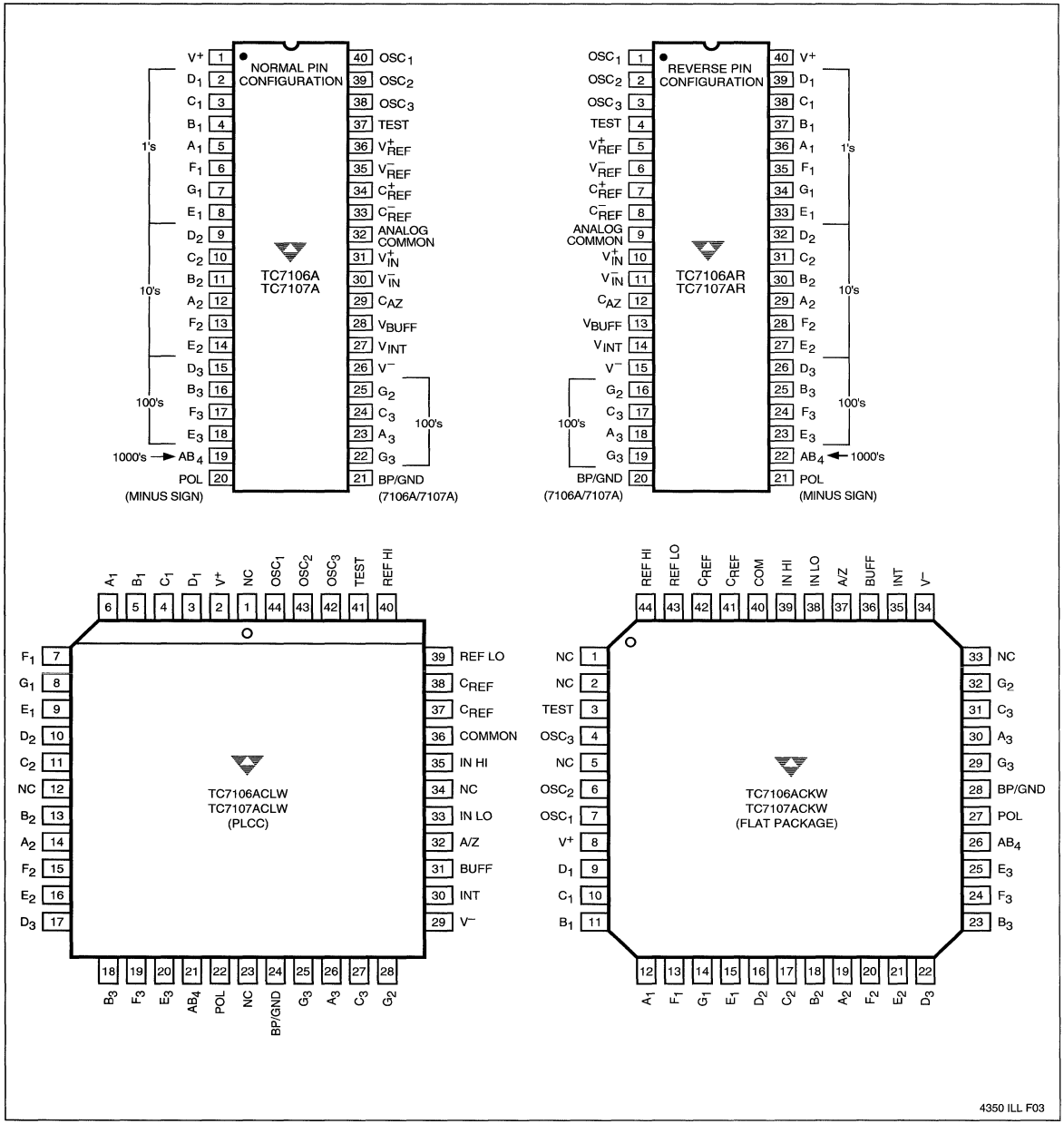
ELECTRICAL CHARACTERISTICS (CONT.) (Note 3)

Characteristics	Conditions	TC7106/A & TC7107/A Min	Typ	Max	Unit
Analog Common Voltage (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 70°C ("C", Commercial Temp. Range Devices)	 7106A/7A 7106/7	 20 80	 50 —	 ppm/°C ppm/°C
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply –25°C ≤ T_A ≤ 85°C ("I," Industrial Temp. Range Devices)	 —	 —	 75	 ppm/°C
TC7106A ONLY Pk – Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TC7106A ONLY Pk – Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TC7107A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TC7107A ONLY Segment Sinking Current (Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES: 1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply to both the TC7106/A and TC7107/A at TA = 25°, f_{CLOCK} = 48 kHz. Parts are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.

TC7106/7106A
TC7107/7107A

PIN CONFIGURATIONS



PIN DESCRIPTION

40-Pin DIP Pin Number (Normal)	(Reverse)	Symbol	Description
1	(40)	V^+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP GND	LCD Backplane drive output (TC7106A). Digital ground (TC7107A).
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V^-	Negative power supply voltage.
27	(14)	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for more details
28	(13)	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for a 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47-μF capacitor for 200 mV full scale, and a 0.047-μF capacitor for 2V full scale. See Paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	V_{IN}^-	The analog LOW input is connected to this pin.
31	(10)	V_{IN}^+	The analog HIGH input signal is connected to this pin.
32	(9)	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See paragraph on ANALOG COMMON for more details.
33	(8)	C_{REF}^-	See pin 34.

PIN DESCRIPTION (CONT,)

40-Pin DIP Pin Number (Normal)	(Reverse)	Symbol	Description
34	(7)	C^+_{REF}	A 0.1-µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V^-_{IN} pin is not at analog common), and a 200-mV scale is used, a 1-µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	V^-_{REF}	See pin 36.
36	(5)	V^+_{REF}	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	Test	Lamp test. When pulled HIGH (to V^+) all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under TEST for additional information.
38	(3)	OSC_3	See pin 40.
39	(2)	OSC_2	See pin 40.
40	(1)	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48-kHz clock (3 readings per section), connect pin 40 to the junction of a 100-kΩ resistor and a 100-pF capacitor. The 100-kΩ resistor is tied to pin 39 and the 100-pF capacitor is tied to pin 38.

General Theory of Operation
Dual Slope Conversion Principles

(All Pin Designations Refer to the 40-Pin DIP)

The TC7106A and TC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 2A).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

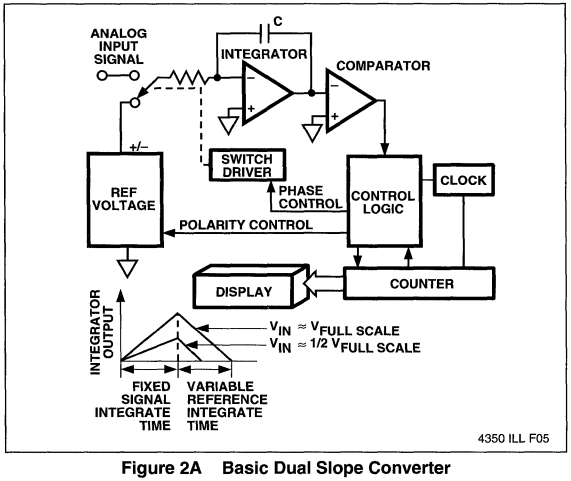


Figure 2A Basic Dual Slope Converter

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period. (Figure 2B)

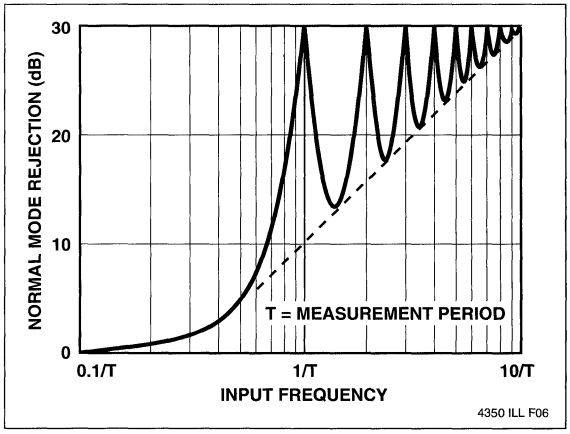


Figure 2B Normal-Mode Rejection of Dual Slope Converter

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without adjusting external potentiometers. A complete conversion consists of three cycles: an auto-zero, signal-integrate and reference-integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero-input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 μV.

The auto-zero cycle length is 1000 to 3000 counts.

Signal Integrate Cycle

When the auto-zero loop is opened, the internal differential inputs connect to V_{IN}^{+} and V_{IN}^{-}. The differential input signal is integrated for a fixed time period. The signal integration period is 1000 counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range (1 V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^{-} should be tied to analog common.

Polarity is determined at the end of the signal integrate phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection, limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. V_{IN}^{-} is internally connected to analog common and V_{IN}^{+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Digital Section (TC7106A)

The TC7106A (Figure 3) contains all the segment drivers necessary to directly drive a 3 1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^{+} and V_{IN}^{-} are reversed, this indicator will reverse.

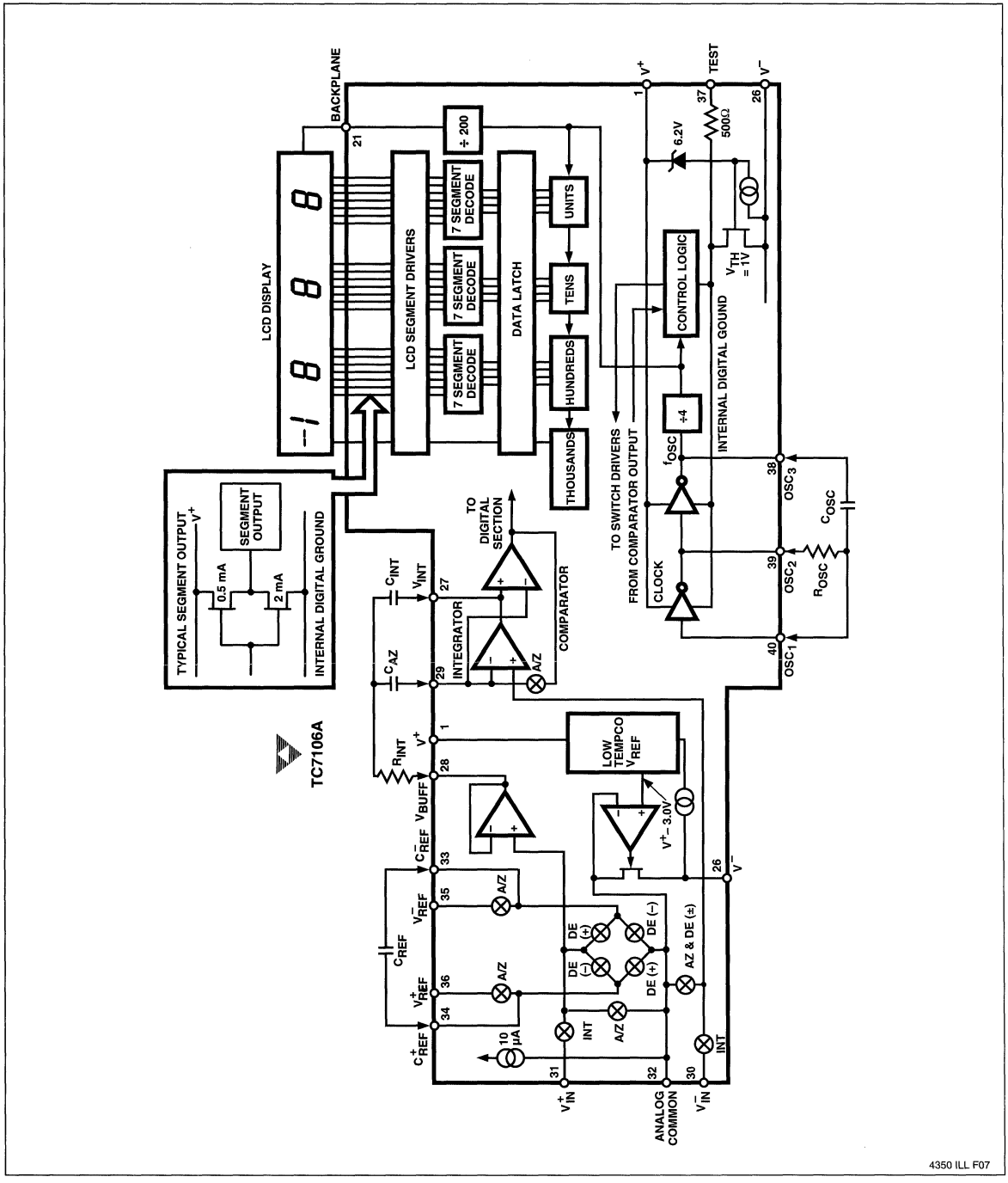


Figure 3 TC7106A Block Diagram

When the TEST pin on the TC7106A is pulled to V+, all segments are turned "ON." The display reads –1888. During this mode the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES! LCD displays may be destroyed if operated with DC levels for extended periods.

The display font and the segment drive assignment are shown in Figure 4.

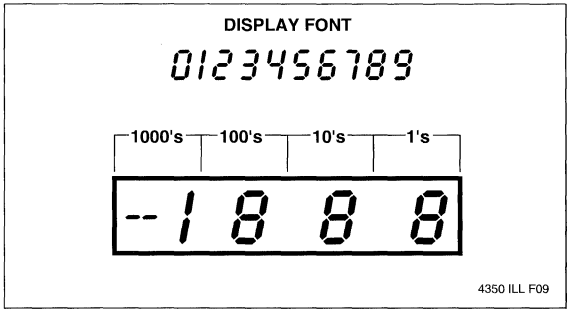


Figure 4 Display Font and Segment Assignment

In the TC7106A, an internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

Digital Section (TC7107A)

Figure 5 shows the TC7107A. It is designed to drive common anode LEDs. It is identical to the TC7106A except that the regulated supply and backplane drive have been eliminated and the segment drive is typically 8 mA. The 1000's output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability.

In both devices, the polarity indication is "ON" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TC7106A.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three-phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale, the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TC7106A/7107A are drop-in replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

Clock Circuit

Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

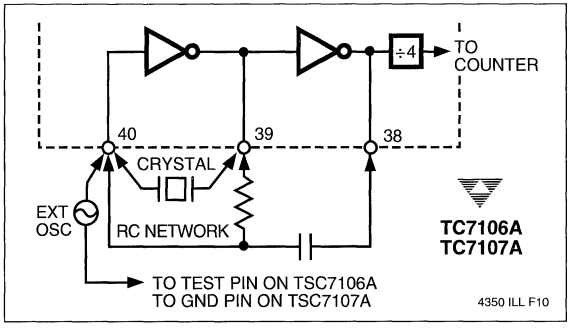


Figure 6 Clock Circuits

Component Value Selection
Auto-Zero Capacitor – C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.047 µF capacitor is adequate for 2.0 V full-scale applications. A mylar dielectric capacitor is adequate.

Reference Voltage Capacitor – C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference-integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires 200 mV full-scale, increase C_{REF} to 1.0 µF. Rollover error will be held to less than 1/2 count. A mylar dielectric capacitor is adequate.

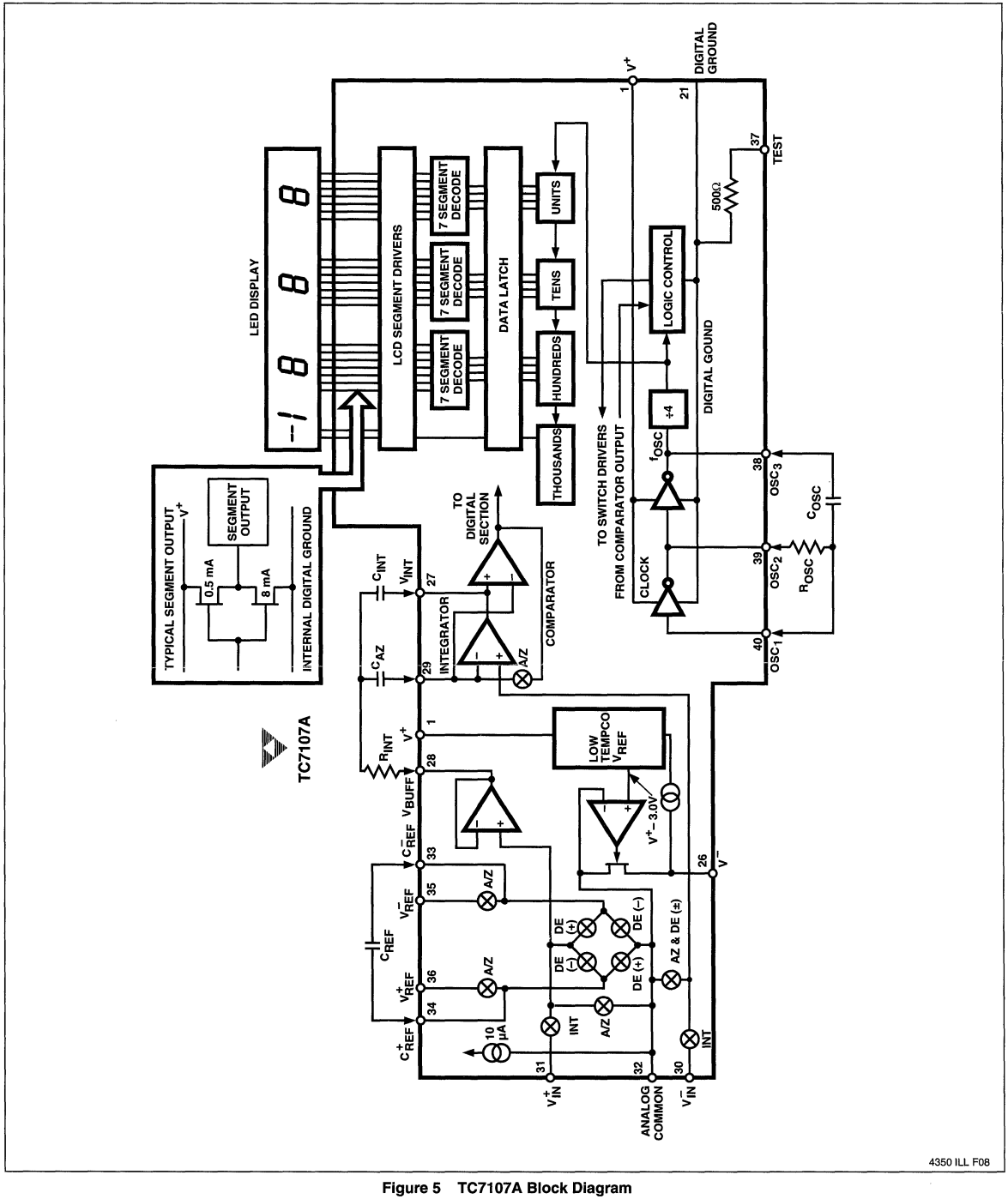


Figure 5 TC7107A Block Diagram

Integrating Capacitor – C_{INT}

C_{INT} should be selected to maximize the integrator output voltage swing without causing output saturation. Due to the TC7106A/7107A superior temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.22 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

INTEGRATING RESISTOR – R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 µA. The integrator and buffer can supply 20 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale, R_{INT} is 47 kΩ. 2.0 V full-scale requires 470 kΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 µF	0.047 µF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 µF	0.22 µF

Note: 1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

R_{OSC} (Pin 40 to Pin 39) should be 100 kΩ. C_{OSC} is selected using the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For f_{OSC} of 48 kHz, C_{OSC} is 100 pF nominally.

Note that f_{OSC} is divided by four to generate the TC7106A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal-integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48kHz, 40 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally-generated reference voltage is desired, refer to Figure 7.

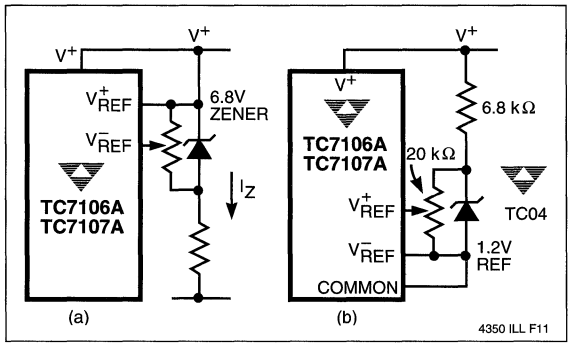


Figure 7 External Reference

Device Pin Functional Description

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TC7106A/7017A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ –1.0 to V^- +1 V. Common-mode voltages are removed from the system when the TC7106A/TC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to analog common (V_{COM}): See Figure 8.

V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increasing linearity errors.

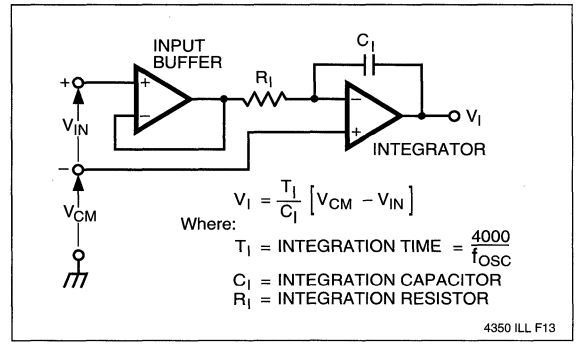


Figure 9 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference (V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

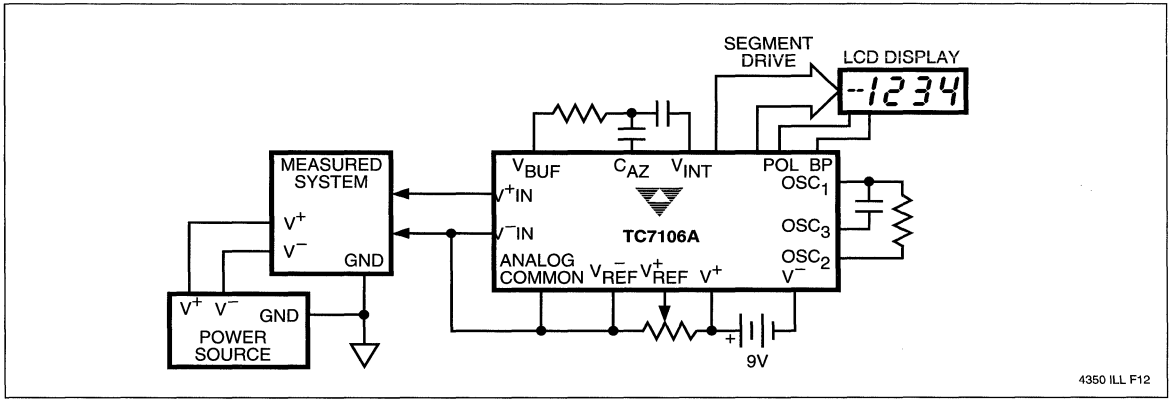


Figure 8 Common-Mode Voltage Removed in Battery Operation with V_{IN}^- = Analog Common

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 9). For such applications the integrator output swing can be reduced below the recommended 2.0

The TC7106A/TC7107A circuits have a significantly lower analog common temperature coefficient. This gives a very stable voltage suitable for use as a reference. The temperature coefficient of analog common is 20 ppm/°C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to the N channel FET capable of sinking 20 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ –3.0 V).

The TC7106A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TC7106A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7106A power source. The analog common potential of V^+ –3.0 V gives a 6 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- >$ 7.0 V) analog common is a very stable potential with excellent temperature stability—typically 20 ppm/°C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/°C maximum temperature coefficient. See Internal Voltage Reference discussion.

Test (Pin 37)

The TEST pin potential is 5 V less than V^+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500Ω resistor in the TC7106A. The TEST pin load should be no more than 1mA .

If TEST is pulled to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TC7106A. With TEST = V^+ the LCD segments are impressed with a DC voltage which will destroy the LCD.

The TEST pin will sink about 10 mA when pulled to V^+.

Internal Voltage Reference Stability

The analog common voltage temperature stability has been significantly improved (Figure 10). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 11 shows analog common supplying the necessary voltage reference for the TC7106A/TC7107A.

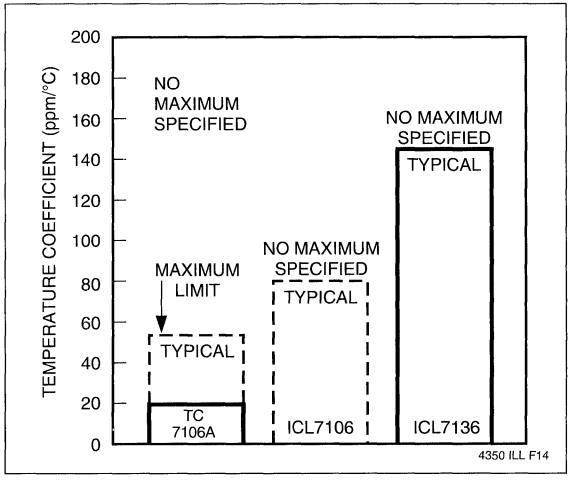


Figure 10 Analog Common Temperature Coefficient

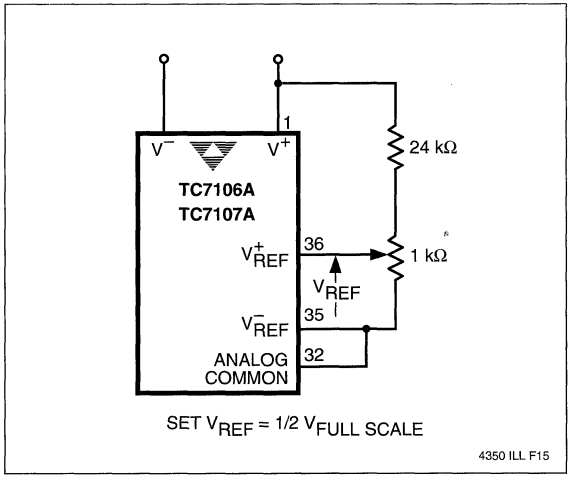


Figure 11 Internal Voltage Reference Connection

Power Supplies

The TC7107A is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC. (Figure 12)

In selected applications a negative supply is not required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5V.
- An external reference is used.

The TC7660 DC to DC converter may be used to generate –5 V from +5 V (Figure 13).

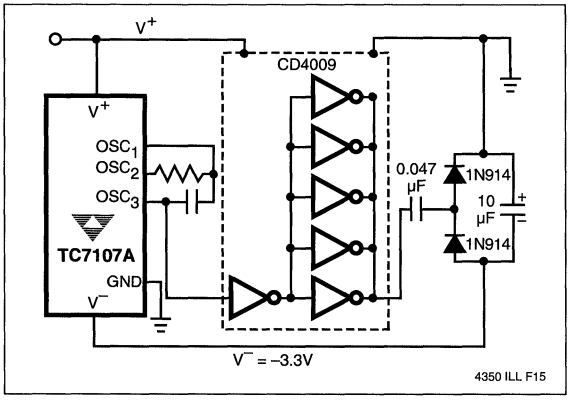


Figure 12 Generating Negative Supply From +5 V

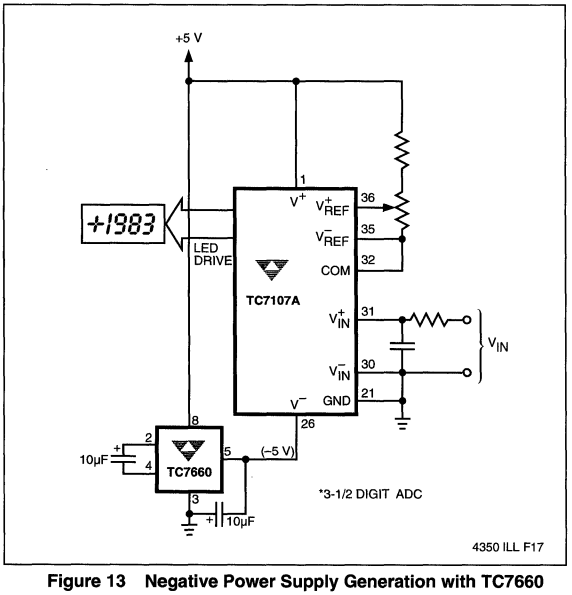


Figure 13 Negative Power Supply Generation with TC7660

TC7107 Power Dissipation Reduction

The TC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing the LED common anode voltage the TC7107A package power dissipation is reduced.

Figure 14 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5 V, the TC7107A output is at 3.2 V (point A on Figure 13). Maximum power dissipation is 8.1 mA x 3.2 V x 24 segments = 622 mW.

Notice, however, that once the TC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B in Figure 14) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is only 7.7 mA x 2.5 V x 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA x 2.2 V x 24 = 385 mW).

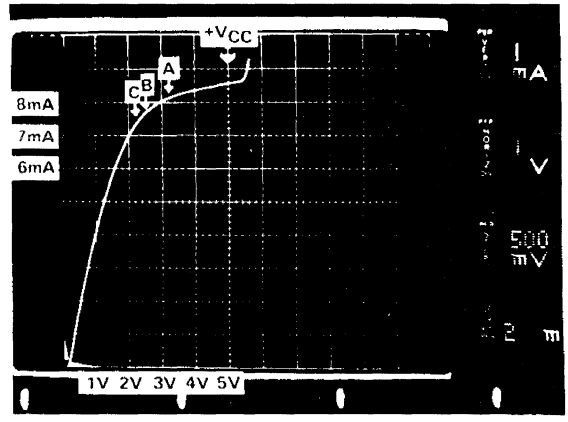


Figure 14 TC7107A Output Current vs Output Voltage

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

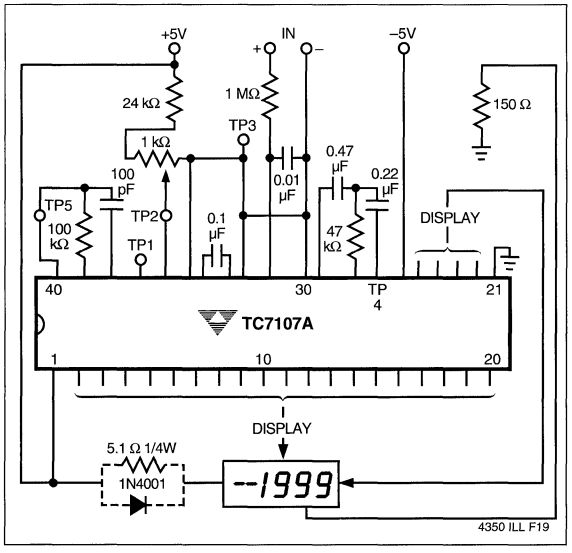


Figure 15 Diode or Resistor Limits Package Power Dissipation

APPLICATIONS INFORMATION
LIQUID CRYSTAL DISPLAY SOURCES

Several LCD manufacturers supply standard LCD displays to interface with the TC7106A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
Epson	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note: 1. Contact LCD manufacturer for full product listing/ specifications.

Light Emitting Diode Display Sources

Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TC7107A.

Manufacturer	Address	Display Type
Hewlett-Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
AND	770 Airport Blvd. Burlingame, CA 94010	LED

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than1 mA should be supplied by the TEST pin: its potential is approximately 5 V below V^+.

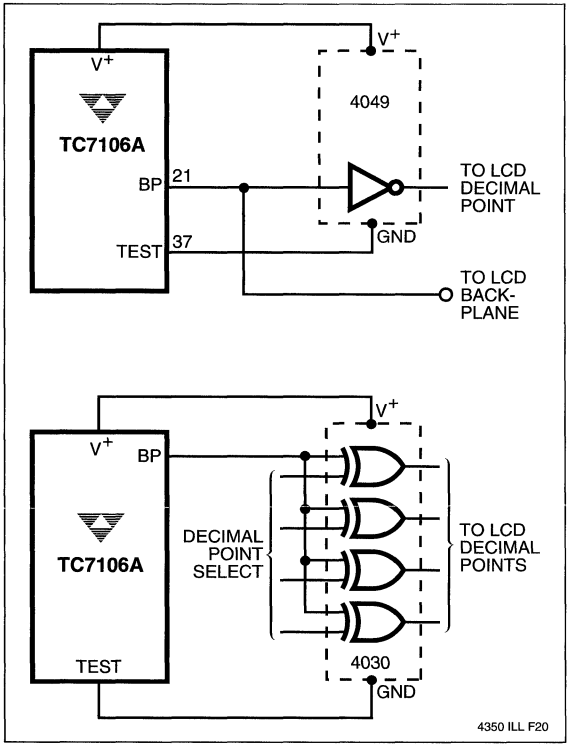


Figure 16 Decimal Point Drive Using TEST as Logic Ground

Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric reading possible. Typically in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R standard.

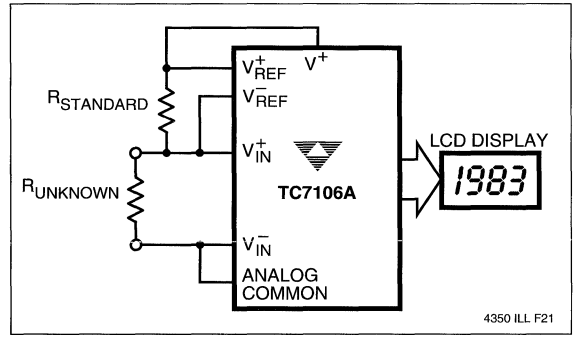


Figure 17 Low Parts Count Ratiometric Resistance Measurement

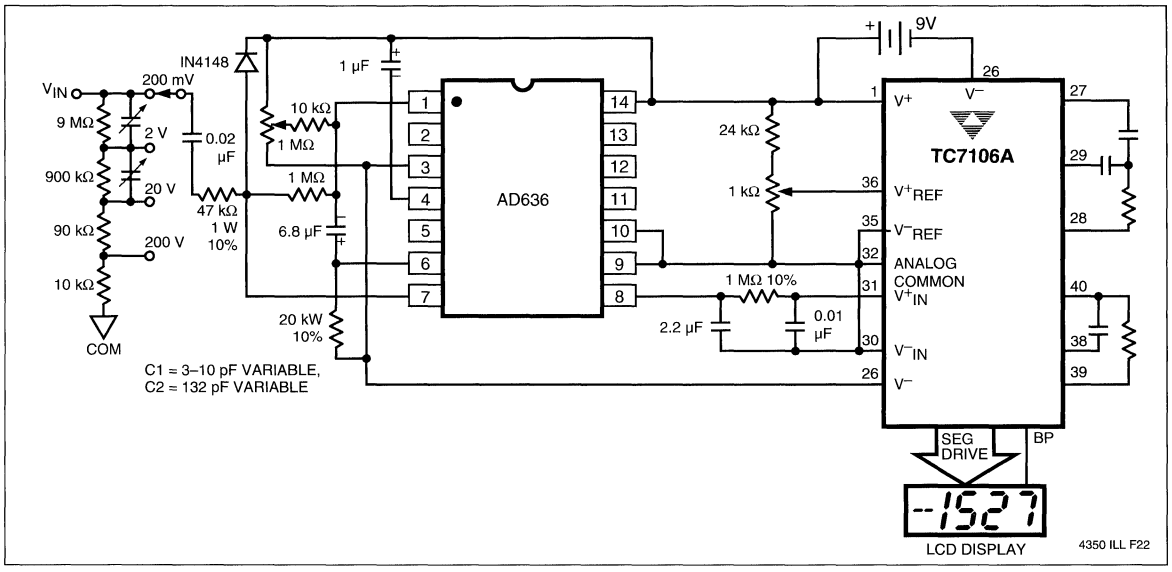


Figure 18 3 1/2 Digit True RMS AC DMM

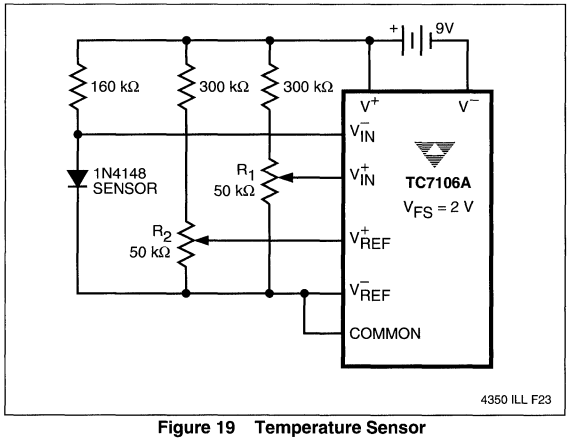


Figure 19 Temperature Sensor

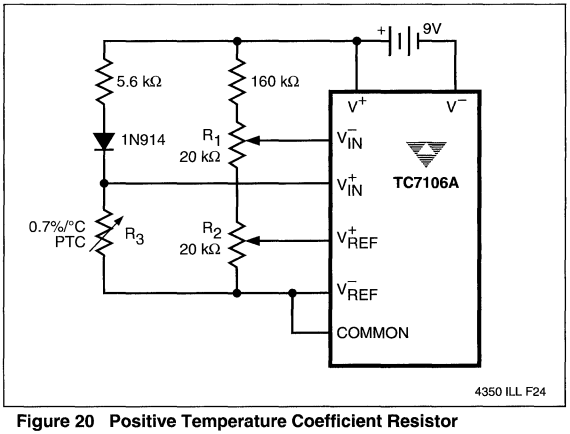


Figure 20 Positive Temperature Coefficient Resistor Temperature Sensor

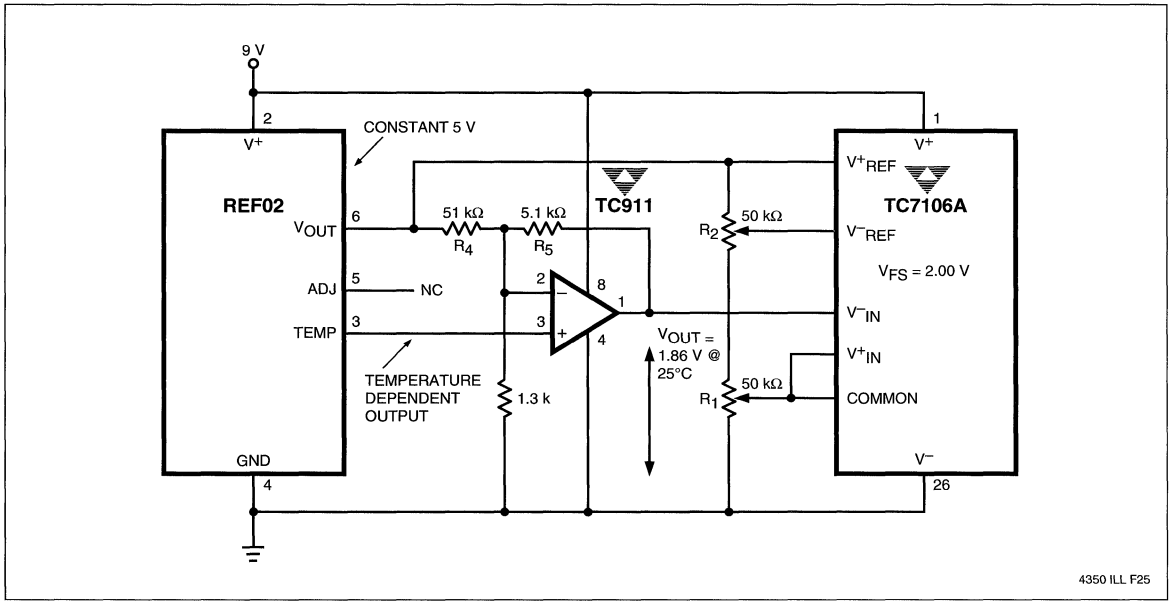


Figure 21 Integrated Circuit Temperature Sensor

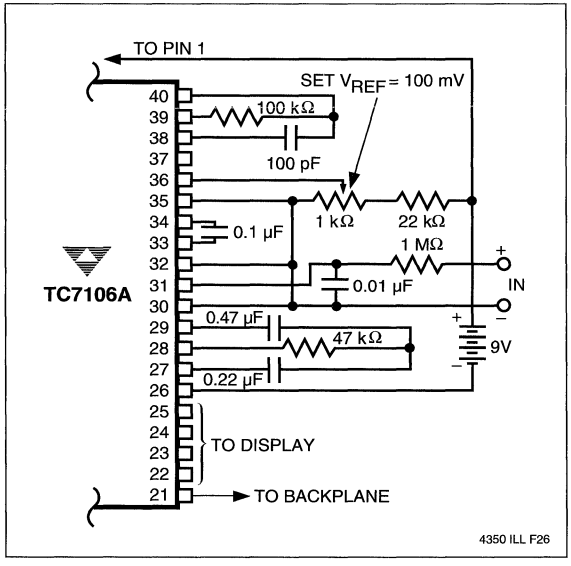


Figure 22 TC7106A Using the Internal Reference: 200 mV Full-Scale, 3 Readings-per-second (RPS).

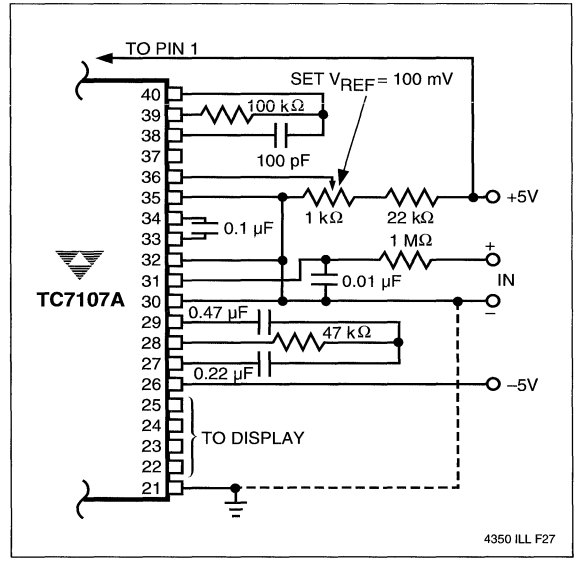


Figure 23 TC7107A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^- Tied to GND for Single Ended Inputs).

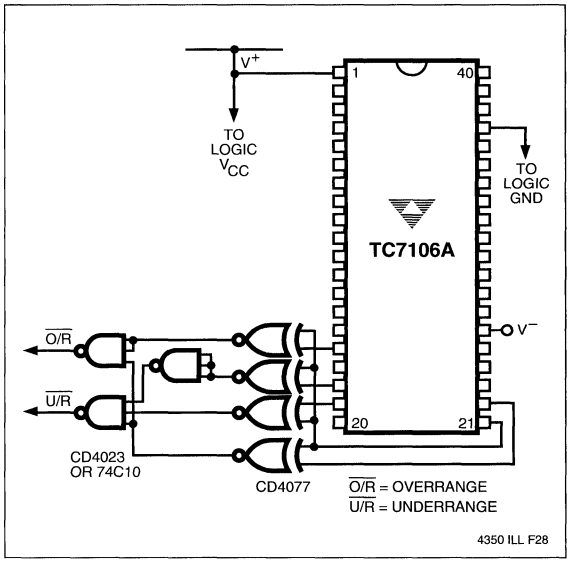


Figure 24 Circuit for Developing Underrange and Overrange Signals from TC7106A Outputs.

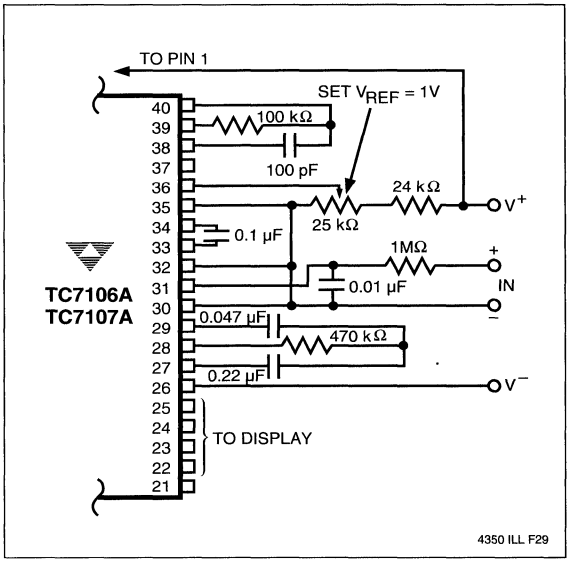


Figure 25 TC7106A/TC7107A: Recommended Component Values for 2.00 V Full-Scale

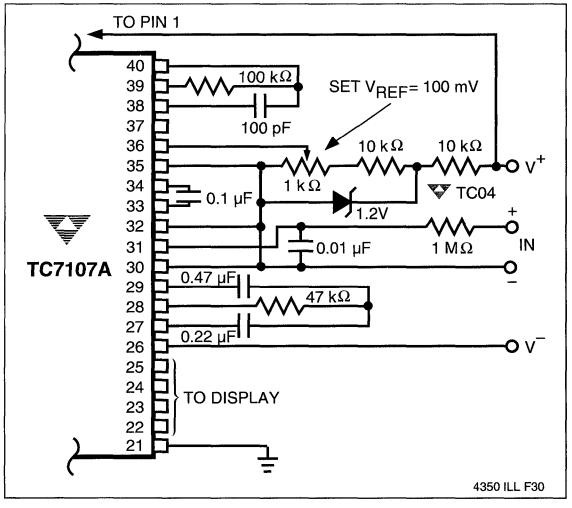


Figure 26 TC7107A With a 1.2 V External Band-Gap Reference. (V^-_{IN} Tied to Common.)

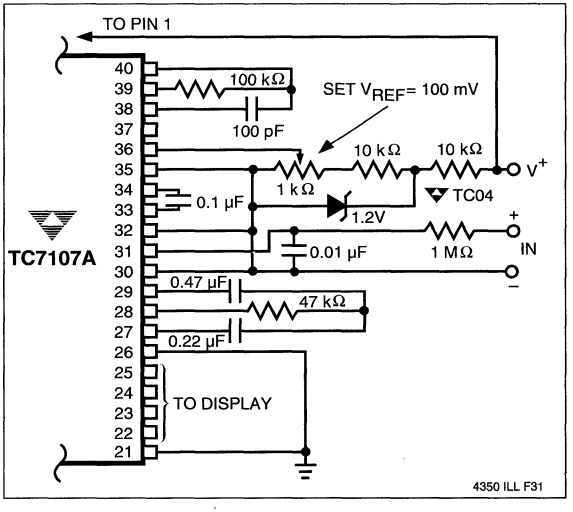


Figure 27 TC7107A Operated from Single +5 V Supply An External Reference Must Be Used in This Application.

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS WITH HOLD

2

FEATURES

- **Low Temperature Drift Internal Reference**
  - **TC7116/TC7117 ..... 80 ppm/°C Typ**
  - **TC7116A/TC7117A ..... 20 ppm/°C Typ**
- **Display Hold Function**
- **Directly Drives LCD or LED Display**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise for Stable Display ..... 2V or 200 mV Full-Scale Range (FSR)**
- **Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer**
- **True Polarity Indication for Precision Null Applications**
- **Convenient 9V Battery Operation (TC7116/TC7116A)**
- **High Impedance CMOS Differential Inputs .... $10^{12}\Omega$**
- **Low Power Operation ..... 10 mW**

ORDERING INFORMATION

PART CODE **TC711X X X XXX**

6 = LCD
7 = LED

A or blank*

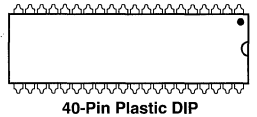
R (reversed pins) or blank (CPL pkg only)

* "A" parts have an improved reference TC

Package Code (see below):

Package Code	Package	Temperature Range
CPL	40-Pin PDIP	0°C to +70°C
CLW	44-Pin PLCC	0°C to +70°C
CKW	44-Pin PQFP	0°C to +70°C
IPL	40-Pin PDIP	– 25°C to +85°C

AVAILABLE PACKAGES



40-Pin Plastic DIP

44-Pin Plastic Quad Flat Package Formed Leads

44-Pin Plastic Chip Carrier PLCC

GENERAL DESCRIPTION

The TC7116A/TC7117A are 3-1/2 digit CMOS analog-to-digital converters (ADCs) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, polarity and digit drivers, voltage reference, and clock circuit are integrated on-chip. The TC7116A drives liquid crystal displays (LCDs) and includes a backplane driver. The TC7117A drives common anode light emitting diode (LED) displays directly with an 8-mA drive current per segment.

These devices incorporate a display hold (HLDR) function. The displayed reading remains indefinitely, as long as HLDR is held high. Conversions continue, but output data display latches are not updated. The reference low input ($V_{\overline{REF}}$) is not available as it is with the TC7106/7107. $V_{\overline{REF}}$ is tied internally to analog common in the TC7116A/7117A devices.

The TC7116A/7117A reduces linearity error to less than 1 count. Roll-over error (the difference in readings for equal magnitude but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a 0V input.

The TC7116A and TC7117A feature a precision, low-drift internal reference, and are functionally identical to the TC7116/TC7117. A low-drift external reference is not normally required with the TC7116A/TC7117A.

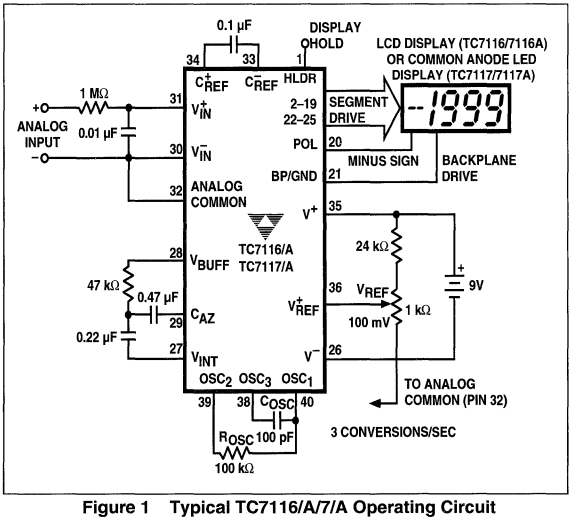


Figure 1 Typical TC7116/A/7/A Operating Circuit

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
- TC7116/TC7116A: V^+ to V^- 15V
- TC7117/TC7117A: V^+ to GND ..... +6V
- V^- to GND ..... – 9V

Analog Input Voltage (Either Input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Either Input) ..... V^+ to V^-
Clock Input
- TC7116/TC7116A ..... TEST to V^+
- TC7117/TC7117A ..... GND to V^+

Power Dissipation (Note 2)
- CerDIP ..... 1000 mW
- Plastic ..... 800 mW

Operating Temperature
- "C" Device ..... 0°C to +70°C
- "I" Device ..... – 25°C to +85°C

Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

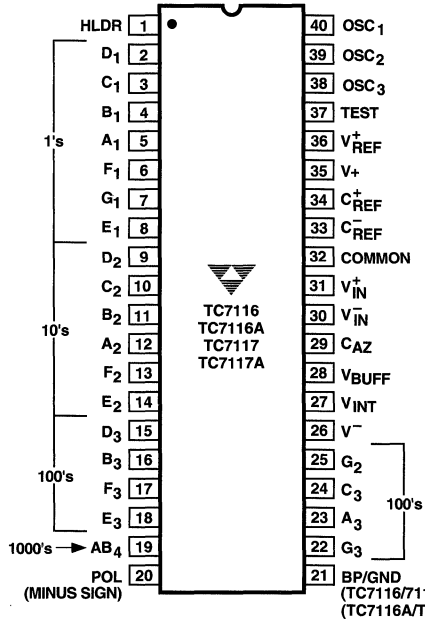
Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	—	±0	—	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Readings Near Full Scale)	$-V_{IN} = +V_{IN} \cong$ 200 mV or ≈ 2V	– 1	±0.2	+1	Counts
Linearity (Maximum Deviation From Best Straight Line Fit)	Full Scale = 200 mV or 2V	– 1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200 mV	—	50	—	µV/V
Noise (Peak-to-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V Full Scale = 200 mV	—	15	—	µV
Leakage Current at Input	V_{IN} = 0V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0V "C" Device: 0°C to +70°C "I" Device: –25°C to +85°C	 — —	 0.2 1	 1 2	 µV/°C µv/°C
Scale Factor Temperature Coefficient	V_{IN} = 199 mV "C" Device: 0°C to +70°C (Ext Ref = 0 ppm/°C) "I" Device: –25°C to +85°C	 — —	 1 —	 5 20	 ppm/°C ppm/°C
Input Resistance, Pin 1	Note 6	30	70	—	kΩ
V_{IL}, Pin 1	TC7116/A Only	—	—	Test +1.5	V
V_{IL}, Pin 1	TC7117/A Only	—	—	GND +1.5	V
V_{IH}, Pin 1	Both	$V^+ – 1.5$	—	—	V
Supply Current (Does Not Include LED Current for 7117/A)	V_{IN} = 0V	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Positive Supply)	25 kΩ Between Common and Positive Supply	2.4	3.05	3.35	V
Temperature Coefficient of Analog Common (With Respect to Positive Supply)	"C" Device: 0°C to +70°C TC7116A/TC7117A TC7116/TC7117	 — —	 20 80	 50 —	 ppm/°C ppm/°C
Temperature Coefficient of Analog Common (With Respect to Positive Supply)	"I" Device: –25°C to +85°C 25 kΩ Between Common and Positive Supply (TC7116A/TC7117A)	—	—	75	ppm/°C

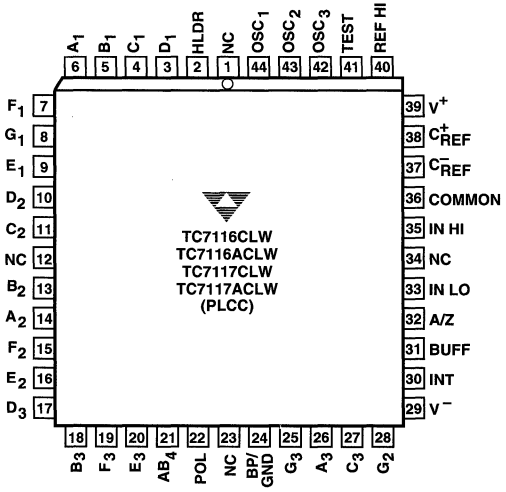
ELECTRICAL CHARACTERISTICS (Cont.)

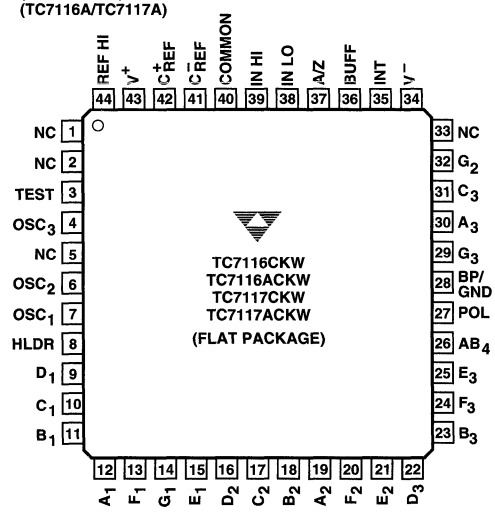
Parameter	Test Conditions	Min	Typ	Max	Unit
TC7116/TC7116A ONLY Peak-to-Peak Segment Drive Voltage	V^+ to V^- = 9V (Note 5)	4	5	6	V
TC7116/TC7116A ONLY Peak-to-Peak Backplane Drive Voltage	V^+ to V^- = 9V (Note 5)	4	5	6	V
TC7117/TC7117A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5V Segment Voltage = 3V	5	8	—	mA
TC7117/TC7117A ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5V Segment Voltage = 3V	10	16	—	mA

NOTES: 1. Input voltages may exceed supply voltages, provided input current is limited to ±100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at T_A = +25°C, f_{CLOCK} = 48 kHz. TC7116/TC7116A and TC7117/TC7117A are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in-phase with segment drive for "OFF" segment, 180° out-of-phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. The TC7116/TC7116A logic inputs have an internal pull-down resistor connected from HLDR, pin 1 to TEST, pin 37.
The TC7117/TC7117A logic inputs have an internal pull-down resistor connected from HLDR, pin 1 to GND, pin 21.

PIN CONFIGURATIONS







NOTES:
1. NC = No internal connection.
2. Pins 9, 25, 40, and 56 are connected to the die substrate. The potential at these pins is approximately V^+. No external connections should be made.

PIN DESCRIPTION

40-Pin DIP Pin Number Normal	44-Pin Plastic Quad Flat Package Pin Number	Symbol	Description
1	8	HLDR	Hold pin, Logic 1 holds present display reading.
2	9	D_1	Activates the D section of the units display.
3	10	C_1	Activates the C section of the units display.
4	11	B_1	Activates the B section of the units display.
5	12	A_1	Activates the A section of the units display.
6	13	F_1	Activates the F section of the units display.
7	14	G_1	Activates the G section of the units display.
8	15	E_1	Activates the E section of the units display.
9	16	D_2	Activates the D section of the tens display.
10	17	C_2	Activates the C section of the tens display.
11	18	B_2	Activates the B section of the tens display.
12	19	A_2	Activates the A section of the tens display.
13	20	F_2	Activates the F section of the tens display.
14	21	E_2	Activates the E section of the tens display.
15	22	D_3	Activates the D section of the hundreds display.
16	23	B_3	Activates the B section of the hundreds display.
17	24	F_3	Activates the F section of the hundreds display.
18	25	E_3	Activates the E section of the hundreds display.
19	26	AB_4	Activates both halves of the 1 in the thousands display.
20	27	POL	Activates the negative polarity display.
21	28	BP GND	LCD backplane drive output (TC7116/TC7116A). Digital ground (TC7117/TC7117A).
22	29	G_3	Activates the G section of the hundreds display.
23	30	A_3	Activates the A section of the hundreds display.
24	31	C_3	Activates the C section of the hundreds display.
25	32	G_2	Activates the G section of the tens display.
26	34	V^-	Negative power supply voltage.
27	35	V_{INT}	Integrator output. Connection point for integration capacitor. See Integration Capacitor section for additional details.
28	36	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	37	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47 µF capacitor for 200 mV full scale and a 0.047 µF capacitor for 2V full scale. See Auto-Zero Capacitor paragraph for more details.
30	38	V_{IN}^-	The analog LOW input is connected to this pin.
31	39	V_{IN}^+	The analog HIGH input is connected to this pin.
32	40	COMMON	This pin is primarily used to set the analog common-mode COMMON voltage for battery operation or in systems where the input signal is referenced to the power supply. See Analog Common paragraph for more details. It also acts as a reference voltage source.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number Normal	44-Pin Plastic Quad Flat Package Pin Number	Symbol	Description
33	41	C^-_{REF}	See pin 34.
34	42	C^+_{REF}	A 0.1 µF capacitor is used in most applications. If a large, common-mode voltage exists (e.g., the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	43	V^+	Positive power supply voltage.
36	44	V^+_{REF}	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full scale. Place 1V between pins 32 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	3	TEST	Lamp test. When pulled HIGH (to V^+), all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See Test paragraph for more details.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	7	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per sec), connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

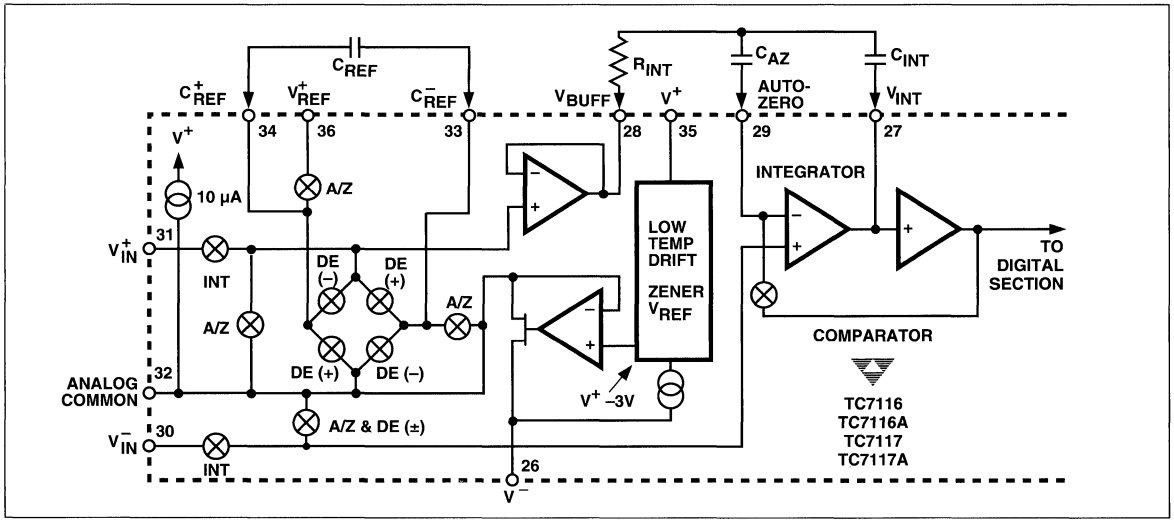


Figure 3 Analog Section of TC7116/TC7116A and TC7117/TC7117A

ANALOG SECTION
(All Pin designations refers to 40-Pin Dip)

Figure 3 shows the block diagram of the analog section for the TC7116/TC7116A and TC7117/TC7117A. Each measurement cycle is divided into three phases: (1) auto-zero (A-Z), (2) signal integrate (INT), and (3) reference integrate (REF) or deintegrate (DE).

Auto-Zero Phase

High and low inputs are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor (C_{AZ}) to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, A-Z accuracy is limited only by system noise. The offset referred to the input is less than 10 µV.

Signal-Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltages between V^+_{IN} and V^-_{IN} for a fixed time. This differential voltage can be within a wide common-mode range; 1V of either supply. However, if the input signal has no return with respect to the converter power supply, V^-_{IN} can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate, or deintegrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}} .$$

Reference

The positive reference voltage (V^+_{REF}) is referred to analog common.

Differential Input

This input can accept differential voltages anywhere within the common-mode range of the input amplifier or, specifically, from 1V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86 dB, typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to ensure that the integrator output does not saturate. A worst- case condition would be a large, positive common-mode voltage with a near full-scale negative differential input voltage. The negative-input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applica-

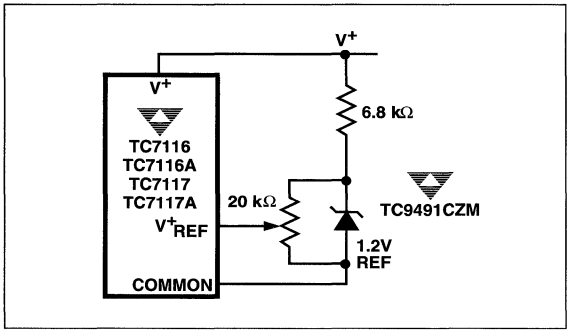


Figure 4 Using an External Reference

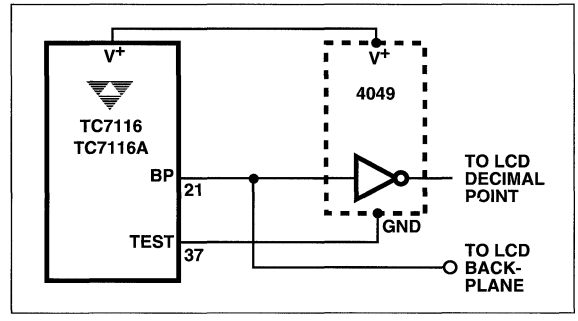


Figure 5 Simple Inverter for Fixed Decimal Point

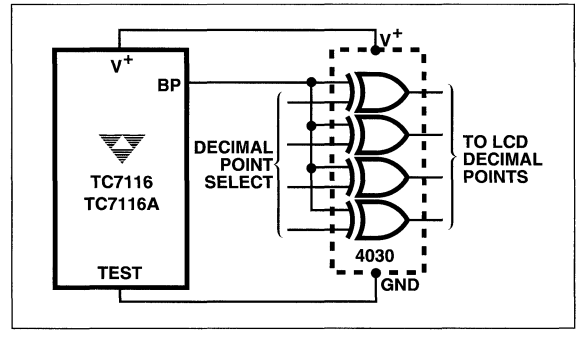


Figure 6 Exclusive "OR" Gate for Decimal Point Drive

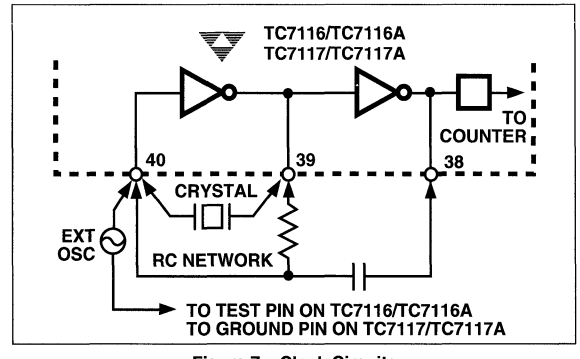


Figure 7 Clock Circuits

tions, the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TC7116/TC7116A) or for any system where the input signals are floating with respect to the power supply. The analog common pin sets a voltage approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog common has some attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the analog common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≅15Ω), and a temperature coefficient of less than 20 ppm/°C, typically, and 50 ppm maximum. The TC7116/TC7117 temperature coefficients are typically 80 ppm/°C.

An external reference may be used, if necessary, as shown in Figure 4.

Analog common is also used as $V_{\overline{IN}}$ return during auto-zero and deintegrate. If $V_{\overline{IN}}$ is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications, $V_{\overline{IN}}$ will be set at a fixed, known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage; if it can be conveniently referenced to analog common, it should be. This removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 3V below the positive supply (when a load is trying to pull the analog common line positive). However, there is only 10 μA of source current, so analog common may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin serves two functions. On the TC7117/TC7117A, it is coupled to the internally-generated digital supply through a 500Ω resistor. Thus, it can be used as a

negative supply for externally-generated segment drivers, such as decimal points or any other presentation the user may want to include on the LCD. (Figures 5 and 6 show such an application.) No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled HIGH (to V^+), all segments will be turned ON and the display should read –1888. The TEST pin will sink about 10 mA under these conditions.

DIGITAL SECTION

Figures 8 and 9 show the digital section for TC7116/TC7116A and TC7117/TC7117A, respectively. For the TC7116/TC7116A (Figure 8), an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency ÷800. For 3 readings per second, this is a 60-Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude, and are in-phase with BP when OFF, but out-of-phase when ON. In all cases, negligible DC voltage exists across the segments.

Figure 9 is the digital section of the TC7117/TC7117A. It is identical to the TC7116/TC7116A, except that the regulated supply and BP drive have been eliminated, and the segment drive is typically 8 mA. The 1000's output (pin 19) sinks current from two LED segments, and has a 16-mA drive capability. The TC7117/TC7117A are designed to drive common anode LED displays.

In both devices, the polarity indication is ON for analog inputs. If V^-_{IN} and V^+_{IN} are reversed, this indication can be reversed also, if desired.

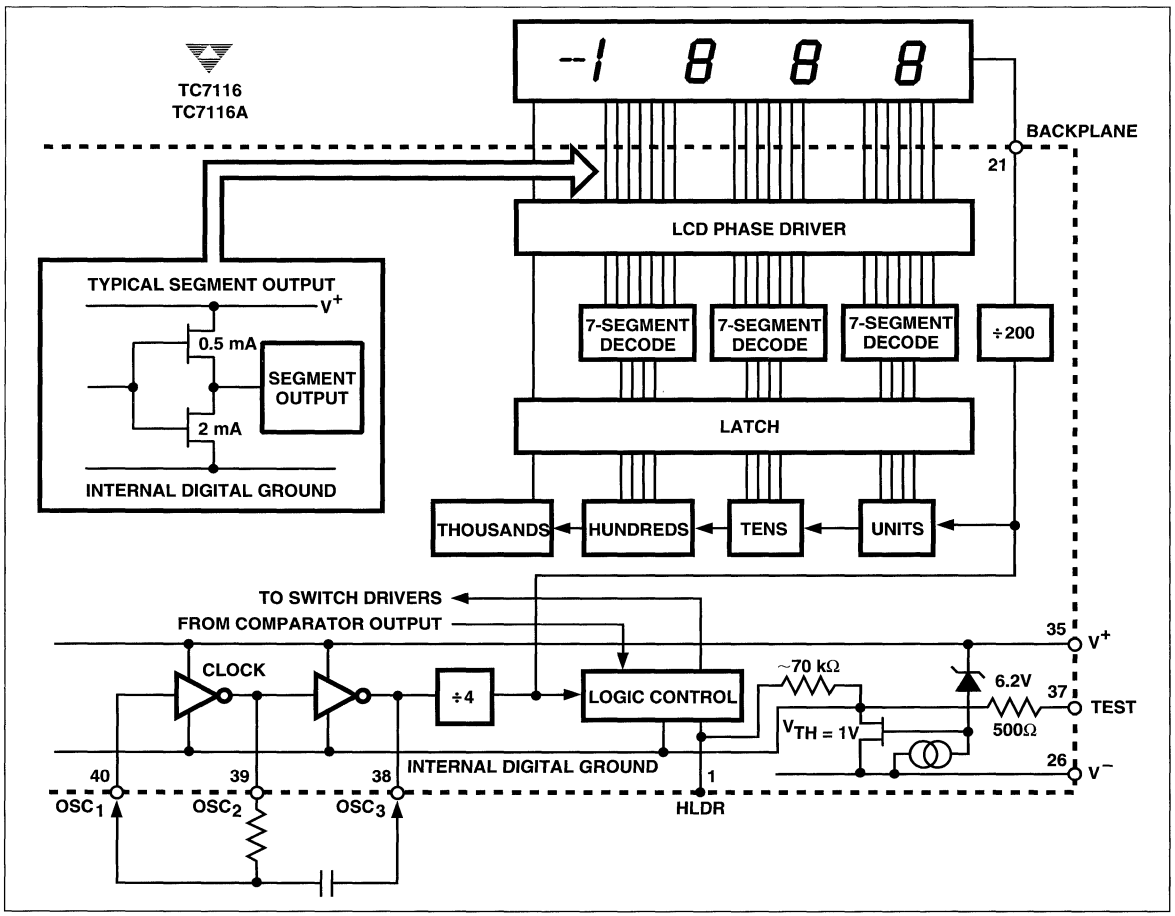


Figure 8 TC7116/TC7116A Digital Section

System Timing

The clocking method used for the TC7116/TC7116A and TC7117/TC7117A is shown in Figure 9. Three clocking methods may be used:

(1) An external oscillator connected to pin 40.
(2) A crystal between pins 39 and 40.
(3) An RC network using all three pins.

The oscillator frequency is ÷4 before it clocks the decade counters. It is then further divided to form the three convert-cycle phases: signal integrate (1000 counts), reference deintegrate (0 to 2000 counts), and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For 3 readings per second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60-Hz pickup, the signal-integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz.

HOLD Reading Input

When HLDR is at a logic HIGH the latch will not be updated. Analog-to-digital conversions will continue but will not be updated until HLDR is returned to LOW. To continuously update the display, connect to test (TC7116/TC7116A) or ground (TC7117/TC7117A), or disconnect. This input is CMOS compatible with 70 kΩ typical resistance to TEST (TC7116/TC7116A) or ground (TC7117/TC7117A).

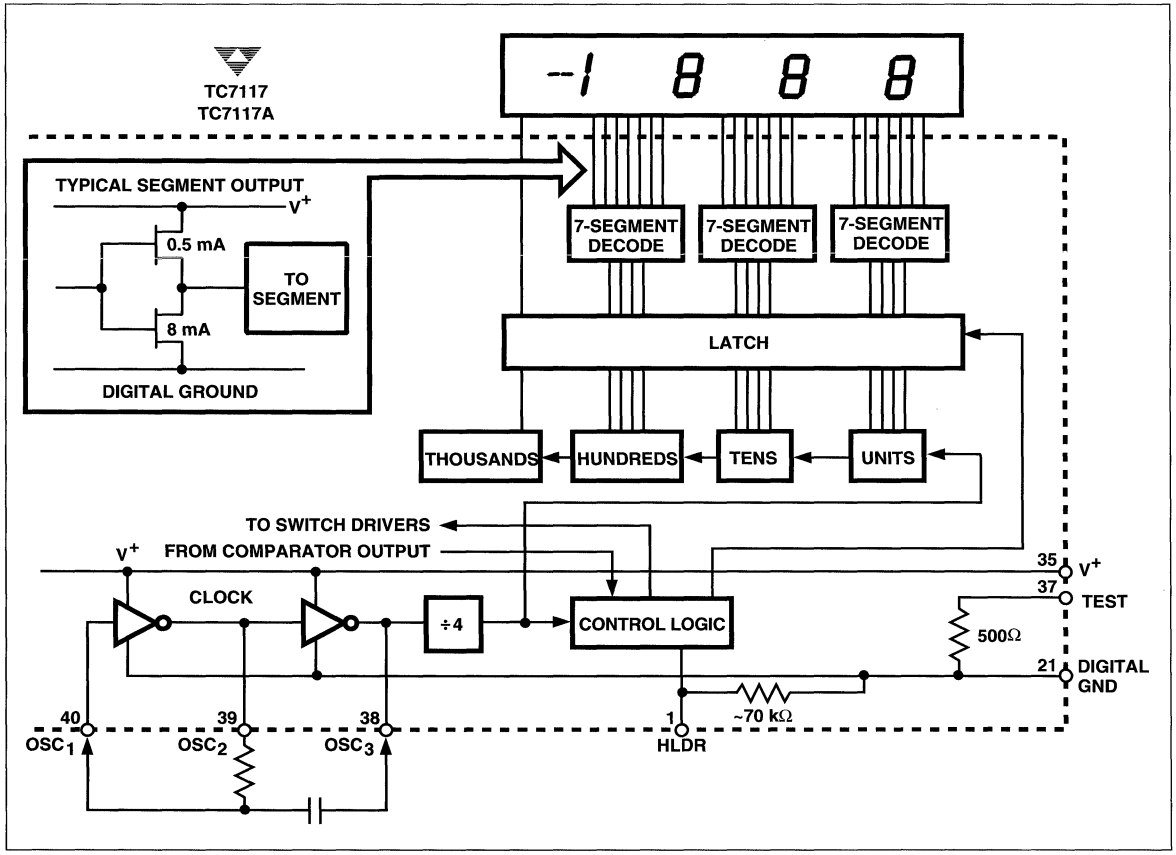


Figure 9 TC7117/TC7117A Digital Section

COMPONENT VALUE SELECTION

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on system noise. For 200 mV full scale, where noise is very important, a 0.47 μF capacitor is recommended. On the 2V scale, a 0.047 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e., the V_{IN}^- pin is not at analog common), and a 200-mV scale is used, a larger value is required to prevent roll-over error. Generally, 1 μF will hold the roll-over error to 0.5 count in this instance.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approximately 0.3V from either supply). In the TC7116/TC7116A or the TC7117/TC7117A, when the analog common is used as a reference, a nominal ±2V full- scale integrator swing is acceptable. For the TC7117/TC7117A, with ±5V supplies and analog common tied to supply ground, a ±3.5V to ±4V swing is nominal. For 3 readings per second (48 kHz clock), nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470 kΩ is near optimum and, similarly, 47 kΩ for 200 mV full scale.

Oscillator Components

For all frequency ranges, a 100-kΩ resistor is recommended; the capacitor is selected from the equation:

$$f = \frac{45}{RC}.$$

For a 48 kHz clock (3 readings per second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts), the analog input requirement is $V_{IN} = 2\ V_{REF}$. Thus, for the 200 mV and 2V scale, V_{REF} should equal 100 mV and 1V, respectively. In many applications, where the ADC is connected to a transducer, a scale factor exists between the input voltage and the digital reading. For instance, in a measuring system the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TC7117/TC7117A, with ±5V supplies, can accept input signals up to ±4V. Another advantage of this system is when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^+ and analog common, and the variable (or fixed) offset voltage between analog common and V_{IN}^-.

TC7117/TC7117A POWER SUPPLIES

The TC7117/TC7117A are designed to operate from ±5V supplies. However, if a negative supply is not available, it can be generated with a TC7660 DC-to-DC converter and two capacitors. Figure 10 shows this application.

In selected applications, a negative supply is not required. The conditions for using a single +5V supply are:

(1) The input signal can be referenced to the center of the common-mode range of the converter.
(2) The signal is less than ±1.5V.
(3) An external reference is used.

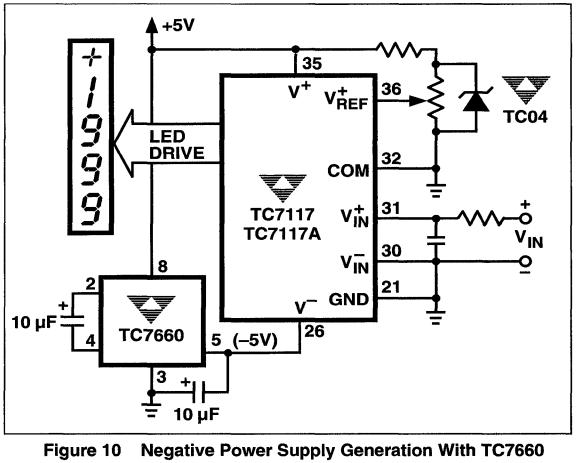


Figure 10 Negative Power Supply Generation With TC7660

TYPICAL APPLICATIONS

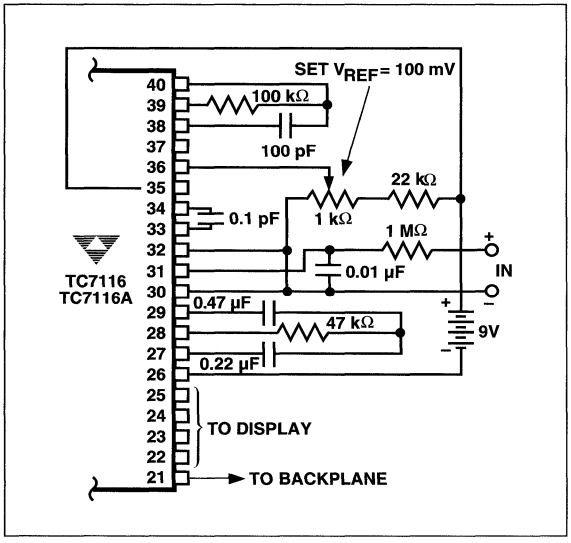


Figure 11 TC7116/TC7116A Using the Internal Reference (200 mV Full Scale, 3 Readings Per Second (RPS)

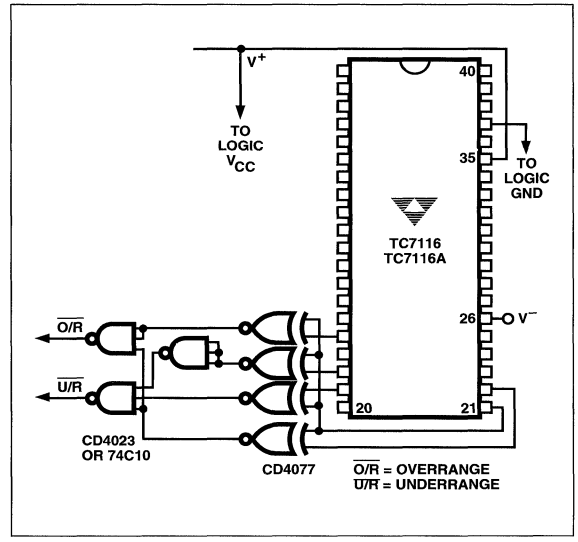


Figure 13 Circuit for Developing Underrange and Overrange Signals from TC7116/TC7116A Outputs

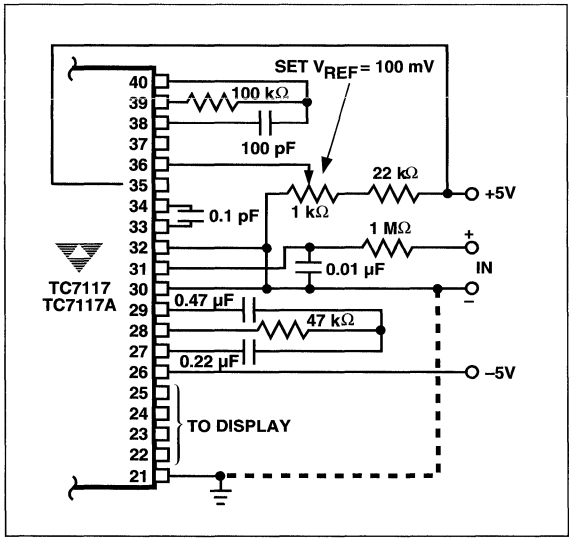


Figure 12 TC7117/TC7117A Internal Reference (200 mV Full Scale, 3 RPS, $V_{\overline{IN}}$ Tied to GND for Single-Ended Inputs.)

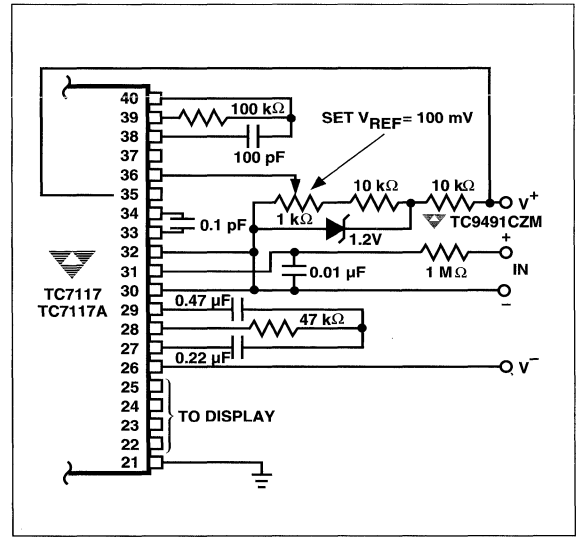


Figure 14 TC7117/TC7117A With a 1.2V External Band-Gap Reference ($V_{\overline{IN}}$ Tied to Common)

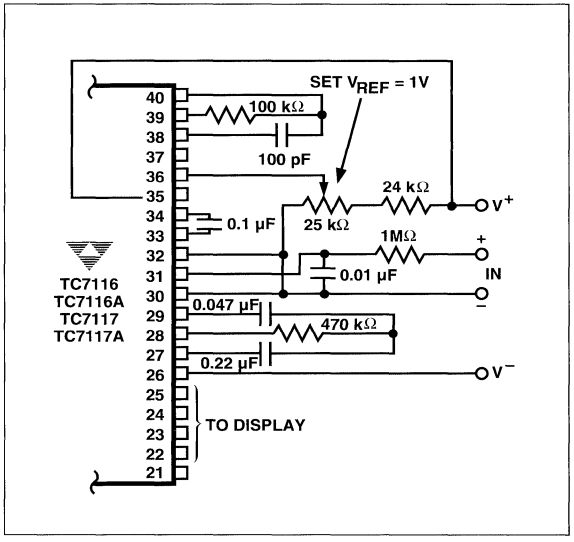


Figure 15 Recommended Component Values for 2V Full Scale (TC7116/TC7116A and TC7117/TC7117A)

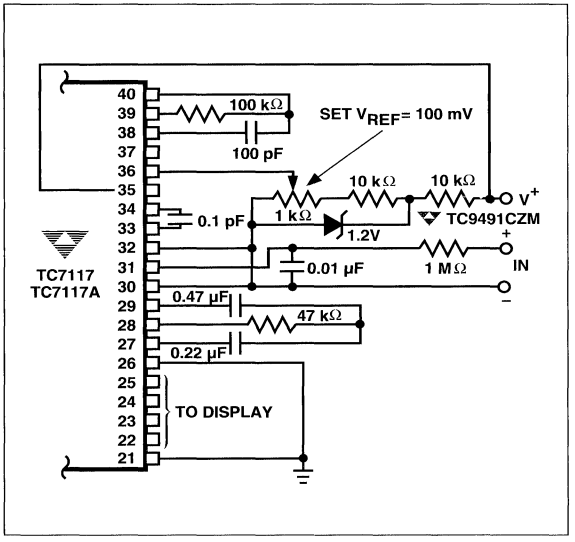


Figure 16 TC7117/TC7117A Operated from Single +5V Supply (An External Reference Must Be Used in This Application.)

APPLICATIONS INFORMATION

The TC7117/TC7117A sink the LED display current, causing heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing the LED common anode voltage, the TC7117/TC7117A package power dissipation is reduced.

Figure 17 is a curve-tracer display showing the relationship between output current and output voltage for typical TC7117CPL/TC7117ACPL devices. Since a typical LED has 1.8V across it at 8 mA and its common anode is connected to +5V, the TC7117/TC7117A output is at 3.2V (Point A, Figure 17). Maximum power dissipation is 8.1 mA × 3.2V × 24 segments = 622 mW.

However, notice that once the TC7117/TC7117A's output voltage is above 2V, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7V (Point B Figure 17) results in 7.7 mA of LED current, only a 5% reduction. Maximum power dissipation is now only 7.7 mA × 2.5V × 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1V (Point C) reduces LED current by 10% (7.3 mA), but power dissipation by 38% (7.3 mA × 2.2V × 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Figure 18 shows two ways: Either a 5.1Ω, 1/4W resistor, or a 1A diode placed in series with the display (but not in series with the TC7117/TC7117A). The resistor reduces the TC7117/TC7117A's output voltage (when all 24 segments are ON) to Point C of Figure 17. When segments turn off, the output voltage will increase. The diode, however, will result in a relatively steady output voltage, around Point B.

In addition to limiting maximum power dissipation, the resistor reduces change in power dissipation as the display changes. The effect is caused by the fact that, as fewer segments are ON, each ON output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display), the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

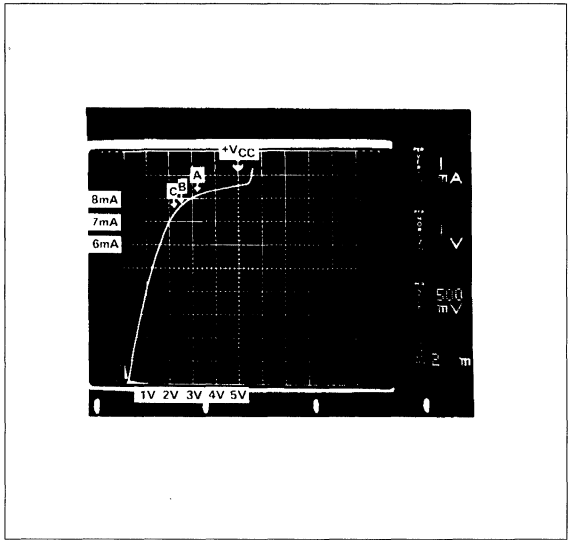


Figure 17 TC7117/TC7117A Output Current vs Output Voltage

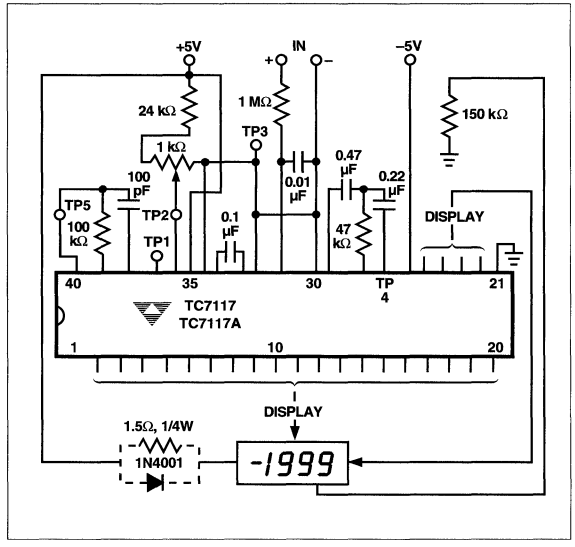


Figure 18 Diode or Resistor Limits Package Power Dissipation

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

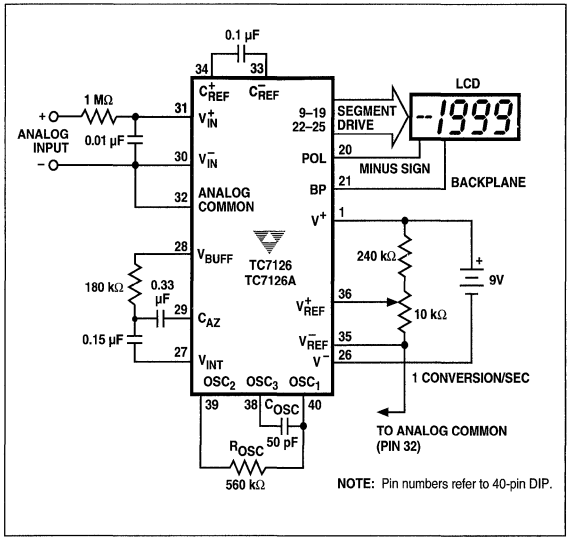
FEATURES

- **Low Temperature Drift Internal Reference**
  TC7126 ..... 80 ppm/°C Typ
  TC7126A ..... 35 ppm/°C Typ
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise ..... 15 μV_{P-P}**
- **High Resolution 0.05%**
- **Low Input Leakage Current ..... 1 pA Typ**
  10 pA Max
- **Precision Null Detectors With True Polarity at Zero**
- **High-Impedance Differential Input**
- **Convenient 9V Battery Operation With Low Power Dissipation ..... 500 μW Typ**
  900 μW Max

TYPICAL APPLICATIONS

- **Thermometry**
- **Bridge Readouts: Strain Gauges, Load Cells, Null Detectors**
- **Digital Meters and Panel Meters**
  — Voltage/Current/Ohms/Power, pH
- **Digital Scales, Process Monitors**

TYPICAL OPERATING CIRCUIT



NOTE: Pin numbers refer to 40-pin DIP.

GENERAL DESCRIPTION

The TC7126A is a 3-1/2 digit CMOS analog-to-digital converter (ADC) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, digit and polarity drivers, voltage reference, and clock circuit are integrated on-chip. The TC7126A directly drives a liquid crystal display (LCD), and includes a backplane driver.

A low-cost, high-resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7126A's extremely low power drain and 9V battery operation make it ideal for portable applications.

The TC7126A reduces linearity error to less than 1 count. Roll-over error (the difference in readings for equal magnitude but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading, and the auto-zero cycle guarantees a zero display reading with a 0V input.

The TC7126A features a precision, low-drift internal voltage reference and is functionally identical to the TC7126. A low-drift external reference is not normally required with the TC7126A.

ORDERING INFORMATION

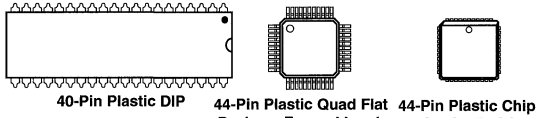
PART CODE **TC7126X X XXX**

A or blank* —— **R (reversed pins) or blank (CPL pkg only)** —— * "A" parts have an improved reference TC

Package Code (see below): ——

Package Code	Package	Temperature Range
CPL	40-Pin PDIP	0°C to +70°C
IPL	40-Pin PDIP (non-A only)	– 25°C to +85°C
CLW	44-Pin PLCC	0°C to +70°C
CKW	44-Pin PQFP	0°C to +70°C

AVAILABLE PACKAGES



40-Pin Plastic DIP — 44-Pin Plastic Quad Flat Package Formed Leads — 44-Pin Plastic Chip Carrier PLCC

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) ..... +15V
Analog Input Voltage (Either Input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Either Input) ..... V^+ to V^-
Clock Input ..... TEST to V^+
Operating Temperature Range
C Devices ..... 0°C to +70°C
I Devices ..... – 25°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Power Dissipation (Note 2)
CerDIP (J) ..... 1000 mW
Plastic DIP (P) ..... 800 mW
Plastic Quad Flat Package, PLCC (B, K, L) .. 500 mW

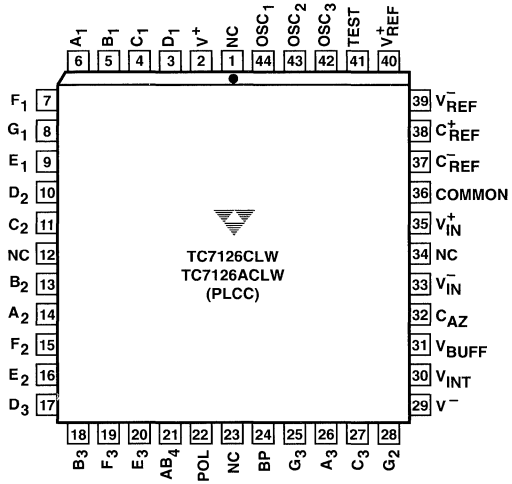
*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

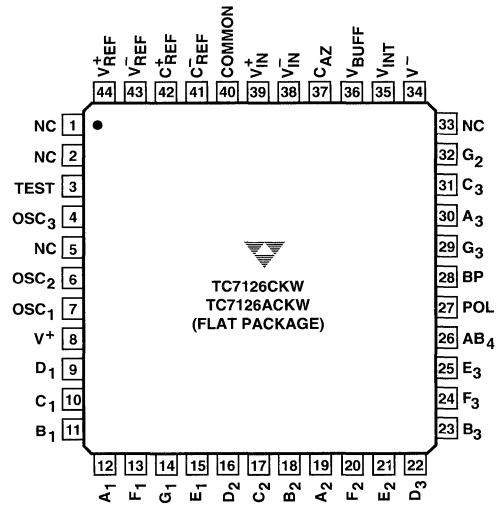
ELECTRICAL CHARACTERISTICS: V_S = +9V, f_{CLK} = 16 kHz, and T_A = +25°C, unless otherwise noted.

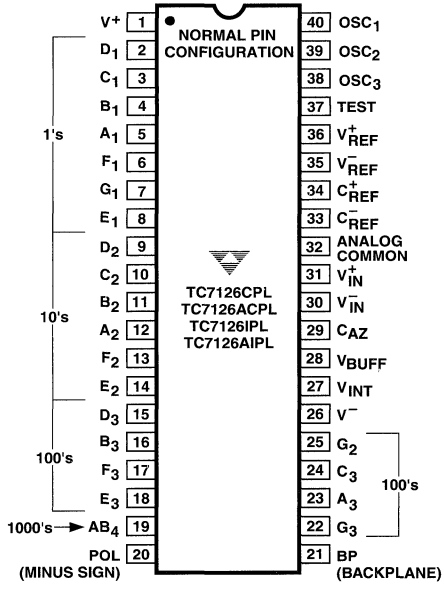
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	–000.0	±000.0	+000.0	Digital Reading
	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C	—	0.2	1	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
NL	Linearity Error	Full Scale = 200 mV or 2V Max Deviation From Best Fit Straight Line	– 1	±0.2	1	Count
	Roll-Over Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200 mV	– 1	±0.2	1	Count
e_N	Noise	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200 mV	—	50	—	µV/V
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C ≤ T_A ≤ +70°C Ext Ref Temp Coeff = 0 ppm/°C	—	1	5	ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ +70°C ("C" Devices): TC7126 TC7126A – 25°C ≤ T_A ≤ +85°C ("I" Device): TC7126A	 — — —	 80 35 35	 — 75 100	 ppm/°C ppm/°C ppm/°C
V_C	Analog Common Voltage	250 kΩ Between Common and V^+	2.7	3.05	3.35	V
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_S	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V (Note 6)	—	55	100	µA

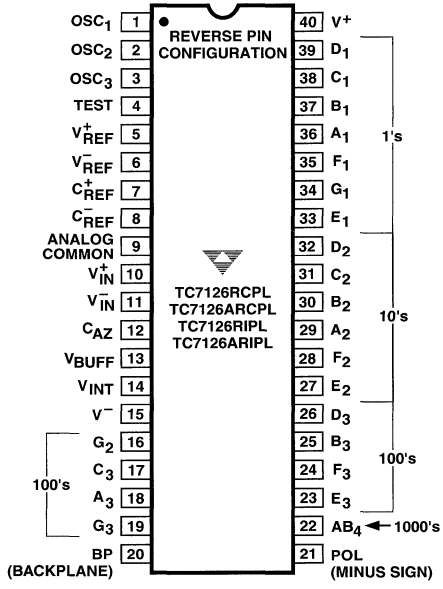
NOTES:
1. Input voltage may exceed supply voltages when input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "OFF" segment and 180° out-of-phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
5. See "Typical Operating Circuit."
6. During auto-zero phase, current is 10–20 µA higher. A 48 kHz oscillator increases current by 8 µA (typical). Common current not included.

PIN CONFIGURATIONS









NC = NO INTERNAL CONNECTION

PIN DESCRIPTION

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
1	(40)	V^+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP	Backplane drive output.
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V^-	Negative power supply voltage.
27	(14)	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build-up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 µF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See "Integrating Capacitor" section for additional details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 180 kΩ resistor for a 200 mV full-scale range and a 1.8 MΩ resistor for a 2V full-scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.33 µF capacitor for 200 mV full scale, and a 0.033 µF capacitor for 2V full scale. See paragraph on auto-zero capacitor for more details.
30	(11)	V_{IN}^-	The low input signal is connected to this pin.
31	(10)	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on analog common for more details. It also acts as a reference voltage source.
33	(8)	C_{REF}^-	See pin 34.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
34	(7)	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	V_{REF}^-	See pin 36.
36	(5)	V_{REF}^+	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on reference voltage.
37	(4)	TEST	Lamp test. When pulled HIGH (to V^+), all segments will be turned ON and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under test for additional information.
38	(3)	OSC_3	See pin 40.
39	(2)	OSC_2	See pin 40.
40	(1)	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per second), connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

GENERAL THEORY OF OPERATION

(All Pin Designations Refer to the 40-Pin DIP)

Dual-Slope Conversion Principles

The TC7126A is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7126A operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period (t_{SI}), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (t_{RI}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

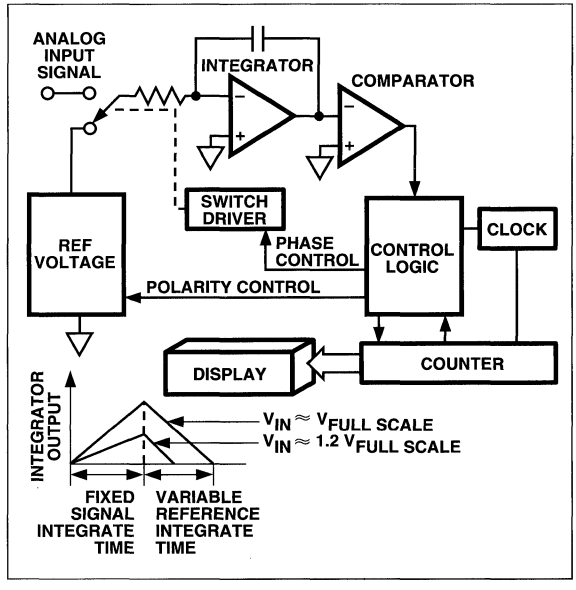


Figure 1 Basic Dual-Slope Converter

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

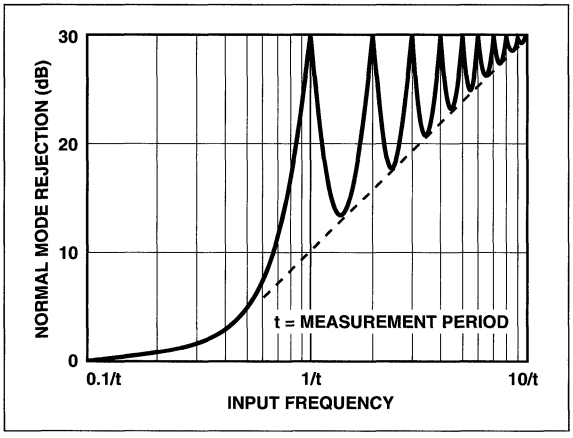


Figure 2 Normal-Mode Rejection of Dual-Slope Converter

For a constant V_{IN}:

$$V_{IN} = V_R \left[\frac{t_{RI}}{t_{SI}}\right].$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period.

ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three phases:

(1) Auto-zero phase
(2) Signal integrate phase
(3) Reference integrate phase

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 μV to 15 μV.

The auto-zero cycle length is 1000 to 3000 clock periods.

Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TC7126A signal integration period is 1000 clock periods, or counts. The externally-set clock frequency is ÷4 before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Phase

The third phase is reference integrate, or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is:

$$1000 \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency ÷800. For 3 conversions per second the backplane frequency is 60 Hz with a 5V nominal amplitude.

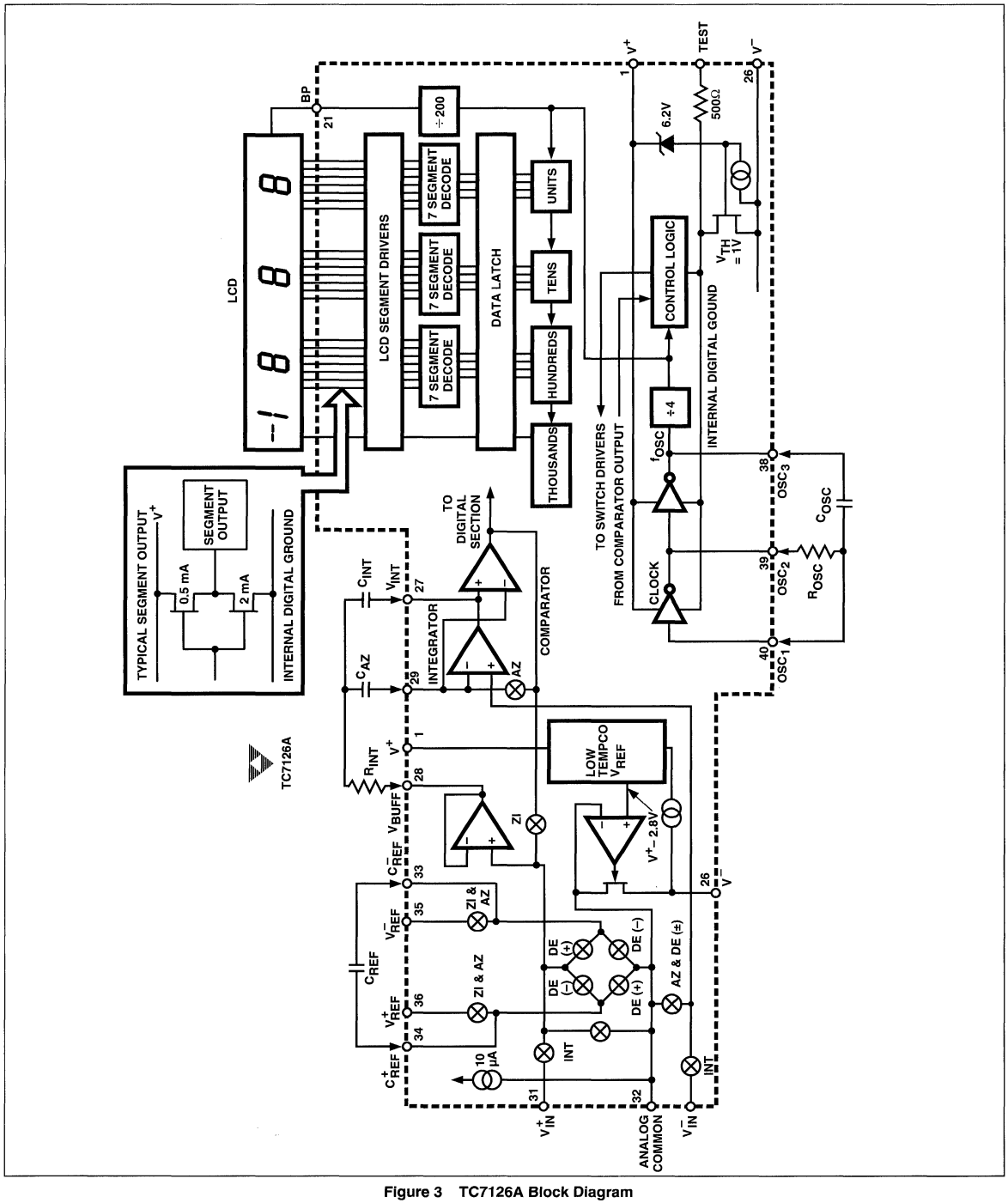


Figure 3 TC7126A Block Diagram

When a segment driver is in-phase with the backplane signal, the segment is OFF. An out-of-phase segment drive signal causes the segment to be ON, or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed, this indicator would reverse.

On the TC7126A, when the TEST pin is pulled to V^+, all segments are turned ON. The display reads –1888. During this mode, LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES; LCDS MAY BE DESTROYED IF OPERATED WITH DC LEVELS FOR EXTENDED PERIODS.

The display font and segment drive assignment are shown in Figure 4.

System Timing

The oscillator frequency is ÷4 prior to clocking the internal decade counters. The three-phase measurement cycle takes a total of 4000 counts (16,000 clock pulses). The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 1000 to 3000 counts
(4000 to 12,000 clock pulses)
For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period.

(2) Signal integrate: 1000 counts
(4000 clock pulses)
This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right],$$

where f_{OSC} is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts
(0 to 8000 clock pulses)

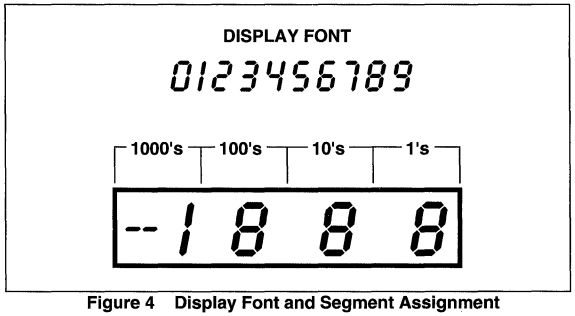


Figure 4 Display Font and Segment Assignment

The TC7126A is a drop-in replacement for the TC7126 and ICL7126 that offers a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

COMPONENT VALUE SELECTION

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} size has some influence on system noise. A 0.33 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.033 µF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage, used to ramp the integrator output voltage back to zero during the reference integrate phase, is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 µF. Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7126A's superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second (f_{OSC} = 48 kHz), a 0.047 µF value is suggested. For 1 reading per second, 0.15 µF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

At 3 readings per second, a 750Ω resistor should be placed in series with C_{INT}. This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 µA. The integrator and buffer can supply 1 µA drive current with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 kΩ. A 2V full scale requires 1.8 MΩ.

Component Value	Nominal Full-Scale Voltage 200 mV	2V
C_{AZ}	0.33 µF	0.033 µF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 µF	0.047 µF

NOTE: f_{OSC} = 48 kHz (3 readings per sec).

Oscillator Components

C_{OSC} should be 50 pF; R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}.$$

For a 48 kHz clock (3 conversions per second), R = 180 kΩ.

Note that f_{OSC} is ÷4 to generate the TC7126A's internal clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*$V_{FS} = 2\ V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used where a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature-measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

2

DEVICE PIN FUNCTIONAL DESCRIPTION

(Pin Numbers Refer to 40-Pin DIP)

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC7126A is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). Typical range is V^+ –1V to V^- +1V. Common-mode voltages are removed from the system when the TC7126A operates from a battery or floating power source (isolated from measured system), and V_{IN}^- is connected to analog common (V_{COM}). (See Figure 5.)

In systems where common-mode voltages exist, the TC7126A's 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 6.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

The TC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C for the TC7126A and 80 ppm/°C for the TC7126.

ANALOG COMMON (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. Analog common is tied internally to an N-channel FET capable of sinking 100 µA. This FET will hold the common line at 3V should an

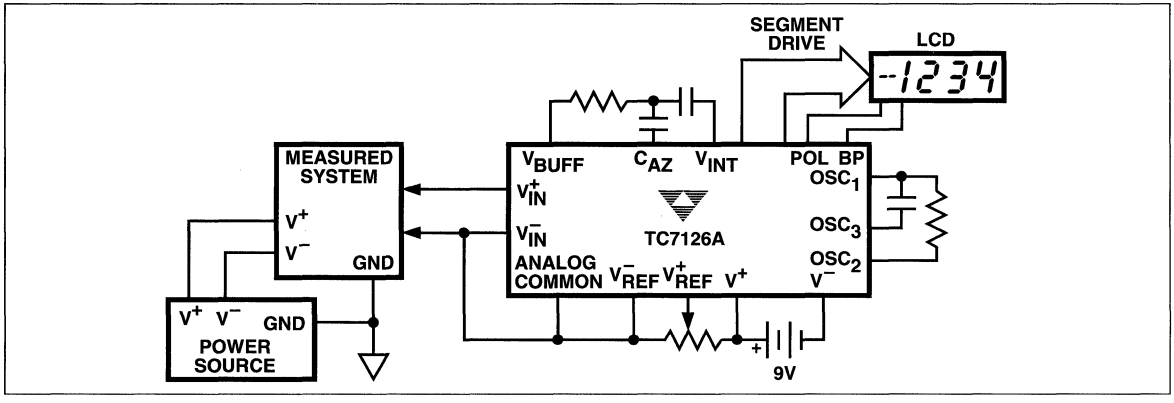


Figure 5 Common-Mode Voltage Removed in Battery Operation With V_{IN} = Analog Common

external load attempt to pull the common line toward V+. Analog common source current is limited to 1 µA. Therefore, analog common is easily pulled to a more negative voltage (i.e., below V+ –3V).

The TC7126A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero phase. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists, but is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference, or common point. The TC7126A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7126A's power source. The analog common potential of V+ –3V gives a 7V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15Ω output impedance.

With sufficiently high total supply voltage (V+–V− >7V), analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°c). This potential can be used to generate the TC7126A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See "TC7126A Internal Voltage Reference" discussion.

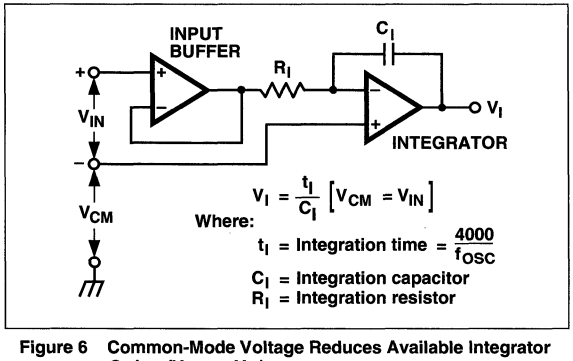


Figure 6 Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

TEST (Pin 37)

The TEST pin potential is 5V less than V+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The TEST pin load should not be more than 1 mA. See "Digital Section" for additional information on using TEST as a negative digital logic supply.

If TEST is pulled HIGH (to V+), all segments plus the minus sign will be activated. DO NOT OPERATE IN THIS MODE FOR MORE THAN SEVERAL MINUTES. With TEST= V+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

TC7126A Internal Voltage Reference

The TC7126A's analog common voltage temperature stability has been significantly improved (Figure 7). The "A" version of the industry-standard TC7126 device allows users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 10 shows analog common supplying the necessary voltage reference for the TC7126A.

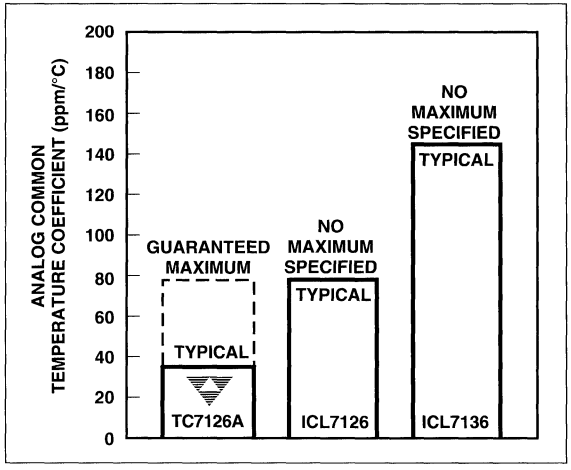


Figure 7 Analog Common Temperature Coefficient

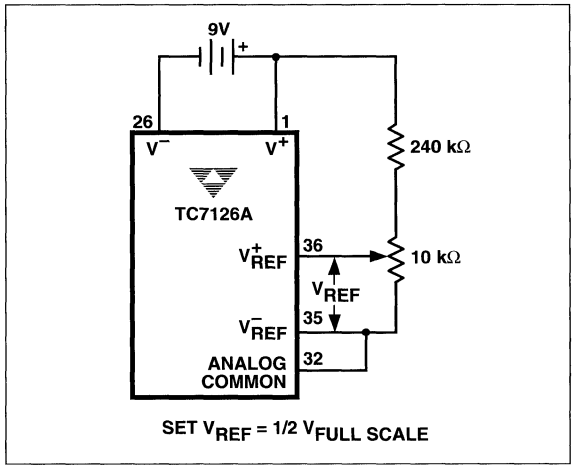


Figure 8 TC7126A Internal Voltage Reference Connection

APPLICATIONS INFORMATION

Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7126A 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	I1048, I1126
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the TEST pin: its potential is approximately 5V below V^+.

Flat Package

The TC7126A is available in an epoxy 64-pin formed-lead flat package. A test socket for the TC7126ACBQ device is available:

Part No. IC 51-42
Manufacturer: Yamaichi
Distribution: Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94043
(415) 856-9332

Ratiometric Resistance Measurements

The TC7126A's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

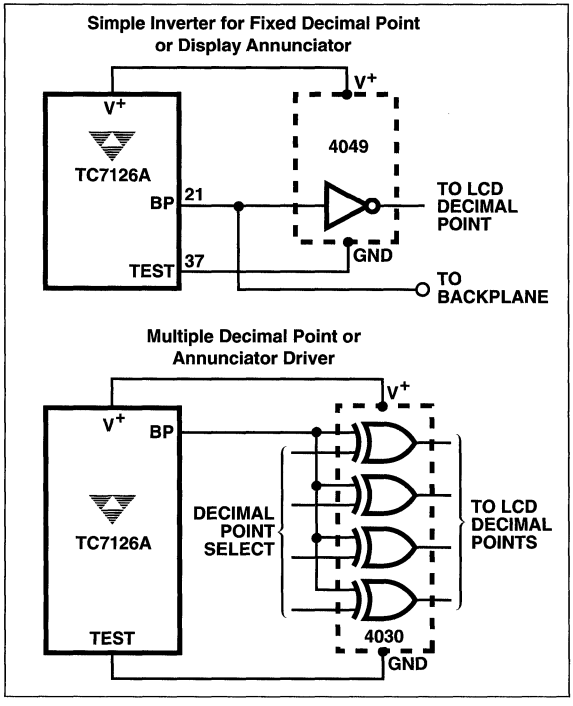


Figure 9 Decimal Point and Annunciator Drives

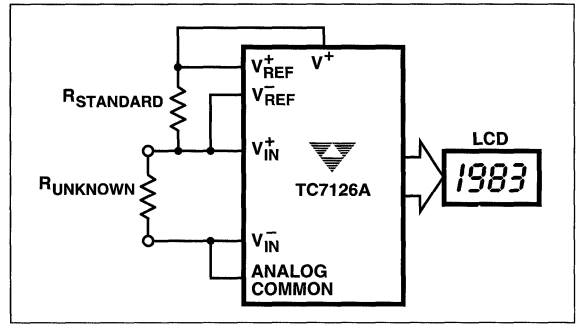


Figure 10 Low Parts Count Ratiometric Resistance Measurement

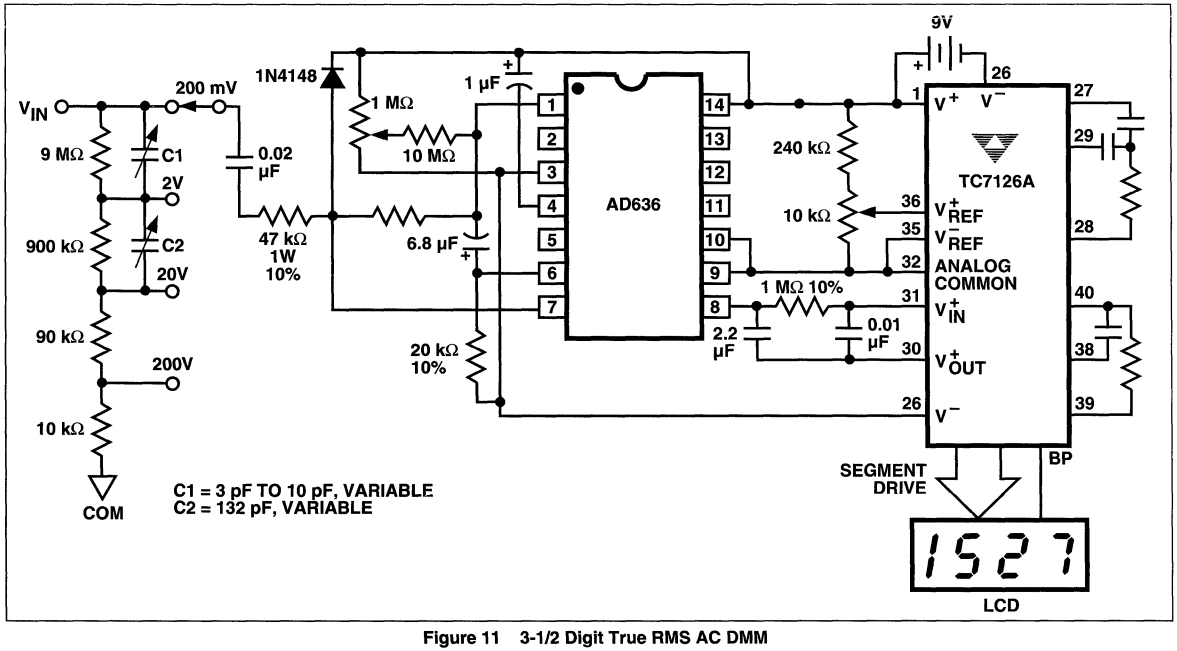


Figure 11 3-1/2 Digit True RMS AC DMM

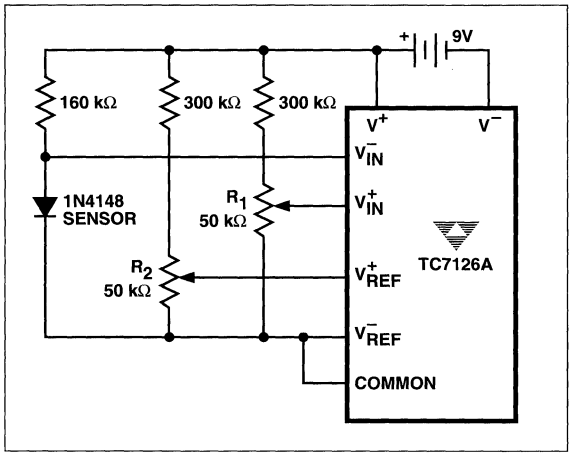


Figure 12 Temperature Sensor

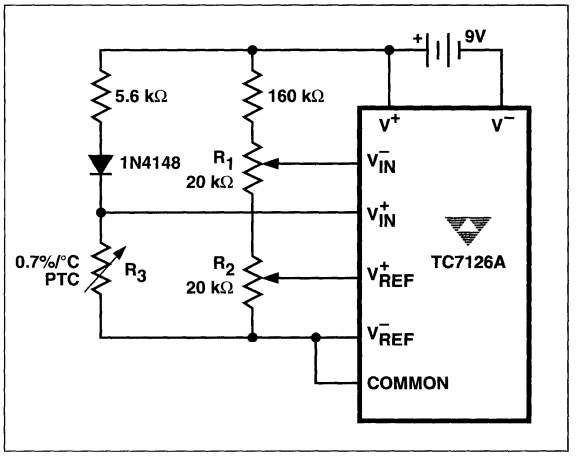


Figure 13 Positive Temperature Coefficient Resistor Temperature Sensor

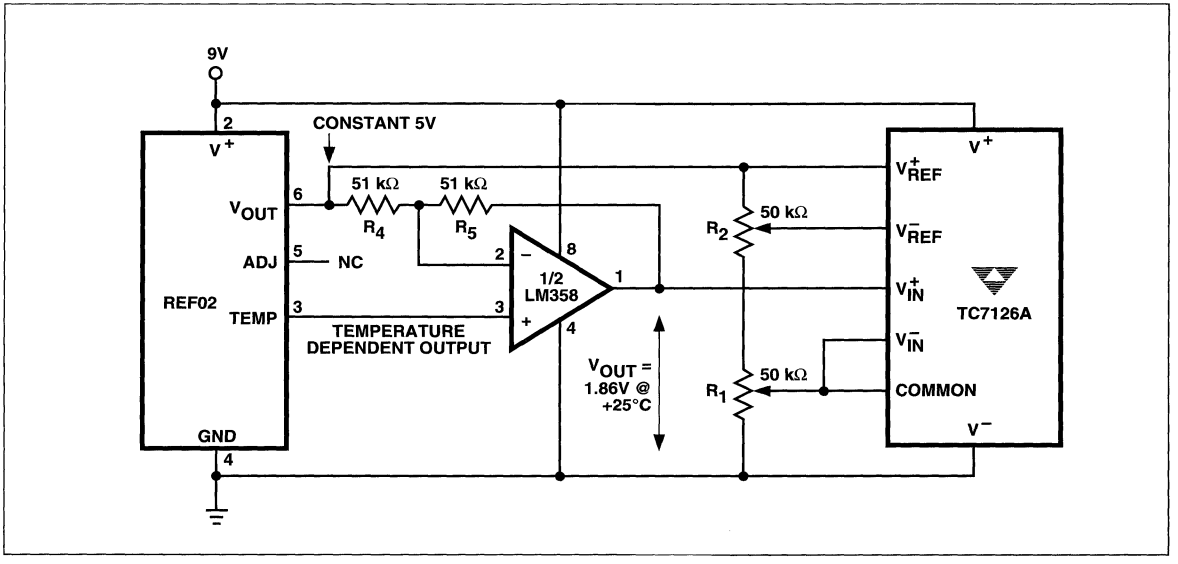


Figure 14 Integrated Circuit Temperature Sensor

4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER WITH ON-CHIP LCD DRIVERS

FEATURES

- **Count Resolution ..... ±19,999**
- **Resolution on 200 mV Scale ..... 10 µV**
- **True Differential Input and Reference**
- **Low Power Consumption ..... 500 µA at 9V**
- **Direct LCD Driver for 4-1/2 Digits, Decimal Points, Low-Battery Indicator, and Continuity Indicator**
- **Overrange and Underrange Outputs**
- **Range Select Input 10:1**
- **High Common-Mode Rejection Ratio ..... 110 dB**
- **External Phase Compensation Not Required**

ORDERING INFORMATION

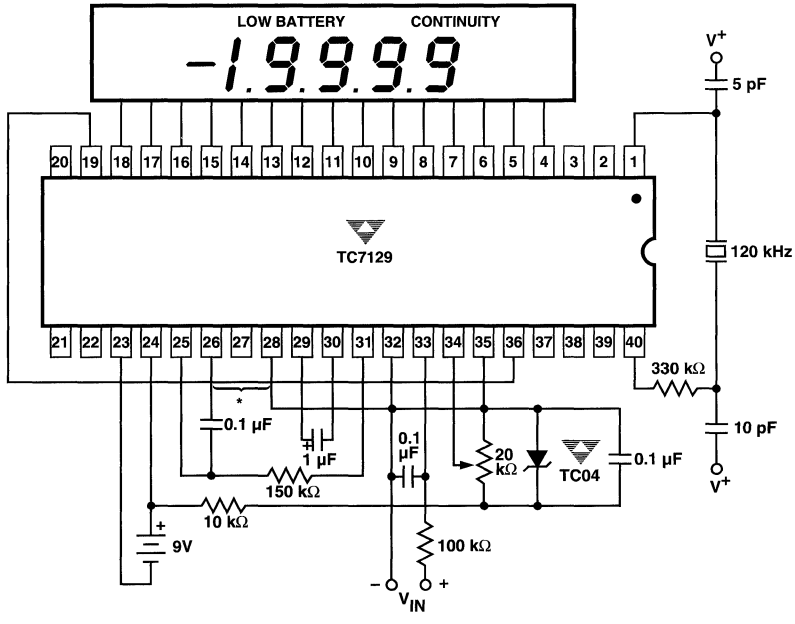
Part No.	Pin Layout	Package	Temperature Range
TC7129CPL	Normal	40-Pin PDIP	0°C to +70°C
TC7129CKW	Formed	44-Pin PQFP	0°C to +70°C
TC7129CLW	—	44-Pin PLCC	0°C to +70°C

GENERAL DESCRIPTION

The TC7129 is a 4-1/2 digit analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Fabricated in high-performance, low-power CMOS, the TC7129 ADC is designed specifically for high-resolution, battery-powered digital multimeter applications. The traditional dual-slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full scale, and resolution down to 10 µV per count.

The TC7129 includes features important to multimeter applications. It detects and indicates low-battery condition. A continuity output drives an annunciator on the display, and can be used with an external driver to sound an audible alarm. Overrange and underrange outputs and a range-change input provide the ability to create auto-ranging instruments. For snapshot readings, the TC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TC7129 the ideal choice for full-featured multimeter and digital measurement applications.

TYPICAL OPERATING CIRCUIT



* **NOTE:** RC network between pins 26 and 28 is not required.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (IN HI or IN LO) (Note 1) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND –0.3V
Digital Input, Pins
1, 2, 19, 20, 21, 22, 27, 37, 39, 40 ..... DGND to V^+
Analog Input, Pins 25, 29, 30 ..... V^+ to V^-
Power Dissipation Plastic Package (Note 2) ..... 800 mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

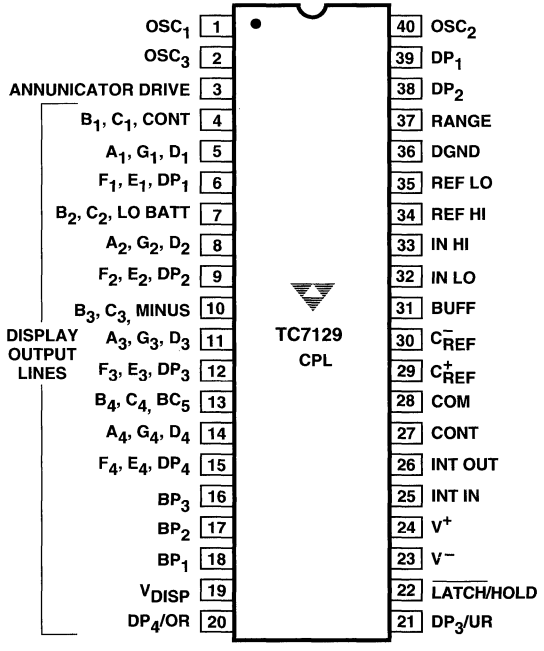
Notes: Input voltages may exceed supply voltages, provided input current is limited to ±400 µA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

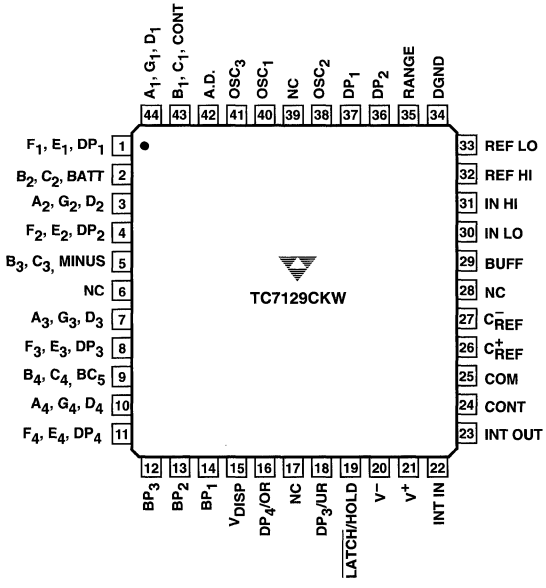
ELECTRICAL CHARACTERISTICS:

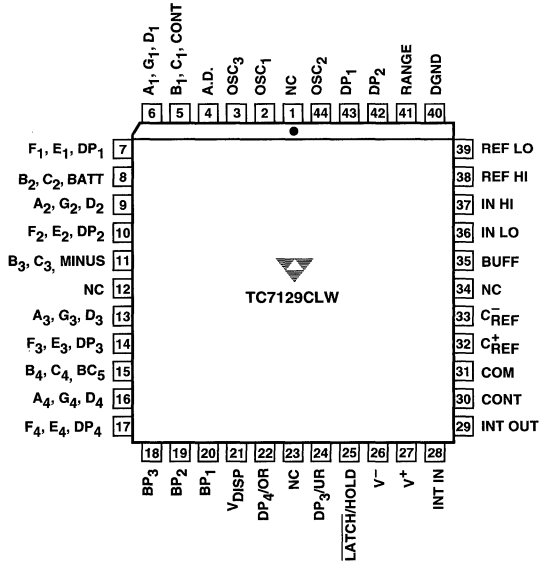
V^+ to V^- = 9V, V_{REF} = 1V, T_A = +25°C, f_{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V, 200 mV Scale	–0000	0000	+0000	Counts
	Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C	—	±0.5	—	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF} = 1000 mV, Range = 2V	9997	9999	10000	Counts
	Range Change Accuracy	V_{IN} = 0.1V on Low Range ÷V_{IN} = 1V on High Range	0.9999	1.0000	1.0001	Ratio
RE	Roll-Over Error	–V_{IN} = +V_{IN} = 199 mV	—	1	2	Counts
NL	Linearity Error	200 mV Scale	—	1	—	Counts
CMRR	Common-Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, 200 mV Scale	—	110	—	dB
CMVR	Common-Mode Voltage Range	V_{IN} = 0V 200 mV Scale	— —	(V^-) +1.5 (V^+) –1	— —	V V
e_N	Noise (Peak-to-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V 200 mV Scale	—	14	—	μV_{P-P}
I_{IN}	Input Leakage Current	V_{IN} = 0V, Pins 32, 33	—	1	10	pA
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C < T_A < +70°C External V_{REF} = 0 ppm/°C	—	2	7	ppm/°C
Power						
V_{COM}	Common Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
	Common Sink Current Common Source Current	ΔCommon = +0.1V ΔCommon = –0.1V	— —	0.6 10	— —	mA µA
DGND	Digital Ground Voltage	V^+ to Pin 36, V^+ to V^- = 9V	4.5	5.3	5.8	V
	Sink Current	ΔDGND = +0.5V	—	1.2	—	mA
	Supply Voltage Range	V^+ to V^-	6	9	12	V
I_S	Supply Current Excluding Common Current	V^+ to V^- = 9V	—	0.5	1	mA
f_{CLK}	Clock Frequency		—	120	360	kHz
	V_{DISP} Resistance	V_{DISP} to V^+	—	50	—	kΩ
	Low-Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
Digital						
	Continuity Comparator Threshold Voltages	V_{OUT} Pin 27 = High V_{OUT} Pin 27 = Low	100 —	200 200	— 400	mV mV
	Pull-Down Current	Pins 37, 38, 39	—	2	10	µA
	"Weak Output" Current Sink/Source	Pins 20, 21 Sink/Source Pin 27 Sink/Source	— —	3/3 3/9	— —	µA µA
	Pin 22 Source Current Pin 22 Sink Current		— —	40 3	— —	µA µA

PIN CONFIGURATIONS







PIN DESCRIPTIONS

40-Pin DIP Pin Number Normal	Name	Function
1	OSC_1	Input to first clock inverter.
2	OSC_3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane square-wave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP_3	Backplane #3 output to display.
17	BP_2	Backplane #2 output to display.
18	BP_1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	Input: When HI, turns on most significant decimal point. Output: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	Input: Second most significant decimal point on when HI. Output: Pulled HI when result count is less than ±1000.
22	LATCH/HOLD	Input: When floating, ADC operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the deintegrate phase of cycle. Output: Negative-going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	Input: When LO, continuity flag on the display is OFF. When HI, continuity flag is ON. Output: HI when voltage between inputs is less than +200 mV. LO when voltage between inputs is more than +200 mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as preregulator for external reference.
29	C_{REF}^+	Positive side of external reference capacitor.
30	C_{REF}^-	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.

PIN DESCRIPTIONS

40-Pin DIP Pin Number Normal	Name	Function
36	DGND	Internal ground reference for digital section. See "±5V Power Supply" paragraph.
37	RANGE	3 μA pull-down for 200 mV scale. Pulled HI externally for 2V scale.
38	DP_2	Internal 3 μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3 μA pull-down. When HI, decimal point 1 will be on.
40	OSC_2	Output of first clock inverter. Input of second clock inverter.

COMPONENT SELECTION

(All pin designations refer to 40-Pin Dip)

The TC7129 is designed to be the heart of a high-resolution analog measurement instrument. The only additional components required are a few passive elements, a voltage reference, an LCD, and a power source. Most component values are not critical; substitutes can be chosen based on the information given below.

The basic circuit for a digital multimeter application is shown in Figure 1. See "Special Applications" for variations. Typical values for each component are shown. The sections below give component selection criteria.

Oscillator (X_{OSC}, C_{O1}, C_{O2}, R_O)

The primary criterion for selecting the crystal oscillator is to chose a frequency that achieves maximum rejection of line-frequency noise. To do this, the integration phase should last an integral number of line cycles. The integration phase of the TC7129 is 10,000 clock cycles on the 200 mV range and 1000 clock cycles on the 2V range. One clock cycle is equal to two oscillator cycles. For 60 Hz rejection, the oscillator frequency should be chosen so that the period of one line cycle equals the integration time for the 2V range:

$$1/60 \text{ second} = 16.7 \text{ ms} = \frac{1000 \text{ clock cycles} * 2 \text{ osc cycles/clock cycle}}{\text{oscillator frequency}},$$

giving an oscillator frequency of 120 kHz. A similar calculation gives an optimum frequency of 100 kHz for 50 Hz rejection.

The resistor and capacitor values are not critical; those shown work for most applications. In some situations, the capacitor values may have to be adjusted to compensate for parasitic capacitance in the circuit. The capacitors can be low-cost ceramic devices.

Some applications can use a simple RC network instead of a crystal oscillator. The RC oscillator has more potential for jitter, especially in the least significant digit. See "RC Oscillator."

Integrating Resistor (R_{INT})

The integrating resistor sets the charging current for the integrating capacitor. Choose a value that provides a current between 5 μA and 20 μA at 2V, the maximum full-scale input. The typical value chosen gives a charging current of 13.3 μA:

$$I_{CHARGE} = \frac{2V}{150\ k\Omega} 13.3\ \mu A$$

Too high a value for R_{INT} increases the sensitivity to noise pickup and increases errors due to leakage current. Too low a value degrades the linearity of the integration, leading to inaccurate readings.

TC7129

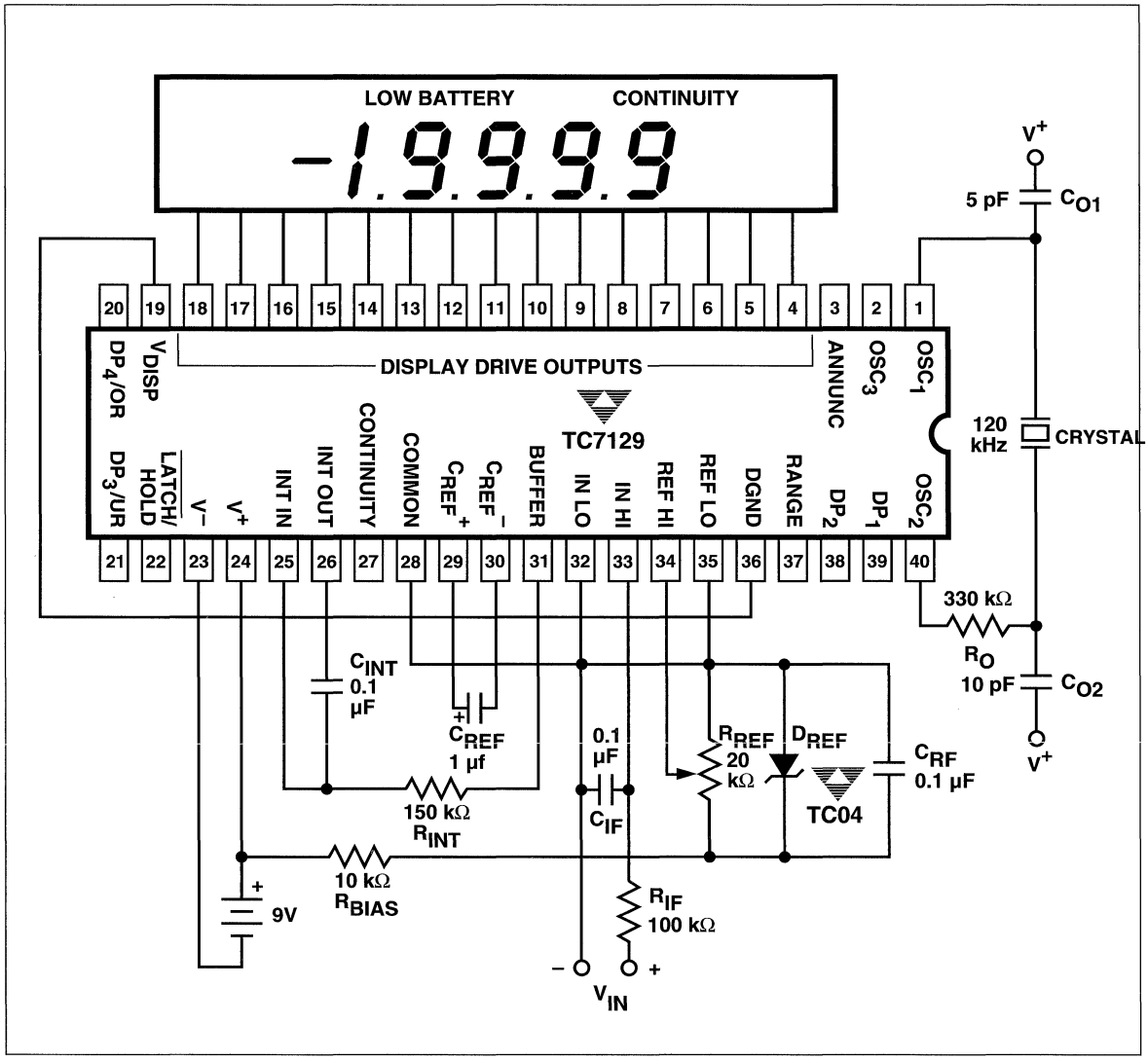


Figure 1 Standard Circuit

Integrating Capacitor (C_{INT})

The charge stored in the integrating capacitor during the integrate phase is directly proportional to the input voltage. The primary selection criterion for C_{INT} is to choose a value that gives the highest voltage swing while remaining within the high-linearity portion of the integrator output range. An integrator swing of 2V is the recommended value. The capacitor value can be calculated from the equation:

$$C_{INT} = \frac{t_{INT} \times I_{INT}}{V_{SWING}},$$

where t_{INT} is the integration time.

Using the values derived above (assuming 60 Hz operation), the equation becomes:

$$C_{INT} = \frac{16.7\ ms \times 13.3\ \mu A}{2V} = 0.1\ \mu F.$$

The capacitor should have low dielectric absorption to ensure good integration linearity. Polypropylene and Teflon capacitors are usually suitable. A good measurement of the dielectric absorption is to connect the reference capacitor across the inputs by connecting:

Pin to Pin
20 → 33 (C_{REF}^+ to IN HI)
30 → 32 (C_{REF}^- to IN LO)

A reading between 10,000 and 9998 is acceptable; anything lower indicates unacceptably high dielectric absorption.

Reference Capacitor (C_{REF})

The reference capacitor stores the reference voltage during several phases of the measurement cycle. Low leakage is the primary selection criterion for this component. The value must be high enough to offset the effect of stray capacitance at the capacitor terminals. A value of at least 1 µF is recommended.

Voltage Reference (D_{REF}, R_{REF}, R_{BIAS}, C_{RF})

A TC04 band-gap reference provides a high-stability voltage reference of 1.25V. The reference potentiometer (R_{REF}) provides an adjustment for adjusting the reference voltage; any value above 20 kΩ is adequate. The bias resistor (R_{BIAS}) limits the current through D_{REF} to less than 150 µA. The reference filter capacitor (C_{RF}) forms an RC filter with R_{BIAS} to help eliminate noise.

Input filter (R_{IF}, C_{IF})

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value should not exceed 100 kΩ. A typical RC time constant value is 16.7 ms to help reject line-frequency noise. The input filter capacitor should have low leakage for a high-impedance input.

Battery

The typical circuit uses a 9V battery as a power source. Any value between 6V and 12V can be used. For operation from batteries with voltages lower than 6V and for operation from power supplies, see "Powering the TC7129."

SPECIAL APPLICATIONS

The TC7129 as a Replacement Part

The TC7129 is a direct pin-for-pin replacement part for the ICL7129. Note, however, that part requires a capacitor and resistor between pins 26 and 28 for phase compensation. Since the TC7129 uses internal phase compensation, these parts are not required and, in fact, **must be removed** from the circuit for stable operation.

Powering the TC7129

While the most common power source for the TC7129 is a 9V battery, there are other possibilities. Some of the more common ones are explained below.

±5V Power Supply

Measurements are made with respect to power supply ground. DGND (pin 36) is set internally to about 5V less than V^+ (pin 24); it is not intended as a power supply input and must not be tied directly to power supply ground. (It can be used as a reference for external logic, as explained in "Connecting to External Logic." (See Figure 2.)

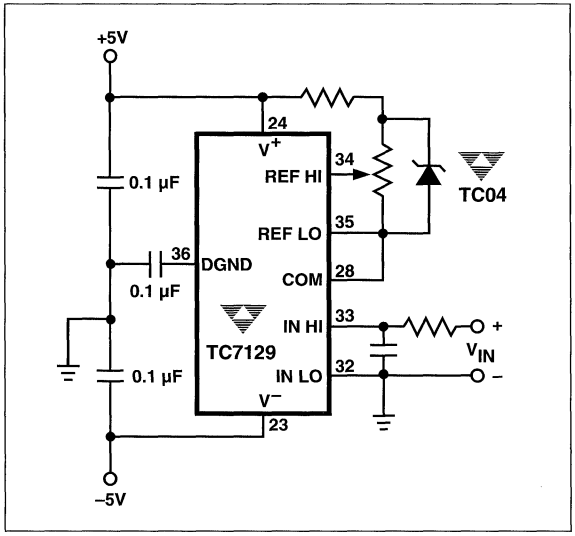


Figure 2 Powering the TC7129 From a ±5V Power Supply

Low-Voltage Battery Source

A battery with voltage between 3.8V and 6V can be used to power the TC7129 when used with a voltage-doubler circuit as shown in Figure 3. The voltage doubler uses the TC7660 DC-to-DC voltage converter and two external capacitors.

+5V Power Supply

Measurements are made with respect to power supply ground. COMMON (pin 28) is connected to REF LO (pin 35). A voltage doubler is needed, since the supply voltage is less than the 6V minimum needed by the TC7129. DGND (pin 36) must be isolated from power supply ground. (See Figure 4.)

Connecting to External Logic

External logic can be directly referenced to DGND (pin 36), provided that the supply current of the external logic does not exceed the sink current of DGND (Figure 5). A safe value for DGND sink current is 1.2 mA. If the sink current is expected to exceed this value, a buffer is recommended. (See Figure 6.)

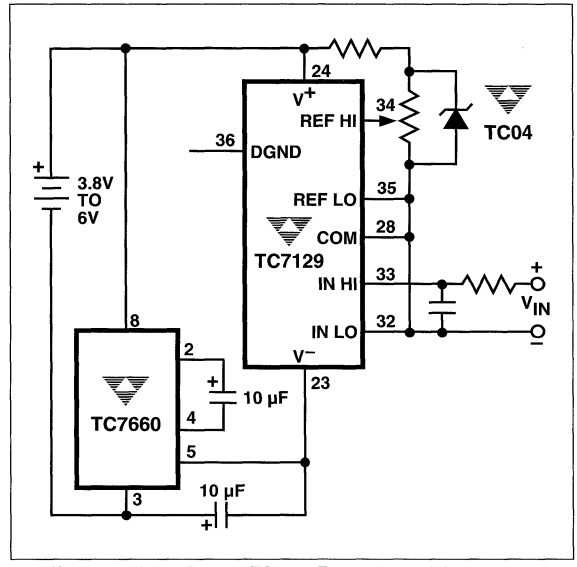


Figure 3 Powering the TC7129 From a Low-Voltage Battery

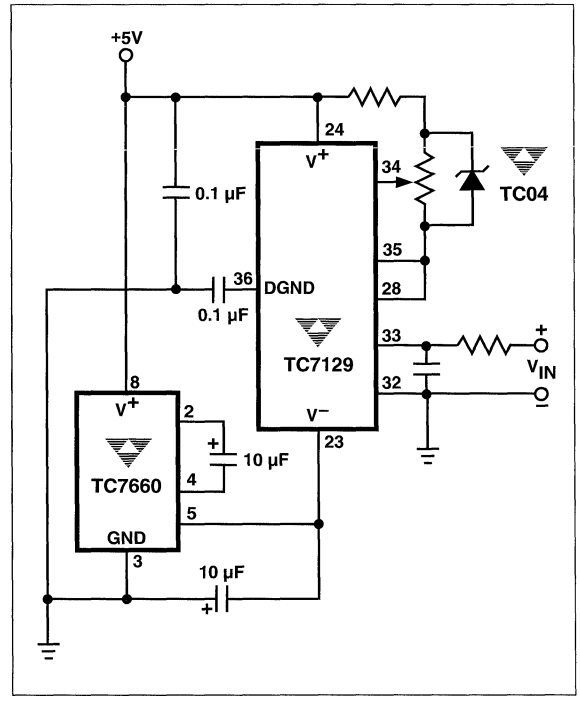


Figure 4 Powering the TC7129 From a +5V Power Supply

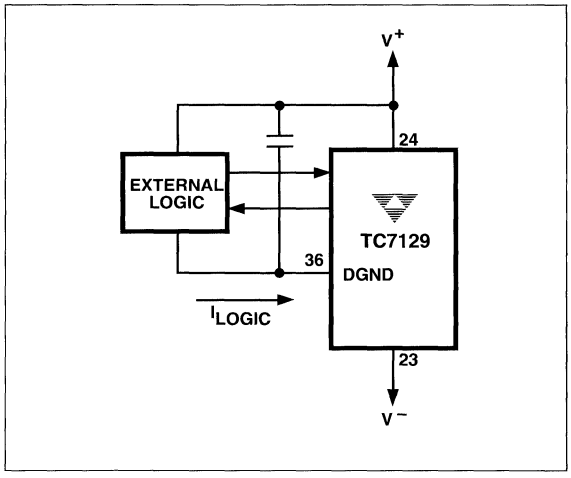


Figure 5 External Logic Referenced Directly to DGND

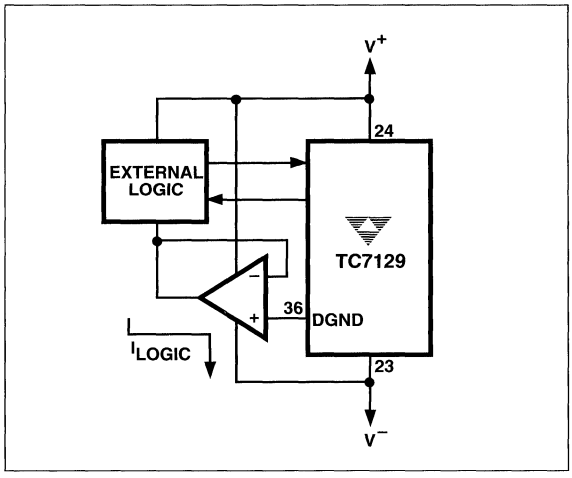


Figure 6 External Logic Referenced to DGND With Buffer

Temperature Compensation

For most applications, V_{DISP} (pin 19) can be connected directly to DGND (pin 36). For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 7 shows two circuits that can be adjusted to give temperature compensation of about 10 mV/°C between V^+ (pin 24) and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-ON voltage because V_{DISP} cannot exceed 0.3V below DGND.

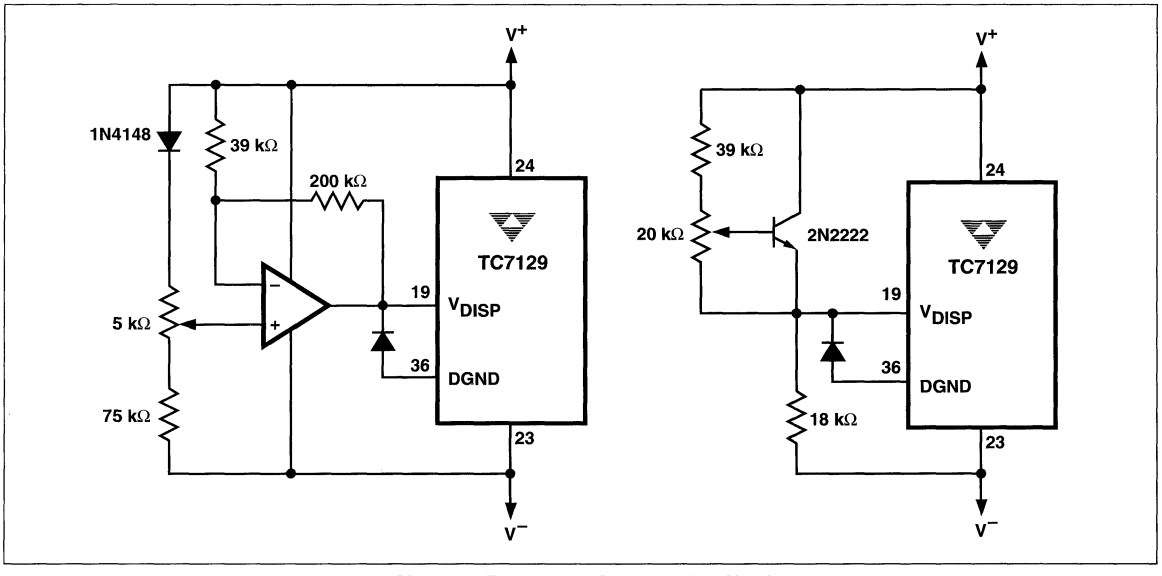


Figure 7 Temperature Compensating Circuits

RC Oscillator

For applications in which 3-1/2 digit (100 μV) resolution is sufficient, an RC oscillator is adequate. A recommended value for the capacitor is 51 pF. Other values can be used as long as they are sufficiently larger than the circuit parasitic capacitance. The resistor value is calculated from:

$$R = \frac{0.45}{freq * C}$$

For 120 kHz frequency and C = 51 pF, the calculated value of R is 75 kΩ. The RC oscillator and the crystal oscillator circuits are shown in Figure 8.

Measuring Techniques

Two important techniques are used in the TC7129: successive integration and digital auto-zeroing. Successive integration is a refinement to the traditional dual-slope conversion technique.

Dual-Slope Conversion

A dual-slope conversion has two basic phases: integrate and deintegrate. During the integrate phase, the input signal is integrated for a fixed period of time; the integrated voltage level is thus proportional to the input voltage. During the deintegrate phase, the integrated voltage is ramped down at a fixed slope, and a counter counts the clock cycles until the integrator voltage crosses zero. The count is a measurement of the time to ramp the integrated voltage to zero, and is therefore proportional to the input voltage being measured. This count can then be scaled and displayed as a measurement of the input voltage. Figure 9 shows the phases of the dual-slope conversion.

The dual-slope method has a fundamental limitation. The count can only stop on a clock cycle, so that measurement accuracy is limited to the clock frequency. In addition, a delay in the zero-crossing comparator can add to the inaccuracy. Figure 10 shows these errors in an actual measurement.

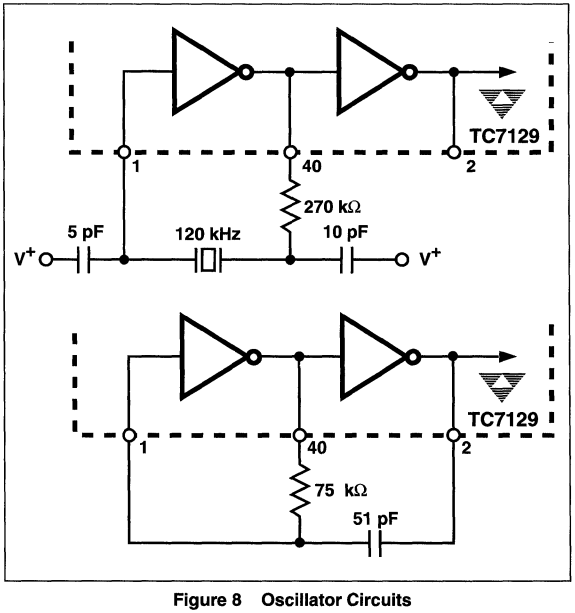


Figure 8 Oscillator Circuits

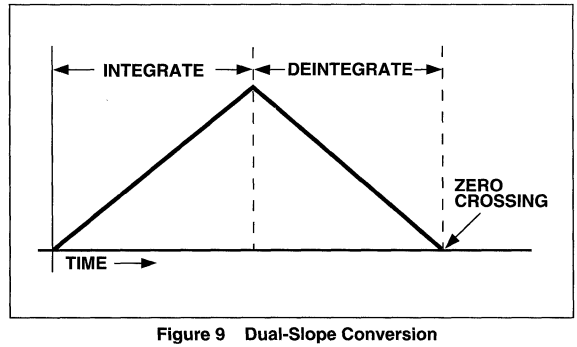


Figure 9 Dual-Slope Conversion

Successive Integration

The successive integration technique picks up where dual-slope conversion ends. The overshoot voltage shown in Figure 10, called the "integrator residue voltage," is measured to obtain a correction to the initial count. Figure 11 shows the cycles in a successive integration measurement.

The waveform shown is for a negative input signal. The sequence of events during the measurement cycle is:

Phase	Description
INT_1	Input signal is integrated for fixed time. (1000 clock cycles on 2V scale, 10,000 on 200 mV)
DE_1	Integrator voltage is ramped to zero. Counter counts up until zero crossing to produce reading accurate to 3-1/2 digits. Residue represents an overshoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE_2	Integrator voltage is ramped to zero. Counter counts down until zero crossing to correct reading to 4-1/2 digits. Residue represents an undershoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE_3	Integrator voltage is ramped to zero. Counter counts up until zero crossing to correct reading to 5-1/2 digits. Residue is discarded.

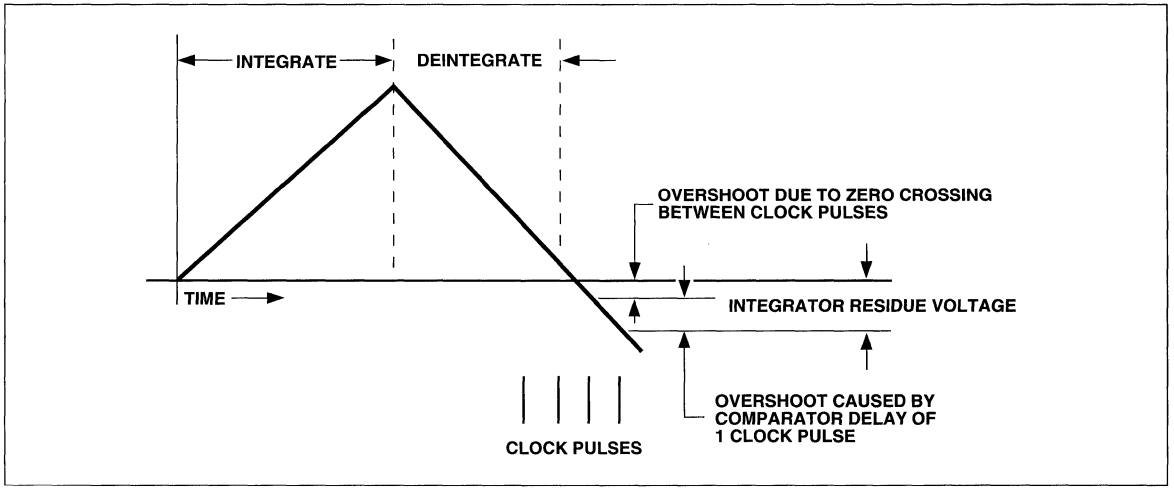


Figure 10 Accuracy Errors in Dual-Slope Conversion

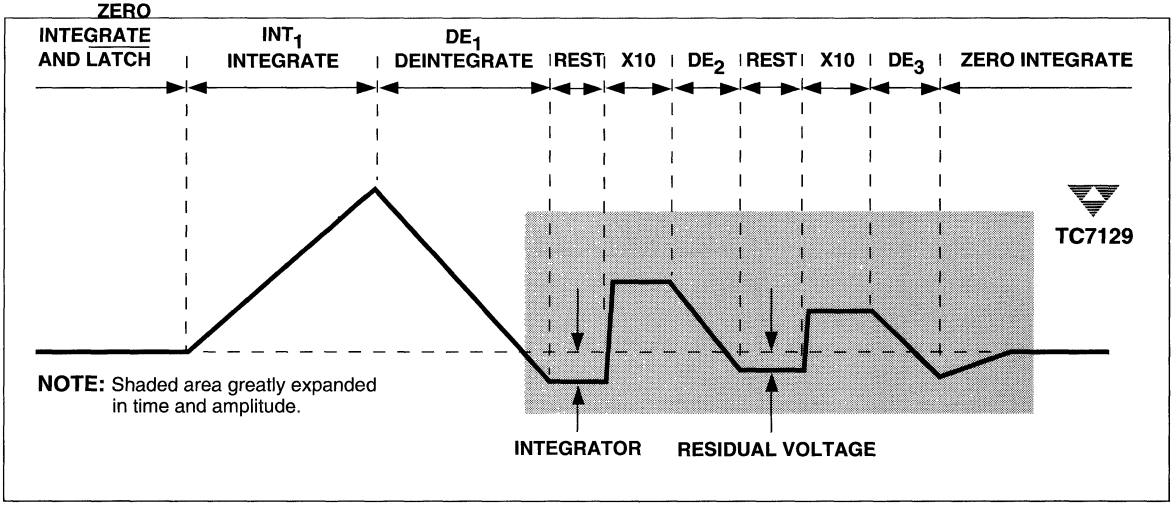


Figure 11 Integrator Waveform

Digital Auto-Zeroing

To eliminate the effect of amplifier offset errors, the TC7129 uses a digital auto-zeroing technique. After the input voltage is measured as described above, the measurement is repeated with the inputs shorted internally. The reading with inputs shorted is a measurement of the internal errors and is subtracted from the previous reading to obtain a corrected measurement. Digital auto-zeroing eliminates the need for an external auto-zeroing capacitor used in other ADCs.

Inside the TC7129

Figure 12 shows a simplified block diagram of the TC7129.

Integrator Section

The integrator section includes the integrator, comparator, input buffer amplifier, and analog switches used to change the circuit configuration during the separate measurement phases described earlier.

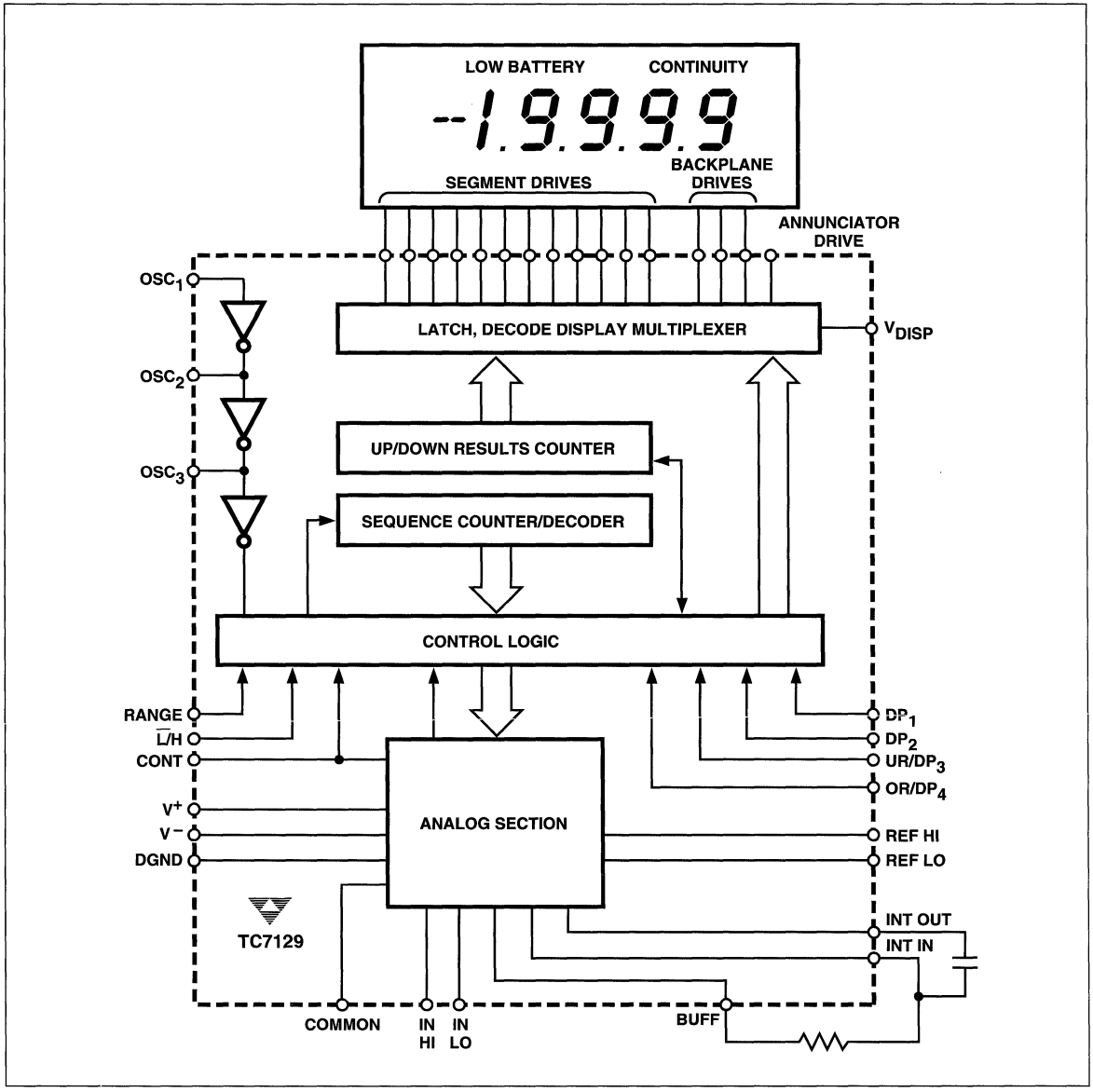


Figure 12 Functional Diagram

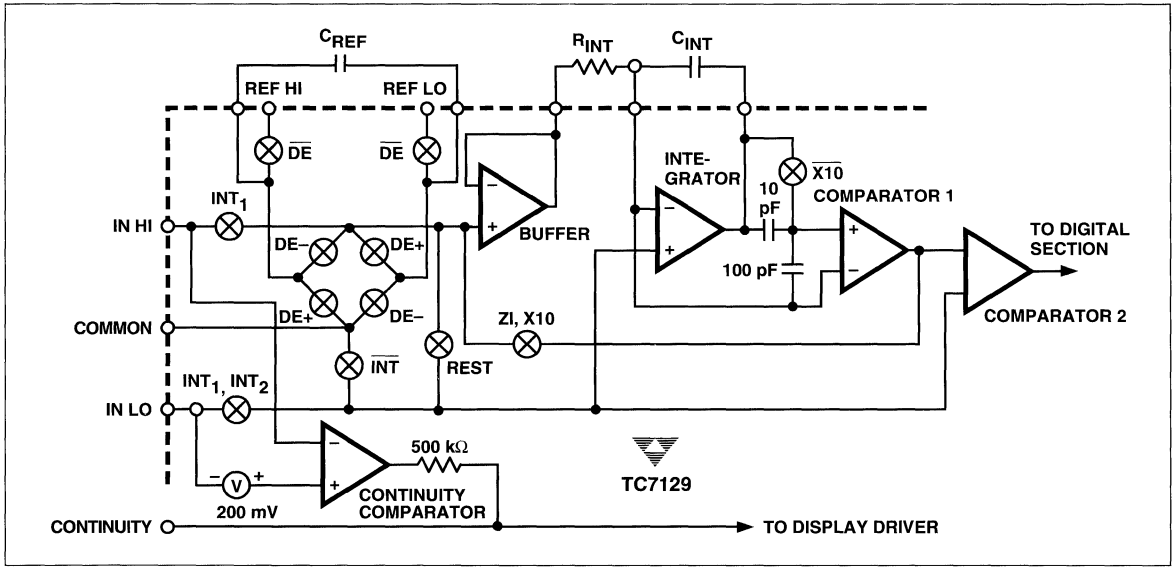


Figure 13 Integrator Block Diagram

Table I. Switch Legends

Label	Meaning
$\overline{DE}$	Open during all deintegrate phases.
DE–	Closed during all deintegrate phases when input voltage is negative.
DE+	Closed during all deintegrate phases when input voltage is positive.
INT_1	Closed during the first integrate phase (measurement of the input voltage).
INT_2	Closed during the second integrate phase (measurement of the amplifier offset).
$\overline{INT}$	Open during both integrate phases.
REST	Closed during the rest phase.
ZI	Closed during the zero-integrate phase.
X10	Closed during the X10 phase.
$\overline{X10}$	Open during the X10 phase.

The buffer amplifier has a common-mode input voltage range from 1.5V above V^- to 1V below V^+. The integrator amplifier can swing to within 0.3V of the rails, although for best linearity the swing is usually limited to within 1V. Both amplifiers can supply up to 80 µA of output current, but should be limited to 20 µA for good linearity.

Continuity Indicator

A comparator with a 200 mV threshold is connected between IN HI (pin 33) and IN LO (pin 32). Whenever the voltage between inputs is less than 200 mV, the CONTINUITY output (pin 27) will be pulled HIGH, activating the continuity annunciator on the display. The continuity pin can also be used as an input to drive the continuity annunciator directly from an external source. A schematic of the input/output nature of this pin is shown in Figure 15.

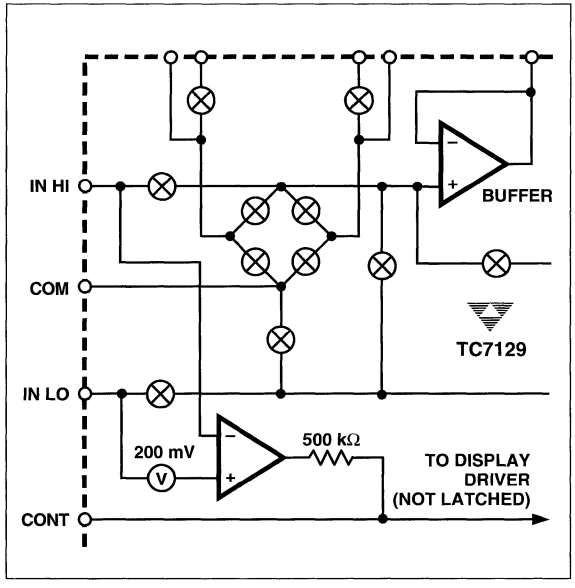


Figure 14 Continuity Indicator Circuit

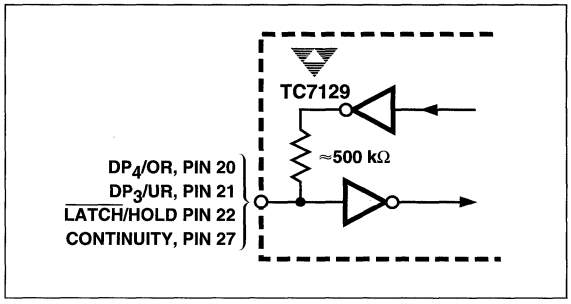


Figure 15 Input/Output Pin Schematic

Common and Digital Ground

The common and digital ground (DGND) outputs are generated from internal zener diodes. The voltage between V^+ and DGND is the internal supply voltage for the digital section of the TC7129. Common can source approximately 12 µA; DGND has essentially no source capability.

Low Battery

The low battery annunciator turns on when supply voltage between V^+ and V^- drops below 6.8V. The internal zener has a threshold of 6.3V. When the supply voltage drops below 6.8V, the transistor tied to V^- turns OFF, pulling the "Low Battery" point HIGH. (See Figure 16.)

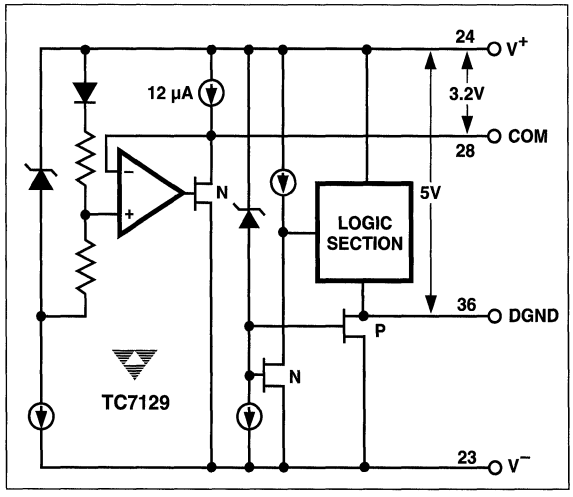


Figure 16 Digital Ground (DGND) and Common Outputs

Sequence and Results Counter

A sequence counter and associated control logic provide signals that operate the analog switches in the integrator section. The comparator output from the integrator gates the results counter. The results counter is a six-section up/down decade counter which holds the intermediate results from each successive integration.

Overrange and Underrange Outputs

When the results counter holds a value greater than ±19,999, the DP_4/OR output (pin 20) is driven HIGH. When the results counter value is less than ±1000, the DP_3/UR output (pin 21) is driven HIGH. Both signals are valid on the falling edge of $\overline{\text{LATCH}}$/HOLD ($\overline{\text{L}}$/H) and do not change until the end of the next conversion cycle. The signals are updated at the end of each conversion unless the L/H input (pin 22) is held HIGH. Pins 20 and 21 can also be used as inputs for external control of decimal points 3 and 4. Figure 15 shows a schematic of the input/output nature of these pins.

Latch/Hold

The $\overline{\text{L}}$/H output goes LOW during the last 100 cycles of each conversion. This pulse latches the conversion data into the display driver section of the TC7129. This pin can also be used as an input. When driven HIGH, the display will not be updated; the previous reading is displayed. When driven LOW, the display reading is not latched; the sequence counter reading will be displayed. Since the counter is counting much faster than the backplanes are being updated, the reading shown in this mode is somewhat erratic.

Display Driver

The TC7129 drives a triplexed LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for continuity and low battery. Figure 17 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 1200. This results in a backplane drive frequency of 100 Hz for 60 Hz operation (120 kHz crystal) and 83.3 Hz for 50 Hz operation (100 kHz crystal).

Backplane waveforms are shown in Figure 18. These appear on outputs BP_1, BP_2, BP_3 (pins 16, 17, and 18). They remain the same regardless of the segments being driven.

Other display output lines (pins 4 through 15) have waveforms that vary depending on the displayed values. Figure 19 shows a set of waveforms for the A, G, D outputs (pins 5, 8, 11, and 14) for several combinations of "ON" segments.

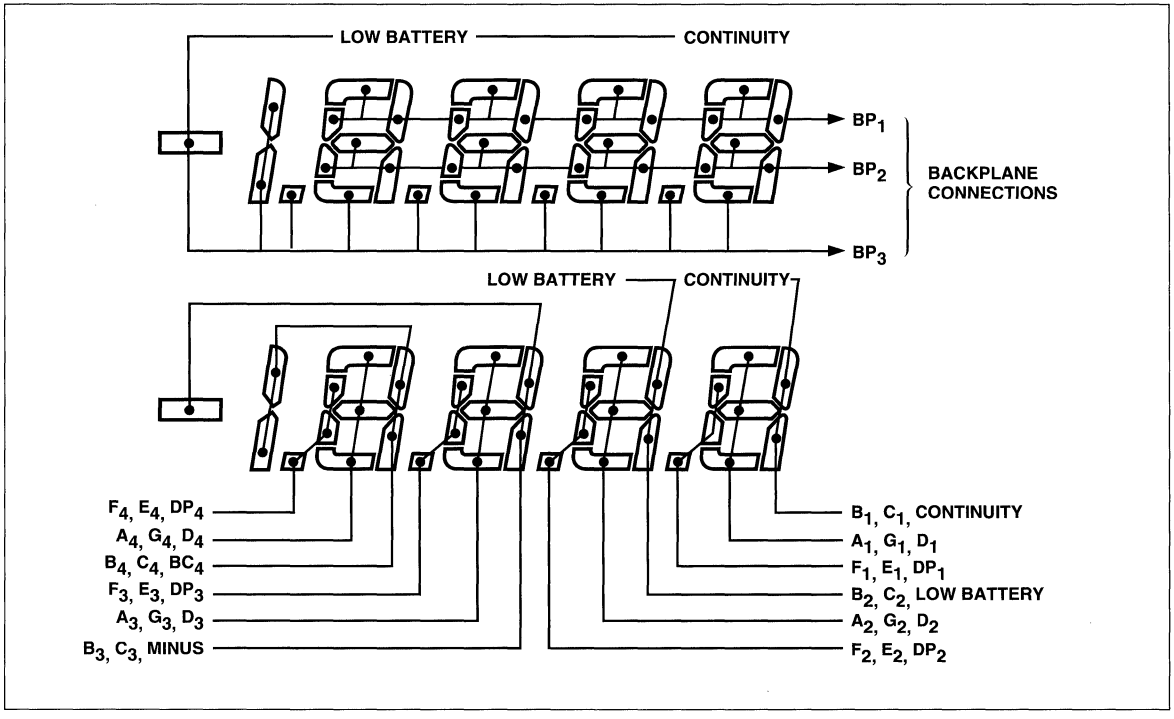


Figure 17 Display Segment Assignments

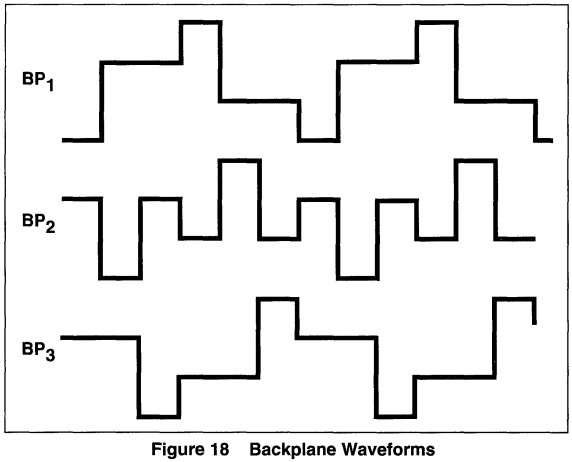


Figure 18 Backplane Waveforms

The ANNUNCIATOR DRIVE output (pin 3) is a square-wave running at the backplane frequency (100 Hz or 83.3 Hz), with a peak-to-peak voltage equal to DGND voltage. Connecting an annunciator to pin 3 turns it ON; connecting it to its backplane turns it OFF.

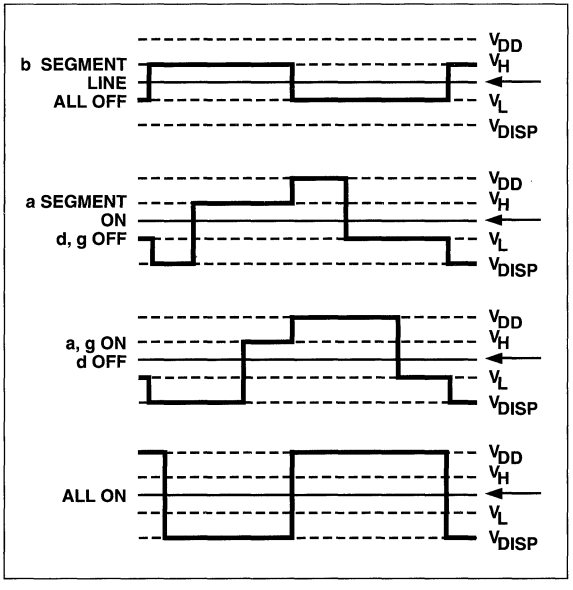


Figure 19 Typical Display Output Waveforms

TelCom Semiconductor, Inc.

LOW POWER, HIGH CMRR, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 120 dB CMRR (± 0.01 Count / Volt CMV error)
- Fast Overrange Recovery, Guaranteed First Reading Accuracy
- Low Temperature Drift Internal Reference
  TC7131 ..... 70 ppm/°C Typ
- Guaranteed Zero Reading With Zero Input
- Low Noise ..... 15 μV_{P-P}
- High Resolution 0.05%
- Wide Dynamic Range ..... 72 dB
- Low Input Leakage Current ..... 1 pA Typ
  10 pA Max
- Direct LCD Drive — No External Components
- Precision Null Detectors With True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation With Low Power Dissipation ..... 500 µW Typ
  900 µW Max
- Internal Clock Circuit

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts
  - — Strain Gauges
  - — Load Cells
  - — Null Detectors
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
  - — Humidity
  - — Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers

ORDERING INFORMATION

Part No.	Package	Temperature Range	Reference TempCo (Max)
TC7131CPL	40-Pin Plastic DIP	0°C to +70°C	150 ppm/°C
TC7131CLW	44-Pin PQFP	0°C to + 70° C	150 ppm/°C

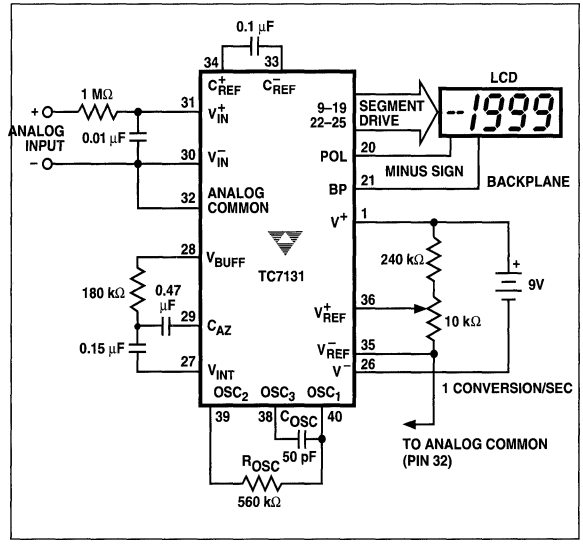
GENERAL DESCRIPTION

The TC7131 is a low-power, 3-1/2 digit, LCD-drive analog-to-digital converter (ADC). It has superior DC Common-Mode Rejection (CMR) when used with either a single or split power supply. It incorporates an "integrator output zero" phase which guarantees overrange recovery. The performance of existing TC7126, TC7126A and ICL7136-based systems may be upgraded with minor changes to external passive components. (see "System Timing")

The TC7131 limits linearity error to less than 1 count on 200 mV or 2V full-scale ranges. Roll-over error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High-impedance differential inputs offer 1 pA leakage currents and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display readout for a 0V input.

The single-chip CMOS TC7131 incorporates all the active devices for a 3-1/2 digit ADC to directly drive an LCD. The internal oscillator, precision voltage reference, and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low-cost, high-resolution (0.05%) indicating meter requires only a display, four resistors, four capacitors and a 9V battery.

TYPICAL OPERATING CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (Either Input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Either Input) ..... V^+ to V^-
Clock Input ..... TEST to V^+
Power Dissipation (Note 2)
  Plastic DIP (P) ..... 800 mW
  Flat Package (L) ..... 500 mW
Operating Temperature Range
  C Devices ..... 0°C to +70°C
  Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

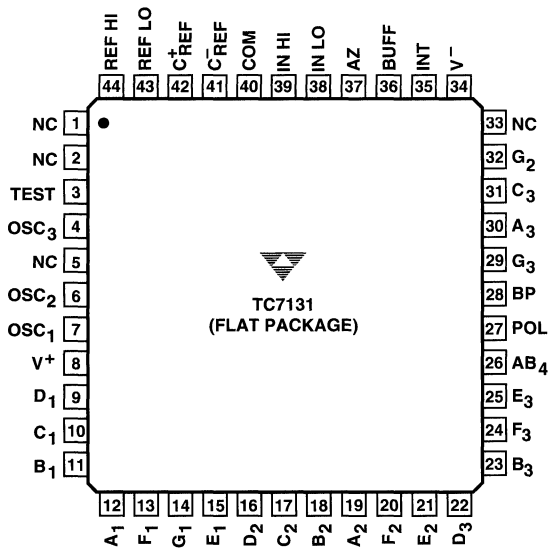
*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

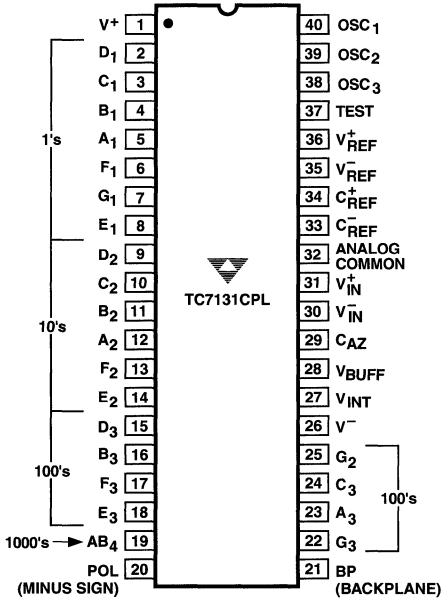
ELECTRICAL CHARACTERISTICS: V_S = 9V, f_{CLK} = 16 kHz, and T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	–000.0	±000.0	+000.0	Digital Reading
	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C	—	0.2	1	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
NL	Nonlinearity Error	Full Scale = 200 mV or 2V Max Deviation From Best Straight Line	–1	±0.2	1	Count
	Roll-Over Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200 mV	–1	±0.2	1	Count
e_N	Noise	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200 mV	—	1	—	µV/V
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C ≤ T_A ≤ +70°C Ext Ref Temp Coeff = 0 ppm/°C	—	1	5	ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ +70°C	—	70	150	ppm/°C
V_C	Analog Common Voltage	250 kW Between Common and V^+	2.7	3.05	3.35	V
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_S	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V (Note 6)	—	70	100	µA

NOTES:
1. Input voltages may exceed supply voltages when input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "off" segment and 180° out-of-phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
5. See "Typical Operating Circuit".
6. A 48 kHz oscillator increases current by 20 µA (typical). Common current not included.

PIN CONFIGURATIONS





NC = NO INTERNAL CONNECTION

PIN DESCRIPTION

40-Pin DIP Pin Number	44-Pin Plastic Quad Flat Package Pin Number	Name	Description
1	2	V^+	Positive supply voltage.
2	3	D_1	Activates the D section of the units display.
3	4	C_1	Activates the C section of the units display.
4	5	B_1	Activates the B section of the units display.
5	6	A_1	Activates the A section of the units display.
6	7	F_1	Activates the F section of the units display.
7	8	G_1	Activates the G section of the units display.
8	9	E_1	Activates the E section of the units display.
9	10	D_2	Activates the D section of the tens display.
10	11	C_2	Activates the C section of the tens display.
11	13	B_2	Activates the B section of the tens display.
12	14	A_2	Activates the A section of the tens display.
13	15	F_2	Activates the F section of the tens display.
14	16	E_2	Activates the E section of the tens display.
15	17	D_3	Activates the D section of the hundreds display.
16	18	B_3	Activates the B section of the hundreds display.
17	19	F_3	Activates the F section of the hundreds display.
18	20	E_3	Activates the E section of the hundreds display.
19	21	AB_4	Activates both halves of the 1 in the thousands display.
20	22	POL	Activates the negative polarity display.
21	24	BP	Backplane drive output.
22	25	G_3	Activates the G section of the hundreds display.
23	26	A_3	Activates the A section of the hundreds display.
24	27	C_3	Activates the C section of the hundreds display.
25	28	G_2	Activates the G section of the tens display.
26	29	V^-	Negative power supply voltage.
27	30	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build-up will not allow the integrator output to saturate. When ANALOG COMMON is used as a reference and the conversion rate is 3 readings per second, a 0.047 µF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See Integrating Capacitor section for additional details.
28	31	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.8 MΩ for 2V full-scale range.
29	32	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 µF capacitor for a 200 mV full scale, and a 0.1 µF capacitor for a 2V full scale. See paragraph on Auto-Zero Capacitor for more details.
30	33	V_{IN}^-	The low input signal is connected to this pin.
31	35	V_{IN}^+	The high input signal is connected to this pin.
32	36	ANALOG COMMON	Internal V COMMON GENERATOR.

TC7131 PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number	44-Pin Plastic Quad Flat Package Pin Number	Name	Description
33	37	C_{REF}^-	See pin 34.
34	38	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	39	V_{REF}^-	See pin 36.
36	40	V_{REF}^+	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	41	TEST	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under TEST for additional information.
38	42	OSC_3	See pin 40.
39	43	OSC_2	See pin 40.
40	44	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per second) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

GENERAL THEORY OF OPERATION

(All Pin designations refer to 40-Pin DIP)

Dual-Slope Conversion Principles

The TC7131 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7131 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period (t_{SI}), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (t_{RI}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

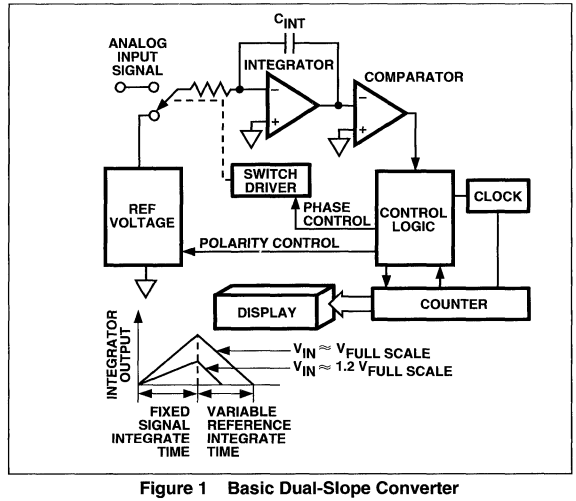


Figure 1 Basic Dual-Slope Converter

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right]$$

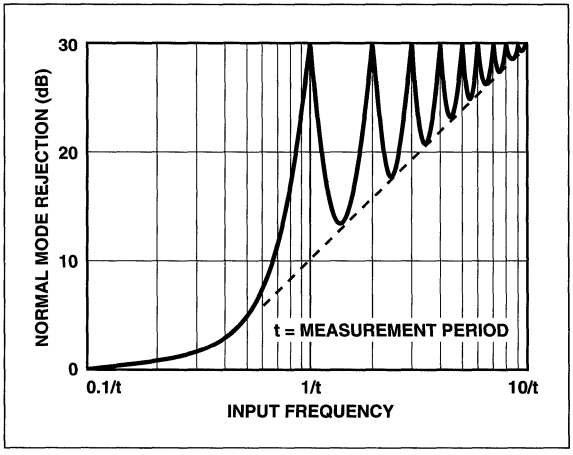


Figure 2 Normal-Mode Rejection of Dual-Slope Converter

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period.

The TC7131 is similar to the 7136 family in terms of features. A side-by -side comparison would show a difference in reference point during the conversion cycle. Specifically, the TC7131 uses IN LO only during the integrate phase, and ANALOG COMMON during the other three phases. The result is superior DC CMR for the TC7131 (120dB) at the expense of a reduced AC CMR.

ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7131 design incorporates an "integrator output-zero cycle" and an "auto-zero cycle." These additional cycles ensure that the integrator starts at 0V (even after a severe overrange conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator output-zero phase
(2) Auto-zero phase
(3) Signal integrate phase
(4) Reference deintegrate phase

Integrator Output-Zero Phase

This phase guarantees the integrator output is at 0V before the system-zero phase is entered. This ensures that true system offset voltages will be compensated for even after an overrange conversion. The count for this phase is a function of the number of counts required by the deintegrate phase.

The count lasts from 11 to 140 counts for non-overrange conversions and from 31 to 640 counts for overrange conversions.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog switches. The internal nodes are shorted to IN LO (ground) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 μV to 15 μV.

The auto-zero duration is from 910 to 2900 counts for non-overrange conversions and from 300 to 910 counts for overrange conversions.

Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TC7131 signal integration period is 1000 clock periods or counts. The externally-set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

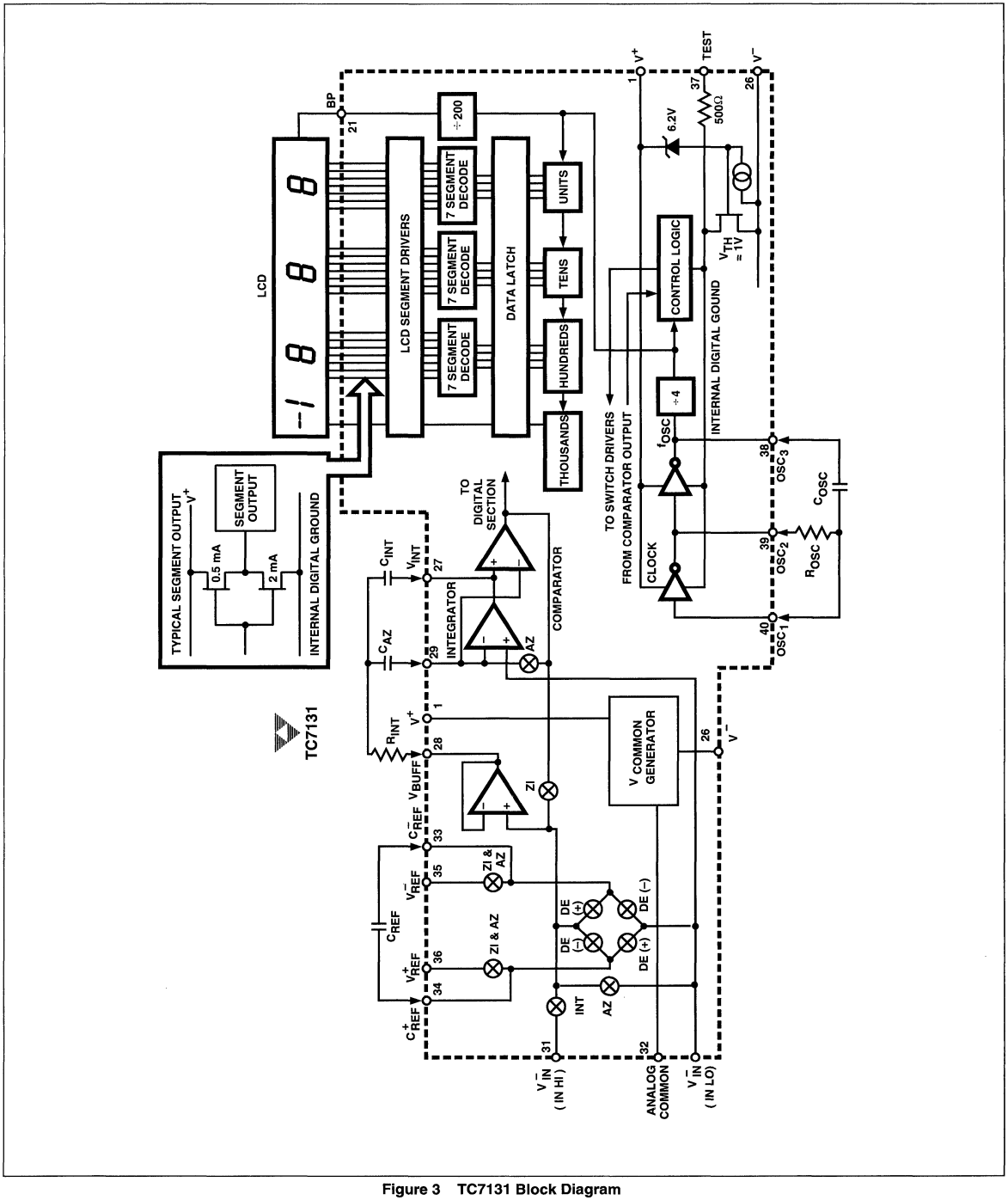


Figure 3 TC7131 Block Diagram

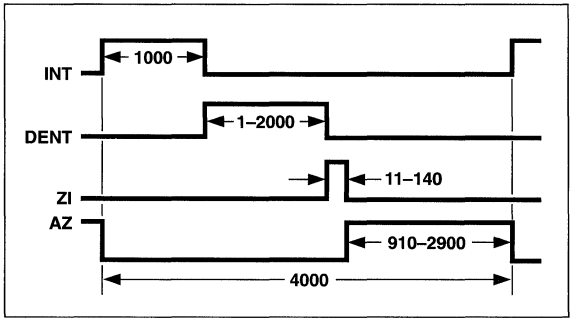


Figure 4 Conversion Timing During Normal Operation

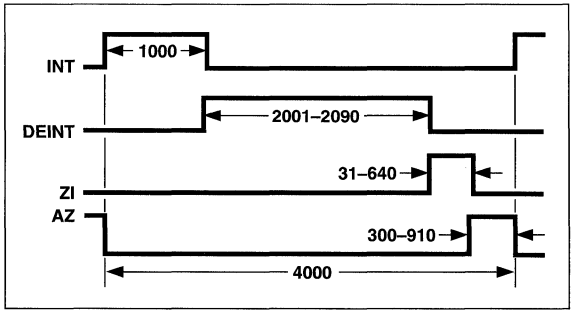


Figure 5 Conversion Timing During Overrange Operation

Reference Integrate Phase

The third phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC7131 contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions per second the backplane frequency is 60 Hz with a 5V nominal amplitude. When a segment driver is in-phase with the backplane signal, the segment is OFF. An out-of-phase segment drive signal causes the segment to be ON, or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed, this indicator would reverse.

On the TC7131, when the TEST pin is pulled to V^+, all segments are turned ON. The display reads –1888. During this mode the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES. LCDs may be destroyed if operated with DC levels for extended periods.

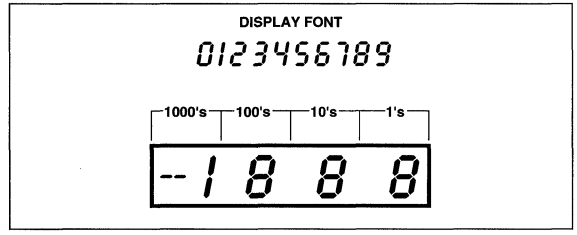


Figure 6 Display FONT and Segment Assignment

The display font and segment drive assignment are shown in Figure 6.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts, or 16,000 clock pulses. The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 3000 to 2900 counts
(1200 to 11,600 clock pulses)

(2) Signal integrate: 1000 counts
(4000 clock pulses)

This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right]$$

where f_{OSC} is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts

(4) Zero integrator: 11 to 640 counts

The TC7131 is a drop-in replacement for the TC7126 and ICL7126 when V_{IN}^- is tied to ANALOG COMMON.

COMPONENT VALUE SELECTION

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.1 µF capacitor is adequate for 2V full-scale applications. A Mylar dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate phase is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- ≠ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 µF. Roll-over error will be held to less than 0.5 count. A Mylar dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference in this case: a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second (f_{OSC} = 48 kHz) a 0.047 µF value is suggested. For one reading per second, 0.15 µF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 µA. The integrator and buffer can supply 1 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 kΩ. A 2V full scale requires 1.8 MΩ.

Component	Nominal Full-Scale Voltage	
Value	**200 mV**	**2V**
C_{AZ}	0.47 µF	0.1 µF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 µF	0.047 µF

NOTE: f_{OSC} = 48 kHz (3 readings per sec). R_{OSC} = kΩ, C_{OSC} = 50 pF.

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

Note that f_{OSC} is ÷ 4 to generate the TC7131's internal clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz,etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*V_{FS} = 2 V_{REF}.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

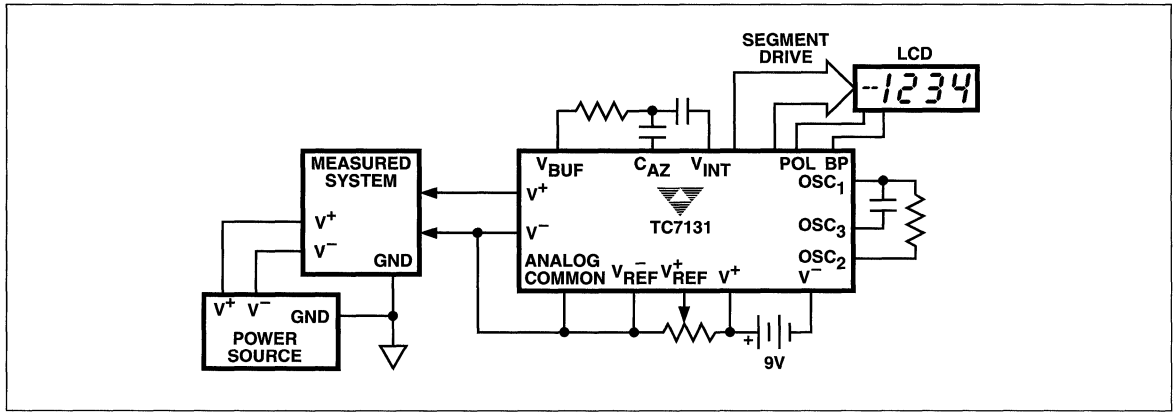


Figure 7 Common-Mode Voltage Removed in Battery Operation With V_{IN} = Analog Common

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC7131 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ - 1V$ to $V^- + 1V$. Common-mode voltages are removed from the system when the TC7131 operates from a battery or floating power source (isolated from measured system), and V_{IN}^- is connected to ANALOG COMMON (V_{COM}). (See Figure 7.)

In systems where common-mode voltages exist, the 120 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 8.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

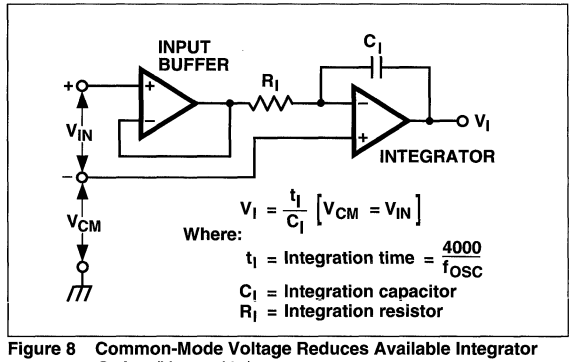


Figure 8 Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

The TC7131 offers a significantly improved ANALOG COMMON temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of ANALOG COMMON is typically 70 ppm/°C.

ANALOG COMMON (Pin 32)

The ANALOG COMMON pin is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. ANALOG COMMON is tied internally to an N-channel FET capable of sinking 100µA. This FET will hold the COMMON line at 3V below V^+ if an external load attempts to pull the COMMON line toward V^+. ANALOG COMMON source current is limited to 1 µA. ANALOG COMMON is therefore easily pulled to a more negative voltage (i.e., below $V^+ - 3V$).

The ANALOG COMMON pin serves to set the analog section reference, or COMMON point. The TC7131 is specifically designed to operate from a battery or in any mea-

surement system where input signals are not referenced (float) with respect to the TC7131 power source. The ANALOG COMMON potential of V^+ –3V gives a 7V end of battery life voltage. The COMMON potential has a 0.001%/% voltage coefficient.

TEST (Pin 37)

The TEST pin potential is 5V less than V^+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The TEST pin load should not be more than 1 mA. See the Applications Section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled high (to V^+), all segments plus the minus sign will be activated. DO NOT OPERATE IN THIS MODE FOR MORE THAN SEVERAL MINUTES. With TEST = V^+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

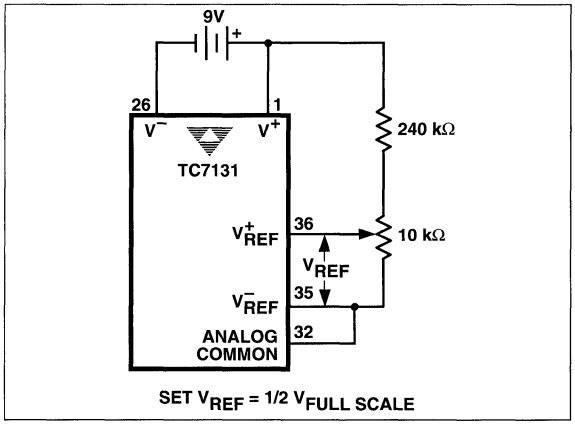


Figure 9 TC7136A Internal Voltage Reference Connection

APPLICATIONS INFORMATION

Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7131 3-1/2 digit analog-to-digital converter applications information

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	I1048, I1126
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the TEST pin; its potential is approximately 5V below V^+.

Ratiometric Resistance Measurements

The TC7131's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

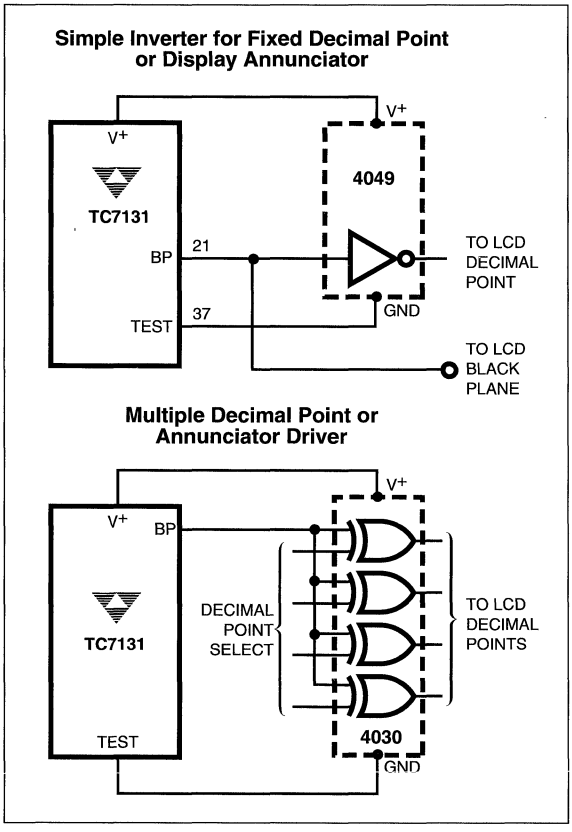


Figure 10 Decimal Point and Annunciator Drives

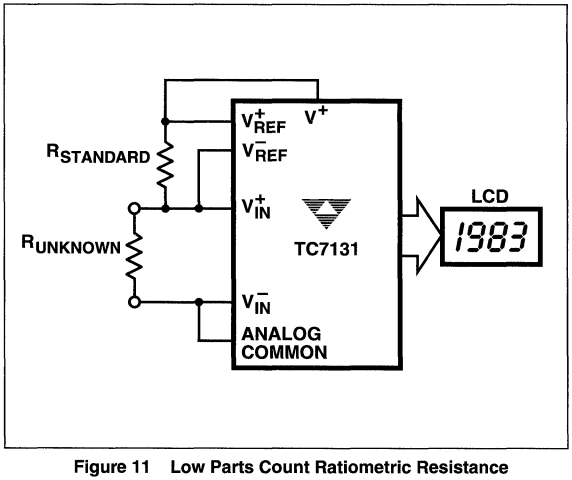


Figure 11 Low Parts Count Ratiometric Resistance Measurement

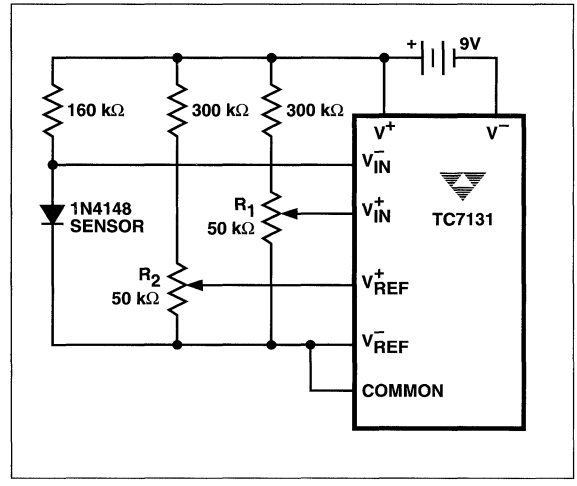
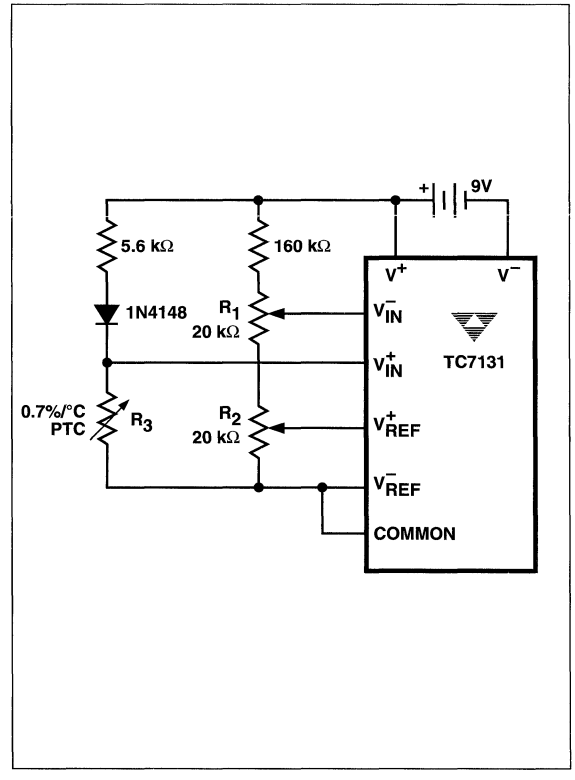


Figure 12 Temperature Sensor



LOW POWER, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **Fast Overrange Recovery, Guaranteed First Reading Accuracy**
- **Low Temperature Drift Internal Reference**
  - **TC7136 ..... 70 ppm/°C Typ**
  - **TC7136A ..... 35 ppm/°C Typ**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise ..... 15 μV_{P-P}**
- **High Resolution 0.05%**
- **Low Input Leakage Current ..... 1 pA Typ**
  10 pA Max
- **Precision Null Detectors With True Polarity at Zero**
- **High-Impedance Differential Input**
- **Convenient 9V Battery Operation With Low Power Dissipation ..... 500 μW Typ**
  900 μW Max

TYPICAL APPLICATIONS

- **Thermometry**
- **Bridge Readouts: Strain Gauges, Load Cells, Null Detectors**
- **Digital Meters: Voltage/Current/Ohms/Power, pH**
- **Digital Scales, Process Monitors**
- **Portable Instrumentation**

ORDERING INFORMATION

PART CODE **TC7136X X XXX**

A or blank* —

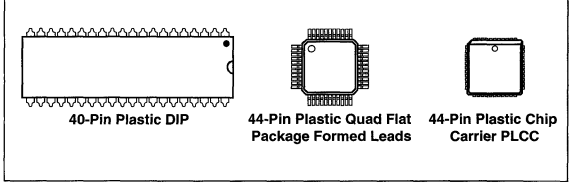
R (reversed pins) or blank (CPL pkg only) —

* "A" parts have an improved reference TC

Package Code (see below): —

Package Code	Package	Pin Layout	Temperature Range
CPL	40-Pin PDIP	Normal	0°C to +70°C
CKW	44-Pin PQFP	Formed Leads	0°C to +70°C
CLW	44-Pin PLCC	—	0°C to +70°C

AVAILABLE PACKAGES



40-Pin Plastic DIP

44-Pin Plastic Quad Flat Package Formed Leads

44-Pin Plastic Chip Carrier PLCC

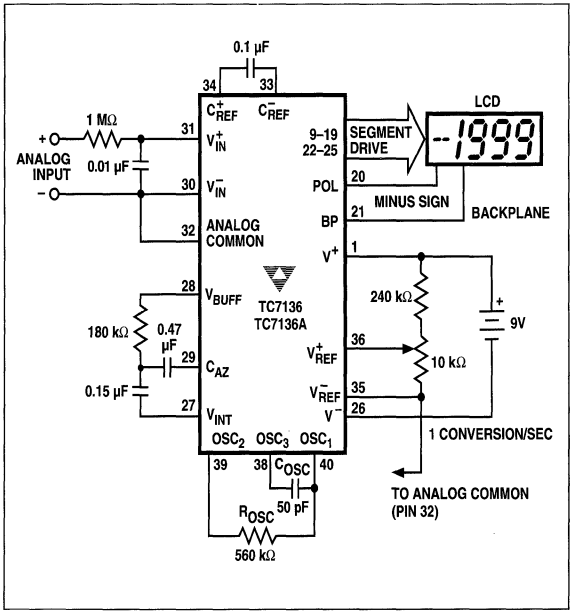
GENERAL DESCRIPTION

The TC7136 and TC7136A are low-power, 3-1/2 digit with liquid crystal display (LCD) drivers with analog-to-digital converters. These devices incorporate an "integrator output zero" phase which guarantees overrange recovery. The performance of existing TC7126, TC7126A and ICL7126-based systems may be upgraded with minor changes to external, passive components.

The TC7136A has an improved internal zener reference voltage circuit which maintains the analog common temperature drift to 35 ppm/°C (typical) and 75 ppm/°C (maximum). This represents an improvement of two to four times over similar 3-1/2 digit converters. The costly, space-consuming external reference source may be removed.

The TC7136/A limits linearity error to less than 1 count on 200 mV or 2V full-scale ranges. Roll-over error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High-impedance differential inputs offer 1 pA leakage currents and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display readout for a 0V input.

TYPICAL OPERATING CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (Either Input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Either Input) ..... V^+ to V^-
Clock Input ..... TEST to V^+
Power Dissipation (Note 2)
- CerDIP (J) ..... 1000 mW
- Plastic DIP (P) ..... 800 mW
- Flat Package (K, L) ..... 500 mW

Operating Temperature Range
- C Devices ..... 0°C to +70°C
- I Devices ..... –25°C to +85°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

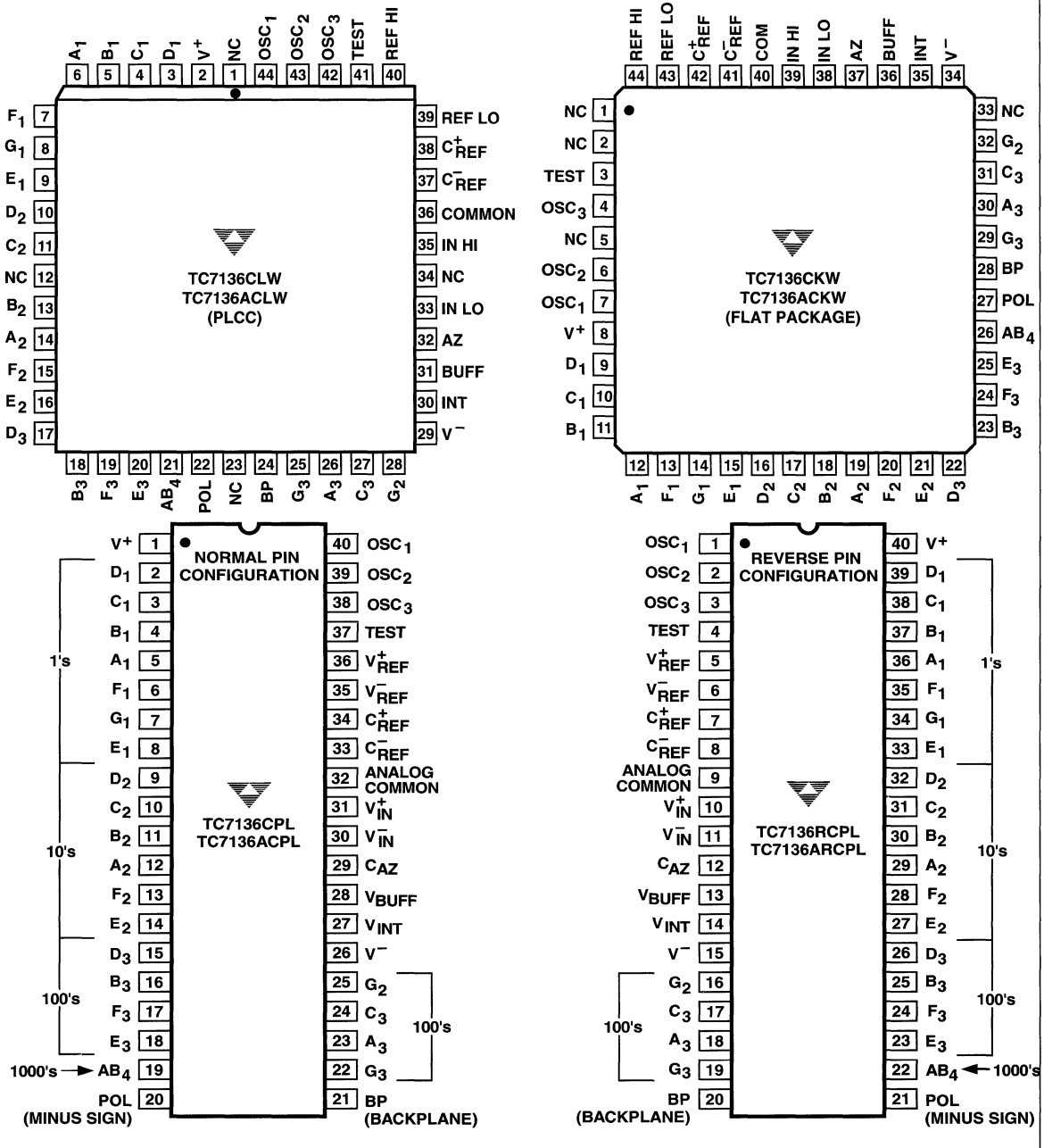
ELECTRICAL CHARACTERISTICS: V_S = 9V, f_{CLK} = 16 kHz, and T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	– 000.0	±000.0	+000.0	Digital Reading
	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C	—	0.2	1	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
NL	Nonlinearity Error	Full Scale = 200 mV or 2V Max Deviation From Best Straight Line	– 1	±0.2	1	Count
	Roll-Over Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200 mV	– 1	±0.2	1	Count
e_N	Noise	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200 mV	—	50	—	µV/V
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C ≤ T_A ≤ +70°C Ext Ref Temp Coeff = 0 ppm/°C	—	1	5	ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+				
		0°C ≤ T_A ≤ +70°C TC7136A	—	35	75	ppm/°C
		"C" Commercial Temp TC7136 Range Devices	—	70	150	ppm/°C
		– 25°C ≤ T_A ≤ +85°C TC7136A	—	35	100	ppm/°C
		"I" Industrial Temp TC7136 Range Devices	—	70	150	ppm/°C
V_C	Analog Common Voltage	250 kW Between Common and V^+	2.7	3.05	3.35	V
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_S	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V (Note 6)	—	70	100	µA

NOTES:
1. Input voltages may exceed supply voltages when input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "OFF" segment and 180° out-of-phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
5. See "Typical Operating Circuit".
6. A 48 kHz oscillator increases current by 20 µA (typical). Common current not included.

2

PIN CONFIGURATIONS



TC7136/A PIN DESCRIPTION

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
1	(40)	V^+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP	Backplane drive output.
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V^-	Negative power supply voltage.
27	(14)	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build-up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 µF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See Integrating Capacitor section for additional details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.8 MΩ for 2V full-scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 µF capacitor for a 200 mV full scale, and a 0.1 µF capacitor for a 2V full scale. See paragraph on Auto-Zero Capacitor for more details.
30	(11)	V_{IN}^-	The low input signal is connected to this pin.
31	(10)	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on Analog Common for more details. It also acts as a reference voltage source.

TC7136/A PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
33		(8)	C_{REF}^- See pin 34.
34	(7)	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	V_{REF}^-	See pin 36.
36	(5)	V_{REF}^+	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	(4)	TEST	Lamp test. When pulled HIGH (to V^+) all segments will be turned ON and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under Test for additional information.
38	(3)	OSC_3	See pin 40.
39	(2)	OSC_2	See pin 40.
40	(1)	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per second) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

GENERAL THEORY OF OPERATION

(All Pin designations refer to 40-Pin Dip)

Dual-Slope Conversion Principles

The TC7136/A is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7136/A operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period (t_{SI}), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (t_{RI}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

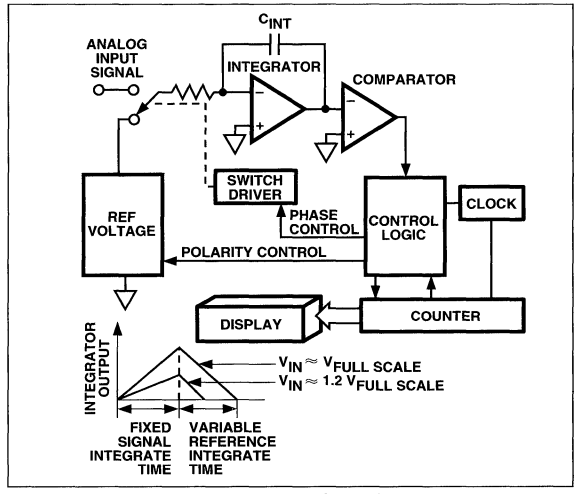


Figure 1 Basic Dual-Slope Converter

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right].$$

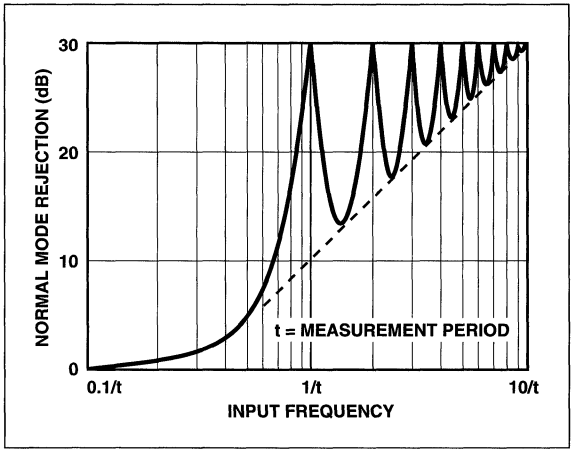


Figure 2 Normal-Mode Rejection of Dual-Slope Converter

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period.

ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7136/A designs incorporate an "integrator output-zero cycle" and an "auto-zero cycle." These additional cycles ensure the integrator starts at 0V (even after a severe overrange conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator output-zero phase
(2) Auto-zero phase
(3) Signal integrate phase
(4) Reference deintegrate phase

Integrator Output-Zero Phase

This phase guarantees the integrator output is at 0V before the system-zero phase is entered. This ensures that true system offset voltages will be compensated for even after an overrange conversion. The count for this phase is a function of the number of counts required by the deintegrate phase.

The count lasts from 11 to 140 counts for non-overrange conversions and from 31 to 640 counts for overrange conversions.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 μV to 15 μV.

The auto-zero duration is from 910 to 2900 counts for non-overrange conversions and from 300 to 910 counts for overrange conversions.

Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TC7136/A signal integration period is 1000 clock periods or counts. The externally-set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Phase

The third phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is bet-

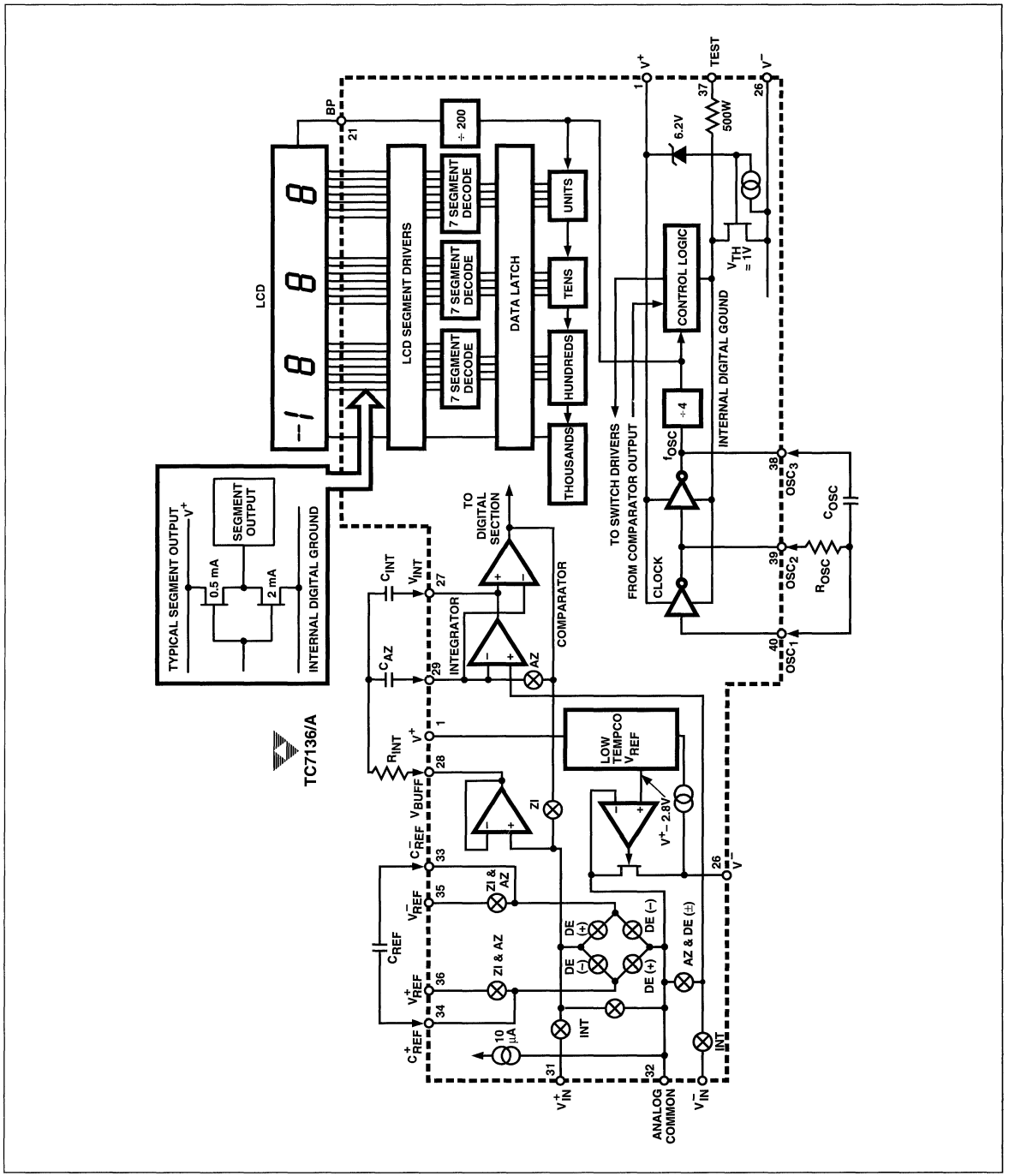


Figure 3 TC7136A Block Diagram

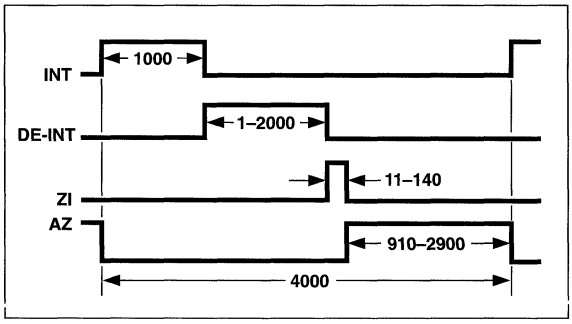


Figure 4 Conversion Timing During Normal Operation

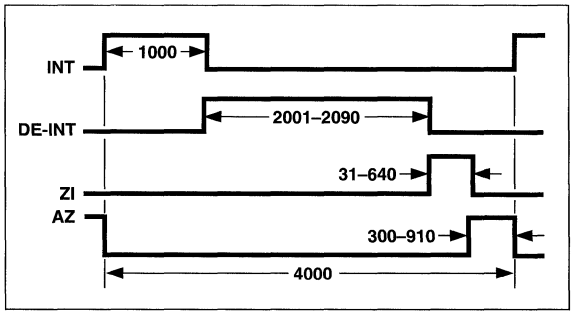


Figure 5 Conversion Timing During Overrange Operation

ween 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC7136/A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions per second the backplane frequency is 60 Hz with a 5V nominal amplitude. When a segment driver is in-phase with the backplane signal, the segment is OFF. An out-of-phase segment drive signal causes the segment to be ON, or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed, this indicator would reverse.

On the TC7136/A, when the TEST pin is pulled to V^+, all segments are turned ON. The display reads –1888. During this mode the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES. LCDS MAY BE DESTROYED IF OPERATED WITH DC LEVELS FOR EXTENDED PERIODS.

The display font and segment drive assignment are shown in Figure 6.

System Timing

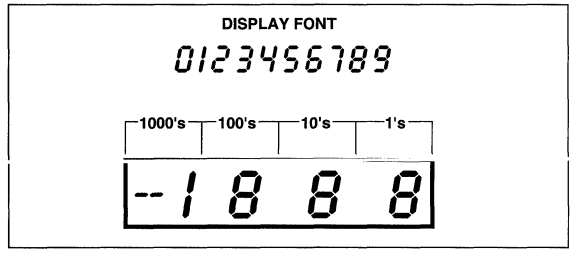


Figure 6 Display FONT and Segment Assignment

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts, or 16,000 clock pulses. The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 3000 to 2900 counts
(1200 to 11,600 clock pulses)

(2) Signal integrate: 1000 counts
(4000 clock pulses)

This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right],$$

where f_{OSC} is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts

(4) Zero integrator: 11 to 640 counts

The TC7136 is a drop-in replacement for the TC7126 and ICL7126. The TC7136A offers a greatly-improved internal reference temperature coefficient. Minor component value changes are required to upgrade existing designs and improve the noise performance.

COMPONENT VALUE SELECTION

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.1 µF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage, used to ramp the integrator output voltage back to zero during the reference integrate phase, is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- ≠ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 µF. Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference this case, a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second (f_{OSC} = 48 kHz) a 0.047 µF value is suggested. For one reading per second, 0.15 µF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 µA. The integrator and buffer can supply 1 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 kΩ. A 2V full scale requires 1.8 MΩ.

Component	Nominal Full-Scale Voltage	
Value	**200 mV**	**2V**
C_{AZ}	0.47 µF	0.1 µF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 µF	0.047 µF

NOTE: f_{OSC} = 48 kHz (3 readings per sec). R_{OSC} = 180kΩ, C_{OSC} = 50 pF.

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}.$$

Note that f_{OSC} is ÷4 to generate the TC7136A's internal clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*V_{FS} = 2 V_{REF}.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC7136/A is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is V^+ –1V to V^- +1V. Common-mode voltages are removed from the system when the TC7136A operates from a battery or floating power source (isolated from measured system), and V_{IN}^- is connected to analog common (V_{COM}). (See Figure 7.)

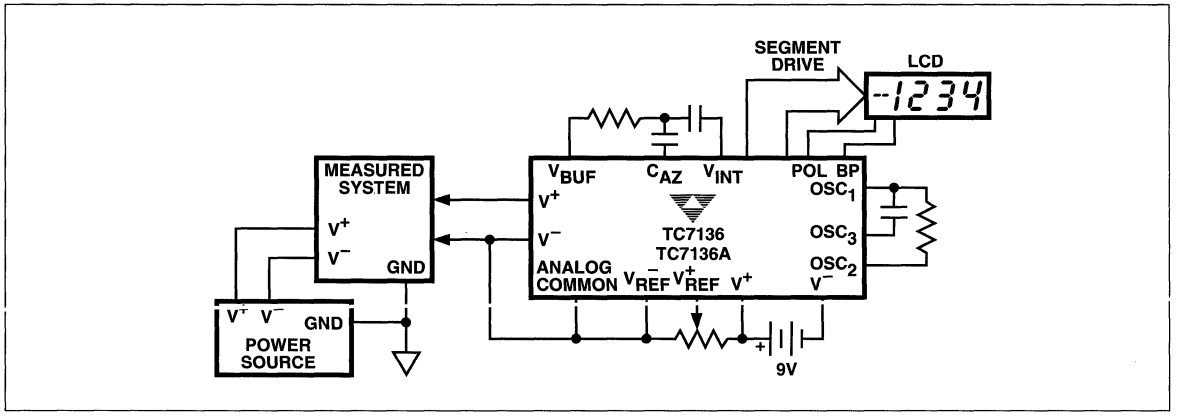


Figure 7 Common-Mode Voltage Removed in Battery Operation With V_{IN} = Analog Common

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 8.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

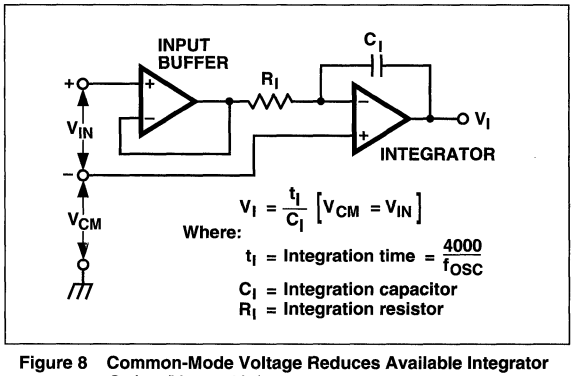


Figure 8 Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

The TC7136/A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C.

ANALOG COMMON (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. Analog common is tied internally to an N-channel FET capable of sinking 100µA. This FET will hold the common line at 3V below V^+ if an external load attempts to pull the common line toward V^+. Analog common source current is limited to 1 µA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ –3V).

The TC7136/A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero phase. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists, but is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference, or common point. The TC7136A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7136A power source. The analog common potential of V^+ –3V gives a 7V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient.

With sufficiently high total supply voltage (V^+–V^- >7V),

analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°c). for TC7136A This potential can be used to generate the TC7136A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See TC7136A Internal Voltage Reference discussion.

TEST (Pin 37)

The TEST pin potential is 5V less than V^+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The TEST pin load should not be more than 1 mA. See the Applications Section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled high (to V^+), all segments plus the minus sign will be activated. DO NOT OPERATE IN THIS MODE FOR MORE THAN SEVERAL MINUTES. With TEST = V^+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

TC7136A Internal Voltage Reference

The TC7136 analog common voltage temperature stability has been significantly improved (Figure 9). The "A" version of the industry-standard TC7136 device allows users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed; however, noise performance will be improved by increasing C_{AZ}. (See Auto-Zero Capacitor section.) Figure 10 shows analog common supplying the necessary voltage reference for the TC7136/A.

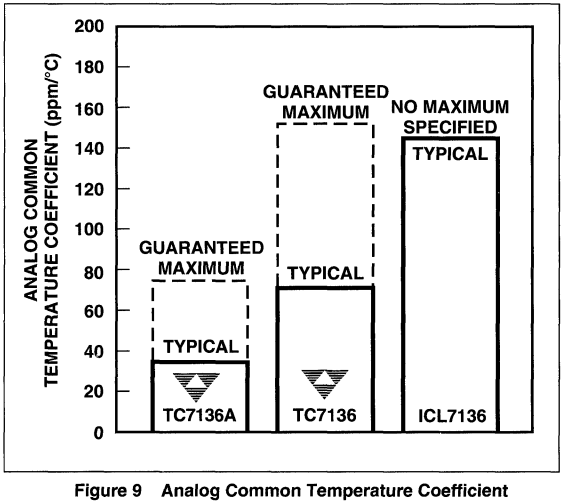


Figure 9 Analog Common Temperature Coefficient

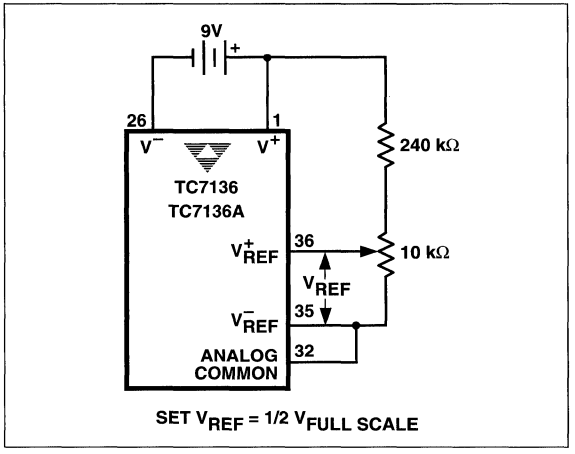


Figure 10 TC7136A Internal Voltage Reference Connection

APPLICATIONS INFORMATION

Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7136A 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	I1048, I1126
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the TEST pin: its potential is approximately 5V below V^+.

Ratiometric Resistance Measurements

The TC7136A's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

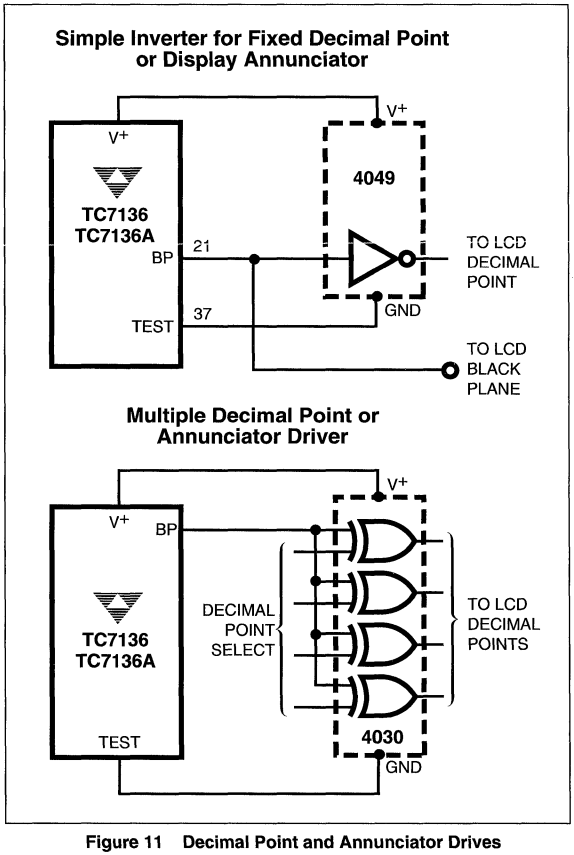


Figure 11 Decimal Point and Annunciator Drives

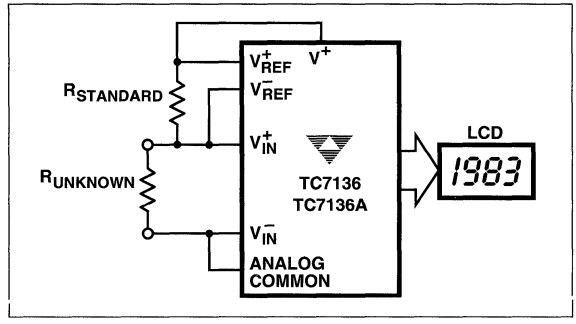


Figure 12 Low Parts Count Ratiometric Resistance Measurement

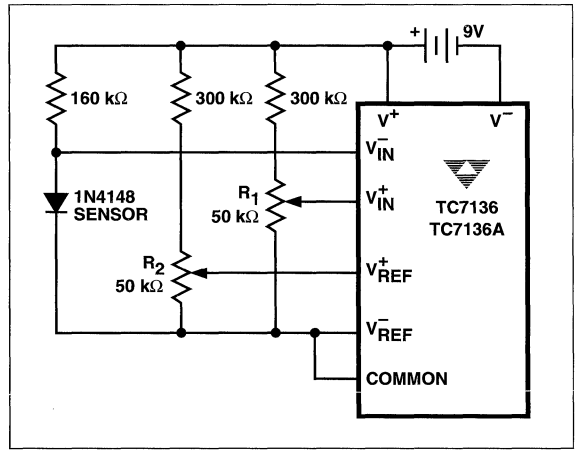
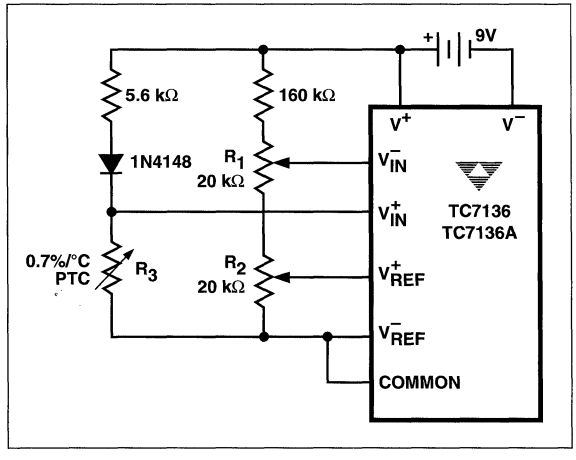


Figure 13 Temperature Sensor

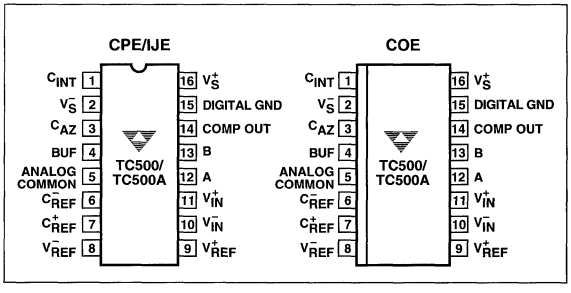


INTEGRATING CONVERTER ANALOG PROCESSORS

FEATURES

- **Resolution ..... (TC500) 50ppm Max (TC500A) 30ppm Max**
- **Differential Analog Input**
- **Differential Reference**
- **Low Linearity Error 0.003%**
- **Fast Zero-Crossing Comparator ..... 4 µs**
- **Low Power Dissipation ..... 10 mW**
- **Auto-Zero Cycle Eliminates Zero-Scale Error and Drift**
- **Zero Integrator Phase Speeds Recovery From Overrange Input Signals**
- **Automatic Internal Polarity Detection**
- **Low Input Current ..... 15 pA Max**
- **Wide Analog Input Voltage ..... ±4.2V**
- **Microprocessor Control of Dual-Slope ADC Conversion**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The CMOS TC500/TC500A contain all the analog circuits needed to construct an integrating analog-to-digital converter.

The user can control resolution and conversion speed through software. A microprocessor controls the TC500/TC500A through the A and B logic input signals. Four phases are possible: auto-zero, signal integrate, reference integrate (deintegrate), and integrator zero output.

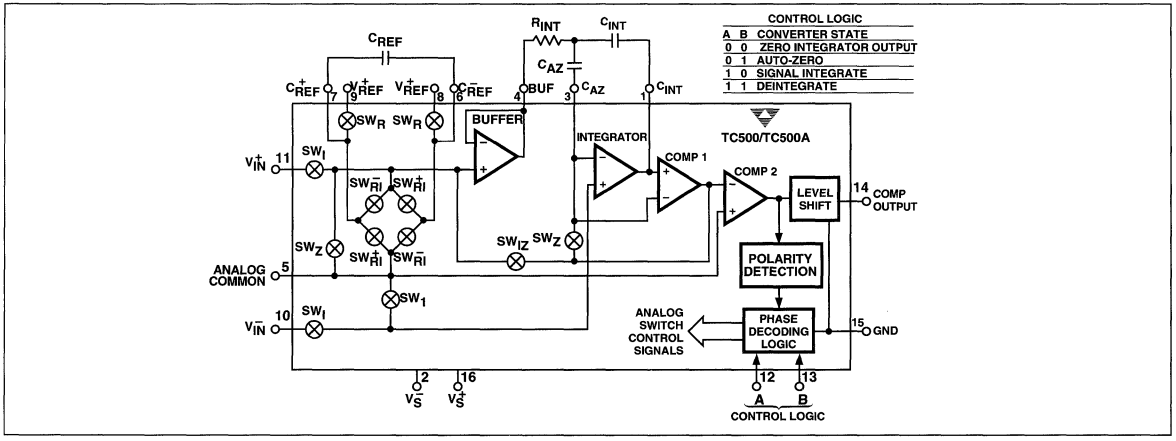
The TC500/TC500A contain the analog circuits needed to construct a dual-slope integrating converter with an auto-zero phase. A zero-integrator output phase can be selected to eliminate errors caused by out-of-range input signals. The zero-integrator phase greatly improves recovery after an overrange conversion.

The CMOS TC500/TC500A operate from ±5V supplies. Power dissipation is only 10 mW. Leakage currents at the differential inputs are a low 10 pA. The TC500/TC500A differential reference inputs allow easy ratiometric measurements.

ORDERING INFORMATION

Part No.	Package	Temperature Range	System Resolution
TC500ACPE	16-Pin Plastic DIP	0°C to +70°C	16-Bit (30 ppm)
TC500AIJE	16-Pin CerDIP	–25°C to +85°C	16-Bit (30 ppm)
TC500ACOE	16-Pin SO	0°C to +70°C	16-Bit (30 ppm)
TC500CPE	16-Pin Plastic DIP	0°C to +70°C	4-1/2 Digits (50 ppm)
TC500IJE	16-Pin CerDIP	–25°C to +85°C	4-1/2 Digits (50 ppm)
TC500COE	16-Pin SO	0°C to +70°C	4-1/2 Digits (50 ppm)

FUNCTIONAL BLOCK DIAGRAM



TC500
TC500A

ABSOLUTE MAXIMUM RATINGS*

Supply (V_S^+ to V_S^-) 18V
Positive Supply Voltage (V_S^+ to GND) ..... +12V
Negative Supply Voltage (V_S^- to GND) ..... –12V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) ..... V_S^+ to V_S^-
Logic Input Voltage ..... V_S^+ +0.3V to GND –0.3V
Package Power Dissipation 0.5W
Ambient Operating Temperature Range
Plastic Package (C) ..... 0°C to +70°C
CerDIP Package (I) ..... –25°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V_S = ±5V, unless otherwise specified. C_{AZ} = C_{REF} = 0.1 µF.

Symbol	Parameter	Test Conditions	TC500 Min	TC500 Typ	TC500 Max	TC500A Min	TC500A Typ	TC500A Max	Unit
Analog									
	Resolution	Note 1	—	—	50	—	—	30	ppm
ZSE	Zero-Scale Error	Note 1	—	—	0.005	—	—	0.003	%
ENL	End Point Linearity	Note 1	—	0.005	0.01	—	0.005	0.01	%
NL	Best Case Straight Line Linearity	Notes 1 and 2	—	—	0.005	—	—	0.003	%
DNL	Differential Nonlinearity		—	—	0.0025	—	—	0.0025	%
TC_{ZS}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range	—	1	2	—	1	2	µV/°C
SYE	Full-Scale Symmetry Error (Roll-Over Error)		—	—	0.01	—	—	0.006	%
	Ratiometric Reading	V_{IN} = V_{REF} = 1V	—	—	0.035	—	—	0.035	%
FS_{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference TC = 0 ppm/°C	—	—	10	—	—	10	ppm/°C
I_{IN}	Input Current	V_{IN} = 0V	—	6	15	—	6	15	pA
CMRR	Common-Mode Rejection Ratio	–1V ≤ V_{CM} ≤ 1V	—	80	—	—	80	—	dB
V_{CMR}	Common-Mode Voltage Range	V_S = ±5V	V_S^- +1.5	—	V_S^+ –1.5	V_S^- +1.5	—	V_S^+ –1.5	V
	Integrator Output Swing	V_S = ±5V	—	—	±4.1	—	—	±4.1	V
	Analog Input Signal Range		V_S^- +0.8	—	V_S^+ –0.8	V_S^- +0.8	—	V_S^+ –0.8	V
e_N	Noise	V_{IN} = 0V	—	30	—	—	30	—	μV_{P-P}
Digital									
	Reference Input Signal Range		V_S^- +1	—	V_S^+ –1	V_S^- +1	—	V_S^+ –1	V
V_{OH}	Comparator Logic 1, Output High	I_{SOURCE} = 800 µA	4	—	—	4	—	—	V
V_{OL}	Comparator Logic 0, Output Low	I_{SINK} = 4 mA	—	—	0.4	—	—	0.4	V
V_{IH}	Logic 1, Input High Voltage		3.5	—	—	3.5	—	—	V
V_{IL}	Logic 0, Input Low Voltage		—	—	1	—	—	1	V
I_L	Logic Input Current	Logic 1 or 0	—	0.05	—	—	0.05	—	µA
t_D	Comparator Delay		—	4	—	—	4	—	µs

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	TC500 Min	TC500 Typ	TC500 Max	TC500A Min	TC500A Typ	TC500A Max	Unit
Power									
I_S	Supply Current	V_S = ±5V, A = 1, B = 1	—	1	1.5	—	1	1.5	mA
P_D	Power Dissipation	V_S = ±5V	—	—	15	—	—	15	mW
V_S^+	Positive Supply Operating Voltage Range		4	—	10	4	—	10	V
V_S^-	Negative Supply Operating Voltage Range		–3	—	–8	–3	—	–8	V
V_S^+–V_S^-	Supply Operating Voltage Range		7	—	15	7	—	15	V

NOTES: 1. Integrate time ≥200 ms, auto-zero time ≥100 ms, V_{INT} (peak) ≈ 4V.
2. End point linearity at ±1/4, ±1/2, ±3/4 FS after full-scale adjustment.

OPERATIONAL THEORY

The TC500 and TC500A are dual-slope, integrating analog processors which are used with a microprocessor to generate analog-to-digital conversions of up to 16 bits of resolution. Although the TC500 and TC500A are virtually the same, the TC500A is recommended for applications requiring more than 14 bits of resolution.

The TC500 and TC500A incorporate a system zero phase and integrator output voltage zero phase, in addition to the normal two-phase, dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and shorter overrange recovery time result.

The TC500 and TC500A measurement cycle can use all four phases, if desired.

(1) Auto zero

(2) Analog input signal integration

(3) Reference voltage integration (deintegrate)

(4) Integrator output zero

Internal analog gate status is shown in Table I for each phase (see the functional diagram).

Auto-Zero Phase

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal integration Phase

The TC500/TC500A integrate the differential voltage between the (+) and (–) inputs. The differential voltage must be within the device's common-mode range.

The input signal polarity is normally checked via software at the end of this phase.

Table I. Internal Analog Gate Status

Conversion Phase	Internal Analog Gate Status SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}
Auto-Zero (A=0, B=1)				Closed	Closed	Closed	
Input Signal Integration	Closed						
(A=1, B=0)							
Reference Voltage		Closed*				Closed	
Deintegration (A=1, B=1)							
Integrator Output Zero					Closed	Closed	Closed
(A=0, B=0)							

*Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

Reference Voltage Deintegration Phase

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero.

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated. This phase is used at the end of the reference voltage deintegration (DEINT) phase and SHOULD be used for all TC500/TC500A applications. This phase MUST be used for resolutions of more than 14 bits. If this phase is not used, the value of the auto-zero capacitor (C_{AZ}) must be about 2 to 3 times the value of the integration capacitor (C_{INT}) to reduce the effects of charge-sharing. The integrator output zero phase should be programmed to operate until the output of the comparator returns "HIGH" (1) or for fixed time of about 2 ms.

ANALOG SECTION

Differential Inputs (V_{IN}^+ [Pin 11], V_{IN}^- [Pin 10])

The TC500/TC500A operate with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.8V below positive supply to 0.8V above negative supply. Within this common-mode voltage range, a common-mode rejection is typically 80 dB. Full accuracy is maintained, however, when the inputs are no less than 1.5V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced. The integrator output can swing within 0.9V of either supply without loss of linearity.

Analog Common (Pin 5)

Analog common is used as V_{IN} return during system-zero and reference deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, V_{IN}^- will be set at a fixed known voltage (i.e., power supply common). A common-mode voltage will exist when V_{IN}^- is not connected to analog common.

Differential Reference (V_{REF}^+ [Pin 9], V_{REF}^- [Pin 8])

The reference voltage can be generated anywhere within 1V of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (–) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A [Pin 12], B [Pin 13])

The A, B unlatched logic inputs select the TC500/TC500A operating phase. The A, B inputs are normally driven by a microprocessor I/O port or peripheral I/O chip.

Comparator Output

By monitoring the comparator output during the fixed-signal integrate time, the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is HIGH for positive signals and LOW for negative signals during the signal-integrate phase.

During the reference deintegrate phase, the comparator output will make a HIGH-to-LOW transition as the integrator output ramp crosses zero. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 4 µs, typically.

Figure 1 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is nonexistent. If common-mode noise is present, the comparator can switch several times during the signal-integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of signal integrate.

A "LOW" (0) on the TC500/TC500A comparator, during the deintegrate phase, signals the processor that the conversion is complete.

The comparator output is undefined during the auto-zero and the integrator output zero phases.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC500 is an integrating analog-to-digital converter building block. An understanding of the dual-slope conversion technique will aid in following the detailed TC500A operation theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

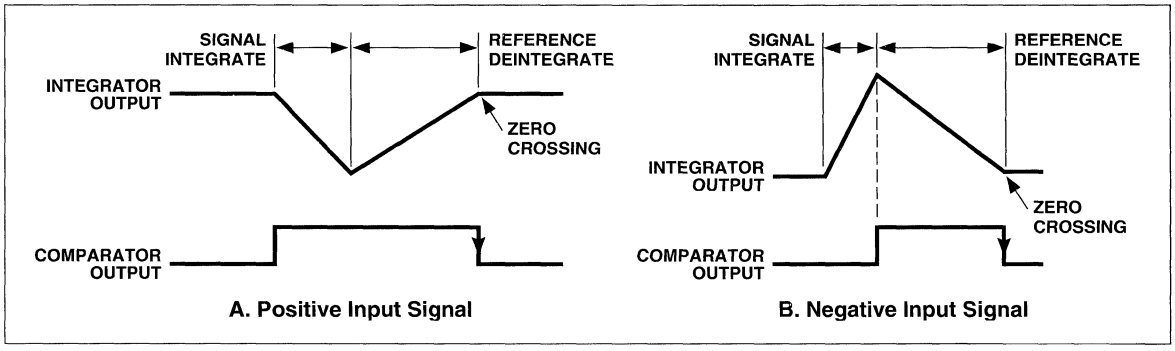


Figure 1. Comparator Output

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The TC500/TC500A automatically switch in the proper polarity reference signal. The reference integration time is directly proportional to the input signal (Figure 2).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down." The TC500/TC500A comparator zero-crossing signals the processor to indicate the deintegrate cycle is complete.

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

V_{REF} = Reference voltage
t_{INT} = Signal integration time (fixed)
t_{DEINT} = reference voltage integration time (variable)

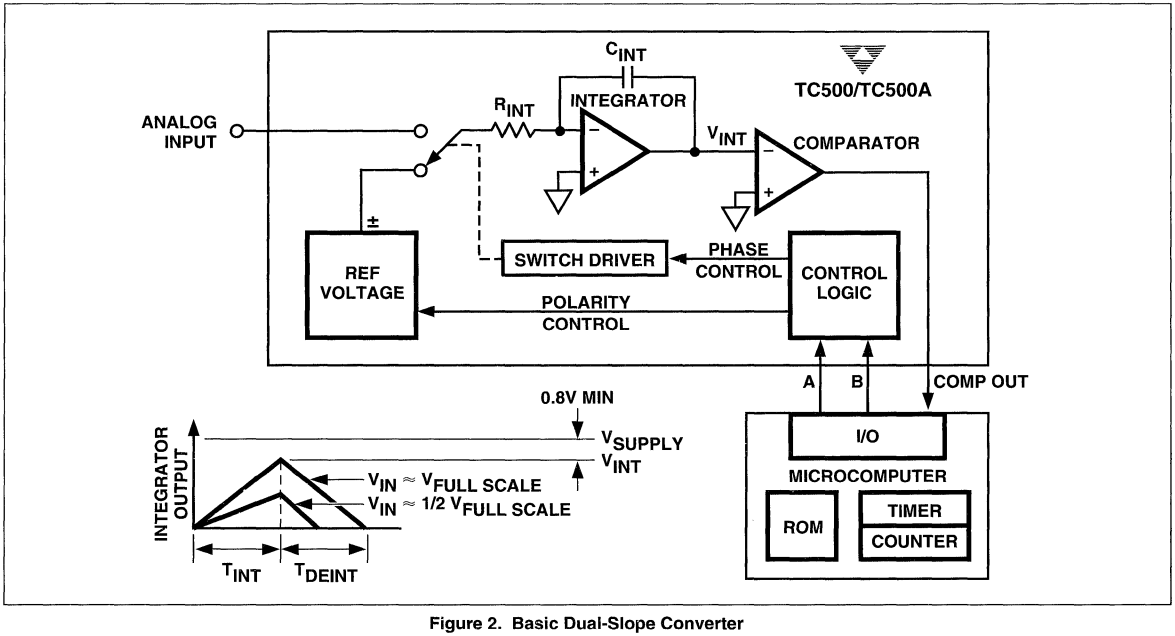


Figure 2. Basic Dual-Slope Converter

For a constant V_{IN}:

$$V_{IN} = V_{REF} \frac{t_{DEINT}}{t_{INT}}$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

Integrating converters provide noise rejection automatically with at least a 20-dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are, theoretically, completely removed. This intuitively makes sense, since the average value of a sine wave of frequency (1/t) averaged over a period (t) is zero.

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 3). Normal mode rejection is limited in practice to 50 to 65 dB, since the line frequency can deviate by a few tenths of a percent (Figure 4).

Criteria for C_{AZ} and C_{REF}

$$C_{AZ} \approx C_{REF} \approx \frac{2^N t_{INT} (V_{INT} + V_{REF}) I_{LEAKAGE}}{V_{INT} V_{REF}}$$

where:

N = resolution (bits)

$I_{LEAKAGE} \approx 15$ pA

V_{INT} (see Figure 2)

This equation is for reference only. Use 0.1 µF capacitor for all applications that have 8 or more conversions per second. Use a 0.22 µF capacitor for 3 to 7 conversions per second, and a 0.47 µF capacitor for conversions of 2 or less per second.

COMPONENT VALUE SELECTION

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20-µA drive current with minimal linearity error. R_{INT} is easily calculated for a 20-µA full-scale current:

$$R_{INT}\ (M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20} \quad \pm 20\%$$

For loop stability, R_{INT} should be ≥ 50 kΩ.

Reference Capacitor (C_{REF})

A 0.1-µF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors (such as polypropylene) are required.

Auto-Zero Capacitor (C_{AZ})

A 0.1-µF polypropylene capacitor is suggested.

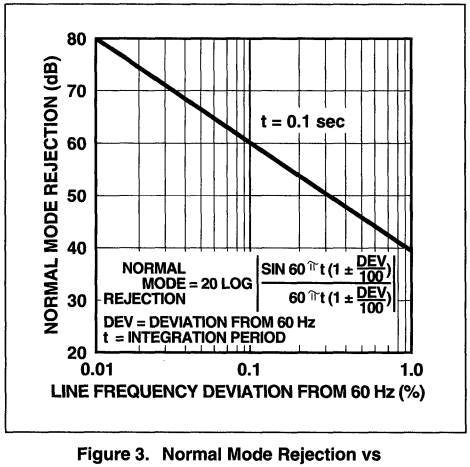


Figure 3. Normal Mode Rejection vs Input Frequency

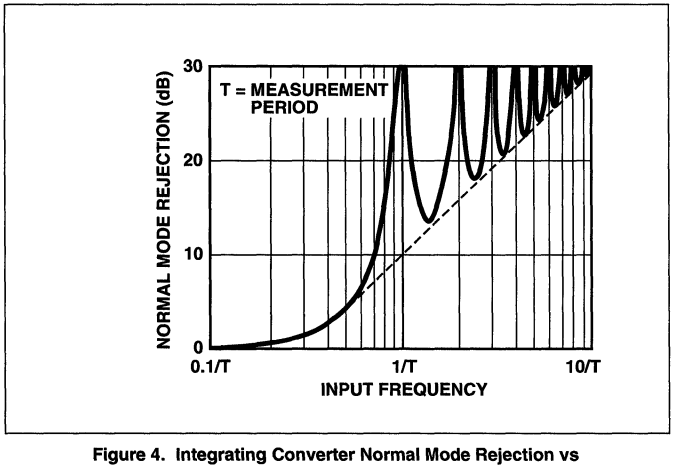


Figure 4. Integrating Converter Normal Mode Rejection vs 60 Hz Line Frequency Variations

2

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.8V of V_S^+ or V_S^- without saturating.

Using the suggested 20-μA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT} = \frac{(t_{INT})\,(V_{FS})}{(V_{INT})\,(R_{INT})} \approx 5\ t_{INT}\ (\mu F)$$

where:

t_{INT} = Integration period
V_{FS} = Full-scale input voltage
V_{INT} = Integrator output voltage swing

A very important integrating capacitor characteristic is dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polyester and polycarbonate capacitors may also be used in less critical applications.

The threshold noise (N_{TH}) is the algebraic sum of the integrator noise and the comparator noise. This value is typically about 30 μV. The graph shows how the value of the reference voltage can influence the results of the final count.

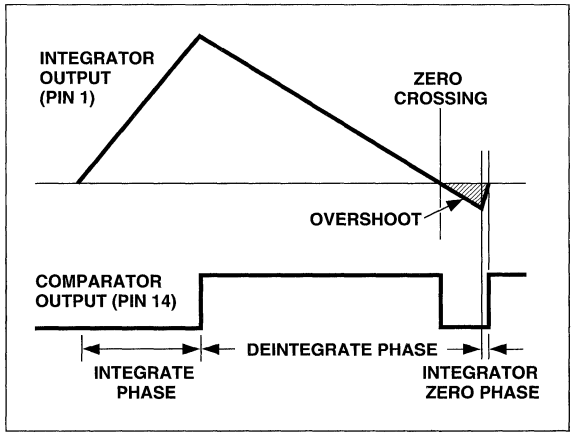
Errors caused by the low-frequency buffer noise may be reduced by increased integration times.

Signal-to-Noise Ratio

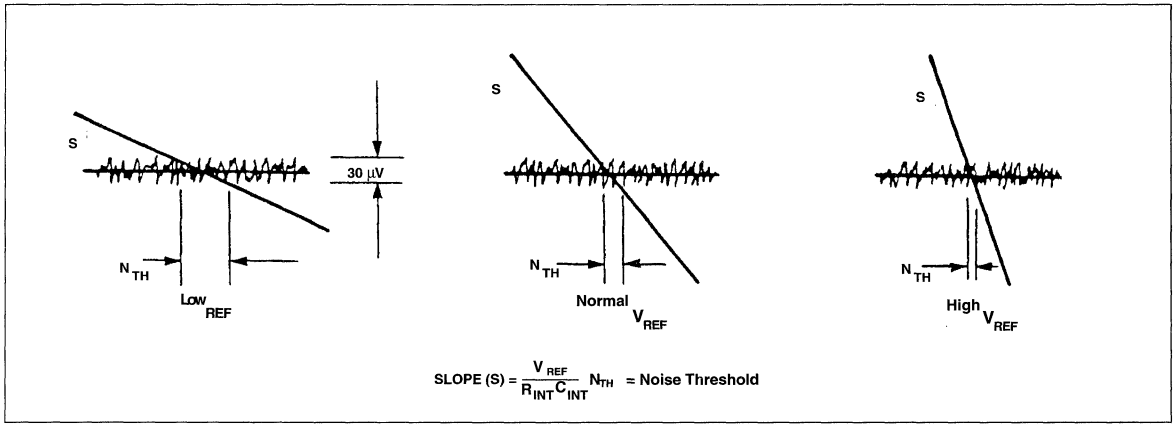
$$S/N\ (dB) = 20\ Log\left(\frac{V_{IN}}{30\ \mu V} \bullet \frac{t_{INT}}{R_{INT} \bullet C_{INT}}\right)$$

The maximum performance of the TC500/TC500A require that overshoot at the end of the deintegration phase be minimized. Also, the integrator zero phase may be terminated as soon as the comparator output returns to HIGH (1).

OVERSHOOT

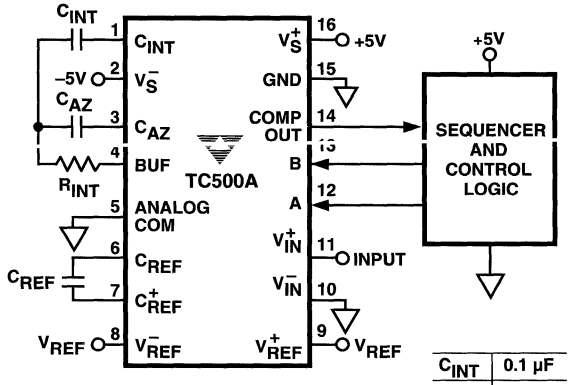


NOISE



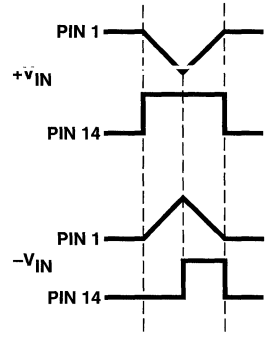
TC500A DESIGN EXAMPLE (See "Component Selection Example")

TIMING CONDITIONS: A) AZ PLUS ZI.....10,000 CLOCK PERIODS (40 ms)
B) INT.....10,000 CLOCK PERIODS (40 ms)
C) DEINT.....V_{IN} (V) 10,000 CLOCK PERIODS (14 bits)
D) CLOCK PERIOD.....4 µs
E) V_{FS}.....±2.5V

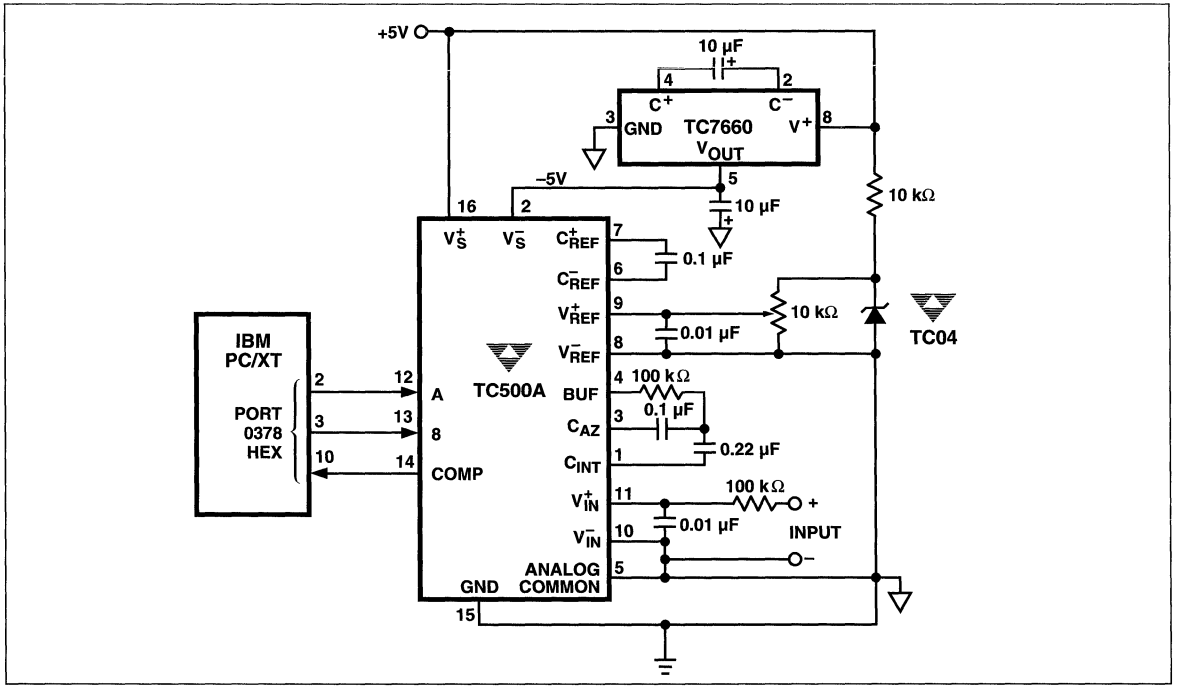


C_{INT}	0.1 µF
R_{INT}	250 kΩ
C_{AZ}	0.1 µF
C_{REF}	0.1 µF

TYPICAL WAVEFORMS



TC500A TO IBM PC/XT PRINTER PORT



Interrupt Operation

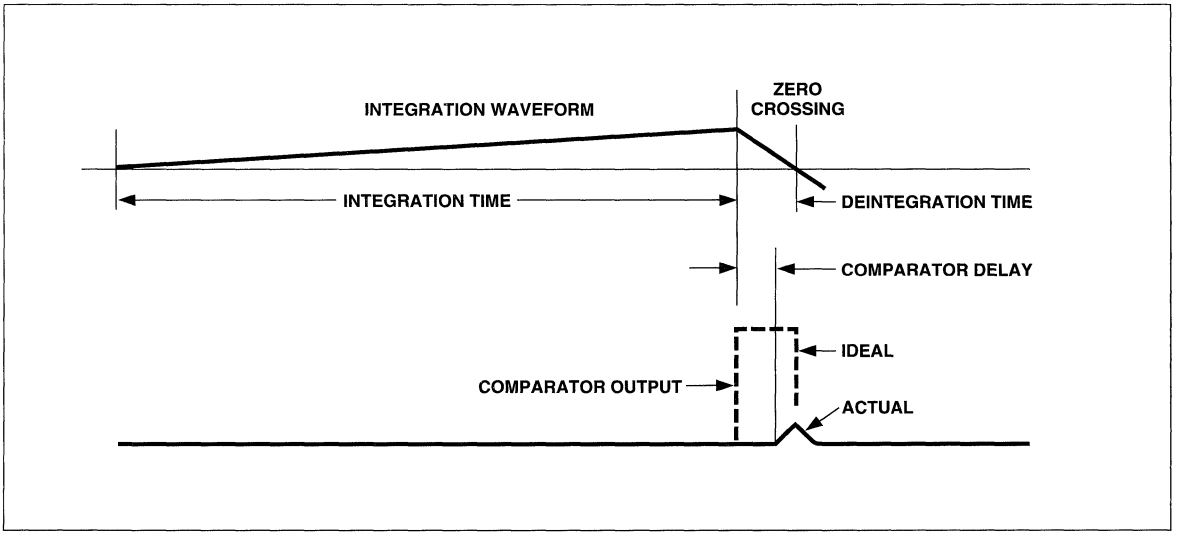
The comparator output stays low during the Integration phase (A=1, B=0) whenever the input polarity is negative. In those cases where the input polarity is negative AND very near zero, the zero-crossing occurs before the comparator has had a chance to go positive. Thus, no negative edge will be generated and the microprocessor will not be interrupted.

With a negative input voltage very near zero, the output of the comparator does not have enough time to get fully positive. This anomaly is caused by the comparator delay and rise time limitations.

One solution to overcome this condition is to have the microprocessor monitor the comparator output. It can then end the deintegration phase as soon as it sees a zero.

Another solution is to have the microprocessor enable the interrupt and look at the comparator output. If the output is HIGH, the interrupt will be properly triggered. If the output is LOW, end the deintegration phase and disable the interrupt.

Either solution will produce reliable low voltage conversions.



Rate of Conversion

The conversion times for the TC500/TC500A are a function of many variables and constants. The dominant component is C_{INT}:

$$\text{Conversion Time (sec)} = 0.4 \times C_{INT}\ (\mu F) \times (2 + (V_{IN}/V_{REF}))$$

The assumptions for this equation are suggested but not strictly required. They are:

Auto-zero time (T_{AZ}) = Integration time (T_{NT})
Peak integration voltage (V_{INT}) = 4V
Maximum buffer current ($V_{IN(MAX)}/R_{INT}$) = 20 µA

Component Selection Example

Known:

1)	Supply voltage for TC500A	(V_{SUP})
2)	Maximum input voltage	($V_{IN(MAX)}$)
3)	Integration time	(T_{INT})
4)	Output resolution (bits)	(N)
5)	Clock period	(t_{CLOCK})

Assume:

$V_{SUP} = \pm 5V$	$V_{SUP} = \lvert V_{SUP}\rvert$
$V_{IN(MAX)} = \pm 2.5V$	$V_{IN(MAX)} = \lvert V_{IN(MAX)}\rvert$
T_{INT} = 40 ms	
N = 14 bits	
t_{CLOCK} = 4 µs	

Step 1: Calculate R_{INT} $\quad R_{INT} = \dfrac{V_{IN(MAX)}}{I_{BUF(MAX)}}$

Where $I_{BUF(MAX)} \approx 20\ \mu A$

$$R_{INT} = \frac{2.5V}{20\ \mu A} = 125K$$

Use 130K

$$\therefore I_{BUF} = \frac{2.5V}{130K} = 19.2\ \mu A$$

Step 2: Calculate C_{INT} $\quad C_{INT} = \dfrac{T_{INT}\, I_{BUF(MAX)}}{V_{INT}}$

Where $V_{INT} = V_{SUP} - 1V = 4V$

$$C_{INT} = \frac{40\ ms\ 19.2\ \mu A}{4V} = 0.192\ \mu F$$

Use 0.2 µF

Step 3: Calculate V_{REF} $\quad V_{REF} = \dfrac{V_{INT}\, C_{INT}\, R_{INT}}{T_{DEINT}}$

Where $K_{DEINT} = 2^N\, t_{CLOCK}$

$$V_{REF} = \frac{4V \bullet 0.2\ \mu F \bullet 130K}{2^N\, t_{CLOCK}} = 1.587...V$$

Step 4: Calculate integrate count $\quad K_{INT} = \dfrac{T_{INT}}{t_{CLOCK}}$

Where $K_{INT}\ \dfrac{40\ ms}{4\ \mu s} = 10{,}000$ Counts

Results: $K_{DEINT} = V_{IN}\ \dfrac{K_{INT}}{V_{REF}} = V_{IN}\ \dfrac{10{,}000}{1.587...V}$

Where K_{DEINT} = Number of clock periods during T_{DEINT}

Normalization

The reference voltage can be adjusted to scale the deintegrate count to be directly equivalent to the input voltage.

Since: $\dfrac{K_{INT}}{V_{REF}}$ = Counts/Volt

If: V_{REF} is adjusted such that

$$V_{REF} = \frac{10000\ Counts}{10000\ Counts/Volt} = \frac{K_{INT}}{10000\ Counts/Volt} = 1V$$

Then: $K_{DEINT} = \dfrac{V_{IN}}{100\ \mu V}$ and $N \approx 14.61$ Bits

e.g., If $K_{DEINT} = 18357$ Counts,
then $V_{IN} = 1.8357V$

16-BIT SERIAL INTERFACE CONTROLLER FOR TC500 AND TC500A

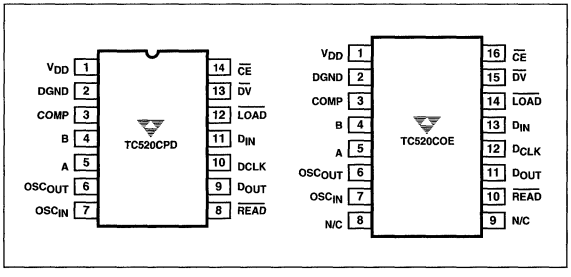
FEATURES

- **Up to 16-Bits of Resolution**
- **Independent Data Clock Rate**
- **Binary Data Output**
- **Programmable Conversion Rate**
- **"Visible" Overrange Bit**
- **Double Buffered Data Latch**
- **On-Chip Oscillator Circuit**
- **Serial Data for Compact Circuits**
- **"Overrange" may be used as 17 Bit**
- **14-Pin DIP or 16-Pin SMD**
- **HiZ Output on D_{OUT} when not selected**

ORDERING INFORMATION

Part No.	Package	Operating Temp Range
TC520CPD	14-Pin DIP	0°C to +70°C
TC520COE	16-Pin SOIC (Wide)	0°C to +70°C

PIN CONFIGURATION



GENERAL DESCRIPTION

The TC520 Serial Interface Controller provides complete logic control for the TC500 or TC500A Analog Processors in a compact 14 or 16 pin package. The TC520 contains a programmable "Auto-Zero" and "Integrate" time, and 16-bit "results" counter. The TC520 controls the "A" and "B" inputs to the TC500A for each one of the four conversion phases.

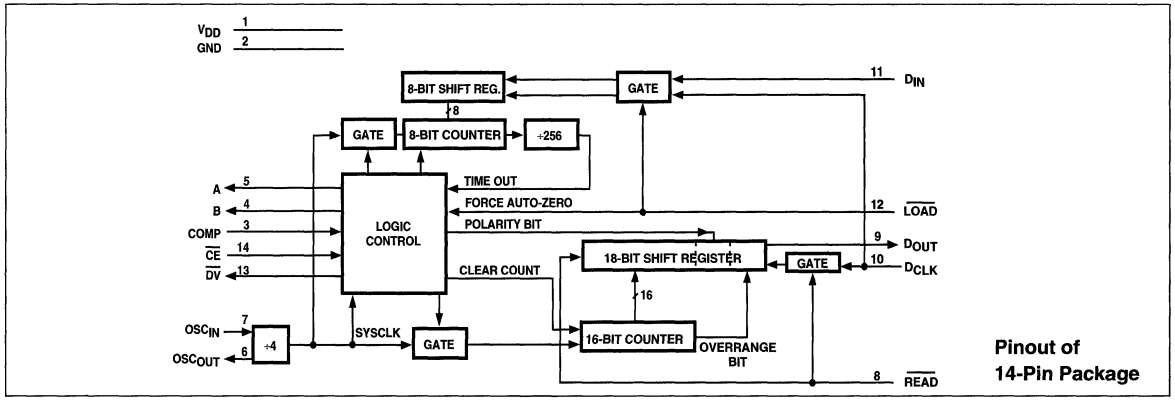
An 18-bit shift register holds the 16-bit conversion data plus the sign bit and overrange bit until it is read or until the next conversion has been completed. The shift register data will not update while data is being read from the TC520 although the TC500 will continue to convert. Some or all of this serial information may be clocked out at any time and at any rate that the user prefers.

The TC520 may operate from the system clock, its own external crystal, or any other appropriate source. The timing of the conversion phases of the TC500/A are determined by the TC520's frequency of operation and may be completely independent of the microprocessor clock rate.

The TC520 allows full flexibility of the TC500 or TC500A by providing programmable auto zero and integrate timing. The timing is determined by a 16-bit counter which is made up of an 8-bit counter (÷256) and an 8-bit multiplier (÷N) working in series. The TC520 supports multiple conversion rate applications by allowing the 8-bit multiplier to be modified under software control through a serial interface.

The CMOS TC520 operates from a single 5V supply. Power dissipation is less than 7.5mW.

FUNCTIONAL BLOCK DIAGRAM



Pinout of 14-Pin Package

NOTE: All electrical data is included for reference only. Values are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage (V_{DD}) ..... –0.5 to +6.0
Input Voltage, All Inputs (V_{IN}) ..... –0.5 to V_{DD} +0.5
Operating Temperature Range (T_A) ..... –25°C to +85°C
Storage Temperature Range (T_{STG}) ..... –65°C to +150°C
Lead Temperature (10 sec) (T_{SDR}) ..... 300°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Operational Specifications is not implied. Any exposure to Absolute Maximum Rating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS: unless otherwise specified V_{DD} = 5V, f_{osc} = 1 MHz, T_A = +25°C:

Parameter	Symbol	Min	Typ	Max	Unit
Supply					
Operating Voltage Range	V_{DD}	4.5	5	5.5	V
Supply Current	I_{DD}	–	0.8	1.5	mA
Input Characteristics					
Input Voltage Range	V_{IR}	–0.3	–	V_{DD} +0.3	V
Low Input Voltage	V_{IL}	–	–	1.0	V
High Input Voltage	V_{IH}	2.5	–	–	V
Input Leakage Current	I_{ILC}	–	–	10	µA
Pull-down Current (CE)	I_{PD}	–	5	–	µA
Pull-up Current (READ, LOAD)	I_{PU}	–	5	–	µA
Output Characteristics (I_{OUT} = 250 µAmps, V_{DD} = 5V)					
Low Output Voltage	V_{OL}	–	0.2	0.3	V
High Output Voltage	V_{OH}	3.5	4.3	–	V
Rise/Fall Times	C_L = 10pF	–	–	250	nsec
Oscillator (OSC_{IN}, OSC_{OUT})					
Crystal Frequency	f_{xtl}	–	1.0	4.0	MHz
External Frequency (OSC_{IN})	f_{osc}	–	–	6.0	MHz
Timing Characteristics					
READ Delay Time	t_{RD}	250	–	–	nsec
Data Read Setup Time	t_{RS}	1	–	–	µsec
D_{CLK} to D_{OUT} Delay	t_{DRS}	450	–	–	nsec
LOAD Setup Time	t_{LS}	1	–	–	µsec
Data Load Setup Time	t_{DLS}	50	–	–	nsec
D_{CLK} Pulse Width Low Time	t_{PWL}	150	–	–	nsec
D_{CLK} Pulse Width High Time	t_{PWH}	150	–	–	nsec
Load Default Low Time	t_{LDL}	250	–	–	nsec
Load Default Setup Time	t_{LDS}	250	–	–	nsec

GENERAL DESCRIPTION

Basic Timing: The crystal oscillator and clock input circuit has a divide-by-4 prescaler which generates the internal system clock (SYSCLK). All of the timing operations of the TC520 are controlled by SYSCLK.

Auto-Zero (AZ) and Integrate (INT) Timing: There is one 16-bit binary counter which controls the timing of both the auto-zero phase and the integration phase of the TC500/A. The lower 8 bits of this up-counter always divides by 256 and the upper 8 bits has a default value of 128 or 256. This results in a default AZ and INT timing of 32768 (256 x 128) or 65536 (256 x 256) SYSCLK periods.

Serial Data Input: The upper 8 bits of the auto-zero/integrate counter may be pre-loaded by shifting a new 8-bit byte (MSB first) into the TC520. This gives the user a range of counts from 256 to 65536 in steps of 256.

Serial Data Output: An 18-bit output shift register includes overrange bit, a sign bit and 16 bits of conversion data. An overrange bit is visible on the D_{OUT} pin without clocking the data. An overrange conversion may be ignored or may be used as the MSB for 17 bits of resolution. The serial data may be read at any time because the data clock is independent of the conversion cycle. The internal data latch will not update while $\overline{READ}$ is held LOW.

Chip Enable ($\overline{CE}$): A HIGH on the chip enable pin will force the TC500A into the auto-zero (AZ) state (A=0, B=1). This is the proper phase for idling the TC500/A and still having it ready for the next conversion.

Comparator (COMP): The comparator input is used by the TC520 to determine the polarity of the voltage input to the TC500A and to determine the end-of-conversion zero-crossing.

Data Clock (D_{CLK}): The data clock input from the host µP is used to clock in the 8-bit multiplier of the auto-zero/integration counter on the data input pin (D_{IN}), or to clock out the 18 bit of conversion data from the data output pin (D_{OUT}). This data clock is independent of the system clock (SYSCLK).

Load Integrate Count ($\overline{LOAD}$): The leading edge (negative transition) of the LOAD input clears the high-byte shift register of the auto-zero/integrate counter and the state of the data input pin (D_{IN}) is loaded into the MSB. The A and B outputs to the TC500/A are forced to the auto-zero phase whenever LOAD is pulled LOW.

Data Input (D_{IN}): An 8-bit data word may be clocked into the high-byte shift register of the auto-zero/integration counter using the data clock (D_{CLK}) whenever LOAD is LOW. The auto zero and integrate times will be equal to 256 times the 2's complement of the 8-bit value loaded into the high-byte shift register (MSB first).

Data Output (D_{OUT}): The overrange bit appears on the data output pin whenever READ goes LOW. The first negative transition of the data clock (D_{CLK}) will clock the polarity bit to D_{OUT}. Subsequent negative transitions on D_{CLK} will clock out the conversion data (MSB first).

PIN DESCRIPTIONS

PIN#*		DESCRIPTION
1	(1)	**V_{DD}**, Positive Supply.
2	(2)	**DGND**, Digital Ground.
3	(3)	**COMP**, Connected to comparator output of TC500A. Controls the timing of the TC520.
4	(4)	**OUTPUT B**, "B" Input to TC500/A.
5	(5)	**OUTPUT A**, "A" Input to TC500/A.
6	(6)	**OSC_{OUT}**. Output of the internal crystal controlled oscillator. Connect to one side of the crystal or must be left open if a clock input is used on OSC_{IN}.
7	(7)	**OSC_{IN}**, Input of the internal crystal controlled oscillator. Connect to one side of the crystal or a clock input may be used instead.
	(8)	N/C.
	(9)	N/C.
8	(10)	**$\overline{READ}$**, Logic LOW enables the output shift-register. D_{CLK} can clock out the deintegrate count of the most recent conversion cycle to D_{OUT}.
9	(11)	**D_{OUT}**, Conversion data serial output. The overrange bit of the most recent conversion is available without strobing D_{CLK}. The sign bit and the 16 conversion bits (MSB first) may be clocked out with D_{CLK} when $\overline{READ}$ is set LOW.
10	(12)	**D_{CLK}**, The data clock is used to clock in the required integration counts (default = 2^{15}) or to clock out the conversion data.
11	(13)	**D_{IN}** , Integrate count serial input. An 8-bit (or less) serial input word (MSB first) will be multiplied by 256 to determine the integration count for the TC500/A.
12	(14)	**$\overline{LOAD}$**, Logic LOW enables input shift register. D_{CLK} can clock in the integrate count multiplier on D_{IN}.
13	(15)	**$\overline{DV}$**, LOW transition indicates new conversion data is ready.
14	(16)	**$\overline{CE}$**, Logic LOW selects TC520. If CE is HIGH then the TC500/A is forced into the auto-zero mode.

*Pin # on left for 14-pin DIP package, on right for 16-pin SMD (SO) package.

THEORY OF OPERATION

Load Auto-Zero/Integrate Timing Register Value ($\overline{LOAD}$, D_{IN}, D_{CLK})

One of two default values is entered if $\overline{LOAD}$ is pulsed LOW and no value is clocked into the shift register. The state of the data input pin (D_{IN}) is loaded into the MSB of the high-byte shift register. If D_{IN} is HIGH then the normal default count of 32768 is established. If D_{IN} is LOW then the count will be set to 65536.

The auto-zero and integrate timing may be changed to any value between 65536 counts of the system clock (SYSCLK) to 256 counts of SYSCLK in 256-count steps. With $\overline{LOAD}$ held LOW, an 8-bit data word can be clocked into the high-byte shift register of the auto-zero/integration counter with positive transitions on the data clock (D_{CLK}). The 8-bit word is clocked in MSB first. The auto zero and integrate times will be equal to 256 times the 2's complement of the 8-bit value loaded into the high-byte shift register.

AZ and INT Counts	Auto-Zero/Integrate High-Byte Counter								8 Bit HEX
	MSB	•••	•••	•••	•••	•••	•••	LSB	
65536 (1)	0	0	0	0	0	0	0	0	00
49152	0	1	0	0	0	0	0	0	40
32768 (2)	1	0	0	0	0	0	0	0	80
16384	1	1	0	0	0	0	0	0	C0
8192	1	1	1	0	0	0	0	0	E0
4096	1	1	1	1	0	0	0	0	F0
2048	1	1	1	1	1	0	0	0	F1
1024	1	1	1	1	1	1	0	0	FC
512	1	1	1	1	1	1	1	0	FE
256	1	1	1	1	1	1	1	1	FF

Effect of the High-Byte Value on the Auto-Zero/Integrate Timing Default Counts (1) D_{IN} = LOW, (2) D_{IN} = HIGH

"A" (Pin 5) and "B" (Pin 4)

The A and B outputs from the TC520 connect directly to the A and B inputs of the TC500/A. These control the timing and phasing operation of the TC500/A.

Read Conversion Value ($\overline{READ}$, D_{OUT}, D_{CLK})

The serial data output of the TC520 consists of 18 bits of information. The Data Output pin (D_{OUT}) stays as a high impedance state until $\overline{READ}$ is selected. A HIGH-to-LOW transition on the $\overline{READ}$ input loads the output shift register with the most recent 16-bit conversion data, the overrange bit (OVR) and the polarity bit (POL). The first bit on the output shift register is the overrange bit which is available as soon as $\overline{READ}$ is LOW. This bit may be used as the MSB when a 17-bit conversion result is required. This bit does not require clocking the D_{CLK} input.

The rest of the information is clocked out by negative transitions on the data clock (D_{CLK}) while $\overline{READ}$ is held LOW. The first bit clocked out is the polarity bit (HIGH = input positive, LOW = input negative). The remaining 16 bits represent the conversion value in binary form, MSB first. Excess $D_{CLK's}$ will produce zero - value bits.

The Conversion Value may be read at any time during the conversion process or the $\overline{DV}$ output may be used to trigger an interrupt. The conversion cycles of the TC500/A are unaffected by the reading sequence but the serial data output shift register will not update as long as $\overline{READ}$ is LOW.

The $\overline{READ}$ cycle may be terminated at any time by bringing $\overline{READ}$ to HIGH.

Oscillator Circuit

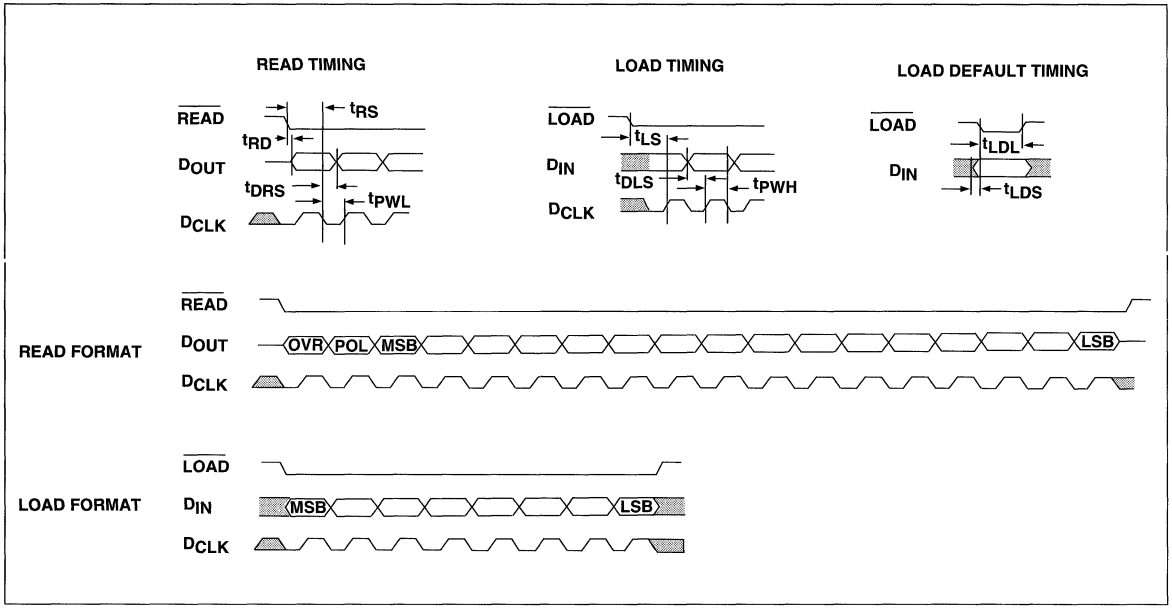
A crystal oscillator circuit is included on the TC520 which will work up to 4MHz. An external clock may also be applied to OSC_{IN} (Pin 7). An internal ÷4 generates the system clock (SYSCLK) which is used to time the auto-zero and integrate phases of the TC500A and is used as the count-rate for the conversion data (results) counter.

Power-On Considerations

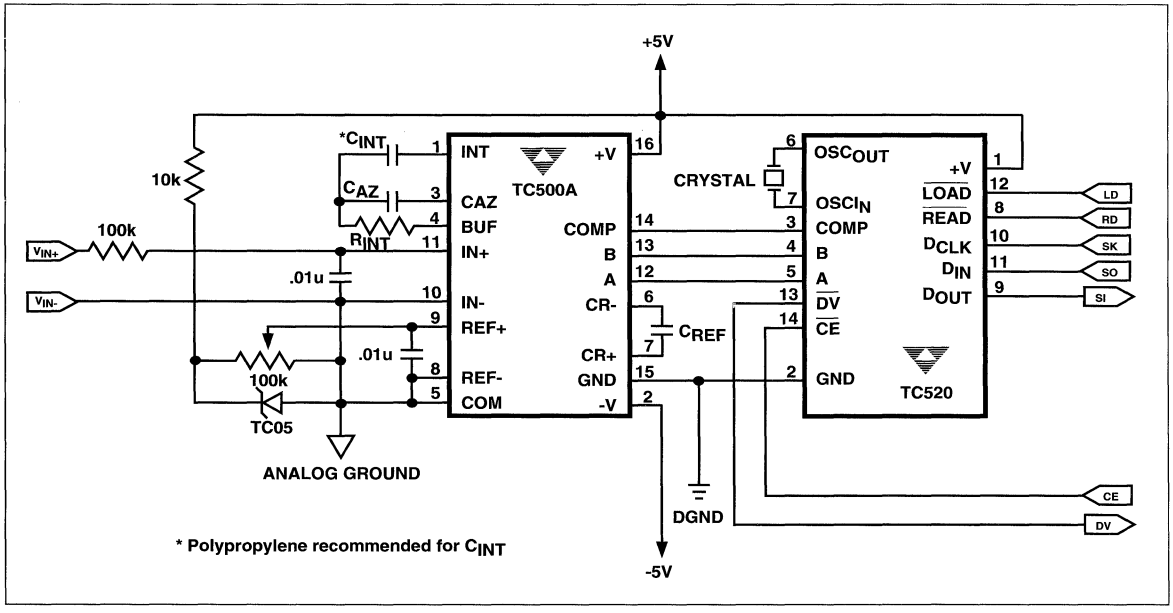
At power-on, the TC520 comes up with the A and B lines at zero (IZ phase) and is waiting for the TC500 comparator to go LOW. The TC500 is, unfortunately, hung-up at this point and will not respond.

There are two ways to force a momentary auto-zero mode to overcome this condition: 1) have the micro strobe LOW on the $\overline{LOAD}$ or $\overline{CE}$ input, or 2) put a small capacitor (≈0.01µF) from $\overline{CE}$ to V_{CC}. There is an internal pull-down current on $\overline{CE}$ which will reactivate the TC520.

TIMING DIAGRAMS



TYPICAL TC520 INTERFACE TO TC500 OR TC500A



USING THE TC520

Conversion Timing and Component Selection

The values of R_{INT}, C_{INT}, C_{REF}, C_{AZ} and V_{REF} for the TC500 or TC500A are selected by using the criteria spelled out in the TC500/A data sheet to fit your specific application. The only external constraint, when using the TC520, is the value used for T_{INT} (integration time) in your calculations. This time will now be a function of the crystal or clock you use for timing the TC520.

The TC520 generates a system clock (SYSCLK) used for timing and counting by dividing the crystal frequency by 4. You will need to use the period of SYSCLK (for t_{sk}) to determine T_{INT}. The TC520 can use from 256 (2^8) to 65536 (2^{16}) counts of (t_{sk})t for the integrate time. The two default values are 2^{15} and 2^{16}. If you conform to conventional dual-slope wisdom, you will select 2^{15} ($2^{16}/2$) as your integrate count. A value of 4µs for t_{SK} will minimize the error due to the comparator delay of the TC500/A so a 1MHz crystal (or clock) is advisable.

With an integrate count of 2^{15} (32768) and SYSCLK of 250KHz, your integration time (T_{INT}) will be 131ms. This time period is also used to control the auto-zero time (T_{AZ}). The maximum deintegration time (T_{DEINT}) will be 2 x T_{INT}, or 262ms. This will make your total maximum conversion time (full-scale input) be 524ms. That is 1.9 to 3.8 conversion per second.

The value of the reference voltage (V_{REF}) is determined by T_{INT} and the maximum input voltage (V_{IN} MAX):

$$V_{REF} = V_{IN}\,MAX \times T_{INT}/T_{DEINT}$$

Maximum 50/60Hz line rejection is achieved when T_{INT} is 100ms. This would result in a t_{SK} of 3µs. The worst TC500/A comparator delay is not likely to be greater than 3.2µs so the effect would be virtually impossible to detect. Your full-scale conversion rate would be 2.5 conversions per second with a practically undiscernable anomaly at V_{IN} = 0.

You can control the integration and auto-zero timing of the TC520 by loading a specific 8-bit number into its timer through a serial interface. The timer is an "up" counter so the timing decreases when larger numbers are loaded. If, for example, you had a 1MHz clock (t_{SK} = 4µs) but still wanted the integration time (T_{INT}) to be ≈100ms instead of 131ms, then you would serially load a value of $9E_H$ into the TC520. If you wanted the same T_{INT} with a 2MHz clock (t_{SK} = 2µs) then the number would be $3D_H$. The formula for this calculation is:

$$LOAD\ VALUE = (2^{16} - (T_{INT}/t_{SK}))/2^8$$

Chip Enable and Start-Up

The chip enable ($\overline{CE}$) input does not really enable the chip. What it does is allow the TC500/TC520 to do conversions as long as it is LOW. This input has a "pull-down" current so no external connection is required for operation. If you pull CE high, the TC520 will force the TC500 into the auto-zero mode. This is an advisable precaution whenever you switch an input multiplexer or suspend conversions for other considerations.

The logic flow chart shows that the TC520 starts out in the Zero Integrate phase. It then waits for the comparator on the TC500 to go HIGH. Most (or all) of the time, on "power-up," the TC500 hangs up with the comparator output LOW. There are two known solutions to this problem: 1) Use $\overline{CE}$ to force an auto-zero phase during initialization, or 2) Connect a 1000pF capacitor between $\overline{CE}$ and V_{DD}. This will force the AZ phase on the TC500 until the internal current sink discharges the capacitor. The capacitor technique is especially desirable in opto-isolated applications.

Opto-Isolated Applications

The TC500/TC520 combination is ideally suited for opto-isolation because they operate autonomously as a pair. You only need 3 opto-isolated lines between the TC520 and the microprocessor to read the conversion data, i.e., 2 input lines and one output line. One of the input lines selects the TC520 for reading and the other supplies the data clock. The one output line brings the data back to the micro. The data may be read at any speed you choose in order to optimize your opto-coupled transfer rate. The TC500/TC520 pair will continue to convert while the data is being read but the data in the output shift register will not be updated. The data clock is completely independent of the TC520's SYSCLK.

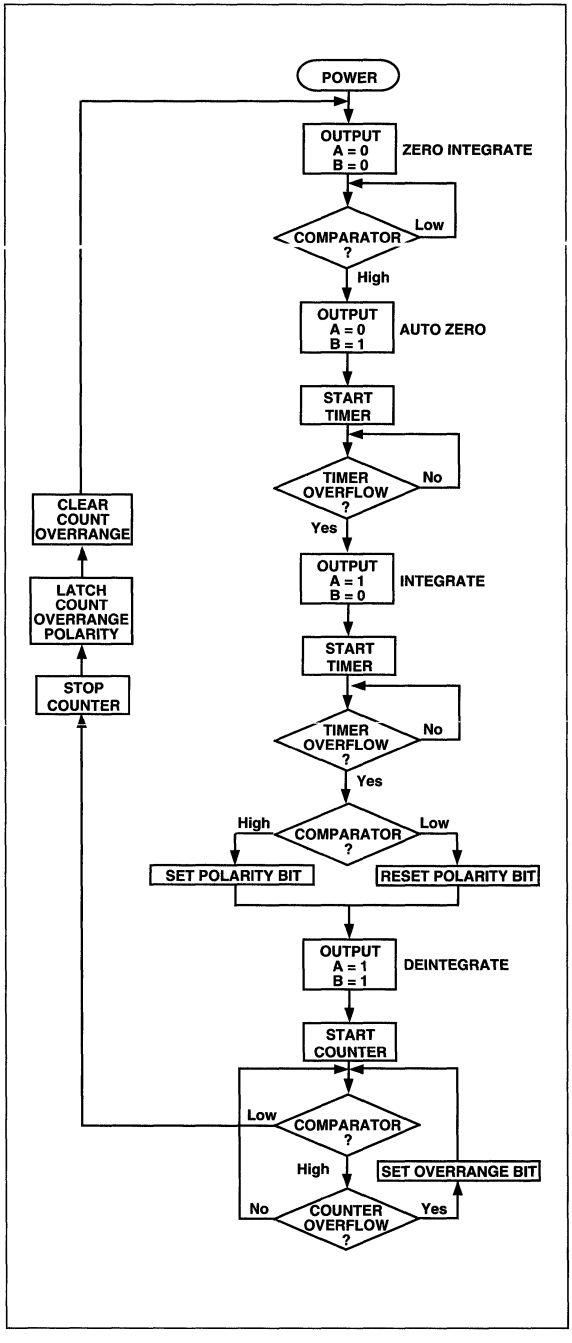
You will be unable to change the integrate timer or force an auto-zero state with only three wires. If you set up the application properly in the first place, it won't be needed. A small capacitor between the $\overline{CE}$ pin and V_{DD} will help in a clean startup.

The only time when you would need the data valid output ($\overline{DV}$) is when the conversion data has to be read as soon as the conversion has been completed. This would require another opto-coupler.

Default Timer Values

The two default values for the 8-bit high byte of the integrate/auto-zero timer are 80_H and 00_H. The most significant bit (MSB) of this byte is equal to the input on the data input pin (D_{IN}) when a negative pulse is applied to the $\overline{LOAD}$ input. i.e., if D_{IN} is low then a default count of 2^{16} is used, otherwise the default count would be 2^{15}.

TC520 LOGIC FLOW CHART



3-3/4 DIGIT A/D CONVERTER WITH AUTO-RANGING FREQUENCY COUNTER

FEATURES

- 3-3/4 Digit, Multiple-Function Measurement System
  - Analog-to-Digital Converter
  - Frequency Counter
  - Interface to LED, VF or LCD Display or microprocessor μP
- Frequency Counter
  - Measures Input Frequency to 4 MHz
  - Auto-Ranging Over Four-Decade Range
- Low Noise A/D Converter
  - Differential Inputs, 1 pA Bias Current
  - Differential Reference for Ratiometric Ohms
  - On-Chip Voltage Reference, 50ppM/°C Drift
- Peak Reading Hold Displays Highest Reading
- 3-3/4 Digit (3999 Maximum) Resolution
- Multiplexed BCD Data Outputs
  - Full 3-3/4 Digit Display
  - Three Decimal Point and Polarity Drivers
- On-Chip Buzzer Driver and Control Input
- Control Input Changes Full Scale Range by 10:1
- Data Hold Input
- Underrange and Overrange Outputs
- Single 5V Operation
  - On-Chip –5V Generator
- Multiple Package Options
  - 40-Pin DIP Package
  - 44-Pin Flat Package or PLCC

GENERAL DESCRIPTION

The TC831 is a 3-3/4 digit measurement system combining an integrating analog-to-digital converter and a frequency counter in a single 40-pin package. A multiplexed Binary-Coded-Decimal (BCD) output provides an easy interface to an LED or LCD display, or to a microprocessor.

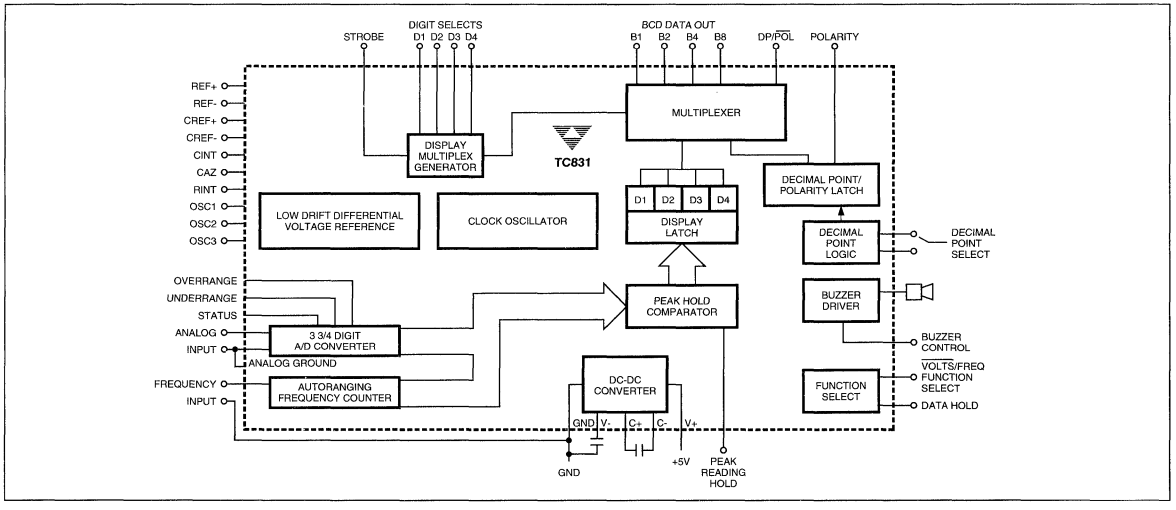
The TC831 supersedes the TC14433 in new designs by improving performance and adding features. Products which presently use the 7107 can also be upgraded with improved resolution, brighter LED display, and BCD data output.

With a maximum range of 3999 counts, the TC831 provides 10 times greater resolution in the 200 mV to 400 mV range than traditional 3-1/2 digit meters. An auto-zero cycle guarantees a zero reading with a 0V input. Rollover error, the difference in readings for equal magnitude but opposite polarity input signals, is less than ±1 count.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC831CKW	44-Pin PQFP	0°C to +70°C
TC831CLW	44-Pin PLCC	0°C to +70°C
TC831CPL	40-Pin PlastiC DIP	0°C to +70°
TC831EKW	44-Pin PQFP	– 40°C to +85°C
TC831ELW	44-Pin PLCC	– 40°C to +85°C
TC831EPL	44-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



3-3/4 DIGIT A/D CONVERTER WITH AUTO-RANGING FREQUENCY COUNTER

TC831

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S^+ to GND) 6V
Analog Input Voltage (Either Input) (Note 1) .... V_S^+ to V_S^-
Reference Input Voltage (Either Input) ..... V_S^+ to V_S^-
Digital Inputs ..... V_S^+ to DGND
Power Dissipation, Plastic Package (Note 2) ..... 800 mW
Operating Temperature Range
"C" Devices ..... 0°C to +70°C
"E" Devices ..... – 40°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTES: 1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

*Static-sensitive devices. Unused devices should be stored in conductive material to protect against static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 5V, – 40°C ≤ T_A ≤ +85°C unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Analog Section							
	Zero Input Reading	V_{IN} = 0V Full Scale = 400 mV	T_A = 25°C – 40°C ≤ T_A ≤ +85°C	– 0000	0000 ±0000	+0000	Digital Reading
RE	Roll-Over Error	V_{IN} = ±390 mV Full-Scale = 400 mV	T_A = 25°C – 40°C ≤ T_A ≤ +60°C	– 1 – 3	±0.2	+1 +3	Counts
NL	Nonlinearity (Maximum Deviation From Best Straight Line Fit)	Full-Scale = 400 mV	T_A = 25°C	– 1	±0.2	+1	Count
	Ratiometric Reading	V_{IN} = V_{REF}	T_A = 25°C – 40°C ≤ T_A ≤ +85°C	1999	1999/2000 1999/2001	2000	Digital Reading
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 400 mV	T_A = 25°C	—	50	—	µV/V
VCMR	Common-Mode Voltage Range	Input High, Input Low		V_S^- + 1.5		V_S^+–1	V
E_N	Noise (P-P Value Not Exceeded 95% of Time)	V_{IN} = 0V Full-Scale = 400 mV		—	15	—	µV
I_{IN}	Input Leakage Current	V_{IN} = 0V	T_A = 25°C 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	— — —	— 50 100	10 — —	pA
V_{COM}	Analog Common Voltage	25 kΩ Between Common and V_S^+ (V_S^+ – V_{COM})		3.0	3.2	3.4	V
V_{CTC}	Common Voltage Temperature Coefficient	25 kΩ Between Common and V_S^+	 0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	 — —	 35 —	 50 75	 ppm/°C
TC_{ZS}	Zero Reading Drift	V_{IN} = 0V	0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	— —	0.2 1	— 2	µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 399 mV Ext Ref = 0 ppm/°C	0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C	— —	1 5	5 25	ppm/°C
Digital Section							
V_{IL}	Input Low Voltage			—	—	0.8	V
V_{IH}	Input High Voltage			3.5	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		—	0.2	0.4	V
V_{OH}	Output High Voltage	I_{OH} = 1.0 mA		4.0	4.5	—	V
	Control Pin Pull-Down Current	V_{IN} = V_S^+		—	5	20	µA

ELECTRICAL CHARACTERISTICS (Cont.) $-40°C \le T_A \le +85°C$ unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Digital Section (Cont.)							
V_{OH}	Output High Voltage	I_{OH} = 1.0 mA		4.0	4.5	—	V
	Control Pin Pull-Down Current	$V_{IN} = V_S^+$		—	5	20	µA
	Control Pin Pull-Up Current	V_{IN} = GND		—	25	50	µA
	Buzzer Frequency	f_{OSC} = 40 kHz		—	5.0	5.0	kHz
	Counter Timebase Period	f_{OSC} = 40 kHz		—	1	1	Second
Power Supply Section							
I_S	Supply Current	V_{S+} = 5V V_{IN} = 0.0V	T_A = 25°C $-40°C \le T_A \le +85°C$	—	2	3 4	mA
	DC-to-DC Converter Output Voltage	V_{S+} = 5V C_{DC-DC} = 1µF		– 4.8	– 4.95	—	V

PIN DESCRIPTION

Pin No. (40-Pin Package)	Pin No. (44-Pin PLCC Package)	Symbol	Description
1	1	OR	**Overrange Output.** This output will be HIGH when the analog signal input is greater than full scale.
2	2	POL	**Polarity Output.** This output is HIGH when the analog input polarity is positive. POL is always HIGH in the frequency counter mode.
3	3	B8	BDC Data Output Bit 8 (most significant bit).
4	4	B4	BCD Data Output Bit 4.
5	5	B2	BCD Data Output Bit 2.
6	6	B1	BCD Data Output Bit 1 (least significant bit).
	7	GT	**Greater Than Output.** This output indicates that the new reading is greater than the reading being displayed. If this condition exists, then GT will go HIGH when the integrator zero crossing occurs, and stay HIGH until 50 clock pulses after EOC. See text.
7	8	D1	Digit Drive Output 1 (least significant digit).
8	9	D2	Digit Drive Output 2.
9	10	D3	Digit Drive Output 3.
10	11	D4	Digit Drive Output 4 (most significant digit).
11	12	$\overline{POL}$/DP	**Polarity and Decimal Point Data Output.** $\overline{Polarity}$, DP3, DP2, DP1 are output on this pin when D4, D3, D2, and D1 are active. See text.
12	13	V_S-	Negative supply voltage, output of on-chip DC-DC converter. Decouple to GND with a1µF capacitor.
13	14	C-	Capacitor connection for on-chip DC-DC converter.
14	15	DGND	**Digital and Power Ground.** The logic "0" level. Connect to ground of +5V supply.
15	16	C+	Capacitor connection for on-chip DC-DC converter.
16	17	V_S+	**Positive Supply Connection.** Connect to +5V.
	18		**NC.** No internal connection.
17	19	UR	**Underrange Output**. This output will be HIGH when the digital reading is equal to
or			less than 380 counts.

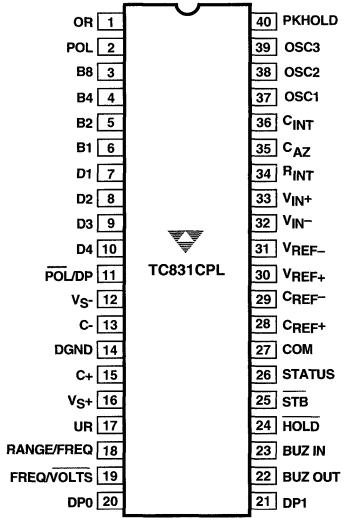
PIN DESCRIPTION (Cont.)

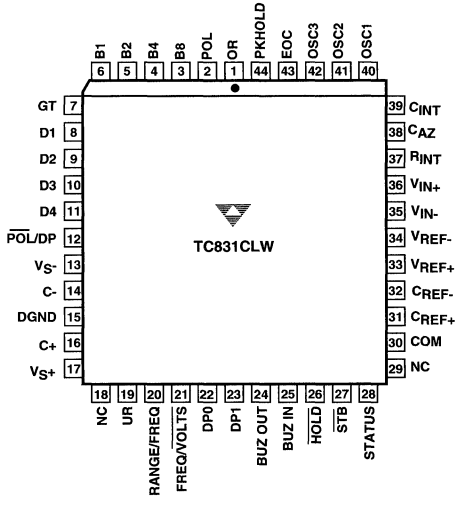
Pin No. (40-Pin Package)	Pin No. (44-Pin PLCC Package)	Symbol	Description
18	20	Range/FREQ	**Dual-Purpose Input.** In voltage mode: When connected to V_S+, the integration time will be 200 counts instead fo 2000 counts, and the TC831 will display the analog input voltage divided by 10. In frequency mode, this pin is the frequency input. A digital signal applied to this pin will be measured with a one second timebase. There is an internal 5µA pulldown to DGND.
19	21	FREQ/$\overline{\text{VOLTS}}$	**Voltage or Frequency Measurement Select Input.** When unconnected or connected to DGND, the A/D converter function is active. When connected to V_S^+, the frequency counter function is active. This pin has an internal 5µA pulldown to DGND.
20	22	DPO	**Decimal Point Select Input for Voltage Measurements.** There is an internal 5µA pulldown to DGND. Decimal point logic: DP1 DP0 Decimal Point Selected 0 0 None 0 1 DP1 1 0 DP2 1 1 DP3
21	23	DP1	**Decimal Point Select Input for Voltage Measurements.** There is an internal 5 µA pull-down to DGND.
22	24	BUZOUT	**Buzzer Output.** Audio frequency, 5 kHz, output which drives a piezoelectric buzzer. Controlled by the BUZIN input.
23	25	BUZIN	**Buzzer Control Input.** Connecting BUZIN to V_S^+ turns the buzzer on. There is an internal 5 µA pull-down to DGND.
24	26	$\overline{\text{HOLD}}$	**Data Hold Input.** Connecting HOLD to DGND will "freeze" the display. In A/D mode, the TC831 will remain in the A/Z phase. In frequency counter mode the TC831 will remain in idle mode. This pin has an internal pullup to V_S^+.
25	27	$\overline{\text{STB}}$	**Digit Strobe Output.** This output goes LOW for 1/2 clock period, in the middle of each digit select pulse, once during each conversion cycle. See text.
26	28	Status	This output is HIGH during the deintegrate portion of an A/D conversion. It is HIGH when the frequency counter is operating.
	29		No connection.
27	30	COM	**Analog Circuit Ground Reference Point.** Nominally 3.3V below V_S^+.
28	31	C_{REF}^+	Positive connection for reference capacitor.
29	32	C_{REF}^-	Negative connection for reference capacitor.
30	33	V_{REF}^+	High differential reference input connection.
31	34	V_{REF}^-	Low differential reference input connection.
32	35	V_{IN}^-	Low analog input signal connection.
33	36	V_{IN}^+	High analog input signal connection.
34	37	R_{INT}	**Buffer Output.** Connect to integration resistor.
35	38	C_{AZ}	Auto-zero capacitor connection.
36	39	C_{INT}	**Integrator Output.** Connect to integration capacitor.
37	40	OSC1	Crystal oscillator (input) connection.
38	41	OSC2	Crystal oscillator (output) connection.
39	42	OSC3	RC oscillator connection.
	43	EOC	**End of Conversion.** This output will go HIGH for one system clock cycle, at the end of each conversion. New data is valid on the falling edge of EOC.

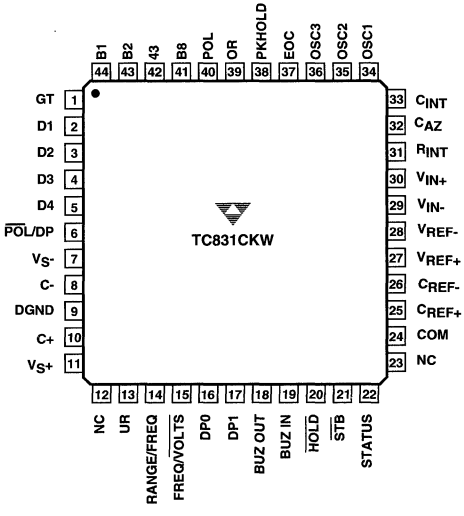
PIN DESCRIPTION (Cont.)

Pin No. (40-Pin Package)	Pin No. (44-Pin PLCC Package)	Symbol	Description
40	44	PKHOLD	**Peak Hold Input.** When connected to V_S^+, the converter will only update the display if a new conversion value is greater than the preceding value. Thus, the peak reading will be stored and held indefinitely. When unconnected or connected to DGND, the converter will operate normally. This pin has an internal 5µA pulldown to DGND.

PIN CONFIGURATIONS







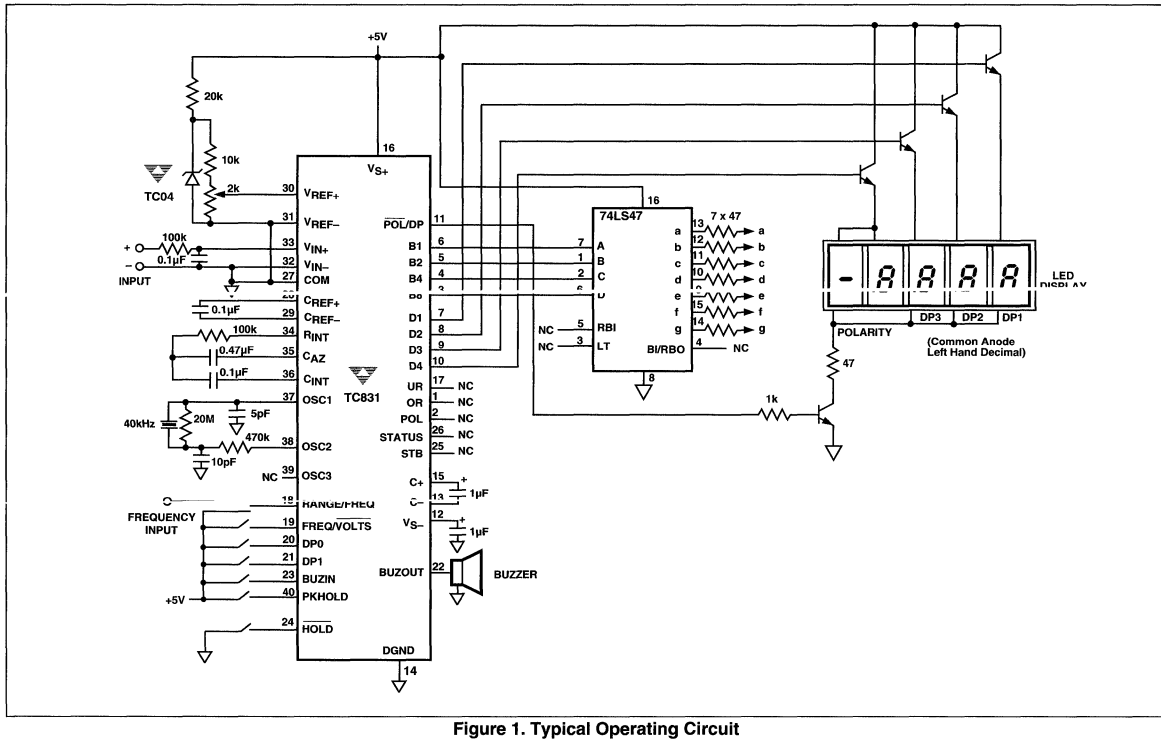


Figure 1. Typical Operating Circuit

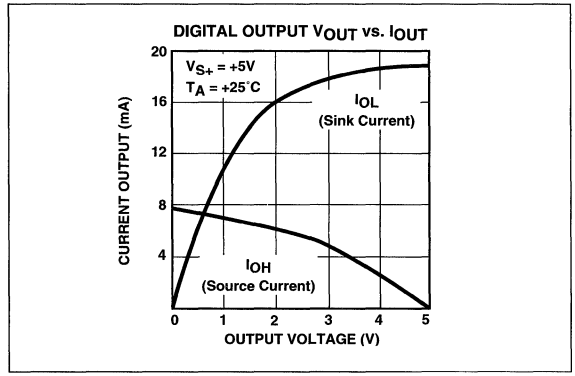
The TC831's frequency counter option simplifies design of flexible, multiple function instruments which combine voltage, current, resistance and precise frequency measurements. The frequency counter will automatically adjust its range to match the input frequency, over a four decade range. The TC831 will measure frequency to 4 MHz directly, and higher frequencies can be measured by adding an external prescaler.

The TC831 A/D converter and frequency counter data is produced in multiplexed BCD data format. This feature permits easy interface to LCD, LED, and VF displays. "Interdigit blanking" on the digit select outputs eliminates "ghosting" in LCD displays. Data Strobe and Status outputs simplify interfacing to microprocessors.

The TC831 operates from a single +5V power supply. A DC-DC converter on the chip, combined with two external capacitors, provides a negative supply.

A "peak reading hold" input allows the TC831 to retain the highest A/D or frequency reading. This feature is useful in measuring motor starting current, maximum temperature, and similar applications. A greater than output signals that the present conversion result has exceeded the previous result. This feature is useful for detecting the negative voltage characteristic of a fully-charged NiCad battery.

Other TC831 features simplify instrument design and reduce parts count. Two digital inputs select the decimal point, while overrange and underrange outputs simplify the design of autoranging instruments. An on-chip piezoelectric buzzer driver can signal overrange or underrange conditions. Two oscillator options are provided: A crystal can be used if highly accurate frequency measurements are required, or a simple RC option can be used for low-end instruments.



The TC831 combines the features of an analog to digital converter and a frequency counter in a single CMOS integrated circuit. With multiplexed BCD Data and Control outputs for easy interface to a μP, the TC831 simplifies the design of multi-mode measurement instruments.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC831 analog-to-digital converter operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC831 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input Signal Integration
(2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

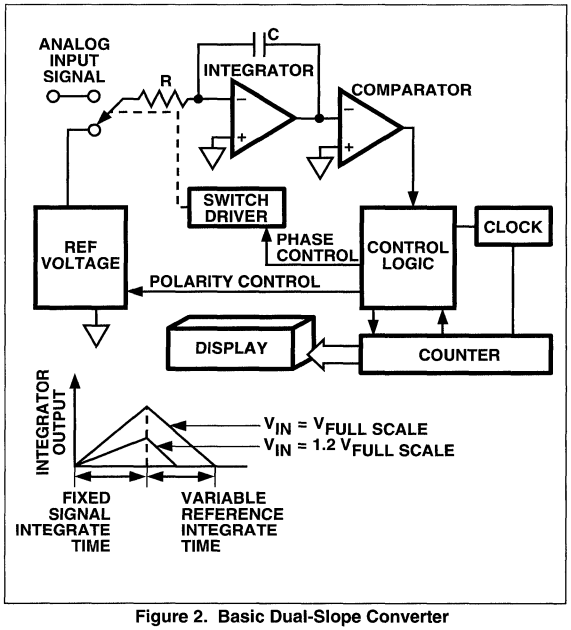


Figure 2. Basic Dual-Slope Converter

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where: V_{REF} = Reference voltage
t_{INT} = Integration time
t_{DEINT} = Deintegration time

For a constant t_{INT}:

$$V_{IN} = V_{REF} \times \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

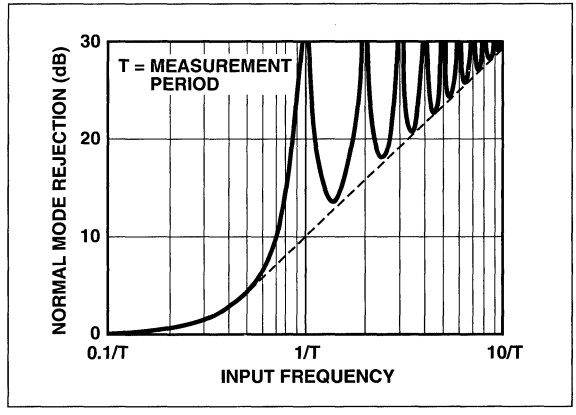


Figure 3. Normal-Mode Rejection of Dual-Slope Converter

TC831 THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC831 design incorporates a "zero integrator output" phase and an "auto-zero" phase. These additional phases ensure that the integrator starts at 0V (even after a severe overrange conversion), and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Zero Integrator Output
(2) Auto-Zero
(3) Signal Integrate
(4) Reference Deintegrate

Zero Integrator Output Phase

This phase guarantees that the integrator output is at 0V before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an overrange conversion. The duration of this phase is 500 counts plus the unused deintegrate counts.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches, and the internal nodes are shorted to Analog Common (0V ref) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The auto-zero phase residual is typically 10 μV to 15 μV. The auto-zero duration is 1500 counts.

Signal Integration Phase

Upon completion of the auto-zero phase, the auto-zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period of 2000 counts (4000 clock periods). The externally-set clock frequency is divided by two before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection that is limited only by device noise and auto-zero residual offsets.

Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the auto-zero phase, is connected to the input of the integrating amplifier. The internal sign logic ensures the polarity of the reference voltage is always connected in the phase opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate determined by the reference potential.

The amount of time required (t_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase:

$$t_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC831 is:

$$\text{Digital Count} = 2000 \times \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

ADC System Timing

The oscillator frequency is divided by 2 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 8000 counts or 16000 clock pulses. The 8000 count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

Conversion Phase	TC831	Units
1) Auto-Zero:	1500	Counts
2) Signal Integrate:[1,2]	2000	Counts
3) Reference Integrate:	1 to 4001	
4) Integrator Output Zero:	499 to 4499	Counts

NOTES: 1. This time period is fixed. The integration period for the TC831 is:

$$t_{INT} = \frac{4000}{f_{OSC}} = 2000 \text{ counts}$$

where f_{OSC} is the clock oscillator frequency.

2. Times shown are with RANGE/FREQ at logic LOW (normal operation). When RANGE/FREQ is logic HIGH, signal integrate times are 200 counts. See "10:1 Range Change" section.

Peak Reading Hold

The TC831 provides the capability of holding the highest (or peak) reading. Connecting the PK HOLD input to V_S^+ enables the peak hold feature. At the end of each conversion the content of the TC831 counter is compared to the content of the display register. If the new reading is higher than the reading being displayed, the higher reading is transferred to the display register. A "higher" reading is defined as the reading with the higher absolute value.

The peak reading is held in the display register so the reading will not "droop" or slowly decay with time. The held reading will be retained until a higher reading occurs, the PK HOLD input is disconnected from V_S^+, or power is removed.

The peak signal to be measured must be present during the TC831 signal integrate period. The TC831 does not perform transient peak detection of the analog input signal. However, in many cases, such as measuring temperature or electric motor starting current, the TC831 "acquisition time" will not be a limitation. If true peak detection is required, a simple circuit will suffice. See the applications section for details.

The peak reading function is also available when the TC831 is in the frequency counter mode. The counter auto-ranging feature is disabled when peak reading hold is selected.

10:1 Range Change

The analog input full-scale range can be changed with the RANGE/FREQ input. Normally, RANGE/FREQ is held low by an internal pulldown. Connecting this pin to V_S^+ will increase the full-scale voltage by a factor of 10. No external component changes are required.

The RANGE/FREQ input operates by changing the integrate period. When RANGE/FREQ is connected to V_S^+, the signal integration phase of the conversion is reduced by a factor of 10.

TC831 FREQUENCY COUNTER THEORY OF OPERATION

In addition to serving as an analog-to-digital converter, the TC831 internal counter can also function as a frequency counter (Figure 4). In the counter mode, pulses at the RANGE/FREQ input will be counted and displayed.

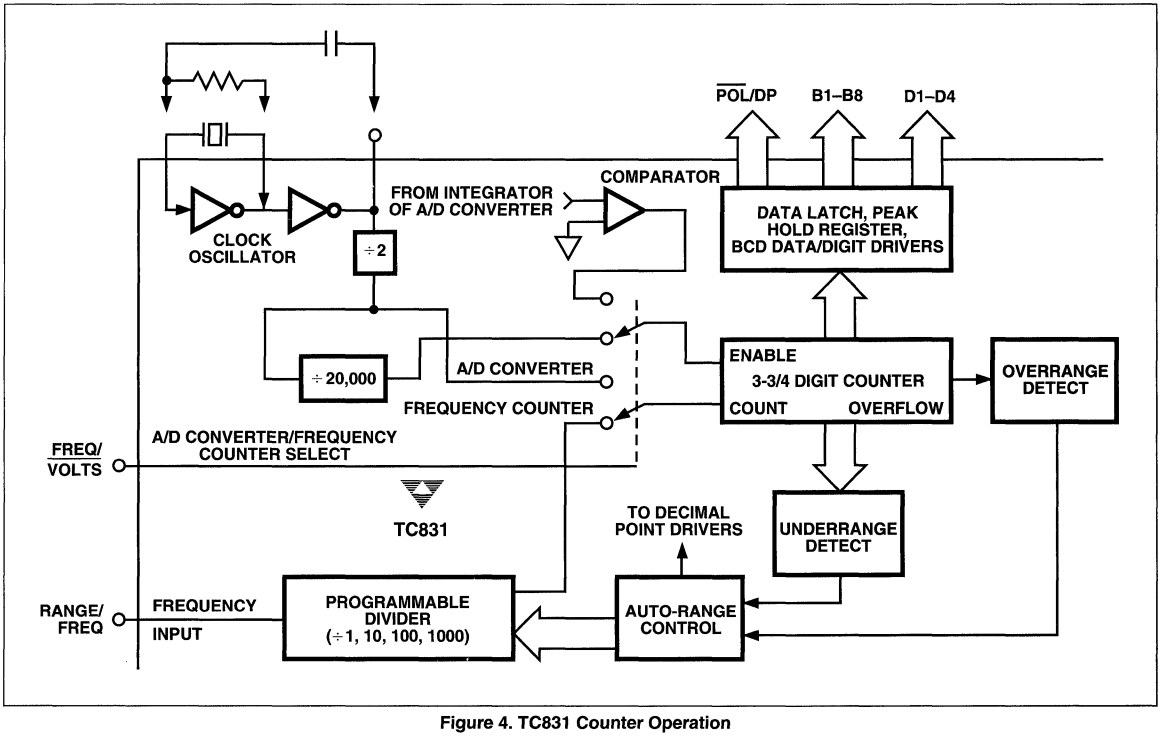


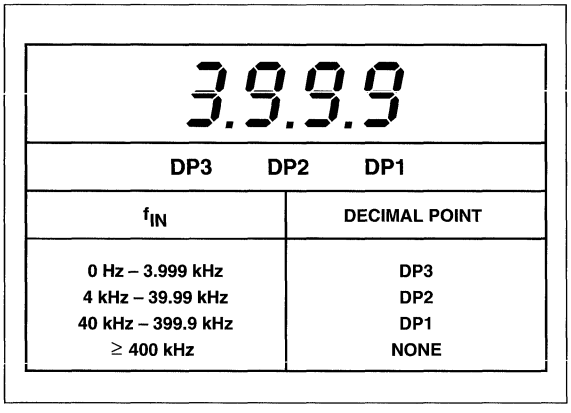
Figure 4. TC831 Counter Operation

The TC831 frequency counter derives its time base from the clock oscillator. The counter time base is:

$$t_{COUNT} = \frac{f_{OSC}}{40{,}000}$$

Thus, the counter will operate with a 1-second time base when a 40 kHz oscillator is used. The frequency counter accuracy is determined by the oscillator accuracy. For accurate frequency measurements, a crystal oscillator is recommended.

The frequency counter will automatically select the proper range. Auto-range operation extends over four decades, from 3.999 kHz to 3.999 MHz. Decimal points are set automatically in the frequency mode (Figure 5).



f_{IN}	DECIMAL POINT
0 Hz – 3.999 kHz	DP3
4 kHz – 39.99 kHz	DP2
40 kHz – 399.9 kHz	DP1
≥ 400 kHz	NONE

Figure 5. TC831 Auto-Range Decimal Point Selection vs Frequency Counter Input

The logic switching levels of the RANGE/FREQ input are CMOS levels. For best counter operation, an external buffer is recommended. See the applications section for details.

ANALOG PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+), (V_{IN}^-)

The TC831 is designed with true differential inputs, and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V_S^+ -1V$ to $V_S^- +1.5V$. Within this common-mode range, an 86dB common-mode rejection is typical.

The integrator output also follows the common-mode voltage and must not be allowed to saturate. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 6). For such applications the integrator output swing can be reduced below the recommended 3.0V full-scale swing. The integrator output will swing within 0.5V of V_S^+ or V_S^- without increased linearity error.

Reference (V_{REF}^+, V_{REF}^-)

The TC831 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors, such as load cells and temperature sensors.

To prevent rollover type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1µF capacitor is a typical value.

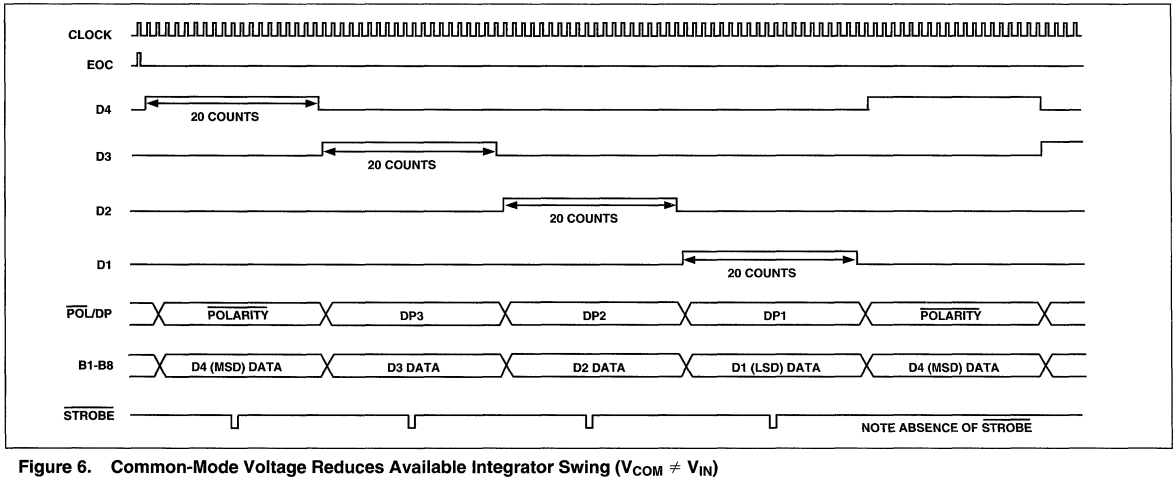


Figure 6. Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

Analog Common

The analog common pin is used as the V_{IN-} return during the autozero and deintegrate phases. In systems where V_{IN-} is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio.

In some applications the analog common pin can be used to set the analog section reference or common point, and at the same time provide an internal voltage reference. This option is useful when making measurements which are not referenced to power ground. Connecting a 27kΩ resistor from the Analog Common pin to V_S^+ will set COM at a voltage potential approximately 3.3V below V_S^+. This potential is guaranteed to be between 3.15V and 3.45V below V_S^+. The temperature coefficient of analog common is typically 35ppm/°C.

Analog common is tied internally to an N channel FET capable of sinking 3mA. This FET will hold the common line at 3.3V below V_S^+ should an external load attempt to pull the common line toward V_S^+. Analog common source current is limited to 12μA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V_S^+ -3.3V), so that COM can be connected to GND when measurements are referenced to power supply ground.

DIGITAL SECTION FUNCTIONAL DESCRIPTION

TC831 Digital Section Functional Description

The TC831 digital section consists of inputs for A/D converter and frequency counter control, and BCD data outputs. The major digital subsystems are illustrated in Figure 7, with timing relationships shown in Figure 8.

The TC831 digital section is best described through a discussion of the data outputs and control signals.

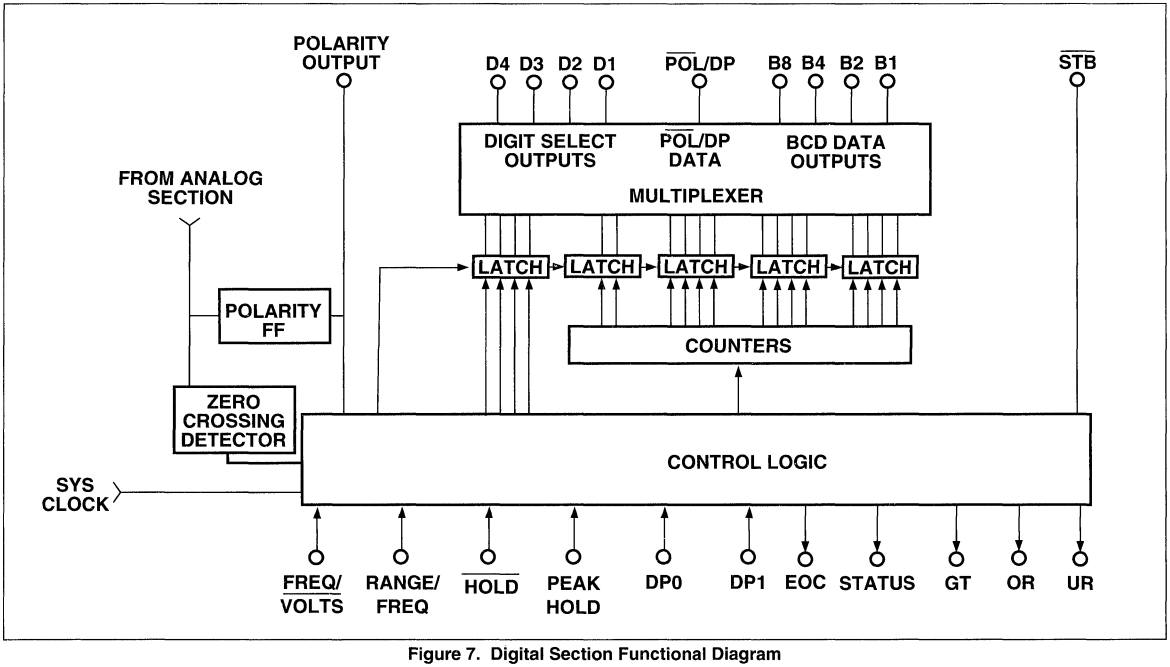


Figure 7. Digital Section Functional Diagram

DATA OUTPUT AND CONTROL PIN FUNCTIONAL DESCRIPTION

BCD Data Outputs (B1-B8)

The TC831 binary coded decimal data bits B8, B4, B2, and B1 are positive true logic. The conversion result is produced in BCD format when the D1 through D4 digit outputs are high. The data format is shown in Table 1.

Table I. TC831 BCD Data Format

	BCD Data Outputs[2]				
Digit Select	**B8**	**B4**	**B2**	**B1**	**$\overline{\text{POL}}$/DP**
D1 (LSD)	BCD Bit8	BCD Bit4	BCD Bit2	BCD Bit1	DP1
D2	BCD Bit8	BCD Bit4	BCD Bit2	BCD Bit1	DP2
D3	BCD Bit8	BCD Bit4	BCD Bit2	BCD Bit1	DP3
D4 (MSD)	0	0	BCD Bit2	BCD Bit1	$\overline{\text{POL}}$

NOTES: [1]The $\overline{\text{POL}}$/DP output will be LOW for a positive polarity input, and HIGH for a negative polarity input.
[2]During an input overrange, B1-B8 are all ones (Hexidecimal "F"), when digit selects D1-D3 are active, so the overrange data is "3FFF$_{16}$". Common display drivers, such as the TC7211A LCD driver, TC7212A LED driver, and 7447 BCD to 7-segment driver, decode "F$_{16}$" as a blank, so the TC831 display will read "3".

The B1-B8 outputs change state 500 nsec before the digit select outputs go HIGH, and remain active until 500 nsec after the digit select outputs go LOW. This interdigit blanking eliminates "ghosting" in LCD displays and simplifies µP interfacing.

The latest conversion result will begin to appear on the BCD data outputs simultaneously with the falling edge of the EOC output.

$\overline{\text{POL}}$/DP

Polarity and decimal point information is produced on this pin simultaneously with the BCD data. The data format is shown in Table 1. Signal timing for the $\overline{\text{POL}}$/DP output is the same as the B1-B8 outputs.

Digit Select Outputs (D1-D4)

Digit Select outputs are positive true. The scan sequence is D4 to D1, and each digit select pulse is 20 clock cycles wide. As mentioned in the BCD Output section of this data sheet, there is an interdigit blanking period of 1µsec between each digit select output becoming active. The digit select outputs will scan continuously as long as the TC831 is not overranged. When an overrange condition occurs, however, the digit select outputs are not active during the reference integrate phase of the next conversion
(i.e. digit selects are low when both the overrange and the status outputs are high.) This feature will make the LED display blink during overrange.

Strobe Output

After each measurement cycle, the $\overline{\text{STB}}$ output is pulsed low four times. The four pulses occur in the center of the digit drive signals (D4-D1), as shown in Figure 9.

D4 goes high for 20 counts when the measurement cycle ends. In the middle of the D4 pulse, the first $\overline{\text{STB}}$ pulse occurs for one half clock cycle. After the D4 digit drive goes LOW, D3 goes HIGH for 20 counts. $\overline{\text{STB}}$ again goes LOW in the middle of D3. This continues through the D1 digit drive pulse.

The digit drive signals will continue, if the output is not overranged so that display scanning is not interrupted. However, the $\overline{\text{STB}}$ pulses will not occur until the next conversion cycle is completed.

The $\overline{\text{STB}}$ pulses simplify the transfer of BCD data to UARTs, microprocessors, and external data latches.

Polarity (POL)

The POL output will be HIGH when the input polarity is positive. The polarity bit is valid at the falling edge of EOC and remains valid until determined during the next conversion.

The polarity bit is valid even for a zero reading. This feature is useful in nulling applications. Polarity is also valid when an overrange condition exists.

Overrange (OR), Underrange (UR)

The OR output will be HIGH when the analog input signal is greater than full scale (3999 counts). The UR output will be high when the display reading is equal to or less than 380 counts. The OR and UR outputs can be used to provide an autoranging meter function.

STATUS

The STATUS output is HIGH during the deintegrate portion of the A/D conversion. Thus, the width of the STATUS output is proportional to the analog input. Logically ANDing STATUS with the system clock will give a pulse train which represents the A/D conversion result.

FUNCTIONAL CONTROL INPUT PIN FUNCTIONAL DESCRIPTION

The TC831 operating modes are selected with the function control inputs. The control input truth table is shown in Table 2. The HIGH logic threshold is ≥V_S+ - 1.5V and the LOW logic level is ≤DGND +1.5V

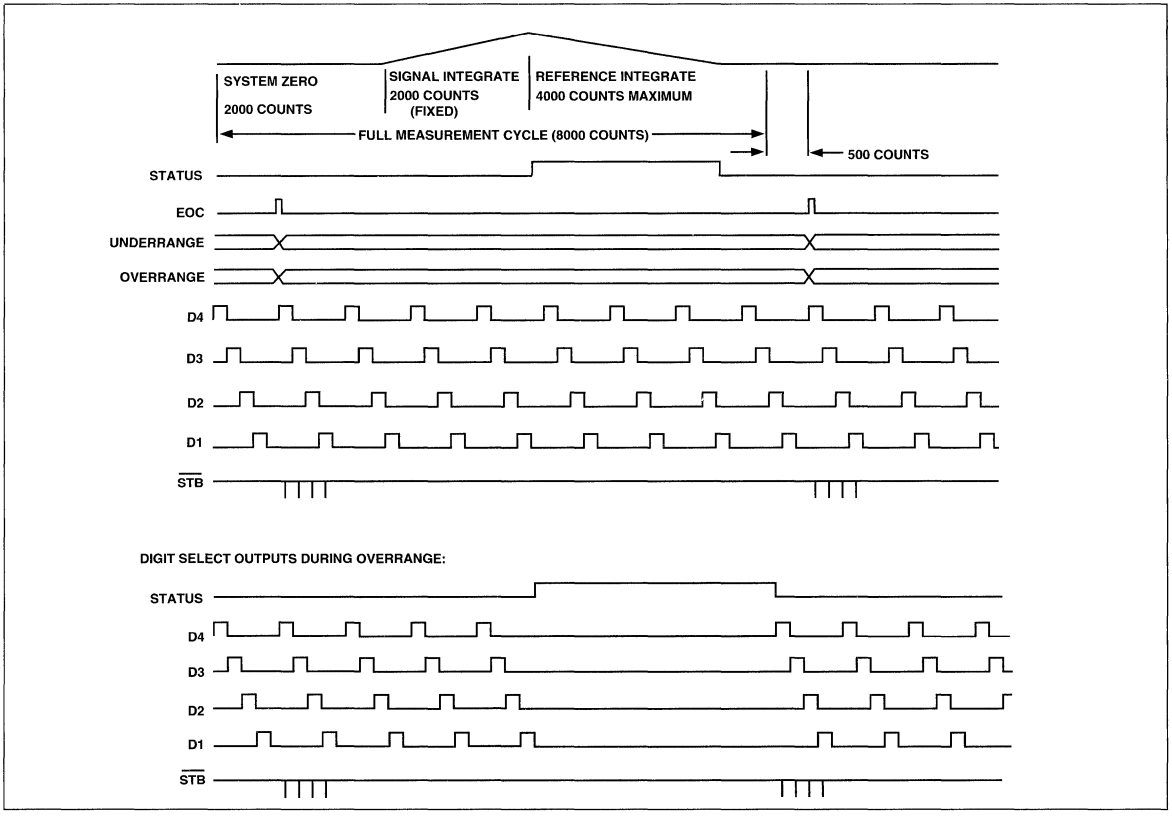


Figure 8. Timing Diagram for Outputs

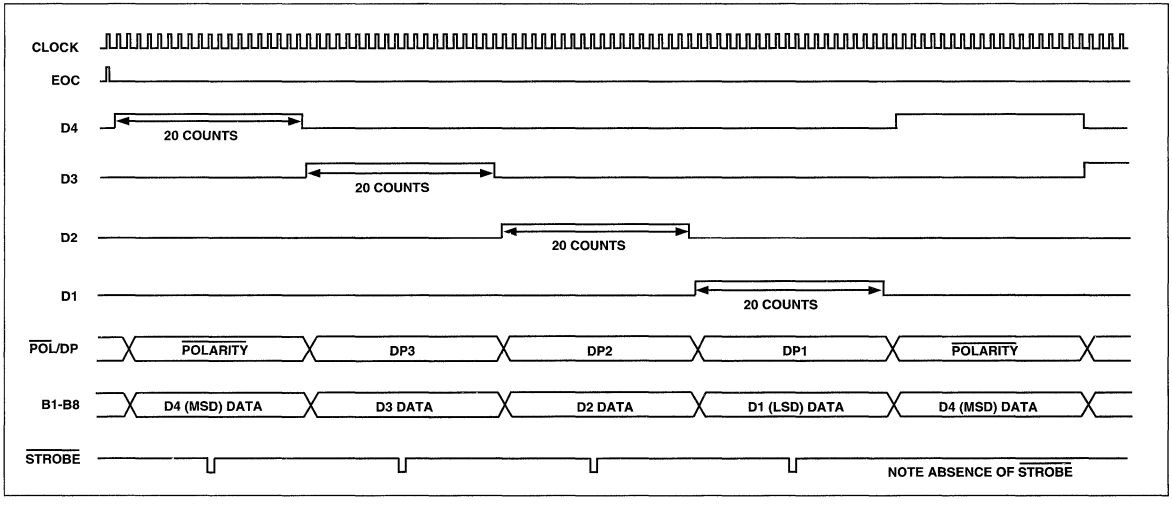


Figure 9. Strobe Signal Pulses LOW Five Times per Conversion

Table II. TC831 Control Input Truth Table

Logic Input		TC831 Function
FREQ/$\overline{\text{VOLTS}}$	RANGE/FREQ	
0	0	A/D Converter V Full Scale = 2 x V_{REF}
0	1	A/D Converter V Full Scale = 20 x V_{REF}
1	Frequency Counter Input	Frequency Counter

NOTES: Logic "0" = DGND
Logic "1" = V_S+

FREQ/$\overline{\text{VOLTS}}$

This input determines whether the TC831 is in the analog-to-digital conversion mode or in the frequency counter mode. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_S+, the TC831 will measure frequency at the RANGE/FREQ input. When unconnected or connected to DGND, the TC831 will operate as an analog-to-digital converter. This input has an internal 5μA pulldown to DGND.

RANGE/FREQ

The function of this dual-purpose pin is determined by the FREQ/$\overline{\text{VOLTS}}$ input. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_S^+, RANGE/FREQ is the input for the frequency counter function. Pulses at this input are counted with a time base equal to f_{OSC}/40,000. Since this input has CMOS input levels (V_S^+ –1.5V and DGND +1.5V), an external buffer is recommended.

When the TC831 analog-to-digital converter function is selected, connecting RANGE/FREQ to V_S^+ will divide the integration time by 10. Therefore, the RANGE/FREQ input can be used to perform a 10:1 range change without changing external components.

DP0, DP1

When the TC831 is in the analog-to-digital converter mode, these inputs control the LCD decimal points. The decimal point truth table is shown in Table III. These inputs have internal 5μA pull-downs to DGND. DP0 and DP1 have no effect when the TC831 is in the frequency counter mode, because the autoranging control circuitry automatically sets the decimal point.

Peak Reading Hold Input

See the "ADC Theory of Operation" section for the description of this input.

Table III. TC831 Decimal Point Truth Table

Decimal Point Inputs		
DP1	DP0	Decimal Point
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

10:1 Range Change Input

See the "ADC Theory of Operation" section for the description of this input.

BUZ IN

This input controls the TC831 on-chip buzzer driver. Connecting BUZ IN to V_S^+ will turn the buzzer on. There is an external pull-down to DGND. BUZ IN can be driven by the overrange and/or underrange outputs to indicate an out-of-range reading.

$\overline{\text{HOLD}}$

The $\overline{\text{HOLD}}$ can be used to hold or "freeze" the display. Connecting this pin to DGND stops the converter (after the present conversion is complete). The TC831 will remain at the beginning of auto zero (A/D mode) or in the idle mode (frequency counter mode) as long as $\overline{\text{HOLD}}$ remains LOW. $\overline{\text{HOLD}}$ will hold the display reading for either analog-to-digital or frequency measurements.

Additional Features

The TC831 is available in 40-pin and 44-pin packages. Two additional features are available in the 44-pin package:

EOC

This output signals the end of an A/D conversion or frequency measurement period. EOC will go high for one system clock cycle at the end of each conversion. New BCD data will be valid on the falling edge of EOC.

The EOC output also simplifies the design of autoranging instruments. By logically ANDing the overrange and underrange outputs with the EOC output, a single pulse will be generated each time that an underranged or overranged conversion occurs (Figure 10).

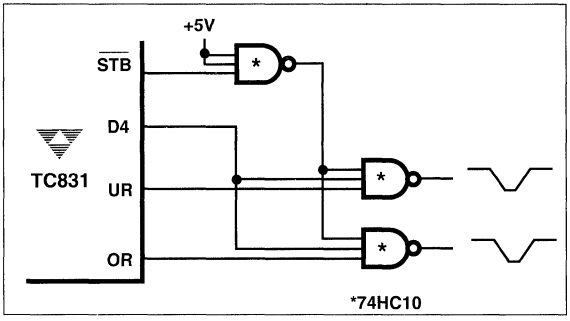


Figure 10. Generating Underrange and Overrange Pulses

Greater Than

The GT output, which is used on the peak reading hold mode, indicates that the new reading is greater than the present reading. GT will go HIGH at the integrator zero crossing and remain HIGH until 50 clock pulses after the falling edge of EOC, if the new conversion result is greater than the contents of the display register.

This output can be used to signal an increasing voltage reading, or to signal that a reading is no longer increasing. For example, the voltage of a NiCad battery will rise during recharging. When the battery is fully charged, however, the voltage will begin to decrease. The GT output can be used to reset a timer which controls the charging current. The GT output pulses will reset the timer and continue to charge the battery as long as the battery voltage increases.
When the battery is fully charged the voltage will decrease, the GT pulses will end, the timer will time out and the charging current will end.

APPLICATIONS INFORMATION

Power Supplies

The TC831 typically operates from a single +5V power supply. The converter will operate over a power supply range of 3.5V to 6V.

An on-chip DC-DC converter, combined with two external capacitors, generates a VS- supply. This permits both positive and negative input polarity signals to be measured without requiring a dual polarity power supply. With VS+ of 5V and capacitors of 1μF, the DC-DC converter output will typically be –4.9V.

Digital Input Logic Levels

Logic levels for the TC831 digital inputs are referenced to V_S^+ and DGND. The HIGH-level threshold is V_S^+ –1.5V and the LOW logic level is DGND +1.5V.

Clock Oscillator

The TC831 oscillator can be controlled with either a crystal or with an inexpensive resistor-capacitor combination. The crystal circuit, shown in Figure 11, is recommended when high accuracy is required in the frequency counter mode. The 40 kHz crystal is a standard frequency for ultrasonic alarms, and will provide a 1-second time base for the counter or 2.5 analog-to-digital conversions per second.

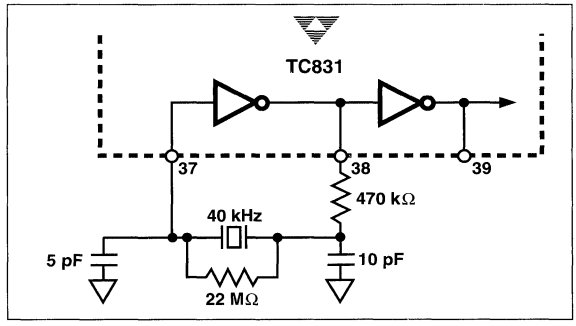


Figure 11. Suggested Crystal Oscillator Circuit

Where low cost is important, the R-C circuit of Figure 12 can be used. The frequency of this circuit will be approximately:

$$f_{OSC} = \frac{0.3}{RC}$$

Typical values are R = 110 kΩ and C = 68 pF. The resistor value should be ⩾100 kΩ. For accurate frequency measurement, an R-C oscillator frequency of 40 kHz is required.

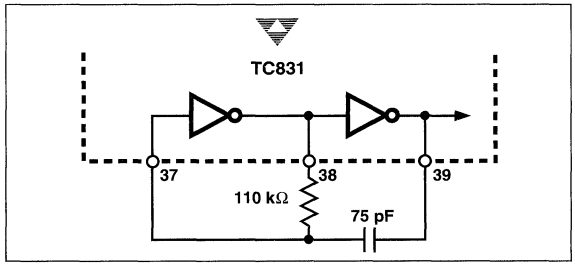


Figure 12. R-C Oscillator Circuit

System Timing

All system timing is derived from the clock oscillator. The clock oscillator is divided by 2 prior to clocking the A/D counters. The clock is also divided by 8 to drive the buzzer, by 160 to generate the BCD multiplex rate, and by 40,000 for the frequency counter time base. A simplified diagram of the system clock is shown in Figure 13.

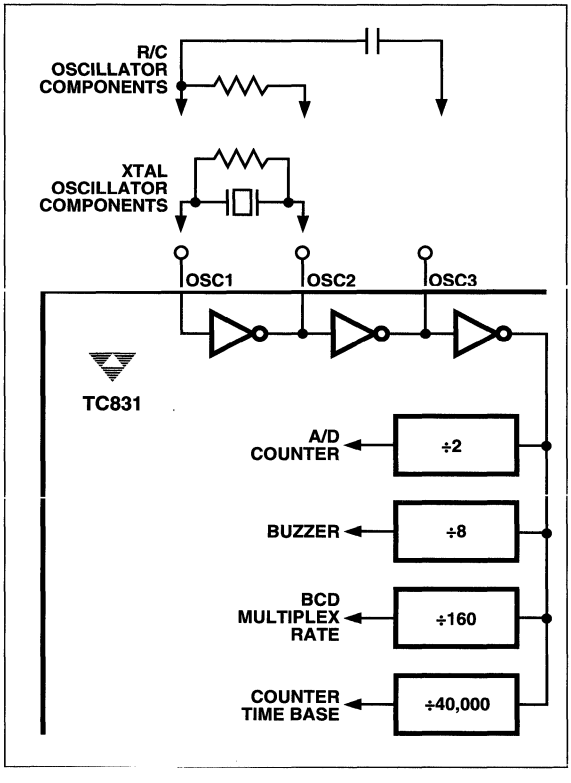


Figure 13. System Clock Generation

COMPONENT VALUE SELECTION

Auto Zero Capacitor — C_{AZ}

The value of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A 0.47 µF capacitor is recommended; a low dielectric absorption capacitor (Mylar) is required.

Reference Voltage Capacitor — C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is typical. A good quality, low leakage capacitor (such as Mylar) should be used.

Integrating Capacitor — C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. With a +5V power supply and Analog Common connected to power supply ground, a ±4V integrator output swing is optimum when the analog input is near full scale. For 2.5 readings/second (f_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.1 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±4V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where: f_{OSC} = Clock frequency
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor — R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 40 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 400 mV full scale, R_{INT} should be about 100 kΩ.

Reference Voltage Selection

A full-scale reading (4000 counts) requires the input signal be twice the reference voltage. For example, a reference voltage of 200mV will produce a 400mV full scale.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 800 mV for 4000 lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 400 mV. This permits the transducer input to be used directly.

If the voltage being measured is not referenced to power ground, the internal voltage reference potential available at analog common can be used to supply the converter's reference voltage.

When measurements are referenced to power ground, an external reference should be used. Figure 14 shows internal and external reference applications.

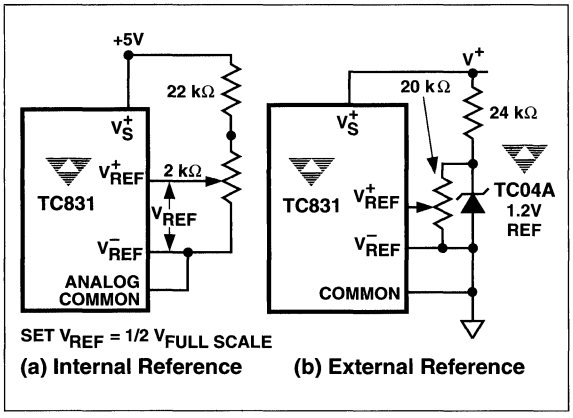


Figure 14. Reference Voltage Connections

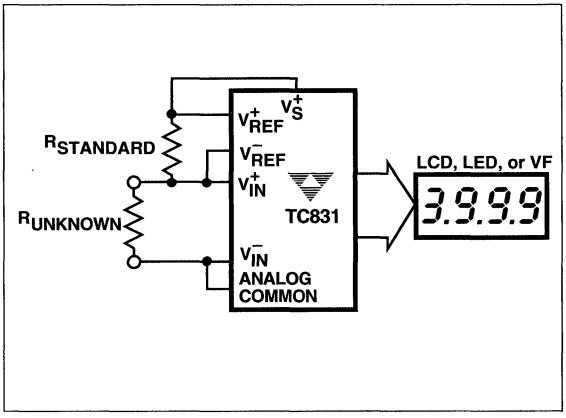


Figure 15. Low Parts Count Ratiometric Resistance Measurement

Ratiometric Resistance Measurements

The TC831 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 15). The voltage developed across the unknown is applied to the input and voltages across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 2000$$

The display will overrange for values of $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

Buffering the FREQ Input

When the FREQ/VOLTS input is HIGH and the LOGIC input is LOW, the TC831 will count pulses at the RANGE/FREQ input. The time base will be f_{OSC}/40,000, or 1 second with a 40 kHz clock. The signal to be measured should swing from V_{S+} to DGND. The RANGE/FREQ input has CMOS input levels without hysteresis. For best results, especially with low frequency sine wave inputs, an external buffer with hysteresis should be added. A typical circuit is shown in Figure 16.

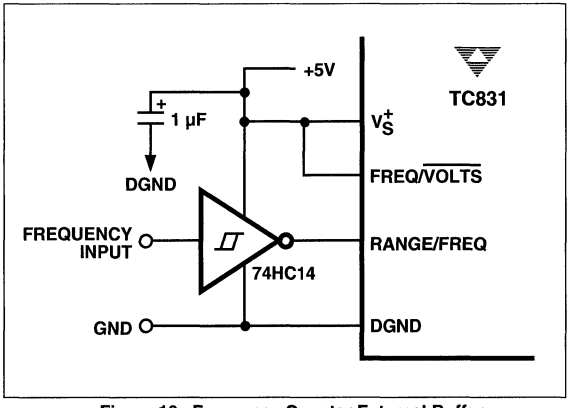


Figure 16. Frequency Counter External Buffer

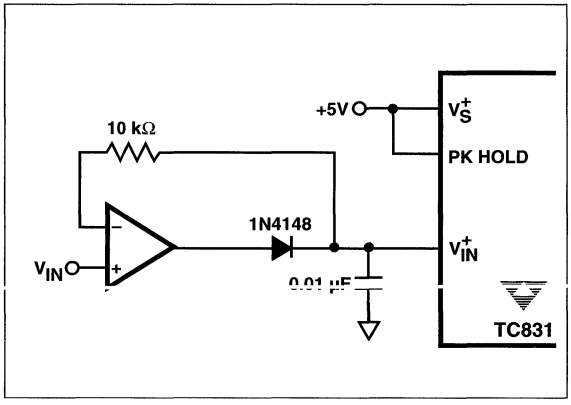


Figure 17. External Peak Detector

External Peak Detection

The TC831 will hold the highest A/D conversion or frequency reading indefinitely when the PK HOLD input is connected to V_S^+. However, the analog peak input must be present during the A/D converter's signal integrate period. For slowly changing signals, such as temperature, the peak reading will be properly converted and held.

If rapidly changing analog signals must be held, an external peak detector should be added. An inexpensive circuit can be made from an Op-Amp and a few discrete components, as shown in Figure17. The droop rate of the external peak detector should be adjusted so that the held voltage will not decay below the desired accuracy level during the converter's 400 ms conversion time.

Crystal Source

Two sources of the 40 kHz crystal are:

Statek Corp
512 N. Main St
Orange, CA 92668
Phone: (714) 639-7810
Fax: (714) 997-1256
Part #: CX-1V-40.0

SPK Electronics
2F-1, No. 312, Sec 4,
Jen Ai Rd
Taipei, Taiwan R.O.C.
Phone: (02) 754-2677
Fax: 886-2-708-4124
Part#: QRT-38-40.0 kHz

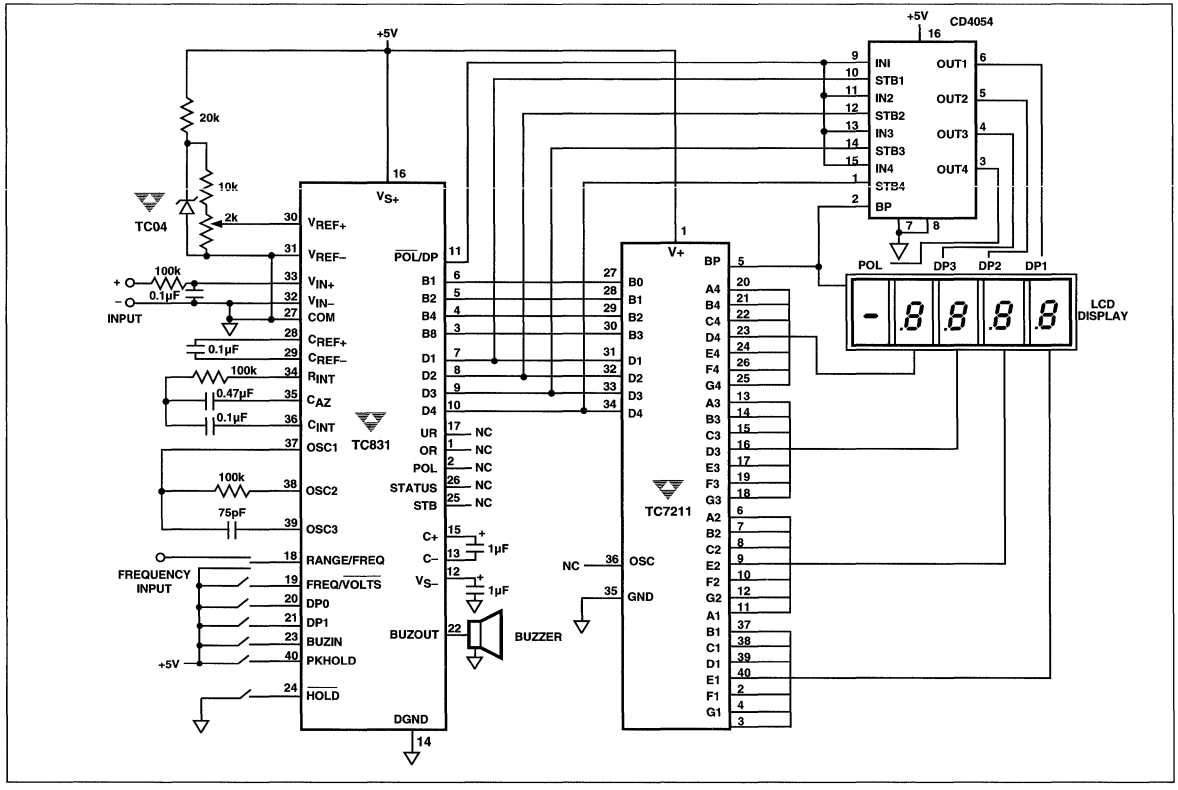


Figure 18. TC831 Interface to LCD Display

PERSONAL COMPUTER DATA ACQUISITION ADC

FEATURES

- **Upgrade of Pin-Compatible TC7135, ICL7135, MAX7135 and SI7135**
- **Guaranteed 200 kHz Operation**
- **Single 5V Operation With TC7660**
- **Multiplexed BCD Data Output**
- **UART and Microprocessor Interface**
- **Control Outputs for Auto-Ranging**
- **Input Sensitivity ..... 100 μV**
- **No Sample and Hold Required**

APPLICATIONS

- **Personal Computer Data Acquisition**
- **Scales, Panel Meters, Process Controls**
- **HP-IL Bus Instrumentation**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC835CPI	28-Pin Plastic DIP	0°C to +70°C
TC835CKW	44-Pin PQFP	0°C to +70°C
TC835CBU	64-Pin PFP	0°C to +70°C

NOTE: Tape and reel available for 44-pin PQFP packages.

GENERAL DESCRIPTION

The TC835 is a low-power, 4-1/2 digit (0.005% resolution), BCD analog-to-digital converter (ADC) that has been characterized for 200 kHz clock rate operation. The five conversions per second rate is nearly twice as fast as the ICL7135 or TC7135. The TC835 (like the TC7135) does not use the external diode-resistor roll-over error compensation circuits required by the ICL7135.

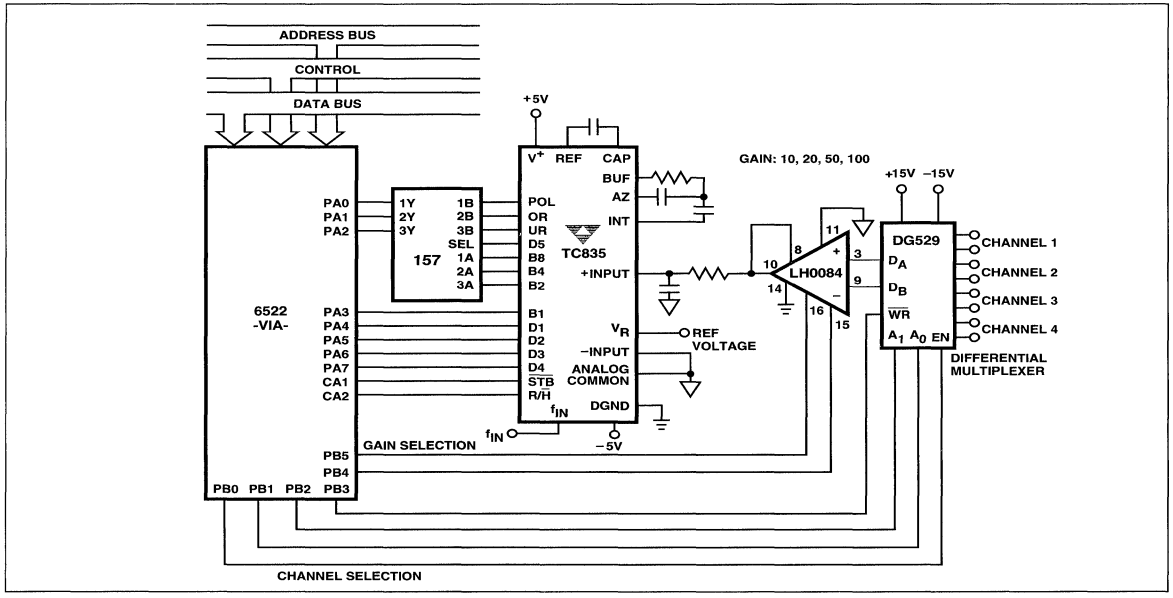
The multiplexed BCD data output is perfect for interfacing to personal computers. The low-cost, greater than 14-bit high-resolution, and 100 μV sensitivity makes the TC835 exceptionally cost-effective.

Microprocessor-based data acquisition systems are supported by the BUSY and STROBE outputs, along with the RUN/HOLD input of the TC835. The overrange, underrange, busy, and run/hold control functions and multiplexed BCD data outputs make the TC835 the ideal converter for μP-based scales and measurement systems and intelligent panel meters.*

The TC835 interfaces with full-function LCD and LED display decoder/drivers (TC7211A or TC7212A). The UNDERRANGE and OVERRANGE outputs may be used to implement an auto-ranging scheme or special display functions.

*See Application Notes 16 and 17 for microprocessor interface techniques.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... –9V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0V to V^+
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Power Dissipation
CerDIP (J) 1W
Plastic (P) 0.8W

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLOCK} = 200 kHz, V^+ = +5V, V^- = –5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Display Reading With Zero Volt Input	Notes 3 and 4	–0.0000	±0.0000	+0.0000	Display Reading
TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0V Note 5	—	0.5	2	µV/°C
TC_{FS}	Full-Scale Temperature Coefficient	V_{IN} = 2V Notes 5 and 6	—	—	5	ppm/°C
NL	Nonlinearity Error	Note 7	—	0.5	1	Count
DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	Display Reading in Ratiometric Operation	V_{IN} = V_{REF} Note 3	+0.9997	+0.9998	+1.0000	Display Reading
±FSE	± Full-Scale Symmetry Error (Roll-Over Error)	$-V_{IN}$ = $+V_{IN}$ Note 8	—	0.5	1	Count
I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
e_N	Noise	Peak-to-Peak Value Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
I_{IL}	Input Low Current	V_{IN} = 0V	—	10	100	µA
I_{IH}	Input High Current	V_{IN} = +5V	—	0.08	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.2	0.4	V
V_{OH}	Output High Voltage B_1, B_2, B_4, B_8, D_1–D_5 Busy, Polarity, Overrange, Underrange, Strobe	 I_{OH} = 1 mA I_{OH} = 10 µA	 2.4 4.9	 4.4 4.99	 5 5	 V V
f_{CLK}	Clock Frequency	Note 10	0	200	1200	kHz
Power Supply						
V^+	Positive Supply Voltage		4	5	6	V
V^-	Negative Supply Voltage		–3	–5	–8	V
I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1	3	mA
I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3	mA
PD	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

NOTES:
1. Functional operation is not implied.
2. Limit input current to under 100 µA if input voltages exceed supply voltage.
3. Full-scale voltage = 2V.
4. V_{IN} = 0V.
5. 0°C ≤ T_A ≤ +70°C.
6. External reference temperature coefficient less than 0.01 ppm/°C.
7. –2V ≤ V_{IN} ≤ +2v. Error of reading from best fit straight line.
8. $|V_{IN}|$ = 1.9959.
9. Test circuit shown in Figure 1.
10. Specification related to clock frequency range over which the TC835 correctly performs its various functions. Increased errors result at higher operating frequencies.

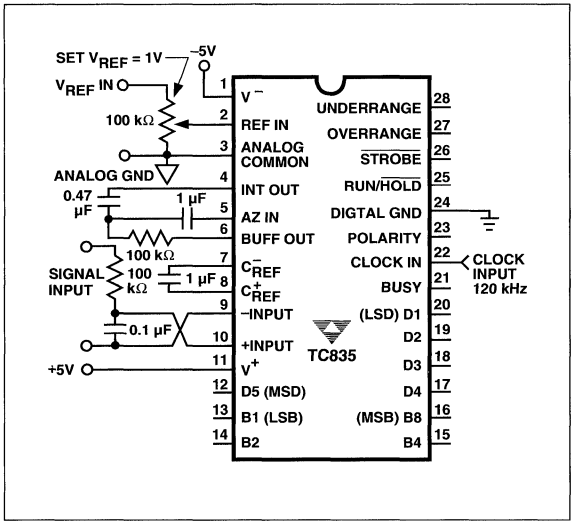


Figure 1 Test Circuit

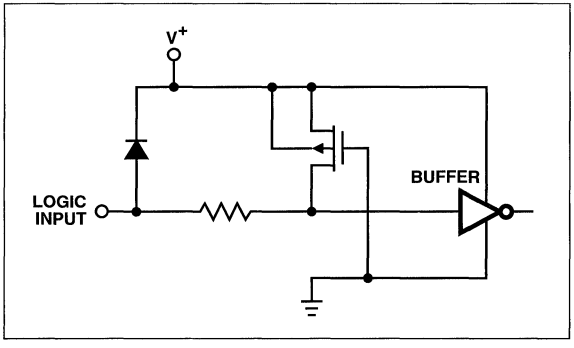


Figure 2 Digital Logic Input

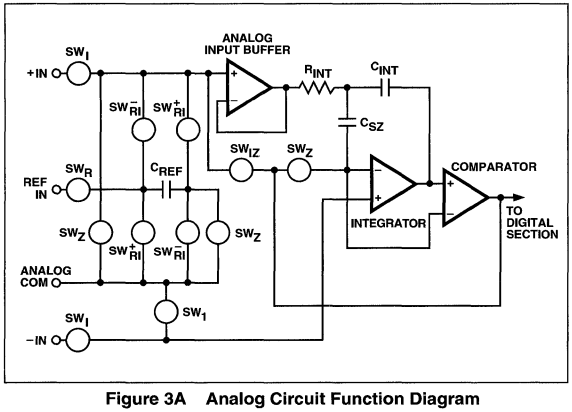


Figure 3A Analog Circuit Function Diagram

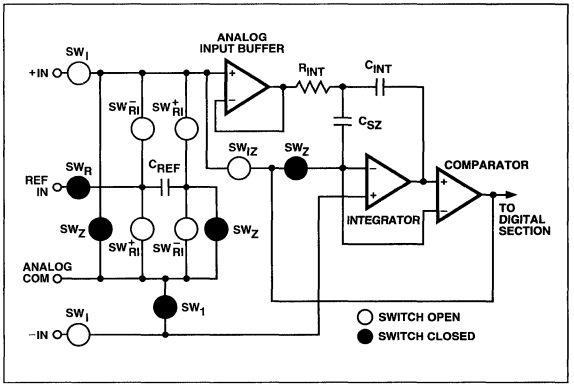


Figure 3B System Zero Phase

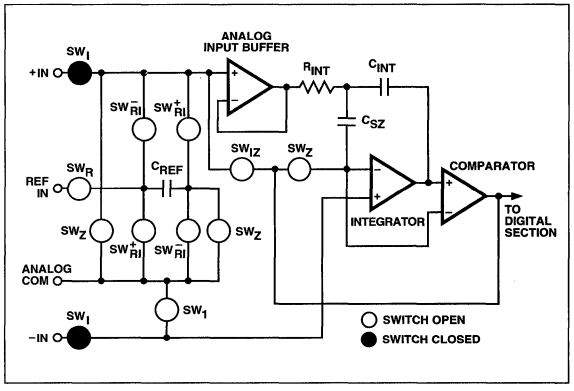


Figure 3C Input Signal Integration Phase

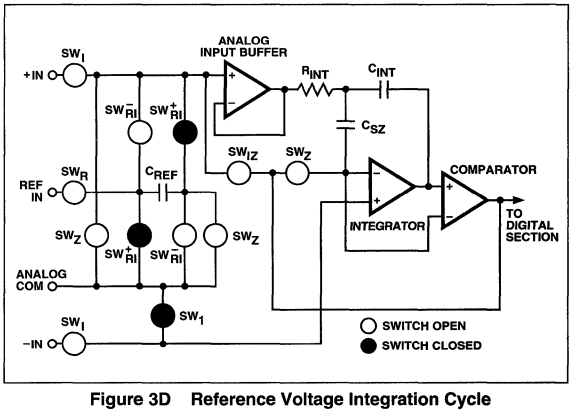


Figure 3D Reference Voltage Integration Cycle

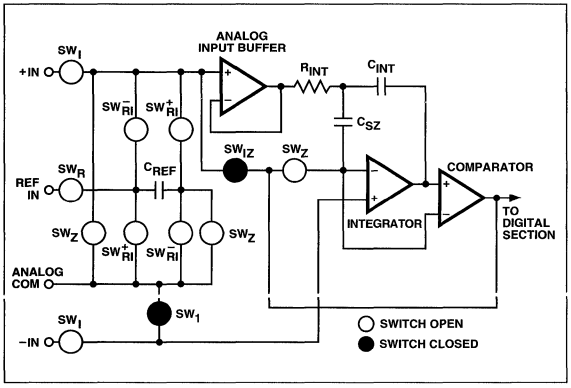


Figure 3E Integrator Output Zero Phase

GENERAL THEORY OF OPERATION

(All Pin Designations Refer to 28-Pin DIP)

Dual-Slope Conversion Principles

The TC835 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following the detailed TC835 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration
(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right].$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. (See Figure 4.)

TC835 Operational Theory

The TC835 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter overrange recovery time result.

The TC835 measurement cycle contains four phases:

(1) System zero
(2) Analog input signal integration
(3) Reference voltage integration
(4) Integrator output zero

Internal analog gate status for each phase is shown in Table I.

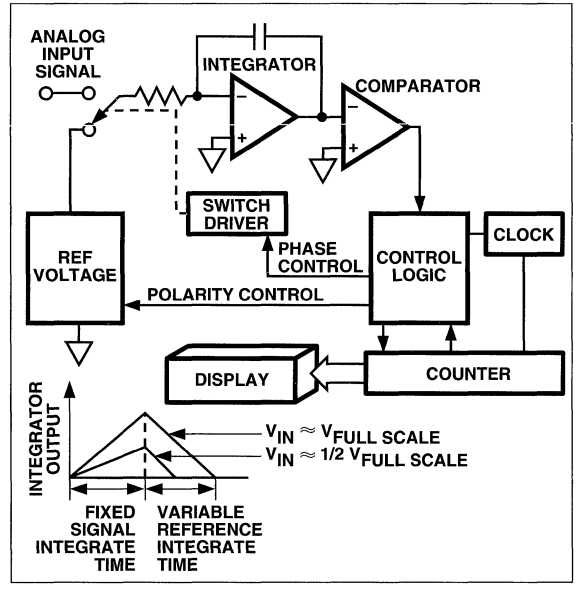


Figure 4 Basic Dual-Slope Converter

Table I. Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}	Reference Schematic
System Zero				Closed	Closed	Closed		3B
Input Signal Integration	Closed							3C
Reference Voltage Integration		Closed*				Closed		3D
Integrator Output Zero						Closed	Closed	3E

***NOTE:** Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

System Zero (Figure 3B)

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to ANALOG COMMON. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages.

Analog Input Signal Integration (Figure 3C)

The TC835 integrates the differential voltage between the +INPUT and –INPUT pins. The differential voltage must be within the device common-mode range; –1V from either supply rail, typically.

The input signal polarity is determined at the end of this phase.

Reference Voltage Integration (Figure 3D)

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}}\right].$$

Integrator Output Zero (Figure 3E)

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles.

Analog Section Functional Description

(In Reference to the 28-Pin Plastic Package)

Differential Inputs
(+INPUT, Pin 10 and –INPUT, Pin 9)

The TC835 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.5V below the positive supply to 1V above the negative supply. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full-scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

ANALOG COMMON Input (Pin 3)

ANALOG COMMON is used as the –INPUT return during auto-zero and deintegrate. If –INPUT is different from ANALOG COMMON, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, –INPUT will be set at a fixed, known voltage (power supply common, for instance). In this application, ANALOG COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to ANALOG COMMON.

REFERENCE Voltage Input (REF IN, Pin 2)

The REF IN input must be a positive voltage with respect to ANALOG COMMON. Two reference voltage circuits are shown in Figure 5.

TC835

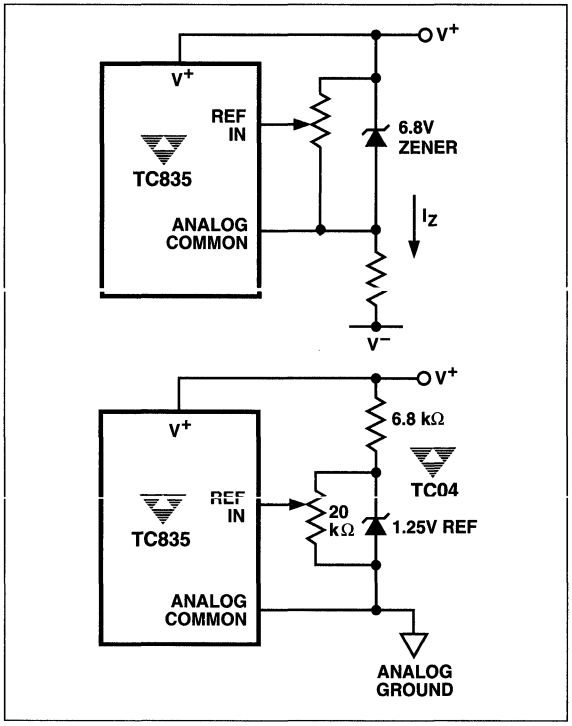


Figure 5 Using an External Reference

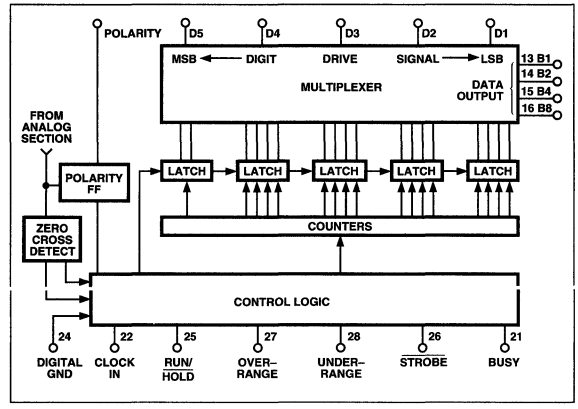


Figure 6 Digital Section Functional Diagram

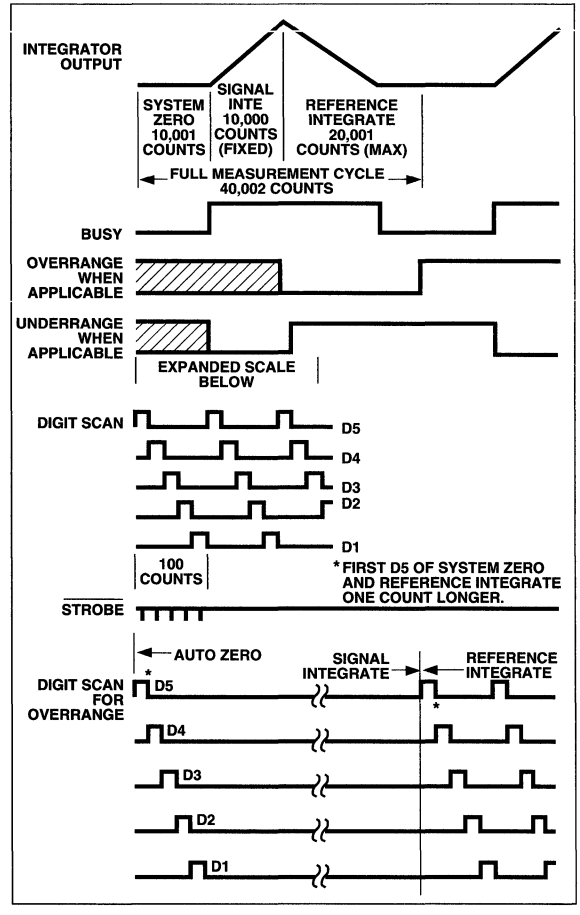


Figure 7 Timing Diagrams for Outputs

Digital Section Functional Description

The major digital subsystems within the TC835 are illustrated in Figure 6, with timing relationships shown in Figure 7. The multiplexed BCD output data can be displayed on an LCD display with the TC7211A (LCD) 4-digit display driver.

The digital section is best described through a discussion of the control signals and data outputs.

RUN/$\overline{\text{HOLD}}$ Input (Pin 25)

When left open, this pin assumes a logic "1" level. With a R/$\overline{\text{H}}$ = 1, the TC835 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to a logic "0," the measurement cycle in progress will be completed, and data held and displayed as long as the logic "0" condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ initiates a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001-count auto-zero phase. At the end of this phase the busy signal goes high.

$\overline{\text{STROBE}}$ Output (Pin 26)

During the measurement cycle, the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5, Figure 8).

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. (See Application Note 16.)

BUSY Output (Pin 21)

At the beginning of the signal-integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY, and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero cycle.

OVERRANGE Output (Pin 27)

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output is set to a logic "1." The overrange output register is set when BUSY goes low, and is reset at the beginning of the next reference-integration phase.

UNDERRANGE Output (Pin 28)

If the output count is 9% of full scale or less (≤1800 counts), the underrange register bit is set at the end of BUSY. The bit is set low at the next signal-integration phase.

POLARITY Output (Pin 23)

A positive input is registered by a logic "1" polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

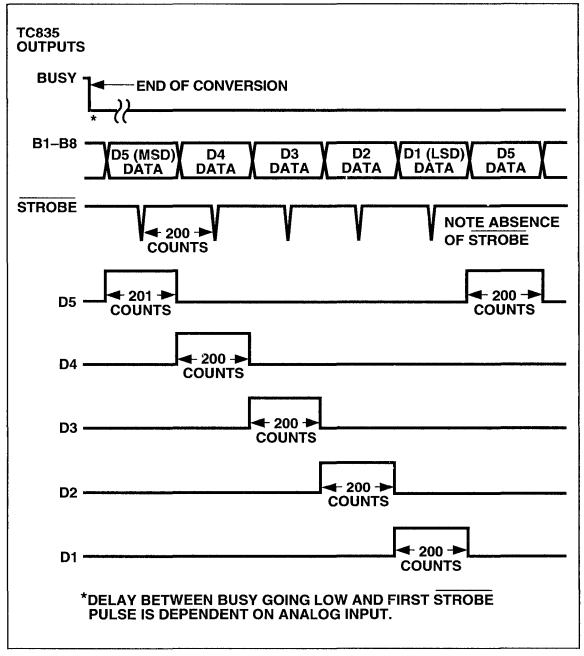


Figure 8 Strobe Signal Pulses Low Five Times per Conversion

The polarity bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

DIGIT Drive Outputs (Pins 12, 17, 18, 19 and 20)

Digit drive signals are positive-going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide, except D_5, which is 201 clock pulses wide.

All five digits are scanned continuously, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference-integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

BCD Data Outputs (Pins 13, 14, 15 and 16)

The binary coded decimal (BCD) bits B_8, B_4, B_2, B_1, are positive-true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition, all data bits are at a logic "0" state.

APPLICATIONS INFORMATION

Component Value Selection

The integrating resistor is determined by the full-scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage, with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 μA to 40 μA give good results. The exact value of an integrating resistor for a 20 μA current is easily calculated.

$$R_{INT} = \frac{\text{full-scale voltage}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing that ensures the tolerance build-up will not saturate the integrator swing (approximately 0.3V from either supply). For ±5V supplies and ANALOG COMMON tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent rollover or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half-scale 0.9999. any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitors

The size of the auto-zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power-on, or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high-quality reference be used where high-accuracy absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TC04A	TelCom Semiconductor
TC9491	TelCom Semiconductor

Conversion Timing

Line Frequency Rejection

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 200 kHz clock frequency will reject 60 Hz and 400 Hz noise. This corresponds to five readings per second.

Conversion Rate vs Clock Frequency

Oscillator Frequency (kHz)	Conversion Rate (Conv/Sec)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1200	30

Oscillator Frequency (kHz)	Line Frequency Rejection 60 Hz	50 Hz	400 Hz
50.000	•	•	•
53.333	—	—	•
66.667	•	—	•
80.000	—	—	•
83.333	—	•	•
100.000	•	•	•
125.000	—	•	•
133.333	—	—	•
166.667	—	—	•
200.000	•	—	•
250.000	—	•	•

The conversion rate is easily calculated:

$$\text{Conversion Rate (Readings 1/sec)} = \frac{\text{Clock Frequency (Hz)}}{4000}$$

Power Supplies and Grounds

Power Supplies

The TC835 is designed to work from ±5V supplies. For single +5V operation, a TC7660 can provide a –5V supply.

Grounding

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

Displays and Driver Circuits

TelCom Semiconductor manufactures two display decoder/driver circuits to interface the TC835 to an LCD or LED display. Each drive has 28 outputs for driving four 7-segment digit displays.

Device	Package	Description
TC7211AIPL	40-Pin Epoxy	4-Digit LCD Driver/Decoder
TC7212AIPL	40-Pin Epoxy	4-Digit LED Driver/Decoder

Several sources exist for LCD and LED display:

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
AND	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrance, CA 90505	LCD

High-Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 200 kHz (5 μs period), half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 at 250 μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 200 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the nonlinearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 200 kHz without this error, however, by using a low-value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

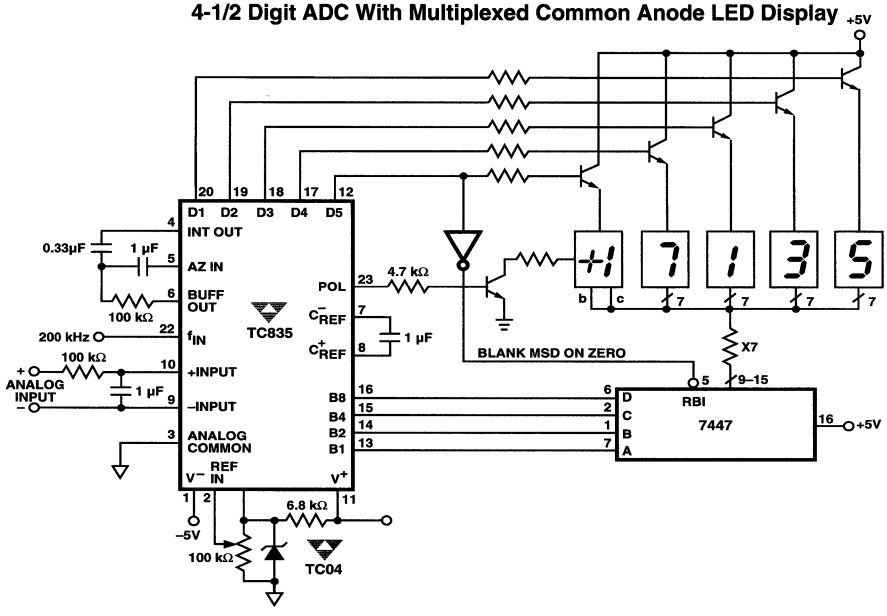
Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (deintegrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

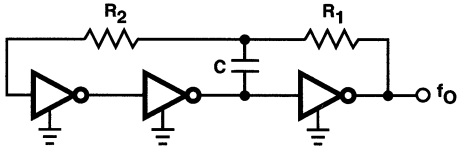
TC835

TYPICAL APPLICATIONS DIAGRAMS

4-1/2 Digit ADC With Multiplexed Common Anode LED Display



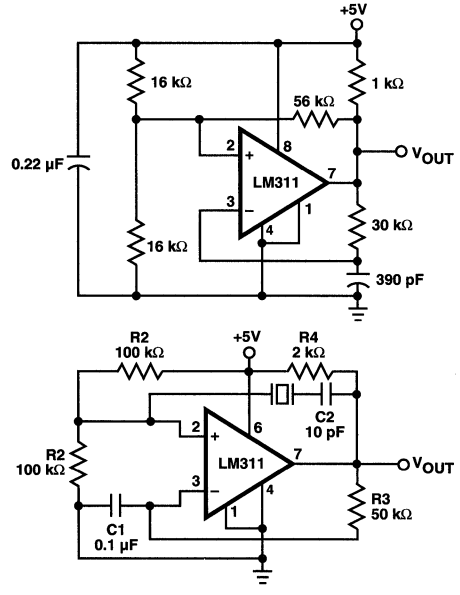
RC Oscillator Circuit



GATES ARE 74C04

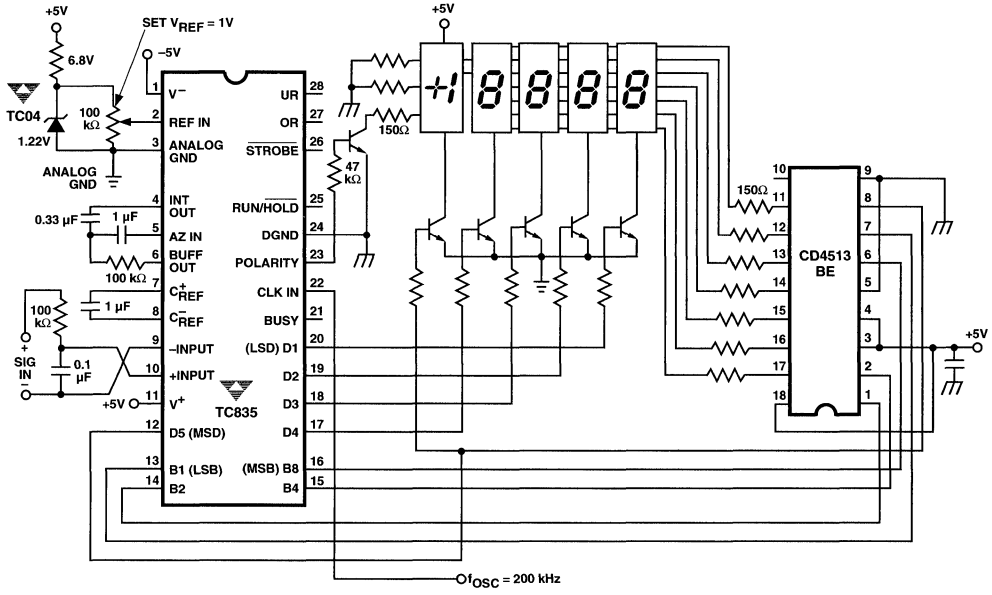
1. $f_O = \frac{1}{2\,C(0.41\,R_P + 0.7\,R_1)}$, $R_P = \frac{R_1\,R_2}{R_1 + R_2}$
   a. If $R_1 = R_2 = R_1$, $f \cong 0.55/RC$
   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$
   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$
2. Examples:
   a. f = 120 kHz, C = 420 pF
      $R_1 = R_2 \approx 10.9\ k\Omega$
   b. f = 120 kHz, C = 420 pF, R_2 = 50 kΩ
      R_1 = 8.93 kΩ
   c. f = 120 kHz, C = 220 pF, R_2 = 5 kΩ
      R_1 = 27.3 kΩ

Comparator Clock Circuits

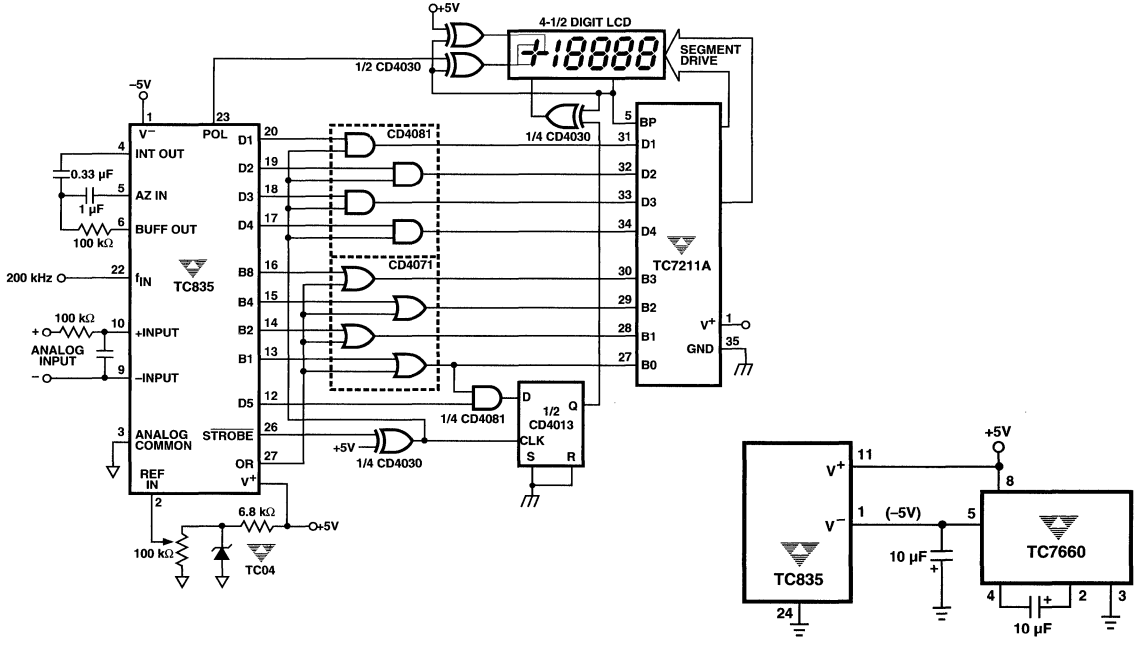


TYPICAL APPLICATIONS DIAGRAMS)

4-1/2 Digit ADC with Multiplexed Common Cathode LED Display

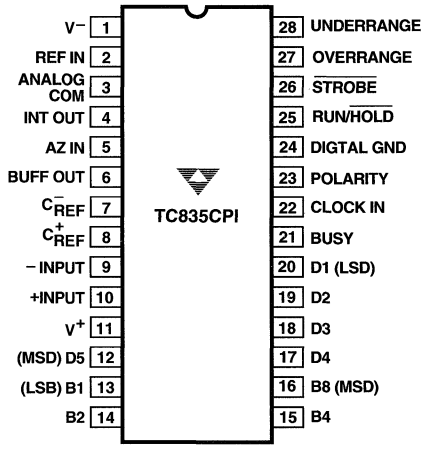


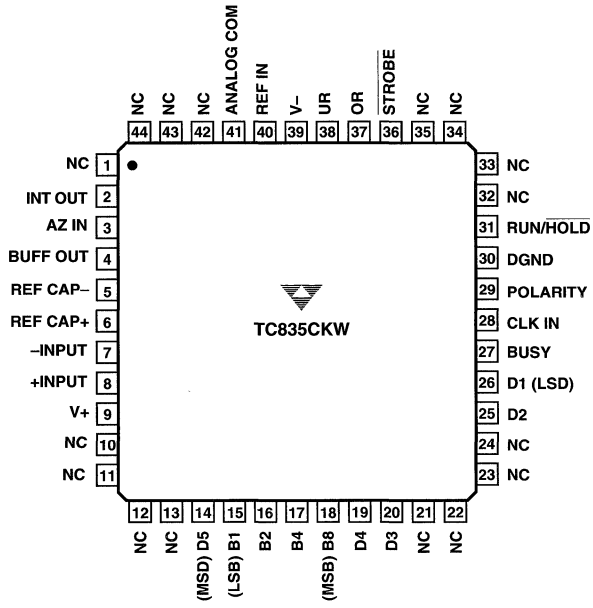
4-1/2 Digit ADC Interfaced to LCD With Digit Blanking on Overrange

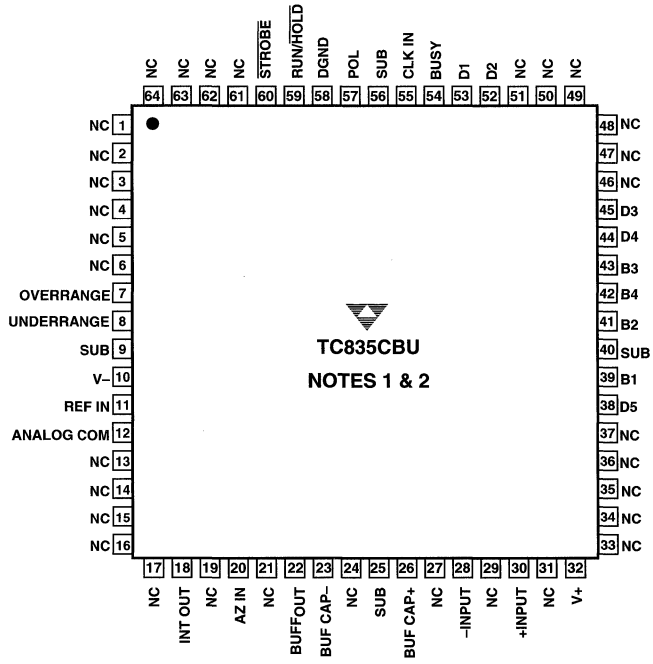


TC835

PIN CONFIGURATIONS







NOTES:

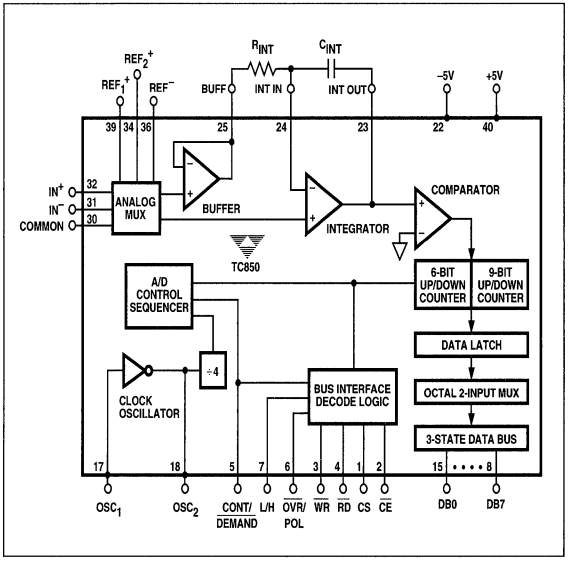
1. NC = No internal connection.
2. Pins 9, 25, 40 and 56 are connected to the die substrate. The potential at these pins is approximately V^+. No external connections should be made.

15-BIT, FAST-INTEGRATING CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 15-bit Resolution Plus Sign Bit
- Up to 40 Conversions per Second
- 12 Conversions per Second Guaranteed
- Integrating ADC Technique
  - — Monotonic
  - — High Noise Immunity
  - — Auto-Zeroed Amplifiers Eliminate Offset Trimming
- Wide Dynamic Range ..... 96 dB
- Low Input Bias Current ..... 30 pA
- Low Input Noise ..... 30 μV_{P-P}
- Sensitivity ..... 100 μV
- Flexible Operational Control
  - — Continuous or On-Demand Conversions
  - — Data Valid Output
- Bus Compatible, 3-State Data Outputs
  - — 8-Bit Data Bus
  - — Simple µP Interface
  - — Two Chip Enables
  - — Read ADC Result Like Memory
- ±5V Power Supply Operation ..... 20 mW
- 40-Pin Dual-in-Line or 44-Pin PLCC Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The TC850 is a monolithic CMOS analog-to-digital converter (ADC) with resolution of 15 bits plus sign. It combines a chopper-stabilized buffer and integrator with a unique multiple-slope integration technique that increases conversion speed. The result is 16 times improvement in speed over previous 15-bit, monolithic integrating ADCs (from 2.5 conversions per sec up to 40 per sec). Faster conversion speed is especially welcome in systems with human interface, such as digital scales.

The TC850 incorporates an ADC and a µP-compatible digital interface. Only a voltage reference and a few noncritical passive components are required to form a complete 15-bit plus sign ADC.

CMOS processing provides the TC850 with high-impedance differential inputs. Input bias current is typically only 30 pA, permitting direct interface to sensors. Input sensitivity of 100 µV per least significant bit (LSB) eliminates the need for precision external amplifiers. The internal amplifiers are auto-zeroed, guaranteeing a zero digital output with 0V analog input. Zero adjustment potentiometers or calibrations are not required.

The TC850 outputs data on an 8-bit, 3-state bus. Digital inputs are CMOS compatible; outputs are TTL/CMOS compatible. Chip-enable and byte-select inputs combined with an end-of-conversion output ensures easy interfacing to a wide variety of microprocessors. Conversions can be performed continuously or on command. In continuous mode, data is read as three consecutive bytes and manipulation of address lines is not required.

Operating from ±5V supplies, the TC850 dissipates only 20 mW. It is packaged in 40-pin plastic or ceramic dual-in-line packages (DIPs) and in a 44-pin plastic leaded chip carrier (PLCC), surface-mount package.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC850CLW	44-Pin PLCC	0°C to +70°C
TC850CPL	40-Pin Plastic DIP	0°C to +70°C
TC850ILW	44-Pin PLCC	– 25°C to +85°C
TC850IJL	40-Pin CerDIP	– 25°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_S^+ to GND) ..... +6V
Negative Supply Voltage (V_S^- to GND) ..... –9V
Analog Input voltage (IN^+ or IN^-) ..... V_S^+ to V_S^-
Voltage Reference Input
(REF_1^+, REF_1^-, REF_2^+) ..... V_S^+ to V_S^-
Logic Input Voltage ..... V_S^+ + 0.3V to GND – 0.3V
Current Into Any Pin ..... 10 mA
While Operating ..... 100 µA
Ambient Operating Temperature Range
C Device ..... 0°C to +70°C
I Device ..... – 25°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation
CerDIP ..... 1W @ +85°C
Plastic DIP ..... 0.5W @ +70°C
Plastic PLCC Package ..... 0.5W @ +70°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, f_{CLK} = 61.44 kHz, V_{FS} = 3.2768V, T_A = 25°C, Fig. 1 Test Circuit

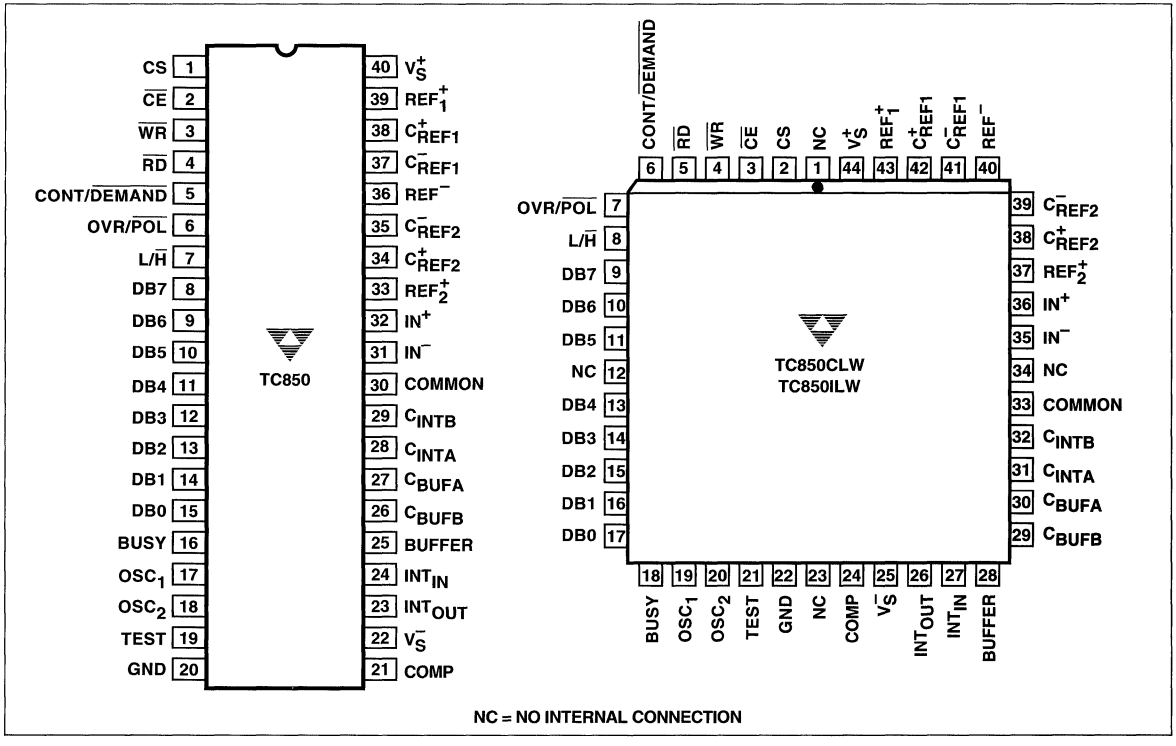
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Zero-Scale Error	V_{IN} = 0V		±0.25	±0.5	LSB
	End Point Linearity Error	$-V_{FS} \le V_{IN} \le +V_{FS}$	—	±1	±2	LSB
	Differential Nonlinearity		—	±0.1	±0.5	LSB
I_{IN}	Input Leakage Current	V_{IN} = 0V, T_A = 25°C 0°C ≤ T_A ≤ +70°C – 25° ≤ T_A ≤ +85°C	— — —	30 — 1.1	75 — 3	pA nA
V_{CMR}	Common-Mode Voltage Range	Over Operating Temperature Range	V_S^- + 1.5	—	V_S^+ – 1.5	V
CMRR	Common-Mode Rejection Ratio	V_{IN} = 0V, V_{CM} = ±1V	—	80	—	dB
	Full-Scale Gain Temperature Coefficient	External Ref Temperature Coefficient = 0 ppm/°C 0°C ≤ T_A ≤ +70°C	—	2	5	ppm/°C
	Zero-Scale Error Temperature Coefficient	V_{IN} = 0V 0°C ≤ T_A ≤ +70°C	—	0.3	2	µV/°C
	Full-Scale Magnitude Symmetry Error	V_{IN} = ±3.275V	—	0.5	2	LSB
e_N	Input Noise	Not Exceeded 95% of Time	—	30	—	μV_{P-P}
I_S^+	Positive Supply Current		—	2	3.5	mA
I_S^-	Negative Supply Current		—	2	3.5	mA
V_{OH}	Output High Voltage	I_O = 500 µA	3.5	4.9	—	V
V_{OL}	Output Low Voltage	I_O = 1.6 mA	—	0.15	0.4	V
I_{OP}	Output Leakage Current	Pins 8–15, High-Impedance State	—	0.1	1	µA
V_{IH}	Input High Voltage	Note 3	3.5	2.3	—	V
IL	Input Low Voltage	Note 3	—	2.1	1	V
I_{PU}	Input Pull-Up Current	Pins 2, 3, 4, 6, 7; V_{IN} = 0V	—	4	—	µA
I_{PD}	Input Pull-Down Current	Pins 1, 5; V_{IN} = 5V	—	14	—	µA
I_{OSC}	Oscillator Output Current	Pin 18, V_{OUT} = 2.5V	—	140	—	µA
C_{IN}	Input Capacitance	Pins 1–7, 17	—	1	—	pF
C_{OUT}	Output Capacitance	Pins 8–15, High-Impedance State	—	15	—	pF
t_{CE}	Chip-Enable Access Time	CS or $\overline{CE}$, $\overline{RD}$ = LOW (Note 1)	—	230	450	ns
t_{RE}	Read-Enable Access Time	CS = HIGH, $\overline{CE}$ = LOW (Note 1)	—	190	450	ns
t_{DHC}	Data Hold From CS or $\overline{CE}$	$\overline{RD}$ = LOW (Note 1)	—	250	450	ns
t_{DHR}	Data Hold From $\overline{RD}$	CS = HIGH, $\overline{CE}$ = LOW (Note 1)	—	210	450	ns
t_{OP}	OVR/$\overline{POL}$ Data Access Time	CS = HIGH, $\overline{CE}$ = LOW, $\overline{RD}$ = LOW (Note 1)	—	140	300	ns

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{LH}	Low/High Byte Access Time	CS = HIGH, $\overline{CE}$ = LOW, $\overline{RD}$ = LOW (Note 1)	—	140	300	ns
	Clock Setup Time	Positive or Negative Pulse Width	100	—	—	ns
t_{WRE}	$\overline{RD}$ Minimum Pulse Width	CS = HIGH, $\overline{CE}$ = LOW (Note 2)	450	230	—	ns
t_{WRD}	$\overline{RD}$ Minimum Delay Time	CS = HIGH, $\overline{CE}$ = LOW (Note 2)	150	50	—	ns
t_{WWR}	$\overline{WR}$ Minimum Pulse Width	CS = HIGH, $\overline{CE}$ = LOW, Demand Mode	75	25	—	ns
	Clock Setup Time	Positive or Negative Pulse Width	100			ns

NOTES: 1. Demand mode, CONT/$\overline{DEMAND}$ = LOW. Figure 10 timing diagram. C_L = 100 pF.
2. Continuous mode, CONT/$\overline{DEMAND}$ = HIGH. Figure 12 timing diagram.
3. Digital inputs have CMOS logic levels and internal pull-up/pull-down resistors. For TTL compatibility, external pull-up resistors to V_{CC} are recommended.

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

TC850

PIN DESCRIPTIONS

40-Pin DIP Pin No.	Symbol	Description
1	CS	Chip select, active HIGH. Logically ANDed with $\overline{CE}$ to enable read and write inputs. (See note 4.)
2	$\overline{CE}$	Chip enable, active LOW. (See note 5.)
3	$\overline{WR}$	Write input, active LOW. When chip is selected (CS = HIGH and CE = LOW) and in demand mode (CONT/$\overline{DEMAND}$ = LOW), a logic LOW on $\overline{WR}$ starts a conversion. (See note 4.)
4	$\overline{RD}$	Read input, active LOW. When CS = HIGH and $\overline{CE}$ = LOW, a logic LOW on $\overline{RD}$ enables the 3-state data outputs. (See note 5.)
5	CONT/$\overline{DEMAND}$	Conversion control input. When CONT/$\overline{DEMAND}$ = LOW, conversions are initiated by the $\overline{WR}$ input. When CONT/$\overline{DEMAND}$ = HIGH, conversions are performed continuously. (See note 4.)
6	OVR/$\overline{POL}$	Overrange/polarity data-select input. When making conversions in the demand mode (CONT/$\overline{DEMAND}$ = LOW), OVR/$\overline{POL}$ controls the data output on DB7 when the high-order byte is active. (See note 5.)
7	$\overline{L/H}$	Low/high byte-select input. When CONT/$\overline{DEMAND}$ = LOW, this input controls whether low-byte or high-byte data is enabled on DB0 through DB7. (See note 5.)
8	DB7	Most significant data bit output. When reading the A/D conversion result, the polarity, overrange, and DB7 data are output on this pin. (See text.)
9–15	DB6–DB0	Data outputs DB6–DB0. 3-state, bus compatible.
16	BUSY	A/D conversion status output. BUSY goes to a logic HIGH at the beginning of the deintegrate phase and goes LOW when conversion is complete. The falling edge of BUSY can be used to generate a µP interrupt.
17	OSC_1	Crystal oscillator connection or external oscillator input.
18	OSC_2	Crystal oscillator connection.
19	TEST	For factory testing purposes only. Do not make external connection to this pin.
20	DGND	Digital ground connection.
21	COMP	Connection for comparator auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
22	V_S^-	Negative power supply connection, typically –5V.
23	INT_{OUT}	Output of the integrator amplifier. Connect to C_{INT}.
24	INT_{IN}	Input to the integrator amplifier. Connect to summing node of R_{INT} and C_{INT}.
25	BUFFER	Output of the input buffer. Connect to R_{INT}.
26	C_{BUFB}	Connection for buffer auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
27	C_{BUFA}	Connection to buffer auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
28	C_{INTA}	Connection for integrator auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
29	C_{INTB}	Connection for integrator auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
30	COMMON	Analog common.
31	IN^-	Negative differential analog input.
30	COMMON	Analog common.
33	REF_2^+	Positive input for reference voltage V_{REF2}. ($V_{REF2} = V_{REF1}/64$)
34	C_{REF2}^+	Positive connection for V_{REF2} reference capacitor.
35	C_{REF2}^-	Negative connection for V_{REF2} reference capacitor.
36	REF^-	Negative input for reference voltages.
37	C_{REF1}^-	Negative connection for V_{REF1} reference capacitor.
38	C_{REF1}^+	Positive connection for V_{REF1} reference capacitor.
39	REF_1^+	Positive input for V_{REF1}.
40	V_S^+	Positive power supply connection, typically +5V.

NOTES: 4. This pin incorporates a pull-down resistor to DGND.
5. This pin incorporates a pull-up resistor to V_S^+.

THEORY OF OPERATION

The TC850 is a multiple-slope, integrating analog-to-digital converter (ADC). The multiple-slope conversion process, combined with chopper-stabilized amplifiers, results in a significant increase in ADC speed, while maintaining very high resolution and accuracy.

Dual-Slope Conversion Principles

The conventional dual-slope converter measurement cycle (shown in Figure 2A) has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, complete conversion requires the integrator output to "ramp-up" and "ramp-down." Most dual-slope converters add a third phase, auto-zero. During auto-zero, offset voltages of the input buffer, integrator, and comparator are nulled, thereby eliminating the need for zero-offset adjustments.

Dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. By converting the unknown analog input voltage into an easily-measured function of time, the dual-slope converter reduces the need for expensive, precision passive components.

Noise immunity is an inherent benefit of the integrating conversion method. Noise spikes are integrated, or averaged, to zero during the integration period. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

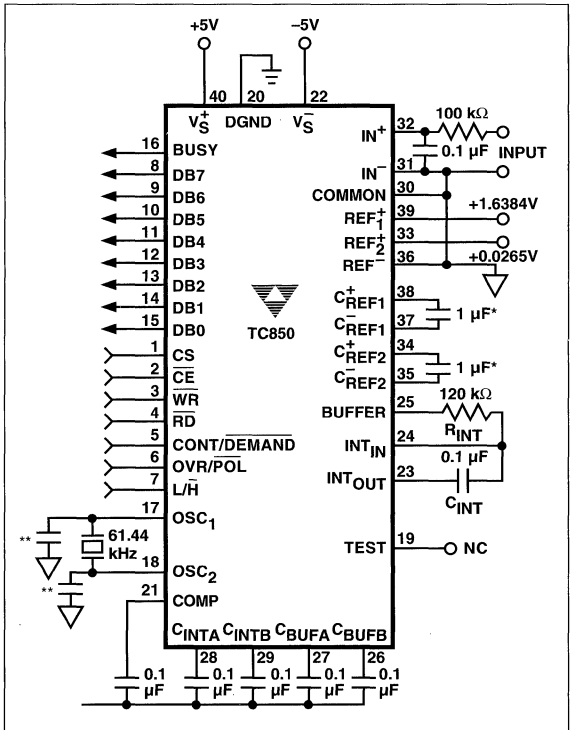
where: V_R = Reference voltage
t_{SI} = Signal integration time (fixed)
t_{RI} = Reference voltage integration time (variable).

Multiple-Slope Conversion Principles

One limitation of the dual-slope measurement technique is conversion speed. In a typical dual-slope method, the auto-zero and integrate times are each one-half of the deintegrate time. For a 15-bit conversion, $2^{14} + 2^{14} + 2^{15}$ (65,536) clock pulses are required for auto-zero, integrate, and deintegrate phases, respectively. The large number of clock cycles effectively limits the conversion rate to about 2.5 conversions per second, when a typical analog CMOS fabrication process is used.

The TC850 uses a multiple-slope conversion technique to increase conversion speed (Figure 2B). This technique makes use of a two-slope deintegration phase and permits 15-bit resolution up to 40 conversions per second.

During the TC850's deintegration phase, the integration capacitor is rapidly discharged to yield a resolution of 9 bits. At this point, some charge will remain on the capacitor. This remaining charge is then slowly deintegrated, producing an



NOTES: Unless otherwise specified, all 0.1 µF capacitors are film dielectric. Ceramic capacitors are not recommended.
NC = No internal connection.
* Polypropylene capacitors.
** 100 pF Mica capacitors.

Figure 1 Standard Circuit Configuration

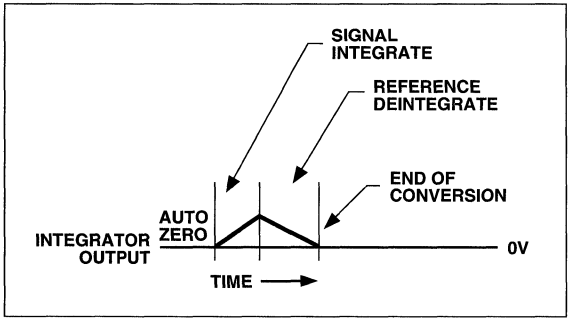


Figure 2A Dual-Slope ADC Cycle

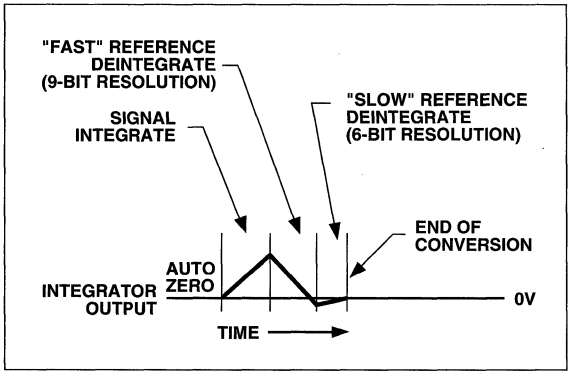


Figure 2B "Fast-Slow" Reference Deintegrate Cycle

additional 6 bits of resolution. The result is 15 bits of resolution achieved with only $2^9 + 2^6$ (512 + 64, or 576) clock pulses for deintegration. A complete conversion cycle occupies only 1280 clock pulses.

In order to generate "fast-slow" integration phases, two voltage references are required. The primary reference (V_{REF1}) is set to one-half of the full-scale voltage (typically V_{REF1} = 1.6384V, and V_{FS} = 3.2768V). The secondary voltage reference (V_{REF2}) is set to $V_{REF1}/64$ (typically 25.6 mV). To maintain 15-bit linearity, a tolerance of 0.5% for V_{REF2} is recommended.

ANALOG SECTION DESCRIPTION

The TC850 analog section consists of an input buffer amplifier, integrator amplifier, comparator, and analog switches. A simplified block diagram is shown in Figure 3.

Conversion Timing

Each conversion consists of three phases: (1) Zero Integrator, (2) Signal Integrate, and (3) Reference Integrate (or Deintegrate). Each conversion cycle requires 1280 internal clock cycles (Figure 4).

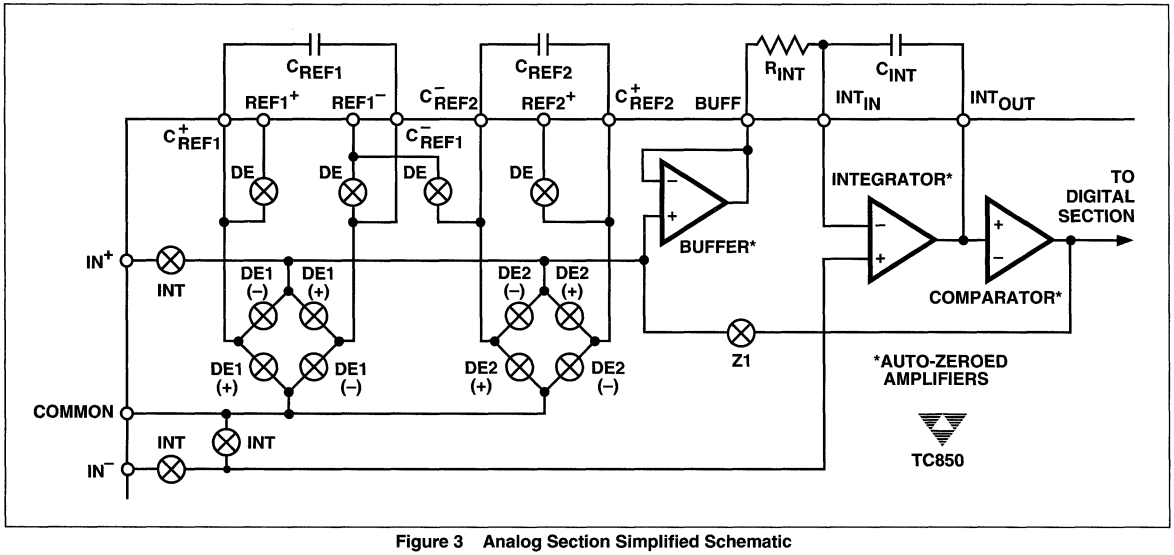


Figure 3 Analog Section Simplified Schematic

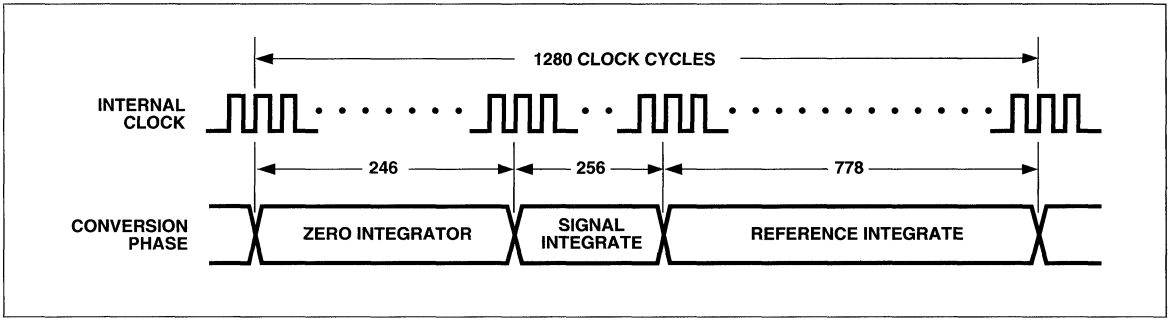


Figure 4 Conversion Timing

Zero-Integrator Phase

During the zero-integrator phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero-input condition. At the same time, a feedback loop is closed around the input buffer, integrator, and comparator. The feedback loop ensures the integrator output is near 0V before the signal-integrate phase begins.

During this phase, a chopper-stabilization technique is used to cancel offset errors in the input buffer, integrator, and comparator. Error voltages are stored on the C_{BUFF}, C_{INT}, and COMP capacitors. The zero-integrate phase requires 246 clock cycles.

Signal-Integrate Phase

The zero-integrator loop is opened and the internal differential inputs are connected to IN^+ and IN^-. The differential input signal is integrated for a fixed time period. The TC850 signal-integrate period is 256 clock periods, or counts. The crystal oscillator frequency is ÷4 before clocking the internal counters.

The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 256$$

Reference-Integrate Phase

During reference-integrate phase, the charge stored on the integrator capacitor is discharged. The time required to discharge the capacitor is proportional to the analog input voltage.

The reference integrate phase is divided into three subphases: (1) fast, (2) slow, and (3) overrange deintegrate.

During fast deintegrate, V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor (C_{REF1}). The integrator capacitor is rapidly discharged for a maximum of 512 internal clock pulses, yielding 9 bits of resolution.

During the slow deintegrate phase, the internal V_{IN}^+ node is now connected to the C_{REF2} capacitor, and the residual charge on the integrator capacitor is further discharged a maximum of 64 clock pulses. At this point, the analog input voltage has been converted with 15 bits of resolution.

If the analog input is greater than full scale, the TC850 performs up to three overrange deintegrate subphases. Each subphase occupies a maximum of 64 clock pulses. The overrange feature permits analog inputs up to 192 LSBs greater than full scale to be correctly converted. This feature permits the user to digitally null up to 192 counts of input offset, while retaining full 15-bit resolution.

In addition to 512 counts of fast, 64 counts of slow, and 192 counts of overrange deintegrate, the reference-integrate phase uses 10 clock pulses to permit internal nodes to settle. Therefore, the reference integrate cycle occupies 778 clock pulses.

Pin Description (Analog)

Differential Inputs (IN^+ and IN^-)

The analog signal to be measured is applied at the IN^+ and IN^- inputs. The differential input voltage must be within the common-mode range of the converter. The input common-mode range extends from V_S^+ –1.5V to V_S^- +1.5V. Within this common-mode voltage range, an 86 dB CMRR is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its available swing has been used up by the positive common-mode voltage. For applications where maximum common-mode range is critical, integrator swing can be reduced. The integrator output can swing within 0.4V of either supply without loss of linearity.

Differential Reference (V_{REF})

The TC850 requires two reference voltage sources in order to generate the "fast-slow" deintegrate phases. The main voltage reference (V_{REF1}) is applied between the REF_1^+ and REF^- pins. The secondary reference (V_{REF2}) is applied between the REF_2^+ and REF^- pins.

The reference voltage inputs are fully differential, and the reference voltage can be generated anywhere within the power supply voltage of the converter. However, to minimize roll-over error, especially at high conversion rates, keep the reference common-mode voltage (i.e., REF^-) near or at the analog common potential. All voltage reference inputs are high impedance. Average reference input current is typically only 30 pA.

Analog Common (COMMON)

Analog common is used as the IN^- return during the zero-integrator and deintegrate phases of each conversion. If IN^- is at a different potential than analog common, a common-mode voltage exists in the system. This signal is rejected by the 86 dB CMRR of the converter. However, in most applications, IN^- will be set at a fixed, known voltage (power supply common, for instance). In this case, analog common should be tied to the same point so that the common-mode voltage is eliminated.

DIGITAL SECTION DESCRIPTION

The TC850 digital section consists of two sets of conversion counters, control and sequencing logic, clock oscillator and divider, data latches, and an 8-bit, 3-state interface bus. A simplified schematic of the bus interface logic is shown in Figure 5.

Clock Oscillator

The TC850 includes a crystal oscillator on-chip. All that is required is to connect a crystal across OSC_1 and OSC_2 pins, and to add two inexpensive capacitors (Figure 1). The oscillator output is ÷4 prior to clocking the A/D internal counters. For example, a 100 kHz crystal produces a system clock frequency of 25 kHz. Since each conversion requires 1280 clock periods, in this case the conversion rate will be 25,000/1280, or 19.5 conversions per second.

In most applications, however, an external clock is divided down from the microprocessor clock. In this case, the OSC_1 pin is used as the external oscillator input and OSC_2 is left unconnected. The external clock driver should swing from digital ground to V_S^+. The ÷4 function is active for both external clock and crystal oscillator operations.

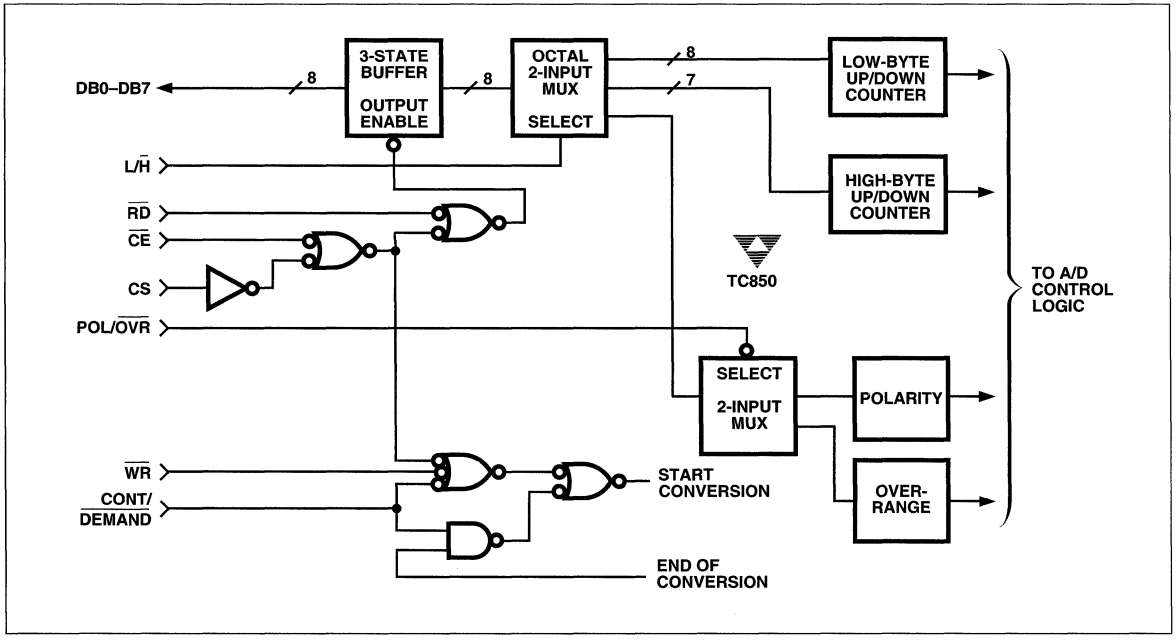


Figure 5 Bus Interface Simplified Schematic

Digital Operating Modes

Two modes of operation are available with the TC850, continuous conversions and on-demand. The operating mode is controlled by the CONT/$\overline{\text{DEMAND}}$ input. The bus interface method is different for continuous and demand modes of operation.

Demand Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is low, the TC850 performs one conversion each time the chip is selected and the $\overline{\text{WR}}$ input is pulsed low. Data is valid on the falling edge of the BUSY output and can be accessed using the interface truth table (Table I).

Continuous Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is high, the TC850 continuously performs conversions. Data will be valid on the falling edge of the BUSY output, and remains valid for 443-1/2 clock cycles.

The low/high (L/$\overline{\text{H}}$) byte-select and overrange/polarity (OVR/$\overline{\text{POL}}$) inputs are disabled during continuous mode operation. Data must be read in three consecutive bytes, as shown in Table I.

NOTE: In continuous mode, the conversion result must be read within 443-1/2 clock cycles of the BUSY output falling edge. After this time (i.e., 1/2 clock cycle before BUSY goes high) the internal counters are reset and the data is lost.

Table I. Bus Interface Truth Table

$\overline{\text{CE}}$•$\overline{\text{CS}}$	$\overline{\text{RD}}$	CONT/$\overline{\text{DEMAND}}$	L/$\overline{\text{H}}$	OVR/$\overline{\text{POL}}$	DB7	DB6–DB0
Pins 1 and 2	Pin 4	Pin 5	Pin 7	Pin 6	Pin 8	Pin 9–Pin 15 (Note 1)
0	0	0	0	0	"1" = Input Positive	Data Bits 14–8
0	0	0	0	1	"1" = Input Overrange (Note 2)	Data Bits 14–8
0	0	0	1	X	Data Bit 7	Data Bits 6–0
0	0	1	X	X	Note 3	
0	1	X	X	X	High-Impedance State	
1	X	X	X	X	High-Impedance State	

NOTES: 1. Pin numbers refer to 40-pin DIP.

2. Extended overrange operation: Although rated at 15 bits (±32,767 counts) of resolution, the TC850 provides an additional 191 counts above full scale. For example, with a full-scale input of 3.2768V, the maximum analog input voltage which will be properly converted is 3.2958V. The extended resolution is signified by the overrange bit being high and the low-order byte contents being between 0 and 190. For example, with a full-scale voltage of 3.2768V:

V_{IN}	Overrange Bit	Low Byte	Data Bits 14–8
3.2767V	Low	255_{10}	127_{10}
3.2768V	High	000_{10}	0_{10}
3.2769V	High	001_{10}	0_{10}
3.2867V	High	099_{10}	0_{10}

3. Continuous mode data transfer:
   a. In continuous mode, data MUST be read in three sequential bytes after the BUSY output goes low:
      (1) The first byte read will be the high-order byte, with DB7 = polarity.
      (2) The second byte read will contain the low-order byte.
      (3) The third byte read will again be the high-order byte, but with DB7 = overrange.
   b. All three data bytes must be read within 443-1/2 clock cycles after the falling edge of BUSY.
   c. The $\overline{\text{RD}}$ input must go high after each byte is read, so that the internal byte counter will be incremented. However, the CS and $\overline{\text{CE}}$ inputs can remain enabled through the entire data transfer sequence.

Pin Description (Digital)

Chip Select and Chip Enable (CS and $\overline{CE}$)

The CS and $\overline{CE}$ inputs permit easy interfacing to a variety of digital bus systems. $\overline{CE}$ is active LOW while CS is active HIGH. These inputs are logically ANDed internally and are used to enable the $\overline{RD}$ and $\overline{WR}$ inputs.

Write Enable Input ($\overline{WR}$)

The write input is used to initiate a conversion when the TC850 is in demand mode. CS and $\overline{CE}$ must be active for the $\overline{WR}$ input to be recognized. The status of the data bus is meaningless during the $\overline{WR}$ pulse, because no data is actually written into the TC850.

Read Enable Input ($\overline{RD}$)

The read input, combined with CS and $\overline{CE}$, enables the 3-state data bus outputs. Also, in continuous mode, the rising edge of the $\overline{RD}$ input activates an internal byte counter to sequentially read the three data bytes.

Low/High Byte Select (L/$\overline{H}$)

The L/$\overline{H}$ input determines whether the low (least significant) byte or high (most significant) byte of data is placed on the 3-state data bus. This input is meaningful only when the TC850 is in the demand mode. In the continuous mode, data must be read in three predetermined bytes, so the L/$\overline{H}$ input is ignored.

Overrange/Polarity Bit Select (OVR/$\overline{POL}$)

The TC850 provides 15 bits of resolution, plus polarity and overrange bits. Thus, 17 bits of information must be transferred on an 8-bit data bus. To accomplish this, the overrange and polarity bits are multiplexed onto data bit DB7 of the most significant byte. When OVR/$\overline{POL}$ is HIGH, DB7 of the high byte contains the overrange status (HIGH = analog input overrange, LOW = input within full scale). When OVR/$\overline{POL}$ is LOW, DB7 is HIGH for positive analog input polarity and LOW for negative polarity. The OVR/$\overline{POL}$ input is meaningful only when CS, $\overline{CE}$, and $\overline{RD}$ are active, and L/$\overline{H}$ is LOW (i.e., the most significant byte is selected). OVR/$\overline{POL}$ is ignored when the TC850 is in continuous mode.

Continuous/Demand Mode Input (CONT/$\overline{DEMAND}$)

This input controls the TC850 operating mode. When CONT/$\overline{DEMAND}$ is HIGH, the TC850 performs conversions continuously. In continuous mode, data must be read in the prescribed sequence shown in Table I. Also, all three data bytes must be read within 443-1/2 internal clock cycles after the BUSY output goes low. After 443-1/2 clock cycles data will be lost.

When CONT/$\overline{DEMAND}$ is LOW, the TC850 begins a conversion each time CS and $\overline{CE}$ are active and $\overline{WR}$ is pulsed LOW. The conversion is complete and data can be read after the falling edge of the BUSY output. In demand mode, data can be read in any sequence, and remains valid until WR is again pulsed LOW.

Busy Output (BUSY)

The BUSY output is used to convey an end-of-conversion to external logic. BUSY goes HIGH at the beginning of the deintegrate phase and goes LOW at the end of the conversion cycle. Data is valid on the falling edge of BUSY. The output-high period is fixed at 836 clock periods, regardless of the analog input value. BUSY is active during continuous and demand mode operation.

This output can also be used to generate an end-of-conversion interrupt in µP-based systems. Noninterrupt-driven systems can poll BUSY to determine when data is valid.

ANALOG SECTION APPLICATIONS

Component Selection

Reference Voltage

The typical value for reference voltage V_{REF1} is 1.6384V. This value yields a full-scale voltage of 3.2768V and resolution of 100 µV per step. The V_{REF2} value is derived by dividing V_{REF1} by 64. Thus, typical V_{REF2} value is 1.6384V/64, or 25.6 mV. The V_{REF2} value should be adjusted within ±1% to maintain 15-bit accuracy for the total conversion process; i.e.,

$$V_{REF2} = \frac{V_{REF1}}{64} \pm 1\%.$$

The reference voltage is not limited to exactly 1.6384V, however, because the TC850 performs a ratiometric conversion. Therefore, the conversion result will be:

$$\text{Digital counts} = \frac{V_{IN}}{V_{REF1}} \bullet 16384.$$

The full-scale voltage can range from 3.2V to 3.5V. Full-scale voltages of less than 3.2V will result in increased noise in the least significant bits, while a full-scale above 3.5V will exceed the input common-mode range.

Integration Resistor

The TC850 buffer supplies 25 µA of integrator charging current with minimal linearity error. R_{INT} is easily calculated:

$$R_{INT} = \frac{V_{FULL\ SCALE}}{25\ \mu A}.$$

For a full-scale voltage of 3.2768V, values of R_{INT} between 120 kΩ and 150 kΩ are acceptable.

Integration Capacitor

The integration capacitor should be selected to produce an integrator swing of ≈4V at full scale. The capacitor value is easily calculated:

$$C = \frac{V_{FS}}{R_{INT}} \bullet \frac{4 \bullet 256}{4V \bullet f_{CLOCK}},$$

where f_{CLOCK} is the crystal or external oscillator frequency and V_{FS} is the maximum input voltage.

The integration capacitor should be selected for low dielectric absorption to prevent roll-over errors. A polypropylene, polyester or polycarbonate dielectric capacitor is recommended.

Reference Capacitors

The reference capacitors require a low leakage dielectric, such as polypropylene, polyester or polycarbonate. A value of 1 µF is recommended for operation over the temperature range. If high-temperature operation is not required, the C_{REF} values can be reduced.

Auto-Zero Capacitors

Five capacitors are required to auto-zero the input buffer, integrator amplifier, and comparator. Recommended capacitors are 0.1 µF film dielectric (such as polyester or polypropylene). Ceramic capacitors are not recommended.

DIGITAL SECTION APPLICATION

Oscillator

The TC850 may operate with a crystal oscillator. The crystal selected should be designed for a Pierce oscillator, such as an AT-cut quartz crystal. The crystal oscillator schematic is shown in Figure 6.

Since low frequency crystals are very large and ceramic resonators are too lossy, the TC850 clock should be derived from an external source, such as a microprocessor clock. The clock should be input on the OSC_1 pin and no connection should be made to the OSC_2 pin. The external clock should swing between DGND and V_S^+.

Since oscillator frequency is ÷4 internally and each conversion requires 1280 internal clock cycles, the conversion time will be:

$$\text{Conversion time} = f_{CLOCK} \times 4 \times 1280.$$

An important advantage of the integrating ADC is the ability to reject periodic noise. This feature is most often used to reject line frequency (50 Hz or 60 Hz) noise. Noise rejection is accomplished by selecting the integration period equal to one or more line frequency cycles. The desired clock frequency is selected as follows:

$$f_{CLOCK} = f_{NOISE} \times 4 \times 256,$$

where f_{NOISE} is the noise frequency to be rejected, 4 represents the clock divider, and 256 is the number of integrate cycles.

For example, 60 Hz noise will be rejected with a clock frequency of 61.44 kHz, giving a conversion rate of 12 conversions/sec. Integer submultiples of 61.44 kHz (such as 30.72 kHz, etc.) will also reject 60 Hz noise. For 50 Hz noise rejection, a 51.2 kHz frequency is recommended.

If noise rejection is not important, other clock frequencies can be used. The TC850 will typically operate at conversion rates ranging from 3 to 40 conversions/sec, corresponding to oscillator frequencies from 15.36 kHz to 204.8 kHz.

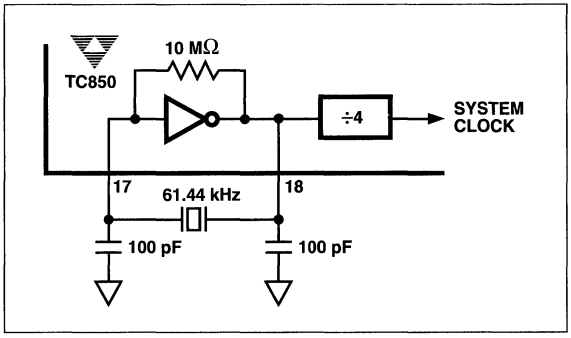


Figure 6 Crystal Oscillator Schematic

Data Bus Interfacing

The TC850 provides an easy and flexible digital interface. A 3-state data bus and six control inputs permit the TC850 to be treated as a memory device, in most applications. The conversion result can be accessed over an 8-bit bus or via a µP I/O port.

A typical µP bus interface for the TC850 is shown in Figure 7. In this example, the TC850 operates in the demand mode, and conversion begins when a write operation is performed to any decoded address space. The BUSY output interrupts the µP at the end-of-conversion.

The A/D conversion result is read as three memory bytes. The two LSBs of the address bus select high/low byte and overrange/polarity bit data, while high-order address lines enable the $\overline{CE}$ input.

Figure 8 shows a typical interface to a µP I/O port or single-chip µC. The TC850 operates in the continuous mode, and can either interrupt the µC/µP or be polled with an input pin.

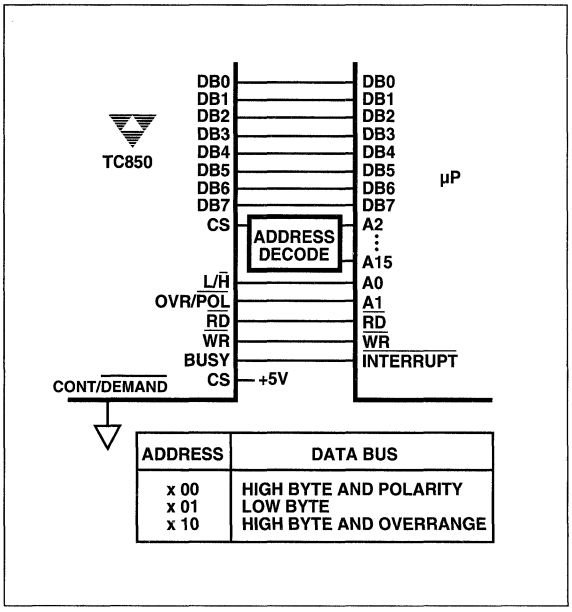


Figure 7 Interface to Typical µP Data Bus

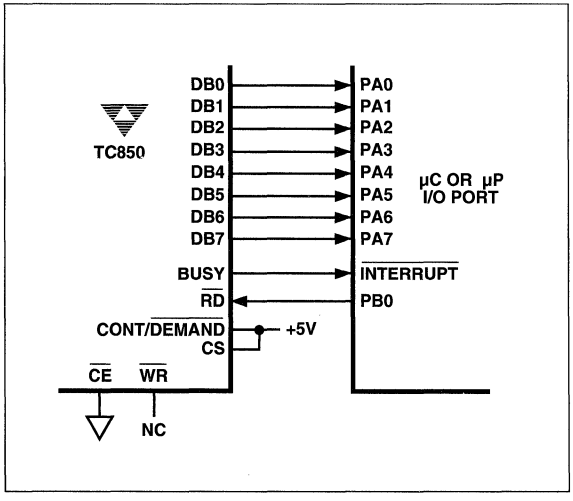


Figure 8 Interface to Typical µP I/O Port or Single-Chip µC

Since the PA0–PA7 inputs are dedicated to reading A/D data, the A/D CS/$\overline{CE}$ inputs can be enabled continuously. In continuous mode, data must be read in 3 bytes, as shown in Table I. The required $\overline{RD}$ pulses are provided by a µC/µP output pin.

The circuit of Figure 8 can also operate in the demand mode, with the start-up conversion strobe generated by a µC/µP output pin. In this case, the L/$\overline{H}$ and CONT/$\overline{DEMAND}$ inputs can be controlled by I/O pins and the $\overline{RD}$ input connected to digital ground.

Demand Mode Interface Timing

When CONT/$\overline{DEMAND}$ input is LOW, the TC850 performs a conversion each time $\overline{CE}$ and CS are active and $\overline{WR}$ is strobed LOW.

The demand mode conversion timing is shown in Figure 9. BUSY goes LOW and data is valid 1155 clock pulses after $\overline{WR}$ goes LOW. After BUSY goes low, 125 additional clock cycles are required before the next conversion cycle will begin.

Once conversion is started, $\overline{WR}$ is ignored for 1100 internal clock cycles. After 1100 clock cycles, another $\overline{WR}$ pulse is recognized and initiates a new conversion when the present conversion is complete. A negative edge on $\overline{WR}$ is required to begin conversion. If $\overline{WR}$ is held LOW, conversions will not occur continuously.

The A/D conversion data is valid on the falling edge of BUSY, and remains valid until one-half internal clock cycle before BUSY goes HIGH on the succeeding conversion. BUSY can be monitored with an I/O pin to determine end of conversion, or to generate a µP interrupt.

In demand mode, the three data bytes can be read in any desired order. The TC850 is simply regarded as three bytes of memory and accessed accordingly. The bus output timing is shown in Figure 10.

Continuous Mode Interface Timing

When the CONT/$\overline{DEMAND}$ input is HIGH, the TC850 performs conversions continuously. Data will be valid on the falling edge of BUSY, and all three bytes must be read within 443-1/2 internal clock cycles of BUSY going LOW. The timing diagram is shown in Figure 11.

In continuous mode, OVR/$\overline{POL}$ and L/$\overline{H}$ byte-select inputs are ignored. The TC850 automatically cycles through three data bytes, as shown in Table I. Bus output timing in the continuous mode is shown in Figure 12.

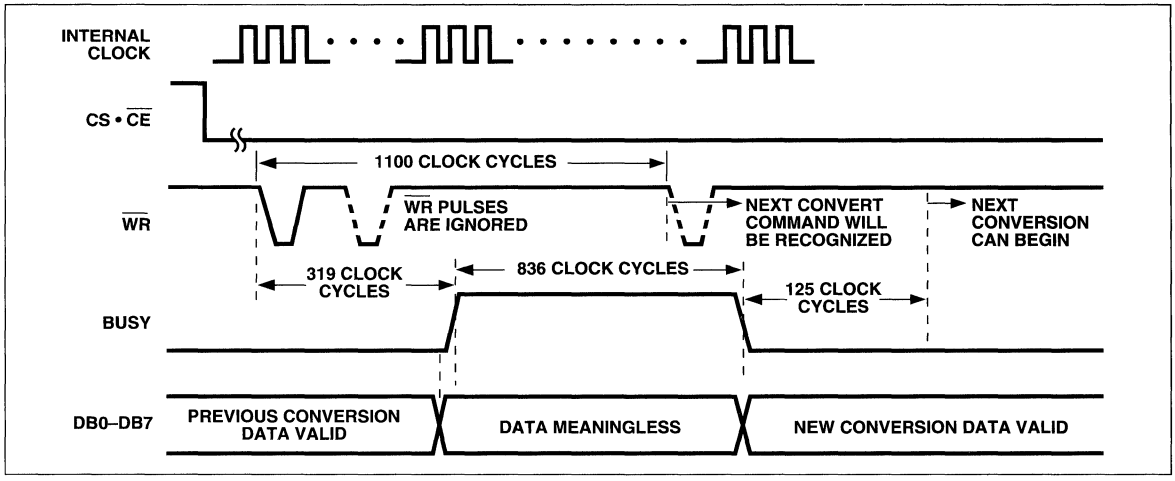
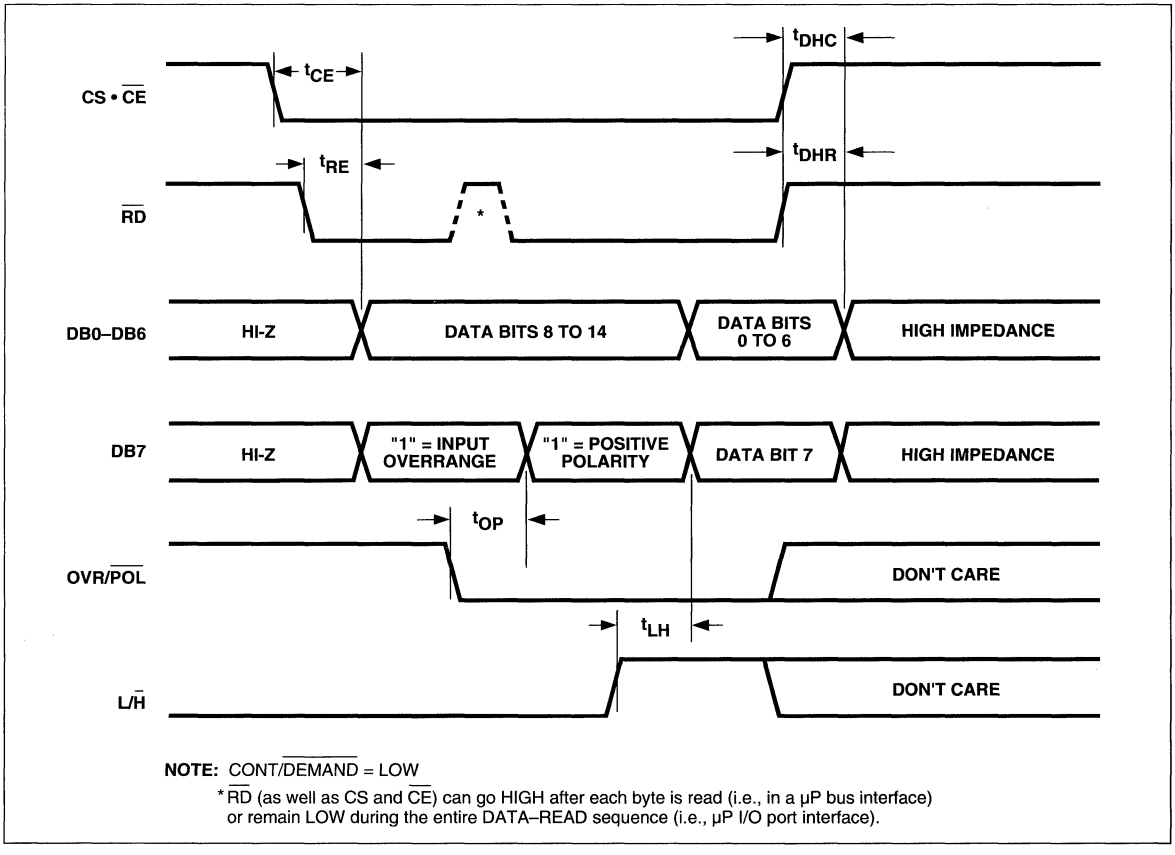


Figure 9 Conversion Timing, Demand Mode



NOTE: CONT/DEMAND = LOW

*RD (as well as CS and CE) can go HIGH after each byte is read (i.e., in a µP bus interface) or remain LOW during the entire DATA–READ sequence (i.e., µP I/O port interface).

Figure 10 Bus Output Timing, Demand Mode

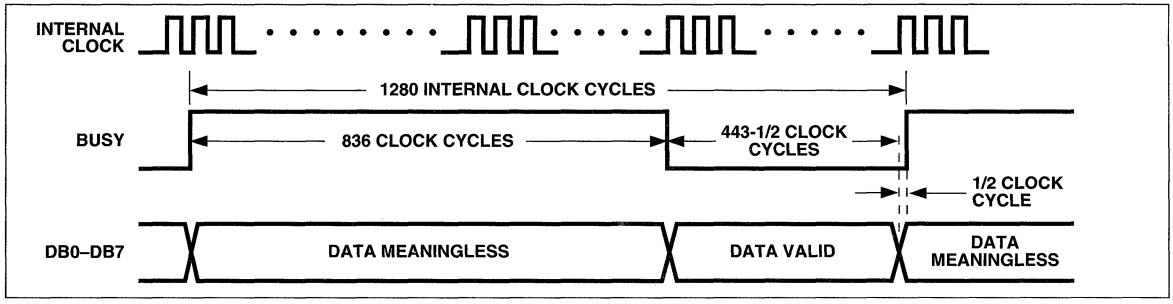


Figure 11 Conversion Timing, Continuous Mode

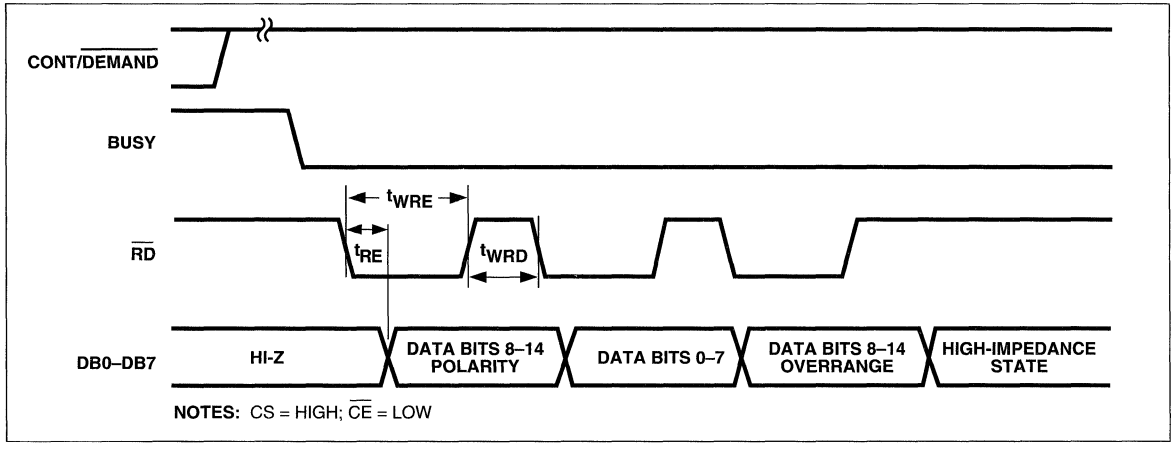


Figure 12 Bus Output Timing, Continuous Mode

12-BIT μP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **Zero-Integrator Cycle for Fast Recovery From Input Overloads**
- **Eliminates Cross -Talk in Multiplexed Systems**
- **12-Bit Plus Sign Integrating A/D Converter With Overrange Indication**
- **Sign Magnitude Coding Format**
- **True Differential Signal Input and Differential Reference Input**
- **Low Noise ..... 15 μV_{P-P} Typ**
- **Input Current ..... 1 pA Typ**
- **No Zero Adjustment Needed**
- **TTL-Compatible, Byte-Organized Tri-State Outputs**
- **UART Handshake Mode for Simple Serial Data Transmission**

ORDERING INFORMATION

PART CODE **TC7109X**

A or blank*

Package Code	Package	Temperature Range
CPL	40-Pin Plastic DIP	0°C to +70°C
CKW	44-Pin Quad Flat Pack	0°C to +70°C
CLW	44-Pin PLCC	0°C to +70°C
IJL	40-Pin CerDIP	–25°C to +85°C

* The "A" version has a higher Iout on the digital lines.

GENERAL DESCRIPTION

The TC7109A is a 12-bit plus sign, CMOS low-power analog-to-digital converter (ADC). Only eight passive components and a crystal are required to form a complete dual-slope integrating ADC.

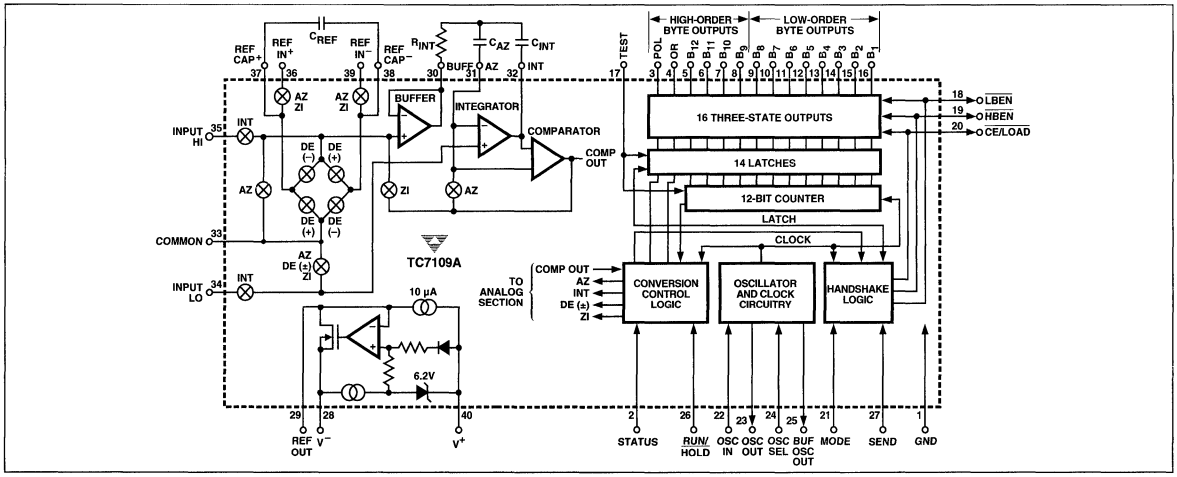
The improved V_{OH} source current TC7109A has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV_{P-P}, and auto-zero. True differential input and reference allow measurement of bridge-type transducers such as load cells, strain gauges, and temperature transducers.

The TC7109A provides a versatile digital interface. In the direct mode, chip select and HIGH/LOW byte enables control parallel bus interface. In the handshake mode, the TC7109A will operate with industry-standard UARTs in controlling serial data transmission — ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/HOLD input and STATUS output.

For applications requiring more resolution, see the TC500, 15-bit plus sign ADC data sheet.

The TC7109A has improved overrange recovery performance and higher output drive capability than the original TC7109. All new (or existing) designs should specify the TC7109A wherever possible.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply voltage (GND to V^-) ..... –9V
Analog Input Voltage (Low to High) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Low to High (Note 1) .. V^+ to V^-
Digital Input Voltage (Pins 2–27) (Note 2) ..... GND –0.3V
Power Dissipation (Note 3)
Ceramic Package ..... 1W at +85°C
Plastic Package ..... 500 mW at +70°C
Operating Temperature Range
Plastic Package (C) ..... 0°C to +70°C
Ceramic Package (I) ..... –25°C to +85°C
(M) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

NOTES:
1. Input voltages may exceed supply voltages if input current is limited to ±100 µA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latch-up. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TC7109A before its power supply is established. In multiple supply systems, the supply to the device should be activated first.
3. This limit refers to that of the package and will not occur during normal operation.

ELECTRICAL CHARACTERISTICS:

All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = +25°C$, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Overload Recovery Time (TC7109A)			0	1	Measurement Cycle
	Zero Input Reading	V_{IN} = 0V Full Scale = 409.6 mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
	Ratio Metric Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8 mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
NL	Nonlinearity (Max Deviation From Best Straight Line Fit)	Full Scale = 409.6 mV to 2.048V Over Full Operating Temperature Range	–1	±0.2	+1	Count
	Roll-Over Error (Difference in Reading for Equal Positive and Negative Inputs Near (Full Scale)	Full Scale = 409.6 mV to 2.048V Over Full Operating Temperature Range	–1	±0.02	+1	Count
CMRR	Input Common-Mode Rejection Ratio	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6 mV		50		µV/V
V_{CMR}	Common-Mode Voltage Range	Input High, Input Low, and Common Pins	V^-+1.5		V^+–1	V
e_N	Noise (P-P Value Not Exceeded 95% of Time)	V_{IN} = 0V Full Scale = 409.6 mV		15		µV
I_{IN}	Leakage Current at Input	V_{IN}, All Packages: +25°C C Device: 0°C ≤ T_A ≤ +70°C I Device: –25°C ≤ T_A ≤ +85°C M Device: –55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
TC_{ZS}	Zero Reading Drift	V_{IN} = 0V		0.2	1	µV/°C
TC_{FS}	Scale-Factor Temperature Coefficient	V_{IN} = 408.9 mV = $>7770_8$ Reading, Ext Ref = 0 ppm/°C		1	5	µV/°C
I^+	Supply Current (V^+ to GND)	V_{IN} = 0V, Crystal Oscillator 3.58 MHz Test Circuit		700	1500	µA
I_S	Supply Current (V^+ to V^-)	Pins 2–21, 25, 26, 27, 29 Open		700	1500	µA

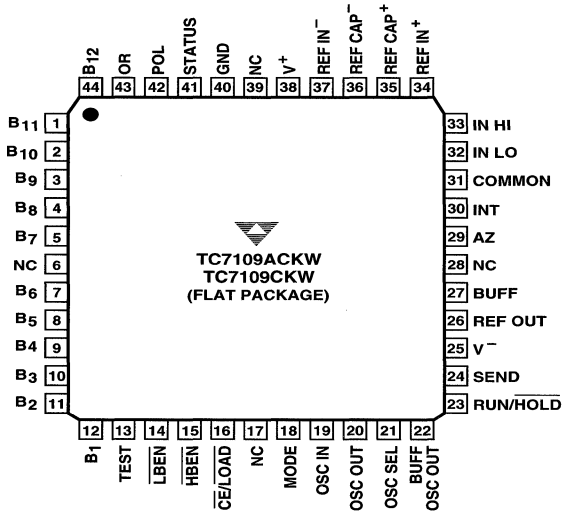
ELECTRICAL CHARACTERISTICS (Cont.)

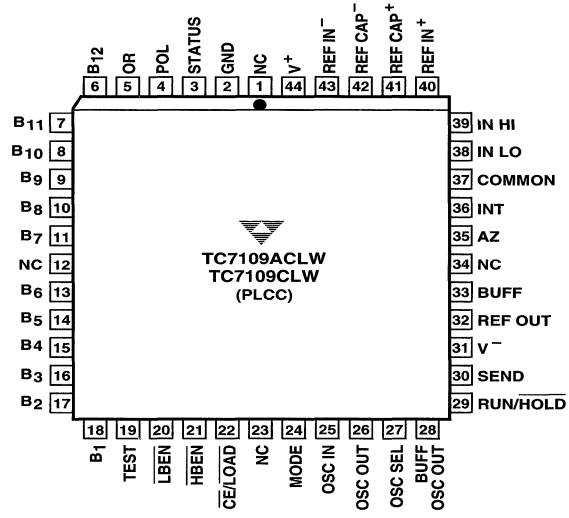
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{REF}	Ref Out Voltage	Referenced to V+, 25 kΩ Between V+ and Ref Out	–2.4	–2.8	–3.2	V
TC_{REF}	Ref Out Temperature Coefficient	25 kΩ Between V+ and Ref Out $0°C \leq T_A \leq +70°C$		80		ppm/°C
Digital						
V_{OH}	Output High Voltage	TC7109: I_{OUT} = 100 µA TC7109A: I_{OUT} = 700 µA Pins 3–16, 18, 19, 20	3.5	4.3		V
V_{OL}	Output Low Voltage	I_{OUT} = 1.6 mA		0.2	0.4	V
	Output Leakage Current	Pins 3–16 High Impedance		±0.01	±1	µA
	Control I/O Pull-Up Current	Pins 18, 19, 20 V_{OUT} = V+–3V Mode Input at GND		5		µA
	Control I/O Loading	$\overline{HBEN}$, Pin 19; $\overline{LBEN}$, Pin 18			50	pF
V_{IH}	Input High Voltage	Pins 18–21, 26, 27 Referenced to GND	2.5			V
V_{IL}	Input Low Voltage	Pins 18-21, 26, 27 Referenced to GND			1	V
	Input Pull-Up Current	Pins 26, 27; V_{OUT} = V+–3V Pins 17, 24; V_{OUT} = V+–3V		5 25		µA µA
	Input Pull-Down Current	Pin 21; V_{OUT} = GND = +3V		1		µA
	Oscillator Output Current, High	V_{OUT} = 2.5V		1		mA
	Oscillator Output Current, Low	V_{OUT} = 2.5V		1.5		mA
	Buffered Oscillator Output Current, High	V_{OUT} = 2.5V		2		mA
	Buffered Oscillator Output Current, Low	V_{OUT} = 2.5V		5		mA
t_W	Mode Input Pulse Width		60			ns

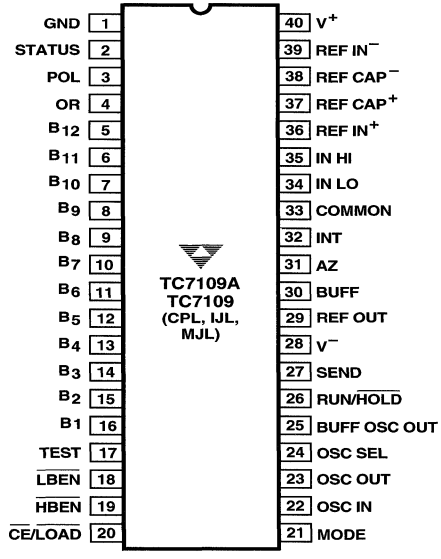
HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes, or other conducting material. Use proper anti-static handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

TC7109
TC7109A

PIN CONFLAGRATIONS







NC = NO INTERNAL CONNECTION

TC7109/A PIN DESCRIPTION

40-Pin DIP Pin Number	Symbol	Description	
1	GND	Digital ground, 0V, ground return for all digital logic.	
2	STATUS	Output HIGH during integrate and deintegrate until data is latched. Output LOW when analog section is in auto-zero or zero-integrator configuration.	
3	POL	Polarity — High for positive input.	All Three-State Data Bits
4	OR	Overrange — High if overranged.	
5	B_{12}	Bit 12 (Most Significant Bit)	
6	B_{11}	Bit 11	
7	B_{10}	Bit 10	
8	B_9	Bit 9	
9	B_8	Bit 8	
10	B_7	Bit 7	
11	B_6	Bit 6	
12	B_5	Bit 5	
13	B_4	Bit 4	
14	B_3	Bit 3	
15	B_2	Bit 2	
16	B_1	Bit 1 (Least Significant Bit)	
17	TEST	Input High — Normal operation. Input LOW — Forces all bit outputs HIGH. **Note:** This input is used for test purposes only.	
18	$\overline{\text{LBEN}}$	Low-Byte Enable — With MODE (Pin 21) LOW, and $\overline{\text{CE/LOAD}}$ (Pin 20) LOW, taking this pin LOW activates low-order byte outputs, B1–B8. With MODE (Pin 21) HIGH, this pin serves as low-byte flag output used in handshake mode. See Figures 7, 8, and 9.	
19	$\overline{\text{HBEN}}$	High-Byte Enable — With MODE (Pin 21) LOW, and $\overline{\text{CE/LOAD}}$ (Pin 20) LOW, taking this pin LOW activates high-order byte outputs, B9–B12, POL, OR. With MODE (Pin 21) HIGH, this pin serves as high-byte flag output used in handshake mode. See Figures 7, 8, and 9.	
20	$\overline{\text{CE/LOAD}}$	Chip Enable/Load — With MODE (Pin 21) LOW, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When HIGH, B1–B12, POL, OR outputs are disabled. When MODE (Pin 21) is HIGH, a load strobe is used in handshake mode. See Figure 7, 8, and 9.	
21	MODE	Input LOW — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed HIGH — Causes immediate entry into handshake mode and output of data as in Figure 9. Input HIGH — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.	
22	OSC IN	Oscillator Input	
23	OSC OUT	Oscillator Output	
24	OSC SEL	Oscillator Select — Input HIGH configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input LOW configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.	
25	BUF OSC OUT	Buffered Oscillator Output	
26	$\overline{\text{RUN/HOLD}}$	Input HIGH — Conversions continuously performed every 8192 clock pulses. Input LOW — Conversion in progress completed; converter will stop in auto-zero seven counts before integrate.	

TC7109/A PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number	Symbol	Description
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to V+ if not used.
28	V^-	Analog Negative Supply — Nominally –5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V^+ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}.
32	INTEGRATOR	Integrator Output — Outside foil of C_{INT}.
33	COMMON	Analog Common — System is auto-zeroed to COMMON.
34	INPUT LOW	Differential Input Low Side
35	INPUT HIGH	Differential Input High Side
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP –	Reference Capacitor Negative
39	REF IN –	Differential Reference Input Negative
40	V^+	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.

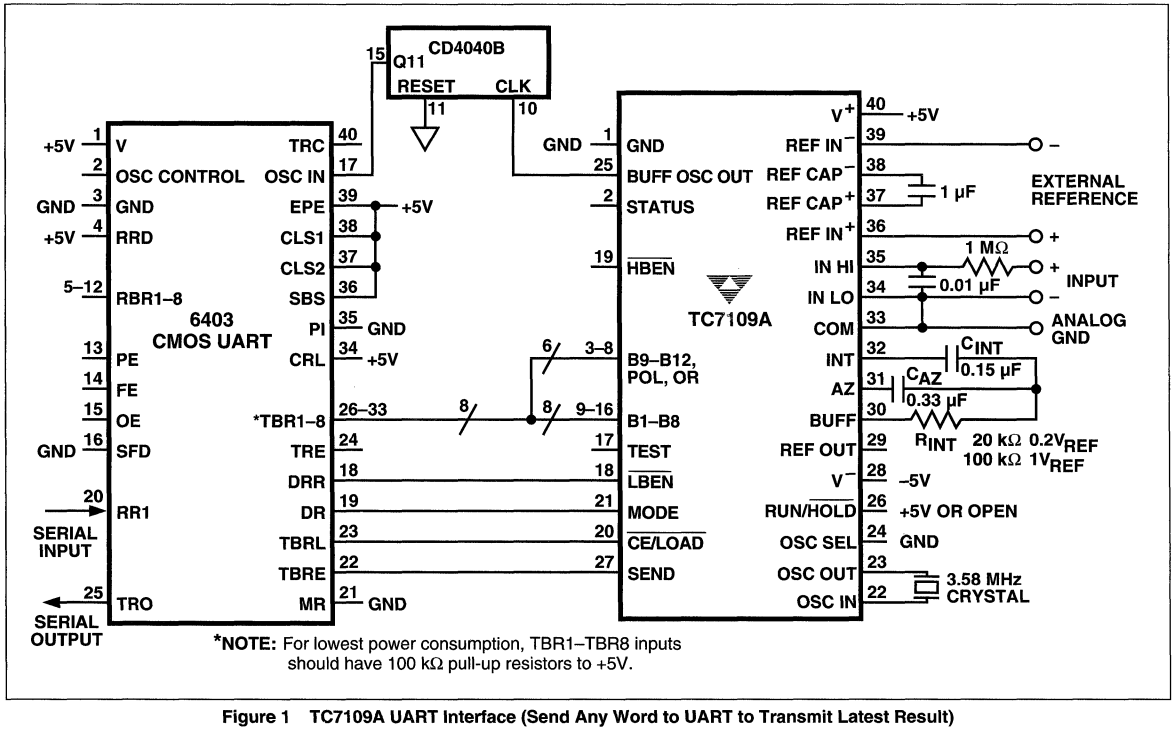


Figure 1 TC7109A UART Interface (Send Any Word to UART to Transmit Latest Result)

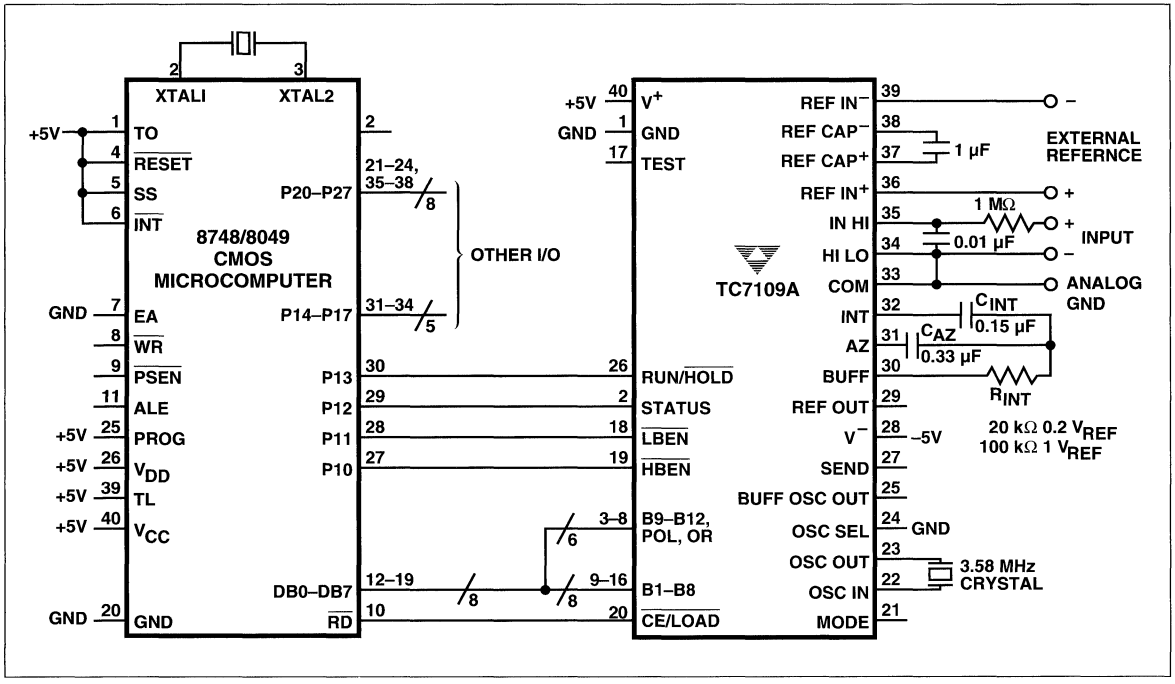


Figure 2 TC7109A Parallel Interface With 8048/8049 Microcomputer

DETAILED DESCRIPTION

(All Pin Designations Refer to 40-Pin DIP)

Analog Section

The functional diagram shows a block diagram of the analog section of the TC7109A. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/$\overline{HOLD}$ input is left open or connected to V^+. Each measurement cycle is divided into four phases, as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE), and (4) Zero Integrator (ZI).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal-Integrate Phase

The buffer and integrator inputs are removed from common and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter's power supply, input low can be tied to analog common to establish the correct common-mode voltage.

Deintegrate Phase

Input high is connected across the previously-charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by auto-zero) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Zero-Integrator Phase

The ZI phase only occurs when an input overrange condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an overrange measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

The ZI phase virtually eliminates hysteresis or "cross talk" in multiplexed systems. An overrange input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 3). The ZI phase only occurs following an overrange and lasts for a maximum of 1024 clock periods.

Differential Input

The TC7109A has been optimized for operation with analog common near digital ground. With +5V and –5V power supplies, a full ±4V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86 dB is achieved for input differential voltages anywhere within the typical common-mode range of 1V below the positive supply to 1.5V above the negative supply. However, for optimum performance, the IN HI and IN LO inputs should not come within 2V of either supply rail. Since the integrator also swings with the common-mode voltage, care must be exercised to ensure the integrator output does not saturate. A worst-case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Roll-over voltage is the main source of common-mode error, caused by the reference capacitor losing or gaining charge due to stray capacity on its nodes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal and lose charge (decrease voltage) when called upon to deintegrate a negative input signal. This difference in reference for (+) or (–) input voltages will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparison to the stray capacitance. To minimize roll-over error from these sources, keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in the block diagram (Figure 4) and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL compatible three-state output drivers, UART handshake logic, polarity, overrange, and control logic. Logic levels are referred to as LOW or HIGH.

Inputs driven from TTL gates should have 3 kΩ to 5 kΩ pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (LOW) to V^+ (HIGH).

STATUS Output

During a conversion cycle, the STATUS output goes HIGH at the beginning of signal integrate and goes LOW one-half clock period after new data from the conversion has been stored in the output latches (see Figure 3). The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while status is LOW.)

MODE Input

The output mode of the converter is controlled by the MODE input. The converter is in its "direct" output mode, when the MODE input is LOW or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a LOW Level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in 2 bytes, then returns to "direct" mode. When the MODE input is kept HIGH, the converter will output data in the handshake mode at the end of every conversion cycle. With MODE = 0 (direct bus transfer), the send input should be tied to V^+. (See "Handshake Mode.")

$\overline{\text{RUN/HOLD}}$ Input

With the $\overline{\text{RUN/HOLD}}$ input high, or open, the circuit operates normally as a dual-slope ADC, as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the deintegrate mode. An internal pull-up resistor is provided to ensure a HIGH level with an open input.

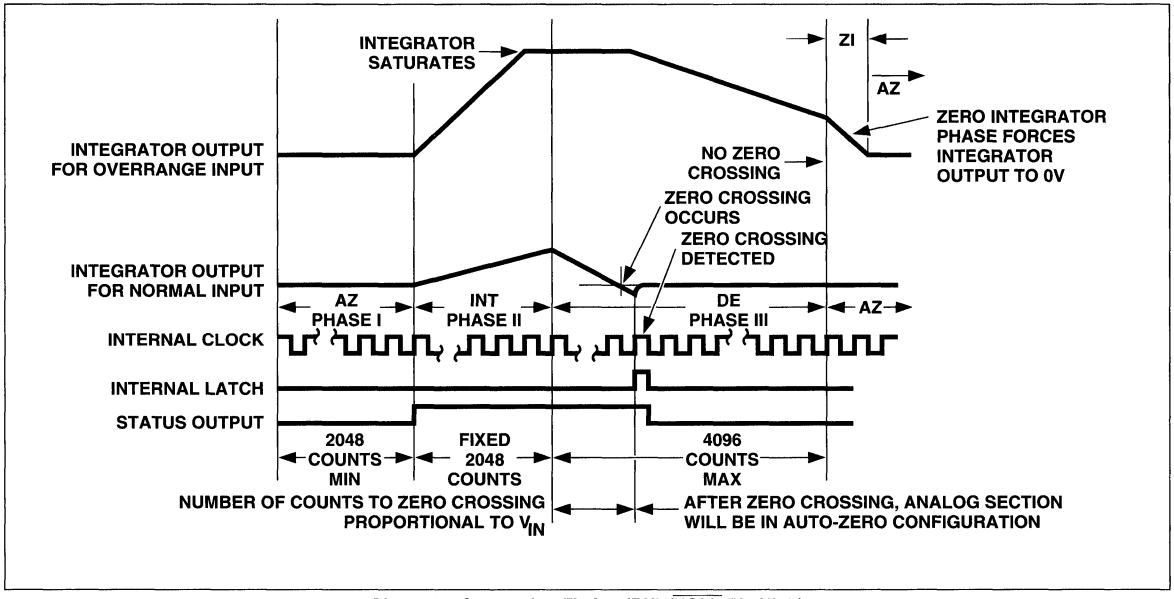


Figure 3 Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

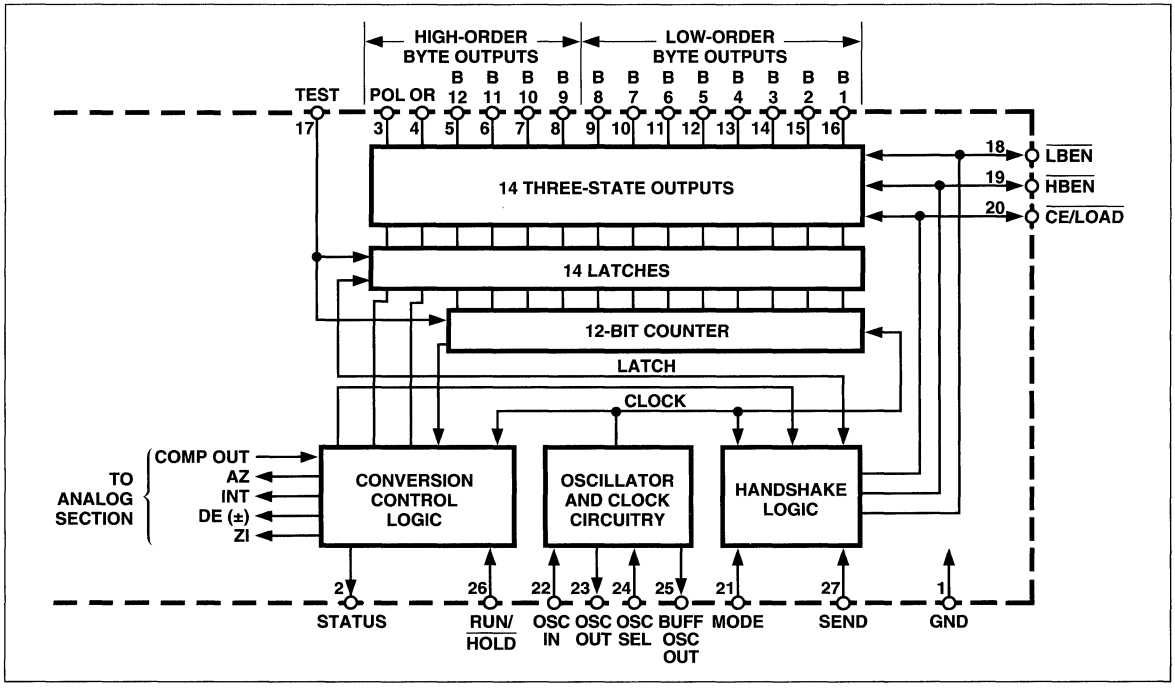


Figure 4 Digital Section

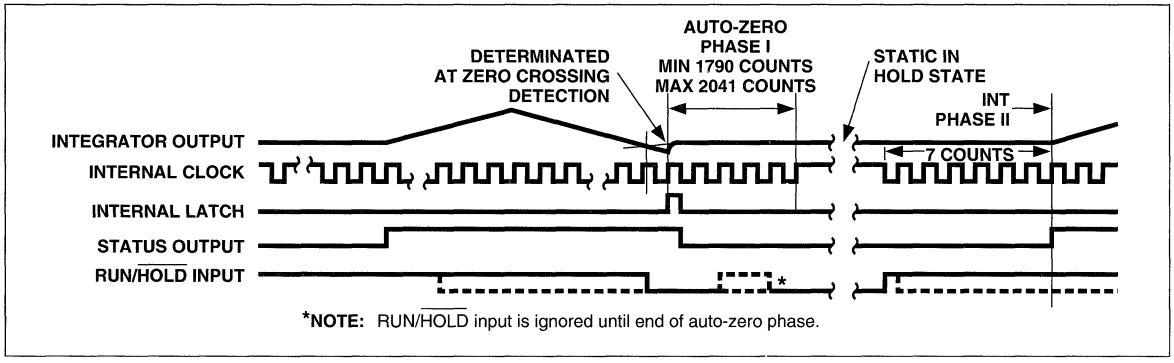


Figure 5 TC7109A RUN/HOLD Operation

The RUN/HOLD input may be used to shorten conversion time. If RUN/HOLD goes LOW any time after zero crossing in the deintegrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in deintegrate.

If RUN/HOLD stays or goes LOW, the conversion will complete with minimum time in deintegrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a HIGH at the RUN/HOLD input. As shown in Figure 5, the STATUS output will go HIGH 7 clock periods after RUN/HOLD is changed to HIGH, and the converter will begin the integrate phase of the next conversion.

The RUN/HOLD input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/HOLD LOW. The conversion is started when RUN/HOLD goes HIGH, and the new data is valid when the STATUS output goes LOW (or is transferred to the UART; see "Handshake Mode"). RUN/HOLD may now go LOW, terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/HOLD goes LOW during deintegrate, after zero crossing, and goes HIGH after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the buffered oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8, low-order bytes; bits 9 through 12, polarity and overrange high-order bytes) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a LOW level. These three inputs are all active LOW. Internal pull-up resistors are provided for an inactive HIGH level when left open. When chip enable is LOW, a byte-enable input LOW will allow the outputs of the byte to become active. A variety of parallel data accessing techniques may be used, as shown in the "Interfacing" section. (See Figure 6 and Table I.)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This prevents accessing data while it is being updated and eliminates the acquisition of erroneous data.

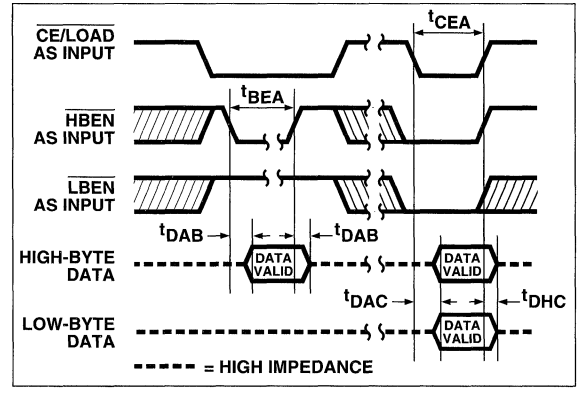


Figure 6 TC7109A Direct Mode Output Timing

Table I TC7109A Direct Mode Timing Requirements

Symbol	Description	Min	Typ	Max	Units
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time From Byte Enable		150	300	ns
t_{DHB}	Data Hold Time From Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time From Chip Enable		200	400	ns
t_{DHC}	Data Hold Time From Chip Enable		200	400	ns

Handshake Mode

An alternative means of interfacing the TC7109A to digital systems is provided when the handshake output mode of the TC7109A becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TC7109A and industry-standard UARTs with no external logic required. The TC7109A provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE input controls the handshake mode. When the MODE input is held HIGH, the TC7109A enters the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE input. At any time during the conversion cycle, the LOW-to-HIGH transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode, data updating will be inhibited (see Figure 9).

When the MODE input is HIGH or when the converter enters the handshake mode, the chip and byte enable inputs become TTL-compatible outputs which provide the output cycle control signals (see Figures 7, 8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held HIGH is shown in Figure 7. The handshake mode (internal MODE HIGH) is entered after the data latch pulse (the $\overline{\text{CE/LOAD}}$, $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs since MODE remains HIGH).

The HIGH level at the SEND input is sensed on the same HIGH-to-LOW internal clock edge. On the next LOW-to-HIGH internal clock edge, the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{\text{CE/LOAD}}$ and the $\overline{\text{HBEN}}$ outputs assume a LOW level. The $\overline{\text{CE/LOAD}}$ output remains LOW for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high-byte enable remains LOW for 2 clock periods. The $\overline{\text{CE/LOAD}}$ output LOW level or LOW-to-HIGH edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining HIGH the converter completes the output cycle using $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ while the low-order byte outputs (bits 1 through 8) are activated. When both bytes are sent, the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows an industry-standard HD6403 or CDP1854 CMOS UART to interface to serial data channels. The SEND input to the TC7109A is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{\text{CE/LOAD}}$ input of the TC7109A drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter buffer register inputs accept the parallel data outputs. With the UART transmitter buffer register empty, the SEND input will be HIGH when the handshake mode is entered after new data is stored. The high-order byte outputs become active and the $\overline{\text{CE/LOAD}}$ and $\overline{\text{HBEN}}$ inputs will go LOW after SEND is sensed. When $\overline{\text{CE/LOAD}}$ goes HIGH at the end of one clock period, the high-order byte data is clocked into the UART transmitter buffer register. The UART TBRE output will go LOW, which halts the output cycle with the $\overline{\text{HBEN}}$ output LOW, and the high-order byte outputs active. When the UART has transferred the data to the transmitter register and cleared the transmitter buffer register, the TBRE returns HIGH. The high-order byte outputs are disabled on the next TC7109A internal clock HIGH-to-LOW edge, and one-half internal clock later, the $\overline{\text{HBEN}}$ output returns HIGH. The $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ outputs go LOW at the same time as the low-order byte outputs become active. When the $\overline{\text{CE/LOAD}}$ returns HIGH at the end of one clock period, the low-order data is clocked into the UART transmitter buffer register, and TBRE again goes LOW. The next TC7109A internal clock HIGH-to-LOW edge will sense when TBRE returns to a HIGH, disabling the data inputs. One-half internal clock later, the handshake mode is cleared, and the $\overline{\text{CE/LOAD}}$, $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ terminals return HIGH and stay active, if MODE still remains HIGH.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a LOW-to-HIGH edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is LOW when the converter enters handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

Figure 9 also shows that the output sequence can take longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

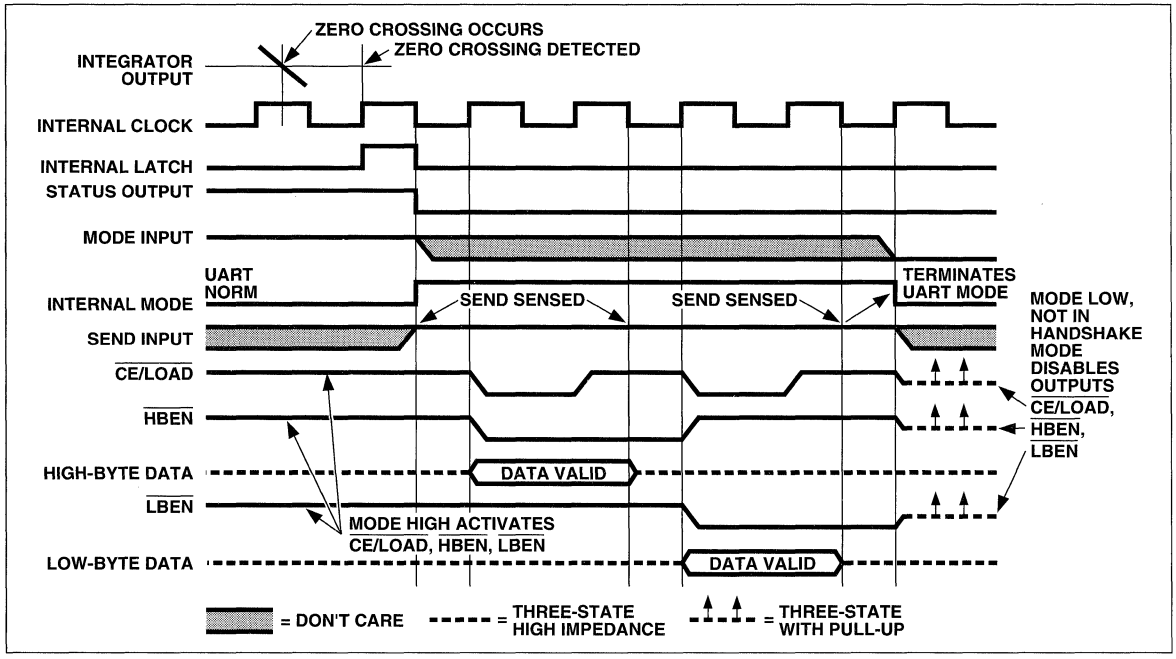


Figure 7 TC7109A Handshake With SEND INPUT Held Positive

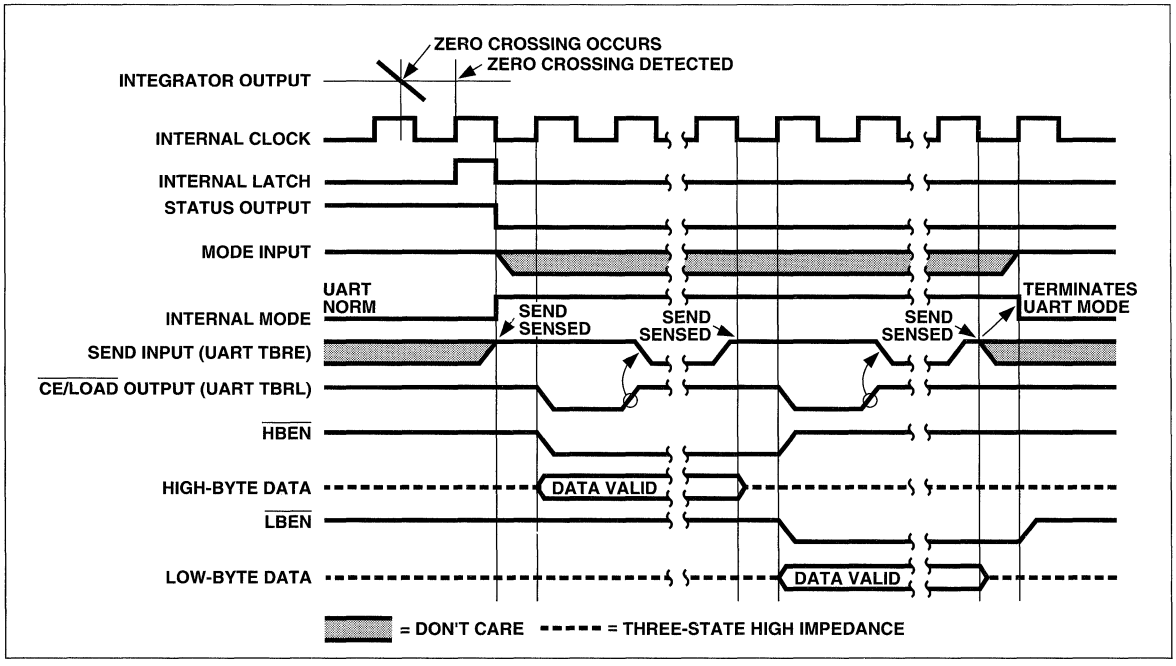


Figure 8 TC7109A Handshake — Typical UART Interface Timing

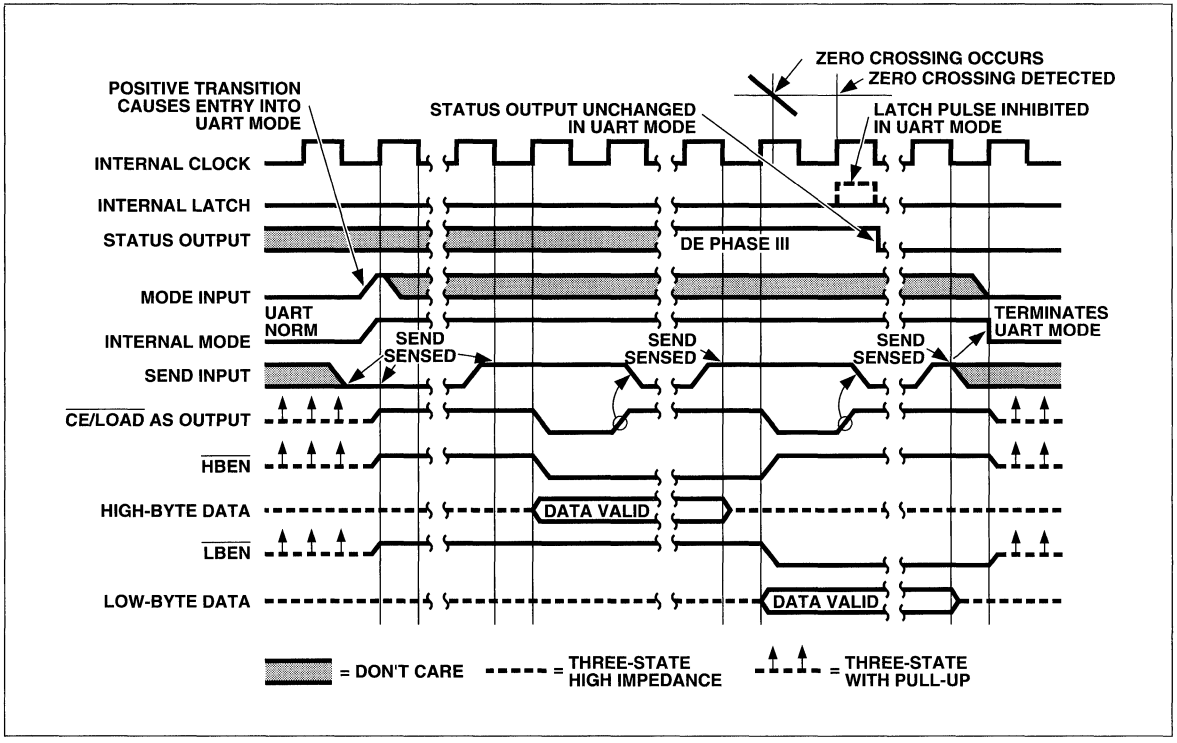


Figure 9 TC7109A Handshake Triggered by MODE Input

Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pull-up resistor. When the OSCILLATOR SELECT input is HIGH or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100 kΩ resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60 Hz period for optimum 60 Hz line rejection.

With OSCILLATOR SELECT input LOW, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range with no external components (Figure 11). The OSCILLATOR SELECT input LOW inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58 MHz TV crystal gives a division ratio providing an integration time given by:

$$t = (2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ ms}$$

The error is less than 1% from two 60 Hz periods, or 33.33 ms, which will give better than 40 dB, 60 Hz rejection. The converter will operate reliably at conversion rates up to 30 per second, corresponding to a clock frequency of 245.8 kHz.

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

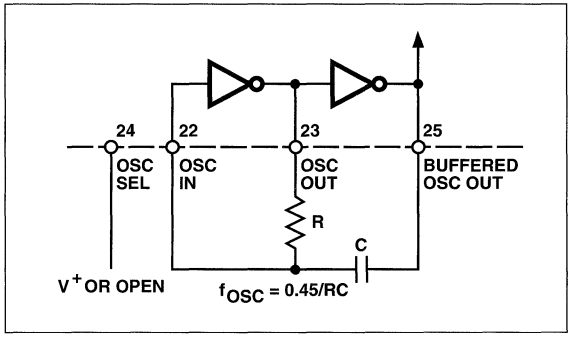


Figure 10 TC7109A RC Oscillator

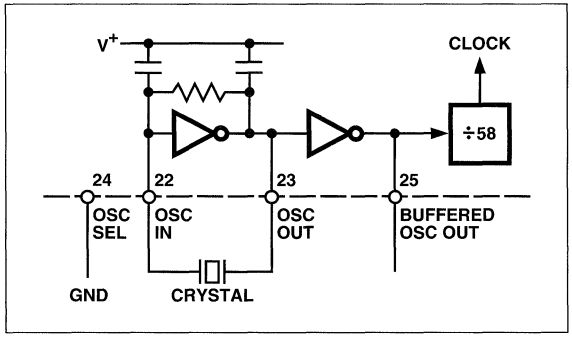


Figure 11 TC7109A Crystal Oscillator

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled and the counter outputs are all forced into the HIGH state. When the input returns to the 1/2 (V^+–GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the LOW state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V^+ and GND, allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly effecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common-mode voltage range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and roll-over errors will be slightly worse than in the ±4V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and roll-over errors. To improve performance, ±6V supplies may be used.

Integrating Capacitor

The integrating capacitor, C_{INT}, should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3V from either supply. A ±3.5V to ±4V integrator output swing is nominal for the TC7109A, with ±5V supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72 kHz internal clock frequency), nominal values C_{INT} and C_{AZ} are 0.15 µF and 0.33 µF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\ \mu A)}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors give undetectable errors, at reasonable cost, up to +85°C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

Integrating Resistor

The integrator and buffer amplifiers have a class A output stage with 100 µA of quiescent current. They supply 20 µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2.048V full-scale a 100 kΩ resistor is recommended and for 409.6 mV full-scale a 20 kΩ resistor is recommended. R_{INT} may be selected for other values of full scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\ \mu A}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large, the system noise is reduced. Since the TC7109A incorporates a zero integrator cycle, the size of the auto-zero capacitor does not affect overload recovery. The optimal value of the auto-zero capacitor is between 2 and 4 times C_{INT}. A typical value for C_{AZ} is 0.33 µF.

The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of stray pickups. For low leakage at temperatures above +85°C, use Teflon capacitors.

Reference Capacitor

A 1 µF capacitor is recommended for most circuits. However, where a large common-mode voltage exists, a larger value is required to prevent roll-over error (e.g., the reference low is not analog common), and a 409.6 mV scale is used. The roll-over error will be held to 0.5 count with a 10 µF capacitor. For temperatures above +80°C use Teflon or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts, the analog input required is $V_{IN} = 2\ V_{REF}$. For 409.6 mV full scale, use a reference of 204.8 mV. In many applications, where the ADC is connected to a transducer, a scale factor will exist between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage for the transducer is 700 mV. Instead of dividing the input down to 409.6 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 34 kΩ and 0.15 µF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TC7109A, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

Reference Sources

A major factor in the absolute accuracy of the ADC is the stability of the reference voltage. The 12-bit resolution of the TC7109A is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 70 ppm/°C, a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled, or where high-accuracy absolute measurements are being made, it is recommended that an external high-quality reference be used.

A reference output (pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage (20 mA may be sunk without significant variation in output voltage). A pull-up bias device is provided which sources about 10 µA. The output voltage is nominally 2.8V below V^+. When using the on-board reference, REF OUT (pin 29) should be connected to REF^- (pin 39), and REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The test circuit shows the circuit for a 204.8 mV reference, generated by a 2 kΩ precision potentiometer in series with a 24 kΩ fixed resistor.

Interfacing

Direct Mode

Combinations of chip-enable and byte-enable control signals which may be used when interfacing the TC7109A to parallel data lines are shown in Figure 12. The $\overline{CE}/\overline{LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE}/\overline{LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The $\overline{CE}/\overline{LOAD}$ is a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be used as a second chip enable, or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 shows interfacing several TC7109A's to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE}/\overline{LOAD}$ input to select the desired converter.

Figures 14–19 give practical circuits utilizing the parallel three-state output capabilities of the TC7109A. Figure 14 shows parallel interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TC7109A data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high-to-low transition of the STATUS driving an interrupt to the microprocessor.

The $\overline{RUN}/HOLD$ input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS Technology MCS650X system.

An interrupt is generated through the Control Register B, CB1 line from the high-to-low transition of the STATUS output. The $\overline{RUN}/HOLD$ pin is controlled by CB2 through Control Register B, allowing software control of conversions.

Direct interfacing to most microprocessor busses is easily accomplished through the three-state output of the TC7109A.

Figures 1, 17 and 18 are typical connection diagrams. To ensure requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low, providing simple address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

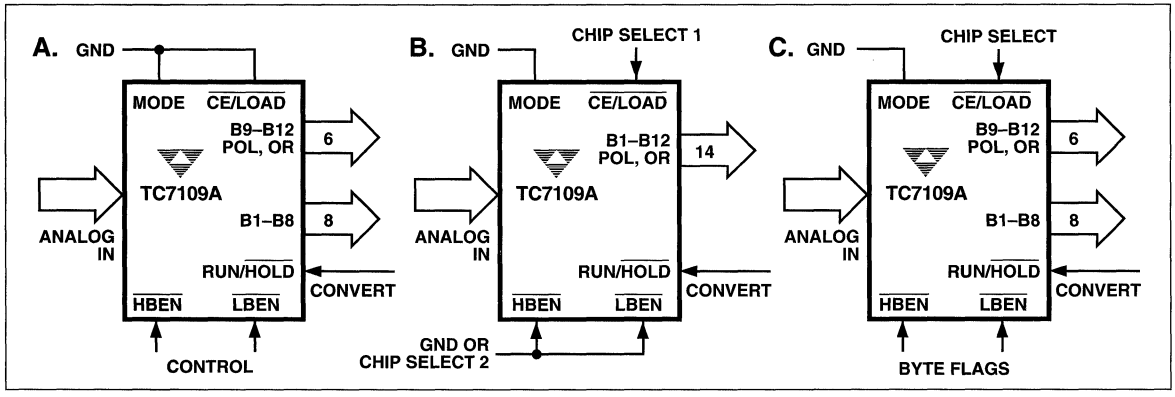


Figure 12 Direct Mode Chip and Byte Enable Combinations

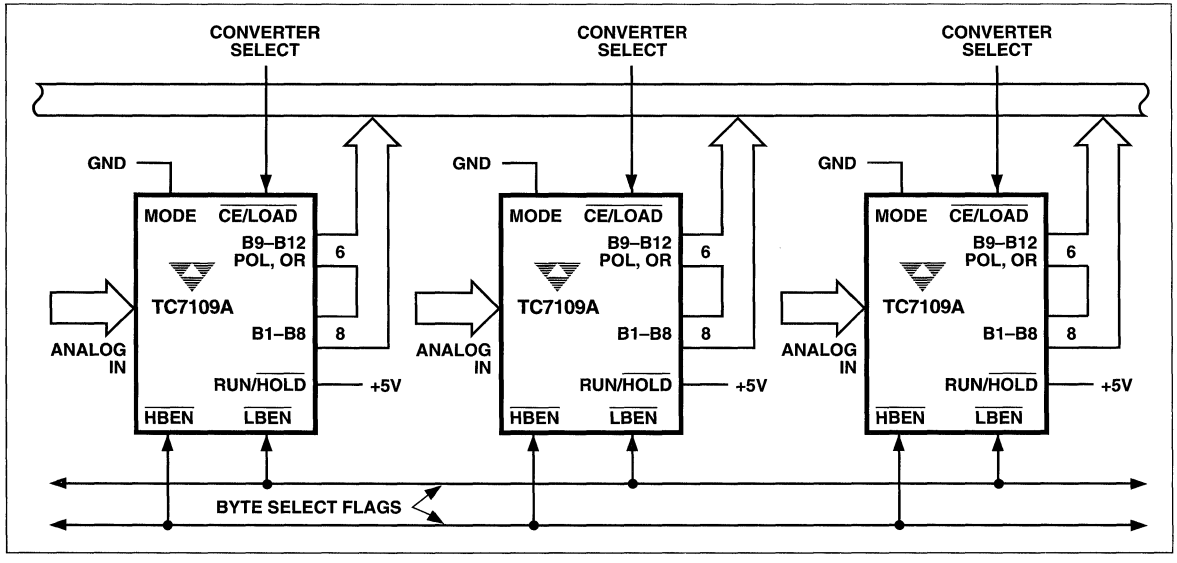


Figure 13 Three-Stating Several TC7109A's to a Small Bus

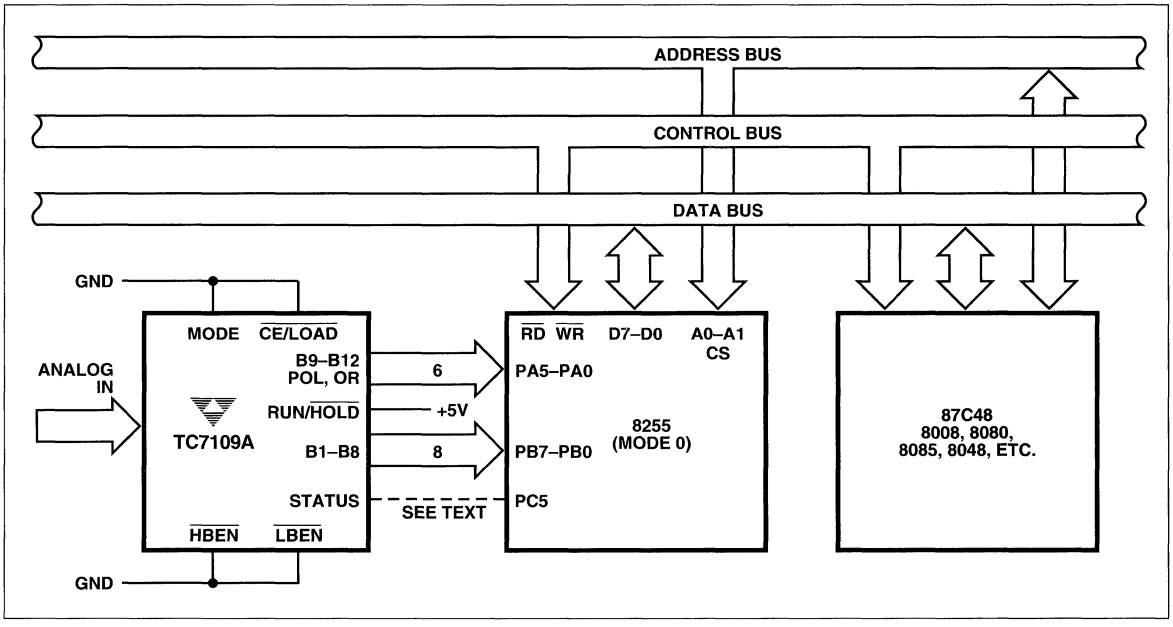


Figure 14 Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers

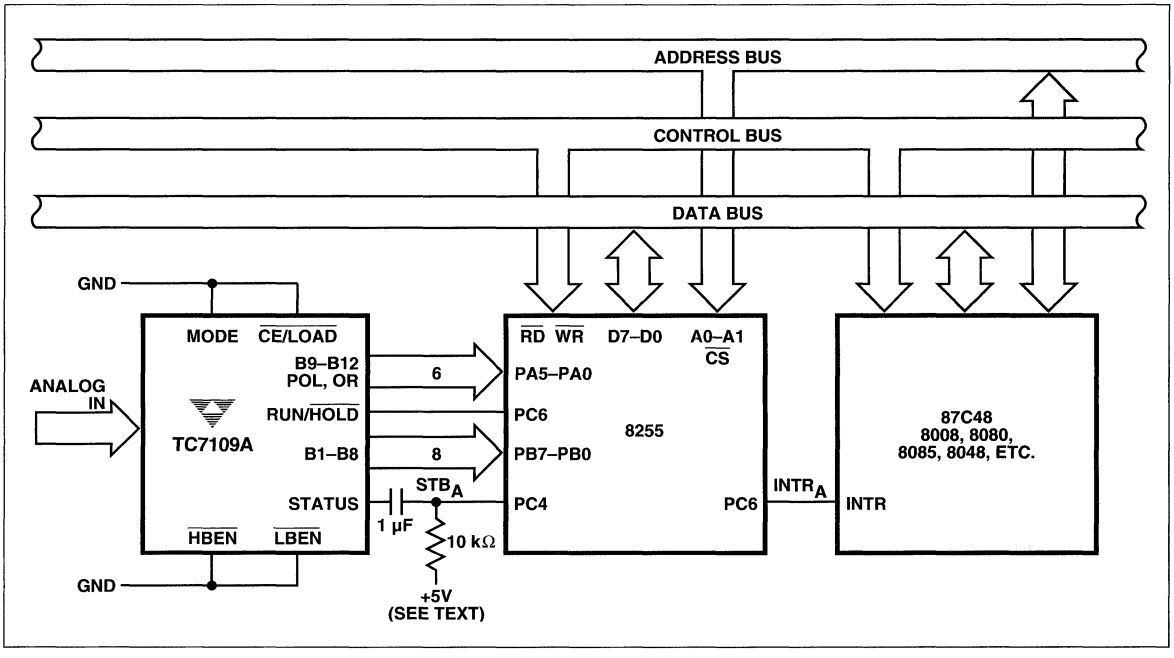


Figure 15 Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers With Interrupt

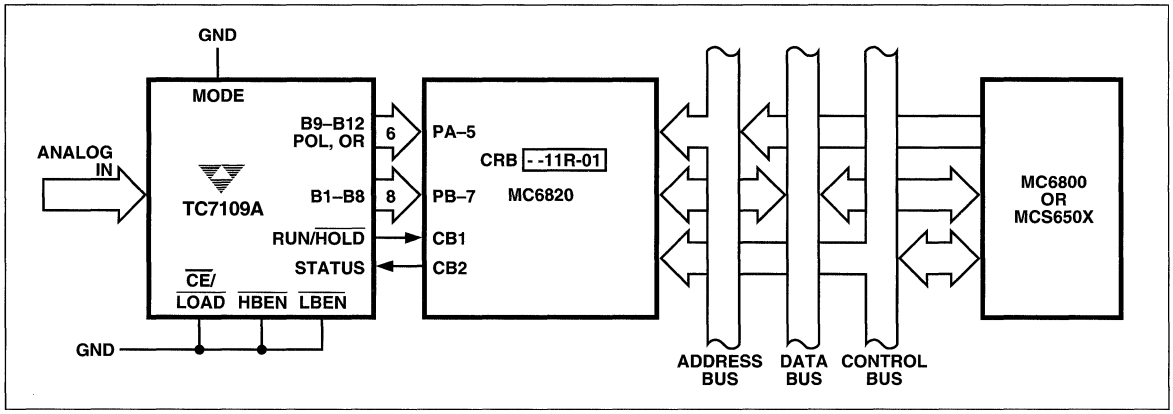


Figure 16 Full-Time Parallel Interface to MC6800 or MCS650X Microprocessor

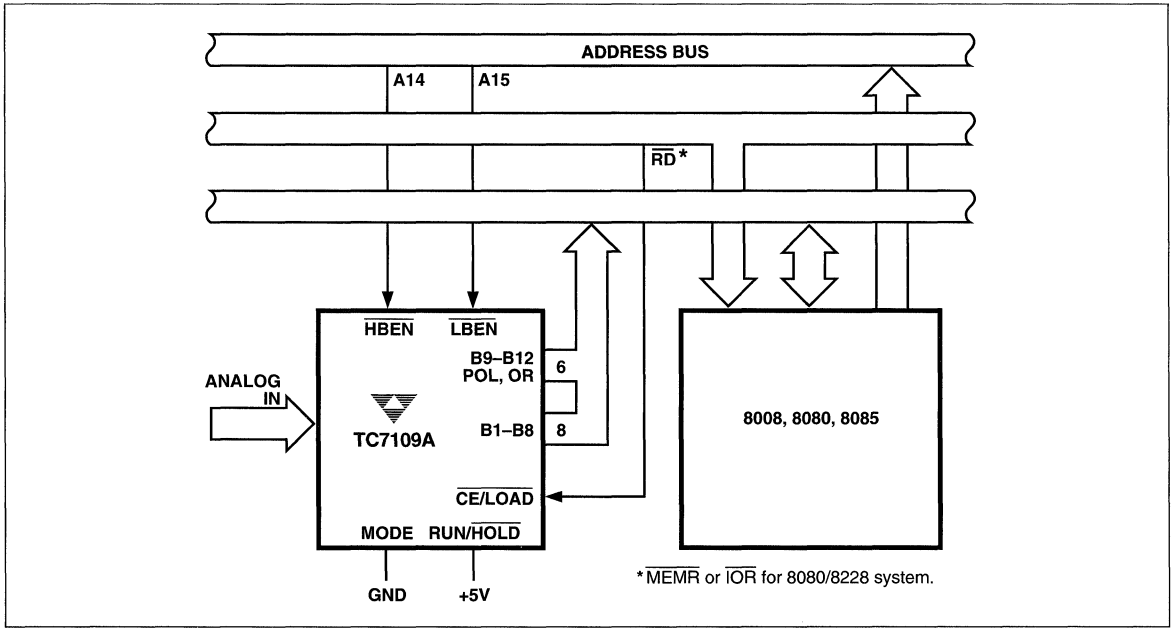


Figure 17 TC7109A Direct Interface to 8080/8085

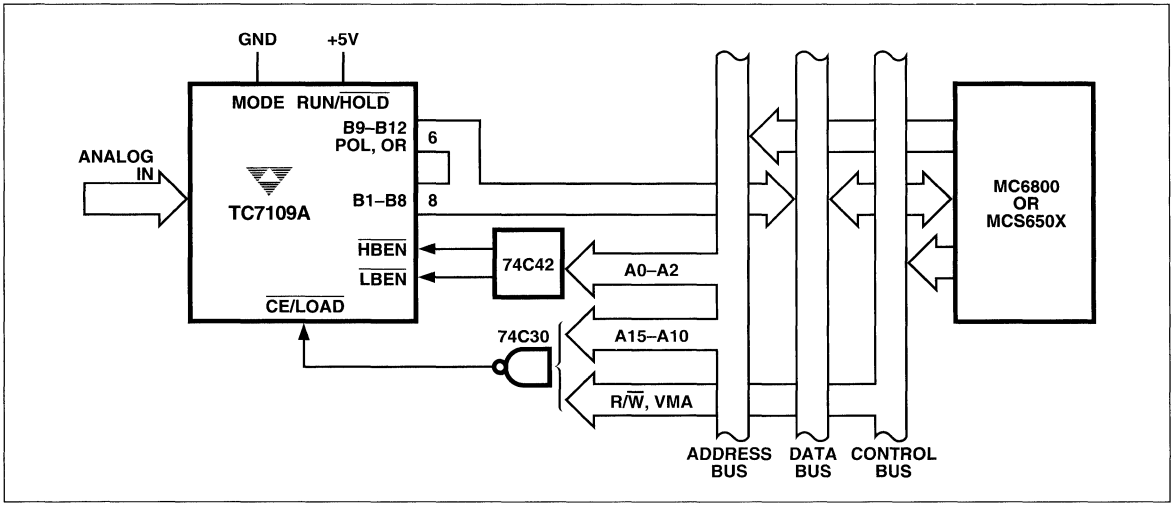


Figure 18 TC7109A Direct Interface to MC6800 Bus

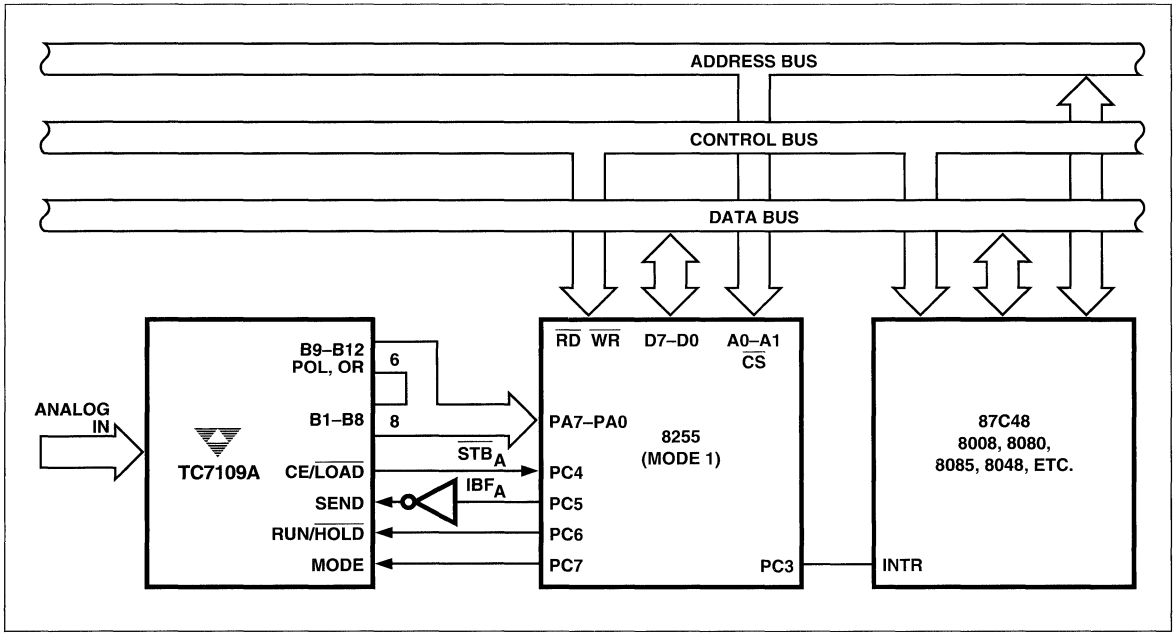


Figure 19 TC7109A Handshake Interface to MCS-48, -80, -85 Microcomputers

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of $\overline{CE}/\overline{LOAD}$. A handshake interface to Intel microprocessors using an 8255 PPI is shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TC7109A, and using the $\overline{CE}/\overline{LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is LOW and the TC7109A is in handshake mode, the next word will be strobed into the port. The strobe will cause IBF to go HIGH (SEND goes LOW), which will keep the enabled byte outputs active. The PPI will generate an interrupt which, when executed, will result in the data being read. The IBF will be reset LOW when the byte is read, causing the TC7109A to sequence into the next byte. The MODE input to the TC7109A is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left HIGH, or tied HIGH separately. (The data access must take less time than a conversion.) The output sequence can be obtained on demand if this output is made to go from LOW to HIGH and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/$\overline{HOLD}$ input to the TC7109A by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/$\overline{HOLD}$ tied HIGH to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry-standard UARTs (such as Western Digital TR1602), providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go HIGH. The MODE input to the TC7109A goes HIGH, triggering the TC7109A into handshake mode. The high-order byte is output to the UART and when the UART has transferred the data to the Transmitter register, TBRE (SEND) goes HIGH again, $\overline{LBEN}$ will go HIGH, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TC7109A to the UART.

An extension of the typical connection to several TC7109A's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is HIGH) is used to select which converter will handshake with the UART. Up to eight TC7109A's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

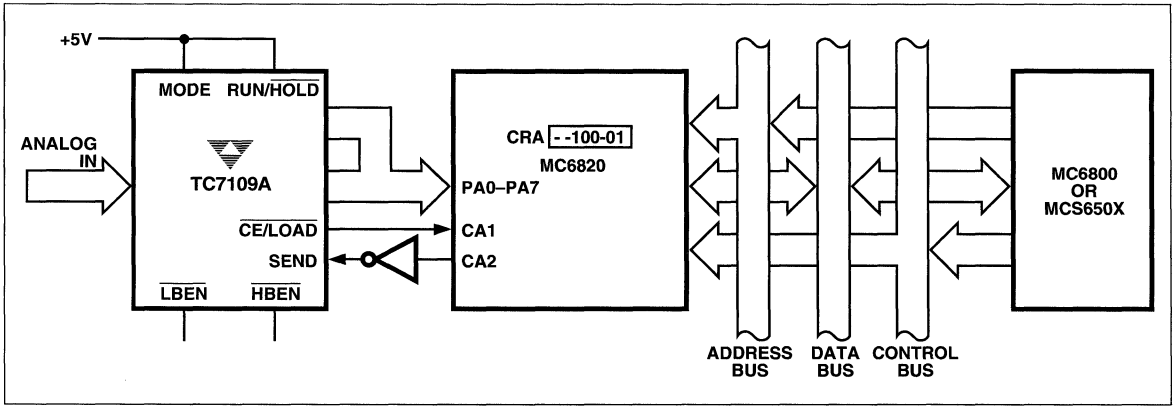


Figure 20 TC7109A Handshake Interface to MCS-6800, MCS650X Microprocessors

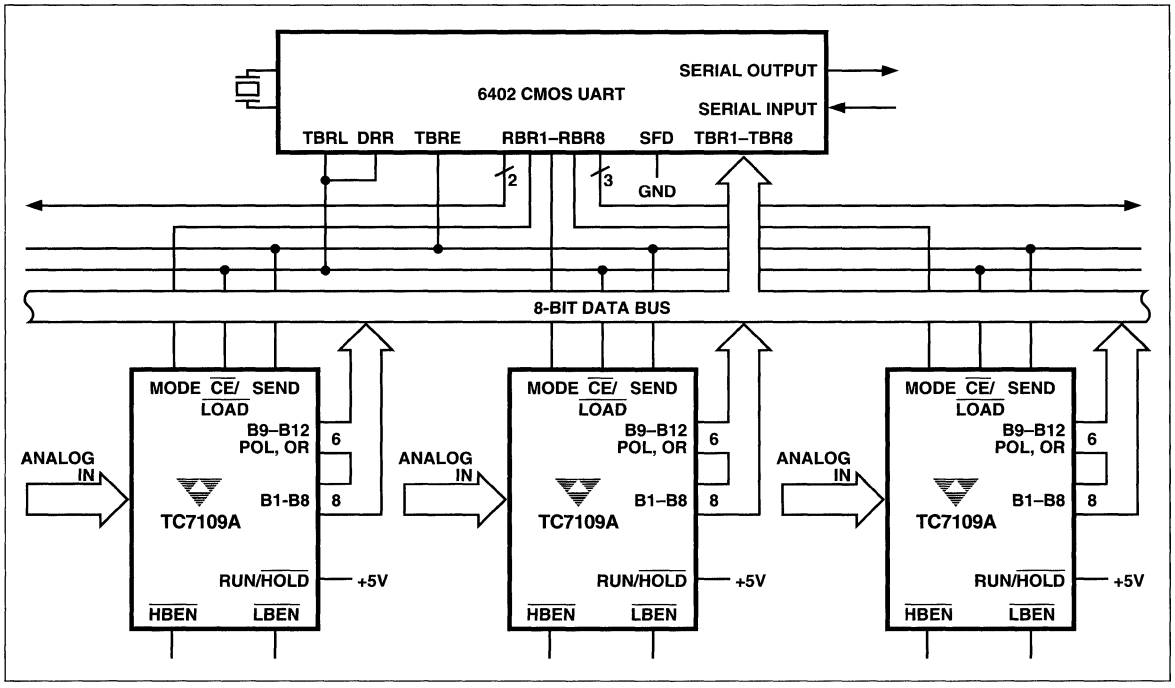


Figure 21 Handshake Interface for Multiplexed Converters

Integrating Converter Features

The output of integrating ADCs represents the integral, or average, of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter averages the effects of noise. A second important characteristic is that time is used to quantize the answer, resulting in extremely small nonlinearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise (Figure 22).

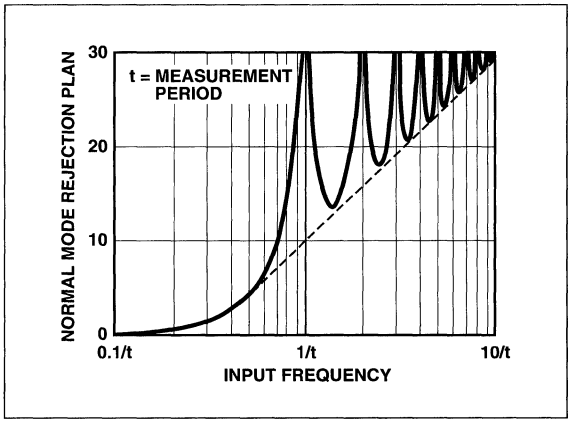


Figure 22 Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency

4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Low Roll-Over Error ..... ±1 Count Max**
- **Guaranteed Nonlinearity Error..... ±1 Count Max**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity Indication at Zero for Null Detection**
- **Multiplexed BCD Data Output**
- **TTL-Compatible Outputs**
- **Differential Input**
- **Control Signals Permit Interface to UARTs and μProcessors**
- **Auto-Ranging Supported With Overrange and Underrange Signals**
- **Blinking Display Visually Indicates Overrange Condition**
- **Low Input Current ..... 1 pA**
- **Low Zero Reading Drift ..... 2 μV/°C**
- **Interfaces to TC7211A (LCD) and TC7212A (LED) Display Drivers**
- **Available in DIP and Surface-Mount Packages**

GENERAL DESCRIPTION

The TC7135 4-1/2 digit analog-to-digital converter (ADC) offers 50 ppm (1 part in 20,000) resolution with a maximum nonlinearity error of 1 count. An auto-zero cycle reduces zero error to below 10 μV and zero drift to 0.5 μV/°C. Source impedance errors are minimized by a 10 pA maximum input current. Roll-over error is limited to ±1 count.

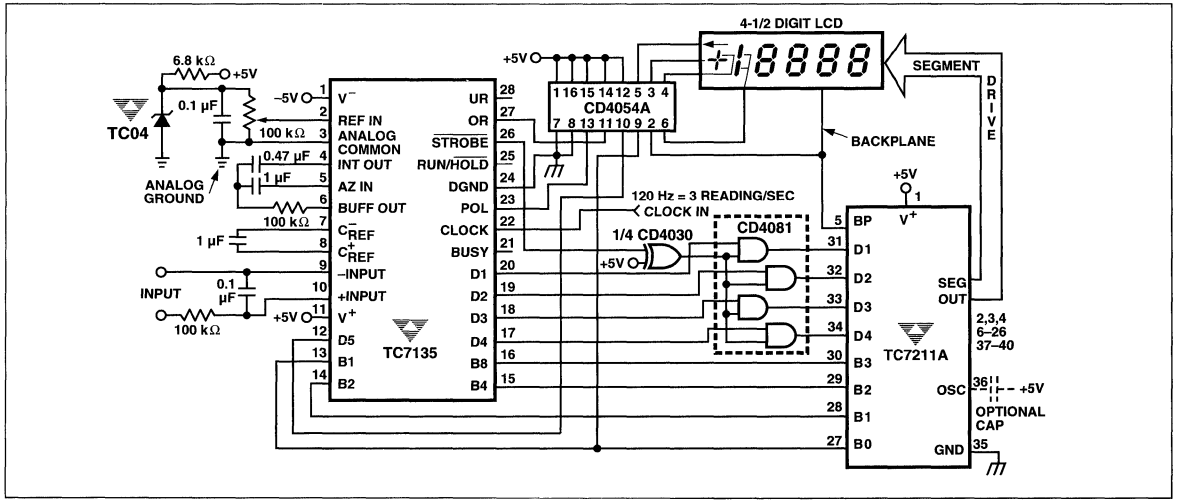
By combining the TC7135 with a TC7211A (LCD) or TC7212A (LED) driver, a 4-1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Microprocessor-based measurement systems are supported by BUSY, STROBE, and RUN/HOLD control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TC7135 the ideal converter for display or microprocessor-based measurement systems.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7135CPI	28-Pin Plastic DIP	0°C to +70°C
TC7135CBU	64-Pin Plastic Quad Flat Package	0°C to +70°C
TC7135CLI	28-Pin PLCC	0°C to +70°C

TYPICAL 4-1/2 DIGIT DVM WITH LCD



TC7135

ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... –9V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0V to V^+
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Power Dissipation
CerDIP (J) 1W
Plastic (P) 0.8W

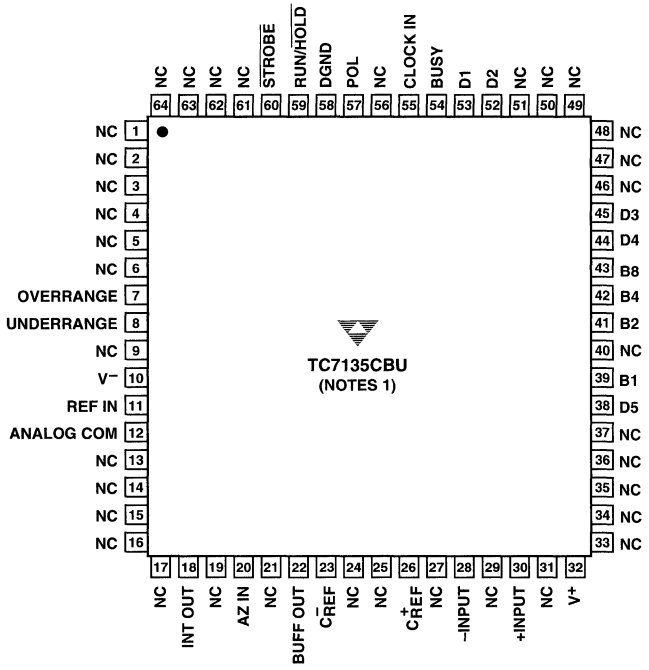
Static-sensitive device. Unused devices must be stored in conductive material to protect them from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

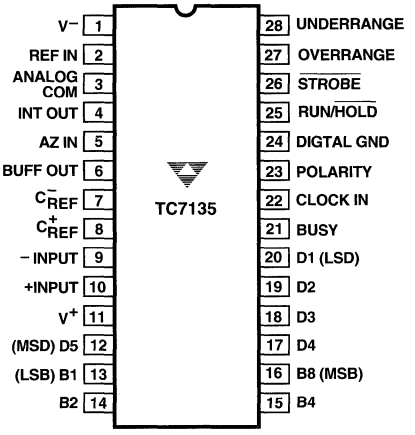
ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLOCK} = 120 kHz, V^+ = +5V, V^- = –5V (Figure 1)

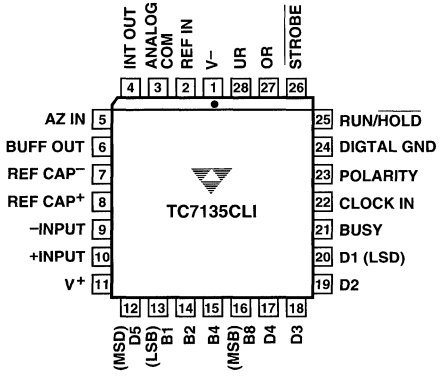
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Display Reading With Zero Volt Input	Notes 2 and 3	–0.0000	±0.0000	+0.0000	Display Reading
TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0V Note 4	—	0.5	2	µV/°C
TC_{FS}	Full-Scale Temperature Coefficient	V_{IN} = 2V Notes 4 and 5	—	—	5	ppm/°C
NL	Nonlinearity Error	Note 6	—	0.5	1	Count
DNL	Differential Linearity Error	Note 6	—	0.01	—	LSB
	Display Reading in Ratiometric Operation	$V_{IN} = V_{REF}$ Note 2	+0.9997	+0.9999	+1.0000	Display Reading
±FSE	± Full-Scale Symmetry Error (Roll-Over Error)	$-V_{IN} = +V_{IN}$ Note 7	—	0.5	1	Count
I_{IN}	Input Leakage Current	Note 3	—	1	10	pA
V_N	Noise	Peak-to-Peak Value Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
I_{IL}	Input Low Current	V_{IN} = 0V	—	10	100	µA
I_{IH}	Input High Current	V_{IN} = +5V	—	0.08	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.2	0.4	V
V_{OH}	Output High Voltage B_1, B_2, B_4, B_8, D_1–D_5 Busy, Polarity, Overrange, Underrange, Strobe	 I_{OH} = 1 mA I_{OH} = 10 µA	 2.4 4.9	 4.4 4.99	 5 5	 V V
f_{CLK}	Clock Frequency	Note 8	0	120	1200	kHz
Power Supply						
V^+	Positive Supply Voltage		4	5	6	V
V^-	Negative Supply Voltage		–3	–5	–8	V
I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1	3	mA
I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3	mA
PD	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

NOTES:
1. Limit input current to under 100 µA if input voltages exceed supply voltage.
2. Full-scale voltage = 2V.
3. V_{IN} = 0V.
4. 0°C ≤ T_A ≤ +70°C.
5. External reference temperature coefficient less than 0.01 ppm/°C.
6. –2V ≤ V_{IN} ≤ +2V. Error of reading from best fit straight line.
7. $|V_{IN}|$ = 1.9959.
8. Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

PIN CONFIGURATIONS







NOTES: 1. NC = No internal connection.

TC7135

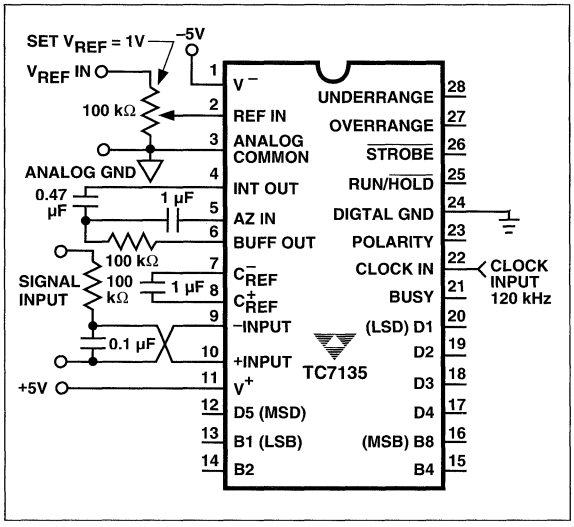


Figure 1. Test Circuit

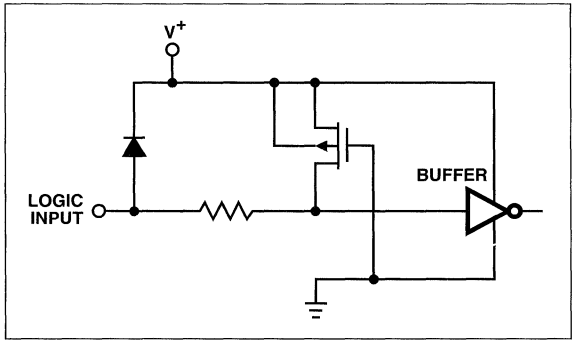


Figure 2. Digital Logic Input

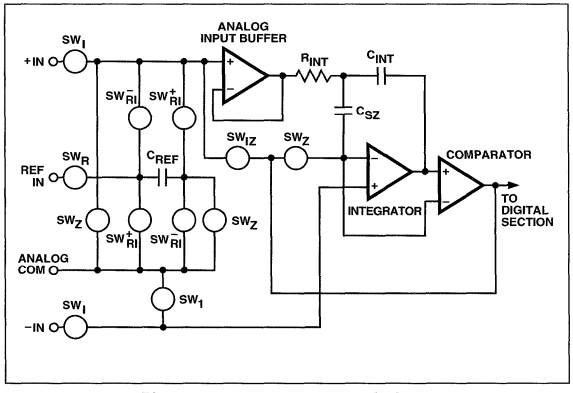


Figure 3A. Internal Analog Switches

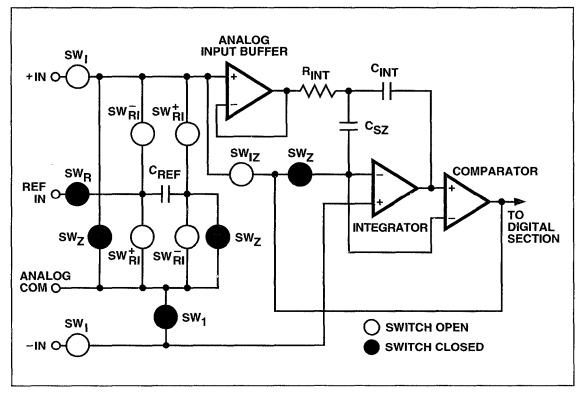


Figure 3B. System Zero Phase

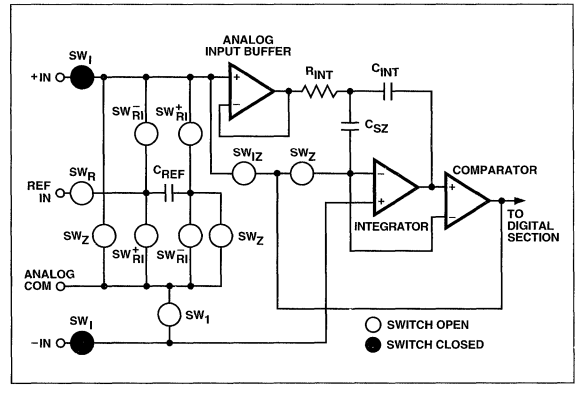


Figure 3C. Input Signal Integration Phase

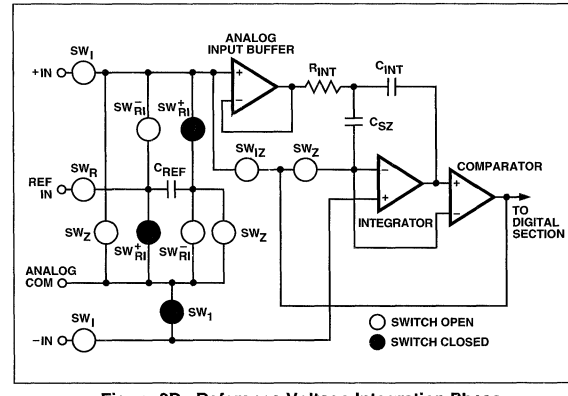


Figure 3D. Reference Voltage Integration Phase

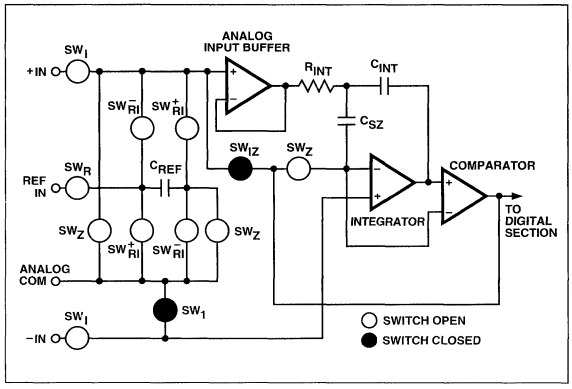


Figure 3E. Integrator Output Zero Phase

GENERAL THEORY OF OPERATION

(All Pin Designations Refer to 28-Pin DIP)

Dual-Slope Conversion Principles

The TC7135 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7135 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right]$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. (See Figure 4.)

TC7135 Operational Theory

The TC7135 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter overrange recovery time result.

The TC7135 measurement cycle contains four phases:

(1) System zero

(2) Analog input signal integration

(3) Reference voltage integration

(4) Integrator output zero

Internal analog gate status for each phase is shown in Table I.

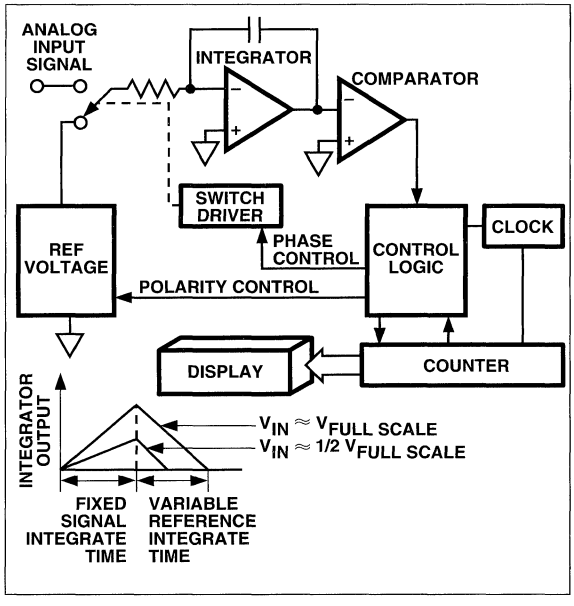


Figure 4. Basic Dual-Slope Converter

Table I. Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status							Reference Schematic
	SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}	
System Zero				Closed	Closed	Closed		3B
Input Signal Integration	Closed							3C
Reference Voltage Integration		Closed*				Closed		3D
Integrator Output Zero						Closed	Closed	3E

***NOTE:** Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

System Zero Phase

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With zero input voltage, the integrator output remains at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages. (See Figure 3B.)

Analog Input Signal Integration Phase

The TC7135 integrates the differential voltage between the +INPUT and –INPUT. The differential voltage must be within the device's common-mode range; –1V from either supply rail, typically.

The input signal polarity is determined at the end of this phase. (See Figure 3C)

Reference Voltage Integration Phase

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. (See Figure 3D.) The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}}\right].$$

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles. (See Figure 3E.)

Analog Section Functional Description

Differential Inputs

The TC7135 operates with differential voltages (+INPUT, pin 10 and –INPUT, pin 9) within the input amplifier common-mode range which extends from 1V below the positive supply to 1V above the negative supply. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage and must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4V full-scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

ANALOG COMMON (pin 3) is used as the –INPUT return during the auto-zero and deintegrate phases. If –INPUT is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, –INPUT will be set at a fixed known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

Reference Voltage

The reference voltage input (REF IN, pin 2) must be a positive voltage with respect to analog common. Two reference voltage circuits are shown in Figure 5.

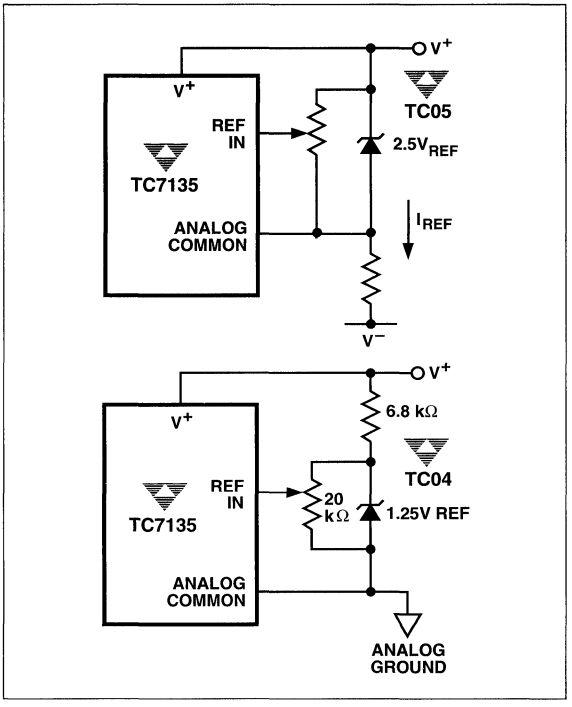


Figure 5. Using an External Reference Voltage

Digital Section Functional Description

The major digital subsystems within the TC7135 are illustrated in Figure 6, with timing relationships shown in Figure 7. The multiplexed BCD output data can be displayed on an LCD or LED display with the TC7211A (LCD) or TC7212A (LED) 4-digit display drivers.

The digital section is best described through a discussion of the control signals and data outputs.

RUN/$\overline{\text{HOLD}}$ Input

When left open, the RUN/$\overline{\text{HOLD}}$ (R/$\overline{\text{H}}$) input (pin 25) assumes a logic "1" level. With R/$\overline{\text{H}}$ = 1, the TC7135 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to logic "0," the measurement cycle in progress will be completed, and data held and displayed, as long as the logic "0" condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ initiates a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed logic "0" must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001-count auto-zero phase. At the end of this phase, the busy signal goes high.

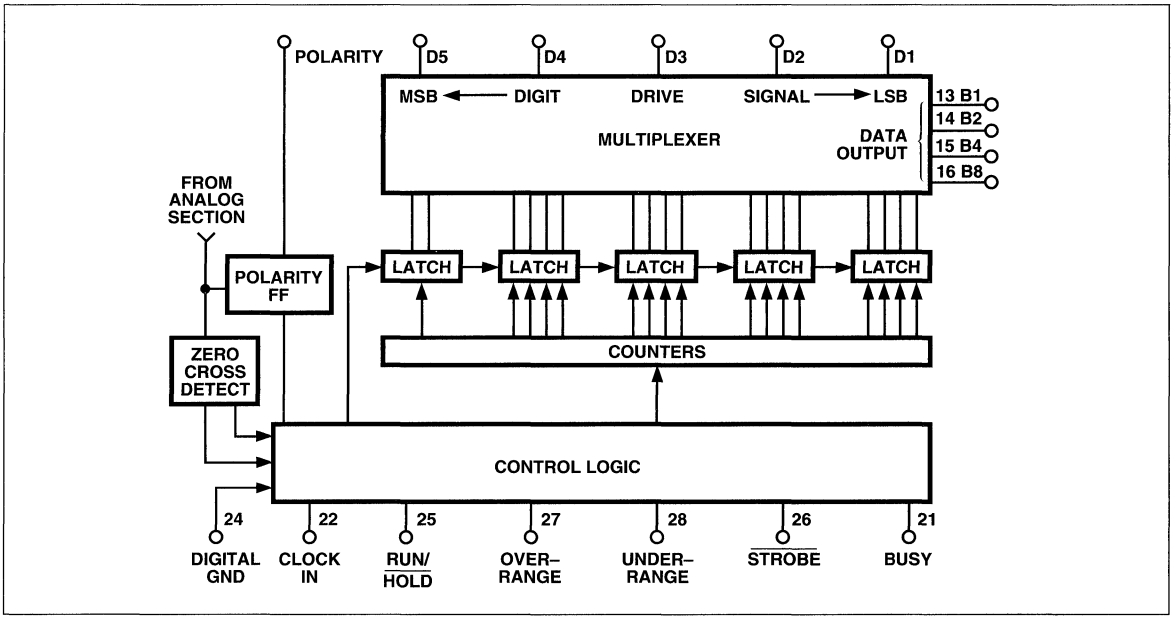


Figure 6. Digital Section Functional Diagram

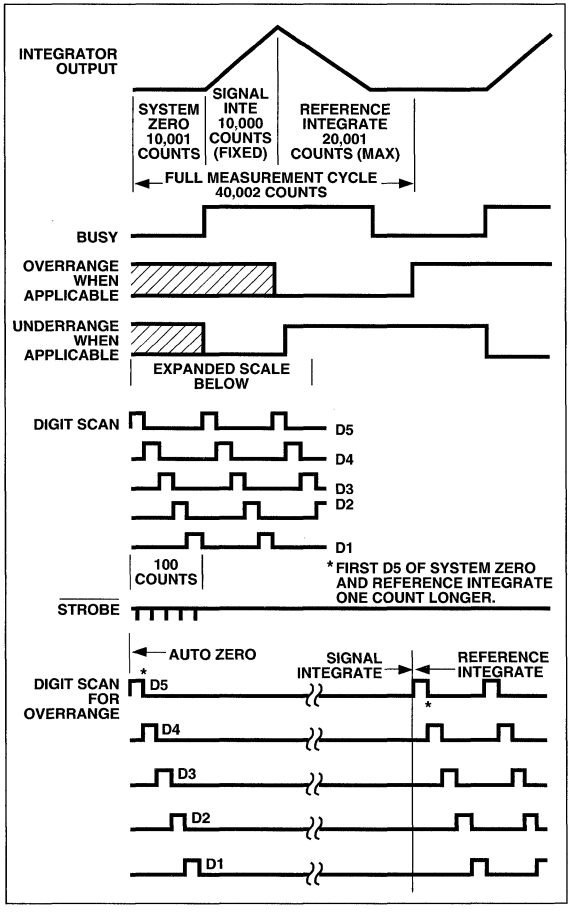


Figure 7. Timing Diagrams for Outputs

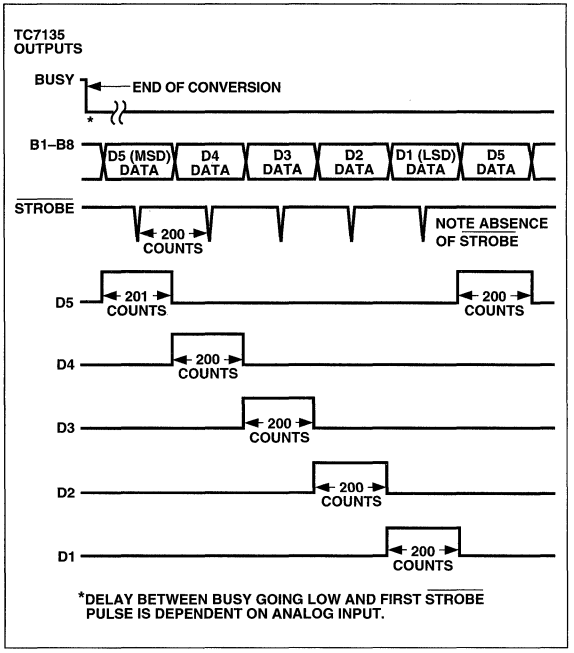


Figure 8. Strobe Signal Pulses Low Five Times per Conversion

STROBE Output

During the measurement cycle, the STROBE output (pin 26) control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_4 and D_5; see Figure 8).

D_5 goes high for 201 counts when the measurement cycles end. In the center of D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first STROBE occurs for one-half clock pulse. After D_5 strobe, D_4 goes high for 200 clock pulses. STROBE goes low 100 clock pulses after D_4 goes high. This continues through the D_1 drive pulse.

The digit drive signals will continue to permit display scanning. STROBE pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active-low STROBE pulses aid BCD data transfer to UARTs, microprocessors, and external latches. (See Application Note AN-16.)

BUSY Output

At the beginning of the signal-integration phase, BUSY (pin 21) goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to logic "0" after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero phase.

OVERRANGE Output

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output (pin 27) is set to logic "1." The OVERRANGE output register is set when BUSY goes low and reset at the beginning of the next reference-integration phase.

UNDERRANGE Output

If the output count is 9% of full scale or less (≤1800 counts), the UNDERRANGE output (pin 28) register bit is set at the end of BUSY. The bit is set low at the next signal-integration phase.

POLARITY Output

A positive input is registered by a logic "1" polarity signal. The POLARITY output (pin 23) is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The POLARITY bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

Digit Drive Outputs

Digit drive outputs are positive-going signals. Their scan sequence is D_5, D_4, D_3, D_2 and D_1 (pins 12, 17, 18, 19 and 20, respectively). All positive signals are 200 clock pulses wide, except D_5, which is 201 clock pulses.

All five digits are continuously scanned, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference-integrate phase. The scanning sequence is then repeated, providing a blinking visual display.

BCD Data Outputs

The binary coded decimal (BCD) outputs, B_8, B_4, B_2 and B_1 (pins 16, 15, 14 and 13, respectively) are positive true-logic signals. They become active simultaneously with digit drive signals. In an overrange condition, all data bits are logic "0".

APPLICATIONS INFORMATION

Component Value Selection

Integrating Resistor

The integrating resistor (R_{INT}) is determined by the full-scale input voltage and output current of the buffer used to charge the integrator capacitor (C_{INT}). Both the buffer amplifier and the integrator have a Class A output stage, with 100 µA of quiescent current. A 20 µA drive current gives negligible linearity errors. Values of 5 µA to 40 µA give good results. The exact value of R_{INT} for a 20 µA current is easily calculated:

$$R_{INT} = \frac{\text{Full-scale voltage}}{20\ \mu A}.$$

Integrating Capacitor

The product of R_{INT} and C_{INT} should be selected to give the maximum voltage swing to ensure tolerance build-up will not saturate integrator swing (approximately 0.3V from either supply). For ±5V supplies, and analog common tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10 µF to 0.47 µF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing}}.$$

A very important characteristic of the C_{INT} is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half-scale 0.9999. Any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitors

The size of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A large capacitor reduces noise. The reference capacitor (C_{REF}) should be large enough such that stray capacitance from its nodes to ground is negligible.

The dielectric absorption of C_{REF} and C_{AZ} is only important at power-on, or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required during the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in overall absolute accuracy of the converter. Therefore, it is recommended that high-quality references be used where high-accuracy, absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TC04	TelCom Semiconductor
TC05	TelCom Semiconductor

Conversion Timing

Line Frequency Rejection

A signal-integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 100 kHz clock frequency will reject 50 Hz, 60 Hz and 400 Hz noise, corresponding to 2.5 readings per second.

Table II. Line Frequency Rejection

Oscillator Frequency (kHz)	Frequency Rejected (Hz)
300, 200, 150, 120, 100, 40, 33-1/3	60
250, 166-2/3, 125, 100	50
100	50, 60, 400

Table III. Conversion Rate vs Clock Frequency

Conversion Rate (Conv/Sec)	Clock Frequency (kHz)
2.5	100
3.0	120
5.0	200
7.5	300
10.0	400
20.0	800
30.0	1200

Displays and Driver Circuits

TelCom Semiconductor manufactures three display decoder/driver circuits to interface the TC7135 to LCDs or LED displays. Each driver has 28 outputs for driving four 7-segment digit displays.

Device	Package	Description
TC7211AIPL	40-Pin Epoxy	4-Digit LCD Driver/Encoder
TC7212AIPL	40-Pin Epoxy	4-Digit LED Driver/Encoder

Several sources exist for LCDs and LED displays.

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Road Palo Alto, CA 94304	LED
AND	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrance, CA 90505	LCD

High-Speed Operation

The maximum conversion rate of most dual-slope ADCs is limited by frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period), half of the first reference integrate clock period is lost in delay. This means the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 with 250 μV, etc. This transition at mid-point is considered desirable by most users; however, if clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications, where the input signal is always of one polarity, comparator delay need not be a limitation. Since nonlinearity and noise do not increase substantially with frequency, clock rates up to ~1 MHz may be used. For a fixed clock frequency, the extra count (or counts) caused by comparator delay will be constant and can be digitally subtracted.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage onto the integrator output at the beginning of reference-integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated for and maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities during the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the applications section. The multiplexed output means if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates data once every clock pulse after transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter

is disabled for one clock pulse at the beginning of the reference integrate (deintegrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so true ratiometric readings result.

Generating a Negative Supply

A negative voltage can be generated from the positive supply by using a TC7660. (See Figure 9.)

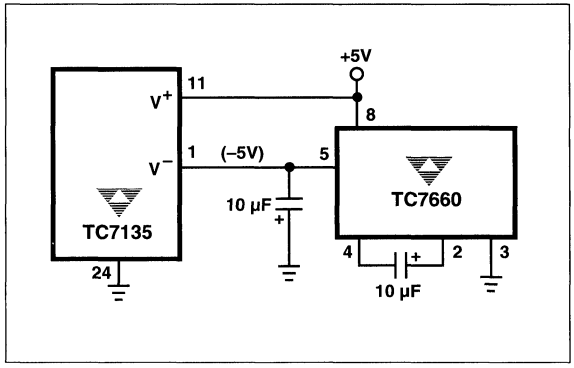
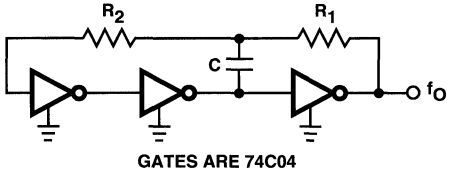


Figure 9. Negative Supply Voltage Generator

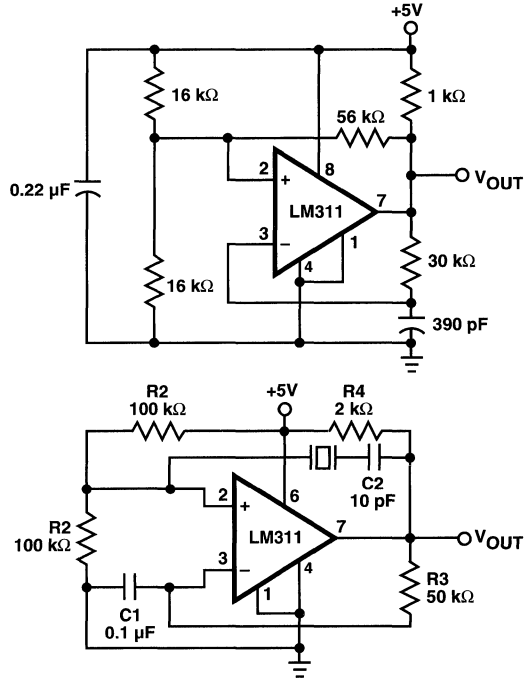
TYPICAL APPLICATIONS DIAGRAMS

RC Oscillator Circuit



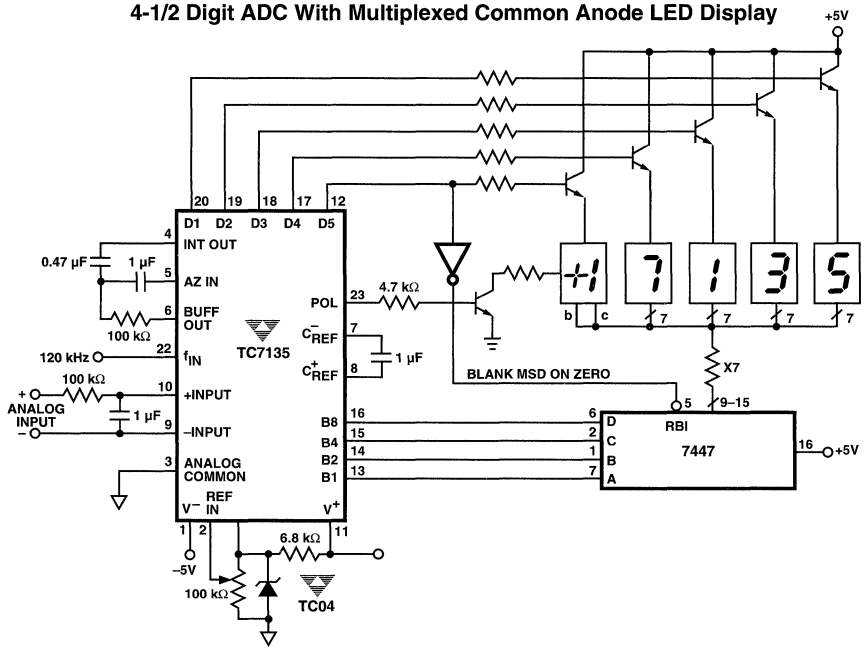
1. $f_O \approx \frac{1}{2\,C[0.41\,R_P + 0.70\,R_1]}$, $R_P = \frac{R_1\,R_2}{R_1 + R_2}$
   a. If $R = R_1 = R_2$, $f \cong 0.55/RC$
   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$
   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$
2. Examples:
   a. f = 120 kHz, C = 420 pF
      $R_1 = R_2 \approx 10.9\ k\Omega$
   b. f = 120 kHz, C = 420 pF, $R_2 = 50\ k\Omega$
      $R_1 = 8.93\ k\Omega$
   c. f = 120 kHz, C = 220 pF, $R_2 = 5\ k\Omega$
      $R_1 = 27.3\ k\Omega$

Comparator Clock Circuit

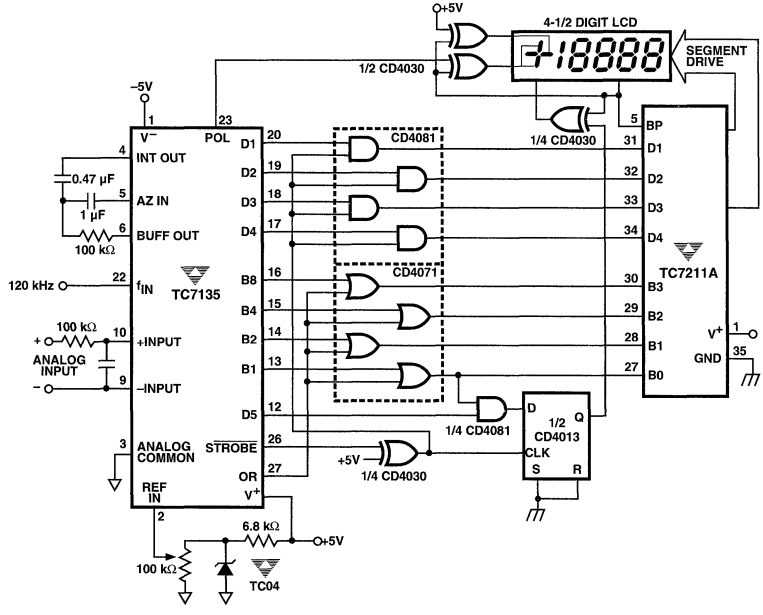


TYPICAL APPLICATIONS DIAGRAMS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Anode LED Display

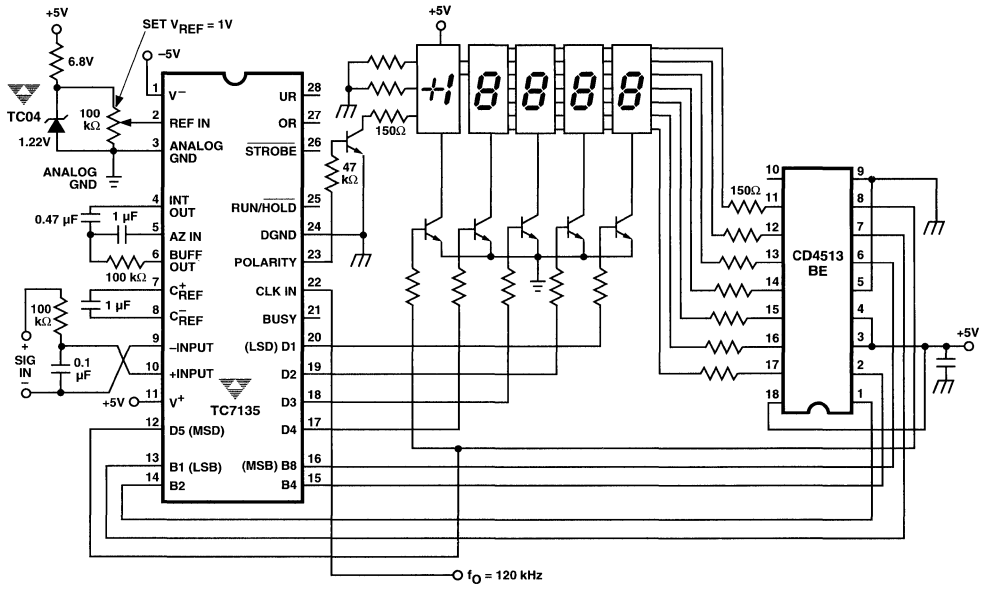


4-1/2 Digit ADC Interfaced to LCD With Digit Blanking on Overrange

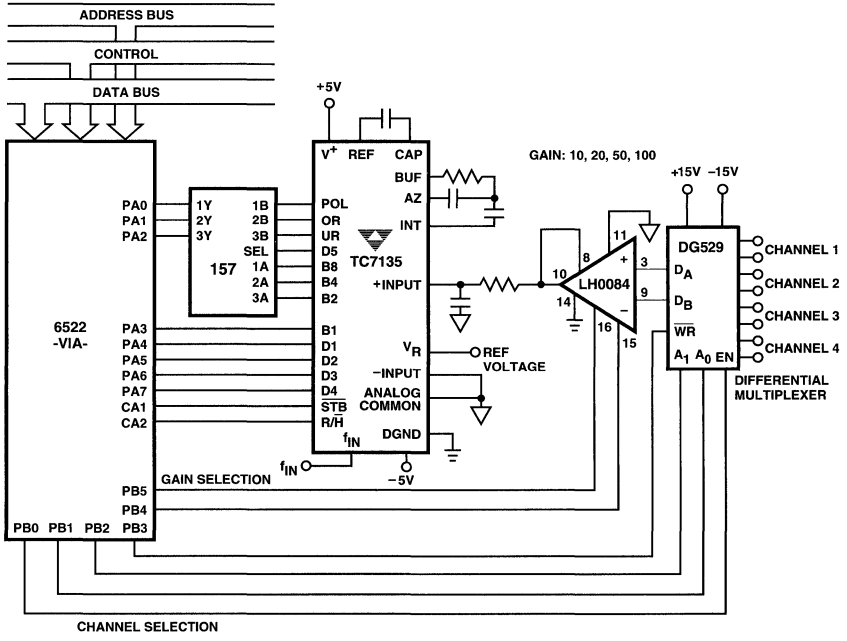


TYPICAL APPLICATIONS DIAGRAMS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Cathode LED Display



4-Channel Data Acquisition System

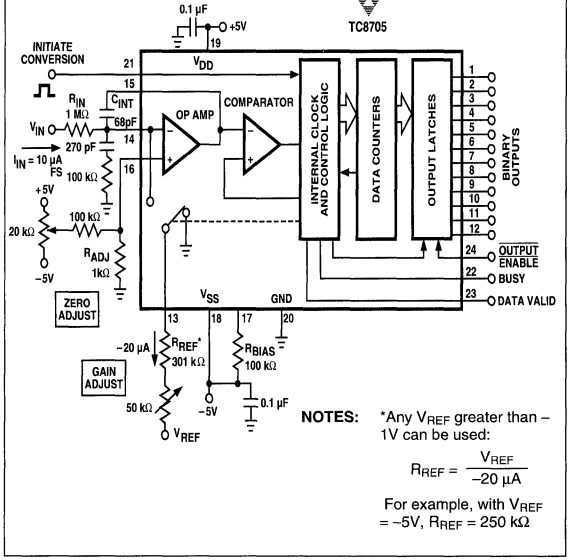


BINARY OUTPUT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **High Accuracy — 12-Bit Resolution With < ± 1/2 LSB Error**
- **Monotonic Performance — No Missing Codes**
- **Monolithic CMOS Construction Gives Low Power Dissipation ..... 20 mW Typ**
- **Contains All Required Active Elements — Needs Only Passive Support Components, Reference Voltage, and Dual-Power Supply**
- **High Stability Over Full Temperature Range**
  - **— Gain Temperature Coefficient.. < 25 ppm/°C Typ**
  - **— Zero Drift ..... < 30 µV/°C Typ**
  - **— Differential Nonlinearity Drift . < 25 ppm/°C Typ**
- **Latched Parallel Binary Outputs**
- **Three-State, Bus Compatible Outputs**
- **LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs**
- **Strobed or Free-Running Conversion**
- **Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor**

TEST CIRCUIT



NOTES: *Any V_{REF} greater than −1V can be used:

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example, with V_{REF} = −5V, R_{REF} = 250 kΩ

GENERAL DESCRIPTION

The TC8705 is a 12-bit monolithic CMOS analog-to-digital converter (ADC). Fully self-contained in a single 24-pin dual-in-line package, the converter requires only passive support components, reference and power supplies.

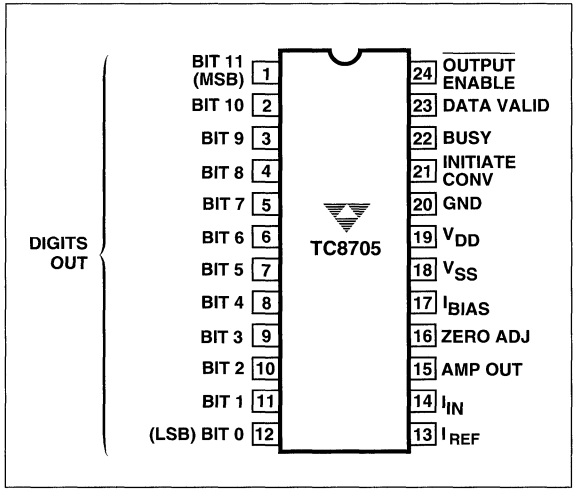
Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion, the total count is latched into the digital outputs as a 12-bit binary word.

The TC8705 features a three-state output bus controlled by an output enable input. The output enable control switches to a high impedance or off-state when held high. The off-state allows bus-organized output connections.

ORDERING INFORMATION

Part No.	Previous Part No.	Package	Temperature Range
TC8705CPG	TSC8705CJ	24-Pin PDIP	0°C to +70°C
TC8705EHG	TSC8705CL	24-Pin CerDIP	− 40°C to +85°C

PIN CONFIGURATION



TC8705

ABSOLUTE MAXIMUM RATINGS*

$V_{DD} - V_{SS}$ Span 18V
I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... – 0.3V to V_{DD} +0.3V
Operating V_{DD} and V_{SS} Range ..... 3.5V to 7V
Storage Temperature Range ..... – 65°C to +150°C
Operating Temperature Range
CPG ..... 0°C to +70°C
EJG ..... – 40°C to +85°C
MJG, MHG ..... – 55°C to +125°C

Package Dissipation ..... 500 mW
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V, V_{SS} = – 5V, V_{GND} = 0, V_{REF} Pin = –6.4V, R_{BIAS} = 100 kΩ, test circuit shown, unless otherwise specified. T_A = +25°C unless full temperature range is specified (– 40°C to +85°C for EHG package, 0°C to +70°C for CPG package).

Parameter	Test Conditions	Definition	Min	Typ	CP/EJ Max	MJ/MH Max	Unit
Resolution		Binary Word Length of Digital Output	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	— —	±1/4 1	±1/2 ±1.5	±1/2 —	LSB LSB
Differential Nonlinearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Nonlinearity Temperature Drift	Full Temperature Range	Variation in Differential Nonlinearity Due to Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate by Trimming R_{IN} or R_{REF})	—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation in A Due to Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset	I_{IN} = 0, C_{INT} = 68 pF, R_{ADJ} = 1 kΩ (See Test Circuit)	Correction at Zero Adjust to Give Zero Output When Input is Zero	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offset Due to Temperature Change	—	±3	±5	±8	ppm/°C
Analog Input (See Note)							
I_{IN} Full Scale		Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	µA
I_{REF}		Reference Current Input to Achieve Specified Accuracy	—	– 20	—	—	µA
Digital Input							
$V_{IN}^{(1)}$	Full Temperature Range	Logic "1" Input Threshold for Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logic "0" Input Threshold for Initiate Conversion Input	—	—	1.5	1.5	V

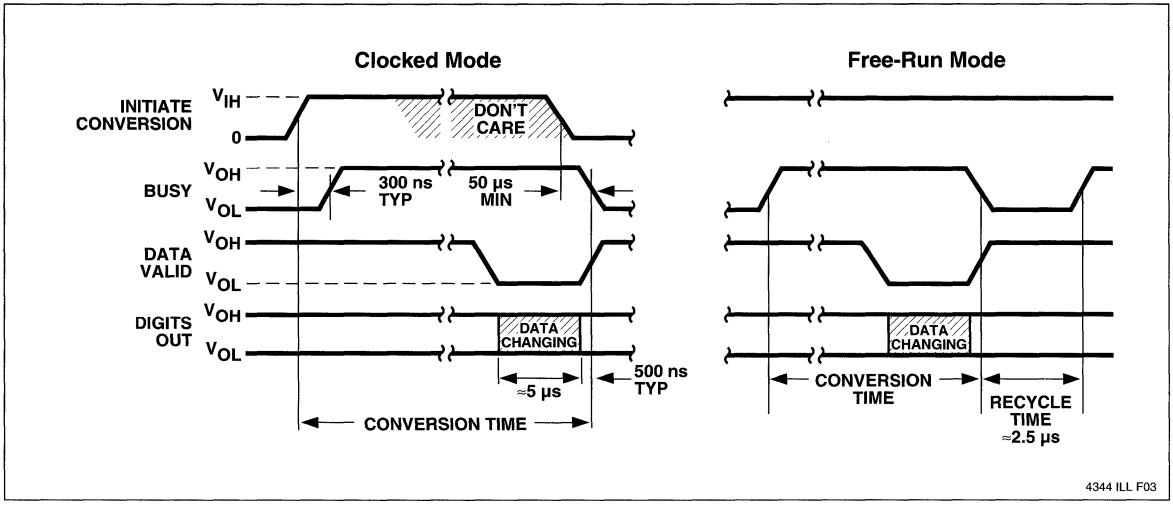
ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Test Conditions	Definition	Min	Typ	CP/EJ Max	MJ/MH Max	Unit
Propagation Delay							
Output Enable	C_L = 100 pF, R_L = 1 kΩ	t_{PLH}, t_{PHL}	—	500	—	1000	ns
Digital Output							
$I_{O(OFF)}$	OE = 3.5V 0.4V < V_C < 2.4V	Off-State Output Current	—	0.1	±10	±10	µA
V_{OUT}(1)	Full Temperature Range, I_{OUT} = −10 µA I_{OUT} = −500 µA	Logic "1" Output Voltage for Digits Out, Busy, and Data Valid Outputs	 4.5 2.4	 — —	 — —	 — —	 V V
V_{OUT}(0)	Full Temperature Range, V_{DD} = 4.75V I_{OUT} = 500 µA	Logic "0" Output Voltage for Digits Out, Busy, and Data Valid Outputs	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Full Temperature Range	Time Required to Perform One Complete A/D Conversion	—	20	24	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = +5V		42	50	—	—	Conv/ Second
Minimum Pulse Width for Initiate Conversion	Full Temperature Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent							
J/H Package	Full Temperature Range, $V_{INT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	—	1.4	2.5	3.5	mA
P Package			—	1.4	5	—	mA
I_{SS} Quiescent							
H Packages	Full Temperature Range, $V_{INT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	—	−1.6	−2.5	−3.5	mA
P Package			—	−1.6	−5	—	mA
Supply Sensitivity	V_{DD} ±1V, V_{SS} ±1V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1	±1	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5V ± 1V	Change in full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V
Supply Voltages							
V_{DD}			+3.5	—	+7.0	+7.0	V
V_{SS}			−3.5	—	−7.0	+7.0	V
Min. Operating Supply Span			7.0	—	14.0	14.0	V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See "Test Circuit."

TC8705

TIMING DIAGRAMS



CIRCUIT DESCRIPTION

During conversion, the sum of a continuous current (I_{IN}) and pulses of a reference current (I_{REF}) is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} is balanced against the pulses of I_{REF}. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock, in addition to an operational amplifier, comparator, latching output buffers, and housekeeping logic. One counter is a clock counter which starts counting clock pulses after a reset pulse; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times I_{REF} is switched into the summing input of the amplifier during the period defined by the clock counter.

When the initiate conversion input is strobed with a positive signal, the busy line latches high and a 10 µs (times given are approximate) start-up cycle begins. The integrating capacitor is discharged and both counters are reset during this start-up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 µs shutdown cycle. During the shutdown cycle, data valid goes low for 5 µs. This binary sequence is shown in the timing diagrams. Busy is true high and, when the circuit is busy, initiate conversion has no effect and may be high or low. Data valid is also true high. The data from a conversion remains valid for as long as power is applied to the circuit or until data valid falls at the end of a subsequent conversion, at which time the output data is updated to reflect the latest conversion.

PIN FUNCTIONS

Initiate Conversion Input

Accepts CMOS and most +5V logic inputs. Applying a logic "1" to the initiate conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the initiate conversion pin is disabled until conversion is complete. Two modes of operation are permitted: clocked or free-running. For clocked operation, the initiate conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation, the initiate conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low-power TTL (can sink and source 500 µA). A logic "1" output on the busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates conversion is complete and the result has been latched at the digit out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the

device is operating in the free-running mode, the busy output will remain low for approximately 2.5 µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low-power TTL (can sink and source 50 µA). A logic "1" output at the data valid pin indicates the digits out pins are latched with the result of the last conversion cycle. The data valid output goes to logic "0" approximately 5 µs before the completion of a conversion cycle. During this 5 µs interval new data is being transferred to the digits out pins, and the digits out are not valid.

Digits Out

The binary digit outputs (Bit 0 . . . Bit 11) which are the result of the A/D conversion. These outputs are CMOS logic and low-power TTL compatible.

APPLICATIONS INFORMATION

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital counts} = \frac{V_{IN} \bullet A \bullet R_{REF}}{R_{IN} \bullet V_{REF}},$$

$$A = 8208$$

where digital counts is the value of the binary output word presented at digits out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Outputs MSB LSB
$V_{IN} \geq$ Full Scale	1 . . . 111 . . . 1
= Full Scale –1 LSB	1 . . . 111 . . . 0
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high-accuracy conversion system depends on the voltage regulation of V_{REF} and thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. Supply connections V_{DD} and V_{SS} should have bypass capacitors of 0.1 µF value, or larger, at the device pins.

R_{IN}, R_{REF}

Values of these components are chosen to give a full-scale input current of approximately 10 µA and a reference current of approximately –20 µA:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}.$$

Examples:

$$R_{IN} \cong \frac{10V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

R_{BIAS}

Specifications for the TC8705 are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS}, the A/D will convert much faster and the supply current will be higher. For example, when R_{BIAS} is 20kΩ, the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA. Likewise, if R_{BIAS} is increased, the conversion time will be longer and the supply current will be much lower. For example, when R_{BIAS} = 1 MΩ, the conversion time will be six times longer, and supply current is now reduced to 0.5 mA. For details of this relationship, refer to AN–9 typical performance curves.

R_{DAMP}

The exact value is not critical, but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP}

The exact value is not critical, but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

The exact value is not critical, but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14 and 15.

TC8705

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended, with 0.05% line and load regulation, and 0.1 μF decoupling capacitors.

Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e., below zero and above full scale), it is recommended transition points be used in setting the zero and full-scale values. The recommended procedure is:

(1) Set initiate conversion control high to provide free-run operation and verify converter is operating.

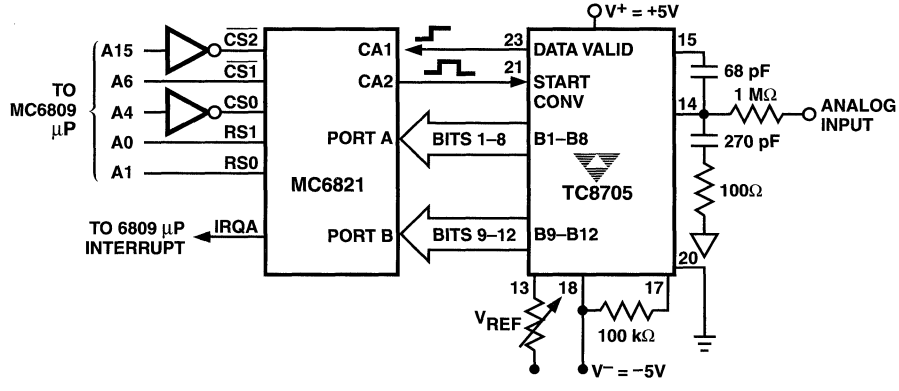
(2) Set V_{IN} to +1/2 LSB and trim the zero-adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.

(3) For full-scale adjustment, set V_{IN} to the full-scale value less 1-1/2 LSB and trim the gain-adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

TYPICAL APPLICATION/DESIGN CIRCUITS

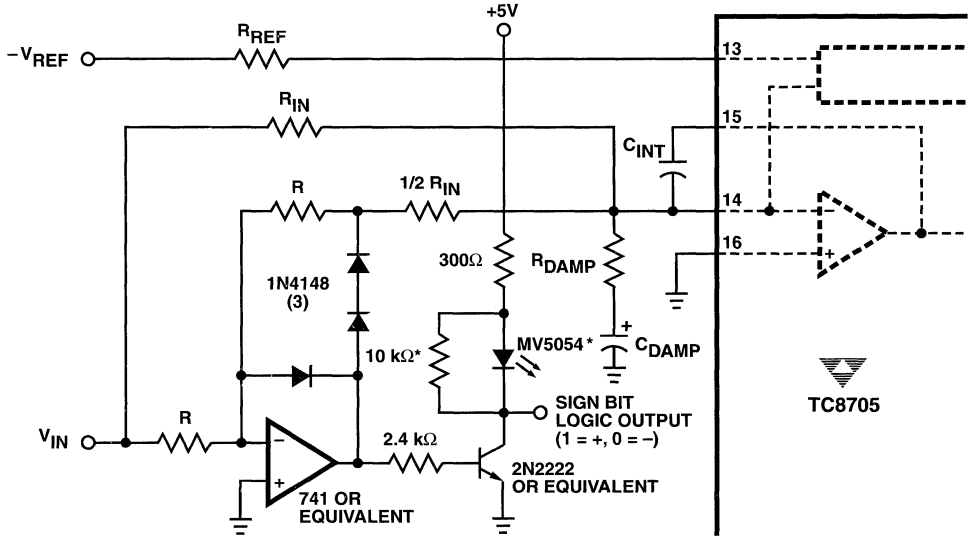
TC8705 Interface to MC6821 PIA



TYPICAL APPLICATION/DESIGN CIRCUITS (Cont.)

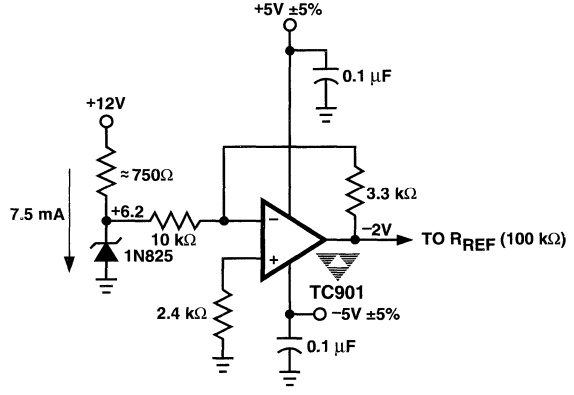
Bipolar Operation (+ and – Inputs)

ABSOLUTE VALUE CIRCUIT WITH SIGN



*Optional visual indication of negative input.
NOTE: Values for R should be between 10 kΩ and 100 kΩ.

Reference Voltage Supply

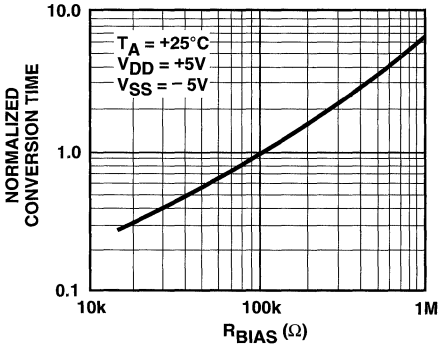


NOTE: V_{REF} = 2V using voltages derived from 8080A µP.

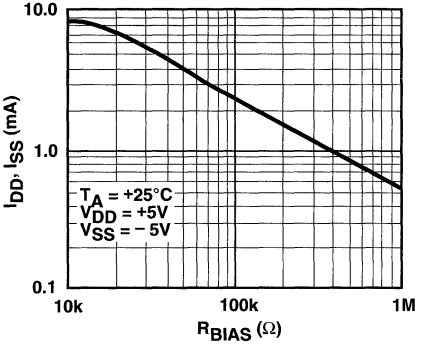
TC8705

TYPICAL PERFORMANCE CURVES

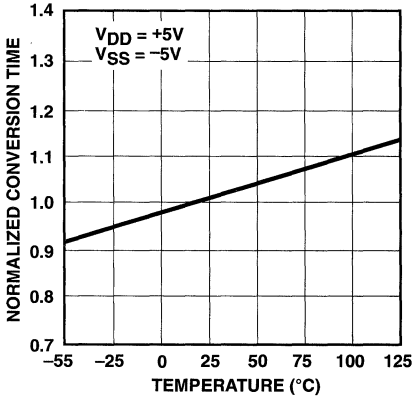
Conversion Time vs R_{BIAS}



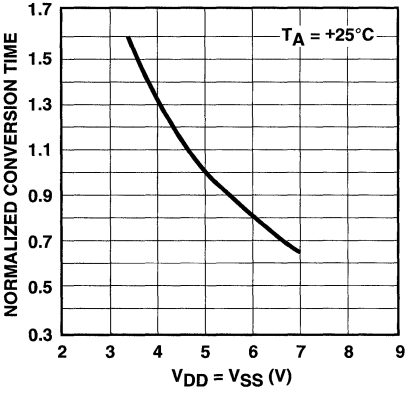
Supply Current vs R_{BIAS}



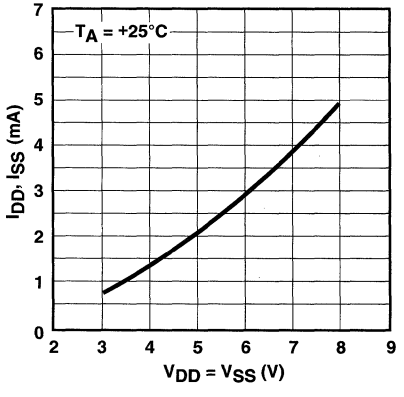
Conversion Time vs Temperature



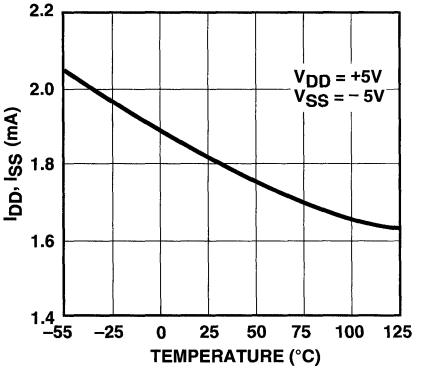
Conversion Time vs Supply Voltage



Supply Current vs Supply Voltage

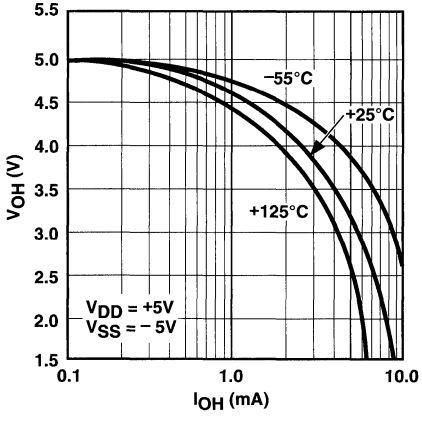


Supply Current vs Temperature

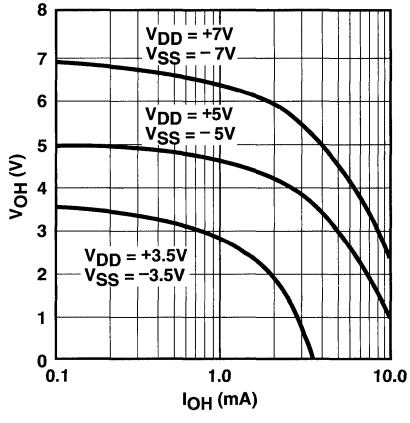


TYPICAL PERFORMANCE CURVES (Cont.)

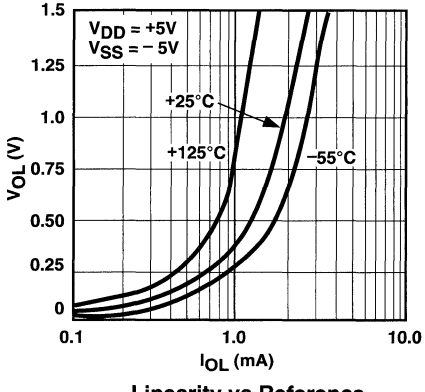
Output Source Current vs Temperature



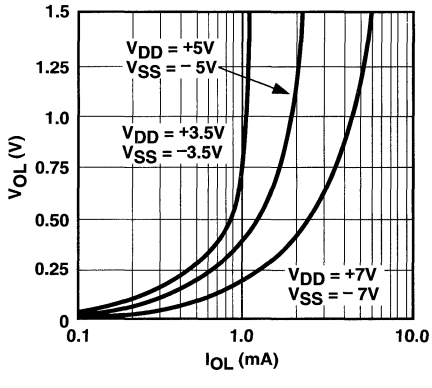
Output Source Current vs Supply Voltage



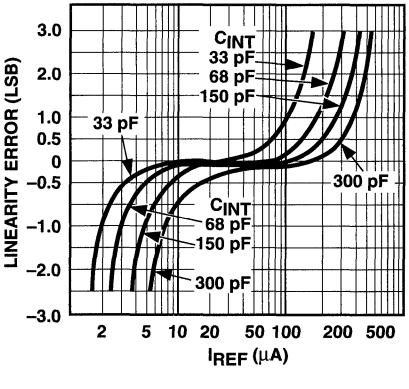
Output Sink Current vs Temperature



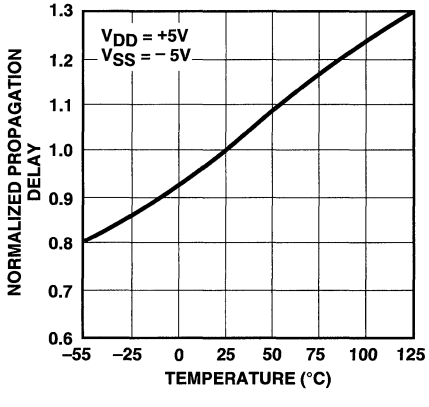
Output Sink Current vs Supply Voltage



Linearity vs Reference Current Input



Three-State Propagation Delay



3-1/2 DIGIT ADC

FEATURES

- **Accuracy: ±0.05% of Reading ±1 Count**
- **Two Voltage Ranges: 1.999V and 199.9 mV**
- **Up to 25 Conversions Per Second**
- **Z_{IN} > 1000M Ohms**
- **Single Positive Voltage Reference**
- **Auto-Polarity and Auto-Zero**
- **Overrange and Underrange Signals Available**
- **Operates in Auto-Ranging Circuits**
- **Uses On-Chip System Clock or External Clock**
- **Wide Supply Range: e.g., ±4.5V to ±8V**
- **Available in Surface-Mount Packages**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC14433AEPG	24-Pin Plastic DIP	– 40°C to +85°C
TC14433BEPG	24-Pin Plastic DIP	– 40°C to +85°C
TC14433EPG	24-Pin Plastic DIP	– 40°C to +85°C
TC14433AEJG	24-Pin CerDIP	– 40°C to +85°C
TC14433BEJG	24-Pin CerDIP	– 40°C to +85°C
TC14433EJG	24-Pin CerDIP	– 40°C to +85°C
TC14433ELI	28-Pin PLCC	– 40°C to +85°C
TC14433AELI	28-Pin PLCC	– 40°C to +85°C

GENERAL DESCRIPTION

The TC14433 is a low power, high-performance, monolithic CMOS 3-1/2 digit A/D converter. The TC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual-slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TC14433 can operate over a wide range of power supply voltages, including batteries and standard 5-volt supplies.

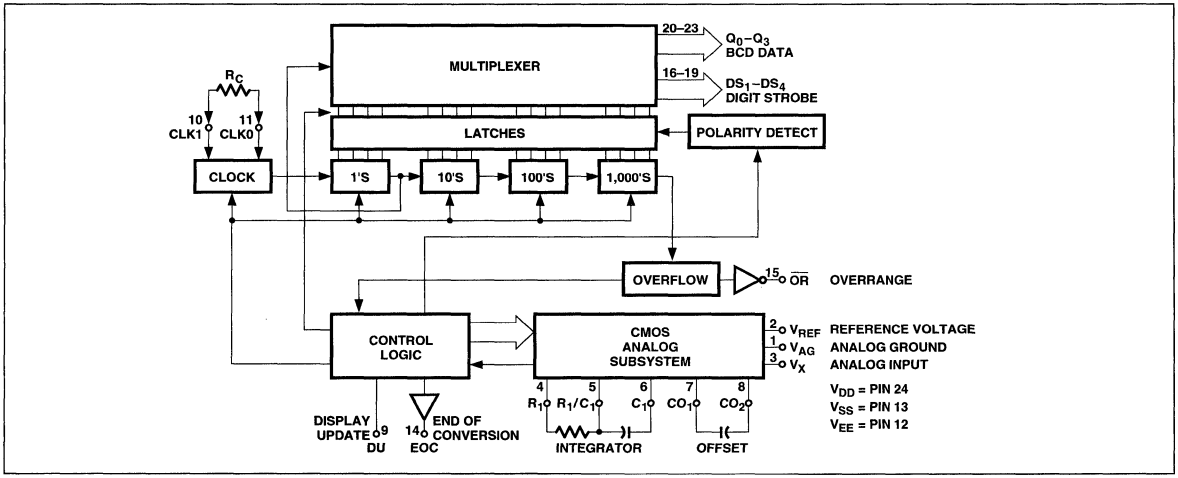
The TC14433 will interface with the TC7211A LCD display driver.

The TC14433A features improved performance over the industry standard TC14433. Rollover, which is the measurement of identical positive and negative signals, is guaranteed to have the same reading within one count for the TC14433A. Power consumption of the TC14433A is typically 4 mW, approximately one-half that of the industry standard TC14433.

APPLICATIONS

- **Portable Instruments**
- **Digital Voltmeters**
- **Digital Panel Meters**
- **Digital Scales**
- **Digital Thermometers**
- **Remote A/D Sensing Systems**
- **MPU Systems**
- **See Application Notes 19 and 21**

FUNCTIONAL BLOCK DIAGRAM



TC14433
TC14433A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	– 0.5 to +18	Vdc
Voltage, Any Pin, Referenced to V_{EE}	V	– 0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	– 40 to +85	°C
Storage Temperature Range	T_{STG}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage:			
V_{DD} to Analog Ground	V_{DD}	+5 to +8	Vdc
V_{EE} to Analog Ground	V_{EE}	– 2.8 to – 8	Vdc
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ± 20%	µF

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(C_I = 0.1 µF mylar, R_I = 470 kΩ at V_{REF} = 2V, R_I = 27 kΩ at V_{REF} = 200 mV, C_O = 0.1 µF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	– 40°C Min	– 40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Analog Input											
Rollover Error (Difference in reading for equal positive and negative reading near full-scale)	14433A			—	—	– 1	—	+1	—	—	Counts
$-V_{IN} = +V_{IN}$: 200 mV Full-Scale	14433			—	—	—	—	—	—	—	
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2V)		5	– 5	—	—	– 0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200 mV)		5	– 5	—	—	– 1 count	—	+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.99V, V_{REF} = 2V)		5	– 5	—	—	—	—	2	—	—	LSD
(V_X = 199 mV, V_{REF} = 200 mV)		5	– 5	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0V, V_{REF} = 2V)	—	5	– 5	—	—	—	0	0	—	—	LSD
Bias Current:											
Analog Input	—	5	– 5	—	—	—	±20	±100	—	—	pA
Reference Input	—	5	– 5	—	—	—	±20	±100	—	—	pA
Analog Ground	—	5	– 5	—	—	—	±20	±500	—	—	pA
Common-Mode Rejection (V_X = 1.4V, V_{REF} = 2V, f_{OC} = 32 kHz)		5	– 5	—	—	—	65	—	—	—	dB
Digital											
Output Voltage–Pins 14 to 23 (Note 3)											
(V_{SS} = 0V) "0" Level	V_{OL}	5	– 5	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5	– 5	4.95	—	4.95	5	—	4.95	—	V
(V_{SS} = –5V) "0" Level	V_{OL}	5	– 5	—	– 4.95	—	– 5	– 4.95	—	– 4.95	V
"1" Level	V_{OH}	5	– 5	4.95	—	4.95	5	—	4.95	—	V

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Output Current — Pins 14 to 23 (V_{SS} = 0V)											
(V_{OH} = 4.6V) Source	I_{OH}	5	−5	−0.25	—	−0.2	−0.36	—	−0.14	—	mA
(V_{OL} = 0.4V) Sink	I_{OL}	5	−5	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = −5V)											
(V_{OH} = 5V) Source	I_{OH}	5	−5	−0.62	—	−0.5	−0.9	—	−0.35	—	mA
(V_{OL} = −4.5V) Sink	I_{OL}	5	−5	1.6	—	1.3	2.25	—	0.9	—	mA
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5	−5	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5	−5	—	±0.3	—	±0.00001	±0.3	—	±1	µA
Power											
Quiescent Current		5	−5	—	3.7	—	0.4	2	—	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0) 14433A	I_Q	8	−8	—	7.4	—	1.4	4	—	3.2	mA
14433	I_Q	5	−5	—	3.7	—	0.9	2	—	1.6	mA
		8	−8	—	7.4	—	1.8	4	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2V)	—	5	−5	—	—	—	0.5	—	—	—	mV/V

NOTES: 1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. The LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-pin DIP.

TC14433
TC14433A

TYPICAL CHARACTERISTICS

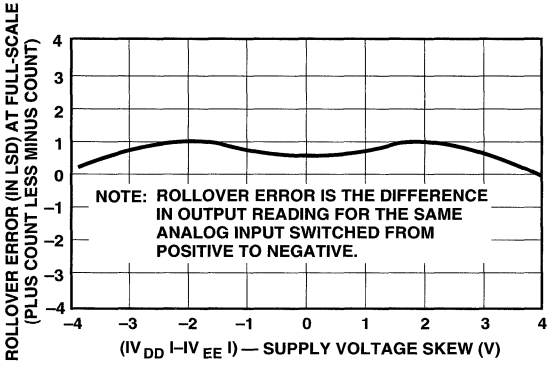


Figure 1. Typical Rollover Error vs Power Supply Skew

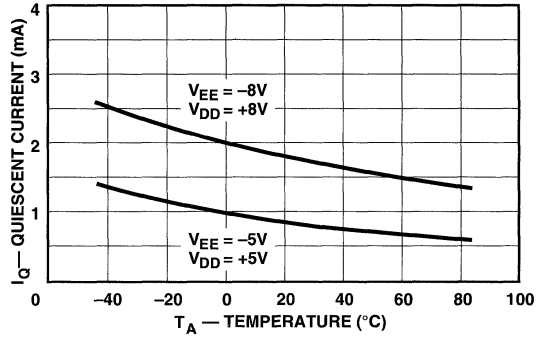


Figure 2. Typical Quiescent Power Supply Current vs Temperature

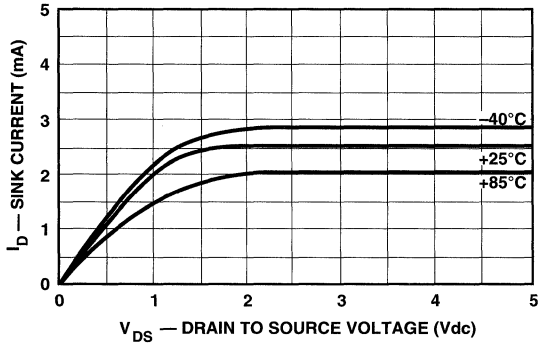


Figure 3. Typical N-Channel Sink Current at V_{DD}–V_{SS} = 5 Volts

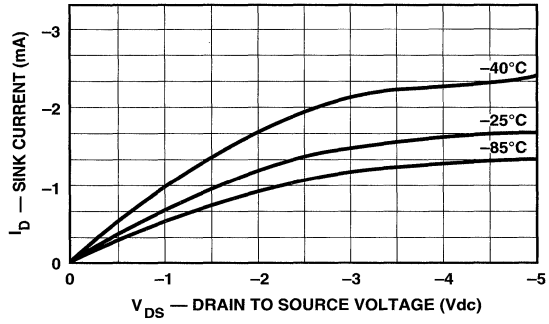


Figure 4. Typical P-Channel Source Current at V_{DD}–V_{SS} = 5 Volts

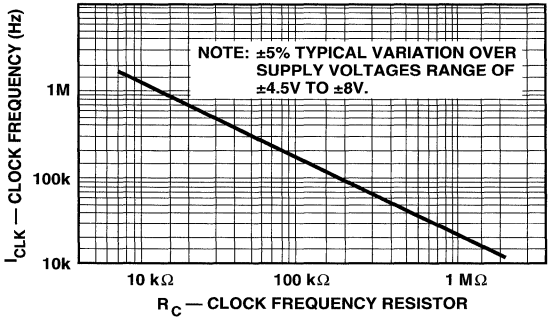


Figure 5. Typical Clock Frequency vs Resistor (R_C)

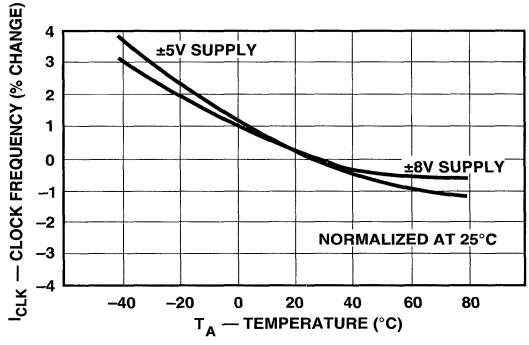
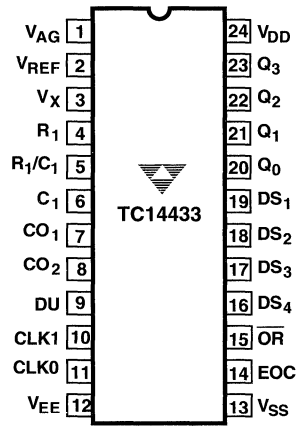


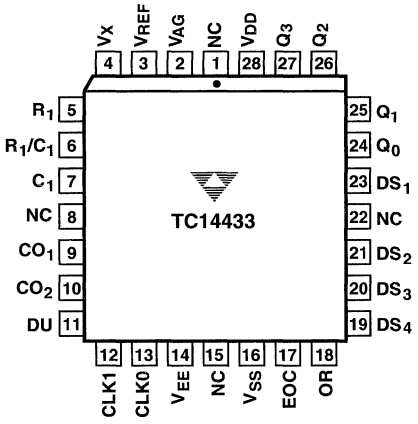
Figure 6. Typical % Change of Clock Frequency vs Temperature

$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

PIN CONFIGURATIONS





$$R_1 = \frac{V_X\ (max)}{C_1}\ 3\ \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (max) - 0.5$$

$$T = 4000\ 3\ \frac{1}{f_{CLK}}$$

WHERE:
R_1 IS IN kΩ
V_{DD} IS THE VOLTAGE AT PIN 24 REFERENCED TO V_{AG}
V_X IS THE VOLTAGE AT PIN 3 REFERENCED TO V_{AG}
f_{CLK} IS THE CLOCK FREQUENCY AT PIN 10 IN kHz

TC14433
TC14433A

PIN DESCRIPTIONS

Pin No. 24-Pin DIP	Symbol	Description
1	V_{AG}	This is the analog ground; it has a high input impedance — This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
2	V_{REF}	Reference voltage — Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999V requires 2V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset also. When switched to V_{EE}, the system is reset to the beginning of the conversion cycle.
3	V_X	The unknown input voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratiometric A/D conversion.
4	R_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1.
5	R_1/C_1	R_1 = 470 kW (resistor) for 2V full-scale.
6	C_1	R_1 = 27 kW (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
7	CO_1	These pins are used for connecting the offset correction capacitor. The recommended value
8	CO_2	is 0.1 μF.
9	DU	Display update input pin — When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
10	CLK_1	Clock input pins — The TC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency.
11	CLK_0	A crystal or OC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kW resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves; see Figure 9 for alternate circuits.)
12	V_{EE}	Negative power current — Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
13	V_{SS}	Negative power supply for output circuitry — This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between the V_{DD} –3 volts and V_{EE}.
14	EOC	End of conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one-half the period of the system clock.
15	OR	Overrange pin — Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
16	DS_4	Digit select pins — The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse.
17	DS_3	The remaining digits turn on in sequence from MSD to LSD.
18	DS_2	To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included.
19	DS_1	Clock frequency divided by 80 equals multiplex rate. For example, a system clock of 60 kHz gives a multiplex rate of 0.8 kHz.
20	Q_0	See Figure 12 for digit select timing diagram.
21	Q_1	BCD data output pins — Multiplexed BCD outputs contain three full digits of information during digit select DS_2, DS_3, DS_4.
22	Q_2	During DS_1, the 1/2 digit, overrange, underrange and polarity information is available.
23	Q_3	Refer to truth table.
24	V_{DD}	Positive power supply — This is the most positive power supply pin.

CIRCUIT DESCRIPTION

The TC14433 CMOS IC becomes a modified dual-slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry, as well as CMOS analog circuitry. It provides the user with digital functions (such as counters, latches, multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip.

Features of this system include auto-zero, high input impedances and auto-polarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage, where a ratio of 1 is equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into 6 segments. Figure 7 shows the conversion cycle in 6 segments for both positive and negative inputs.

Segment 1 — The offset capacitor (C_o), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — During this segment, the integrator output decreases to the comparator threshold voltage. At this time, a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable and less than 800 clock periods.

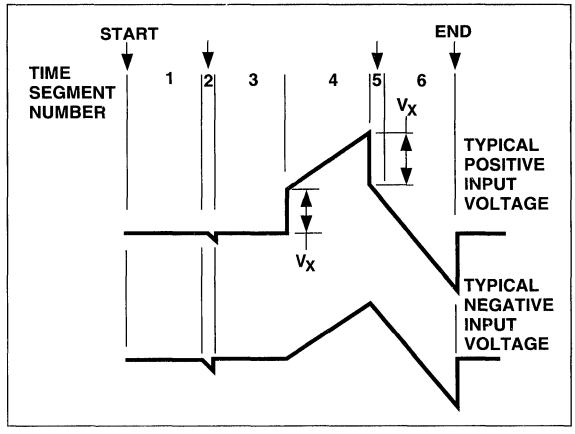


Figure 7. Integrator Waveforms at Pin 6

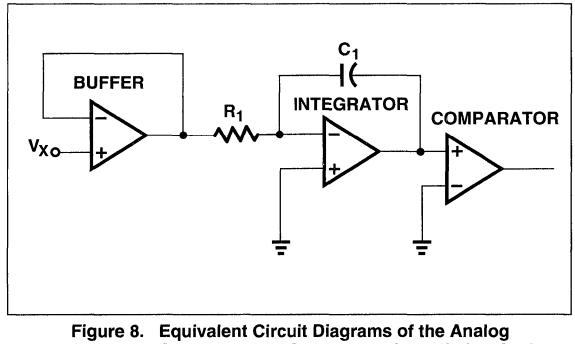


Figure 8. Equivalent Circuit Diagrams of the Analog Section During Segment 4 of the Timing Cycle

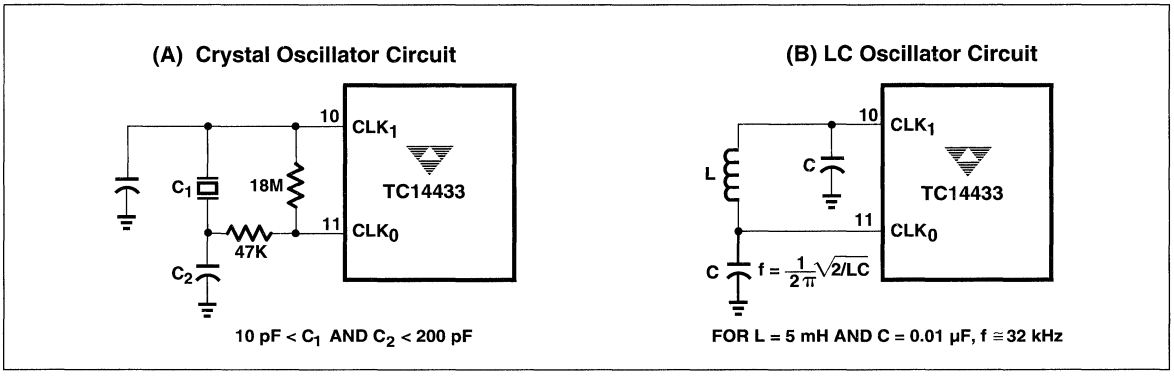


Figure 9. Alternate Oscillator Circuits

TC14433
TC14433A

Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_x) as the input to the integrator. Figure 8 shows the equivalent configuration of the analog section of the TC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

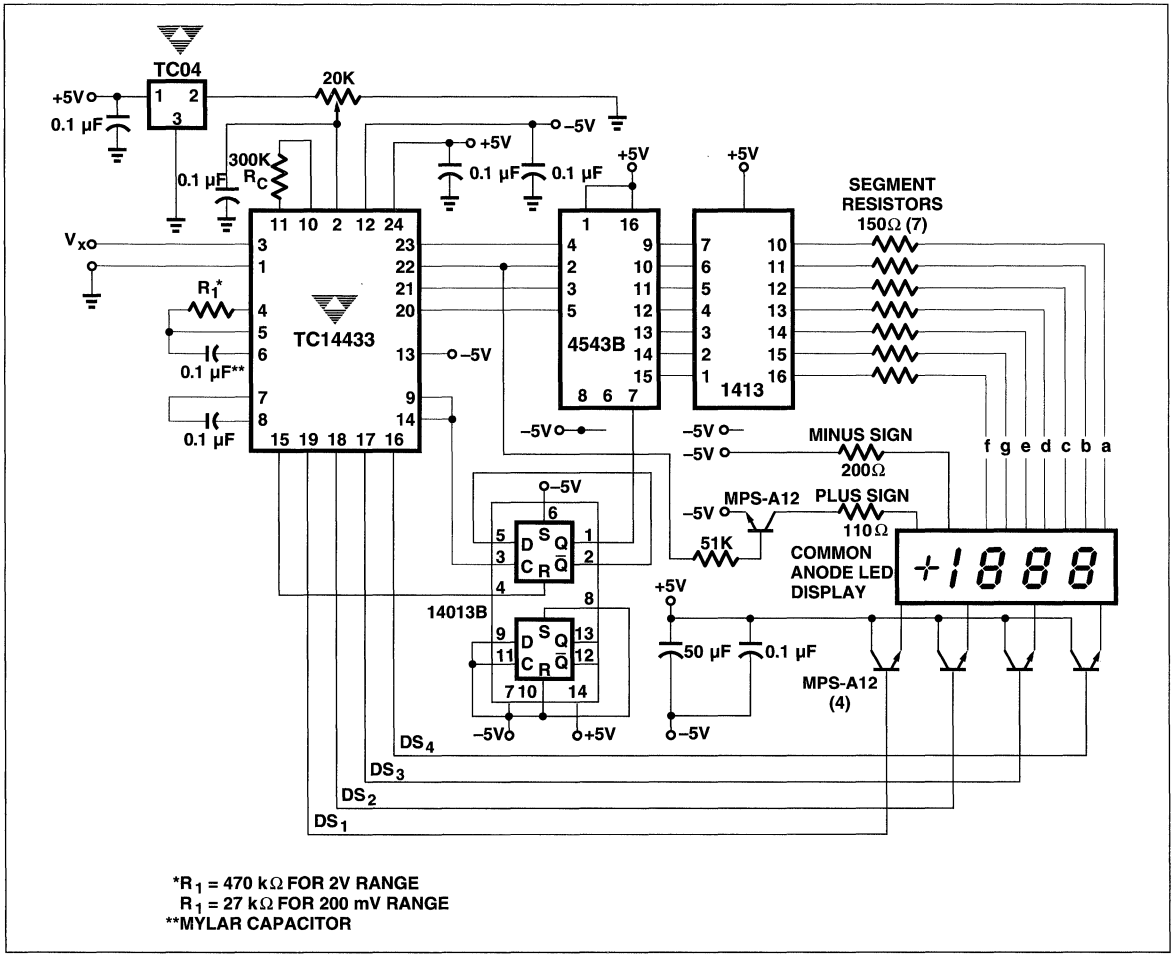


Figure 10. 3-1/2 Digit Voltmeter Common-Anode Displays, Flashing Overrange

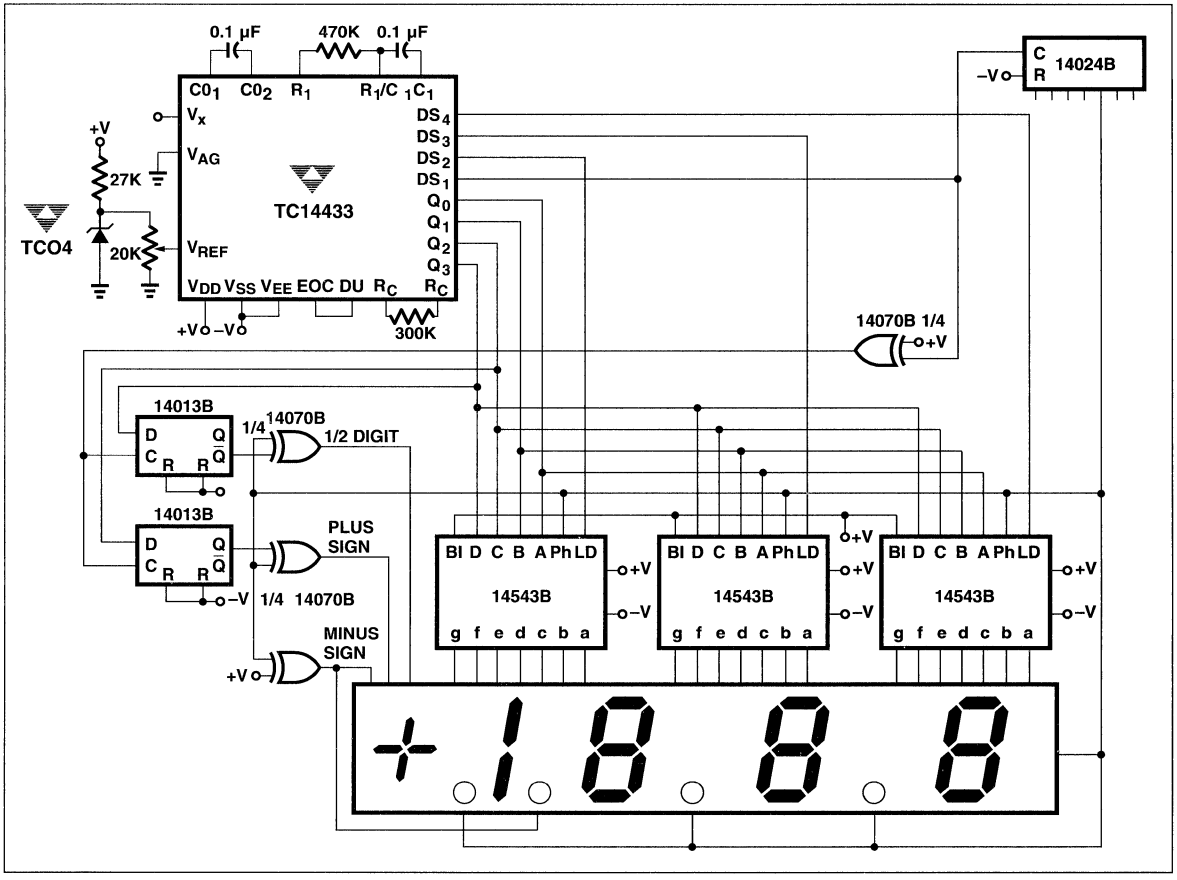


Figure 11. 3-1/2 Digit Voltmeter with LCD Display

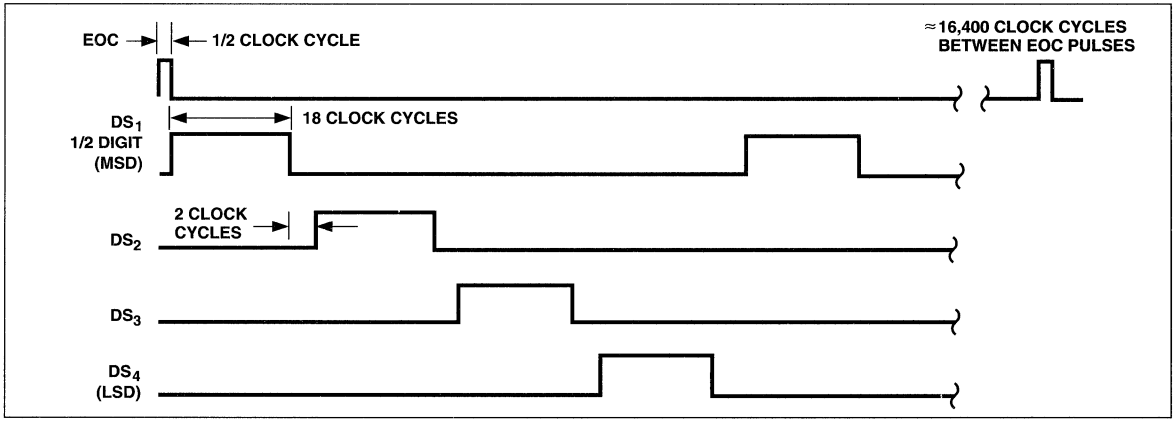


Figure 12. Digit Select Timing Diagram

TC14433
TC14433A

APPLICATIONS INFORMATION

Figure 10 is an example of a 3-1/2 digit voltmeter using the TC14433 with common-anode displays. This system requires a 2.5V reference. Full-scale may be adjusted to 1.999V or 199.9 mV. Input overrange is indicated by flashing a display. This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5V supply; however, the TC14433 will operate over a wide voltage range (see recommended operating conditions, page 2).

The circuit in Figure 11 shows a 3-1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here; however, one supply may be used when V_{SS} is connected to V_{EE}. In this case, V_{AG} must be at least 2.8V above V_{EE}.

When only segments b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication ($Q_3 = 0$ and $Q_0 = 1$) occurs when the count is greater than 1999; e.g., 1.999V for a reference of 2V. The underrange indication, useful for auto-ranging circuits, occurs when the count is less than 180; e.g., 0.180V for a reference of 2V.

CAUTION

If the most significant digit is connected to a display other than a "1" only, such as a full digit display, segments other than b and c must be disconnected. The BCD to 7-segment decoder must blank on BCD inputs 1010 to 1111.

Figure 14 is an example of a 3-1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit, the 14511B provides the segment drive and the 75492 or 1413 provides sink for digit current. Display is blanked during the overrange condition.

TRUTH TABLE

Coded Condition of MSD	Q_3	Q_2	Q_1	Q_0	BCD to 7-Segment Decoding
+0	1	1	1	0	Blank
–0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
–0 UR	1	0	1	1	Blank
+1	0	1	0	0	4–1 Hook up
–1	0	0	0	0	0–1 only
+1 OR	0	1	1	1	7–1 segments
–0 OR	0	0	1	1	3–1 b and c to MSD

NOTES:

Q_3 — 1/2 digit, low for "1", high for "0"

Q_2 — Polarity: "1" = positive, "0" = negative

Q_0 — Out of range condition exists if $Q_0 = 1$. When used in conjunction with Q_3, the type of out of range condition is indicated; i.e., $Q_3 = 0 \rightarrow$ OR or $Q_3 = 1 \rightarrow$ UR.

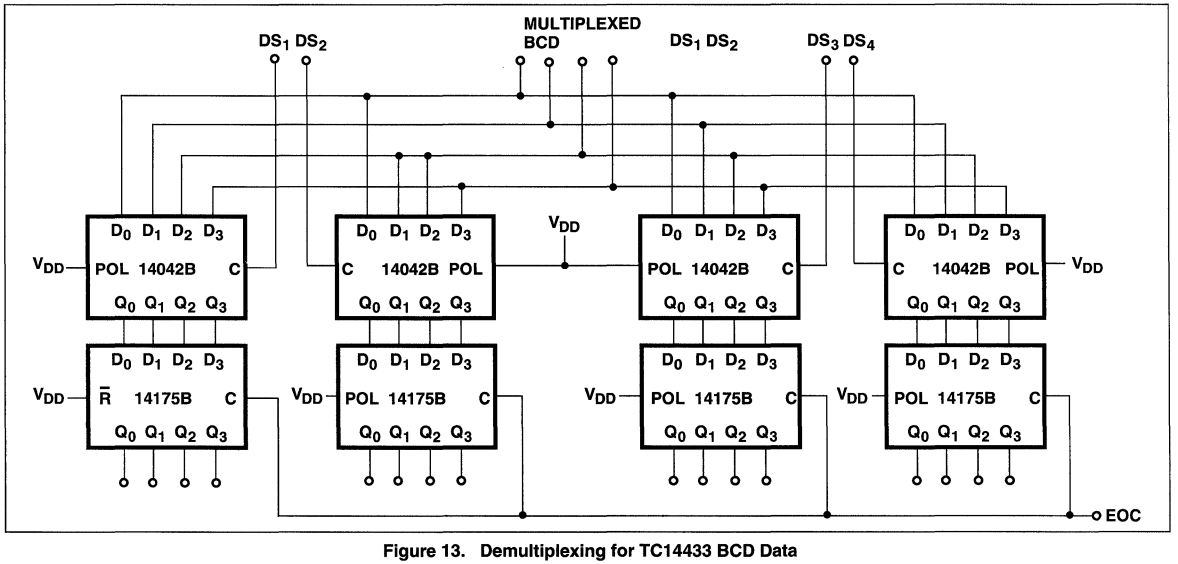


Figure 13. Demultiplexing for TC14433 BCD Data

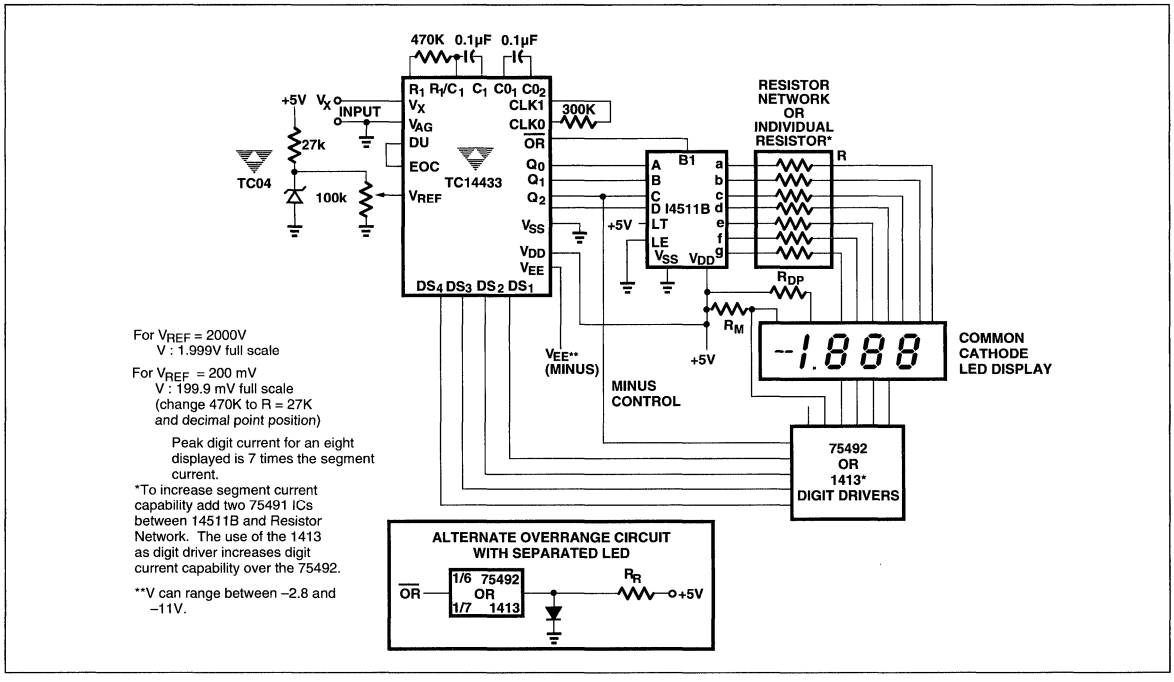


Figure 14. 3-1/2 Digit Voltmeter with Low Component Count Using Common Cathode Displays

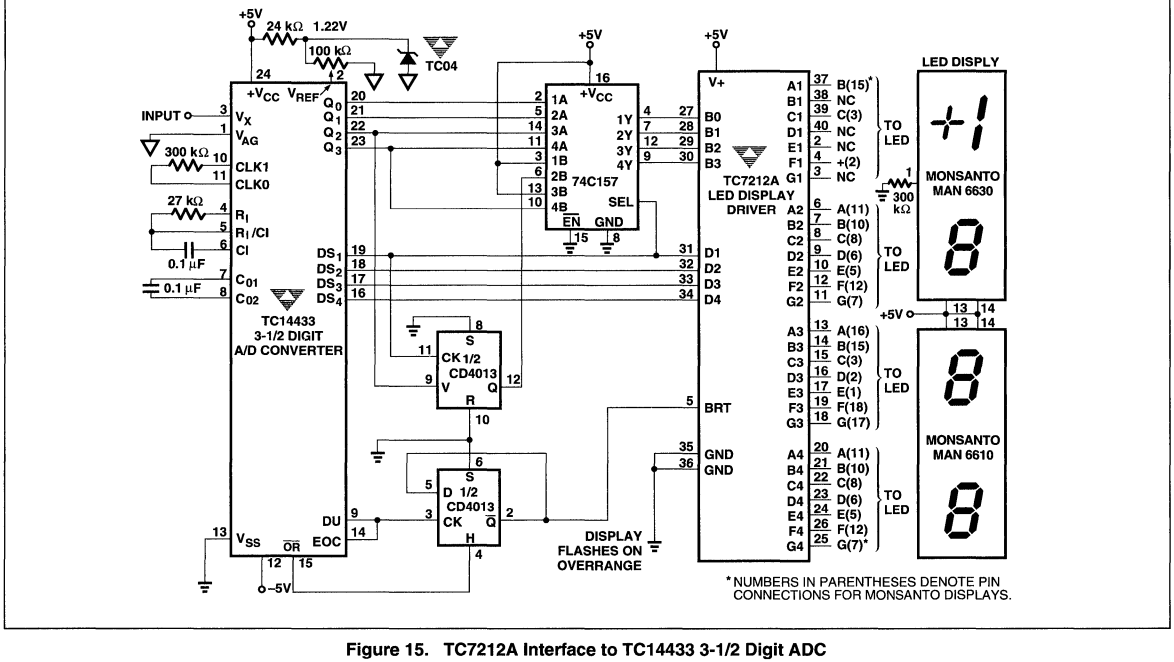


Figure 15. TC7212A Interface to TC14433 3-1/2 Digit ADC

VOLTAGE-TO-FREQUENCY/FREQUENCY-TO-VOLTAGE CONVERTERS

FEATURES

Voltage-to-Frequency

- **Choice of Guaranteed Linearity:**
  - **TC9401 ..... 0.01%**
  - **TC9400 ..... 0.05%**
  - **TC9402 ..... 0.25%**
- **DC to 100 kHz (F/V) or 1Hz to 100 kHz (V/F)**
- **Low Power Dissipation ..... 27 mW Typ**
- **Single/Dual Supply Operation ..... + 8V to + 15V or ± 4V to ± 7.5V**
- **Gain Temperature Stability ..... ± 25 ppm/°C Typ**
- **Programmable Scale Factor**

Frequency-to-Voltage

- **Operation ..... DC to 100 kHz**
- **Choice of Guaranteed Linearity:**
  - **TC9401 ..... 0.02%**
  - **TC9400 ..... 0.05%**
  - **TC9402 ..... 0.25%**
- **Programmable Scale Factor**

APPLICATIONS

- **µP Data Acquisition**
- **13-Bit Analog-to-Digital Converters**
- **Analog Data Transmission and Recording**
- **Phase-Locked Loops**
- **Frequency Meters/Tachometer**
- **Motor Control**
- **FM Demodulation**

GENERAL DESCRIPTION

The TC9400/TC9401/TC9402 are low-cost voltage-to-frequency (V/F) converters utilizing low power CMOS technology. The converters accept a variable analog input signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.

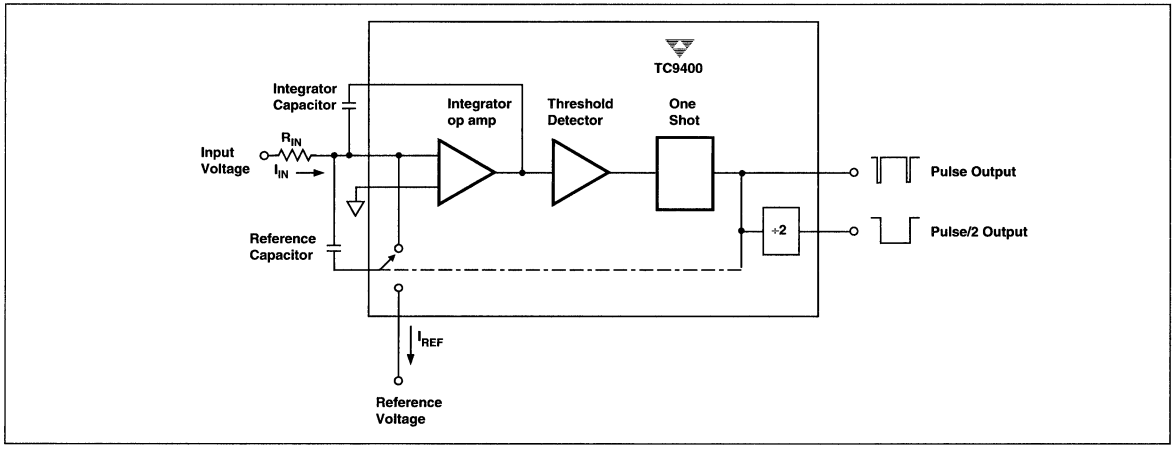
The devices can also be used as highly-accurate frequency-to-voltage (F/V) converters, accepting virtually any input frequency waveform and providing a linearly-proportional voltage output.

A complete V/F or F/V system only requires the addition of two capacitors, three resistors, and reference voltage.

ORDERING INFORMATION

Part No.	Linearity (V/F)	Package	Temperature Range
TC9400CPD	0.05%	14-Pin Plastic DIP	0°C to +70°C
TC9400EJD	0.05%	14-Pin CerDIP	– 40°C to +85°C
TC9400COD	0.05%	14-Pin SO	0°C to +70°C
TC9401CPD	0.01%	14-Pin Plastic DIP	0°C to +70°C
TC9401EJD	0.01%	14-Pin CerDIP	– 40°C to +85°C
TC9402CPD	0.25%	14-Pin Plastic DIP	0°C to +70°C
TC9402EJD	0.25%	14-Pin CerDIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC9400
TC9401
TC9402

VOLTAGE-TO-FREQUENCY/ FREQUENCY-TO-VOLTAGE CONVERTERS

ABSOLUTE MAXIMUM RATINGS*

$V_{DD} - V_{SS}$ ..... +18V
I_{IN} ..... 10 mA
V_{OUT} Max $-V_{OUT}$ Common 23V
$V_{REF} - V_{SS}$ ..... – 1.5V

Storage Temperature Range ..... – 65°C to +150°C
Operating Temperature Range
C Device ..... 0°C to +70°C
E Device ..... – 40°C to +85°C
Package Dissipation ..... 500 mW
Lead Temperature (Soldering, 10 sec) ..... +300°C

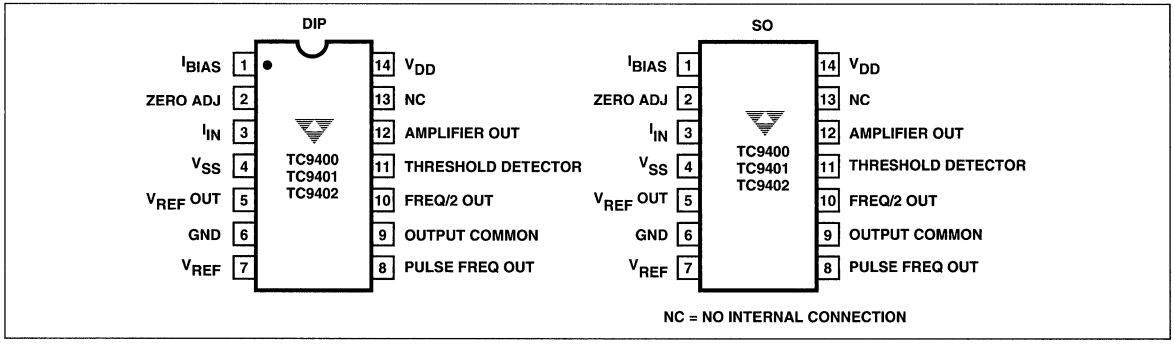
ELECTRICAL CHARACTERISTICS: V_{DD} = +5V, V_{SS} = – 5V, V_{GND} = 0V, V_{REF} = – 5V, R_{BIAS} = 100 kΩ, Full Scale =10 kHz, unless otherwise specified. T_A = +25°C, unless temperature range is specified (– 40°C to +85°C for E device, 0°C to +70°C for C device).

VOLTAGE-TO-FREQUENCY		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Accuracy											
Linearity 10 kHz	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input		0.004	0.01		0.01	0.05		0.05	0.25	% Full Scale
Linearity 100 kHz	Output Deviation From Straight Line Between Normalized Zero Reading and Full-Scale Input		0.04	0.08		0.1	0.25		0.25	0.5	% Full Scale
Gain Temperature Drift (Note 1)	Variation in Gain A Due to Temperature Change		± 25	± 40		± 25	± 40		± 50	± 100	ppm/°C Full Scale
Gain Variance	Variation From Ideal Accuracy		± 10			± 10			± 10		% of Nominal
Zero Offset (Note 2)	Correction at Zero Adjust for Zero Output When Input is Zero		± 10	± 50		± 10	± 50		± 20	± 100	mV
Zero Temperature Drift (Note 1)	Variation in Zero Offset Due to Temperature Change		± 25	± 50		± 25	± 50		± 50	± 100	µV/°C
Analog Input											
I_{IN} Full Scale	Full-Scale Analog Input Current to Achieve Specified Accuracy		10			10			10		µA
I_{IN} Overrange	Overrange Current			50			50			50	µA
Response Time	Settling Time to 0.1% Full Scale		2			2			2		Cycle
Digital Section											
V_{SAT} @ I_{OL} = 10 mA (Note 3)	Logic "0" Output Voltage		0.2	0.4		0.2	0.4		0.2	0.4	V
V_{OUT} Max – V_{OUT} Common (Note 4)	Voltage Range Between Output and Common			18			18			18	V
Pulse Frequency Output Width			3			3			3		µs
Supply Current											
I_{DD} Quiescent (Note 5)	Current Required From Positive Supply During Operation		1.5	6		1.5	6		3	10	mA
I_{SS} Quiescent (Note 5)	Current Required From Negative Supply During Operation		– 1.5	– 6		– 1.5	– 6		– 3	– 10	mA
V_{DD} Supply	Operating Range of Positive Supply	4		7.5	4		7.5	4		7.5	V
V_{SS} Supply	Operating Range of Negative Supply	– 4		– 7.5	– 4		– 7.5	– 4		– 7.5	V
Reference Voltage											
$V_{REF} - V_{SS}$	Range of Voltage Reference Input	– 2.5			– 2.5			– 2.5			V

NOTES:
1. Full temperature range. Guaranteed, Not Tested.
2. I_{IN} = 0.
3. Full temperature range, I_{OUT} = 10 mA.
4. I_{OUT} = 10 µA.
5. Threshold Detect = 5V, Amp Out = 0V, Full Temperature Range

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

PIN#	SYMBOL	DESCRIPTION
1	**I_{BIAS}**	This pin sets bias current in the TC9400. Connect to V_{SS} through a 100 kΩ resistor. See text.
2	**Zero Adj**	Low frequency adjustment input. See text.
3	**I_{IN}**	Input current connection for the V/F converter.
4	**V_{SS}**	Negative power supply voltage connection, typically –5V.
5	**V_{REF}OUT**	Reference capacitor connection.
6	**GND**	Analog ground.
7	**V_{REF}**	Voltage reference input, typically –5V.
8	**Pulse Freq Out**	Frequency output. This open drain output will pulse LOW each time the Freq threshold detector limit is reached. The pulse rate is proportional to input voltage.
9	**Output Common**	Source connection for the open drain output FETs. See text.
10	**Freq/2 Out**	This open drain output is a square wave at one half the frequency of the pulse output (pin 8). Output transitions of this pin occur on the rising edge of pin 8.
11	**Threshold Detect**	Input to the threshold detector. This pin is the frequency input during F/V operation.
12	**Amplifier Out**	Output of the integrator amplifier.
13	**NC**	No internal connection
14	**V_{DD}**	Positive power supply connection, typically +5V.

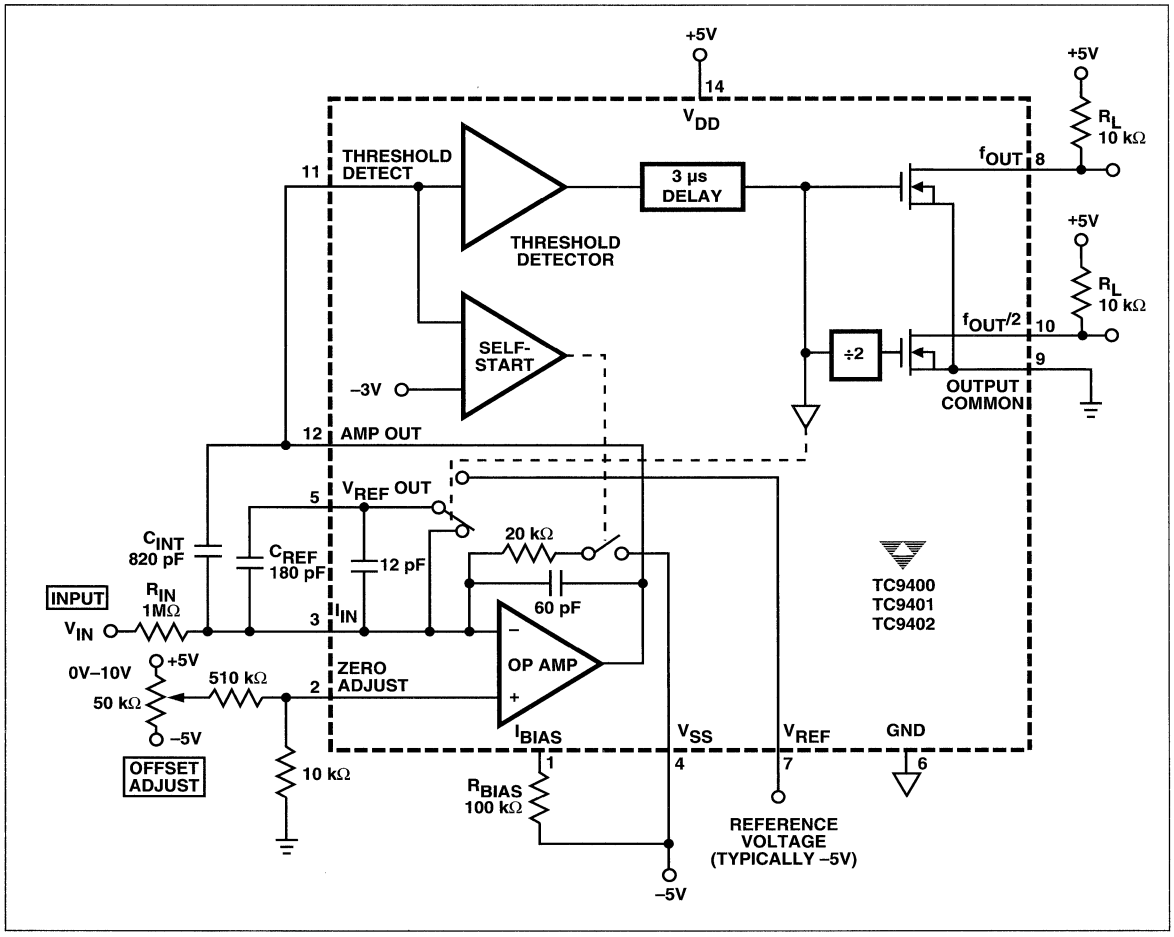
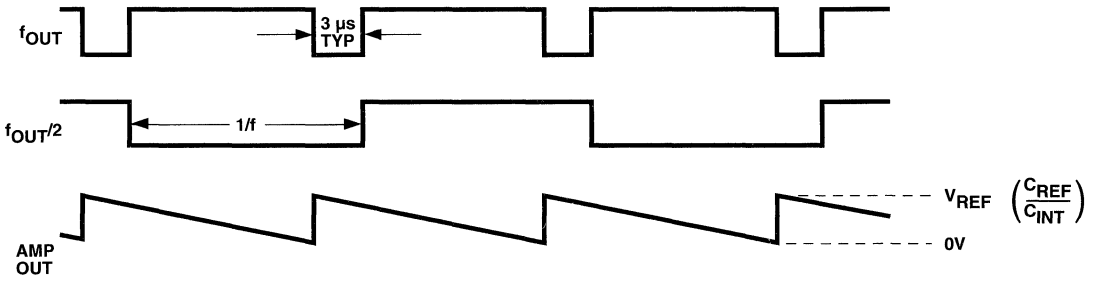


Figure 1 10 Hz to 10 kHz V/F Converter

VOLTAGE-TO-FREQUENCY (V/F) CIRCUIT DESCRIPTION

The TC9400 V/F converter operates on the principal of charge balancing. The operation of the TC9400 is easily understood by referring to Figure 1. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge on the integrating capacitor and shows up as a linearly decreasing voltage at the output of the Op Amp. The lower limit of the output swing is set by the threshold detector, which causes the reference voltage to be applied to the reference capacitor for a time period long enough to charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$), causing the Op Amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out. This dissipates the charge stored on the reference capacitor, so that when the output again crosses zero the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases, which causes the output frequency to also increase. Since each charge increment is fixed, the increase in frequency with voltage is linear. In addition, the accuracy of the output pulse width does not directly affect the linearity of the V/F. The pulse must simply be long enough for full charge transfer to take place.



NOTES: 1. To adjust f_{MIN}, set V_{IN} = 10 mV and adjust the 50 kΩ offset for 10 Hz output.
2. To adjust f_{MAX}, set V_{IN} = 10V and adjust R_{IN} or V_{REF} for 10 kHz output.
3. To increase f_{OUT} MAX to 100 kHz, change C_{REF} to 27 pF and C_{INT} to 75 pF.
4. For high-performance applications, use high-stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass capacitors). Also, separate output ground (pin 9) from input ground (pin 6).

Figure 2 Output Waveforms

The TC9400 contains a "self-start" circuit to ensure the V/F converter always operates properly when power is first applied. In the event that, during power-on, the Op-Amp output is below the threshold and C_{REF} is already charged, a positive voltage step will not occur. The Op-Amp output will continue to decrease until it crosses the –3.0V threshold of the "self-start" comparator. When this happens, an internal resistor is connected to the Op-Amp input, which forces the output to go positive until the TC9400 is in its normal operating mode.

The TC9400 utilizes low power CMOS processing for low input bias and offset currents with very low power dissipation. The open-drain N-channel output FETs provide high voltage and high current sink capability.

VOLTAGE-TO-TIME MEASUREMENTS

The TC9400 output can be measured in the time domain as well as the frequency domain. Some microcomputers, for example, have extensive timing capability but limited counter capability. Also, the response time of a time domain measurement is only the period between two output pulses, while the frequency measurement must accumulate pulses during the entire counter timebase period.

Time measurements can be made from either the TC9400's Pulse Freq Out output or from the Freq/2 output. The Freq/2 output changes state on the rising edge of Pulse Freq Out, so Freq/2 is a symmetrical square wave at one half the pulse output frequency. Timing measurements can therefore be made between successive Pulse Freq Out pulses, or while Freq/2 is high (or low).

PIN FUNCTIONS

Threshold Detector Input

In the V/F mode, this input is connected to the amplifier output (pin 12) and triggers a 3 µs pulse when the input voltage passes through its threshold. In the F/V mode, the input frequency is applied to this input.

The nominal threshold of the detector is halfway between the power supplies, or $(V_{DD} + V_{SS})/2 \pm 400$ mV. The TC9400's charge balancing V/F technique is not dependent on a precision comparator threshold, because the threshold only sets the lower limit of the Op-Amp output. The Op-Amp's peak-to-peak output swing, which determines the frequency, is only influenced by external capacitors and by V_{REF}.

Pulse Freq Out

This output is an open-drain N-channel FET which provides a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Freq/2 Out

This output is an open-drain N-channel FET which provides a square wave one-half the frequency of the pulse frequency output. The Freq/2 output will change state on the rising edge of Pulse Freq Out. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common

The sources of both the Freq/2 out and the Pulse Freq Out are connected to this pin. An output level swing from the drain voltage to ground or to the V_{SS} supply may be obtained by connecting this pin to the appropriate point.

R_{BIAS}

An external resistor, connected to V_{SS}, sets the bias point for the TC9400. Specifications for the TC9400 are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted.

Increasing the maximum frequency of the TC9400 beyond 100 kHz is limited by the pulse width of the Pulse Output (typically 3μs). Reducing R_{BIAS} will decrease the pulse width and increase the maximum operating frequency, but linearity errors will also increase. R_{BIAS} can be reduced to 20 kΩ, which will typically produce a maximum full scale frequency of 500 kHz.

Amplifier Out

The output stage of the operational amplifier. During V/F operation, a negative-going ramp signal is available at this pin. In the F/V mode, a voltage proportional to the frequency input is generated.

Zero Adjust

This pin is the noninverting input of the operational amplifier. The low-frequency set point is determined by adjusting the voltage at this pin.

I_{IN}

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10 μA is specified, but an overrange current up to 50 μA can be used without detrimental effect to the circuit operation. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly, but must be buffered by external resistors.

V_{REF}

A reference voltage from either a precision source or the V_{SS} supply is applied to this pin. Accuracy of the TC9400 is dependent on the voltage regulation and temperature characteristics of the reference circuitry.

Since the TC9400 is a charge balancing V/F converter, the reference current will be equal to the input current. For this reason, the DC impedance of the reference voltage source must be kept low enough to prevent linearity errors. For linearity of 0.01%, a reference impedance of 200Ω or less is recommended. A 0.1 μF bypass capacitor should be connected from V_{REF} to ground.

V_{REF} Out

The charging current for C_{REF} is supplied through this pin. When the Op-Amp output reaches the threshold level, this pin is internally connected to the reference voltage and a charge, equal to V_{REF} x C_{REF}, is removed from the integrator capacitor. After about 3 μs, this pin is internally connected to the summing junction of the Op-Amp to discharge C_{REF}. Break-before-make switching ensures that the reference voltage is not directly applied to the summing junction.

V/F CONVERTER DESIGN INFORMATION

Input/Output Relationships

The output frequency (f_{OUT}) is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})\,(C_{REF})}$$

External Component Selection

R_{IN}

The value of this component is chosen to give a full-scale input current of approximately 10 μA:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full Scale}}{10\ \mu A}.$$

Example: $R_{IN} \cong \frac{10V}{10\ \mu A} = 1\ M\Omega.$

Note that the value is an approximation and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full-scale frequency at V_{IN} full scale (see "Adjustment Procedure"). Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

C_{INT}

The exact value is not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \leq C_{INT} \leq 10\ C_{REF}.$$

Improved stability and linearity are obtained when $C_{INT} \leq 4C_{REF}$. Low-leakage types are recommended, although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 13.

C_{REF}

The exact value is not critical and may be used to trim the full-scale frequency (see "Input/Output Relationships"). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended. For high-accuracy requirements, 0.05% line and load regulation and 0.1 µF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure

Figure 1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure for a 10 kHz full-scale frequency is as follows:

(1) Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10 Hz output frequency.

(2) Set V_{IN} to 10V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10 kHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

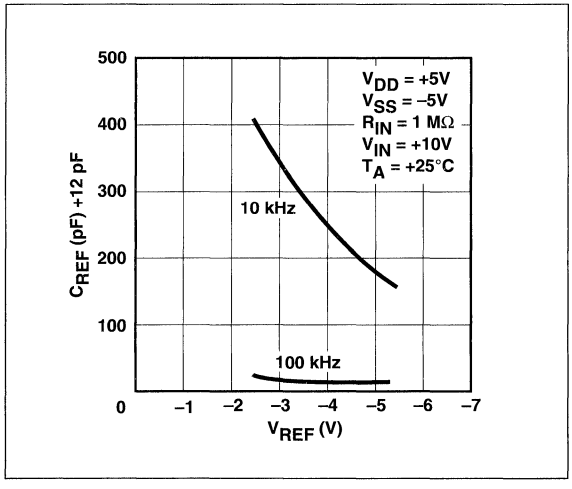


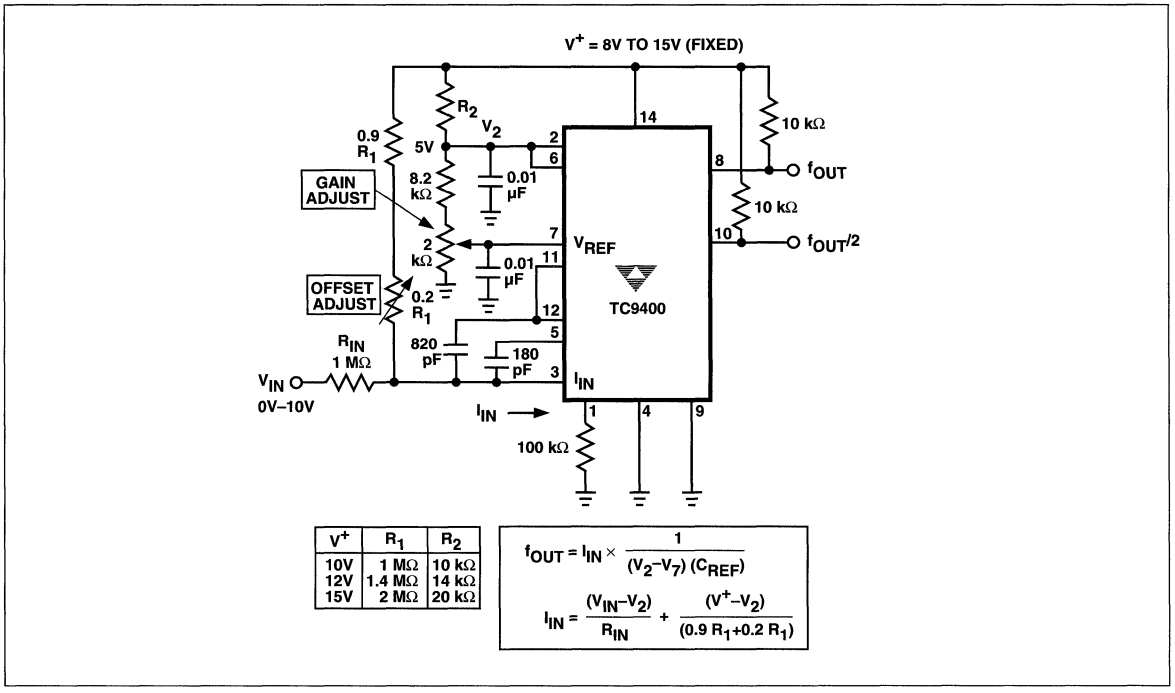
Figure 3 Recommended C_{REF} vs V_{REF}

Improved Single Supply V/F Converter Operation

A TC9400 which operates from a single 12 to 15V variable power source is shown in Figure 5. This circuit uses two Zener diodes to set stable biasing levels for the TC9400. The Zener diodes also provide the reference voltage, so the output impedance and temperature coefficient of the Zeners will directly affect power supply rejection and temperature performance.

Full scale adjustment is accomplished by trimming the input current. Trimming the reference voltage is not recommended for high accuracy applications unless an Op Amp is used as a buffer, because the TC9400 requires a low impedance reference (see the V_{REF} pin description section for more information).

The circuit of Figure 5 will directly interface with CMOS logic operating at 12V to 15V. TTL or 5V CMOS logic can be accommodated by connecting the output pullup resistors to the +5V supply. An optoisolator can also be used if an isolated output is required.

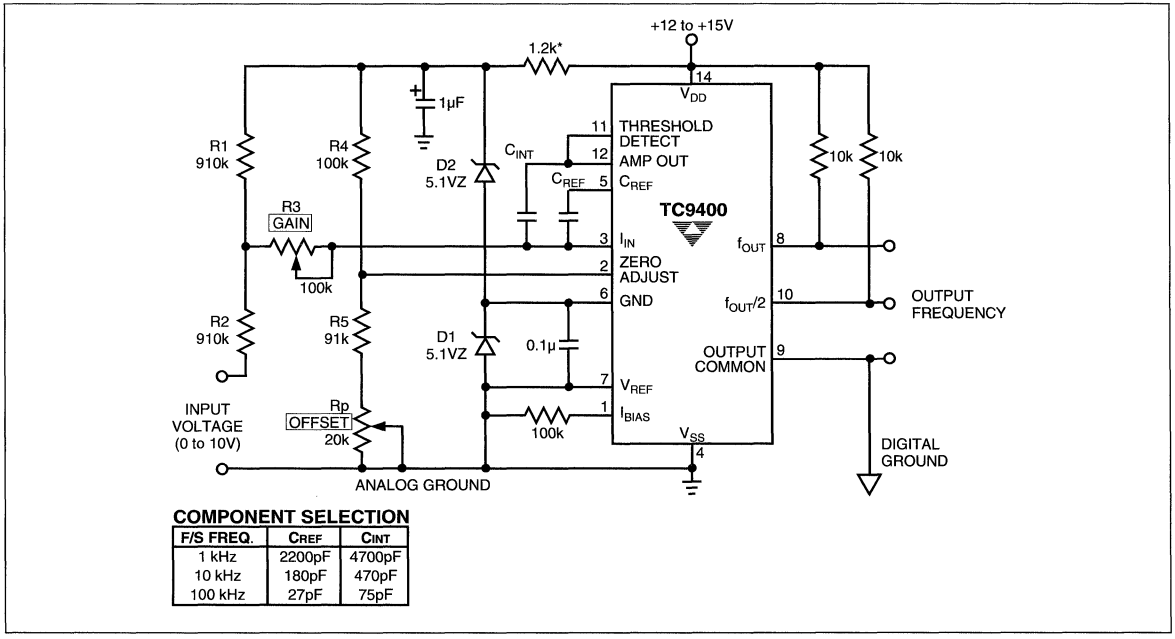


V+	R1	R2
10V	1 MΩ	10 kΩ
12V	1.4 MΩ	14 kΩ
15V	2 MΩ	20 kΩ

$$f_{OUT} = I_{IN} \times \frac{1}{(V_2 - V_7)(C_{REF})}$$

$$I_{IN} = \frac{(V_{IN} - V_2)}{R_{IN}} + \frac{(V^+ - V_2)}{(0.9\,R_1 + 0.2\,R_1)}$$

Figure 4 Fixed Voltage — Single Supply Operation



COMPONENT SELECTION

F/S FREQ.	CREF	CINT
1 kHz	2200pF	4700pF
10 kHz	180pF	470pF
100 kHz	27pF	75pF

Figure 5 Voltage to Frequency

ELECTRICAL CHARACTERISTICS:

V_{DD} = +5V, V_{SS} = – 5V, V_{GND} = 0, V_{REF} = –5V, R_{BIAS} = 100 kΩ, Full Scale = 10 kHz, unless otherwise specified. T_A = +25°C, unless temperature range is specified – 40°C to +85°C for E device, 0°C to +70°C for C device.

FREQUENCY-TO-VOLTAGE		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Accuracy											
Nonlinearity (Note 1)	Deviation From Ideal Transfer Function as a Percentage Full-Scale Voltage		0.01	0.02		0.02	0.05		0.05	0.25	% Full Scale
Input Frequency Range (Note 2 and 3)	Frequency Range for Specified Nonlinearity	10		100k	10		100k	10		100k	Hz
Frequency Input											
Positive Excursion	Voltage Required to Turn Threshold Detector On	0.4		V_{DD}	0.4		V_{DD}	0.4		V_{DD}	V
Negative Excursion	Voltage Required to Turn Threshold Detector Off	– 0.4		– 2	– 0.4		– 2	– 0.4		– 2	V
Minimum Positive Pulse Width (Note 3)	Time Between Threshold Crossings		5			5			5		µs
Minimum Negative Pulse Width (Note 3)	Time Between Threshold Crossings		0.5			0.5			0.5		µS
Input Impedance			10			10			10		MΩ
Analog Outputs											
Output Voltage (Note 4)	Voltage Range of Op Amp Output for Specified Nonlinearity		V_{DD} – 1			V_{DD} – 1			V_{DD} – 1		V
Output Loading	Resistive Loading at Output of Op Amp	2			2			2			kΩ
Supply Current											
I_{DD} Quiescent (Note 5)	Current Required From Positive Supply During Operation		1.5	6		1.5	6		3	10	mA
I_{SS} Quiescent (Note 5)	Current Required From Negative Supply During Operation		– 1.5	– 6		– 1.5	– 6		– 3	– 10	mA
V_{DD} Supply	Operating Range of Positive Supply	4		7.5	4		7.5	4		7.5	V
V_{SS} Supply	Operating Range of Negative Supply	– 4		– 7.5	– 4		– 7.5	– 4		– 7.5	V
Reference Voltage											
V_{REF} – V_{SS}	Range of Voltage Reference Input	– 2.5			– 2.5			– 2.5			V

NOTES:
1. 10 Hz to 100 kHz.; Guaranteed, Not Tested
2. 5 µs minimum positive pulse width and 0.5 µs minimum negative pulse width.
3. $t_R = t_F$ = 20 ns.
4. $R_L \geq 2$ kΩ.; Tested @ 10kΩ
5. Full temperature range, V_{IN} = –0.1V.

FREQUENCY-TO-VOLTAGE (F/V) CIRCUIT DESCRIPTION

When used as an F/V converter, the TC9400 generates an output voltage linearly proportional to the input frequency waveform.

Each zero crossing at the threshold detector's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor, generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

F/V CONVERTER DESIGN INFORMATION

Input/Output Relationships

The output voltage is related to the input frequency (f_{IN}) by the transfer equation:

$$V_{OUT} = [V_{REF}\ C_{REF}\ R_{INT}]\ f_{IN}.$$

The response time to a change in f_{IN} is equal to (R_{INT} C_{INT}). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the input frequency.

C_{INT} can be increased to lower the ripple. Values of 1 µF to 100 µF are perfectly acceptable for low frequencies.

When the TC9400 is used in the single-supply mode, V_{REF} is defined as the voltage difference between pin 7 and pin 2.

Input Voltage Levels

The input frequency is applied to the Threshold Detector input (Pin 11). As discussed in the V/F circuit section of this data sheet, the threshold of pin 11 is approximately (V_{DD} + V_{SS}) /2 ±400mV. Pin 11's input voltage range extends from V_{DD} to about 2.5 V below the threshold. If the voltage on pin 11 goes more than 2.5 volts below the threshold, the V/F mode startup comparator will turn on and corrupt the output voltage. The Threshold Detector input has about 200 mV of hysteresis.

In ±5 V applications, the input voltage levels for the TC9400 are ±400mV, minimum. If the frequency source being measured is unipolar, such as TTL or CMOS operating from a +5V source, then an AC coupled level shifter should be used. One such circuit is shown in Figure 6a.

The level shifter circuit in Figure 6b can be used in single supply F/V applications. The resistor divider ensures that the input threshold will track the supply voltages. The diode clamp prevents the input from going far enough in the negative direction to turn on the startup comparator. The diode's forward voltage decreases by 2.1 mV/°C, so for high ambient temperature operation two diodes in series are recommended.

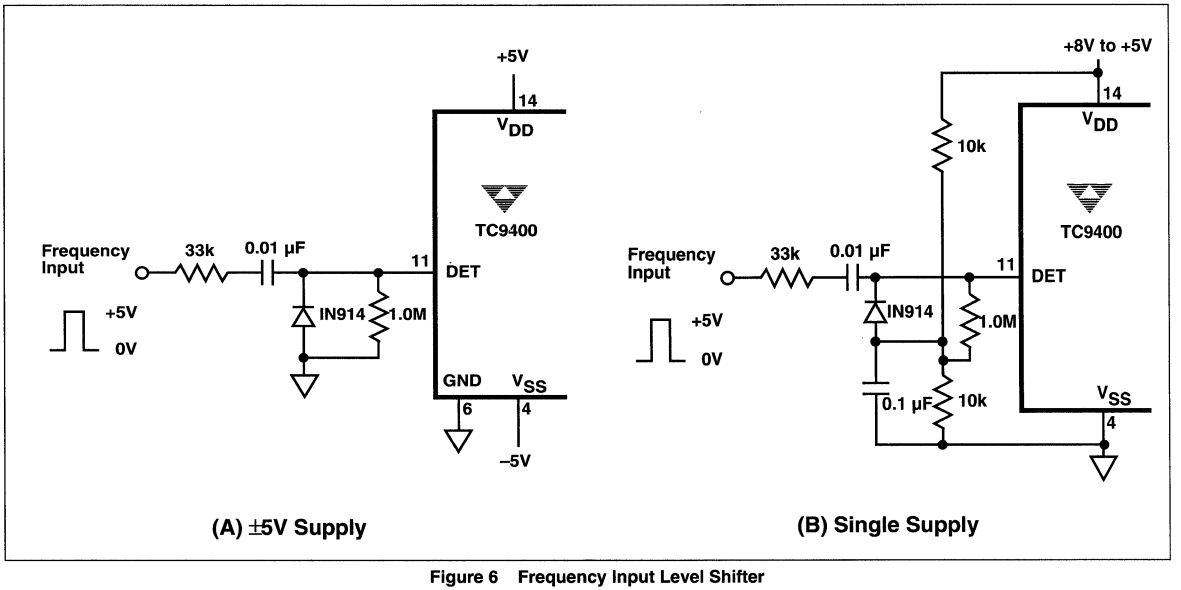


Figure 6 Frequency Input Level Shifter

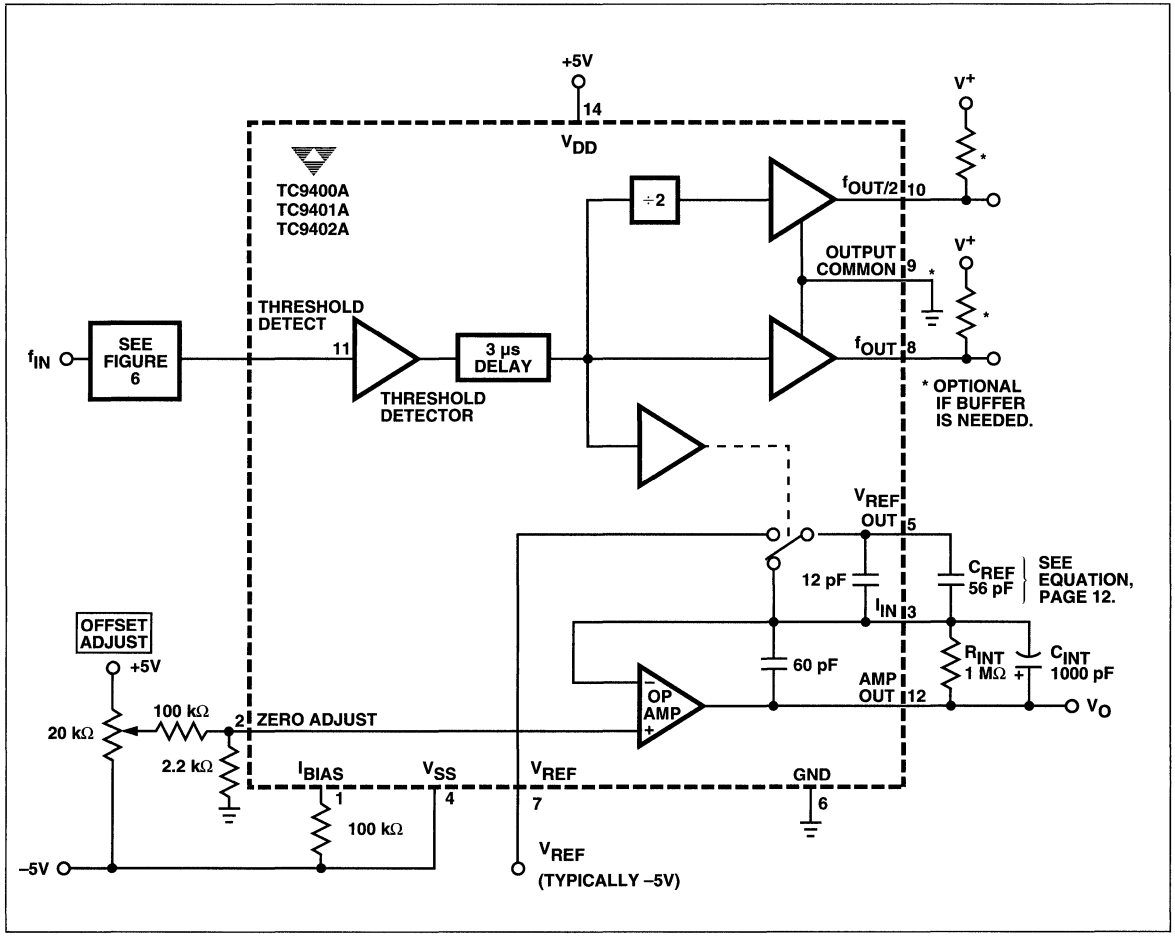


Figure 7 DC — 10 kHz F/V Converter

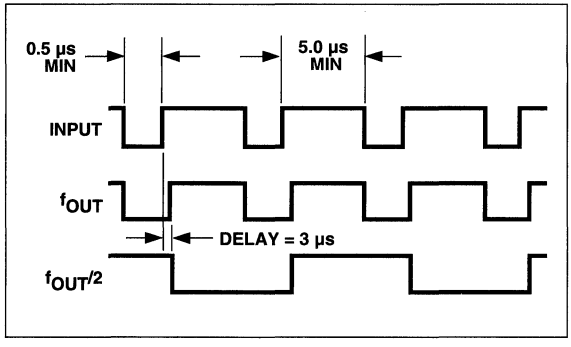
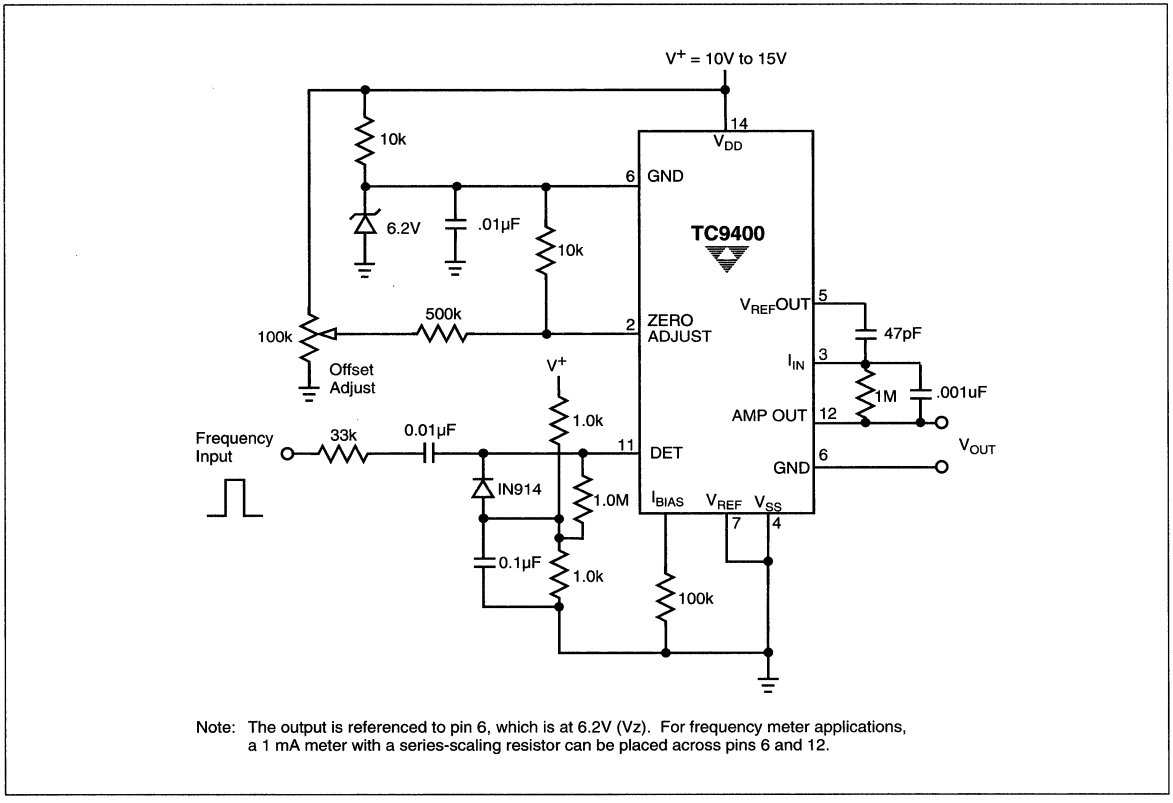


Figure 8 F/V Digital Outputs

Input Buffer

f_{OUT} and $f_{OUT}/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. Then, f_{OUT} will follow the input frequency waveform, except that f_{OUT} will go high 3 µs after f_{IN} goes high; $f_{OUT}/2$ will be squarewave with a frequency of one-half f_{OUT}.

If these outputs are not used, pins 8, 9 and 10 should be connected to ground.



Note: The output is referenced to pin 6, which is at 6.2V (Vz). For frequency meter applications, a 1 mA meter with a series-scaling resistor can be placed across pins 6 and 12.

Figure 9 F/V Single Supply F/V Converter

Output Filtering

The output of the TC9400 has a sawtooth ripple superimposed on a DC level. The ripple will be rejected if the TC9400 output is converted to a digital value by an integrating analog to digital converter, such as the TC7107 or TC7109. The ripple can also be reduced by increasing the value of the integrating capacitor, although this will reduce the response time of the F/V converter.

The sawtooth ripple on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit is a capacitance multiplier, where the output coupling capacitor is multiplied by the AC gain of the op amp. A moderately fast op amp, such as the TL071, should be used.

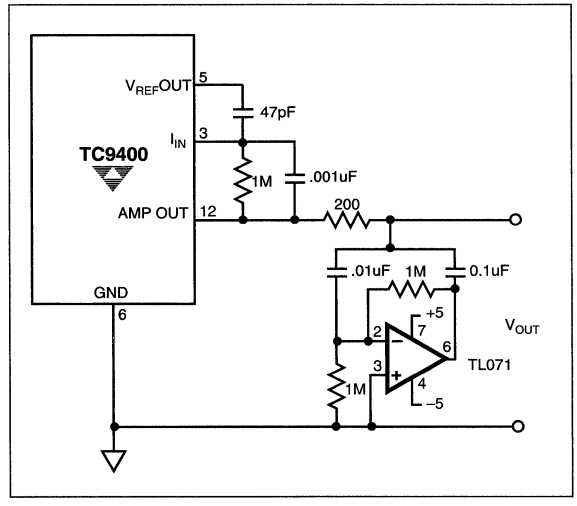


Figure 10 Ripple Filter

F/V POWER-ON RESET

In F/V mode, the TC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition remains until the first pulse is applied to f_{IN}. In most frequency-measurement applications this is not a problem, because proper operation begins as soon as the frequency input is applied.

In some cases, however, the TC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from pin 11 to V_{DD} will usually be sufficient to pulse the TC9400 and provide a power-on reset (see Figure 11A). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 11B, may be required.

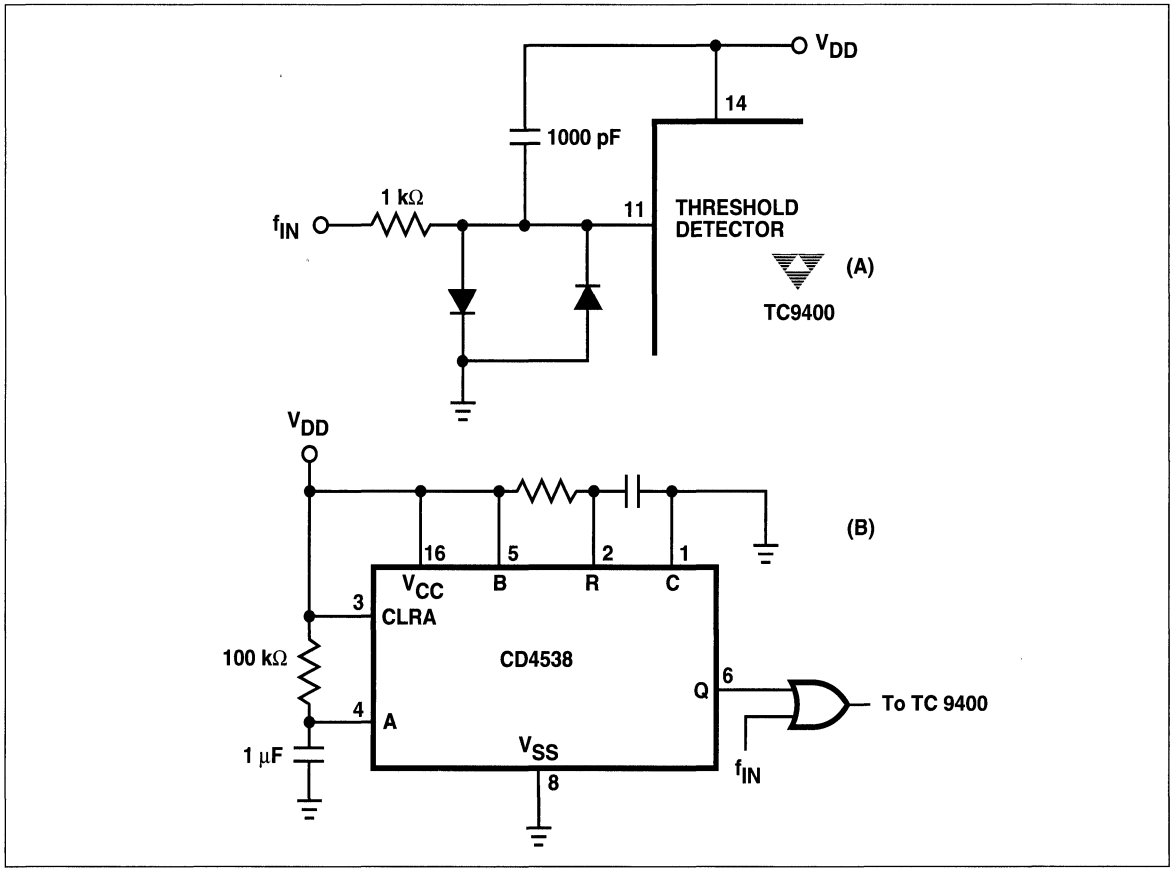


Figure 11 Power-On Operation/Reset

LOW POWER, BAND-GAP VOLTAGE REFERENCES

FEATURES

- **Temperature Coefficient ..... 50 ppm/°C**
- **Wide Operating Current Range**
  - **TC04 ..... 15 µA to 20 mA**
  - **TC05 ..... 20 µA to 20 mA**
- **Dynamic Impedance 1Ω**
- **Output Tolerance 2%**
- **Output Voltage Option**
  - **TC04 ..... 1.25V**
  - **TC05 ..... 2.5V**
- **TO-92 Plastic or TO-52 Hermetic Packages**
- **8-Pin Plastic Small Outline (SO) Package**

APPLICATIONS

- **ADC and DAC Reference**
- **Current Source Generation**
- **Threshold Detectors**
- **Power Supplies**
- **Multimeters**

GENERAL DESCRIPTION

The TC04 (1.25V output) and TC05 (2.5V output) bipolar, two-terminal, band-gap voltage references offer precision performance without premium price. These devices do not require thin-film resistors, greatly lowering manufacturing complexity and cost.

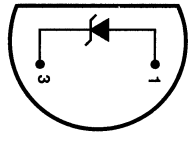
A 50 ppm/°C output temperature coefficient and 15 µA to 20 mA operating current range make these devices attractive for multimeter, data acquisition converter, and telecommunication voltage references.

ORDERING INFORMATION

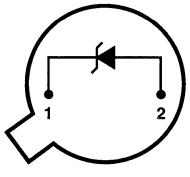
Voltage	Max Temperature Coefficient	Temperature Range: – 55°C to +125°C TO-52 Package	Temperature Range: 0°C to +70°C TO-92 Package	Temperature Range: 0°C to +70°C Surface Mount Package
1.25V	50 ppm/°C	TC04AMRM	TC04ACZM	TC04ACOA
1.25V	100 ppm°C	TC04BMRM	TC04BCZM	TC04BCOA
2.5V	50 ppm/°C	TC05AMRM	TC05ACZM	TC05ACOA
2.5V	100 ppm/°C	TC05BMRM	TC05BCZM	TC05BCOA

PIN CONFIGURATIONS

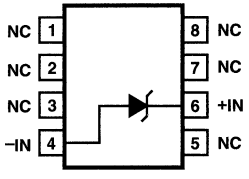
TC04
TC05



TO-92
PLASTIC PACKAGE
(BOTTOM VIEW)



TO-52
HERMETIC PACKAGE
(BOTTOM VIEW)



COA
PLASTIC PACKAGE

NC = NO INTERNAL CONNECTION

ABSOLUTE MAXIMUM RATINGS

Forward Current ..... +10 mA
Reverse Current ..... +30 mA
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
TO-92 Package ..... 0°C to +70°C
TO-52 Package ..... –55°C to +125°C
COA Surface Mount Package ..... 0°C to +70°C

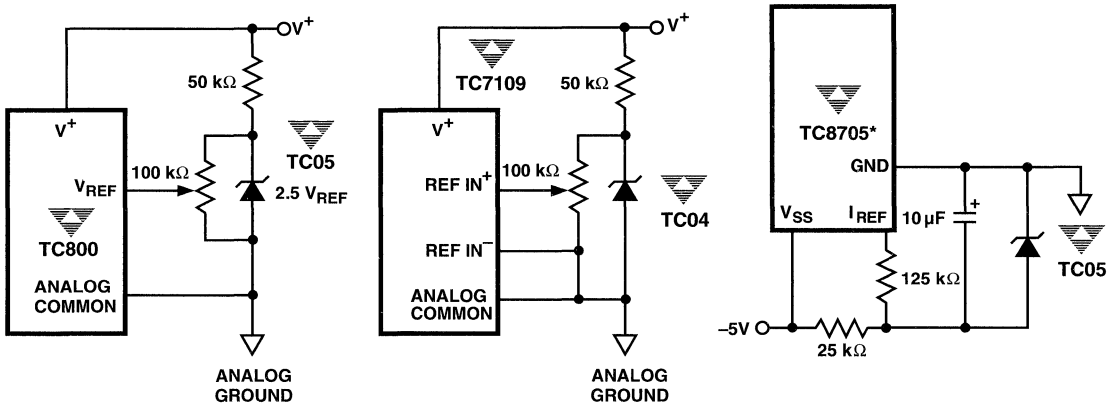
Lead Temperature (Soldering, 10 sec)
TO-92 Package ..... +260°C
TO-52 Package ..... +300°C
COA Surface Mount Package ..... +260°C
Power Dissipation ..... Limited by Forward/ Reverse Current

Functional operation above the absolute maximum stress ratings is not implied.

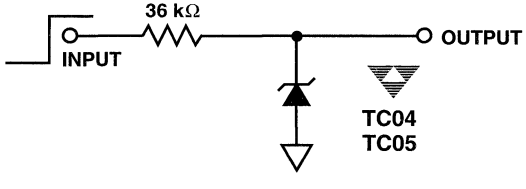
ELECTRICAL CHARACTERISTICS: T_A = +25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BR}	Reverse Breakdown Voltage	I_R = 100 µA				
	TC04		1.24	1.26	1.28	V
	TC05		2.45	2.50	2.60	V
DV_{BR}	Reverse Breakdown Voltage Change					
	TC04	15 µA < I_R < 20 mA	—	10	20	mV
		20 µA < I_R < 1 mA	—	0.25	1	mV
	TC05	20 µA < I_R < 20 mA	—	10	20	mV
		25 µA < I_R < 1 mA	—	0.25	1	mV
TC	Temperature Coefficient	I_R = 100 µA				
	TC04A/TC05A		—	0.003	0.005	%/°C
	TC04B/TC05B		—	0.003	0.01	%/°C
I_R	Reverse Current					
	TC04		0.015	—	20	mA
	TC05		0.020	—	20	mA

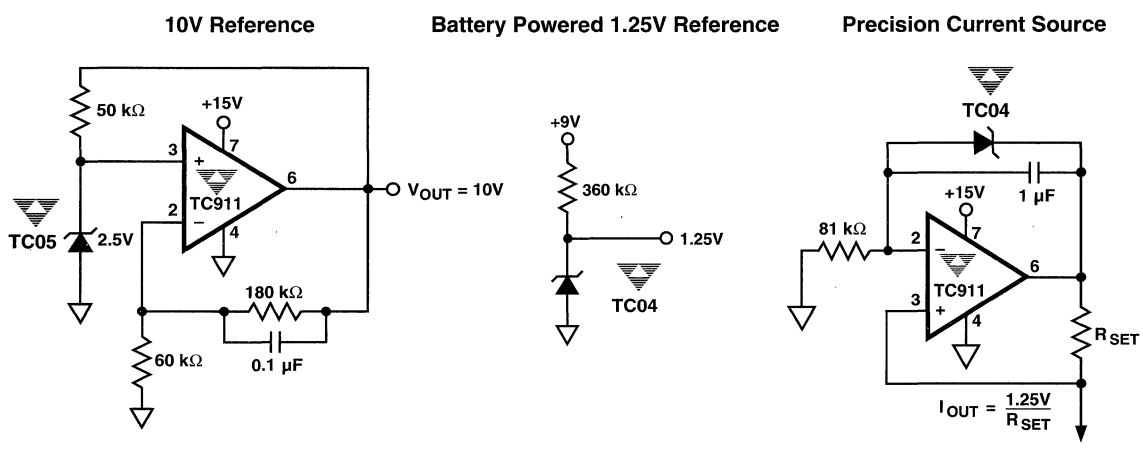
VOLTAGE REFERENCE CIRCUITS FOR SYSTEM DATA CONVERTERS



RESPONSE TIME TEST CIRCUIT

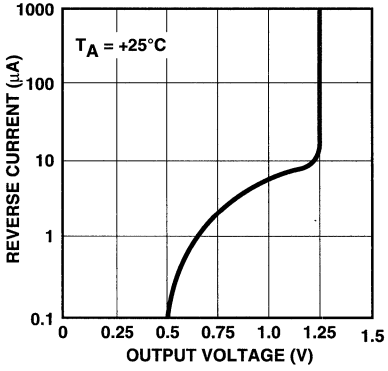


TYPICAL APPLICATIONS

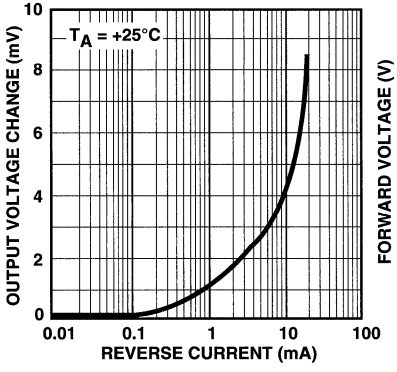


TYPICAL CHARACTERISTICS CURVES

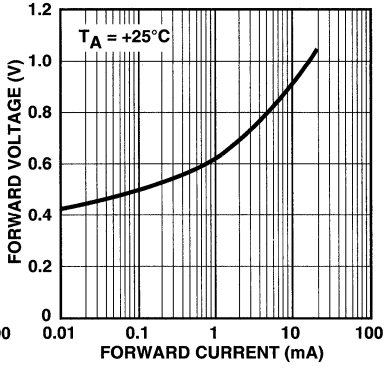
TC04: Output Voltage vs Reverse Current



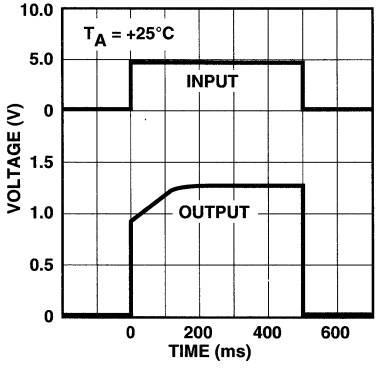
TC04: Output Voltage Change vs Reverse Current



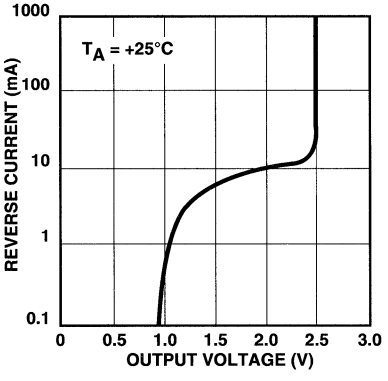
TC04: Forward Voltage vs Forward Current



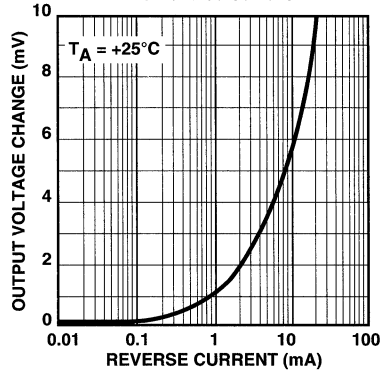
TC04
Response Time



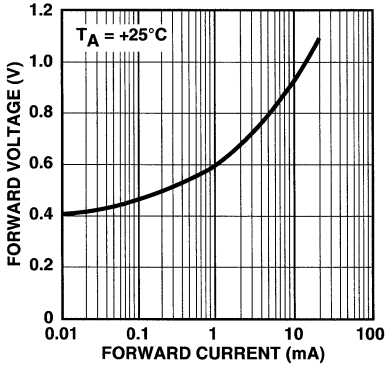
TC05: Output Voltage vs Reverse Current



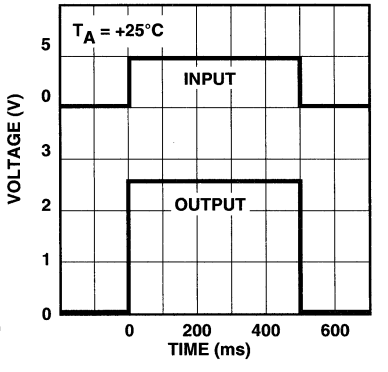
TC05: Output Voltage Change vs Reverse Current



TC05: Forward Voltage vs Forward Current



TC05
Response Time



LOW POWER, BAND-GAP VOLTAGE REFERENCES

FEATURES

- **Output Tolerance ..... 1 or 2%**
- **Output Voltage Option**
  - **LM285/385-1.2V 1.235V**
  - **LM285/385-2.5V 2.5V**
- **Wide Operating Current Range**
  - **LM285/385-1.2V ..... 15 µA to 20 mA**
  - **LM285/385-2.5V ..... 20 µA to 20 mA**
- **Temperature Coefficient ..... 30 ppm/°C**
- **Dynamic Impedance 0.6Ω**
- **TO-92 Plastic Package**
- **8-Pin Plastic Small Outline (SO) Package**

APPLICATIONS

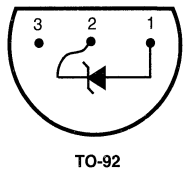
- **ADC and DAC Reference**
- **Current Source Generation**
- **Threshold Detectors**
- **Power Supplies**
- **Multi-meters**

GENERAL DESCRIPTION

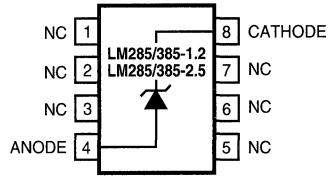
The LM285/385-1.2V (1.235V output) and LM285/385-2.5V (2.5V output) are bipolar, two-terminal, band-gap voltage references that offer precision performance without premium price. These devices do not require thin-film resistors, greatly lowering manufacturing complexity and cost.

A 30 ppm/°C output temperature coefficient and a 15 µA to 20 mA operating current range make these voltage references especially attractive for multimeter, data acquisition and telecommunications applications.

PIN CONFIGURATIONS



TO-92
PLASTIC PACKAGE
(BOTTOM VIEW)



SURFACE MOUNT
PLASTIC PACKAGE

NC = NO INTERNAL CONNECTION

ORDERING INFORMATION

		Temperature Range			
Voltage	Tolerance	0°C to +70°C TO-92 Package	0°C to +70°C Surface Mount Package	– 40°C to +85°C TO-92 Package	– 40°C to +85°C Surface Mount Package
1.2	1%	LM385BCZB-1.2	LM385BCOA-1.2	LM285BEZB-1.2	LM285BEOA-1.2
1.2	2%	LM385CZB-1.2	LM385COA-1.2	LM285EZB-1.2	LM285EOA-1.2
2.5	1.5%	LM385BCZB-2.5	LM385BCOA-2.5	LM285BEZB-2.5	LM285BEOA-2.5
2.5	3%	LM385CZB-2.5	LM385COA-2.5	LM285EZB-2.5	LM285EOA-2.5

LM285/385-1.2V
LM285/385-2.5V

ABSOLUTE MAXIMUM RATINGS

Forward Current ..... +10 mA
Reverse Current ..... +30 mA
Storage Temperature Range ..... – 65°C to +150°C
Operating Temperature Range
TO-92 Package ..... – 40°C to +85°C
COA Surface Mount Package ..... – 40°C to +85°C
Lead Temperature (Soldering, 10 sec)
TO-92 Package ..... +260°C
COA Surface Mount Package ..... +260°C
Power Dissipation
Limited by Forward/Reverse Current

Functional operation above the absolute maximum stress ratings is not implied.

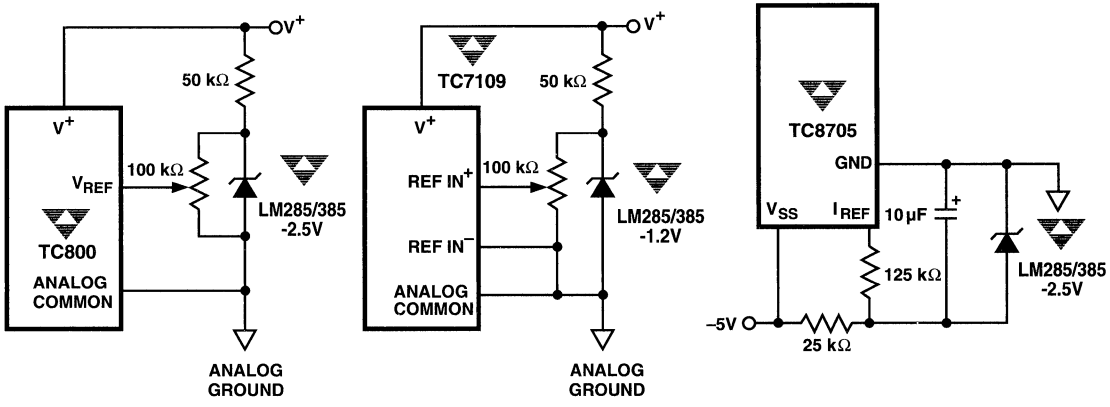
ELECTRICAL CHARACTERISTICS: T_A = +25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	LM285 / LM285B–1.2 Min	Typ	Max	LM385 / LM385B–1.2 Min	Typ	Max	Unit
$V_{(BR)R}$	Reverse Breakdown Voltage	$I_R \le 20$ mA							V
	LM285B-1.2/LM385B-1.2		1.223	1.235	1.247	1.223	1.235	1.247	
	$T_A = T_{low}$ to T_{high} (Note 1)		1.200	—	1.270	1.210	—	1.260	
	LM285-1.2V/LM385-1.2V		1.205	1.235	1.260	1.205	1.235	1.260	
	$T_A = T_{low}$ to T_{high} (Note 1)		1.192	—	1.273	1.192	—	1.273	
I_{RMIN}	Minimum Operating Current								µA
	T_A = +25°C		—	8.0	15	—	8.0	15	
	$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	20	
$\Delta V_{(BR)R}$	Reverse Breakdown Voltage Change with Current								mV
	$I_{Rmin} = I_R$ = 1.0mA, T_A = +25°C		—	—	1.0	—	—	1.0	
	$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
	1.0mA = I_R = 20mA, T_A = +25°C		—	—	10	—	—	20	
	$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Z	Reverse Dynamic Impedance	I_R = 100µA	—	0.6	—	—	0.6	—	Ω
$\Delta V_{(BR)}/\Delta T$	Average Temperature Coefficient	10µA ≤ I_R ≤ 20mA	—	30	100	—	30	100	ppm/°C
S	Long Term Stability	I_R = 100µA, T_A = +25°C ±0.1°C	—	20	—	—	20	—	ppm/kHR

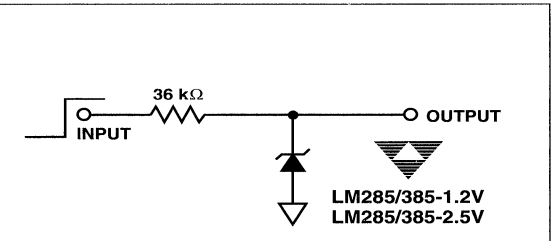
Symbol	Parameter	Test Conditions	LM285 / LM285B–2.5 Min	Typ	Max	LM385 / LM385B–2.5 Min	Typ	Max	Unit
$V_{(BR)R}$	Reverse Breakdown Voltage	I_R = 20 mA							V
	LM285B-2.5/LM385B-2.5		2.462	2.5	2.538	2.462	2.5	2.538	
	$T_A = T_{low}$ to T_{high} (Note 1)		2.415	—	2.585	2.436	—	2.564	
	LM285-2.5V/LM385-2.5V		2.425	2.5	2.575	2.425	2.5	2.575	
	$T_A = T_{low}$ to T_{high} (Note 1)		2.400	—	2.600	2.400	—	2.600	
I_{RMIN}	Minimum Operating Current								µA
	T_A = +25°C		—	13	20	—	13	20	
	$T_A = T_{low}$ to T_{high} (Note 1)		—	—	30	—	—	30	
$\Delta V_{(BR)R}$	Reverse Breakdown Voltage Change with Current								mV
	$I_{Rmin} = I_R$ = 1.0mA, T_A = +25°C		—	—	1.0	—	—	2.0	
	$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	2.5	
	1.0mA = I_R = 20mA, T_A = +25°C		—	—	10	—	—	20	
	$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Z	Reverse Dynamic Impedance	I_R = 100µA	—	0.6	—	—	0.6	—	Ω
$\Delta V_{(BR)}/\Delta T$	Average Temperature Coefficient	10µA ≤ I_R ≤ 20mA	—	30	100	—	30	100	ppm/°C
S	Long Term Stability	I_R = 100µA, T_A = +25°C ±0.1°C	—	20	—	—	20	—	ppm/kHR

Note: 1. T_{low} = –40°C for LM285-1.2, LM285-2.5
0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5
T_{high} = +85°C for LM285-1.2, LM285-2.5
+70°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

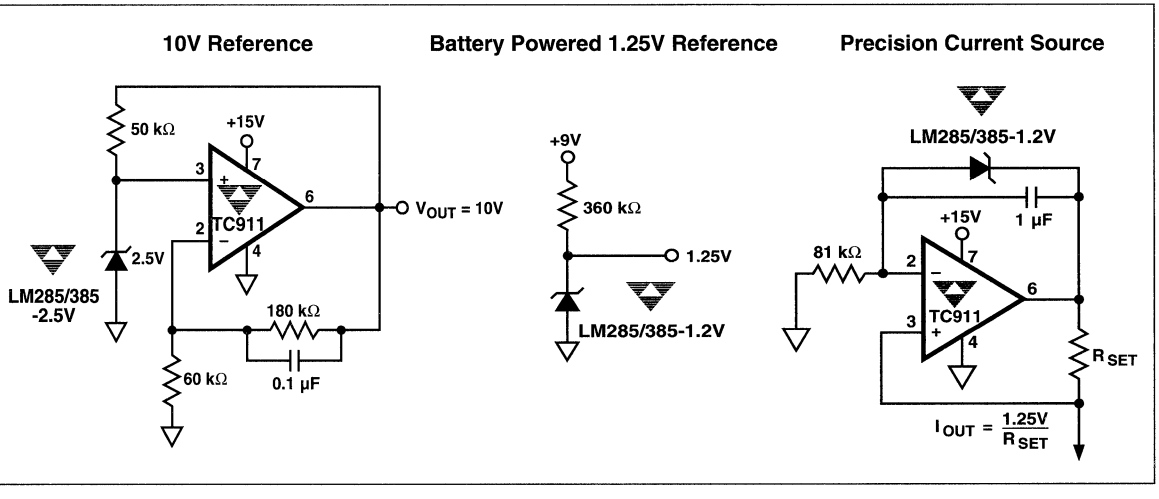
VOLTAGE REFERENCE CIRCUITS FOR SYSTEM DATA CONVERTERS



RESPONSE TIME TEST CIRCUIT

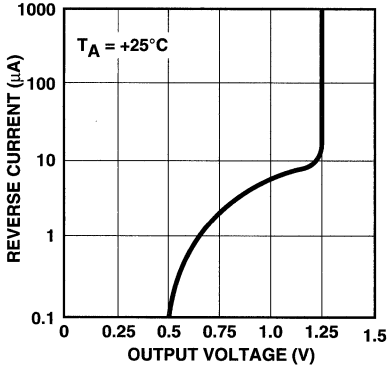


TYPICAL APPLICATIONS

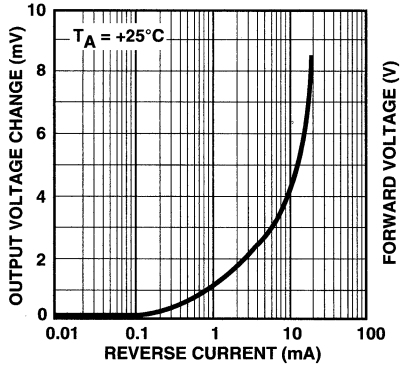


TYPICAL CHARACTERISTICS CURVES

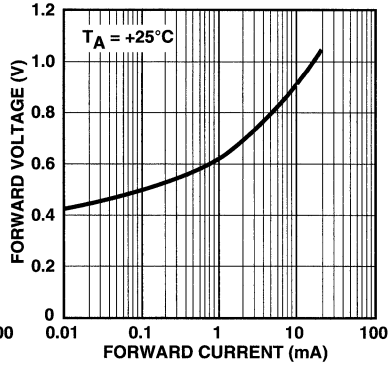
LM285/385-1.2V: Output Voltage vs Reverse Current



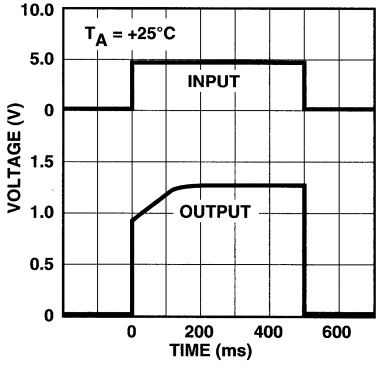
LM285/385-1.2V: Output Voltage Change vs Reverse Current



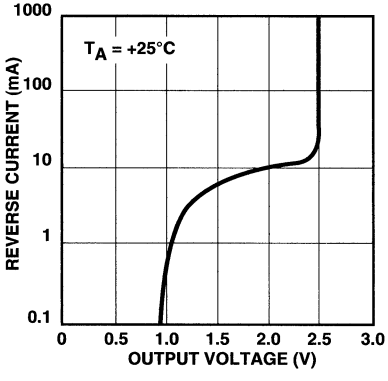
LM285/385-1.2V: Forward Voltage vs Forward Current



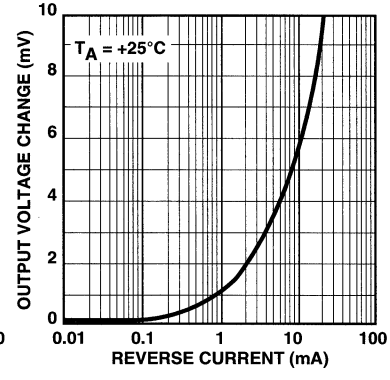
LM285/385-1.2V Response Time



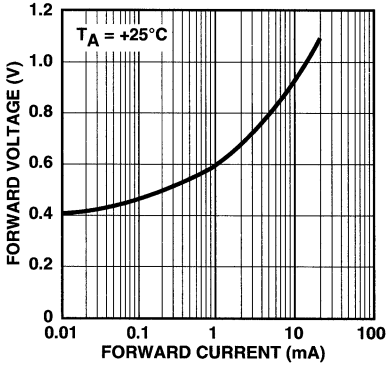
LM285/385-2.5V: Output Voltage vs Reverse Current



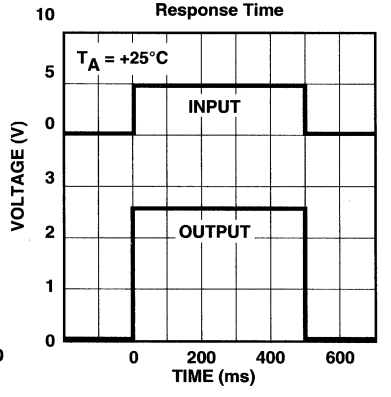
LM285/385-2.5V: Output Voltage Change vs Reverse Current



LM285/385-2.5V: Forward Voltage vs Forward Current



LM285/385-2.5V Response Time



LOW POWER, BAND-GAP VOLTAGE REFERENCES

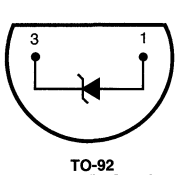
FEATURES

- **Temperature Coefficient ..... 50 ppm/°C**
- **Wide Operating Current Range ..... 15 µA to 20 mA**
- **Dynamic Impedance 0.6Ω**
- **Output Tolerance ..... 1 or 2%**
- **Output Voltage Option 1.220V**
- **TO-92 Plastic Package**
- **8-Pin Plastic Small Outline (SO) Package**

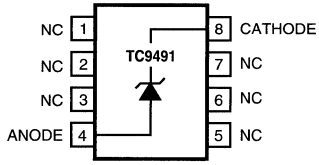
APPLICATIONS

- **ADC and DAC Reference**
- **Current Source Generation**
- **Threshold Detectors**
- **Power Supplies**
- **Multi-meters**

PIN CONFIGURATIONS



TO-92
PLASTIC PACKAGE
(BOTTOM VIEW)



SURFACE MOUNT
PLASTIC PACKAGE

NC = NO INTERNAL CONNECTION

GENERAL DESCRIPTION

The TC9491 (1.220V output) bipolar, two-terminal, band-gap voltage references offer precision performance without premium price. These devices do not require thin-film resistors, greatly lowering manufacturing complexity and cost.

A 50 ppm/°C output temperature coefficient and a 15 µA to 20 mA operating current range make these devices attractive for multimeter, data acquisition converter, and telecommunication voltage references.

ORDERING INFORMATION

	Temperature Range	
Temperature Coeff.	**0°C to +70°C Surface Mount**	**0°C TO +70°C (TO-92)**
50 ppm°C	TC9491ACOA	TC9491ACZB
100 ppm°C	TC9491BCOA	TC9491BCZB

ABSOLUTE MAXIMUM RATINGS

Forward Current ..... +10 mA
Reverse Current ..... +30 mA
Storage Temperature Range ..... – 65°C to +150°C
Operating Temperature Range
TO-92 Package ..... 0°C to +70°C
COA Surface Mount Package ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec)
TO-92 Package ..... +260°C
COA Surface Mount Package ..... +260°C
Power Dissipation
Limited by Forward/Reverse Current

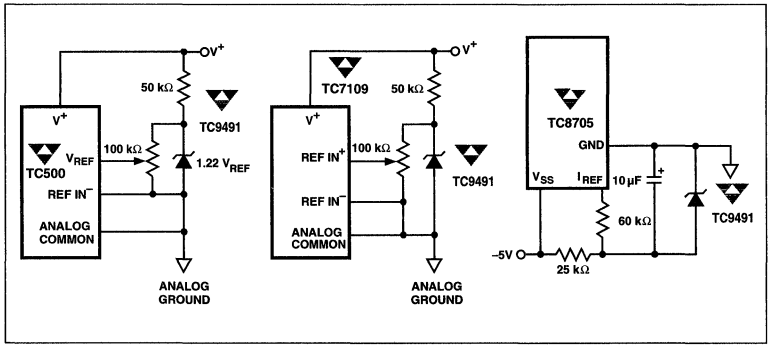
Functional operation above the absolute maximum stress ratings is not implied.

TC9491

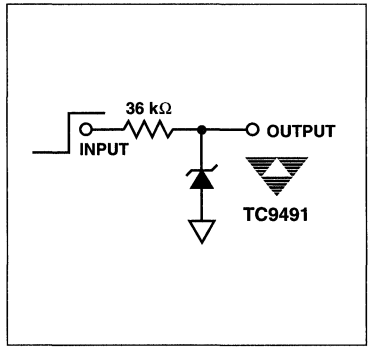
ELECTRICAL CHARACTERISTICS: T_A = +25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	TC9491A Min	TC9491A Typ	TC9491A Max	TC9491B Min	TC9491B Typ	TC9491B Max	Unit
$V_{(BR)R}$	Reverse Breakdown Voltage	$I_R \leq 20$ mA	1.200	1.22	1.250	1.200	1.220	1.250	V
	T_A = 0°C to +70°C		1.180	—	1.290	1.219	—	1.260	
I_{RMIN}	Minimum Operating Current								µA
	T_A = +25°C		—	8.0	15	—	8.0	15	
	T_A = 0°C to +70°C		—	—	20	—	—	20	
$\Delta V_{(BR)R}$	Reverse Breakdown Voltage Change with Current								
	$I_{Rmin} = I_R$ = 1.0mA, T_A = +25°C		—	—	1.0	—	—	1.0	
	T_A = 0°C to +70°C		—	—	1.5	—	—	1.5	mV
	1.0mA = I_R = 20mA, T_A = +25°C		—	—	10	—	—	20	
	T_A = 0°C to +70°C		—	—	20	—	—	25	
Z	Reverse Dynamic Impedence	I_R = 100µA	—	0.6	—	—	0.6	—	Ω
$\Delta V_{(BR)}/\Delta T$	Average Temperature Coefficient	10µA = I_R = 20mA	—	—	50	—	—	100	ppm/°C
S	Long Term Stability	I_R = 100µA, T_A = +25°C ±0.1°C	—	20	—	—	20	—	ppm/kHR

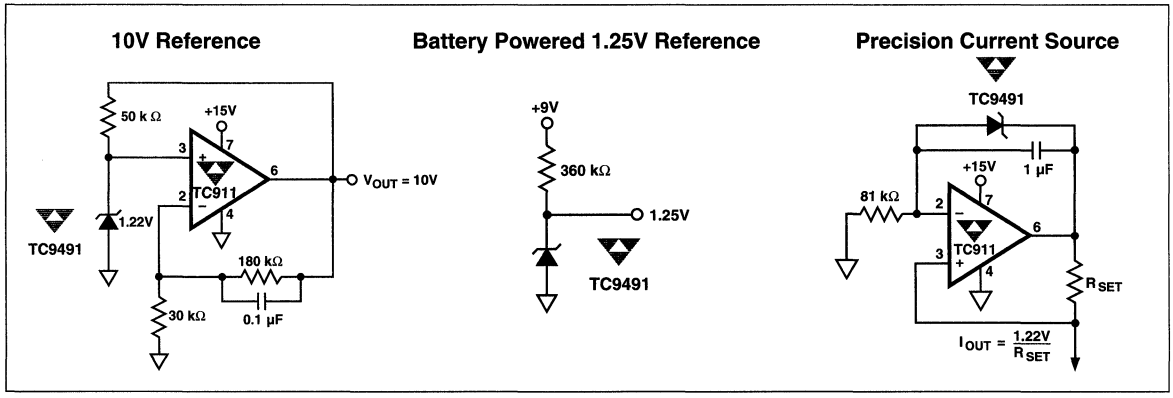
VOLTAGE REFERENCE CIRCUITS FOR SYSTEM DATA CONVERTERS



RESPONSE TIME TEST CIRCUIT

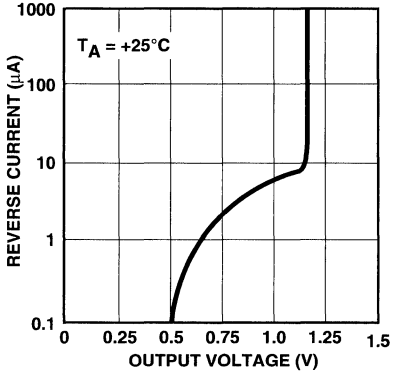


TYPICAL APPLICATIONS

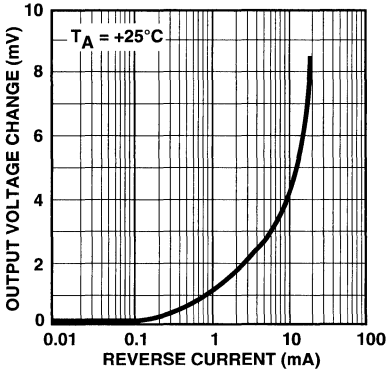


TYPICAL CHARACTERISTICS CURVES

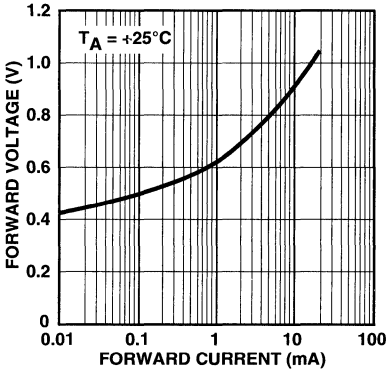
Output Voltage vs Reverse Current



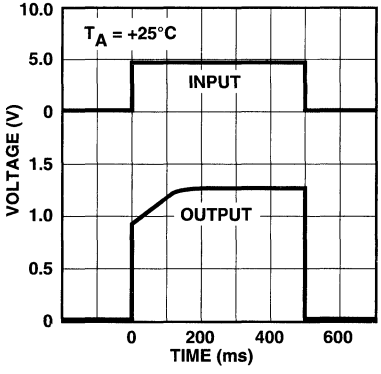
Output Voltage Change vs Reverse Current



Forward Voltage vs Forward Current



Response Time

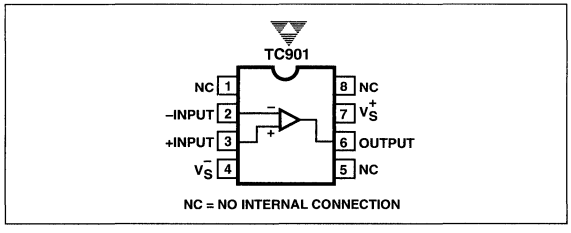


AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

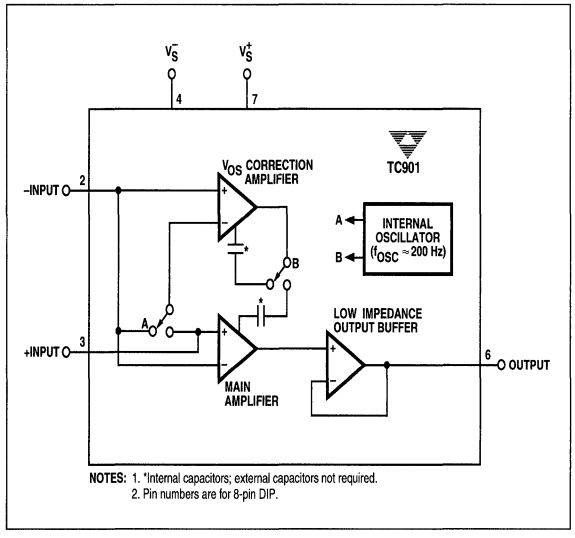
- **Second-Generation Monolithic, Chopper-Stabilized Op-Amp**
- **No External Capacitors Required**
- **Single-Supply Operation ..... ±15V or 5V to 32V**
- **Supply Current ..... 450 μA at 15V, Typ**
- **Input Offset Voltage ..... 7 μV, Typ**
- **Common-Mode Rejection Ratio ..... 140 dB, Typ**
- **Open-Loop Gain ..... 140 dB Into 10k Load, Typ**
- **Input Noise ..... 5 μV at 10 Hz Bandwidth**
- **Pinout Compatible With ICL7650**
- **Lowest Parts Count Chopper Op-Amp**

PIN CONFIGURATION (DIP and SO)



NC = NO INTERNAL CONNECTION

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. *Internal capacitors; external capacitors not required.
2. Pin numbers are for 8-pin DIP.

GENERAL DESCRIPTION

The TC901 is a monolithic, auto-zeroed operational amplifier. It is a second-generation design of the TC91X series, the world's first monolithic, CMOS chopper-stabilized op-amps with on-chip capacitors. This second-generation design allows use of higher supply voltages (±15V or single supply 30V), while decreasing noise.

Elimination of the external capacitors allows the designer to increase reliability, lower cost, and simplify design by lowering parts count.

Since the TC901 is an auto-zeroing op-amp, input offset voltage is very low. More important, there is almost zero drift with time. This eliminates production line adjustments, as well as periodic calibration.

Notable electrical characteristics are low supply current (450 μA, typical), single-supply operation (5V to 32V), low input offset voltage (7 μV, typical), low noise (<5 μV_{P-P}, typical, for a 10 Hz bandwidth), and fast recovery from saturation without the use of external clamp circuitry.

This device is supplied in 8-pin mini-dual-in-line and plastic SO (small outline) packages. It is pin compatible with bipolar, CMOS, JFET and chopper-stabilized op-amps using the industry-standard 741 pinout.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC901COA	8-Pin SO	0°C to +70°C
TC901CPA	8-Pin Plastic DIP	0°C to +70°C
TC901IOA	8-Pin SO	– 25°C to +85°C
TC901IPL	8-Pin Plastic DIP	– 25°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +36V
Input Voltage ..... (V_S^+ + 0.3V) to (V_S^- – 0.3V)
Current Into Any Pin ..... 10 mA
  While Operating ..... 100 µA
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
  C Device ..... 0°C to +70°C
  I Device ..... – 25°C to +85°C
  M Device ..... – 55°C to +125°C

Package Power Dissipation (T_A = +25°C)
  CerDIP ..... 500 mW
  Plastic DIP ..... 375 mW

Static-sensitive device. Appropriate precautions should be taken when handling, shipping, or storing these devices. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: V_S ±15V, T_A = +25°C, unless otherwise indicated (each amplifier).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage (Figure 2)	T_A = +25°C	—	7	15	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage (Note 2)	0°C ≤ T_A ≤ +70°C	—	0.05	0.15	µV/°C
I_{BIAS}	Average Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	30 0.2 0.2	50 10 10	pA nA nA
I_{OS}	Average Input Offset Current	T_A = +25°C T_A = +85°C	— —	50 —	100 1	pA nA
e_N	Input Voltage Noise (Figure 1B)	0.1 to 1 Hz, R_S ≤ 100W	—	1.2	—	μV_{P-P}
e_N	Input Voltage Noise (Figure 1A)	0.1 to 10 Hz, R_S ≤ 100W	—	5	—	μV_{P-P}
CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2V$	120	140	—	dB
CMVR	Common-Mode Voltage Range	V_S = ±5V to ±15V	V_S^-	—	$V_S^+ - 2$	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kW, V_S = ±15V	120	140	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kW	$V_S^- + 1$	—	$V_S^+ - 1.2$	V
BW	Closed-Loop Bandwidth (Figure 7)	Closed-Loop Gain = +1	—	0.8	—	MHz
sr	Slew Rate	R_L = 10 kW, C_L = 50 pF	—	2	—	V/µs
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	120	140	—	dB
V_S	Operating Supply Voltage Range	Note 1	±3	—	±16	V
I_S	Quiescent Supply (Figure 2)	V_S = ±15V	—	0.45	0.6	mA

NOTES: 1. Single supply operation: V_S^+ = +5V to +32V.
2. Characterized; not 100% tested.

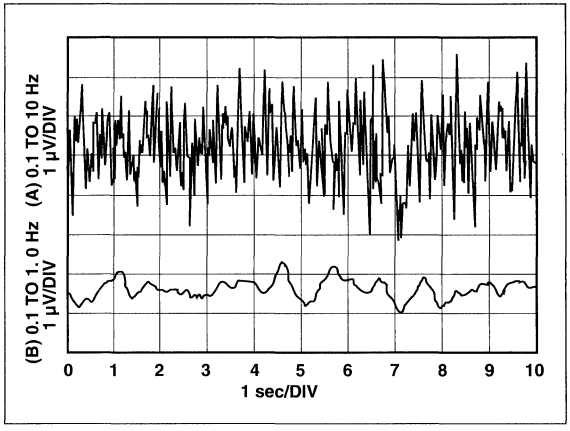


Figure 1 Input Voltage Noise

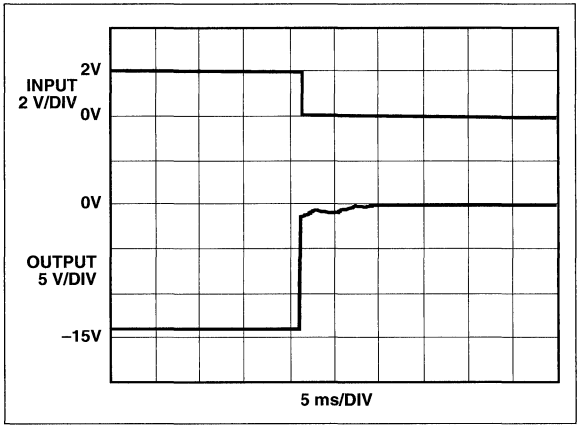


Figure 3 Recovery From Negative Saturation

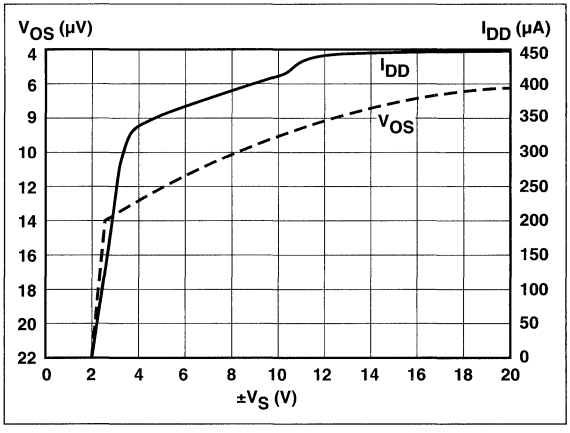


Figure 2 V_{OS} and I_{DD} vs Supply Voltage

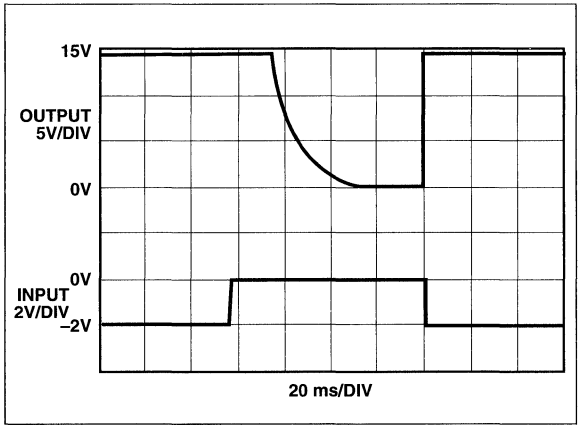


Figure 4 Recovery From Positive Saturation

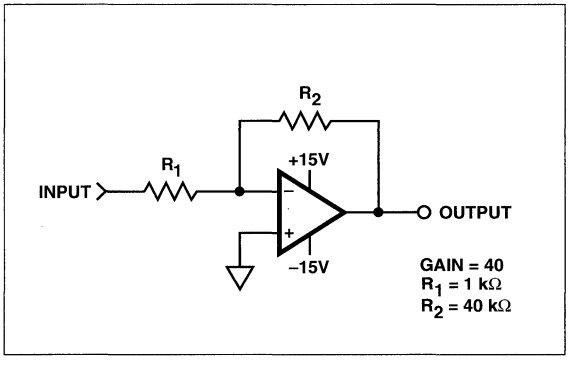


Figure 5 Saturation Test Circuit

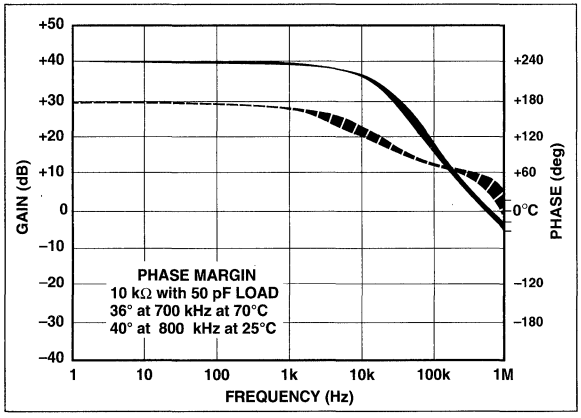


Figure 6 Phase-Gain

Overload Recovery

The TC901 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open-circuit voltage (Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1 μV/°C to 10 μV/°C. Thermal-induced voltages can be many times larger than the TC901's offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermoelectric coefficient solder can reduce errors. A 60% Cd/40% Sn Pb solder has one-tenth the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 7).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and minimize thermocouple-induced errors.

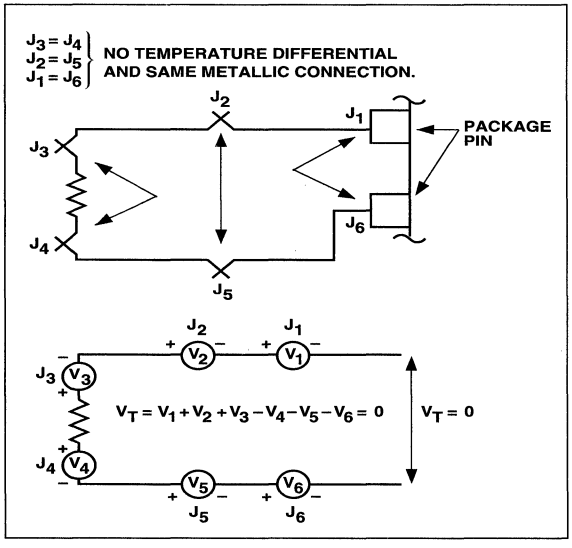


Figure 7 Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC901's power supply should be established at the same time (or before) input signals are applied. If this is not possible, input current should be limited to 100 μA to avoid triggering the p-n-p-n structure.

Pin Compatibility

The CMOS TC901 is pin compatible with other chopper-stabilized amplifiers, such as the 7650, 7652 and 1052. Amplifiers such as the 7650 require 0.1 μF external capacitors connected to pins 1 and 8. The TC901 includes the chopper capacitors on-chip, so external capacitors are not required. Since pins 1, 5 and 8 of the TC901 are not connected, the TC901 can directly replace other chopper-stabilized amplifiers in existing circuits.

The TC901 pinout also matches many popular bipolar and JFET op-amps, such as the OP-07, OP20, LM101, LM108, 356 and 741. In many applications that operate from ±15V power supplies, the TC901 offers superior electrical performance and is a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs. System parts count, assembly time, and system cost are reduced, while reliability and performance are improved.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers establish "static safe" CMOS component handling areas. Two such companies are:

- 3M
  Static Control Systems Division
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- **First Monolithic Chopper-Stabilized Amplifier With On-Chip Nulling Capacitors**
- **Offset Voltage ..... 5 μV**
- **Offset Voltage Drift ..... 0.05 μV/°C**
- **Low Supply Current ..... 350 μA**
- **High Common-Mode Rejection ..... 116 dB**
- **Single Supply Operation ..... 4.5V to 16V**
- **High Slew Rate ..... 2.5 V/μs**
- **Wide Bandwidth ..... 1.5 MHz**
- **High Open-Loop Voltage Gain (R_L = 10 kΩ) ..... 120 dB**
- **Low Input Voltage Noise (0.1 Hz to 1 Hz) ..... 0.65 μV_{P-P}**
- **Pin Compatible With ICL7650**
- **Lower System Parts Count**

ORDERING INFORMATION

Part No.	Package	Temperature Range	Maximum Offset Voltage
TC911ACPA	8-Pin Plastic DIP	0°C to +70°C	15 μV
TC911ACOA	8-Pin SO	0°C to +70°C	15 μV
TC911BCPA	8-Pin Plastic DIP	0°C to +70°C	30 μV
TC911BCOA	8-Pin SO	0°C to +70°C	30 μV

GENERAL DESCRIPTION

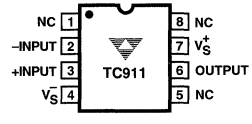
The TC911 CMOS auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user-supplied, external offset compensation storage capacitors. **External capacitors are not required with the TC911.** Just as easy to use as the conventional OP07 type amplifier, the TC911 significantly reduces offset voltage errors. Pinout matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors: lower system parts count; reduced assembly time and cost; greater system reliability; reduced PC board layout effort and greater board area utilization. Also, space savings can be significant in multiple-amplifier designs.

Electrical specifications include 15 μV maximum offset voltage, 0.15 μV/°C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. The TC911 improves offset drift performance by eight times.

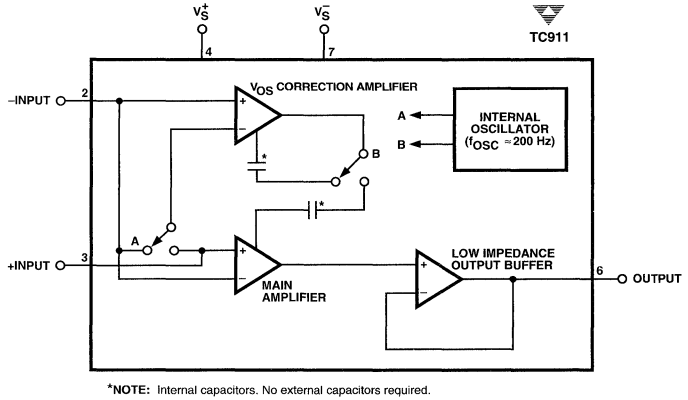
The TC911 operates from dual or single power supplies. Supply current is typically 350 μA. Single 4.5V to 16V supply operation is possible, making single 9V battery operation possible. The TC911 is available in 2 package types: 8-pin plastic DIP,and SO package.

PIN CONFIGURATION (SO AND DIP)



NC = NO INTERNAL CONNECTION

FUNCTIONAL BLOCK DIAGRAM



*NOTE: Internal capacitors. No external capacitors required.

TC911A/B

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +18V
Input Voltage ..... (V_S^++0.3V) to (V_S^-–0.3V)
Current into Any Pin ..... 10 mA
While Operating ..... 100 µA
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
C Device ..... 0°C to +70°C
I Device ..... –25°C to +85°C

Package Power Dissipation (T_A = +25°C)
CerDIP ..... 500 mW
Plastic DIP and SO ..... 375 mW

Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

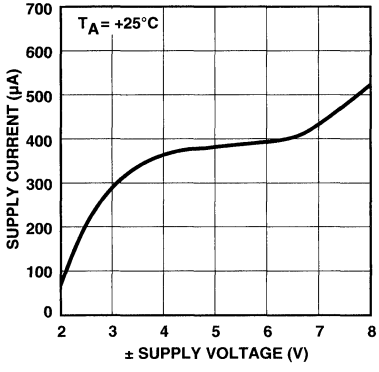
ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

			TC911A			TC911B			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C (Note 1)	— —	0.05 0.05	0.15 0.15	— —	0.1 0.1	0.25 0.25	µV/°C µV/°C
I_B	Average Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	— — —	70 3 4	— — —	— — —	120 4 6	pA nA nA
I_{OS}	Average Input Offset Current	T_A = +25°C T_A = +85°C	— —	5 —	20 1	— —	10 —	40 1	pA nA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω 0.1 to 10 Hz, R_S ≤ 100Ω	— —	0.65 11	— —	— —	0.65 11	— —	μV_{P-P} μV_{P-P}
CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2$	110	116	—	105	110	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	$V_S^+ - 2$	V_S^-	—	$V_S^+ - 2$	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- +0.3	—	$V_S^+ - 0.9$	V_S^- +0.3	—	$V_S^+ - 0.9$	V
BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2.5	—	—	2.5	—	V/µs
PSRR	Power Supply Rejection Ratio	±3.3V to ±5.5V	112	—	—	105	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply Single Supply	±3.3 6.5	— —	±8 16	±3.3 6.5	— —	±8 16	V V
I_S	Quiescent Supply Current	V_S = ±5V	—	350	600	—	—	800	µA

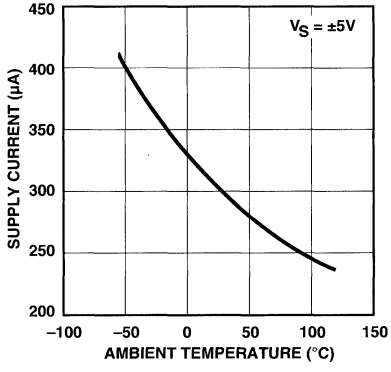
NOTES: 1. Characterized; not 100% tested.

TYPICAL CHARACTERISTICS CURVES

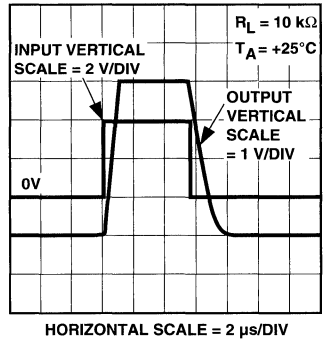
Supply Current vs ± Supply Voltage



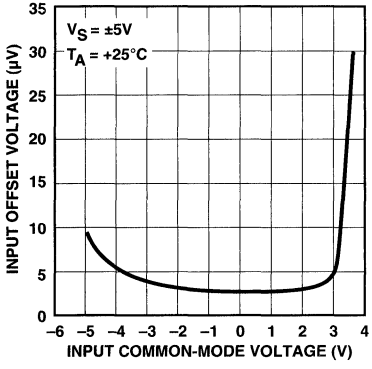
Supply Current vs Temperature



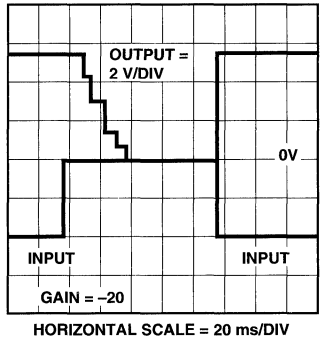
Large Signal Output Switching Waveform



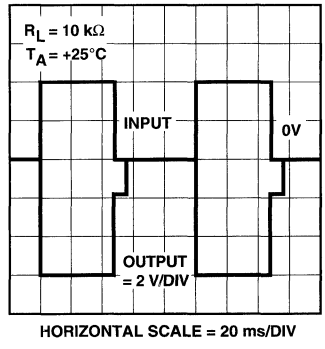
Input Offset Voltage vs Common-Mode Voltage



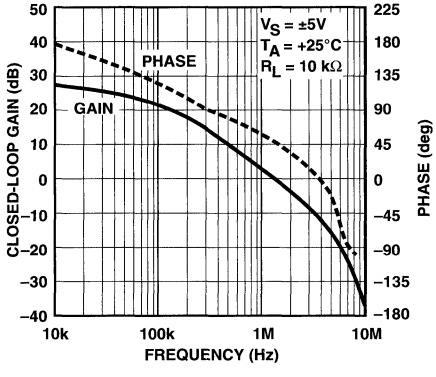
Positive Overload Recovery Time



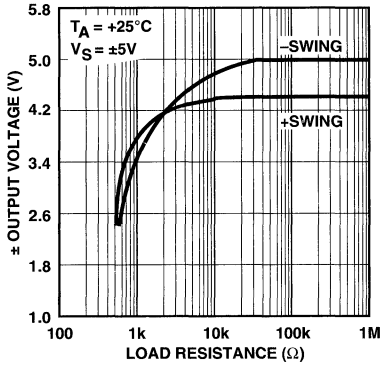
Negative Overload Recovery Time



Gain and Phase vs Frequency



Output Voltage Swing vs Load Resistance



Pin Compatibility

The CMOS TC911 is pin compatible with the industry standard ICL7650 chopper-stabilized amplifier. The ICL7650 must use external 0.1 μF capacitors connected at pins 1 and 8. **With the TC911, external offset voltage error canceling capacitors are not required.** On the TCS911 pins 1, 8 and 5 are not connected internally. The ICL7650 uses pin 5 as an optional output clamp connection. External chopper capacitors and clamp connections are not necessary with the TC911. External circuits connected to pins 1, 8 and 5 will have no effect. The TC911 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required, system part count, assembly time, and total system cost are reduced. Reliability is increased and PC board layout eased by having the error storage capacitors integrated on the TC911 chip.

The TC911 pinout matches many existing op-amps: 741, LM101, LM108, OP05–OP08, OP20, OP21, ICL7650 and ICL7652. In many applications operating from +5V supplies the TC911 offers superior electrical performance and can be a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs.

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open circuit voltage (Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1 μV/°C to 10 μV/°C. Thermal-induced voltages can be many times larger than the TC911 offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

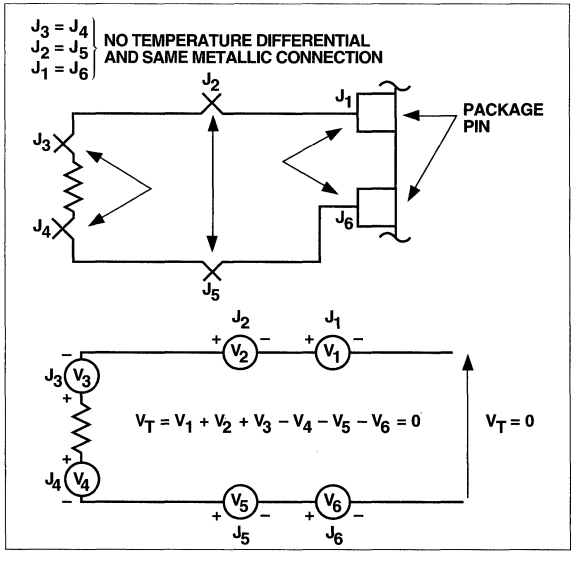


Figure 1. Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has 1/10 the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 1).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and thermocouple-induced errors.

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC911 power supplies should be established at the same time or before input signals are applied. If this is not possible input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers to establish "static safe" CMOS component handling areas. A partial company list is:

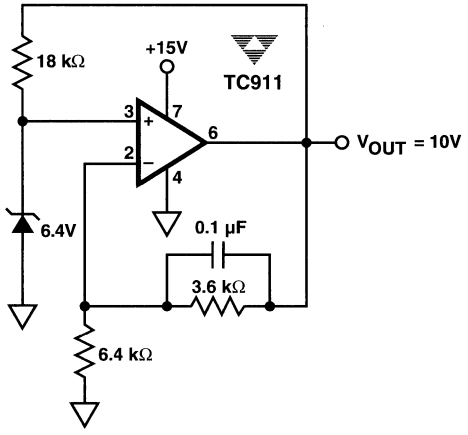
- 3M
  Static Control Systems Div
  223-23W EM Center
  St Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Overload Recovery

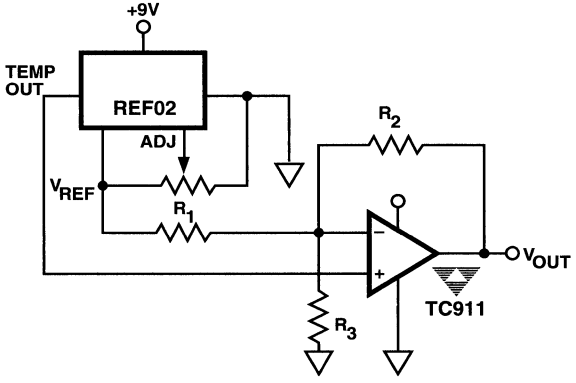
The TC911 recovers quickly from the output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

TYPICAL APPLICATIONS

10-Volt Precision Reference



Thermometer Circuit

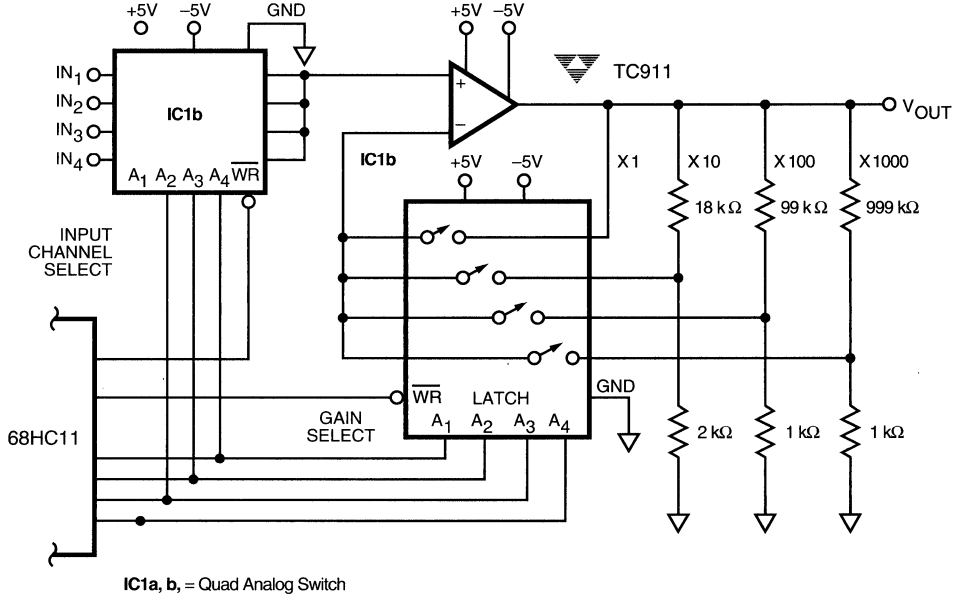


$$V_{OUT} = V_{TEMP}\left[1 + R_2\left(\frac{R_3 + R_1}{R_3 X\ R_1}\right)\right] - \left[V_{REF}\frac{R_2}{R_1}\right]$$

$$\frac{d\,V_{OUT}}{dT} = \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 X\ R_1}\right)\right]\frac{d\,(V_{TEMP})}{dT} \approx K\ (2.1\ mV/°C)$$

$$K = 1 + \frac{R_2}{R_3 X\ R_1}$$

Programmable Gain Amplifier With Input Multiplexer



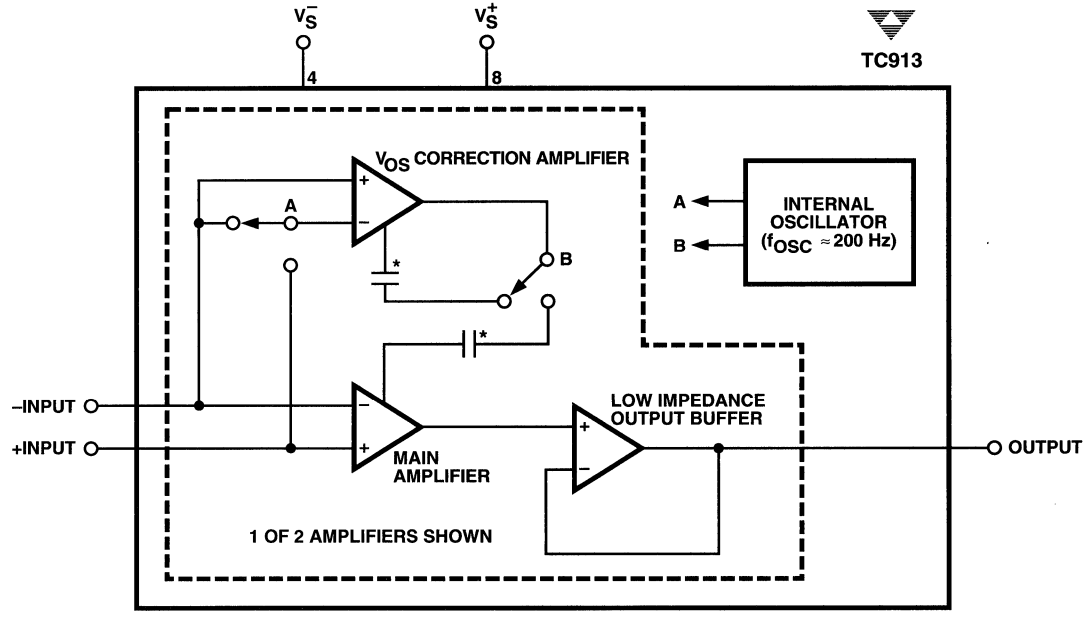
IC1a, b, = Quad Analog Switch

DUAL AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- First Monolithic Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — V_{OS} ..... 15 μV Max
  - — V_{OS} Drift ..... 0.15 μV/°C Max
  - — Saves Cost/Assembly of Four "Chopper" Capacitors
- SO Packages Available
- High DC Gain ..... 120 dB
- Low Supply Current ..... 650 μA
- Low Input Voltage Noise (0.1 Hz to 10 Hz) ..... 0.65 μV_{P-P}
- Wide Common-Mode Voltage Range ..... V_S^- to V_S^+ –2V
- High Common-Mode Rejection ..... 116 dB
- Dual or Single Supply Operation .... ±3.3V to ±8.3V, +6.5V to +16V
- Excellent AC Operating Characteristics
  - — Slew Rate ..... 2.5 V/μs
  - — Unity-Gain Bandwidth ..... 1.5 MHz
- Pin Compatible With LM358, OP14, MC1458, ICL7621, TL082, TLC322

FUNCTIONAL BLOCK DIAGRAM



*NOTE: Internal capacitors. No external capacitors required.

TC913

GENERAL DESCRIPTION

The TC913 is the world's first complete monolithic, dual auto-zeroed operational amplifier. The TC913 sets a new standard for low-power, precision dual-operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error, and storing correction voltages on capacitors. Previous single amplifier designs required two user-supplied, external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TC913 architecture requires smaller capacitors, making on-chip integration possible. Microvolt offset levels are achieved and **external capacitors are not required.**

The TC913 system benefits are apparent when contrasted with a TC7650 chopper amplifier circuit implementation. A single TC913 replaces two TC7650's and four capacitors. Five components and assembly steps are eliminated.

The TC913 pinout matches many popular dual-operational amplifiers: OP04, TLC322, LM358, and ICL7621 are typical examples. In many applications, operating from dual 5V power supplies or single supplies, the TC913 offers superior electrical performance, and can be a functional drop-in replacement; printed circuit board rework is not necessary. The TC913's low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low-accuracy CMOS operational amplifiers.

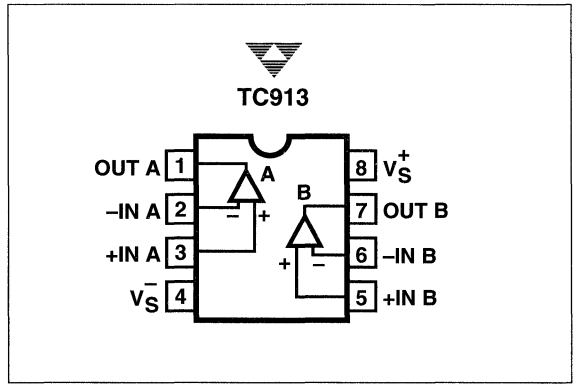
The TC913 takes full advantage of TelCom's proprietary CMOS technology. The TC913's 650 μA supply current (250 μA per amplifier) makes the TC913 the lowest power, precision dual-operational amplifier available. The 250 μA amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

For single- and quad-operational amplifiers, see the TC911 and TC914 data sheets.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Maximum Offset Voltage
TC913ACPA	8-Pin Plastic DIP	0°C to +70°C	15 μV
TC913ACOA	8-Pin SO	0°C to +70°C	15 μV
TC913BCPA	8-Pin Plastic DIP	0°C to +70°C	30 μV
TC913BCOA	8-Pin SO	0°C to +70°C	30 μV
TC913AIJA	8-Pin CerDIP	–25°C to +85°C	15 μV
TC913BIJA	8-Pin CerDIP	–25°C to +85°C	30 μV

PIN CONFIGURATION (SO and DIP)



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +18V
Input Voltage ..... (V_S^++0.3V) to (V_S^-–0.3V)
Current into Any Pin ..... 10 mA
  While Operating ..... 100 µA
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
  C Device ..... 0°C to +70°C
  I Device ..... –25°C to +85°C

Package Power Dissipation (T_A = +25°C)
  CerDIP ..... 500 mW
  Plastic DIP and SO ..... 375 mW

Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

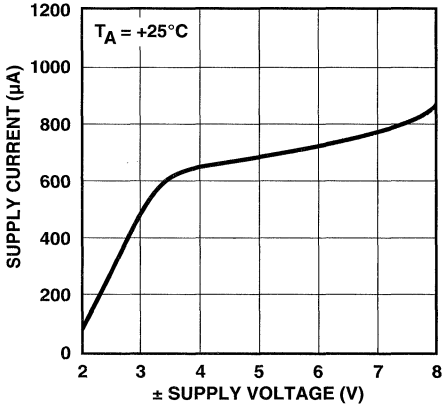
ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

			TC913A			TC913B			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C (Note 1)	— —	0.05 0.05	0.15 0.15	— —	0.1 0.1	0.25 0.25	µV/°C µV/°C
I_B	Average Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
I_{OS}	Average Input Offset Current	T_A = +25°C T_A = +85°C	— —	5 —	20 1	— —	10 —	40 1	pA nA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω 0.1 to 10 Hz, R_S ≤ 100Ω	— —	0.6 11	— —	— —	0.6 11	— —	μV_{P-P} μV_{P-P}
CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2V$	110	116	—	100	110	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ –2	V_S^-	—	V_S^+ –2	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- +0.3	—	V_S^+ –0.9	V_S^- +0.3	—	V_S^+ –0.9	V
BW	Closed-Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2.5	—	—	2.5	—	V/µs
PSRR	Power Supply Rejection Ratio	±3.3V ≤ V_S ≤ ±5.5V	110	—	—	100	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply Single Supply	±3.3 6.5	— —	±8.3 16	±3.3 6.5	— —	±8.3 16	V V
I_S	Quiescent Supply Current	V_S = ±5V	—	0.65	0.85	—	—	1.1	mA

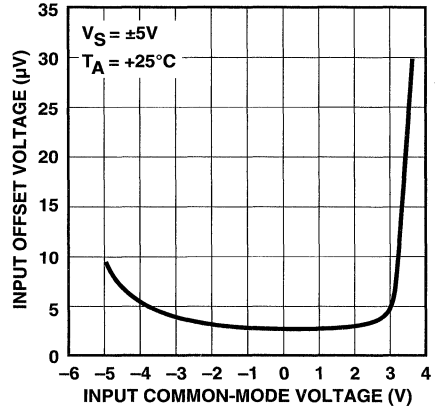
NOTE: 1. Characterized; not 100% tested.

TYPICAL CHARACTERISTICS CURVES

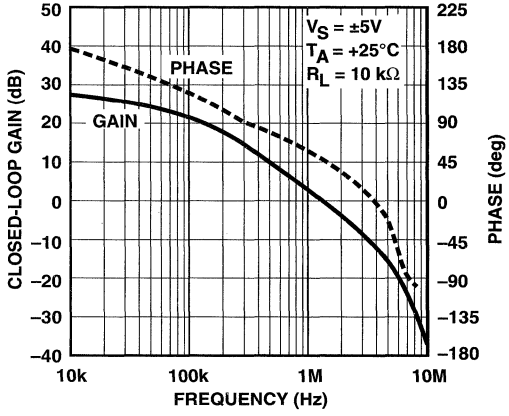
Supply Current vs ± Supply Voltage



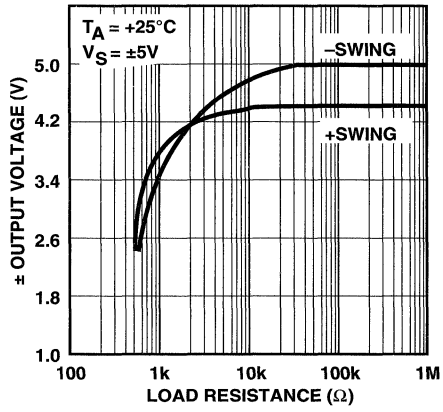
Input Offset Voltage vs Common-Mode Voltage



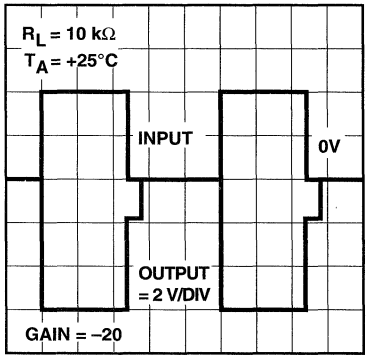
Gain and Phase vs Frequency



Output Voltage Swing vs Load Resistance

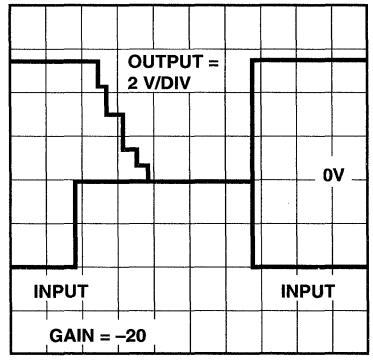


Negative Overload Recovery Time



HORIZONTAL SCALE = 20 ms/DIV

Positive Overload Recovery Time



HORIZONTAL SCALE = 20 ms/DIV

Theory of Operation

Each of the TC913's two op-amps actually consists of two amplifiers. A main amplifier is always connected from the input to the output. A separate nulling amplifier alternately nulls its own offset and then the offset of the amplifier. Since each amplifier is continuously being nulled, offset voltage drift with time, temperature, and power supply variations is greatly reduced.

All nulling circuitry is internal and the nulling operation is transparent to the user. Offset nulling voltages are stored on two internal capacitors. An internal oscillator and control logic, shared by the TC913's two amplifiers, control the nulling process.

Pin Compatibility

The TC913 pinout is compatible with OP14, LM358, MC1458, LT1013, TLC322, and similar dual op-amps. In many circuits operating from single or ±5V supplies, the TC913 is a drop-in replacement offering DC performance rivaling that of the best single op-amps.

The TC913's amplifiers include a low-impedance class AB output buffer. Some previous CMOS chopper amplifiers used a high-impedance output stage which made open-loop gain dependent on load resistance. The TC913's open-loop gain is not dependent on load resistance.

Overload Recovery

The TC913 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and power dissipation. The TC913's power supplies should be established at the same time or before input signals are applied. If this is not possible, input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers to establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- **Low Input Offset Voltage ..... 0.7 μV Typ**
- **Low Input Offset Voltage Drift ..... 0.05 μV/°C Max**
- **Low Input Bias Current ..... 10 pA Max**
- **High Impedance Differential CMOS Inputs .... $10^{12}\Omega$**
- **High Open-Loop Voltage Gain ..... 120 dB Min**
- **Low Input Noise Voltage ..... 2.0 μ Vp-p**
- **High Slew Rate ..... 2.5 V/μs**
- **Low-Power Operation ..... 20 mW**
- **Output Clamp Speeds Recovery Time**
- **Compensated Internally for Stable Unity Gain Operation**
- **Direct Replacement for ICL7650**
- **Available in 8-Pin Dip**

ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC7650CPA	8-Pin Plastic DIP	0°C to +70°C	5 μV
TC7650IJA	8-Pin CerDIP	–25°C to +85°C	5 μV
TC7650CPD	14-Pin Plastic DIP	0°C to +70°C	5 μV
TC7650IJD	14-Pin CerDIP	–25°C to +85°C	5 μV

GENERAL DESCRIPTION

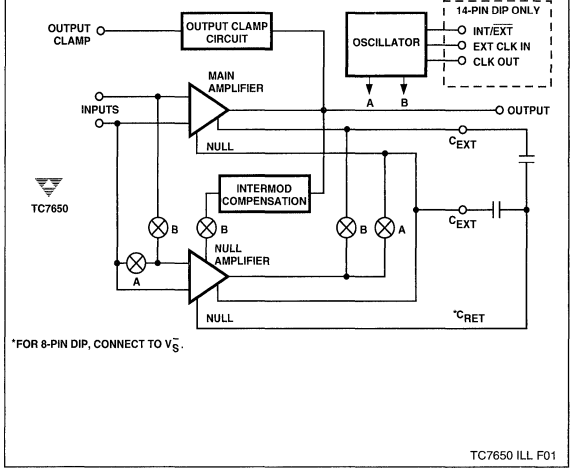
The TC7650 CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a 15 times improvement over the industry-standard OP07E. The 50 nV/°C offset drift specification is over 25 times lower than the OP07E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

The TC7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques.

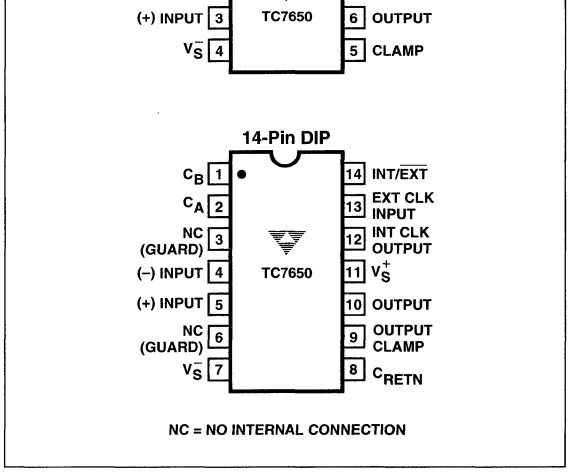
The TC7650 nulling scheme corrects both DC V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user-supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TC7650 output.

The 14-pin dual-in-line package (DIP has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8- and 14-pin DIPs have an output voltage clamp circuit to minimize overload recovery time.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



TC7650

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) 18V
Input Voltage ..... (V_S^++0.3V) to (V_S^-–0.3V)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Output Short Circuit Duration ..... Indefinite
Current Into Any Pin ..... 10 mA
  While Operating (Note 4) ..... 100 µA
Operating Temperature Range
  I Device ..... –25°C to +85°C
  C Device ..... 0°C to +70°C

Package Power Dissipation (T_A = 25°C)
  CerDIP ..... 500 mW
  Plastic DIP ..... 375 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = –5V, C_A = C_B = 0.1 µF, T_A = 25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
V_{OS}	Input Offset Voltage	T_A = +25°C Over Operating Temp Range (Note 1)	— —	±0.7 ± 1.0	±5 —	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Temperature Coefficient	Operating Temperature Range (Note 1)	—	0.01	0.05	µV/°C
	Offset Voltage vs. Time		—	100	—	nV/ month
I_{BIAS}	Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	1.5 35 100	10 150 400	pA pA pA
I_{OS}	Input Offset Current	T_A = +25°C	—	0.5	—	pA
e_{NP-P}	Input Noise Voltage	R_S = 100Ω, 0 to 10 Hz	—	2	—	μV_{P-P}
I_N	Input Noise Current	f = 10 Hz	—	0.01	—	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance		—	10^{12}		Ω
CMVR	Common-Mode Voltage Range		–5	–5.2 to +2	+1.6	V
CMRR	Common-Mode Rejection Ratio	CMVR = –5V to +1.5V	120	130	—	dB
Output						
A	Large Signal Voltage Gain	R_L = 10 kΩ	120	130	—	dB
V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ R_L = 100 kΩ	±4.7 —	±4.85 ±4.95	— —	V V
	Clamp ON Current (Note 2)	R_L = 100 kΩ	25	70	200	µA
	Clamp OFF Current (Note 2)	–4V < V_{OUT} < +4V	—	1	—	pA
Dynamic						
B_W	Unity-Gain Bandwidth	Unity Gain (+1)	—	2.0	—	MHz
S_R	Slew Rate	C_L = 50 pF, R_L = 10 kΩ	—	2.5	—	V/µs
t_R	Rise Time		—	0.2	—	µs
	Overshoot		—	20	—	%
f_{CH}	Internal Chopping Frequency	Pins 12–14 Open (DIP)	120	200	375	Hz

ELECTRICAL CHARACTERISTICS: $V_S^+ = +5V$, $V_S^- = -5V$, $C_A = C_B = 0.1\ \mu F$, $T_A = 25°C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Supply						
V_S^+, V_S^-	Operating Supply Range		4.5	—	16	V
I_S	Supply Current	No Load	—	2	3.5	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 8V$	120	130		dB

NOTES: 1. Operating temperature range is –25°C to +85°C for "I" grade and 0°C to +70°C for "C" grade.
2. See "Output Clamp" discussion.
3. Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems.

Theory of Operation

Figure 1 shows the major elements of the TC7650. There are two amplifiers (the main amplifier and the nulling amplifier), and both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed-forward-type injection into the compensation capacitor that can cause output spikes in this type circuit.

The circuit's offset voltage compensation is easily shown. With the nulling inputs shorted, a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$V_{OSE} = \frac{1}{A_N + 1} \quad V_{OSN} \qquad (1)$$

After the nulling amplifier is zeroed, the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$V_O = A_M [V_{OSM} + (V^+ - V^-) + A_N (V^+ - V^-) + A_N V_{OSE}] \qquad (2)$$

Substituting (1) → (2) and assuming $A_N >> 1$:

$$V_O = A_M A_N \left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right] \qquad (3)$$

As desired, the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, the lower gain is of little consequence, since the DC gain is typically greater than 120 dB, even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This results in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region, where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier results in a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies, and causing disturbances to the gain and phase versus frequency characteristics near the chopping frequency. These effects are substantially reduced in the TC7650 by feeding the nulling circuit with a dynamic current corresponding to the compensation capacitor current in such a way as to cancel that portion of the input signal due to a finite AC gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

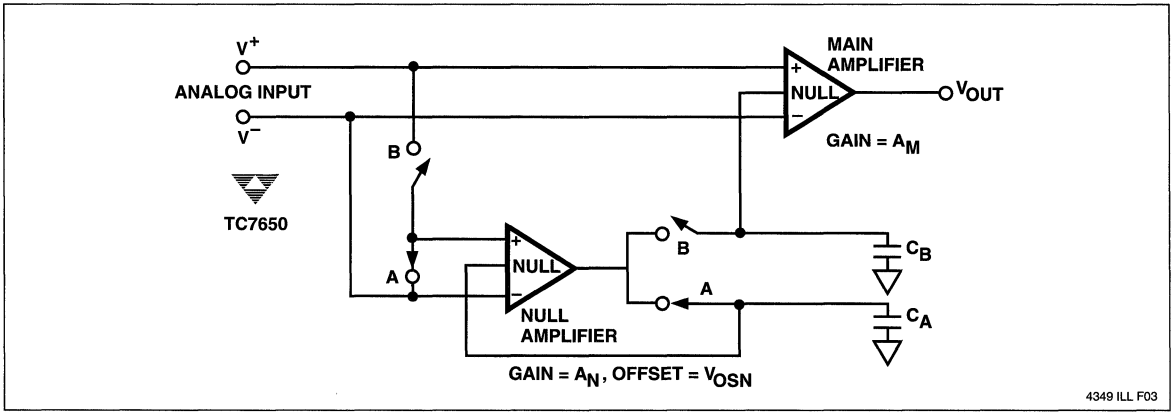


Figure 1 TC7650 Contains a Nulling and Main Amplifier. Offset Correction Voltages Are Stored on Two External Capacitors.

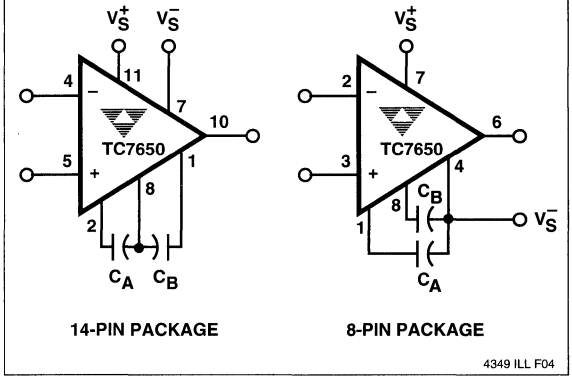


Figure 2 Nulling Capacitor Connection

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (pin 4) on the 8-pin packages and to capacitor return (C_R, pin 8) on the 14-pin packages. The common connection should be made through either a separate PC trace or wire, to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or V_S^-.

Clock Operation

The internal oscillator is set for a 200 Hz nominal chopping frequency on both the 8- and 14-pin DIPs. With the 14-pin DIP TC7650, the 200 Hz internal chopping frequency is available at the internal clock output (pin 12). A 400 Hz nominal signal will be present at the external clock input pin (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide-by-two operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V and between V^+ and V^+ – 6V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical, since an internal divide-by-two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is LOW during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitors pins are very low. At 25°C a typical TC7650 will drift less than 10 µV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TC7650 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

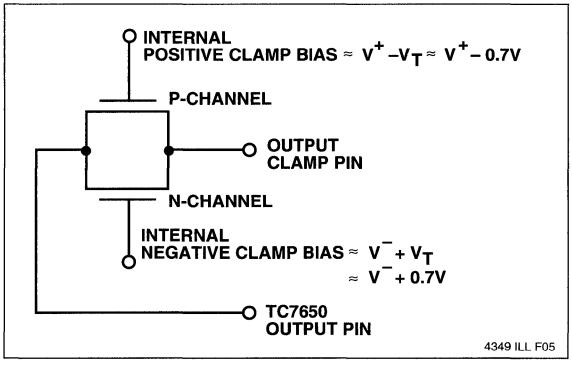


Figure 3 Internal Clamp Circuit

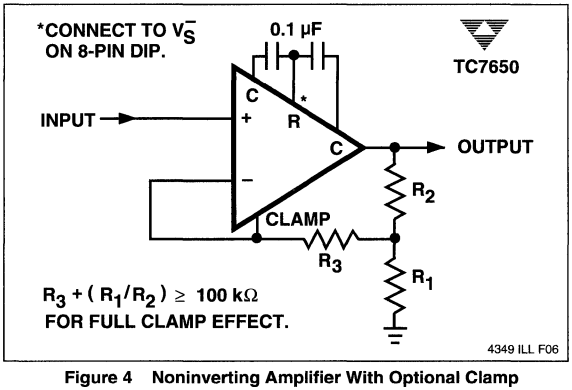


Figure 4 Noninverting Amplifier With Optional Clamp

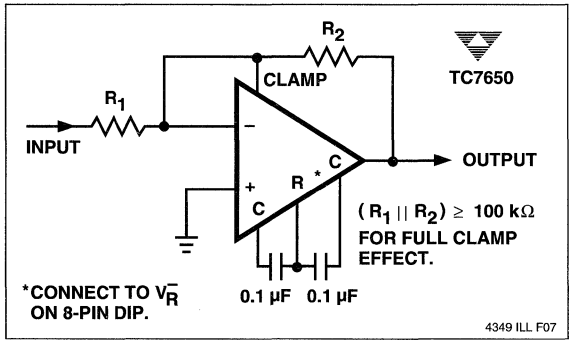


Figure 5 Inverting Amplifier With Optional Clamp

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. Output voltage versus clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Converters
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Thermoelectric Potentials

Precision DC measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages, typically around 0.1 µV/°C, but up to tens of µV/°C for some materials, will be generated. In order to realize the benefits extremely-low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-DIP TC7650, the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null potentiometer between pins 1 and 8 by two capacitors from the pins to V_S^- will convert the OP05/07 pin configurations for TC7650 operation. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are modified similarly by removing any circuit connections to pin 5. On the TC7650, pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offst or compensation point.

The minor modifications needed to retrofit a TC7650 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straightforward.

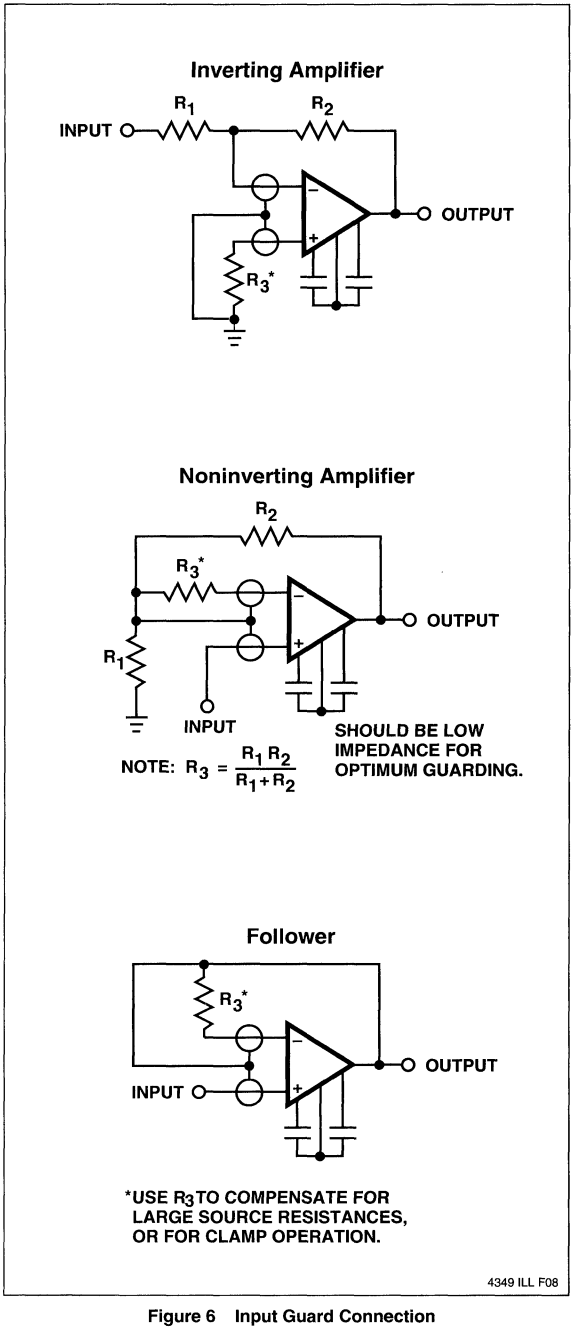


Figure 6 Input Guard Connection

Input Guarding

High impedance, low leakage CMOS inputs allow the TC7650 to make measurements of high-impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive PC trace surrounding the input terminals. The ring connects to a low-impedance point at the same potential as the inputs. Stray leakages are absorbed by the low-impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

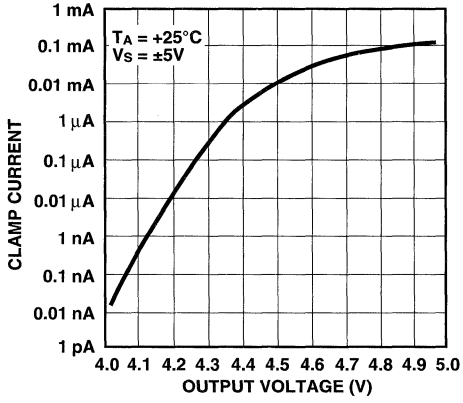
In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.

Component Selection

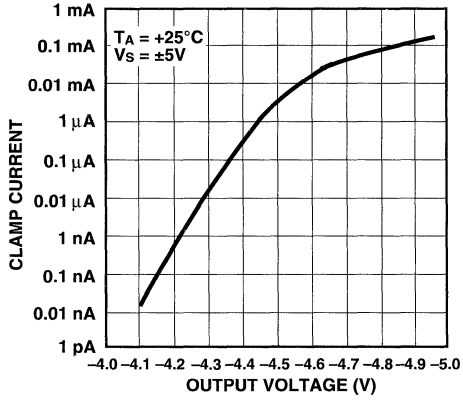
The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality film-type capacitors (such as Mylar) are preferred; ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

TYPICAL CHARACTERISTIC CURVES

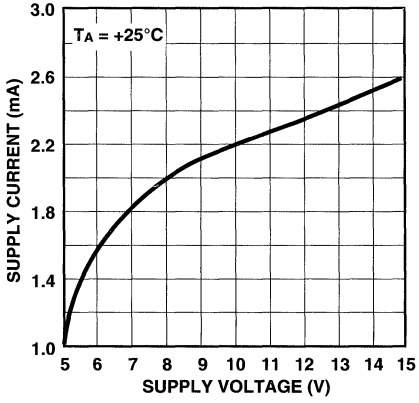
Positive Clamp Current vs Output Voltage



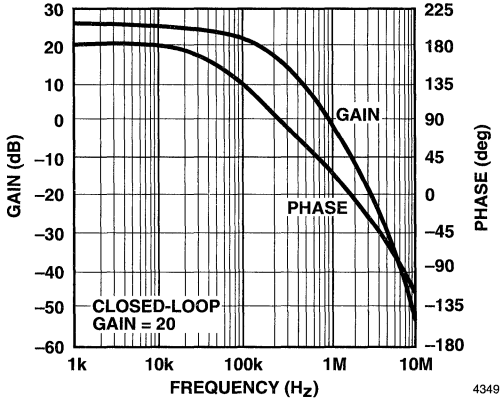
Negative Clamp Current vs Output Voltage



Supply Current vs Supply Voltage



Gain/Phase vs Frequency



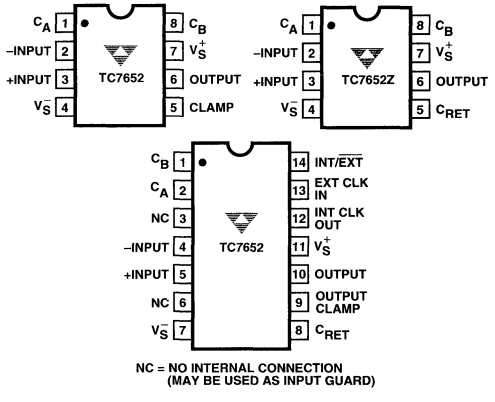
4349 ILL F10

LOW NOISE, CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- **Low Offset Over Temperature Range ..... 10 μV**
- **Ultra-Low Long-Term Drift ..... 150 nV/Month**
- **Low Temperature Drift ..... 100 nV/°C**
- **Low DC Input Bias Current ..... 15 pA**
- **High Gain, CMRR and PSRR ..... 110 dB Min**
- **Low Input Noise Voltage ..... 0.2 μV_{P-P}; DC to 1 Hz**
- **Internally-Compensated for Utility-Gain Operation**
- **Clamp Circuit for Fast Overload Recovery**

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION
(MAY BE USED AS INPUT GUARD)

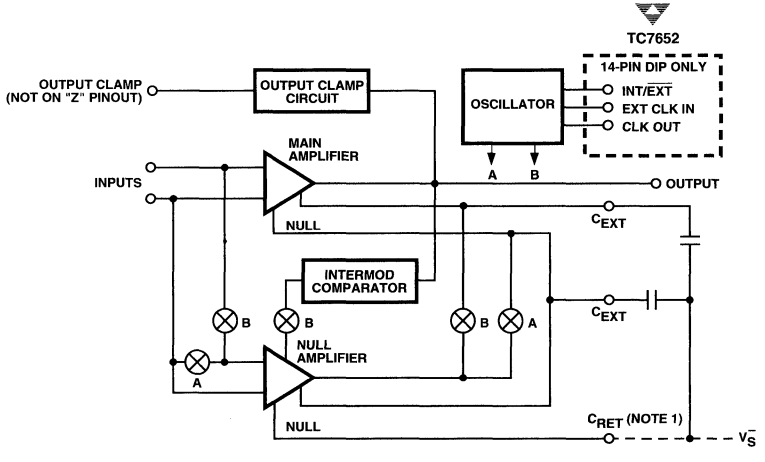
GENERAL DESCRIPTION

The TC7652 is a lower noise version of the TC7650, sacrificing some input specifications (bias current and bandwidth) to achieve a 10x reduction in noise. All the other benefits of the chopper technique are present, i.e. freedom from offset adjust, drift, and reliability problems from external trim components. Like the TC7650, the TC7652 requires only two noncritical external caps for storing the chopped null potentials. There are no significant chopping spikes, internal effects or overrange lockup problems.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7652CPA	8-Pin Plastic DIP	0°C to +70°C
TC7652ZCPA	8-Pin Plastic DIP	0°C to +70°C
TC7652IJA	8-Pin CerDIP	– 25°C to +85°C
TC7652CPD	14-Pin Plastic DIP	0°C to +70°C
TC7652IJD	14-Pin CerDIP	– 25°C to +85°C
TC7652ZIJA	8-Pin CerDIP	– 25°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. For 8-pin DIP connect to V_S^-, or to C_{RET} on "Z" pinout.

*Patented

TC7652

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +18V
Input Voltage ..... (V_S^+ + 0.3V) to (V_S^- – 0.3V)
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Duration of Output Short Circuit ..... Indefinite
Current Into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 µA

Continuous Total Power Dissipation (T_A = 25°C)
CerDIP ..... 500 mW
Plastic DIP ..... 375 mW
Storage Temperature Range ..... – 65°C to +150°C
Operating Temperature Range
C Device ..... 0°C to +70°C
I Device ..... – 25°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = – 5V, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage	T_A = +25°C Over Operating Temperature Range (Note 1)		±2 ±10	±5	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	Operating Temperature Range (Note 1)		0.01	0.05	µV/°C
$V_{OS}/\Delta T$	Offset Voltage vs Time			150		nV/mo
I_{BIAS}	Input Bias Current (CLK On)	T_A = +25°C 0°C < T_A < +70°C – 25°C < T_A < +85°C		30 100 250	100 1000	pA pA pA
I_{BIAS}	Input Bias Current (CLK Off)	T_A = +25°C 0°C < T_A < +70°C – 25°C < T_A < +85°C		15 35 100	30	pA pA pA
I_{OS}	Input Offset Current	T_A = +25°C		25	150	pA
R_{IN}	Input Resistance			10^{12}		Ω
OL	Large Signal Voltage Gain	R_L = 10 kΩ V_{OUT} = ±4V	120	150		dB
V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ R_L = 100 kΩ	±4.7	±4.85 ±4.95		V V
CMVR	Common-Mode Voltage Range		– 4.3		+3.5	V
MRR	Common-Mode Rejection Ratio	CMVR = – 4.3V to +3.5V	120	140		dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	120	140		dB
e_N	Input Noise Voltage	R_S = 100Ω, DC to 1 Hz DC to 10 Hz		0.2 0.7	1.5 5	μV_{P-P} μV_{P-P}
I_N	Input Noise Current	f = 10 Hz		0.01		$pA/\sqrt{Hz}$
GBW	Unity-Gain Bandwidth			0.4		MHz
SR	Slew Rate	C_L = 50 pF, R_L = 10 kΩ		1		V/µs
	Overshoot			15		%
V_S^+, V_S^-	Operating Supply Range		5		16	V
I_S	Supply Current	No Load		1	3	mA
f_{CH}	Internal Chopping Frequency	Pins 12 – 14 Open (DIP)	100	275		Hz
	Clamp ON Current (Note 2)	R_L = 100 kΩ	25	100		µA
	Clamp OFF Current (Note 2)	– 4V ≤ V_{OUT} < +10V		1		pA

NOTES: 1. –25°C to +85°C, or 0°C to +70°C.
2. See "Output Clamp" under detailed description.
3. Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems. Typically, 1 mA is safe; however, this is not guaranteed.

Capacitor Connection

Connect the null-storage capacitors to the C_A and C_B pins with a common connection to the C_{RET} pin (14-pin TC7652 or 8-pin TC7652Z) or to V_S^- (8-pin TC7652). When connecting to V_S^-, avoid injecting load current IR drops into the capacitive circuitry by making this connection directly via a separate wire or PC trace.

Output Clamp

In chopper-stabilized amplifiers, the output clamp pin reduces overload recovery time. When a connection is made to the inverting input pin (summing junction), a current path is created between that point and the output pin, just before the device output saturates. This prevents uncontrolled differential input voltages and charge buildup on correction-storage capacitors. Output swing is reduced.

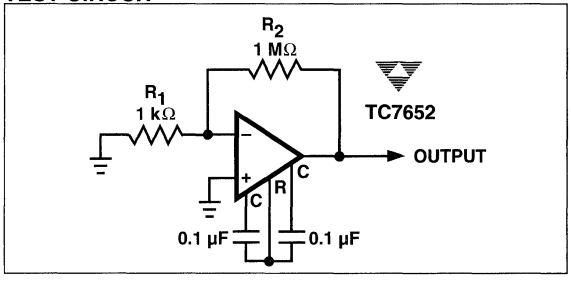
Clock

The TC7652 has a 550 kHz internal oscillator, which is divided by two before clocking the input chopper switches. The 275 Hz chopping frequency is available at INT CLK OUT (pin 12) on 14-pin devices. In normal operation, INT/EXT (pin 14), which has an internal pull-up, can be left open.

An external clock can also be used. To disable the internal clock and use an external one, the INT/EXT pin must be tied to V_S^-. The external clock signal is then applied to the EXT CLK IN input (pin 13). An internal divide-by-two provides a 50% switching duty cycle. The capacitors are only charged when EXT CLK IN is high, so a 50% to 80% positive duty cycle is recommended for higher clock frequencies. The external clock can swing between V_S^+ and V_S^-, with the logic threshold about 2.5V below V_S^+.

The output of the internal oscillator, before the divide-by-two circuit, is available at EXT CLK IN when INT/EXT is high or unconnected. This output can serve as the clock input for a second TC7652 (operating in a master/slave mode), so that both op amps will clock at the same frequency. This prevents clock intermodulation effects when two TC7652's are used in a differential amplifier configuration.

TEST CIRCUIT



If the TC7652's output saturates, error voltages on the external capacitors will slow overload recovery. This condition can be avoided if a strobe signal is available. The strobe signal is applied to EXT CLK IN and the overload signal is applied to the amplifier while the strobe is LOW. In this case, neither capacitor will be charged. The low leakage of the capacitor pins allow long measurements to be made with negligible errors (typical capacitor drift is 10 µV/sec).

APPLICATION NOTES

Component Selection

C_A and C_B (external capacitors) should be in the 0.1 µF to 1 µF range. For minimum clock ripple noise, use a 1 µF capacitor in broad bandwidth circuits. For limited bandwidth applications where clock ripple is filtered out, use a 0.1 µF capacitor for slightly lower offset voltage. High-quality film-type capacitors (polyester or polypropylene) are recommended, although a lower grade (ceramic) may work in some applications. For quickest settling after initial turn-on, use low dielectric absorption capacitors (e.g., polypropylene). With ceramic capacitors, settling to 1 µV takes several seconds.

Static Protection

Although input diodes static-protect all device pins, avoid strong electrostatic fields and discharges that can cause degraded diode junction characteristics and produce increased input-leakage currents.

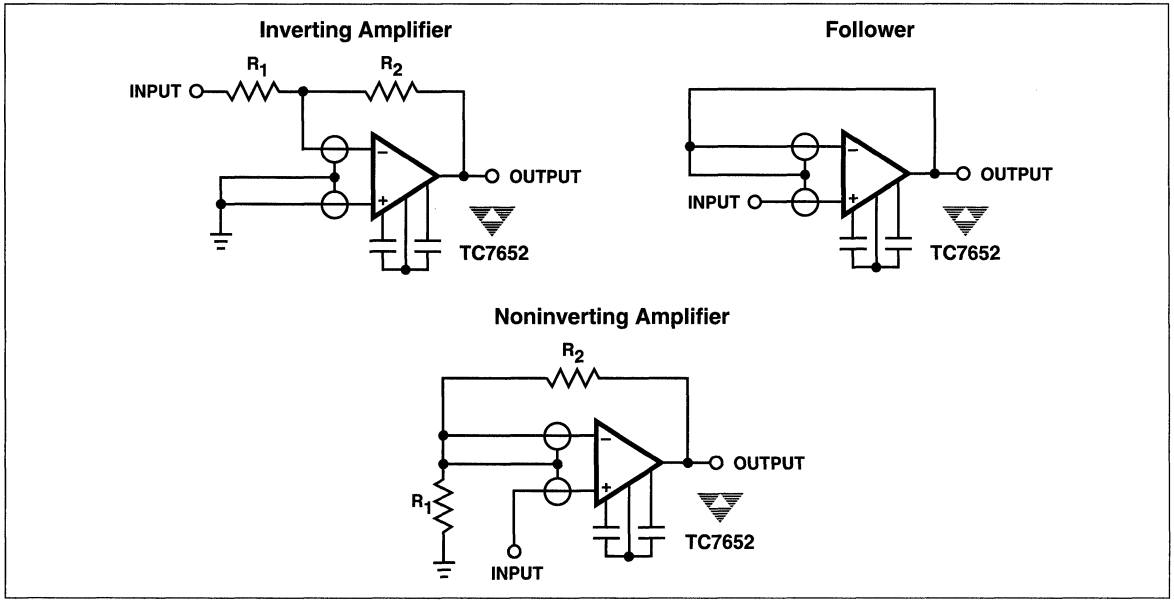
Latch-Up

Junction-isolated CMOS circuits have a 4-layer (p-n-p-n) structure similar to an SCR. Sometimes this junction can be triggered into a low-impedance state and produce excessive supply current. Therefore, avoid applying voltage greater than 0.3V beyond the supply rails to any pin. Establish the amplifier supplies at the same time or before any input signals are applied. If this is not possible, drive circuits must limit input current flow to under 1 mA to avoid latch-up, even under fault conditions.

Output Stage/Load Driving

The output circuit is high impedance (about 18 kW). With lesser loads, the chopper amplifier behaves somewhat like a transconductance amplifier with an open-loop gain proportional to load resistance. (For example, the open-loop gain is 17 dB lower with a 1 kW load than with a 10 kW load.) If the amp is used only for DC, the DC gain is typically greater than 120 dB (even with a 1 kW load), and this lower gain is inconsequential. For wideband, the best frequency response occurs with a load resistor of at least 10 kW. This produces a 6 dB/octave response from 0.1 Hz to 2 MHz, with phase

CONNECTION OF INPUT GUARDS



shifts of less than 2 degrees in the transition region, where the main amplifier takes over from the null amplifier.

Thermoelectric Effects

The thermoelectric (Peltier) effects in thermocouple junctions of dissimilar metals, alloys, silicon, etc. limit ultra-high-precision DC amplifiers. Unless all junctions are at the same temperature, thermoelectric voltages around 0.1 μV/°C (up to tens of μV/°C for some materials) are generated. To realize the low offset voltages of the chopper, avoid temperature gradients. Enclose components to eliminate air movement, especially from power-dissipating elements in the system. Where possible, use low thermoelectric-coefficient connections. Keep power supply voltages and power dissipation to a minimum. Use high-impedance loads and seek maximum separation from surrounding heat-dissipating elements.

Guarding

To benefit from TC7652 low-input currents, take care assembling printed circuit boards. Clean boards with alcohol or TCE, and blow dry with compressed air. To prevent contamination, coat boards with epoxy or silicone rubber.

Even if boards are cleaned and coated, leakage currents may occur because input pins are next to pins at supply potentials. To reduce this leakage, use guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard (a conductive ring surrounding inputs) is connected to a low-impedance point at about the same voltage as inputs. Then the guard absorbs leakage currents from high-voltage pins.

The 14-pin dual-in-line arrangement simplifies guarding. Like the LM108 pin configuration (but unlike the 101A and 741), pins next to inputs are not used.

Pin Compatibility

Where possible, the 8-pin device basic pinout conforms to such industry standards as the LM101 and LM741. Null-storing external capacitors connect to pins 1 and 8, which are usually for offset-null or compensation capacitors. Output clamp (pin 5) is similarly used. For OP05 and OP07 devices, replacement of the offset-null potentiometer (connected between pins 1 and 8 and V_S^+ by two capacitors from those pins to V_S^-) provides compatibility. Replacing the compensation capacitor between pins 1 and 8 by two capacitors to V_S^- is required. The same operation (with the removal of any connection to pin 5) works for LM101, μA748, and similar parts.

Because NC pins provide guarding between input and other pins, the 14-pin device pinout conforms closely to the LM108. Because this device does not use any extra pins and does not provide offset-nulling (but requires a compensation capacitor), some layout changes are necessary to convert to the TC7652.

Some Applications

Figures 1 and 2 show basic inverting and noninverting amplifier circuits using the output clamping circuit to enhance overload recovery performance. The only limitations on replacing other op amps with the TC7652 are supply voltage (±8V maximum) and output drive capability (10 kΩ load for full swing). Overcome these limitations with a booster circuit (Figure 3) to combine output capabilities of the LM741 (or other standard device) with input capabilities of the TC7652. These two form a composite device; therefore, when adding the feedback network, monitor loop gain stability.

Figure 4 shows the clamp circuit of a zero-offset comparator. Because the clamp circuit requires the inverting input to follow the input signal, problems with a chopper-stabilized op amp are avoided. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disrupting other parts of the system.

Figure 5 shows how the TC7652 can offset-null high slew-rate and wideband amplifiers.

Mixing the TC7652 with circuits operating at ±15V requires a lower supply voltage divider with the TC7660 voltage converter circuit operated "backwards." Figure 6 shows an approximate connection.

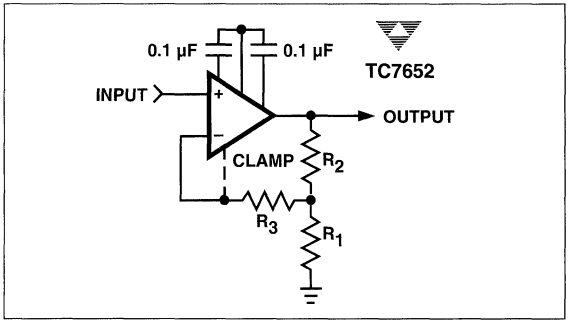


Figure 1 Noninverting Amplifier With Optional Clamp

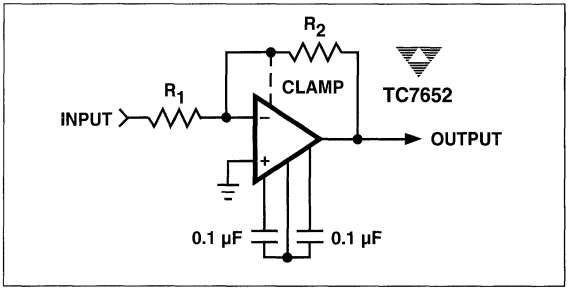


Figure 2 Inverting Amplifier With Optional Clamp

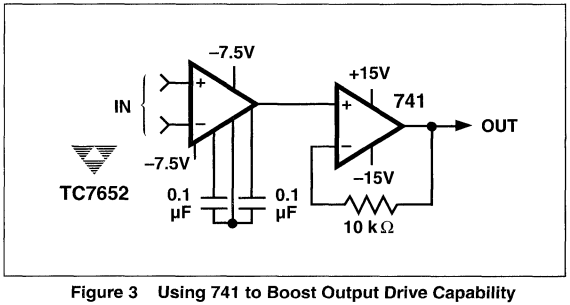


Figure 3 Using 741 to Boost Output Drive Capability

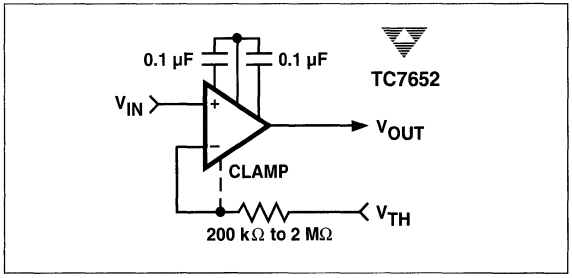


Figure 4 Low Offset Comparator

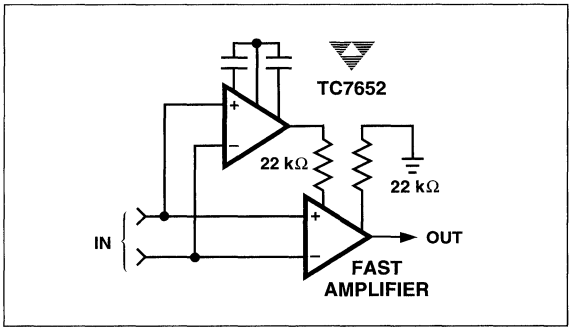


Figure 5 1437 Offset-Nulled by TC7652

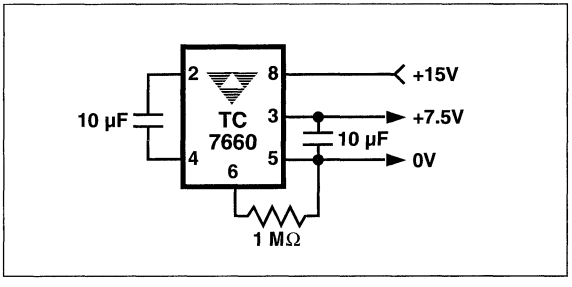
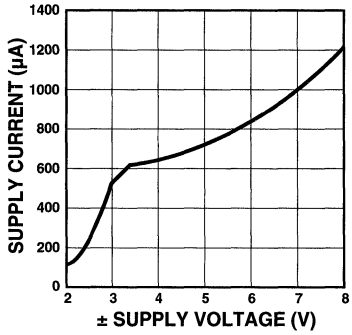


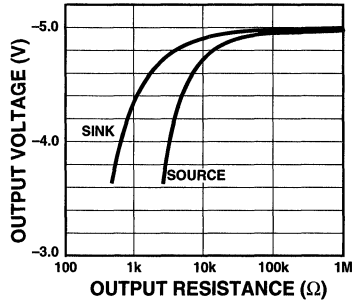
Figure 6 Splitting +15V With the 7660 at >95% Efficiency

TYPICAL CHARACTERISTICS CURVES

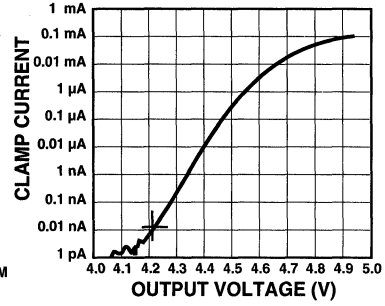
Supply Current vs ± Supply Voltage



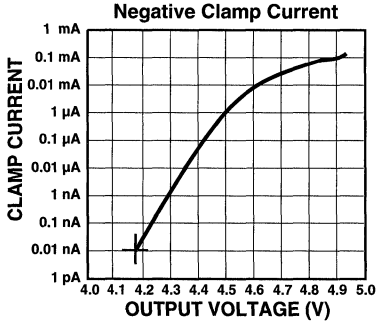
Output Resistance vs Output Voltage



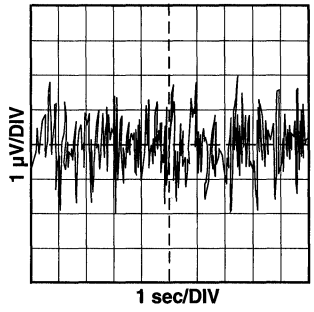
Positive Clamp Current



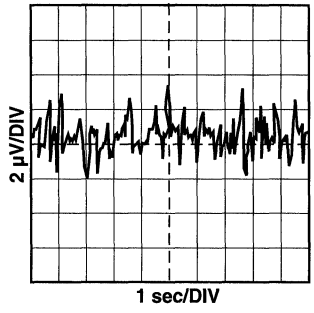
Negative Clamp Current



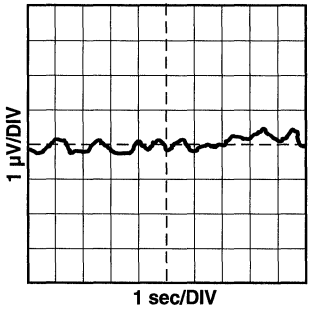
Noise at 0.1 Hz to 100 Hz



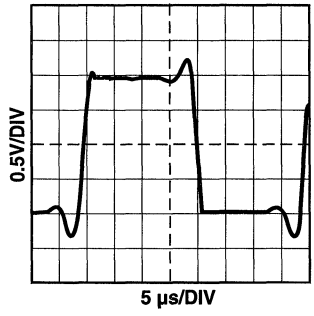
Noise at 0.1 Hz to 10 Hz



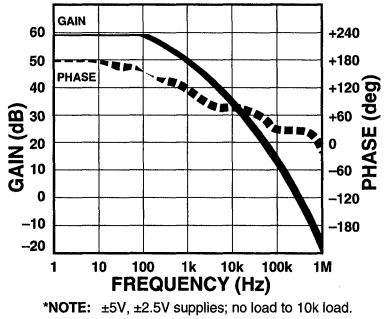
Noise at 0.1 Hz to 1 Hz



Slew Rate

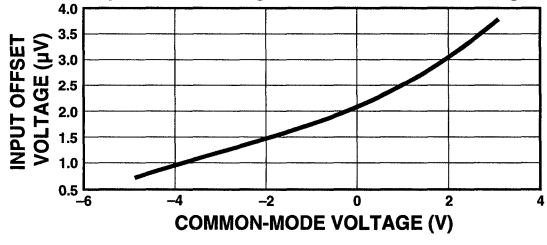


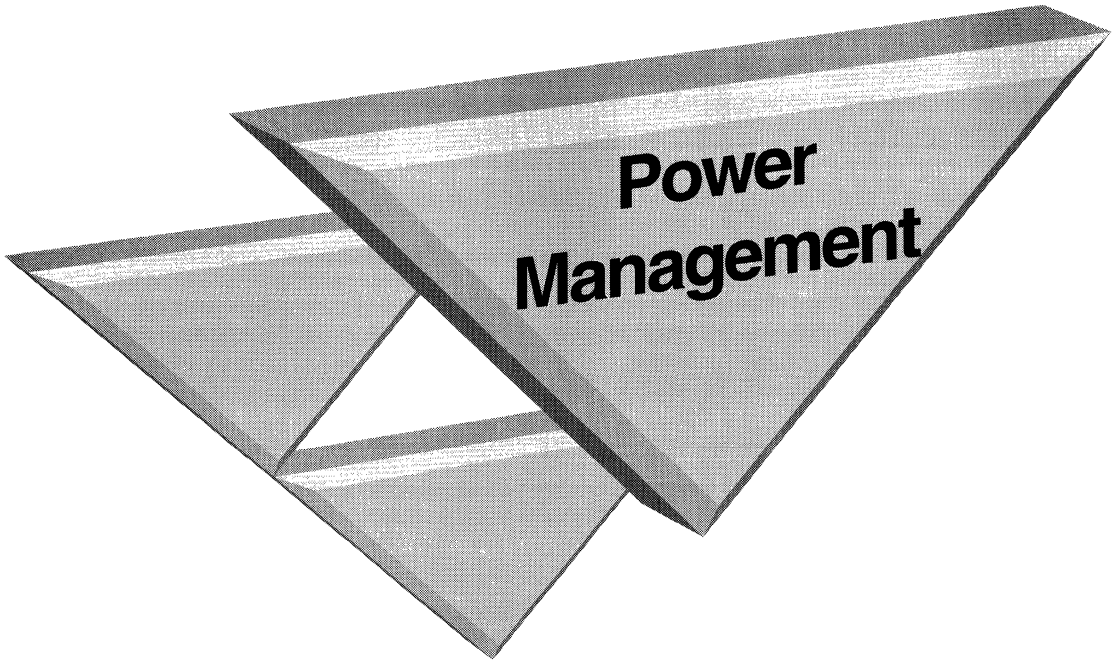
Phase-Gain (Bode Plot)*



*NOTE: ±5V, ±2.5V supplies; no load to 10k load.

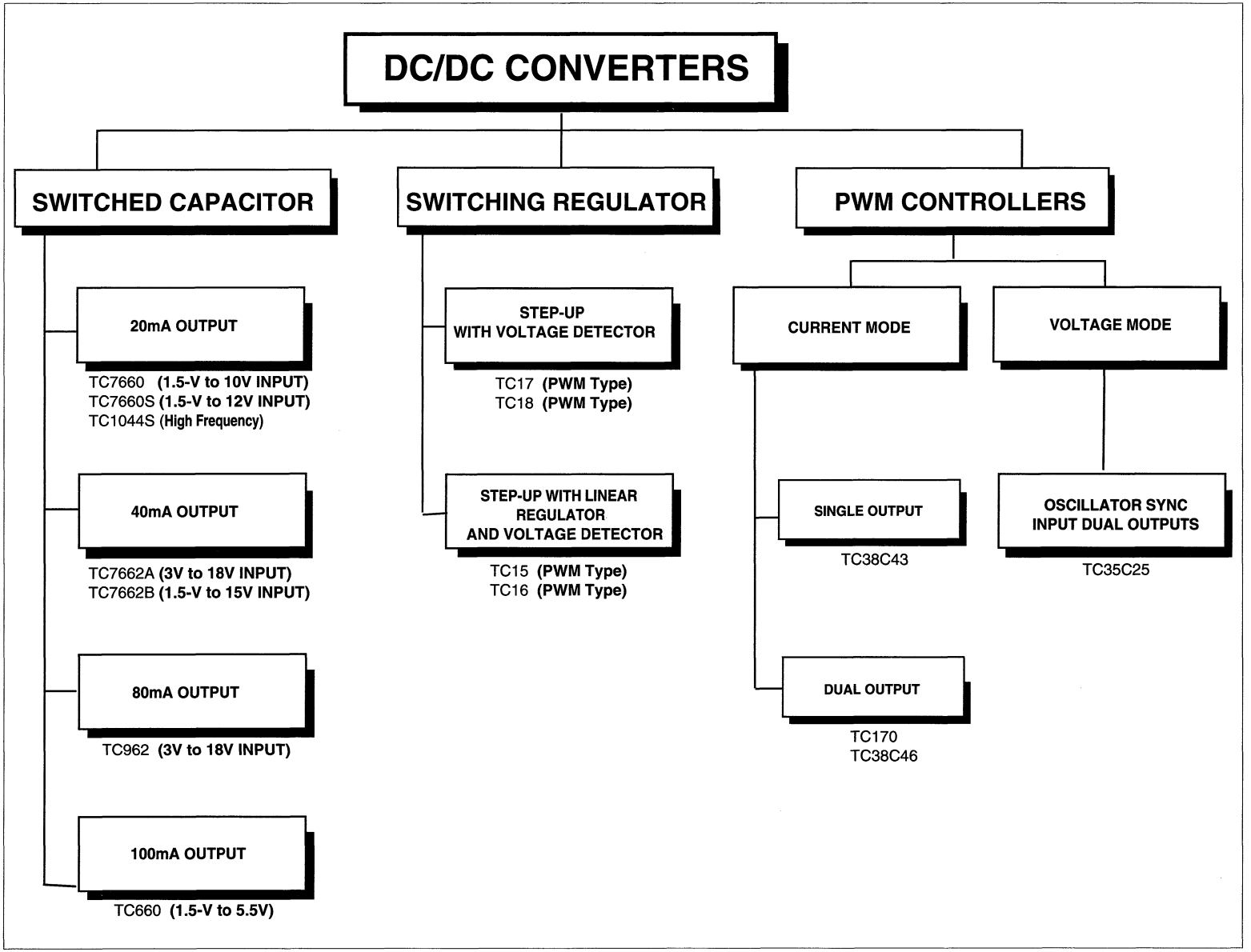
Input Offset Voltage vs Common-Mode Voltage

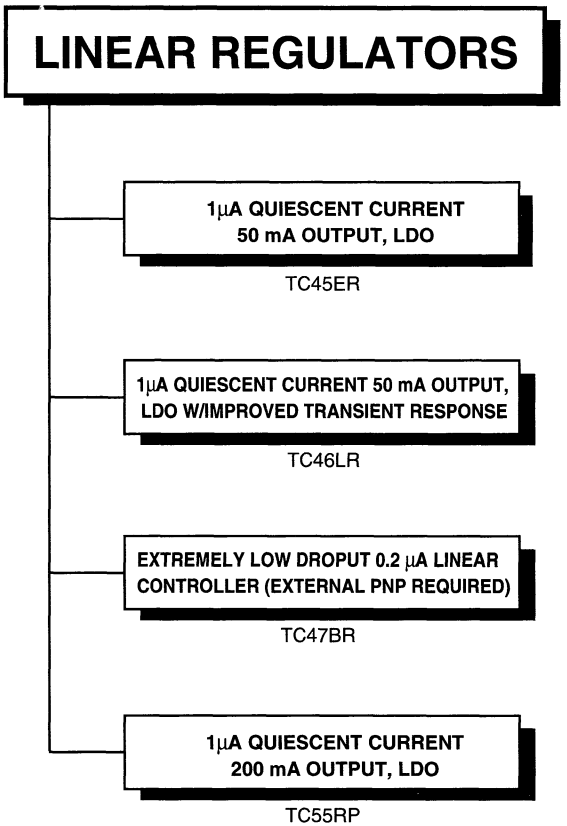


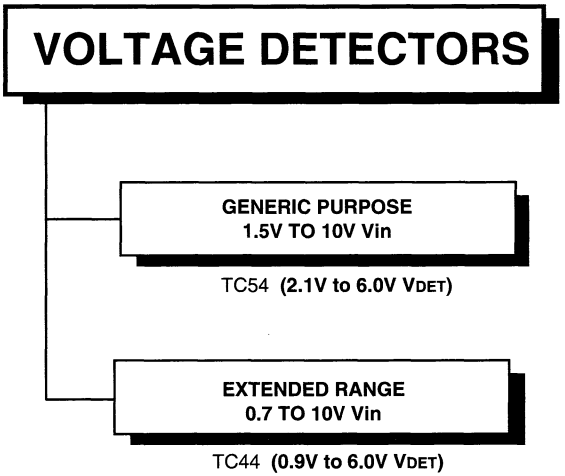


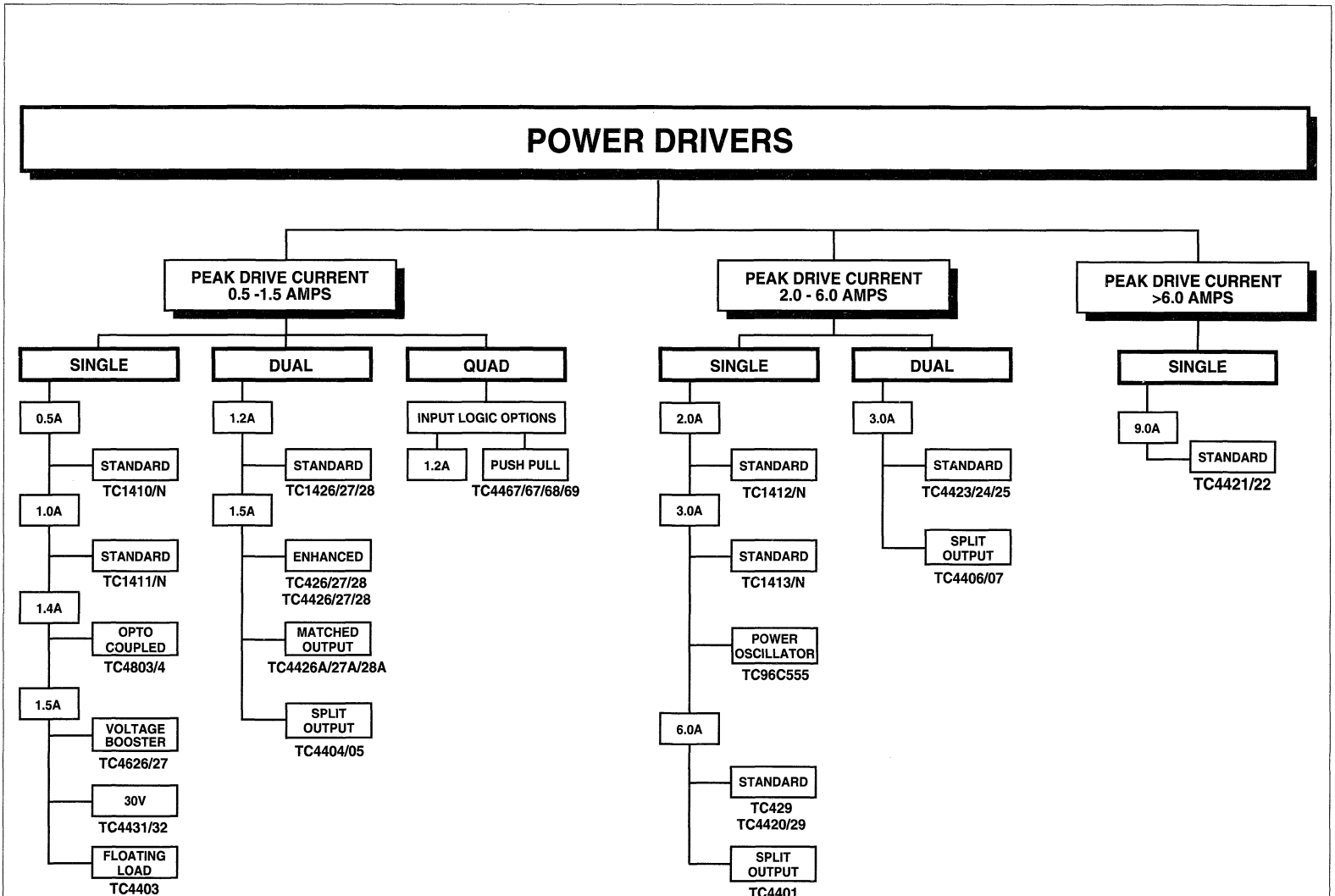
3

- **DC/DC Converters**
  - Switched Capacitor
  - Switching Regulators
  - PMW Controllers
- **Voltage Detectors**
- **Voltage Regulators**
- **Power MOSFET, Motor and PIN Drivers**


DC/DC CONVERTERS
SWITCHED CAPACITOR
SWITCHING REGULATOR
PWM CONTROLLERS
20mA OUTPUT
TC7660 (1.5-V to 10V INPUT)
TC7660S (1.5-V to 12V INPUT)
TC1044S (High Frequency)
40mA OUTPUT
TC7662A (3V to 18V INPUT)
TC7662B (1.5-V to 15V INPUT)
80mA OUTPUT
TC962 (3V to 18V INPUT)
100mA OUTPUT
TC660 (1.5-V to 5.5V)
STEP-UP WITH VOLTAGE DETECTOR
TC17 (PWM Type)
TC18 (PWM Type)
STEP-UP WITH LINEAR REGULATOR AND VOLTAGE DETECTOR
TC15 (PWM Type)
TC16 (PWM Type)
CURRENT MODE
VOLTAGE MODE
SINGLE OUTPUT
TC38C43
DUAL OUTPUT
TC170
TC38C46
OSCILLATOR SYNC INPUT DUAL OUTPUTS
TC35C25


LINEAR REGULATORS
1µA QUIESCENT CURRENT
50 mA OUTPUT, LDO
TC45ER
1µA QUIESCENT CURRENT 50 mA OUTPUT,
LDO W/IMPROVED TRANSIENT RESPONSE
TC46LR
EXTREMELY LOW DROPUT 0.2 µA LINEAR
CONTROLLER (EXTERNAL PNP REQUIRED)
TC47BR
1µA QUIESCENT CURRENT
200 mA OUTPUT, LDO
TC55RP


VOLTAGE DETECTORS
GENERIC PURPOSE
1.5V TO 10V Vin
TC54 (2.1V to 6.0V VDET)
EXTENDED RANGE
0.7 TO 10V Vin
TC44 (0.9V to 6.0V VDET)


POWER DRIVERS
PEAK DRIVE CURRENT 0.5 -1.5 AMPS
PEAK DRIVE CURRENT 2.0 - 6.0 AMPS
PEAK DRIVE CURRENT >6.0 AMPS
SINGLE
DUAL
QUAD
SINGLE
DUAL
SINGLE
0.5A
STANDARD
TC1410/N
1.0A
STANDARD
TC1411/N
1.4A
OPTO COUPLED
TC4803/4
1.5A
VOLTAGE BOOSTER
TC4626/27
30V
TC4431/32
FLOATING LOAD
TC4403
1.2A
STANDARD
TC1426/27/28
1.5A
ENHANCED
TC426/27/28
TC4426/27/28
MATCHED OUTPUT
TC4426A/27A/28A
SPLIT OUTPUT
TC4404/05
INPUT LOGIC OPTIONS
1.2A
PUSH PULL
TC4467/67/68/69
2.0A
STANDARD
TC1412/N
3.0A
STANDARD
TC1413/N
POWER OSCILLATOR
TC96C555
6.0A
STANDARD
TC429
TC4420/29
SPLIT OUTPUT
TC4401
3.0A
STANDARD
TC4423/24/25
SPLIT OUTPUT
TC4406/07
9.0A
STANDARD
TC4421/22

STEP-UP/STEP-DOWN PWM DC/DC CONVERTER WITH VOLTAGE DETECTOR

FEATURES

- **Low quiescent current ..... typ 50µA (TC151A/1B3624; V_{IN} = 3.0V, No Load)**
- **Low standby current ..... 1A version 1.0µA MAX 1B version 10.0µA MAX**
- **Low voltage operation ..... V_{IN} = 1.2 to 10V**
- **High accuracy output voltage ..... ±2.5%**
- **Wide choice of V_{OUT} ..... 1.5V to 6.0V in 0.1V Steps**
- **Wide choice of V_{DET} ..... 1.2V to 5.0V in 0.1V Steps**
- **Soft start and driver protection circuit**
- **Phase compensation circuit**
- **Small package ..... 8-Pin SOIC**
- **Larger current can be obtained by connecting an external power transistor**

APPLICATIONS

- **Laptop computers**
- **Portable equipment**
- **Pagers, cellular and cordless telephones**
- **Cameras and hand-held systems**

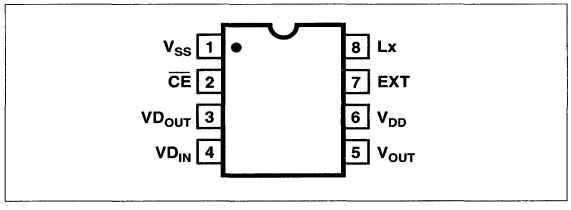
GENERAL DESCRIPTION

The TC15 Series are CMOS power-supply ICs containing a low-dropout linear regulator, an under-voltage detector, and a PWM DC/DC step-up (boost) converter. In normal operation (V_{IN} well above V_{OUT}), the device functions as a linear regulator. When V_{IN} drops below V_{IN} (min.) or less, the voltage detector (V_{DET}) senses this and turns on the boost converter that raises V_{IN} back up to the linear regulator's operating range. The TC15 thus extends battery life considerably by allowing the battery voltage to drop to formerly unusable levels.

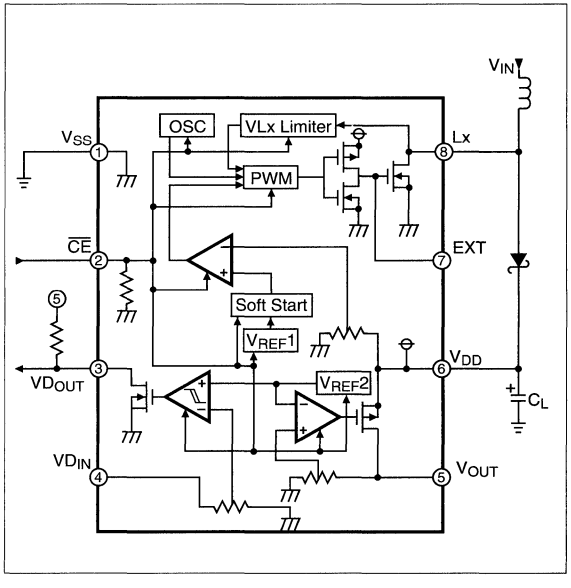
As a user-selected option, the chip-enable pin, $\overline{CE}$, can shut down the entire IC (option A) or just the boost converter (option B), leaving the voltage detector active.

3

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

The range for V_{OUT} is 1.5V to 6.0V, and that for V_{DET} is 1.2V to 5.0V; both come in 0.1V increments, and are user-selected.

PART CODE TC15 XX XX XX X XX XXX

$\overline{CE}$ form: 1A*, 1B**

Output Voltage:
Ex: 15 = 1.5V; 60 = 6.0V

Detected Voltage:
Ex: 12 = 1.2V; 50 = 5.0V

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
OA: 8-Pin SOIC

Taping Direction:
723: Left Taping
713: Right Taping

* A: If $\overline{CE}$ is High (+V_{DD}) then whole chip is disabled.
**B: If $\overline{CE}$ is High (+V_{DD}) then only the DC/DC converter is disabled and the detector is still operational.

TC15 Series

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{IN}	– 0.3 to 12	V
Output Voltage of Lx pin	VLx	– 0.3 to 12	V
EXT pin	VEXT	– 0.3 to (V_{DD} + 0.3)	V
V_{OUT} pin	V_{OUT}	– 0.3 to (V_{DD} + 0.3)	V
VD_{OUT} pin	VD_{OUT}	– 0.3 to 12	V
Input Voltage of $\overline{CE}$ pin	$V\overline{CE}$	– 0.3 to (V_{DD} + 0.3)	V
VD_{IN} pin	VD_{IN}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V (ver. A)
		(V_{SS} – 0.3) to 12	V (ver. B)
Output Current of EXT pin	IEXT	50	mA
Lx pin	ILx	250	mA
Power Dissipation	Pd	300	mW
Operating Temperature	T_A	– 40 to +85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
Soldering Condition	T_{solder}	260° 10 sec	

ELECTRICAL CHARACTERISTICS:
TC151A/1B3624 (3.6V Output)

T_A = 25°C, V_{IN} = 4.1V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage	No Load	1.2		10	V
V_{DD}	Stepped-up Output Voltage	No Load	3.99	4.10	4.21	V
V_{OSCST}	Oscillator Start-up Voltage	No Load		0.9	1.2	V
f_{osc}	Oscillator Frequency		40	50	60	kHz
Maxdty	Maximum Oscillator Duty Cycle		65	80	90	%
V_{OL1}	Lx Output Voltage	I_{OL} = 50mA			0.5	V
I_{OH1}	Lx Leakage Current			0.01	10	µA
V_{LXlim}	Lx Voltage Limit	Lx pin ON		0.9		V
V_{OH}	EXT Output Pch ON Voltage	I_{EXT} = – 3mA, V_{IN} = 4.1V	3.6			V
V_{OL2}	EXT Output Nch ON Voltage	I_{EXT} = 5mA, V_{IN} = 4.1V			0.5	V
V_{OUT}	Output Voltage	I_{OUT} = 5mA	3.51	3.60	3.69	V
V_{DIF}	Dropout Voltage	I_{OUT} = 30mA		0.3		V
$\Delta V_{OUT}/I_{OUT}$	Load Regulation	– 30mA ≤ I_{OUT} ≤ 0mA			100	mV
$-V_{DET}$	Detector Threshold		2.34	2.4	2.46	V
V_{HYS}	Detector Threshold Hysteresis Range		60	120	240	mV
V_{OL3}	VD_{OUT} ON Voltage	I_{OL} = 5mA			0.5	V
I_{OH2}	VD_{OUT} Leakage Current			0.01	5	µA
I_{VDINH}	VD_{IN} "H" Input Current	VD_{IN} = V_{IN}			5	µA
I_{VDINL}	VD_{IN} "L" Input Current	VD_{IN} = V_{SS}	– 0.5		0.5	µA
V_{CEH}	$\overline{CE}$ "H" Input Voltage		V_{DD} – 0.3		V_{DD}	V
V_{CEL}	$\overline{CE}$ "L" Input Voltage		0		0.2 V_{DD}	V
I_{CEH}	$\overline{CE}$ "H" Input Current	$\overline{CE}$ = V_{IN}	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ "L" Input Current	$\overline{CE}$ = V_{SS}	– 0.5		0.5	µA
I_{DD}	Supply Current	V_{IN} = 3V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{SS}, No Load		55	120	µA
Istandby	Supply Current	V_{IN} = 3V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{DD}, No Load			1.0 10.0	µA[1] µA[2]

NOTES
[1] Standby current of version A (see "Ordering Information")
[2] Standby current of version B

ELECTRICAL CHARACTERISTICS: TC151A/1B5045 (5.0V Output)

T_A = 25°C, V_{IN} = 5.5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operation Input Voltage	No Load	1.2		10	V
V_{DD}	Step-up Output Voltage	No Load	5.36	5.5	5.64	V
V_{OSCST}	Oscillator Start-up Voltage	No Load		0.9	1.2	V
f_{osc}	Oscillator Frequency		40	50	60	kHz
Maxdty	Maximum Oscillator Duty Cycle		65	80	90	%
V_{OL1}	Lx Output Voltage	I_{OL} = 50mA			0.5	V
I_{OH1}	Lx Leakage Current			0.01	10	µA
V_{LXlim}	Lx Voltage Limit	Lx pin ON		0.9		V
V_{OH}	EXT Output Pch ON Voltage	I_{EXT} = – 3mA, V_{IN} = 5.5V	5.0			V
V_{OL2}	EXT Output Nch ON Voltage	I_{EXT} = 5mA, V_{IN} = 5.5V			0.5	V
V_{OUT}	Output Voltage	I_{OUT} = 5mA	4.87	5.0	5.13	V
V_{DIF}	Dropout Voltage	I_{OUT} = 30mA		0.3		V
$\Delta V_{OUT}/I_{OUT}$	Load Regulation	– 30mA ≤ I_{OUT} ≤ 0mA			100	mV
$-V_{DET}$	Detector Threshold		4.38	4.5	4.62	V
V_{HYS}	Detector Threshold Hysteresis Range		112	225	450	mV
V_{OL3}	VD_{OUT} ON Voltage	I_{OL} = 5mA			0.5	V
I_{OH2}	VD_{OUT} Leakage Current			0.01	5	µA
I_{VDINH}	VD_{IN} "H" Input Current	VD_{IN} = V_{IN}			5	µA
I_{VDINL}	VD_{IN} "L" Input Current	VD_{IN} = V_{SS}	– 0.5		0.5	µA
V_{CEH}	$\overline{CE}$ "H" Input Voltage		V_{DD} – 0.3		V_{DD}	V
V_{CEL}	$\overline{CE}$ "L" Input Voltage		0		0.2 V_{DD}	V
I_{CEH}	$\overline{CE}$ "H" Input Current	$\overline{CE}$ = V_{IN}	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ "L" Input Current	$\overline{CE}$ = V_{SS}	– 0.5		0.5	µA
I_{DD}	Supply Current	V_{IN} = 4V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{SS}, No Load		70	150	µA
Istandby	Supply Current	V_{IN} = 4V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{DD}, No Load			1.0 10.0	µA[1] µA[2]

NOTES
[1] Standby current of version A (see "Ordering Information")
[2] Standby current of version B

PIN DESCRIPTION

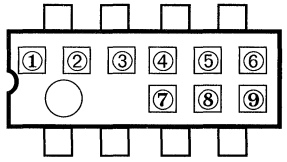
Pin No.	Symbol	Description
1	V_{SS}	Ground
2	$\overline{CE}$	Chip Enable. Set the pin to V_{DD} to change the device to standby state
3	VD_{OUT}	Output of voltage detector (NMOS open drain output)
4	VD_{IN}	Input to voltage detector

Pin No.	Symbol	Description
5	V_{OUT}	Output of voltage regulator
6	V_{DD}	Input to linear regulator from boost converter
7	EXT	Output drive for external PWM switch transistor
8	Lx	Input to internal switch (from L)

TC15 Series

MARKING

8 pin-SOIC



a & b represent 15: Fixed

c represents first digit of voltage

Mark c	Volt
1	1.d (V)
2	2.d (V)
3	3.d (V)
4	4.d (V)
5	5.d (V)
6	6.d (V)

d represents first decimal place of voltage

Mark d	Volt	Mark d	Volt
0	c.0 (V)	5	c.5 (V)
1	c.1 (V)	6	c.6 (V)
2	c.2 (V)	7	c.7 (V)
3	c.3 (V)	8	c.8 (V)
4	c.4 (V)	9	c.9 (V)

e represents detected voltage

Mark e	V_{DET}	Mark e	V_{DET}	Mark e	V_{DET}
0	1.2	C	2.9	R	5.0
1	1.5	D	3.0	S	1.3
2	1.8	E	3.1	T	3.7
3	1.9	F	3.3		
4	2.0	G	3.5		
5	2.1	H	3.6		
6	2.2	J	4.0		
7	2.4	K	4.1		
8	2.5	L	4.3		
9	2.6	M	4.5		
A	2.7	N	4.7		
B	2.8	O	4.8		

f represents $\overline{CE}$ version

Mark f	Version
A	A
B	B

g, h and i, represents assembly lot number

TEST CIRCUITS (Keyed to following graphs)

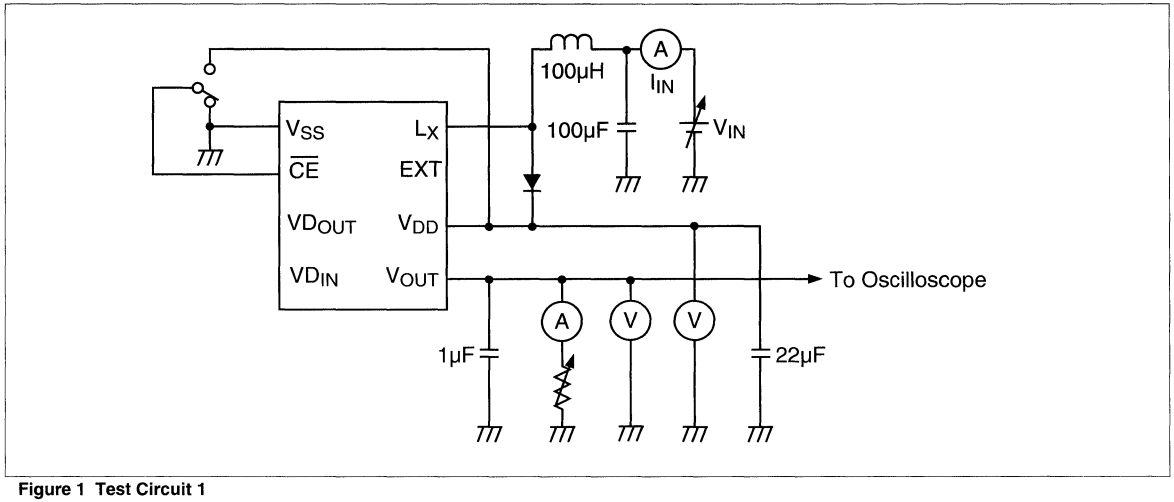


Figure 1 Test Circuit 1

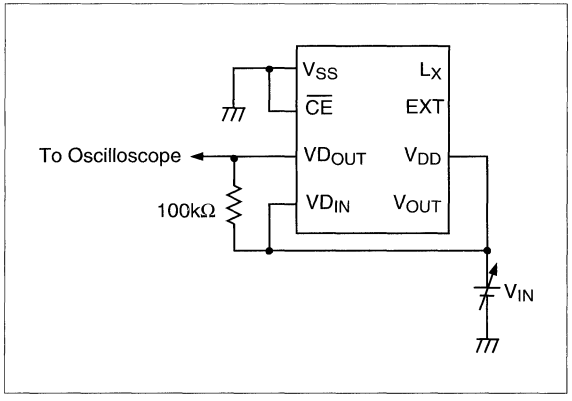


Figure 2 Test Circuit 2

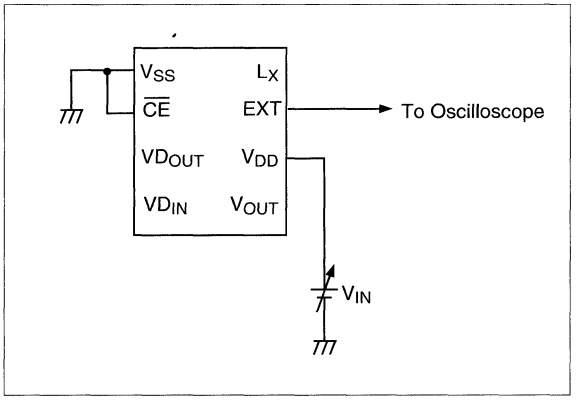


Figure 3 Test Circuit 3

Test Circuit 1 Applies to graphical characteristics 1) - 4), 7), 8) and 11) - 14)
[Change the 100µF capacitance to 1µF for characteristics 13) and 14)
STANDBY state: $\overline{CE} = V_{DD}$]

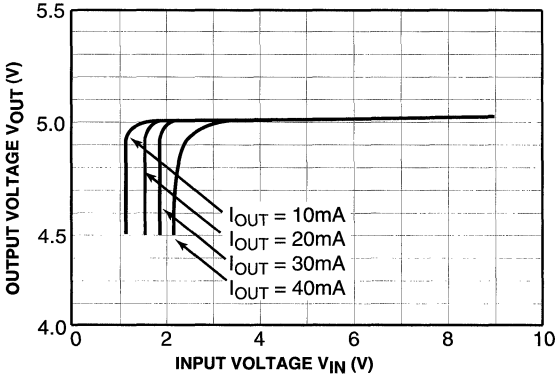
Test Circuit 2 Applies to graphical characteristics 9) and 10)

Test Circuit 3 Applies to graphical characteristics 5) and 6)
Definition of efficiency is as follows: $(V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN})$

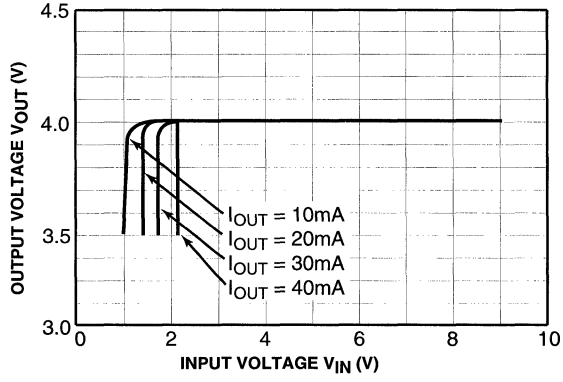
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Input Voltage

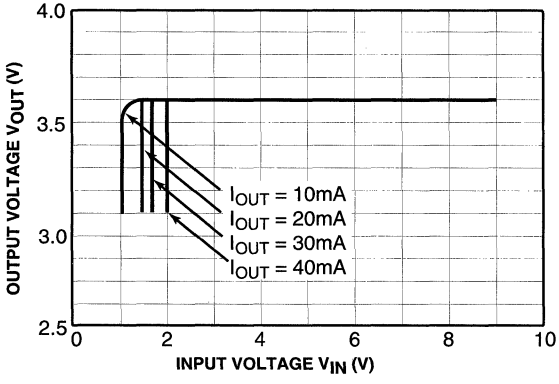
TC151A5045



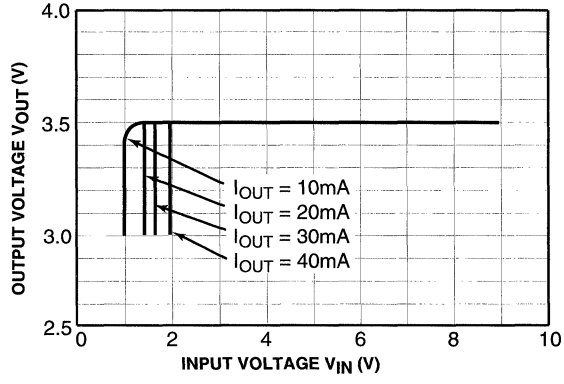
TC151A4036



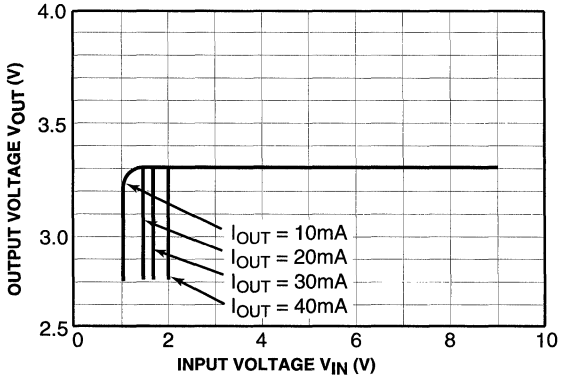
TC151A3624



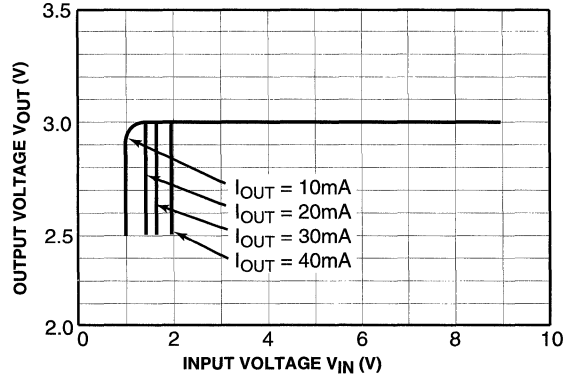
TC151A3531



TC151A3329



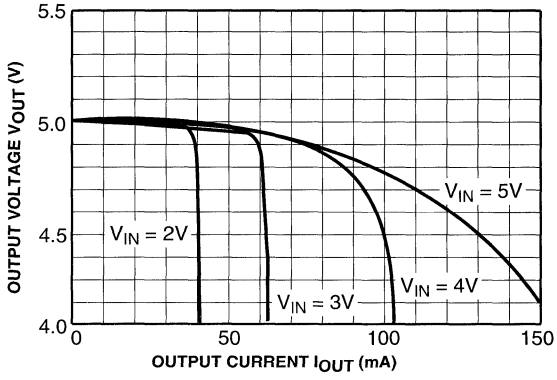
TC151A3027



TYPICAL CHARACTERISTICS

2) Output Voltage vs. Output Current (T_A = 25°C)

TC151A5045



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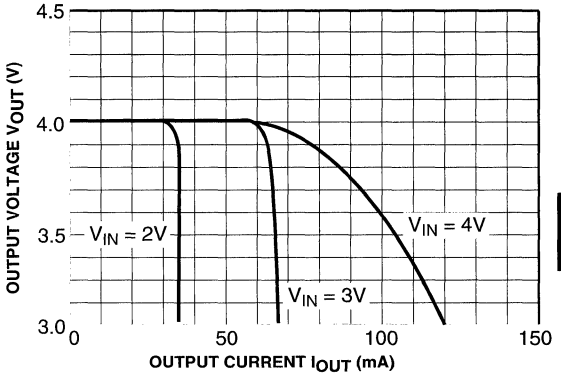
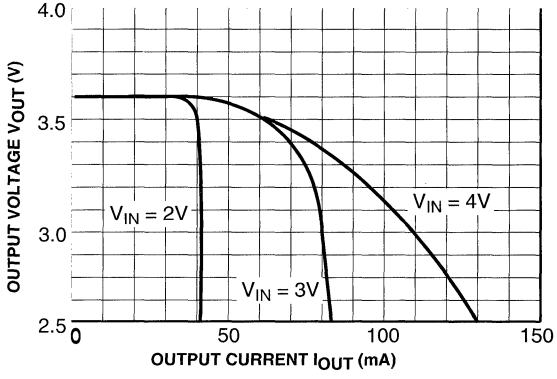


TC151A3624



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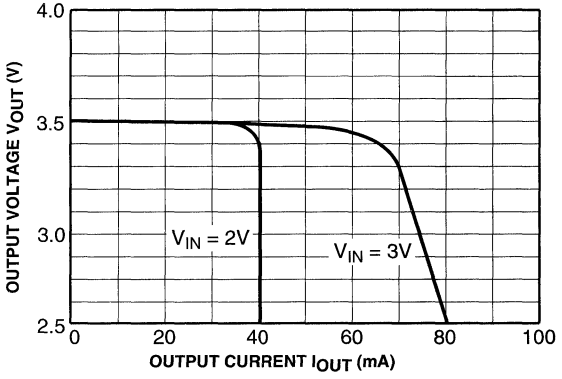
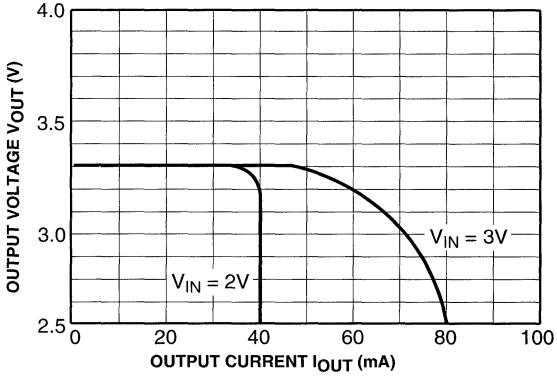
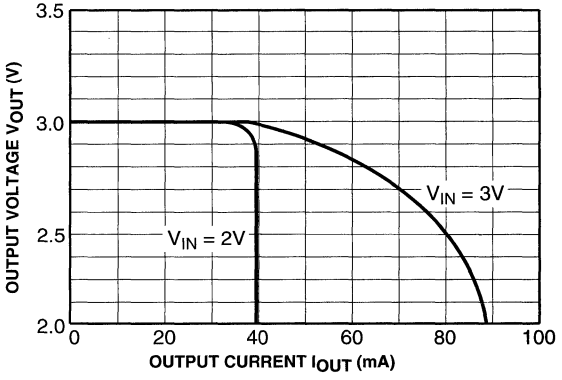


TC151A3329



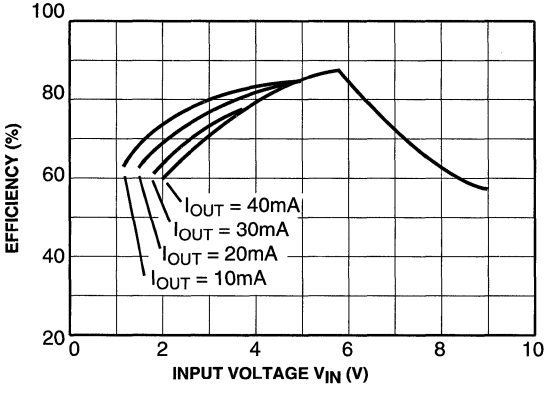
TC151A3027



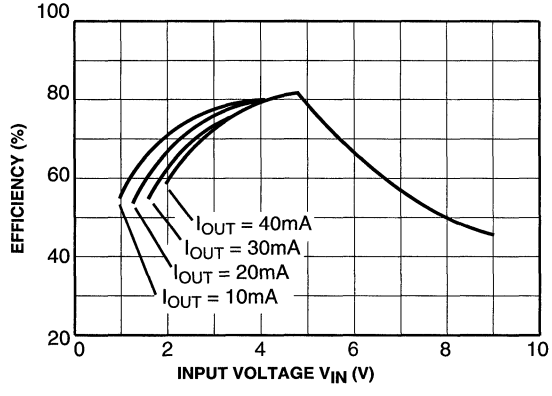
TYPICAL CHARACTERISTICS

3) Efficiency vs. Input Voltage (T_A = 25°C)

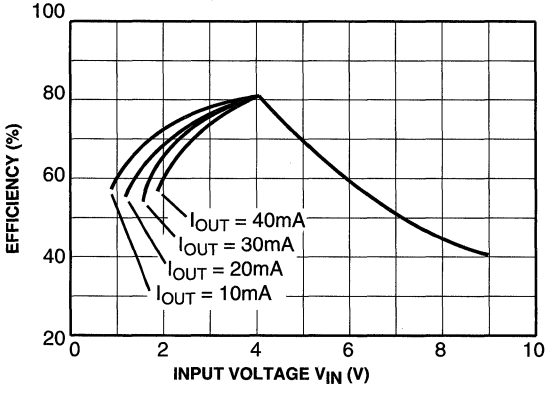
TC151A5045



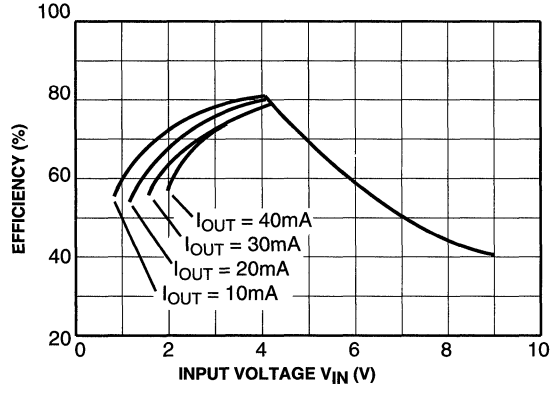
TC151A4036



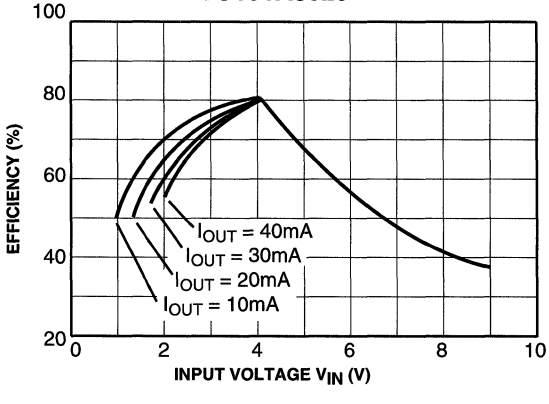
TC151A3624



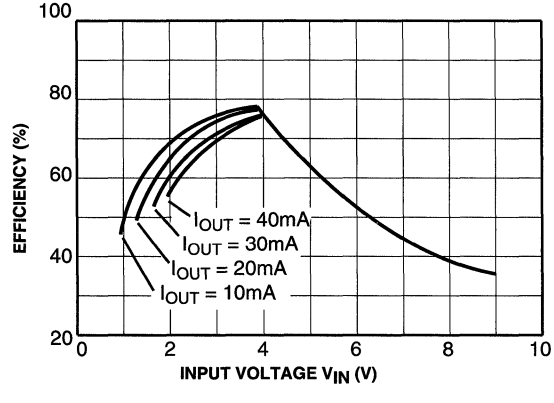
TC151A3531



TC151A3329



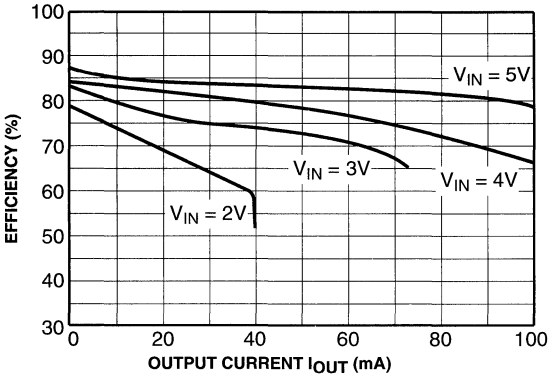
TC151A3027



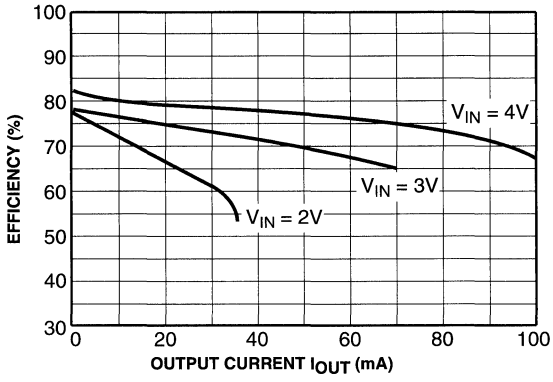
TYPICAL CHARACTERISTICS

4) Efficiency vs. Output Current (T_A = 25°C)

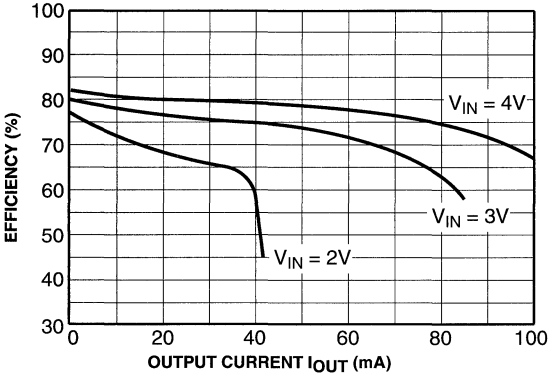
TC151A5045



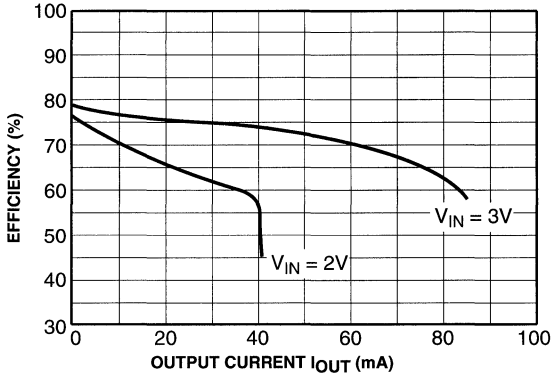
TC151A4036



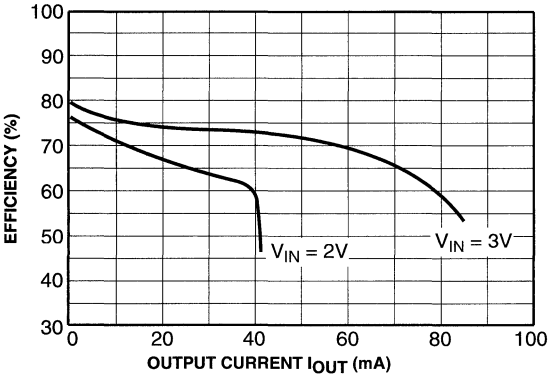
TC151A3624



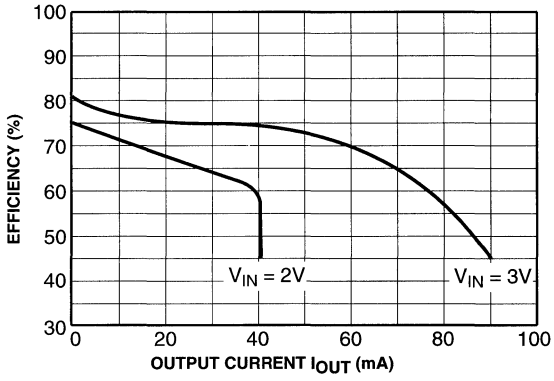
TC151A3531



TC151A3329



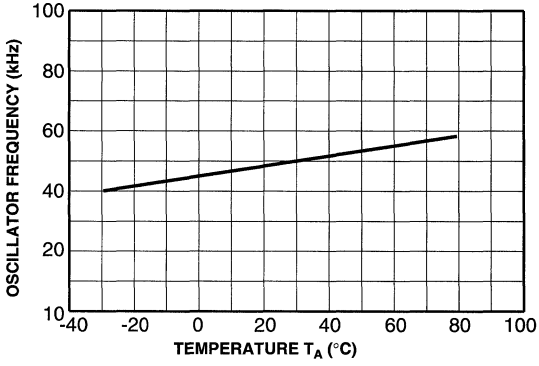
TC151A3027



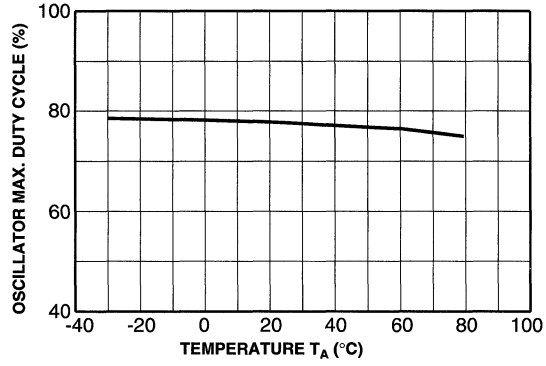
3

TYPICAL CHARACTERISTICS

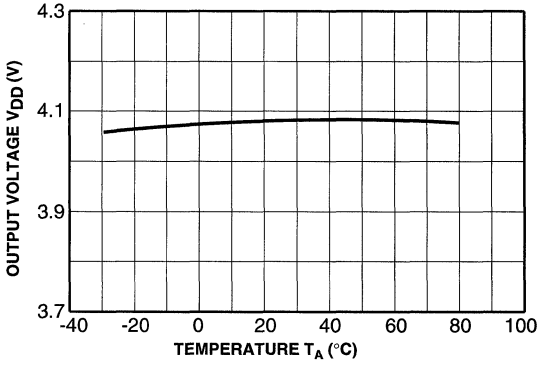
5) Oscillator Frequency vs. Temperature
TC151A3624



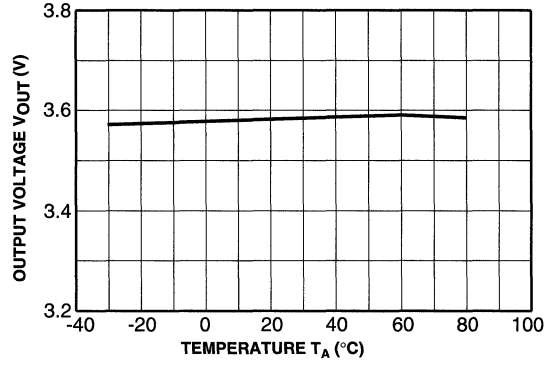
6) Oscillator Maximum Duty Cycle vs. Temperature
TC151A3624



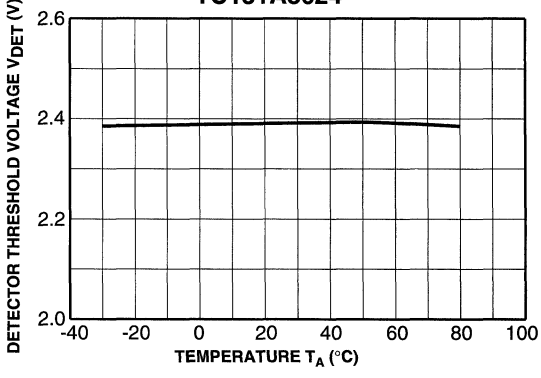
7) Output Voltage V_{DD} vs. Temperature
TC151A3624



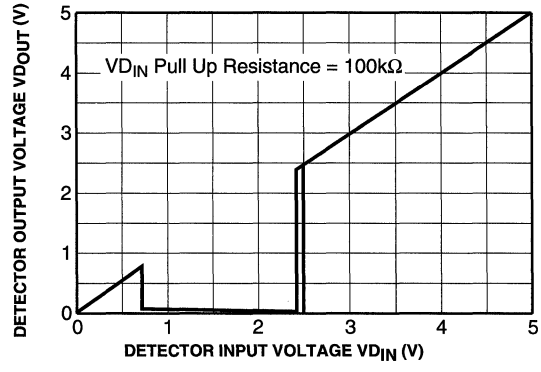
8) Output Voltage V_{OUT} vs. Temperature
TC151A3624



9) Detector Threshold vs. Temperature
TC151A3624

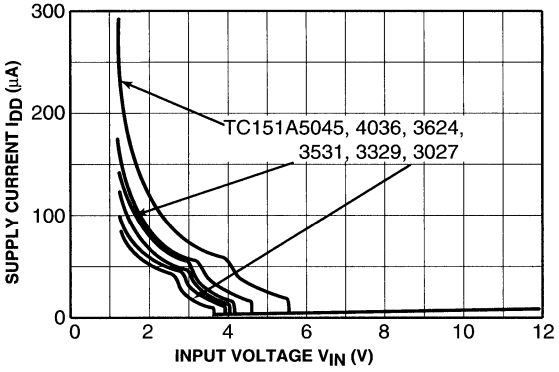


10) Detector Output Voltage vs. Detector Input Voltage
TC151A3624

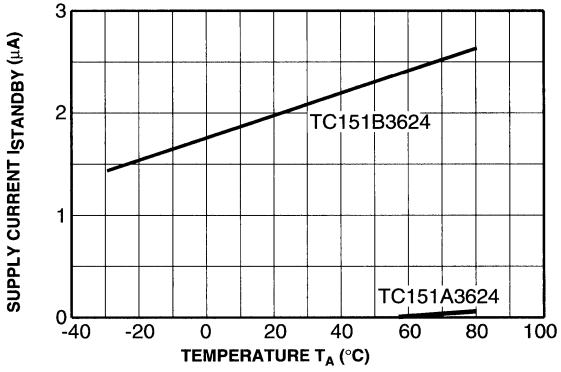


TYPICAL CHARACTERISTICS

11) Supply Current (No Load) vs. Input Voltage TC151AXXXX

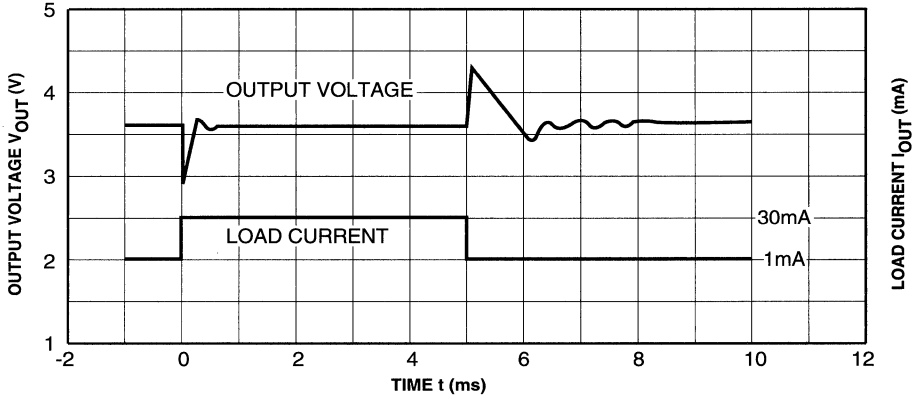


12) Supply Current (No Load) vs. Temperature TC151A3624/1B3624

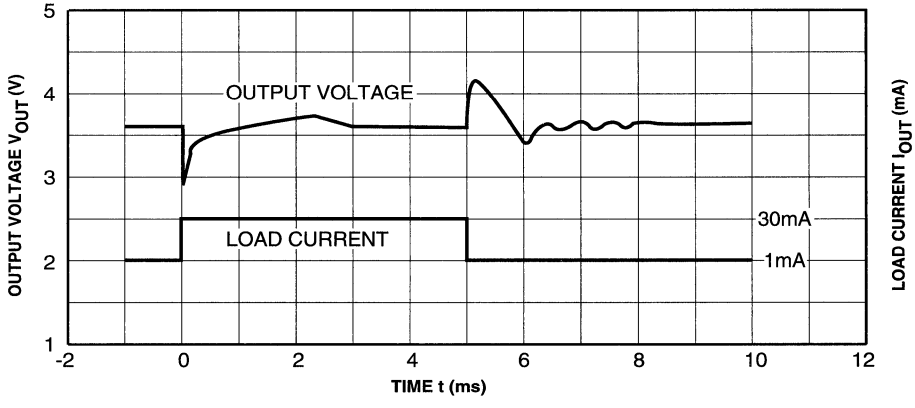


13) Load Transient Response TC151A3624

1) V_{IN} = 3V



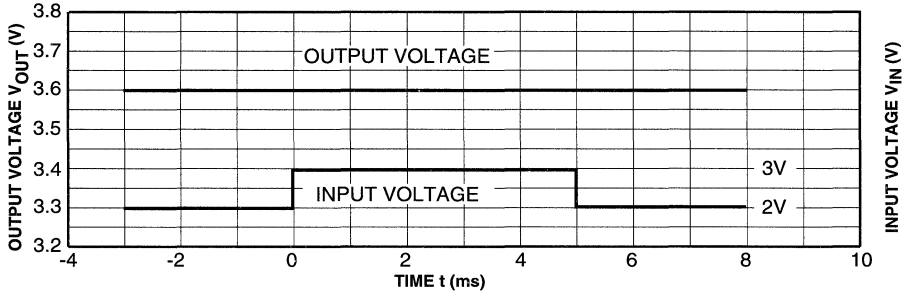
2) V_{IN} = 5V

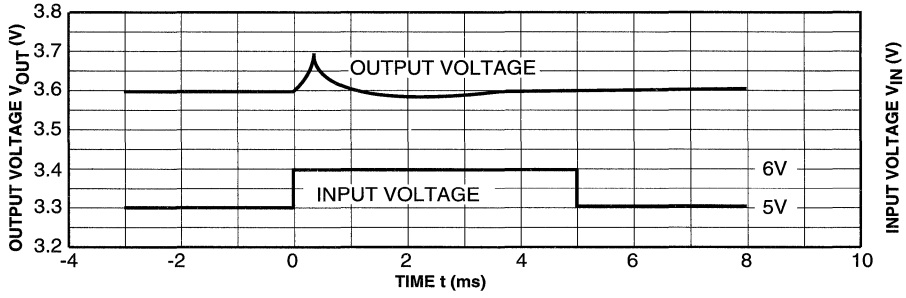


TYPICAL CHARACTERISTICS

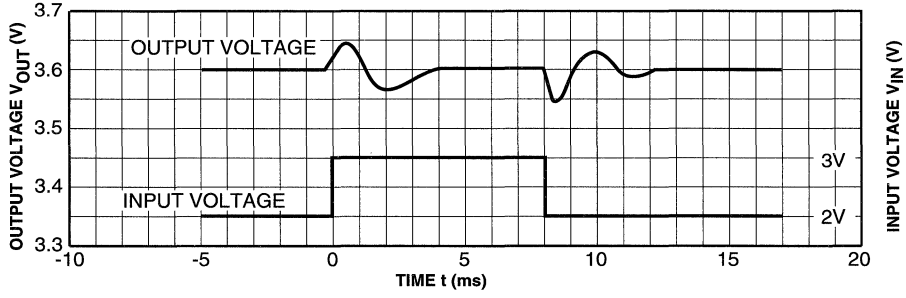
14) Line Transient Response

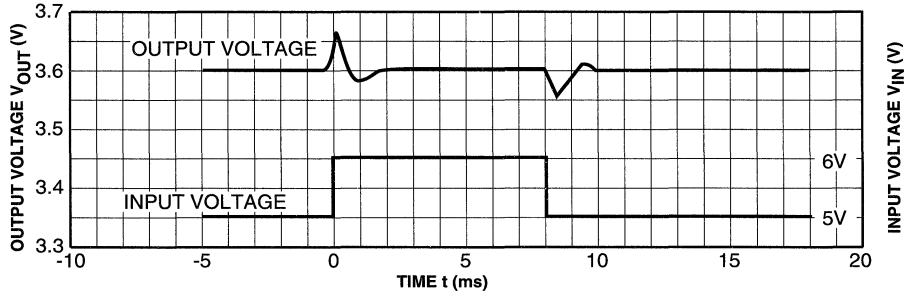
1) I_{OUT} = −1mA





2) I_{OUT} = −30mA

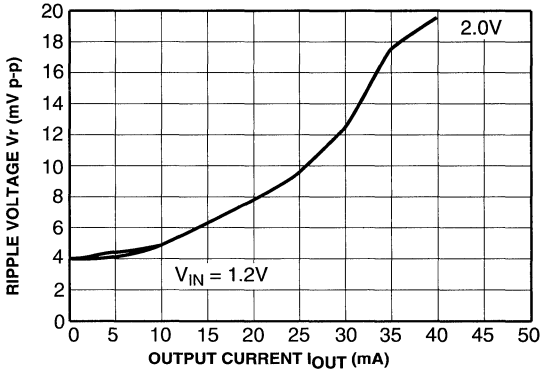




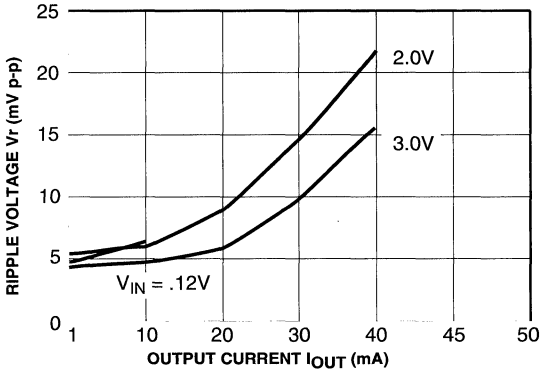
TYPICAL CHARACTERISTICS

15) Output Ripple Voltage vs. Output Current (T_A = 25°C)

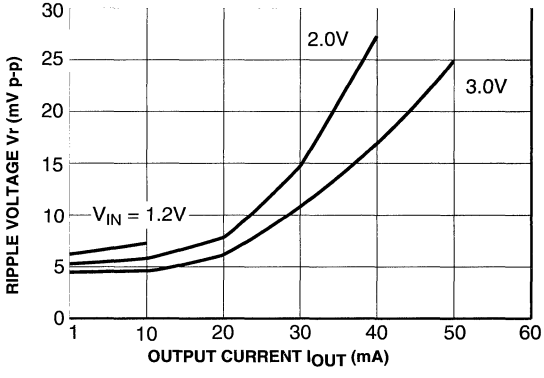
TC151B3027



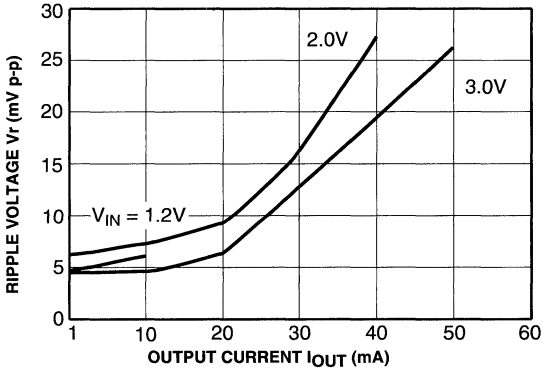
TC151B3329



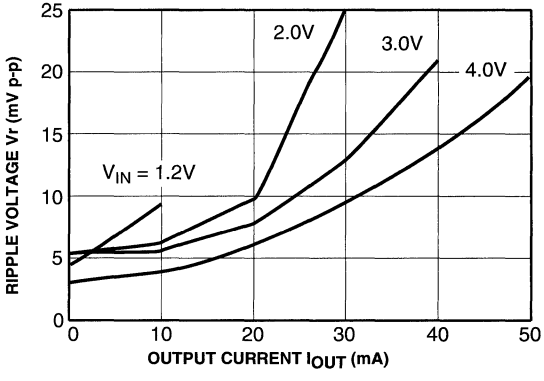
TC151B3531



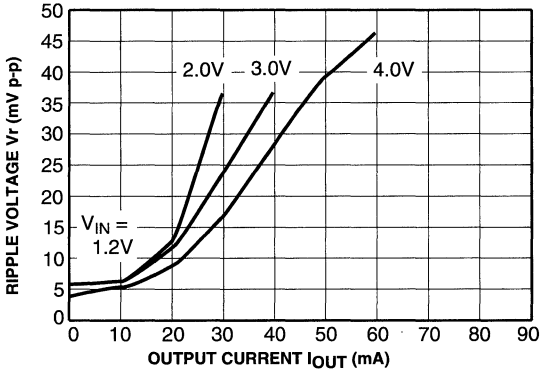
TC151B3624



TC151B4036



TC151B5045



3

BICMOS PWM CONTROLLERS

FEATURES

- **Low Power BICMOS Construction**
- **Low Supply Current at 20 KHz ..... 1.0 mA Typ**
- **Latch-Up Immunity .....>500 mA on Outputs**
- **Below Rail Input Protection ..... -5V**
- **High Output Drive ..... 500 mA Peak**
- **Fast Rise/Fall Time ..... 50 ns @ 1000 pF**
- **High Frequency Operation ..... Up to 1 MHz**
- **Tri-state Sync Pin for Easy Parallel Operation**
- **Under Voltage Hysteresis Guaranteed**
- **Shutdown Pin Available**
- **Double-Ended**
- **Soft Start, With Small Cap**
- **Low Prop Delay Shutdown to Output.. 140 ns Typ.**

GENERAL DESCRIPTION

The TC35C25 family of PWM controllers are CMOS implementations of the industry standard 3525 voltage mode SMPS ICs.

These second generation CMOS devices employ TelCom Semiconductors' Tough BiCMOS™ process for latch-up proof operation. They offer much lower power consumption than any of their previous CMOS or bipolar counterparts.

These controllers have separate supply pins for the control and output sections of the circuit. This allows "boot-strap" operation. The CMOS output stage allows the output voltage to swing to within 25 mV of either rail.

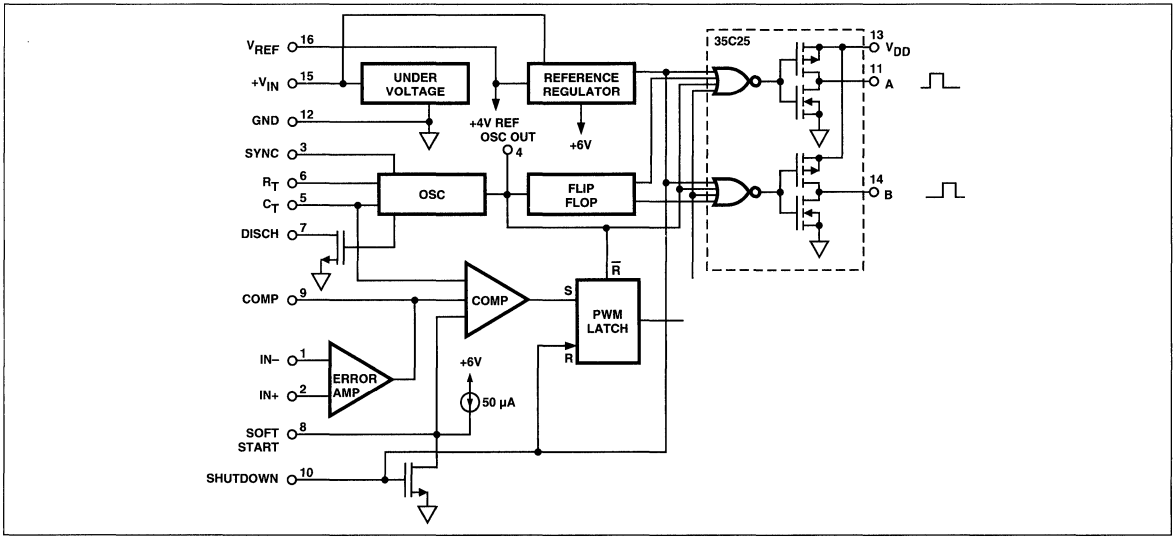
Other improved features include tighter hysteresis and undervoltage start-up specifications over temperature, and very low input bias current on all inputs.

3

ORDERING INFORMATION

Part No.	Configuration	Pkg./Temperature
TC15C25MJE	Non-Inverting	16-Pin CerDIP –55 to +125°C
TC25C25EOE	Non-Inverting	16-Pin SOIC (wide) –40 to +85°C
TC25C25EPE	Non-Inverting	16-Pin Plastic DIP –40 to +85°C
TC35C25COE	Non-Inverting	16-Pin SOIC (wide) 0 to +70°C
TC35C25CPE	Non-Inverting	16-Pin Plastic DIP 0 to +70°C

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply for $-55°C < T_A < +125°C$ for TC15C25MJE; $-40°C < T_A < +85°C$ for the TC25C25EXX; and $0°C < T_A < +70°C$ for the TC35C25CXX; V_{IN} and V_{DD} = 16V; R_T = 3.7kΩ; C_T = 1000 pF; RD = 760 Ω

Parameter	Test Conditions	Min	Typ	Max	Units
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1 mA	3.9	4	4.1	V
Line Regulation	V_{IN} = 8V to 18V	—	±4	±10	mV
Load Regulation	I_I = 1mA to 12 mA	—	±4	±15	mV
Temp Coefficient	Note 1	—	±0.01	±0.4	mV/°C
V_{REF}	Worst Case	3.85	4	4.15	V
Long Term Drift	T_J = 25°C, (note 1)	—	±50	—	mV/1000Hrs
Short Circuit	V_{REF} to GND	20	40	70	mA
Output Noise	T_J = 25°C, 10 Hz ≤ f ≥ 10 kHz, (note 1)	—	21	—	µV(rms)
Oscillator Section					
Initial Accuracy	T_J = 25°C, at 97 KHz	—	±2	±3	%
Voltage Coefficient	V_{IN} = 8V to 18V	—	±0.01	±0.1	%/V
Temp Coefficient	Note 1	—	±0.025	±0.06	%/°C
OSC Ramp Amplitude		2.9	3.2	3.4	V
Reset Switch $R_{DS\ (ON)}$	T_J = 25°C	30	50	60	Ω
Clock Amplitude	f_{osc} = 100 kHz, R_L = 1MΩ, (note1)	4.9	5.5	6.7	V
Clock Min Width	T_J = 25°C, R_D = 0Ω, (note 1) C_T = 100 pF, R_T = 1Ω	—	170	200	ns
Sync Threshold	R_T pin tied to V_{REF}, C_T pin at GND	1.8	2.2	2.8	V
Sync Input Current	Sync Voltage = 4V, V(R_T) = 4V	—	—	±1	µA
Min Sync Pulse Width	T_J = 25°C, Sync Amplitude = 5V, (note 1)	—	130	175	ns
Max OSC Freq	R_T = 1Ω, C_T = 100 pF, R_D = 0Ω, (note 1) T_J = 25°C	1.0	—	—	MHz
Error Amplifier Section (V_{CM} = 2.5V)					
Input Offset Voltage		—	±5	±15	mV
Input Bias Current	T_J = 25°C	—	±50	±200	pA
Input Offset Current	T_J = 25°C	—	±25	±100	pA
DC Open Loop Gain	R_L = 100kΩ	70	85	—	dB
Gain Bandwidth Product	Note 1	0.7	0.9	1.2	MHz
Output Low Level	R_L = 100kΩ (NChannel)	—	10	20	mV
Output High Level	R_L = 100kΩ (NPN)	4.9	5.4	5.9	V
CMRR	V_{CM} = 0.5 to 4.7V	60	75	—	dB
Supply Voltage Rejection	V_{IN} = 8V to 18V	90	120	—	dB
Slew Rate	C_{LOAD} = 50 pF, ACL = 1 V(EA+) = 1V to 3V pulse, (note 1)	—	1	—	V/µs
Threshold Hysteresis		0.6	0.8	1	V
Total Standby Current					
Supply Current		—	1.2	2.5	mA
Start-Up Current		—	250	350	µA

ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply for $-55°C < T_A < +125°C$ for TC15C25MJE; $-40°C < T_A < +85°C$ for the TC25C25EXX; and $0°C < T_A < +70°C$ for the TC35C25CXX; V_{IN} and V_{DD} = 16V; R_T = 3.7kΩ; C_T = 1000 pF; RD = 760 Ω

Parameter	Test Conditions	Min	Typ	Max	Units
PWM Comparator					
Min. Duty Cycle	Note 1, $T_J = 25°C$	—	—	0	%
Max Duty Cycle	$T_J = 25°C$, f_{OSC} = 100KHz, (note 1)	45	49	—	%
Input Threshold	$V(C_T) = 0.6V$	0.5	0.6	0.7	V
Input Threshold	$V(C_T) = 3.6V$	3.4	3.6	3.7	V
Input Bias Current	Note 1, $T_J = 25°C$	—	—	±1	µA
Soft Start Section					
Soft Start Current	$V_{SHUTDOWN}$ = 0V	30	46	75	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 3V	—	30	100	mV
Shutdown Input Current	$V_{SHUTDOWN}$ = 3V	—	±1	±100	nA
Min Shutdown Pulse Width	$V_{SHUTDOWN}$ = 5V, (note 1)	—	20	40	ns
Shutdown Delay	$V_{SHUTDOWN}$ = 5V, (note 1)	130	140	220	ns
Shutdown Threshold		1.5	2.4	3	V
Output Drivers (each output)					
Output Low Level RDS (ON)	I_{SINK} = 20mA	—	13	25	Ω
Output High Level RDS (ON)	I_{SOURCE} = 20 mA	—	20	35	Ω
Rise Time	$C_L = 1_{nF}$, (note 1)	—	55	80	ns
Fall Time	$C_L = 1_{nF}$, (note 1)	—	40	65	ns
Power Suppy					
Supply Current	f_{OSC} = 100KHz	—	2	3	mA
UV Lockout Threshold		6.6	7	7.3	V
UV Lockout Hysteresis		1.7	2.2	2.5	V
Start-up Current		—	75	200	µA

NOTE: 1. Not Tested.

OUTPUT SECTION

The output stage of the TC35C25 is comprised of two pairs of complimentary CMOS drivers operating in a push-pull mode. Each output is capable of sinking or sourcing nearly 500 mA of peak current. They are also capable of absorbing just as much "kick-back" current without latching.

SOFT START

A soft restart recovery rate may be selected by placing a capacitor from SOFT START (pin 8) to ground. The calculation for the recovery timing is approximately 60 ms/ µF.

SOFT START will mediate the start-up from under voltage recovery, power-on, or SHUTDOWN.

SHUTDOWN

There is a minimum delay, non-latching shutdown feature on the TC35C25 PWM controller. Both outputs may be turned off by applying a positive voltage to SHUTDOWN (pin 10). Typical shutdown threshold is 2.4 V. Returning the pin back to ground will reinitialize the soft start cycle.

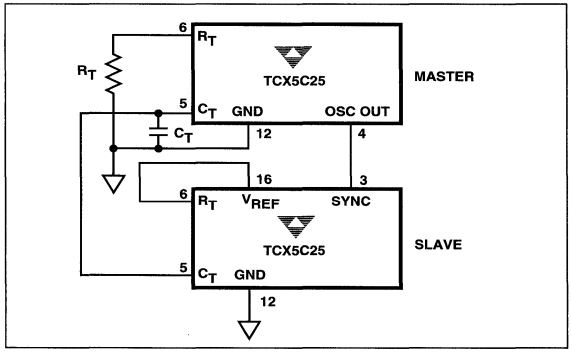
OSCILLATOR SECTION

A tri-state feature has been added to accommodate systems which require multiple controllers to be run in a "master/slave" configuration. The timing resistor pin (R_T, pin 6) may be tied to V_{REF} to place the sync pin (SYNC, pin 3) in a high impedance state. This will allow the chip to be clocked from an external source.

The sync output (OSC OUT, pin 4) of the TC35C25 can drive several sync inputs configured in this manner.

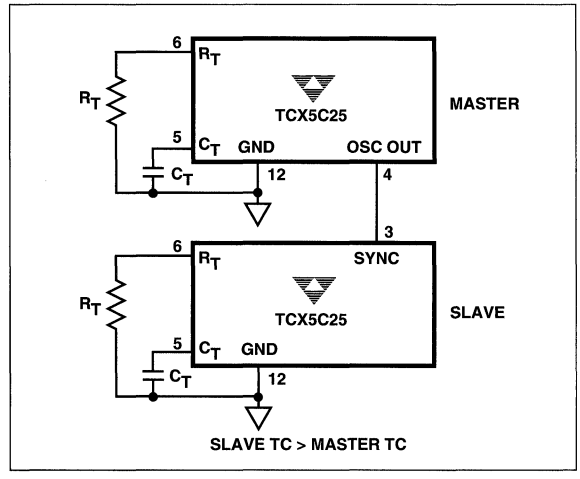
SCILLATOR SYNCHRONIZATION

Synchronization of two TC15C25/27 can be done by making one PWM Controller as the master oscillator to synchronize the slave as follows:

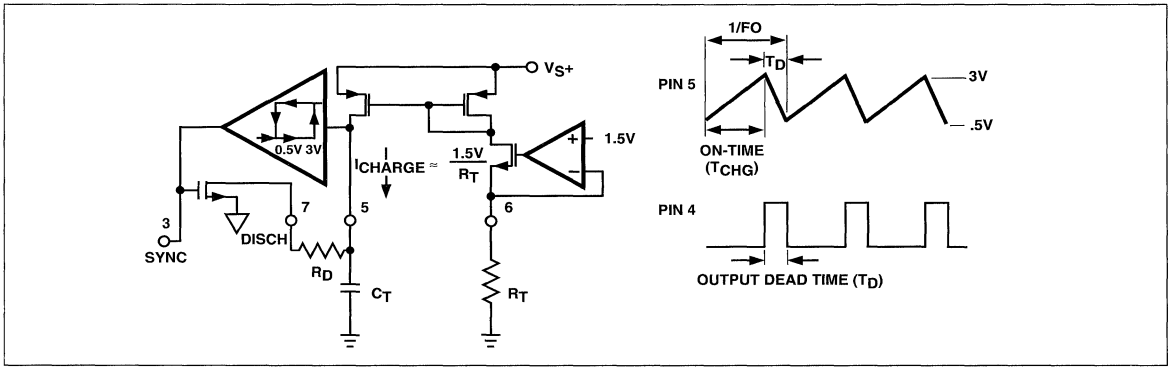


OSCILLATOR SYNCHRONIZATION WITH SEPARATE RC TIMER

Synchronization can also be done by having a separate RC timing circuit on the slave oscillator that is slightly lower frequency than the master oscillator. The sync input will not be in a high impedance state so the number of slave oscillators is limited. This method of synchronization is useful when slave oscillator is located in a different location. When a separate RC timer is used in the slave controller, ground loop noise pickup in the oscillator is minimized.



OSCILLATOR FREQUENCY AND OUTPUT DEAD TIME



The oscillator frequency (F_O) = $\frac{1}{T_{CHG} + T_D}$

T_{CHG} is the charging duration of C_T. One of the PWM Controller output drivers is ON during charging of C_T. T_D is the output dead time when both of the output drivers are inactive. Resistor (R_T) sets the Capacitor (C_T) charging current.

To choose an oscillator frequency (F_O), first select the period of dead time (T_D) required. Calculate the capacitor charge time (T_{CHG}).

$$T_{CHG} = \frac{1 - F_O \times T_C}{F_O}$$

Select a capacitor in the range of 100 pF to 1000 pF for C_T. See graph in Typical Characteristic Curve. Calculate capacitor charging current (I_{CHG}).

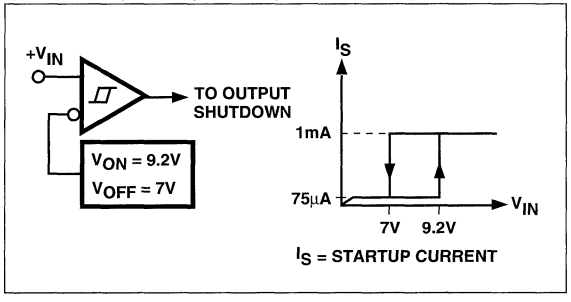
$$I_{CHG} = \frac{2.5 \times C_T}{T_{CHG}}$$

C_T in Farads, T_{CHG} in seconds, I_{CHG} in amperes, and R_T in ohms.

$$R_T = \frac{1.5}{I_{CHG}}$$

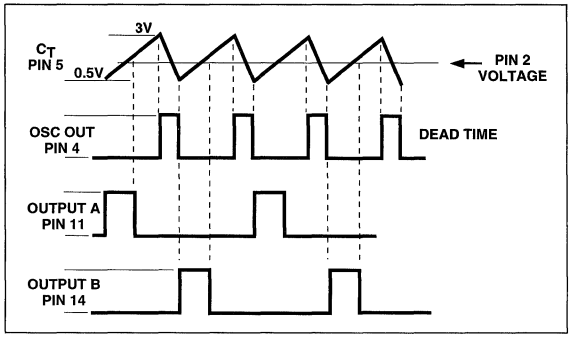
The resistor (R_D) controls the period of dead time (T_D). During dead time this resistor (R_D) current is the sum of the C_T discharge current and the I_{CHG} current. The value for R_D can range from >1 ohm to <900 ohm. Dead time increases when R_D is increased. See graph in Typical Characteristic Curve for dead time resistor value.

UNDERVOLTAGE LOCKOUT SECTION

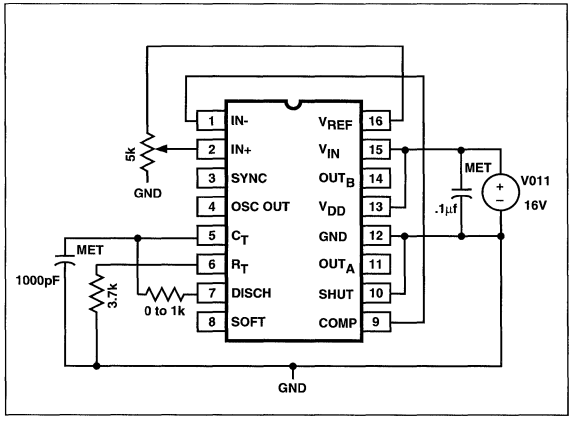


The typical turn on threshold is 9.2 V for operation of this family of PWM Controllers. When supply voltage at pin 15 drops below 7 V, after normal operation above 9.2 V, lockout occurs and both output drives to pin 11 and 14 are terminated.

BENCH TEST OPERATIONAL SIMULATION WAVEFORMS



The 5K potentiometer sets a reference voltage at pin 2. When ramp voltage of pin 5 reaches this reference voltage, output drive pulse is active ON. Varying the discharge resistor will vary the dead time. Increasing the discharge resistor will effect an increase in the dead time.



REPLACING BIPOLAR VERSIONS WITH CMOS

Although the pin-out and functions are the same for both the Bipolar and CMOS versions, there are several differences that need to be taken into account. The reference voltage on the TC35C25 is 4 V instead of 5 V and the oscillator ramp is 3 V, not 4 V. The R_T and C_T values are different for any particular frequency and dead-time requirement.

The most important difference is that the absolute maximum rating of the V_{DD} and V_{IN} voltages for the TC35C25 is 18 V, whereas the UC3525 is 40 V.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Maximum Chip Temperature ..... 150 °C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (10 sec) ..... 300 °C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 250°C/W
- SOIC $R_{\theta J-A}$ ..... 75°C/W

Operating Temperature
- 15C2X ..... $-55°C \le T_A \le +125°C$
- 25C2X ..... $-40°C \le T_A \le +85°C$
- 35C2X ..... $0°C \le T_A \le +70°C$

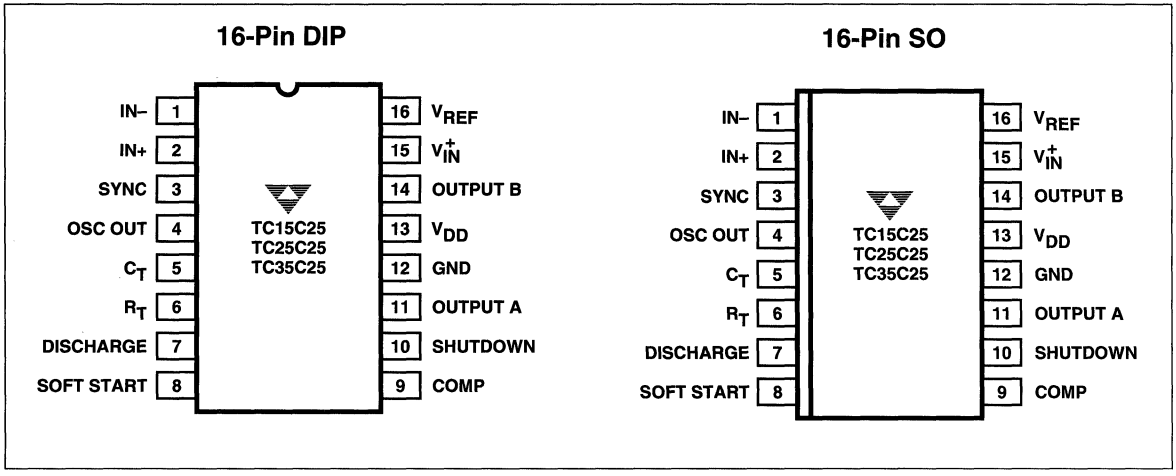
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

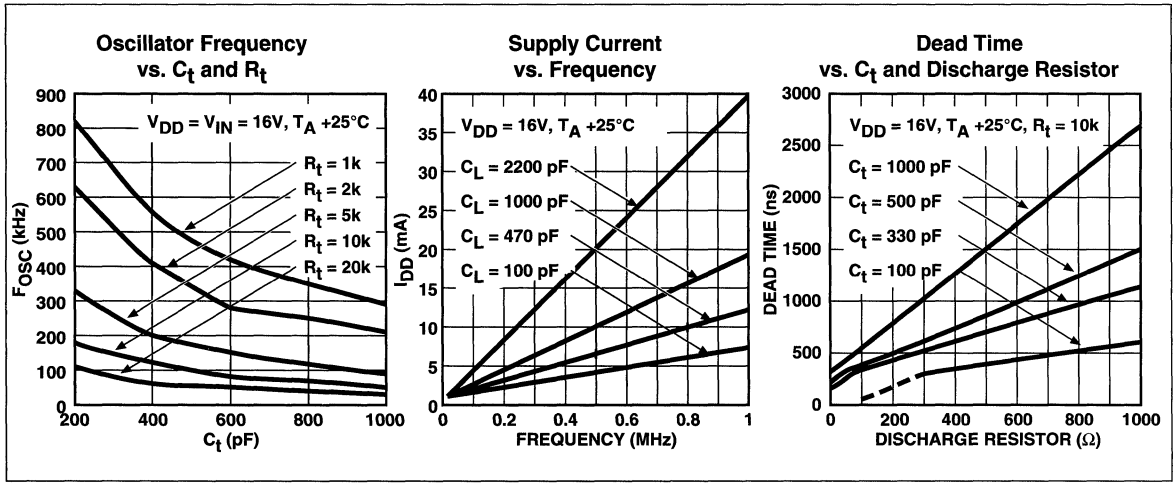
PIN	DESCRIPTION
1	**IN-, ERROR AMPLIFIER** inverting input for output voltage reference input and amplifier gain set.
2	**IN+, ERROR AMPLIFIER,** non-inverting input for output voltage feedback to regulate voltage.
3	**SYNC** input pin for PWM controller oscillator synchronization of two or more controllers from an external clock output or from another PWM controller oscillator output.
4	**OSC OUT** pin is for output of the internal oscillator. This signal can be used as a master oscillator to sync other oscillators to run at the same timing period.
5	C_T pin is the capacitor timing input to set oscillator frequency in conjunction with pin 6 R_T timing resistor.
6	R_T pin is for timing resistor input to set oscillator frequency by setting the charge current into capacitor C_T of pin 5.
7	**DISCH** pin is for discharging the timing capacitor, C_T of pin 5. During discharging time period, PWM controller output is disabled. This is called dead time. With a resistor between pin 7 and pin 5, the dead time can be controlled.
8	**SOFT START** pin is for soft starting the power supply. A capacitor from this pin to GND pin 12 will limit duty cycle till capacitor is charged above error amplifier output.
9	**COMP** pin is for compensation of the feedback loop response.
10	**SHUTDOWN** pin is for terminating both outputs of pins 11 and 14. This will shutdown the power supply outputs. A positive input with shutdown threshold of 2.4 V is required for shutdown.
11	**OUTPUT A** pin is for output drive of phase A to drive push pull transistor A.
12	**GND** pin is for ground return for all inputs and output signals.
13	V_{DD} pin is for power supply input to operate the output drivers A and B.
14	**OUTPUT B** pin is for output drive of phase B to drive push pull transistor B.
15	V_{IN} pin is for voltage bias supply input for all PWM controller functions except output drive circuits.
16	V_{REF} pin is the reference supply output voltage of 4.0 volts that may be used for any voltage reference purposes such as a reference to control output voltage.

TC15C25
TC25C25
TC35C25

PIN CONFIGURATION



TYPICAL CHARACTERISTIC CURVES



STEP-UP/STEP-DOWN DC/DC CONVERTER WITH VOLTAGE DETECTOR

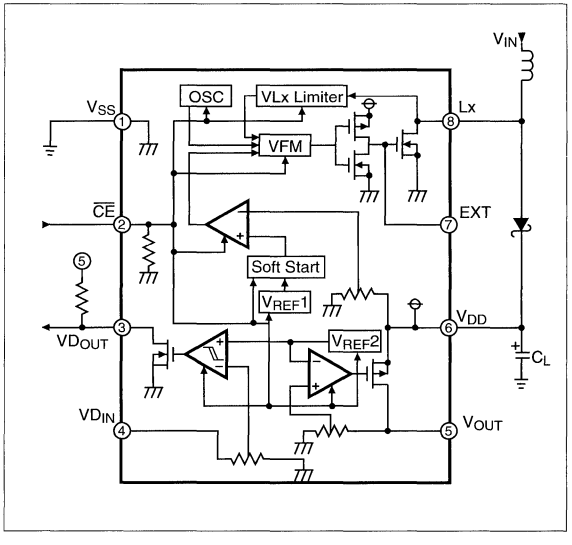
FEATURES

- **Low quiescent current ..... typ 15μA (TC163624; V_{IN} = 3.0V, No Load)**
- **Low standby current ..... 1A version 1.0μA MAX**
  1B version 10.0μA MAX
- **Low voltage operation ..... V_{IN} = 1.2 to 10V**
- **High accuracy output voltage ..... ±2.5%**
- **Wide choice of V_{OUT} ..... 1.5V to 6.0V in 0.1V Steps**
- **Wide choice of V_{DET} ..... 1.2V to 5.0V in 0.1V Steps**
- **Soft-start and driver protection circuits**
- **Small package ..... 8-Pin SOIC**
- **Larger current can be obtained by connecting an external power transistor**

APPLICATIONS

- **Laptop computers, portable automation equipment**
- **Pagers, cellular and cordless telephones**
- **Cameras and hand-held systems**

FUNCTIONAL BLOCK DIAGRAM

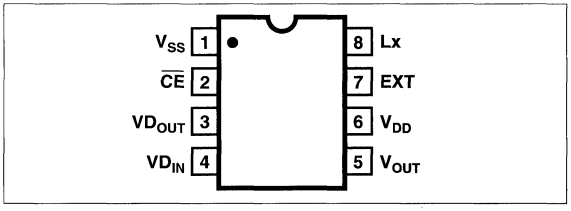


GENERAL DESCRIPTION

The TC16 Series are CMOS power-supply ICs containing a low-dropout linear regulator, an under-voltage detector, and a PFM DC/DC step-up (boost) converter. In normal operation (V_{IN} well above V_{OUT}), the device functions as a linear regulator. When V_{IN} drops below V_{IN} (min.) or less, the voltage detector (V_{DET}) senses this and turns on the boost converter that raises V_{IN} back up to the linear regulator's operating range. The TC16 thus extends battery life considerably by allowing the battery voltage to drop to formerly unusable levels.

As a user-selected option, the chip-enable pin, $\overline{CE}$, can shut down the entire IC (option A) or just the boost converter (option B), leaving the voltage detector active.

PIN CONFIGURATION



ORDERING INFORMATION

The range for V_{OUT} is 1.5V to 6.0V, and that for V_{DET} is 1.2V to 5.0V; both come in 0.1V increments, and are user-selected.

PART CODE **TC16 XX XX XX X XX XXX**

$\overline{CE}$ form: 1A*, 1B**

Output Voltage:
Ex: 15 = 1.5V; 60 = 6.0V

Detected Voltage:
Ex: 12 = 1.2V; 50 = 5.0V

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
OA: 8-Pin SOIC

Taping Direction:
723: Left Taping
713: Right Taping

* A: If $\overline{CE}$ is High (+V_{DD}) then whole chip is disabled.
**B: If $\overline{CE}$ is High (+V_{DD}) then only the DC/DC converter is disabled and the detector is still operational.

TC16 Series

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Limit	Unit
Power Supply Voltage		V_{IN}	– 0.3 to 12	V
Output Voltage of	Lx pin	VLx	– 0.3 to 12	V
	EXT pin	VEXT	– 0.3 to (V_{DD} + 0.3)	V
	V_{OUT} pin	V_{OUT}	– 0.3 to (V_{DD} + 0.3)	V
	VD_{OUT} pin	VD_{OUT}	– 0.3 to 12	V
Input Voltage of	$\overline{CE}$ pin	$V\overline{CE}$	– 0.3 to (V_{DD} + 0.3)	V
	VD_{IN} pin	VD_{IN}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V (ver. A)
			(V_{SS} – 0.3) to 12	V (ver. B)
Output Current of	EXT pin	IEXT	50	mA
	Lx pin	ILx	250	mA
Power Dissipation		Pd	300	mW
Operating Temperature		T_A	– 40 to +85	°C
Storage Temperature		T_{stg}	– 65 to +150	°C
Soldering Condition		T_{solder}	260° 10 sec	

ELECTRICAL CHARACTERISTICS: TC161A/1B3624 (3.6V Output)

T_A = 25°C, V_{IN} = 4.1V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operation Input Voltage	No Load	1.2		10	V
V_{DD}	Step-up Output Voltage	No Load	3.99	4.10	4.21	V
V_{OSCST}	Oscillator Start-up Voltage	No Load		0.9	1.2	V
f_{osc}	Maximum Oscillator Frequency			100		kHz
Maxdty	Maximum Oscillator Duty Cycle		65	80	90	%
V_{OL1}	Lx Output Voltage	I_{OL} = 50mA			0.5	V
I_{OH1}	Lx Leakage Current			0.01	10	µA
V_{LXlim}	Lx Voltage Limit	Lx pin ON		0.9		V
V_{OH}	EXT Output Pch ON Voltage	I_{EXT} = – 3mA, V_{IN} = 4.1V	3.6			V
V_{OL2}	EXT Output Nch ON Voltage	I_{EXT} = 5mA, V_{IN} = 4.1V			0.5	V
V_{OUT}	Output Voltage	I_{OUT} = – 5mA	3.51	3.60	3.69	V
V_{DIF}	Dropout Voltage	I_{OUT} = – 30mA		0.3		V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	– 30mA ≤ I_{OUT} ≤ 0mA			100	mV
$-V_{DET}$	Detector Threshold		2.34	2.4	2.46	V
V_{HYS}	Detector Threshold Hysteresis Range		60	120	240	mV
V_{OL3}	VD_{OUT} ON Voltage	I_{OL} = 5mA			0.5	V
I_{OH2}	VD_{OUT} Leakage Current			0.01	5	µA
I_{VDINH}	VD_{IN} "H" Input Current	VD_{IN} = V_{IN}			5	µA
I_{VDINL}	VD_{IN} "L" Input Current	VD_{IN} = V_{SS}	– 0.5		0.5	µA
V_{CEH}	$\overline{CE}$ "H" Input Voltage		V_{DD} – 0.3		V_{DD}	V
V_{CEL}	$\overline{CE}$ "L" Input Voltage		0		0.2 V_{DD}	V
I_{CEH}	$\overline{CE}$ "H" Input Current	$\overline{CE}$ = V_{IN}	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ "L" Input Current	$\overline{CE}$ = V_{SS}	– 0.5		0.5	µA
I_{DD}	Supply Current	V_{IN} = 3V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{SS}, No Load		15	30	µA
Istandby	Supply Current	V_{IN} = 3V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{DD}, No Load			1.0 10.0	µA[1] µA[2]

NOTES
[1] Standby current of version A
[2] Standby current of version B

ELECTRICAL CHARACTERISTICS:

TC161A/1B5045 (5.0V Output) T_A = 25°C, V_{IN} = 5.5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operation Input Voltage	No Load	1.2		10	V
V_{DD}	Step-up Output Voltage	No Load	5.36	5.5	5.64	V
V_{OSCST}	Oscillator Start-up Voltage	No Load		0.9	1.2	V
f_{osc}	Maximum Oscillator Frequency		80	100	120	kHz
Maxdty	Maximum Oscillator Duty Cycle		65	80	90	%
V_{OL1}	Lx Output Voltage	I_{OL} = 50mA			0.5	V
I_{OH1}	Lx Leakage Current			0.01	10	µA
V_{LXlim}	Lx Voltage Limit	Lx pin ON		0.9		V
V_{OH}	EXT Output Pch ON Voltage	I_{EXT} = – 3mA, V_{IN} = 5.5V	5.0			V
V_{OL2}	EXT Output Nch ON Voltage	I_{EXT} = 5mA, V_{IN} = 5.5V			0.5	V
V_{OUT}	Output Voltage	I_{OUT} = – 5mA	4.87	5.0	5.13	V
V_{DIF}	Dropout Voltage	I_{OUT} = – 30mA		0.3		V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	– 30mA ≤ I_{OUT} ≤ 0mA			100	mV
$-V_{DET}$	Detector Threshold		4.38	4.5	4.62	V
V_{HYS}	Detector Threshold Hysteresis Range		112	225	450	mV
V_{OL3}	VD_{OUT} ON Voltage	I_{OL} = 5mA			0.5	V
I_{OH2}	VD_{OUT} Leakage Current			0.01	5	µA
I_{VDINH}	VD_{IN} "H" Input Current	VD_{IN} = V_{IN}			5	µA
I_{VDINL}	VD_{IN} "L" Input Current	VD_{IN} = V_{SS}	– 0.5		0.5	µA
V_{CEH}	$\overline{CE}$ "H" Input Voltage		V_{DD} – 0.3		V_{DD}	V
V_{CEL}	$\overline{CE}$ "L" Input Voltage		0		0.2 V_{DD}	V
I_{CEH}	$\overline{CE}$ "H" Input Current	$\overline{CE}$ = V_{IN}	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ "L" Input Current	$\overline{CE}$ = V_{SS}	– 0.5		0.5	µA
I_{DD}	Supply Current	V_{IN} = 4V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{SS}, No Load		20	40	µA
Istandby	Supply Current	V_{IN} = 4V, L = 100µH, C = 22µF, $\overline{CE}$ = V_{DD}, No Load			1.0 10.0	µA[1] µA[2]

NOTES
[1] Standby current of version A
[2] Standby current of version B

PIN DESCRIPTION

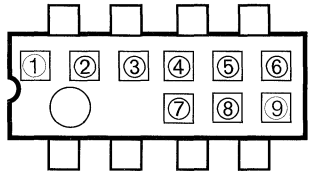
Pin No.	Symbol	Description
1	V_{SS}	Ground
2	$\overline{CE}$	Chip Enable. Set the pin to V_{DD} to change the device to standby state
3	VD_{OUT}	Output of voltage detector (NMOS open drain output)
4	VD_{IN}	Input to voltage detector
5	V_{OUT}	Output of voltage regulator

Pin No.	Symbol	Description
6	V_{DD}	Input to linear regulator from boost converter
7	EXT	Output drive for external PFM switch transistor
8	Lx	Input to internal switch (from L)

TC16 Series

MARKING

8 pin-SOIC



①&②represent 16: Fixed

③ represents first digit of voltage

Mark③	Volt
1	1.④(V)
2	2.④(V)
3	3.④(V)
4	4.④(V)
5	5.④(V)
6	6.④(V)

④ represents first decimal place of voltage

Mark④	Volt	Mark④	Volt
0	③.0(V)	5	③.5(V)
1	③.1(V)	6	③.6(V)
2	③.2(V)	7	③.7(V)
3	③.3(V)	8	③.8(V)
4	③.4(V)	9	③.9(V)

⑤ represents detective voltage

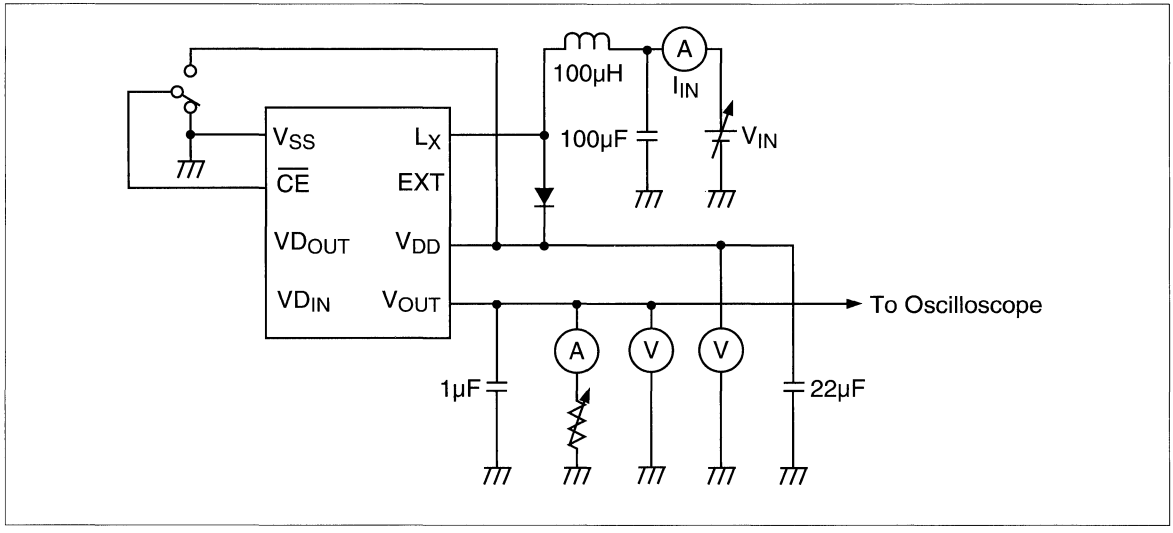
Mark⑤	V_{DET}	Mark⑤	V_{DET}	Mark⑤	V_{DET}
0	1.2	C	2.9	R	5.0
1	1.5	D	3.0	S	1.3
2	1.8	E	3.1		
3	1.9	F	3.3		
4	2.0	G	3.5		
5	2.1	H	3.6		
6	2.2	J	4.0		
7	2.4	K	4.1		
8	2.5	L	4.3		
9	2.6	M	4.5		
A	2.7	N	4.7		
B	2.8	O	4.8		

⑥ represents $\overline{CE}$ version

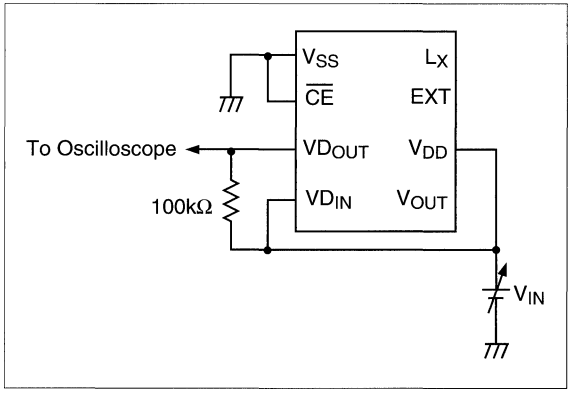
Mark⑥	Version
A	1A
B	1B

⑦, ⑧ and ⑨, represents assembly lot number

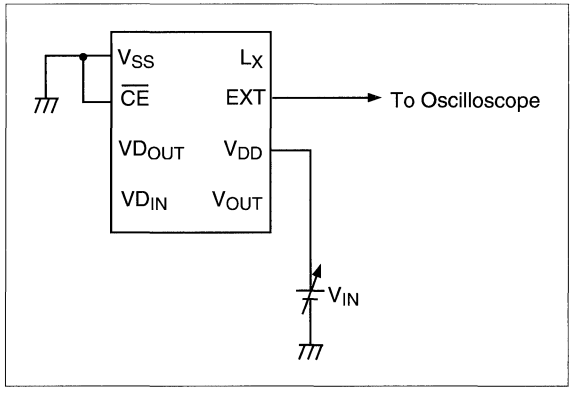
TEST CIRCUITS (Keyed to following graphs)



Test Circuit 1



Test Circuit 2



Test Circuit 3:

Test Circuit 1 Applies to graphical characteristics 1) - 4), 7), 8) and 11) - 14)
[Change the 100µF capacitance to 1µF for characteristics 13) and 14)
STANDBY state: $\overline{CE} = V_{DD}$]

Test Circuit 2 Applies to graphical characteristics 9) and 10)

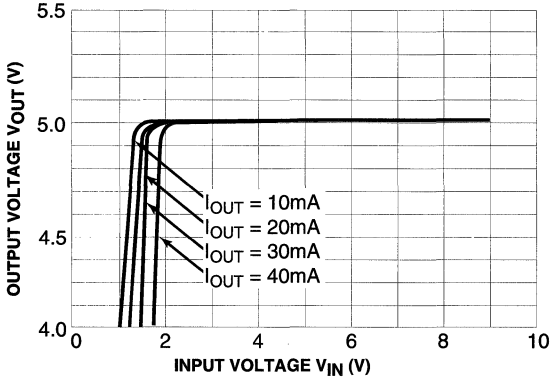
Test Circuit 3 Applies to graphical characteristics 5) and 6)
Definition of efficiency is as follows: $(V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN})$

TC16 Series

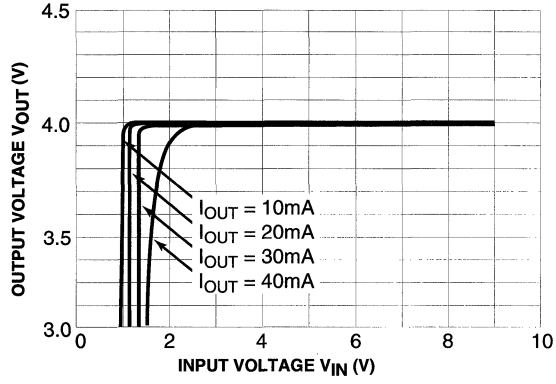
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Input Voltage

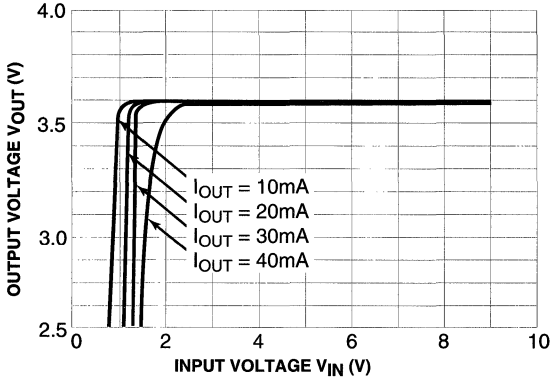
TC161A5045



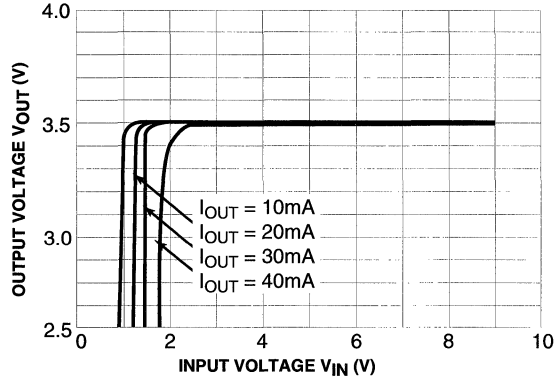
TC161A4036



TC161A3624



TC161A3531



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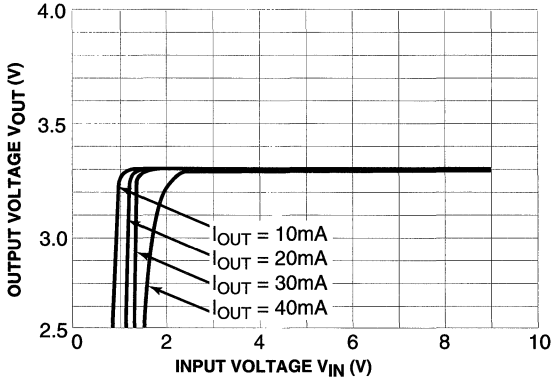

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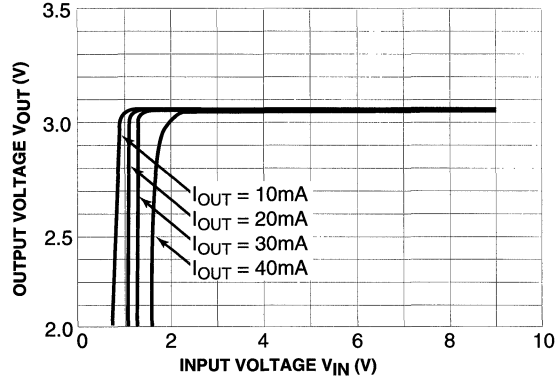
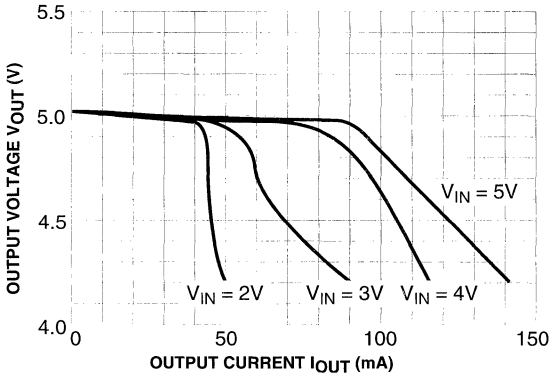


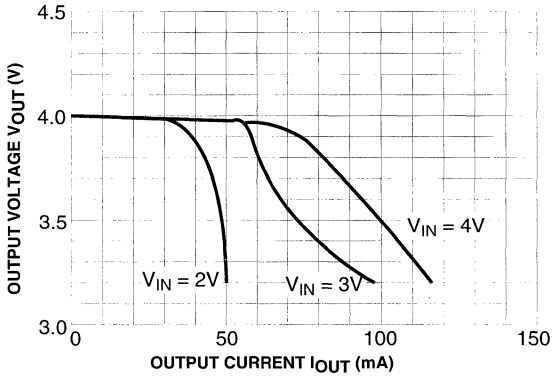
TYPICAL CHARACTERISTICS

2) Output Voltage vs. Output Current (T_A = 25°C)

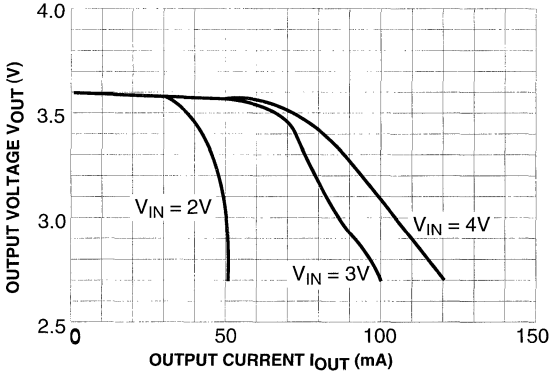
TC161A5045



TC161A4036



TC161A3624



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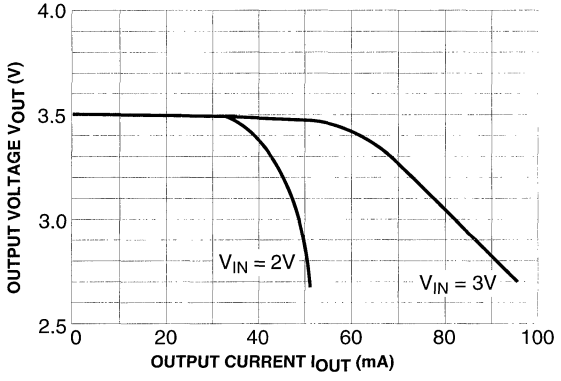

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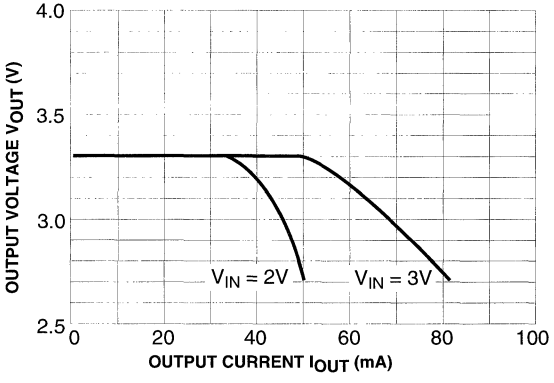

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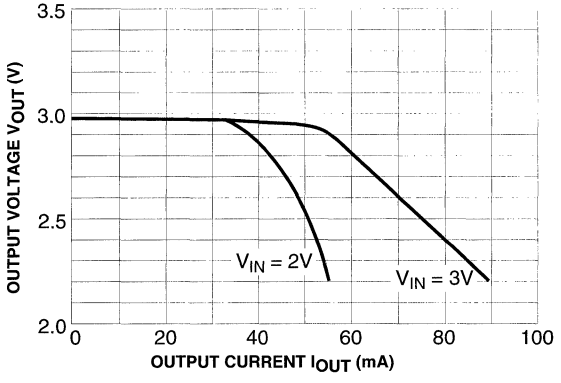


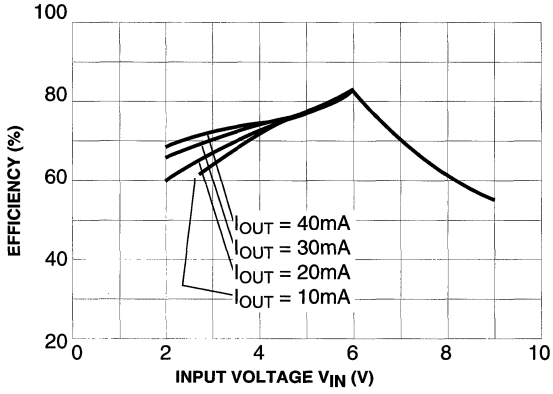
3

TC16 Series

TYPICAL CHARACTERISTICS

3) Efficiency vs. Input Voltage (T_A = 25°C)

TC161A5045



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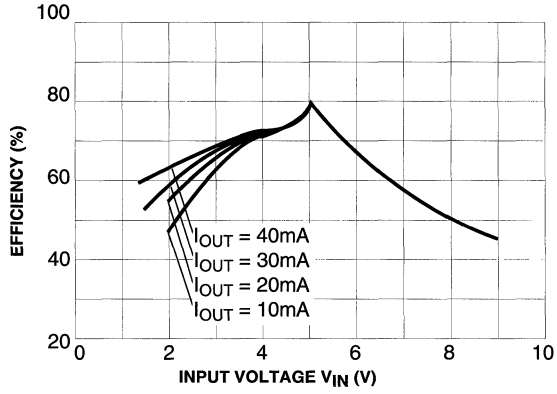

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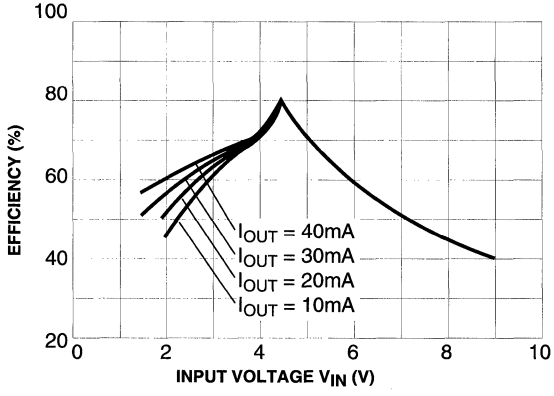

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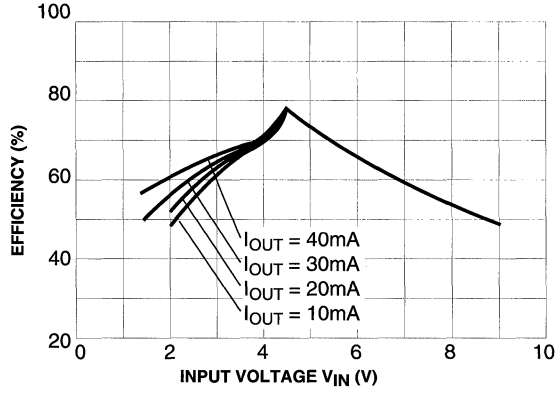
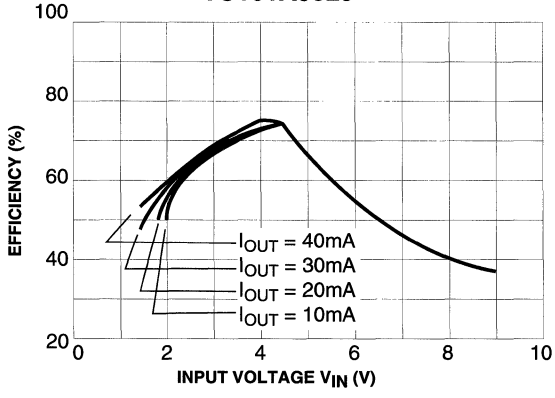


TC161A3329



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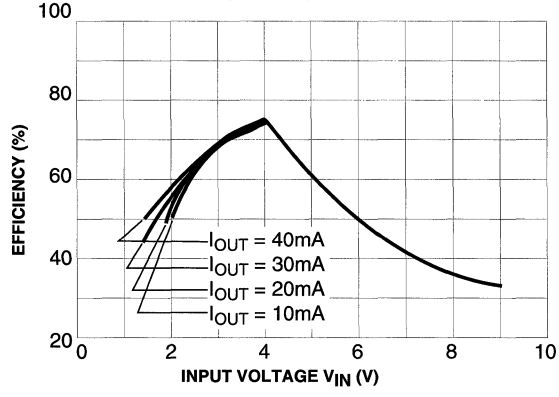
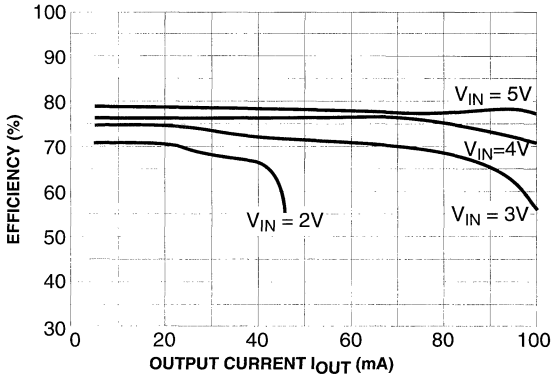


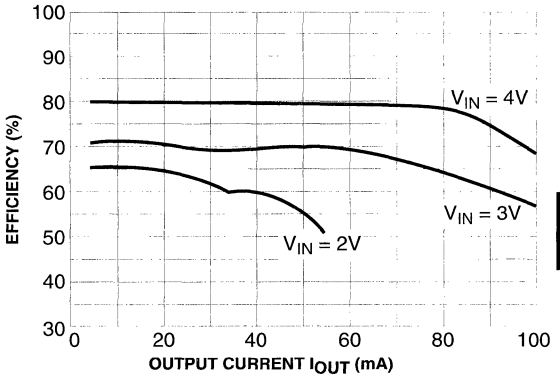
TYPICAL CHARACTERISTICS

4) Efficiency vs. Output Current (T_A = 25°C)

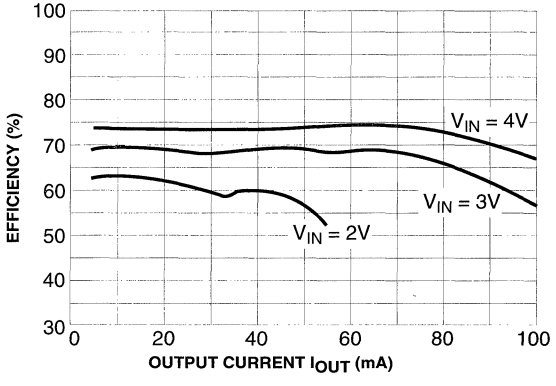
TC161A5045



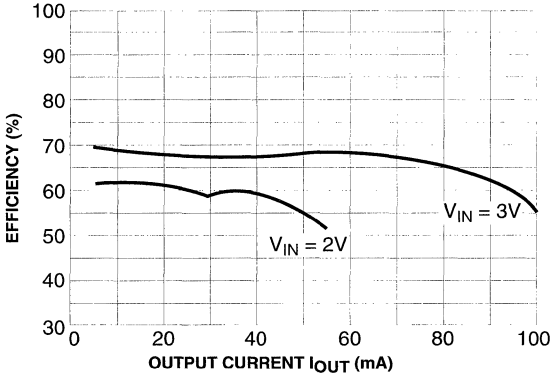
TC161A4036



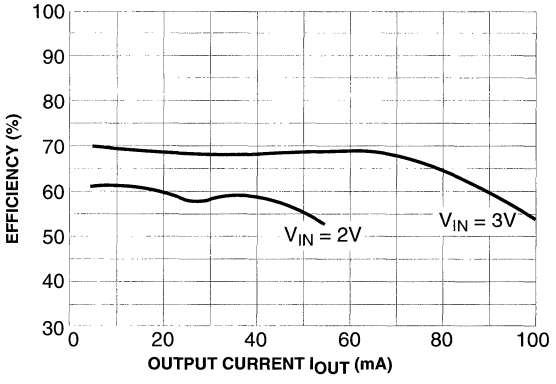
TC161A3624



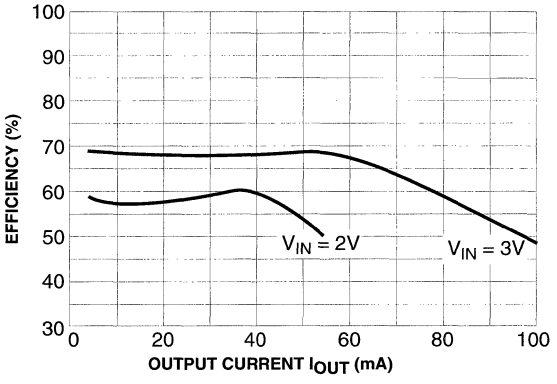
TC161A3531



TC161A3329



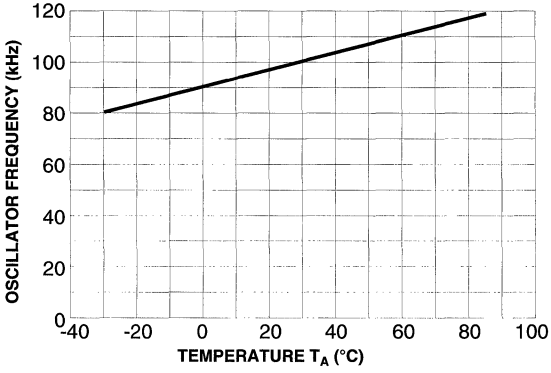
TC161A3027



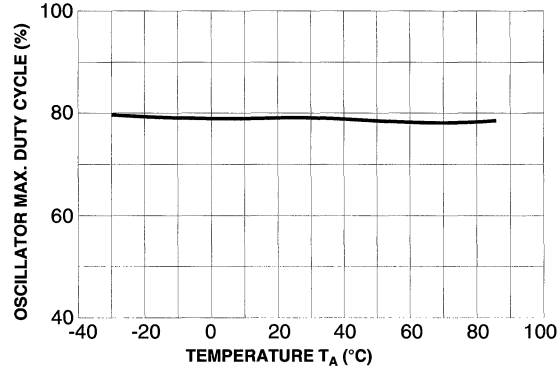
TC16 Series

TYPICAL CHARACTERISTICS

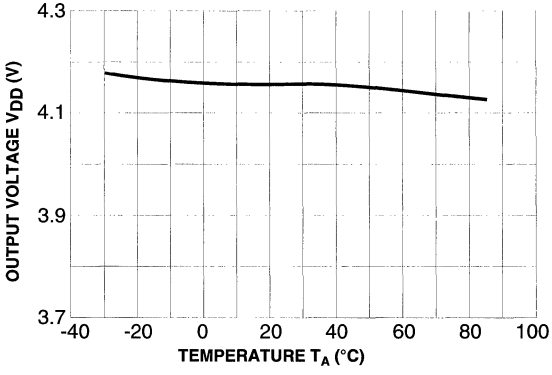
5) Oscillator Frequency vs. Temperature
TC161A3624



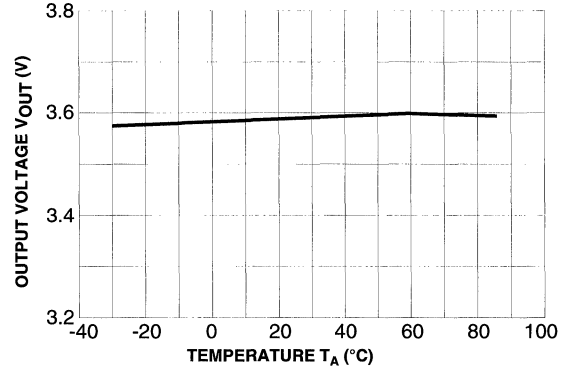
6) Oscillator Maximum Duty Cycle vs. Temperature
TC161A3624



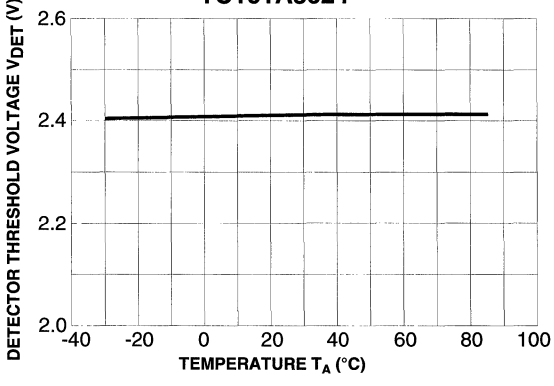
7) Output Voltage V_{DD} vs. Temperature
TC161A3624



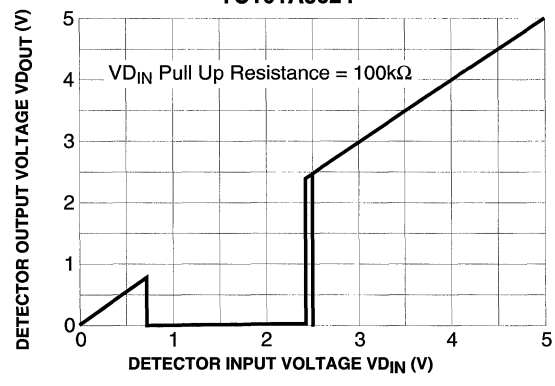
8) Output Voltage V_{OUT} vs. Temperature
TC161A3624



9) Detector Threshold vs. Temperature
TC161A3624

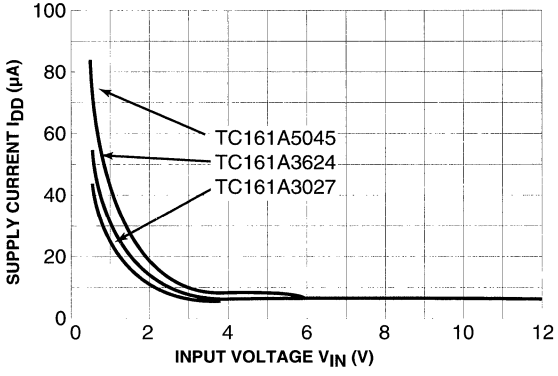


10) Detector Output Voltage vs. Detector Input Voltage
TC161A3624

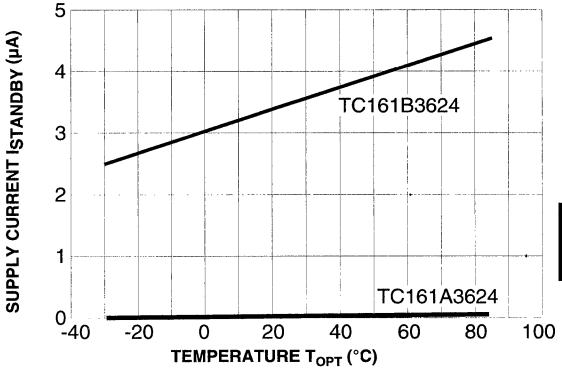


TYPICAL CHARACTERISTICS

11) Supply Current (No Load) vs. Input Voltage TC161AXXXX

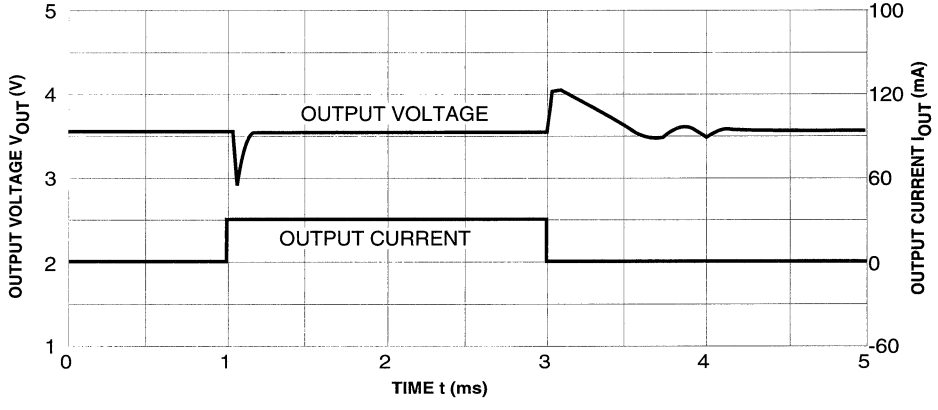


12) Supply Current (No Load) vs. Temperature TC161A/1B3624

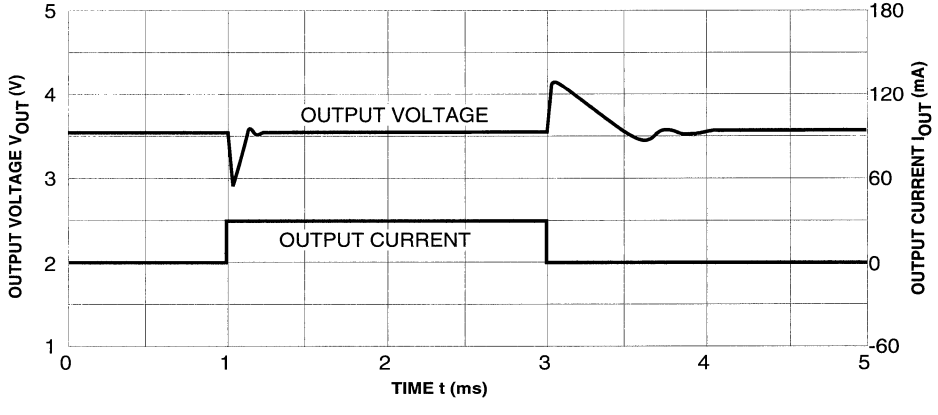


13) Load Transient Response TC161A3624

1) V_{IN} = 3V



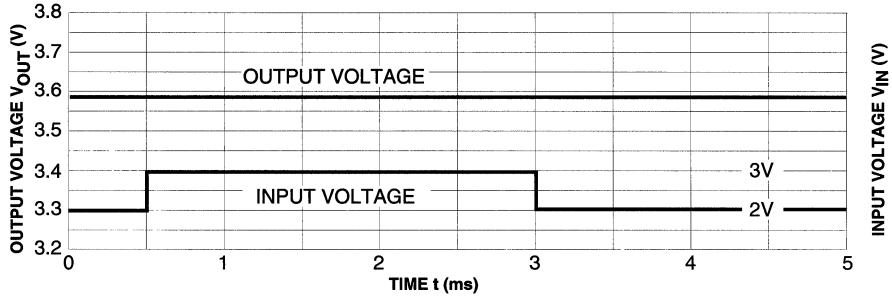
2) V_{IN} = 5V

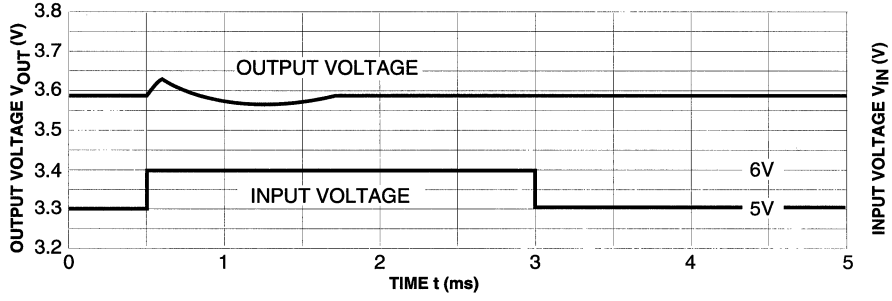


TYPICAL CHARACTERISTICS

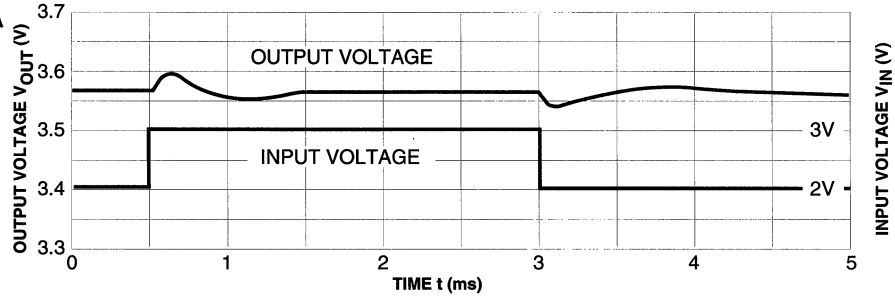
14) Line Transient Response TC161A3624

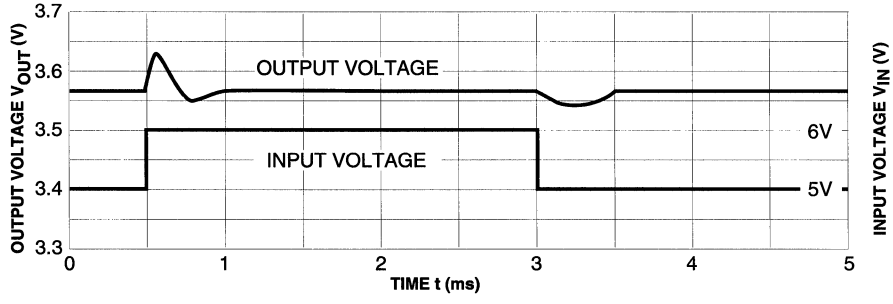
1) I_{OUT} = −1mA





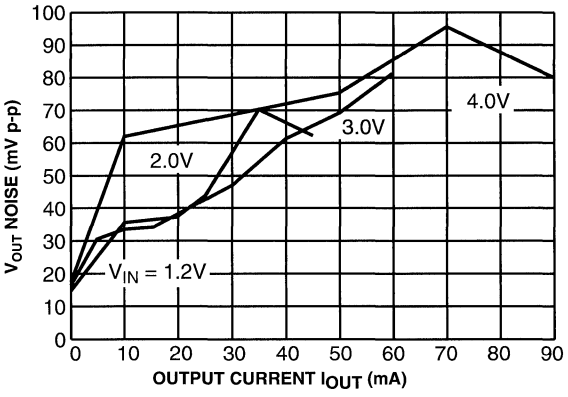
2) I_{OUT} = −30mA





TYPICAL CHARACTERISTICS

TC161A5045



PWM STEP-UP SWITCHING REGULATOR

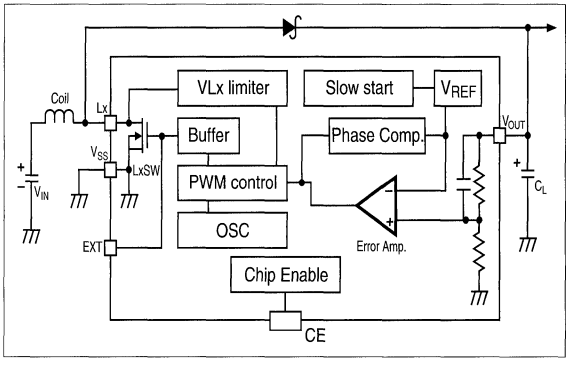
FEATURES

- **Only 3 external components required ..... Coil, diode, capacitor**
- **Low operating current ..... Typ. 30μA**
- **Low ripple and noise**
- **Low voltage operation ..... 0.9V Max. (Output current 1mA)**
- **Wide Choice of V_{OUT} ..... 2.7V to 7.5V in 0.1V Steps**
- **High accuracy output voltage ..... ±2.5% Max.**
- **High efficiency ..... 85% Typ.**
- **Soft start circuit ..... 500μs Min.**
- **Compact packages ..... SOT-89-3 and SOT-89-5**
- **Larger current can be obtained by connecting an external power transistor**

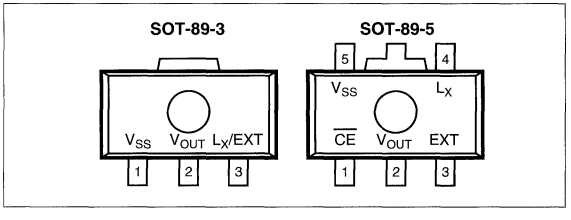
APPLICATIONS

- **Constant voltage source for battery-operated products**
- **Constant voltage source for cameras, electronic and portable communication products**
- **Constant voltage source for devices that require a higher voltage than battery voltages**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The TC17 Series ICs are PWM control step-up switching regulators. Their unique design keeps external components to a minimum.

The TC171AXX IC consists of an oscillator circuit, PWM control circuit, control transistor (Lx switch), reference voltage source, error amplifier circuit, phase correction circuit, voltage detection resistor, soft start circuit, and Lx switch protection circuit. The internal switch allows output currents of 60 to 80 mA

The TC172BXX ICs are similar to the XX1A series, but have an external transistor drive pin (EXT) instead of an Lx pin. This permits connection of a small external power transistor with a low ON resistance to control much larger currents. The TC172BXX ICs are suitable for applications that require output currents up to several hundred milliamps.

The TC173BXX IC allows either connection and also includes a chip enable circuit so that it is possible to set the standby supply current at 0.5 μA max.

A newly developed PWM control circuit allows the TC17 Series ICs to attain the lowest supply current (no load), equal to that of many PFM step-up converters. When V_{IN} exceeds V_{OUT} (plus diode and coil drops), the oscillator circuit stops, reducing current drain to 2μA.

The TC17 Series ICs are recommended for applications which require a low ripple PWM DC/DC converter, but cannot adopt conventional circuits because of their large supply currents.

ORDERING INFORMATION

PART CODE TC17 XX XX XX X XX XXX

Switch Selection:
1A: Internal (see Fig. 1)
2B: External (see Fig. 2)
3B: Internal & External, plus $\overline{CE}$

Output Voltage:
Ex: 30 = 3.0V; 50 = 5.0V

Extra Feature Code: Fixed: 00

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
MB: SOT-89-3, MT: SOT-89-5

Taping Direction:
723: Left Taping, 713: Right Taping

TC17 Series

ABSOLUTE MAXIMUM RATINGS: V_{SS} = 0.0V

Parameter	Symbol	Limit	Unit
Output Voltage	V_{OUT}	12	V
Lx Voltage[1]	VLx	12	V
EXT Pin Voltage[2]	V_{EXT}	– 0.3 to (V_{OUT} + 0.3)	V
$\overline{CE}$ Pin Voltage[3]	V_{CE}	– 0.3 to (V_{OUT} + 0.3)	V
Lx Output Current[1]	I_{LX}	250	mA
EXT Pin Current[2]	I_{EXT}	±50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	– 40 to +85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

NOTES: 1 Applicable for 1AXX & 3BXX
2 Applicable for 2BXX & 3BXX
3 Applicable for 3BXX

PIN DESCRIPTION

Pin No			Name	Description
1AXX	2BXX	3BXX		
1	1	5	V_{SS}	Ground
2	2	2	V_{OUT}	Voltage Output
3	–	4	Lx	Switching Pin
–	3	3	EXT	Transistor Drive Pin (CMOS)
–	–	1	$\overline{CE}$	Chip Enable Pin (Active LOW)

ELECTRICAL CHARACTERISTICS:

TC171A30: V_{OUT} = 3V, V_{IN} = 2V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 2V		0.8	0.9	V
V_{hold}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 2 → 0V	0.7			V
Idd1	Supply Current 1	at V_{OUT} pin		15	25	µA
Idd2	Supply Current 2	at V_{OUT} pin, V_{IN} = 3.5V		2	5	µA
V_{OUT}	Output Voltage		2.925	3.000	3.075	V
ILx	Lx Switching Current	VLx = 0.4V	60			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 3.5V			0.5	µA
f_{osc}	Oscillating Frequency		40	50	60	kHz
maxdty	Max. Oscillator Duty Cycle	on (VLx "Low")	70	80	90	%
η	Efficiency		70	85		%
tst	Soft Start Time[1]	Time for V_{OUT} = 0 → 5V	0.5	2.0		ms
V_{Lxlim}	VLx Pin Voltage Limit[2]	Lx Switch on	0.65	0.8	1.0	V

ELECTRICAL CHARACTERISTICS (continued):

TC171A50: V_{OUT} = 5V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 3V		0.8	0.9	V
V_{hold}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 3 → 0V	0.7			V
Idd1	Supply Current 1	at V_{OUT} pin		30	45	µA
Idd2	Supply Current 2	at V_{OUT} pin, V_{IN} = 5.5V		2	5	µA
V_{OUT}	Output Voltage		4.875	5.000	5.125	V
ILx	Lx Switching Current	VLx = 0.4V	80			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 5.5V			0.5	µA
f_{osc}	Oscillating Frequency		40	50	60	kHz
maxdty	Max. Oscillator Duty Cycle	on (VLx "Low")	70	80	90	%
η	Efficiency		70	85		%
tst	Soft Start Time[1]	Time for V_{OUT} = 0 → 5V	0.5	2.0		ms
V_{Lxlim}	VLx Pin Voltage Limit[2]	Lx Switch on	0.65	0.8	1.0	V

TC172B30: V_{OUT} = 3V, V_{IN} = 2V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	EXT no Load, V_{OUT}: 0 → 2V		0.7	0.8	V
Idd1	Supply Current 1	EXT no Load, V_{OUT} = 2.9V		30	50	µA
Idd2	Supply Current 2	EXT no Load, V_{OUT} = 3.5V		2	5	µA
V_{OUT}	Output Voltage		2.925	3.000	3.075	V
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} = – 0.4V	– 1.5			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	1.5			mA
f_{osc}	Oscillating Frequency		80	100	120	kHz
maxdty	Max. Oscillator Duty Cycle	V_{EXT} "High"	70	80	90	%
tst	Soft Start Time[1]	V_{OUT} = 0 → 3V	0.5	2.0		ms

TC172B50: V_{OUT} = 5V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	EXT no Load, V_{OUT}: 0 → 3V		0.7	0.8	V
Idd1	Supply Current 1	EXT no Load, V_{OUT} = 4.8V		60	90	µA
Idd2	Supply Current 2	EXT no Load, V_{OUT} = 5.5V		2	5	µA
V_{OUT}	Output Voltage		4.875	5.000	5.125	V
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} = – 0.4V	– 2			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	2			mA
f_{osc}	Oscillating Frequency		80	100	120	kHz
maxdty	Max. Oscillator Duty Cycle	V_{EXT} "High"	70	80	90	%
tst	Soft Start Time[1]	V_{OUT} = 0 → 5V	0.5	2.0		ms

ELECTRICAL CHARACTERISTICS (continued):

TC173B30: V_{OUT} = 3.0V, V_{IN} = 2V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		2.925	3.0	3.075	V
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 2V		0.8	0.9	V
V_{hold}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 2 → 0V	0.7			V
η	Efficiency		70	85		%
Idd1	Supply Current 1	at V_{OUT} pin		30	50	µA
Idd2	Supply Current 2	at V_{OUT} pin, V_{IN} = 3.5V		2	5	µA
ILx	Lx Switching Current	VLx = 0.4V	60			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 3.5V			0.5	µA
$I_{EXT}H$	EXT "H" Output Current	$V_{EXT} = V_{OUT} - 0.4V$	– 1.5			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	1.5			mA
V_{CEH1}	$\overline{CE}$ Input Voltage "H"1	$V_{OUT} \geq 1.5V$	V_{OUT} – 0.4			V
V_{CEL1}	$\overline{CE}$ Input Voltage "L"1	$V_{OUT} \geq 1.5V$			0.4	V
V_{CEH2}	$\overline{CE}$ Input Voltage "H"2	$0.8V \leq V_{OUT} \leq 1.5V$	V_{OUT} – 0.1			V
V_{CEL2}	$\overline{CE}$ Input Voltage "L"2	$0.8V \leq V_{OUT} \leq 1.5V$			0.1	V
I_{CEH}	$\overline{CE}$ Input Current "H"	$\overline{CE}$ = 3V	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ Input Current "L"	$\overline{CE}$ = 0V	– 0.5		0.5	µA
f_{osc}	Oscillating Frequency		80	100	120	kHz
maxdty	Max. Oscillator Duty Cycle	on (VLx "Low")	70	80	90	%
t_{start}	Soft Start Time[1]	V_{OUT} = 0→ 3V	0.5	2.0		ms
V_{Lxlim}	Lx Pin Voltage Limit[2]	Lx Switch on	0.65	0.8	1.0	V

ELECTRICAL CHARACTERISTICS (continued):

TC173B50: V_{OUT} = 5.0V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		4.875	5.0	5.125	V
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 3V		0.8	0.9	V
V_{hold}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 3 → 0V	0.7			V
η	Efficiency		70	85		%
Idd1	Supply Current 1	at V_{OUT} pin		60	90	µA
Idd2	Supply Current 2	at V_{OUT} pin, V_{IN} = 5.5V		2	5	µA
ILx	Lx Switching Current	VLx = 0.4V	80			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 5.5V			0.5	µA
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} – 0.4V	– 2.0			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	2.0			mA
V_{CEH1}	$\overline{CE}$ Input Voltage "H"1	V_{OUT} ≥ 1.5V	V_{OUT} – 0.4			V
V_{CEL1}	$\overline{CE}$ Input Voltage "L"1	V_{OUT} ≥ 1.5V			0.4	V
V_{CEH2}	$\overline{CE}$ Input Voltage "H"2	0.8V ≤ V_{OUT} ≤ 1.5V	V_{OUT} – 0.1			V
V_{CEL2}	$\overline{CE}$ Input Voltage "L"2	0.8V ≤ V_{OUT} ≤ 1.5V			0.1	V
I_{CEH}	$\overline{CE}$ Input Current "H"	$\overline{CE}$ = 5V	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ Input Current "L"	$\overline{CE}$ = 0V	– 0.5		0.5	µA
f_{osc}	Oscillating Frequency		80	100	120	kHz
maxdty	Max. Oscillator Duty Cycle	on (VLx "Low")	70	80	90	%
t_{start}	Soft Start Time[1]	V_{OUT} = 0 → 5V	0.5	2.0		ms
V_{Lxlim}	VLx Pin Voltage Limit[2]	Lx Switch on	0.65	0.8	1.0	V

Note 1: The soft start circuit follows the sequence below:
When V_{IN} is applied → V_{REF} is kept at 0V for about 200µs → During this period, error amplifier output is brought to "H" → V_{REF} rises and then the error amplifier output gradually decreases to the appropriate value due to the internal phase compensation circuit. Accordingly, the output gradually increases.

Note 2: ILx gradually rises after the Lx switch is turned on, and VLx rises accordingly. If the voltage reaches Lxlim, the Lx switch protection circuit turns off the Lx switch.

NOTICE

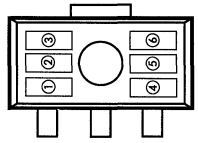
To use these ICs, note the following points:

- Place external components as close as possible to the IC to reduce wiring. In particular, wire the capacitor connected to the V_{OUT} pin using the shortest route possible.
- Ensure sufficient grounding. The V_{SS} pin receives large currents due to switching. High impedance in the V_{SS} routing causes the internal potential of the IC to fluctuate with the switching current, resulting in unstable operation.
- Use capacitors with good high frequency response, such as tantalum capacitors or electrolytic aluminum + ceramic capacitors. The capacity must be 10µF or more. It is recommended that the rated voltage of the capacitors be at least three times the specified output voltage, because the coil may cause a high spike-like voltage when the Lx transistor is turned off.
- Select coils that have a small DC resistance and are not magnetically-saturated easily. If the coil inductance is too small, ILx may exceed the absolute maximum rating under maximum load. Select the proper inductance value.
- Use Schottky diodes with fast switching speed, and adequate current-carrying capability.

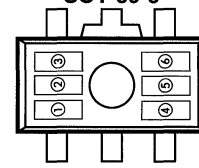
TC17 Series

MARKING

SOT-89-3



SOT-89-5



a and b represents first digit and decimal place of V_{OUT}. For example:

Mark a	Mark b	V_{OUT} Voltage
2	7	2.7V

c represents driver type

Mark c	Type		
1	1	TC171AXX	Internal Switch (SOT-89-3-only)
2	2	TC172BXX	External Switch (SOT-89-3-only)
3	3	TC173BXX	Int./Ext. Switch, plus $\overline{CE}$ (SOT-89-5-only)

d and e represent assembly lot number

f represents oscillator frequency

Mark f	Type	
A	A	50kHz
B	B	100kHz

TEST CIRCUITS

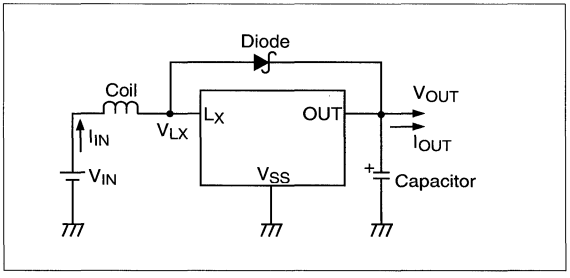


Figure 1. TC171AXX

Parts

	Capacitor	22µF (Tantalum)
	Coil	120 µH, 270 µH (Sumida Electric Company Ltd., CM-5)
	Diode	MA721 (Matsushita Electronics Corp., Schottky)

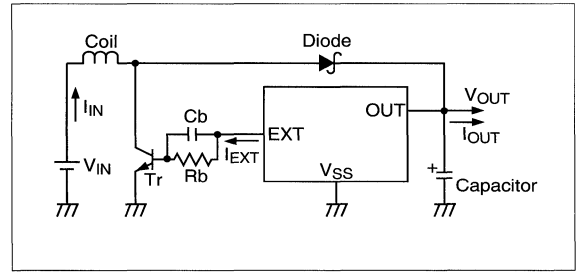


Figure 2. TC172BXX

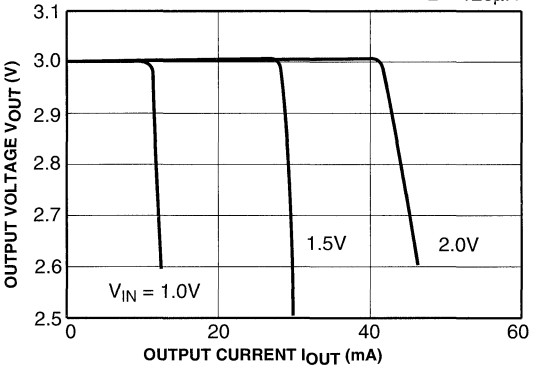
Parts

	Capacitor	100µF (Aluminum Electrolytic)// 22µF (Tantalum)
	Coil	28µH (Sumida Electric Company Ltd., CM-5)
	Diode	MA721 (Matsushita Electronics Corp., Schottky)
	Transistor	2SD1628G
	Rb	300Ω
	Cb	0.01µF

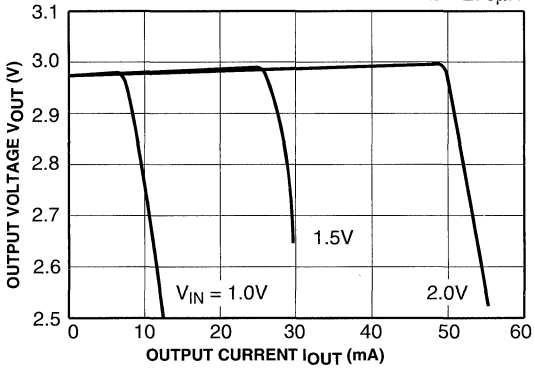
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current (T_A = 25°C)

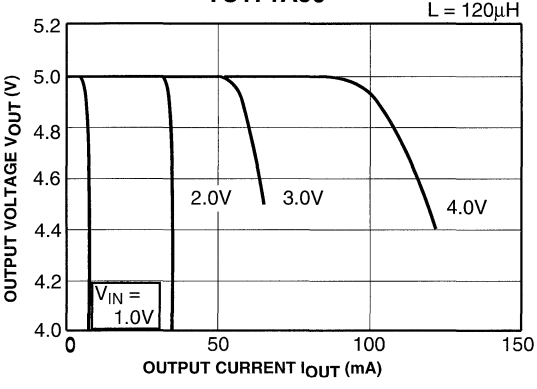
TC171A30



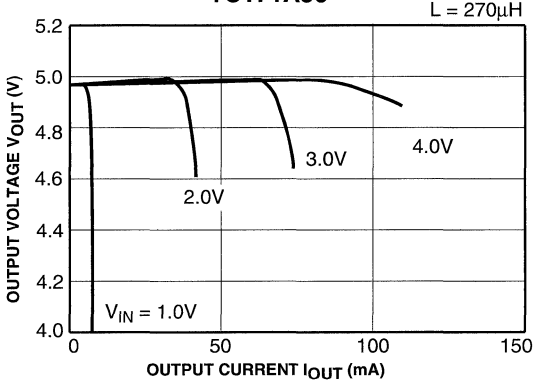
TC171A30



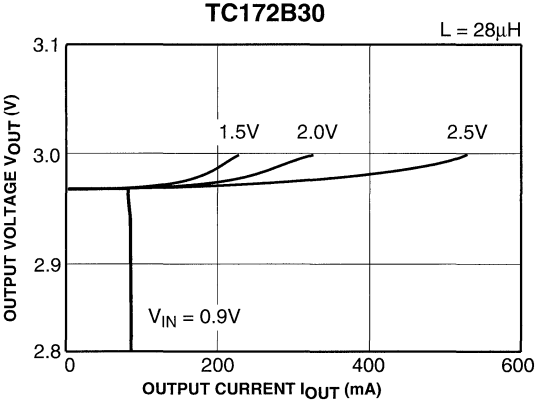
TC171A50



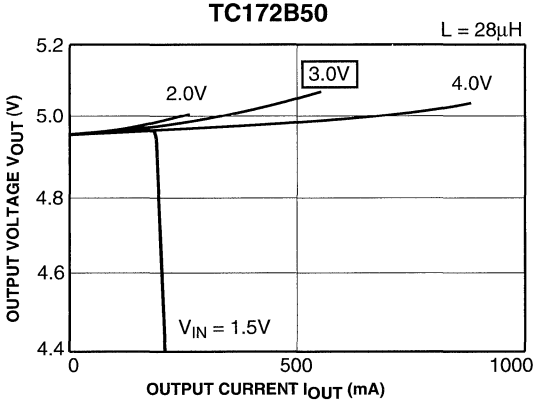
TC171A50



TC172B30



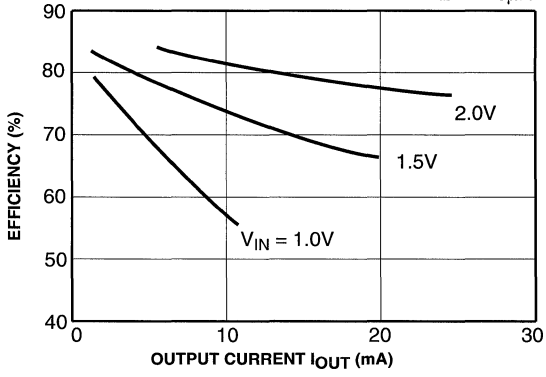
TC172B50



TYPICAL CHARACTERISTICS

2) Efficiency vs. Output Current (T_A = 25°C)

TC171A30



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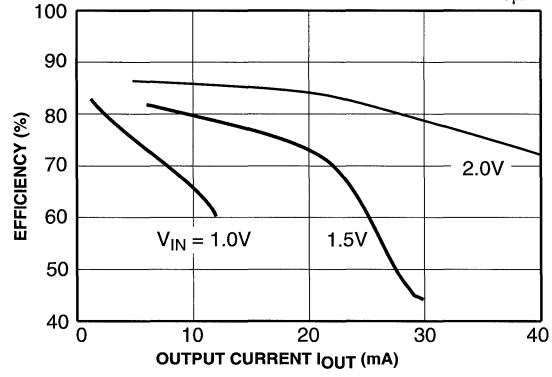
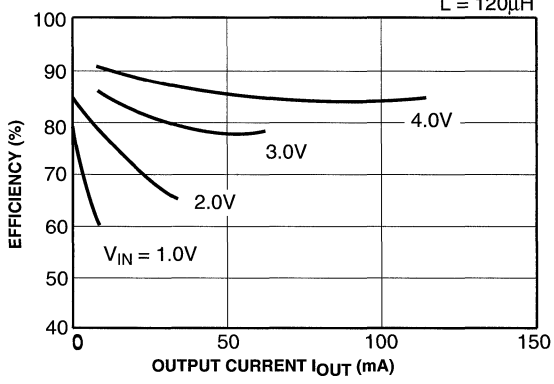
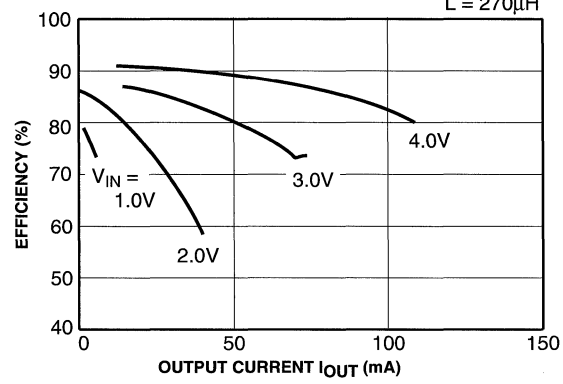


TC171A50



TC171A50



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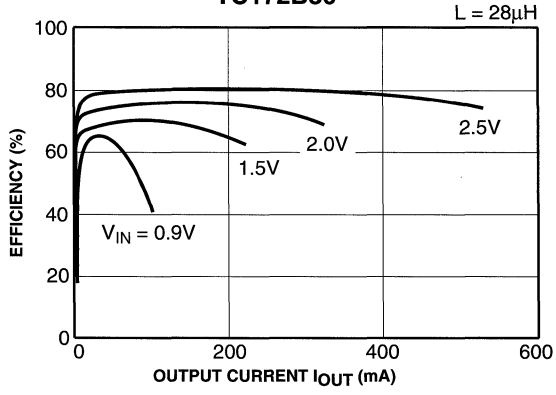
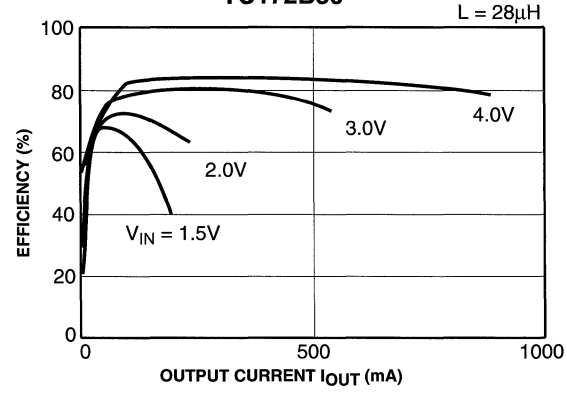
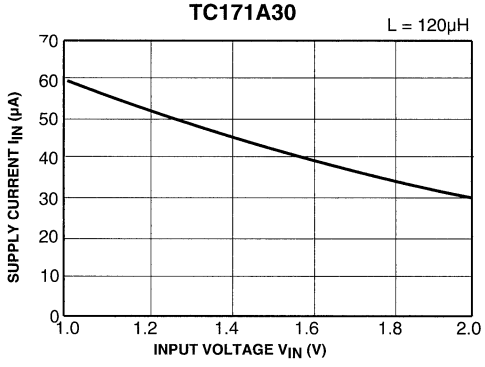


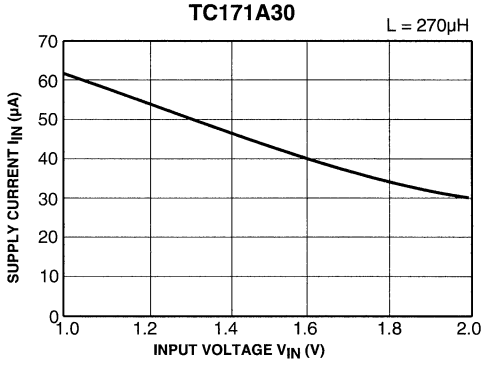
TC172B50

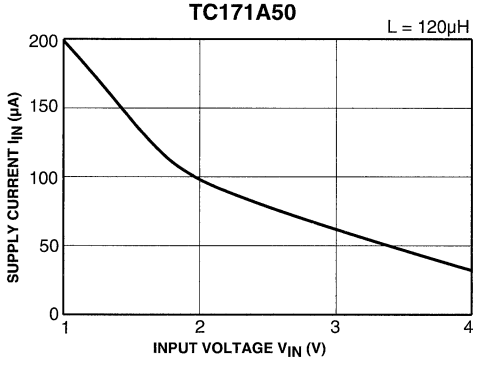


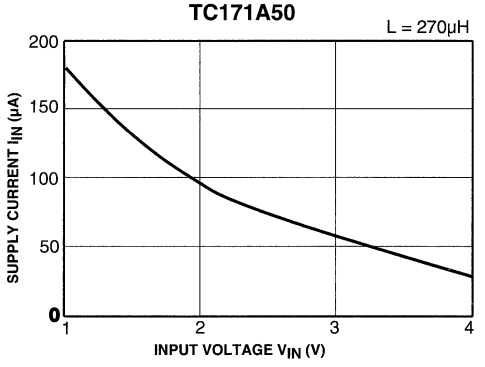
TYPICAL CHARACTERISTICS

3) Supply Current (No Load) vs. Input Voltage (T_A = 25°C)







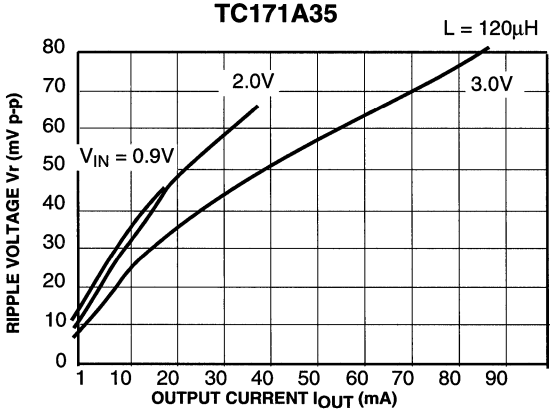


TC17 Series

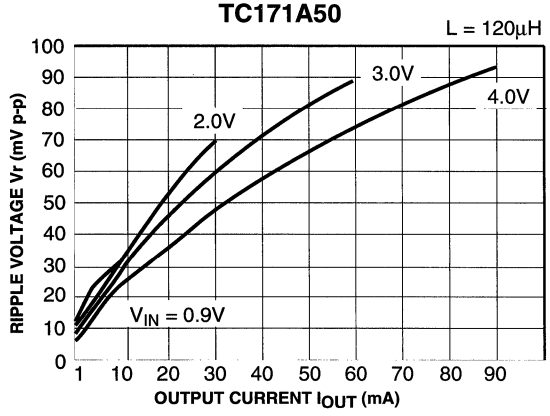
TYPICAL CHARACTERISTICS

4) Output Ripple Voltage vs. Output Current (T_A = 25°C)

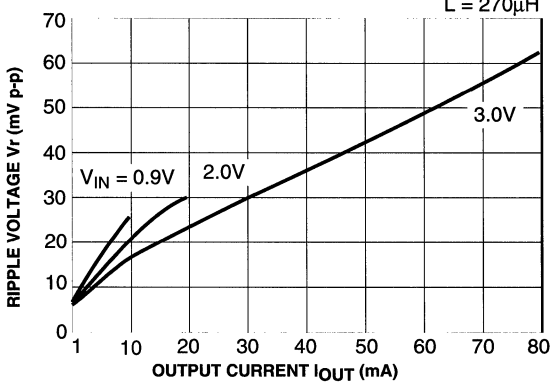
TC171A35



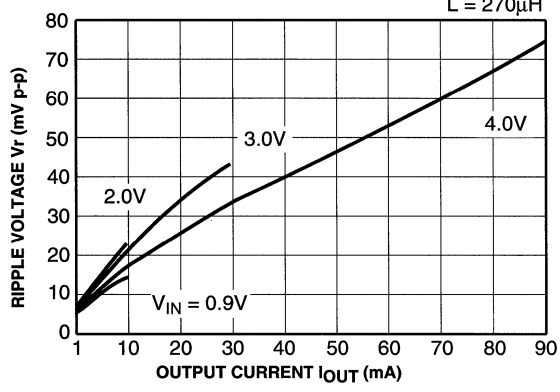
TC171A50



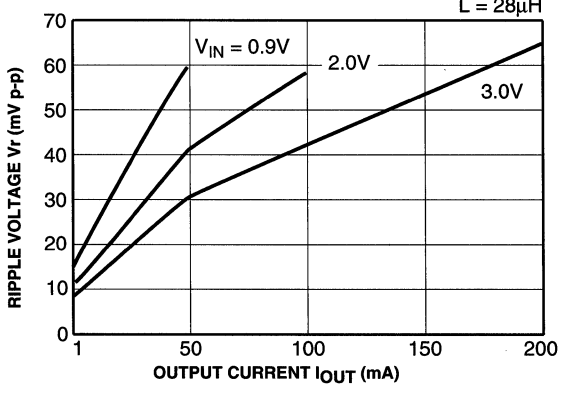
TC171A35



TC171A50



TC172B35



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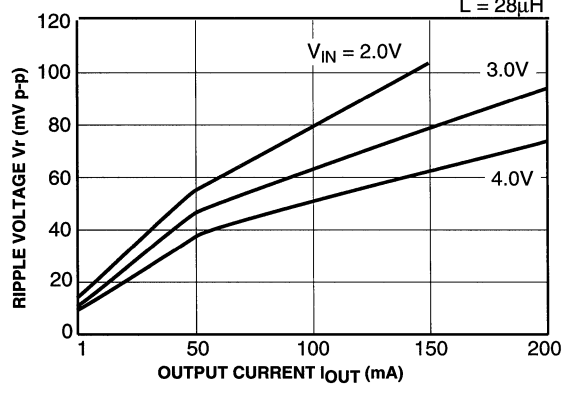
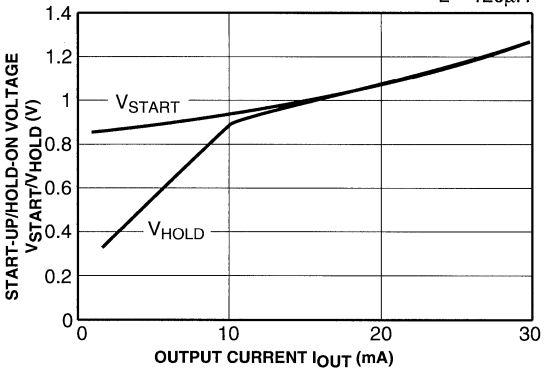


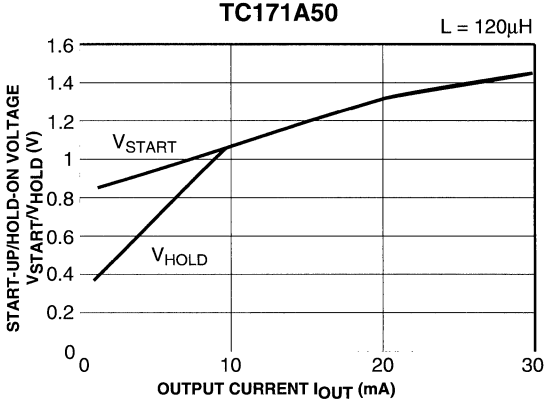
TYPICAL CHARACTERISTICS

5) Start-up/Hold-on Voltage vs. Output Current (T_A = 25°C)

TC171A35



TC171A50



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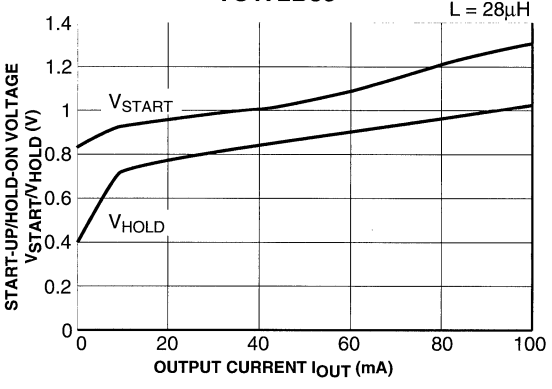

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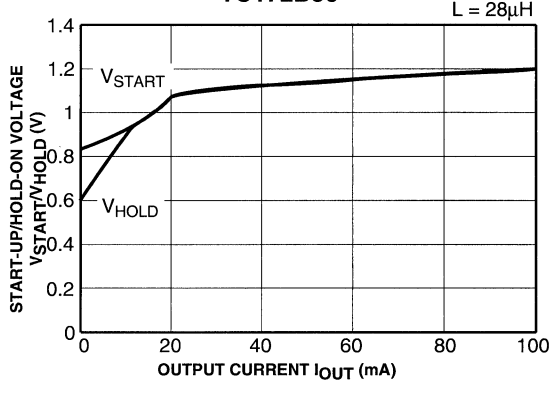

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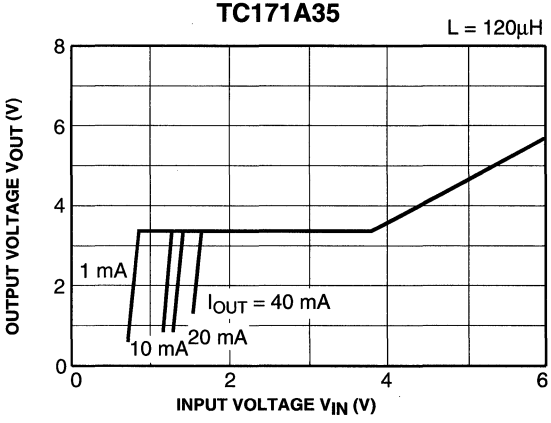
TC17 Series

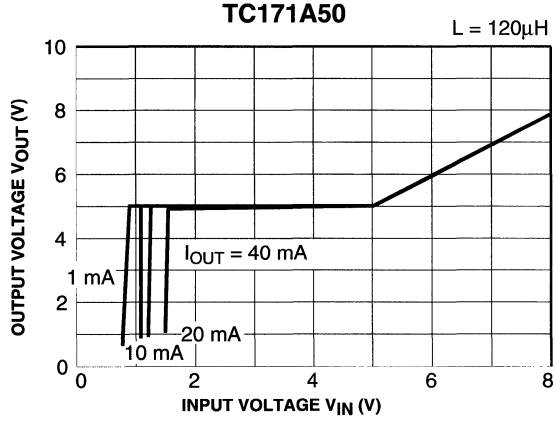
TYPICAL CHARACTERISTICS

6) Output Voltage vs. Input Voltage (T_A = 25°C)

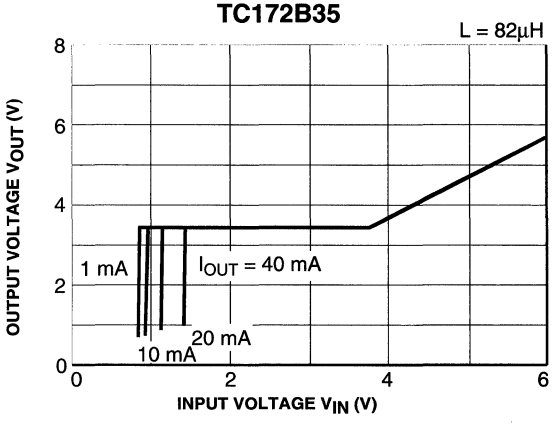
TC171A35



TC171A50



TC172B35



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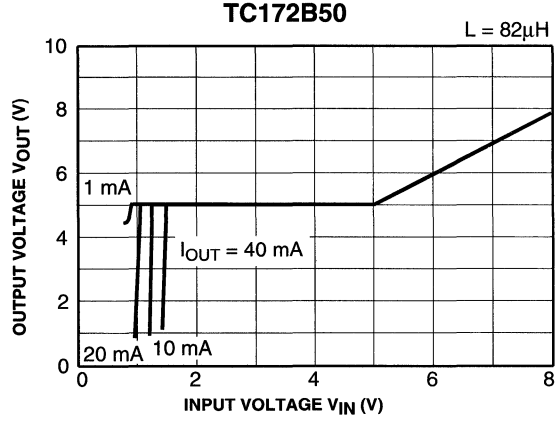
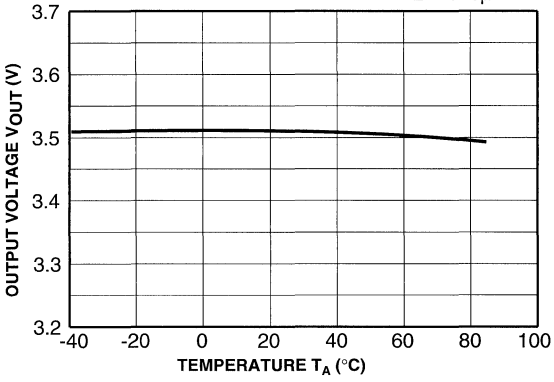


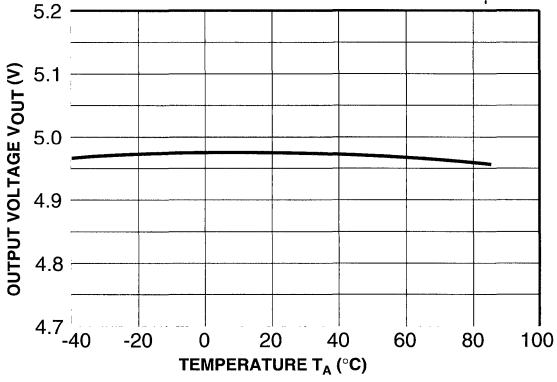
TYPICAL CHARACTERISTICS

7) Output Voltage vs. Temperature (T_A = 25°C)

TC171A35



TC171A50



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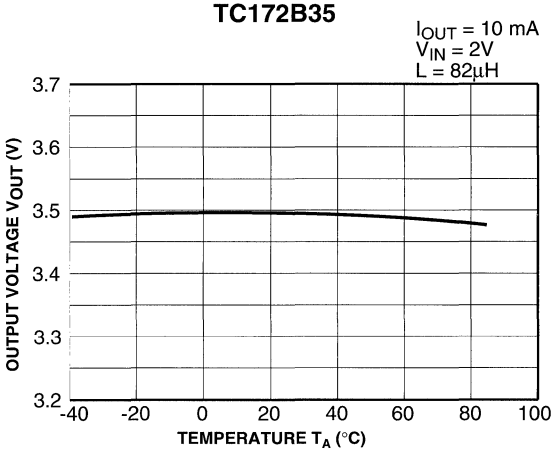

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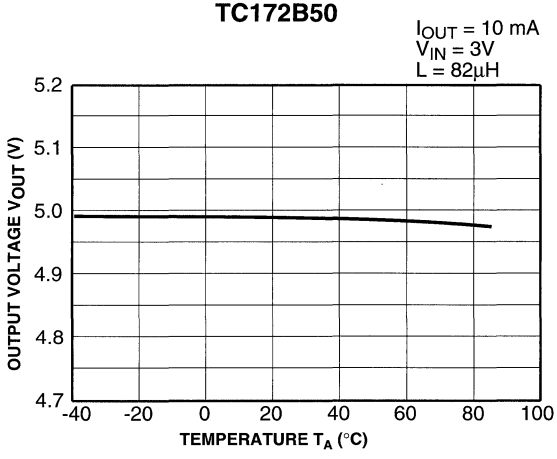

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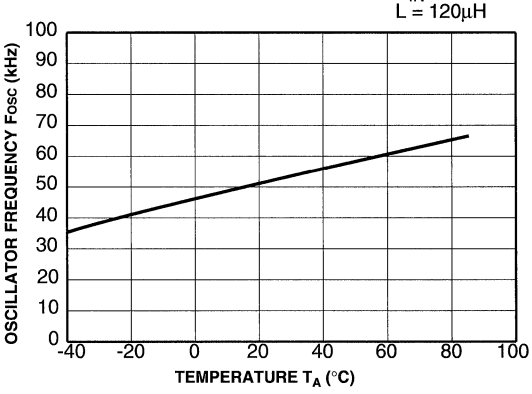
TYPICAL CHARACTERISTICS

8) Oscillator Frequency vs. Temperature (T_A = 25°C)

TC171A35



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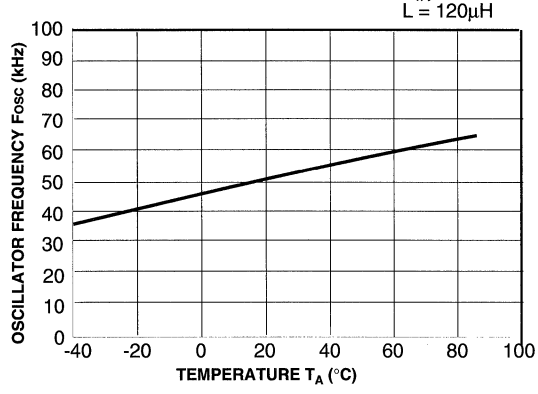

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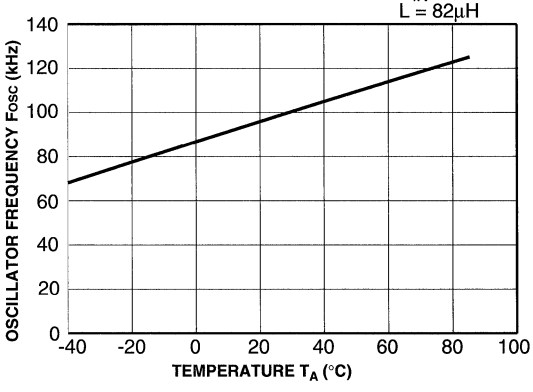

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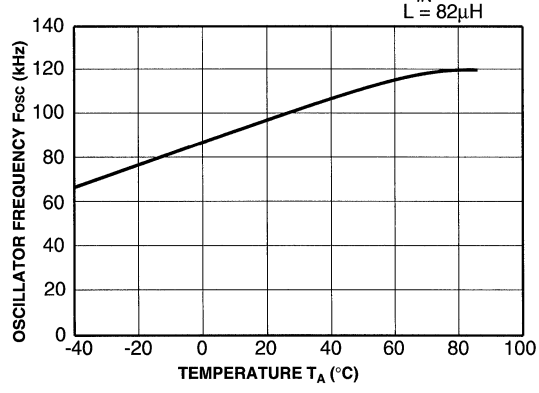
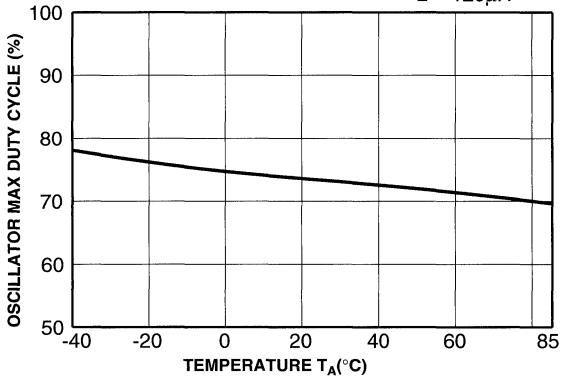


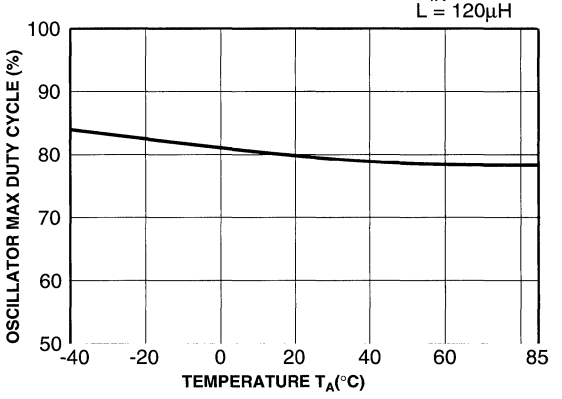
TYPICAL CHARACTERISTICS

9) Oscillator Max Duty Cycle vs. Temperature (T_A = 25°C)

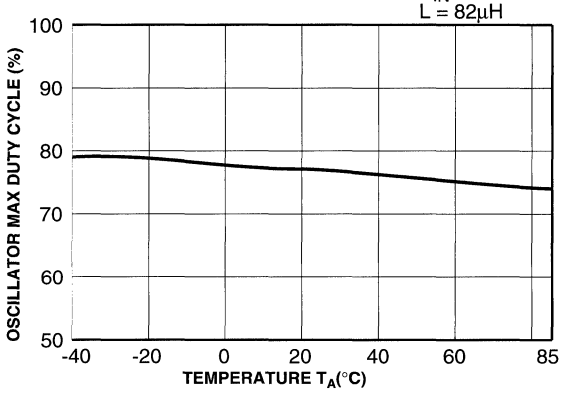
TC171A35



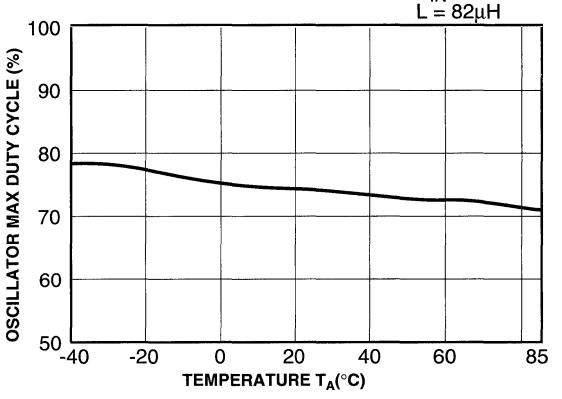
TC171A50



TC172B35



TC172B50

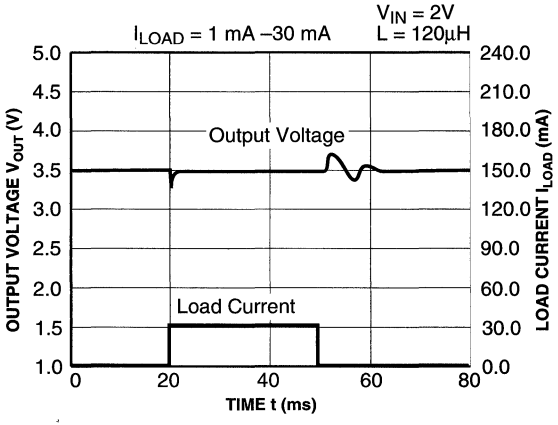


TC17 Series

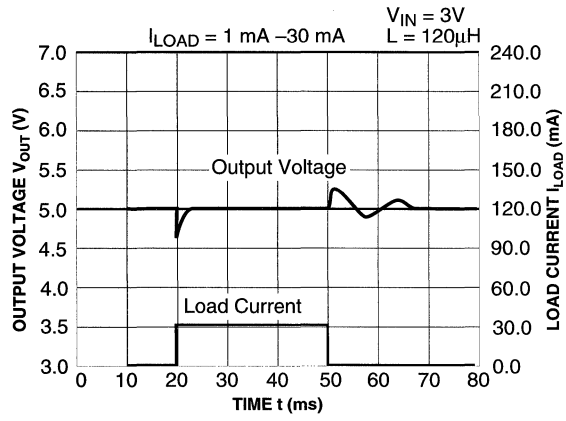
TYPICAL CHARACTERISTICS

10) Load Transient Response (T_A = 25°C)

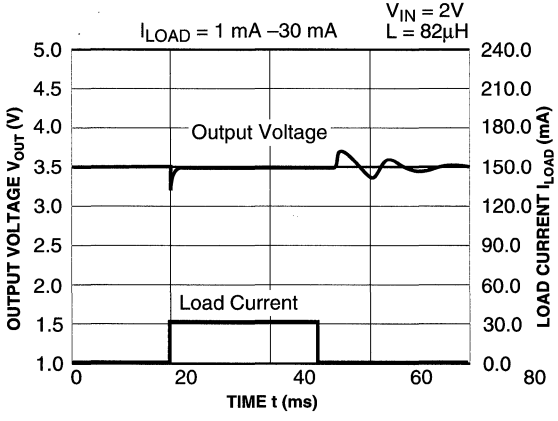
TC171A35



TC171A50



TC172B35



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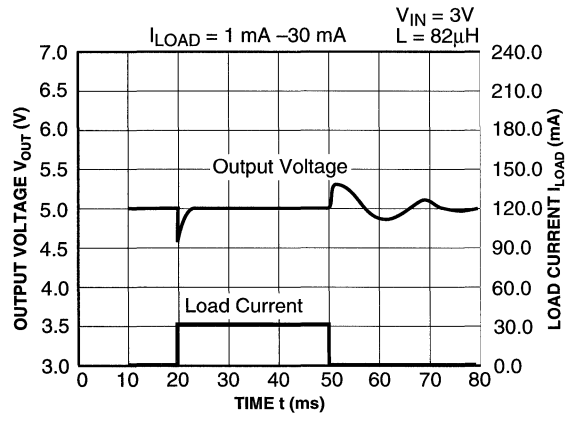
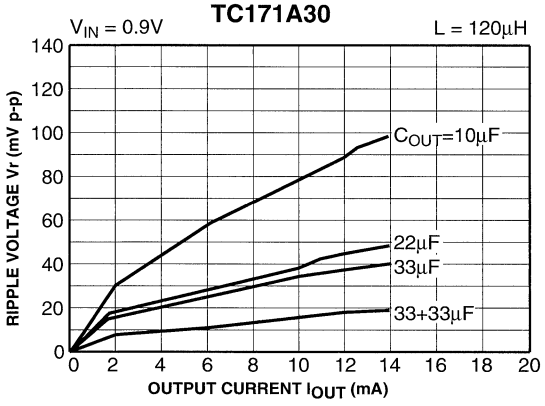
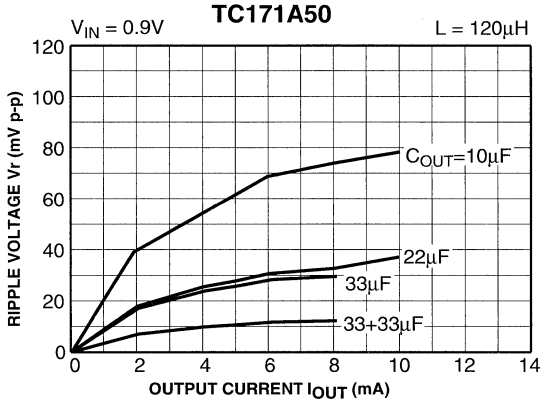
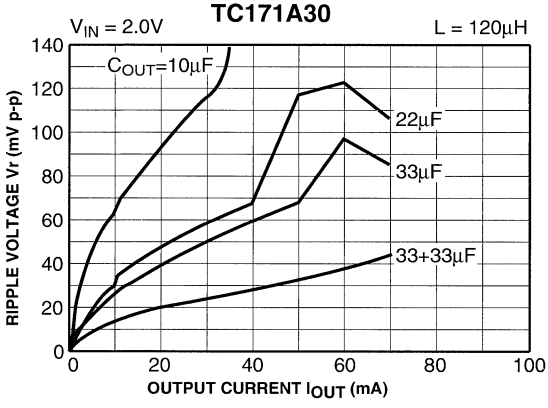


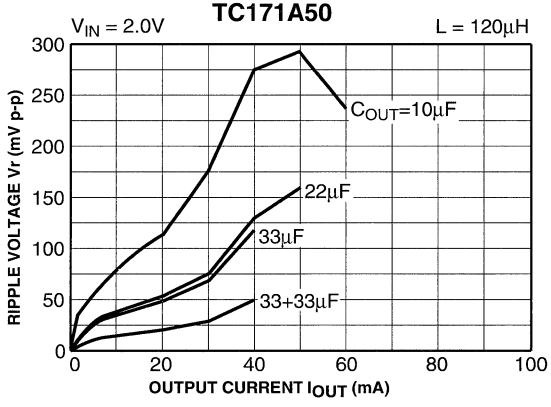
TYPICAL CHARACTERISTICS

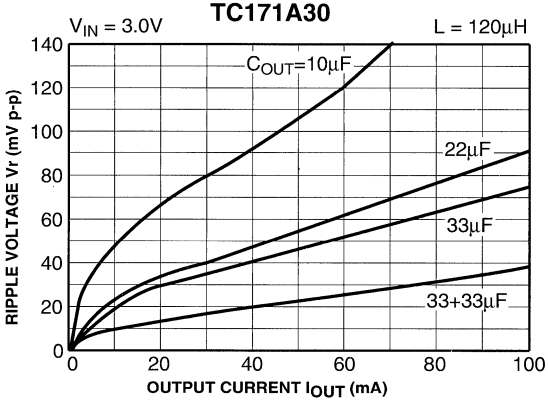
11) Ripple Voltage vs. Output Current (T_A = 25°C)

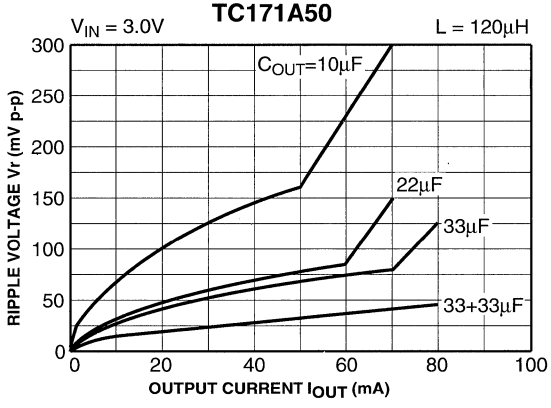








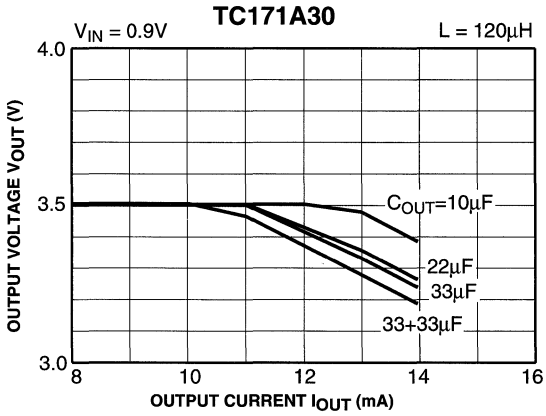


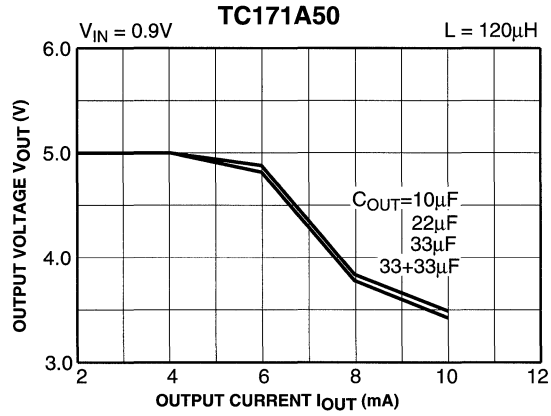


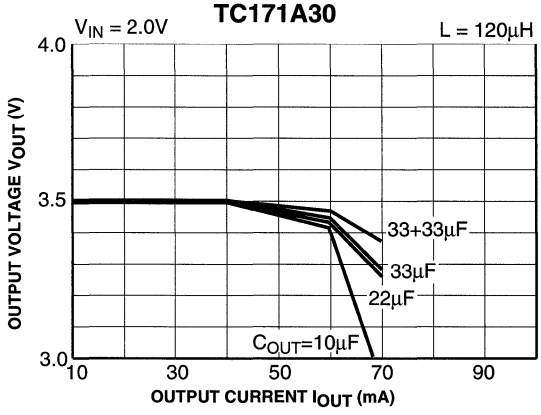
TC17 Series

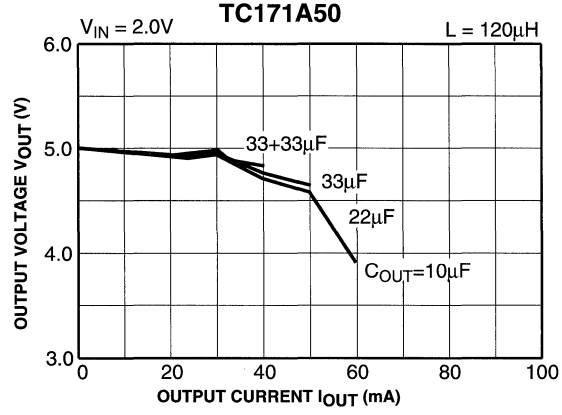
TYPICAL CHARACTERISTICS

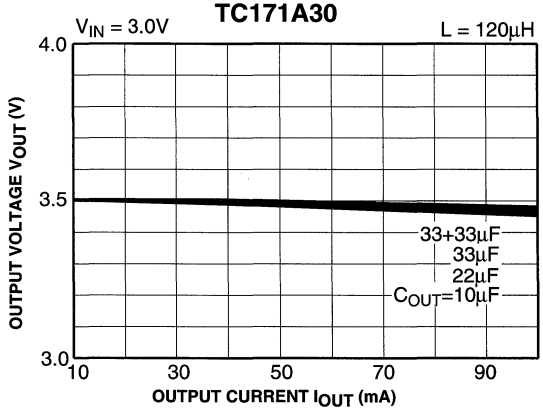
12) Output Voltage vs. Output Current

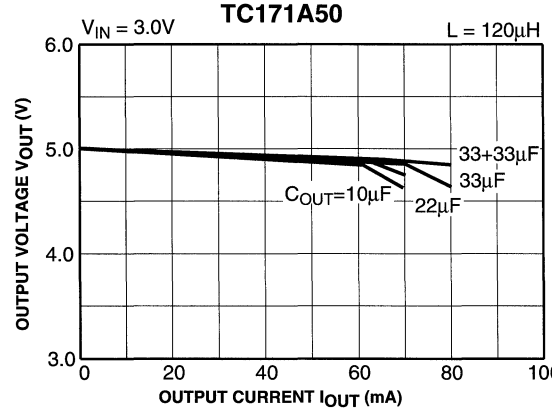






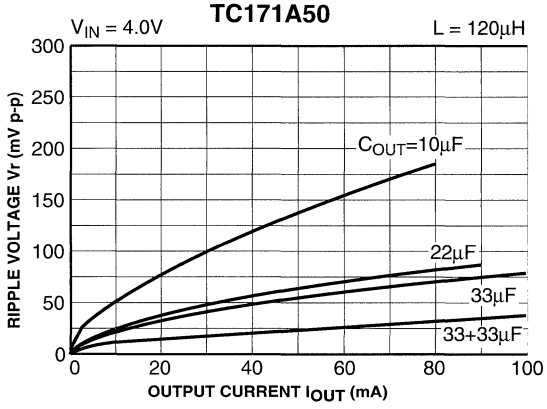


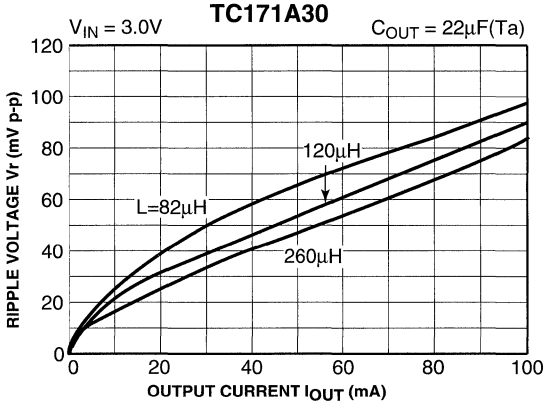


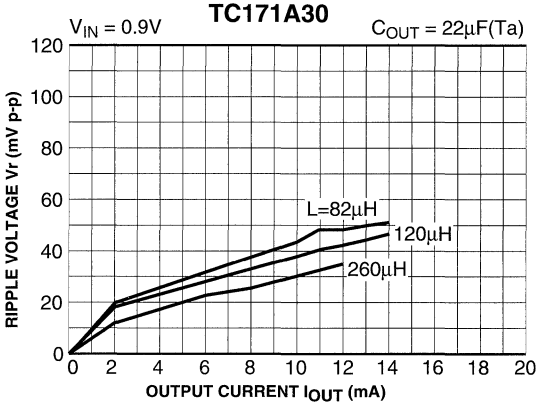


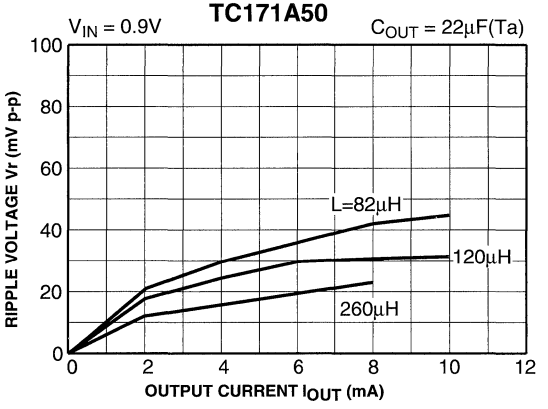
TYPICAL CHARACTERISTICS

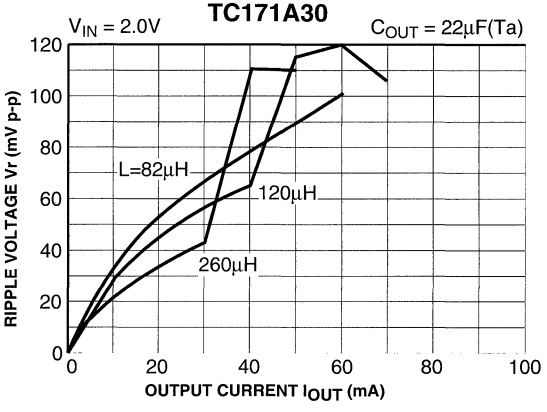
13) Ripple Voltage vs. Output Current

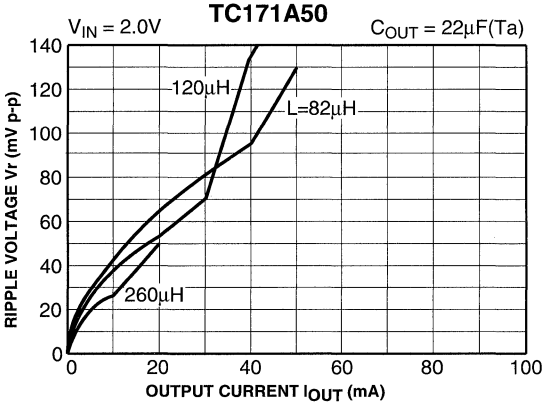








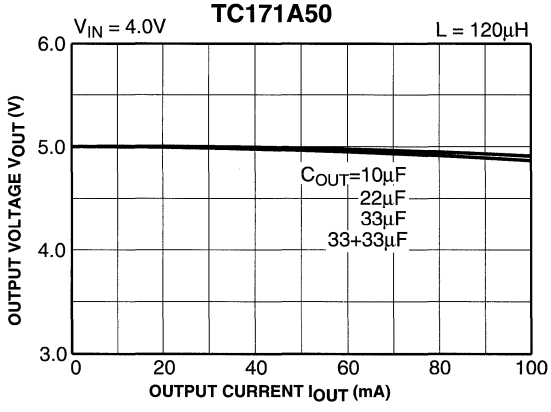


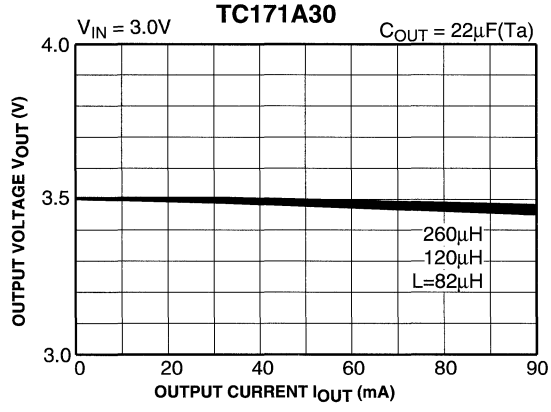


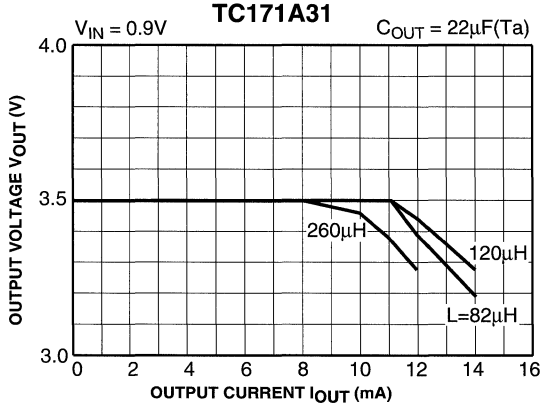
TC17 Series

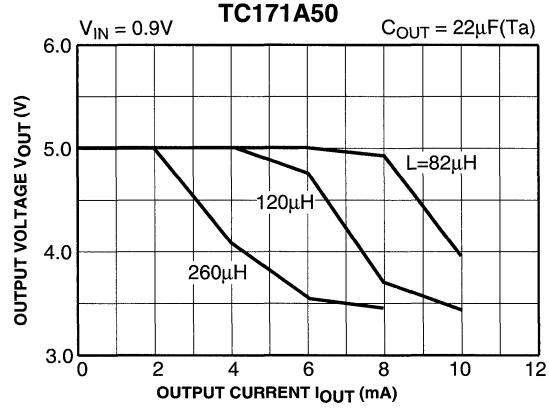
TYPICAL CHARACTERISTICS

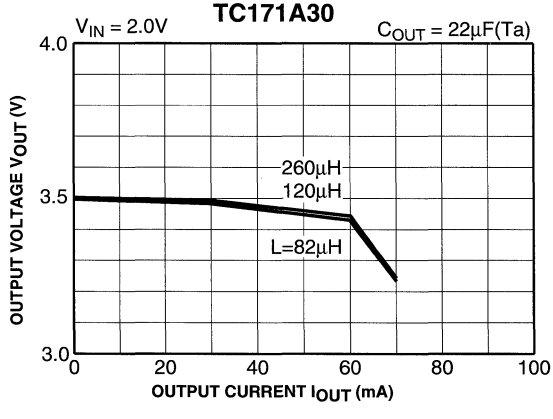
14) Output Voltage vs. Output Current

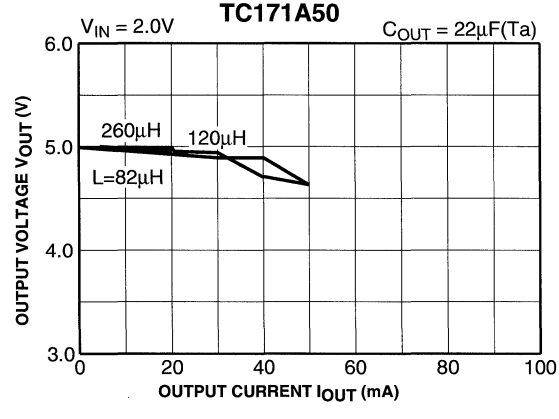






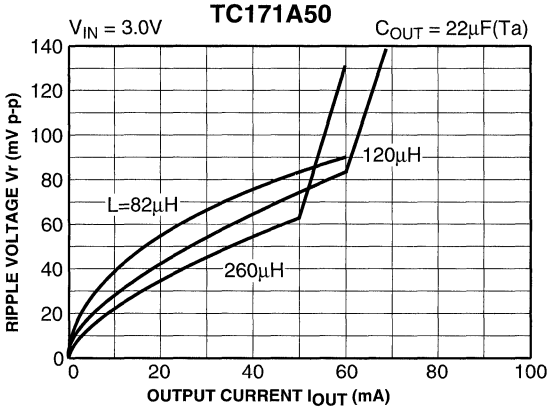


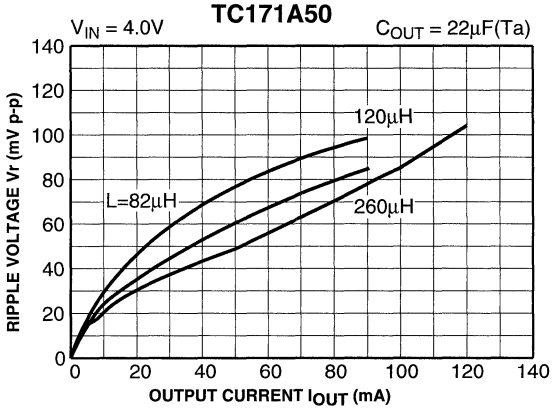




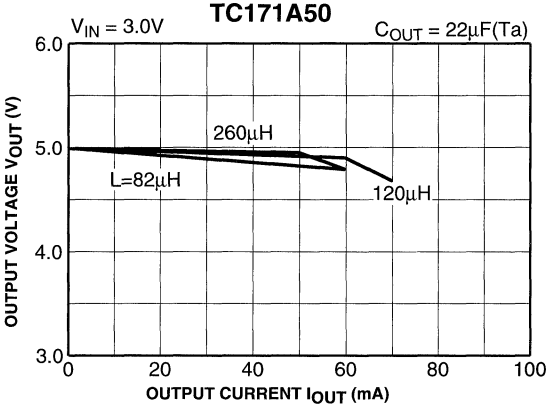
TYPICAL CHARACTERISTICS

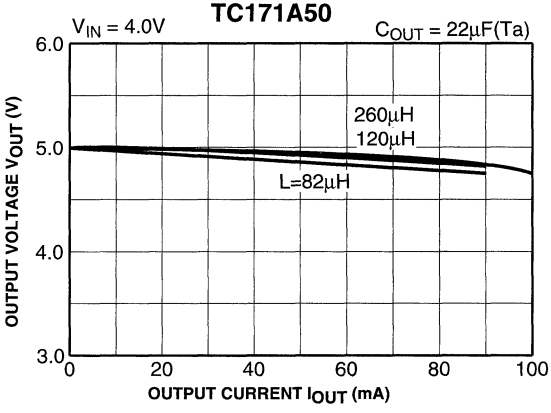
15) Ripple Voltage vs. Output Current (T_A = 25°C)





16) Output Voltage vs. Output Current





PFM STEP-UP SWITCHING REGULATORS

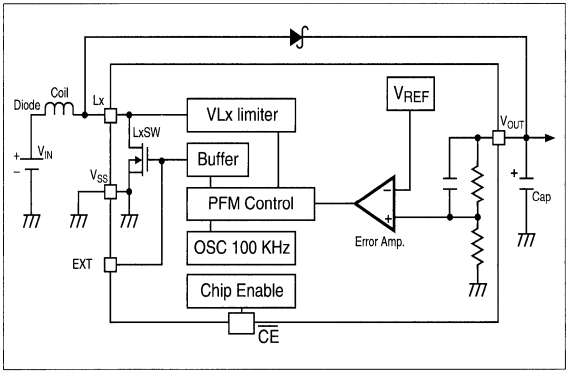
FEATURES

- **Only 3 external components required ..... Coil, diode, capacitor**
- **Ultra low operating current ..... 4 - 6μA, Typ.**
- **Wide Choice of V_{OUT} ..... 2.5V to 7.5V in 0.1V Steps**
- **High-accuracy output voltage..... ±2.5% Max.**
- **Low noise**
- **Low voltage operation ..... 0.9V Max. (Output current 1mA)**
- **High efficiency ..... 80% Typ.**
- **Compact packages ..... SOT-89-3 and SOT-89-5**
- **Larger current can be obtained by connecting an external power transistor**

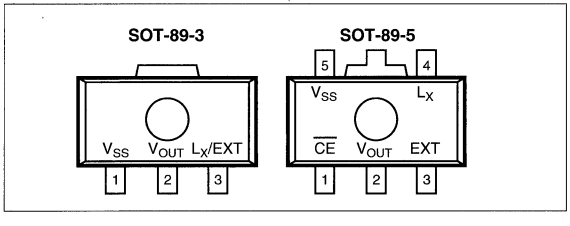
APPLICATIONS

- **Constant voltage supply for battery-operated products**
- **Constant voltage supply for cameras, electronic and portable communication products**
- **Constant voltage source for devices that require a higher voltage than battery voltages**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The TC18 Series are PFM-control, low operating current, step-up switching regulator ICs. Their unique design keeps the required external components to a minimum. PFM control can allow even less operating current than PWM control.

The TC181BXX IC comprises an oscillator, PFM control circuit, control transistor (Lx switch), reference voltage, differential amplifier circuit, voltage sensing resistor and an Lx switch protective circuit, and requires only three externally connected components (a coil, diode and capacitor). The internal switch allows output currents of 60 to 80 mA.

The TC182BXX IC utilizes the same chip as the TC181BXX device, but a transistor drive terminal (EXT) appears in place of the Lx terminal. This permits connection of a small external power transistor with a low ON resistance to control much larger currents. This device is ideal for applications which require outputs up to several hundred milliamps.

The TC183BXX version allows either connection and includes an internal chip enable circuit so that is possible to set the standby supply current to 0.5 μA max.

The TC18 Series is ideal for use with battery-operated devices, and combines high-efficiency operation with low noise and ultra-low current consumption.

ORDERING INFORMATION

PART CODE **TC18 XX XX XX X XX XXX**

Switch Selection:
- 1B: Internal (see Fig. 1)
- 2B: External (see Fig. 2)
- 3B: Internal & External, plus $\overline{CE}$

Output Voltage:
Ex: 30 = 3.0V; 50 = 5.0V

Extra Feature Code: Fixed: 00

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
MB: SOT-89-3, MT: SOT-89-5

Taping Direction:
723: Left Taping, 713: Right Taping

TC18 Series

ABSOLUTE MAXIMUM RATINGS:

Parameter	Symbol	Limit	Unit
Output Voltage	V_{OUT}	12	V
Lx Voltage	VLx	12	V
EXT Pin Voltage	V_{EXT}	– 0.3 to (V_{OUT} + 0.3)	V
Lx Output Current	ILx	250	mA
EXT Pin Current	I_{EXT}	±50	mA
Power Dissipation	Pd	500	mW
Operating Temperature	T_A	– 40 to +85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
$\overline{CE}$ Pin Voltage	V_{CE}	– 0.3 to (V_{OUT} + 0.3)	V

PIN DESCRIPTION

Pin No			Name	Description
XX1	XX2	XX3		
1	1	5	V_{SS}	Ground
2	2	2	V_{OUT}	Voltage Output
3	–	4	Lx	Switching Pin
–	3	3	EXT	Transistor Drive Pin (CMOS)
–	–	1	$\overline{CE}$	Chip Enable Pin (Active LOW)

ELECTRICAL CHARACTERISTICS:

TC181B30: V_{OUT} = 3V, V_{IN} = 2V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		2.925	3.000	3.075	V
V_{IN}	Max. Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 2V		0.8	0.9	V
V_{hdl}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 2 → 0V	0.7			V
$I_{IN}1$	Input Current 1	at V_{IN} pin, No Load		4	8	µA
$I_{IN}2$	Input Current 2	at V_{IN} pin, V_{IN} = 3.5V		2	5	µA
ILx	Lx Switching Current	VLx = 0.4V	60			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 3.5V			0.5	µA
f_{osc}	Oscillator Frequency		80	100	120	kHz
maxdty	Oscillator Duty Cycle	on (VLx "Low")	65	75	85	%
η	Efficiency		70	80		%
V_{LXlim}	VLx Pin Voltage Limit[1]	Lx Switch on	0.65	0.8	1.0	V

TC181B50: V_{OUT} = 5V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		4.875	5.000	5.125	V
V_{IN}	Max. Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 3V		0.8	0.9	V
V_{hdl}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 3 → 0V	0.7			V
$I_{IN}1$	Input Current 1	at V_{IN} pin, No Load		6	12	µA
$I_{IN}2$	Input Current 2	at V_{IN} pin, V_{IN} = 5.5V		2	5	µA
ILx	Lx Switching Current	VLx = 0.4V	80			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 5.5V			0.5	µA
f_{osc}	Oscillator Frequency		80	100	120	kHz
maxdty	Oscillator Duty Cycle	on (VLx "Low")	65	75	85	%
η	Efficiency		70	80		%
V_{LXlim}	VLx Pin Voltage Limit[1]	Lx Switch on	0.65	0.8	1.0	V

ELECTRICAL CHARACTERISTICS (continued):

TC182B30: V_{OUT} = 3V, V_{IN} = 2V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		2.925	3.000	3.075	V
V_{IN}	Max. Input Voltage				8	V
V_{ST}	Starting Voltage	EXT no Load, V_{OUT}: 0 → 2V		0.7	0.8	V
Idd1	Operating Current 1	EXT no Load, V_{OUT} = 2.9V		30	50	µA
Idd2	Operating Current 2	EXT no Load, V_{OUT} = 3.5V		2	5	µA
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} = – 0.4V	– 1.5			mA
$I_{EXT}L$	EXT "Low" Output Current	V_{EXT} = 0.4V	1.5			mA
f_{osc}	Oscillator Frequency		80	100	120	kHz
maxdty	Oscillator Duty Cycle	V_{EXT} "High"	65	75	85	%

TC182B50: V_{OUT} = 5V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified. (See Fig. 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		4.875	5.000	5.125	V
V_{IN}	Max. Input Voltage				8	V
V_{ST}	Starting Voltage	EXT no Load, V_{OUT}: 0 → 3V		0.7	0.8	V
Idd1	Operating Current 1	EXT no Load, V_{OUT} = 4.8V		60	90	µA
Idd2	Operating Current 2	EXT no Load, V_{OUT} = 5.5V		2	5	µA
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} = - 0.4V	– 2			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	2			mA
f_{osc}	Oscillator Frequency		80	100	120	kHz
maxdty	Oscillator Duty Cycle	V_{EXT} "High"	65	75	85	%

CIRCUIT EXAMPLES

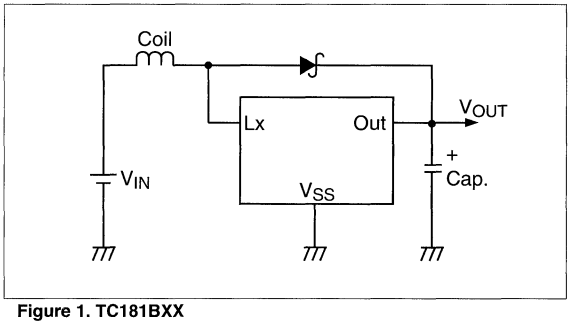


Figure 1. TC181BXX

Parts

Coil	82 µH	(Sumida Electric Company Ltd. CM-5)
Diode	MA721	(Matsushita Electronics Corp. Schottky)
Capacitor	22µF	(Tantalum)

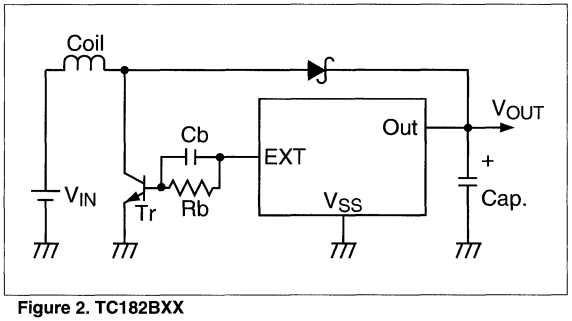


Figure 2. TC182BXX

Parts

Coil	28µH (Toroidal Core)
Diode	HRP22 (Hitachi, Schottky)
Capacitor	100µF (Tantalum)
Transistor	2SD1628G
Rb	300Ω
Cb	0.01µF

TC18 Series

ELECTRICAL CHARACTERISTICS (continued):

TC183B30: V_{OUT} = 2V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		2.295	3.0	3.075	V
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 3V		0.8	0.9	V
V_{hold}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 3 → 0V	0.7			V
η	Efficiency		70	80		%
I_{IN1}	Supply Current 1	At V_{IN} Pin, No Load		4	8	µA
I_{IN2}	Supply Current 2	At V_{IN} Pin, V_{IN} = 3.5V		2	5	µA
ILx	Lx Switching Current	VLx = 0.4V	60			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 3.5V			0.5	µA
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} – 0.4V	– 1.5			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	1.5			mA
V_{CEH1}	$\overline{CE}$ Input Voltage "H"1	$V_{OUT} \geq$ 1.5V	VOUT - 0.4			V
VCEL1	$\overline{CE}$ Input Voltage "L"1	$V_{OUT} \geq$ 1.5V			0.4	V
V_{CEH2}	$\overline{CE}$ Input Voltage "H"2	0.8V ≤ V_{OUT} ≤ 1.5V	VOUT - 0.1			V
V_{CEL2}	$\overline{CE}$ Input Voltage "L"2	0.8V ≤ V_{OUT} ≤ 1.5V			0.1	V
I_{CEH}	$\overline{CE}$ Input Current "H"	$\overline{CE}$ = 3V	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ Input Current "L"	$\overline{CE}$ = 3V	– 0.5		0.5	µA
f_{osc}	Oscillator Frequency		80	100	120	kHz
Maxdty	Oscillator Duty Cycle	on (V_{LX} "Low")	65	75	85	%
V_{LXlim}	VLx Pin Voltage Limit[1]	Lx Switch on	0.65	0.8	1.0	V

NOTICE

Observe the following precautions when using this IC:

- Place external components as close as possible to the IC to reduce wiring. In particular, wire the capacitor connected to the V_{OUT} pin using the shortest route possible.

- Ensure sufficient grounding. The V_{SS} pin receives a large current due to switching. High impedance in the V_{SS} routing causes the internal potential of the IC to fluctuate with the switching current, resulting in unstable operation.

- Use capacitors with good high frequency response, such as tantalum capacitors or electrolytic aluminum and ceramic capacitors. The capacitance must be 10µF or more. It is recommended that the capacitors be able to withstand at least three times the specified output voltage, because the coil may cause a high spikelike voltage when the Lx transistor is turned off.

- Select a coil with a low resistance, adequate current carrying capacity and resistance to magnetic saturation. The ILx may exceed its absolute maximum rated value during a maximum load when the coil inductance value is too low. Be sure to select the proper inductance value.

- Use Schottky diodes with fast switching speed. Ensure that they have adequate current-carrying capacity.

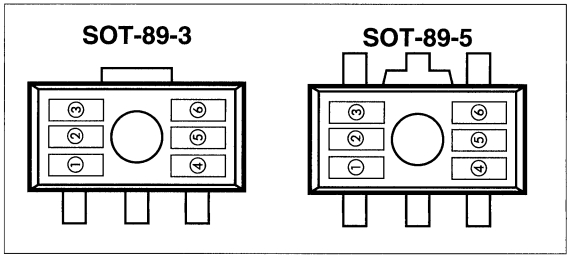
ELECTRICAL CHARACTERISTICS (continued):

TC183B50: V_{OUT} = 5V, V_{IN} = 3V, V_{SS} = 0V, I_{OUT} = 10mA, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage		4.875	5.000	5.125	V
V_{IN}	Input Voltage				8	V
V_{ST}	Starting Voltage	I_{OUT} = 1mA, V_{IN}: 0 → 3V		0.8	0.9	V
V_{hold}	Holding Voltage	I_{OUT} = 1mA, V_{IN}: 3 → 0V	0.7			V
η	Efficiency		70	85		%
I_{IN1}	Supply Current 1	At V_{IN} Pin, No Load		6	12	µA
I_{IN2}	Supply Current 2	At V_{IN} Pin, V_{IN} = 5.5V		2	5	µA
ILx	Lx Switching Current	VLx = 0.4V	80			mA
ILxL	Leakage Current of Lx pin	VLx = 6V, V_{IN} = 5.5V			0.5	µA
$I_{EXT}H$	EXT "H" Output Current	V_{EXT} = V_{OUT} – 0.4V	– 2.0			mA
$I_{EXT}L$	EXT "L" Output Current	V_{EXT} = 0.4V	2.0			mA
V_{CEH1}	$\overline{CE}$ Input Voltage "H"1	$V_{OUT} \geq$ 1.5V	VOUT - 0.4			V
V_{CEL1}	$\overline{CE}$ Input Voltage "L"1	$V_{OUT} \geq$ 1.5V			0.4	V
V_{CEH2}	$\overline{CE}$ Input Voltage "H"2	0.8V ≤ V_{OUT} < 1.5V	VOUT - 0.1			V
V_{CEL2}	$\overline{CE}$ Input Voltage "L"2	0.8V ≤ V_{OUT} < 1.5V			0.1	V
I_{CEH}	$\overline{CE}$ Input Current "H"	$\overline{CE}$ = 5V	– 0.5		0.5	µA
I_{CEL}	$\overline{CE}$ Input Current "L"	$\overline{CE}$ = 5V	– 0.5		0.5	µA
f_{osc}	Oscillator Frequency		80	100	120	kHz
Maxdty	Oscillator Duty Cycle	on (V_{LX} "Low")	65	75	85	%
V_{LXlim}	VLx Pin Voltage Limit[1]	Lx Switch on	0.65	0.8	1.0	V

Note 1: The ILx increases steadily after the Lx switch is set to ON due to use of an external coil. The accompanying VLx also increases. When the VLx reaches the V_{LXlim}, the Lx switch is set to OFF by the protective circuit.

MARKING



a and b represents first digit and decimal place of V_{OUT}. For example:

Mark a	Mark b	V_{OUT} Voltage
2	7	2.7V

c represents driver type

Mark c	Type		
1	1	TC18XX1	Internal Switch (SOT-89-3 only)
2	2	TC18XX2	External Switch (SOT-89-3 only)
3	3	TC18XX3	Int./Ext. Switch, plus $\overline{CE}$ (SOT-89-5 only)

d and e represent assembly lot number

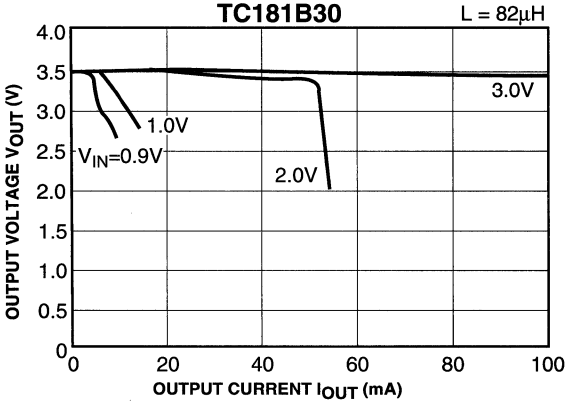
f represents oscillator frequency

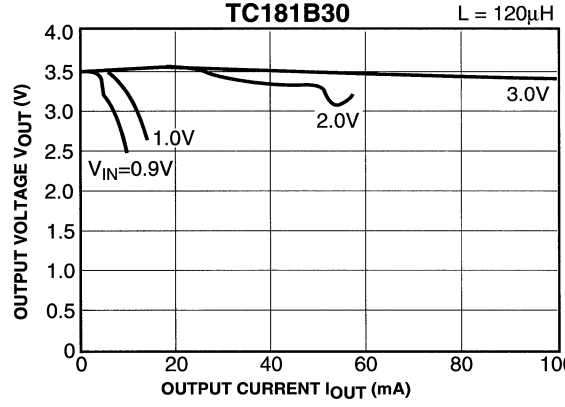
Mark f	Type	
B	B	100kHz

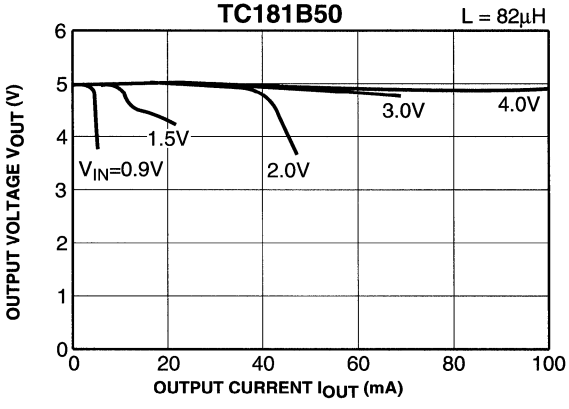
TC18 Series

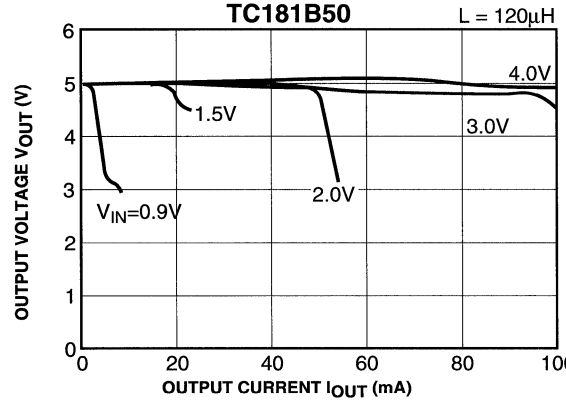
TYPICAL CHARACTERISTICS

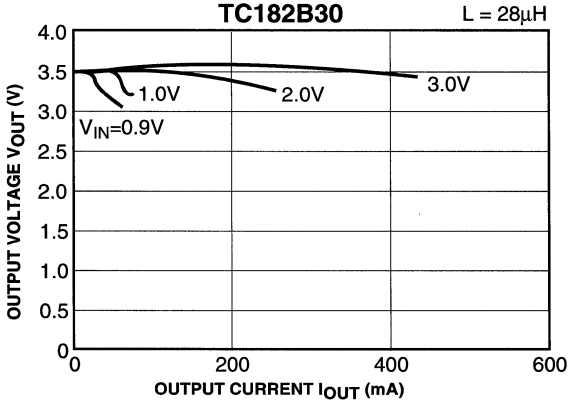
1) Output Voltage vs. Output Current (T_A = 25°C)

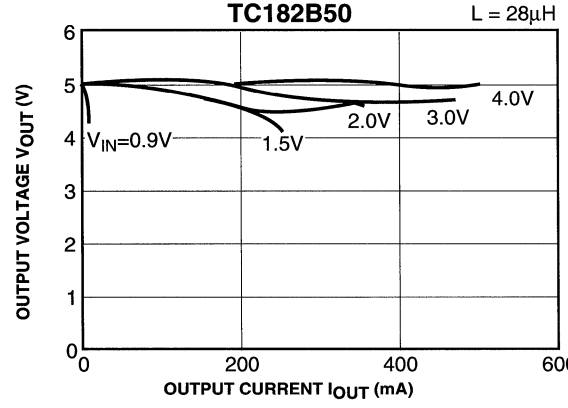






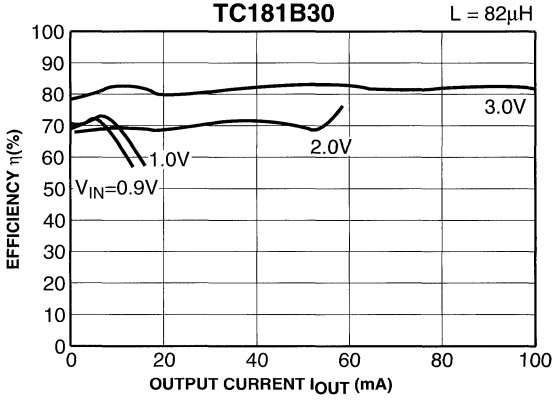


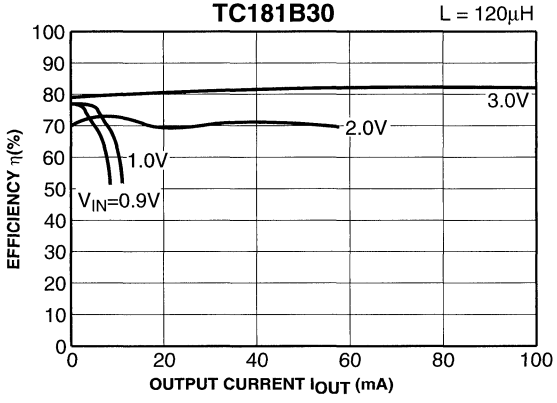


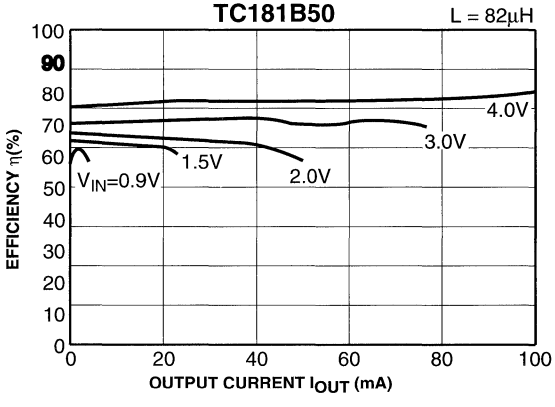


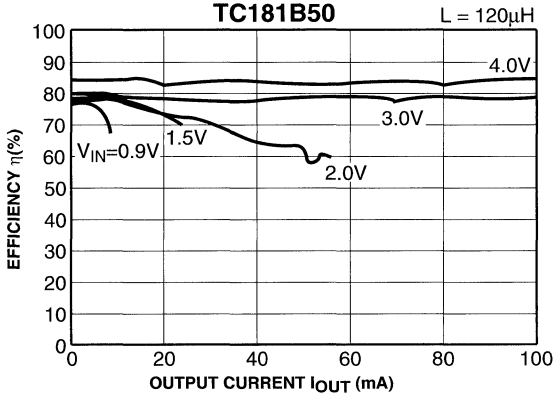
TYPICAL CHARACTERISTICS (continued):

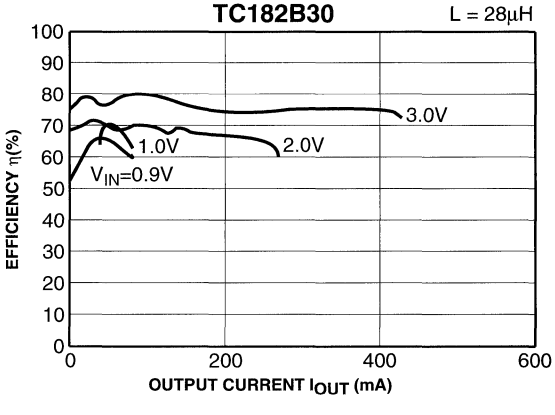
2) Efficiency vs. Output Current (T_A = 25°C)

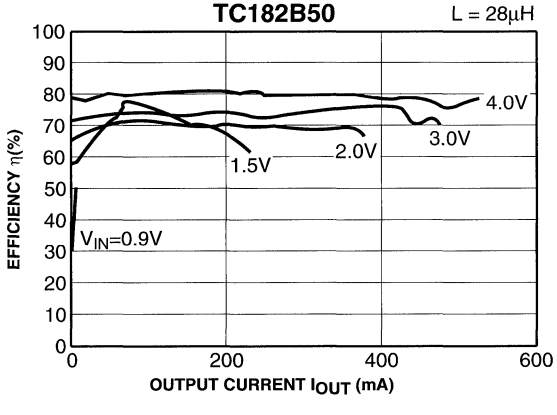








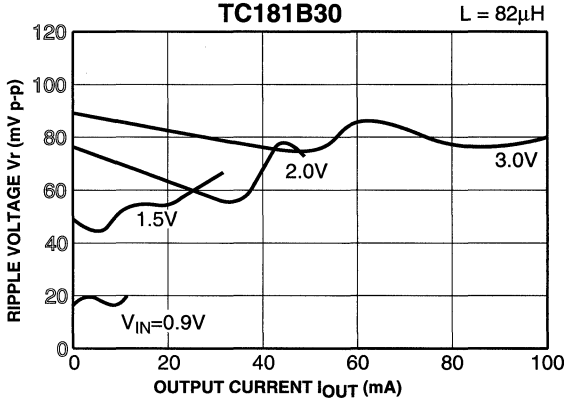


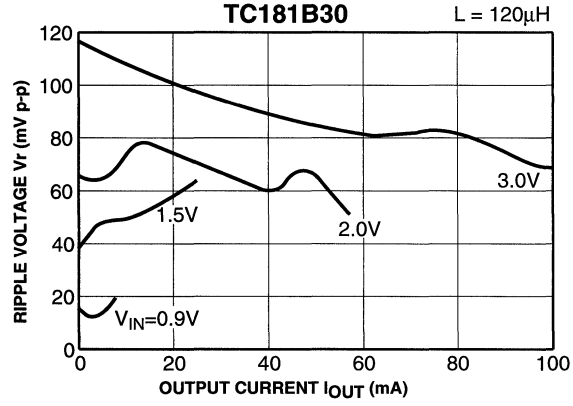


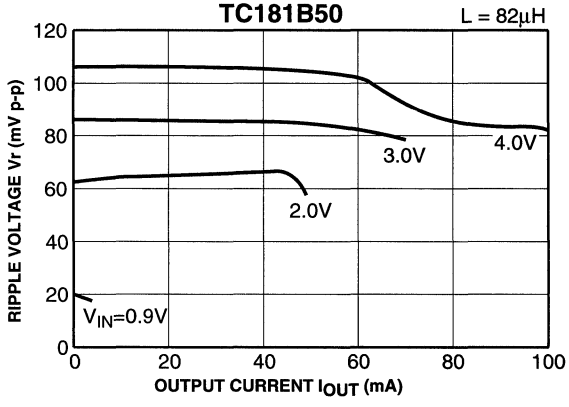
TC18 Series

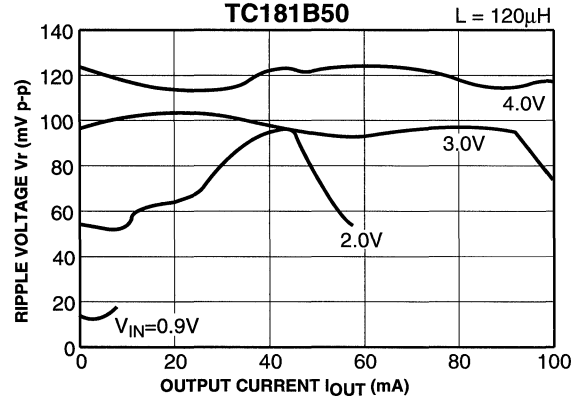
TYPICAL CHARACTERISTICS (continued):

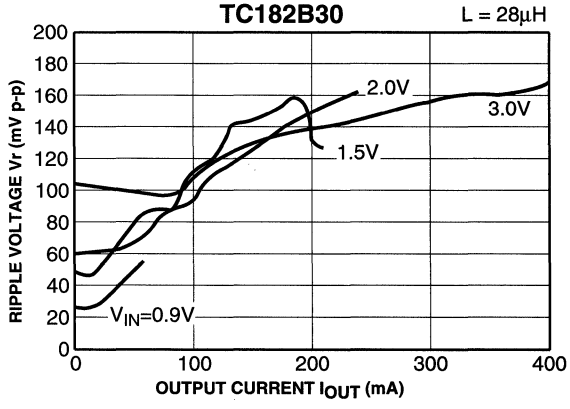
3) Output Ripple Voltage vs. Output Current (T_A = 25°C)

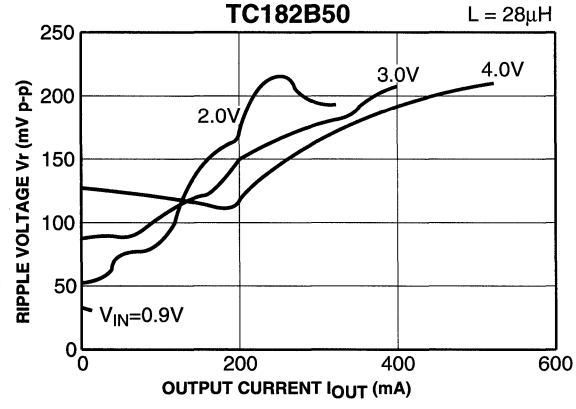






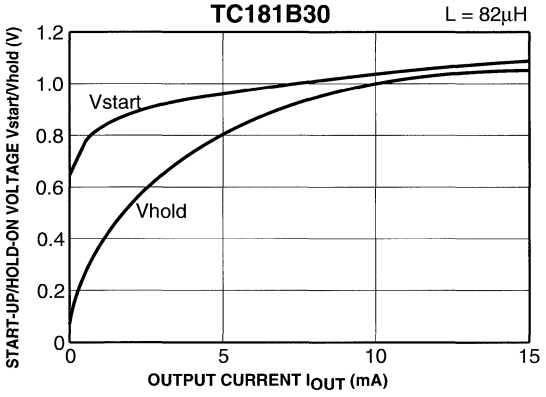


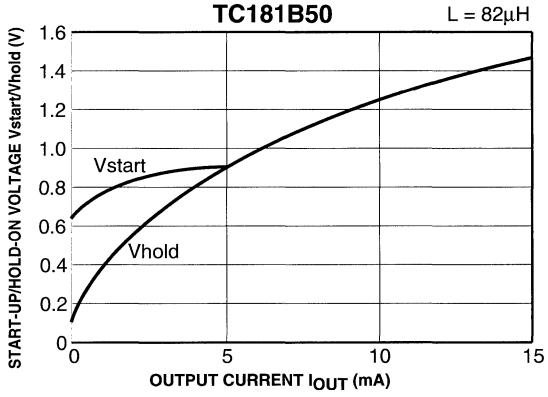




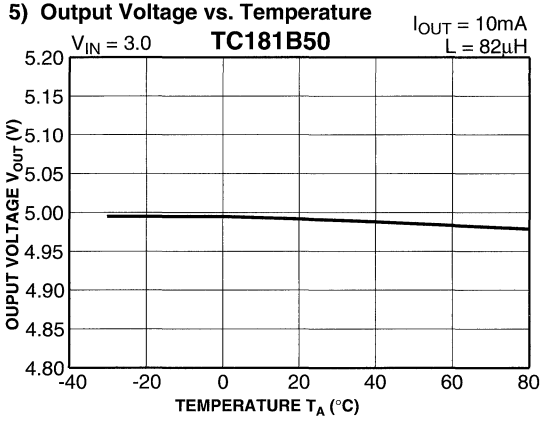
TYPICAL CHARACTERISTICS (continued):

4) Start-up/Hold-ON Voltage vs. Output Current (T_A = 25°C) Vstart: Increasing V_{IN} from 0V, Vhold: Decreasing V_{IN} from 2.0V

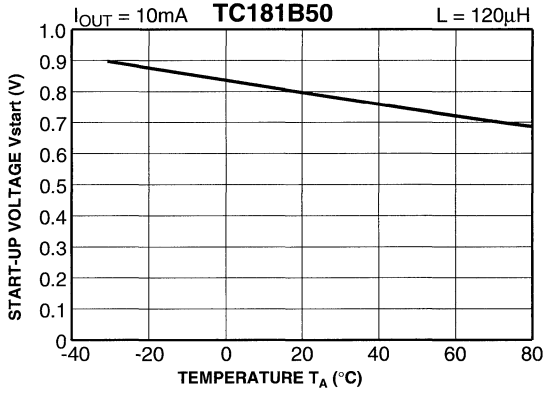




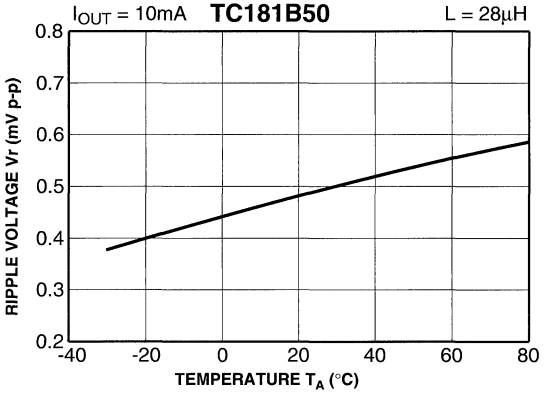
5) Output Voltage vs. Temperature



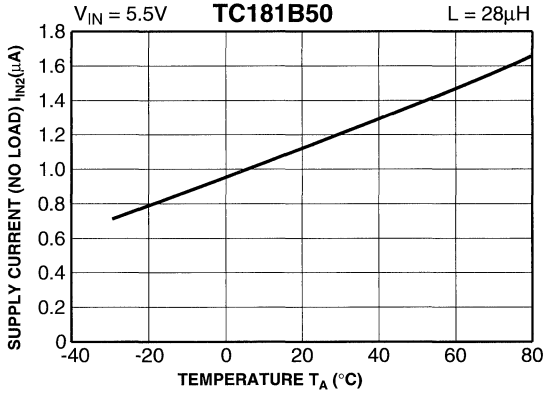
6) Start-up Voltage vs. Temperature



7) Hold-ON Voltage vs. Temperature



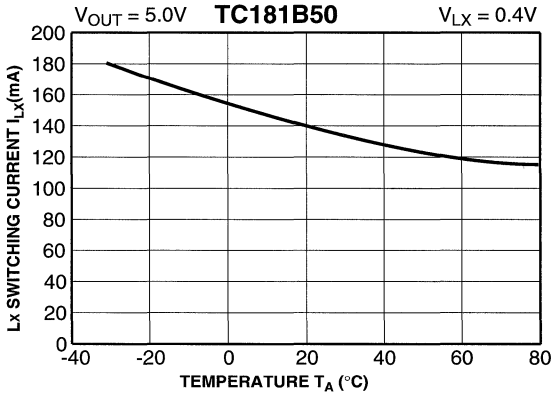
8) Supply Current (No Load) vs. Temperature



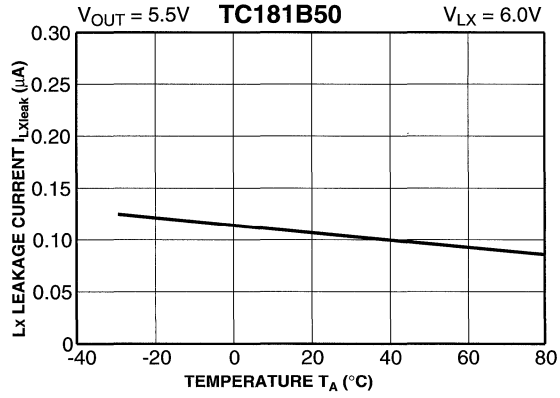
TC18 Series

TYPICAL CHARACTERISTICS (continued):

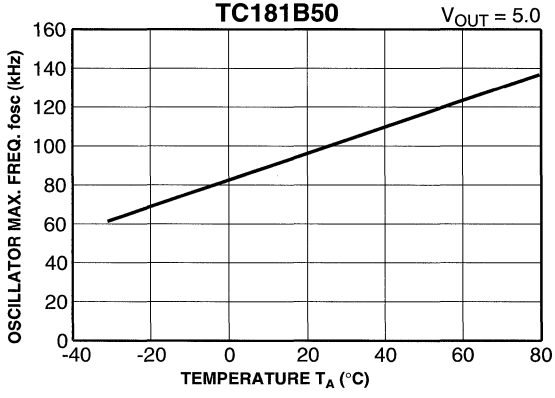
9) Switching Current vs. Temperature



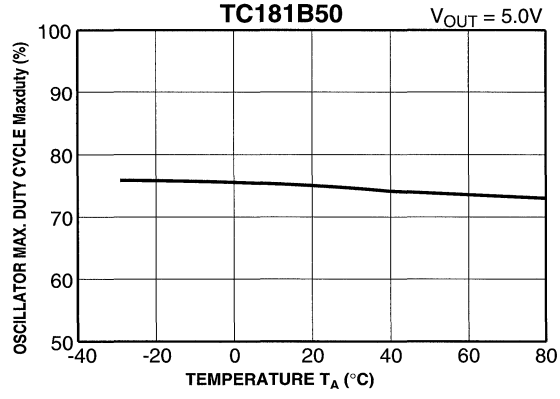
10) Lx Leakage Current vs. Temperature



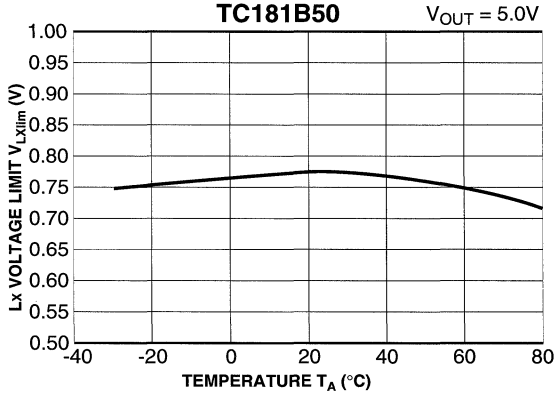
11) Oscillator Maximum Frequency vs. Temperature



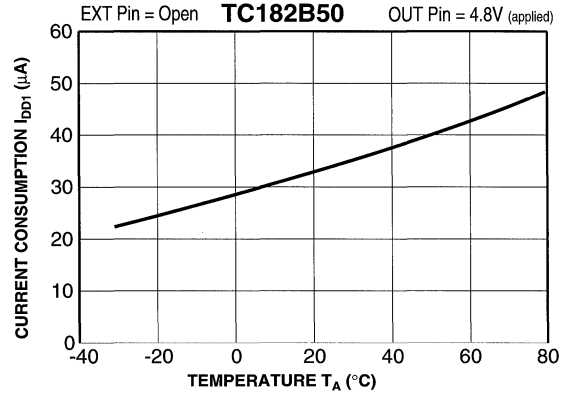
12) Oscillator Maximum Duty Cycle vs. Temperature



13) Lx Voltage Limit vs. Temperature

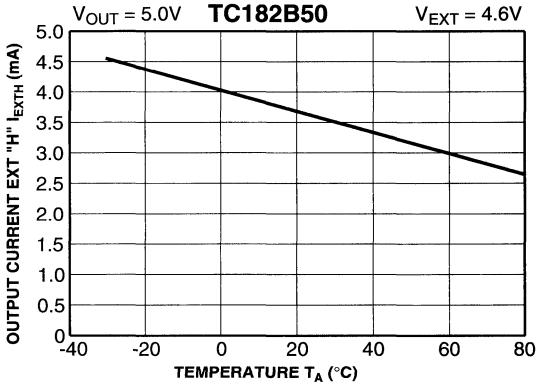


14) Consumption Current vs. Temperature

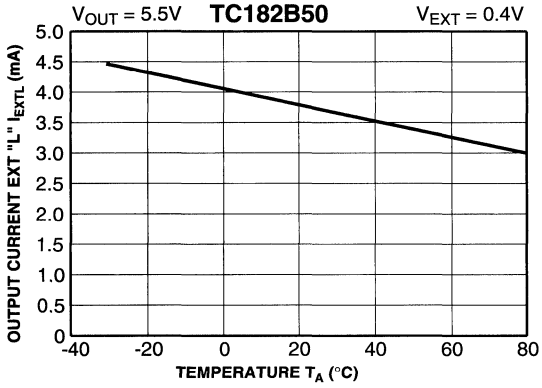


TYPICAL CHARACTERISTICS (continued):

15) EXT "High" Output Current vs. Temperature



16) EXT "Low" Output Current vs. Temperature

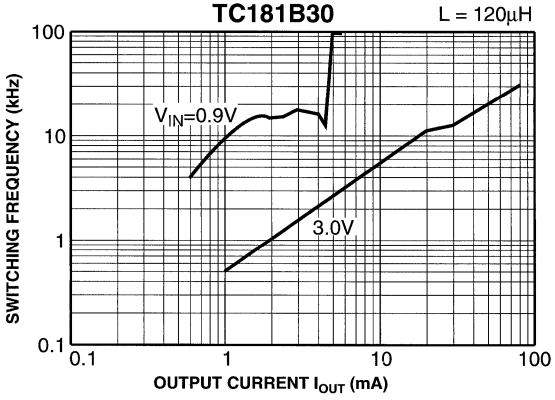


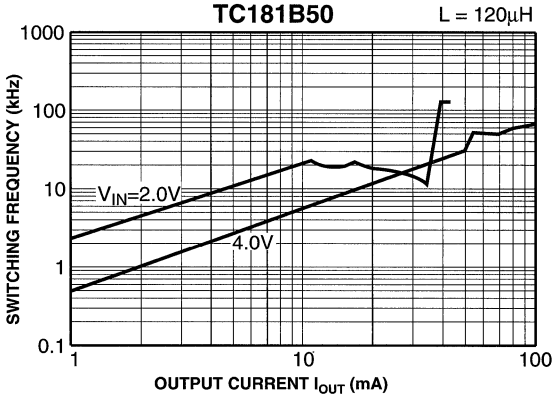
3

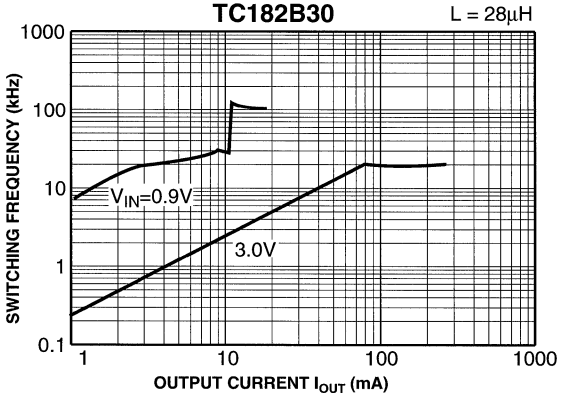
TC18 Series

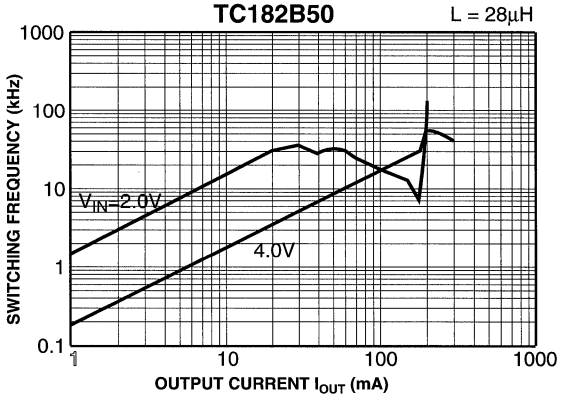
TYPICAL CHARACTERISTICS (continued):

17) Switching Frequency vs. Output Current

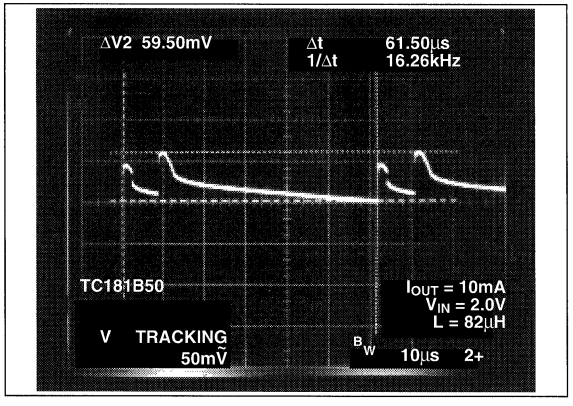








Output Voltage Ripple



BiCMOS CURRENT MODE PWM CONTROLLER

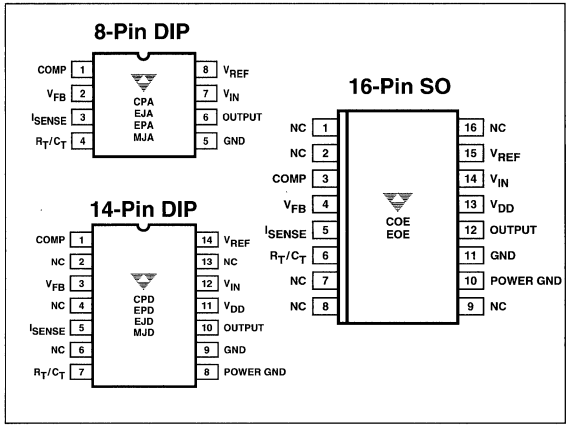
FEATURES

- **Low Power BiCMOS Design**
- **Tough CMOS™ Construction**
- **Low Supply Current ..... 1.0 mA Typ @ 100 kHz**
- **Wide Supply Voltage Operation ..... 8V to 15V**
- **Latch-Up Immunity ..... 500 mA on Outputs**
- **Input Will Withstand Negative Inputs to –5 Volts**
- **High Output Drive ..... 0.7A Peak (1.2A on 14 and 16-Pin Versions)**
- **2 kV ESD Protection**
- **Current Mode Control**
- **Fast Rise/Fall Time (Max) ..... 60 ns @ 1000 pF**
- **High Frequency Operation ..... 500 kHz**
- **Clock Ramp Reset Current ..... 2.5 mA ±10%**
- **Low Propagation Delay Current Amp to Output ..... 140 ns Typ**
- **Pin Compatible with UC3843**

ORDERING INFORMATION

Part No.	Package	Temperature
TC18C**MJA	8-pin CerDIP	–55°C to +125°C
TC18C**MJD	14-pin CerDIP	–55°C to +125°C
TC28C**EOE	16-pin SOIC Wide	–40°C to +85°C
TC28C**EPA	8-pin Plastic DIP	–40°C to +85°C
TC28C**EPD	14-pin Plastic	–40°C to +85°C
TC38C**COE	16-pin SOIC Wide	0°C to +70°C
TC38C**CPA	8-pin Plastic DIP	0°C to +70°C
TC38C**CPD	14-pin Plastic	0°C to +70°C

PIN CONFIGURATION



GENERAL DESCRIPTION

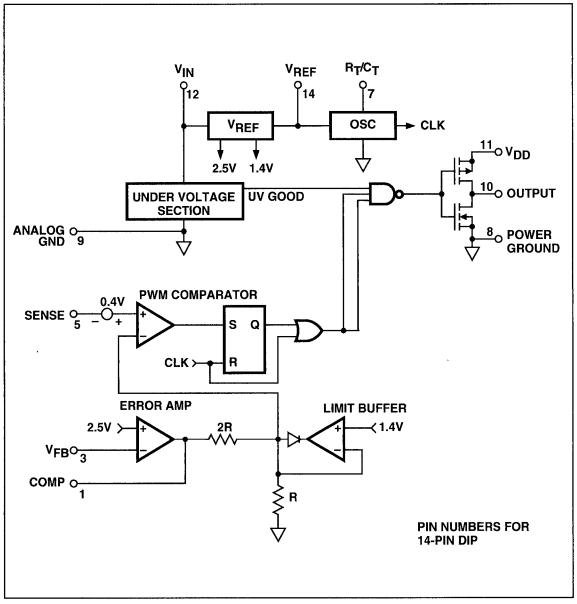
The TC38C43 is a current mode BiCMOS PWM control IC. With a low 1.0 mA supply current along with high drive current (0.7A peak) it provides a low cost solution for a PWM that operates to 500 kHz and directly drives MOSFETs up to HEX 3 size.

Performance of the oscillator and current sense amplifier have been greatly improved over previous bipolar versions. Voltage and temperature stability have been improved by a factor of 3. Noise immunity (PSRR) has also been improved.

The TC38C43 is pin compatible with the earlier bipolar version so that designers can easily update older designs. Improvements have been added, though. For example, clock ramp reset current is specified at 2.5 mA (±10%) for accurate dead time control. A few component values must be changed (R_T & C_T) to use the TC38C43 in existing bipolar designs.

The 14-pin DIP and 16-pin SO versions have separate and internally isolated grounds, and are rated for higher output current (1.2A). These separate grounds allow for 'bootstrap' operation of the PWM to further improve efficiency.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 18V
Maximum Chip Temperature ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (10 sec) ..... +300°C
Package Thermal Resistance
CerDip $R_{\theta J-A}$ ..... 150°C/W
CerDip $R_{\theta J-C}$ ..... 55°C/W
PDIP $R_{\theta J-A}$ ..... 125°C/W
PDIP $R_{\theta J-C}$ ..... 45°C/W
SOIC $R_{\theta J-A}$ ..... 250°C/W
SOIC $R_{\theta J-C}$ ..... 75°C/W
Operating Temperature
18C4X ..... $-55C° \le T_A \le +125°C$
28C4X ..... $-40C° \le T_A \le +85°C$
38C4X ..... $0C° \le T_A \le +70°C$

Electrical Characteristics: unless otherwise stated, these specifications apply over specified temperature range. $V_{IN} = V_{DD} = 15V$; $R_T = 71\ k\Omega$; $C_T = 150\ pF$

		TC18C43 / TC28C43			TC38C43			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	$T_A = 25°C$, $I_O = 1\ mA$	4.9	5	5.1	4.90	5	5.10	V
Line Regulation	$9.5V \le V_{IN} \le 15V$, $I_O = 1\ mA$	—	±3	±10	—	±3	±10	mV
Load Regulation	$1mA \le I_O \le 11\ mA$	—	±5	±15	—	±3	±10	mV
Temp Stability	(note 1)	—	±0.25	±0.5	—	±0.25	±0.5	mV/°C
Output Noise Voltage	$10\ Hz \le f \le 10\ kHz$, $T_A = 25°C$ (note 1)	—	100	—	—	100	—	µV(rms)
Long Term Stability	$T_A = 125°C$, 1000 Hrs. (note 1)	—	±0.5	—	—	±0.5	—	%
Output Short Circuit		-20	-50	-100	-30	-50	-100	mA
Oscillator Section								
Initial Accuracy	$T_A = 25°C$ (note 4)	95	100	105	95	100	105	kHz
Voltage Stability	$9.5V \le V_{IN} \le 15V$	—	±0.2	±0.3	—	±0.2	±0.3	%
Temp Stability	$T_{MIN} \le T_A \le T_{MAX}$ (note 1); Figure 2	—	±0.01	±0.05	—	±0.01	±0.03	%/°C
Clock Ramp Reset	R_T/C_T pin at 4V	2.25	2.5	2.75	2.25	2.5	2.75	mA
Amplitude	R_T/C_T pin peak to peak	2.45	2.65	2.85	2.45	2.65	2.85	V
Maximum Freq	(note 1)	1	—	—	1	—	—	MHz
Error Amp Section								
Input Offset Voltage	$V_{(COMP)} = 2.5V$	—	±15	±50	—	±15	±50	mV
Input Bias Current	(note 1)	—	±0.3	±2	—	±0.3	±2	nA
A_{VOL}	$2V \le V_O \le 4V$	70	90	—	70	90	—	dB
Gain Bandwidth Product	(note 1)	650	750	—	650	750	—	kHz
	PSR9.5V ≤ IN ≤ 15V	80	100	—	80	100	—	dB
Output Sink Current	$V_{FB} = 2.7V$, $V_{(COMP)} = 1.1V$ (note 1)	1.2	1.5	—	1.5	1.7	—	mA
Output Source Current	$V_{FB} = 2.3V$, $V_{(COMP)} = 5V$ (note 1)	3	3.4	—	3.9	4.2	—	mA
V_{OUT} High	$V_{FB} = 2.3V$, $R_L = 10k$ to ground	5.8	6	6.5	5.8	6	6.5	V
V_{OUT} Low	$V_{FB} = 2.7V$, $R_L = 10k$ to V_{REF} 0.1	0.7	1.1	0.1	0.7	1.1	V	
Rise Response	(note 1)	—	5	7	—	5	7	µs
Fall Response	(note 1)	—	3	5	—	3	5	µs
Current Sense Section								
Gain Ratio	(notes 2 & 3)	2.8	2.9	3.1	2.8	2.9	3.1	V/V
Maximum Input Signal	$V_{(COMP)} = 5V$ (note 2)	0.85	0.95	1.05	0.85	0.95	1.05	V
PSRR	$9.5V \le V_{IN} \le 15V$ (notes 1, 2 & 5)	70	80	—	70	80	—	dB
Input Bias Current	(note 1)	—	±0.3	±2	—	±0.3	±2	nA
Delay to Output	$V_{(I_{SENSE})} = 1V$ (note 1); Figure 3	—	140	160	—	140	150	ns

ELECTRICAL CHARACTERISTICS (Cont): unless otherwise stated, these specifications apply over specified temperature range. $V_{IN} = V_{DD} = 15V$; $R_T = 71\ k\Omega$; $C_T = 150\ pF$.

		TC18C4X TC28C4X			TC38C4X			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Section								
R_{DS} (ON)	$I_{SINK} = 20$ mA	—	7	15	—	7	15	Ω
R_{DS} (ON)	$I_{SOURCE} = 20$ mA	—	11	20	—	11	15	Ω
Rise Time	$C_L = 1$ nF (Note 1)	—	40	60	—	35	60	ns
Fall Time	$C_L = 1$ nF (Note 1)	—	30	60	—	30	40	ns
Cross Conduction	In coulombs (note 1)	—	6.5	—	—	6.5	—	nC
V_{DD} Ma	(Note1)	—	—	18	—	—	18	V
Undervoltage Lockout Section								
Start Threshold	X8C43	8	8.4	8.8	8	8.4	8.8	V
Undervoltage Threshold	X8C43	7.3	7.6	7.9	7.3	7.6	7.9	V
PWM Section								
Maximum Duty Cycle	X8C43 (note 1)	95	97	100	95	97	100	%
Minimum Duty Cycle				0			0	%
Supply Current								
Start Up	$T_A = 25°C$, $V_{IN} < V_{UV}$; Figure 1	50	170	300	50	170	300	µA
Operating	$V_{FB} = V(I_{SENSE}) = 0V$; Figure 4		1	2		1	1.5	mA

NOTES: 1. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.
2. Parameter measured at trip point of latch.
3. Gain ratio is defined as:

$$\frac{\Delta V_{COMP}}{\Delta V(I_{SENSE})}$$

where $0 \le V(I_{SENSE}) \le 0.8V$

4. Output frequency equals oscillator frequency for the X8C43.
5. PSRR of V_{REF}, Error Amp and PWM Comparator combination.

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PIN DESCRIPTION

8-PIN	14-PIN	16-PIN		
Pin No.	**Pin No**	**Pin No**	**Symbol**	**Description**
	2	1	NC	No Connection
	4	2	NC	No Connection
1	1	3	COMP	Compensation of the feedback loop response.
2	3	4	V_{FB}	Feedback of voltage to error amplifier to regulate voltage.
3	5	5	I_{SENSE}	For sensing pass transistor current and terminate drive when current limit threshold is reached at this pin.

PIN DESCRIPTION (CONT)...

8 -PIN	14 -PIN	16- PIN		
Pin No.	Pin No	Pin No	Symbol	Description
4	7	6	R_T/C_T	Capacitor and resistor input to set oscillator frequency of this PWM controller. The resistor is connected from V_{REF} output to R_T/C_T. The capacitor is connected from R_T/C_T to ANALOG GND.
	6	7	NC	No Connection
	13	8	NC	No Connection
		9	NC	No Connection
	8	10	POWER GROUND	Ground return of output driver.
5	9	11	ANALOG GND	For all the low level analog signal returns.
6	10	12	OUTPUT	Output to drive switching transistor gate input.
	11	13	V_{DD}	
7	12	14	V_{IN}	Voltage bias supply of all PWM Controller circuit functions.
8	14	15	V_{REF}	Reference: 5.0 volt output.
		16	NC	No Connection.

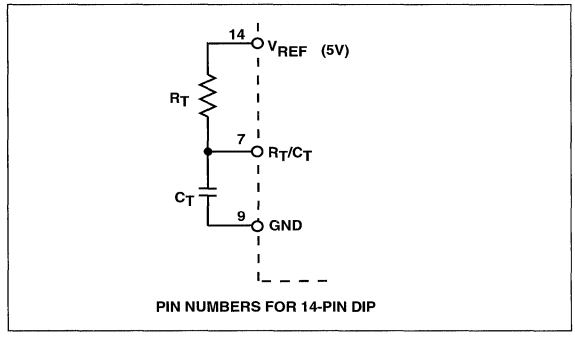
REFERENCE SECTION

The reference is a zener-based design with a buffer amplifier to drive the output. It is unstable with capacitances between 0.01 μF and 3.3 μF. In a normal application a 4.7 μF is used. In some lower noise layouts the capacitor can be eliminated entirely.

The reference is active as soon as the 38C4X has power supplied. This is different than its bipolar counterparts, in that the bipolar reference comes on only after the IC has come out of its under voltage mode. Thus, on the 38C4X, the reference pin can not be used as a reset function such as on a soft start circuit.

OSCILLATOR SECTION

The oscillator frequency is set by the combination of a resistor from the reference to the R_T/C_T pin and by a capacitor from this pin to ground. The oscillator is designed to have ramp amplitude from 0.15 to 2.5 volts. This is approximate, as over shoot on the oscillator comparator causes the ramp amplitude to increase with frequency due to comparator delay. Minimum values for C_T and R_T are 33 pF and 1 kΩ respectively. Maximum values are dependent on leakage currents in the capacitor, not on the input currents to the R_T/C_T pin.



PIN NUMBERS FOR 14-PIN DIP

FREQUENCY OF OPERATION

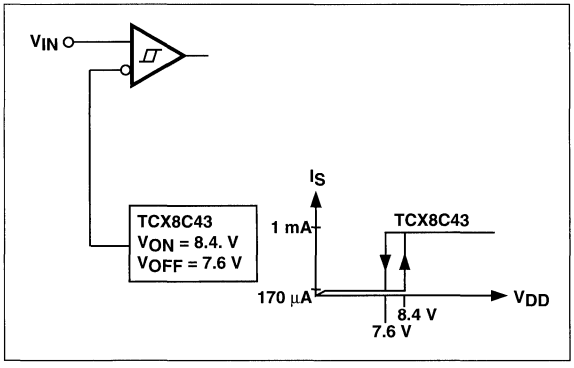
The frequency of oscillation for the TC38C43 is controlled by a resistor to V_{REF} (R_T) and a capacitor to ground (C_T). V_{REF} supplies current through the resistor and charges the capacitor until its voltage reaches the threshold of the upper comparator (≈2.5V). A 2.5 mA current is then applied to the capacitor to discharge it to near ground (≈0.15V). The discharge current is then shut off and the cycle repeats. An approximate equation for the frequency of operation is:

$$f_O \approx \frac{1}{R_T C_T} \quad (R_T \text{ in Ohms and } C_T \text{ in Farads})$$

The value of R_T affects the discharge current and the upper and lower comparators each have delays. As R_T gets smaller and as the frequency of operation gets higher, the above equation is no longer valid.

Dead Time

The value of R_T has an effect on the discharge rate but the primary consideration is the value of C_T. The time required to discharge the capacitor is approximately 1000 C_T.

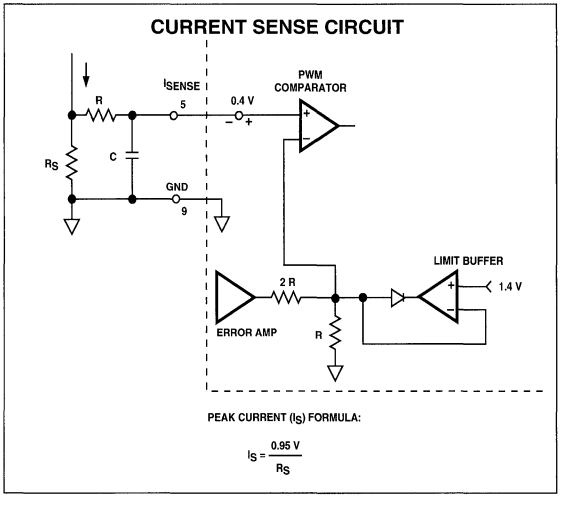


Undervoltage Lockout Range

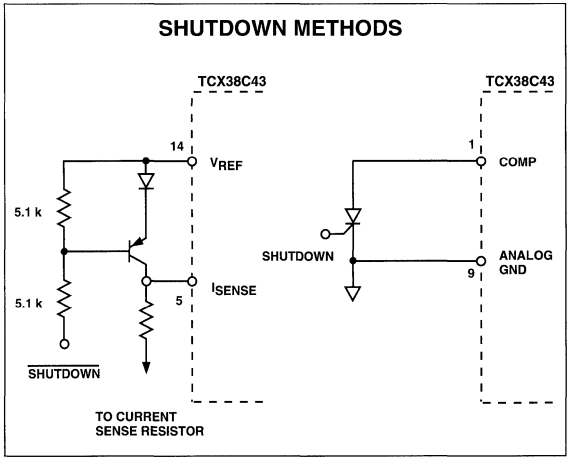
The TCx8C43 PWM Controller is used where wide ranges of input voltage is not required. The range from starting V_{in} voltage threshold to under voltage threshold is approximately 9.5% of the starting voltage. The typical start-up voltage is 8.4 V and dropout voltage is 7.6 V. This range is used most in DC-to-DC converter applications.

Duty Cycle Limit

The TCx8C43 PWM Controller has a duty cycle limit maximum of 99%. The oscillator is running at the same frequency as the output.



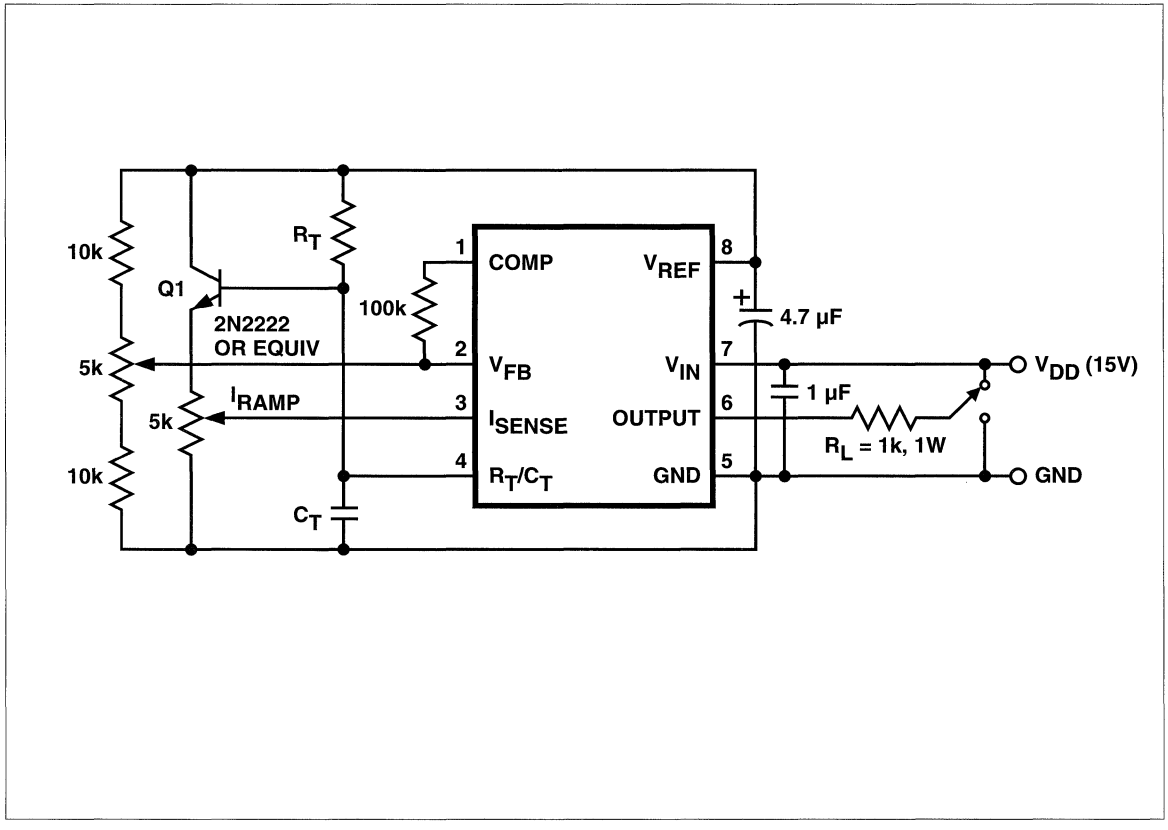
Current is sensed through voltage drop across resistor RS. A small RC filter may be required to suppress switching transient. This voltage enters PWM Controller at I_{SENSE}, pin 5. A voltage of 0.4 V is added before this is fed into PWM Comparator (+) input. The PWM Comparator (–) input senses the voltage feedback error amp output with a limit buffer that limits this voltage to 1.4 V maximum. This limit buffer limits the peak current across RS to a maximum of 0.95 V. In normal operation, the error amplifier controls the current limit threshold.



Shutdown can be accomplished by either pulling I_{SENSE} above 1 volt or pulling COMP, pin 1 to GND. This will set the PWM latch so that the output will remain low until the next clock pulse after the shutdown condition is removed.

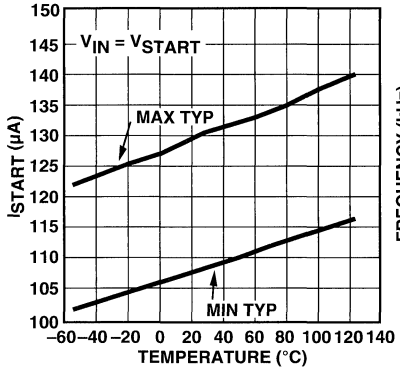
BENCH TEST OPERATIONAL SIMULATION

The timing ramp (R_T/C_T) is buffered by the emitter follpwer and fed back to the I_{SENSE} input. This ramp simulates the dI/dT current ramp which would flow through the primary of the transformer. The output voltage of the power supply is simulated by feeding some of the reference voltage into V_{FB}. The combination of the two levels determined the operating characteristics of the current mode controller.

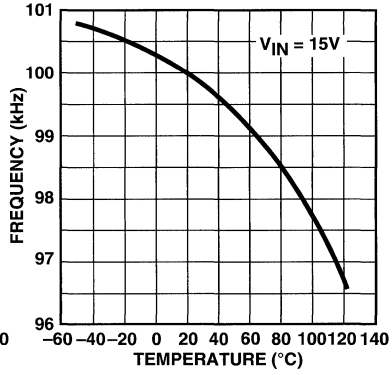


TYPICAL CHARACTERISTICS

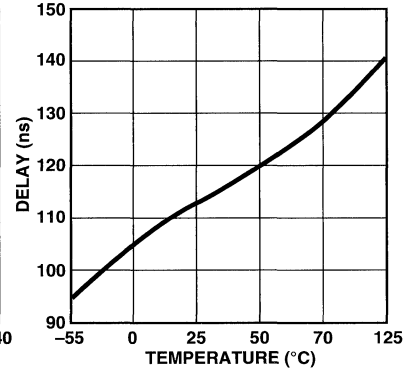
Start Current vs. Temperature



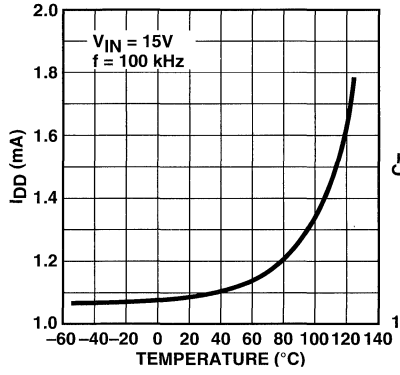
Oscillator Frequency Changes vs. Temperature



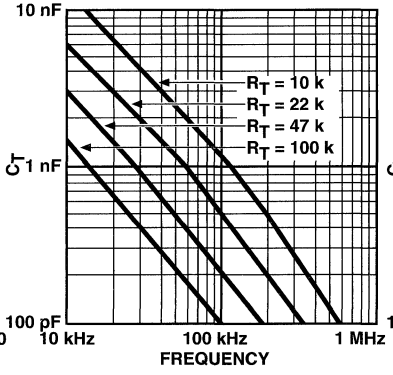
I_{SENSE} to Out Delay



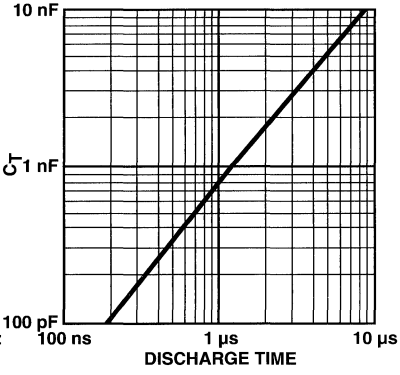
I_{DD} vs. Temperature

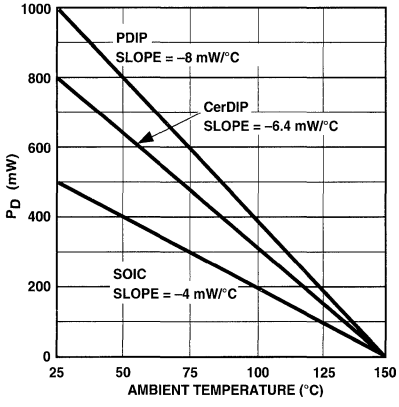


Frequency of Operation



Dead Time vs. C_T





CMOS CURRENT MODE PWM CONTROLLER

FEATURES

- Isolated Output Drive
- Low Power CMOS Construction
- Low Supply Current ..... 2 mA Typ
- Wide Supply Voltage Operation ..... 8V to 18V
- Latch-Up Immunity ..... 500 mA on Outputs
- Above and Below Rail Input Protection 6V
- High Output Drive ..... 500 mA Peak
- Current Mode Control
- Fast Rise/Fall Time ..... 50 ns @ 1000 pF
- High Frequency Operation ..... 500 kHz
- UV Hysteresis Guaranteed
- Programmable Current Limit
- Shutdown Pin Available
- Double Ended
- Soft Start
- Low Prop Delay Current Amp to Output ..... < 350 ns Typ
- Low Prop Delay Shutdown to Output ..... < 400 ns Typ
- TC38C46Pin Compatible with Unitrode UC3846
- ESD Protected ..... ±2 kV

GENERAL DESCRIPTION

The TC38C46 is a current mode CMOS PWM control IC. It draws only 2 mA supply current, so it can be driven without a costly 50-60 Hz transformer. The output drive stage is capable of high drive currents, 300 mA typical.

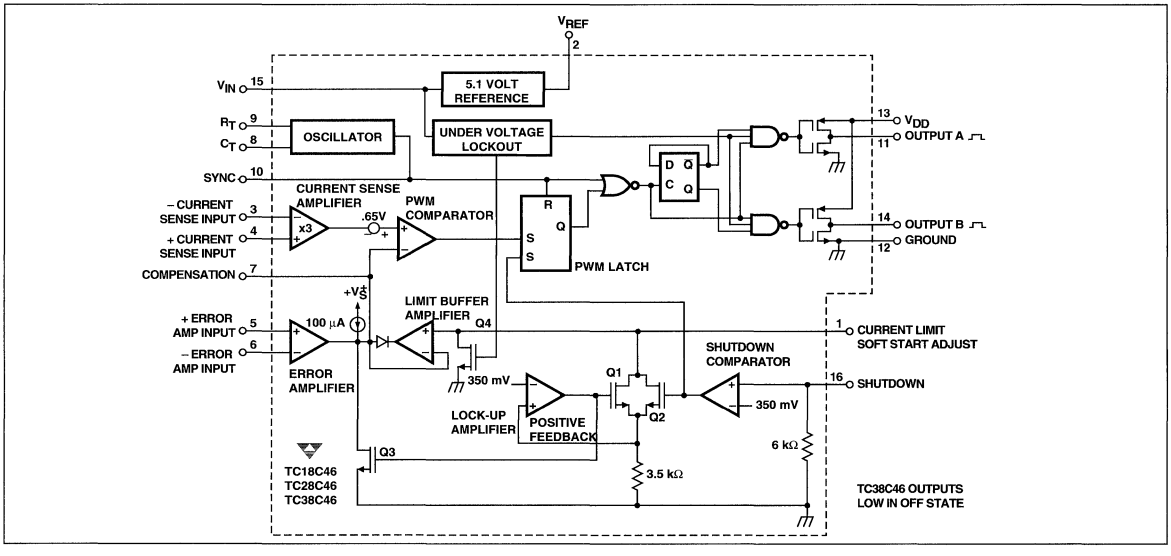
The TC38C46 is pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added.

This second generation part has been designed with an isolated drive stage. Unlike its cousin, the TC170, the output stage of the TC38C46 can be run from a separate power supply such as a secondary winding on an output transformer. This allows for bootstrap start-up of the power supply.

ORDERING INFORMATION

Part No.	Configuration	Pkg./Temperature
TC18C46MJE	Non-Inverting	16-Pin CerDIP –55 to +125°C
TC28C46EOE	Non-Inverting	16-Pin SOIC (wide) –40 to +85°C
TC28C46EPE	Non-Inverting	16-Pin Plastic DIP –40 to +85°C
TC38C46COE	Non-Inverting	16-Pin SOIC (wide) 0 to +70°C
TC38C46CPE	Non-Inverting	16-Pin Plastic DIP 0 to +70°C

FUNCTIONAL BLOCK DIAGRAM

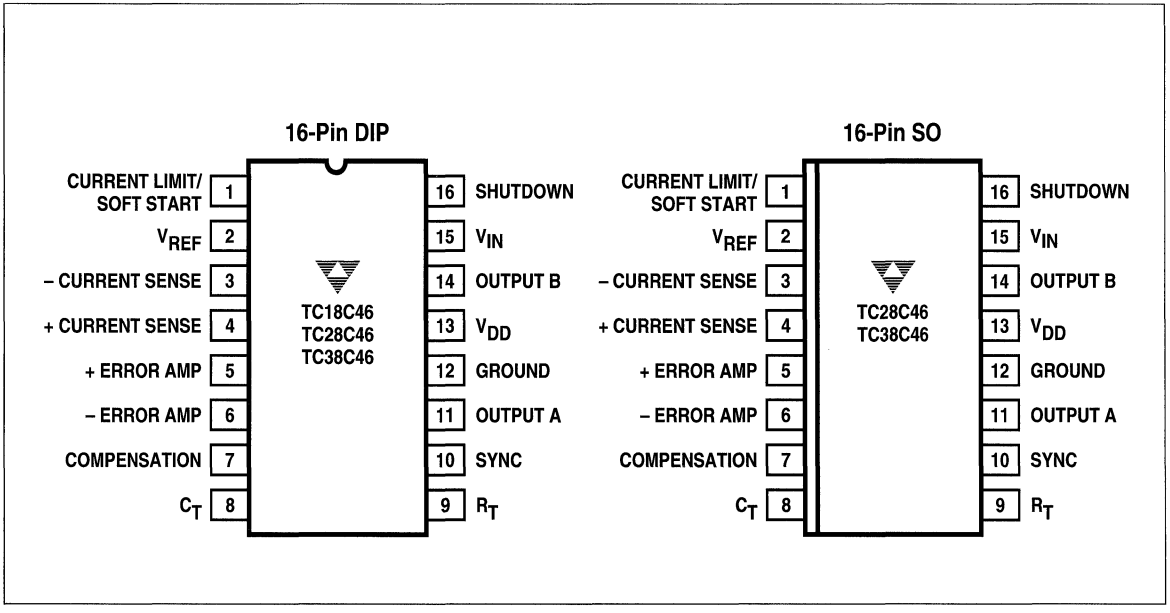


ABSOLUTE MAXIMUM RATINGS

Output Current, Source or Sink (Pins 1, 14) ..... 500 mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... –0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... –30 mA
Sync Output Current (Pin 10) ..... –5 mA
Error Amplifier Output Current (Pin 7) ..... –5 mA
Soft Start Sink Current (Pin 1) ..... 50 mA
Oscillator Charging Current (Pin 9) ..... 5 mA
Supply Voltage 18V
Maximum Chip Temperature ..... 150 °C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (10 sec) ..... 300 °C
Package Thermal Resistance
CerDIP $R_{\theta J-A}$ ..... 150°C/W
CerDIP $R_{\theta J-C}$ ..... 55°C/W
PDIP $R_{\theta J-A}$ ..... 125°C/W
PDIP $R_{\theta J-C}$ ..... 45°C/W
SOIC $R_{\theta J-A}$ ..... 250°C/W
SOIC $R_{\theta J-A}$ ..... 75°C/W

NOTES:
1.All voltages are with respect to Ground, Pin 12. Currents are positive into, negative out of the specified terminal.
2.Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for TC18C46; –40°C to +85°C for the TC28C46; and 0°C to +70°C for the TC38C46; $V_{IN} = V_{DD}$ = 16V; R_T = 30.1k; C_T = 270 pF.

		TC18C46 TC28C46			TC38C46			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	T_f = 25°C, I_O = 1 mA	5.0	5.1	5.2	5.0	5.1	5.2	V
Line Regulation	V_{IN} = 8V to 16V	—	±4	±20	—	±4	±20	mV
Load Regulation	I_O = 1mA to 10 mA	—	±4	±20	—	±4	±20	mV
Temp Coefficient	Over Operating Range, (note 1)	—	±0.2	±0.5	—	±0.2	±0.5	mV/°C
Total Output Range	Line, Load, and Temperature (note 1)	4.97	—	5.24	4.94	—	5.26	V
Long Term Drift	T_f = 125°C, 1000 Hrs (note 1)	—	±50	—	—	±50	—	mV
Short Circuit Output Current	V_{REF} = 0V	20	—	70	20	—	70	mA
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_f = 25°C (note 1)	—	22	—	—	22	—	µV(rms
Oscillator Section								
Initial Accuracy	T_f = 25°C	96.5	102	106.5	96.5	101	106.5	kHz
Voltage Coefficient	V_{IN} = 8V to 16V	—	±.1	±1.5	—	±.1	±1.5	%/V
Temp Coefficient	Over Operating Range (note 1)	—	±.04	±0.06	—	±.04	±0.06	%/°C
Clock Ramp Reset Current		1.2	2	3	1.2	2	3	mA
Osc Ramp Amplitude		3.6	3.8	4	3.6	3.8	4	V
Sync Output High Level	(note 1)	V_{DD} –0.5	—	—	V_{DD} –0.5	—	—	V
Sync Output Low Level	(note 1)	—	—	0.5	—	—	0.5	V
Sync Input High Level	Pin 8 = 0V, (note 1)	—	8.5	—	—	8.5	—	V
Sync Input Low Level	Pin 8 = 0V, (note 1)	—	8.5	5	—	8.5	5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V	—	±5	±50	—	±5	±50	nA
Error Amp Section								
Input Offset Voltage		—	±5	±25	—	±5	±25	mV
Input Bias Current		—	±10	±100	—	±0.1	±0.5	nA
Input Offset Current		—	±10	±100	—	±0.1	±0.5	nA
Open Loop Voltage Gain	ΔV_O = 1V to 6V, R_L = 100k	70	90	—	70	90	—	dB
Gain Bandwidth Product	T_f = 25°C (note 1)	0.7	1	—	0.7	1	—	MHz
CMRR	V_{CM} = 0V to 11V	70	90	—	70	90	—	dB
PSRR	V_{IN} = 8V to 16V	70	90	—	70	90	—	dB
Output Sink Current V(COMP) = 1.2V	V(EA –) = 5V, V(EA+) = 4.9V,	2	4	—	2	4	—	mA
Output Source Current V(COMP) = 2.5V	V(EA –) = 5V, V(EA+) = 5.1V,	5	10	—	5	10	—	mA
High Level Output Volt	R_L = (COMP) 5 kΩ to GND, A_{CL} = 300	4.9	5	5.1	4.9	5	5.1	V
Low Level Output Volt	R_L = (COMP) 5 kΩ to GND, A_{CL} = 300	—	0.4	0.9	—	0.4	0.9	V
Slew Rate		1.3	2	—	1.3	2	—	V/µs
Current Sense Section								
Amplifier Gain	(notes 2, 3)	2.7	3	3.4	2.7	3	3.4	V
Max Differential	(note 2) 1.1	1.5	1.8	1.1	1.5	1.8	V	

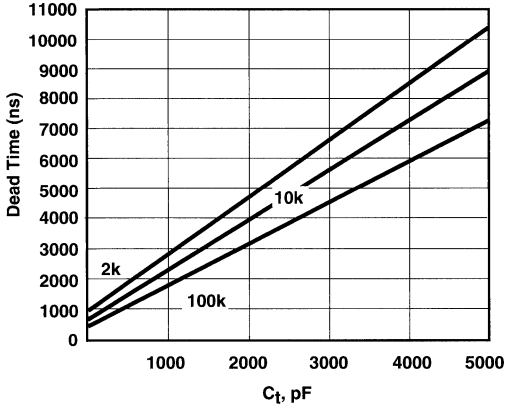
ELECTRICAL CHARACTERISTICS (Cont): unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for TC18C46; –40°C to +85°C for the TC28C46; and 0°C to +70°C for the TC38C46; $V_{IN} = V_{DD}$ = 16V; R_T = 30.1k; C_T = 270 pF.

		TC18C46 TC28C46			TC38C46			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Signal ($V_{Pin\ 4}$-$V_{Pin\ 3}$)								
Input Offset Voltage	(note 2)	0.4	0.65	0.85	0.4	0.65	0.85	V
CMRR V_{CM} = 1V to 12V,	(note 2)	40	60	—	40	60	—	dB
PSRR V_{IN} = 8V to 16V,	(note 2)	40	60	—	40	60	—	dB
Input Bias Current	(note 1)	—	±1	±100	—	±1	±100	nA
Input Offset Current	(note 1)	—	±0.1	±2	—	±0.1	±2	nA
Input Common Mode Range	(note 1)	0	—	11	0	—	11	V
Delay to Outputs T_f = 25°C,	(note 1)	150	225	400	150	225	400	ns
Current Limit Adjust Section								
Current Limit Voltage Offset		—	±1	±25	—	±1	±25	mV
Input Impedance	(Shutdown Unlatched)	3	3.5	4	3	3.5	4	kΩ
Shutdown Terminal Section								
Threshold Voltage		320	360	400	320	360	400	mV
Input Voltage Range	(note 1)	0	—	V_{IN}	0	—	V_{IN}	V
Min Latching Current ($I_{Pin\ 1}$)	(note 4) 140		—	—	140	—	—	µA
Max Non-Latching Current (I_{Pin1})	(note 5)	—	—	65	—	—	65	µA
Min Pulse Width	(note 1)	100	50	—	100	50	—	ns
Delay to Outputs	(note 1)	125	250	400	125	250	400	ns
Output Section								
Output Low Level $r_{DS\ (ON)}$	I_{SINK} = 20 mA	—	10	20	—	10	20	Ω
Output High Level $r_{DS\ (ON)}$	I_{SOURCE} = 20 mA	—	20	35	—	20	35	Ω
Output Rise Time C_L = 1 µF		—	55	90	—	55	90	ns
Output Fall Time C_L = 1 µF		—	55	90	—	55	90	ns
Undervoltage Lockout Section								
Undervoltage Threshold		6.6	7	7.3	6.6	7	7.3	V
Start Threshold		7.5	7.8	8	7.5	7.8	8	V
Threshold Hysteresis		0.6	0.8	1	0.6	0.8	1	V
Total Standby Current								
Supply Current		—	1.2	2.5	—	1.2	2	mA
Start-Up Current		—	250	350	—	250	350	µA

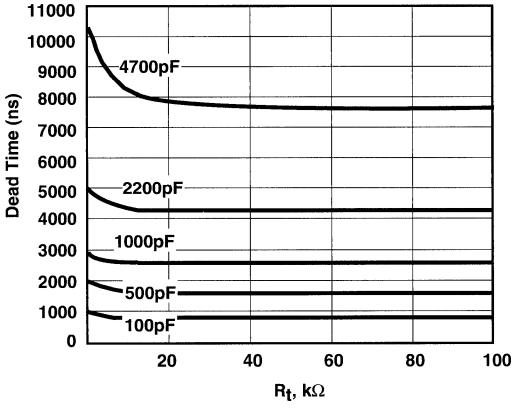
NOTES:
1. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.
2. Parameter measured at trip point of latch with $V_{Pin\ 6} = V_{REF}$, $V_{Pin\ 16}$ = 0V.
3. Amplifier gain is defined as: $G = \frac{\Delta V_{Pin\ 7}}{\Delta V_{Pin\ 4}}$; $\Delta V_{Pin\ 4}$ = 0V to 1V
4. Current into Pin 1 guaranteed to latch circuit in shutdown state.
5. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

TYPICAL CHARACTERISTIC CURVES

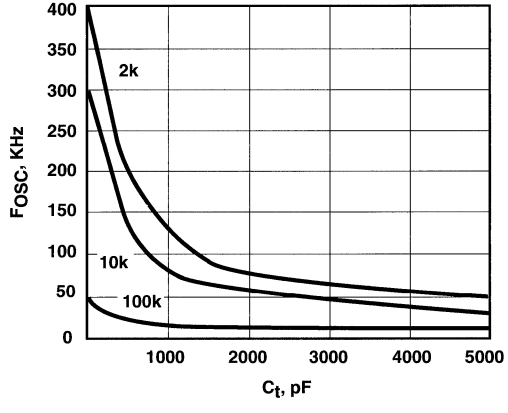
18C46 Dead Time vs. C_t



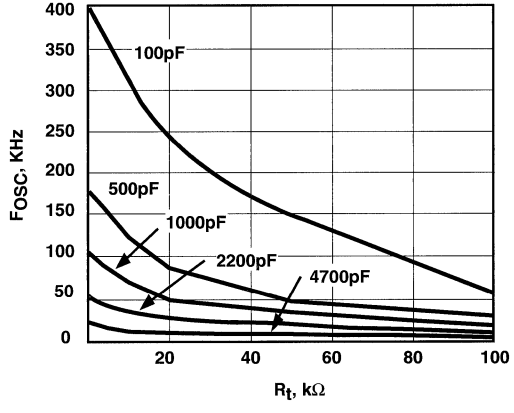
18C46 Dead Time vs. R_t



18C46 OSC Frequency vs. C_t



18C46 OSC Frequency vs. R_t



PIN DESCRIPTIONS

PIN	DESCRIPTION
1	**CURRENT LIMIT, SOFT START ADJUST** pin is for setting the peak current limit threshold of sense inputs pin 3 and pin 4. A second function of this pin is for Soft-Start programming with a capacitor between this pin and ground, pin 12.
2	V_{REF} pin is an output for the reference supply voltage of 5.1 volts. This reference can supply a minimum of 20 mA of output current.
3	**– CURRENT SENSE INPUT** pin is the current sense inverting input for sensing peak current of the pass transistor through the series current monitor resistor.
4	**+ CURRENT SENSE INPUT** pin is the non-inverting input for sensing peak current of the pass transistor. The positive end of the current sense resistor is connected here.
5	**+ ERROR AMP INPUT** pin is the non-inverting input for sensing voltage feedback from output for voltage regulation.
6	**– ERROR AMP INPUT** pin is the inverting input for sensing the reference voltage to regulate the output.
7	**COMPENSATION** pin is for compensating the feedback loop response.
8	C_T pin is the input for timing capacitor, C_T, to set oscillator frequency in conjunction with pin 9, resistor R_T, input. A second function is for setting the crossover dead time of the outputs, pins 11 and 14.
9	R_T pin is the input for the timing resistor, R_T, to set oscillator frequency by setting the (constant) current charge rate for capacitor C_T.
10	**SYNC** pin is the input or output for the oscillator synchronization pulse.
11	**OUTPUT A** pin is the output drive of phase A to drive push pull transistor A.
12	**GROUND** pin is the ground return path for all input and output signals.
13	V_{DD} pin is the supply power input terminal for the output drivers.
14	**OUTPUT B** pin is the output drive of phase B to drive push pull transistor B.
15	V_{IN} pin is voltage bias supply input for all circuits except the output drivers.
16	**SHUTDOWN** pin is an input for shutdown when a 350 mV threshold is exceeded: both output drives will then be terminated.

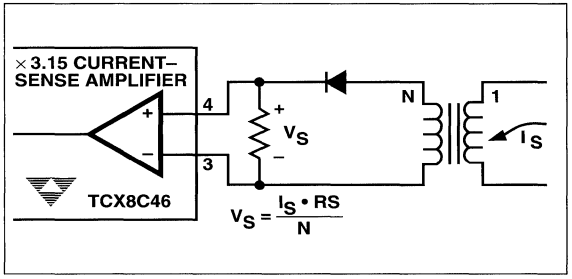


Figure 3 Transformer Isolated Current Sense

Under Voltage Lockout

The under voltage lockout circuit forces the PWM controller outputs OFF (LOW) if the supply voltage is below 7V. Threshold hysteresis is 0.8V and guarantees clean, jitter-free turn-ON and turn-OFF points. The hysteresis also reduces capacitive filtering requirements at the PWM controller supply input (pin 15).

Circuit Synchronization

Current-mode-controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage-mode controllers unequally share the load current, decreasing system reliability.

Two or more of these PWM controllers can be slaved together for parallel operation. Circuits can operate from a master PWM controller internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding pin 8. Slave controllers derive an oscillator from the bidirectional synchronization output signal at pin 10.

Pin 10 is bidirectional in that it is intended to be both a sync output and input. This is accomplished by making the output driver "weak." This is advantageous in that it eliminates an additional pin from the package but does not enable the device to directly drive another device. In order to make it an effective driver, a buffer is required (Figure 4). In order to use pin 10 as a sync input, it is necessary to overcome the internal driver. This requires a pulse with an amplitude equal to V_S. Since V_S must be above 7V for the undervoltage lockout to be disabled, a CMOS or open-collector TTL driver should be used.

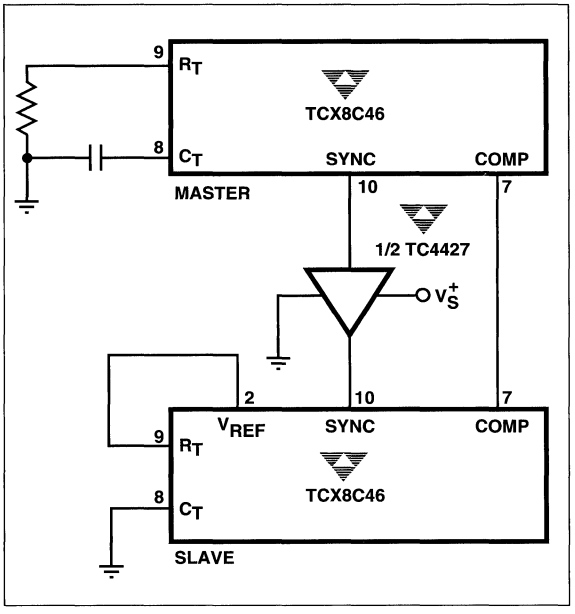


Figure 4 Master/Slave Parallel Operation

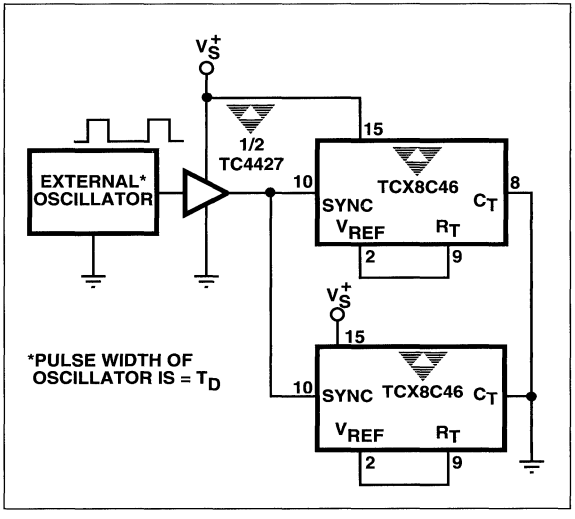


Figure 5 External Clock Synchronization

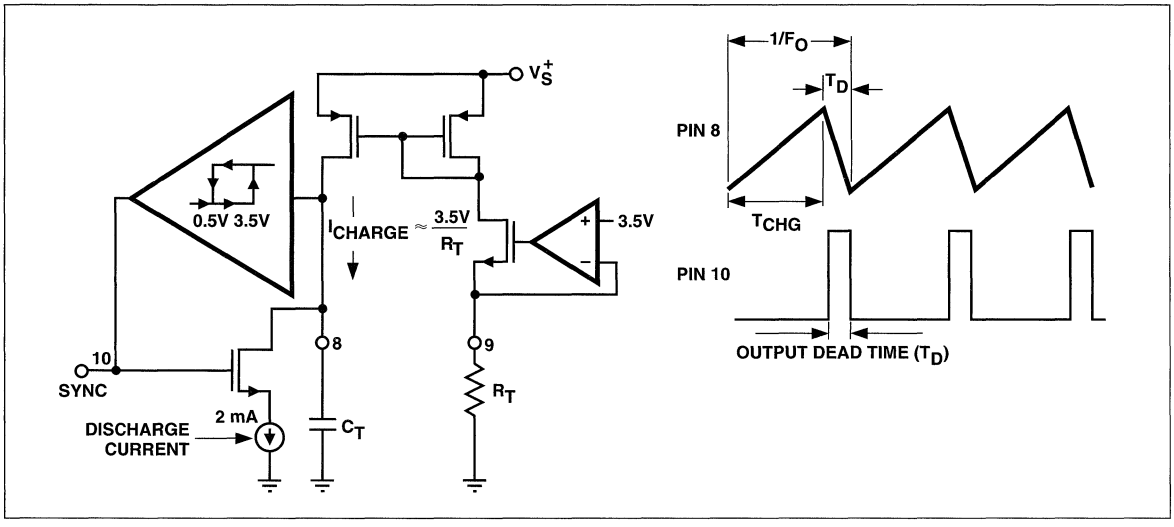


Figure 6 Oscillator Circuit

Selection of Timing Capacitor and Resistor (C_T & R_T)

1) First determine the frequency of operation F_O and the desired " dead" time", T_D (see Fig.6 graph).

   We need to choose R_T and C_T.

2) The current mirror in Fig. 6 , shows:

$$I_{CHG} = \frac{3.5\ V}{R_T} \quad . \quad \text{Also,}$$

$$I_{CHG} = C_T \frac{\triangle V}{\triangle T} \quad \text{Where,} \quad \triangle V = 3.5 - 0.5 = 3.0 \text{ Volts}$$

and $\triangle T = T_{CHG}$

3) During discharge (T_D), the discharge current pulls 2 m A out of C_T, minus the I_{CHG} that keeps trying to charge it:

$$2\text{ m A} - I_{CHG} = C_T \frac{\triangle V}{\triangle T} \text{ ,where } \triangle V = 3.0 \text{ Volts}, \quad \triangle T = T_D$$

Substituting and rearranging,

$$C_T = \frac{T_D}{3} \frac{(.002 - 3.5)}{R_T}$$

Knowing T_D choosing R_T permits calculation of C_T .

Peak Current Limit Setup

Resistors R1 and R2 at the current limit input (pin 1) set the peak current limit (Figure 1). The potential at pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for $(V_{REF} - 0.35)/R1 < 65\ \mu A$ and is latched for currents greater than 140 μA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.

I_{PCL}, the peak current limit, is the current that causes the PWM comparator noninverting input to exceed V1, the potential at the inverting input. Once the comparator trip point is exceeded, both outputs are disabled.

I_{PCL} is easily calculated:

$$I_{PCL} = \frac{V1 - 0.65V}{3\ (RS)}$$

where:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

V_{REF} = Internal voltage reference = 5.1V

3 = Gain of current-sense amplifier

0.65V = Current limit offset

Both driver outputs (pins 11 and 14) are OFF (LOW) when the peak current limit is exceeded. When the sensed current goes below I_{PCL}, the circuit operates normally.

Output Shutdown

The outputs can be turned OFF quickly through the shutdown input (pin 16). A signal greater than 360 mV at pin 16 forces the shutdown comparator output HIGH. The PWM latch is held set, disabling the outputs.

Q2 is also turned ON. If $V_{REF}/R1$ is greater than 140 μA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.65V. Q3 remains ON even after the shutdown input signal is removed. This is because the lock-up amplifier is in latched mode driving Q3 ON. This state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at pin 1 is below 0.65V.

The shutdown terminal gives a fast, direct way to disable the PWM controller output transistors. System protection and remote shutdown applications are possible.

The input pulse to pin 16 should be at least 100 ns wide and have an amplitude of at least 1V in order to get the minimum propagation delay from input to output. If these parameters are met, the delay should be less than 400 ns at 25°C; however, the delay time will increase as the device temperature rises.

Soft Restart From Shutdown

A soft restart can be programmed if nonlatched shutdown operation is used.

A capacitor at pin 1 will cause a gradual increase in potential toward V1. When the voltage at pin 1 reaches 0.75V, the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Even if a soft start is not required, it is necessary to insert a capacitor between pin 1 and ground if the current I_L is greater than 140 μA. This capacitor will prevent "noise triggering" of the latch, yet minimize the soft-start effect.

Soft-Start Power-Up

During power-up, a capacitor at R1, R2 initiates a soft-start cycle. As the input voltage (pin 15) exceeds the undervoltage lockout potential (7V), Q4 is turned OFF, ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.65V, both outputs are disabled.

When the undervoltage lockout start threshold is exceeded, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current-Sense Amplifier

The current-sense amplifier operates at a fixed gain of 3. Maximum differential input voltage (V_{PIN4}–V_{PIN3}) is 1.1V. Common-mode input voltage range is 0V to V_{IN} – 3V.

Resistive-sensing methods are shown in Figure 2. In Figure 2(A), a simple RC filter limits transient voltage spikes at pin 4, caused by external output transistor-collector capacitance. Transformer coupling (Figure 3) offers isolation and better power efficiency, but cost and complexity increase.

In order to minimize the propagation delay from the input to the current amplifier to the output terminals, the current ramp should be in the order of 1 μs in width (min). Typical time delay values are in the 225 ns region at 25°C. The delay time increases with device temperature so that at 50°C, the delay times may be increased by as much as 100 ns.

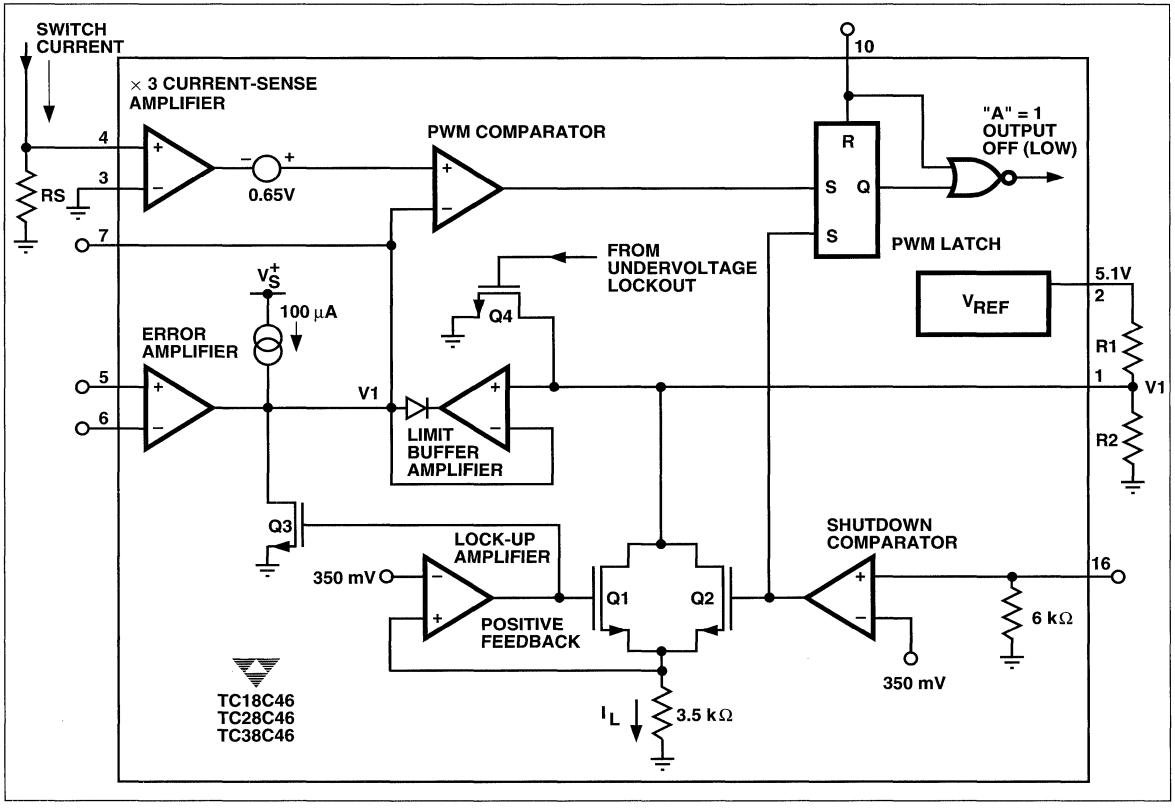


Figure 1 R1 and R2 Set Maximum Peak Output Current

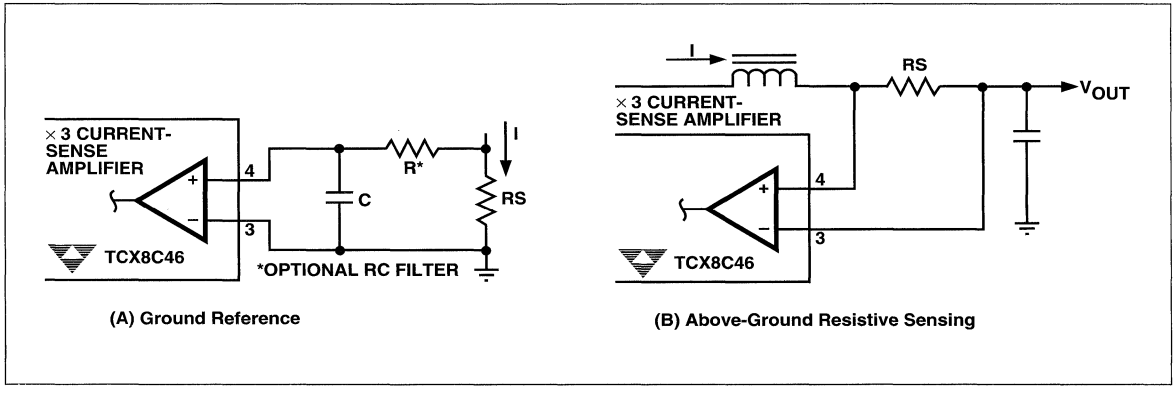


Figure 2 Resistive Sensing

CMOS CURRENT-MODE PWM CONTROLLER

FEATURES

- **Low Supply Current With CMOS Technology ..... 3.8 mA Max**
- **Internal Reference 5.1V**
- **Fast Rise/Fall Times (C_L = 1000 pF) ..... 50 ns**
- **Dual Push-Pull Outputs**
- **Direct-Power MOSFET Drive**
- **High Totem-Pole Output Drive ..... 300 mA**
- **Differential Current-Sense Amplifier**
- **Programmable Current Limit**
- **Soft-Start Operation**
- **Double-Pulse Suppression**
- **Undervoltage Lockout**
- **Wide Supply Voltage Operation ..... 8V to 16V**
- **High Frequency Operation ..... 200 kHz**
- **Available with Low OFF State Outputs**
- **Low Power, Pin-Compatible Replacement for UC3846**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC170CPE	16-Pin Plastic DIP	0°C to +70°C
TC170COE	16-Pin SO	0°C to +70°C

GENERAL DESCRIPTION

The TC170 brings low-power CMOS technology to the current-mode-switching power supply controller market. Maximum supply current is 3.8 mA. Bipolar current-mode control integrated circuits require five times more operating current.

The dual totem-pole CMOS outputs drive power MOSFETs or bipolar transistors. The 50-ns typical output rise and fall times (1000-pF capacitive loads) minimize MOSFET power dissipation. Output peak current is 300 mA.

The TC170 contains a full array of system-protection circuits (see features).

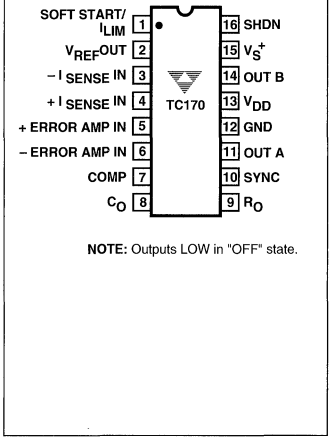
Current-mode control lets users parallel power supply modules. Two or more TC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TC170 internal oscillator or an external system oscillator.

The TC170 operates from an 8V to 16V power supply. An internal 2%, 5.1V reference minimizes external component count. The TC170 is pin compatible with the Unitrode UC1846/2846/3846 bipolar controller.

Other advantages inherent in current-mode control include superior line and load regulation and automatic symmetry correction in push-pull converters.

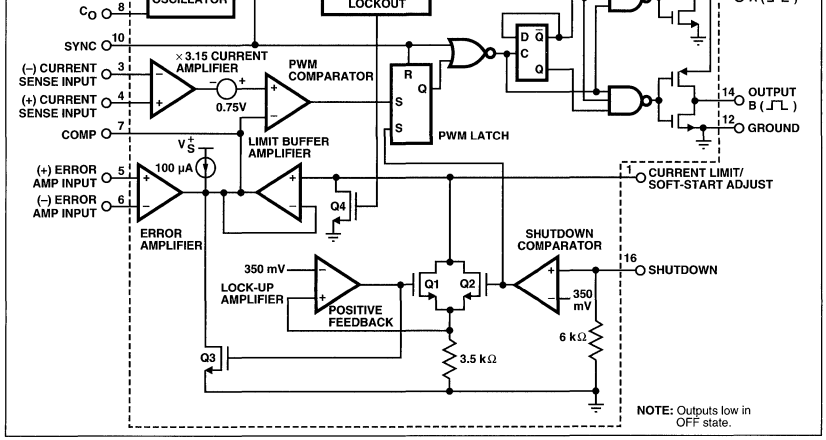
3

PIN CONFIGURATION



NOTE: Outputs LOW in "OFF" state.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: V_{IN} = 16V, R_O = 24 kΩ, C_O = 1 nF, T_A = 25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Reference Voltage						
V_{REF}	Output Voltage	I_{OUT} = 1 mA	5	5.1	5.3	V
	Line Regulation	V_{IN} = 8V to 16V		5	15	mV
	Load Regulation	I_{OUT} = 1 mA to 10 mA		13	20	mV
V_{RTC}	Temperature Coefficient	Over Operating Temperature Range		0.4	0.5	mV/°C
Oscillator						
	Oscillator Frequency		35	42	46	kHz
	Voltage Stability	V_{IN} = 8V to 16V		1.1	1.5	%/V
	Temperature Stability	Over Operating Temperature Range		5	10	%
Error Amplifier						
V_{OS}	Input Offset Voltage				±30	mV
I_B	Input Bias Current				±1	nA
V_{CMRR}	Common-Mode Input Voltage	V_{IN} = 8V to 16V	0		V_{DD} – 2V	V
A_{VOL}	Open-Loop Voltage Gain	V_{OUT} =1V to 6V	70			dB
BW	Unity Gain Bandwidth			1.2		MHz
CMRR	Common-Mode Rejection Ratio	V_{CMV} 0V to 14V	60			dB
PSRR	Power Supply Rejection Ratio	V_{IN} = 8V to 16V	60			dB
Current Sense Amplifier						
	Amplifier Gain	Pin 3 = 0V to 1.1V	3	3.15	3.3	V/V
	Maximum Differential Input Signal	$V_{PIN4} - V_{PIN3}$			≤1.1	V
	Common-Mode Input Voltage		0		V_{DD} – 3V	V
Current Limit Adjust						
	Current Limit Offset Voltage		0.5		1	V
I_B	Input Bias Current				1	nA
Shutdown Terminal						
V_{TB}	Threshold Voltage		0.3	0.35	0.4	V
V_{IN}	Input Voltage Range		0		V_{DD}	V
	Minimum Latching Current at Pin 1		125			µA
	Maximum Nonlatching Current at Pin 1				50	µA
Output Stage						
V_{DD}	Output Voltage	Pin 13	V_{IN}–. 5	V_{IN}	V_{IN} + .5	V
V_{OL}	Output Low Level	I_{SINK} = 20 mA			0.4	V
V_{OL}	Output Low Level	I_{SINK} = 100 mA			2	V
V_{OH}	Output High Level	I_{SOURCE} = 20 mA	V_{DD} – 1V			V
V_{OL}	Output High Level	I_{SOURCE} = 100 mA	V_{DD} – 4V			V
t_R	Output Rise Time	C_L = 1000 pF		50	150	ns
t_F	Output Fall Time	C_L = 1000 pF		50	150	ns
Undervoltage Lockout						
	Start-Up	Threshold	7.25	7.7	8.25	V
	Threshold Hysteresis		0.5	0.75	1	V
Supply						
I_S	Standby Supply Current			2.7	3.8	mA

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 18V
Output Voltage ..... V_{DD} or 18V
Analog Inputs ..... – 0.3V to V_S + 0.3V
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Maximum Chip Temperature ..... 150°C
Plastic Package Thermal Resistance:
θ_{JA} (Junction to Ambient) ..... 140°C/W
θ_{JC} (Junction to Case) ..... 70°C/W

Operating Temperature Range
Commercial ..... 0°C to +70°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

3

PIN DESCRIPTION

Pin No.	Symbol	Description
1	SOFT START/I_{LIM}	Soft Start Adjust / Current Limit. For setting the peak current threshold of sense inputs (pins 3 and 4). Second function of this pin is Soft-Start Adjust.
2	V_{REF} OUT	Reference supply output of 5.1 volts. It can supply a minimum of 10mA.
3	– I_{SENSE} IN	– Current Sense Input. Inverting input for sensing peak current of the pass transistor through series sense current monitor resistor.
4	+ I_{SENSE} IN	+ Current Sense Input. Non-inverting input used in conjunction with pin 3. This senses the positive end of current monitor resistor.
5	+ ERROR AMP IN	+ Error Amp In. Non-inverting input for output voltage regulation.
6	- ERROR AMP IN	– Error Amp In. Inverting input of the amplifier for the reference voltage.
7	COMP	For compensation of the feedback loop response.
8	C_O	Timing capacitor (C_O) input to set oscillator frequency in conjunction with pin 9, R_O, resistor input. Second function is for setting crossover dead time of pin 11and 14 outputs.
9	R_O	Timing resistor (R_O) input to set oscillator frequency by setting constant current charge rate to charge capacitor C_O.
10	SYNC	For PWM controller oscillator synchronization of two or more controllers. or as a clock input to sync oscillator from external signal.
11	OUTPUT	A output drive of phase A from push pull transistors.
12	GROUND	Ground return for all input and output pins.
13	V_{DD}	Supplies power to operate the output drivers only.
14	OUTPUT B	Output of phase B from push pull transistors.
15	V_{IN}	Voltage bias supply for all TC170 circuits except the output transistors.
16	SHUTDOWN	Input pin to disable both output drives to 0V OFF.

Peak Current Limit Setup

Resistors R1 and R2 at the current limit input (pin 1) set the TC170 peak current limit (Figure 1). The potential at pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for $(V_{REF} - 0.35)/R1 < 50\ \mu A$ and is latched for currents greater than 125 μA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.15.

I_{PCL}, the peak current limit, is the current that causes the PWM comparator noninverting input to exceed V1, the potential at the inverting input. Once the comparator trip point is exceeded, both outputs are disabled.

I_{PCL} is easily calculated:

$$I_{PCL} = \frac{V1 - 0.75V}{3.15\ (RS)}$$

where:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

V_{REF} = Internal voltage reference = 5.1V

3.15 = Gain of current-sense amplifier

0.75V = Current limit offset

Both driver outputs (pins 11 and 14) are OFF (LOW) when the peak current limit is exceeded. When the sensed current goes below I_{PCL}, the circuit operates normally.

Output Shutdown

The TC170 outputs can be turned OFF quickly through the shutdown input (pin 16). A signal greater than 350 mV at pin 16 forces the shutdown comparator output HIGH. The PWM latch is held set, disabling the outputs.

Q2 is also turned ON. If $V_{REF}/R1$ is greater than 125 μA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.75V. Q3 remains ON even after the shutdown input signal is removed, because of the positive feedback. The state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at pin 1 is below 0.75V.

The shutdown terminal gives a fast, direct way to disable the TC170 output transistors. System protection and remote shutdown applications are possible.

The input pulse to pin 16 should be at least 500 ns wide and have an amplitude of at least 1V in order to get the minimum propagation delay from input to output. If these parameters are met, the delay should be less than 600 ns at 25°C; however, the delay time will increase as the device temperature rises.

Soft Restart From Shutdown

A soft restart can be programmed if nonlatched shutdown operation is used.

A capacitor at pin 1 will cause a gradual increase in potential toward V1. When the voltage at pin 1 reaches 0.75V, the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Even if a soft start is not required, it is necessary to insert a capacitor between pin 1 and ground if the current I_L is greater than 125 μA. This capacitor will prevent "noise triggering" of the latch, yet minimize the soft-start effect.

Soft-Start Power-Up

During power-up, a capacitor at R1, R2 initiates a soft-start cycle. As the input voltage (pin 15) exceeds the undervoltage lockout potential (7.7V), Q4 is turned OFF, ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.5V, both outputs are disabled.

When the undervoltage lockout level is passed, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current-Sense Amplifier

The current-sense amplifier operates at a fixed gain of 3.15. Maximum differential input voltage (V_{PIN4}–V_{PIN3}) is 1.1V. Common-mode input voltage range is 0V to $V_{IN} - 3V$.

Resistive-sensing methods are shown in Figure 2. In Figure 2(A), a simple RC filter limits transient voltage spikes at pin 4, caused by external output transistor-collector capacitance. Transformer coupling (Figure 3) offers isolation and better power efficiency, but cost and complexity increase.

In order to minimize the propagation delay from the input to the current amplifier to the output terminals, the current ramp should be in the order of 1 μs in width (min). Typical time delay values are in the 300 to 400 ns region at 25°C. The delay time increases with device temperature so that at 50°C, the delay times may be increased by as much as 100 ns.

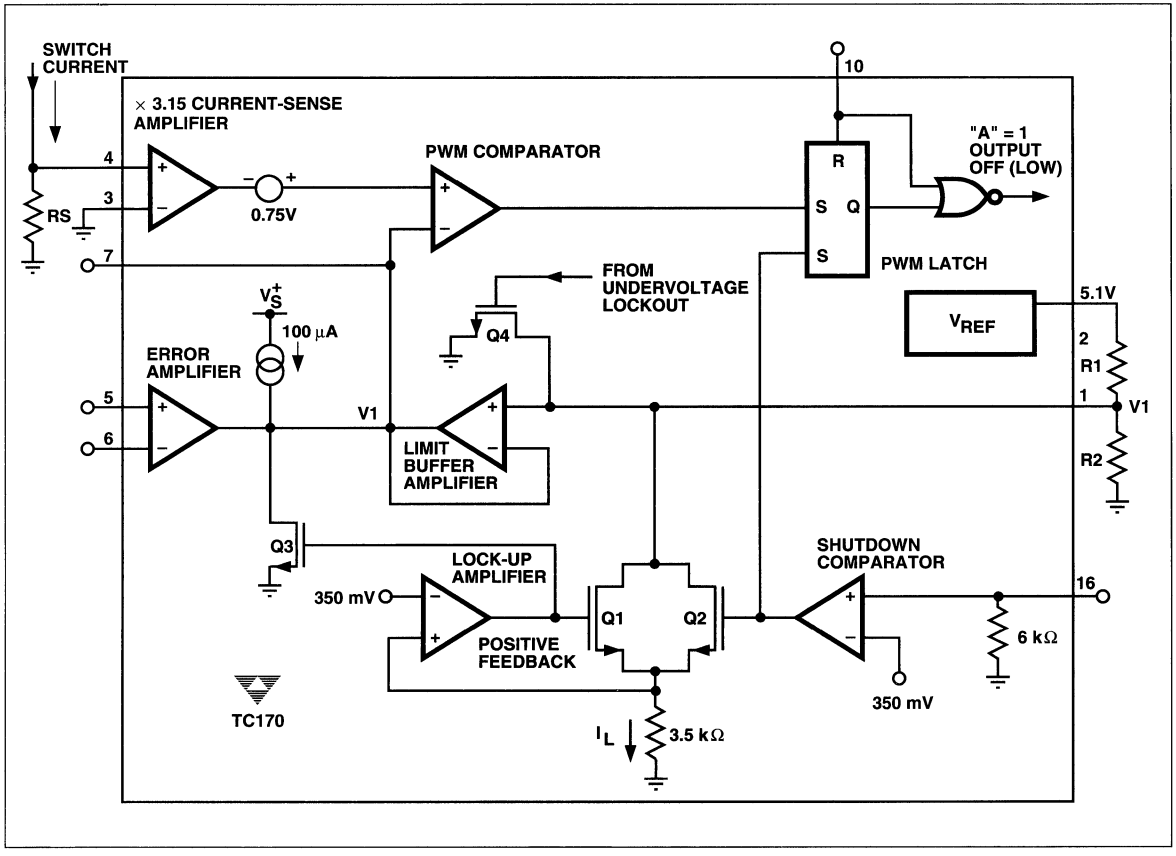


Figure 1 R1 and R2 Set Maximum Peak Output Current

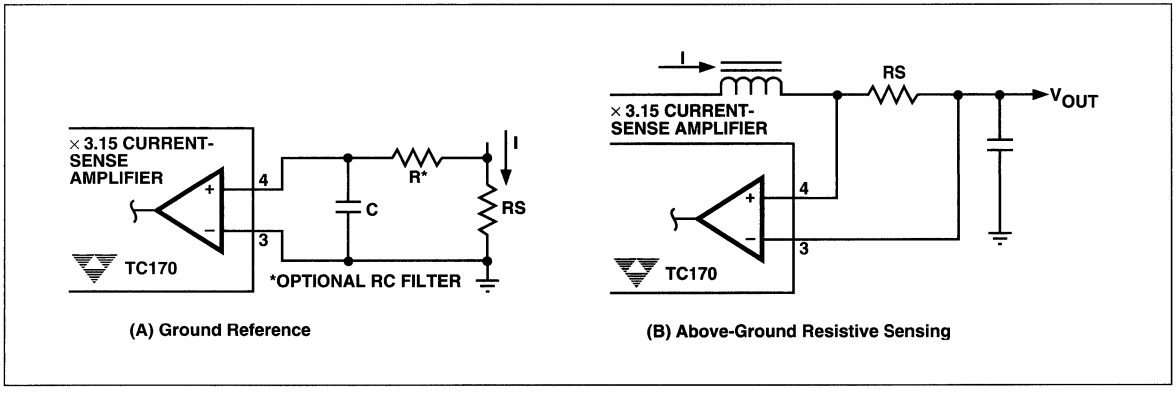


Figure 2 Resistive Sensing

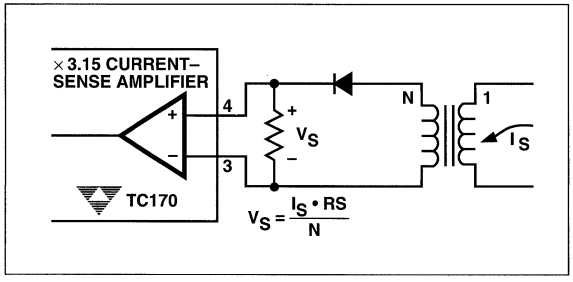


Figure 3 Transformer Isolated Current Sense

Undervoltage Lockout

The undervoltage lockout circuit forces the TC170 outputs OFF (low) if the supply voltage is below 7.7V. Threshold hysteresis is 0.75V and guarantees clean, jitter-free turn-on and turn-off points. The hysteresis also reduces capacitive filtering requirements at the PWM controller supply input (pin 15).

Circuit Synchronization

Current-mode-controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage-mode controllers unequally share the load current, decreasing system reliability.

Two or more TC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TC170 internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding pin 8. Slave controllers derive an oscillator from the bidirectional synchronization output signal at pin 10.

Pin 10 is bidirectional in that it is intended to be both a sync output and input. This is accomplished by making the output driver "weak." This is advantageous in that it eliminates an additional pin from the package but does not enable the device to directly drive another device. In order to make it an effective driver, a buffer is required (Figure 4). In order to use pin 10 as a sync input, it is necessary to overcome the internal driver. This requires a pulse with an amplitude equal to V_{IN}. Since V_{IN} must be above 8.25V for the undervoltage lockout to be disabled, a CMOS or open-collector TTL driver should be used.

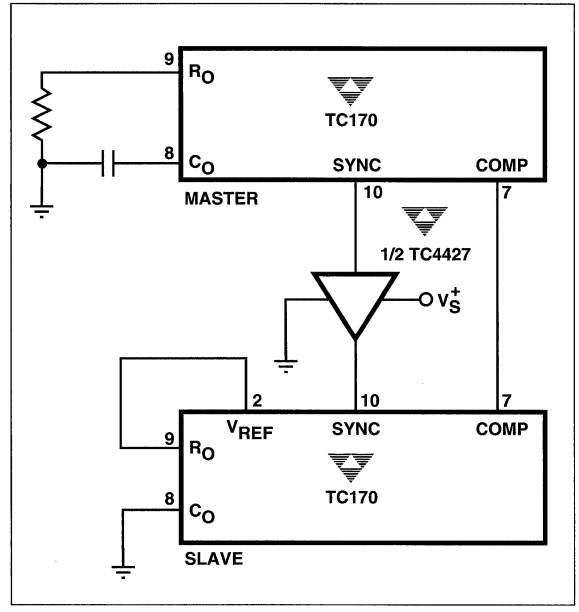


Figure 4 Master/Slave Parallel Operation

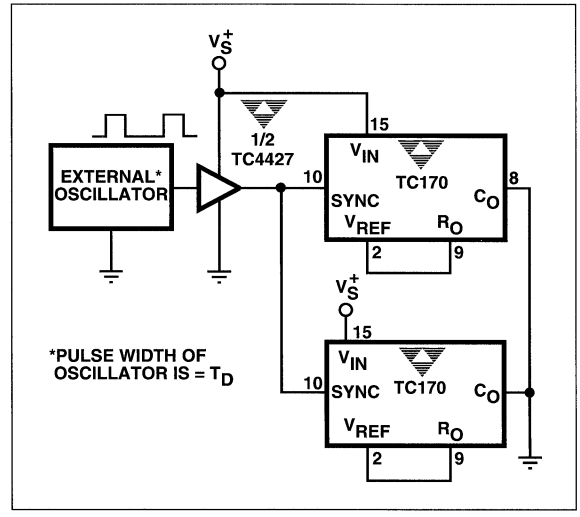


Figure 5 External Clock Synchronization

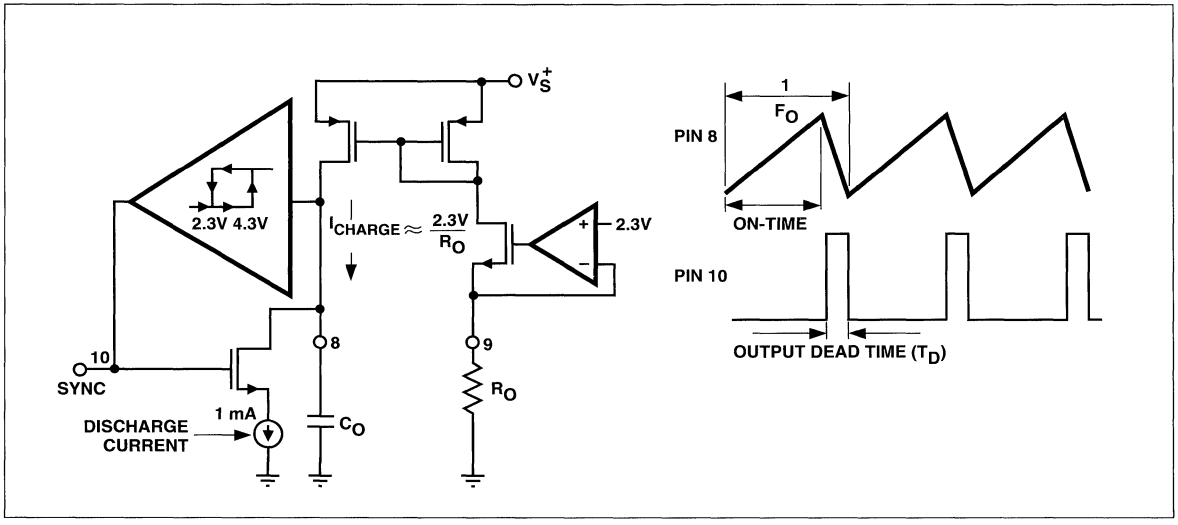


Figure 6 Oscillator Circuit

Oscillator Frequency and Output Dead Time

The oscillator frequency for R_O = 24 kΩ and C_O = 1000 pF is:

$$F_O = \left[\frac{1.27}{R_O C_O} - \frac{2800}{R_O^2 C_O} \right] \frac{C_O}{C_O + 150 \times 10^{-12}}$$

where: R_O = Oscillator Resistor (Ω)
C_O = Oscillator Capacitor (F)
F_O = Oscillator Frequency (Hz)

The oscillator resistor can range from 5 kΩ to 50 kΩ.

Oscillator capacitor can range from 250 pF to 1000 pF. Figure 7 shows typical operation for various resistance and capacitance values.

During transitions between the two outputs, simultaneous conduction is prevented. Oscillator fall time controls the output off, or dead time (Figure 6).

Dead time is approximately:

$$T_D = \frac{2000\ [C_O]}{1 - \left(\frac{2.3}{R_O} \right)}$$

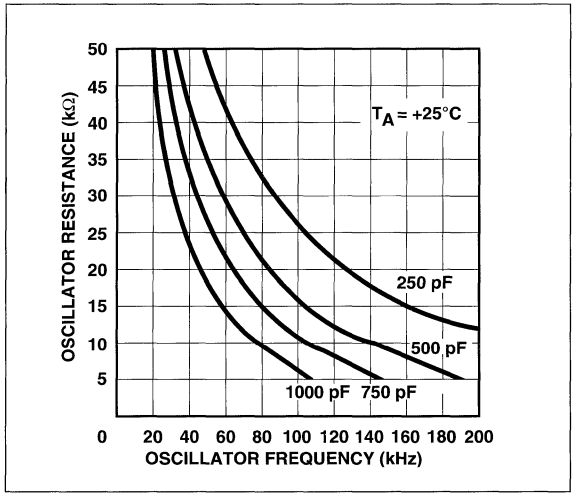


Figure 7 Oscillator Frequency vs Oscillator Resistance

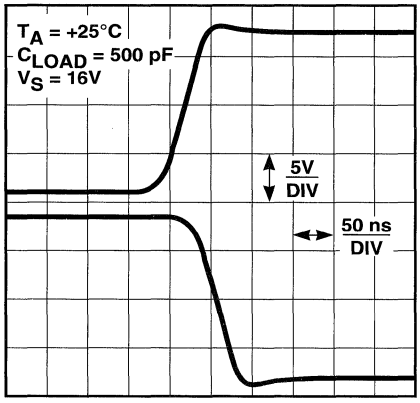
where: R_O = Oscillator Resistor (kΩ)
C_O = Oscillator Capacitor (pF)
T_D = Output Dead Time (sec)

Maximum possible duty cycle is set by the dead time.

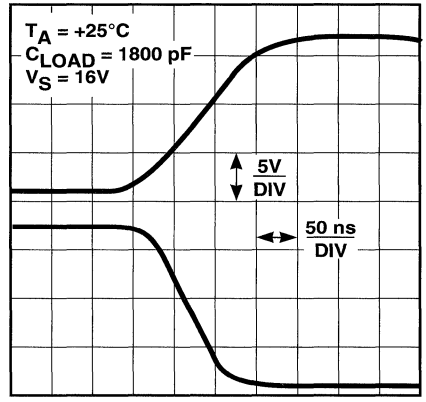
TC170

TYPICAL CHARACTERISTIC CURVES

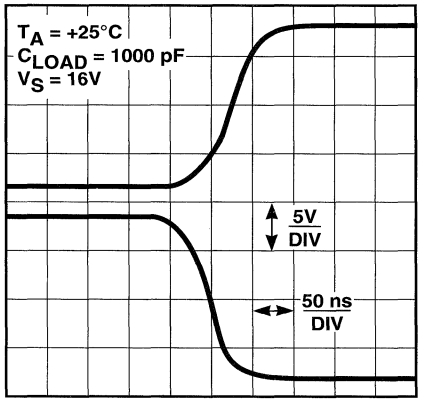
Output Rise and Fall Times



Output Rise and Fall Times



Output Rise and Fall Times



TelCom Semiconductor, Inc.

TC660

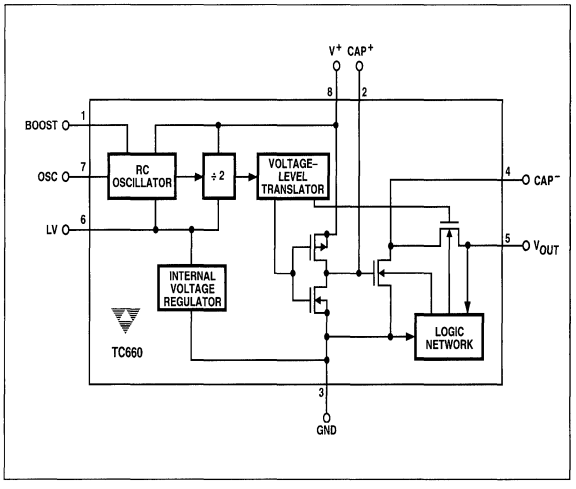
*CONTACT FACTORY FOR FULL DATA SHEET

DC-TO-DC VOLTAGE CONVERTER

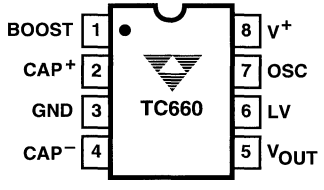
FEATURES

- **High Current 100mA**
- **Converts (+ 1.5V to 5.5V) to (- 1.5V to -5.5V)**
- **Excellent Power Efficiency ..... 88% typ**
- **Low Power Requirement ..... 200 µA @ 5 V_{IN}**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **Improved ESD Protection ..... Up to 3KV**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (DIP and SO)



NC = NO INTERNAL CONNECTION

GENERAL DESCRIPTION

The TC660 DC-to-DC voltage converter will generate a negative voltage from a positive source. With two external capacitors, the TC660 will convert a 1.5V to 5V input signal to a –1.5V to –5V level.

Many analog-to-digital converters, digital-to-analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TC660 allows +5V digital logic systems to incorporate these analog components without adding an additional main power source. The TC660 can lower total system cost, ease engineering development, and save space, power and weight.

The TC660 charges a capacitor to the applied supply voltage. Internal analog switches connect the capacitor across the output. Charge is transferred to an output storage capacitor, completing the voltage conversion. Operation requires only two external capacitors.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage-level translator, four output power MOS switches, and a unique logic element which ensures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5V. This frequency can be lowered by the addition of an external capacitor to the OSC terminal (pin 7), or raised to approx. 45 kHz by connecting BOOST to V^+. Alternatively, the oscillator may be overdriven by an external clock.

The low voltage (LV) terminal (pin 6) may be tied to GND (pin 3) to bypass the internal series regulator and improve LV operation. At medium-to-high voltages (+3.5V to +10V), the LV pin is left floating to prevent device latch-up.

The TC660 open-circuit output voltage is equal to the input voltage to within 0.1%. The TC660 has a 98% power conversion efficiency for 2 mA to 5 mA load currents.

ORDERING INFORMATION

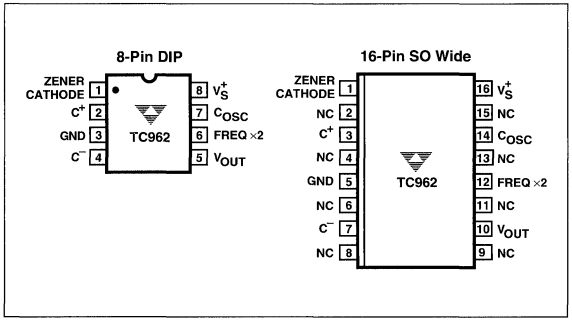
Part No.	Package	Temperature Range
TC660CPA	8-Pin Plastic DIP	0°C to +70°C
TC660EOA	8-Pin SO	– 40°C to +85°C
TC660EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC660COA	8-Pin SO	0°C to +70°C

HIGH CURRENT DC-TO-DC CONVERTER

FEATURES

- **Pin Compatible With TC7662/ICL7662/SI7661**
- **High Output Current ..... 80 mA**
- **No External Diodes Required**
- **Wide Operating Range ..... 3V to 18V**
- **Low Output Impedance ..... 28Ω Typ**
- **No Low Voltage Terminal Required**
- **Application Zener On Chip**
- **OSC Frequency Doubling Pin Option for Smaller Output Capacitors**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC962 is an advanced version of the industry-standard 7662 high-voltage DC-to-DC converter. Using improved design techniques and CMOS construction, the TC962 can source as much as 80 mA versus the 7662's 20 mA capability.

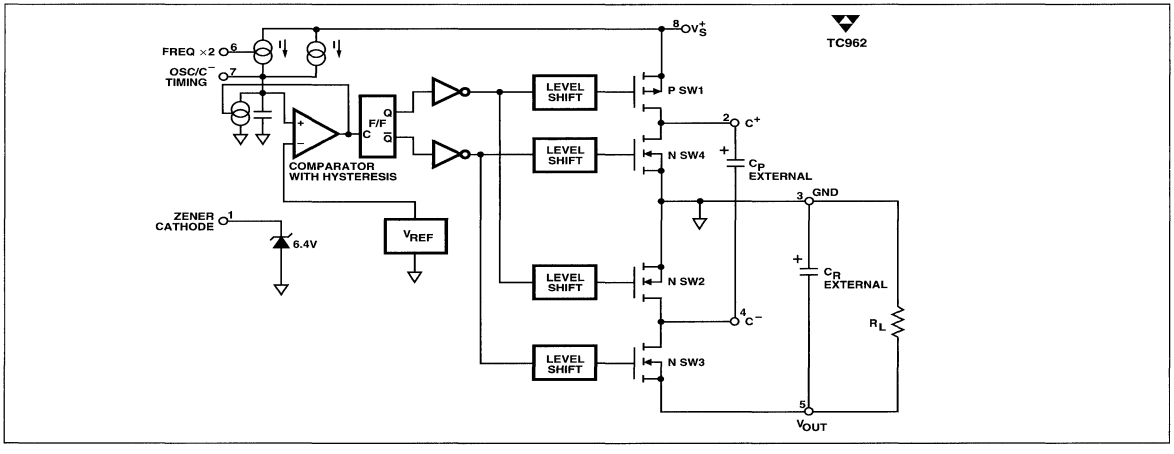
As an inverter, the TC962 can put out voltages as high as 18V and as low as 3V without the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9%, and power conversion efficiency is 97%.

The low voltage terminal (pin 6) required in some 7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12 kHz to 24 kHz. This will allow the use of smaller capacitors for the same output current and ripple, in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TC962 (such as paralleling), driving this pin directly will cause the internal oscillator to sync to the external clock.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC962CPA	8-Pin Plastic DIP	0°C to +70°C
TC962IJA	8-Pin CerDIP	– 25°C to +85°C
TC962EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC962MJA	8-Pin CerDIP	– 55°C to +125°C
TC962COE	16-Pin SO Wide	0 to +70°C
TC962EOE	16-Pin SO Wide	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC962

Pin 1, which is used as a test pin on the 7662, is a voltage reference zener on the TC962. This zener (6.4V at 5 mA) has a dynamic impedance of 12Ω and is intended for use where the TC962 is supplying current to external regulator circuitry and a reference is needed for the regulator circuit. (See applications section.)

The TC962 is compatible with the LTC1044, SI7661, and ICL7662. It should be used in designs that require greater power and/or less input to output voltage drop. It offers superior performance over the ICL7660S.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+_S to GND) ..... +18V
Input Voltage (Any Pin) ..... (V^+_S + 0.3) to (V^-_S – 0.3)
Current Into Any Pin ..... 10 mA
ESD Protection ..... ±2000V
Output Short Circuit ..... Continuous (at 5.5V Input)
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
- CPA, COE ..... 0°C to +70°C
- IJA ..... – 25°C to +85°C
- EOE, EPA ..... – 40°C to +85°C
- MJA ..... – 55°C to +125°C

Max Dissipation
- COE, CPA, EOE, EPA ..... 375 mW
- IJA, MJA ..... 500 mW

Package Thermal Resistance
- CerDIP, $R_{\theta J-A}$ ..... 90°C/W
- PDIP, $R_{\theta J-A}$ ..... 140°C/W

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V^+_S = 15V, T_A = +25°C (See Test Circuit)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V^+_S	Supply Voltage		3		18	V
I_S	Supply Current	$R_L = \infty$				
	V^+_S = 15V	T_A = +25°C		510	700	µA
		0 ≤ T_A ≤ +70°C		560		µA
		–55 ≤ T_A ≤ +125°C		650		µA
	V^+_S = 5V	T_A = +25°C		190		µA
		0 ≤ T_A < +70°C		210		µA
		–55 ≤ T_A ≤ +125°C		210		µA
R_O	Output Source Resistance	I_L = 20 mA, V^+_S = 15V		32	37	Ω
		I_L = 80 mA, V^+_S = 15V		5	40	Ω
		I_L = 3 mA, V^+_S = 5V		—	50	Ω
C_{OSC}	Oscillator Frequency	Pin 6 Open		12		kHz
		Pin 6 GND		24		kHz
P_{EFF}	Power Efficiency	V^+_S = 15V R_L = 2 kΩ	93	97		%
V_{DEF}	Voltage Efficiency	V^+_S = 15V $R_L = \infty$	99	99.9		%
		Over Temperature Range	96	—		%
V_Z	Zener Voltage	I_Z = 5 mA	6.0	6.2	6.4	V
Z_{ZT}	Zener Impedance	I_L = 2.5 mA to 7.5 mA		12		Ω

APPLICATIONS INFORMATION

Theory of Operation

The TC962 is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional diagram (page 1) shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown:

$$3\ (R_{DS(ON)}\ C_P) < C_P/(0.5\ f_{OSC})$$

In the next cycle, SW1 and SW2 are turned off and after a very short interval of all switches being off (this prevents large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C_P is then transferred to C_R, BUT WITH THE POLARITY INVERTED. In this way, a negative voltage is now derived.

Page 1 shows a functional diagram of the TC962. An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is returned to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC962. Grounding pin 6 will turn on a current source and double the frequency. This will double the charge current going into the internal capacitor, as well as any capacitor added to pin 7.

A zener diode has been added to the TC962 for use as a reference in building external regulators. This zener runs from pin 1 to ground.

Capacitors

In early charge pump converters, the capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this, let's look at a model of a typical electrolytic capacitor (Figure 1).

Note that one of its characteristics is ESR (equivalent series resistance). This parasitic resistance winds up in series with the load. Thus, both voltage conversion efficiency and power conversion efficiency are compromised if a low ESR capacitor is not used.

In the test circuit, for example, just changing two capacitors, C_P and C_R, from capacitors with unspecified ESR to low ESR-type output, impedance changes from 36Ω to 28Ω, an improvement of 23%!

This applies to all types of capacitors, including film types (polyester, polycarbonate, etc.).

Some applications information suggest that the capacitor is not critical and attribute the limiting factor of the capacitor to its reactive value. Let's examine this:

$$X_C = \frac{1}{2\pi f\ C} \quad \text{and} \quad Z_C = \frac{X_C}{DS},$$

where DS (duty cycle) = 50%.

Thus, $Z_C \approx 2.6\Omega$ at f = 12 kHz, where C = 10 µF.

For the TC962, f = 12,000 Hz, and a typical value of C would be 10 µF. This is a reactive impedance of ≈ 2.6Ω. If the ESR is as great as 5Ω, the reactive value is not as critical as it would first appear, as the ESR would predominate. The 5Ω value is typical of a general-purpose electrolytic capacitor.

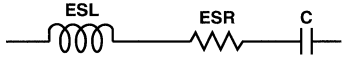
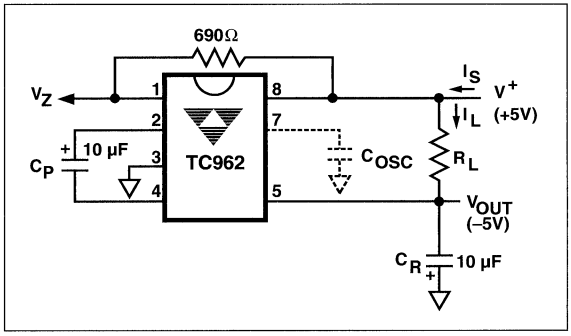


Figure 1 Typical Electrolytic Capacitor

Latch Up

All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input from going above or below the supply rail, or latch up will occur. The result of latch up is an effective short between V^+_S and V^-_S. Unless the power supply input has a current limit, this latch-up phenomena will result in damage to the device. (See Application Note 31 for additional information.)

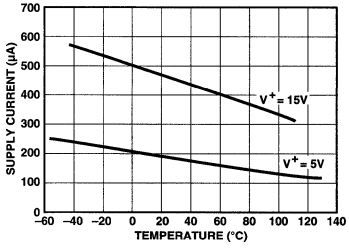
TEST CIRCUIT



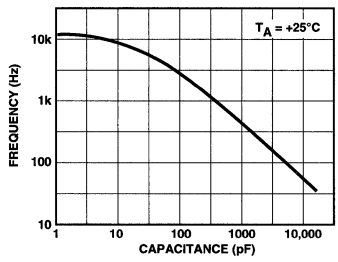
TC962

TYPICAL CHARACTERISTICS CURVES

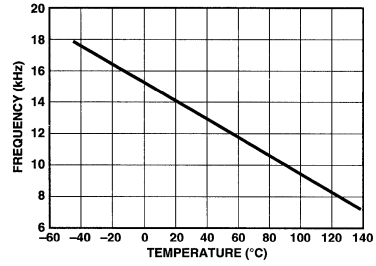
Supply Current vs Temperature



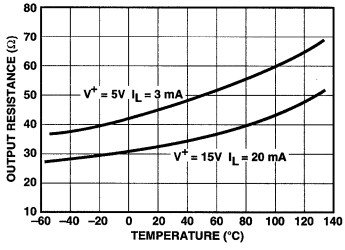
Oscillator Frequency vs C_{EXT}



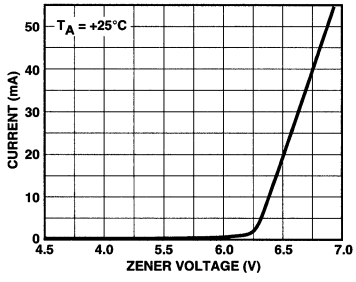
Frequency vs Temperature



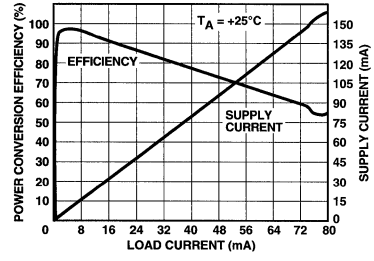
Output Resistance vs Temperature



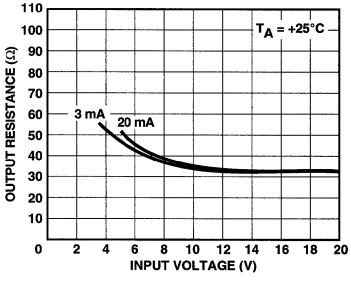
Current vs Zener Voltage



Power Conversion Efficiency vs I_{LOAD}

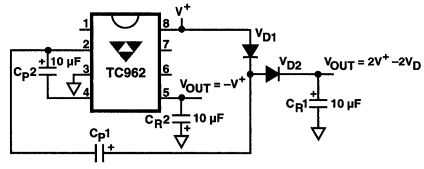


Output Resistance vs Input Voltage

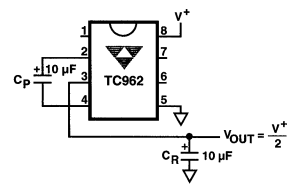


TYPICAL APPLICATIONS

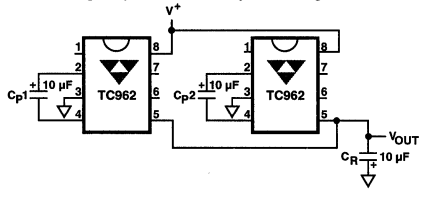
Combined Negative Converter and Positive Multiplier



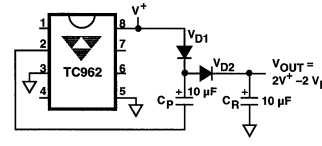
Split V^+ In Half



Lowering Output Resistance by Paralleling Devices



Positive Voltage Multiplier

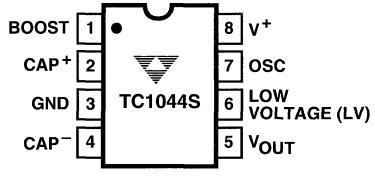


DC-TO-DC VOLTAGE CONVERTER

FEATURES

- **Converts +5V Logic Supply to ±5V System**
- **Wide Input Voltage Range ..... 1.5V to 12V**
- **Efficient Voltage Conversion 99.9%**
- **Excellent Power Efficiency 98%**
- **Low Power Consumption ..... 80 μA @ V_{IN} = 5V**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **RS-232 Negative Power Supply**
- **Available in Small Outline (SO) Package**
- **Improved ESD Protection ..... Up to 10KV**
- **No External Diode Required for High Voltage Operation**
- **Frequency Boost Raises F_{OSC} to 45kHz**

PIN CONFIGURATION (DIP and SO)



GENERAL DESCRIPTION

The TC1044S DC-to-DC voltage converter is the Super Voltage Converter version of TC7660. Added features include extended operating supply voltage range up to 12V, and frequency boost pin for higher operating frequency to lower output impedance with smaller capacitors.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage-level translator, four output power MOS switches, and a unique logic element which ensures latch-up free operation.

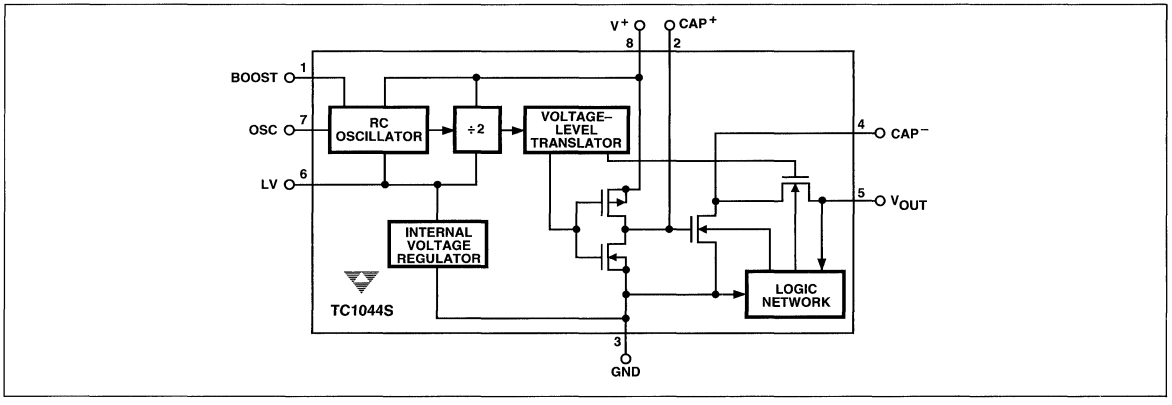
The oscillator, with boost, pin 1 open or grounded, and osc pin 7 open, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5V. When boost pin 1 is connected to V+, nominal frequency increases to 45 kHz. If operation below 10 kHz is desired, a capacitor may be added to osc pin 7 with boost pin 1 open. The oscillator may also be overdriven by an external clock.

The TC1044S can generate a negative voltage from a positive source. With two external capacitors, the TC1044S will convert a 1.5V to 12V input signal to a -1.5V to -12V level. The TC1044S easily generates -5V in +5V digital systems.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1044SCPA	8-Pin Plastic DIP	0°C to +70°C
TC1044SIJA	8-Pin CerDIP	–25°C to +85°C
TC1044SEOA	8-Pin SO	–40°C to +85°C
TC1044SEPA	8-Pin Plastic DIP	–40°C to +85°C
TC1044SMJA	8-Pin CerDIP	–55°C to +125°C
TC1044SCOA	8-Pin SO	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



TC1044S

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +13V
LV, Boost and OSC Inputs
Voltage (Note 1) ..... – 0.3V to (V^++0.3V) for V^+ <5.5V
(V^+ – 5.5V) to (V^++0.3V) for V^+ >5.5V
Current Into LV (Note 1) ..... 20 µA for V^+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous

Power Dissipation (Note 2)
CerDIP ..... 500 mW
Plastic DIP ..... 375 mW
Operating Temperature Range
C Suffix ..... 0°C to +70°C
I Suffix ..... – 25°C to +85°C
E Suffix ..... – 40°C to +85°C
M Suffix ..... – 55°C to +125°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

Specifications Measured Over Operating Temperature Range With, V^+ = 5V, C_{OSC} = 0, Test Circuit (Figure 1), unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current	$R_L = \infty$, 25°C	—	80	160	µA
		0°C < T_A < +70°C			180	
		– 40°C < T_A < +85°C			180	
		– 55°C < T_A < +125°C			200	
I^+	Supply Current (Boost pin = V+)	0°C < T_A < +70°C	—	—	300	µA
		– 40°C < T_A < +85°C			350	
		– 55°C < T_A < +125°C			400	
V^+_{H2}	Supply Voltage Range, High	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV Open	3	—	12	V
V^+_{L2}	Supply Voltage Range, Low	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV to GND	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25°C	—	60	100	Ω
		I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C	—	70	120	Ω
		I_{OUT} = 20 mA, –40°C ≤ T_A ≤ +85°C	—	70	120	Ω
		I_{OUT} = 20 mA, –55°C ≤ T_A ≤ +125°C	—	105	150	Ω
		V^+ = 2V, I_{OUT} = 3 mA, LV to GND				
		0°C ≤ T_A ≤ +70°C	—	—	250	Ω
		– 55°C ≤ T_A ≤ +125°C	—	—	400	Ω
F_{OSC}	Oscillator Frequency	Pin 7 open; Pin 1 open or GND	—	10	—	kHz
		Pin 1 = V^+	—	45	—	kHz
P_{EFF}	Power Efficiency	R_L = 5 kΩ	96	98	—	%
		T_{MIN} < T_A < T_{MAX}	95	97	—	%
V_{OUT} E_{FF}	Voltage Conversion Efficiency	$R_L = \infty$	99	99.9	—	%
Z_{OSC}	Oscillator Impedance	V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

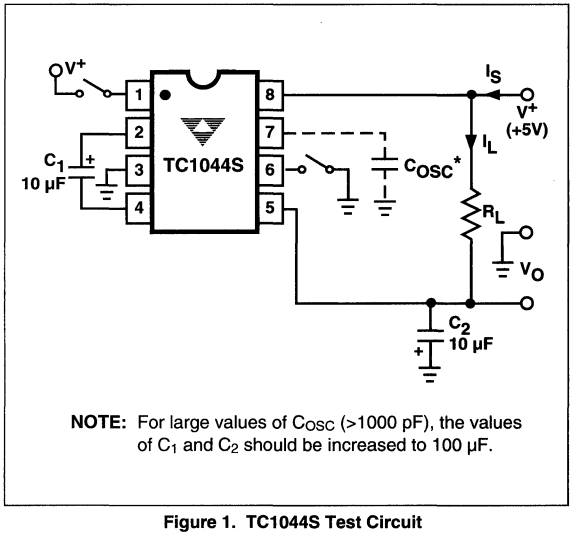
NOTES: 1. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC1044S.
2. Derate linearly above 50°C by 5.5 mW/°C.

Circuit Description

The TC1044S contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The four switches in Figure 2 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC1044S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.



NOTE: For large values of C_{OSC} (>1000 pF), the values of C_1 and C_2 should be increased to 100 µF.

Figure 1. TC1044S Test Circuit

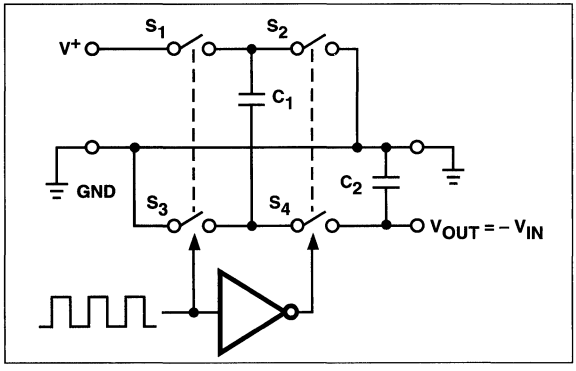


Figure 2. Idealized Switched Capacitor

The voltage regulator portion of the TC1044S is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC1044S approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

TC1044S

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC1044S and the + terminal of C_2 must be connected to GND.

Simple Negative Voltage Converter

Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

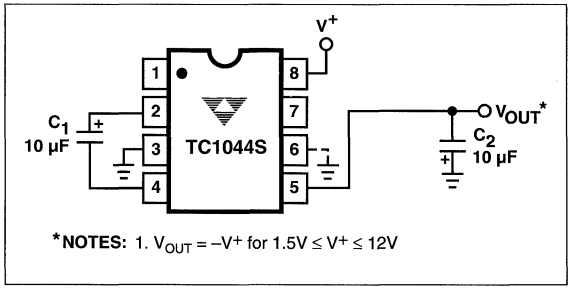


Figure 3. Simple Negative Converter

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of –10 mA and a supply voltage of +5V, the output voltage would be –4.3V.

The dynamic output impedance of the TC1044S is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f\, C_1} = 3.18\Omega,$$

where f = 10 kHz and C_1 = 10 µF.

Paralleling Devices

Any number of TC1044S voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of TC1044S})}{n\ (\text{number of devices})}$$

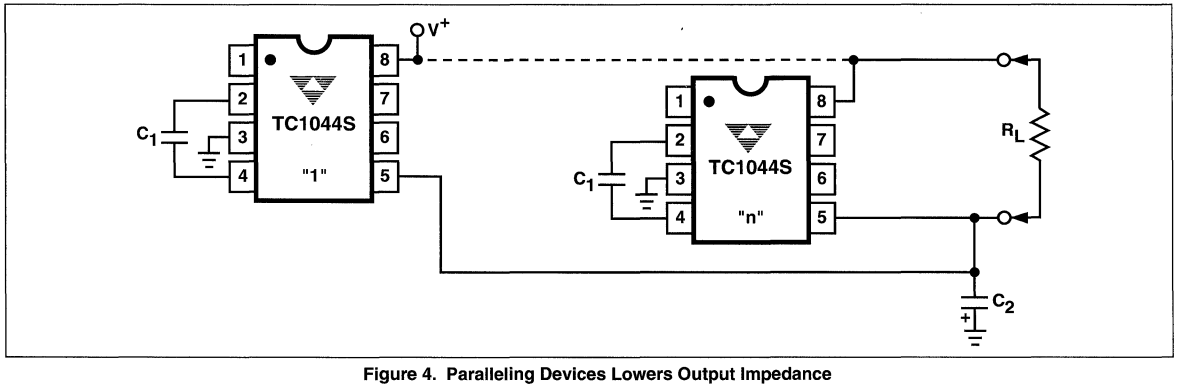


Figure 4. Paralleling Devices Lowers Output Impedance

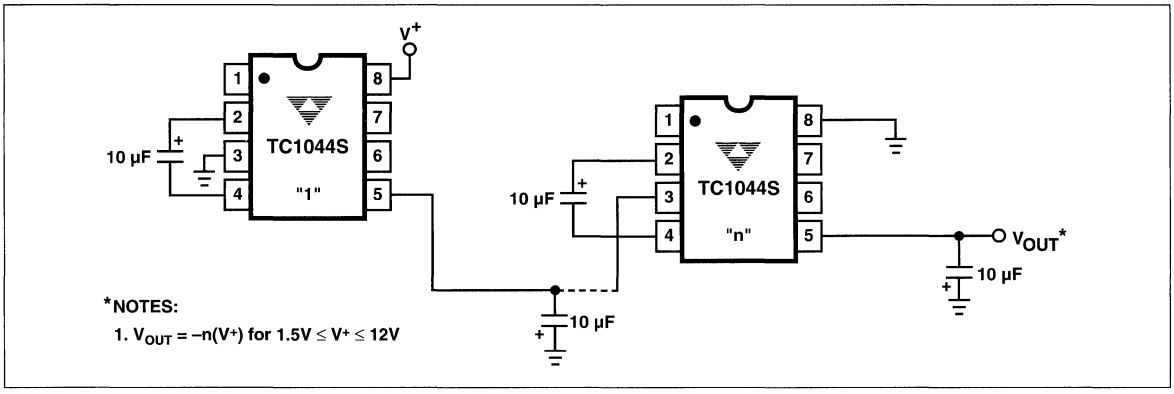


Figure 5. Increased Output Voltage by Cascading Devices

Cascading Devices

The TC1044S may be cascaded as shown (Figure 5) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC1044S R_{OUT} values.

Changing the TC1044S Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, frequency boost pin may be connected to V+ to increase oscillator frequency to 45 kHz from a nominal of 10 kHz for an input supply voltage of 5.0 volts. The oscillator may also be synchronized to an external clock as shown in Figure 6. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

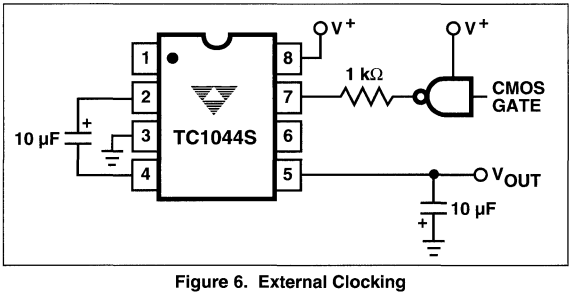


Figure 6. External Clocking

It is also possible to increase the conversion efficiency of the TC1044S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 µF to 100 µF).

Positive Voltage Multiplication

The TC1044S may be employed to achieve positive voltage multiplication using the circuit shown in Figure 8. In this application, the pump inverter switches of the TC1044S are used to charge C_1 to a voltage level of $V^+ – V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2\ V^+) – (2\ V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

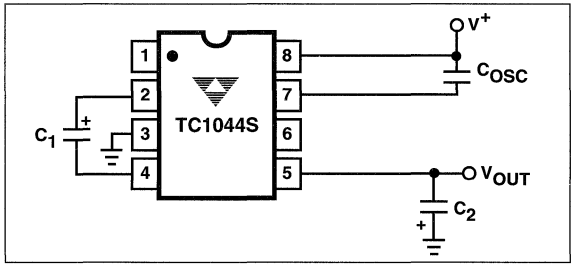


Figure 7. Lowering Oscillator Frequency

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 9 combines the functions shown in Figures 3 and 8 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 10 shows a TC1044S transforming –5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 9, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 9 would never turn on), or else the diode and resistor shown dotted in Figure 10 can be used to "force" the internal regulator on.

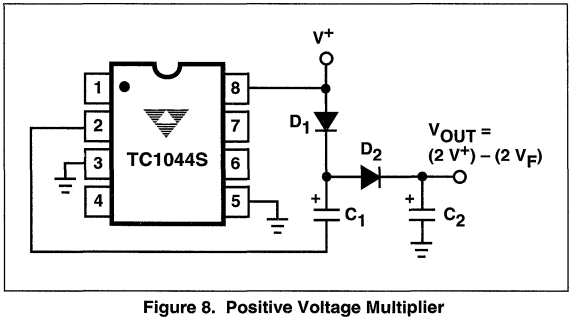


Figure 8. Positive Voltage Multiplier

Voltage Splitting

The same bidirectional characteristics used in Figure 10 can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5, +15V can be converted (via +7.5V and –7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

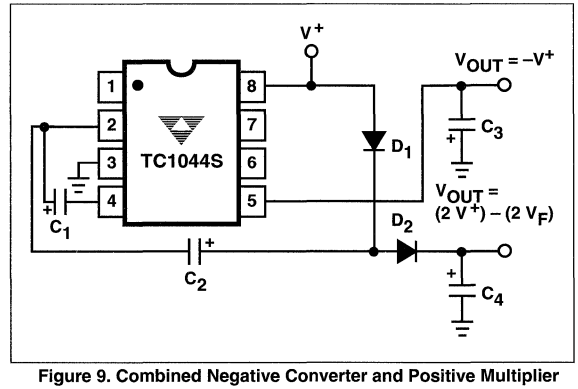


Figure 9. Combined Negative Converter and Positive Multiplier

Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

Negative Supply Generation for 4-1/2 Digit Data Acquisition System

The TC7135 is a 4-1/2 digit ADC operating from ±5V supplies. The TC1044S provides an inexpensive –5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

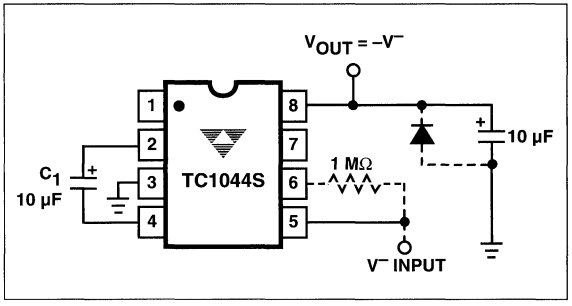


Figure 10. Positive Voltage Conversion

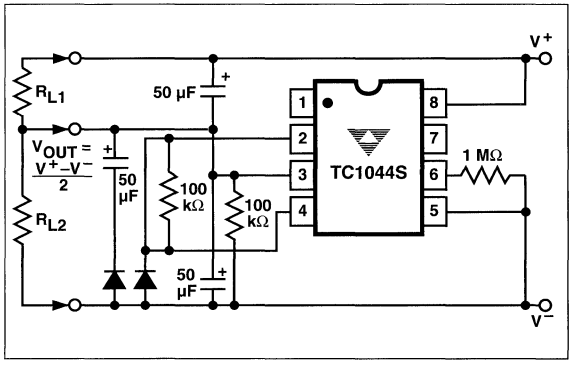


Figure 11. Splitting a Supply in Half

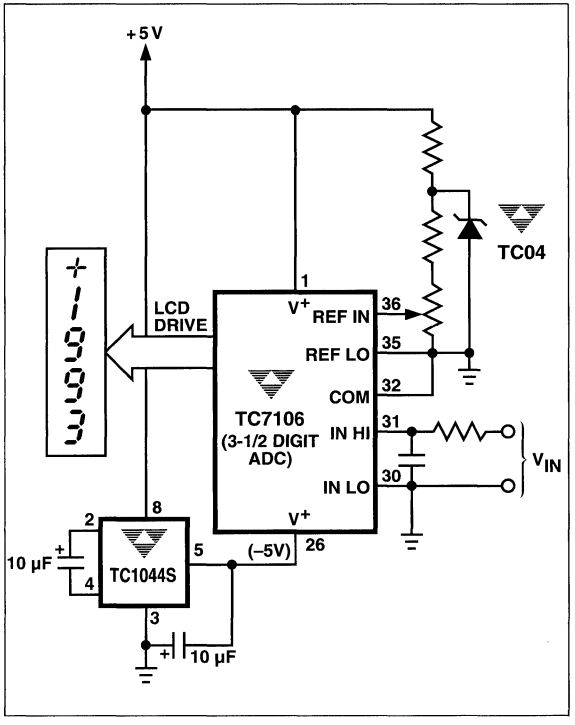


Figure 12a. Fixed Power Supply Operation of TC7106 ADC

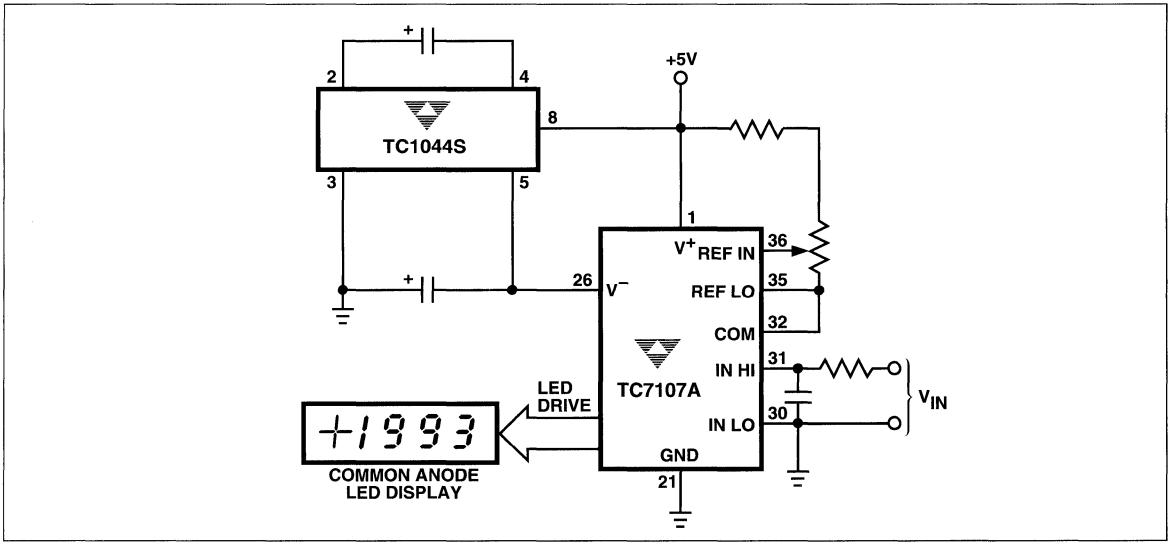


Figure 12b. Negative Power Supply Generation for TC7107A ADC

TC1044S

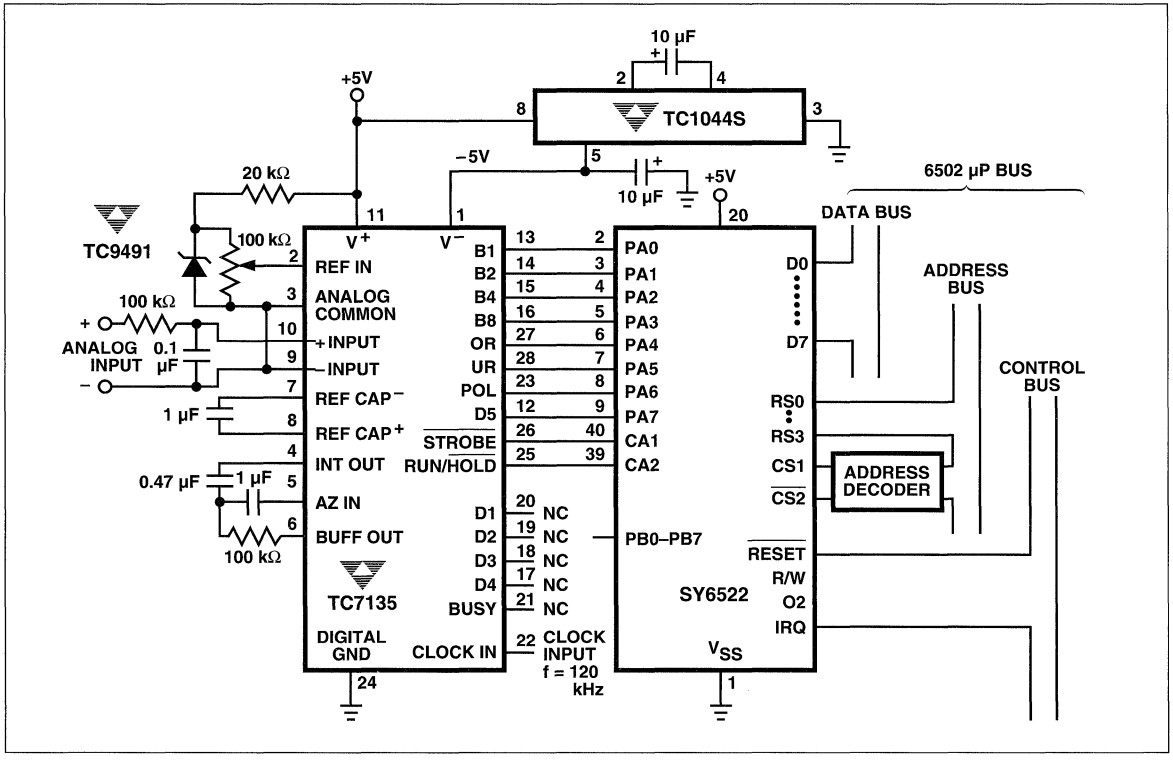
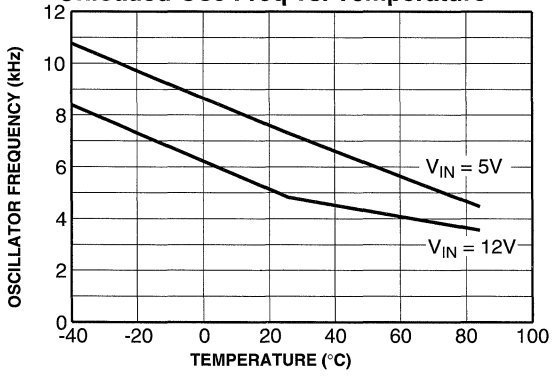


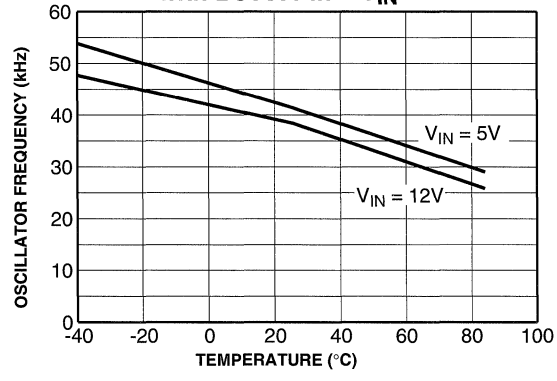
Figure 13. TC1044S Supplies –5V for Converters in Microprocessor-Controlled Data Acquisition Systems

TYPICAL CHARACTERISTICS

Unloaded Osc Freq vs. Temperature

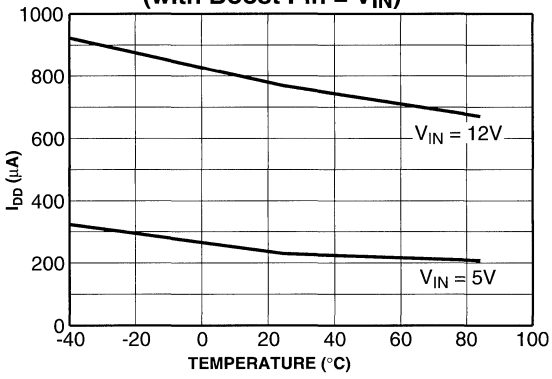


Unloaded Osc Freq vs. Temperature with Boost Pin = V_{IN}

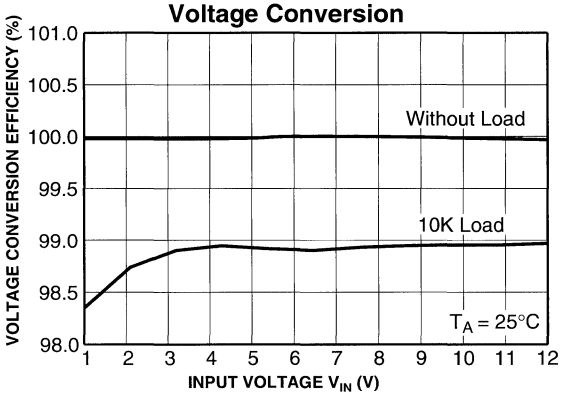


TYPICAL CHARACTERISTICS *(cont.)*

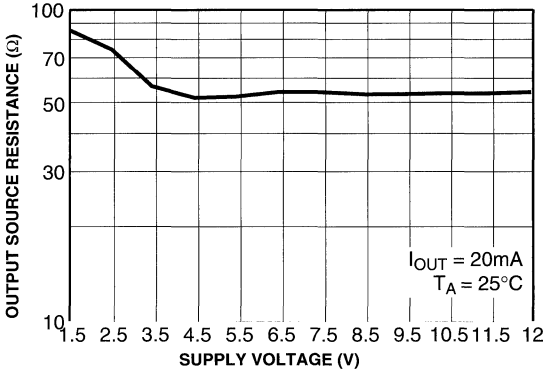
Supply Current vs. Temperature (with Boost Pin = V_{IN})



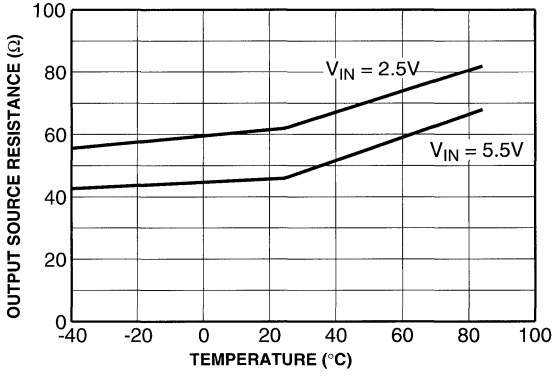
Voltage Conversion



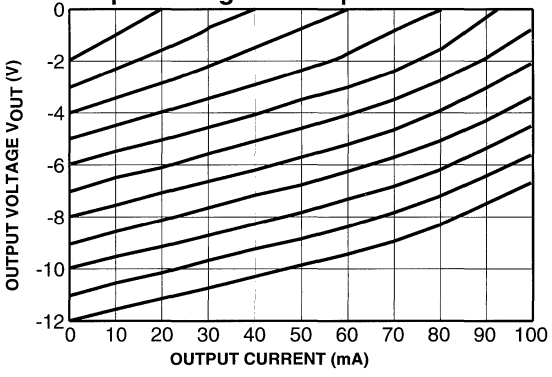
Output Source Resistance vs. Supply Voltage



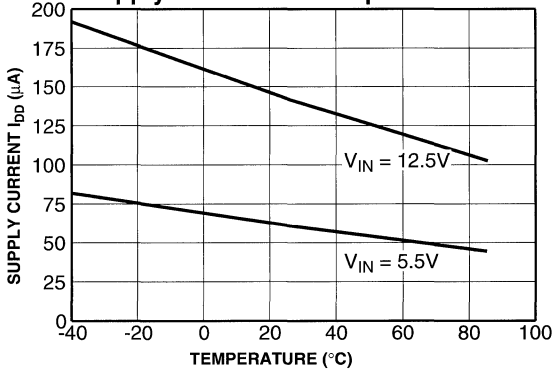
Output Source Resistance vs. Temperature



Output Voltage vs. Output Current



Supply Current vs. Temperature

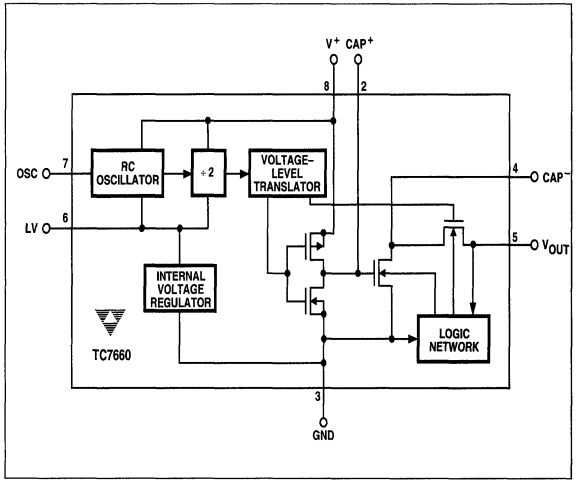


DC-TO-DC VOLTAGE CONVERTER

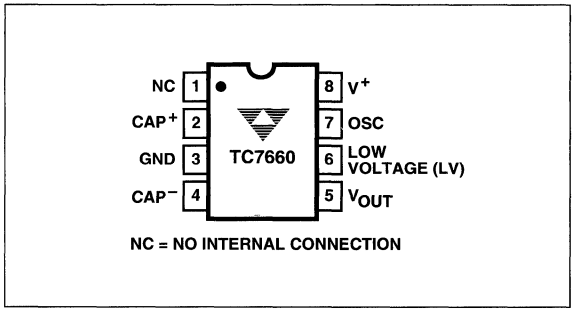
FEATURES

- **Converts +5V Logic Supply to ±5V System**
- **Wide Input Voltage Range ..... 1.5V to 10V**
- **Efficient Voltage Conversion 99.9%**
- **Excellent Power Efficiency 98%**
- **Low Power Supply ..... 80 μA @ 5 V_{IN}**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **RS232 Negative Power Supply**
- **Available in Small Outline (SO) Package**
- **Improved ESD Protection ..... Up to 3KV**
- **No Dx Diode Required for High Voltage Operation**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (DIP and SO)



NC = NO INTERNAL CONNECTION

GENERAL DESCRIPTION

The TC7660 DC-to-DC voltage converter will generate a negative voltage from a positive source. With two external capacitors, the TC7660 will convert a 1.5V to 10V input signal to a –1.5V to –10V level. The TC7660 easily generates –5V in +5V digital systems.

Many analog-to-digital converters, digital-to-analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TC7660 allows +5V digital logic systems to incorporate these analog components without adding an additional main power source. The TC7660 can lower total system cost, ease engineering development, and save space, power and weight.

The TC7660 charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor, completing the voltage conversion. Operation requires only two external capacitors for supply voltage <6.5V.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage-level translator, four output power MOS switches, and a unique logic element which ensures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5V. This frequency can be lowered by the addition of an external capacitor to the OSC terminal (pin 7), or the oscillator may be overdriven by an external clock.

The low voltage (LV) terminal (pin 6) may be tied to GND (pin 3) to bypass the internal series regulator and improve LV operation. At medium-to-high voltages (+3.5V to +10V), the LV pin is left floating to prevent device latch-up.

The TC7660 open-circuit output voltage is equal to the input voltage to within 0.1%. The TC7660 has a 98% power conversion efficiency for 2 mA to 5 mA load currents.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7660CPA	8-Pin Plastic DIP	0°C to +70°C
TC7660IJA	8-Pin CerDIP	– 40°C to +85°C
TC7660EOA	8-Pin SO	– 40°C to +85°C
TC7660EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7660MJA	8-Pin CerDIP	– 55°C to +125°C
TC7660COA	8-Pin SO	0°C to +70°C

TC7660

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +10.5V
LV and OSC Inputs
Voltage (Note 1) ..... –0.3V to (V^++0.3V)
for V^+ <5.5V
(V^+–5.5V) to (V^++0.3V)
for V^+ >5.5V
Current Into LV (Note 1) .....20 µA for V^+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq$ 5.5V) ..... Continuous
Power Dissipation (Note 2)
CerDIP ..... 500 mW
Plastic DIP ..... 375 mW
Operating Temperature Range
C Suffix .....0°C to +70°C
I Suffix .....–25°C to +85°C
E Suffix .....–40°C to +85°C
M Suffix .....–55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

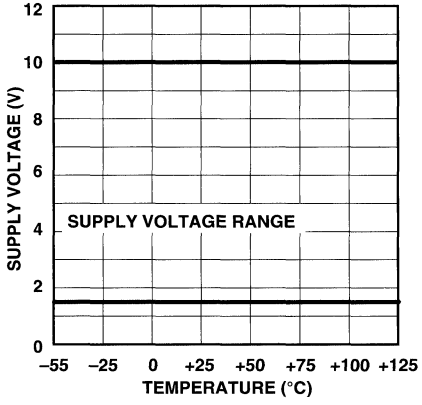
Specifications Measured Over Operating Temperature Range With, V^+ = 5V, C_{OSC} = 0, Test Circuit (Figure 1), unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I+	Supply Current	$R_L = \infty$	—	80	180	µA
V^+_H	Supply Voltage Range, High	Min $\leq T_A \leq$ Max, R_L = 10 kΩ, LV Open	3	—	10	V
V^+_L	Supply Voltage Range, Low	Min $\leq T_A \leq$ Max, R_L = 10 kΩ, LV to GND	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25°C	—	70	100	Ω
		I_{OUT} = 20 mA, 0°C $\leq T_A \leq$ +70°C (C Device)	—	—	120	Ω
		I_{OUT} = 20 mA, –25°C $\leq T_A \leq$ +85°C (I Device)	—	—	130	Ω
		I_{OUT} = 20 mA, –55°C $\leq T_A \leq$ +125°C (M Device)	—	104	150	Ω
		V^+ = 2V, I_{OUT} = 3 mA, LV to GND 0°C $\leq T_A \leq$ +70°C	—	150	300	Ω
		V^+ = 2V, I_{OUT} = 3 mA, LV to GND –55°C $\leq T_A \leq$ +125°C (Note 3)	—	160	600	Ω
			—	10	—	kHz
		R_L = 5 kΩ	95	98	—	%
		$R_L = \infty$	97	99.9	—	%
		V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

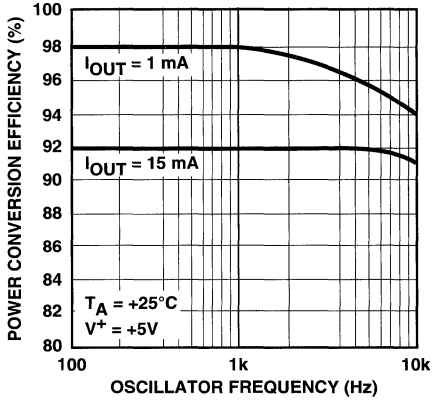
NOTES: 1. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC7660.
2. Derate linearly above 50°C by 5.5 mW/°C.
3. TC7660M only.
4. The TC7660 can be operated without the Dx diode over full temperature and voltage range.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 1)

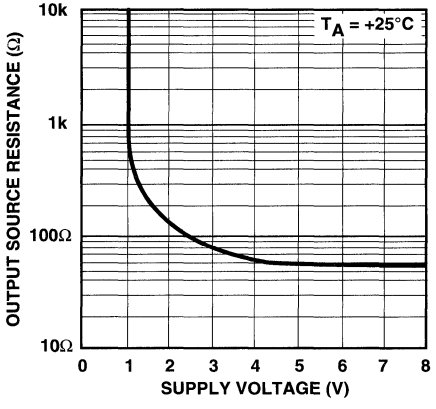
Operating Voltage vs Temperature



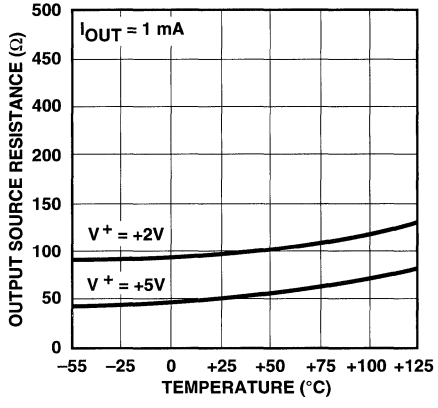
Power Conversion Eff vs Osc Freq



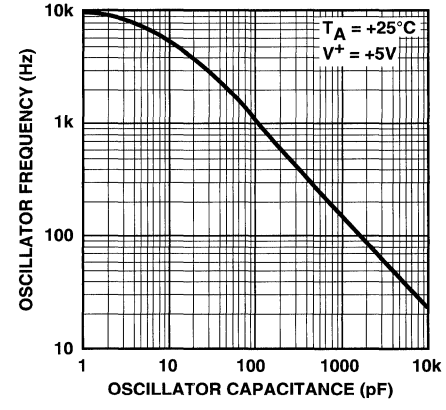
Output Source Resistance vs Supply Voltage



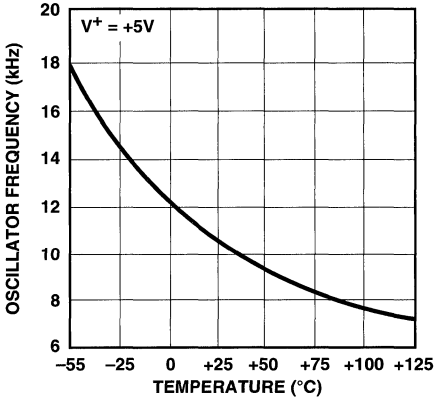
Output Source Resistance vs Temperature



Freq of Osc vs Ext Osc Capacitance

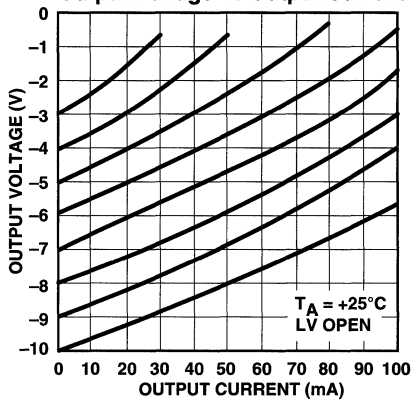


Unloaded Osc Freq vs Temperature

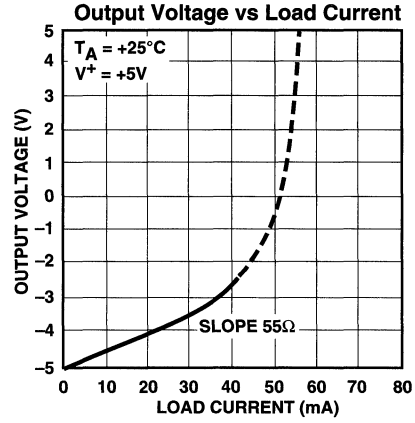


TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

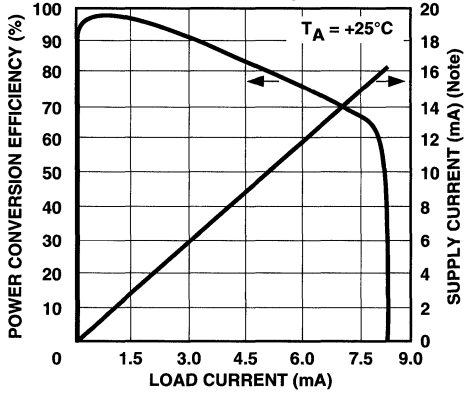
Output Voltage vs Output Current

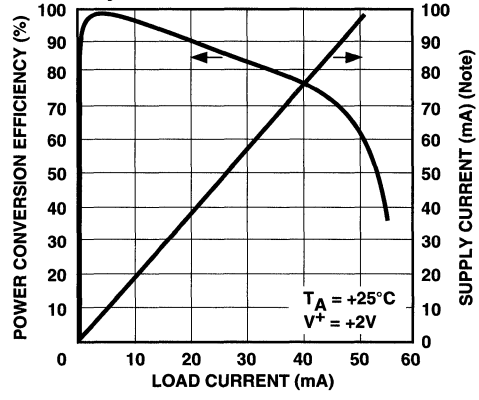


Output Voltage vs Load Current

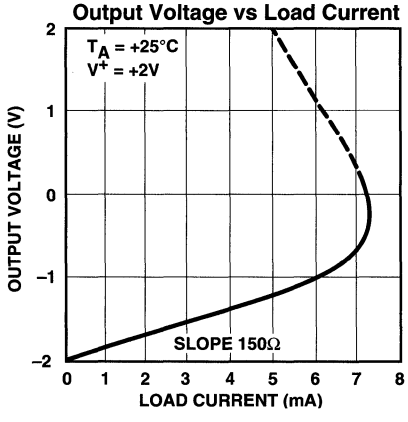


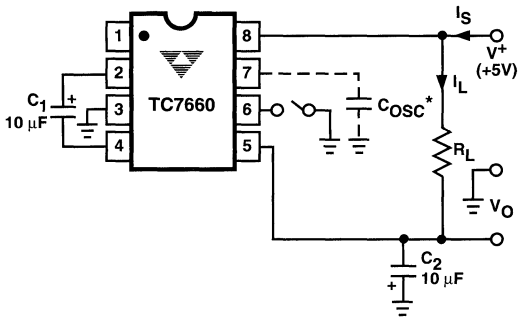
Supply Current and Power Conversion Efficiency vs Load Current





Output Voltage vs Load Current





NOTES: * For large values of C_{OSC} (>1000 pF), the values of C_1 and C_2 should be increased to 100 µF.

Figure 1. TC7660 Test Circuit

Circuit Description

The TC7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

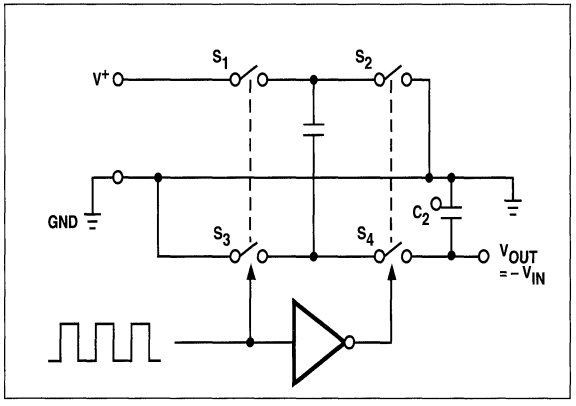


Figure 2. Idealized Switched Capacitor

The four switches in Figure 2 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TC7660 is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC7660 and the – terminal of C_2 must be connected to GND Pin 4.

Simple Negative Voltage Converter

Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of –10 mA and a supply voltage of +5V, the output voltage would be –4.3V.

The dynamic output impedance of the TC7660 is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f\ C_1} = 3.18\Omega,$$

where f = 10 kHz and C_1 = 10 µF.

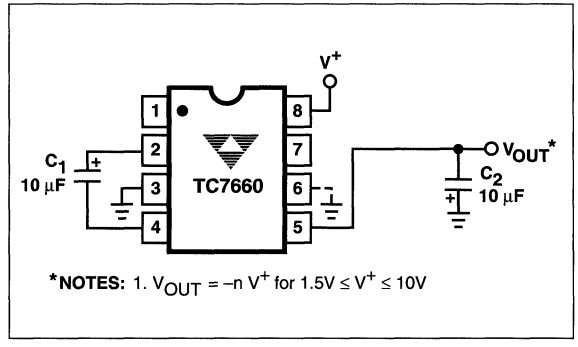


Figure 3. Simple Negative Converter

Paralleling Devices

Any number of TC7660 voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of TC7660})}{n\ (\text{number of devices})}$$

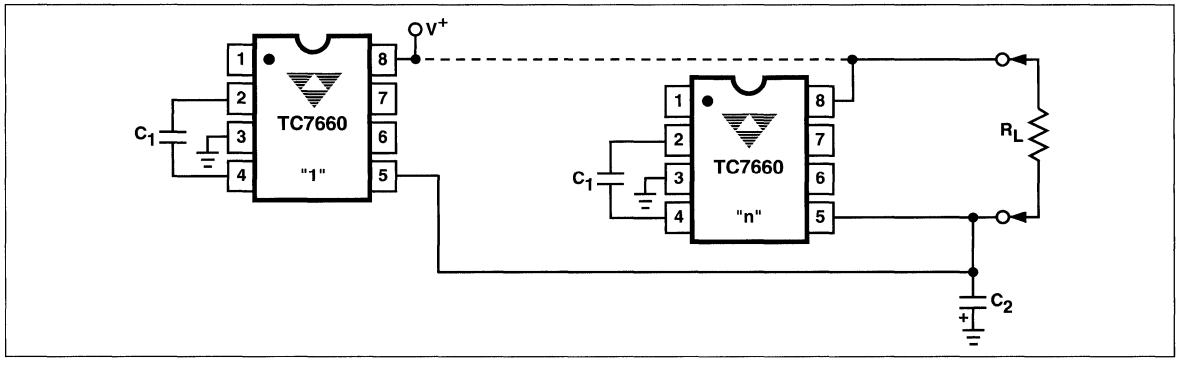


Figure 4. Paralleling Devices Lowers Output Impedance

Cascading Devices

The TC7660 may be cascaded as shown (Figure 6) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7660 R_{OUT} values.

Changing the TC7660 Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 6. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the TC7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 µF to 100 µF).

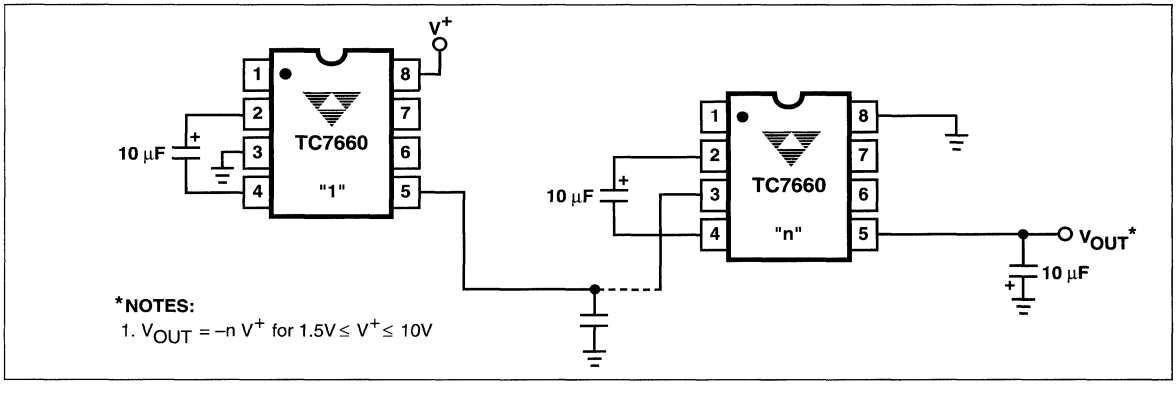


Figure 5. Increased Output Voltage by Cascading Devices

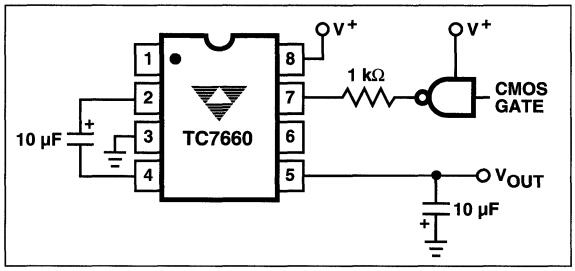


Figure 6. External Clocking

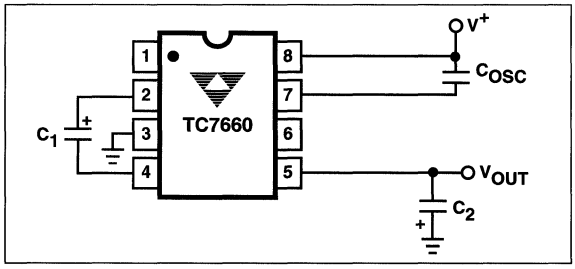


Figure 7. Lowering Oscillator Frequency

Positive Voltage Multiplication

The TC7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 8. In this application, the pump inverter switches of the TC7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2\,V^+) - (2\,V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

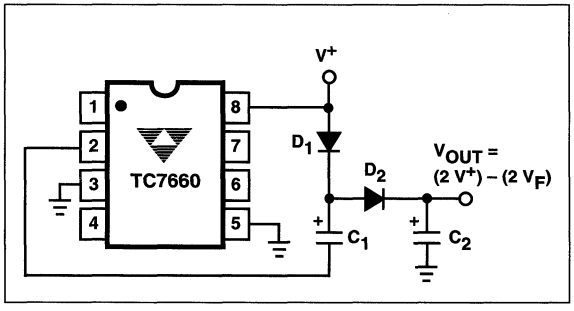


Figure 8. Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 9 combines the functions shown in Figures 3 and 8 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

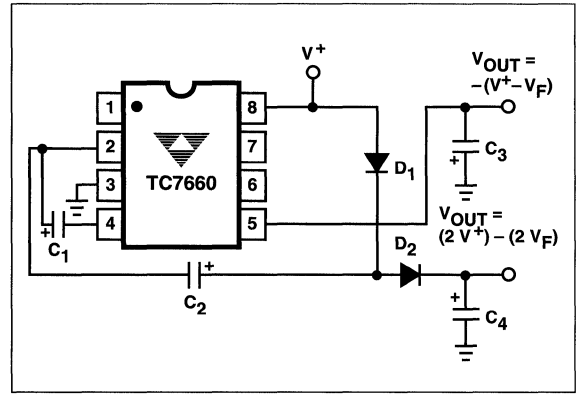


Figure 9. Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 10 shows a TC7660 transforming –5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 9, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 9 would never turn on), or else the diode and resistor shown dotted in Figure 10 can be used to "force" the internal regulator on.

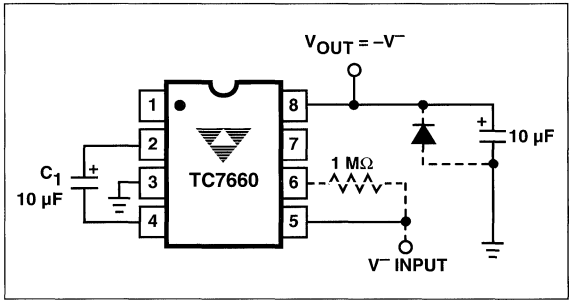


Figure 10. Positive Voltage Conversion

Voltage Splitting

The same bidirectional characteristics used in Figure 10 can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5, +15V can be converted (via +7.5V and –7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

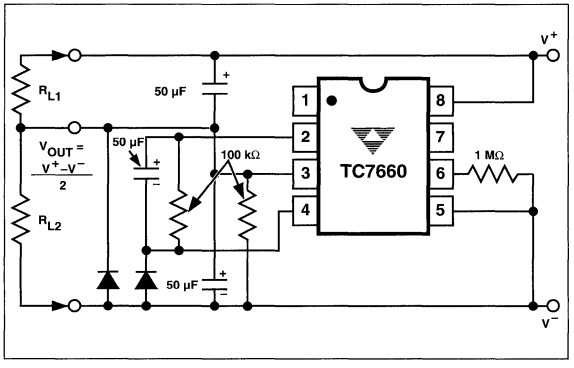


Figure 11. Splitting a Supply in Half

Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

Negative Supply Generation for 4-1/2 Digit Data Acquisition System

The TC7135 is a 4-1/2 digit ADC operating from ±5V supplies. The TC7660 provides an inexpensive –5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

3

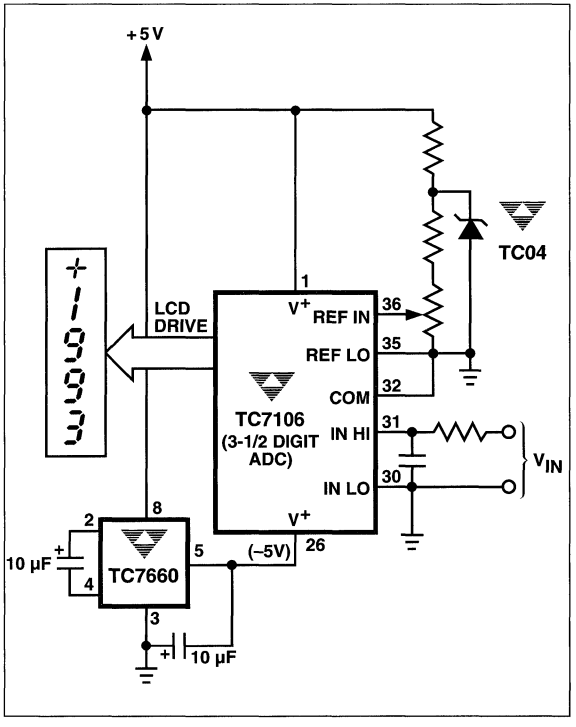


Figure 12a. Fixed Power Supply Operation of TC7106 ADC

TC7660

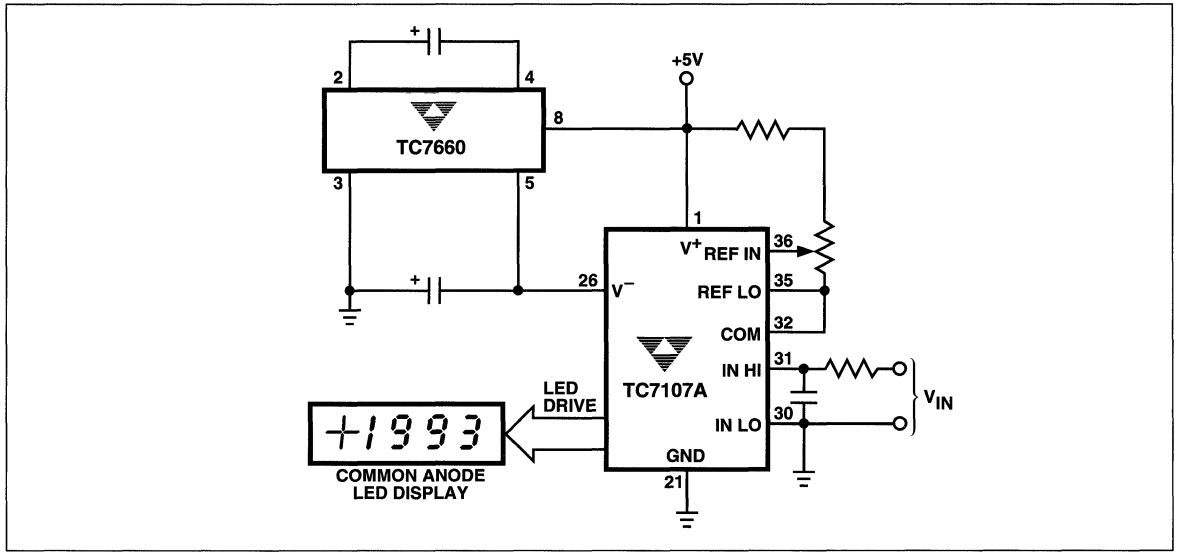


Figure 12b. Negative Power Supply Generation for TC7107A ADC

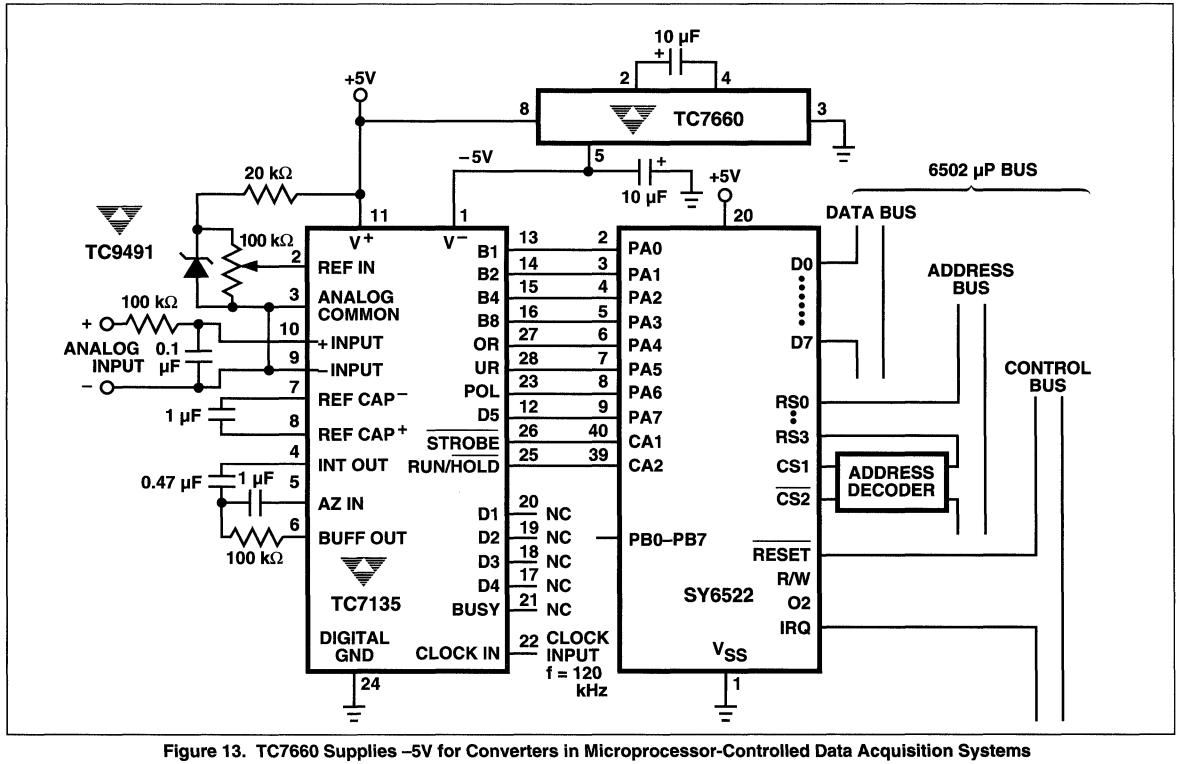


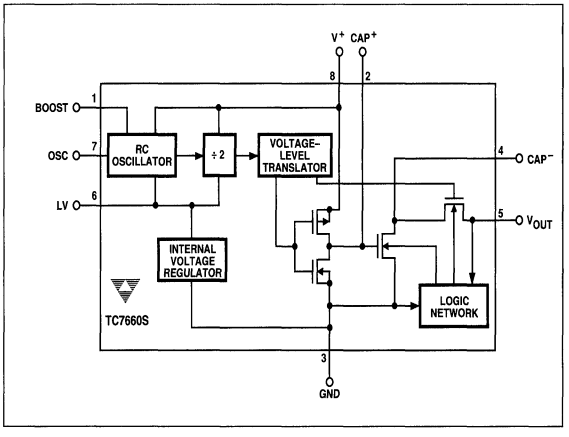
Figure 13. TC7660 Supplies –5V for Converters in Microprocessor-Controlled Data Acquisition Systems

SUPER VOLTAGE CONVERTER

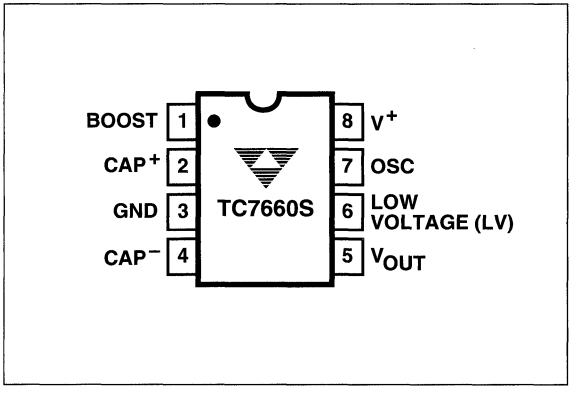
FEATURES

- **Oscillator boost from 10kHz to 45kHz**
- **Converts +5V Logic Supply to ±5V System**
- **Wide Input Voltage Range ..... 1.5V to 12V**
- **Efficient Voltage Conversion 99.9%**
- **Excellent Power Efficiency 98%**
- **Low Power Supply ..... 80 µA @ 5 V_{IN}**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **Available in Small Outline (SO) Package**
- **Improved ESD Protection ..... Up to 10KV**
- **No External Diode Required for High Voltage Operation**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (DIP and SO)



GENERAL DESCRIPTION

The TC7660S DC-to-DC voltage converter is the Super Voltage Converter version of TC7660. Added features include extended operating supply voltage range up to 12V, and frequency boost pin for higher operating frequency to lower output impedance with smaller capacitors.

The TC7660S can generate a negative voltage from a positive source. With two external capacitors, the TC7660S will convert a 1.5V to 12V input signal to a -1.5V to -12V level. The TC7660S easily generates -5V in +5V digital systems.

Many A/D converters, D/A converters, operational amplifiers, and multiplexers require negative supply voltages. The TC7660S allows +5V digital logic systems to incorporate these analog components without adding an additional main power source.

The TC7660S charges a capacitor to the applied supply voltage. Internal analog switches connect the capacitor across the output. Charge is transferred to an output storage capacitor completing the voltage conversion. Operation requires only two external capacitors for full supply voltage range.

The oscillator can be boosted from 10kHz to 45kHz. If operation below 10 kHz is desired, a capacitor may be added to osc pin 7 with boost pin 1 open. The oscillator may also be overdriven by an external clock.

The low voltage (LV) terminal (pin 6) may be tied to GND (pin 3) to bypass the internal series regulator and improve low voltage (LV) operation. At medium-to-high voltages (+3.5V to +12V), the LV pin is left floating to prevent device latch-up.

The TC7660S open-circuit output voltage is equal to the input voltage to within 0.1%. The TC7660S has a 98% power conversion efficiency for 2 mA to 5 mA load currents.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7660SCPA	8-Pin Plastic DIP	0°C to +70°C
TC7660SEJA	8-Pin CerDIP	– 40°C to +85°C
TC7660SEOA	8-Pin SO	– 40°C to +85°C
TC7660SEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7660SMJA	8-Pin CerDIP	– 55°C to +125°C
TC7660SCOA	8-Pin SO	0°C to +70°C

TC7660S

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +13V
LV, Boost, OSC Inputs
Voltage (Note 1) ..... – 0.3V to (V^++0.3V) for V^+ <5.5V
(V^+–5.5V) to (V^++0.3V) for V^+ >5.5V
Current Into LV (Note 1) ..... 20 µA for V^+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous

Power Dissipation (Note 2)
CerDIP ..... 500 mW
Plastic DIP ..... 375 mW
Operating Temperature Range
C Suffix ..... 0°C to +70°C
I Suffix ..... – 25°C to +85°C
E Suffix ..... – 40°C to +85°C
M Suffix ..... – 55°C to +125°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

Specifications Measured Over Operating Temperature Range With, $V^+ = 5V$, $C_{OSC} = 0$, Test Circuit (Figure 1), unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current (Boost pin OPEN or GND)	$R_L = \infty$, 25°C	—	80	160	µA
		0°C ≤ T_A ≤ +70°C			180	
		– 40°C ≤ T_A ≤ +85°C			180	
		– 55°C ≤ T_A ≤ +125°C			200	
I^+	Supply Current (Boost pin = V+)	0°C ≤ T_A ≤ +70°C	—	—	300	µA
		– 40°C ≤ T_A ≤ +85°C			350	
		– 55°C ≤ T_A ≤ +125°C			400	
V^+_H	Supply Voltage Range, High	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV Open	3	—	12	V
V^+_L	Supply Voltage Range, Low	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV to GND	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25°C	—	60	100	Ω
		I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C	—	70	120	Ω
		I_{OUT} = 20 mA, – 40°C ≤ T_A ≤ +85°C	—	70	120	Ω
		I_{OUT} = 20 mA, – 55°C ≤ T_A ≤ +125°C	—	105	150	Ω
		V^+ = 2V, I_{OUT} = 3 mA, LV to GND				
		0°C ≤ T_A ≤ +70°C	—	—	250	Ω
		– 55°C ≤ T_A ≤ +125°C	—	—	400	Ω
F_{OSC}	Oscillator Frequency	Pin 7 open; Pin 1 open or GND	—	10	—	kHz
		Pin 1 = V^+	—	45	—	kHz
P_{EFF}	Power Efficiency	R_L = 5 kΩ	96	98	—	%
		$T_{MIN} \leq T_A \leq T_{MAX}$	95	98	—	%
V_{OUT} E_{FF}	Voltage Conversion Efficiency	$R_L = \infty$	99	99.9	—	%
Z_{OSC}	Oscillator Impedance	V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

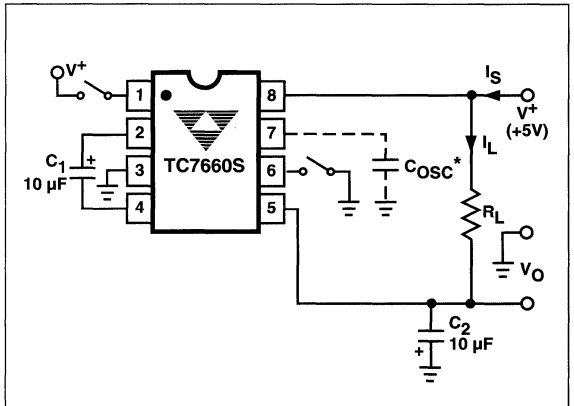
NOTES: 1. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC7660S.
2. Derate linearly above 50°C by 5.5 mW/°C.

Circuit Description

The TC7660S contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage V^+ for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 negatively by V+ volts. Charge is then tranferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The four switches in Figure 2 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.



NOTE: For large values of C_{OSC} (>1000 pF), the values of C_1 and C_2 should be increased to 100 µF.

Figure 1. TC7660S Test Circuit

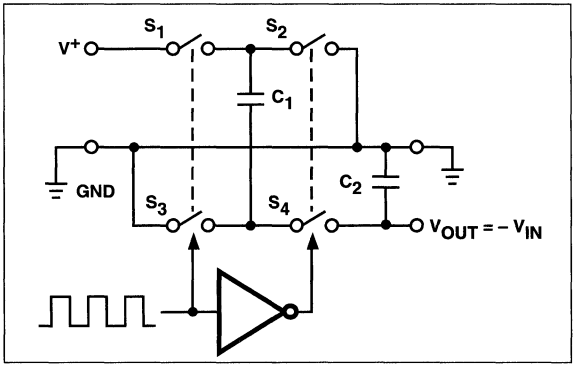


Figure 2. Idealized Switched Capacitor

The voltage regulator portion of the TC7660S is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7660S approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

TC7660S

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC7660S and the – terminal of C_2 must be connected to GND.

Simple Negative Voltage Converter

Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

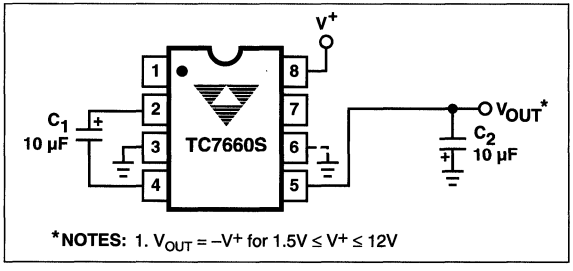


Figure 3. Simple Negative Converter

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of –10 mA and a supply voltage of +5V, the output voltage would be –4.3V.

The dynamic output impedance of the TC7660S is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f\, C_1} = 3.18\Omega,$$

where f = 10 kHz and C_1 = 10 µF.

Paralleling Devices

Any number of TC7660S voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\text{ (of TC7660S)}}{\text{n (number of devices)}}$$

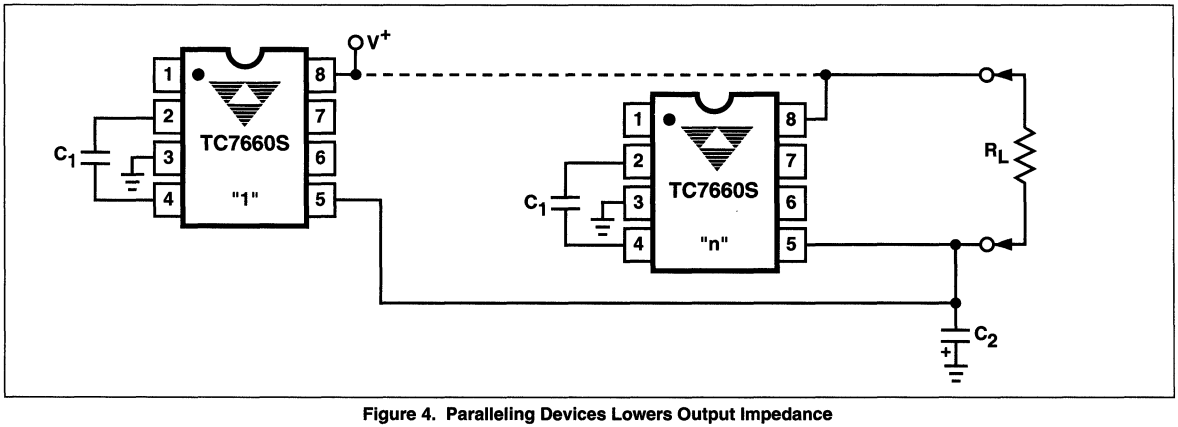


Figure 4. Paralleling Devices Lowers Output Impedance

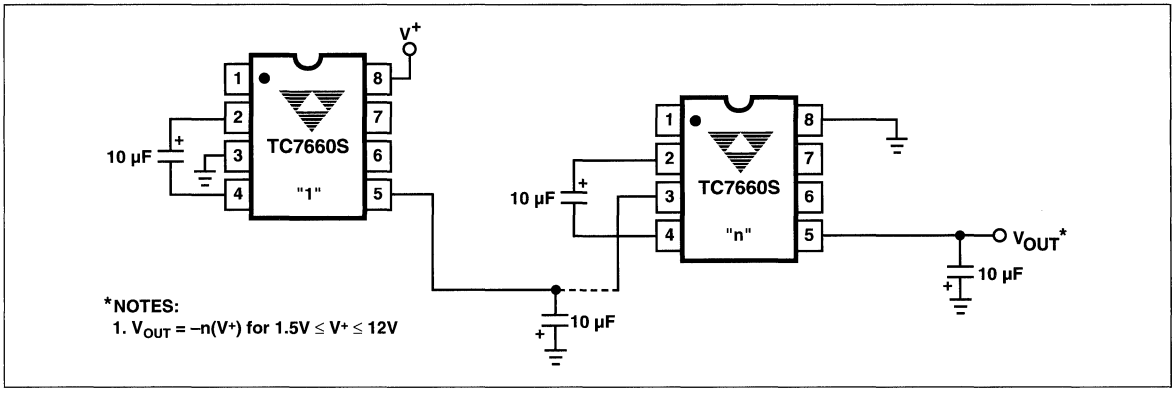


Figure 5. Increased Output Voltage by Cascading Devices

Cascading Devices

The TC7660S may be cascaded as shown (Figure 5) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7660S R_{OUT} values.

Changing the TC7660S Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, frequency boost pin may be connected to V+ to increase oscillator frequency to 45 kHz from a nominal of 10 kHz for an input supply voltage of 5.0 volts. The oscillator may also be synchronized to an external clock as shown in Figure 6. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

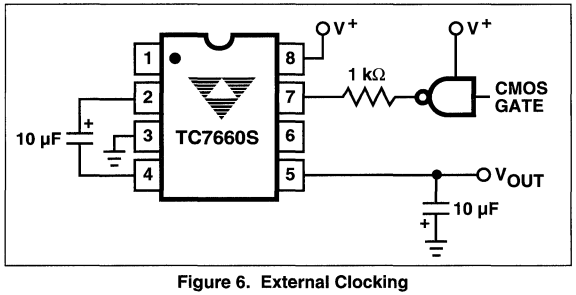


Figure 6. External Clocking

It is also possible to increase the conversion efficiency of the TC7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 µF to 100 µF).

Positive Voltage Multiplication

The TC7660S may be employed to achieve positive voltage multiplication using the circuit shown in Figure 8. In this application, the pump inverter switches of the TC7660S are used to charge C_1 to a voltage level of $V^+ – V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2\ V^+) – (2\ V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

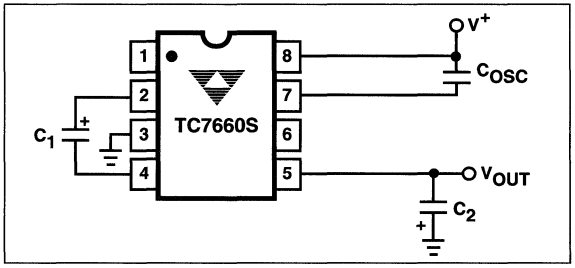


Figure 7. Lowering Oscillator Frequency

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 9 combines the functions shown in Figures 3 and 8 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 10 shows a TC7660S transforming –5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 9, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 9 would never turn on), or else the diode and resistor shown dotted in Figure 10 can be used to "force" the internal regulator on.

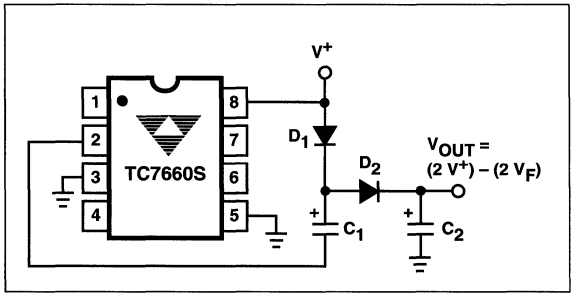


Figure 8. Positive Voltage Multiplier

Voltage Splitting

The same bidirectional characteristics used in Figure 10 can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5, +15V can be converted (via +7.5V and –7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

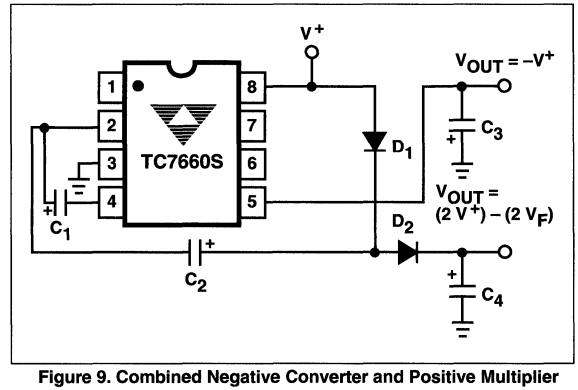


Figure 9. Combined Negative Converter and Positive Multiplier

Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

Negative Supply Generation for 4-1/2 Digit Data Acquisition System

The TC7135 is a 4-1/2 digit ADC operating from ±5V supplies. The TC7660S provides an inexpensive –5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

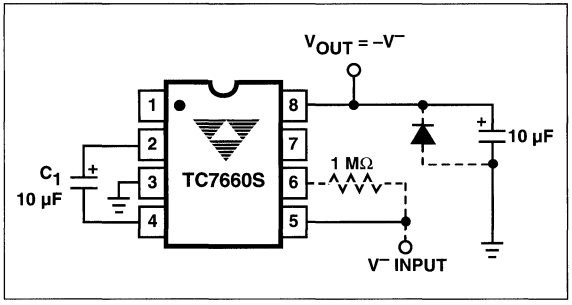


Figure 10. Positive Voltage Multiplier

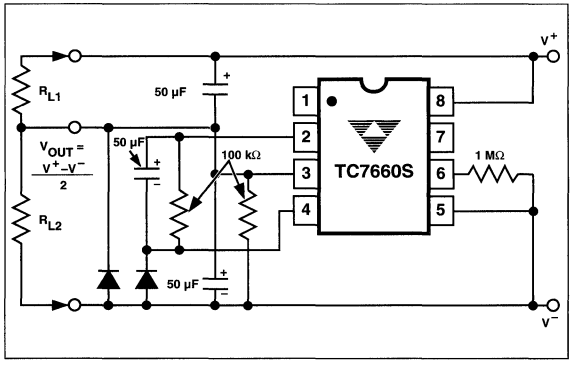


Figure 11. Splitting a Supply in Half

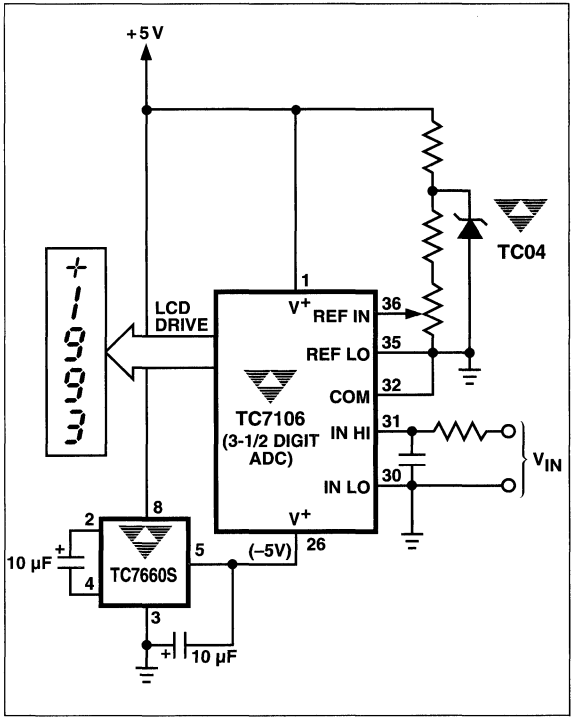


Figure 12a. Fixed Power Supply Operation of TC7106 ADC

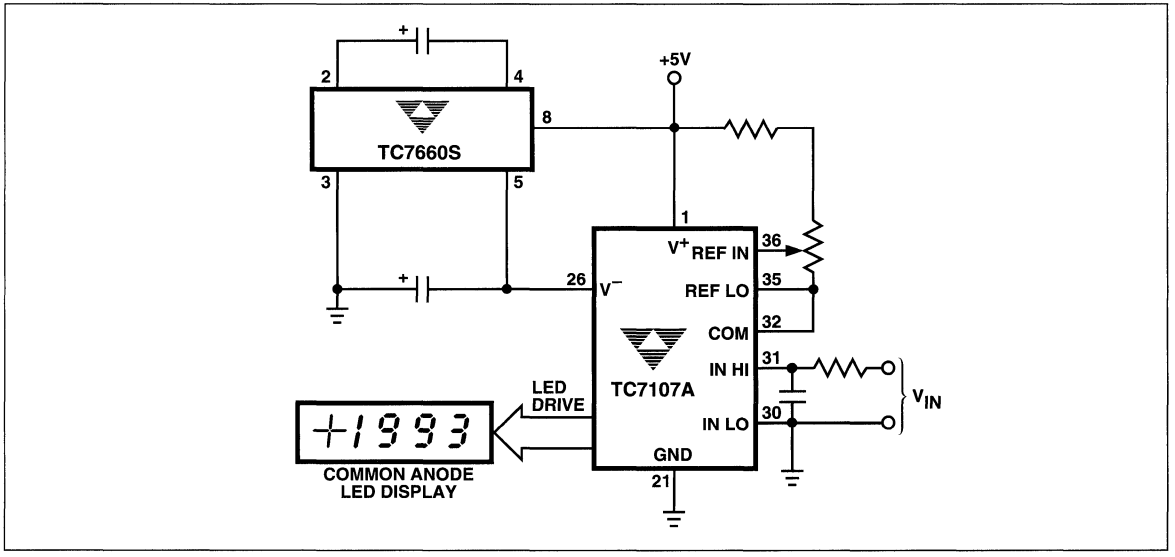


Figure 12b. Negative Power Supply Generation for TC7107A ADC

TC7660S

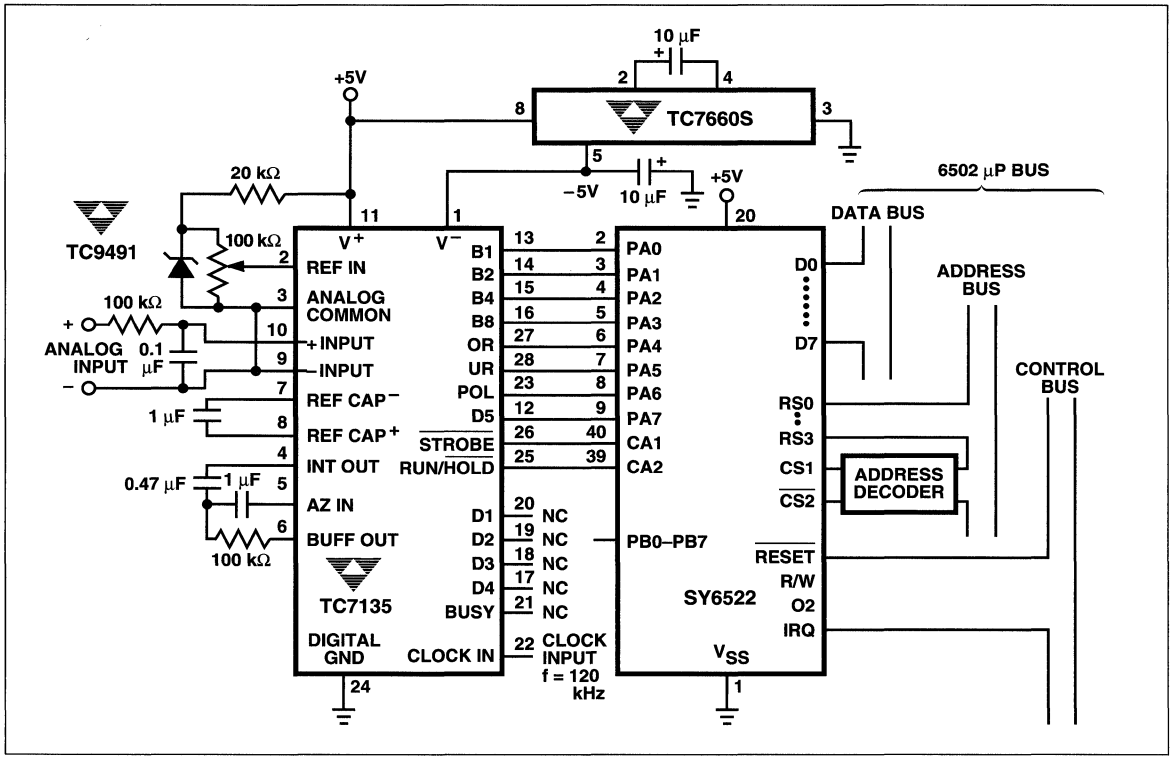
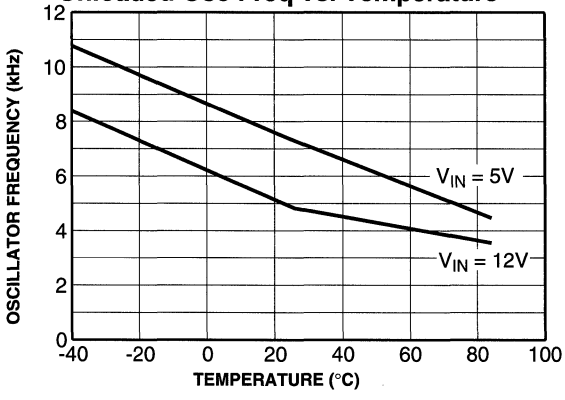


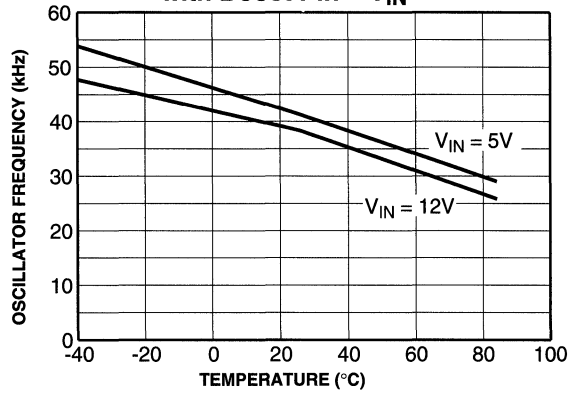
Figure 13. TC7660S Supplies –5V for Converters in Microprocessor-Controlled Data Acquisition Systems

TYPICAL CHARACTERISTICS

Unloaded Osc Freq vs. Temperature

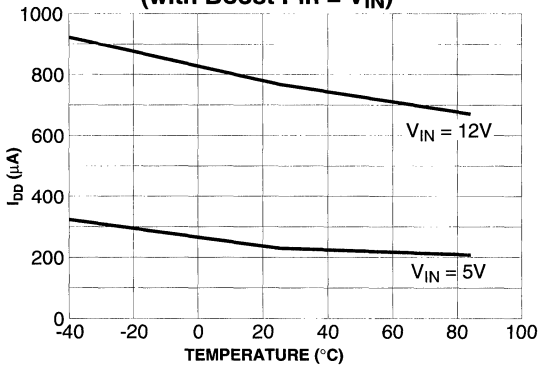


Unloaded Osc Freq vs. Temperature with Boost Pin = V_{IN}

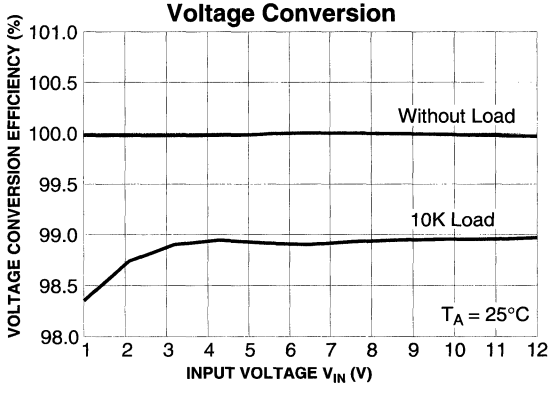


TYPICAL CHARACTERISTICS *(cont.)*

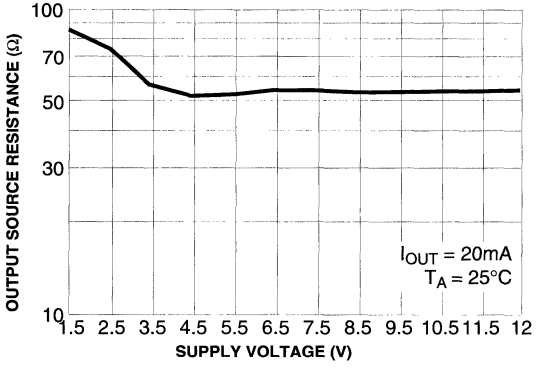
Supply Current vs. Temperature (with Boost Pin = V_{IN})



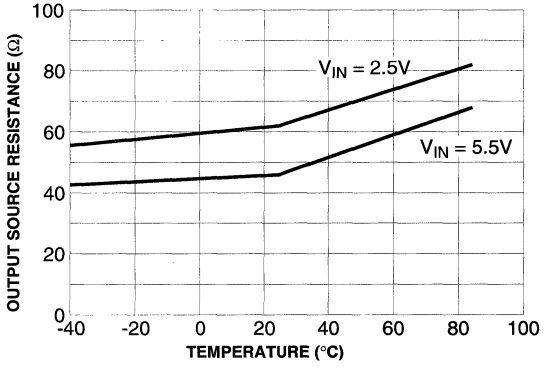
Voltage Conversion



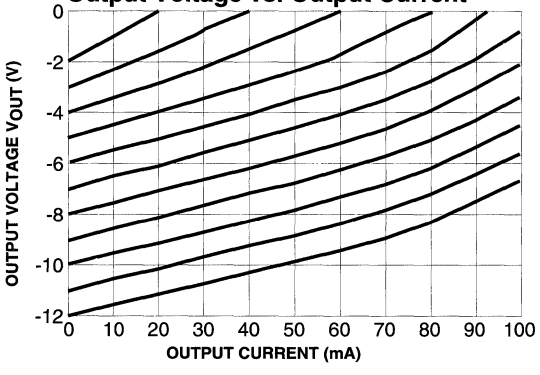
Output Source Resistance vs. Supply Voltage



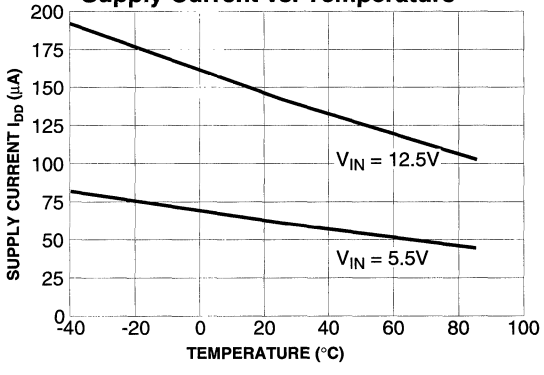
Output Source Resistance vs. Temperature



Output Voltage vs. Output Current



Supply Current vs. Temperature



DC-TO-DC CONVERTER

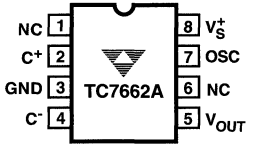
FEATURES

- **Wide Operating Range ..... 3V to 18V**
- **Increased Output Current ..... 40 mA**
- **Pin Compatible with ICL7662/SI7661/TC7660/ LTC1044**
- **No External Diodes Required**
- **Low Output Impedance @ I_L = 20 mA ..... 40Ω Typ**
- **No Low-Voltage Terminal Required**
- **CMOS Construction**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7662ACPA	8-Pin Plastic DIP	0°C to +70°C
TC7662AIJA	8-Pin CerDIP	– 25°C to +85°C
TC7662AEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7662AMJA	8-Pin CerDIP	– 55°C to +125°C

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

GENERAL DESCRIPTION

The TC7662A is an improved version of the industry-standard TC7660/TC7662 switched-capacitor DC-to-DC converters. CMOS construction and advanced design result in a device with twice the output power of the TC7662, but requires fewer parts in many applications.

The TC7662A can source 40 mA versus the TC7662's 20 mA capability. As an inverter, the TC7662A can output voltages as high as 18V and as low as 3V, without the need for external diodes. The output impedance of the device is a low 40Ω (typical), voltage conversion efficiency is 99.9%, and power conversion efficiency is 97%.

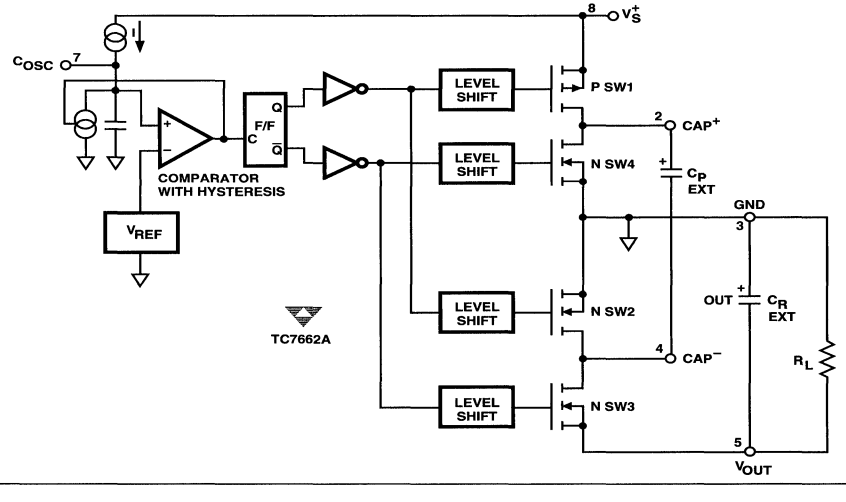
See TC962 if higher output current is required.

The low-voltage terminal (pin 6) required in some TC7662 applications has been eliminated. Only two external capacitors are required for inverter applications. If an external clock is needed to drive the TC7662A (such as when paralleling), driving pin 7 directly will cause the internal oscillator to sync to the external clock.

The TC7662A can be used in applications such as a DC-to-DC inverter, a doubler, a plus and minus supply splitter, and (when combined with other TC7662A's), as a voltage multiplier greater than two.

The TC7662A is compatible with the LTC1044, ICL7660, ICL7662, SI7661, and TC7660. It is recommended for designs requiring greater power and/or less input-to-output voltage drop.

FUNCTIONAL BLOCK DIAGRAM



TC7662A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+_S to GND ..... +18V
Input Voltage (Any Pin) ..... $(V^+_S + 0.3)$ to $(V^-_S - 0.3)$
Current Into Any Pin ..... 10 mA
Operating Temperature Range
- CPA ..... 0° to +70°C
- IJA ..... – 25°C to +85°C
- EPA ..... – 40°C to +85°C
- MJA ..... – 55°C to +125°C

Max Dissipation
- CPA, EPA ..... 375 mW
- IJA, MJA ..... 500 mW

Package Thermal Resistance
- CPA, EPA θ_{JA} ..... 140°C/W
- IJA, MJA θ_{JA} ..... 90°C/W

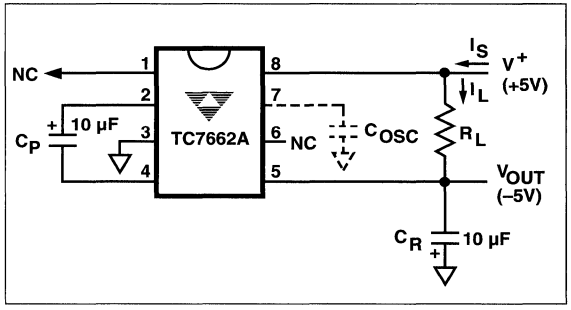
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
ESD Protection ..... ±2000V
Output Short Circuit ..... Continuous (at 5.5V Input)

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V^+_S = 15V, T_A = +25°C (See Test Circuit)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V^+_S	Supply Voltage		3	—	18	V
I_S	Supply Current	$R_L = \infty$				
	V^+_S = +15V	T_A = +25°C	—	510	700	µA
		$0 \le T_A \le +70°C$	—	560	—	µA
		$-55 \le T_A \le +125°C$	—	650	—	µA
	V^+_S = +5V	T_A = +25°C	—	190	—	µA
		$0 \le T_A \le +70°C$	—	210	—	µA
		$-55 \le T_A \le +125°C$	—	210	—	µA
R_O	Output Source Resistance	I_L = 20 mA, V^+_S = +15V	—	40	50	Ω
		I_L = 40 mA, V^+_S = +15V	—	50	60	Ω
		I_L = 3 mA, V^+_S = +5V	—	100	125	Ω
C_{OSC}	Oscillator Frequency		—	12	—	kHz
P_{EFF}	Power Efficiency	V^+_S = +15V R_L = 2 kΩ	93	97	—	%
V_{EFF}	Voltage Efficiency	V^+_S = +15V $R_L = \infty$	99	99.9	—	%
		Over Temperature Range	96	—	—	%

TEST CIRCUIT



APPLICATIONS INFORMATION

Theory of Operation

The TC7662A is a capacitive charge pump (sometimes called a switched-capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional diagram (page 1) shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C1 to the supply voltage, V_S^+. This assumes that the ON resistance of the MOSFETs in series with the capacitor produce a charging time (3 time constants) less than the ON time provided by the oscillator frequency, as shown:

$$3\,(R_{DS(ON)}\,C1) < C1/(0.5\,f_{OSC}).$$

In the next cycle, SW1 and SW2 are turned OFF and, after a very short interval with all switches OFF (preventing large currents from occurring due to cross conduction), SW3 and SW4 are turned ON. The charge in C1 is then transferred to C_{OUT}, BUT WITH THE POLARITY INVERTED. In this way, a negative voltage is derived.

An oscillator supplies pulses to a flip-flop that is fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has a pin that controls the frequency of oscillation. Pin 7 can have a capacitor added that is connected to ground. This will lower the frequency of the oscillator by adding capacitance to the internal timing capacitor of the TC7662A. (See Oscillator Frequency vs. C_{EXT}, page 5.)

Capacitors

In early charge pump converters, capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this, let's look at a model of a typical electrolytic capacitor (Figure 1).

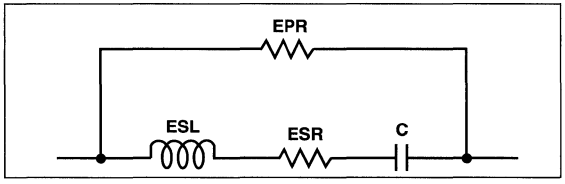


Figure 1 Capacitor Equivalent Circuit

Note one of its characteristics is ESR (equivalent series resistance). This parasitic resistance winds up in series with the load. Thus, both voltage and power conversion efficiency are compromised if a low ESR capacitor is not used.

For example, in the "Test Circuit", changing C_P and C_R capacitors from typical ESR to low ESR types, the effective converter output impedance changed from 45Ω to 40Ω, an improvement of 12%.

This applies to all types of capacitors, including film types (polyester, polycarbonate etc.).

Some applications information suggests that the capacitor is not critical and attributes the limiting factor to the capacitor's reactance value. Let's examine this:

$$X_C = \frac{1}{2\pi f\,C} \quad \text{and} \quad Z_C = \frac{X_C}{DS},$$

where DS (duty cycle) = 50%.

Thus, $Z_C \approx 1.33\Omega$ at f = 12 kHz, where C = 10 µF.

For the TC7662A, f = 12,000 Hz, and a typical value of C would be 10 µF. This is a reactive impedance of ≈1.33Ω. If the ESR is as great as 5Ω, the reactive value is not as critical as it would first appear, since the ESR would dominate. The 5Ω value is typical of a general-purpose electrolytic capacitor.

Synchronizing

The TC7662A may be synchronized by connecting pin 7 of the TC7662A through a 100k resistor in series with a diode to a negative-going pulse source. The negative pulse voltage can be +5V with a 5 microsecond duration going negative to 0V.

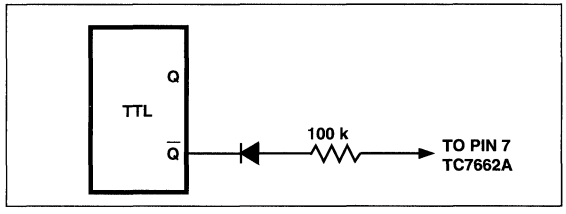
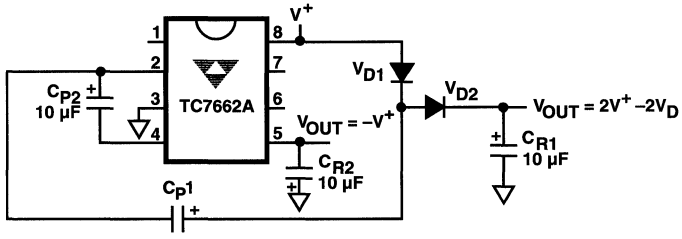


Figure 2 Synchronization

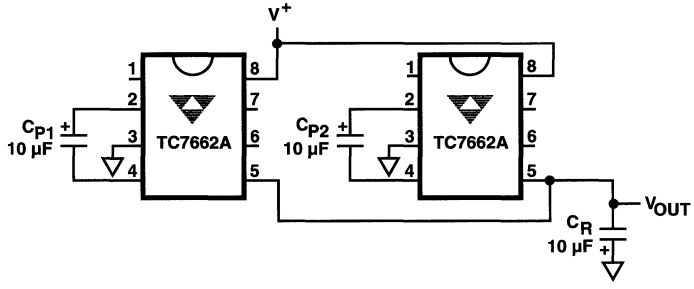
TC7662A

TYPICAL APPLICATIONS

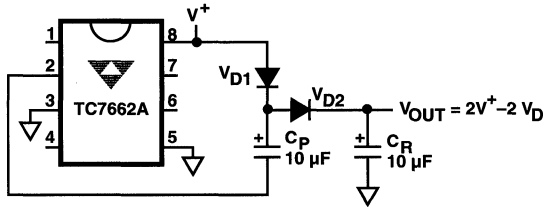
Combined Negative Converter and Positive Multiplier



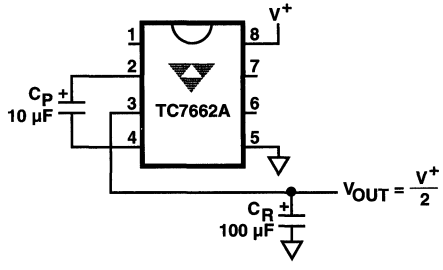
Lowering Output Resistance by Paralleling Devices



Positive Voltage Multiplier

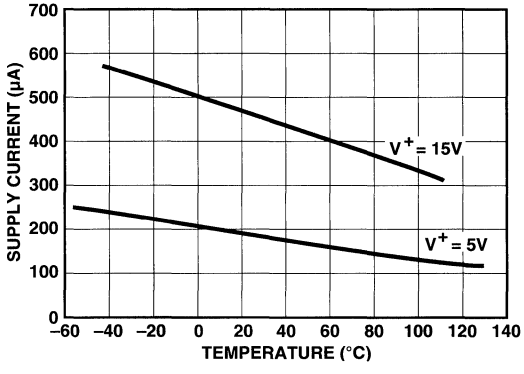


Split V^+ In Half

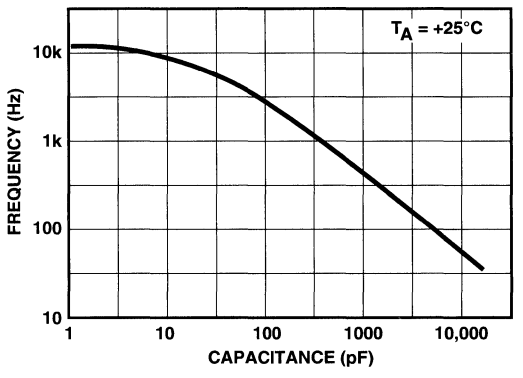


TYPICAL CHARACTERISTICS CURVES

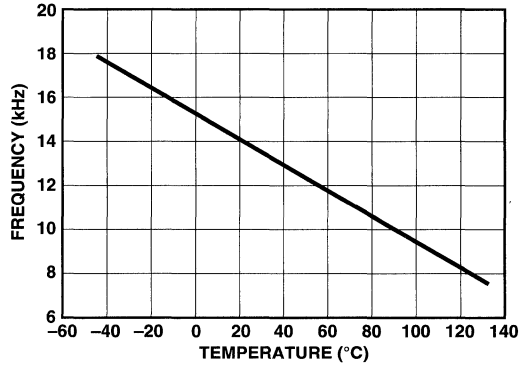
Supply Current vs Temperature



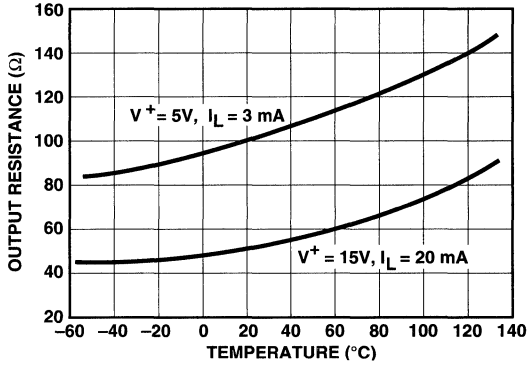
Oscillator Frequency vs C_{EXT}



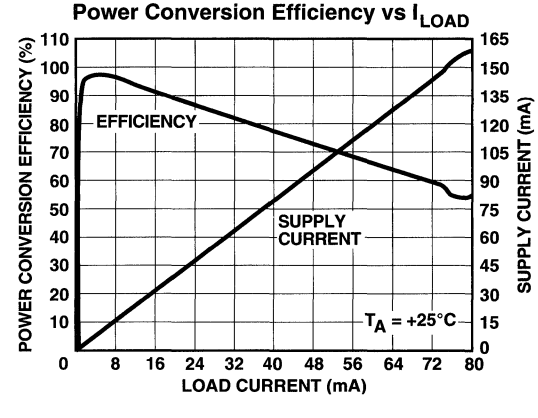
Frequency vs Temperature



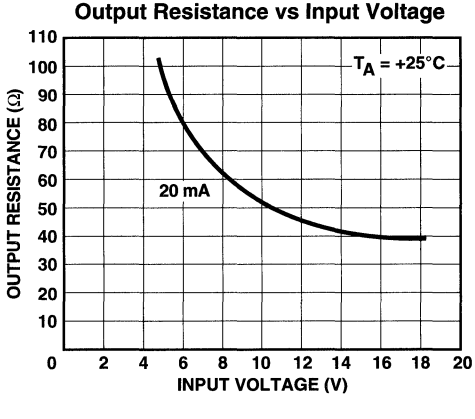
Output Resistance vs Temperature



Power Conversion Efficiency vs I_{LOAD}



Output Resistance vs Input Voltage



DC-TO-DC VOLTAGE CONVERTER

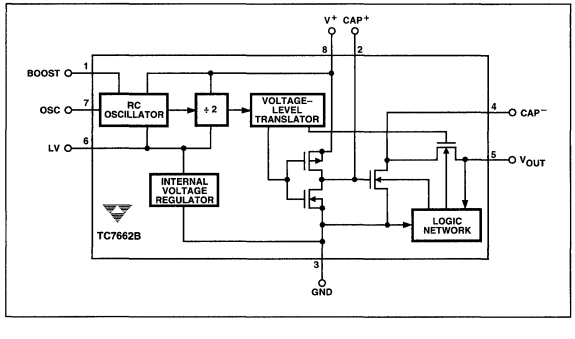
FEATURES

- **Guaranteed Lower Max Supply Current for All Temperature Ranges**
- **Guaranteed Wider Operating Voltage Range 1.5V to 15V**
- **No External Diode Over Full Temperature and Voltage Range**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- **Guaranteed Minimum Power Efficiency is 96%**
- **Improved SCR Latchup Protection**
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$**
- **Easy to Use – Requires Only 2 External Non-Critical Passive Components**
- **Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices**
- **ESD Protection ..... up to 10kV**

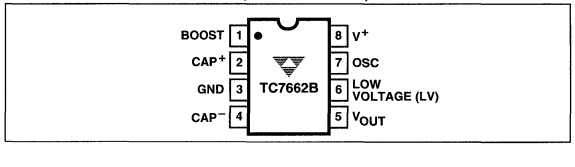
APPLICATIONS

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems and Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter, $V_{OUT} = \pm V_S/2$**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (DIP and SO)



GENERAL DESCRIPTION

The TC7662B DC-to-DC Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry standard ICL7660 offering an ***extended*** operating supply voltage range up to 15V, with ***lower*** supply current. ***No external diode*** is needed for the TC7662B. In addition, a ***Frequency Boost pin*** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

The TC7662B performs supply voltage conversion from positive to negative for an input range of 1.5V to 15V, resulting in complementary output voltages of - 1.5V to - 15V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The TC7662B can be connected to function as a voltage doubler and will generate up to 28.5V with 15V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock. In addition, pin 1 may be tied to V^+, automatically raising the OSC frequency above 35 kHz.

The "LV" terminal may be tied to GND to bypass the internal series regulator and to improve low voltage (LV) operation. At medium to high voltages (3.5V to 15V), the LV pin is left floating to prevent device latchup.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7662BCPA	8-Pin Plastic DIP	0°C to +70°C
TC7662BEOA	8-Pin SO	– 40°C to +85°C
TC7662BEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7662BCOA	8-Pin SO	0°C to +70°C

TC7662B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +16.5V
LV, Boost and OSC Inputs Voltage (Note 1)
V+<5.5V ..... – 0.3V to (V+ + 0.3V)
>5.5V ..... (V+ – 5.5V) to (V+ + 0.3V)
Current Into LV (Note 1)
V+ >3.5V ..... 20 µA
Output Short Duration
(V_{SUPPLY} ≤ 5.5V) ..... Continuous
Power Dissipation (Note 2)
Plastic DIP ..... 375 mW
SO ..... 300 mW

Operating Temperature Range
C Suffix ..... 0°C to +70°C
E Suffix ..... – 40°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

V^+ = 5V, T_A = +25°C, OSC = Free running, Test Circuit Figure 2, Unless Otherwise Specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current (Note 3) (Boost pin OPEN OR GND)	R_L = ∞, +25°C	—	80	160	µA
		0°C ≤ T_A ≤ +70°C	—	—	180	µA
		– 40°C ≤ T_A ≤ +85°C	—	—	180	µA
		– 55°C ≤T_A ≤ +125°C	—	—	200	µA
I^+	Supply Current (Boost pin = V+)	0°C ≤ T_A ≤ +70°C – 40°C ≤ T_A ≤ +85°C – 55°C ≤ T_A ≤ +125°C	—	—	300 350 400	µA
V^+_H	Supply Voltage Range, High (Note 4)	R_L = 10 kΩ, LV Open, T_{MIN} ≤ T_A ≤ T_{MAX}	3.0	—	15	V
V^+_L	Supply Voltage Range, Low	R_L = 10 kΩ, LV to GND, T_{MIN} ≤ T_A ≤ T_{MAX}	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C	—	65	100	Ω
		I_{OUT} = 20 mA, – 40°C ≤ T_A ≤ +85°C	—	—	120	Ω
		I_{OUT} = 20 mA, - 55°C ≤ T_A ≤ +125°C	—	—	150	Ω
		I_{OUT} = 3 mA, V^+ = 2V, LV to GND , 0°C ≤ T_A ≤ +70°C	—	—	250	Ω
		I_{OUT} = 3 mA, V^+ = 2V, LV to GND , – 40°C ≤ T_A ≤ +85°C	—	—	300	Ω
		I_{OUT} = 3 mA, V^+ = 2V, LV to GND , – 55°C ≤ T_A ≤ +125°C	—	—	400	Ω
f_{OSC}	Oscillator Frequency	C_{OSC} = 0, Pin 1 Open or GND Pin 1 = V+	5	10 35	—	kHz
P_{Eff}	Power Efficiency	R_L = 5 kΩ T_{MIN} ≤ T_A ≤ T_{MAX}	96 95	96 97	—	%
$V_{OUT}Eff$	Voltage Conversion Efficiency	R_L = ∞	99	99.9	—	%
Z_{OSC}	Oscillator Impedance	V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

NOTES:

1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC7662B.
2. Derate linearly above 50°C by 5.5 mW/°C.
3. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
4. The TC7662B can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

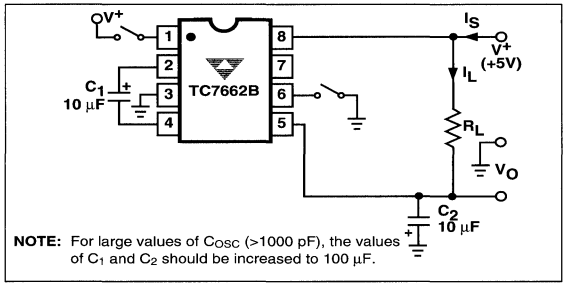
DETAILED DESCRIPTION

The TC7662B contains all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors which may be inexpensive 1μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage V+ for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The TC7662B approaches this ideal situation more closely than existing non-mechanical circuits.

In the TC7662B, the four switches of Figure 2 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

The problem is eliminated in the TC7662B by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TC7662B is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation, the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 volts, the LV terminal must be left open to insure latchup proof operation and prevent device damage.



NOTE: For large values of C_{OSC} (>1000 pF), the values of C_1 and C_2 should be increased to 100 μF.

Figure 1. TC7662B Test Circuit

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7662B approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Dos and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect the LV terminal to GND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for voltages above 5.5 volts for extended periods; however, transient conditions including start-up are okay.

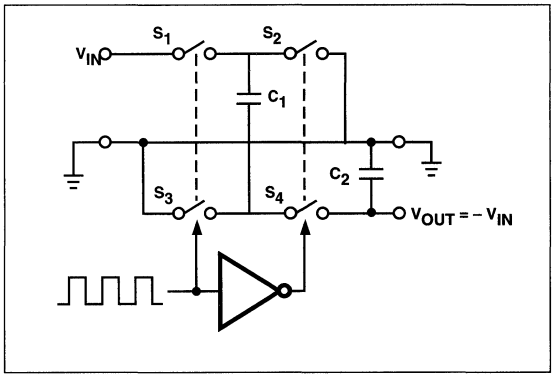


Figure 2. Idealized Negative Voltage Capacitor

4. When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC7662B and the – terminal of C_2 must be connected to GND.
5. If the voltage supply driving the TC7662B has a large source impedance (25-30 ohms), then a 2.2µF capacitor from pin 8 to ground may be required to limit the rate of rise of the input voltage to less than 2V/µs.

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the TC7662B for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply where a positive supply of +1.5V to +15V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

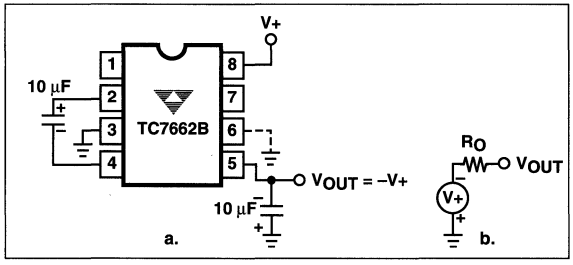


Figure 3. Simple Negative Converter and its Output Equivalent

The output characteristics of the circuit in Figure 3 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 3b. The voltage source has a value of–(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, \; R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2}\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when $C_1 >$ 10µF and there is not enough time to fully charge the capacitors every cycle. In a typical application when f_{OSC} = 10kHz and $C = C_1 = C_2 = 10\mu F$:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_O \cong (46 + 20 + 5 \times ESR_C)\,\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x ESR_{C2} volts. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current to the load. The drop at B is $I_{OUT} \times t_2/C_2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_2} + ESR_{C2} \times I_{OUT}\right)$$

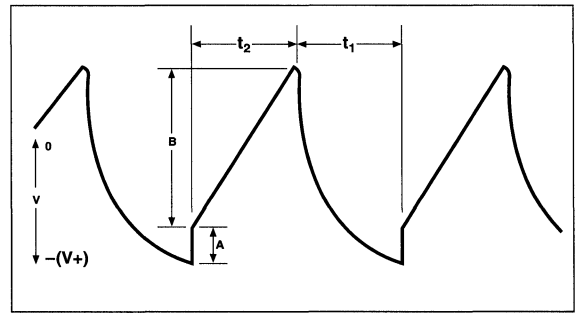


Figure 4. Output Ripple

Paralleling Devices

Any number of TC7662B voltage converters may be paralleled to reduce output resistance (Figure 5). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of TC7662B)}}{\text{n (number of devices)}}$$

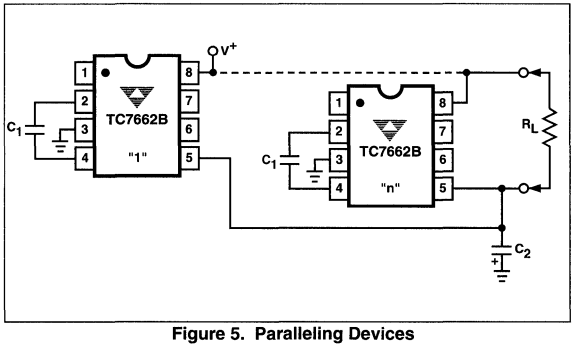


Figure 5. Paralleling Devices

Cascading Devices

The TC7662B may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7662B R_{OUT} values.

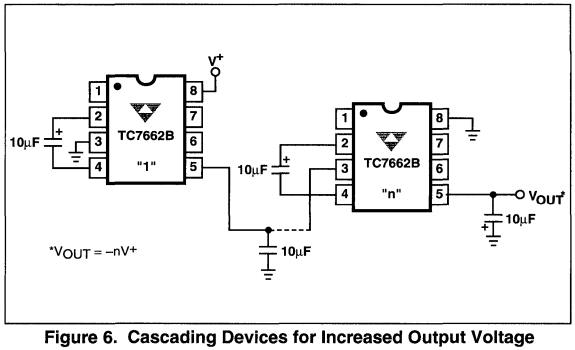


Figure 6. Cascading Devices for Increased Output Voltage

Changing the TC7662B Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by one of several methods described below:

By connecting the Boost Pin (Pin 1) to V+, the oscillator charge and discharge current is increased and, hence the oscillator frequency is increased by approximately 3 1/2 times. The result is a decrease in the output impedance and ripple. This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, e.g., 0.1µF, can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 1\mu F$ or 10µF. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock as shown in Figure 7. In order to prevent device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

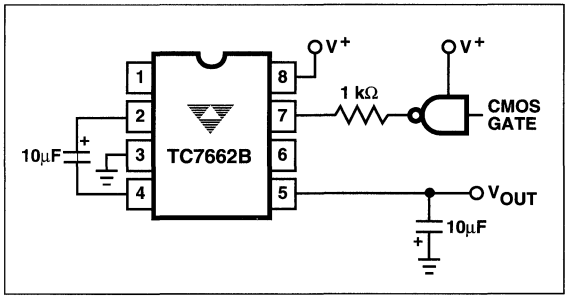


Figure 7. External Clocking

It is also possible to increase the conversion efficiency of the TC7662B at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

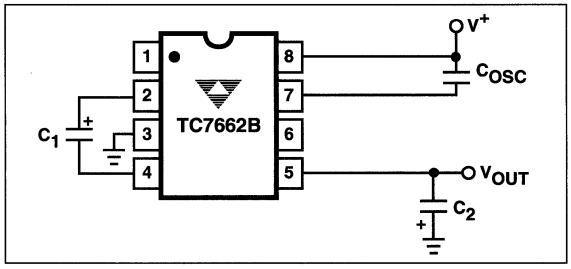


Figure 8. Lowering Oscillator Frequency

Positive Voltage Doubling

The TC7662B may be employed to achieve positive voltage doubling using the circuit shown in Figure 9. In this application, the pump inverter switches of the TC7662B are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage on C_1 plus the supply voltage (V+) applied through diode D_2 to capacitor C_2). The voltage thus created on C_2 becomes $(2\ V^+) - (2\ V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

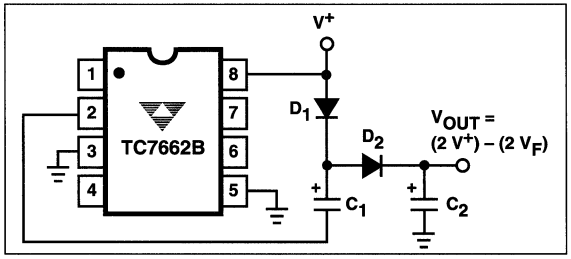


Figure 9. Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 3 and 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

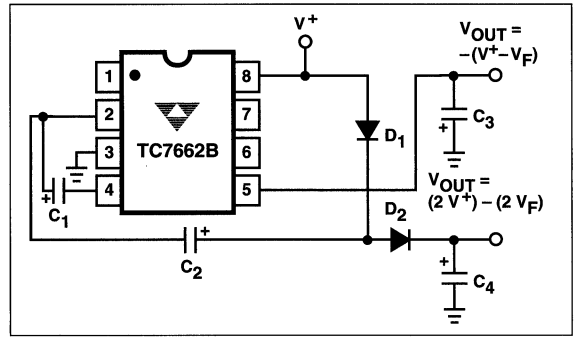


Figure 10. Combined Negative Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15V can be converted (via +7.5V and –7.5V) to a nominal – 15V, though with rather high series resistance (~250Ω).

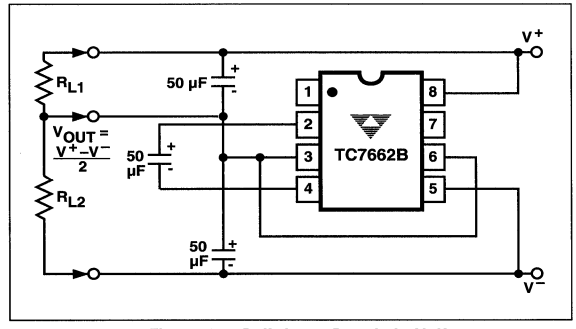


Figure 11. Splitting a Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the TC7662B can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is advisable, since the TC7662B's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the TC7662B, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provide an output impedance of less than 5Ω to a load of 10mA.

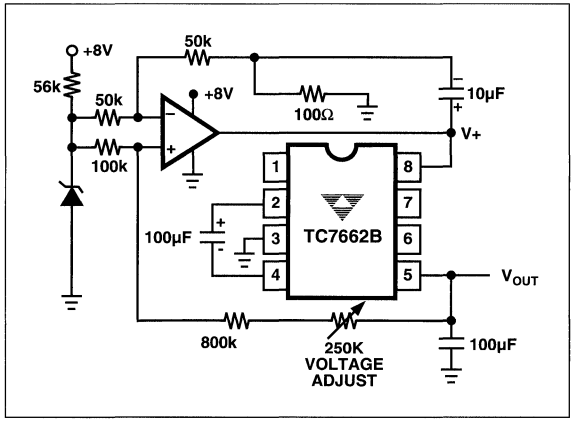


Figure 12. Regulating the Output Voltage

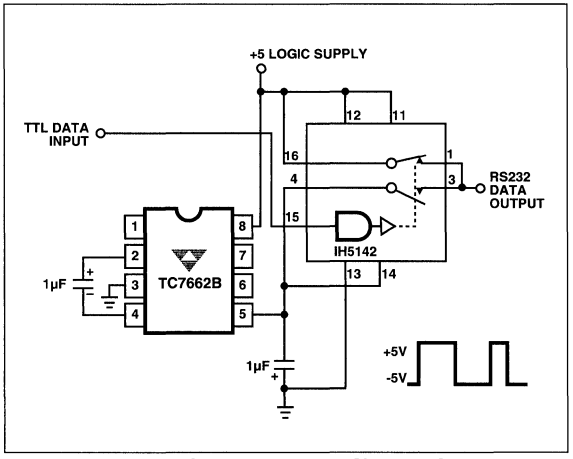


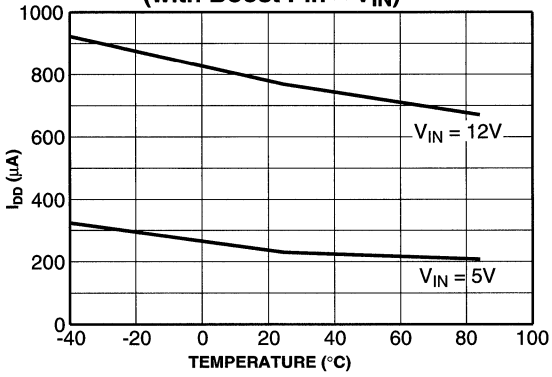
Figure 13. RS232 Levels from a Single 5V Supply

3

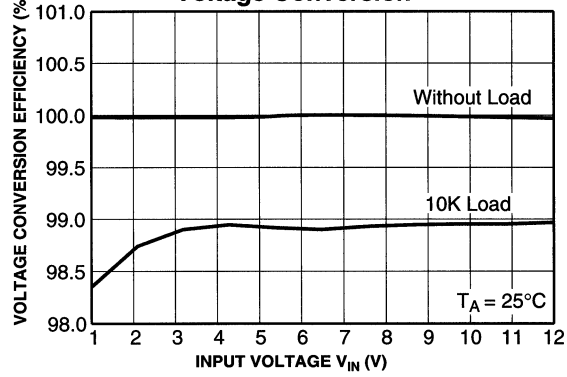
TC7662B

TYPICAL CHARACTERISTICS

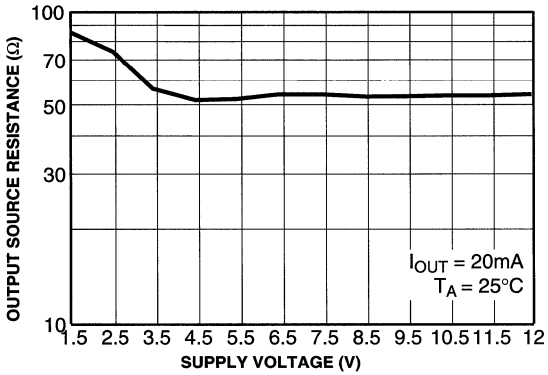
Supply Current vs. Temperature (with Boost Pin = V_{IN})



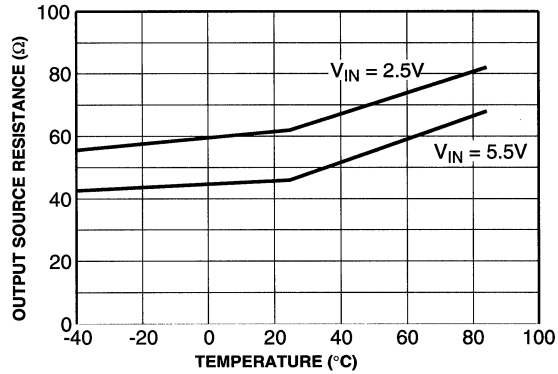
Voltage Conversion



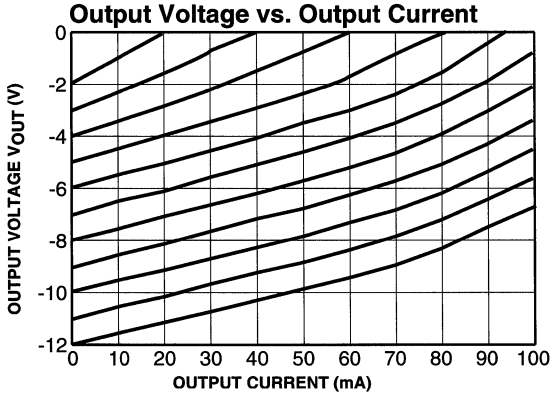
Output Source Resistance vs. Supply Voltage



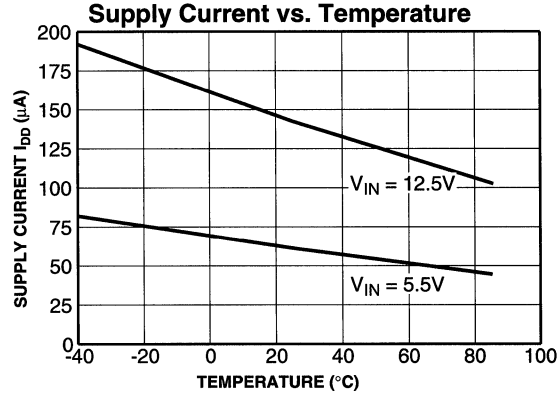
Output Source Resistance vs. Temperature



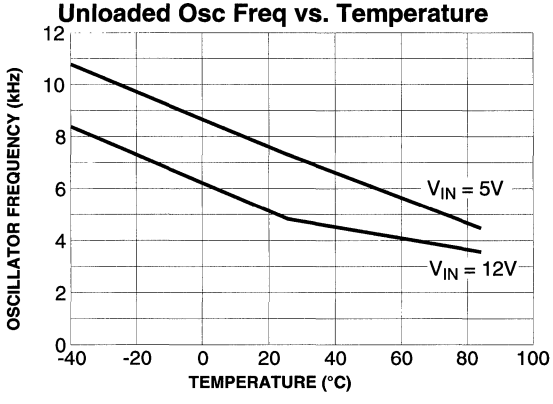
Output Voltage vs. Output Current

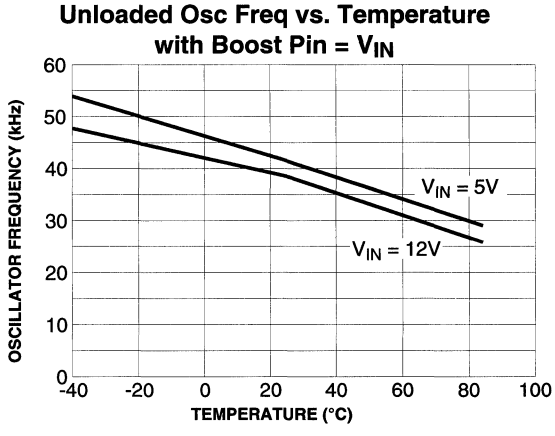


Supply Current vs. Temperature



TYPICAL CHARACTERISTICS *(cont.)*





3

VOLTAGE DETECTOR

FEATURES

- Precise Detection Thresholds ..... Standard ±2.5%
- Small Packages ..... SMT: SOT-23-5
  SMT: SOT-89-3
  Thru-hole: TO-92
- Low Current Drain ..... Typ. 1µA
- Voltage Detection Range ..... 0.9V to 6.0V
- Operating Voltage Range ..... 0.7V to 10.0V

APPLICATIONS

- Microprocessor Reset
- Battery Status Indicator
- Level Discriminator
- Power-failure Detector
- Switching Circuit in Battery Backup
- Waveform Shaping Circuit

GENERAL DESCRIPTION

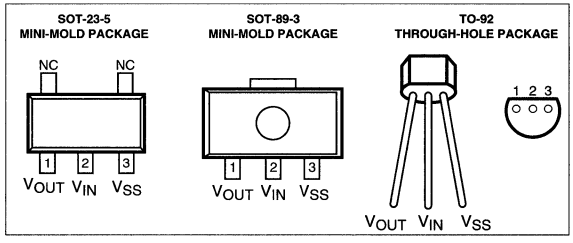
The TC44 Series are CMOS voltage detectors, suited especially for battery-powered applications because of their extremely low 1 µA operating current and small surface-mount packaging. Each part is laser trimmed to the desired threshold voltage which can be ordered in the range of 0.9V to 6.0V, in 0.1V steps.

The design includes a comparator, low-current high-precision reference, laser-trimmed divider, hysteresis circuit and output driver. The latter is available in either an open-drain or complementary ("CMOS") configuration.

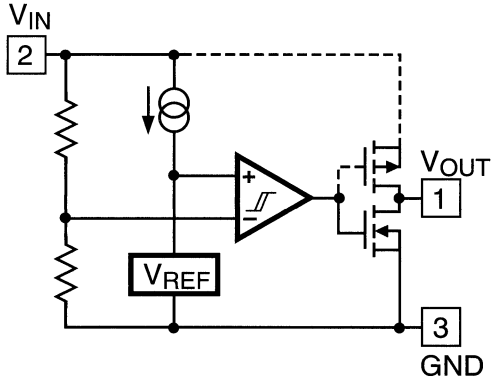
In operation, the TC44 output (V_{OUT}) remains in the logic HIGH state as long as V_{IN} is greater than the specified threshold voltage ($-V_{DET}$). When VIN falls below $-V_{DET}$, the output is driven to a logic LOW. V_{OUT} remains LOW until V_{IN} rises above $-V_{DET}$ by an amount Vhyst, whereupon it resets to a logic HIGH.

3

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



Open-drain version (N) has only an N-channel output transistor. [Ordering code N.]

Complementary ("CMOS") version includes a P-channel output transistor (dotted lines). [Ordering code C.]

ORDERING INFORMATION

PART CODE TC44 V X XX X X X XX XXX

Output form:
N = Nch Open Drain
C = CMOS Output

Detected Voltage:
Ex: 09 = 0.9V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance: 3: ±2.5%

Temperature: E: - 40°C to +85°C

Package Type and Pin Count:
CT: SOT-23-5, MB:SOT-89-3, ZB: TO-92-3

Taping Direction:
723: Left Taping, 713: Right Taping
no suffix: TO-92 Bulk

TC44 Series

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{IN} 12V
Output Voltage: CMOS ..... (V_{SS} – 0.3) to (V_{IN} + 0.3)
Open Drain 12V
Output Current 70mA
Operating Temperature ..... – 40°C to +85°C

Power Dissipation: SOT-23-5 ..... 150mW
SOT-89-3 ..... 300mW
TO-92 ..... 300mW
Storage Temperature ..... – 65°C to +150°C
Soldering Temperature ..... 260°C, 10 seconds

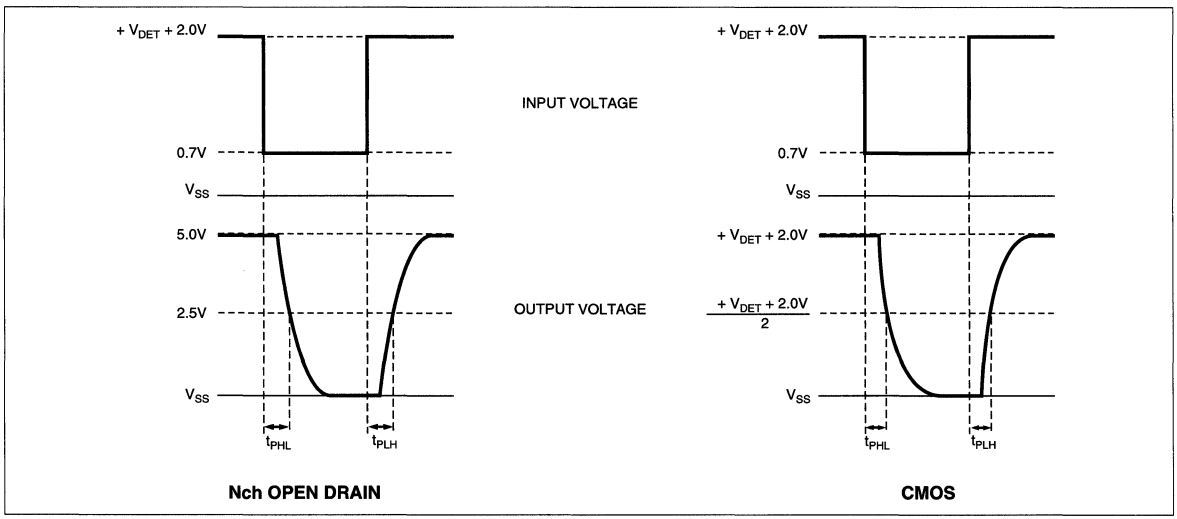
ELECTRICAL CHARACTERISTICS: (T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$-V_{DET}$	Threshold Voltage			($-V_{DET}$) x 0.975		($-V_{DET}$) x 1.025	V
V_{HYST}	Hysteresis Range			($-V_{DET}$) x 0.03	($-V_{DET}$) x 0.05	($-V_{DET}$) x 0.07	V
I_{SS}	Quiescent Current	V_{IN} = 1V (Output = ON)			1.0	(note 1)	µA
V_{IN}	Operating Voltage			0.7		10.0	V
I_{OUT} (Note 2)	Output Current	N-channel	V_{DS} = 0.5V				
		$-V_{DET}$ = 4.5V	V_{IN} = 4.0V		12.0		mA
		2.7V	2.5V		7.2		
		0.9V	0.8V		0.45		
		P-channel	V_{DS} = 0.5V				
		$-V_{DET}$ = 4.5V	V_{IN} = 5.0V		0.6		mA
		2.7V	3.0V		0.4		
		0.9V	1.0V		0.05		
$\frac{\Delta(-V_{DET})}{\Delta T_A}$	Tempco of ($-V_{DET}$)				±100		ppm/°C

NOTE 1: When V_{IN} drops to 1.5 volts or less, I_{SS} is approximately 0.5 – 1.0µA. At ($-V_{DET}$) ± 1V, it is approximately 1.5µA. For I_{SS} at higher values of V_{IN} or over temperature, see the appropriate curves.

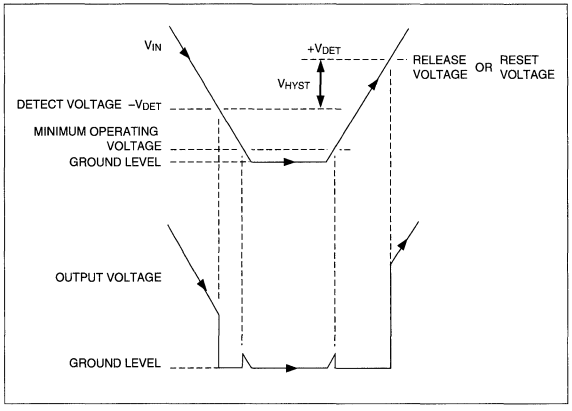
NOTE 2: These are average values for devices in the "ON" condition (V_{IN} lower than $-V_{DET}$ for the N-channel output, and V_{IN} higher than $-V_{DET}$ for the P-channel output).

DEFINITION OF OUTPUT DELAY TIME



Nch OPEN DRAIN **CMOS**

TIMING CHART

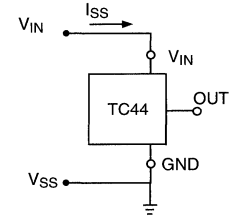


DESCRIPTION OF OPERATION

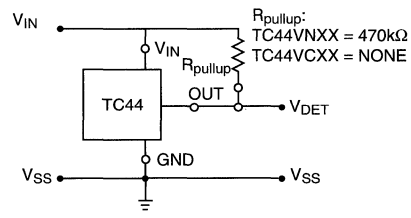
- When an input voltage (V_{IN}) is larger than the detected voltage ($-V_{DET}$), V_{IN} will equal V_{OUT} (OFF mode in Nch open drain).
- When V_{IN} is lower than $-V_{DET}$, V_{OUT} will equal V_{SS}.
- When V_{IN} drops below the minimum operating voltage (V_{MIN}), V_{OUT} will be undefined.
- When V_{IN} rises from ground potential (GND), the output will be undefined when V_{IN} is between GND and V_{MIN}. V_{OUT} will be equal to V_{SS} when V_{IN} is between V_{MIN} and the release voltage ($+V_{DET}$).
- The difference between $+V_{DET}$ and $-V_{DET}$ is V_{HYST}.

3

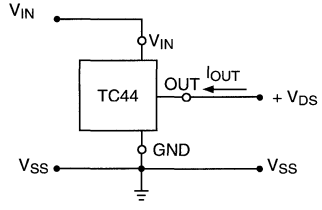
TEST CIRCUITS



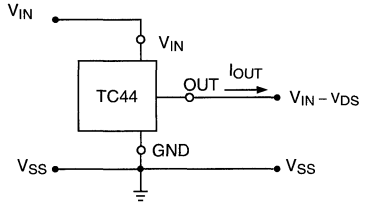
QUIESCENT CURRENT
(See Typical Characteristics #1, page 4)



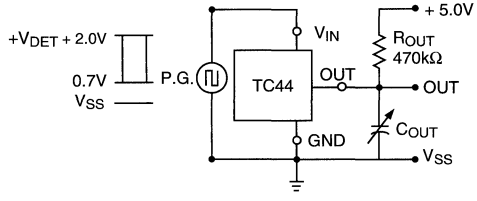
DETECTOR THRESHOLD
(See Typical Characteristics #2 & 7, pages 4 & 6)



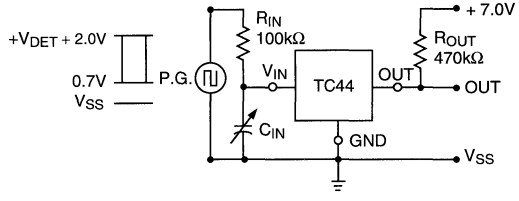
Nch DRIVER OUTPUT CURRENT
(See Typical Characteristics #3 & 8, pages 4 & 7)



Pch DRIVER OUTPUT CURRENT
(See Typical Characteristics #4, page 5)



OUTPUT DELAY (1)
(See Typical Characteristics #5, page 5)



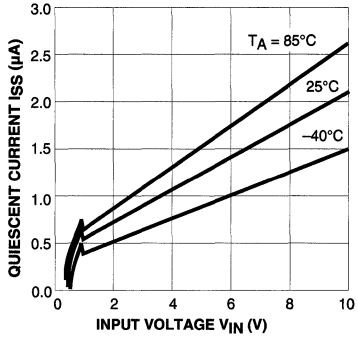
OUTPUT DELAY (2)
(See Typical Characteristics #6, page 5)

TC44 Series

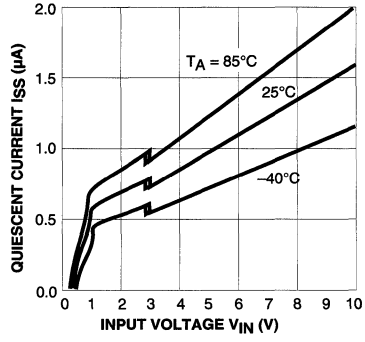
TYPICAL CHARACTERISTICS

1) Quiescent Current vs. Input Voltage

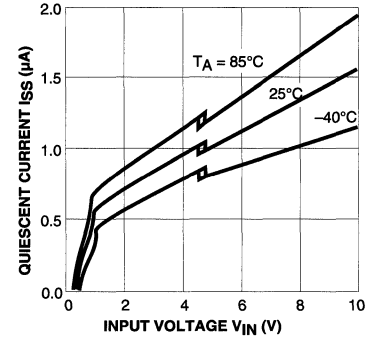
TC44VC09



TC44VC27

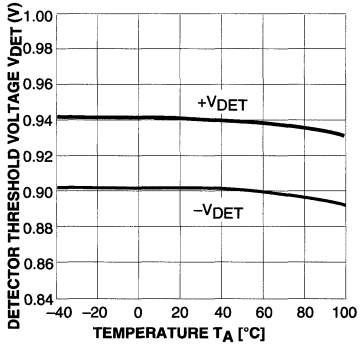


TC44VC45

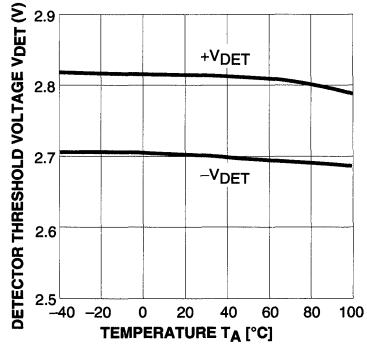


2) Detector Threshold vs. Temperature

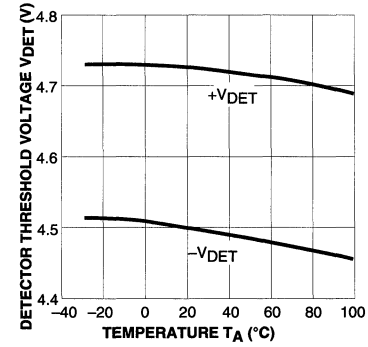
TC44VC09



TC44VC27

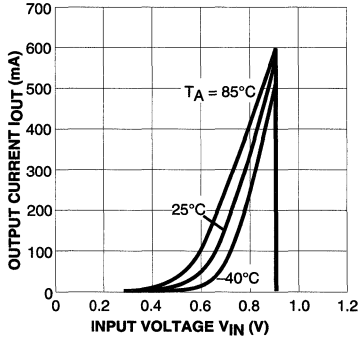


TC44VC45

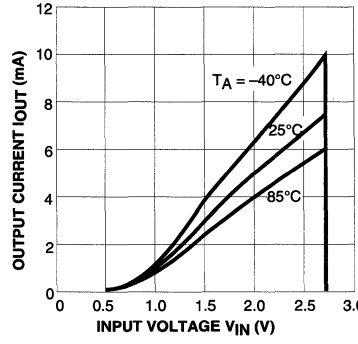


3) Nch Driver Output Current vs. Input Voltage

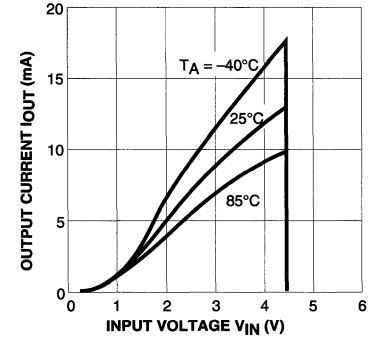
TC44VC09 or TC44VN09



TC44VC27 or TC44VN27



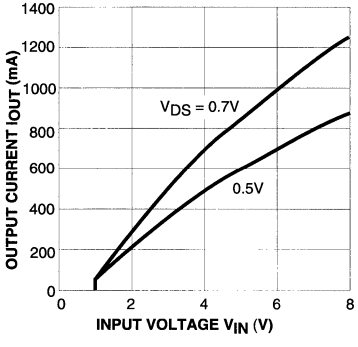
TC44VC45 or TC44VN45



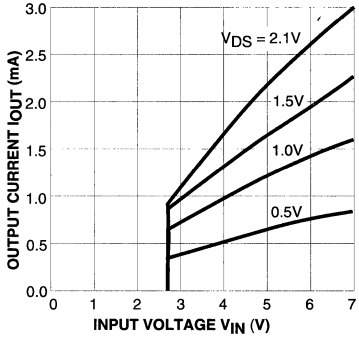
TYPICAL CHARACTERISTICS *(continued)*

4) Pch Driver Output Current vs. Input Voltage (T_A = 25°C)

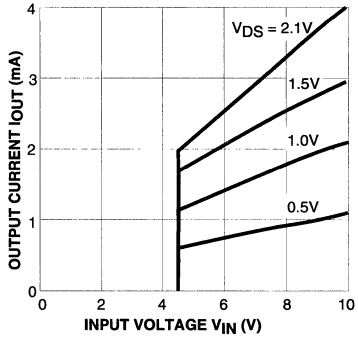
TC44VC09



TC44VC27

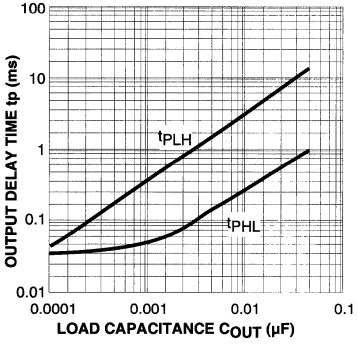


TC44VC45

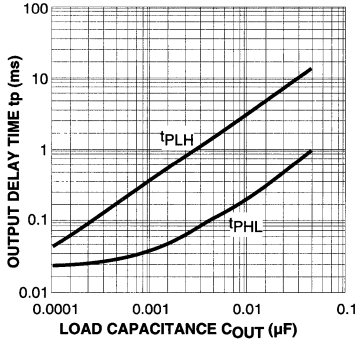


5) Output Delay vs. Load Capacitance (T_A = 25°C)

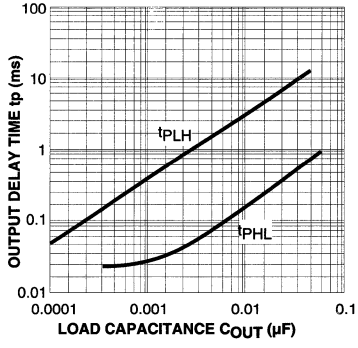
TC44VN09



TC44VN27

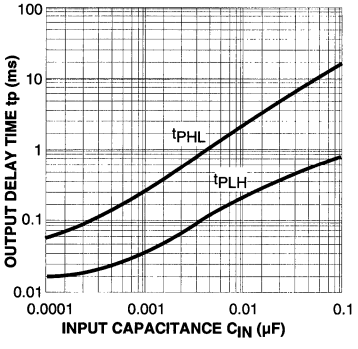


TC44VN45

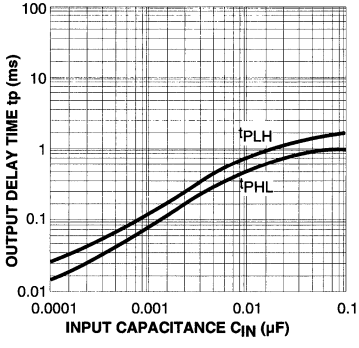


6) Output Delay vs. Input Capacitance (External)

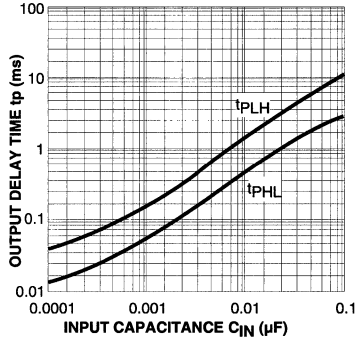
TC44VN09



TC44VN27



TC44VN45

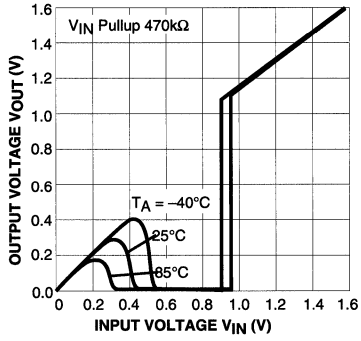


TC44 Series

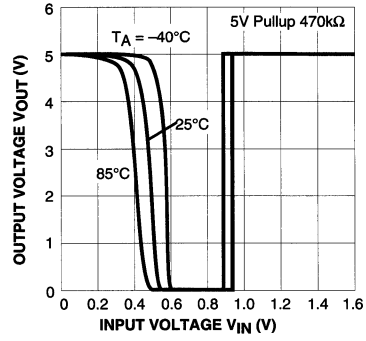
TYPICAL CHARACTERISTICS *(continued)*

7) Output Voltage vs. Input Voltage

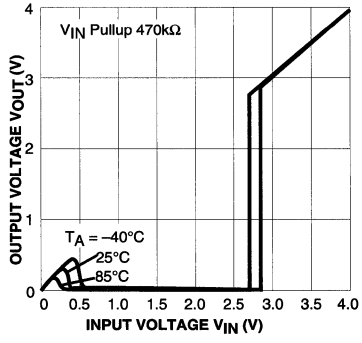
TC44VN09



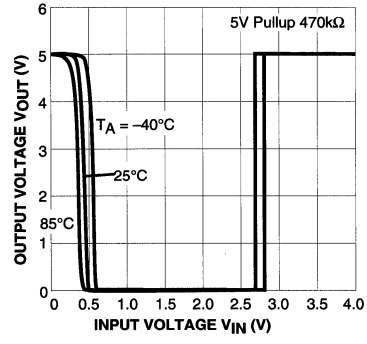
TC44VN09



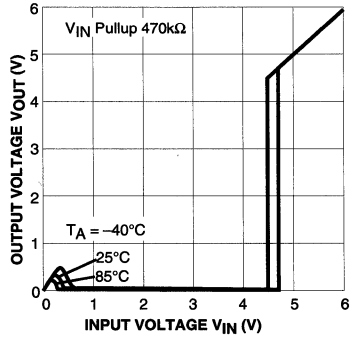
TC44VN27



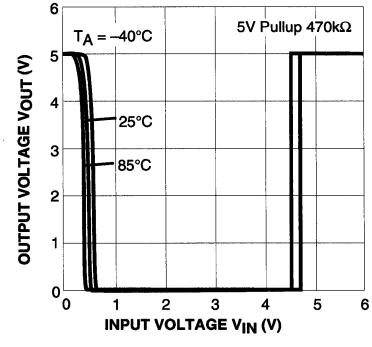
TC44VN27



TC44VN45



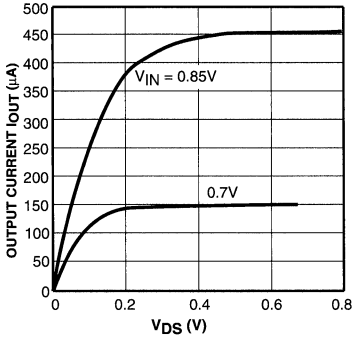
TC44VN45



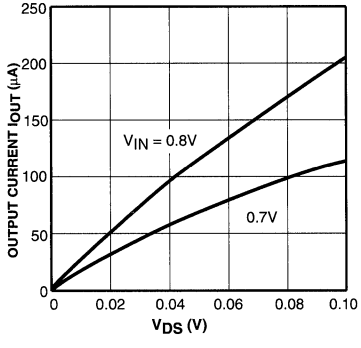
TYPICAL CHARACTERISTICS *(continued)*

8) Nch Driver Output Current vs. V_{DS} (T_A = 25°C)

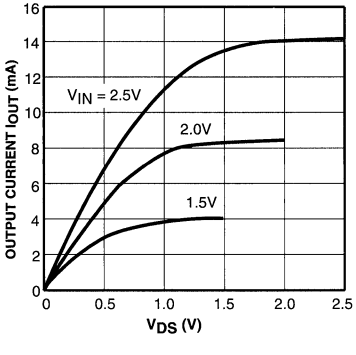
TC44VC09 or TC44VN09



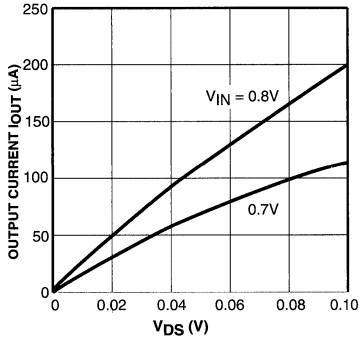
TC44VC09 or TC44VN09



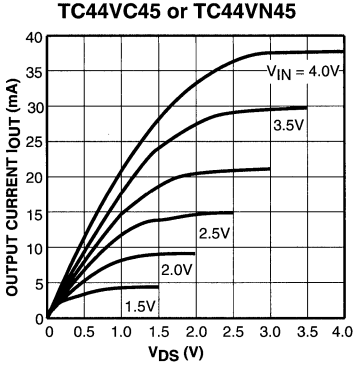
TC44VC27 or TC44VN27



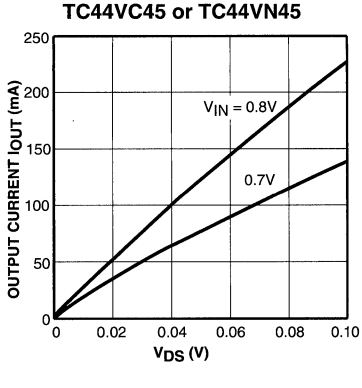
TC44VC27 or TC44VN27



TC44VC45 or TC44VN45



TC44VC45 or TC44VN45

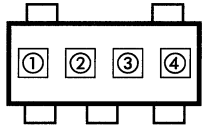


3

TC44 Series

MARKING

SOT-23-5



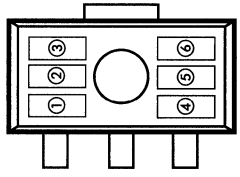
② = output (Nch or CMOS) plus first voltage digit

	0	1	2	3	4	5	6	
Nch	N	P	R	S	T	U	V	ex:CMOS3.X=◯◯Ⓚ
CMOS	G	H	J	K	L	M	N	

① = first voltage decimal ex:CMOS3.4=④Ⓚ◯◯

③ & ④ = assembly lot number

SOT-89-3



① = T (fixed)

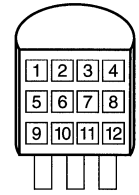
② = first voltage digit (0-6)

③ = first voltage decimal (0-9)

④ = output (Nch = A, CMOS = C)

⑤ and ⑥ = lot assembly number

TO-92



①, ② & ③ = 44V (fixed)

④ = output (C = CMOS, N = Nch)

⑤ = first voltage digit (0-6)

⑥ = first voltage decimal (0-9)

⑦ = fixed: 0

⑧ = $-V_{DET}$ ± tolerance: 3 = ±2.5%

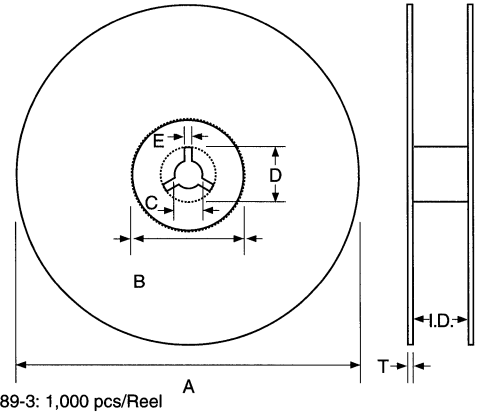
⑨, ⑩, ⑪ & ⑫ = assembly lot number

TAPING REEL

	SOT-23-5		SOT-89		TO-92
A	178	±1.0	178	±2.0	360
B	60	±2.0	80	±1.0	80
C	13	±0.2	13	±0.05	30
D	22	±0.5	21	±0.5	45
E	2	±0.2	2	±0.2	2
I.D.	8.5	±1.5	14.0	+1/-1.5	43
T	1.5	±0.3	2.0	±0.5	5

(unit = mm)

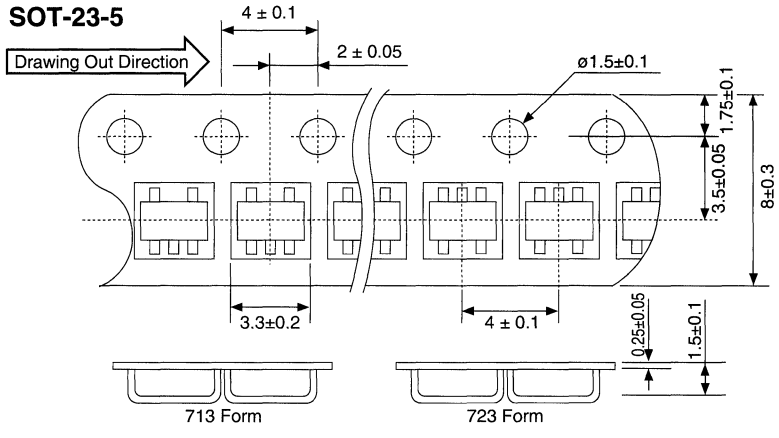
Reel Materials: SOT-23-5/SOT-89: Plastic
TO-92: Cardboard + Plastic Hub



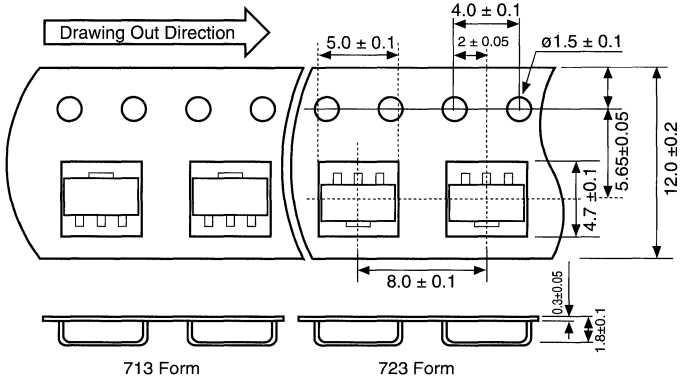
SOT-89-3: 1,000 pcs/Reel
TO-92: 2,000 pcs/Reel
SOT-23-5: 3,000 pcs/Reel

TAPING FORM

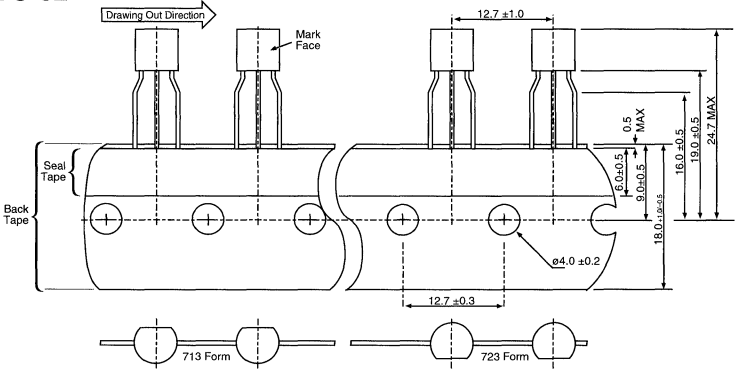
SOT-23-5

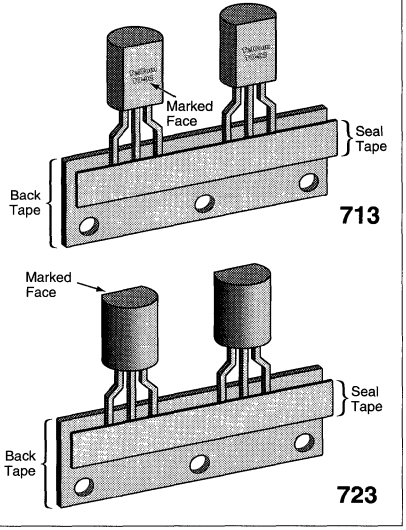


SOT-89-3



TO-92





VOLTAGE DETECTOR

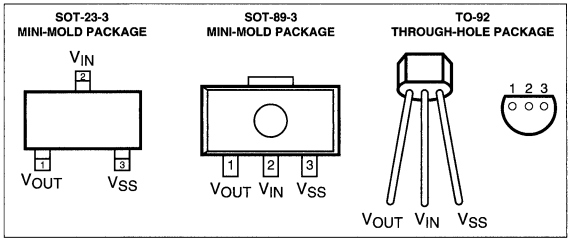
FEATURES

- Precise Detection Thresholds ..... Standard ± 2.0%
  Custom ± 1.0%
- Small Packages SOT-23, SOT-89, TO-92
- Low Current Drain ..... Typ. 1μA
- Wide Detection Range ..... 2.1V to 6.0V
- Wide Operating Voltage Range ..... 1.5V to 10.0V

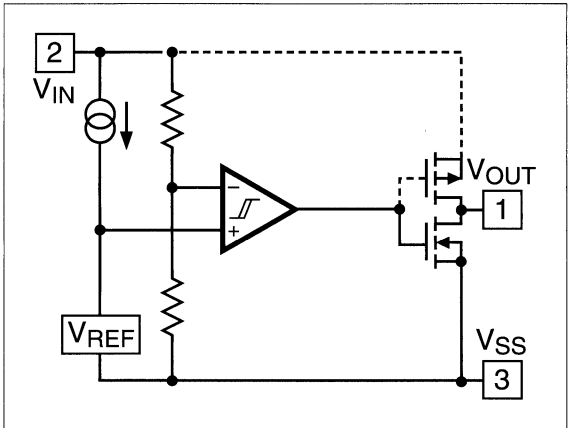
APPLICATIONS

- Battery Voltage Monitoring
- Microprocessor Reset
- System Brownout Protection
- Switching Circuit in Battery Backup
- Level Discriminator

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



Open-drain version (N) has only an N-channel output.
"CMOS" output has both an N-channel and a P-channel output.

GENERAL DESCRIPTION

The TC54 Series are CMOS voltage detectors, suited especially for battery-powered applications because of their extremely low 1 μA operating current and small surface-mount packaging. Each part is laser trimmed to the desired threshold voltage which can be ordered in the range of 2.1V to 6.0V, in 0.1V steps.

The design includes a comparator, low-current high-precision reference, laser-trimmed divider, hysteresis circuit and output driver. The latter is available in either an open-drain or complementary ("CMOS") configuration.

In operation, the TC54 output (V_{OUT}) remains in the logic HIGH state as long as V_{IN} is greater than the specified threshold voltage ($-V_{DET}$). When V_{IN} falls below $-V_{DET}$, the output is driven to a logic LOW. V_{OUT} remains LOW until V_{IN} rises above $-V_{DET}$ by an amount V_{HYST}, whereupon it resets to a logic HIGH.

ORDERING INFORMATION

PART CODE TC54 V X XX X X X XX XXX

Output form:
N = Nch Open Drain
C = CMOS Output

Detected Voltage:
Ex: 21 = 2.1V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance:
1 = ± 1.0% (custom)
2 = ± 2.0% (standard)

Temperature: E: – 40°C to + 85°C

Package Type and Pin Count:
CB: SOT-23-3, MB: SOT-89-3, ZB: TO-92

Taping Direction:
723: Left Taping, 713: Right Taping,
no suffix: TO-92 Bulk

TC54 Series

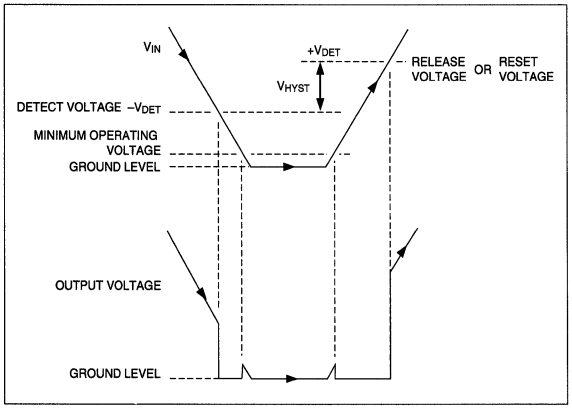
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{IN} 12V
Output Voltage: CMOS ..... (V_{SS} – 0.3) to (V_{IN} + 0.3)
Open Drain ..... (V_{SS} – 0.3) to 12 V
Output Current 50mA
Power Dissipation: SOT-23-3 ..... 150mW
SOT-89-3 ..... 300mW
TO-92 ..... 300mW
Operating Temperature ..... – 40°C to + 85°C
Storage Temperature ..... – 65°C to + 150°C
Soldering Temperature ..... 260°C, 10 seconds

ELECTRICAL CHARACTERISTICS: (T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{IN}	Operating Voltage	$-V_{DET}$ = 2.1 to 6.0V		1.5		10.0	V
I_{SS}	Quiescent Current	V_{IN} = 2.1V			1.0	3.0	µA
		3.0V			1.3	3.4	
		4.0V			1.6	3.8	
		5.0V			2.0	4.2	
$-V_{DET}$	Threshold Voltage			($-V_{DET}$) x 0.98		($-V_{DET}$) x 1.02	V
V_{HYST}	Hysteresis Range			($-V_{DET}$) x 0.02	($-V_{DET}$) x 0.05	($-V_{DET}$) x 0.08	V
I_{OUT}	Output Current	Nch V_{DS} = 0.5	V_{IN} = 2.1V		7.7		mA
			3.0V		10.1		
			4.0V		11.5		
			5.0V		13.0		
		Pch V_{DS} = 2.1V	V_{IN} = 8.0V		– 10.0		
	Tempco of ($-V_{DET}$)	– 40°C ≤ T_A ≤ 85°C			± 100		ppm/°C

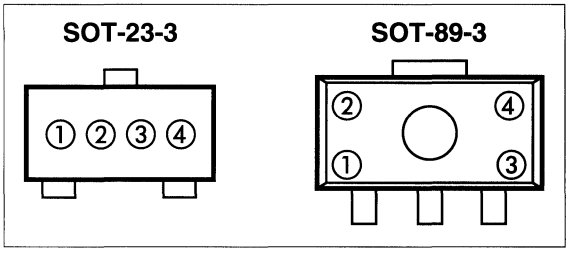
TIMING CHART



DESCRIPTION OF OPERATION

- When an input voltage (V_{IN}) is larger than the detected voltage ($-V_{DET}$), V_{IN} will equal V_{OUT} (OFF mode in CMOS output).
- When V_{IN} is lower than $-V_{DET}$, V_{OUT} will equal V_{SS}.
- When V_{IN} drops below the minimum operating voltage (V_{MIN}), V_{OUT} will be undefined.
- When V_{IN} rises from ground potential (GND), the output will be undefined when V_{IN} is between GND and V_{MIN}. V_{OUT} will be equal to V_{SS} when V_{IN} is between V_{MIN} and the release voltage ($+V_{DET}$).
- The difference between $+V_{DET}$ and $-V_{DET}$ is V_{HYST}.

MARKING



① = output (Nch or CMOS) plus first voltage digit

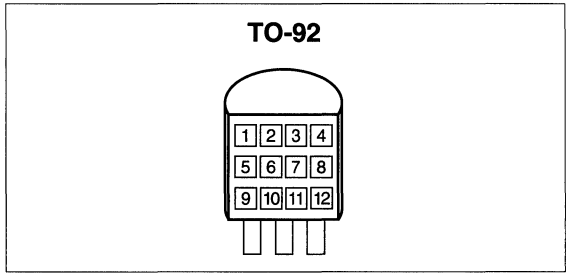
	2	3	4	5	6
Nch	M	N	P	R	S
CMOS	C	D	E	F	H

ex:CMOS3.X=⓪◯◯◯

② = first voltage decimal (0-9)

ex:CMOS3.4=⓪④◯◯

③ & ④ = assembly lot number



①, ② & ③ = 54_ (fixed)

④ = output (C = CMOS, N = Nch)

⑤ = first voltage digit (2-6)

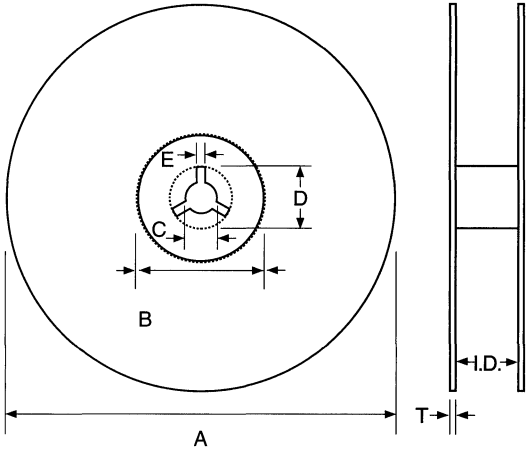
⑥ = first voltage decimal (0-9)

⑦ = extra feature code : fixed : 0

⑧ = detecting accuracy
1 = ± 1.0% (custom), 2 = ± 2.0% (standard)

⑨, ⑩, ⑪ & ⑫ = assembly lot number

TAPING REEL



	SOT-23-5		SOT-89-3		TO-92
A	178	±1.0	178	±2.0	360
B	60	±2.0	80	±1.0	80
C	13	±0.2	13	±0.05	30
D	22	±0.5	21	±0.5	45
E	2	±0.2	2	±0.2	2
I.D.	8.5	±1.5	14.0	+1/-1.5	43
T	1.5	±0.3	2.0	±0.5	5

(unit = mm)

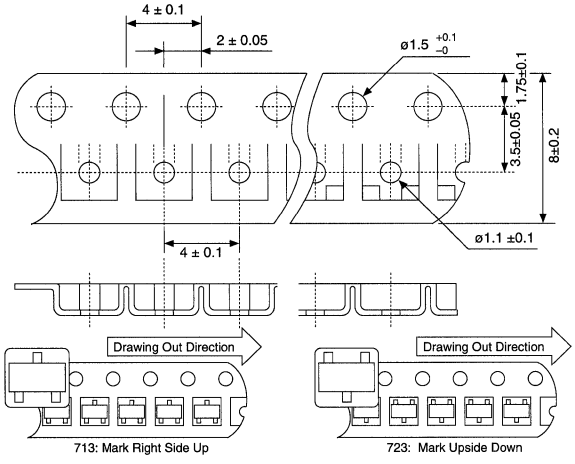
Reel Materials: SOT-23-5/SOT-89-3: Plastic
TO-92: Cardboard + Plastic Hub

SOT-89-3: 1,000 pcs/Reel
TO-92: 2,000 pcs/Reel
SOT-23-5: 3,000 pcs/Reel

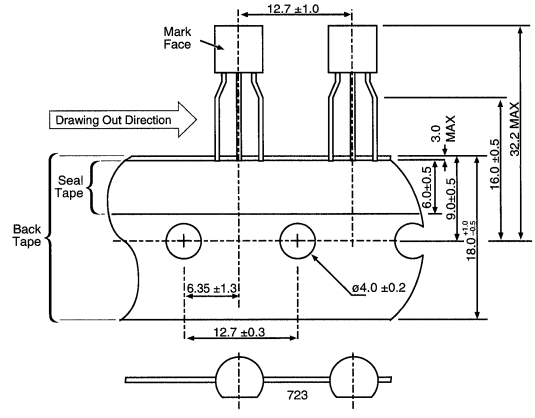
TC54 Series

TAPING FORM

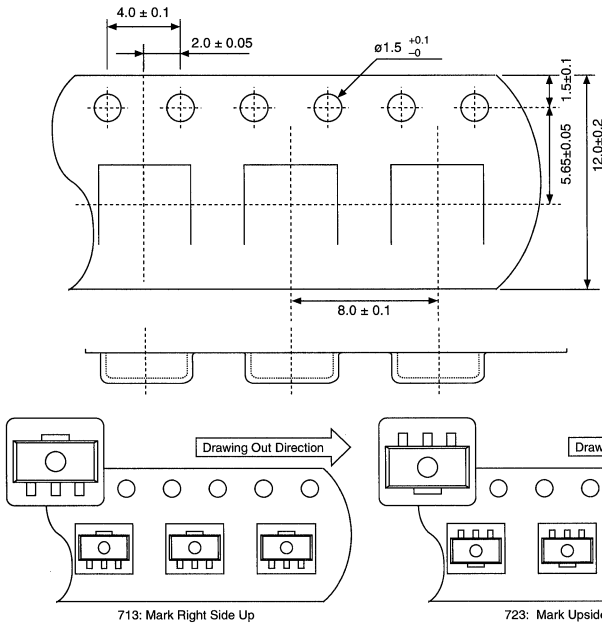
SOT-23-3

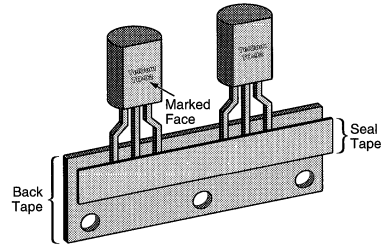


TO-92



SOT-89-3





VOLTAGE REGULATOR (MEDIUM CURRENT)

FEATURES

- **Low Power CMOS**
- **Extremely Low Power Consumption ..... 1.1μA Typ**
- **Dropout Voltage ..... 0.5V Typ at 60mA**
- **High Output Current ..... 120mA Typ**
- **High Accuracy Output Voltage ..... ±2.5%**
- **Low Temp. Coefficient of Output Voltage ..... ±100ppm/°C Typ**
- **Wide Choice of V_{OUT} ..... 2.0V to 6.0V in 0.1V Steps**
- **Compact Package TO-92, SOT-89-3**

APPLICATIONS

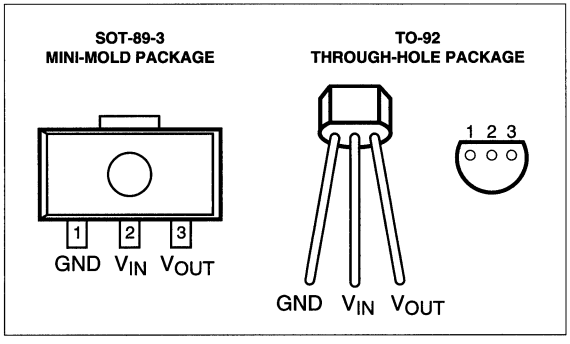
- **Constant-voltage power supply for battery-powered devices**
- **Constant-voltage power supply for communications, and video equipment**
- **Stable standard voltage supply**

GENERAL DESCRIPTION

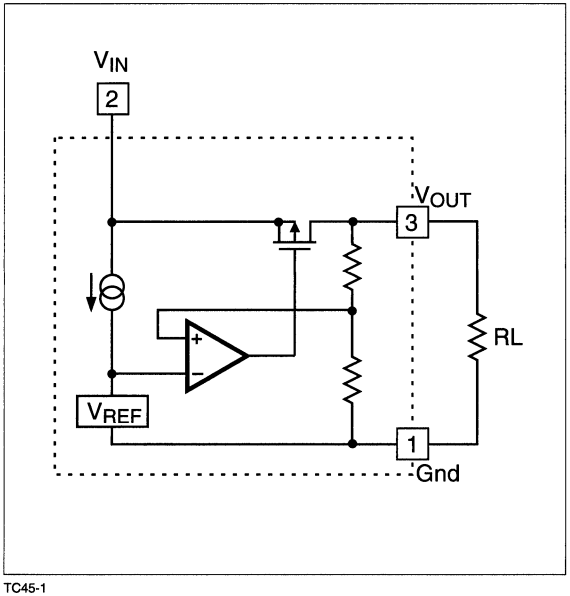
The TC45 Series are high accuracy 3-terminal CMOS voltage regulators. Output currents extend to 120mA, with quiescent currents around 1μA. The design features very low dropout voltage and overcurrent protection. Available output voltages extend from 2.0V to 6.0V in 0.1V steps. The device is available in TO-92 and SOT-89-3 packages.

3

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



TC45-1

ORDERING INFORMATION

PART CODE **TC45ER XX X X X XX XXX**

Output Voltage:
Ex: 20 = 2.0V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance:
3: ±2.5%

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
MB: SOT-89-3
ZB: TO-92-3

Taping Direction:
723: Left Taping
713: Right Taping
no suffix: TO-92 Bulk

TC45 Series

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Input Voltage	V_{IN}	+ 12	V
Output Current	I_{OUT}	150	mA
Output Voltage	V_{OUT}	(V_{SS} – 0.3) to (V_{IN} + 0.3)	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	T_A	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Soldering Temperature	T_{solder}	260°C, 10 sec	

ELECTRICAL CHARACTERISTICS:
TC45ER30 (V_{OUT} = 3.0V, T_A = 25°C)

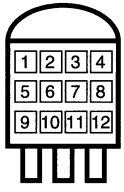
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage	I_{OUT} = 10mA	2.925	3.000	3.075	V
I_{OUT}	Output Current	V_{IN} = 5.0V	50	80		mA
ΔV_{OUT}	Load Regulation	V_{IN} = 5.0V, 1mA ≤ I_{OUT} ≤ 60mA		40	80	mV
Vdif	I/O Voltage Difference	I_{OUT} = 40mA		0.5	0.7	V
I_{SS}	Operating Current	V_{IN} = 5.0V		1.1	3.3	µA
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \cdot V_{OUT}}$	Line Regulation	I_{OUT} = 10mA $\lvert V_{OUT}\rvert$ +1.0V ≤ $\lvert V_{IN}\rvert$ ≤ 10V		0.1		% /V
V_{IN}	Input Voltage				10	V
Ilim	Current Limit			240		mA
$\Delta V_{OUT}/\Delta T_A$	Temperature Coefficient	I_{OUT} = 10mA – 40°C ≤ T_A ≤ 85°C		±100		ppm/°C

ELECTRICAL CHARACTERISTICS:
TC45ER50 (V_{OUT} = 5.0V, T_A = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage	I_{OUT} = 10mA	4.875	5.000	5.125	V
I_{OUT}	Output Current	V_{IN} = 7.0V	80	120		mA
ΔV_{OUT}	Load Regulation	V_{IN} = 7.0V, 1mA ≤ I_{OUT} ≤ 80mA		40	80	mV
Vdif	I/O Voltage Difference	I_{OUT} = 60mA		0.5	0.7	V
I_{SS}	Operating Current	V_{IN} = 7.0V		1.3	3.9	µA
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \cdot V_{OUT}}$	Line Regulation	I_{OUT} = 10mA $\lvert V_{OUT}\rvert$ + 1.0V ≤ $\lvert V_{IN}\rvert$ ≤ 10V		0.1		% /V
V_{IN}	Input Voltage				10	V
Ilim	Current Limit			240		mA
$\Delta V_{OUT}/\Delta T_A$	Temperature Coefficient	I_{OUT} = 10mA – 40°C ≤ T_A ≤ 85°C		±100		ppm/°C

MARKING

TO-92



①, ②, ③ & ④ represent 45ER: Fixed

⑤ represents first digit of voltage

Mark ⑤	Volt	Mark ⑤	Volt
2	2. ⑥ (V)	5	5. ⑥ (V)
3	3. ⑥ (V)	6	6. ⑥ (V)
4	4. ⑥ (V)		

⑥ represents first decimal place of voltage

Mark ⑥	Volt	Mark ⑥	Volt
0	⑤ .0 (V)	5	⑤ .5 (V)
1	⑤ .1 (V)	6	⑤ .6 (V)
2	⑤ .2 (V)	7	⑤ .7 (V)
3	⑤ .3 (V)	8	⑤ .8 (V)
4	⑤ .4 (V)	9	⑤ .9 (V)

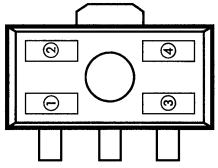
⑦ Extra Feature Code: Fixed: 0

⑧ represents regulation accuracy

Mark ⑧	Regulation Accuracy
3	±2.5% (Standard)

⑨, ⑩, ⑪ & ⑫ represent assembly lot number

SOT-89-3



① represents first decimal place of voltage

Mark ①	Volt	Mark ①	Volt
0	②. 0 (V)	5	② .5 (V)
1	②.1 (V)	6	② .6 (V)
2	②.2 (V)	7	② .7 (V)
3	②.3 (V)	8	② .8 (V)
4	②.4 (V)	9	② .9 (V)

② represents first digit of voltage

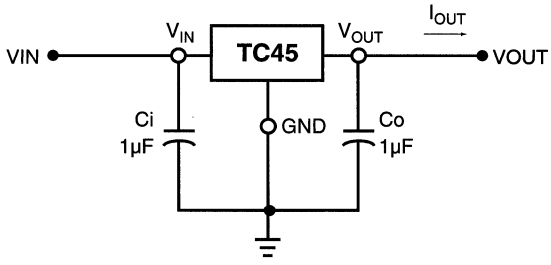
Mark ②	Volt	Mark ②	Volt
J	2. ① (V)	M	5.① (V)
K	3. ① (V)	N	6.① (V)
L	4. ① (V)		

③ & ④ represent assembly lot number

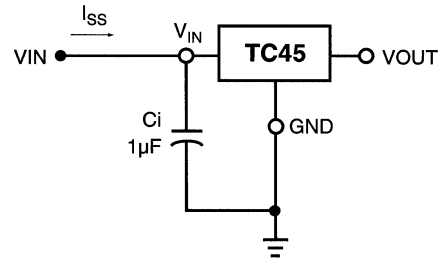
3

TC45 Series

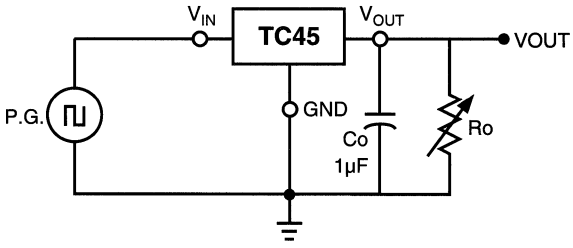
TEST CIRCUITS
TC45ER50



STATIC CHARACTERISTICS



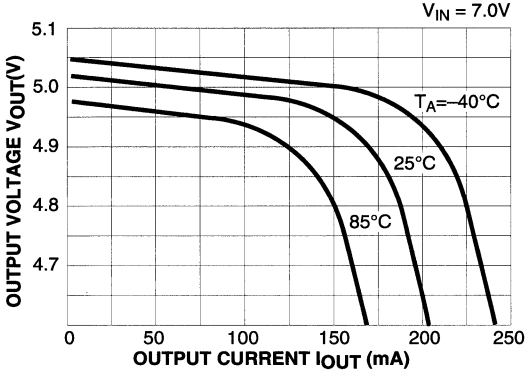
QUIESCENT CURRENT



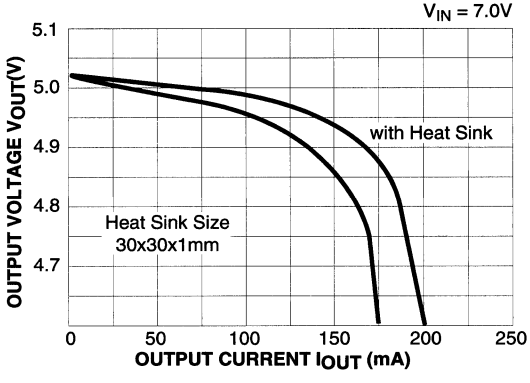
LINE TRANSIENT RESPONSE

TYPICAL CHARACTERISTICS
TC45ER50

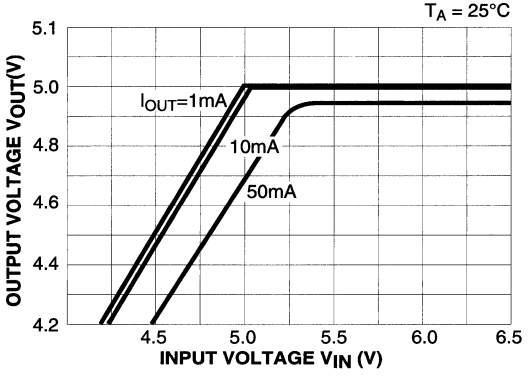
Output Voltage vs. Output Current



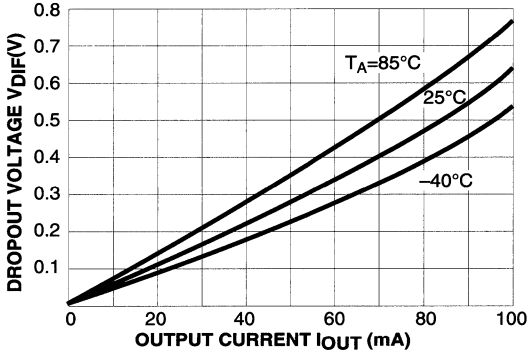
Output Voltage vs. Output Current



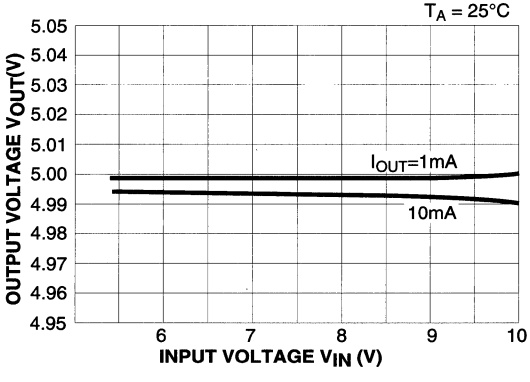
Output Voltage vs. Input Voltage



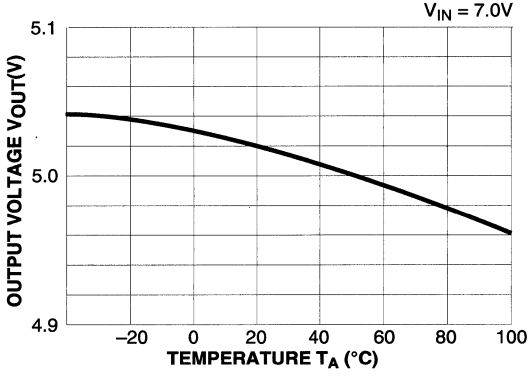
Dropout Voltage vs. Output Current



Output Voltage vs. Input Voltage



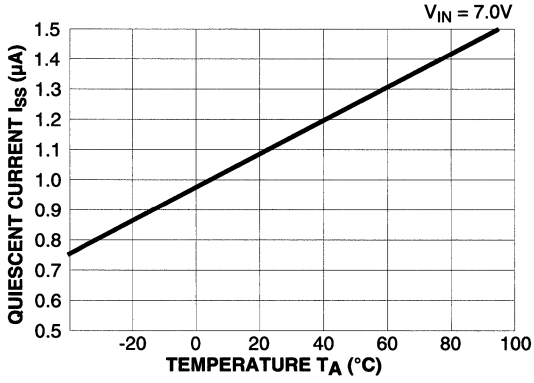
Output Voltage vs. Temperature



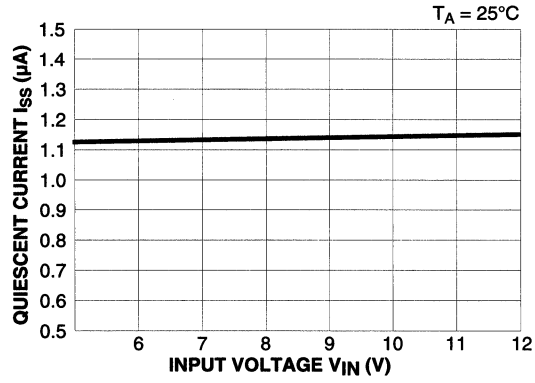
TC45 Series

TYPICAL CHARACTERISTICS
TC45ER50

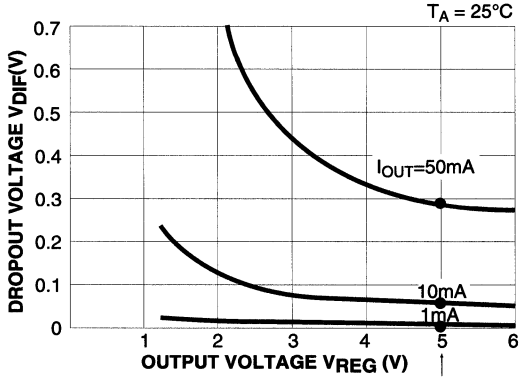
Quiescent Current vs. Temperature



Quiescent Current vs. Input Voltage

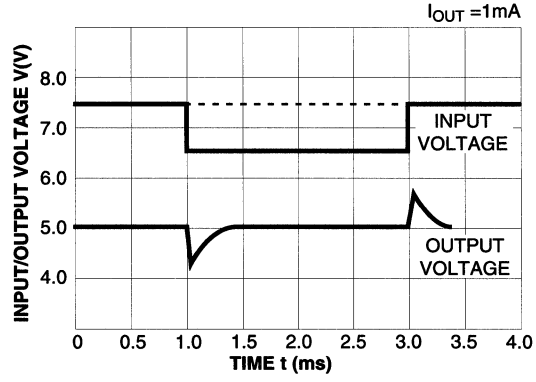


Dropout Voltage vs. Output Voltage

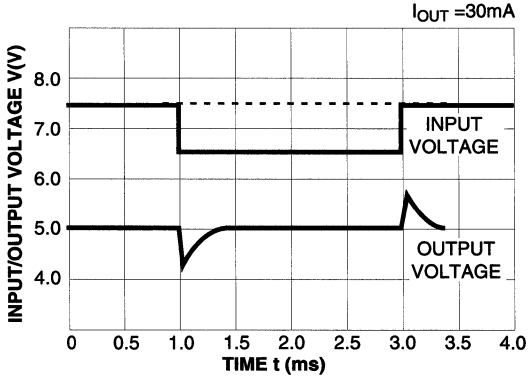


e.g., TC45ER5003EMB

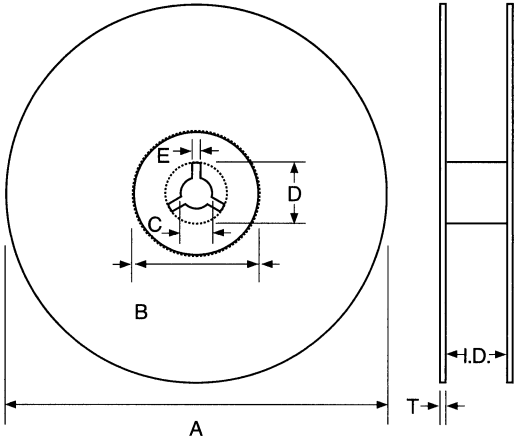
Line Transient Response



Line Transient Response



TAPING REEL



	SOT-89-3	TO-92
A	178 ±2.0	360
B	80 ±1.0	80
C	13 ±0.05	30
D	21 ±0.5	45
E	2 ±0.2	2
I.D.	14.0 +1/-1.5	43
T	2.0 ±0.5	5

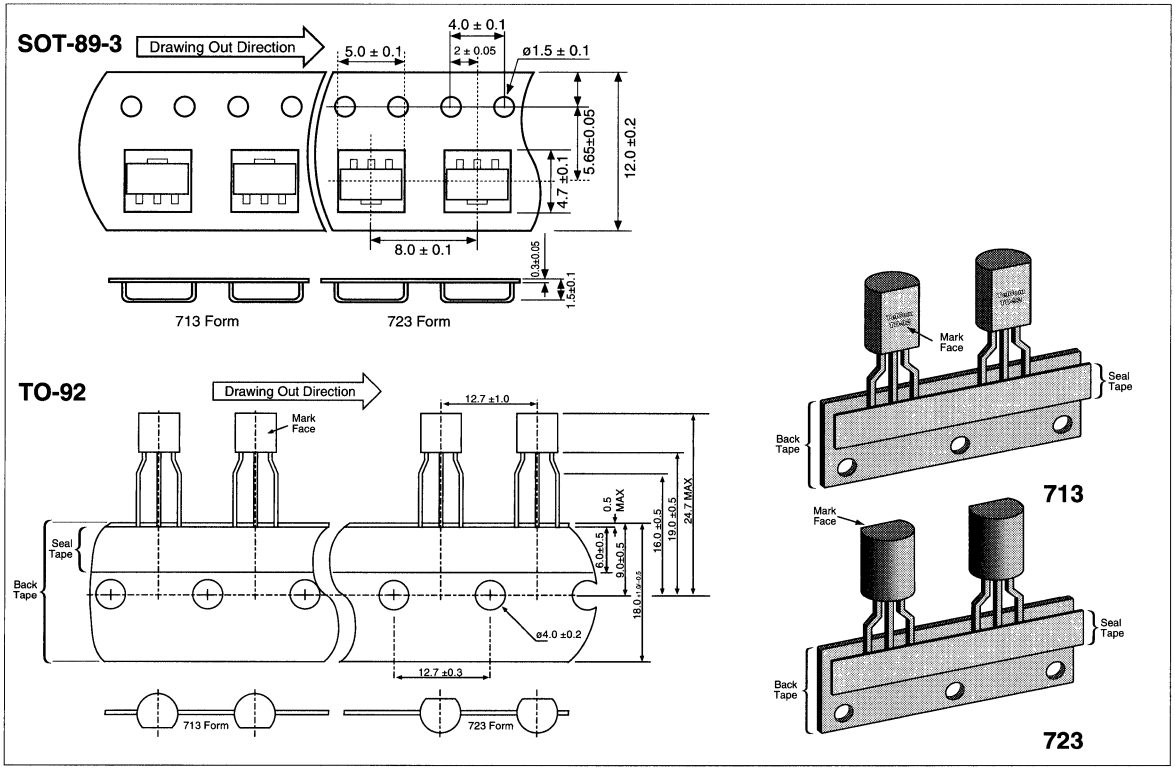
(unit = mm)

Reel Materials: SOT-89-3: Plastic
TO-92: Cardboard + Plastic Hub

SOT-89-3: 1,000 pcs/Reel
TO-92: 2,000 pcs/Reel

3

TAPING FORM



VOLTAGE REGULATOR (LOW DROPOUT, LOW CURRENT)

FEATURES

- **Extremely Low Quiescent Current ..... 1.1 μA Typ**
- **Low Dropout Voltage ..... 30 mV @ 1 mA Typ**
- **High Accuracy Output Voltage ..... ±2.5%**
- **Wide Choice of V_{OUT} ..... 2.0V to 6.0V in 0.1V Steps**
- **Surface Mount or Through-Hole Packages**

APPLICATIONS

- **Low-loss power supply for battery-powered devices**
- **Post-regulator for boost converters in portable equipment**
- **Low Iq programmable reference**

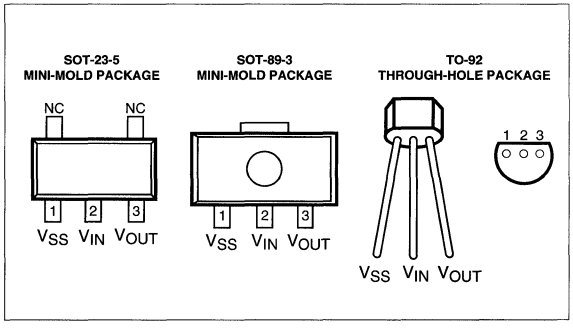
GENERAL DESCRIPTION

The TC46 Series are high accuracy 3-terminal CMOS voltage regulators. Output currents extend to 80mA, with quiescent currents around 1μA. The design features very low dropout voltage and fast recovery from turn-on transients, both important features for battery-operated communications equipment. The device is also suitable as a micropower voltage reference.

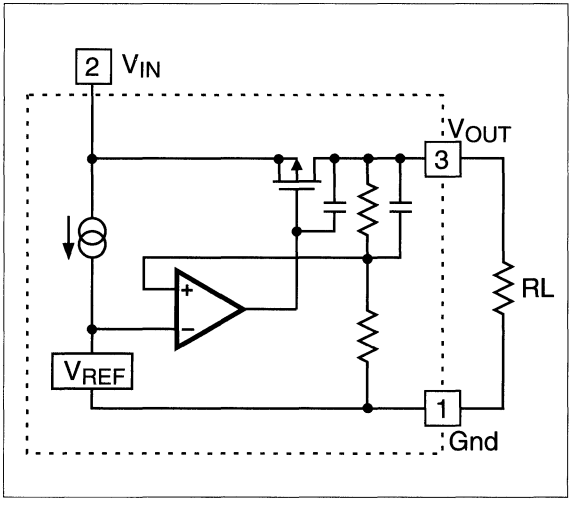
Available output voltages extend from 2.0V to 6.0V in 0.1V steps. They are available in SOT-23, SOT-89, and TO-92 packages.

3

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART CODE **TC46LR XX X X X XX XXX**

Output Voltage:
Ex: 20 = 2.0V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance:
3: ±2.5%

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
CT: SOT-23-5
MB: SOT-89-3
ZB: TO-92-3

Taping Direction:
723: Left Taping
713: Right Taping
no suffix: TO-92 Bulk

TC46

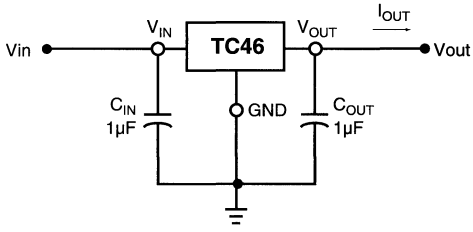
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Input Voltage	V_{IN}	+12	V
Output Current	I_{OUT}	150	mA
Output Voltage	V_{OUT}	(V_{SS} – 0.3) to (V_{IN} + 0.3)	V
Power Dissipation TO-92 and SOT-89-3 SOT-23-5	Pd1 Pd2	300 150	mW
Operating Temperature Range	T_A	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Soldering Temperature	T_{solder}	260°C, 10 sec	

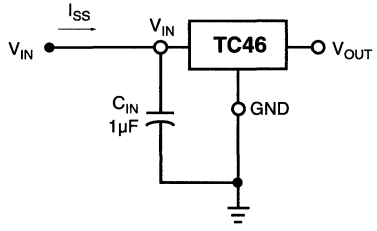
ELECTRICAL CHARACTERISTICS: (T_A = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage	10µA ≤ I_{OUT} ≤ 10mA	V_{OUT} x 0.975		V_{OUT} x 1.025	V
I_{OUT}	Output Current	V_{IN} = V_{OUT} + 2.0V				
		V_{OUT} = 2.0V	25	35		
		V_{OUT} = 3.0V	35	50		mA
		V_{OUT} = 4.0V	45	65		
		V_{OUT} = 5.0V, 6.0V	55	80		
ΔV_{OUT}	Load Regulation	V_{IN} = V_{OUT} + 2.0V				
		V_{OUT} = 2.0V, 1mA ≤ I_{OUT} ≤ 35mA		30	45	
		V_{OUT} = 3.0V, 1mA ≤ I_{OUT} ≤ 50mA		40	60	mV
		V_{OUT} = 4.0V, 1mA ≤ I_{OUT} ≤ 65mA		50	75	
		V_{OUT} = 5.0V, 6.0V, 1mA ≤ I_{OUT} ≤ 80mA		60	90	
Vdif	I/O Voltage Difference	I_{OUT} = 1mA				
		V_{OUT} = 2.0V		60	90	
		V_{OUT} = 3.0V		40	60	mV
		V_{OUT} = 4.0V, 5.0V, 6.0V		25	38	
I_{SS}	Quiescent Current	V_{IN} = V_{OUT} + 2.0V				
		V_{OUT} = 2.0V		1.0	3.0	
		V_{OUT} = 3.0V		1.1	3.3	µA
		V_{OUT} = 4.0V		1.2	3.6	
		V_{OUT} = 5.0V, 6.0V		1.3	3.9	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	I_{OUT} = 1mA (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 10V		0.05	0.2	%/V
V_{IN}	Input Voltage				10	V
$\Delta V_{OUT}/\Delta T_A$	Temperature Coefficient	I_{OUT} = 10mA – 40°C ≤ T_A ≤ 85°C		±100		ppm/°C

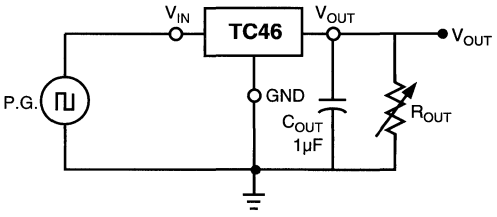
TEST CIRCUITS



STATIC CHARACTERISTICS
(Except QUIESCENT CURRENT)



QUIESCENT CURRENT



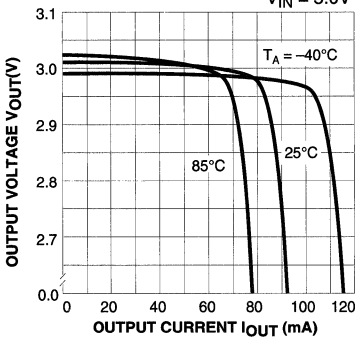
LINE TRANSIENT RESPONSE

TC46

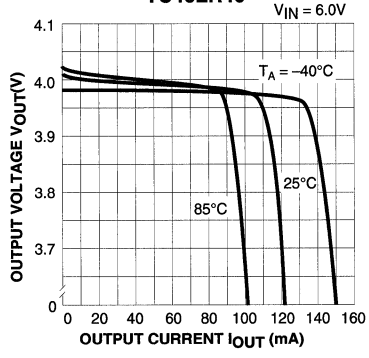
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current

TC46LR30



TC46LR40



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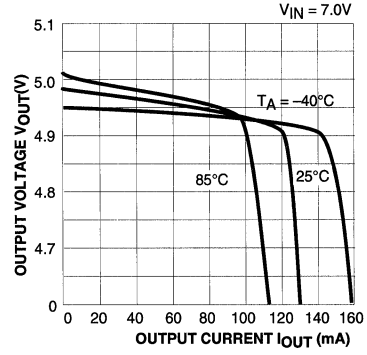
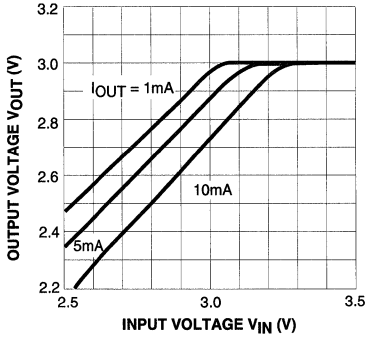


2) Output Voltage vs. Input Voltage (T_A = 25°C)

TC46LR30



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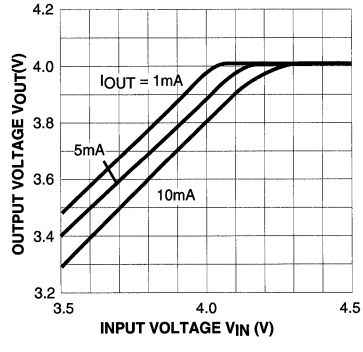

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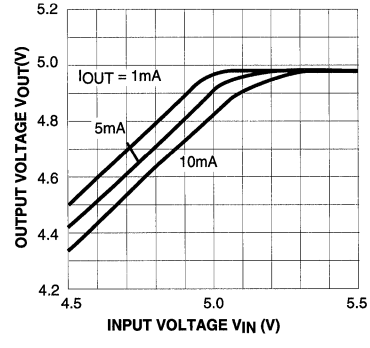

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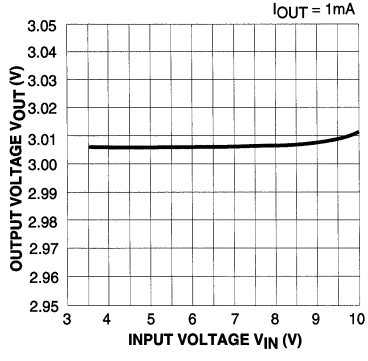

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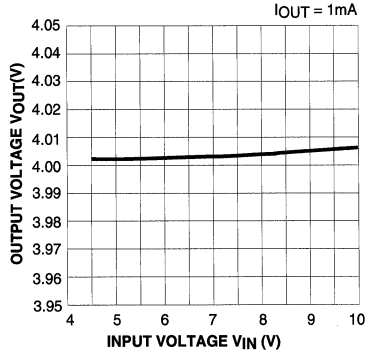

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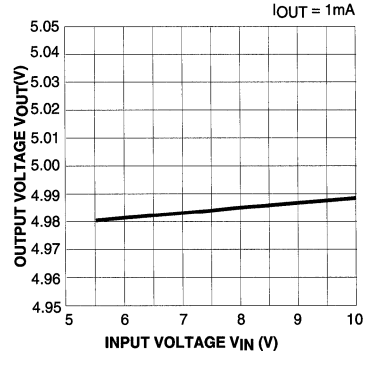
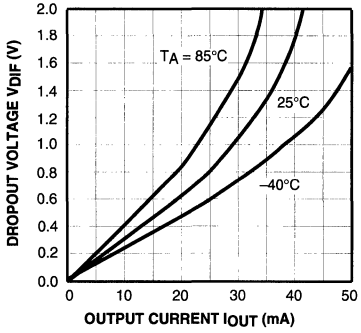


TYPICAL CHARACTERISTICS (CONT.)

3) Dropout Voltage vs. Output Current

TC46LR30



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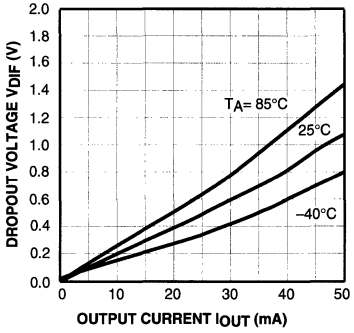

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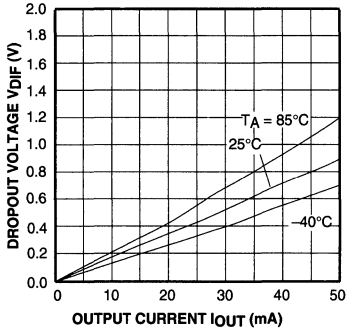
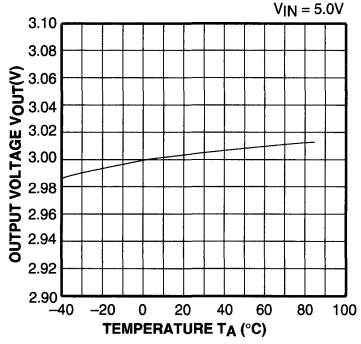


4) Output Voltage vs. Temperature (I_{OUT} = 10mA)

TC46LR30



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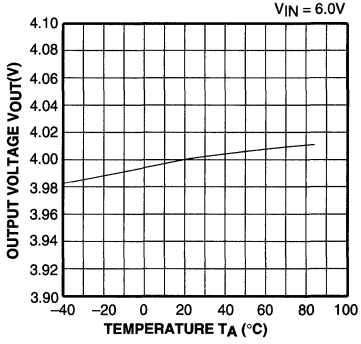

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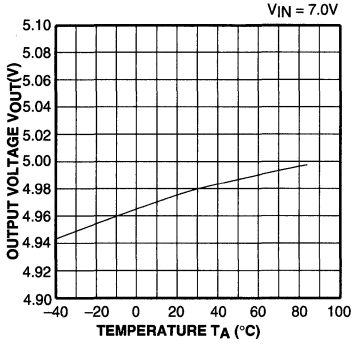
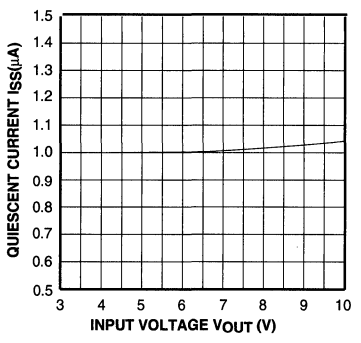


5) Quiescent Current vs. Input Voltage (T_A = 25°C)

TC46LR30



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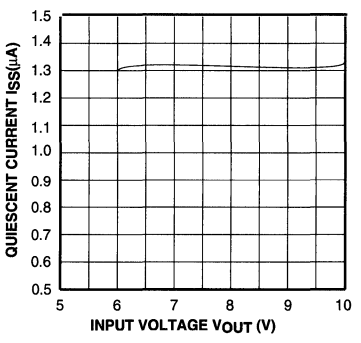

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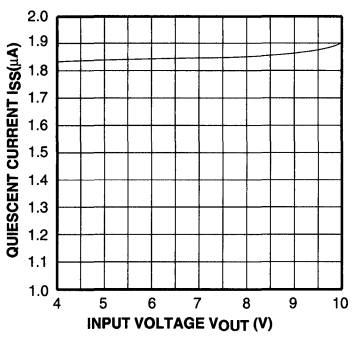
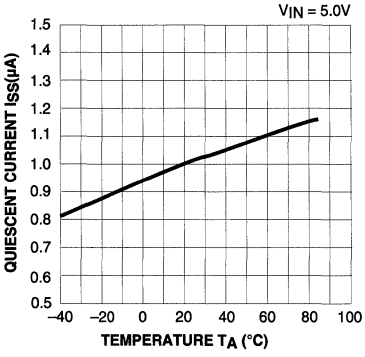


TC46

TYPICAL CHARACTERISTICS (CONT.)

6) Quiescent Current vs. Temperature

TC46LR30



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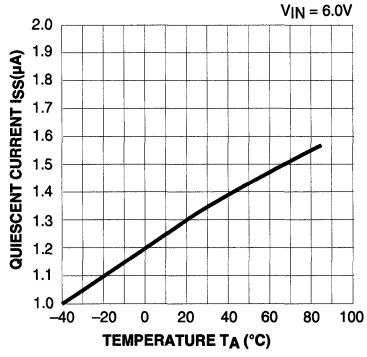

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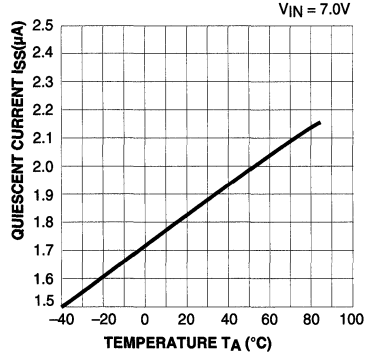
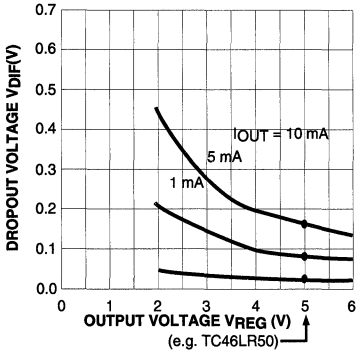
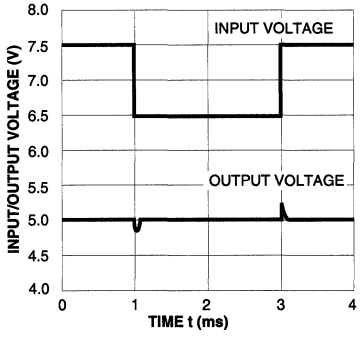


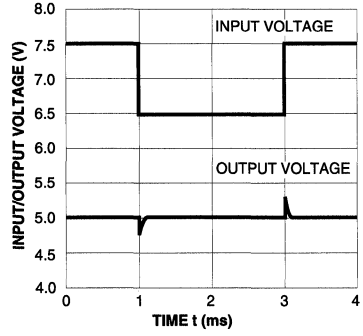
7) Dropout Voltage vs. Output Voltage (Set up Voltage)



8) Line Transient Response 1 (IOUT = 1mA)

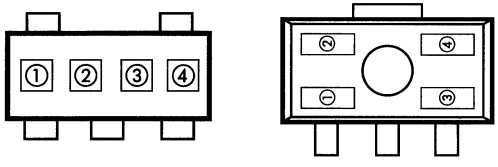


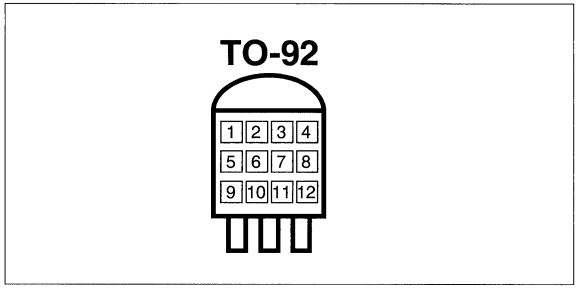
9) Line Transient Response 2 (IOUT = 10mA)



TC46

MARKING





a represents first decimal place of voltage

Mark a	Volt	Mark a	Volt
0	b.0 (V)	5	b.5 (V)
1	b.1 (V)	6	b.6 (V)
2	b.2 (V)	7	b.7 (V)
3	b.3 (V)	8	b.8 (V)
4	b.4 (V)	9	b.9 (V)

b represents first digit of voltage

Mark b	Volt
B	2. a (V)
C	3. a (V)
D	4. a (V)
E	5. a (V)
F	6. a (V)

c and d represent assembly lot number

a, b, c & d represent 46LR: Fixed

e represents first digit of voltage

Mark e	Volt	Mark e	Volt
2	2.f (V)	5	5.f (V)
3	3.f (V)	6	6.f (V)
4	4.f (V)		

f represents first decimal place of voltage

Mark f	Volt	Mark f	Volt
0	e .0 (V)	5	e .5 (V)
1	e.1 (V)	6	e .6 (V)
2	e.2 (V)	7	e .7 (V)
3	e.3 (V)	8	e .8 (V)
4	e.4 (V)	9	e .9 (V)

g Extra Feature Code: Fixed: 0

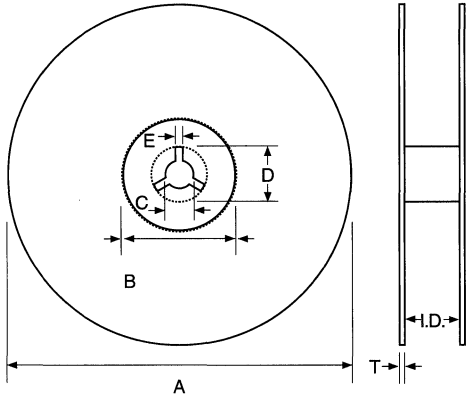
h represents regulation accuracy

Mark h	Regulation Accuracy
3	±2.5% (Standard)

i, j, k & l represent assembly lot number

TC46

TAPING REEL



	SOT-23-5	SOT-89	TO-92
A	178 ±1.0	178 ±2.0	360
B	60 ±2.0	80 ±1.0	80
C	13 ±0.2	13 ±0.05	30
D	22 ±0.5	21 ±0.5	45
E	2 ±0.2	2 ±0.2	2
I.D.	8.5 ±1.5	14.0 +1/-1.5	43
T	1.5 ±0.3	2.0 ±0.5	5

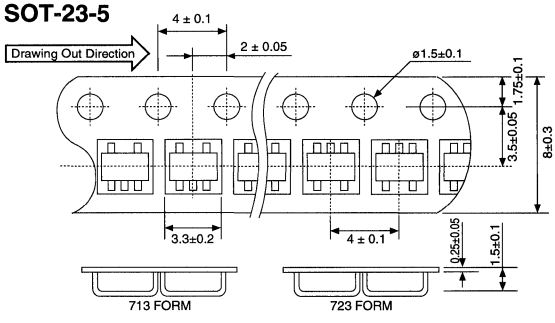
(unit = mm)

Reel Materials: SOT-23-5/SOT-89: Plastic
TO-92: Cardboard + Plastic Hub

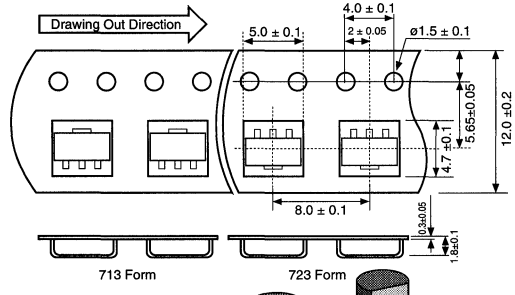
SOT-89: 1,000 pcs/Reel
TO-92: 2,000 pcs/Reel
SOT-23-5: 3,000 pcs/Reel

TAPING FORM

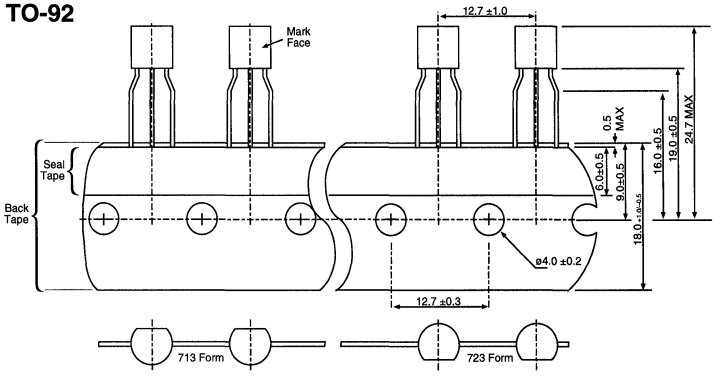
SOT-23-5

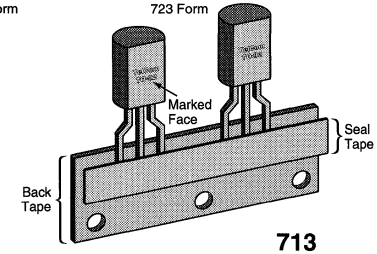


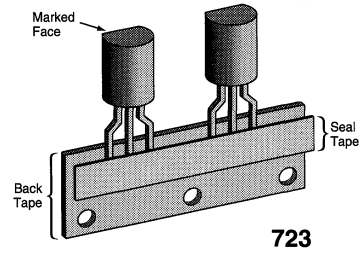
SOT-89-3



TO-92







TelCom Semiconductor, Inc.

VOLTAGE REGULATOR CONTROLLER

FEATURES

- **Low Supply Current ..... 50μA Typ (TC4730A)**
- **Standby Quiescent Current ..... 0.2μA Typ (TC4730A)**
- **Low Dropout Voltage ..... 0.1V Typ (I_{OUT} = 100mA: with External Tr.)**
- **High Line Regulation ..... 0.1%/V Typ**
- **Broad Output Voltage Range ..... 2.0V to 6.0V in 0.1V steps**
- **High Accuracy Output Voltage ..... ±2.5%**
- **Small Package ..... SOT-23-5 (Mini-mold)**

APPLICATIONS

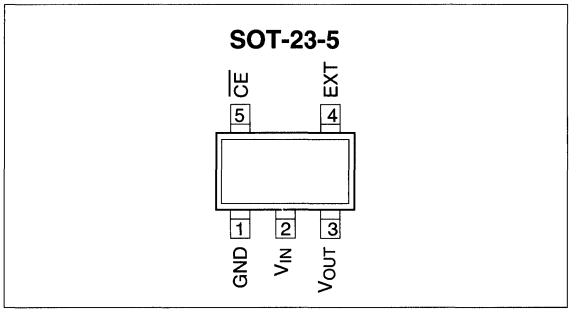
- **Regulator Control IC for a variety of external low V_{CE} (sat) transistors**

GENERAL DESCRIPTION

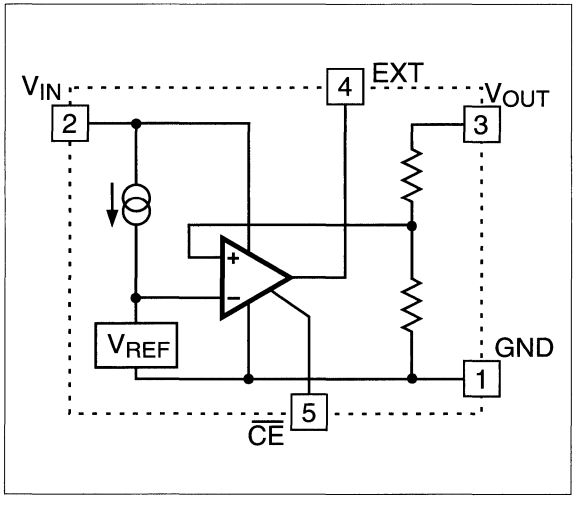
The TC47 Series are CMOS voltage regulator controller ICs for use with an external power transistor. They feature high output voltage accuracy (±2.5%) and low supply current. Each is composed of a voltage reference unit, an error amplifier and precision laser-trimmed resistors. These ICs are suitable for constructing regulators with extremely low dropout voltage and an output current in the range of several tens to several hundreds of mA. Furthermore, these ICs have a chip enable function, so that the supply current on standby can be minimized. The SOT-23-5 package ensures that the entire regulator will be minimally larger than the power transistor alone.

3

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART CODE TC47BR XX X X X XX XXX

Output Voltage:
Ex: 20 = 2.0V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance:
3: ± 2.5%

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
CT: SOT-23-5

Taping Direction:
723: Left Taping
713: Right Taping

TC47 Series

ABSOLUTE MAXIMUM RATINGS

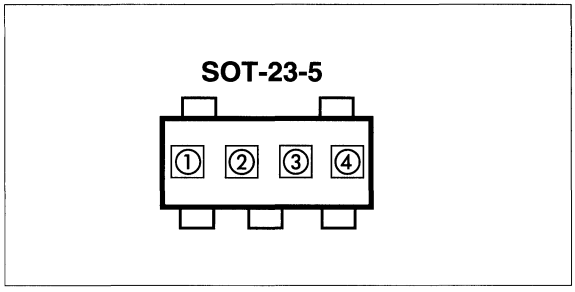
Parameter	Symbol	Limit	Unit
Input Voltage	V_{IN}	+12	V
Input Voltage ($\overline{CE}$ Pin)	V_{CE}	– 0.3 to (V_{IN} + 0.3)	V
EXT Output Voltage	V_{EXT}	+12	V
EXT Output Current	I_{EXT}	50	mA
Power Dissipation	P_D	150	mW
Operating Temperature Range	T_A	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Lead Temperature (Soldering)	T_{solder}	260°C, 10 sec	–

ELECTRICAL CHARACTERISTICS: (T_A = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage	I_{OUT} = 50mA	V_{OUT} x 0.975		V_{OUT} x 1.025	V
I_{OUT}	Output Current	$V_{IN} - V_{OUT}$ = 1.0V (Note 1)		1000		mA
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$V_{IN} - V_{OUT}$ = 1.0V 1mA ≤ I_{OUT} ≤ 100mA	– 60		60	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 100mA		100	200	mV
I_{SS}	Supply Current	$V_{IN} - V_{OUT}$ = 1.0V No Load		50	80	µA
$I_{STANDBY}$	Supply Current (Standby)	V_{IN} = 8.0V No Load	0.01	0.2	1.0	µA
$I_{EXTLEAK}$	EXT Leakage Current				0.5	µA
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	I_{OUT} = 50mA V_{OUT} + 0.5V ≤ V_{IN} ≤ 8.0V	0	0.1	0.3	%/V
V_{IN}	Input Voltage				8.0	V
V_{EXT}	EXT Output Voltage				8.0	V
$\frac{\Delta V_{OUT}}{\Delta T}$	Output Voltage Temperature Coefficient	I_{OUT} = 10mA – 40°C ≤ T_A ≤ 85°C		±100		ppm/°C
V_{CEH}	$\overline{CE}$ Input Voltage "H"		1.5			V
V_{CEL}	$\overline{CE}$ Input Voltage "L"				0.25	V
I_{CEH}	$\overline{CE}$ Input Current "H"			0	– 0.1	µA
I_{CEL}	$\overline{CE}$ Input Current "L"		5	3	0.1	µA

Note: 1. The output current depends upon the performance of the external PNP transistor. Use a low saturation type, with an h_{FE} of 100 or more.

MARKING



① represents first digit of voltage

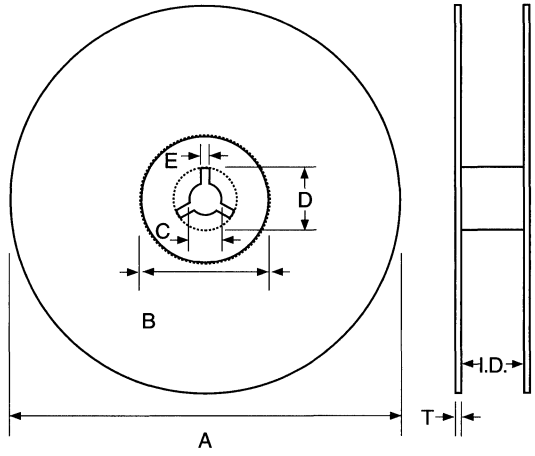
Mark①	Volt
J	2.②(V)
K	3.②(V)
L	4.②(V)
M	5.②(V)
N	6.②(V)

② represents first decimal place of voltage

Mark②	Volt	Mark②	Volt
0	①.0(V)	5	①.5(V)
1	①.1(V)	6	①.6(V)
2	①.2(V)	7	①.7(V)
3	①.3(V)	8	①.8(V)
4	①.4(V)	9	①.9(V)

③and④represent assembly lot number

TAPING REEL



SOT-23-5: 3,000 pcs/Reel

	SOT-23-5	
A	178	±1.0
B	60	±2.0
C	13	±0.2
D	22	±0.5
E	2	±0.2
I.D.	8.5	±1.5
T	1.5	±0.3

(unit = mm)

Reel Materials: Plastic

3

OPERATION

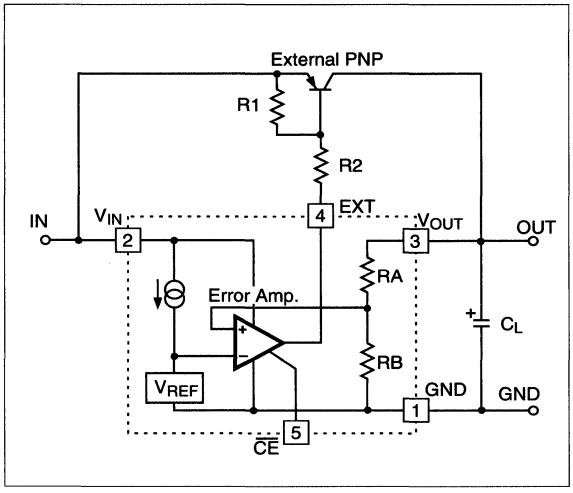


Figure 1

SELECTION GUIDE FOR EXTERNAL COMPONENTS

1. External PNP Transistor

The external PNP should have low V_{CE} (sat) and high h_{FE} at the desired I_{OUT}. If V_{IN} is not close to V_{OUT}, the package must be able to dissipate the heat.

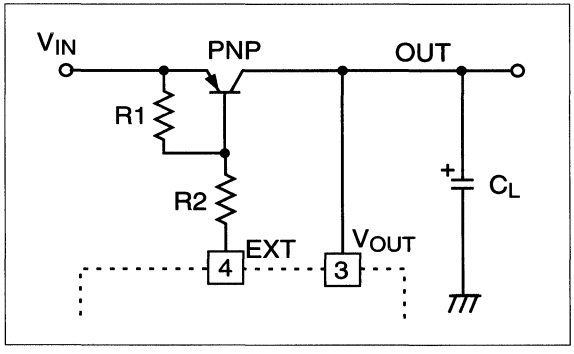


Figure 2. R1 approximately 10k.

2. Base Resistor R2

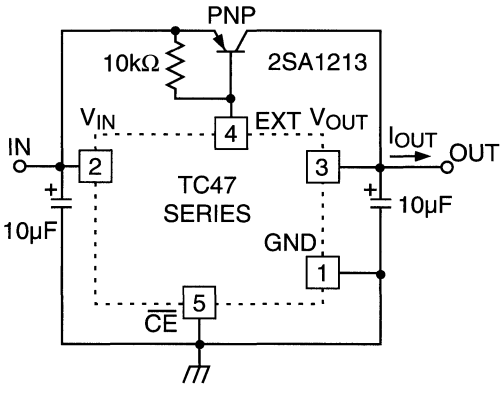
The EXT Pin of these ICs is protected by a current limit circuit. However, since this circuit protects the IC, use a resistor R2 to protect the external transistor, although this IC is operable without such a resistor. R2 is calculated with the input voltage, output voltage, output current, temperature, and the h_{FE} value (and their tolerances) taken into consideration. The following must also be satisfied:

$$\frac{V_{IN}\,[min] - 1.2(V)}{R2} - \frac{0.7(V)}{R1} > \frac{I_{OUT}\,[max]}{h_{FE}}$$

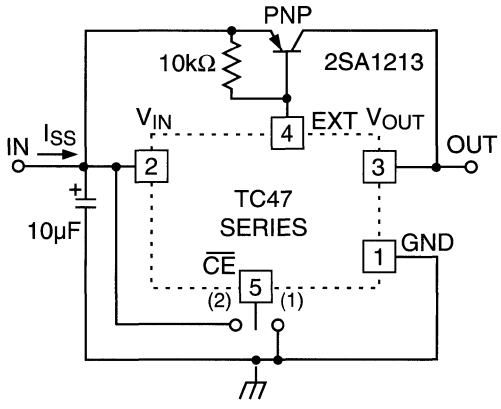
3. Phase Compensation

In these ICs, phase compensation is required for stable operation. For this purpose, be sure to use a capacitor C_L with a value of 10μF or more (preferably tantalum) and a resistor R1 of about 10kΩ between the base and the emitter.

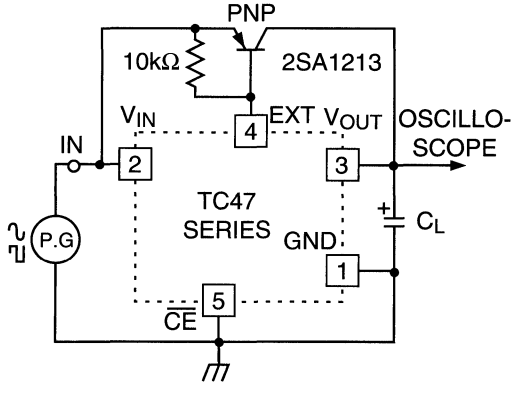
TEST CIRCUITS



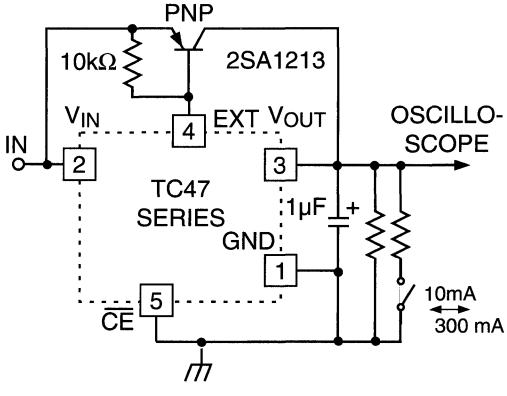
STATIC CHARACTERISTICS TEST (Except QUIESCENT CURRENT, STANDBY CURRENT)



QUIESCENT CURRENT (1), STANDBY CURRENT TEST



RIPPLE REJECTION, LINE TRANSIENT RESPONSE TEST

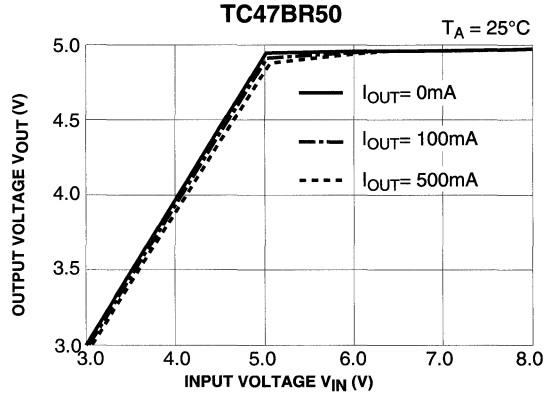


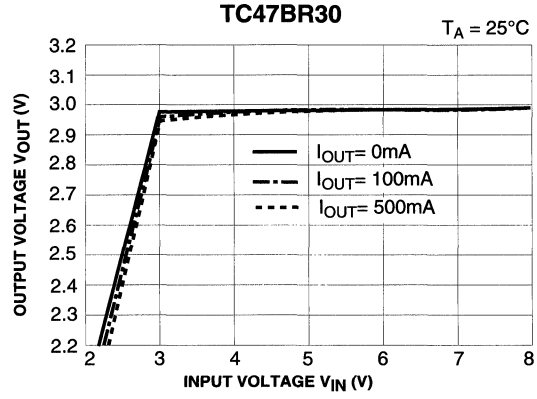
LOAD TRANSIENT RESPONSE TEST

TC47 Series

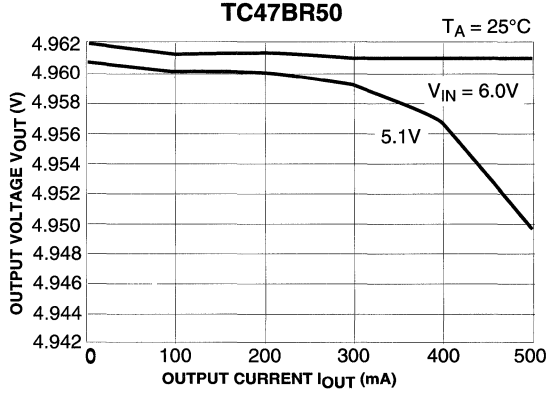
TYPICAL CHARACTERISTICS

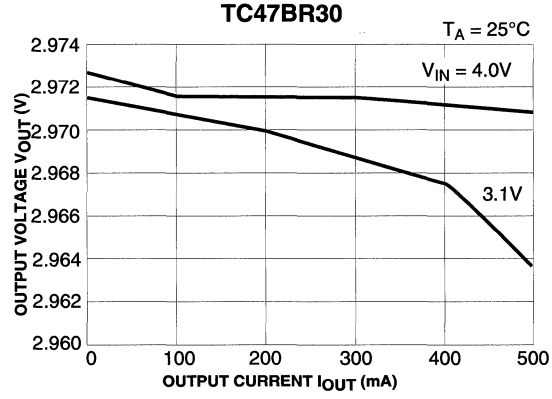
1) Output Voltage vs. Input Voltage



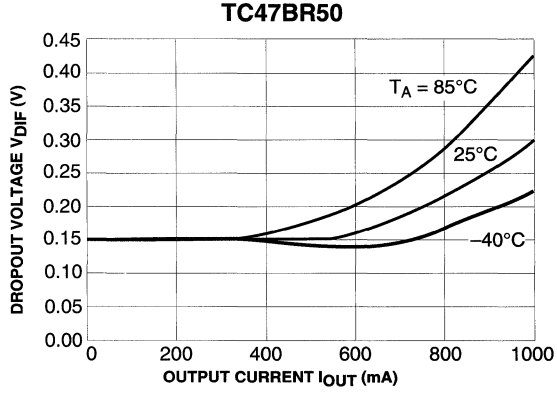


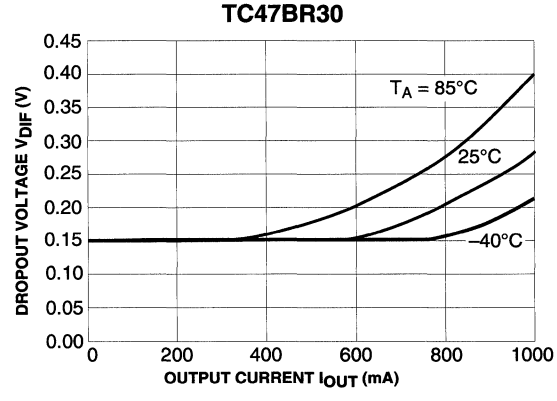
2) Output Voltage vs. Output Current





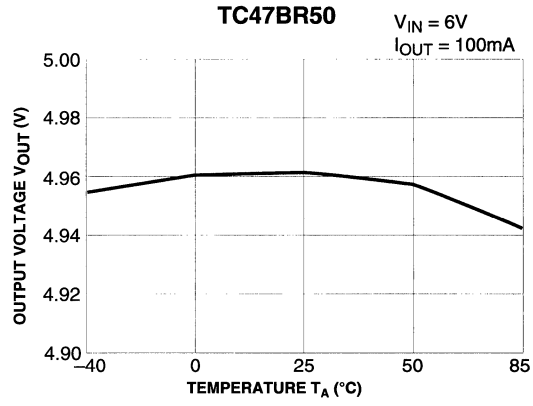
3) Dropout Voltage vs. Output Current

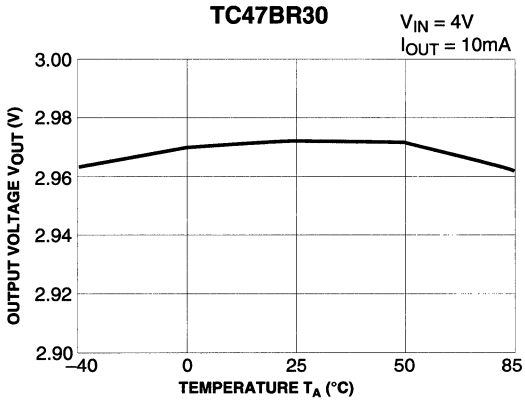




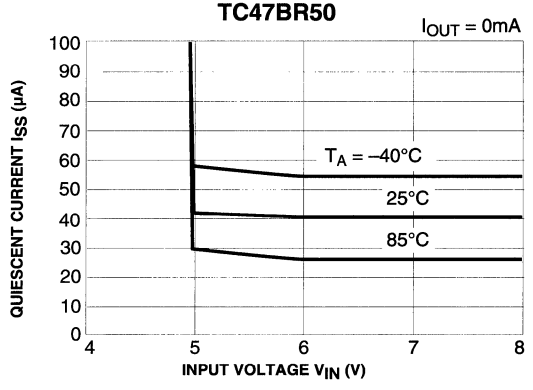
TYPICAL CHARACTERISTICS (CONT.)

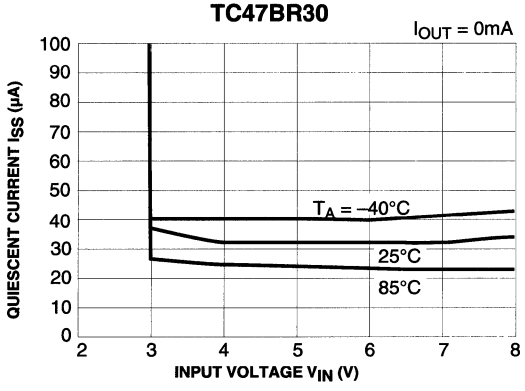
4) Output Voltage vs. Temperature



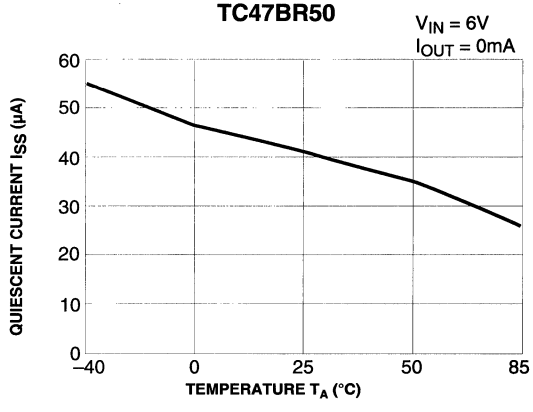


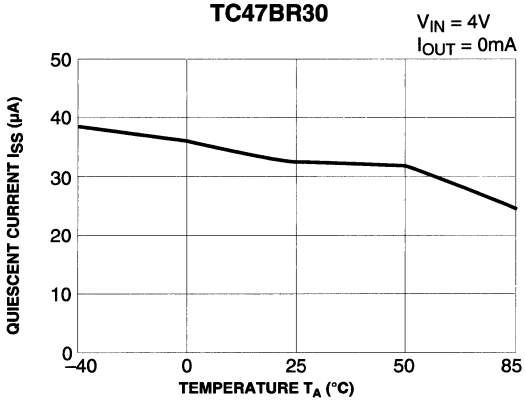
5) Quiescent Current vs. Input Voltage





6) Quiescent current vs. Temperature

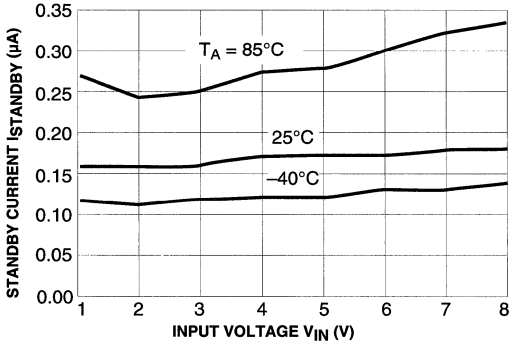




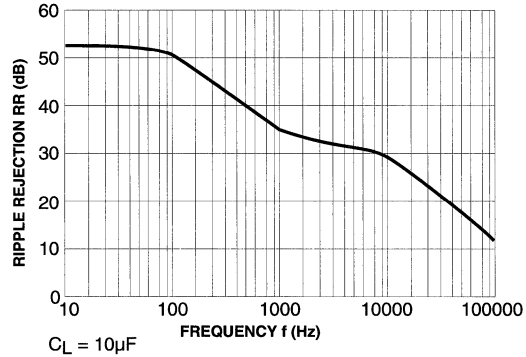
TC47 Series

TYPICAL CHARACTERISTICS (CONT.)

7) Standby Current vs. Input Voltage

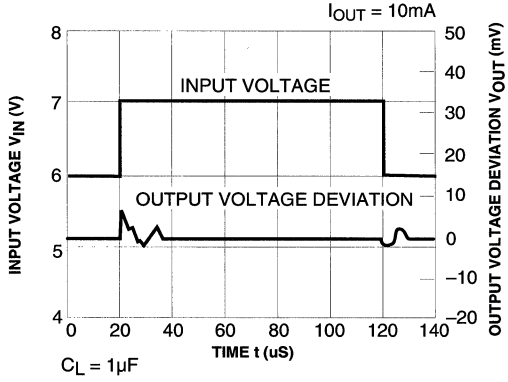


8) Ripple Rejection (T_A = 25°C)



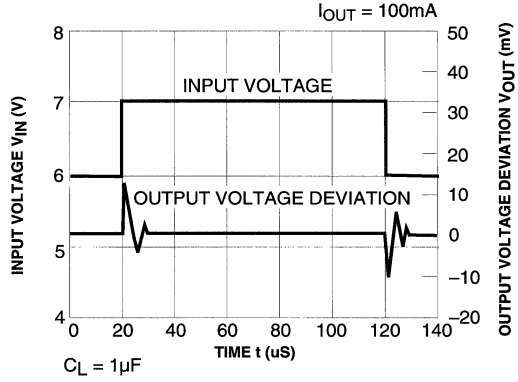
C_L = 10μF
I_{OUT} = 200mA
V_{IN} = 6Vdc + 0.5 (p-p)

9) Line Transient Response (1) (T_A = 25°C)



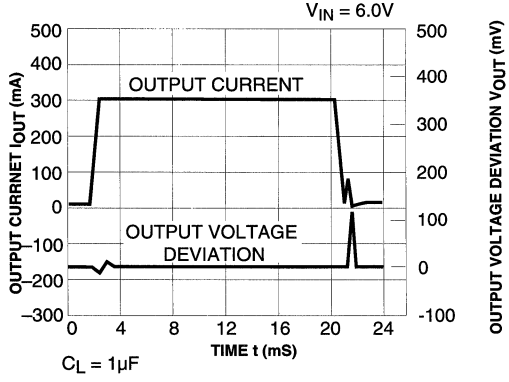
C_L = 1μF

10) Line Transient Response (2) (T_A = 25°C)



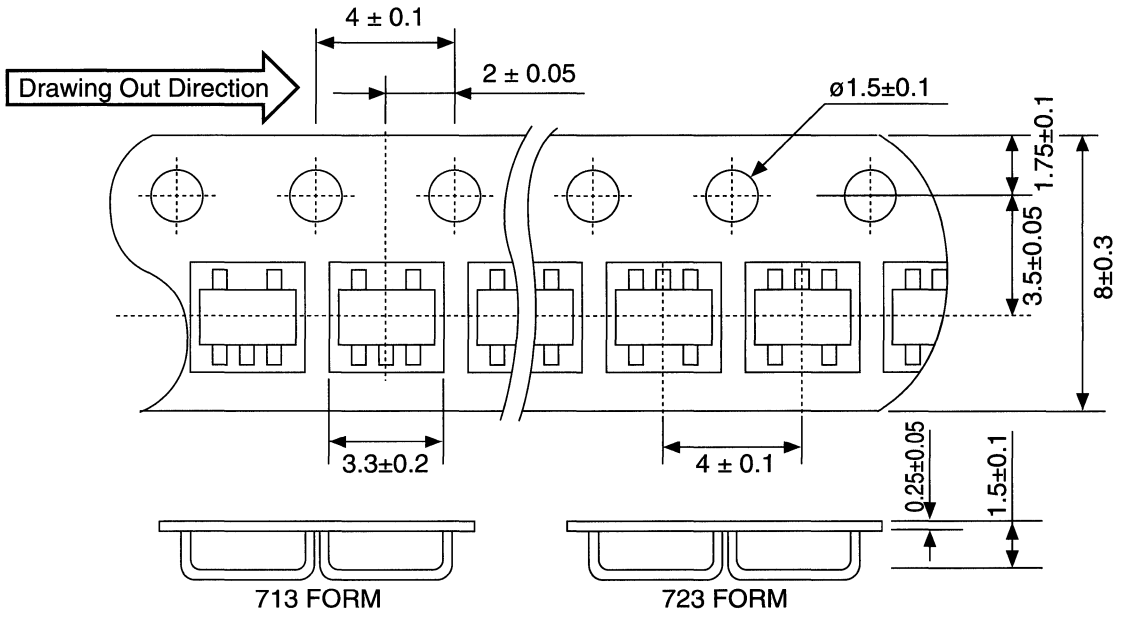
C_L = 1μF

11) Load Transient Response (T_A = 25°C)



C_L = 1μF

TAPING FORM



SOT-23-5

LOW DROPOUT POSITIVE VOLTAGE REGULATOR

FEATURES

- **Very Low "Dropout" Voltage 120mV typ at 100mA 380mV typ at 200mA**
- **High Output Current ..... 250mA (V_{OUT}=5.0V)**
- **High Accuracy Output Voltage ..... ±2% (±1% Semicustom Version)**
- **Wide Output Voltage Range 2.1V-6.0V**
- **Low Power Consumption ..... 1.1μA (V_{OUT}=5.0V) (at NO LOAD)**
- **Good Temperature Stability ..... ±100ppm/°C Typ**
- **Good Voltage Regulation ..... 0.1%/V Typ**
- **Package Options ..... SOT-23-3 (150mW) Surface Mount SOT-89-3 (500mW) Surface Mount TO-92 Through-hole Package**
- **Short Circuit Protected**
- **Custom voltages available from 2.1V to 6.0V (in 0.1V steps).**

APPLICATIONS

- **Battery-Powered Devices**
- **Cameras and Portable Video Equipment**
- **Pagers and Cellular Phones**
- **Solar-Powered Instruments**
- **Portable Instruments**

GENERAL DESCRIPTION

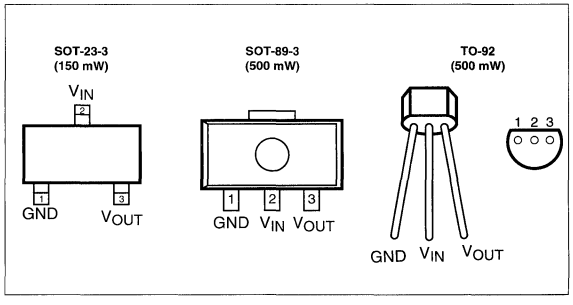
The TC55 Series is a collection of CMOS low dropout positive voltage regulators which can source up to 250mA of current with an extremely low input-output voltage differential of 380mV.

The low dropout voltage combined with the low current consumption of only 1.1 μA makes this part ideal for battery operation. The low voltage differential (dropout voltage) extends battery operating lifetime. It also permits high currents in small packages when operated with minimum V_{IN} - V_{OUT} differentials.

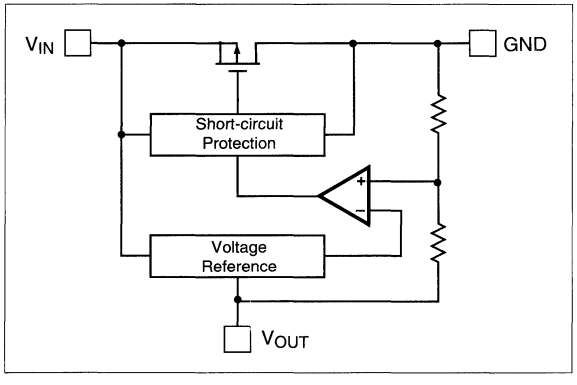
The circuit also incorporates short-circuit protection to ensure maximum reliability.

3

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART CODE TC55 RP XX X X X XX XXX

Output Voltage:
Ex: 21 = 2.1V; 60 = 6.0V

Extra Feature Code: Fixed: 0

Tolerance:
1 = ±1.0% (custom)
2 = ±2.0% (standard)

Temperature: E: – 40°C to +85°C

Package Type and Pin Count:
CB: SOT-23-3
MB: SOT-89-3
ZB: TO-92

Taping Direction:
723: Left Taping
713: Right Taping
no suffix: TO-92 Bulk

TC55 Series

ABSOLUTE MAXIMUM RATINGS

Item		Code	Ratings	Units
Input Voltage		V_{IN}	+12	V
Output Current		I_{OUT}	$Pd/(V_{IN} - V_{OUT})$	mA
Output Voltage		V_{OUT}	$(V_{SS} - 0.3)$ to $(V_{IN} + 0.3)$	V
Power Dissipation	SOT-23 SOT-89 TO-92	Pd	150 500 500	mW
Operating Temperature Range		T_A	– 40 to +85	°C
Storage Temperature Range		T_{stg}	– 65 to +150	°C

TC55RP50 ELECTRICAL CHARACTERISTICS:

$V_{OUT}(S) = 5.0V$, $T_A = 25°C$ (see REMARKS)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{OUT}(A)$	Output Voltage	$I_{OUT} = 40$ mA $V_{IN} = 6.0V$	x 0.98 4.90	$V_{OUT}(S)$ 5.0	x 1.02 5.10	V
$I_{OUT}max$	Maximum Output Current	$V_{IN} = 6.0V$, $V_{OUT}(A) \geq 4.5V$	250			mA
ΔV_{OUT}	Load Regulation	$V_{IN} = 6.0$ V, 1 mA $\leq I_{OUT} \leq$ 100 mA		40	80	mV
V_{dif}	I/O Voltage Difference	$I_{OUT} = 100$ mA $I_{OUT} = 200$ mA		120 380	300 600	mV
I_{SS}	Current Consumption	$V_{IN} = 6.0V$		1.1	3.0	µA
$\frac{V_{OUT}(A) \cdot 100}{\Delta V_{IN} \cdot V_{OUT}(S)}$	Voltage Regulation	$I_{OUT} = 40$ mA $6.0V \leq V_{IN} \leq 10.0V$		0.2	0.3	%/V
V_{IN}	Input Voltage				10.0	V
$\frac{\Delta V_{OUT}(A) \cdot 10^6}{V_{OUT}(S) \cdot \Delta T_A}$	Temperature Coefficient of Output Voltage	$I_{OUT} = 40$ mA $-40°C \leq T_A \leq 85°C$		±100		ppm/°C

REMARKS: $V_{OUT}(S)$: Preset value of Output voltage
$V_{OUT}(A)$: Actual value of Output voltage
V_{dif}: Definition of I/O voltage difference = $\{V_{IN}1 - V_{OUT}(A)\}$
$V_{OUT}(A)$: Output Voltage when I_{OUT} is fixed and $V_{IN} = V_{OUT}(S) + 1.0V$
$V_{IN}1$: Input Voltage when the output voltage is 98% $V_{OUT}(A)$

TC55RP40 ELECTRICAL CHARACTERISTICS:

$V_{OUT}(S) = 4.0V$, $T_A = 25°C$ (see REMARKS)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{OUT}(A)$	Output Voltage	$I_{OUT} = 30$ mA $V_{IN} = 5.0V$	x 0.98 3.92	$V_{OUT}(S)$ 4.0	x 1.02 4.08	V
$I_{OUT}max$	Maximum Output Current	$V_{IN} = 5.0V$, $V_{OUT}(A) \geq 3.6V$	200			mA
ΔV_{OUT}	Load Regulation	$V_{IN} = 5.0$ V, 1 mA $\leq I_{OUT} \leq$ 100 mA		45	90	mV
V_{dif}	I/O Voltage Difference	$I_{OUT} = 100$ mA $I_{OUT} = 200$ mA		170 400	330 630	mV
I_{SS}	Current Consumption	$V_{IN} = 5.0V$		1.0	2.9	µA
$\frac{\Delta V_{OUT}(A) \cdot 100}{\Delta V_{IN} \cdot V_{OUT}(S)}$	Voltage Regulation	$I_{OUT} = 30$ mA $5.0V \leq V_{IN} \leq 10.0V$		0.2	0.3	%/V
V_{IN}	Input Voltage				10.0	V
$\frac{\Delta V_{OUT}(A)}{V_{OUT}(S) \cdot \Delta T_A}$	Temperature Coefficient of Output Voltage	$I_{OUT} = 30$ mA $-40°C \leq T_A \leq 85°C$		±100		ppm/°C

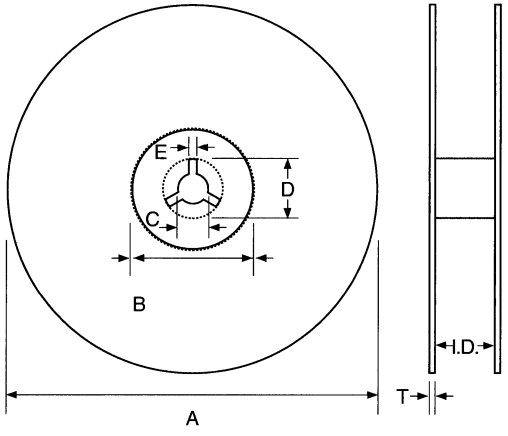
TC55RP30 ELECTRICAL CHARACTERISTICS:

$V_{OUT}(S)$ = 3.0V, T_A = 25°C (see REMARKS)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{OUT}(A)$	Output Voltage	I_{OUT} = 20 mA V_{IN} = 4.0V	x 0.98 2.94	$V_{OUT}(S)$ 3.0	x 1.02 3.06	V
$I_{OUT}max$	Maximum Output Current	V_{IN} = 4.0V, $V_{OUT}(A) \geq 2.7V$	150			mA
ΔV_{OUT}	Load Regulation	V_{IN} = 4.0V, 1 mA ≤ I_{OUT} ≤ 80 mA		45	90	mV
V_{dif}	I/O Voltage Difference	I_{OUT} = 80 mA I_{OUT} = 160 mA		180 400	360 700	mV
I_{SS}	Current Consumption	V_{IN} = 4.0V		0.9	2.8	µA
$\frac{V_{OUT}(A)\cdot 100}{\Delta V_{IN}\cdot V_{OUT}(S)}$	Voltage Regulation	I_{OUT} = 20 mA 4.0V ≤ V_{IN} ≤ 10.0V		0.2	0.3	%/V
V_{IN}	Input Voltage				10.0	V
$\frac{\Delta V_{OUT}(A)\cdot 10^6}{\Delta T_A\cdot V_{OUT}(S)}$	Temperature Coefficient of Output Voltage	I_{OUT} = 20 mA –40°C ≤ T_A ≤ 85°C		±100		ppm/°C

3

TAPING REEL



SOT-23-3: 3,000 pcs/Reel
SOT-89-3: 1,000 pcs/Reel
TO-92: 2,000 pcs/Reel

TAPING REEL

	SOT-23		SOT-89		TO-92
A	178	±1.0	178	±2.0	360
B	60	±2.0	80	±1.0	80
C	13	±0.2	13	±0.05	30
D	22	±0.5	21	±0.5	45
E	2	±0.2	2	±0.2	2
I.D.	8.5	±1.5	14.0	+1/-1.5	43
T	1.5	±0.3	2.0	±0.5	5

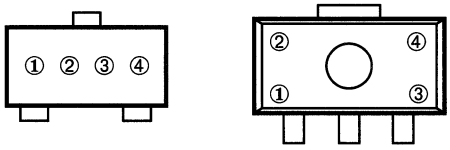
(unit = mm)

Reel Materials: SOT-23/SOT-89: Plastic
TO-92: Cardboard + Plastic Hub

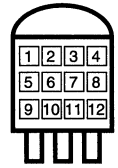
TC55 Series

MARKING

SOT-23-3 **SOT-89-3**



TO-92



① represents first voltage digit
2 3 4 5 6
ex: 3.X = ○○③○

② first voltage decimal (0-9)
ex: 3.4 = ○○③④

③ represents tolerance/feature code
1= ±1.0% (custom)
2 = ±2.0% (standard)

④ represents assembly lot number

①, ② & ③ = 55R_ (fixed)

④ = output voltage polarity : P : positive

⑤ = first voltage digit (2-6)

⑥ = first voltage decimal (0-9)

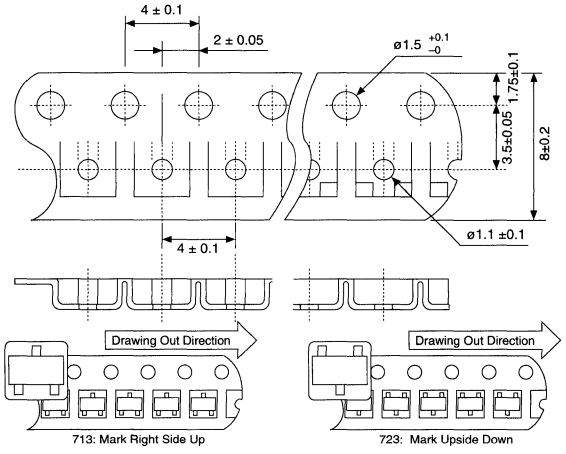
⑦ = extra feature code : fixed : 0

⑧ = regulation accuracy
1 = ±1.0% (custom), 2 = ±2.0% (standard)

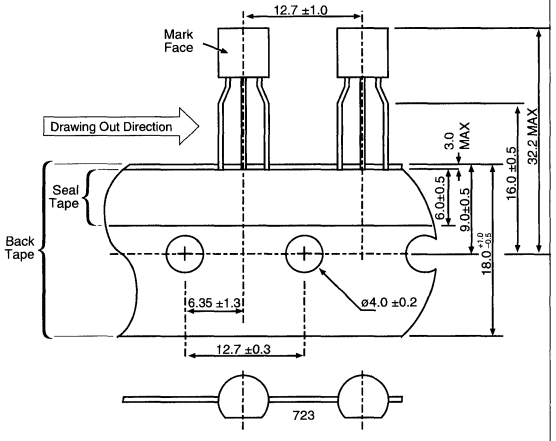
⑨, ⑩, ⑪ & ⑫ = assembly lot number

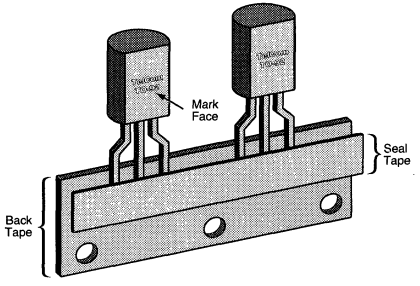
TAPING FORM

SOT-23-3

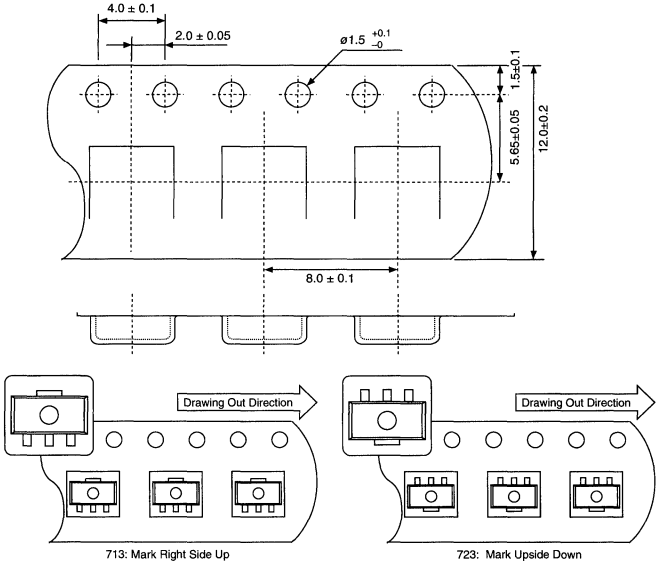


TO-92





SOT-89-3



3A OUTPUT PROGRAMMABLE POWER OSCILLATOR

FEATURES

- **Controllable Duty Cycle**
- **Wide Operating Range ..... 5V to 18V**
- **High Peak Output Current 3A**
- **High Capacitive Load Drive Capability ..... 1800pF in 20ns**
- **Short Delay Time ..... <150ns Typ**

APPLICATIONS

- **Fixed Frequency Power Oscillator**
- **Voltage Controlled Oscillator**
- **Low Power Buck Regulator Supply**
- **MOSFET Driver**
- **Simple diode inverters and doublers**

ORDERING INFORMATION

Part No.	Operating Package	Temp Range
TC96C555COA	8-Pin SOIC	0°C to +70°C
TC96C555EOA	8-Pin SOIC	– 40°C to +85°C
TC96C555CPA	8-Pin Plastic DIP	0°C to +70°C
TC96C555EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC96C555MJA	8-Pin CerDIP	– 55°C to +125°C

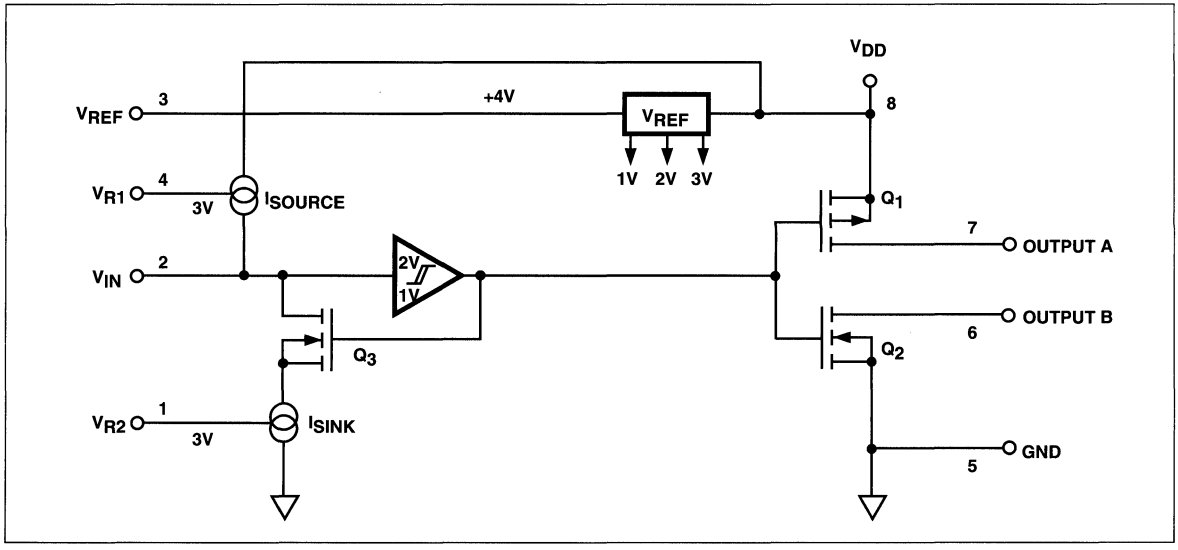
GENERAL DESCRIPTION

The TC96C555 Power Oscillator is an easily programmed IC that can be used in simple switch-mode power supplies, diode doublers and inverters, and similar circuits where high-current pulses are needed in an economical form.

The TC96C555 uses TelCom Semiconductors' new Tough CMOS™ process. The output drive capability is similar to the TC4423/4/5 MOSFET Drivers, which can switch in 25ns into a capacitive load of 1,800pF. The TC96C555 will not latch up under any conditions within their power and voltage ratings. They can accept, without damage, up to 1.5A of reverse current (of either polarity) being forced back into the output. All terminals are also fully protected against up to 4kV of electrostatic discharge. The peak output is rated at 3A. Split outputs permits driving of an external pair of MOSFETS, with controllable cross conduction between upper and lower devices.

3

FUNCTIONAL BLOCK DIAGRAM



TC96C555

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage, Pin 1 or 4 ..... V_{DD} +0.3 to GND –0.3
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Package Thermal Resistance
- CerDIP $R_{\Theta J-A}$ ..... 150°C/W
- CerDIP $R_{\Theta J-C}$ ..... 50°C/W
- PDIP $R_{\Theta J-A}$ ..... 125°C/W
- PDIP $R_{\Theta J-C}$ ..... 42°C/W
- SOIC $R_{\Theta J-A}$ ..... 155°C/W
- SOIC $R_{\Theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Power Dissipation
- Plastic 1000mW
- CerDIP 800mW
- SOIC 500mW

ELECTRICAL CHARACTERISTICS: unless otherwise specified T_A = +25°C with 5V ≤ V_{DD} ≤ 18V:

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Programmable Current Range						
Pin 4 Input Current for I_{SOURCE} Control		$(V_{REF} - V_{R1}) / R_{CHG}$ Fig. 2	5.0	–	150	µA
Pin 1 Input Current for I_{SINK} Control		$(V_{REF} - V_{R2}) / R_{DIS}$ Fig. 2	5.0	–	150	µA
Reference Section						
V_{REF}		V_{DD} = 15V, I_{REF} = 10µA	3.8	4	4.2	V
Line Regulation of V_{REF}		V_{DD} = 7V to 18V	–	0.6	1	%/V
Load Regulation of V_{REF}		I_{REF} = 0 to 1mA	–	0.1	0.2	%/mA
V_{REF} Drift Over Lifetime	V_{DRIFT}		–	–	5	%
V_{REF} Tempco	TCV_{REF}	– 55 ≤ Temp ≤ 125°C	–	1100	2000	ppm/°C
Voltage at Pin 1 & 4	V_{R1}, V_{R2}	V_{DD} = 15V	2.85	3.0	3.15	V
Voltage Across R_{CHG} and R_{DIS}	$V_{REF} - V_R$		0.85	1	1.15	V
Pin 2, High Switching Threshold	V_{ih}	V_{DD} = 15V	1.8	2	2.2	V
Pin 2, Low Switching Threshold	V_{il}	V_{DD} = 15V	0.8	1	1.2	V
Delta High to Low Threshold	$V_{ih} - V_{il}$	V_{DD} = 15V	0.9	1.0	1.1	V
V_{REF} Pin 3 Short to GND Pin 5	I_{REF}	V_{DD} = 15V	–	8	15	mA

ELECTRICAL CHARACTERISTICS: unless otherwise specified T_A = +25°C with 10V ≤ V_{DD} ≤ 18V:

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator						
Voltage Stability		V_{DD} = 7 to 18V	–	1	5	%/V
Temperature Stability		– 55 ≤ Temp ≤ 125°C	–	0.4	–	%/°C
Power Supply						
Power Supply Current	I_{DD}	0 ≤ V_{IN} ≤ 3V	–	2	3	mA
Switching Time[1]						
Rise Time	t_R	C1 = 1800pF	–	23	30	ns
Fall Time	t_F	C1 = 1800pF	–	20	30	ns
Delay Time	t_{D1}	C1 = 1800pF	–	140	180	ns
Delay Time	t_{D2}	C1 = 1800pF	–	100	140	ns
Output						
High Output Voltage	V_{OH}		V_{DD} – 0.025	–	–	V
Low Output Voltage	V_{OL}		–	–	0.025	V
Output Res Hi State	R_O	V_{DD} = 15V	–	3.5	5	Ω
Output Res Lo State	R_O	V_{DD} = 15V	–	2.5	5	Ω
Peak Output Current	I_{PK}	V_{DD} = 18V	–	3	–	A

ELECTRICAL CHARACTERISTICS: specifications over operating temperature range unless otherwise specified $5.0V < V_{DD} < 18V$:

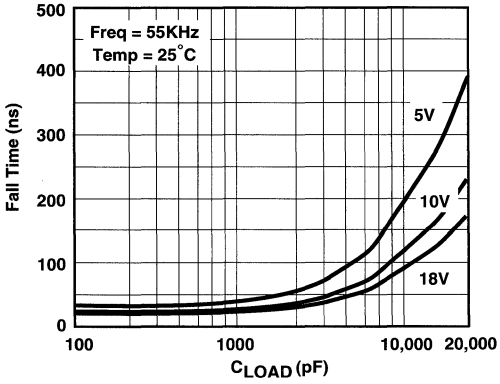
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Programmable Current Range						
Pin 4 Input Current for I_{SOURCE} Control		$(V_{REF}-V_{R1}) / R_{CHG}$ Fig. 2	5.0	–	100	µA
Pin 1 Input Current for I_{SINK} Control		$(V_{REF}-V_{R2}) / R_{DIS}$ Fig. 2	5.0	–	100	µA
Reference Section						
V_{REF}	V_{DD} = 15V	I_{REF} = 10µA	3.6	4	4.4	V
Line Regulation of V_{REF}	V_{DD} = 7 to 18V		–	0.9	1.5	%/V
Load Regulation of V_{REF}	I_{REF} = 0 to 1mA		–	0.1	0.4	%/mA
V_{REF} Drift Over Lifetime	V_{DRIFT}		–	–	5	%
V_{REF} Tempco	TCV_{REF}	– 55 ≤ Temp ≤ 125°C	–	1100	2000	ppm/°C
Voltage Pin at 1 and 4	V_{R1}, V_{R2}	V_{DD} = 15V	2.7	3	3.3	V
Voltage Across R_{CHG} and R_{DIS}	$V_{REF}-V_R$		0.8	1	1.2	V
Pin 2, High Switching Threshold	V_{ih}	V_{DD} = 15V	1.75	2	2.25	V
Pin 2, Low Switching Threshold	V_{il}	V_{DD} = 15V	0.75	1	1.25	V
Delta High to Low Threshold	V_{ih} to V_{il}	V_{DD} = 15V	0.9	1.0	1.1	V
V_{REF} Pin 3 Short to GND Pin 5	I_{REF}	V_{DD} = 15V	–	–	18	mA
Oscillator						
Voltage Stability		V_{DD} = 7V to 18V	–	1	8	%/V
Temperature Stability		– 55 ≤ Temp ≤ 125°C	–	0.4	–	%/°C
Power Supply						
Power Supply Current	I_{DD}	$0 \le V_{IN} \le 3V$	–	–	4	mA
Switching Time[1]						
Rise Time	t_R	C1 = 1800pF, Fig. 1	–	33	40	ns
Fall Time	t_F	C1 = 1800pF, Fig. 1	–	30	40	ns
Delay Time	t_{D1}	Fig. 1	–	180	220	ns
Delay Time	t_{D2}	Fig. 1	–	160	200	ns
Output						
High Output Voltage	V_{OH}		V_{DD} – 0.025	–	–	V
Low Output Voltage	V_{OL}		–	–	0.025	V
Output Res Hi State	R_O	V_{DD} = 15V	–	4.5	6	Ω
Output Res Lo State	R_O	V_{DD} = 15V	–	3.4	6	Ω
Peak Output Current	I_{PK}	V_{DD} = 18V	–	2	–	A

NOTE : [1]Switching times guaranteed by design.
The typical values are from 125°C measurements.

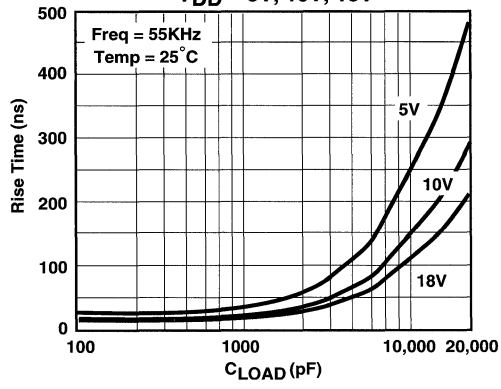
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Operational Specifications is not implied. Any exposure to Absolute Maximum Rating Conditions may affect device reliability.

TYPICAL CHARACTERISTICS CURVES

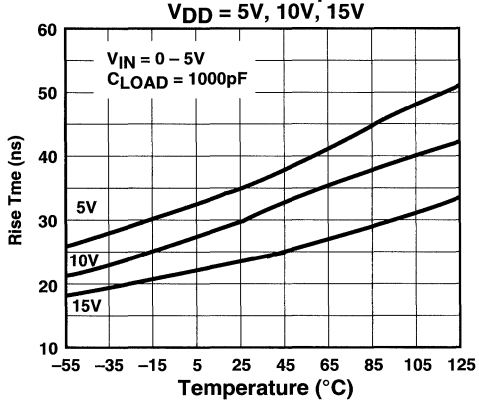
Fall Time vs. Capacitive Load
V_{DD} = 5V, 10V, 18V



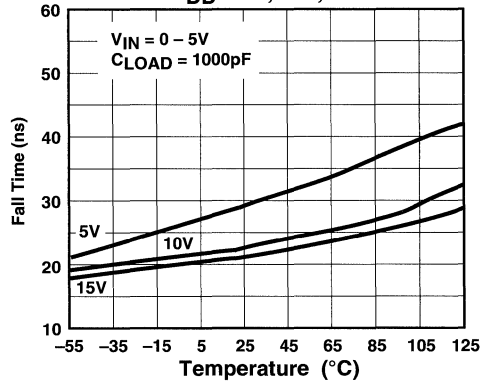
Rise TIme vs Capacitive Load
V_{DD} = 5V, 10V, 18V



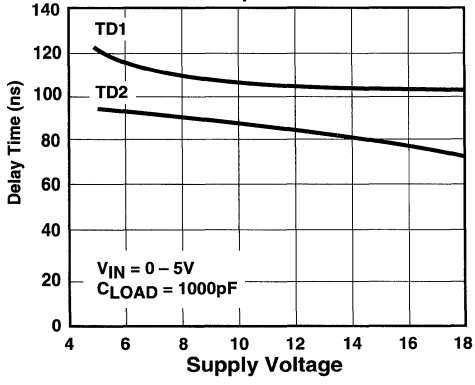
Rise Time vs. Temperature
V_{DD} = 5V, 10V, 15V



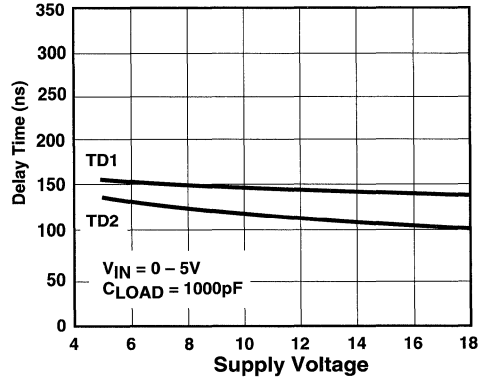
Fall Time vs. Temperature
V_{DD} = 5V, 10V, 15V



Delay Time vs Supply Voltage
Temp = –55°C

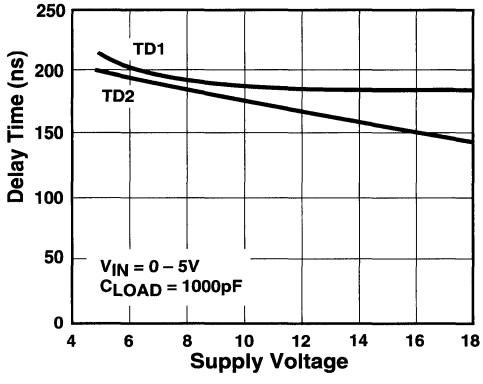


Delay Time vs Supply Voltage
Temp = 25°C

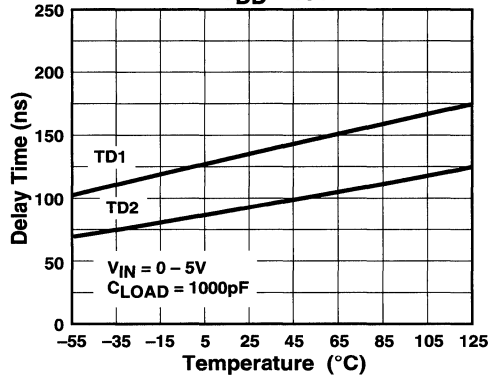


TYPICAL CHARACTERISTICS CURVES

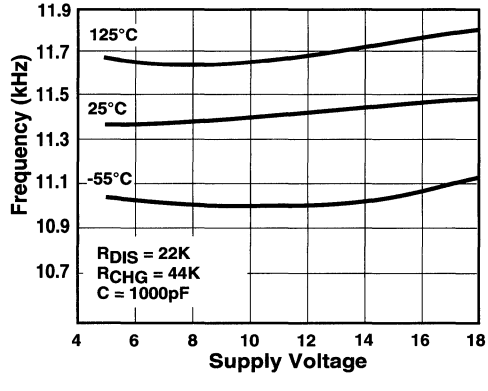
Delay Time vs Supply Voltage
Temp = 125°C



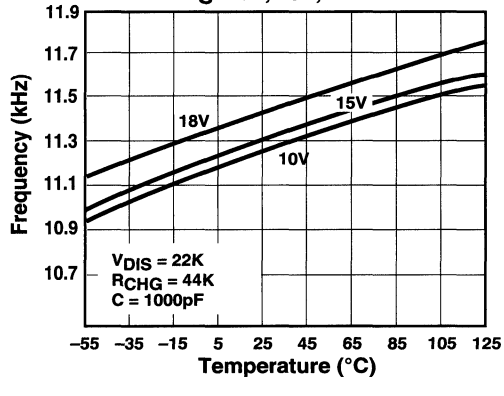
Delay Time vs. Temperature
V_{DD} = 18V



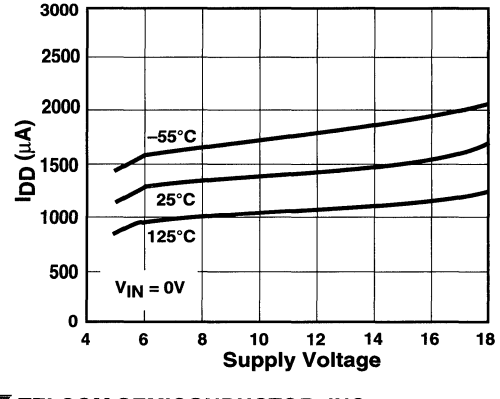
Oscillation Frequency vs Supply Voltage
Temp at 25°C, – 55°C, 125°C



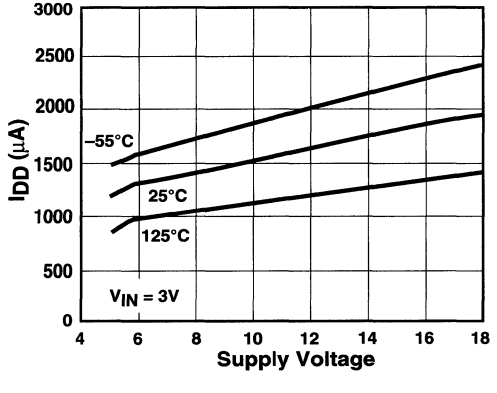
Oscillation Frequency vs Temperature
V_S = 5V, 10V, 18V



I_{DD} vs Supply Voltage
Temp = – 55°C, 25°C, 125°C

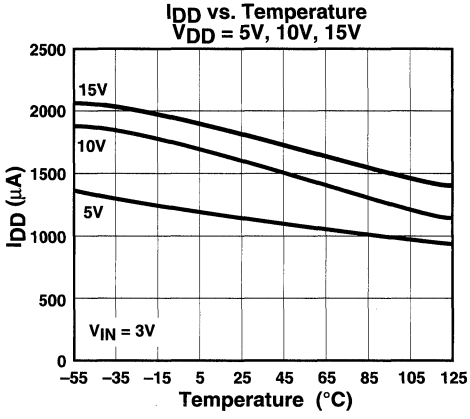


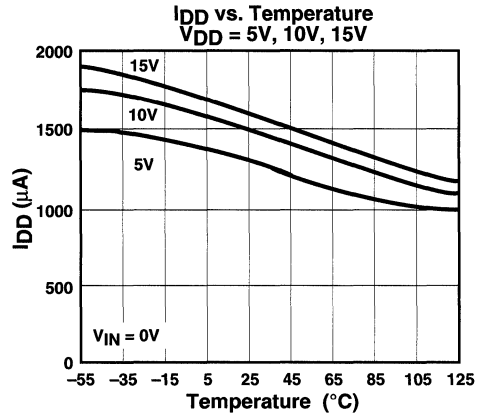
I_{DD} vs Supply Voltage
Temp = – 55°C, 25°C, 125°C

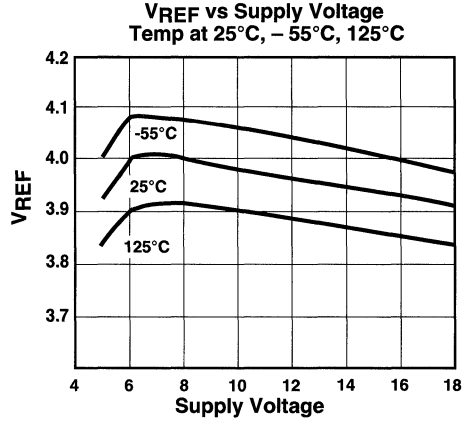


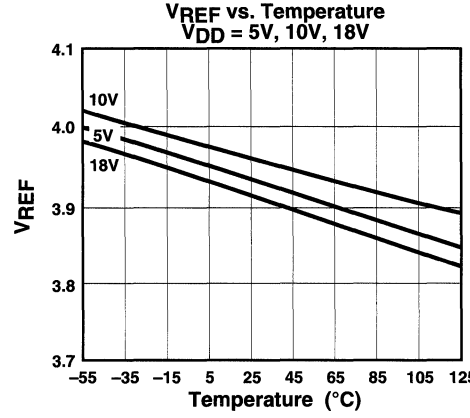
3

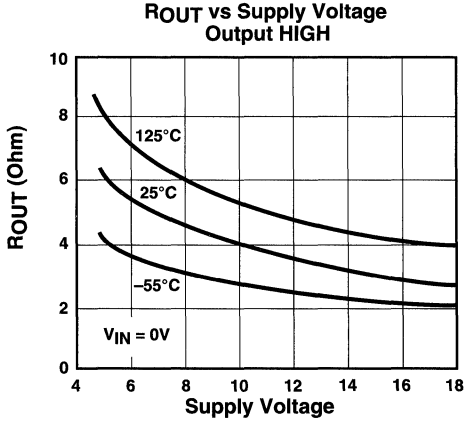
TYPICAL CHARACTERISTICS CURVES

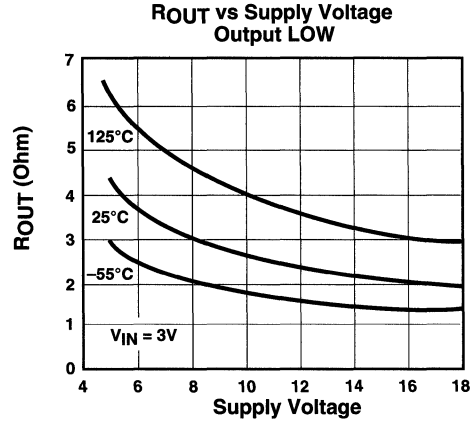




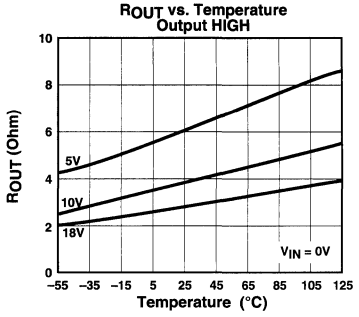


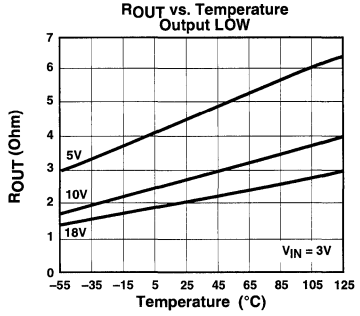






TYPICAL CHARACTERISTICS CURVES





3

APPLICATIONS

The oscillator timing can easily be controlled by two external resistors, R_{CHG} and R_{DIS}, and capacitor C. R_{CHG} and R_{DIS} set the two constant current sources for charging and discharging C. The source current is always flowing when in operation. When the capacitor has charged to a 2V threshold, the current sink circuit is enabled to discharge the capacitor to the 1V threshold. When 1V is reached, the current sink turns OFF to start another cycle.

Resistor R_{CHG} is connected from V_{REF} at Pin 3 to V_{R1} Pin 4 to program the charging current. Current is set with resistor R_{DIS} connected from V_{REF} Pin 3 to V_{R2} Pin 1. Both currents can range from 5µA to 150µA.

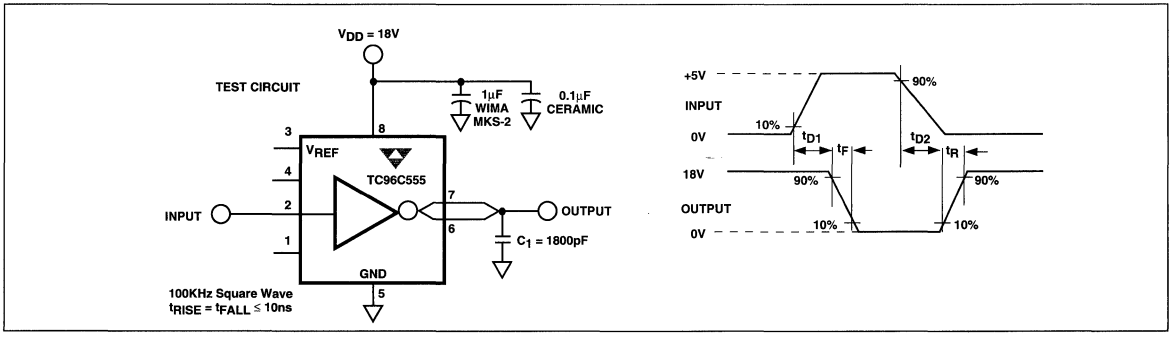


Figure 1 Output Switching Time

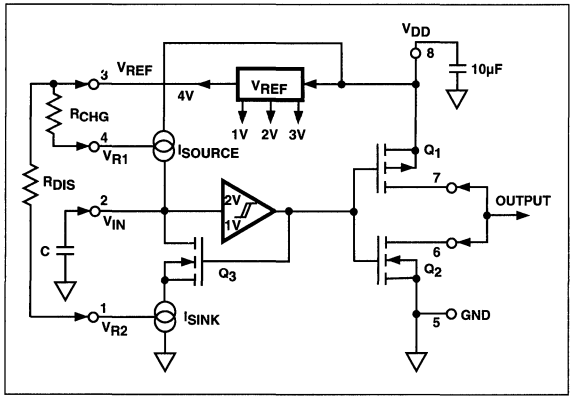


Figure 2 Fixed Frequency Power Oscillator

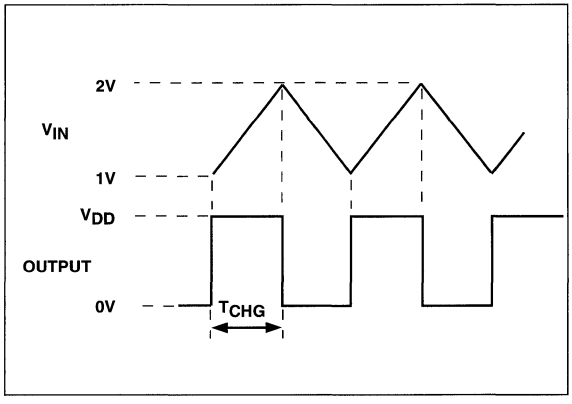


Figure 3 V_{IN} and Output Waveform

TC96C555

APPLICATIONS (cont.)

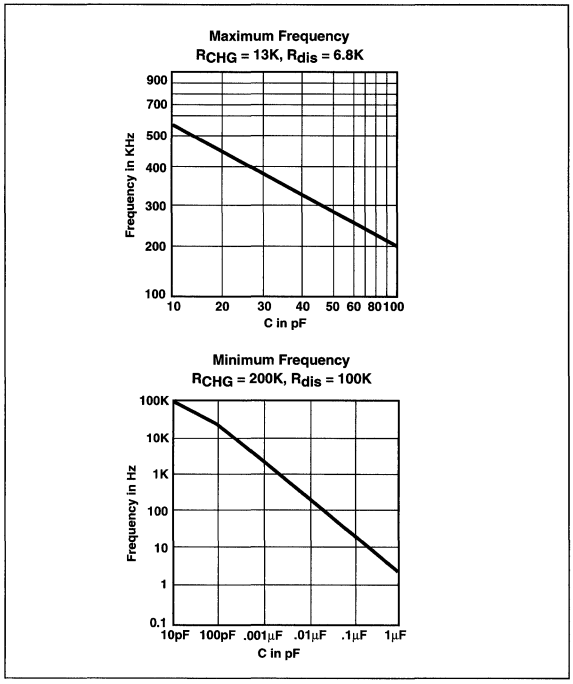


Figure 4 Typical Maximum and Minimum Operating Frequency vs. Capacitor

This circuit will convert a 6 to 15V input to a 5V output of 200 milliamps. Normal operating frequency is 50kHz. Peak to peak ripple is 50 millivolts. A change from 100mA to 200mA produces a 50mV peak change in V_{OUT}, with recovery in 200µs.

The TC96C555 is used here as a duty cycle modulator in a buck output circuit. The source current is modulated to control the duty cycle. Sink current is fixed at 100µA with a resistor (R4) of 10K. Transistor Q1, (2N2907A), is used for current modulation into TC96C555 Pin 4, the charge current program input. Shunt regulator TL431 is used for voltage sense and regulation feedback. The TL431 has an internal reference of 2.495V. Terminal R is compared with this reference to control conduction of cathode C to anode A. R2 and R3 are selected to give proper bias current to the TL431. C2 and R7 are for loop compensation and are optimized for a recovery time of 200µs. The TC96C555 outputs, Pin 7 and 6, are tied together so that when output is HIGH, current conducts from V_{DD} Pin 8 to output Pin 7 to charge the inductor, L1. When output is OFF or LOW, energy stored in L1 will continue to conduct through TC96C555 Pin 6 to the lower internal MOSFET and out to Pin 5, the ground return. This circuit does not have current limiting. A fuse is recommended for protection. Figure 6 shows the duty cycle as a function of the source current. Figure 8 shows the frequency vs control voltage.

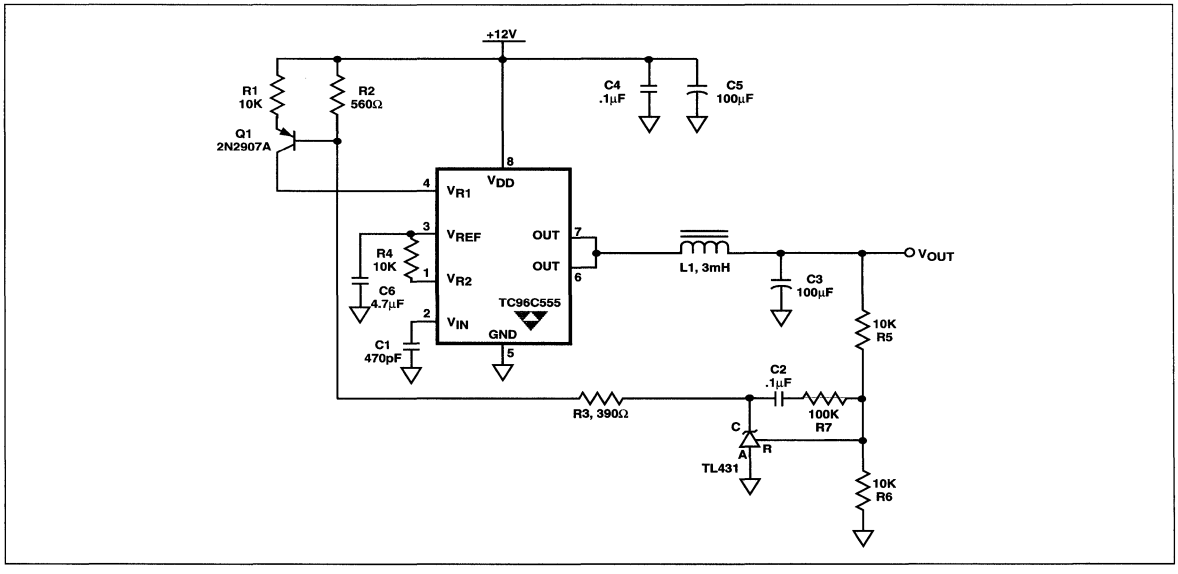


Figure 5 +5V Buck Regulator Power Supply with 82% Efficiency at 200mA Output

APPLICATIONS (cont.)

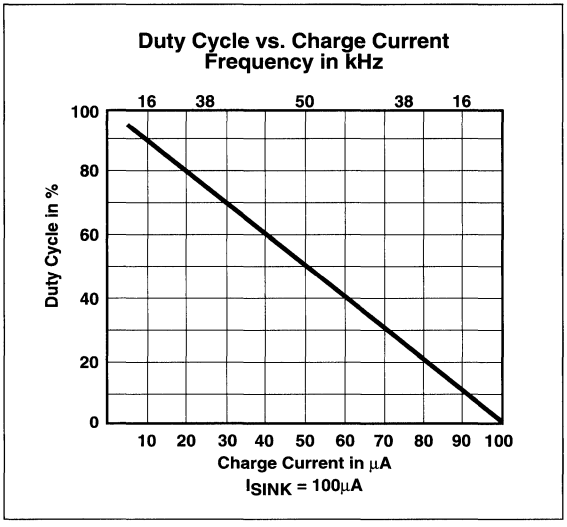


Figure 6 Duty Cycle vs. Charge Current

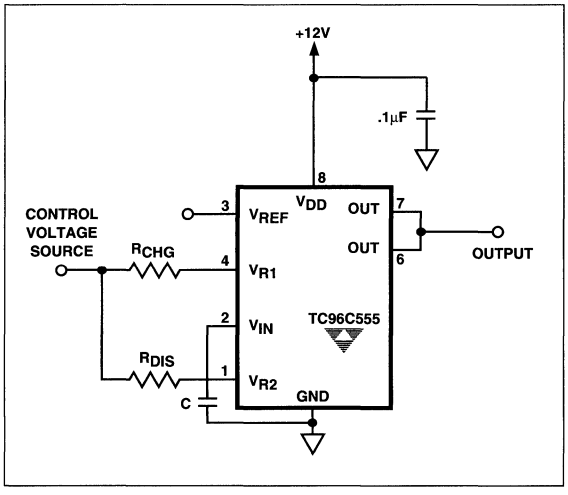


Figure 7 Voltage Controlled Power Oscillator

By connecting both resistors, R_{CHG} and R_{DIS}, to a voltage source instead of connecting to the 4V reference of Pin 3, one can increase or decrease the output frequency. Increasing the voltage source to 5V will double the oscillator frequency by doubling the voltage across both R_{CHG} and R_{DIS}. Decreasing the voltage source to 3.5V will drop the frequency in half.

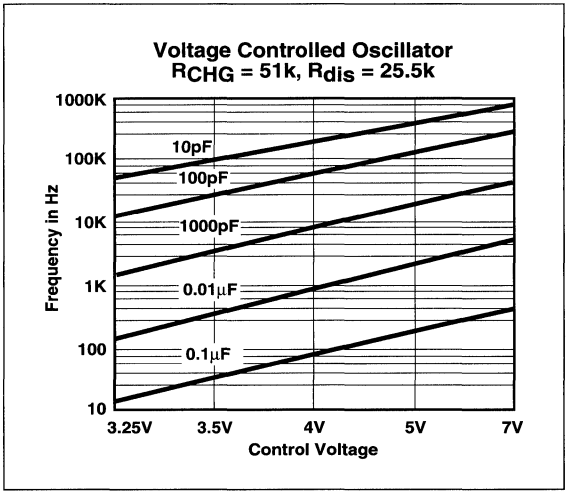


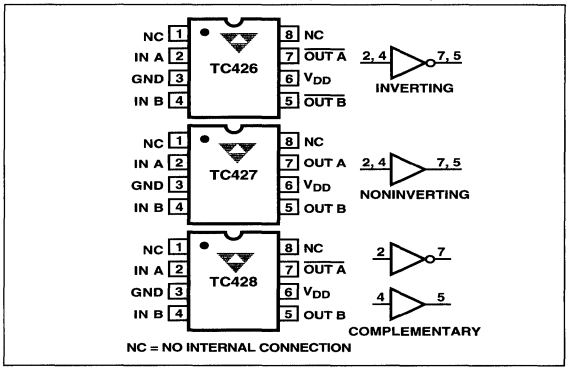
Figure 8 Frequency vs Control

DUAL HIGH-SPEED POWER MOSFET DRIVERS

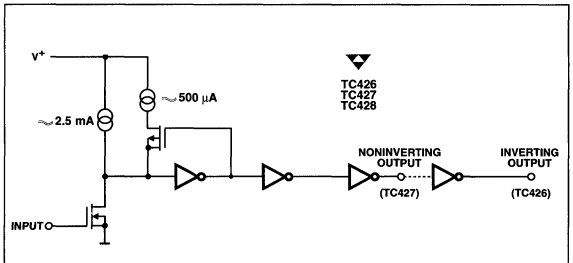
FEATURES

- **High-Speed Switching (C_L = 1000 pF) ..... 30 ns**
- **High Peak Output Current 1.5A**
- **High Output Voltage Swing ..... V_{DD}–25 mV GND+25 mV**
- **Low Input Current (Logic "0" or "1") ..... 1 µA**
- **TTL/CMOS Input Compatible**
- **Available in Inverting and Noninverting Configurations**
- **Wide Operating Supply Voltage ..... 4.5V to 18V**
- **Current Consumption**
  - **— Inputs Low ..... 0.4 mA**
  - **— Inputs High ..... 8 mA**
- **Single Supply Operation**
- **Low Output Impedance 6Ω**
- **Pinout Equivalent of DS0026 and MMH0026**
- **Latch-Up Resistant: Withstands >500 mA Reverse Current**
- **ESD Protected ..... 2 kV**

PIN CONFIGURATIONS (DIP and SO)



FUNCTIONAL DIAGRAM



Note: The TC428 has one inverting and one noninverting driver. Ground any unused driver input.

GENERAL DESCRIPTION

The TC426/TC427/TC428 are dual CMOS high-speed drivers. A TTL/CMOS input voltage level is translated into an output voltage level swing equaling the supply. The CMOS output will be within 25 mV of ground or positive supply. Bipolar designs are capable of swinging only within 1V of the supply.

The low impedance, high-current driver outputs will swing a 1000 pF load 18V in 30 ns. The unique current and voltage drive qualities make the TC426/TC427/TC428 ideal power MOSFET drivers, line drivers, and DC-to-DC converter building blocks.

Input logic signals may equal the power supply voltage. Input current is a low 1 µA, making direct interface to CMOS/bipolar switch-mode power supply control ICs possible, as well as open-collector analog comparators.

Quiescent power supply current is 8 mA maximum. The TC426 requires 1/5 the current of the pin-compatible bipolar DS0026 device. This is important in DC-to-DC converter applications with power efficiency constraints and high-frequency switch-mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pF load 18V at 100 kHz.

The inverting TC426 driver is pin-compatible with the bipolar DS0026 and MMH0026 devices. The TC427 is noninverting; the TC428 contains an inverting and noninverting driver.

Other pin compatible driver families are the TC1426/27/28, TC4426/27/28, and TC4426A/27A/28A.

ORDERING INFORMATION

Part No.	Package	Configuration	Temperature Range
TC426CPA	8-Pin PDIP	Inverting	0°C to +70°C
TC427CPA	8-Pin PDIP	Noninverting	0°C to +70°C
TC428CPA	8-Pin PDIP	Complementary	0°C to +70°C
TC426COA	8-Pin SOIC	Inverting	0°C to +70°C
TC427COA	8-Pin SOIC	Noninverting	0°C to +70°C
TC428COA	8-Pin SOIC	Complementary	0°C to +70°C
TC426IJA	8-Pin CerDIP	Inverting	–25°C to +85°C
TC427IJA	8-Pin CerDIP	Noninverting	–25°C to +85°C
TC428IJA	8-Pin CerDIP	Complementary	–25°C to +85°C
TC426EOA	8-Pin SOIC	Inverting	–40°C to +85°C
TC427EOA	8-Pin SOIC	Noninverting	–40°C to +85°C
TC428EOA	8-Pin SOIC	Complementary	–40°C to +85°C
TC426MJA	8-Pin CerDIP	Inverting	–55°C to +125°C
TC427MJA	8-Pin CerDIP	Noninverting	–55°C to +125°C
TC428MJA	8-Pin CerDIP	Complementary	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +20V
Input Voltage, Any Terminal ..... V_{DD}+0.3V to GND –0.3V
Power Dissipation
  Plastic ..... 1000 mW
  CerDIP ..... 800 mW
  SOIC ..... 500 mW
Derating Factor
  Plastic ..... 8 mW/°C
  CerDIP ..... 6.4 mW/°C
  SOIC ..... 4 mW/°C
Operating Temperature Range
  C Version ..... 0°C to +70°C
  I Version ..... –25°C to +85°C
  E Version ..... –40°C to +85°C
  M Version ..... –55°C to +125°C
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OH}	High Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	10	15	Ω
R_{OL}	Low Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	6	10	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time (Note 1)						
t_R	Rise Time	Test Figure 1/2	—	—	30	ns
t_F	Fall Time	Test Figure 1/2	—	—	30	ns
t_{D1}	Delay Time	Test Figure 1/2	—	—	50	ns
t_{D2}	Delay Time	Test Figure 1/2	—	—	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

ELECTRICAL CHARACTERISTICS: Over Operating Temperature Range with 4.5V≤V_{DD}≤18V, unless otherwise specified.

Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OH}	High Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	13	20	Ω
R_{OL}	Low Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	8	15	Ω
Switching Time (Note 1)						
t_R	Rise Time	Test Figure 1/2	—	—	60	ns
t_F	Fall Time	Test Figure 1/2	—	—	30	ns
t_{D1}	Delay Time	Test Figure 1/2	—	—	75	ns
t_{D2}	Delay Time	Test Figure 1/2	—	—	120	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	12	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	mA

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

SUPPLY BYPASSING

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 1000-pF load to18V in 25 ns requires an 0.72A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 µF film capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

GROUNDING

The TC426 and TC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 0.4 mA maximum. Minimum power dissipation occurs for logic "0" inputs for the TC426/427/428. **Unused driver inputs must be connected to V_{DD} or GND.**

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making the device TTL compatible over the 4.5V to 18V supply operating range. Input current is less than 1 µA over this range.

The TC426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560, and similar switch-mode power supply integrated circuits.

POWER DISSIPATION

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TC426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:
- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$Po = P_{DC} + PAC$

$= Vo\ (I_{DC}) + f\ C_L\ V_S$

Where:

Vo = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
Vs = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

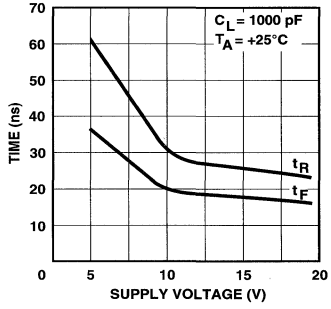
The magnitude of P_{AC} is readily estimated for several cases:

A.		B.	
1. f	= 20kHZ	1. f	= 200 kHz
2. C_L	=1000 pf	2. C_L	=1000 pf
3. Vs	= 18V	3. VS	=15V
4. P_{AC}	= 65 mW	4. P_{AC}	= 45 mW

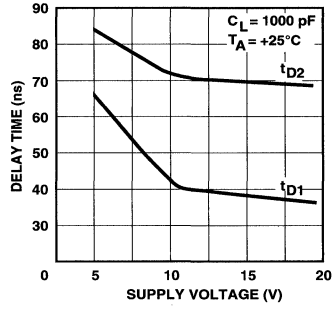
During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF". The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

TYPICAL CHARACTERISTICS CURVES

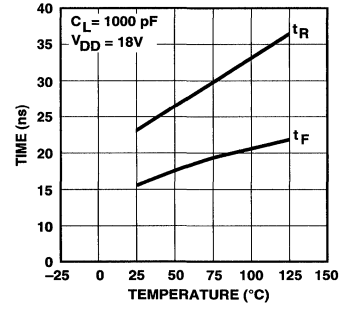
Rise and Fall Times vs Supply Voltage



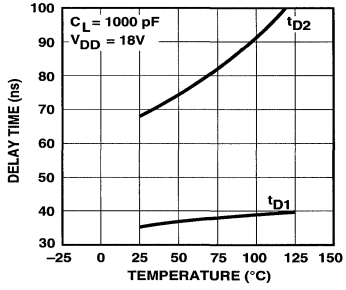
Delay Times vs Supply Voltage



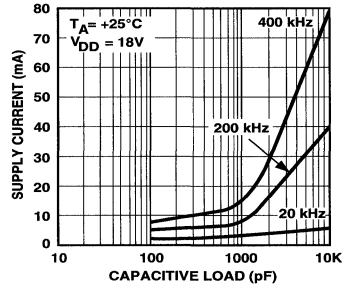
Rise and Fall Times vs Temperature



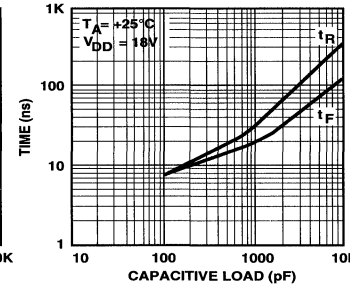
Delay Times vs Temperature



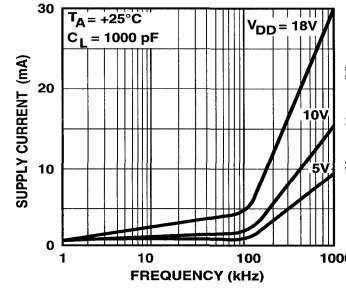
Supply Current vs Capacitive Load



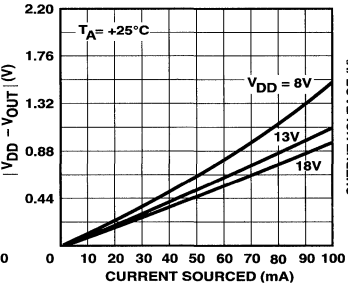
Rise and Fall Times vs Capacitive Load



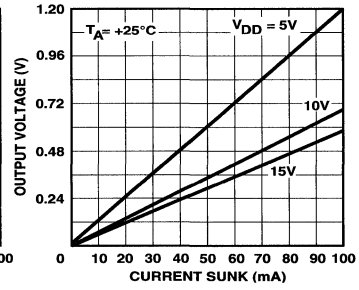
Supply Current vs Frequency



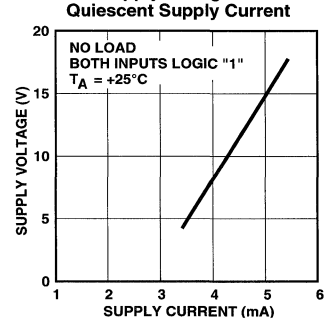
High Output vs Voltage



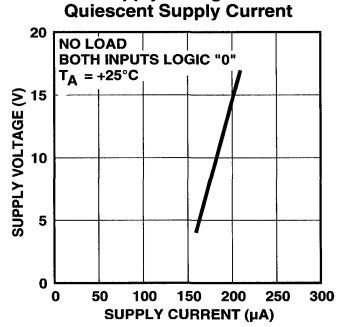
Low Output vs Voltage



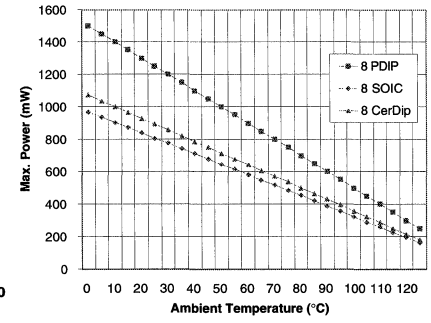
Supply Voltage vs Quiescent Supply Current

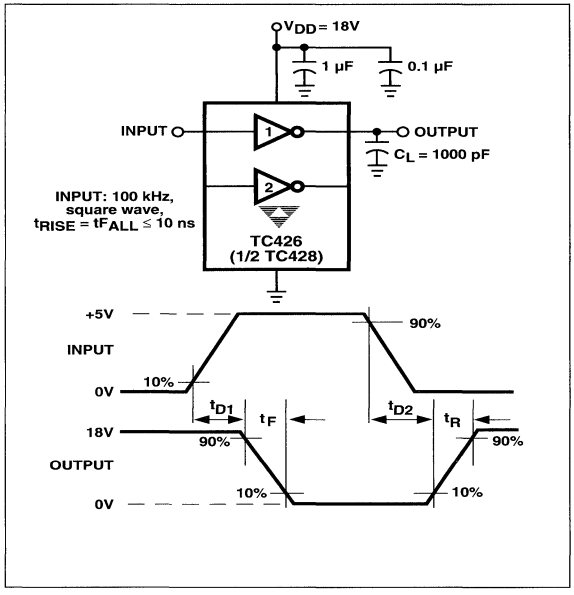


Supply Voltage vs Quiescent Supply Current

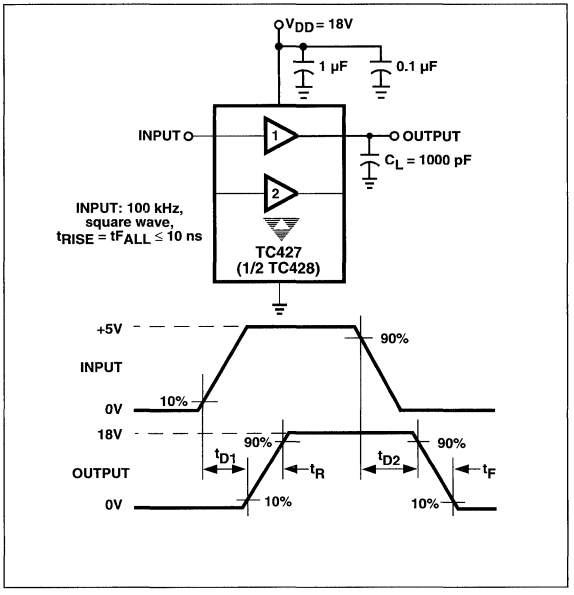


Thermal Derating Curve





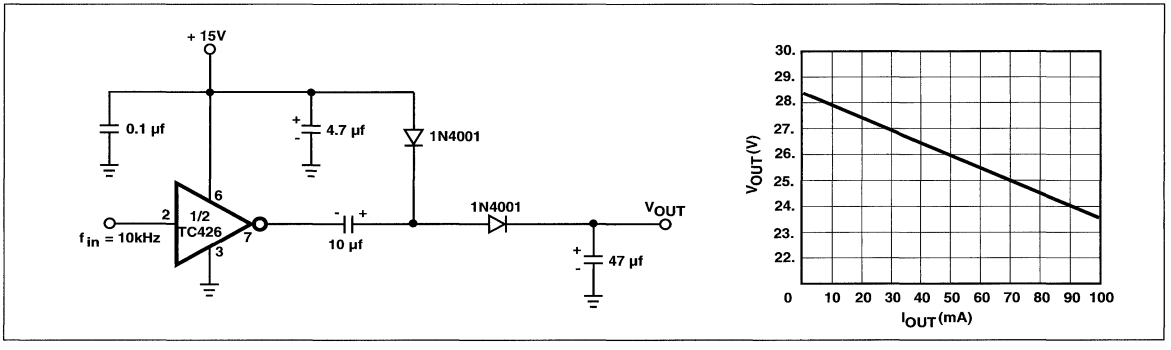
Test Figure 1. Inverting Driver Switching Time Test Circuit



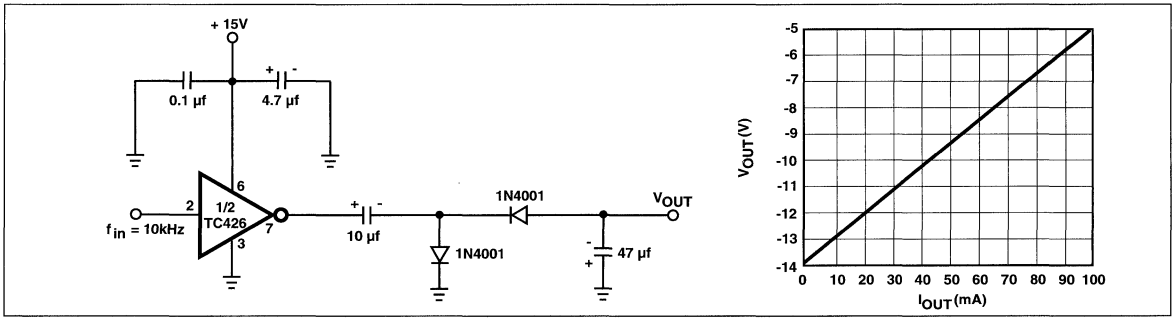
Test Figure 2. Noninverting Driver Switching Time Test Circuit

3

VOLTAGE DOUBLER



VOLTAGE INVERTER



SINGLE HIGH-SPEED, CMOS POWER MOSFET DRIVER

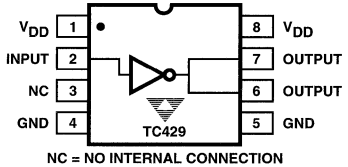
FEATURES

- **High Peak Output Current 6A**
- **Wide Operating Range ..... 7V to 18V**
- **High-Impedance CMOS Logic Input**
- **Logic Input Threshold Independent of Supply Voltage**
- **Low Supply Current**
  - **— With Logic 1 Input ..... 5 mA Max**
  - **— With Logic 0 Input ..... 0.5 mA Max**
- **Output Voltage Swing Within 25 mV of Ground or V_{DD}**
- **Short Delay Time ..... 75 ns Max**
- **High Capacitive Load Drive Capability**
  - **— t_{RISE}, t_{FALL} = 35 ns Max With C_{LOAD} = 2500 pF**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **CCD Drivers**
- **Pulse Transformer Drive**
- **Class D Switching Amplifiers**

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

NOTE: Duplicate pins must both be connected for proper operation.

GENERAL DESCRIPTION

The TC429 is a high-speed, single CMOS-level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the TC429 features 2.5Ω output impedance and 6A peak output current drive.

A 2500 pF capacitive load will be driven 18V in 25 ns. Delay time through the device is 60 ns. The rapid switching times with large capacitive loads minimize MOSFET transition power loss.

A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply and will swing to within 25 mV of ground or V_{DD}. Input voltage swing may equal the supply. Logic input current is under 10 μA, making direct interface to CMOS/bipolar switch-mode power supply controllers easy. Input "speed-up" capacitors are not required.

The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5 mA maximum and decreases to 0.5 mA for logic 0 inputs.

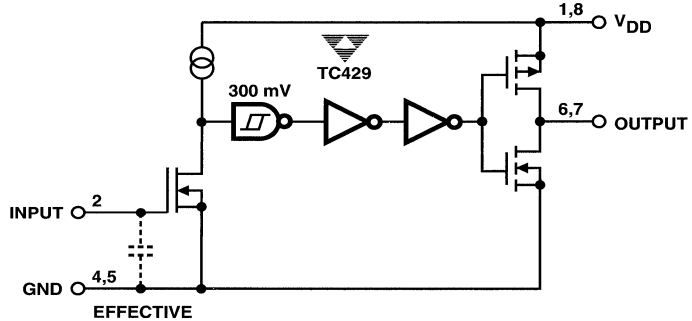
For dual devices, see the TC426/TC427/TC428 data sheet.

For noninverting applications, or applications requiring latch-up protection, see the TC4420/TC4429 data sheet.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC429CPA	8-Pin Plastic DIP	0°C to +70°C
TC429EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC429MJA	8-Pin CerDIP	– 55°C to +125°C

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +20V
Input Voltage, Any Terminal .... V_{DD} +0.3V to GND – 0.3V
Power Dissipation
  Plastic ..... 500 mW
  CerDIP ..... 800 mW
Derating Factors
  Plastic ..... 5.6 mW/°C Above 36°C
  CerDIP ..... 6 mW/°C
Operating Temperature Range
  C Version ..... 0°C to +70°C
  I Version ..... – 25°C to +85°C
  E Version ..... – 40°C to +85°C
  M Version ..... – 55°C to +125°C

Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

T_A = +25°C with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0, Low Input Voltage		—	1.3	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V	—	1.8	2.5	Ω
		I_{OUT} = 10 mA, V_{DD} = 18V				
		V_{IN} = 2.4V	—	1.5	2.5	Ω
		I_{OUT} = 10 mA, V_{DD} = 18V				
I_{PK}	Peak Output Current	V_{DD} = 18V (See Figure 3)	—	6	—	A
Switching Time (note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	53	75	ns
t_{D2}	Delay Time	Figure 1	—	60	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	3.5	5	mA
		V_{IN} = 0V	—	0.3	0.5	mA

NOTES: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS: Over operating temperature with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V	—	—	5	Ω
		I_{OUT} = 10 mA, V_{DD} = 18V				
		V_{IN} = 2.4V	—	—	5	Ω
		I_{OUT} = 10 mA, V_{DD} = 18V				
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	—	70	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	—	70	ns
t_{D1}	Delay Time	Figure 1	—	—	100	ns
t_{D2}	Delay Time	Figure 1	—	—	120	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	—	12	mA
		V_{IN} = 0V	—	—	1	mA

NOTE: 1. Switching times guaranteed by design.

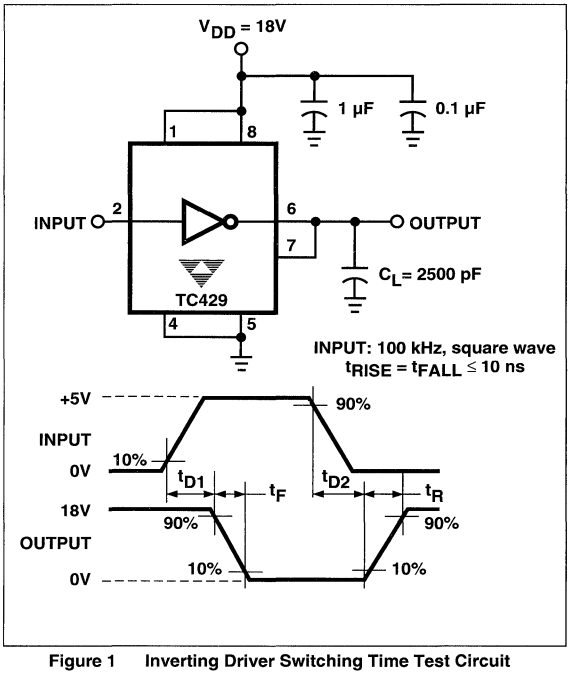
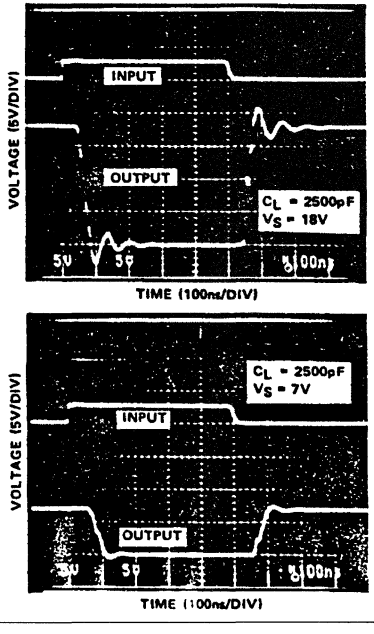


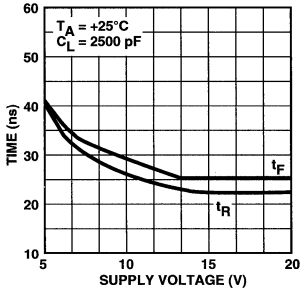
Figure 1 Inverting Driver Switching Time Test Circuit

SWITCHING SPEED

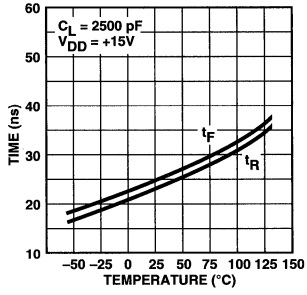


TYPICAL CHARACTERISTICS CURVES

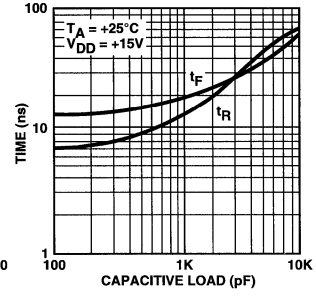
Rise/Fall Times vs. Supply Voltage



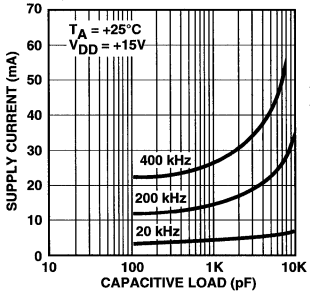
Rise/Fall Times vs. Temperature



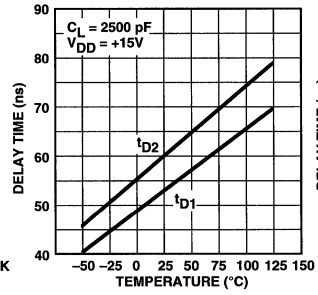
Rise/Fall Times vs. Capacitive Load



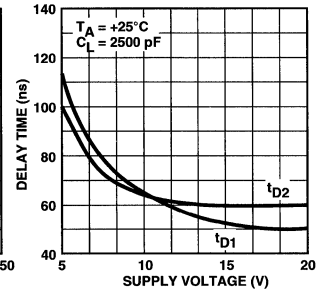
Supply Current vs. Capacitive Load



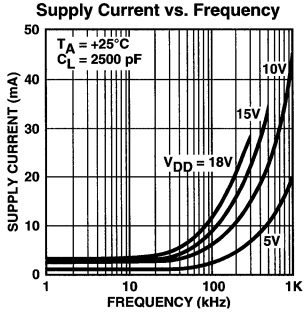
Delay Times vs. Temperature



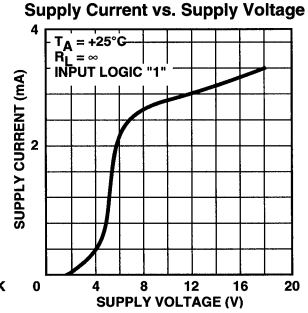
Delay Times vs. Supply Voltage



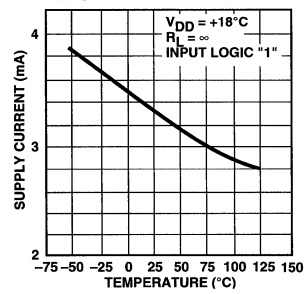
Supply Current vs. Frequency



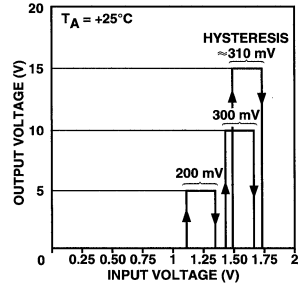
Supply Current vs. Supply Voltage



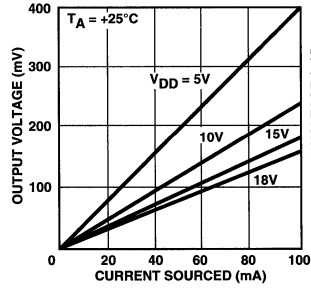
Supply Current vs. Temperature



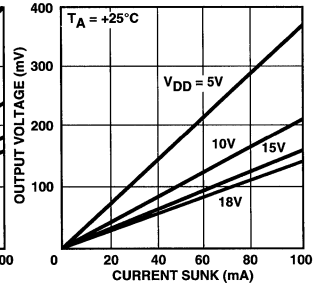
Voltage Transfer Characteristics



High Output Voltage vs. Current



Low Output Voltage vs. Current



SUPPLY BYPASSING

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500 pF load 18V in 25 ns requires a 1.8A current from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 μF film capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

GROUNDING

The high-current capability of the TC429 demands careful PC board layout for best performance. Since the TC429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow rise-time inputs, such as those produced by an open-collector output with resistor pull-up. The TC429 input structure includes about 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the TC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the TC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

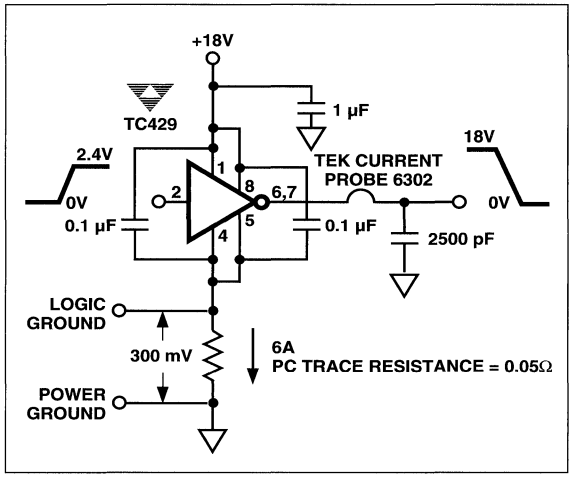


Figure 2 Switching Time Degradation Due to Negative Feedback

To ensure optimum device performance, separate ground traces should be provided for the logic and power connections. Connecting logic ground directly to the TC429 GND pins ensures full logic drive to the input and fast output switching. Both GND pins should be connected to power ground.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 3 mA current source load. With a logic "1" input, the maximum quiescent supply current is 5 mA. Logic "0" input level signals reduce quiescent current to 500 μA maximum.

The TC429 input is designed to provide 300 mV of hysteresis, providing clean transitions and minimizing output stage current spiking when changing states. Input voltage levels are approximately 1.5V, making the device TTL compatible over the 7V to 18V operating supply range. Input current is less than 10 μA over this range.

The TC429 can be directly driven by TL494, SG1526/1527, SG1524, SE5560 or similar switch-mode power supply integrated circuits. By off-loading the power-driving duties to the TC429, the power supply controller can operate at lower dissipation, improving performance and reliability.

POWER DISSIPATION

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TC429, however, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Table I lists the maximum operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 8-pin CerDIP junction-to-ambient thermal resistance is 150°C/W. At +25°C, the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

(1) Capacitive load dissipation (P_C)
(2) Quiescent power (P_Q)
(3) Transition power (P_T)

The capacitive load-caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

$$P_C = f\ C\ V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low-power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5 mA maximum. The queiscent power dissipation is:

$$P_Q = V_S\ (D\ (I_H) + (1-D)\ I_L),$$

where: I_H = Quiescent current with input high (5 mA max)
I_L = Quiescent current with input low (0.5 mA max)
D = Duty cycle.

Transition power dissipation arises because the output stage N- and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

$$P_T = f\ V_S\ (3.3 \times 10^{-9}\ A \cdot Sec).$$

An example shows the relative magnitude for each item.

Example 1:

C = 2500 pF
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 10 mW + 41 mW
= 164 mW.

Maximum operating temperature = $T_J - \theta_{JA}\ (P_D)$
= 125°C,

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (150°C/W, CerDIP).

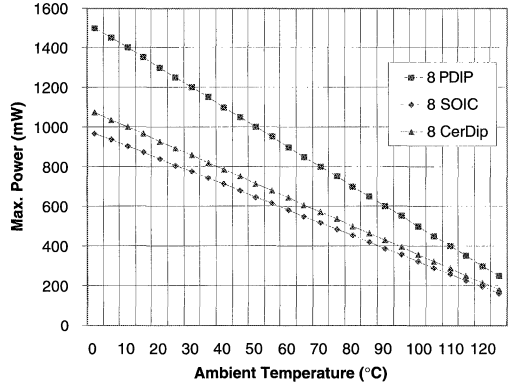
NOTE: Ambient operating temperature should not exceed +85°C for IJA devices or +125°C for MJA devices.

Table I. Maximum Operating Frequencies

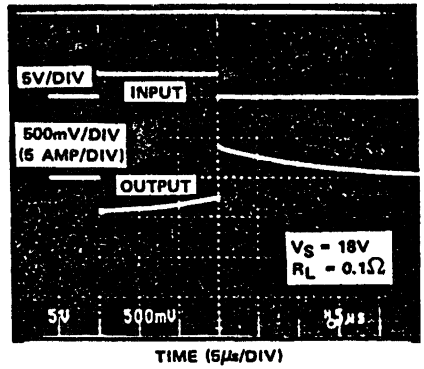
V_S	f_{Max}
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	>2 MHz

CONDITIONS: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = +25°C
3. C_L = 2500 pF

Thermal Derating Curve



Peak Output Current Capability



POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

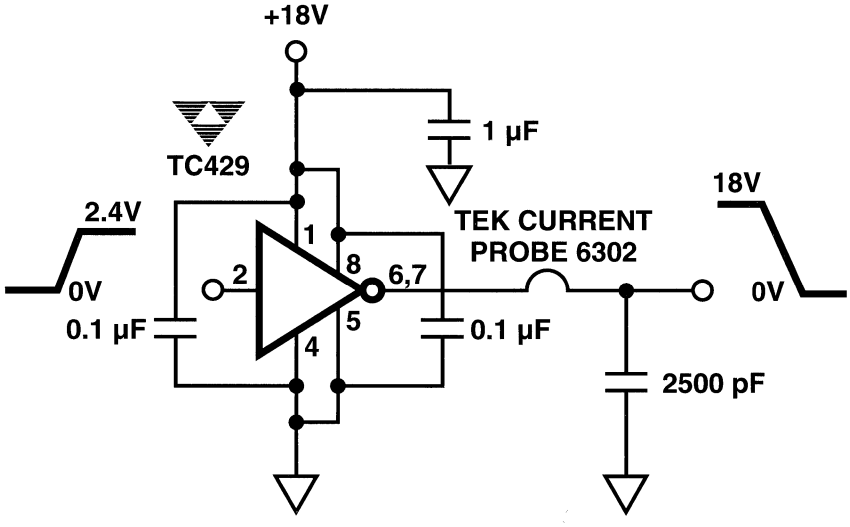


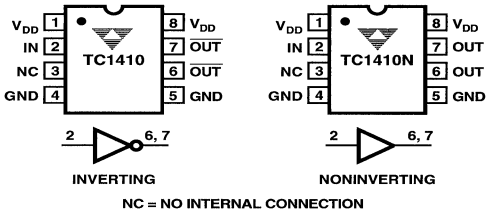
Figure 3 Peak Output Current Test Circuit

0.5A HIGH-SPEED MOSFET DRIVERS

FEATURES

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand 500mA Reverse Current**
- **Input Will Withstand Negative Inputs Up to 5V**
- **ESD Protected ..... 4 kV**
- **High Peak Output Current 0.5A**
- **Wide Operating Range ..... 4.5V to 16V**
- **High Capacitive Load Drive Capability ..... 500 pF in 25 ns**
- **Short Delay Time ..... 35 ns Typ**
- **Consistent Delay Times With Changes in Supply Voltage**
- **Matched Delay Times**
- **Low Supply Current**
  - **— With Logic "1" Input ..... 500 µA**
  - **— With Logic "0" Input ..... 150 µA**
- **Low Output Impedance ..... 16 Ω**
- **Pinout Same as TC1411/12/13**

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.

GENERAL DESCRIPTION

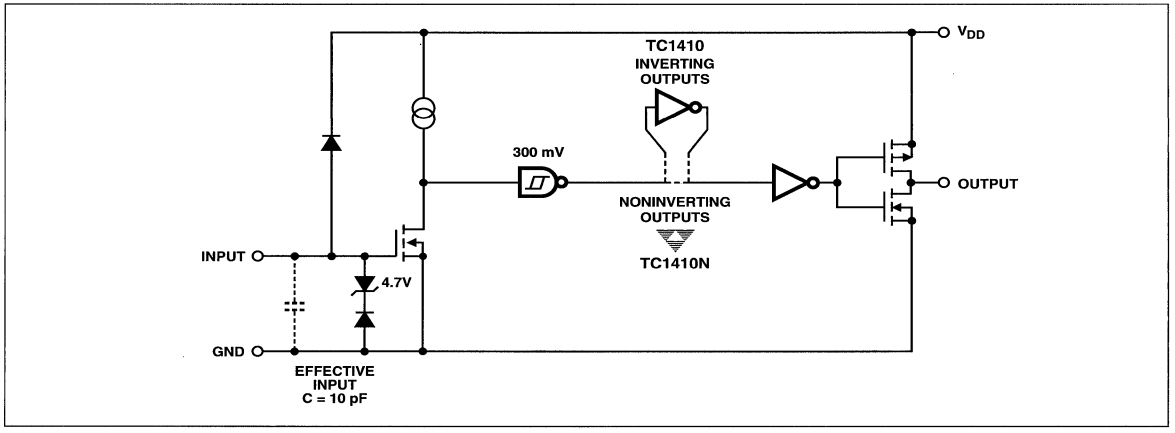
The TC1410/1410N are CMOS buffer/drivers built using TelCom Semiconductor's proprietary Tough CMOS™ process. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity toccurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC1410/1410N can easily switch 500 pF gate capacitance in 25 ns with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The rise and fall time edges are matched to allow driving short-duration inputs with greater accuracy.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1410COA	8-Pin SOIC	0°C to +70°C
TC1410EOA	8-Pin SOIC	– 40°C to +85°C
TC1410CPA	8-Pin Plastic DIP	0°C to +70°C
TC1410EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC1410NCOA	8-Pin SOIC	0°C to +70°C
TC1410NEOA	8-Pin SOIC	– 40°C to +85°C
TC1410NCPA	8-Pin Plastic DIP	0°C to +70°C
TC1410NEPA	8-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC1410
TC1410N

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

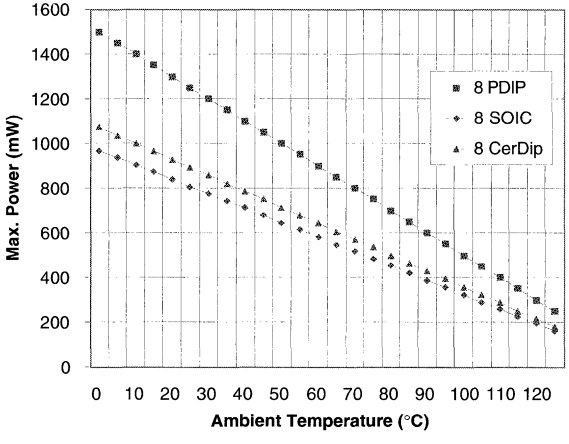
ELECTRICAL CHARACTERISTICS:

Over operating temperature range with $4.5V \le V_{DD} \le 16V$, unless otherwise specified. Typical values are measured at T_A=25°C; V_{DD}=16V.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Input							
V_{IH}	Logic 1 High Input Voltage			2.0	—	—	V
V_{IL}	Logic 0 Low Input Voltage			—	—	0.8	V
I_{IN}	Input Current	$-5V \le V_{IN} \le V_{DD}$	T_A=25°C	– 1	—	1	µA
			– 40°C≤T_A≤85°C	– 10	—	10	µA
Output							
V_{OH}	High Output Voltage	DC Test		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	DC Test		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 16V, I_O = 10 mA	T_A=25°C	—	16	22	Ω
			0°C≤T_A≤70°C	—	20	28	Ω
			– 40°C≤T_A≤85°C	—	20	28	Ω
I_{PK}	Peak Output Current	V_{DD} = 16V		—	0.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	V_{DD} = 16V	0.5	—	—	A
Switching Time (Note 1)							
t_R	Rise Time	Figure 1	T_A=25°C	—	25	35	ns
			0°C≤T_A≤70°C	—	27	40	ns
			– 40°C≤T_A≤85°C	—	29	40	ns
t_F	Fall Time	Figure 1	T_A=25°C	—	25	35	ns
			0°C≤T_A≤70°C	—	27	40	ns
			– 40°C≤T_A≤85°C	—	29	40	ns
t_{D1}	Delay Time	Figure 1	T_A=25°C	—	30	40	ns
			0°C≤T_A≤70°C	—	33	45	ns
			– 40°C≤T_A≤85°C	—	35	45	ns
t_{D2}	Delay Time	Figure 1	T_A=25°C	—	30	40	ns
			0°C≤T_A≤70°C	—	33	45	ns
			– 40°C≤T_A≤85°C	—	35	45	ns
Power Supply							
I_S	Power Supply Current	V_{IN} = 3V	V_{DD} = 16V	—	0.5	1.0	mA
		V_{IN} = 0V		—	0.1	0.15	mA

NOTE: 1. Switching times are guaranteed by design.

Thermal Derating Curve



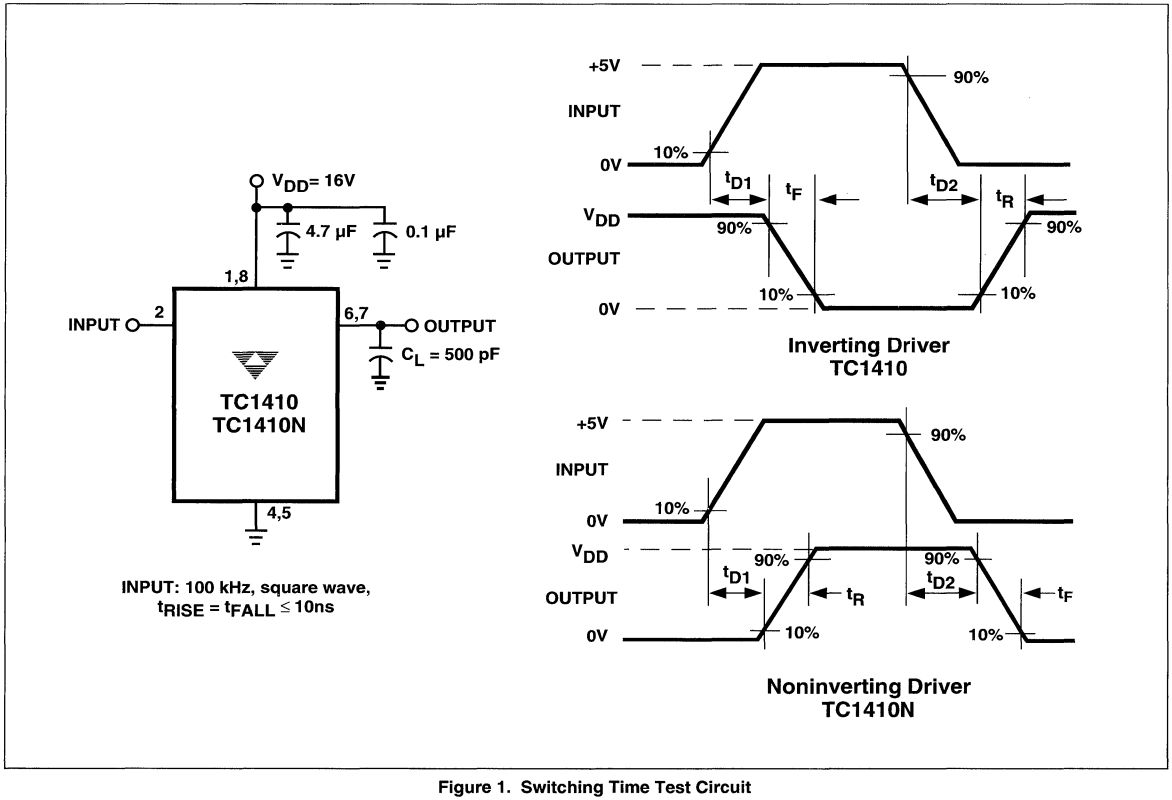
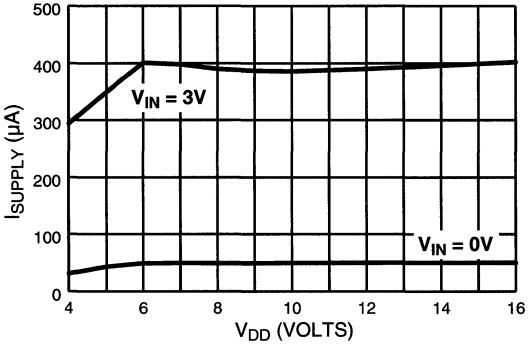


Figure 1. Switching Time Test Circuit

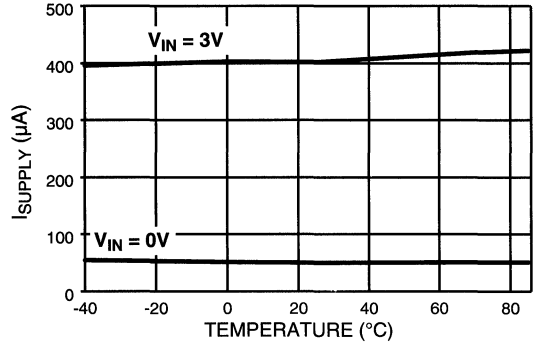
Quiescent Supply Current vs. Supply Voltage

T_A = 25°C



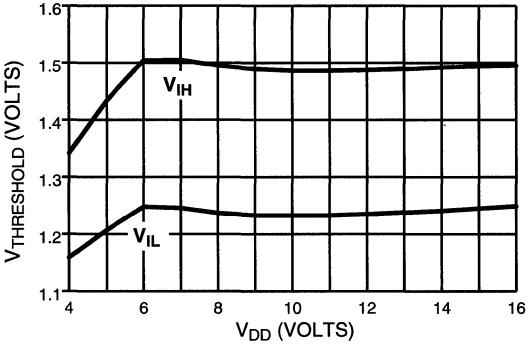
Quiescent Supply Current vs. Temperature

V_{SUPPLY} = 16V



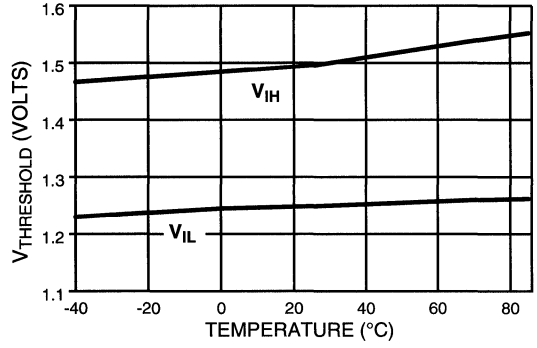
Input Threshold vs. Supply Voltage

T_A = 25°C

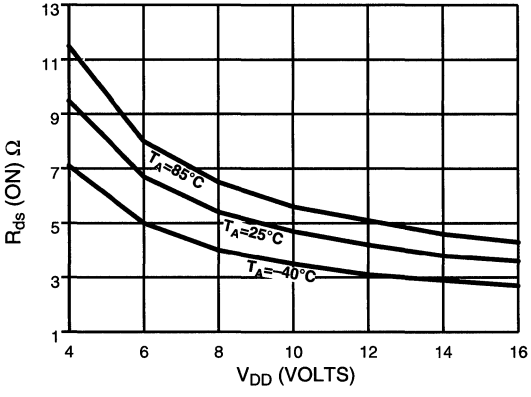


Input Threshold vs. Temperature

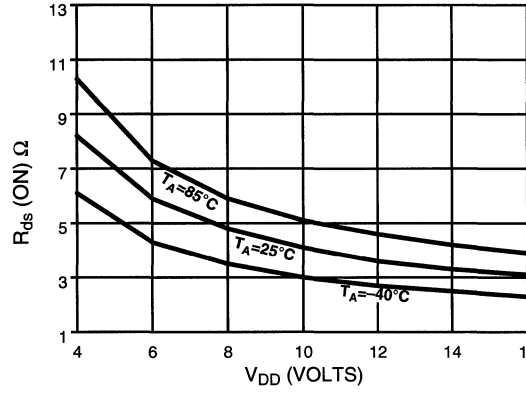
V_{SUPPLY} = 16V



High-State Output Resistance

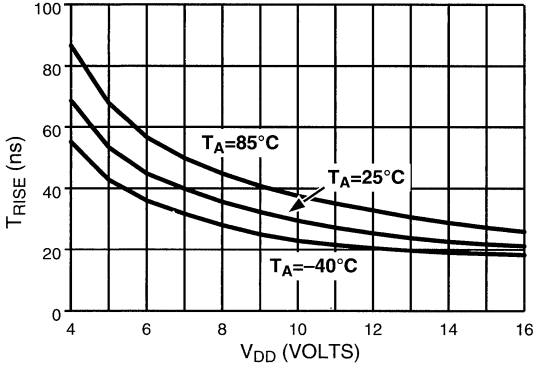


Low-State Output Resistance



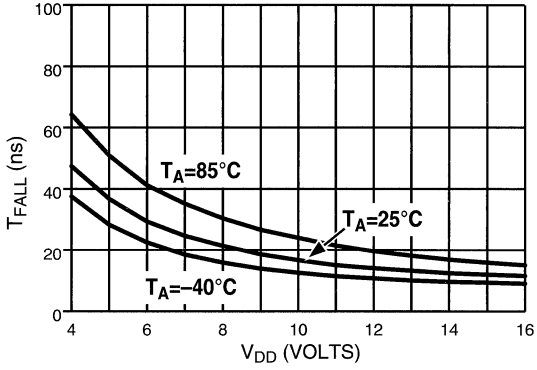
Rise Time vs. Supply Voltage

C_{LOAD} = 500pF



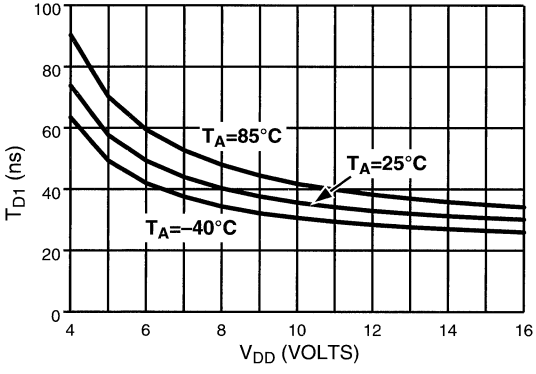
Fall Time vs. Supply Voltage

C_{LOAD} = 500pF



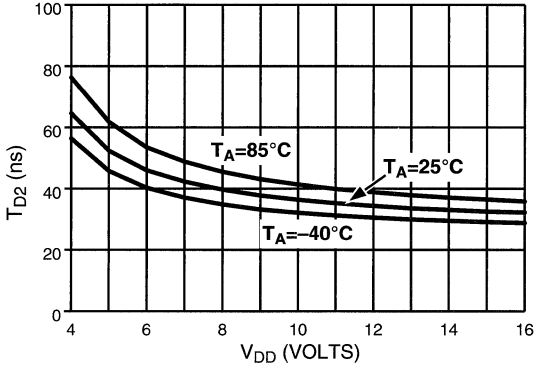
T_{D1} Propagation Delay vs. Supply Voltage

C_{LOAD} = 500pF



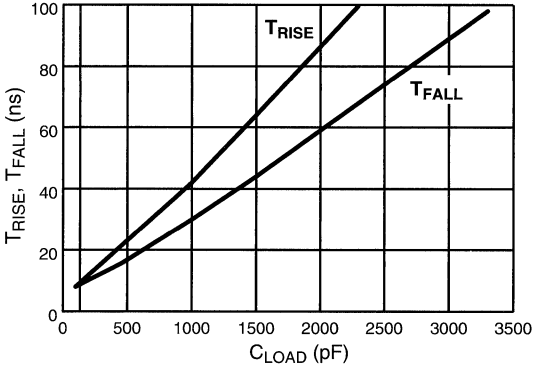
T_{D2} Propagation Delay vs. Supply Voltage

C_{LOAD} = 500pF



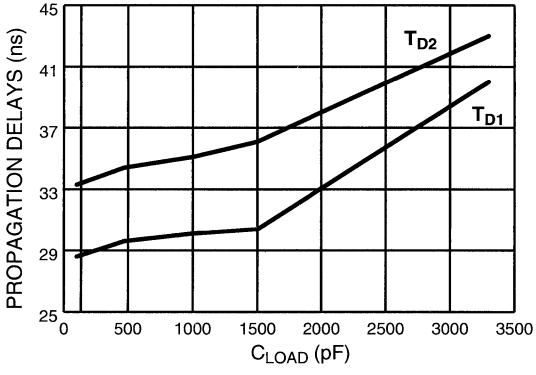
Rise and Fall Times vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V



Propagation Delays vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V

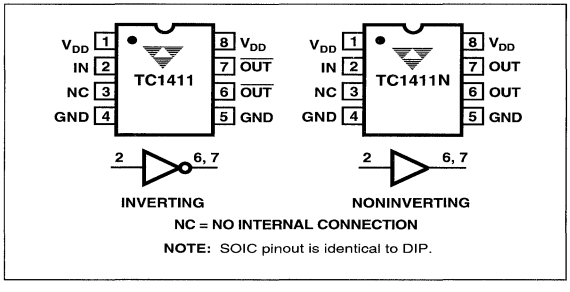


1A HIGH-SPEED MOSFET DRIVERS

FEATURES

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand 500mA Reverse Current**
- **Input Will Withstand Negative Inputs Up to 5V**
- **ESD Protected ..... 4 kV**
- **High Peak Output Current 1A**
- **Wide Operating Range ..... 4.5V to 16V**
- **High Capacitive Load Drive Capability ..... 1000 pF in 25 ns**
- **Short Delay Time ..... 30 ns Typ**
- **Consistent Delay Times With Changes in Supply Voltage**
- **Matched Delay Times**
- **Low Supply Current**
  - **— With Logic "1" Input ..... 500 µA**
  - **— With Logic "0" Input ..... 150 µA**
- **Low Output Impedance ..... 8 Ω**
- **Pinout Same as TC1410/12/13**

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.

GENERAL DESCRIPTION

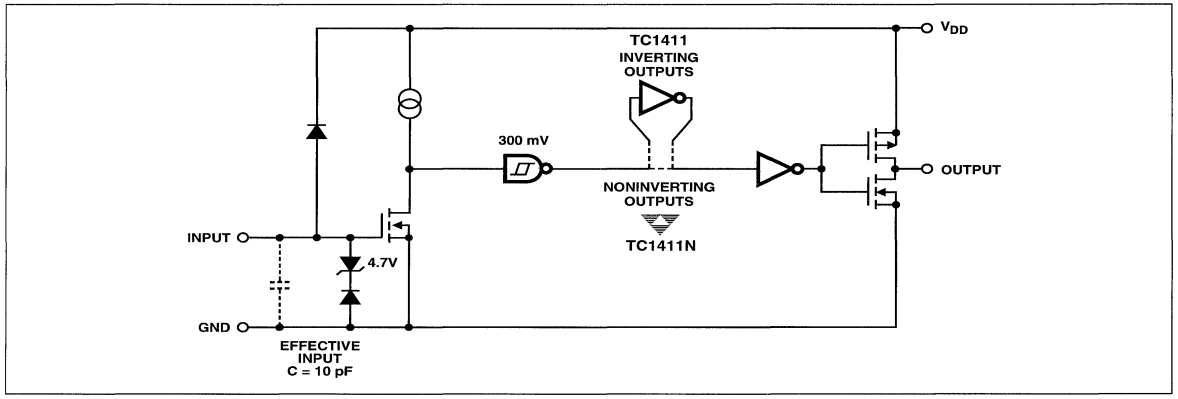
The TC1411/1411N are CMOS buffer/drivers built using TelCom Semiconductor's proprietary Tough CMOS™ process. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC1411/1411N can easily switch 1000 pF gate capacitance in 25 ns with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The rise and fall time edges are matched to allow driving short-duration inputs with greater accuracy.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1411COA	8-Pin SOIC	0°C to +70°C
TC1411EOA	8-Pin SOIC	– 40°C to +85°C
TC1411CPA	8-Pin Plastic DIP	0°C to +70°C
TC1411EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC1411NCOA	8-Pin SOIC	0°C to +70°C
TC1411NEOA	8-Pin SOIC	– 40°C to +85°C
TC1411NCPA	8-Pin Plastic DIP	0°C to +70°C
TC1411NEPA	8-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC1411
TC1411N

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

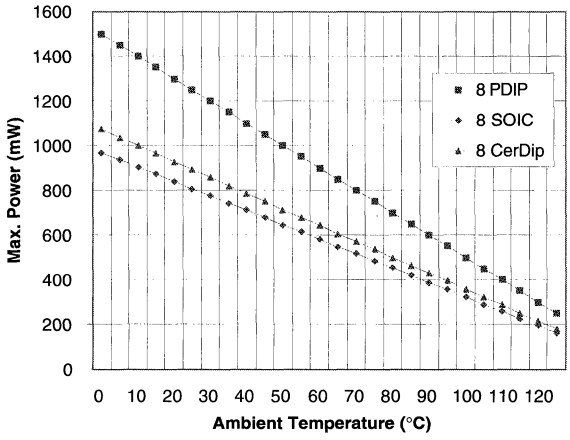
ELECTRICAL CHARACTERISTICS:

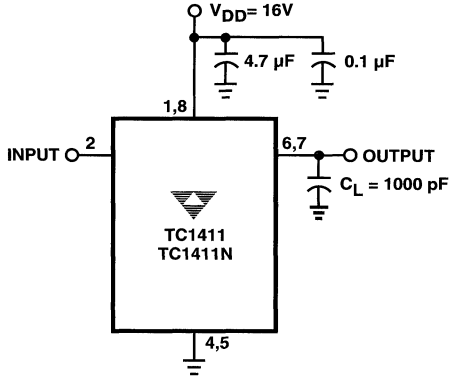
Over operating temperature range with 4.5V ≤ V_{DD} ≤ 16V, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Input							
V_{IH}	Logic 1 High Input Voltage			2.0	—	—	V
V_{IL}	Logic 0 Low Input Voltage			—	—	0.8	V
I_{IN}	Input Current	–5V ≤ V_{IN} ≤ V_{DD}	T_A=25°C	– 1	—	1	µA
			– 40°C≤T_A≤85°C	– 10	—	10	µA
Output							
V_{OH}	High Output Voltage	DC Test		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	DC Test		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 16V, I_O = 10 mA	T_A=25°C	—	8	11	Ω
			0°C≤T_A≤70°C	—	10	14	Ω
			– 40°C≤T_A≤85°C	—	10	14	Ω
I_{PK}	Peak Output Current	V_{DD} = 16V		—	1.0	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	V_{DD} = 16V	0.5	—	—	A
Switching Time (Note 1)							
t_R	Rise Time	Figure 1	T_A=25°C	—	25	35	ns
			0°C≤T_A≤70°C	—	27	40	ns
			– 40°C≤T_A≤85°C	—	29	40	ns
t_F	Fall Time	Figure 1	T_A=25°C	—	25	35	ns
			0°C≤T_A≤70°C	—	27	40	ns
			– 40°C≤T_A≤85°C	—	29	40	ns
t_{D1}	Delay Time	Figure 1	T_A=25°C	—	30	40	ns
			0°C≤T_A≤70°C	—	33	45	ns
			– 40°C≤T_A≤85°C	—	35	45	ns
t_{D2}	Delay Time	Figure 1	T_A=25°C	—	30	40	ns
			0°C≤T_A≤70°C	—	33	45	ns
			– 40°C≤T_A≤85°C	—	35	45	ns
Power Supply							
I_S	Power Supply Current	V_{IN} = 3V	V_{DD} = 16V	—	0.5	1.0	mA
		V_{IN} = 0V		—	0.1	0.15	mA

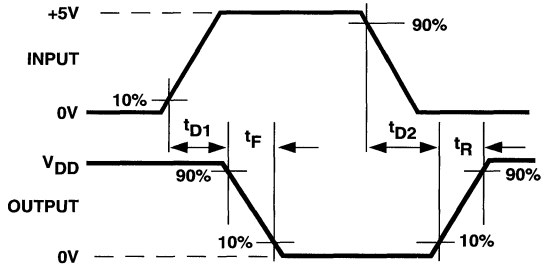
NOTE: 1. Switching times are guaranteed by design.

Thermal Derating Curve

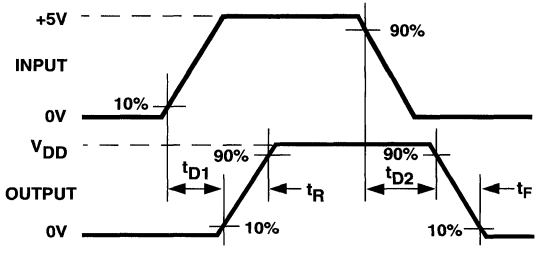




INPUT: 100 kHz, square wave,
$t_{RISE} = t_{FALL} \leq 10ns$



Inverting Driver
TC1411



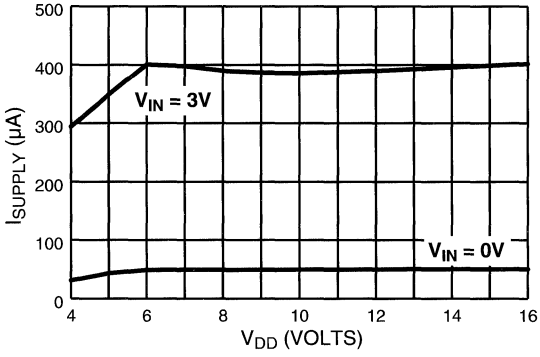
Noninverting Driver
TC1411N

Figure 1. Switching Time Test Circuit

TC1411
TC1411N

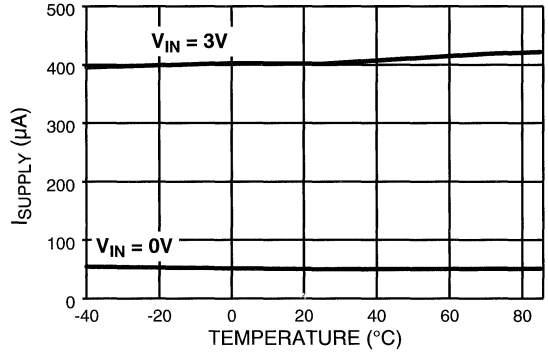
Quiescent Supply Current vs. Supply Voltage

T_A = 25°C



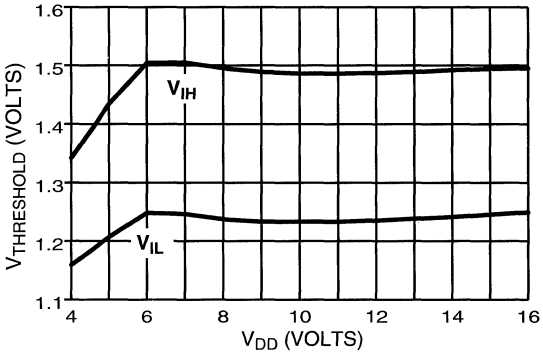
Quiescent Supply Current vs. Temperature

V_{SUPPLY} = 16V



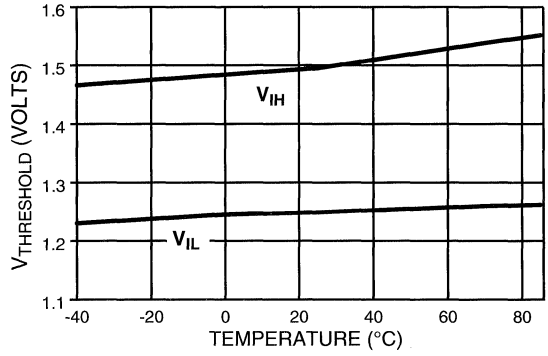
Input Threshold vs. Supply Voltage

T_A = 25°C

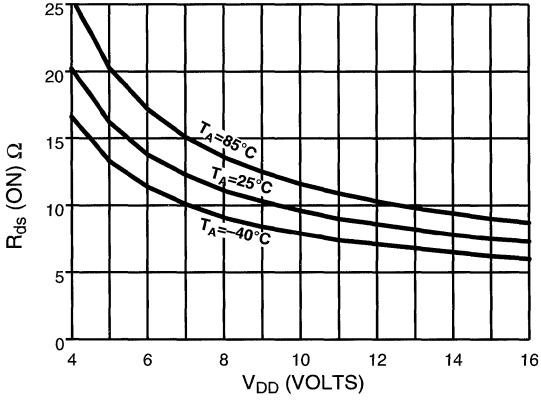


Input Threshold vs. Temperature

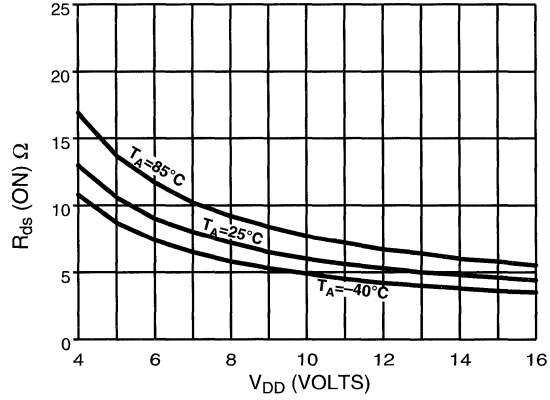
V_{SUPPLY} = 16V



High-State Output Resistance

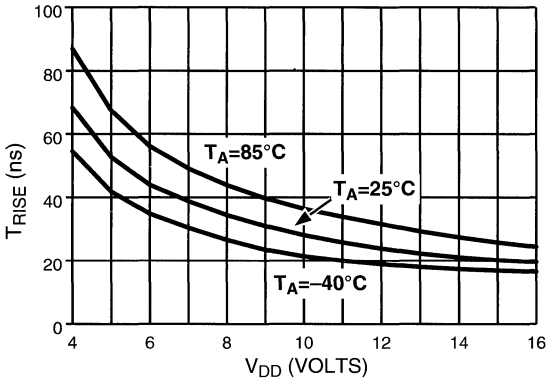


Low-State Output Resistance



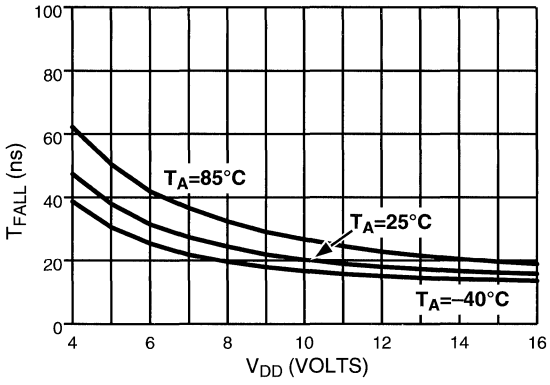
Rise Time vs. Supply Voltage

C_{LOAD} = 1000pF



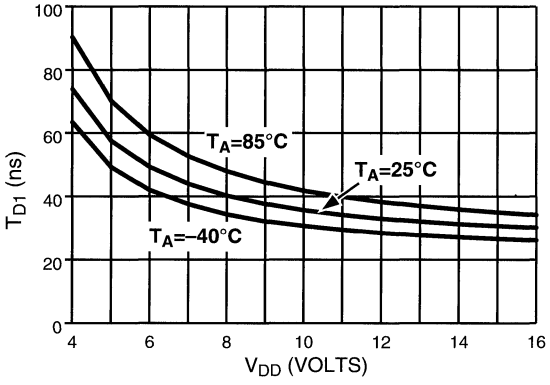
Fall Time vs. Supply Voltage

C_{LOAD} = 1000pF



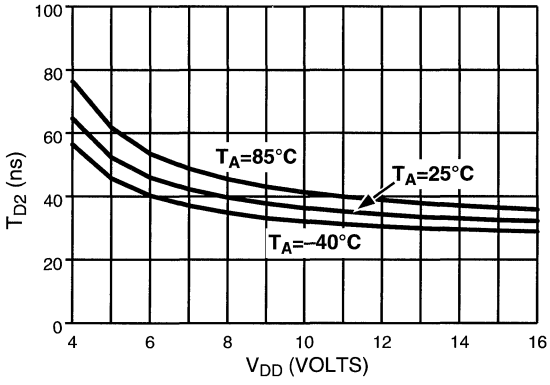
T_{D1} Propagation Delay vs. Supply Voltage

C_{LOAD} = 1000pF



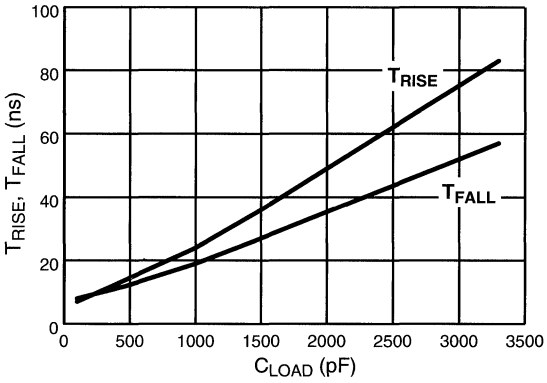
T_{D2} Propagation Delay vs. Supply Voltage

C_{LOAD} = 1000pF



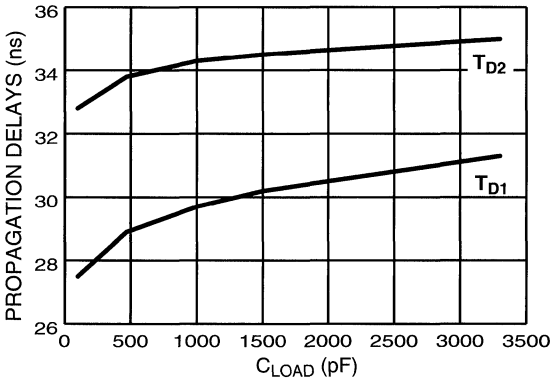
Rise and Fall Times vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V



Propagation Delays vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V

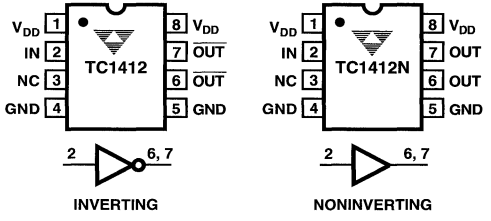


2A HIGH-SPEED MOSFET DRIVERS

FEATURES

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand 500mA Reverse Current**
- **Input Will Withstand Negative Inputs Up to 5V**
- **ESD Protected ..... 4 kV**
- **High Peak Output Current 2A**
- **Wide Operating Range ..... 4.5V to 16V**
- **High Capacitive Load Drive Capability ..... 1000 pF in 18 ns**
- **Short Delay Time ..... 35 ns Typ**
- **Consistent Delay Times With Changes in Supply Voltage**
- **Matched Delay Times**
- **Low Supply Current**
  - **— With Logic "1" Input ..... 500 μA**
  - **— With Logic "0" Input ..... 150 μA**
- **Low Output Impedance ..... 4 Ω**
- **Pinout Same as TC1410/11/13**

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.

GENERAL DESCRIPTION

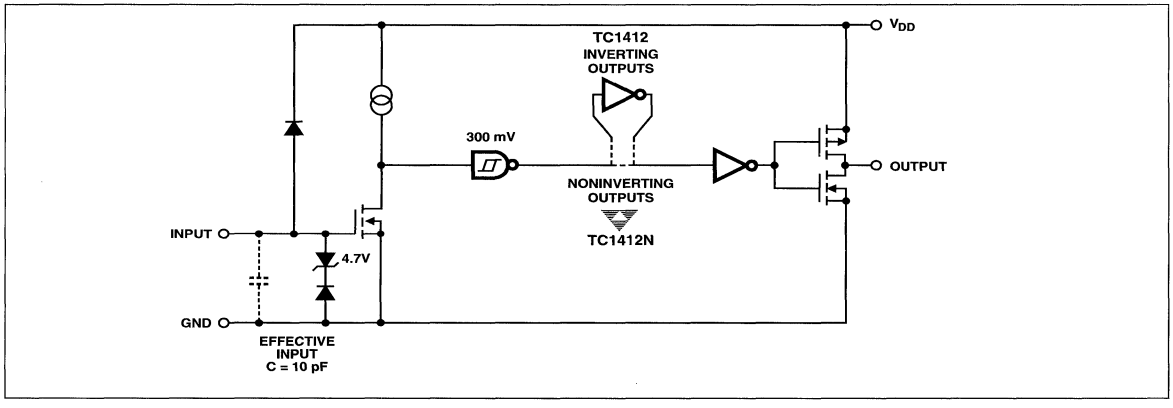
The TC1412/1412N are CMOS buffer/drivers built using TelCom Semiconductor's proprietary Tough CMOS™ process. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC1412/1412N can easily switch 1000 pF gate capacitance in 18 ns with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The rise and fall time edges are matched to allow driving short-duration inputs with greater accuracy.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1412COA	8-Pin SOIC	0°C to +70°C
TC1412EOA	8-Pin SOIC	– 40°C to +85°C
TC1412CPA	8-Pin Plastic DIP	0°C to +70°C
TC1412EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC1412NCOA	8-Pin SOIC	0°C to +70°C
TC1412NEOA	8-Pin SOIC	– 40°C to +85°C
TC1412NCPA	8-Pin Plastic DIP	0°C to +70°C
TC1412NEPA	8-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC1412
TC1412N

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

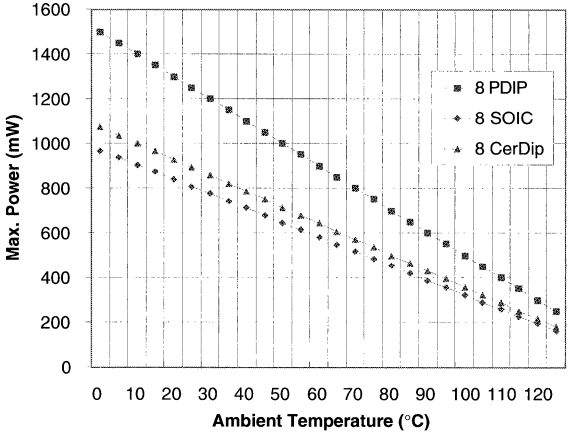
ELECTRICAL CHARACTERISTICS:

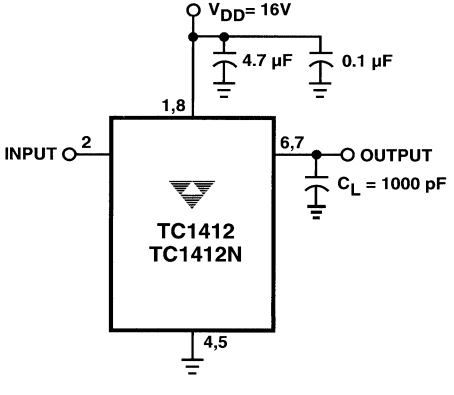
Over operating temperature range with 4.5V ≤ V_{DD} ≤ 16V, unless otherwise specified. Typical values are measured at T_A=25°C; V_{DD}=16V.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Input							
V_{IH}	Logic 1 High Input Voltage			2.0	—	—	V
V_{IL}	Logic 0 Low Input Voltage			—	—	0.8	V
I_{IN}	Input Current	–5V ≤ V_{IN} ≤ V_{DD}	T_A=25°C	– 1	—	1	µA
			– 40°C≤T_A≤85°C	– 10	—	10	µA
Output							
V_{OH}	High Output Voltage	DC Test		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	DC Test		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 16V, I_O = 10 mA	T_A=25°C	—	4	6	Ω
			0°C≤T_A≤70°C	—	5	7	Ω
			– 40°C≤T_A≤85°C	—	5	7	Ω
I_{PK}	Peak Output Current	V_{DD} = 16V		—	2.0	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	V_{DD} = 16V	0.5	—	—	A
Switching Time (Note 1)							
t_R	Rise Time	Figure 1	T_A=25°C	—	18	26	ns
			0°C≤T_A≤70°C	—	20	31	ns
			– 40°C≤T_A≤85°C	—	22	31	ns
t_F	Fall Time	Figure 1	T_A=25°C	—	18	26	ns
			0°C≤T_A≤70°C	—	20	31	ns
			– 40°C≤T_A≤85°C	—	22	31	ns
t_{D1}	Delay Time	Figure 1	T_A=25°C	—	35	45	ns
			0°C≤T_A≤70°C	—	40	50	ns
			– 40°C≤T_A≤85°C	—	40	50	ns
t_{D2}	Delay Time	Figure 1	T_A=25°C	—	35	45	ns
			0°C≤T_A≤70°C	—	40	50	ns
			– 40°C≤T_A≤85°C	—	40	50	ns
Power Supply							
I_S	Power Supply Current	V_{IN} = 3V	V_{DD} = 16V	—	0.5	1.0	mA
		V_{IN} = 0V		—	0.1	0.15	mA

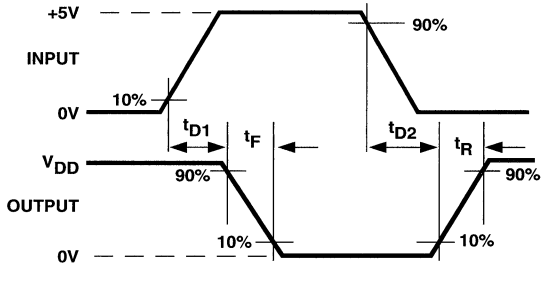
NOTE: 1. Switching times are guaranteed by design.

Thermal Derating Curve

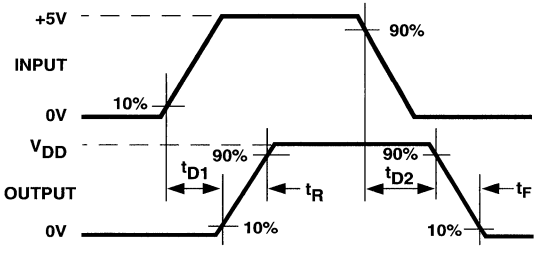




INPUT: 100 kHz, square wave,
$t_{RISE} = t_{FALL} \leq 10ns$



Inverting Driver
TC1412



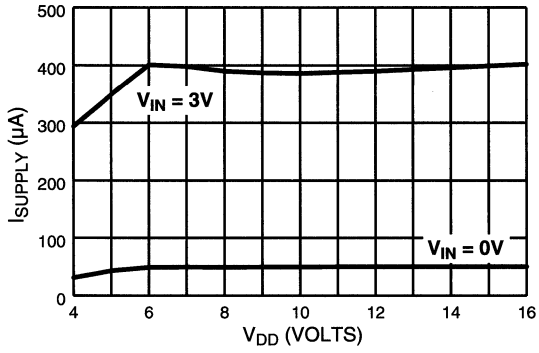
Noninverting Driver
TC1412N

Figure 1. Switching Time Test Circuit

TC1412
TC1412N

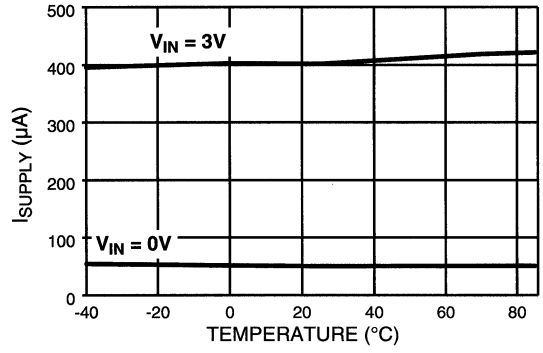
Quiescent Supply Current vs. Supply Voltage

T_A = 25°C



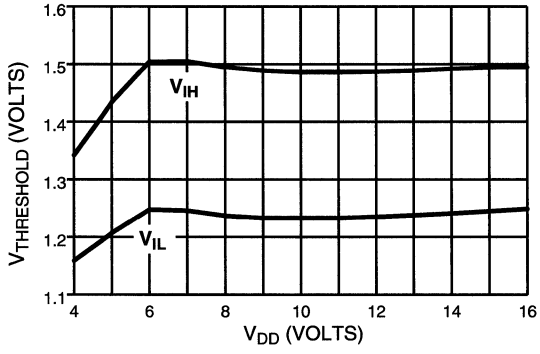
Quiescent Supply Current vs. Temperature

V_{SUPPLY} = 16V



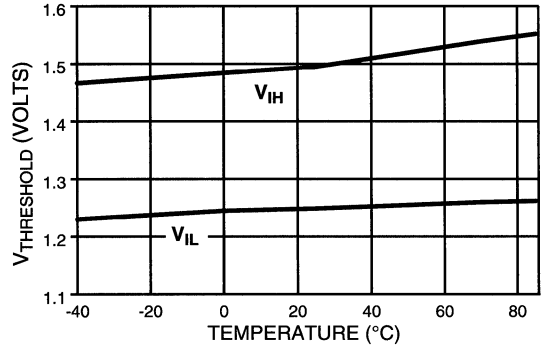
Input Threshold vs. Supply Voltage

T_A = 25°C

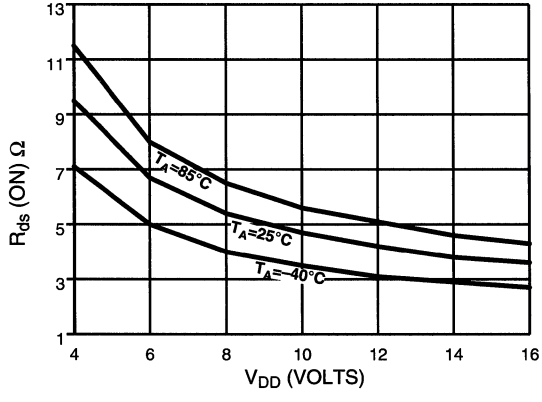


Input Threshold vs. Temperature

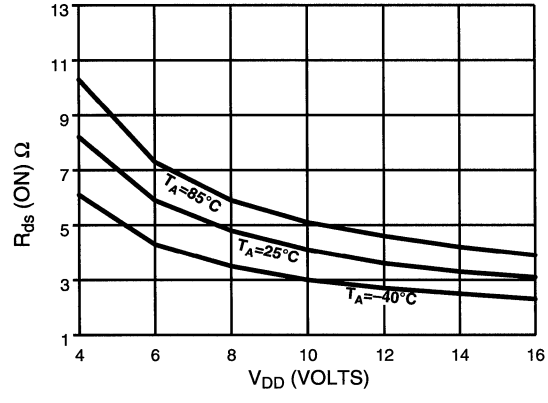
V_{SUPPLY} = 16V



High-State Output Resistance

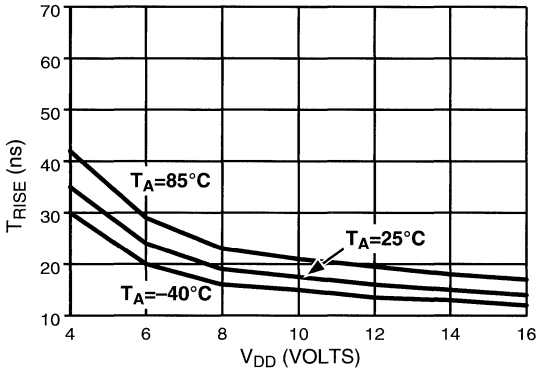


Low-State Output Resistance



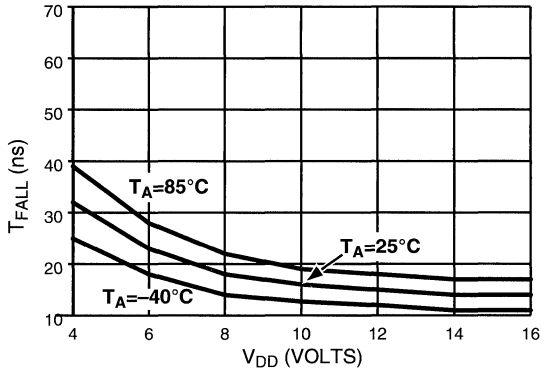
Rise Time vs. Supply Voltage

C_{LOAD} = 1800pF



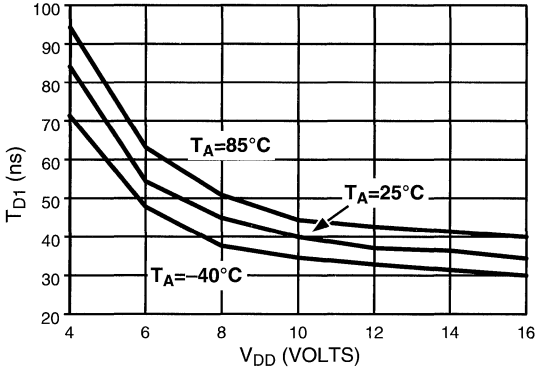
Fall Time vs. Supply Voltage

C_{LOAD} = 1800pF



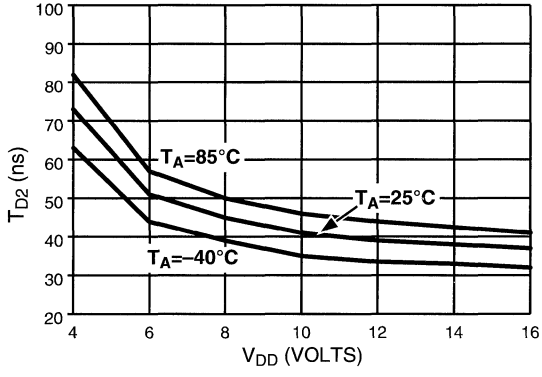
T_{D1} Propagation Delay vs. Supply Voltage

C_{LOAD} = 1800pF



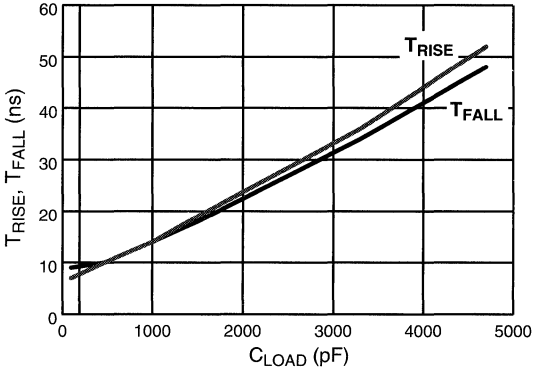
T_{D2} Propagation Delay vs. Supply Voltage

C_{LOAD} = 1800pF



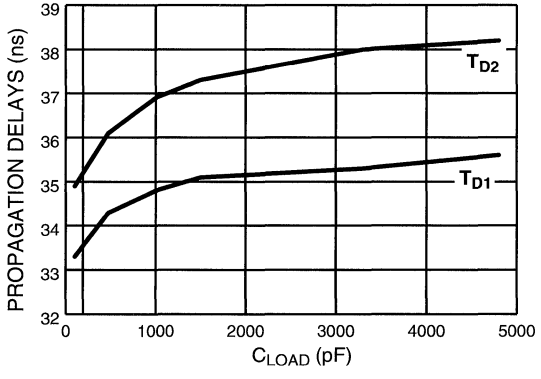
Rise and Fall Times vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V



Propagation Delays vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V

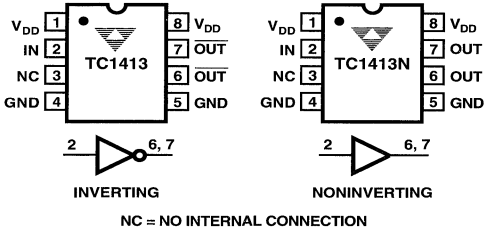


3A HIGH-SPEED MOSFET DRIVERS

FEATURES

- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand 500mA Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected ..... 4 kV
- High Peak Output Current 3A
- Wide Operating Range ..... 4.5V to 16V
- High Capacitive Load Drive Capability ..... 1800 pF in 20 ns
- Short Delay Time ..... 35 ns Typ
- Consistent Delay Times With Changes in Supply Voltage
- Matched Delay Times
- Low Supply Current
  - — With Logic "1" Input ..... 500 µA
  - — With Logic "0" Input ..... 150 µA
- Low Output Impedance ..... 2.7 Ω
- Pinout Same as TC1410/11/12

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.

GENERAL DESCRIPTION

The TC1413/1413N are CMOS buffer/drivers built using TelCom Semiconductor's proprietary Tough CMOS™ process. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity that occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

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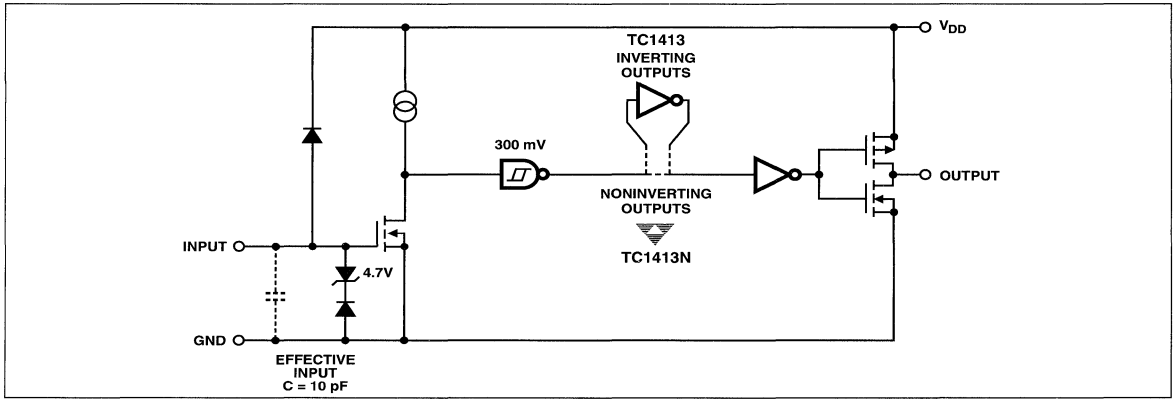
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1413COA	8-Pin SOIC	0°C to +70°C
TC1413EOA	8-Pin SOIC	– 40°C to +85°C
TC1413CPA	8-Pin Plastic DIP	0°C to +70°C
TC1413EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC1413NCOA	8-Pin SOIC	0°C to +70°C
TC1413NEOA	8-Pin SOIC	– 40°C to +85°C
TC1413NCPA	8-Pin Plastic DIP	0°C to +70°C
TC1413NEPA	8-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC1413
TC1413N

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 500 mW

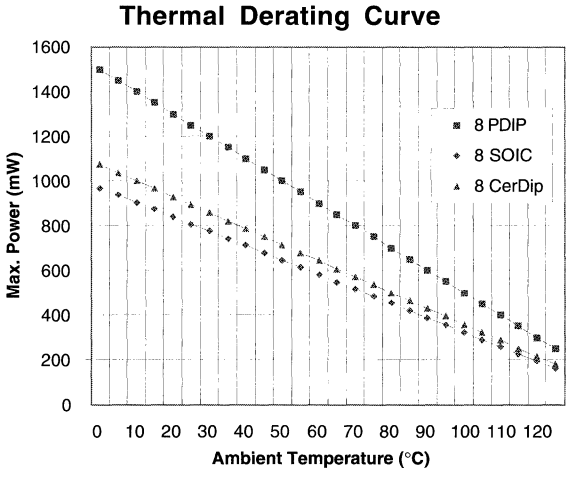
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

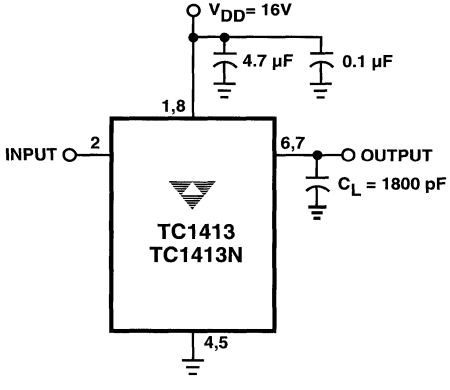
ELECTRICAL CHARACTERISTICS:

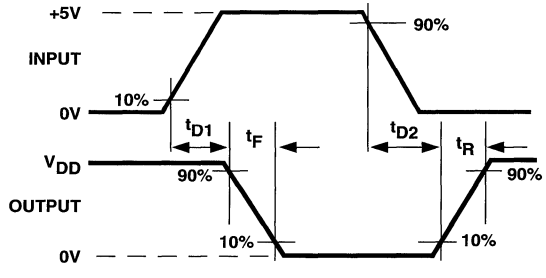
Over operating temperature range with 4.5V ≤ V_{DD} ≤ 16V, unless otherwise specified. Typical values are measured at T_A=25°C; V_{DD}=16V

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Input							
V_{IH}	Logic 1 High Input Voltage			2.0	—	—	V
V_{IL}	Logic 0 Low Input Voltage			—	—	0.8	V
I_{IN}	Input Current	– 5V ≤ V_{IN} ≤ V_{DD}	T_A=25°C	– 1	—	1	µA
			– 40°C≤T_A≤85°C	– 10	—	10	µA
Output							
V_{OH}	High Output Voltage	DC Test		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	DC Test		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 16V, I_O = 10 mA	T_A=25°C	—	2.7	4	Ω
			0°C≤T_A≤70°C	—	3.3	5	Ω
			– 40°C≤T_A≤85°C	—	3.3	5	Ω
I_{PK}	Peak Output Current	V_{DD} = 16V		—	3.0	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	V_{DD} = 16V	0.5	—	—	A
Switching Time (Note 1)							
t_R	Rise Time	Figure 1	T_A=25°C	—	20	28	ns
			0°C≤T_A≤70°C	—	22	33	ns
			– 40°C≤T_A≤85°C	—	24	33	ns
t_F	Fall Time	Figure 1	T_A=25°C	—	20	28	ns
			0°C≤T_A≤70°C	—	22	33	ns
			– 40°C≤T_A≤85°C	—	24	33	ns
t_{D1}	Delay Time	Figure 1	T_A=25°C	—	35	45	ns
			0°C≤T_A≤70°C	—	40	50	ns
			– 40°C≤T_A≤85°C	—	40	50	ns
t_{D2}	Delay Time	Figure 1	T_A=25°C	—	35	45	ns
			0°C≤T_A≤70°C	—	40	50	ns
			– 40°C≤T_A≤85°C	—	40	50	ns
Power Supply							
I_S	Power Supply Current	V_{IN} = 3V	V_{DD} = 16V	—	0.5	1.0	mA
		V_{IN} = 0V		—	0.1	0.15	mA

NOTE: 1. Switching times are guaranteed by design.







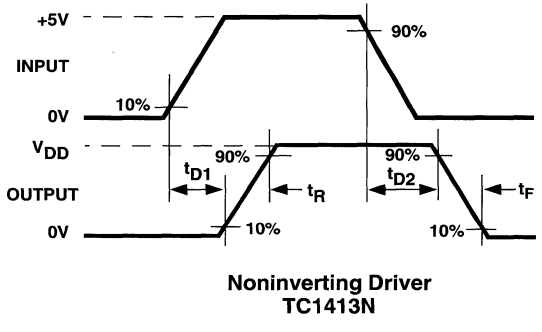
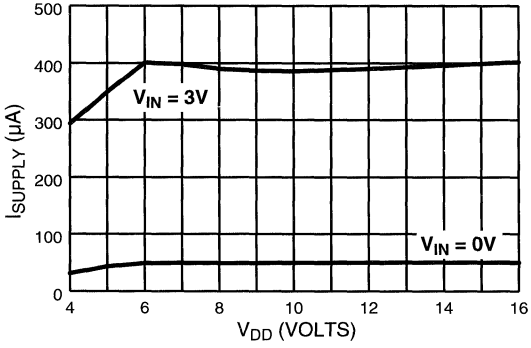


Figure 1. Switching Time Test Circuit

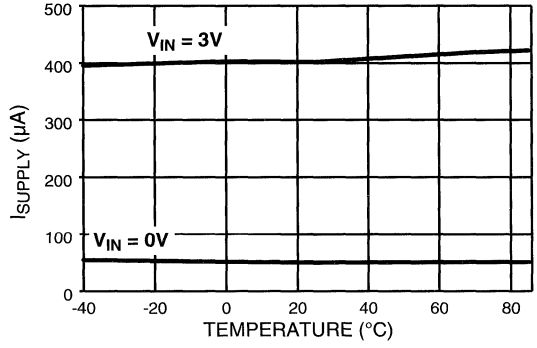
Quiescent Supply Current vs. Supply Voltage

T_A = 25°C



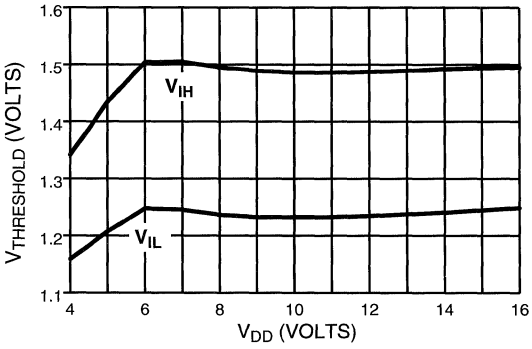
Quiescent Supply Current vs. Temperature

V_{SUPPLY} = 16V



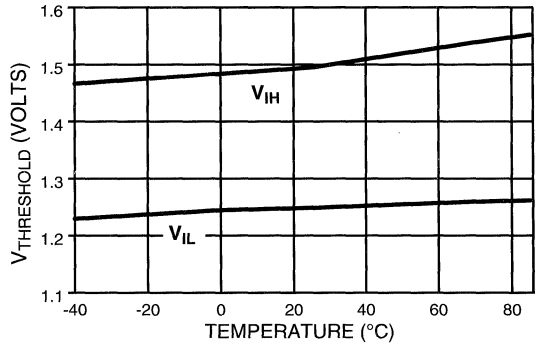
Input Threshold vs. Supply Voltage

T_A = 25°C

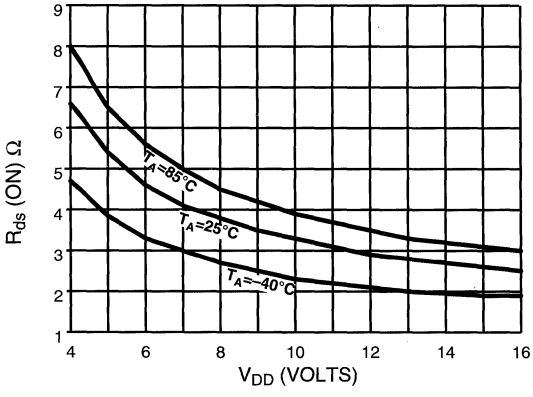


Input Threshold vs. Temperature

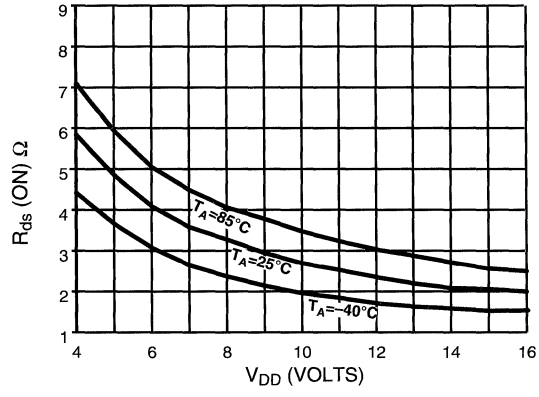
V_{SUPPLY} = 16V



High-State Output Resistance

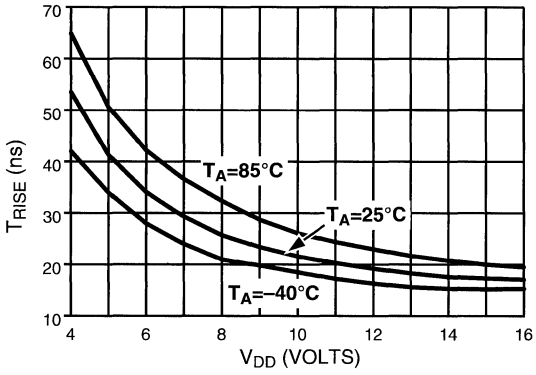


Low-State Output Resistance



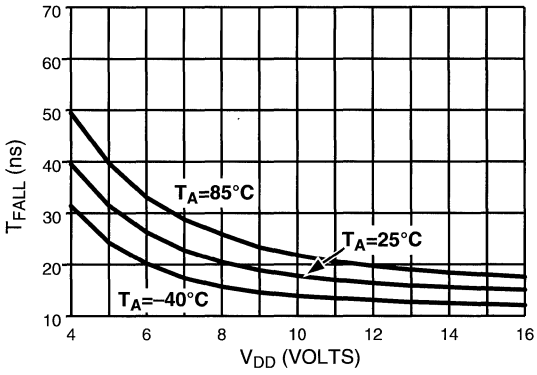
Rise Time vs. Supply Voltage

C_{LOAD} = 1800pF



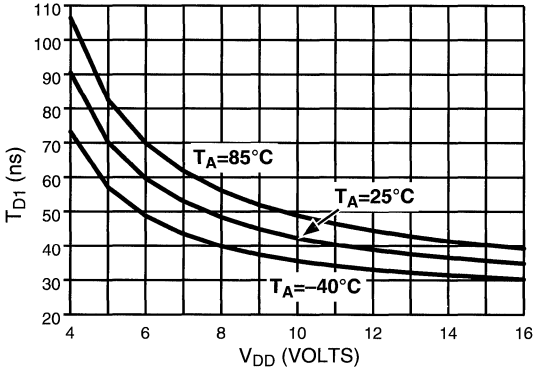
Fall Time vs. Supply Voltage

C_{LOAD} = 1800pF



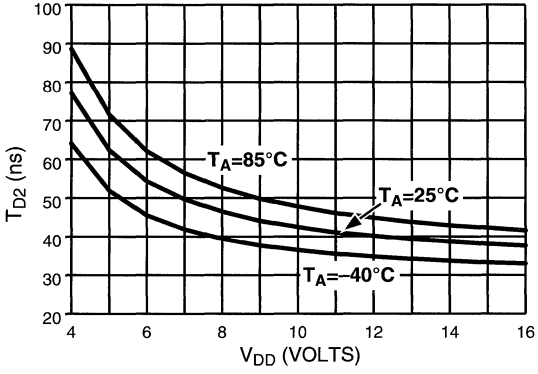
T_{D1} Propagation Delay vs. Supply Voltage

C_{LOAD} = 1800pF



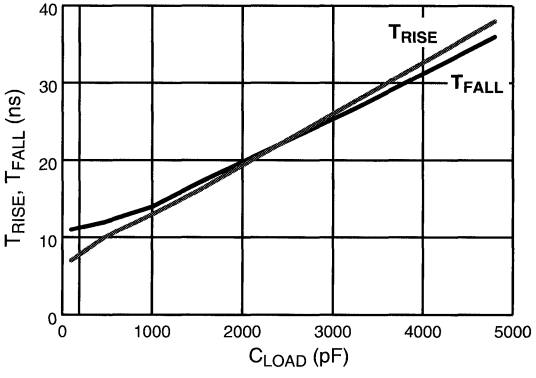
T_{D2} Propagation Delay vs. Supply Voltage

C_{LOAD} = 1800pF



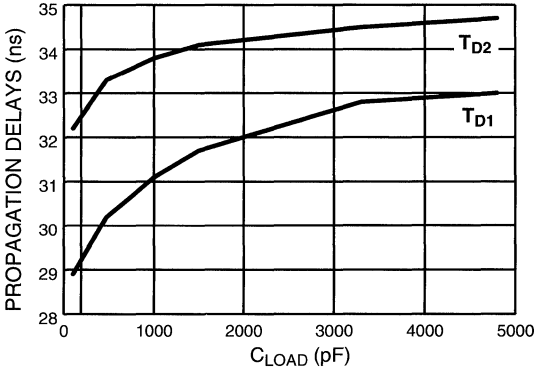
Rise and Fall Times vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V



Propagation Delays vs. Capacitive Load

T_A = 25°C, V_{DD} = 16V



1.2A DUAL HIGH-SPEED MOSFET DRIVERS

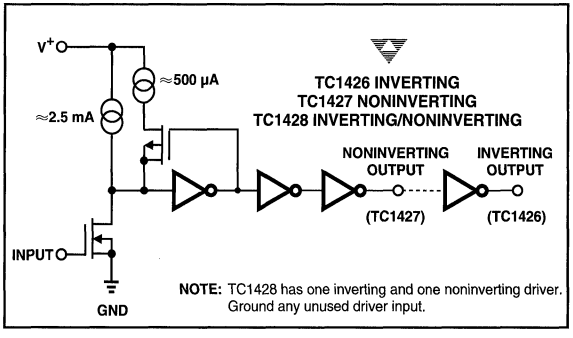
FEATURES

- **Low Cost**
- **Latch-Up Protected: Will Withstand 500 mA Reverse Output Current**
- **ESD Protected ..... ±2 kV**
- **High Peak Output Current ..... 1.2A Peak**
- **High Capacitive Load Drive Capability ..... 1000 pF in 38 ns**
- **Wide Operating Range ..... 4.5V to 16V**
- **Low Delay Time ..... 75 ns Max**
- **Logic Input Threshold Independent of Supply Voltage**
- **Output Voltage Swing to Within 25 mV of Ground or V_{DD}**
- **Low Output Impedance 8Ω**

APPLICATIONS

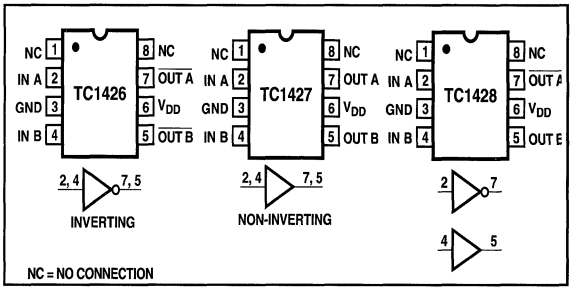
- **Power MOSFET Drivers**
- **Switched Mode Power Supplies**
- **Pulse Transformer Drive**
- **Small Motor Controls**
- **Print Head Drive**

FUNCTIONAL BLOCK DIAGRAM



NOTE: TC1428 has one inverting and one noninverting driver. Ground any unused driver input.

PIN CONFIGURATIONS



NC = NO CONNECTION

GENERAL DESCRIPTION

The TC1426/27/28 are a family of 1.2A dual high-speed drivers. They are ideal for high-volume OEM applications, with latch-up protection, ESD protection, and a proprietary molding compound for high reliability. CMOS fabrication is used for low power consumption and high efficiency.

These devices are fabricated using an epitaxial layer to effectively short out the intrinsic parasitic transistor responsible for CMOS latch-up. They incorporate a number of other design and process refinements to increase their long-term reliability.

The TC1426 is compatible with the bipolar DS0026, but only draws 1/5 of the quiescent current. The TC1426/27/28 are also compatible with the TC426/27/28, but with 1.2A peak output current rather than the 1.5A of the TC426/27/28 devices.

Other compatible drivers are the TC4426/27/28 and the TC4426A/27A/28A. The TC4426/27/28 have the added feature that the inputs can withstand negative voltage up to 5V with diode protection circuits. The TC4426A/27A/28A have matched input to output leading edge and falling edge delays, tD1 and tD2, for processing short duration pulses in the 25 nanoseconds range. All of the above drivers are pin compatible.

The high-input impedance TC1426/27/28 drivers are CMOS/TTL input-compatible, do not require the speed-up needed by the bipolar devices, and can be directly driven by most PWM ICs.

This family of devices is available in inverting and noninverting versions. Specifications have been optimized to achieve low-cost and high-performance devices, well-suited for the high-volume manufacturer.

ORDERING INFORMATION

Part No.	Package	Range
TC1426COA	8-Pin SO	0°C to +70°C
TC1426CPA	8-Pin Plastic DIP	0°C to +70°C
TC1427COA	8-Pin SO	0°C to +70°C
TC1427CPA	8-Pin Plastic DIP	0°C to +70°C
TC1428COA	8-Pin SO	0°C to +70°C
TC1428CPA	8-Pin Plastic DIP	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Power Dissipation
- Plastic DIP 1W
- SOIC ..... 500 mW

Derating Factor
- Plastic DIP ..... 8 mW/°C
- SOIC ..... 4 mW/°C

Supply Voltage 18V
Input Voltage, Any Terminal ... (V_{DD} + 0.3V) to (Gnd – 0.3V)
Operating Temperature: C Version ..... 0°C to +70°C
: E Version ..... - 40°C to +85°C
Maximum Chip Temperature ..... +150°C
Storage Temperature ..... +65°C to +150°C
Lead Temperature (10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated inthe operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C with 4.5V ≤ V_{DD} ⁺ ≤ 16V unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, Input Voltage		3	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage	Test Figures 1 and 2	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	Test Figures 1 and 2	—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10 mA, V_{DD} = 16V	—	12	18	Ω
		V_{IN} = 3V I_{OUT} = 10 mA, V_{DD} = 16V	—	8	12	Ω
I_{PK}	Peak Output Current		—	1.2	—	A
I	Latch-Up Current	Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Test Figures 1 and 2	—	22	30	ns
t_F	Fall Time	Test Figures 1 and 2	—	22	30	ns
t_{D1}	Delay Time	Test Figures 1 and 2	—	18	30	ns
t_{D2}	Delay Time	Test Figures 1 and 2	—	36	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	9	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.5	mA

Note: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS

(Over operating temperature range with $4.5V \leq V_{DD}^{+} \leq 16V$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, Input Voltage		3	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	Test Figures 1 and 2	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	Test Figures 1 and 2	—	—	0.025	V
R_O	Output Resistance	$V_{IN} = 0.8V$ $I_{OUT} = 10$ mA, $V_{DD} = 16V$	—	15	23	Ω
		$V_{IN} = 3V$ $I_{OUT} = 10$ mA, $V_{DD} = 16V$	—	10	18	Ω
I	Latch-Up Current	Withstand Reverse Current	>500	—	—	mA
Switching Time						
t_R	Rise Time	Test Figures 1 and 2	—	32	—	ns
t_F	Fall Time	Test Figures 1 and 2	—	32	—	ns
t_{D1}	Delay Time	Test Figures 1 and 2	—	25	—	ns
t_{D2}	Delay Time	Test Figures 1 and 2	—	45	—	ns
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ (Both Inputs)	—	—	13	mA
		$V_{IN} = 0V$ (Both Inputs)	—	—	0.7	mA

SUPPLY BYPASSING

Large currents are required to charge and discharge capacitive loads quickly. For example, charging a 1000-pF load to 16V in 25 ns requires an 0.8A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5-in.) should be used. A 1.0-µF film capacitor in parallel with one or two 0.1-µF ceramic MLC capacitors normally provides adequate bypassing.

GROUNDING

The TC1426 and TC1428 contain inverting drivers. Individual ground returns for the input and output circuits or a ground plane should be used. This will reduce negative feedback that causes degradation in switching speed characteristics.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 9 mA. Logic "0" input level signals reduce quiescent current to 500 µA maximum. **Unused driver inputs must be connected to V_{DD} or GND.** Minimum power dissipation occurs for logic "0" inputs for the TC1426/27/28.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making logic "1" input any voltage greater than 1.5V up to V_{DD}. Input current is less than 1 µA over this range.

The TC1426/27/28 may be directly driven by the TL494, SG1526/27, TC38C42, TC170 and similar switch-mode power supply integrated circuits.

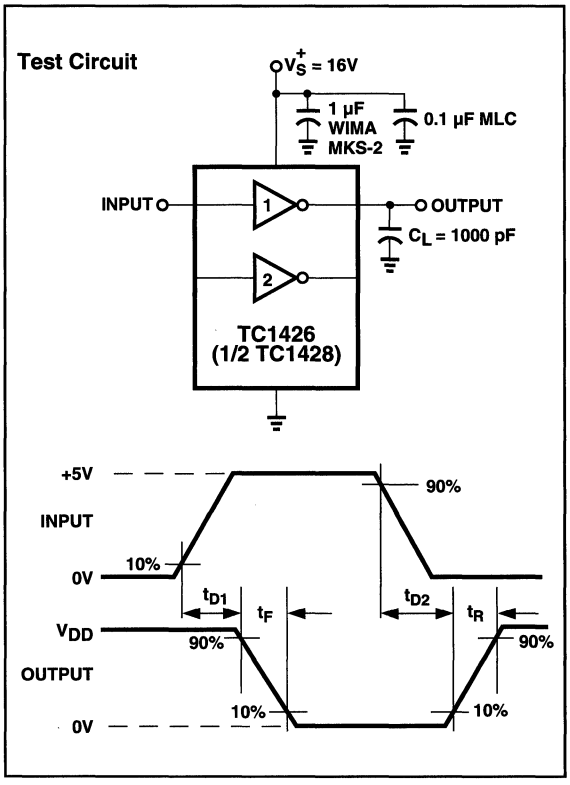


Figure 1. Inverting Driver Switching Time

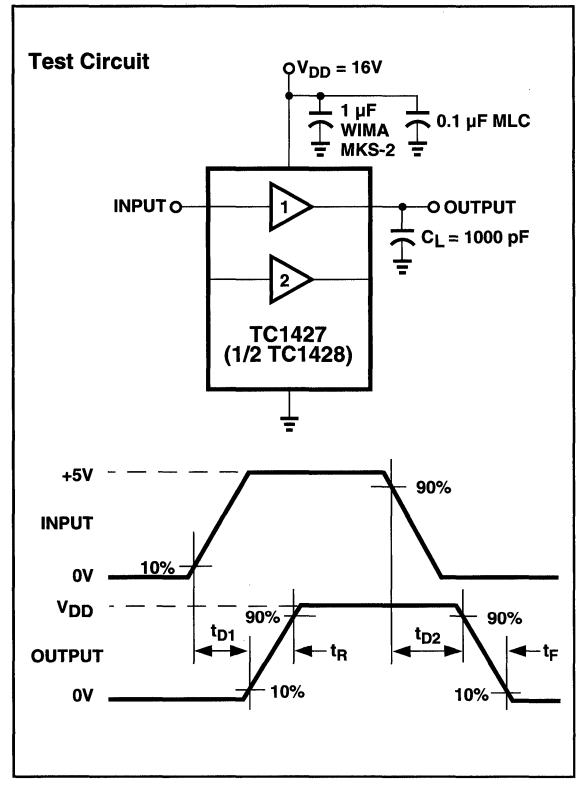
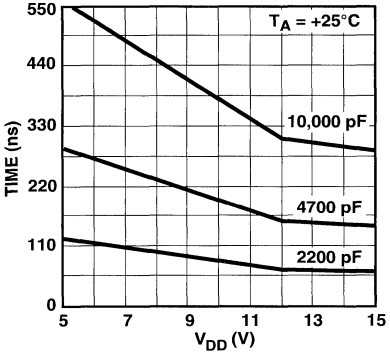


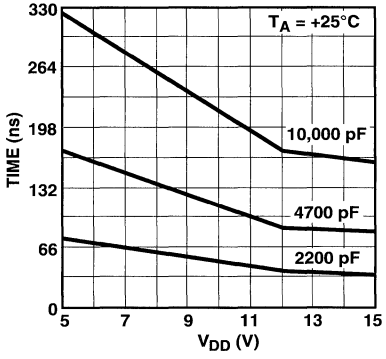
Figure 2. Non-Inverting Driver Switching Time

TYPICAL CHARACTERISTIC CURVES

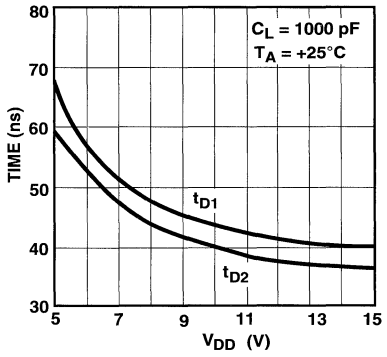
Rise Time vs Supply Voltage



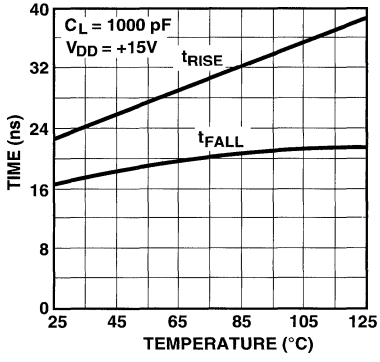
Fall Time vs Supply Voltage



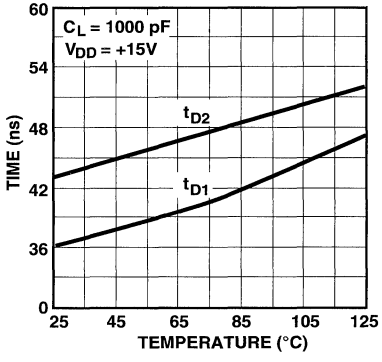
Delay Time vs Supply Voltage



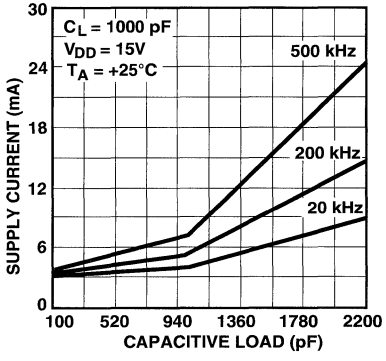
Rise and Fall Times vs Temperature



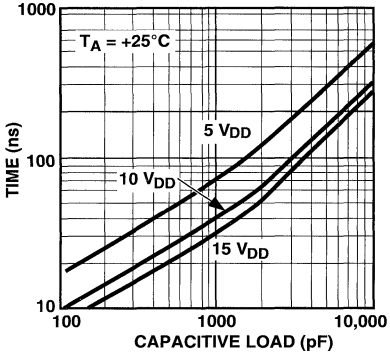
Delay Time vs Temperature



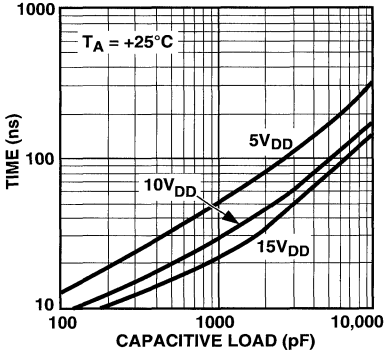
Supply Current vs Capacitive Load



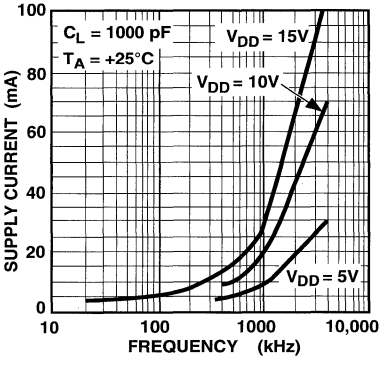
Rise Time vs Capacitive Load



Fall Time vs Capacitive Load

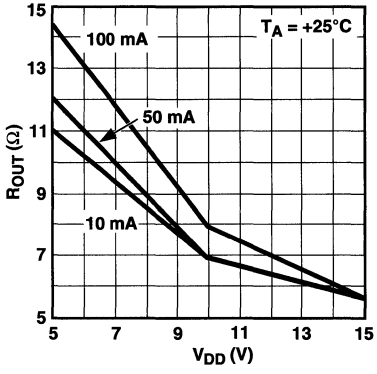


Supply Current vs Frequency

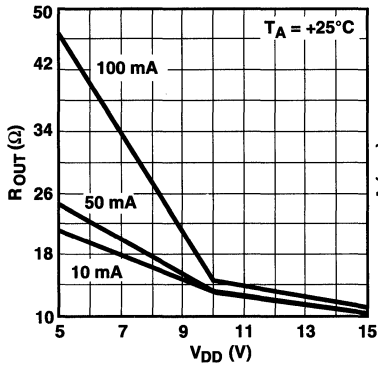


TYPICAL CHARACTERISTIC CURVES (Cont.)

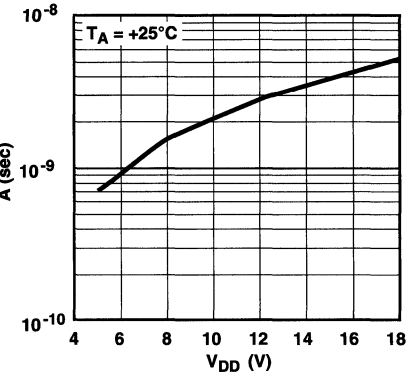
Low-State Output Resistance



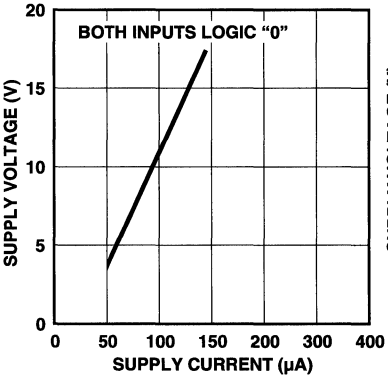
High-State Output Resistance



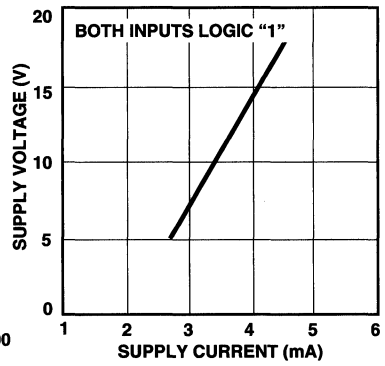
Crossover Energy Loss



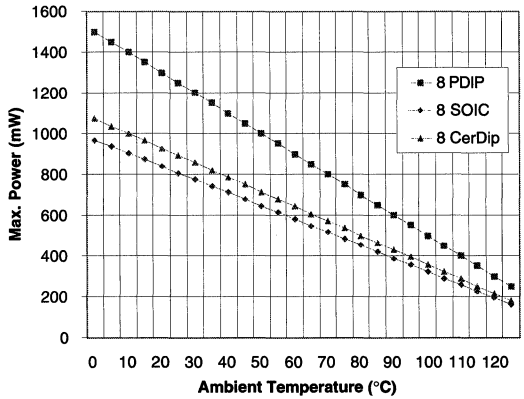
Quiescent Power Supply Current vs Supply Voltage



Quiescent Power Supply Current vs Supply Voltage



Thermal Derating Curve



6A OPEN-DRAIN MOSFET DRIVER

FEATURES

- **Independently-Programmable Rise and Fall Times**
- **High Peak Output Current ..... 6A Peak**
- **Low Output Impedance ..... 2.5Ω Typ**
- **High Speed t_R, t_F ..... <30 ns with 1800 pF Load**
- **Short Delay Times ..... 55ns Typ**
- **Wide Operating Range ..... 4.5V to 18V**

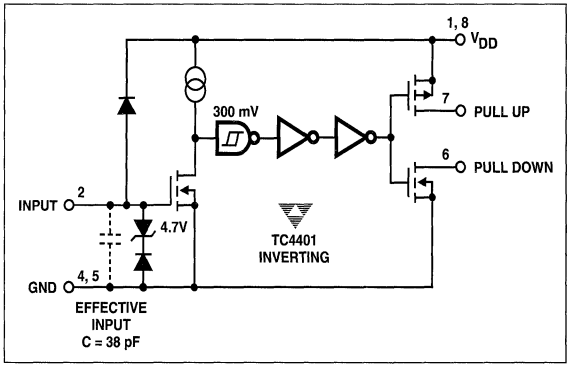
APPLICATIONS

- **Motor Controls**
- **Self-Commutating MOSFET Bridge Driver**
- **Driving Bipolar Transistors**
- **Driver for Nonoverlapping Totem Poles**
- **Reach-Up/Reach-Down Driver**

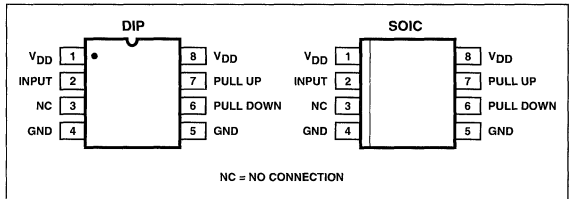
RUGGED

- **Tough CMOS Construction**
- **Latch-Up Protected: Will Withstand >1.5 A Reverse Current (Either Polarity) into Output**
- **Input Withstands Negative Swings Up to – 5V**
- **ESD Protected 4kV**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



NOTE: 1. Duplicate pins must both be connected for proper operation.

GENERAL DESCRIPTION

The TC4401 is a CMOS buffer-driver constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain current-limiting resistors in the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 2500-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, the TC4401 is superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because it allows accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for the device being driven.

The TC4401 is built using TelCom Semiconductor's new Tough CMOS process and is capable of giving reliable service in the most demanding electrical environments: it will not latch under any conditions within its power and voltage ratings; it is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin; and it can accept, without damage or logic upset, up to 1.5 amp of reverse current (of either polarity) being forced back into the outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4401CPA	8-Pin PDIP	0°C to +70°C
TC4401EPA	8-Pin PDIP	– 40°C to +85°C
TC4401COA	8-Pin SOIC	0°C to +70°C
TC4401EOA	8-Pin SOIC	– 40°C to +85°C
TC4401MJA	8-Pin CerDIP	– 55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Input Voltage ..... V_{DD} + 0.3V to GND - 5.0V
Input Current (V_{IN} > V_{DD}) 50mA
Power Dissipation, T_A ≤25°C
PDIP 1W
SOIC 500mW
CerDIP 800mW
Derating Factors (To Ambient)
PDIP ..... 8 mW/°C
SOIC ..... 4 mW/°C
CerDIP ..... 6.4 mW/°C
Storage Temperature Range ..... – 65°C to +150°C
Maximum Chip Temperature ..... +150°C
Operating Temperature Range
C Version ..... 0°C to +70°C
I Version ..... – 25°C to +85°C
E Version ..... – 40°C to +85°C
M Version ..... – 55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Low Input Voltage		—	1.3	0.8	V
V_{IN} (Max)	Input Voltage Range		– 5	—	V_{DD} + 0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.1	2.8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	1.5	2.5	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V	—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	55	75	ns
t_{D2}	Delay Time	Figure 1	—	55	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 55	1.5 150	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
V_{IN} (Max)	Input Voltage Range		– 5	—	V_{DD} + 0.3	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_S$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.3	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	32	60	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	34	60	ns
t_{D1}	Delay Time	Figure 1	—	50	100	ns
t_{D2}	Delay Time	Figure 1	—	65	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 60	3 400	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

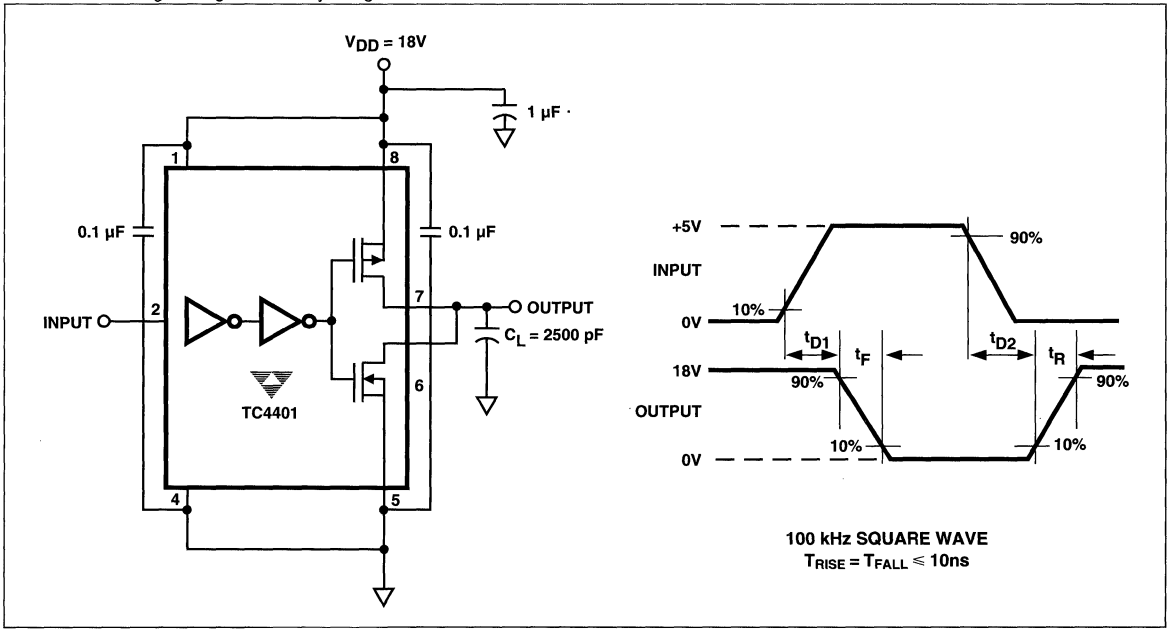
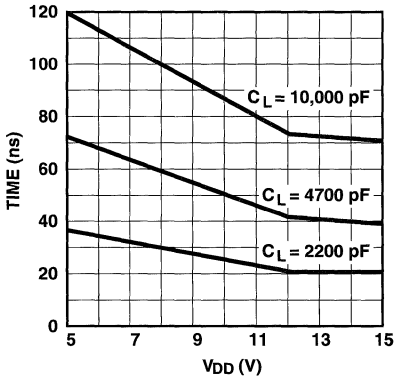


Figure 1. Switching Time Test Circuit

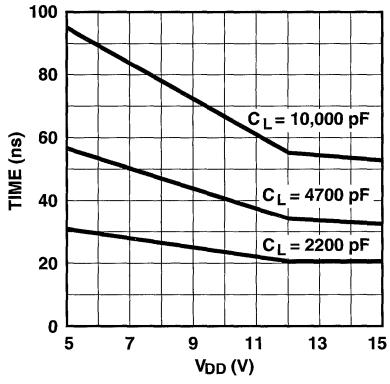
TC4401

TYPICAL CHARACTERISTICS CURVES

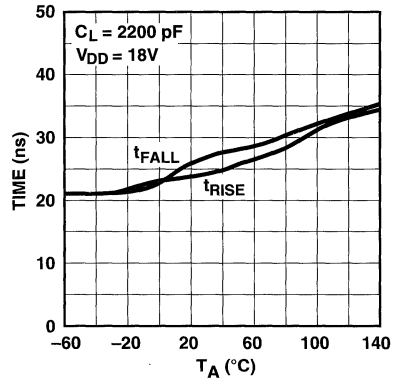
Rise Time vs Supply Voltage



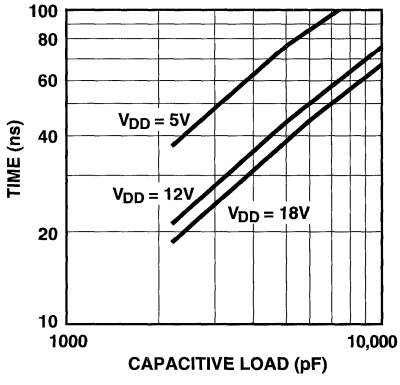
Fall Time vs Supply Voltage



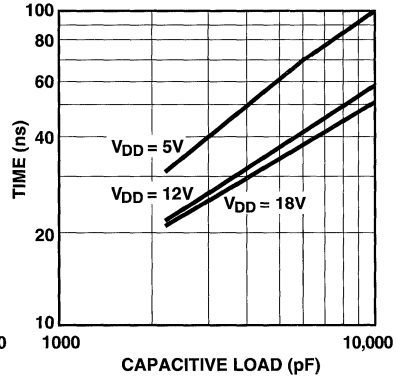
Rise and Fall Times vs Temperature



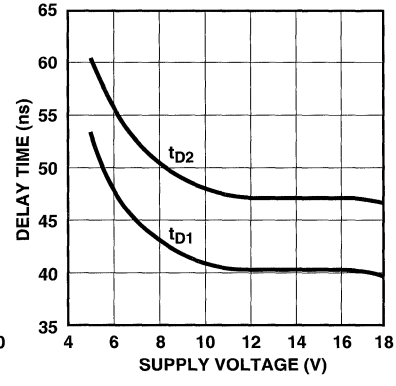
Rise Time vs Capacitive Load



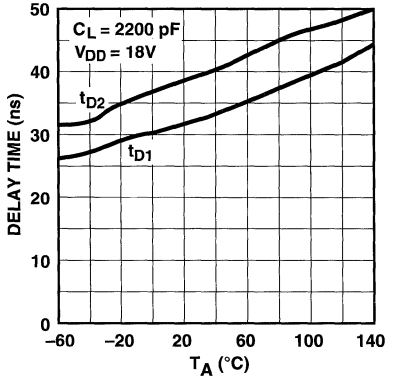
Fall Time vs Capacitive Load



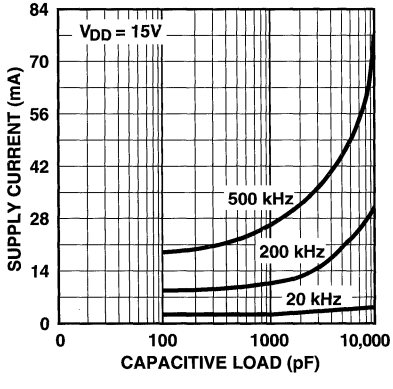
Propagation Delay Time vs Supply Voltage



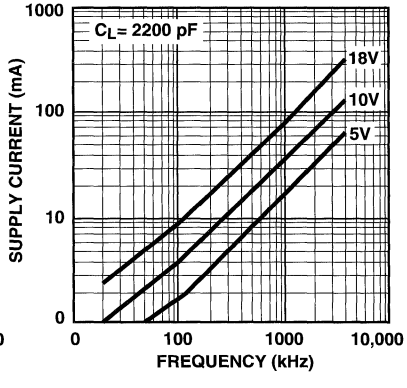
Propagation Delay Time vs Temperature



Supply Current vs Capacitive Load

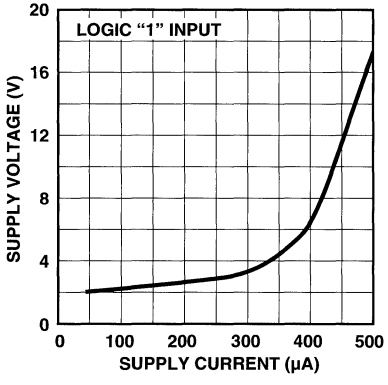


Supply Current vs Frequency

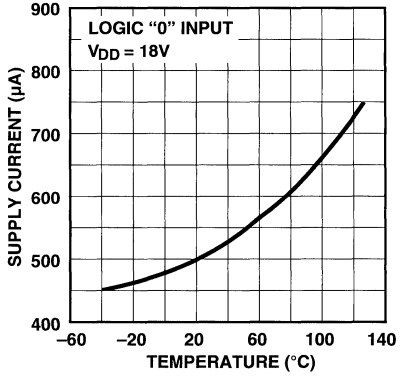


TYPICAL CHARACTERISTICS CURVES (Cont.)

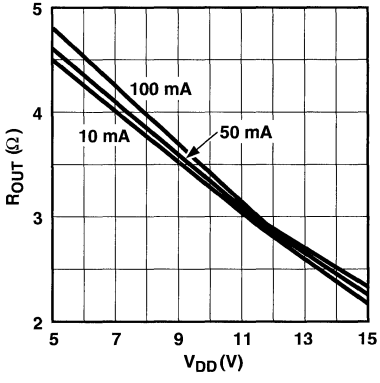
Quiescent Power Supply Current vs Supply Voltage



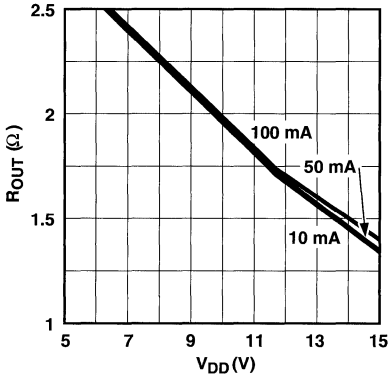
Quiescent Power Supply Current vs Temperature



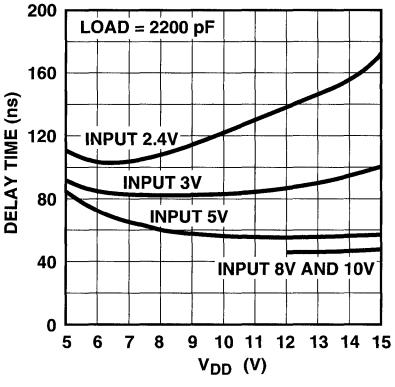
High-State Output Resistance



Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay



APPLICATION HINTS

When used to drive bipolar transistors, the TC4401 maintains the high speeds common to other TelCom drivers and allows insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-OFF. By proper positioning of the resistor, either npn or pnp transistors can be driven.

For driving many loads in low-power regimes, this driver, because it has very low quiescent current (<150 µA) and minimizes shoot-through currents in the output stage, requires significantly less power than similar drivers, and can be helpful in meeting low-power budgets.

Because neither drain in an output is dependent on the other (though they do switch simultaneously), this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused open drain should be returned to the supply rail that its device source is connected to (pull-down to ground, pull-up to V_{DD}), to prevent static damage. Alternatively, in situations where timing resistors, or other means of limiting crossover currents are used, multiple TC4401's may be paralleled for greater current-carrying capacity.

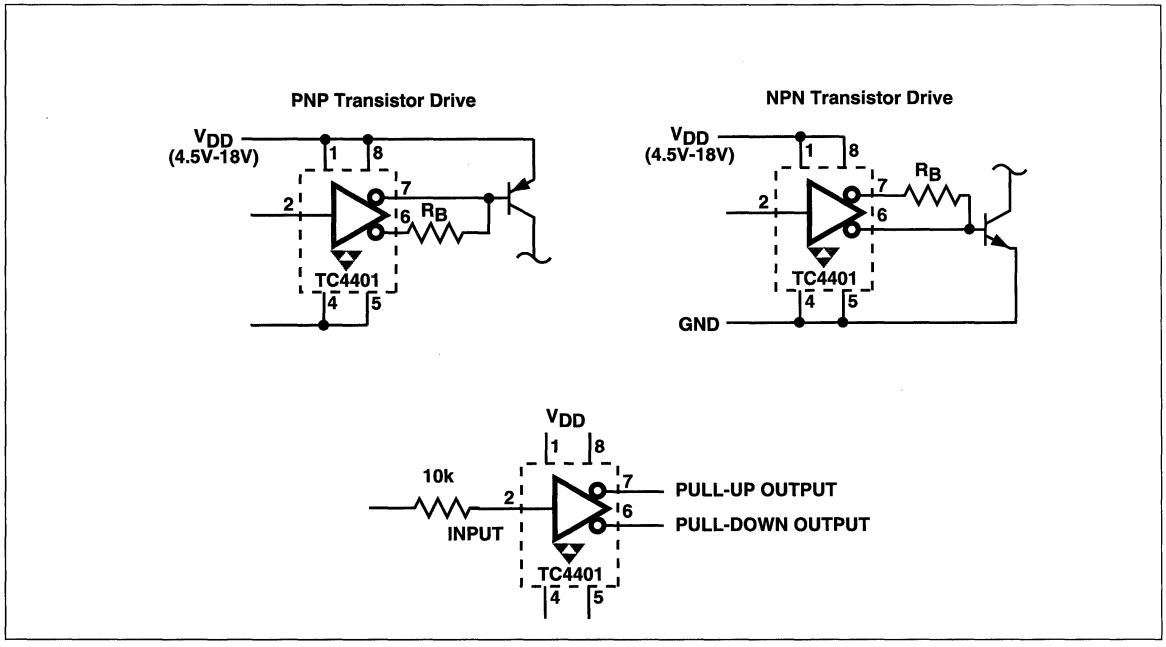
TC4401

POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement.

TYPICAL APPLICATION



At turn-ON, RB limits the base current in the transistor. The output that does the turn-OFF does not require a limiting resistor.

1.5A HIGH-SPEED, FLOATING LOAD DRIVER

FEATURES

- **Tough CMOS™ Construction**
- **Low Quiescent Current ..... 300 µA Max**
- **Capacitive Inputs With 300 mV Hysteresis**
- **Both Inputs Must Be Driven to Drive Load**
- **Low Output Leakage**
- **High Peak Current Capability**
- **Fast Output Rise Time**
- **Outputs Individually Testable**

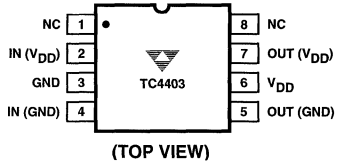
APPLICATIONS

- **Isolated Load Drivers**
- **Pulsers**
- **Safety Interlocks**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4403CPA	8-Pin PDIP	0°C to 70°C
TC4403EPA	8-Pin PDIP	–40°C to +85°C
TC4403MJA	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATION



(TOP VIEW)

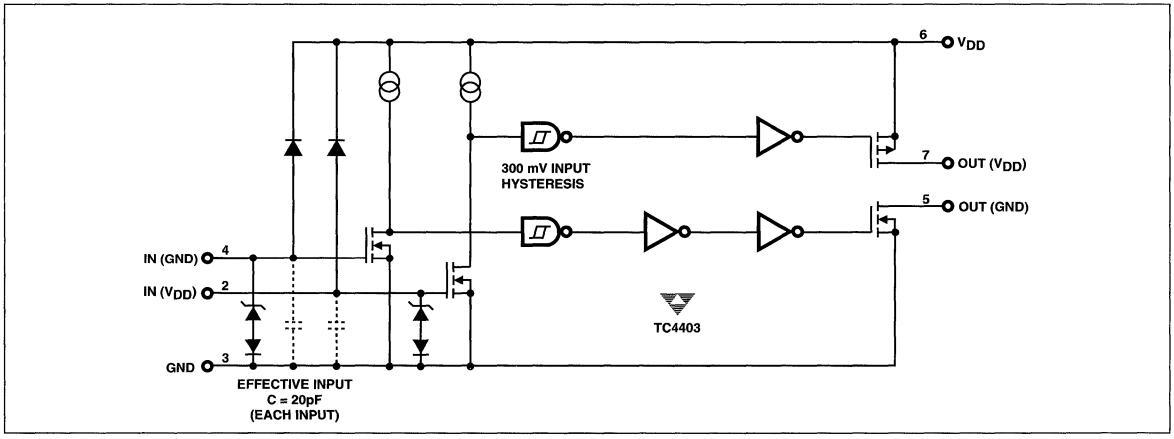
GENERAL DESCRIPTION

The TC4403 is a modified version of the TC4425 driver, intended to drive floating or isolated loads requiring high-current pulses. The load is intended to be connected between the outputs without other reference to supply or ground. Then, only when both logic inputs and the V_{DD} input are energized, is power supplied to the load. This construction allows the implementation of a wide variety of redundant input controllers.

The low OFF-state output leakage and independence of the two half-circuits permit a wide variety of testing schemes to be utilized to assure functionality. The high peak current capability, short internal delays, and fast output rise and fall times ensure that sufficient power will be available to the load when it is needed. The TTL and CMOS compatible inputs allow operation from a wide variety of input devices. The ability to swing the inputs negative without affecting device performance allows negative biases to be placed on the inputs for greater safety. In addition, the capacitive nature of the inputs allows the use of series resistors on the inputs for extra noise suppression.

The TC4403 is built using TelCom Semiconductor's new Tough CMOS process for outstanding ruggedness and reliability in harsh applications. Input voltage excursions above the supply voltage or below ground are clamped internally without damaging the device. The output stages are power MOSFETs with high-speed body diodes to prevent damage to the driver from inductive kickbacks.

FUNCTIONAL BLOCK DIAGRAM

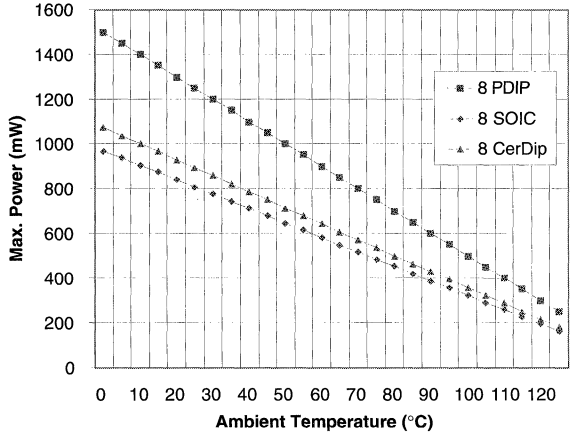


ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
CerDIP, $R_{\theta J-A}$ ..... 150°C/W
CerDIP, $R_{\theta J-C}$ ..... 50°C/W
PDIP, $R_{\theta J-A}$ ..... 125°C/W
PDIP, $R_{\theta J-C}$ ..... 42°C/W
Operating Temperature Range
C Version ..... 0°C to +70°C
E Version ..... –40°C to +85°C
M Version ..... –55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Thermal Derating Curve



ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ∂ V_{DD} ∂ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	-5V∂ V_{IN}∂ V_{DD}	–1000	±10	+1000	nA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OS}	Sourcing Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.8	5	Ω
R_{OG}	Grounding Output Resistance	I_{OUT} = –10 mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	33	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	1.5	2.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.15	0.25	mA

NOTE: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \leq V_{IN} \leq V_{DD}$	–10,000	±10	+10,000	nA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OS}	Sourcing Output Resistance	V_{IN} = 2.4V I_{OUT} = 10 mA, V_{DD} = 18V	—	3.7	8	Ω
R_{OG}	Grounding Output Resistance	V_{IN} = 2.4V I_{OUT} = –10 mA, V_{DD} = 18V	—	4.3	8	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	28	60	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	32	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	32	100	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	2 0.2	3.5 0.3	mA mA

NOTE: 1. Switching times guaranteed by design.

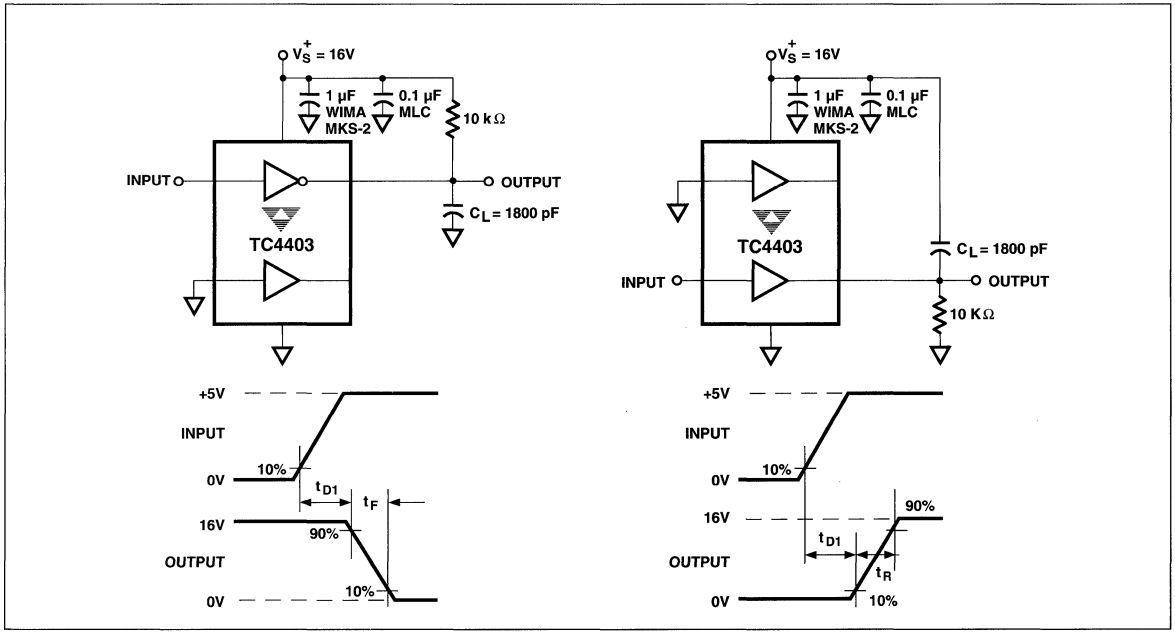
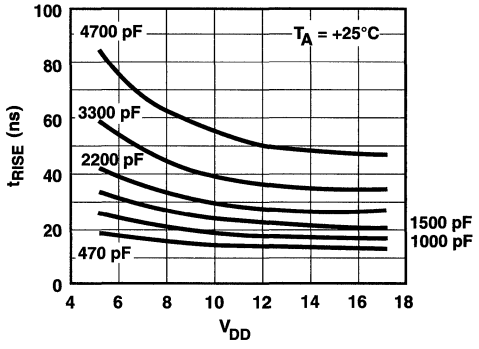


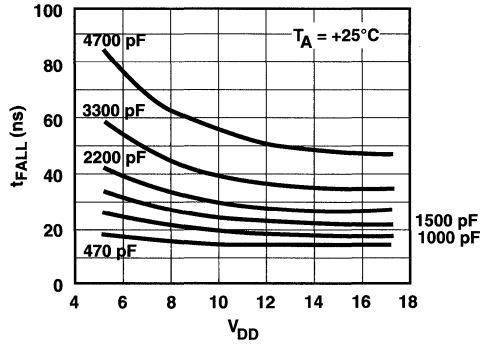
Figure 1 Switching Time Test Circuits

TYPICAL CHARACTERISTICS CURVES

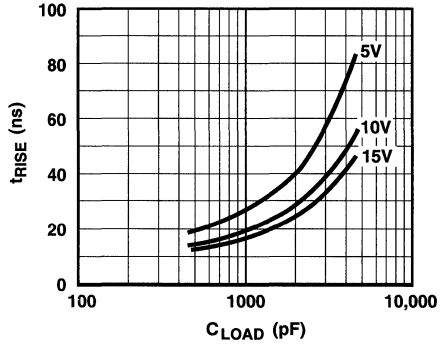
Rise Time vs Supply Voltage



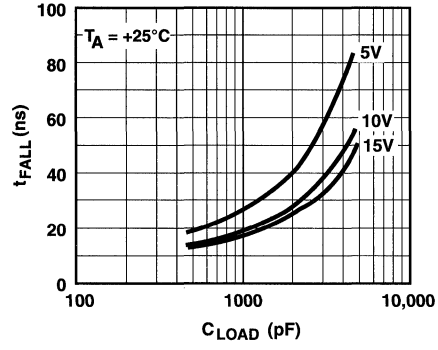
Fall Time vs Supply Voltage



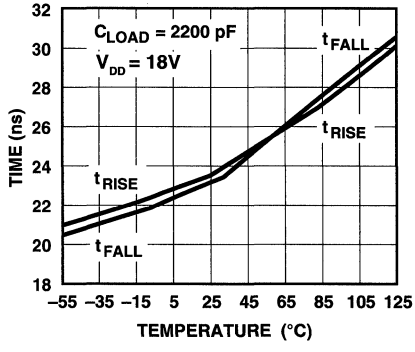
Rise TIme vs Capacitive Load



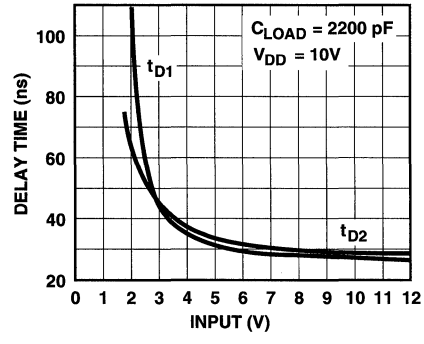
Fall Time vs Capacitive Load



Rise and Fall Times vs Temperature

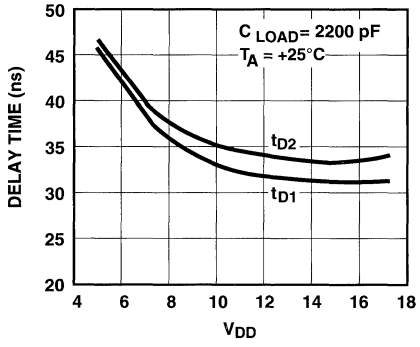


Propagation Delay vs Input Amplitude

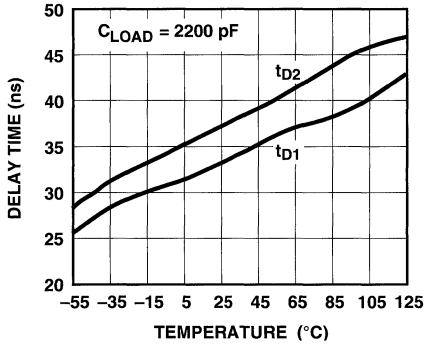


TYPICAL CHARACTERISTICS CURVES (Cont.)

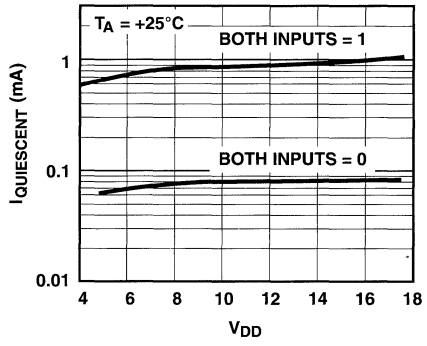
Delay Time vs Supply Voltage



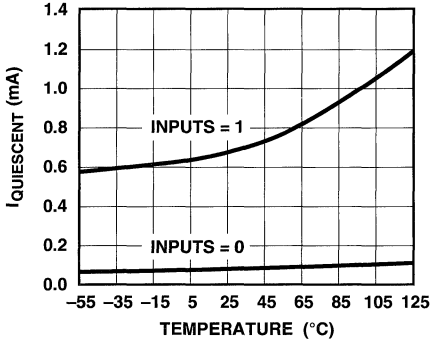
Delay Time vs Temperature



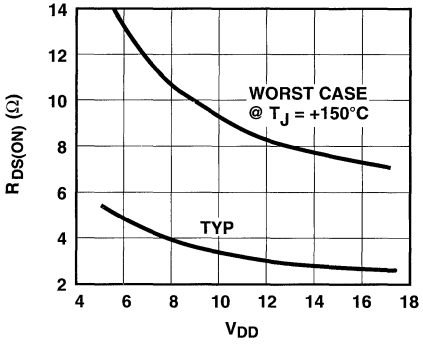
Quiescent Current vs Voltage



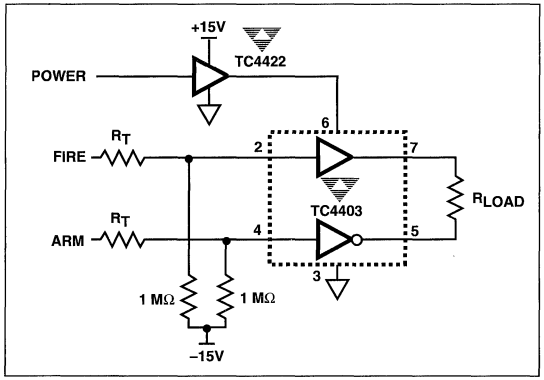
Quiescent Current vs Temperature



Output Resistance vs Supply Voltage



TYPICAL APPLICATION



1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- **Independently-Programmable Rise and Fall Times**
- **Low Output Impedance ..... 7Ω Typ**
- **High Speed t_R, t_F ..... <30 ns with 1000 pF Load**
- **Short Delay Times ..... < 30 ns**
- **Wide Operating Range ..... 4.5V to 18V**

APPLICATIONS

- **Motor Controls**
- **Driving Bipolar Transistors**
- **Driver for Nonoverlapping Totem Poles**
- **Reach-Up/Reach-Down Driver**

RUGGED

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand >500 mA Reverse Current (Either Polarity)**
- **Input Withstands Negative Swings Up to –5V**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4404CPA	8-Pin PDIP	0°C to +70°C
TC4404COA	8-Pin SOIC	0°C to +70°C
TC4405CPA	8-Pin PDIP	0°C to +70°C
TC4405COA	8-Pin SOIC	0°C to +70°C
TC4404EPA	8-Pin PDIP	– 40°C to +85°C
TC4404EOA	8-Pin SOIC	– 40°C to +85°C
TC4405EPA	8-Pin PDIP	– 40°C to +85°C
TC4405EOA	8-Pin SOIC	– 40°C to +85°C
TC4404MJA	8-Pin CerDIP	– 55°C to +125°C
TC4405MJA	8-Pin CerDIP	– 55°C to +125°C

GENERAL DESCRIPTION

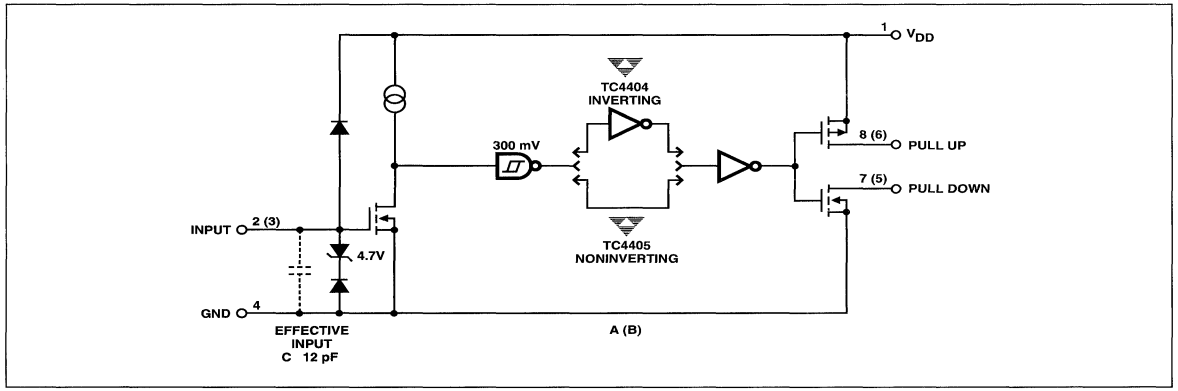
The TC4404 and TC4405 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the totem-pole output have been left separated so that individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of drain-current-limiting resistors in the pull-up and/or pull-down sections, allowing the user to define the rates of rise and fall for a capacitive load; or a reduced output swing, if driving a resistive load, or to limit base current, when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 1000-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-ON/fast-OFF operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for an OFF device.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other TelCom drivers. They allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-OFF. By proper positioning of the resistor, either npn or pnp transistors can be driven.

For driving many loads in low-power regimes, these drivers, because they eliminate shoot-through currents in the output stage, require significantly less power at higher frequencies, and can be helpful in meeting low-power budgets.

FUNCTIONAL BLOCK DIAGRAM



Because neither drain in an output is dependent on the other, these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail that their device sources are connected to (pull-downs to ground, pull-ups to V_{DD}), to prevent static damage. In addition, in situations where timing resistors or other means of limiting crossover currents are used, like drains may be paralleled for greater current carrying capacity.

These devices are built using TelCom Semiconductors' new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments: they will not latch up under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

Specifications measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	– 5V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	7	10	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle <2%, t ≤ 300µsec	—	1.5	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	100	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle <2%, t ≤ 300µsec	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	25	30	ns
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	25	30	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	15	30	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	32	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	4.5	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

NOTE: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS: Specifications measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \leq V_{IN} \leq V_{DD}$	−10	—	10	µA
Output						
V_{OH}	High Output Voltage		$V_{DD} - 0.025$	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	9	12	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle <2%, t ≤ 300µsec	—	1.5	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	100	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle <2%, t ≤ 300µsec	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	—	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	mA

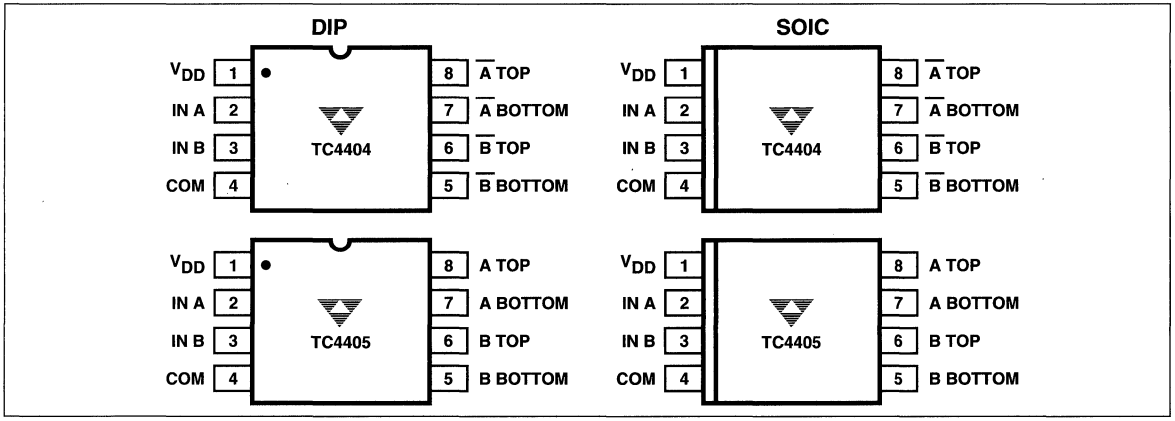
NOTE 1. Switching times guaranteed by design.

POWER-ON OSCILLATION

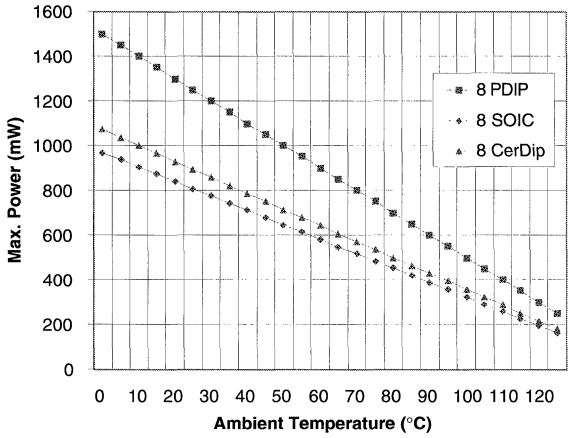
It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement.

PIN CONFIGURATIONS



Thermal Derating Curve



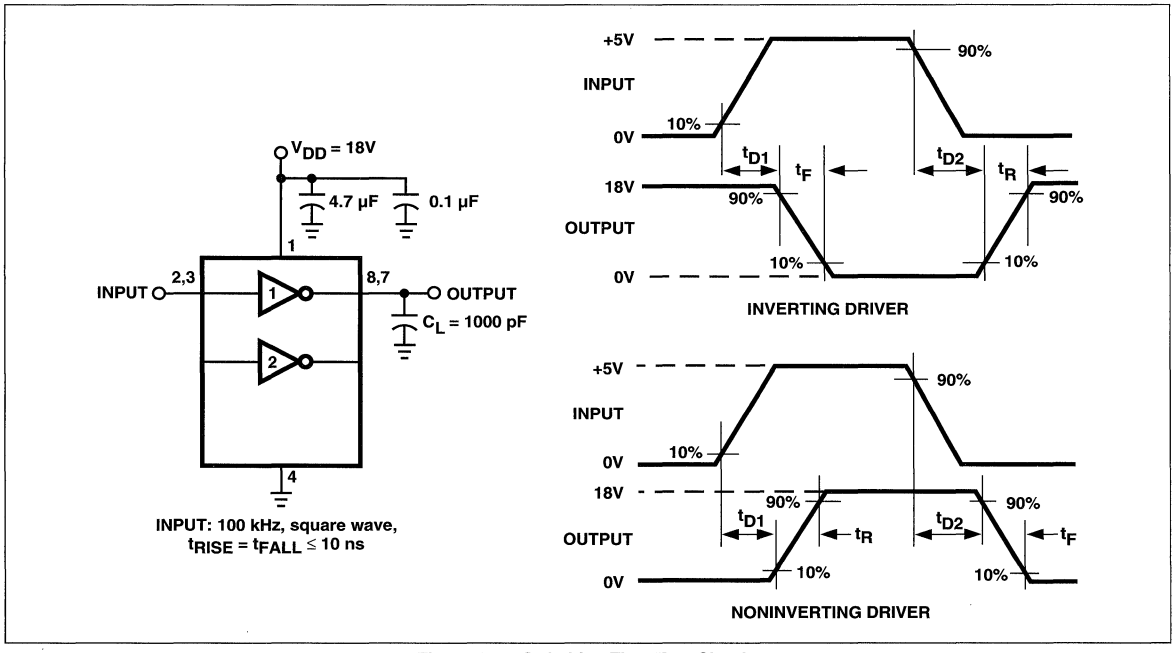
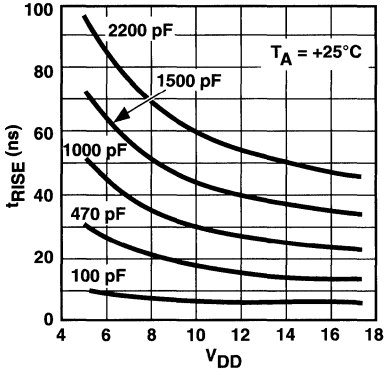


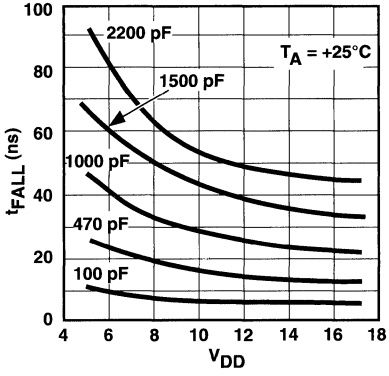
Figure 1 Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

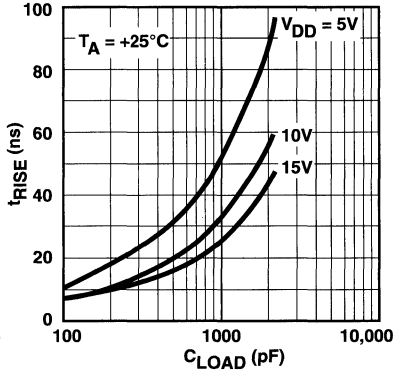
Rise Time vs. Supply Voltage



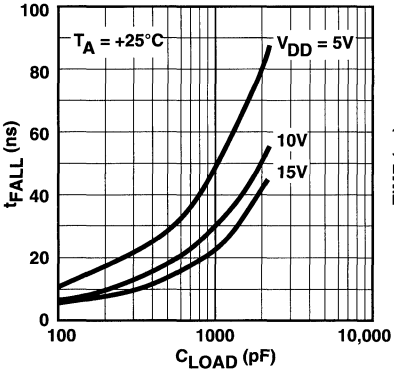
Fall Time vs. Supply Voltage



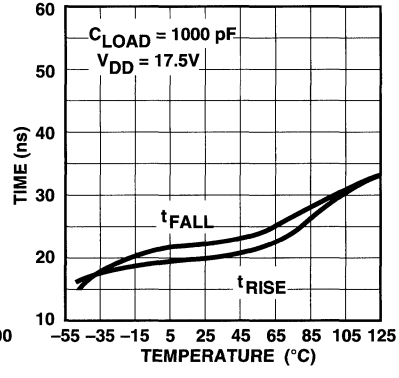
Rise TIme vs. Capacitive Load



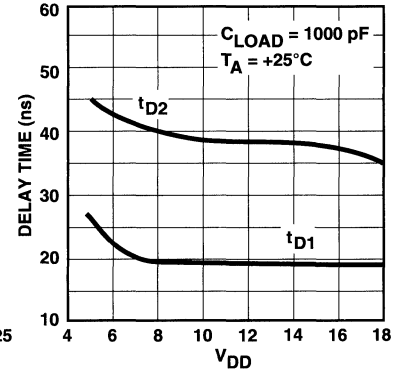
Fall Time vs. Capacitive Load



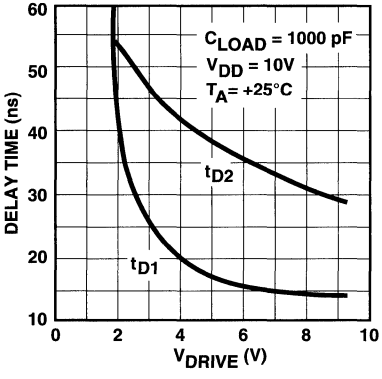
Rise and Fall Times vs. Temperature



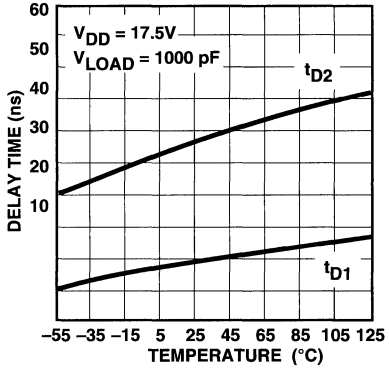
Propagation Delay vs. Supply Voltage



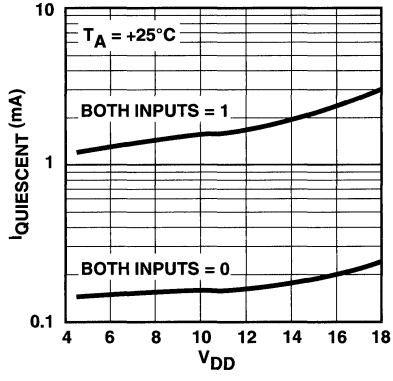
Effect of Input Amplitude on Delay Time



Propagation Delay Time vs. Temperature



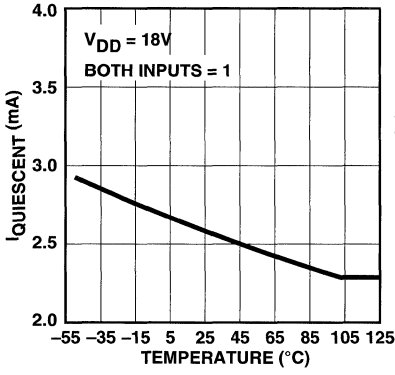
Quiescent Supply Current vs. Voltage



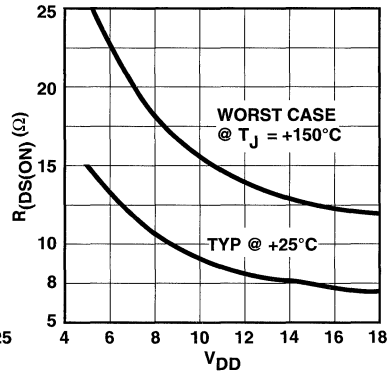
3

TYPICAL CHARACTERISTICS CURVES (Cont.)

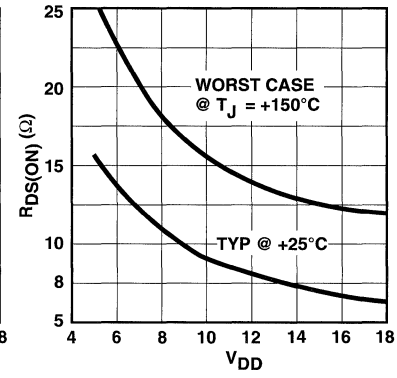
Quiescent Supply Current vs. Temperature



Pull-Up Output Resistance

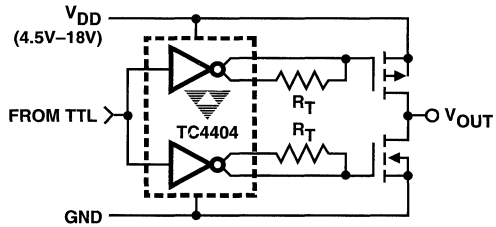


Pull-Down Output Resistance

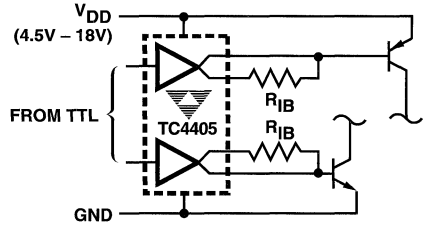


TYPICAL APPLICATIONS

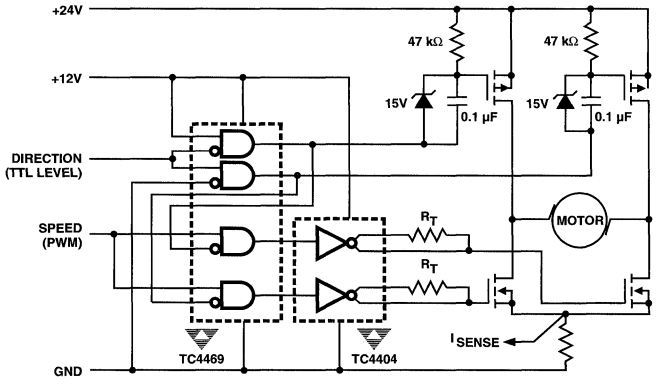
Zero Crossover Current Totem-Pole Switch



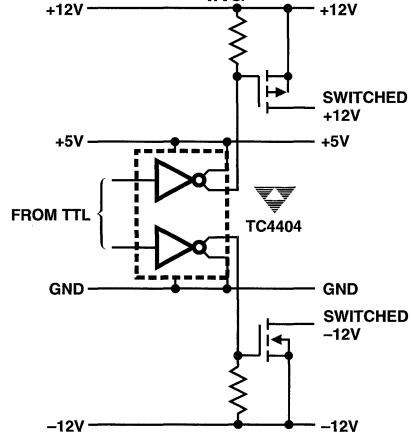
Driving Bipolar Transistors



Servo Motor Control



REACH-UP AND REACH-DOWN DRIVING



3A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- **Independently-Programmable Rise and Fall Times**
- **Low Output Impedance ..... 3.5Ω Typ**
- **High Speed t_R, t_F .... <30 ns with 1800 pF Load Typ**
- **Short Delay Times ..... 35 ns Typ**
- **Wide Operating Range ..... 4.5V to 18V**

APPLICATIONS

- **Motor Controls**
- **Driving Bipolar Transistors**
- **Driver for Nonoverlapping Totem Poles**
- **Reach-Up/Reach-Down Driver**

RUGGED

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand >500 mA Reverse Current (Either Polarity)**
- **Input Withstands Negative Swings Up to –5V**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4406CPA	8-Pin PDIP	0°C to +70°C
TC4406EPA	8-Pin PDIP	– 40°C to + 85°C
TC4406EOE	16-Pin SO Wide	– 40°C to + 85°C
TC4406MJA	8-Pin CerDIP	– 55°C to +125°C
TC4406COE	16-Pin SO Wide	0°C to +70°C
TC4407CPA	8-Pin PDIP	0°C to +70°C
TC4407EPA	8-Pin PDIP	– 40°C to + 85°C
TC4407EOE	16-Pin SO Wide	– 40°C to + 85°C
TC4407MJA	8-Pin CerDIP	– 55°C to +125°C
TC4407COE	16-Pin SO Wide	0°C to +70°C

GENERAL DESCRIPTION

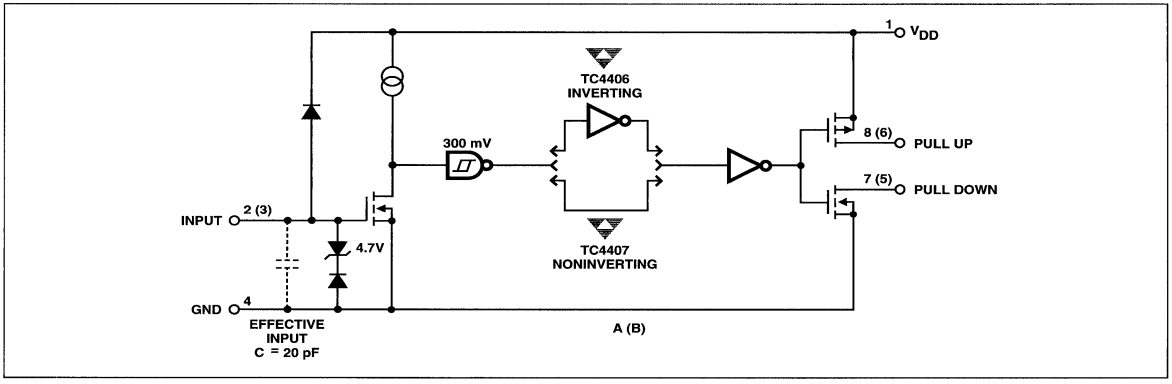
The TC4406 and TC4407 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the totem-pole output have been left separated so that individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of drain current-limiting resistors in the pull-up and/or pull-down sections, allowing the user to define the rates of rise and fall for a capacitive load; or a reduced output swing, if driving a resistive load, or to limit base current, when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 1800-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-ON/fast-OFF operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for the device being driven.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other TelCom drivers. They allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-OFF. By proper positioning of the resistor, either npn or pnp transistors can be driven.

For driving many loads in low-power regimes, these drivers, because they have very low quiescent current (<250 μA) and minimize shoot-through currents in the output stage, require significantly less power than similar drivers, and can be helpful in meeting low-power budgets.

FUNCTIONAL BLOCK DIAGRAM



Because neither drain in an output is dependent on the other (though they do switch simultaneously), these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail that their device sources are connected to (pull-downs to ground, pull-ups to V_{DD}), to prevent static damage. Alternatively, in situations where timing resistors or other means of limiting crossover currents are used, like drains may be paralleled for greater current-carrying capacity.

The TC4406 and TC4407 are built using TelCom Semiconductor' new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments: they will not latch up under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

unless otherwise specified, specifications measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	– 5V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, Pull Up	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.8	5	Ω
R_O	Output Resistance, Pull Down	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle <2%, t ≤ 300µsec	—	3	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	150	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle <2%, t ≤ 300µsec	> 500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	33	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	1.5	2.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.15	0.25	mA

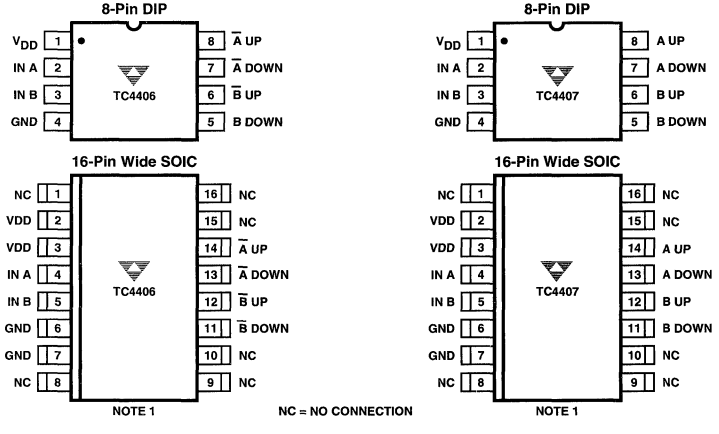
ELECTRICAL CHARACTERISTICS:

Specifications measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \leq V_{IN} \leq V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, Pull Up	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.7	8	Ω
R_O	Output Resistance, Pull Down	I_{OUT} = 10 mA, V_{DD} = 18V	—	4.3	8	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle <2%, t ≤ 300µsec	—	3	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	150	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle <2%, t ≤ 300µsec	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	—	60	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	—	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	—	100	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	—	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	2	3.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.2	0.3	mA

NOTE : 1. Switching times guaranteed by design.

PIN CONFIGURATIONS



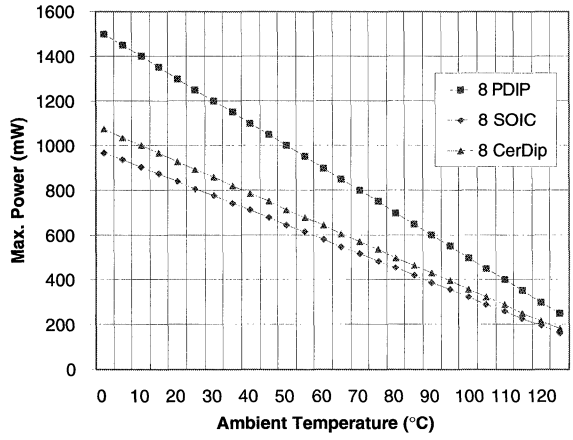
NOTE: 1. Duplicate pins must both be connected for proper operation.

POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement.

Thermal Derating Curve



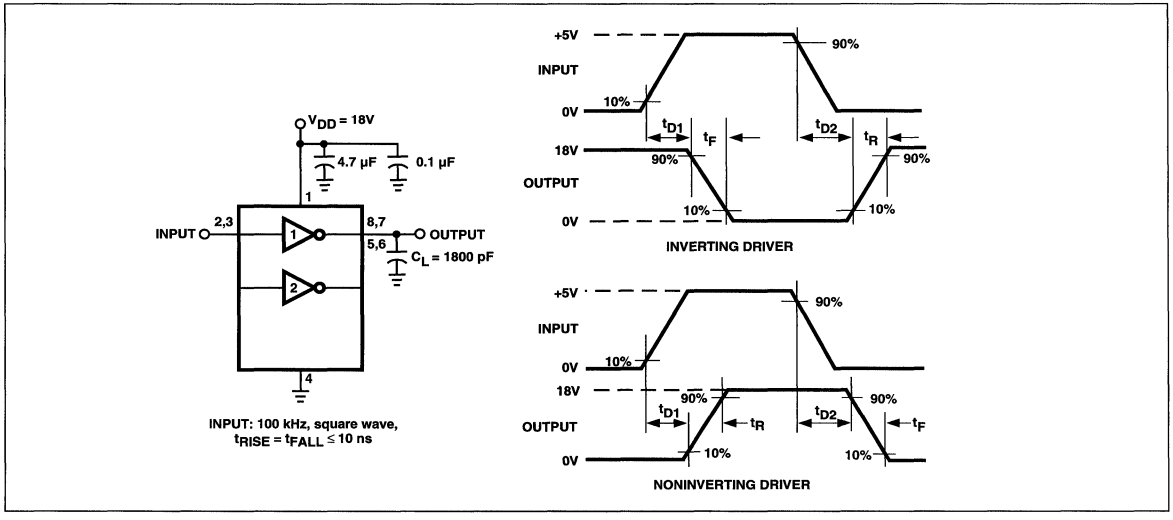
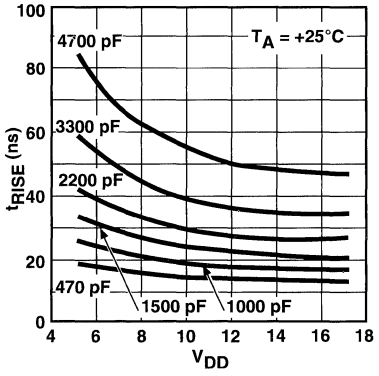


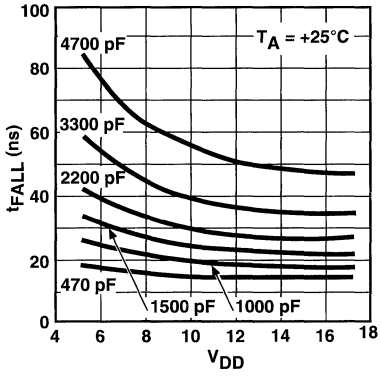
Figure 1 Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

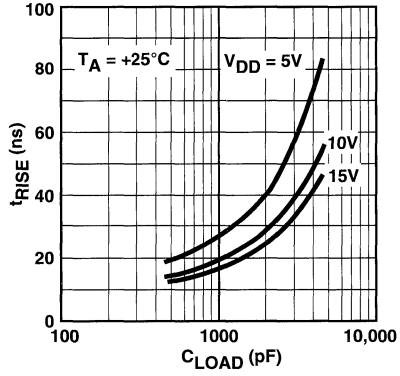
Rise Time vs. Supply Voltage



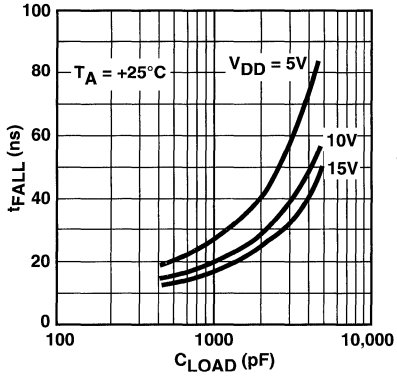
Fall Time vs. Supply Voltage



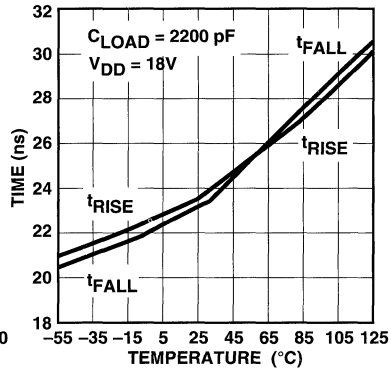
Rise Time vs. Capacitive Load



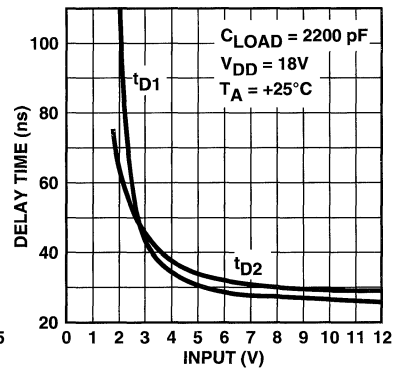
Fall Time vs. Capacitive Load



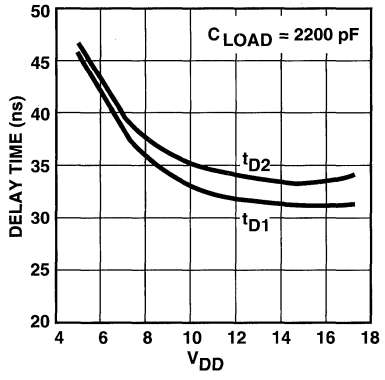
Rise and Fall Times vs. Temperature



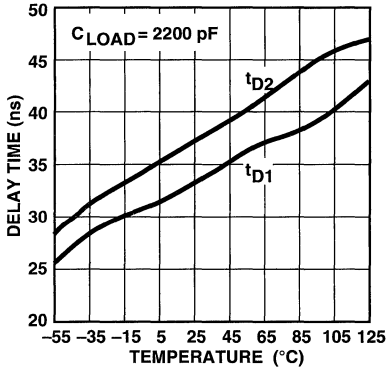
Propagation Delay vs. Input Amplitude



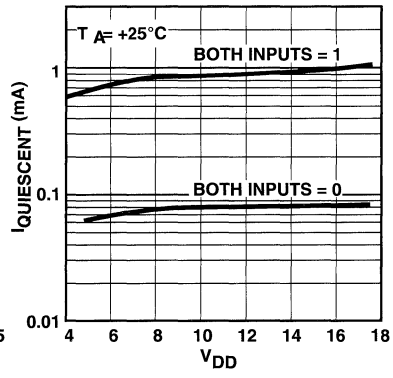
Propagation Delay Time vs. Supply Voltage



Propagation Delay Time vs. Temperature

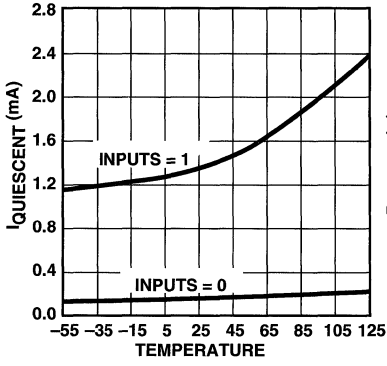


Quiescent Supply Current vs. Voltage

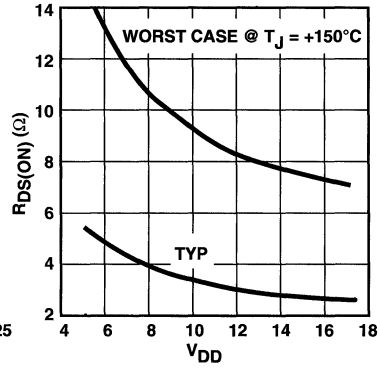


TYPICAL CHARACTERISTICS CURVES (Cont.)

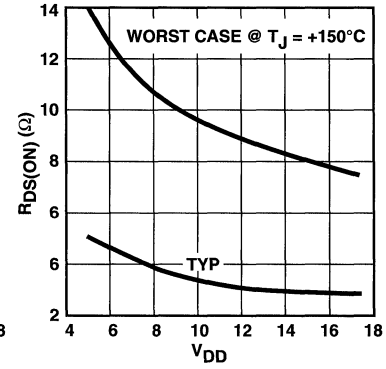
Quiescent Current vs. Temperature



Output Resistance (Pull Up) vs. Supply Voltage

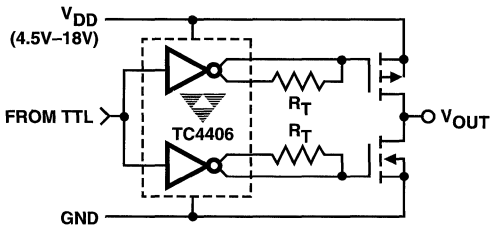


Output Resistance (Pull Down) vs. Supply Voltage

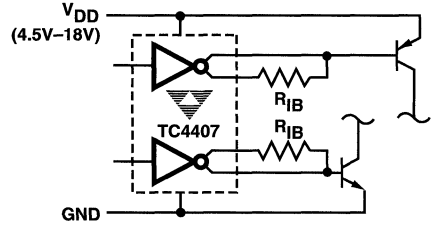


TYPICAL APPLICATIONS

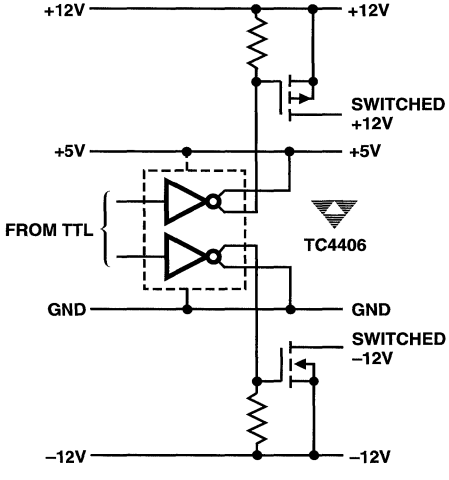
Zero Crossover-Current Totem-Pole Switch



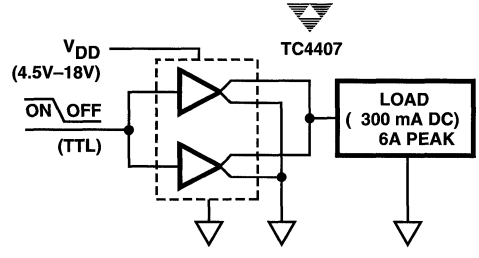
Driving Bipolar Transistors



Reach-Up and Reach-Down Driving



High-Side Switch



NOTE: Unused drains should be connected to their respective supplies.

6A HIGH-SPEED MOSFET DRIVERS

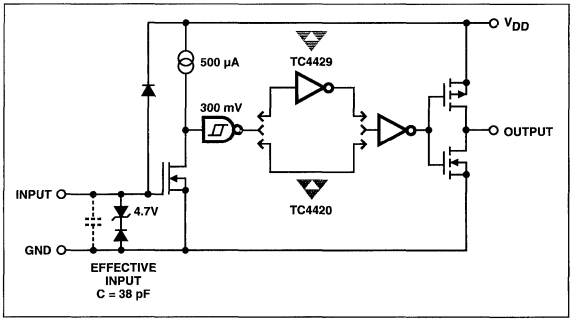
FEATURES

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand >1.5A Reverse Output Current**
- **Logic Input Will Withstand Negative Swing Up to 5V**
- **ESD Protected ..... 4 kV**
- **Matched Rise and Fall Times ..... 25 ns**
- **High Peak Output Current ..... 6A Peak**
- **Wide Operating Range ..... 4.5V to 18V**
- **High Capacitive Load Drive ..... 10,000 pF**
- **Short Delay Time ..... 55 ns Typ**
- **Logic High Input, Any Voltage ..... 2.4V to V_{DD}**
- **Low Supply Current With Logic "1" Input ..450 µA**
- **Low Output Impedance 2.5Ω**
- **Output Voltage Swing to Within 25 mV of Ground or V_{DD}**

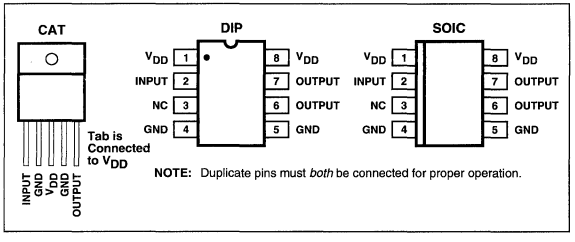
APPLICATIONS

- **Switch-Mode Power Supplies**
- **Motor Controls**
- **Pulse Transformer Driver**
- **Class D Switching Amplifiers**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC4420/4429 Tough CMOS™ drivers are efficient and easy to use. These devices are 6A (peak) single output MOSFET drivers.

The TC4420/4429 will drive even the largest MOSFETs.

These devices are tough due to extra steps taken to protect them from failures. An epitaxial layer is used to prevent CMOS latch-up. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part. Special circuits have been added to protect against damage from electrostatic discharge. A special molding compound is used for increased moisture resistance and ability to withstand high voltages.

Because these devices are fabricated in CMOS, they run cool, use less power and are easier to drive. The rail-to-rail swing capability of CMOS better insures adequate gate voltage to the MOSFET during power up/down sequencing.

The Tough CMOS™ drivers are easy to use. Three or more discrete components can be replaced with a single device to save PCB area. Any logic input from 2.4V to V_{DD} can be used without external speed-up capacitors or resistor networks.

This family is available in inverting (TC4429) and noninverting (TC4420) configurations. The TC4429 is pin compatible with the popular TC429.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4420CPA	Noninverting	8-Pin PDIP	0°C to +70°C
TC4420EPA	Noninverting	8-Pin PDIP	–40°C to +85°C
TC4420COA	Noninverting	8-Pin SOIC	0°C to +70°C
TC4420EOA	Noninverting	8-Pin SOIC	–40°C to +85°C
TC4420IJA	Noninverting	8-Pin CerDIP	–25°C to +85°C
TC4420MJA	Noninverting	8-Pin CerDIP	–55°C to +125°C
TC4420CAT	Noninverting	5-Pin TO-220	0°C to +70°C
TC4429CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4429EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4429COA	Inverting	8-Pin SOIC	0°C to +70°C
TC4429EOA	Inverting	8-Pin SOIC	–40°C to +85°C
TC4429IJA	Inverting	8-Pin CerDIP	–25°C to +85°C
TC4429MJA	Inverting	8-Pin CerDIP	–55°C to +125°C
TC4429CAT	Inverting	5-Pin TO-220	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage ..... – 5V to >V_{DD}
Input Current (V_{IN} > V_{DD}) ..... 50 mA
Power Dissipation, $T_A \leq 25°C$
PDIP 1W
SOIC ..... 500 mW
CerDIP ..... 800 mW
5-Pin TO-220 ..... 1.5W
Power Dissipation, $T_C \leq 25°C$
5-Pin TO-220 ..... 12.5W
Derating Factors (To Ambient)
PDIP ..... 8 mW/°C
SOIC ..... 4 mW/°C
CerDIP ..... 6.4 mW/°C
5-Pin TO-220 ..... 12 mW/°C
Thermal Impedances (To Case)
5-Pin TO-220 $R_{\theta J-A}$ ..... 10°C/W

Storage Temperature Range ..... – 65°C to +150°C
Operating Temperature (Chip) ..... +150°C
Operating Temperature Range (Ambient)
C Version ..... 0°C to +70°C
I Version ..... – 25°C to +85°C
E Version ..... – 40°C to +85°C
M Version ..... – 55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

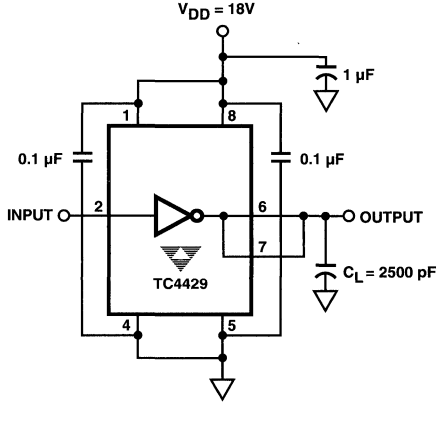
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Low Input Voltage		—	1.3	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.1	2.8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	1.5	2.5	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V (See Figure 5)	—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	55	75	ns
t_{D2}	Delay Time	Figure 1	—	55	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 55	1.5 150	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

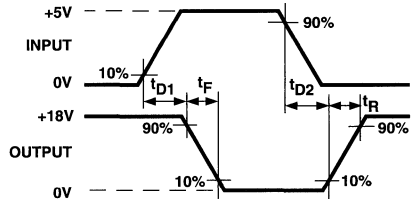
ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
V_{IN} (Max)	Input Voltage Range		– 5	—	V_{DD} + 0.3	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_S$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.3	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	32	60	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	34	60	ns
t_{D1}	Delay Time	Figure 1	—	50	100	ns
t_{D2}	Delay Time	Figure 1	—	65	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 60	3 400	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.



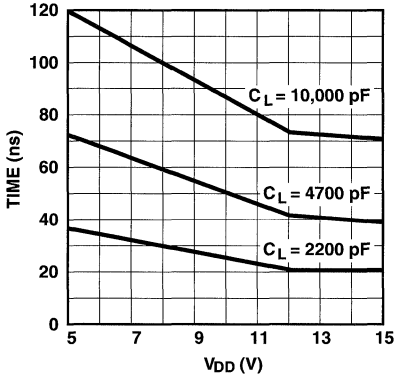


INPUT: 100 kHz, square wave,
$t_{RISE} = t_{FALL} \le 10$ nS

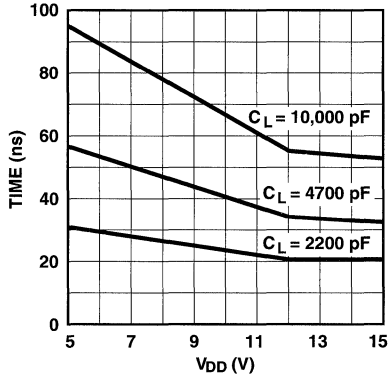
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

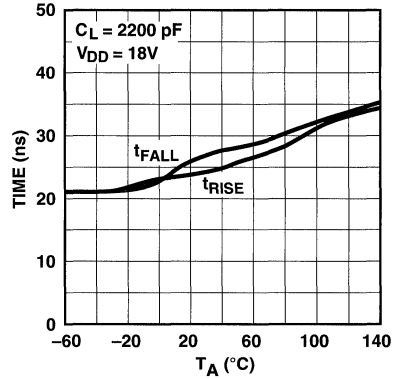
Rise Time vs Supply Voltage



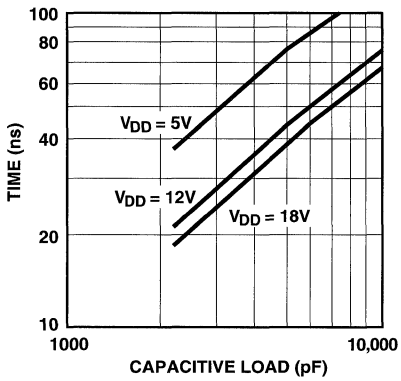
Fall Time vs Supply Voltage



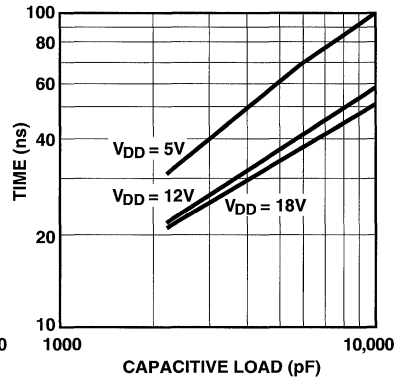
Rise and Fall Times vs Temperature



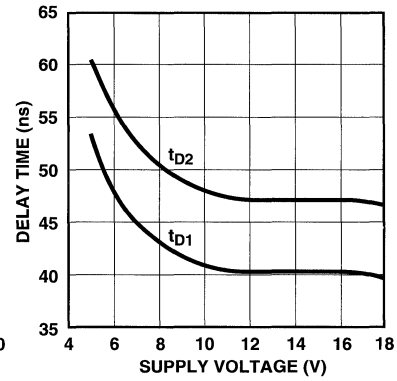
Rise Time vs Capacitive Load



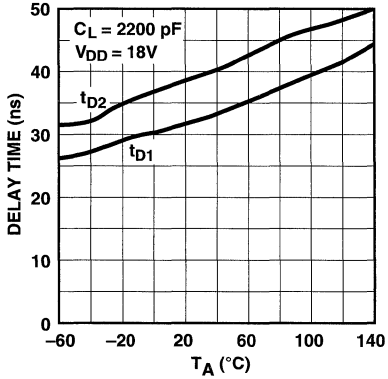
Fall Time vs Capacitive Load



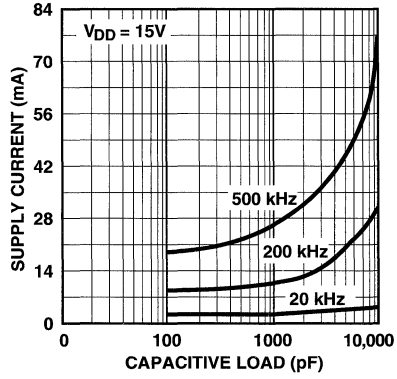
Propagation Delay Time vs Supply Voltage



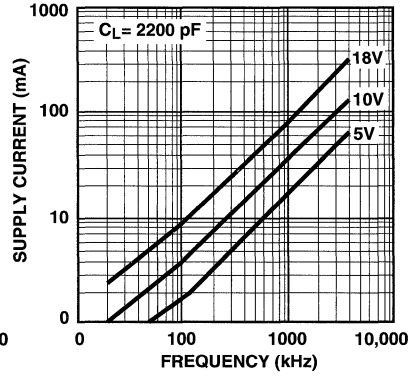
Propagation Delay Time vs Temperature



Supply Current vs Capacitive Load

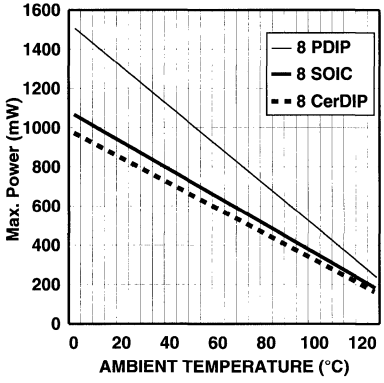


Supply Current vs Frequency

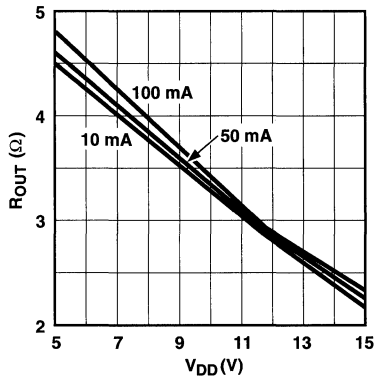


TYPICAL CHARACTERISTICS CURVES (Cont.)

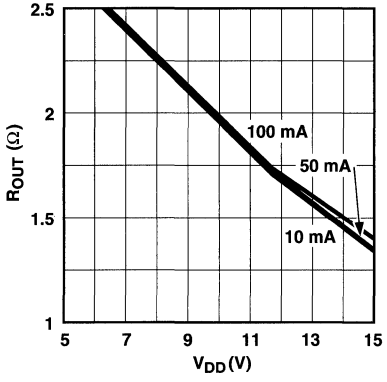
Thermal Derating Curve



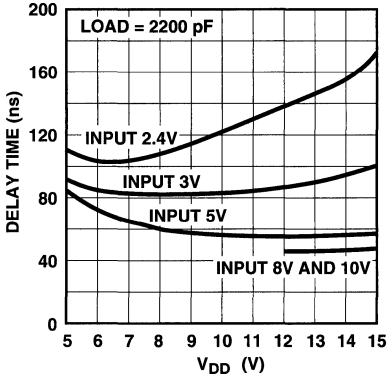
High-State Output Resistance



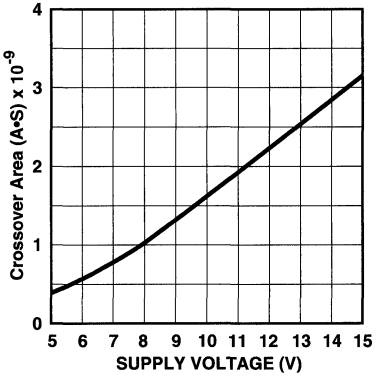
Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay



Total nA•S Crossover*



* The values on this graph represent the loss seen by the driver during one complete cycle. For a single transition, divide the value by 2.

9A HIGH-SPEED MOSFET DRIVERS

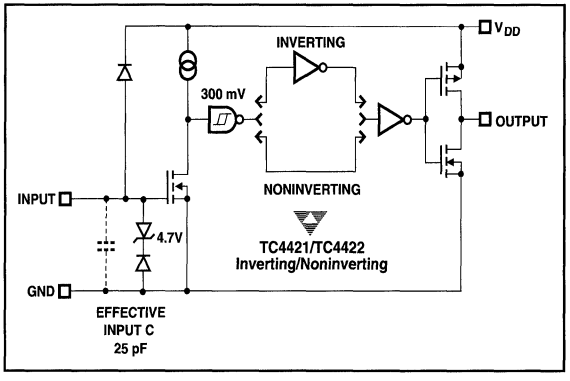
FEATURES

- Tough CMOS™ Construction
- High Peak Output Current 9A
- High Continuous Output Current ..... 2A Max
- Fast Rise and Fall Times:
  - — 30 ns with 4,700 pF Load
  - — 180 ns with 47,000 pF Load
- Short Internal Delays ..... 30 ns Typ
- Low Output Impedance ..... 1.4Ω Typ

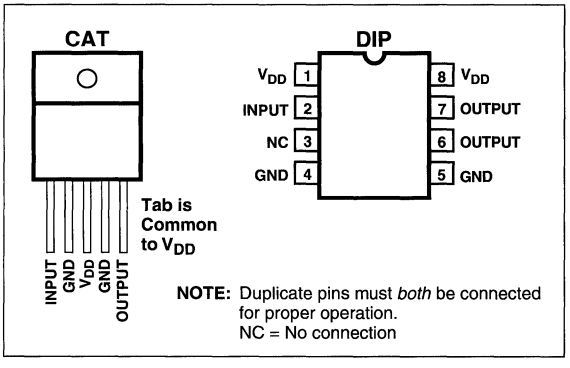
APPLICATIONS

- Line Drivers for Extra-Heavily-Loaded Lines
- Pulse Generators
- Driving the Largest MOSFETs and IGBTs
- Local Power ON/OFF Switch
- Motor and Solenoid Driver

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC4421/4422 are large buffer/drivers built using TelCom Semiconductor' proprietary Tough CMOS process. They can drive the largest MOSFETs and IGBTs now produced (including parallel-chip modules) at speeds up to the MHz region with fast rise and fall times and short delays.

They are essentially immune to any form of upset except direct overvoltage or over-dissipation — they cannot be latched under any conditions within their power and voltage ratings; they are not subject to damage or improper operation when up to 5V of ground bounce is present on their ground terminals; they can accept, without either damage or logic upset, more than 1A inductive current of either polarity being forced back into their outputs. In addition, all terminals are fully protected against up to 4 kV of electrostatic discharge.

The TC4421/4422 inputs may be driven directly from either TTL or CMOS (3V to 18V). In addition, 300 mV of hysteresis is built into the input, providing noise immunity and allowing the device to be driven from slowly rising or falling waveforms.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4421CPA	8-Pin PDIP	0°C to +70°C
TC4421EPA	8-Pin PDIP	– 40°C to +85°C
TC4421MJA	8-Pin CerDIP	– 55°C to +125°C
TC4421CAT	5-Pin TO-220	0°C to +70°C
TC4422CPA	8-Pin PDIP	0°C to +70°
TC4422EPA	8-Pin PDIP	– 40°C to +85°C
TC4422MJA	8-Pin CerDIP	– 55°C to +125°C
TC4422CAT	5-Pin TO-220	0°C to +70°C

TC4421
TC4422

ABSOLUTE MAXIMUM RATINGS

Power Dissipation, $T_A \leq 25°C$
- PDIP 1W
- CerDIP ..... 800 mW
- 5-Pin TO-220 ..... 1.5W

Power Dissipation, $T_C \leq 25°C$
- 5-Pin TO-220 ..... 12.5W

Derating Factors (To Ambient)
- PDIP ..... 8 mW/°C
- CerDIP ..... 6.4 mW/°C
- 5-Pin TO-220 ..... 12 mW/°C

Thermal Impedance (To Case)
- 5-Pin TO-220 $R_{\Theta J-A}$ ..... 10°C/W

Storage Temperature ..... – 65°C to +150°C

Operating Temperature (Chip) ..... 150°C

Operating Temperature (Ambient)
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Lead Temperature (10 sec) ..... 300°C

Supply Voltage 20V

Input Voltage ..... (V_{DD} + 0.3V) to (GND - 5V)

Input Current ($V_{IN} > V_{DD}$) ..... 50 mA

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C with 4.5V ≤ V_{DD} ≤ 18V unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Input Voltage		—	1.3	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	V_{DD} = 18V, I_O = 10 mA	—	1.4	—	Ω
R_O	Output Resistance, Low	V_{DD} = 18V, I_O = 10 mA	—	0.9	1.7	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V	—	9	—	A
I_{DC}	Continuous Output Current (TC4421/22 CAT only)	10V ≤ V_{DD} ≤ 18V, T_C = 25°	2			A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000 pF	—	60	75	ns
t_F	Fall Time	Figure 1, C_L = 10,000 pF	—	60	75	ns
t_{D1}	Delay Time	Figure 1	—	30	60	ns
t_{D2}	Delay Time	Figure 1	—	33	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	0.2	1.5	mA
		V_{IN} = 0V	—	55	150	µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

ELECTRICAL CHARACTERISTICS

(Measured over operating temperature range with $4.5V \le V_S \le 18V$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	V_{DD} = 18V, I_O = 10 mA	—	2.4	3.6	Ω
R_O	Output Resistance, Low	V_{DD} = 18V, I_O = 10 mA	—	1.8	2.7	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000 pF	—	60	120	ns
t_F	Fall Time	Figure 1, C_L = 10,000 pF	—	60	120	ns
t_{D1}	Delay Time	Figure 1	—	50	80	ns
t_{D2}	Delay Time	Figure 1	—	65	80	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	0.45	3	mA
		V_{IN} = 0V	—	0.06	0.2	mA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

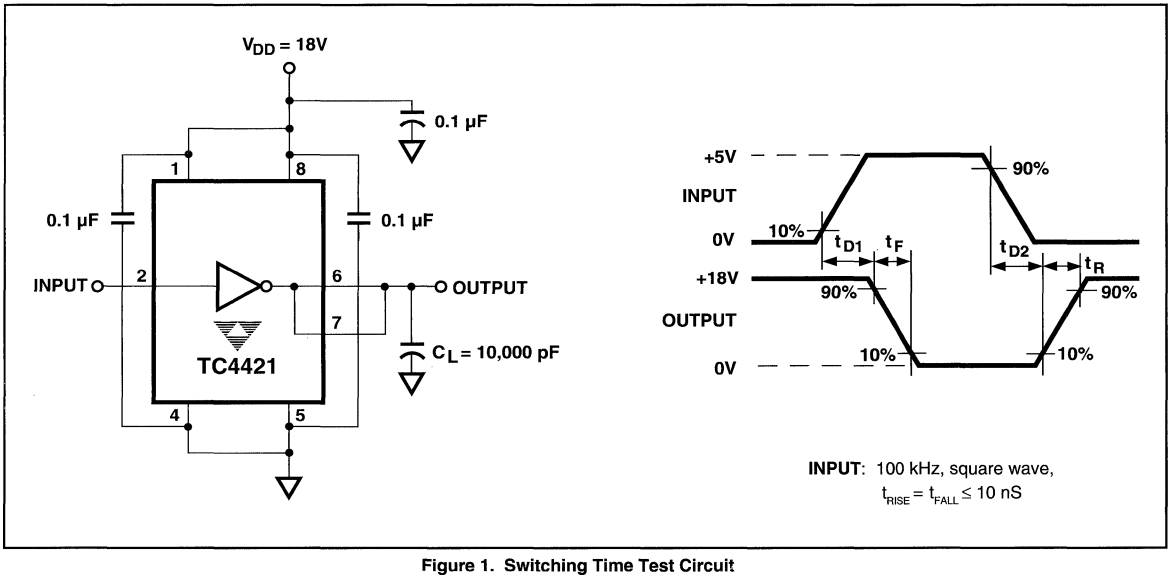
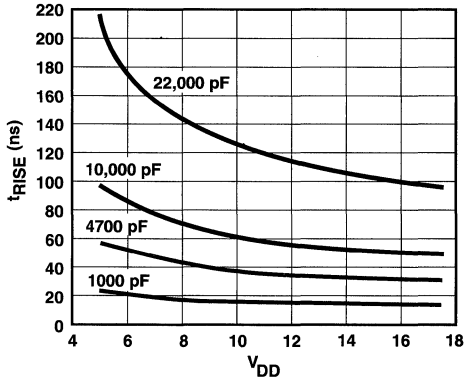


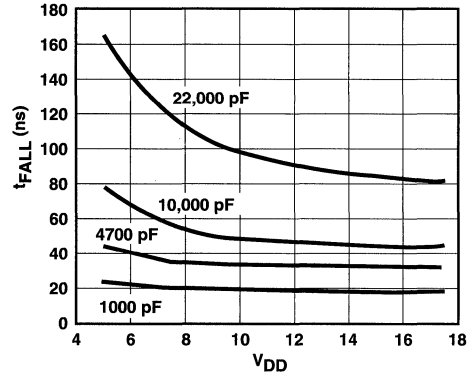
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTIC CURVES

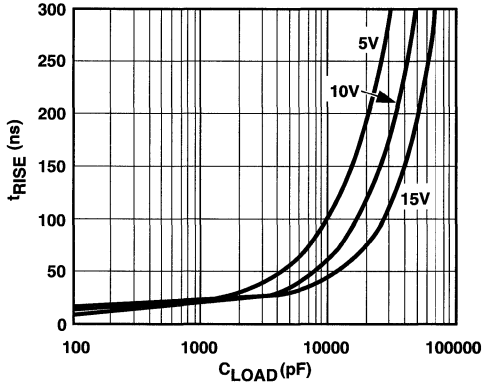
Rise Time vs Supply Voltage



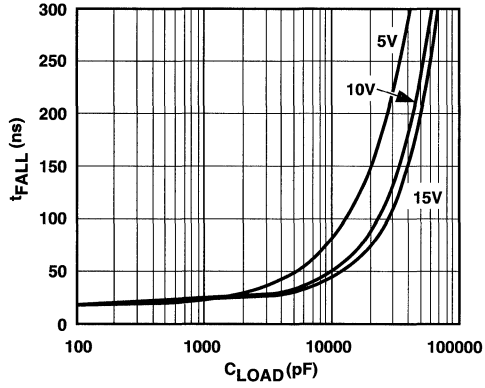
Fall Time vs Supply Voltage



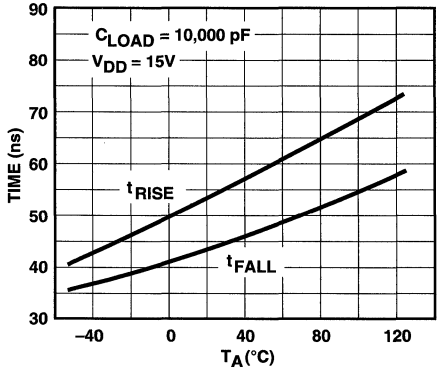
Rise TIme vs Capacitive Load



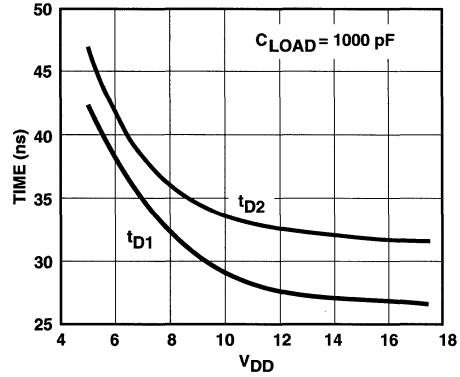
Fall TIme vs Capacitive Load



Rise and Fall Times vs Temperature

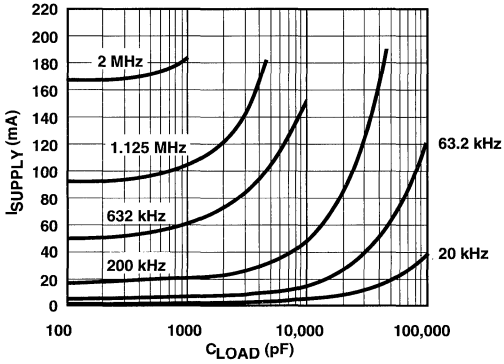


Propagation Delay vs Supply Voltage

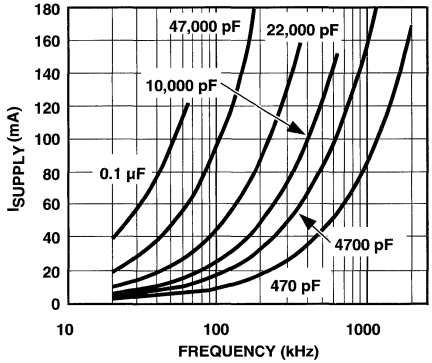


TYPICAL CHARACTERISTIC CURVES (Cont.)

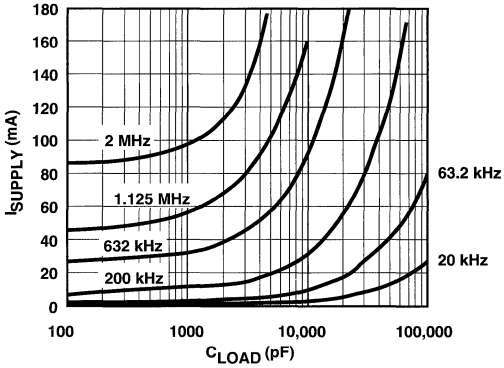
Supply Current vs Capacitive Load
(V_{DD} = 18V)



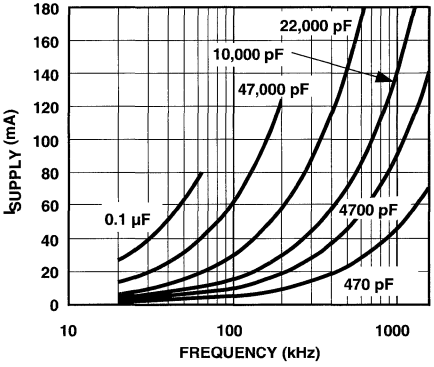
Supply Current vs Frequency
(V_{DD} = 18V)



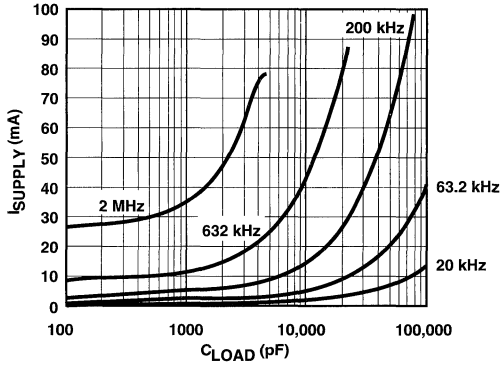
Supply Current vs Capacitive Load,
(V_{DD} = 12)



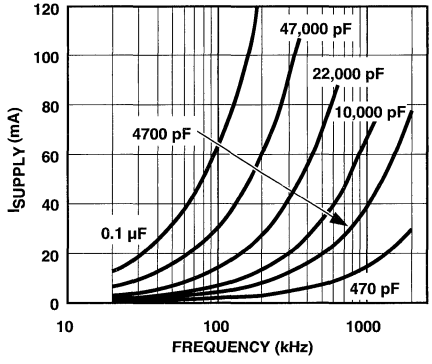
Supply Current vs Frequency
(V_{DD} = 12)



Supply Current vs Capacitive Load
(V_{DD} = 6V)

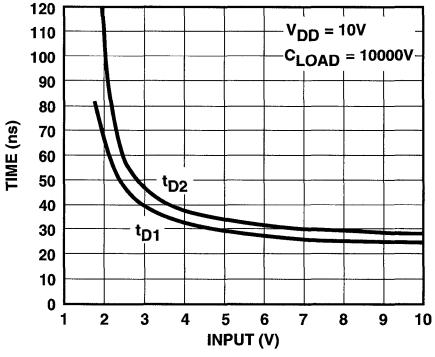


Supply Current vs Frequency
(V_{DD} = 6V)

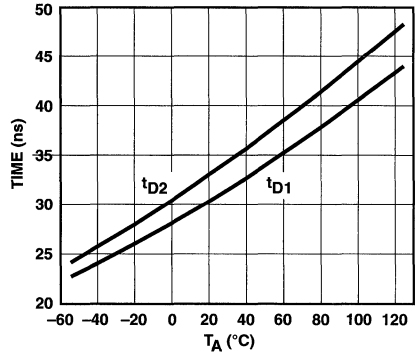


TYPICAL CHARACTERISTIC CURVES (Cont.)

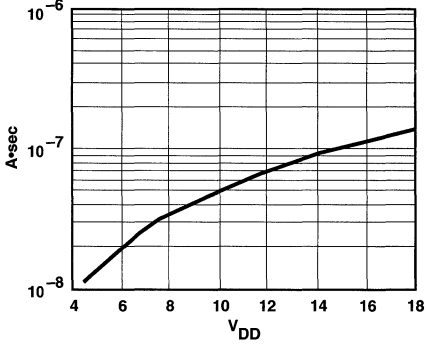
Propagation Delay vs Input Amplitude



Propagation Delay vs Temperature

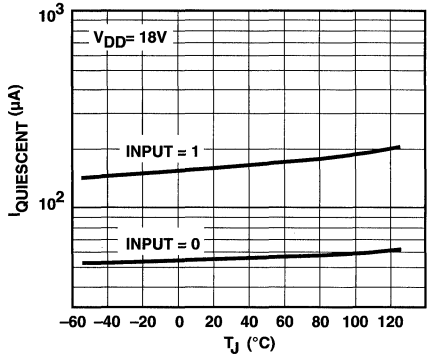


Crossover Energy vs Supply Voltage

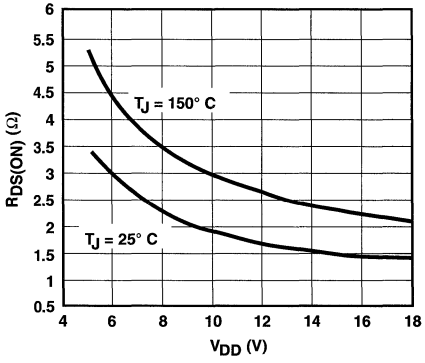


NOTE: The values on this graph represent the loss seen by the driver during a complete cycle. For the loss in a single transition, divide the stated value by 2.

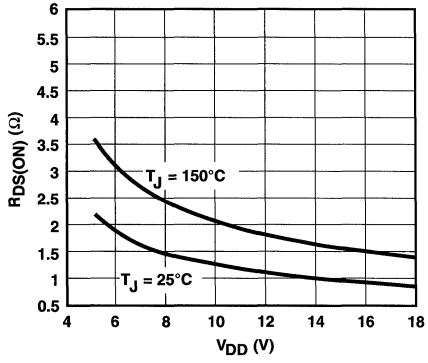
Quiescent Supply Current vs Temperature



High-State Output Resistance vs Supply Voltage



Low-State Output Resistance vs Supply Voltage



3A DUAL HIGH-SPEED MOSFET DRIVERS

FEATURES

- **High Peak Output Current 3A**
- **Wide Operating Range ..... 4.5V to 18V**
- **High Capacitive Load Drive Capability ..... 1800 pF in 25 ns**
- **Short Delay Times ..... <40 ns Typ**
- **Matched Rise/Fall Times**
- **Low Supply Current**
  - **— With Logic "1" Input ..... 3.5 mA**
  - **— With Logic "0" Input ..... 350 μA**
- **Low Output Impedance ..... 3.5Ω Typ**
- **Latch-Up Protected: Will Withstand 1.5A Reverse Current**
- **Logic Input Will Withstand Negative Swing Up to 5V**
- **ESD Protected ..... 4 kV**
- **Pinouts Same as TC1426/27/28; TC4426/27/28**

GENERAL DESCRIPTION

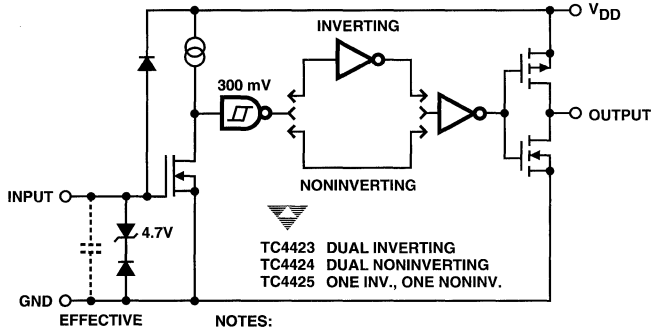
The TC4423/4424/4425 are CMOS buffer/drivers built using TelCom Semiconductors' new Tough CMOS process. They are higher output current versions of the new TC4426/4427/4428 buffer/drivers, which, in turn, are improved versions of the earlier TC426/427/428 series. All three families are pin-compatible. The TC4423/4424/4425 drivers are capable of giving reliable service in far more demanding electrical environments than their antecedents.

Although primarily intended for driving power MOSFETs, the TC4423/4424/4425 drivers are equally well-suited to driving any other load (capacitive, resistive, or inductive) which requires a low impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers can all be driven from the TC4423/4424/4425. The only known limitation on loading is the total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4423COE	16-Pin SO Wide	0°C to +70°C
TC4423CPA	8-Pin Plastic DIP	0°C to +70°C
TC4423MJA	8-Pin CerDIP	– 55°C to +125°C
TC4423EOE	16-Pin SO Wide	– 40°C to +85°C
TC4423EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4424COE	16-Pin SO Wide	0°C to +70°C
TC4424CPA	8-Pin Plastic DIP	0°C to +70°C
TC4424MJA	8-Pin CerDIP	– 55°C to +125°C
TC4424EOE	16-Pin SO Wide	– 40°C to +85°C
TC4424EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4425COE	16-Pin SO Wide	0°C to +70°C
TC4425CPA	8-Pin Plastic DIP	0°C to +70°C
TC4425MJA	8-Pin CerDIP	– 55°C to +125°C
TC4425EOE	16-Pin SO Wide	– 40°C to +85°C
TC4425EPA	8-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. TC4425 has one inverting and one noninverting driver.
2. Ground any unused driver input.

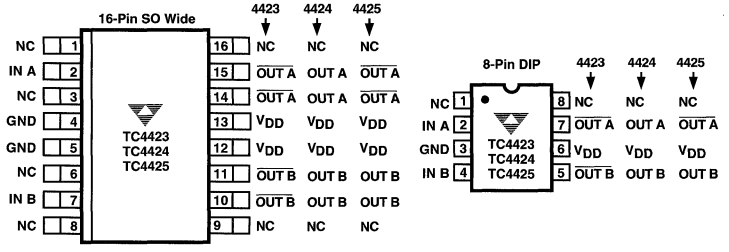
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Input Voltage, IN A or IN B ..... V_{DD} + 0.3V to GND – 5.0V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 75°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- I Version ..... - 25°C to +85°C
- E Version ..... - 40°C to +85°C
- M Version ..... - 55°C to +125°C

Power Dissipation
- Plastic DIP ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 800 mW

PIN CONFIGURATIONS



NC = NO CONNECTION
NOTE: Duplicate pins must **both** be connected for proper operation.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{OH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.8	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current		—	3	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	33	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	1.5 0.15	2.5 0.25	mA mA

ELECTRICAL CHARACTERISTICS:

Over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.7	8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	4.3	8	Ω
I_{PK}	Peak Output Current		—	3	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	28	60	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	32	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	32	100	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	2 0.2	3.5 0.3	mA mA

NOTE: 1. Switching times guaranteed by design.

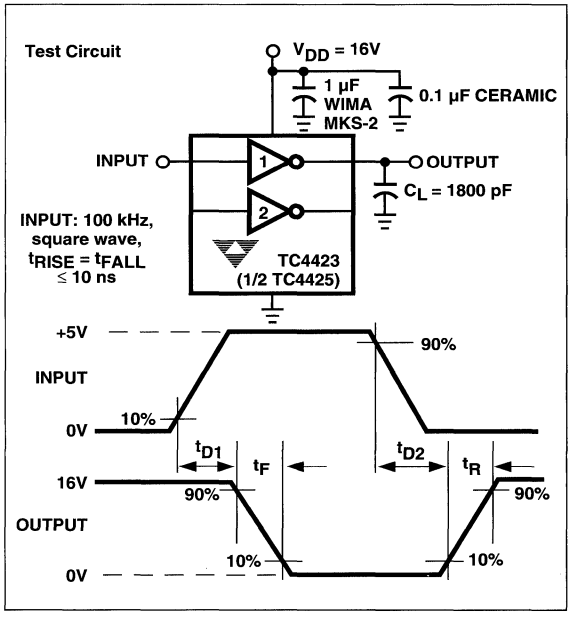


Figure 1 Inverting Driver Switching Time

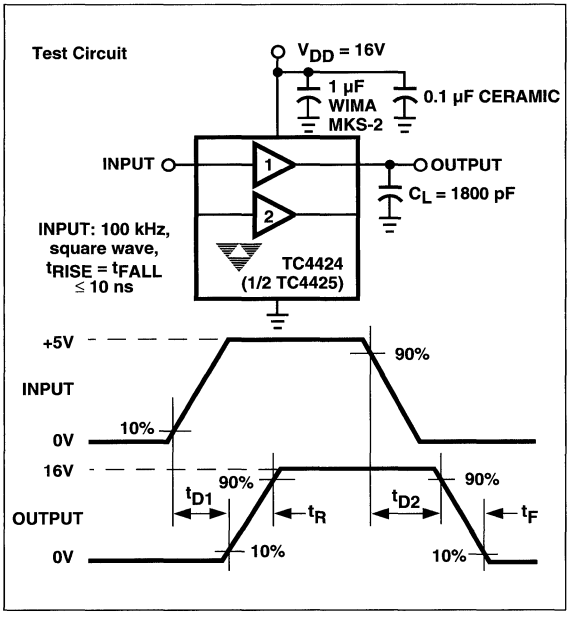
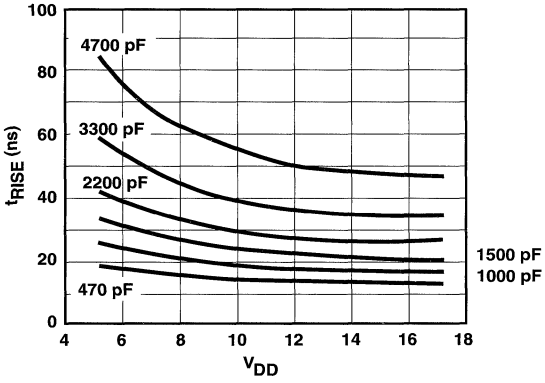


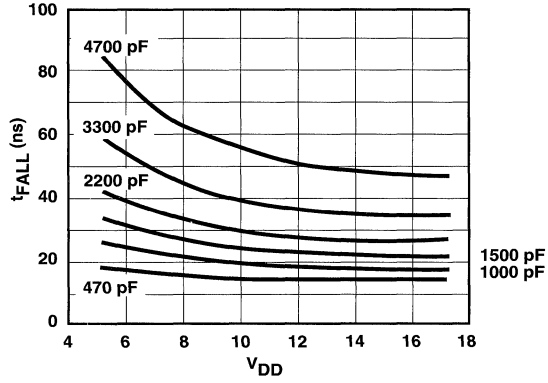
Figure 2 Noninverting Driver Switching Time

TYPICAL CHARACTERISTICS CURVES

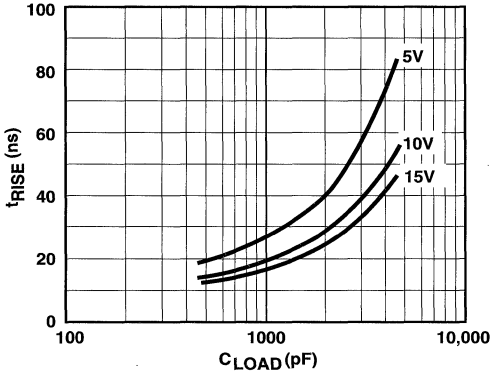
Rise Time vs Supply Voltage



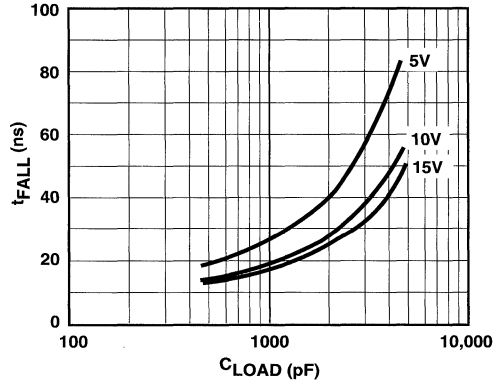
Fall Time vs Supply Voltage



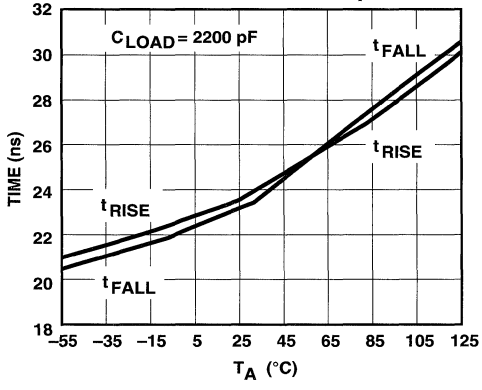
Rise TIme vs Capacitive Load



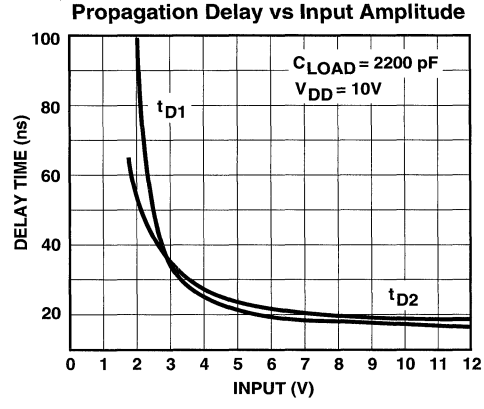
Fall TIme vs Capacitive Load



Rise and Fall Times vs Temperature

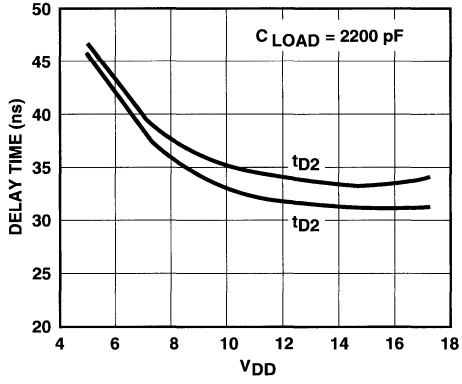


Propagation Delay vs Input Amplitude

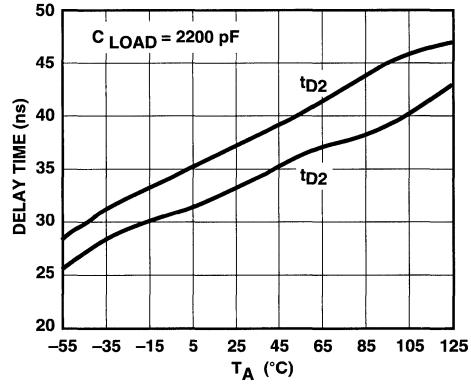


TYPICAL CHARACTERISTICS CURVES (Cont.)

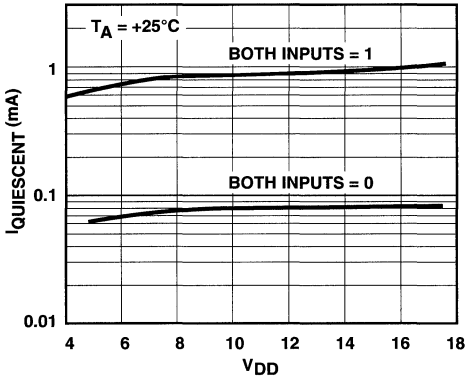
Propagation Delay Time vs Supply Voltage



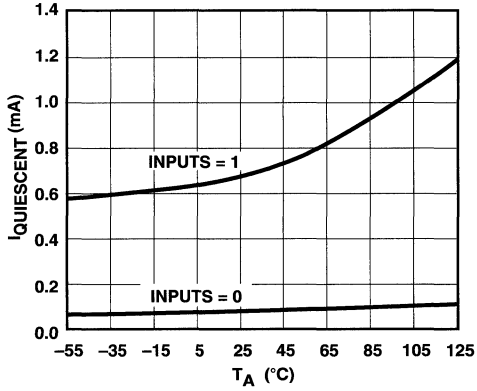
Delay Time vs Temperature



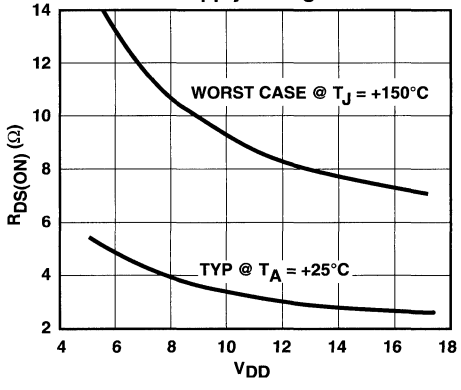
Quiescent Current vs Supply Voltage



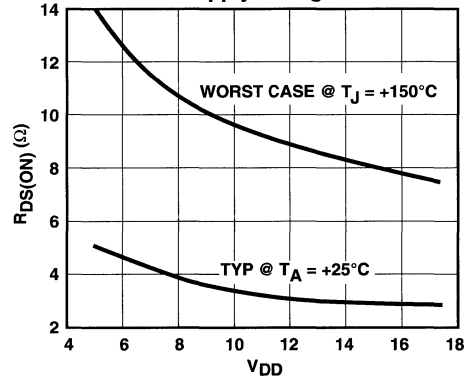
Quiescent Current vs Temperature



Output Resistance (Output High) vs Supply Voltage

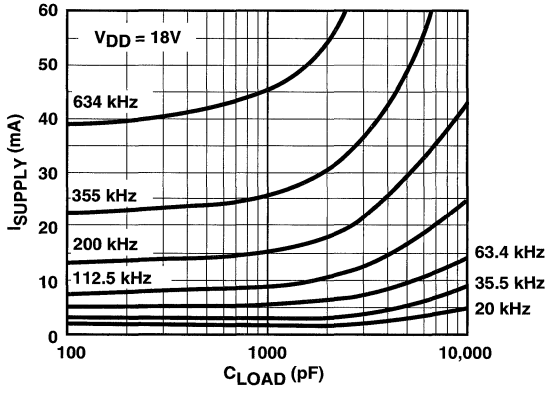


Output Resistance (Output Low) vs Supply Voltage

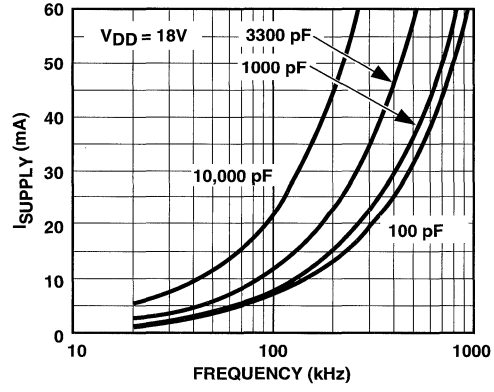


SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

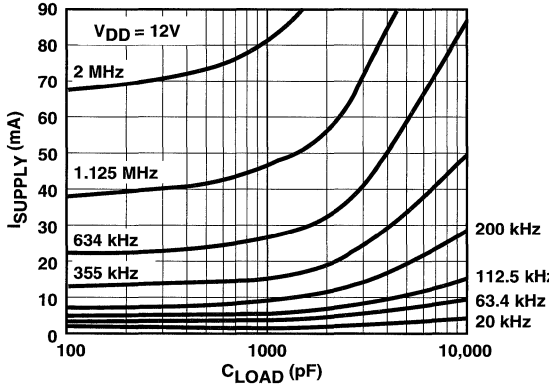
Supply Current vs Capacitive Load



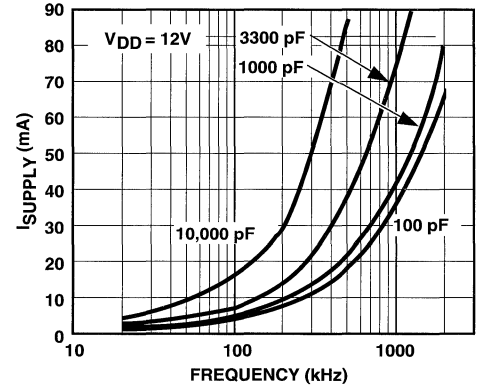
Supply Current vs Frequency



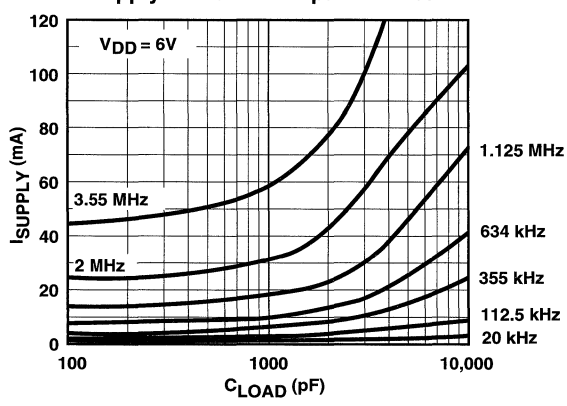
Supply Current vs Capacitive Load



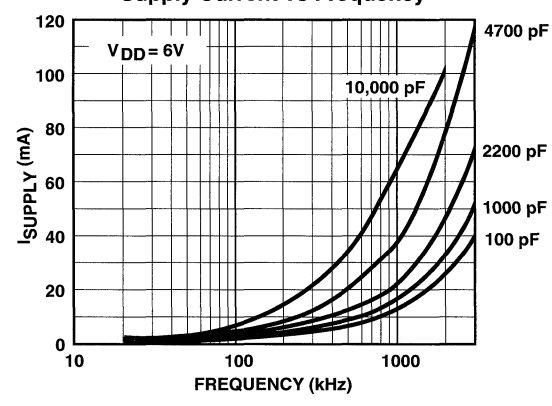
Supply Current vs Frequency



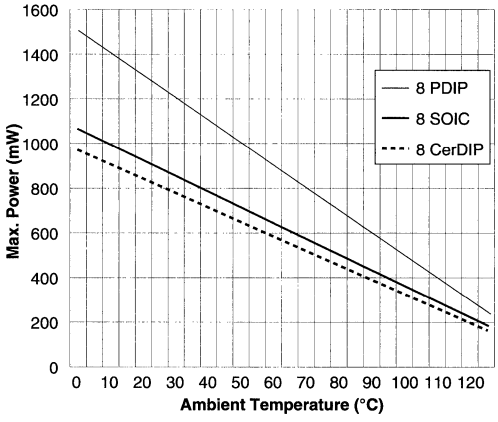
Supply Current vs Capacitive Load

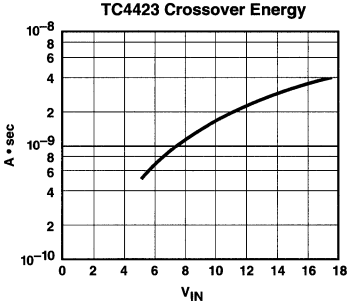


Supply Current vs Frequency



Thermal Derating Curve





NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

3

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings (See page 2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

1.5A DUAL HIGH-SPEED MOSFET DRIVERS

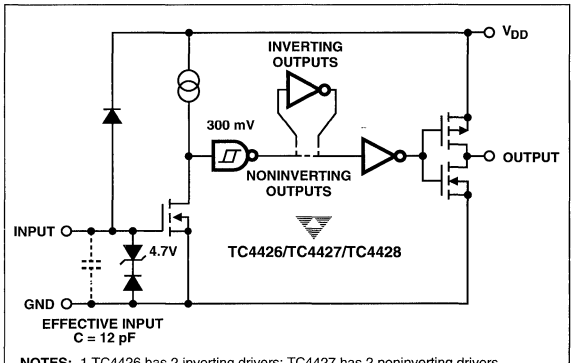
FEATURES

- **High Peak Output Current 1.5A**
- **Wide Operating Range ..... 4.5V to 18V**
- **High Capacitive Load Drive Capability ..... 1000 pF in 25 ns**
- **Short Delay Time ..... <40 ns Typ**
- **Consistent Delay Times With Changes in Supply Voltage**
- **Low Supply Current**
  - **— With Logic "1" Input ..... 4 mA**
  - **— With Logic "0" Input ..... 400 µA**
- **Low Output Impedance 7Ω**
- **Latch-Up Protected: Will Withstand >0.5A Reverse Current ..... Down to –5V**
- **Input Will Withstand Negative Inputs**
- **ESD Protected ..... 4 kV**
- **Pinout Same as TC426/TC427/TC428**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4426COA	8-Pin SOIC	0°C to +70°C
TC4426EOA	8-Pin SOIC	– 40°C to +85°C
TC4426CPA	8-Pin Plastic DIP	0°C to +70°C
TC4426EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4426MJA	8-Pin CerDIP	– 55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1.TC4426 has 2 inverting drivers; TC4427 has 2 noninverting drivers.
2. TC4428 has one inverting and one noninverting driver.
3. Ground any unused driver input.

GENERAL DESCRIPTION

The TC4426/4427/4428 are CMOS buffer/drivers built using TelCom Semiconductors' new Tough CMOS process. They are improved versions of the earlier TC426/427/428 family of buffer/drivers (with which they are pin compatible). They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC4426/4427/4428 can easily switch 1000 pF gate capacitances in under 30 ns, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

Other compatible drivers are the TC4426A/27A/28A. These drivers have matched input to output leading edge and falling edge delays, tD1 and tD2, for processing short duration pulses in the 25 nanoseconds range. They are pin compatible with the TC4426/27/28.

Part No.	Package	Temperature Range
TC4427COA	8-Pin SOIC	0°C to +70°C
TC4427EOA	8-Pin SOIC	– 40°C to +85°C
TC4427CPA	8-Pin Plastic DIP	0°C to +70°C
TC4427EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4427MJA	8-Pin CerDIP	– 55°C to +125°C
TC4428COA	8-Pin SOIC	0°C to +70°C
TC4428EOA	8-Pin SOIC	– 40°C to +85°C
TC4428CPA	8-Pin Plastic DIP	0°C to +70°C
TC4428EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4428MJA	8-Pin CerDIP	– 55°C to +125°C

TC4426
TC4427
TC4428

ABSOLUTE MAXIMUM RATINGS

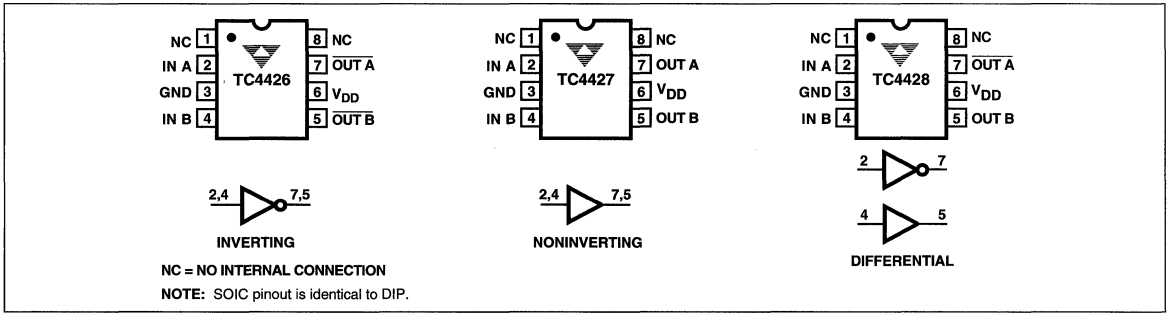
Supply Voltage ..... +22V
Input Voltage, IN A or IN B .... VDD + 0.3V to GND – 5.0V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... - 40°C to +85°C
- M Version ..... - 55°C to +125°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 800 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	7	10	Ω
I_{PK}	Peak Output Current	Duty Cycle ≤ 2%, t ≤ 300 µs	—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	> 0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	19	30	ns
t_F	Fall Time	Figure 1	—	19	30	ns
t_{D1}	Delay Time	Figure 1	—	20	30	ns
t_{D2}	Delay Time	Figure 1	—	40	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	4.5	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

NOTE: 1. Switching times are guaranteed by design.

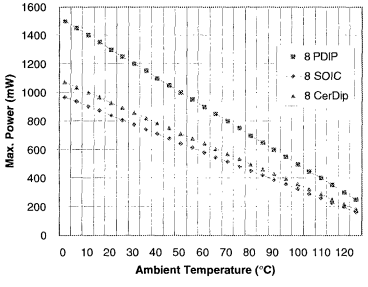
ELECTRICAL CHARACTERISTICS

Specifications measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

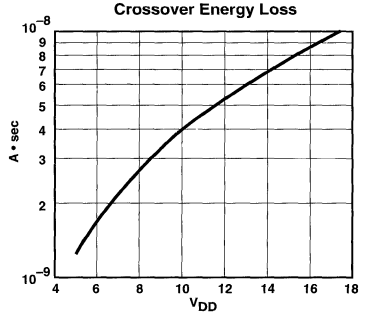
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{DD}$	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	9	12	Ω
I_{PK}	Peak Output Current	Duty Cycle ≤ 2%, t ≤ 300 µs	—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle≤ 2% t ≤ 300 µs	> 0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	—	40	ns
t_F	Fall Time	Figure 1	—	—	40	ns
t_{D1}	Delay Time	Figure 1	—	—	40	ns
t_{D2}	Delay Time	Figure 1	—	—	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	mA

NOTE: 1. Switching times are guaranteed by design.

Thermal Derating Curve



Crossover Energy Loss



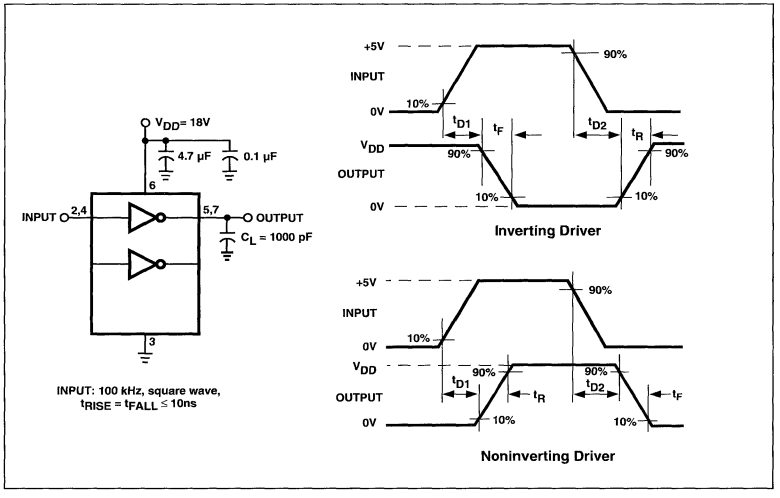
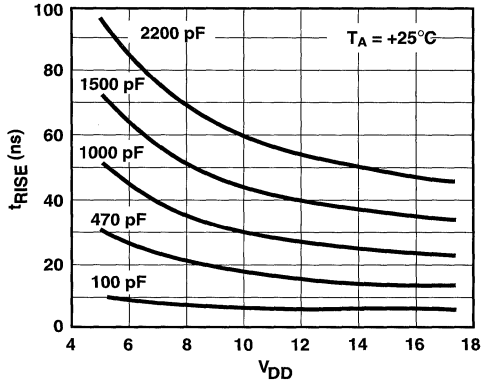


Figure 1. Switching Time Test Circuit

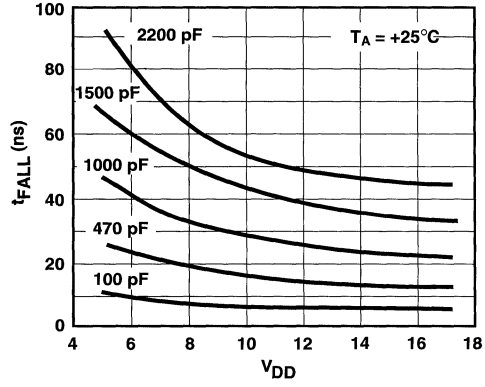
NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

TYPICAL CHARACTERISTICS CURVES

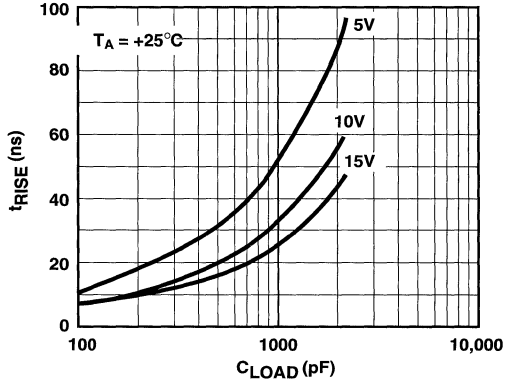
Rise Time vs Supply Voltage



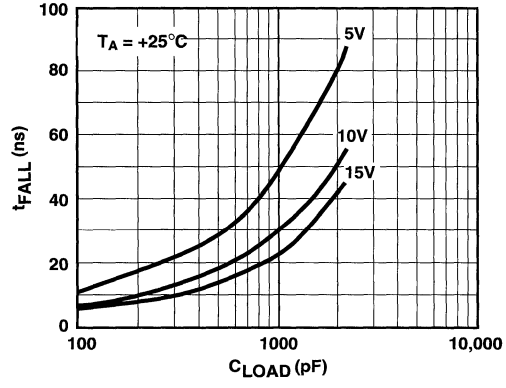
Fall Time vs Supply Voltage



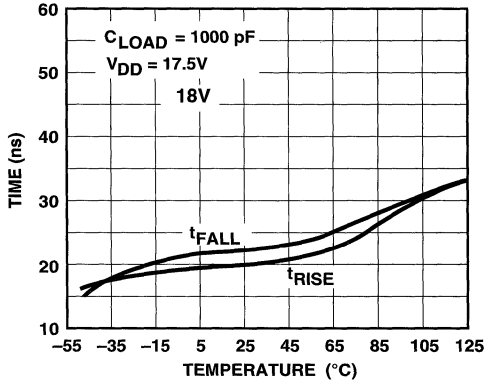
Rise TIme vs Capacitive Load



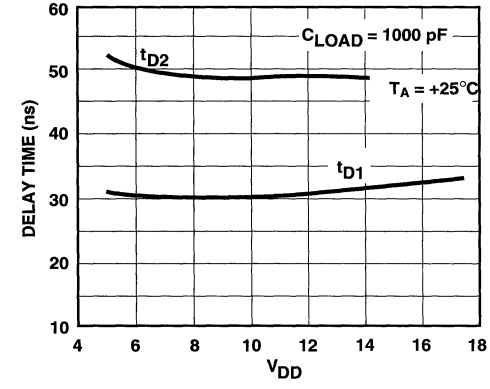
Fall TIme vs Capacitive Load



Rise and Fall Times vs Temperature

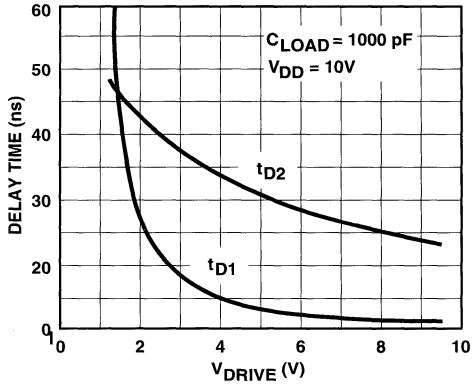


Propagation Delay vs Supply Voltage

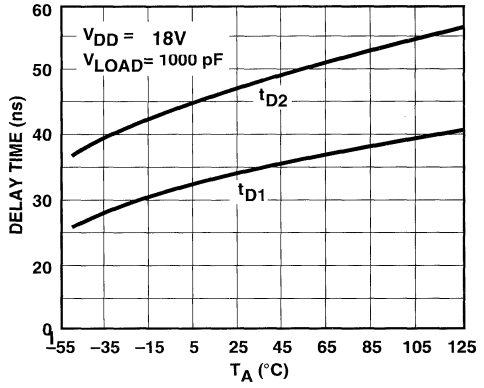


TYPICAL CHARACTERISTICS CURVES (Cont.)

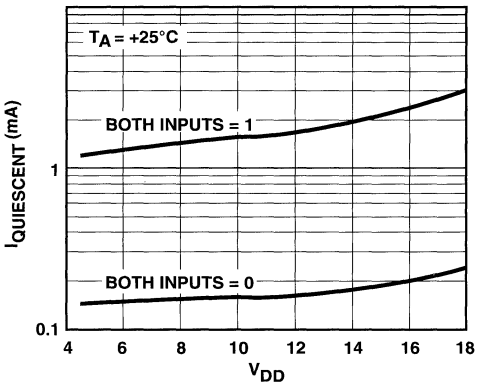
Effect of Input Amplitude on Delay Time



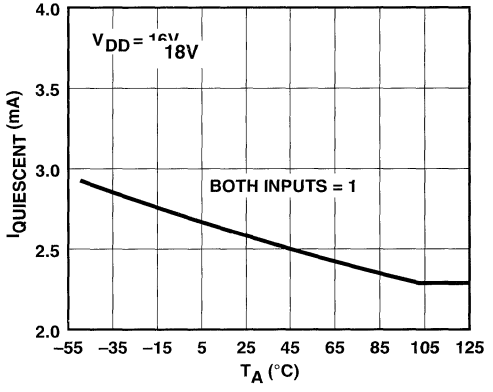
Propagation Delay Time vs Temperature



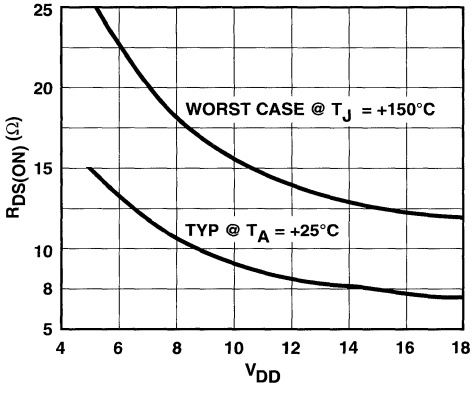
Quiescent Supply Current vs Voltage



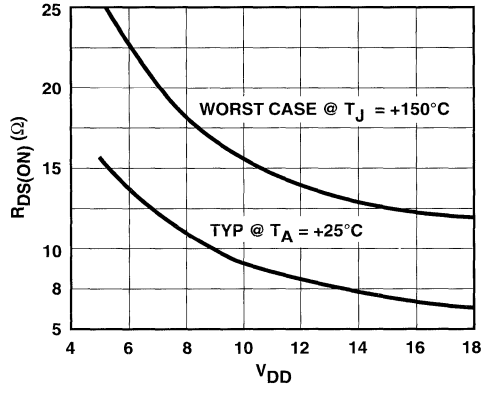
Quiescent Supply Current vs Temperature



High-State Output Resistance

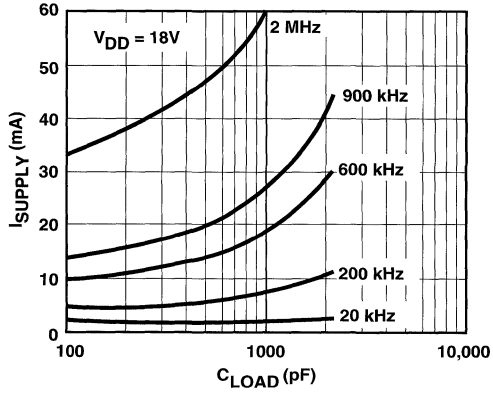


Low-State Output Resistance

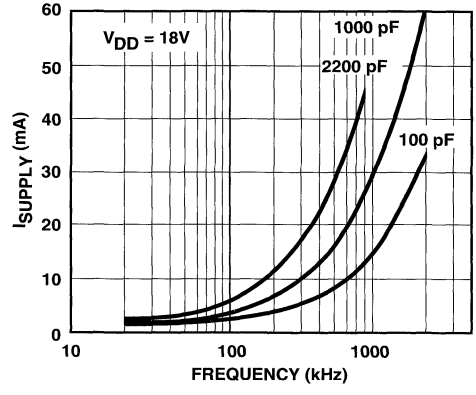


SUPPLY CURRENT CHARACTERISTICS CURVES (Load on Single Output Only)

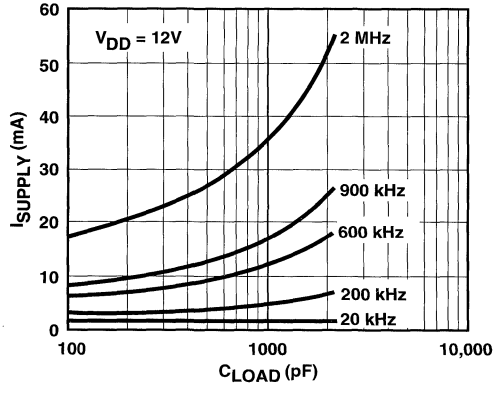
Supply Current vs Capacitive Load



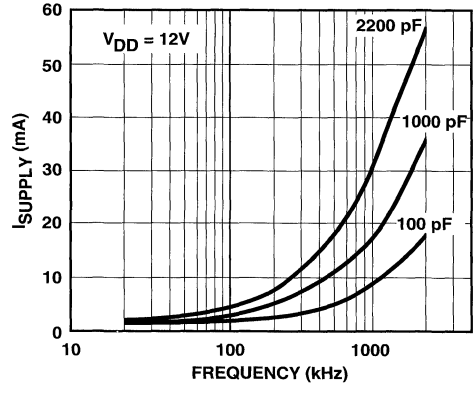
Supply Current vs Frequency



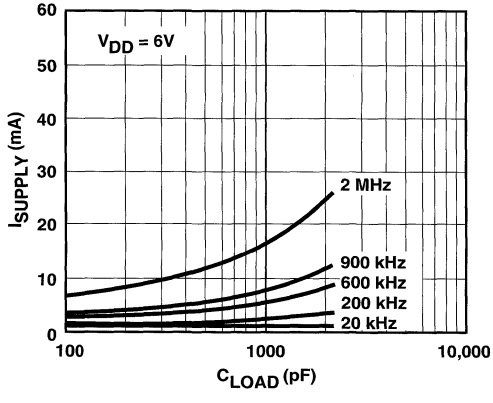
Supply Current vs Capacitive Load



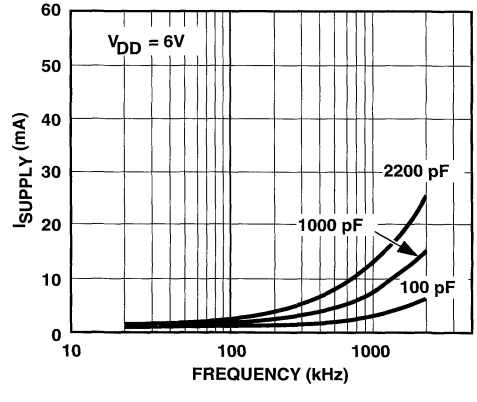
Supply Current vs Frequency



Supply Current vs Capacitive Load



Supply Current vs Frequency



1.5A DUAL HIGH-SPEED MOSFET DRIVERS

FEATURES

- **High Peak Output Current 1.5A**
- **Wide Operating Range ..... 4.5V to 18V**
- **High Capacitive Load Drive Capability ..... 1000 pF in 25 ns Typ**
- **Short Delay Time ..... 30 ns Typ**
- **Matched Rise, Fall and Delay Times**
- **Low Supply Current**
  - **— With Logic "1" Input ..... 1 mA Typ**
  - **— With Logic "0" Input ..... 100 μA Typ**
- **Low Output Impedance ..... 7Ω Typ**
- **Latch-Up Protected: Will Withstand 0.5A Reverse Current**
- **Input Will Withstand Negative Inputs Up to 5V**
- **ESD Protected ..... 4 kV**
- **Pinout Same as TC426/TC427/TC428**

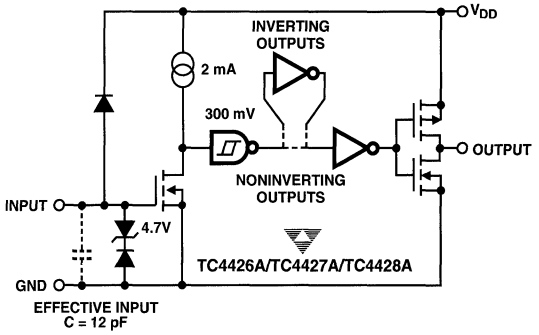
GENERAL DESCRIPTION

The TC4426A/4427A/4428A are CMOS buffer/drivers built using TelCom Semiconductors' new Tough CMOS™ process. They are improved versions of the earlier TC426/427/428 family of buffer/drivers (with which they are pin compatible). They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC4426A/4427A/4428A can easily switch 1000 pF gate capacitances in under 30 ns, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

3

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. TC4426A has 2 inverting drivers; TC4427A has 2 noninverting drivers.
2. TC4428A has one inverting and one noninverting driver.
3. Ground any unused driver input.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4426ACOA	8-Pin SOIC	0°C to +70°C
TC4426AEOA	8-Pin SOIC	– 40°C to +85°C
TC4426ACPA	8-Pin Plastic DIP	0°C to +70°C
TC4426AEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4426AMJA	8-Pin CERDIP	–55°C to +125°C
TC4427ACOA	8-Pin SOIC	0°C to +70°C
TC4427AEOA	8-Pin SOIC	– 40°C to +85°C
TC4427ACPA	8-Pin Plastic DIP	0°C to +70°C
TC4427AEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4427AMJA	8-Pin CERDIP	–55°C to +125°C
TC4428ACOA	8-Pin SOIC	0°C to +70°C
TC4428AEOA	8-Pin SOIC	– 40°C to +85°C
TC4428ACPA	8-Pin Plastic DIP	0°C to +70°C
TC4428AEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4428AMJA	8-Pin CERDIP	–55°C to +125°C

TC4426A
TC4427A
TC4428A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 800 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

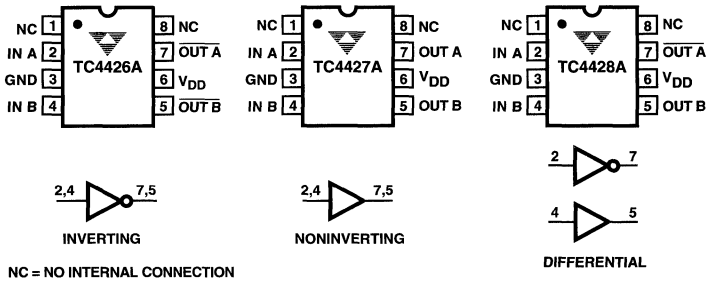
ELECTRICAL CHARACTERISTICS:

Over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Input							
V_{IH}	Logic 1 High Input Voltage			2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage			—	—	0.8	V
I_{IN}	Input Current	–5V ≤ V_{IN} ≤ V_{DD}	T_A=25°C	–1	—	1	µA
			-40°C≤T_A≤85°C	–10	—	10	µA
Output							
V_{OH}	High Output Voltage	DC Test		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	DC Test		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	T_A=25°C	—	7	9	Ω
			0°C≤T_A≤70°C	—	7	10	Ω
			-40°C≤T_A≤85°C	—	8	11	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V		—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	V_{DD} = 18V	0.5	—	—	A
Switching Time (Note 1)							
t_R	Rise Time	Figure 1	T_A=25°C	—	25	35	ns
			0°C≤T_A≤70°C	—	27	40	ns
			-40°C≤T_A≤85°C	—	29	40	ns
t_F	Fall Time	Figure 1	T_A=25°C	—	25	35	ns
			0°C≤T_A≤70°C	—	27	40	ns
			-40°C≤T_A≤85°C	—	29	40	ns
t_{D1}	Delay Time	Figure 1	T_A=25°C	—	30	35	ns
			0°C≤T_A≤70°C	—	33	40	ns
			-40°C≤T_A≤85°C	—	35	45	ns
t_{D2}	Delay Time	Figure 1	T_A=25°C	—	30	35	ns
			0°C≤T_A≤70°C	—	33	40	ns
			-40°C≤T_A≤85°C	—	35	45	ns
Power Supply							
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)		—	1.0	2.0	mA
		V_{IN} = 0V (Both Inputs)	V_{DD} = 18V	—	0.1	0.2	mA

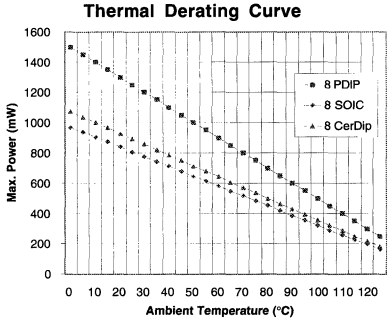
NOTE: 1. Switching times are guaranteed by design.

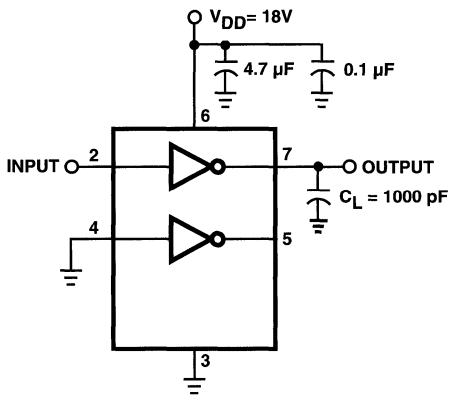
PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.





INPUT: 100 kHz, square wave,
$t_{RISE} = t_{FALL} \leq 10ns$

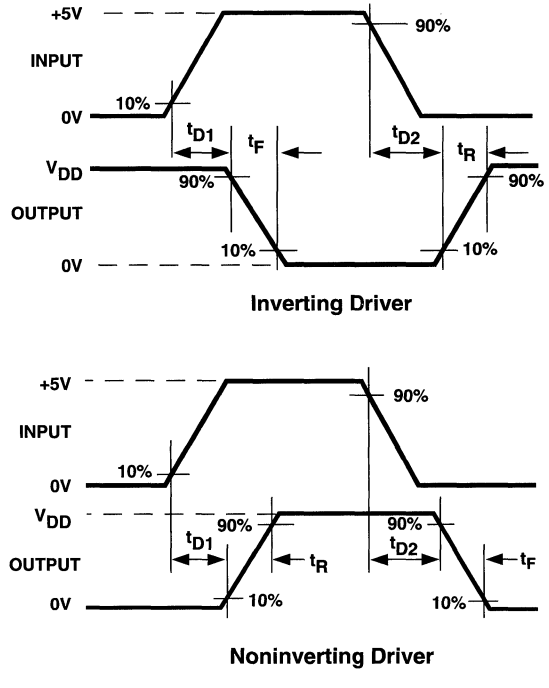
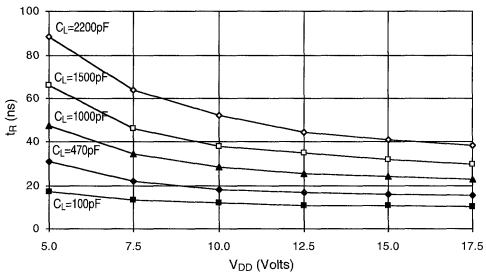


Figure 1. Switching Time Test Circuit

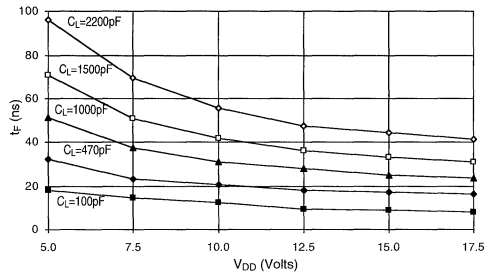
TC4426A
TC4427A
TC4428A

TYPICAL CHARACTERISTICS CURVES

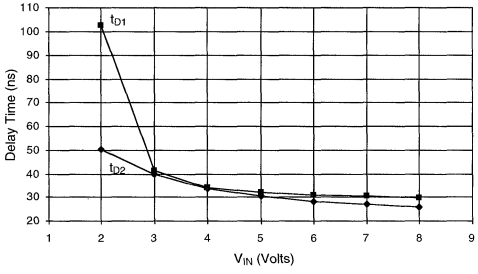
Rise Time vs. Supply Voltage



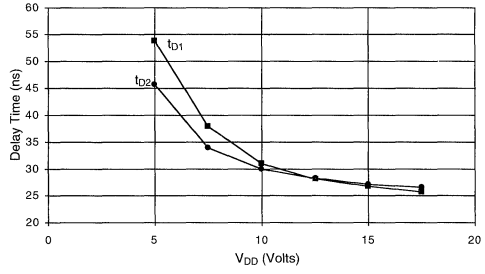
Fall Time vs. Supply Voltage



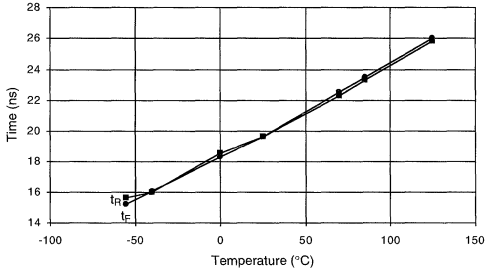
Effect of Input Amplitude on Delay



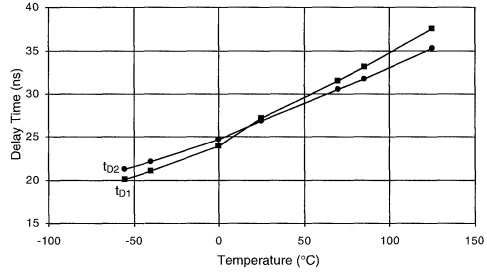
Propagation Delay Time vs. Supply Voltage



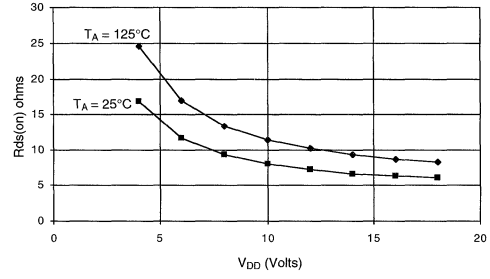
Rise and Fall Times vs. Temperature



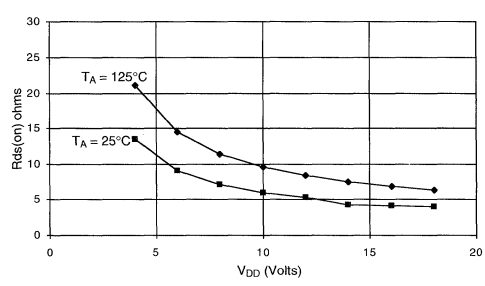
Propagation Delay Time vs. Temperature



High-State Output Resistance

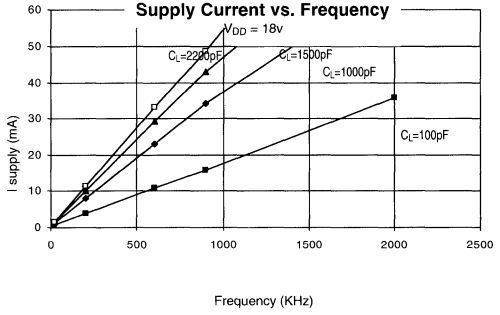


Low-State Output Resistance

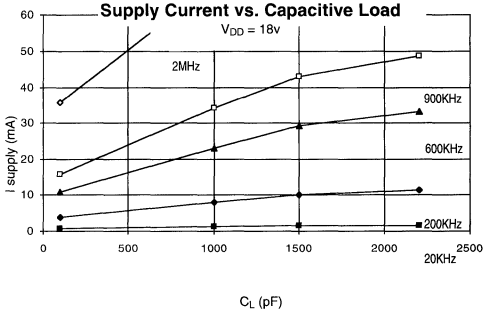


TYPICAL CHARACTERISTICS CURVES (Cont.)

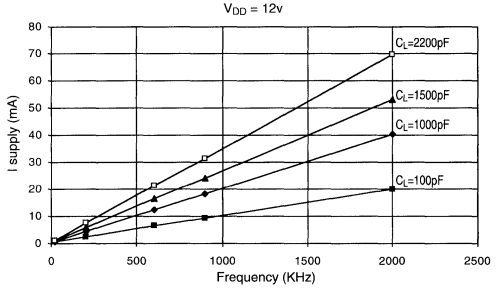
Supply Current vs. Frequency



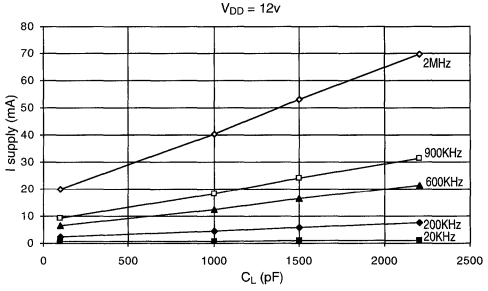
Supply Current vs. Capacitive Load



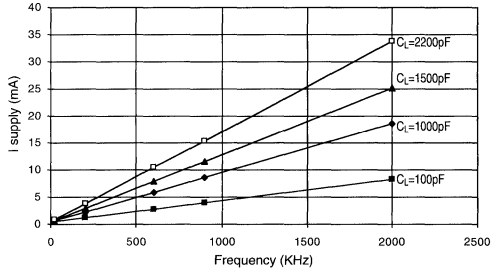
Supply Current vs. Frequency



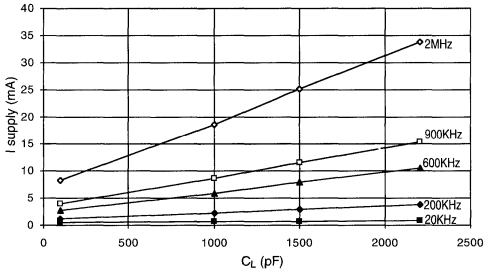
Supply Current vs. Capacitive Load



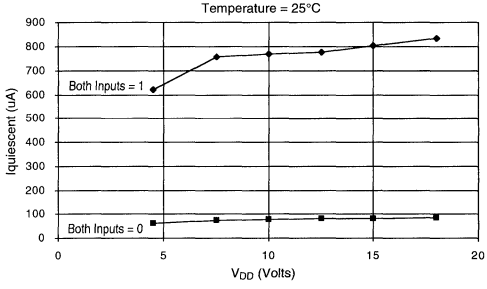
Supply Current vs. Frequency



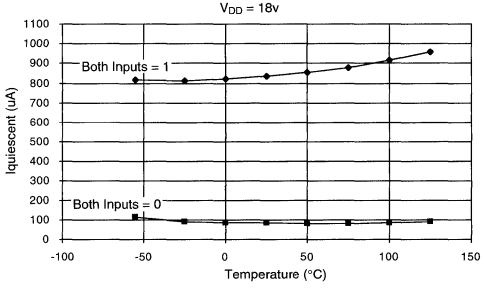
Supply Current vs. Capacitive Load



Quiescent Supply Current vs. Voltage



Quiescent Supply Current vs. Temperature



1.5A HIGH-SPEED 30V MOSFET DRIVERS

FEATURES

- **High Peak Output Current 1.5A**
- **Wide Operating Range ..... 5V to 30V**
- **High Capacitive Load Drive Capability ..... 1000 pF in 25 ns**
- **Short Delay Time ..... <78ns Typ**
- **Low Supply Current**
  - **— With Logic "1" Input 2.5mA**
  - **— With Logic "0" Input 300µA**
- **Low Output Impedance 7Ω**
- **Latch-Up Protected: Will Withstand >300mA Reverse Current**
- **ESD Protected ..... 4 kV**

GENERAL DESCRIPTION

The TC4431/4432 are CMOS buffer/drivers built using TelCom Semiconductors' new Tough CMOS™ process. They are improved versions of the earlier TC4426/4427/4428 family of buffer/drivers. They will not latch up under any conditions within their power and voltage ratings. They can accept, without damage or logic upset, up to 300mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4 kV of electrostatic discharge.

Under-voltage lockout circuitry forces the output to a "low" state when the input supply voltage drops below 7V. Maximum startup V_{DD} bias voltage threshold is 10V. For operation at lower voltages, the LOCK DIS, Pin 3 can be grounded to disable the lockout and start-up circuit. The under-voltage lockout and start-up circuit gives brown out protection when driving MOSFETS.

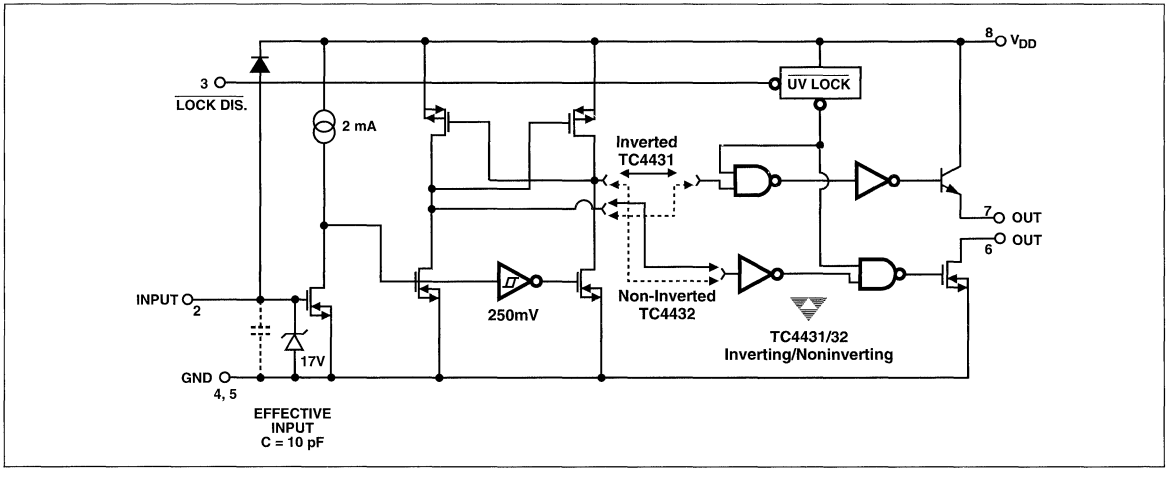
3

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4431COA	8-Pin SOIC	0°C to +70°C
TC4431EOA	8-Pin SOIC	– 40°C to +85°C
TC4431CPA	8-Pin Plastic DIP	0°C to +70°C
TC4431EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4431EJA	8-Pin CerDIP	– 40°C to +85°C

Part No.	Package	Temperature Range
TC4432COA	8-Pin SOIC	0°C to +70°C
TC4432EOA	8-Pin SOIC	– 40°C to +85°C
TC4432CPA	8-Pin Plastic DIP	0°C to +70°C
TC4432EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4432EJA	8-Pin CerDIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



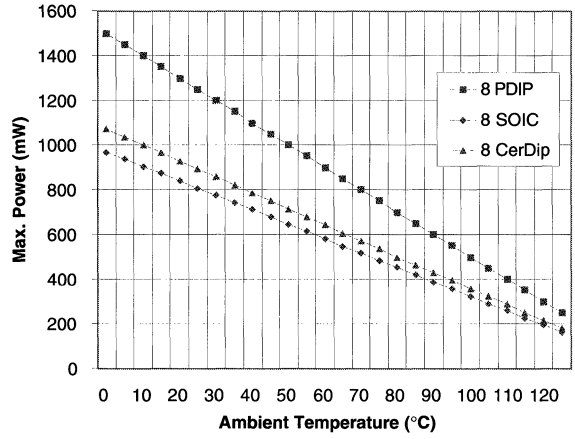
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 36V
Input Voltage (Note 1) ..... VDD + 0.3V to GND
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 250°C/W
- SOIC $R_{\theta J-C}$ ..... 75°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... - 40°C to +85°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 500 mW

Thermal Derating Curve



Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 30V, unless otherwise specified.

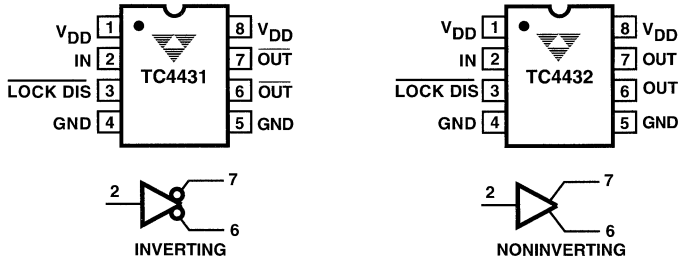
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current (Note 1)	0V ≤ V_{IN} ≤ V_{DD} (17V MAX)	–1	—	1	µA
Output						
V_{OH}	High Output Voltage	I_{OUT} = 100mA	V_{DD} – 1.0	V_{DD} – 0.8	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance (V_{OL})	V_{DD} = 30V, I_O = 10mA	—	7	10	Ω
I_{PK}	Peak Output Current	Source: V_{DD} = 30V	—	3.0	—	A
		Sink: V_{DD} = 30V	—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	0.3	—	—	A
Switching Time (Note 2)						
t_R	Rise Time	Figure 1	—	25	40	ns
t_F	Fall Time	Figure 1	—	33	50	ns
t_{D1}	Delay Time	Figure 1	—	62	80	ns
t_{D2}	Delay Time	Figure 1	—	78	90	ns

NOTES: 1. For inputs >17V, add a 1kΩ resistor in series with the input. See graph on page 6 for input current.
2. Switching times are guaranteed by design.
3. For operation below 7V, the $\overline{\text{LOCK DIS.}}$, Pin3 can be grounded to disable the lockout and start-up circuit.

ELECTRICAL CHARACTERISTICS (Cont.): T_A = +25°C with 4.5V ≤ V_{DD} ≤ 30V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	2.5	4	mA
		V_{IN} = 0V	—	0.3	0.4	mA
V_S	Start-up Threshold		—	8.7	10	V
V_{DO}	Drop-out Threshold	(Note 3)	7	7.9	—	V

PIN CONFIGURATIONS



NOTE: SOIC pinout is identical to DIP.

ELECTRICAL CHARACTERISTICS

Specifications measured over operating temperature range with 4.5V ≤ V_{DD} ≤ 30V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current (Note 1)	0V≤ V_{IN} ≤ V_{DD} (17V MAX)	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage	I_{OUT} = 100mA	V_{DD} – 1.2	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 30V, I_O = 10mA	—	—	12	Ω
Switching Time (Note 2)						
t_R	Rise Time	Figure 1	—	—	60	ns
t_F	Fall Time	Figure 1	—	—	70	ns
t_{D1}	Delay Time	Figure 1	—	—	100	ns
t_{D2}	Delay Time	Figure 1	—	—	110	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	—	6	mA
		V_{IN} = 0V	—	—	0.7	mA
V_S	Start-up Threshold		—	—	10	V
V_{DO}	Drop-out Threshold	(Note 3)	7	—	—	V

NOTES: 1. For inputs >17V, add a 1kΩ resistor in series with the input. See graph on page 6 for input current.
2. Switching times are guaranteed by design.
3. For operation below 7V, the $\overline{\text{LOCK DIS.}}$, Pin3 can be grounded to disable the lockout and start-up circuit.

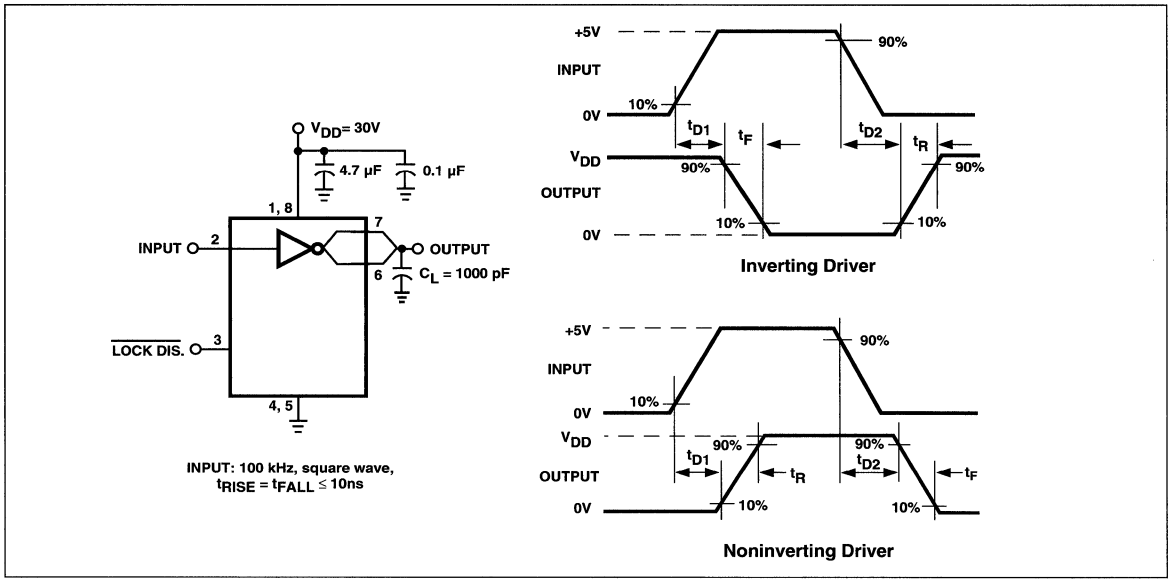
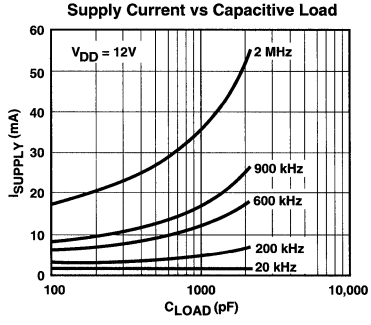
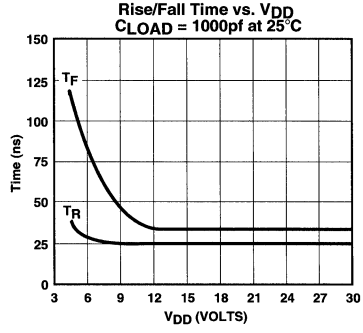
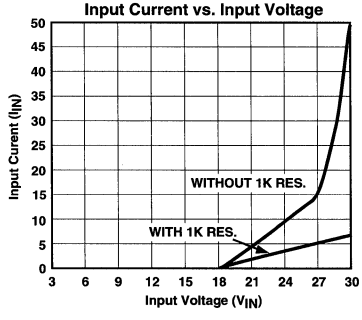


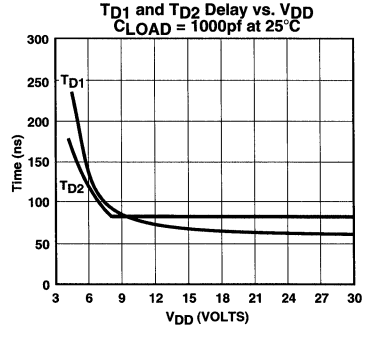
Figure 1. Switching Time Test Circuit

CHARACTERISTIC CURVES









LOGIC-INPUT CMOS QUAD DRIVERS

FEATURES

- **High Peak Output Current 1.2A**
- **Wide Operating Range ..... 4.5 to 18V**
- **Symmetrical Rise and Fall Times ..... 25 ns**
- **Short, Equal Delay Times ..... 75 ns**
- **Tough CMOS™ Construction**
- **Latchproof! Withstands 500 mA Inductive Kickback**
- **3 Input Logic Choices**
  - **— AND/NAND/AND+Inv**
- **2 kV ESD Protection on All Pins**

APPLICATIONS

- **General-Purpose CMOS Logic Buffer**
- **Driving All Four MOSFETs in an H-Bridge**
- **Direct Small Motor Driver**
- **Relay or Peripheral Drivers**
- **CCD Driver**
- **Pin-Switching Network Driver**

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC446*CPD	14-Pin Plastic DIP	0° to +70°C
TC446*COE	16-Pin Wide SOIC	0° to +70°C
TC446*EJD	14-Pin CerDIP	– 40° to +85°C
TC446*MJD	14-Pin CerDIP	– 55° to +125°C

*A digit must be added in this position to define the device input configuration: TC446X — 7 NAND
8 AND
9 AND with INV

GENERAL DESCRIPTION

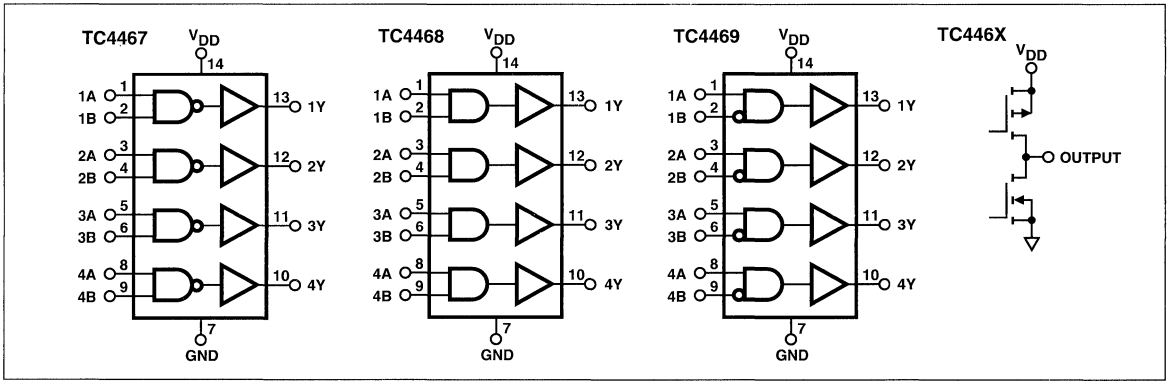
The TC446X family of four-output CMOS buffer/drivers are an expansion from our earlier single- and dual-output drivers. Each driver has been equipped with a two-input logic gate for added flexibility.

The TC446X drivers can source up to 250 mA into loads referenced to ground. Heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be driven easily with the 446X series drivers. The only limitation on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

The TC446X series drivers are built using TelCom Semiconductor's new Tough CMOS™ process. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset. In addition, all terminals are protected against ESD to at least 2000V. Even the molding epoxy used on our plastic packages has been custom developed to contain less sodium and chlorine contamination than standard commercial molding compounds. In tests, it demonstrated zero device failures after 10,000 hours in an 85°C, 85% relative humidity environment.

3

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage ..... (GND – 5V) to (V_{DD} + 0.3V)
Maximum Chip Temperature
  Operating ..... +150°C
  Storage ..... – 65° to +150°C
Maximum Lead Temperature
  (Soldering, 10 sec) ..... +300°C
Operating Ambient Temperature Range
  C Device ..... 0° to +70°C
  E Device ..... – 40° to +85°C
  M Device ..... – 55° to +125°C
Power Dissipation
  JD Package (14-Pin CerDIP) 1.25W
  PD Package (14-Pin Plastic DIP) 1.5W
  OE Package (16-Pin Wide SOIC) 1W

Package Thermal Resistance

JD Package (14-Pin CerDIP)	$R_{\theta J-A}$	100°C/W
	$R_{\theta J-C}$	23°C/W
PD Package (14-Pin Plastic DIP)	$R_{\theta J-A}$	80°C/W
	$R_{\theta J-C}$	35°C/W
OE Package (16-Pin Wide SOIC)	$R_{\theta J-A}$	95°C/W
	$R_{\theta J-C}$	28°C/W

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage	Note 3	2.4		V_{DD}	V
V_{IL}	Logic 0, Low Input Voltage	Note 3	0		0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 1		1	µA
Output						
V_{OH}	High Output Voltage	I_{LOAD} = 100 µA (Note 1)	V_{DD} – 0.025			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA (Note 1)			0.15	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V		10	15	Ω
I_{PK}	Peak Output Current			1.2		A
I_{DC}	Continuous Output Current	Single Output Total Package			300 500	mA mA
I	Latch-Up Protection Withstand Reverse Current	4.5V ≤ V_{DD} ≤ 16V	500			mA
Switching Time						
t_R	Rise Time	Figure 1		15	25	ns
t_F	Fall Time	Figure 1		15	25	ns
t_{D1}	Delay Time	Figure 1		40	75	ns
t_{D2}	Delay Time	Figure 1		40	75	ns
Power Supply						
I_S	Power Supply Current			1.5	4	mA
V_{DD}	Power Supply Voltage	Note 2	4.5		18	V

TRUTH TABLE

Part No.	TC4467 NAND				TC4468 AND				TC4469 AND/INV			
INPUTS A	H	H	L	L	H	H	L	L	H	H	L	L
INPUTS B	H	L	H	L	H	L	H	L	H	L	H	L
OUTPUTS TC446X	L	H	H	H	H	L	L	L	L	H	L	L

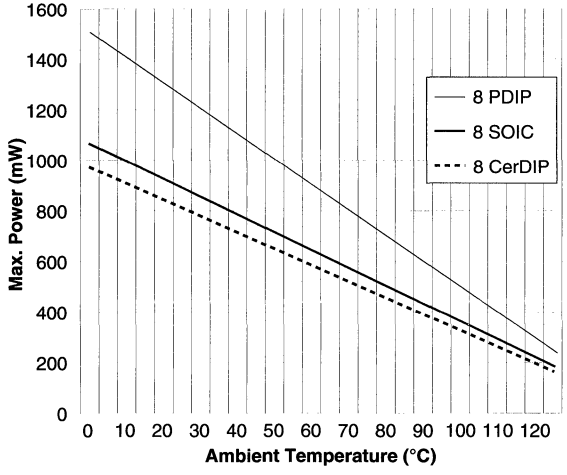
H = High L = Low

ELECTRICAL CHARACTERISTICS: Measured throughout operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

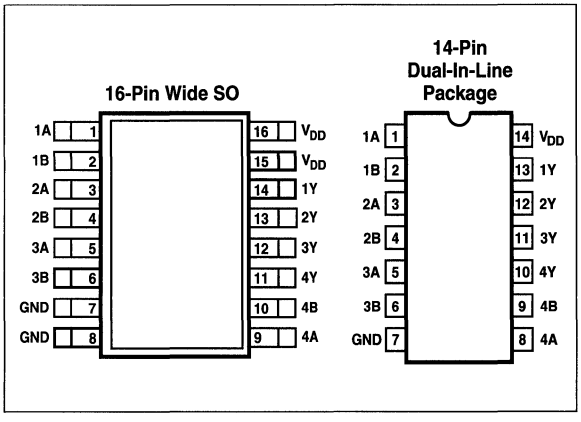
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage	(Note 3)	2.4			V
V_{IL}	Logic 0, Low Input Voltage	(Note 3)			0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{DD}$	– 10		10	µA
Output						
V_{OH}	High Output Voltage	I_{LOAD} = 100 µA (Note 1)	V_{DD} – 0.025			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA (Note 1)			0.30	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V		20	30	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current	$4.5V \le V_{DD} \le 16V$	500			mA
Switching Time						
t_R	Rise Time	Figure 1			50	ns
t_F	Fall Time	Figure 1			50	ns
t_{D1}	Delay Time	Figure 1			100	ns
t_{D2}	Delay Time	Figure 1			100	ns
Power Supply						
I_S	Power Supply Current				8	mA
I_S	Power Supply Voltage	Note 2	4.5		18	V

NOTES: 1. Totem-pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device.
2. When driving all four outputs simultaneously in the same direction, V_{DD} shall be limited to 16V. This reduces the chance that internal dv/dt will cause high-power dissipation in the device.
3. The input threshold has about 50 mV of hysteresis centered at approximately 1.5V. Slow moving inputs will force the device to dissipate high peak currents as the input transitions through this band. Input rise times should be kept below 5 µs to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum or below the minimum input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

Thermal Derating Curve



PIN CONFIGURATIONS



Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, charging a 1000 pF load to 18V in 25 ns requires 0.72A from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a 1 μF film capacitor in parallel with one or two low-inductance 0.1 μF ceramic disk capacitors with short lead lengths (<0.5 in.) normally provide adequate bypassing.

Grounding

The TC4467 and TC4469 contain inverting drivers. Potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics. Instead, individual ground returns for input and output circuits, or a ground plane, should be used.

Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With logic "0" outputs, maximum quiescent supply current is 4 mA. Logic "1" output level signals reduce quiescent current to 1.4 mA maximum. Unused driver inputs must be connected to V_{DD} or V_{SS}. Minimum power dissipation occurs for logic "1" outputs.

The drivers are designed with 50 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making any voltage greater than 1.5V up to V_{DD} a logic 1 input . Input current is less than 1 μA over this range.

Power Dissipation

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. TelCom Semiconductor's CMOS drivers have greatly reduced quiescent DC power consumption.

Input signal duty cycle, power supply voltage and load type, influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operating temperature is easily calculated. The 14-pin plastic package junction-to-ambient thermal resistance is 83.3°C/W. At +25°C, the package is rated at 1500 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

(1) Load-caused dissipation (P_L)
(2) Quiescent power (P_Q)
(3) Transition power (P_T).

A capacitive-load-caused dissipation (driving MOSFET gates), is a direct function of frequency, capacitive load, and supply voltage. The power dissipation is:

$$P_L = f\ C\ V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

A resistive-load-caused dissipation for ground-referenced loads is a function of duty cycle, load current, and load voltage. The power dissipation is:

$$P_L = D\ (V_S - V_L)\ I_L,$$

where: D = Duty cycle
V_S = Supply voltage
V_L = Load voltage
I_L = Load current.

A resistive-load-caused dissipation for supply-referenced loads is a function of duty cycle, load current, and output voltage. The power dissipation is:

$$P_L = D\ V_O\ I_L,$$

where: f = Switching frequency
V_O = Device output voltage
I_L = Load current.

Quiescent power dissipation depends on input signal duty cycle. Logic HIGH outputs result in a lower power dissipation mode, with only 0.6 mA total current drain (all devices driven). Logic LOW outputs raise the current to 4 mA maximum. The quiescent power dissipation is:

$$P_Q = V_S\ (D(I_H) + (1-D)I_L),$$

where: I_H = Quiescent current with all outputs LOW (4 mA max)
I_L = Quiescent current with all outputs HIGH (0.6 mA max)
D = Duty cycle
V_S = Supply voltage.

Transition power dissipation arises in the complementary configuration (TC446X) because the output stage N-channel and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition power dissipation is approximately:

$P_T = f\,V_S\,(10 \times 10^{-9})$.

Package power dissipation is the sum of load, quiescent and transition power dissipations. An example shows the relative magnitude for each term:

C = 1000 pF capacitive load
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package Power Dissipation = $P_L + P_Q + P_T$

= 45 mW + 35 mW + 30 mW = 110 mW.

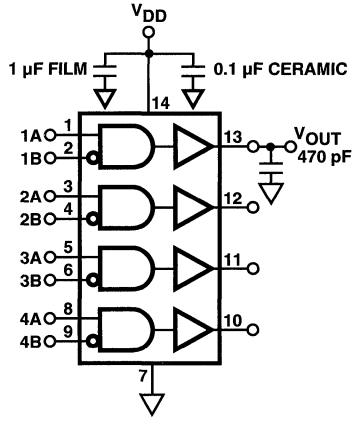
Maximum operating temperature:

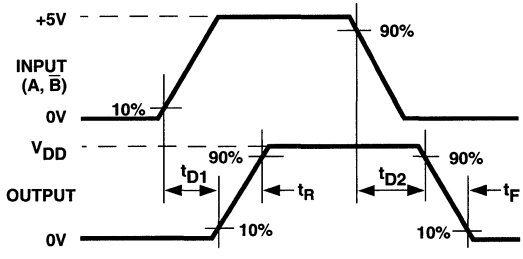
$T_J - \theta_{JA}\,(P_D) = 141°C$,

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (83.3°C/W) 14-pin plastic package.

NOTE: Ambient operating temperature should not exceed +85°C for "EJD" device or +125°C for "MJD" device.

3



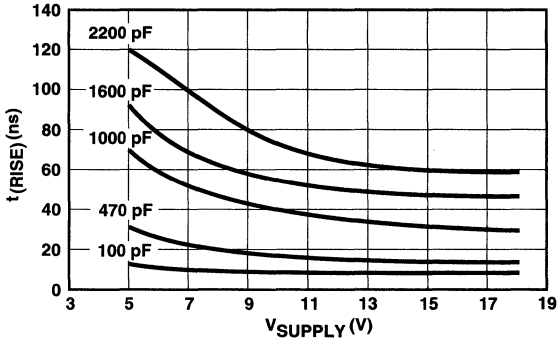


Input: 100 kHz, square wave,
$t_{RISE} = t_{FALL} \leq 10$ns

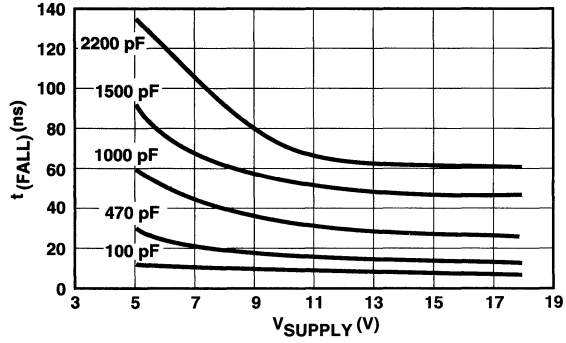
Figure 1 Switching Time Test Circuit

CHARACTERISTICS CURVES

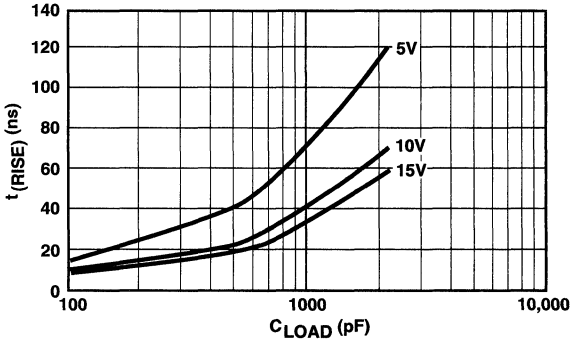
Rise Time vs Supply Voltage



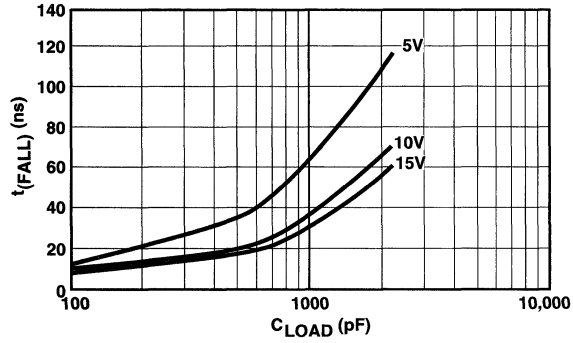
Fall Time vs Supply Voltage



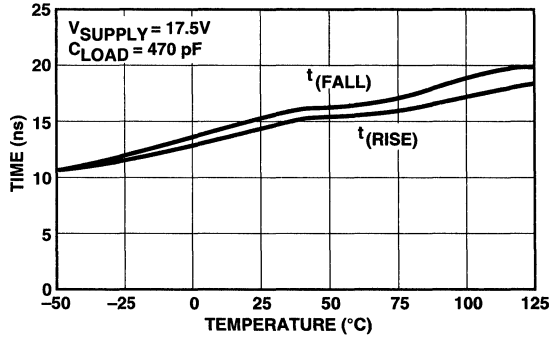
Rise Time vs Capacitive Load



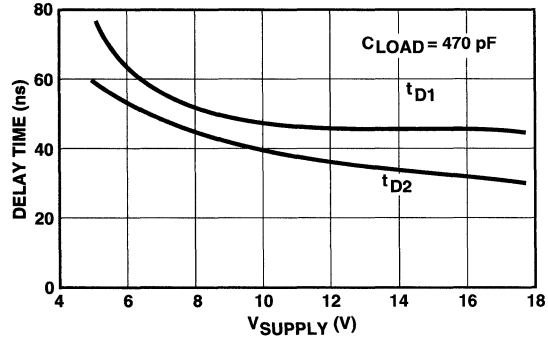
Fall Time vs Capacitive Load



Rise/Fall Times vs Temperature

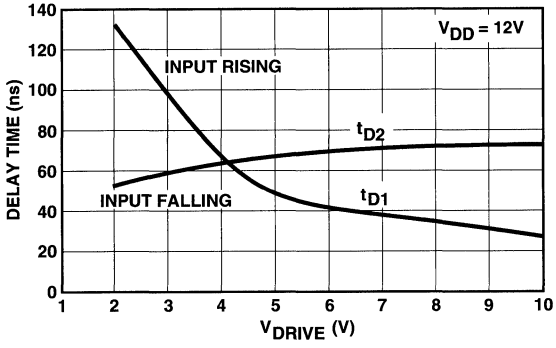


Propagation Delay Time vs Supply Voltage

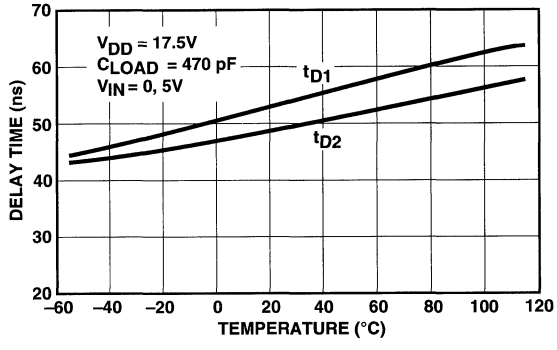


CHARACTERISTICS CURVES (Cont.)

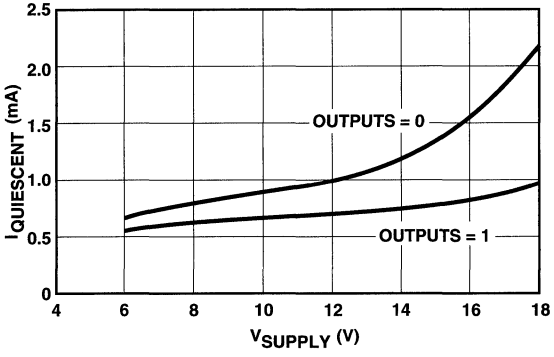
Input Amplitude vs Delay Times



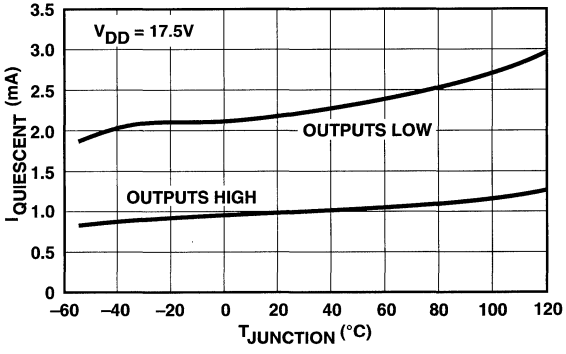
Propagation Delay Times vs Temperature



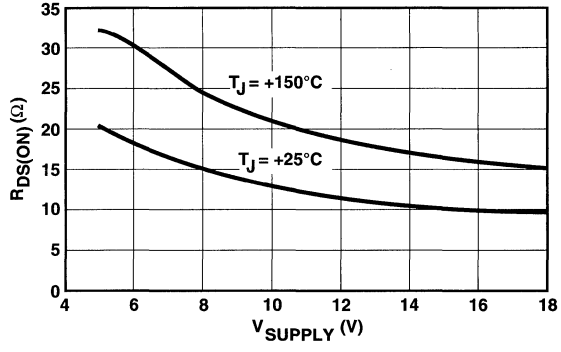
Quiescent Supply Current vs Supply Voltage



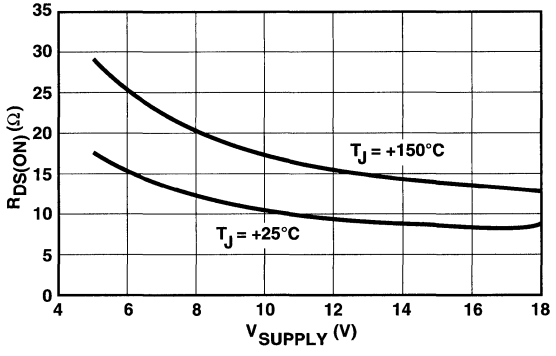
Quiescent Supply Current vs Temperature



High-State Output Resistance

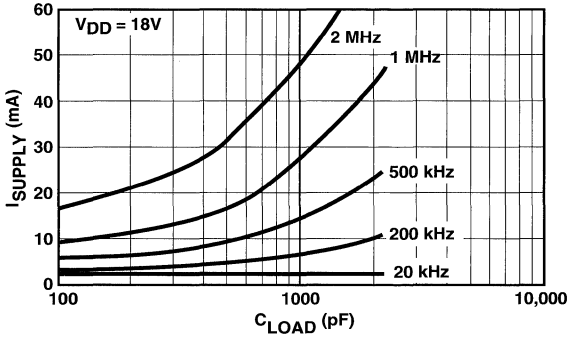


Low-State Output Resistance

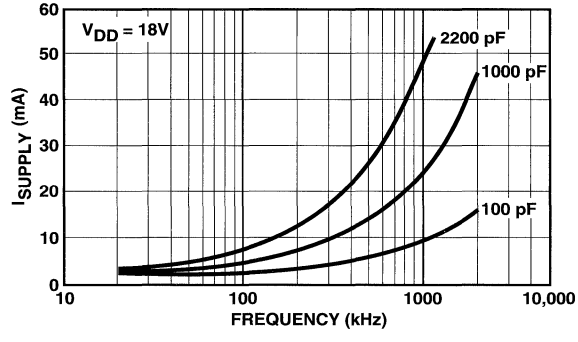


SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

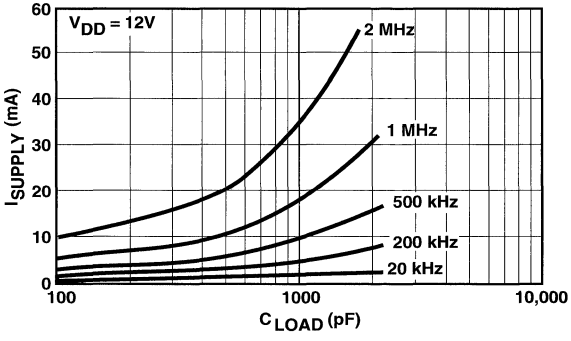
Supply Current vs Capacitive Load



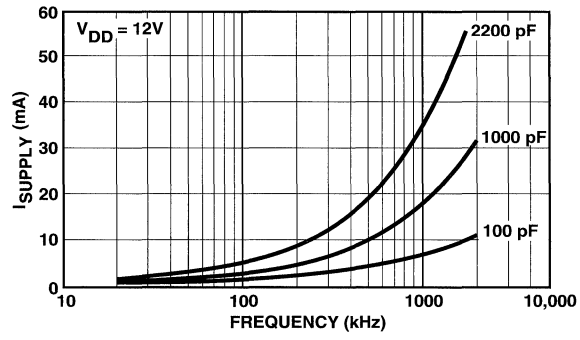
Supply Current vs Frequency



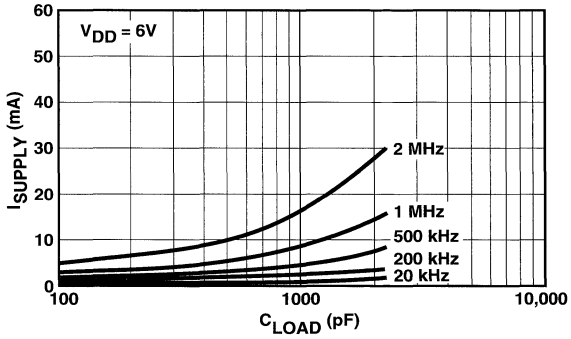
Supply Current vs Capacitive Load



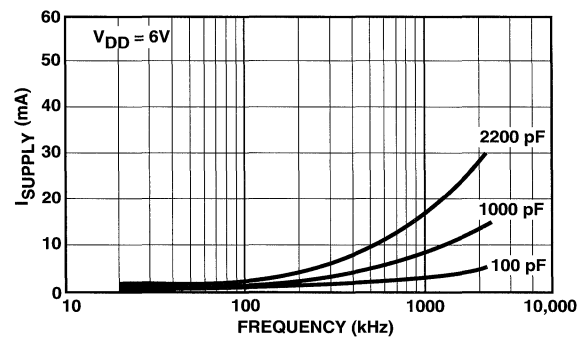
Supply Current vs Frequency



Supply Current vs Capacitive Load

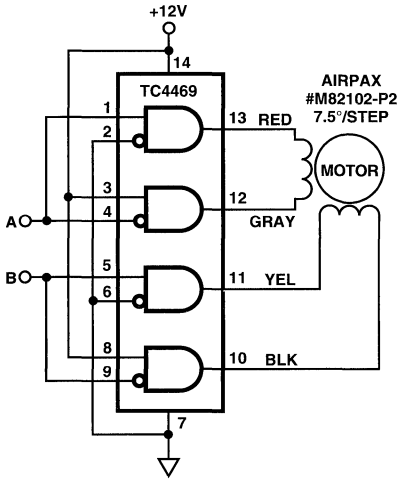


Supply Current vs Frequency

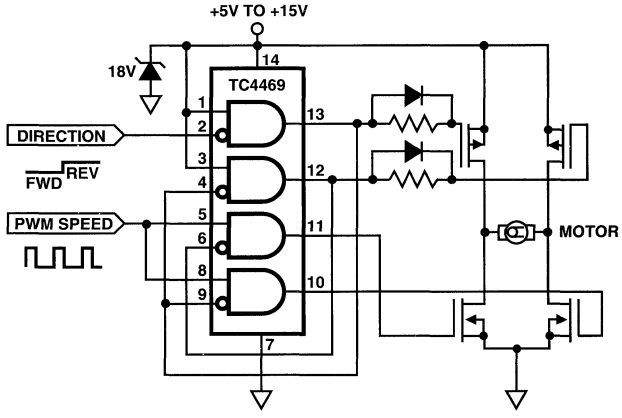


TYPICAL APPLICATIONS

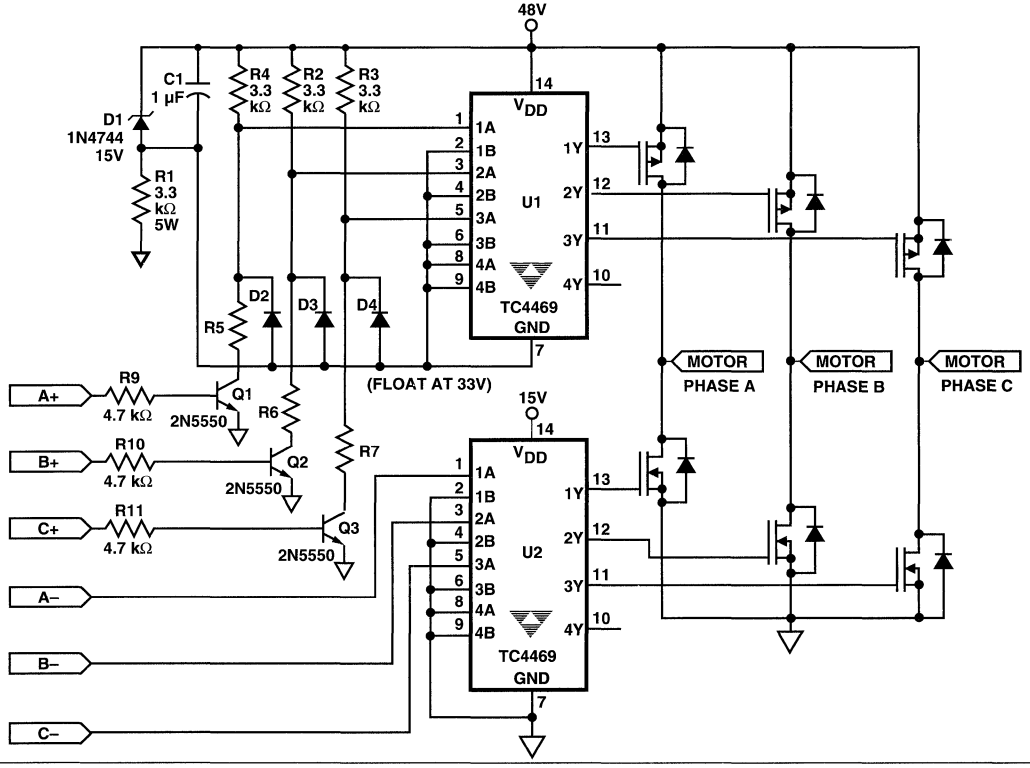
Stepper Motor Drive



Quad Driver for H-Bridge Motor Control



48-Volt, 3-Phase Brushless Output Stage



POWER CMOS DRIVERS WITH VOLTAGE TRIPLER

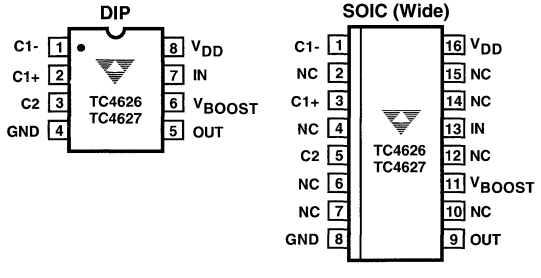
FEATURES

- **Power driver with on Board Voltage Booster**
- **Low IDD < 4 mA**
- **Small Package - 8 Pin PDIP**
- **Under-Voltage Circuitry**
- **Fast Rise-Fall Time < 40 ns @ 1000pF**
- **Below-Rail Input Protection**

APPLICATIONS

- **Raises 5V to drive higher-Vgs(ON) MOSFETs**
- **Eliminates one system power supply**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

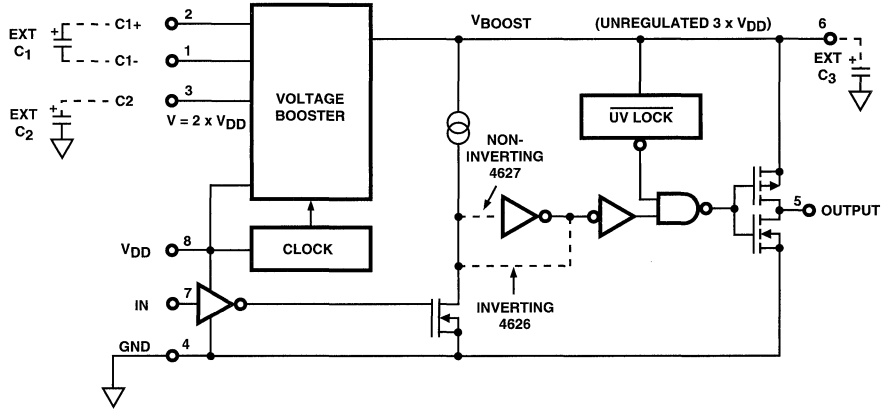
The TC4626/4627 are single CMOS high speed drivers with an on-board voltage boost circuit. These parts work with an input supply voltage from 4 to 6 volts. The internal voltage booster will produce a V_{BOOST} potential up to 12 volts above V_{IN}. This V_{BOOST} is not regulated, so its voltage is dependent on the input V_{DD} voltage and output drive loading requirements. An internal undervoltage lockout circuit keeps the output in a low state when V_{BOOST} drops below 7.8 volts. Output is enabled when V_{BOOST} is above 11.3 volts.

3

ORDERING INFORMATION

Part No.	Package
TC4626MJA	8-Pin CerDIP
TC4626EPA	8-Pin PDIP
TC4626EOE	16-Pin SOIC (Wide)
TC4626CPA	8-Pin PDIP
TC4626COE	16-Pin SOIC (Wide)
TC4627MJA	8-Pin CerDIP
TC4627EPA	8-Pin PDIP
TC4627EOE	16-Pin SOIC (Wide)
TC4627CPA	8-Pin PDIP
TC4627COE	16-Pin SOIC (Wide)

FUNCTIONAL BLOCK DIAGRAM



NOTE: Pin numbers correspond to 8-pin package

ABSOLUTE MAXIMUM RATINGS

Power Dissipation
- PDIP ..... 500 mW
- CerDIP 800mW

Derating Factor
- PDIP ..... 5.6 mW/°C Above 36°C
- CerDIP ..... 6.0 mW/°C

Supply Voltage 6.2V

Input Voltage, Any Terminal ..... V_S + 0.3V to GND – 0.3V
Operating Temperature: M Version ..... - 55°C to +125°C
E Version ..... - 40°C to +85°C
C Version ..... 0°C to +70°C
Maximum Chip Temperature ..... +150°C
Storage Temperature ..... - 65°C to +150°C
Lead Temperature (10 sec) ..... +300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C V_{DD} = 5V $C_1 = C_2 = C_3$ 10µF unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Driver Input						
V_{IH}	Logic 1, Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{DRIVE}$	– 1	—	1	µA
Driver Output						
V_{OH}	High Output Voltage		V_{BOOST} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 5V	—	10	15	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 5V	—	8	10	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time						
t_R	Rise Time	Test Figure 1,2	—	33	40	ns
t_F	Fall Time	Test Figure 1,2	—	27	35	ns
t_{D1}	Delay Time	Test Figure 1,2	—	35	45	ns
t_{D2}	Delay Time	Test Figure 1,2	—	45	55	ns
F_{MAX}	Maximum Switching Frequency	Test Figure 1	1.0	—	—	MHz
		V_{DD} = 5V, V_{BOOST} > 8.5V				
Voltage Booster						
R_3	Voltage Tripler Output Source Resistance	I_L = 10 mA, V_{DD} = 5V	—	300	400	Ω
R_2	Voltage Doubler Output Source Resistance		—	120	200	Ω
F_{OSC}	Oscillator Frequency		12	—	28	kHz
V_{OSC}	Oscillator Amplitude Measured at C1-	R_{LOAD} = 10kΩ	4.5	—	10	V
UV @ V_{BOOST}	Undervoltage Threshold		7.0	7.8	8.5	V
V_{START} @ V_{BOOST}	Start Up Voltage		10.5	11.3	12	V
V_{BOOST}	@V_{DD} = 5V	No Load	14.6	—	—	V
Power Supply						
I_{DD}	Power Supply Current	V_{IN} = LOW or HIGH	—	—	2.5	mA
V_{DD}	Supply Voltage		4.0	—	6.0	V

ELECTRICAL CHARACTERISTICS (T_A = Over Operating Temperature Range V_{DD} = 5V $C_1 = C_2 = C_3$ 10µF unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Driver Input						
V_{IH}	Logic 1, Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{BOOST}$	–10	—	10	µA
Driver Output						
V_{OH}	High Output Voltage		V_{DRIVE} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 5V				
		C & E Version (T_A = 70°C or 85°C)	—	15	20	Ω
		M Version (T_A = 125°C)	—	15	25	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 5V				
		C & E Version (T_A = 70°C or 85°C)	—	10	13	Ω
		M Version (T_A = 125°C)	—	10	15	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time						
t_R	Rise Time	Test Figure 1,2	—	—	55	ns
t_F	Fall Time	Test Figure 1,2	—	—	50	ns
t_{D1}	Delay Time	Test Figure 1,2	—	—	60	ns
t_{D2}	Delay Time	Test Figure 1,2	—	—	70	ns
F_{MAX}	Maximum Switching Frequency	Test Figure 1	750	—	—	kHz
		V_{DD} = 5V, V_{Boost} > 8.5V				
Voltage Booster						
R_3	Voltage Boost Output Source Resistance	I_L = 10 mA, V_{DD} = 5V	—	400	500	Ω
R_2	Voltage Doubler Output Source Resistance		—	170	300	Ω
F_{OSC}	Oscillator Frequency		5	—	50	kHz
V_{OSC}	Oscillator Amplitude Measured at C1-	R_{LOAD} = 10kΩ	4.5	—	10	V
UV @ V_{BOOST}	Undervoltage Threshold		7.0	7.8	8.5	V
V_{START} @ V_{BOOST}	Start Up Voltage		10.5	11.3	12	V
V_{BOOST}	@V_{DD} = 5V	No Load	14.6	—	—	V
Power Supply						
I_{DD}	Power Supply Current	V_{IN} = LOW or HIGH	—	—	4	mA
V_{DD}	Supply Voltage		4.0	—	6.0	V

SWITCHING TIME TEST CIRCUITS

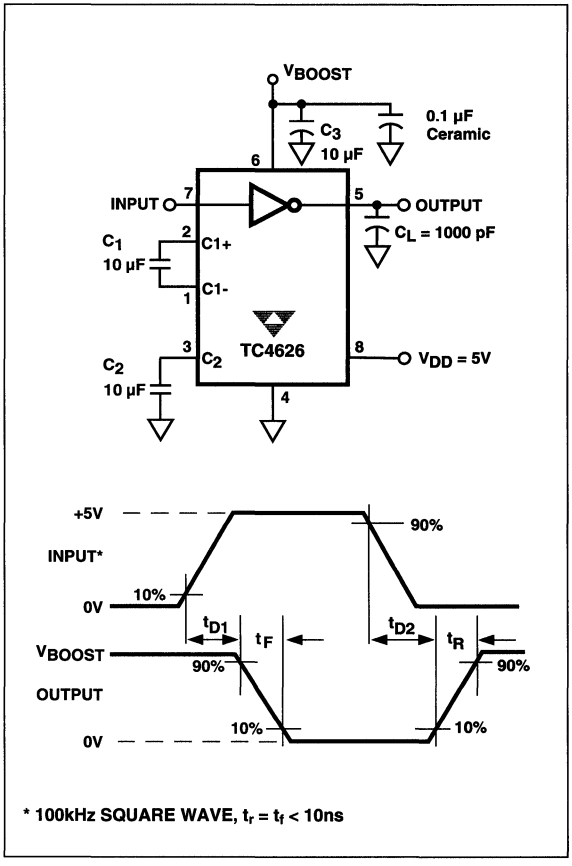


Figure 1. Inverting Driver Switching Time

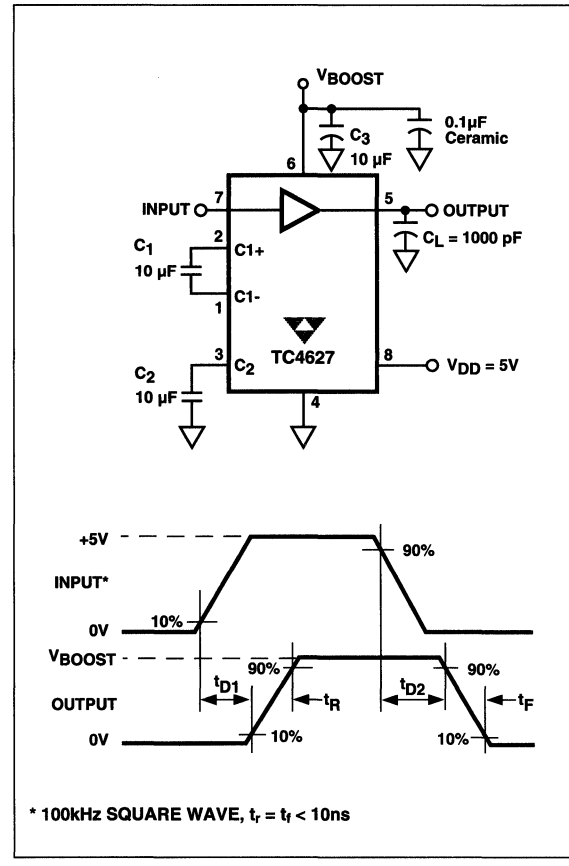
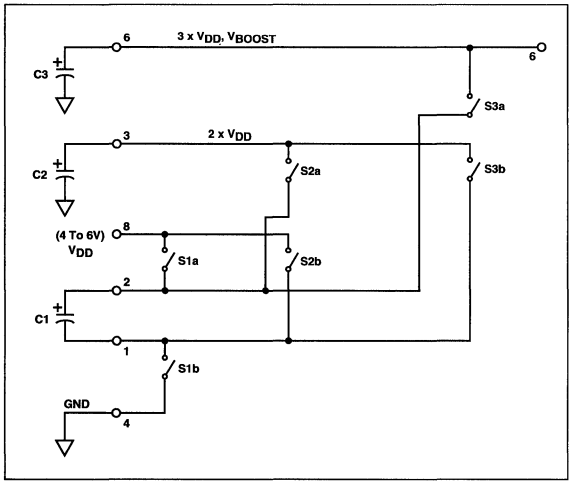


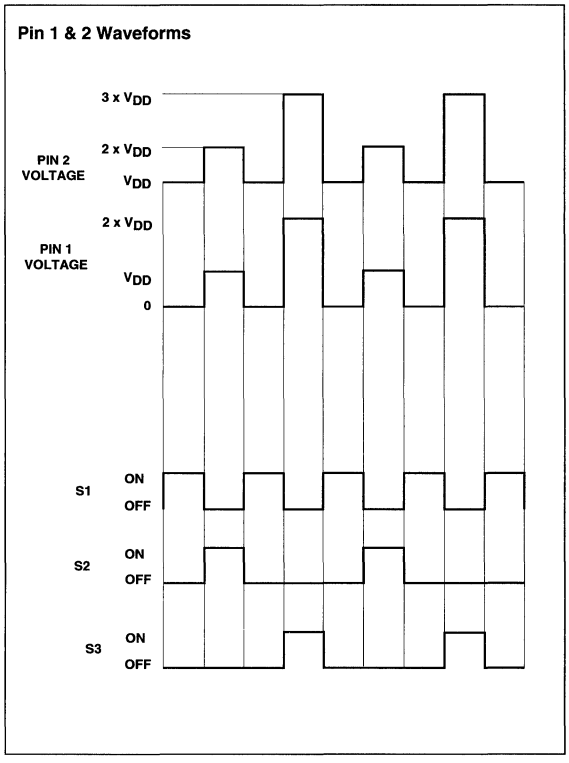
Figure 2. Non-Inverting Driver Switching Time

BOOSTER FUNCTION

The voltage booster is an unregulated voltage tripler circuit. The tripler consists of three sets of internal switches and three external capacitors. S1a and S1b charge capacitor C1 to V_{DD} potential. S2a and S2b add C1 potential to V_{DD} input to charge C2 to 2 x V_{DD}. S3a and S3b add C1 potential to C2 to charge C3 to 3 x V_{DD}. The position of the switches is controlled by the internal 4 phase clock.



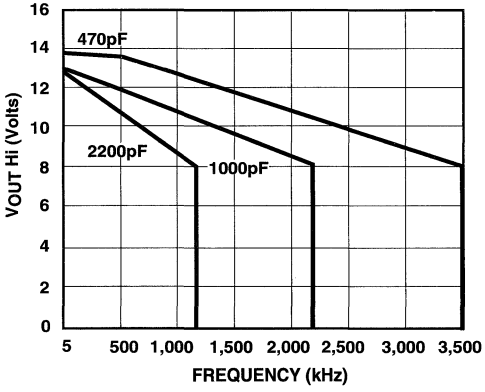
Voltage Booster



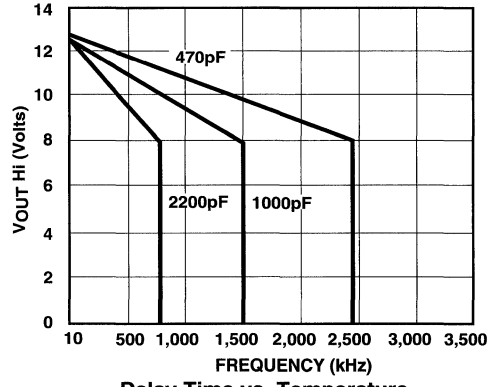
Position of Switches

TYPICAL CHARACTERISTICS CURVES

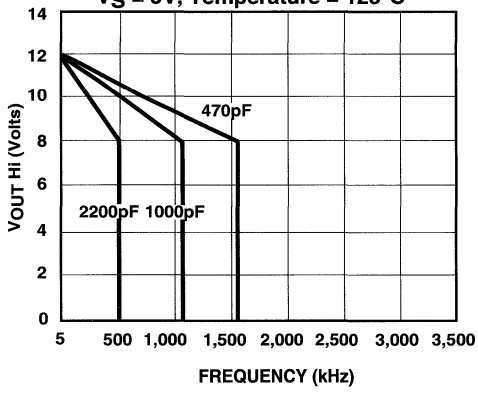
TC4626 V_{OH} vs. Frequency
V_S = 5V, Temperature = –55°C



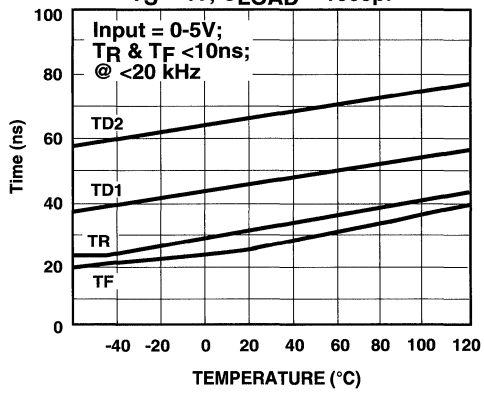
TC4626 V_{OH} vs. Frequency
V_S = 5V, Temperature = 25°C



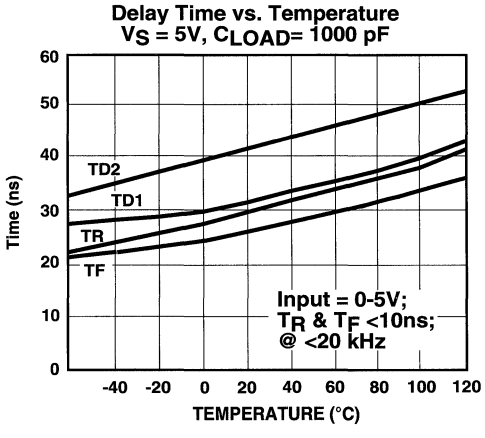
TC4626 V_{OH} vs. Frequency
V_S = 5V, Temperature = 125°C



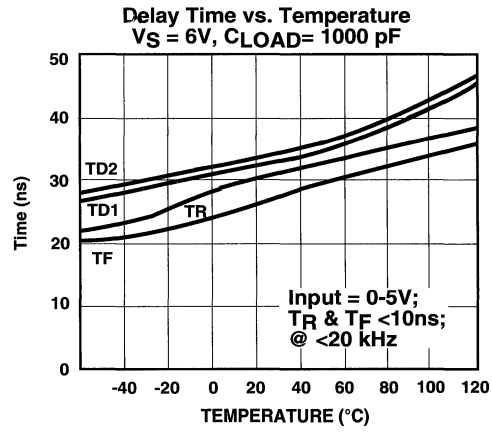
Delay Time vs. Temperature
V_S = 4V, C_{LOAD} = 1000pF



Delay Time vs. Temperature
V_S = 5V, C_{LOAD}= 1000 pF

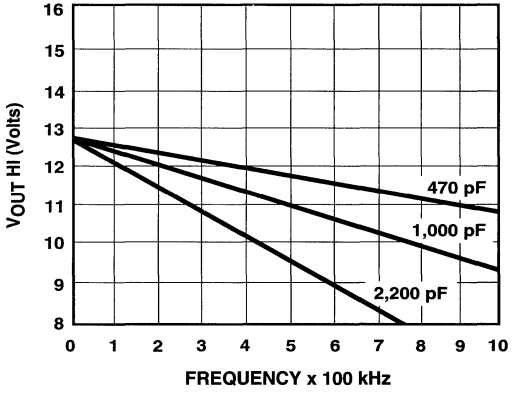


Delay Time vs. Temperature
V_S = 6V, C_{LOAD}= 1000 pF

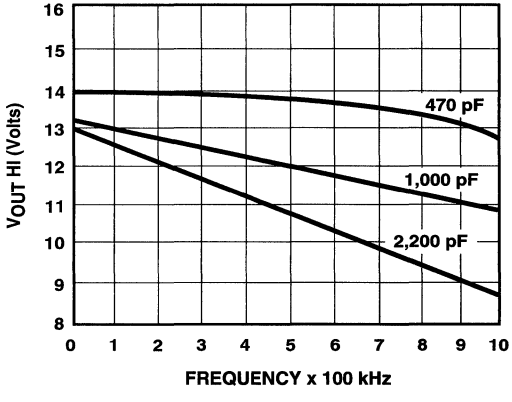


TYPICAL CHARACTERISTICS CURVES

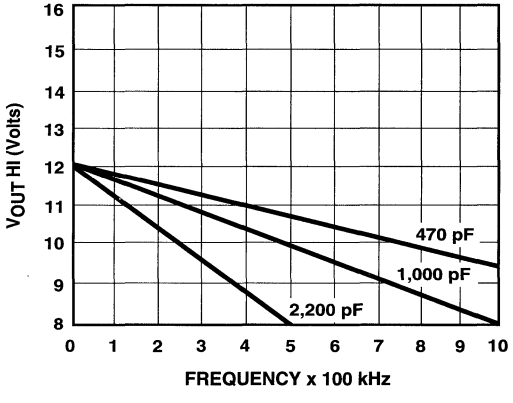
TC4626 V_{OH} vs. Frequency
V_S = 5V, Temperature = 25°C



TC4626 V_{OH} vs. Frequency
V_S = 5V, Temperature = -55°C



TC4626 V_{OH} vs. Frequency
V_S = 5V, Temperature = 125°C



1.4A HIGH-SPEED OPTO-ISOLATED POWER MOSFET DRIVER

FEATURES

- **Input to Output Isolation to 2.5kV RMS**
- **Operating Range ..... 10V to 18V**
- **High Peak Output Current ..... 1.4A Typ**
- **Short Delay Time ..... <250 ns Typ**
- **Fast Switching on Outputs ..... T_R, T_F < 80ns Typ ..... with C_L = 1000pF**
- **Low Power BiCMOS Design**
- **Undervoltage Lock-out with Hysteresis**
- **Available in 8-pin DIP with SMT-formed leads**

APPLICATIONS

- **Isolated Digital Line Driver**
- **Isolated Line Receiver**
- **"High-Side" Driver**
- **SMPS Control**
- **High-side Motor Control**
- **Solid State Relays**
- **Off-Line Regulation/Control**

UL File No: E151672 on TC4803/4

GENERAL DESCRIPTION

The TC4803 AND TC4804 are BiCMOS optocoupled driver ICs for switching loads when electrical isolation is desired. Input drive current is converted to low impedance voltage drive with the ability to source 1.4A peak current into a capacitive load of 1,000 pF with fast output rise and fall times. UV lockout circuitry forces the output to an "OFF" state when the supply voltage drops below 7.8V. 0.4V of hysteresis prevents output toggling around the drop-out voltage. The output "OFF" state is LOW on both the TC4803 and the TC4804.

Because shoot-through currents are reduced in the output stage, these drivers consume significantly less power at higher frequencies, and can be helpful in meeting low-power budgets.

These devices are built using TelCom Semiconductor's new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments. They will not latch under normal conditions within their power and voltage ratings.

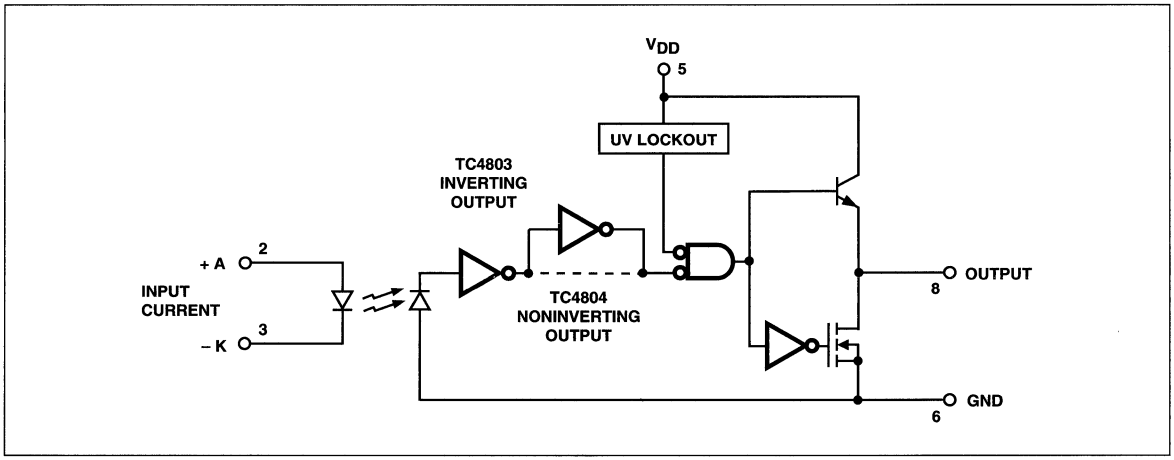
All terminals are fully protected against up to 4 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Package	Operating Temp Range
TC4803CPA	8-Pin PDIP	0°C to +70°C
TC4803EPA	8-Pin PDIP	–40°C to +85°C
TC4803EFA*	8-Pin PDIP*	–40°C to +85°C
TC4803CFA*	8-Pin PDIP*	0°C to +70°C
TC4804CPA	8-Pin PDIP	0°C to +70°C
TC4804EPA	8-Pin PDIP	–40°C to +85°C
TC4804EFA*	8-Pin PDIP*	–40°C to +85°C
TC4804CFA*	8-Pin PDIP*	0°C to +70°C

* Plastic DIP with preformed surface mount leads

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Diode Current Input 20mA
Maximum Chip Temperature ..... 85°C
Storage Temperature Range ..... –55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Thermal Resistance
PDIP $R_{\theta J-A}$ ..... 200°C/W
Operating Temperature Range
Thermal Derating ..... 5mW/°C above 25°C
Power Dissipation 300mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

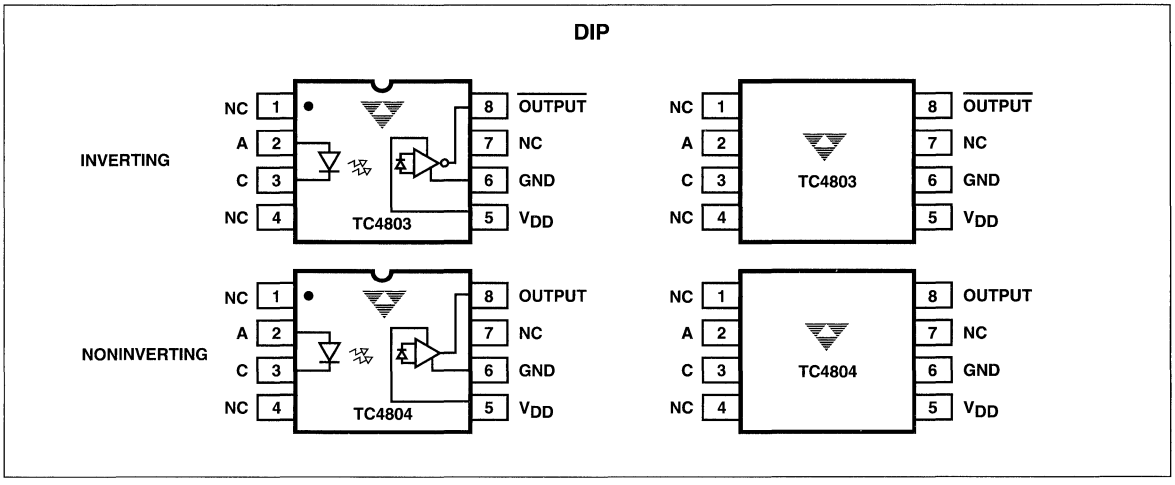
ELECTRICAL CHARACTERISTICS:

Typical specifications measured at T_A = +25°C with V_{DD} = 18V, unless otherwise specified. Minimum and maximum specifications guaranteed over full temperature and power supply range.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input LED						
$I_{F(TH)}$-ON	LED Forward Threshold "ON"-Current (DC)		5	—	—	mA
$I_{F(TH)}$-OFF	LED Forward Threshold "OFF"-Current (DC)		—	—	0.5	mA
V_F	LED Forward Voltage @ 7 mA Current		1.3	1.5	1.7	V
V_R	LED Reverse Voltage @ 50nA		6.0	—	—	V
	Isolation Voltage		2.5	—	—	kVRMS
Output						
V_{OH}	High Output Voltage, V_{DD} =18V, I_{OUT} = 50mA		16.3	16.9	—	V
V_{OL}	Low Output Voltage, V_{DD} =18V, I_{OUT} = 50mA		—	0.70	1.0	V
I_{PK}	Peak Output Current (Note 1)	Source	—	1.4	—	A
		Sink		0.5		A
I_{DC}	Continuous Output Current V_{DD} = 18V (Source, sink)		100	—	—	mA
	DV/DT Input to Output Common Mode Transient Immunity @ 150V		0.25	—	—	V/ns
Switching Time						
t_R	Rise Time	Figure 1	—	35	60	ns
t_F	Fall Time	Figure 1	—	40	80	ns
t_{D1}	Delay Time	Figure 1 (4803)	—	160	200	ns
t_{D2}	Delay Time	Figure 1 (4803)	—	200	500	ns
t_{D1}	Delay Time	Figure 1 (4804)	—	160	200	ns
t_{D2}	Delay Time	Figure 1 (4804)	—	240	500	ns
F_{MAX}	Maximum Operating Frequency		1	1.2	—	MHz
Power Supply						
I_{DD}	Power Supply Current	Output HIGH	—	4.0	8.0	mA
I_{DD}	Power Supply Current	Output LOW	—	3.0	5.0	mA
V_S	Start up threshold		—	8.7	10.0	V
V_{UV}	Drop-out threshold		7.5	8.4	—	V

NOTE: 1. 1µs, 1% duty cycle pulse input, output shorted to V_{DD} or GND.

PIN CONFIGURATION



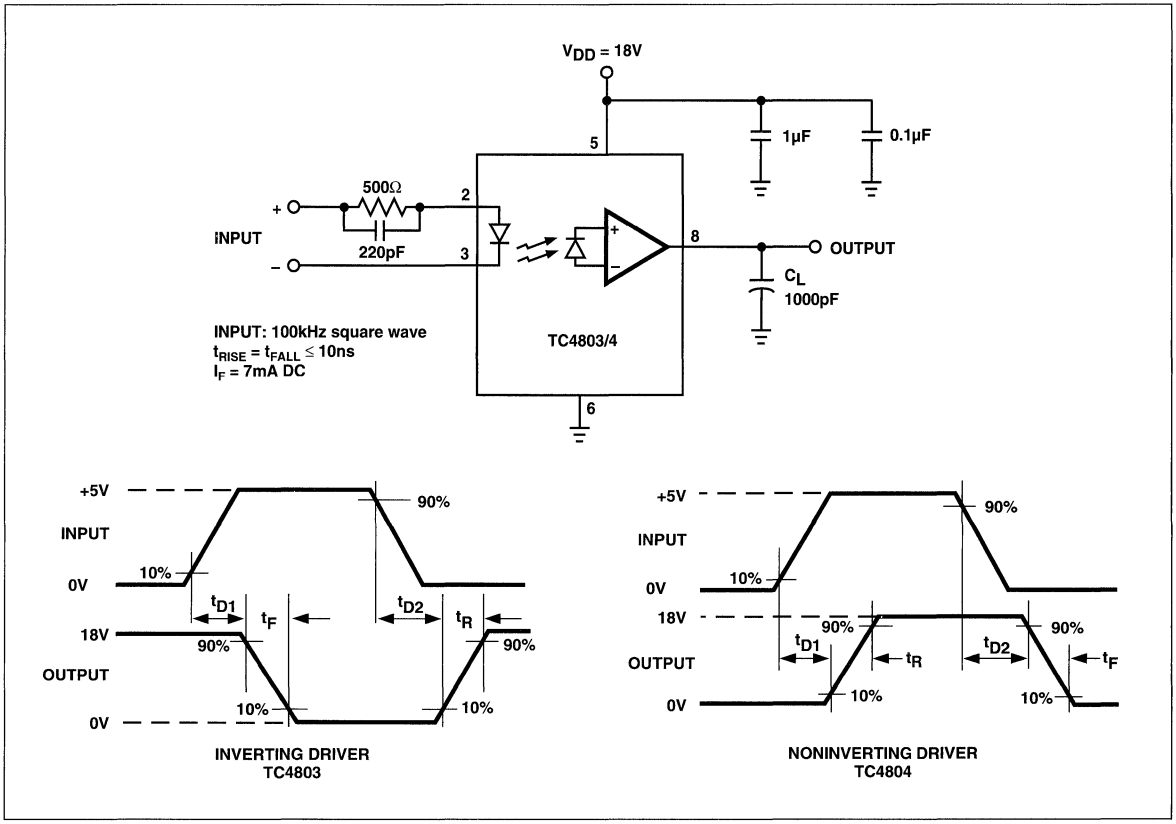
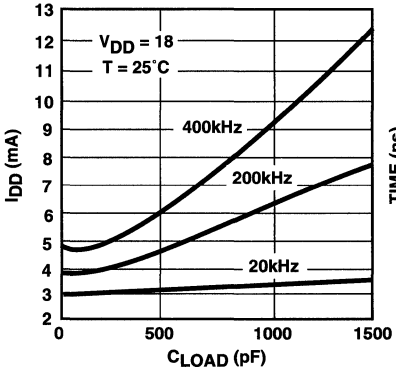


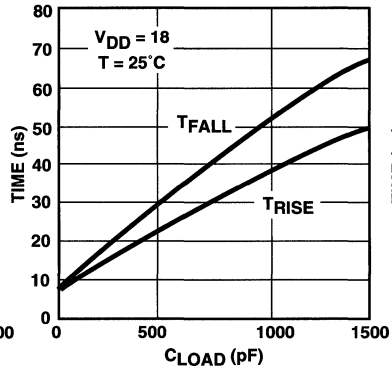
Figure 1 Switching Time Test Circuit

TYPICAL CHARACTERISTIC CURVES

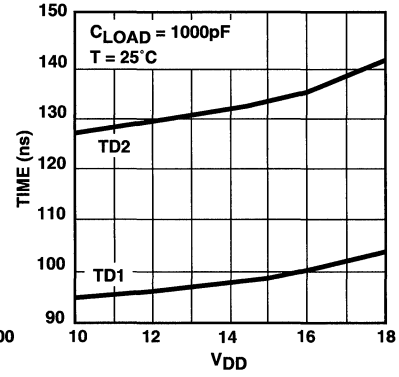
I_{DD} vs. C_{LOAD}



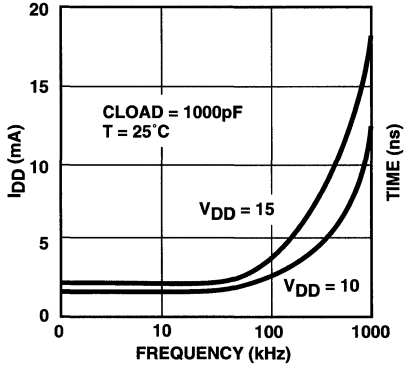
Rise, Fall Time vs. C_{LOAD}



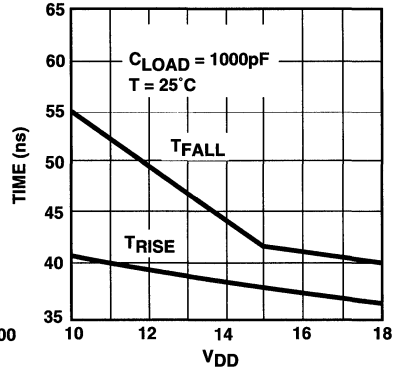
Delay Time vs. V_{DD}



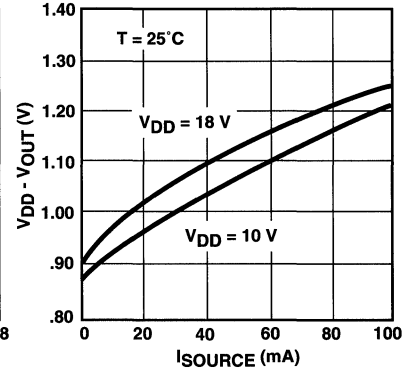
I_{DD} vs. Frequency



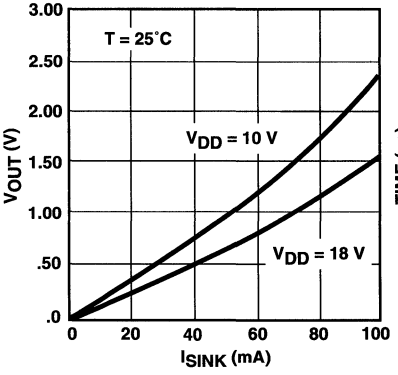
Rise, Fall Time vs. V_{DD}



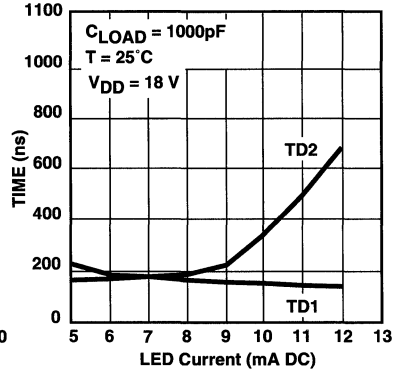
V_{OH} vs. I_{SOURCE}



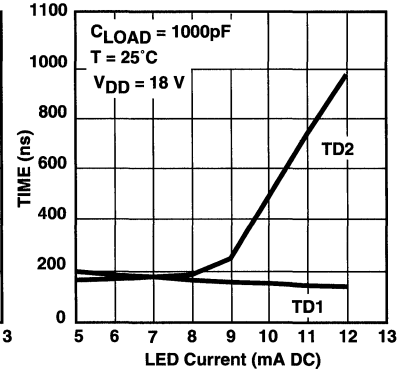
V_{OL} vs. I_{SINK}

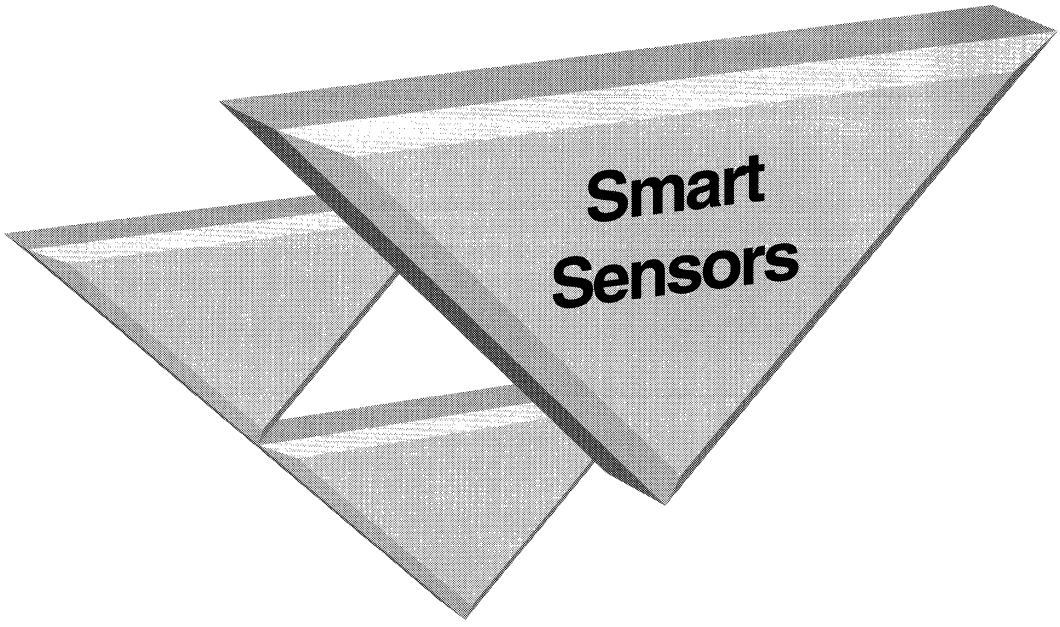


TC4803 Delay Time vs. LED Current



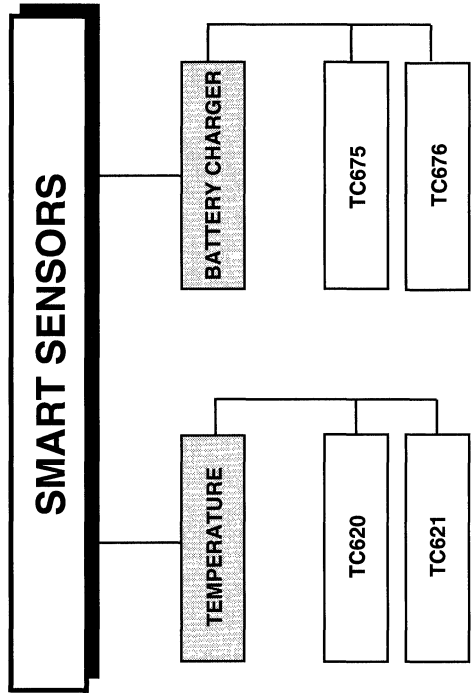
TC4804 Delay Time vs. LED Current





- Sensors
- Battery Chargers

4


SMART SENSORS
BATTERY CHARGER
TC675
TC676
TEMPERATURE
TC620
TC621

SOLID STATE TEMPERATURE SENSOR

FEATURES

- ±3°C Absolute Temperature Accuracy
- 2 kV ESD Protection on All Pins
- Replaces Mechanical Thermostats and Switches
- On-Chip Temperature Sense (TC620)
- External Temperature Sense (TC621)
- 8-Pin DIP or SOIC for Direct PCB Mounting
- 2 User-Programmable Temperature Set Points
- 2 Independent Temperature Limit Outputs
- Heat/Cool Regulate Output

APPLICATIONS

- Vibration-Immune Temperature Sensing
- System Over- or Under-Temperature Shutdown
- Advanced Thermal Warning
- Fan Speed Control Circuits
- Accurate Appliance Temperature Sensing

GENERAL DESCRIPTION

The TC620 and TC621 are programmable solid-state temperature switches designed to replace mechanical switches in temperature sensing and control applications. Ambient temperature is sensed and compared to programed minimums and maximums.

Both devices provide a LOW LIMIT and HIGH LIMIT logical output as well as a CONTROL output. On the TC620, the LOW LIMIT is LOW when the measured temperature is below the low temperature set-point and the HIGH LIMIT is LOW when the measured temperature is below the high temperature set-point. The TC621 provides the same output functions except that the logical states are inverted. These outputs allow for easy 'over' and 'under' temperature detection.

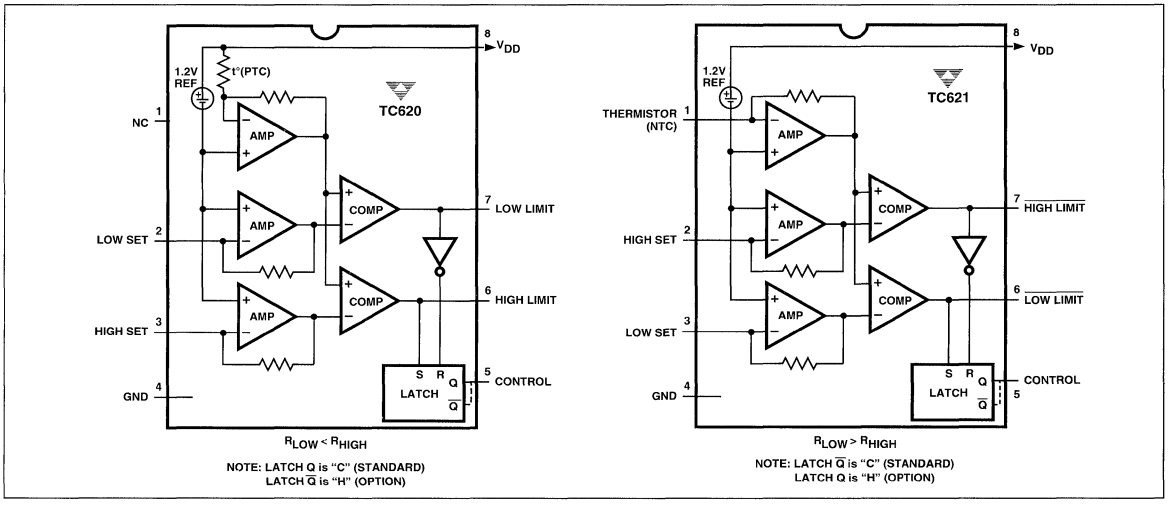
ORDERING INFORMATION

Part No.	Package	Ambient Temperature
TC620XCOA	8-Pin SOIC	0°C to +70°C
TC620XEOA	8-Pin SOIC	- 40°C to +85°C
TC620XVOA	8-Pin SOIC	- 40°C to +125°C
TC620XCPA	8-Pin Plastic DIP	0°C to +70°C
TC620XEPA	8-Pin Plastic DIP	- 40°C to +85°C

Part No.	Package	Ambient Temperature
TC621XCOA	8-Pin SOIC	0°C to+ 70°C
TC621XEOA	8-Pin SOIC	- 40°C to +85°C
TC621XCPA	8-Pin Plastic DIP	0°C to +70°C
TC621XEPA	8-Pin Plastic DIP	- 40°C to +85°C

X in the part code will be C or H (see Functional Block Diagram, below, and page 2).

FUNCTIONAL BLOCK DIAGRAM



TC620
TC621

ABSOLUTE MAXIMUM RATINGS*

Power Dissipation
- Plastic 1W
- CerDIP ..... 800 mW

Derating Factors
- Plastic ..... 8 mW/°C
- CerDIP ..... 6.4 mW/°C

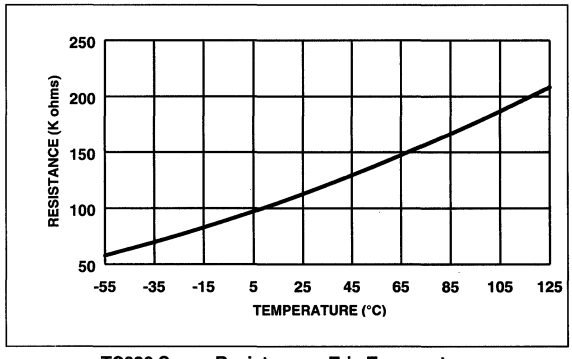
Supply Voltage 20V
Input Voltage Any Input ..... (Gnd -0.3) to (VDD +0.3)
Operating Temperature
- M Version ..... - 55 to +125°C
- V Version ..... - 40 to +125°C
- E Version ..... - 40 to +85°C
- C Version ..... 0 to +70°C

Maximum Chip Temperature ..... +150°C
Storage Temperature ..... - 65 to +150°C
Lead Temperature (10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (TA = 25°C)

Parameter		Conditions		Min	Typ	Max	Unit
Supply Voltage Range				4.5		18	V
Supply Current		$5V \le V_{DD} \le 18V$			170	200	µA
Output Resistance		Output High or Low, $5V \le V_{DD} \le 18V$			400	1000	Ω
Output Current	620	Temp Sensed	Source/Sink			1	mA
	621	Temp Sensed	Source/Sink			10	mA
Output Current	620	Cool/Heat	Source/Sink			1	mA
	621	Cool/Heat	Source/Sink			10	mA
Absolute Accuracy		T = Programmed Temperature		T -3	T	T +3	°C



TC620 Sense Resistors vs. Trip Temperature

Control and Limit Outputs

The CONTROL output provides a programmable hysteresis in that it goes HIGH when the measured temperature goes above the HIGH LIMIT set-point and returns to LOW when the measured temperature goes below the LOW LIMIT set-point. The CONTROL output of either device is easily applied to a temperature control system.

TelCom's proprietary technology provides excellent absolute temperature accuracy (±3°C). The low current requirement of these devices make them especially appealing in battery powered applications. The TC620 and TC621 have no moving parts so they are rugged and work well in equipment that needs to take a lot of abuse. Automotive, marine and industrial users will benefit from the ruggedness of these devices.

The LOW LIMIT and HIGH LIMIT temperatures are set by connecting the appropriate resistors to the LOW SET and HIGH SET inputs. The value of these SET resistors are a function of the temperature sensing element.

Internal Temperature Sensor (TC620)

The TC620 incorporates an on-board positive-temperature-coefficient (PTC) thermal sensor which reacts to the internal temperature of the die. The LOW SET resistor (pin 2) should always be lower than the HIGH SET resistor (pin 3) to insure proper operation.

External Temperature Sensor (TC621)

The TC621 performs the same function as the TC620 but employs a user-supplied temperature sensing device. The most common type of temperature sensor is a negative-temperature-coefficient (NTC) thermistor. An NTC sensor requires that the input and output functions be reversed from that of the TC620. This means that the HIGH SET resistor (pin 2) should always be lower than the LOW SET resistor (pin 3) to insure proper operation. See the applications section of this data sheet for recommendations on selecting the thermistor.

DESIGN PARAMETERS

The designer must be sure that the LOW SET programming resistor is smaller than the HIGH SET programming resistor for the TC620, or that the LOW SET resistor is larger than the HIGH SET resistor when using the TC621 with an NTC external thermistor. No damage will be done to the part if this is not correct, but the CONTROL output logic will be affected.

The LOW LIMIT and HIGH LIMIT outputs will go to a HIGH state (LOW state for TC621) whenever the temperature of the device (or external thermistor) exceeds the temperature programmed for the respective inputs.

The CONTROL output latch will go to a HIGH whenever the sensed temperature exceeds the HIGH SET temperature and will go to a LOW if the sensed temperature drops below the LOW SET temperature. A bonding option may be selected to invert the CONTROL output logic for heating applications. The part number for this option has an 'H' instead of a 'C' placed after the '620' or '621' digits.

If power is applied to the device while the sensed temperature is between the LOW SET temperature and the HIGH SET temperature, the LOW LIMIT output will go HIGH (LOW for the TC621) and the CONTROL output will go HIGH.

The resistance value for the TC620 can be determined by inserting the desired trip temperature (T) into the following formula:

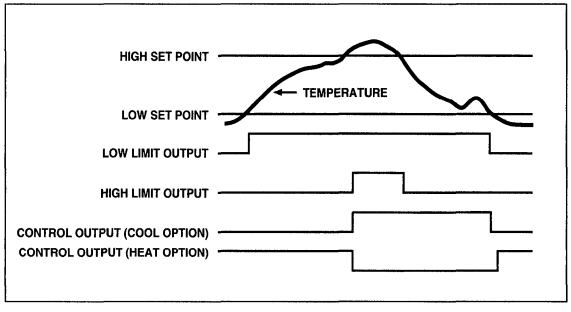
$$R_{TRIP} = 0.5997 \times T^{2.1312}$$

Where Rtrip = Programming resistor value in Ohms
T = Desired trip temperature in degrees Kelvin

For example, to program the device to trip at 50°C, the programming resistor would be:

$$R_{trip} = 0.5997 \times ((50 + 273.15)^{2.1312}) = 133{,}652\ \Omega$$

The TC621 can source or sink 10 mA per output. The outputs of the TC620 can source or sink 1mA. If higher currents are utilized in the TC620, the device will generate internal heat, possibly causing erroneous temperature sensing.

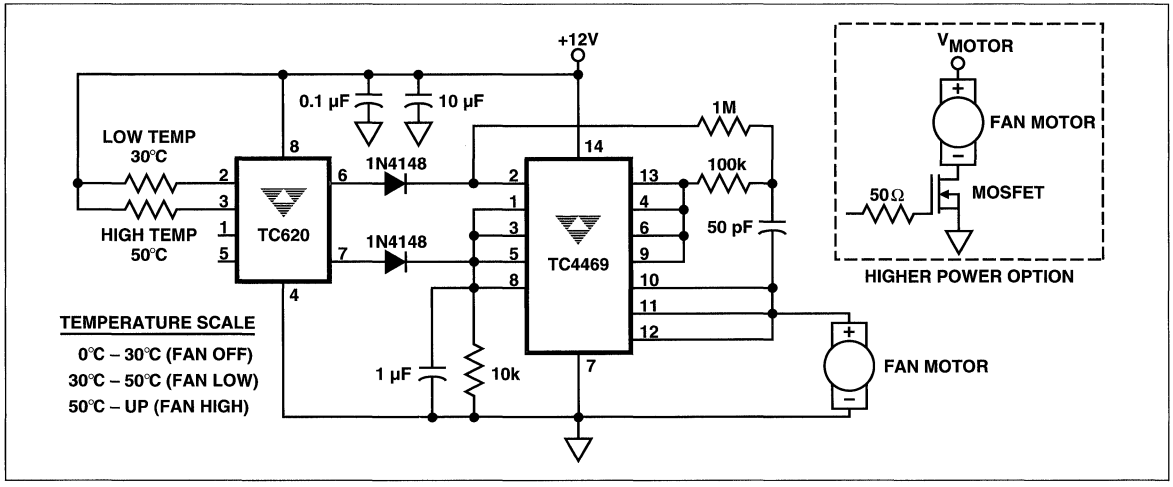


TC620/621 Input vs. Output Logic

TYPICAL APPLICATIONS

Dual Speed Temperature Control

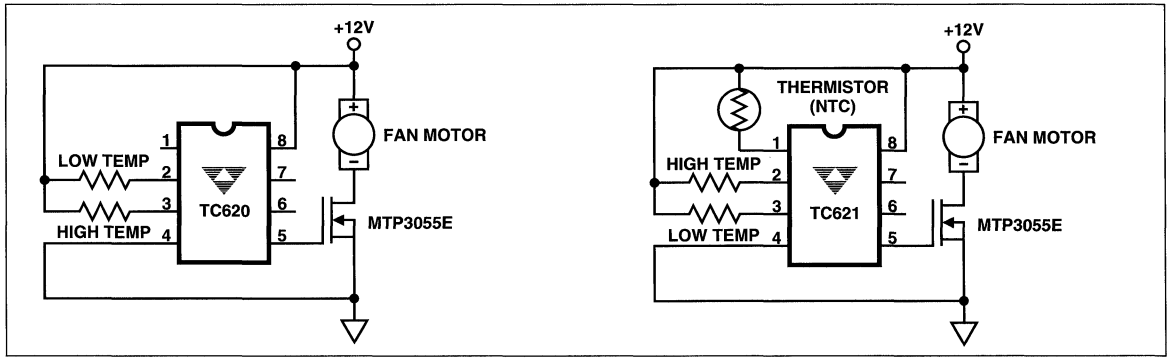
The Dual Speed Temperature Control adds features to the basic controller by using the TC4469 quad driver. Two of the drivers are configured in a simple oscillator. When the temperature is below the LOW TEMP set point, the output of the driver is OFF. When the temperature exceeds the LOW TEMP set point, the TC4469 gates the oscillator signal to the outputs of the driver. This square wave signal modulates the remaining outputs and drives the motor at a low speed. If this speed cannot keep the temperature below the HIGH TEMP set point, then the driver turns on continuously which increases the fan speed to high. The TC620 will monitor the temperature and only allow the fan to operate when needed, and at the required speed to maintain the desired temperature. A higher power option can be designed by adding a resistor and a power MOSFET.



Temperature Controlled Fan

In the Temperature Controlled Fan schematic, a high and a low temperature is selected by two 'set' resistors. The TC620 then monitors the ambient temperature and will turn on the FET switch when the temperature exceeds the HIGH TEMP set point. The fan remains on until the temperature decreases to the LOW TEMP set point. This provides the hysteresis. In this application, the fan will not turn on unless needed. This makes for a high-power fan control with only four parts.

The TC621 uses an external thermistor to monitor the ambient temperature. This adds one part, but allows more flexibility in location of the sensor.



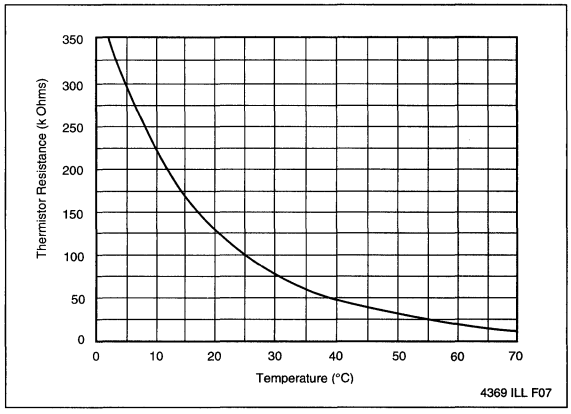
USING THE TC621

The TC621 uses an external thermistor to monitor the controlling temperature. A thermistor with a resistance value of approximately 100kΩ at 25°C is recommended.

Typical thermistors exhibit a negative temperature coefficient (NTC) which must be considered when selecting the set-point resistors. A temperature set-point is selected by picking a resistor whose value is equal to the resistance of the thermistor at the desired temperature.

A 30kΩ resistor between HIGH TEMP (pin 2) and V_{DD} (pin 8) will set the high temperature trip point at +50°C and a 49kΩ resistor on LOW TEMP (pin 3) will set the low temperature trip point to +40°C.

TYPICAL NTC THERMISTOR

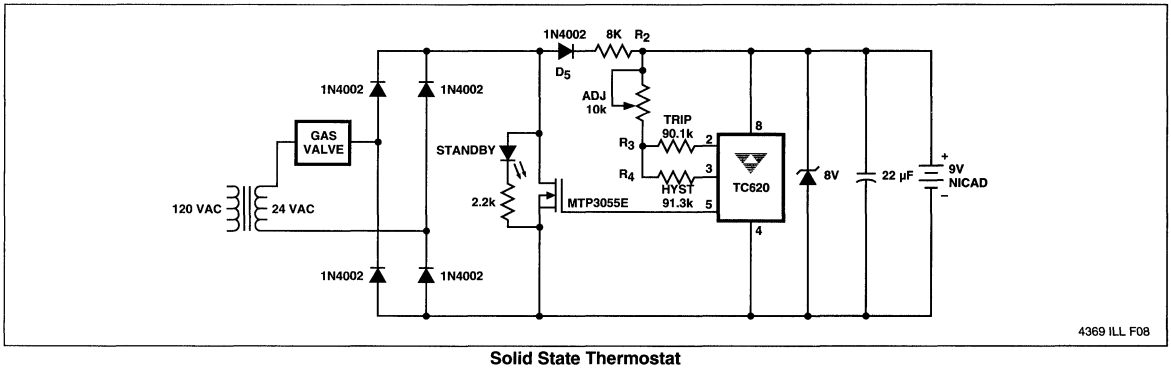


Typical Thermistor Resistance vs Temperature

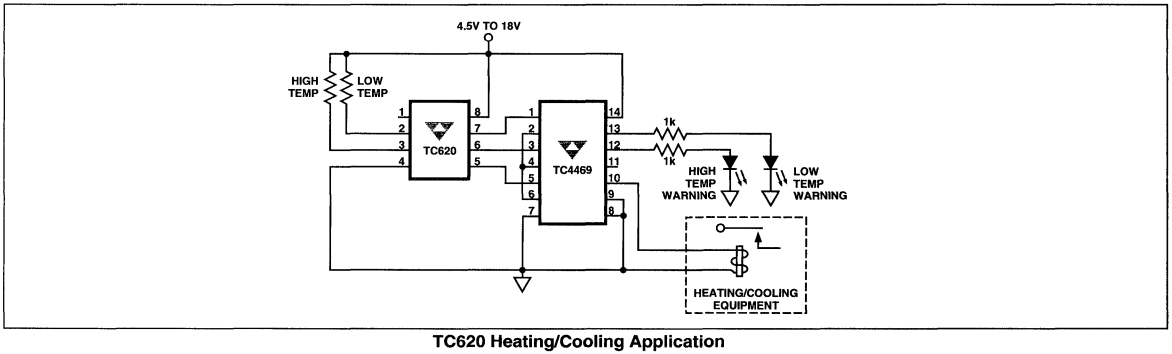
TYPICAL APPLICATIONS

Solid State Thermostat

The Solid State Thermostat diagram shows how the TC620 can be used to control home, industrial and commercial heating and cooling applications in a low cost, simple approach. The TC620 monitors the temperature and when heating is required, turns on the FET switch. This applies power to the gas valve and turns off the "standby" indicator. The NiCad battery provides power to the circuit when the FET is energized. D5 and R2 provide current limited power to the circuit when the FET is off. This also keeps the Nicad battery recharged. R3 and R4 set the desired hysteresis to prevent rapid cycling of the heating or cooling equipment.



Solid State Thermostat



TC620 Heating/Cooling Application

FAST NiCAD/Ni-HYDRIDE BATTERY CHARGER

FEATURES

- Fast Charge Cycle
- Automatic Overcharge Protection
- Fail Safe Fast Charge Shut-Off
- Programmable Min/Max Ambient Limits
- Selectable Charge Rate
- Automatic Trickle Charge
- Timed Fast-Charge Mode with Switchable Trickle Mode (TC675)
- Auto Trickle Charge Mode with Switchable Timed Fast-Charge (TC676)
- Safety Features
- Temperature Controlled Shut-Off
- Time Controlled Shut-Off
- Dual Mode Automatic Shut-Off
- Automatic Battery Insertion Detector

APPLICATIONS

- Battery Powered Applications
  - —Power Tools
  - —Laptop/Notebook Computers
  - —Medical
  - —Emergency Lighting Systems
  - —Communications
  - —Cellular Phones/Mobile Radio
  - —Portable Instruments

GENERAL DESCRIPTION

The TC675 and TC676 are designed for use with both NiCad and Ni-Hydride batteries. These two devices meet the needs of the system designer whose battery charge applications require fast, reliable, and safe design.

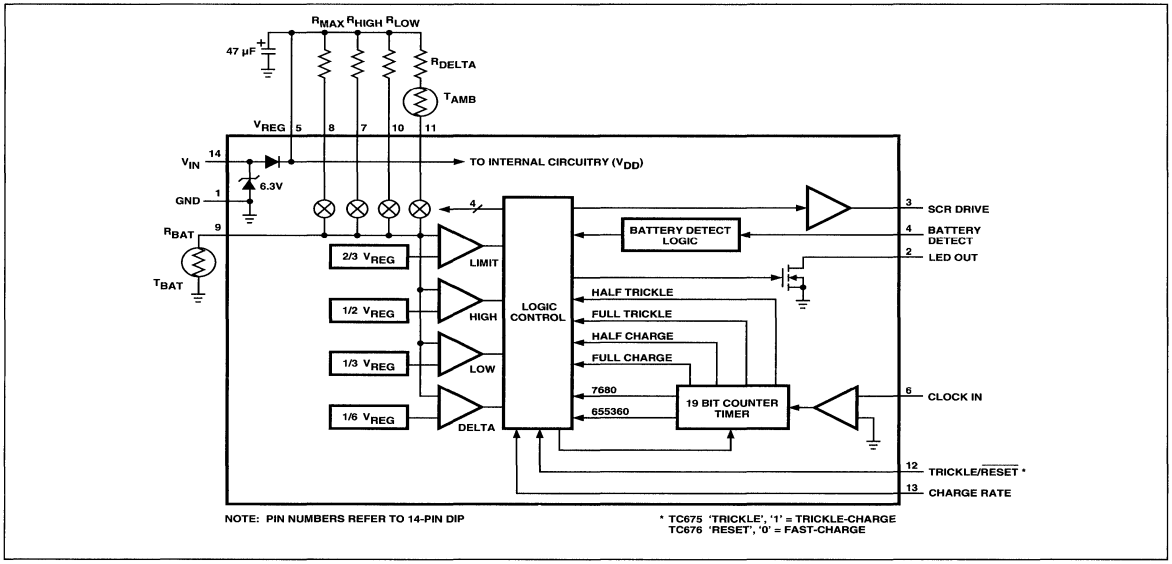
The many automatic, programmable and selectable features of these devices provide capabilities found only in more expensive implementations. These, combined with their capability of use in both AC or DC power sources, provide a flexible, cost-effective solution to battery recharge *maintenance.*

ORDERING INFORMATION

Part No.	Operating Package	Temp Range
TC675CPD	14-Pin Plastic DIP	0°C to +70°C
TC675EPD	14-Pin Plastic DIP	– 40°C to +85°C
TC675MJD	14-Pin Ceramic DIP	– 55°C to +125°C
TC676CPD	14-Pin Plastic DIP	0°C to +70°C
TC676EPD	14-Pin Plastic DIP	– 40°C to +85°C
TC676MJD	14-Pin Ceramic DIP	– 55°C to +125°C

4

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Dissipation
- Plastic ..... 1000 mW
- Ceramic ..... 800 mW

Derating Factors
- Plastic ..... 8 mW/°C
- Ceramic ..... 6.4 mW/°C

Operating Temperature
- M Version ..... – 55°C to +125°C
- E Version ..... – 40°C to +85°C
- C Version ..... 0°C to +70°C

Storage Temperature ..... – 65°C to +150°C
Lead Temperature (10 sec) ..... +300°C
Max Zener Current (I_{IN}) ..... 50 mA

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Operational Specifications is not implied. Any exposure to Absolute Maximum Rating Conditions may affect device reliability.

OPERATIONAL SPECIFICATIONS: unless otherwise specified T_A = +25°C; I_S = 6 mA.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply						
I_S	Supply Current (	thru current limit resistor)	1	6	30	mA
V_Z	Zener Clamp Voltage	I_Z = 6 mA	6	6.3	7	V
R_Z	Zener Output Resistance	I_Z = 10 mA to 30 mA	—	10	20	Ω
V_{DD}	DC Input on	V_{REG} V_{IN} Open	4	5	6	V
I_{DD}	Internal Circuit Current	V_{DD} (V_{REG}) = 5V	—	0.3	1	mA
Regulator						
V_{REG}	Regulated Output	I_{REG} = 5 mA	5	—	6	V
R_{REG} V_{REG}	Output Resistance	-I_{REG} = 0 mA to 5 mA	—	38	45	Ω
Switch Resistance (r_{DS} ON)						
RSW_{MAX}	MAX Switch		—	—	200	Ω
RSW_{HIGH}	HIGH Switch		—	—	450	Ω
RSW_{LOW}	LOW Switch		—	—	350	Ω
RSW_{DELTA}	DELTA Switch		—	—	300	Ω
RSW_{LED}	LED Drive		—	—	80	Ω
Threshold Voltage Tolerance						
δV_{MAX}MAX		2/3 V_{REG}	—	±4	±10	%
δV_{HIGH}	HIGH	1/2 V_{REG}	—	±4	±10	%
δV_{LOW}	LOW	1/3 V_{REG}	—	±4	±10	%
δV_{DELTA}	DELTA	1/6 V_{REG}	—	±4	±10	%
TCδV	Threshold Voltage Temp Coefficient		—	±0.01	±0.1	%/°C

OPERATIONAL SPECIFICATIONS (Cont): unless otherwise specified T_A = +25°C; I_S = 6 mA.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Output						
$I_{OH}G$	SCR Gate Drive Source		—	5	—	mA
$I_{OL}G$	SCR Gate Drive Sink		—	3	—	mA
$V_{OL}L$	LED Low Output Voltage	$I_{OL}L$ = 10 mA	—	—	0.8	V
Digital Input						
$I_{IL}CR$	CHARGE RATE Pull-up Current		—	—	10	µA
$I_{IH}TR$	TRICKLE/$\overline{\text{RESET}}$ Pull-down Current		—	—	25	µA
$I_{IL}BD$	BATTERY DETECT Pull-up Current		—	—	20	µA

ELECTRICAL CHARACTERISTICS: unless otherwise specified T_A = Operating Temperature Range; I_S = 6 mA.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply						
I_S	Supply Current	(thru current limit resistor)	1.2	6	30	mA
V_Z	Zener Clamp Voltage	I_Z = 6 mA	5.5	—	7.5	V
R_Z	Zener Output Resistance	I_Z = 10 mA to 30 mA	—	—	25	Ω
V_{DD}	DC Input on $V_{REG}V_{IN}$ Open		4	5	6	V
I_{DD}	Internal Circuit Current	V_{DD} ($V_{R\ EG}$) = 5V	—	0.5	1.2	mA
Regulator						
V_{REG}	Regulated Output	I_{REG} = 0 mA to 5 mA	4.8	—	7	V
R_{REG}	V_{REG} Output Resistance	I_{REG} = 5 mA	—	45	60	Ω
Switch Resistance (r_{DS} ON)						
RSW_{MAX}	MAX Switch		—	—	260	Ω
RSW_{HIGH}	HIGH Switch		—	—	510	Ω
RSW_{LOW}	LOW Switch		—	—	410	Ω
RSW_{DELTA}	DELTA Switch		—	—	360	Ω
RSW_{LED}	LED Drive		—	—	100	Ω
Threshold Voltage Tolerance						
δV_{MAX}	MAX	2/3 V_{REG}	—	—	±10	%
δV_{HIGH}	HIGH	1/2 V_{REG}	—	—	±10	%
δV_{LOW}	LOW	1/3 V_{REG}	—	—	±10	%
δV_{DELTA}	DELTA	1/6 V_{REG}	—	—	±10	%
$TC\delta V$	Threshold Voltage Temp Coefficient		—	—	0.1	%/°C
Output						
$I_{OH}G$	SCR Gate Drive Source		—	5	—	mA
$I_{OL}G$	SCR Gate Drive Sink		—	3	—	mA
$V_{OL}L$	LED Low Output Voltage	$I_{OL}L$ = 10 mA	—	—	1	V
Digital Input						
$I_{IL}CR$	CHARGE RATE Pull-up Current		—	—	15	µA
$I_{IH}TR$	TRICKLE/$\overline{\text{RESET}}$ Pull-down Current		—	—	35	µA
$I_{IL}BD$	BATTERY DETECT Pull-up Current		—	—	25	µA

TIMER-COUNTER

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Charge Time Counter	(1.517 Hr @ 120 Hz)	—	655360	—	Counts
	Delay Time Counter	(1.07 Min @ 120 Hz)	—	7680	—	Counts

DEVICE OPERATION

(All pin numbers refer to the 14-pin dip package)

Temperature Control

Safety is critical in charging NiCad/Ni-Hydride batteries because a fast-charge applied under the wrong conditions may cause severe damage to the battery and it's surroundings. In circuits using the TC675/676, the battery temperature is monitored by an external thermistor, and the controller will not allow the battery to start a fast-charge cycle while the battery temperature is too hot or too cold. A NiCad/Ni-Hydride battery tends to warm up during a fast-charge cycle, so a temperature that was too high to allow the charging to start may not be too high to allow the charging to continue. Therefore, another temperature threshold causes the charger to stop the fast-charge cycle as soon as the battery temperature gets too high.

A charger may also be required to work in cold ambient temperatures. The preprogrammed absolute maximum charging temperature may be too high for these conditions so a separate 'delta' temperature may be used. This will stop the fast-charge cycle if the battery temperature exceeds the ambient temperature by a predetermined amount. This option requires a second thermistor to monitor the ambient temperature.

Time Control

The TC675 and TC676 both use an on-board timer-counter which limits the maximum duration of the fast-charge cycle to 1.5 hours (1.8 hrs @ 50 Hz AC power). There is also a time delay of 60 seconds (or 77 sec if using 50 Hz AC power) before starting a fast-charge cycle. This delay gives the battery temperature sensor time to stabilize.

The counters are clocked by the full-wave rectified AC input. This clock rate is divided by 655,360 to time out the 1.517 hour (1.82 hrs @ 50 Hz AC power) maximum for the fast-charge cycle. A faster or slower clock may be used to modify the timing (pin 6).

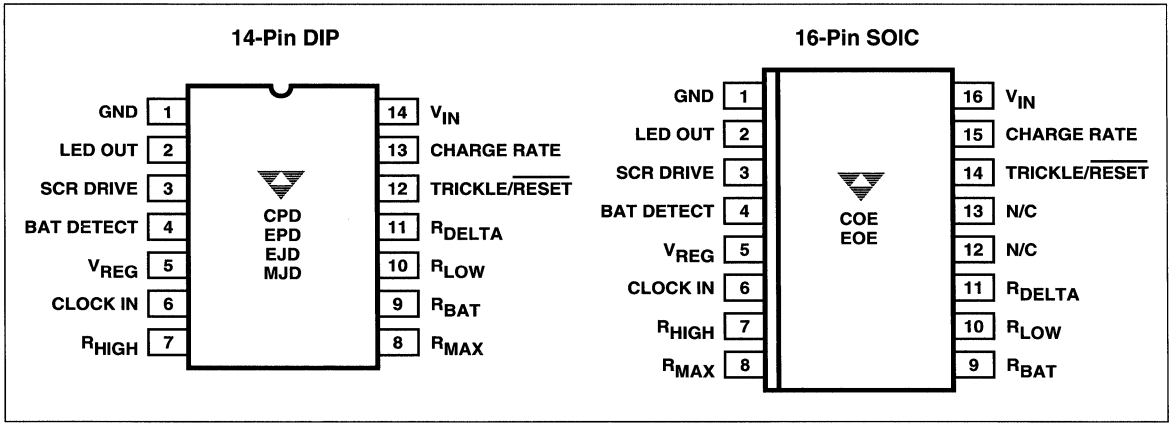
Full-Charge or Half-Charge Option

Both the TC675 and TC676 have a half-charge selection option. The CHARGE RATE input has an internal pull-up to select the full-charge mode (7/8 duty cycle). A LOW on this pin will select the half-charge mode (7/16 duty cycle). This input may be selected or toggled at anytime during a fast-charge cycle without affecting the time-out sequence. NOTE: "full-charge" is the same as "fast-charge".

Trickle-Charge

The trickle-charge mode of the TC675 and the TC676 runs at ≈7% of the fast-charge mode (1/16 duty cycle for full-charge and 1/32 duty cycle for half-charge), and is the default mode whenever the fast-charge cycle is not running.

PIN CONFIGURATIONS



TRICKLE/RESET (PIN 12)

The only difference between the TC675 and the TC676 is the operation of the input on pin 12.

On the TC675 (pin 12 = 'TRICKLE'), a HIGH (V_{DD}) on this pin will hold the charger in the trickle-charge mode. The internal timer will continue to count down. If the timer hasn't timed out, the charger will go back to the full-charge mode if this pin is returned to LOW (0V).

On the TC676 (pin 12 = 'RESET'), a LOW transition (V_{DD} to 0V) on this pin will reset the timer and initiate a fast-charge cycle.

BATTERY SENSE (PIN 4)

This input is internally pulled up to about 1 volt. It is designed to be capacitively coupled to the cathode of the SCR (the positive terminal of the battery). Without a battery present, the pulses from the full-wave rectified AC signal are coupled by a bypass resistor around the SCR into the battery input through the capacitor. This produces a zero-crossing waveform at the battery pin which is interpreted as a "no battery" condition. The presence of a battery will prevent these zero-crossings and the TC675/TC676 can begin a charge sequence.

Some battery packs contain a diode in series with the cells for safety purposes. This diode may prevent the battery from clamping the waveform to prevent zero-crossings. The auxiliary detect circuitry should be added to cause the diode, if present, to forward bias, which will then clamp the waveform to prevent zero-crossings and will indicate the presence of the battery (see page 7).

CLOCK IN (PIN 6)

This input accepts the rectified AC signal and uses its pulses to establish timing. The waveform must reach zero volts during the pulse OFF time for accurate timing. Noise on this line could cause false clock triggering, which can be prevented by placing a 0.01 µF capacitor from pin 6 to ground. This input is internally clamped to the V_{DD} (V_{IN}) potential (≈6V). A current limiting resistor must be used to connect the rectified AC signal.

SCR DRIVE (PIN 3)

A 1.5 kHz pulse is the output on this pin which turns on the SCR during each cycle of the rectified AC waveform. This signal should be capacitively coupled to the gate of the SCR. A 0.01 µF capacitor will effectively turn on the SCR and block any DC component.

CHARGE RATE (PIN 13)

This input has an internal pull-up which selects the normal-charge mode as default. A LOW on this pin will select 1/2 the current charge rate, i. e. if the charger is in full-charge mode, then a LOW on pin 13 will select 1/2 full-charge: if the charger is in trickle-charge mode, then 1/2 trickle-charge is selected.

LED OUTPUT (PIN 2)

This pin has a pull-down resistor to ground. With power applied and no battery installed, and during the 1 minute start delay, the transistor is ON. The output will toggle at a 3 Hz rate during a fast-charge cycle. The output will stay ON steady during the trickle-charge mode.

CONTROL TEMPERATURE

Each control temperature has a unique voltage threshold which is derived as a ratio of an internal, zener generated reference voltage (V_{REG}).

T_{MAX} ($\delta V_{MAX} = 2/3\ V_{REG}$)
the charger will stop the fast-charge mode if the battery temperature reaches this value.

T_{HIGH} ($\delta V_{HIGH} = 1/2\ V_{REG}$)
the charger will not start the fast-charge mode if the battery temperature is above this value.

T_{LOW} ($\delta V_{LOW} = 1/3\ V_{REG}$)
the charger will not start the fast-charge mode if the battery temperature is below this value.

T_{DELTA} ($\delta V_{DELTA} = 1/6\ V_{REG}$)
the charger will stop the fast-charge mode if the battery temperature exceeds the ambient temperature by this value.

THERMISTOR TEMPERATURE SENSOR

A common type of thermistor for this application is a negative-temperature-coefficient (NTC) with a relatively high resistance ratio. Some examples of this type are KC009-ND, KC020-ND or RL1006-53 from Keystone.

Thermistor Characteristics

The transfer function (Resistance vs. Temperature) of a normal NTC thermistor takes the form:

$\ln R_T = A_0 + A_1/T + A_2/T^2 = \ldots + A_N/T^N$ (T in °Kelvin)

The first three terms of this equation are sufficient to give a fit of better than ±0.01°C. The coefficients may be determined by setting up 3 simultaneous equations based on 3 known points.

The following calculations are based on a typical NTC thermistor (Keystone RL1006-53.4K-140-D1) with resistance values of 48.15 kΩ at 40°C (313.15°K), 100 kΩ at 25°C (298.15 K) and 221.8 kΩ at 10°C (282.15°K).

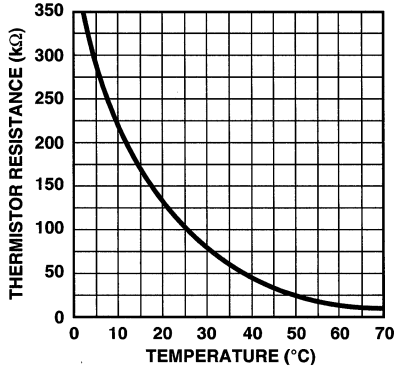
1st point:
ln (48150) $= A_0 + A_1/313.15 + A_2/313.152$

2nd point:
ln (100000) $= A_0 + A_1/298.15 + A_2/298.152$

3rd point:
ln (221800) $= A_0 + A_1/283.15 + A_2/283.152$

Solving these three equations for A_0, A_1 and A_2 yields:

$$R_T = \ln^{-1}(-5.825 + 5821/T - 194235/T^2)$$



SETTING UP THE CONTROL TEMPERATURES

Assume an application which requires that the battery charger not start while the battery temperature is below 20°C (T_{LOW}) or above 30°C (T_{HIGH}). Also assume that the battery should stop charging if its temperature gets up to either 40°C (T_{MAX}) or 20°C (T_{DELTA}) above an ambient temperature of 15°C (T_{AMB}).

The control temperatures are programmed as a function of the resistance value of the battery temperature thermistor ($R_{BAT}T$) when it is at the temperature to be programmed (T) and the threshold voltage ratio (δV_X).

The form of the equation to determine the values of R_{LOW}, R_{HIGH} and R_{MAX} is as follows:

$$R_X = \frac{R_{BAT}T}{\delta V_X} - R_{BAT}T$$

where $R_{BAT}T$ is the resistance of the battery thermistor at temperature T connected to pin 9.

R_{MAX} (pin 8):
$T_{MAX} = 40°C$, $\delta V_{MAX} = 2/3$, $R_{BAT}40 = 48.1k$,

$$R_{MAX} = \frac{R_{BAT}40}{\delta V_{MAX}} - R_{BAT}40 = \frac{48.1k}{2/3} - 48.1k = 24k$$

R_{HIGH} (pin 7):
$T_{HIGH} = 30°C$, $\delta V_{HIGH} = 1/2$, $R_{BAT}30 = 77.8k$,

$$R_{HIGH} = \frac{R_{BAT}30}{\delta V_{HIGH}} - R_{BAT}30 = \frac{77.8k}{1/2} - 77.8k = 77.8k$$

R_{LOW} (pin 10):
$T_{LOW} = 20°C$, $\delta V_{LOW} = 1/3$, $R_{BAT}20 = 129.4k$,

$$R_{LOW} = \frac{R_{BAT}20}{\delta V_{LOW}} - R_{BAT}20 = \frac{129.4k}{1/3} - 129.4k = 268.8k$$

R_{DELTA} (PIN 11)

A second thermistor can be used to modify the battery temperature shutdown point as a function of the ambient temperature. A 'delta' temperature may be set up to limit the battery temperature to some value above ambient. This value is called T_{DELTA} and the ambient temperature that it works against is called T_{AMB}.

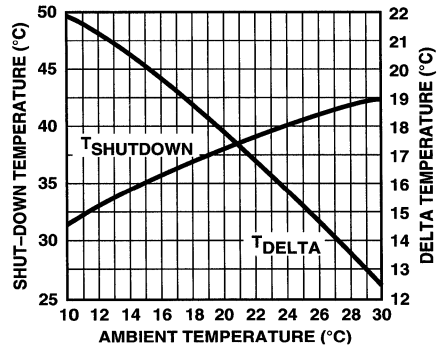
This control is very important for applications which are required to work over a wide range of ambient temperatures. Once a T_{DELTA} value has been set up to work at some T_{AMB} then the T_{DELTA} will change in inverse proportion to T_{AMB}. This means that as the ambient temperature goes up, the trip point goes up at a decreasing rate, because T_{DELTA} gets smaller.

The form of the equation to determine the values of R_{DELTA} is different from the ones for the other temperature control resistors because two thermistors are used. If the same thermistor type is used for monitoring the ambient temperature as is used to monitor the battery temperature, then the value of R_{DELTA}, based on the above example, is calculated thus:

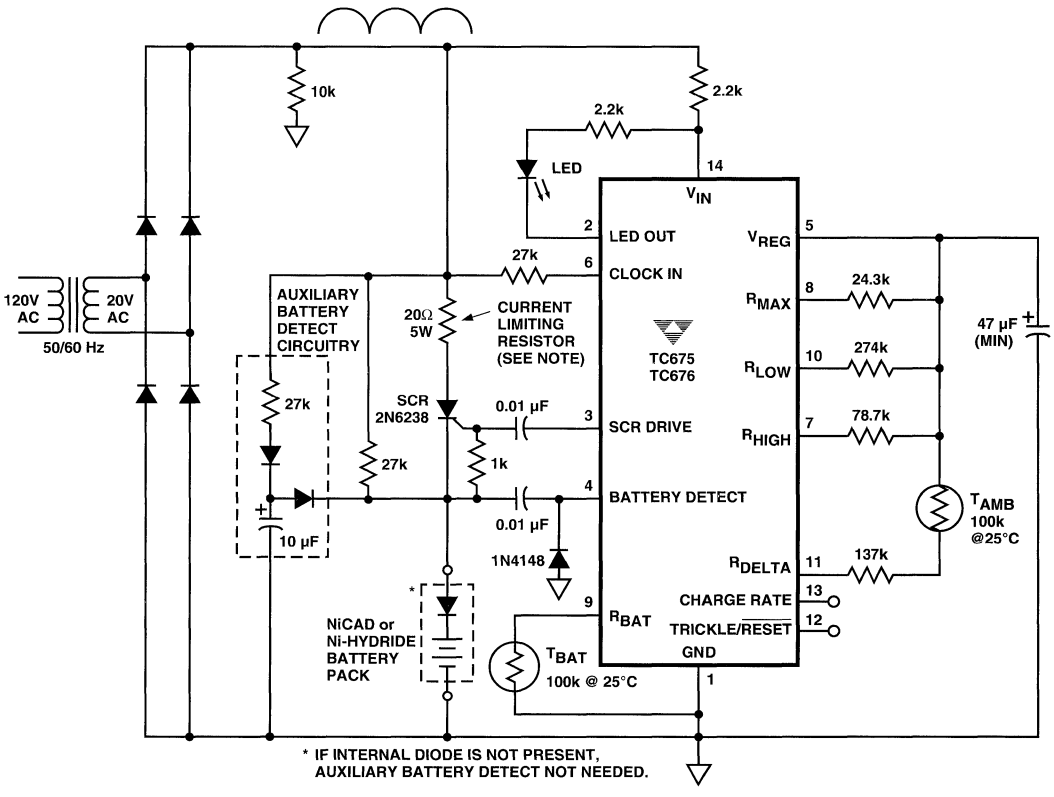
$T_{DELTA} = 20°C$, $T_{AMB} = 15°C$,
$T_{BAT} = T_{AMB} + T_{DELTA} = 35°C$, $\delta V_{DELTA} = 1/6$,

$$R_{DELTA} = \frac{R_{BAT}35}{\delta V_{DELTA}} - R_{BAT}35 - R_{AMB}15 =$$

$$\frac{61k}{1/6} - 61k - 168.7k = 197.3k$$



TYPICAL APPLICATION



IMPORTANT NOTE: THE TC675 AND TC676 WILL MONITOR THE CHARGE TIME AND THE BATTERY TEMPERATURE BUT DO NOT CONTROL THE CHARGING CURRENT. THE DESIGNER MUST LIMIT THE CHARGING CURRENT BASED ON THE APPROPRIATE RATE FOR THE TYPE AND NUMBER OF CELLS IN THE NiCAD/Ni-HYDRIDE BATTERY TO BE CHARGED. EXCEEDING THE BATTERY MANUFACTURER'S MAXIMUM CHARGING CURRENT CAN RESULT IN DEGRADED PERFORMANCE OR EVEN CATASTROPHIC FAILURE.
CHARGING CURRENT CAN BE LIMITED WITH A RESISTOR, AS SHOWN, OR BY MATCHING THE MAXIMUM TRANSFORMER OUTPUT CURRENT TO THE BATTERY CHARGING RATE.

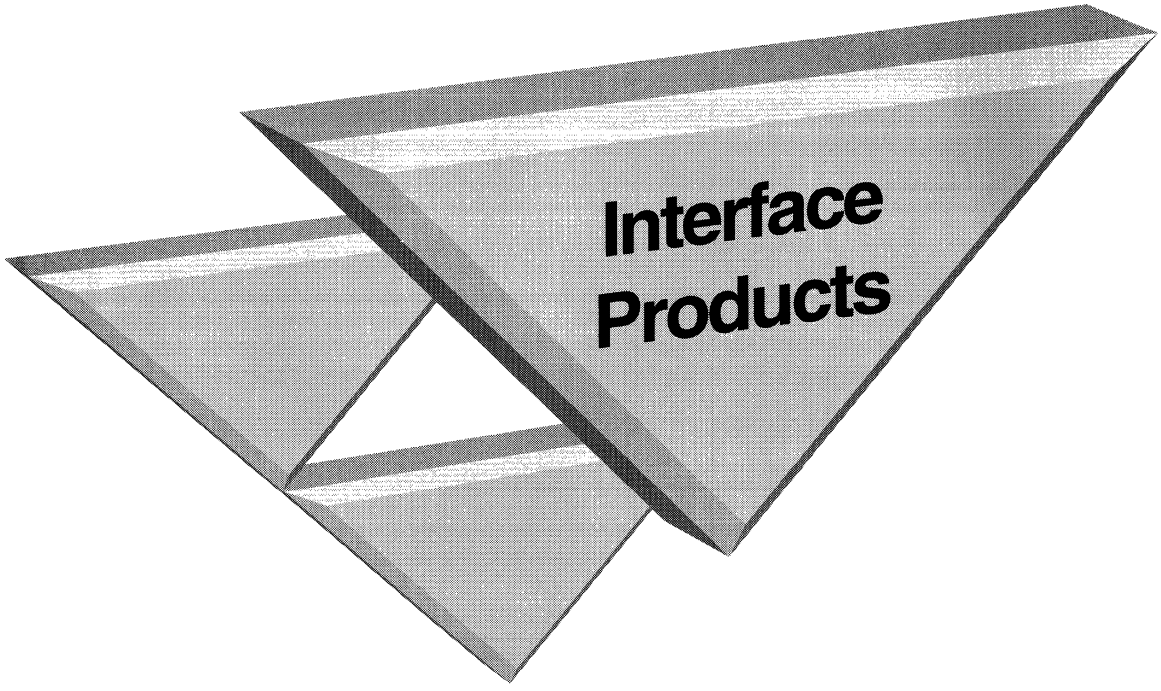
CHARGING NiCAD BATTERIES FROM A DC SOURCE

The TC675 and TC676 are designed to control the charging of NiCad/Ni-Hydride batteries from a self-clocking, self-commutating power source (full-wave rectified, unfiltered 50/60 Hz AC power). However, some applications may require that the NiCad be charged from a DC power source, i. e. battery-to-battery.

When a DC power source is used, the application must provide a clock pulse to CLOCK IN (pin 6) to control the timing, and a pulse train to the BATTERY DETECT (pin 4) whenever a battery is NOT present. This pulse train should be modified by the presence of a battery such that it does not provide zero-crossings on pin 6.

A SET/RESET latch may be controlled by the SCR DRIVE output (pin 3) and the timing clock (pin 6) which can then mediate the charge current to the battery.

DC voltage may be supplied directly to the internal circuitry through pin 5. Under these conditions, V_{REG} becomes V_{DD} and must be at least 4 volts and no greater than 6 volts. The internal circuitry will take about 300 µA (1 mA max) and the V_{IN} input (pin 14) should be left open.



- Data Communication
- Display Drivers

5

DATA COMMUNICATIONS

RS232
DRIVERS/RECEIVERS

TC232

LCD DISPLAY DRIVERS

TC7211A
TC7211AM

DUAL RS-232 TRANSMITTER/RECEIVER AND POWER SUPPLY

FEATURES

- **Meets All RS-232 Specifications**
- **Operates From Single 5V Power Supply**
- **2 Drivers and 2 Receivers**
- **On-Board Voltage Quadrupler**
- **Input Levels ..... ±30V**
- **Output Swing With +5V Supply ..... ±9V**
- **Low Supply Current ..... 5 mA**
- **Does not require external ±12V supplies**

APPLICATIONS

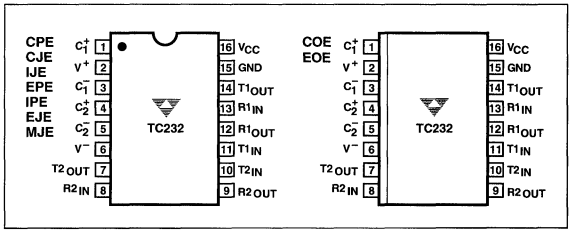
- **RS-232C Communication Links**
- **Modems, peripherals, computers**
- **Battery-powered systems**

GENERAL DESCRIPTION

The TC232 is a dual RS-232 transmitter/receiver that complies with EIA /TIA RS-232E guidelines and is ideal for all RS-232 communication links. This device operates from a 5V power supply and contains two charge pump voltage converters that produce ±10V power supplies.

The TC232 has four level translators. Two are RS-232 transmitters that convert TTL/CMOS input levels to 9V RS-232 outputs. The other two translators are RS-232 receivers that convert RS-232 inputs to 5V TTL/CMOS output levels. The receivers have a nominal threshold of 1.3V, a typical hysteresis of 0.5V, and can operate with inputs up to ±30V.

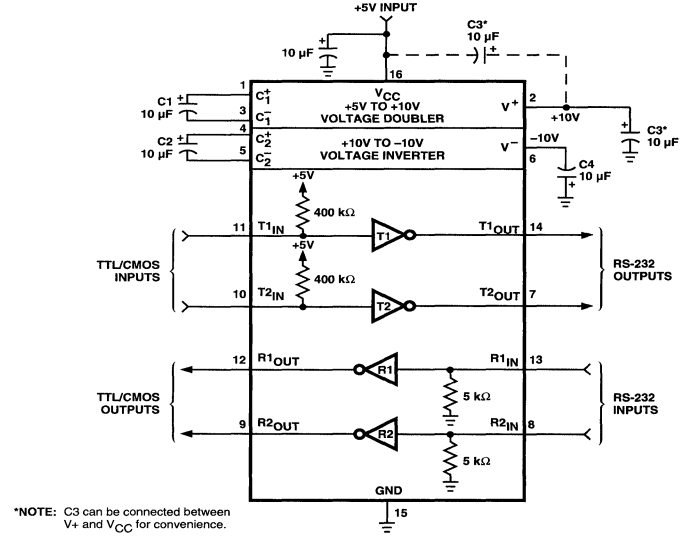
PIN CONFIGURATIONS



ORDERING INFORMATION

Part No.	Package	Temperature Range
TC232CPE	16-Pin Plastic	0°C to +70°C
TC232IJE	16-Pin CerDIP	– 25°C to +85°C
TC232EPE	16-Pin Plastic	– 40°C to +85°C
TC232COE	16-Pin SO	0°C to +70°C
TC232EOE	16-Pin SO	– 40°C to +85°C
TC232MJE	16-Pin CerDIP	– 55°C to +125°C

TYPICAL APPLICATION



*NOTE: C3 can be connected between V+ and V_{CC} for convenience.

5

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... +6V
V^+ ..... +12V
V^- ..... +12V
Input Voltages
$T1_{IN}$, $T2_{IN}$ .....–0.3 to (V_{CC} +0.3V)
$R1_{IN}$, $R2_{IN}$ ..... ±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ ..... (V^+ +0.3V) to (V^- –0.3V)
$R1_{OUT}$, $R2_{OUT}$ ..... –0.3 to (V_{CC} +0.3V)
Short Circuit Duration
V^+ ..... 30 sec
V^- ..... 30 sec
$T1_{OUT}$, $T2_{OUT}$ ..... Continuous

Storage Temperature Range ..... -65°C to +150°C
Power Dissipation
CerDIP ..... 675 mW
Derate 9.5 mW/°C Above +70°C
Plastic DIP ..... 375 mW
Derate 7 mW/°C Above +70°C
Small Outline (SO) ..... 375 mW
Derate 7 mW/°C Above +70°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

V_{CC} = 5V ±10%, T_A = operating temperature range, test circuit unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Voltage Swing	$T1_{OUT}$, $T2_{OUT}$ Loaded With 3 kΩ to Ground	±5	±9	±10	V
Power Supply Current			5	10	mA
Input Logic Threshold Low	$T1_{IN}$, $T2_{IN}$			0.8	V
Input Logic Threshold High	$T1_{IN}$, $T2_{IN}$	2			V
Logic Pull-Up Current	$T1_{IN}$, $T2_{IN}$ = 0V		15	200	µA
RS-232 Input Voltage Operating Range		– 30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V	0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V		1.7	2.4	V
RS-232 Input Hysteresis		0.2	0.5	1	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V	3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2 mA			0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = – 1 mA	3.5			V
Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5		µs
Instantaneous Slew Rate	C_L = 10 pF, R_L = 3 kΩ to 7 kΩ, T_A = +25°C (Note 1)			30	V/µs
Transition Region Slew Rate	R_L = 3 kΩ, C_L = 2500 pF Measured From +3V to – 3V or –3V to +3V		3		V/µs
Output Resistance	V_{CC} = V^+ = V^- = 0V, V_{OUT} = ±2V	300			Ω
RS-232 Output Short-Circuit Current			±10		mA

NOTE 1. Sample tested.

DETAILED DESCRIPTION

The TC232 contains a +5V to ±10V dual charge pump voltage converter, a dual transmitter and a dual receiver.

+5V to ±10V Dual Charge Pump Voltage Converter

The TC232 power supply consists of two charge pumps. One uses external capacitor C1 to double the +5V input to +10V, with output impedance of about 200Ω. The other uses C2 to invert +10V to – 10V, with overall output impedance of 450Ω (including effects of +5V to +10V doubler impedance).

The clock in the doubler circuit will start at ≈4.2V in the typical part, but external loads may make this point rise to as high as 4.5V with a load of 2 kΩ on each of the two output voltages.

Because of this, use of the doubler and inverter to run additional external circuits should be limited. The maximum current should be no more than 2.5 mA from the +10V and - 10V. in order to guarantee start-up of the doubler clock.

The test circuit employs 22 µF capacitors for C1 to C4, but the value is not critical. These capacitors usually are low-cost aluminum or tantalum electrolytic capacitors.

Increasing C1 and C2 to 47 µF lowers the output impedance of the +10V doubler and the - 10V inverter by the change in the ESR of the capacitors.

Increasing C3 and C4 lowers ripple on the ±10V outputs and 16 kHz ripple on the RS-232 outputs. Where size is critical, the value of C1 to C4 can be lowered to 1 µF. The use of a low ESR capacitor will help lower the output ripple and keep the output impedance of the ±10V as low as possible.

Dual Transmitter

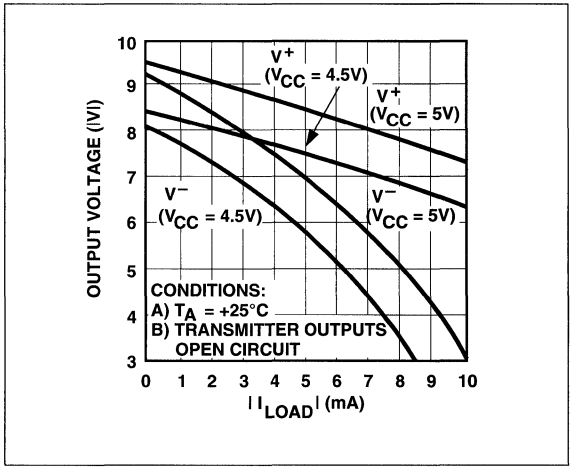
TC232 transmitters are CMOS inverters driven by ±10V internally-generated voltages. The input is TTL/CMOS compatible, with a logic threshold of about 26% of V_{CC} (1.3V for 5V V_{CC}). The input of an unused transmitter can be left unconnected, since an internal 400 kΩ pull-up resistor connected between the transmitter input and V_{CC} pulls the input HIGH and forces the unused transmitter output to the LOW state.

With V_{CC} at 5V, the outputs will go from (V+ – 0.6V) to V^- with no load and will swing ±9V when loaded with 3 kΩ. The minimum output voltage swing, with V_{CC} at 4.5V and at maximum ambient temperature, is ±5V. This conforms to RS-232 specifications for "worst-case" conditions.

EIA/TIA RS-232E specs limit the slew rate at output to less than 30V/µs.

The powered-down output impedance (V_{CC} = 0V) is a minimum of 300Ω with ±2V applied to outputs.

V^+, V^- Output Voltages vs Load Current



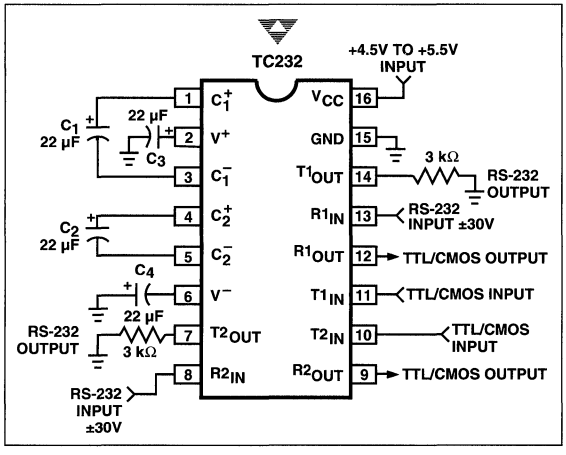
The outputs are protected and can be short-circuited to ground indefinitely.

Dual Receiver

TC232 receivers meet RS-232 input specifications. Input impedance is between 3 kΩ and 7 kΩ. Switching thresholds are within the ±3V limits, and the receivers withstand up to ±30V inputs. RS-232 and TTL/CMOS input compatible, the receivers have 0.8V V_{IL} and 2.4V V_{IH} with 0.5V hysteresis to reject noise.

The TTL/CMOS compatible receiver output is LOW when an RS-232 input is greater than 2.4V. It is HIGH when an input is floating or between +0.8V and – 30V.

TEST CIRCUIT



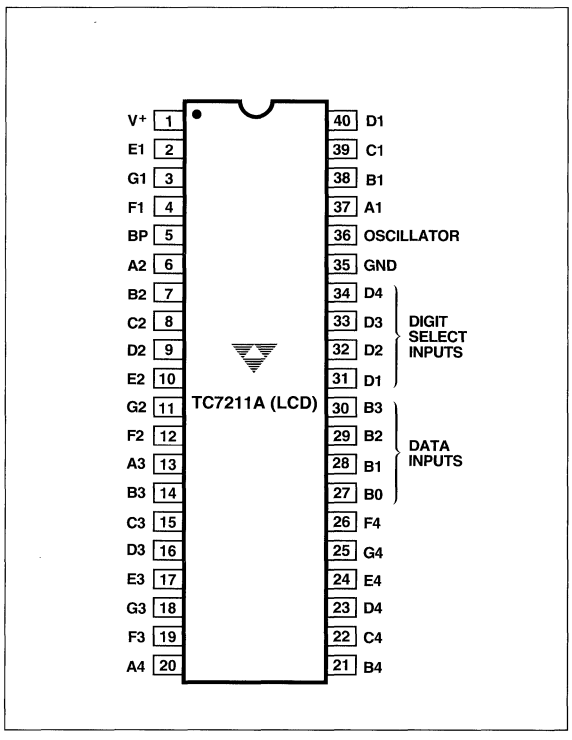
5

4-DIGIT CMOS DISPLAY DECODER/DRIVER

FEATURES

- **4-Digit Nonmultiplexed, 7-Segment LCD Outputs With Backplane Driver**
- **RC Oscillator On Chip Generates Backplane Drive Signal**
- **Eliminates DC Bias Which Degrades LCD Life**
- **Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal**
- **Separate Digit Select Inputs to Accept Multiplexed BCD/Binary Inputs**
- **Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)**
- **Pin Compatible and Functionally Equivalent to ICM7211A and DF411**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC7211A is a direct drive, 4-digit, 7-segment display decoder and driver.

The TC7211A drives conventional LCDs. An RC oscillator, divider chain, backplane driver, and 28-segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane, but in-phase for an OFF segment and out-of-phase for an ON segment. The net DC voltage applied between driver segment and backplane is zero.

The TC7211A requires only 4 data bit inputs and 4 digit select signals to interface with multiplexed BCD or binary output devices (such as the ICM7217, ICM7226, ICL7103 and TC7135). The 4-bit binary input is decoded into the 7-segment alphanumeric code known as "Code B."

The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the 7-segment display format.

The CMOS TC7211A is available in a 40-pin epoxy dual-in-line package . All inputs are protected against static discharge.

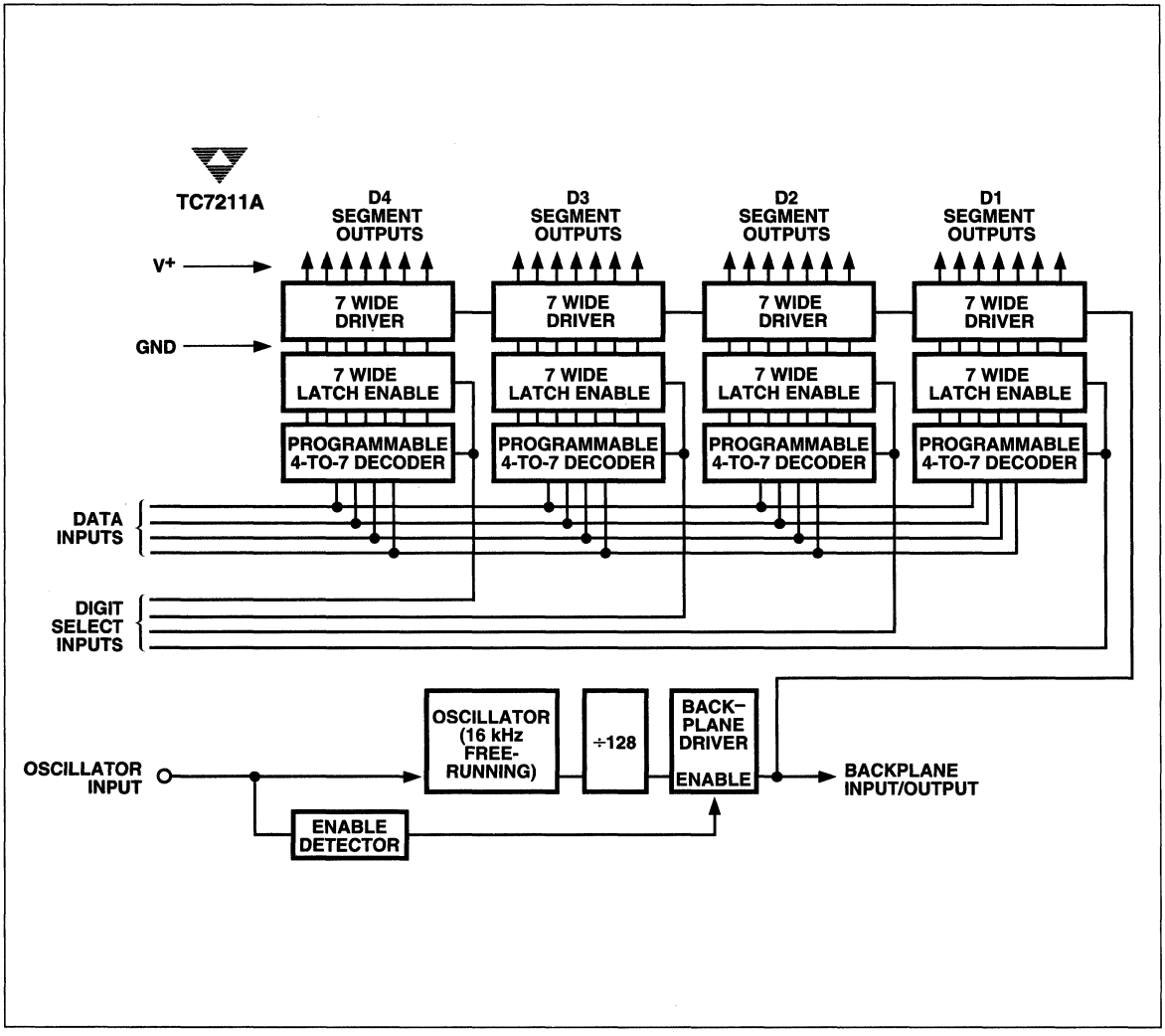
ORDERING INFORMATION

Part No.	Driver Type	Package	Output Code	Input Config.
TC7211AIPL	LCD	40-Pin Plastic DIP	Code B	Multiplexed 4-bit Binary or BCD

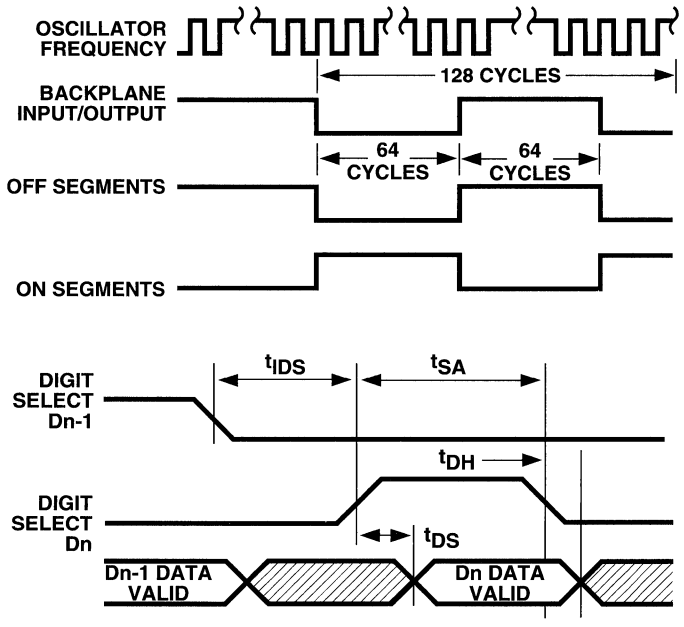
5

TC7211A

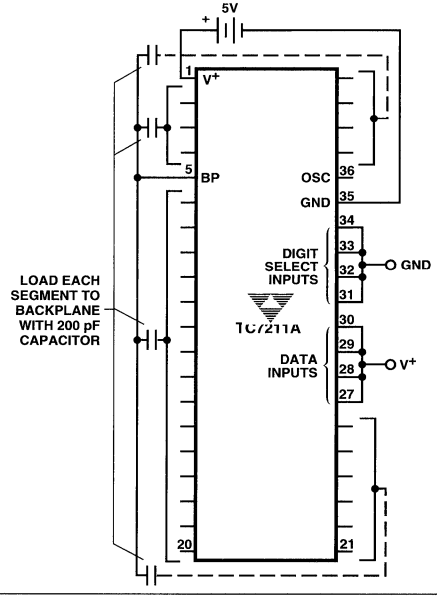
FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAMS



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +6.5V
Input Voltage, Any Terminal
(Note 2) ..... V^+ +0.3V, GND – 0.3V
Power Dissipation (Note 1) ..... 0.8 W at +70°C
Operating Temperature Range ..... – 20°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less that GND may cause destructive latch-up. For this reason it is recommended that inputs from external sources not operating on the same power supply not be applied to the device before its supply is established, and, in multiple supply systems, the supply to the TC7211A/TC7212A be turned on first.

TABLE I: OPERATING CHARACTERISTICS

Test Conditions: All parameters measured with V+ = 5V, T_A = 25°C

TC7211A Characteristics (LCD Decoder/Driver)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SUP}	Operating Voltage Range		3	5	6	V
I_{OP}	Operating Current	Display Blank	—	10	50	µA
I_{OSCI}	Oscillator Input Current	Pin 36	—	±2	±10	µA
t_{RFS}	Segment Rise/Fall Time	C_L = 200 pF	—	0.5	—	µA
t_{RFB}	Backplane Rise/Fall Time	C_L = 5000 pF	—	1.5	—	µs
f_{OSC}	Oscillator Frequency	Pin 36 Floating	—	16	—	kHz
f_{BP}	Backplane Frequency	Pin 36 Floating	—	125	—	Hz
AC Characteristics						
t_{SA}	Chip Select Active Pulse Width	Refer to Timing Diagrams	1	—	—	µs
t_{DS}	Data Valid Time	Refer to Timing Diagrams	—	—	—	ns
t_{DH}	Data Hold Time	Refer to Timing Diagrams	200	—	—	ns
t_{IDS}	Inter-Digit Select Time	Refer to Timing Diagrams	2	—	—	µs

INPUT DEFINITIONS

In this table, V^+ and GND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

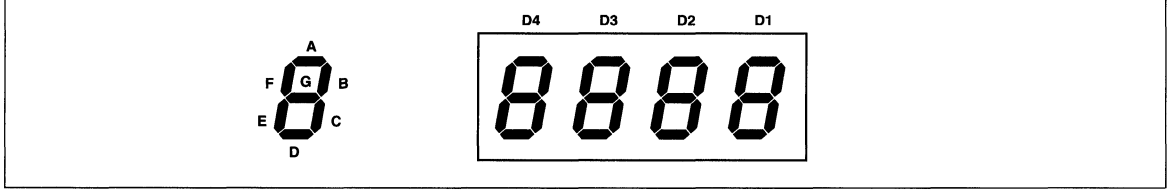
Input	Pin No.	Condition	Function	
B0	27	V^+ = Logic "1" GND = Logic "0"	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logic "1" GND = Logic "0"	Twos	
B2	29	V^+ = Logic "1" GND = Logic "0"	Fours	
B3	30	V^+ = Logic "1" GND = Logic "0"	Eights (Most Significant)	
OSC	36	Floating or with external capacitor GND	Oscillator input. Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (pin 5)	
D1	31		D1 Digit Select (Least Significant)	
D2	32	V^+ = Active	D2 Digit Select	
D3	33	GND = Inactive	D3 Digit Select	
D4	34		D4 Digit Select (Most Significant)	
V+	1		Power-Supply Voltage	
BP	5		Back Plane	
GND	35		System Ground	

OUTPUT DEFINITIONS

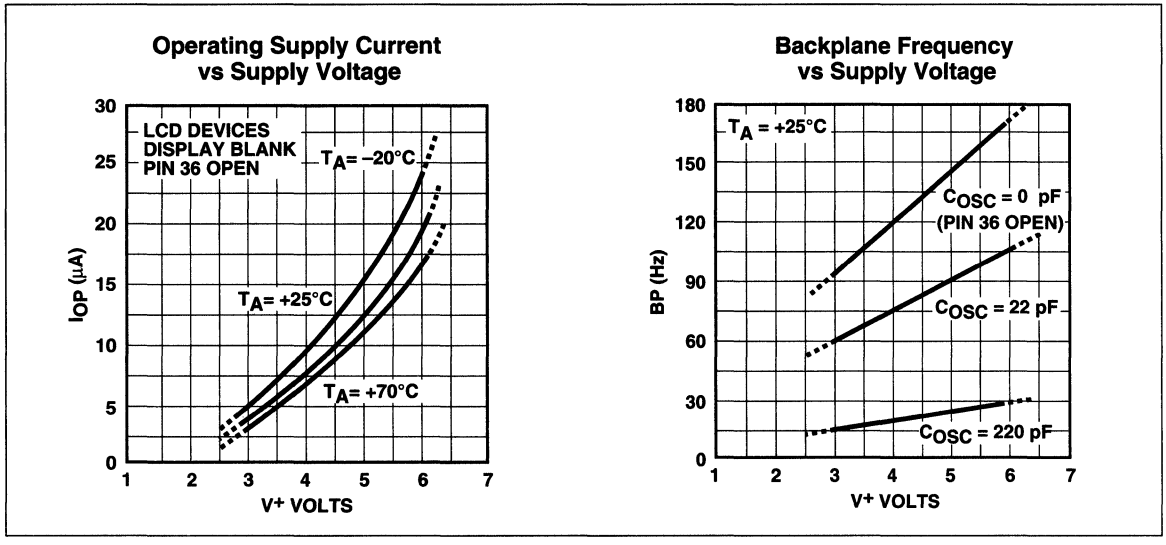
Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

Output	Pin No.	Function			Output	Pin No.	Function		
A1	37 A	Segment Drive	Digit 1	(LSD)	A3	13 A	Segment Drive	Digit 3	
B1	38 B	↓	↓	↓	B3	14B	↓	↓	
C1	39 C	↓	↓	↓	C3	15C	↓	↓	
D1	40 D	↓	↓	↓	D3	16D	↓	↓	
E1	2 E	↓	↓	↓	E3	17E	↓	↓	
F1	4 F	↓	↓	↓	F3	19F	↓	↓	
G1	3 G	↓	↓	↓	G3	18G	↓	↓	
A2	6 A	Segment Drive	Digit 2		A4	20A	Segment Drive	Digit 4	(MSD)
B2	7 B	↓	↓		B4	21B	↓	↓	↓
C2	8 C	↓	↓		C4	22C	↓	↓	↓
D2	9 D	↓	↓		D4	23D	↓	↓	↓
E2	10 E	↓	↓		E4	24E	↓	↓	↓
F2	12 F	↓	↓		F4	26F	↓	↓	↓
G2	11 G	↓	↓		G4	25	↓	↓	↓

DIGIT ASSIGNMENT



TYPICAL OPERATING CHARACTERISTICS CURVES



BASIC OPERATION

The TC7211A drives 4-digit by 7-segment LCDs. The device contains 28 individual segment drivers, a backplane driver, an on-chip oscillator, and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N- and P-channel transistors for identical "ON" resistance. The equal resistances eliminate the DC output driver component resulting from unequal rise and fall times. This ensures maximum LCD life.

The backplane output driver can be disabled by grounding the OSCILLATOR input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane (BP) terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCDs with characters in multiples of four. (See Figure 1.)

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices drivable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half-inch characters with rise and fall times under 5 µs. This represents a system with three slave devices and a fourth master device driving the backplane.

If more than four devices are slaved together, the backplane signal should be derived externally and all TC7211A devices slaved to it. The external drive signal must drive a high capacitive load with 1µs to 2 µs rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures, the frequency may be reduced to compensate for display response time.

The on-chip RC oscillator free-runs at approximately 16 kHz. A ÷128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal and V^+. (See typical operating characteristics curves.)

The free-running oscillator may be overridden (if desired) by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or LOW portion, as this will result in a DC drive component being applied to the LCD, limiting the LCD's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the LOW portion duration is less than 1 µs. The backplane disable sensing circuit will not respond to such a short signal.

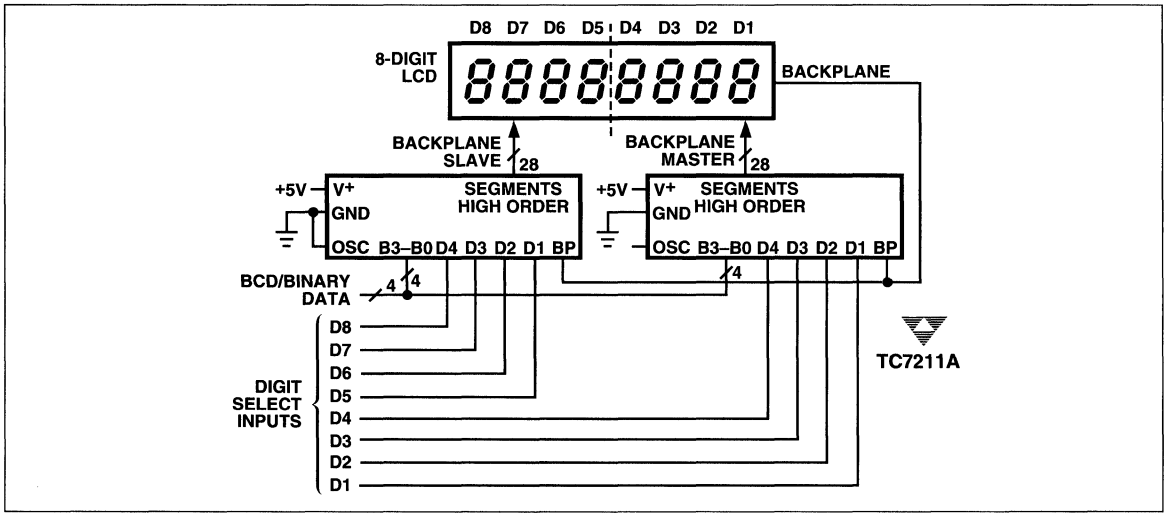


Figure 1. TC7211AM Driving an 8-Digit LCD Display in Master/Slave Configuration

Input Configuration and Output Codes

The TC7211AM accepts a 4-bit, true binary (positive level = logic "1") input at pin 27 (LSB) through pin 30 (MSB). The binary input is decoded to the 7-segment output known as Code B. The output display format is 0 to 9, —, E, H, L, P and blank display (see Table I). Segment assignments are shown in Figure 2. The TC7211AM will correctly decode binary and BCD true codes to a 7-segment output.

The TC7211A accepts multiplexed binary or BCD input data at pin 27 (LSB) through pin 30 (MSB). Pins 31 (LSD) through 34 (MSD) are the digit select lines. When the digit select line is taken to logic "1", input data is decoded and stored in the enabled output latch of the selected digit. More than one digit selected line may be activated simultaneously. The same character will be written into all selected digits. (See Figure 4 for decoder segment assignments.)

Table I. Output Code

B3	B2	B1	B0	Code B
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	–
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

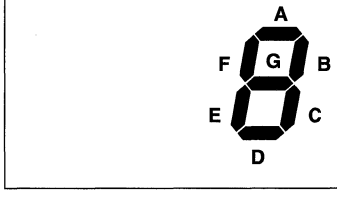


Figure 2. Segment Assignment

Special Order Decoder Option

The TC7211A is mask-programmed to give the 16 combinations of 7-segment output codes. For large volume orders (50K pieces minimum), custom decoder options are available. Contact TelCom Semiconductor for details.

TC7211A

TYPICAL APPLICATIONS

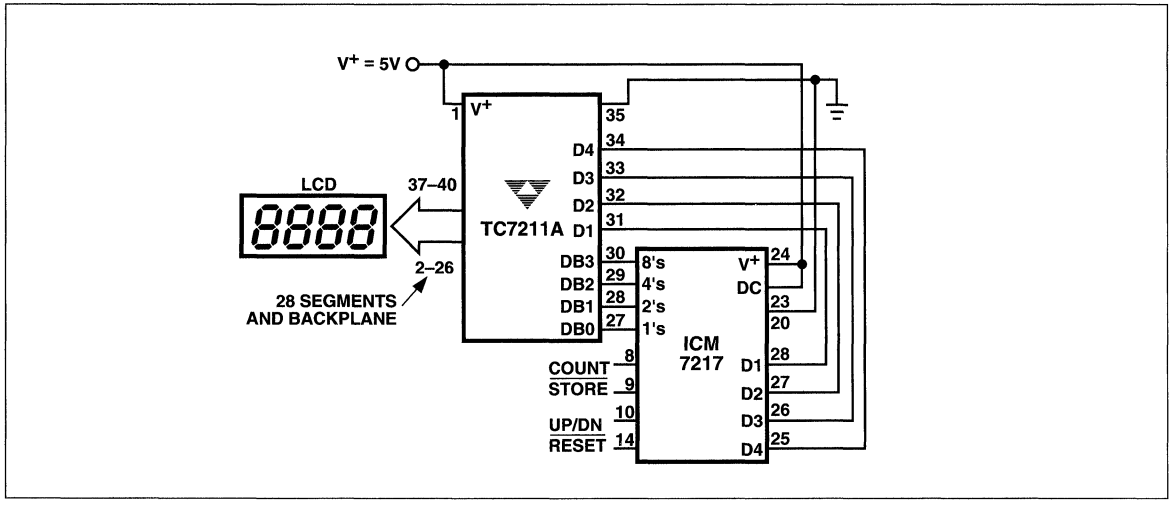


Figure 3. LCD Display Interface to 4-Digit Counter

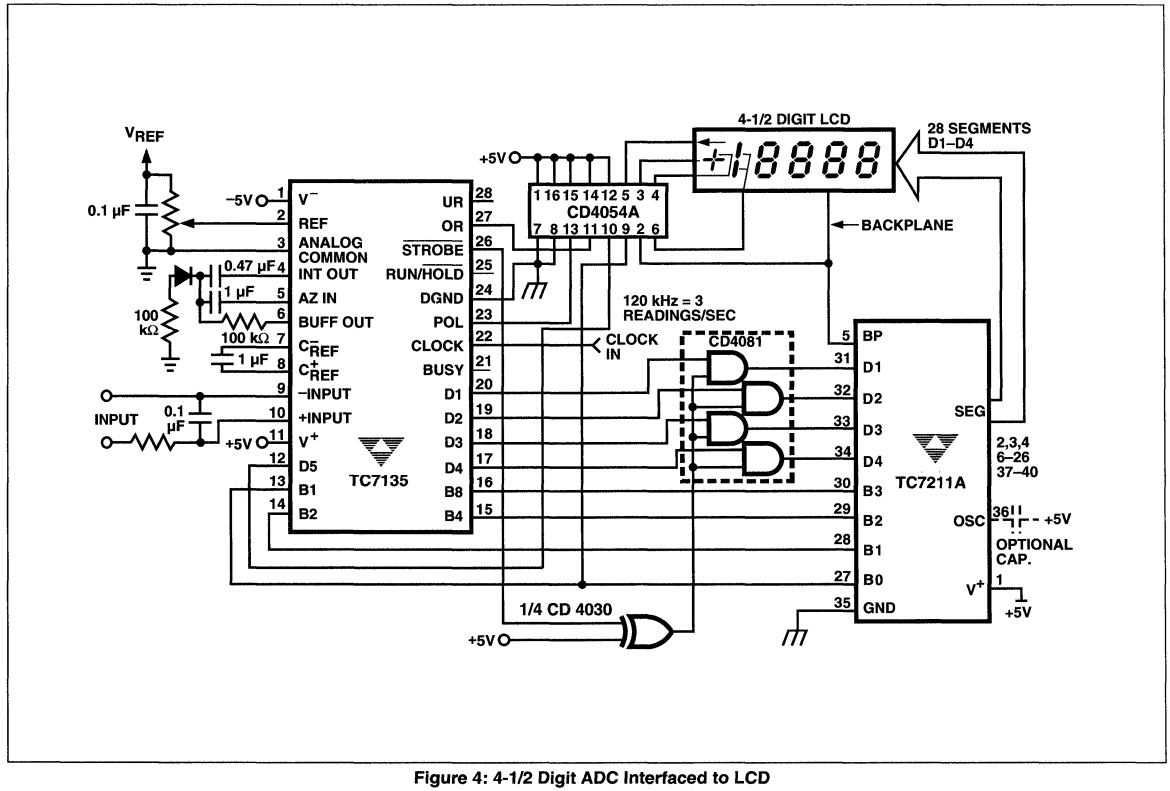


Figure 4: 4-1/2 Digit ADC Interfaced to LCD

TYPICAL APPLICATIONS (Cont.)

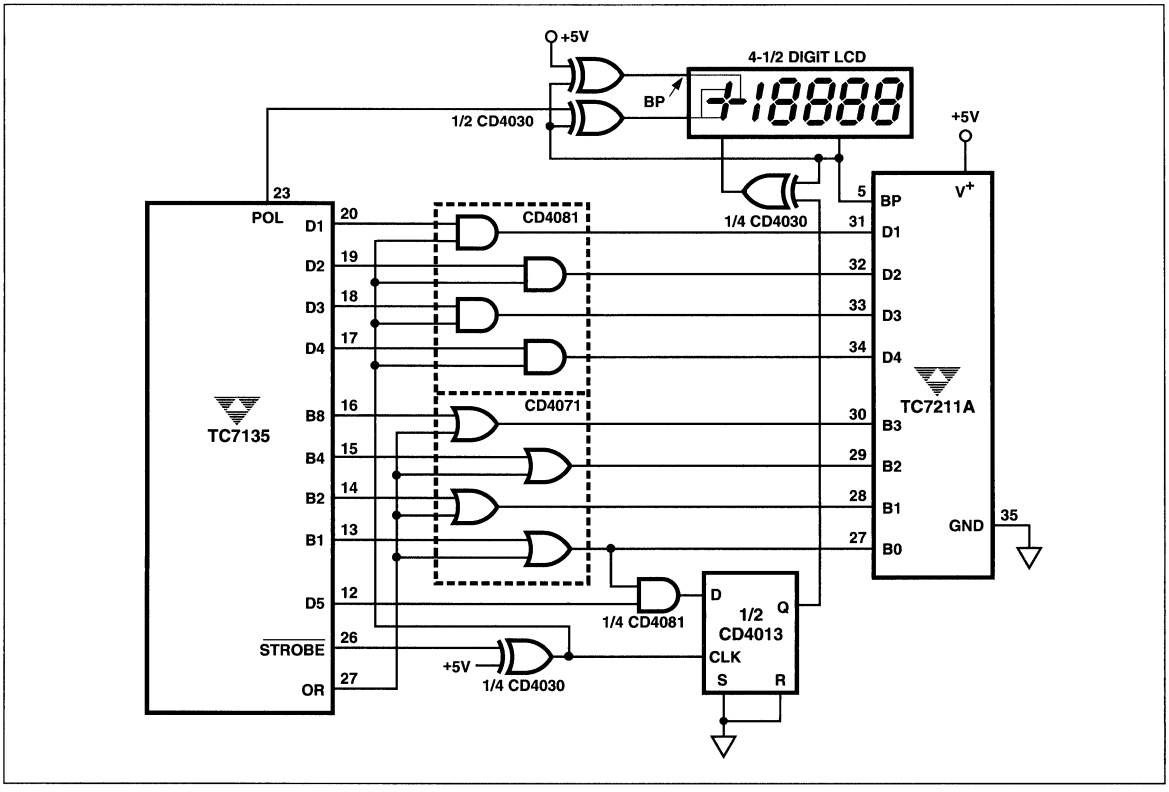


Figure 5. 4-1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

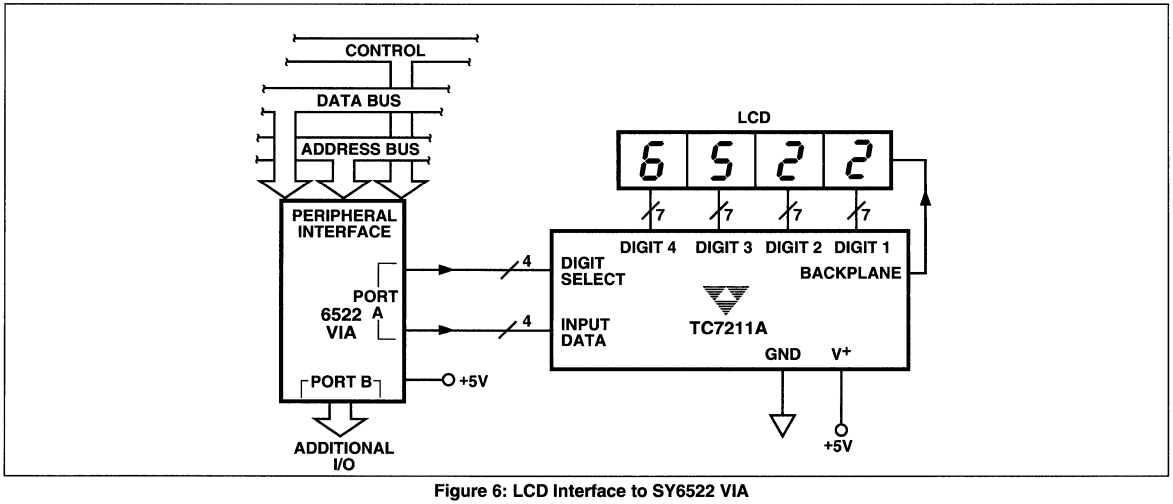


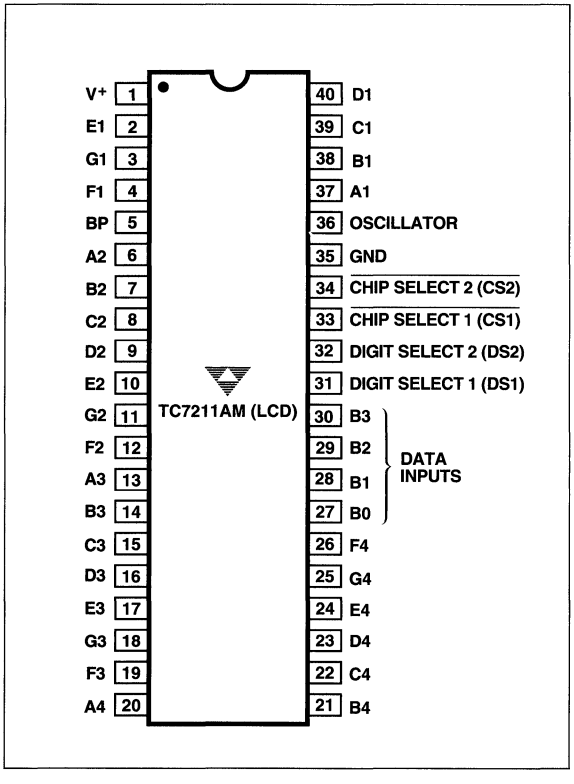
Figure 6: LCD Interface to SY6522 VIA

BUS COMPATIBLE 4-DIGIT CMOS DECODER/DRIVER

FEATURES

- **4-Digit Non-Multiplexed 7-Segment LCD Outputs With Backplane Driver**
- **Input and Digit Select Data Latches**
- **RC Oscillator On-Chip Generates Backplane Drive Signal**
- **Eliminates DC Bias Which Degrades LCD Life**
- **Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal**
- **Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)**
- **Pin Compatible and Functionally Equivalent to ICM7211AM**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC7211AM (LCD Decoder/driver) is a CMOS direct drive, 4-digit, 7-segment display decoder and driver. The bus compatible making microprocessor controlled displays possible. Two chip-select signals control data and digit-select code latching prior to decoding and display. External data latches are unnecessary.

The TC7211AM drives conventional LCDs. An RC oscillator, divider chain, backplane driver, and 28-segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane, but in-phase for an OFF segment and out-of-phase for an ON segment. The net DC voltage applied between driver segment and backplane is near zero maximizing display lifetime.

The four bit binary input is decoded into the seven segment alphanumeric code known as "Code B". The "Code B" output format results in a 0 to 9,—, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

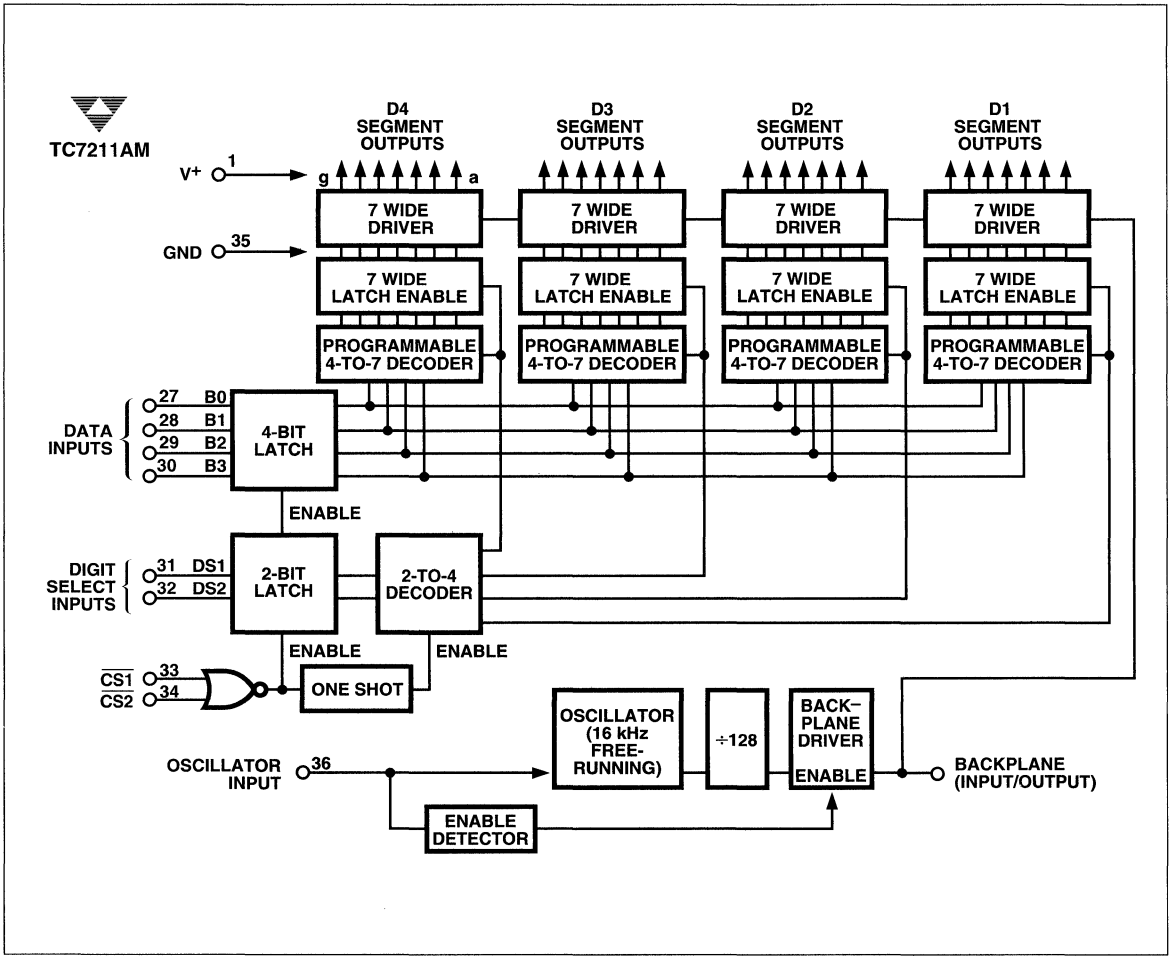
ORDERING INFORMATION

Driver	Input	Output		
Part No.	**Type**	**Package**	**Code**	**Config.**
TC7211AMIPL	LCD	40-PDIP	Code B	Data and Digit Select Latches

5

TC7211AM

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +6.5V
Input Voltage, Any Terminal
(Note 2) ..... V^+ +0.3V, GND –0.3V
Power Dissipation (Note 1) ..... 1W at +70°C
Operating Temperature Range ..... –20°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. For this reason, it is recommended that inputs from external sources not operating on the same power supply not be applied to the device before its supply is established, and, in multiple supply systems, the supply to the TC7211AM be turned on first.

TABLE I: OPERATING CHARACTERISTICS

Test Conditions: All parameters measured with V+ = 5V, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SUP}	Operating Voltage Range		3	5	6	V
I_{OP}	Operating Current	Display Blank	—	10	50	µA
I_{OSCI}	Oscillator Input Current	Pin 36	—	±2	±10	µA
t_{RFS}	Segment Rise/Fall Time	C_L = 200 pF	—	0.5	—	µA
t_{RFB}	Backplane Rise/Fall Time	C_L = 5000 pF	—	1.5	—	µs
f_{OSC}	Oscillator Frequency	Pin 36 Floating	—	16	—	kHz
f_{BP}	Backplane Frequency	Pin 36 Floating	—	125	—	Hz
Input Characteristics						
V_{IH}	Logic "1" High Input Voltage		3	—	—	V
V_{IL}	Logic "0" Low Input Voltage		—	—	1	V
I_{ILK}	Input Leakage Current	Pins 27–34	—	±0.01	±1	µA
C_{IN}	Input Capacitance	Pins 27–34	—	5	—	pF
I_{BPLK}	BP Input Current Leakage	Measured at Pin 5 With Pin 36 at GND	—	±0.01	±1	µA
C_{BPI}	BP Input Capacitance	All Devices	—	200	—	pF

5

TABLE I: OPERATING CHARACTERISTICS

Test Conditions: All parameters measured with V+ = 5V, $T_A = 25^{\circ}C$

AC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{CSA}	Chip Select Active Pulse Width	(Note 3)	200	—	—	ns
t_{DS}	Data Setup Time		100	—	—	ns
t_{DH}	Data Hold Time		10	0	—	ns
t_{ICS}	Inter-Chip Select Time		2	—	—	µs

NOTE: 3. Other chip select (CS) is either held at logic zero or both CS1 and CS2 driven together.

TIMING DIAGRAMS

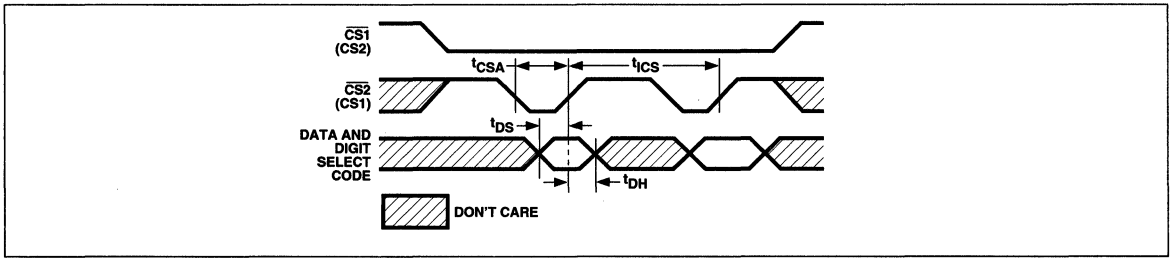


Figure 1: BUS Interface Timing Diagram

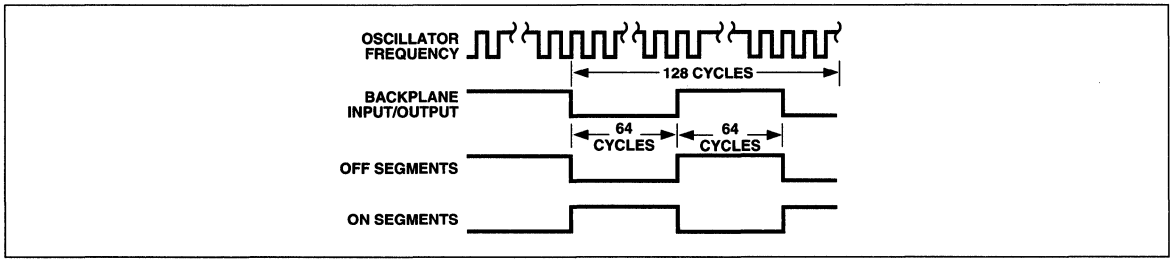


Figure 2: LCD Display Waveforms

INPUT DEFINITIONS

In this table, V^+ and GND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

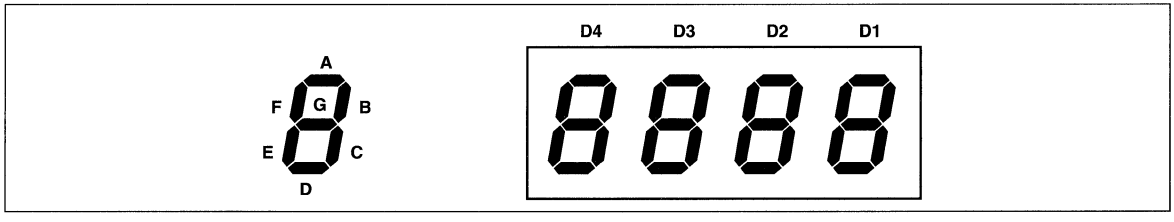
Input	Pin No.	Condition	Function	
B0	27	V^+ = Logic "1" GND = Logic "0"	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logic "1" GND = Logic "0"	Twos	
B2	29	V^+ = Logic "1" GND = Logic "0"	Fours	
B3	30	V^+ = Logic "1" GND = Logic "0"	Eights (Most Significant)	
OSC	36	Floating or with external capacitor GND	Oscillator input. Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (pin 5)	
DS1	31	V^+ = Logical One	DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	Digit Select Inputs
$\overline{DS2}$	32	GND = Logical Zero		
$\overline{CS1}$	33	V^+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are LOW, the data and digit select input latches are open or enabled.	
CS2	34	GND = Active	On the rising of $\overline{CS1}$ or $\overline{CS2}$, data is latched, decoded and stored in the output drive latches.	

OUTPUT DEFINITIONS

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

Output	Pin No.		Function			Output	Pin No.		Function		
A1	37	A	Segment Drive	Digit 1	(LSD)	A3	13	A	Segment Drive	Digit 3	
B1	38	B	↓	↓	↓	B3	14	B	↓	↓	
C1	39	C	↓	↓	↓	C3	15	C	↓	↓	
D1	40	D	↓	↓	↓	D3	16	D	↓	↓	
E1	2	E	↓	↓	↓	E3	17	E	↓	↓	
F1	4	F	↓	↓	↓	F3	19	F	↓	↓	
G1	3	G	↓	↓	↓	G3	18	G	↓	↓	
A2	6	A	Segment Drive	Digit 2		A4	20	A	Segment Drive	Digit 4	(MSD)
B2	7	B	↓	↓		B4	21	B	↓	↓	↓
C2	8	C	↓	↓		C4	22	C	↓	↓	↓
D2	9	D	↓	↓		D4	23	D	↓	↓	↓
E2	10	E	↓	↓		E4	24	E	↓	↓	↓
F2	12	F	↓	↓		F4	26	F	↓	↓	↓
G2	11	G	↓	↓		G4	25	G	↓	↓	↓

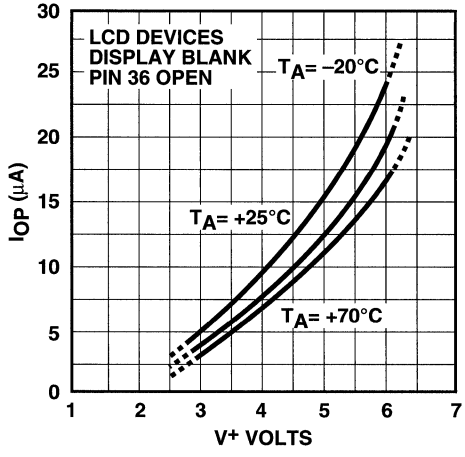
DIGIT ASSIGNMENT



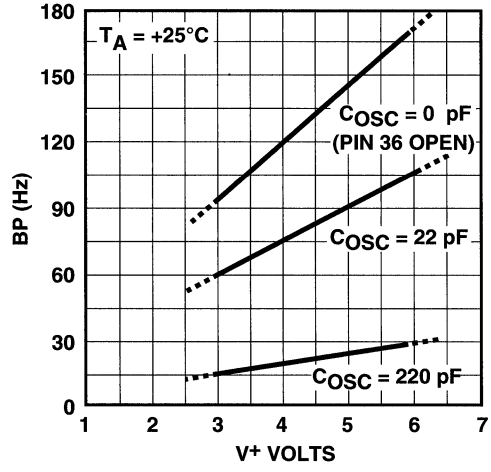
TC7211AM

TYPICAL OPERATING CHARACTERISTICS CURVES

Operating Supply Current vs Supply Voltage



Backplane Frequency vs Supply Voltage



BASIC OPERATION

The TC7211AM drives 4-digit, 7-segment LCDs. This device contains 28 individual segment drivers, a backplane driver, a self-contained oscillator, and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N- and P-channel transistors for identical ON resistance. The equal resistances eliminate the DC output driver component resulting from unequal rise and fall times. This ensures maximum LCD life.

The backplane output driver can be disabled by grounding the OSCILLATOR input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane (BP) terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCDs with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices drivable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half-inch characters with rise and fall times under 5 μs. This represents a system with three slave devices and a fourth master device driving the backplane. (See Figure 1.)

If more than four devices are slaved together, the backplane signal should be derived externally and all TC7211AM devices slaved to it. The external drive signal must drive a high capacitive load with 1μs to 2 μs rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures, the frequency may be reduced to compensate for display response time.

The on-chip RC oscillator free-runs at approximately 16 kHz. A ÷128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal and V+. (See typical operating characteristics curves.)

The free-running oscillator may be overridden (if desired) by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or lOW portion, as this will result in a DC drive component being applied to the LCD, limiting the LCD's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the LOW portion duration is

less than 1 µs. The backplane disable sensing circuit will not respond to such a short signal.

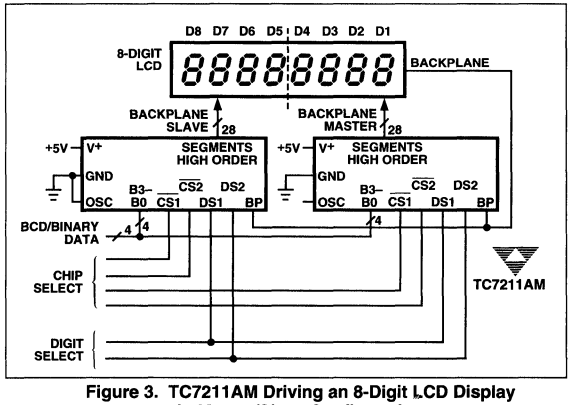


Figure 3. TC7211AM Driving an 8-Digit LCD Display in Master/Slave Configuration

Input Configuration and Output Codes

The TC7211AM accepts a 4-bit, true binary (positive level = logic "1") input at pin 27 (LSB) through pin 30 (MSB). The binary input is decoded to the 7-segment output known as Code B. The output display format is 0 to 9, —, E, H, L, P and blank display (see Table I). Segment assignments are shown in Figure 2. The TC7211AM will correctly decode binary and BCD true codes to a 7-segment output.

The TC7211AM is designed to interface with a data bus and display data under microprocessor control. Four data inputs (pins 27–30) and two digit select input bits (pins 31 and 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The 2-bit digit code selects the appropriate output digit latch. The 4-bit display data word is decoded to the "Code B" 7-segment output format.

For applications where bus compatibility is not required, refer to the TC7211AM (LCD) 4-digit decoder driver data sheet. This device is designed to accept multiplexed BCD/binary input data for display under the control of four separate digit select control signals.

Binary Input				Code B
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	Blank

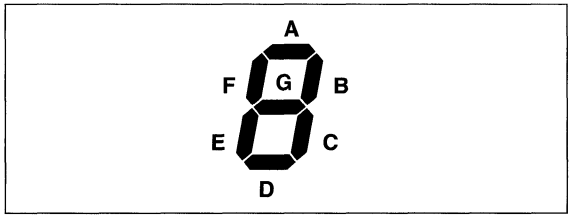
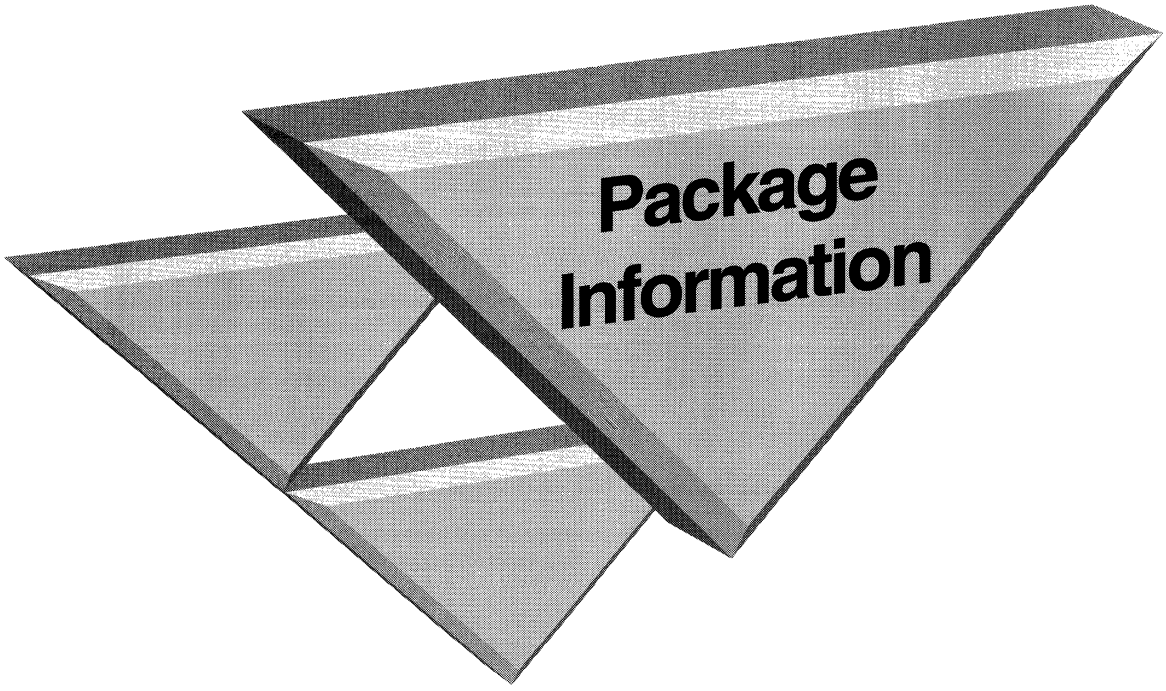


Figure 2. Segment Assignment

Special Order Decoder Option

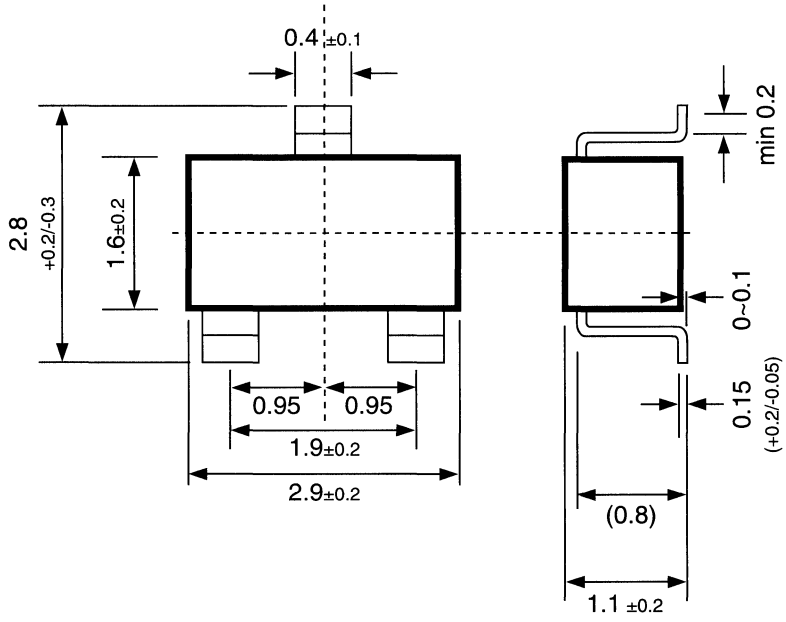
The TC7211AM is mask programmed to give the 16 combinations of 7-segment output codes. For large volume orders (50K pieces minimum), custom decoder options are available. Contact TelCom Semiconductor for details.

5



6

SOT-23-3
MINI-MOLD PACKAGE



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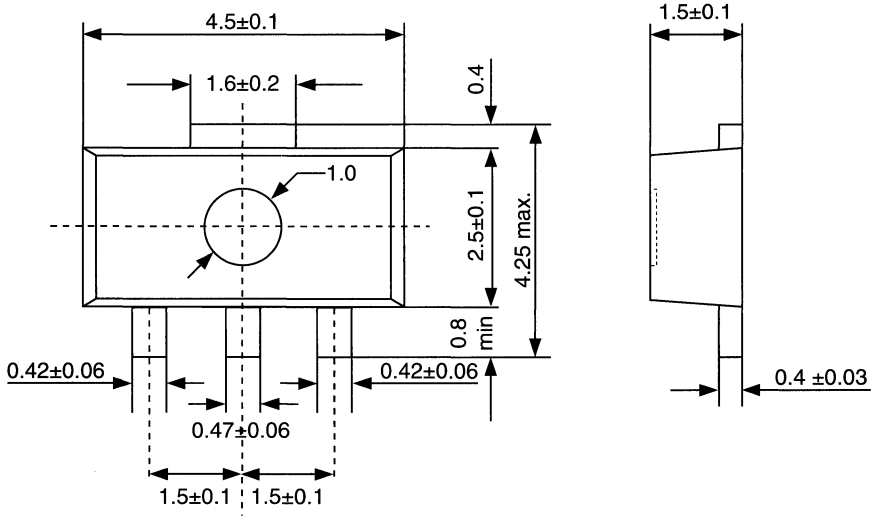

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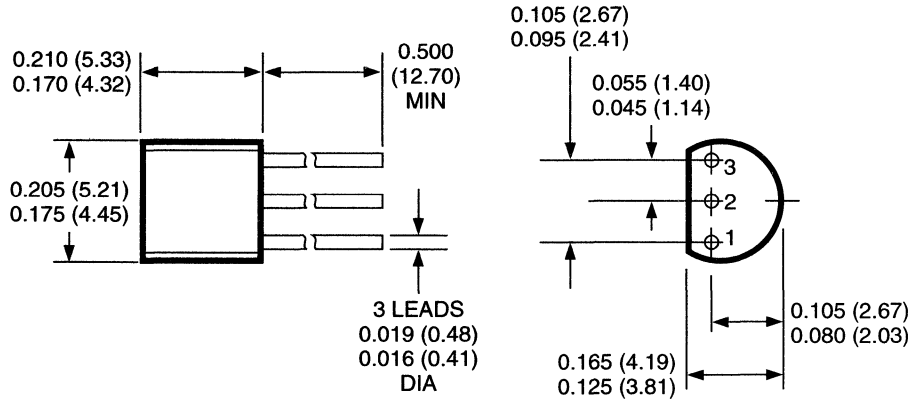
TO-92-3
THROUGH-HOLE PACKAGE



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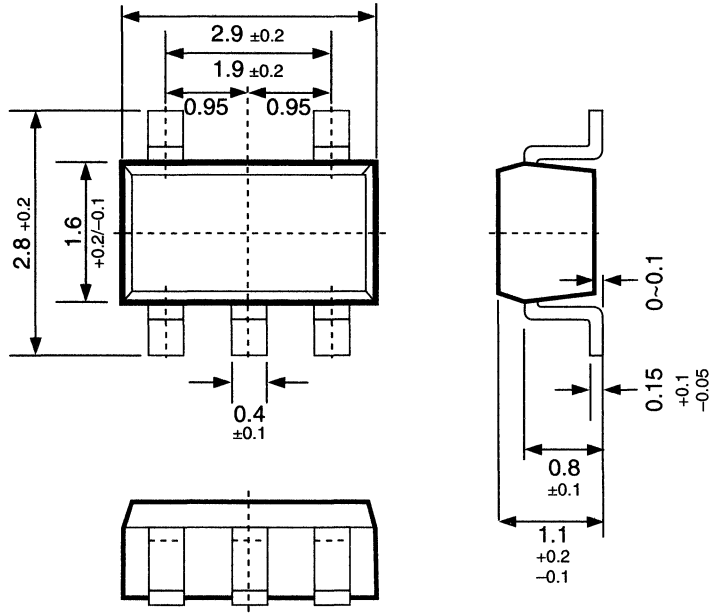

SOT-89-5
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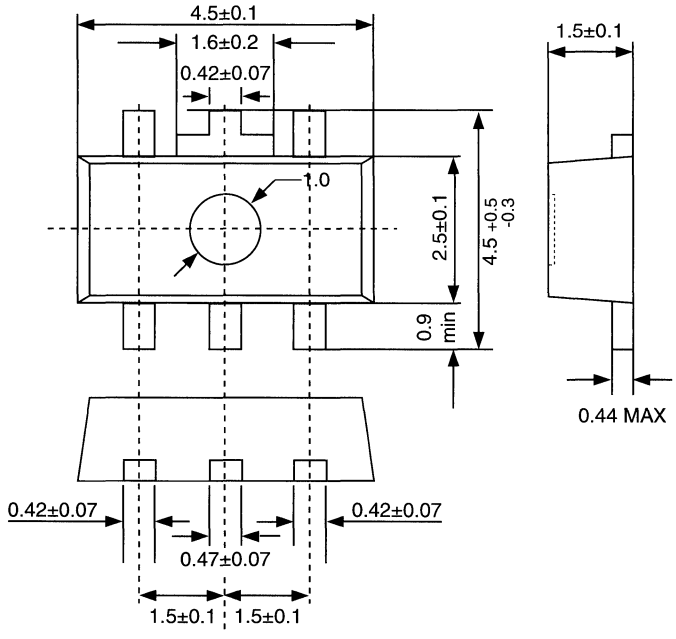
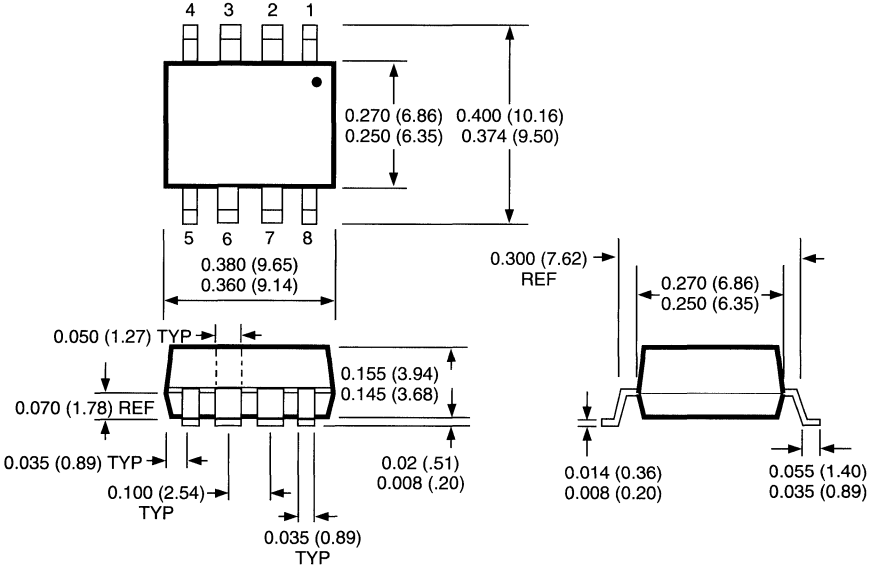
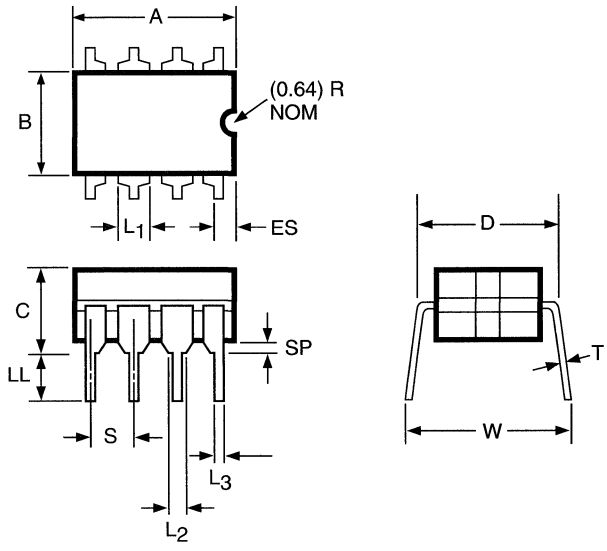


8-Pin Gullwing DIP



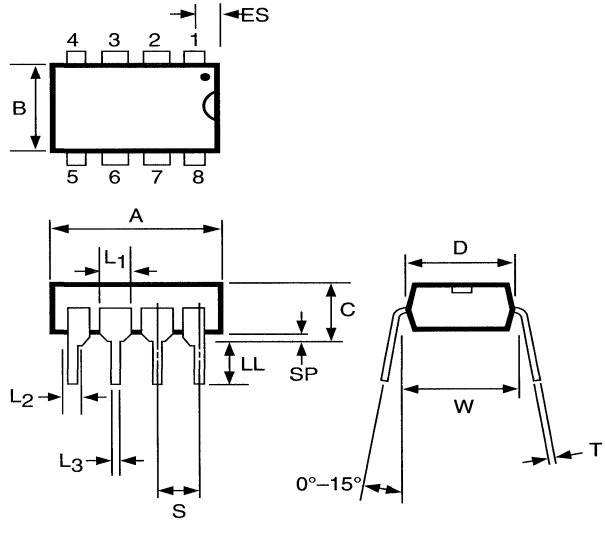
6

8-Pin CERDIP



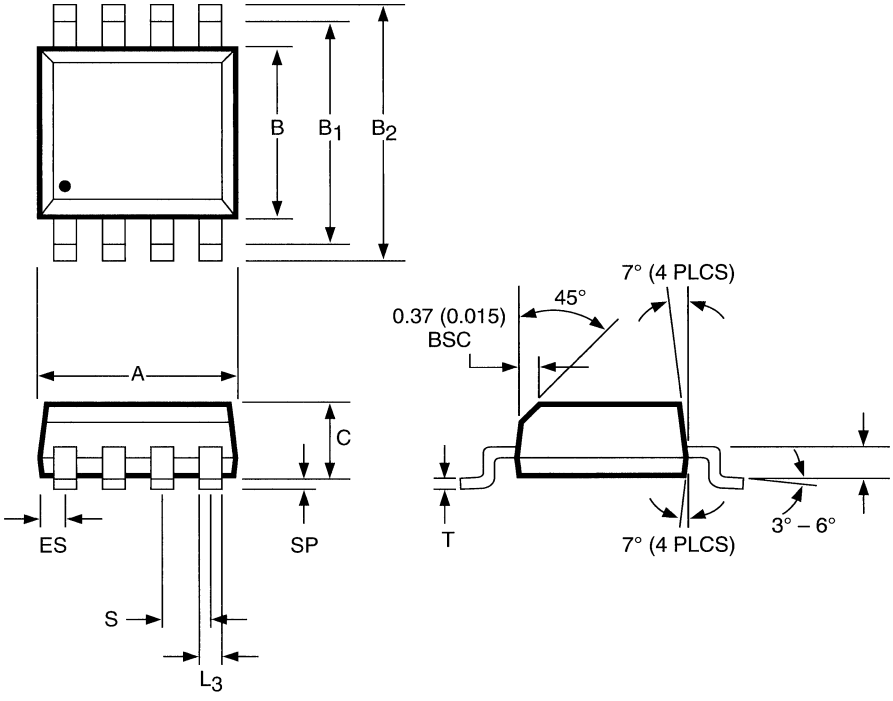
Dimension	Inches		mm	
	Min	Max	Min	Max
A	0.370	0.400	9.40	10.16
B	0.230	0.300	5.84	7.62
C	0.160	0.200	4.06	5.08
D	0.290	0.325	7.37	8.26
L1	0.045	0.085	1.14	2.16
L2	0.040	0.050	1.02	1.27
L3	0.016	0.020	0.41	0.51
LL	0.125	0.165	3.18	4.19
S	0.090	0.110	2.29	2.79
SP	0.020	0.040	0.51	1.02
ES	0.015	0.045	0.38	1.14
T	0.008	0.015	0.20	0.38
W	0.360	0.400	9.14	10.16
W	0.360	0.400	9.14	10.16

8-Pin Plastic DIP



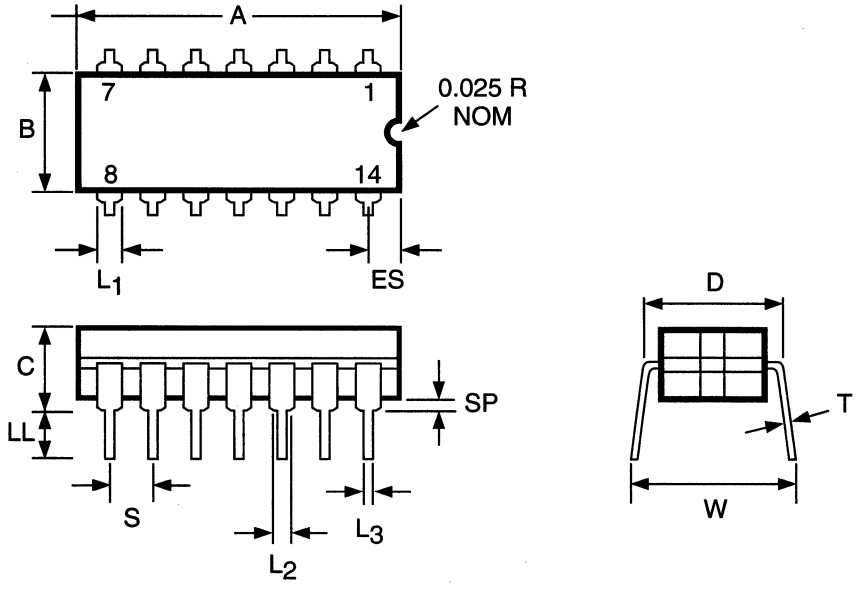
Dimension	Inches		mm	
	Min	Max	Min	Max
A	0.348	0.380	8.84	9.65
B	0.240	0.260	6.10	6.60
C	0.160	0.200	4.06	5.08
D	0.290	0.310	7.37	7.87
L1	0.045	0.085	1.14	2.16
L2	0.040	0.050	1.02	1.27
L3	0.015	0.022	0.38	0.56
LL	0.100	0.150	2.54	3.81
S	0.090	0.110	2.29	2.79
SP	0.020	0.040	0.51	1.02
ES	0.015	0.045	0.38	1.14
T	0.008	0.015	0.20	0.38
W	0.360	0.400	9.14	10.16

8-Pin SOIC



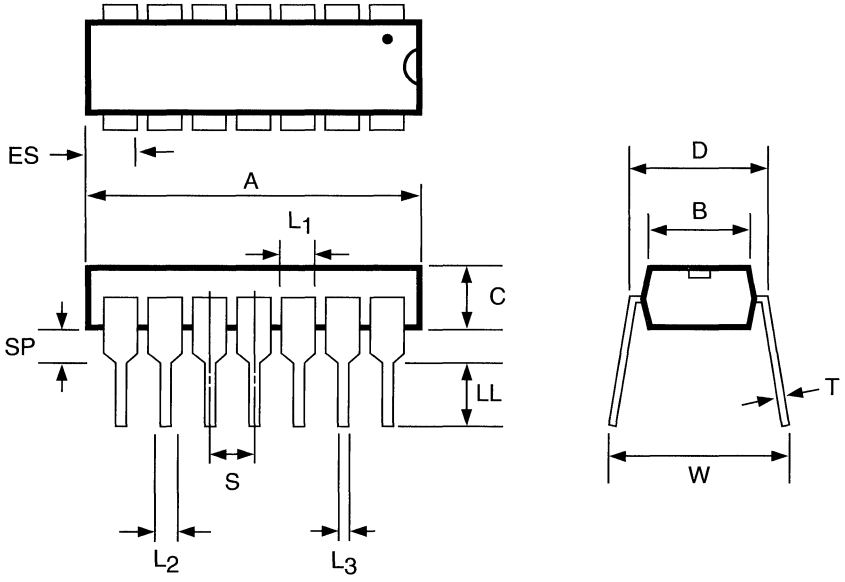
Dimension	Inches		mm	
	Min	Max	Min	Max
A	0.189	0.197	4.80	5.00
B	0.150	0.157	3.81	3.99
B1	0.181	0.205	4.60	5.21
B2	0.228	0.244	5.79	6.20
C	0.053	0.069	1.35	1.75
L3	0.014	0.018	0.36	0.46
S	0.049	0.051	1.24	1.30
SP	0.004	0.008	0.10	0.20
ES	0.018	0.022	0.46	0.56
T	0.007	0.010	0.18	0.25

14-Pin CERDIP



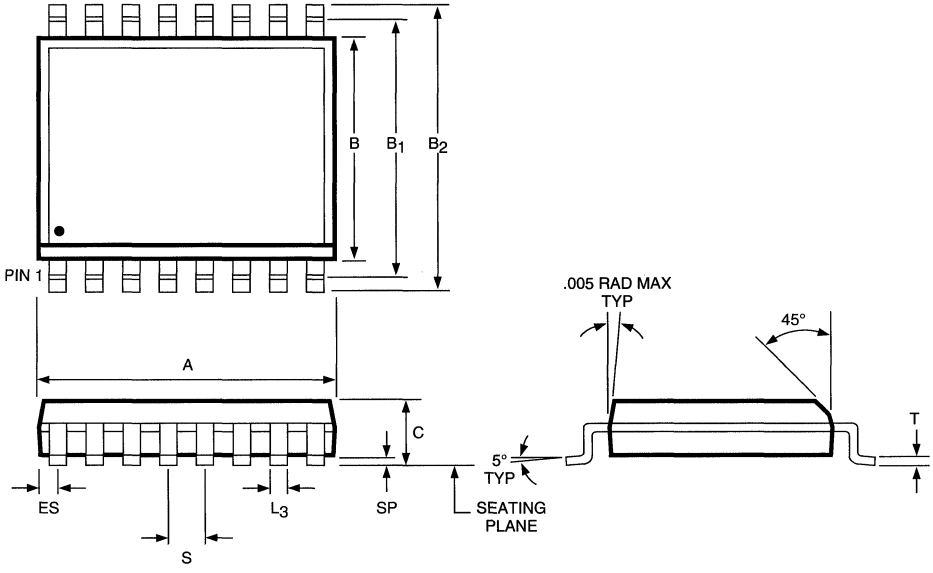
Dimension	Inches		mm	
	Min	Max	Min	Max
A	0.740	0.780	18.80	19.81
B	0.230	0.300	5.84	7.62
C	0.160	0.200	4.06	5.08
D	0.290	0.325	7.37	8.26
L1	0.045	0.085	1.14	2.16
L2	0.040	0.050	1.02	1.27
L3	0.016	0.020	0.41	0.51
LL	0.125	0.165	3.18	4.19
S	0.090	0.110	2.29	2.79
SP	0.020	0.040	0.51	1.02
ES	0.015	0.045	0.38	1.14
T	0.008	0.015	0.20	0.38
W	0.360	0.400	9.14	10.16

14-Pin Plastic DIP



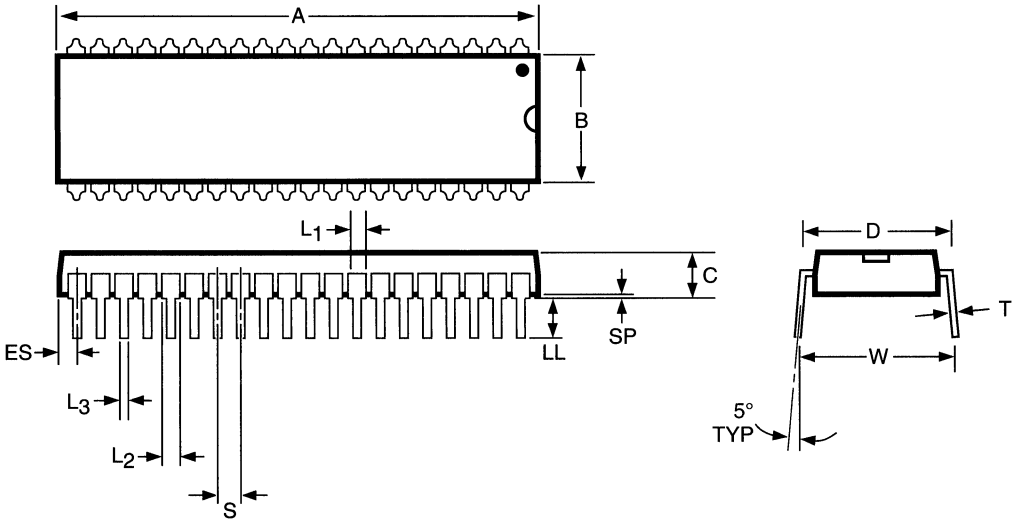
Dimension	Inches		mm	
	Min	Max	Min	Max
A	0.745	0.770	18.92	19.56
B	0.240	0.260	6.10	6.60
C	0.140	0.200	3.56	5.08
D	0.290	0.325	7.37	8.26
L1	0.045	0.085	1.14	2.16
L2	0.040	0.050	1.02	1.27
L3	0.015	0.022	0.38	0.56
LL	0.115	0.165	2.92	4.19
S	0.090	0.110	2.29	2.79
SP	0.020	0.040	0.51	1.02
ES	0.015	0.045	0.38	1.14
T	0.008	0.015	0.20	0.38
W	0.360	0.400	9.14	10.16

16-Pin SOIC



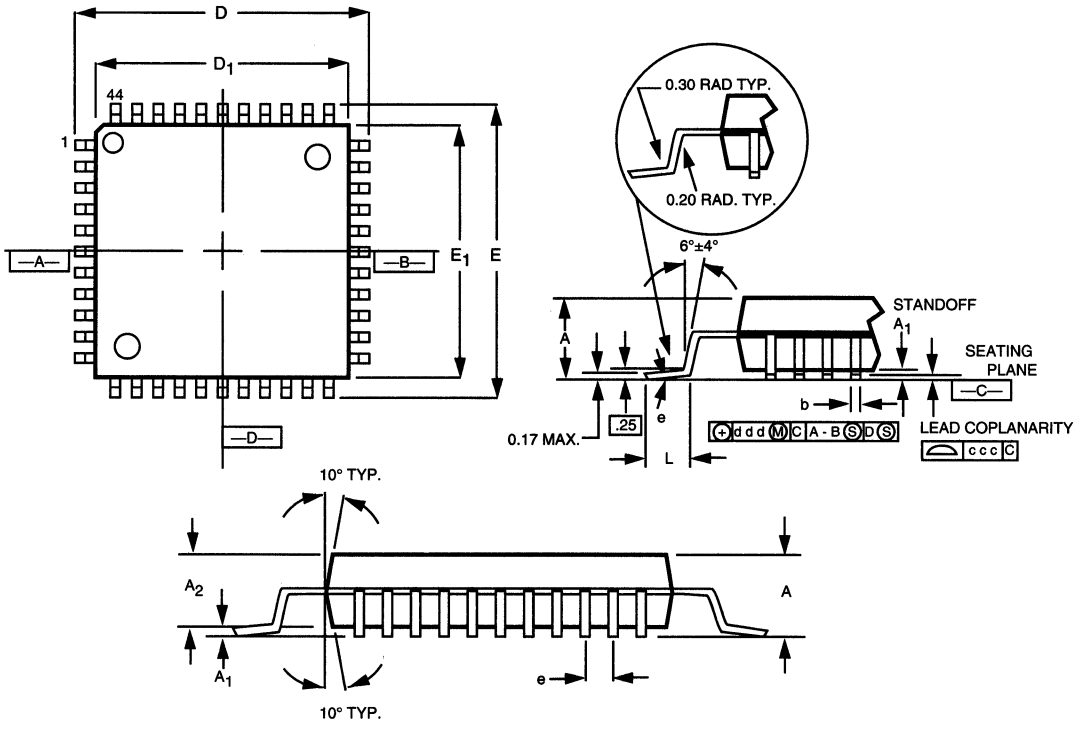
Dimension	Inches		mm	
	Min	Max	Min	Max
A	0.403	0.413	10.24	10.49
B	0.292	0.300	7.42	7.62
B1	0.330	0.374	8.38	9.50
B2	0.400	0.410	10.16	10.41
C	0.097	0.104	2.46	2.64
L3	0.015	0.022	0.38	0.56
S	0.049	0.051	1.24	1.30
SP	0.006	0.012	0.15	0.30
ES	0.028	0.030	0.71	0.76
T	0.008	0.015	0.20	0.38

40-Pin Plastic DIP



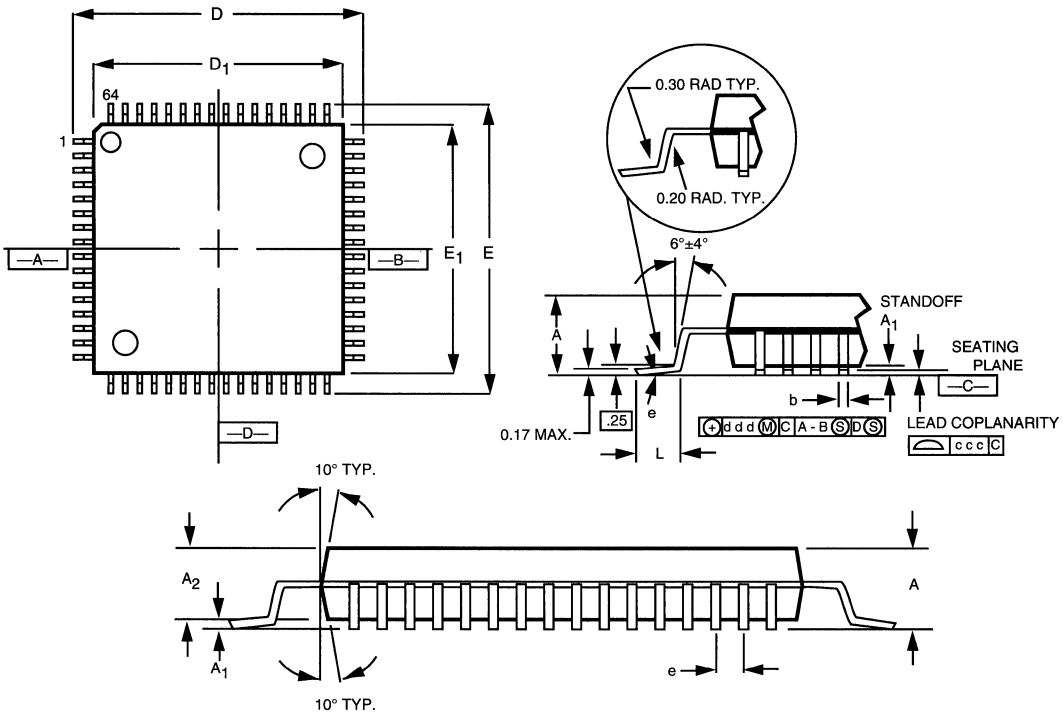
Dimension	Inches		mm	
	Min	Max	Min	Max
A	2.035	2.065	51.69	52.45
B	0.530	0.555	13.46	14.10
C	0.165	0.205	4.19	5.21
D	0.590	0.610	14.99	15.49
L1	0.040	0.065	1.02	1.65
L2	0.040	0.050	1.02	1.27
L3	0.015	0.022	0.38	0.56
LL	0.115	0.150	2.92	3.81
S	0.090	0.110	2.29	2.79
SP	0.020	0.040	0.51	1.02
ES	0.015	0.045	0.38	1.14
T	0.008	0.015	0.20	0.38
W	0.660	0.700	16.76	17.78

44 PQFP



Body Thickness		2.00
Footprint (Body+)		3.90
Dimensions	**Tolerance**	
A	MAX.	2.45
A1	MIN.	0.25
A2	±0.10	2.00
D	—0.25	13.90
D1	±0.10	10.00
E	±0.25	13.90
E1	±0.10	10.00
L	+0.15/–0.10	0.88
e	BASIC	0.80
b	±0.05	0.35
ccc	MAX.	0.10
ddd	NOM.	0.20
θ		0° – 7°

64-Pin Flat Package



Body Thickness		2.70
Footprint (Body+)		3.20
Dimensions	**Tolerance**	
A	MAX.	3.15
A1	MIN.	0.25
A2	±0.10	2.70
D	—0.25	17.20
D1	±0.10	14.00
E	±0.25	17.20
E1	±0.10	14.00
L	+0.15/–0.10	0.88
e	BASIC	0.80
b	±0.05	0.35
ccc	MAX.	0.10
ddd	NOM.	0.20
θ		0° – 7°

6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