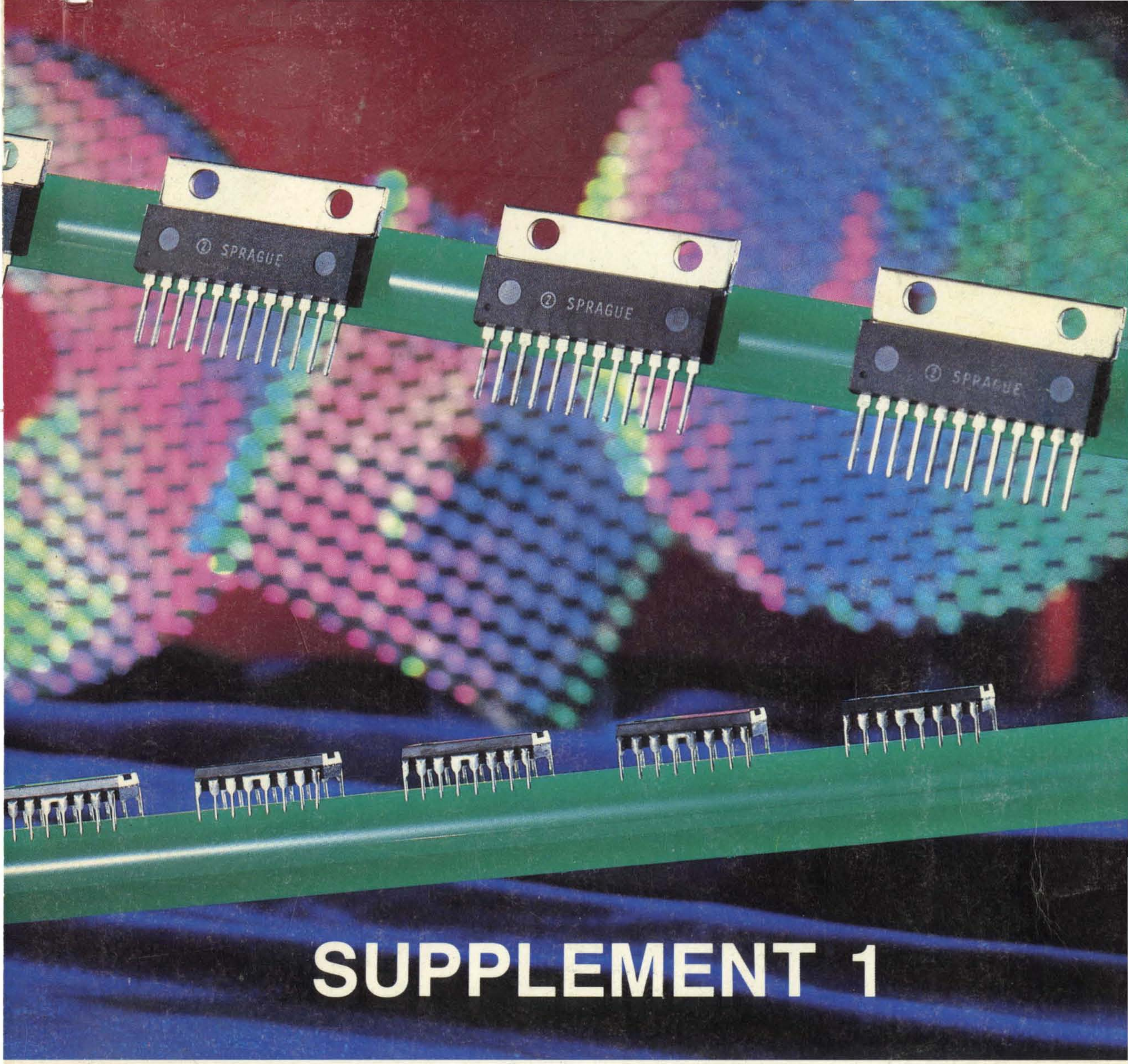

SUPPLEMENT 1

SPRAGUE
THE MARK OF RELIABILITY

INTEGRATED CIRCUITS

DATA BOOK
WR-503-1

Power Interface • **Linear** • **Hall Effect** • **Transistor Arrays**

SPRAGUE
THE MARK OF RELIABILITY

INTEGRATED CIRCUITS

INTERFACE

- High Voltage
- High Current
- BiMOS and Complex Arrays

LINEAR

- Radio/Communications
- Audio
- Power Supply Controllers

HALL EFFECT DEVICES

TRANSISTOR ARRAYS

□ □ □

SPRAGUE ELECTRIC COMPANY

INTERFACE AND LINEAR INTEGRATED CIRCUITS
115 Northeast Cutoff □ Worcester, Mass. 01606 □ 617/853-5000

DISCRETE SEMICONDUCTORS AND HALL EFFECT ICs
70 Pembroke Road □ Concord, N.H. 03301 □ 603/224-1961

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†Complete information is provided in Data Book WR-503.
*New product. Contact factory for information.

SECTION 3—HIGH-CURRENT INTERFACE DRIVERS

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†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 3—HIGH-CURRENT INTERFACE DRIVERS (Continued)

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 4—BiMOS AND COMPLEX ARRAY INTERFACE DRIVERS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 5—MILITARY AND AEROSPACE DEVICES

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 6—RADIO/COMMUNICATIONS INTEGRATED CIRCUITS

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†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.
®CQUAM (Compatible QUadrature Amplitude Modulation) is a registered trademark of Motorola, Inc.

SECTION 7—VIDEO AND TELEVISION INTEGRATED CIRCUITS

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†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

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†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 10B—TRANSISTOR ARRAYS AND MISCELLANEOUS DEVICES

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*New product. Contact factory for detailed information.

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†Complete information is provided in Data Book WR-503.

Product Index in Numerical Order

†Complete information is provided in Data Book WR-503.

Product Index (Continued)

†Complete information is provided in Data Book WR-503.
*New Product. Contact factory for detailed information.

Product Index (Continued)

†Complete information is provided in Data Book WR-503.
*New Product. Contact factory for detailed information.

Product Index (Continued)

†Complete information is provided in Data Book WR-503.
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Product Index (Continued)

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

Product Index (Continued)

†Complete information provided in Data Book WR-503.
*New product. Contact factory for detailed information.

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SECTION 1—GENERAL INFORMATION

Sprague Part Numbering System

UL N - 2046 A - 1

INSTRUCTIONS.
- 1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
- BU = BURNED-IN PARTS TO DOUBLE-DEUCE PROGRAM
- MIL = MILITARY GRADE WITH SCREENING (PACKAGES H, J, AND R ONLY)

PACKAGE DESIGNATION.
- A = PLASTIC, 14- THROUGH 40-PIN DUAL IN-LINE
- B = PLASTIC, 8- THROUGH 22-PIN DUAL IN-LINE SEMI-TAB
- C = UNPACKAGED CHIP
- CW = PROBED WAFER
- D = METAL CAN, 3-LEAD (TO-52)
- E = LEADLESS CHIP CARRIER (CONTACT FACTORY)
- H = GLASS/METAL HERMETIC, 8- THROUGH 40-PIN DUAL IN-LINE
- J = GLASS/METAL HERMETIC, 14-LEAD FLAT PACK
- L = PLASTIC SOIC (CONTACT FACTORY)
- M = PLASTIC, 8-PIN DUAL IN-LINE
- P = DIRECTLY REPLACED BY B PACKAGE
- Q = PLASTIC, 16-PIN QUAD IN-LINE
- R = CERAMIC/GLASS HERMETIC, 14- THROUGH 40-PIN DUAL IN-LINE
- S = PLASTIC, 4-LEAD SINGLE IN-LINE
- T = PLASTIC, 3-LEAD SINGLE IN-LINE
- U = PLASTIC, 3-LEAD THIN SINGLE IN-LINE
- V = METAL FLANGE MOUNT, 11-LEAD (TO-3)
- W = PLASTIC, 12-LEAD SINGLE IN-LINE POWER TAB
- Y = PLASTIC, 3-LEAD (TO-92)
- Z = PLASTIC, 5-LEAD SINGLE IN-LINE POWER TAB (TO-220)
- ZH = Z PACKAGE WITH FORMED LEADS FOR HORIZONTAL MOUNT
- ZV = Z PACKAGE WITH FORMED LEADS FOR VERTICAL MOUNT

DEVICE TYPE (FOUR DIGITS).

OPERATING AMBIENT TEMPERATURE RANGE.
- N = COMMERCIAL/INDUSTRIAL, SEE DETAIL SPECIFICATIONS
- Q = EXTENDED (−40°C TO +85°C)
- S = FULL MILITARY (−55°C TO +125°C)
- X = SPECIAL SIGNIFIER FOR PRE-PRODUCTION DEVICES

FAMILY (UC, UD, UG, UL, OR UT).

CROSS-REFERENCE in Numerical Order

The suggested Sprague replacement devices are based on similarity as shown in currently published data. Exact replacement in all applications is not guaranteed and the user should compare the specifications of the competitive and recommended Sprague replacement.

Manufacturers' Abbreviations:

AMI	American Microsystems
CS	Cherry Semiconductor
DI	Dionics, Inc.
EXR	Exar Integrated Systems
FSC	Fairchild Semiconductor
FUJ	Fujitsu
GE	General Electric
HIT	Hitachi Ltd.
IP	Integrated Power
ITT	ITT Semiconductors
MIT	Mitsubishi Electric Corp.
MOT	Motorola Semiconductor
NEC	Nippon Electric Co.
NS	National Semiconductor
OKI	Oki Semiconductor
PE	Pro-Electron‡
PLS	Plessey Semiconductor
RCA	RCA
RFA	Rifa
SANY	Sanyo
SG	Silicon General Inc.
SIEM	Siemens Corp.
SIG	Signetics Corp.
SIL	Siliconix
SGS	SGS/ATES
SPR	Sprague Electric Co.
THM	Thomson-CSF
TI	Texas Instruments
TLF	AEG-Telefunken
TOS	Toshiba Corp.
UNI	Unitrode

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
CA758E	RCA	ULN-3812A††
CA1190E	RCA	ULN-2290B
CA1190Q	RCA	ULN-2290Q
CA1524E	RCA	ULS-8124A
CA1724E	RCA	TPQ-3724
CA1725E	RCA	TPQ-3725
CA2002	RCA	ULN-3701ZV
CA2002M	RCA	ULN-3701ZH
CA2004	RCA	ULN-3702ZV
CA2004M	RCA	ULN-3702ZH
CA2111AE	RCA	ULN-2111A
CA2524E	RCA	ULQ-8124A
CA3045	RCA	ULS-2045R
CA3045F	RCA	ULS-2045R
CA3045L	RCA	ULS-2045H
CA3046	RCA	ULN-2046A
CA3054	RCA	ULN-2054A
CA3081	RCA	ULN-2081A
CA3082	RCA	ULN-2082A
CA3083	RCA	ULN-2083A
CA3086	RCA	ULN-2086A
CA3145	RCA	ULN-3812A
CA3146E	RCA	ULN-2046A-1
CA3183AE	RCA	ULN-2083A-1
CA3183E	RCA	ULN-2083A-1
CA3195E	RCA	ULN-3812A

††The ULN-3812A features a reduced output impedance.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
CA3219E	RCA	UDN-2541B
CA3524E	RCA	ULN-8124A
CA3724G	RCA	TPQ-3724
CA3725G	RCA	TPQ-3725
CS166	CS	ULN-2429A
DH3724CN	NS	TPQ-3724
DH3725CN	NS	TPQ-3725
DI302	DI	UDN-7183A
DI507	DI	UDN-6116A-1¶
DI509	DI	UDN-6116A-2¶
DI510	DI	UDN-6510A
DI512	DI	UDN-6514A
DI514	DI	UDN-6118A-2¶
DM3724CN	NS	TPQ-3724
DM3725CN	NS	TPQ-3725
DS3611N	NS	UDN-3611M
DS3612N	NS	UDN-3612M
DS3613N	NS	UDN-3613M
DS3614N	NS	UDN-3614M
FPQ2222	FSC	TPQ-2222
FPQ2907	FSC	TPQ-2907
FPQ3724	FSC	TPQ-3724
FPQ3725	FSC	TPQ-3725
FSA2619P	FSC	TND-908
FSA2719P	FSC	TND-903
GEL2113	GE	ULN-2111A
HA1199	HIT	ULN-2249A
HA1364	HIT	ULN-2290Q
HA12402	HIT	ULN-2204A
IP1526	IP	ULN-8126A
IP2064	IP	ULN-2064B
IP2065	IP	ULN-2065B

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
IP2066	IP	ULN-2066B
IP2067	IP	ULN-2067B
IP2068	IP	ULN-2068B
IP2069	IP	ULN-2069B
IP2070	IP	ULN-2070B
IP2071	IP	ULN-2071B
IP2074	IP	ULN-2074B
IP2075	IP	ULN-2075B
IP2076	IP	ULN-2076B
IP2077	IP	ULN-2077B
IP2524	IP	ULQ-8124A
IP2526	IP	ULQ-8126A
IP3524	IP	ULS-8124R
IP3526	IP	ULS-8126R
ITT552	ITT	ULN-2001A
ITT554	ITT	ULN-2002A
ITT556	ITT	ULN-2003A
ITT652	ITT	ULN-2001A
ITT654	ITT	ULN-2002A
ITT656	ITT	ULN-2003A
L165	SGS	ULN-3751Z
L201	SGS	ULN-2001A
L202	SGS	ULN-2002A
L203	SGS	ULN-2003A
L204	SGS	ULN-2004A
L272	SGS	(ULN-3755B)
L293	SGS	(UDN-2993B)
L295	SGS	(UDN-2965W)
L298	SGS	(UDN-2998W)
L601	SGS	ULN-2821A
L602	SGS	ULN-2822A
L603	SGS	ULN-2823A
L604	SGS	ULN-2824A
LA705PC	SANY	ULN-3812A††
LA758PC	SANY	ULN-3812A††
LA1160	SANY	ULN-2243A
LA3045	SANY	ULS-2045H

¶Sprague device includes internal pull-down resistors.
††The ULN-3812A features a reduced output impedance.
( )Functional equivalent only; improved performance but not pin compatible.

ompetitive art umber	Manufacturer	Suggested Sprague Replacement
A3046	SANY	ULN-2046A
A3086	SANY	ULN-2086A
B1231	SANY	ULN-2001A
B1232	SANY	ULN-2002A
B1233	SANY	ULN-2003A
B1234	SANY	ULN-2004A
M380N	NS	ULN-2280B
M383AT	NS	ULN-3702Z
M383T	NS	ULN-3701Z
M384N	NS	ULN-3784B
M1800N	NS	ULN-3812A††
M2002AT	NS	ULN-3702Z
M2002T	NS	ULN-3701Z
M2111N	NS	ULN-2111A
M2113N	NS	ULN-2111A
M3045D	NS	ULS-2045H
M3046N	NS	ULN-2046A
M3054N	NS	ULN-2054A
M3086N	NS	ULN-2086A
M3611N	NS	UDN-3611M
M3612N	NS	UDN-3612M
M3613N	NS	UDN-3613M
M3614N	NS	UDN-3614M
54523P	MIT	ULN-2003A
54524P	MIT	ULN-2001A
54525P	MIT	ULN-2002A
54526P	MIT	ULN-2004A
54532P	MIT	ULN-2064B
54562P	MIT	UDN-2982A
54563P	MIT	UDN-2981A
B3759C	FUJ	ULQ-8194R§
B3759P	FUJ	ULQ-8194A§
B3760C	FUJ	ULQ-8195R§
S3760P	FUJ	ULQ-8195A§
C1309	MOT	ULN-3809A
C1311P	MOT	ULN-3812A††

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
MC1344P	MOT	ULN-3812A††
MC1357P	MOT	ULN-2111A
MC1411L	MOT	ULN-2001R
MC1411P	MOT	ULN-2001A
MC1411TP	MOT	ULQ-2001A
MC1412L	MOT	ULN-2002R
MC1412P	MOT	ULN-2002A
MC1412TP	MOT	ULQ-2002A
MC1413L	MOT	ULN-2003R
MC1413P	MOT	ULN-2003A
MC1413TP	MOT	ULQ-2003A
MC1416L	MOT	ULN-2004R
MC1416P	MOT	ULN-2004A
MC1416TP	MOT	ULQ-2004A
MC1417P	MOT	UDN-2580A
MC1471P1	MOT	UDN-5711M
MC1472P1	MOT	UDN-5712M
MC1472U	MOT	UDN-5712R
MC1473P1	MOT	UDN-5713M
MC1474P1	MOT	UDN-5714M
MC3346	MOT	ULN-2046A
MC3359P	MOT	ULN-3859A
MC3386P	MOT	ULN-2086A
ML3045		ULS-2045H
ML3046		ULN-2046A
ML3086		ULN-2086A
MPQ2221	MOT	TPQ-2221
MPQ2222	MOT	TPQ-2222
MPQ2369	MOT	TPQ-2369
MPQ2483	MOT	TPQ-2483
MPQ2484	MOT	TPQ-2484
MPQ2906	MOT	TPQ-2906
MPQ2907	MOT	TPQ-2907
MPQ3724	MOT	TPQ-3724
MPQ3725	MOT	TPQ-3725
MPQ3725A	MOT	TPQ-3725A
MPQ3798	MOT	TPQ-3798
MPQ3799	MOT	TPQ-3799
MPQ3904	MOT	TPQ-3904
MPQ3906	MOT	TPQ-3906

§Sprague engineering bulletin in preparation.
††The ULN-3812A features a reduced output impedance.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
MPQ6001	MOT	TPQ-6001
MPQ6002	MOT	TPQ-6002
MPQ6100	MOT	TPQ-6100
MPQ6100A	MOT	TPQ-6100A
MPQ6501	MOT	TPQ-6501
MPQ6502	MOT	TPQ-6502
MPQ6600	MOT	TPQ-6600
MPQ6600A	MOT	TPQ-6600A
MPQ6700	MOT	TPQ-6700
MSL912R	OKI	UDN-6118A-2
N5111A	SIG	ULN-2111A
NA3086		ULN-2086A
NE564N	SIG	ULN-8564A§
NE564F	SIG	ULN-8564R§
NE594N	SIG	UDN-6118A-2
NE594F	SIG	UDN-6118R-2
NE5501N	SIG	ULN-2021A
NE5502N	SIG	ULN-2022A
NE5503N	SIG	ULN-2023A
NE5504N	SIG	ULN-2024A
NE5560F	SIG	ULN-8160R
NE5560N	SIG	ULN-8160A
NE5561N	SIG	ULN-8161M
NE5562F	SIG	ULN-8162R§
NE5562N	SIG	ULN-8162A§
NE5563F	SIG	ULN-8163R§
NE5563N	SIG	ULN-8163A
NE5601N	SIG	ULN-2001A
NE5602N	SIG	ULN-2002A
NE5603N	SIG	ULN-2003A
NE5604N	SIG	ULN-2004A
PBD352301J	RFA	ULN-2001R
PBD352301N	RFA	ULN-2001A
PBD352302J	RFA	ULN-2004R
PBD352302N	RFA	ULN-2004A
PBD352303J	RFA	ULN-2003R
PBD352303N	RFA	ULN-2003A
PBD352304J	RFA	ULN-2002R
PBD352304N	RFA	ULN-2002A
PBD352311N	RFA	ULN-2021A
PBD352312N	RFA	ULN-2024A
PBD352313N	RFA	ULN-2023A
PBD352314N	RFA	ULN-2022A
PBD353801J	RFA	ULN-2801R
PBD353802J	RFA	ULN-2804R
PBD353803J	RFA	ULN-2803R
PBD353804J	RFA	ULN-2802R
PWM25BK	SIL	ULQ-8125R§
PWM25CK	SIL	ULN-8125R§
PWM27BK	SIL	ULQ-8127R§
PWM27CK	SIL	ULN-8127R§
Q2T2222	TI	TPQ-2222
Q2T3725	TI	TPQ-3725
S4534	AMI	UCN-5810A
S4535	AMI	UCN-5818A
SA594F	SIG	UDQ-6118R-2§
SA594N	SIG	UDQ-6118A-2§
SE564F	SIG	ULS-8564R§
SE5560F	SIG	ULS-8160R
SE5560N	SIG	ULS-8160A
SE5561N	SIG	ULS-8161M
SE5562F	SIG	ULS-8162R§
SE5562N	SIG	ULS-8162A§
SE5563F	SIG	ULS-8163R§
SE5563N	SIG	ULS-8163A§
SFC2046E	THM	ULN-2046A
SFC2054EC	THM	ULN-2054A
SFC2086E	THM	ULN-2086A
SG1173	SG	ULN-3751Z
SG1524BJ	SG	ULS-8124R§
SG1524F	SIG	ULS-8124R§

§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SG1525AJ	SG	ULS-8125R§
SG1526J	SG	ULS-8126R
SG1527AJ	SG	ULS-8127R§
SG2001J	SG	ULS-2001R
SG2001N	SG	ULN-2001A
SG2002J	SG	ULS-2002R
SG2002N	SG	ULN-2002A
SG3081N	SG	ULN-2081A
SG3082N	SG	ULN-2082A
SG3083N	SG	ULN-2083A
SG3086N	SG	ULN-2086A
SG3146N	SG	ULN-2046A-1
SG3183N	SG	ULN-2083A-1
SG3524BJ	SG	ULN-8124R§
SG3524BN	SG	ULN-8124A§
SG3524N	SIG	ULN-8124A§
SG3525AJ	SG	ULN-8125R§
SG3525AN	SG	ULN-8125A§
SG3526J	SG	ULN-8126R
SG3526N	SG	ULN-8126A
SG3527AJ	SG	ULN-8127R§
SG3527AN	SG	ULN-8127A§
SG3635P	SG	UDN-2935Z
SG3638	SG	UDN-2976W
SG3643	SG	(UDN-2965W)
SG3821J	SG	ULS-2045H
SG3821N	SG	ULN-2046A
SG3822N	SG	ULN-2054A
SG3851J	SG	ULS-2011R
SG3851N	SG	ULN-2011A
SG3852J	SG	ULS-2012R
SG3852N	SG	ULN-2012A
SG3853J	SG	ULS-2013R
SG3853N	SG	ULN-2013A
SG3854J	SG	ULS-2014R
G3854N	SG	ULN-2014A
G3886N	SG	ULN-2086A
G6118N	SG	UDN-6118A

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SL3045C	PLS	ULS-2045R
SL3046C	PLS	ULN-2046A
SL3054	PLS	ULN-2054A
SL3081C	PLS	ULN-2081A
SL3082C	PLS	ULN-2082A
SL3083E	PLS	ULN-2083A
SL3086	PLS	ULN-2086A
SL3145E	PLS	ULS-2045H
SL3146E	PLS	ULN-2046A-1
SL3183E	PLS	ULN-2083A-1
SN75064NE	TI	ULN-2064B
SN75065NE	TI	ULN-2065B
SN75066NE	TI	ULN-2066B
SN75067NE	TI	ULN-2067B
SN75068NE	TI	ULN-2068B
SN75069NE	TI	ULN-2069B
SN75074NE	TI	ULN-2074B
SN75075NE	TI	ULN-2075B
SN75076NE	TI	ULN-2076B
SN75077NE	TI	ULN-2077B
SN75407P	TI	UDN-5732M
SN75437ND	TI	UDN-2541B
SN75465J	TI	ULN-2025R
SN75465N	TI	ULN-2025A
SN75466J	TI	ULN-2021R
SN75466N	TI	ULN-2021A
SN75467J	TI	ULN-2022R
SN75467N	TI	ULN-2022A
SN75468J	TI	ULN-2023R
SN75468N	TI	ULN-2023A
SN75469J	TI	ULN-2024R
SN75469N	TI	ULN-2024A
SN75471P	TI	UDN-3611M†
SN75472P	TI	UDN-3612M†
SN75473P	TI	UDN-3613M†
SN75474P	TI	UDN-3614M†
SN75475P	TI	UDN-5712M†
SN75476P	TI	UDN-5711M†
SN75477P	TI	UDN-5722M†

†Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.
§Sprague engineering bulletin in preparation.
( )Functional equivalent only; improved performance but not pin compatible.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SN75478P	TI	UDN-5713M†
SN75479P	TI	UDN-5714M†
SN75518N	TI	UCN-5818A
SN75551FN	TI	UCN-5851EP
SN75552FN	TI	UCN-5852EP
SN75553FN	TI	UCN-5853EP
SN75554FN	TI	UCN-5853EP
SN75605K	TI	UDN-2950Z
SN76116N	TI	ULN-3812A††
SN76642N	TI	ULN-2111A
SN76643N	TI	ULN-2111A
SP3724QD	TI	TPQ-3724
SP3725QD	TI	TPQ-3725
TA7272P	TOS	(ULN-3755W)
TA7613P	TOS	ULN-2204A
TAA930		ULN-2111A
TCA365	SIEM	(ULN-3751Z)
TD62001AP	TOS	ULN-2001A
TD62001P	TOS	ULN-2001A
TD62002AP	TOS	ULN-2002A
TD62002P	TOS	ULN-2002A
TD62003AP	TOS	ULN-2003A
TD62003P	TOS	ULN-2003A
TD62004AP	TOS	ULN-2004A
TD62004P	TOS	ULN-2004A
TD62064AP	TOS	ULN-2064B
TD62064P	TOS	ULN-2064B
TD62074AP	TOS	ULN-2074B
TD62074P	TOS	ULN-2074B
TD62081AP	TOS	ULN-2801A
TD62082AP	TOS	ULN-2802A
TD62083	TOS	ULN-2803A
TD62084AP	TOS	ULN-2804A
TD62101P	TOS	ULN-2001A
TD62103P	TOS	ULN-2003A
TD62104P	TOS	ULN-2004A
TD62479P	TOS	UDN-5714M
TD62781AP	TOS	UDN-6118A-2

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
TD62782AP	TOS	UDN-6128A-2
TDA1060	PE	ULN-8160A
TDA1083	PE	ULN-2204A
TDA1170	PE	ULN-2270Q
TDA1190P	PE	ULN-2290B
TDA1190Z	PE	ULN-2290Q
TDA2002	PE	ULN-3701Z
TDA2002A	PE	ULN-3702Z
TDA2002H	PE	ULN-3701ZH
TDA2002V	PE	ULN-3701ZV
TDA2003H	PE	ULN-3703ZH
TDA2003V	PE	ULN-3703ZV
TDA2008V	PE	ULN-3702ZV
TDA3190	PE	ULN-2290B
TDA3190P	PE	ULN-2290B
TID121	TI	TND-933
TID122	TI	TND-940
TID123	TI	TND-938
TID124	TI	TND-939
TL494CJ	TI	ULN-8194R§
TL494CN	TI	ULN-8194A
TL494IJ	TI	ULQ-8194R§
TL494IN	TI	ULQ-8194A§
TL494MJ	TI	ULS-8194R§
TL495CJ	TI	ULN-8195R§
TL495CN	TI	ULN-8195A
TL495IJ	TI	ULQ-8195R§
TL495IN	TI	ULQ-8195A§
TL594CJ	TI	ULN-8194R§
TL594CN	TI	ULN-8194A
TL594IJ	TI	ULQ-8194R§
TL594IN	TI	ULQ-8194A§
TL594MJ	TI	ULS-8194R§
TL595CJ	TI	ULN-8195R§
TL595CN	TI	ULN-8195A
TL595IJ	TI	ULQ-8195R§
TL595IN	TI	ULQ-8195A§
TL595MJ	TI	ULS-8195R§

†Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.
§Sprague engineering bulletin in preparation.
††The ULN-3812A features a reduced output impedance.
( )Functional equivalent only; improved performance but not pin compatible.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
U6A758394	FSC	ULN-3812A††
U417B	TLF	ULN-2204A
UA705PC	FSC	ULN-3812A††
UA758PC	FSC	ULN-3812A††
UA3045DM	FSC	ULS-2045H
UA3046PC	FSC	ULN-2046A
UA3054PC	FSC	ULN-2054A
UA3086PC	FSC	ULN-2086A
UA7327	FSC	ULN-2270B
UC494AJ	UNI	ULS-8194R
UC494ACJ	UNI	ULN-8194R
UC494ACN	UNI	ULN-8194A
UC495AJ	UNI	ULS-8195R
UC495ACJ	UNI	ULN-8195R
UC495ACN	UNI	ULN-8195A
UC1524AJ	UNI	ULS-8124R§
UC1525AJ	UNI	ULS-8125R§
UC1526J	UNI	ULS-8126R
UC1527AJ	UNI	ULS-8127R§
UC2524AJ	UNI	ULQ-8124R§
UC2524AN	UNI	ULQ-8124A§
UC2525AJ	UNI	ULQ-8125R§
UC2525AN	UNI	ULQ-8125A§
UC2526J	UNI	ULQ-8126R
UC2526N	UNI	ULQ-8126A
UC2527AJ	UNI	ULQ-8127R§
UC2527AN	UNI	ULQ-8127A§
UC3524AJ	UNI	ULN-8124R§
UC3524AN	UNI	ULN-8124A§
UC3525AJ	UNI	ULN-8125R§
UC3525AN	UNI	ULN-8125A§
UC3526J	UNI	ULN-8126R
UC3526N	UNI	ULN-8126A
UC3527AJ	UNI	ULN-8127R§
UC3527AN	UNI	ULN-8127A§
UC3717	UNI	(UDN-2953B)
UC494ACJ	UNI	ULN-8194R§

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
UC494ACN	UNI	ULN-8194A
UC494AJ	UNI	ULS-8194R§
UC495ACJ	UNI	ULN-8195R§
UC495ACN	UNI	ULN-8195A
UC495AJ	UNI	ULS-8195R§
UCN-4810A	SPR	UCN-5810A
UCN4810N	TI	UCN-5810A
UCN-4815A	SPR	UCN-5815A
UDN2841B	MOT	UDN-2841B
UDN2841NE	TI	UDN-2841B
UDN2845B	MOT	UDN-2845B
UDN2845NE	TI	UDN-2845B
UDN5711N	TI	UDN-5711M
UDN5712N	TI	UDN-5712M
UDN5713N	TI	UDN-5713M
UDN5714N	TI	UDN-5714M
UDN-6126A	SPR	UDN-6116A
UDN-6148A	SPR	UDN-6138A
UDN-6164A	SPR	UDN-6116A-1
UDN-6184A	SPR	UDN-6118A-1
UHC-400	SPR	UDS-0400J
UHC-400-1	SPR	UDS-0400J-1
UHC-402	SPR	UDS-0402J
UHC-402-1	SPR	UDS-0402J-1
UHC-403	SPR	UDS-0403J
UHC-403-1	SPR	UDS-0403J-1
UHC-406	SPR	UDS-0406J
UHC-406-1	SPR	UDS-0406J-1
UHC-407	SPR	UDS-0407J
UHC-407-1	SPR	UDS-0407J-1
UHC-408	SPR	UDS-0408J

§Sprague engineering bulletin in preparation.
††The ULN-3812A features a reduced output impedance.
( )Functional equivalent only; improved performance but not pin compatible.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
UHC-408-1	SPR	UDS-0408J-1
UHC-432	SPR	UDS-0432J
UHC-432-1	SPR	UDS-0432J-1
UHC-433	SPR	UDS-0433J
UHC-433-1	SPR	UDS-0433J-1
UHC-500	SPR	UDS-0500J
UHC-502	SPR	UDS-0502J
UHC-503	SPR	UDS-0503J
UHC-506	SPR	UDS-0506J
UHC-507	SPR	UDS-0507J
UHC-508	SPR	UDS-0508J
UHC-532	SPR	UDS-0532J
UHC-533	SPR	UDS-0533J
UHD-400	SPR	UDS-0400H
UHD-400-1	SPR	UDS-0400H-1
UHD-402	SPR	UDS-0402H
UHD-402-1	SPR	UDS-0402H-1
UHD-403	SPR	UDS-0403H
UHD-403-1	SPR	UDS-0403H-1
UHD-406	SPR	UDS-0406H
UHD-406-1	SPR	UDS-0406H-1
UHD-407	SPR	UDS-0407H
UHD-407-1	SPR	UDS-0407H-1
UHD-408	SPR	UDS-0408H
UHD-408-1	SPR	UDS-0408H-1
UHD-432	SPR	UDS-0432H
UHD-432-1	SPR	UDS-0432H-1
UHD-433	SPR	UDS-0433H
UHD-433-1	SPR	UDS-0433H-1
UHD-500	SPR	UDS-0500H
UHD-502	SPR	UDS-0502H
UHD-503	SPR	UDS-0503H
UHD-506	SPR	UDS-0506H
UHD-507	SPR	UDS-0507H
UHD-508	SPR	UDS-0508H
UHD-532	SPR	UDS-0532H
UHD-533	SPR	UDS-0533H
ULN2001A	MOT	ULN-2001A
ULN2001A	SGS	ULN-2001A

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
ULN2001AJ	TI	ULN-2001R
ULN2001AN	TI	ULN-2001A
ULN2002A	MOT	ULN-2002A
ULN2002A	SGS	ULN-2002A
ULN2002AJ	TI	ULN-2002R
ULN2002AN	TI	ULN-2002A
ULN2003A	MOT	ULN-2003A
ULN2003A	SGS	ULN-2003A
ULN2003AJ	TI	ULN-2003R
ULN2003AN	TI	ULN-2003A
ULN2003F	SIG	ULN-2003R
ULN2003N	SIG	ULN-2003A
ULN2004A	MOT	ULN-2004A
ULN2004A	SGS	ULN-2004A
ULN2004AJ	TI	ULN-2004R
ULN2004AN	TI	ULN-2004A
ULN2004F	SIG	ULN-2004R
ULN2004N	SIG	ULN-2004A
ULN2005AJ	TI	ULN-2005R
ULN2005AN	TI	ULN-2005A
ULN2064B	MOT	ULN-2064B
ULN2064B	SGS	ULN-2064B
ULN2064NE	TI	ULN-2064B
ULN2065B	MOT	ULN-2065B

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Competitive Part Number	Manufacturer	Suggested Sprague Replacement
ULN2065B	SGS	ULN-2065B
ULN2065NE	TI	ULN-2065B
ULN2066B	MOT	ULN-2066B
ULN2066B	SGS	ULN-2066B
ULN2066NE	TI	ULN-2066B
ULN2067B	MOT	ULN-2067B
ULN2067B	SGS	ULN-2067B
ULN2067NE	TI	ULN-2067B
ULN2068B	MOT	ULN-2068B
ULN2068B	SGS	ULN-2068B
ULN2068NE	TI	ULN-2068B
ULN2069B	MOT	ULN-2069B
ULN2069B	SGS	ULN-2069B
ULN2069NE	TI	ULN-2069B
ULN2070B	SGS	ULN-2070B
ULN2071B	SGS	ULN-2071B
ULN2074B	MOT	ULN-2074B
ULN2074B	SGS	ULN-2074B
ULN2074NE	TI	ULN-2074B
ULN2075B	MOT	ULN-2075B
ULN2075B	SGS	ULN-2075B

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
ULN2075NE	TI	ULN-2075B
ULN2076B	SGS	ULN-2076B
ULN2077B	SGS	ULN-2077B
ULN2801A	MOT	ULN-2801A
ULN2801A	SGS	ULN-2801A
ULN2802A	MOT	ULN-2802A
ULN2802A	SGS	ULN-2802A
ULN2803A	MOT	ULN-2803A
ULN2803A	SGS	ULN-2803A
ULN2804A	MOT	ULN-2804A
ULN2804A	SGS	ULN-2804A
ULN2805A	SGS	ULN-2805A
ULN-2113A	SPR	ULN-2111A
ULN-2244A	SPR	ULN-3812A††
ULN-2245A	SPR	ULN-3812A
ULN-2281B	SPR	ULN-3784B
ULN-3006M	SPR	UGN-3201M
ULN-3006T	SPR	UGN-3019T
ULN-3007M	SPR	UGN-3203M
ULN-3008M	SPR	UGN-3501M
ULN-3008T	SPR	UGN-3501T
ULN-3100M	SPR	UGN-3600M
ULN-3101M	SPR	UGN-3601M
ULN-3330Y-2	SPR	ULN-3330Y
ULS-3006T	SPR	UGS-3019T
UPA2001C	NEC	ULN-2001A
UPA2002C	NEC	ULN-2002A
UPA2003C	NEC	ULN-2003A
UPA2004C	NEC	ULN-2004A

††The ULN-3812A features a reduced output impedance.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
US5438A	SPR	UDS-0408H
US5438J	SPR	UDS-0408J
US5439J	SPR	UDS-0408J
US7438A	SPR	UHP-0408
US7438J	SPR	UDS-0408J
US7439J	SPR	UDS-0408J
XR1800P	EXR	ULN-3812A††
XR2001CN	EXR	ULN-2001R
XR2001P	EXR	ULQ-2001A§
XR2002CN	EXR	ULN-2002R
XR2002P	EXR	ULQ-2002A§
XXR2003CN	EXR	ULN-2003R
XR2003P	EXR	ULQ-2003A§
XR2004CN	EXR	ULN-2004R
XR2004P	EXR	ULQ-2004A§
XR2011CN	EXR	ULN-2011R
XR2011CP	EXR	ULN-2011A
XR2012CN	EXR	ULN-2012R
XR2012CP	EXR	ULN-2012A
XR2013CN	EXR	ULN-2013R
XR2013CP	EXR	ULN-2013A
XR2014CN	EXR	ULN-2014R
XR2014CP	EXR	ULN-2014A
XR2201CP	EXR	ULN-2001A
XR2202CP	EXR	ULN-2002A
XR2203CP	EXR	ULN-2003A
XR2204CP	EXR	ULN-2004A
XR2205CP	EXR	ULN-2005A
XR6118P	EXR	UDN-6118A
XR6128P	EXR	UDN-6128A
ZN1060	FER	ULN-8160A
552	ITT	ULN-2001A
554	ITT	ULN-2002A
556	ITT	ULN-2003A
652	ITT	ULN-2001A
654	ITT	ULN-2002A
656	ITT	ULN-2003A
9665DC	FSC	ULN-2001R
9665DM	FSC	ULS-2001R
9665PC	FSC	ULN-2001A
9666DC	FSC	ULN-2002R
9666DM	FSC	ULS-2002R
9666PC	FSC	ULN-2002A
9667DC	FSC	ULN-2003R
9667DM	FSC	ULS-2003R
9667PC	FSC	ULN-2003A
9668DC	FSC	ULN-2004R
9668DM	FSC	ULS-2004R
9668PC	FSC	ULN-2004A

††The ULN-3812A features a reduced output impedance.

HOW TO ORDER

TO PLACE AN ORDER, obtain price and delivery information, or request additional technical literature, call or write your local sales office (see inside back cover) or:

From U.S.A.	Sprague Electric Co. 92 Hayden Avenue Lexington, MA (617) 862-5500 Telex: 710-321-0021
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REQUESTS FOR additional technical information on standard or custom devices may be sent to the appropriate manufacturing facility:

For all monolithic integrated circuits except Hall effect devices,

Sprague Electric Co.
115 Northeast Cutoff
Worcester, MA 01606
(617) 853-5000
Telex: 710-340-6304

For discrete semiconductors and Hall Effect devices,

Sprague Electric Co.
70 Pembroke Road
Concord, NH 03301
(603) 224-1961
Telex: 710-361-1495

CURRENT-SINK DRIVERS

In Order of (1) Output-Current rating
(2) Output-Voltage rating
(3) Number of Drivers

TYPICAL APPLICATIONS													
DISPLAYS				INDUCTIVE LOADS		PRINTERS		OUTPUTS*					
LED	Vacuum-Fluorescent	Gas-Discharge	Incan-descent	Solenoids	Motors	Thermal	Electro-sensitive	mA	V	Number	Part Number	Hermetic MIL-Part Available	Sprague Engineerin Bulletin
—	—	X	—	—	—	—	—	20	−115	8	Series UDN-7180A	—	29311
		TF Electroluminescent Display Row Driver						80	225	32	UCN-5851/52A/EP	—	26187
X	—	—	X	—	—	—	—	100	20	8¶	UDN-2595A	X	29320
X	—	—	X	—	—	X	—		30	32§	UCN-5833A	—	—
X	—	—	X	—	—	X	—		40	32¶§	UCN-5832A/C	—	26185.10
		3-Line to 8-Line Decoder/Driver						150	50	8¶†	UCN-4807A	—	26186
—	—	X	—	X	X	—	—	200	200	8	UDN-6540B	—	29301.10
X	—	—	X	X	X	X	—	250	40	4¶	Series UHP-400	X	29300
X	—	—	X	X	X	X	—		70	4¶	Series UHP-400-1	X	29300
X	—	—	X	X	X	X	—		100	4¶	Series UHP-500	X	29300
X	—	—	X	X	X	X	—	300	80	2¶	Series UDN-3610M	X	29308
X	—	—	X	X	X	X	—		80	2¶	Series UDN-5710M	X	29307
X	—	—	X	X	X	X	—		80	4¶	Series UDN-5700A	X	29306
—		Pin Diode Driver			—	—	—		120	4	UDN-5791A	X	29315
X	—	—	X	X	X	X	X	350	50	4†	UCN-5800A	X	26180
X	—	—	X	X	X	X	—		50	7	Series ULN-2000A	X	29304
X	—	—	X	X	X	X	—		50	8	Series ULN-2800A	X	29304.3
X	—	—	X	X	X	X	—		50	8¶	UDN-2596/98A	—	29320.2
X	—	—	X	X	X	X	X		50	8†	UCN-5801A	X	26180
X	—	—	X	X	—	X	X		50	8†	UCN-5821A	X	26185.12
		4-Line to 16-Line Decoder/Driver							60	16†	UCN-5816A	—	26186.10
X	—	—	X	X	X	X	—		70	2¶	Series UDN-5720M	—	29307.2
—	—	—	X	X	—	—	X		80	8†	UCN-5822A	X	26185.12
X	—	X	X	X	X	X	—		95	7	Series ULN-2020A	X	29304
X	—	X	X	X	X	X	—		95	8	Series ULN-2820A	X	29304.3
—	—	X	X	X	—	—	X		100	8§	UCN-5823A	X	26185.12
—	—	X	X	X	X	—	—		150	4†	UCN-5900A	X	26180.12
—	—	X	X	X	X	—	—		150	8†	UCN-5901A	X	26180.12
		Stepper Motor Translator/Driver						500	20	4	UCN-4202A	—	26184
		Stepper Motor Translator/Driver							50	4	UCN-4203A	—	26184
X	—	—	X	X	X	X	—		50	7	Series ULN-2010A	X	29304
X	—	—	X	X	X	X	—		50	8	Series ULN-2810A	X	29304.3
		3-Line to 8-Line Decoder/Driver							50	8¶†	UCN-4808A	X	26186
X	—	—	X	X	X	X	—		70	2¶	Series UDN-5750M	X	29307.4
X	—	—	X	X	X	X	—	600	70	2¶	Series UDN-5740M	—	29307.4
X	—	—	X	X	X	X	—	750	50	8¶	UDN-2597/99A	—	29320.2
X	—	—	X	X	X	—	—	1000	50	4†	UCN-5813/14B	—	26180.14
X	—	—	X	X	X	—	—		80	4¶	UDN-2542B	—	29317
X	—	—	X	X	X	—	—		80	4†	UCN-5813/14B-1	—	26180.14
		Stepper Motor Translator/Driver						1250	20	4	UCN-4204B	—	26184.10
X	—	—	X	X	X	—	—		50	2	ULN-2061M	—	29305
X	—	—	X	X	X	—	—		50	4	Series ULN-2064B	X	29305
		Stepper Motor Translator/Driver							50	4	UCN-4205B	—	26184.10
X	—	—	X	X	X	—	—		60	4¶	UDN-2541B	—	29317
X	—	—	—	X	X	—	X	1500	−50	4	UDN-2841/45B	—	29314
X	—	—	X	X	X	—	—		80	2	ULN-2062M	—	29305
X	—	—	X	X	X	—	—		80	4	Series ULN-2065B	X	29305
—	—	—	X	X	X	—	—	1750	60	4§	UCN-5825B	—	26185.3
—	—	—	X	X	X	—	—		80	4§	UCN-5826B	—	26185.3
—	—	—	X	X	X	—	—	2000	80	4	UDN-2545B	—	29317.10
X	—	—	X	X	X	—	—	4000	50	4	UDN-2878W	—	29305.10
X	—	—	X	X	X	—	—		80	4	UDN-2879W	—	29305.10

*Current is maximum tested condition. Voltage is absolute maximum rating.
†Latched Drivers.
§Serial-input, latched parallel outputs.
¶Saturated, non-Darlington outputs for minimum voltage drop.

CURRENT-SOURCE DRIVERS

In Order of (1) Output-Current rating
(2) Output-Voltage rating
(3) Number of Drivers

TYPICAL APPLICATIONS: DISPLAYS				INDUCTIVE LOADS		PRINTERS		OUTPUTS*					
LED	Vacuum-Fluorescent	Gas-Discharge	Incan-descent	Solenoids	Motors	Thermal	Electro-sensitive	mA	V	Number	Part Number	Hermetic MIL-Part Available	Sprague Engineering Bulletin
—	X	—	—	—	—	—	—	−25	±40	8	UDN-6138A	—	29313
X	X	7-Segment Decoder/Driver							60	8†	UCN-4805A	—	26181
X	X	—	—	—	—	X	—		60	8†	UCN-5815A	X	26183.10
X	X	—	—	—	—	X	—		60	10§	UCN-5810A	X	26182
X	X	—	—	—	—	X	—		60	20§	UCN-5812A	X	26182
X	X	—	—	—	—	X	—		60	32§	UCN-5818A	X	26182
—	X	X	—	—	—	X	—		80	8†	UCN-5815A-1	X	26183
X	X	X	—	—	—	X	—		80	10§	UCN-5810A-1	X	26182
X	X	X	—	—	—	X	—		80	20§	UCN-5812A-1	X	26182
X	X	X	—	—	—	X	—		80	32§	UCN-5818A-1	X	26182
		TF Electroluminescent Display Column Driver							80	32	UCN-5853/54A/EP	—	—
—	X	—	—	—	—	—	—		85	6	UDN-6116A	X	29313
—	X	—	—	—	—	—	—		85	8	UDN-6118/28A	X	29313
—	X	X	—	—	—	—	—		115	6	UDN-6116A-1	—	29313
—	X	X	—	—	—	—	—		115	8	UDN-6118/28A-1	—	29313
—	X	X	—	—	—	—	—		140	8	UDN-6514A	—	29313.3
—	X	X	—	—	—	—	—		200	8	UDN-6510A	—	29313.3
—	X	X	—	—	—	—	—	−40	150	10§	UCN-5910A	X	26182.2
X	—	—	X	X	X	X	—	−120	±25	8¶	UDN-2585A	—	29316
X	—	—	X	X	X	X	—		30	8¶	UDN-2985/86A	—	29310.2
X	—	—	X	X	X	X	X		50	8§¶	UCN-5895A	—	26182.14
X	—	—	X	X	—	—	—	−350	−50	8	UDN-2580A	—	29316
X	—	—	X	X	—	—	—		−50	8	UDN-2588A	—	29316
X	—	—	X	X	X	X	X		50	8	UDN-2981/82A	X	29310
X	—	—	X	X	X	X	X		50	8§	UCN-5891A/B	—	26182.12
—	—	—	—	X	—	—	—		−80	5	UDN-2956/57A	—	29309
X	—	—	X	X	X	X	X		80	8§	UCN-5890A/B	—	26182.12
X	X	—	X	X	X	X	X		80	8	UDN-2983/84A	X	29310
X	X	—	X	X	—	—	—		−80	8	UDN-2580A-1	X	29316
X	—	—	X	X	—	—	—		−80	8	UDN-2588A-1	X	29316
X	—	—	X	X	X	—	—	−1500	35	4	UDN-2941B/W	—	29310.10
X	—	—	—	X	X	—	X		−50	4	UDN-2845B	—	29314
—	—	—	X	X	X	—	—	−4000	60	4	UDN-2944W	—	29310.20
—	—	—	X	X	X	—	—		60	4	UDN-2948W	—	29309.10

*Current is maximum tested condition. Voltage is absolute maximum rating.
†Latched Drivers.
§Serial-input, latched parallel outputs.
¶Saturated, non-Darlington outputs for minimum voltage drop.

SINK/SOURCE DRIVERS

In Order of (1) Output-Current rating
(2) Output-Voltage rating
(3) Number of Drivers

TYPICAL APPLICATIONS: DISPLAYS				INDUCTIVE LOADS		PRINTERS		OUTPUTS*					
LED	Vacuum-Fluorescent	Gas-Discharge	Incan-descent	Solenoids	Motors	Thermal	Electro-sensitive	mA	V	Number	Part Number	Hermetic MIL-Part Available	Sprague Engineering Bulletin
—	Full-Bridges			—	X	—	—	±500	40	2	UDN-2993B	—	29319.5
—	Half-Bridges			—	X	—	—	±800	30	3¶	UDN-2933/34B	—	29318.10
—	Half-Bridge			—	X	—	—	±1000	26	1	UDN-2943Z	—	29318.4
	Power Operational Amplifier				X	—	—		28	1	ULN-3751B/Z	—	27118.1
	Power Operational Amplifier				X	—	—		34	1	ULN-3751B/Z-1	—	27118.1
	Power Operational Amplifiers				X	—	—		40	2	ULN-3755B/W	—	27118.10
—	Half-Bridge			—	X	—	—	±2000	30	1	UDN-2935/50Z	—	29318.3
—	Full-Bridge			—	X	—	—		40	1	UDN-2952B/W	—	29319
—	Full-Bridge			—	X	—	—		50	1	UDN-2953B/W	—	29319.2
—	Full-Bridges			—	X	—	—		50	2	UDN-2998W	—	29319.6
—	—	—	—	X	—	—	—	±4000	50	2	UDN-2975W	—	29319.10
—	—	—	—	X	—	—	—		60	2	UDN-2976W	—	29319.10
—	PWM Control			X	X	—	—		60	2	UDN-2965W	—	29319.11

*Current is maximum tested condition. Voltage is absolute maximum rating.
¶Saturated, non-Darlington outputs for minimum voltage drop.

SECTION 2—HIGH-VOLTAGE INTERFACE DRIVERS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for information.

SELECTION GUIDE TO HIGH-VOLTAGE INTERFACE DRIVERS

Device Type	Absolute Maximum Ratings I_{OUT}	Absolute Maximum Ratings V_{OUT}	Outputs
UHP-500 through 533†	500 mA	100 V	Sink 4
UCN-5823 and 5843A*	500 mA	100 V	Sink 8
UCN-5851A/EP*	80 mA	225 V	Sink 32
UCN-5852A/EP*	80 mA	225 V	Sink 32
UCN-5900A*	400 mA	150 V	Sink 4
UCN-5901A*	400 mA	150 V	Sink 8
UCN-5910A*	50 mA	150 V	Source 10
UDN-6116A/R	−40 mA	85 V	Source 6
UDN-6116A-1	−40 mA	115 V	Source 6
UDN-6116A/R-2	−40 mA	65 V	Source 6
UDN-6118A/R	−40 mA	85 V	Source 8
UDN-6118A-1	−40 mA	115 V	Source 8
UDN-6118A/R-2	−40 mA	65 V	Source 8
UDN-6126A/R	−40 mA	85 V	Source 6
UDN-6126A-1	−40 mA	115 V	Source 6
UDN-6126A/R-2	−40 mA	65 V	Source 6
UDN-6128A/R	−40 mA	85 V	Source 8
UDN-6128A-1	−40 mA	115 V	Source 8
UDN-6128A/R-2	−40 mA	65 V	Source 8
UDN-6138A	−40 mA	±40 V	Source 8
UDN-6138A-2	−40 mA	±30 V	Source 8
UDN-6148A	−40 mA	±40 V	Source 8
UDN-6148A-2	−40 mA	±30 V	Source 8
UDN-6510A/R	−40 mA	200 V	Source 8
UDN-6514A/R	−40 mA	140 V	Source 8
UDN-6540B	200 mA	200 V	Sink 8
ULN-7001 through 7005A	300 mA	150 V	Sink 7
UDN-7180A	20 mA	−115 V	Sink 8
UDN-7183A	3.25 mA	−115 V	Sink 8
UDN-7184A	2.0 mA	−115 V	Sink 8
UDN-7186A	1.0 mA	−115 V	Sink 8

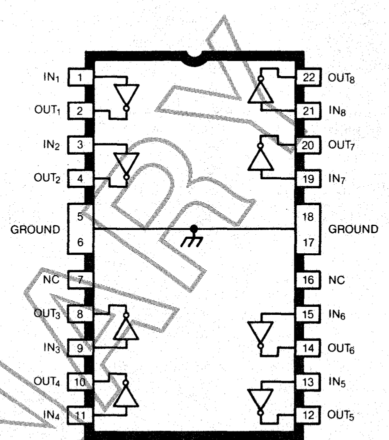
†See Section 3.
*Smart Power, see Section 4.

2

UDN-6540B
8-CHANNEL DMOS HIGH-VOLTAGE DRIVER

FEATURES

- Output Voltage 200 V
- CMOS, PMOS and HV Open Collector TTL Compatible Inputs
- Internal Gate Limiting Resistors
- Diode Clamp Inputs and Outputs
- High-Voltage DMOS Technology
- Superior Output SOA over Conventional Bipolar Technology

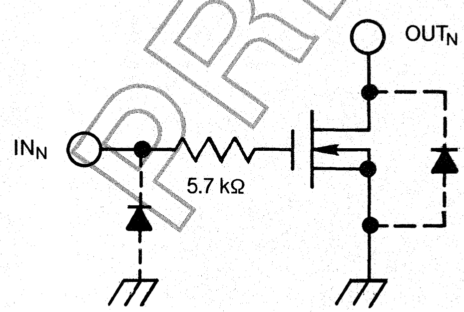


The UDN-6540B is an eight-channel high-voltage DMOS driver capable of sinking 200 mA and maintaining an output OFF voltage of 200 V. This device has many possible applications such as driving piezo electric elements, gas discharge or electroluminescent displays, and other high-voltage power loads. This device is input compatible with 7-20 V logic such as PMOS, CMOS, and high-voltage open collector TTL.

The UDN-6540B is packaged in a 22-pin dual in-line with 0.400″ row centers with heat-sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat-sinks for increased power dissipation with standard IC sockets and printed wiring boards.

PARTIAL SCHEMATIC DIAGRAM

One of Eight Drivers



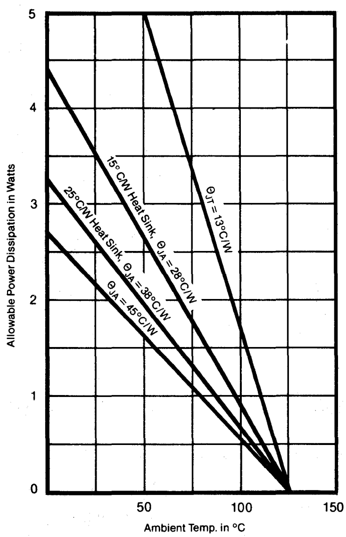
ABSOLUTE MAXIMUM RATINGS at $T_A = 25°C$

Output Voltage, V_{DS}	200 V
Input Voltage, V_{IN}	20 V
Output Current, I_{OUT}	200 mA
Power Dissipation,	
One Driver	0.5 W
Total Package	2.77W
Operating Temperature Range, T_A	−20°C to +85°C

*Derate at the rate of 22 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{DSS}	$V_{DS} = 200$ V, Gate shorted to source	—	10	μA
Drain to Source ON Voltage	$V_{DS(ON)}$	$V_{GS} = 10$ V, $I_{OUT} = 100$ mA	—	2.5	V
		$V_{GS} = 10$ V, $I_{OUT} = 200$ mA	—	4.0	V
		$V_{GS} = 15$ V, $I_{OUT} = 200$ mA	—	3.0	V
Input Threshold Voltage	V_{TH}	$I_{OUT} = 10$ mA, $V_{DS} = 0.5$ V	—	7.0	V
		$I_{OUT} = 50$ mA, $V_{DS} = 1.0$ V	—	8.5	V
Turn-On Delay	t_{ON}	0.5 E_{IN} to 0.5 E_{OUT}, $R_L = 1$ kΩ, $V_{OUT} = 100$ V	—	0.5	μs
Turn-Off Delay	t_{OFF}	0.5 E_{IN} to 0.5 E_{OUT}, $R_L = 1$ kΩ, $V_{OUT} = 100$ V	—	0.5	μs



SERIES ULN-7000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

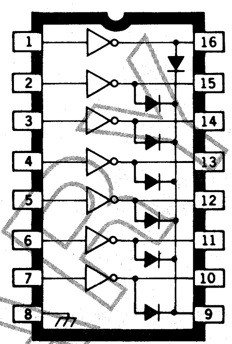
These high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

Series ULN-7001A devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.

Series ULN-7002A is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-7003A has a 2.7 kΩ series base resistor for each Darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs—particularly those beyond the capabilities of standard logic buffers.

Series ULN-7004A has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-7003A, while the required input voltage is less than that required by Series ULN-7002A.

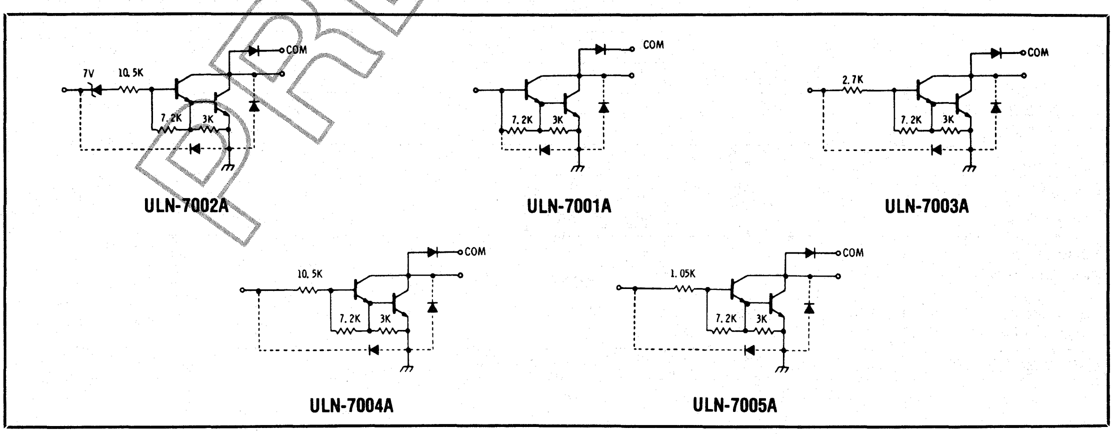


Series ULN-7005A is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 250 mA when driven from a ''totem pole'' logic output.

Series ULN-7000A is the original high-voltage, high-current Darlington Array. The output transistors are capable of sinking 300 mA and will sustain at least 150 V in the OFF state. Outputs may be paralleled for higher load-current capability.

All Series ULN-7000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These devices can also be supplied in a hermetic dual in-line package for use in military and aerospace applications.

PARTIAL SCHEMATICS



ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} . . . . 150 V
Input Voltage,
V_{IN} (ULN-7002/7003/7004A) . . . . 30 V
(ULN-7005A) . . . . 15 V
Continuous Collector Current, I_C . . . . 300 mA
Continuous Input Current, I_{IN} . . . . 25 mA
Power Dissipation, P_D (total package) . . . . 2.0 W*
Operating Ambient Temperature Range, T_A . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +150°C

*Derate at rate of 16.67 mW/°C above 25°C.

Device Number Designation

$V_{CE(MAX)}$ / $I_{C(MAX)}$	150 V / 300 mA
Logic	Type Number
General Purpose PMOS, CMOS	ULN-7001A
14-25 V PMOS	ULN-7002A
5 V TTL, CMOS	ULN-7003A
6-15 V CMOS, PMOS	ULN-7004A
High-Output TTL	ULN-7005A

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	V_{CE} = 150 V, T_A = 25°C	—	—	50	µA
			V_{CE} = 150 V, T_A = 70°C	—	—	100	µA
		ULN-7002A	V_{CE} = 150 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	µA
		ULN-7004A	V_{CE} = 150 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	I_C = 100 mA, I_B = 250 µA	—	1.2	1.3	V
			I_C = 250 mA, I_B = 350µA	—	1.4	1.6	V
Input Current	$I_{IN(ON)}$	ULN-7002A	V_{IN} = 17 V	—	0.82	1.25	mA
		ULN-7003A	V_{IN} = 3.85 V	—	0.93	1.35	mA
		ULN-7004A	V_{IN} = 5.0 V	—	0.35	0.5	mA
			V_{IN} = 12 V	—	1.0	1.45	mA
		ULN-7005A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	ULN-7002A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	13	V
		ULN-7003A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
		ULN-7004A	V_{CE} = 2.0 V, I_C = 100 mA	—	—	5.0	V
			V_{CE} = 2.0 V, I_C = 150 mA	—	—	6.0	V
			V_{CE} = 2.0 V, I_C = 200 mA	—	—	7.0	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	8.0	V
		ULN-7005A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULN-7001A	V_{CE} = 2.0 V, I_C = 250 mA	1000	—	—	—
Input Capacitance	C_{IN}	All		—	15	25	pF
Turn-On Delay	t_{PLH}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	All	V_R = 150 V, T_A = 25°C	—	—	50	µA
			V_R = 150 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 250 mA	—	1.7	2.0	V
Sustaining Voltage	$V_{CE(SUS)}$	All	L = 2 mH; R = 450 Ω	90	—	—	V

SECTION 3—HIGH-CURRENT INTERFACE DRIVERS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 3—HIGH-CURRENT INTERFACE DRIVERS (Continued)

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SELECTION GUIDE TO HIGH-CURRENT INTERFACE DRIVERS

Device Type	Absolute Maximum Ratings I_{OUT}	V_{OUT}	Outputs
UHP-400 through 433	500 mA	40 V	Sink 4
UHP-400-1 through 433-1	500 mA	70 V	Sink 4
UHP-500 through 533	500 mA	100 V	Sink 4
ULN-2001 through 2005A/L	500 mA	50 V	Sink 7
ULN-2011 through 2015A	600 mA	50 V	Sink 7
ULN-2021 through 2025A	500 mA	95 V	Sink 7
ULN-2061M	1.75 A	50 V	Source/Sink 2
ULN-2062M	1.75 A	80 V	Source/Sink 2
ULN-2064/66/68/70B	1.75 A	50 V	Sink 4
ULN-2065/67/69/71B	1.75 A	80 V	Sink 4
ULN-2074B and 2076B	1.75 A	50 V	Source/Sink 4
ULN-2075B and 2077B	1.75 A	80 V	Source/Sink 4
UDN-2541B and 2541W	1.5 A	60 V	Sink 4
UDN-2542B and 2542W	1.5 A	80 V	Sink 4
UDN-2545B	2.5 A	80 V	Sink 4
UDN-2580A	−500 mA	50 V	Source 8
UDN-2580A-1	−500 mA	80 V	Source 8
UDN-2585A	−250 mA	20 V	Source 8
UDN-2588A	−500 mA	50 V	Source 8
UDN-2588A-1	−500 mA	80 V	Source 8
UDN-2595A	200 mA	20 V	Sink 8
UDN-2596A and 2598A	500 mA	50 V	Sink 8
UDN-2597A and 2599A	1.0 A	50 V	Sink 8
ULN-2801 through 2805A	500 mA	50 V	Sink 8
ULN-2811 through 2815A	600 mA	50 V	Sink 8
ULN-2821 through 2825A	500 mA	95 V	Sink 8
UDN-2841B	1.75 A	−50 V	Sink 4
UDN-2845B	1.75 A	−50 V	Source/Sink 4
UDN-2878W	5.0 A	50 V	Sink 4
UDN-2879W	5.0 A	80 V	Sink 4
UDN-2933B and 2934B	±1.0 A	30 V	3× Half-Bridge
UDN-2935Z	±2.0 A	37 V	Half-Bridge
UDN-2936W and 2937W	±2.0 A	36 V	3× Half-Bridge
UDN-2938W and 2939B	1.0 A	24 V	Sink 3
UDN-2941B	−2.0 A	35 V	Source 4
UDN-2943Z	±1.0 A	26 V	Half-Bridge
UDN-2944W and 2948W	−4.0 A	60 V	Source 4
UDN-2949Z	±2.0 A	30 V	Half-Bridge
UDN-2950Z	±2.0 A	37 V	Half-Bridge
UDN-2952B/W	±3.5 A	40 V	Full-Bridge
UDN-2953B and 2953W	±3.5 A	50 V	Full-Bridge
UDN-2956/57A	−500 mA	−80 V	Source 5
UDN-2962W	4.0 A PWM	40 V	Source/Sink 2
UDN-2965W	5.0 A PWM	60 V	Source/Sink 2
UDN-2975W	5.0 A	50 V	Source/Sink 2
UDN-2976W	5.0 A	60 V	Source/Sink 2
UDN-2981/82A	−500 mA	50 V	Source 8
UDN-2983/84A	−500 mA	80 V	Source 8
UDN-2987/88A	−500 mA	50 V	Source 8
UDN-2993B	±600 mA	40 V	2× Full-Bridge
UDN-2998W	±2.0 A	50 V	2× Full-Bridge
UDN-3611 through 3614M	600 mA	80 V	Sink 2
UDN-5703 through 5707A	600 mA	80 V	Sink 4
UDN-5711 through 5714M	600 mA	80 V	Sink 2
UDN-5721 through 5724M	600 mA	70 V	Sink 2
UDN-5733	600 mA	80 V	Sink 4
UDN-5741 through 5744M	700 mA	70 V	Sink 2
UDN-5751 through 5754M	600 mA	70 V	Sink 2
UCN-5813B and 5814B*	1.5 A	80 V	Sink 4
UCN-5816A*	500 mA	60 V	Sink 16
UCN-5821A and 5841A*	500 mA	50 V	Sink 8
UCN-5822A and 5842A*	500 mA	80 V	Sink 8
UCN-5823A and 5843A*	500 mA	100 V	Sink 8
UCN-5825B*	2.0 A	60 V	Sink 4
UCN-5826B*	2.0 A	80 V	Sink 4

*Smart Power, see Section 4.

SERIES ULN-2000L
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

These high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

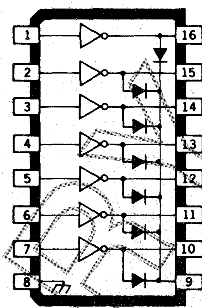
Peak inrush currents to 600 mA (Series ULN-2000L) permissible, making them ideal for driving tungsten filament lamps.

Series ULN-2001L devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.

Series ULN-2002L is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-2003L has a 2.7 kΩ series base resistor for each Darlingon pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs—particularly those beyond the capabilities of standard logic buffers.

Series ULN-2004L has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-2003L, while the required input voltage is less than that required by Series ULN-2002L.

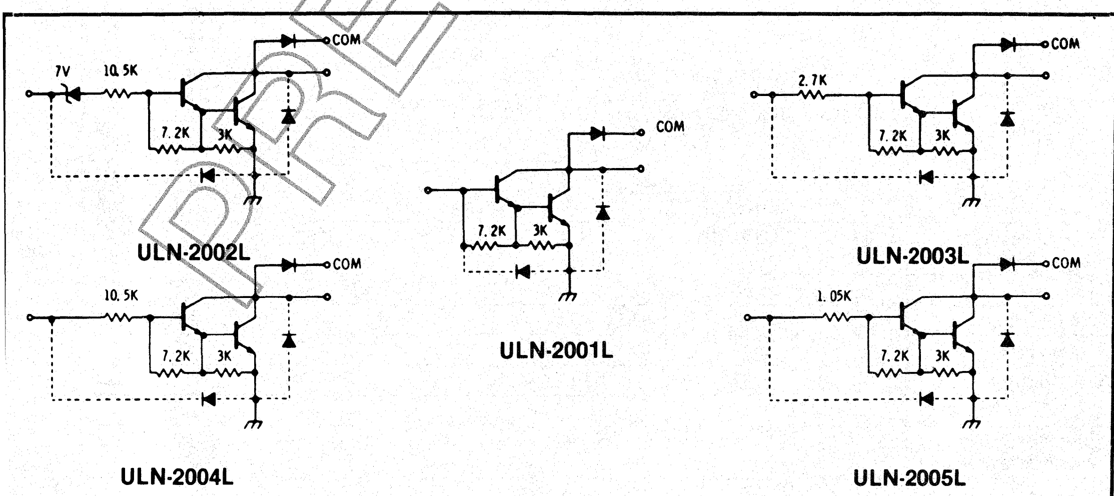


SOIC PACKAGE

Series ULN-2005L is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

Series ULN-2000L is the original high-voltage, high-current Darlington Array. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Outputs may be paralleled for higher load-current capability. All devices are packaged in the SOIC package.

PARTIAL SCHEMATICS



ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} .... 50 V
Input Voltage,
V_{IN} (ULN-2002, 2003, 2004L) .... 30 V
(ULN-2005L) .... 15 V
Continuous Collector Current, I_C .... 500 mA
Continuous Input Current, I_{IN} .... 25 mA
Power Dissipation, P_D (total package) .... 0.96 W*
Operating Ambient Temperature Range, T_A . −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

*Derate at rate of 7.7 mW/°C above = 25°C.

Device Number Designation

$V_{CE(MAX)}$ $I_{C(MAX)}$	50 V 500 mA
Logic	Type Number
General Purpose PMOS, CMOS	ULN-2001L
14-25 V PMOS	ULN-2002L
5 V TTL, CMOS	ULN-2003L
6-15 V CMOS, PMOS	ULN-2004L
High-Output TTL	ULN-2005L

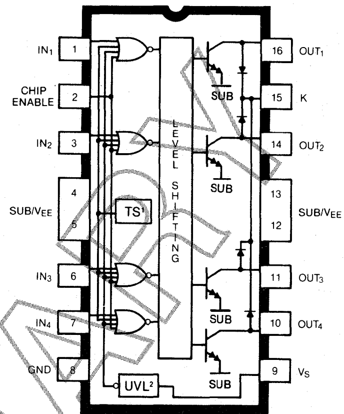
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
			V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		ULN-2002L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
		ULN-2004L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
			I_C = 200 mA, I_B = 350μA	—	1.1	1.3	V
			I_C = 350 mA, I_B = 5 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	ULN-2002L	V_{IN} = 17 V	—	0.82	1.25	mA
		ULN-2003L	V_{IN} = 3.85 V	—	0.93	1.35	mA
		ULN-2004L	V_{IN} = 5.0 V	—	0.35	0.5	mA
			V_{IN} = 12 V	—	1.0	1.45	mA
		ULN-2005L	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	ULN-2002L	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
		ULN-2003L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
			V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
		ULN-2004L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
		ULN-2004L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
			V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
			V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
		ULN-2005L	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULN-2001L	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	—
Input Capacitance	C_{IN}	All		—	15	25	pF
Turn-On Delay	t_{PLH}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
			V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	—	1.7	2.0	V

UDN-2545B
UNIVERSAL QUAD DRIVER

FEATURES

- Output Current of 2 A
- 80 V Min. Output Breakdown
- 50 V Output Sustaining Voltage
- PMOS, CMOS, TTL Compatible
- Built-in Thermal Shutdown
- Output Transient Protection
- CHIP ENABLE for Microprocessor Control
- Under-Voltage Protection



[1]TS = THERMAL SHUTDOWN
[2]UVL = UV ⊏⊐ LOCKOUT

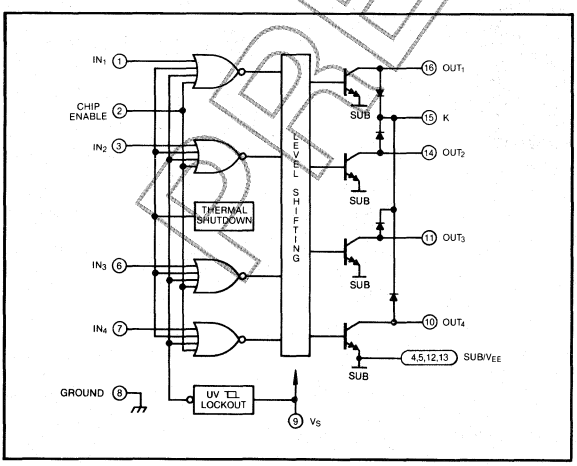
3

The UDN-2545B is a four-channel high-current, high-voltage integrated circuit designed to provide the interface between stepper motors and microprocessor or logic motor control circuitry. The UDN-2545B will accept most standard logic signal inputs and provide motor drive current to both positive and negative supply rails.

The UDN-2545B is capable of sinking up to 2.5 A and maintaining an output OFF voltage of 80 volts. This device incorporates some unique features such as under-voltage protection, thermal shutdown, and CHIP ENABLE control. The under-voltage protection guards against supply line transients and has built-in hystersis. The thermal shutdown with hystersis is to guard against damage to the device. CHIP ENABLE is especially good for use in microprocessor control. All outputs have clamp diodes for suppression of inductive loads.

The UDN-2545B is supplied in a 16 pin plastic dual in-line package with heat-sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat sinks for increased power dissipation with standard IC sockets and printed wiring boards.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Logic Supply Voltage, V_S	20 V
Emitter Supply Voltage, V_{EE}	−25 V
Output Current, I_{OUT}	2.5 A
Output Voltage, V_{CE}	80 V
Input Voltage, V_{IN}	25 V
Package Power Dissipation, P_D	2.77 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

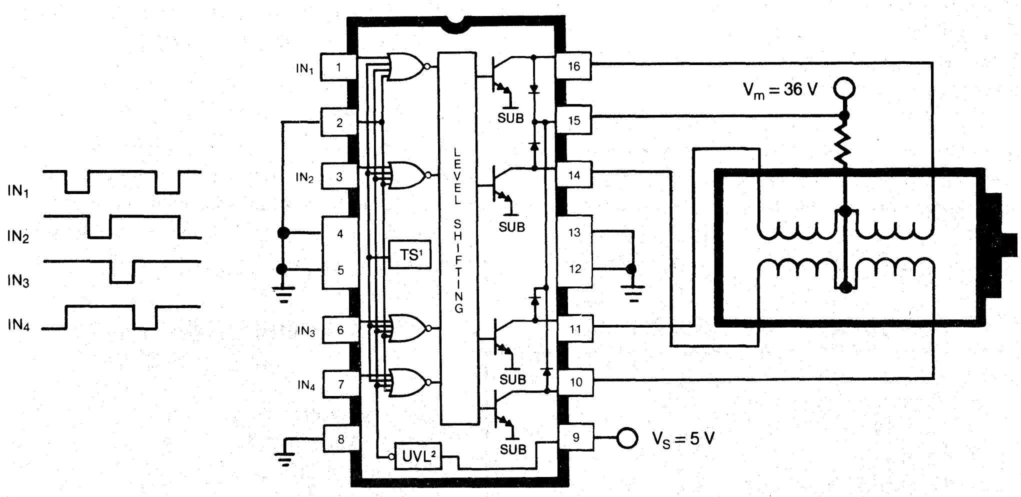
*Derate at the Rate of 22.2 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C, V_S = 15\ V, V_{EE} = 0\ V$

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 80$ V, $V_{IN} = 2.0$ V, Other Inputs = 0 V	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 100$ mA, Inputs = 5.0 V	50	—	V
Output Saturation Voltage*	$V_{CE(SAT)}$	$I_{OUT} = 2$ A, Inputs = 0 V	—	2.2	V
Clamp Diode Leakage Current	I_R	$V_R = 80$ V	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 2$ A	—	2.5	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 0.8$ V, CHIP ENABLE = 5.0 V	—	−200	μA
		CHIP ENABLE = 0 V	—	−400	μA
	$I_{IN(OFF)}$	Input = 15.0 V	—	50	μA
Supply Current	$I_{S(ON)}$	All Inputs = 0.8 V	—	65	mA
	$I_{S(OFF)}$	All Inputs = 5.0 V	—	20	mA

*Pulse Test

STEPPER MOTOR APPLICATION

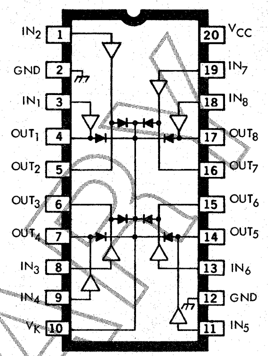


[1]TS = THERMAL SHUTDOWN
[2]UVL = UV LOCKOUT

UDN-2596A THROUGH UDN-2599A 8-CHANNEL SATURATED SINK DRIVERS

FEATURES

- Low Output "ON" Voltage (non-Darlington)
- Up to 1.0 A Sink Capability
- 50 V Output Breakdown
- CMOS, DTL, Compatible Inputs
- Output Pull-Down for Fast "OFF" time



Dwg. No. A-12,670

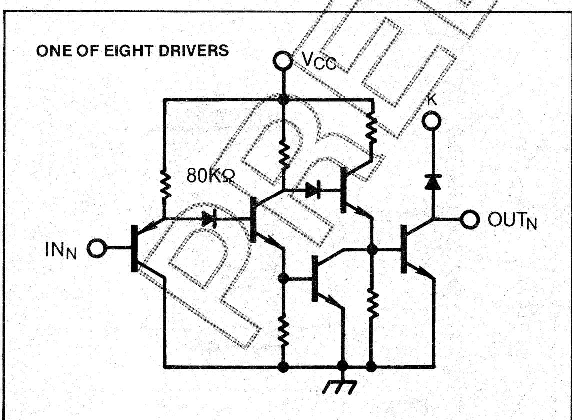
These eight-channel active-low saturated sink drivers feature high-voltage, high-current open collector outputs with transient suppression clamp diodes and inputs which directly interface to NMOS, CMOS, and TTL logic families. All devices in this series can be used as interface drivers between standard low-power digital logic and high-power loads such as relays, solenoids, stepping motors and LED or incandescent displays.

The saturated, non-Darlington outputs feature low collector-emitter voltage drops as well as fast turn-off times due to an active pull-down function within the output predrive section. Inputs require virtually no logic current sourcing capability and are activated by a low logic level consistent with the relatively high-current sinking capability associated with NMOS, CMOS, and TTL logic types.

The type UDN-2596A features 500 mA output sink capability, and is intended for use with 5 V logic systems. The UDN-2598 A also features 500 mA output sink capability but is intended for use with 12 V logic systems. UDN-2597A (5 V Logic Systems) and UDN-2599A (12 V Logic Systems) are the higher current versions capable of handling 1 A.

All devices feature 50 V output breakdown capability and 35 V output sustaining voltage. All devices are furnished in a 20-pin DIP package with copper lead frames for improved thermal characteristics.

PARTIAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

Output Voltage, V_{CE}		50 V
Output Current, I_{OUT}	(UDN-2596A/2598A)	500 mA
	(UDN-2597A/2599A)	1.0 A
Supply Voltage, V_{CC}	(UDN-2596A/2597A)	7.0 V
	(UDN-2598A/2599A)	15 V
Input Voltage, V_{IN}	(UDN-2596/97A)	7.0 V
	(UDN-2598/99A)	15 V
Package Power Dissipation, P_D		2.27W*
Operating Free Air Temperature Range, T_A		−20°C to +85°C
Storage Temperature Range, T_S		−65°C to +150°C

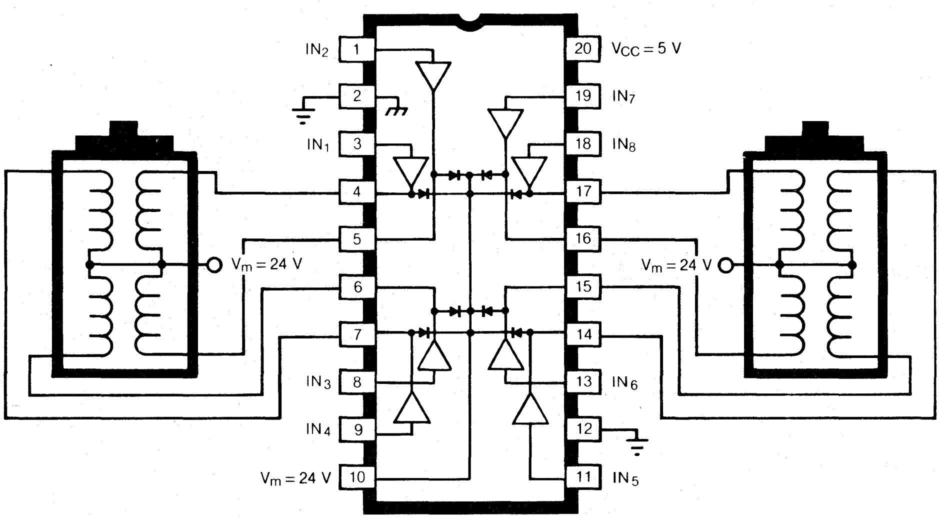
*Derate at rate of 18.18 mW/°C above $T_A = 25°C$

ELECTRICAL CHARACTERISTICS at T_A = 25°C
V_{CC} = 5.0 V (UDN-2596A/2597A) & V_{CC} = 12.0 V (UDN-2598A/2599A)

Characteristics	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	All	V_{OUT} = 50 V, V_{IN} = 2.4 V	—	10	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2596/98	I_{OUT} = 300 mA	35	—	V
		2597/99	I_{OUT} = 750 mA	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	2596/98	I_{OUT} = 300 mA	—	0.5	V
		2597/99	I_{OUT} = 750 mA	—	1.0	V
Clamp Diode Leakage Current	I_R	All	V_R = 50 V	—	10	μA
Clamp Diode Forward Voltage	V_F	2596/98	I_F = 300 mA	—	1.8	V
		2597/99	I_F = 750 mA	—	1.8	V
Input Current	$I_{IN(0)}$	2596/97	V_{IN} = 0.8 V	—	−15	μA
		2598/99	V_{IN} = 0.8 V	—	−50	μA
	$I_{IN(1)}$	2596/97	V_{IN} = 2.4 V	—	10	μA
		2598/99	V_{IN} = 12 V	—	10	μA
Supply Current (per driver)	$I_{CC(ON)}$	2596/97	V_{IN} = 0.8 V	—	5.0	mA
		2598/99	V_{IN} = 0.8 V	—	15	mA
	$I_{CC(OFF)}$	2596/97	V_{IN} = 2.4 V	—	1.3	mA
		2598/99	V_{IN} = 12 V	—	1.3	mA
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	1.0	μs
Turn-Off Delay	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	2.0	μs

*Complete part number includes prefix UDN- and suffix A, e.g. UDN-2596A.

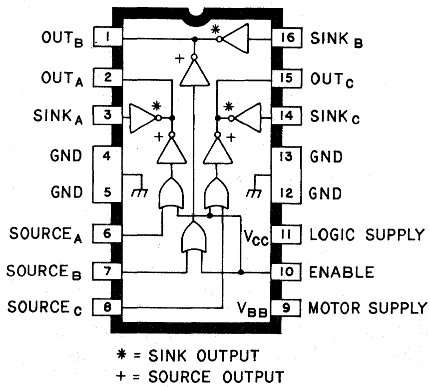
DUAL STEPPER MOTOR DRIVE SCHEME



UDN-2933B AND UDN-2934B 3-CHANNEL HALF-BRIDGE MOTOR DRIVERS

FEATURES

- Output Currents to 1 A
- Output Voltages to 30 V
- Low Output-Saturation Voltage
- Transient-Protected Outputs
- Tri-State Outputs
- TTL or CMOS Compatible Inputs
- Reliable Monolithic Construction



Dwg.No. A-12,356

DEVELOPED for use in 3-phase brushless d-c motor applications, Types UDN-2933B and UDN-2934B provide drive capabilities to 1 A and 30 V. Saturated drivers provide for low output voltage drops at maximum rated current.

The 1 A half-bridge drivers differ only in input circuitry: Type UDN-2933B is compatible with TTL and 5 V CMOS; Type UDN-2934B is used with 12 V CMOS. Economical versions of the drivers (Types UDN-2933B-2 and UDN-2934B-2), with 600 mA maximum output-current ratings, are recommended for applications with reduced load current requirements. The "-2" parts are identical to the basic devices except for the maximum allowable load-current rating.

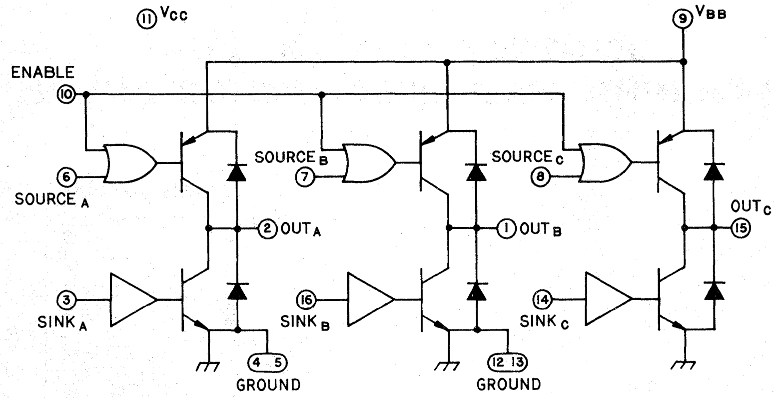
Monolithic construction and a 16-pin dual in-line package with centered heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent power dissipation ratings, minimum size, and ease of installation. The package configuration allows easy attachment of an inexpensive heat sink. It fits a standard IC socket or printed wiring board layout.

Half-bridge drivers with Darlington outputs (Type UDN-2935Z and UDN-2950Z) are supplied in TO-220 power-tab packages for operation with load currents of up to 3.5 A. They are described in the most recent issue of Sprague Engineering Bulletin 29318.3.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

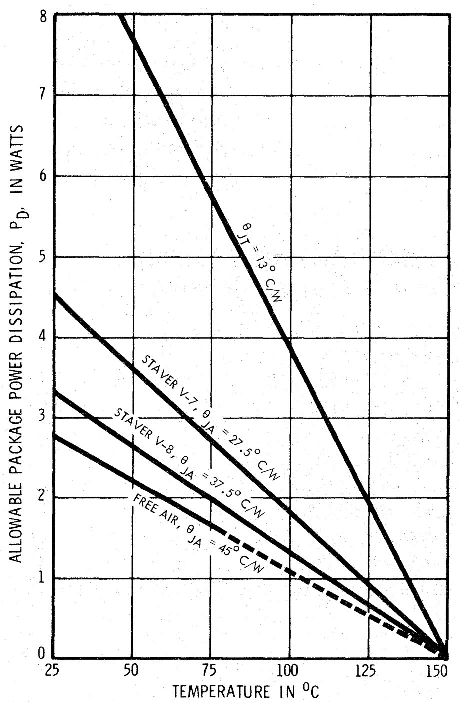
Motor Supply Voltage, V_{BB}	30 V
Logic Supply Voltage Range, V_{CC}	
(UDN-2933B and UDN-2933B-2)	4.5 V to 7.0 V
(UDN-2934B and UDN-2934B-2)	10 V to 15 V
Logic Input Voltage, V_{IN}	V_{CC}
Output Current, I_{OUT}	
(UDN-2933B and UDN-2934B)	±1.0 A
(UDN-2933B-2 and UDN-2934B-2)	±0.6 A
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



Dwg.No. A-12,357

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,793A

TRUTH TABLE

Sink Driver Input	Source Driver Input	Enable Input	Output
Low	Low	Low	High
Low	High	Low	Open
High	Low	Low	Disallowed
High	High	Low	Low
High	Any	High	Low
Low	Any	High	Open

3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 5 V (UDN-2933B/B-2) or V_{CC} = 12 V (UDN-2934B/B-2), $T_{TAB} \leq$ +70°C

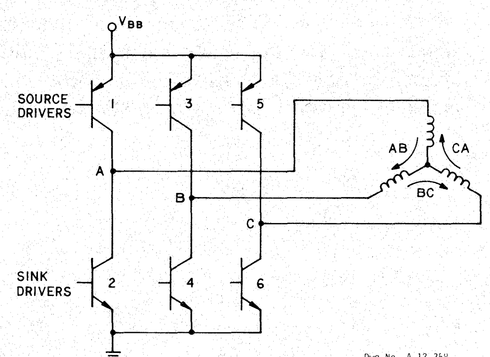
Characteristic	Symbol	Applicable Devices	Test Condtions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	All	All Drivers OFF, V_{OUT} = 0 V	—	−5.0	−100	μA
			All Drivers OFF, V_{OUT} = 30 V	—	5.0	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	All	I_{OUT} = −100 mA	—	—	1.1	V
			I_{OUT} = 100 mA	—	—	0.2	V
			I_{OUT} = −250 mA	—	—	1.2	V
			I_{OUT} = 250 mA	—	—	0.3	V
			I_{OUT} = −500 mA	—	—	1.5	V
			I_{OUT} = 500 mA	—	—	0.6	V
		2933B/34B	I_{OUT} = −800 mA	—	—	1.8	V
			I_{OUT} = 800 mA	—	—	0.8	V
Motor Supply Current	I_{BB}	All	All Drivers OFF	—	50	200	μA
			1 Source + 1 Sink ON, No Loads	—	1.0	1.3	mA
Clamp Diode Forward Voltage	V_F	All	I_F = 500 mA	—	1.3	2.0	V
		UDN-2933/34B	I_F = 800 mA	—	1.3	2.0	V
Logic Input Voltage	$V_{IN(1)}$	2933B/B-2		2.4	—	—	V
		2934B/B-2		8.0	—	—	V
	$V_{IN(0)}$	2933B/B-2		—	—	0.8	V
		2934B/B-2		—	—	4.0	V
Logic Input Current	$I_{IN(1)}$	2933B/B-2	V_{IN} = 2.4 V	—	<1.0	10	μA
		2934B/B-2	V_{IN} = 8.0 V	—	<1.0	10	μA
	$I_{IN(0)}$	All	V_{IN} = 0.8 V	—	−50	−300	μA
Logic Supply Current	I_{CC}	All	All Drivers OFF	—	1.7	3.0	mA
			1 Source + 1 Sink ON	—	30	40	mA
Output Rise Time	t_r	All	I_{OUT} = −500 mA, V_{BB} = 20 V	—	250	—	ns
			I_{OUT} = 500 mA, V_{BB} = 20 V	—	150	—	ns
Output Fall Time	t_f	All	I_{OUT} = −500 mA, V_{BB} = 20 V	—	500	—	ns
			I_{OUT} = 500 mA, V_{BB} = 20 V	—	30	—	ns

NOTES: 1. Each driver is tested separately.
2. Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL COMMUTATION SEQUENCE

Drivers ON*	Motor Current	Elec. Degrees
1+4	AB	0
1+6	−CA	60
3+6	BC	120
3+2	−AB	180
5+2	CA	240
5+4	−BC	300

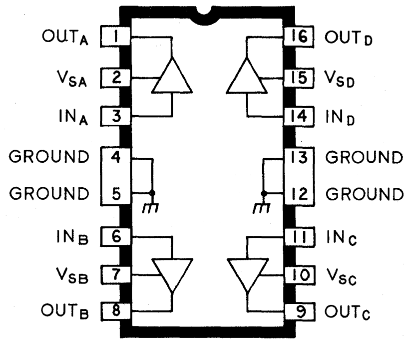
*Enable input must be low; Source drivers are turned ON with a logic low, sink drivers are turned ON with a logic high.



UDN-2941B
QUAD HIGH-CURRENT SOURCE DRIVER

FEATURES

- 1.5 A Output Source Current
- Minimized Saturation Voltage
- 30 V Output Sustaining Voltage
- Transient-Protected Outputs
- TTL or CMOS Compatible Inputs
- Plastic Dual In-Line Package With Heat-Sink Contact Tabs



Dwg. No. A-12,514

HIGH-CURRENT SOURCE DRIVERS are designed to serve as interface between low-level logic and a variety of peripheral power loads, including solenoids, d-c or stepper motors using pulse-width modulation, and multiplexed LED or incandescent displays.

The UDN-2941B high-current source driver has four independent emitter-follower drivers. Special circuit design techniques, resulting in reduced output-saturation voltages, allow any one driver to source up to −1.5 A continuously with minimal voltage drops and package power dissipation.

The device's high switching speed prevents "ghosting" effects when it is used to drive multiplexed displays. All outputs are rated for operation to 35 V (30 V sustaining). The low-level inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The UDN-2941B integrated circuit is supplied in a 16-pin plastic dual in-line package with copper heat-sink contact tabs. The lead configuration facilitates attachment of an inexpensive external heat sink for maximum power dissipation with standard cooling methods. It fits a standard IC socket or printed wiring board layout. The heat sink is at ground potential and needs no insulation.

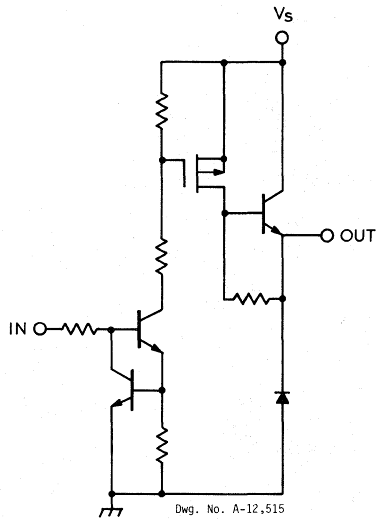
Similar devices, for operation with load currents of up to −500 mA, are the 8-channel source drivers of Series UDN-2980A. They are described in Sprague Engineering Bulletin 29310.

ABSOLUTE MAXIMUM RATINGS

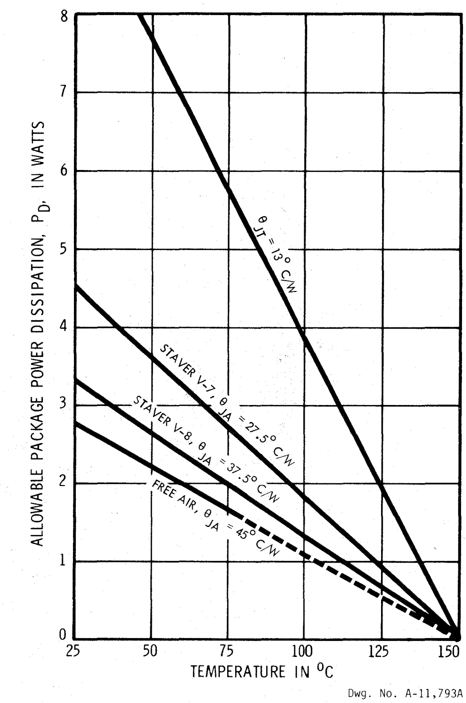
Supply Voltage Range, V_S	12 V to 35 V
Peak Output Current, I_{OUT}	−2.0 A
Input Voltage, V_{IN}	15 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature, T_S	−55°C to +150°C

Output current rating will be limited by ambient temperature, duty cycle, heat sinking, air flow, and number of outputs conducting. Under any set of conditions, do not exceed the −2.0 A peak current and a junction temperature of +150°C.

PARTIAL SCHEMATIC
One of 4 Drivers



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



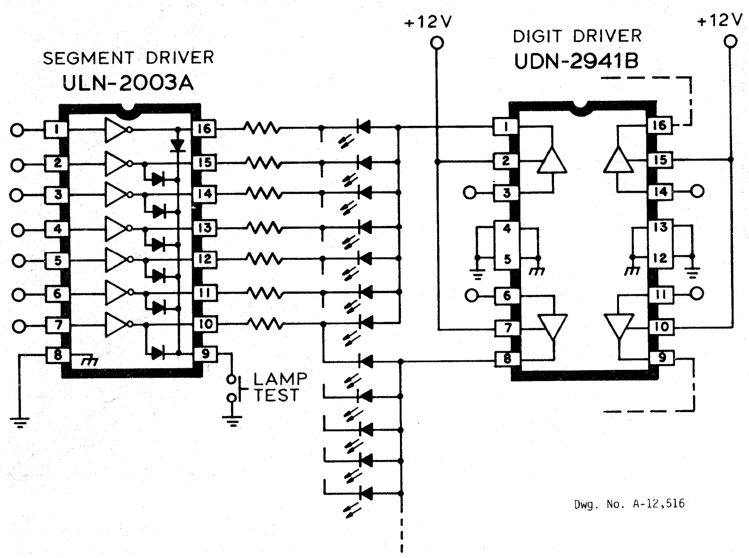
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 35$ V, $T_{TAB} \le +70°C$

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} = 0.4$ V, $V_{OUT} = 0$ V, $T_A = +25°C$	—	< -10	-100	μA
		$V_{IN} = 0.4$ V, $V_{OUT} = 0$ V, $T_A = +70°C$	—	< -10	-500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	30	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 2.4$ V, $I_{OUT} = -1.0$ A	—	1.3	1.5	V
		$V_{IN} = 2.4$ V, $I_{OUT} = -1.5$ A	—	1.6	1.8	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 2.4$ V	—	175	500	μA
	$I_{IN(OFF)}$	$V_{IN} = 0.4$ V	—	—	-10	μA
Output Source Current	I_{OUT}	$V_{IN} = 2.4$ V	-1.5	—	—	A
Total Supply Current	I_S	$V_{IN} = 2.4$ V (Note 3), Outputs Open	—	11	15	mA
Clamp Diode Leakage Current	I_R	$V_R = 35$ V	—	<10	100	μA
Clamp Diode Forward Current	V_F	$I_F = 1.5$ A	—	1.4	2.0	V
Turn-On Delay	t_{PLH}	0.5 V_{in} to 0.5 V_{out}, Resistive Load	—	0.25	2.5	μs
Turn-Off Delay	t_{PHL}	0.5 V_{in} to 0.5 V_{out}, Resistive Load	—	0.5	5.0	μs

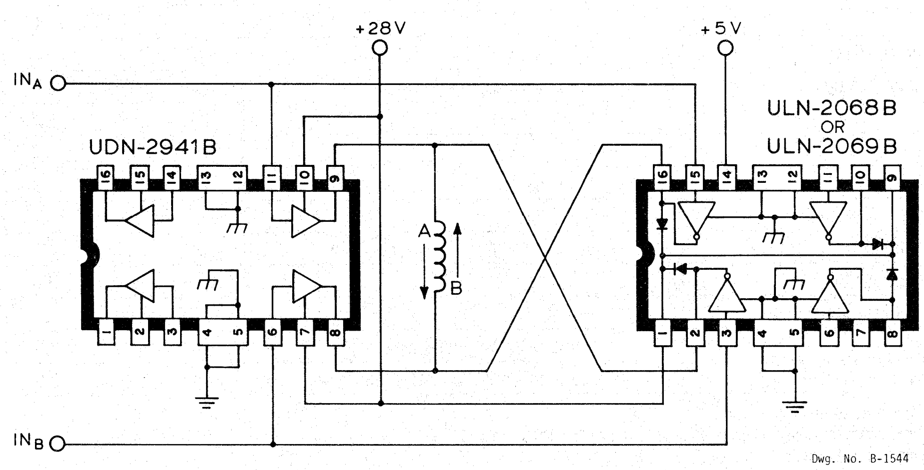
NOTES: 1. Each driver tested separately.
2. Negative current is defined as coming out of (sourcing) the specified device pin.
3. All inputs simultaneously.

TYPICAL APPLICATIONS

MULTIPLEXED COMMON-ANODE LED DISPLAY DRIVER



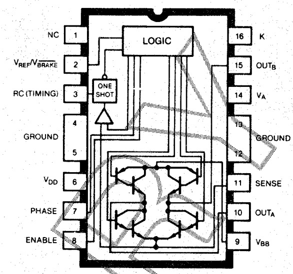
FULL-BRIDGE MOTOR DRIVER
(One of 2 Windings)



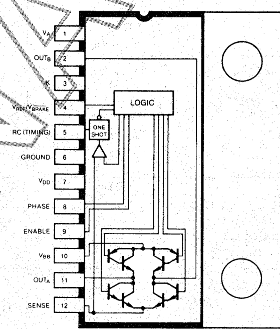
UDN-2953B AND UDN-2953W FULL-BRIDGE MOTOR DRIVER

FEATURES

- Output Voltage 50 V
- Output Current of 2 A
- 50 Thermal Shutdown
- Anti-Crossover Protection
- BRAKING, ENABLE, and Current Limit Functions



UDN-2953B



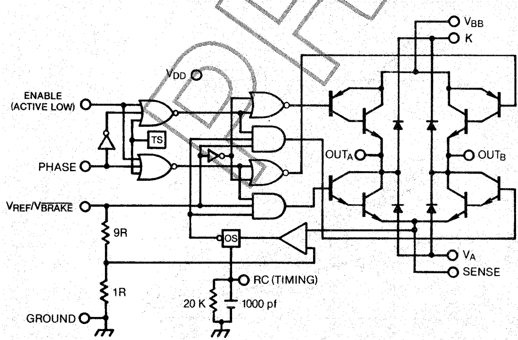
UDN-2953W

Full-Bridge Motor-Driver integrated circuits, Types UDN-2953B and UDN-2953W combine low-level logic circuitry and Darlington output power drivers for bidirectional control of d-c or 2-phase bipolar motors operating with continuous load currents of up to 2 A and peak start-up currents as high as 3.5 A.

These monolithic integrated circuits have extensive circuit protection. Both drivers have thermal shutdown networks that disable motor drive if the package power dissipation ratings are exceeded. Internal diode transient protection is provided on chip. Output-current limiting is determined by the user's selection of a sensing resistor. When $V_{REF}/\overline{V_{BRAKE}}$ pin is low the BRAKING function is enabled. The BRAKING function turns OFF both sink drivers and turns ON both source drivers. When $V_{REF}/\overline{V_{BRAKE}}$ is set above 2.4 V, then the REFERENCE function is enabled and the reference level is set. An RC TIMING pin is present to use for an integral One Shot to control pulse duration for sense-line inputs.

The Type UDN-2953B FULL-BRIDGE DRIVER is supplied in a 16-pin dual in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. Type UDN-2953W, for higher power requirements, is supplied in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation.

FUNCTIONAL BLOCK DIAGRAM



OS = One Shot
TS = Thermal Shutdown

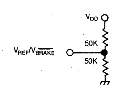
ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

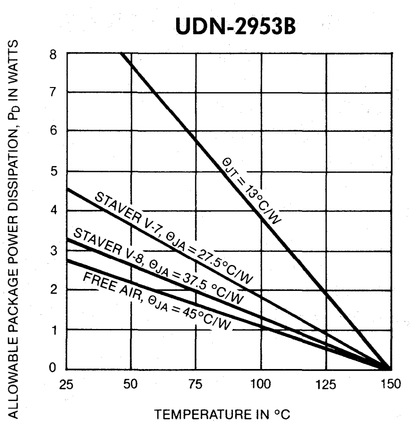
Motor Supply Voltage Range, V_{BB}	7.5 V to 50 V
Logic Supply Voltage Range, V_{DD}	4.5 V to 15 V
Logic Input Voltage, V_{PHASE}, V_{ENABLE}	30 V
Reference Voltage, $V_{REF/BRAKING}$	15 V
Output Current, I_{OUT} (Peak)	±3.5 A
(Continuous)	±2.0 A
Package Power Dissipation, P_D	See Graphs
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

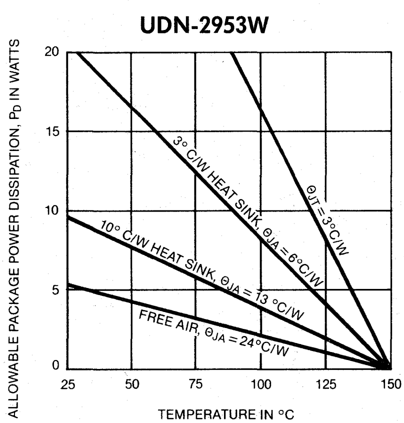
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 50 V, V_{DD} = 5 V

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{ENABLE} = 5 V, V_{OUT} = V_{BB}, (note 1)	—	—	50	μA
		V_{ENABLE} = 5 V, V_{OUT} = 0 V, (note 2)	—	—	50	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 2 A, Sink Driver	50	—	—	V
		I_{OUT} = −2 A, Source Driver	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 0 V, I_{OUT} = 2 A, Sink Driver	—	1.5	1.8	V
		V_{ENABLE} = 0 V, I_{OUT} = 2 A, Source Driver	—	1.5	1.8	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	μA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.8	2.2	V
Logic Input Current	$I_{IN(1)}$	All Inputs = 2.4 V	—	<1.0	10	μA
	$I_{IN(0)}$	All Inputs = 0.8 V	—	50	200	μA
Logic Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
Reference Voltage Range	V_{REF}		2.4	—	15	V
V_{REF} Open Circuit Voltage	$V_{REF\ (OPEN)}$	I_{REF} = 0 V	—	$V_{DD}/2$	—	V
V_{REF} to V_{SENSE}	V_{REF}/V_{SENSE}		9.5	—	10.5	V
Sense Voltage	V_{SENSE}		—	—	1.5	V
Turn-On Delay	t_{ON}	All Drivers	—	1.0	—	μs
Turn-Off Delay	t_{OFF}	All Drivers	—	1.0	—	μs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V, V_{BRAKE} = 2.4 V, No Load	—	20	30	mA
	$I_{BB(OFF)}$	V_{ENABLE} = V_{BRAKE} = 2.4 V, No Load	—	1.7	2.5	mA
		V_{ENABLE} = 5 V_{BRAKE} = 0.8 V, No Load	—	40	60	mA
One Shot R_{EXT} Range			—	50	—	kΩ
One Shot C_{EXT} Range			—	390	—	pf
Logic Supply Current	I_{DD}	V_{ENABLE} = V_{BRAKE} = 2.4 V	—	15	20	mA
		V_{ENABLE} = V_{BRAKE} = 0.8 V	—	22	30	mA

Note 1: Tests performed at OUT_B with V_{PHASE} = 2.4 V and at OUT_A with V_{PHASE} = 0.8 V.
Note 2: Test performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
Note 3: For voltage higher than 2.4 V (min. V_{REF}) the $V_{REF}/\overline{V_{BRAKE}}$ input resistance is as shown in figure.



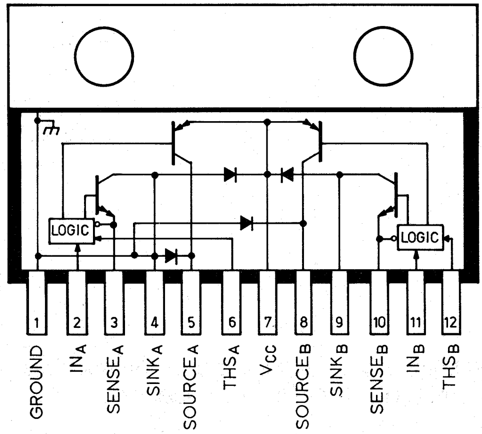




UDN-2965W DUAL SOLENOID/MOTOR DRIVER —Pulse-Width Modulated Current Control

FEATURES

- 5 A Peak Output
- 60 V Min. Ouput Breakdown
- TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- Internal Thermal Shutdown
- High-Speed Chopper
- Plastic SIP With Heat-Sink Tab



Dwg.No. A-12,413

DESIGNED TO DRIVE impact printer solenoids and stepper motors, the UDN-2965W includes two independent driver pairs rated for continuous operation to ±4 A. Each half-bridge driver includes diode transient protection, input gain and level shifting, a voltage regulator for single-supply operation, thermal protection, and pulse-width modulated (PWM) output-current control. Inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The PWM mode helps minimize power dissipation and maximize load efficiency. The peak output current and hysteresis for each half-bridge is set independently. Output current, threshold voltage, and hysteresis are set by the user's selection of external resistors. If desired, internal threshold and hysteresis defaults (400 mV and ≤10%) can be used. At the specified output-current trip level, the source driver turns OFF. The internal flyback diode then allows current to flow without additional input from the power supply. When the lower current trip point is reached, the source driver turns back ON.

For maximum power-handling capability, the driver is supplied in 12-pin single in-line power tab package. An external heat sink is required for proper operation. The tab is at ground potential and needs no insulation.

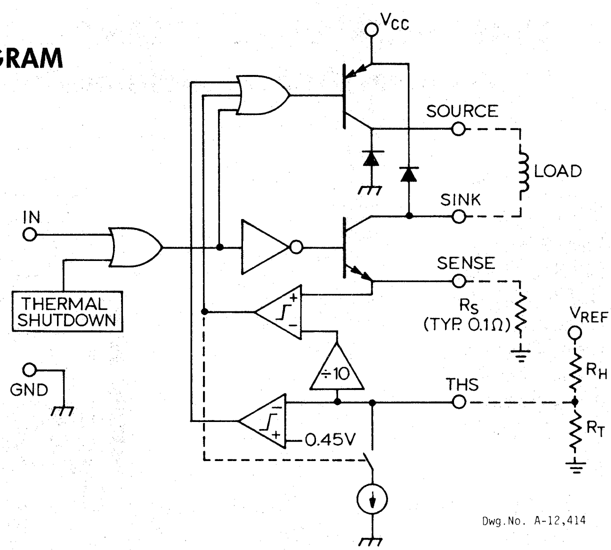
Similar dual 4 A solenoid drivers, for non-PWM applications, are available as Sprague Types UDN-2975W and UDN-2976W.

ABSOLUTE MAXIMUM RATINGS at $T_{TAB} \leq +70°C$

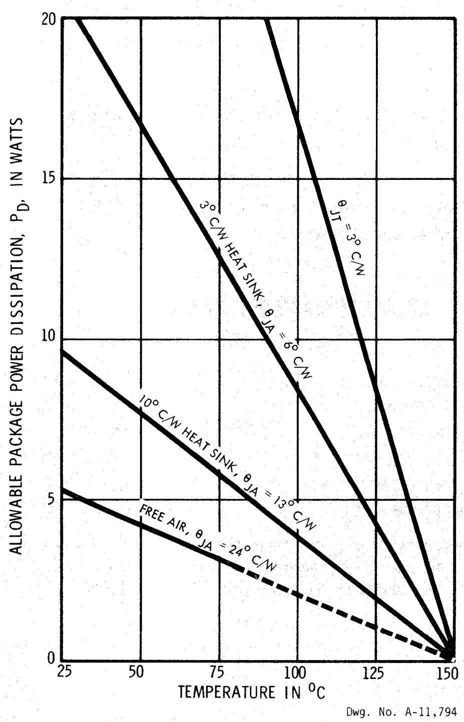
Supply Voltage, V_{CC}	60 V
Peak Output Current, I_{OUT}	±5 A
Input Voltage Range, V_{IN}	−0.3 V to +7.0 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

NOTE: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



TRUTH TABLE

V_{IN}	V_{THS}	V_{SENSE}	Source Driver	Sink Driver	Hysteresis
High	NA	NA	Off	Off	NA
Low	<0.4 V	NA	Off	On	NA
Low	0.6 V to 4.0 V	$<V_{THS}/10$	On	On	Set by R_{TH}
Low	0.6 V to 4.0 V	$>V_{THS}/10$	Off	On	—
Low	>4.5 V	<0.4 V	On	On	5% to 10%
Low	>4.5 V	>0.4 V	Off	On	—

3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_{TAB} ≤ +70°C, V_{CC} = 60 V, V_{SENSE} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	V_{CC}	Operating	20	—	60	V
Output Drivers						
Output Leakage Current	I_{CEX}	V_{IN} = 2.4 V, V_{SOURCE} = 0 V	—	−10	−100	μA
		V_{IN} = 2.4 V, V_{SINK} = 60 V	—	10	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Drivers, I_{LOAD} = 4.0 A	—	1.6	2.2	V
		Source Drivers, I_{LOAD} = 1.0 A	—	1.3	1.6	V
		Sink Drivers, I_{LOAD} = 4.0 A	—	1.5	2.0	V
		Sink Drivers, I_{LOAD} = 1.0 A	—	1.0	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±4.0 A, L = 3.5 mH	60	—	—	V
Output Current Regulation	ΔI_{OUT}	V_{THS} = 0.6 V to 1.0 V, L = 3.5 mH	—	—	±25	%
		V_{THS} = 1.0 V to 2.0 V, L = 3.5 mH	—	—	±10	%
		V_{THS} = 2.0 V to 4.0 V, L = 3.5 mH	—	—	±5.0	%
Clamp Diode Forward Voltage	V_F	I_F = 4.0 A	—	1.3	1.8	V
Output Rise Time	t_r	I_{LOAD} = 4.0 A, 10% to 90%, Resistive Load	—	0.5	1.0	μs
Output Fall Time	t_f	I_{LOAD} = 4.0 A, 90% to 10%, Resistive Load	—	0.5	1.0	μs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	1.0	10	μA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−20	−100	μA
	$I_{THS(OFF)}$	V_{THS} ≤ 400 mV	—	−60	—	μA
	$I_{THS(ON)}$	V_{THS} ≥ 500 mV, V_{SENSE} ≤ V_{THS}/10.5	—	−2.0	—	μA
	$I_{THS(HYS)}$	V_{SENSE} ≥ V_{THS}/9.5, V_{THS} = 0.6 V to 4.5 V	140	200	260	μA
Output Disable Voltage	$V_{THS(OFF)}$		—	—	400	mV
V_{THS}/V_{SENSE} Ratio	—	V_{THS} = 2.0 V to 4.0 V	9.5	10	10.5	—
Default Sense Trip Voltage	V_{SENSE}	V_{THS} = 4.5 V	380	400	420	mV
Default Hysteresis	H	V_{THS} = 4.5 V	5.0	—	10	%
Supply Current (Total Device)	I_{CC}	V_{IN} = 2.4 V, Outputs OFF	—	15	25	mA
		V_{IN} = 0.8 V, Outputs Open	—	30	40	mA
Propagation Delay Time (Resistive Load)	t_{pd}	50% V_{IN} to 50% V_{OUT}, Turn OFF	—	—	2.5	μs
		50% V_{IN} to 50% V_{OUT}, Turn ON	—	—	3.0	μs
		100% V_{SENSE} to 50% V_{OUT}*	—	—	2.0	μs
Thermal Shutdown	T_J		—	175	—	°C

*Where V_{SENSE} ≥ V_{THS}/9.5
NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

APPLICATIONS

The UDN-2965W driver is intended for use as a free-running, pulse-width modulated, motor or solenoid driver.

The source and sink drivers are both turned ON by a low level at the input. When the load current reaches the trip point (set by external resistors or internal default), the comparator output goes high and the source driver is turned OFF. The internal flyback diode then allows current to flow without further input from the power supply. An internal constant current sink reduces the trip point (hysteresis) until the decaying current reaches the lower threshold, when the comparator output goes low and the source driver is again turned ON. Hysteresis percentage is a function of the external resistance R_H and is independent of the peak output load current set by R_T. The chopping frequency is asynchronous and a function of the system and circuit parameters, including load inductance, supply voltage, hysteresis setting, and switching speed of the driver.

Maximum load current and hysteresis percentage are determined by the user:

$$R_H = 50\,V_{REF}\,H$$

$$R_T = \frac{R_H(10\,I_{MAX}\,R_S)}{V_{REF} - (10\,I_{MAX}\,R_S)}$$

where $10\,I_{MAX}\,R_S = V_{THS} = 0.6$ to 4.0 V

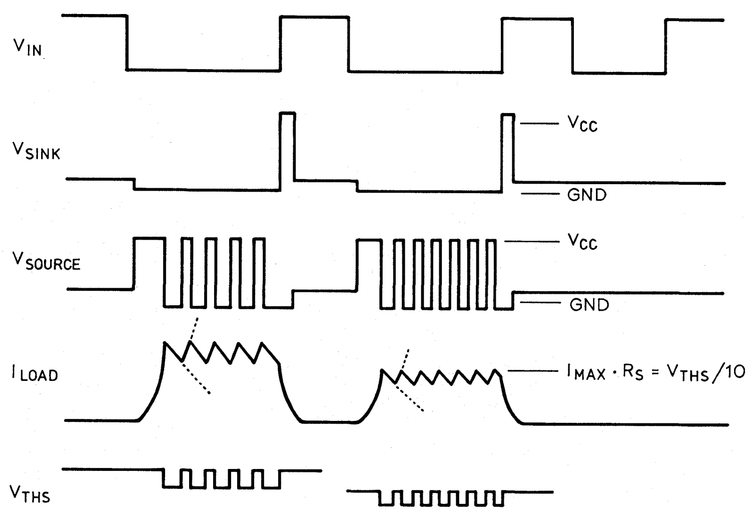
and H = desired hysteresis in percent.

Graphical solutions for R_H and R_T, with V_{REF} = 5 V and $R_S = 0.1\,\Omega$, follow.

Pulling V_{THS} down to less than 0.4 V disables the source driver, turning the load OFF. With V_{THS} greater than 4.5 V, the hysteresis is fixed at (defaults to) between 5% and 10% and the peak load current is fixed at:

$$I_{MAX} = 0.4/R_S$$

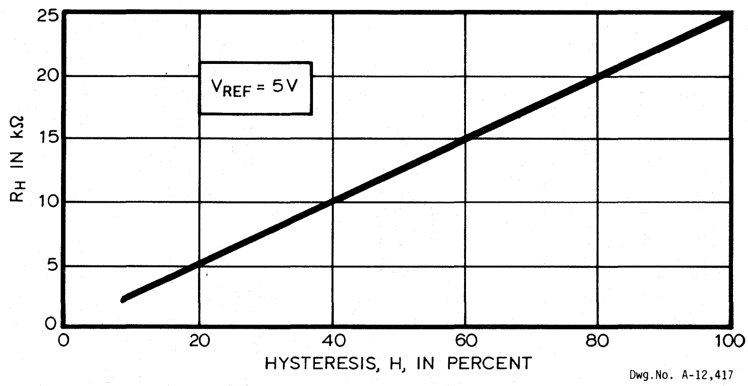
TYPICAL WAVESHAPES



Dwg.No. A-12,415

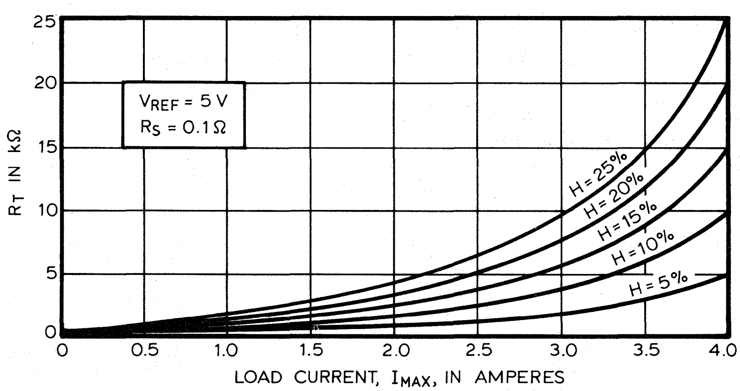
APPLICATIONS (Continued)

RESISTOR R_H VALUE
AS A FUNCTION OF HYSTERESIS



Dwg.No. A-12,417

RESISTOR R_T VALUE
AS A FUNCTION OF PEAK LOAD CURRENT



Dwg.No. A-12,416

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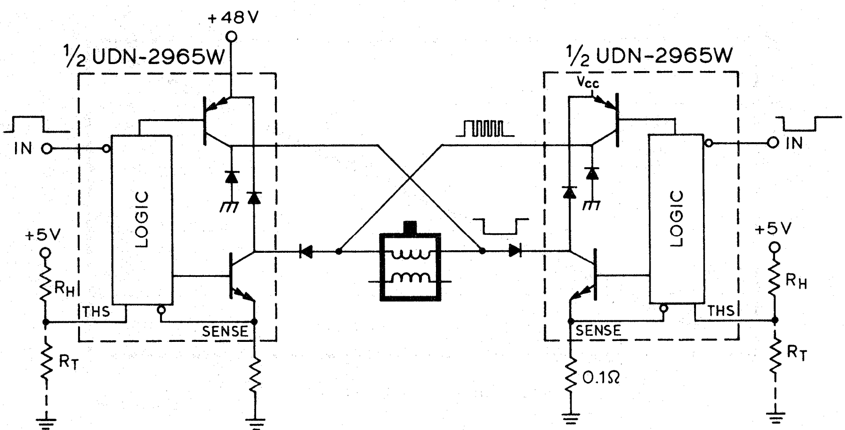
TYPICAL APPLICATION

BIPOLAR, PULSE-WIDTH MODULATED, STEPPER-MOTOR DRIVE



R_H AND R_T DETERMINE HYSTERESIS AND PEAK CURRENT

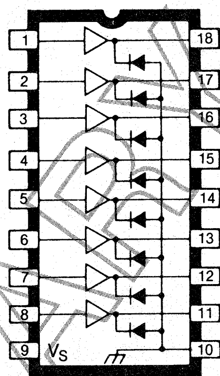
Dwg. No. B-1538

NOTE: Each of the drivers within the UDN-2965W includes an internal logic delay to prevent potentially destructive crossover currents within the driver during phase changes. However, never simultaneously enable both inputs in the full-bridge configuration: A destructive short-circuit to ground will result.

UDN-2985A AND UDN-2986A 8-CHANNEL SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 300 mA Output Source Current Capability
- Transient-Protected Outputs
- 30 V Min. Output Breakdown Voltage
- Low ON Voltage Non-Darlington Drivers



Recommended for applications requiring separate logic and load grounds, load supply voltage to +30 V, and load currents to 300 mA, UDN-2985A and UDN-2986A source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, and LEDs.

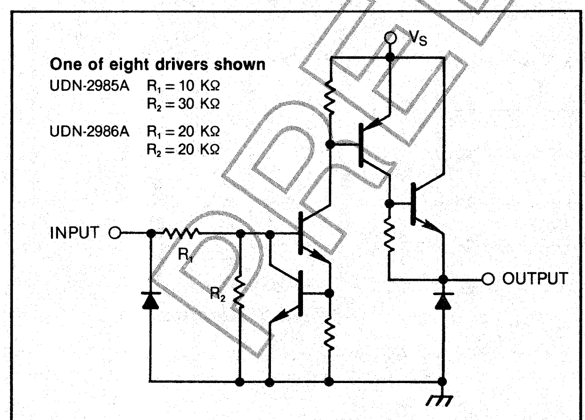
Under normal operating conditions these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

The UDN-2985A driver is for use with +5 V logic systems—TTL, Schottky, TTL, DTL, and CMOS. The UDN-2986A is intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. Both devices will maintain a maximum output OFF voltage of +30 V.

In all cases, the output is switched ON by an active high input level.

The UDN-2985A and UDN-2986A source drivers are supplied in 18-lead dual in-line packages. On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.

PARTIAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

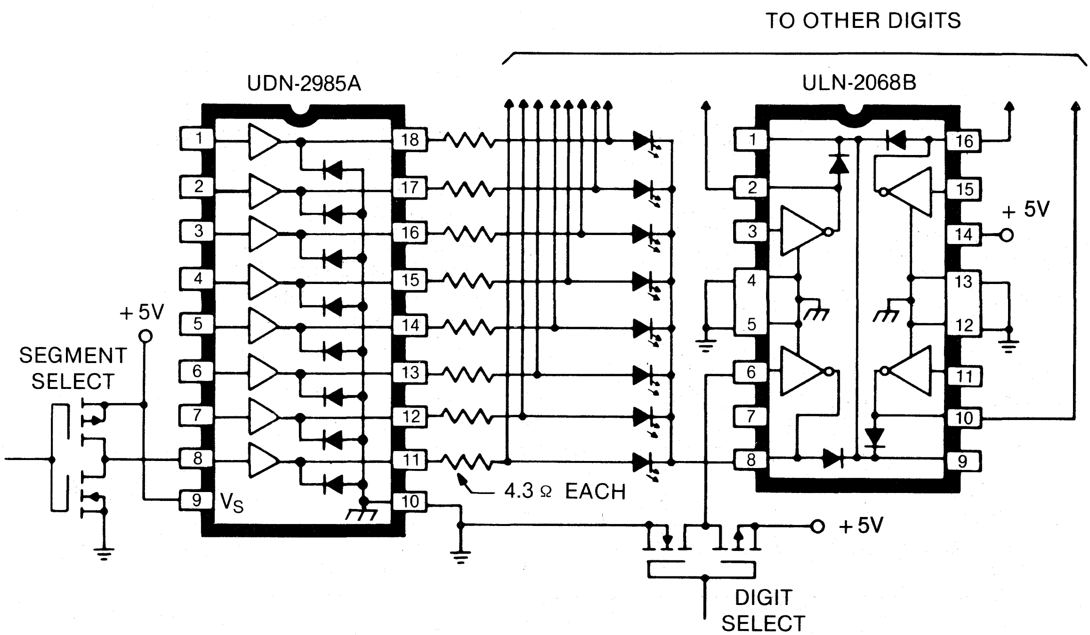
Driver Supply Voltage, V_S	30 V
Continuous Output Current, I_{OUT}	−300 mA
Input Voltage, V_{IN}	20 V
Package Power Dissipation, P_D	2.2W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at rate of 18 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = 30 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	Both	V_{IN} = 0.4 V, V_{OUT} = 0 V	—	−100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	Both	V_{IN} = 0.4 V, I_{OUT} = −25 mA	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	UDN-2985A	V_{IN} = 2.4 V, I_{OUT} = −60 mA	—	1.1	V
			V_{IN} = 2.4 V, I_{OUT} = −120 mA	—	1.2	V
		UDN-2986A	V_{IN} = 4.0 V, I_{OUT} = −60 mA	—	1.1	V
			V_{IN} = 4.0 V, I_{OUT} = −120 mA	—	1.2	V
Input Current	$I_{IN(ON)}$	UDN-2985A	V_{IN} = 2.4 V	—	225	μA
			V_{IN} = 5.0 V	—	650	μA
		UDN-2986A	V_{IN} = 4.0 V	—	250	μA
			V_{IN} = 15 V	—	1150	μA
	$I_{IN(OFF)}$	Both	V_{IN} = 0.4 V	—	10	μA
Clamp Diode Leakage Current	I_R	Both	V_R = 30 V, T_A = 70°C	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	I_F = 120 mA	—	2.0	V

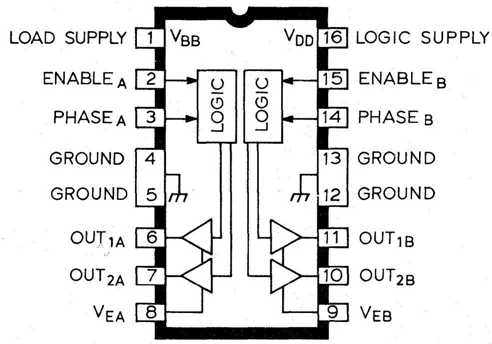
COMMON-CATHODE LED DRIVER



UDN-2993B
DUAL H-BRIDGE MOTOR DRIVER

FEATURES

- ±600 mA Output Current
- Output Voltage to 40 V
- Crossover Current Protection
- TTL/NMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- Plastic DIP With Heat-Sink Tabs (Machine Insertable)



Dwg. No. A-12,455

BRUSHLESS D-C or bipolar stepper motors to 40 V and 500 mA per phase are economically driven with the Type UDN-2993B dual H-bridge driver. Each of the pair of full-bridge drivers has separate input level shifting, internal logic, source and sink drivers in an H-bridge configuration, and internal clamp diodes.

The device provides an internally-generated dead-time to prevent crossover currents during changes in load-current phase. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Except for supply voltages, the two H-bridges are independent. The ENABLE function is provided for each bridge to allow pulse-width (chopper) modulation with the use of external comparators. The chopper-drive mode is characterized by low power-dissipation levels and maximum efficiency.

A PHASE input to each bridge determines load-current direction. In addition, the emitters from each bridge are externally available to allow the addition of current-sensing circuitry.

The Type UDN-2993B integrated circuit is supplied in a 16-pin dual in-line plastic package with a copper lead frame for optimum power dissipation without a heat sink. The lead configuration allows automatic insertion, fits a standard integrated circuit socket or printed wiring board layout, and enables easy attachment of a heat sink for maximum power-handling capability. The heat-sink tabs are at ground potential and require no insulation.

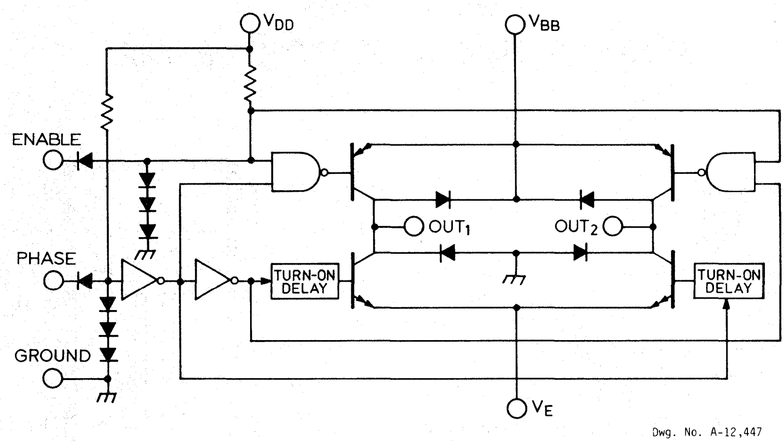
A full-bridge bipolar driver with a current rating of ±3.5 A is supplied as Type UDN-2952B. It is described in Sprague Engineering Bulletin 29319.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

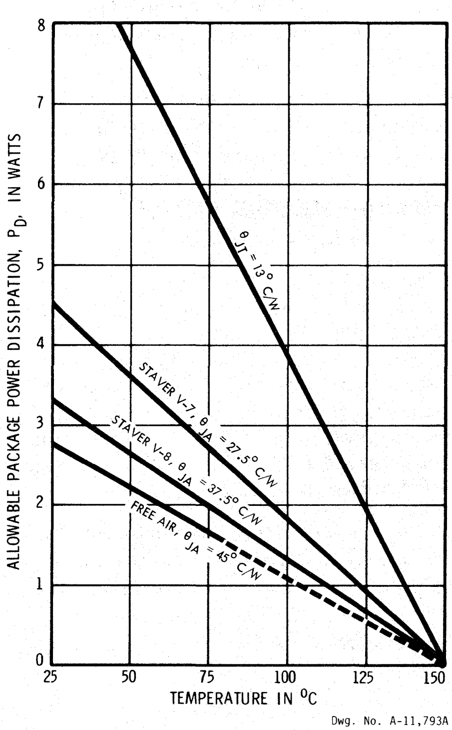
Load Supply Voltage, V_{BB}	40 V
Logic Supply Voltage, V_{DD}	7.0 V
Logic Input Voltage Range, V_{PHASE} or V_{ENABLE}	−0.3 V to V_{CC} + 0.3 V
Output Current, I_{OUT}	±600 mA
Sink Driver Emitter Voltage, V_E	1.5 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

NOTE: Output current rating may be limited by chopping frequency, ambient temperature, air flow, and heat sinking. Under any set of conditions, do not exceed the specified maximum current and a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.

TRUTH TABLE

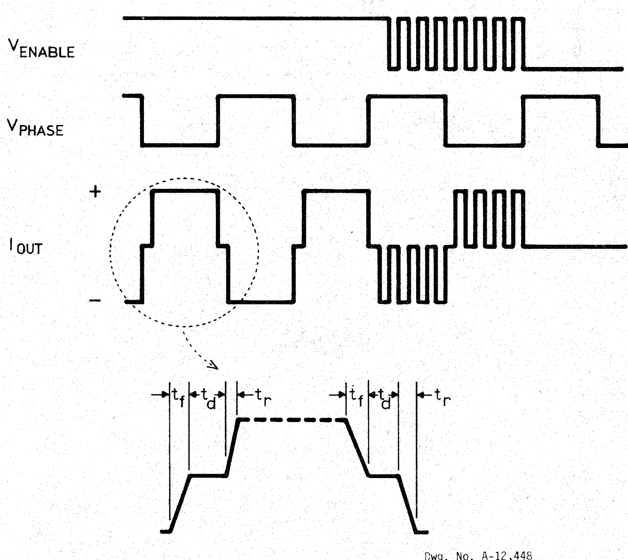
Enable Input	Phase Input	Output 1	Output 2
High	High	Low	High
High	Low	High	Low
Low	High	Low	Open
Low	Low	Open	Low

3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 40 V, V_{DD} = 5 V, V_E = 0 V, $T_{TAB} \leq$ +70°C Figure 1 (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		20	—	40	V
Output Leakage Current	I_{CEX}	V_{ENABLE} = 0.8 V, V_{OUT} = V_{BB}, Note 2	—	<1.0	10	μA
		V_{ENABLE} = 0.8 V, V_{OUT} = 0 V, Note 2	—	<−1.0	−10	μA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 2.4 V, I_{OUT} = 500 mA	—	1.6	1.8	V
		V_{ENABLE} = 2.4 V, I_{OUT} = −500 mA	—	1.6	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±500 mA, Figure 2, Note 2	40	50	—	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 2.4 V, Outputs Open, Note 2	—	1.0	3.0	mA
	$I_{BB(OFF)}$	V_{ENABLE} = 0.8 V, Outputs Open, Note 2	—	<1.0	10	μA
Source Driver Rise Time	t_r	I_{OUT} = −500 mA, V_{BB} = 30 V	—	250	—	ns
Source Driver Fall Time	t_f	I_{OUT} = −500 mA, V_{BB} = 30 V	—	500	—	ns
Deadtime	t_d	I_{OUT} = ±500 mA, V_{BB} = 30 V	—	1.5	—	μs
Clamp Diode Forward Voltage	V_F	I_F = 500 ma	—	1.6	1.8	V
Control Logic (PHASE or ENABLE)						
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.4 V	—	<1.0	10	μA
	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8 V	—	−200	−300	μA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	14	20	mA
Turn-on Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	75	—	ns
Turn-off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	280	—	ns

NOTES: 1. Each driver is tested separately.
2. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
3. Negative current is defined as coming out of (sourcing) the specified device pin.



TEST FIGURES

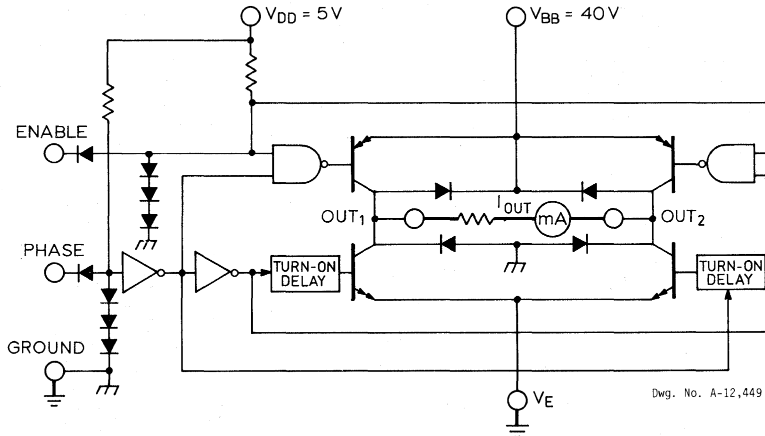


FIGURE 1

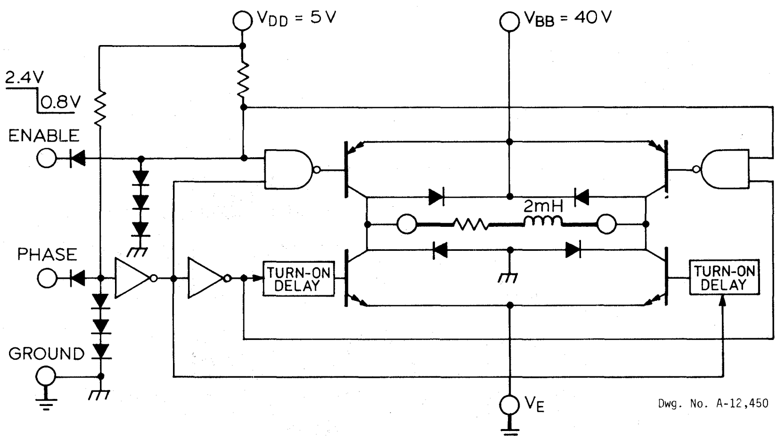


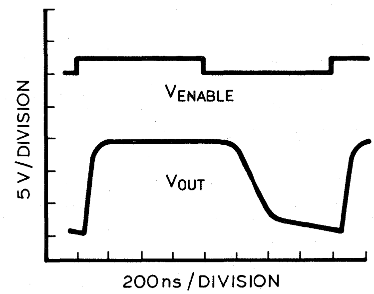
FIGURE 2

APPLICATIONS INFORMATION

1. The output waveform for a chopping frequency of 600 kHz, and a 50-ohm resistive load, is shown in Figure 3. With higher load resistances, the fall time may increase significantly.

2. While switching the PHASE input, the d-c cross-over during each polarity transition is eliminated by means of the internally generated deadtime delay (t_d). If the load is resistive, both outputs float during t_d. If the load is inductive, one output goes to $V_{BB} + V_F$ (clamp diode) while the other output goes to $-V_F$, quickly discharging the inductance.

3. The clamp-diode power loss at 30 kHz is 500 mW. This loss can be significantly reduced by paralleling the internal diodes with external high-speed diodes. Switching losses during the rise and, particularly, the fall transitions also limit the maximum frequency of operation with an inductive load.



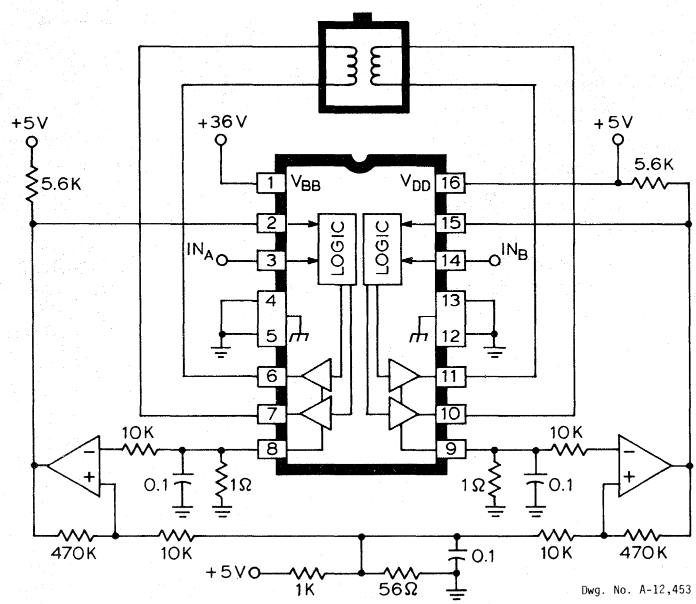
Dwg. No. A-12,451

FIGURE 3
V_{BB} = 30 V
R_L = 50 Ω
f = 600 kHz

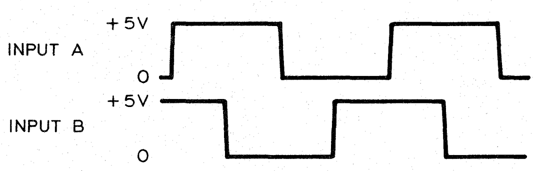
3

TYPICAL APPLICATION

2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)



Dwg. No. A-12,453

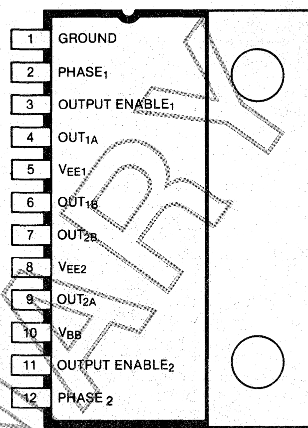


Dwg. No. A-12,454

UDN-2998W
DUAL FULL-BRIDGE MOTOR DRIVER

FEATURES

- Output Current to 3 A (peak)
- Output Voltage of 50 V
- TTL, DTL, 5 V CMOS Compatible Inputs
- Integral Output Suppression Diodes
- V_{SENSE} Pin for Current Sensing
- Internal Thermal Shutdown Circuitry
- Cross Over Current Protected



The UDN-2998W is a dual full-bridge motor driver which accepts standard TTL, DTL, and 5 V CMOS inputs and drives loads up to 50 V and 2 amps/bridge.

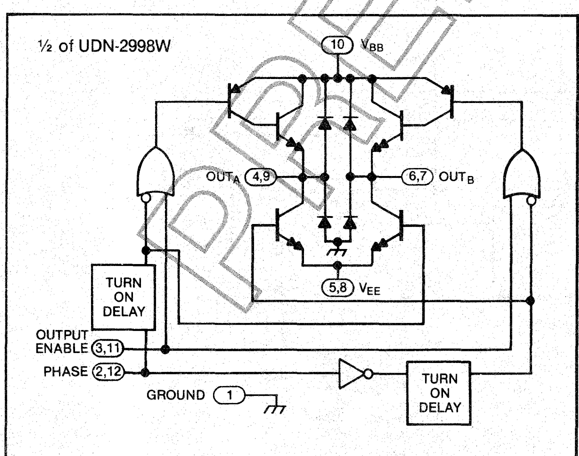
The UDN-2998W is ideal for use in driving bi-directional d-c motors or solenoids, two phase stepper or brushless motors operating with continuous load currents of up to 2 A and peak start-up currents of 3 A.

These monolithic integrated circuits have extensive circuit protection. Each driver has a thermal shutdown network that disables load drive if package power dissipation ratings are exceeded. This device is crossover current-protected and internal diode transient suppression is provided on-chip.

Emitters of sink drivers have been pinned out for connection to external current-sensing resistors. For external PWM control an OUTPUT ENABLE for each bridge circuit has been provided which can be very useful in microprocessor control applications.

The UDN-2998W is packaged in a 12-pin single in-line power tab package for higher power capabilities. Driving either of the bridges at the full 2 A d-c rating will require the use of an external heat-sink.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

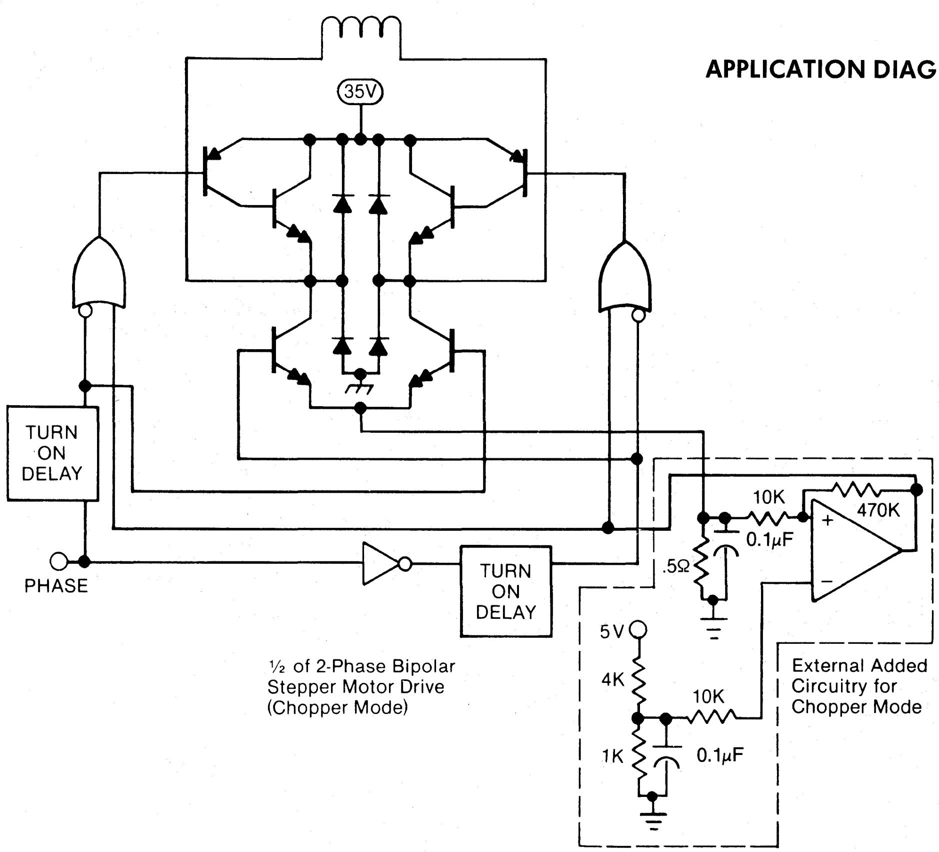
Output Voltage, V_{CE}	50 V
Power Supply, V_{BB}	50 V
Output Current, I_{OUT} (DC)	2 A
(PEAK)	3 A
Package Power Dissipation, P_D (Free Air)	5.2 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 41.6 mW/°C θJA = 24°C, θJC = 3°C/W.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Power Supply Voltage Range	V_{BB}		10	50	V
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	50	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 2 A, L = 3.5 mH	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 2 A, Sink Driver	—	2.0	V
		I_{OUT} = −2 A, Source Driver	—	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	μA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	2.0	V
Input Voltage	$V_{IN(0)}$	I_{OUT} = 1.0 A, OUTPUT ENABLE = 0 V	0.8	—	V
	$V_{IN(1)}$	I_{OUT} = 1.0 A, OUTPUT ENABLE = 0 V	—	2.0	V
Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V, All Inputs	—	100	μA
	$I_{IN(1)}$	V_{IN} = 2.0 V, All Inputs	—	10	μA
Supply Current	I_{BB}	Both Bridges ON, No Load	—	12	mA
Turn-On Delay	t_{ON}	0.5 E_{IN} to 0.5 E_{OUT}	—	4.0	μs
Turn-Off Delay	t_{OFF}	0.5 E_{IN} to 0.5 E_{OUT}	—	1.0	μs

APPLICATION DIAGRAM



½ of 2-Phase Bipolar Stepper Motor Drive (Chopper Mode)

RELIABILITY OF SERIES ULN-2000A AND ULN-2800A HIGH-CURRENT DARLINGTON DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series ULN-2000A and ULN-2800A integrated circuits and provides information that can be used to calculate the failure rate at normal junction operating temperatures.

3

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at an ambient temperature of +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.
2) Accelerated testing is performed at junction temperatures above +125°C and is used to generate failure-rate data.
3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Tables Ia and Ib contain data produced by life tests that were conducted at +150°C and +175°C. The data include the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing alloca-

TABLE Ia
TEST RESULTS at T_J = +150°C

TEST NUMBER	QTY.	90	150	300	600	1200	1800	2400	3000	5000
		HOURS ON TEST / NUMBER OF FAILURES								
1	12	0	0	0	0	2	0	—	—	—
2	22	0	0	0	0	0	0	0	0	—
3	22	0	0	0	0	0	0	0	0	—
4	22	0	0	2	0	0	3	0	0	—
5	22	0	0	0	0	0	0	0	0	—
6	22	0	0	0	0	0	1	0	0	—
7	12	0	0	0	0	0	0	—	—	—
8	12	0	0	0	0	0	0	—	—	—
9	90	0	0	0	2	0	0	—	—	—
10	12	0	0	0	0	0	0	—	—	—
11	12	0	0	0	0	0	0	—	—	—
12	12	0	0	0	0	0	0	0	0	—
13	12	0	0	0	0	0	0	0	0	—
14	35	0	0	0	0	0	0	1	—	—
15	12	0	0	0	1	1	0	0	0	0
16	25	0	0	0	0	0	—	—	—	—
17	25	0	0	0	0	0	—	—	—	—
TOTAL ON TEST		381	381	381	379	376	323	173	138	10
TOTAL FAILURES		0	0	2	3	3	4	1	0	0
TOTAL GOOD		381	381	379	376	373	319	172	138	10
P_s		1.00	1.00	0.995	0.992	0.992	0.988	0.994	1.00	1.00
Cumulative P_s		1.00	1.00	0.995	0.987	0.979	0.967	0.961	0.961	0.961
$P_f = 1 - P_s$		0	0	0.005	0.013	0.021	0.033	0.039	0.039	0.039
Cumulative % Failures		0	0	0.5	1.3	2.1	3.3	3.9	3.9	3.9

tion of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 40 hours at +175°C or 200 hours at +150°C to 1000 hours of qualification life test at +125°C.

The data at the bottom of Tables Ia and Ib were compiled by calculating the probability of success (P_s), the cumulative probability of success, the probabilityof failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% failure point. The mediam life at a junction temperature of +150°C is 1.6 × 10^5 hours. At +175°C, the median lifetime is 3.0 × 10^4 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^o e^{-\epsilon/kT}$$

where V_r^o = a constant
ϵ = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5710M, and Series UDN-2980A devices at

3

TABLE Ib
TEST RESULTS at T_J = +175°C

TEST NUMBER	QTY.	90	150	300	600	1200	1800	2400	3000	5000
		HOURS ON TEST / NUMBER OF FAILURES								
1	25	0	0	0	7	—	—	—	—	—
2	25	0	0	0	0	0	0	0	—	—
3	25	0	0	1	2	1	0	0	—	—
4	24	0	1	0	1	0	0	0	0	—
5	19	0	0	0	0	0	0	—	—	—
6	19	0	0	0	0	0	0	—	—	—
7	12	0	0	2	3	2	—	—	—	—
8	12	0	0	0	0	0	—	—	—	—
9	12	0	0	0	0	0	0	—	—	—
10	18	0	0	0	0	0	—	—	—	—
11	12	0	0	0	0	0	2	0	0	2
12	12	0	0	0	0	0	0	—	—	—
13	12	1	0	0	0	0	0	0	—	—
14	18	0	0	1	2	0	7	—	—	—
15	12	1	0	0	0	0	0	—	—	—
16	12	0	0	0	0	0	—	—	—	—
17	24	0	0	0	0	0	0	—	—	—
18	12	0	1	0	1	0	0	0	0	—
19	24	0	0	0	0	0	—	—	—	—
TOTAL ON TEST		329	327	325	321	287	213	99	42	10
TOTAL FAILURES		2	2	4	16	3	9	0	0	2
TOTAL GOOD		327	325	321	305	284	204	99	42	8
P_s		0.994	0.994	0.988	0.950	0.990	0.958	1.00	1.00	0.800
Cumulative P_s		0.994	0.988	0.976	0.927	0.917	0.879	0.879	0.879	0.703
$P_f = 1 - P_s$		0.006	0.012	0.024	0.073	0.083	0.121	0.121	0.121	0.300
Cumulative % Failures		0.6	1.2	2.4	7.3	8.3	12.1	12.1	12.1	30.0

multiple temperatures. Failure analysis of devices rejected during this testing of Series ULN-2000A and ULN-2800A also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line drawn through +150°C and +175°C failure points has a slope corresponding to that of the 1.0 eV failure mechanism.

Figure 1
CUMULATIVE PERCENT OF FAILURES

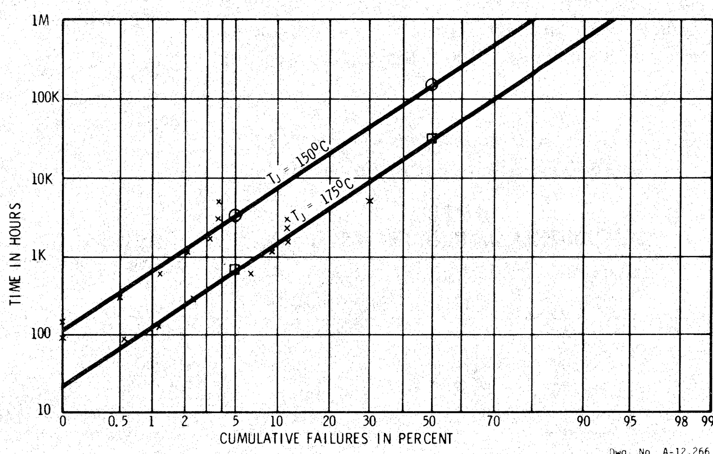
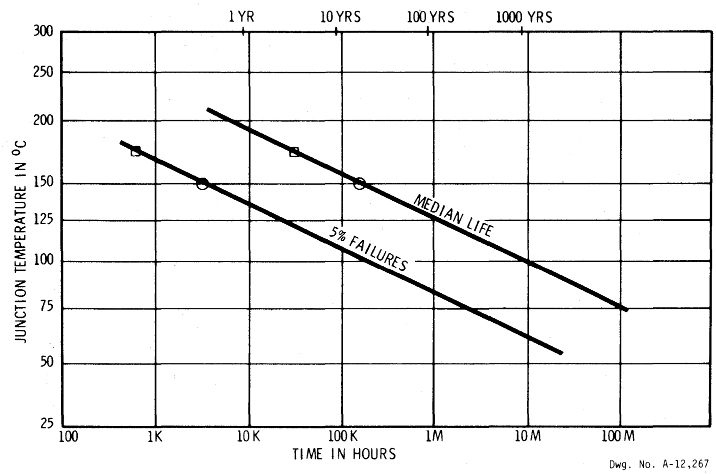


Figure 2
MEDIAN LIFE



Although not as statistically accurate as the median lifetime, the 5% failure point can be read from Figure 1. It is plotted in Figure 2.

The median life with lower junction temperatures can now be determined by using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\theta_{JA} + T_A \text{ or } T_J = P_D\theta_{JC} + T_C$$

The median lifetime, or 50% failure point, as determined in Figure 2, is approximately 100 years at +125°C or 1,000 years at +100°C junction temperature.

The approximate failure rate (FR) can be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(8.8 \times 10^6 \text{ hours})$$
$$= 0.0011\%/1000 \text{ hours} = 11 \text{ FIT}$$

where *FIT* = failures per 10^9 unit-hours

TABLE II
SERIES ULN-2000A AND ULN-2800A FAILURE RATE

T_J (°C)	Median Life (h)	Failure Rate (%/1000 h)	Failures In Time (No./10^9 unit-hours)
125	1.0×10^6	0.010	100
100	8.8×10^6	0.0011	11
75	1.0×10^8	0.00010	1.0
50	8.8×10^8	0.000011	0.11

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calcualted from internal power dissipation and external ambient temperature, would not reach the 5% failure point in 10 years. Lowering the junction temperature to +70°C increases the time to the 5% failure point to 300 years.

A complete sequence of environmental tests on Series ULN-2000A and ULN-2800A, including temperature cycle, pressure cooker, and biased humidity tests are continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K. E., and Bird, D. W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions,* Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook,* Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.,* p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control,* 1961, pp. 208-213.

Knowing 'inductive logic' keeps power interface ICs alive and switching

When it comes to inductive loads, keeping within a few critical specifications and good design practices protect chips from premature burnout.

Integrated circuits that carry both logic and bipolar power devices—whether for driving print hammers, servos, steppers, relays, or brushless dc motors—are going a long way toward consolidating industrial-control electronics. Though these power interface ICs greatly simplify the system designer's task, they must be implemented carefully when they operate an inductive load.

To do so, the engineer must fully understand how the device's fundamental specifications relate to that inductive load, ensuring that the chip's breakdown limits are never exceeded. For example, the designer must be able to distinguish between the vaguely similar but quite different output-voltage specifications and know how to clamp transients since they cannot be prevented. The limitations and idiosyncrasies of ever-present parasitic elements also need to be well understood if the device is to operate flawlessly.

The biggest roadblocks to successful circuit design are two frequently misunderstood specifications. The first is the power interface chip's maximum output voltage, V_{CEX}. In most cases, this parameter approximates BV_{CBO}, the minimum collector-base breakdown voltage with the emitter lead open. The actual designation would be BV_{CEX}, which denotes that there is a standard resistance in the emitter lead. It should not be exceeded at any time, especially if the load is inductive.

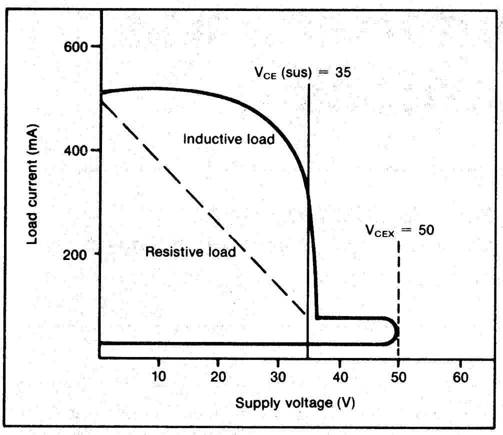
The maximum collector-base breakdown value for a given IC is confirmed by applying a voltage to the device's output to measure its maximum leakage current, which is specified in the data sheet. Operating any load above the voltage that may produce the maximum leakage current is thus unsafe. Even with resistive loads, the user may encounter occasional trouble if the load line is steep. Trouble occurs because the line may cross the point equal to the minimum collector-emitter sustaining voltage.

The second fundamental specification, $V_{(CE)}$ (sus), is the greatest voltage that the chip can sustain under worst-case conditions. This limit is determined by the minimum collector-emitter voltage for a specified output current. It can also be measured with a coil dump test, in which the IC's output is switched off and its output voltage measured. Generally, the first test is done at 5% to 10% of the nominal output current for a given application. The coil test is often run at a high output current and for a specified inductance. Either of these conditions will satisfactorily confirm a device's minimum output-sustaining voltage.

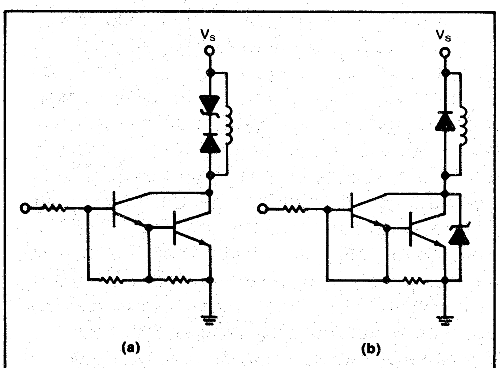
Switching inductive loads with interface ICs, then, demands careful attention to both the device's load line and the guaranteed output-sustaining voltage. With inductive loads, reactive voltages often greatly exceed the source voltages when the chip is switched off (Fig. 1). The source voltage is clamped off to a safe value with fly-back diodes that are effectively shunted across the inductive load and are often internal to the device. Without such protection, or that offered by resistor-capacitor snubbing networks, the high voltage that results from switching the coil will likely damage or destroy the device. Unfortunately, internal protection alone is often insufficient, and external clamping circuitry must be added.

Of great concern to the designer is that insufficient output protection may result in gradual —and thus hard to detect—secondary breakdown. Particularly hardy power interface chips may seem to stand up well to occasional transients in excess of 100 V for a load supply voltage of 12 V; that is, until they suddenly fail.

When fast switching is a must, it is generally only achieved with a circuit that allows the output voltage to rise fast and exceed the supply voltage. For such approaches, other schemes must be used. Typically, both external zener diodes and resistors should be employed. Together, they furnish inexpensive protection. Zener diodes, however, are often used alone.



1. The limits of power interface chips are more likely to be exceeded when operating inductive loads due to the reactive voltages generated by switching. Also, the collector-emitter potential may be above the supply voltage. Thus designs must ensure the dc operating voltage stays below the device's minimum sustaining voltage, V_{CE} (sus), for a given quiescent load current. In no case should its maximum output voltage, V_{CEX}, be exceeded.



2. Arranging a zener-diode network in series to clamp a power interface chip's output allows its fly-back voltage to rise above the supply voltage, enabling the device to be turned off faster (a). When poorly regulated supply voltages power a circuit that drives multiple devices whose voltage transients exceed the chip's capability, a parallel configuration is preferred (b).

Dropping the resistor

The reason for this apparent omission is obvious once it is realized that the fly-back voltage is not only a function of current and resistance but also of the number of outputs switching off at any time. Only well-defined or simultaneous switching sequences are suitable for resistors; without either, the magnitude of the voltage transient produced is difficult to determine. Some industrial timing circuits may be both low-speed and predictable; unfortunately, random switching is the rule rather than the exception.

Zener diodes, on the other hand, do not suffer from that limitation. The voltage rating for a series arrangement (Fig. 2a) is determined by:

$$V_Z = V_{CE}(sus) - V_{supply} - V_F$$

where V_F is the diode's forward-voltage drop. Thus for an IC with a sustaining voltage of 35 V, a 15-V supply, and a diode drop of 2 V, the maximum zener value is 18 V. For designs that use many power ICs for multiple loads, it is often practical to work with multiple zener diodes with lower power and maximum current ratings. That avoids the cost of power devices and sidesteps their need for heat sinks.

Zener diodes can be placed in parallel across the output as well (Fig. 2b). In this case, the zener voltage must be slightly below the minimum sustaining voltage. Automotive systems, for one, typically employ internal 30- to 35-V clamps in their interface chips because such operations as "jump starting" two or three 12-V batteries precludes the series approach. A setup exhibiting an unregulated supply voltage, which varies considerably, may also necessitate the parallel clamping approach.

Beyond staying within the chip's maximum voltage rating, the designer's second major concern is avoiding problems created by inherent parasitic elements. In the early days of the TTL device and its gold-doped low-resistivity silicon, parasitic problems were virtually nonexistent. (Adding gold to improve circuit speed effectively killed parasitic elements.) Linear bipolar ICs and a wider range of power loads make parasitic concerns much more of an issue. The vast majority of today's chips are junction-isolated ICs and they all demonstrate such unwanted by-products inherent in their fabrication processes.

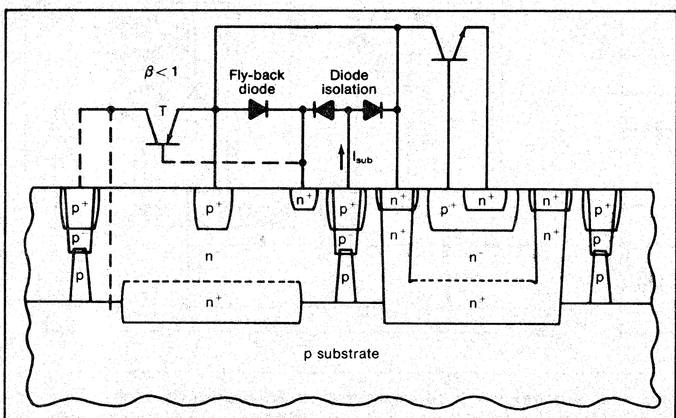
The most common parasites pertaining to inductive loads are the vertical pnp and lateral npn transistors that are created by a device's protection circuitry. The internal fly-back diode of a power interface chip, for instance, becomes a low-gain transistor (Fig. 3).

Most circuits are not affected by this parasitic transistor, unless the switching frequency is above the audio range. Curiously enough, many of the problems are related to power dissipation. The parasitic transistor often draws considerable power, thus raising the chip's temperature, even when the transistor's gain is below unity.

3

Minimizing the problem

Where practical, lowering the supply voltage and decreasing the pulse repetition rate will minimize the trouble. When high switching rates and maximum source voltages are necessary, the best technique is to place a discrete diode across the devices' output stage, between collector and the supply line (or to ground if zener clamping is used). A discrete diode, with



3. The interface IC's fly-back diode almost always creates a parasitic transistor (T) at the device's output. Further, substrate currents form a transistor across the diodes that isolate various junctions of the chip. Moreover, parasitic diodes at the inputs also are common. Adding external protection diodes at both the input and output eliminates many undesired circuit operations such as false triggering. Further, it may well prevent the device from being destroyed by the positive feedback currents that are occasionally generated.

its lower forward-voltage drop, effectively shunts the fly-back diode and will conduct most of the current during clamping.

Less troublesome, but still of concern, are the lateral parasitics that may cause circuit anomalies and malfunctions. In many stepper motors particularly, the transformer action of the motor windings produces undesirable substrate currents into the IC. In effect, a negative voltage is applied at the device's output, and current is injected into its substrate.

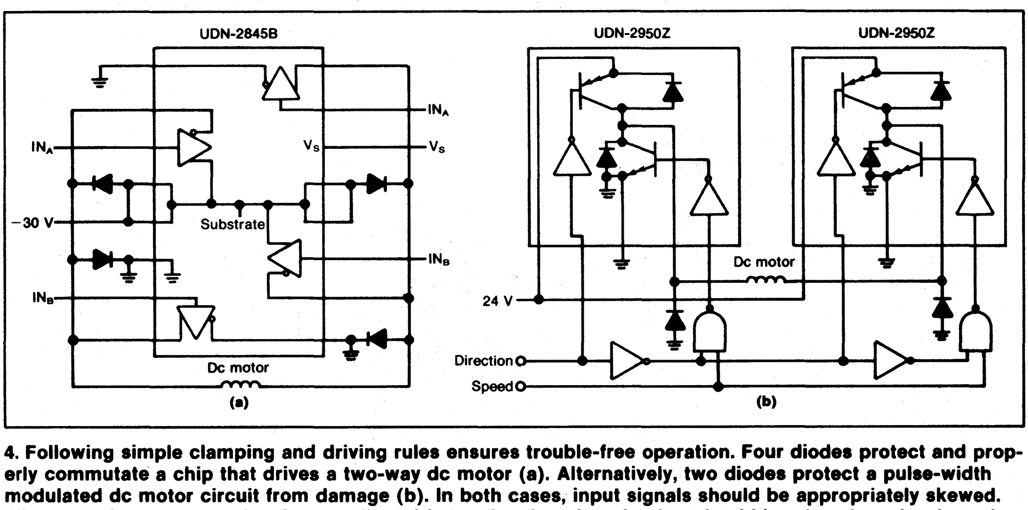
The problem is exacerbated by the IC's junction isolation, which produces a parasitic transistor across the isolation diodes (the transistor's base lead is connected at their junction). Frequently, current injected into the device's output is sufficient to create formidable substrate currents, thus turning all lateral transistors on.

As a result, the device's leakage current may increase, and the chip may be inadvertently activated. In extreme cases, positive feedback causes the IC to destroy itself. Circuits employing small low-current stepper motors are not generally a problem, since the substrate current is seldom sufficient to turn on the transistor. In high-current applications, however, putting a discrete diode across the output device's collector-ground junction will cure the problem.

A parasitic diode exists at the input circuit to most power interface chips. In many instances, it may hinder circuit operation when a negative voltage is applied to the input, since substrate currents may be created. Connecting a discrete back-biased diode directly between input and ground diverts current away from the substrate. Provisions should be made, though, for limiting the current if the input state is to be pulled to voltages well below ground.

Turning it over

Employing power interface ICs to drive motors demands adherance to four basic design rules. First, if the device is without internal protection, diodes must be added to clamp both positive and negative overshoots caused by inductive loads. Second, if the device is protected with internal clamps, external diodes could be added. That not only serves as insur-



4. Following simple clamping and driving rules ensures trouble-free operation. Four diodes protect and properly commutate a chip that drives a two-way dc motor (a). Alternatively, two diodes protect a pulse-width modulated dc motor circuit from damage (b). In both cases, input signals should be appropriately skewed. When transistors are used as intermediate drivers, the clamping circuitry should be placed as closely to the motor as possible.

ance but eliminates the effects of parasitic elements, which occasionally trigger or even destroy the chip. Third, in balanced-drive arrangements, complementary input signals should be appropriately skewed. Doing so avoids crossover currents that may cause excessive heating and reduce available output current. Finally, when it is unclear if the interface chip furnishes suitable drive to the motor—or if it is difficult to damp the effects of parasitics at high outputs—discrete bipolar transistors and appropriate clamping may be the solution. The transistors driven by the chip, in turn power the motor.

Consider a dc motor circuit driven by a 1.5-A quad Darlington device that uses four discrete diodes for protection and commutation (Fig. 4a). The configuration, which employs a so-called bipolar, or bridge arrangement, allows the motor to turn either clockwise or counterclockwise.

Half bridge operation

Alternatively, the half-bridge motor driver run by a pair of chips also makes possible bipolar operation (Fig. 4b). Further, speed is controlled by a pulse-width-modulated waveform. Clamping diodes on either side of the motor take care of the problems caused when the motor changes direction. And with minimal modification, the driving circuitry accommodates ac motors as well. More specifically, no clamping diode is required between pin 4 of each device and ground. The designer need only build circuitry to control the speed of the motor; no circuitry for defining its direction is required. As before, pins 2 and 5 of each device accept complementary driving signals.

Where intermediate, or discrete, bipolar transistors drive a dc motor, it is always best to install any clamping or commutating diodes close to the motor itself. Otherwise, inductive undershoots or overshoots may find their way through the transistors, triggering or damaging them or the power interface chip. □

SECTION 4—BiMOS AND COMPLEX ARRAY INTERFACE DRIVERS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

4

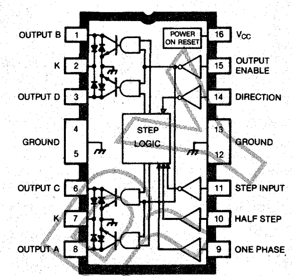
SELECTION GUIDE TO BiMOS ARRAYS AND COMPLEX DEVICES

Device Type	Description	Absolute Maximum Ratings I_{OUT}	Absolute Maximum Ratings V_{OUT}
Serial-Input, Latched Drivers			
UCN-5825B	4-Bit	2.0 A	60 V
UCN-5826B	4-Bit	2.0 A	80 V
UCN-5821A and 5841A	8-Bit	500 mA	50 V
UCN-5822A and 5842A	8-Bit	500 mA	80 V
UCN-5823A and 5843A	8-Bit	500 mA	100 V
UCN-5895A	8-Bit Saturated Drivers	−250 mA	50 V
UCN-5891A/B	8-Bit	−500 mA	50 V
UCN-5890A/B	8-Bit	−500 mA	80 V
UCN-5810A	10-Bit	−40 mA	60 V
UCN-5810A-1	10-Bit	−40 mA	80 V
UCN-5910A	10-Bit	50 mA	150 V
UCN-5811A	12-Bit	−40 mA	80 V
UCN-5812A	20-Bit	−40 mA	60 V
UCN-5812A-1	20-Bit	−40 mA	80 V
UCN-5851A/EP	32-Bit (No Latches)	80 mA	225 V
UCN-5852A/EP	32-Bit (No Latches)	80 mA	225 V
UCN-5853A/EP	32-Bit	±50 mA	80 V
UCN-5854A/EP	32-Bit	±50 mA	80 V
UCN-5832A/C	32-Bit Saturated Drivers	150 mA	40 V
UCN-5833A/C/EP	32-Bit	125 mA	30 V
UCN-5818A	32-Bit	−40 mA	60 V
UCN-5818A-1	32-Bit	−40 mA	80 V
Parallel-Input, Latched Drivers			
UCN-5900A	4-Bit	400 mA	150 V
UCN-4401A and 5800A	4-Bit	500 mA	50 V
UCN-5813B and 5814B	4-Bit	1.5 A	50 V
UCN-5813B-1 and 5814B-1	4-Bit	1.5 A	80 V
UCN-5881EP	8-Bit (with Readback)	50 mA	20 V
UCN-5901A	8-Bit	400 mA	150 V
UCN-5801A	8-Bit	500 mA	50 V
UCN-5815A	8-Bit	−40 mA	60 V
UCN-5815A-1	8-Bit	−40 mA	80 V
Special-Purpose Functions			
UCN-4202A	Stepper-Motor Translator/Driver	600 mA	20 V
UCN-4203A	Stepper-Motor Translator/Driver	600 mA	50 V
UCN-4204B	Stepper-Motor Translator/Driver	1.5 A	20 V
UCN-4205B	Stepper-Motor Translator/Driver	1.5 A	50 V
UCN-4805A	Latched 7-Segment Decoder/Driver	−40 mA	60 V
UCN-4807A	Addressable, Latched Octal Drivers	200 mA	40 V
UCN-4808A	Addressable, Latched Octal Drivers	600 mA	40 V
UCN-5816A	Addressable, Latched Hexadecimal Drivers	500 mA	60 V

UCN-4204B AND UCN-4205B STEPPER MOTOR TRANSLATOR DRIVERS

FEATURES

- High Output Current Capability
- Direct Control
- Half Step, Full Step Drive Formats
- Internal Clamp Diodes
- Output Enable
- Internal Thermal Shutdown
- Power ON Reset



The UCN-4204B and UCN-4205B devices provide control and drive to unipolar 4-phase stepper motors up to 1.5 A/phase and 15 V (UCN-4204B) or 35 V (UCN-4205B). In addition to direct drive capability these devices feature on-chip I²L logic to provide direction, output enable, step enable, thermal shutdown, power-on reset functions as well as one phase (wave drive), two phase, and half step drive formats.

One phase consists of energizing one motor phase at a time in an A-B-C-D sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding imbalance in the motor.

Two phase "ON" drive energizes two adjacent phases in each detent position. The two phase "ON" mode offers an improved torque-speed product, greater detent torque and is less susceptible to motor resonance.

Half step excitation alternates between the one phase "ON" and two phase "ON" modes, providing an eight step sequence.

The UCN-4204B and UCN-4205B differ only with respect to their output breakdown capability, the UCN-4204B has a minimum 20 volt breakdown and the UCN-4205B has a 50 volt breakdown.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . 7.0 V
Output Voltage, V_K, V_{CE} (UCN-4204B) . . . . 20 V
(UCN-4205B) . . . . 50 V
Input Voltage, V_{IN} . . . . 7.0 V
Output Sink Current, I_{OUT} . . . . 1.5 A
Package Power Dissipation, P_C . . . . 2.77 W*
Operating Ambient Temperature Range, T_A . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +125°C

*Derate at rate of 22.2 mW/°C above T_A = 25°C.

WAVE DRIVE SEQUENCE

Half Step = L, One Phase = H (DIRECTION = 0 ↓, DIRECTION = 1 ↑)

Step	A	B	C	D
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
3	OFF	OFF	ON	OFF
4	OFF	OFF	OFF	ON

TWO-PHASE DRIVE SEQUENCE

Half Step = L, One Phase = L (DIRECTION = 0 ↓, DIRECTION = 1 ↑)

Step	A	B	C	D
POR	ON	OFF	OFF	ON
1	ON	OFF	OFF	ON
2	ON	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	ON

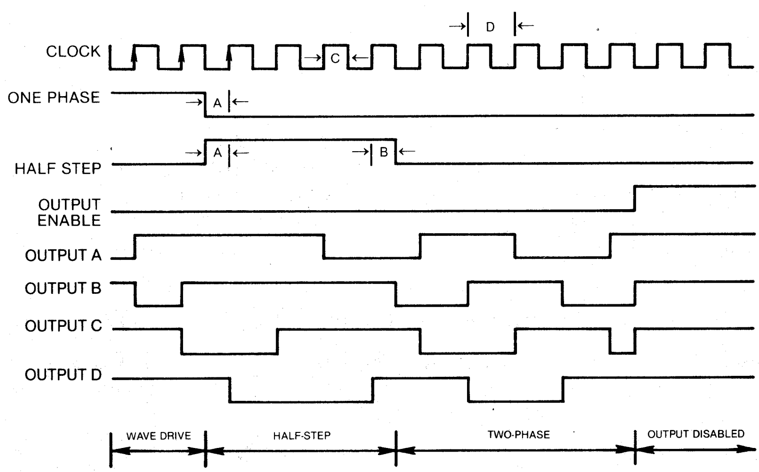
HALF STEP DRIVE SEQUENCE

Half Step = H, One Phase = L (DIRECTION = 0 ↓, DIRECTION = 1 ↑)

Step	A	B	C	D
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	OFF	ON	OFF	OFF
4	OFF	ON	ON	OFF
5	OFF	OFF	ON	OFF
6	OFF	OFF	ON	ON
7	OFF	OFF	OFF	ON
8	ON	OFF	OFF	ON

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 5 V, T_{TAB} ≤70°C

Characteristics	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Supply Current	I_{CC}	All	2 Drivers ON	—	85	mA
Input Current	$I_{IN(1)}$	All	V_{CC} = 4.5 V, V_{IN} = 2.0 V, T_A = 25°C	—	5.0	µA
	$I_{IN(0)}$	All	V_{CC} = 4.5 V, V_{IN} = 2.0 V, T_A = 70°C	—	40	µA
		All	V_{CC} = 5.5 V, V_{IN} = 0.8 V	—	−1.6	mA
Input Voltage	$V_{IN(1)}$	All	V_{CC} = 4.5 V	2.0	—	V
	$V_{IN(0)}$	All	V_{CC} = 5.5 V	—	0.8	V
Input Clamp Voltage	V_{IN}	All	I_{IN} = −12 mA	—	−1.5	V
Output Leakage Current	I_{CEX}	UCN-4204A	V_{CC} = 5.5 V, K = Open, V_{OUT} = 20 V	—	500	µA
		UCN-4205A	V_{CC} = 5.5 V, K = Open, V_{OUT} = 50 V	—	500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	UCN-4204A	V_{CC} = 4.5 V, I_{OUT} = 700 mA	—	0.5	V
			V_{CC} = 4.5 V, I_{OUT} = 1.0 A	—	0.7	V
			V_{CC} = 4.5 V, I_{OUT} = 1.25 A	—	1.0	V
		UCN-4205A	V_{CC} = 4.5 V, I_{OUT} = 700 mA	—	0.8	V
			V_{CC} = 4.5 V, I_{OUT} = 1.0 A	—	1.0	V
			V_{CC} = 4.5 V, I_{OUT} = 1.25 A	—	1.3	V
Output Sustaining Voltage	$V_{CE(SUS)}$	UCN-4204A	I_{OUT} = 1.25 A, t_p ≤300 µs, D-Cycle ≤2%	15	—	V
		UCN-4205A	I_{OUT} = 1.25 A, t_p ≤300 µs, D-Cycle ≤2%	35	—	V
Clamp Diode Leakage Current	I_R	UCN-4204A	V_R = 20 V	—	50	µA
		UCN-4205A	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 1.5 A	—	3.0	V
Turn-On Delay	t_{pd0}	All	0.5 E_{IN} (Pin 11) to 0.5 E_{OUT}	—	10	µs
Turn-Off Delay	t_{pd1}	All	0.5 E_{IN} (Pin 11) to 0.5 E_{OUT}	—	10	µs



TIMING CONDITIONS

A. Minimum data set-up time .... 1 µs
B. Minimum data hold time .... 1 µs
C. Minimum data pulse width .... 1 µs
D. Minimum clock period .... 200 µs

UCN-5800A AND UCN-5801A BiMOS II LATCHED DRIVERS

FEATURES

- 2 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

THE UCN-5800A and UCN-5801A latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

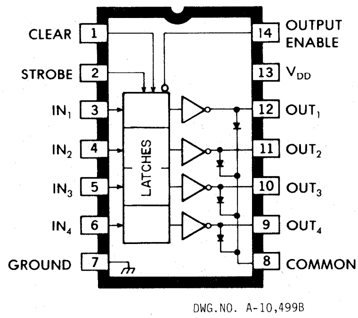
The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. Type UCN-5800A contains four latched drivers; Type UCN-5801A contains eight latched drivers.

BiMOS II devices have much faster data input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

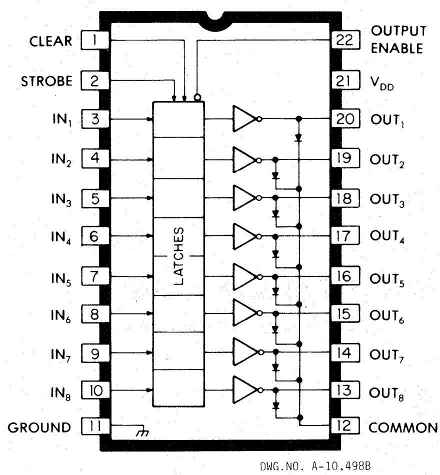
The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

UCN-5800A, the 4-latch device, is furnished in a standard 14-pin dual in-line plastic package. UCN-5801A, the 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400″ (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.



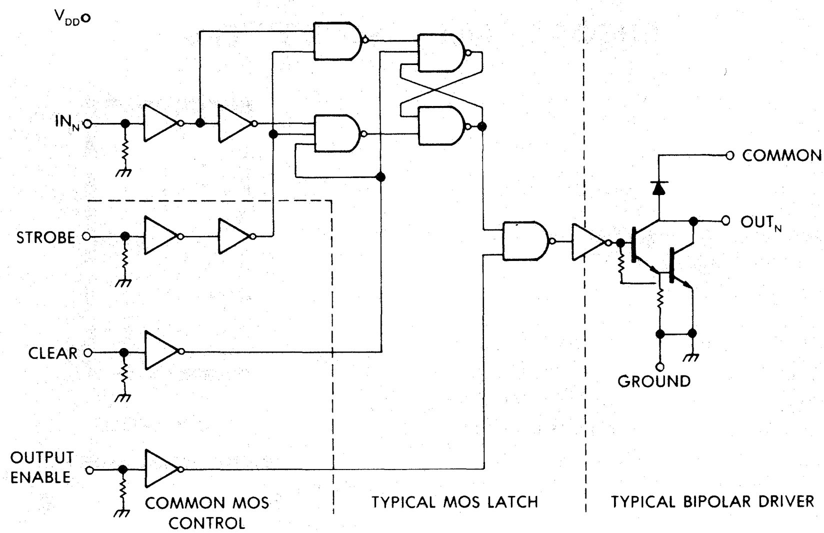
UCN-5800A



UCN-5801A

4

FUNCTIONAL BLOCK DIAGRAM



DWG.NO. A-10,495A

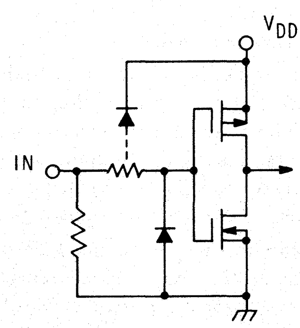
ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . 50 V
Supply Voltage, V_{DD} . . . . 15 V
Input Voltage Range, V_{IN} . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . 500 mA
Package Power Dissipation, P_D
(UCN-5800A) . . . . 1.6 W*
(UCN-5801A) . . . . 2.0 W**
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = +25°C.
**Derate at the rate of 20 mW/°C above T_A = +25°C.

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,520

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted)

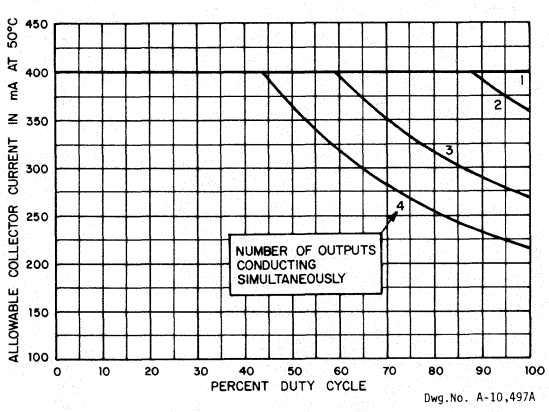
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	—	—	50	μA
		V_{CE} = 50 V, T_A = +70°C	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	—	200	μA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	50	100	μA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C	—	—	50	μA
		V_R = 50 V, T_A = +70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "I".

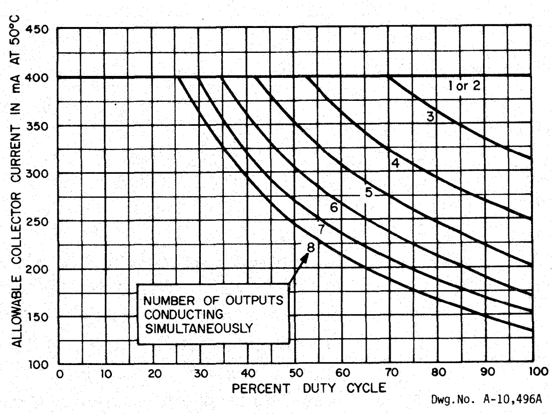
4

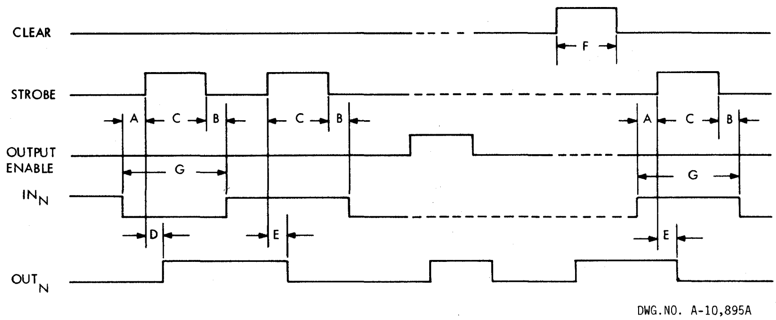
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5800A



UCN-5801A





TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})

A. Minimum data active time before strobe enabled (data set-up time) .... 50 ns
B. Minimum data active time after strobe disabled (data hold time) .... 50 ns
C. Minimum strobe pulse width .... 125 ns
D. Typical time between strobe activation and output on to off transition .... 500 ns
E. Typical time between strobe activation and output off to on transition .... 500 ns
F. Minimum clear pulse width .... 300 ns
G. Minimum data pulse width .... 225 ns

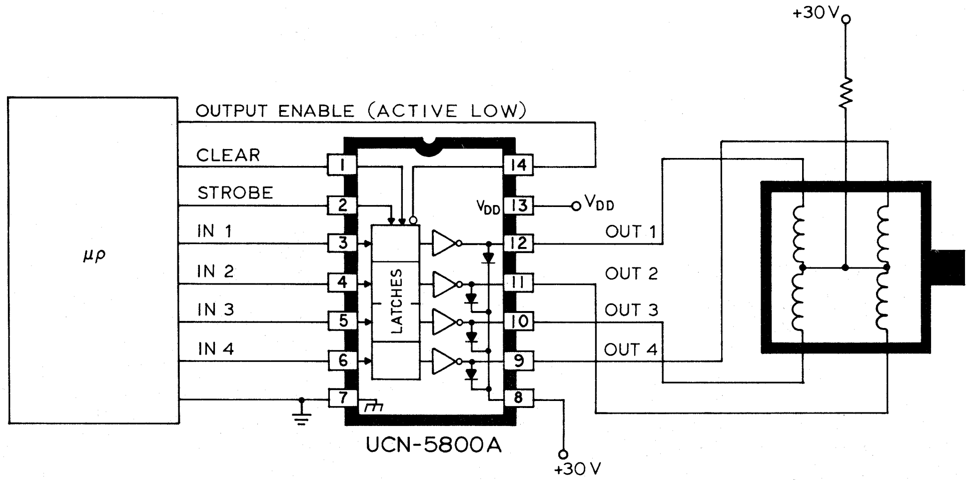
TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



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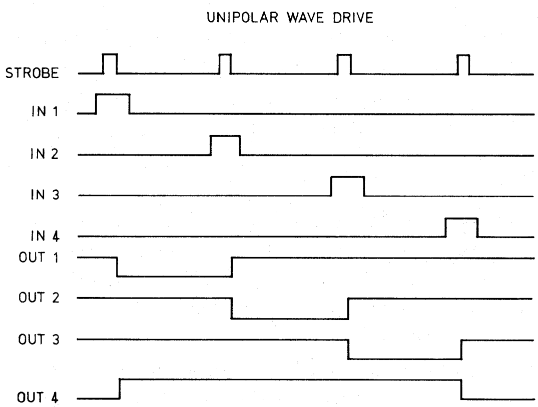
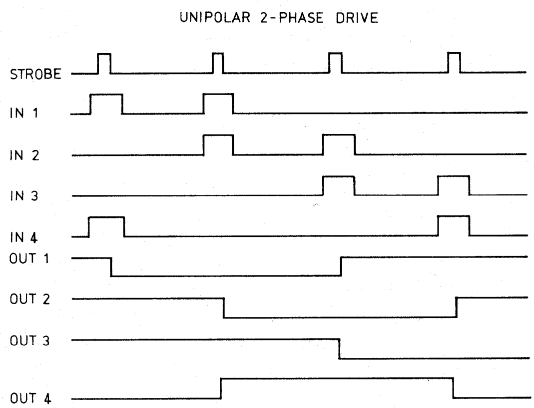


DWG.NO. A-11,446



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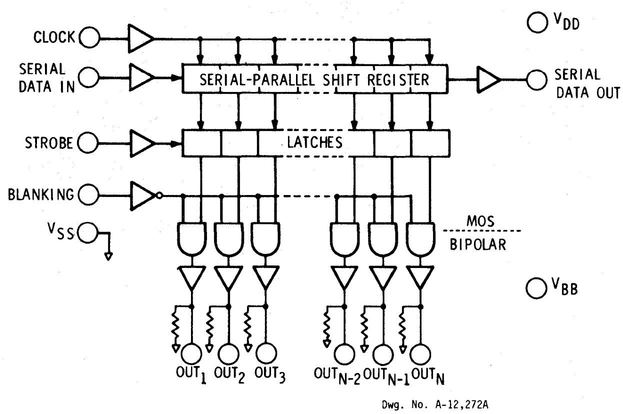
4

UCN-5810A, UCN-5812A, AND UCN-5818A BiMOS II SERIAL-INPUT, LATCHED DRIVERS —10, 20, and 32 Bits

FEATURES

- 5 MHz Minimum Data Input Rate
- Low-Power CMOS Logic and Latches
- 60 V or 80 V Source Outputs
- Internal Pull-Down Resistors



FUNCTIONAL BLOCK DIAGRAM

DESIGNED for use as segment or digit drivers in high-voltage, vacuum-fluorescent display applications, Type UCN-5810A, UCN-5812A, and UCN-5818A combine a CMOS register (10, 20, or 32 bits, respectively), associated latches, and control circuitry (strobe and blanking) with 60 V bipolar source outputs. The BiMOS drivers can also be used with non-multiplexed LED displays within their output limitation of 40 mA per driver.

Selected devices (suffix −1) have maximum ratings of 80 V and 40 mA per driver. In all other respects, the basic part and the part with the "−1" suffix are identical.

BiMOS II devices have much faster input data rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high. A CMOS serial-data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

Type UCN-5810A, a 10-bit driver, is furnished in an 18-pin dual in-line plastic package. It is a high-speed, pin-compatible version of the UCN-4810A driver.

Type UCN-5812A, a 20-bit driver, is furnished in a 28-pin dual in-line plastic package with 0.600″ (15.24 mm) row spacing. Type UCN-5818A, a 32-bit driver, is supplied in a 40-pin dual in-line plastic package with 0.600″ row spacing.

All devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle. The devices are also available with an extended operating temperature range (prefix UCQ-) and ceramic/glass cer-DIP hermetic packages (suffix R).

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

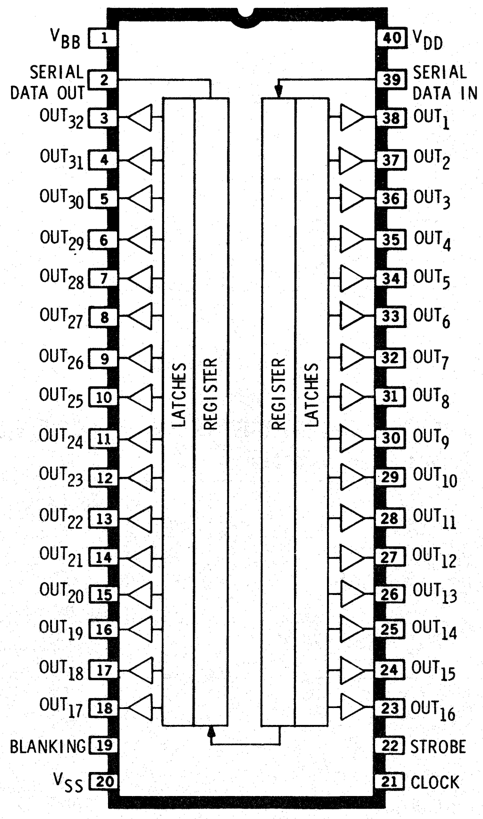
Output Voltage, V_{OUT}	60 V
(Suffix −1)	80 V
Logic Supply Voltage Range, V_{DD}	4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}	5.0 V to 60 V
(Suffix −1)	5.0 V to 80 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT}	−40 mA
Allowable Package Power Dissipation, P_D	
(UCN-5810A)	1.82 W*
(UCN-5812A)	2.5 W*
(UCN-5818A)	2.8 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate linearly to 0 W at T_A = +125°C.

Part Number	Max. Allowable Duty Cycle With All Outputs ON (I_{OUT} = −25 mA) at T_A = +25°C	+40°C	+50°C	+60°C	+70°C
UCN-5810A	100%	97%	85%	73%	62%
UCN-5812A	100%	85%	75%	65%	55%
UCN-5818A	72%	61%	54%	43%	39%

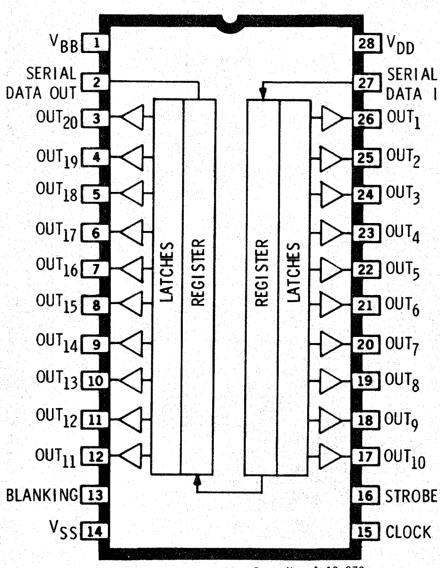
Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5818A



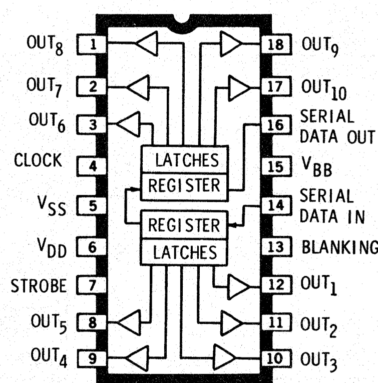
Dwg. No. A-12,269

UCN-5812A



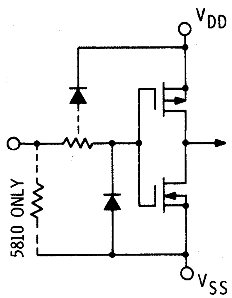
Dwg. No. A-12,270

UCN-5810A



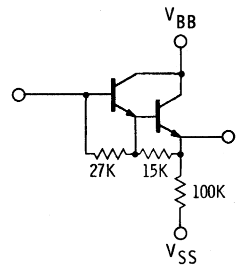
Dwg. No. A-10,988A

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,304

TYPICAL OUTPUT DRIVER

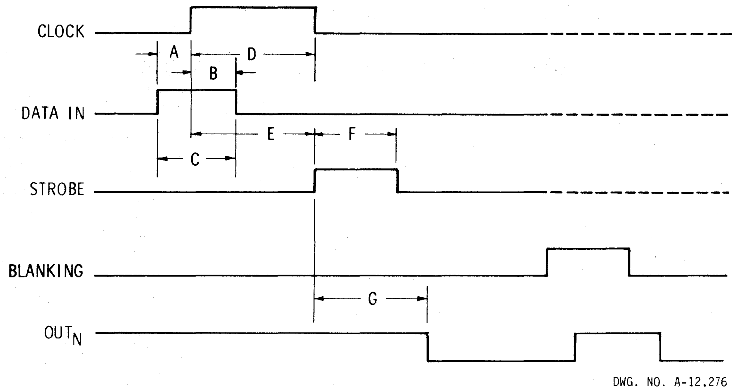


Dwg. No. A-10,981A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}	All		—	1.0	V
Output ON Voltage	V_{OUT}	All	I_{OUT} = −25 mA, V_{BB} = 60 V	57.5	—	V
		Suffix −1	I_{OUT} = −25 mA, V_{BB} = 80 V	77.5	—	V
Output Pull-Down Current	I_{OUT}	All	V_{OUT} = 60 V	400	850	μA
		Suffix −1	V_{OUT} = 80 V	550	1150	μA
Output Leakage Current	I_{OUT}	All	T_A = +70°C	—	−15	μA
Input Voltage	$V_{IN(1)}$	All	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	All	V_{DD} = 5 V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	UCN-5810A	V_{DD} = V_{IN} = 5.0 V	—	100	μA
			V_{DD} = V_{IN} = 12 V	—	240	μA
		UCN-5812/18A	V_{DD} = V_{IN} = 5.0 V	—	0.5	μA
			V_{DD} = V_{IN} = 12 V		1.0	μA
	$I_{IN(0)}$	UCN-5812/18A	V_{DD} = 12 V, V_{IN} = 0.8 V	—	−1.0	μA
Input Impedance	Z_{IN}	All	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	All	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	UCN-5810A	All outputs ON, All outputs open	—	13	mA
		UCN-5812A	All outputs ON, All outputs open	—	22	mA
		UCN-5818A	All outputs ON, All outputs open	—	35	mA
		UCN-5810A	All outputs OFF, All outputs open	—	200	μA
		UCN-5812/18A	All outputs OFF, All outputs open	—	500	μA
	I_{DD}	All	V_{DD} = 5.0 V, All outputs OFF, Inputs = 0 V	—	100	μA
			V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	μA
		UCN-5810A	V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
			V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
		UCN-5812/18A	V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	0.5	mA
			V_{DD} = 12 V, One output ON, All inputs = 0 V	—	1.2	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
*"Suffix −1" indicates UCN-5810A-1, UCN-5812A-1, and UCN5818A-1 only; "UCN-5810A", etc., indicates basic device and same part number with −1 suffix.



TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking Input	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5813B AND UCN-5814B
4-BIT BiMOS LATCH/DRIVERS

FEATURES

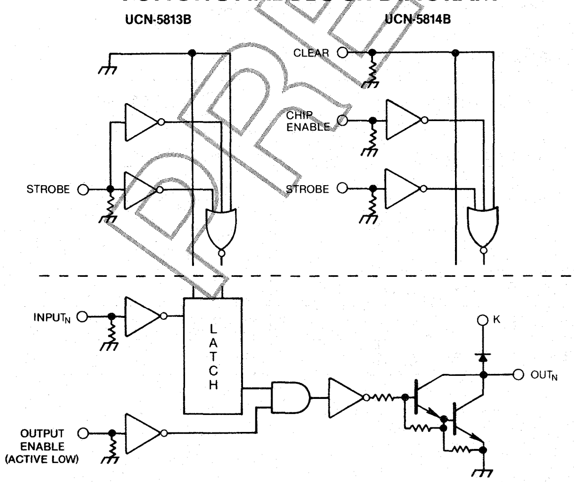
- Low-Current CMOS Input Latches
- Clear, Blanking, Chip Enable and Strobe Functions
- Transient-Protected Outputs
- Handles Loads to 480 Watts
- Plastic Dual In-Line Packages with Heat Sink Contact Tabs

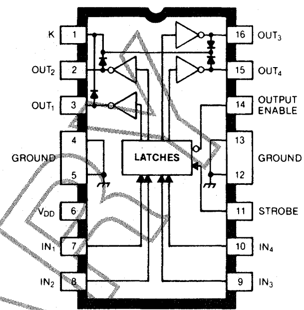
The UCN-5813B and UCN-5814B consist of 4 CMOS latches, 4 open-collector NPN bipolar drivers with output transient suppression diodes, plus common STROBE and OUTPUT ENABLE functions. The UCN-5814B provides the two additional features of CHIP ENABLE and CHIP CLEAR functions for easier µP interface.

Both devices feature CMOS inputs which are compatible with CMOS, PMOS and NMOS logic families. TTL and DTL applications may require pull-up resistors to insure a proper logic "1" level. Outputs are rated at 80 V in the OFF state while each device can sustain 50 V, and 1.0 A when driving inductive loads.

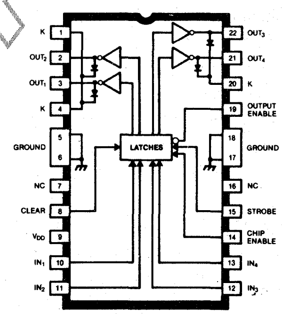
These devices are suitable for applications such as driving relays, solenoids, stepping motors, LED or Incandescent displays, and other high-power loads.

FUNCTIONAL BLOCK DIAGRAM





UCN-5813B



UCN-5814B

The UCN-5813B is furnished in a 16-pin dual in-line plastic package with 0.300 inch row centers while the UCN-5814B device is furnished in a 22-pin batwing package with 0.400 inch row centers. Both packages feature a heat-sinkable tab for improved thermal characteristics and a dual in-line format for easy automatic insertion.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

Output Voltage, V_{CE}	80 V
Output Sustaining Voltage, $V_{CE(SUS)}$	50 V
Output Current, I_{OUT}	1.5 A
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D	2.2 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

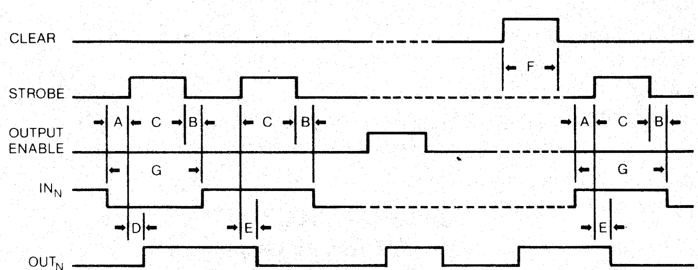
*Derate at the rate of 22.2 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5.0 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 1.0 A	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 1.0 A	—	1.25	V
Clamp Diode Leakage Current	I_R	V_R = 80 V	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	2.0	V
Input Voltage	$V_{IN(0)}$	V_{DD} = 5.0 V	0.3	0.8	V
	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
Input Resistance	R_{IN}	V_{DD} = 5.0 V	100	—	kΩ
		V_{DD} = 12 V	50	—	kΩ
Supply Current	$I_{DD(OFF)}$	V_{DD} = 5.0 V, All Outputs OFF, All Inputs = 0 V	—	100	μA
		V_{DD} = 12 V, All Outputs OFF, All Inputs = 0 V	—	200	μA
	$I_{DD(ON)}$	V_{DD} = 5.0 V, One Output ON, All Inputs = 0 V	—	5.0	mA
		V_{DD} = 12 V, One Output ON, All Inputs = 0 V	—	10	mA

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)



A. Minimum data active time before stroke enabled (data set-up time) .... 50 ns
B. Minimum data active time after strobe disabled (data hold time) .... 50 ns
C. Minimum strobe pulse width .... 125 ns
D. Typical time between strobe activation and output on to off transition .... 500 ns
E. Typical time between strobe activation and output off to on transition .... 500 ns
F. Minimum clear pulse width (UCN-5814B only) .... 300 ns
G. Minimum data pulse width .... 225 ns

TRUTH TABLE

OUTPUT ENABLE	CLEAR	CHIP ENABLE	STROBE	DATA IN	$\overline{OUTPUT}$	NOTES
UCN 5813B						
1			X	X	0	A
0			X	X	n-1	A
0			0	X	n-1	A
0			X	X	0	B
0			1	0	0	B
0			1	1	1	C
UCN 5814B						
1	X	X	X	X	0	A
0	0	0	X	X	n-1	A
0	0	X	0	X	n-1	A
0	1	X	X	X	0	B
0	0	1	1	0	0	B
0	0	1	1	1	1	C

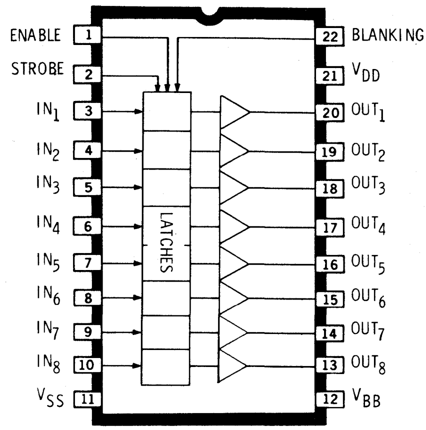
A—does not affect the latch state.
B—resets latch state to 0.
C—sets latch state to 1.
X—irrelevant.
n-1—is previous output state.

Information present at an input is transferred to its latch when the STROBE (UCN-5813B) and STROBE/ENABLE (UCN-5814B) inputs are high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels (UCN-5814 only). A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

UCN-5815A
BiMOS II 8-BIT LATCHED SOURCE DRIVER

FEATURES

- 2 MHz Minimum Data-Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range



Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCN-5815A BiMOSII integrated circuit consists of eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

Selected devices (UCN-5815A-1) have maximum output ratings of 80 V and 40 mA per driver. In all other respects, the UCN-5815A-1 is identical to the 60 V UCN-5815A.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 2 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 12 V. When employed with either standard TTL or low-speed TTL logic, the UCN-5815A may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures up to 60°C. To simplify circuit board layout, output pins are opposite input pins.

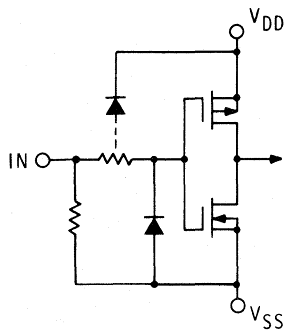
A minimum component display subsystem, requiring few or no discrete components, can be assembled using the UCN-5815A with the UCN-5810A, UCN-5812A or UCN-5818A serial-to-parallel latched driver.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCN-5815A)	60 V
(UCN-5815A-1)	80 V
Logic Supply Voltage Range, V_{DD}	4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}	
(UCN-5815A)	5.0 V to 60 V
(UCN-5815A-1)	5.0 V to 80 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT}	−40 mA
Package Power Dissipation, P_D	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 20 mW/°C above T_A = +25°C.

TYPICAL INPUT CIRCUIT



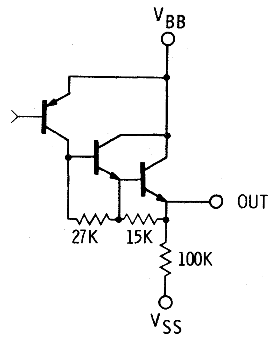
Dwg. No. A-12,517

MAXIMUM DUTY CYCLE

Number of Outputs ON (I_{OUT} = −25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of +50°C	+60°C	+70°C
8	100%	100%	86%
7	100%	100%	98%
6	100%	100%	100%
1	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL OUTPUT DRIVER



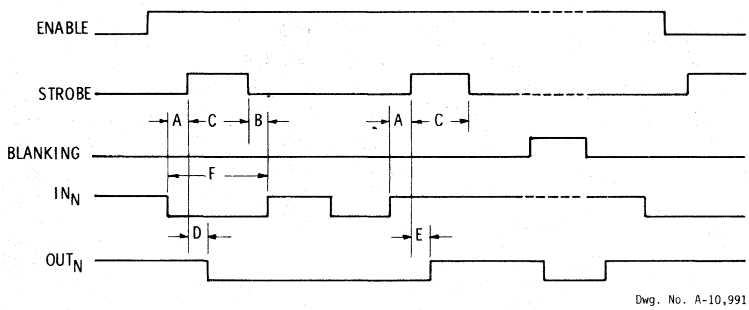
Dwg. No. A-12,546

4

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 4.5 V to 12 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = −25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = −25 mA, V_{BB} = 80 V, UCN-5815A-1 only	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	µA
		V_{BB} = V_{OUT} = 80 V, UCN-5815A-1 only	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = 70°C	—	−15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF, All outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	125 ns
D. Typical Time Between Strobe Activation and Output ON to OFF Transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F. Minimum Data Pulse Width	225 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 2.2 MHz, minimum data input rate (50% duty cycle) with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

UCN-5815A TRUTH TABLE

Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

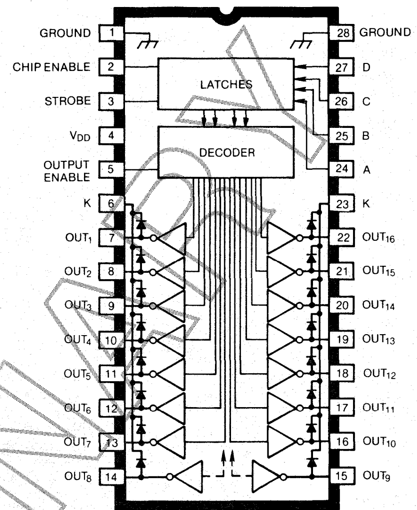
X = irrelevant
T-1 = previous output state
T = present output state

4

UCN-5816A
DECODER/LATCH/SINK DRIVER

FEATURES

- Addressable Data Entry
- 60 V Output Voltage
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Output Transient Protection
- STROBE, CHIP ENABLE, OUTPUT ENABLE* Functions



This sixteen-bit, addressable, latched driver is used in a wide variety of power demultiplexer applications. The UCN-5816A can drive all types of common peripheral power loads, including lamps, relays, solenoids, LED's, printer heads, heaters, and stepper motors. It can also be used as a DMUX driver for higher power loads requiring discrete power semiconductors.

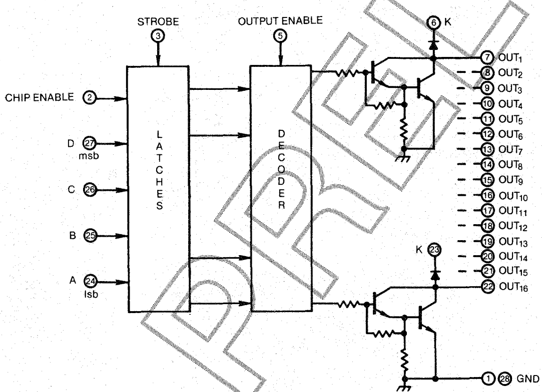
The UCN-5816A is capable of maintaining an output OFF voltage of 60 V and an output ON current of 500 mA.

The logic for this device is all new and is divided into sixteen latches, quadrant select, four 2-line to 4-line decoders, sixteen open-collector output drivers, and MOS control circuitry for CHIP ENABLE, OUTPUT ENABLE*, and STROBE functions. Any of the sixteen power loads can be addressed individually and can be turned ON or OFF independent of the other loads.

This device is supplied in a 28-pin dual in-line plastic package for operation over the temperature range of $-20°C$ to $+85°C$. This device is also available in an industrial-grade ceramic package (UCQ-5816R) or in a side-brazed, hermetically sealed package (UCS-5816H).

*Output Enable—Active Low

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at $T_A = 25°C$

Output Voltage, V_{CE}	60 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage, V_{IN}	-0.3 V to V_{DD} $+0.3$ V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	2.5 W*
Operating Temperature Range, T_A	$-20°C$ to $+85°C$
Storage Temperature Range, T_S	$-55°C$ to $+125°C$

*Derate at the rate of 25 mW/°C above $T_A = 25°C$.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise specified)

Characteristic	Symbol	Applicable Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 60 V, T_A = +25°C	—	—	50	μA
		V_{CE} = 60 V, T_A = +70°C	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 ma	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10.0 V	8.5	—	—	V
		V_{DD} = 5.0 V (See note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.5	3.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.35	2.55	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.05	1.5	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, OE = High	—	50	100	μA
Clamp Diode Leakage Current	I_R	V_R = 60 V, T_A = +25°C	—	—	50	μA
		V_R = 60 V, T_A = +70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "I".

TRUTH TABLE

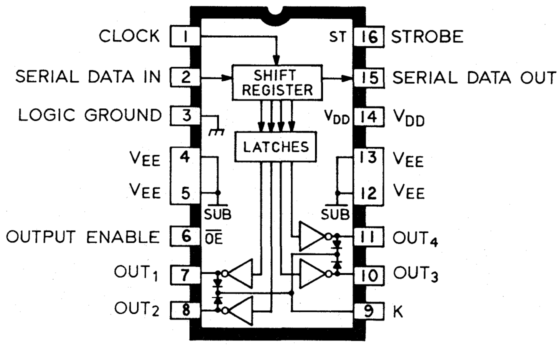
INPUTS																			
STR	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	X	1
OE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
CE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	0
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	X	X	X
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	X	X	X
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	X	X	X
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	X	X	X
OUTPUTS (all outputs OFF unless otherwise specified)																			
1	ON																		
2		ON																	
3			ON																
4				ON															
5					ON														
6						ON													
7							ON										↑	↑	
8								ON									Q_0	ALL	
9									ON									OFF	
10										ON							↓	↓	
11											ON								
12												ON							
13													ON						
14														ON					
15															ON				
16																ON			

NOTE: Q_0 = The Output Conditions before the 1 to 0 transition of the STROBE pin.
1 = High Logic Level 0 = Low Logic Level X = Irrelevant

UCN-5825B AND UCN-5826B BiMOS II HIGH-CURRENT, SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 2 A Open Collector Outputs
- 60 V or 80 V Minimum Output Breakdown
- 35 V or 60 V Sustaining Voltage
- Output-Transient Protection
- Low-Power CMOS Logic and Latches
- Typical Data Input Rate > 5 MHz
- Internal Pull-Down Resistors
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Thermal Shutdown Circuitry



Dwg. No. A-12,557

UCN-5825B and UCN-5826B BiMOS II integrated circuits combine a 4-bit CMOS shift register, associated latches, control circuitry, and level shifting, with bipolar Darlington outputs and transient-suppression diodes for inductive load applications.

The high-current, serial-input, latched drivers can be used with relays, solenoids, stepper motors, LED displays, incandescent displays, and other high-power loads. Control circuitry for both devices includes STROBE and OUTPUT ENABLE functions, and an internal latch that disables outputs at power-up and provides thermal shutdown protection.

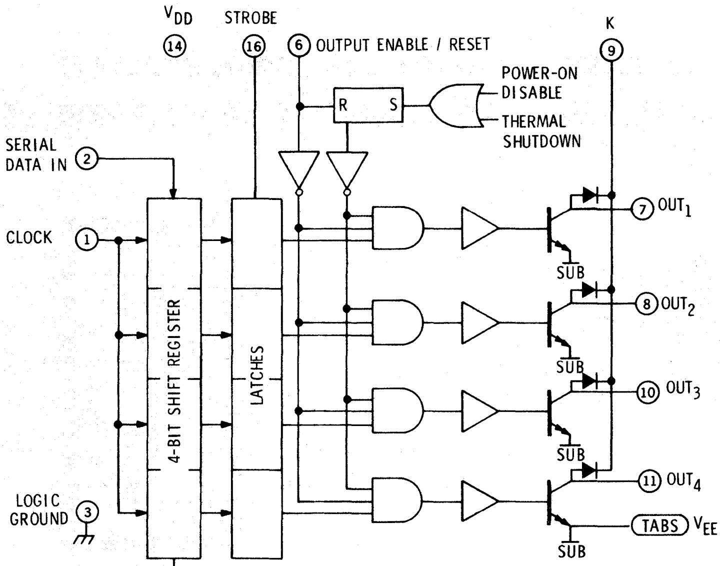
Except for output-voltage ratings, the UCN-5825B and UCN-5826B drivers are identical. The former is rated for operation to 60 V (35 V sustaining); the latter has a minimum output breakdown rating of 80 V (60 V sustaining).

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high level. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. With a 5 V supply, BiMOS II devices typically operate at data-input rates above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Monolithic construction and a 16-pin dual in-line package with copper heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent package power dissipation rating, minimum size, and ease of installation. The package configuration is suitable for automatic insertion, allows easy attachment of an inexpensive heat sink, and fits a standard IC socket or printed wiring board layout.

Both devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,558

ABSOLUTE MAXIMUM RATINGS at + 25°C Free-Air Temperature

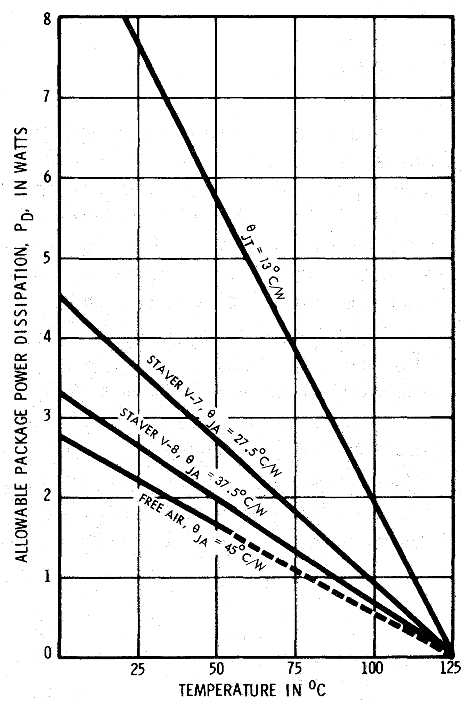
Output Voltage, V_{CE}
(UCN-5825B) .... 60 V
(UCN-5826B) .... 80 V
Output Voltage, $V_{CE(sus)}$
(UCN-5825B) .... 35 V*
(UCN-5826B) .... 60 V*
Logic Supply Voltage Range, V_{DD} .... 4.5 V to 15 V
V_{DD} with reference to V_{EE} .... 25 V
Emitter Supply Voltage, V_{EE} .... −20 V
Input Voltage Range, V_{IN} .... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} .... 2 A
Allowable Package Power Dissipation, P_D .... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +125°C

*For inductive load applications: The sum of the load supply voltage and clamping voltage(s).

Note: Output-current rating may be limited by duty cycle, ambient temperature, heat sinking, and a number of outputs conducting. Under any combination of conditions, do not exceed the specified maximum current rating and a junction temperature of + 125°C.

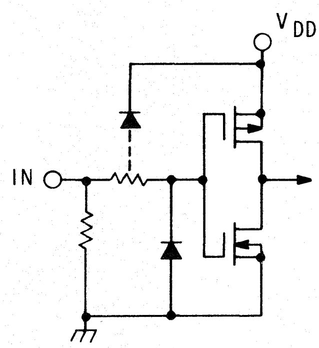
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



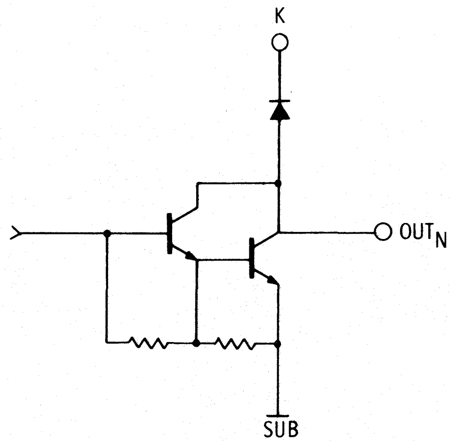
Dwg. No. A-12,560

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,559

TYPICAL OUTPUT DRIVER

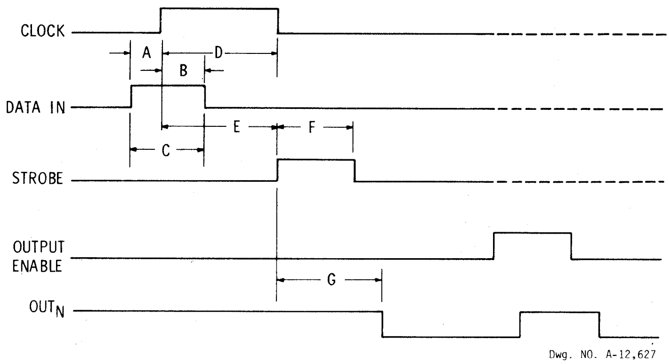


Dwg. No. A-12,561

4

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 60 V, V_{DD} = 5 V to 12 V, V_{EE} = 0 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCN-5825B	T_A = +25°C	—	100	μA
			T_A = +70°C	—	500	μA
		UCN-5826B	V_{CC} = 80 V, T_A = +25°C	—	100	μA
			V_{CC} = 80 V, T_A = +70°C	—	500	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	I_{OUT} = 1.75A	—	1.75	V
Output Sustaining Voltage	$V_{CE(sus)}$	UCN-5825B	I_{OUT} = 1.75 A, L = 2 mH	35	—	V
		UCN-5826B	I_{OUT} = 1.75 A, L = 2 mH	60	—	V
Clamp Diode Leakage Current	I_R	UCN-5825B	V_R = 60 V	—	100	μA
		UCN-5826B	V_R = 80 V	—	100	μA
Clamp Diode Forward Voltage	V_F	Both	I_F = 1.75 A	—	2.0	V
Input Voltage	$V_{IN(1)}$	Both	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	Both	V_{DD} = 5 V to 12 V	−0.3	+0.8	V
Input Resistance	R_{IN}	Both	V_{DD} = 5.0 V	100	—	kΩ
			V_{DD} = 12 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	Both	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{DD}	Both	All outputs OFF	—	3.0	mA
			All outputs ON	—	20	mA
Maximum Clock Frequency	f_C	Both		3.3	—	MHz
Turn-ON Delay	t_{PLH}	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-OFF Delay	t_{PHL}	Both	0.5 E_{in} to 0.5 E_{out}	—	2.0	μs
Propagation Delay	t_{PD}	Both	0.5 E_{clock} to 0.5 E_{out}	—	100	ns



TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of the latches.

Two additional functions serve to protect the system and the device. Either power-up or overheating will set an internal latch that disables the outputs. With the latch set, data can be shifted and latched while the outputs are disabled. To resume normal operation, the latch must be reset by toggling OUTPUT ENABLE a minimum of 500 ns.

TRUTH TABLE

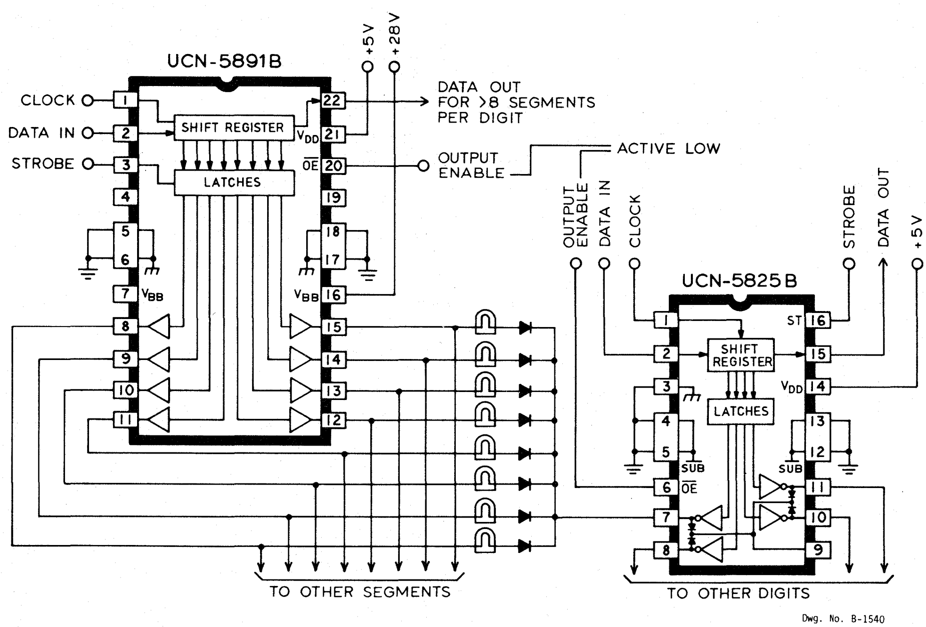
Serial Data Input	Clock Input	Shift Register Contents				Serial Data Output	Strobe Input	Latch Contents				Output Enable	Output Contents			
		I_1	I_2	I_3	I_4			I_1	I_2	I_3	I_4		I_1	I_2	I_3	I_4
H	↑	H	R_1	R_2	R_3	R_3										
L	↑	L	R_1	R_2	R_3	R_3										
X	↓	R_1	R_2	R_3	R_4	R_4										
		X	X	X	X	X	L	R_1	R_2	R_3	R_4					
		P_1	P_2	P_3	P_4	P_4	H	P_1	P_2	P_3	P_4	L	P_1	P_2	P_3	P_4
								X	X	X	X	H	H	H	H	H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

4

TYPICAL APPLICATION

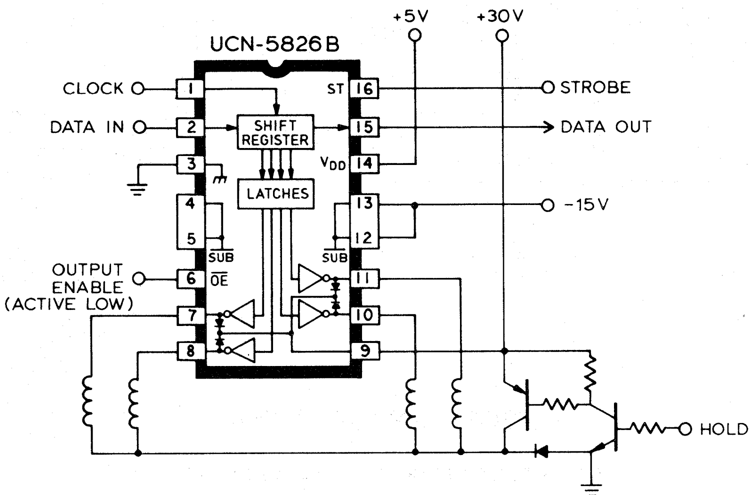
MULTIPLEXED INCANDESCENT LAMP DRIVE



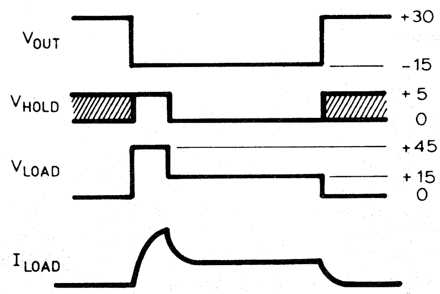
*Active Low

TYPICAL APPLICATION

HAMMER DRIVE



*Active Low



Dwg. No. B-154.

UCN-5832A AND UCN-5832C
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

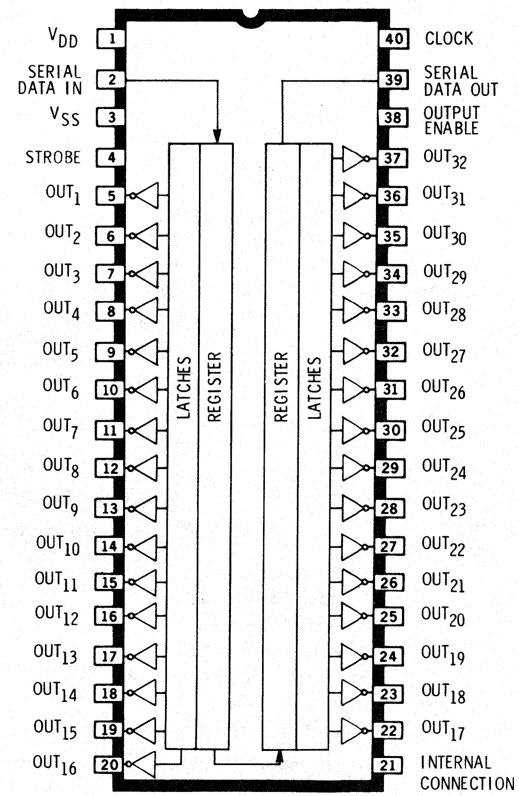
FEATURES

- 5 MHz Minimum Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current-Sink Outputs
- Low Saturation Voltage

INTENDED PRIMARILY to drive thermal printheads, Types UCN-5832A and UCN-5832C have been optimized for low output-saturation voltage, high-speed operation, and pin/pad configurations most convenient for the tight space requirements of high-resolution printheads. The integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. A combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

Type UCN-5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, all outputs of the packaged device will sustain 100 mA continuously over the operating temperature range without derating. Type UCN-5832C is an unpackaged, passivated, bare-back device in chip form. In this version, the shift register is divided into two 16-bit blocks for maximum flexibility. For either device, MOS serial outputs permit cascading for interface applications requiring additional drive lines.

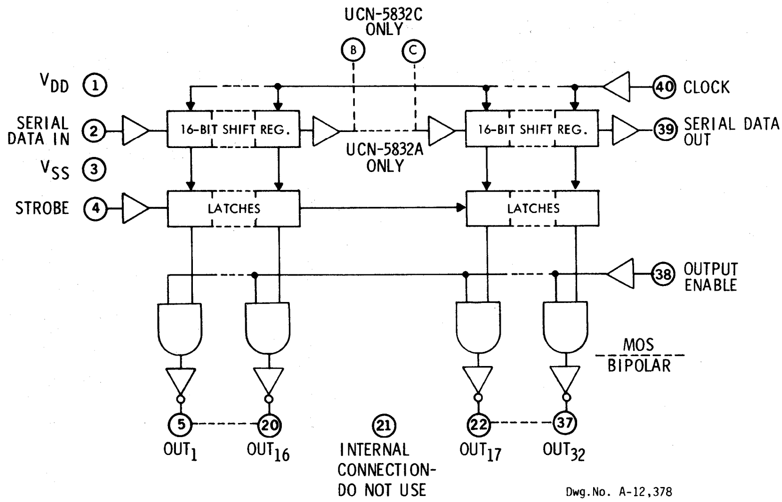


Dwg.No. A-12,377

A similar 32-bit serial-input latched source driver is available as UCN-5818A. High-voltage, high-current 8-bit devices are available in Series UCN-4820A.

4

FUNCTIONAL BLOCK DIAGRAM



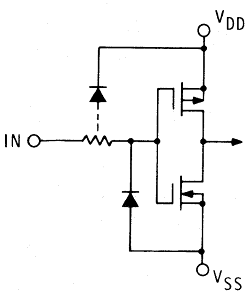
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT}	40 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT}	150 mA
Package Power Dissipation, P_D (UCN-5832A)	2.8 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 28 mW/°C above T_A = +25°C

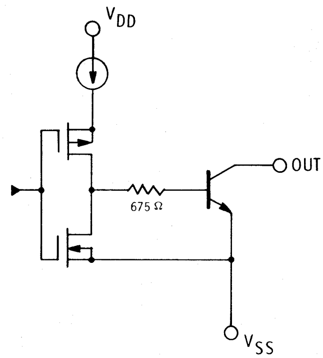
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,379

TYPICAL OUTPUT DRIVER



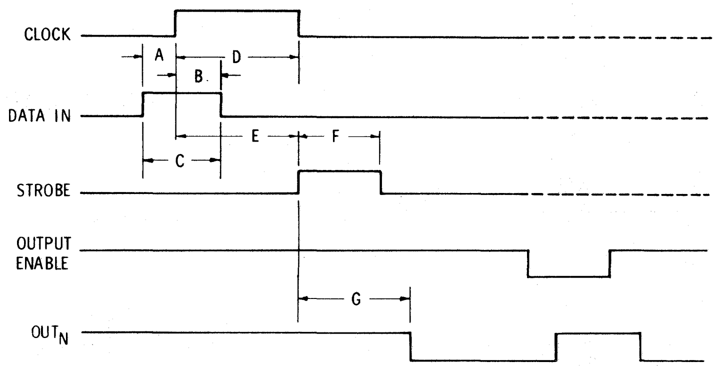
Dwg.No. A-12-380

4

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 40 V, T_A = 70°C	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	275	mV
		I_{OUT} = 100 mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 3.5 V	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−1.0	µA
Input Impedance	Z_{IN}	V_{IN} = 3.5 V	3.5	—	MΩ
Serial Data/Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	2.0	µs
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	2.0	µs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



DWG. NO. A-12,276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

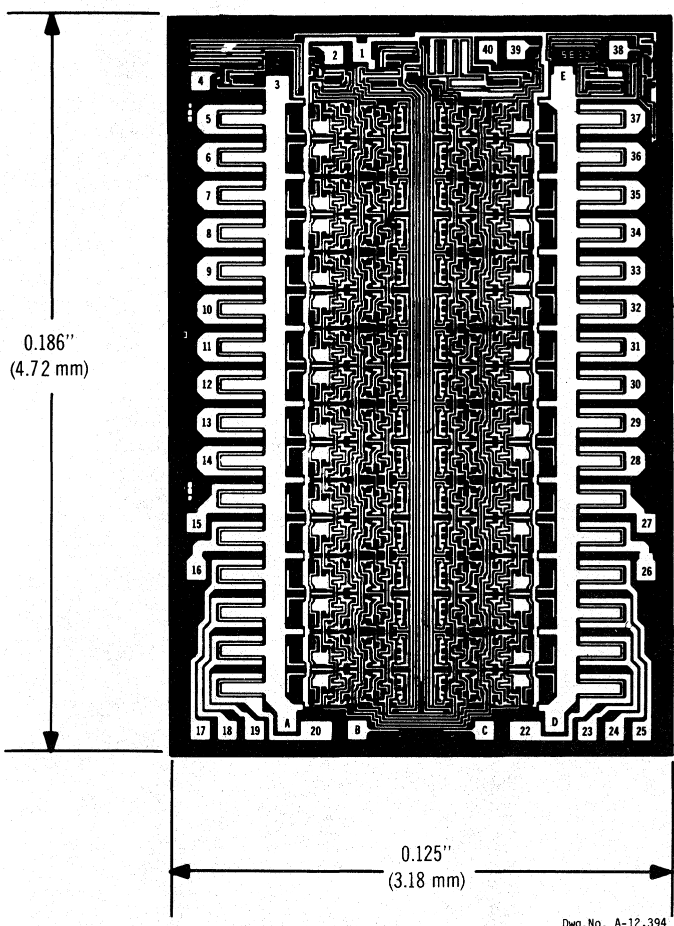
When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	L	H H H ... H H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5832C



UCN-5832 chips are of silicon planar epitaxial construction. They are identical to those used for packaged devices. When assembled correctly, they should lead to a high final test yield. All chips are visually inspected for masking, diffusion, and scribing defects. Conformance to electrical parameters can be guaranteed (at additional charge) by performing measurements on packaged units assembled from a random sample taken from the lot.

The preferred method of sale for unpackaged die is in wafer form. These are identified as UCN-5832C*W* and are supplied in 4" (100 mm) wafers that have been tested (probed) in wafer form. Electrically defective devices are identified by ink dots during this operation. Wafers do not include visual die inspection. Orders for UCN-5832C*W* will be accepted only for complete wafers.

Because Sprague Electric Company does not control the customer packaging of UCN-5832C chips or UCN-5832C*W* wafers, Sprague Electric company assumes no liability for final electrical and reliability parameters.

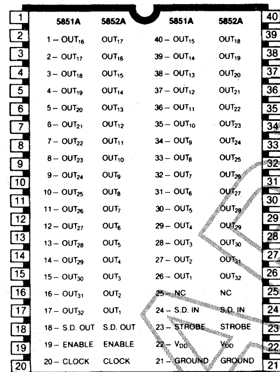
	PAD DESIGNATIONS	
PAD	UCN-5832A	UCN-5832C
1	V_{DD}	V_{DD}
2	SERIAL DATA IN	SERIAL DATA IN_1
3	V_{SS}	V_{SS}*
4	STROBE	STROBE
5	OUT_1	OUT_1
6	OUT_2	OUT_2
7	OUT_3	OUT_3
8	OUT_4	OUT_4
9	OUT_5	OUT_5
10	OUT_6	OUT_6
11	OUT_7	OUT_7
12	OUT_8	OUT_8
13	OUT_9	OUT_9
14	OUT_{10}	OUT_{10}
15	OUT_{11}	OUT_{11}
16	OUT_{12}	OUT_{12}
17	OUT_{13}	OUT_{13}
18	OUT_{14}	OUT_{14}
19	OUT_{15}	OUT_{15}
A	—	V_{SS}*
20	OUT_{16}	OUT_{16}
B	—	SERIAL DATA OUT_{16}
21	INTERNAL CONNECTION—DO NOT USE	—
C	—	SERIAL DATA IN_{17}
22	OUT_{17}	OUT_{17}
D	—	V_{SS}*
23	OUT_{18}	OUT_{18}
24	OUT_{19}	OUT_{19}
25	OUT_{20}	OUT_{20}
26	OUT_{21}	OUT_{21}
27	OUT_{22}	OUT_{22}
28	OUT_{23}	OUT_{23}
29	OUT_{24}	OUT_{24}
30	OUT_{25}	OUT_{25}
31	OUT_{26}	OUT_{26}
32	OUT_{27}	OUT_{27}
33	OUT_{28}	OUT_{28}
34	OUT_{29}	OUT_{29}
35	OUT_{30}	OUT_{30}
36	OUT_{31}	OUT_{31}
37	OUT_{32}	OUT_{32}
38	OUTPUT ENABLE	OUTPUT ENABLE
E	—	V_{SS}*
39	SERIAL DATA OUT	SERIAL DATA OUT_{32}
40	CLOCK	CLOCK

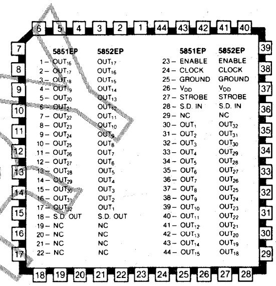
*Bonding pads *A* or *3* and *D* or *E* must be connected to the substrate. For maximum output current capability, pads *A, D, E,* and *3* must all be bonded to the substrate.

UCN-5851A/EP AND UCN-5852A/EP 32-BIT TFEL SHIFT REGISTER DRIVERS

FEATURES

- 32 Sink Outputs
- Output Voltage of 225 V
- Output Current of 80 mA
- Low-Power CMOS Logic
- 5 MHz Data Input Rate
- STROBE, OUTPUT ENABLE Functions
- Direct Replacement for SN75551/52



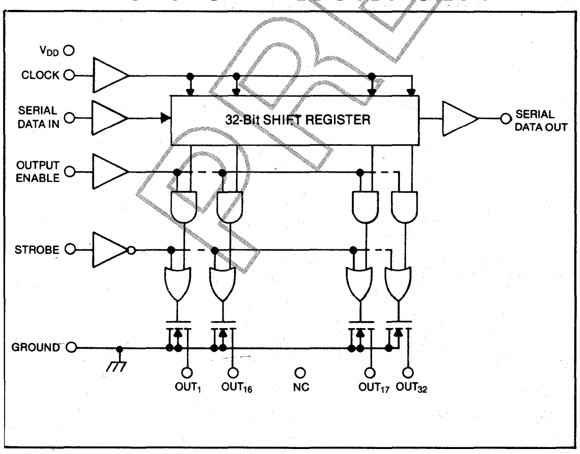


4

The UCN-5851A/EP and UCN-5852A/EP are 32-channel TFEL (Thin Film Electroluminescent Display) Row Electrode drivers. These devices are capable of maintaining an output OFF voltage of 225 V and an ON current of 80 mA. The UCN-5851 A/EP and UCN-5852A/EP are identical except for pinning designations. These devices have reverse output pin designations (UCN-5851A/EP pin 1 = OUT_{16}, pin 26 = OUT_1. UCN-5852A/EP pin 1 = OUT_{17}, pin 26 = OUT_{32}).

The input logic structure consists of BiMOS II logic circuitry for low-power consumption, high speed versatility, and interface flexibility. Standard TTL may require the use of a pull-up resistor to ensure a logical high.

FUNCTIONAL BLOCK DIAGRAM



Serial data is entered into the register on the high-to-low transition of the CLOCK input. A high input turns ON the corresponding output. When OUTPUT ENABLE is high data present in the register is transferred to the outputs. When OUTPUT ENABLE is low all outputs are turned OFF. When the STROBE pin is held high data in the register is transferred to the latches. When the STROBE pin is held low the outputs are turned ON.

The SERIAL DATA output may be used to cascade additional devices. This output is not affected by the OUTPUT ENABLE or STROBE functions.

The UCN-5851A and UCN-5852A are packaged in a 40-pin dual in-line plastic package with 0.600″ (15.24 mm) row spacing. The UCN-5851EP and UCN-5852EP are packaged in 44 pin plastic leaded chip carriers with 0.050″ (1.27 mm) pin spacings (J lead bend) for surface mount applications.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{CE} . . . . 225 V
Logic Supply Voltage, V_{DD} . . . . 15 V
Logic Input Voltage, V_{IN} . . . . −0.3 V to V_{DD} +0.3 V
Output Current, I_{OUT} . . . . 80 mA
Package Power Dissipation, P_D (A Package) . . . . 2.8 W*
(EP Package) . . . . 1.2 W
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +125°C

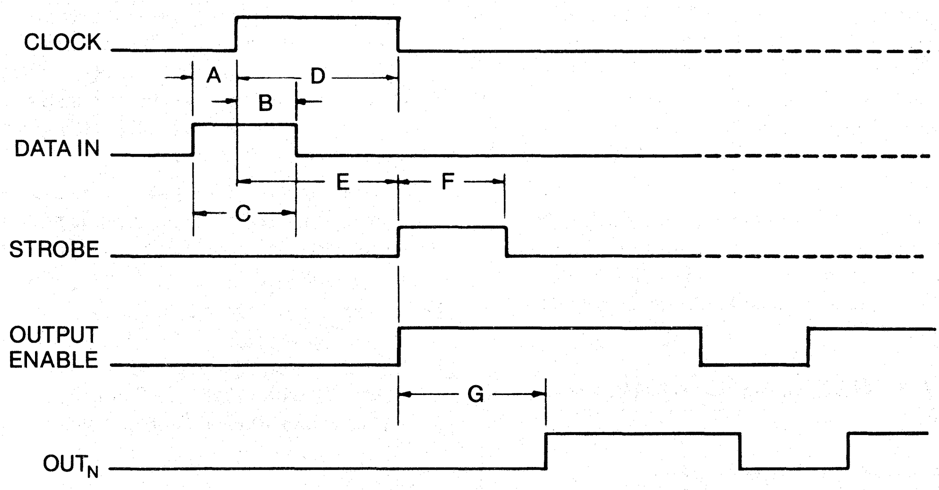
*Derate at the rate of 28 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{DSK}	$V_{OUT} = 200$ V	—	10	μA
Output Clamp Current		$V_{OUT} = -2$ V	80	—	mA
Output Sink Current	I_{OUT}		50	—	mA
		$V_{DD} = 12$ V	80	—	mA
Low Level Output Voltage	$V_{DS(ON)}$	$I_{OUT} = 30$ mA	10.0	—	V
		$V_{DD} = 12$ V, $I_{OUT} = 80$ mA	5.0	—	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
		$V_{DD} = 12$ V	10.5	12.3	V
Input Current	$I_{IN(1)}$		—	0.5	μA
		$V_{DD} = 12$ V	—	1.0	μA
	$I_{IN(0)}$	$V_{DD} = 12$ V, $V_{IN} = 0.8$ V	—	−1.0	μA
Supply Current	I_{DD}	All Drivers Off	—	500	μA

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

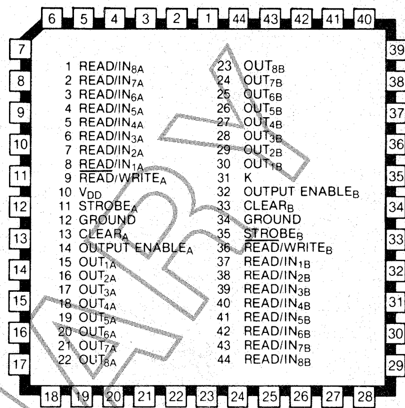


	$V_{DD} = 5.0$ V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	150 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

UCN-5881EP
BiMOS LATCHED DRIVER WITH READ BACK

FEATURES

- READ/WRITE Inputs
- STROBE, CLEAR, OUTPUT ENABLE Functions
- Low Power CMOS Logic
- 50 mA capabilities
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low Profile Leadless Chip Carrier



The UCN-5881EP is comprised of 16 CMOS data latches (2 sets of 8), a bipolar non-darlington Driver for each latch, and CMOS control circuitry for 2 sets of Common CLEAR, STROBE, and OUTPUT ENABLE functions. The Bipolar/MOS combination provides for an extremely low-power latch with maximum interface flexibility. The UCN-5881EP also incorporates thermal shutdown to protect against thermal damage. The UCN-5881EP also has READ back capabilities.

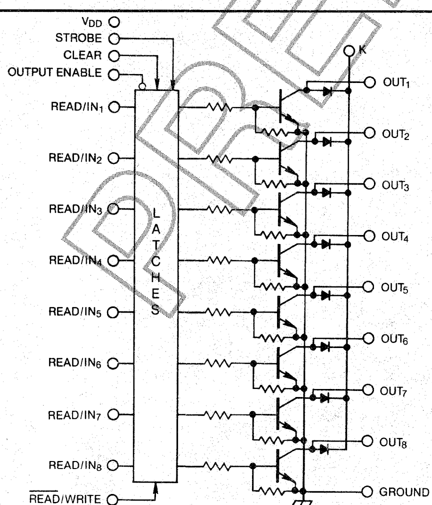
The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull up resistors. The bipolar outputs are suitable for use with low power relays, solenoids, stepping motors, and LED's.

A high on the READ/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

A low on the READ/WRITE input will allow the latched data to be "read back" on the data input lines. This READ feature is for error checking applications. When "reading back" the data inputs will be capable of sinking 8 mA if its corresponding latch is low or sourcing 400 μA if its corresponding latch is high.

This device features integral diodes for inductive load transient suppression. The output transistors are capable of sinking 50 mA and will maintain at least 20 V in the OFF state. Outputs may be paralleled for higher current capability.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at $T_A = 25°C$

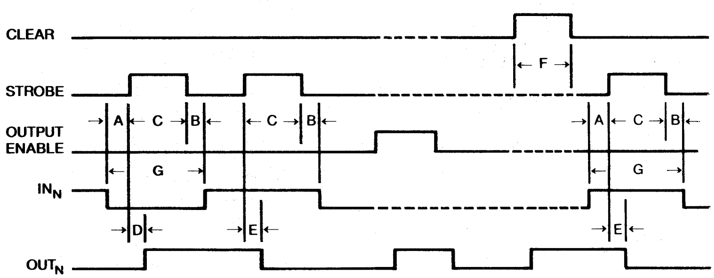
Output Voltage, V_{OUT}	20 V
Output Current, I_{OUT}	50 mA
Input Voltage, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Logic Supply Voltage, V_{DD}	15 V
Package Power Dissipation, P_D	1.2 W
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature, T_S	−55°C to +125°C
Junction Temperature, T_J	+125°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 20 V	—	50	μA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 10 mA	—	0.1	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$		2.7	—	V
Logic Supply Current	$I_{DD(ON)}$	One Driver ON	—	1.0	mA
	$I_{DD(OFF)}$	All Drivers OFF	—	100	μA
Input Current	$I_{IN(1)}$	V_{IN} = 5 V	—	10	μA
Clamp Diode Leakage Current	I_R	V_R = 20 V	—	50	μA
Clamp Diode Forward Voltage	V_F	I_F = 50 mA	—	0.5	V
High Level Readback Current	I_{RBH}	V_{IN} = 2.7 V	—	−400	μA
Low Level Readback Current	I_{RBL}	V_{IN} = 0.8 V	—	8.0	mA

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)



A. Minimum data active time before strobe enabled (data set-up time) .... 50 ns
B. Minimum data active time after strobe disabled (data hold time) .... 50 ns
C. Minimum strobe pulse width .... 150 ns
D. Typical time between strobe activation and output on to off transition .... 500 ns
E. Typical time between strobe activation and output off to on transition .... 500 ns
F. Minimum clear pulse width .... 225 ns
G. Minimum data pulse width .... 125 ns

TRUTH TABLE

IN/READ	STROBE	CLEAR	OUTPUT ENABLE	$\overline{READ}$/WRITE	OUTPUT	LATCH CONTENTS
X	X	X	1	X	X	0
0	1	0	0	1	0	0
1	1	0	0	1	1	1
X	0	0	0	1	n-1	n-1
X	0	1	0	1	0	0
n	X	0	X	0	n	X

NOTES:

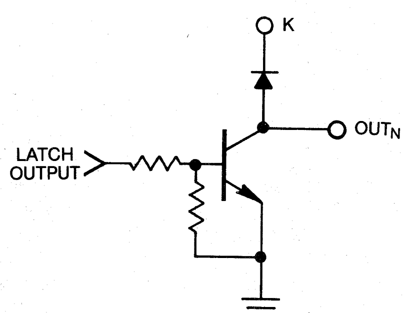
A. If $\overline{READ}$/WRITE is low strobe is internally disabled.

B. CLEAR is not gated.
1. Do not raise STROBE high while CLEAR is high.
2. Do not attempt to CLEAR while Reading latch contents.

C. OUTPUT 1 refers to Driver "ON" condition not to high voltage at output ie. Sink "1" = Low V.

n = Present Latch Contents
n-1 = Previous Latch Contents

SINK DRIVER



UCN-5890A/B AND UCN-5891A/B BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

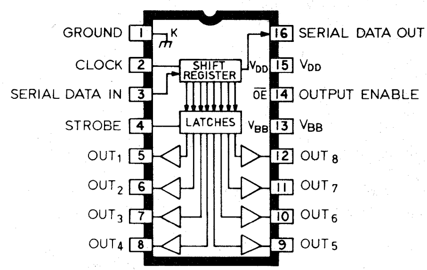
- 50 V or 80 V Source Outputs
- Output Current to − 500 mA
- Output Transient-Suppression Diodes
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic and Latches

PRIMARILY DESIGNED for use with thermal or electromagnetic printers, the UCN-5890A/B and UCN-5891A/B BiMOS II serial-input, latched drivers combine an 8-bit CMOS register, associated latches, and control circuitry (strobe and output enable) with Darlington sourcing outputs. They may also be used with relays or multiplexed LED displays within their output limitation of − 500 mA per driver.

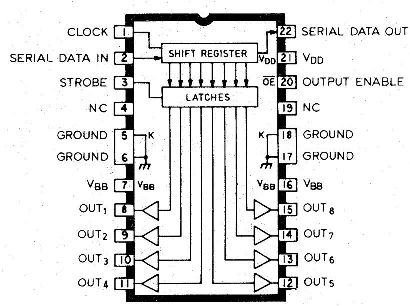
Suffix "A" devices are supplied in a standard 16-pin dual in-line plastic package. Complementary, 8-bit serial-input latched sink drivers are in Series UCN-5820A, described in Engineering Bulletin 26185.12. Suffix "B" devices are furnished in a 22-pin dual in-line package with heat-sink contact tabs that allows increased package power dissipation.

Electrical ratings for the four devices are identical except for allowable load voltage ratings. UCN-5890A and UCN-5890B are rated for operation with supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. For applications using supply voltages of 20 V to 50 V (35 V sustaining), lower-cost UCN-5890A-2 and UCN-5890B-2 are recommended. The UCN-5891A and UCN-5891B are optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining). A similar driver (featuring reduced output-saturation voltage), the UCN-5895A, is described in Engineering Bulletin 26182.14.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained.



UCN-5890A
UCN-5891A



UCN-5890B
UCN-5891B

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

All devices are rated for continuous operation over the temperature range of − 20°C to + 85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

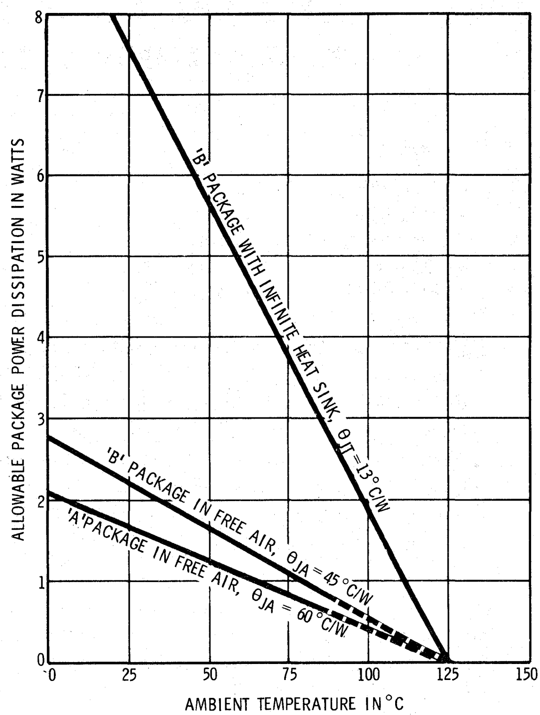
Output Voltage, V_{OUT} (UCN-5890A/B) . . . . 80 V
(UCN-5890A/B-2) . . . . 50 V
(UCN-5891A/B) . . . . 50 V
Logic Supply Voltage Range, V_{DD} . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}
(UCN-5890A/B) . . . . 20 V to 80 V
(UCN-5890A/B-2) . . . . 20 V to 50 V
(UCN-5891A/B) . . . . 5.0 to 50 V
Input Voltage Range, V_{IN} . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . −500 mA
Allowable Package Power Dissipation, P_D . . . . See Graph
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +125°C

Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Number of Outputs ON at I_{OUT} = −200 mA	Max. Allowable Duty Cycle at T_A of					
	50°C	60°C	70°C	50°C	60°C	70°C
	Package "A"			Package "B"		
8	40%	34%	28%	53%	46%	39%
7	45%	39%	33%	60%	52%	44%
6	53%	46%	39%	70%	61%	51%
5	63%	55%	46%	84%	73%	62%
4	79%	68%	58%	100%	91%	77%
3	100%	91%	77%	100%	100%	100%
2	100%	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%	100%

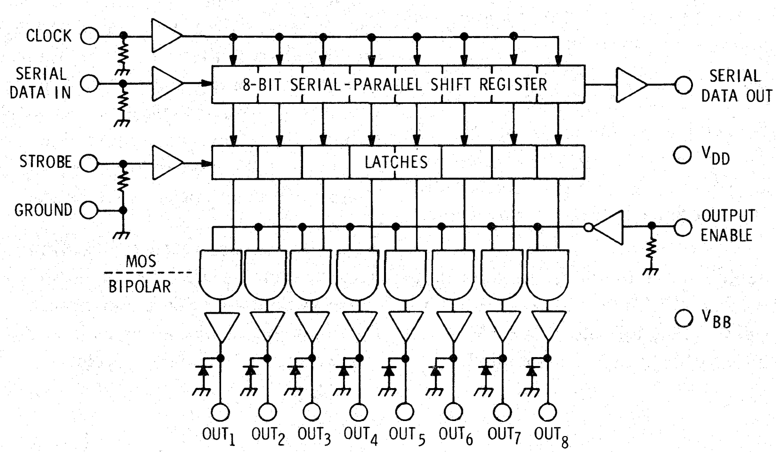
Also see Allowable Output Current graphs

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-12,645

FUNCTIONAL BLOCK DIAGRAM



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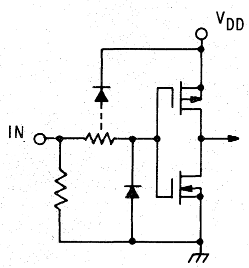
TYPICAL INPUT CIRCUIT



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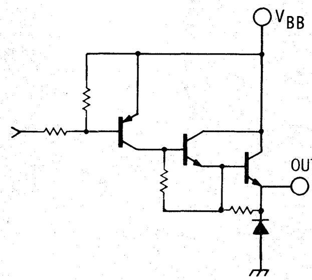
TYPICAL OUTPUT DRIVER



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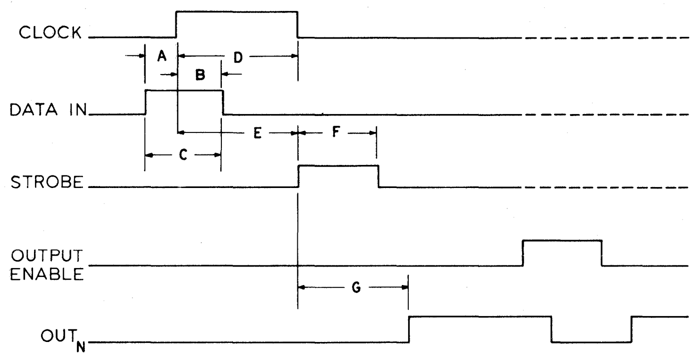
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 80 V (UCN-5890A/B) or 50 V (UCN-5890A/B-2 & UCN-5891A/B), V_{DD} = 5 V to 12 V (unless otherwise noted)

Characteristic	Symbol	V_{BB}	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	Max.	T_A = +25°C	—	−50	µA
			T_A = +70°C	—	−100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	I_{OUT} = −100 mA	—	1.8	V
			I_{OUT} = −225 mA	—	1.9	V
			I_{OUT} = −350 mA	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	I_{OUT} = −350 mA, L = 2 mH, UCN-5890A/B-2 & UCN-5891A/B	35	—	V
			I_{OUT} = −350 mA, L = 2 mH, UCN-5890A & UCN-5890B only	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	50 V	V_{DD} = 5 V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	V_{DD} = V_{IN} = 5.0 V	—	50	µA
			V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	50 V	V_{DD} = 5.0 V	100	—	kΩ
			V_{DD} = 12 V	50	—	kΩ
Clock Frequency	f_c	50 V		3.3	—	MHz
Serial Data Output Resistance	R_{OUT}	50 V	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	50 V	Output Enable to Output, I_{OUT} = −350 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	50 V	Output Enable to Output, I_{OUT} = −350 mA	—	10	µs
Supply Current	I_{BB}	50 V	All outputs ON, All outputs open	—	10	mA
			All outputs OFF	—	200	µA
	I_{DD}	50 V	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
			V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
			V_{DD} = 5 V, One output ON, All inputs = 0 V	—	1.0	mA
			V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	Max.	T_A = +25°C	—	50	µA
			T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	Open	I_F = 350 mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



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TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... 75 ns
C. Minimum Data Pulse Width .... 150 ns
D. Minimum Clock Pulse Width .... 150 ns
E. Minimum Time Between Clock Activation and Strobe .... 300 ns
F. Minimum Strobe Pulse Width .... 100 ns
G. Typical Time Between Strobe Activation and Output Transition .... 1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

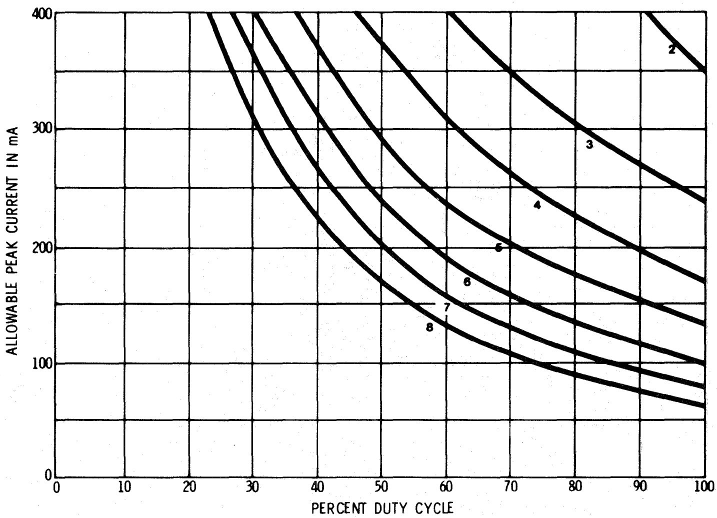
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Output Enable	Output Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE at +25°C Free-Air Temperature

UCN-5°°0A AND UCN-5891A



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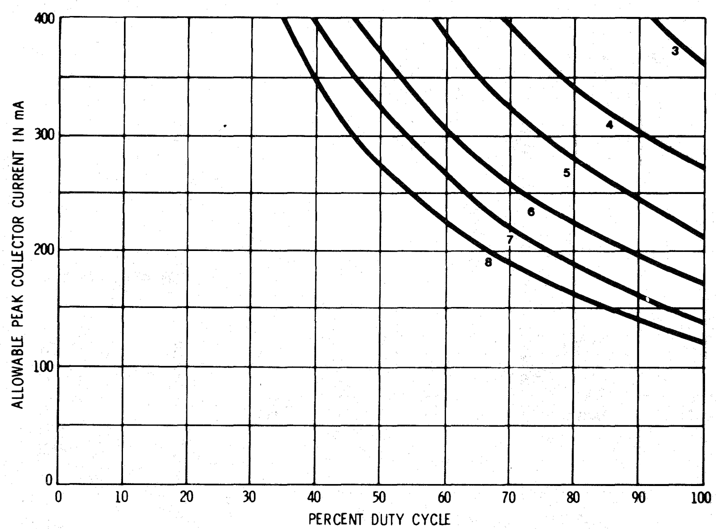
UCN-5890B AND UCN-5891B



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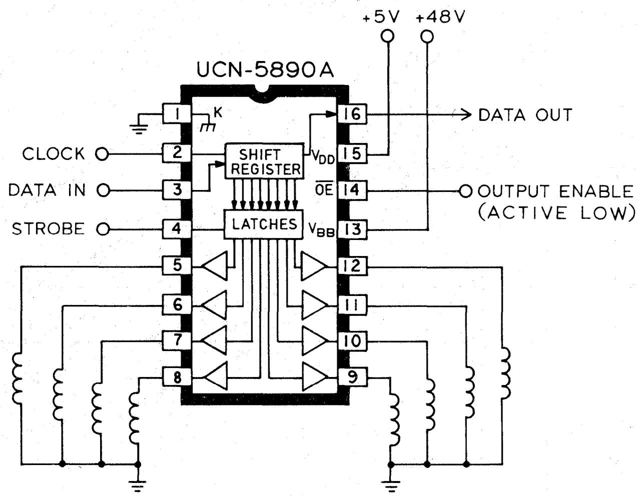
TYPICAL APPLICATIONS

SOLENOID OR RELAY DRIVER



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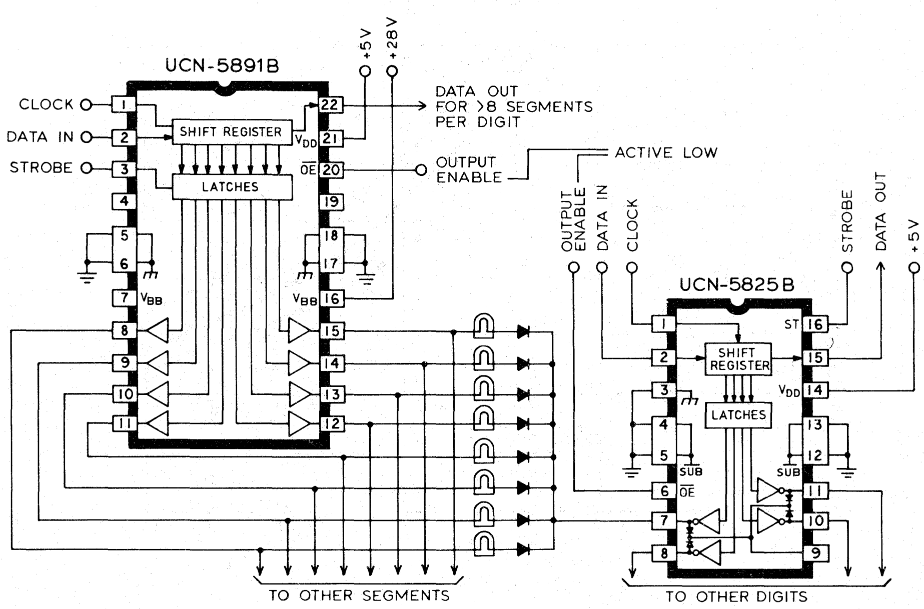
MULTIPLEXED INCANDESCENT LAMP DRIVER



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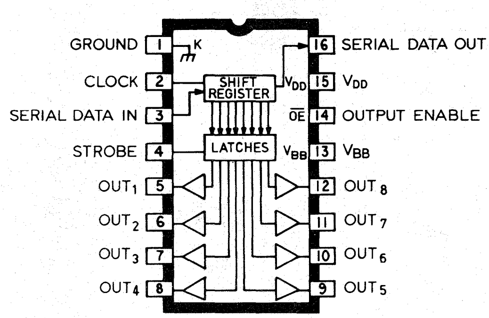
UCN-5895A AND UCN-5895A-2 BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

- Low Output-Saturation Voltage
- Source Outputs to 50 V
- Output Current to − 250 mA
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic & Latches



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UCN-5895A AND UCN-5895A-2 BiMOS II serial-input, latched source drivers are designed for use in applications requiring low output-saturation voltages and currents to − 250 mA per driver. Each driver combines an 8-bit CMOS register, associated latches and control circuitry (strobe and output enable), with saturated bipolar emitter-follower outputs. Typical loads are low-voltage LEDs and incandescent displays. They can also be used with multiplexed LED displays, thermal printers, or electromagnetic printers within their output limitations.

The UCN-5895A is rated for operation with supply voltages to 50 V and features a minimum output sustaining voltage of 35 V. The more economical UCN-5895A-2 is for use with supply voltages to 25 V (15 V sustaining). Under normal operation conditions, at + 25°C, all outputs will source − 120 mA continuously without derating. Similar drivers, featuring Darlington outputs for increased output ratings, are the UCN-5890A/B and UCN-5891A/B, described in Engineering Bulletin 26182.12.

BiMOS II devices can operate at greatly improved data-input rates. With a 5 V supply, they will typically operate at better than 5 MHz. At 12 V, significantly higher speeds are obtained.

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

These devices are rated for continuous operation over the temperature range of − 20°C to + 85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle. The UCN-5895A and UCN-5895A-2 are supplied in standard 16-pin dual in-line plastic packages with copper lead frames for increased allowable package power dissipation.

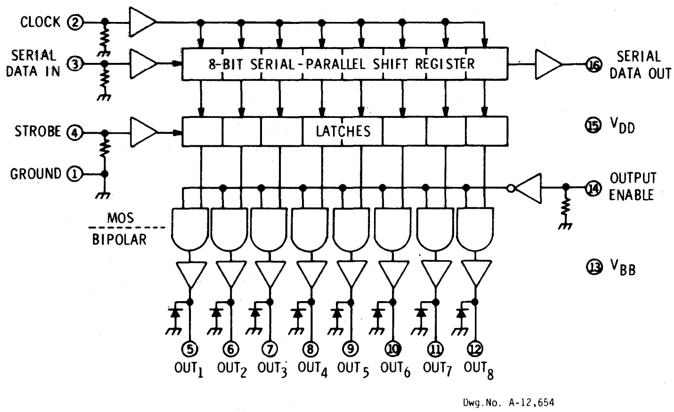
ABSOLUTE MAXIMUM RATINGS at T_A = + 25°C

Output Voltage, V_{OUT} (UCN-5895A)	50 V
(UCN-5895A-2)	25 V
Logic Supply Voltage Range, V_{DD}	4.5 V to 12 V
Driver Supply Voltage Range, V_{BB}	
(UCN-5895A)	5.0 V to 50 V
(UCN-5895A-2)	5.0 V to 25 V
Input Voltage Range, V_{IN}	− 0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT}	− 250 mA
Allowable Package Power Dissipation, P_D	1.67 W*
Operating Temperature Range, T_A	− 20°C to + 85°C
Storage Temperature Range, T_S	− 55°C to + 125°C

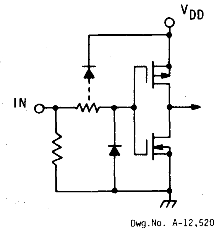
*Derate at the rate of 16.67 mW/°C above T_A = + 25°C.

Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

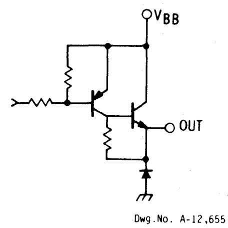
FUNCTIONAL BLOCK DIAGRAM



TYPICAL INPUT CIRCUIT



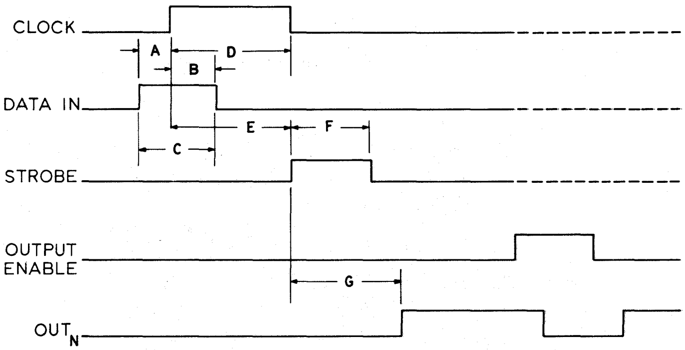
TYPICAL OUTPUT DRIVER



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 25 V, V_{DD} = 5 V to 12 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{OUT}	T_A = +25°C	—	−50	μA
		T_A = +70°C	—	−100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = −60 mA	—	1.1	V
		I_{OUT} = −120 mA	—	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = −120 mA, L = 2 mH, UCN-5895A only	35	—	V
		I_{OUT} = −120 mA, L = 2 mH, UCN-5895A-2 only	15	—	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	V_{DD} = 5 V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	50	μA
		V_{DD} = V_{IN} = 12 V	—	240	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	100	—	kΩ
		V_{DD} = 12 V	50	—	kΩ
Clock Frequency	f_c		3.3	—	MHz
Serial Data-Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	Output Enable to Output, I_{OUT} = −120 mA	—	2.0	μs
Turn-OFF Delay	t_{PHL}	Output Enable to Output, I_{OUT} = −120 mA	—	10	μs
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10	mA
		All outputs OFF	—	200	μA
	I_{DD}	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	μA
		V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	μA
		V_{DD} = 5 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	V_R = 25 V, T_A = +25°C	—	50	μA
		V_R = 25 V, T_A = +70°C	—	100	μA
Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,649

4

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... 75 ns
C. Minimum Data Pulse Width .... 150 ns
D. Minimum Clock Pulse Width .... 150 ns
E. Minimum Time Between Clock Activation and Strobe .... 300 ns
F. Minimum Strobe Pulse Width .... 100 ns
G. Typical Time Between Strobe Activation and Output Transition .... 1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

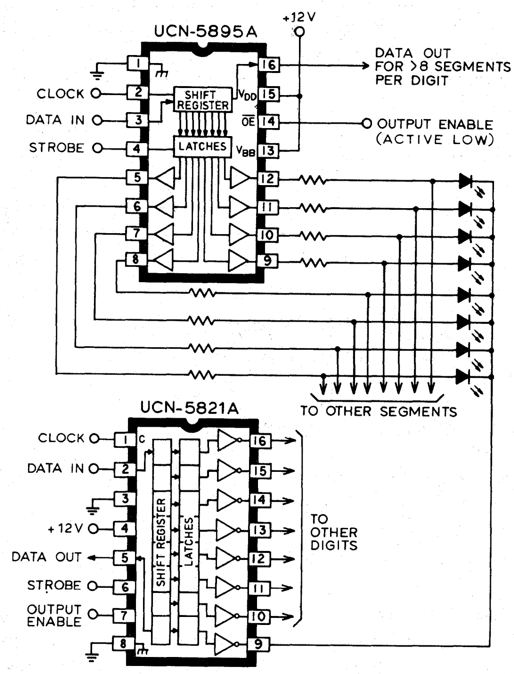
When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking Input	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL APPLICATION



Dwg. No. B-1541

UCN-5900A AND UCN-5901A BiMOS LATCH/DRIVERS

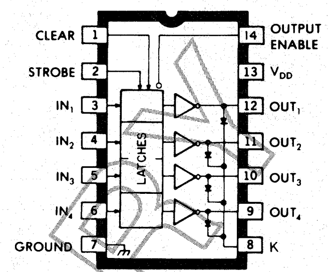
FEATURES

- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Output Sustaining Voltage of 90 V min.

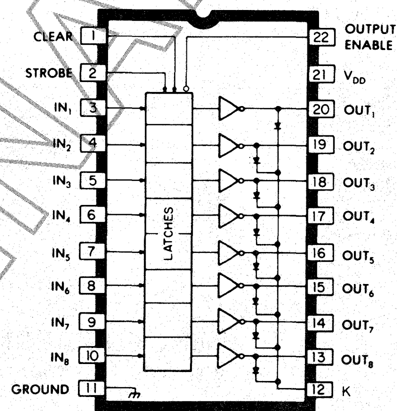
These high-voltage, high-current latch/ drivers are comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar CMOS combination provides an extremely low-power latch with maximum interface flexibility. The UCN-5900A contains four latch/drivers while the UCN-5901A contains eight latch/ drivers.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 400 mA and will sustain at least 150 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.



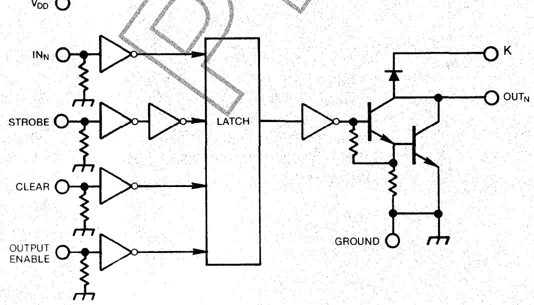
UCN-5900A



UCN-5901A

The UCN-5900A 4-latch device is furnished in a standard 14-pin dual in-line plastic package. The UCN-5901A 8-latch device is furnished in a 22-pin dual in-line plastic package with row centers on 0.400″ (10.16 mm) spacing. All outputs are pinned opposite their respective inputs to simplify circuit board layout.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{CE}	150 V
Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C	400 mA
Package Power Dissipation, P_D (UCN-5900A)	1.67 W*
(UCN-5901A)	2.0 W**
Operating Ambient Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

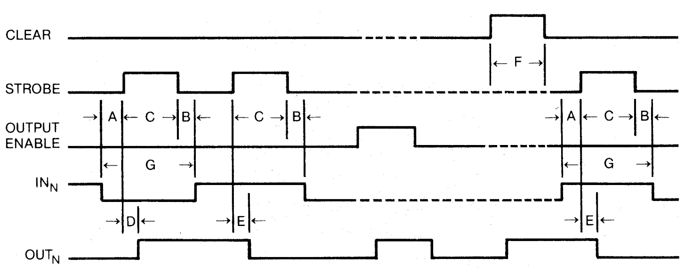
*Derate at the rate of 16.7 mW/°C above T_A = 25°C.
**Derate at the rate of 20 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Applicable Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 150 V, T_A = +25°C	—	—	50	μA
		V_{CE} = 150 V, T_A = +70°C	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.2	1.4	V
		I_C = 200 mA	—	1.4	1.6	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.6	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 5.0 V	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	All Drivers Off, All Inputs = 0 V	—	50	100	μA
Clamp Diode Leakage Current	I_R	V_R = 150 V, T_A = +25°C	—	—	50	μA
		V_R = 150 V, T_A = +70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 25 mA	90	—	—	V

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)



A. Minimum data active time before strobe enabled (data set-up time) .... 100 ns
B. Minimum data active time after strobe disabled (data hold time) .... 100 ns
C. Minimum strobe pulse width .... 300 ns
D. Typical time between strobe activation and output on to off transition .... 500 ns
E. Typical time between strobe activation and output off to on transition .... 500 ns
F. Minimum clear pulse width .... 300 ns
G. Minimum data pulse width .... 500 ns

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

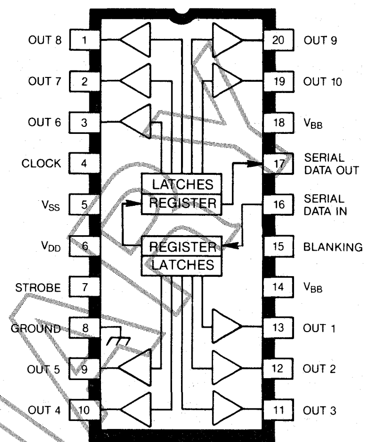
X = irrelevant
t-1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

UCN-5910A
HIGH-VOLTAGE BiMOS 10-BIT SERIAL-INPUT LATCHED DRIVER

FEATURES

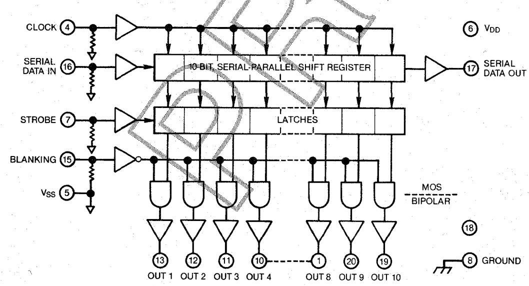
- 150 Volt Output Breakdown
- 50 mA push-pull outputs
- Low Power CMOS Logic
- Blanking and Strobe Functions
- High Data Rates—5 MHz.



The UCN-5910A is a 10-bit shift register latch driver which features 10 high-voltage push-pull outputs consisting of a bipolar sourcing device and a DMOS pull-down. These devices have been specifically designed to directly drive the grids or anodes of high voltage vacuum fluorescent displays (graphic panels and large alphanumeric) which require high voltage switching (80-150 V) to maintain adequate display brightness. The DMOS active pull-down function improves output switching over passive pulldowns which becomes especially important when driving loads of 100 V or more. Because of the output drive capability of this device (150 V, ±50 mA) and its relatively fast switching speed, it is also useful as an anode drive for a gas discharge display or as a driver for a piezo electric element in a drop on demand ink jet printer.

High impedance CMOS inputs, as well as fast data rates (5 MHz typically at V_{DD} = 5 V) make this device compatible with most uPs. When bussing several drive lines together, a pull-up resistor may be required to ensure a proper logic '1' level especially when interfacing with logic that has minimal sourcing capability (TTL, NMOS).

FUNCTIONAL BLOCK DIAGRAM



SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are low without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

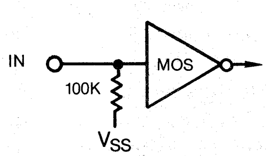
Driver Supply Voltage, V_{BB}	150 V
Output Current, I_{OUT}	±50 mA
Logic Supply Voltage, V_{DD}	15 V
Input Voltage, V_{IN}	−0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D	1.82 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = 25°C.

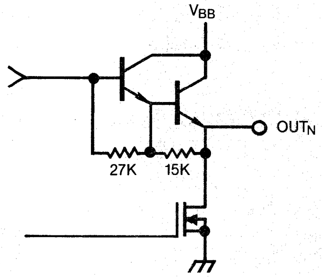
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 150 V, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	Output OFF, Blanking = 5 V, Output = 0 V	—	−10	μA
Output Pulldown Current	I_{OUT}	Output OFF, Output = 150 V, Blanking = V_{DD} = 5 V	10	20	mA
		Output OFF, Output = 150 V, Blanking = V_{DD} = 12 V	25	50	mA
Output ON Voltage	$V_{OUT(1)}$	Output ON, I_{OUT} = −40 mA	145	—	V
Output OFF Voltage	$V_{OUT(0)}$	Output OFF, I_{OUT} = 40 mA, Blanking = V_{DD} = 12 V	—	5.0	V
Supply Current	$I_{DD(OFF)}$	V_{DD} = 12 V	—	10	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5 V	—	100	μA
		V_{DD} = V_{IN} = 12 V	—	40	μA
Input Impedance	Z_{IN}	V_{DD} = 5 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	Blanking = 0.8 V, All Drivers ON, Outputs OPEN	—	2.0	mA
		Blanking = 5.0 V, All Outputs OPEN	—	100	μA

TYPICAL INPUT CIRCUIT

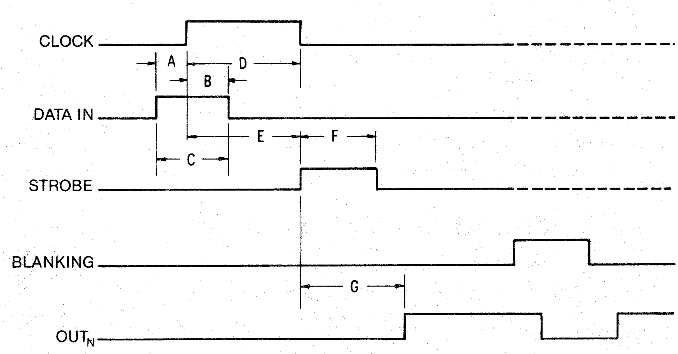


TYPICAL OUTPUT DRIVER



TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})



A. Minimum data active time before clock pulse (data set-up time) .... 75 ns
B. Minimum data active time after clock pulse (data hold time) .... 75 ns
C. Minimum data pulse width .... 150 ns
D. Minimum clock pulse width .... 150 ns
E. Minimum time between clock activation and strobe .... 150 ns
F. Minimum strobe pulse width .... 100 ns
G. Typical time between strobe activation and output transition .... 1.0 μs

RELIABILITY OF SERIES UCN-4800A AND UCN-5800A BiMOS DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series UCN-4800A and UCN-5800A BiMOS integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, burn-in, and accelerated-life tests:

1) Qualification testing is performed at an ambient temperature of +125°C, reduced so as to limit junction temperature to +150°C, for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure-rate data in a reasonable period of time.
2) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found that most failures are due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, are typically less than 0.1%.
3) Accelerated-life testing is performed at temperatures above +125°C and is used to generate failure-rate data.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution can be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminate level.

Table I contains data produced by life tests that were conducted at +150°C. The data include the number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C.

The data at the bottom of Table I are compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% fail-point. The median life at a junction temperature of +150°C is, in this case, 31,000 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1]

TABLE I
TEST RESULTS AT T_J = +150°C

		HOURS ON TEST											
TEST NUMBER	QTY.	48	90	150	300	600	1200	1800	2400	3000	5000	6000	7000
		NUMBER OF FAILURES											
1	35	0	0	0	0	0	0	0	0	0	0	5	7
2	25	0	0	3	0	1	6	—	—	—	—	—	—
3	21	0	1	—	—	—	—	—	—	—	—	—	—
4	30	0	0	4	9	—	—	—	—	—	—	—	—
5	17	0	0	0	0	2	0	0	0	0	1	0	2
6	20	0	0	3	10	0	—	—	—	—	—	—	—
7	20	0	0	0	0	0	2	0	1	0	0	—	—
8	25	0	0	1	0	2	0	2	0	0	0	1	—
9	25	0	0	0	1	0	0	0	0	0	2	—	—
10	25	0	0	0	0	0	0	—	—	—	—	—	—
11	30	0	0	0	0	0	0	0	—	—	—	—	—
12	30	0	0	0	0	0	0	0	—	—	—	—	—
13	30	0	0	0	5	0	0	0	0	0	—	—	—
14	30	0	0	0	0	0	1	0	2	—	—	—	—
15	26	0	0	0	—	—	—	—	—	—	—	—	—
16	30	0	0	0	0	—	—	—	—	—	—	—	—
17	20	1	0	0	1	0	0	—	—	—	—	—	—
18	25	0	0	0	0	0	0	—	—	—	—	—	—
19	28	0	0	0	0	0	0	—	—	—	—	—	—
20	45	0	0	0	0	0	0	—	—	—	—	—	—
21	25	0	0	0	0	0	—	—	—	—	—	—	—
TOTAL ON TEST		562	561	540	503	430	387	228	166	136	111	69	44
TOTAL FAILURES		1	1	11	26	5	9	2	3	0	3	6	9
TOTAL GOOD		561	560	529	477	425	378	226	163	136	108	63	35
P_s		.998	.998	.980	.948	.988	.977	.991	.982	1.00	.973	.913	.795
Cumulative P_s		.998	.996	.976	.926	.915	.894	.886	.870	.870	.846	.773	.615
$P_f = 1 - P_s$		.002	.004	.024	.074	.085	.106	.114	.130	.130	.154	.227	.385
% Failures		0.18	.036	2.39	7.43	8.51	10.6	11.4	13.0	13.0	15.4	22.7	38.5

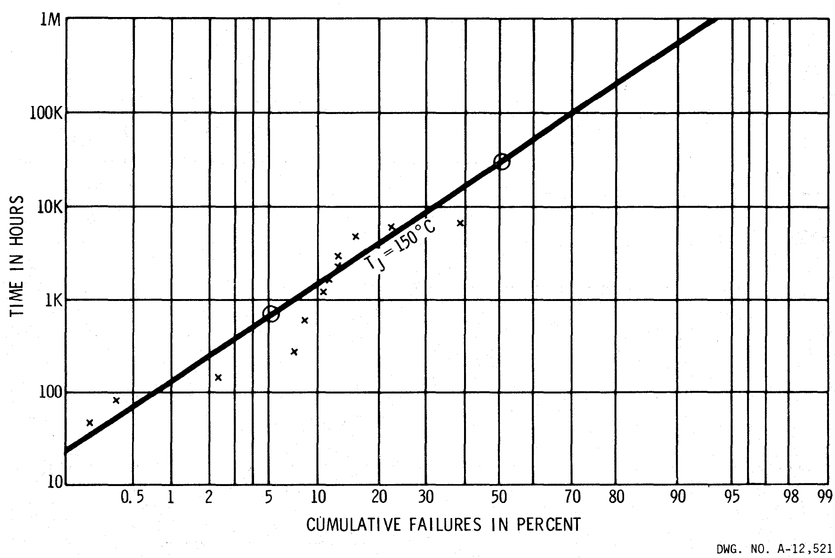


Figure 1
CUMULATIVE PERCENT FAILURES

The Arrhenius equation is:

$V_r = V_r^o e^{-\epsilon/kT}$

where V_r^o = a constant
ϵ = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5710M, and Series UDN-2980A devices at multiple temperatures. Failure analysis of devices rejected during that testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. The Arrhenius plot gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of $\varepsilon = 1.0$ eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life at reduced junction temperatures can now be determined using Figure 2. It must be emphasized that this is junction temperature and *not* ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\theta_{JA} + T_A \quad \text{or} \quad T_J = P_D\theta_{JC} + T_C$$

The median lifetime, or 50% fail-point, as graphically determined in Figure 2, is approximately 22 years at +125°C or 190 years at +100°C junction temperature.

The approximate failure rate (FR) may be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life line. The actual instantaneous failure rate can be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(1.7 \times 10^6\ hours)$$
$$= 0.06\%/1000\ hours = 600\ FIT$$

where *FIT* = failures per 10^9 unit-hours

Other failure-rate values have been calculated and appear in Table II.

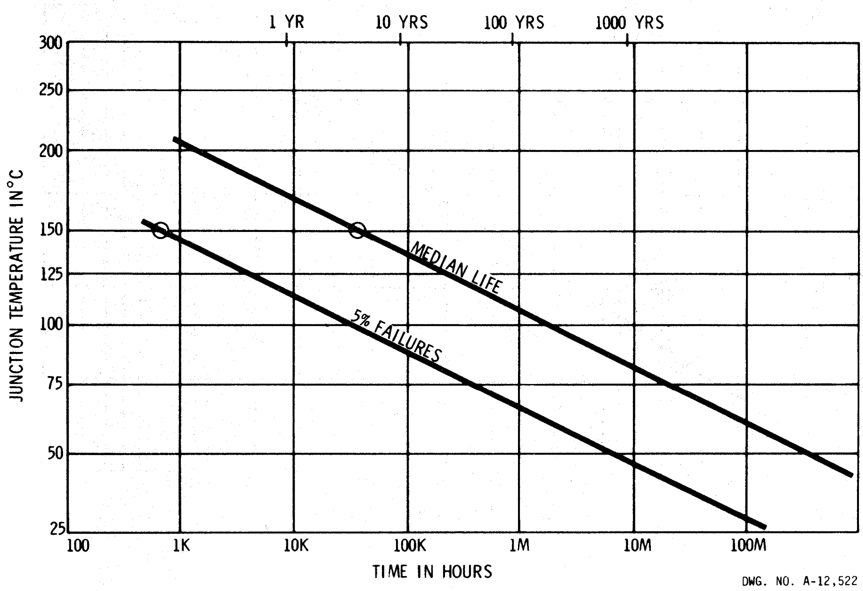


Figure 2
MEDIAN LIFE

TABLE II
SERIES UCN-4800A AND UCN-5800A FAILURE RATE

T_J (°C)	Median Life (h)	Failure Rate (%/1000h)	Failures In Time (No./10^9 unit-hours)
125	2×10^5	0.5	5000
100	1.7×10^6	0.06	600
75	1.7×10^7	0.006	60
50	3×10^8	0.0003	3

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides a failure rate within design objectives.

Figure 2 shows that a design with a continuous operating junction temperature of +100°C (internal power dissipation plus external ambient temperature) would reach the 5% failure point in 3.8 years. perature to +75°C increases the time to the 5% failure point to 42 years.

A complete sequence of environmental tests, including temperature cycle, pressure cooker, and biased humidity tests, are continuously monitored to ensure that assembly and package technology remain within established units.

The environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K.E., and Bird, D.W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208-213.

BiMOS II POWER DRIVERS

THE second generation of merged CMOS/bipolar integrated circuits extends the lead in innovative interface forged by Sprague Electric's original BiMOS power drivers.

Higher-density CMOS logic gives BiMOS II integrated circuits improved switching speeds at reduced costs. With a 5 V supply, second generation BiMOS typically operates at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. The BiMOS II series also offers new and improved functions, as shown below:

BiMOS II Type Number	CMOS Input Logic	Bipolar Output Ratings*	Original BiMOS Type Number
UCN-5800A	Quad Latch	350 mA/50 V Sink†	UCN-4401A
UCN-5801A	8-Bit Latch	350 mA/50 V Sink†	UCN-4801A
UCN-5810A	10-Bit Serial/Parallel and Latches	−25 mA/60 V Source	UCN-4810A
UCN-5810A-1	10-Bit Serial/Parallel and Latches	−25 mA/80 V Source	UCN-4810A-1
UCN-5812A	20-Bit Serial/Parallel and Latches	−25 mA/60 V Source	None
UCN-5812A-1	20-Bit Serial/Parallel and Latches	−25 mA/80 V Source	None
UCN-5813/14B	Quad Latch	1.5 A/50 V Sink†	None
UCN-5813/14B-1	Quad Latch	1.5 A/80 V Sink†	None
UCN-5815A	8-Bit Latch	−25 mA/60 V Source	UCN-4815A
UCN-5815A-1	8-Bit Latch	−25 mA/80 V Source	UCN-4815A-1
UCN-5818A	32-Bit Serial/Parallel and Latches	−25 mA/60 V Source	None
UCN-5818A-1	32-Bit Serial/Parallel and Latches	−25 mA/80 V Source	None
UCN-5821A	8-Bit Serial/Parallel and Latches	350 mA/50 V Sink	UCN-4821A
UCN-5822A	8-Bit Serial/Parallel and Latches	350 mA/80 V Sink	UCN-4822A
UCN-5823A	8-Bit Serial/Parallel and Latches	350 mA/100 V Sink	UCN-4823A
UCN-5825A	4-Bit Serial/Parallel and Latches	1.75 A/60 V Sink†	None
UCN-5826B	4-Bit Serial/Parallel and Latches	1.75 A/80 V Sink†	None
UCN-5832A	32-Bit Serial/Parallel and Latches	100 mA/40 V Sink	None
UCN-5841A	8-Bit Serial/Parallel and Latches	350 mA/50 V Sink†	None
UCN-5842A	8-Bit Serial/Parallel and Latches	350 mA/80 V Sink†	None
UCN-5843A	8-Bit Serial/Parallel and Latches	350 mA/100 V Sink†	None
UCN-5851/52A	32-Bit Serial/Parallel	±50 mA/200 V Sink/Source	None
UCN-5853/54A	32-Bit Serial/Parallel and Latches	±15 mA/60 V Sink/Source	None
UCN-5890A/B	8-Bit Serial/Parallel and Latches	−350 mA/80 V Source†	None
UCN-5891A/B	8-Bit Serial/Parallel and Latches	−350 mA/50 V Source†	None
UCN-5895A	8-Bit Serial/Parallel and Latches	−120 mA/50 V Source†	None

*Current ratings are maximum test condition; voltage ratings are absolute maximum allowable.
†Internal transient-suppression diodes included for inductive-load protection.

Reliable, single-chip BiMOS II solutions are available for a wide variety of peripheral and power interface problems. Two or more devices are no longer required to interface low-level (TTL, CMOS, NMOS, PMOS) LSI or microprocessor functions with power loads such as LEDs, gas-discharge or vacuum-fluorescent displays, relays, solenoids, thermal printers, motors, impact printer hammers, and incandescent lamps. Since all BiMOS devices include logic and control in addition to power functions, they also free the microprocessor from many housekeeping tasks.

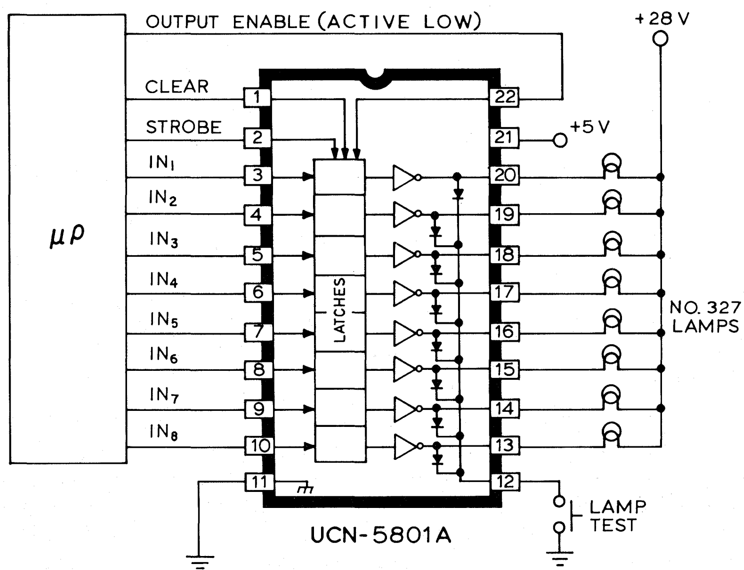
INCANDESCENT LAMP DRIVERS

EACH of the UCN-5800A or UCN-5801A open-collector Darlington outputs will sink up to 500 mA and will sustain at least 50 V in the OFF state. The high peak current rating of these devices allows their use with the high inrush (10 ×) currents normally associated with incandescent lamps. Internal diodes can be used to perform the lamp test function. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current: Either a reduction in output current or a suitable combination of duty cycle and number of active outputs is usually required.

The UCN-5800A is supplied in a standard 14-lead DIP. The UCN-5801A is furnished in a 22-lead DIP with 0.400″ row spacing.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . 45 V
Logic Supply Voltage Range . . . . 5.0 V to 12 V
Continuous Output Current . . . . 350 mA



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PLANAR GAS-DISCHARGE DISPLAY DRIVERS

COMBINING the high-voltage UCN-5810A-1, UCN-5812A-1, or UCN-5818A-1 serial-input, latched source driver with the UCN-5823A serial-input, latched sink driver provides a simple way to drive multiplexed high-voltage planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 .... 75 V
- UCN-5823A .... 95 V

Logic Supply Voltage Range .... 5.0 V to 12 V

Continuous Output Current
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 .... −25 mA
- UCN-5823A .... 350 mA

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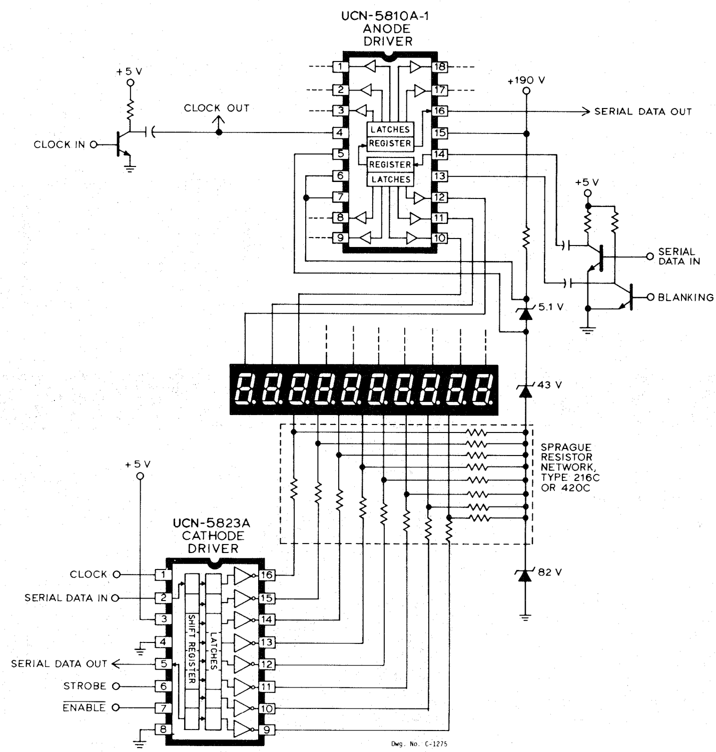


VACUUM-FLUORESCENT DISPLAY DRIVERS

THE UCN-5815A 8-bit, latched, source driver provides a practical means of driving the segments, dots (matrix panel), or bars of multiplexed high-voltage vacuum-fluorescent displays. The UCN-5810A (10-bit), UCN-5812A (20-bit), or UCN-5818A (32-bit) serial-input, latched source drivers are well-suited for use as character or digit drivers. The high-voltage versions (suffix -1) can also be used to drive the anodes of planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

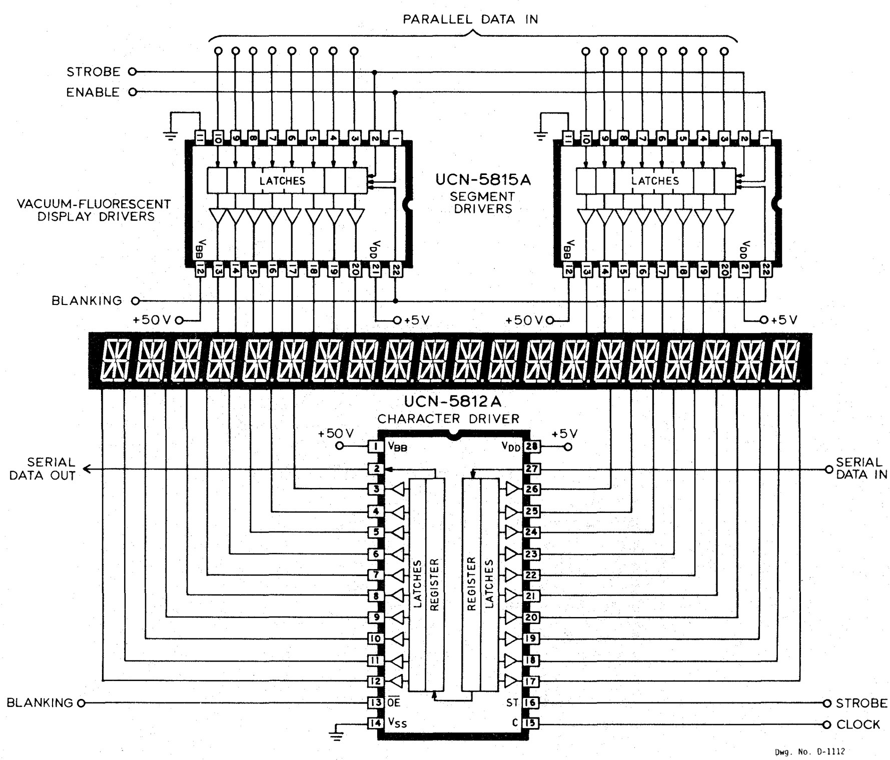
Output Voltage

UCN-5810A, UCN-5812A, UCN-5818A .... 55 V

UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 .... 75 V

Logic Supply Voltage Range .... 5.0 V to 12 V

Continuous Output Current .... −25 mA



MULTIPLEXED INCANDESCENT LAMP DRIVERS

IN ORDER to obtain brightness equivalent to normal d-c operation, multiplexed incandescent displays must be operated at a voltage:

$$E_{MPX} = E_{DC}\sqrt{N}$$

where E_{MPX} = the recommended operating supply voltage,
E_{DC} = the rated d-c lamp voltage, and
N = the number of digits being multiplexed.

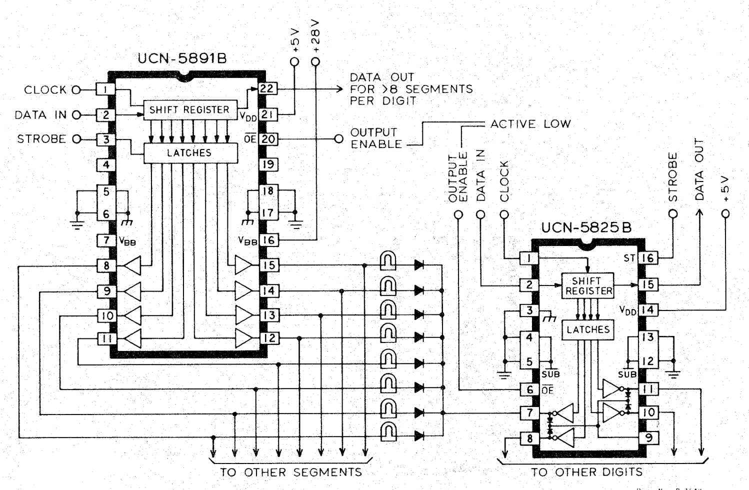
Multiplexed lamps also require isolation diodes to prevent sneak series/parallel paths to unaddressed elements.

Serial-input, latched source drivers provide simple, compact, and economical segment drivers for mutiplexed incandescent lamp applications. The UCN-5890A/B and UCN-5891A/B feature high-voltage, high-current (500 mA, peak) Darlington outputs. The UCN-5895A has saturated outputs for minimum voltage drop and will source up to 250 mA per driver. The drivers are supplied in an economical 16-pin "A" package or, for improved package power dissipation, a 22-pin "B" package. In either package style, UCN-5890, UCN-5891 and UCN-5895 are pin-compatible except for output ratings.

High-current UCN-5825B or UCN-5826B serial-input, latched sink drivers are used to drive the digits. Their high peak current rating is required to withstand the substantial inrush currents created by cold filaments. These BiMOS II power drivers also include internal thermal shutdown circuitry.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	
UCN-5825B	55 V
UCN-5826B	75 V
UCN-5890A/B	75 V
UCN-5891A/B	45 V
UCN-5895A	45 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	
UCN-5825B	1.75 A
UCN-5826B	1.75 A
UCN-5890A/B	−350 mA
UCN-5891A/B	−350 mA
UCN-5895A	−120 mA



MULTIPLEXED LED DRIVERS

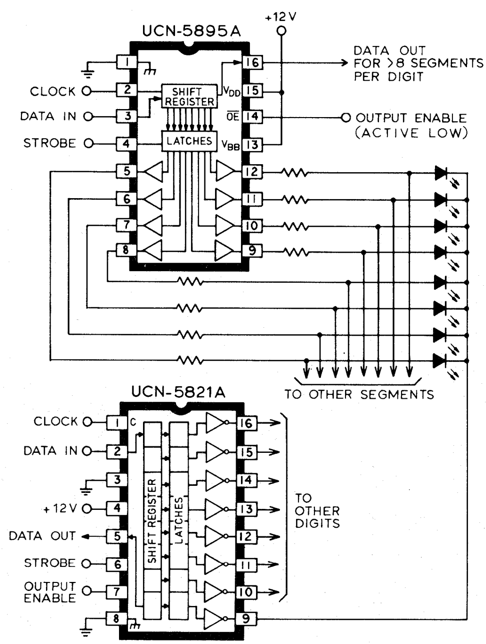
LATCHED source drivers are simple, compact, and economical segment drivers for multiplexed LED and incandescent lamp applications. The UCN-5895A features saturated outputs for minimum voltage drop. It sources a minimum of 120 mA per driver. The source driver is supplied in an economical 16-pin 'A' package.

A typical common-cathode LED display driver application is shown below. The high-current UCN-5821A, a latched sink driver, is used to drive the digits. Common-anode LED displays would require the use of the UCN-5891A source driver and UCN-5821A sink driver.

In order to obtain sufficient brightness, multiplexed LED displays must typically be operated at greatly increased current. Appropriate current limiting is required.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	
UCN-5821A	45 V
UCN-5890A/B	75 V
UCN-5891A/B	45 V
UCN-5895A	45 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	
UCN-5821A	350 mA
UCN-5890A/B	−350 mA
UCN-5891A/B	−350 mA
UCN-5895A	−120 mA

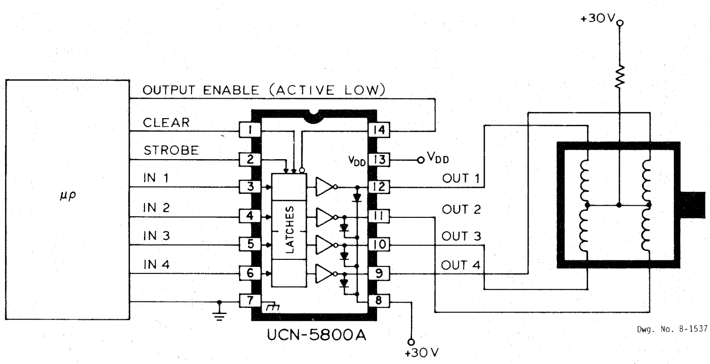


UNIPOLAR MOTOR DRIVERS

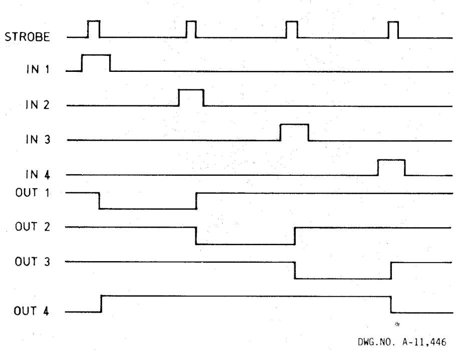
DRIVING unipolar motors is but one of the many successful applications for the UCN-5800A, UCN-5801A, UCN-5813B, and UCN-5814B BiMOS II latched sink drivers. The UCN-5801A is an eight-channel driver. The rest are four-channel drivers. The UCN-5814B includes CHIP ENABLE and CLEAR functions. Its larger 22-lead dual in-line package also allows increased package power dissipation without the use of an external heat sink. All devices contain CMOS data latches, CMOS control circuitry, and high-voltage, high-current bipolar Darlington outputs. Internal transient-protection diodes for use with inductive loads are included with all devices.

RECOMMENDED MAX. OPERATING CONDITIONS

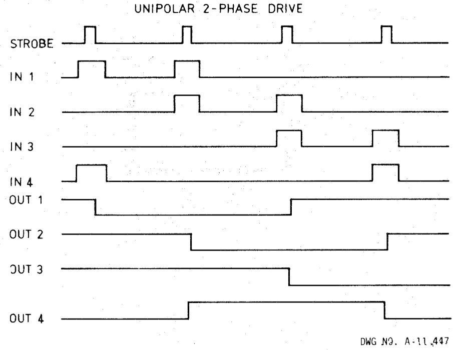
Output Voltage (Inductive Load)	
UCN-5800A, UCN-5801A,	
UCN-5813B, UCN-5814B	35 V
UCN-5813B-1, UCN-5814B-1	50 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	
UCN-5800A	350 mA
UCN-5801A	350 mA
UCN-5813B/B-1	1.5 A
UCN-5814B/B-1	1.5 A



UNIPOLAR WAVE DRIVE



UNIPOLAR 2-PHASE DRIVE



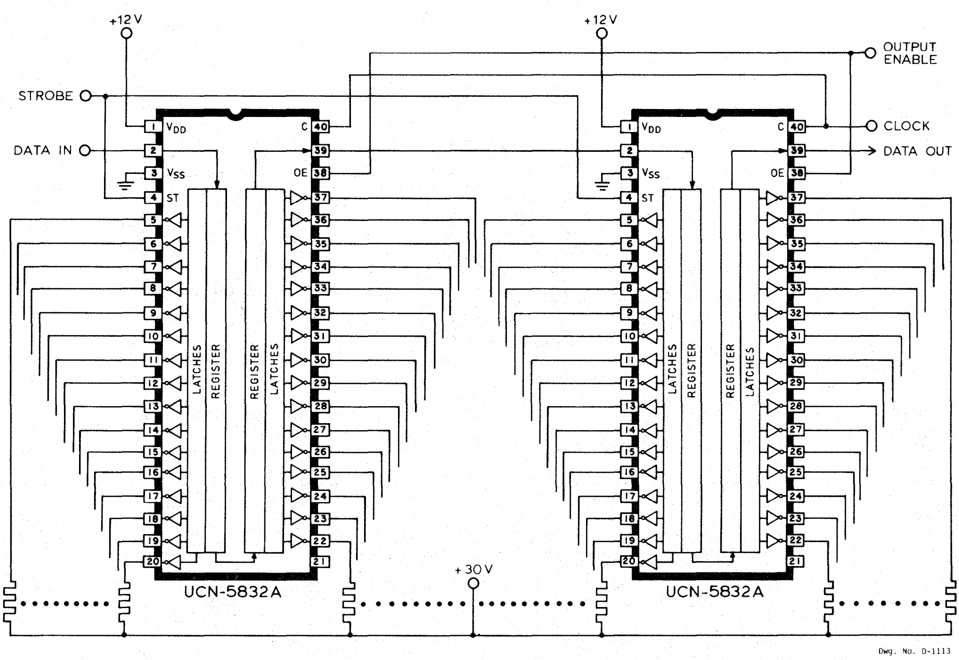
THERMAL PRINTHEAD DRIVER

DESIGNED primarily for use with thermal printheads, the UCN-5832A is optimized for low output-saturation voltage and high-speed operation. Each device has 32 bipolar, open-collector saturated outputs, a CMOS data latch for each driver, a 32-bit CMOS shift register, and CMOS control circuitry. A CMOS serial data output allows these devices to be cascaded in applications requiring more than 32 bits.

The UCN-5832A is supplied in a 40-pin DIP with 0.600" row spacing. Under normal conditions, all outputs will sustain 100 mA continuously without derating. They can also be supplied in unpackaged chip form or in a leaded chip carrier.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . 40 V
Logic Supply Voltage Range . . . . 5.0 V to 12 V
Continuous Output Current . . . . 100 mA



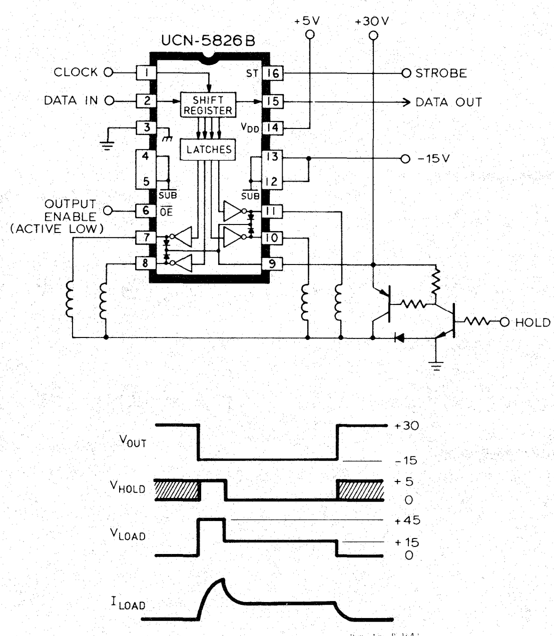
IMPACT PRINT-HAMMER DRIVERS

THE UCN-5825B and UCN-5826B 4-bit shift register/latched drivers are specifically designed for use with high-current inductive loads such as impact printers, solenoid, relays, and stepper motors. A CMOS serial data output allows cascading drivers where more than 4 bits is required. Except for output-voltage ratings, the two drivers are identical.

A bilevel current driver is shown. This application takes advantage of the split supply capability of the device. A relatively high turn-on current provides for high-speed operation and overcomes the inertia of a heavy solenoid or relay armature. The reduced holding current generates minimum heat and allows for improved power supply efficiency.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (Inductive Load)	
UCN-5825B	35 V
UCN-5826B	60 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	1.75 A



RELAY AND SOLENOID DRIVERS

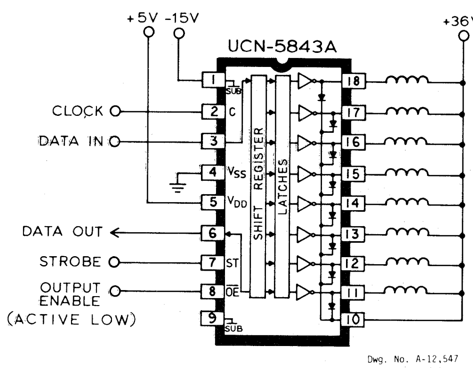
BiMOS II DRIVERS provide an interface flexibility beyond the reach of standard logic buffers and power-driver arrays. Drivers with internal transient-suppression diodes are ideal for use with relay and solenoid loads.

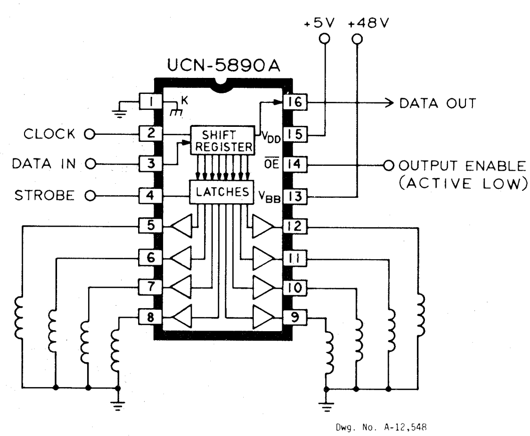
Series UCN-5840A sink drivers feature isolated logic and power grounds that allow split-supply operation or isolated grounds for reduction of transients and noise currents on common logic/load ground lines. The UCN-5890A and UCN-5890B source drivers require load supply voltages of at least 20 V. For lower-voltage operation, the UCN-5891A or UCN-5891B is recommended.

The serial DATA OUTPUT allows cascading for interface applications requiring additional drive lines. The OUTPUT ENABLE can also provide a CHIP ENABLE function that uses a minimum number of drive lines to control output from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (Inductive Load)	
UCN-5841A	35 V
UCN-5842A	50 V
UCN-5843A	60 V
UCN-5890A/B	50 V
UCN-5891A/B	35 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	350 mA



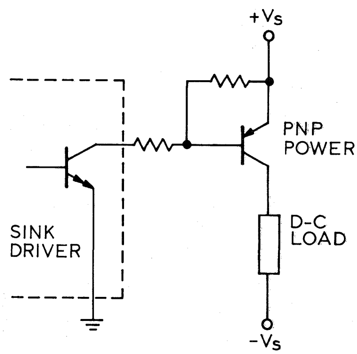


MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

SPRAGUE BiMOS II power drivers can also be used as multi-channel pre-drivers for discrete high-current semiconductors, reducing the need for many discrete components. BiMOS II sink drivers provide enough switching current to the bases of discrete PNP power transistors for load currents of up to 20 A. Higher load currents can be obtained by using power Darlington devices. BiMOS II source drivers may require discrete Darlington power drivers for significant load currents, but have the advantage of allowing rather wide load-voltage swings.

Higher voltage requirements can be satisfied with discrete semiconductors or with the BiMOS III devices described below.

For a-c loads, source drivers can be used to provide gate current (with appropriate current limiting) to a power SCR or triac. This scheme can provide an economical approach to many applications such as driving incandescent lamps or a-c motors with current levels of up to 20 A.



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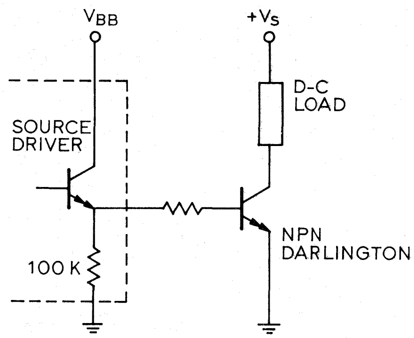

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4

SERIES UCN-5900 BiMOS III *HIGH-VOLTAGE* INTERFACE DRIVERS

THE original UCN-4800 BiMOS interface integrated circuit designs evolved into high-speed UCN-5800 BiMOS II designs. Improvements continue with the new 150 V Sprague Series UCN-5900 *BiMOS III* designs.

Original BiMOS Type Number	BiMOS II Type Number	BiMOS III Type Number
UCN-4401A (50 V)	UCN-5800A (50 V)	UCN-5900A (150 V)
UCN-4801A (50 V)	UCN-5801A (50 V)	UCN-5901A (150 V)
UCN-4810A-1 (80 V)	UCN-5810A-1 (80 V)	UCN-5910A (150 V)

Detailed information on the new BiMOS III parts is available directly from the factory in Worcester, Mass., Telephone (617) 853-5000.

SECTION 5—MILITARY AND AEROSPACE DEVICES

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

5

SERIES UDS-0400H/R, UDS-0400H/R-1, UDS-0500H/R POWER & RELAY DRIVERS —Hermetically Sealed

FEATURES

- 500 mA Output Current-Sink Capability
- Four Logic Types
- Pinning Compatible with 54/74 Logic Series
- High-Voltage Output:
  100 V Series UDS-0500H/R
  70 V Series UDS-0400H/R-1
  40 V Series UDS-0400H/R

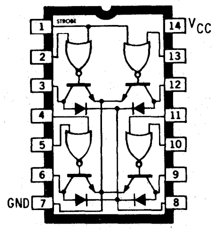
THE 48 HERMETIC DEVICES in these three versatile interface series each combine logic gates and high-current switching transistors on the same chip. The integrated circuits drive incandescent lamps, relays, solenoids, and other peripheral power loads.

Four of eight logic/output configurations are shown at right. For others, see following pages. Drivers rated for use with inductive loads have internal transient-suppression diodes. Three minimum output-breakdown voltage ratings are available: 40 V (Series UDS-0400H/R), 70 V (Series UDS-0400H/R-1), and 100 V (Series UDS-0500H/R).

These devices are supplied in either the popular glass/metal side-brazed 14-pin hermetic package (suffix "H") or lower-cost ceramic/glass cer-DIP hermetic packages (suffix "R"). Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of −55°C to +125°C.

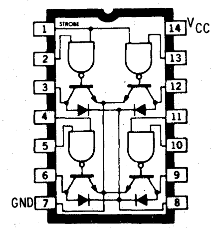
Reverse-bias burn-in and 100% high-reliability screening are standard for all Series UDS-0400H, UDS-0400H-1, and UDS-0500H devices. The tests are optional for series UDS-0400R, UDS-0400R-1, and UDS-0500R.

Series UDS-0400H, UDS-0400H-1, and Series UDS-0500H were previously manufactured as the Series UHD-400, UHD-400-1, and UHD-500. Power and relay drivers in flat-pack packages, Series UHC-400, UHC-400-1, and UHC-500, will continue to be available on special order as Series UDS-0400J, UDS-0400J-1, and UDS-0500J.



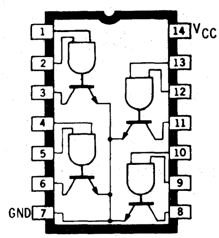
Dwg. No. A-9130A

UDS-0403H/R
UDS-0403H/R-1
UDS-0503H/R



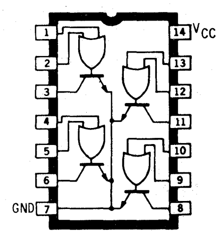
DWG. NO. A-7880A

UDS-0406H/R
UDS-0406H/R-1
UDS-0506H/R



DWG. NO. A-12,388

UDS-0408H/R
UDS-0408H/R-1
UDS-0508H/R



DWG. NO. A-12,389

UDS-0432H/R
UDS-0432H/R-1
UDS-0532H/R

Device Part Number Designation

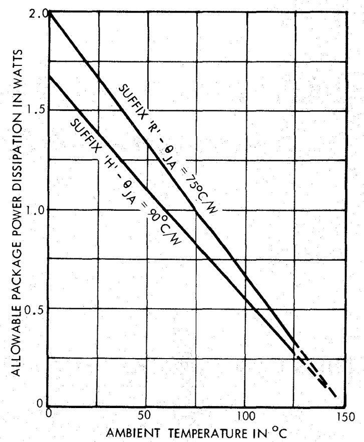
Part Numbers*			Function
0400	0400-1	0500	Quad 2-Input AND
0402	0402-1	0502	Quad 2-Input OR
0403	0403-1	0503	Quad OR for Inductive Loads
0406	0406-1	0506	Quad AND for Inductive Loads
0407	0407-1	0507	Quad NAND for Inductive Loads
0408	0408-1	0508	Quad 2-Input NAND
0432	0432-1	0532	Quad 2-Input NOR
0433	0433-1	0533	Quad NOR for Inductive Loads

*Complete part number includes the prefix "UDS-" and a suffix that identifies package style.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 7 V
Output Voltage, V_{IN} .... 5.5 V
Output Off-State Voltage, V_{OFF}
Series UDS-0400H/R .... 40 V
Series UDS-0400H/R-1 .... 70 V
Series UDS-0500H/R .... 100 V
Output On-State Sink Current, I_{ON}
(one driver) .... 500 mA
(total package) .... 1 A
Suppression Diode Off-State Voltage, V_R
Series UDS-0400H/R .... 40 V
Series UDS-0400H/R-1 .... 70 V
Series UDS-0500H/R .... 100 V
Suppression Diode On-State Current, I_F .... 500 mA
Operating Free-Air Temperature Range, T_A .... −55°C to +125°C
Storage Temperature Range, T_S .... −65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION



Dwg.No. A-10,884A

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into Any Output (ON State)	—	—	250	mA

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

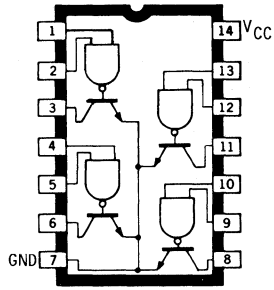
Characteristic	Series	Test Conditions (Note 3)	Limits Min.	Limits Typ.	Limits Max.	Units
Turn-On Delay Time (t_{pd0})	UDS-0400H/R	V_S = 40 V, R_L = 265Ω (6 W)	—	200	500	ns
	UDS-0400H/R-1	V_S = 70 V, R_L = 465Ω (10 W)	—	200	500	ns
	UDS-0500H/R	V_S = 100 V, R_L = 670Ω (15 W)	—	200	500	ns
Turn-Off Delay Time (t_{pd1})	UDS-0400H/R	V_S = 40 V, R_L = 265Ω (6 W)	—	300	750	ns
	UDS-0400/R-1	V_S = 70 V, R_L = 465Ω (10 W)	—	300	750	ns
	UDS-0500/R	V_S = 100 V, R_L = 670Ω (15 W)	—	300	750	ns

NOTES:
1. Each input tested separately.
2. Voltage values shown in the test-circuit waveforms are with respect to network ground terminal.
3. C_L = 15 pF. Capacitance value specified includes probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0 V	t_f = 7.0 ns	t_p = 1.0 μs
$V_{in(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

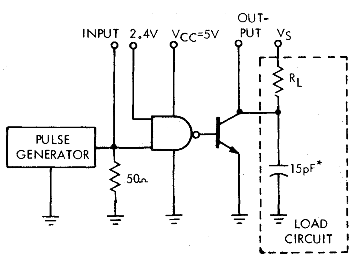
UDS-0400H/R, UDS-0400H/R-1, UDS-0500H/R
Quad 2-Input AND Power Drivers

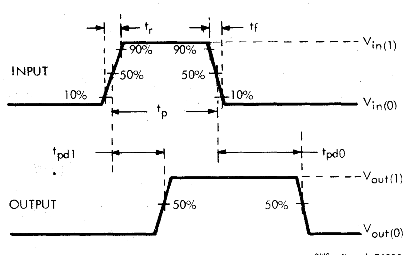


ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0400H/R	4.5 V	2.0 V	2.0 V	40 V	—	—	100	µA
			UDS-0400H/R-1	4.5 V	2.0 V	2.0 V	70 V	—	—	100	µA
			UDS-0500H/R	4.5 V	2.0 V	2.0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	17.5	26.5	mA

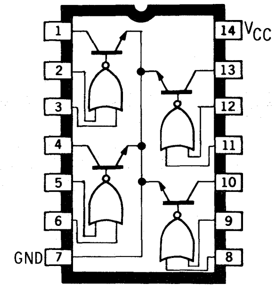
NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.





*Includes probe and test fixture capacitance.

UDS-0402H/R, UDS-0402H/R-1, UDS-0502H/R
Quad 2-Input OR Power Drivers



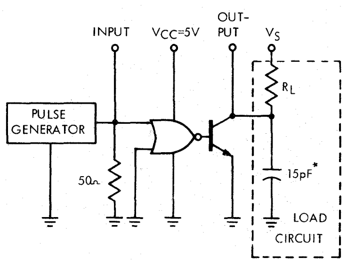
DWG. NO. A-7608

5

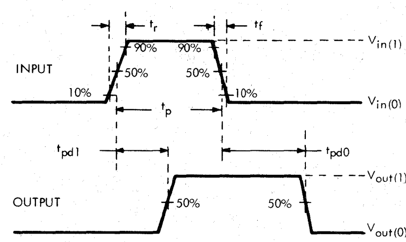
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions: V_{CC}	Driven Input	Other Input	Output	Limits: Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0402H/R	4.5 V	2.0 V	0 V	40 V	—	—	100	μA
			UDS-0402H/R-1	4.5 V	2.0 V	0 V	70 V	—	—	100	μA
			UDS-0502H/R	4.5 V	2.0 V	0 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.1	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	18	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.

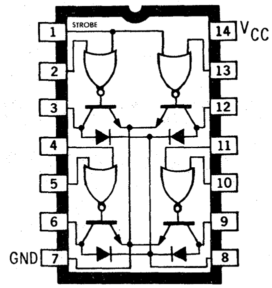


DWG. NO. A-7877B



DWG. No. A-7628C

*Includes probe and test fixture capacitance.



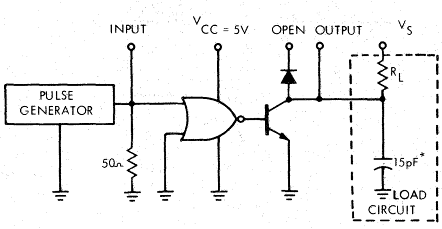
Dwg. No. A-9130A

UDS-0403H/R, UDS-0403H/R-1, UDS-0503H/R
Quad OR Relay Drivers

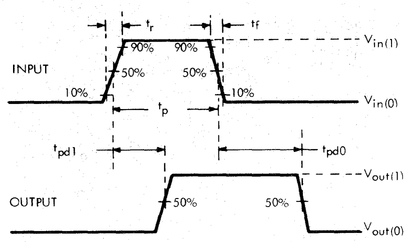
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions: V_{CC}	Driven Input	Other Input	Output	Limits: Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0403H/R	4.5 V	2.0 V	0 V	40 V	—	—	100	μA
			UDS-0403H/R-1	4.5 V	2.0 V	0 V	70 V	—	—	100	μA
			UDS-0503H/R	4.5 V	2.0 V	0 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Strobe Input Current	$I_{IN(1)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(0)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	μA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. Measured at rated minimum output-breakdown voltage.



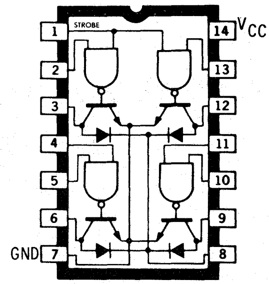
DWG. NO. A-9123B



DWG. No. A-7628C

*Includes probe and test fixture capacitance.

UDS-0406H/R, UDS-0406H/R-1, UDS-0506H/R
Quad AND Relay Drivers

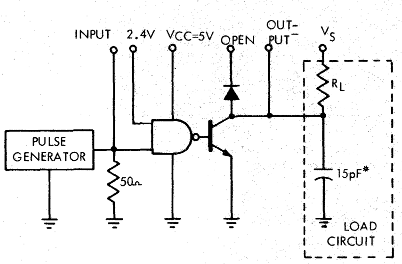


DWG. NO. A-7880A

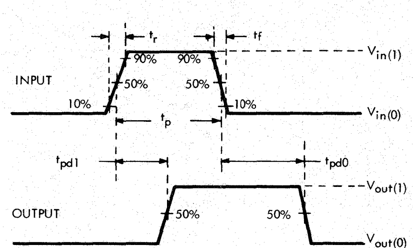
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0406H/R	4.5 V	2.0 V	2.0 V	40 V	—	—	100	μA
			UDS-0406H/R-1	4.5 V	2.0 V	2.0 V	70 V	—	—	100	μA
			UDS-0506H/R	4.5 V	2.0 V	2.0 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Strobe Input Current	$I_{IN(1)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(0)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	μA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	17.5	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. Measured at rated minimum output-breakdown voltage.



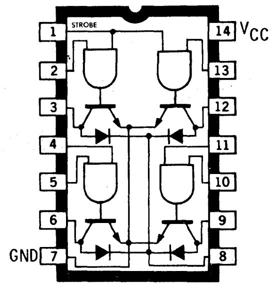
DWG. NO. A-7878B



DWG. No. A-7628C

*Includes probe and test fixture capacitance.

UDS-0407H/R, UDS-0407H/R-1, UDS-0507H/R
Quad NAND Relay Drivers

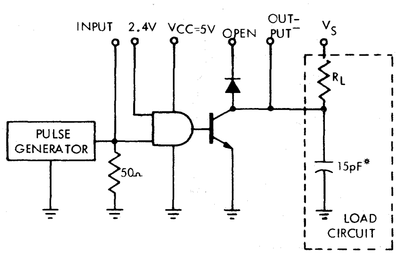


DWG. NO. A-7973A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

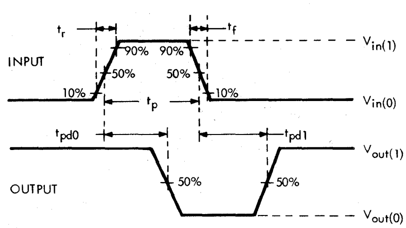
Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0407H/R	4.5 V	0.8 V	4.5 V	40 V	—	—	100	µA
			UDS-0407H/R-1	4.5 V	0.8 V	4.5 V	70 V	—	—	100	µA
			UDS-0507H/R	4.5 V	0.8 V	4.5 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(1)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(0)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. Measured at rated minimum output-breakdown voltage.



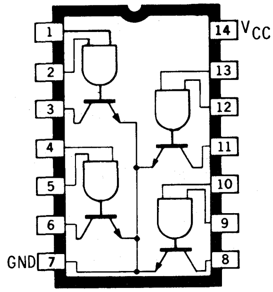
DWG. NO. A-7899B

*Includes probe and text fixture capacitance.



DWG. NO. A-7900A

UDS-0408H/R, UDS-0408H/R-1, UDS-0508H/R
Quad 2-Input NAND Power Drivers

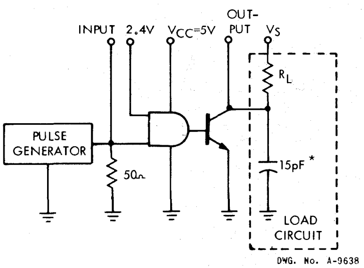


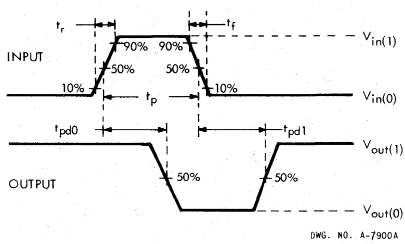
DWG. NO. A-12,388

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

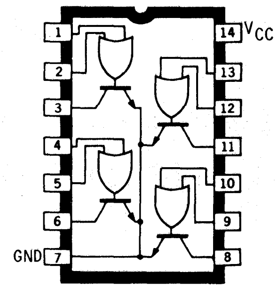
Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0408H/R	4.5 V	0.8 V	4.5 V	40 V	—	—	100	μA
			UDS-0408H/R-1	4.5 V	0.8 V	4.5 V	70 V	—	—	100	μA
			UDS-0508H/R	4.5 V	0.8 V	4.5 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.





*Includes probe and test fixture capacitance.



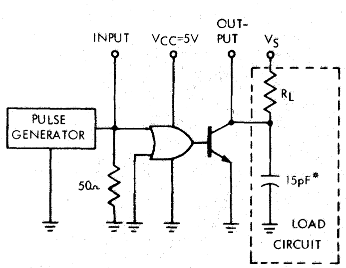
DWG. NO. A-12,389

UDS-0432H/R, UDS-0432H/R-1, UDS-0532H/R
Quad 2-Input NOR Power Drivers

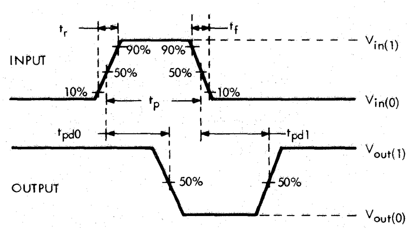
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0432H/R	4.5 V	0.8 V	0.8 V	40 V	—	—	100	μA
			UDS-0432H/R-1	4.5 V	0.8 V	0.8 V	70 V	—	—	100	μA
			UDS-0532H/R	4.5 V	0.8 V	0.8 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.



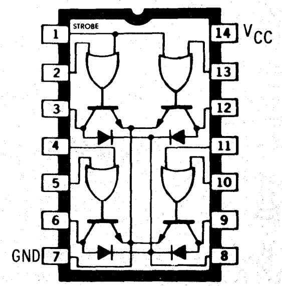
DWG. NO. A-7902B



DWG. NO. A-7900A

*Includes probe and test fixture capacitance.

UDS-0433H/R, UDS-0433H/R-1, UDS-0533H/R
Quad NOR Relay Drivers

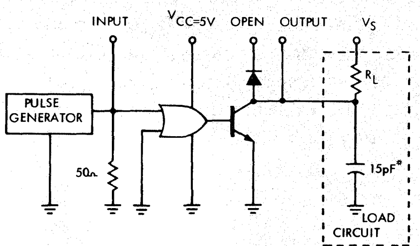


DWG. NO. A-12,390

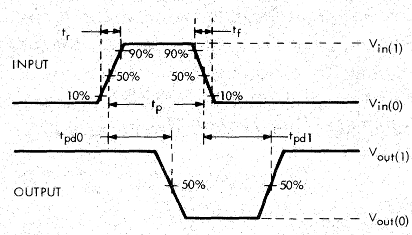
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UDS-0433H/R	4.5 V	0.8 V	0.8 V	40 V	—	—	100	μA
			UDS-0433H/R-1	4.5 V	0.8 V	0.8 V	70 V	—	—	100	μA
			UDS-0533H/R	4.5 V	0.8 V	0.8 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	+25°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−550	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Strobe Input Current	$I_{IN(1)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(0)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	μA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values at are V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. Measured at rated minimum output-breakdown voltage.



DWG. NO. A-9135B



DWG. NO. A-7900A

*Includes probe and test fixture capacitance.

5

UCS-5800R AND UCS-5801R HERMETIC BiMOS II LATCHED DRIVERS

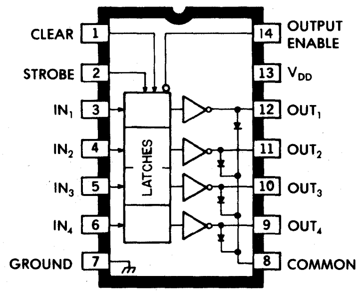
FEATURES

- 4.4 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Control & Latches
- High-Voltage, High-Current Outputs
- Transient-Protected Outputs
- Operating Temperature − 55°C to + 125°C
- Cer-DIP Hermetic Packages

SIMPLIFYING interface between LSI and peripheral power loads, the hermetically-sealed UCS-5800R (4-bit) and UCS-5801R (8-bit) latched drivers combine the advantages of CMOS logic/control and high-voltage/high-current bipolar output buffers. Typical applications include microprocessor interface to relays, solenoids, d-c and stepper motors, printers, LED or incandescent displays, etc. requiring hermetic packaging and an operating temperature range of − 55°C to + 125°C. Both devices are subject to 100% screening to stringent high-reliability requirements (see page 8). Additional high-temperature reverse-bias burn-in is specified by adding the suffix "-MIL" to the part number.

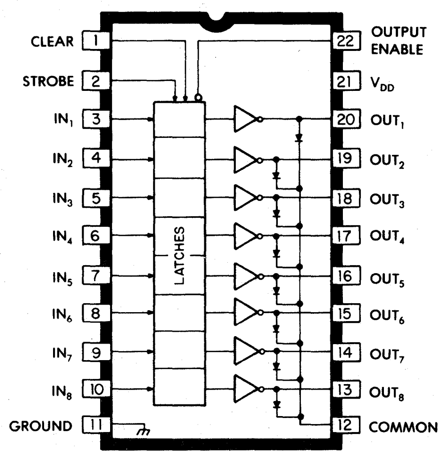
BiMOS II latches have improved input data rates over the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors.

The Darlington open-collector outputs will drive power loads rated to 50 V and 350 mA (500 mA max.). Integral diodes for inductive load transient suppression are included. Because of limitations on package power dissipation, the simultaneous operation of all drivers at high current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.



DWG. NO. A-10,499B

UCS-5800R

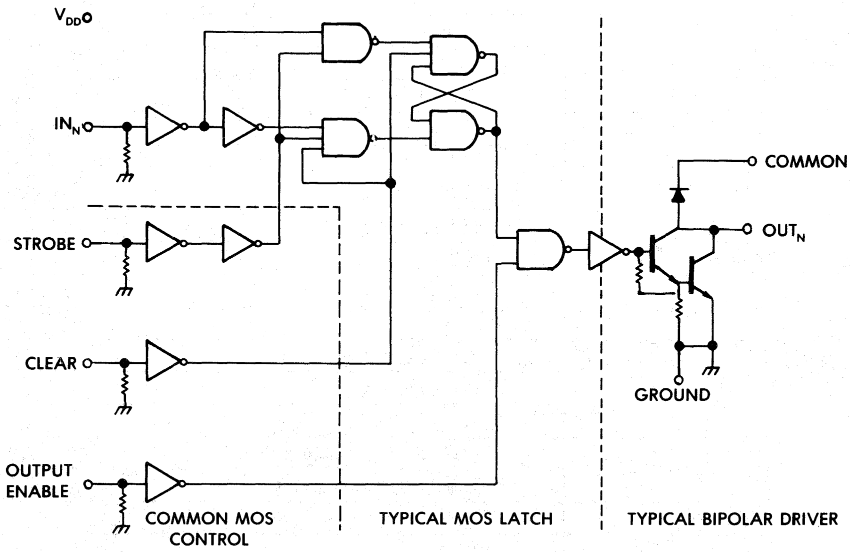


DWG. NO. A-10,498B

UCS-5801R

The 4-bit, UCS-5800R is furnished in a standard 14-pin dual in-line ceramic/glass cer-DIP hermetic package. The 8-bit, UCS-5801R is supplied in a 22-pin dual in-line ceramic/glass cer-DIP hermetic package with row spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs. Both packages conform to the dimensional requirements of MIL-M-38510.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

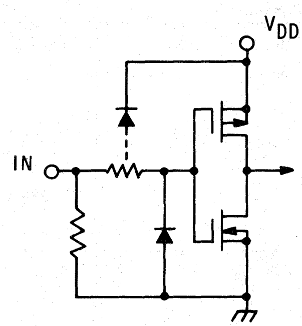
Output Voltage, V_{CE} .... 50 V
Supply Voltage, V_{DD} .... 15 V
Input Voltage Range, V_{IN} .... −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C .... 500 mA
Package Power Dissipation, P_D
(UCS-5800R) .... 1.4 W*
(UCS-5801R) .... 1.75 W**
Operating Temperature Range, T_A .... −55°C to +125°C
Storage Temperature Range, T_S .... −65°C to +150°C

*Derate at the rate of 13.3 mW/°C above T_A = +25°C.
**Derate at the rate of 16.7 mW/°C above T_A = +25°C.

NOTE: Output current rating may be limited by duty cycle, ambient temperature, air flow, and number of outputs conducting. Under any set of conditions, do not exceed a maximum junction temperature of +130°C.

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50$ V	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100$ mA	—	1.1	V
		$I_C = 200$ mA	—	1.3	V
		$I_C = 350$ mA, $V_{DD} = 7.0$ V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12$ V	10.5	—	V
		$V_{DD} = 10$ V	8.5	—	V
		$V_{DD} = 5.0$ V (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12$ V	50	—	kΩ
		$V_{DD} = 10$ V	50	—	kΩ
		$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12$ V, Outputs Open	—	2.0	mA
		$V_{DD} = 10$ V, Outputs Open	—	1.7	mA
		$V_{DD} = 5.0$ V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12$ V, Outputs Open, Inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50$ V	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350$ mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5$ V (unless otherwise specified)

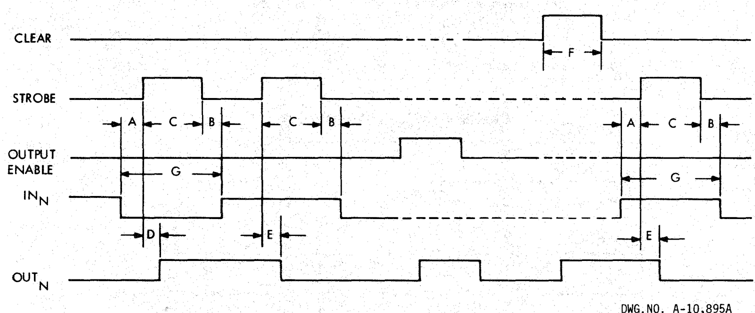
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50$ V	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100$ mA	—	1.3	V
		$I_C = 200$ mA	—	1.5	V
		$I_C = 350$ mA, $V_{DD} = 7.0$ V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12$ V	11	—	V
		$V_{DD} = 10$ V	9.0	—	V
		$V_{DD} = 5.0$ V (See Note)	3.6	—	V
Input Resistance	R_{IN}	$V_{DD} = 12$ V	35	—	kΩ
		$V_{DD} = 10$ V	35	—	kΩ
		$V_{DD} = 5.0$ V	35	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12$ V, Outputs Open	—	2.5	mA
		$V_{DD} = 10$ V, Outputs Open	—	1.9	mA
		$V_{DD} = 5.0$ V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12$ V, Outputs Open, Inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50$ V	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350$ mA	—	2.1	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.3	V
		I_C = 200 mA	—	1.5	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."



TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) .... 50 ns
B. Minimum data active time after strobe disabled (data hold time) .... 50 ns
C. Minimum strobe pulse width .... 125 ns
D. Typical time between strobe activation and output on to off transition .... 500 ns
E. Typical time between strobe activation and output off to on transition .... 500 ns
F. Minimum clear pulse width .... 300 ns
G. Minimum data pulse width .... 225 ns

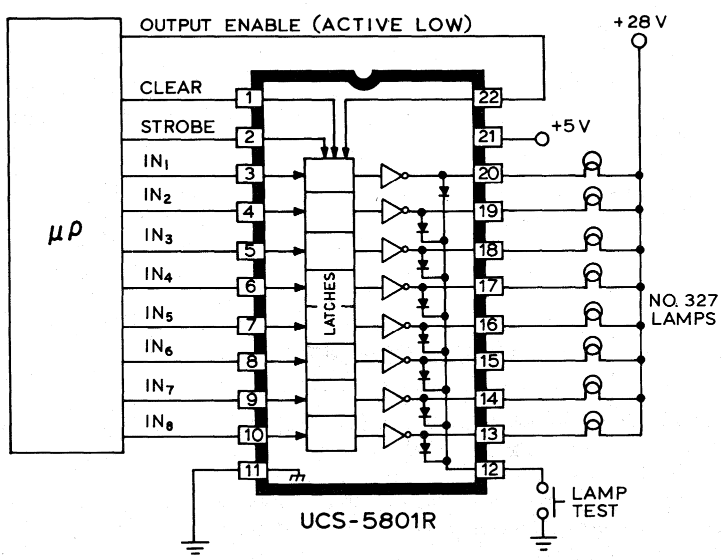
TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

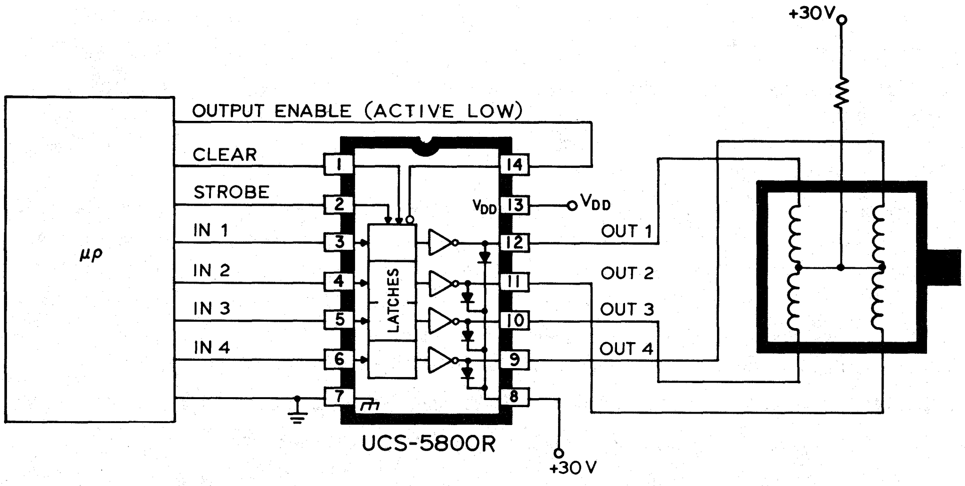
TYPICAL APPLICATION
INCANDESCENT LAMP DRIVER



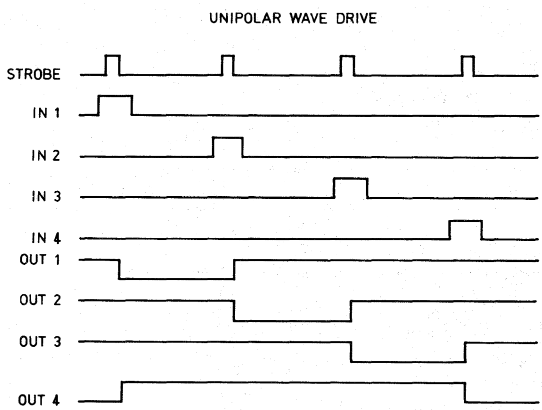
Dwg. No. A-12,656

TYPICAL APPLICATION

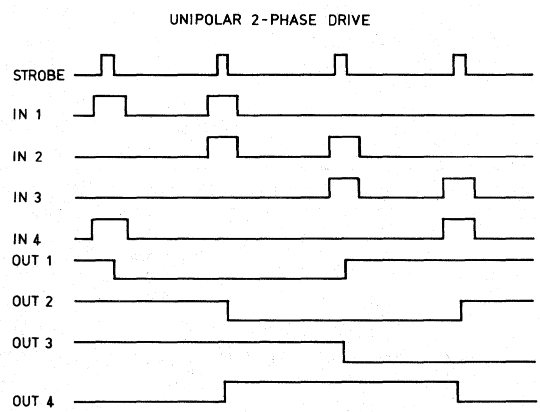
UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. No. B-1547



DWG.NO. A-11,446



DWG.NO. A-11,447

5

HERMETIC DEVICES AND HIGH-RELIABILITY SCREENING

Sprague integrated circuits with extended temperature ranges and in hermetic packages are intended for use in military and aerospace programs requiring unique Sprague device performance characteristics and proven reliability. To accomplish this, Sprague Electric Company utilizes extensive quality conformance proceedures, including selected and relevant tests and requirements from MIL-STD-883.

Customer orders classified with any reference to MIL-STD-883 must comply with paragraphs 1.2.1 and 1.2.2 of that standard. These paragraphs require that references to that standard cannot be used unless the device is manufactured in complete compliance with all of the requirements of MIL-STD-883 and MIL-M-38510 without deviations. Therefore, and

notwithstanding anything contained in the customer specification or any imposed document, all references to processing and testing of Sprague hermetically sealed integrated circuits in conformance to the requirements of MIL-M-38510, and all references to the requirements imposed by MIL-STD-883, are hereby deleted and replaced by the following:

1. The design, material, performance, control, and documentation for these devices shall be performed as set forth in the latest issue of the Sprague Electric Company Integrated Circuit Quality Assurance and Reliability Manual.

2. Electrical test characteristics shall be in accordance with the applicable Sprague Electric Company Engineering Bulletin.

3. Screening and preconditioning will be performed in accordance with the following methods:

3.1. All hermetic devices are subjected to 100% production screen tests consisting of the following:

Screen	Conditions	MIL-STD-883 Test Method
Internal Visual	—	2010, Cond. B
Stabilization Bake	150°C, 24 hours	1008, Cond. C
Thermal Shock	0°C to 100°C, 15 cycles	1011, Cond. A
Constant Acceleration	30,000 Gs, Y1 plane	2001, Cond. E
Fine Seal	5×10^{-7} atm•cm^3/s maximum	1014, Cond. A
Gross Seal	—	1014, Cond. C
Electrical	Per specification	—
Marking	Sprague or customer part number, date code, lot identification, index point	—

3.2. All high-reliability devices ('-MIL' suffix) are subjected to additional 100% screening consisting of the following:

Screen	Conditions	MIL-STD-883 Test Method
Interim Electrical	25°C per specification	—
Burn-In	125°C, 160 hours	1015, Cond. A
Final Electrical	25°C, −55°C, and +125°C per specification	—
Fine Seal	5×10^{-7} atm•cm^3/s maximum	1014, Cond. A
Gross Seal	—	1014, Cond. C
External Visual	—	2009

3.3. All screens are in accordance with industry standards with copies available on request.

4. Quality conformance inspection and qualification is performed routinely on each production lot, every 90 days, and every 6 months, as required.

SECTION 6—RADIO/COMMUNICATIONS INTEGRATED CIRCUITS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.
®CQUAM (Compatible QUadrature Amplitude Modulation) is a registered trademark of Motorola, Inc.

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SELECTION GUIDE TO RADIO/COMMUNICATIONS INTEGRATED CIRCUITS

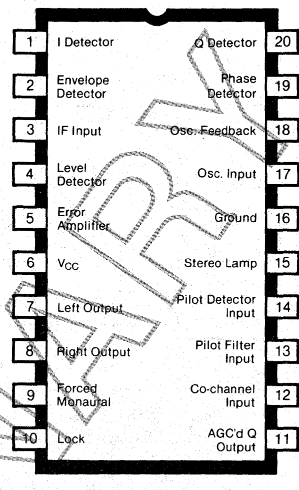
Device Type	R-F Mixer	F-M I-F	F-M Det.	Mute/ Squelch	Δ f Mute	Stereo Decoder	A-M Radio	Audio Amp.	Supply Voltage Range
ULN-2111A	—	X	X	—	—	—	—	—	8-14 V
ULN-2204A	—	X	X	—	—	—	X	X	2-12 V
ULN-2240A	—	X	X	X	X	—	X	—	8.5-16 V
ULN-2241A	—	X	X	—	—	—	X	—	10-16 V
ULN-2243A	X	X	—	—	—	—	—	—	8-12 V
ULN-2249A	—	—	—	—	—	—	X	—	8-16 V
ULN-3803A	—	X	X	—	—	—	X	—	3-12 V
ULN-3809A	—	—	—	—	—	X	—	—	9-16 V
ULN-3812A	—	—	—	—	—	X	—	—	9-16 V
ULN-3820A	—	—	—	—	—	X*	—	—	6-12 V
ULN-3823A	—	—	—	—	—	X	—	—	1.8-9 V
ULN-3839A	—	—	—	—	—	—	X	X	1.8-9 V
ULN-3840A	—	X	X	X	X	—	X	—	8.5-16 V
ULN-3841A	—	—	—	—	—	—	X	—	6.5-16 V
ULX-3842A	X	X	X	X	X	—	X	—	8.5-16 V
ULN-3859A	X	X	X	X	—	—	—	—	4-9 V
ULN-3862A	X	X	X	X	—	—	—	—	2-8 V
ULN-3883A	X	X	X	X	—	—	—	X	3-9 V

*CQUAM A-M Stereo Decoder.

ULN-3820A
CQUAM® AM STEREO DECODER

FEATURES

- Identical to MC13020P
- No Adjustments or Coils
- 25 HZ Pilot Presence Required to Decode Stereo
- PLL Detection for L − R
- True Full Wave Envelope Detection for L + R
- Pilot Acquisition Time 300 ms for Strong Signals
- Pilot Acquisition Time Extended for Noise Conditions to Prevent "Falsing"
- Internal Level Detector can be used as an AGC Source



This integrated circuit is a complete, one chip AM stereo decoding and pilot detection system. Unlike competitive devices, requiring numerous external functions to approach the correct decoding algorithm, this device provides a direct non-compromising one chip solution for the Motorola CQUAM AM stereo system. Full wave envelope detection is provided continuously for the L + R signal with the L − R decoded only in the presence of a valid stereo transmission. The device is packaged in an industry standard 20-pin plastic package.

This device, when combined with the Sprague ULN-3841A AM signal processing system or the Sprague ULN-3842A AM/FM signal processing system results in a very high performance complete AM stereo receiver.

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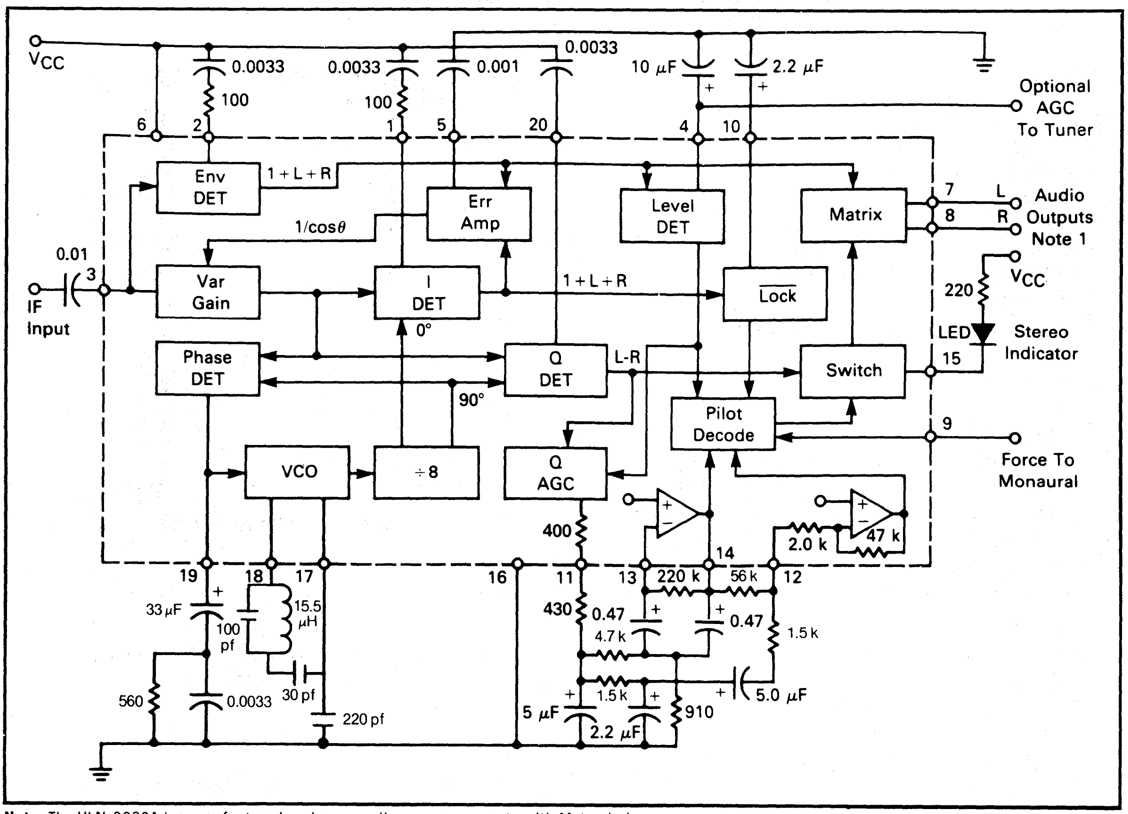
ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C)

Characteristic		Min.	Typ.	Max.	Unit
Power Supply Operating Range		6.0	8.0	12.0	Vdc
Supply Line Current Drain, Pin 6		—	30	—	mAdc
Input Signal Level, Unmodulated, Pin 3		—	200	350	mVRMS
Audio Output Level, 50% Modulation, L only or R only		—	220	—	mVRMS
Audio Output Level, 50% Modulation, Monaural		—	110	—	mVRMS
Output THD Monaural		—	0.5	—	%
Stereo		—	1.0	—	
Channel Separation		—	30	—	dB
Pilot Acquisition Time		—	300	—	ms
Input Impedance	R_{IN}	20	27	—	kΩ
	C_{IN}	—	6.0	—	pF
Output Impedance		—	100	150	Ω
Level Detector Filter Voltage, Pin 4	0 Signal	—	1.7	—	Vdc
	200 mVRMS Signal	—	2.5	—	
Lock Detector Filter Voltage, Pin 10	In Lock	—	4.3	—	Vdc
	Out of Lock	—	0.8	—	Vdc
Force to Monaural, Pin 9, Pull Down for Monaural Mode		—	<2.5	—	Vdc
		—	150	—	nA
Force to Monaural, Pin 9, Pull Up for Automatic Mode		—	>3.5	—	Vdc
		—	<1.0	—	nA

®CQUAM: Compatible QUadrature Amplitude Modulation, is a registered trademark of MOTOROLA INC.

APPLICATION AND BLOCK DIAGRAM



Note: The ULN-3820A is manufactured under cross-license agreements with Motorola Inc.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	Vdc
Pilot Lamp Current, Pin 15	—	50	mAdc
Operating Temperature	T_A	− 40 to + 85	°C
Storage Temperature	T_{stg}	− 65 to + 150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation	P_D	1.25	W
Derate above 25°C	—	10	mW/°C

The purchase of the Sprague CQUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Sprague or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

SECTION 7—VIDEO AND TELEVISION INTEGRATED CIRCUITS

†Complete information is provided in Data Book WR-503.

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SELECTION GUIDE TO VIDEO AND TELEVISION INTEGRATED CIRCUITS

Device Type	Sound	Sync.	Defl.
ULN-2260A	—	X	—
ULN-2270B/Q	—	—	X
ULN-2290B/Q	X	—	—
ULN-3702Z*	X	—	X

NOTE: Additional devices for use as sound channels may be found in Section 6. Audio amplifiers may be found in Section 8.

*See Section 8.

SECTION 8—AUDIO POWER AMPLIFIERS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

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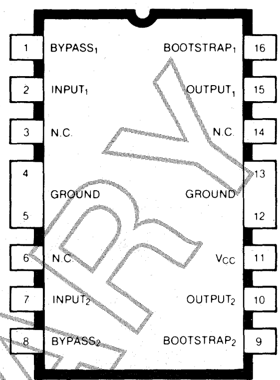
SELECTION GUIDE TO AUDIO POWER AMPLIFIERS

Device Type	Monophonic	Stereo	P_{OUT}	@	R_L	&	V_{CC}	Supply Range
ULN-2280B	X	—	2.5 W		8		18 V	8-26 V
			2.5 W		16		24 V	
ULN-2283B	X	—	350 mW		8		6 V	3-18 V
			1.2 W		16		12 V	
ULN-3701Z	X	—	5.2 W		4		14.4 V	8-18 V
			10 W		2		16 V	
ULN-3702Z	X	—	8 W		8		24 V	8-26 V
			12 W		4		24 V	
ULN-3703Z	X	—	7.5 W		3.2		14.4 V	8-18 V
			12 W		1.6		14.4 V	
ULN-3705M	X	—	220 mW		8		4.5 V	1.8-9 V
			240 mW		16		6 V	
			310 mW		32		9 V	
ULN-3782M	—	X	220 mW		8		3 V	1.8-9 V
			430 mW		8		6 V	
ULN-3783M	—	X	220 mW		8		4.5 V	.2.4-9 V
			240 mW		16		6 V	
			310 mW		32		9 V	
ULN-3784B	X	—	5 W		8		24 V	9-28 V
			4.8 W		16		28 V	
ULN-3793W	X	—	18 W		4		13.2 V	8-16 V
			11 W		8		13.2 V	

ULN-3750B
DUAL LOW-VOLTAGE POWER AMP

FEATURES

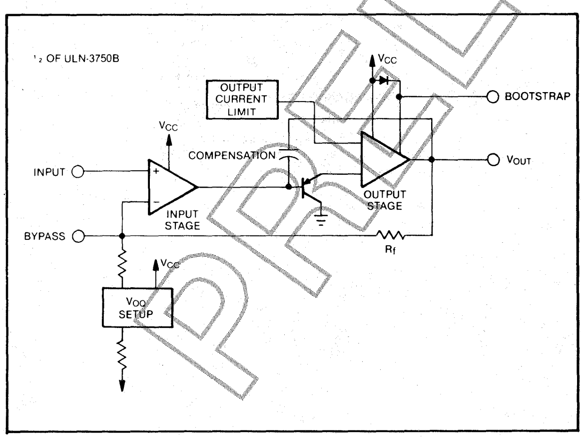
- Wide Operating Supply Range, 3 to 14 V
- Internal Gain Set to 40 dB—externally adjustable
- Bootstrap Operation Option
- Bridge Operation Option
- Internal Compensation
- Low Distortion, typ. 0.3%
- Internal Short Circuit Current Limit



The ULN-3750B is a dual channel 1 watt, low voltage audio amplifier that is a cost-effective solution for use in portable stereos, cassette players, table radios as well as portable communications equipment.

The voltage gain of each channel is set internally to 40 dB, with channel balance typically within 1 dB or less. The ULN-3750B is also internally compensated to a typical bandwidth of 70 kHz which acts to significantly eliminate AM interference radiated from the speaker wires while maintaining low distortion at high audio frequencies.

PARTIAL BLOCK DIAGRAM



The built-in output current limiting acts to protect the IC as well as external circuitry from shorted speaker load conditions while allowing high currents to be delivered to the loads without interference. It also has bootstrap capability and can be used in bridge applications.

The type ULN-3750B audio amplifier is supplied in an improved 16-lead dual in-line plastic-package with two webbed tabs. A copper alloy lead frame results in maximum power dissipation without the need for an external heat sink. Lead configuration is compatible with standard IC sockets or printed wiring board hole layouts.

APPLICATIONS

- Portable or Table Radios
- Battery Operated Equipment
- Portable Tape Recorders
- Walkie-Talkies

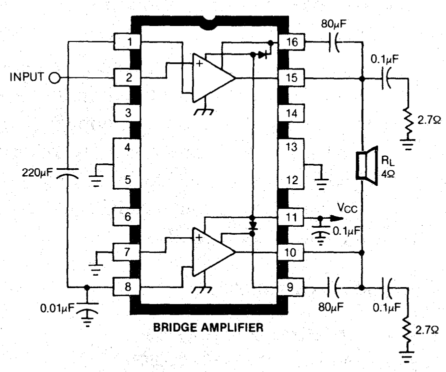
ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

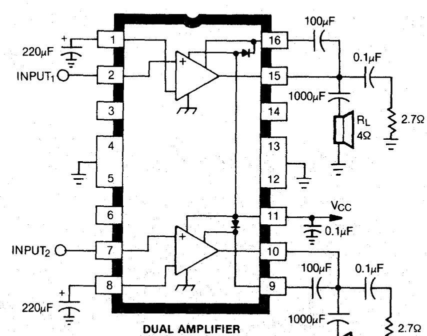
Supply Voltage, V_{CC} . . . . 14 V
Output Current, I_{OUT} . . . . 2.0 A
Operating Ambient Temperature Range, T_A . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 6 V, R_L = 4 Ω, f_{in} = 1 kHz, P_0 = 50 mW (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}		3.0	6.0	14	V
Supply Current	I_{CC}	V_{CC} = 6 V	—	14.0	—	mA
		V_{CC} = 12 V	—	20.0	—	mA
Voltage Gain	A_V		—	40.0	—	dB
Bandwidth	BW		—	70.0	—	kHz
Total Harmonic Distortion	THD		—	0.3	—	%
Output Noise		BW = 20 kHz	—	0.5	—	mVrms
Power Output (@ 10% THD)	P_0	V_{CC} = 6 V, R_L = 4 Ω	—	0.9	—	W
		V_{CC} = 9 V, R_L = 8 Ω	—	1.3	—	W
		V_{CC} = 12 V, R_L = 8 Ω	—	2.3	—	W
Current Limit			—	1.8	—	A
Channel Separation			—	55.0	—	dB
Channel Balance			—	1.0	—	dB

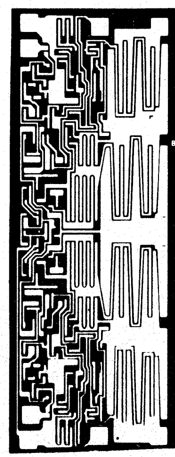
TYPICAL APPLICATION DIAGRAMS





NOTE: For non-bootstrapped operation simply connect V_{CC}(Pin 11) to pins 9 and 16, and eliminate 100 μF capacitors.

ULN-3783M
DUAL LOW-VOLTAGE AUDIO POWER AMPLIFIER



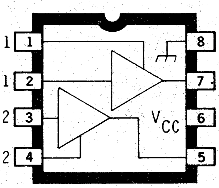
FEATURES

- Wide Operating Voltage Range
- Low Quiescent Current
- A-C Short-Circuit Protection
- Low External Parts Count
- Low Distortion
- 42 dB Voltage Gain
- Low Noise

SPECIFICALLY DESIGNED as a stereo headphone driver for portable radios and tape players, the Type ULN-3783M dual low-voltage audio power amplifier is well suited to use in all types of battery-operated equipment. Its small size and low external component count contribute to portability and low system cost. Its low-noise output and excellent channel separation provide for premium performance.

The dual audio amp operates with supply voltages as low as 2.4 V (at reduced volume) without significant increase in distortion. Weak batteries need no longer be a major concern. Class AB operation results in low quiescent current drain for maximum battery life.

Type ULN-3783B is supplied in a compact 8-pin dual in-line plastic package. A copper alloy lead frame allows maximum power dissipation without the need for an external heat sink.



DWG. NO. A-12,384

8

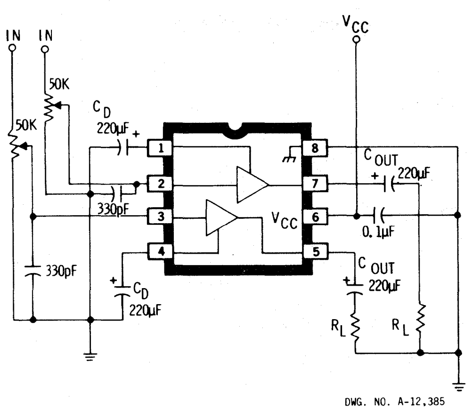
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 12 V
Package Power Dissipation, P_D . . . . See Graph
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

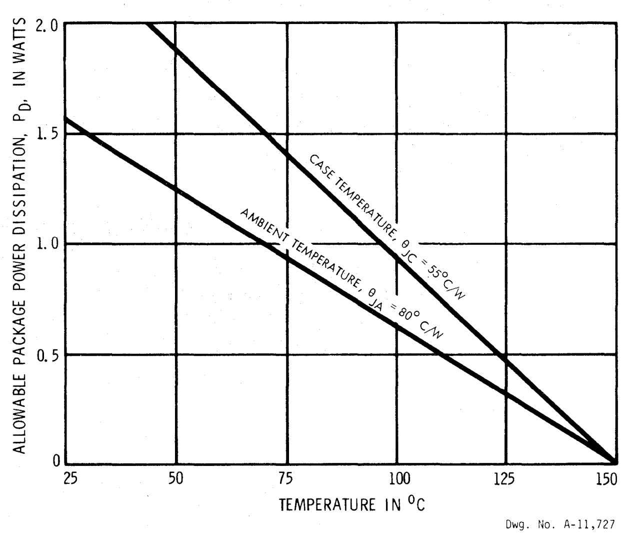
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = +6 V, R_L = 32 Ω, f_{in} = 400 Hz, one channel driven (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage Range	V_{CC}		2.4	6.0	9.0	V
Quiescent Supply Current	I_{CC}	V_{CC} = 4.5 V	—	13	—	mA
		V_{CC} = 6.0 V	—	15	25	mA
		V_{CC} = 9.0 V	—	20	—	mA
Voltage Gain	A_V		—	42	—	dB
Channel Balance	ΔA_V		—	±1	±3	dB
Separation			35	55	—	dB
Audio Power Output	P_{OUT}	R_L = 8 Ω, V_{CC} = 4.5 V, THD = 10%	—	220	—	mW
		R_L = 8 Ω, V_{CC} = 6.0 V, THD = 10%	250	430	—	mW
		R_L = 16 Ω, V_{CC} = 4.5 V, THD = 10%	—	125	—	mW
		R_L = 16 Ω, V_{CC} = 6.0 V, THD = 10%	150	240	—	mW
		R_L = 16 Ω, V_{CC} = 9.0 V, THD = 10%	—	600	—	mW
		R_L = 32 Ω, V_{CC} = 4.5 V, THD = 10%	—	60	—	mW
		R_L = 32 Ω, V_{CC} = 6.0 V, THD = 10%	85	110	—	mW
		R_L = 32 Ω, V_{CC} = 9.0 V, THD = 10%	—	310	—	mW
Distortion	THD	P_{OUT} = 50 mW, R_L = 32 Ω	—	0.4	1.0	%
		P_{OUT} = 50 mW, R_L = 16 Ω	—	0.5	—	%
Output Noise	V_{out}	Input shorted, BW = 80 kHz	—	225	—	μV
Input Resistance	R_{IN}	Pin 2 or Pin 3	—	250	—	kΩ
Power Supply Rejection	PSRR	C_D = 500 μF, f = 120 Hz	—	34	—	dB

TEST CIRCUIT AND TYPICAL APPLICATION



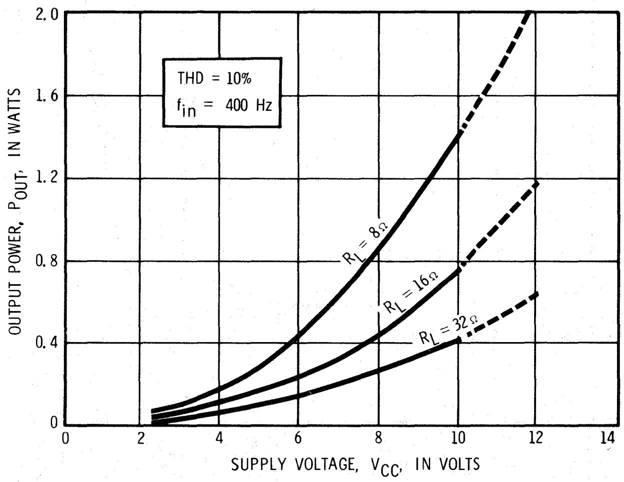
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



TYPICAL CHARACTERISTICS

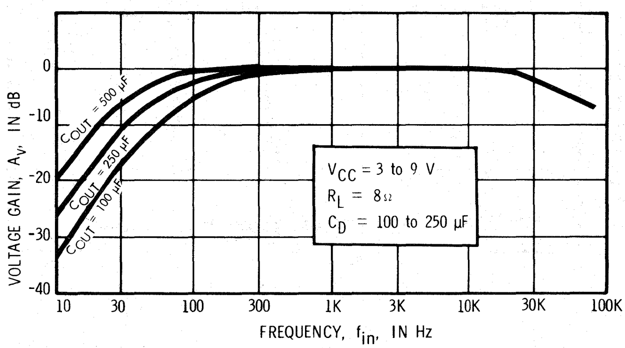
(One Channel Driven)

TYPICAL OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



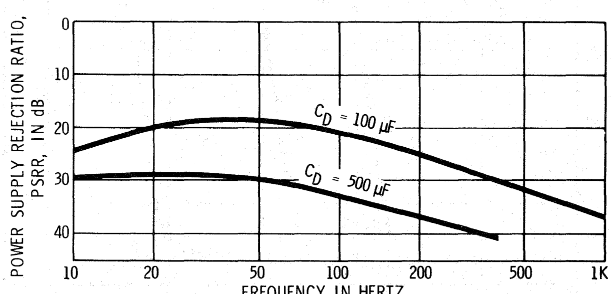
Dwg. No. A-11,720A

TYPICAL FREQUENCY RESPONSE



Dwg. No. A-11,717

POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREQUENCY



Dwg. No. A-10,838

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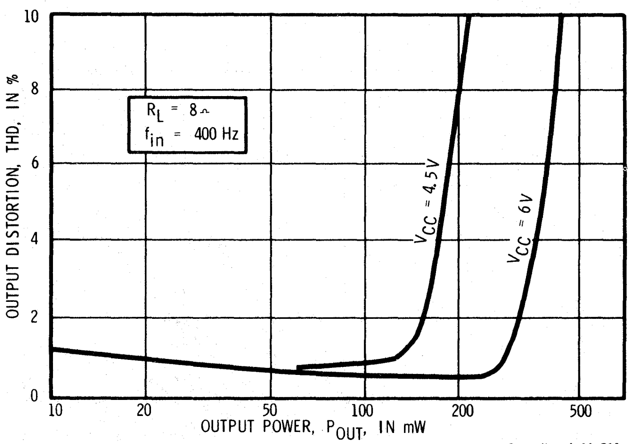
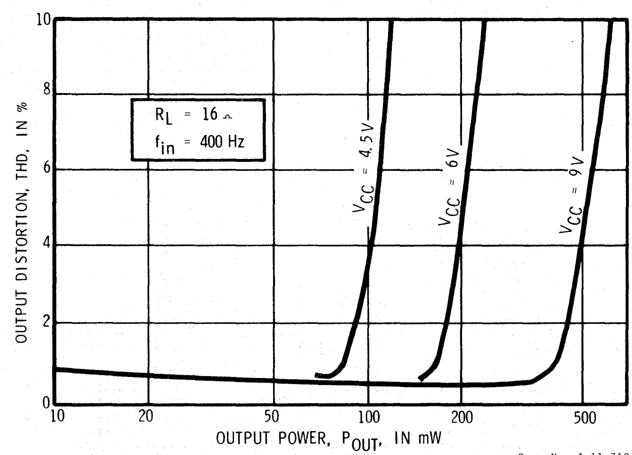
TYPICAL CHARACTERISTICS (Continued)



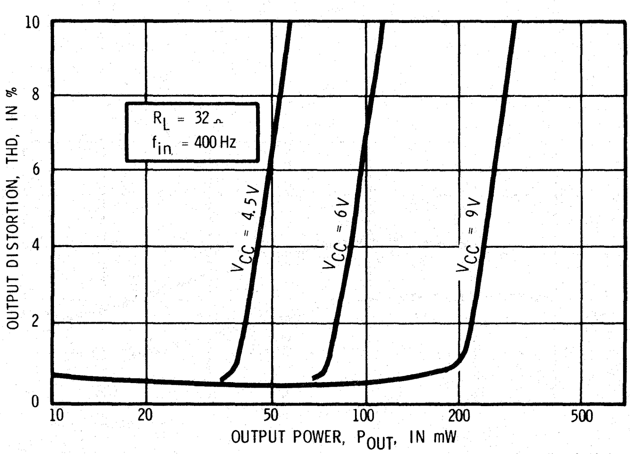
Dwg. No. A-11,718

TOTAL HARMONIC DISTORTION WITH 8 Ω LOAD



Dwg. No. A-11,719

TOTAL HARMONIC DISTORTION WITH 16 Ω LOAD

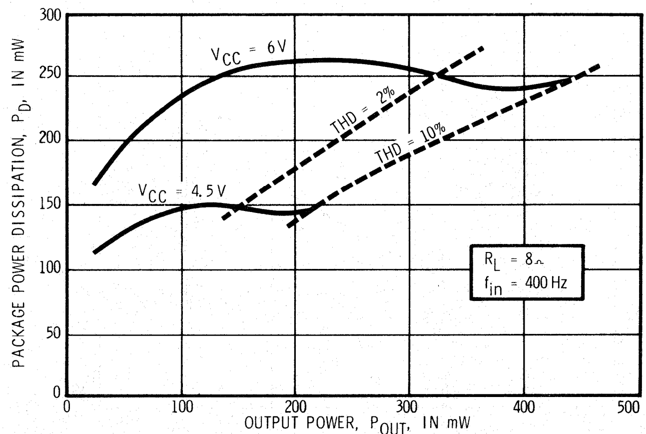


Dwg. No. A-11,990

TOTAL HARMONIC DISTORTION WITH 32 Ω LOAD

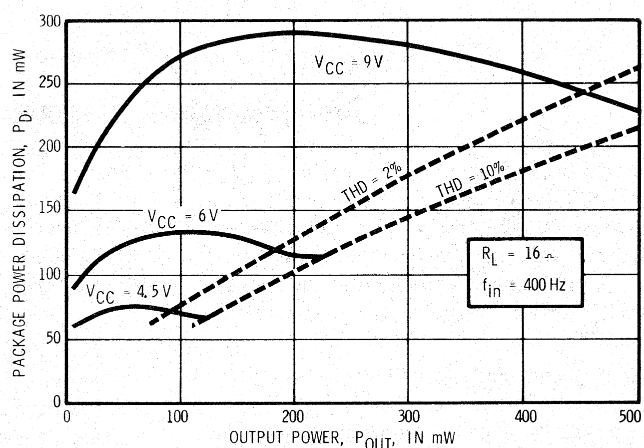
TYPICAL CHARACTERISTICS (Continued)

PACKAGE POWER DISSIPATION WITH 8 Ω LOAD



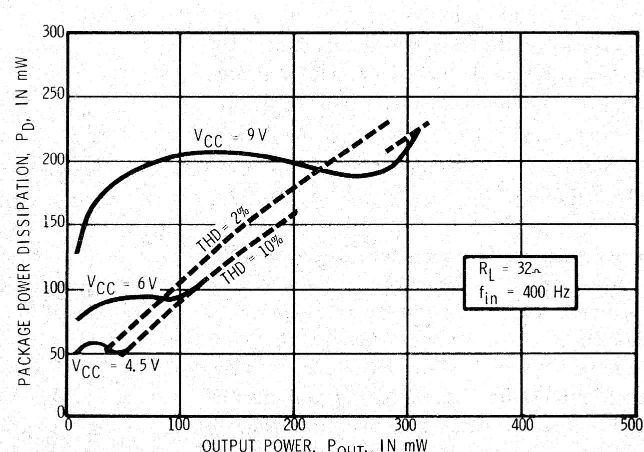
Dwg. No. A-11,721

PACKAGE POWER DISSIPATION WITH 16 Ω LOAD



Dwg. No. A-11,722A

PACKAGE POWER DISSIPATION WITH 32 Ω LOAD



Dwg. No. A-12,025A

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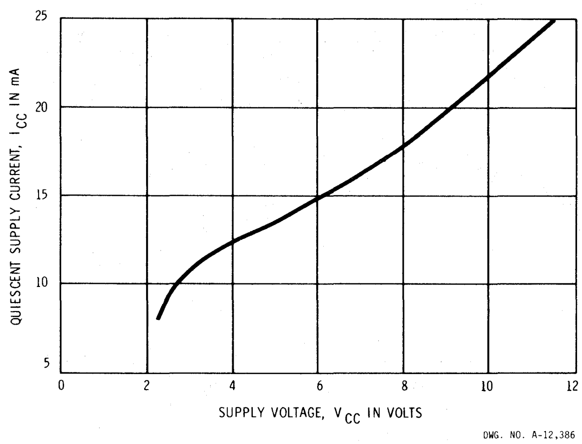
TYPICAL CHARACTERISTICS (Continued)



QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

APPLICATIONS INFORMATION

Selection of power-supply voltage and speaker impedance allows a designer to choose audio power levels within the allowable package power dissipation rating for any maximum operating temperature. No unique precautions are necessary when designing with this device. It is stable and a-c short-circuit immune.

External component selection for this low-power amplifier involves only two capacitors per channel —one for output coupling and one for feedback and ripple decoupling. The coupling capacitor value should be selected to provide the desired low-frequency cutoff with the chosen load impedance. The decoupling capacitor should be chosen for both low-frequency audio rolloff and supply-ripple rejection.

Ripple rejection is not practical to calculate due to the large number of mechanisms involved. A 500 μF capacitor achieves typically 34 dB rejection at 120 Hz.

The high gain and the high input impedance of the power amplifier recommend use of this device in many diverse applications. However, the input stage does have other characteristics that should be taken into account for best results. The input is referenced to ground for internal biasing and must be provided with a d-c path to ground. A current of typically 1 μA flows from the input through the volume control, producing an IR drop that is multiplied by the closed loop d-c gain of the amplifier and appears as an error in output centering. This recommends a value of 200 kΩ or less for the volume control; values of less than 100 kΩ are preferred.

The selection of amplifier load impedance involves more than just consideration of the desired power output. A low load impedance will produce the highest power output for any given supply voltage. Higher impedances will furnish significant reduction in harmonic distortion and improvement in overall repeatability of power output capacity.

Special steps toward minimizing tendencies towards instabilities of all types were taken in the design of this device. However, as with all high-gain circuits, care should be given to printed wiring board layout to avoid undesirable effects. Inputs and outputs should be well separated and should avoid common-mode impedances wherever possible. For best performance, grounds should be kept reasonably close to the low level input-signal grounds because their respective inputs represent inverting and non-inverting inputs to the amplifiers and exhibit about 40 dB of common-mode rejection. The high-level speaker ground should be connected directly to the power ground. The signal ground and the power ground should be interconnected at only one point.

SECTION 9—HALL EFFECT DEVICES

†Complete information is provided in Data Book WR-503.

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Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

SELECTION GUIDE TO HALL EFFECT DEVICES

Device Type	Switch Points (Gauss)		Outputs
UGN-3013T/U	225	300	1
UGN/UGS-3019T/U	300	420	1
UGN/UGS-3020T/U	165	220	1
UGN/UGS-3030T/U	110	160	1
UGN-3035U	− 25	+ 25	1
UGN-3040T/U	100	150	1
UGN/UGS-3075T/U	−100	+100	1
UGN/UGS-3076T/U	−100	+100	1
UGN-3201M	300	450	2
UGN-3203M	100	235	2
UGN-3220S	160	220	2
UGN-3501M	Linear		Push-Pull
UGN-3501T/U	Linear		1
UGN/UGS-3503U	Linear		1
UGN-3604M	Linear		Push-Pull
UGN-3605M	Linear		Push-Pull

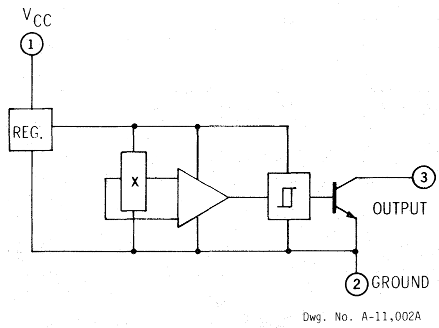
Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

UGN-3035U HALL EFFECT ASSEMBLY —Magnetically Biased Bipolar Digital Latch

FEATURES

- Extreme Sensitivity
- For Use with Multipole Ring Magnets
- High Reliability—No Moving Parts
- Small Size
- Output Compatible with All Digital Logic Families
- Symmetrical Output



FUNCTIONAL BLOCK DIAGRAM

DEVELOPED for use with multipole ring magnets in applications requiring extreme sensitivity to magnetic field reversal, the Type UGN-3035U Hall Effect latch assembly provides rugged, reliable interface between electromechanical equipment and bipolar or MOS logic circuits at switching frequencies of up to 100 kHz.

The bipolar output of the magnetically biased device saturates when the Hall cell is exposed to a magnetic flux density greater than the ON threshold (25 G typical, 50 G maximum). The output transistor remains in the ON state until magnetic field reversal exposes the Hall cell to a magnetic flux density below the OFF threshold (−25 G typical, −50 G minimum). Because the operating state switches only with magnetic field reversal, and not merely with a change in its strength, the integrated circuit qualifies as a true Hall Effect latch.

Each circuit consists of a voltage regulator, Hall voltage generator, signal amplifier, Schmitt trigger circuit, and an open-collector output driver on a single silicon chip. The on-board regulator permits operation over a wide range of supply voltages. The components of the monolithic circuit are carefully matched to provide accurate operation with wide variations in temperature.

The Type UGN-3035U assembly is a single-output Hall Effect digital latch in a three-pin plastic "U" package with a bias magnet (0.065" or 1.65 mm long) epoxy-glued to its rear surface.

Note that the operational symmetry of this sensitive device will be lost if the latch is exposed to magnetic flux density greater than 500 Gauss. Symmetry can also be affected by ferrous materials near the assembly.

9

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC}	25 V
Magnetic Flux Density, B	500 G
Output OFF Voltage	25 V
Output ON Current, I_{SINK}	25 mA
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C

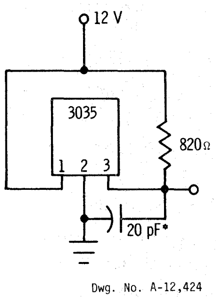
*Selected devices are available with a maximum T_A rating of +150°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operate Point*	B_{OP}		—	+25	+50	Gauss
Release Point*	B_{RP}		−50	−25	—	Gauss
Hysteresis*	B_H		20	50	—	Gauss
Output Saturation Voltage	V_{SAT}	$B \geq +50$ Gauss, $I_{SINK} = 15$ mA	—	85	400	mV
Output Leakage Current	I_{OFF}	$B \leq -50$ Gauss, $V_{OUT} = 24$ V	—	0.05	10	μA
Supply Current	I_{CC}	$B \leq 50$ Gauss, $V_{CC} = 4.5$ V, Output open	—	2.3	5.0	mA
		$B \leq 50$ Gauss, $V_{CC} = 24$ V, Output open	—	3.0	5.0	mA
Output Rise Time	t_r	$V_{CC} = 12$ V, $R_L = 820\Omega$, $C_L = 20$ pF	—	150	—	ns
Output Fall Time	t_f	$V_{CC} = 12$ V, $R_L = 820\Omega$, $C_L = 20$ pF	—	400	—	ns

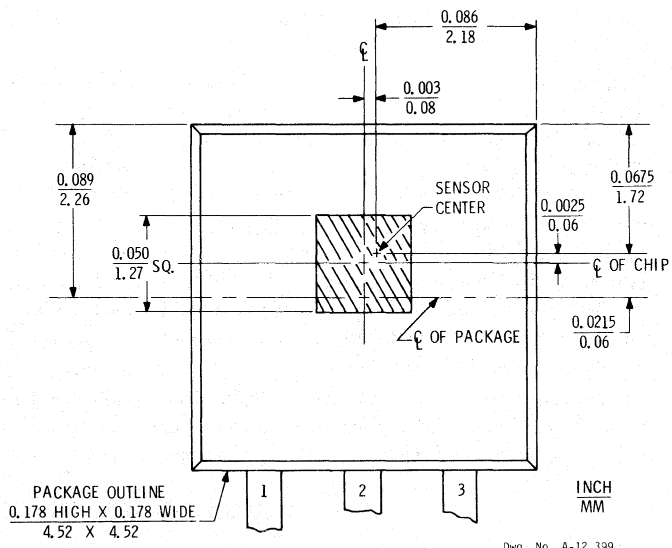
*Magnetic flux density is measured at most sensitive area of device located 0.016" ±0.002" (0.41 mm ±0.05 mm) below the branded face of the package.

TEST CIRCUIT



*Includes probe and test fixture capacitance.

SENSOR-CENTER LOCATION



OPERATION

Under power-up conditions, and in the absence of an externally applied magnetic field, the output transistor of most UGN-3035U assemblies is ON and capable of sinking 25 mA of current. This is, however, a formally ambiguous state and should be treated as such.

In normal operation, the output transistor turns ON as the strength of the magnetic field perpendicular to the surface of the chip reaches the Operate Point. The output transistor switches OFF as magnetic field reversal takes magnetic flux density to the Release Point.

Note that the device latches: That is, a south pole of sufficient strength, presented to the branded face of the assembly, turns the device ON. Removal of the south pole leaves the device ON. The presence of a north magnetic pole of sufficient strength is required to turn the switch OFF.

The UGN-3035U digital latch is primarily intended for operation with a multipole ring magnet, as shown in Figure 1. Other methods of operation are possible.

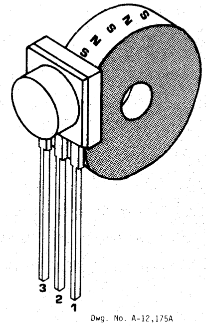
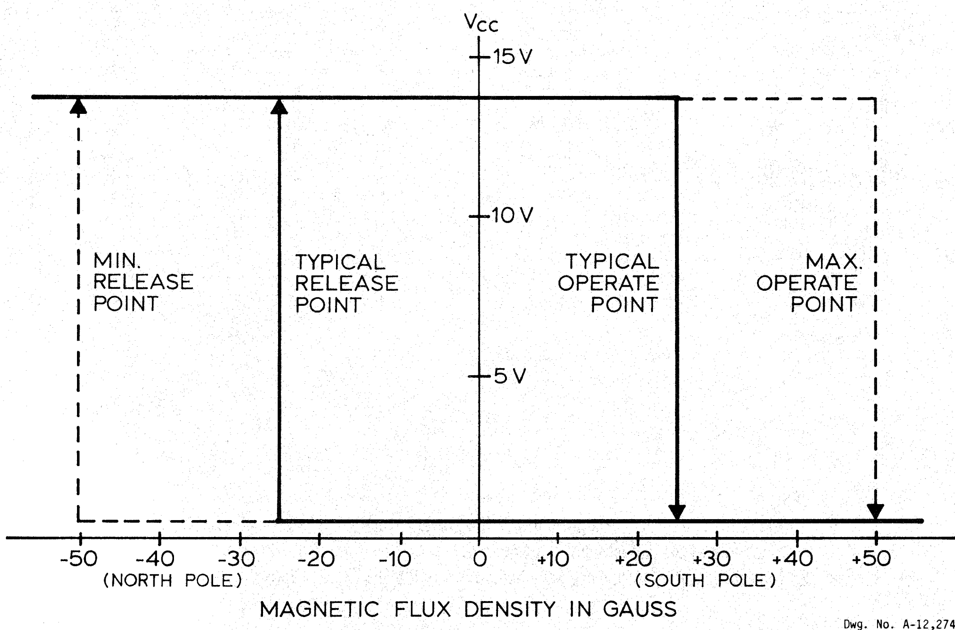


Figure 1

With the branded surface of the assembly facing you, and with pins pointing down, "U" package pinouts are: 1—V_{CC}, 2—Ground, 3—V_{OUT}.

The magnetic flux densities indicated in the operating-points graph below are measured at the active area of the device, which is 0.016 in. (0.41 mm) below the branded surface of the "U" package.

TYPICAL TRANSFER CHARACTERISTICS AT T_A = +25°C

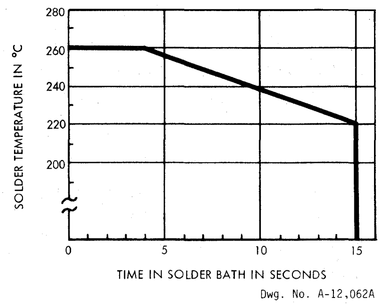


9

GUIDE TO INSTALLATION

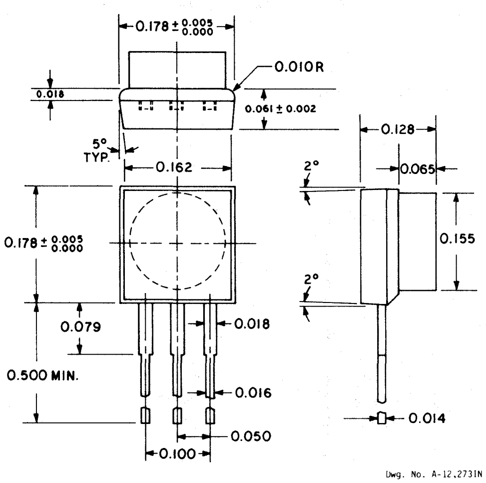
1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package. Use of epoxy glue is recommended. Other types may deform the epoxy package.

2. To prevent permanent damage to the Hall cell, heat-sink the leads during hand-soldering. Recommended maximum conditions for wave soldering are shown in the graph at right. Solder flow should be no closer than 0.125″ (3.18 mm) to the epoxy package.

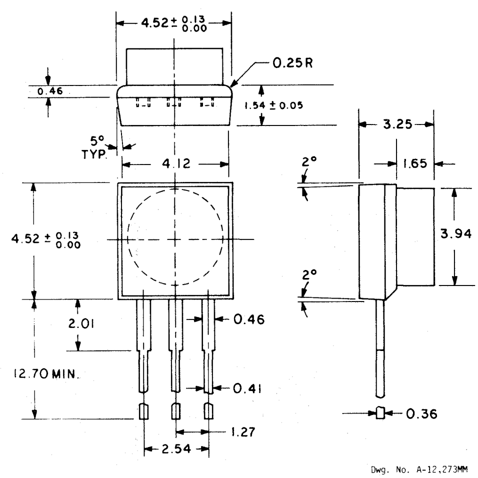


'U' PACKAGE/MAGNET ASSEMBLY

DIMENSIONS IN INCHES



DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm

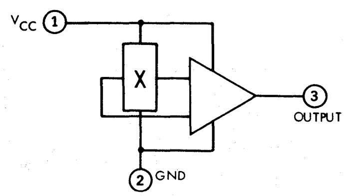


NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Tolerances, unless otherwise specified, are ± 0.005″ (0.13 mm) and ± ½°.

UGN-3503U AND UGS-3503U RATIOMETRIC, LINEAR HALL EFFECT SENSORS

FEATURES

- Extremely Sensitive
- Flat Response to 23 kHz
- Low-Noise Output
- 4.5 V to 6 V Operation
- Magnetically Optimized Package



Dwg. No. A-12,538

FUNCTIONAL BLOCK DIAGRAM

TYPE UGN-3503U AND UGS-3503U Hall Effect sensors accurately track extremely small changes in magnetic flux density—changes generally too small to operate Hall Effect switches.

As motion detectors, gear tooth sensors, and proximity detectors, they are magnetically driven mirrors of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while providing isolation from contaminated and electrically noisy environments.

Each Hall Effect integrated circuit includes a Hall sensing element, linear amplifier, and emitter-follower output stage. Problems associated with handling tiny analog signals are minimized by having the Hall cell and amplifier on a single chip.

The sensors are supplied in a three-pin plastic package only 61 mils (1.54 mm) thick. Type UGN-3503U is rated for continuous operation over the temperature range of −20°C to +85°C. Type UGS-3503U operates over an extended temperature range of −40°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 8 V
Magnetic Flux Density, B . . . . Unlimited
Operating Temperature Range, T_A
UGN-3503U . . . . −20°C to +85°C
UGS-3503U . . . . −40°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

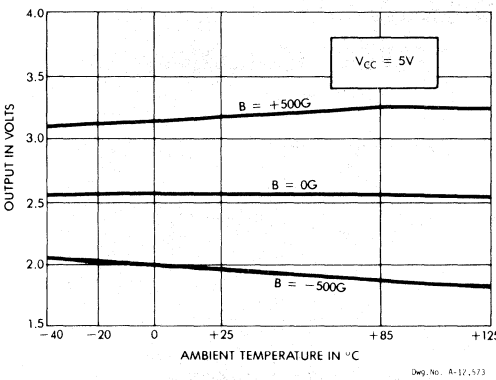
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 5 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage	V_{CC}		4.5	—	6.0	V
Supply Current	I_{CC}		—	9.0	14	mA
Quiescent Output Voltage	V_{OUT}	B = 0G	2.25	2.50	2.75	V
Sensitivity	ΔV_{OUT}	B = 0G to ±900G	0.75	1.30	1.72	mV/G
Bandwidth (−3 dB)	BW		—	23	—	kHz
Broadband Output Noise	V_{out}	BW = 10 Hz to 10 kHz	—	90	—	μV
Output Resistance	R_{OUT}		—	50	—	Ω

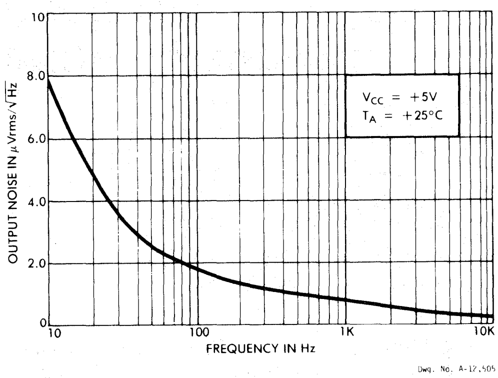
All output-voltage measurements are made with a voltmeter having an input impedance of at least 10 kΩ.
Magnetic flux density is measured at most sensitive area of device located 0.016″ ±0.002″ (0.41 mm ±0.05 mm) below the branded face of the 'U' package.

9

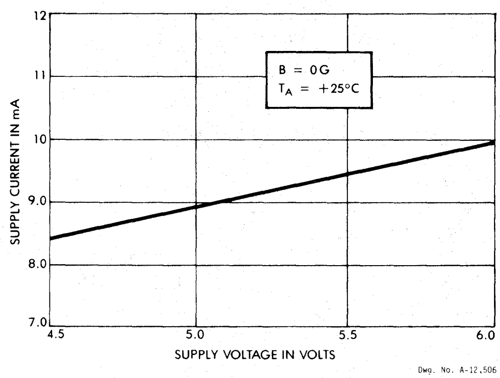
OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



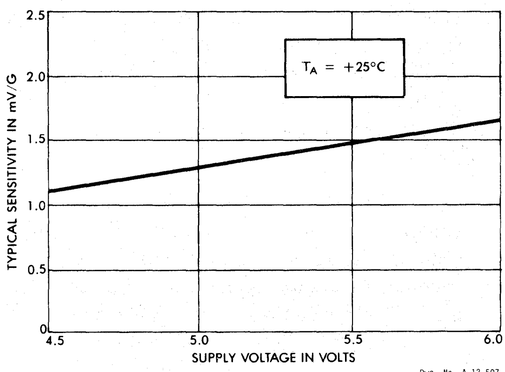
OUTPUT NOISE AS A FUNCTION OF FREQUENCY



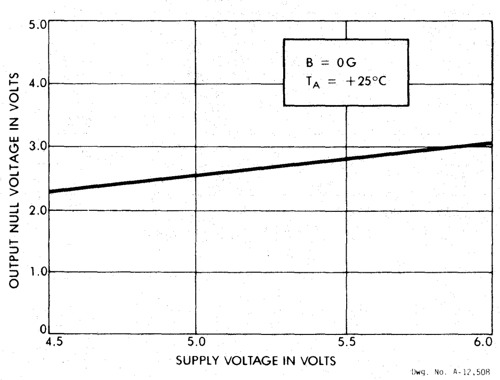
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



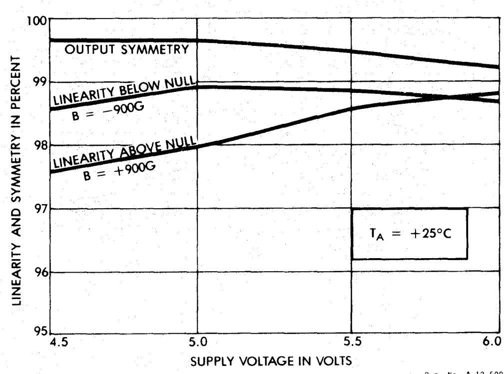
DEVICE SENSITIVITY AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT NULL VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



LINEARITY AND SYMMETRY AS A FUNCTION OF SUPPLY VOLTAGE



OPERATION

The output null voltage (see preceding graph) is nominally one-half the supply voltage. A south magnetic pole, presented to the branded face of the Hall Effect sensor, will drive the ouput higher than the null voltage level. A north magnetic pole will drive the output below the null level.

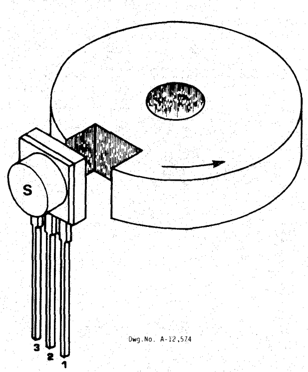
In operation, instantaneous and proportional output-voltage levels are dependent on magnetic flux density at the most sensitive area of the device. Greatest sensitivity is obtained with a supply voltage of 6 V, but at the cost of increased supply current and a slight loss of output symmetry. The sensor's output is usually capacitively coupled to an amplifier that boosts the output above the millivolt level.

In two applications shown below, a permanent bias magnet is attached with epoxy glue to the back of the epoxy package. The presence of ferrous material at the face of the package acts as a flux concentrator.

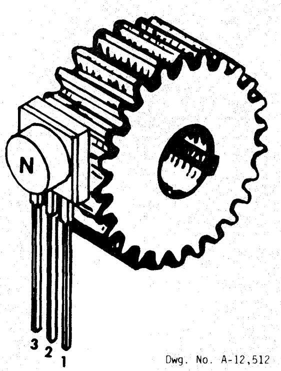
The south pole of a magnet is attached to the back of the package if the Hall Effect IC is to sense the presence of ferrous material. The north pole of a magnet is attached to the back surface if the integrated circuit is to sense the absence of ferrous material.

Calibrated linear Hall devices, which can be used to determine the actual flux density presented to the Type 3503 sensor in a particular application, are available from Hall Effect Applications Engineering, Sprague Electric Co., Concord, N.H.

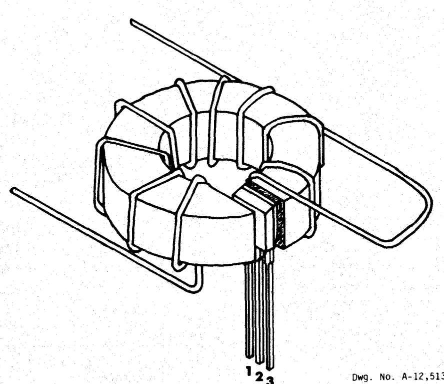
NOTCH SENSOR



GEAR TOOTH SENSOR



CURRENT MONITOR



GUIDE TO INSTALLATION

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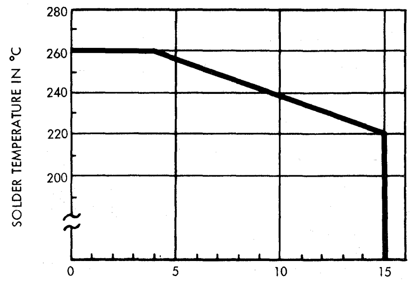
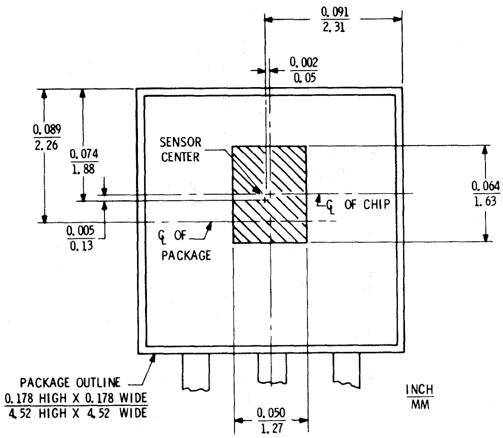


Dwg. No. A-12,062B

SENSOR-CENTER LOCATION



Dwg. No. A-12,626

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

SECTION 10A—POWER SUPPLY CONTROL CIRCUITS

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

SECTION 10B—TRANSISTOR ARRAYS AND MISCELLANEOUS DEVICES

†Complete information is provided in Data Book WR-503.
*New product. Contact factory for detailed information.

Additional information on the
ULN-3310D/T and ULN-3330D/T/Y
Optoelectronic Switches is available from:

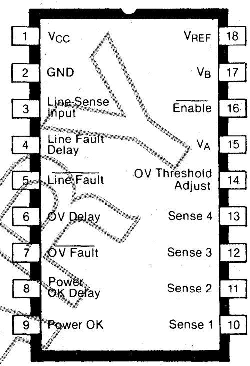
Sprague Electric Company
Sensor Division
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

10

ULN-8130A
LINE AND QUAD VOLTAGE MONITOR

FEATURES

- 10 to 35 Volts Operation
- Low Standby Current
- Precision 2.5 Volt 1% Trimmed Reference
- Monitors Four Separate D.C. Supply Levels
- UV Threshold Fixed at V_{REF}
- Independently Programmable 0 V Threshold
- Separate UV Comparators for Precision Sensing
- Line or Switch Sense Input for Early Failure Warning
- Unique Pull Up Clamped Outputs Drive LED's or Logic
- Individual Programmable Output Delays
- Input Supply UV Lockout Prevents False Outputs

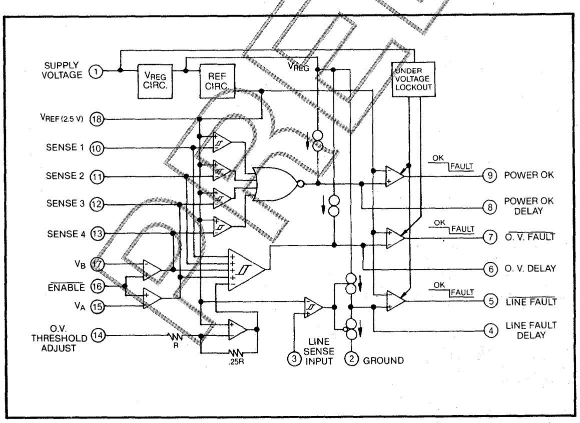


The ULN-8130A is a power fault monitor capable of monitoring four D.C. voltages for both under and over voltages. Two of the four inputs are dedicated to monitor only positive voltages. The other two inputs can either be both positive or negative or combined to monitor one negative voltage. The only combination that cannot be monitored is three positive and one negative (the 20 pin 8131 is capable of this combination). The circuit of the 8130 allows easy programming of over voltage threshold, which is a percentage above the 2.5 Volt reference. An output delay section can be controlled externally by adding a capacitor from the 0 V delay pin to ground.

The 0 V delay is initiated by one or more of the four sense inputs rising above the 0 V trip point. The output of the power OK section will remain high as long as the power input is above the preset level. The programmability of the line fault delay, 0 V delay, and power OK delay are independent of each other. The line monitor will accept a DC voltage proportional to either the high voltage VNR or the AC line. The value of capacitor used for the line fault delay should be selected to provide suitable detection of fault conditions.

The device is packaged in an industry standard 18-pin plastic package.

FUNCTIONAL BLOCK DIAGRAM



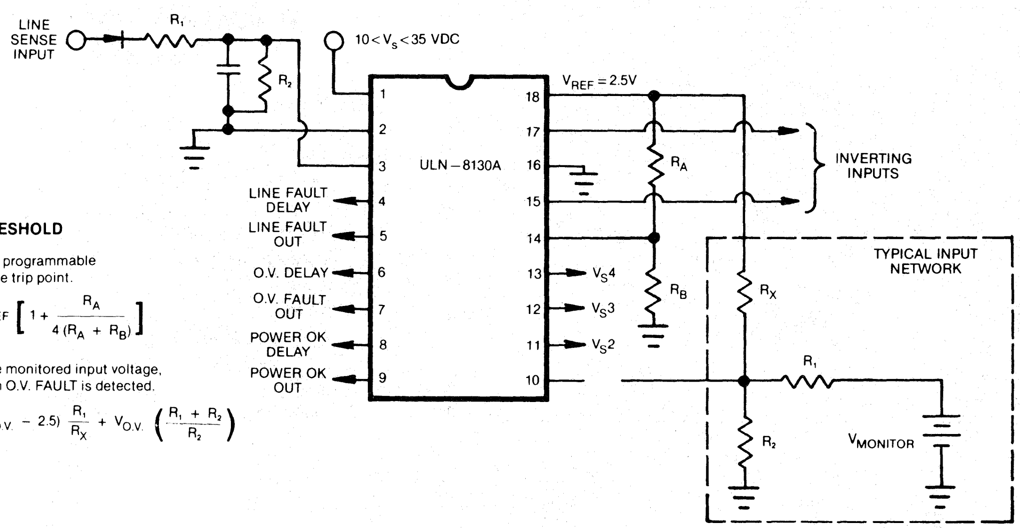
ABSOLUTE MAXIMUM RATINGS
at $T_A = 25°C$

Supply Voltage, V_{CC}	40 V
Operating Temperature, T_A	−40 to +85°C
Storage Temperature, T_S	−65°C to +150°C
Junction Temperature, $T_{J(MAX)}$	150°C
Power Dissipation, P_D	1,000 mW

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, T_A = 25°C)

Characteristics	Symbol	Limits		Units
		Min.	Max.	
Quiescent Current (V_{in} = 35 V)	QI		15	mA
Usable V_{in}	V_{CC}	10	35	V
Reference Voltage	V_{REF}	2.47	2.53	V
Load Regulation	LDR		20	mV
Line Regulation	LNR		10	mV
Ripple Rejection	RR	60		dB
Input Bias Current for V1, V2, V3, V4 and Line Monitor	IB1		6.0	μA
Input Bias Current for VA, VB	IB2		2.0	μA
Line Monitor Trip Threshold (V_{CC} = 15 V)		2.46	2.54	V
Under Voltage Lockout Enable		8.5		V
Under Voltage Lockout Disable			10	V
Under Voltage Trip Points V1, V2, V3, V4	VU 1 VU 2	2.47 2.441	2.53 2.521	V V
U. V. Trip Hysteresis		10	25	mV
Over Voltage Trip Points V1, V2, V3, V4 (V_{14} = 0 V)	VO 1	3.08	3.17	V
O. V. Trip Hysteresis		10	25	mV
VOL for Power OK and Power Fail	VOL		0.4	V
VOL for Over Voltage	VOL		0.4	V
VOH for Power OK and Power Fail	VOH	4.0	5.25	V
VCE Maximum for Over Voltage Open Collector Output	VCE_{max}		35	V
Under Voltage Delay Current Source	IDS	35	75	μA
Line Fault Delay Source Sink	IDCS – IDCS	160 3.2	240 4.8	μA mA
Over Voltage Delay Current Source	IDS	160	240	μA

TYPICAL APPLICATION DIAGRAM



O.V. THRESHOLD

$V_{O.V.}$ is the programmable over voltage trip point.

$$V_{O.V.} = V_{REF}\left[1 + \frac{R_A}{4(R_A + R_B)}\right]$$

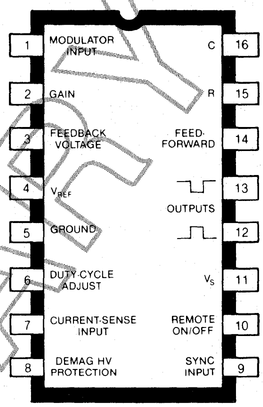
V_{MAX} is the monitored input voltage, at which an O.V. FAULT is detected.

$$V_{MAX} = (V_{O.V.} - 2.5)\frac{R_1}{R_X} + V_{O.V.}\left(\frac{R_1 + R_2}{R_2}\right)$$

SERIES 8163
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUITS

FEATURES

- Supply Range of 4.5 to 15 V
- High Frequency Range of Sawtooth Generator
- Improved Feed-forward Control (5:1 Range)
- Accurate Current Sense Thresholds (5%)
- Band-gap Voltage Reference (3 V ±1%)
- Improved Stability Over Temperature
- Internal Voltage Regulator
- Current Limiting
- Pulse-width Modulator
- External Synchronization
- Loop-fault Protection
- Demagnetization/High-voltage Protection
- Remote ON/OFF Switching

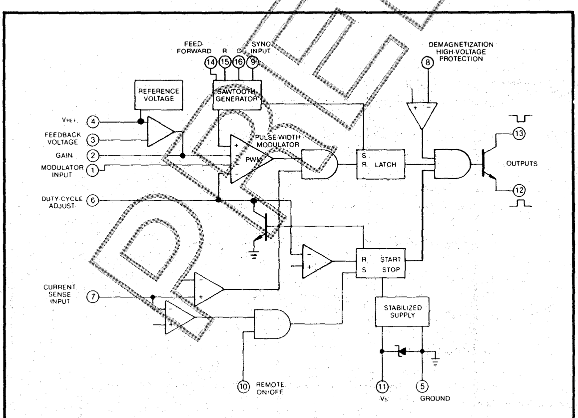


Featuring the basic architecture of 8160 series, the 8163 series is an improved switched-mode power supply control circuit. The ULN-8163A, ULN-8163R and ULS-8163A each has a temperature-compensated reference control, an internal error amplifier, a high frequency range sawtooth waveform generator, a pulse-width modulator, an output driver, and a variety of protection circuitry.

Type ULN-8163A is supplied in a 16-pin dual in-line package with a copper lead frame for enhanced power dissipation ratings for operation over a temperature range of 0°C to +70°C.

Types ULN-8163R and ULS-8163R are furnished in 16-pin hermetically sealed glass/ceramic packages for withstanding severe environmental contamination. ULS-8163R can be used in extended temperature ranges of −55°C to +125°C for military and aerospace applications.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Supply Voltage, V_S	(See Note)
Supply Current, I_{REG}	30 mA
Output Current, I_O	200 mA
Package Power Dissipation, P_D	
(ULN-8163A)	2.1 W*
(ULN-8163R/ULS-8163R)	1.7 W*
Operating Temperature Range, T_A	
(ULN-8163A/R)	0°C to +70°C
(ULS-8163R)	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate linearity to 0 W at T_A = +150°C.
NOTE: Maximum allowable supply voltage is dependent on value of external current limiting resistor: 18 V @ 0 Ω.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = 12 V (unless otherwise specified)

Characteristic	Test Pin	Applicable Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Clamp Voltage	11	I_S = 10 mA; V_5, V_{12}, V_{16} = 0 V	14	—	18	V
		I_S = 30 mA; V_5, V_{12}, V_{16} = 0 V	14	—	18	V
Supply Current	11	V_S = 12 V; V_5, V_{12}, V_{16} = 0 V	—	3.5	5.0	mA
REFERENCE SECTION						
Internal Reference, V_{REF}		T_A = +25°C	2.97	3.0	3.03	V
		Over Operating Temp. Range	2.95	—	3.06	V
Temperature Coefficient of V_{REF}			—	—	±100	ppm/°C
OSCILLATOR SECTION						
Oscillator Frequency Range	15, 16		50	—	300K	Hz
Initial Oscillator Accuracy	15, 16	f = 40 KHz	—	—	5.0	%
Duty-Cycle Range	15, 16	f = 40 KHz	—	—	97	%
HOUSEKEEPING FUNCTIONS						
Duty-Cycle Control	6	V_6 = 2.0 V	47	50	53	%
PWM Input Current	6	Over Operating Temp. Range	—	—	5.0	μA
Protection Thresholds @ T_A = +25°C	11	Low Supply-Voltage Protection	3.8	—	—	V
		Low Supply-Voltage Hysteresis	450	—	550	mV
	8	Demagnetization/High-Voltage Protection	555	600	650	mV
Sense-Input Current	3	Over Operating Temp. Range	—	—	−0.5	μA
Input Current	8	T_A = +25°C, V_8 = 0 V	—	—	2.0	μA
		Over Operating Temp. Range	—	—	4.0	μA
Feed-Forward Control	14	V_{14} = 2 V, percent of original duty cycle	30	40	50	%
Input Current	14	T_A = +25°C	—	0.2	2.0	μA
		Over Operating Temp. Range	—	—	4.0	μA
CURRENT LIMITING						
Input Current	7	V_7 = 250 mV, T_A = +25°C	—	—	4.0	μA
		V_7 = 250 mV, over operating temp. range	—	—	8.0	μA
Inhibit Delay	7	One pulse, 20% overdrive @ I_0 = 40 mA	—	—	800	nS
Trip Levels	7	Shutdown/slow start	570	600	630	mV
		Current limit	455	480	505	mV
		Shutdown/Current limit ratio	—	1.25	—	—
OUTPUT STAGE						
Output Current	13		—	—	100	mA
Output-Saturation Voltage	13	$V_{CE(sat)}$ @ I_C = 100 mA	—	—	1.5	V
Output Compliance Voltage	12	V_{11} = V_{13}	—	—	V_{11-3}	—

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ORDERING INFORMATION

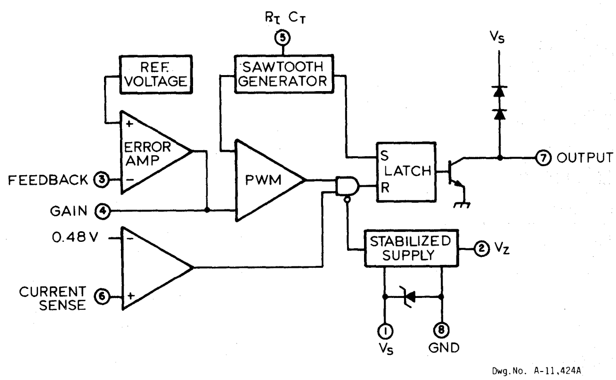
Sprague Part Number	Signetics Corp.* Part Number	Operating Temperature Range	Package
ULN-8163A	NE5563N	0°C to +70°C	Plastic
ULN-8163R	NE5563F	0°C to +70°C	Cer-DIP
ULS-8163R	SE5563F	−55°C to +125°C	Cer-DIP

*These devices are manufactured under a cross-license with Signetics Corp. (a subsidiary of U.S. Philips Corp.)

ULN-8168M (NE5568N)
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

FEATURES

- Stabilized Power Supply
- Current Limiting
- Temperature-Compensated (±2%) Reference Source
- Sawtooth Generator
- Pulse-Width Modulator
- Double-Pulse Protection
- Applications in:
  —Switched-Mode Power Supplies
  —Motor Controller-Inverters
  —D-C/D-C Converters



FUNCTIONAL BLOCK DIAGRAM

DESIGNED AS A CONTROLLER for low-cost switched-mode power supplies, the Type ULN-8168M integrated circuit includes a ±2% temperature-compensated reference source.

This SMPS controller is ideally suited to applications requiring limited housekeeping functions. It has its own internal Zener reference, sawtooth waveform generator, error amplifier, pulse-width modulator, output driver, current-sensing, and low-voltage protection.

Type ULN-8168M is supplied in an 8-pin dual in-line plastic package with a copper lead frame that gives it enhanced power dissipation ratings. It is rated for continuous operation over the temperature range of 0°C to +70°C. Similar devices are available for operation over extended temperature ranges.

Type ULN-8168M is normally marked with the original-source part number, NE5568N; however, the Sprague part number should be used in orders and correspondence.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_S (Voltage-Fed)	18 V
Supply Current, I_S (Current-Fed)	30 mA
Output Current, I_O	40 mA
Output Duty Cycle	98%
Package Power Dissipation, P_D	1.5 W*
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate at the rate of 12.5 mW/°C above T_A = +25°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 12 V (unless otherwise noted)

Characteristic	Test Pin	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Clamp Voltage	1	I_S = 10 mA, Current-fed	19	—	24	V
		I_S = 30 mA, Current-fed	20	—	30	V
Internal Reference, V_{REF}	—	Over operating temperature range	3.66	—	3.87	V
	—	T_A = +25°C	3.69	3.75	3.84	V
Temperature Coefficient of V_{REF}	—		—	±100	—	ppm/°C
Zener Reference, V_Z	2	I_2 = −7.0 mA	7.8	8.4	9.0	V
Temperature Coefficient of V_Z	2		—	±150	—	ppm/°C
Oscillator Frequency Range	5	Over operating temperature range	50	—	100k	Hz
Initial Oscillator Accuracy	5		—	2.0	—	%
Duty-Cycle Range	5	f_0 = 20 kHz	0	—	98	%
Input Current	6	V_6 = 250 mV, Over operating temperature range	—	—	−20	μA
	6	V_6 = 250 mV, T_A = +25°C	—	−2.0	−10	μA
Inhibit Delay	6	Single pulse, 20% overdrive at I_0 = 20 mA	—	700	800	ns
Trip Level	6	Current limit	400	520	600	mV
Error-Amplifier Gain	3-4	Open loop	—	60	—	dB
Error-Amplifier Feedback Resistance	4		10	—	—	kΩ
Small-Signal Bandwidth	3-4		—	3.0	—	MHz
Output-Voltage Swing	4	Positive limit	6.2	—	—	V
	4	Negative limit	—	—	0.6	V
Output Current	7	Over operating temperature range	20	—	—	mA
Output-Saturation Voltage	7	I_C = 20 mA	—	—	0.5	V
Supply Current	1	I_Z = 0, Over operating temp. range, Voltage-fed	—	—	15	mA
	1	I_Z = 0, T_A = +25°C, Voltage-fed	—	—	9.0	mA

ORDERING INFORMATION

Original Source* Part Number	Sprague Part Number	Operating Temperature Range	Package
NE5568N	ULN-8168M	0°C to +70°C	Plastic

* These devices are manufactured in accordance with a cross-license with Signetics Corp. (a subsidiary of U.S. Philips Corp.).

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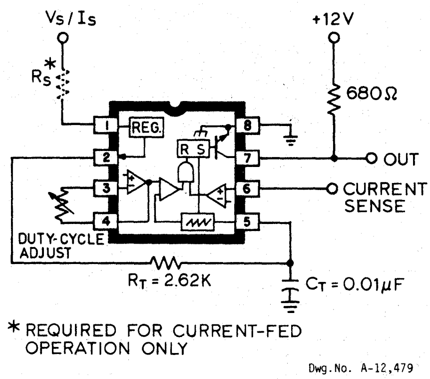
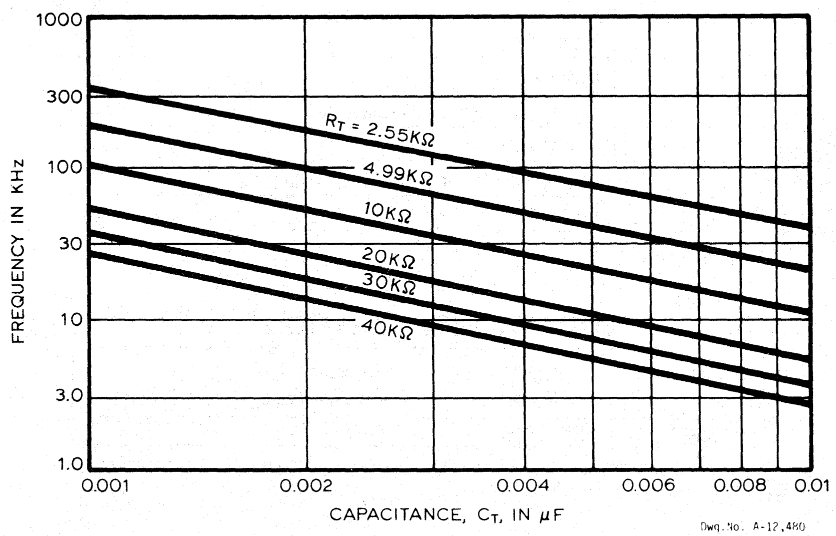
TEST CIRCUIT



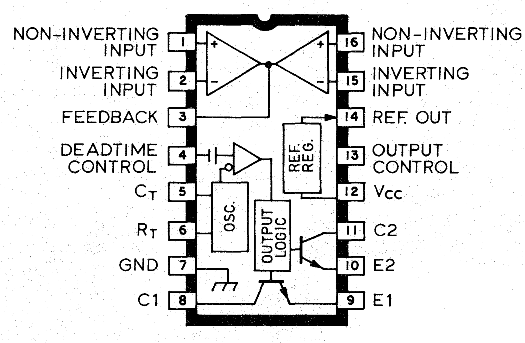
TYPICAL OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING CAPACITANCE



ULN-8194A
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

FEATURES

- Complete PWM Control Circuitry
- Under-Voltage Lockout with Hysteresis
- 200 mA Output Current Sink or Source
- Output Control Selects Single-Ended or Push-Pull Operation
- Double-Pulse Suppression
- Variable Deadtime Control
- 5 V Reference Trimmed to 1%
- Easy Multiple Device Slaving
- Equivalent to TL594CN



Dwg. No. A-12,362A

ALL functions required of a high-performance switched-mode power supply control circuit or pulse-width modulation controller are provided by the Type ULN-8194A integrated circuit.

This single, monolithic device contains an on-chip 5 V precision reference (trimmed to ±1%), two error amplifiers, a deadtime control comparator, output-control circuitry, low-voltage lockout, and an adjustable oscillator designed primarily for power supply control.

Type ULN-8194A has uncommitted output transistors that can be used in either a common-emitter or an emitter-follower configuration. Push-pull or single-ended output can be selected by externally available output-control logic.

Internal structure of the device protects outputs from double pulses during push-pull operation. Low-voltage lockout circuitry prevents activation of outputs until on-board voltages reach operational levels. The error amplifiers operate over a common-mode voltage range of −0.3 V to (V_{CC} − 2.0 V). Unless externally altered, the deadtime control comparator has a fixed offset that provides a delay of approximately 5 percent.

Type ULN-8194A is furnished in a 16-pin dual in-line plastic package with a copper lead frame that gives it enhanced power dissipation ratings. It is rated for operation over a temperature range of 0°C to +70°C. The controller can also be supplied, on request, in a ceramic/glass hermetic (cer-DIP) package.

ABSOLUTE MAXIMUM RATINGS
Over Operating Free-Air Temperature Range

Supply Voltage, V_{CC}	41 V
Output Voltage, V_C	41 V
Output Current, I_O	250 mA
Amplifier Input Voltage, V_{IN}	V_{CC} + 0.3 V
Package Power Dissipation, P_D	1.0 W*
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate linearly to 0 W at T_A = +150°C.

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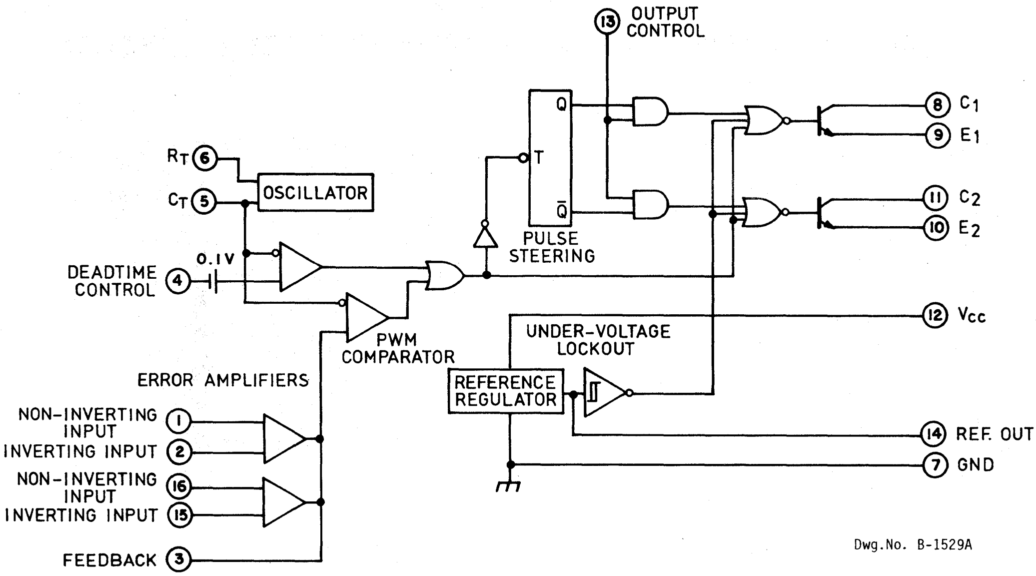
FUNCTIONAL BLOCK DIAGRAM



Dwg.No. B-1529A

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC}	7.0 to 40 V
Amplifier Input Voltage Range, V_I	-0.3 V to $V_{CC} - 2.0$ V
Output Voltage, V_C	40 V
Output Current, I_O (each transistor)	200 mA
Feedback Current, I_F	300 μA
Timing Capacitance Range, C_T	470 pF to 10 μF
Timing Resistor Range, R_T	1.8 to 500 kΩ
Oscillator Frequency Range	1.0 to 300 kHz

FUNCTION TABLE

Output Control, V_{13}	Output Function
<400 mV	Single-ended or Parallel Output
>2.4 V	Normal Push-Pull Operation

ELECTRICAL CHARACTERISTICS over operating free-air temperature range, V_{CC} = 15 V, f_o = 10 kHz (unless otherwise noted)

Characteristic	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
OUTPUT SECTION					
Collector Off-State Current	V_{CE} = 40 V, V_{CC} = 40 V	—	2.0	100	μA
Emitter Off-State Current	V_{CC} = V_C = 40 V, V_E = 0 V	—	—	−100	μA
Common-Emitter V_{CE}	V_E = 0 V, I_C = 200 mA	—	1.1	1.3	V
Emitter-Follower $V_{CE(SAT)}$	V_C = 15 V, I_E = −200 mA	—	1.5	2.5	V
Output-Control Input Current	V_{13} = V_{REF}	—	—	3.5	mA
Output-Current Voltage-Lockout Condition	V_{CC} = 1.0 to 3.0 V, V_C = 15 V, V_{CTRL} = 0 V	—	4.0	200	μA
REFERENCE SECTION					
Output Voltage (V_{REF})	I_0 = 1.0 mA, T_A = +25°C	4.95	5.0	5.05	V
Input Regulation	V_{CC} = 7.0 V to 40 V, T_A = +25°C	—	2.0	25	mV
Output Regulation	I_0 = 1.0 mA to 10 mA, T_A = +25°C	—	14	35	mV
Output-Voltage Change with Temperature	ΔT_A = 0°C to +70°C	—	0.2	1.0	%
Short-Circuit Output Current	V_{REF} = 0 V	10	35	50	mA
OSCILLATOR SECTION					
Operating Frequency	C_T = 0.01 μF, R_T = 12 kΩ	—	10	—	kHz
Standard Deviation of Frequency	External Conditions and Components Constant	—	10	—	%
Frequency Change with Voltage	V_{CC} = 7.0 V to 40 V, T_A = +25°C	—	0.1	—	%
Frequency Change with Temperature	C_T = 0.01 μF, R_T = 12 kΩ, ΔT_A = 0°C to +70°C	—	1.0	5.0	%

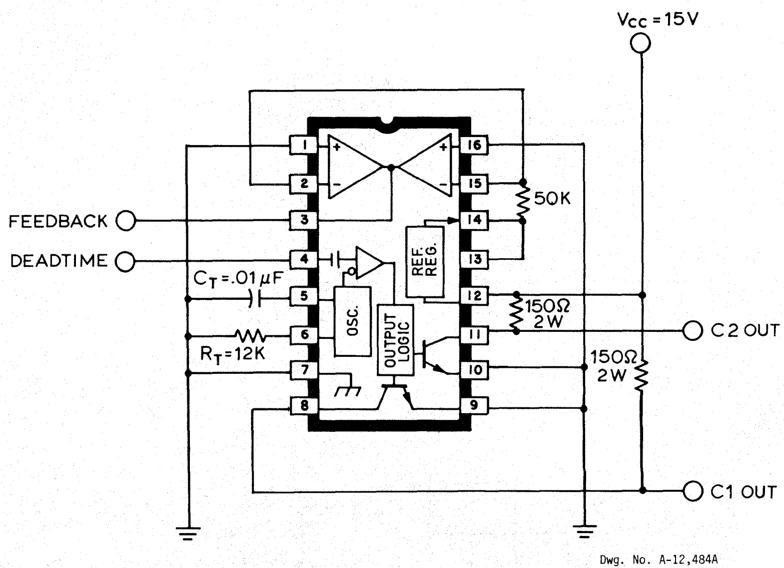
Continued next page

ELECTRICAL CHARACTERISTICS (Continued)

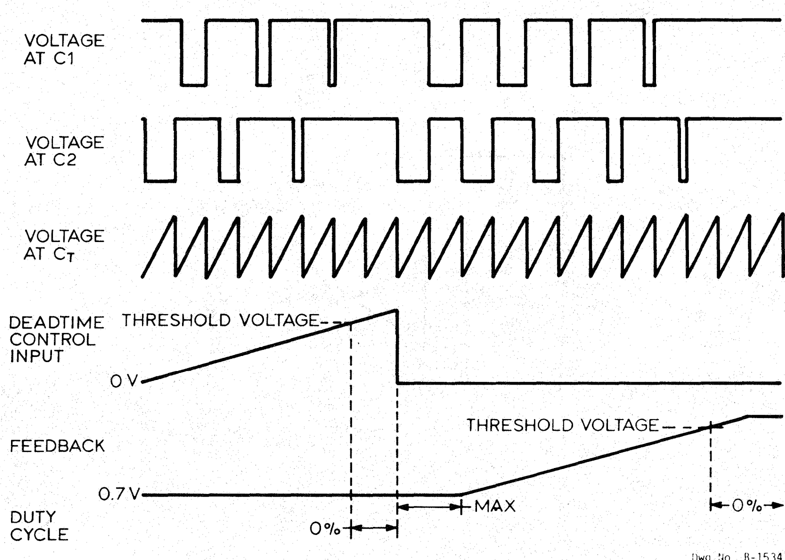
Characteristic	Test Conditions	Limits Min.	Typ.	Max.	Units
SWITCHING CHARACTERISTICS at $T_A = +25°C$					
Output-Voltage Rise Time, t_r	Common-Emitter Output	—	100	200	ns
	Emitter-Follower Output	—	200	400	ns
Output-Voltage Fall Time t_f	Common-Emitter Output	—	30	100	ns
	Emitter-Follower Output	—	45	100	ns
DEADTIME CONTROL					
Input Bias Current	V_4 = 0 V to 5.25 V	—	−2.0	−10	μA
Maximum Duty Cycle	Each Output, V_4 = 0 V	45	—	—	%
Input Threshold Voltage	Duty Cycle = 0%	—	3.0	3.3	V
	Duty Cycle = Maximum	0	—	—	V
ERROR AMPLIFIERS					
Input Offset Voltage	V_0 = 2.5 V (Pin 3)	—	2.0	10	mV
Input Offset Current	V_0 = 2.5 V (Pin 3)	—	25	250	nA
Input Bias Current	V_0 = 2.5 V (Pin 3)	—	200	1000	nA
Common-Mode Input Voltage	V_{CC} = 7.0 V to 40 V	−0.3	—	V_{CC} − 2.0	V
Open-Loop Voltage Gain	ΔV_0 = 3.0 V, V_0 = 0.5 V to 3.5 V	70	95	—	dB
Unity-Gain Bandwidth		—	800	—	kHz
Common-Mode Rejection Ratio	V_{CC} = 40 V, T_A = +25°C	65	80	—	dB
Output Sink Current	V_{IN} = −0.015 V to −5.0 V, V_0 = 0.5 V	300	700	—	μA
Output Source Current	V_{IN} = 0.015 V to 5.0 V, V_0 = 3.5 V	−2.0	—	—	mA
UNDER-VOLTAGE SECTION					
Under-Voltage Lockout	At T_A = +25°C	—	—	6.0	V
	Over Operating Temperature Range	3.5	—	6.9	V
Hysteresis		100	—	—	mV
PWM COMPARATOR SECTION					
Input Threshold Voltage	Zero Duty Cycle	—	4.0	4.5	V
Input Sink Current	V_3 = 0.5 V	300	700	—	μA
TOTAL DEVICE					
Quiescent Supply Current	V_{CC} = 15 V, Pin 6 = V_{REF}, Inputs and Outputs Open	—	9.0	15	mA
	V_{CC} = 40 V, Pin 6 = V_{REF}, Inputs and Outputs Open	—	11	18	mA
Average Supply Current	V_4 = 2.0 V	—	12.4	—	mA

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.
All typical values, except for parameter changes with temperature, are at T_A = +25°C.

TEST CIRCUIT



TYPICAL WAVEFORMS



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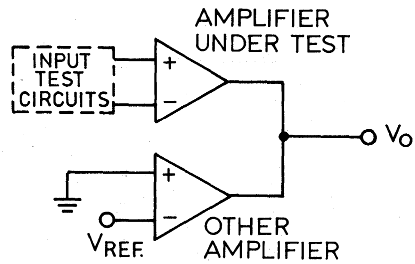
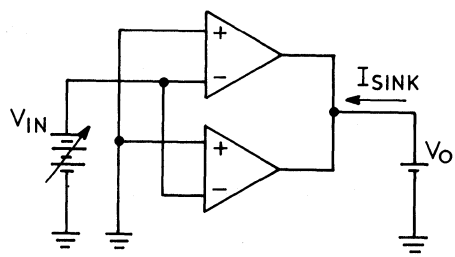
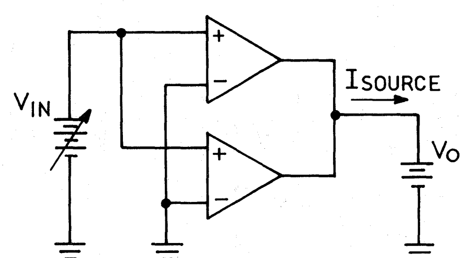
ERROR-AMPLIFIER TEST CIRCUITS

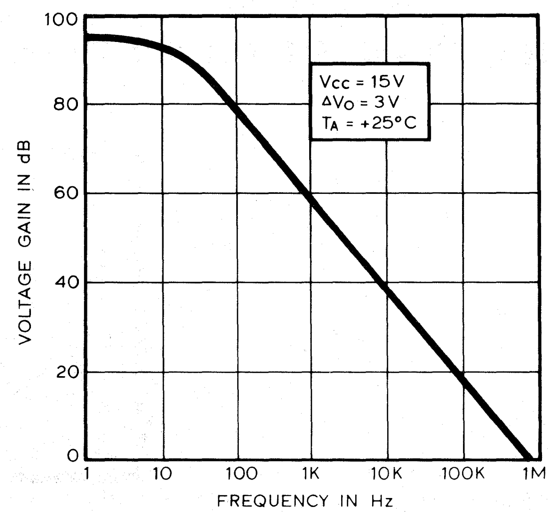






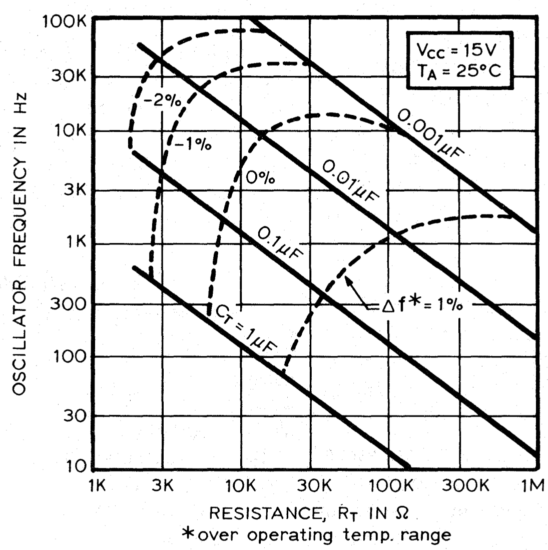
Dwg.No. B-1535

TYPICAL FREQUENCY RESPONSE OF ERROR AMPLIFIER



Dwg.No. A-12,483

TYPICAL OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING RESISTANCE



Dwg. No. A-12,482

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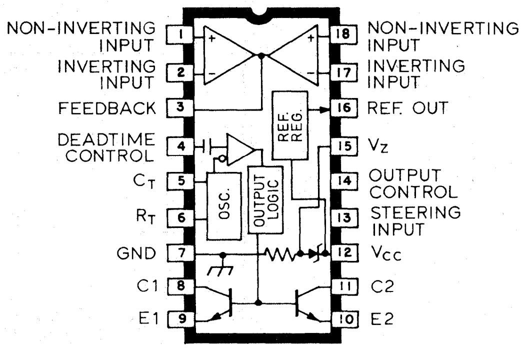
ULN-8195A
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

FEATURES

- Complete PWM Control Circuitry
- Under-Voltage Lockout with Hysteresis
- 200 mA Output Current Sink or Source
- Output Control Selects Single-Ended or Push-Pull Operation
- Double-Pulse Suppression
- Variable Deadtime Control Over Total Range
- 5 V Reference Trimmed to 1%
- Easy Multiple Device Slaving
- On-Chip 39 V Zener
- External Control of Output Steering
- Equivalent to TL595CN



Dwg. No. A-12,361A

A SINGLE monolithic Type ULN-8195A provides all of the functions required of a high-performance switched-mode power supply controller or pulse-width modulation control circuit. In addition, the integrated circuit has a 39 V Zener diode for high-voltage applications in which V_{CC} exceeds 40 V, and an output-steering control that overrides the internal pulse-steering flip-flop.

The Type ULN-8195A controller contains an on-chip 5 V precision reference (trimmed to ± 1%), two error amplifiers, a deadtime control comparator, output-control circuitry, low-voltage lockout, and an adjustable oscillator designed primarily for power supply control.

Type ULN-8195A has uncommitted output transistors that can be used in either a common-emitter or an emitter-follower configuration. Push-pull or single-ended output can be selected by externally available output-control logic.

Internal structure of the device protects outputs from double pulses during push-pull operation. Low-voltage lockout circuitry prevents activation of outputs until on-board voltages reach operational levels. The error amplifiers operate over a common-mode voltage range of −0.3 V to (V_{CC} − 2.0 V). Unless externally altered, the deadtime control comparator has a fixed offset that provides a delay of approximately 5 percent.

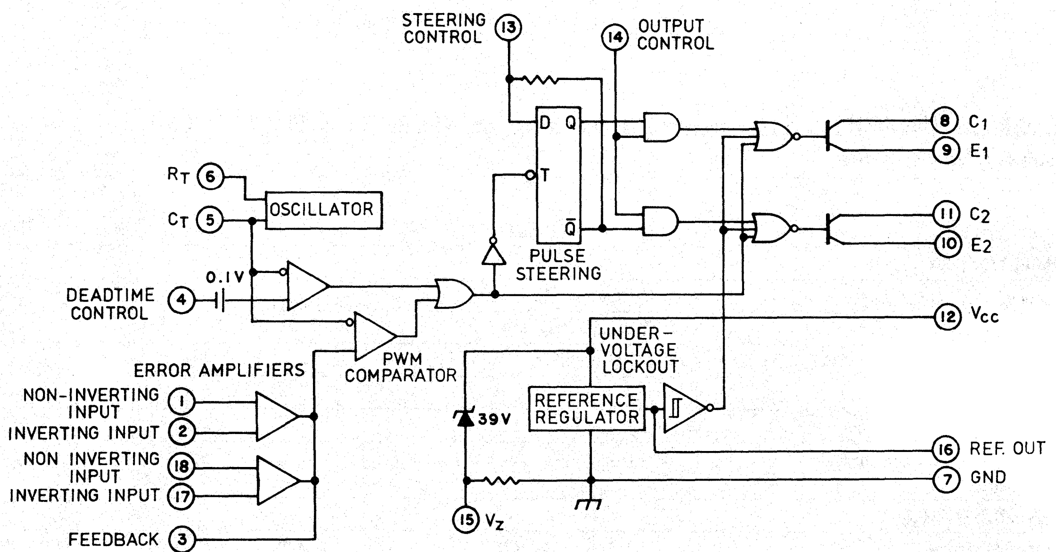
Type ULN-8195A is supplied in an 18-pin dual in-line plastic package with a copper lead frame that gives it enhanced power dissipation ratings. It is rated for operation over a temperature range of 0°C to +70°C. The controller can also be supplied, on request, in a ceramic/glass hermetic (cer-DIP) package.

ABSOLUTE MAXIMUM RATINGS
Over Operating Free-Air Temperature Range

Supply Voltage, V_{CC}	41 V
Output Voltage, V_C	41 V
Output Current, I_O	250 mA
Amplifier Input Voltage, V_{IN}	V_{CC} + 0.3 V
Package Power Dissipation, P_D	1.0 W*
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate linearly to 0 W at T_A = +150°C.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. B-1530A

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC}	7.0 to 40 V
Amplifier Input Voltage Range, V_I	$-$0.3 V to $V_{CC}-$2.0 V
Output Voltage, V_C	40 V
Output Current, I_O (Each Transistor)	200 mA
Feedback Current, I_F	300 µA
Timing Capacitance Range, C_T	470 pF to 10 µF
Timing Resistor Range, R_T	1.8 to 500 kΩ
Oscillator Frequency Range	1.0 to 300 kHz

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FUNCTION TABLE

Output Control, V_{14}	Steering Input, V_{13}	Output Function
<400 mV	Open	Single-Ended or Parallel Output
>2.4 V	Open	Normal Push-Pull Operation
>2.4 V	<400 mV	PWM Output at C_1E_1
>2.4 V	>2.4 V	PWM Output at C_2E_2

ELECTRICAL CHARACTERISTICS over operating free-air temperature range, V_{CC} = 15 V, f_o = 10 kHz (unless otherwise noted)

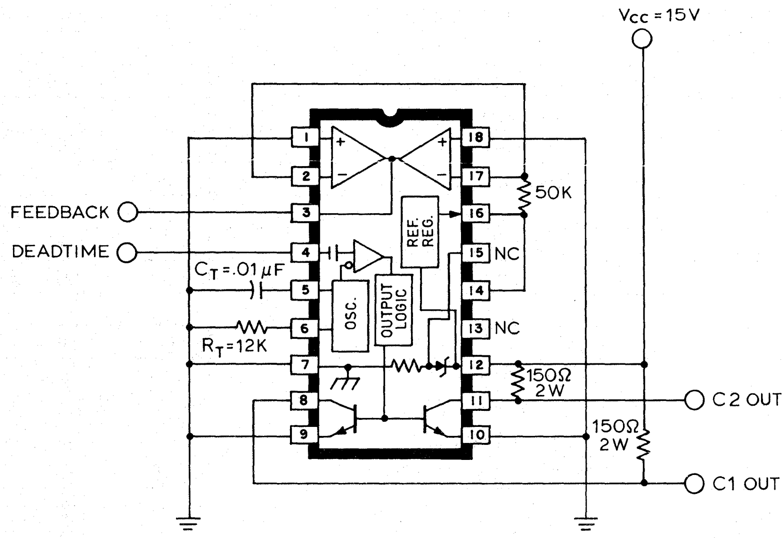
Characteristic	Test Conditions	Limits Min.	Typ.	Max.	Units
OUTPUT SECTION					
Collector Off-State Current	V_{CE} = 40 V, V_{CC} = 40 V	—	2.0	100	μA
Emitter Off-State Current	V_{CC} = V_C = 40 V, V_E = 0 V	—	—	−100	μA
Common-Emitter V_{CE}	V_E = 0 V, I_C = 200 mA	—	1.1	1.3	V
Emitter-Follower $V_{CE(SAT)}$	V_C = 15 V, I_E = −200 mA	—	1.5	2.5	V
Output-Control Input Current	V_{14} = V_{REF}	—	—	3.5	mA
Output-Current Voltage-Lockout Condition	V_{CC} = 1.0 to 3.0 V, V_C = 15 V, V_{CTRL} = 0 V	—	4.0	200	μA
REFERENCE SECTION					
Output Voltage (V_{REF})	I_0 = 1.0 mA, T_A = +25°C	4.95	5.0	5.05	V
Input Regulation	V_{CC} = 7.0 V to 40 V, T_A = +25°C	—	2.0	25	mV
Output Regulation	I_0 = 1.0 mA to 10 mA, T_A = +25°C	—	14	35	mV
Output-Voltage Change with Temperature	ΔT_A = 0°C to +70°C	—	0.2	1.0	%
Short-Circuit Output Current	V_{REF} = 0 V	10	35	50	mA
OSCILLATOR SECTION					
Operating Frequency	C_T = 0.01 μF, R_T = 12 kΩ	—	10	—	kHz
Standard Deviation of Frequency	External Conditions and Components Constant	—	10	—	%
Frequency Change with Voltage	V_{CC} = 7.0 V to 40 V, T_A = +25°C	—	0.1	—	%
Frequency Change with Temperature	C_T = 0.01 μF, R_T = 12 kΩ, ΔT_A = 0°C to +70°C	—	1.0	5.0	%
SWITCHING CHARACTERISTICS at T_A = +25°C					
Output-Voltage Rise Time, t_r	Common-Emitter Output	—	100	200	ns
	Emitter-Follower Output	—	200	400	ns
Output-Voltage Fall Time, t_f	Common-Emitter Output	—	30	100	ns
	Emitter-Follower Output	—	45	100	ns

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
DEADTIME CONTROL					
Input Bias Current	V_4 = 0 V to 5.25 V	—	−2.0	−10	μA
Maximum Duty Cycle	Each Output, V_4 = 0 V	45	—	—	%
Input Threshold Voltage	Duty Cycle = 0%	—	3.0	3.3	V
	Duty Cycle = Maximum	0	—	—	V
ZENER CIRCUIT					
Breakdown Voltage	V_{CC} = 41 V, I_Z = 2.0 mA	—	39	—	V
Sink Current	V_{15} = 1.0 V	—	300	—	μA
ERROR AMPLIFIERS					
Input Offset Voltage	V_0 = 2.5 V (Pin 3)	—	2.0	10	mV
Input Offset Current	V_0 = 2.5 V (Pin 3)	—	25	250	nA
Input Bias Current	V_0 = 2.5 V (Pin 3)	—	200	1000	nA
Common-Mode Input Voltage	V_{CC} = 7.0 V to 40 V	−0.3	—	V_{CC} − 2.0	V
Open-Loop Voltage Gain	ΔV_0 = 3.0 V, V_0 = 0.5 V to 3.5 V	70	95	—	dB
Unity-Gain Bandwidth		—	800	—	kHz
Common-Mode Rejection Ratio	V_{CC} = 40 V, T_A = +25°C	65	80	—	dB
Output Sink Current	V_{IN} = −0.015 V to −5.0 V, V_0 = 0.5 V	300	700	—	μA
Output Source Current	V_{IN} = 0.015 V to 5.0 V, V_0 = 3.5 V	−2.0	—	—	mA
UNDER-VOLTAGE SECTION					
Under-Voltage Lockout	At T_A = +25°C	—	—	6.0	V
	Over Operating Temperature Range	3.5	—	6.9	V
Hysteresis		100	—	—	mV
PWM COMPARATOR SECTION					
Input Threshold Voltage	Zero Duty Cycle	—	4.0	4.5	V
Input Sink Current	V_3 = 0.5 V	300	700	—	μA
TOTAL DEVICE					
Quiescent Supply Current	V_{CC} = 15 V, Pin 6 = V_{REF}, Inputs and Outputs Open	—	9.0	15	mA
	V_{CC} = 40 V, Pin 6 = V_{REF}, Inputs and Outputs Open	—	11	18	mA
Average Supply Current	V_4 = 2.0 V	—	12.4	—	mA

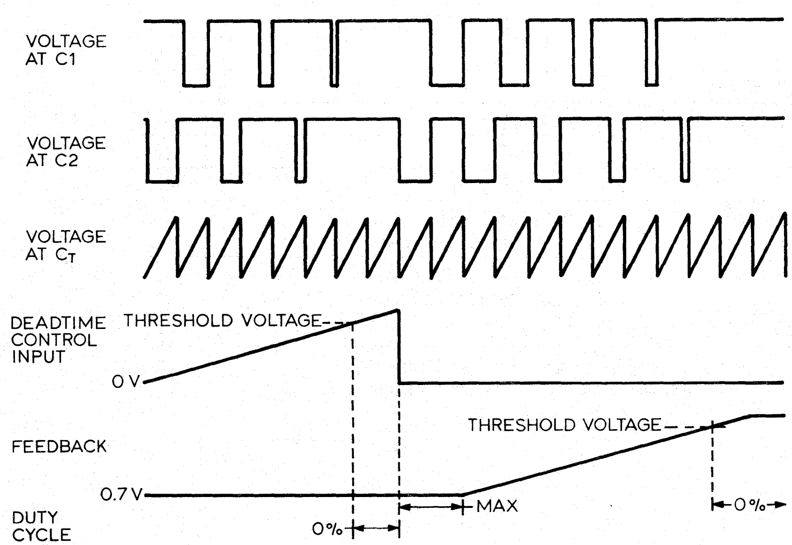
NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.
All typical values, except for parameter changes with temperature, are at T_A = +25°C.

TEST CIRCUIT



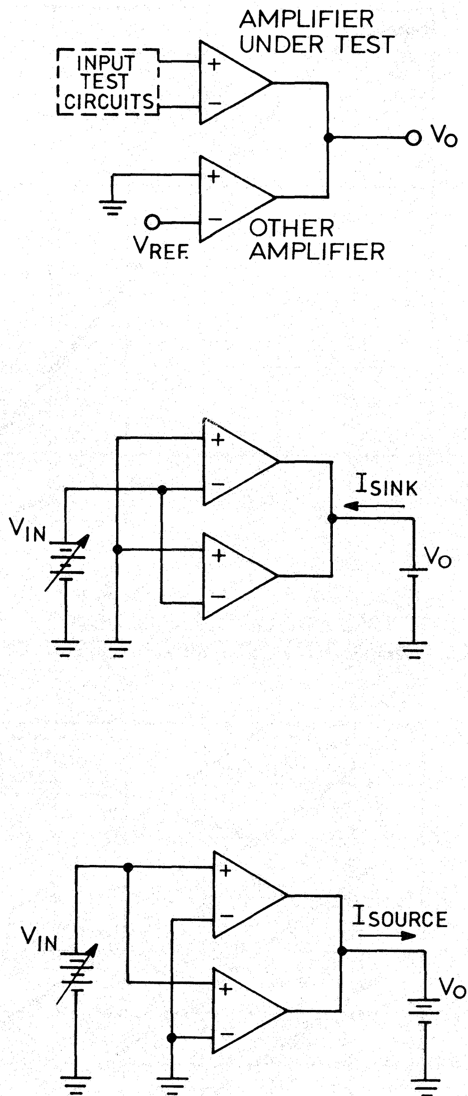
Dwg. No. A-12,481A

TYPICAL WAVEFORMS



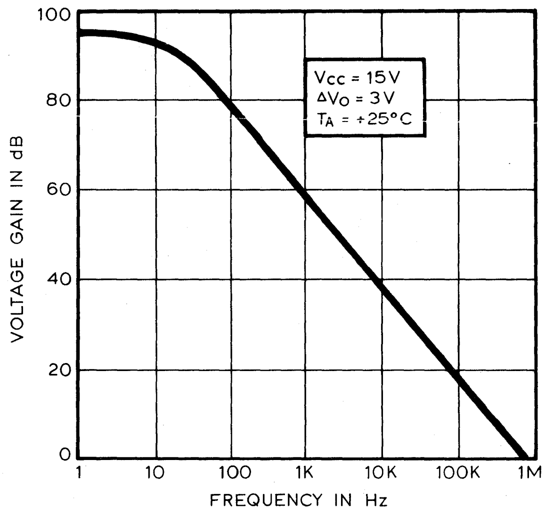
Dwg.No. B-1534

ERROR-AMPLIFIER TEST CIRCUITS



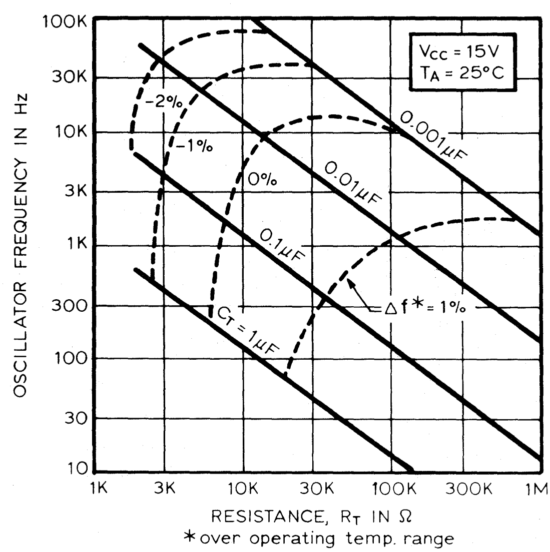
Dwg.No. B-1535

TYPICAL FREQUENCY RESPONSE OF ERROR AMPLIFIER



Dwg. No. A-12,483

TYPICAL OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING RESISTANCE

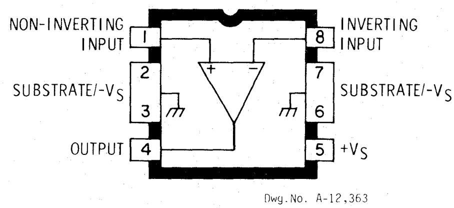


Dwg. No. A-12,482

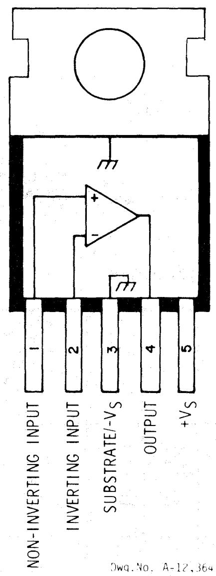
ULN-3751B AND ULN-3751Z
POWER OPERATIONAL AMPLIFIERS

FEATURES

- ± 3 V to ± 15 V Operation
- High Output Swing
- Peak Output Current to ± 3.5 A
- 2 mV Typical Input Offset
- 90 dB Typical Open-Loop Gain
- Internal Thermal Shutdown
- High Common-Mode Input Range
- Unity Gain Stable
- Pin Compatible with L165, L465, SG1173



ULN-3751B



ULN-3751Z

AS COMBINATION general-purpose operational amplifiers and power boosters, Type ULN-3751B and ULN-3751Z integrated circuits simplify circuit design, reduce component count, and enhance system reliability.

The power op amps feature high-impedance differential inputs, a unity-gain stable amplifier that needs no external compensation, and a high-current power output. Typical applications include use as voice-coil motor drivers, linear servo amplifiers, power oscillators, bipolar voltage regulators, and audio power drivers.

The economical Type ULN-3751B is for applications requiring up to ± 2 A of peak output current. It is supplied in an improved 8-lead dual in-line plastic package with two webbed tabs. A copper alloy lead frame allows maximum power dissipation without a heat sink. The lead configuration is compatible with standard IC sockets and printed wiring board layouts.

The more powerful Type ULN-3751Z is for applications demanding up to ± 3.5 A of peak output current. It is furnished in a modified 5-lead JEDEC-style TO-220 plastic package. Lead forming for vertical or horizontal mounting is available (ULN-3751ZV or ULN-3751ZH). The heat sink tab is at substrate potential and must be insulated from ground when the device is used with a split supply.

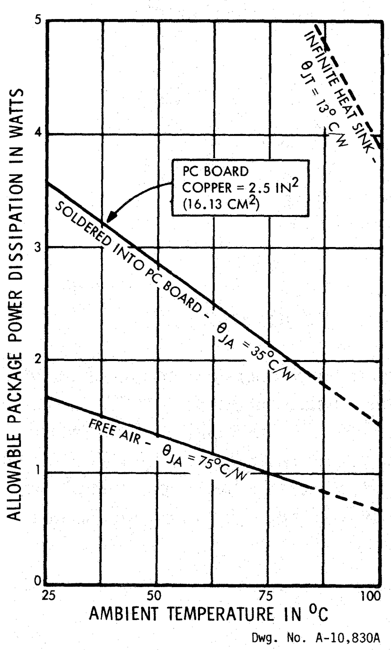
The power op amps operate over a recommended supply-voltage range of ± 3.0 V to ± 13 V. Selected devices that operate with supplies of ± 15 V (± 17 V, maximum), are available as ULN-3751B-1 and ULN-3751Z-1. Except for the supply-voltage specification, parts with the "– 1" suffix are identical to the basic parts.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

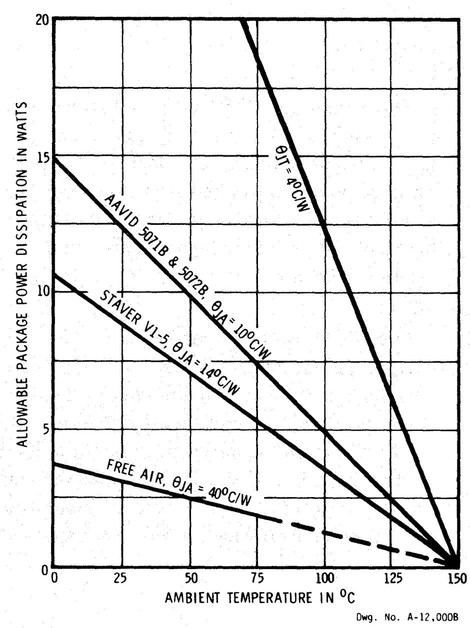
Supply Voltage Differential ($+V_S$ to $-V_S$)
(ULN-3751B, ULN-3751Z) .... 28 V
(ULN-3751B-1, ULN-3751Z-1) .... 34 V
Peak Output Current, I_{OUT}
(ULN-3751B, ULN-3751B-1) .... ±2.0 A
(ULN-3751Z, ULN-3751Z-1) .... ±3.5 A
Input Voltage Range, V_{IN} .... $(+V_S - 2\ V)$ to $-V_S$
Differential Input Voltage .... ΔV_S
Junction Temperature, T_J .... +150°C
Operating Temperature Range, T_A .... 0°C to +70°C
Storage Temperature Range, T_S .... −40°C to +150°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

ULN-3751B



ULN-3751Z

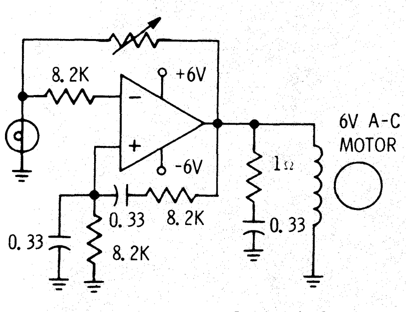


ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_{TAB} \leq$ +70°C, $+V_S$ = +6.0 V, $-V_S$ = −6.0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Operating Voltage Range	V_S	ULN-3751B and ULN-3751Z	±3.0	±6.0	±13	V
		ULN-3751B-1 and ULN-3751Z-1	±3.0	±12	±15	V
Quiescent Supply Current	$+I_S$		—	52	70	mA
	$-I_S$		—	−52	−70	mA
Input Offset Voltage	V_{OS}	V_{out} = 0 V	—	±2.0	±10	mV
Input Bias Current	I_{IN}	V_{out} = 0 V	—	40	1000	nA
Input Offset Current	I_{OS}		—	10	100	nA
Open-Loop Gain	A_V	f = 0 Hz	80	90	—	dB
Slew Rate	SR	V_{in} = 200 mV, $R_L = \infty$	1.0	2.3	—	V/µs
Output Swing	V_{out}	I_{out} = 1.0 A	9.0	9.5	—	V_{pp}
Power Supply Rejection Ratio	PSRR	Positive or Negative Supply	60	80	—	dB
Common-Mode Rejection Ratio	CMRR	Positive or Negative Supply	60	85	—	dB
Thermal Shutdown	T_J		—	160	—	°C
Thermal Resistance	θ_{JT}	ULN-3751B and ULN-3751B-1	—	—	15	°C/W
		ULN-3751Z and ULN-3751Z-1	—	—	3.0	°C/W

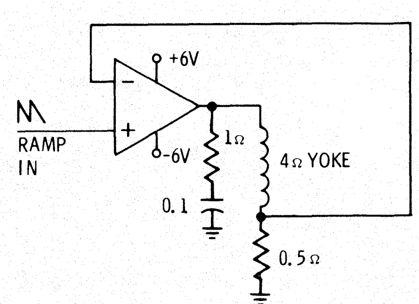
TYPICAL APPLICATIONS

WIEN BRIDGE OSCILLATOR/MOTOR DRIVER



Dwg.No. A-12,376

VIDEO MONITOR VERTICAL DEFLECTION AMP



Dwg.No. A-12,375

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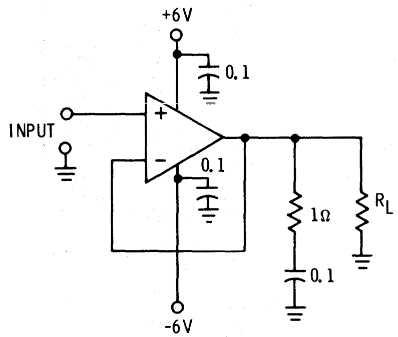
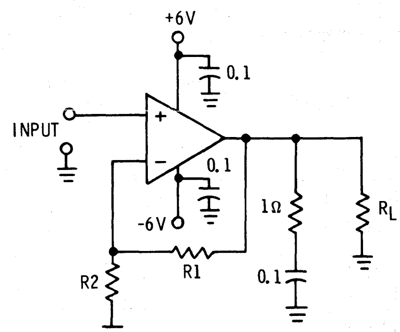
TYPICAL APPLICATIONS

UNITY GAIN VOLTAGE FOLLOWER



Dwg. No. A-12,551

NON-INVERTING POWER AMPLIFIER

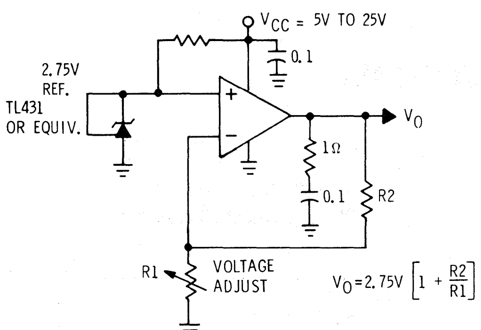


$A_V = 1 + \frac{R1}{R2}$

CAPACITANCE VALUES IN µF.

Dwg.No. A-12,552

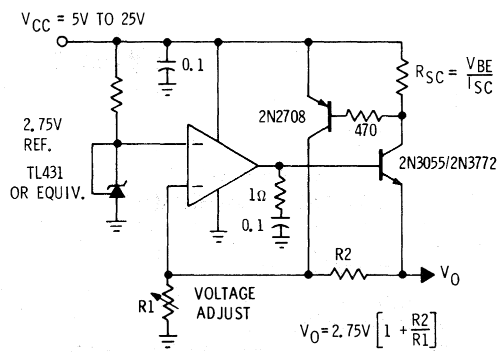
LINEAR VOLTAGE REGULATOR



CAPACITANCE VALUES IN µF.

Dwg. No. A-12,553

HIGH-POWER LINEAR REGULATOR
(Short-Circuit Protected)

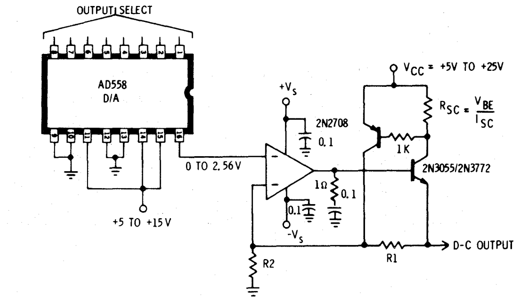


CAPACITANCE VALUES IN µF.

Dwg. No. A-12,554

TYPICAL APPLICATIONS

PROGRAMMABLE HIGH-CURRENT LINEAR REGULATOR



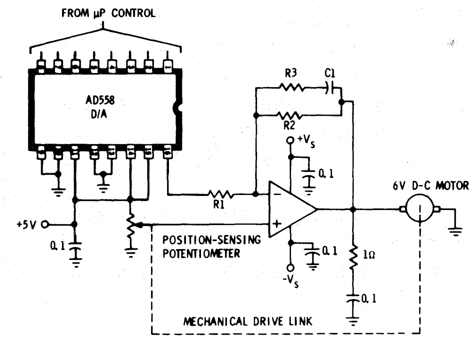
R1 AND R2 ARE SELECTED TO PROVIDE THE DESIRED OUTPUT. IT IS RECOMMENDED THAT $1.2 < \frac{R1}{R2} < 3.0$.

PINS 14 AND 15 OF D/A CONVERTER CAN BE CONNECTED TO PROVIDE EITHER 2.56V OR 10V FULL SCALE.

CAPACITANCE VALUES IN µF.

Dwg. No. A-12,555

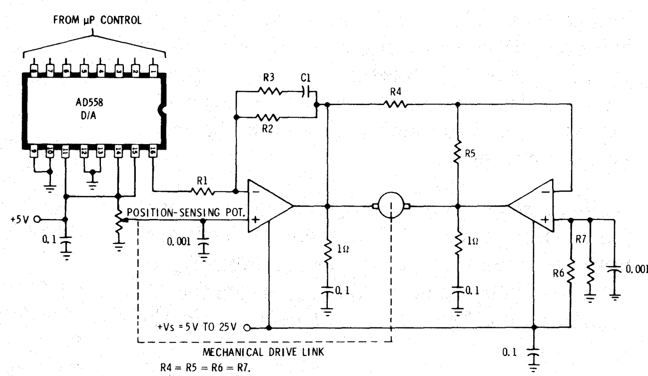
SINGLE-ENDED POSITION SERVO



R1, R2 DEFINE D-C GAIN.
R3, C1 PICKED TO PROVIDE LOOP COMPENSATION.
CAPACITANCE VALUES IN µF.

Dwg. No. A-12,556

FULL-BRIDGE POSITION SERVO



R4 = R5 = R6 = R7.
R1, R2 DEFINE D-C GAIN.
R3, C1 SELECTED FOR LOOP COMPENSATION.
CAPACITANCE VALUES IN µF.

Dwg. No. B-1543

10

A PRECISION LIGHT-SENSING INTEGRATED CIRCUIT

The Precision Light Sensor (PLS)[1] is a low-cost innovative approach to the accurate sensing of light levels in electronic circuits. It is a two-terminal monolithic integrated circuit that linearly converts light impinging upon it to a proportional output current. It is a light dependent current source. It requires no separate d-c bias current, so its supply current (output current) is a linear function of light level.

Introduction

The Precision Light Sensor, encased in a clear plastic TO-92 package, may be used as a direct replacement for photocells and phototransistors. The PLS, in many ways, is a superior device. The PLS output current (6 μA/lm/ft^2 of tungsten light at 2850°K) is comparable in magnitude to that of a phototransistor, but unlike a phototransistor, the PLS is within ±5% of the nominal value. The PLS is linear within 5% over the range of 1 to 200 lm/ft^2 of incident illumination. It operates over a supply voltage range of 2.7 to 24 V, having a typical power supply rejection ratio $(\Delta Io/Io)/\Delta V$ of 0.3%/V.

Need For A Precise Light Sensor

Many situations exist in which there is a need for the precise, linear conversion of light energy into an electrical signal. This conversion is usually accomplished through the use of devices such as photocells, phototransistors, and photodiodes. Limitations associated with these devices make them difficult and costly to use in precise, linear applications:

Photocells exhibit a change in resistance proportional to changes in light intensity. They are, however, highly inaccurate and exhibit a property of light memory; that is, a photocell's response to a light level is dependent on the previous ambient light level. For any reasonably accurate light sensing using a photocell, the ambient light level must be controlled. Due to unit-to-unit variation in sensitivity, photocells require an external calibration component, such as a trimmer potentiometer, in all but the simplest applications.

Phototransistors produce an output current proportional to the incident light intensity. They generally react much faster than photocells and do not exhibit the memory phenomenon. They do, however, exhibit an extremely wide variation of output current per unit of light due to process and beta variations. These variations in sensitivity can be ±50% or more within a group of devices of the same type.

Photodiodes have the inherent property of linearity of output current as a function of illumination, but the value of output current is very small, in the range of tens of nA per lm/ft^2. The photodiode's variation in sensitivity may be as much as ±25% from unit to unit.

In order to provide a precise, linear output current per unit of light at a usable current level, the best alternative to the devices mentioned previously is a device that combines the linearity of a photodiode with the output level of a calibrated current amplifier. The alternative is a two-terminal device that replaces all three previously mentioned light-sensing devices in most applications. This is the concept behind the design of the PLS.

(1) Sprague Electric Type ULN-3310Y.

Basic Circuit Concept

A simplified block diagram of the PLS is shown in Figure 1. In this configuration the PLS consists of a photodiode whose photocurrent, I_D, is amplified by a current amplifier having a constant gain, A_I. For the sensor's total current to be a linear function of light level, the amplifier's supply current must be a constant multiple, B, of the photocurrent, or else must be negligible in comparison to the output current.

One method of implementing this concept in circuit form is shown in Figure 2. In this case, a photodiode feeds a series of simple current mirrors, each having a fixed gain of 5 due to ratioed emitter areas. It can be shown that the output current of the entire circuit is a multiple of the photodiode current. In this manner, the requirement that the amplifier's supply current be either negligible or a constant multiple of the photocurrent is satisfied.

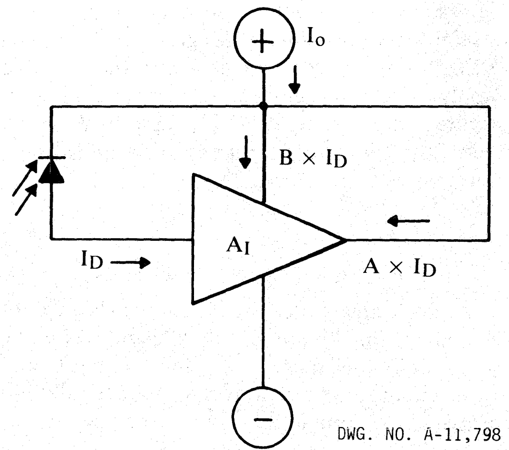


Figure 1
SIMPLIFIED PLS BLOCK DIAGRAM

This simple circuit fails to meet precision requirements for several reasons: First, the relatively low output resistance of the simple current mirrors results in great variations in output current with respect to changes in supply voltage $((\Delta Io/Io)/\Delta V)$. Second, since the photodiode's reverse-bias voltage is unregulated, it exhibits a significant variation in photocurrent due to changes in supply voltage. In both of these cases, the error current is multiplied through gain stages of the current amplifier, so the total output-current error can be large.

There are other problems associated with the basic circuit of Figure 2. The simple current mirrors exhibit large base-current errors and therefore are highly beta-dependent in terms of gain-accuracy. In addition, there is no means available to calibrate this circuit to the precision required, taking into account mismatches in the current-mirror transistors and processing variations among individual photodiodes.

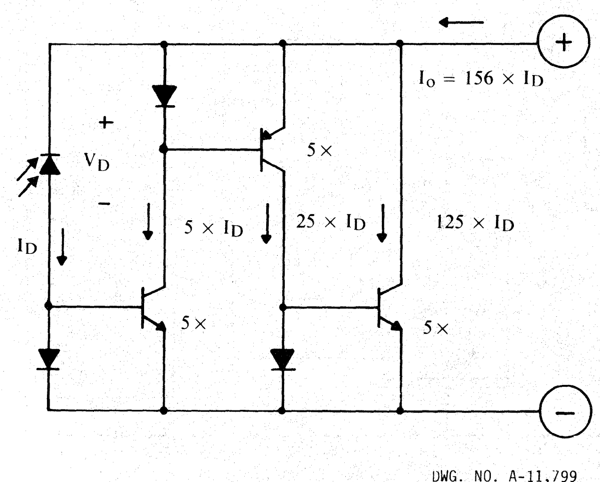


Figure 2
SIMPLIFIED PLS SCHEMATIC

Even though the basic circuit described above has some significant drawbacks, it can be a useful starting point in design of a functional PLS. Using the basic concept as presented, and applying certain circuit techniques and configurations, a practical PLS integrated circuit with the desired operating characteristics is feasible.

Functional Circuit Description

A block diagram of the functional PLS circuit is shown in Figure 3. It is similar to the simplified block diagram of Figure 1, but it contains circuit modifications that dramatically improve its performance.

A series-pass voltage regulator circuit (Figure 4) has been added in order to regulate the reverse-bias voltage on the primary photodiode. The voltage regulator, in turn, is driven by an auxiliary photodiode that is approximately one-half the area of the primary photodiode. Through the use of an auxiliary photodiode, the regulator bias current becomes a linear function of light level. Under dark conditions, there is no d-c bias current.

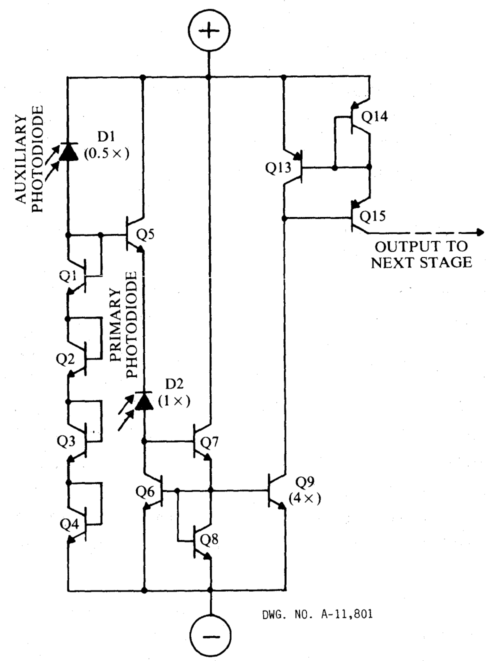


Figure 4
PHOTODIODE-DRIVEN SERIES-PASS VOLTAGE REGULATOR/MODIFIED WILSON CURRENT-MIRROR INPUT STAGE

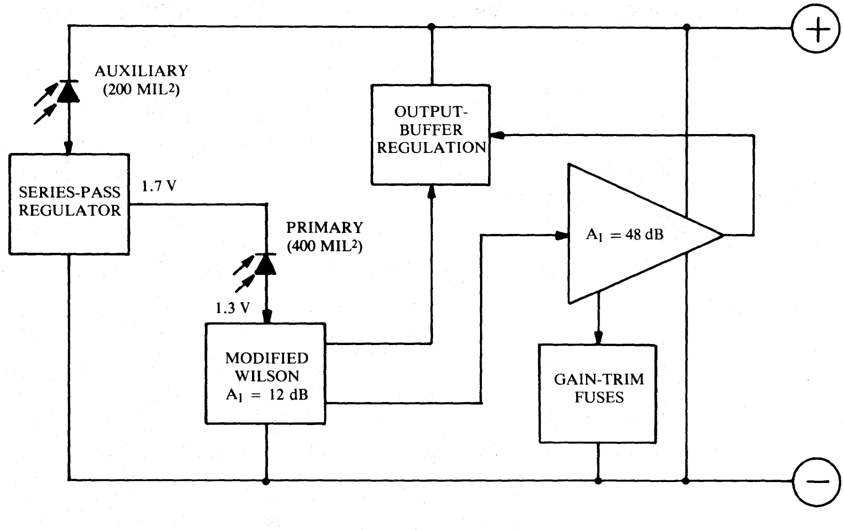


Figure 3
DETAILED PLS BLOCK DIAGRAM

An equivalent resistor pull-up would require a prohibitively large resistive value. In addition, a d-c bias current would flow, independent of light level but dependent on supply voltage. This condition is unacceptable for a two-terminal device such as the PLS.

Under dark conditions the auxiliary photodiode shuts down the regulator, shutting down the primary photodiode, thus minimizing the PLS dark current.

The regulated voltage applied to the cathode of the primary photodiode is approximately 1.7 V ($3 \times V_{BE}$). The anode of the primary photodiode is fed into a modified Wilson current mirror[2] input stage (Figure 4). Since the input of this mirror is approximately 1.3 V ($2 \times V_{BE}$) above ground, the regulated voltage across the primary photodiode is held to approximately 400 mV.

The modified Wilson input stage, in addition to providing 12 dB of current gain (4:1 emitter-area ratio), greatly improves PLS linearity at low light levels. The modified Wilson current mirror is basically a compromise between a Wilson current mirror and a buffered current mirror. The Wilson mirror has excellent linearity and accuracy, but has unity gain. The buffered current mirror can have a fixed gain greater than unity, but has poor linearity at low currents due to beta rolloff of the buffer transistor. The modified Wilson current mirror improves low-current operation by biasing up the buffer transistor, Q7, with the collector current of Q8. In this manner, the beta of Q7 does not roll off before the beta of Q6 or Q9 as it would in a buffered current mirror. This low-current operation is extended at the expense of a higher base-current error in the input stage. This compromise is essential if PLS output-current linearity down to 0.5 lm/ft^2 is to be achieved.

The remaining current-mirror stages provide a total of approximately 48 dB of current gain. The PNP mirrors are Wilson current mirrors having a unity gain. These mirrors have high output resistance and a low value of beta error ($\propto \beta^{-2}$). As mentioned previously, the Wilson current mirror's accuracy loses its independence with respect to beta variation if a gain greater than unity is required, so all of the gain must take place in the NPN mirror stages. Since the NPN betas are approximately four times as large as the PNP betas, buffered current mirrors with ratioed emitters are used to attain low values of beta error.

Although the gain and accuracy of the NPN buffered current mirrors are sufficient for the PLS, their output resistance is too low. In order to increase output resistance without adding a source of current error, the outputs of the NPN mirrors are buffered by a cascode output using a Darlington pair as the common-base stage. These buffers are, in turn, biased by a string of three diodes (Q19, Q20, Q21) driven by an auxiliary PNP buffered current mirror (Figure 5). In this manner, the outputs of the NPN current mirrors are buffered to increase output resistance by an arrangement that has a negligible effect on the total output current. This condition exists because the bias current driving the three-diode string is only two times the photodiode current. Any error caused by the buffer-stage base currents is isolated from the remaining gain stages.

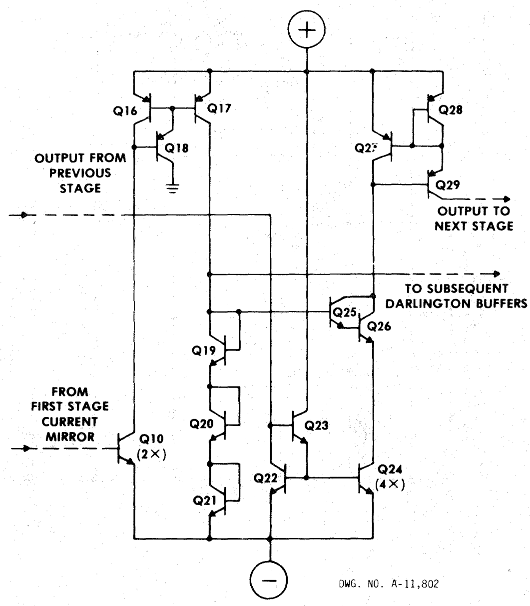


Figure 5
CASCODE-BUFFERED
NPN CURRENT-MIRROR OUTPUTS

(2) P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits,* Wiley, 1977, p. 208.

10

In order to provide the means for calibration of the output current at a standard light level, the emitters of the output transistors in the final NPN gain stage are connected to ground through fusible links. This fusing feature enables the initial accuracy of the PLS to be set at wafer probe to a value of ±5%.

An automatic current-limit feature has also been designed into the PLS circuit. By placing a 75kΩ resistor in series with the primary photodiode, the photocurrent — and therefore the output current — is limited to 8 mA, maximum (400 lm/ft^2). This limit protects the PLS, and any circuitry to which it is connected, from high output currents caused by abnormally high incident light levels. This current-limit feature can be easily masked out during manufacture if external current limiting is to be provided. The PLS schematic, incorporating all of the features discussed previously, is shown in Figure 6.

To summarize, the PLS is basically a photodiode with its photocurrent multiplied by a series of current mirrors having a gain fixed by ratioed emitter areas. In addition, to counteract variations in output current due to supply voltage changes, the primary photodiode is biased by a series-pass voltage regulator that, in turn, is driven by an auxiliary photodiode current. The current mirror stages are designed to have high output resistance. The final gain stage of the PLS has fusible links to facilitate the calibration of the output current to an initial accuracy of ±5%. An optional internal current-limit feature protects the PLS from exceeding its package power dissipation specifications due to abnormally high incident light levels.

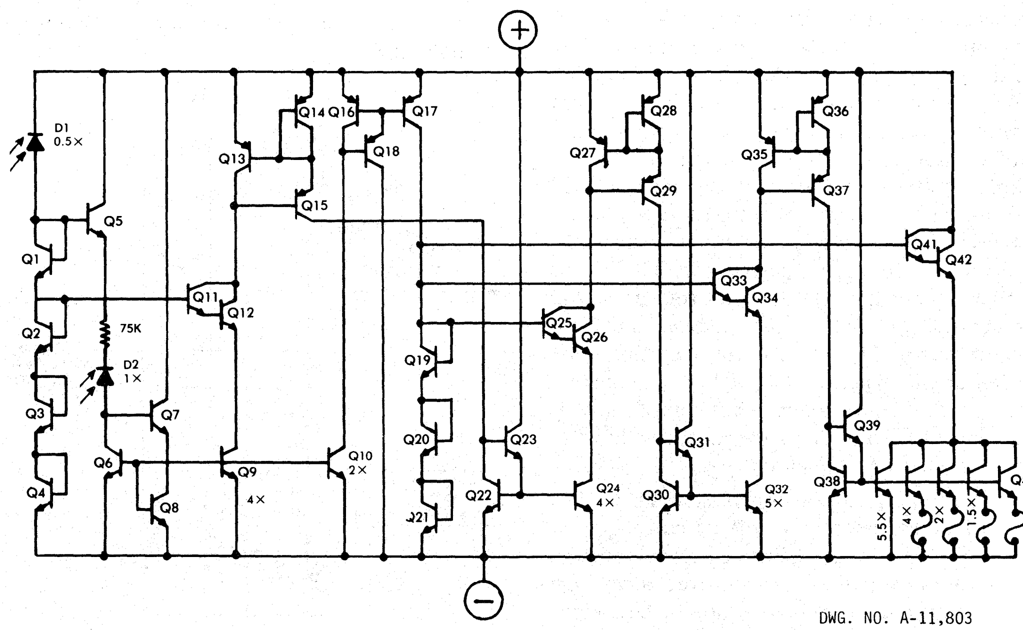


Figure 6
PLS SCHEMATIC

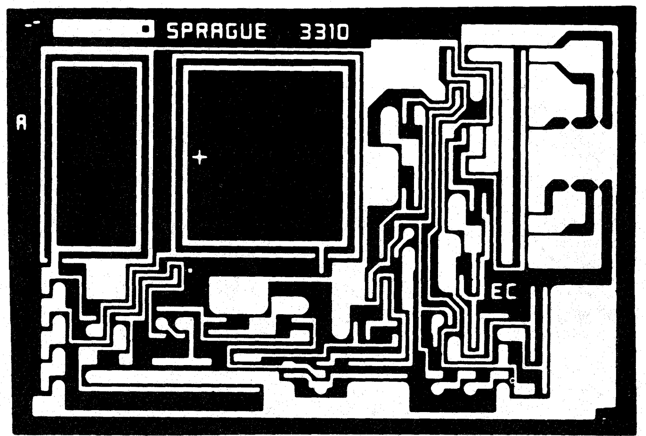


Figure 7
PLS METALLIZATION MASK

Layout and Processing

The PLS integrated circuit metallization mask is shown in Figure 7. The primary photodiode has an active area of 399 square mils; the auxiliary photodiode has an active area of 217 square mils. Both photodiodes use a base-collector structure as the active junction. The photodiode structure is shown in Figure 8. The major disadvantage of this structure is high capacitance per unit area that limits the maximum speed of the entire device. Since high speed was not an original requirement of the PLS, this structure was chosen for its floating (not grounded) anode. The large (14 ×) output transistor and its associated calibration fuse pads can be seen at the upper right-hand corner of the mask.

The PLS is processed using a 2 ohm•cm [100] epitaxial layer. This provides for high beta at low collector current (< 10 nA), which is a particular requirement for the input stage and voltage-regulator stage. This process will also provide circuit operation at a supply voltage of up to 24 V.

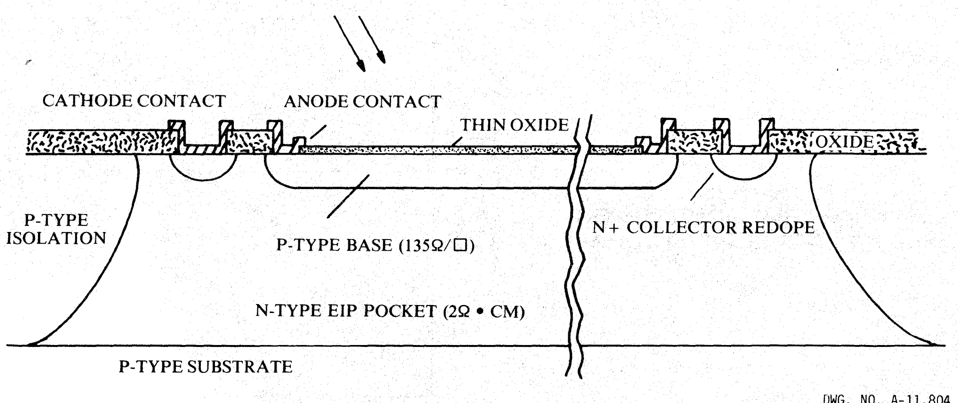


Figure 8
PLS PHOTODIODE STRUCTURE

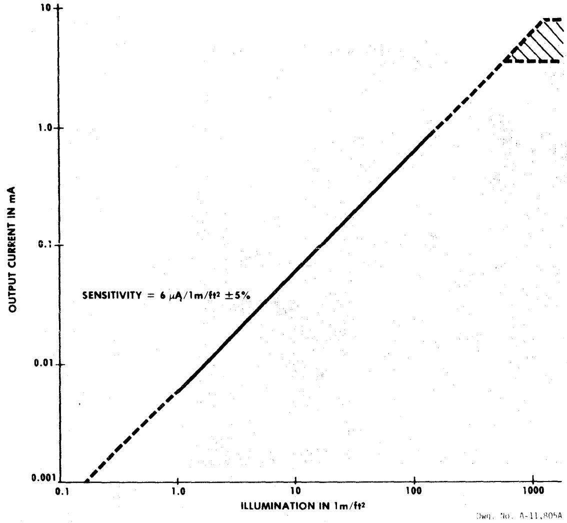


Figure 9
PLS OUTPUT CURRENT
AS A FUNCTION OF ILLUMINANCE

Circuit Performance

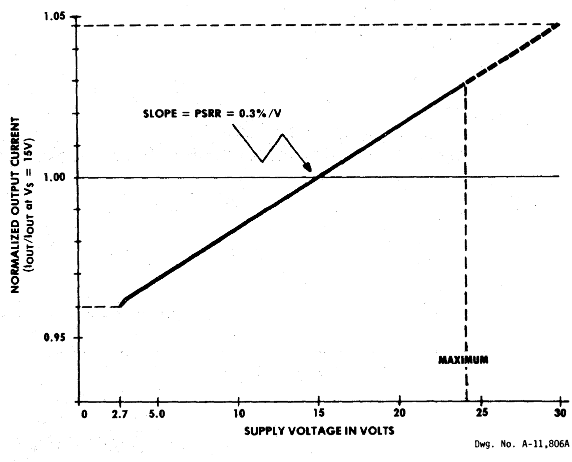
The PLS is calibrated and functionally tested at wafer probe using a computer-controlled light reference. It is operationally tested at 20 lm/ft² and then tested at 1 lm/ft² and 200 lm/ft² for linearity. The calibrated chips are then encased in clear TO-92 packages and subjected to final tests for correct operation.

A graph of typical output current as a function of illuminance is shown in Figure 9. The linearity drops off at less than 0.5 lm/ft². The internal current limit takes effect in the range between 200 and 400 lm/ft².

A graph of normalized output current as a function of supply voltage is shown in Figure 10. The power supply rejection ratio $((\Delta Io/Io)/\Delta V)$ is approximately 0.3%/V. This corresponds to an effective output conductance of 60n℧/1m/ft² for the PLS.[3]

(3) The International Electrotechnical Commission recommends the use of siemens (S) as the standard international unit of conductance.

Figure 10
PLS NORMALIZED OUTPUT CURRENT
AS A FUNCTION OF SUPPLY VOLTAGE



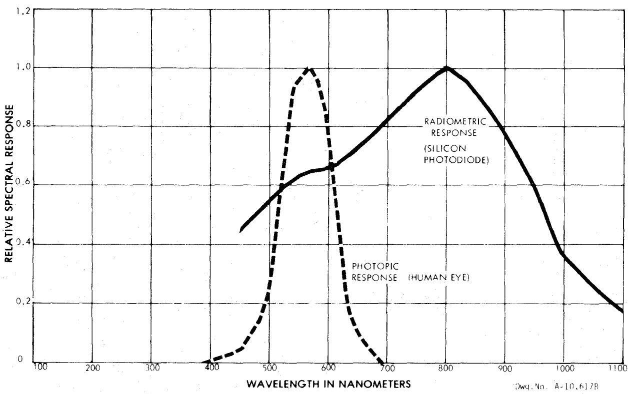


Figure 11
PLS PHOTODIODE SPECTRAL RESPONSE

The spectral response of the PLS photodiode, along with the photopic response curve, is shown in Figure 11. The wavelength of light incident on the PLS must be taken into account in all output-current calculations.

PLS Applications

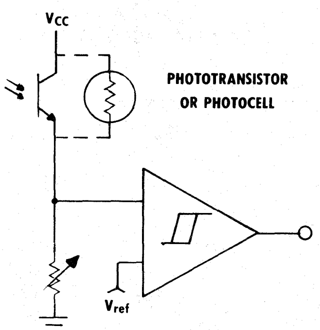
Precise Light-Level Sensing

A basic circuit application normally calling for a photocell or phototransistor is a light-level detection circuit (Figure 12A). In this configuration, at a certain predetermined incident light level, the voltage at the input of the Schmitt trigger reaches the threshold value and some event is triggered accordingly. In this case, in order to achieve the required precision, a potentiometer must be used to provide a means for system calibration.

The same circuit, using a PLS in place of the photocell or phototransistor, is shown in Figure 12B. Since the PLS is already calibrated to ±5% internally, a fixed-value resistor may be used, thus eliminating the need for manual calibration of the system.

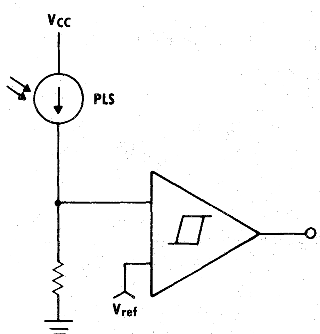
Display-Brightness Control

A PLS may be used in conjunction with a current-amplifier circuit, such as the one in Figure 13, in order to control the brightness of an LED display in stereo receivers and clock radios. As the ambient light level decreases, the display is automatically and proportionately dimmed. The 15kΩ resistor sets the minimum LED brightness level.



DWG. NO. A-11,808

Figure 12A
LIGHT-LEVEL DETECTOR
REQUIRING EXTERNAL CALIBRATION



DWG. NO. A-11,809

Figure 12B
LIGHT-LEVEL DETECTOR USING PLS

Camera Applications

The PLS can be used as a simple through-the-lens light meter in conjunction with a D'Arsonval movement (Figure 14). As the shutter speed switch is rotated, different shunt resistors are introduced into the circuit, relating the shutter speed setting to the meter reading.

Another camera application of the PLS is in automatic shutter timing (Figure 15). In this case, when the shutter is opened, the PLS begins to charge a capacitor, integrating the light level, until a predetermined trip voltage is reached. The shutter is then closed by the threshold detection circuitry.

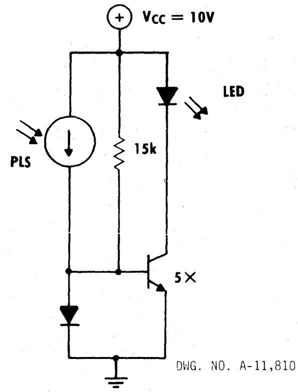


Figure 13
AUTOMATIC LED DISPLAY-BRIGHTNESS CONTROL

Conclusion

The PLS is designed as a low-cost, two-terminal replacement for photocells and phototransistors in the majority of light-sensing applications. In addition, the PLS is internally calibrated for an output current accurate to within ±5% at a nominal value of incident illumination. The PLS has a distinct advantage over photocells and phototransistors whenever precise light sensing is required, since no external calibration is required.

In the applications described previously and in many other instances, the PLS is a cost-effective solution to the problem of precise electronic light sensing.

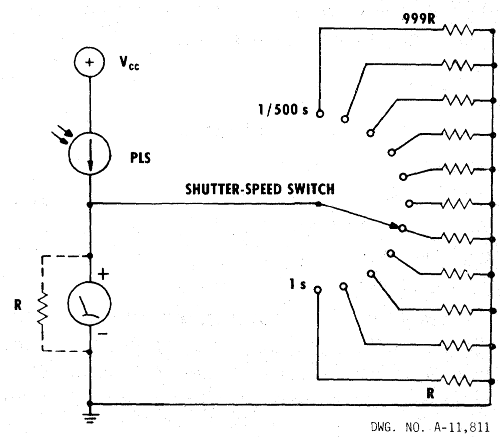


Figure 14
IN-CAMERA LIGHT METER

Specifications

Initial Accuracy at 20 lm/ft^2	±5%
Sensitivity	6 μA/lm/ft^2
Operating Voltage Range	2.7 to 30 V
Output Linearity (1 to 200 lm/ft^2)	5%
Output Conductance	60 n℧/lm/ft^2
Output Current Limit	8 mA
Power Supply Rejection Ratio	0.3%/V

Acknowledgements

The author thanks Walter Gontowski for his assistance with PLS development, from original design concept to final layout, and Paul Bergquist and Dorothy Westling for their help in the preparation of this paper.

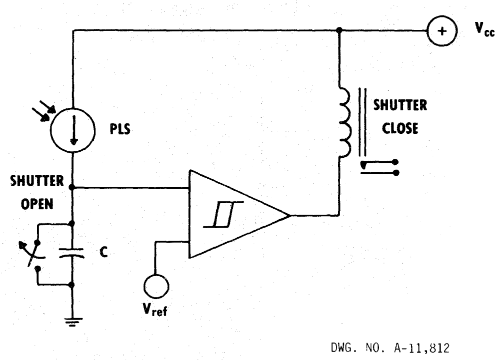


Figure 15
AUTOMATIC SHUTTER CONTROL

SECTION 11—CUSTOM DEVICES

†Complete information is provided in Data Book WR-503.

11

SECTION 12—PACKAGE INFORMATION

†Complete information is provided in Data Book WR-503.

Package Thermal Characteristics

Package Designator	Package Type	Frame Material	$R\Theta_{JA}$† (°C/W)	$R\Theta_{JC}$† (°C/W)
A	14-Pin Plastic DIP	Copper	60	38
A	16-Pin Plastic DIP	Copper	60	38
A	18-Pin Plastic DIP	Copper	55	25
A	20-Pin Plastic DIP	Copper	55	25
A	22-Pin Plastic DIP	Copper	50	21
A	28-Pin Plastic DIP	Copper	40	16
A	40-Pin Plastic DIP	Copper	36	—
B	8-Pin Semi-Tab Plastic DIP	Copper	75	13*
B	14-Pin Semi-Tab Plastic DIP	Copper	45	13*
B	16-Pin Semi-Tab Plastic DIP	Copper	45	13*
B	22-Pin Semi-Tab Plastic DIP	Copper	40	13*
D	3-Lead Metal Can		300	150
EC	20-Lead Hermetic LCC	Kovar	110	—
EC	28-Lead Hermetic LCC	Kovar	100	—
EP	20-Lead Plastic LCC	Copper	95	—
EP	44-Lead Plastic LCC	Copper	68	20
H	8-Pin Hermetic DIP	Kovar	120	40
H	14-Pin Hermetic DIP	Kovar	90	20
H	16-Pin Hermetic DIP	Kovar	90	20
H	18-Pin Hermetic DIP	Kovar	75	20
H	22-Pin Hermetic DIP	Kovar	65	20
J	14-Lead Flat Pack	Kovar	140	80
L	8-Lead SOIC	Copper	175	—
L	14-Lead SOIC	Copper	125	—
L	16-Lead SOIC	Copper	120	—
M	8-Pin Mini DIP	Copper	80	55
Q	16-Pin Quad In-Line	Copper	45	13*
R	14-Pin CerDIP	Kovar	75	—
R	16-Pin CerDIP	Kovar	75	—
R	18-Pin CerDIP	Kovar	65	—
W	12-Lead Power Tab SIP	Copper	24	3.0*
Y	3-Lead Plastic Transistor	Copper	310	170
Z	5-Lead Power Tab SIP	Copper	40	4.5*

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specification takes precedence.

†$G\Theta_{JA} = 1/R\Theta_{JA}$ and $G\Theta_{JC} = 1/R\Theta_{JC}$

*$R\Theta_{JT}$

Operating and Handling Practices for MOS Integrated Circuits

Handling Practices — Packaged Devices

Sprague Electric incorporates input protection diodes in all of its MOS/CMOS devices. Because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.
2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.
3. Devices should not be inserted into or removed from test stations unless the power is off.
4. Neither should signals be applied to the inputs while the device power supply is in an off condition.
5. Unused input leads should be committed to either V_{SS} or V_{DD}.

Handling Practices — Die

A conductive carrier should be used in order to avoid differences in voltage potential.

Automatic Handling Equipment

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aide here and are available commercially. This method is very effective in eliminating static electricity problems.

Ambient Conditions

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

Alert Failure Modes

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.
2. Shorted or 'blown' open gates.
3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

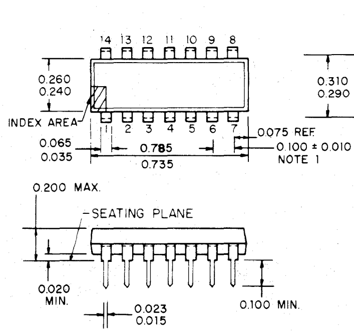
MOUNTING OF POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. "Brute Force" mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass/filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

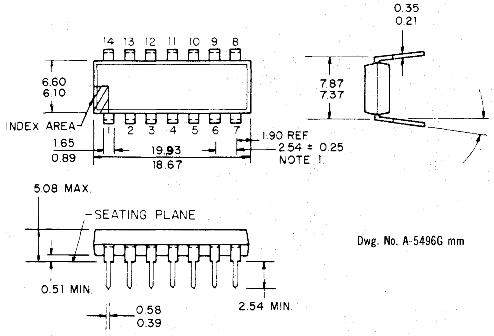
'A' PACKAGE: 14-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



Dwg. No. A-5496G in

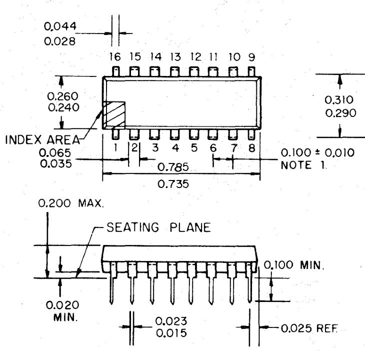
DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm



Dwg. No. A-5496G mm

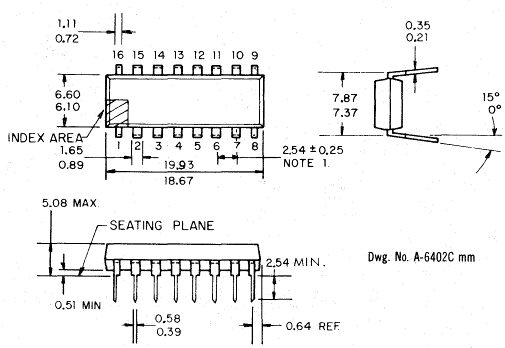
'A' PACKAGE: 16-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



Dwg. No. A-6402C in

DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm



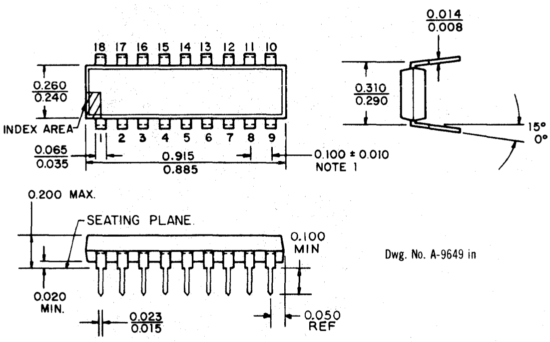
Dwg. No. A-6402C mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

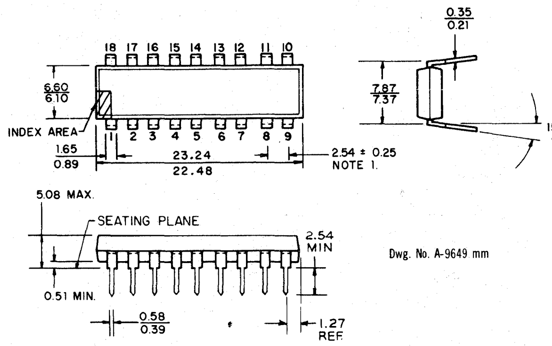
12

'A' PACKAGE: 18-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

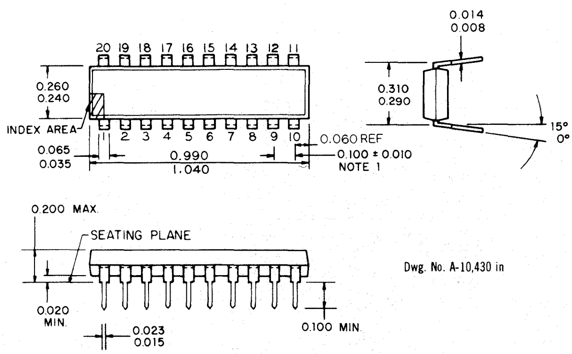


DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm

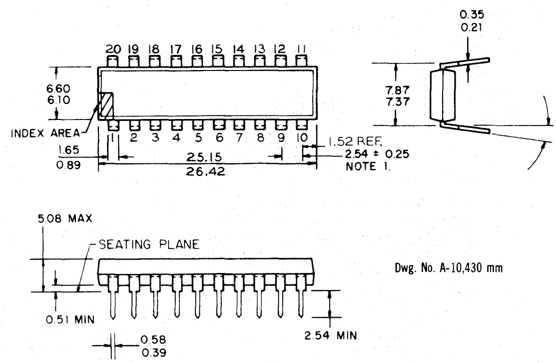


'A' PACKAGE: 20-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



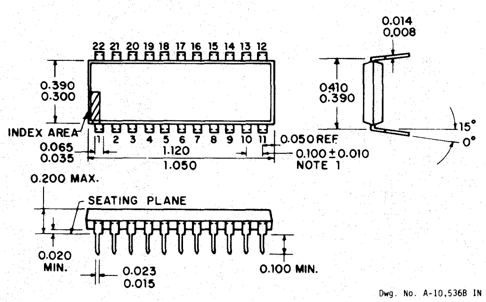
DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm



NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

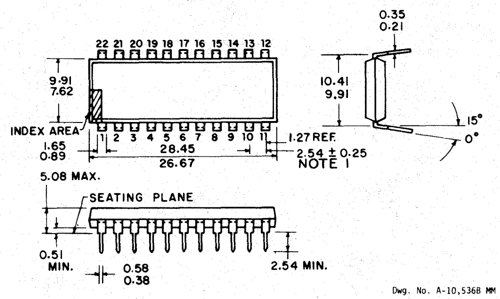
'A' PACKAGE: 22-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



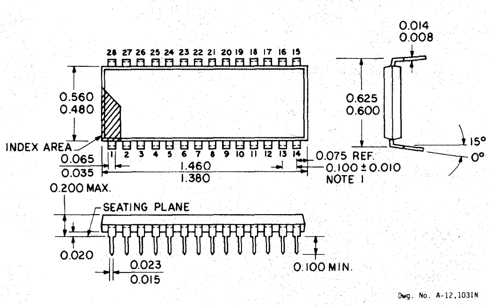
DIMENSIONS IN MILLIMETRES

Based on 1″ = 25.4 mm



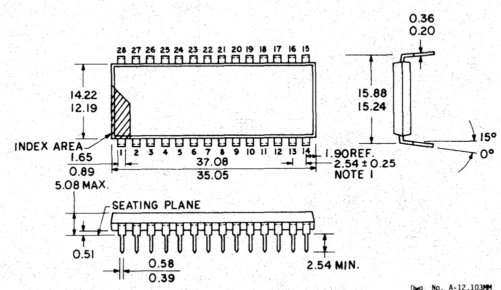
'A' PACKAGE: 28-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



DIMENSIONS IN MILLIMETRES

Based on 1″ = 25.4 mm



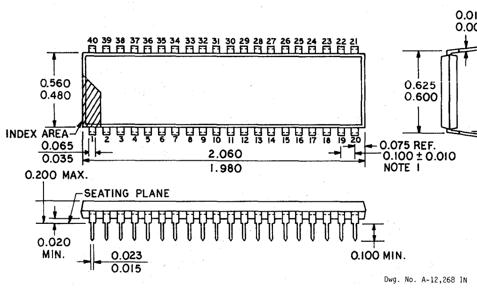
NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

12

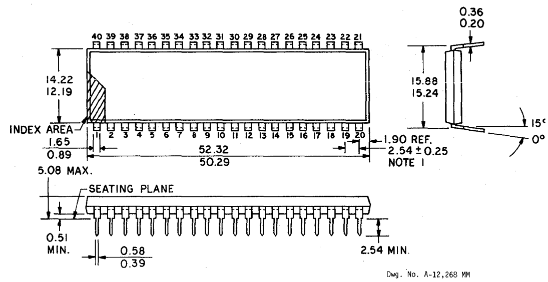
'A' PACKAGE: 40-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



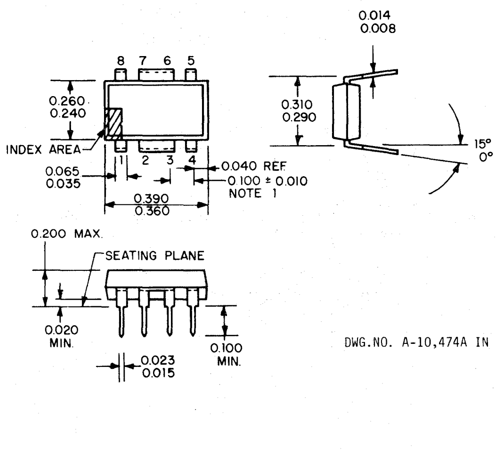
DIMENSIONS IN MILLIMETRES

(Based on 1 in. = 25.4 mm)



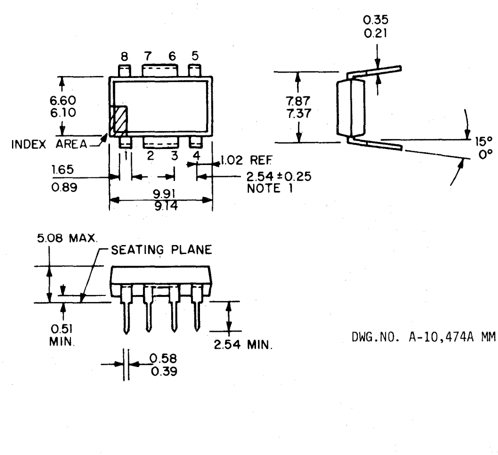
'B' PACKAGE: 8-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



DIMENSIONS IN MILLIMETRES

(Based on 1 in. = 25.4 mm)

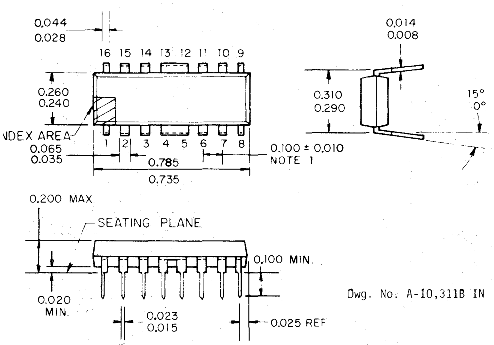


NOTES:

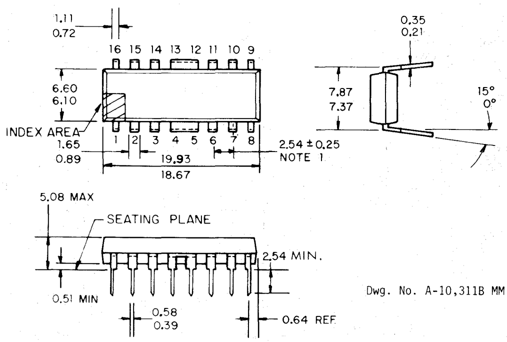
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

'B' PACKAGE: 16-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

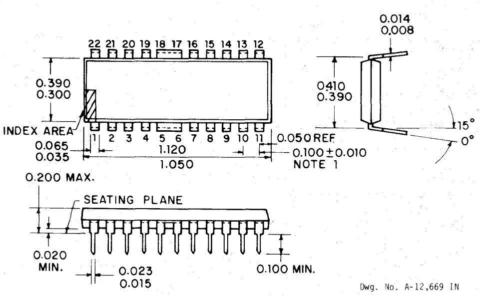


DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm

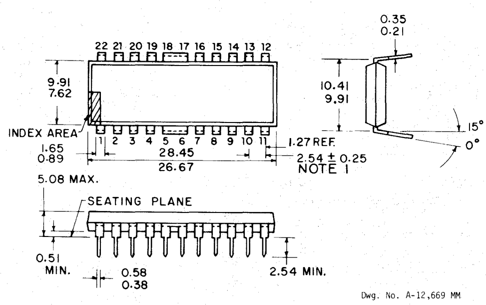


'B' PACKAGE: 22-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



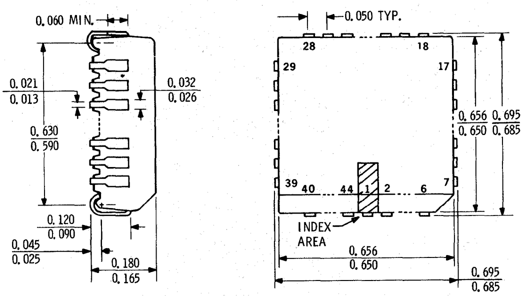
DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)



NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

'EP' PACKAGE: 44-Lead Plastic Leaded Chip Carrier (PLCC)

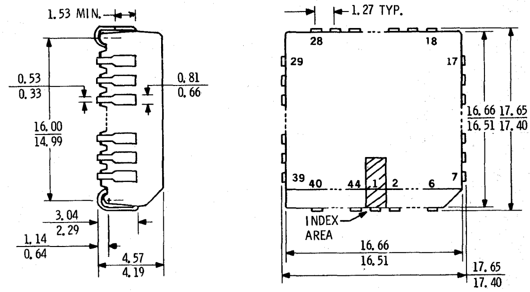
DIMENSIONS IN INCHES



Dwg. No. A-12,664 IN

DIMENSIONS IN MILLIMETRES

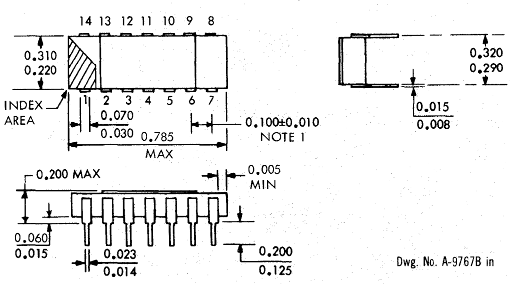
(Based on 1 in. = 25.4 mm)



Dwg. No. A-12,664 MM

'H' PACKAGE: 14-Pin Hermetic Dual In-Line

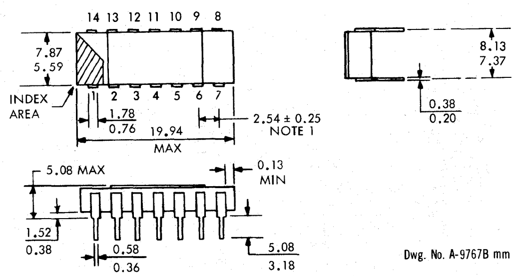
DIMENSIONS IN INCHES



Dwg. No. A-9767B in

DIMENSIONS IN MILLIMETRES

(Based on 1 in. = 25.4 mm)



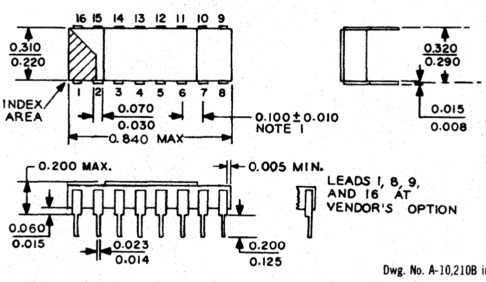
Dwg. No. A-9767B mm

NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

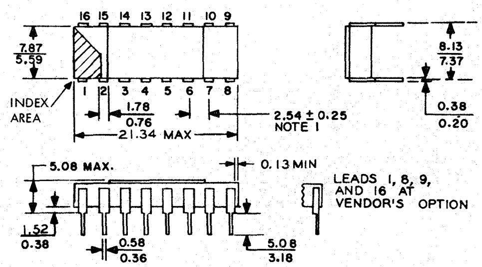
'H' PACKAGE: 16-Pin Hermetic Dual In-Line

DIMENSIONS IN INCHES



Dwg. No. A-10,210B in

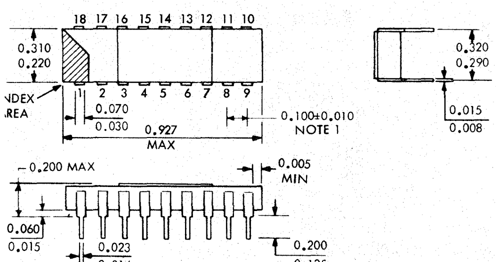
DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm



Dwg. No. A-10,211B mm

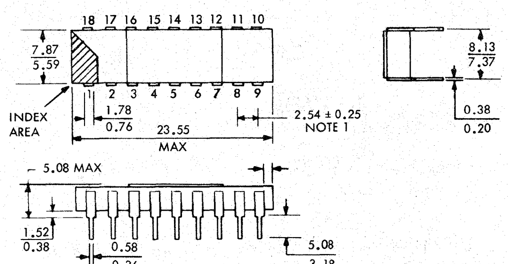
'H' PACKAGE: 18-Pin Hermetic Dual In-Line

DIMENSIONS IN INCHES



Dwg. No. A-10,312A in

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm



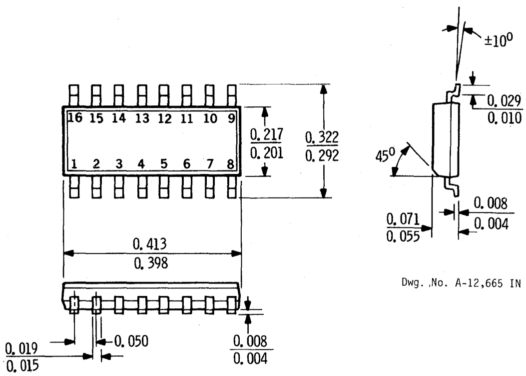
Dwg. No. A-10,312A mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

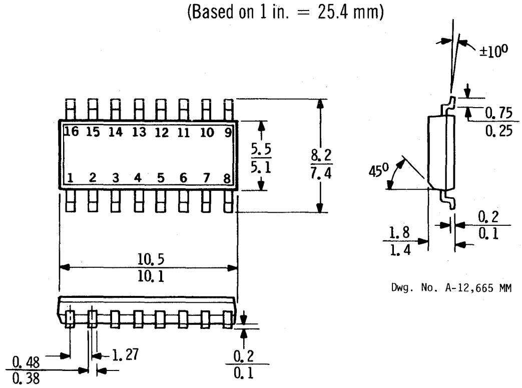
12

'L' PACKAGE: 16-Lead Small Outline (SOIC)

DIMENSIONS IN INCHES

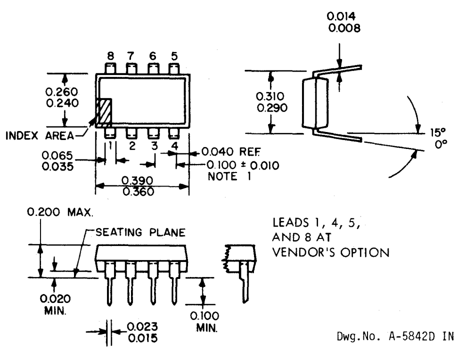


DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)

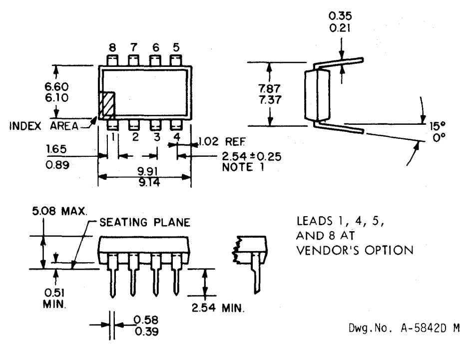


'M' PACKAGE: 8-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES



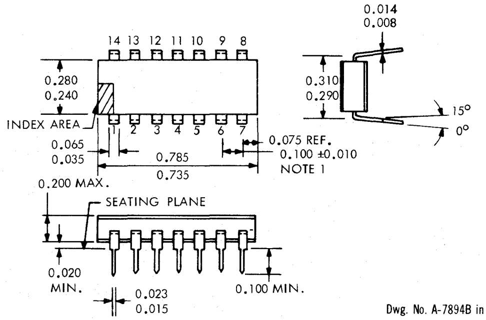
DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)



NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

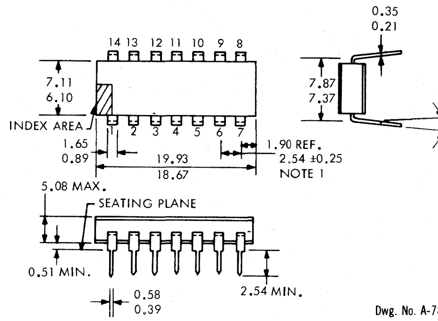
'R' PACKAGE: 14-Pin Ceramic Dual In-Line

DIMENSIONS IN INCHES



Dwg. No. A-7894B in

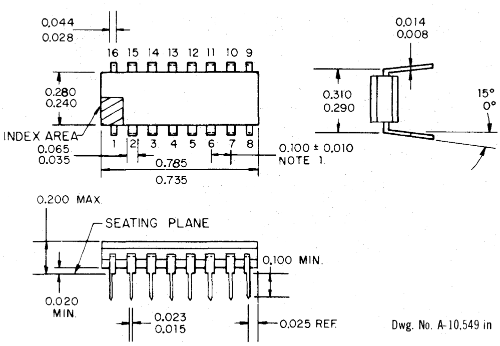
DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)



Dwg. No. A-7894B mm

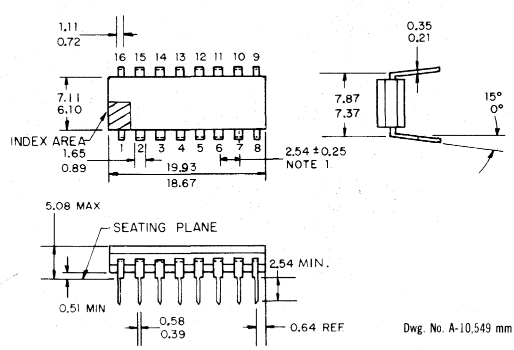
'R' PACKAGE: 16-Pin Ceramic Dual In-Line

DIMENSIONS IN INCHES



Dwg. No. A-10,549 in

DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)



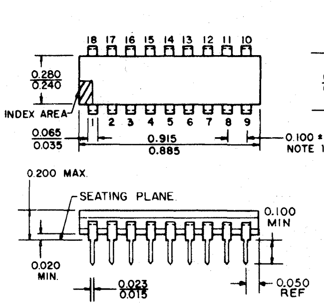
Dwg. No. A-10,549 mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

12

'R' PACKAGE: 18-Pin Ceramic Dual In-Line

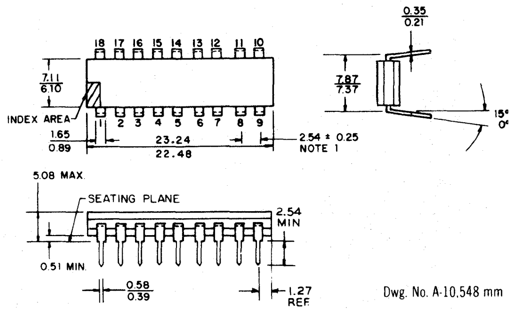
DIMENSIONS IN INCHES



Dwg. No. A-10,548 in

DIMENSIONS IN MILLIMETRES

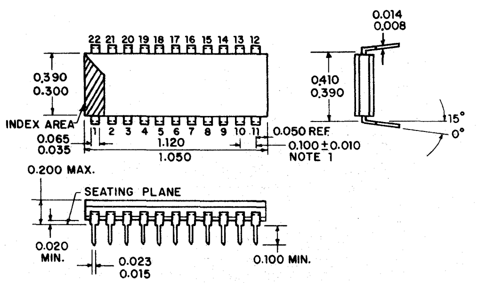
(Based on 1 in. = 25.4 mm)



Dwg. No. A-10,548 mm

'R' PACKAGE: 22-Pin Ceramic Dual In-Line

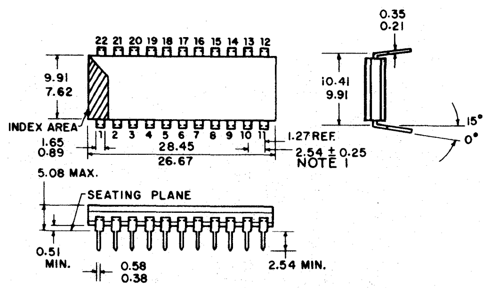
DIMENSIONS IN INCHES



Dwg. No. A-11,620 IN

DIMENSIONS IN MILLIMETRES

(Based on 1 in. = 25.4 mm)

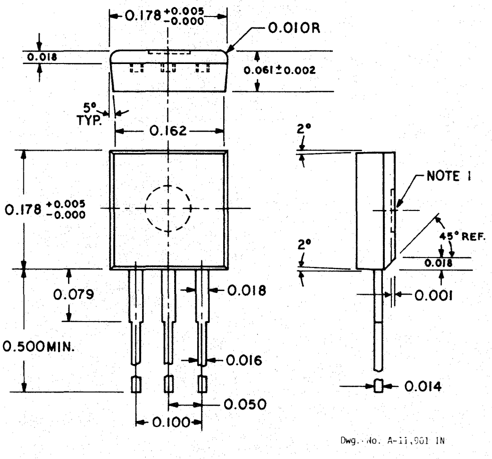


Dwg. No. A-11,620 MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

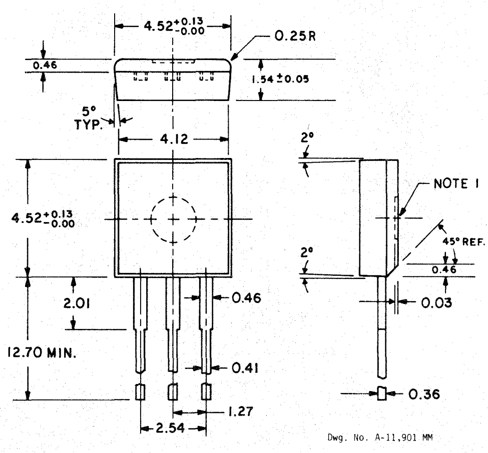
'U' PACKAGE: 3-Pin Plastic Single In-Line

DIMENSIONS IN INCHES



DIMENSIONS IN MILLIMETRES

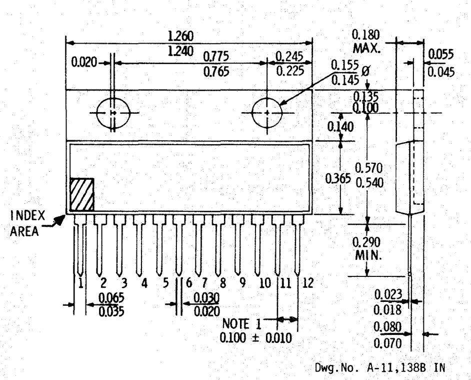
Based on 1″ = 25.4 mm



NOTE: Lead diameter is controlled in the zone between 0.050″ (0.13 mm) and 0.250″ (6.35 mm) from the seating plane. Between 0.250″ (6.35 mm) and 0.500″ (12.7 mm) from the seating plane, a maximum lead diameter of 0.021″ (0.53 mm) is specified. Outside of these zones the lead diameter is not controlled.

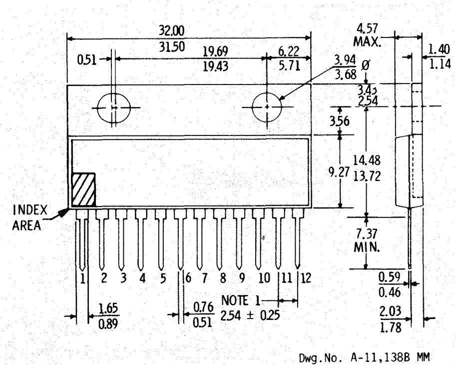
'W' PACKAGE: 12-Pin Plastic Single In-Line

DIMENSIONS IN INCHES



DIMENSIONS IN MILLIMETRES

Based on 1″ = 25.4 mm



NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

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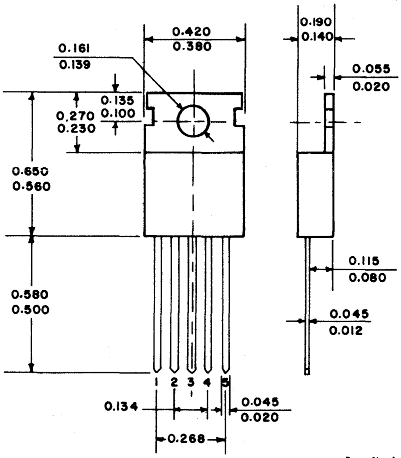
'Z' PACKAGE: 5-Lead TO-220

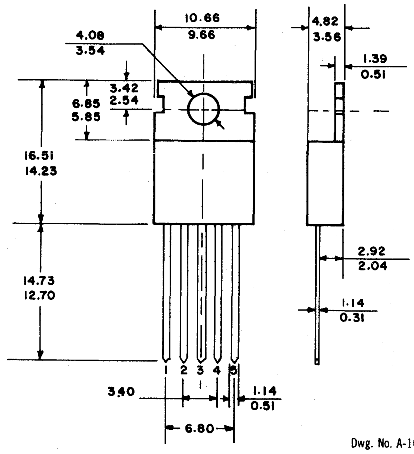
DIMENSIONS IN INCHES



Dwg. No. A-10,460 in

DIMENSIONS IN MILLIMETRES

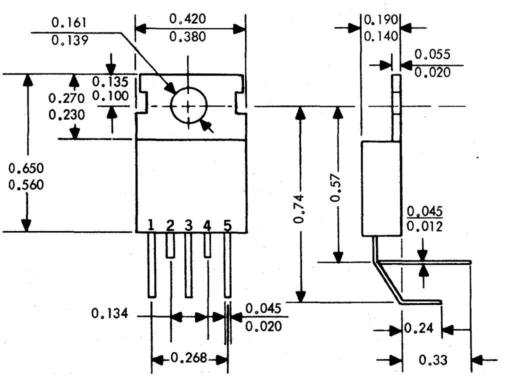
Based on 1″ = 25.4 mm



Dwg. No. A-10,460 mn

'ZH' PACKAGE: 5-Lead TO-220 (Horizontal Mount)

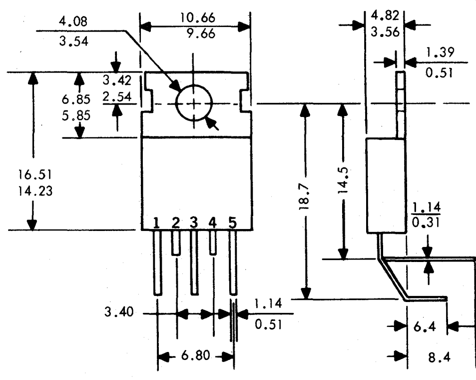
DIMENSIONS IN INCHES



Dwg. No. A-10,462B IN

DIMENSIONS IN MILLIMETRES

Based on 1″ = 25.4 mm



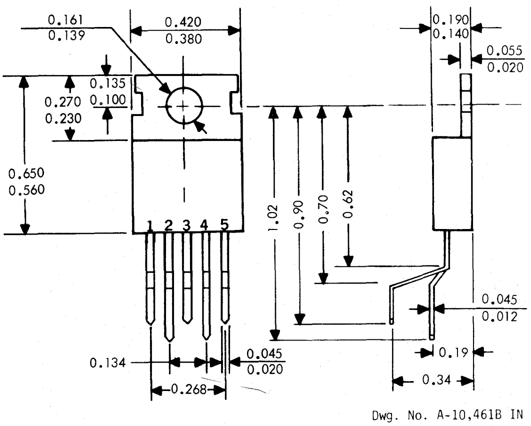
Dwg. No. A-10,462B MM

NOTES:

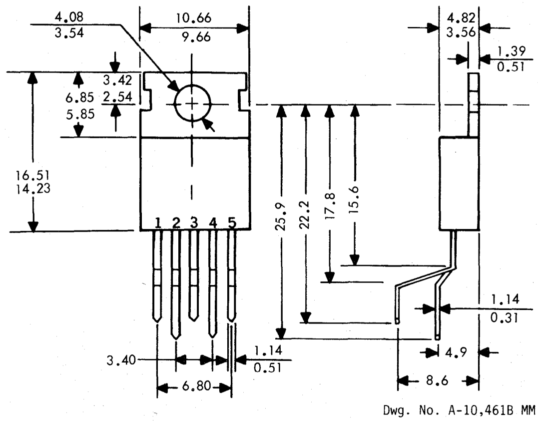
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

'ZV' PACKAGE: 5-Lead TO-220 (Vertical Mount)

DIMENSIONS IN INCHES



DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm



NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

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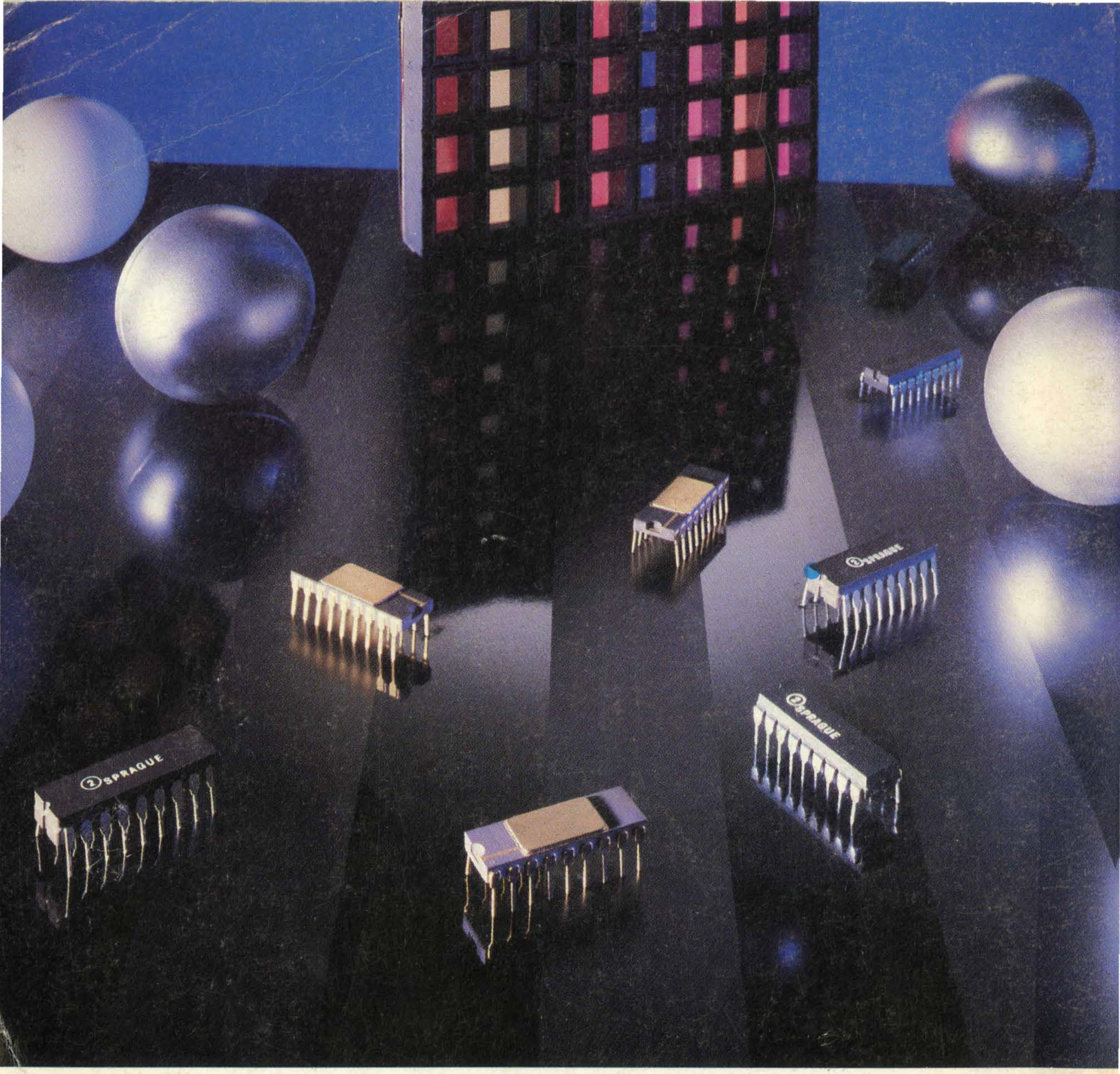

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