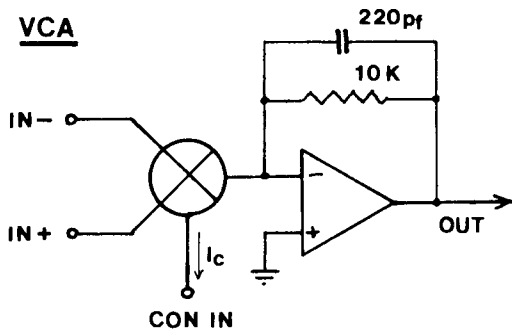
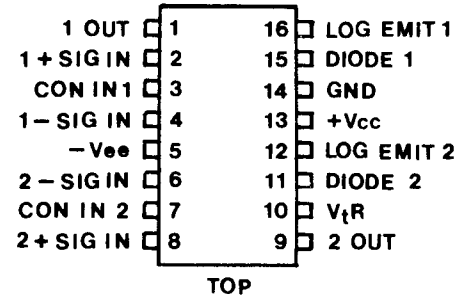


# DUAL LINEAR-ANTILOG VOLTAGE CONTROLLED AMPLIFIER

The SSM 2000 is a dual two-quadrant multiplier, each channel having separate control and differential signal inputs and a current output. In addition to linear amplitude control, on chip logging elements have been provided for producing an antilog control characteristic at the option of the designer. The device may be used in a wide variety of audio frequency applications including Voltage Controlled Amplifiers, Mixdown Panels and as a Biquad Tuning Element. Both channels are temperature compensated and each channel has an 80 db range.

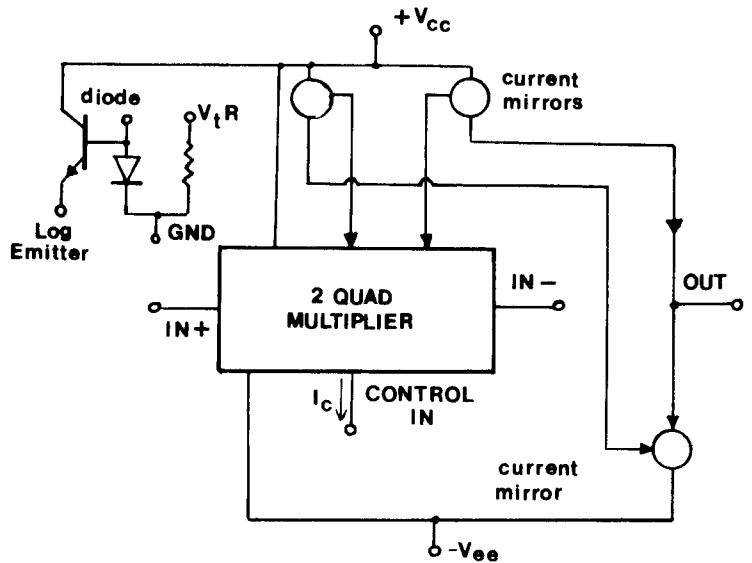


**APPLICATIONS**

- Voltage Controlled Filters
- Two and Four Quadrant Multipliers
- Audio Mixdown Panels
- AGC Circuits
- Voltage Controlled Current Sources and Sinks
- Antilog Amplifiers and Expanders
- Voltage Controlled Quadrature Oscillators

**FEATURES**

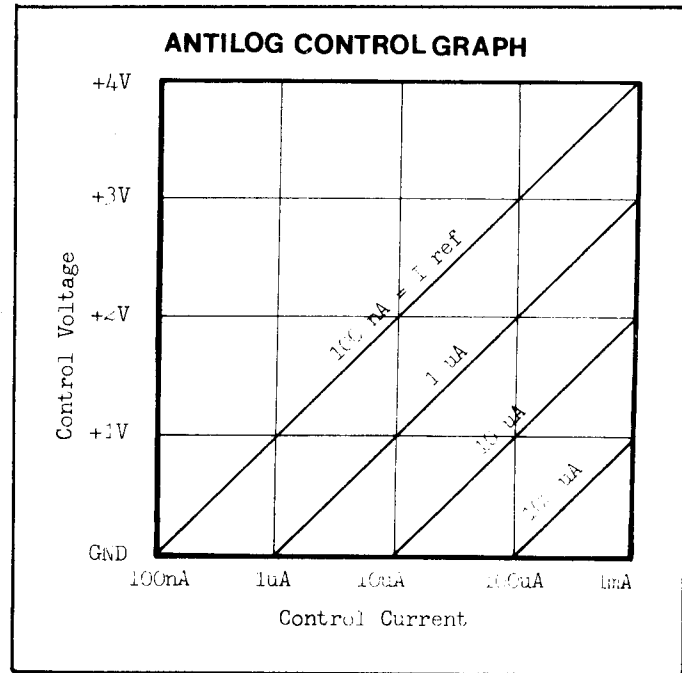
- Linear or Antilog Control Characteristics
- 80 db Control Range
- Excellent Control Accuracy (1% or better over the entire control range)
- Dual Design (completely independent selection of control characteristics)
- Internal Temperature Compensation
- Current Output
- Differential Signal Inputs
- 200 Nanoamp Input Bias Current
- Low Noise
- Low Distortion



**EQUIVALENT SCHEMATIC [ONE SIDE]**

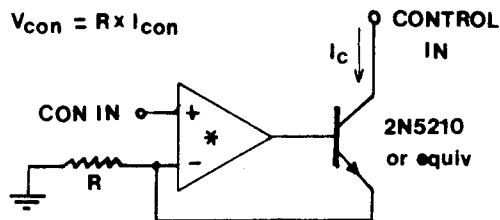
## SPECIFICATIONS

	Min	Typ	Max
<u>Signal Input Bias Current</u>	-	200nA	400nA
<u>Noise Sig/Noise@10Vpp</u>	-	<b>84db</b>	-
<u>Channel Matching</u>			
a - Linear	-	1%	2.5%
b - Antilog	-	2.5%	10%
<u>Channel Separation</u>	-	<b>100db</b>	-
<u>Supply Voltage</u>	± 6V	± 10V	± 12V
<u>Control Current</u>	-	-	1 mA
<u>Input Resistance</u>	50 Meg	100 Meg	-
<u>Output Offset Current</u>			
I offset/I control	-	2%	-
<u>Supply Current</u>			
@ I control = 1 mA	-	10 mA	12mA
<u>Signal Input Voltage</u>	$V_{ee} + 4.0V$	-	$V_{cc} - 2.5V$
$V_t$ Resistor	600	650	800
$V_t$ Temp. Comp.	-	+2000ppm/C°	-
<u>Distortion (THD)</u>			
@ 1 Vpp Sig In	-	0.1 %	-

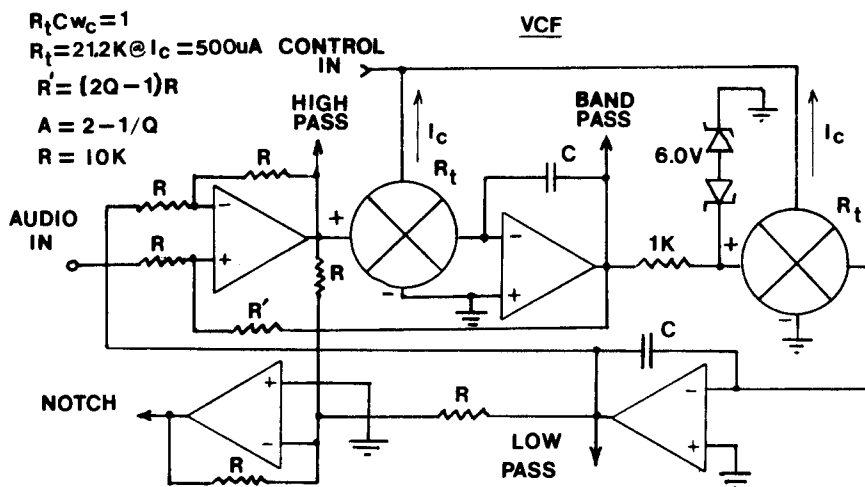
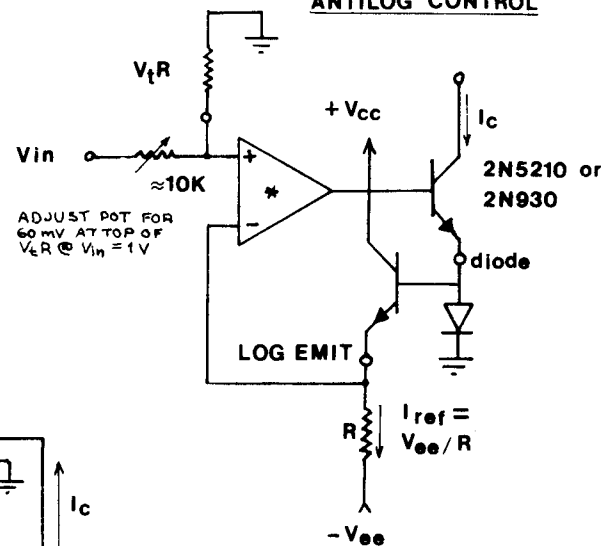


### LINEAR CONTROL (non inverting)

$$V_{con} = R \times I_{con}$$



### ANTILOG CONTROL



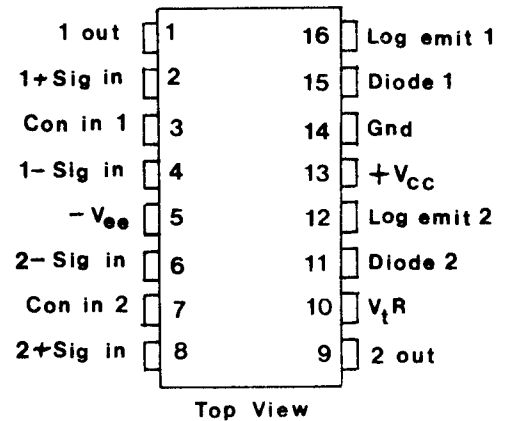
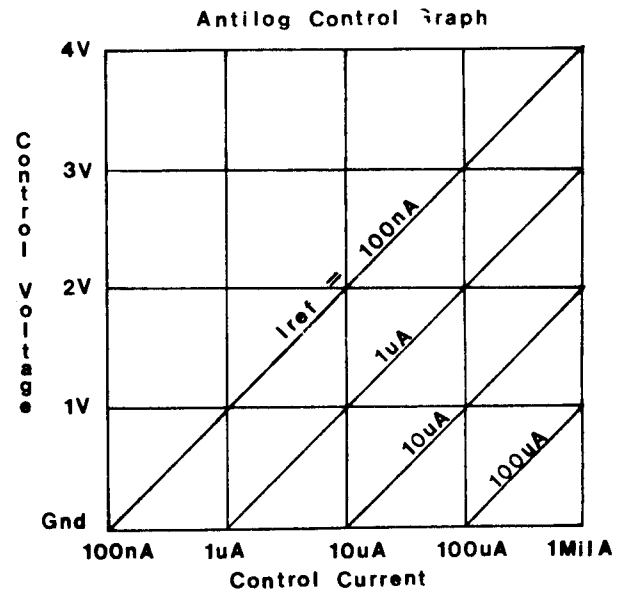
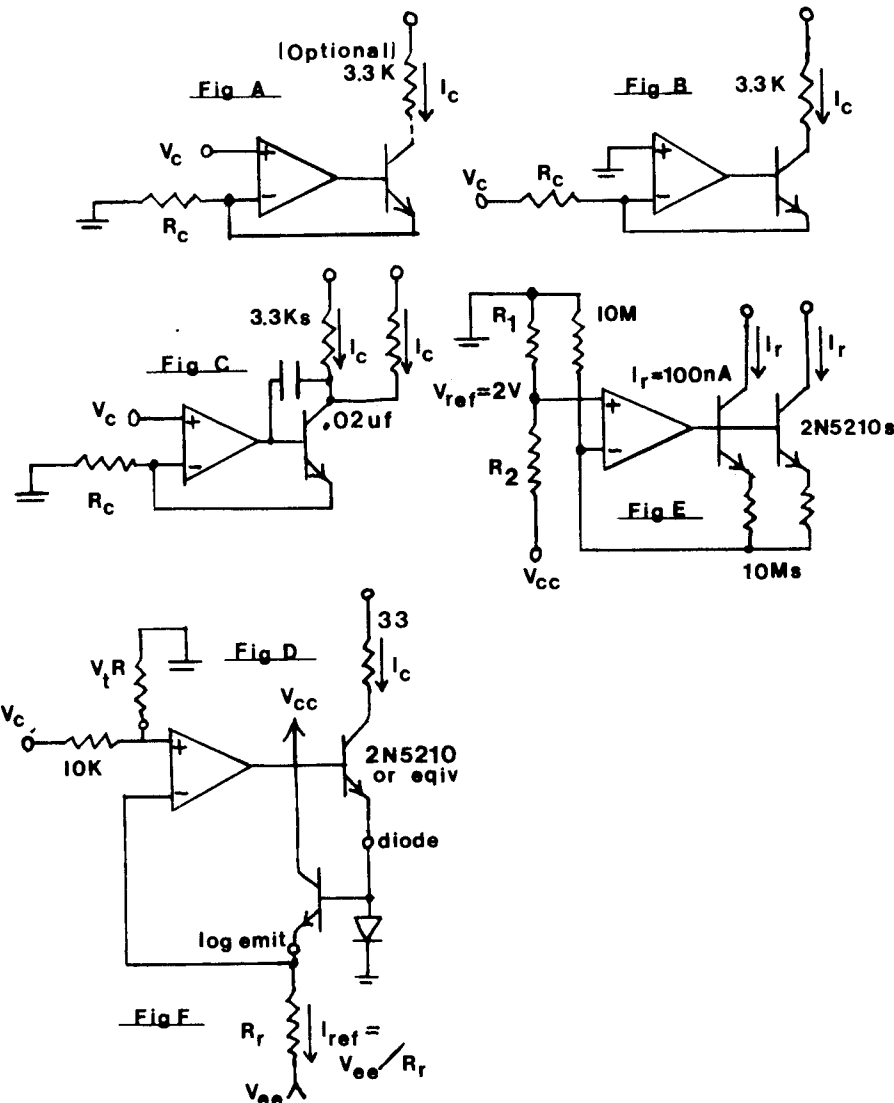
\* CONTROL OP AMPS (For 80db range):  
LM 308, Tele grey 614,  
MC 1158, or FET input.

### Control Circuits

To produce a linear control of amplification in the SSM2000, a linear voltage to current converter is used to supply an output control current from an input voltage. The circuit in Fig. A is used for a positive control voltage ( $V_C/R_C = I_C$ ), and Fig. B for a negative voltage ( $-V_C/R_C = I_C$ ). The resistor in these circuits should be chosen so that the maximum desired input voltage will produce an output current of 1 Mil. The Fig. A circuit has the advantage of higher input impedance and in Fig. B a larger control voltage can be used without running into the bias voltage on the control pin ( $V_{CC} - 4V$ ). To "gang" the gain of both halves of the I.C to the same control voltage, the circuit in Fig. C is used. The 3.3K resistors force a match in the control currents in both amps and also offer current limiting. For the latter reason, it may be a good idea to include such a resistor in circuit B, and also in circuit A if a small  $R_C$  is selected.

Antilog control of gain is achieved by the exponential voltage to current converters in Fig. D. The graph at the bottom of the page shows the Antilog  $I_C$  to  $V_C$  in relationship at various reference currents. As can be seen from the graph, the range of control is determined by the reference current which is set up by the circuits in Figs. E and F; 80 db for  $I_{ref} = 100$  nA etc. The scale factor, 1 decade per volt, is determined by the attenuator which in this case gives 60 mV at the op amp non-inverting input for 1 Volt at the control input. In the more general case:

$$\ln(I_C/I_{ref}) = R_1 V_{in}/(R_1 + R_2) \cdot V_t \quad V_t = kT/q$$



As one can see this expression is temperature sensitive. This effect can be largely cancelled if the  $V_t$  resistor provided on the chip is used for  $R_1$ . With this resistor an 80db control range can be used with a  $\pm 10\%$  error due to temperature over the span from  $10^\circ\text{C}$  to  $45^\circ\text{C}$ . This worst case error will occur for the largest control current in the range. An ordinary resistor can be used as  $R_1$  for room temperature applications ( $25^\circ\text{C} \pm 10^\circ\text{C}$ ) with only a 10% error if the control range is restricted to 40db. (100 to 1). An ideal temperature compensating resistor would have a temperature coefficient of  $3300\text{ppm}/^\circ\text{C}$ . If extremely precise  $V_t$  temperature compensation is required in the antilog control mode, a Tel Labs Type Q81 resistor or equivalent can be used in place of the on chip  $V_t$  resistor. Another alternative is to use a Fairchild uA726 Temperature Controlled Differential pair in place of the on chip logging elements. In this case, no  $V_t$  resistor is required.

If a control range of 60db or greater is desired, a low input bias op amp such as the LM 308 or the Teledyne 844 should be used in the V to I converter with a low leakage output transistor such as a 2N5210 or a 2N930. As with the linear inverting control circuit, a 3.3K resistor is placed in a series with the collector of the output transistor for current limiting. To gang both amplifiers to the same control voltage, the circuit in Fig. G is used.

#### VCA

Fig. H shows half of the SSM2000 used as a voltage controlled amplifier. The output voltage is related to the input voltages and control current by:

$$V_{out} = I_{con} (V_+ - V_-) R_F / 1.06 \times 10^1$$

A linear or antilog voltage to current converter sets the control current and the op amp converts the output current to an output voltage. The capacitor in parallel with the feedback resistor is necessary to prevent oscillation. For a 10K feedback resistor, 150 to 220pf should be sufficient, giving a bandwidth of about 100KHZ.

#### ANTILOG VCA WITH 130db CONTROL RANGE

In Fig. I, both halves of the SSM2000 are cascaded to produce an antilog amplifier with a 130db control range. The control current in each half of the device varies only from  $500\mu\text{A}$  to  $250\text{nA}$ , making it possible to maintain a signal bandwidth in excess of 50KHZ down to the extreme low end. The control circuit is designed to provide 10db of gain per volt; the .02uf capacitor was found necessary to prevent oscillation. If the input signal level is kept at 3 volts peak to peak, the signal to noise ratio is 68db and distortion will be less than 0.3%.

#### Four Quadrant Multiplier

In Fig. J half of a SSM2000 is used as a four quadrant multiplier. The output current into a virtual ground is:

$$I_{out} = -V_1 V_2 / R_C (1.06 \times 10^1)$$

To adjust the circuit for proper operation, a signal is applied to the  $V_2$  input with  $V_1$  grounded and  $R_p$  trimmed for minimum feedthrough.  $V_2$  is then grounded, a signal applied to  $V_1$  and  $R_F$  trimmed for minimum feedthrough which should occur when:

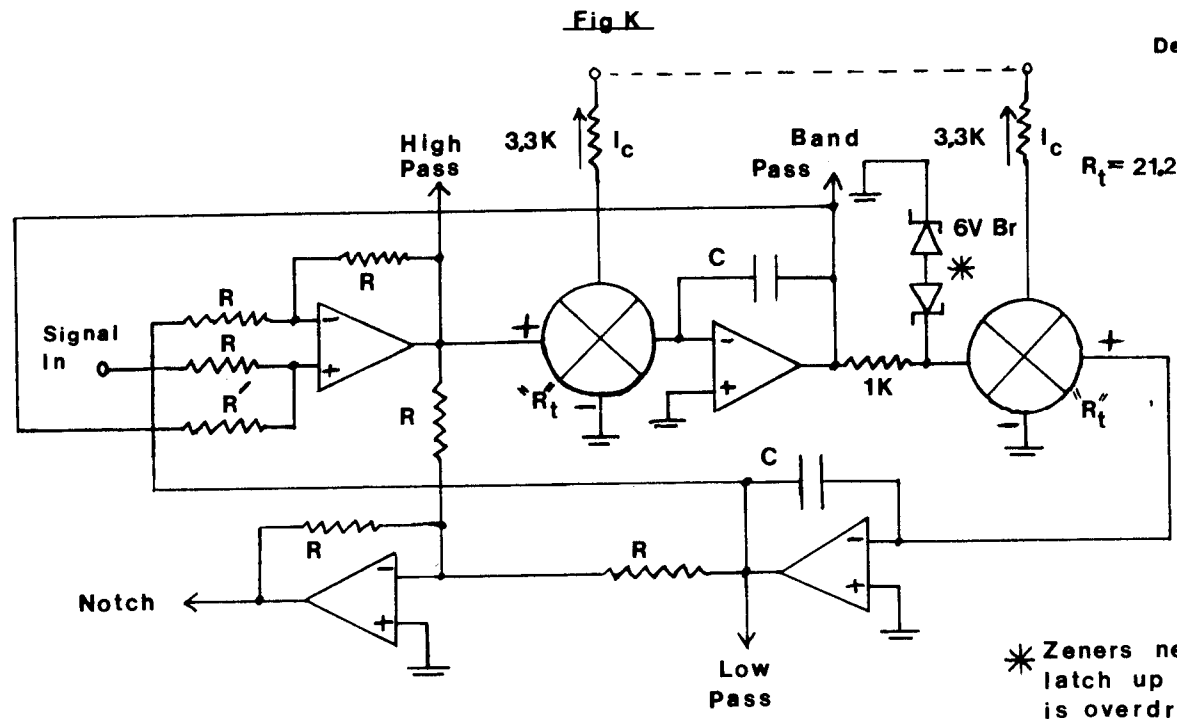
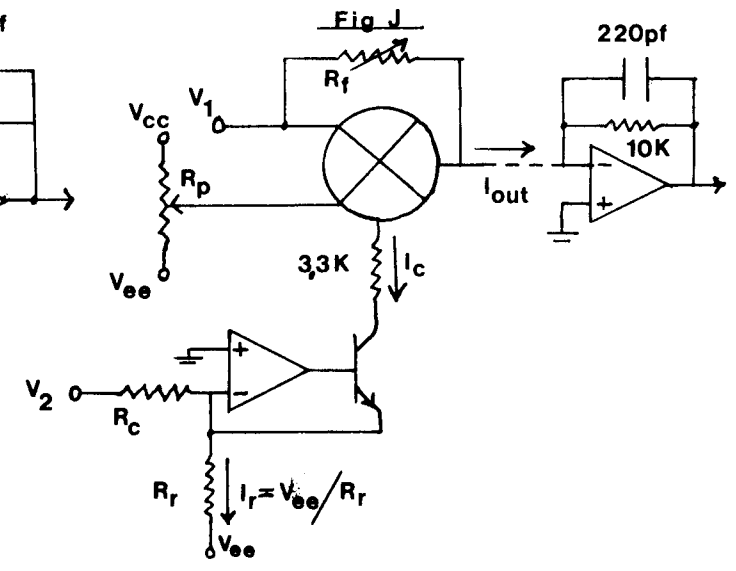
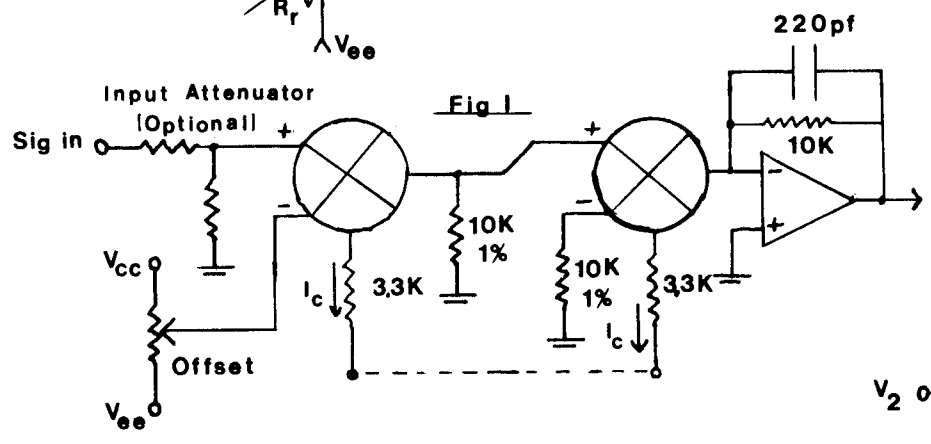
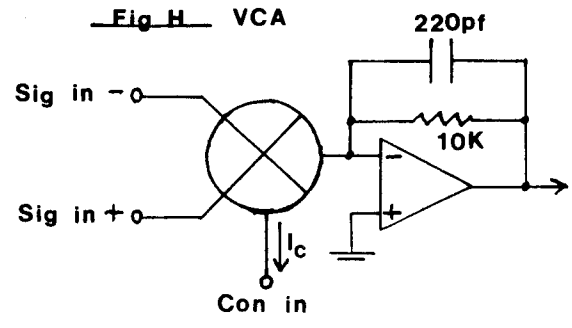
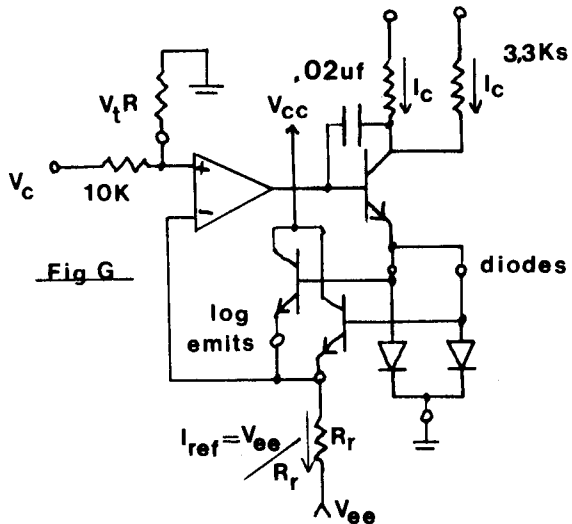
$$R_F = 1.06 \times 10^1 / I_{ref}$$

A maximum bandwidth of about 250KHZ will be obtained with  $I_{ref} = 200\mu\text{A}$ . The op amp circuit used with the VCA can be added to convert the output current to a buffered voltage.

#### Voltage Controlled Filter

Using the circuit in Fig. K a voltage controlled filter with a 10,000 to 1 control range can be implemented. The low and high pass outputs have 12db/octave rolloffs, the band pass output has 6db/octave skirts and the notch output has a sharp null at the cutoff frequency. Such circuits can be series to produce more complex filters. In this application the SSM2000 can be thought of as a pair of matched voltage controlled resistors. The  $R_T$  in the design equation for the cutoff frequency given next to the figure is 10.6K when the control current in both halves of the device is 1 Mil. At  $100\mu\text{A}$  control current, the value of the  $R_T$  will increase to 106K and so forth. For control ranges of 1000 to 1 or greater, low input bias op amps should be used in the control circuit and signal section of the filter. The MC1456 and the Teledyne 844 perform well in the signal section offering low input bias, low noise and wide power bandwidth. If antilog control is used, the greatest control accuracy for a 1000 to 1 range is obtained for control currents of  $250\text{nA}$  to  $250\mu\text{A}$ .

(For other filters that can be used with the 2000 see J Tow, "A Step by Step Active Filter Design" IEEE Spectrum, pp64-68, Dec. 1969).



VCF  
Design Equations

$$R = 10K$$

$$R_t C \omega_0 = 1$$

$$R_t = 21.2K @ I_c = 500\mu A$$

$$R' = |2Q - 1|R$$

$$A = 2 - 1/Q$$

\* Zeners needed to prevent latch up when circuit is overdriven.

Voltage Controlled Quadrature Oscillator

The voltage controlled oscillator circuit shown in Fig. L is very similar to the voltage controlled filter. An extremely low distortion sine wave (approximately .04%) can be produced using this circuit. As in the filter, the SSM2000 is used as a pair of voltage controlled resistors to tune a biquad stage. All the design tips given for the VCF also apply here. The design procedure is:

Specify:

- GB (Gain bandwidth product of op amps in Hz)
- P<sub>o</sub> (Output power in dbm)
- R<sub>o</sub> (Circuit impedance in ohms)
- f<sub>o</sub> (Center frequency in Hz)
- D<sub>o</sub> (Total harmonic distortion in db)

- 3) Peak limiter voltage;  $V_{lp} = 2V_{po} \pi / r$
- 4) Q setting resistor;  $R = r / 16\pi C f_o$
- 5) C: f<sub>o</sub> capacitor;  $R_2 = R_3 = 1 / (2\pi C f_o) = 21.2K @ I_c = 500\mu A$
- 6) R<sub>7</sub> & R<sub>8</sub>;  $R_7 = R_8 = 100(V_{cc} - 0.6 - V_{lp}) / V_{lp}$
- 7) C<sub>c</sub>;  $C_c = 4 / (2\pi GB \cdot R_3)$

Find:

- 1) Peak output voltage;  $V_{po} = (R_o / 500)^{1/2} \cdot 10^{(P_o / 20)}$
- 2) Transfer ratio;  $r = 10^{((D-9)/20)} = 8Q$

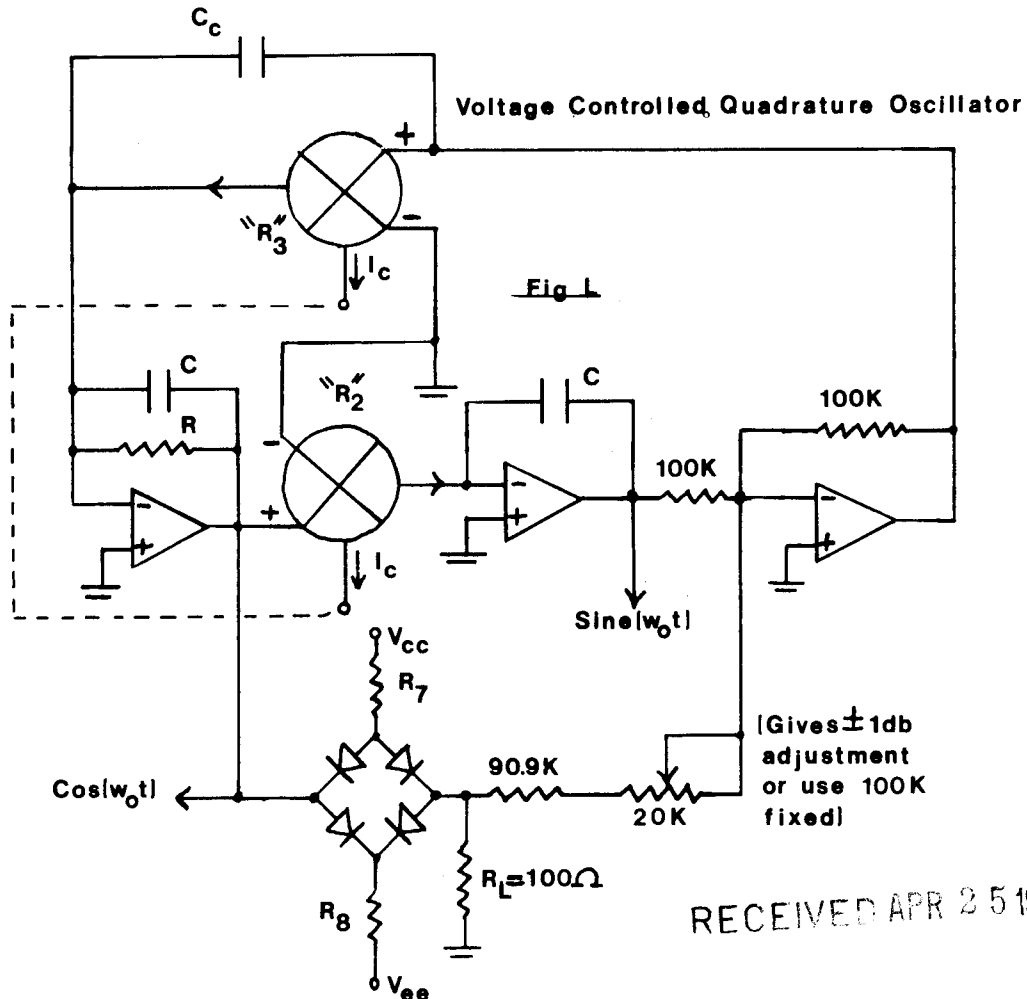
Noise, Distortion and Offset

The output signal to noise ratio of the 2000 into a 10K metal film resistor with an input signal of 3 volts peak to peak is 72db independent of the control current.

The total harmonic distortion is linearly dependent on the input signal amplitude. Typical values are 1% with a 10 volt peak to peak signal and 0.1% with a 1 volt signal, etc.\*

Offset in the 2000 is best thought of referred to the output rather than the signal inputs. Due to the nature of the design, the D.C. offset appearing at the output will be a small fraction of the control current. Typically, 2% with both signal inputs grounded. If the control current is kept under 500uA, the offset can be trimmed out by a pot stretched between the supplies and with the wiper connected to one of the signal inputs.

\*Note; If the circuits in figures C or G are used as control circuits to gang both sides of the SSM2000 to the same control voltage, the distortion figure is doubled and includes some second harmonic distortion. Using two control circuits with a common input will avoid this.



# THE GILBERT MULTIPLIER IN ELECTRONIC MUSIC:

-by Dave Rossum, Ep Systems, 3046 Scott Blvd., Santa Clara, CA 95050

Most ELECTRONOTES readers are familiar with the RCA CA3080 and its uses as a gain controlled stage in forming voltage controlled amplifiers and filters. The CA3080 has its problems, as many readers have no doubt discovered. Some of these come from process variations, mostly due to the fact that the PNP transistors used in the positive rail current mirrors have betas of around 10, which, when the processing is poor, can go to more like 5. But even at their best, 3080's used in VCA applications are noisy and cause significant distortion.

The 3080 type multiplier, whether discrete (see ENS-73 design for VCA by Dave Rossum) or integrated, uses a differential input stage such as that shown in figure 1. The two output currents,  $I_1$  and  $I_2$  are then subtracted and converted to a voltage, either by the current mirror arrangement in the 3080 chip or by a differential amplifier in the discrete design. The resulting theoretical transfer equation for the circuit is then:

$$V_o = R I_c [ e^{\lambda(V^+ - V^-)} - 1 ] / [ e^{\lambda(V^+ - V^-)} + 1 ] \quad \lambda = q/kT$$

Thus we see that the circuit is by no means linear, and to avoid gross distortion the input voltage to the transistor bases of the input stage must be kept small. We have typically been using the attenuation of 100K to 220 ohms into the stage; at 10V p/p this gives a distortion of 1.3%. If we assume 10 microvolts of noise at the transistor base, this gives also a worst case signal to noise ratio of 66 dB, for the same 10V p/p signal.

Obviously, if we could improve the theoretical transfer characteristic to a more linear form, we could improve the distortion. If instead we chose to increase our signal level to the transistor bases, we could use the improved distortion to instead lower the noise. Fortunately, a circuit with such an improved transfer characteristic exists - it is called a Gilbert multiplier.

The Gilbert multiplier derives its improved performance by pre-distorting the input signal to our already shown gain control stage. This is done by adding a pair of matched diodes in front of the transistors, and making the input a differential current, as shown in figure 2. The transfer equation is now:

$$V_o = R I_c [ (I^+ / I^-) - 1 ] / [ (I^+ / I^-) + 1 ]$$

Note that if the diodes are on a common substrate with the differential pair, the temperature dependence of the gain disappears!

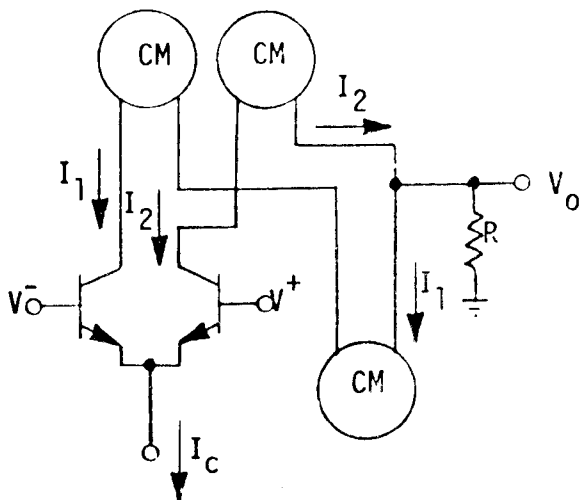


FIGURE 1 - BASIC MULTIPLIER

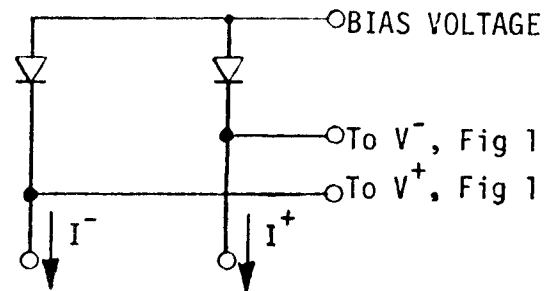


FIGURE 2 - PRE-DISTORTION

This new equation looks a lot more linear. In fact, using the full circuit of figure 3, we find it is linear, ideally linear. The final equation, ignoring the variation in  $V_{be}$  of the input transistors (which really is pretty small) is:

$$V_o = R I_c (V^+ - V^-) / I' R'$$

In fact the  $V_{be}$  variation introduces a very small distortion, about 0.2% for a 10Vp/p signal. But look what we can do to the signals at the various transistor bases. The first input stage has the full 10V p/p across it; with 10 microvolt noisy transistors S/N is 120 dB. The second pair, our old friends, can also have large signals, like 200 mV, for another 20 dB or 86 dB S/N. Much better.

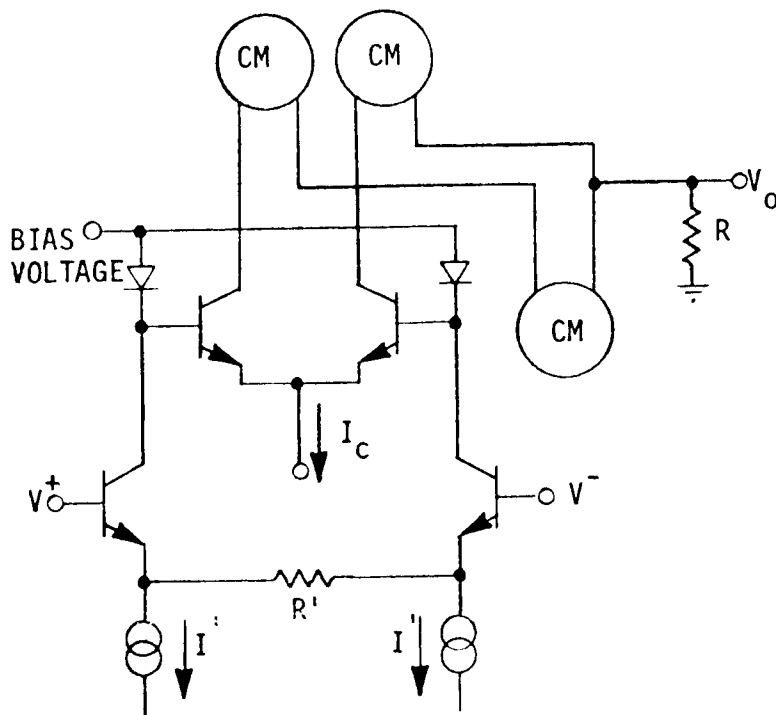


FIGURE 3 - GILBERT MULTIPLIER

What have we paid for all this improvement? Obviously more parts, including some matched pairs. Also the inputs to the amplifier are no longer summing nodes; they require full level signals and any summing must be done by external op-amps. The control input to the input pair no longer floats around with common mode, but stays put and can be easily supplied with current without another current mirror.

The additional parts would be a problem for us little folk, but on an IC they are no problem; matched transistors are cheap and small on chips. A dual 2 quadrant (yes Virginia, 4 quadrant Gilberts have been used for years in the 1495) multiplier chip has been developed by Ron Dow of Exar and is available for sale (see below). It's kind of a neat chip, as it not only has two independent Gilbert VCA's on it, but the extra pins are connected to some matched parts that can be used for exponential generators for controlling the channels, very useful in VCF designs.

Figure 4 shows a basic block diagram of the chip; the quoted specs are in table 1. Bad news: the chip is designed with 24 volt breakdown, and use from  $\pm 15$  volt supplies isn't recommended. However, I've spec checked 8 chips at the higher supply voltage and all worked fine with no noticeable leakage. Talking this over with Ron, we decided that the things "should" work OK at  $\pm 15$ V for most applications, as no NPN collector in the device exceeds 23V in such operation and the spec is 24V min. So use them, but beware.

Figure 5 shows a linear VCA, an exponentially controlled VCA and a VCF, using more or less traditional techniques. Note for the biquad VCF shown, some limiting diodes must be added as the input stage to the Gilbert multiplier is subject to latch-up if overdriven. This diodes won't turn on in normal operation.



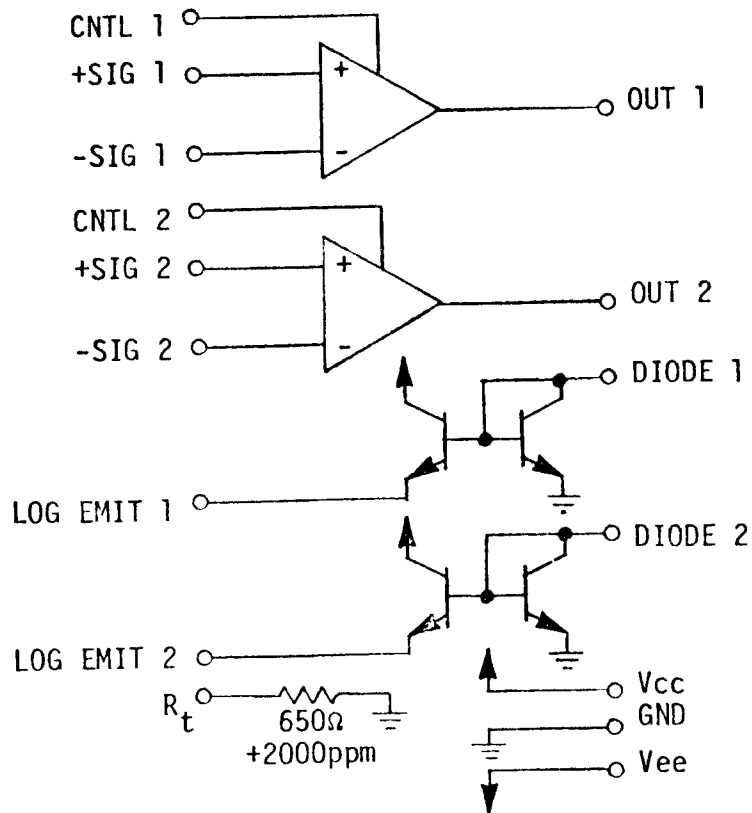


FIGURE 4 - SSM 2000 DUAL VCA

PARAMETER	MIN	TYP	MAX	UNIT
Signal Input Bias Current		200	400	nA
Input Resistance	50	100		MΩ
Signal Input Voltage	Vee+4		Vcc-2.5	V
Noise			-80dB	In/Ic
Distortion (THD) 1V p/p signal		0.2%		
Output Offset Current		2		%Ic
Channel Matching		1	2.5	%
		2.5	10	%
Channel Isolation	100			dB
Control Current			1	mA
Supply Voltage	±6		±12	V
Supply Current		10	12	mA

TABLE 1.

I checked, as mentioned above, a group of these IC's and found a few specs that ought to be reported. The noise was incredibly low, better than 80 dB down (virtually inaudible). The control rejection varied a lot, but averaged about 40 mV for a sweep from 0 to unity gain (about 50 dB). The control rejection in filter circuits was worse, averaging about 500 mV (26 dB) for a 13 octave sweep. One part I got was not totally functional; I cannot vouch for the testing on parts for sale (mine were untested).

If you are interested in purchasing these, the IC is called the SSM 2000, available through Solid State Music, 2102A Walsh Ave., Santa Clara, CA 95050. I don't have firm prices, but was told parts will be about \$6 in ones, dropping in any quantity. Best thing to do is write for a spec sheet and ap notes, and ask about prices.

**Fig. 5** Linear VCA, Exponential VCA, and VCF  
Using SSM2000 Dual VCA

