Sitronix

2004 **DATA BOOK**

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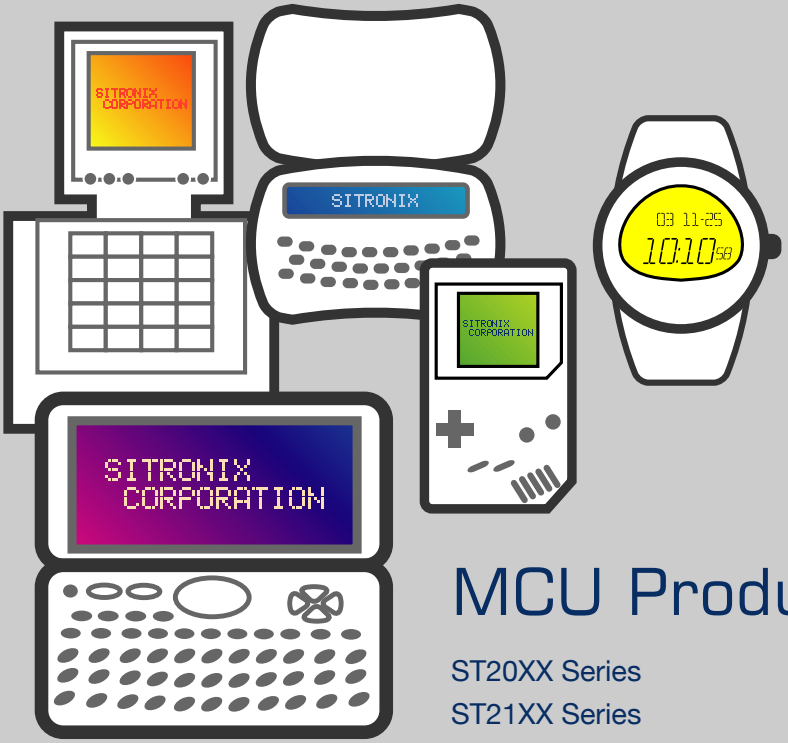
Content



MCU Product Line

ST20XX Series
ST21XX Series
ST22XX Series
ST26XX Series
Low Cost LCD Driver

ST20XX Series

Part No.	ST2006	ST2012	ST2016A/B	ST2024	ST2032A/B	ST2064B	ST20P64
Voltage	2.4~3.6	2.4~5	2.4~3.6	2.4~3.6	2.4~3.6	2.4~5.5	2.6~5.5
RAM	96bytes	192bytes	192bytes	384bytes	1.2Kbytes	2Kbytes	2Kbytes
ROM	6Kbytes	12Kbytes	16Kbytes	24Kbytes	32Kbytes	64Kbytes	64Kbytes
LCD dots	4x32	8x40	8x40	8x40	16x36	16x48	16x48
LCD bias	1/2, 1/3	1/3, 1/4	1/3, 1/4	1/3, 1/4	1/5	1/4,1/5	1/4,1/5
IOs	12	10	4 + 20 share with seg+2i+4O	10+2(I)	8+16 (share with seg)	8+16 (share with seg)	8+16 (share with seg)
PSG/Vol.	1 ch/ 4 level	1 ch/ 4 level	2ch/ 16 level	2ch/ 16 level	2ch/ 16 level	2 ch/ 16 level	2 ch/ 16 level
Audio	X	PWM	PWM	PWM	PWM	PWM	PWM

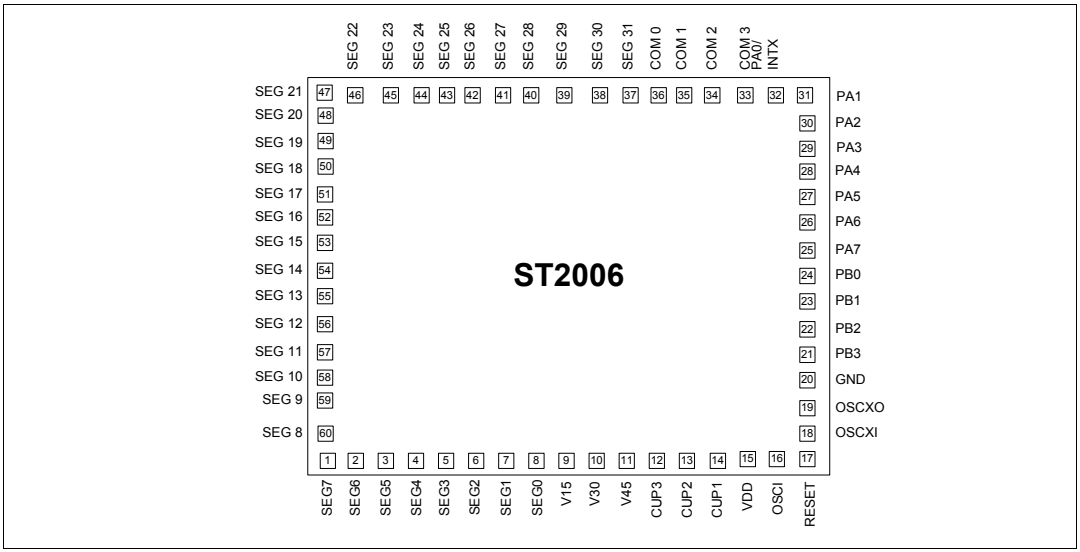
1. Features

- 8-bit static pipeline CPU
- ROM: 6K x 8 bits
- RAM: 96 x 8 bits (data + stack)
- Operation voltage : 2.4V~3.6V
- 12 CMOS Bi-directional bit programmable I/O pins
- 8 Output pins (Shared with LCD segment)
- Hardware de-bounce option for Port-A interrupt
- Bit programmable PULL-UP for input port
- Timer/Counter :
  - One 8-bit timer / 16-bit event counter
  - One 8-bit BASE timer
- Four powerful interrupt sources :
  - External interrupt (edge trigger)
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
- 16-level deep stack
- Dual clock source :
  - OSCX: Crystal oscillator: 32.768K Hz
  - OSC: RC oscillator 500K ~ 2M Hz
- Build-in oscillator with warm-up timer
- LCD driver programmable duty :
  - 128 (4x32) dots (1/4 duty, 1/3 bias)
  - 96 (3x32) dots (1/3 duty, 1/2 bias)
- Programmable Sound Generator (PSG) includes :
  - Tone generator
  - Noise generator
  - 4 level volume control
- Three power down modes :
  - WAI0 mode
  - WAI1 mode
  - STP mode
- Stand by current < 5uA

2. Application

- Timepieces -- Watch / Calendar Clock / Digital wall Clock
- Calculator / Currency converter
- Radio control clock
- Handhold LCD segment game
- Sport meter - Step , distance , speed , calorie , pulse … counter
- IR Remote control

3. Pad Diagram



4. Pad Description

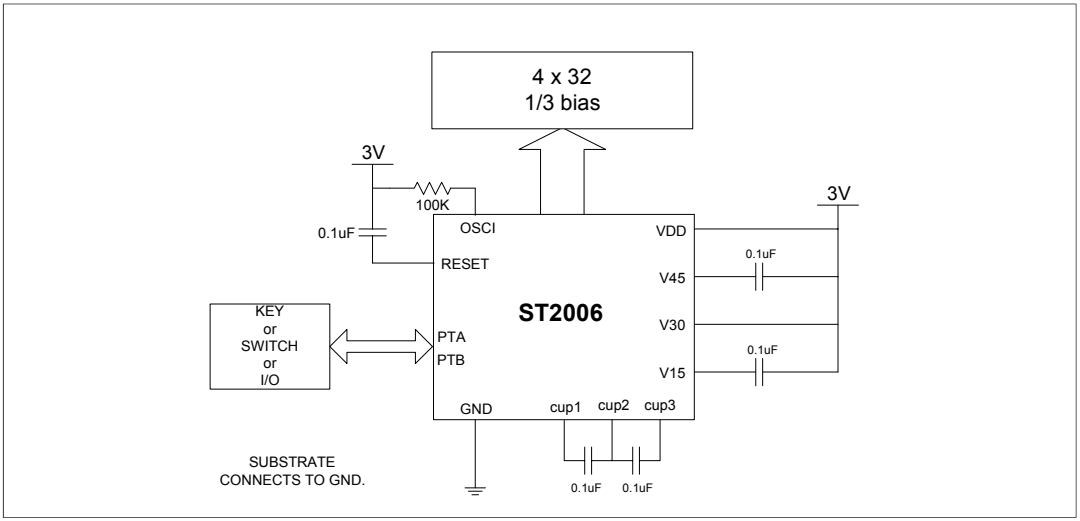
Designation	Pad #	Type	Description
SEG 0 - 7	1~8	O	LCD Segment output or output port
SEG 8 - 31	37~60	O	LCD Segment output
COM 0 - 3	33~36	O	LCD Common output
RESET	17	I	Pad reset input (high active)
GND	20	P	Ground Input and chip substrate
PA0/INTX	32	I/O I I I	Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source
PA 1-7	25~31	I/O I	Port-A bit programmable I/O Transition-trigger Interrupt
PB 0-1	23, 24	I/O	Port-B bit programmable I/O
PB 2-3	21, 22	I/O O	Port-B bit programmable I/O PSG Output
VDD	15	P	Power supply
OSCXI	18	I	OSCX input pin, for 32768Hz crystal
OSCXO	19	O	OSCX output pin, for 32768Hz crystal
OSCI	16	I	OSC input pin, toward external resistor
CUP1~3	12~14	I	Voltage pump up capacitor
V15,V30,V45	9~11	I	LCD voltage capacitor

Legend: I = input, O = output, I/O = input/output, P = power.

5. Application Circuits

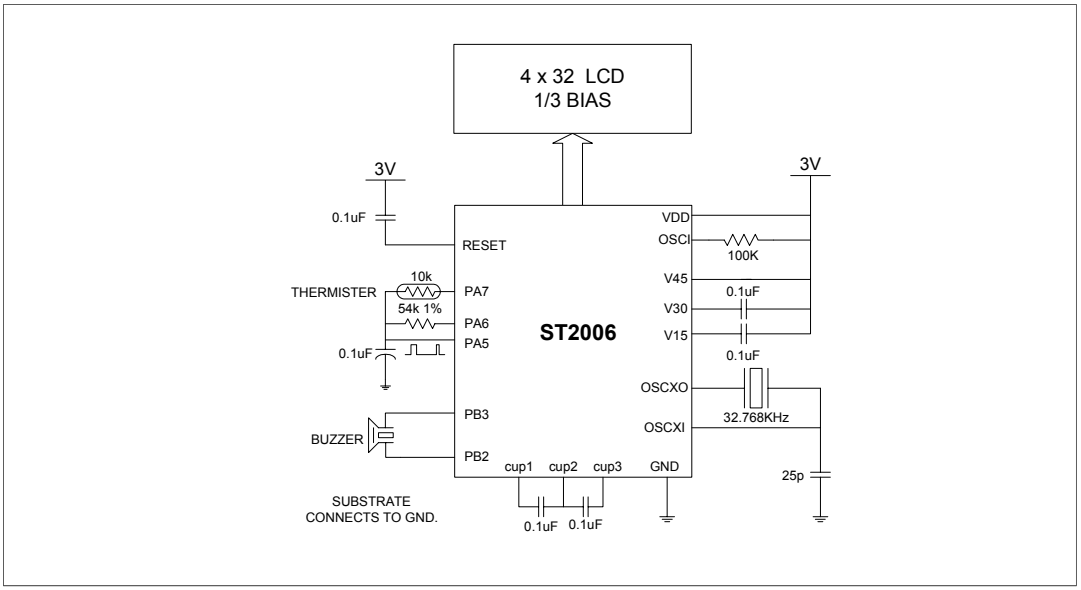
5.1 4.5v LCD Application :

- VDD: 3.0V
- CLOCK: 2.0MHz RC oscillator
- LCD: 4.5V , 1/4 duty , 1/3 bias.



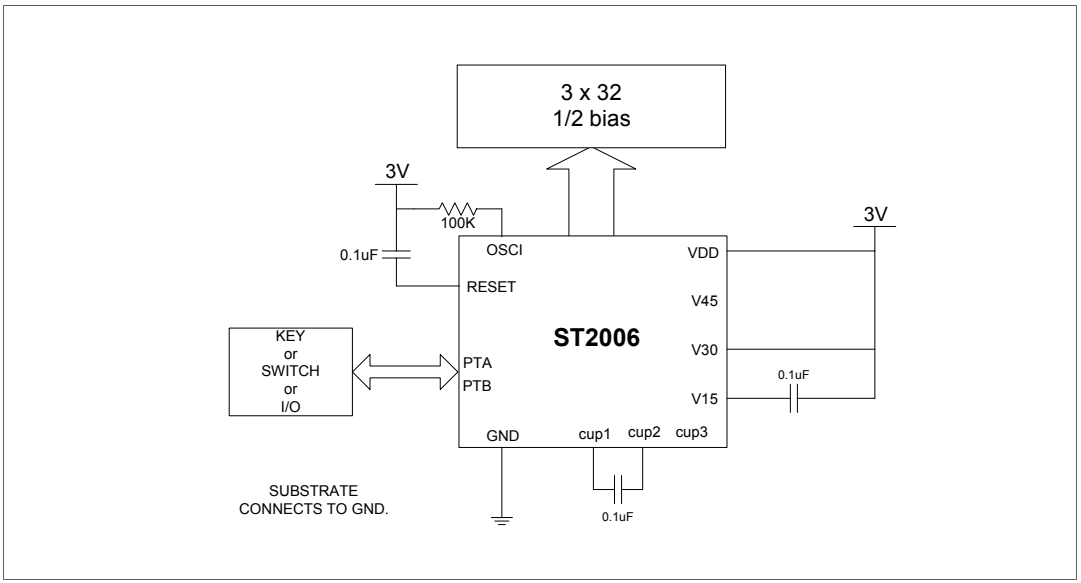
5.2 3v LCD Application 2:

- VDD : 3V
- CLOCK : 32.768KHz crystal and 2.0MHz RC oscillator
- LCD : 3.0V , 1/4 duty , 1/3 bias



5.3 1/2 bias 3v LCD Application :

- VDD : 3V
- CLOCK : 32.768KHz crystal and 2.0MHz RC oscillator
- LCD : 3.0V,1/3 duty, 1/2 bias



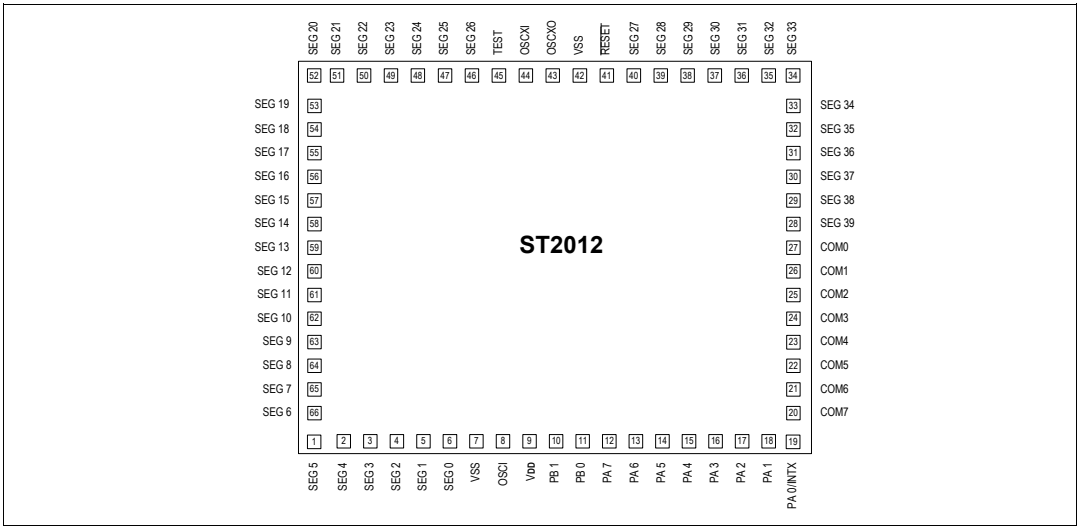
1. Features

- 8-bit static pipeline CPU
- ROM: 12K x 8 bits
- RAM: 192 x 8 bits
- Operation voltage : 2.4V ~ 5V
- 10 CMOS Bi-directional bit programmable I/O pins
- 8 Output pins (Shared with LCD common/ segment)
- Hardware debounce option for input port
- Bit programmable PULL-UP for input port
- Timer/Counter :
  - One 8-bit timer / 16-bit event counter
  - One 8-bit BASE timer
- Five powerful interrupt sources :
  - External interrupt (edge trigger)
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
  - DAC reload interrupt
- 32-level deep stack
- Dual clock source :
  - OSCX: Crystal oscillator: 32.768K Hz
  - OSC: RC oscillator 500K ~ 4M Hz
- Build-in oscillator with warm-up timer
- LCD driver programmable duty :
  - 320 (8x40) dots (1/8 duty, 1/4 bias)
  - 160 (4x40) dots (1/4 duty, 1/3 bias)
- Programmable Sound Generator (PSG) includes :
  - Tone generator
  - Sound effect generator
  - 4 level volume control
  - Digital DAC for speech / tone
- Three power down modes :
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Application

- Timepieces -- Watch / Calendar Clock
- Calculator / Currency converter
- LCD Education Toys
- LCD Segment game
- Sport meter - Step , distance , speed , calorie , pulse … counter
- Radio control clock

3. Pad Diagram



4. Pad Description

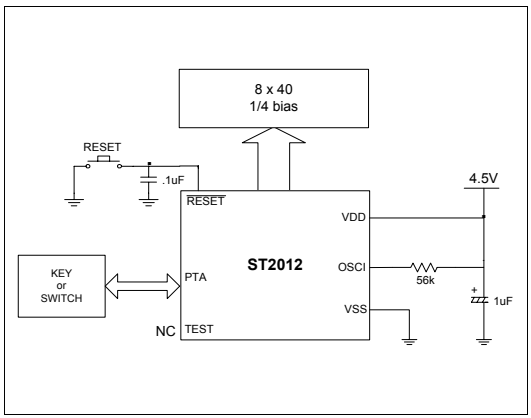
Designation	Pad #	Type	Description
SEG 0 - 3	3~6	O O	LCD Segment output Output port
SEG 4 - 39	1,2, 28~40, 46~66	O	LCD Segment output
COM 0 - 3	24~27	O	LCD Common output
COM 4 - 7	20~23	O O	LCD Common output Output port
$\overline{\text{RESET}}$	41	I	Pad reset input (LOW Active)
VSS	7, 42	P	Ground Input and chip substrate
PA0/INTX	19	I/O I I I	Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source
PA 1-7	12~18	I/O I	Port-A bit programmable I/O Transition-trigger Interrupt
PB 0-1	10, 11	I/O O	Port-B bit programmable I/O PSG/DAC Output
V_{DD}	9	P	Power supply
OSCXI	44	I	OSC input pin. For 32768Hz crystal
OSCXO	43	O	OSC output pin. For 32768Hz crystal
OSCI	8	I	OSC input pin. toward to external resistor
TEST	45	I	Test pin

Legend: I = input, O = output, I/O = input/output, P = power.

5. Application Circuits

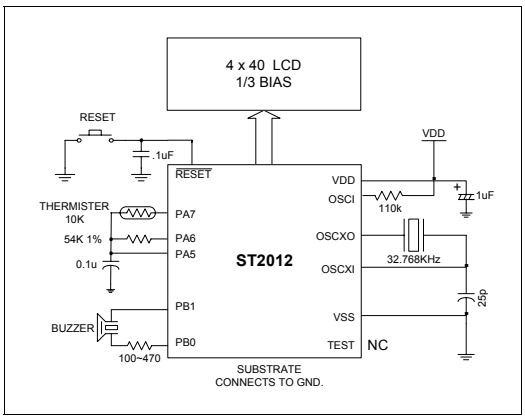
Application 1:

- V_{DD} : 4.5V
- CLOCK : RC 4.0M
- LCD : 1/8 duty, 1/4 bias;
- I/O : PORT A



Application 2:

- Clock : 32.768KHz crystal and 2.0M RC oscillator
- LCD : 1/4 duty, 1/3 bias
- I/O : PORT A
- ALARM : PB.0, PB.1



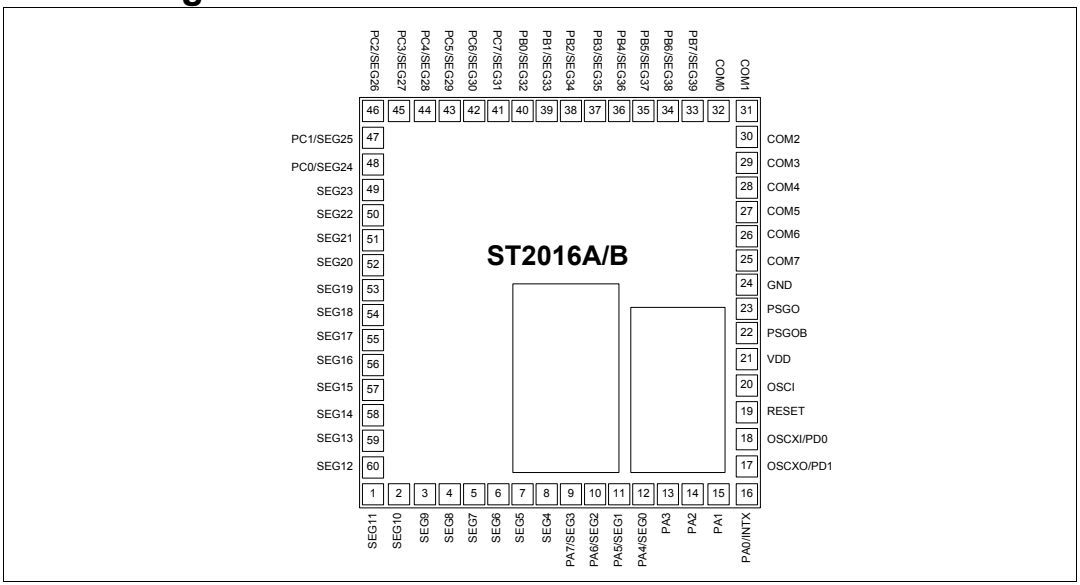
1. Features

- 8-bit static pipeline CPU
- ROM: 16K x 8 bits
- RAM: 192 x 8 bits
- Operation voltage : 2.4V ~ 3.6V
- Power consumption:
- 24 CMOS Bi-directional bit programmable I/O pins
  - Twenty (Port-A high nibble & Port-B/C) are shared with LCD drives
- 6 Output pins (Four are shared with LCD common and two are shared with PSG)
- 2 Input pins (code option: Shared with OSCX)
- Hardware debounce option for input port
- Bit programmable PULL-UP for input port
- Timer/Counter :
  - One 8-bit timer / 16-bit event counter
  - One 8-bit BASE timer
- Five powerful interrupt sources :
  - External interrupt (edge trigger)
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
  - DAC reload interrupt
- 32-level deep stack
- Dual clock source :
  - OSCX: Crystal oscillator: 32768Hz
  - OSC: RC oscillator 500K ~ 4M Hz
- Build-in oscillator with warm-up timer
- LCD controller driver:
  - 16 level contrast control
  - 320 (8x40) dots (1/8 duty, 1/4 bias, programmable)
  - 160 (4x40) dots (1/4 duty, 1/3 bias, programmable)
  - Two clock source options: RC and resonator oscillator
  - Keyboard scan function supported on 20 shared segment drives
  - Internal bias resistors(1/4 bias & 1/3 bias) with 32 level driving strength control
- Programmable Sound Generator (PSG) includes :
  - Tone generator
  - Sound effect generator
  - 16 level volume control
  - Digital DAC for speech / tone
- Three power down modes :
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Application

- Watch
- Calendar clock
- Calculator
- Handhold LCD game
- Remote control
- Sport meter

3. Pad Diagram



4. Pad Description

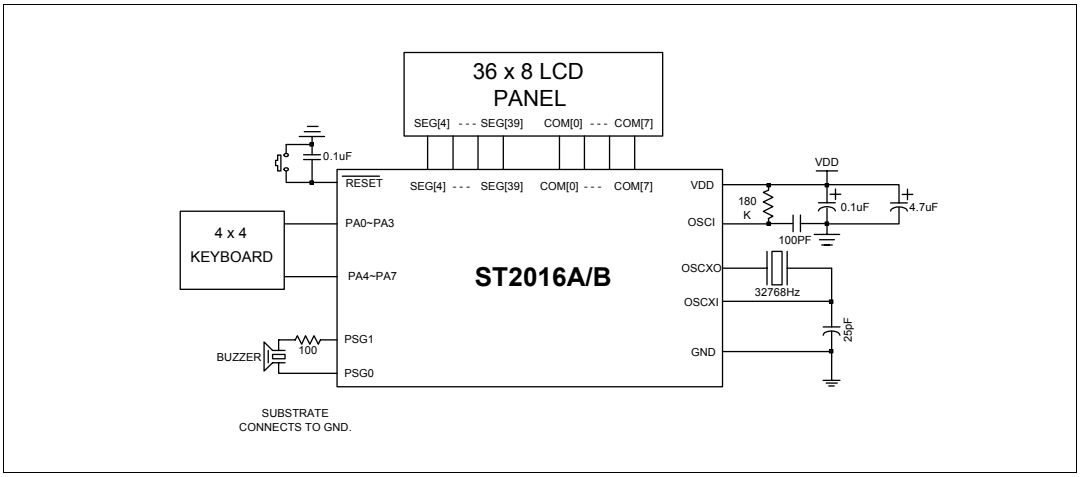
Designation	Pad #	Type	Description
SEG0/PA4 ~ SEG3/PA7	12 ~ 9	O I/O	LCD Segment output Port-A bit programmable I/O
SEG4 ~ SEG23	8 ~ 1 60 ~ 49	O	LCD Segment output
SEG24/PC0 ~ SEG31/PC7	48 ~ 41	O I/O	LCD Segment output Port-C bit programmable I/O
SEG32/PB0 ~ SEG39/PB7	40 ~ 33	O I/O	LCD Segment output Port-B bit programmable I/O
COM 0 – 3	32 ~ 29	O	LCD Common output
COM 4 - 7	28 ~ 25	O O	LCD Common output Output port
$\overline{\text{RESET}}$	19	I	Pad reset input (HIGH Active)
VSS	24	P	Ground Input and chip substrate
PA0/INTX	16	I/O I I I	Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source
PA 1-7	15 ~ 13	I/O I	Port-A bit programmable I/O Transition-trigger Interrupt
PSGO,PSGOB	23,22	O	PSG/DAC Output
V_{DD}	21	P	Power supply
OSCXI/PD0	18	I I	OSC input pin. For 32768Hz crystal Port-D input
OSCXO/PD1	17	O I	OSC output pin. For 32768Hz crystal Port-D input
OSCI	20	I	OSC input pin. toward to external resistor

Legend: I = input, O = output, I/O = input/output, P = power.

5. Application Circuit

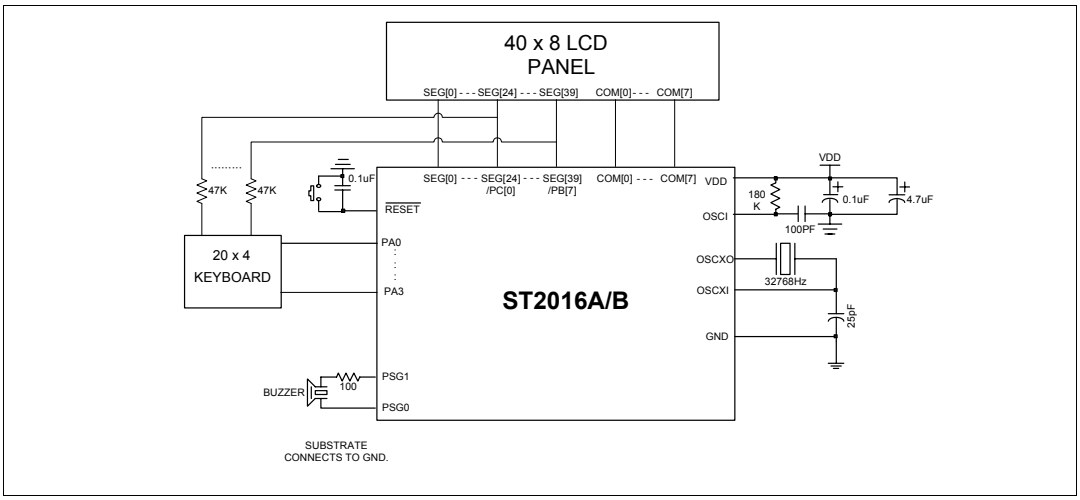
a. Application circuit without LCD keyboard awaking pulse

- V_{DD} : 3V
- Clock : 32768Hz crystal and 4.0MHz RC oscillator
- LCD : 1/8 duty
- I/O : PORT A
- ALARM : PSG0, PSG1



b. Application circuit with LCD keyboard awaking pulse

- V_{DD} : 3V
- Clock : 32768Hz crystal and 4.0MHz RC oscillator
- LCD : 1/8 duty
- I/O : PORT A
- ALARM : PSG0, PSG1



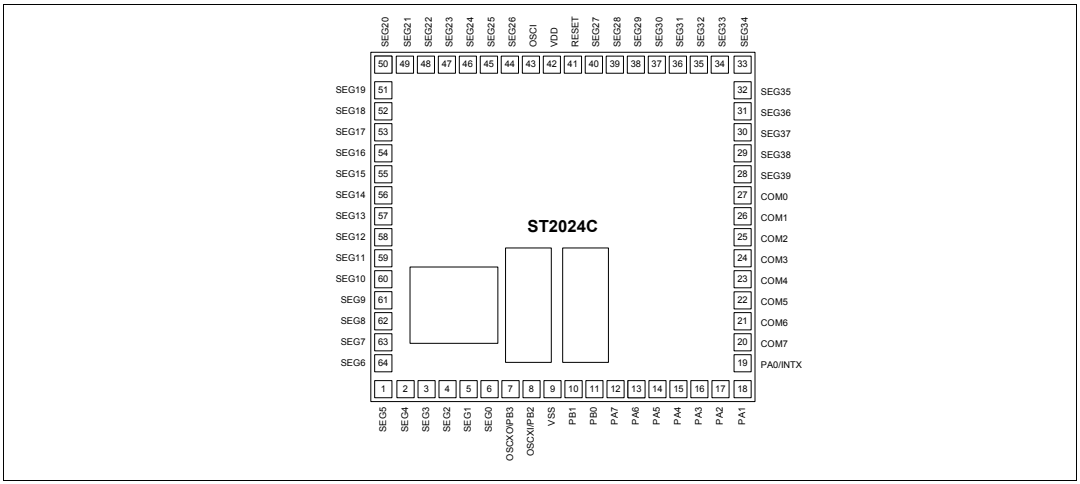
1. Features

- 8-bit static pipeline CPU
- ROM: 24K x 8 bits
- RAM: 384 x 8 bits(256/128)
- Operation voltage : 2.4V ~ 3.6V
- 10 CMOS Bi-directional bit programmable I/O pins
- 8 Output pins (Shared with LCD common/ segment)
- Hardware debounce option for input port
- Bit programmable PULL-UP for input port
- Timer/Counter :
  - One 8-bit timer / 16-bit event counter
  - One 8-bit BASE timer
- Five powerful interrupt sources :
  - External interrupt (edge trigger)
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
  - DAC reload interrupt
- 128-level deep stack
- Dual clock source :
  - OSCX: Crystal oscillator: 32.768K Hz
  - OSC: RC oscillator 500K ~ 4M Hz (dedicated for game)
- Build-in oscillator with warm-up timer
- LCD driver programmable 30*8 or 34*4duty :
  - 320 (8x40) dots (1/8 duty, 1/4 bias)
  - 160 (4x40) dots (1/4 duty, 1/3 bias)
  - Internal bias resistor(1/4 bias, 1/3 bias) with 32 - - - level driving strength control.
- Programmable Sound Generator (PSG) includes :
  - Tone generator
  - Sound effect generator
  - 4 level volume control
  - Digital DAC for speech / tone
- Three power down modes :
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Application

- LCD Game
- Calendar Clock
- Education Toys
- Databank
- Talking Calculator / SCT calculator
- IR Remote controller

3. Pad Diagram



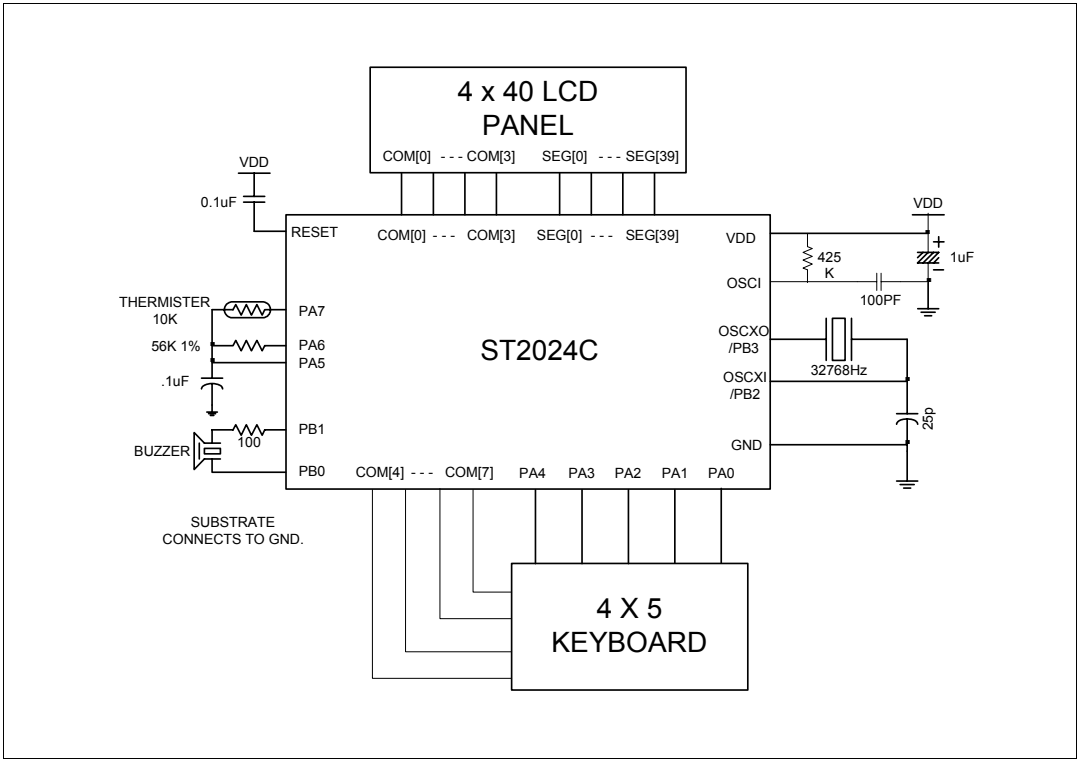
4. Pad Description

Designation	Pad #	Type	Description
SEG 0 - 3	3~6	O O	LCD Segment output Output port
SEG 4 - 31	1,2, 36~40, 46~66	O	LCD Segment output
SEG 32 - 39	28~35	O	LCD Segment output
COM 0 - 3	24~27	O	LCD Common output
COM 4 - 7	20~23	O O	LCD Common output Output port
$\overline{\text{RESET}}$	41	I	Pad reset input (HIGH Active)
VSS	9	P	Ground Input and chip substrate
PA0/INTX	19	I/O I I I	Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source
PA 1-7	12~18	I/O I	Port-A bit programmable I/O Transition-trigger Interrupt
PB 0-1	10, 11	I/O O	Port-B bit programmable I/O PSG/DAC Output
V_{DD}	42	P	Power supply
OSCXI/PB2	8	I I	OSC input pin. For 32768Hz crystal Port-B input
OSCXO/PB3	7	O I	OSC output pin. For 32768Hz crystal Port-B input
OSCI	43	I	OSC input pin. toward to external resistor

Legend: I = input, O = output, I/O = input/output, P = power.
The chip substrate should be connected with the VSS pin.

5. Application Circuit:

- VDD : 3V
- Clock : 32.768KHz crystal and 2.0MHz RC oscillator
- LCD : 1/8 duty, 1/4 bias
- I/O : PORT A
- ALARM : PB.0, PB.1
- PIN OPTION : PB.2, PB.3



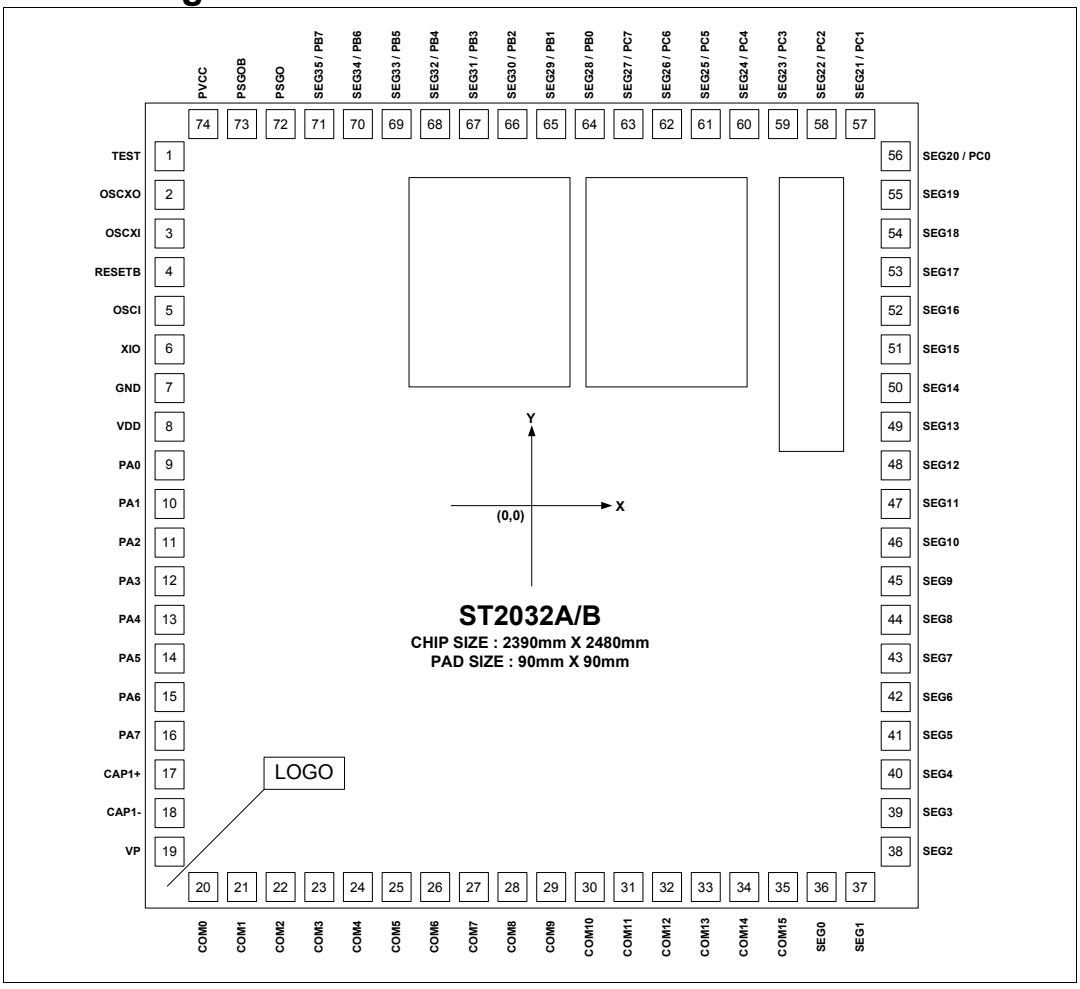
1. Features

- 8-bit static pipeline CPU
- ROM: 32K x 8-bit
- RAM: 1K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage: 2.4V~3.4V
- Built-in double DC-DC voltage converter for LCD driver
- I/O ports
  - 24 CMOS bidirectional bit programmable I/O pins, - - sixteen (Port-B/C) are shared with LCD drives
  - Bit programmable pull-up for input pins
  - Hardware de-bounce option for Port-A
- Low voltage detector
- Timer/Counter:
  - Two 8-bit timer/16-bit event counter
  - One 8-bit Base timer
- 6 hardware interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - Timer0 interrupt
  - Timer1 interrupt
  - Base timer interrupt
  - Port-A[7~0] interrupt (transition triggered)
  - DAC reload interrupt
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator ..... 32768 Hz
  - RC oscillator .....500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (code option).....455K~4M Hz
- LCD controller/driver
  - Resolution: 20x16 ~ 36x16, maximum 576 dots
  - Two clock source options: RC and resonator oscillator
  - Internal bias resistors (1/5 bias) with 16-level driving strength control
  - Up to 12-level contrast control
  - Keyboard-scan function supported on 16 shared segment drives
- Programmable sound generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
  - Dedicated outputs for directly connection to buzzer
- PWM DAC: Three modes up to 8-bit resolution
- Three power down modes:
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Application

- Databank
- LCD Game
- Calendar Clock
- SCT calculator / Talking calculator
- Education Toys
- IR Remote controller

3. Pad Diagram



4. Pad Description

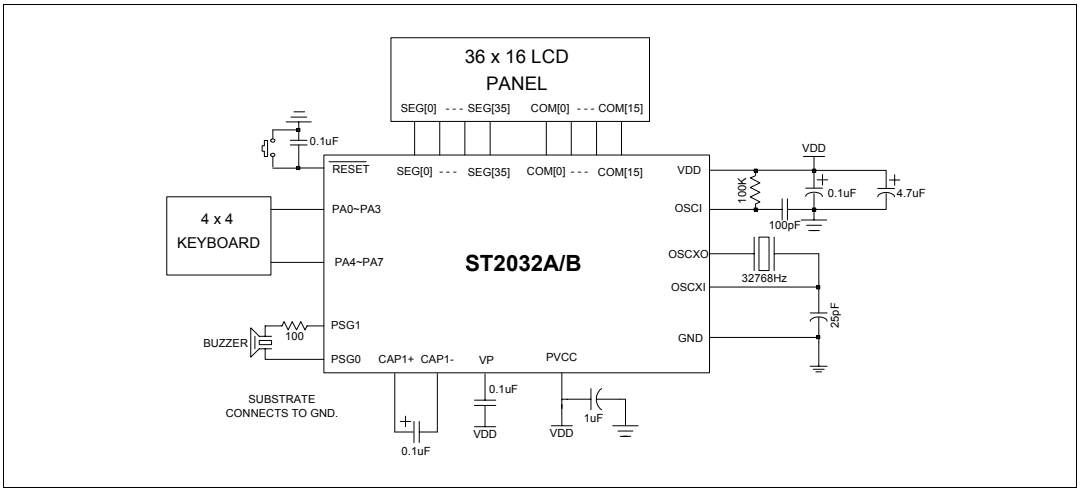
Pin No.	Designation	I/O	Description
20~35	COM0~15	O	LCD common drive output pins, drives 0~15
36~55	SEG0~19	O	LCD segment drive output pins, drives 0~19
9	PA0 / INTX	I/O I I I	- Port-A bit programmable I/O - Edge-trigger Interrupt. - Transition-trigger Interrupt - Programmable Timer1 clock source
10~16	PA1~7	I/O I	- Port-A bit programmable I/O - Transition-trigger Interrupt
64~71	SEG28/PB0~ SEG35/PB7	I/O O	- Port-B bit programmable I/O - LCD segment drives 28~35
56~63	SEG20/PC0~ SEG27/PC7	I/O O	- Port-C bit programmable I/O - LCD segment drives 20~27
72,73	PSGO,PSGOB	O	PSG/ PWM DAC Outputs
2,3	OSCXO, OSCXI	I/O	Low frequency crystal oscillator I/O pins. Connect to external 32768 Hz crystal.
4	$\overline{\text{RESET}}$	I	Reset signal input (low active)
5	OSCI	I I	- RC oscillator input pin. Connected to external resistor - High frequency crystal/resonator oscillator input pin. Connect to external crystal/resonator.
6	XIO	O	- NC - High frequency crystal/resonator oscillator output pin. Connect to external crystal/resonator.
7	GND	P	Ground pin
8	V_{DD}, AVDD	P	Power supply pin, Analogy Power supply pin
17	CAP1+	I/O	Connect to booster capacitor positive(+) terminal
18	CAP1-	I/O	Connect to booster capacitor negative(-) terminal
19	VP	O	Voltage output of booster circuit
1	TEST	I	Chip test function. Leave it open.
74	PVCC	I	PSG power input

Note: I = input, O = output, I/O = input/output, P = power.

5. Application Circuit

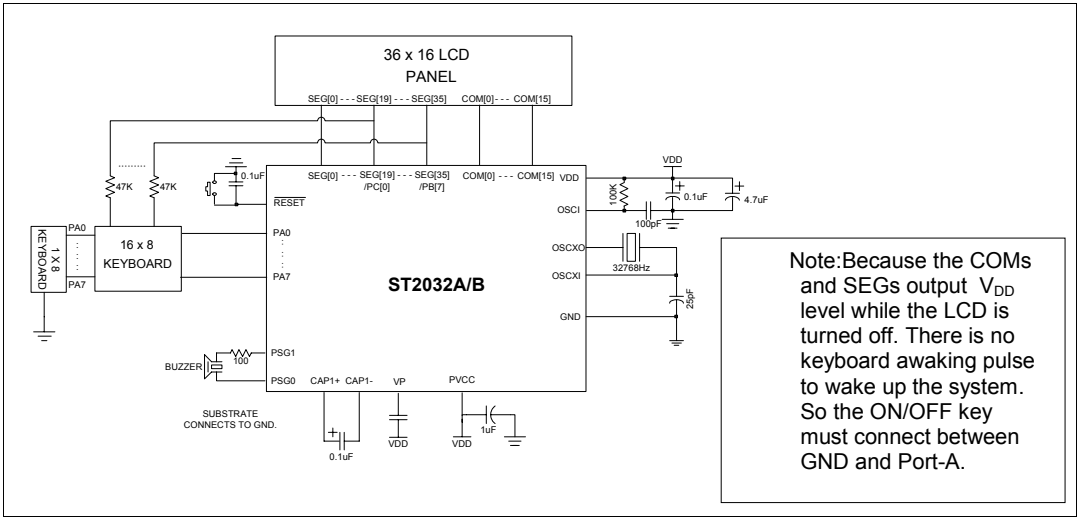
a. Application Circuit without LCD keyboard awaking pulse

- V_{DD} : 3V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT-A
- ALARM : PSG0, PSG1



b. Application Circuit with LCD keyboard awaking pulse

- V_{DD} : 3V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT-A/B/C
- ALARM : PSG0, PSG1



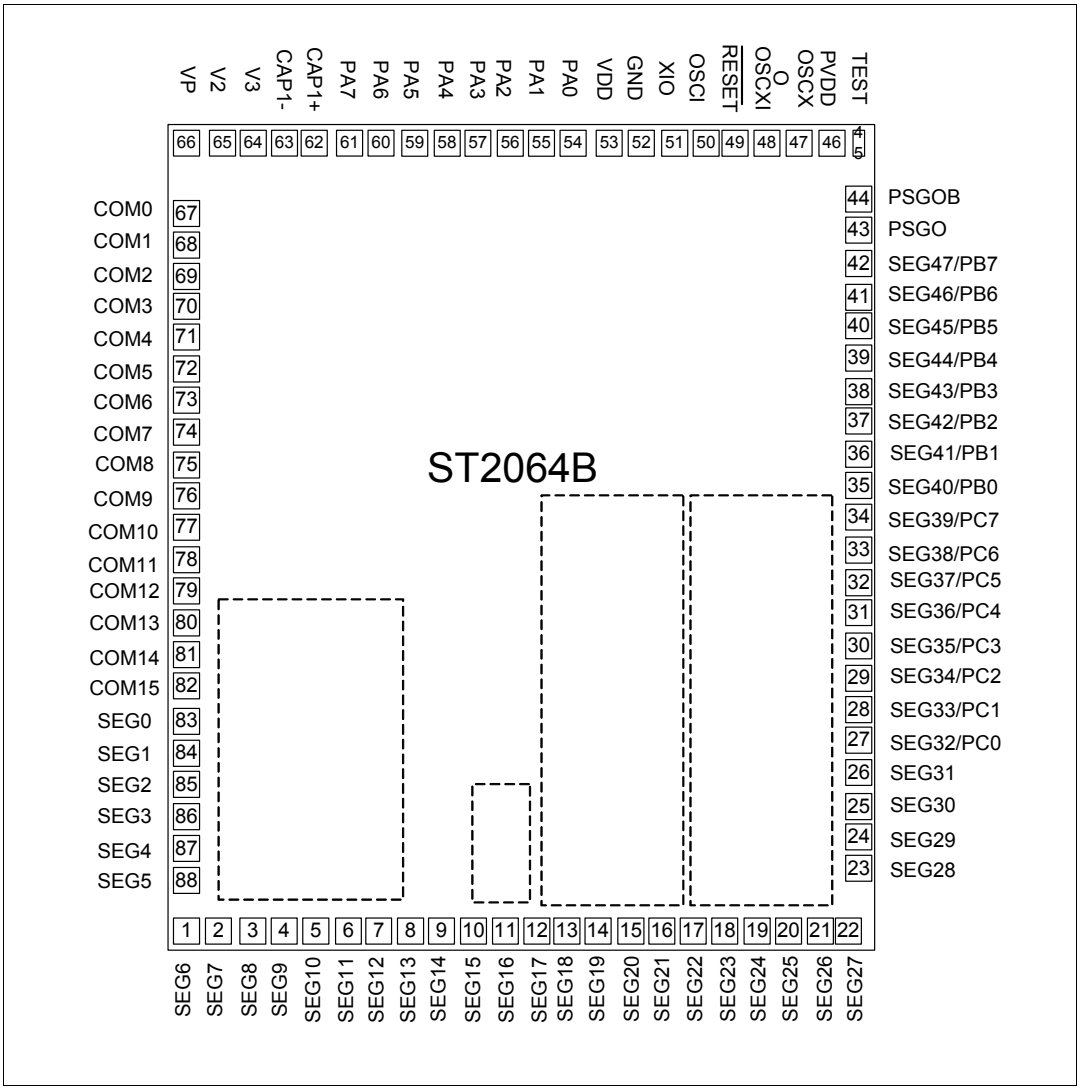
1. Features

- 8-bit static pipeline CPU
- ROM: 64K x 8-bit
- RAM: 2K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage:
  - DC-DC Converter Enable:2.4V ~ 3.6V
  - DC-DC Converter Disable:2.4V ~ 5.5V
- Built-in double DC-DC voltage converter for LCD driver
- I/O ports
  - 24 CMOS bidirectional bit programmable I/O pins, sixteen (Port-B/C) are shared with LCD drives
  - 8 open drain output pins are shared with LCD drives
- - 2 COMS output pins are shared with PSG drives
  - Bit programmable pull-up for input pins
  - Hardware de-bounce option for Port-A
- Low voltage detector
  Timer/Counter:
  - Two 8-bit timer/16-bit event counter
  - One 8-bit Base timer
- 6 hardware interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - Timer0 interrupt
  - Timer1 interrupt
  - Base timer interrupt
  - Port-A[7~0] interrupt (transition triggered)
  - DAC reload interrupt
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator ..... 32768 Hz
  - RC oscillator .....500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (code option).....455K~4M Hz
- LCD controller/driver
  - Resolution: 32x8 ~ 48x16, maximum 768 dots
  - Two clock source options: RC and resonator oscillator
  - Internal bias resistors (1/5 bias/1/4 bias) with 16-level driving strength control
  - Up to 16-level contrast control
  - Keyboard scan function supported on 16 shared segment drives
- Programmable sound generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
  - Dedicated outputs for directly connection to buzzer
- PWM DAC: Three modes up to 8-bit resolution
- Three power down modes:
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Application

- Databank
- LCD game
- Education Toys
- Calendar Clock
- IR Remote control
- SCT Calculator

3. Pad Diagram



4. Pad Description

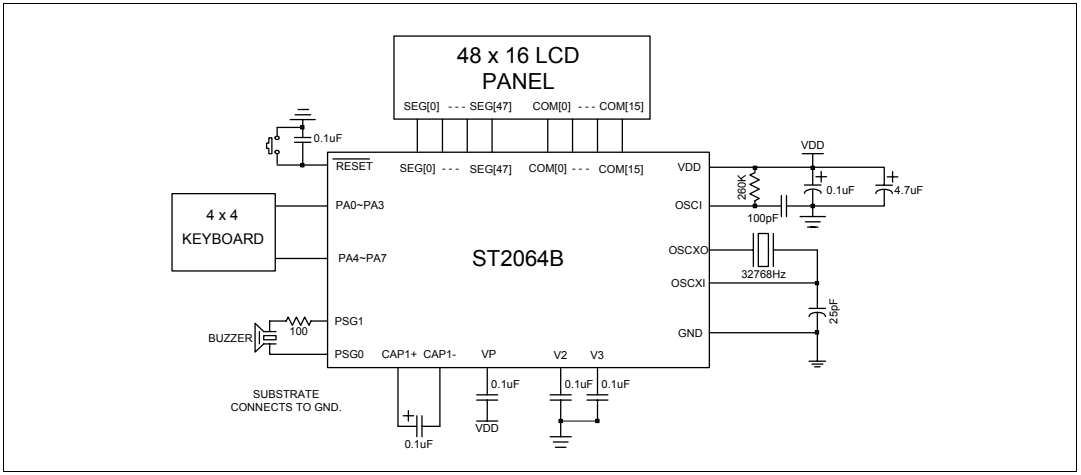
Pin No.	Designation	I/O	Description
67~74	COM0~7	O	LCD common drive output pins, drives 0~7
75~82	COM8/~15	O O	LCD common drive output pins, drives 8~15 Common open drain output port.
83~26	SEG0~31	O	LCD segment drive output pins, drives 0~31
54	PA0 / INTX	I/O I I I	- Port-A bit programmable I/O - Edge-trigger Interrupt. - Transition-trigger Interrupt - Programmable Timer1 clock source
55~61	PA1~7	I/O I	- Port-A bit programmable I/O - Transition-trigger Interrupt
35~42	SEG40/PB0~ SEG47/PB7	I/O O	- Port-B bit programmable I/O - LCD segment drives 40~47
27~34	SEG32/PC0~ SEG39/PC7	I/O O	- Port-C bit programmable I/O - LCD segment drives 32~39
44,43	PSGOB,PSGO	O	PSG/ PWM DAC Outputs
47,48	OSCXO, OSCXI	I/O	Low frequency crystal oscillator I/O pins. Connect to external 32768 Hz crystal.
49	$\overline{\text{RESET}}$	I	Reset signal input (low active)
50	OSCI	I I	- RC oscillator input pin. Connected to external resistor - High frequency crystal/resonator oscillator input pin. Connect to external crystal/resonator.
51	XIO	O	- NC - High frequency crystal/resonator oscillator output pin. Connect to external crystal/resonator.
52	GND	P	Ground pin
53	V_{DD}	P	Power supply pin
62	CAP1+	I/O	Connect to booster capacitor positive(+) terminal
63	CAP1-	I/O	Connect to booster capacitor negative(-) terminal
65,64	V2~V3	P	Multi-level power supply for the liquid crystal drive
66	VP	O	Voltage output of booster circuit
45	TEST	I	Chip test function. Leave it open.
46	PVDD	P	PSG Power

Note: I = input, O = output, I/O = input/output, P = power.

5. Application Circuit

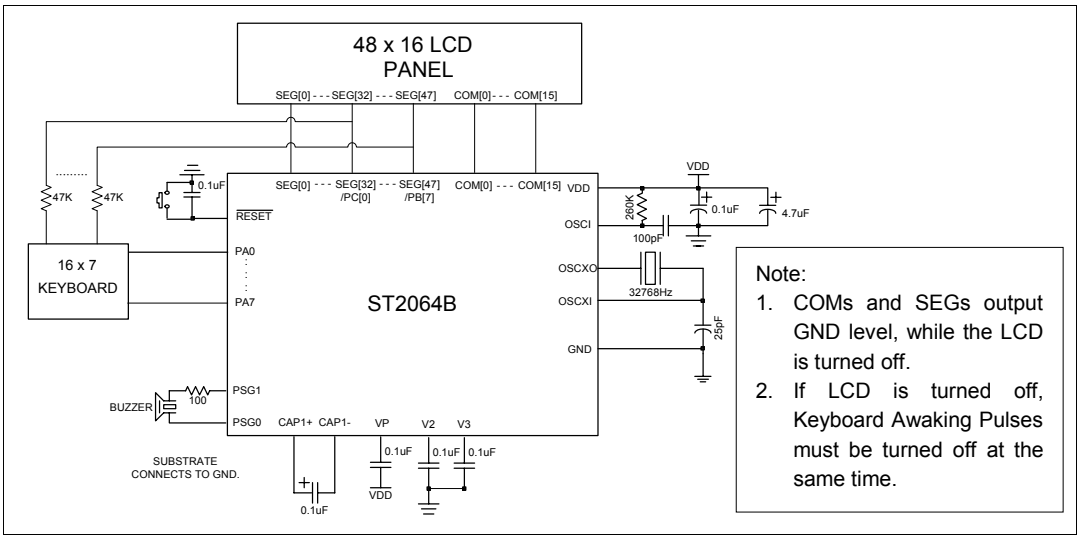
5.1 Application circuit without LCD keyboard awaking pulse

- V_{DD} : 3V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT A
- ALARM : PSG0, PSG1



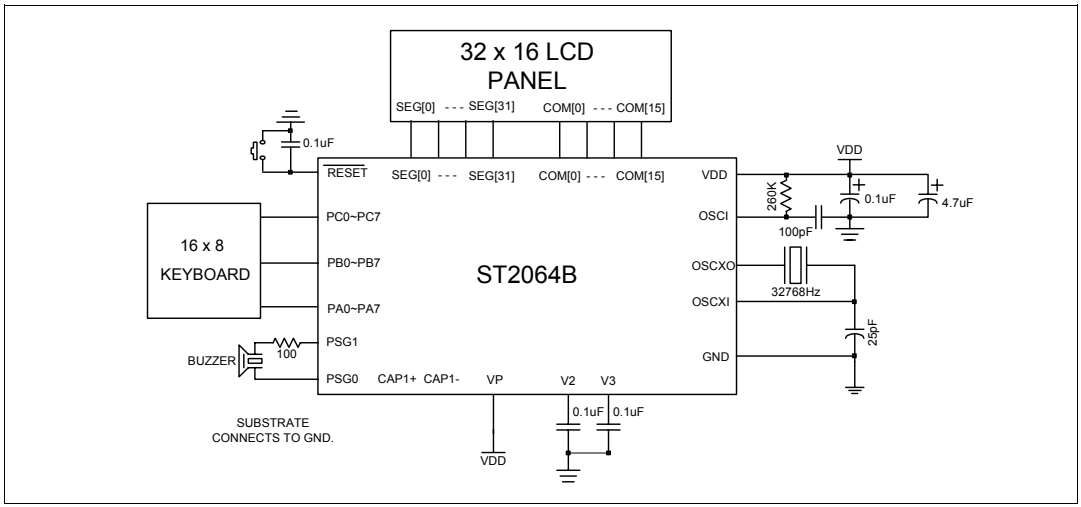
5.2 Application circuit with LCD keyboard awaking pulse

- V_{DD} : 3V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT A
- ALARM : PSG0, PSG1



5.3 Application circuit without DC-DC converter

- V_{DD} : 5V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT A/B/C
- ALARM : PSG0, PSG1



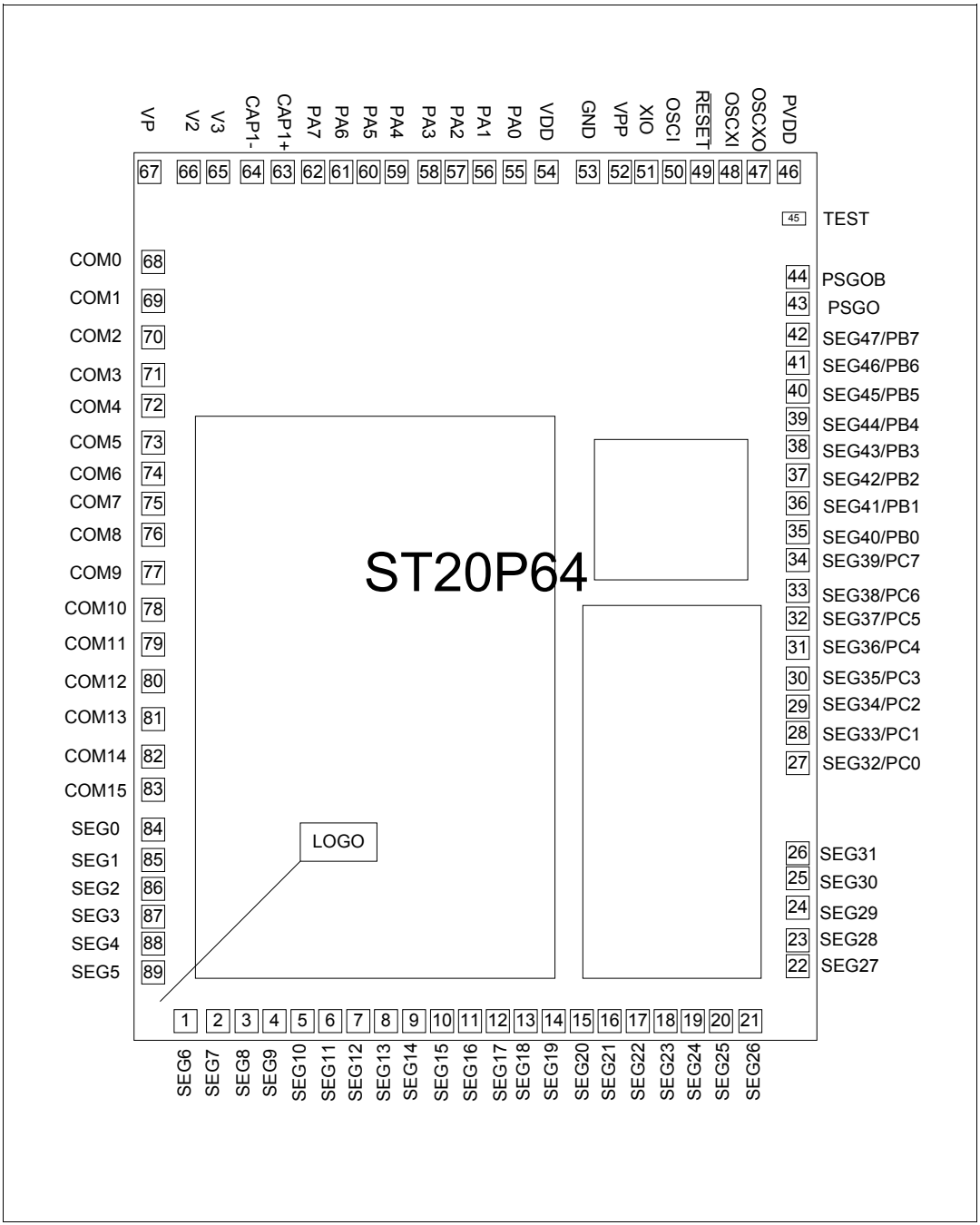
1. Features

- 8-bit static pipeline CPU
- ROM: 64K x 8-bit PROM
- RAM: 2432 x 8-bit
- Stack: Up to 128-level deep
- Operation voltage: 2.6V ~ 5.5V
- Built-in double DC-DC voltage converter for LCD driver
- I/O ports
  - 24 CMOS bidirectional bit programmable I/O pins, sixteen (Port-B/C) are shared with LCD drives
  - 8 open drain output pins are shared with LCD drives
  - 2 CMOS output pins are shared with PSG drives
  - Bit programmable pull-up for input pins
  - Hardware de-bounce option for Port-A
- Low voltage detector
- Timer/Counter:
  - Two 8-bit timer/16-bit event counter
  - One 8-bit Base timer
- 6 hardware interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - Timer0 interrupt
  - Timer1 interrupt
  - Base timer interrupt
  - Port-A[7~0] interrupt (transition triggered)
  - DAC reload interrupt
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator…..32768 Hz
  - RC oscillator ……..500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (code option)…….455K~4M Hz
- LCD controller/driver
  - Resolution: 32x8 ~ 48x16, maximum 768 dots
  - Two clock source options: RC and resonator oscillator
  - Internal bias resistors (1/5 bias/1/4 bias) with 16-level driving strength control
  - Up to 16-level contrast control
  - Keyboard scan function supported on 16 shared segment drives
- Programmable sound generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
  - Dedicated outputs for directly connection to buzzer
- PWM DAC: Three modes up to 8-bit resolution
- Three power down modes:
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. General Description

The ST20P64 is a W65C02S based 8-bit microcontroller designed with CMOS silicon gate technology. This single chip microcontroller is useful for translator, databank and other consumer applications. It integrates with SRAM, mask ROM, LCD controller/driver, DC-DC voltage converter, I/O ports, timers, PSG and PWM DAC. This chip also builds in dual oscillators for the chip performance enhancement.

3. Pad Diagram



4. Pad Description

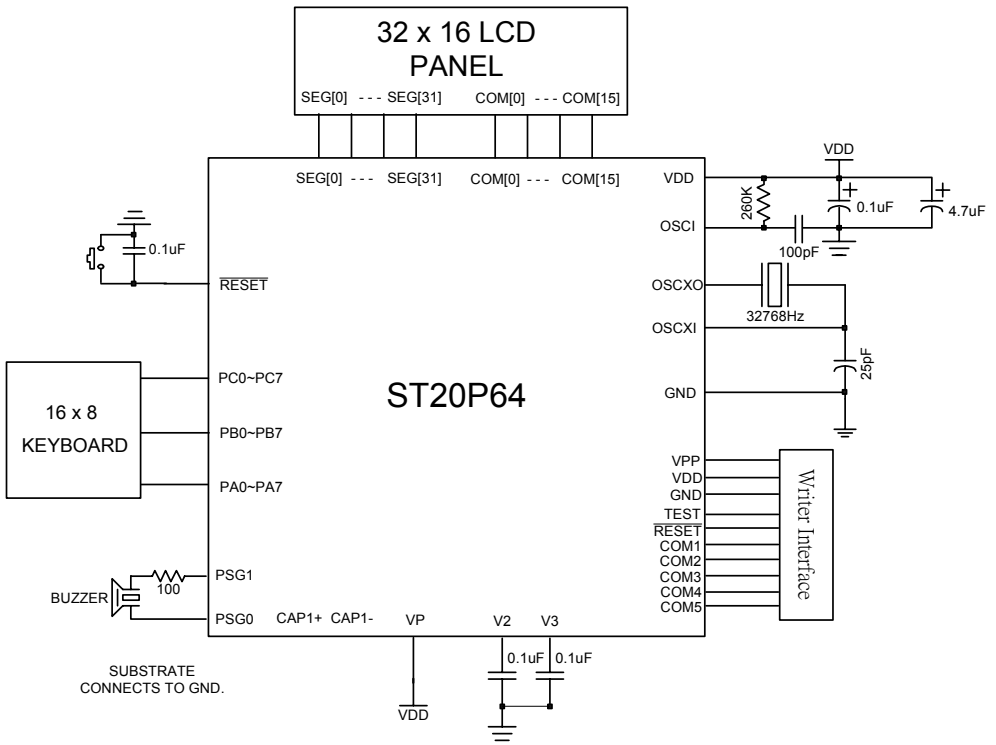
Pin No.	Designation	I/O	Description
70~73	COM/SCK COM2 COM3/SS COM4/MOSI COM5/MISO	I/O	LCD common drive output pins, drives 2~5 SPI interface for OTP programming.
68,69,74,75	COM0,1,6,7	O	LCD common drive output pins, drives 0, 1, 6, 7
76~83	COM8~5	O O	LCD common drive output pins, drives 8~15 Common poen drain output port.
8 4 ~ 8 9 , 0~26	SEG0~31	O	LCD segment drive output pins, drives 0~31
54	PA0/ INTX	I/O I I I	- Port-A bit programmable I/O - Edge-trigger Interrupt. - Transition– trigger Interrupt - Programmable Timer1 clock source
56~62	PA1~7	I/O I	- Port-A bit programmable I/O - Transition– trigger Interrupt
35~42	SEG40/PB0~ SEG47/PB7	I/O O	- Port-B bit programmable I/O - LCD sement drives 40~47
27~33	SEG32/ PC0~ SEG39/PC7	I/O O	- Port-C bit programmable I/O - LCD segment drives 32~39
44,43	PSGOB,PSGO	O	PSG/ PWM DAC Outputs
47,48	OSCXO, OSCXI	I/O	Low frequency crystal oscillator I/O pins. Connect to external 32768 Hz crystal.
49	$\overline{\text{RESET}}$	I	Reset signal input (low active)
50	OSCI	I I	- RC oscillator input pin. Connected to external resistor. - High frequency crystal/ resonator oscillator input pin. Connect to external crystal/ resonator.
51	XIO	O	- NC - High frequency crystal/ resonator oscillator output pin. Connect to external crystal/ resonator.
53	GND	P	Ground pin
54	VDD	P	Power supply pin
63	CAP1+	I/O	Connect to booster capacitor positive (+) terminal
64	CAP1-	I/O	Connect to booster capacitor positive (-) terminal
66,65	V2, V3	P	Multi-level power supply for the liquid crystal drive
67	VP	O	Voltage output of booster circuit
45	TEST	I	Chip test function. Leave it open.

Note: I = input, O = output, I/O = input/output, P = power.

5. Application Circuit

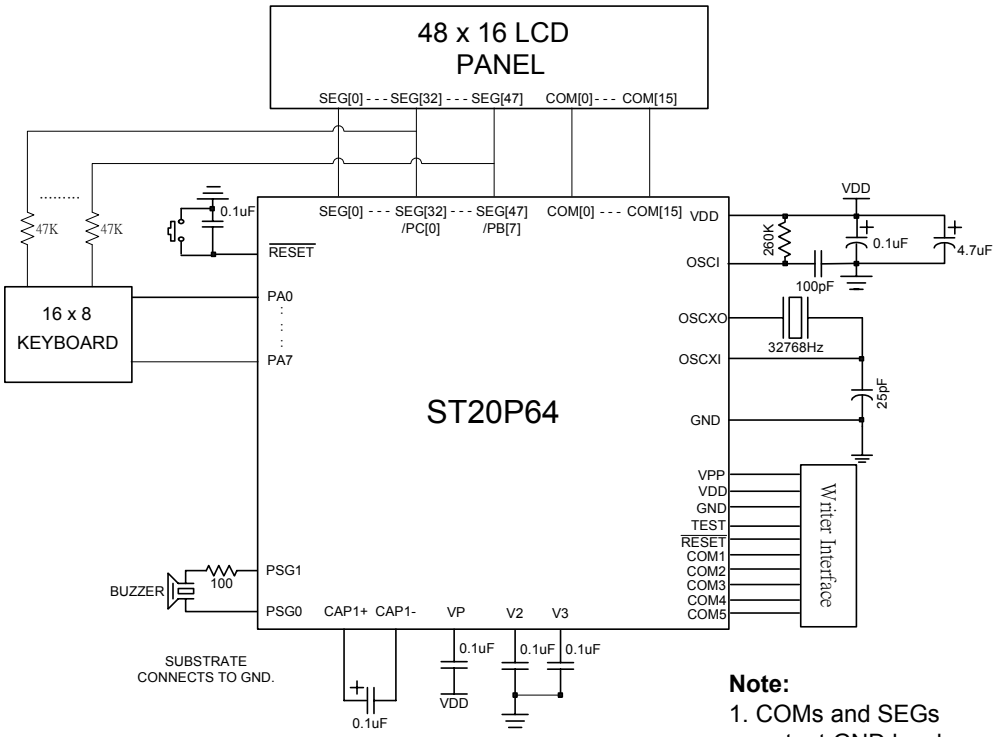
5.1 Application circuit under 3V operating voltage

- VDD : 3V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT A
- ALARM : PSG0, PSG1



APPLICATION CIRCUIT WITHOUT LCD KEYBOARD AWAKING PULSE

- VDD : 3V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT A
- ALARM : PSG0, PSG1



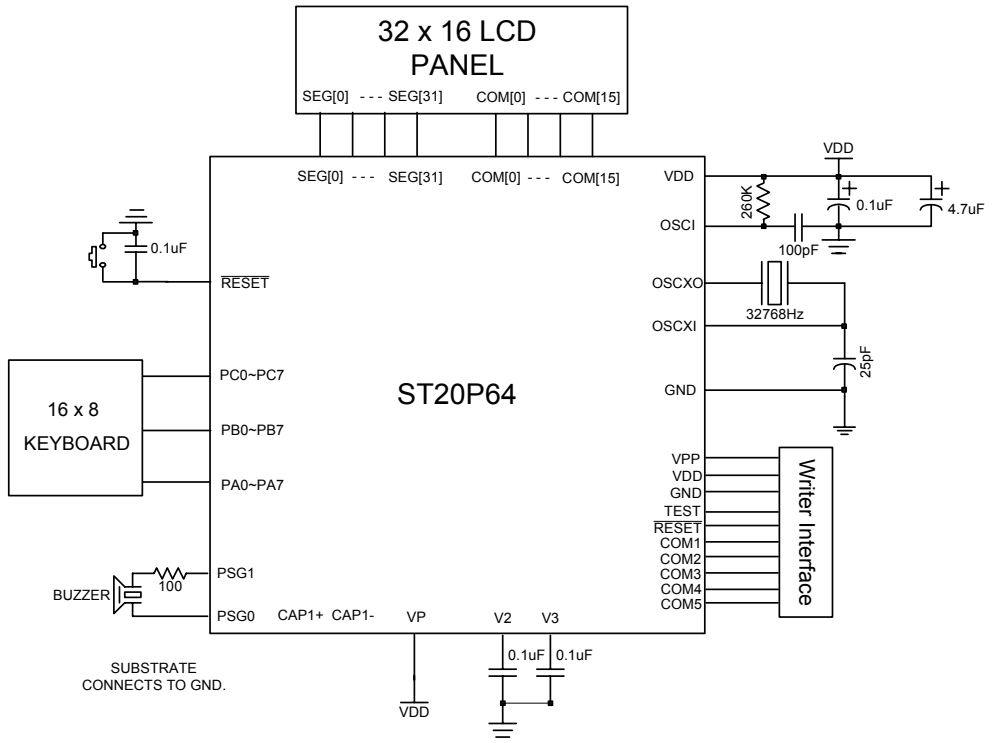
APPLICATION CIRCUIT WITH LCD KEYBOARD AWAKING PULSE

Note:

1. COMs and SEGs output GND level, while the LCD is turned off.
2. If LCD is turned off, Keyboard Awaking Pulses must be turned off at the same time.

5.2 APPLICATION CIRCUIT UNDER 5V OPERATING VOLTAGE

- VDD : 5V
- Clock : 32768Hz crystal and 2.0MHz RC oscillator
- LCD : 1/16 duty
- I/O : PORT A/B/C
- ALARM : PSG0, PSG1



APPLICATION CIRCUIT WITHOUT DC-DC CONVERTER

ST21XX Series

Part No.	ST2104A/B	ST2108	ST2100
ROM	4Mbits	8Mbits	16Mbits
RAM	4KB	4KB	4KB
Max. LCD	65x24/73x16	73x24	128x48
LCD driver	Built-in	Built-in	External
I/O	24	24	24
Memory extend	No	No	8M Bytes
Audio output	8-bit PWM	8-bit PWM	8-bit PWM

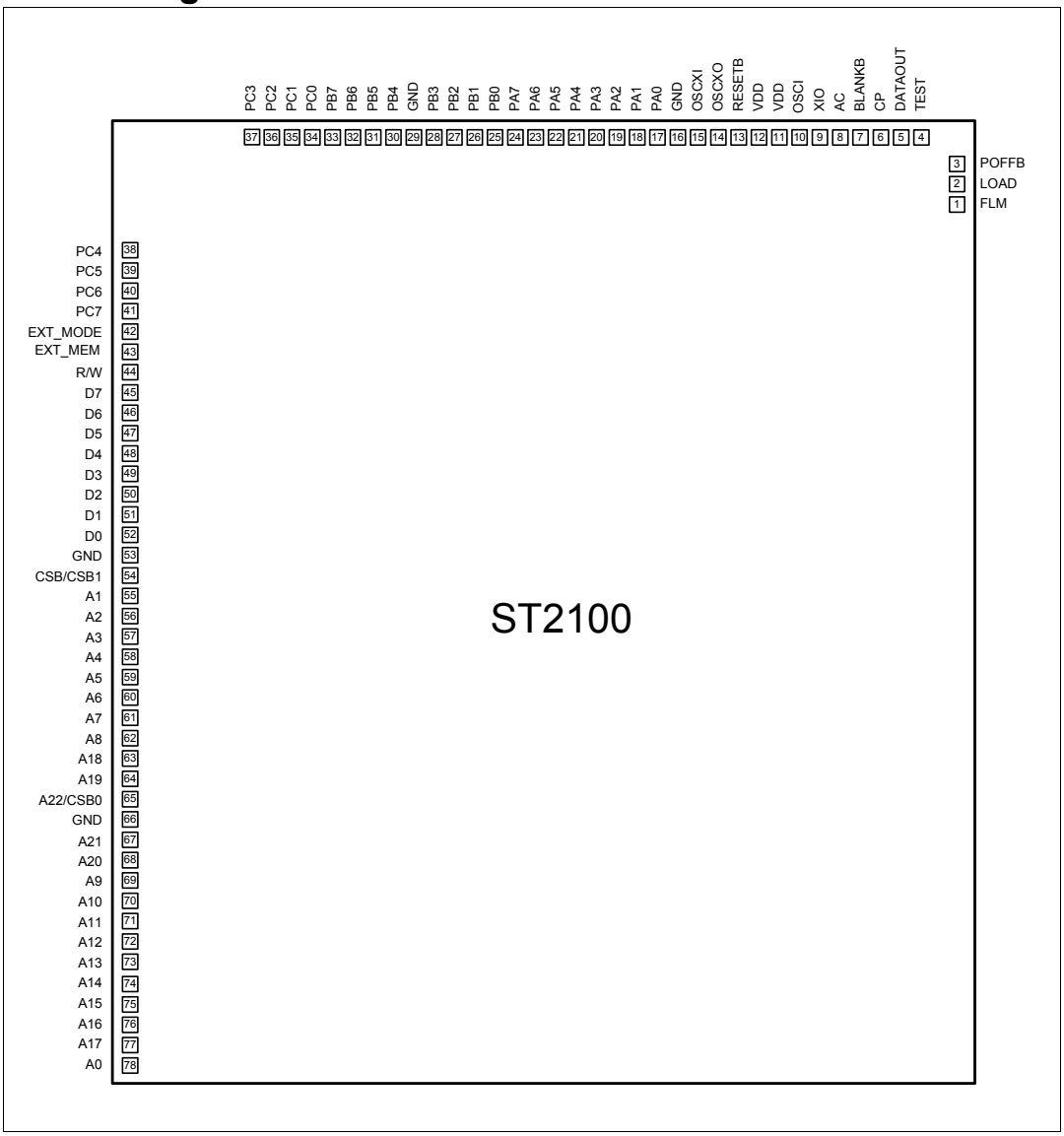
1. Features

- Totally static 8-bit CPU
- ROM: 2M x 8 bits
- RAM: 4K x 8 bits
- Stack: Up to 128-level deep
- Operation voltage: 2.4V ~ 5.5V
- Operation frequency:
  - 3.0Mhz@2.4V(min.)
  - 4.0Mhz@2.7V(min.)
- External memory control up to 8M x 8 bits
- 24 CMOS bidirectional bit programmable I/O pins
- Hardware de-bounce option for input port
- Bit programmable pull-up for input port
- Timer/Counter :
  - Two 8-bit timer/16-bit event counter
  - One 8-bit Base timer
- Six powerful interrupt sources :
  - External interrupt (edge trigger)
  - TIMER0 interrupt
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
  - DAC reload interrupt
- Dual clock sources with warm-up timer :
  - OSCX:Crystal oscillator 32.768K Hz
  - OSCI: RC oscillator 500K ~ 4M Hz or OSCI,XIO: Resonator 500K ~ 4M Hz (code option)
- Direct Memory Access (DMA)
- LCD controller with two panel size :
  - 6144 (128x48) dots
  - 4096 (128x32) dots
- Programmable Sound Generator (PSG) includes :
  - Dual Tone generator
  - Noise generator
  - 16 level volume sound effect generator
  - Digital DAC for speech / tone
- Three power down modes :
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. General Description

The ST2100 is a single chip micro-controller designed with CMOS silicon gate technology. This single chip micro-controller is useful for business equipment and other consumer applications. It integrates with 8-bit CPU core, SRAM, timer, LCD driver, I/O port and mask program ROM. This chip built-in a dual-oscillator to enhance the chip performance.

3. Pad Diagram



4. Pad Description

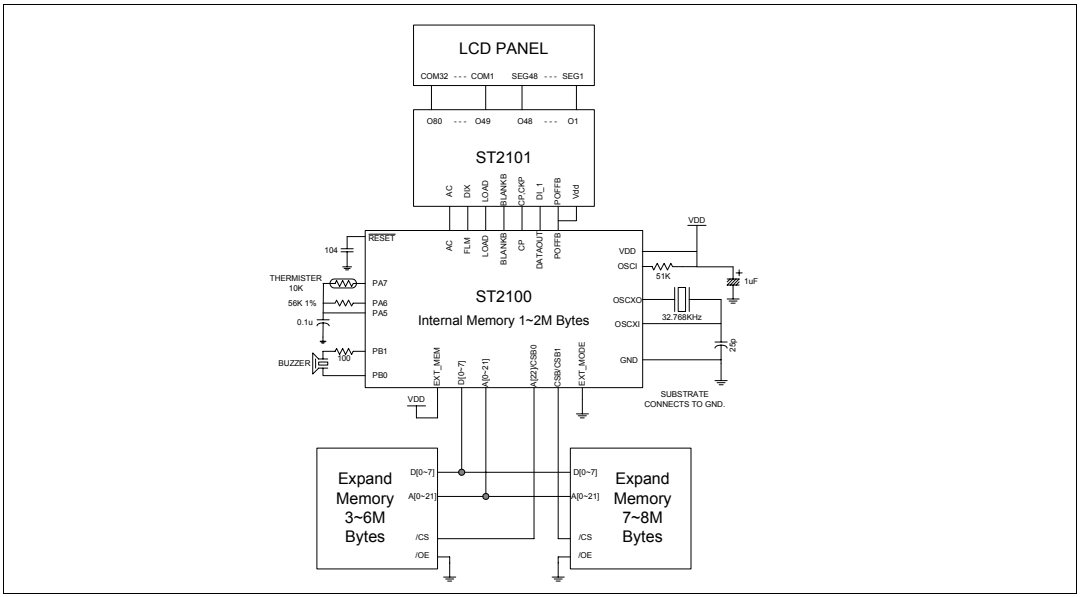
Pin No.	Designation	I/O	Description
13	$\overline{\text{RESET}}$	I	Pad reset input (active low)
16,29,53,66	GND	P	Ground Input and chip sub-strate
17-24	PORTA[0-7]	I/O	Programmable I/O, Transition Interrupt(edge active), INTX Interrupt , Timer Prescaler PRE16 clock source
25-28,30-33	PORTB [0-7]	I/O	Bit programmable I/O,PSG output, DAC output
34-41	PORTC [0-7]	I/O	Bit programmable I/O
55-64,67-78	A[0-21]	O	Address bus for expand memory
65	A[22]/CSB0	O	Address bus for expand memory / Expand memory chip select signal
45-52	D[0-7]	I/O	Data bus for expand memory
44	R/W	O	Read or write signal for expand memory
54	CSB/CSB1	O	Expand memory chip select signal
43	EXT_MEM	O	External memory enable/disable control signal
11	VDD	P	Power supply pin
14,15	OSCXO, OSCXI	I/O	OSCX I/O pin. For 32768Hz crystal used.
10	OSCI	I	RC oscillator pin, had to be connected to external resistor
4	TEST	I	Test pin for chip test, normal to NC.
1	FLM	O	First line mark for common signal(to LCD driver ST2101)
2	LOAD	O	Load data into Segment or common driver's data latch (to LCD driver ST2101)
8	AC	O	LCD alternating signal (connect to LCD driver ST2101)
3	POFFB	O	Control the power generator of voltage pumping circuit (to LCD driver ST2101)
9	XIO	O	OSCI,XIO for resonator 500K ~ 4M Hz (code option)
6	CP	O	Shift clock pulse for segment driver (to LCD driver ST2101)
5	DATAOUT	O	Output serial data for segment driver (to LCD driver ST2101)
7	BLANKB	O	LCD display can be turn off directly by external control. When BLANKB is low, the LCD display automatically set to blank state (to LCD driver ST2101).
42	EXT_MODE	I	Select {CSB,A[22]} or {CSB0,CSB1}
12	V_{DD}	P	Power supply pin

Legend: I = input, O = output, I/O = input/output, P = power.

5. Application Circuits

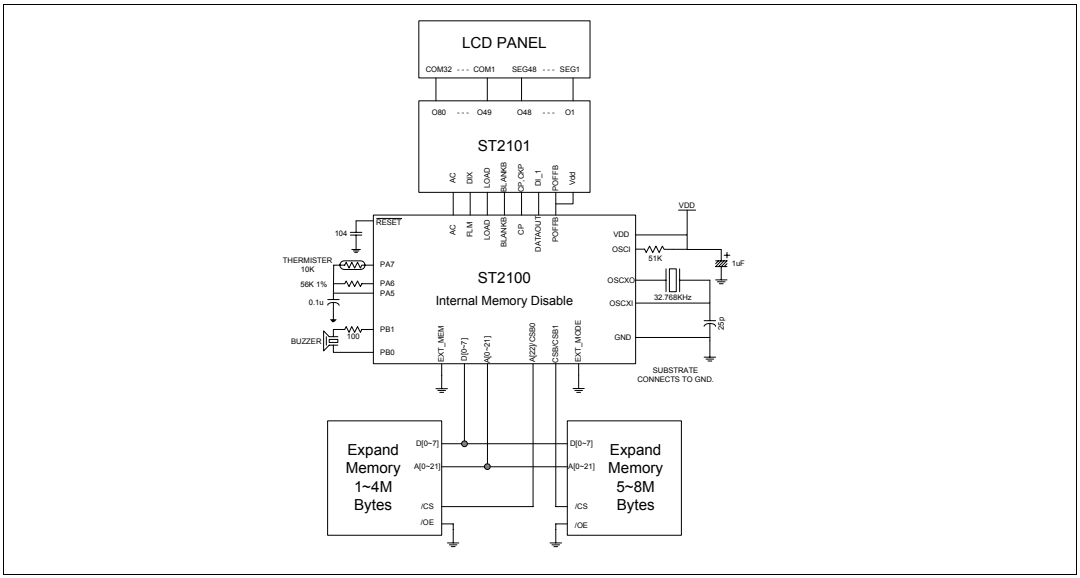
5.1 Application 1:

Internal memory = 1~2M bytes, Expand memory = 3~8M bytes.



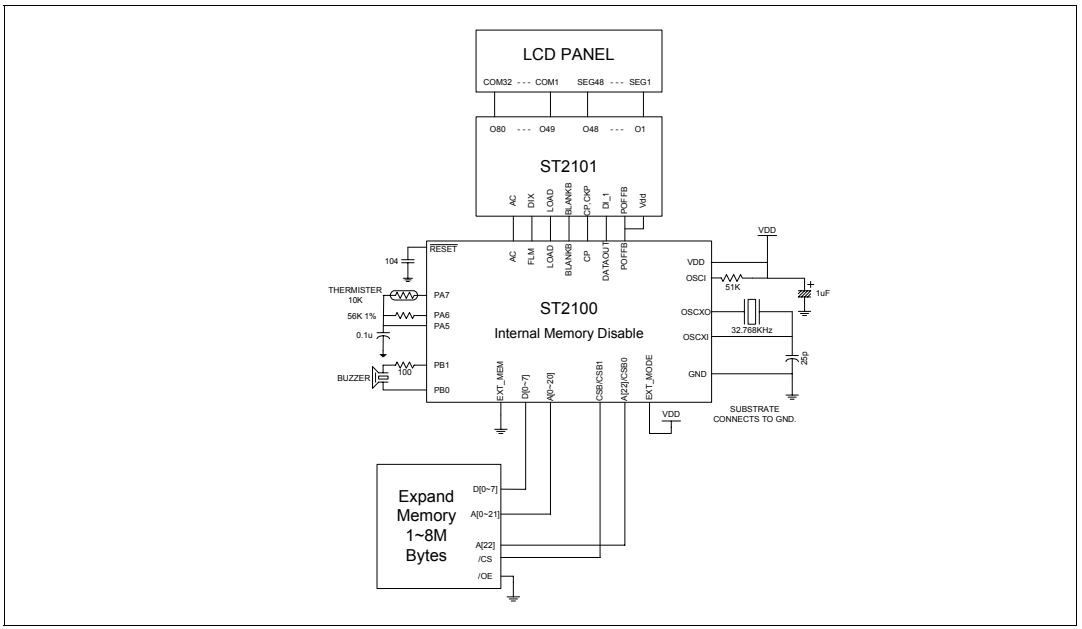
5.2 Application 2:

Internal memory = Disable, Expand memory = 1~8M bytes.



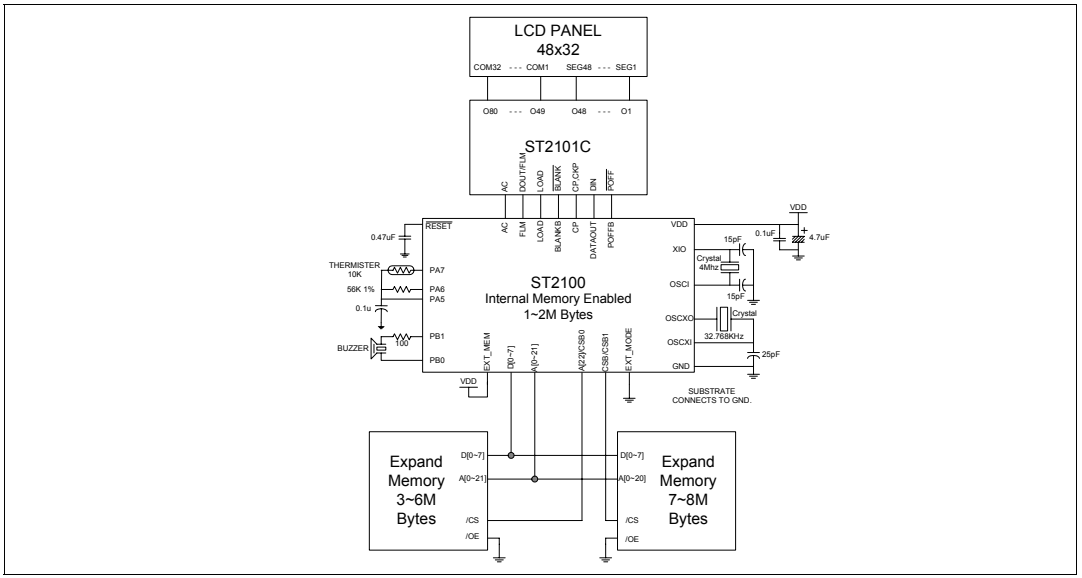
5.3 Application 3:

Internal memory = Disable, Expand memory = 1~8M bytes.



5.4 Application 4:

Internal memory = Enabled, Expand memory = 6M bytes.



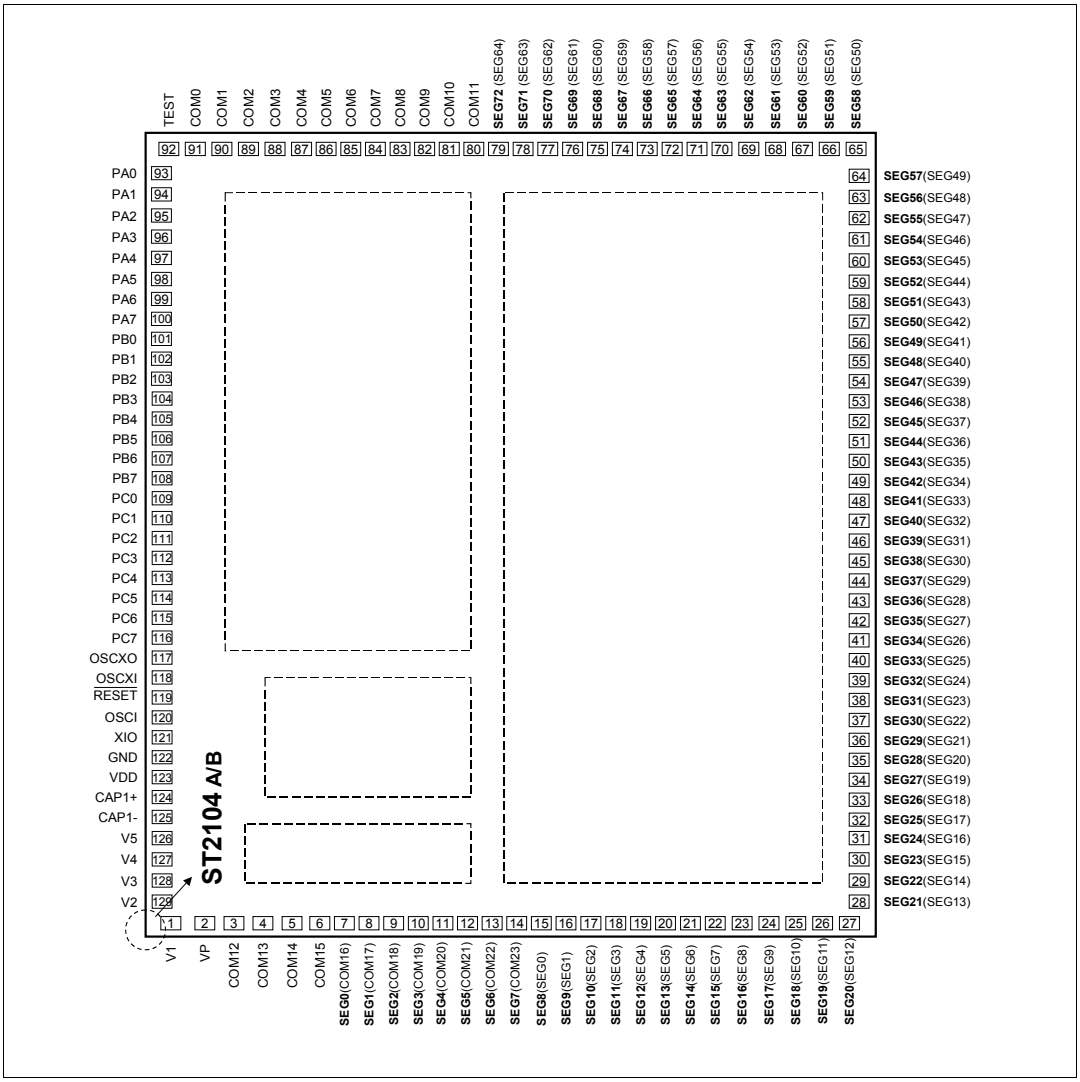
1. Features

- Totally static 8-bit CPU
- ROM: 512K x 8-bit
- RAM: 4K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage:
  - DC-DC converter enabled: 2.4V ~ 3.4V
  - DC-DC converter disabled: 2.4V ~ 5.5V
- Operation frequency:
  - 3.0Mhz@2.4V(min.)
  - 4.0Mhz@2.7V(min.)
- Built-in double DC-DC voltage converter for LCD driver
- I/O ports
  - 24 CMOS bidirectional bit programmable I/O pins
  - Bit programmable pull-up for input pins
  - Hardware de-bounce option for Port-A
- Low voltage detector
- Timer/Counter:
  - Two 8-bit timer/16-bit event counter
  - One 8-bit Base timer
- 6 hardware interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - Timer0 interrupt
  - Timer1 interrupt
  - Base timer interrupt
  - Port-A interrupt (transition triggered)
  - DAC reload interrupt
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator 32768 Hz
  - RC oscillator 500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (code option) 455K~4M Hz
- Direct memory access (DMA)
  - Block-to-Block move
  - Block to Single port
- LCD controller/driver
  - 16-level contrast control
  - 1168 (73x16) dots (1/16 duty, metal option)
  - 1560 (65x24) dots (1/24 duty, metal option)
- Programmable sound generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
- PWM DAC: Three modes up to 8-bit resolution
- Three power down modes:
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Applications

- Databank
- Translator
- Education Toys
- ELA
- Handhold LCD Game
- SCT calculator

3. Pad Diagram



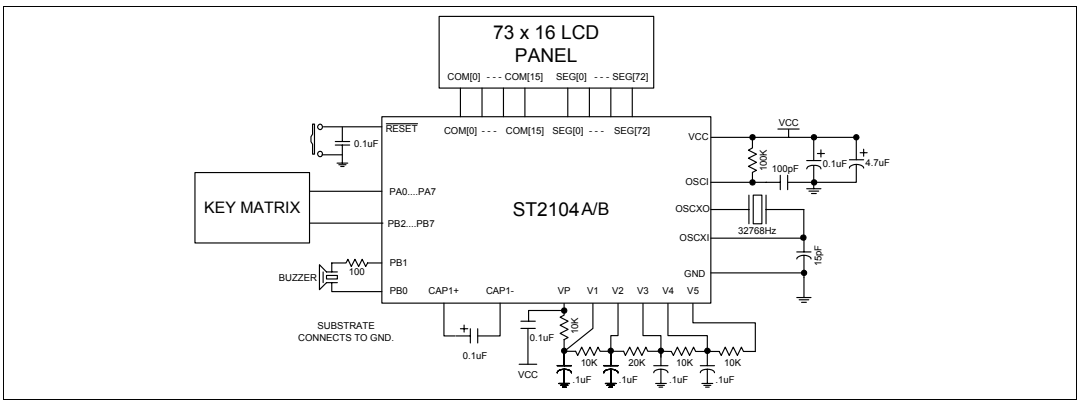
4. Pad Description

Pin No.	Designation	I/O	Description
7~14	SEG0(COM16)~ SEG7(COM23)	O O	- LCD segment drives 0~7 (1/16 duty mode) - LCD common drives 16~32 (1/24 duty mode)
15~79	SEG8(SEG0)~ SEG72(SEG64)	O O	- LCD segment drives 8~72 (1/16 duty mode) - LCD segment drives 0~64 (1/24 duty mode)
91~80, 3~6	COM0~11, 12~15	O	LCD common drives 0~15
92	TEST	I	Chip test function. Leave it open.
93	PA0 / INTX	I/O I I I	- Port-A bit programmable I/O - Edge-trigger Interrupt. - Transition-trigger Interrupt - Programmable Timer1 clock source
94~100	PA1~7	I/O I	- Port-A bit programmable I/O - Transition-trigger Interrupt
101,102	PB0, 1	I/O O	- Port-B bit programmable I/O
103~108	PB2~7	I/O	Port-B bit programmable I/O
109~116	PC0~7	I/O	Port-C bit programmable I/O
117, 118	OSCXO, OSCXI	I/O	Low frequency crystal oscillator I/O pins. Connect to external 32768 Hz crystal.
119	$\overline{\text{RESET}}$	I	Reset signal input (low active)
120	OSCI	I I	- RC oscillator input pin. Connected to external resistor - High frequency crystal/resonator oscillator input pin. Connect to external crystal/resonator.
121	XIO	O	High frequency crystal/resonator oscillator output pin. Connect to external crystal/resonator.
122	GND	P	Ground
123	VCC	P	Power supply
124	CAP1+	I/O	Connect to booster capacitor positive(+) terminal
125	CAP1-	I/O	Connect to booster capacitor negative(-) terminal
1, 129~126	V1, V2~V5	I	Inputs of external power supply for LCD drives
2	VP	O	Voltage output of booster circuit

Note: I = input, O = output, I/O = input/output, P = power.

5. Application Circuit

- VCC : 3.0V
- CLOCK : RC 2M Hz and crystal 32768 Hz
- LCD : 73 x 16
- KEY : 48 key



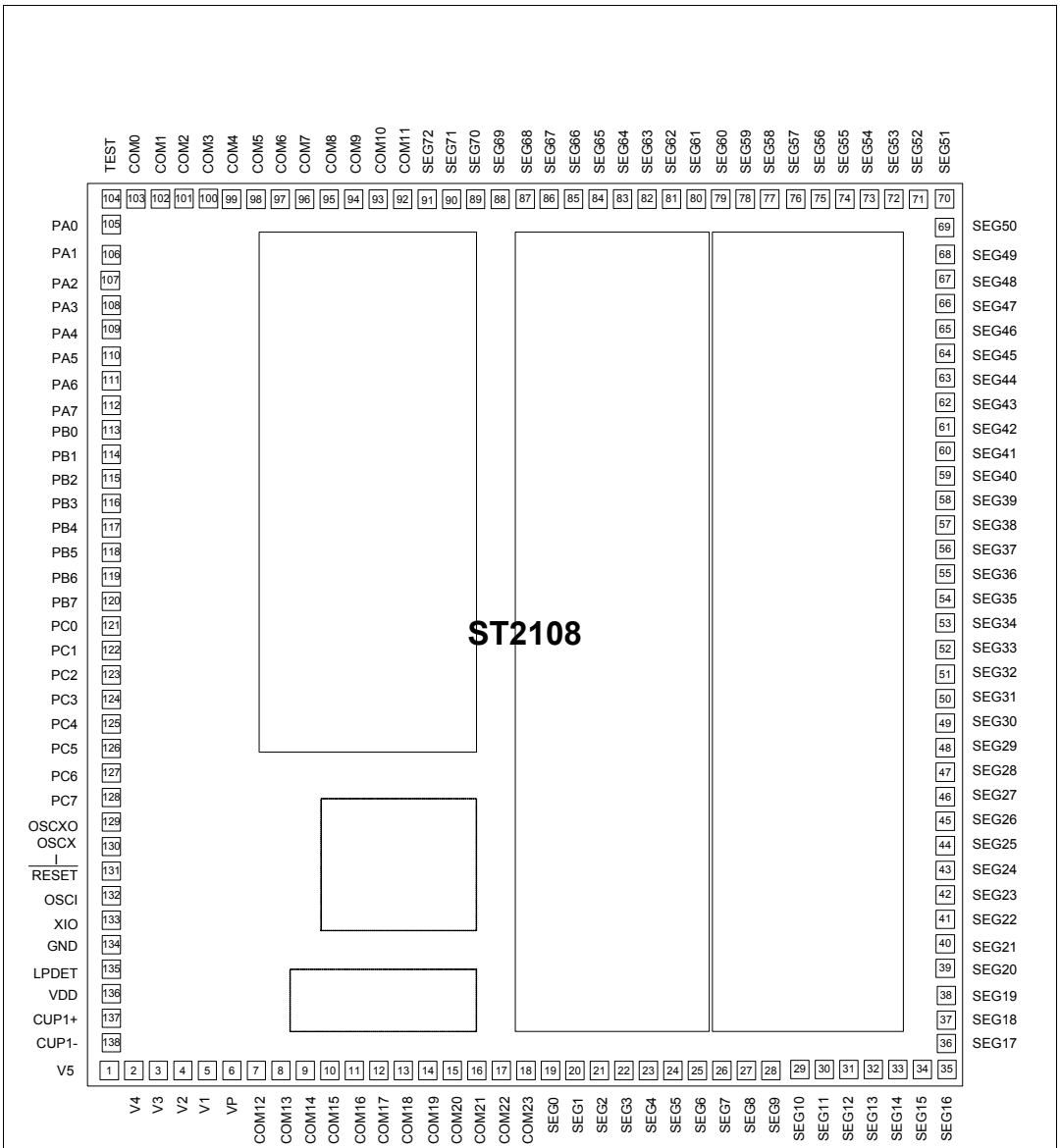
1. Features

- Totally static 8-bit CPU
- ROM: 1M x 8-bit
- RAM: 4K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage:
  - DC-DC converter enabled: 2.4V ~ 3.4V
  - DC-DC converter disabled: 2.4V ~ 5.5V
- Operation frequency:
  - 3.0Mhz@2.4V(min.)
  - 4.0Mhz@2.7V(min.)
- I/O ports
  - 24 CMOS bidirectional bit programmable I/O pins
  - 8 output pins (shared with LCD common output)
  - Bit programmable pull-up for input pins
  - Hardware de-bounce option for Port-A
- Low voltage detector
- Timer/Counter:
  - Two 8-bit timer/16-bit event counter
  - One 8-bit Base timer
- 6 Prioritized interrupt sources
  - External interrupt (edge triggered)
  - Timer0 interrupt
  - Timer1 interrupt
  - Base timer interrupt
  - Port-A[7~0] interrupt (transition triggered)
  - DAC reload interrupt
- Dual clock source with warm-up timer
  - Crystal oscillator 32.768K Hz
  - RC oscillator 500K~4M Hz
  - Resonator oscillator (code option) 455K~4M Hz
- Direct memory access (DMA)
  - Block-to-Block move
  - Block to Single port
- LCD controller
  - 16-level contrast control
  - 1752 (73x24) dots (1/24 duty)
  - 1168 (73x16) dots (1/16 duty)
- Programmable sound generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
- PWM DAC: Three modes up to 8-bit resolution
- Three power down modes:
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Applications

- Translator & Dictionary
- Databank
- LCD Toys
- ELA
- Handhold LCD Game

3. Pad Diagram



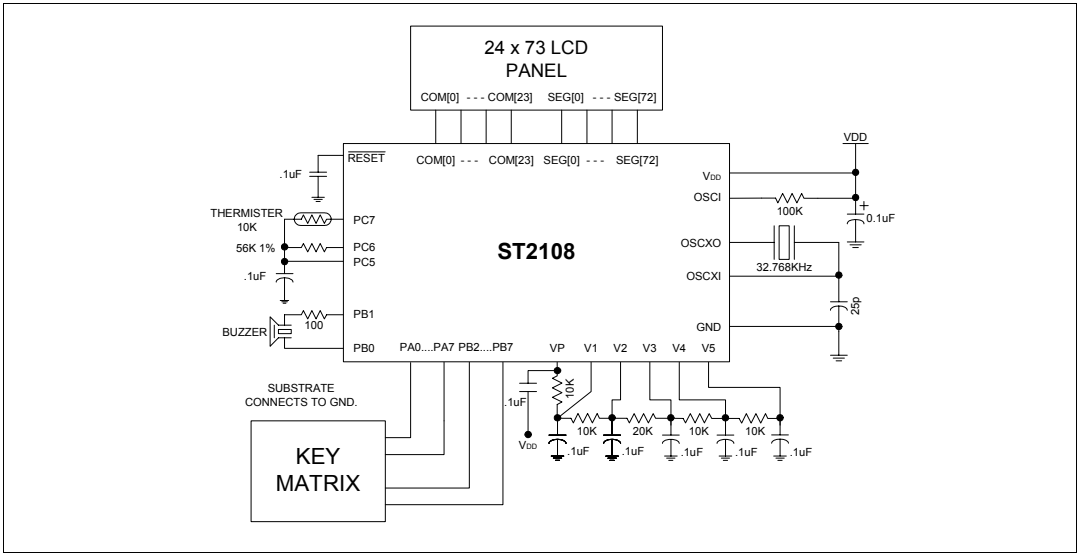
4. Pad Description

Pin No.	Designation	I/O	Description
19~91	SEG 0~72	O	LCD segment output
103~92, 7~18	COM 0~23	O	LCD common output
105	PA0 / INTX	I/O I I I	Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source
106~112	PA 1~7	I/O I	Port-A bit programmable I/O Transition-trigger Interrupt
113,114	PB 0, 1	I/O O	Port-B bit programmable I/O PSG/DAC Output
115~120	PB 2~7	I/O	Port-B bit programmable I/O
121~128	PC 0~7	I/O	Port-C bit programmable I/O
131	$\overline{\text{RESET}}$	I	Pad reset input (low active)
134	GND	P	Ground Input and chip substrate
136	V_{DD}	P	Power supply
129, 130	OSCXO, OSCXI	I/O	OSC I/O pin. For 32768Hz crystal used.
132	OSCI	I	RC oscillator pin, had to be connected to external resistor
133	XIO	I	Resonator input pin
135	NC		
6	VP	O	LCD pumping voltage output
137	CUP1+	I/O	Pump capacitance 1 positive edge
138	CUP1-	I/O	Pump capacitance 1 negative edge
5~1	V1~V5	I	External LCD voltage supply
104	TEST	I	Test pin for chip test, normal to NC.

Note: I = input, O = output, I/O = input/output, P = power.

5. Application Circuits

- V_{DD} : 3.0v
- CLOCK : RC 2M Hz and crystal 32.768K Hz
- LCD : 24 x 73
- KEY : 48 key



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- CLOCK : RC 2M Hz and crystal 32.768K Hz
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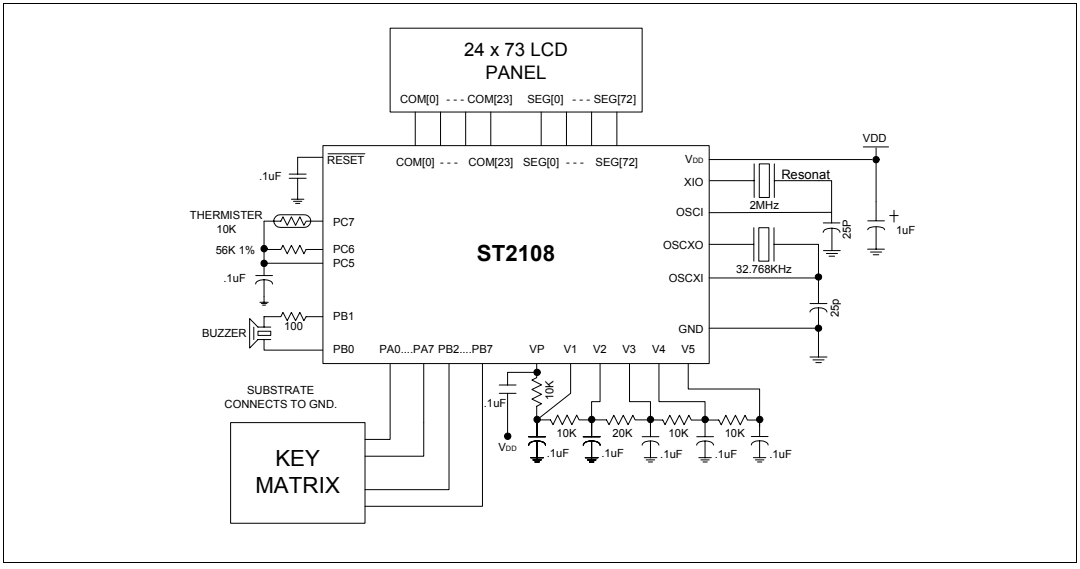


ST22XX Series

Part No.	ST2202	ST2204	ST2205U
ROM	256KB	512KB	512KB
RAM	4KB	10KB	32KB
I/O	48	48	56
Operation Voltage	2.4V~5.0V	2.4V~3.6V	2.4V~3.6V
Operation Speed	32K & 4MHz	32K & 4MHz	32K & 4/6MHz
LCD Size	160x80 -> 240x120	160x80 -> 340x120	160x80 -> 160xRGBx120
LCD Controller	B/W	4 Gray	16 Gray
PSG/ Volume control	2CH/ 16 level	2CH/ 16 level	4CH Wavetable/ 64 levels
DAC	8-bit PWM	8-bit PWM	9-bit PWM/ 12-bit Current
L.V.D.	V	V	V
L.V.R.	X	V	V
W.D.T.	V	V	V
Serial Interfaces	UART, SPI, IrDA	UART, SPI, IrDA	UART, SPI, IrDA, USB
Others			Nand Flash I/F Real Time Clock

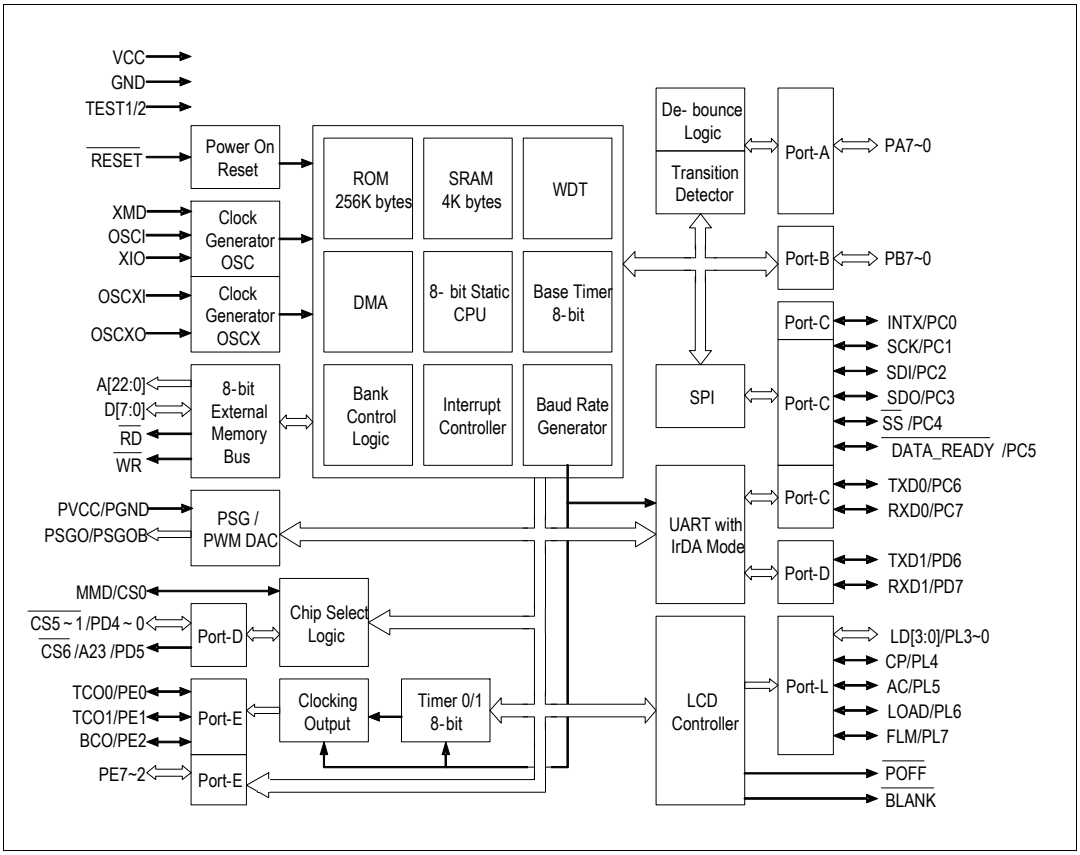
1. Features

- Totally static 8-bit CPU
- ROM: 256K x 8-bit
- RAM: 4K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage: 2.4V ~ 5.5V
- Operation frequency:
  - 3.0Mhz@2.4V(Min.)
  - 4.0Mhz@2.7V(Min.)
- Low Voltage Detector (LVD)
- Memory interface to ROM, RAM, Flash
- Memory configuration
  - Three kinds of bank for program, data and interrupts
  - 12-bit bank register supports up to 44M bytes
  - 6 programmable chip-selects with 4 modes
  - Maximum single device of 16M bytes at $\overline{CS5}$
- General-Purpose I/O (GPIO) ports
  - 48 multiplexed CMOS bidirectional bit programmable I/Os
  - Hardware de-bounce option for Port-A
  - Bit programmable pull-up for input pins
  - Bit programmable pull-up/down and open-drain/CMOS for Port-C
- Programmable Watchdog Timer (WDT)
- Timer/Counter
  - Two 8-bit timer, one can be a 16-bit event counter
  - One 8-bit Base timer with 5 coexistent interrupt time settings
- Three clocking outputs
  - Clock sources including Timer0/1, baud rate generator
- 11 prioritized interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - TIMER0 interrupt
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA interrupt (transition triggered)
  - DAC reload interrupt
  - LCD frame interrupt
  - SPI interrupt (x2)
  - UART interrupts (x2)
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator (OSCX) ..... 32768 Hz
  - RC oscillator (OSC) ..... 500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (Bonding option) ..... 455K~4M Hz
- Direct Memory Access (DMA)
  - Block-to-Block transfer
  - Block to Single port
- LCD Controller (LCDC)
  - Software programmable screen size up to 240X120 (including 160x160, 160x80, etc.)
  - Support 1-, 4-bit LCD data bus
  - Share system memory with display memory
  - Unique internal bus for memory sharing with no loss of the CPU time
  - Diverse functions including virtual screen , panning , scrolling , contrast control and alternating signal generator
  - Support software 16 gray levels
- Universal Asynchronous Receiver/Transmitter (UART)
  - Full-duplex operation
  - Baud rate generator with one digital PLL
  - Standard baud rates of 600 bps to 115.2 kbps
  - Direct glueless support of IrDA physical layer protocol
  - Two sets of I/Os (TX,RX) for two independent devices
- Serial Peripheral Interface (SPI)
  - Master and slave modes
  - 5 serial signals including enable and data-ready
  - One stage buffer for transmitter and receiver for continuous data exchange
  - Programmable data length from 7-bit to 16-bit
- Programmable Sound Generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
  - 8-bit PWM DAC for speech/voice
  - Two dedicated outputs for directly driving and large current
- Three power down modes
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Applications

- Dictionary & Translator
- Organizer/PDA
- Handhold Device
- Education learning aids
- LCD game

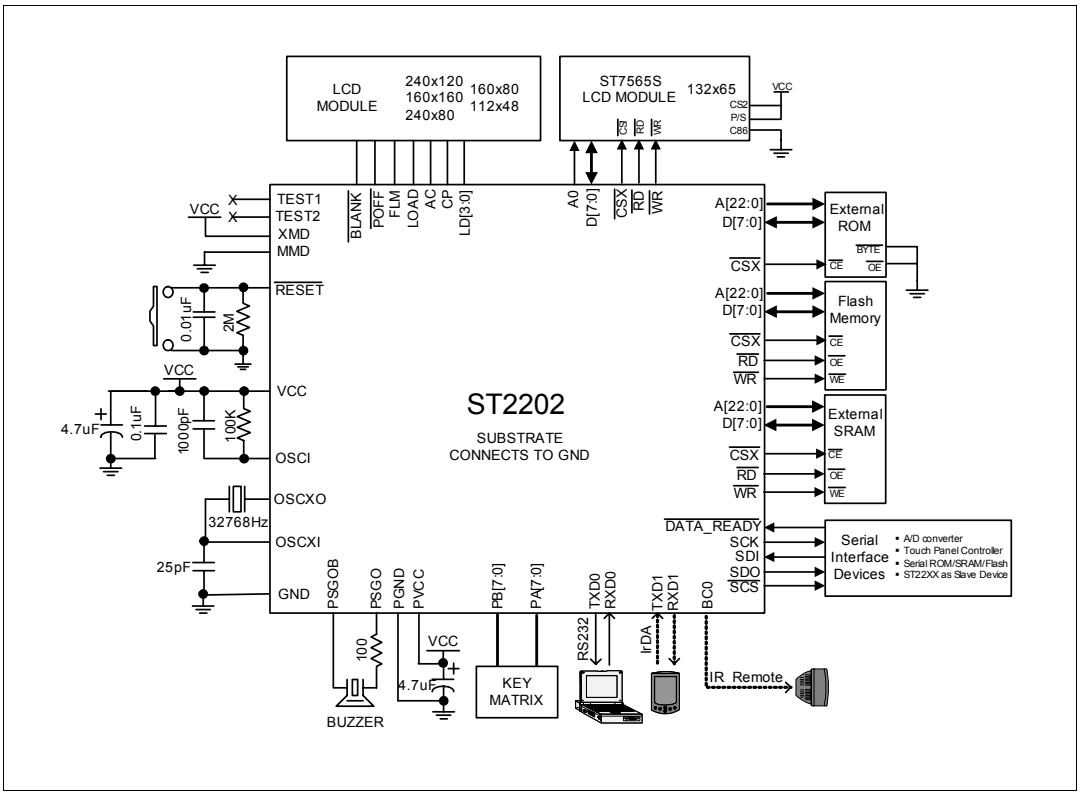
3. Block Diagram



4. Pad Description

Function Group	Pad No.	Designation	Description
Power	17, 52, 90	VCC , PVCC	**VCC:** Power supply for system **PVCC:** Power supply for PSGO and PSGOB
Ground	22, 48, 49, 71	GND , PGND	**GND:** System power ground **PGND:** Power ground for PSGO and PSGOB
System control	15, 1, 77, 26	$\overline{\text{RESET}}$, TEST1/2 MMD/ $\overline{\text{CS0}}$	$\overline{\text{RESET}}$: Active low system reset signal input **TEST1/2:** Leave them open when normal operation **MMD/** $\overline{\text{CS0}}$: Memory modes selection pin **Normal mode**: Enable internal ROM. MMD/ $\overline{\text{CS0}}$ connects to GND. **Emulation mode:** Disable internal ROM. MMD/ $\overline{\text{CS0}}$ connects to chip-select pin of external ROM. One resistor should be added between VCC and this pin. After reset cycles, MMD/ $\overline{\text{CS0}}$ changes to be an output, and outputs signal $\overline{\text{CS0}}$.
Clock	16, 18~21	OSCXO, OSCXI, OSCI, XIO, XMD	**XMD:** High frequency oscillator (OSC) mode selection input **Low:** Crystal mode. One crystal or resonator should be connected between OSCI and XIO **High:** Resistor oscillator mode. One resistor should be connected between OSCI and VCC OSCXI, OSCXO: Connect one 32768Hz crystal between these two pins when using low frequency oscillator
External memory bus signals	69, 70	$\overline{\text{WR}}$, $\overline{\text{RD}}$	External memory R/W control signals
	2~4, 81~89, 91~101	A[22:0]	External memory address bus
	72~76, 78~80	D[7:0]	External memory data bus
PSG/PWM DAC	50, 51	PSGO, PSGOB	PSG outputs. Connect to one buzzer or speaker
Keyboard scan signal (return line)	23~25, 27~31	PA7~0	I/O port A
GPIO	32~39	PB7~0	I/O port B
Chip selects	61~66	$\overline{\text{CS6}}$ /A23/PD5 , / $\overline{\text{CS5~1}}$/PD4~0	I/O port D and chip-select outputs
UART	46, 47, 67, 68	RXD0/PC7 , TXD0/ PC6 , RXD1/PD7 , TXD1/PD6	UART signals and I/Os
SPI	41~45	$\overline{\text{DATA\_READY}}$ /PC5 , / $\overline{\text{SS}}$ / PC4 , SDO/ PC3 , SDI/PC2 , SCK/ PC1	SPI signals and I/Os
External interrupt	40	INTX/PC0	External interrupt inputs
Clocking output	53~55	BCO/PE2 , TCO1/PE1 , TCO0/PE0	Clocking outputs
GPIO	56~60	PE7~3	I/O port E
LCD controller	5~14	FLM/PL7, LOAD/PL6, AC/PL5 , CP/PL4, LD [3:0]/PL3~0, $\overline{\text{POFF}}$, $\overline{\text{BLANK}}$	LCD control signals

5. Application Circuits



Note: 1. The capacitor connected to $\overline{\text{RESET}}$ should be of the value not greater than 0.01uF.

2. The resistor in parallel with the reset capacitor helps a lot to generate correct reset signal and should not be removed. The drawback is an additional current of about 1.5 uA rises.

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1. Features

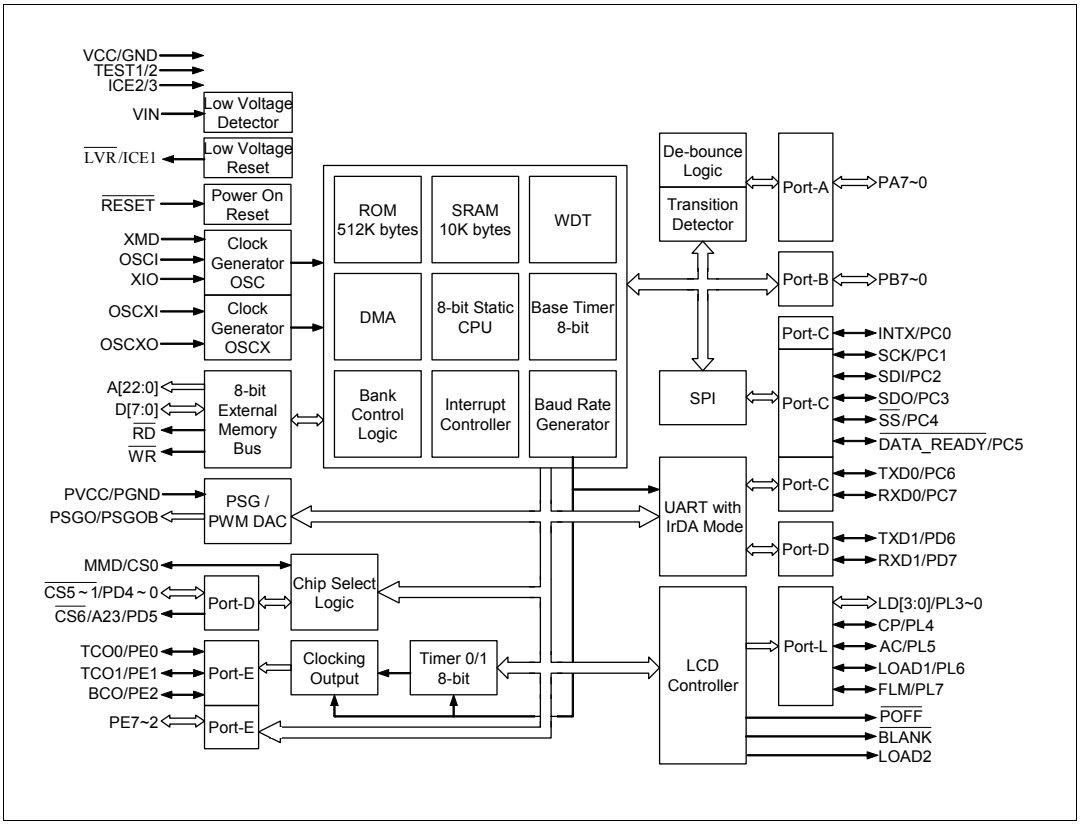
- Totally static 8-bit CPU
- ROM: 512K x 8-bit
- RAM: 10K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage: 2.4V ~ 3.6V
- Operation frequency:
  - 3.0Mhz@2.4V(Min.)
  - 4.0Mhz@2.7V(Min.)
- Low Voltage Detector (LVD)
- Low Voltage Reset (LVR)
- Memory interface to ROM, RAM, Flash
- Memory configuration
  - Three kinds of bank for program, data and interrupts
  - 12-bit bank register supports up to 44M bytes
  - 6 programmable chip-selects with 4 modes
  - Maximum single device of 16M bytes at $\overline{CS5}$
- General-Purpose I/O (GPIO) ports
  - 48 multiplexed CMOS bidirectional bit programmable I/Os
  - Hardware de-bounce option for Port-A
  - Bit programmable pull-up for input pins
  - Bit programmable pull-up/down and open-drain/CMOS for Port-C
- Programmable Watchdog Timer (WDT)
- Timer/Counter
  - Two 8-bit timer, one can be a 16-bit event counter
  - One 8-bit Base timer with 5 coexistent interrupt time settings

  Three clocking outputs
  - Clock sources including Timer0/1, baud rate generator
- 11 prioritized interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - TIMER0 interrupt
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA interrupt (transition triggered)
  - DAC reload interrupt
  - LCD frame interrupt
  - SPI interrupt (x2)
  - UART interrupts (x2)
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator (OSCX) ..... 32768 Hz
  - RC oscillator (OSC) ..... 500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (Bonding option) ..... 455K~4M Hz
- Direct Memory Access (DMA)
  - Block-to-Block transfer
  - Block to Single port
- LCD Controller (LCDC)
  - Software programmable screen size up to 240x240 (including 240X120, 160x160, 160x80, etc.)
  - Support 1-, 4-bit LCD data bus
  - Share system memory with display memory
  - Unique internal bus for memory sharing with no loss of the CPU time
  - Diverse functions including virtual screen , panning , scrolling , contrast control and alternating signal generator
  - Support software 16 gray levels
- Universal Asynchronous Receiver/Transmitter (UART)
  - Full-duplex operation
  - Baud rate generator with one digital PLL
  - Standard baud rates of 600 bps to 115.2 kbps
  - Direct glueless support of IrDA physical layer protocol
  - Two sets of I/Os (TX,RX) for two independent devices
- Serial Peripheral Interface (SPI)
  - Master and slave modes
  - 5 serial signals including enable and data-ready
  - One stage buffer for transmitter and receiver for continuous data exchange
  - Programmable data length from 7-bit to 16-bit
- Programmable Sound Generator (PSG)
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
  - 8-bit PWM DAC for speech/voice
  - Two dedicated outputs for directly driving and large current
- Three power down modes
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Applications

- Dictionary & Translator
- Organizer/ PDA
- Handhold Device
- Education learning aids
- LCD game

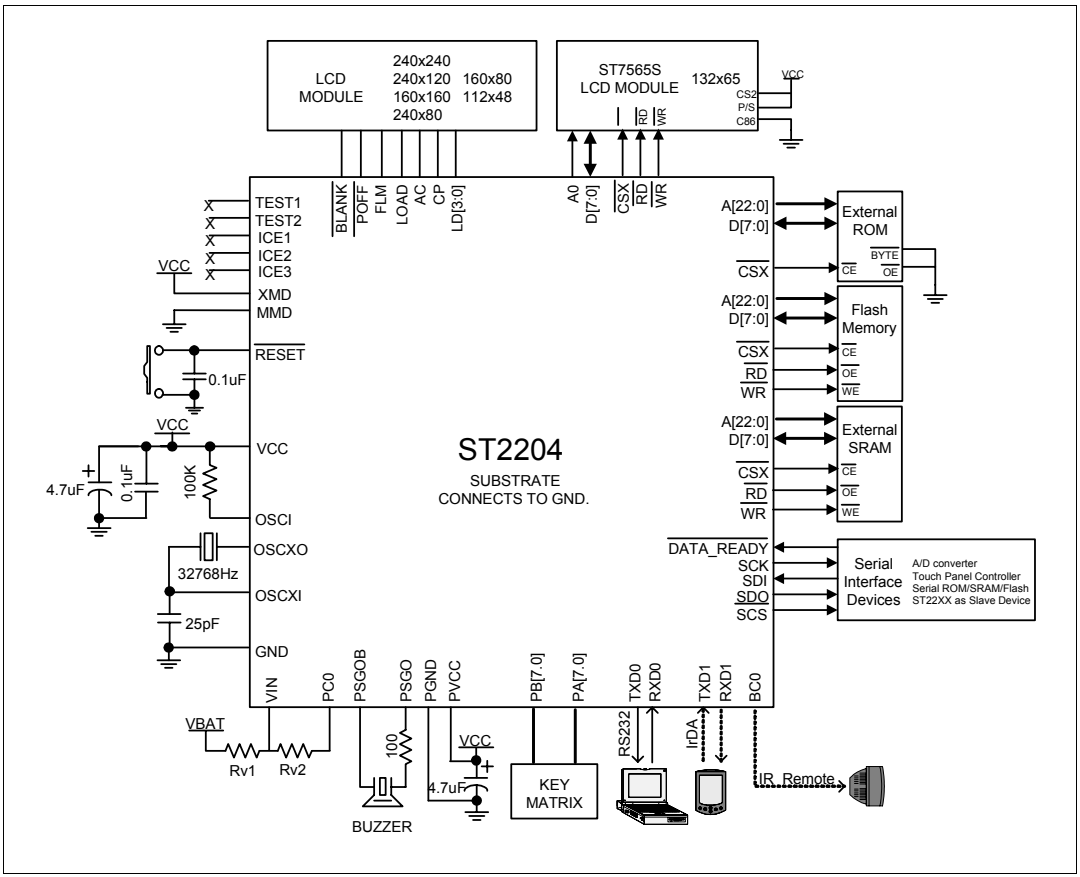
3. Block Diagram



4. Pad Description

Function Group	Pad No.	Designation	Description
Power	18,55, 94	VCC , PVCC	**VCC:** Power supply for system **PVCC:** Power supply for PSGO and PSGOB
Ground	23,51, 52, 74	GND , PGND	**GND:** System power ground **PGND:** Power ground for PSGO and PSGOB
System control	15, 26, 50,80, 1,81, 28	$\overline{\text{RESET}}$ $\overline{\text{LVR}}$ /ICE1, ICE2/3, TEST1/2 MMD/ $\overline{\text{CS0}}$	$\overline{\text{RESET}}$: Active low system reset signal input $\overline{\text{LVR}}$ /ICE1: $\overline{\text{LVR}}$:Low voltage reset signal output, connect this pin to $\overline{\text{RESET}}$ to make Low Voltage Reset function work. **ICE1:** function when in ICE mode. **TEST1/2, ICE2/3:** Leave them open when normal operation **MMD/CS0:** Memory modes selection pin **Normal mode:** Enable internal ROM. MMD/ $\overline{\text{CS0}}$ connects to GND. **Emulation mode:** Disable internal ROM. MMD/ $\overline{\text{CS0}}$ connects to chip-select pin of external ROM. One resistor should be added between VCC and this pin. After reset cycles, MMD/ $\overline{\text{CS0}}$ changes to be an output, and outputs signal $\overline{\text{CS0}}$.
Clock	16, 19~22	OSCXO, OSCXI, OSCI, XIO, XMD	**XMD:** High frequency oscillator (OSC) mode selection input **Low:** Crystal mode. One crystal or resonator should be connected between OSCI and XIO **High:** Resistor oscillator mode. One resistor should be connected between OSCI and VCC **OSCXI, OSCXO:** Connect one 32768Hz crystal between these two pins when using low frequency oscillator
External memory bus signals	72, 73	$\overline{\text{WR}}$, $\overline{\text{RD}}$	External memory R/W control signals
	2~4, 85~93, 95~105	A[22:0]	External memory address bus
	75~79, 82~84	D[7:0]	External memory data bus
PSG/PWM DAC	53, 54	PSGO, PSGOB	PSG outputs. Connect to one buzzer or speaker
Keyboard scan signal (return line)	24~25, 27,29~33	PA7~0	I/O port A
GPIO	34~41	PB7~0	I/O port B
Chip selects	64~69	$\overline{\text{CS6}}$/A23/PD5 , / $\overline{\text{CS5~1}}$/PD4~0	I/O port D and chip-select outputs
UART	48, 49, 70, 71	RXD0/PC7 , TXD0/ PC6 , RXD1/PD7 , TXD1/PD6	UART signals and I/Os
SPI	43~47	$\overline{\text{DATA\_READY}}$/PC5 , / $\overline{\text{SS}}$ /PC4 , SDO/ PC3 , SDI/PC2 , SCK/PC1	SPI signals and I/Os
External interrupt	42	INTX/PC0	External interrupt inputs
Clocking output	56~58	BCO/PE2 , TCO1/ PE1 , TCO0/PE0	Clocking outputs
GPIO	59~63	PE7~3	I/O port E
LCD controller	5~14, 106	FLM/PL7, LOAD/ PL6, AC/PL5 , CP/ PL4, LD[3:0]/PL3~0, $\overline{\text{POFF}}$, $\overline{\text{BLANK}}$	LCD control signals

5. Application Circuit



Note: 1. Connect one capacitor of 100pF to OSCI to stabilize the oscillation frequency. This capacitor must be close to OSCI

2. In case of Low Voltage Reset code option is not selected, the Low Voltage Reset function can still work by connecting $\overline{\text{LVR}}$/ICE1 to $\overline{\text{RESET}}$
Remove this connection when this code option is selected.

1. Features

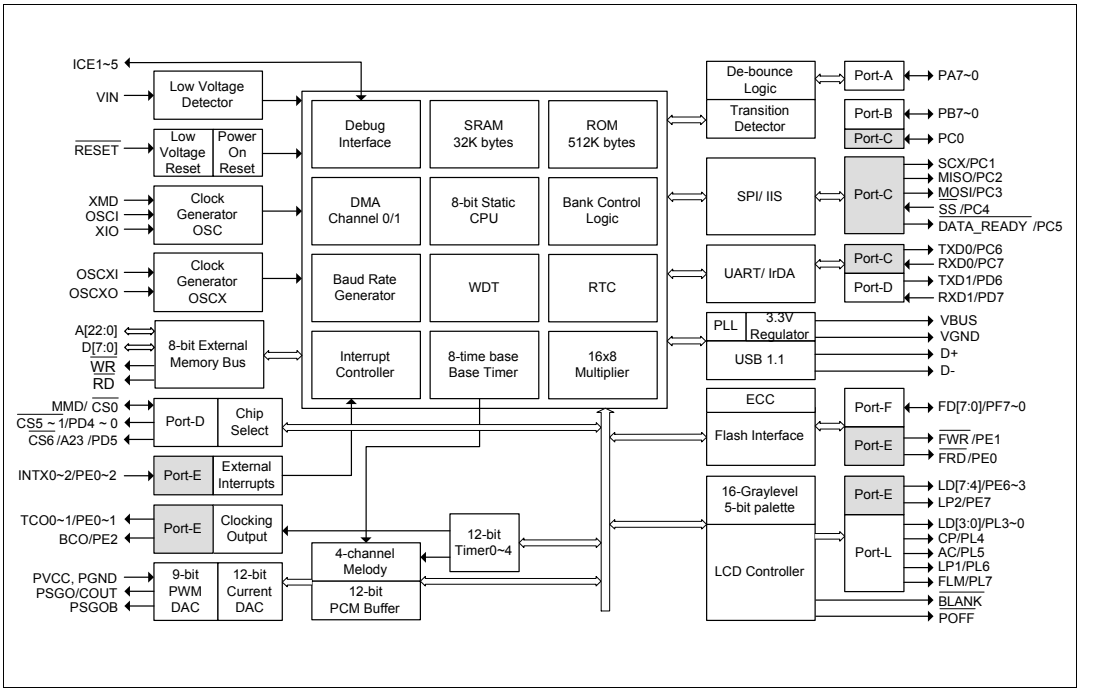
- Totally static 8-bit CPU
- ROM: 512K x 8-bit
- RAM: 32K x 8-bit
- Stack: Up to 128-level deep
- Operation voltage: 2.4V ~ 3.6V
- Operation frequency:
  - 4.0Mhz@2.4V(Min.)
  - 6.0Mhz@2.7V(Min.)
- One 16x8 Signed Multiplier
- Low Voltage Reset (LVR)
  - Two levels of code options
- Low Voltage Detector (LVD)
  - Programmable 4 levels
  - System power or external battery level can be detected.
- Flash Memory Interface
  - On the fly ECC code generation and detection
  - Fast data transfer with dedicated DMA channel
  - Nand and And type Flash supported
- USB 1.1 device
  - Integrate one PLL to produce 48Mhz clock
  - Built-in 3.3V regulator for transceiver
  - Mass storage class supported
  - Double buffering and direct buffer access increase throughput and ease real-time data transfer
- Direct Memory Access (DMA)
  - Two channels with special modes for Flash and display
  - Three address generation modes
- Memory configuration
  - Four kinds of banks for program, data, interrupt and internal RAM
  - 12-bit bank registers support up to 44M bytes
  - Six programmable chip-selects with 4 modes
  - Maximum single device of 16M bytes
- General-Purpose I/O (GPIO) ports
  - 56 multiplexed CMOS bit programmable I/Os
  - Hardware de-bounce option for Port-A
  - Bit programmable pull-up/down or open-drain/CMOS
- Timer/Counter
  - Four 12-bit timers
  - One 8-bit base timer
  - Seven fixed time bases
- Watchdog Timer (WDT)
  - Two selectable time bases
  - Programmable WDT interrupt or reset
- Real-time Clock (RTC)
  - Full clock function, second/ minute/ hour and day, with three counters and interrupts
  - One programmable alarm
- Three External Interrupt Sources
- Three clocking outputs
  - Clock sources including Timer0/1, baud rate generator
- Fourteen prioritized interrupts with dedicated exception vectors
  - External interrupts (x3) (edge triggered)
  - PortA interrupt (transition triggered)
  - LCD buffer interrupt
  - Base timer interrupt
  - Timer0~4 interrupts (x4)
  - SPI interrupts (x2)
  - UART interrupts (x2)
  - USB interrupt
  - RTC interrupt
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator (OSCX) .....32768 Hz
  - High frequency resistor or crystal/resonator oscillator (OSC) selected by pin option ....455K~4M Hz
- LCD Controller (LCDC)
  - Programmable display size:
    - COM: 512 max. SEG: 1024 max.
    - Max. 160xRGBx120 color STN supported by internal buffer
  - Hardware 4/16 gray levels with 5-bit palette, up to 4096 colors supported
  - Share system memory with display buffer and with no loss of the CPU time
  - Support 1-/4-/8-bit LCD data bus
  - Diverse functions including virtual screen, panning, scrolling, contrast control, alternating signal generator, buffer switching and fast graphic data manipulation
- Programmable Sound Generator (PSG)
  - Four channels with three playing modes: 9-bit ADPCM, 8-bit PCM and 8-bit melody
  - One 16-byte buffer and 6-bit volume control per channel
  - Wavetable melody support
  - Two dedicated PWM outputs for direct driving
  - One 12-bit current DAC

- Universal Asynchronous Receiver/ Transmitter (UART)
  - Full-duplex operation
  - Baud rate generator with one digital PLL
  - Standard baud rates of 600 bps to 115.2 kbps
  - Both transmitter and receiver buffers supported
  - Direct glueless support of IrDA physical layer protocol
  - Two sets of I/Os (TX,RX) for two independent devices
- Serial Peripheral Interface (SPI)
  - Inter IC sound (IIS) supported
  - Master and slave modes
  - Five serial signals including enable and data-ready
  - Both transmitter and receiver buffers supported
  - Programmable data length from 7-bit to 16-bit
- Three power down modes
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Applications

- Dictionary & Translator
- Organizer/ PDA
- Handhold Device
- Education learning aids
- LCD game

3. Block Diagram



4. Pad Description

Function Group	Pad Count	Designation	Description
Power	3	VCC , PVCC	**VCC:** Power supply for system **PVCC:** Power supply for PSGO and PSGOB
Ground	3	GND , PGND	**GND:** System power ground **PGND:** Power ground for PSGO and PSGOB
System control	8	$\overline{RESET}$, $\overline{LVR}$/ICE1, ICE2/3/4/5, TEST, MMD/ $\overline{CS0}$	$\overline{RESET}$**:** Active low system reset signal input $\overline{LVR}$**/ICE1:** $\overline{LVR}$: Low voltage reset signal output, connect this pin to RESET to make Low Voltage Reset function work. **ICE1**: ICE1 function when in ICE mode **TEST, ICE2/3/4/5:** Leave them open when normal operation **MMD/CS0:** Memory modes selection pin **Normal mode:** Enable internal ROM. MMD/$\overline{CS0}$ connects to GND. **Emulation mode:** Disable internal ROM. MMD/ $\overline{CS0}$ connects to chip-select pin of external ROM. One resistor should be added between VCC and this pin. After reset cycles, MMD/$\overline{CS0}$ changes to be an output, and outputs signal $\overline{CS0}$.
Clock	5	XMD, XIO,OSCI OSCXO,OSCXI, ,	**XMD:** High frequency oscillator (OSC) mode selection input **Low:** Crystal mode. One crystal or resonator should be connected between OSCI and XIO **High:** Resistor oscillator mode. One resistor should be connected between OSCI and VCC **OSCXI, OSCXO:** Connect one 32768Hz crystal between these two pins when using low frequency oscillator
External memory bus signals	2	$\overline{WR}$, $\overline{RD}$	External memory R/W control signals
	23	A[22:0]	External memory address bus
	8	D[7:0]	External memory data bus
PWM DAC Current DAC	2	PSGO/COUT, PSGOB	PSG outputs. Connect to one buzzer or speaker Also 10-bit current DAC output by register control
Keyboard scan signal (return line)	8	PA7~0	I/O port A
GPIO	9	PB7~0 PC0	I/O port B and PC0
Flash Data Bus	8	PD7~0/PF7~0	Flash data bus
Chip selects	6	$\overline{CS5\sim1}$/PD4~0, $\overline{CS6}$/A23/PD5	I/O port D and chip-select outputs
UART	4	RXD0/PC7,TXD0/PC6, RXD1/PD7,TXD1/PD6	UART signals and I/Os
SPI	5	$\overline{DATA\_READY}$/PC5 , $\overline{SS}$ /PC4 , SDO/PC3 , SDI/PC2 , SCK/PC1	SPI signals and I/Os

Function Group	Pad Count	Designation	Description
Clocking output/ External clock input or interrupt sources	3	BCO/INTX2/PE2 , TCO1/INTX1//PE1/ $\overline{\text{FWR}}$ TCO0/INTX0//PE0/ $\overline{\text{FRD}}$	■ When function bits are set, and I/O direction is output, and FEN=0, these three can be clocking outputs. ■ When function bits are set, and I/O direction is output, and FEN=1, PE0/1 are flash control signals ■ When function bits are set, and I/O direction is input, these three can be external clock inputs or external interrupt sources. ■ When function bits are cleared, they can be three GPIOs.
LCD control signals	15	FLM/PL7, LP1/PL6, AC/PL5 , CP/PL4, LD [3:0]/PL3~0, LD[7:4]/ PE6~3, LP2/PE7, $\overline{\text{POFF}}$, $\overline{\text{BLANK}}$,	LCD control signals

ST26XX Series

Part No.	ST2602	ST2604	ST2608
ROM	256KB	512KB	1MB
RAM	2KB	3KB	5KB
I/O	35 (8/27)	55(16/39)	56 (16/40)
Operation Voltage	2.4V~3.6V	2.4V~3.6V	2.4V~3.6V
Operation Speed	32K & 4MHz@2.7V 6MHz@3.0V	32K & 4MHz@2.7V 6MHz@3.0V	32K & 4MHz@2.7V 6MHz@3.0V
LCD Size	56X32	64X36	72X36
Ext. Driver-16 gray -Mono	~3000 dots ~12000 dots	~5000 dots ~20000 dots	~9000 dots ~36000 dots
LCD Controller	16 Gray	16 Gray	16 Gray
PSG/ Volume control	4CH Wavetable/ 64 levels	4CH Wavetable/ 64 levels	4CH Wavetable/ 64 levels
DAC	9-bit PWM/ 10-bit Current	9-bit PWM/ 10-bit Current	9-bit PWM/ 10-bit Current
L.V.D.	4 levels	4 levels	4 levels
L.V.R.	V	V	V
W.D.T.	V	V	V
Serial Interfaces	UART, SPI, IrDA	UART, SPI, IrDA	UART, SPI, IrDA
Others	Built-in LCD drives and power	Built-in LCD drives and power	Built-in LCD drives and power

1. Features

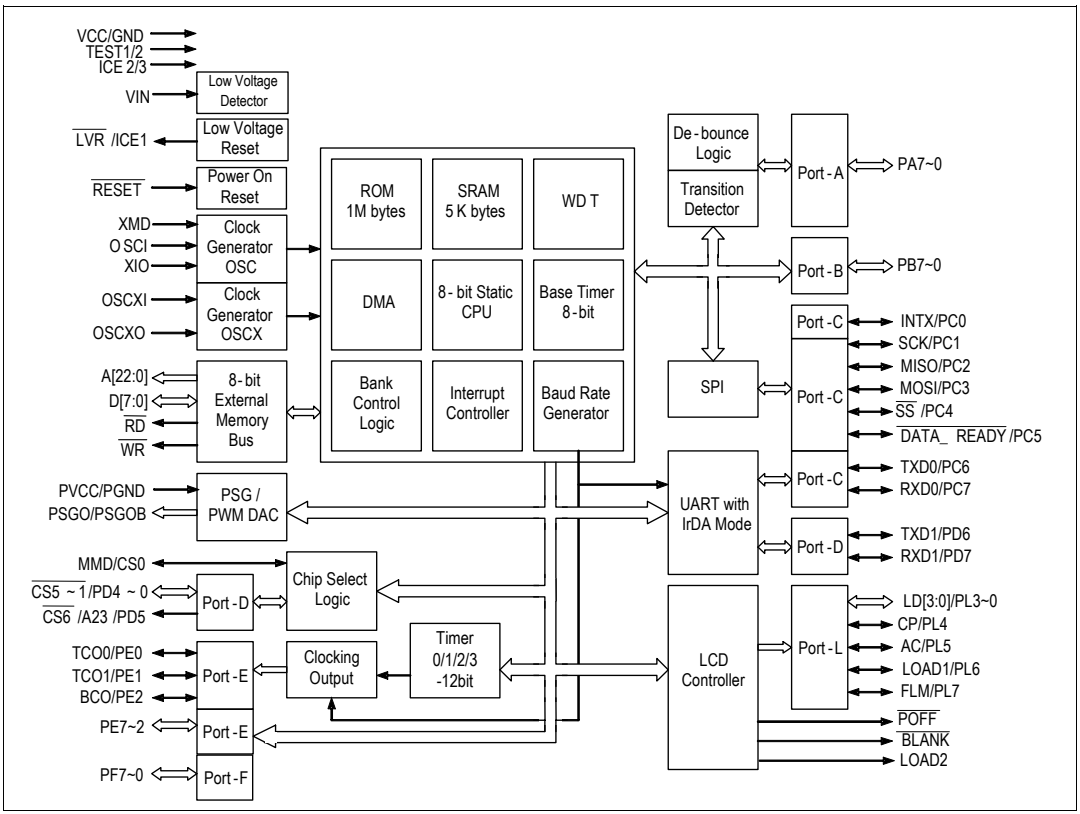
- Totally static 8-bit CPU
- ROM: 1M x 8-bit
- RAM: 5K x 8bit (Pin option)
- Stack: Up to 128-level deep
- Operation voltage: 2.4V ~ 3.6V
- Operation frequency:
  - 3.0Mhz@2.4V(Min.)
  - 4.0Mhz@2.7V(Min.)
  - 6.0Mhz@3.0V(Min.)
- One 8x8 Signed Multiplier
- Low Voltage Reset (LVR)
- Low Voltage Detector (LVD)
  - Programmable 4 levels
  - System power or external voltage level can be detected.
- Programmable Watchdog Timer (WDT)
- Memory interface to ROM, RAM, Flash
- Memory configuration
  - Three kinds of banks for program, data and interrupt
  - 12-bit bank registers support up to 44M bytes
  - Six programmable chip-selects with 4 modes
  - Maximum single device of 16M bytes
- General-Purpose I/O (GPIO) ports
  - Up to 56 bit programmable I/Os, 32 pins shared with LCD drives
  - Bit programmable pull-up for input pins
  - Hardware de-bounce option for Port-A
  - Pull-up/down and open-drain/CMOS control for Port-C
- Timer/Counter
  - Four 12-bit timers.
  - One 8-bit base timer
  - Seven fixed base-timers
- Three clocking outputs
  - Clock sources including Timer0/1, baud rate generator
- Twelve prioritized interrupts with dedicated exception vectors
  - External interrupt (edge triggered)
  - Port A interrupt (transition triggered)
  - LCD buffer interrupt
  - Base timer interrupt
  - Timer0~4 interrupts (x4)
  - SPI interrupts (x2)
  - UART interrupts (x2)
- Dual clock sources with warm-up timer
  - Low frequency crystal oscillator (OSCX) .....32768 Hz
  - High frequency resistor or crystal/resonator oscillator (OSC) selected by pin option ....455K~4M Hz
- Direct Memory Access (DMA)
  - Block-to-Block transfer
  - Block to Single port
- LCD Power Management
  - DC-DC converter with 8-level output control
  - LCD driving voltage regulator with 16-level control
  - 1/4, 1/5, 1/6 bias options with 4 voltage followers
- LCD Driver
  - COM: 36 outputs. Eight shared with one output port
  - SEG: 72 outputs. Shared with 3 I/O ports and memory bus signals.
  - 32x28~72x36 resolution, maximum 2592 dots
  - Segment cascade function supported
- LCD Controller (LCDC)
  - Software programmable display size up to 240X160
  - B/W, Hardware 4/16 gray levels with 5-bit palette
  - Support 1-/4-/8-bit LCD data bus
  - Share system memory with display buffer and with no loss of the CPU time
  - LCD buffer extension function to combine both internal and external RAM for larger display
  - Diverse functions including virtual screen, panning, scrolling, contrast control and alternating signal generator
- Programmable Sound Generator (PSG)
  - Four channels with three playing modes: 9-bit ADPCM, 8-bit PCM and 8-bit tone-melody
  - One 16-byte buffer and 6-bit volume control per channel
  - Wavetable melody support
  - Two dedicated PWM outputs for direct driving
  - One 10-bit current DAC

- Universal Asynchronous Receiver/Transmitter (UART)
  - Full-duplex operation
  - Baud rate generator with one digital PLL
  - Standard baud rates of 600 bps to 115.2 kbps
  - Both transmitter and receiver buffers supported
  - Direct glueless support of IrDA physical layer protocol
  - Two sets of I/Os (TX,RX) for two independent devices
- Serial Peripheral Interface (SPI)
  - Master and slave modes
  - Five serial signals including enable and data-ready
  - Both transmitter and receiver buffers supported
  - Programmable data length from 7-bit to 16-bit
- Three power down modes
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. Applications

- Dictionary & Translator
- Organizer / PDA
- Handheld Device
- LCD game
- Educational Learning Aid

3. Block Diagram



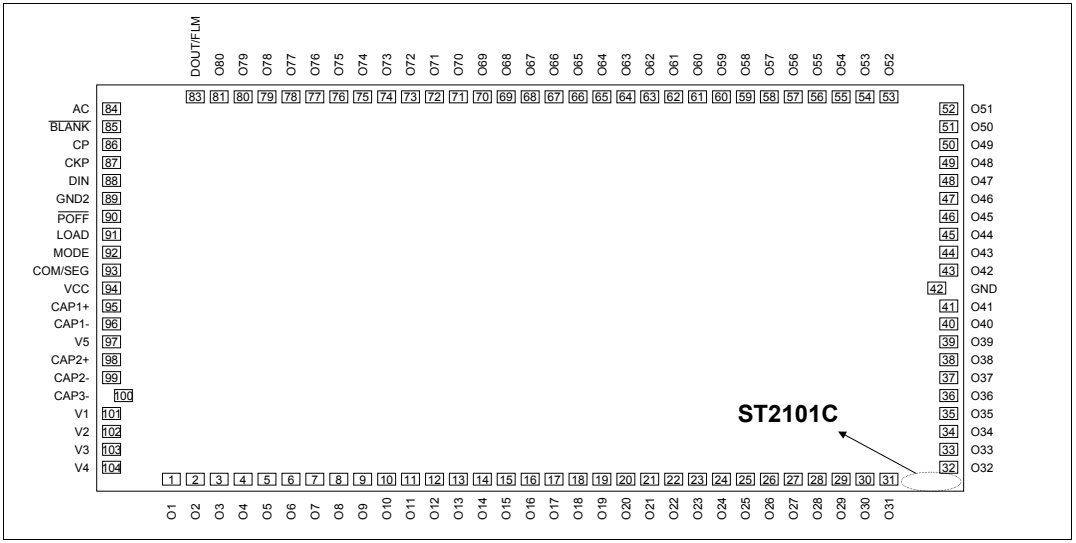
Low Cost LCD Driver Series

Part No.	#SEG x #COM	VDD	VLCD	Booster	IDD	I/O	Package
ST2101C	80S/C driver	2.5~5.5	Max. 13V	4x	550uA	1-bit	Bare chip
ST2501	80S/C driver	2.5~5.5	Max. 13V	4x	550uA	1-bit	Bare chip
ST2502	40S driver	2.5~5.5	Max. 11V	X	300uA	1-bit	Bare chip

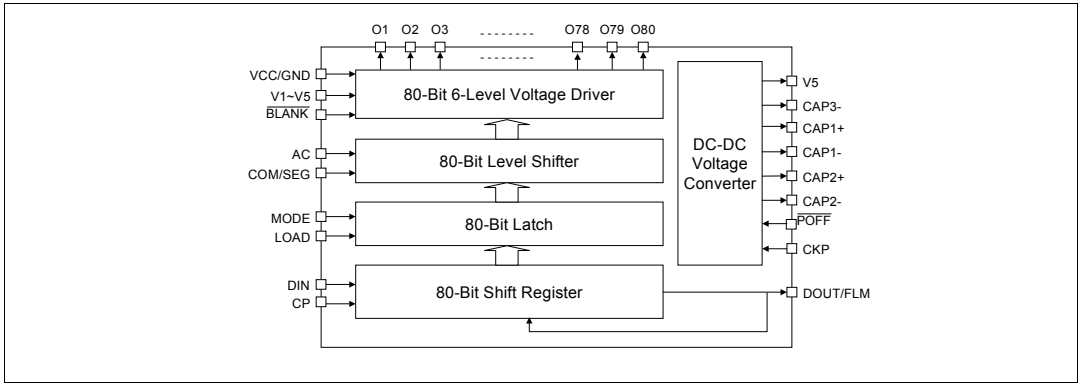
1. Features

- Number of LCD drive outputs: 80
- Supply voltage for LCD drive: +5.0 to +12.0 V
- Supply voltage for the logic system: +2.4 to +5.5 V
- Built-in double/triple/quad DC-DC voltage converter.
- Low power consumption
- Low output impedance
- 1-bit serial data input
- Interface with ST2100 LCD controller
- PWM contrast control function
- Programmable duty ratio: 1/32, 1/48, and 1/80
- Support cascade function to drive large size and high resolution panels

2. Pad Diagram



3. Block Diagram



4. Pad Description

Pin Number	Designation	I/O	Description
1~41,43~81	O1~O80	O	LCD common/segment drives
82	NC		
83	DOUT/FLM	I	- MODE="H":Connect to frame marker signal (FLM). Common data is input and shift at the falling edge of LOAD signal.
		O	- MODE="L": Segment (or common) data is shift and output from this pin. Connect to next ST2101C data input if two ST2101C are cascaded. Leave it open (NC) when there is no further connection.
84	AC	I	Alternating signal input for LCD drive waveform
85	$\overline{\text{BLANK}}$	I	Dual functions of display off and PWM contrast control signals input. - Display off : "L" pulse lasts for more than 2 lines will make all drives to output VCC level to turn the display off. - Contrast control :"L" pulse asserted during each line will makes the selected common drive to output non-selected level to disable this line and lower the effective driver voltage output.
86	CP	I	Clock pulse input pin for 80-bit shift register. Data is shifted at falling edge of clock. - Connect to LCD pixel clock for LCD segment data - Connect to line latch pulse (LOAD) for common data when 80-common mode is selected.
87	CKP	I	Clock is inputted from this pin and is divided by 32 to be the booster clock. Tie to VCC if voltage converter is not used.
88	DIN	I	80-bit shift register data input. - Connect to 1-bit LCD serial data input at segment function - Connect to frame marker signal (FLM) when 80-common mode is selected
90	$\overline{\text{POFF}}$	I	Voltage converter circuit on/off switch. - "H" :Turn on voltage converter, and display on/off control will be masked to be off until 2 AC cycle is passed. - "L" :Turn off voltage converter and force display to be off Note :To ensure the same display-on time, if two or more ST2101C are connected, all $\overline{\text{POFF}}$ must be connected together even those don't use their voltage converters.
91	LOAD	I	Latch pulse of the 80-bit display data latch at segment function. Shift clock input of shift register at common function. Data is latched when LOAD="H"
92,93	MODE, COM/SEG	I	- MODE="H": Mixed common and segment functions - MODE="L": Either common or segment function is selected

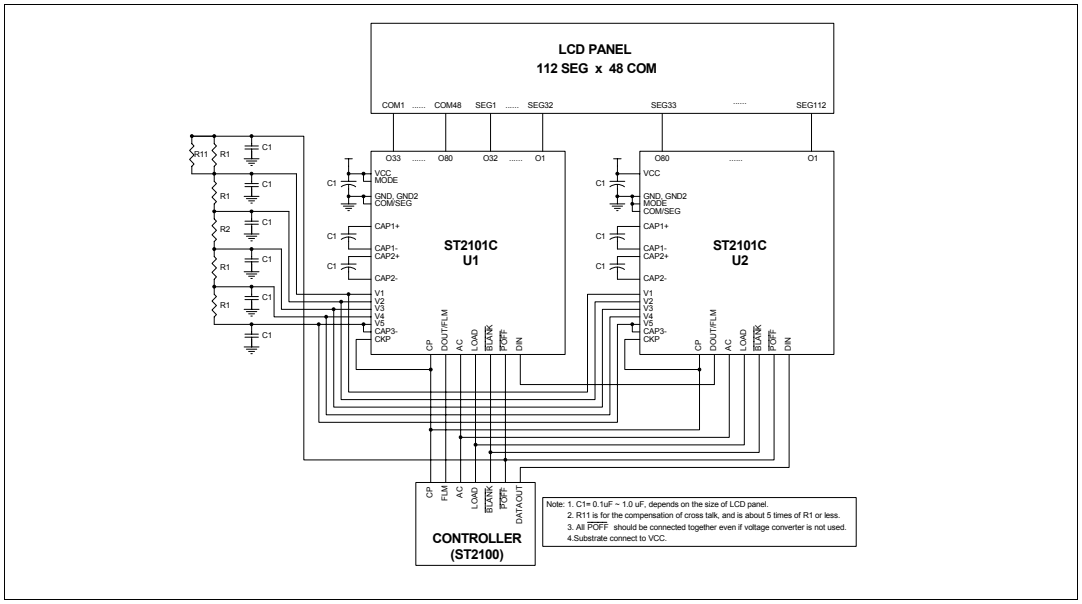
		COM/SEG	
		L	H
MODE	L	80 segments	80 commons
	H	32 seg / 48 com	48 seg / 32 com

94	V_{DD}	P	Power supply for logic and voltage converter circuit
42,89	GND, GND2	P	Ground
95	CAP1+	O	Connect to booster capacitor 1 positive(+) terminal
96	CAP1-	O	Connect to booster capacitor 1 negative(-) terminal
98	CAP2+	O	Connect to booster capacitor 2 positive(+) terminal
99	CAP2-	O	Connect to booster capacitor 2 negative(-) terminal
97	V5	O	Negative voltage output of booster circuit Power supply for LCD drives
100	CAP3-	O	Connect to booster capacitor 3 negative(-) terminal
101~104	V1~V4	I	Inputs of external power supply for LCD drives

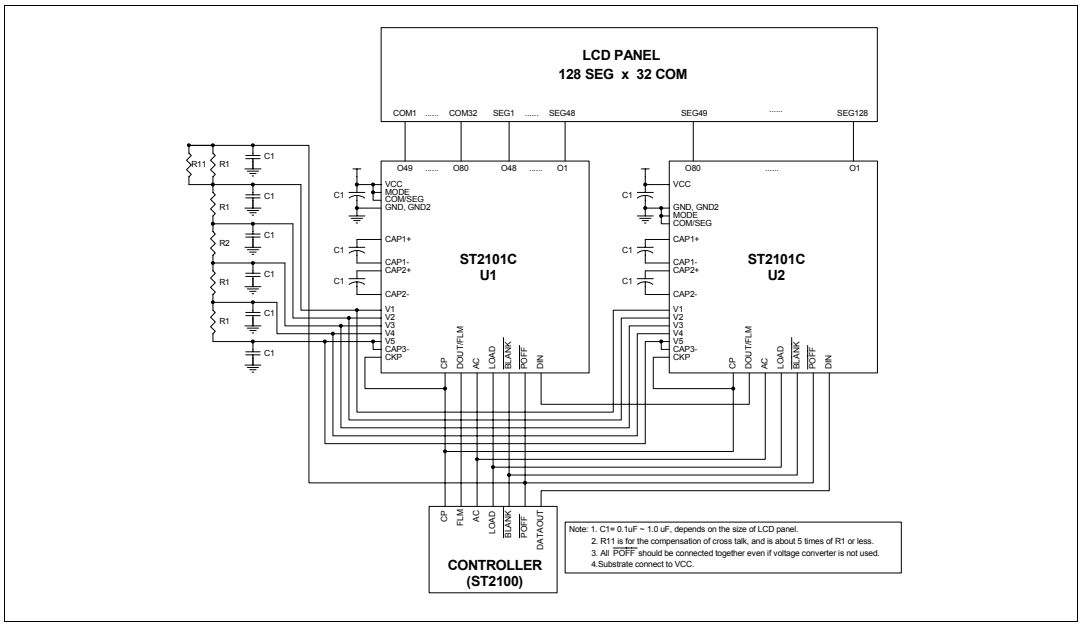
Note: P=power pin, I=input pin, O=output pin

5. Application Circuits

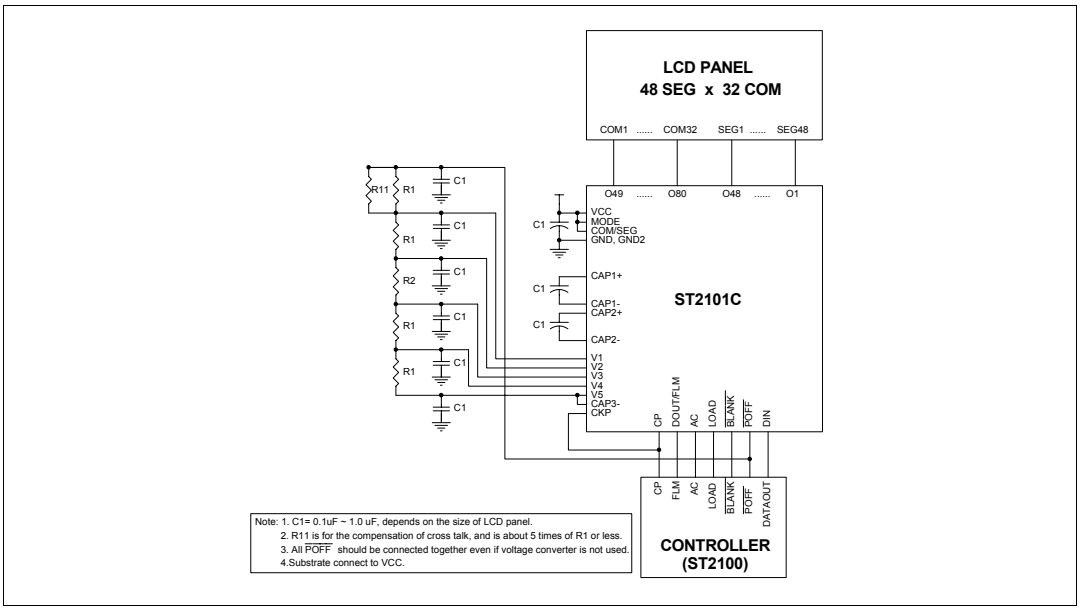
5.1 1/48 duty, 112 segments, 3X set-up



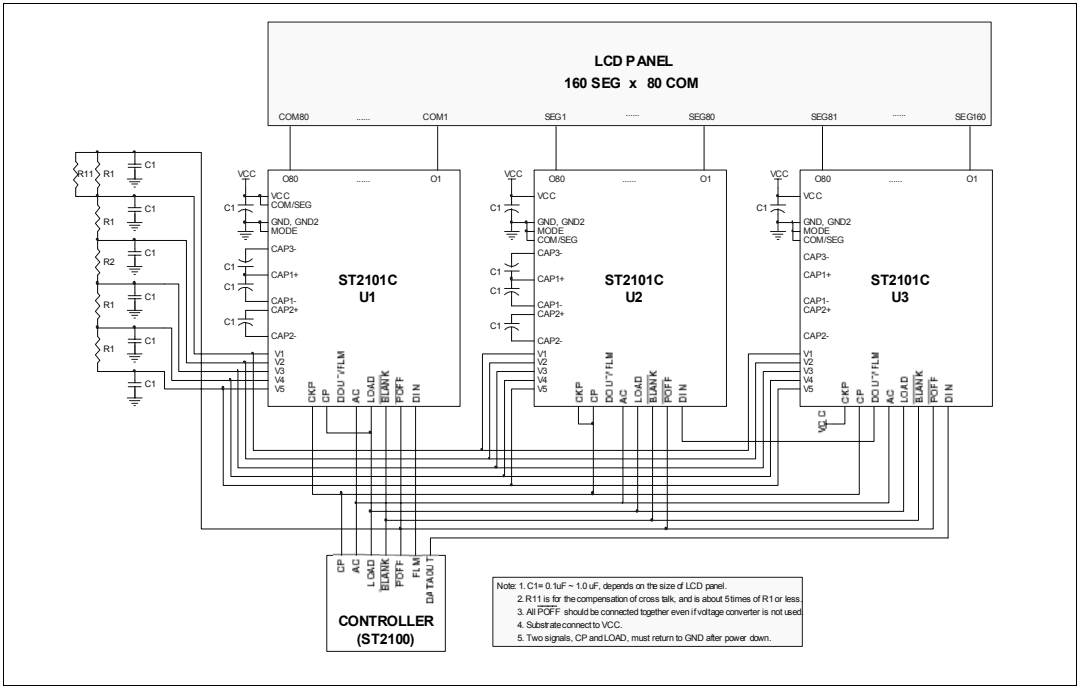
5.2 1/32 duty, 128 segments, 3X set-up



5.3 1/32 duty, 48 segments, 3X set-up



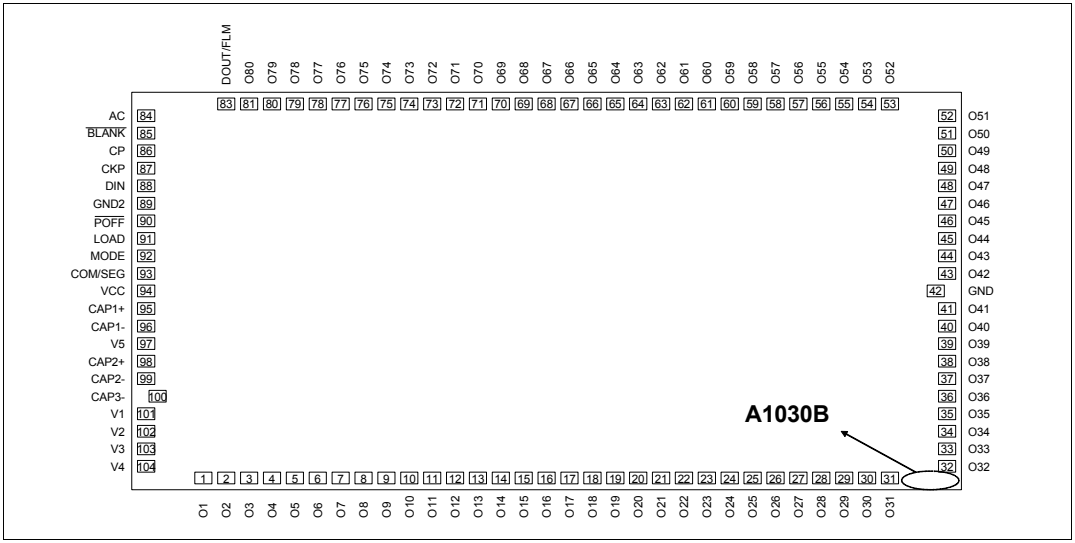
5.4 1/80 duty, 160 segments, 4X set-up



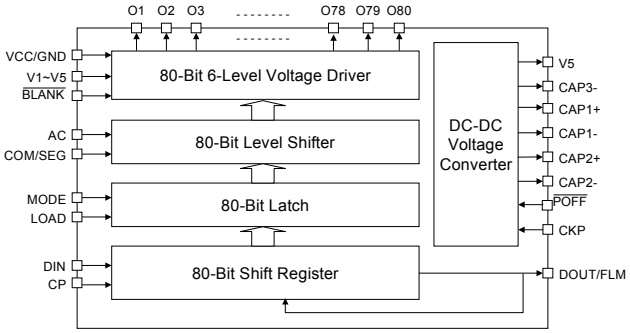
1. Features

- Number of LCD drive outputs: 80
- Supply voltage for LCD drive: +5.0 to +12.0 V
- Supply voltage for the logic system: +2.4 to +5.5 V
- Built-in double/triple/quad DC-DC voltage converter.
- Low power consumption
- Low output impedance
- 1-bit serial data input
- Interface with ST2100 LCD controller
- PWM contrast control function
- Programmable duty ratio: 1/32, 1/48, and 1/80
- Support cascade function to drive large size and high resolution panels

2. Pad Diagram



3. Block Diagram



4. Pad Description

Pin Number	Designation	I/O	Description
1~41,43~81	O1~O80	O	LCD common/segment drives
82	NC		
83	DOUT/FLM	I	- MODE="H":Connect to frame marker signal (FLM). Common data is input and shift at the falling edge of LOAD signal.
		O	- MODE="L": Segment (or common) data is shift and output from this pin. Connect to next ST2501 data input if two ST2501 are cascaded. Leave it open (NC) when there is no further connection.
84	AC	I	Alternating signal input for LCD drive waveform
85	$\overline{BLANK}$	I	Dual functions of display off and PWM contrast control signals input. - Display off : "L" pulse lasts for more than 2 lines will make all drives to output VCC level to turn the display off. - Contrast control :"L" pulse asserted during each line will makes the selected common drive to output non-selected level to disable this line and lower the effective driver voltage output.
86	CP	I	Clock pulse input pin for 80-bit shift register. Data is shifted at falling edge of clock. - Connect to LCD pixel clock for LCD segment data - Connect to line latch pulse (LOAD) for common data when 80-common mode is selected.
87	CKP	I	Clock is inputted from this pin and is divided by 32 to be the booster clock. Tie to VCC if voltage converter is not used.
88	DIN	I	80-bit shift register data input. - Connect to 1-bit LCD serial data input at segment function - Connect to frame marker signal (FLM) when 80-common mode is selected
90	$\overline{POFF}$	I	Voltage converter circuit on/off switch. - "H" :Turn on voltage converter, and display on/off control will be masked to be off until 2 AC cycle is passed. - "L" :Turn off voltage converter and force display to be off Note :To ensure the same display-on time, if two or more ST2501 are connected, all $\overline{POFF}$ must be connected together even those don't use their voltage converters.
91	LOAD	I	Latch pulse of the 80-bit display data latch at segment function. Shift clock input of shift register at common function. Data is latched when LOAD="H"
92,93	MODE, COM/SEG	I	- MODE="H": Mixed common and segment functions - MODE="L": Either common or segment function is selected

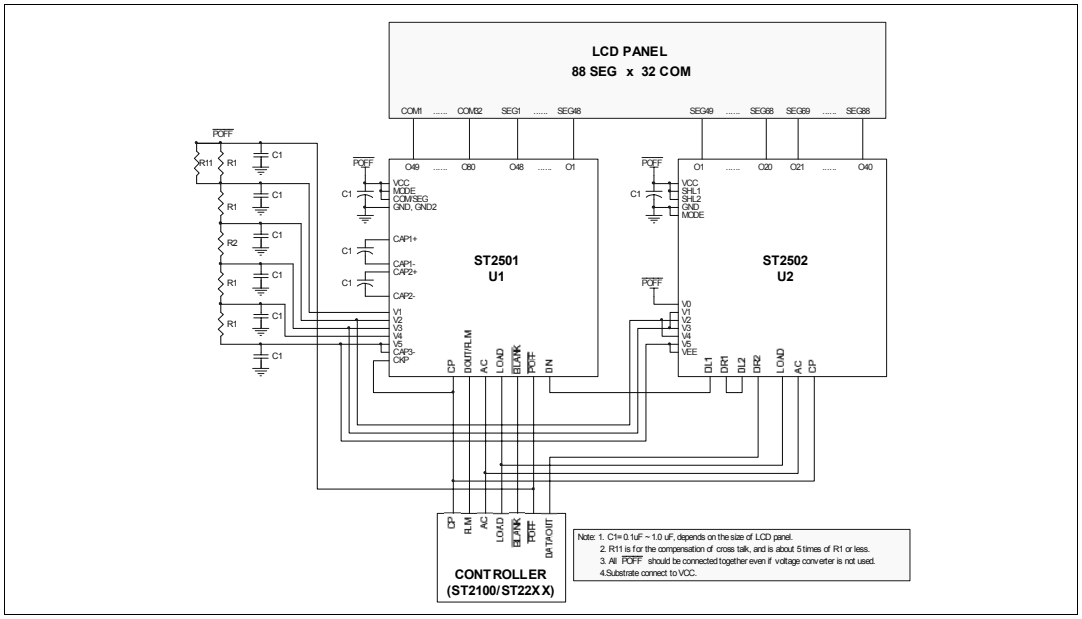
		COM/SEG	
		L	H
MODE	L	80 segments	80 commons
	H	32 seg / 48 com	48 seg / 32 com

94	V_{DD}	P	Power supply for logic and voltage converter circuit
42,89	GND, GND2	P	Ground
95	CAP1+	O	Connect to booster capacitor 1 positive(+) terminal
96	CAP1-	O	Connect to booster capacitor 1 negative(-) terminal
98	CAP2+	O	Connect to booster capacitor 2 positive(+) terminal
99	CAP2-	O	Connect to booster capacitor 2 negative(-) terminal
97	V5	O	Negative voltage output of booster circuit Power supply for LCD drives
100	CAP3-	O	Connect to booster capacitor 3 negative(-) terminal
101~104	V1~V4	I	Inputs of external power supply for LCD drives

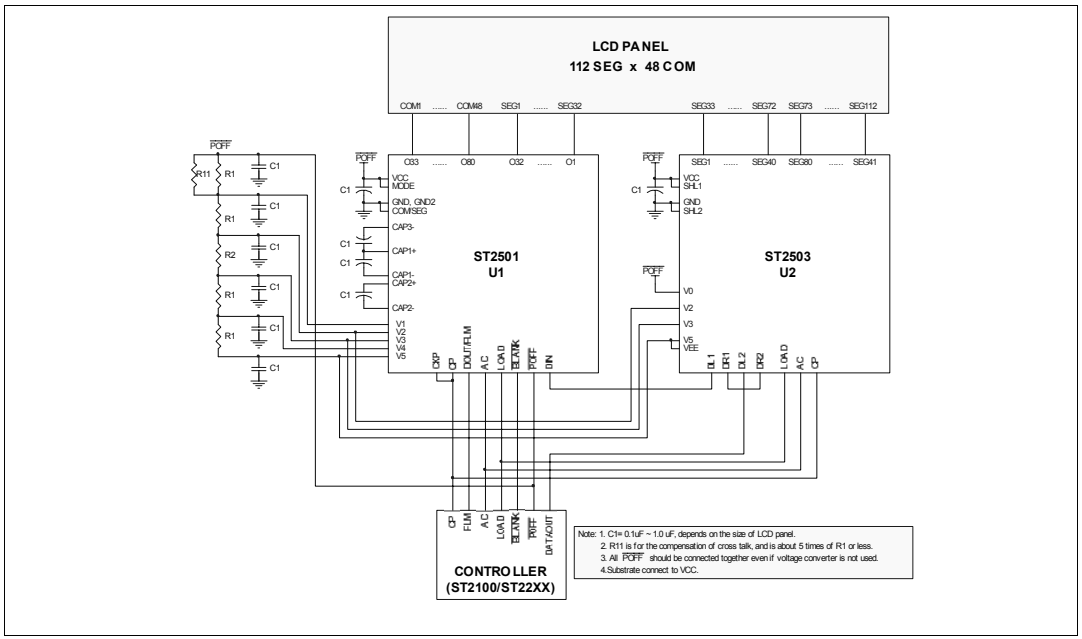
Note: P=power pin, I=input pin, O=output pin

5. Application Circuits

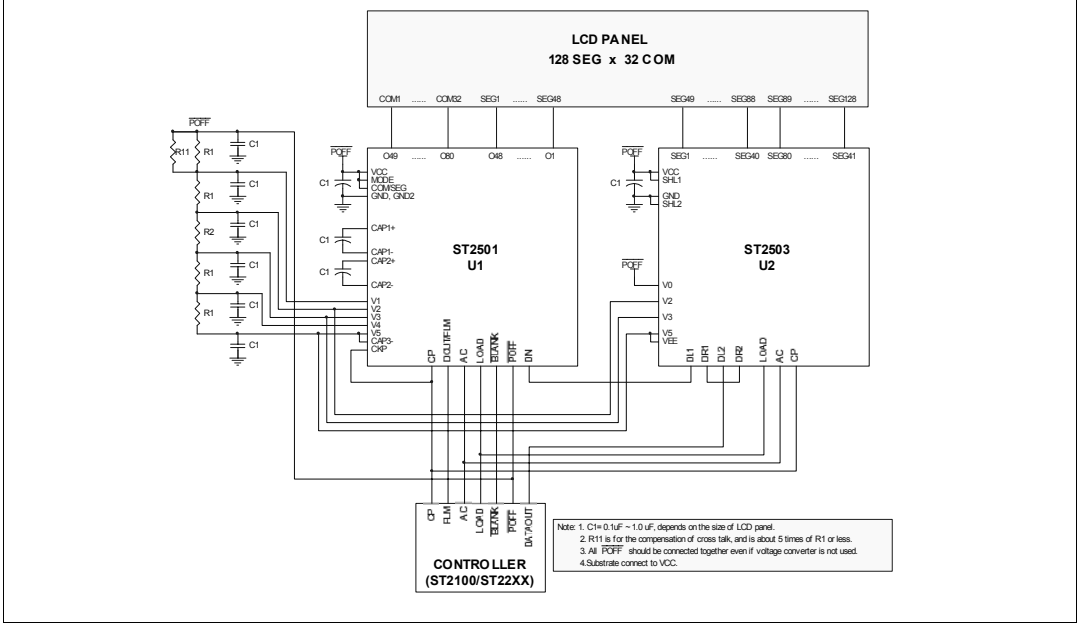
5.1 1/32 duty, 88 segments, 3X set-up



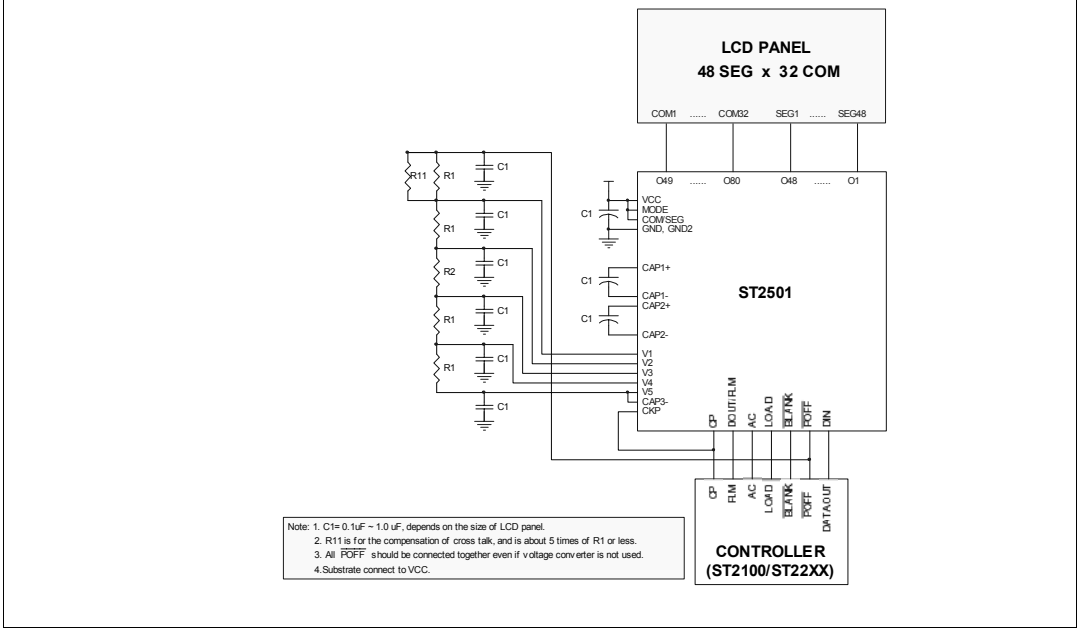
5.2 1/48 duty, 112 segments, 4X set-up



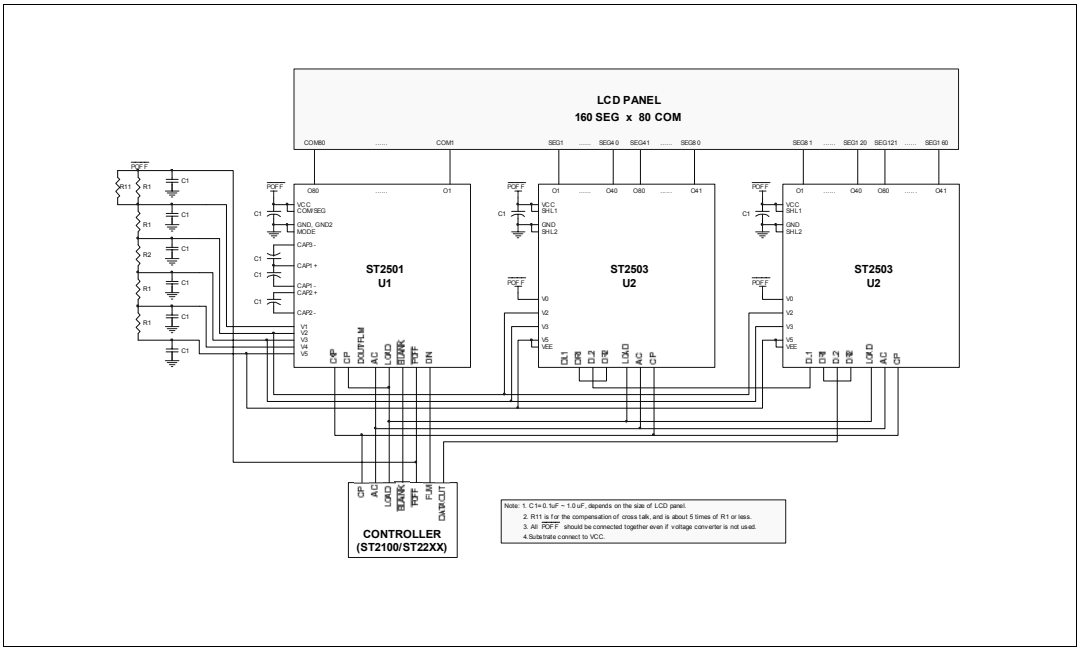
5.3 1/32 duty, 128 segments, 3X set-up



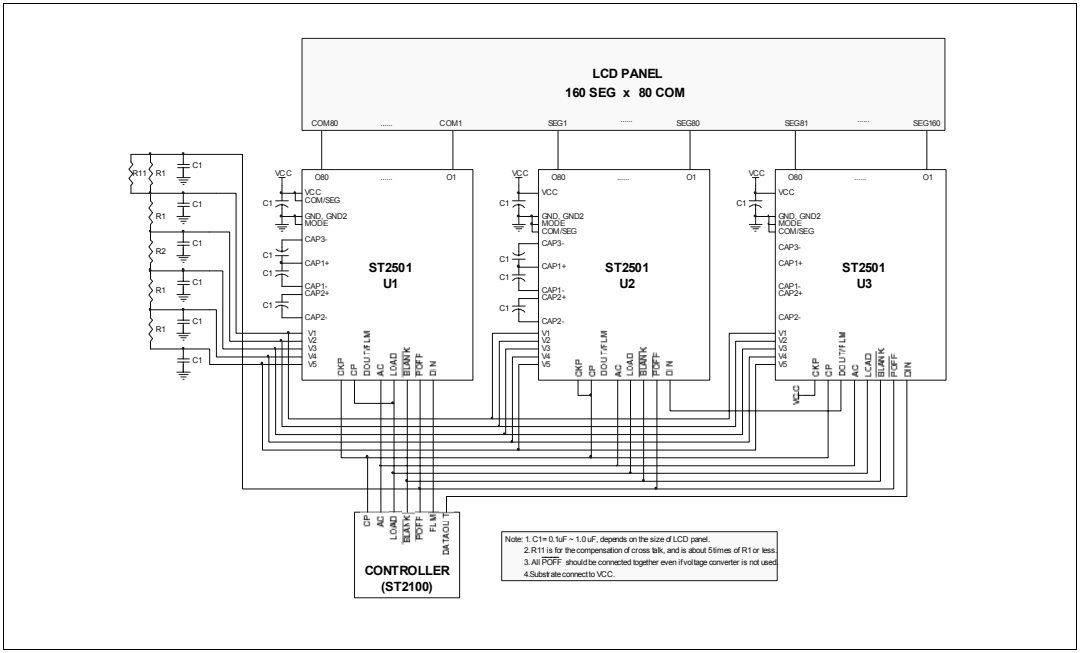
5.4 1/32 duty, 48 segments, 3X set-up



5.5 1/80 duty, 160 segments, 4X set-up (ST2501+ST2503x2)



5.6 1/80 duty, 160 segments, 4X set-up (ST2501x3)



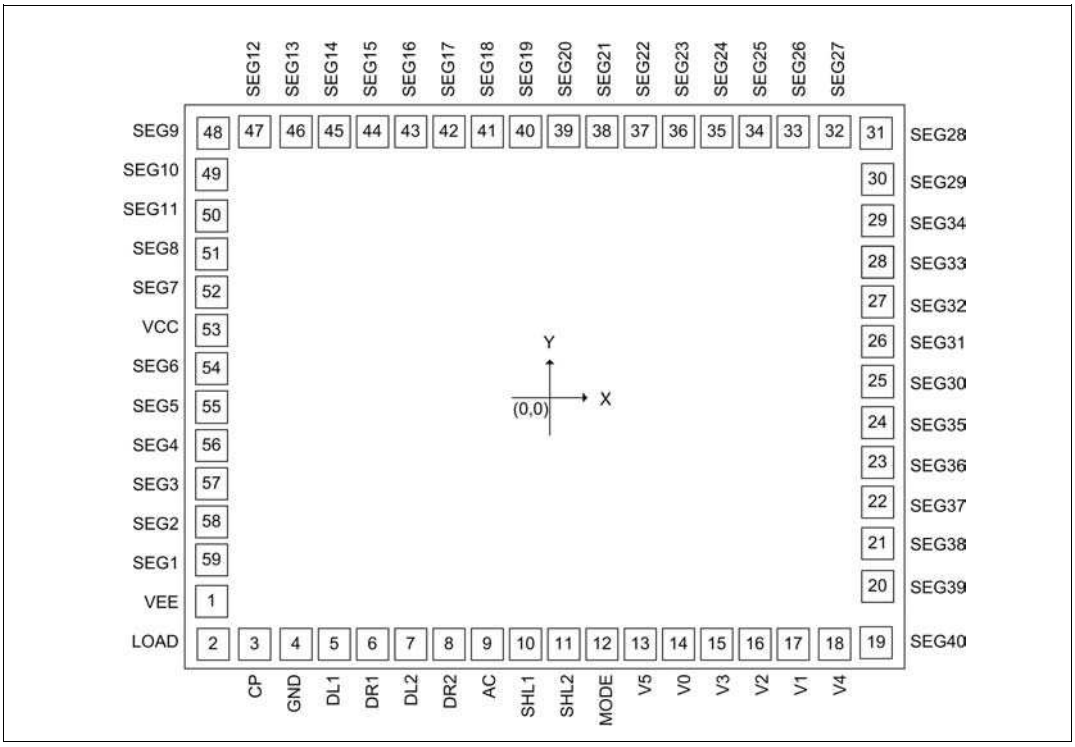
1. Features

- Number of LCD segment drives: 40 (20x2)
- Supply voltage for LCD drive: 12.0 V Max.
- Supply voltage for the logic system: +2.4 to +5.5 V
- Low power consumption
- Low output impedance
- 1-bit serial data input
- Interface with ST2100/ST22XX LCD controller
- Support cascade function to drive large size and high resolution panels
- Shift to left or right options for different glass layout

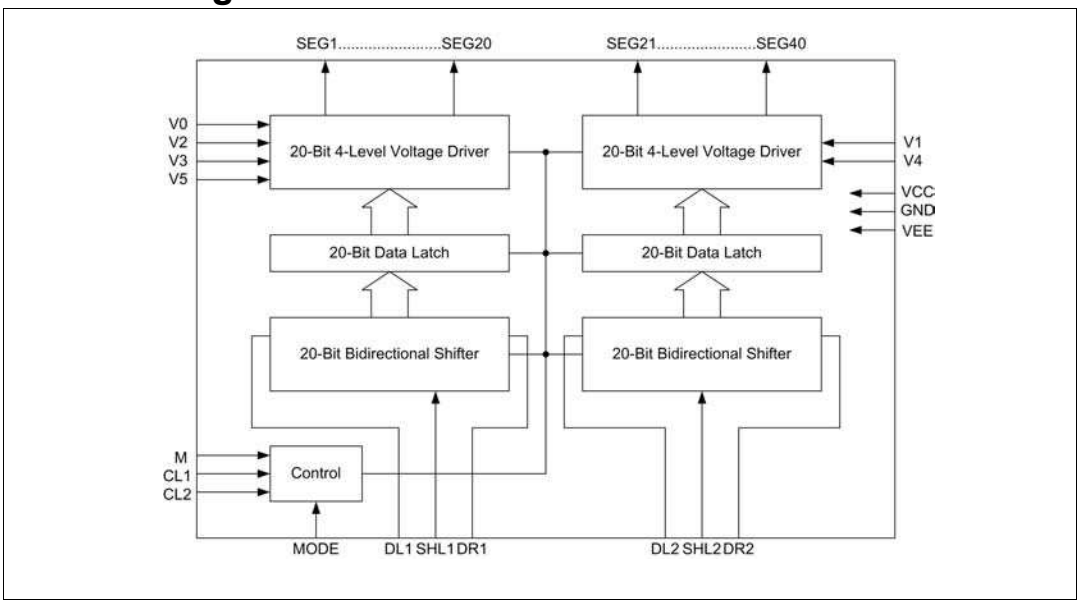
2. General Description

The ST2502 is a dot matrix segment LCD driver LSI that is fabricated by advanced low power CMOS silicon gate technology. It is suitable for driving various small/medium scale and different display resolution LCD panels, and is useful for personal equipments or other consumer applications. This chip consists of two 20-bit shift register, data latch, and 4-level driver. It converts serial data, which is received from LCD controller (ex: ST2100/ST22XX) to parallel data and outputs LCD driving waveform to the LCD panel. This LSI can drive a variety of LCD panels because of the cascade capability, and also the flexibility of bias voltages which are provided externally.

3. Pad Diagram



3. Block Diagram



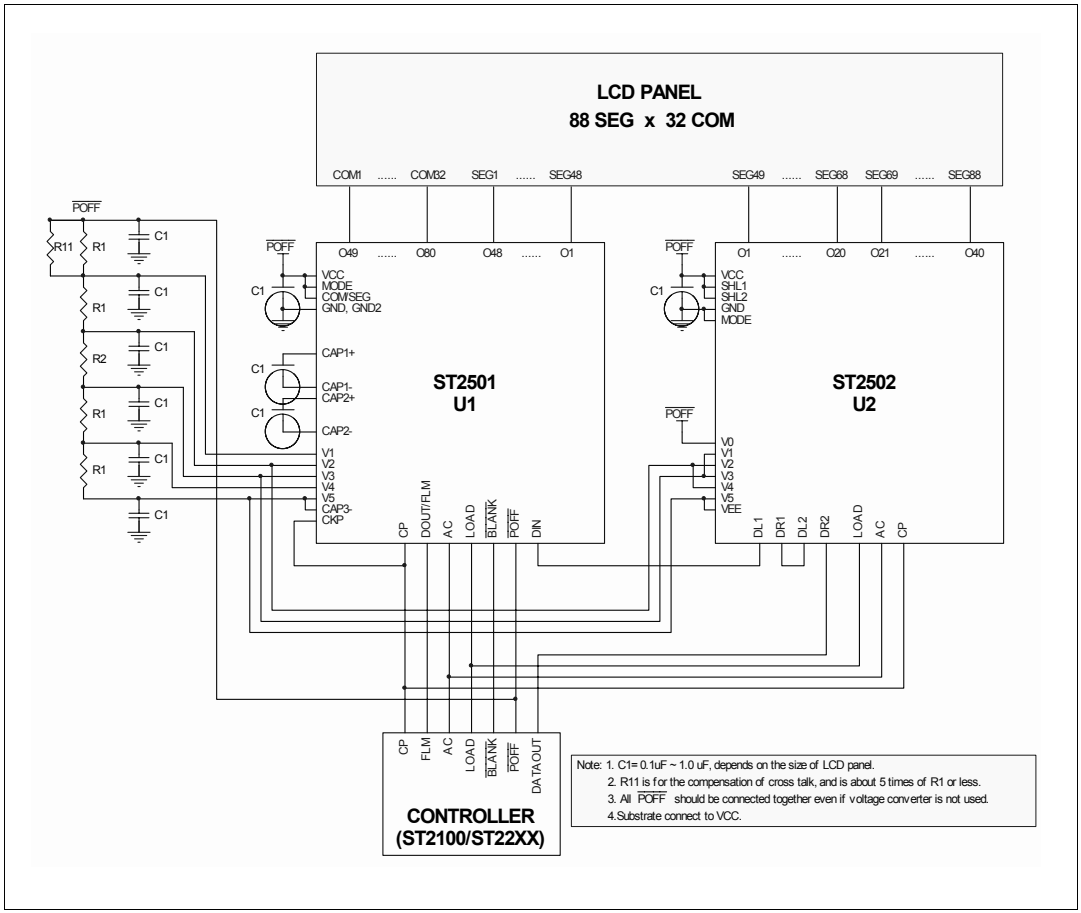
4. Pad Description

Pin Number	Designation	I/O	Description
1	VEE	I	Power supply for LCD drives
2	LOAD	I	Latch pulse of two 40-bit display data latch.
3	CP	I	Clock pulse input pin for two 40-bit shift registers. Data is shifted at falling edge of clock. Connect to LCD pixel clock for LCD segment data
4	GND	P	Ground
5,6	DL1,DR1	I/O	If SHL1=0 data is inputted from DL1 and then outputted to DR1 If SHL1=1 data is inputted from DR1 and then outputted to DL1
7,8	DL2,DR2	I/O	If SHL2=0 data is inputted from DL2 and then outputted to DR2 If SHL2=1 data is inputted from DR2 and then outputted to DL2
9	AC	I	Alternating signal input for LCD drive waveform
10	SHL1	I	Direction control of first 20-bit shift register
11	SHL2	I	Direction control of second 20-bit shift register
12	MODE	I	Connect to GND for normal operation
13~18	V5,V0,V3, V2,V1,V4	I	Inputs for external power supply for LCD drives
19~52,54~59	SEG1~SEG40	O	LCD segment drives
53	VCC	P	Power supply for logic circuit

Note: P=power pin, I=input pin, O=output pin

5. Application Circuits

5.1 32 duty, 88 segments, 3X set-up



LCD Driver Product Line

Character LCD Controller / Drivers

Graphic LCD Drivers

Single Chip LCD Controller / Drivers

Character LCD Controller/ Drivers Series

Part No.	#COMx #SEG	VDD	VLCD	Booster Bias	I/O	Package	REMARK
ST7066U	16CX40S	2.7~5.5	3~10	X	4 OR 8bit PARAELL	Bare chip	Max display : 80x1 or 40x2 5x8 dot chars (with additional drivers)
ST7065C	40CH DRIVER	2.7~5.5	3~11	X	---	Bare chip	
ST7063C	80SCH DRIVER	2.7~5.5	3~11	X	---	Bare chip	
ST7070	16Cx80S (496 char built-in)	2.7~5.5	3~7	X	4 OR 8bit PARAELL 3/4 SPI	Bare chip	
ST7032 ST7032i	16CX80S +80 icons	2.7~5.5	2.7~7	2X Ext 2C	4/8 bit P serial I2C	Gold bump	Max display : 16x2 5x8 dot chars
ST7036 ST7036i	16CX100S 24CX80S +80 icons	2.7~5.5	2.7~7	2X Ext 2C	4/8bit P serial I2C	Gold bump	Max display : 20x2 or 16x3 5x8 dot chars
ST7920	33Cx64S	2.7~5.5	3~7	2X EXT 2C	4/8 bit or serial	Bare chip	Built-IN 8192 chinese font (16x16 dot) max display:16x2
ST7921	96S driver	2.7~5.5	3~7	x	---	Bare chip	

1. Features

- 5 x 8 and 5 x 11 dot matrix possible
- Low power operation support:
  - 2.7 to 5.5V
- Wide range of LCD driver power
  - 3.0 to 10V
- Correspond to high speed MPU bus interface
  - 2 MHz (when VCC = 5V)
- 4-bit or 8-bit MPU interface enabled
- 80 x 8-bit display RAM (80 characters max.)
- 13,200-bit character generator ROM for a total of 240 character fonts(5 x 8 dot or 5 x 11 dot)
- 64 x 8-bit character generator RAM
  - 8 character fonts (5 x 8 dot)
  - 4 character fonts (5 x 11 dot)
- 16-common x 40-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 x 8 dots with cursor
  - 1/11 for one line of 5 x 11 dots & cursor
  - 1/16 for two lines of 5 x 8 dots & cursor
- Wide range of instruction functions:
  Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780, KS0066 and SED1278
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption
- QFP80 and Bare Chip available

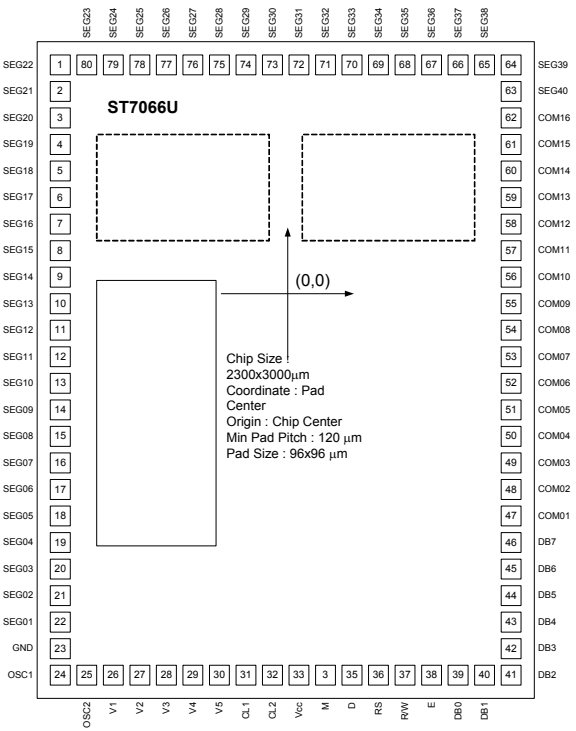
2.General Description

The ST7066U dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/ driver.

The ST7066U has pin function compatibility with the HD44780, KS0066 and SED1278 that allows the user to easily replace it with an ST7066U. The ST7066U character generator ROM is extended to generate 240 5x8(5x11) dot character fonts for a total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the ST7066U is suitable for any portable battery-driven product requiring low power dissipation.

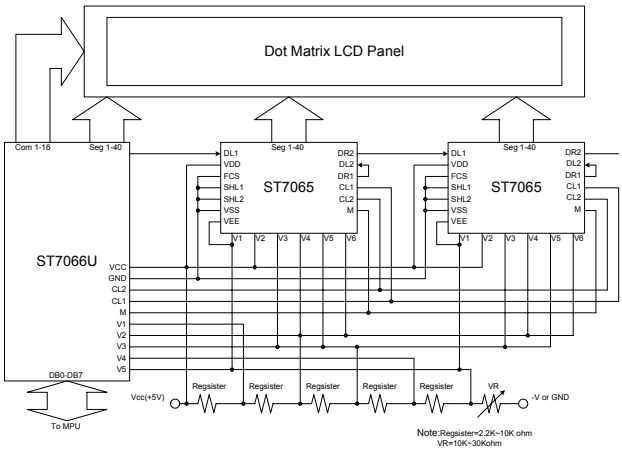
The ST7066U LCD driver consists of 16 common signal drivers and 40 segment signal drivers which can extend display size by cascading segment driver ST7065 or ST7063. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7066U can display up to one 8-character line or two 8-character lines

3. Pad Arrangement



Substrate Connect to V_{DD}.

4. Application Circuit

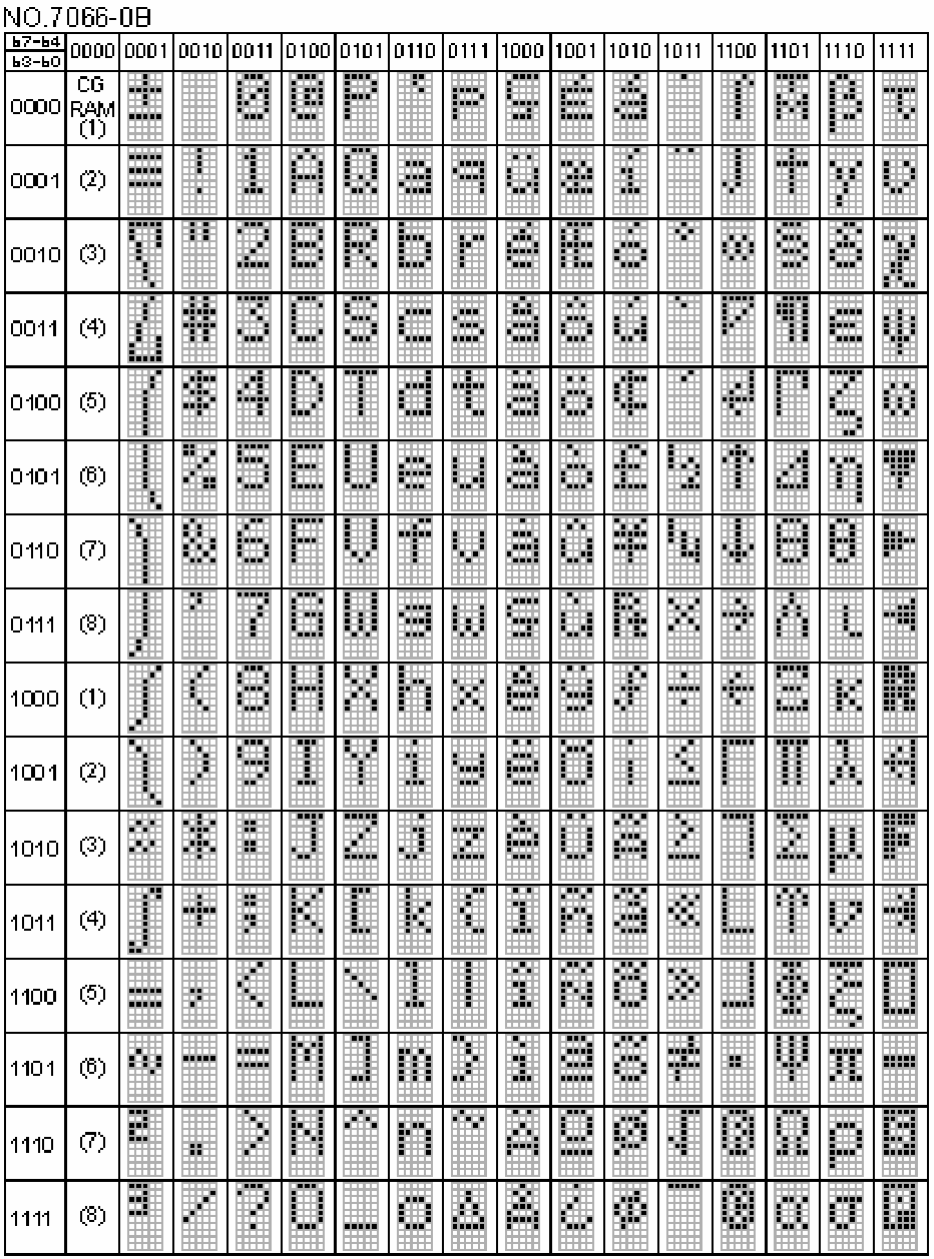


Correspondence between Character Codes and Character Patterns (ROM Code: 0A)

NO.7066-0A

Correspondence between Character Codes and Character Patterns (ROM Code: 0B)

NO.7066-0B

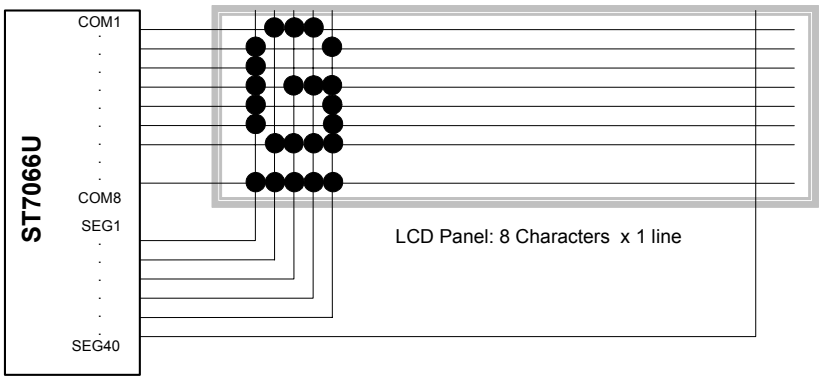


Correspondence between Character Codes and Character Patterns (ROM Code: 0E)

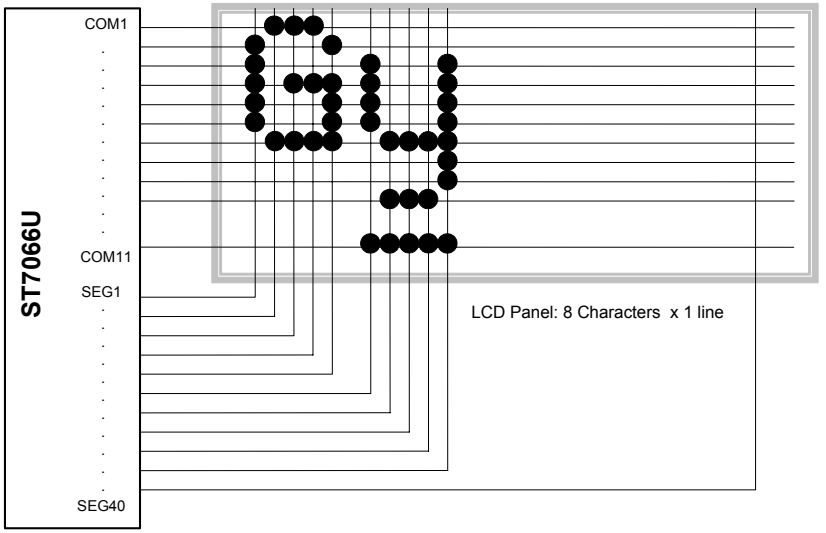
NO.7066-0E

5. LCD and ST7066U Connection

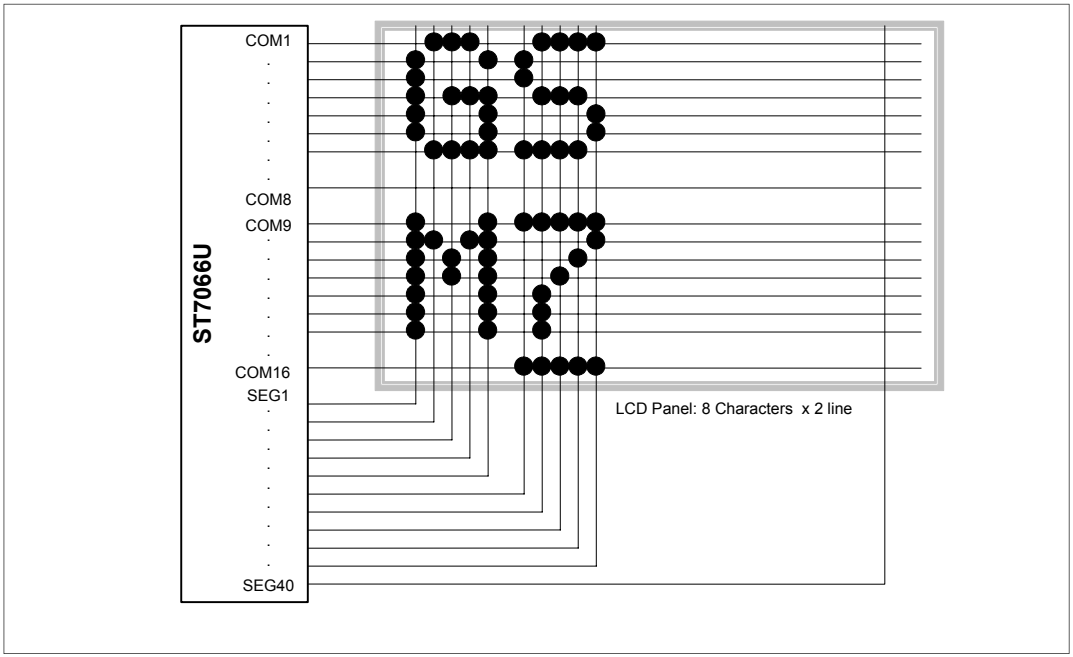
5.1 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



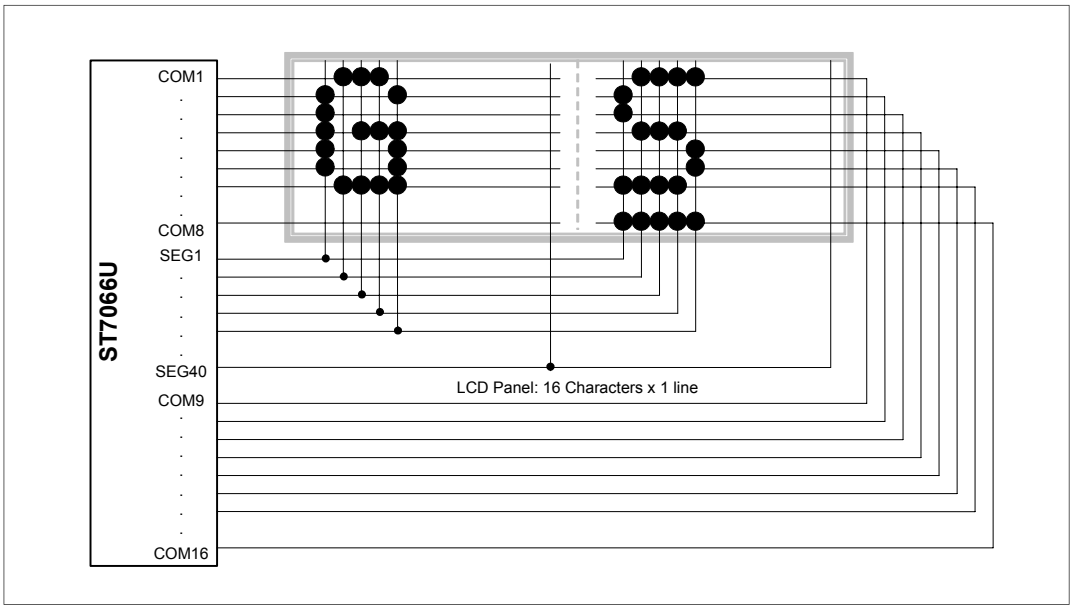
5.2 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



5.3 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



5.4 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



1. Function

- Dot matrix LCD driver with two 20 channel outputs
- Selectable function to use common/segment drivers simultaneously
- Bias voltage (V1 ~ V6)
- Input/output signals
  - nput : Serial display data and control pulse from controller IC
  - Output : 20 X 2 channels waveform for LCD driving

2. Feature

- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (VDD~VEE) : 3V ~ 11V
- 64 Pin QFP package and bare chip available

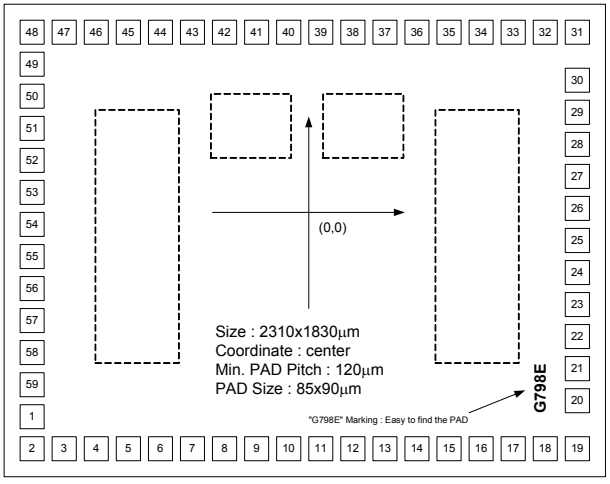
3.General Description

ST7065C is a segment/common driver for dot matrix type LCD display. It features 40 channels with 20 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

The ST7065C can convert serial data received from a LCD controller, such as ST7066U, into parallel data and send out LCD driving waveforms to the LCD panel. The ST7065C is designed for general-purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment/common driver.

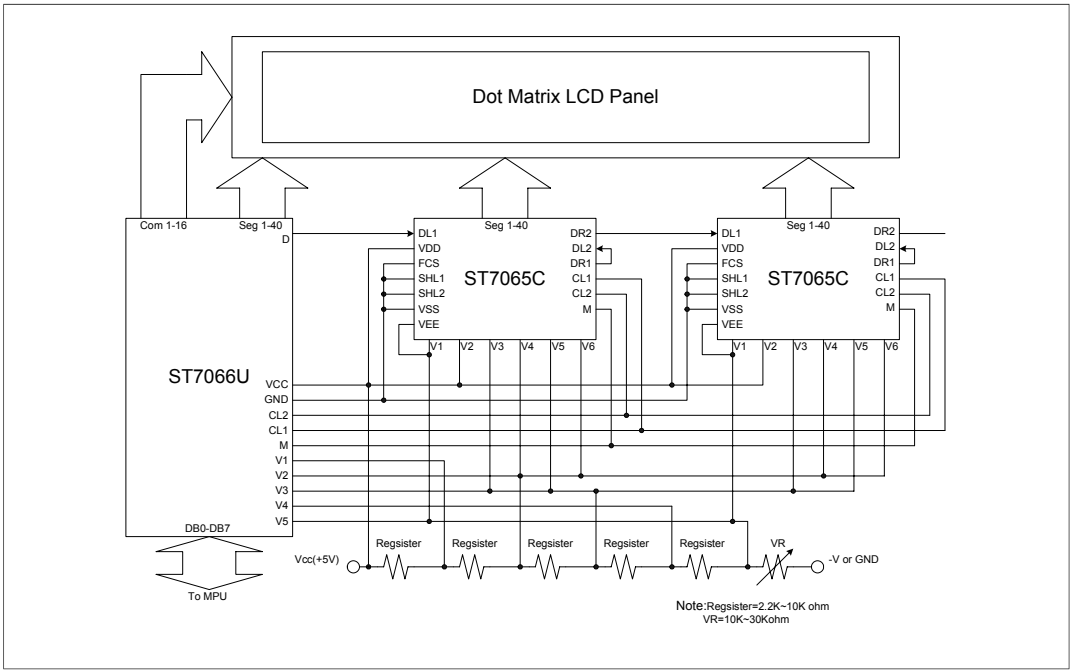
The ST7065C has pin function compatibility with the KS0065B that allows the user easily to replace it with a ST7065C.

4.Pad Arrangement



Substrate connect to VDD.

5. Application Circuit: (2Line x 24Word)



1. Function

- Dot matrix LCD driver with two 40 channel outputs
- Bias voltage (V1 ~ V4)
- input/output signals
  - Input : Serial display data and control pulse from controller IC
  - Output : 40 X 2 channels waveform for LCD driving

2. Feature

- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (VDD~VEE) : 3V ~ 11V

100 Pin QFP package and bare chip available

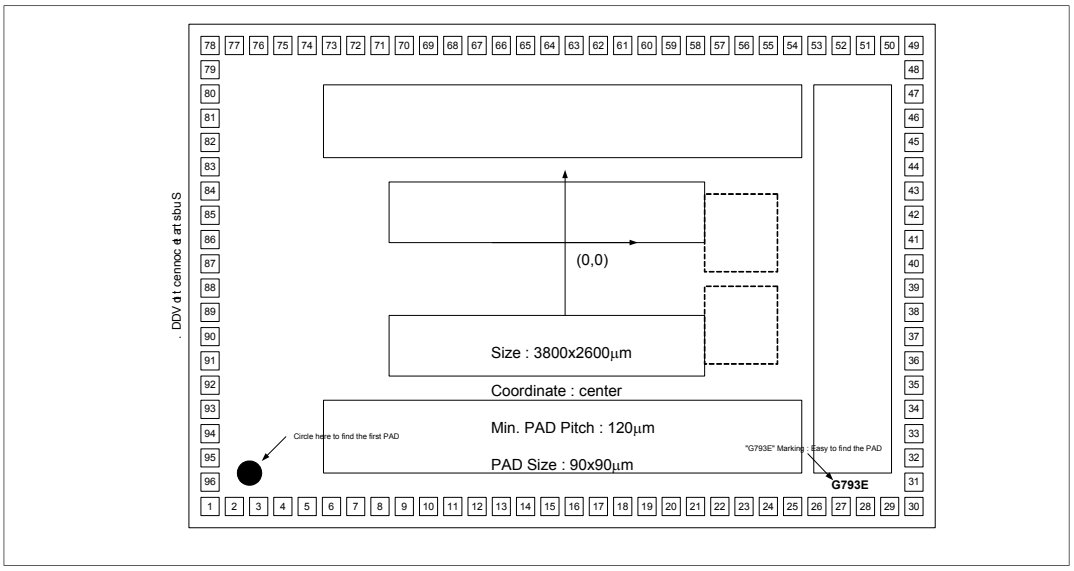
3. General Description

ST7063C is a segment driver for dot matrix type LCD display. It features 80 channels with 40 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

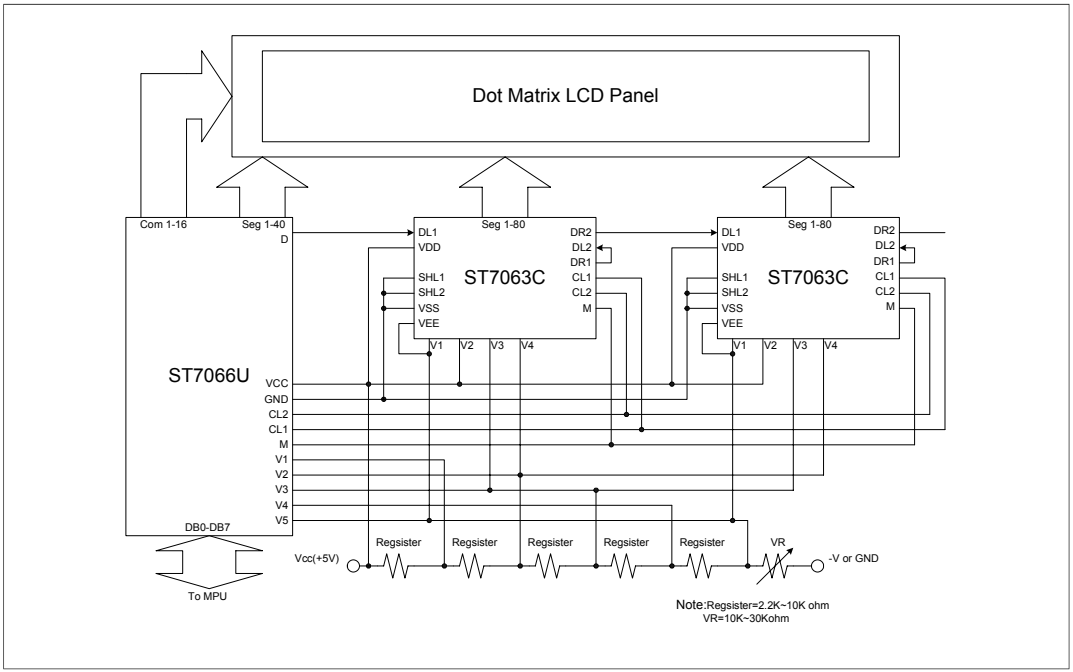
The ST7063C can convert serial data received from an LCD controller, such as ST7066U, into parallel data and send out LCD driving waveforms to the LCD panel. The ST7063C is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment driver.

The ST7063C has pin function compatibility with the KS0063(B) that allows the user to easily replace it with an ST7063C.

4.Pad Arrangement



5. Application Circuit : (2Line x 40Word)



1. Feature

- 5 x 8 dot matrix possible
- Low power operation support:
  - 2.7 to 5.5V
- Wide range of LCD driver power
  - 3.0 to 7.0V
- Support high speed serial interface
- Correspond to high speed MPU bus interface
  - 2 MHz (when VCC = 5V)
- 80 x 9-bit display RAM (80 characters max.)
- 19840-bit character generator ROM for a total of 496 character fonts(5 x 8 dot)
- 64 x 8-bit character generator RAM
  - 8 character fonts (5 x 8 dot)
- 16-common x 80-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 x 8 dots with cursor
  - 1/16 for two lines of 5 x 8 dots & cursor
- Wide range of instruction functions: Display clear, cursor home, display on/off, cursor on/off, cursor blink, cursor shift, display shift
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption
- Bare chip available

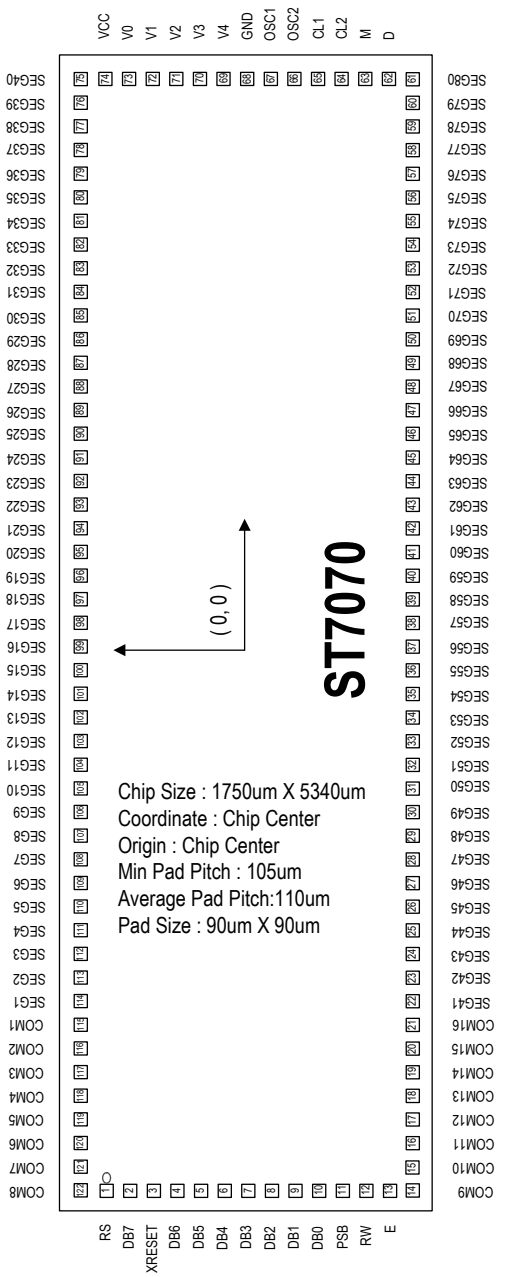
2. General Description

The ST7070 dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. With high speed serial interface(3-line SPI , 4-line SPI), the external MCU can control ST7070 directly. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/ driver.

The ST7070 has function partial compatibility with the HD44780, KS0066 and SED1278 that allows the user to easily replace it with an ST7070. The ST7070 character generator ROM is extended to generate 496 5x8 dot character fonts for a total of 496 different character fonts. The low power supply (2.7V to 5.5V) of the ST7070 is suitable for any portable battery-driven product requiring low power dissipation.

The ST7070 LCD driver consists of 16 common signal drivers and 80 segment signal drivers which can extend display size by cascading segment driver ST7921. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7070 can display

3. Pad Arrangement

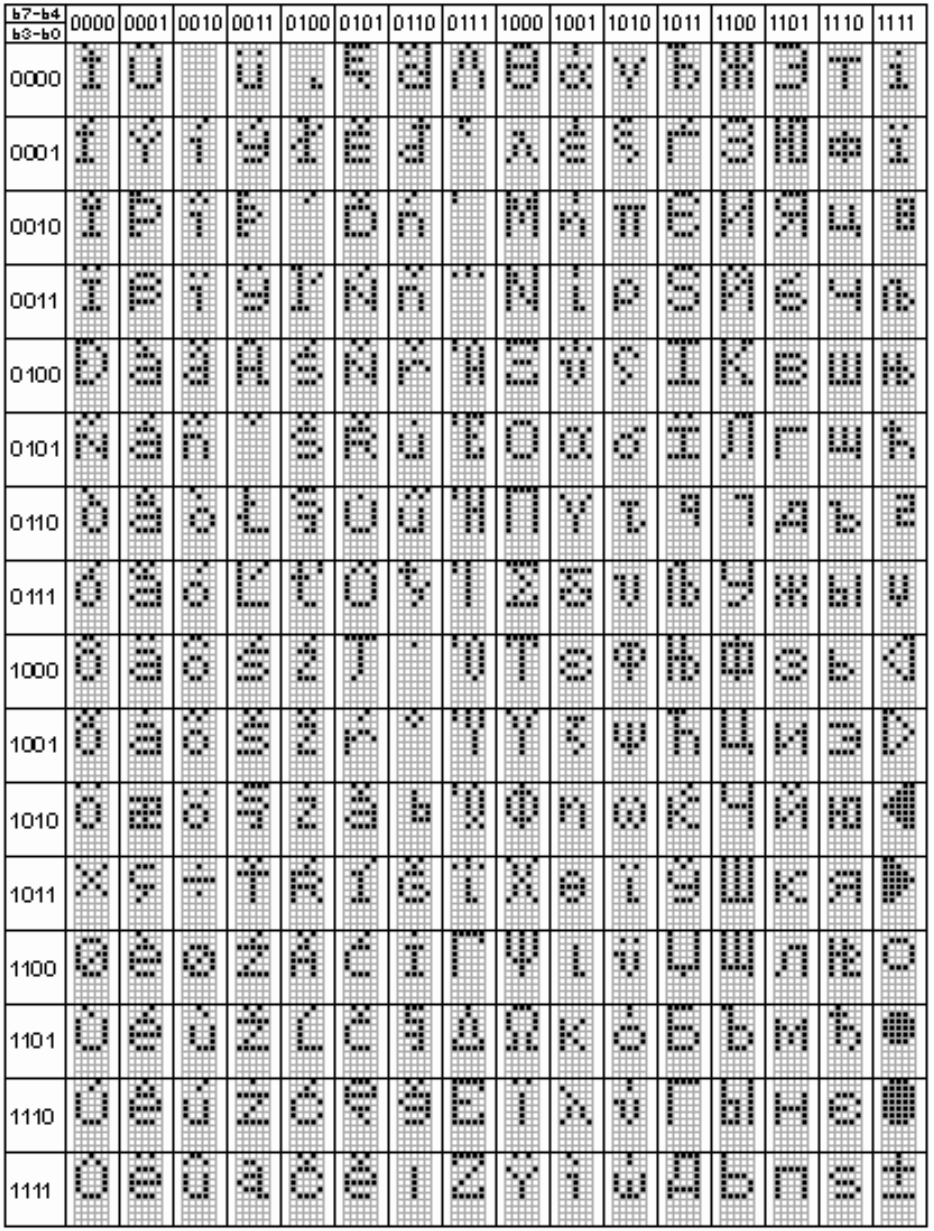


Correspondence between Character Codes and Character Patterns (ROM Code: 0B)

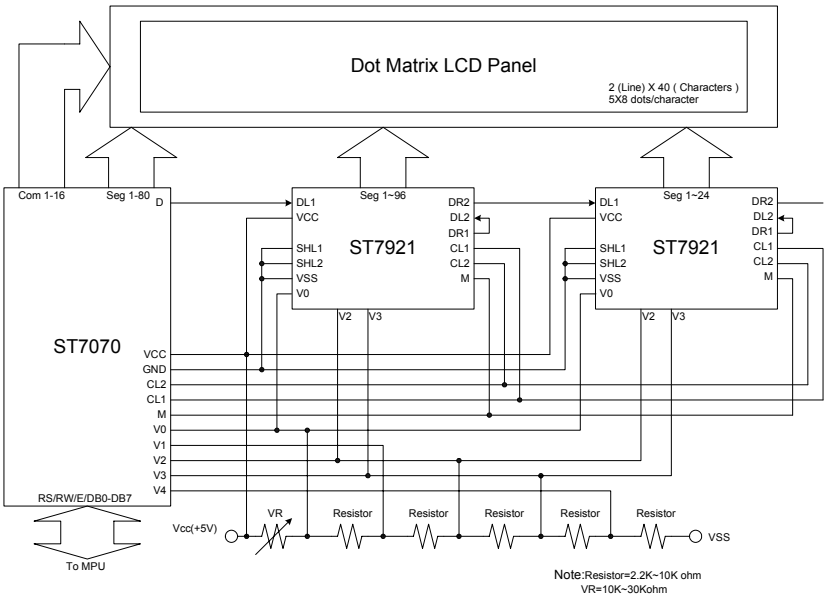
ST7070-0B-01

Correspondence between Character Codes and Character Patterns (ROM Code: 0B)

ST7070-0B-02

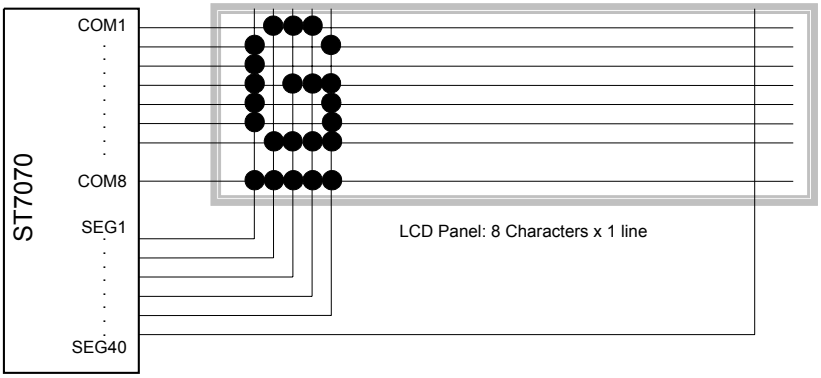


4. Application Circuit

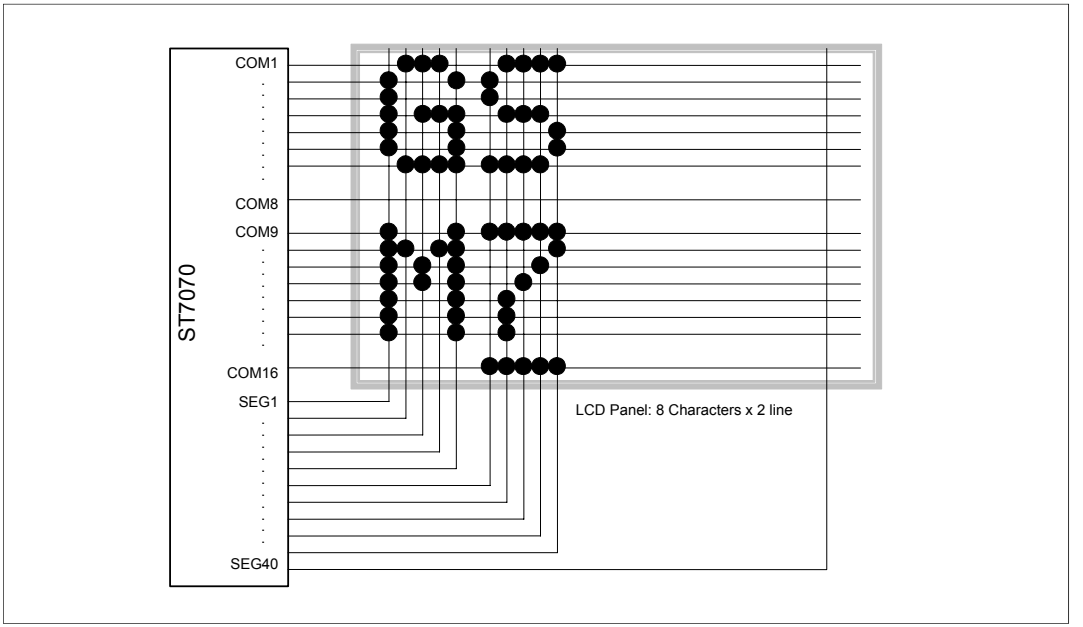


5.LCD and ST7070 Connection

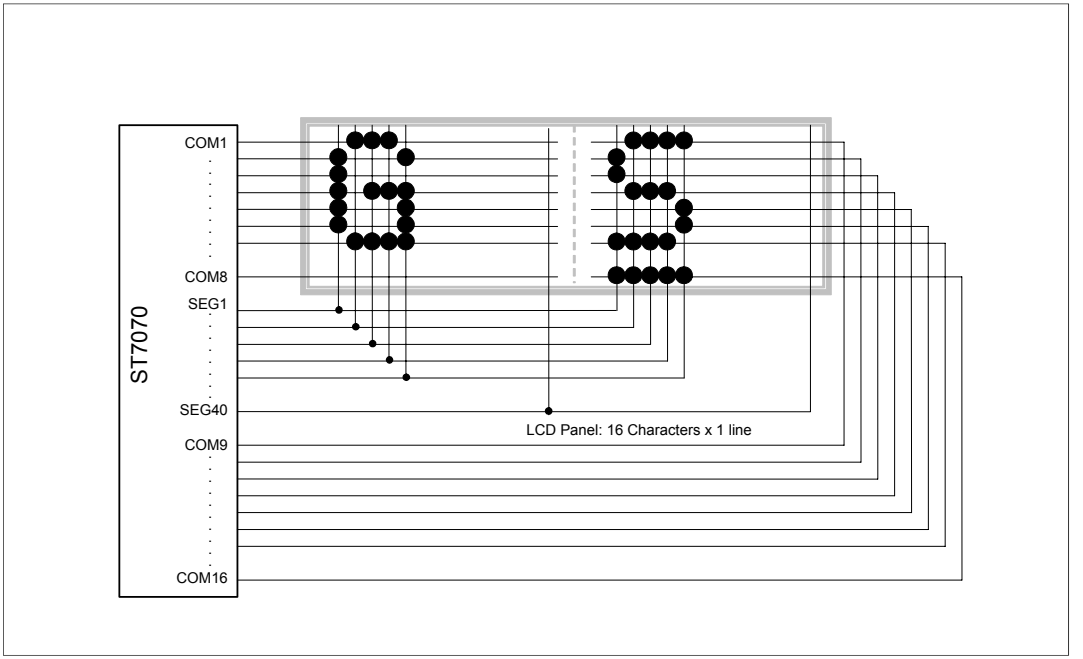
5.1 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



5.2 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



5.3 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)

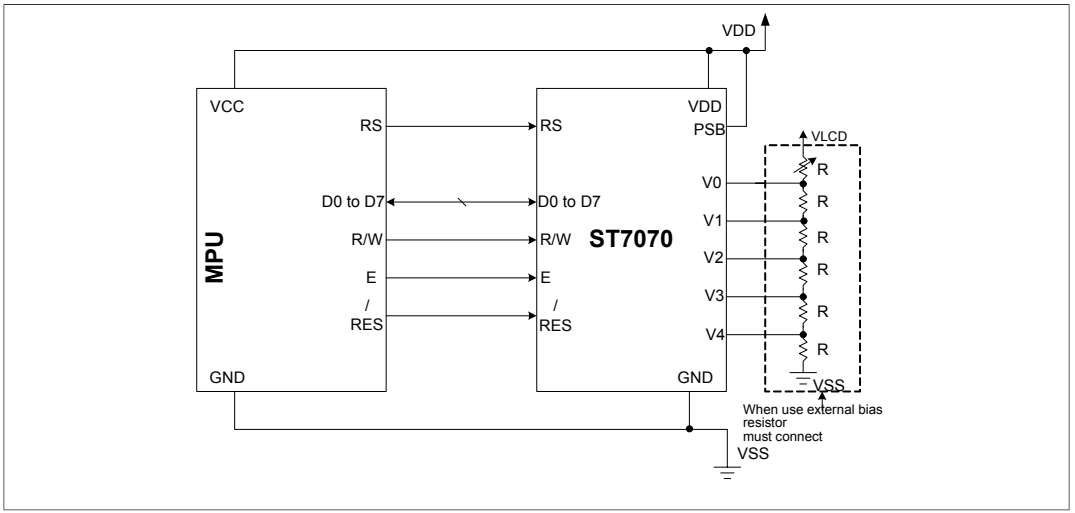


6. The MPU Interface

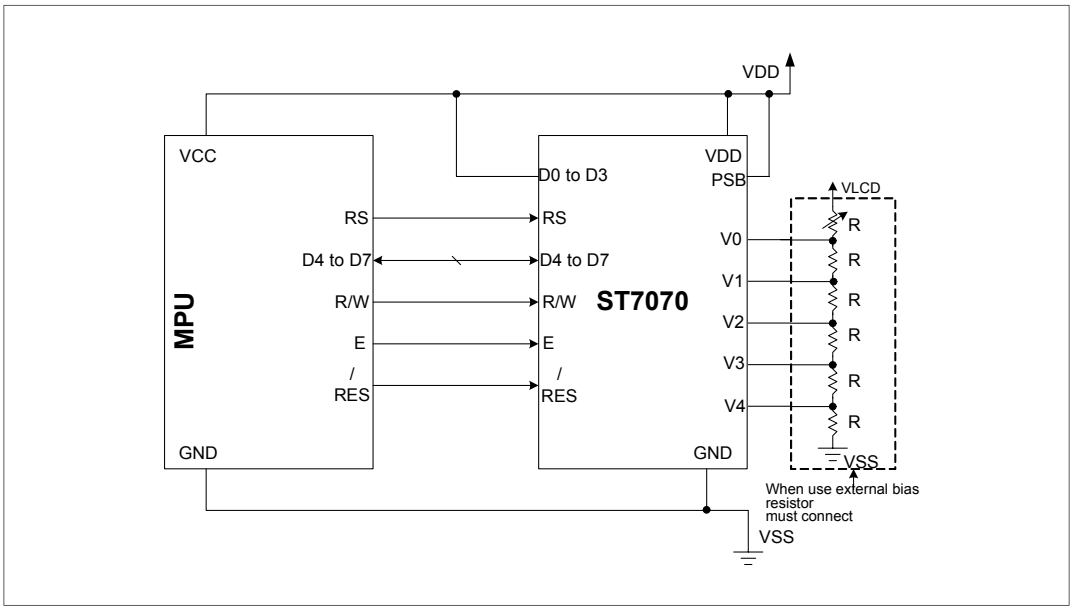
The ST7070 Series can be connected to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7070 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7070 Series chips . When this is done , the chip select signal can be used to select the individual Ics to access.

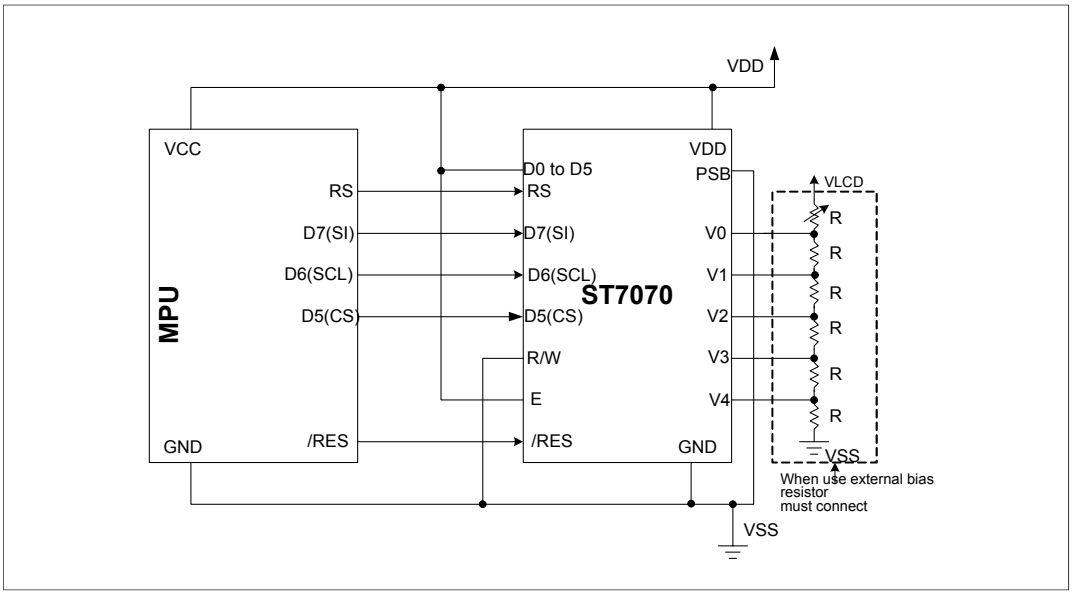
6.1 6800 8 bits Series MPUs



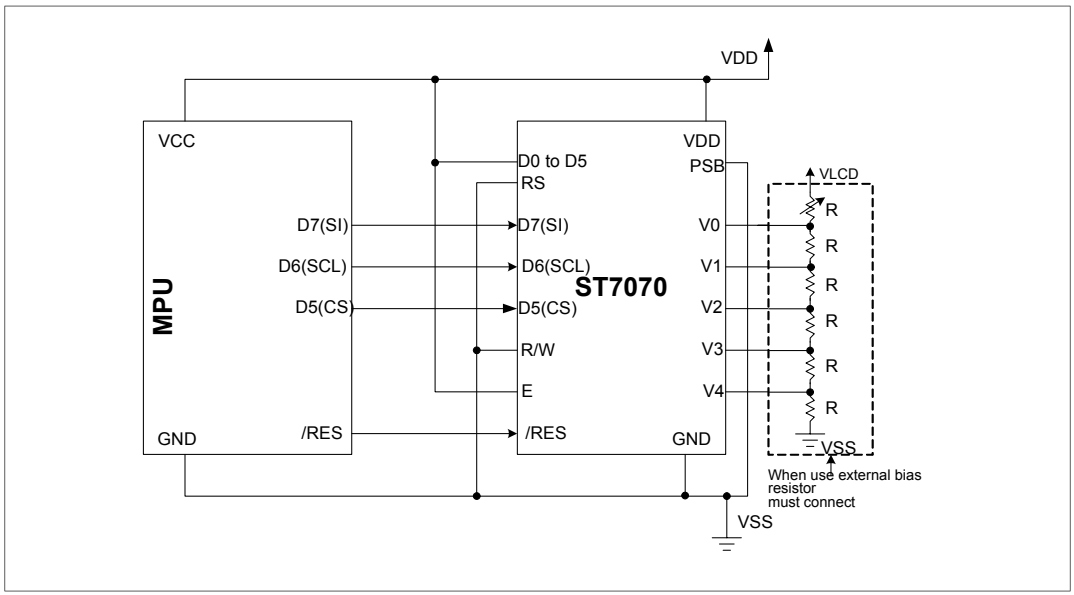
6.2 6800 4 bits Series MPUs



6.3 Using the Serial Interface-For 4 SPI



6.4 Using the Serial Interface-For 3 SPI



1. Features

- 5 x 8 dot matrix possible
- Low power operation support:
  - 2.7 to 5.5V
- Range of LCD driver power
  - 2.7 to 7.0V
- 4-bit or 8-bit or serial MPU interface enabled
- 80 x 8-bit display RAM (80 characters max.)
- 10,240-bit character generator ROM for a total of 256 character fonts (max)
- 64 x 8-bit character generator RAM (max)
- 16-common x 80-segment and 1-common x 80-segment ICON liquid crystal display driver
- 16 x 5 -bit ICON RAM (max)
- Programmable duty cycles
  - 1/8 or 1/9 for one line of 5 x 8 dots with cursor
  - 1/16 or 1/17 for two lines of 5 x 8 dots & cursor
- Wide range of instruction functions:
  Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift, double height font
- Automatic reset circuit that initializes the controller/driver after power on and external reset pin
- Internal oscillator (Frequency=540KHz) and external clock
- Built-in voltage booster and follower circuit (low power consumption)
- Com/Seg direction selectable
- Multi-selectable for CGRAM/CGROM size
- Instruction compatible to ST7066U and KS0066U and HD44780
- I2C Bus Available(ST7032i)
- Gold-bumped chip available

2. General Description

The ST7032 dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4-/ 8-bit or serial interface microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

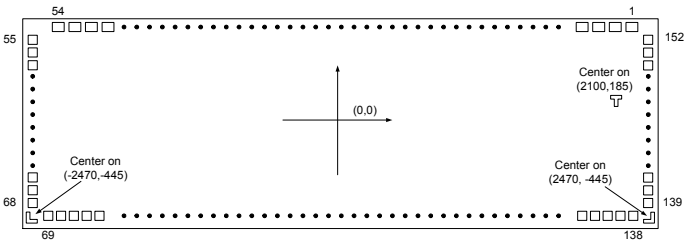
The ST7032 character generator ROM is extended to generate 256 5x8dot character fonts for a total of 256 different character fonts. The low power supply (2.7V to 5.5V) of the ST7032 is suitable for any portable battery-driven product requiring low power dissipation.

The ST7032 LCD driver consists of 17 common signal drivers and 80 segment signal drivers. The maximum display RAM size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7032 can display up to one 16-character line or two 16-character lines.

No extra drivers can be cascaded .

3. Pad Arrangement

Chip Size: 5130.0 x 1080.0μm
- Bump Pitch : 62μm (min)
- Bump Size :
  Pad No.1~54 : 54 x 97μm
  Pad No.55~152 : 40 x 97μm



4. LCD and ST7032 Connection

SHLC/SHLS ITO option pin can select at different direction for LCD panel

■ Com normal direction/Seg normal direction

2Line x 16 Characters,SHLC=1,SHLS=1

■ Com normal direction/Seg reverse direction

2Line x 16 Characters,SHLC=1,SHLS=0

■ Com reverse direction/Seg normal direction

2Line x 16Characters,SHLC=0,SHLS=1

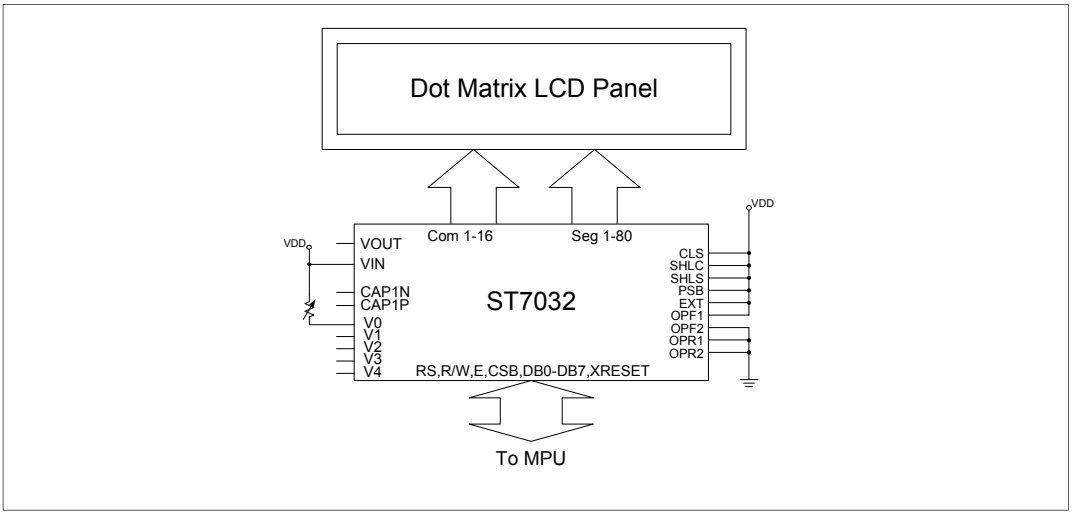
■ Com reverse direction/Seg reverse direction

2Line x 16Characters,SHLC=0,SHLS=0

5. Application Circuit

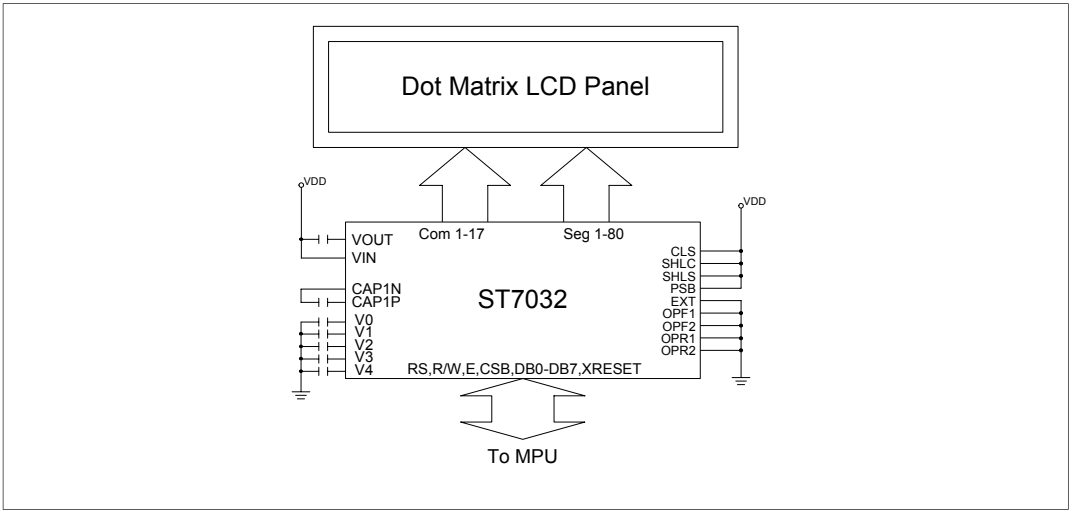
ST7066U normal mode

- Use internal resistor(9.6K ohm) and contrast adjust with external VR.
- Booster always off.
- Has 240 character of CGROM and 8 characters of CGRAM
- Internal oscillator.



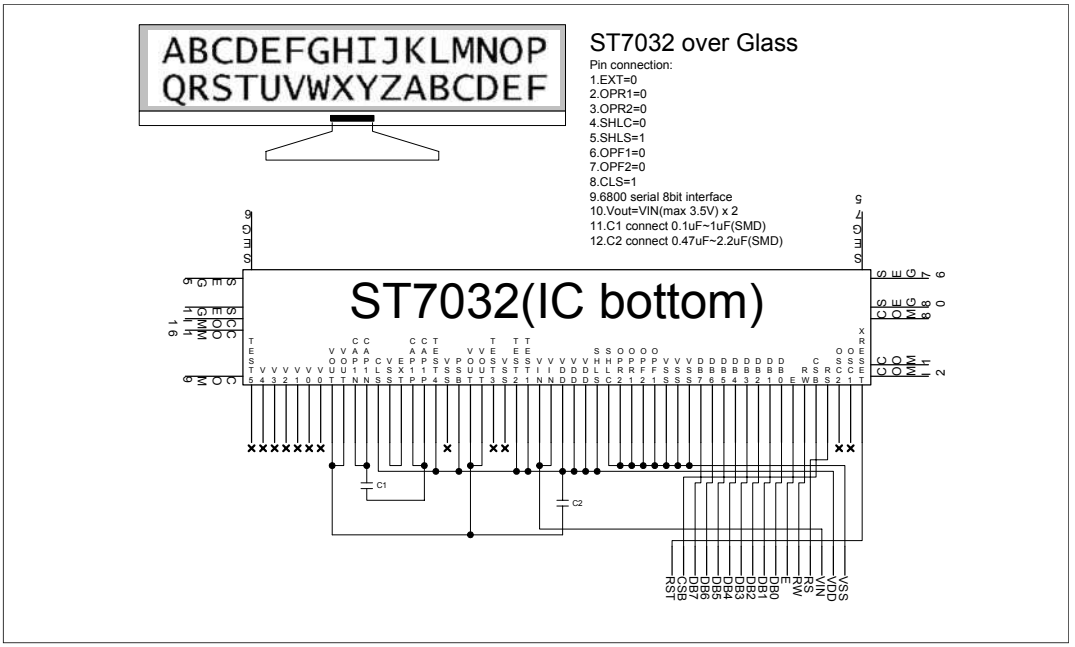
Extension mode

- Use internal follower circuit.
- Booster has 2 times pump.
- Has 240 character of CGROM and 8 characters of CGRAM
- Internal oscillator

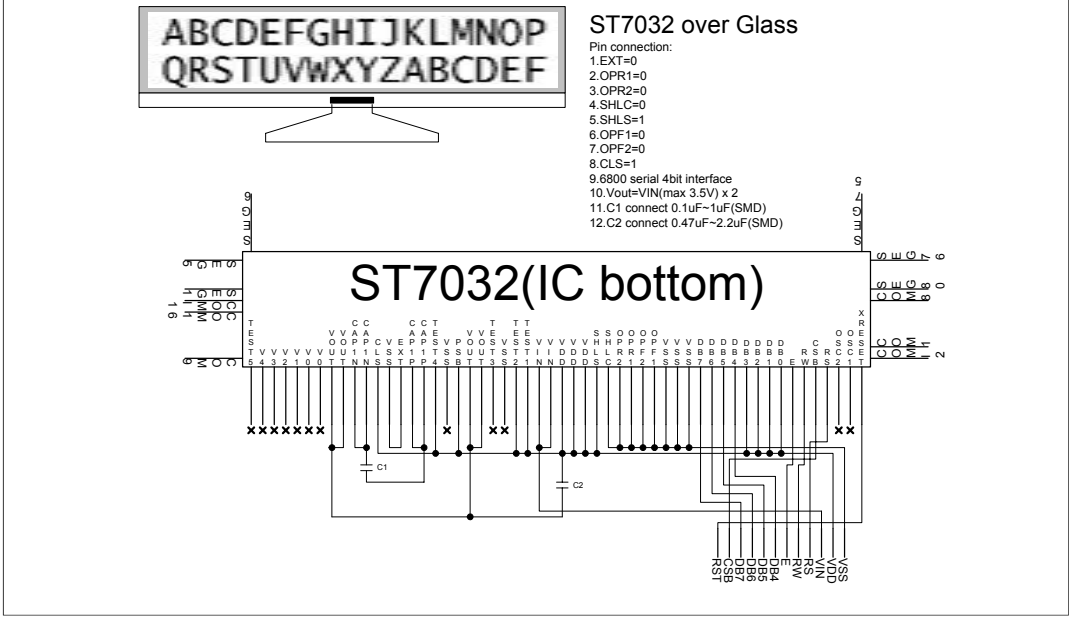


for glass layout

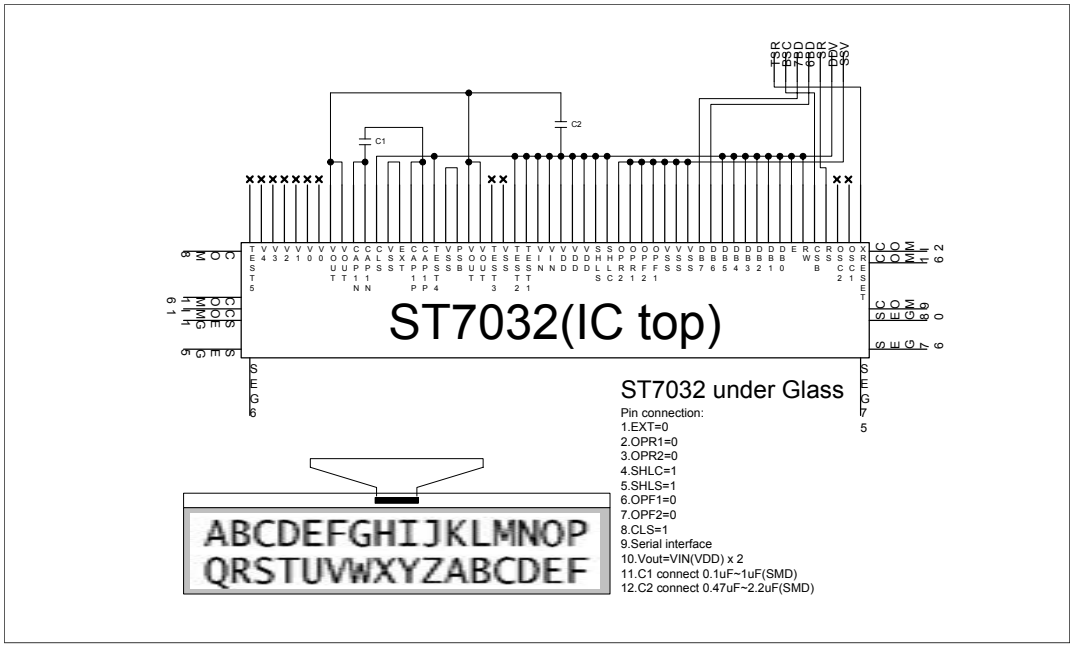
■ ST7032 over Glass,6800 serial 8bit interface, with booster and follower circuit on.



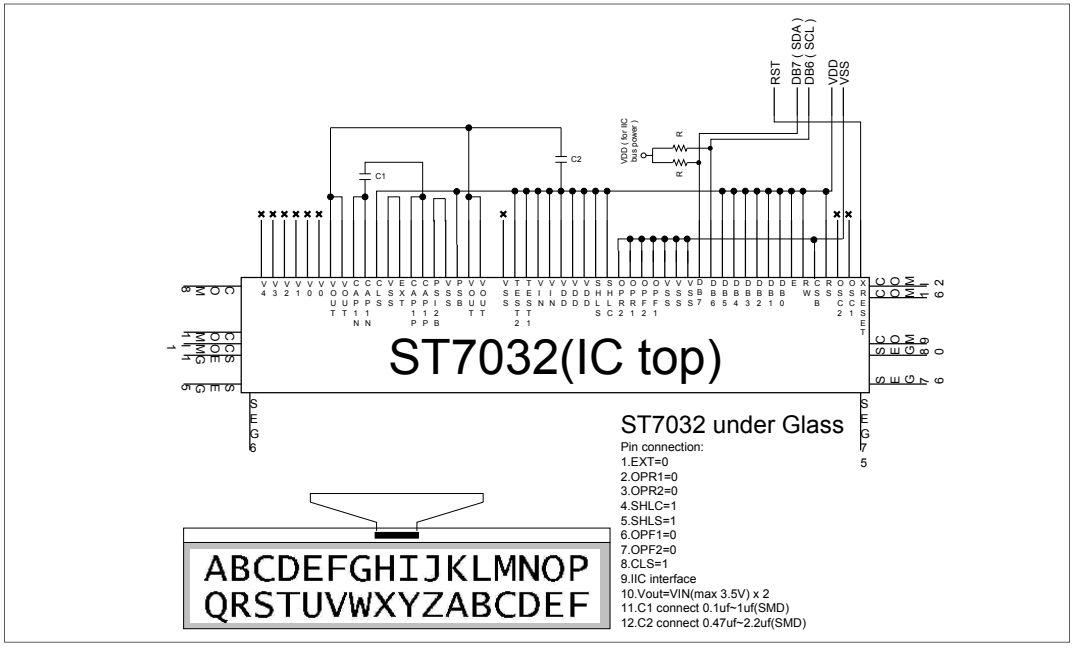
■ ST7032 over Glass,6800 serial 4bit interface, with booster and follower circuit on



■ ST7032 under Glass, serial interface, with booster and follower circuit on



■ ST7032i under Glass, IIC interface, with booster and follower circuit on



1. Features

- 5 x 8 dot matrix possible
- Low power operation support:
  - 2.7 to 5.5V
- Range of LCD driver power
  - 2.7 to 7.0V
- 4-bit or 8-bit or serial MPU interface enabled
- 80 x 8-bit display RAM (80 characters max.)
- 10,240-bit character generator ROM for a total of 256 character fonts(max)
- 64 x 8-bit character generator RAM(max)
- Support two display mode:
  - 16-com x 100-seg and 80 ICON
  - 24-com x 80-seg and 80 ICON
- 16 x 5 -bit ICON RAM(max)
- Programmable duty cycles
  - 1/8 or 1/9 for one line of 5 x 8 dots with cursor
  - 1/16 or 1/17 for two lines of 5 x 8 dots & cursor
  - 1/25 for three lines of 5 x 8 dots & cursor
- Wide range of instruction functions:
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift, double height font
- Automatic reset circuit that initializes the controller/driver after power on and external reset pin
- Internal oscillator(Frequency=540KHz) and external clock
- Built-in voltage booster and follower circuit (low power consumption)
- Com/Seg direction selectable
- Multi-selectable for CGRAM/CGROM size
- Instruction compatible to ST7066U and KS0066U and HD44780
- I2C Bus Available(ST7036i)
- Gold bumped chip available

2. General Description

The ST7036 dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4-/ 8-bit or serial interface microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

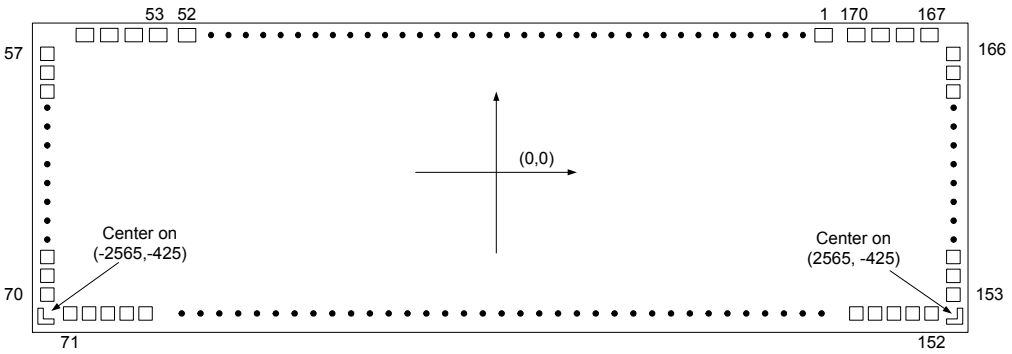
The ST7036 character generator ROM is extended to generate 256 5x8dot character fonts for a total of 256 different character fonts. The low power supply (2.7V to 5.5V) of the ST7036 is suitable for any portable battery-driven product requiring low power dissipation.

The ST7036 LCD driver consists of 17 common signal drivers and 100 segment signal drivers. And the second mode is consists of 25 common signal and 80 segment signal drivers. The maximum display RAM size can be either 80 characters in 1-line display or 40 characters in 2-line display or 16 characters in 3-line. A single ST7036 can display up to one 20-character line or two 20-character lines or three 16-character lines.

No extra drivers can be cascaded.

3. Pad Arrangement

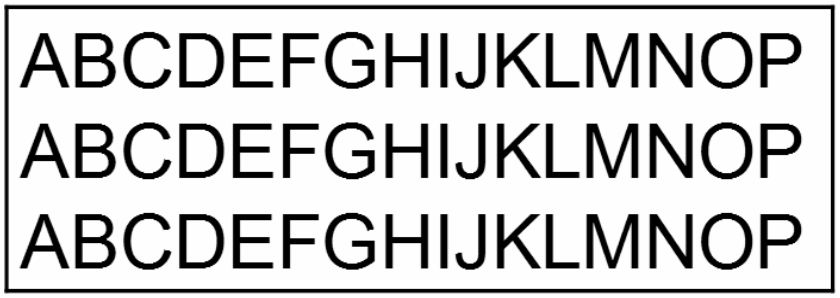
- Chip Size: 5150.0 x 870.0μm
- Bump Pitch : 55μm(min)
- Bump Size :
  - Pad No.1~52 : 56 x 72μm
  - Pad No.53~170 : 35 x 101μm



4. LCD and ST7036 Connection

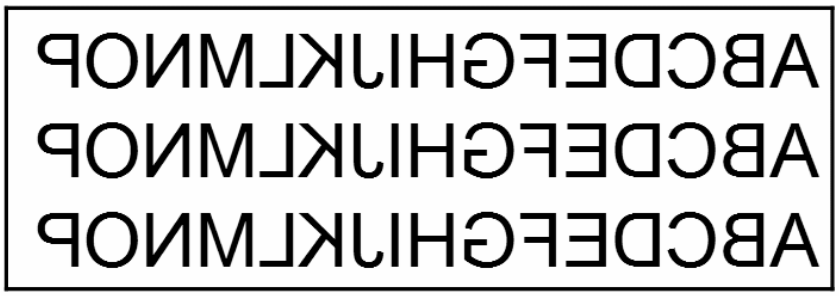
SHLC/SHLS ITO option pin can select at different direction for LCD panel

- Com normal direction/Seg normal direction



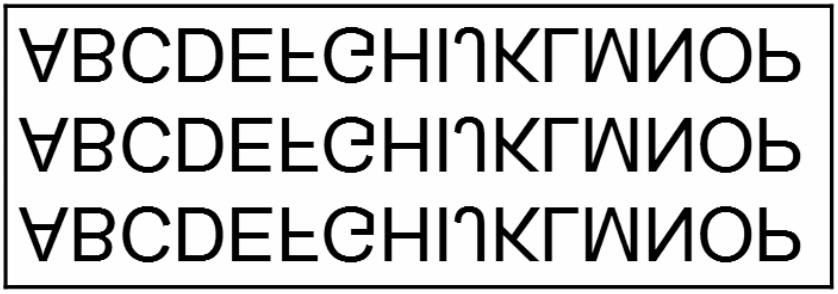
3 line x 16 characters, SHLC=1 SHLS=1

■ Com normal direction/Seg reverse direction



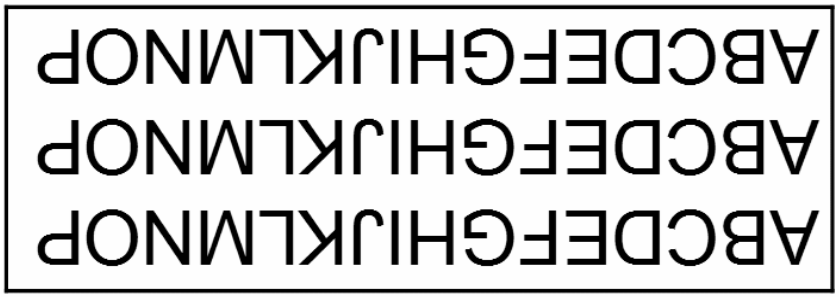
3 line x 16 characters, SHLC=1, SHLS=0

■ Com reverse direction/Seg normal direction



3 line x 16 characters, SHLC=0, SHLS=1

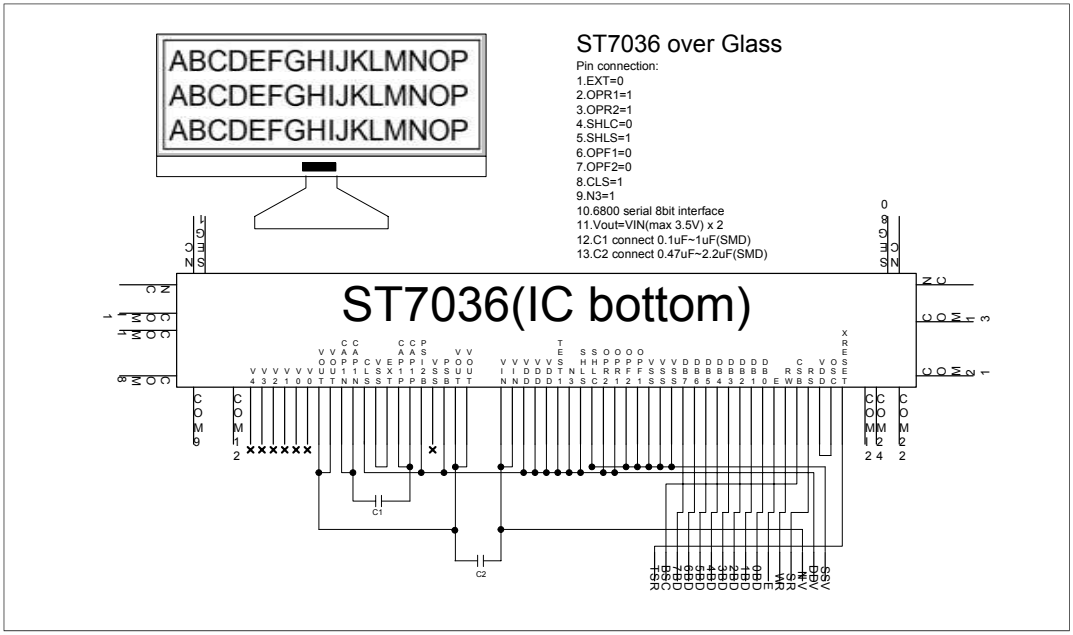
■ Com reverse direction/Seg reverse direction



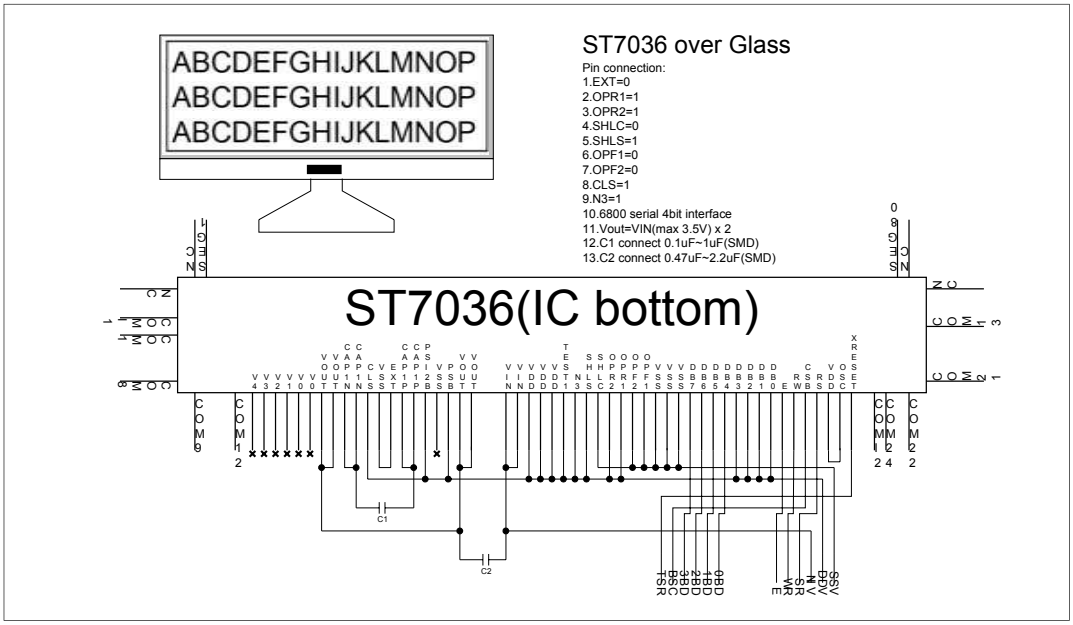
3 line x 16 characters, SHLC=0, SHLS=0

5. Application Circuit

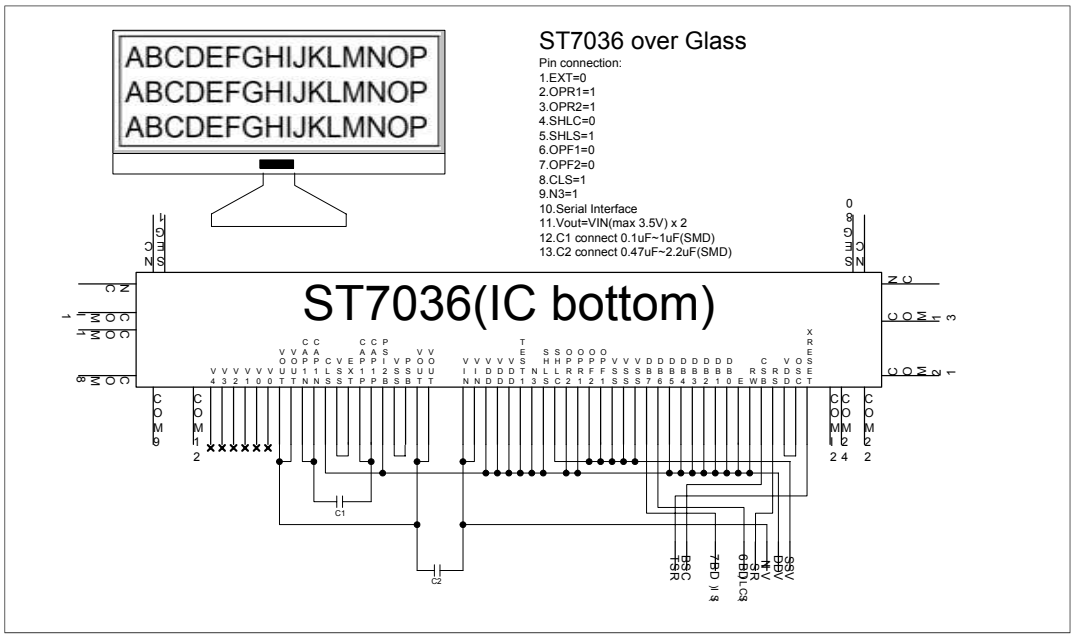
■ ST7036 over Glass,6800 serial 8bit interface, with booster and follower circuit on



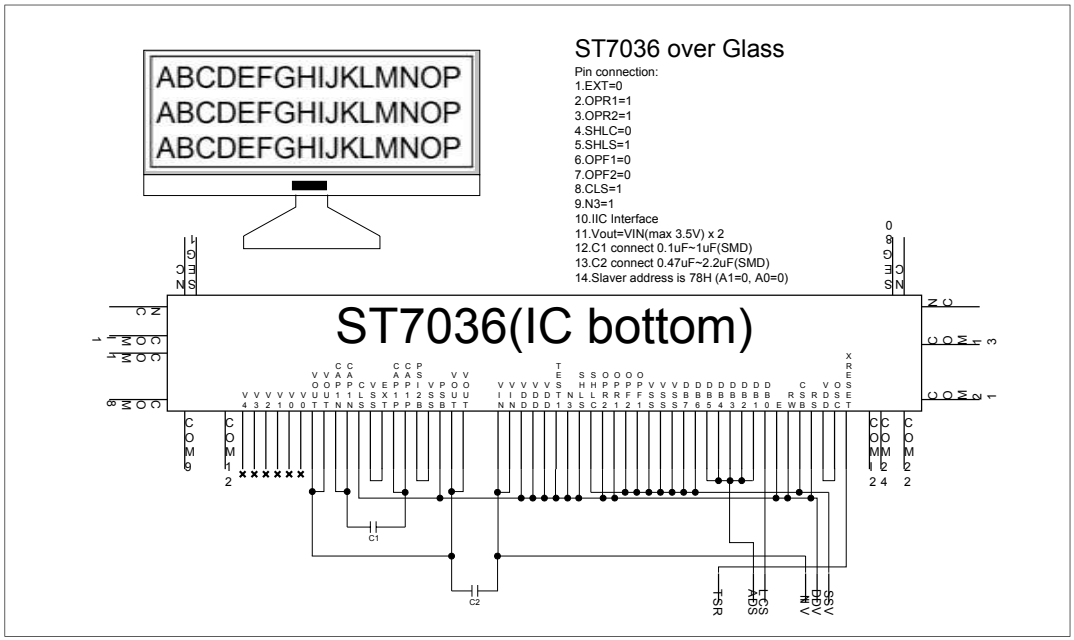
■ ST7036 over Glass,6800 serial 4bit interface, with booster and follower circuit on



■ ST7036 over Glass, serial interface, with booster and follower circuit on



■ ST7036 over Glass, I²C interface, with booster and follower circuit on



1. Feature

- Voltage operating range:
  - 2.7 to 5.5V
- Support 8 bit, 4 bit, serial bus MPU interface
- 64 x 16-bits character display RAM (max. 16 chars x 4 lines, LCD display range 16 char. X 2 lines
- 64 x 256-bits graphic display RAM (GDRAM)
- 2M-bits Chinese fonts ROM (CGROM) supporting 8192 Chinese fonts (16x16 dot matrix)
- 16K-bits half height ROM (HCGROM) supporting 126 character set (16x8 dot matrix)
- 64 x 16-bits character generation RAM (CGRAM)
- 15 x 16-bits total 240 ICON RAM (IRAM)
- 33-common x 64-segment (2 lines display) LCD drivers
- Automatic power on reset
- External reset pin (XRESET)
- With extension segment drivers display area can up to 16x2 lines
- RC oscillator built in (with external R)
- Low power design
  - Normal mode (450uA Typ VDD=5V)
  - Standby mode (30uA Max VDD=5V)
- VLCD (V0~ Vss): max 7V
- Graphic and character mix modes display
- Multiple instructions :
  - (Display clear)
  - (Return home)
  - (Display on/off)
  - (Cursor on/off)
  - (Display character blink)
  - (Cursor shift)
  - (Display shift)
  - (Vertical line scroll)
  - (By_line reverse display)
  - (Standby mode)
- Built in voltage booster (2 times)

2. General Description

ST7920 LCD controller/driver IC can display alphabets, numbers, Chinese fonts and self-defined characters. It supports 3 kinds of bus interface, namely 8 bit/ 4bit and serial. All functions, including display RAM, character generator ROM, LCD display drivers and control circuits are all in a one-chip solution. With a minimum system configuration, a Chinese character display system can easily achieved.

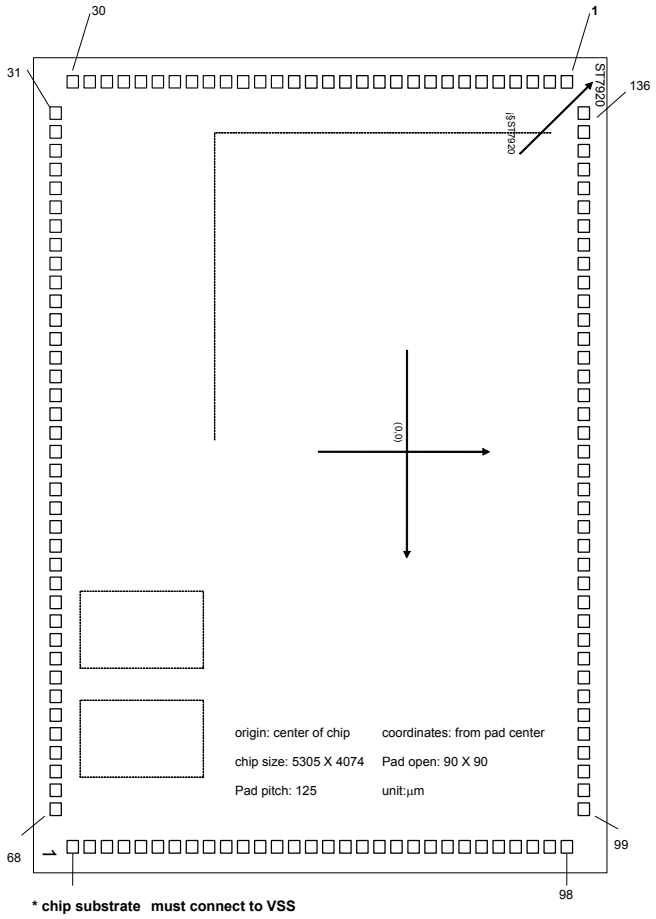
ST7920 includes character ROM with 8192 16X16 dots Chinese fonts and 126 16X8 dots half height alphanumerical fonts. Also for graphic display it supports 64x256 dots graphic display area (GDRAM) and 240 dots ICON RAM. Mix mode display with both character and graphic data is possible. ST7920 has built in 4 sets CGRAM providing software programmable 16X16 font.

ST7920 has wide operating voltage (2.7V to 5.5V) and low power consumption suitable for battery power portable device.

ST7920 LCD driver consists of 33 common and 64 segments. Together with extension segment driver ST7921, ST7920 can support up to 33 common x 256 segments display.

Product	Font type
ST7920-0A	BIG-5 code traditional character set
ST7920-0B	GB code simplified character set
ST7920-0C	GB code,BIG-5 code and Japanese code

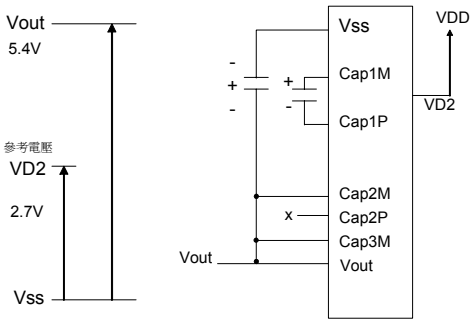
3. Pad Arrangement



- origin: center of chip
- coordinates: from pad center
- chip size: 5305 X 4074
- Pad open: 90 X 90
- Pad pitch: 125
- unit: μm

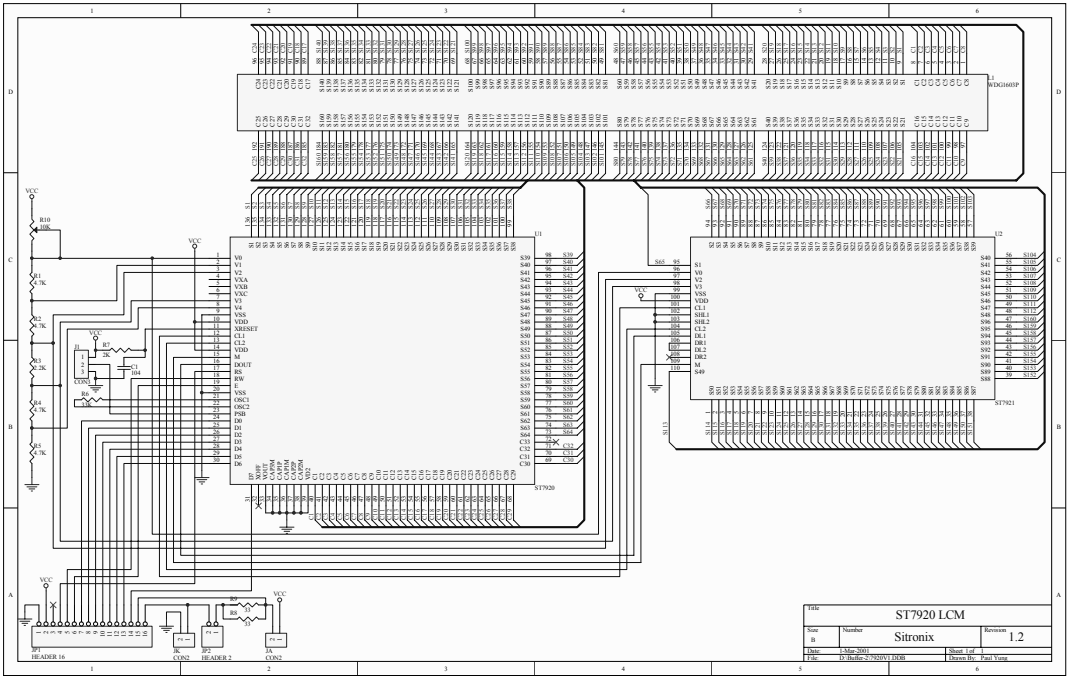
*chip substrate must connect to VSS

Built in voltage booster



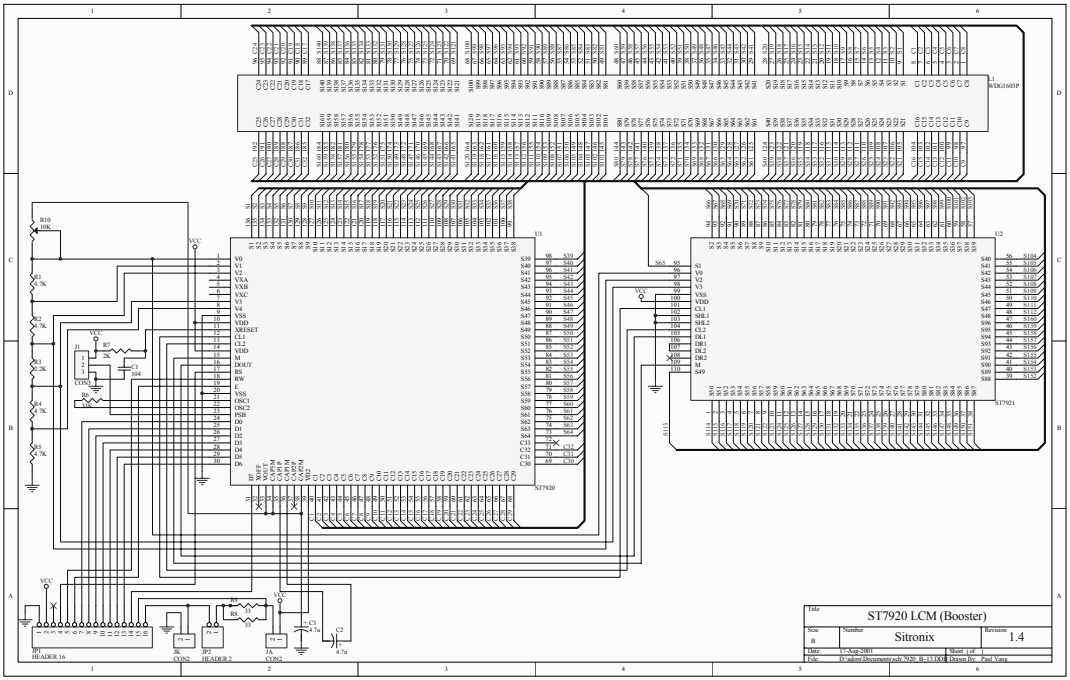
4. Application circuit 1 :

- LCD : 32 COM x 160 SEG
- LCD Voltage : VCC



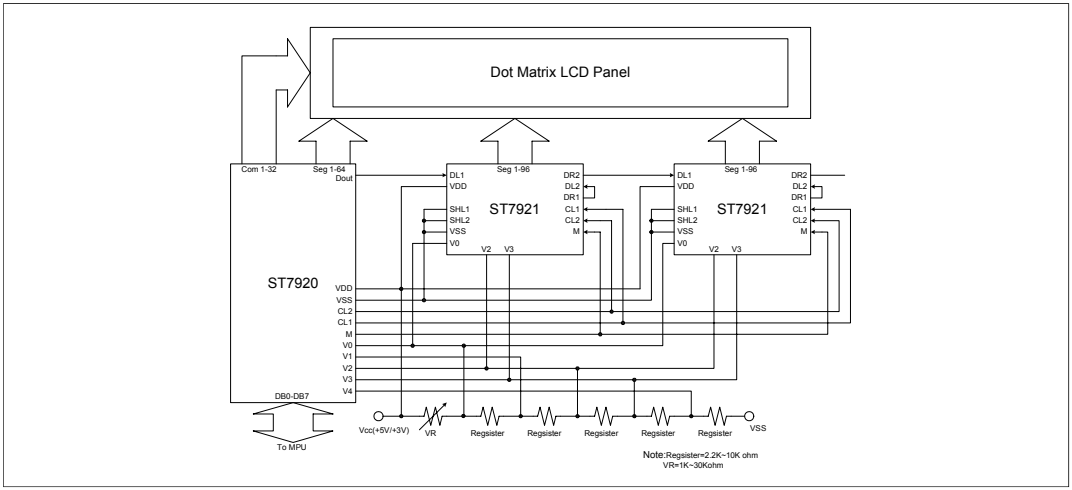
5. Application circuit 2:

- LCD : 32 COM x 160 SEG
- LCD Voltage : VCC x 2 (Voltage doubler is used) *Vlcd should not over 7v.



6. Application circuit 3 :

- LCD : 2Line 16Chinese Word (32 COM x 256 SEG)



1. Feature

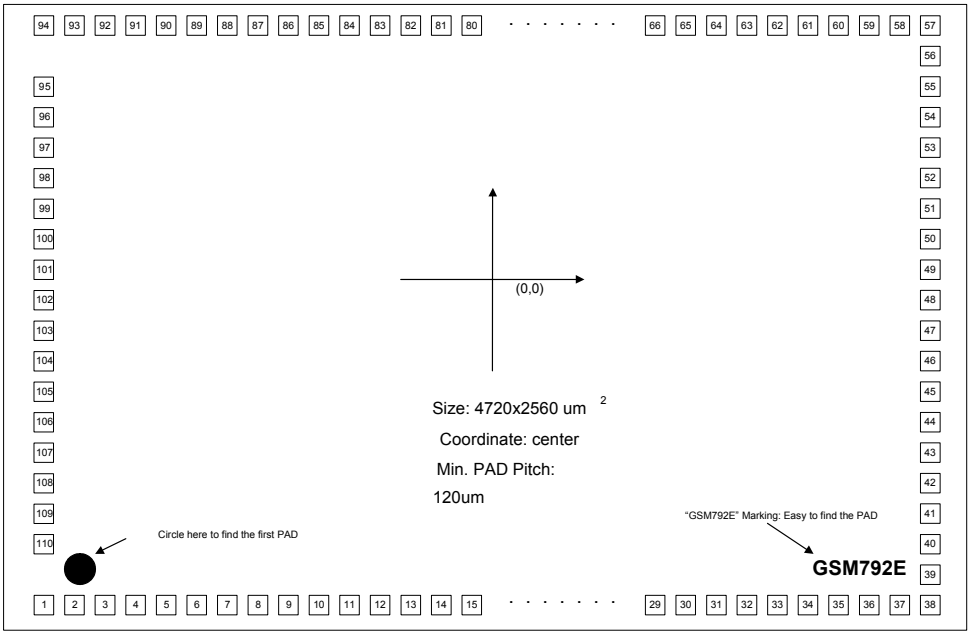
- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (V0~VSS) : 3V ~ 7V
- Dot matrix LCD driver with two 48 channel outputs
- Bias voltage (V0 ~ V4)
- Input/Output signals
- Input : Serial display data and control pulse from controller IC
- Output : 48 X 2 channels waveform for LCD driving
  - Bare chip available

2. General Description

ST7921 is a segment driver for dot matrix type LCD display. It features 96 channels with 48 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

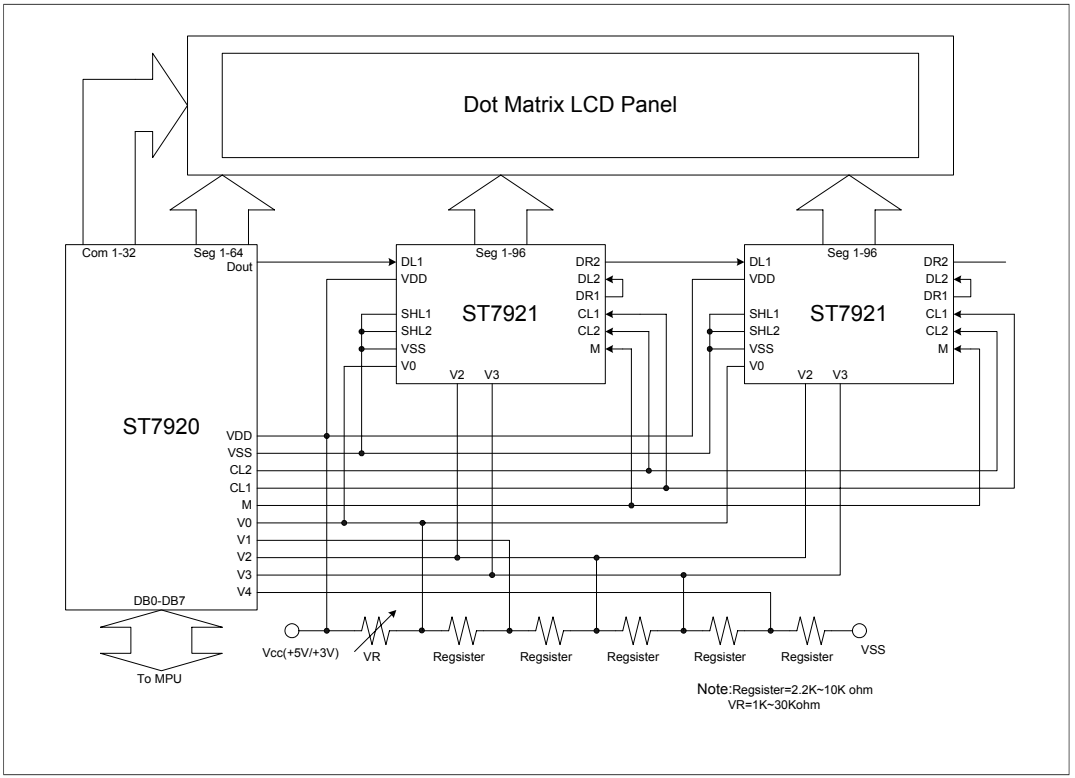
The ST7921 can convert serial data received from an LCD controller, such as ST7920, into parallel data and send out LCD driving waveforms to the LCD panel. The ST7921 is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment driver.

3. Pad Arrangement



*chip substrate must connect to VSS

4. Application Circuit : (2Line x 16 Chinese Word)



Graphic LCD Drivers Series

Part No.	#COM x #SEG	VDD	VLCD	Booster	I/O	Package
ST8808	80S driver	2.5~5.5	Max15	x	4 bit parallel or serial	Bare chip
ST8809	80C/S driver	2.5~5.5	Max15	2X, 3X, 4X, 5X, 6X	4 bit parallel or serial	Bare chip
ST8012	120C/S driver	2.5~5.5	Max16	2X, 3X, 4X, 5X, 6X	4 bit parallel or serial	Bare chip
ST8011	120S driver	2.5~5.5	Max16	x	4 bit parallel or serial	Bare chip
ST8016	160C/S driver	2.5~5.5	15~40	X	4 /8bit parallel	Gold bump Or TCP
ST8024	240 C/S driver	2.5~5.5	15~42	X	4 /8bit parallel	Gold bump Or TCP

1. Feature

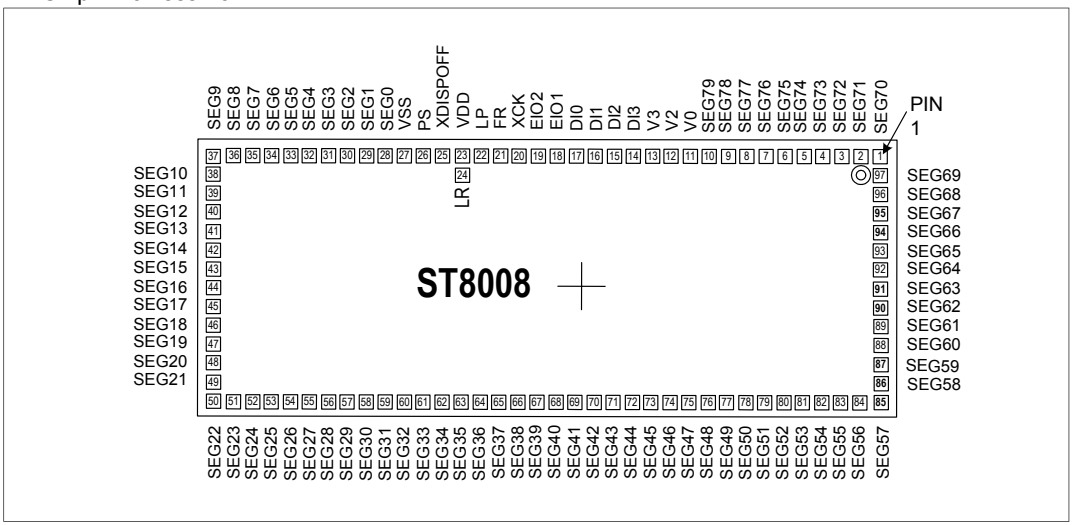
- Number of LCD drive outputs: 80
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Package: 96-pin COB.
- (Segment mode)
- Shift clock frequency
  - 20 MHz (MAX.): VDD = +5.0 ± 0.5 V
  - 15 MHz (MAX.): VDD = +3.0 to + 4.5 V
  - 12 MHz (MAX.): VDD = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 80 bits of input data
- Line latch circuits are reset when XDISPOFF active

2. General Description

The ST8008 is a 80-output segment driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary . The ST8008 is good as a segment driver, and it can create a low power consuming, high-resolution LCD.

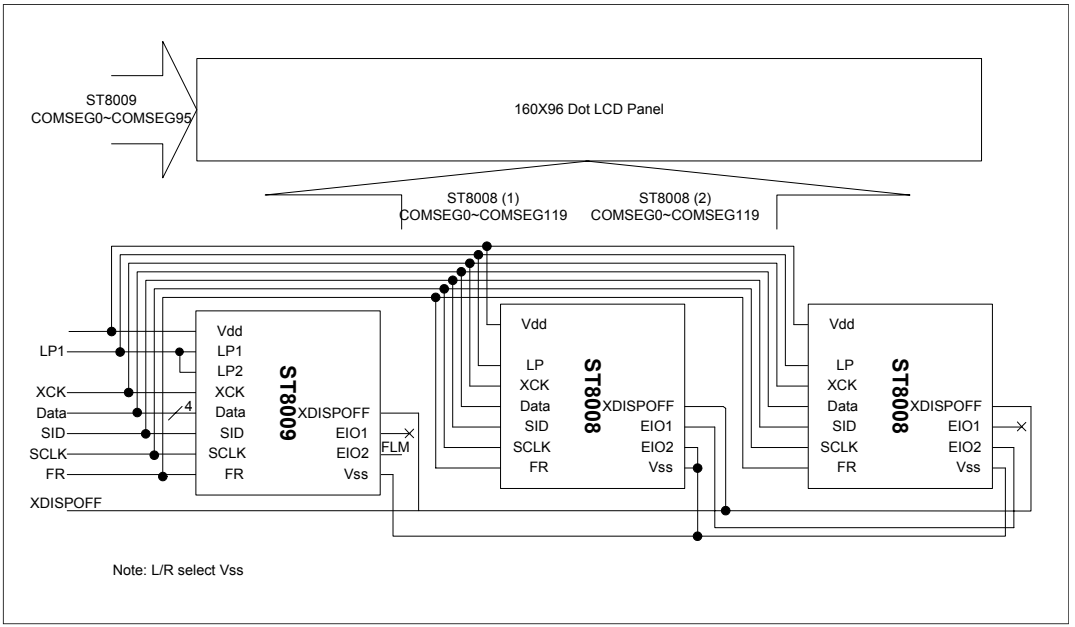
3. Pad Arrangement

- Chip size: 3800(μm)X1560(μm)
- Pad size: 80(μm)X80(μm)
- Pin Pitch: 100(μm)~120(μm)
- Origin: chip center(0,0)
- Chip Thiclness:19 mil



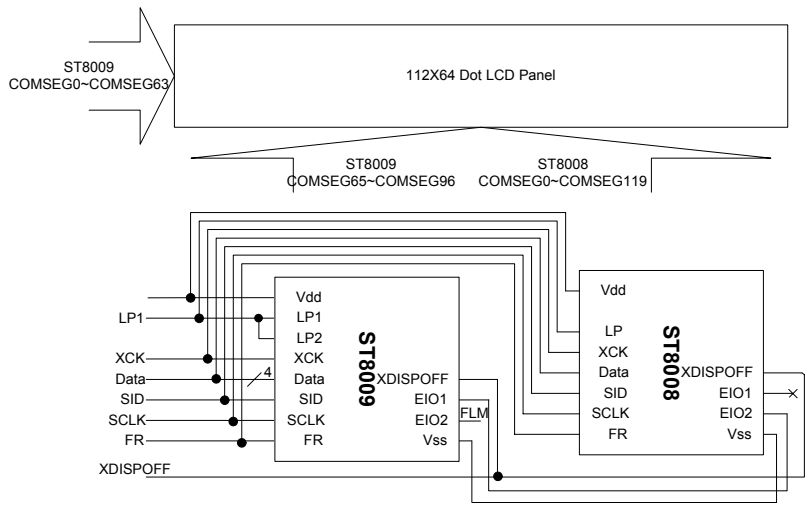
4. Application Circuit

4.1 When use one ST8009 and two ST8008 (160X96)



Note: L/R select Vss

4.2 When use one ST8009 and one ST8008 (112X64)



Note: L/R select Vss

1. Feature

- Number of LCD drive outputs: 96
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption and low output impedance
- Display duty selectable by internal select register

SEL2,SEL1,SEL0	DUTY	BIAS
0 0 0	---	Segment mode
0 0 1	1/16	1/5 or 1/4
0 1 0	1/32	1/6 or 1/5
0 1 1	1/48	1/7 or 1/5
1 0 0	1/64	1/9 or 1/7
1 0 1	1/80	1/9 or 1/7
1 1 0	1/96	1/10 or 1/8
1 1 1	1/96	1/10 or 1/8

- Low-power liquid crystal display power supply circuit equipped internally.
  - Booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)
  - Regulator circuit
  - Follower circuit
- Abundant command functions
  - LCD bias set, electronic volume, VSS voltage regulation internal resistor ratio and booster frequency.
  - All Functions have initial value, user can set by programmable.
- Package: 124-pin COB.

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): VDD = +5.0 ± 0.5 V
  - 15 MHz (MAX.): VDD = +3.0 to + 4.5 V
  - 12 MHz (MAX.): VDD = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable by programmable.
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 16、32、48 、64、 80、96 bits of input data
- Line latch circuits are reset when XDISPOFF active

(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in X-bit shift register
- Available in a single mode
  Y1->YX Single mode
  YX->Y1 Single mode
- PS:X=16、32、48、64、64、80、96

The above 4 shift directions are register selectable

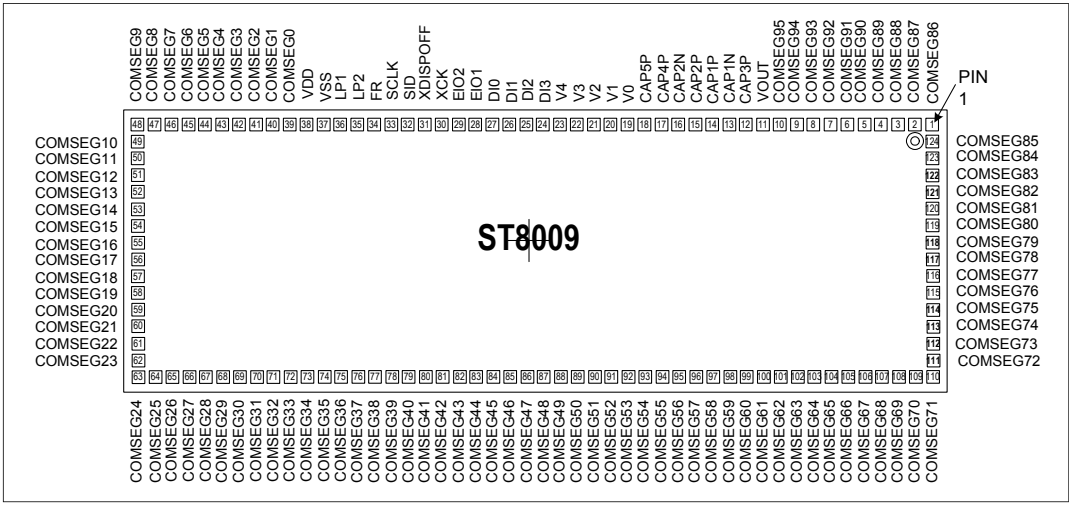
- Shift register circuits are reset when XDISPOFF active

2. General Description

The ST8009 is a 96-output segment/common driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary . The ST8009 is good as a segment driver or a common driver or a common/segment driver, and it can create low power consumption, high-resolution LCD. The ST8009 have eight modes can selected to set common and segment numbers by select pin. The ST8009 also have analog DC/DC converter to used.

3. Pad Arrangement

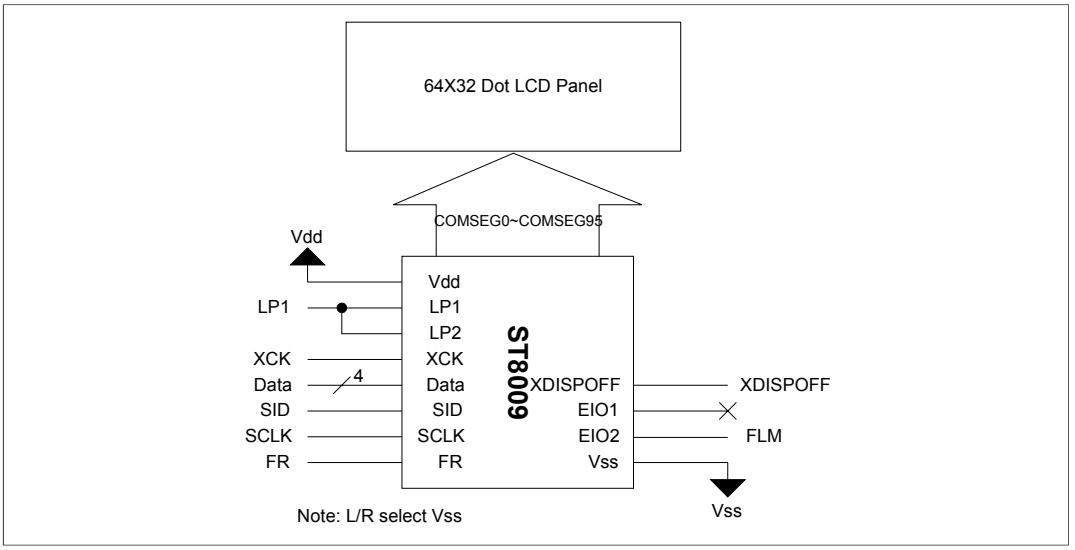
- Chip size: 5070.0(um) x1790.0 (um)
- Pad size : 80 (um) x80 (um)
- Pad pin pitch: 100 (um) ~ 140 (um)
- Origin : chip center (0,0)
- Chip Thickness : 19 mil



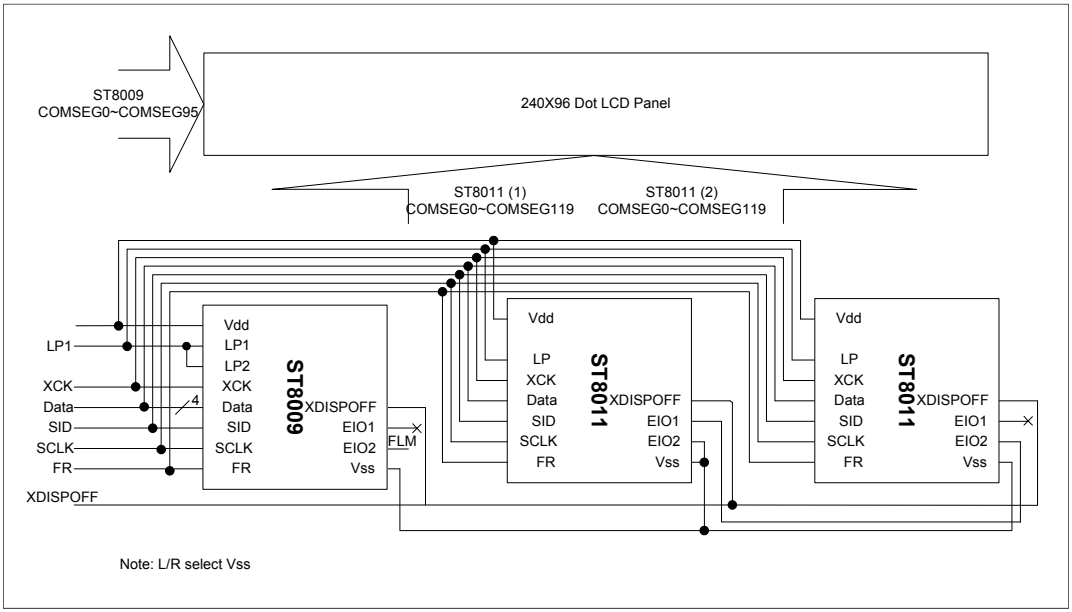
Substrate Connect to Vss.

4. Application Circuit for Module

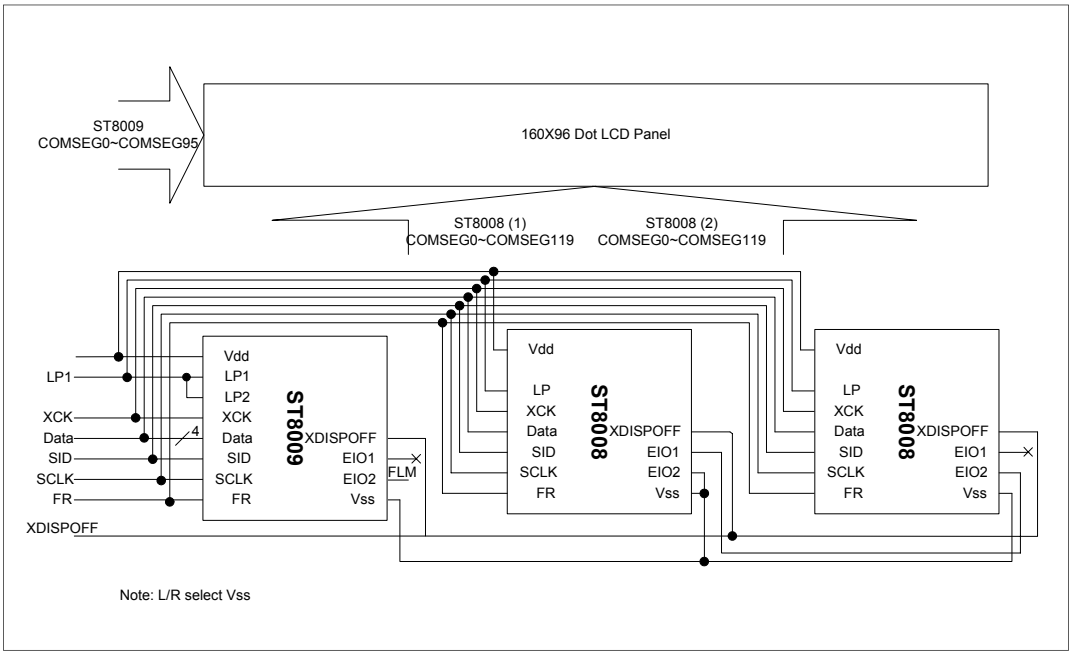
4.1 When only use one ST8009 in mix mode (64X32)



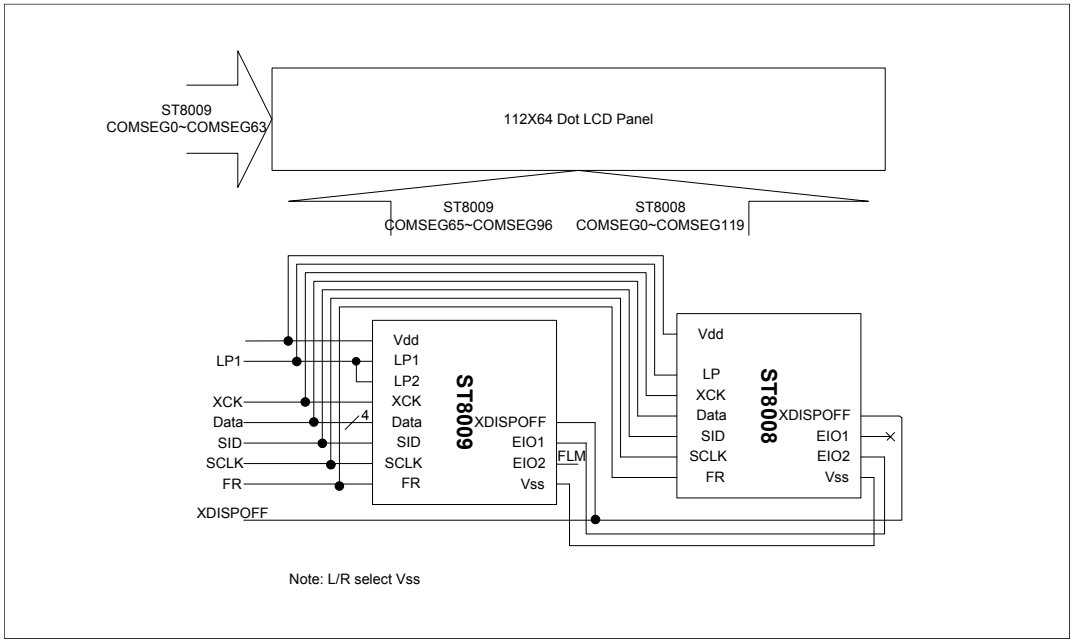
4.2 When use one ST8009 and two ST8011 (240X96)



4.3 When use one ST8009 and two ST8008 (160X96)



4.4 When use one ST8009 and one ST8008 (112X64)



1. Feature

- Number of LCD drive outputs: 120
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption and low output impedance
- Display duty selectable by select pin

SEL2,SEL1,SEL0	DUTY	BIAS
0 0 0	---	Segment mode
0 0 1	1/32	1/6 or 1/5
0 1 0	1/48	1/7 or 1/5
0 1 1	1/64	1/9 or 1/7
1 0 0	1/80	1/9 or 1/7
1 0 1	1/96	1/10 or 1/8
1 1 0	1/112	1/11 or 1/9
1 1 1	1/120	1/11 or 1/9

- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)
- Abundant command functions
  LCD bias set, electronic volume, VSS voltage regulation internal resistor ratio and booster frequency.
  All Functions have initial value, user can use the default value or setting by programmable pin to set.
- If select segment mode then except booster circuit will opened others circuit (follower and regulator circuit) will automatic closed.
- When don't used the serial interface, we can select one of default modes by serial interface pins please see Table5.
- Package: Bare chip available

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): VDD = +5.0 ± 0.5 V
  - 15 MHz (MAX.): VDD = +3.0 to + 3.6 V
  - 12 MHz (MAX.): VDD = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 88、72、56 、40、 24、8 or 120 bits of input data
- Line latch circuits are reset when XDISPOFF active

(Common mode)

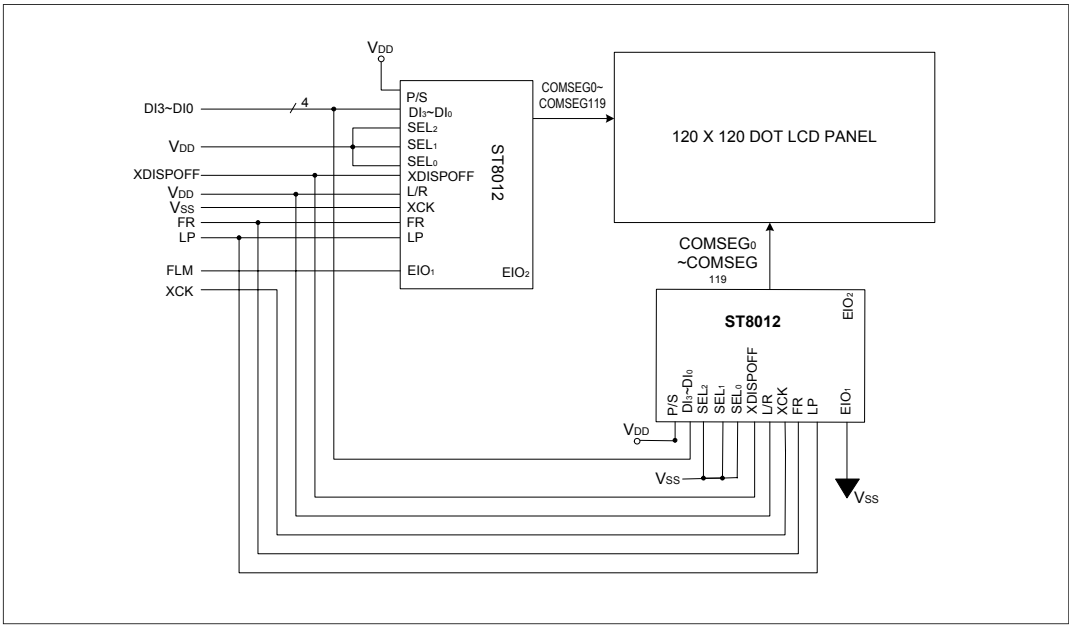
- Shift clock frequency: 4 MHz (MAX.)
- Built-in X-bit shift register
- Available in a single mode
- Y1->YX Single mode
  YX->Y1 Single mode
  PS:X=32、48、64、80、96、112、120
  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when XDISPOFF active.

2. General Description

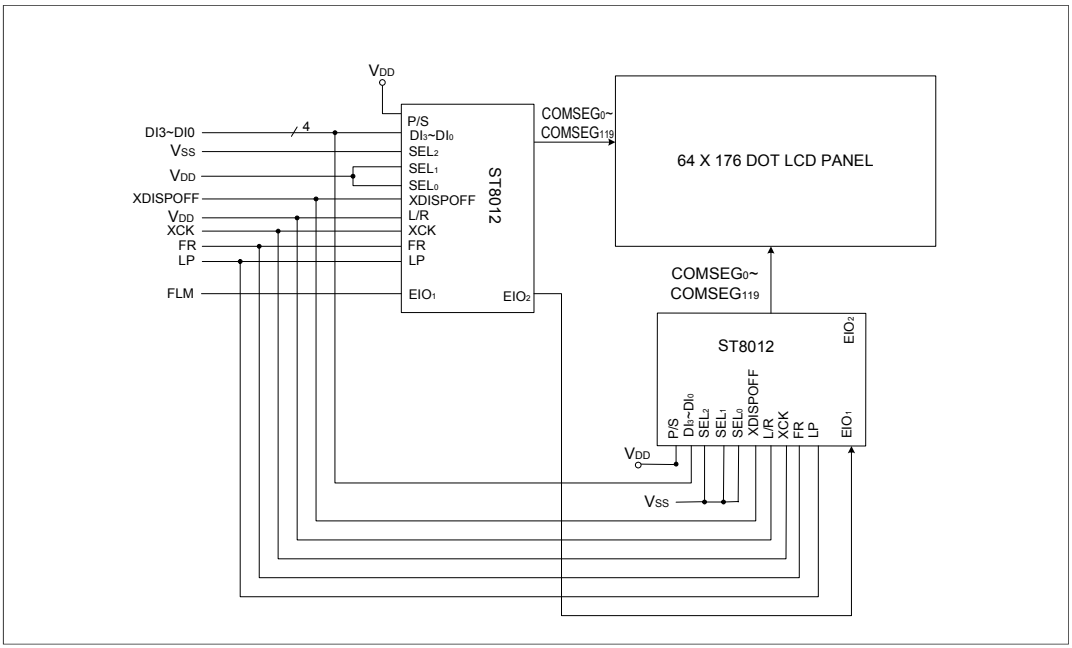
The ST8012 is a 120-output segment/common driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary . The ST8012 is good as a segment driver or a common driver or a common/segment driver, and it can create a low power consuming, high-resolution LCD. The ST8012 have eight modes can selected to set common and segment numbers by select pin. The ST8012 also have analog DC/DC converter to used.

3. Application Circuit for Module

3.1 1/120 duty, 120 commons and 120 segments



3.2 1/64 duty, 64 commons and 176 segments



1. Feature

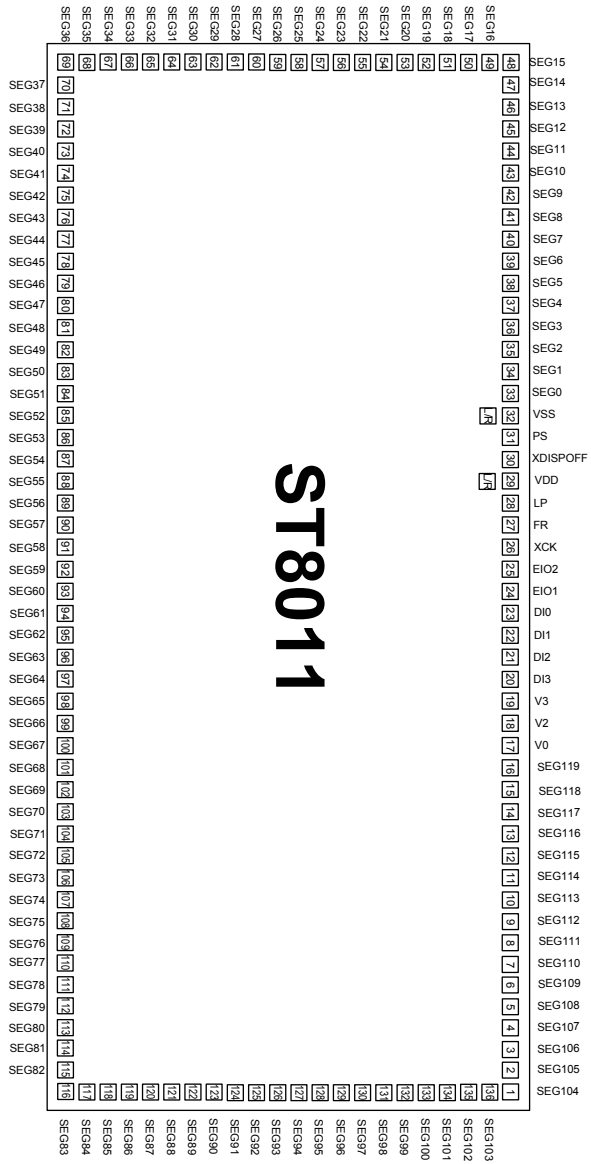
- Number of LCD drive outputs: 120
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Package: Bare chip available.
- (Segment mode)
- Shift clock frequency
  - 20 MHz (MAX.): VDD = +5.0 ± 0.5 V
  - 15 MHz (MAX.): VDD = +3.0 to + 4.5 V
  - 12 MHz (MAX.): VDD = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 120 bits of input data
- Line latch circuits are reset when XDISPOFF active

2. General Description

The ST8011 is a 120-output segment driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary . The ST8011 is good as a segment driver, and it can create a low power consuming, high-resolution LCD.

3. Pad Arrangement

- Chip size: 4860(μm) × 2220(μm)
- Pad size: 80(μm) × 80(μm)
- Pin Pitch: 110 μm



Substrate Connect to Vss.

1. Feature

- Number of LCD drive outputs: 160
- Supply voltage for LCD drive: +15.0 to +40.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance
- Package: 186-pin TCP (Tape Carrier Package) or Gold-bumped chip

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): VDD = +5.0 ± 0.5 V
  - 15 MHz (MAX.): VDD = +3.0 to + 4.5 V
  - 12 MHz (MAX.): VDD = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input data
- Line latch circuits are reset when DISPOFF active

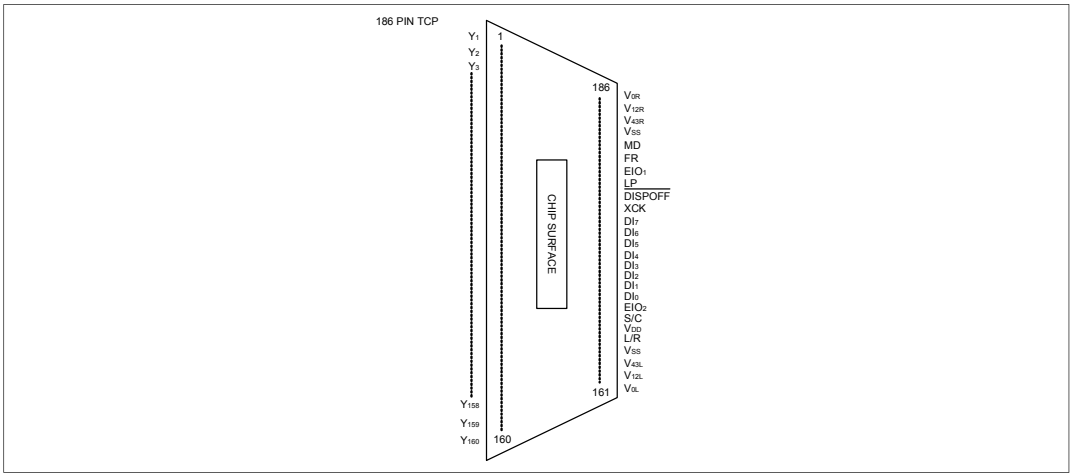
(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
  - Y1->Y160 Single mode
  - Y160->Y1 Single mode
  - Y1->Y80, Y81->Y160 Dual mode
  - Y160->Y81, Y80->Y1 Dual mode
- The above 4 shift directions are pin-selectable
- Shift register circuits are reset when DISPOFF

2. General Description

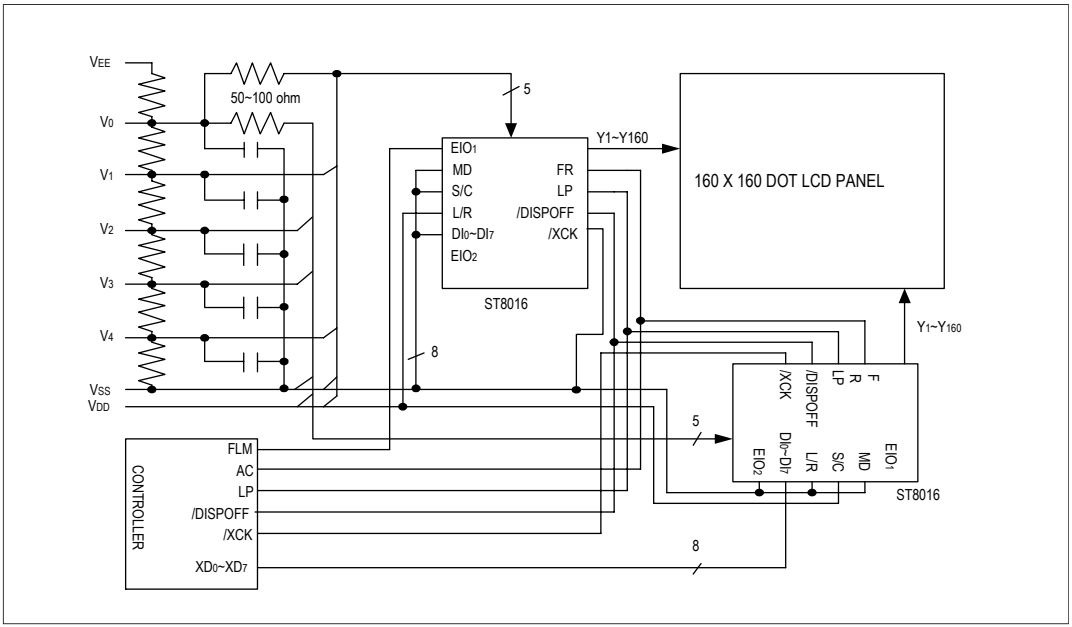
The ST8016 is a 160-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The ST8016 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3. Pin Connections



4. Application Circuit

4.1 Application Circuit for Module



1. Feature

- Number of LCD drive outputs: 240
- Supply voltage for LCD drive: +15.0 to +42.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance
- Package: 269-pin TCP (Tape Carrier Package) or Gold-bumped chip

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): VDD = +5.0 ± 0.5 V
  - 15 MHz (MAX.): VDD = +3.0 to + 4.5 V
  - 12 MHz (MAX.): VDD = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Line latch circuits are reset when DISPOFF active

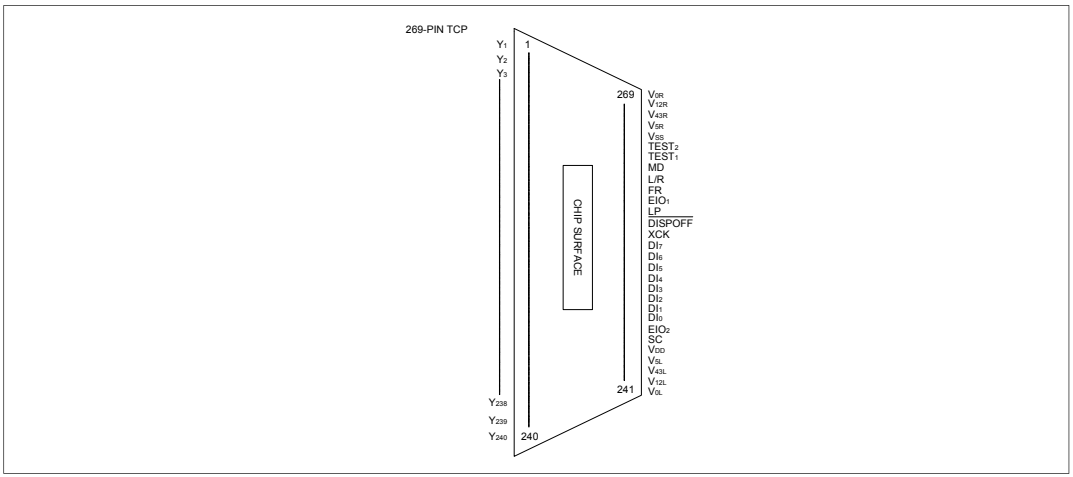
(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
- Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)
  - Y1->Y240 Single mode
  - Y240->Y1 Single mode
  - Y1->Y120, Y121->Y240 Dual mode
  - Y240->Y121, Y120->Y1 Dual mode
- The above 4 shift directions are pin-selectable
- Shift register circuits are reset when DISPOFF active

2. General Description

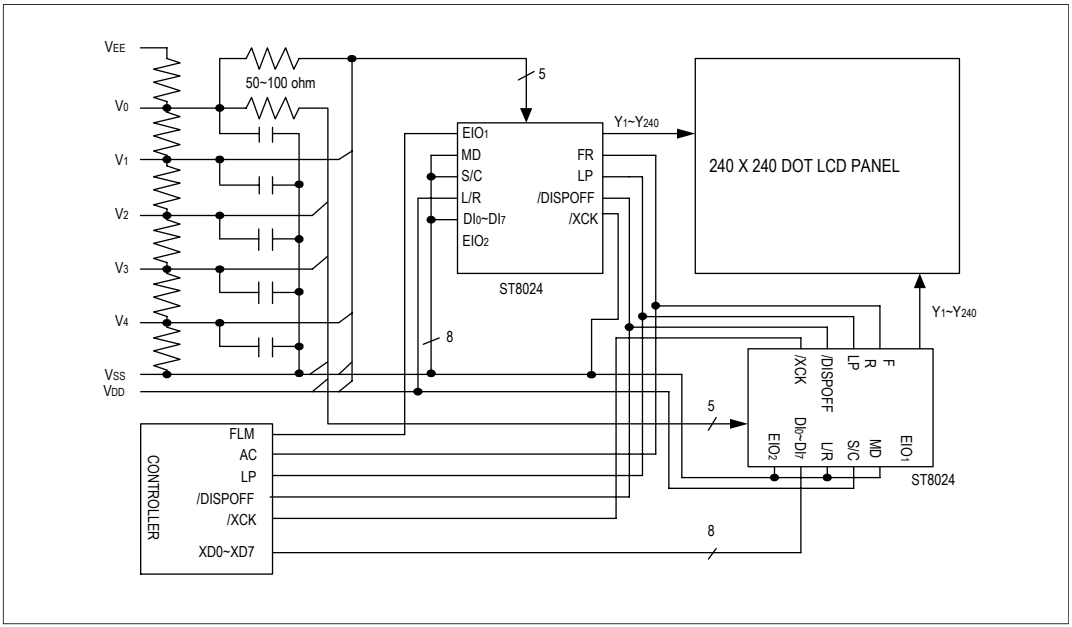
The ST8024 is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The ST8024 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3. Pin Connections



4. Application Circuit

4.1 Application Circuit for Module



Single Chip LCD Controller/Driver Series

Part No.	#COM x#SEG	TONE	VDD	VLCD	Booster	I/O	Package
ST7522	17Cx96S	MONO	2.7~5.5	3.5~7	2x	8 bit or serial	Bare chip
ST7533	33Cx96S	MONO	1.8~3.3	4~13	4X Ext 9C	8 bit or serial	Gold bump
ST7565V/P	65Cx132S	MONO	(1.8~3.3)	4~13	6X Ext 9C	8 bit or serial	Gold bump/ TCP
ST7549 ST7549i	68Cx102S	MONO	(1.7~3.3)	(MAX13)	5X Ext 2C	8 bit 3/4 -SPI I2C	Gold bump
ST7568 ST7568i	68Cx102S	4-Gray	1.7~3.3	MAX13	5X Ext 2C	8 bit 4- SPI I2C	Gold bump
ST7541	129Cx128S	4-Gray	1.8~3.3	4~15	6X Ext 2C	8 bit 3/4- SPI I^2C	Gold bump
ST7528 ST7528i	101Cx160S 129Cx132S	16-Gray	1.8~3.3	4~15	6X Ext 2C	8 bit 3/4- SPI I^2C	Gold bump
ST7632	132Cx132RGB	65K color	(1.7~3.6)	MAX21	TBD	8/16 bit 2,3,4 line SPI	Gold bump

1. Feature

- Fast 8-bit MPU interface compatible with 80- and 68- family microcomputers and serial interface
- Clock synchronous serial interface
- Many command set Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set , column address set , status read , display all points ON/OFF, LCD bias set, electronic volume, read/modify/ write, segment driver direction select, power saver, static indicator, adjustable OSC frequency, booster input voltage select, follower input voltage and amplified ratio selectable
- 4 static indicator and 96 icon available
- Total 118 (segment + common + static) drive sets
- Wide range of supply voltages
  - V_{DD} - VSS : 2.7 to 5.5 V
  - V_{DD} - V5 : 3.5 to 7.0 V
  - V_{DD} - VCAP3 : 3.5 to 7.0 V
- Low-power CMOS
- 64 level digital contrast control
- Bare chip available

2. General Description

The ST7522 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.

The drivers are available in two configurations The ST7522 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

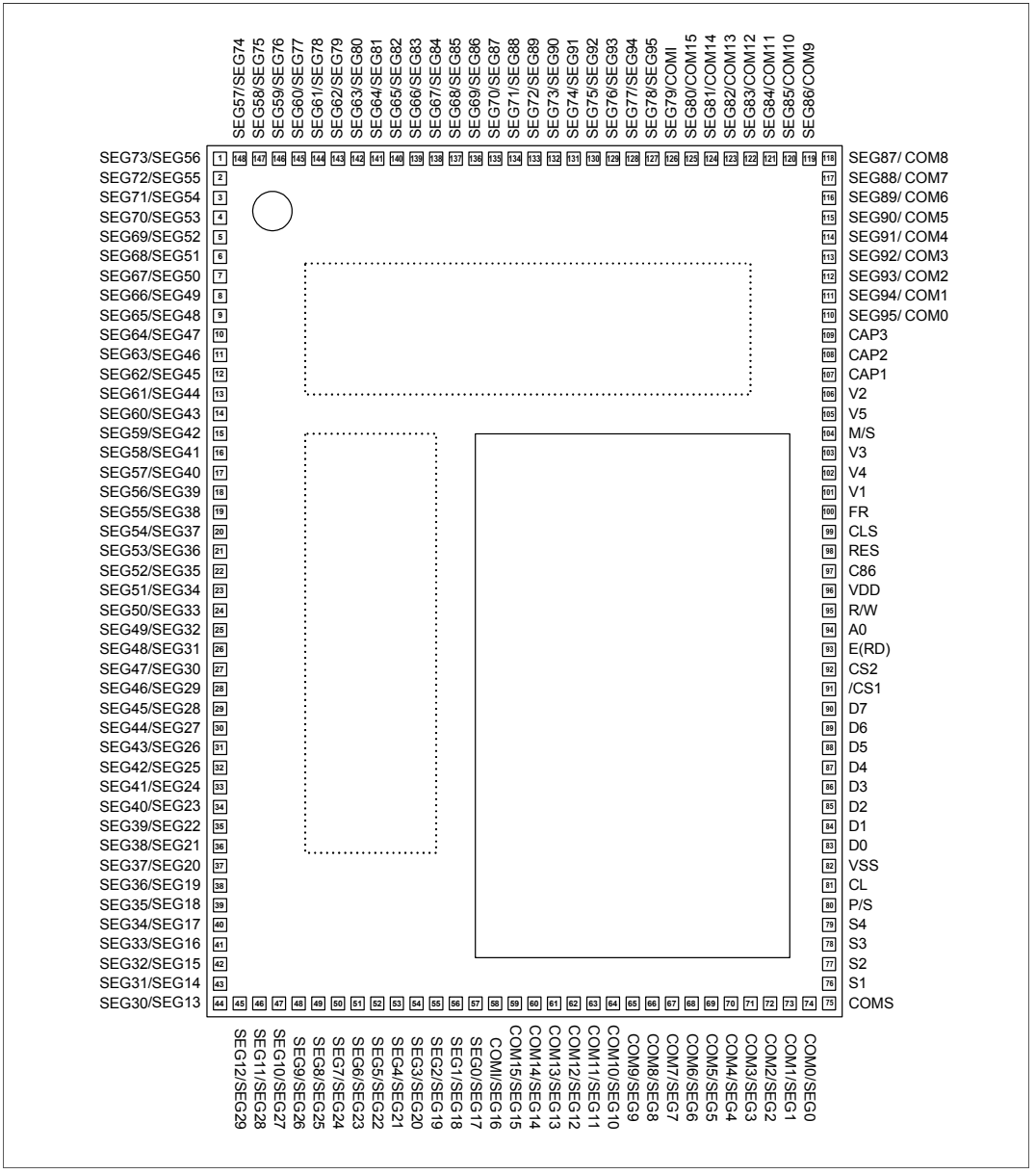
The ST7522 which is able to drive 1 line of 6 Chinese characters or 2 lines of 12 Chinese characters each line with two ST7522.

Product name	Clock frequency		Number of COM	Number of SEG	Bias	Duty
	On-Chip	External				
ST7522D	1.2KHz,2.4KHz (When VDD=3.0V)	2.8KHz	17	96	1/5,1/6	1/17,1/33

3. PAD Arrangement

- Chip specifications of AL pad package
- Chip size : 3720 µm x 5040 µm
- Minimum pad pitch : 110µm
- Pad size : 90µm X 90µm

* Substrate connect to VDD.

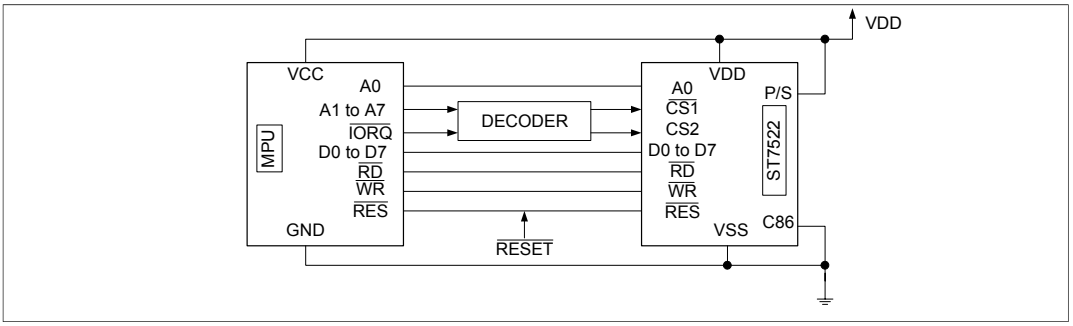


4. The MPU Interface (Reference examples)

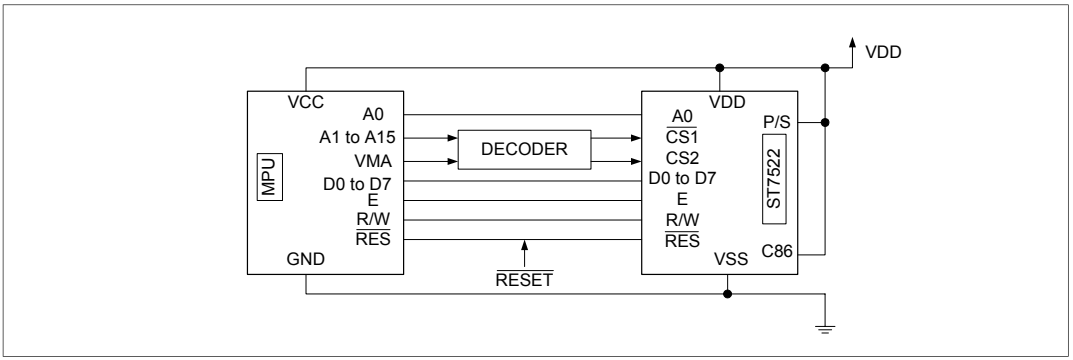
The ST7522 Series can be connected to either 80x86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7522 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7522 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

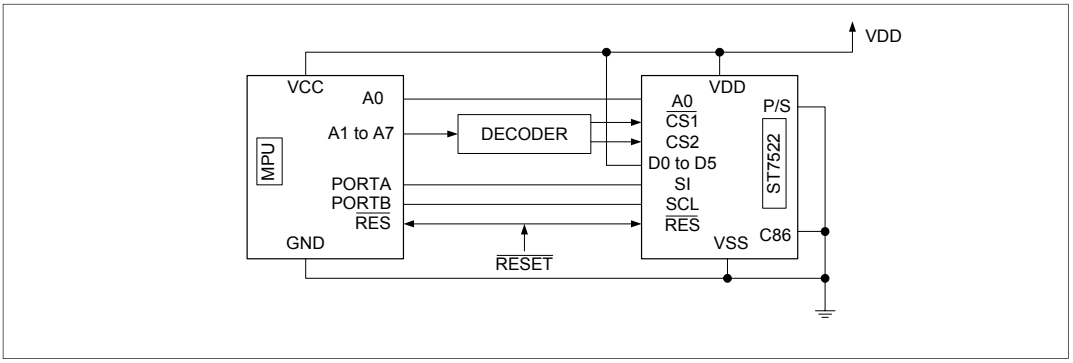
4.1 8080 Series MPUs



4.2 6800 Series MPUs



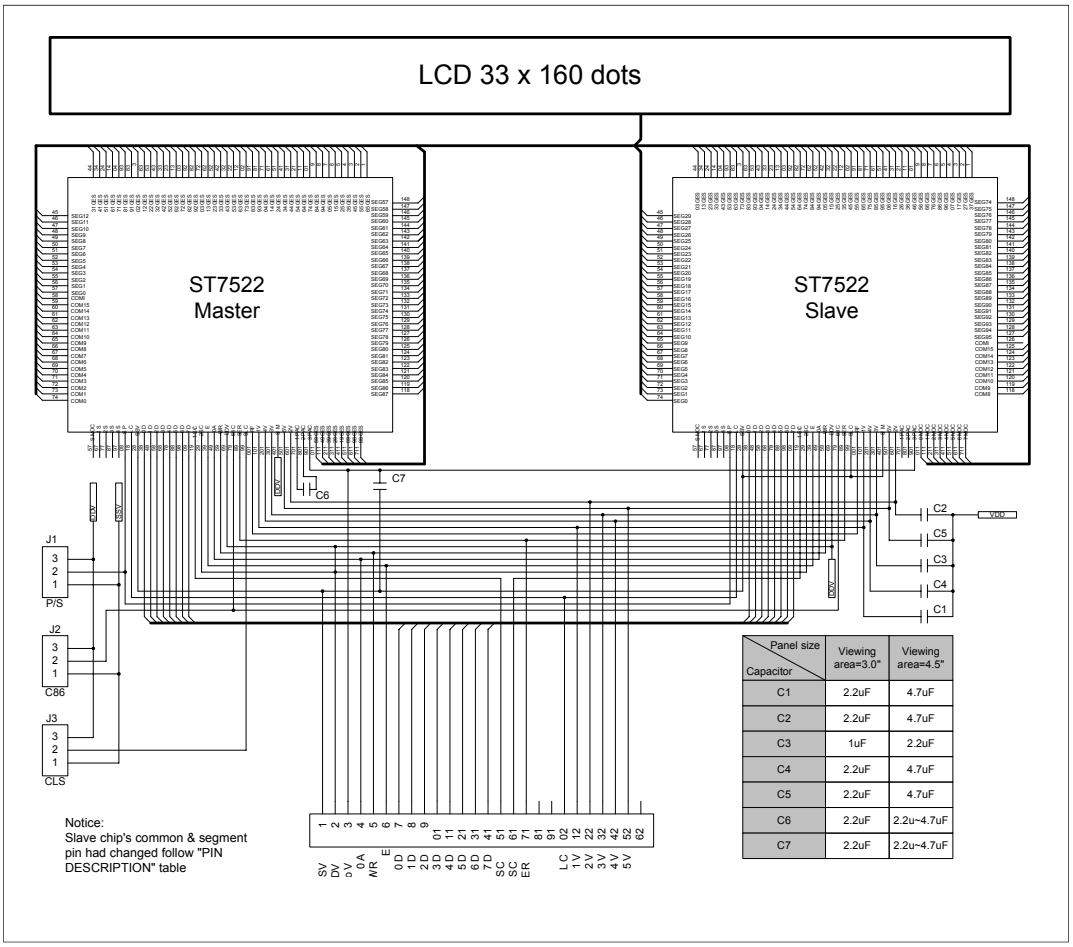
4.3 Using the Serial Interface



5. Application (Master & Slave Mode)

Condition:

1. 2 time booster
2. internal follower
3. internal OSC frequency

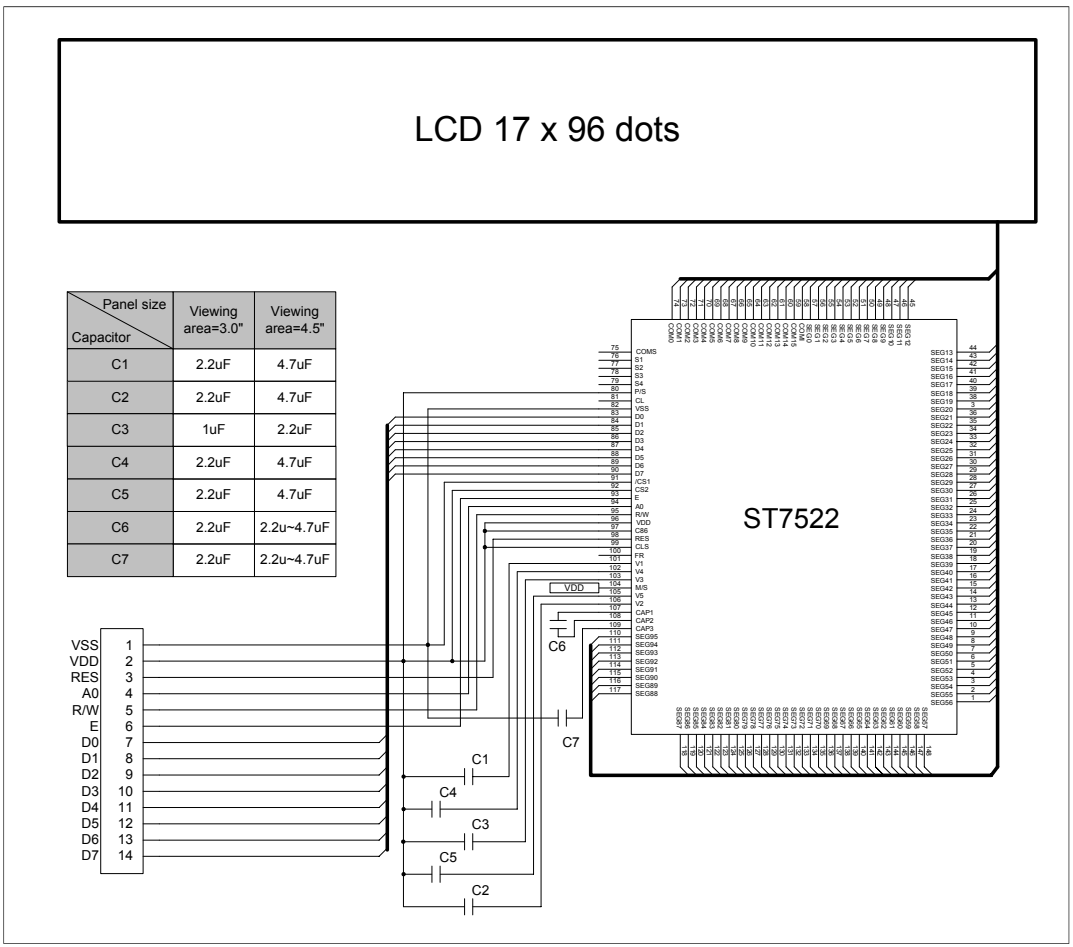


Capacitor \ Panel size	Viewing area=3.0"	Viewing area=4.5"
C1	2.2uF	4.7uF
C2	2.2uF	4.7uF
C3	1uF	2.2uF
C4	2.2uF	4.7uF
C5	2.2uF	4.7uF
C6	2.2uF	2.2u~4.7uF
C7	2.2uF	2.2u~4.7uF

6. Application (Only use master mode)

Resemble ST7066U+ST7065C (2 line x 16 word with 14 pin assign application)
condition:

1. 68 interface
2. 2 time booster
3. internal follower
4. internal OSC frequency



Panel size / Capacitor	Viewing area=3.0"	Viewing area=4.5"
C1	2.2uF	4.7uF
C2	2.2uF	4.7uF
C3	1uF	2.2uF
C4	2.2uF	4.7uF
C5	2.2uF	4.7uF
C6	2.2uF	2.2u~4.7uF
C7	2.2uF	2.2u~4.7uF

1. Features

- Direct display of RAM data through the display data RAM.
- RAM capacity : 33 x 96 = 3168 bits
- Display duty selectable by select pin
  - 1/33 duty : 33 common x 96 segment
  - 1/17 duty : 17 common x 96 segment
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs) / Serial interfaces are supported.
- Abundant command functions Display data Read/Write, display ON/OFF, Normal/ Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of 2X/3X/4X , where the step-up voltage reference power supply can be input externally). High-accuracy voltage adjustment circuit (Thermal gradient -0.15%/°C) V5 voltage regulator resistors equipped internally, V1 to V4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption Operating power when the built-in power supply is used (an example)
  70uA (VDD - VSS = VDD - VSS2 =3.0 V, Quad voltage, V5 - VDD = - 11.0 V).
  Conditions: When displays pattern OFF and the normal mode is selected.
- Power supply operate on the low 1.8 voltage
  Logic power supply VDD - VSS = 1.8V to 3.3V (+10% Range)
  Boost reference voltage: VDD - VSS2 = 1.8V to 3.3V
  Booster maximum voltage limited
  VOUT= -13V (+10% Range)
  Liquid crystal drive power supply:
  VDD - V5 = 4.0V to 13.0 V
- Wide range of operating temperatures: -40 to 85°C
- CMOS process
- These chips not designed for resistance to light or resistance to radiation.
- Gold bumped chip available

2. General Description

The ST7533 is a single-chip dot matrix LCD drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the ST7533 contain 33x96 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The ST7533 chips contain 33 common output circuits and 96 segment output circuits, so that a single chip can drive a 33x96 dot display (capable of displaying 8 columnsx4 rows of a 16x16 dot kanji font).

Moreover, the capacity of the display can be extended through the use of master/slave structures between chips. The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, resistors for LCD driver power voltage adjustment and a display clock CR oscillator circuit, the ST7533 can be used to create the lowest power display system with the fewest components for high-performance portable devices.

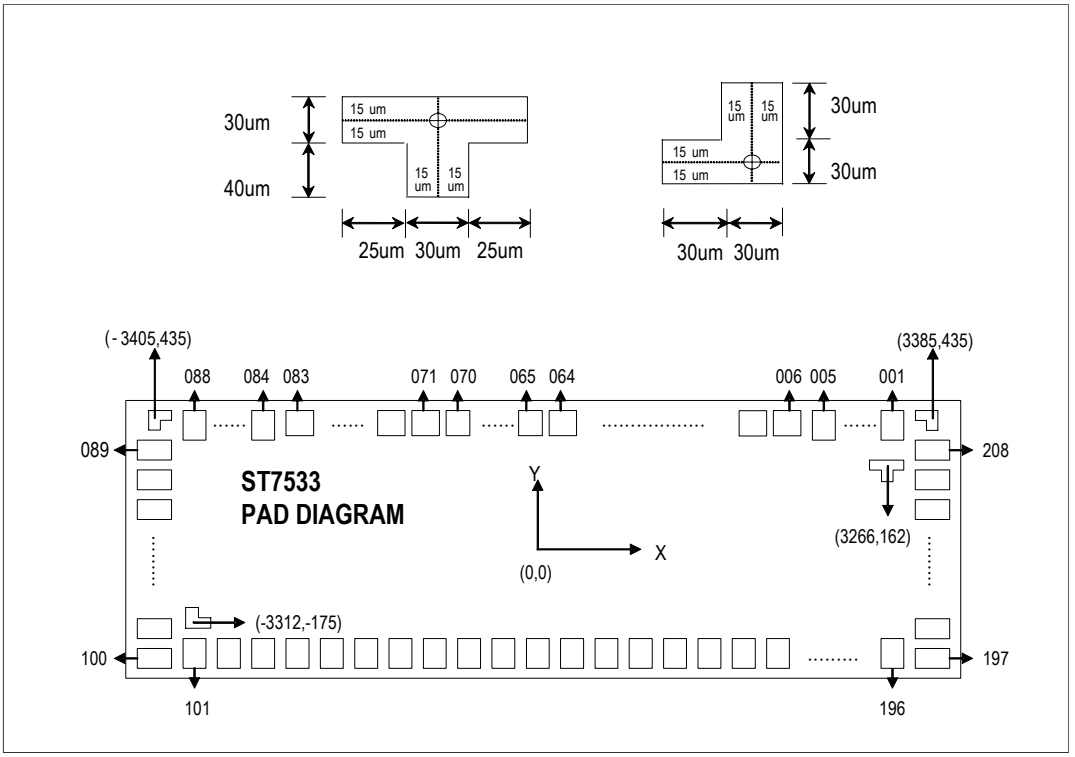
PART NO.	VRS temperature gradient	VRS range
ST7533	-0.15%/°C	-2.1V ±0.03V

3. ST7533 Pad Arrangement

- Chip Size: 7240μm x 1,000 μm
- Origin: Chip Center
- Bump Pitch: 69.1μm(Min.)
- Bump Size:

PAD No. 001 ~ 005	49.1μm x 70.5μm
PAD No. 006 ~ 064	56μm x 60μm
PAD No. 065 ~ 070	51μm x 60μm
PAD No. 071 ~ 083	56μm x 60μm
PAD No. 084 ~ 088	49.1μm x 70.5μm
PAD No. 089 ~ 100	70.5μm x 49.1μm
PAD No. 101 ~ 196	49.1μm x 70.5μm
PAD No. 197 ~ 208	70.5μm x 49.1μm

- Bump Height: 18μm(Typ)
- Chip Thickness: 660μm

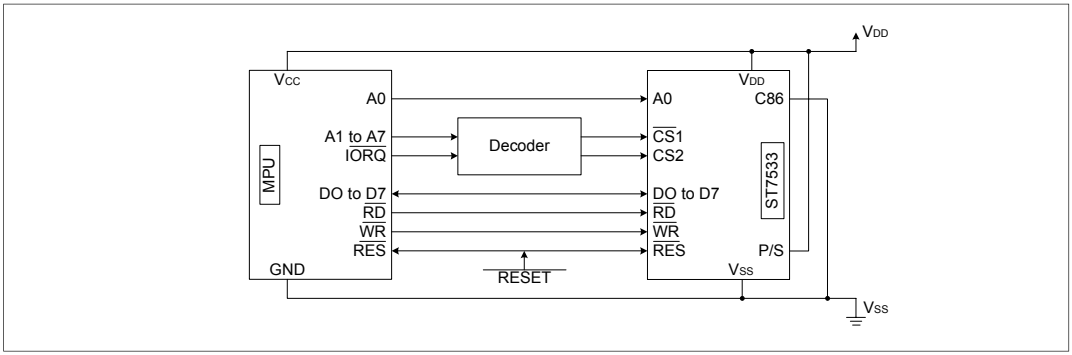


4. The MPU Interface (Reference examples)

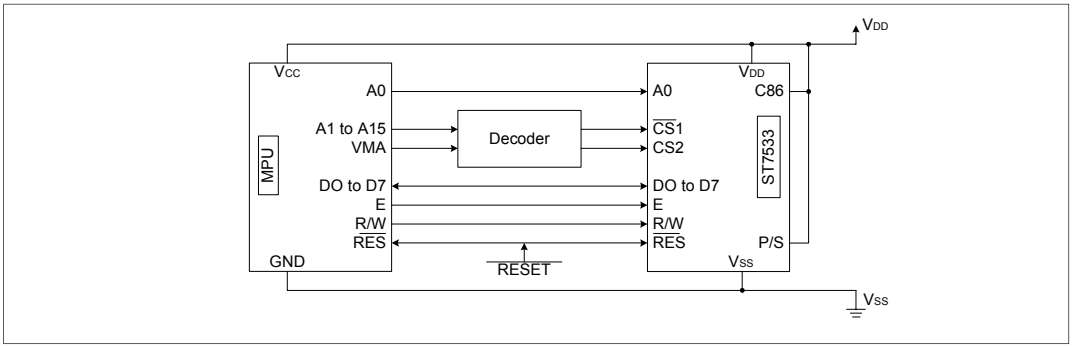
The ST7533 Series can be connected to either 80X86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7533 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7533 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

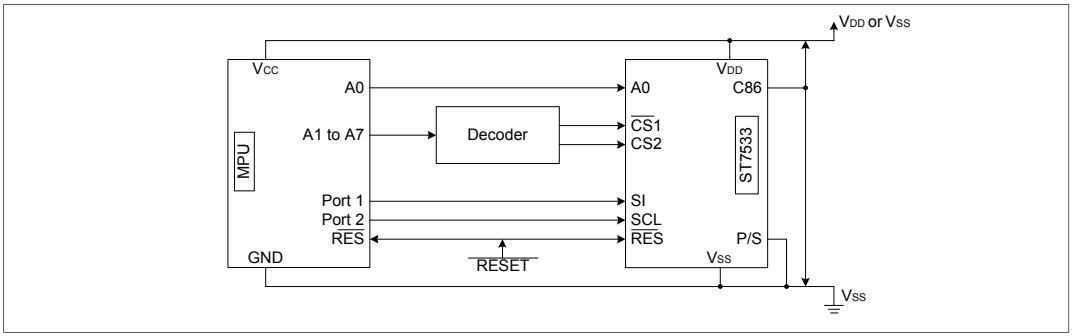
4.1 8080 Series MPUs



4.2 6800 Series MPUs



4.3 Using the Serial Interface

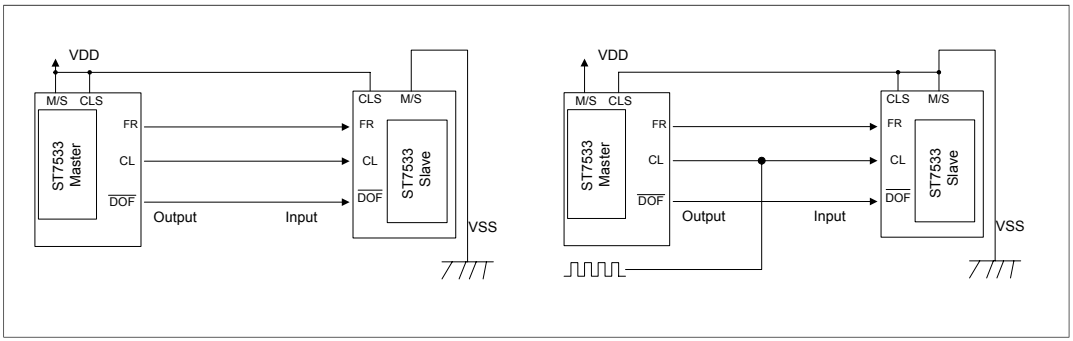


5. Connections Between LCD Drivers (REFERENCE EXAMPLE)

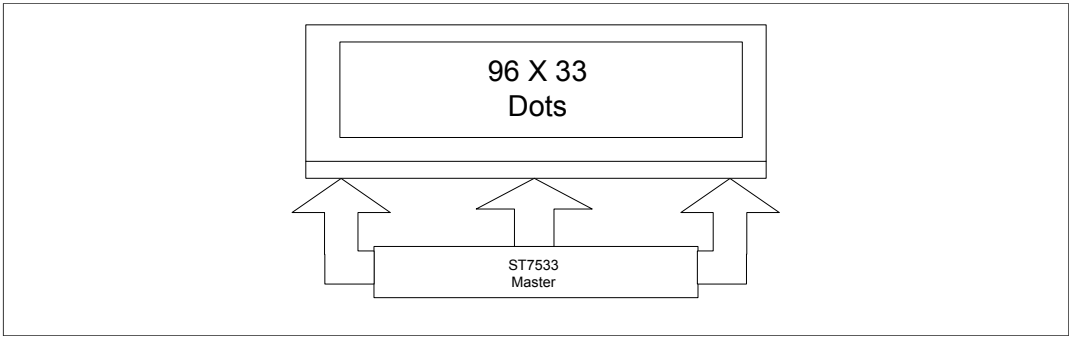
The liquid crystal display area can be enlarged with ease through the use of multiple ST7533 Series chips. Use a same equipment type.

5.1 ST7533 (master)

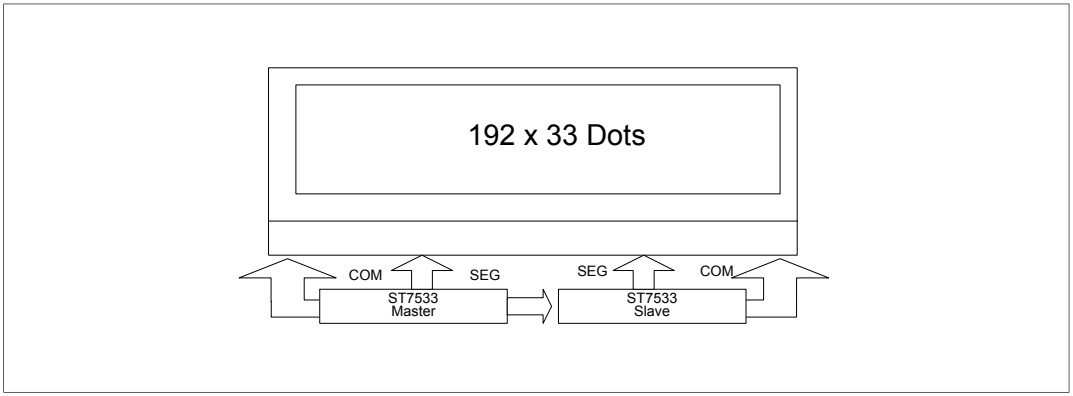
5.2 ST7533 (slave)



5.3 Single-chip Structure



5.4 Double-chip Structure



1. Features

- Direct display of RAM data through the display data RAM.
- RAM capacity : 65 x 132 = 8580 bits
- Display duty selectable by select pin
  - 1/65 duty : 65 common x 132 segment
  - 1/49 duty : 49 common x 132 segment
  - 1/33 duty : 33 common x 132 segment
  - 1/55 duty : 55 common x 132 segment
  - 1/53 duty : 53 common x 132 segment
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs) / Serial interfaces are supported.
- Abundant command functions Display data Read/Write, display ON/OFF, Normal/ Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction selects, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of 2X/3X/4X/5X/6X , where the step-up voltage reference power supply can be input externally).
- High-accuracy voltage adjustment circuit (Thermal gradient -0.05%/°C) V5 voltage regulator resistors equipped internally, V1 to V4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption Operating power when the built-in power supply is used (an example)
  60uA (VDD - VSS = VDD - VSS2 =3.0 V, Quad voltage, V5 - VDD = - 11.0 V).
  Conditions: When displays pattern OFF and the normal mode is selected.
- Power supply operate on the low 1.8 voltage Logic power supply
  VDD - VSS = 1.8V to 3.3 V (+10% Range)
  Boost reference voltage: VDD - VSS2 = 1.8V to 3.3V
  Booster maximum voltage limited
  VOUT= -16.0V (+10% Range)
  Liquid crystal drive power supply:
  VDD - V5 = 4.0V to 13.0 V (ST7565V)
  V0~Vss = 4.0V to 13.0V (ST7565P)
- Wide range of operating temperatures: -40 to 85°C
- CMOS process gold bumped chip or TCP available.
- These chips not designed for resistance to light or resistance to radiation.

2. General Description

The ST7565V/P is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the ST7565V/P contain 65x132 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The ST7565V/P chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65x132 dot display (capable of displaying 8 columnsx4 rows of a 16x16 dot kanji font).

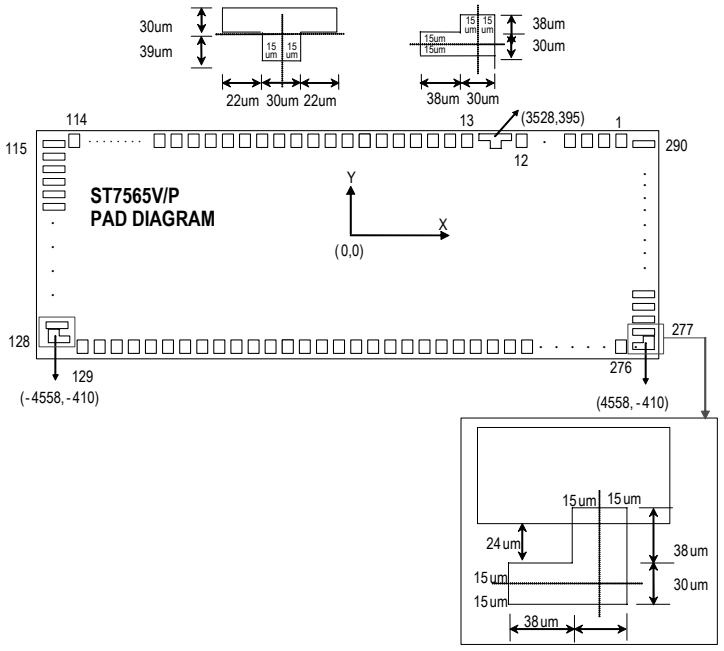
Moreover, the capacity of the display can be extended through the use of master/slave structures between chips. The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, resistors for LCD driver power voltage adjustment and a display clock CR oscillator circuit, the ST7565V/P can be used to create the lowest power display system with the fewest components for high-performance portable devices.

PART NO.	VRS temperature gradient	VRS range
ST7565S	-0.05%/°C	-2.1V ±0.03V

3. ST7565V/P Pad Arrangement (COG)

- Chip Size: 7240μm x 1,000 μm
- Origin: Chip Center
- Bump Pitch: 69.1μm(Min.)
- Bump Size: PAD No. 001 ~ 005 49.1μm x 70.5μm
  PAD No. 006 ~ 064 56μm x 60μm
  PAD No. 065 ~ 070 51μm x 60μm
  PAD No. 071 ~ 083 56μm x 60μm
  PAD No. 084 ~ 088 49.1μm x 70.5μm
  PAD No. 089 ~ 100 70.5μm x 49.1μm
  PAD No. 101 ~ 196 49.1μm x 70.5μm
  PAD No. 197 ~ 208 70.5μm x 49.1μm
- Bump Height: 18μm(Typ)
- Chip Thickness: 660μm

- VOUT maximum - 16V (+10% Range)
- Logic power supply VDD – VSS = 1.8V to 3.3 V (+10% Range)
- Add new booster ratio 5 times and 6 times
- Use select pin to define display duty as following table

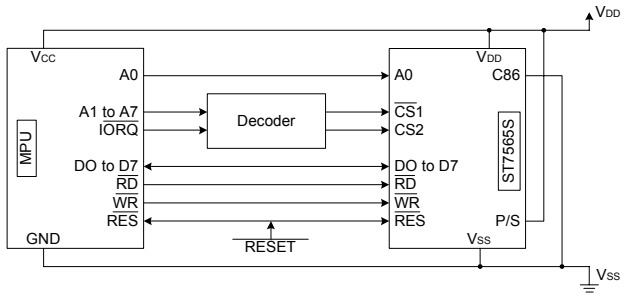


4. The MPU Interface (Reference examples)

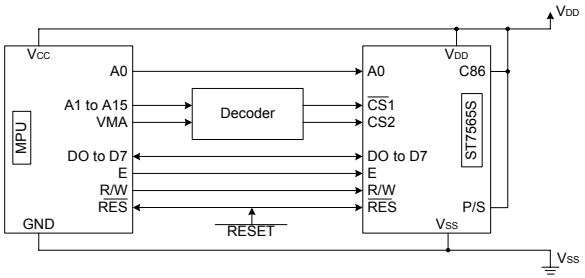
The ST7565V/P Series can be connected to either 80X86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7565V/P series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7565V/P Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

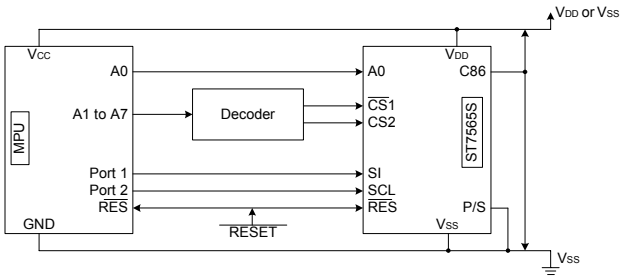
4.1 8080 Series MPUs



4.2 6800 Series MPUs



4.3 Using the Serial Interface

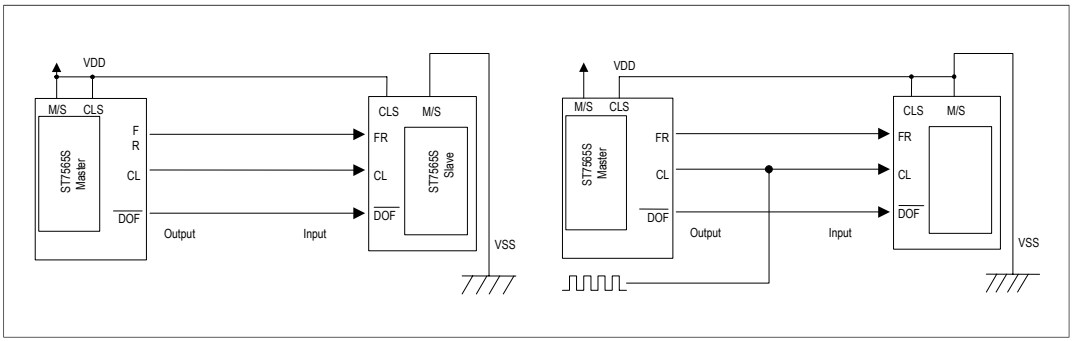


5. Connections Between LCD Drivers (Reference Examples)

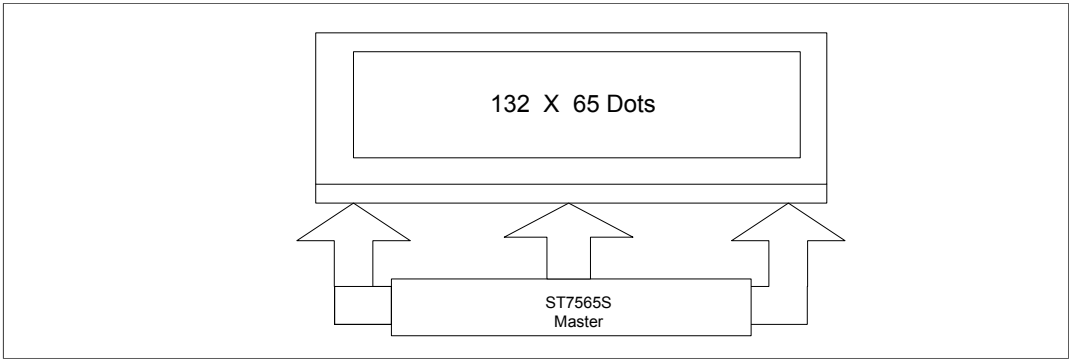
The liquid crystal display area can be enlarged with ease through the use of multiple ST7565V/P Series chips. Use a same equipment type.

5.1 ST7565V/P (master)

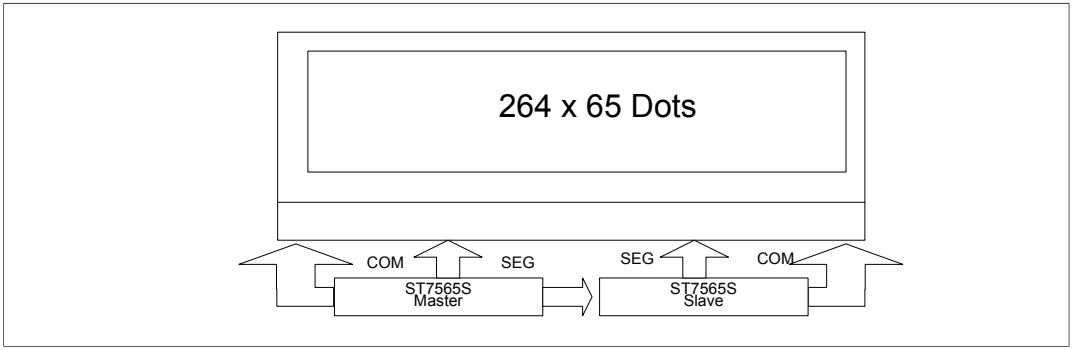
5.2 ST7565V/P (slave)



5.3 Single-chip Structure



5.4 Double-chip Structure



1.General Description

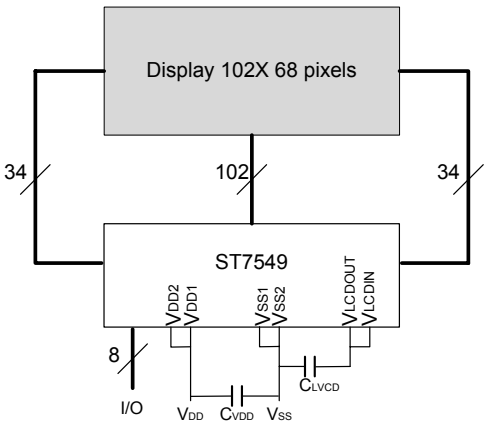
The ST7549 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102 segment and 68 common driver circuits. This chip is connected directly to a microprocessor, accepts 3-line or 4-line serial peripheral interface (SPI)、2-line serial interface or 8-bit parallel interface, display data can stores in an on-chip display data RAM of 68 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. Features

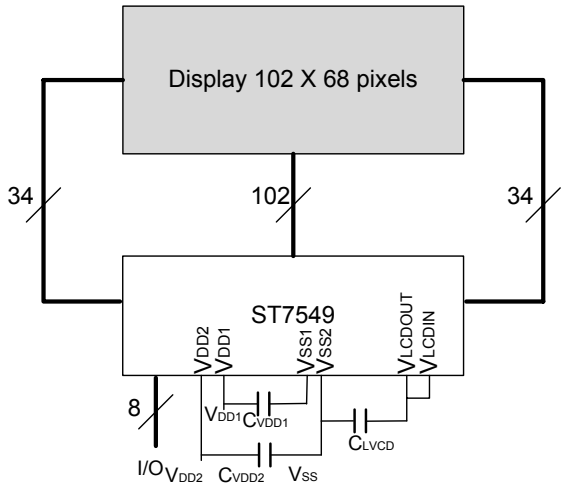
- Single-chip LCD controller & driver
- Driver Output Circuits
- 102 segment outputs / 68 common outputs
- On-chip Display Data ram
  - Capacity: 68X102=6,936 bits
- Microprocessor Interface
  - 8-bit parallel bi-directional interface with 6800-series or 8080-series
  - 4-line SPI (serial peripheral interface) available (only write operation)
  - 3-line SPI (serial peripheral interface) available
  - 2-line Interface (Inter-Integrated Circuit) Interface
- i^2C interface available (ST7548i)
- On-chip Low Power Analog Circuit
  - Generation of LCD supply voltage (externally Vout voltage supply is possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
  - Voltage converter (x4, x5)
  - Voltage regulator
  - Voltage follower
  - On-chip electronic contrast control function (128 steps)
- External RESB (reset) pin
- Logic supply voltage range VDD1,2 -VSS
  - 1.7 to 3.3V
- Display supply voltage range VLCD -VSS
  - 4.5 to 13V
- Temperature range: -40 to +85 degree

3.Application Diagram

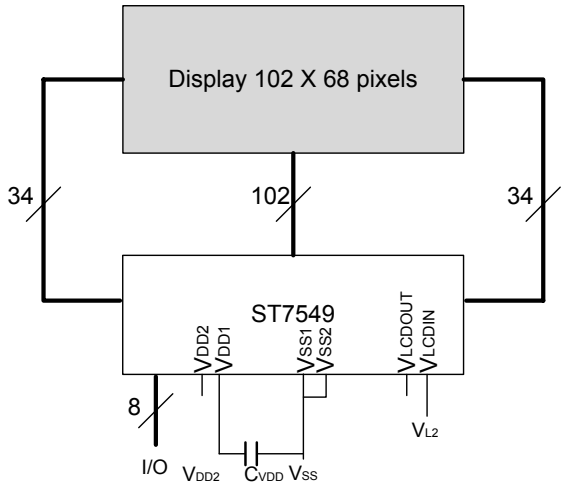
Application diagram: internal charge pump is used and single V_{DD}



Application diagram: Internal charge pump is used and two separate V_{DD1}(V_{DD2})



application diagram : External high voltage generation is used



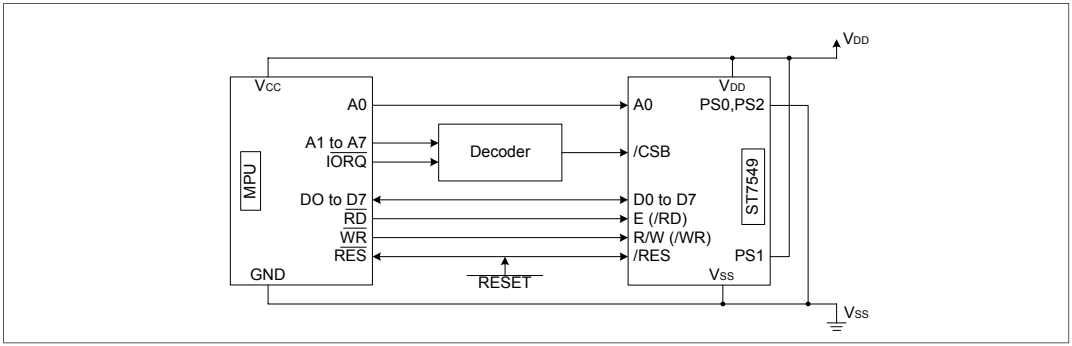
The required minimum value for the external capacitors in an application with the ST7548 are:
C_{VLCD} = min. 100nF $C_{VDD1,2}$= min. 1.0 μF
Higher capacitor values are recommended for ripple reduction.

4.The MPU Interface (Reference Examples)

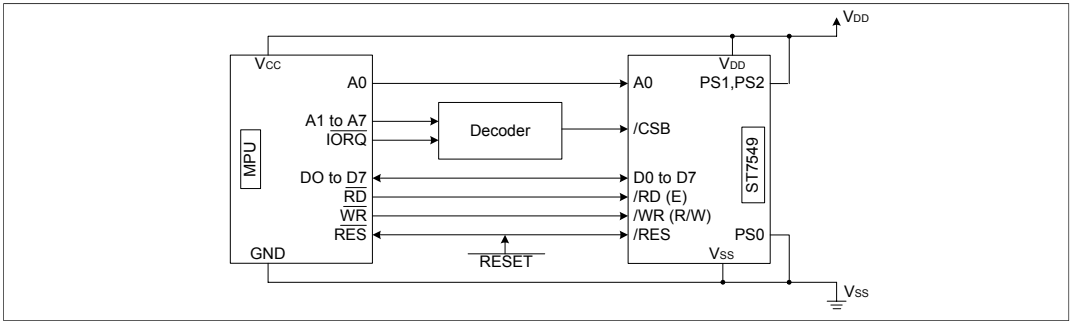
The ST7549 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7549 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7549 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

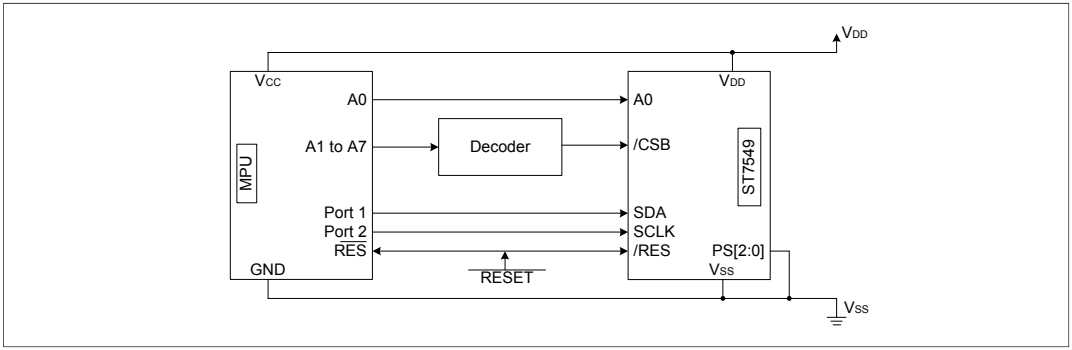
4.1 8080 Series MPUs



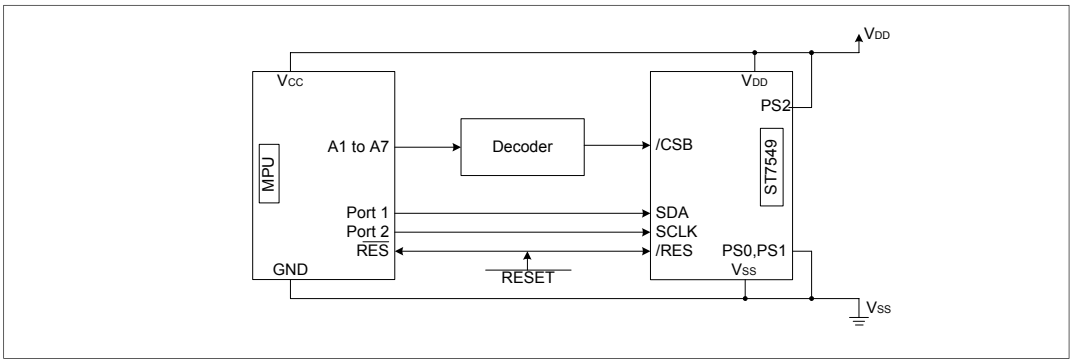
4.2 6800 Series MPUs



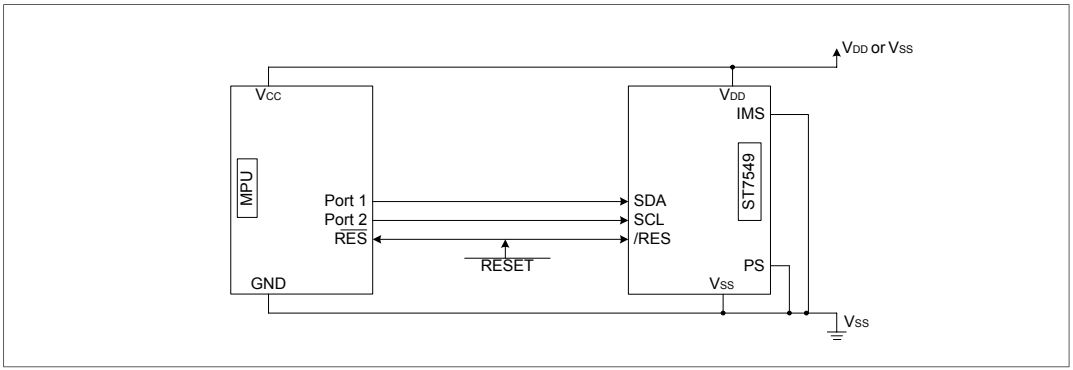
4.3 Using the Serial Interface (4– line interface)



4.4 Using the Serial Interface (3– line interface)



4.5 Using the Serial Interface (2– line interface)



1.General Description

The ST7568 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 102 segment and 68 common driver circuits. This chip is connected directly to a microprocessor, accepts 4-line serial interface(SPI) 、2-line serial interface or 8-bit parallel interface, display data can stores in an on-chip display data RAM of 68 x 102 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. Features

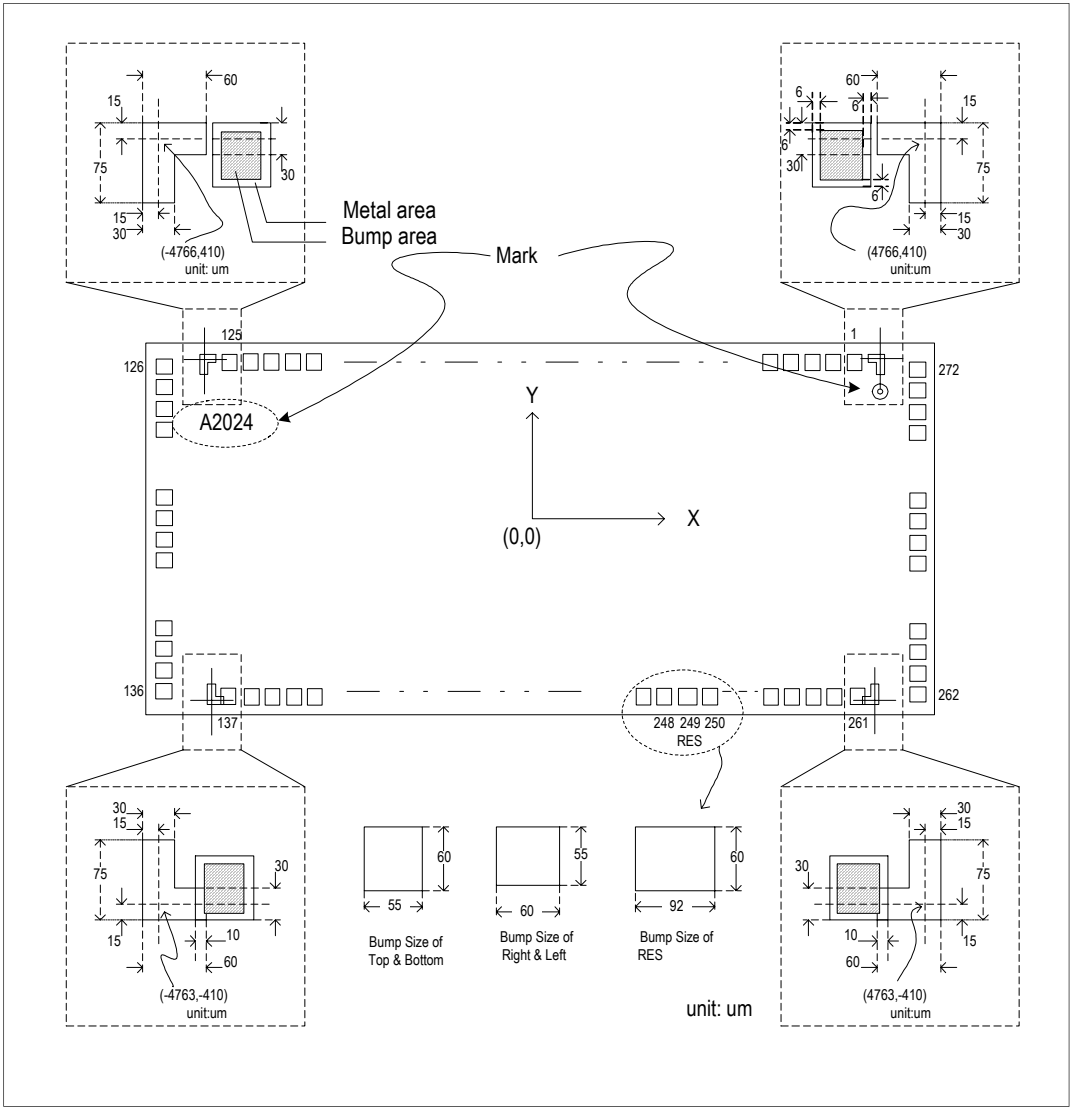
Single chip LCD controller/driver for 4 GRAY SCALE STN LCD

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM and FRC Methods

- Driver Output Circuits
  102 segment outputs / 68 common outputs
- On-chip Display Data ram
  - Capacity: 68X102X2=13,872 bits
  - Bit data " 11 ": a dot of display is illuminated in dark mode.
  - Bit data " 10 ": a dot of display is not illuminated in dark gray mode.
  - Bit data " 01 ": a dot of display is not illuminated in light gray mode.
  - Bit data " 00 ": a dot of display is not illuminated in white mode.
- Microprocessor Interface
  - 8-bit parallel bi-directional interface with 6800-series or 8080-series
  - 4-line SPI (serial peripheral interface) available (only write operation)
  - 2-line Interface (Inter-Integrated Circuit) Interface
  - i^2C interface available (ST7568i)
- On-chip Low Power Analog Circuit
  - Generation of LCD supply voltage (externally Vout voltage supply is possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
  - Voltage converter (x2, x3, x4, x5)
  - Voltage regulator
  - Voltage follower
  - On-chip electronic contrast control function (128 steps)
- External RESB (reset) pin
- Logic supply voltage range VDD -VSS
  - 1.7 to 3.3V
- Temperature range: -40 to +85 degree
- Gold bumped chip available

3. ST7568 Pad Arrangement (COG)

- Chip Size: 10,220 um × 1000 um
- Bump Pitch: PAD NO 1 ~ 148 , 250 ~ 272 : 75.5 um (com/seg)
- PAD NO 149 ~ 248 : 75 um (I/O) PAD NO 148 ~ 149 : 114 um
- PAD NO 248 ~ 249 : 93.5 um (Reset)
- PAD NO 249 ~ 250 : 95.9 um (Reset)
- Bump Size:PAD NO 1 ~ 125 , 137 ~ 248 , 250 ~ 261 : 55(x) um × 60(y) um
- PAD NO 249 : 92(x) um × 60(y) um
- PAD NO 126 ~ 136 , 262 ~ 272 : 60(x)um × 55(y) um
- Bump Height: 18 um (Typ)
- Chip Thickness: 635 um

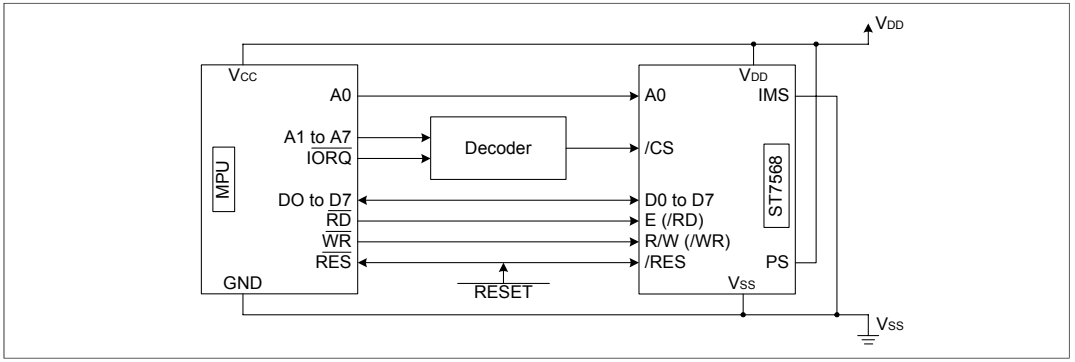


4.The MPU Interface (Reference Examples)

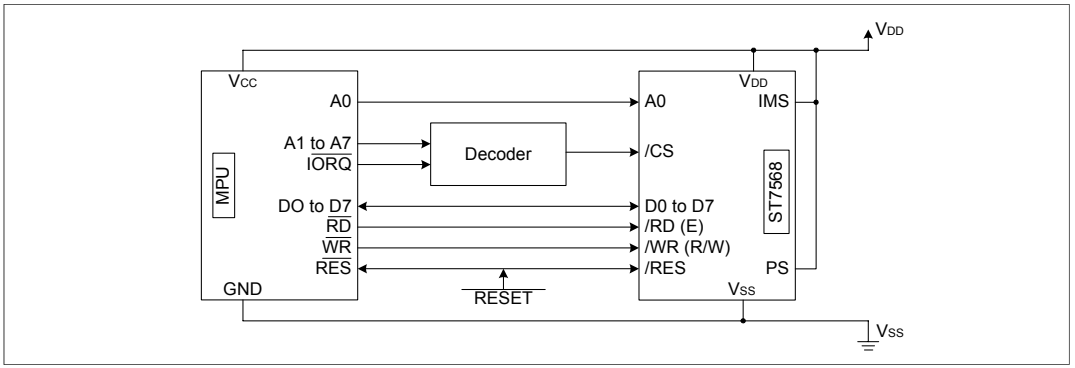
The ST7568 Series can be connected to either60X86 Series MPUs or to 6800Swries MPUs. Moreover, using the serial interface it is possible to operate the ST7568 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7568 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

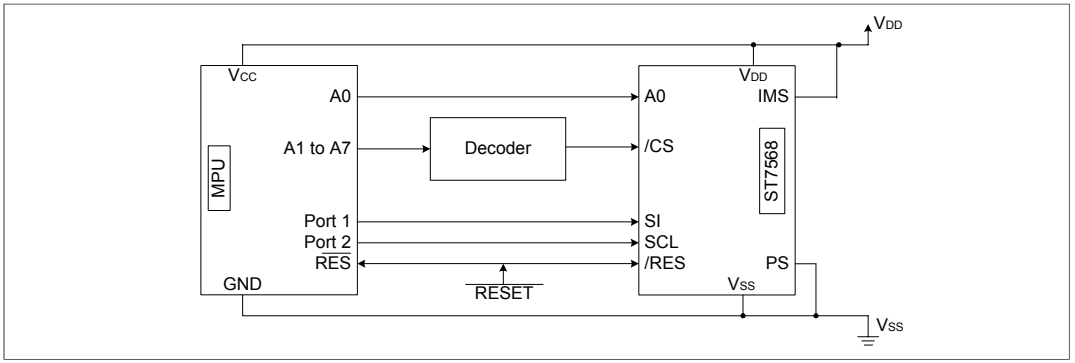
4.1 8080 Series MPUs



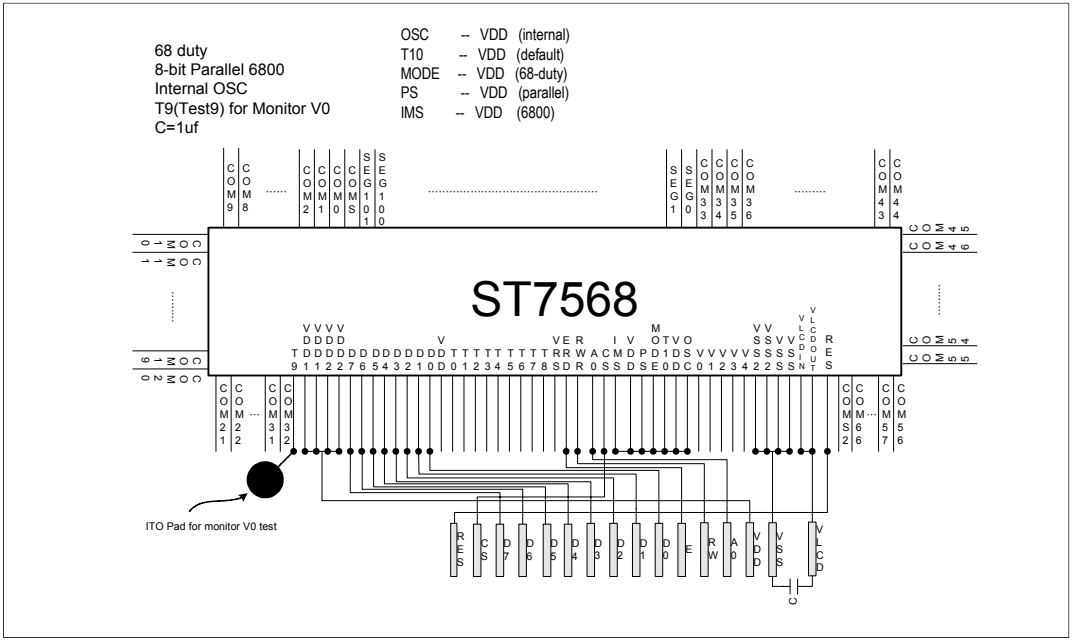
4.2 6800 Series MPUs



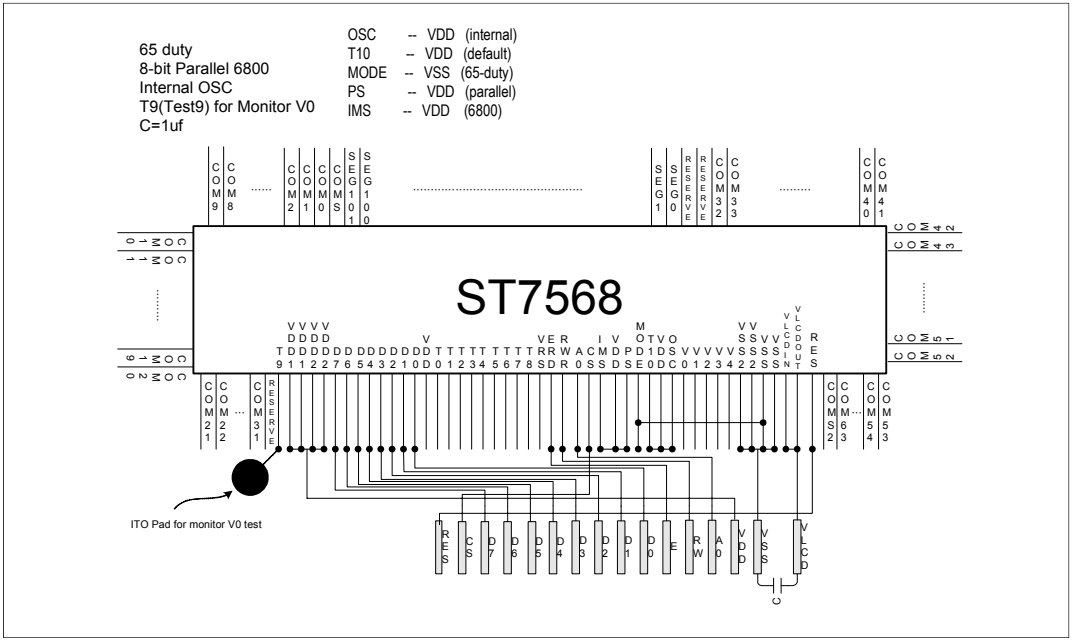
4.3 Using the Serial Interface (4-line interface)



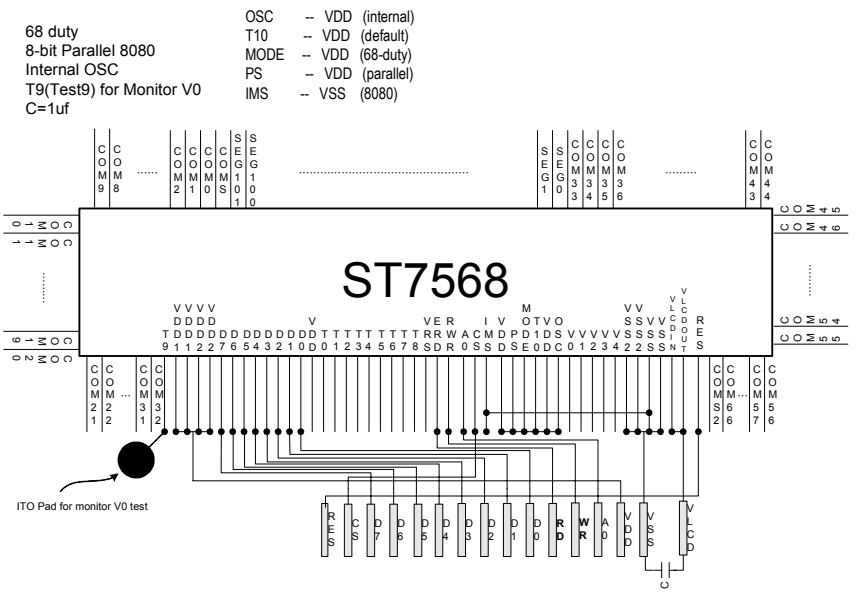
■ 68-duty/parallel-6800/VLCDIN-internal/VDD2=VDD/internal-OSC



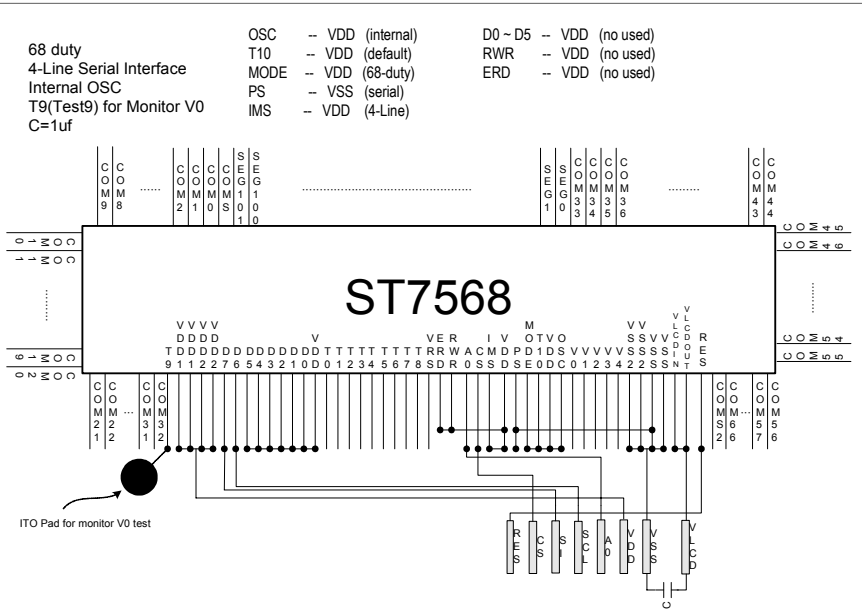
■ 65-duty/parallel-6800/VLCDIN-internal/VDD2=VDD/internal-OSC



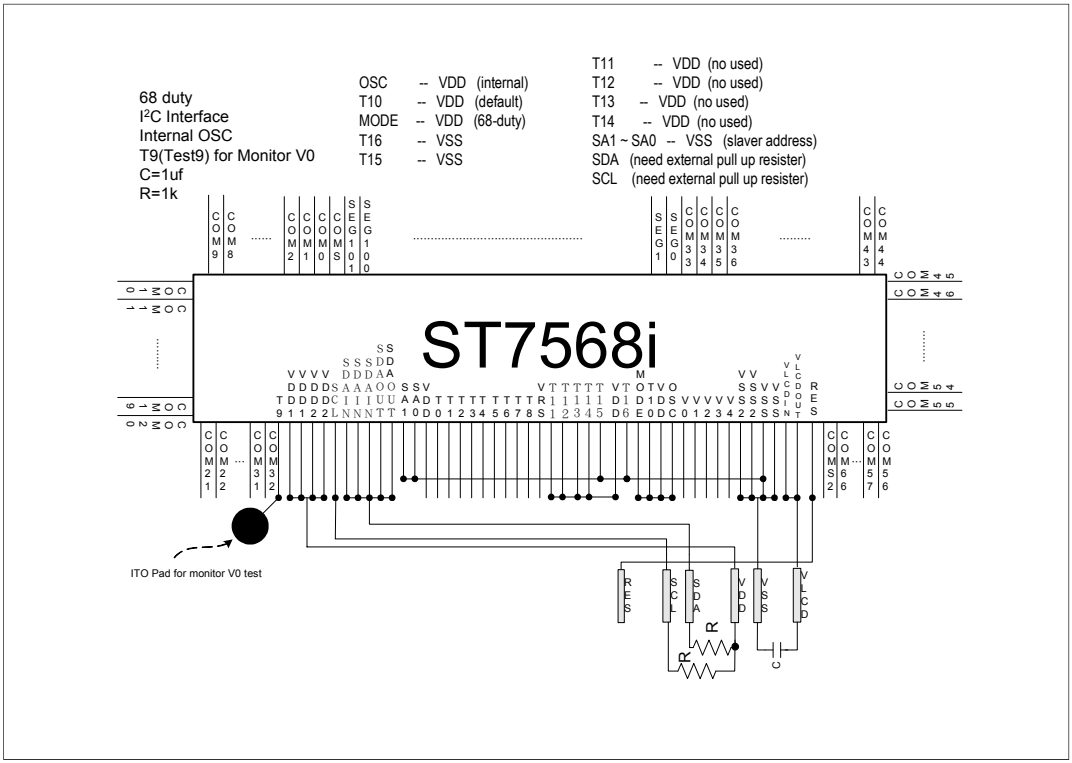
■ 68-duty/parallel-8080/VLCDIN-internalVDD2=VDD/internal-OSC



■ 68-duty/serial-4Line/VLCDIN-internal/VDD2=VDD/internal-OSC



■ 68-duty/ I2C interface /VLCDIN-internal/VDD2=VDD/internal-OSC



1.General Description

The ST7541 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. Features

■ 4-level (White, Light Gray, Dark Gray, Dark) Gray Scale Display with PWM and FRC Methods

DDRAM data [2n : 2n+1]		**Gray Scale**
2n	**2n + 1**	
0	0	White
0	1	Light gray
1	0	Dark gray
1	1	Dark

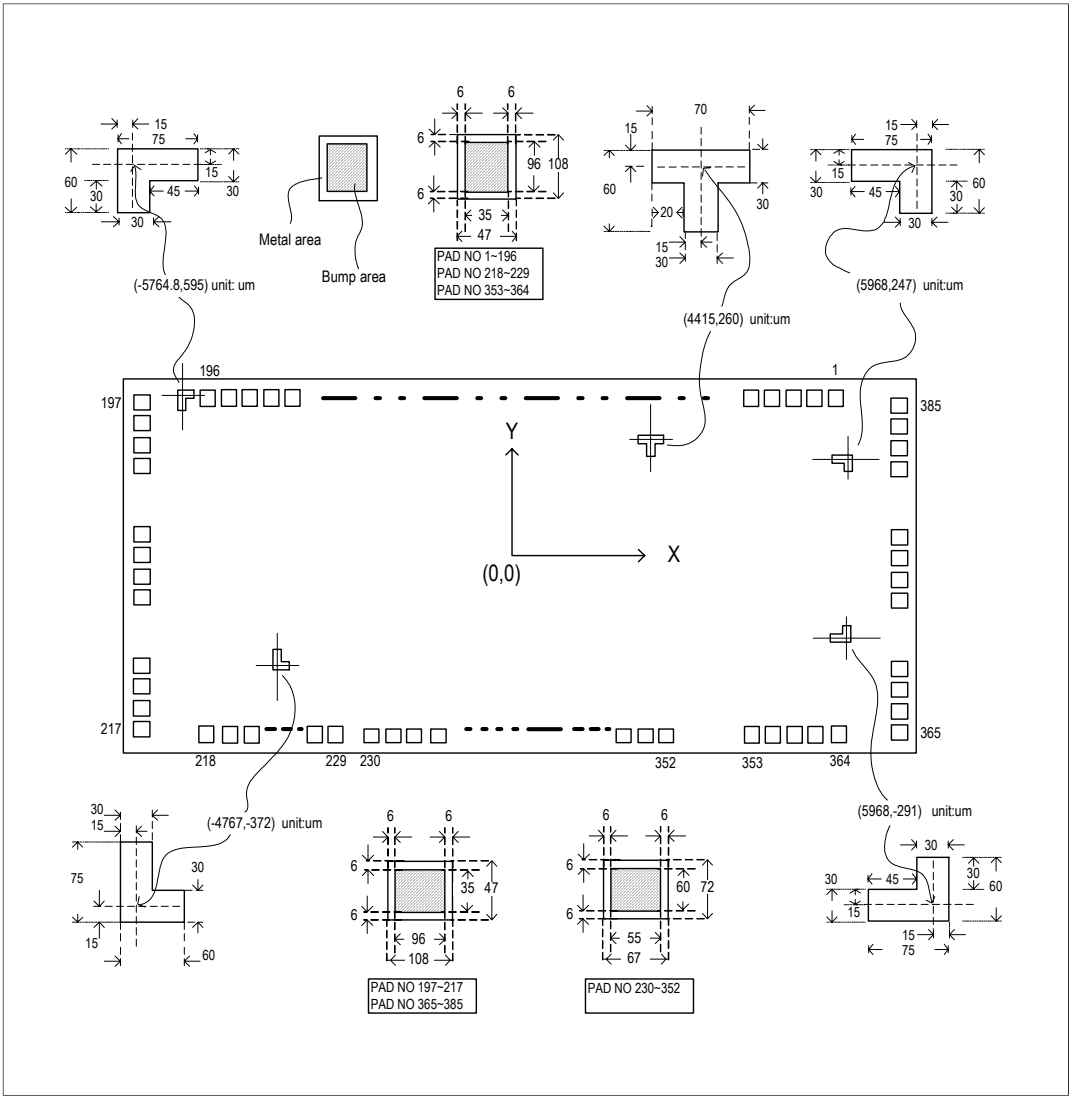
(Accessible column address, n = 0, 1, 2, ……, 125, 126, 127)

■ Driver Output Circuits
■ 128 segment outputs / 128+1 common outputs
■ Applicable Duty Ratios
  - Various partial display
  - Partial window moving & data scrolling
■ On-chip Display Data RAM
  - Capacity: 128 × 129 × 2= 33,024 bits
■ Microprocessor Interface
  - 8-bit parallel bi-directional interface with 6800-series or 8080-series
  - 4-line serial interface (4-line-SIF)
  - 3-line serial interface (3-line-SIF)
  - IIC serial interface
■ On-chip Low Power Analog Circuit
  - On-chip oscillator circuit
  - Voltage converter (x3, x4, x5 or x6)
  - Voltage regulator (temperature coefficient: 0.125%/ C, or external input)
  - On-chip electronic contrast control function (64 steps)
  - Voltage follower (LCD bias : 1/5 to 1/12)
■ Operating Voltage Range
  - Supply voltage (VDD): 1.8 to 3.3V
  - LCD driving voltage (VLCD = V0 - VSS): 4.0 to 15.0 V
■ Package Type
  - Application for COG

ST7541	6800 , 8080 , 4-Line , 3-Line interface (without IIC interface)	Sitronix
ST7541i	IIC interface	I²C BUS

3. ST7541 Pad Arrangement (COG)

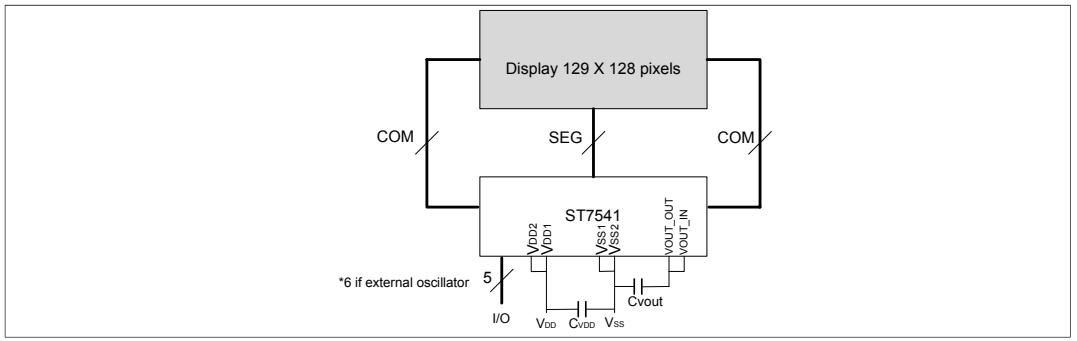
- Chip Size: 12,575 um × 1,220 um
- Bump Pitch:
- PAD NO 1 ~ 229, 353 ~ 385: 55 um (COM/SEG), PAD NO 230 ~ 352: 75 um (I/O),
- PAD NO 229 ~ 230: 84 um, PAD NO 352 ~ 353: 913 um
- Bump Size:
- PAD NO 1 ~ 196, 218 ~ 229, 353 ~ 364 : 35(x) um ×96(y) um PAD NO 197 ~ 217, 365 ~ 385 : 96(x) um ×35(y) um
- PAD NO 230 ~ 352 : 55(x)um ×60(y) um
- Bump Height: 18 um (Typ)
- Chip Thickness: 635 um



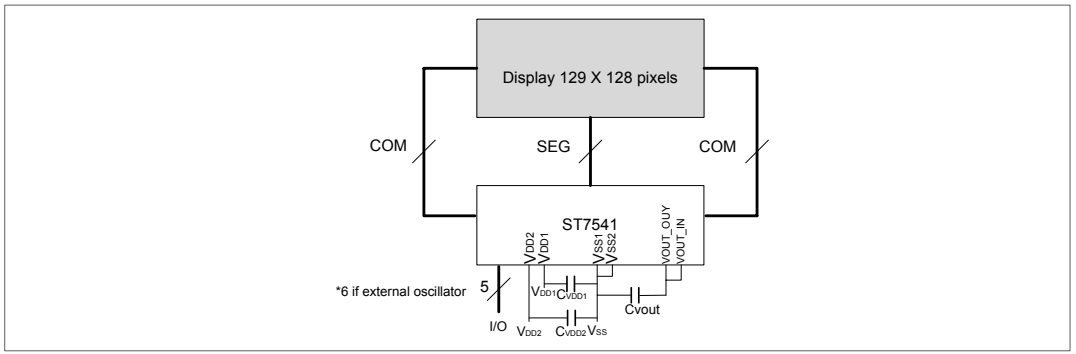
4. Power Pad Connect

The pinning of the ST7541 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 129 X 128 pixels.

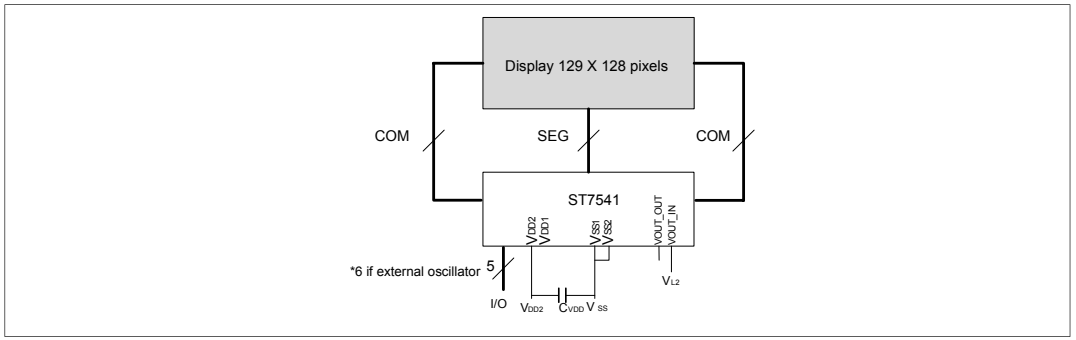
■ Application diagram: internal charge pump is used and s single V_{DD}



■ Application diagram: Internal charge pump is used and two separate V_{DD1}(V_{DD2})



■ application diagram : External high voltage generation is used



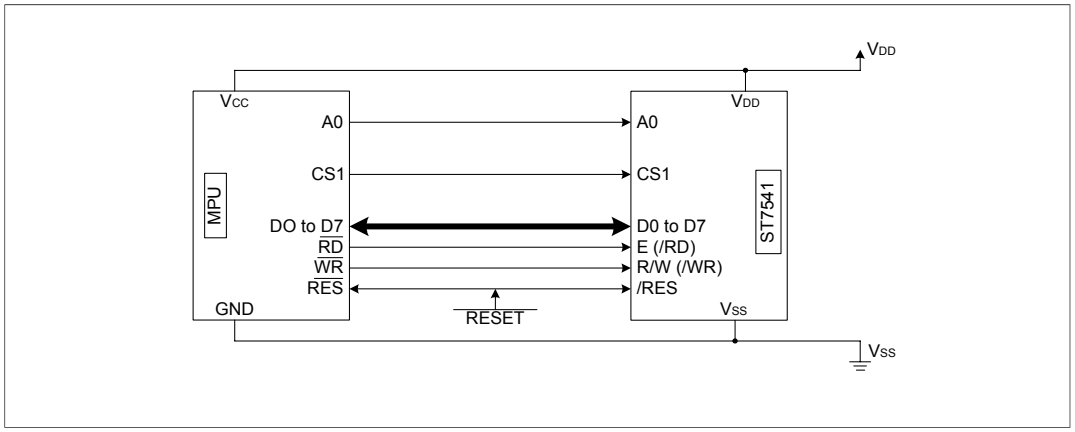
The required minimum value for the external capacitors in an application with the ST7541 are: CVLCD = min. 100nF CVDD1,2= min. 1.0 µF

5. The MPU Interface (Reference Examples)

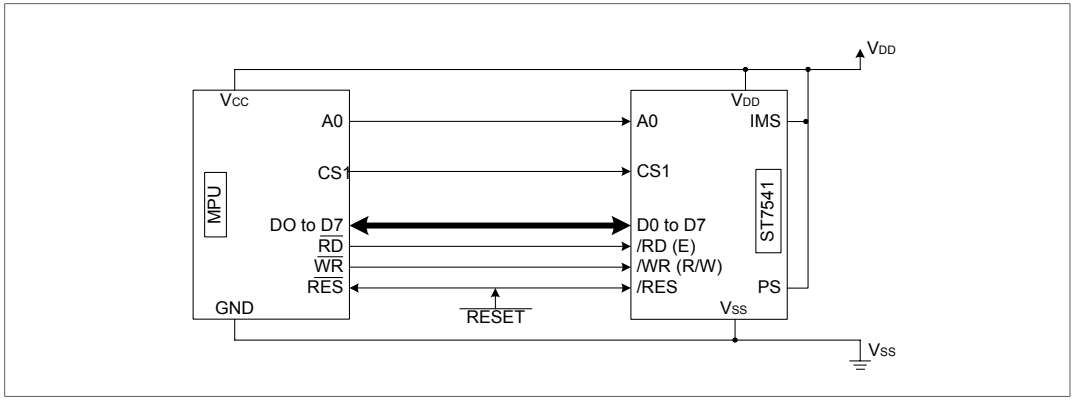
The ST7541 Series can be connected to either60X86 Series MPUs or to 6800Swries MPUs. Moreover, using the serial interface it is possible to operate the ST7541 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7541 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

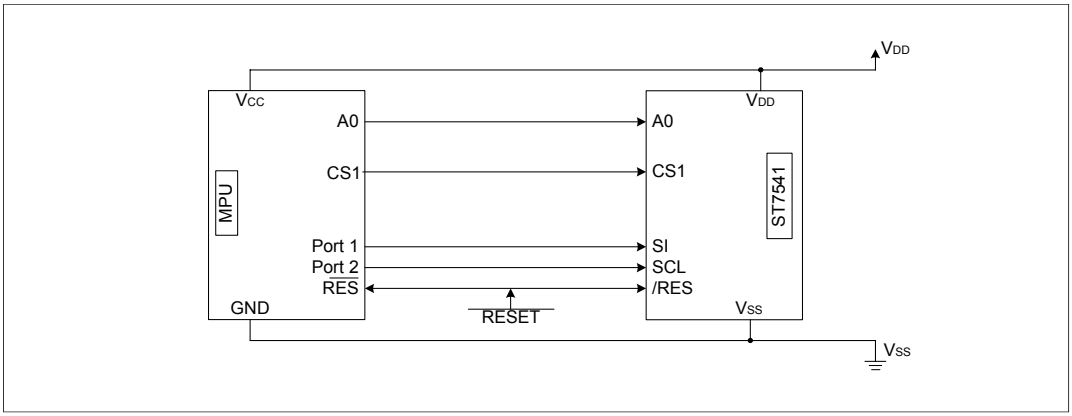
5.1 8080 Series MPUs



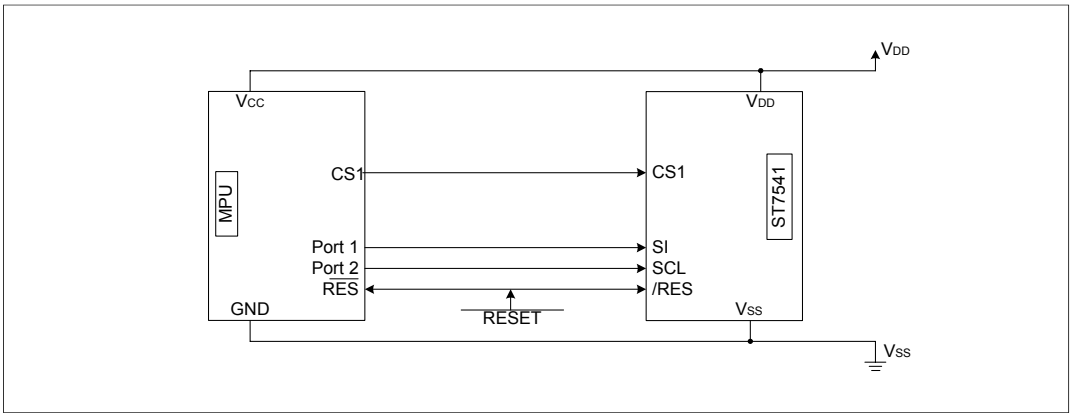
5.2 6800 Series MPUs



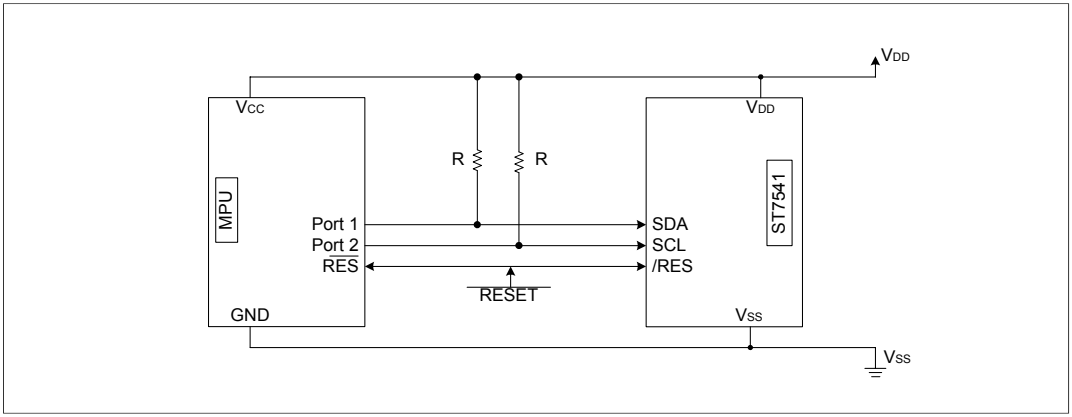
5.3 Using the Serial Interface (4-line interface)



5.4 Using the Serial Interface (3-line interface)



5.5 Using the Serial Interface (IIC interface)



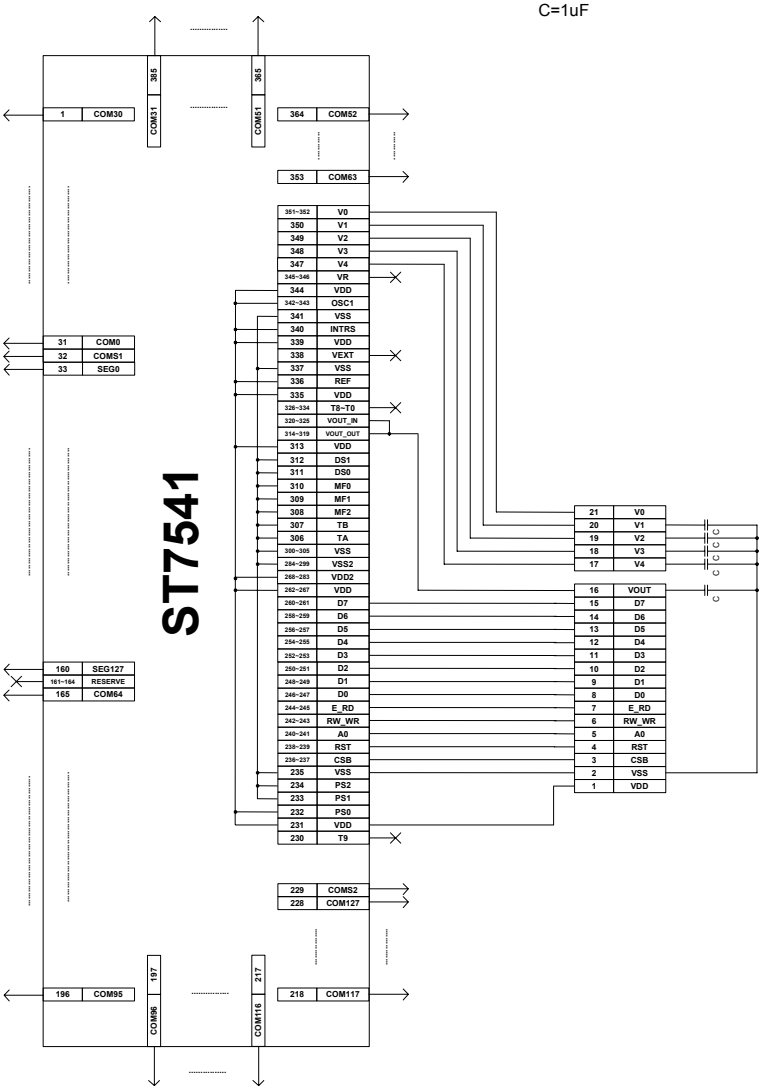
6. ST7541 Application Note

ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface:8080 series
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VDD
PS1:VSS
PS2:VSS
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

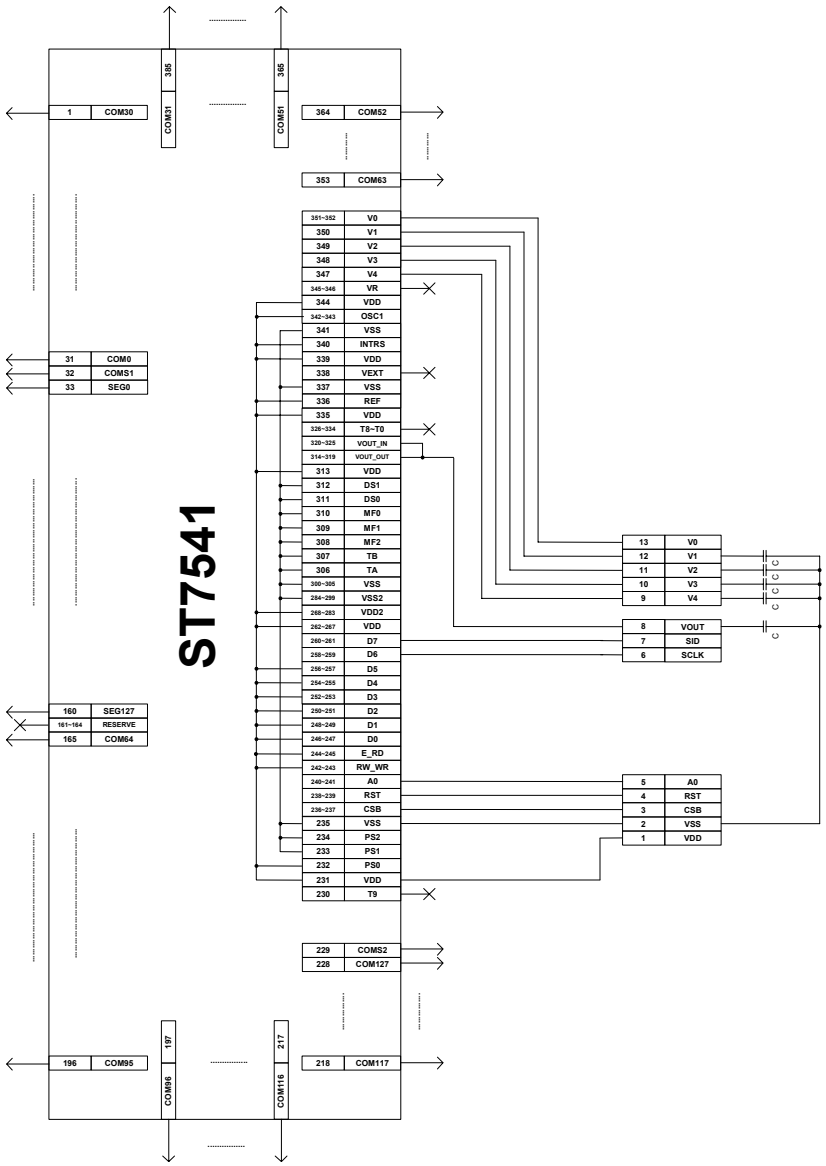


ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface : 4 SPI
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VSS
PS1:VDD
PS2:VSS
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

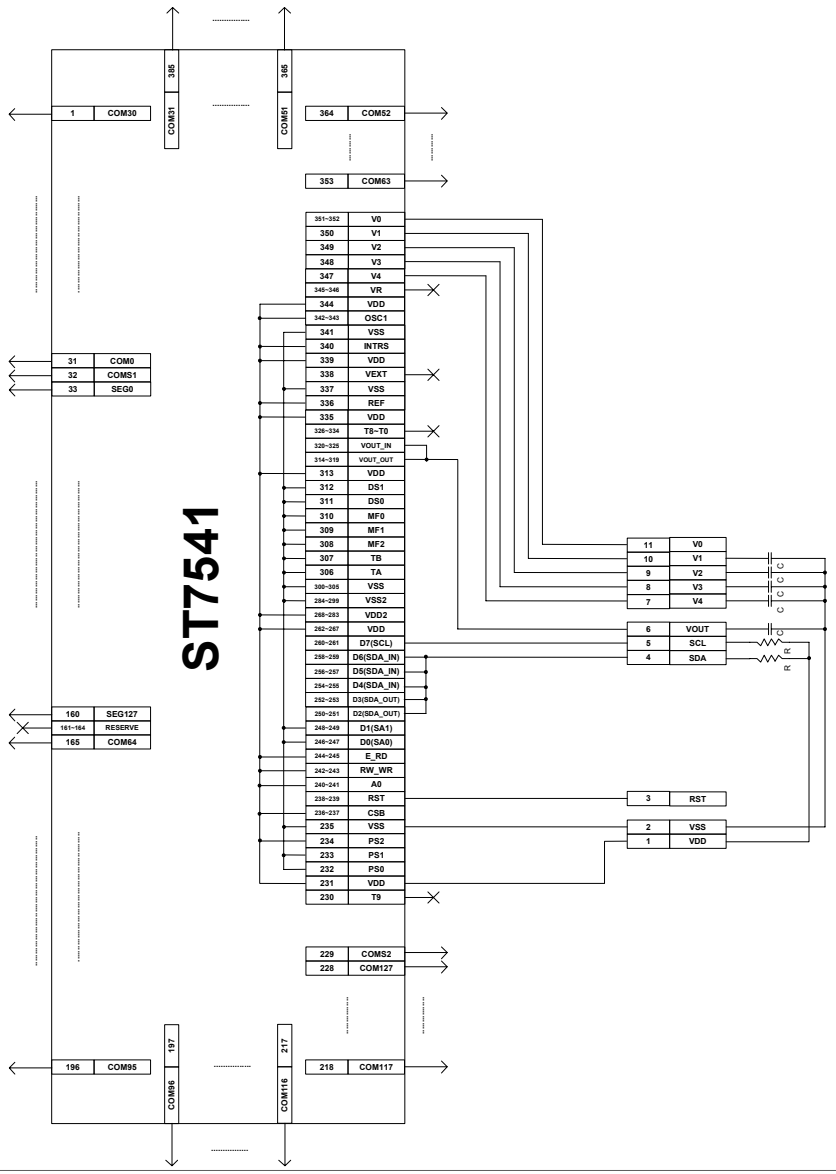


ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface : I2C
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)
SA[1:0]:VDD OR VSS=(0,0)
(SA[1:0] are Slave address of I2C)

PS0:VSS
PS1:VSS
PS2:VDD
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF ; R=10K歐姆

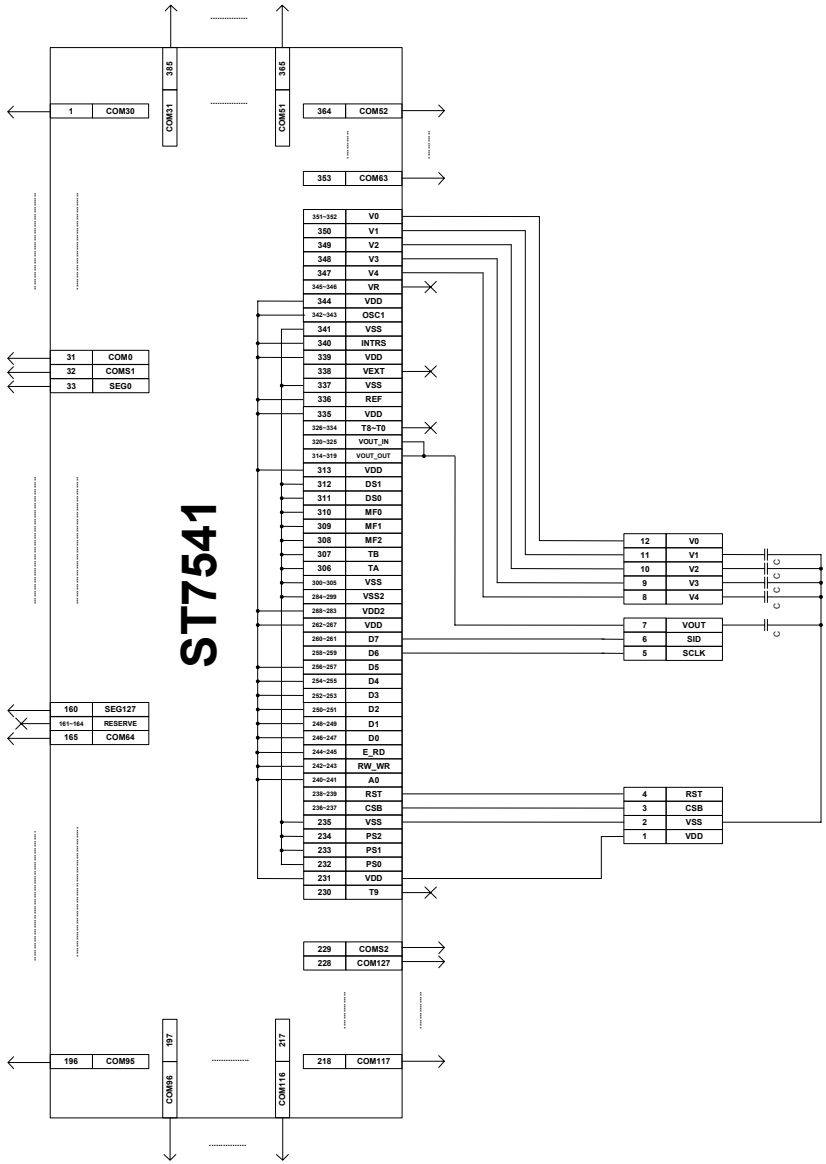


ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface : 3 SPI
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VSS
PS1:VDD
PS2:VSS
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF



1.General Description

The ST7528 is a driver & controller LSI for 16-level gray scale graphic dot-matrix liquid crystal display systems. It contains 2 Mode (160X100,132X128) for Segment and Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI),IIC or 8-bit parallel display data and stores in an on-chip display data RAM of 160 x 129 x 4 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. Features

■ 16-level (White Mode ~ Dark Mode) Gray Scale Display with PWM and FRC Methods

DDRAM data [4n : 4n+3]				**Gray Scale**
4n	**4n + 1**	**4n + 2**	**4n+ 3**	
0	0	0	0	White Mode
0	0	0	1	Gray Level 1
0	0	1	0	Gray Level 2
:	:	:	:	:
:	:	:	:	:
1	1	0	1	Gray Level 13
1	1	1	0	Gray Level 14
1	1	1	1	Dark

- (Mode0: Accessible column address, n = 0, 1, 2, ……, 129, 130, 131)
- (Mode1: Accessible column address, n = 0, 1, 2, ……, 157, 158, 159)

■ Driver Output Circuits
- Mode 0 : 132 segment outputs / 128+1 common outputs (16-level gray scale)
- Mode 1: 160 segment outputs / 100+1 common outputs (16-level gray scale)

■ Applicable Duty Ratios
- Various partial display
- Partial window moving & data scrolling

■ On-chip Display Data RAM
- Capacity: 129 160 4 = 82,560 bits
- 16-Gray Level display dot is illuminated by 4 bit data control

■ Microprocessor Interface
- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line serial interface (4-line-SIF)
- 3-line serial interface (3-line-SIF)
- IIC serial interface

■ On-chip Low Power Analog Circuit
- On-chip oscillator circuit
- Voltage converter (x3, x4, x5 or x6)
- Voltage regulator (temperature coefficient: -0.125%/ C, or external input)
- On-chip electronic contrast control function (64 steps X 8)
- Voltage follower (LCD bias: 1/5 to 1/12)

■ Operating Voltage Range
- Supply voltage (VDD): 1.8 to 3.3V
- LCD driving voltage (VLCD = V0 - VSS): 4.0 to 15.0 V

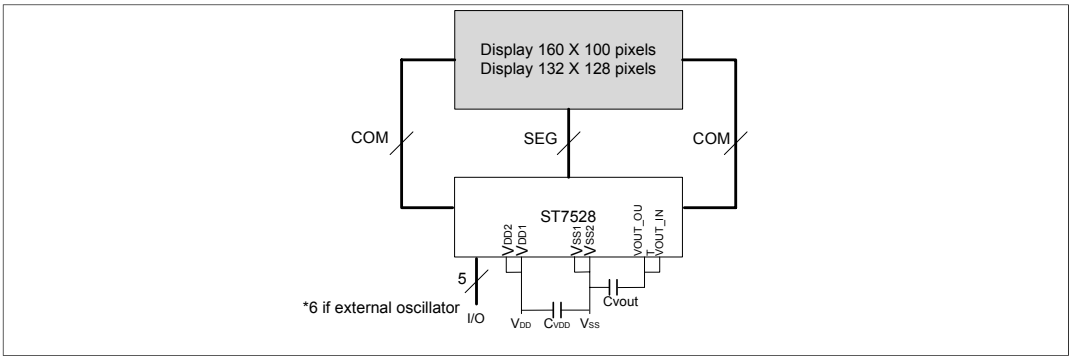
■ Package Type
- Application for COG

ST7528	6800 , 8080 , 4-Line , 3-Line interface (without IIC interface)	Sitronix
ST7528i	IIC interface	I²C BUS

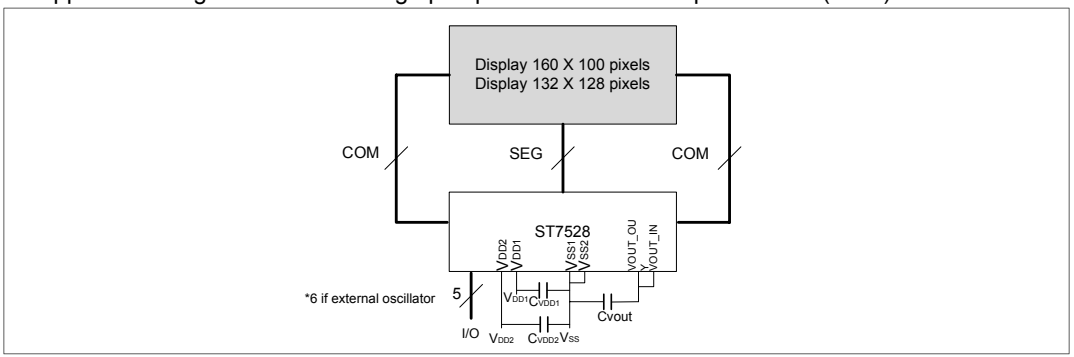
3. Power PAD Connect

The pinning of the ST7528 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 160 X 100 pixels or 132 X 128 pixels.

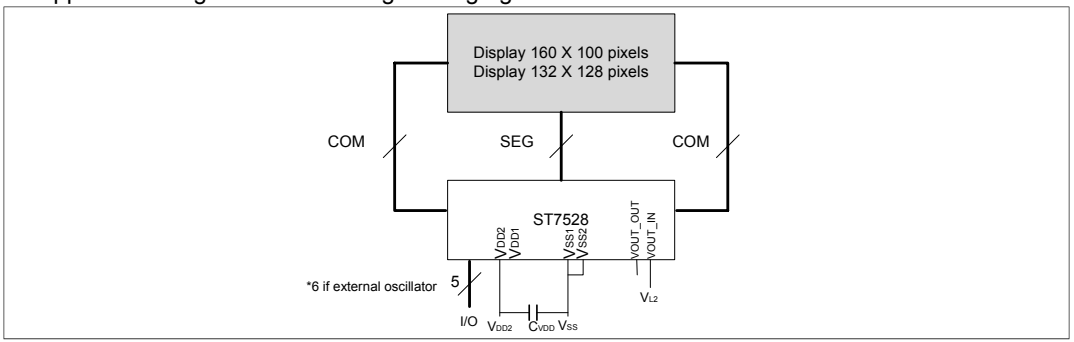
■ Application diagram: internal charge pump is used and s single V_{DD}



■ Application diagram: Internal charge pump is used and two separate V_{DD1}(V_{DD2})



■ Application diagram : External high voltage generation is used



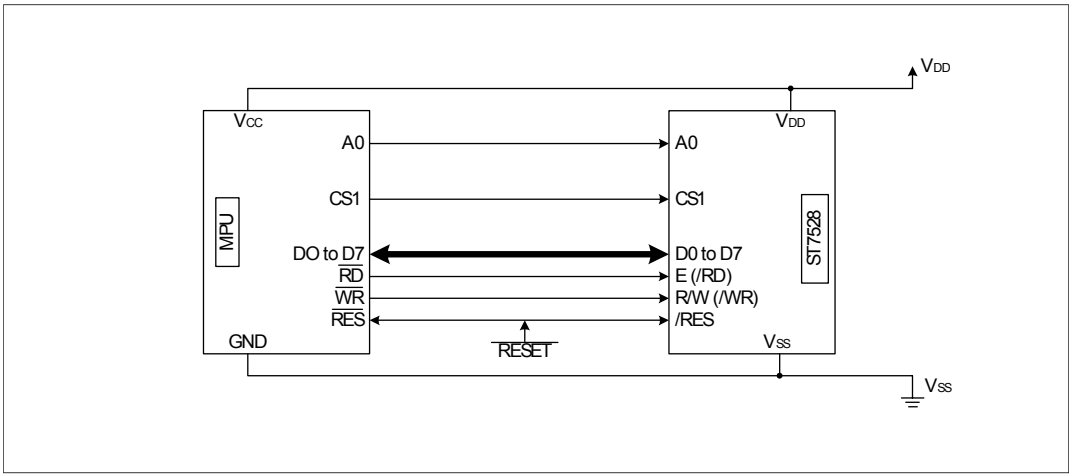
The required minimum value for the external capacitors in an application with the ST7528 are:
CVLCD = min. 100nF CVDD1,2= min. 1.0 µF
Higher capacitor values are recommended for ripple reduction.

4. The MPU Interface (Reference Examples)

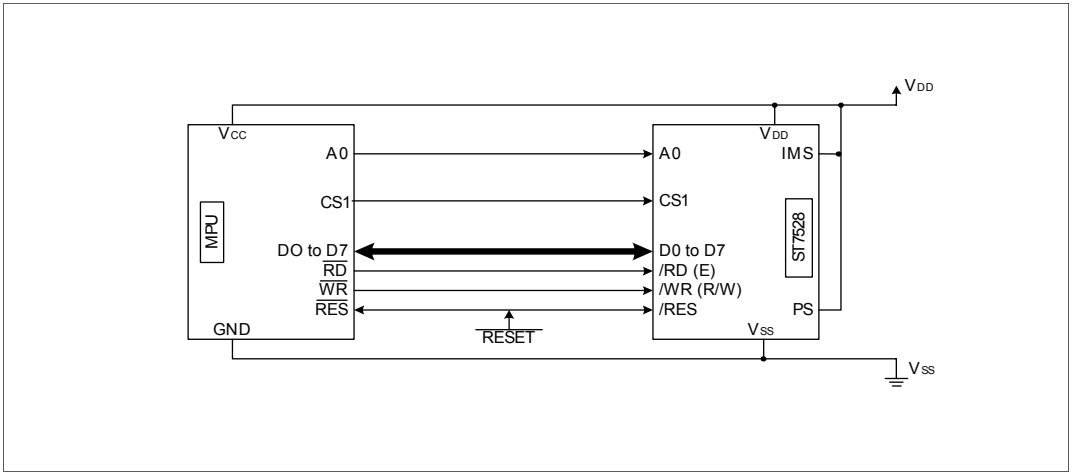
The ST7528 Series can be connected to either60X86 Series MPUs or to 6800Swries MPUs. Moreover, using the serial interface it is possible to operate the ST7528 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7528 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

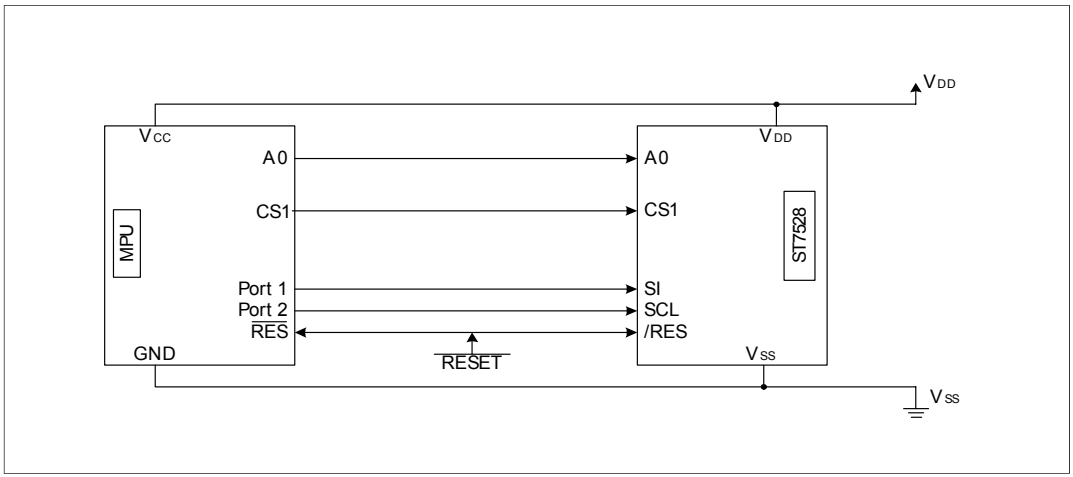
4.1 8080 Series MPUs



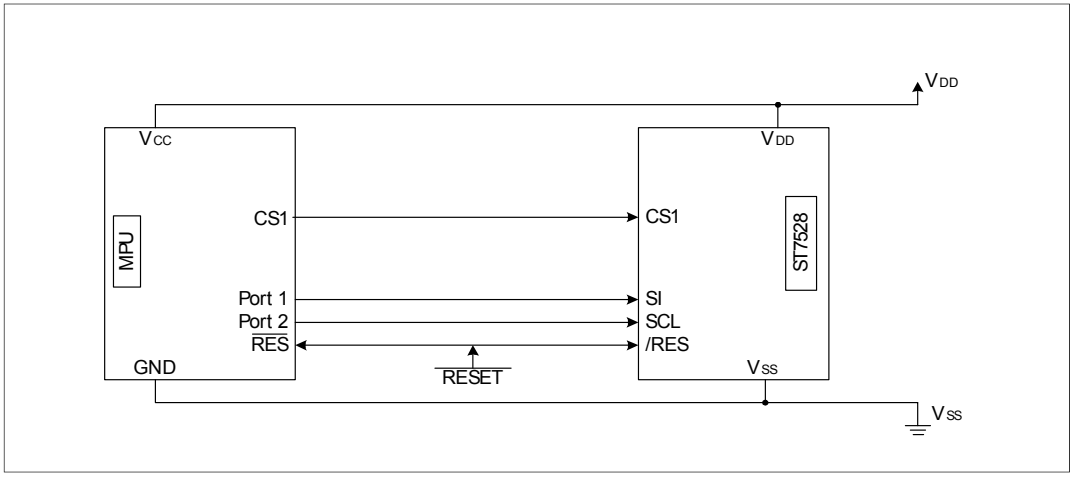
4.2 6800 Series MPUs



4.3 Using the Serial Interface (4-line interface)



4.4 Using the Serial Interface (2-line interface)



1.General Description

The ST7632 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 396 Segment and 132 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. Features

- Driver Output Circuits
  - 396 segment outputs / 132 common outputs
- Applicable Duty Ratios
  - Various partial display
  - Partial window moving & data scrolling
- On-chip Display Data RAM
  - Capacity: 396 132 4 =209,088 bits
  - 256 colors (RGB)=(332) mode
  - 4K colors (RGB)=(444) mode
  - Dithered 65K colors (RGB)=(565) mode
  - Dithered 262K colors (RGB)=(666) mode
  - Dithered 16M colors (RGB)=(888) mode
- Microprocessor Interface
  - 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
  - 4-line serial interface (4-line-SIF)
  - 3-line serial interface (3-line-SIF)
  - IIC serial Interface
- On-chip Low Power Analog Circuit
  - On-chip oscillator circuit
  - Voltage converter (x2, x3, x4, x5, x6, x7, x8)
  - Voltage regulator (with temperature compensation by software setting)
  - On-chip electronic contrast control function (512 steps)
  - Voltage follower (LCD bias: 1/5 to 1/12)
- Operating Voltage Range
  - Supply voltage (VDD, VDD1): 1.7 to 3.6V (VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
  - LCD driving voltage (VLCD = V0 - VSS): 4.5 to 18.0 V
- Temperature measurement circuit
  - On-chip temperature measurement without external component
- LCD driving voltage (EEPROM)
  - To store contrast adjustment value for better display
- Package Type
  - Slim chip for TCP
  - Application for COG

ST7632	6800 , 8080 , 4-Line , 3-Line interface (without IIC interface)	Sitronix
ST7632i	IIC interface	I²C BUS

Sitronix
矽 創 電 子
Sitronix Technology Corp.

This brochure provides an overview of the products and services of LCD DRIVER & MCU ICs.
For further information and queries kindly contact:

Sitronix Marketing & Sales Div.
Phone: +886-2-2659-1276
Fax: +886-2-2658-2554
E-Mail: sales@sitronix.com.tw

Detailed and latest information on our products and services is also accessible via our website:
www.sitronix.com.tw/products

Headerquarter

新竹縣 302 竹北市台元街 20 號 6 樓之 2
6F-2, No. 20, Tai Yuen St., ChuPei City 302,Hsin Chu Hsien, Taiwan
TEL 03-552-6500
FAX 03-552-6501

Taipei

台北市 114 內湖區內湖路一段 308 號 6 樓之 2
6F-2, No. 308, Sec. 1, Neihu Road, Taipei 114, Taiwan
TEL 02-2659-1276
FAX 02-2658-2554

Hong Kong

香港九龍灣臨興街 32 號 美羅中心一期 11 樓 01 室
Flat/Rm1-2, 11/F, Metro Centre Tower 1, No.32, Lam Hing Street, Kowloon Bay, Hong Kong
TEL 852-2953-0854
FAX 852-2953-0254

ShenZhen

深圳市福田區天安創新科技廣場 A 座 1503 室
Room 1503, TianAn Hi-Tech Plaza Tower A, TianAn Cyber Park, FuTian District, ShenZhen
TEL 86-755-8343-9077
FAX 86-755-8343-9711

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