SIGNETICS BIPOLAR MEMORIES

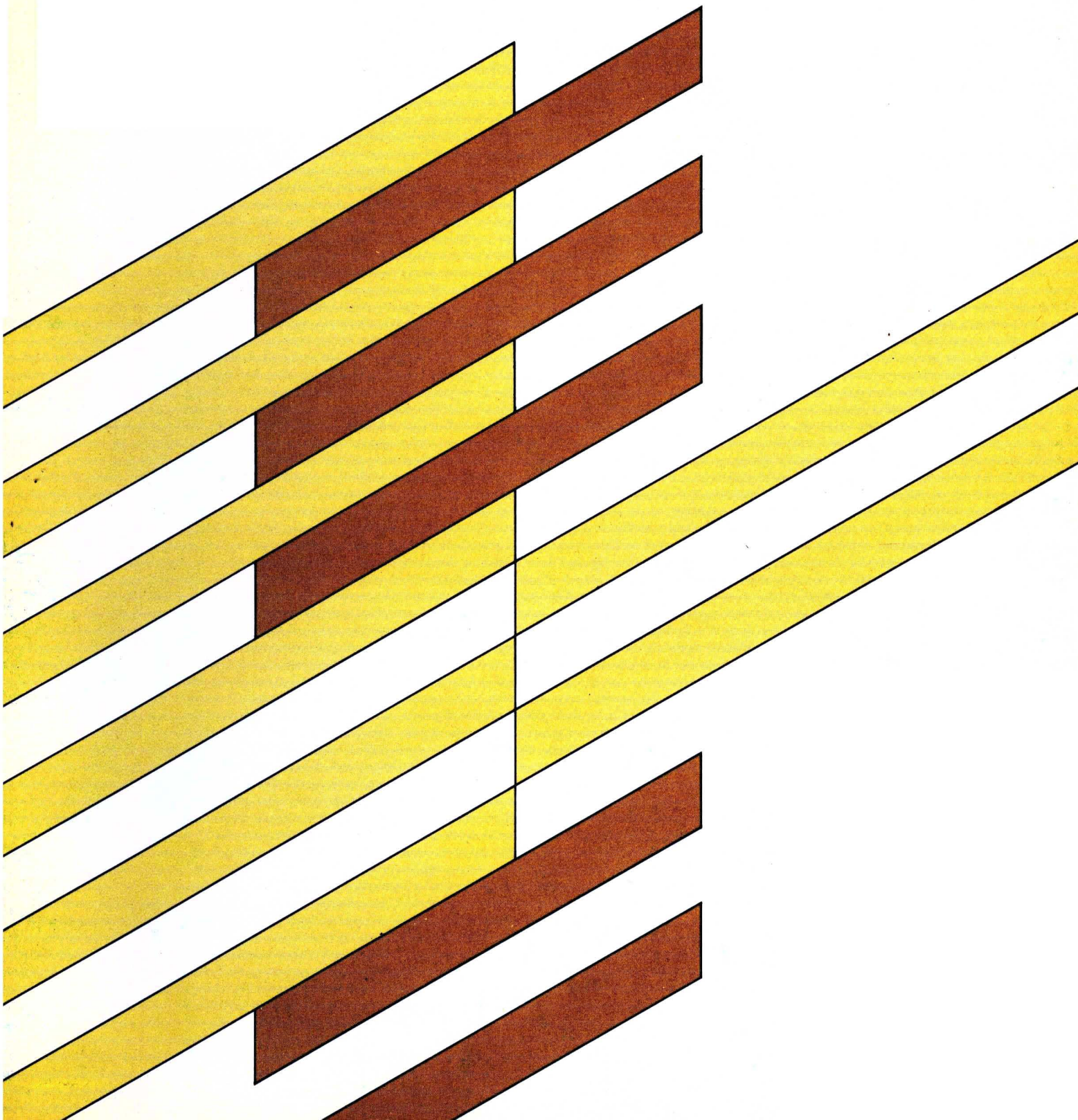


TABLE OF CONTENTS

DESCRIPTION

The 8228 is a 4096 Bit Bipolar Read Only Memory organized as 1024 words by 4 bits per word. Available in a 16 pin dual in-line package, the 8228 can provide very high bit packing density by replacing four standard 256X4 ROMS.

The 8228 is fully TTL compatible and includes on-the-chip decoding. Typical access time is 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N8228I - CB162, while custom circuits are identified as N8228I - CXXX. A truth table/order blank is included on page 4-46 for ordering custom patterns.

See page 4-35 for CB162 Pattern and USASCII Row Character Generator.

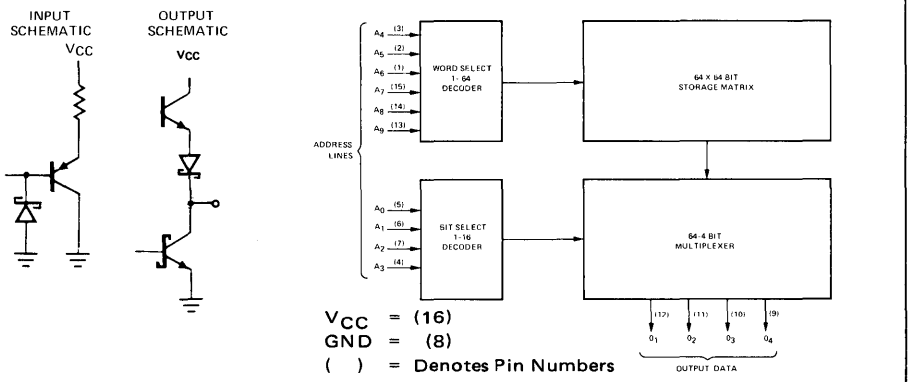
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TOTEM POLE OUTPUTS
- DIODE PROTECTED INPUTS
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)

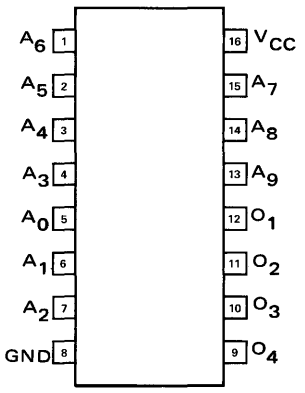
APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATION
CONTROL STORE

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			0.5	V	I_{out} = 11.2 mA	
"1" Output Voltage	2.7			V	I_{out} = -1.0 mA	
"0" Input Current		-10	-400	μA	V_{in} = 0.45V	
"1" Input Current		1	25	μA	V_{in} = 5.5V	
Input Voltage						
"0" Level (V_{IL})			.85	V		
"1" Level (V_{IH})	2.0			V		

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Input Clamp Voltage	−1.2			V	I_{in} = −18mA	
Power Consumption		140	170	mA	O_1 to O_3 = "0"	
Output Short Circuit Current	−20		−70	mA	V_{OUT} = 0 Volts	

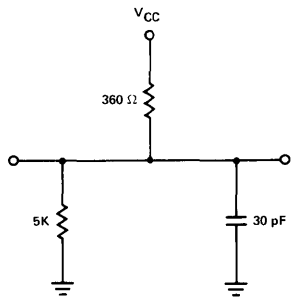
SWITCHING CHARACTERISTICS $0 \leqslant T_A \leqslant 75^oC$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Access Time—Address to Output		50	70	ns		5

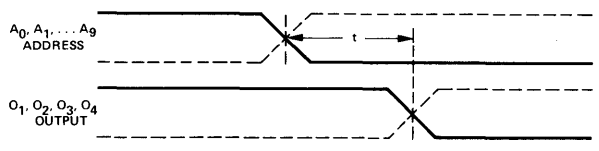
NOTES
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 6.0V. Input currents must not exceed ±30mA. Output currents must not exceed ±100mA. Storage temperature must be between −60°C to +150°C.
5. Rise and fall time for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

AC TEST FIGURE AND WAVEFORM

TEST LOAD



READ CYCLE



DESCRIPTION

The 82S09 is a 576-Bit, Schottky clamped TTL, random access memory, organized as 64X9. This organization allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 is fully TTL compatible, and features open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

During WRITE operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

The 82S09 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S09, I. For the military temperature range (−55°C to +125°C) specify S82S09, I.

FEATURES

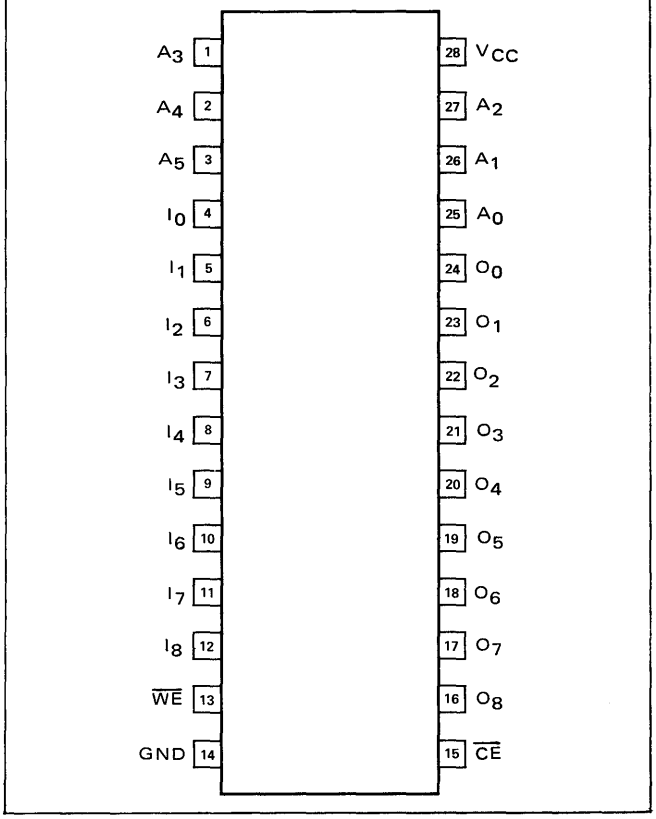
- ORGANIZATION – 64 X 9
- ADDRESS ACCESS TIME:
  - S82S09 – 80ns, MAXIMUM
  - N82S09 – 45ns, MAXIMUM
- WRITE CYCLE TIME:
  - S82S09 – 70ns, MAXIMUM
  - N82S09 – 45ns, MAXIMUM
- POWER DISSIPATION – 1.3mW/BIT TYPICAL
- INPUT LOADING:
  - S82S09 – (−150μA) MAXIMUM
  - N82S09 – (−100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- CHIP ENABLE FOR WORD EXPANSION
- BYTE I/O MANIPULATION, INCLUDING PARITY

APPLICATIONS

BUFFER MEMORY
CONTROL REGISTER
FIFO MEMORY
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

I PACKAGE

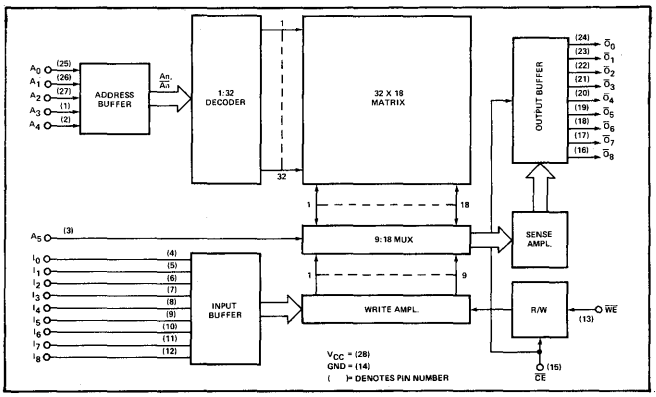


TRUTH TABLE

MODE	CE	WE	I_N	O_N
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	0
DISABLED	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S09)	0° to +75°	°C
	(S82S09)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[7]

S82S09 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5$
N82S09 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER[1]		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX	2.2			2.0			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 5)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 6.4mA (Note 6)		0.35	0.50		0.35	0.5	V
I_{OLK}	Output Leakage Current	V_{CC} = MAX, V_{OUT} = 5.5V (Note 4)		1	60		1	40	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 3)		150	200		150	190	mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V (Note 4)		8			8		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. Test each input one at the time.
6. Measured with the logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
7. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up.

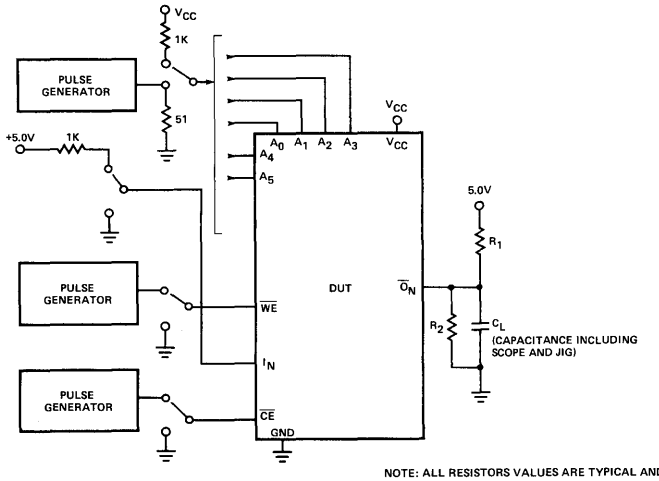
SWITCHING CHARACTERISTICS[3]

S82S09 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S09 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 600Ω R_2 = 900Ω		30	80		30	45	ns
T_{CE}	Chip Enable Access Time			15	50		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	50		15	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		10	0		5	0		ns
T_{WSD}	Data In to Write Enable		50	25		35	25		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

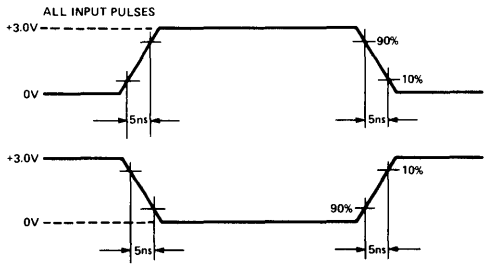
AC TEST LOAD

LOADING CONDITION



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

INPUT PULSES

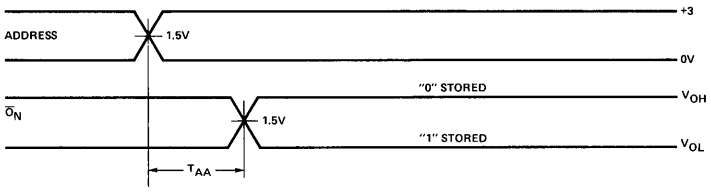


NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up.

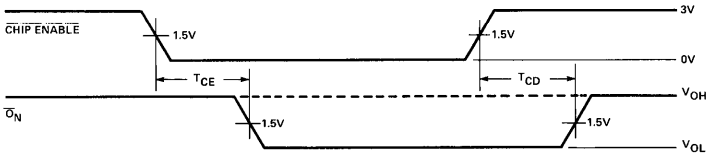
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

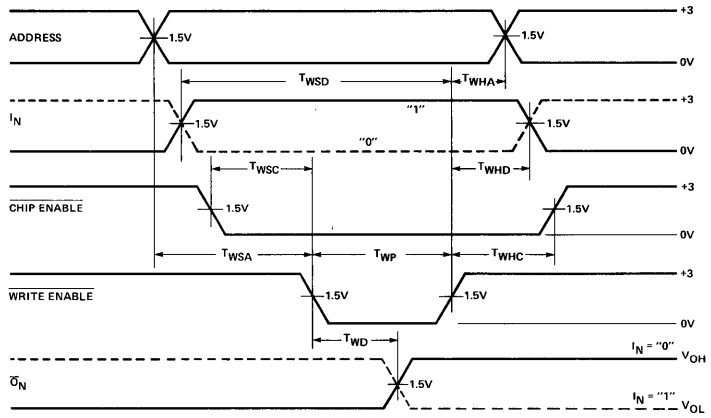
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

DESCRIPTION

The 82S10/11 is a high speed 1024-bit random access memory organized as 1024 words X 1 bit. With a typical access time of 30ns, it is ideal for cache buffer applications and for systems requiring very high speed main memory.

Both the 82S10 and 82S11 require a single +5 volts power supply and feature very low current PNP input structures. They are fully TTL compatible, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S10 and 82S11 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S10/11, I. For the military temperature range (−55°C to +125°C) specify S82S10/11, I.

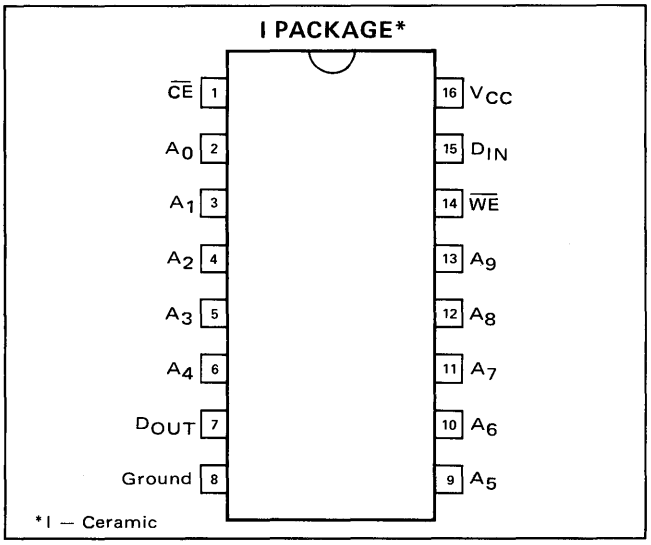
FEATURES

- ORGANIZATION – 1024 X 1
- ADDRESS ACCESS TIME:
  S82S10/11 – 70ns, MAXIMUM
  N82S10/11 – 45ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S10/11 – 75ns, MAXIMUM
  N82S10/11 – 45ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT, TYPICAL
- INPUT LOADING:
  S82S10/11 – (−150μA) MAXIMUM
  N82S10/11 – (−100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  82S10 – OPEN COLLECTOR
  82S11 – TRI-STATE
- NON-INVERTING OUTPUT
- BLANKED OUTPUT DURING WRITE
- 16 PIN CERAMIC PACKAGE

APPLICATIONS

HIGH SPEED MAIN FRAME
CACHE MEMORY
BUFFER STORAGE
WRITABLE CONTROL STORE

PIN CONFIGURATION

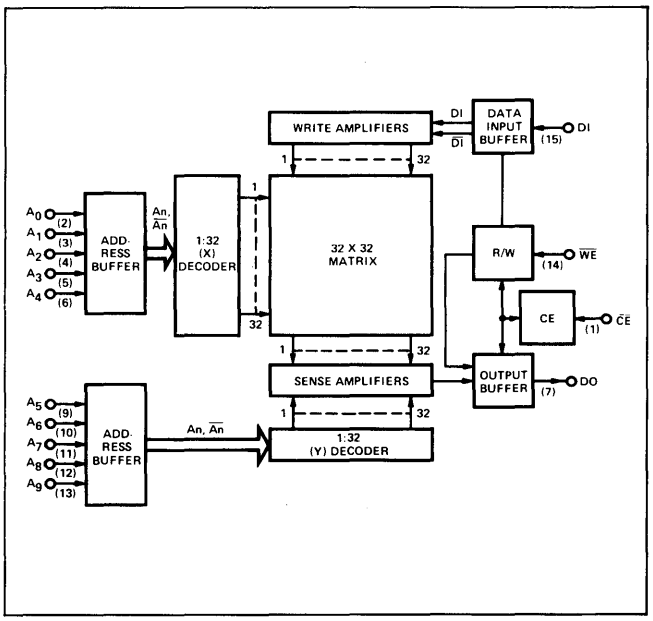


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S10	82S11
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
V_O	Off-State Output Voltage (82S11)	+5.5	Vdc
T_A	Operating Temperature Range (N82S10/11) (S82S10/11)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[9]

S82S10/11 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN (Note 1)			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX (Note 1)	2.1			2.1			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 1, 7)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA (Note 1, 8)		0.35	0.50		0.35	0.45	V
V_{OH}	High Level Output Voltage (82S11)	V_{CC} = MIN, I_{OH} = −2mA (Note 1, 5)	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S10)	V_{CC} = MAX, V_{OUT} = 5.5V (Note 6)		1	60		1	40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 5.5V V_{CC} = MAX, V_{OUT} = 0.45V (Note 6)		1 −1	100 −100		1 −1	60 −60	μA μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{OS}	Short Circuit Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 0V (Note 3)	−20		−100	−20		−100	mA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 4) $0 < T_A < 25°C$ $T_A \geq 25°C$ $T_A \leq 0°C$		 120 95	 155 130 170		 120 95	 155 130 170	 mA mA mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		4			4		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		7			7		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each input one at the time.
8. Measured with a logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
9. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   ϕ_{JA} Junction to Ambient at 400 fpm air flow — 50°C/Watt
   ϕ_{JA} Junction to Ambient — still air — 90°C/Watt
   ϕ_{JA} Junction to Case — 20°C/Watt

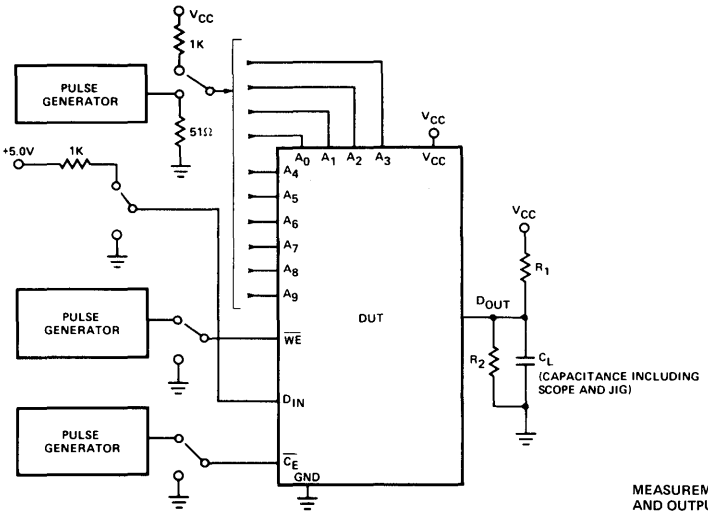
SWITCHING CHARACTERISTICS[3]

S82S10/11 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0^{\circ}C \leq T_A \leq +75^{\circ}C$, $4.75V \leq V_{CC} \leq 5.25$

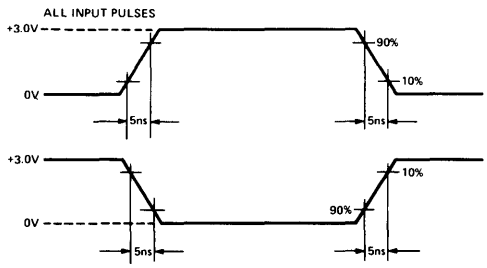
PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		30	70		30	45	ns
T_{CE}	Chip Enable Access Time			15	45		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	45		15	30	ns
T_{WD}	Write Enable to Output Disable Time			20	45		20	30	ns
T_{WR}	Write Recovery Time			20	45		20	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		15	0		5	0		ns
T_{WSD}	Data In to Write Enable		55	35		40	35		ns
T_{WSC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

AC TEST LOAD

LOADING CONDITION



INPUT PULSES



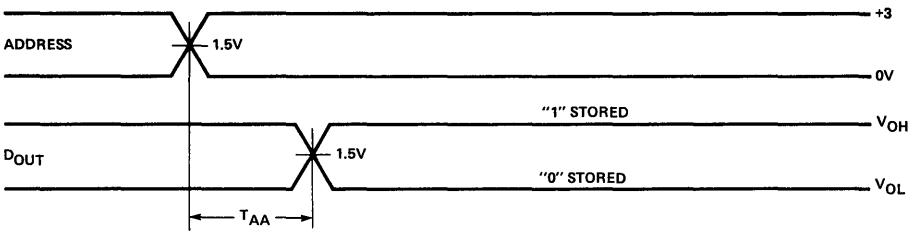
MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} Junction to Ambient at 400 fpm air flow – 50° C/Watt
   θ_{JA} Junction to Ambient – still air – 90° C/Watt
   θ_{JA} Junction to Case – 20° C/Watt

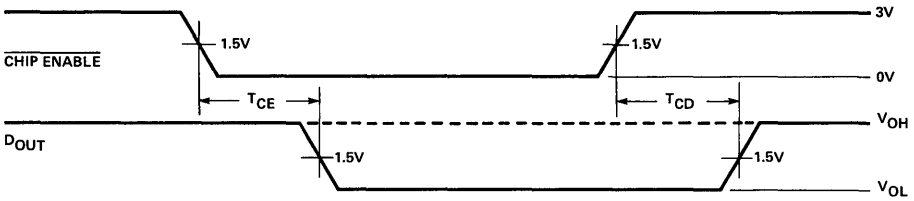
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

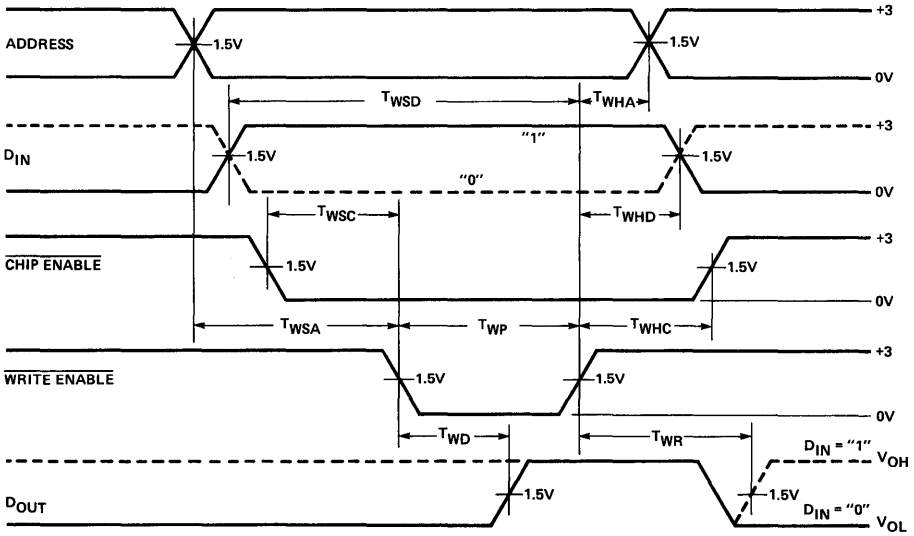
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

DESCRIPTION

The 82S12/112 is a Schottky TTL 32 bit multiport memory organized in 8 words of 4 bits each. The device is ideally suited for high speed accumulators and buffer memories.

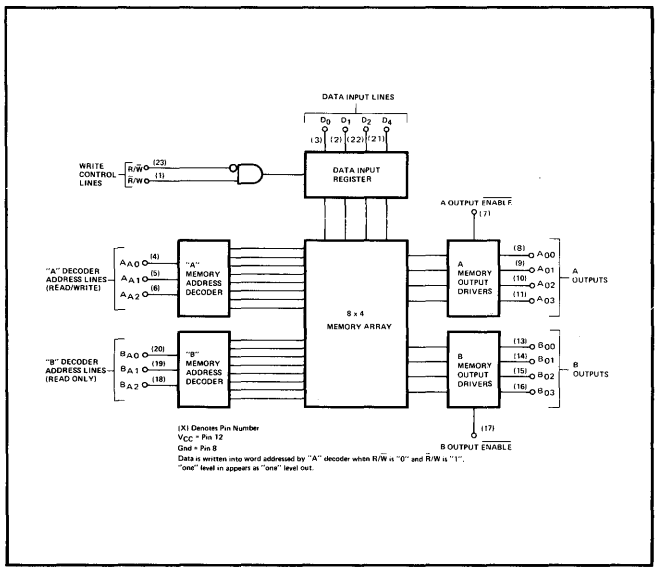
Stored data is addressed through 2 independent sets of 3-input decoders, and read out when the corresponding output enable line is low. Two separate word locations can, therefore, be read at the same time by enabling both the A and B output drivers. In addition, data can be read and written at the same time by utilizing the "A" address to specify the location of the word to be written, and the "B" address to specify the word to be read.

The 82S12/112 can be used in larger memory arrays since it includes all the control logic required to disable the chip and the outputs are open-collector devices suitable for "Wire-ORing."

FEATURES

- LOW CURRENT INPUT BUFFERS (−25μA TYPICAL)
- SEPARATE INPUT DECODERS FOR EACH WORD
- SEPARATE OUTPUT ENABLE LINES FOR EACH WORD
- OPEN COLLECTOR (82S12) OR TRI-STATE (82S112) OUTPUTS
- 2 WRITE ENABLE LINES
- FAST ACCESS (20 ns TYPICAL)
- USEFUL 8 X 4 ORGANIZATION
- TTL COMPATIBLE
- NON INVERTING DATA LINES

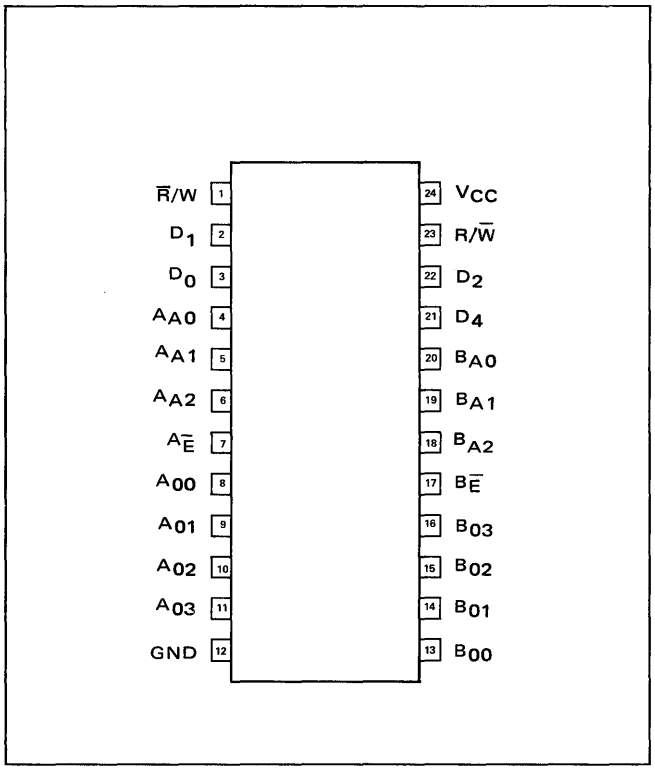
BLOCK DIAGRAM



APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
GENERAL REGISTER

PIN CONFIGURATION



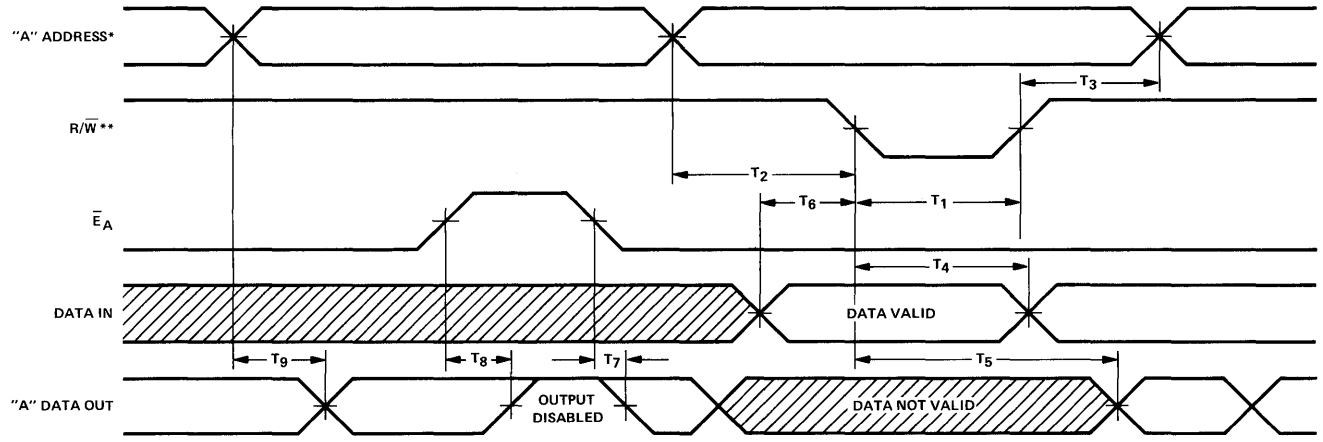
TRUTH TABLE

R/W	R/W	A OUTPUT ENABLE	B OUTPUT ENABLE	MODE	OUTPUTS A	OUTPUTS B
0	X	1	1	Outputs Disabled	"1"	"1"
0	X	1	0	Read	"1"	Data
0	X	0	1	Read	Data	"1"
0	X	0	0	Read	Data	Data
1	1	1	1	Read	"1"	"1"
1	1	1	0	Read	"1"	Data
1	1	0	1	Read	Data	"1"
1	1	0	0	Read	Data	Data
1	0	1	1	Write	"1"	"1"
1	0	1	0	Write	"1"	Data "B" Address
1	0	0	1	Write	Data Being Written	"1"
1	0	0	0	Write	Data Being Written	Data "B" Address

OBJECTIVE ELECTRICAL SPECIFICATIONS $0°C \leq T_A \leq 75°C$; $-4.75\ V \leq V_{CC} \leq 5.25\ V$.

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
Input "0" Current				−250	μA	$V_{in} = 0.45\ V$
Input "1" Current				25	μA	$V_{in} = 5.5\ V$
Input "0" Threshold Voltage				0.85	V	
Input "1" Threshold Voltage		2.0			V	
Input Clamp Voltage		−1.2			V	$I_{in} = -18\ mA$
Output "0" Current		16			mA	$V_{out} = 0.5\ V$
Output "0" Current		9.6				$V_{out} = 0.45\ V$
Output "1" Voltage (825112)		2.6			Volts	$I_{out} = -3.2\ mA$
Output Off Current (82S12)				40	μA	$V_{out} \leq 5.5\ V$
Output Off Current (82S112)		−40		+40	μA	$0.45 \leq V_{out} \leq 5.5\ V$
Power Consumption			110/550	160/840	mA/mW	Outputs Enabled
Write Pulse Width	T_1		15	30	ns	$T_A = 25°C$ Only
	T_1			45	ns	$0°C \leq T_A \leq 75°C$
Address Set Up Time	T_2		10		ns	
Address Hold Time	T_3		0		ns	
Data Input Hold Time	T_4		15		ns	
Write Access Time	T_5		30		ns	
Data Input Set Up Time	T_6		5		ns	
Output Enable Time	T_7		10	20	ns	
Output Disable Time	T_8		10	20	ns	
Address Access Time	T_9		20	30	ns	

TIMING DIAGRAM



T_1 WRITE PULSE WIDTH – Width of write pulse (when R/W="1" and R/W="0")

T_2 ADDRESS SETUP TIME – Required delay between beginning of valid Address and beginning of Write pulse.

T_3 ADDRESS HOLD TIME – Required delay between end of Write pulse and end of valid Address.

T_4 DATA INPUT HOLD TIME – Required delay between start of Write pulse and end of Valid Data input.

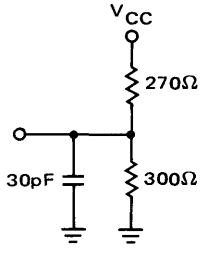
T_5 WRITE ACCESS TIME – Delay between beginning of Write pulse and Data Out at new value.

T_6 DATA INPUT SET-UP TIME – Required delay between beginning ov Valid Data Input and start of Write pulse.

T_7 OUTPUT ENABLE TIME – Delay between beginning of Output Enable high and when Data Output becomes valid.

T_8 OUTPUT DISABLE TIME – Delay between when Output Enable becomes low and Data Output is in off state.

T_9 ADDRESS ACCESS TIME – Delay between beginning of Valid Address (with Output Enable high, R/W high and R/W low) and when Data Output becomes valid.



A. C. LOAD

NOTES

*"B" Address functions identically in read mode. No write mode through B address decoder.

**R/W input is either the reverse of R/W or held high.

Outputs can be disabled during write cycle to penetrate a known output state during write.

DESCRIPTION

The 82S16 and 82S17 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and −250μA (S82S16/17) or −100μA (N82S16/17) for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S16 and 82S17 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S16/17, B or F. For the military temperature range (−55°C to +125°C) specify S82S16/17, F only.

FEATURES

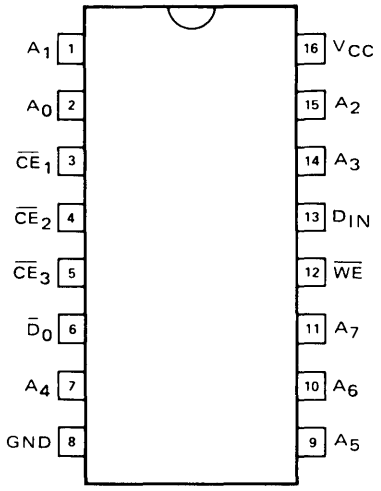
- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME:
  S82S16, S82S17 – 70ns, MAXIMUM
  N82S16, N82S17 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S16, S82S17 – 70ns, MAXIMUM
  N82S16, N82S17 – 55ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING:
  S82S16, S82S17 – (−250μA) MAXIMUM
  N82S16, N82S17 – (−100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- 16 PIN CERAMIC DIP
- OUTPUT OPTION:
  TRI-STATE – 82S16
  OPEN COLLECTOR – 82S17

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



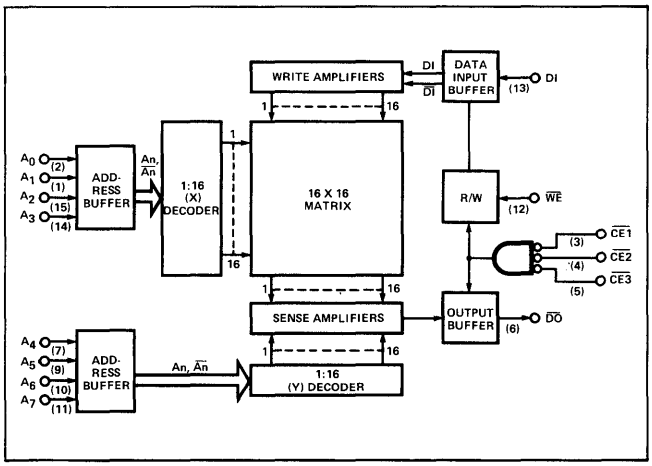
*B — Plastic
C — Cerdip

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S16	82S17
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S17)	+5.5	Vdc
V_O	Off-State Output Voltage (82S16)	+5.5	Vdc
T_A	Operating Temperature Range		
	S82S16/17	−55° to +125°	°C
	N82S16/17	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S16/17 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S16/17 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS		N82S16/17			S82S16/17			UNIT	NOTES
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX		
V_{IH}	High-Level Input Voltage	V_{CC} = MAX		2.0			2.0			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = MIN				0.85			0.8	V	
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA			−1.0	−1.5		−1.0	−1.5	V	1, 8
V_{OH}	High-Level Output Voltage (82S16)	V_{CC} = MIN, I_{OH} = −3.2mA		2.6			2.4			V	1, 6
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA			0.35	0.45		0.35	0.5	V	1, 7
I_{OLK}	Output Leakage Current (82S17)	V_{OUT} = 5.5V			1	40		1	40	μA	5
$I_{O(OFF)}$	Hi-Z State Output Current (82S16)	V_{OUT} = 5.5V			1	40		1	50	μA	5
		V_{OUT} = 0.45V			−1	−40		−1	−50	μA	5
I_{IH}	High-Level Input Current	V_{CC} = MAX, V_{IN} = 5.5V			1	25		1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = MAX, V_{IN} = 0.45V			−10	−100		−10	−250	μA	8
I_{OS}	Short-Circuit Output Current (82S16)	V_{CC} = MAX, V_O = 0V		−20		−70	−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S16/17)	V_{CC} = MAX			80	115		80	120	mA	4
	V_{CC} Supply Current (82S16/17)	V_{CC} = MAX, T_A = +125°C							99	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5			5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	V_{CC} = 5.0V		8			8		pF	

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

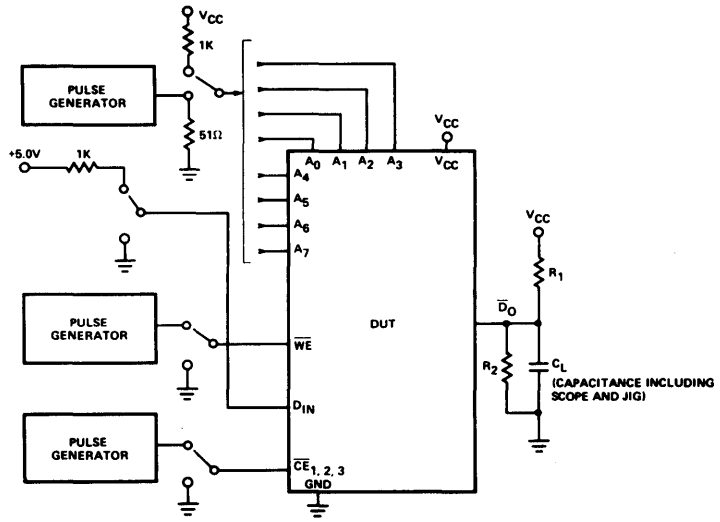
SWITCHING CHARACTERISTICS

S82S16/17 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S16/17 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

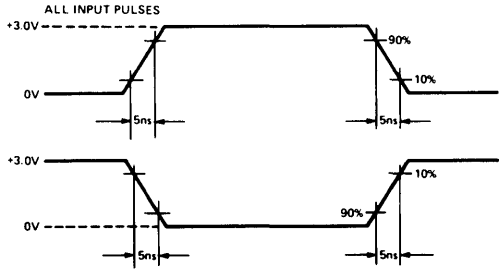
PARAMETER		TEST CONDITIONS	S82S16/17			N82S16/17			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delay									
T_{AA}	Address Access Time	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$		40	70		40	50	ns
T_{CE}	Chip Enable Access Time			30	40		30	40	ns
T_{CD}	Chip Enable Output Disable Time			30	40		30	40	ns
T_{WD}	Write Enable to Output Valid Time			30	55		30	40	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	20	5		20	5		ns
T_{WSD}	Data In to Write Enable		50	40		40	30		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		10	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width	Note 2	40	20		30	15		ns

AC TEST LOAD

LOADING CONDITION



INPUT PULSES

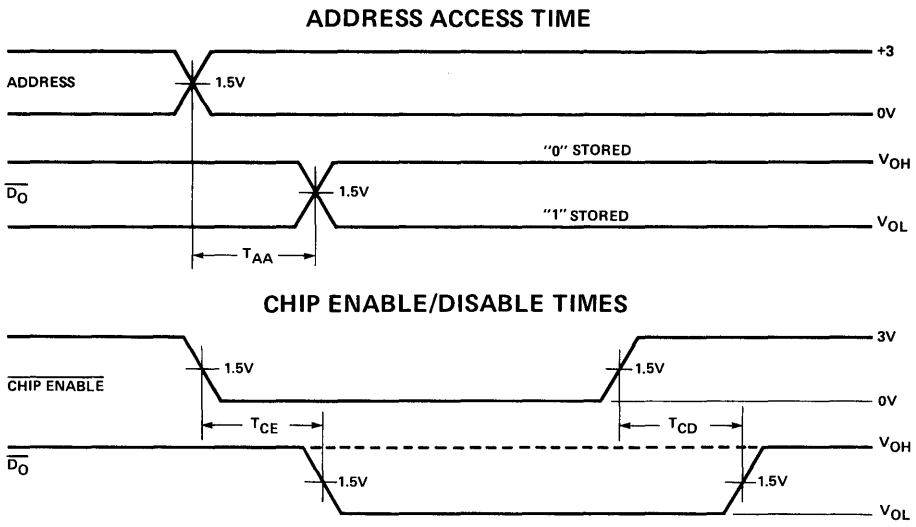


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

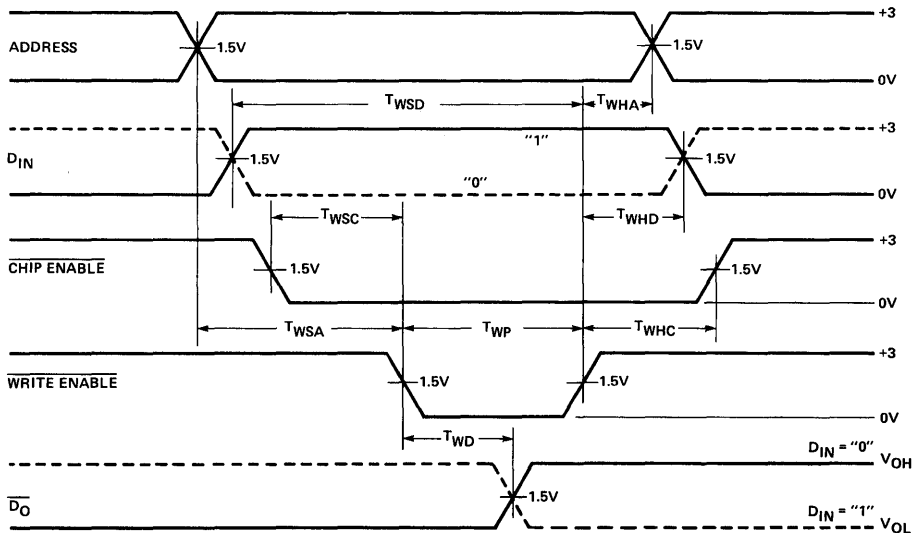
NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

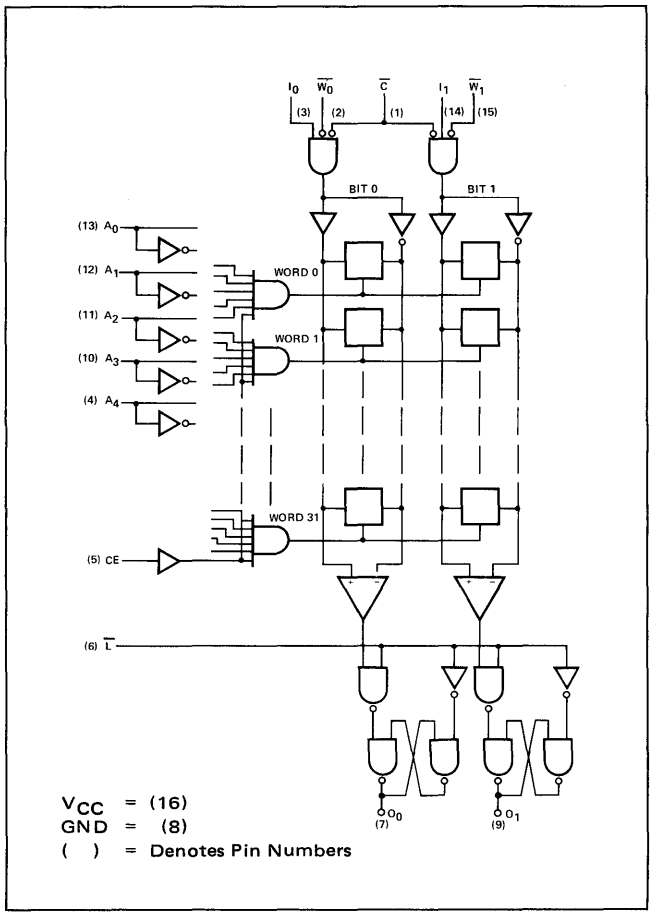
FEATURES

- BUFFERED ADDRESS LINES
- ON CHIP LATCHES
- ON CHIP DECODING
- BIT MASKING CONTROL LINES
- ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS WITH 40mA CAPABILITY
- PROTECTED INPUTS
- VERY HIGH SPEEDS (25ns TYP)

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

LOGIC DIAGRAM



TRUTH TABLE

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C; 4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			.45	V	V_{out} = 32mA	
"1" Output Leakage Current			40	μA	V_{out} = 5.5V	
"0" Input Current (All Inputs)			−1.6	mA	V_{in} = 0.45V	
"1" Input Current (All Inputs)			25	μA	V_{in} = 5.5V	
Input "0" Voltage (V_{IL})			0.85	V		
Input "1" Voltage (V_{IH})	2.0			V		
Power Consumption			130/683	mA/mW		
Input Clamp Voltage	−1.2			V	I_{in} = −18mA	

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C, 4.75 \leq V_{CC} \leq 5.25V$

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Read Access Time Address to Output	t_1		25	50	ns		
Address Set-Up Time	t_2		8	15	ns		
Data Set-Up Time	t_3		15	20	ns		
Address Hold Time	t_4			0	ns		
Control or Write Pulse Width	t_5		15	20	ns		
Write Access Time	t_6		20	25	ns		
Address to Latch Set-Up Time	t_7		25	50	ns		
Latch Address to Address Hold Time	t_8		7	10	ns		
Delatch Access Time	t_9		15	25	ns		
Data Hold Time	t_{10}		0	5	ns		

AC WAVEFORM

Read Access Time

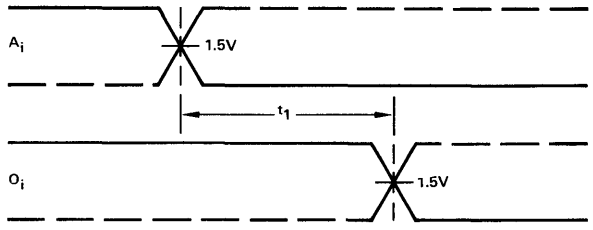
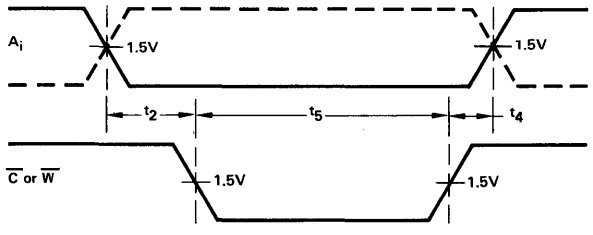


FIGURE 1

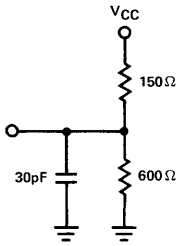
Address Setup and Hold Time



$t_r = t_f \leq 5$ ns, INPUT VOLTAGE = 2.8 Volts

FIGURE 2

TEST LOAD



AC WAVEFORMS

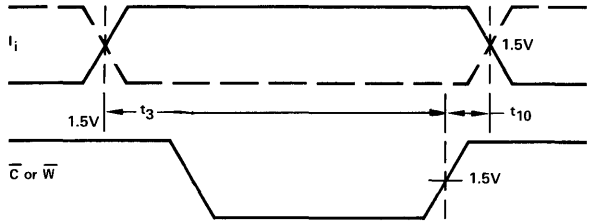


Fig. 3 Data Setup and Hold Time

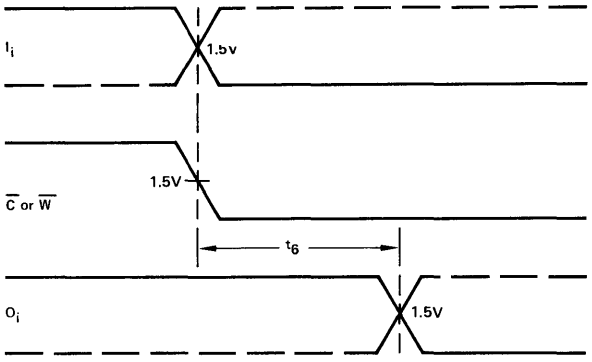


Fig. 4 Write Access Time

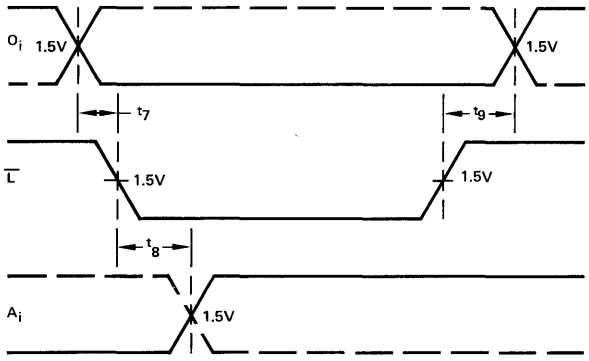
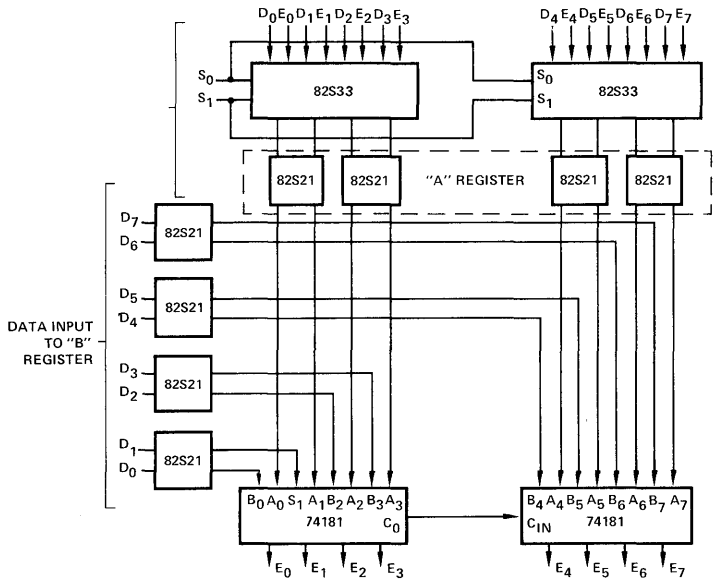


Fig. 5 Latch Times

TYPICAL APPLICATION



BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 x 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

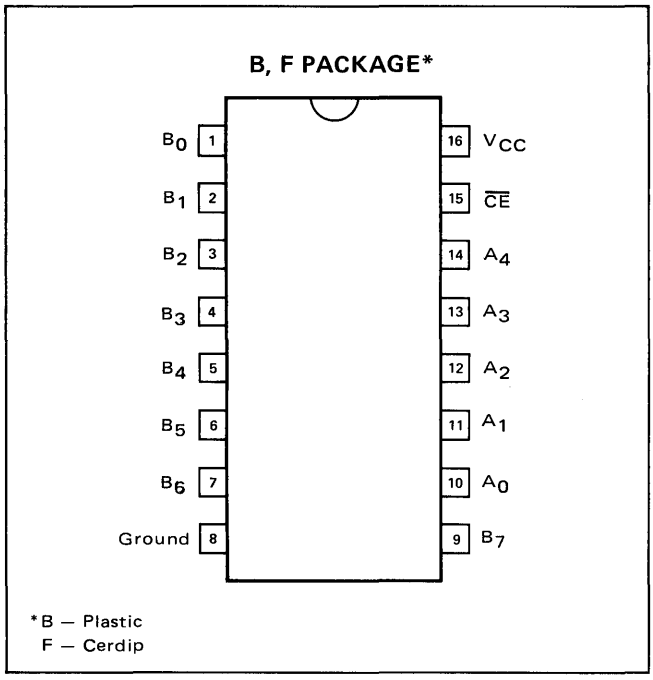
DESCRIPTION

The 82S23 (Open Collector Outputs) and the 82S123 (Tri-State Outputs) are Bipolar 256-Bit Read Only Memories, organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S23 and 82S123 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, B or F. For the military temperature range (−55°C to +125°C) specify S82S23/123, F only.

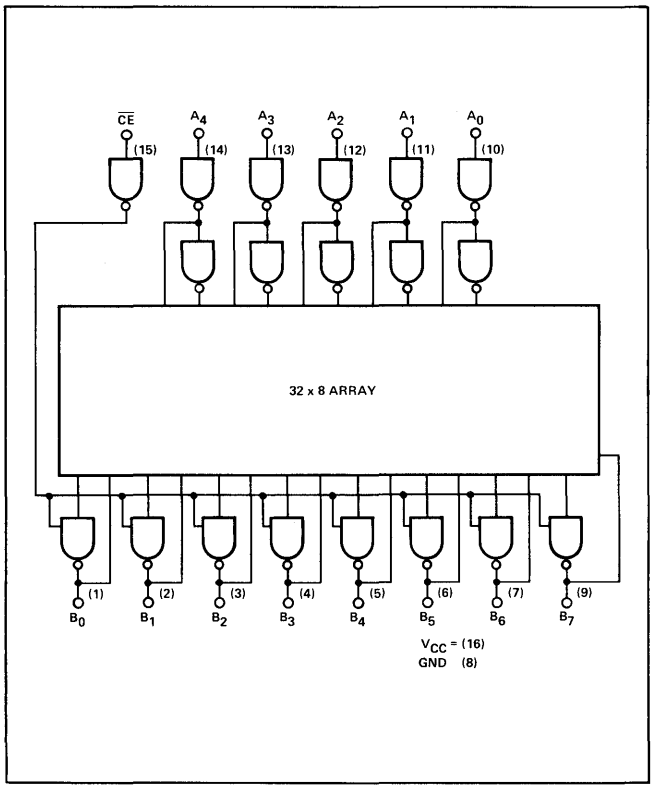
PIN CONFIGURATION



FEATURES

- ORGANIZATION — 32 X 8
- ADDRESS ACCESS TIME:
  - S82S23/S82S123 — 65ns, MAXIMUM
  - N82S23/N82S123 — 50ns, MAXIMUM
- POWER DISSIPATION — 1.3mW/BIT TYPICAL
- INPUT LOADING:
  - S82S23/123 — (−150μA) MAXIMUM
  - N82S23/123 — (−100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - OPEN COLLECTOR — 82S23
  - TRI-STATE — 82S123
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

LOGIC DIAGRAM



APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
FORMAT CONVERSION
HARDWIRED ALGORITHMS
RANDOM LOGIC
CODE CONVERSION

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S23)	+5.5	Vdc
V_O	Off-State Output Voltage (82S123)	+5.5	Vdc
T_A	Operating Temperature Range (N82S23/123) (S82S23/123)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S23/S82S123 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S23/N82S123 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S23/S82S123			N82S23/N82S123			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.45	V
I_{OLK}	Output Leakage Current (82S23)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			50			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S123)	$\overline{CE}$ = "1", V_{OUT} = 5.5V $\overline{CE}$ = "1", V_{OUT} = 0.5V			50 −50			40 −40	μA μA
V_{OH}	"1" Output Voltage (82S123)	$\overline{CE}$ = "0", I_{OUT} = −2mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			50	μA
V_{IL}	"0" Level Input Voltage				0.8			0.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			65	85		65	77	mA
V_{IC}	Input Clamp Voltage	I_N = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S123)	V_{OUT} = 0V	−20		−100	−20		−90	mA

SWITCHING CHARACTERISTICS

S82S23/S82S123 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S23/N82S123 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S23/S82S123			N82S23/N82S123			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		35	65		35	50	ns
T_{CD}	Chip Disable to Output			25	40		25	35	ns
T_{CE}	Chip Enable to Output			25	40		25	35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^{\circ}C$

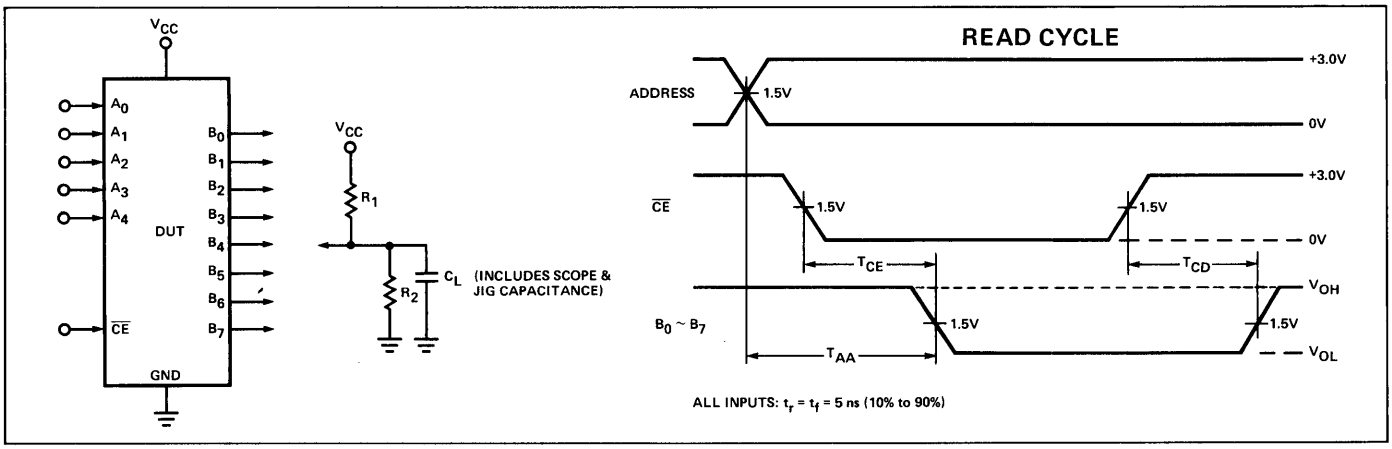
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 250 \pm 50mA$ (Transient or steady state)	9.5	10.0	10.5	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +10.0 \pm 0.5V$	200	250	300	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 65 \pm 3mA$ (Transient or steady state)	15.0	15.5	16.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +15.5 \pm 0.5V$	62	65	68	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_V	Verify Delay		50			μs
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

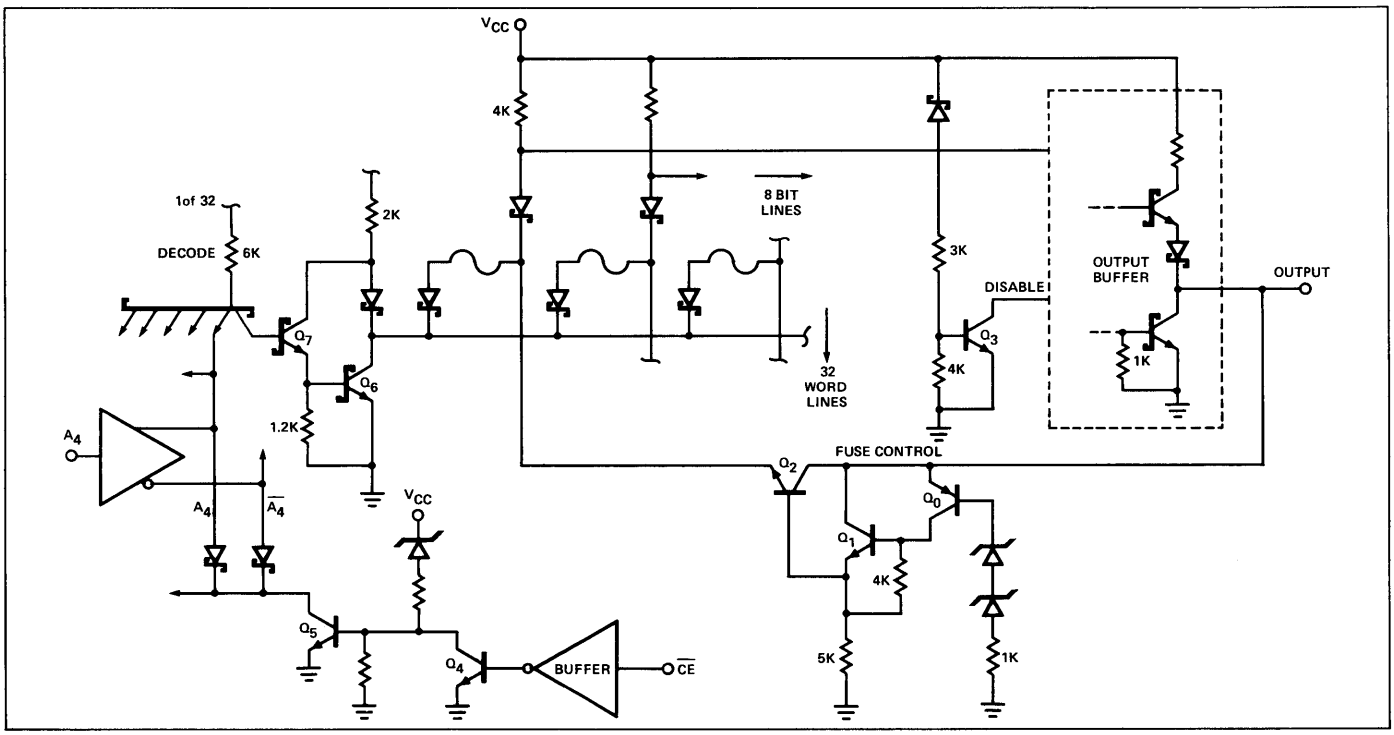
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = +10 \pm 0.5V$.
3. After 10μs delay, apply $I_{OUT} = 65 \pm 3mA$ to the output to be programmed. Program one output at a time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove I_{OUT} from the programmed output.
6. After 10μs delay, return V_{CC} to 0V.
7. To verify programming, after 50μs delay, raise V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
8. Raise V_{CC} to $V_{CCP} = +10 \pm 0.5V$ and repeat steps 3 through 7 to program other bits at the same address.
9. After 10μs delay, repeat steps 2 through 8 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure that +15.5 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.

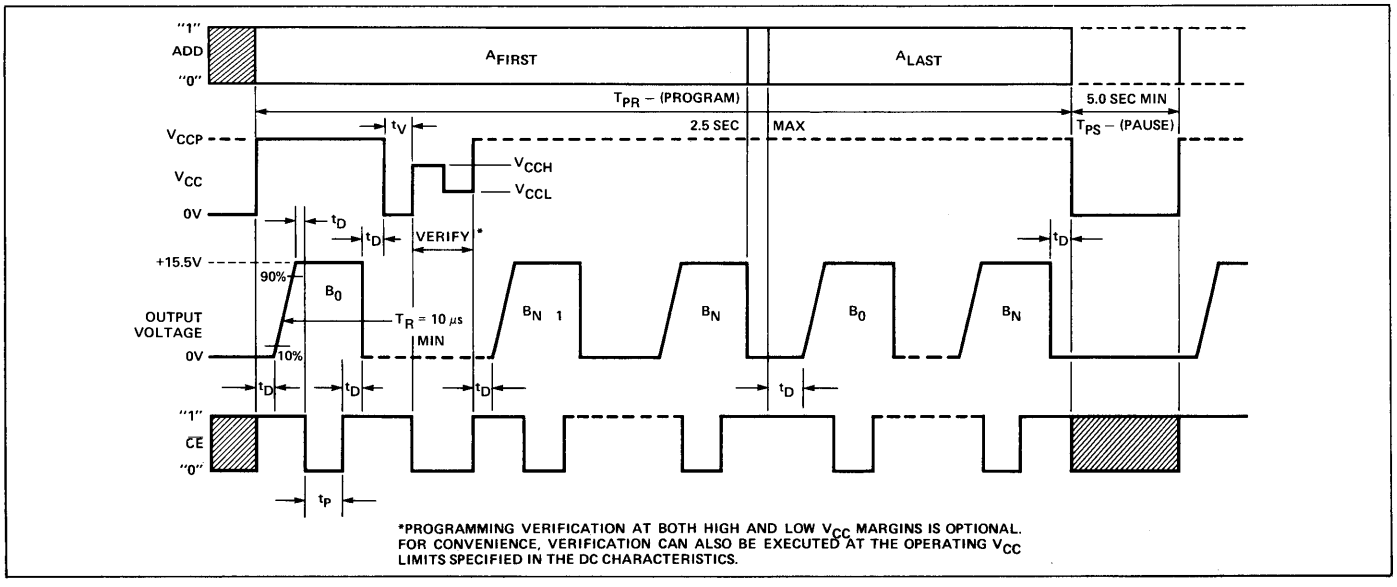
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH

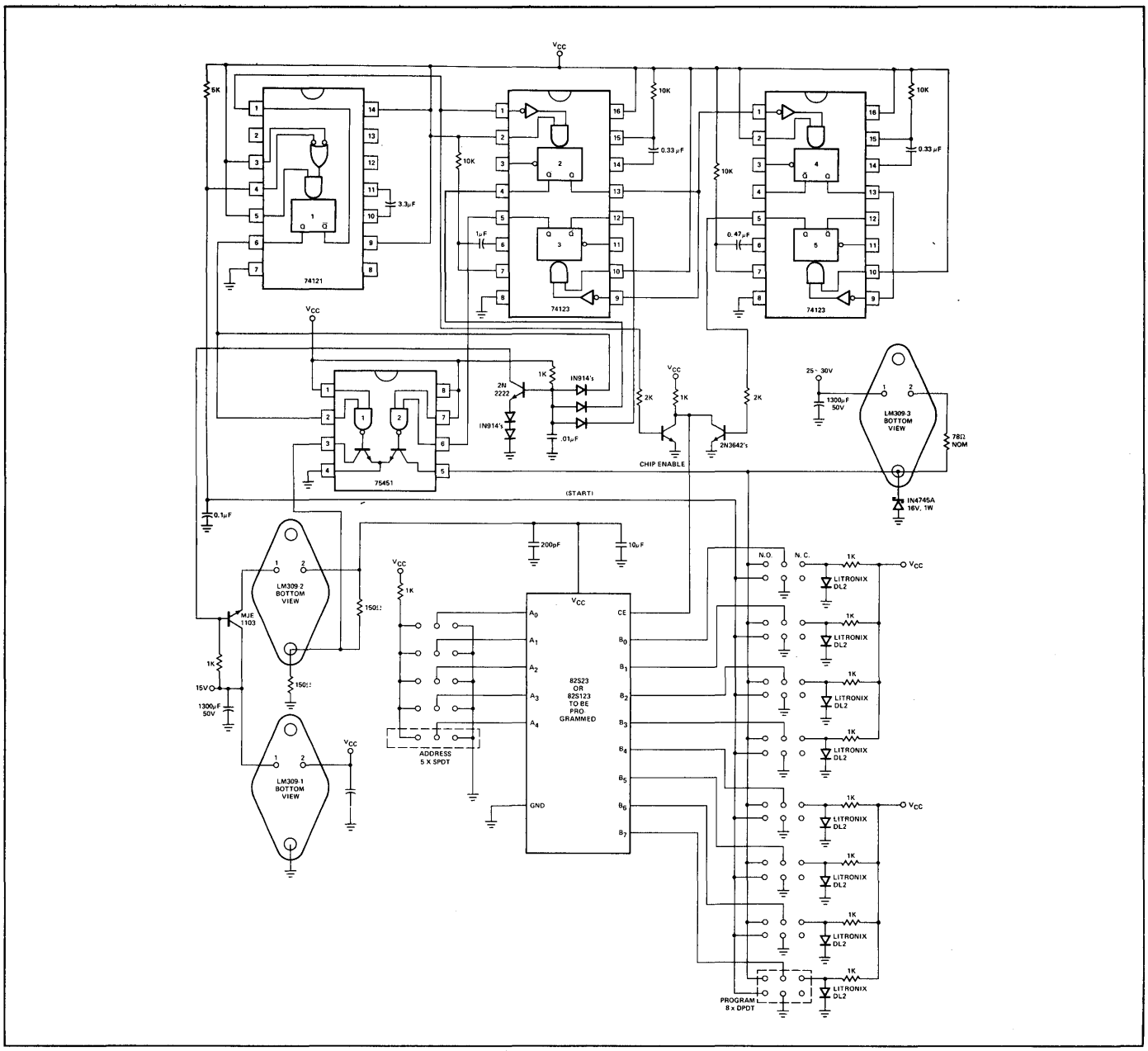


TYPICAL PROGRAMMING SEQUENCE

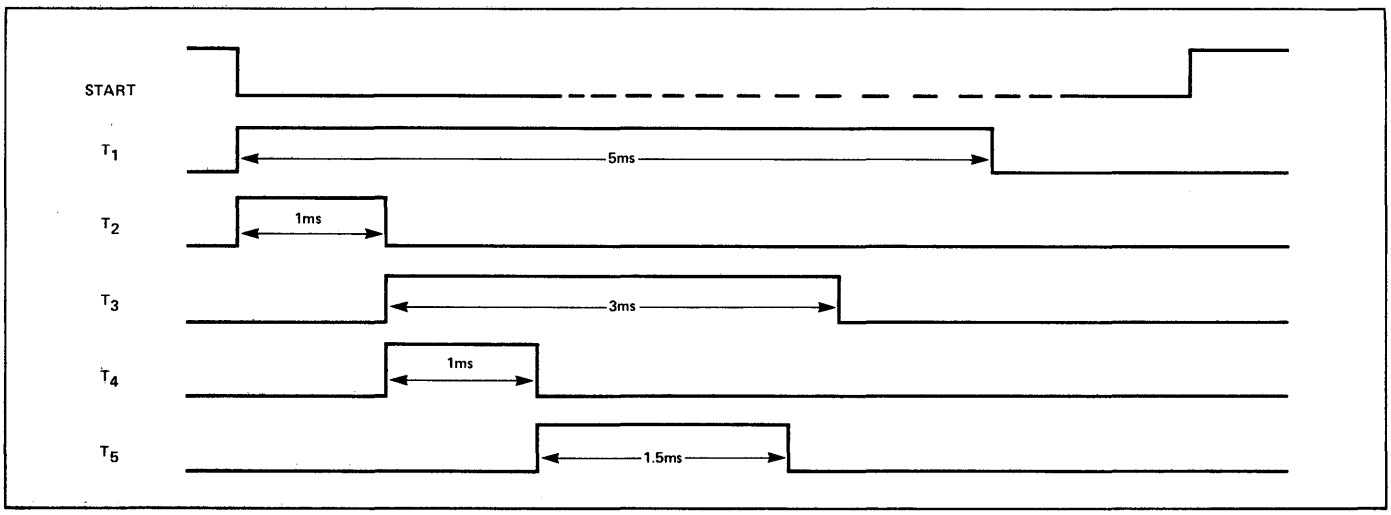


*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

MANUAL PROGRAMMER



TIMING SEQUENCE



signetics

64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM) 82S25

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S25 is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

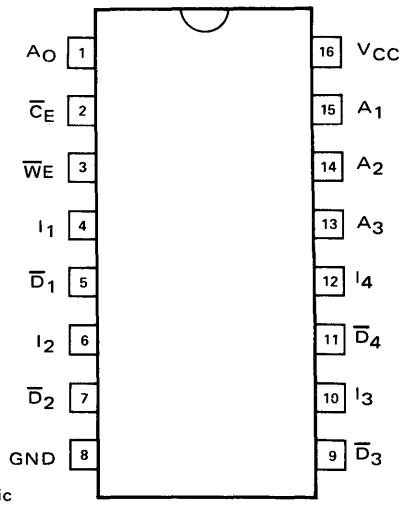
The 82S25 is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 82S25 assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 82S25 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S25, B or F. For the military temperature range (−55°C to +125°C) specify S82S25, F only.

PIN CONFIGURATION

B, F PACKAGE*



*B — Plastic
F — Cerdip

TRUTH TABLE

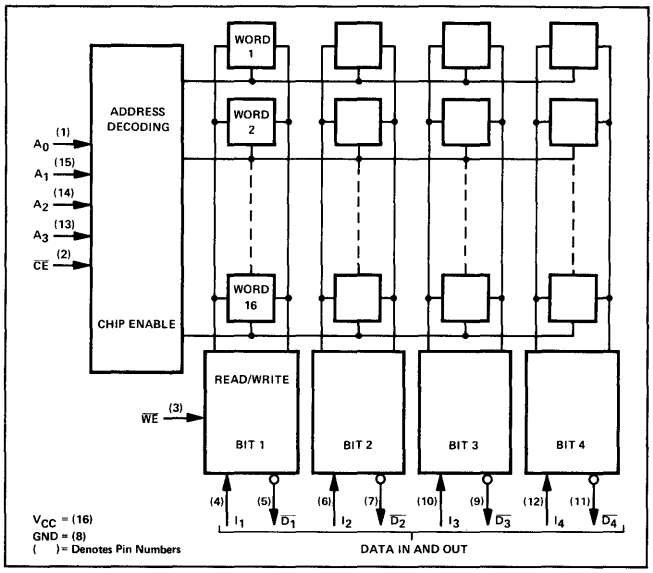
MODE	$\overline{CE}$	$\overline{WE}$	In	$\overline{Dn}$
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care.

FEATURES

- ORGANIZATION – 16 X 4
- ADDRESS ACCESS TIME:
  S82S25 – 60ns, MAXIMUM
  N82S25 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S25 – 50ns, MAXIMUM
  N82S25 – 35ns, MAXIMUM
- POWER DISSIPATION – 6.25mW/BIT, TYPICAL
- INPUT LOADING:
  S82S25 – (−150μA) MAXIMUM
  N82S25 – (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

BLOCK DIAGRAM



APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS
CONTROL STORE

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S25)	0° to +75°	°C
	(S82S25)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S25 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5V$
N82S25 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	S82S25[1,2,3]			N82S25[1,2,3]			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25			10	μA
V_{IL}	"0" Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	"1" Level Input Voltage	V_{CC} = MAX	2.0			2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −12mA, V_{CC} = MIN (Note 6)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA, V_{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C_{IN}	Input Capacitance	V_{IH} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V, $\overline{CE}$ = "1"		8			8		pF
I_{CC}	Power Supply Current	(Note 5)		80	120		80	105	mA
I_{OLK}	Output Leakage Current	$\overline{CE}$ = "1", V_{OUT} = 5.5V, V_{CC} = MIN		<1	100		<1.0	100	μA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V; "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at V_{CC} = +5.0V and T_A = +25°C.

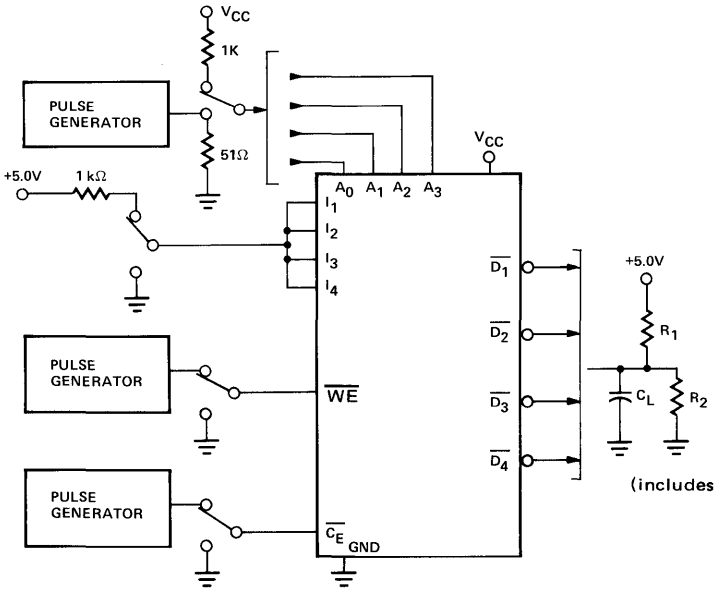
SWITCHING CHARACTERISTICS

S82S25 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S25 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S25			N82S25			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			35	60		35	50	ns
T_{CE}	Chip Enable Access Time			20	35		20	35	ns
T_{CD}	Chip Enable Output Disable Time			20	35		20	35	ns
T_{WD}	Write Enable to Output Disable Time			20	30		20	25	ns
T_{WR}	Write Recovery Time			35	60		35	50	ns
Write Set-up Times		$R_1 = 270\Omega$ $R_2 = 600\Omega$							
T_{WSA}	Address to Write Enable	$C_L = 30pF$	10	−8		0	−8		ns
T_{WSD}	Data In to Write Enable		25	5		20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0	−5		0	−5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	−3		5	−3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 7)		30	18		30	18		ns

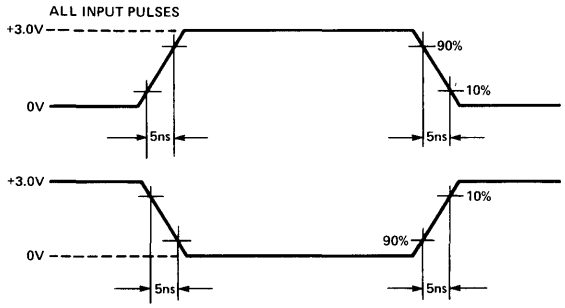
AC TEST LOAD AND WAVEFORMS

LOADING CONDITION



(includes jig and scope capacitance)

INPUT PULSES

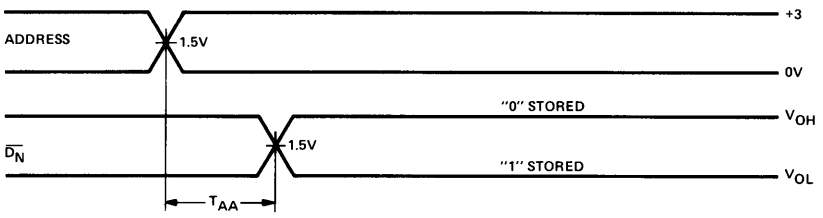


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

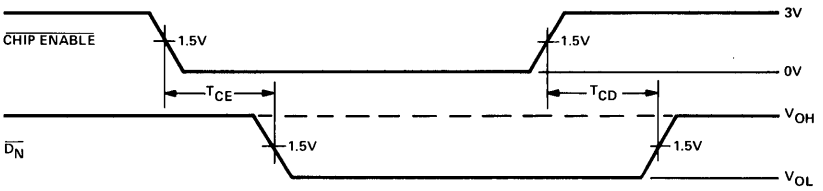
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

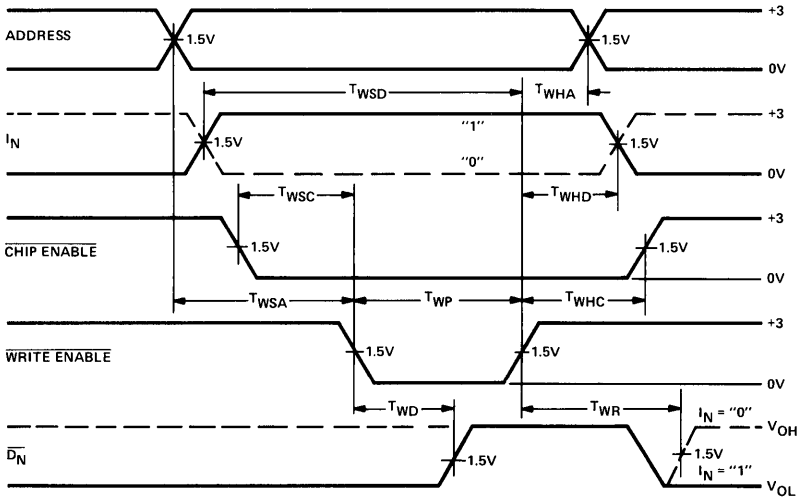
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid — not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

DESCRIPTION

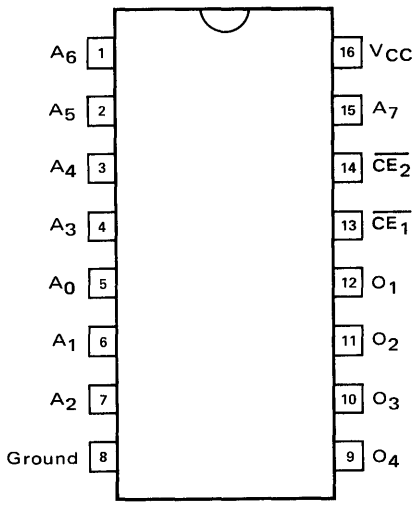
The 82S27 is a Bipolar 1024-Bit Read Only Memory, organized as 256 words by 4 bits per word. It is Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S27 is supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S27 is fully TTL compatible, and includes on-chip decoding, two chip enable inputs, and open collector outputs for ease of memory expansion.

The 82S27 is available in the commercial temperature range. For the commercial temperature range (0°C to +75°C) specify N82S27, F.

PIN CONFIGURATION

F PACKAGE*

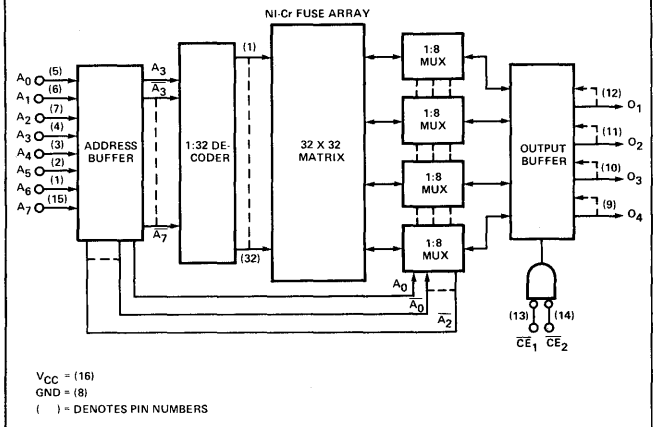


*F = Cerdip

FEATURES

- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME – 40ns, MAXIMUM
- POWER DISSIPATION – 0.6mW/BIT, TYPICAL
- INPUT LOADING – 1.6mA, MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

BLOCK DIAGRAM

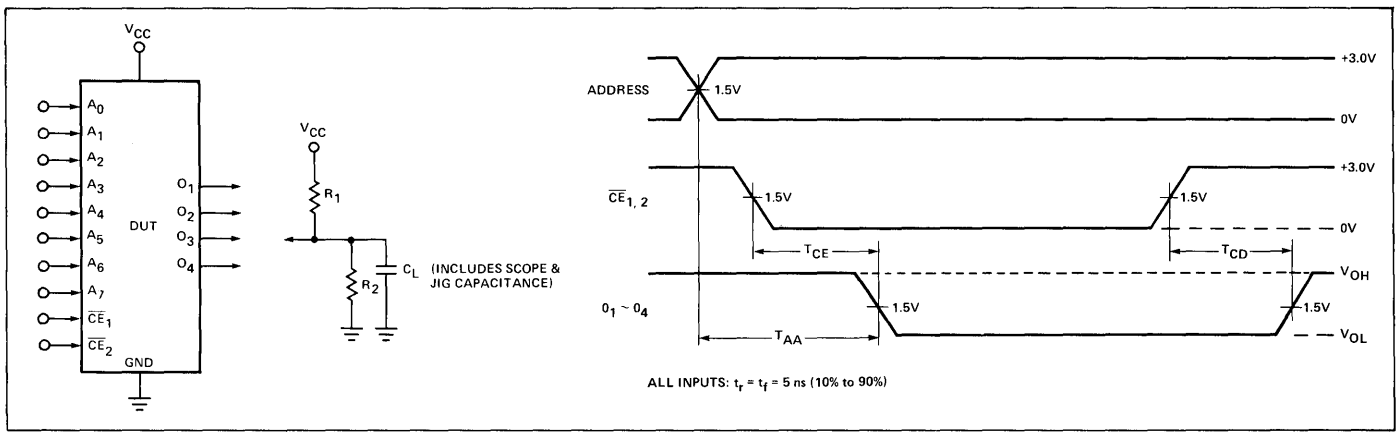


VCC = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

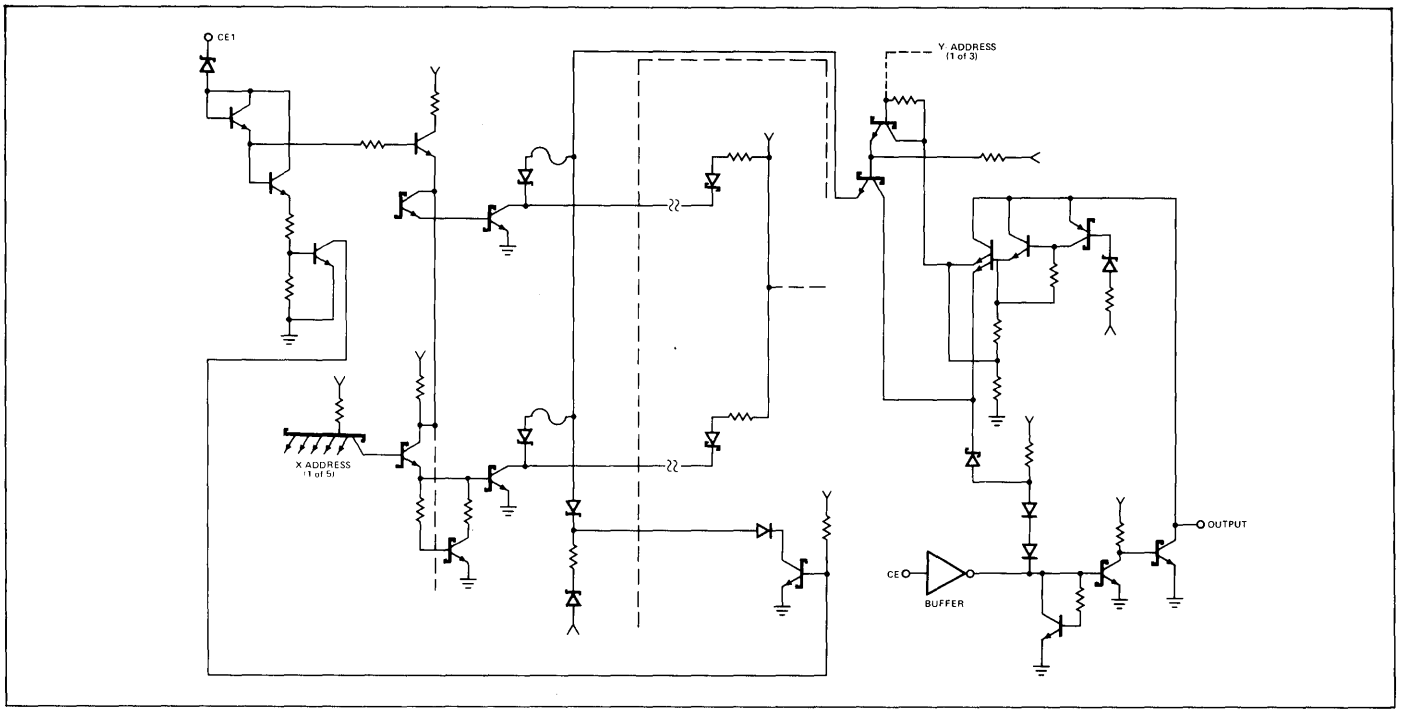
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

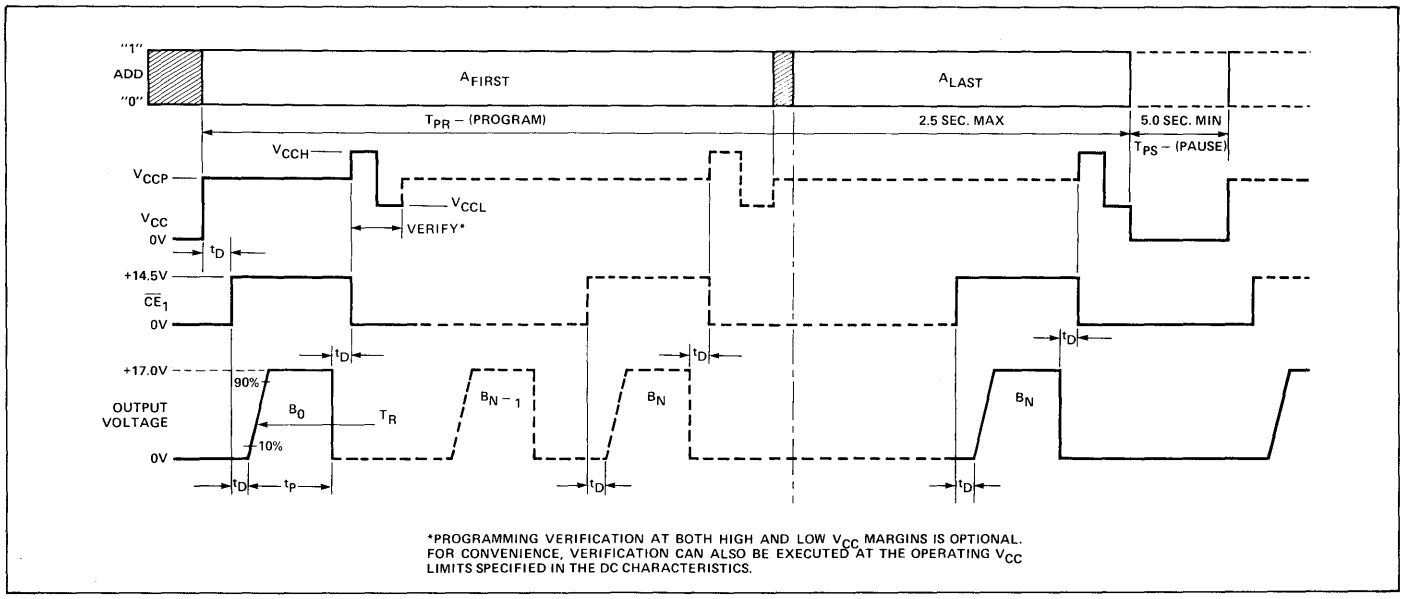
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

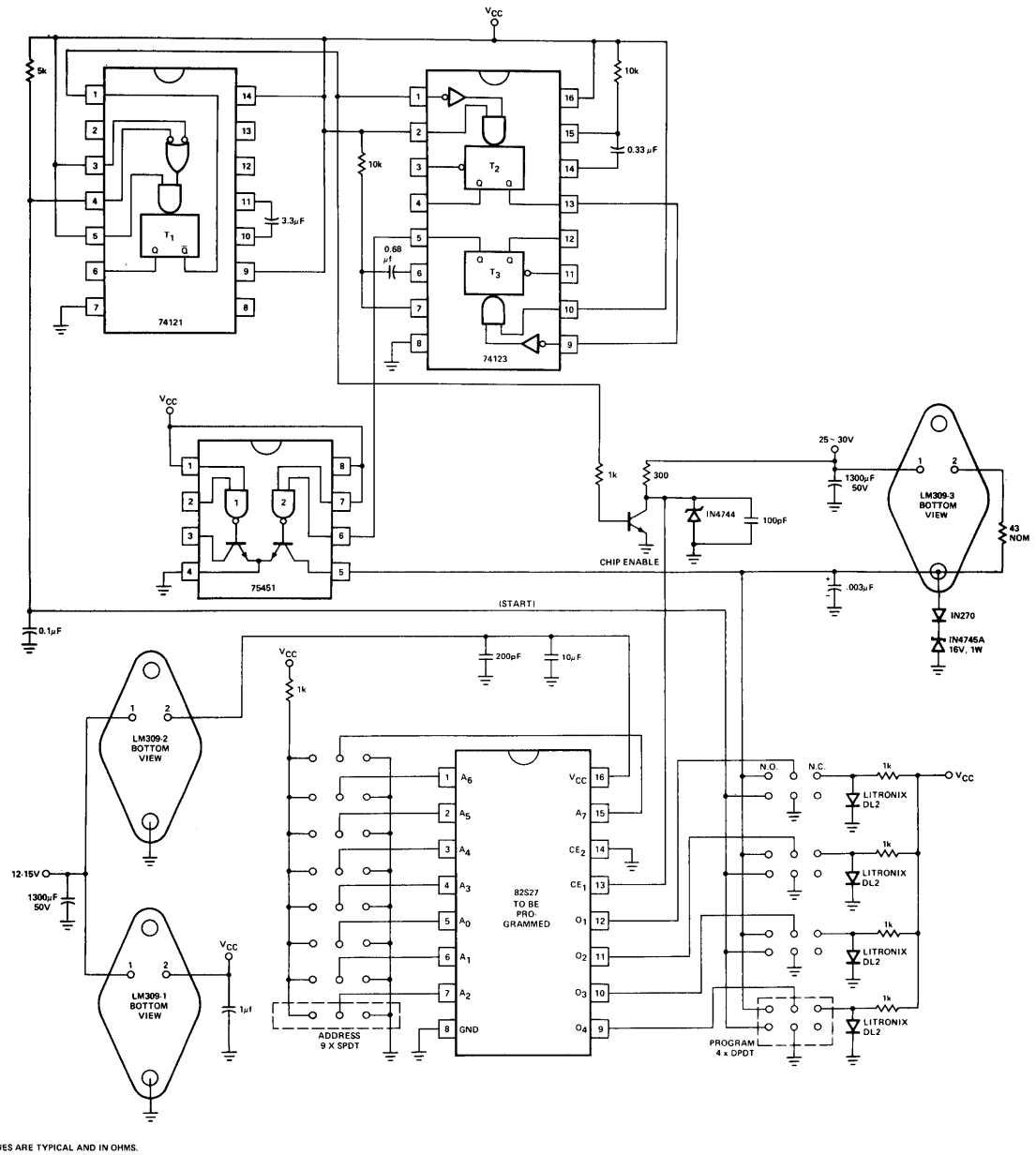
PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 32mA		0.45	0.50	V
I_{OLK}	Output Leakage Current	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{OUT} = 5.5V			100	μA
I_{IH}	"1" Input Current	V_{IN} = 2.4V			40	μA
		V_{IN} = 5.5V			1	mA
I_{IL}	"0" Input Current	V_{IN} = 0.50V			−1.6	mA
V_{IL}	"0" Level Input Voltage				.80	V
V_{IH}	"1" Level Input Voltage		2.0			V
I_{CC}	V_{CC} Supply Current			120	140	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −12mA		−1.0	−1.5	V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V, $\overline{CE_1}$ or $\overline{CE_2}$ = "1"		8		pF

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{AA}	Address to Output	C_L = 30pF		30	40	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		15	20	ns

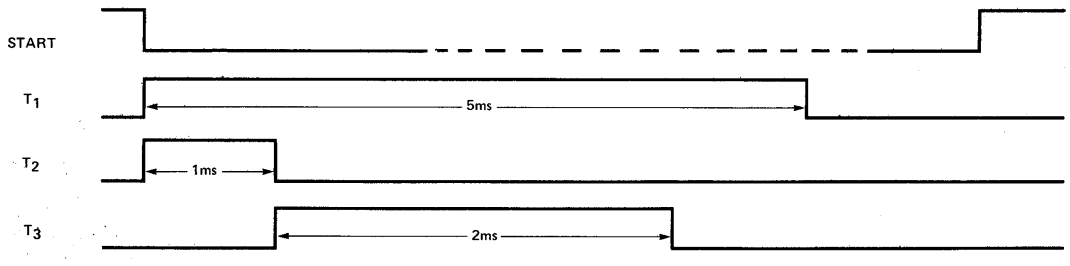
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

MANUAL PROGRAMMER



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TIMING SEQUENCE



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^{\circ}C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 300 \pm 50mA$ (Transient or steady state)	5.0		5.25	V
V_{CCH}	Upper Verify Limit		5.0	5.25	5.5	V
V_{CCL}	Lower Verify Limit		4.5	4.75	5.0	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm 0.25V$	250	300	350	mA
Input Voltage						
V_{IH}	Logical "1" (Except $\overline{CE_1}$)		3.0		5.0	V
V_{IN}	Program Level ($\overline{CE_1}$ Only)		14.0	14.5	15.0	V
V_{IL}	Logical "0"		0	0.4	0.5	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +3.0V$			100	μA
I_{IL}	Logical "0"	$V_{IL} = +0.5V$			-1.6	mA
I_{IN}	Program Level ($\overline{CE_1}$ Only)	$V_{IN} = +15.0V$			15	mA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 115 \pm 10mA$ (Transient or steady state)	16.5	17.0	17.5	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17.0 \pm 0.5V$	105	115	125	mA
T_R[5]	Output Pulse Rise Time		0.2		0.5	μs
t_P	Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10kΩ resistor to V_{CC}.

c. Set $\overline{CE_2}$ to logic "0".

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to $\overline{CE_1}$ (pin 13) a voltage source of 14.5 ± 0.5V, with 15mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 0.5V to the output to be programmed. The source must have a current limit of 115mA. Program one output at the time.

Step 4 After 10μs delay, remove +17.0V supply from programmed output.

Step 5 To verify programming, after 10μs delay, return $\overline{CE_1}$ to 0V. Raise V_{CC} to $V_{CCH} = +5.25 \pm .25V$. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.75 \pm .25V$, and verify that the programmed output remains in the "1" state.

Step 6 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 5 to program other bits at the same address.

Step 7 Repeat steps 1 through 6 to program all other address locations.

NOTES:

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period ($V_{CC} = 0V$) of 4ms.
5. Measured with a 1k dummy load connected across the fusing source.

DESCRIPTION

The 82S100 (Tri-State Outputs) and the 82S101 (Open Collector Outputs) are Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 output functions. Each output function can be programmed either true active-High (Fp), or true active-Low ($F\overset{*}{p}$). The true state of the output functions is controlled via an output Sum (OR) Matrix by a logical combination of 16-input variables, or their complements, up to 48 terms.

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include a chip-enable clocking input for output deskewing and inhibit. They feature either Open Collector or Tri-State outputs for ease of expansion of product terms and/or input variables.

FEATURES

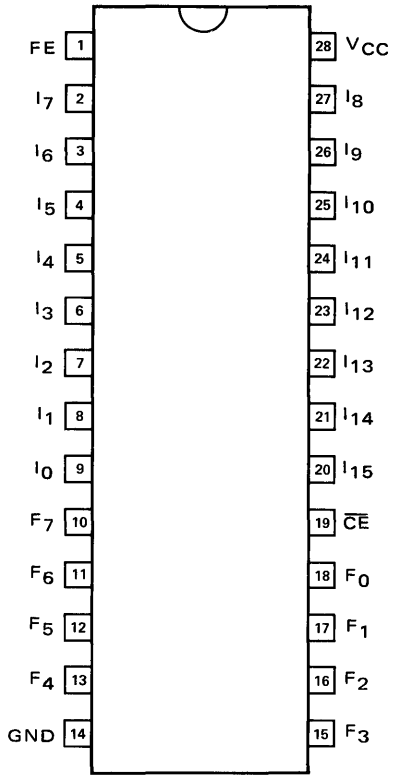
- FIELD PROGRAMMABLE (Ni-Cr LINK)
- INPUT VARIABLES – 16
- OUTPUT FUNCTIONS – 8
- PRODUCT TERMS – 48
- ADDRESS ACCESS TIME – 50ns, MAXIMUM
- POWER DISSIPATION – 600mW, TYPICAL
- INPUT LOADING – (–100μA), MAXIMUM
- OUTPUT OPTION:
  TRI-STATE OUTPUTS – 82S100
  OPEN COLLECTOR OUTPUTS – 82S101
- OUTPUT DISABLE FUNCTION:
  TRI-STATE – Hi-Z
  OPEN COLLECTOR – Hi
- CERAMIC DIP

APPLICATIONS

LARGE READ ONLY MEMORY
RANDOM LOGIC
CODE CONVERSION
PERIPHERAL CONTROLLERS
LOOK-UP AND DECISION TABLES
MICROPROGRAMMING
ADDRESS MAPPING
CHARACTER GENERATORS
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION

I PACKAGE



TRUTH TABLE

LET:

$P_n = \Pi_0^{15} (k_m I_m + j_m \overline{I_m})$; k = 0, 1, X (Don't Care)

n = 0, 1, 2, ... , 47

where:

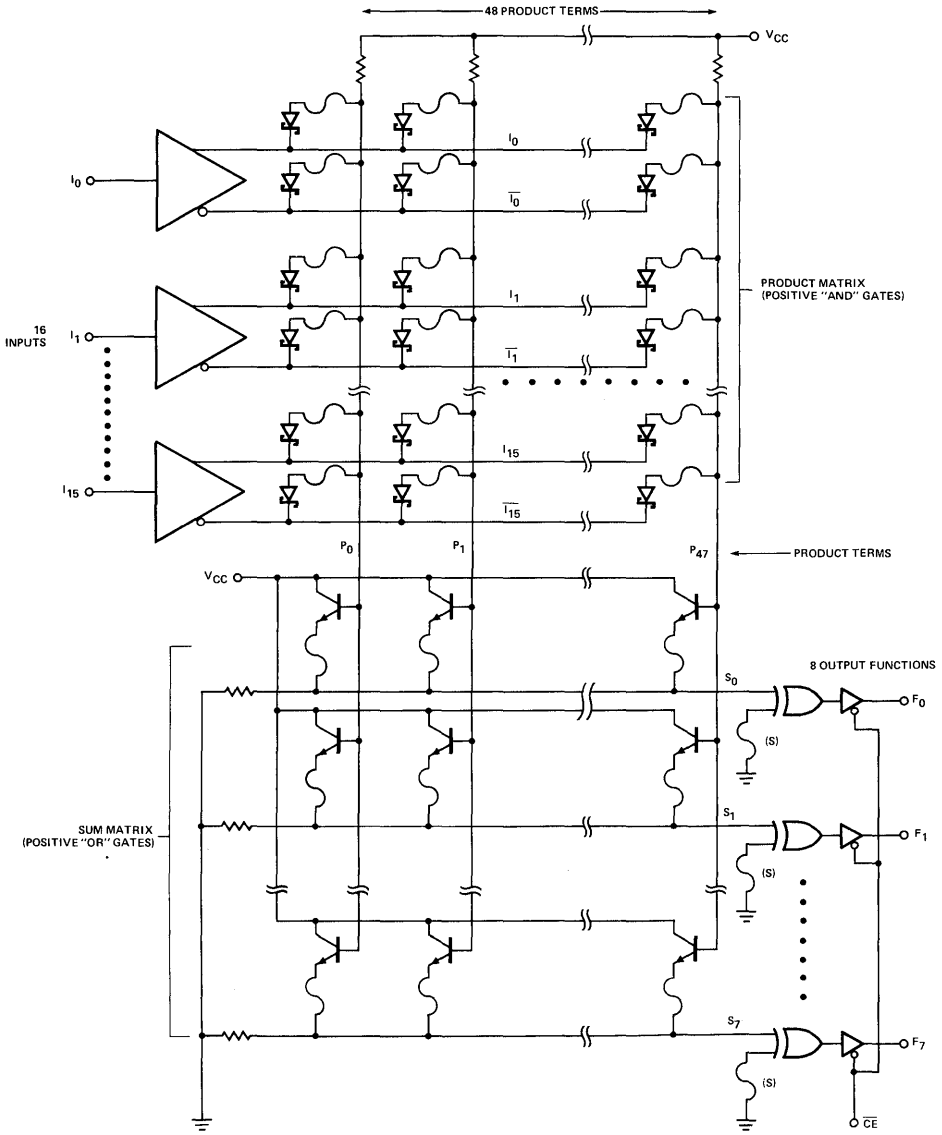
Unprogrammed state : $j_m = k_m = 0$

Programmed state : $j_m = \overline{k_m}$

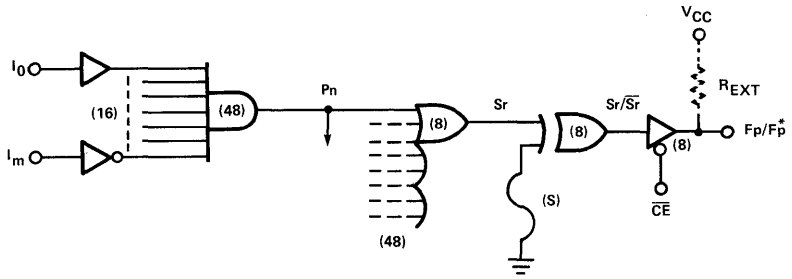
$S_r = f(\Sigma_0^{47} P_n)$; r ≡ p = 0, 1, 2, ... , 7

MODE	P_n	$\overline{CE}$	F_p	F_p^*	$S_r \overset{?}{=} f(P_n)$
Disabled (82S101)	X	1	1	1	X
Disabled (82S100)			Hi-Z	Hi-Z	
Read	1	0	1	0	YES
	0	0	0	1	
	X	0	0	1	NO

BLOCK DIAGRAM



FPLA TYPICAL LOGIC PATH



NOTE:
FOR EACH OF THE 8 OUTPUTS, EITHER THE FUNCTION Fp (ACTIVE HIGH) OR F_p^* (ACTIVE LOW) IS AVAILABLE, BUT NOT BOTH. THE REQUIRED FUNCTION POLARITY IS USER PROGRAMMABLE VIA FUSE (S).

$Pn = I_0 \overline{I_1}\,\overline{I_2}\,I_3 \ldots\ldots \overline{I_m}$

$Sr = P_0 + P_1 + P_2 + \ldots\ldots Pn$

$\overline{Sr} = \overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2} \bullet \ldots\ldots \overline{Pn}$

$Fp = (\overline{CE}) + (Sr) = (\overline{CE}) + (P_0 + P_1 + P_2 + \ldots\ldots Pn)$ @ S = SHORT

$F_p^* = (\overline{CE}) + (\overline{Sr}) = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2} \bullet \ldots\ldots \overline{Pn})$ @ S = OPEN

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S101)	+5.5	Vdc
V_O	Off-State Output Voltage (82S100)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C; 4.75V \leqslant V_{CC} \leqslant 5.25V$

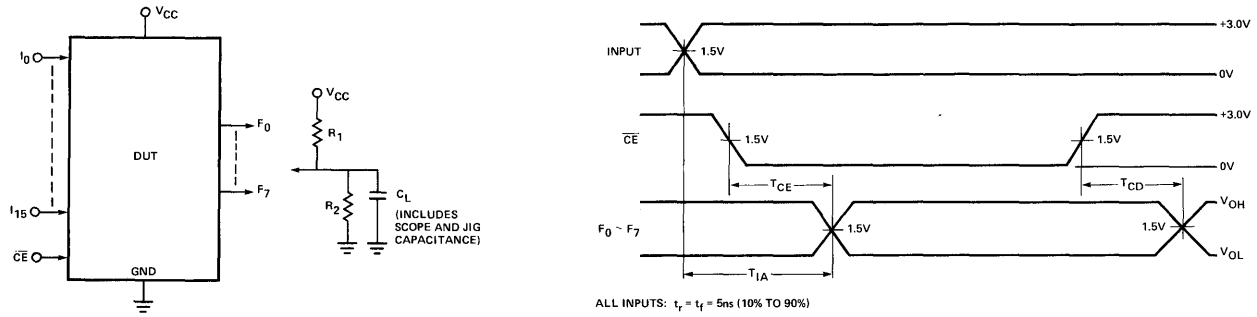
PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT	NOTES
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.8	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −18mA			−0.8	−1.2	V	1, 7
V_{OH}	High-Level Output Voltage (82S100)	V_{CC} = 4.75V, I_{OH} = −2mA		2.4			V	1, 5
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 9.6mA			0.35	0.45	V	1, 8
I_{OLK}	Output Leakage Current (82S101)	V_{CC} = 5.25V	V_{OUT} = 5.25V		1	40	μA	6
$I_{O(OFF)}$	Hi-Z State Output Current (82S100)		V_{OUT} = 5.25V		1	40	μA	6
			V_{OUT} = 0.45V		−1	−40	μA	6
I_{IH}	High-Level Input Current	V_{IN} = 5.5V			<1	25	μA	
I_{IL}	Low-Level Input Current	V_{IN} = 0.45V			−10	−100	μA	
I_{OS}	Short-Circuit Output Current (82S100)	V_{CC} = 5.25V, V_{OUT} = 0V		−20		−70	mA	3, 7
I_{CC}	V_{CC} Supply Current (82S100, 82S101)	V_{CC} = 5.25V			120	170	mA	4
C_{IN}	Input Capacitance	V_{CC} = 5.0V	V_{IN} = 2.0V		5		pF	
C_O	Output Capacitance		V_{OUT} = 2.0V		8		pF	6

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of short circuit should not exceed one second.
4. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each output one at the time.
8. Measured with a programmed logic condition for which the output under test is at a "0" logic level. Output sink current is supplied thru a resistor to V_{CC}.

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{IA}	Input to Output	C_L = 30pF		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600		15	20	ns

AC TEST FIGURE AND WAVEFORM



NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, and T_A = +25°C.

OBJECTIVE PROGRAMMING PROCEDURE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

A. All internal Ni-Cr links are intact.

B. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "FALSE").

C. The Sum Matrix contains all 48 P-terms.

D. The polarity of each output is set to active HIGH (F_p function).

E. All outputs are at a LOW logic level.

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the Product Matrix, Sum Matrix, and Output Polarity outlined below.

OUTPUT POLARITY

PROGRAM ACTIVE LOW (F_p^* Function)

Program output polarity before programming Product Matrix and Sum Matrix. Program one output at the time.

1. Set GND (pin 14) to OV.
2. Do not apply power to the device (V_{CC}, pin 28, open).
3. Apply V_{OUT} = +18V to the appropriate output for 1ms, and return to OV.
4. Repeat step 3 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to LOW logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a HIGH logic level are programmed active HIGH (F_p function), while all outputs at a LOW logic level are programmed active LOW (F_p^* function).
5. Remove V_{IN} = +10V from inputs I_0 through I_{15}.

PRODUCT MATRIX

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to HIGH logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to

outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage to I_0 from V_{IN} = +10V to a LOW logic level. Execute step 6.

6a. After 10μs delay, raise FE (pin 1) from 0V to +17V. The source must have a current limit of 250mA, and rise time of 10 to 50μs.

6b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

6c. After 10μs delay, return FE input to 0V.

7. Return input I_0 to a disable state by applying V_{IN} = +10V.

8. Repeat steps 5 through 7 for all other input variables.

9. Repeat steps 4 through 8 for all other P-terms.

10. Remove V_{IN} = +10V from all input variables.

VERIFY INPUT VARIABLE

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.

2. Enable F_7 output by setting $\overline{CE}$ to +10V.

3. Disable input variables by applying V_{IN} = +10V to inputs I_0 through I_{15}.

4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to outputs F_0 through F_5.

5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level, and sense the state of output F_7.
   B. Lower the input voltage to I_0 from a HIGH to a LOW logic level, and sense the logic state of output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	Input Variable State Contained In P-Term
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Dont Care
0 1	0 0	(I_0), ($\overline{I_0}$)

Note that two tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Return input I_0 to a disable state by applying V_{IN} = +10V.

7. Repeat steps 5 and 6 for all other input variables.

8. Repeat steps 4 through 7 for all other P-terms.

9. Remove V_{IN} = +10V from all input variables.

SUM MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links of unused P-terms in the Sum Matrix are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Disable the chip by setting $\overline{CE}$ (pin 19) to a HIGH logic level.

3. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB. Use standard TTL levels.

4a. If the P-term is contained in output function F_0 (F_0 = 1 or F_0^* = 0), go to step 6.

4b. If the P-term **is not** contained in output function F_0 (F_0 = 0 or F_0^* = 1), set to fuse the P_n link by applying V_{OUT} = +10V to output F_0.

5a. After 10μs delay, raise FE (pin 1) from 0V to +17V.

5b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

5c. After 10μs delay, return FE input to 0V.

6. Repeat steps 4 and 5 for all other output functions.

7. Repeat steps 3 through 6 for all other P-terms.

8. Remove +8.5V from V_{CC}.

VERIFY PRODUCT TERM

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Enable the chip by setting $\overline{CE}$ (pin 19) to a LOW logic level.

3. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as the LSB. Use standard TTL levels.

4. To determine the status of the P_n link in the Sum Matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

Output		P-term Link
Active HIGH (F_p)	Active LOW (F_p^*)	
0	1	FUSED
1	0	PRESENT

5. Repeat steps 3 and 4 for all other P-terms.

6. Remove +8.5V from V_{CC}.

DESCRIPTION

The 82S114 and 82S115 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S114 and 82S115 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S114 and 82S115 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines. In the LATCHED READ mode, after the desired address is applied and both $\overline{CE1}$ and CE2 are enabled, data will enter the output latches following the positive transition of STROBE, and the data out lines will be locked into their last valid state following the negative transition of STROBE. The latches will remain set and the outputs enabled until the chip is disabled and STROBE is brought high.

Both 82S114 and 82S115 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S114/115, I.

FEATURES

- ORGANIZATION:
  - 82S114 – 256 X 8
  - 82S115 – 512 X 8
- ADDRESS ACCESS TIME – 60ns, MAXIMUM
- POWER DISSIPATION – 165μW/BIT, TYPICAL
- INPUT LOADING – (–100μA), MAXIMUM
- ON-CHIP ADDRESS DECODING
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS
- FAST PROGRAMMING – 5 SEC., MAXIMUM
- PIN COMPATIBLE TO N8204/N8205 ROMs

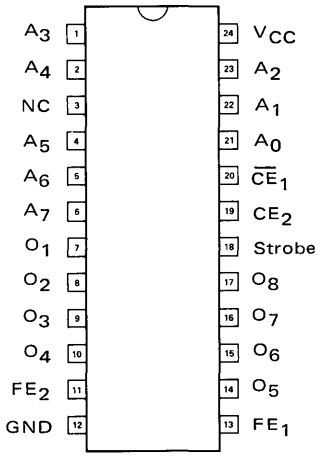
APPLICATIONS

MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

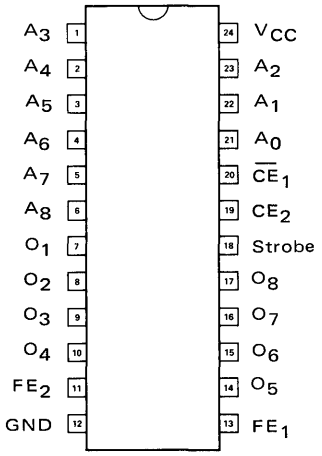
PIN CONFIGURATION

I PACKAGE*

82S114

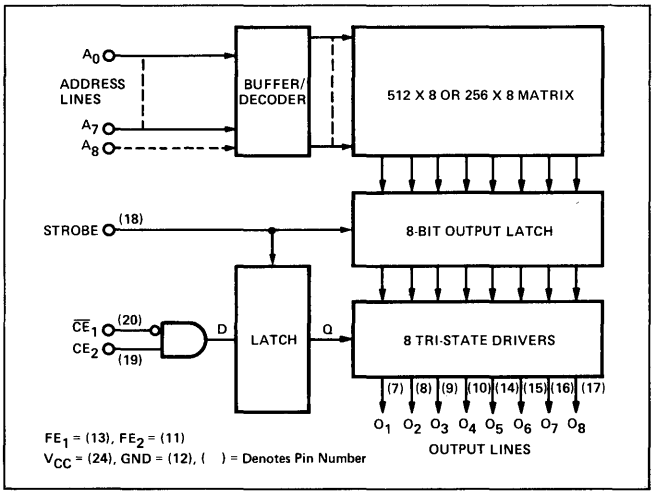


82S115



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER		TEST CONDITIONS	LIMITS[1]			UNIT
			MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25	μA
V_{IL}	"0" Level Input Voltage				.85	V
V_{IH}	"1" Level Input Voltage		2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6 mA			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE_1}$ = "0", CE_2 = "1", I_{OUT} = −2 mA, "1" STORED	2.7	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 5.5V			40	μA
		$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			−40	μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V, $\overline{CE_1}$ = "1" or CE_2 = 0		8		pF
I_{CC}	V_{CC} Supply Current			135	185	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	mA

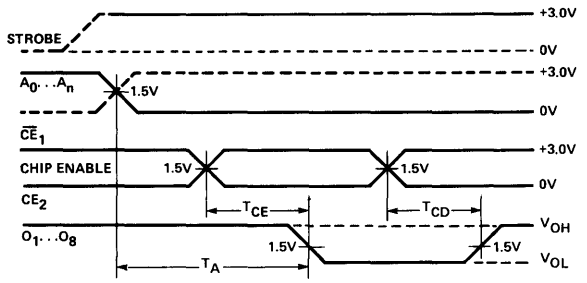
SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60	ns
T_{CE}	Chip Enable Access Time	R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 4)		20	40	ns
T_{CD}	Chip Disable Time			20	40	ns
T_{ADH}	Address Hold Time	LATCHED READ ONLY R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 5)	0	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		ns
T_{SW}	Strobe Pulse Width		30	20		ns
T_{SL}	Strobe Latch Time		60	35		ns
T_{DL}	Strobe Delatch Time				30	ns
T_{CDS}	Chip Enable Set-up Time		40			ns

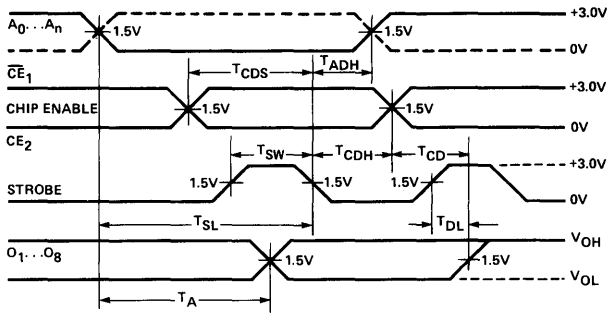
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25° C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

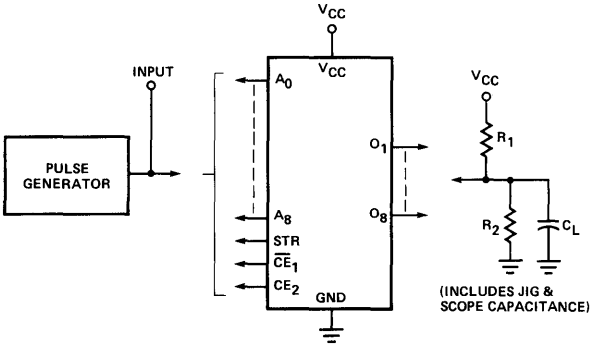
TRANSPARENT READ[5]
(Output Latches Not Used)



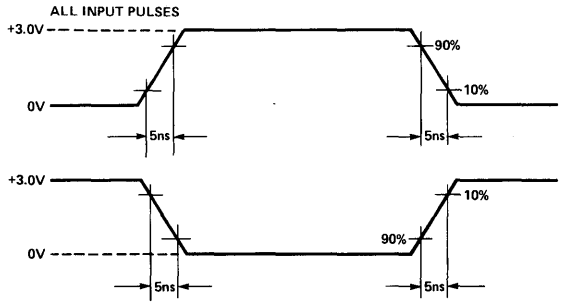
LATCHED READ[6]
(Output Latches Used)



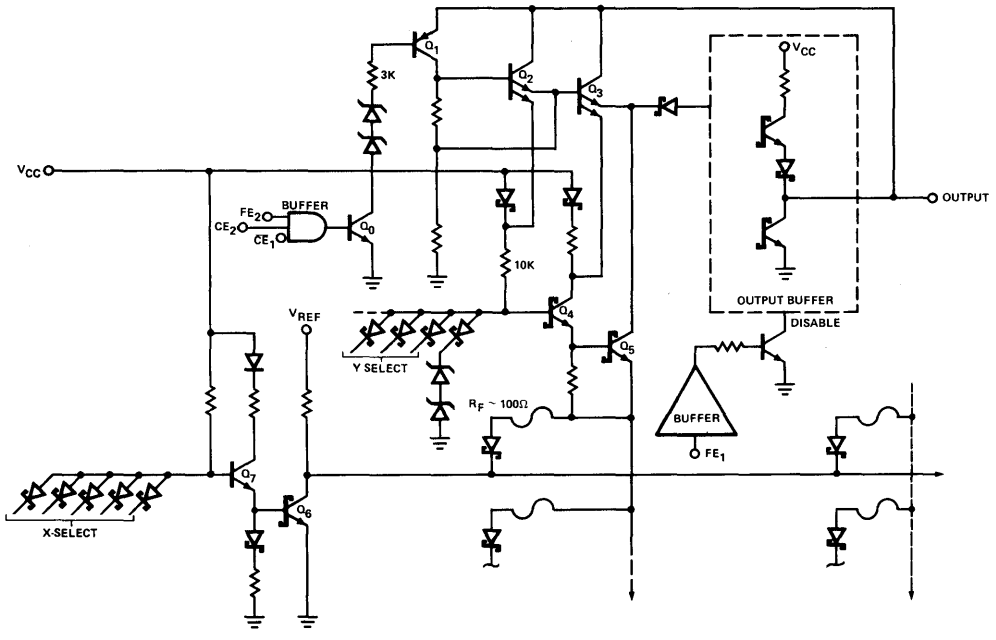
AC TEST LOAD AND WAVEFORMS



INPUT PULSES



TYPICAL FUSING PATH



RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10KΩ resistor to V_{CC}.

c. Set $\overline{CE}$ 1 to logic "0", and CE2 to logic "1" (TTL levels).

d. Set Strobe to logic "1" level.

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to FE1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10 mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit of 200 mA. Program one output at the time.

Step 4 After 10μs delay, raise FE2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10 mA sourcing current capability.

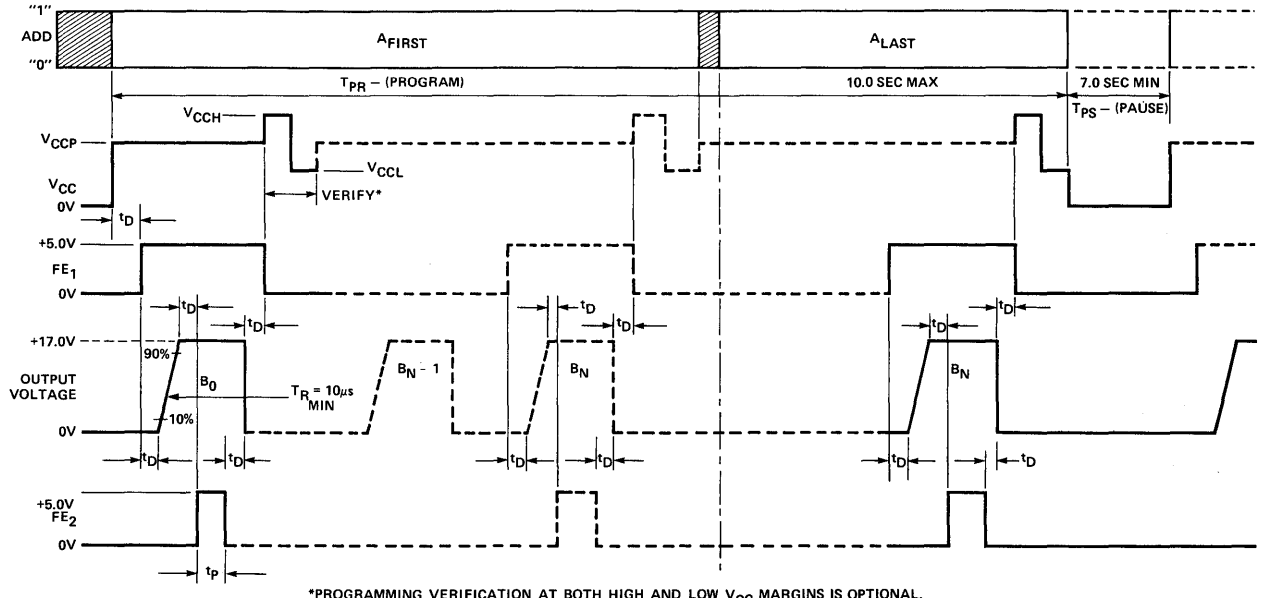
Step 5 After 10μs delay, remove +17.0V supply from programmed output.

Step 6 To verify programming, after 10μs delay, return FE1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.

Step 7 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 6 to program other bits at the same address.

Step 8 Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



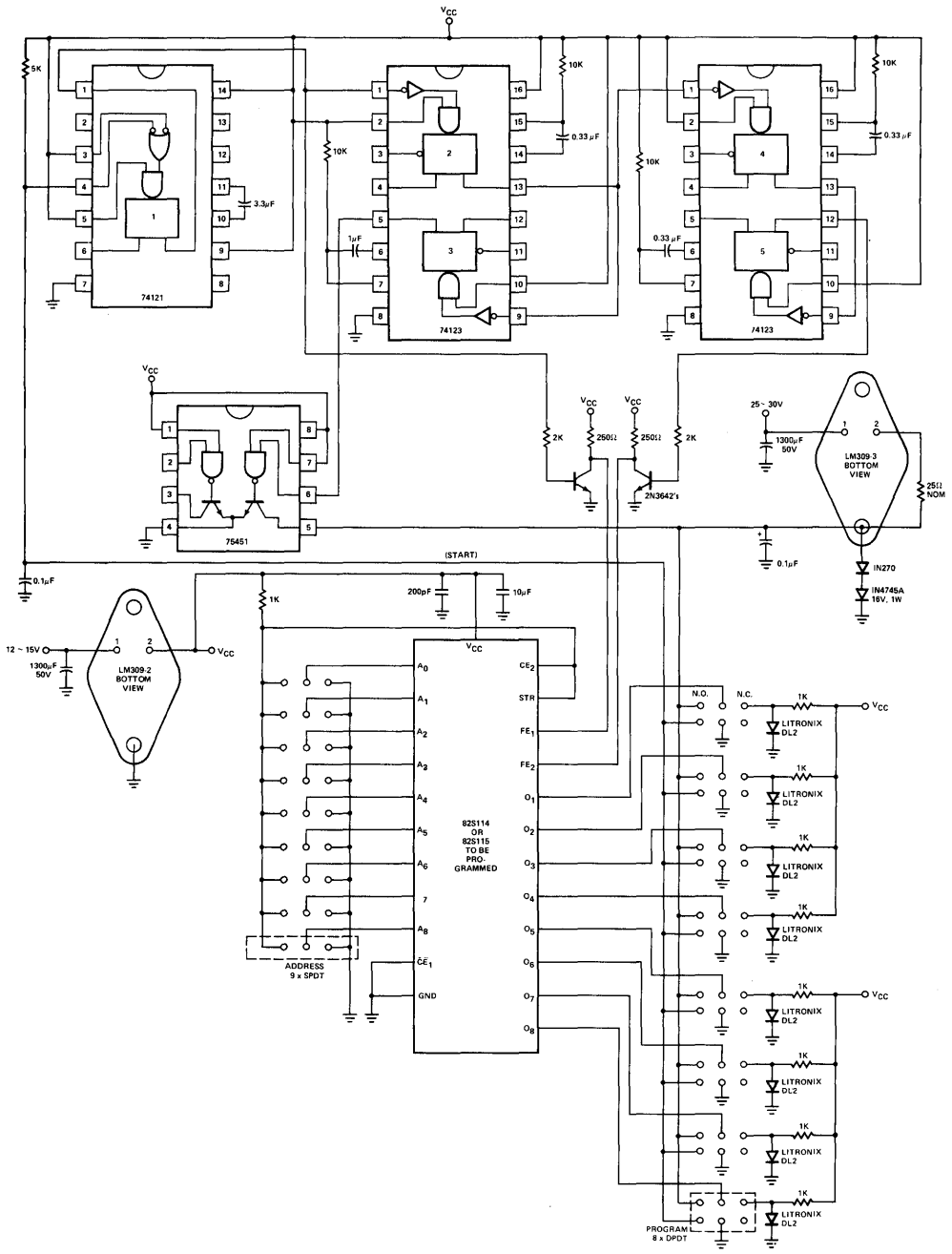
*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

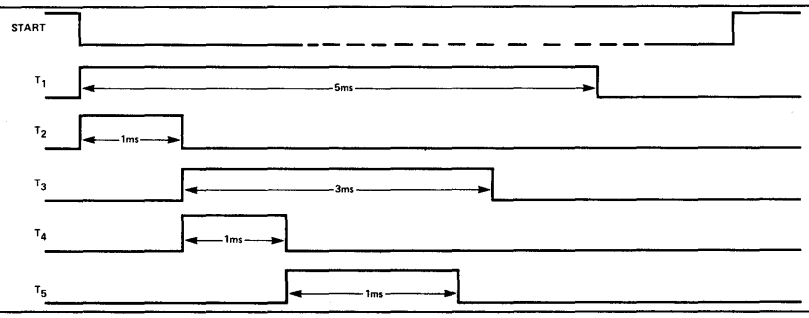
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 200 \pm 25$ mA (Transient or steady state)	4.75	5.0	5.25	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm .25$V	175	200	225	mA
Input Voltage						
V_{IL}	Low Level Input Voltage		0	0.4	0.8	V
V_{IH}	High Level Input Voltage		2.4		5.5	V
Input Current (FE_1 & FE_2 Only)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45$V			−100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5$V			10	mA
Input Current (Except FE_1 & FE_2)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45$V			−100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5$V			25	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20$ mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1$V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	FE_2 Programming Pulse Width		1		1.5	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			10	sec
T_{PS}	Programming Pause	$V_{CC} = 0$V	7			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				60	%

NOTES:
1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0$V) of 3 mS.

82S114/115 MANUAL PROGRAMMER



TIMING SEQUENCE



signetics

256-BIT BIPOLAR RAM (256x1 RAM) (82S116 TRI-STATE) (82S117 OPEN COLLECTOR)

82S116
82S117

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S116 and 82S117 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and -100μA for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S116 and 82S117 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S116/117, B or F.

FEATURES

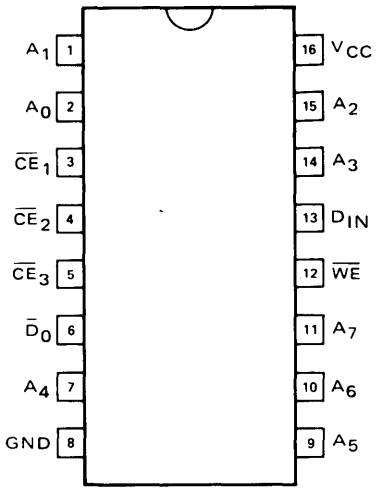
- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME – 40ns, MAXIMUM
- WRITE CYCLE TIME – 25ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING – (-100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - TRI-STATE – 82S116
  - OPEN COLLECTOR – 82S117
- 16 PIN CERAMIC DIP

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



*B – Plastic
C – Cerdip

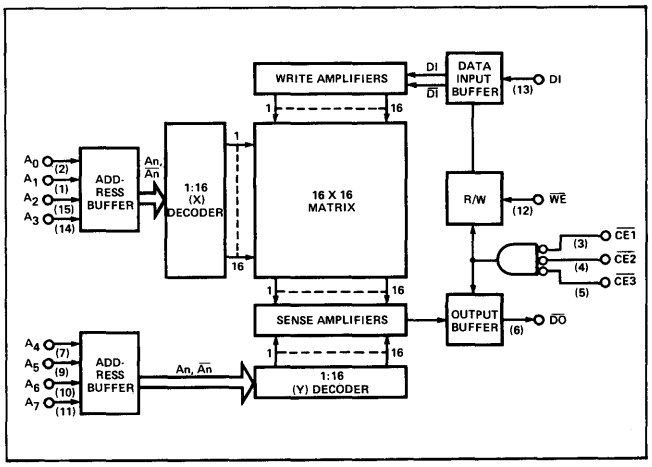
TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S116	82S117
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S117)	+5.5	Vdc
V_O	Off-State Output Voltage (82S116)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS		LIMITS			UNIT	NOTES
				MIN	TYP[2]	MAX		
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2.0			V	
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.85	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −12 mA			−1.0	−1.5	V	1,8
V_{OH}	High-Level Output Voltage (82S116)	V_{CC} = 4.75V, I_{OH} = −3.2 mA		2.6			V	1,6
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 16 mA			0.35	0.45	V	1,7
I_{OLK}	Output Leakage Current (82S117)	V_{OUT} = 5.5V			1	40	μA	5
$I_{O(OFF)}$	HI-Z State Output Current (82S116)	V_{OUT} = 5.5V			1	40	μA	5
		V_{OUT} = 0.45V			−1	−40	μA	5
I_{IH}	High-Level Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = 5.25V, V_{IN} = 0.45V			−10	−100	μA	8
I_{OS}	Short-Circuit Output Current (82S116)	V_{CC} = 5.25V, V_O = 0V		−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S116)	V_{CC} = 5.25V			80	115	mA	4
	V_{CC} Supply Current (82S117)	V_{CC} = 5.25V			80	115	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8		pF	

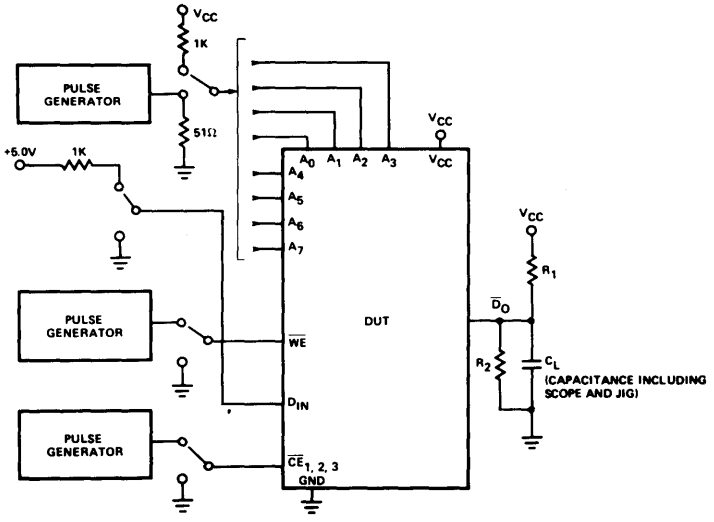
NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

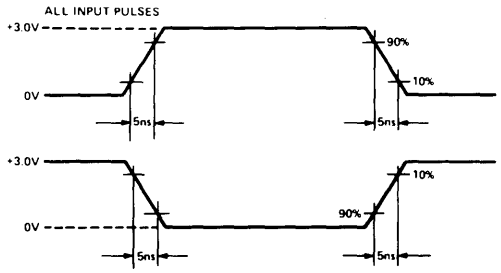
PARAMETER		TEST CONDITIONS	LIMITS			UNIT	NOTE
			MIN	TYP[1]	MAX		
Propagation Delays							
T_{AA}	Address Access Time	$R_1 = 270\Omega$ $R_2 = 600\Omega$ $C_L = 30pF$		30	40	ns	
T_{CE}	Chip Enable Access Time			15	25	ns	
T_{CD}	Chip Enable Output Disable Time			15	25	ns	
T_{WD}	Write Enable to Output Disable Time			30	40	ns	
Write Set-up Times							
T_{WSA}	Address to Write Enable		0	-5		ns	
T_{WSD}	Data In to Write Enable		25	15		ns	
T_{WSC}	$\overline{CE}$ to Write Enable		0	-5		ns	
Write Hold Times							
T_{WHA}	Address to Write Enable		0	-5		ns	
T_{WHD}	Data In to Write Enable		0	-5		ns	
T_{WHC}	$\overline{CE}$ to Write Enable		0	-5		ns	
T_{WP}	Write Enable Pulse Width		25	15		ns	2

AC TEST LOAD

LOADING CONDITION



INPUT PULSES



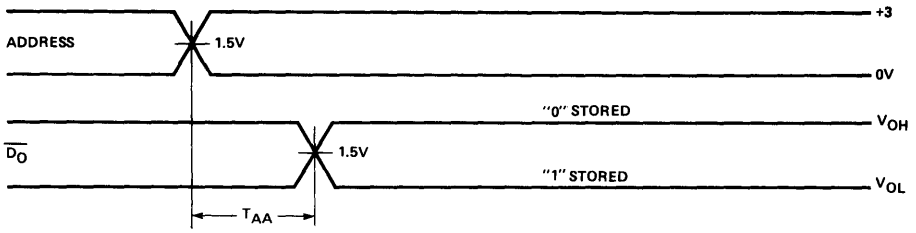
MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

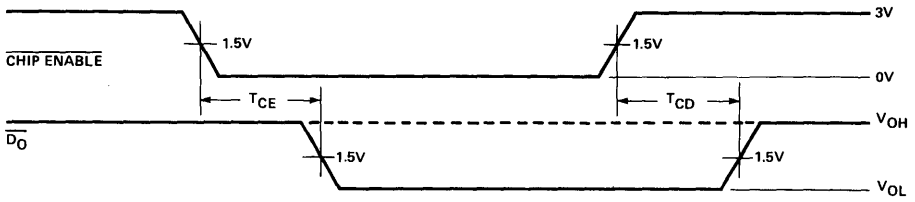
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

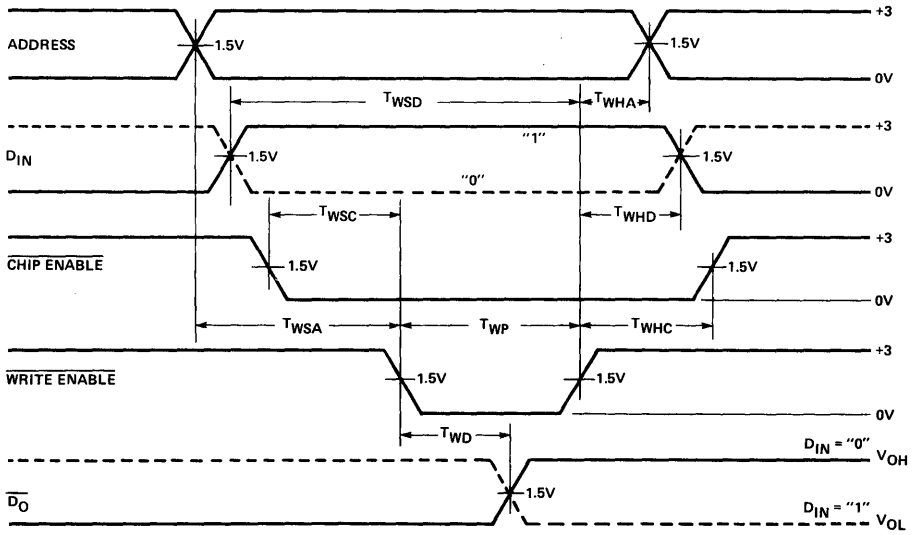
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

signetics

1024-BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

82S126
82S129

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S126 (Open Collector Outputs) and the 82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S126 and 82S129 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, B or F. For the military temperature range (−55°C to +125°C) specify S82S126/129, F only.

FEATURES

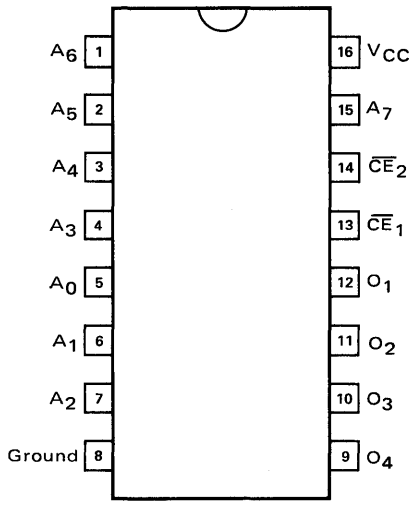
- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME:
  - S82S126/129 – 70ns, MAXIMUM
  - N82S126/129 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT TYPICAL
- INPUT LOADING:
  - S82S126/129 – (−150μA) MAXIMUM
  - N82S126/129 – (−100μA) MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - OPEN COLLECTOR – 82S126
  - TRI-STATE – 82S129
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

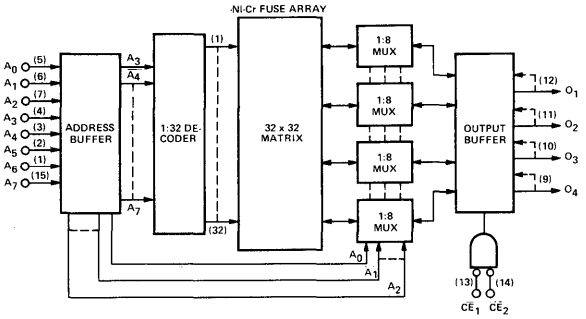
PIN CONFIGURATION

B, F PACKAGE*



*B — Plastic
F — Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S126)	+5.5	Vdc
V_O	Off-State Output Voltage (82S129)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S126/129)	0° to +75°	°C
	(S82S126/129)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S126/S82S129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/N82S129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.5	V
I_{OLK}	Output Leakage Current (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 0.5V			−60			−40	μA
V_{OH}	"1" Output Voltage (82S129)	$\overline{CE}_1$ = $\overline{CE}_2$ = "0", I_{OUT} = −2.0mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			105	125		105	120	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S129)	V_{OUT} = 0V	−15		−85	−20		−70	mA

SWITCHING CHARACTERISTICS

S82S126/129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF, R_1 = 270Ω, R_2 = 600Ω		35	70		35	50	ns
T_{CD}	Chip Disable to Output			15	35		15	20	ns
T_{CE}	Chip Enable to Output			15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

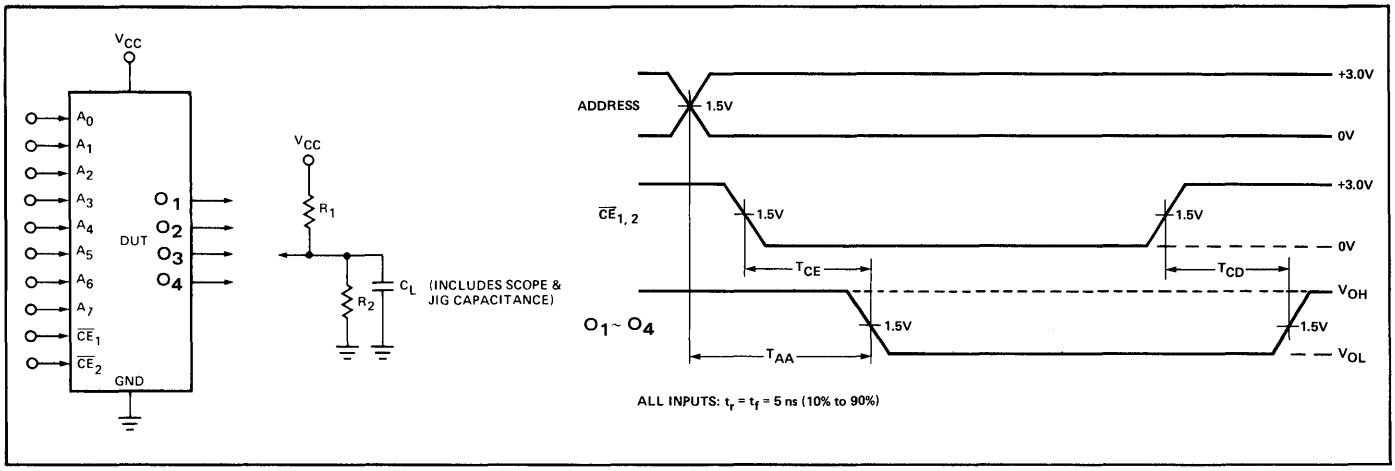
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

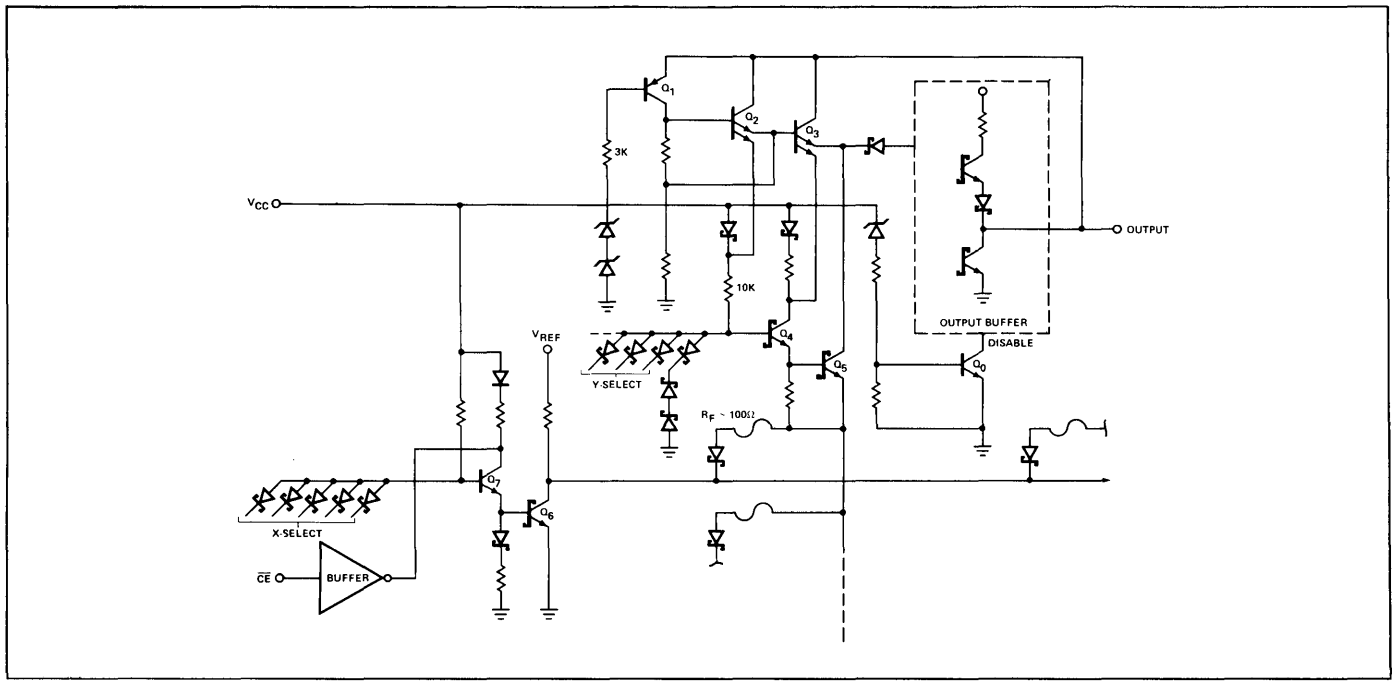
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0V$) of 4ms.

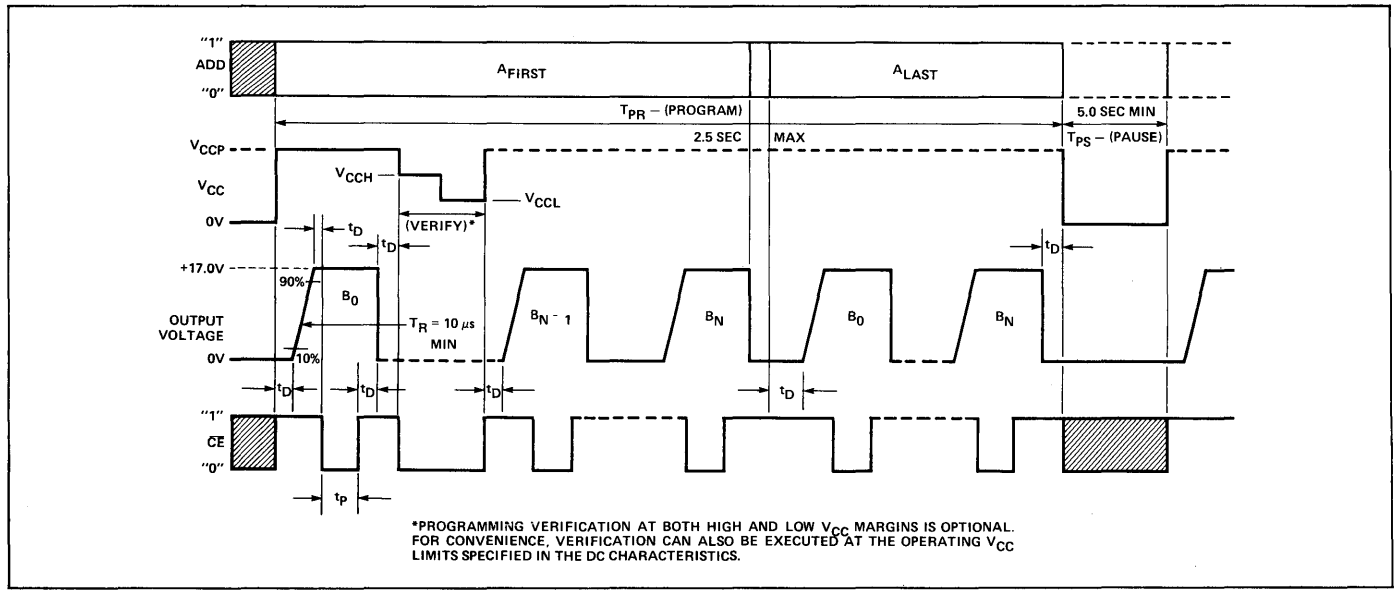
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH

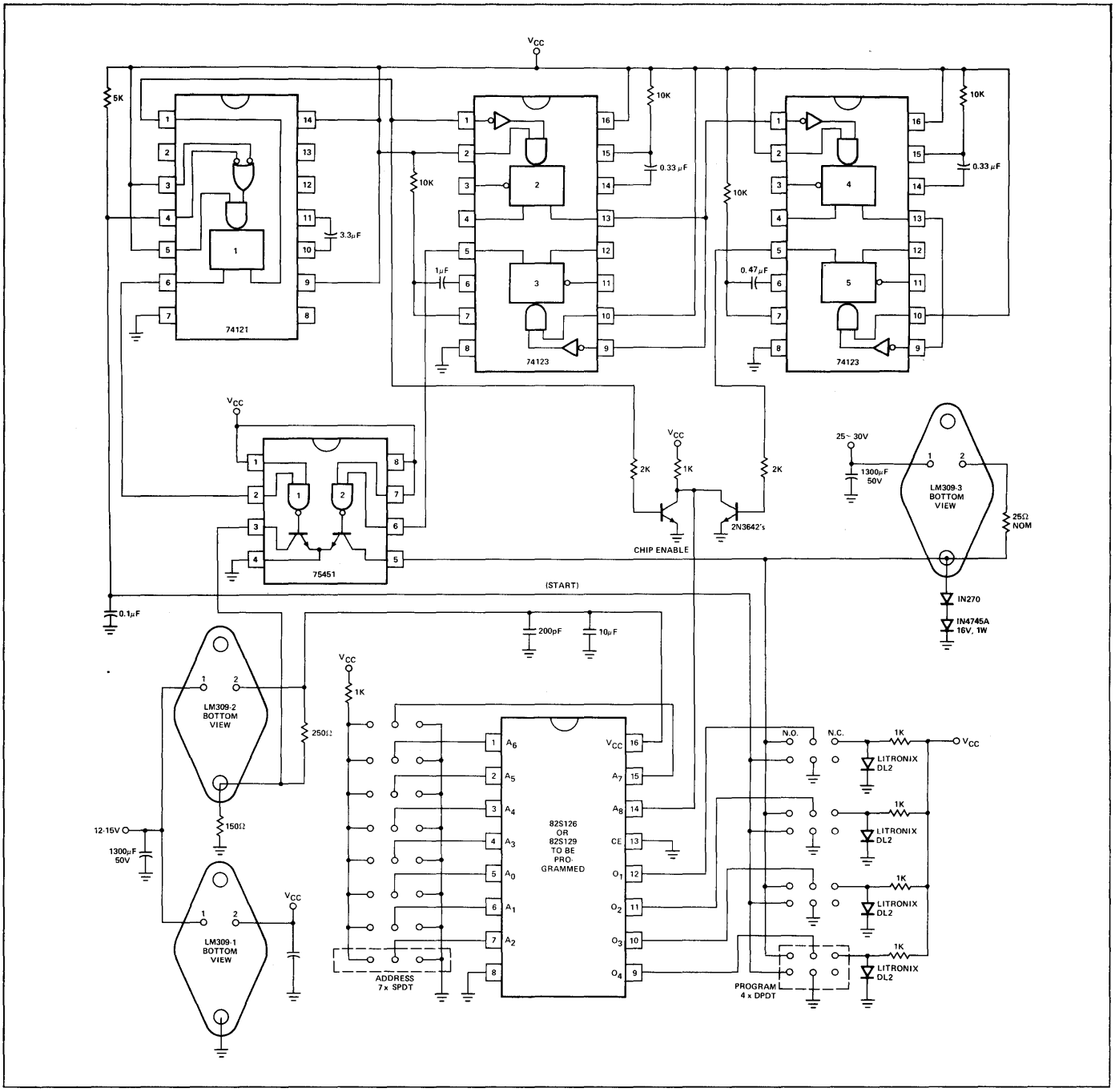


TYPICAL PROGRAMMING SEQUENCE

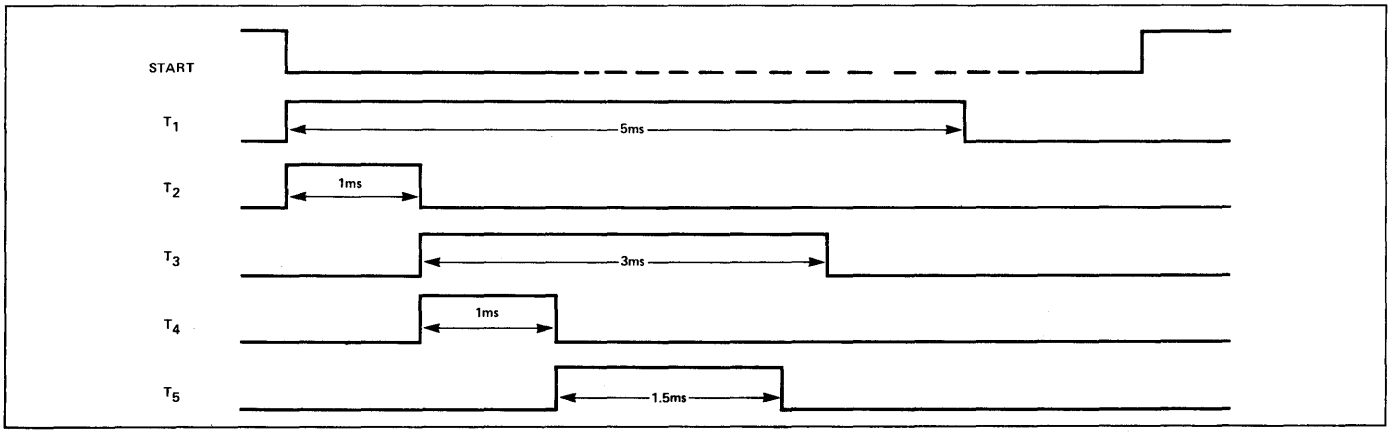


*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

MANUAL PROGRAMMER



TIMING SEQUENCE



DESCRIPTION

The 82S130 (Open Collector Outputs) and the 82S131 (Tri-State Outputs) are Bipolar 2048-Bit Read Only Memories, organized as 512 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S130 and 82S131 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S130/131, F. For the military temperature range (−55°C to +125°C) specify S82S130/131, F.

FEATURES

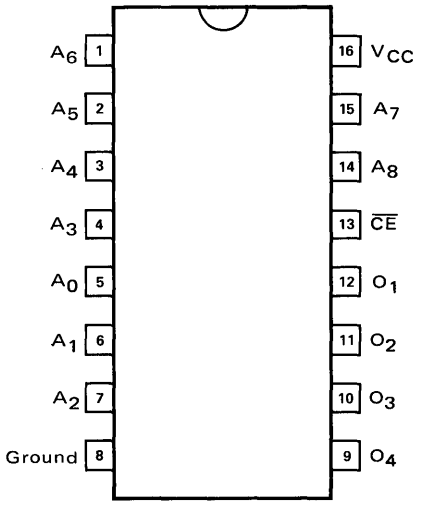
- ORGANIZATION – 512 X 4
- ADDRESS ACCESS TIME:
  S82S130/131 – 70ns, MAXIMUM
  N82S130/131 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.3mW/BIT TYPICAL
- INPUT LOADING:
  S82S130/131 – (−150μA) MAXIMUM
  N82S130/131 – (−100μA) MAXIMUM
- ONE CHIP ENABLE INPUT
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  82S130 – OPEN COLLECTOR
  82S131 – TRI-STATE
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

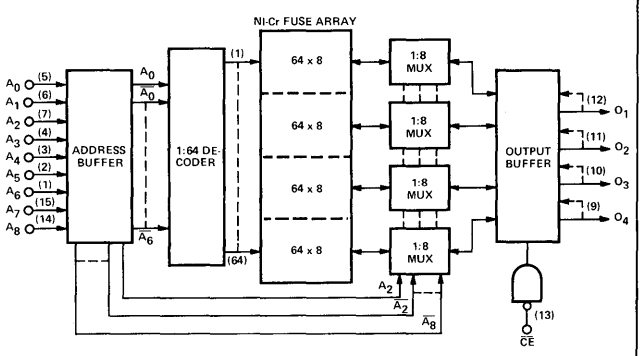
PIN CONFIGURATION

F PACKAGE*



*F – Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S130)	+5.5	Vdc
V_O	Off-State Output Voltage (82S131)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S130/131)	0° to +75°	°C
	(S82S130/131)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S130/131 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S130/131 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S130/131			N82S130/131			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.45	V
I_{OLK}	Output Leakage Current (82S130)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S131)	$\overline{CE}$ = "1", V_{OUT} = 0.5V			−60			−40	μA
		$\overline{CE}$ = "1", V_{OUT} = 5.5V			60			40	μA
V_{OH}	High Level Output Voltage (82S131)	$\overline{CE}$ = "0", I_{OUT} = −2.4mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			120	140		120	140	mA
V_{IC}	Input Clamp Voltage	I_N = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S131)	V_{OUT} = 0V	−15		−85	−20		−70	mA

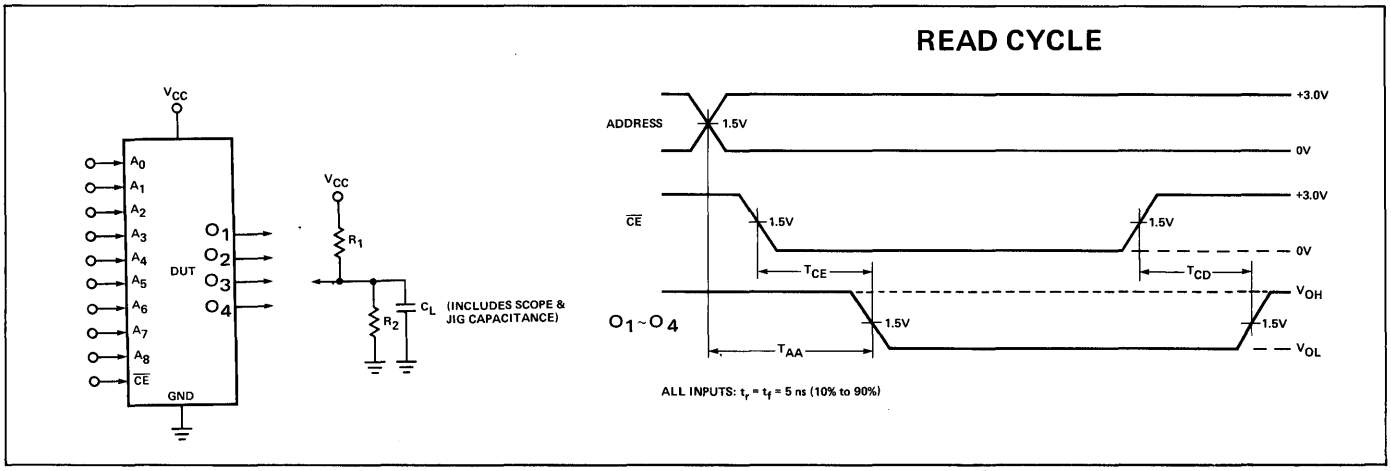
SWITCHING CHARACTERISTICS

S82S130/131 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S130/131 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

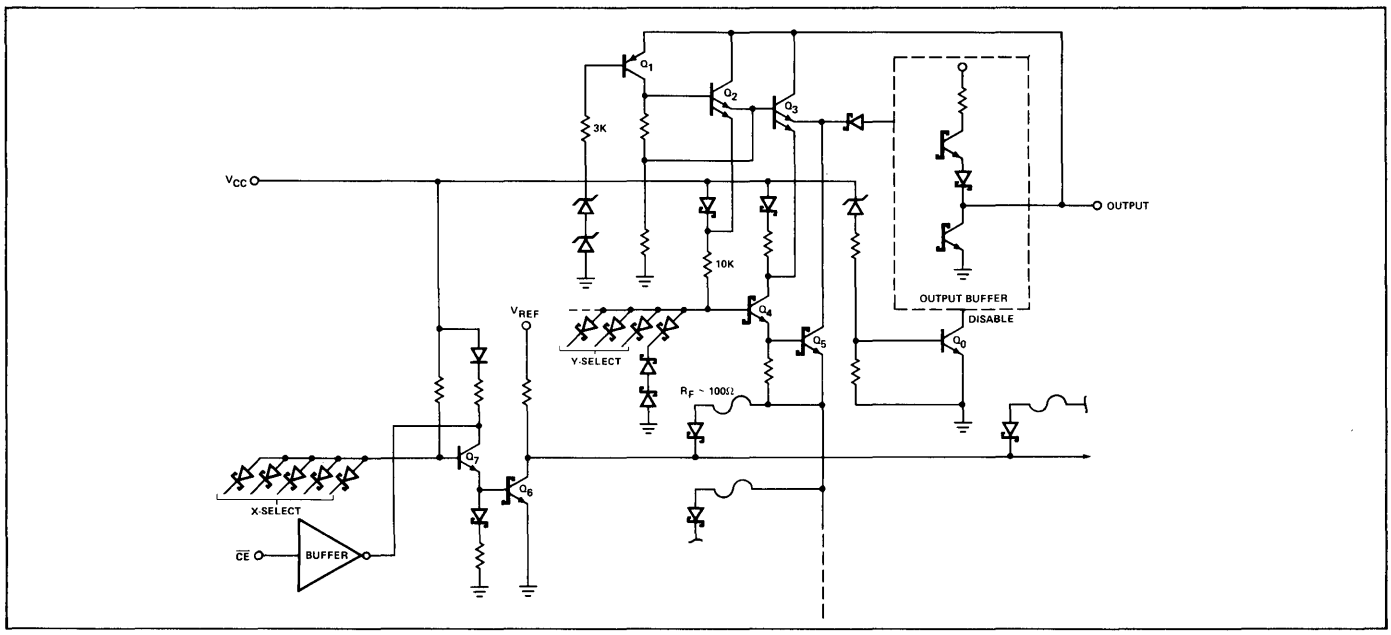
PARAMETER		TEST CONDITIONS[1]	S82S130/131			N82S130/131			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF		40	70		40	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		20	30		20	30	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		20	30		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25° C.

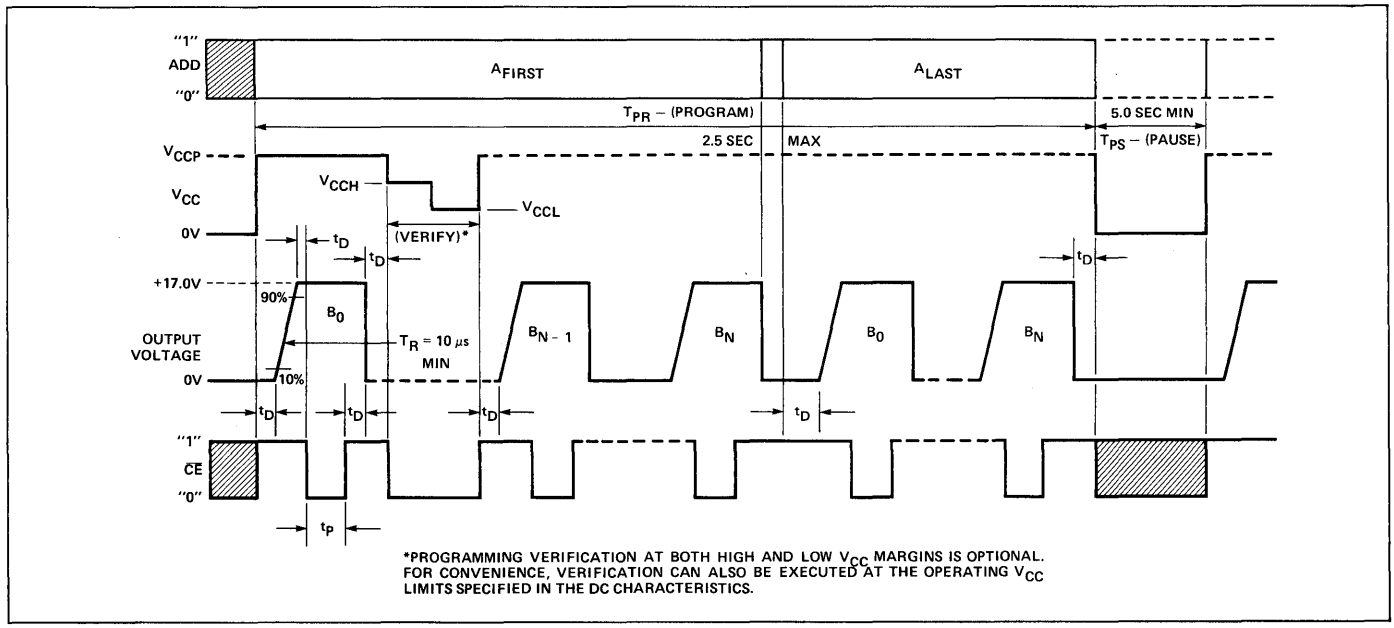
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^{\circ}C$

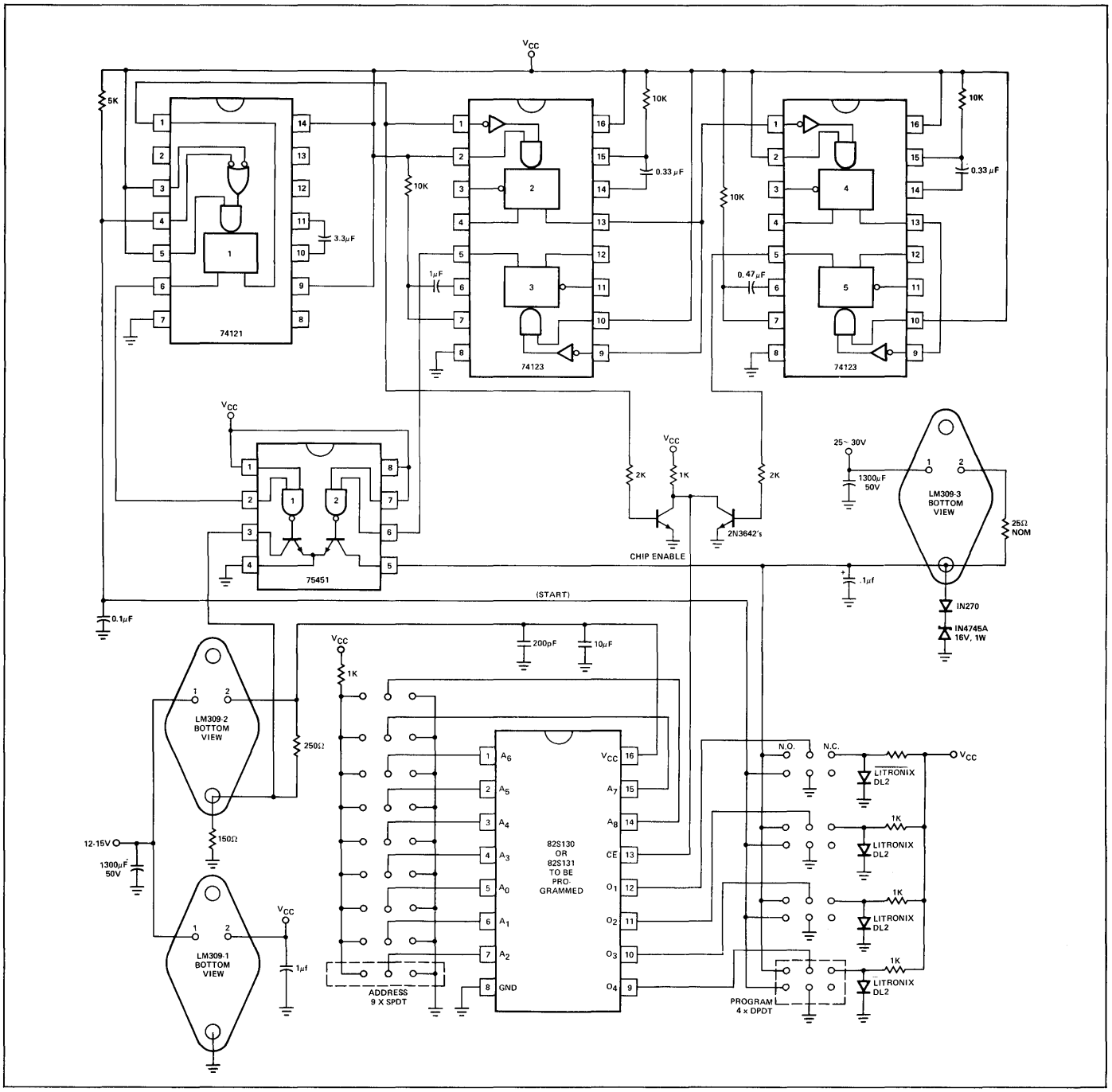
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}[5]	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

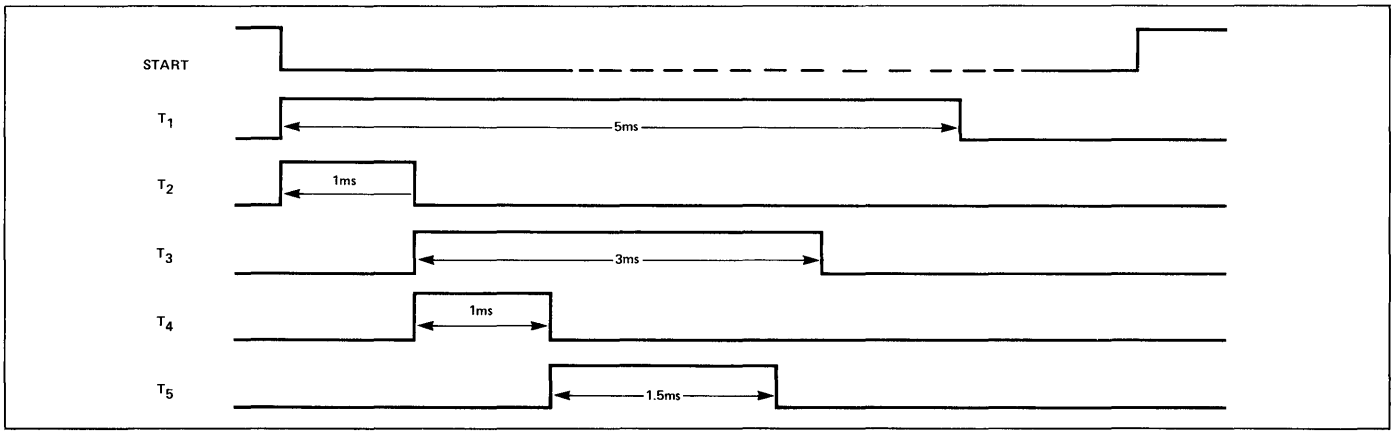
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.

N82S130/131 MANUAL PROGRAMMER



TIMING SEQUENCE



DESCRIPTION

The 82S214 and 82S215 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers.

The 82S214 and 82S215 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizat ons. A D-type latch is used to enable the Tri-State output d ivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or high Z) as long as STROBE is low, regardless of the state of address or chip enable. A positive STROBE transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative STROBE transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S214 and 82S215 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S214/215 I. For the military temperature range (−55°C to +125°C) specify S82S214/215 I.

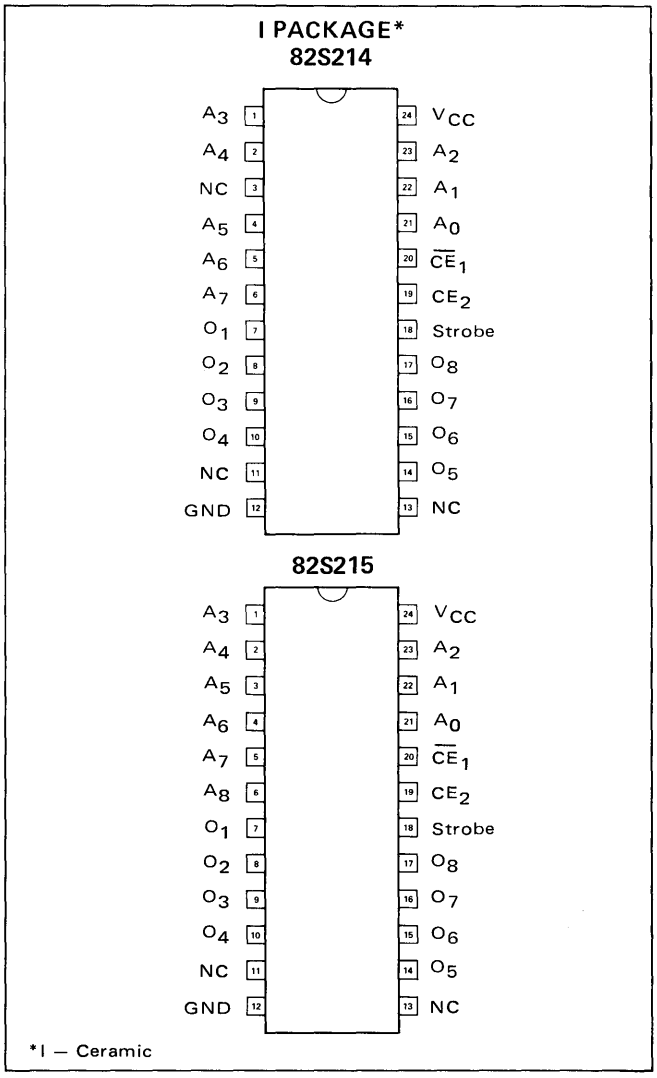
FEATURES

- ORGANIZATION:
  - 82S214 – 256 X 8
  - 82S215 – 512 X 8
- ADDRESS ACCESS TIME:
  - S82S214/215 – 90ns, MAXIMUM
  - N82S214/215 – 60ns, MAXIMUM
- POWER DISSIPATION – 165μW/BIT, TYPICAL
- INPUT LOADING:
  - S82S214/215 – (−150μA) MAXIMUM
  - N82S214/215 – (−100μA) MAXIMUM
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS
- FULLY COMPATIBLE WITH 82S114 AND 82S115 SIGNETICS PROMS

APPLICATIONS

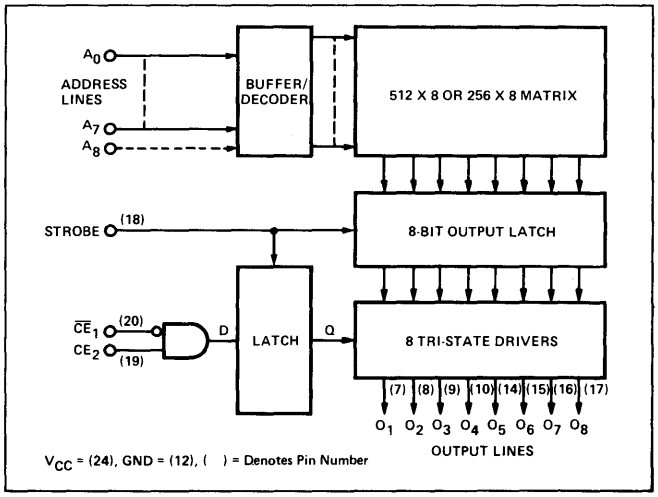
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S214/215)	0° to +75°	°C
	(S82S214/215)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

N82S214/215 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
S82S214/215 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−100			−150	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25			50	μA
V_{IL}	"0" Level Input Voltage				.85			.8	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6mA			0.5			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE}_1$ = "0", CE_2 = "1", I_{OUT} = −2mA, "1" STORED	2.7	3.3		2.4	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE}_1$ = "1" or CE_2 = 0, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE}_1$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			−40			−100	μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V $\overline{CE}_1$ = "1" or CE_2 = 0		8			8		pF
I_{CC}	V_{CC} Supply Current			130	175		130	185	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	−15		−85	mA

SWITCHING CHARACTERISTICS

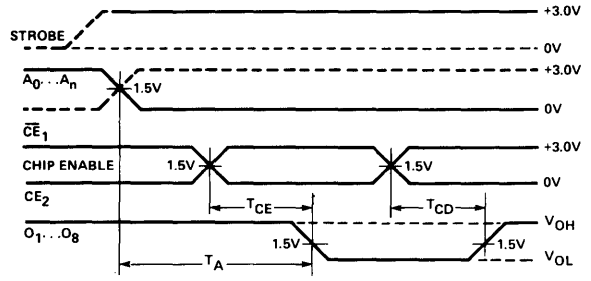
N82S214/215 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
S82S214/215 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60		35	90	ns
T_{CE}	Chip Enable Access Time	R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF (Note 4)		20	40		20	50	ns
T_{CD}	Chip Disable Time			20	40		20	50	ns
T_{ADH}	Address Hold Time		0	−10		5	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		10	0		ns
T_{SW}	Strobe Pulse Width	LATCHED READ ONLY	30	20		40	20		ns
T_{SL}	Strobe Latch Time	R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF (Note 5)	60	35		90	35		ns
T_{DL}	Strobe Delatch Time				30			35	ns
T_{CDS}	Chip Enable Set-up Time		40			50			ns

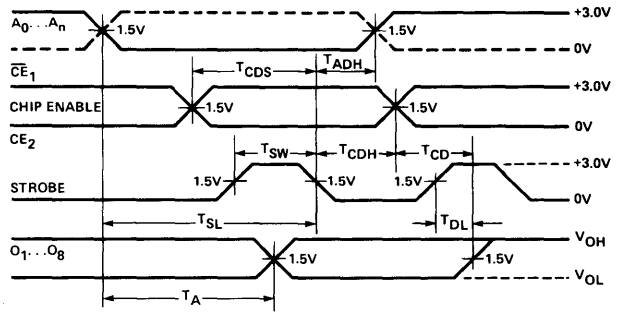
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner idential to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

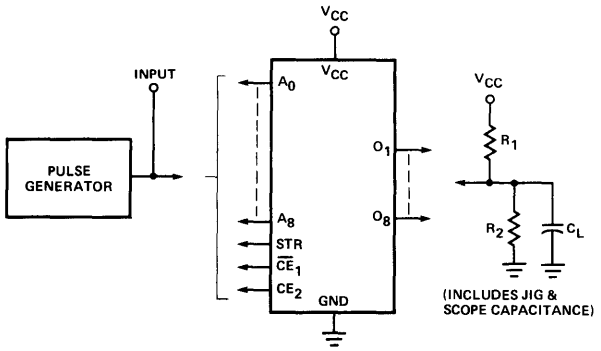
TRANSPARENT READ[5]
(Output Latches Not Used)



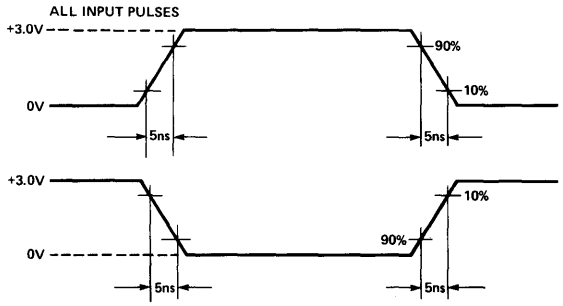
LATCHED READ[6]
(Output Latches Used)



AC TEST LOAD AND WAVEFORMS



INPUT PULSES



signetics

1024-BIT BIPOLAR READ ONLY MEMORY (256x4 ROM)

82S226
82S229

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S226 (Open Collector Outputs) and the 82S229 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both the 82S226 and 82S229 are also fully compatible with the 82S126/129, Signetics' 1024-Bit Programmable Read Only Memories.

Both 82S226 and 82S229 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S226/229, B or F. For the military temperature range (−55°C to +125°C) specify S82S226/229, F only.

FEATURES

- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME:
  - S82S226/229 – 70ns, MAXIMUM
  - N82S226/229 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT, TYPICAL
- INPUT LOADING:
  - S82S226/229 – (−150μA) MAXIMUM
  - N82S226/229 – (−100μA) MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  - 82S226 – OPEN COLLECTOR
  - 82S229 – TRI-STATE
- 16-PIN CERAMIC PACKAGE
- FULLY COMPATIBLE WITH 82S126/129, SIGNETICS' 256 X 4 PROM

APPLICATIONS

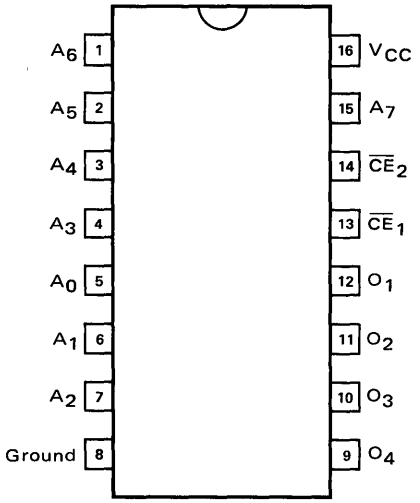
VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

ORDERING INFORMATION

Customer may specify patterns for the 1024-Bit Read Only Memory by completing the truth table/order blank in Signetics' Digital/Linear/MOS data book.

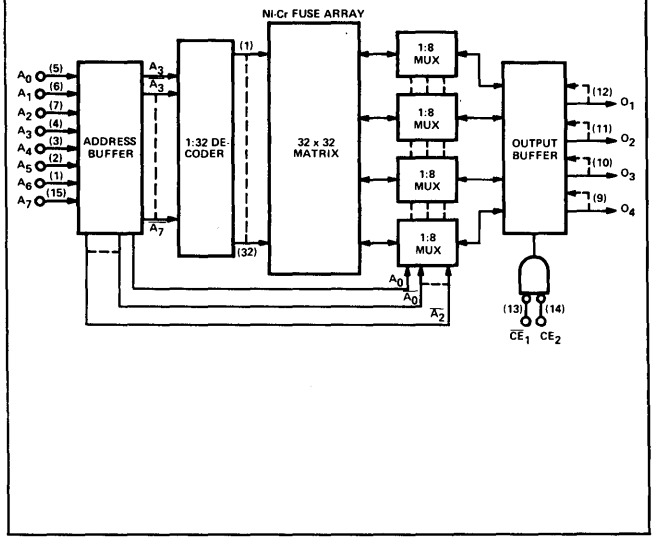
PIN CONFIGURATION

B, F PACKAGE*



*B – Plastic
F – Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S226)	+5.5	Vdc
V_O	Off-State Output Voltage (82S229)	+5.5	Vdc
T_A	Operating Temperature Range (N82S226/229) (S82S226/229)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S226/229 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S226/229 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS[1]	S82S226/229			N82S226/229			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage				.80			.85	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_{IC}	Input Clamp Voltage	$I_{IN} = -18mA$		−0.8	−1.2		−0.8	−1.2	V
V_{OL}	Low Level Output Voltage	$I_{OUT} = 16mA$			0.5			0.5	V
V_{OH}	High Level Output Voltage (82S229)	$\overline{CE}_1 = \overline{CE}_2 =$ "0", $I_{OUT} = -2mA$, "1" STORED	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S226)	$\overline{CE}_1$ or $\overline{CE}_2 =$ "1", $V_{OUT} = 5.5V$			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S229)	$\overline{CE}_1$ or $\overline{CE}_2 =$ "1", $V_{OUT} = 5.5V$			60			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2 =$ "1", $V_{OUT} = 0.5V$			−60			−40	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.45V$			−150			−100	μA
I_{IH}	High Level Input Current	$V_{IN} = 5.5V$			50			40	μA
I_{OS}	Output Short Circuit Current (82S229)	$V_{OUT} = 0V$	−15		−85	−20		−70	mA
I_{CC}	V_{CC} Supply Current			105	125		105	120	mA
C_{IN}	Input Capacitance	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5			5		pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$		8			8		pF

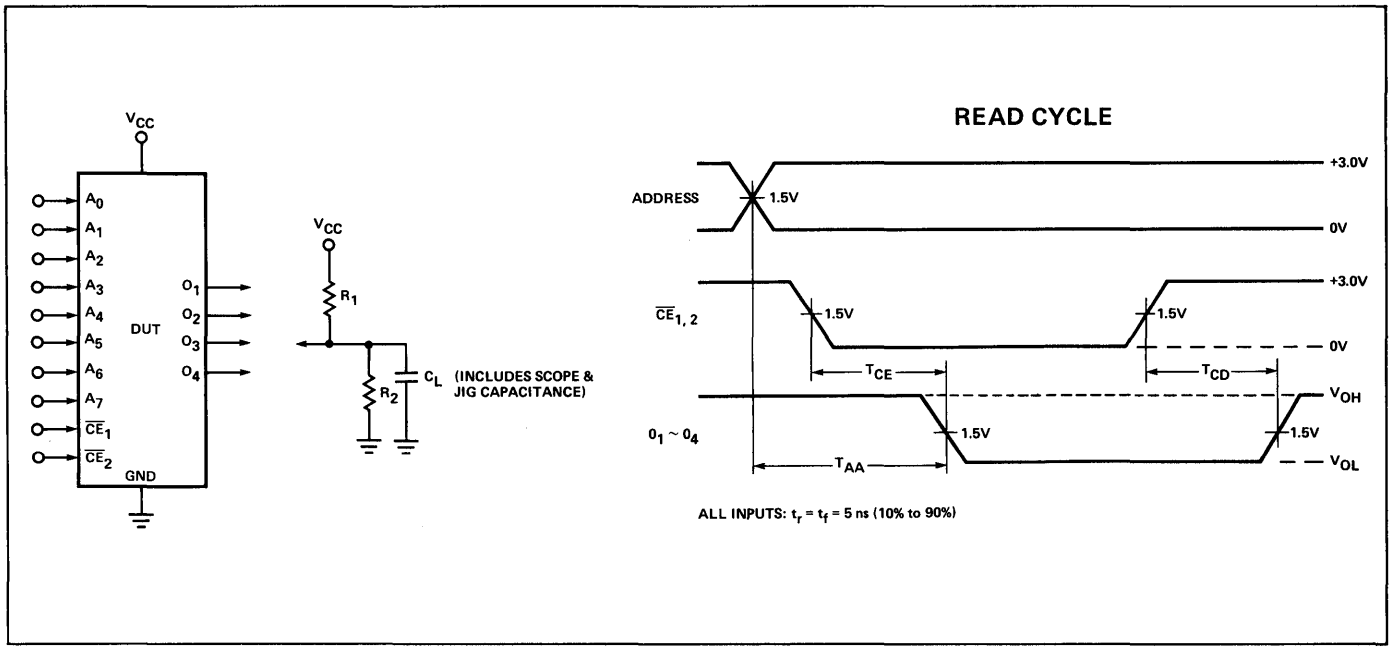
SWITCHING CHARACTERISTICS

S82S226/229 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S226/229 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S226/229			N82S226/229			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	$C_L = 30pF$, $R_1 = 270\Omega$, $R_2 = 600\Omega$		35	70		35	50	ns
T_{CD}	Chip Disable to Output			15	35		15	20	ns
T_{CE}	Chip Enable to Output			15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

AC TEST FIGURE AND WAVEFORM



DESCRIPTION

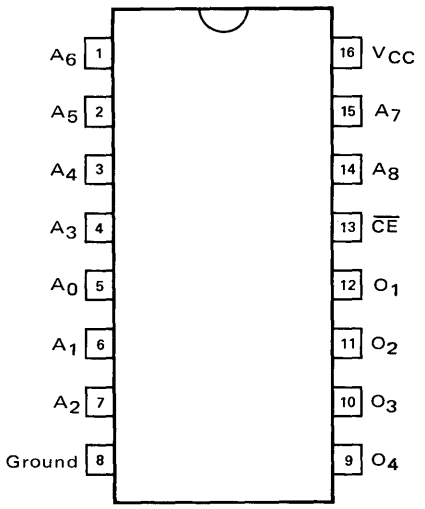
The 82S230 (Open Collector Outputs) and the 82S231 (Tri-State Outputs) are Bipolar 2048-Bit Read Only Memories, organized as 512 words by 4 bits per word.

The 82S230 and 82S231 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S230 and 82S231 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S230/231, F. For the military temperature range (−55°C to +125°C) specify S82S230/231, F.

PIN CONFIGURATION

F PACKAGE*

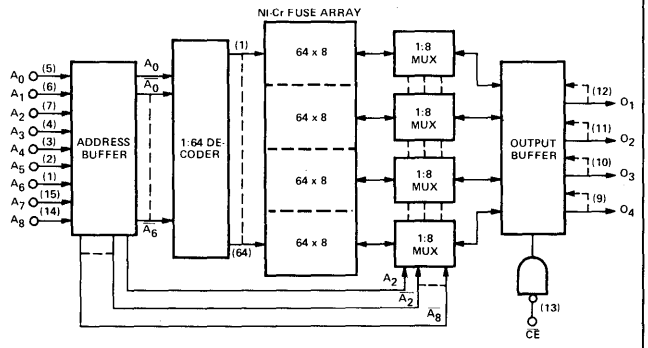


*F — Cerdip

FEATURES

- ORGANIZATION — 512 X 4
- ADDRESS ACCESS TIME:
  S82S230/231 — 70ns, MAXIMUM
  N82S230/231 — 50ns, MAXIMUM
- POWER DISSIPATION — 0.3mW/BIT TYPICAL
- INPUT LOADING:
  S82S230/231 — (−150μA) MAXIMUM
  N82S230/231 — (−100μA) MAXIMUM
- ONE CHIP ENABLE INPUT
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  82S230 — OPEN COLLECTOR
  82S231 — TRI-STATE
- FULLY COMPATIBLE WITH 82S130 AND 82S131 SIGNETICS PROMS
- 16-PIN CERAMIC DIP

BLOCK DIAGRAM



APPLICATIONS

SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S230)	+5.5	Vdc
V_O	Off-State Output Voltage (82S231)	+5.5	Vdc
T_A	Operating Temperature Range (N82S230/231) (S82S230/231)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S230/231 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S230/231 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S230/231			N82S230/231			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.45	V
I_{OLK}	Output Leakage Current (82S130)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S131)	$\overline{CE}$ = "1", V_{OUT} = 0.5V $\overline{CE}$ = "1", V_{OUT} = 5.5V			−60 60			−40 40	μA μA
V_{OH}	High Level Output Voltage (82S131)	$\overline{CE}$ = "0", I_{OUT} = −2.4mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			120	140		120	135	mA
V_{IC}	Input Clamp Voltage	I_N = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S231)	V_{OUT} = 0V	−15		−85	−20		−70	mA

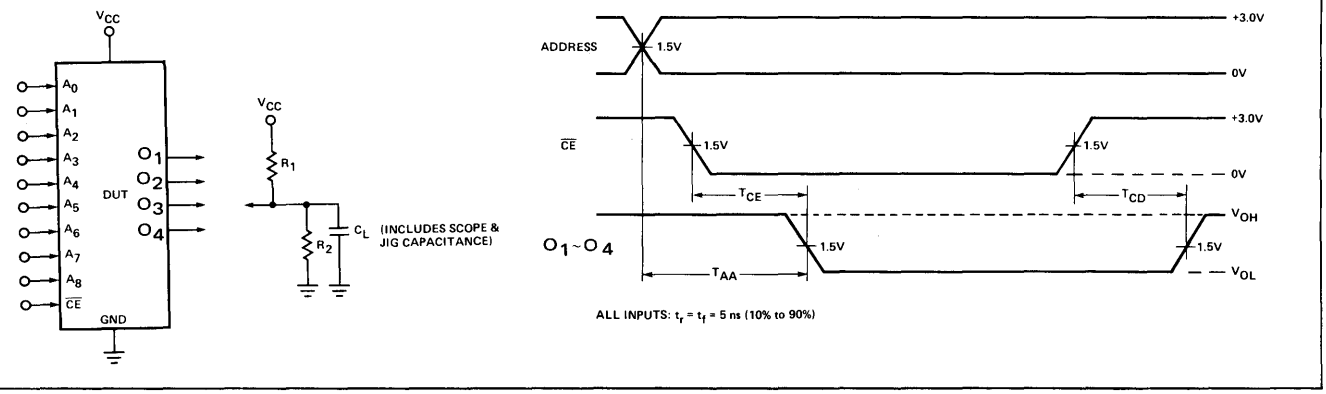
SWITCHING CHARACTERISTICS

S82S230/231 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S230/231 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S230/231			N82S230/231			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		40	70		40	50	ns
T_{CD}	Chip Disable to Output			20	30		20	30	ns
T_{CE}	Chip Enable to Output			20	30		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

AC TEST FIGURE AND WAVEFORM



DESCRIPTION

The 54/74S200/201 and 54/74S301 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state outputs options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, three chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level and −250μA (S54S200/201/301) or −100μA (N74S200/201/301) for a "0" level.

The additional feature of output blanking during write ($\overline{D_O}$ terminal "H" or "Hi-Z" state) permits $\overline{D_O}$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. Both devices have fast read access and write cycle times and thus are ideally suited in high speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S200/201/301, B or F. For the military temperature range (−55°C to +125°C) specify S54S200/201/301, F only.

FEATURES

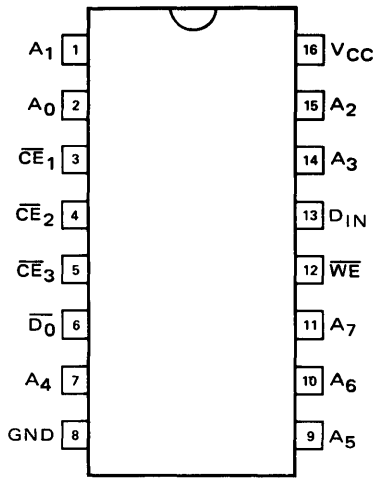
- **ORGANIZATION – 256 X 1**
- **ADDRESS ACCESS TIME:**
  - **S54S200/201/301 – 70ns MAXIMUM**
  - **N74S200/201/301 – 50 ns MAXIMUM**
- **WRITE CYCLE TIME:**
  - **S54S200/201/301 – 60ns MAXIMUM**
  - **N74S200/201/301 – 50ns MAXIMUM**
- **POWER DISSIPATION – 1.5mW/BIT TYPICAL**
- **INPUT LOADING:**
  - **S54S200/201/301 – (−250μA) MAXIMUM**
  - **N74S200/201/301 – (−100μA) MAXIMUM**
- **OUTPUT BLANKING DURING WRITE**
- **ON-CHIP ADDRESS DECODING**
- **OUTPUT OPTION:**
  - **TRI-STATE – 54/74S200/201**
  - **OPEN COLLECTOR – 54/74S301**
- **16 PIN CERAMIC DIP**

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



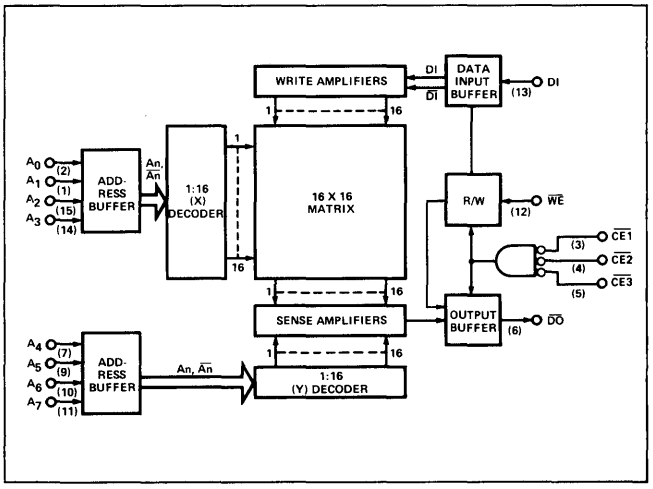
*B – Plastic
F – Cerdip

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				54/74S301	54/74S200/201
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (54/74S301)	+5.5	Vdc
V_O	Off-State Output Voltage (54/74S200/201)	+5.5	Vdc
T_A	Operating Temperature Range S54S200/201/301 N74S200/201/301)	 -55° to $+125^\circ$ 0° to $+70^\circ$	 °C °C
T_{stg}	Storage Temperature Range	-65° to $+150^\circ$	°C

ELECTRICAL CHARACTERISTICS

S54S200/201/301 $-55^\circ C \leq T_A \leq +125^\circ C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S200/201/301 $0^\circ C \leq T_A \leq +70^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S54S200/201/301			N74S200/201/301			UNIT	NOTES
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX		
V_{IH}	High Level Input Voltage	V_{CC} = MAX	2.0			2.0			V	1
V_{IL}	Low Level Input Voltage	V_{CC} = MIN			0.8			0.85	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V	1, 8
V_{OH}	High Level Output Voltage (N74S200/201)	V_{CC} = MIN I_{OH} = −10.3mA				2.4			V	1, 6
V_{OH}	High Level Output Voltage (S54S200/201)	V_{CC} = MIN I_{OH} = −5.2mA	2.4						V	1, 6
V_{OL}	Low Level Output Voltage	V_{CC} = MIN I_{OL} = 16mA		0.35	0.50		0.35	0.45	V	1, 7
I_{OLK}	Output Leakage Current (54/74S301)	V_{CC} = MIN V_O = 2.4V		1	50		1	40	μA	5
		V_{IH} = 2V V_O = 5.5V		1	50		1	40	μA	5
$I_{O(OFF)}$	Hi-Z State Output Current (54/74S200/201)	V_{CC} = MAX V_O = 5.5V		1	50		1	40	μA	5
		V_{IH} = 2V V_O = 0.4V		−1	−50		−1	−40	μA	5
I_I	Input Current at V_{IN} MAX	V_{CC} = MAX, V_{IN} = 5.5V			1			1	mA	8
I_{IH}	High Level Input Current	V_{CC} = MAX, V_{IH} = 2.7V		1	25		1	25	μA	8
I_{IL}	Low Level Input Current	V_{CC} = MAX, V_{IL} = 0.45V		−10	−250		−10	−100	μA	8
I_{OS}	Short Circuit Output Current (54/74S200/201)	V_{CC} = MAX V_O = 0V	−30		−100	−30		−100	mA	3
I_{CC}	V_{CC} Supply Current (54/74S200/201/301)	V_{CC} = MAX		80	130		80	130	mA	4
	V_{CC} Supply Current (54S200/201/301)	V_{CC} = MAX, T_A = +125°C			99				mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF	

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with logic "0" stored, and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS

S54S301 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S301 $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS		S54S301			N74S301			UNIT	NOTES[1]
		S54S301	N74S301	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX		
t_{PLH}	Access Time From Address				40	70		40	50	ns	B, D, E
t_{PHL}					40	70		40	50	ns	B, D, E
t_{PHL}	Enable Time From Chip Enable					45			35	ns	C, D, E
t_{PLH}	Disable Time From Chip Enable					30			20	ns	C, D, E
t_{PLH}	Disable Time From Write Enable					40			30	ns	C, D, E
t_{SR}	Sense-Recovery Time					50			40	ns	D
t_W	Width of Write Enable Pulse			50			40			ns	H
	Setup Time:										
	Address-to-Write Enable			0			0			ns	
t_{setup}	Data-to-Write Enable	$R_{L1} = 270\Omega$ $R_{L2} = 1K\Omega$ $C_L = 15pF$	$R_{L1} = 270\Omega$ $R_{L2} = 1K\Omega$ $C_L = 15pF$	50			40			ns	
	Chip Enable-to-Write Enable			0			0			ns	
	Hold Time:										D
	Address-From-Write Enable			10			10			ns	
t_{hold}	Data-From-Write Enable			10			10			ns	
	Chip Enable-From-Write Enable			0			0			ns	

SWITCHING CHARACTERISTICS

S54S200/201 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S200/201 $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

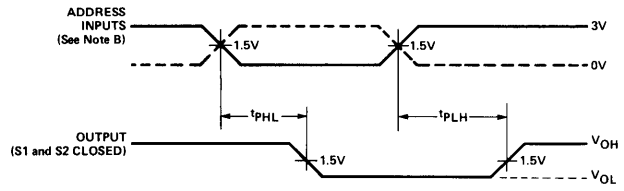
PARAMETER		TEST CONDITIONS		S54S200/201			N74S200/201			UNIT	NOTES[1]
		S54S200/201	N74S200/201	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX		
t_{PLH}	Access Time From Address	$R_L = 270\Omega$ $C_L = 15pF$	$R_L = 270\Omega$ $C_L = 15pF$		40	70		40	50	ns	B, D, E
t_{PHL}					40	70		40	50	ns	B, D, E
t_{ZH}	Enable Time From Chip Enable					45			35	ns	C, D, F, G
t_{ZL}						45			35	ns	C, D, F, G
t_{HZ}	Disable Time From Chip Enable	$R_L = 270\Omega$ $C_L = 5pF$	$R_L = 270\Omega$ $C_L = 5pF$			30			20	ns	C, D, F, G
t_{LZ}						30			20	ns	C, D, F, G
t_{HZ}	Disable Time From Write Enable					40			30	ns	D, G
t_{LZ}						40			30	ns	D, G
t_{ZH}	Sense-Recovery Time					50			40	ns	D, F
t_{ZL}						50			40	ns	D, F
t_W	Width of Write Enable Pulse			50			40			ns	H
	Setup Time:										
	Address-to-Write Enable			0			0			ns	
t_{setup}	Data-to-Write Enable	$R_L = 270\Omega$ $C_L = 15pF$	$R_L = 270\Omega$ $C_L = 15pF$	50			40			ns	
	Chip Enable-to-Write Enable			0			0			ns	
	Hold Time:										D
	Address-From-Write Enable			10			10			ns	
t_{hold}	Data-From-Write Enable			10			10			ns	
	Chip Enable-From-Write Enable			0			0			ns	

NOTES: 1. All typical values are $V_{CC} = 5V$, $T_A = 25°C$. 2. See Notes on Switching Parameter Measurement Information.

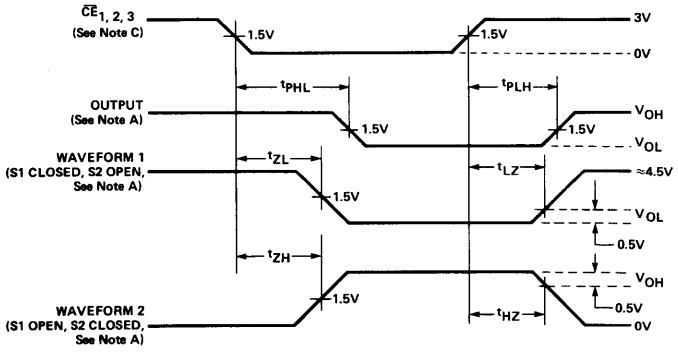
SWITCHING PARAMETER MEASUREMENT INFORMATION

READ CYCLE

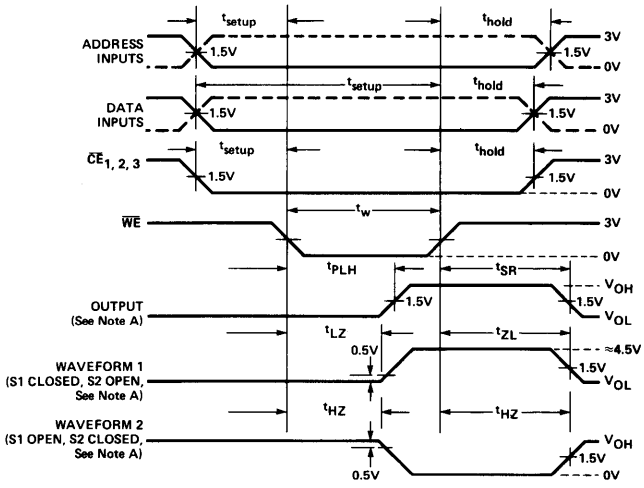
ACCESS TIME FROM ADDRESS



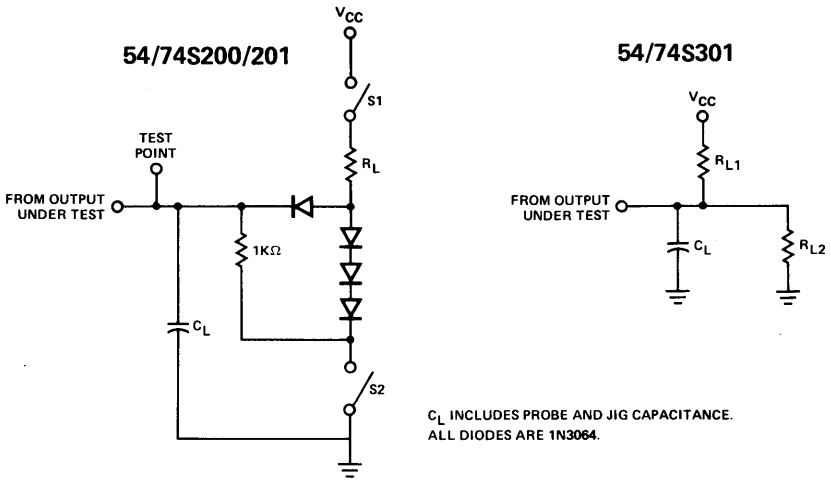
CHIP ENABLE AND DISABLE TIME



WRITE CYCLE



AC TEST LOAD



C_L INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.

NOTES:

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, PRR $\leq$ 1MHz, and $Z_{out} \approx 50\Omega$.
E. t_{PLH} propagation delay time, low-to-high-level output, t_{PHL} propagation delay time, high-to-low-level output.
F. t_{ZH} propagation delay time, hi-Z to high-level output, t_{ZL} propagation delay time, hi-Z to low-level output.
G. t_{HZ} propagation delay time, high-level to hi-Z output, t_{LZ} propagation delay time, low-level to hi-Z output.
H. Minimum required to guarantee a WRITE into the slowest bit.

DESCRIPTION

The 3101A is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

The 3101A is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 3101A assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 3101A is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N3101A, B or F. For the military temperature range (−55°C to +125°C) specify S3101A, F only.

FEATURES

- ORGANIZATION – 16 X 4
- ADDRESS ACCESS TIME:
  S3101A – 50ns, MAXIMUM
  N3101A – 35ns, MAXIMUM
- WRITE CYCLE TIME:
  S3101A – 25ns, MAXIMUM
  N3101A – 25ns, MAXIMUM
- POWER DISSIPATION – 6.25mW/BIT, TYPICAL
- INPUT LOADING:
  S3101A – (−150μA) MAXIMUM
  N3101A – (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

APPLICATIONS

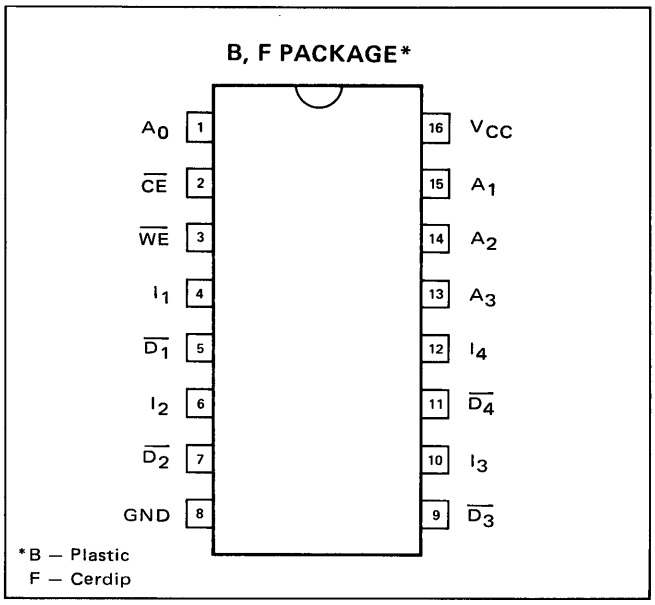
SCRATCH PAD MEMORY

BUFFER MEMORY

PUSH DOWN STACKS

CONTROL STORE

PIN CONFIGURATION

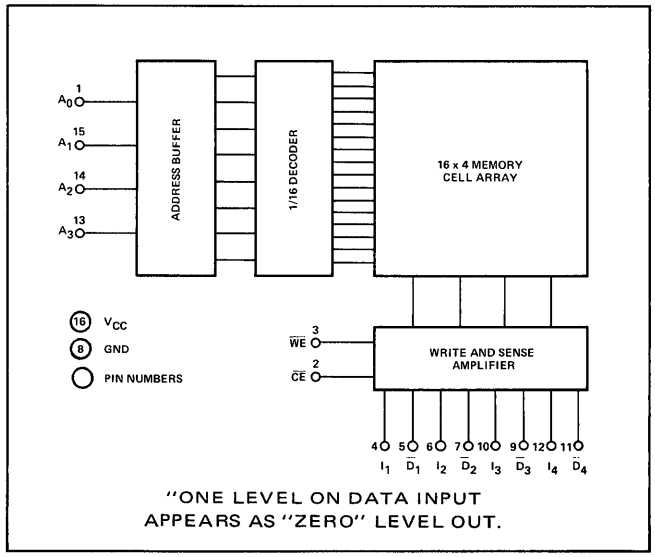


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{D}_N$
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	1
DISABLED	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N3101A)	0° to +75°	°C
	(S3101A)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S3101A $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N3101A $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S3101A[1,2,3]			N3101A[1,2,3]			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
I_{IL}	"0" Input Current	$V_{IN} = 0.45V$		−10	−150		−10	−100	μA
I_{IH}	"1" Input Current	$V_{IN} = 5.5V$			25			10	μA
V_{IL}	"0" Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	"1" Level Input Voltage	V_{CC} = MAX	2.0			2.0			V
V_{IC}	Input Clamp Voltage	$I_{IN} = -12mA$, V_{CC} = MIN (Note 6)					−1.0	−1.5	V
		$I_{IN} = -18mA$, V_{CC} = MIN (Note 6)		−0.8	−1.2				V
V_{OL}	"0" Output Voltage	$I_{OUT} = 16mA$, V_{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C_{IN}	Input Capacitance	$V_{IH} = 2.0V$, $V_{CC} = 5.0V$		5			5		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0V$, $V_{CC} = 5.0V$, $\overline{CE}$ = "1"		8			8		pF
I_{CC}	Power Supply Current	(Note 5)		80	105		80	105	mA
I_{OLK}	Output Leakage Current	$\overline{CE}$ = "1", $V_{OUT} = 5.5V$, V_{CC} = MIN		<1	100		<1.0	100	μA
		$\overline{CE}$ = "1", $V_{OUT} = 2.4V$, V_{CC} = MIN		<1	40				μA

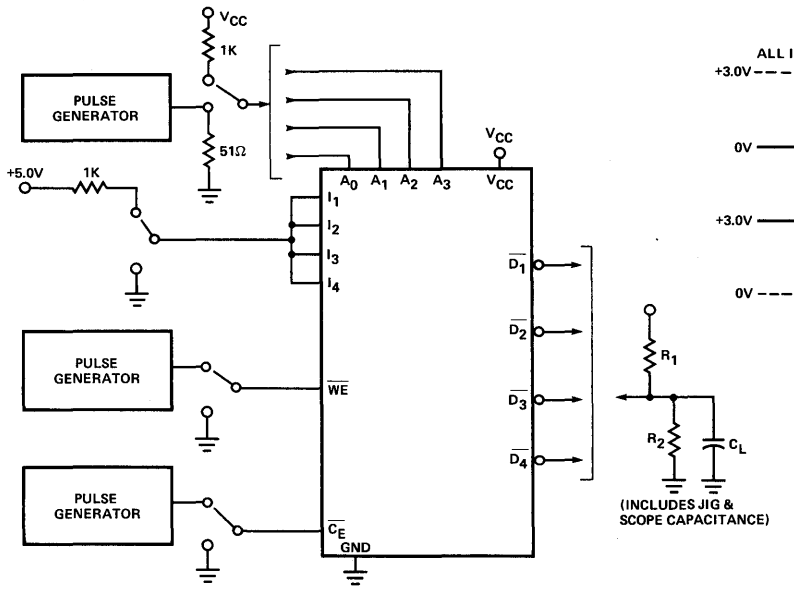
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V; "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.

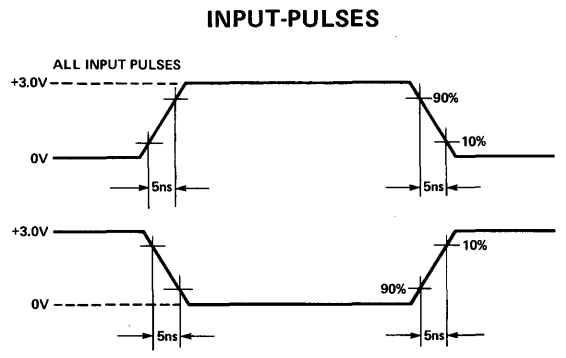
SWITCHING CHARACTERISTICS

S3101A $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N3101A $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S3101A			N3101A			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			25	50	10		35	ns
T_{CE}	Chip Enable Access Time			12	25	5		17	ns
T_{CD}	Chip Enable Output Disable Time			12	25	5		17	ns
T_{WD}	Write Enable to Output Disable Time			15	25			20	ns
T_{WR}	Write Recovery Time			22	40			35	ns
Write Set-up Times		$R_1 = 270\Omega$ $R_2 = 600\Omega$ $C_L = 30pF$							
T_{WSA}	Address to Write Enable		0			0	-8		ns
T_{WSD}	Data In to Write Enable		25			20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0			0	-5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		0			0			ns
T_{WHD}	Data In to Write Enable		0			0	-3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		0			0			ns
T_{WP}	Write Enable Pulse Width (Note 7)		25	18		25	18		ns

AC TEST LOAD AND WAVEFORMS



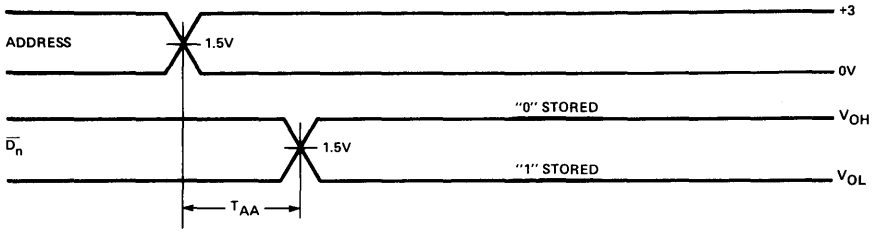


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

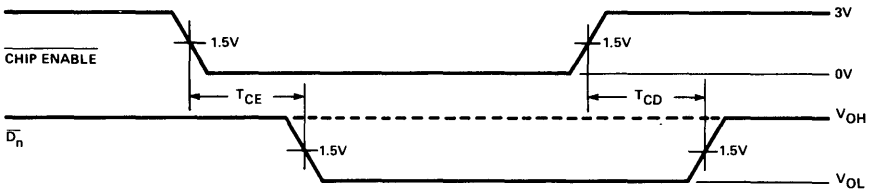
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

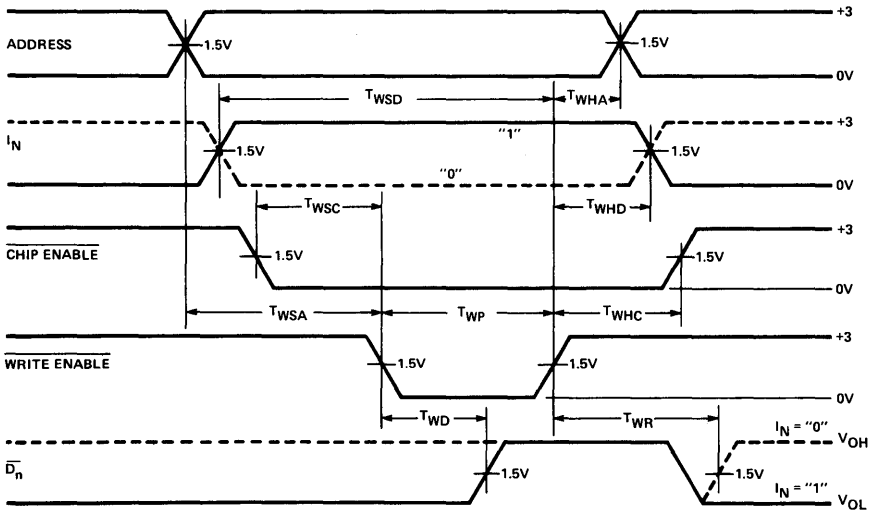
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

PRELIMINARY INFORMATION

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 10139 is an ECL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to low state when the chip enable input is high. This device is fully compatible with all of Signetics series 10,000 products. Address to output access time is 15 ns typical. Power dissipation is 580 milliwatts typical with separate internal bond wires and metal systems for V_{CC1} and V_{CC2}. The 10139 may be programmed to any desired pattern by the user. The 10139 is suitable for use in high performance ECL systems. A Truth Table/Order Blank is attached.

TEMPERATURE RANGE

–30 to +85°C Operating Ambient

RECOMMENDED OPERATING VOLTAGE

V_{CC} = GND, V_{EE} = –5.2V ±5%

FEATURES

- 15 ns TYPICAL ACCESS TIME
- 16 PIN PACKAGE
- EASY PROGRAMMING
- FULLY DECODED
- FULLY COMPATIBLE WITH ECL 10,000 SERIES
- HIGH IMPEDANCE INPUTS 50K OHM PULLDOWN
- OPEN EMITTER OUTPUTS

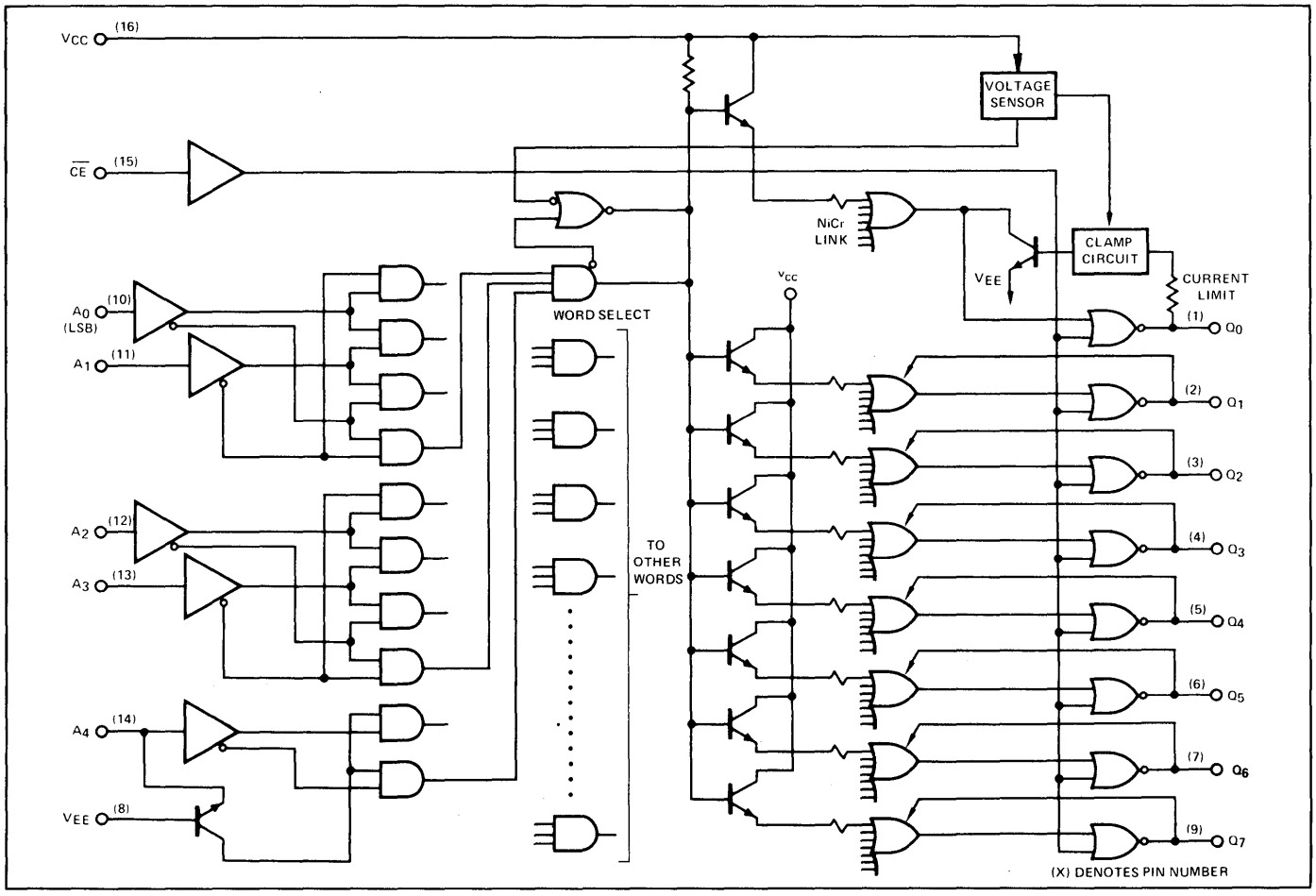
APPLICATIONS

PROGRAMMABLE LOGIC
CONTROL STORES
MICROPROGRAMMING
VOLUME PRODUCTION
HARDWIRED ALGORITHMS

PACKAGE TYPE

F: 16 Pin CERDIP

BLOCK DIAGRAM



PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = OV, R_L = 50Ω, V_{EE} = −5.2V)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Drain Current	I_{EO}		110	145	mAdc
Input Current V_{IH} = −0.810V, V_{IL} = −1.850V	 I_{inH} I_{inL}	 30		265	 μAdc μAdc
Output Voltage Logic "1" (V_{IH} = −0.810V, V_{IL} = −1.850V)	V_{OH}	−0.960		−0.810	Vdc
Logic "0" (V_{IH} = −0.810V, V_{ILA} = 1.850V)	V_{OL}	−1.990		−1.650	Vdc
Threshold Voltage Logic "1" (V_{IHA} = −1.105V, V_{ILA} = −1.475V)	V_{OHA}	−0.980			Vdc
Logic "0" (V_{IHA} = −1.105V, V_{ILA} = 1.475V)	V_{OLA}			−1.630	Vdc

PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = OV, V_{EE} = −5.2V, R_L = 50Ω)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Chip Enable Prop Delay			10	15	ns
Output Rise Time (20 to 80%) Output Fall Time (20 to 80%)			4.2 4.2		ns ns
Access Time Address to Output	T_{AD}		15	20	ns

RECOMMENDED PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write logical "1's", proceed as follows:

MANUAL (see Fig. 1)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Address the word to be programmed by applying 4.0 to 4.6 volts for a logic "1" and 0.0 to 1.0 volts for a logic "0" to the appropriate address inputs.

STEP 2

Raise V_{CC} (Pin 16) to 12 volts.

STEP 3

After V_{CC} has stabilized at 12 volts (including any ringing which may be present on the V_{CC} line) apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

STEP 4

Return V_{CC} to 5.2 volts.

CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 volts for more than 1 second.

STEP 5

Verify that the selected bit has programmed by connecting a 460Ω resistor to ground and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once.

STEP 6

If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (see Fig. 2)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Apply the proper address data and raise V_{CC} (Pin 16) to 12 volts.

STEP 2

After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.5 \leqslant PW \leqslant 1$ ms).

STEP 3

Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time; The delay between output programming pulses should be equal to or less than 1.0 ms.)

STEP 4

After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at 12 volts during the entire programming time.

STEP 5

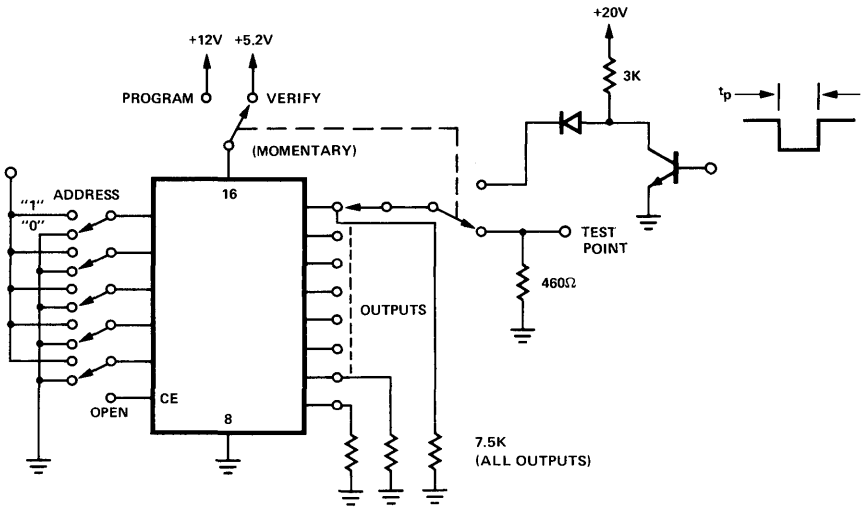
After stepping through all address words, return V_{CC} to +5.2 and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once.

PROGRAMMING SPECIFICATIONS

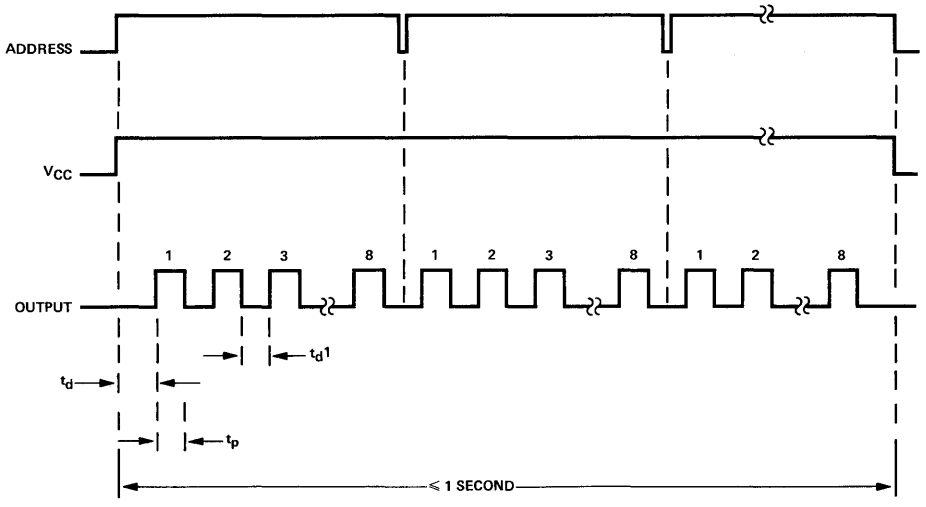
CHARACTERISTIC	SYMBOL	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
Power Supply Voltage						
To Program	V_{CCP}	11.5	12.0	12.5	Volts	
To Verify	V_{CCV}	5.0	5.2	5.4	Volts	
Programming Supply Current	I_{CCP}			250	mA	V_{CC} = 12.0 Volts
Address Voltage						
logical "1"	V_{IH}	4.0		4.6	Volts	
logical "0"	V_{IL}	0.0		1.0	Volts	
Max. Time at $V_{CC} = V_{CCP}$				1.0	Sec.	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mA	
Output Program Pulse Width	t_p	0.5		1.0	ms	
Output Pulse Rise Time				10	μs	
Programming Pulse Delay (1)						
following V_{CC} change	t_d	0.1		1.0	ms	
between output pulses	t_d1	0.01		1.0	ms	

NOTE:
(1) Maximum is specified to minimize the amount of time V_{CC} is at 12 volts.

MANUAL PROGRAMMING CIRCUIT



AUTOMATIC PROGRAMMING CIRCUIT



signetics

1024 x 1 BIT BIPOLAR RAM OPEN COLLECTOR (93415A) TRI-STATE (93425A)

93415A
93425A

MARCH 1975

DIGITAL 8000 SERIES TTL MEMORY

DESCRIPTION

The 93415A and 93425A are high speed 1024-bit random access memories organized as 1024 words X 1 bit. With a typical access time of 30ns, they are ideal for cache buffer applications and for systems requiring very high speed main memory.

Both the 93415A and 93425A require a single +5 volts power supply and feature very low current PNP input structures. They are fully TTL compatible, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 93415A and 93425A devices are available in the commercial temperature range (0°C to +75°C).

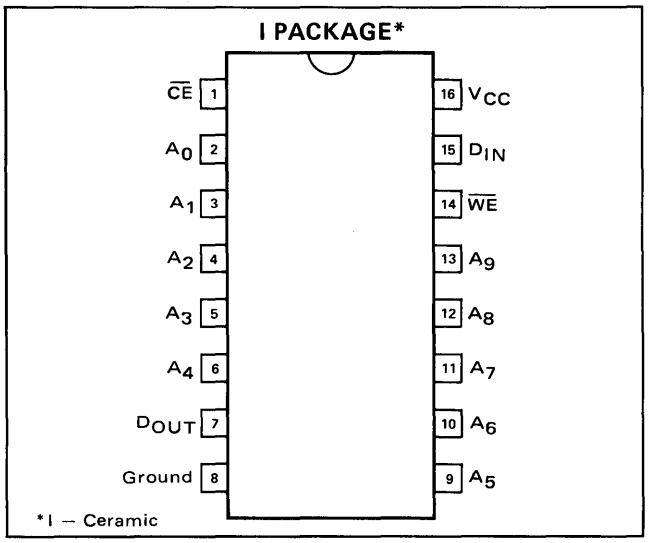
FEATURES

- ORGANIZATION – 1024 X 1
- ADDRESS ACCESS TIME – 45ns, MAXIMUM
- WRITE CYCLE TIME – 45ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT, TYPICAL
- INPUT LOADING – (–100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  - 93415A – OPEN COLLECTOR
  - 93425A – TRI-STATE
- NON-INVERTING OUTPUT
- BLANKED OUTPUT DURING WRITE
- 16 PIN CERAMIC PACKAGE

APPLICATIONS

HIGH SPEED MAIN FRAME
CACHE MEMORY
BUFFER STORAGE
WRITABLE CONTROL STORE

PIN CONFIGURATION



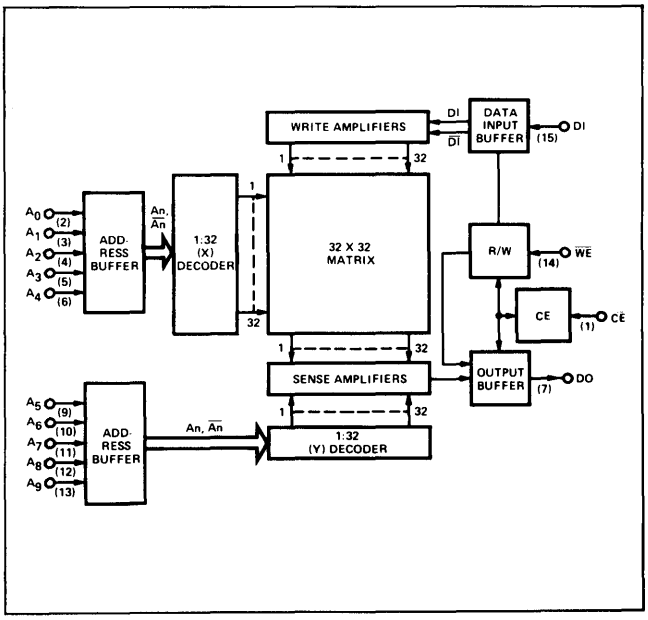
*I – Ceramic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				93415A	93425A
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (93415A)	+5.5	Vdc
V_O	Off-State Output Voltage (93425A)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

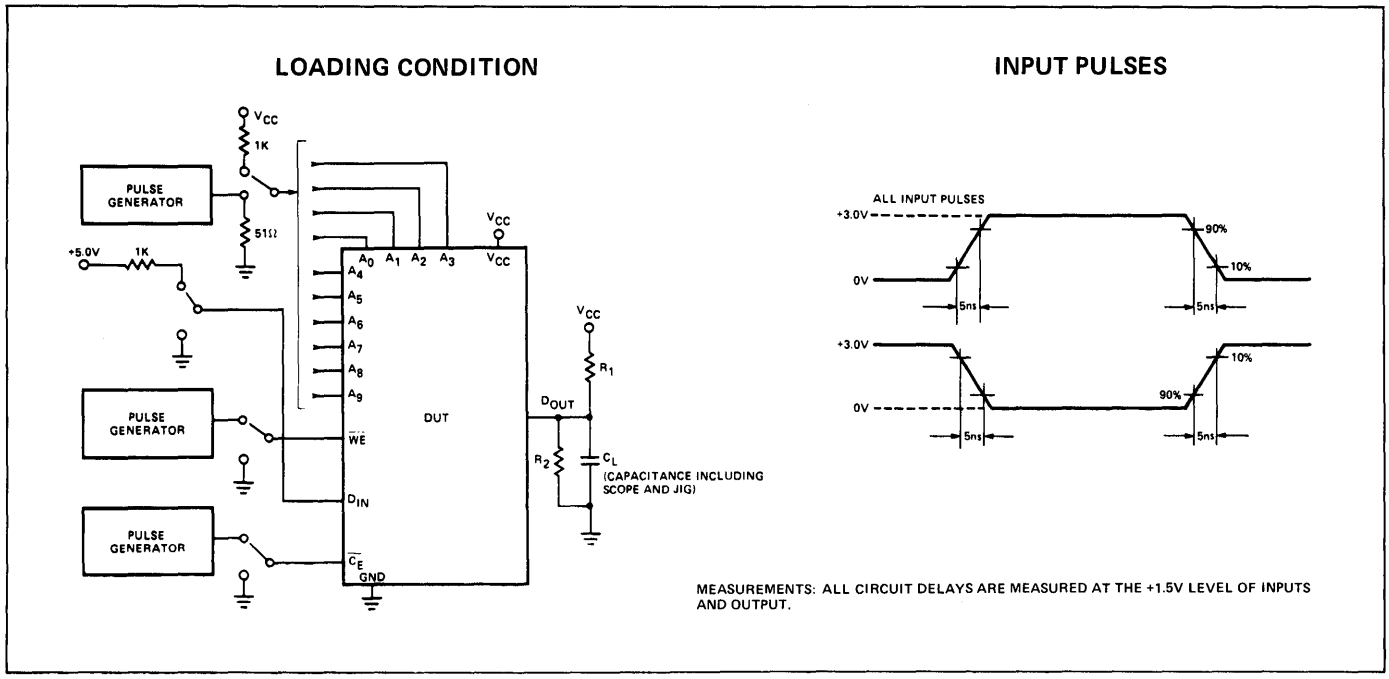
PARAMETER		TEST CONDITIONS	93415A/93425A			UNIT
			MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN (Note 1)			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX (Note 1)	2.1			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 1, 7)		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA (Note 1, 8)		0.35	0.45	V
V_{OH}	High Level Output Voltage (93425A)	V_{CC} = MIN, I_{OH} = −2mA (Note 1, 5)	2.4			V
I_{OLK}	Output Leakage Current (93415A)	V_{CC} = MAX, V_{OUT} = 5.5V (Note 6)		1	40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (93425A)	V_{CC} = MAX, V_{OUT} = 5.5V V_{CC} = MAX, V_{OUT} = 0.45V (Note 6)		1 −1	60 −60	μA μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	25	μA
I_{OS}	Short Circuit Output Current (93425A)	V_{CC} = MAX, V_{OUT} = 0V (Note 3)	−20		−100	mA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 4) $0 < T_A < 25°C$ $T_A \geq 25°C$ $T_A \leq 0°C$		 120 95	 155 130 170	 mA mA mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		4		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		7		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each input one at the time.
8. Measured with a logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
9. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   ϕ_{JA} Junction to Ambient at 400 fpm air flow — 50°C/Watt
   ϕ_{JA} Junction to Ambient — still air — 90°C/Watt
   ϕ_{JA} Junction to Case — 20°C/Watt

SWITCHING CHARACTERISTICS[3] $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER		TEST CONDITIONS	93415A/93425A			UNIT
			MIN	TYP[1]	MAX	
Propagation Delays						
T_{AA}	Address Access Time	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		30	45	ns
T_{CE}	Chip Enable Access Time			15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	30	ns
T_{WD}	Write Enable to Output Disable Time			20	30	ns
T_{WR}	Write Recovery Time			20	30	ns
Write Set-up Times						
T_{WSA}	Address to Write Enable		5	0		ns
T_{WSD}	Data In to Write Enable		40	35		ns
T_{WSC}	$\overline{CE}$ to Write Enable		5	0		ns
Write Hold Times						
T_{WHA}	Address to Write Enable		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		35	25		ns

AC TEST LOAD



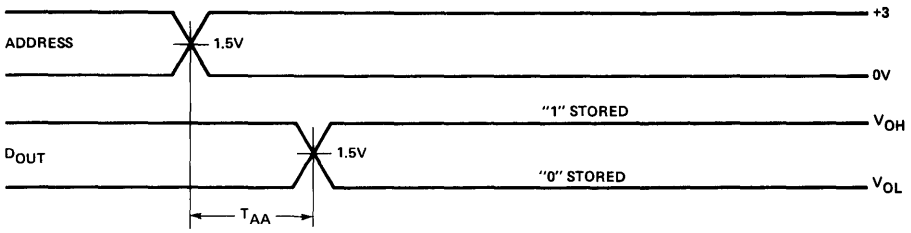
MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25° C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} Junction to Ambient at 400 fpm air flow — 50° C/Watt
   θ_{JA} Junction to Ambient — still air — 90° C/Watt
   θ_{JA} Junction to Case — 20° C/Watt

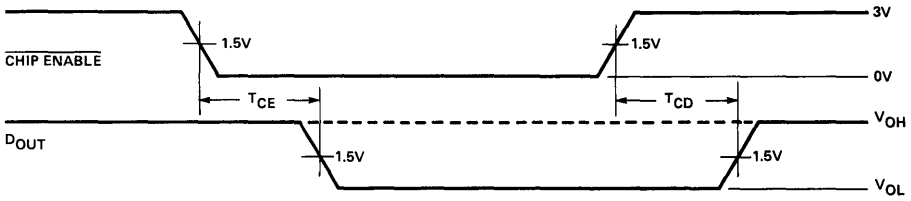
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

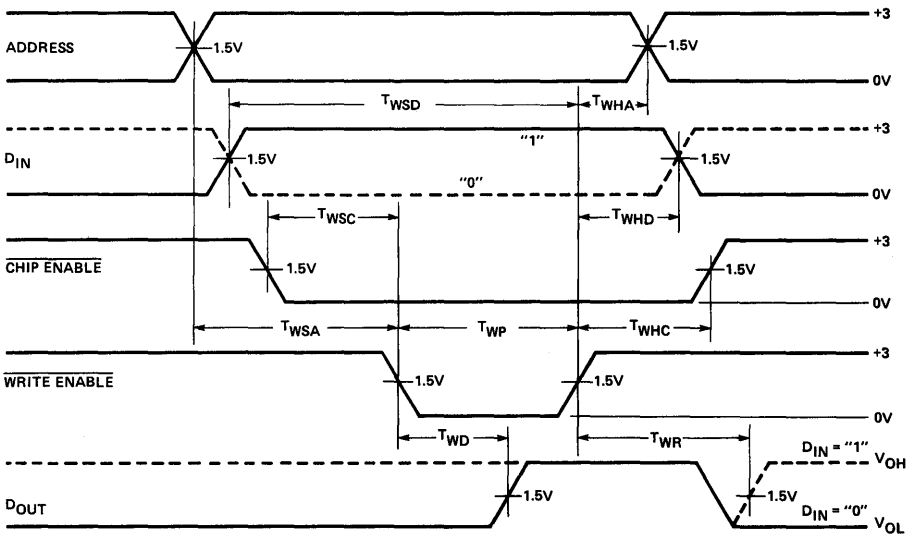
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

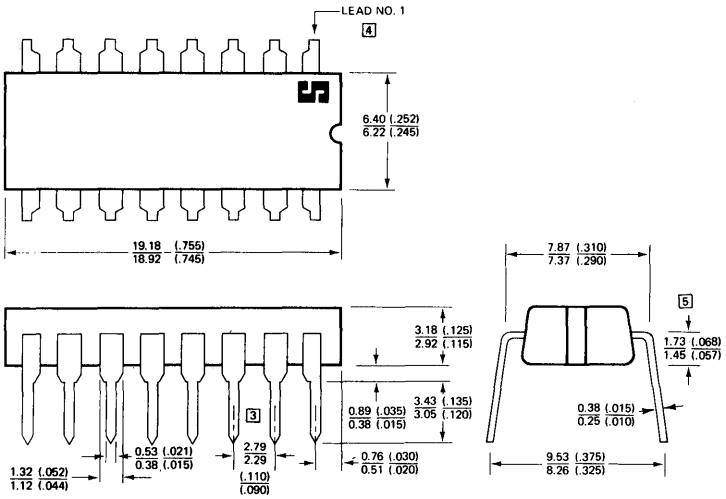
T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

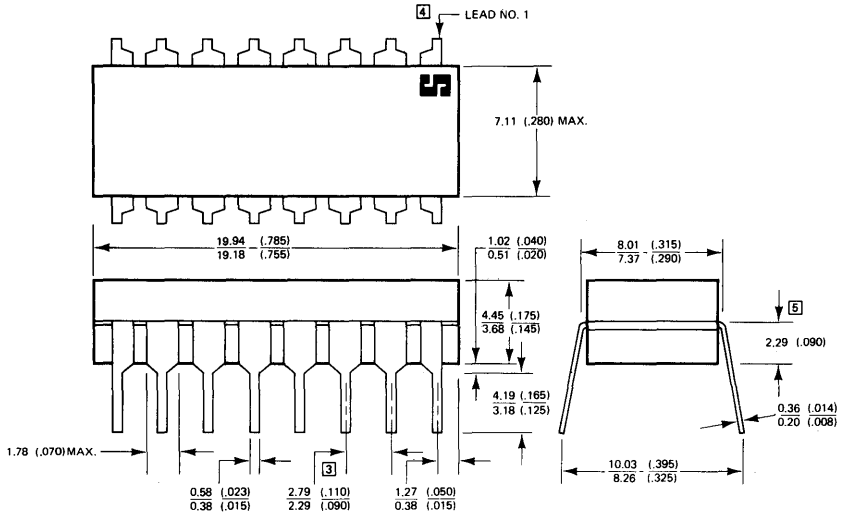
B PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

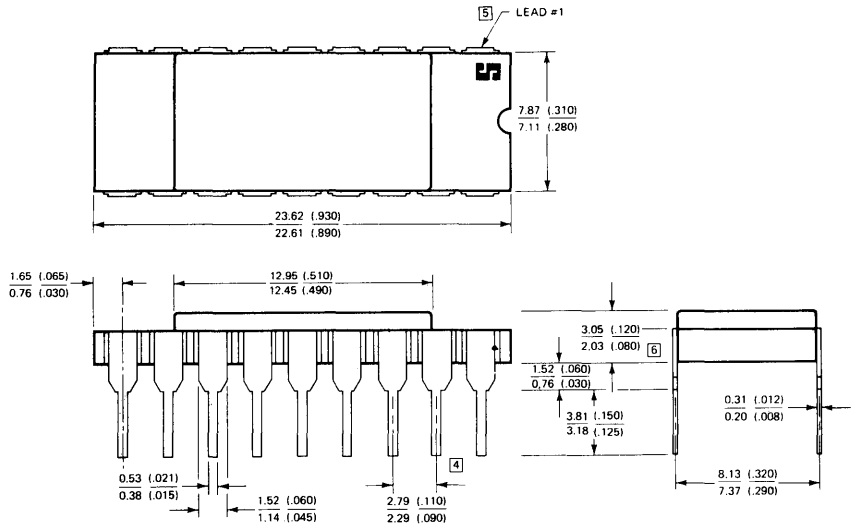
FJ PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Thermal resistance: Θ Ja = .090°C/mW, Θ Jc = .025°C/mW.
7. All dimensions shown in parentheses are English. (Inches)

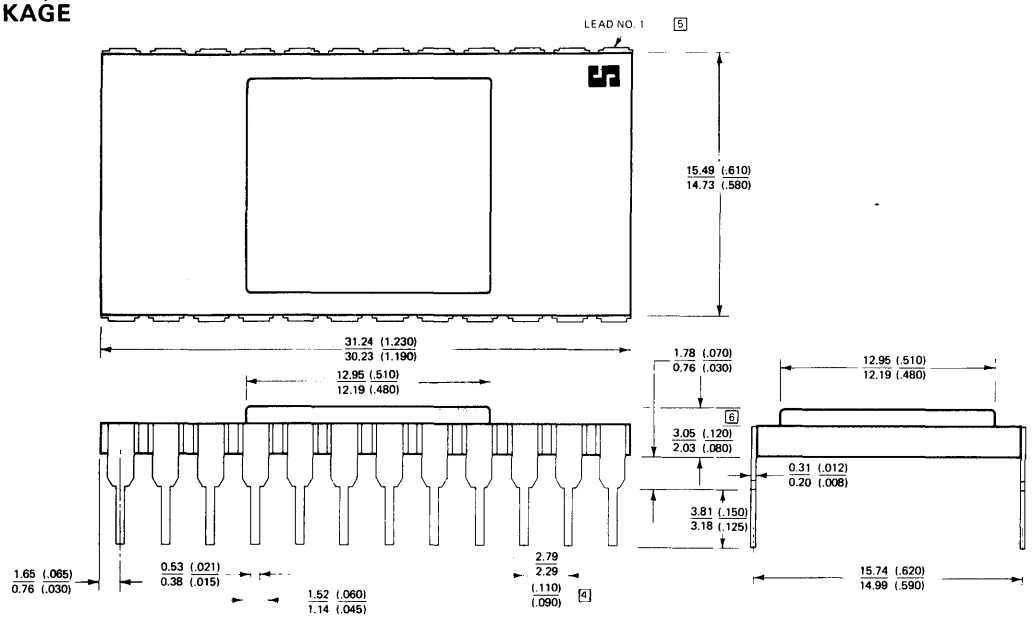
IJA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .080°C/mW, Θ Jc = .020°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

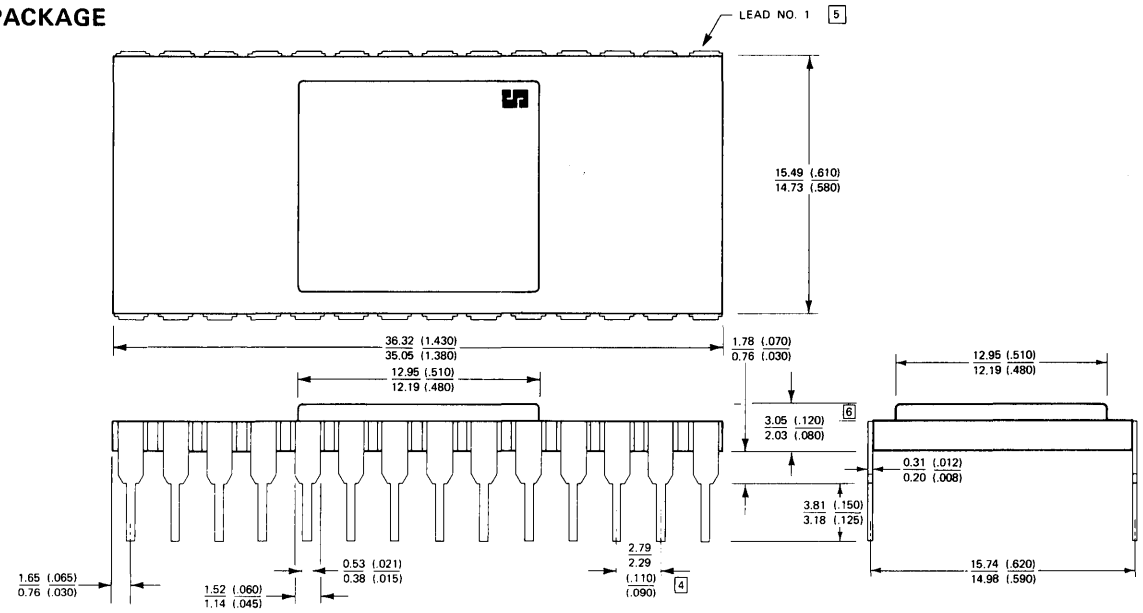
INB PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .015°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

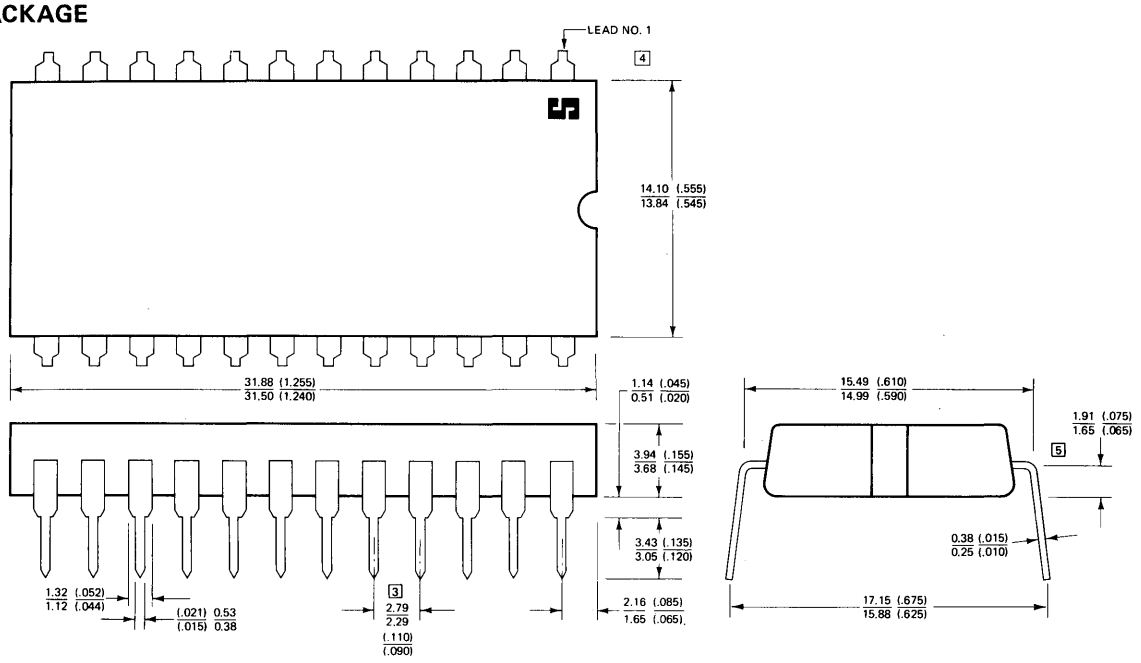
IQ PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

N PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .12°C/mW, Θ Jc = .05°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

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