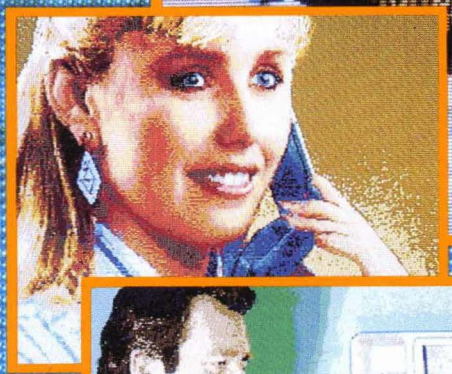
TELECOMS
IC Handbook



Plessey Semiconductors

TELECOMS IC HANDBOOK

PLESSEY

TELECOMS
IC Handbook

PLESSEY
Semiconductors

Foreword

Plessey Semiconductors is committed to the development of exciting and innovative products for telecommunications systems. Working in conjunction with major equipment manufacturers and PTTs has resulted in a wide range of IC products for all aspects of telecommunications equipment from central office to subscriber.

Two new devices typifying this philosophy are the **MV3000** and **SL376M**. Together these offer a highly integrated line card solution with great flexibility. The **MV3000** SLAC (Subscriber Line Audio Circuit) is DSP in action, a highly complex audio/digital processing circuit implemented in low power CMOS technology, whilst the **SL376M** SLIC (Subscriber Line Interface Circuit) is a Bipolar high voltage interface and control circuit. Both combine to offer the ultimate in performance and cost effectiveness.

In addition to innovative new products, Plessey offer a wide range of industry standard devices including DTMF circuits, LD dialers, Codecs and PCM building blocks.

This Handbook gives details of all current and soon-to-be-introduced products; Plessey are continually assessing the needs of equipment manufacturers and will be expanding the range in the future.

Contents

Product Index

Subscriber and line card circuits

Type	Function	Page
MV3000	Subscriber line audio circuit, automatic 2 to 4 wire balance; A to D; D to A; Time Slot Alignment; fully programmable	61
MV4320	Keypad pulse dialler with selectable pulse mark/space ratio 2:1 or 3:1; selectable outpulsing rate of 10,16, 20 or 932Hz; M1 masking output; +2.5V to +5.5V supply and low power: 375μW at +13V; last number redial	97
MV5087	DTMF generator for 2 of 8 (Form A) keypad, single contact	101
MV5089	DTMF generator for 2 of 8 active keypad, or electronic input	106
MV8804	8 x 4 analog switch array (32 crosspoint switch for PABX and key systems), 5V to 13V operation, bandwidth up to 40MHz	121
MV8870	Combined DTMF tone separation filter and decoder with 4-bit binary output code and low/high group outputs	127
MV8870-1	Combined DTMF tone separation filter and decoder with 4-bit binary output code	135
SL376M	Subscriber line interface circuit, line power feed; hybrid function; signalling; handles meter pulses	145
ZN470 series	Microphone amplifiers	198
ZN482/483	Buffer amplifiers for electret microphones	237
ZN480E	Ring detector, TTL logic output	224
ZN488E	Tone ringer, single ended or balanced output	231

PCM circuits

Type	Function	Page
MJ1410	8-bit format converter, 2MBit/s; 5V; 40mA	9
MJ1440	HDB3 coder/decoder, 2MBit/s; 5V; 20mA	14
MJ1444	Time slot zero transmitter, 2MBit/s; 5V; 20mA	19
MJ1445	Time slot zero receiver, 2MBit/s; 5V; 20mA	22
MJ1446	Time slot access, 2MBit/s; 5V; 20mA	25
MS2002	256 x 256 serial digital switch, 32-channel PCM, 2MBit/s, 5V, 40mA	37
MV1441	HDB3 with clock regeneration, 2MBit/s; 5V	49
MV1448	HDB3 coder/decoder, 8MBit/s; 5V	55
MV3506	Single channel PCM A-law codec with filter: featuring low power (60mW operating, 5mW standby), stable on-chip voltage reference and idle channel noise reduction circuit	86
MV3507	Single channel PCM μ-law codec with filter: other features as for **MV3506**	86
MV3507A	Single channel PCM μ-law codec with filter and A/B signalling capability: other features as for **MV3506**	86
MV3508	Single channel PCM A-law filter/codec with optional squelch	86
MV3508A	Single channel PCM μ-law filter/codec with optional squelch	86

PCM circuits (cont.)

Type	Function	Page
SP1450B(B)	34MBit/s PCM signal monitor 5V/2.5mA supply	159
SP1455B(B)	40MBit/s PCM signal monitor 5V/2.5mA supply	159
ZNPCM1	Single channel PCM A-law codec	177
ZNPCM2	Delta sigma modulator/demodulator	191
ZN1003	8 channel time slot assigner for use with codecs without on-chip timeslot assignment facilities	244
ZN5683E/J	PCM line interface, 8MBit/s; 5V	251

Other telecoms products

Type	Function	Page
D3702	5 relay drivers, -65V output, to BT approved spec.	158
MS2014	Digital 16-bit filter and detector - signalling tone detector	29
MV6001	Fast HDLC/DMA controller (e.g. for ISDN)	111
SL9009	Adaptive line equaliser	147
SP1404BW	5 relay drivers, -65V output	158

Fibre optic links/LANs

Type	Function	Page
SL9901	Trans-impedance amplifier	155
SP9921	Manchester decoder	163
SP9960	Encoder/LED driver	171

Product List - alpha numeric

Technical Data

PLESSEY
Semiconductors

MJ1410

8 BIT FORMAT CONVERTER

The MJ1410 is realised in N-channel MOS technology and operates from a single 5V supply. The circuit can be clocked from d.c. up to 2.5MHz and has 3-state output buffers capable of driving two LSTTL loads. All inputs are TTL compatible.

The MJ1410 performs the complementary functions of serial-to-parallel and parallel-to-serial data conversion on 8 bits of data. Both these conversions are achieved using the same time-position matrix, which has eight inputs and eight outputs.

An 8-bit parallel word clocked into the eight inputs appears as a serial 8-bit data stream on one of the eight outputs. Successive parallel words at the inputs appear as serial data streams on each of the eight outputs in turn.

Conversely, a serial 8-bit data stream on one of the eight inputs appears as an 8-bit parallel word on the eight outputs. Successive parallel words appearing at the eight outputs correspond to the serial data on each of the eight inputs in rotation.

The conversion can be 'programmed' to start in any register by setting the appropriate binary value on the counter pre-load inputs and applying a pulse to the Sync input. If the loading sequence produced by the counter is not required it can be disabled by connecting 'clock' to 'sync'. At each positive clock edge the register loaded will depend on the data on the counter inputs on the previous positive clock edge.

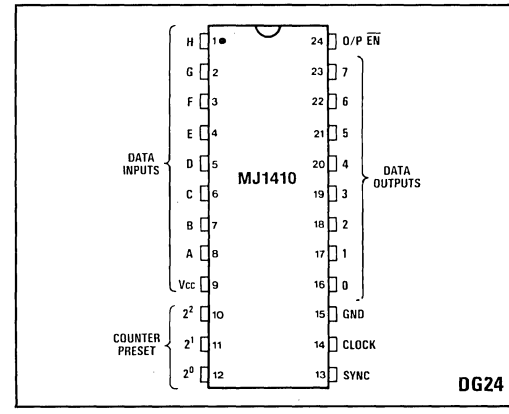


Fig.1 Pin connections

FEATURES

- Single 5V supply.
- Three-state outputs.
- All inputs TTL compatible.

FUNCTIONAL DESCRIPTION

Pin No.	Title	Function
1	H	Data i/p H
2	G	Data i/p G
3	F	Data i/p F
4	E	Data i/p E
5	D	Data i/p D
6	C	Data i/p C
7	B	Data i/p B
8	A	Data i/p A
	Data inputs	See Figs. 3 and 4
9	V_{CC}	Positive supply, 5V ± 5%
10	2^2	Counter preset i/p bit 2
11	2^1	Counter preset i/p bit 1
12	2^0	Counter preset i/p bit 0
		The counter is preset to the data on these i/ps on the 3rd positive clock edge following a negative edge on the 'sync' input.
13	SYNC	A negative edge on this i/p initiates the counter preset sequence which causes the conversion cycle to start in the register which corresponds to the binary value of the counter preset i/ps.
14	CLOCK	System clock
15	GND	Zero volts
16	0	Three state data o/p '0'
17	1	Three state data o/p '1'
18	2	Three state data o/p '2'
19	3	Three state data o/p '3'
20	4	Three state data o/p '4'
21	5	Three state data o/p '5'
22	6	Three state data o/p '6'
23	7	Three state data o/p '7'
	Data outputs	See Figs. 3 and 4
24	O/P $\overline{EN}$	A logic '1' on this i/p forces all the data outputs to a high impedance state.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{CC} = 5V, T_{amb} = 22°C ± 2°C, Test circuit: Fig.6.
Supply voltage V_{CC} = 5V ± 10%, Ambient operating temperature T_{amb} = 10°C to +70°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level I/P voltage	V_{IL}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	-0.3		0.8	Volts	
High level I/P voltage	V_{IH}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	2.5		V_{CC}	Volts	
Low level I/P current/high level I/P current	I_{IN}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24		1	50	µA	
Low level O/P voltage	V_{OL}	16,17,18, 19,20,21, 22,23			0.5	Volts	I_{SYNC} = 1.6mA
High level O/P voltage	V_{OH}	16,17,18, 19,20,21, 22,23	2.5			Volts	I_{SOURCE} = 100uA
Low level O/P current sink capability	I_{OL}	16,17,18, 19,20,21, 22,23	-1.6			mA	
High level O/P current source capability	I_{OH}	16,17,18, 19,20,21, 22,23	100			µA	
OFF state O/P current	$I_{OFF\ L}$	16,17,18, 19,20,21, 22,23			40	µA	V_{OUT} = GND
	$I_{OFF\ H}$	16,17,18, 19,20,21, 22,23			-40	µA	V_{OUT} = V_{CC}
Power dissipation	P_{DISS}		90		500	mW	V_{CC} = 5.5V

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.clock frequency	$F_{max.}$	2.4		10	MHz	
Min. clock frequency	$F_{min.}$	0			MHz	
Sync. pulse width (positive)	t_{SPP}	60			ns	Fig. 6
Sync. pulse width (negative)	t_{SPN}	100			ns	Fig. 6
Lead of sync. clocking edge on positive clock edge	t_{SL}	130			ns	Fig. 6
Set up time of counter inputs (2^0,2^1,2^2)	t_{SC}	70			ns	Fig. 6
Hold time of counter inputs	t_{HC}	60			ns	Fig. 6
Set up time of data inputs (A-H)	t_{SD}	80			ns	Fig. 6

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Hold time of data inputs	t_{HD}	85			ns	Fig. 6
Propagation delay, data out valid from output ENABLE low	t_{PDE}			100	ns	Fig. 6
Propagation delay, data out disabled from output ENABLE high	t_{PDD}			100	ns	Fig. 6
Propagation delay, clock to data out valid	t_{PCD}			200	ns	Fig. 6

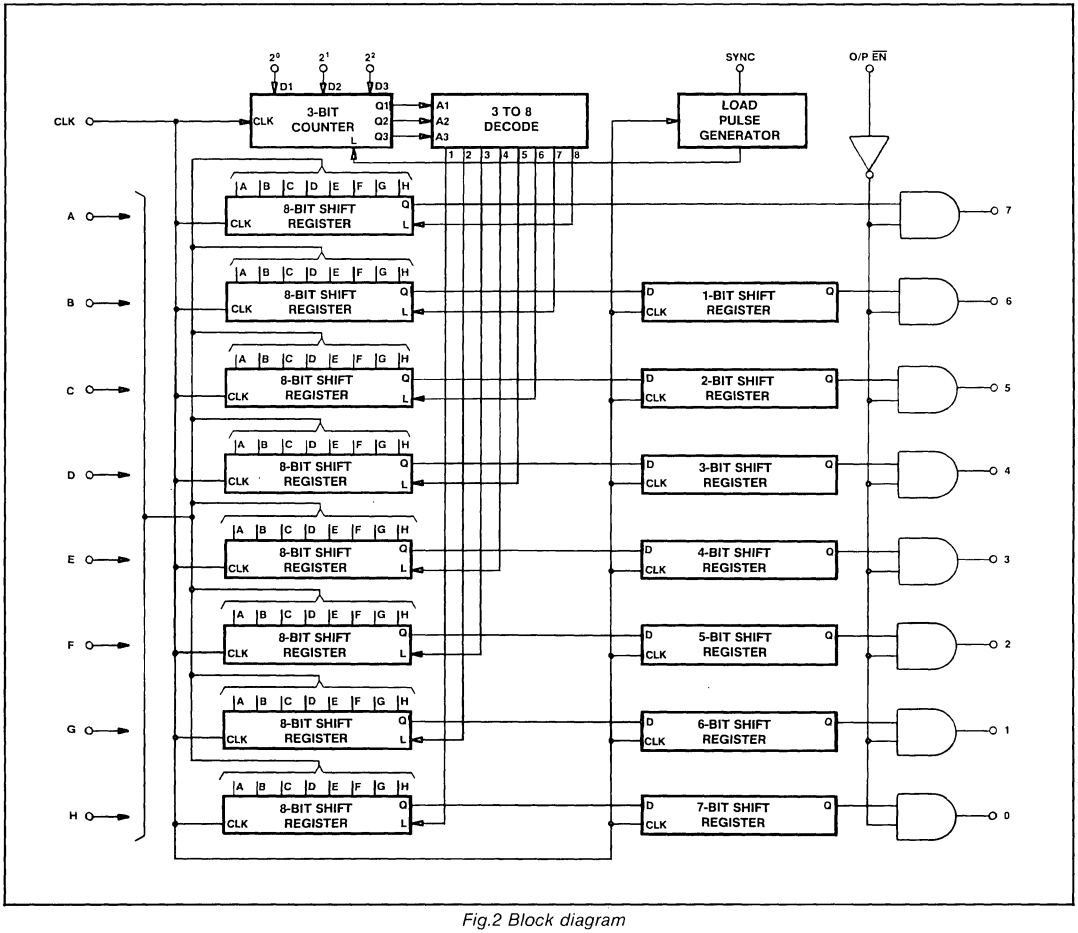


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. ground = 7V max.
Storage temperature = -55°C to +125°C

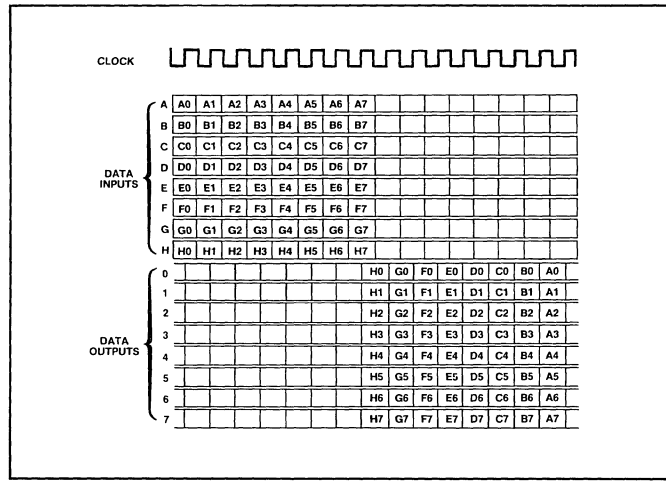


Fig.3 Data conversion

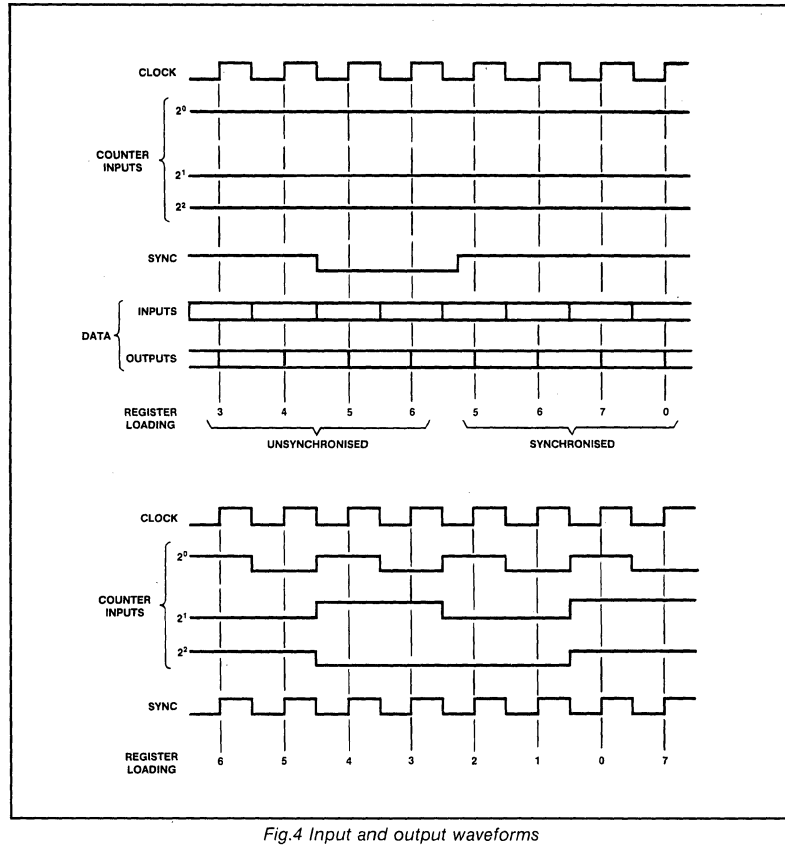


Fig.4 Input and output waveforms

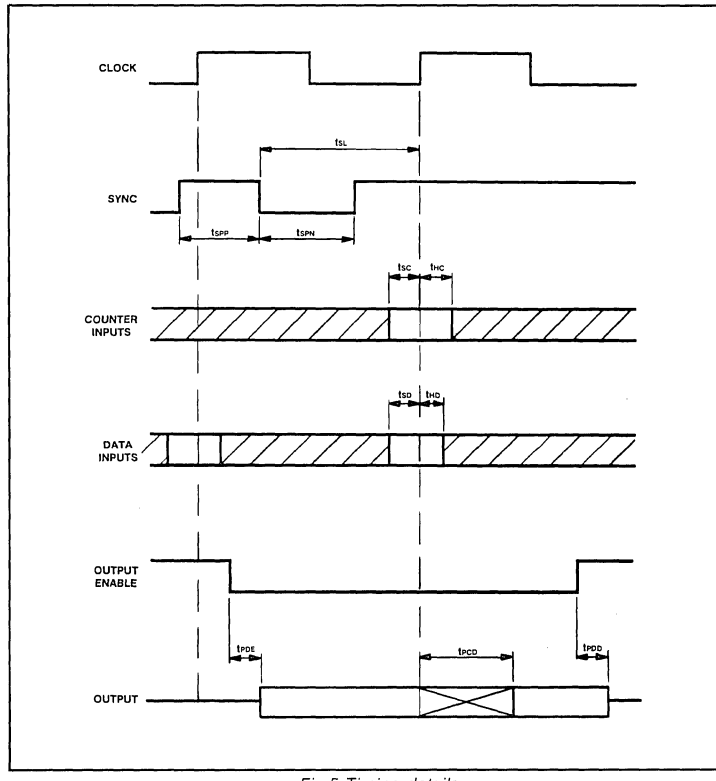


Fig.5 Timing details

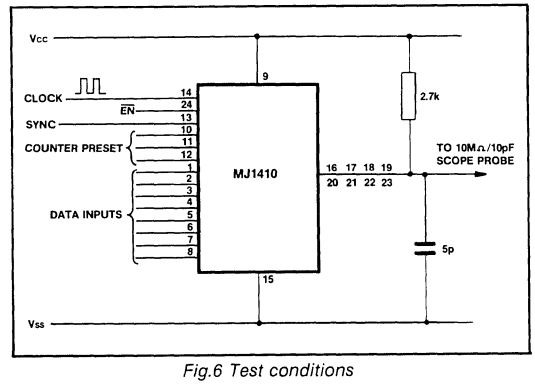


Fig.6 Test conditions

2 MBIT PCM SIGNALLING CIRCUIT

MJ1440

HDB3 ENCODER/DECODER

The 2.048 MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply, relevant inputs and outputs are TTL compatible.

The MJ1440 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeroes detection). In addition a loop back function is provided for terminal testing.

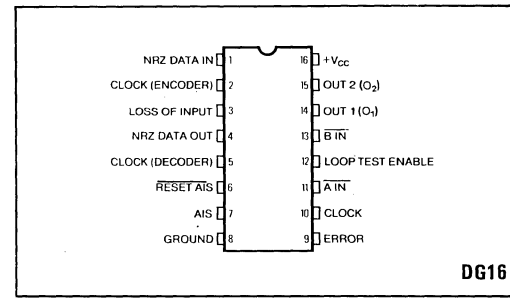


Fig. 1 Pin connections

FEATURES

- 5v ± 5% Supply −50mA Max
- HDB3 Encoding and Decoding to CCITT rec. G703.
- Asynchronous Operation.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal Generated from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector).
- Decode Data in NRZ Form.

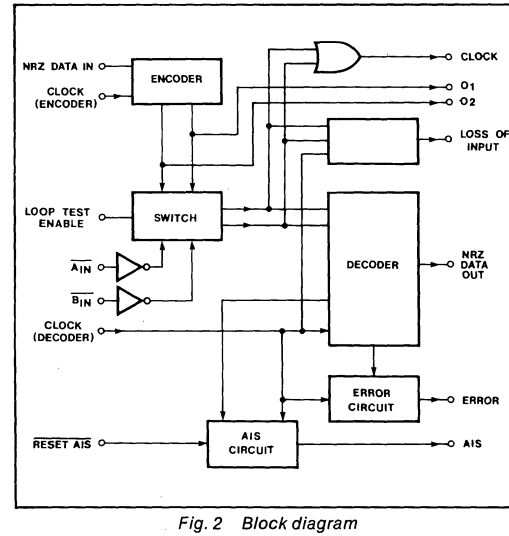


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
40°C/Watt	120°C/Watt

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = 0°C$ to $+70°C$

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,5,6 10,11,12,13	-0.3		0.8	V	
Low level input current	I_{IL}				50	µA	$V_{IL} = 0V$
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	µA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 80µA
		3,4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	3,4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	50	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0			MHz	Figs.10, 15
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2			MHz	Figs.11, 15
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.10, 15. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10, 15
tpd1A-tpd1B				20	ns	Figs.10, 15
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = Figs.13, 15
Setup time of NRZ data in to Clock (Encoder)	ts3	30			ns	Figs.8, 10, 15
Hold time of NRZ data in	th3	55			ns	Figs.10, 15
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.9, 13, 15
Propagation delay Clock (Decoder) to loss of input				150	ns	
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.12, 15
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.14, 15
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.9, 11, 15. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.9, 11, 15
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.9, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs.9, 14, 15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	200			ns	Figs.9, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.14, 15

NOTES
1. Encoded HDB3 outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4).

FUNCTIONAL DESCRIPTION

Functions Listed by Pin Number

1. NRZ data in
Input data for encoding into ternary HDB3 form. The NRZ data is clocked by the negative edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. Loss of input alarm
This output goes to logic '1' if eleven consecutive zeroes are detected in the incoming HDB3 data. The output is set to logic '0' on receipt of a '1'.

4. NRZ data out
Decoded data in NRZ form from ternary HDB3 input data (A_{in}, B_{in}), data is clocked out by positive going edge of clock (Decoder).

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on Reset AIS enables the internal decoded zero counter.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 coding has been received i.e. 3 '1's of the same polarity.

10. Clock
'OR' function of $\overline{A}_{in}$, $\overline{B}_{in}$ for clock regeneration when pin 12 = '0', 'OR' function of O_1, O_2 when pin 12 = '1'.

11,13. $\overline{A}_{in}$, $\overline{B}_{in}$
Inputs representing the received ternary HDB3 PCM signal. $\overline{A}_{in}$ = '0' represents a positive going '1', $\overline{B}_{in}$ = '0' represents a negative going '1'. $\overline{A}_{in}$ and $\overline{B}_{in}$ are sampled by the positive going edge of the Clock (Decoder). $\overline{A}_{in}$ and $\overline{B}_{in}$ may be interchanged.

12. Loop test enable
Input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 12 = '1' O_1 is connected internally to A_{in}. O_2 is connected to B_{in}. Clock becomes the OR function $O_1 + O_2$. The delay from NRZ in to NRZ out is 6½ clock periods in the loop back condition.

14,15. O_1, O_2
Outputs representing the ternary encoded data for line transmission O_1 = '1' representing a positive going '1', O_2 = '1' represents a negative going '1'. O_1 and O_2 may be interchanged.

16. V_{CC}
Positive supply, 5V ± 5%.

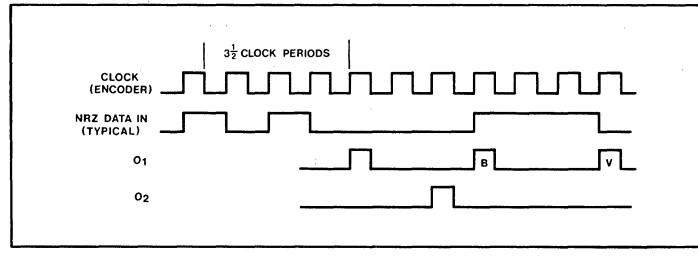


Fig. 3 Encode waveforms

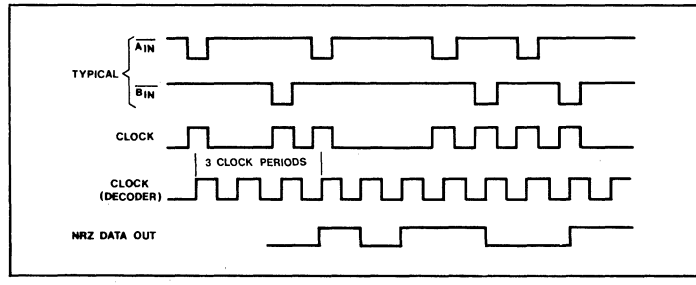


Fig. 4 Decode waveforms

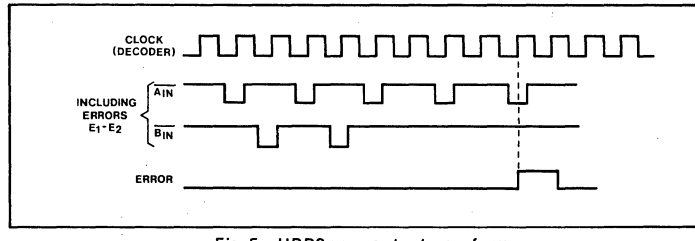


Fig. 5 HDB3 error output waveforms

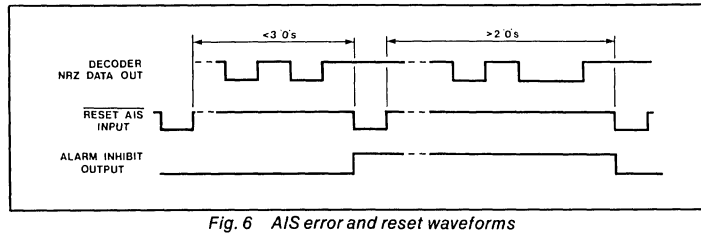


Fig. 6 AIS error and reset waveforms

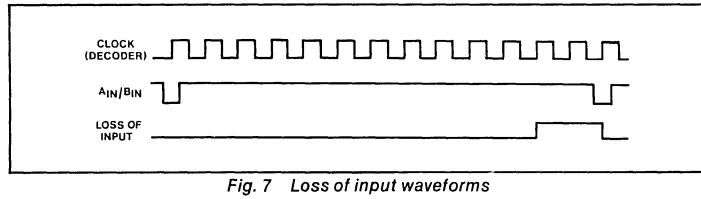


Fig. 7 Loss of input waveforms

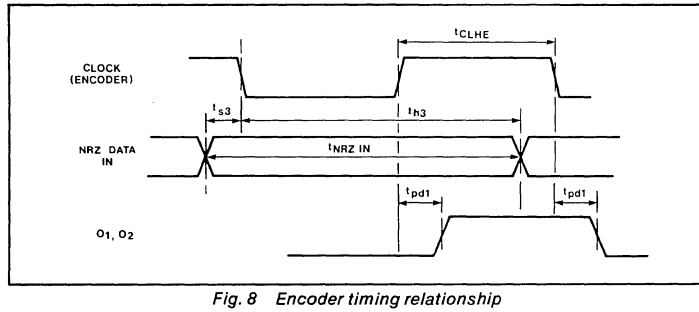


Fig. 8 Encoder timing relationship

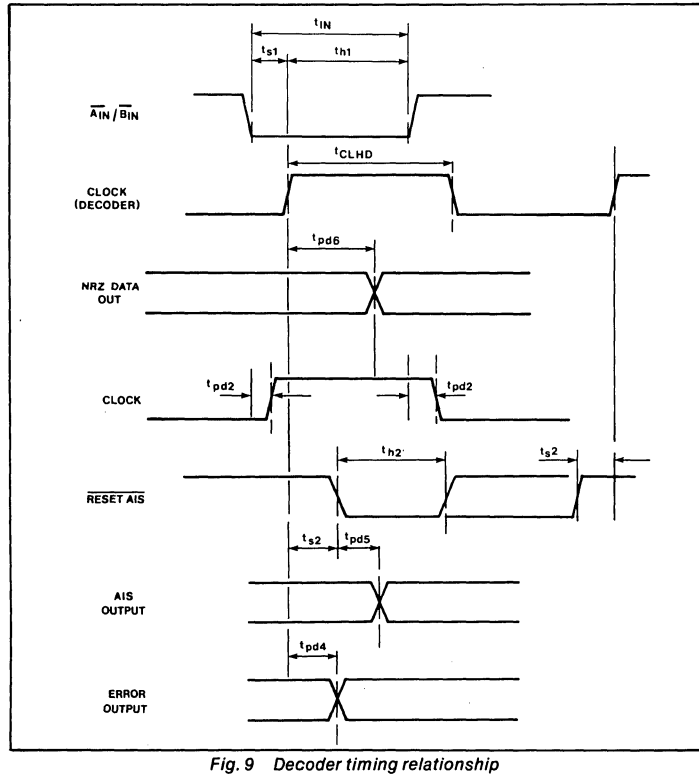


Fig. 9 Decoder timing relationship

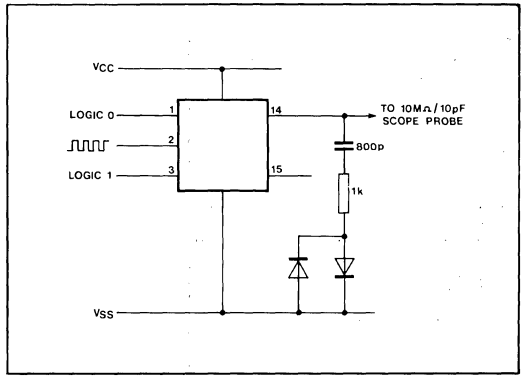


Fig. 10

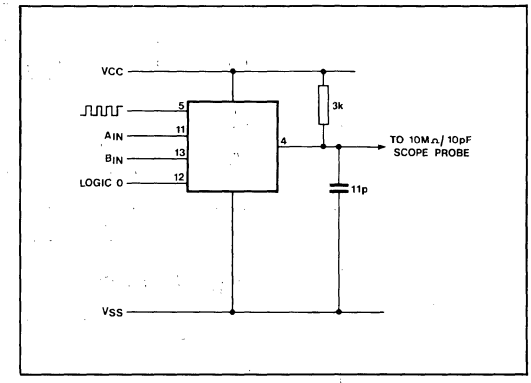


Fig. 11

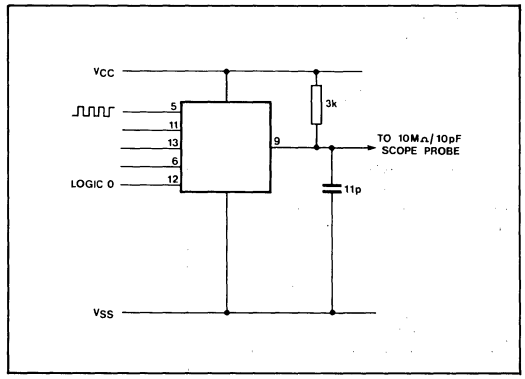


Fig. 12

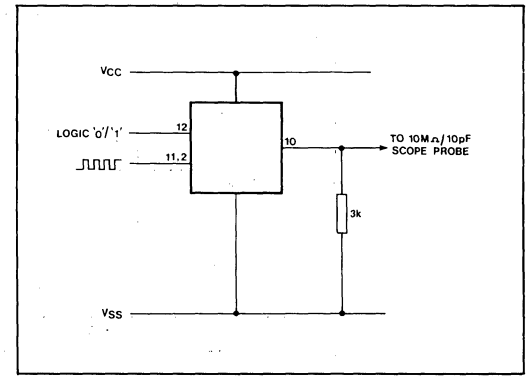


Fig. 13

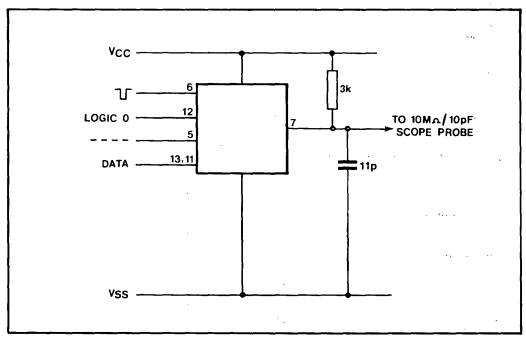


Fig. 14

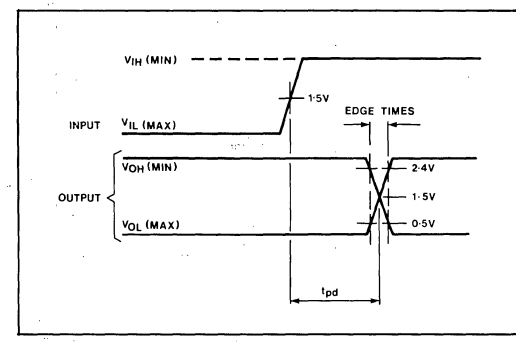


Fig. 15 *Test timing definitions*

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

PCM SYNCHRONISING WORD GENERATOR

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{SF}$', and time slot 16 'TS16' outputs.

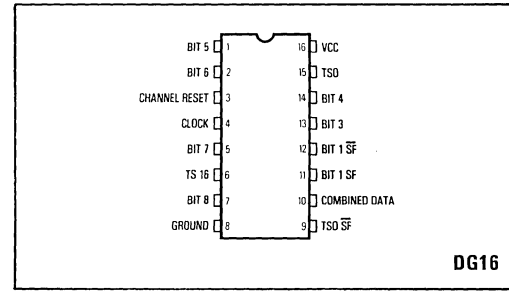


Fig.1 Pin connections

FEATURES

- 5V ± 5% Supply — 20 mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

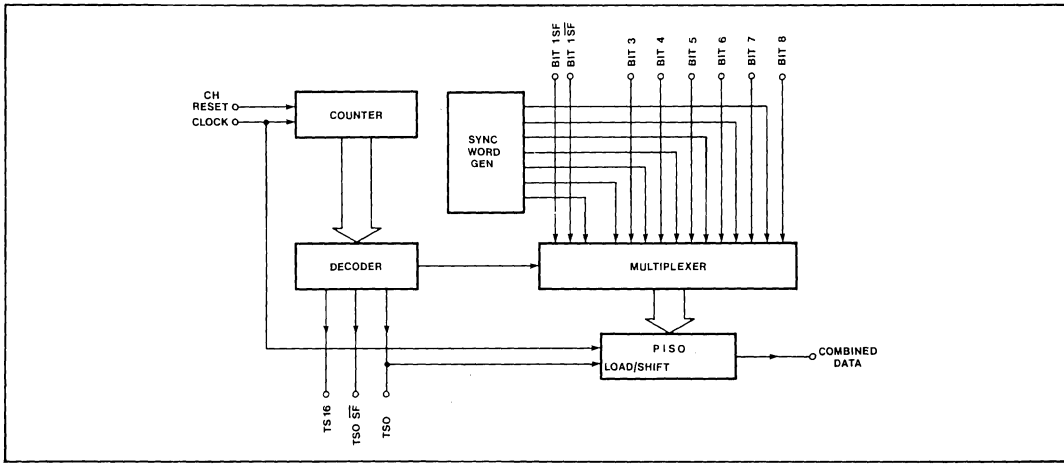


Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient operating temperature $-10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	−0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15 10			0.5 0.7	V V	$I_{sink} = 2mA$ $I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3			MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_P	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

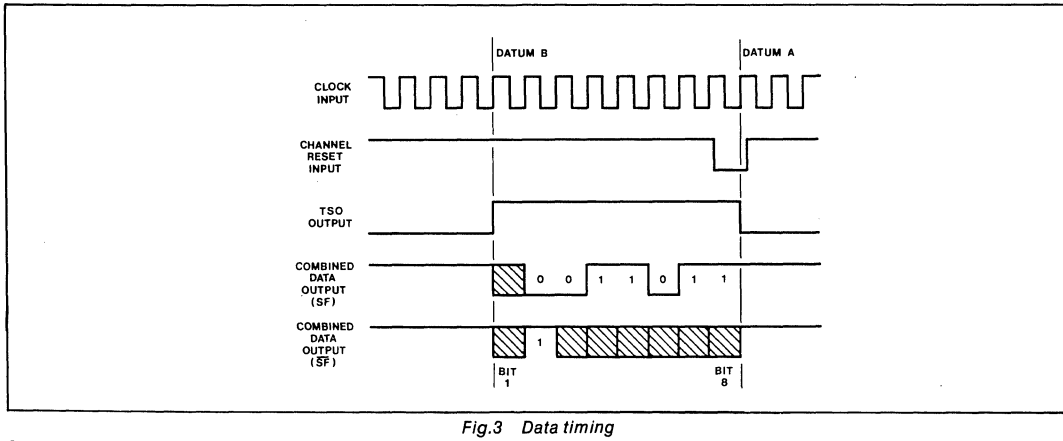


Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8
Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset
A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock
System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16
This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND
Zero volts.

9. TS0 $\overline{SF}$
This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data
This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X—indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0
This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}
Positive supply, 5V ±5%.

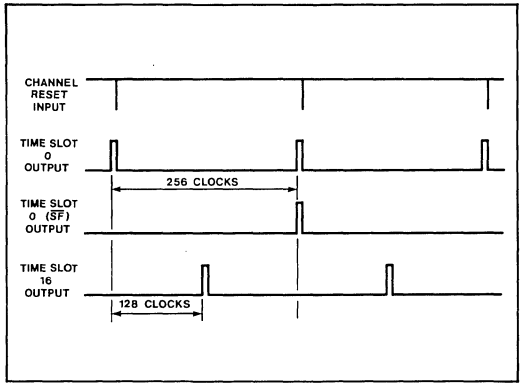


Fig.4 Sync. timing

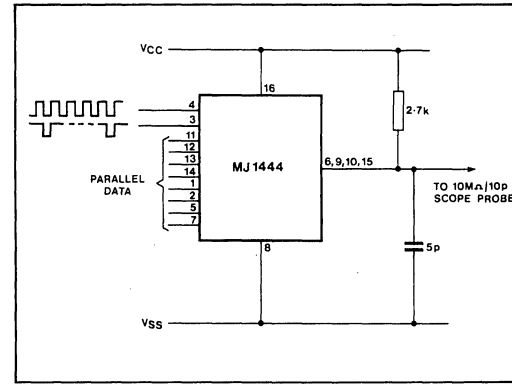


Fig.5 Test conditions (all outputs)

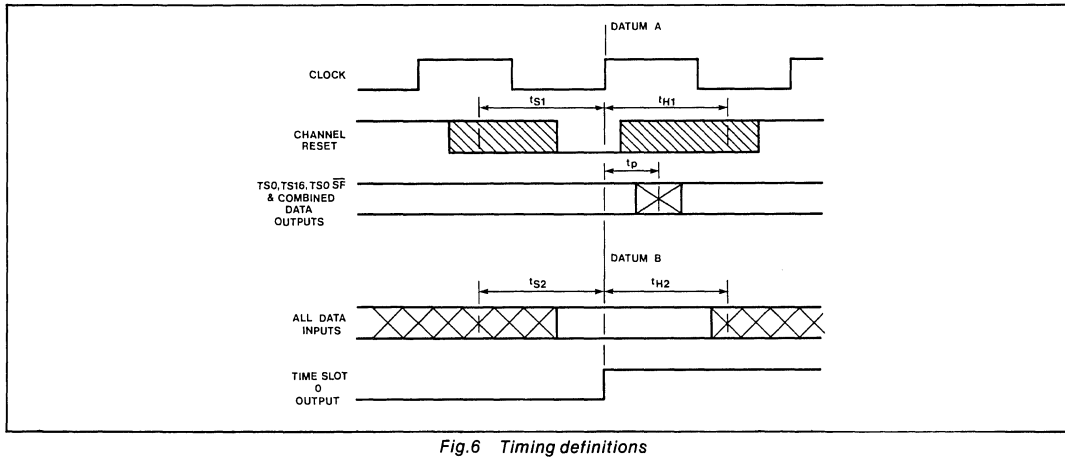


Fig.6 Timing definitions

2 MBIT PCM SIGNALLING CIRCUIT

MJ1445

PCM SYNCHRONISING WORD RECEIVER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1445 establishes synchronisation by detecting the synchronising word when it is received at the remote end of the transmission system. The MJ1444 has been designed to generate this synchronisation word at the sending end of the system in accordance with CCITT recommendation G732.

Corruption of individual synchronisation words is signified by an 'Error' output, loss of synchronisation is indicated by a 'Sync Alarm' output and follows CCITT G732 in that loss of synchronism is assumed when 3 consecutive synchronisation words have been received with errors.

The 'Channel Reset' output goes low for the first period of the clock after time slot 0 in sync frames whenever the MJ1445 has established that the receiver terminal is in synchronisation in order that the rest of the receiver terminal may be reset.

The 'TSO' output is high for a period of 8 bits starting from the end of the first bit of the synchronising word. The spare data bits from the synchronising word are provided as parallel outputs.

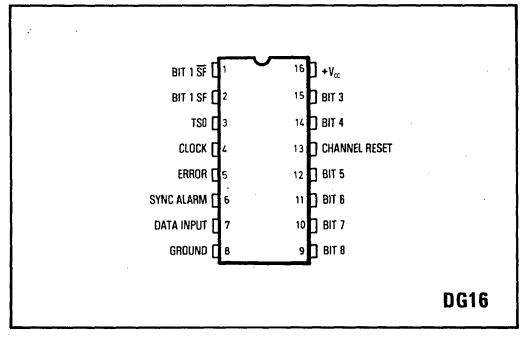


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply – 20 mA Typical.
- Conforms to CCITT Recommendation G732
- Synchronising Word Error Monitor
- Out of Sync. Alarm
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd — 0.3V
Outputs	Vcc, Gnd —0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

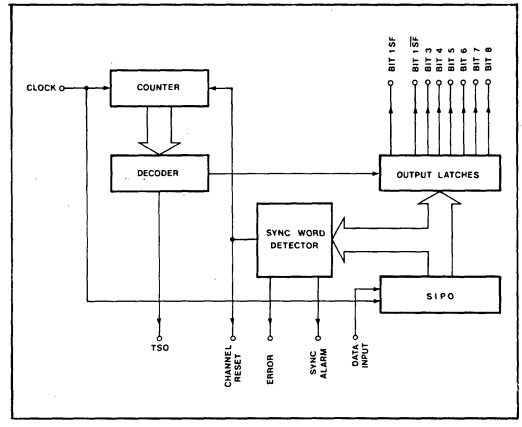


Fig.2 Block diagram MJ1445

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	4, 7	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	4, 7		1	50	μA	
High level input voltage	V_{IH}	4, 7	2.4		V_{CC}	V	
Low level output voltage	V_{OL}	1, 2, 3, 5, 6 9, 10, 11, 12 13, 14, 15			0.5	V	$I_{sink} = 2mA$
High level output voltage	V_{OH}		2.8				$I_{source} = 200\mu A$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock frequency	f_{max}	2.2			MHz	
Input delay of data input	$t_{d\ data}$	20		200	ns	f_{clock} = 2.048MHz
Propagation delay, clock to TS0 output	$t_{d\ TS0}$	40		200	ns	Fig.3
Propagation delay clock to error output, sync alarm and CH. Reset output high	t_d	50		400	ns	Fig.3
Propagation delay, clock to CH. Reset output low (T — t_p)	t_p	100		450	ns	Fig.3
Propagation delay clock to spare bits	$t_{d\ SB}$	50		300	ns	Fig.3

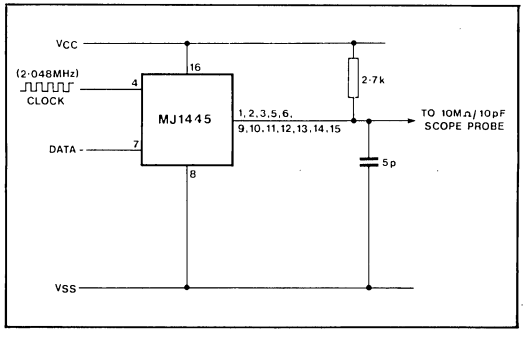


Fig.3 Test conditions, all outputs

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Bit 1 $\overline{SF}$
This output is set to the level of data bit 1 during time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

2. Bit 1 SF
This output is set to the level of data bit 1 during time slot 0 of sync frames. The data becomes true on the first falling edge of the clock during TS1.

3. TS0
This output provides a positive pulse of 8 clock periods in every frame starting from the end of the first bit of the synchronising word of the received data.

4. Clock
System clock input (2.048MHz for a 2MBit PCM system).

5.Error
This output goes high at the end of time slot 0 in the 2nd sync frame following the frame with sync word errors. If consecutive sync words occur with errors this output will remain high. If a sync alarm is generated this output will remain high until sync is regained.

6. Sync Alarm
This output goes high at the end of time slot 0 output in the 3rd consecutive sync frame containing sync word errors. It returns low at the end of TS0 output in the 3rd consecutive frame received correctly (sync and non sync).

7. Data input
Serial data (2MBit/s) at this input is clocked through the SIPO shift register and examined by the sync word detector.

8. GND
Zero volts

9, 10, 11, 12, 14, 15. Bits 3 to 8
These parallel outputs are set to the level of the spare data bits (3 to 8) of time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

13. Channel reset
This output goes low for the first period of the clock after time slot 0 of the received data as long as synchronisation has been established. This pulse can be used to reset the rest of the receiver terminal.

16. V_{CC}
Positive supply 5V ±5%.

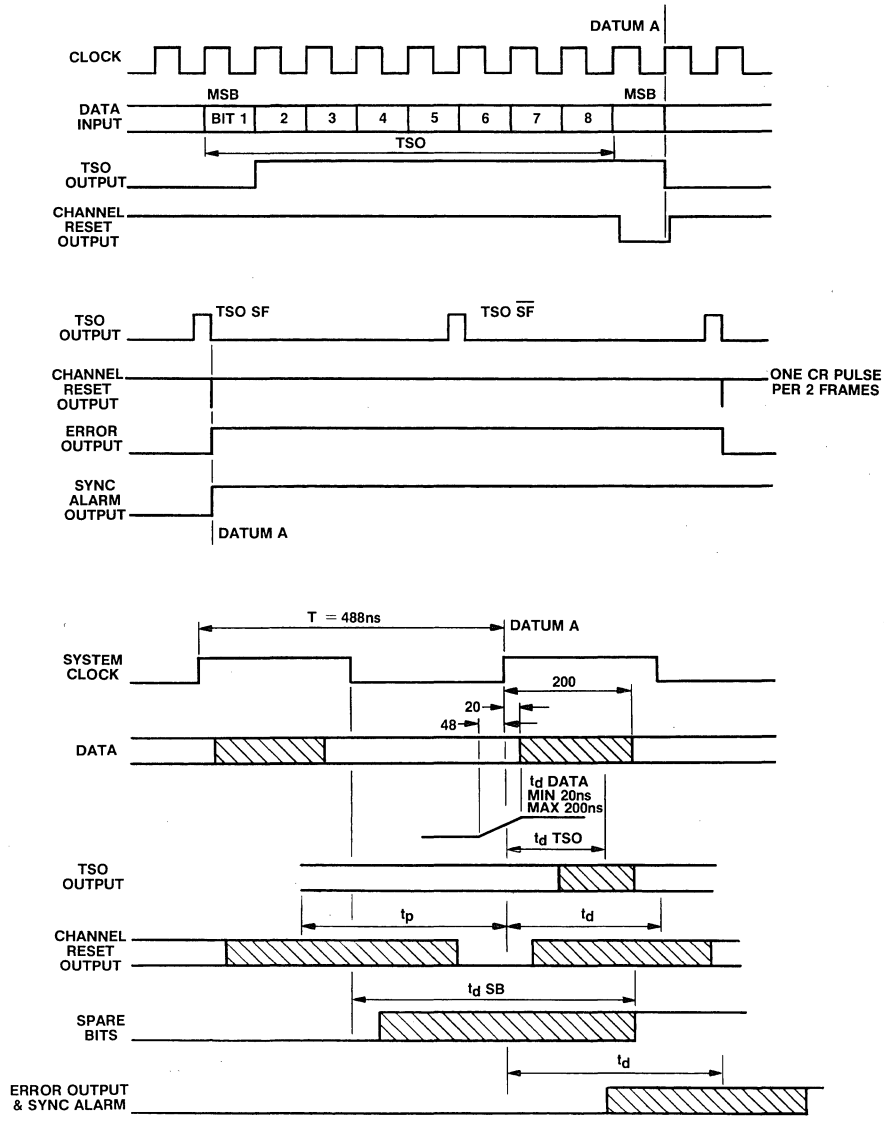


Fig.4 Timing diagram and output waveforms

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ1446

TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependent on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64kbits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

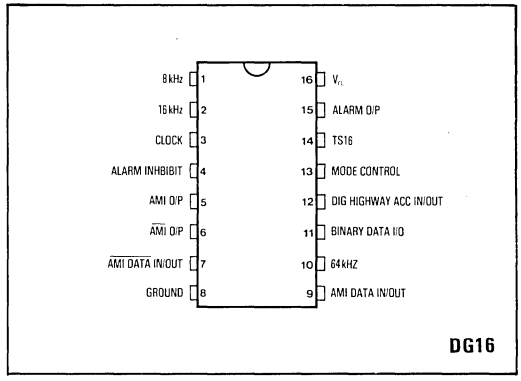


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply—20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receiver or Transmit
- All Inputs and Outputs are TTL Compatible.

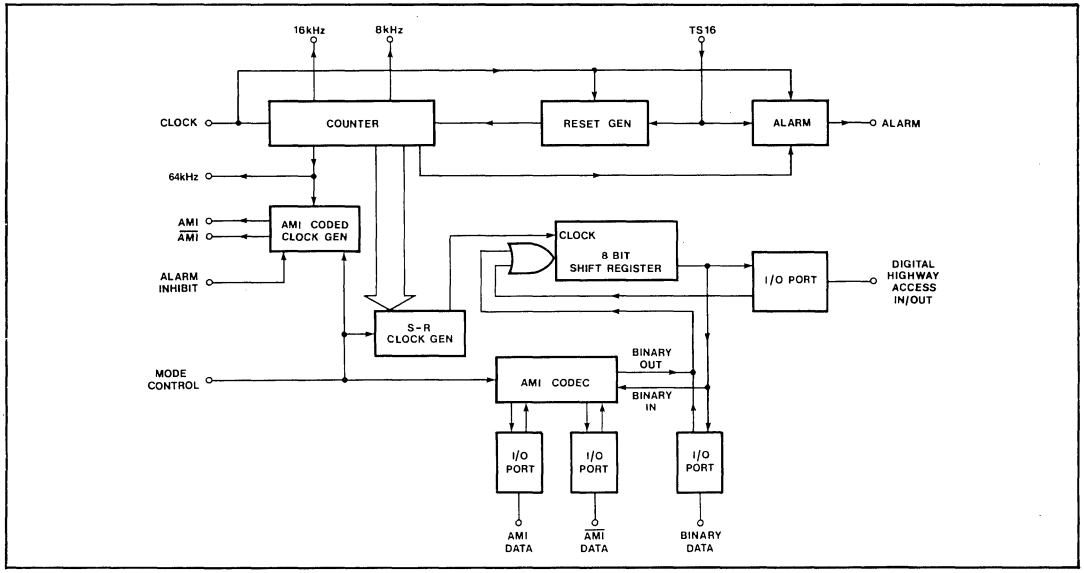


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} = 5V ± 0.25V, Ambient temperature T_{amb} = -10°C to +70°C,

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	I_{sink} = 2mA
		12			0.5	V	I_{sink} = 5mA
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	I_{source} = 200μA
High level output leakage current	I_{CH}	7, 9, 11, 12			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	V_{CC} = 5.25V

Dynamic Characteristics (f_{clock} = 2.048 MHz)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\,DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\,TS16}$	80		200	ns	
Output delay 64kHz to 16kHz output	$t_{p\,16}$			70	ns	Fig.7
Output delay, 64kHz to 8kHz output	$t_{p\,8}$			170	ns	Fig.7
Output delay, 64kHz to binary data output (64kHz)	$t_{p\,BIN}$	20		450	ns	Fig.8
Output delay 64kHz to AMI, $\overline{\text{AMI}}$, AMI data & $\overline{\text{AMI}}$ data o/p's	$t_{p\,AMI}$	20		400	ns	Fig.8
Input delay, 64kHz to binary data in (64kHz)	$t_{d\,BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8kHz
8kHz square wave output.

2. 16kHz
16kHz square wave output.

3. Clock
System clock input (2.048MHz for a 2Mbit PCM system)

4. Alarm inhibit
A high level on this input inhibits the 8kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64kHz.

6. $\overline{\text{AMI}}$ output

7. $\overline{\text{AMI}}$ Data in/out
In the transmit mode 64kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

8. GND
Zero volts.

9. AMI Data in/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64kbits/sec in AMI format.

10. 64kHz
64kHz square wave output.

11. Binary data in/out
In the transmit mode 64k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64k bits/sec in binary format.

12. Digital Highway access in/out
In the receive mode 2Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2Mbits/sec.

13. Mode control
A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16
This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output
A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}
Positive supply 5V ±5%.

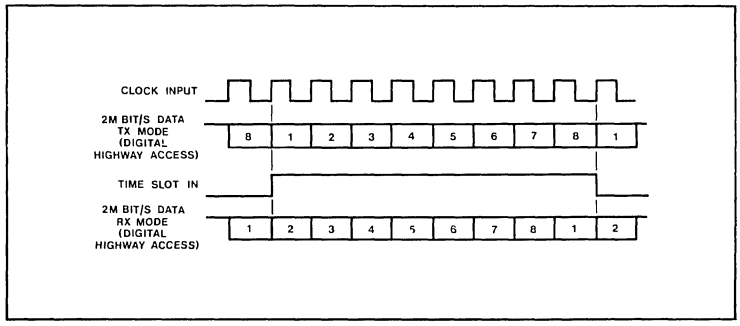


Fig.3 2MBit/s operation

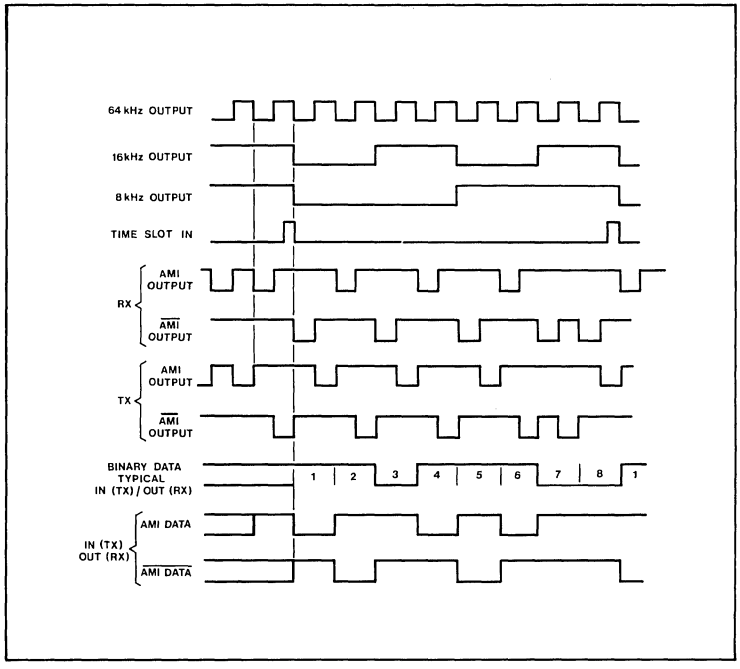


Fig.4 64kBit/s operation

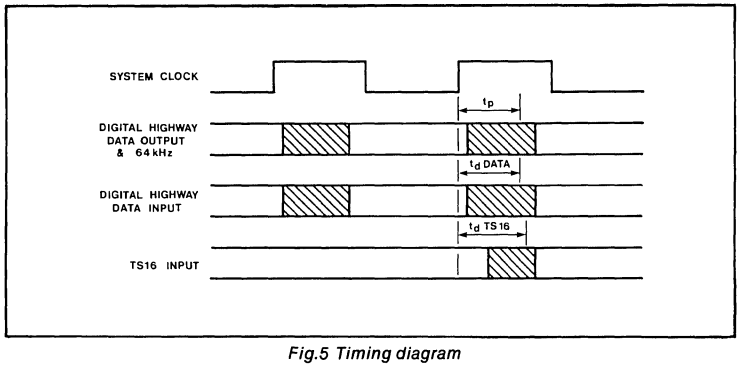


Fig.5 Timing diagram

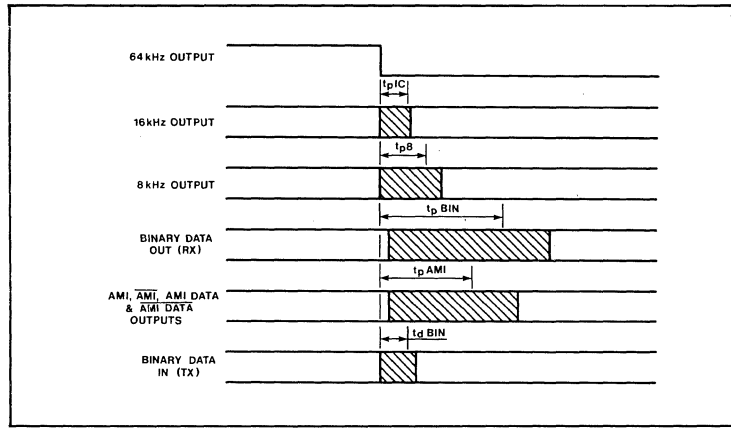


Fig.6 Timing diagram

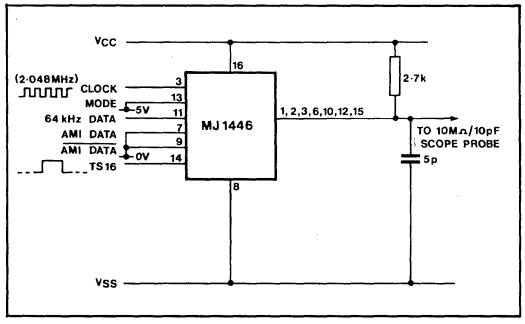


Fig.7 Test conditions (transmit mode)

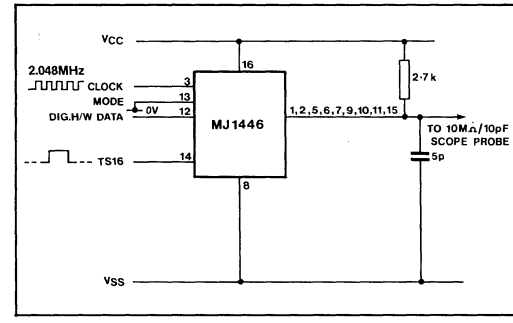


Fig.8 Test conditions (receive mode)

MS2014

DIGITAL FILTER AND DETECTOR (FAD)

The MS2014 is a real time general purpose digital signal processor (DSP) which is easily programmed to perform digital filtering and level detection. The architecture of the FAD comprises a cascadable second order recursive filter and level detector using dedicated multipliers, adders and delay elements.

The data controlling the response of the MS2014 is stored in an external PROM or RAM and consists of a list of filter coefficients and comparison levels. This simple data format means that the user does not need an expensive development system at the design stage (in contrast to other DSP devices, which use microprocessor-based structures and require considerable software development effort to realise their function). The off-chip data memory allows for easy adaptive control, even when complicated algorithms are to be implemented.

The filter and detector have been designed to give maximum flexibility in use and can easily generate most of the functions required in tone detector, spectral analysis, adaptive filter and speech synthesis systems.

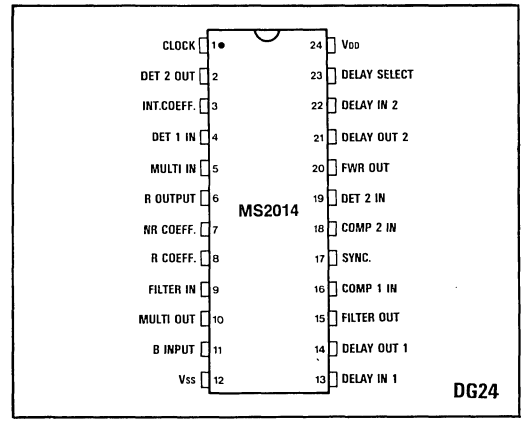


Fig.1 Pin connections - top view

FEATURES

- Linear 16-Bit Data
- 13-Bit Coefficient
- 2MHz Operating Clock Frequency
- Serial Operation
- 448 Bits of On-Chip Shift Register Data Storage for 8th Order Multiplex
- Nth Order Multiplexing ($N \leqslant 8$)
- TTL Compatible
- Single +5V Supply

APPLICATIONS

- Low Cost Digital Filtering
- Level Detection
- Spectral Analysis
- Tone Detectors (Multi-Frequency Receivers)
- Speech Synthesis and Analysis
- Data Modems
- Group Delay Equalisers (All-Pass Networks)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.5V to +7V
Input voltage	-0.5V to +7V
Maximum output voltage	+7V
Temperature: Storage	-65°C to 125°C
Operating	0°C to 70°C

NOTE
All voltages with respect to Vss.

PIN NAMES

	Name	Function	I/O
1	Clock	Single phase clock input	I
2	Detect 2 Out	Output from detector 2	O
3	Int.Coeff	Integrator coefficients	I
4	DET 1 In	Detector 1 input	I
5	Mult In	Input to NR B multiplier	I
6	R Output	Output of recursive section	O
7	NR Coeff	Non-recursive (NR) coefficient input	I
8	R Coeff	Recursive coefficient input	I
9	Filter In	Data input to filter section	I
10	Mult Out	Output from B multiplier	O
11	B Input	Input from B multiplier	I
12	Vss	0V	
13	Delay In 1	Input from filter external delay	I
14	Delay Out 1	Output to filter external delay	O
15	Filter Out	Data output from filter section	O
16	Comp 1 In	Comparison level 1 input	I
17	Sync	Synchronisation pulse input	I
18	Comp 2 In	Comparison level 2 input	I
19	DET 2 In	Input for detector 2 via FWR	I
20	FWR Out	FWR output from Det 2 In data	O
21	Delay Out 2	Output from detectors 1 and 2, and connection to detector external delay	O
22	Delay In 2	Input from detector external delay	I
23	Delay Select	Internal/External delay selector	I
24	VDD	+5V supply	

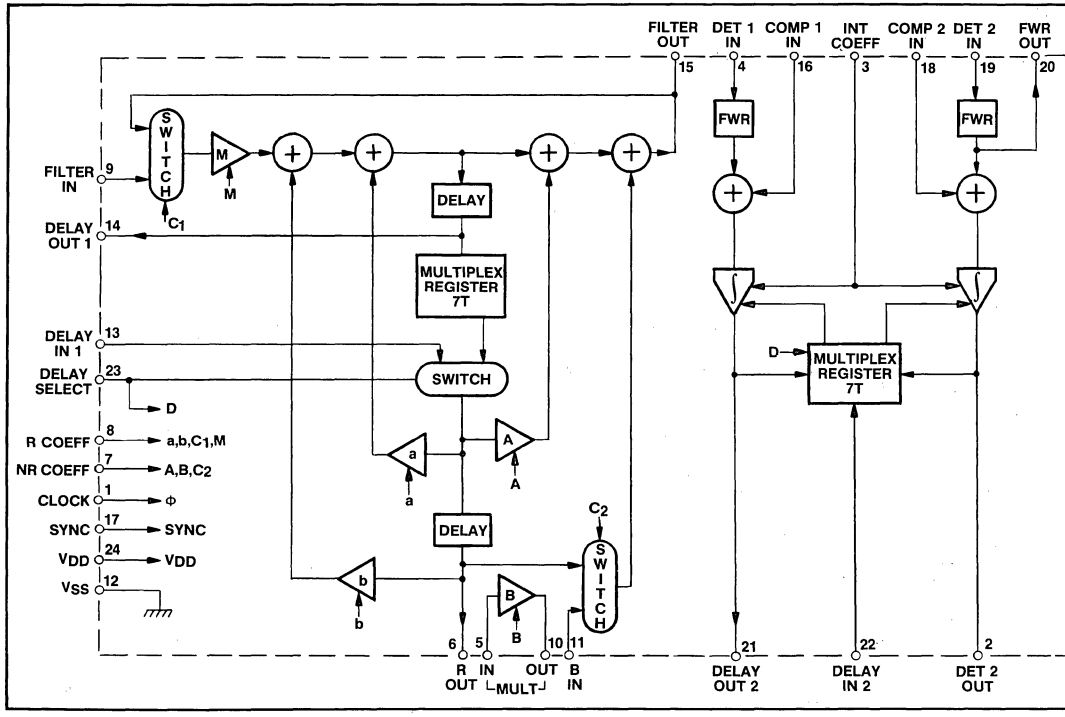


Fig.2 Block diagram

PERFORMANCE

A sample throughput of 64000 samples/s is guaranteed. Thus using a sampling period of 125μs (8000 samples/s) the following may be realised:

8 bi-quadratic 2nd-order recursive filter sections;
plus 16 full-wave rectification operations;
plus 16 1st-order leaky integrations;
plus 16 level comparisons.

Filters of more than 16th order are possible but will require a lower sampling rate or more than one MS2014.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Supply voltage	V_{DD}	4.75	5.25	V	
Input voltage (high state) except clock	V_{IH}	2.2	-	V	
Input voltage (low state) except clock	V_{IL}	-	0.7	V	
Input voltage (high state) clock	V_{IHC}	4.5	-	V	
Input voltage (low state) clock	V_{ILC}	-	0.5	V	
Clock rise and fall time	t_{cl}		30	ns	10% - 90% (Note 1)
Clock frequency	f_{cl}	0.5	2.048	MHz	
Operating temperature	T_{amb}	0	70	°C	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V T_{amb} = 25° C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		90	120	mA	
Output voltage, low	V_{OL}	-	-	0.5	V	I_{OL} = 0.4mA (Note 2)
Output voltage, high	V_{OH}	2.7	3.4	-	V	I_{OH} = -40μA (Note 2)
Input capacitance (except clock)	C_{in}		5	7	pF	
Input capacitance (clock)	C_{inc}		25		pF	
Input data set up time	t_{is}	50	-	-	ns	Fig.7
Input data hold time	t_{ih}	150	-	-	ns	Fig.7
Output data delay time	t_{os}	-	-	200	ns	Fig.7

NOTES
1. An operating clock frequency of 2.048MHz is guaranteed over the supply voltage range and the full operating temperature range.
2. The output stage is designed to drive a standard TTL LS gate (74LS series).

FUNCTIONAL DESCRIPTION

The Filter Section

The filter section provided in the MS2014 is a second order recursive type (see Fig.3). This structure was chosen because of its good coefficient sensitivity and predictable round-off, limit-cycle and overflow properties. Higher order filters are easily produced by cascading sections in a similar manner to analogue active filter design.

The transfer function of the section is given by:

$$H(z) = M \frac{[1 + Az^{-1} + Bz^{-2}]}{[1 - az^{-1} - bz^{-2}]} \quad \ldots (1)$$

The coefficients *a* and *b* define a pair of complex poles, whilst *A* and *B* define a pair of complex zeros. The Scaling Factor *M* is necessary because many filters have greater than unity gain, hence there is a danger of numeric overflow in the filter arithmetic. In the MS2014 this scaler multiplies by a factor of

$$M = (\tfrac{1}{2})^n \text{ where } 0 \leqslant n \leqslant 13$$

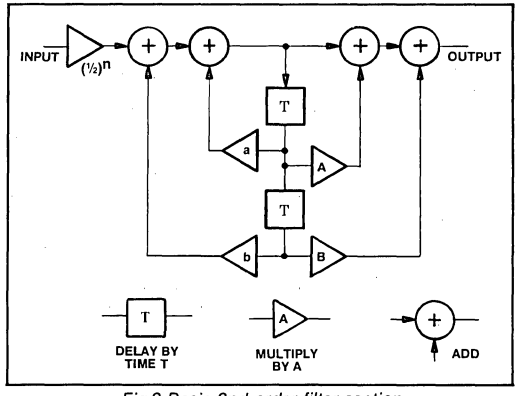


Fig.3 Basic 2nd order filter section

The multipliers in the MS2014 are serial/parallel types which require the coefficient data as a static parallel word. To minimise the number of pins on the device, this data is loaded serially and stored in a SIPO shift register. Each multiplier requires the coefficient data to be in 2s complement form with 12 bits for the fractional part of the number.

The range for the coefficients are:

$$2 > A \geqslant -2$$
$$2 > a \geqslant -2$$
$$1 \geqslant B \geqslant -1$$
$$1 > b \geqslant -1$$

For the *A,a* coefficients there is an added bit ($a_S A_S$) to give the extra ±1 range, which gives a total of 14 bits for the *A,a* coefficients and 13 bits for *B,b*.

The second-order filter is very easily multiplexed by increasing the delay function in steps of *T* (where *T* is the computation period*) and time-sharing the arithmetic elements. The limit on this process is the maximum clock rate of the MS2014. With a 32 bit computation cycle the clock rate f_{cl} is given by:

$$f_{cl} = 32 \times f_s \times Y$$

where *Y* is the number of times the filter is multiplexed and f_s is the sampling rate (the reciprocal of the sampling period T_s **). In telephony applications it is usual for f_s to be 8000 samples/s; hence at the maximum guaranteed clock rate of 2048kHz, *Y* must be less than or equal to 8.

By presenting an input sample during every 32-bit computation cycle, 8 separate second-order filters can be implemented. As the inputs can be independent of each other the filter is then said to be 'channel multiplexed'.

Filters of higher order can be built by feeding the output data emerging from one second-order section back to the input via an on-chip data selector, which is enabled by the control bit C_1; since the delay between the input and output of the filter section is 32 clock periods, the data arrives at the beginning of the next computation cycle. Thus by controlling the data selector two or more second-order filter sections can be cascaded. This arrangement allows any combination of filter and channel multiplexing to be achieved.

Higher orders of channel or filter multiplex require the connection of additional delay. For 8th-order multiplex, a delay of *7T* (224 bits) is provided on chip; together with the inherent delay *T* (32 bits) of the computation cycle, this

*T = computation period = 32 x (1/2048k)s = 15.63μs i.e. 32 bits at 2048 kbit/s clock rate.

**Ts = sampling period = (1/8000)s = 125μs at a sampling rate of 8kHz i.e. 256 bits at 2048 kbit/s clock rate.

makes up the necessary $8T$ delay. Other orders of multiplex require the external connection of $(Y - 1) \times 32$ bits of delay.

The detector function is carried out by 'full wave rectifiers' followed by comparators and leaky integrators. By interconnecting these in different ways various absolute and relative level decisions can be made.

The 'Full Wave Rectifiers'

Data entering the 'full wave rectifiers' is inverted if the sign bit of the word is a '1' (i.e. negative). The 1LSB error generated by this is insignificant and does not materially affect operation of the detector.

The Integrators

The integrators in the MS2014 are unity gain variable-leak-factor types. Fig.4 shows the internal arrangement. The leak factor

$$1\text{-}2^{-(K\ +\ 1)}$$

controls the rise time of the integrator, the relationship is given in Table 1.

Level Detection

Both relative and absolute level detectors can be implemented in the MS2014. Fig.5 shows the arrangement for an absolute level detector. The sign bit of the data word emerging from the integrator is '1' if the mean level of the filter output is greater than the comparator input level.

Relative level detection can be achieved by using the arrangement of Fig.6. In most applications where relative level sensing is required, the filtering can be arranged such that $B = 1$ (i.e. the complex zeros are located on the unit circle in the z plane), this allows the B multiplier to be used for scaling the relative levels. In this application the B coefficient must be negative.

Leak factor	Rise time (0 to 90%)
1/2	3 Ts + T
3/4	8 Ts + T
7/8	17 Ts + T
15/16	35 Ts + T
31/32	72 Ts + T
63/64	146 Ts + T
127/128	293 Ts + T
255/256	588 Ts + T

Table 1 Integrator rise times

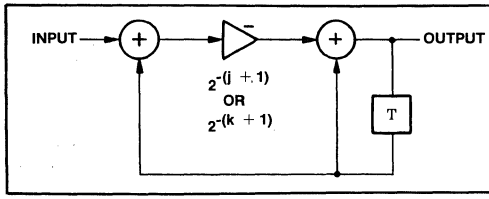


Fig.4 Leaky integrator

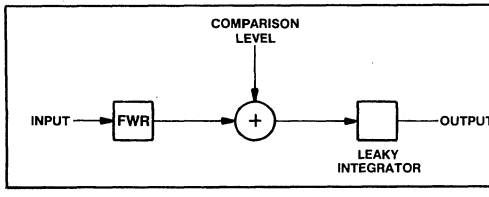


Fig.5 Simple level detector

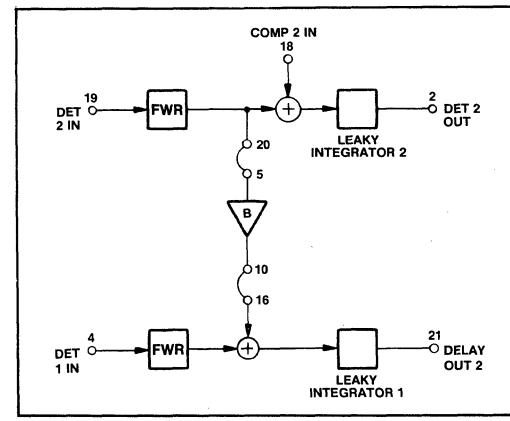


Fig.6 Relative level detection

FILTER DESIGN WITH THE MS2014

One of the commonest techniques for designing analogue filters is to factor the transfer function into blocks which can be realised by second order filter sections. Most designs of this type are done using tables which give coefficients for equations of the form:

$$H(s) = \frac{Cs^2 + Ds + K}{Es^2 + Fs + 1} \quad \text{... (2)}$$

Since the MS2014 filter section is a general second-order structure, the same design technique can be employed. By using the Bilinear Transform:

$$s = \frac{2\ (1 - z^{-1})}{T\ (1 + z^{-1})} \quad \text{... (3)}$$

it is possible to design digital filters from analogue prototypes. By substituting equation (3) into (2) and re-arranging the result into the form of equation (1) the following relationships are derived:

$$A = \frac{2KT^2 - 8C}{4C + 2DT + T^2}$$

$$a = \frac{8E - 2T^2}{4E + 2FT + T^2}$$

$$M = \frac{4C + 2DT + KT^2}{4E + 2FT + T^2} \quad \text{... (4)}$$

$$B = \frac{4C - 2DT + KT^2}{4C + 2DT + KT^2}$$

$$b = \frac{2FT - 4E - T^2}{4E + 2FT + T^2}$$

These five equations allow an analogue filter design to be transformed into digital form.

In addition to the four coefficients required by the filter section the data streams fed to the NR and R coefficient inputs include the four bits setting the Scaling Factor M (M_1 to M_4) and two selector control bits C_1 and C_2.

When $C_1 = 1$, data applied to FILTER IN (pin 9) goes to the filter section, when $C_1 = 0$ data emerging on FILTER OUT (pin 15) is fed back to the filter at the start of the next computation cycle.

When $C_2 = 0$ the B multiplier is by-passed by a direct connection, setting $B = 1$.

Table 2 shows the format of the serial data words for the NR and R coefficient inputs. The timing diagram (Fig.7) shows where this fits into the computation cycle. The synchronising pulse (SYNC) is coincident with the first clock pulse of the cycle and must be low before the rising edge of

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Clock Pulse Number
C_1	M_1	M_2	M_3	M_4	b Coeff. msb												lsb	a_s	a Coeff. (Recursive) msb													lsb	
X	X	X	X	C_2	B Coeff. msb												lsb	A_s	A Coeff. (Non-Recursive) msb													lsb	
0.125					0													0.73217773437														
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	1	0	1	1	1	R
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NR

Table 2 Filter data format

the clock. The SYNC pulse is applied every *Y* clock pulses, where *Y* = CLOCK RATE/SAMPLING RATE.

Coefficient Conversion

After the coefficients have been obtained (from the Bilinear Transform or FAD Development Program) they must be assembled in the format given in Table 2. The FAD Development Program gives the multiplier coefficients in a ready-to-use binary string format, other techniques will give numerical values for the coefficients which must be converted into binary strings.

Coefficient Conversion Algorithm for '*A*'

The algorithm for converting *A* or *a* to binary is as follows:

Obtain $A = \frac{|A|}{2} . 8191$

Convert *A* into a binary number (13 bits)

If *A* is positive INVERT THE MSB AND APPEND '0' AS NEW MSB.

If *A* is negative INVERT ALL BITS AND APPEND '1' AS NEW MSB, then ADD '1' LSB.

Conversion of '*B*' Coefficients

Obtain $B = B.4096$

Convert *B* into a binary number (12 bits)

If *B* is negative INVERT ALL BITS, ADD '1' LSB AND APPEND '1' AS NEW MSB.

If *B* is positive APPEND '0' AS NEW MSB.

In addition to the coefficient data streams one further input must be set up. DELAY SELECT (pin 23) is the control pin used to select the internal *7T* delay. A '1' maintained on pin 23 selects the internal delay and a '0' the external option. The *B* multiplier is independent of the rest of the circuit and may be used for any purpose, although usually it will form part of either the filter or detect functions. In each case the appropriate connections must be made externally.

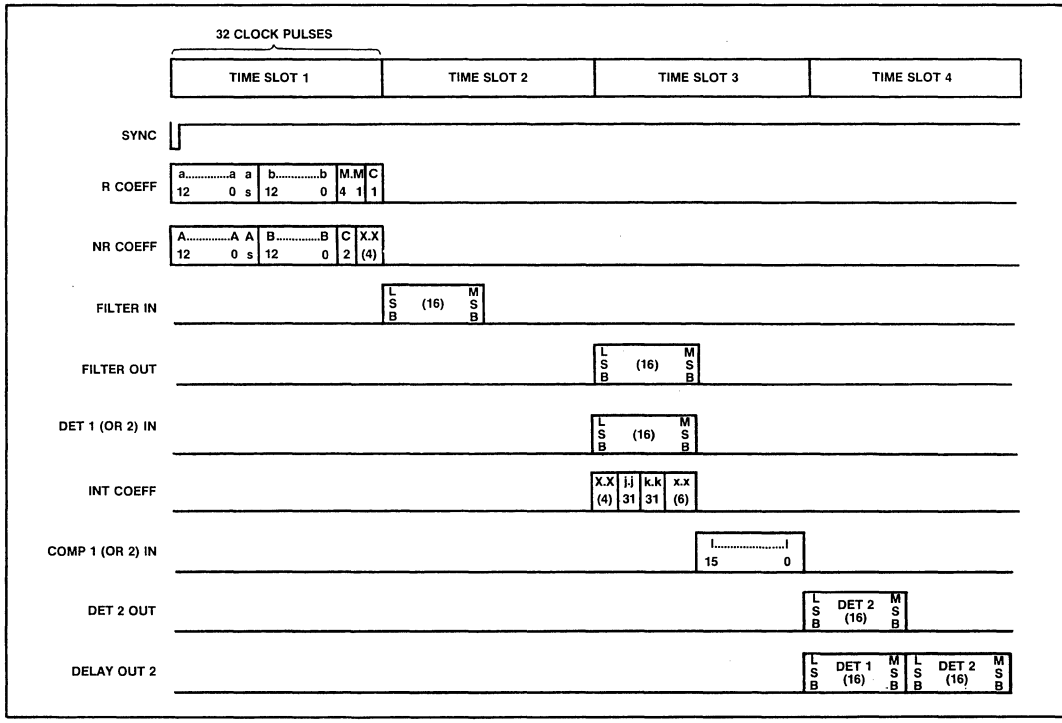


Fig.7 Timing diagram

Clock pulse number	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Integrator coefficients	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	K_1	K_2	K_3	J_1	J_2	J_3	X	X	X	X
Comparison level 1 or 2	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{15}	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 3 Detector data format

Programming the Detector

Control data for the detect function is supplied by an external memory to the INT COEFF input (pin 3) and to the COMP 1 IN and COMP 2 IN inputs (pins 16 and 18) of the MS2014. The relative positions in time of the input sample data, detect function control data and output sample data are shown on the timing diagram (Fig.7).

Note that it is possible to economise on memory by strapping pin 3 either to pin 16 or to pin 18, since valid data for either combination of pins occurs at different times in the computation cycle. There are two integrator scaling factors in the INT COEFF data stream. The j_1, j_2, j_3 data bits determine the integrator coefficient for the data stream applied to DET 1 IN (pin 4) and the k_1, k_2, k_3 data bits for the DET 2 IN (pin 19) data stream; their definitions and clock pulse positions are given in Table 3.

In most applications, the comparison levels *l* and *m* applied to COMP 1 IN (pin 16) and COMP 2 IN (pin 18) will be negative quantities, and as they are coded in two's complement, each sign bit at clock pulse 32 will be a '1'. However,a positive quantity can be input by setting the sign bit to '0'. In this case, care must be taken to ensure that the addition of the DET data and the COMP data does not result in a number greater than unity and cause overflow, since no protection against overflow is provided in either detect function.

NOTE Round-off errors in the detector section may result in the integrator 'jamming' if the signal is below the 4 LSBs. Consequently, the available dynamic range is limited to the 12 MSBs.

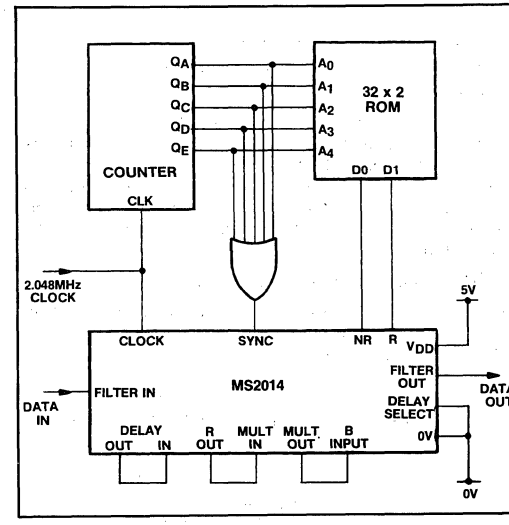


Fig.8 2nd order 32kHz bandwidth filter

TYPICAL APPLICATIONS CIRCUITS

A Second-Order High Sampling Rate Filter (Fig.8)

This is the simplest filter arrangement for the MS2014. No external delay is required so that DELAY 1 IN is connected to DELAY 1 OUT and DELAY SELECT is grounded.

A ÷32 counter generates the 5-bit wide address for the coefficient ROM. A 5-input OR gate on the address lines generates the SYNC pulse every 32 clock cycles so that at a 2.048MHz clock rate the sample rate is 64000 samples/second giving a maximum bandwidth of 32kHz.

If the desired *B* coefficient is not unity then R_{OUT} (pin 16) must be connected to MULT IN (pin 5) and MULT OUT (pin 10) to *B* INPUT (pin 11).

A 16th Order Filter 8kHz Sample Rate Fig.9)

In this example DELAY SELECT (pin 23) is high so that the internal *7T* delay is switched in. Input data is applied during the first computation cycle (the one with the SYNC pulse in it) and coefficient data is loaded in the last computation cycle.

Channel Multiplexed Second Order Filter 8kHz Sampling

The hardware for this filter is identical to Fig.9. However, input data is provided during each computation cycle and each cycle contains a separate output. If the filter required for each channel is identical, then the coefficient memory need only be 32 x 2 bits.

Other Configurations

Sampling rates other than 64kHz and 8kHz can be achieved either by reducing the clock rate and/or by using external delays in place of the internal 0/7*T*. The use of external delay also allows different orders of multiplexing.

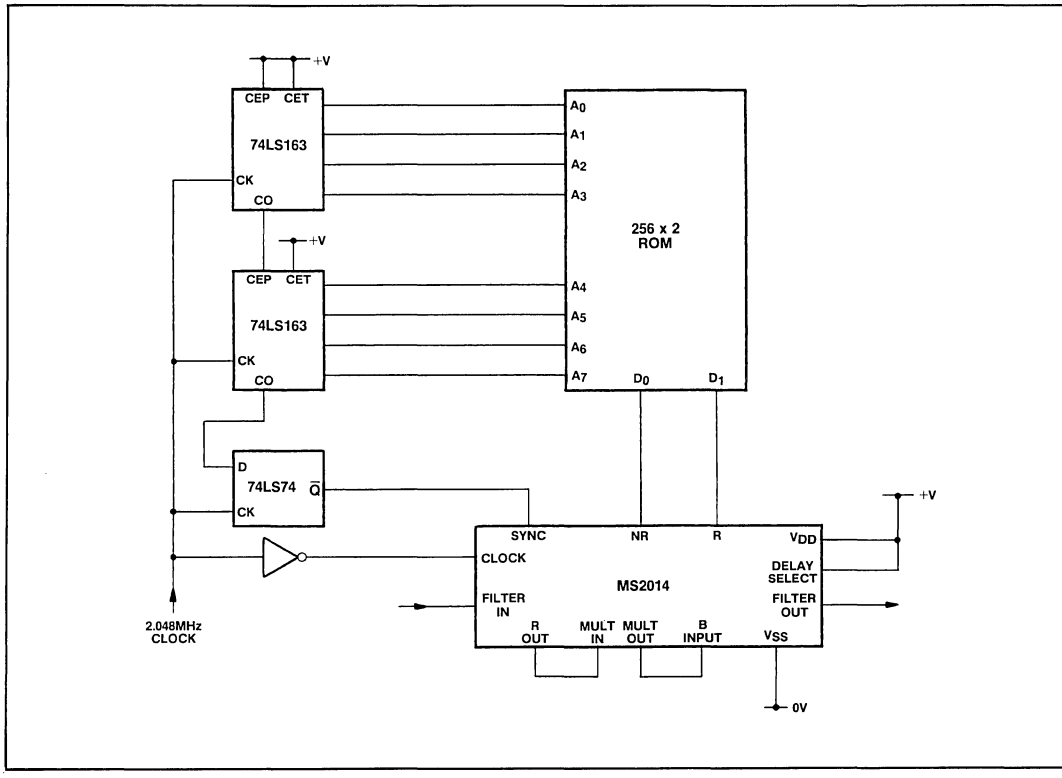


Fig.9 A 16th order 4kHz bandwidth filter

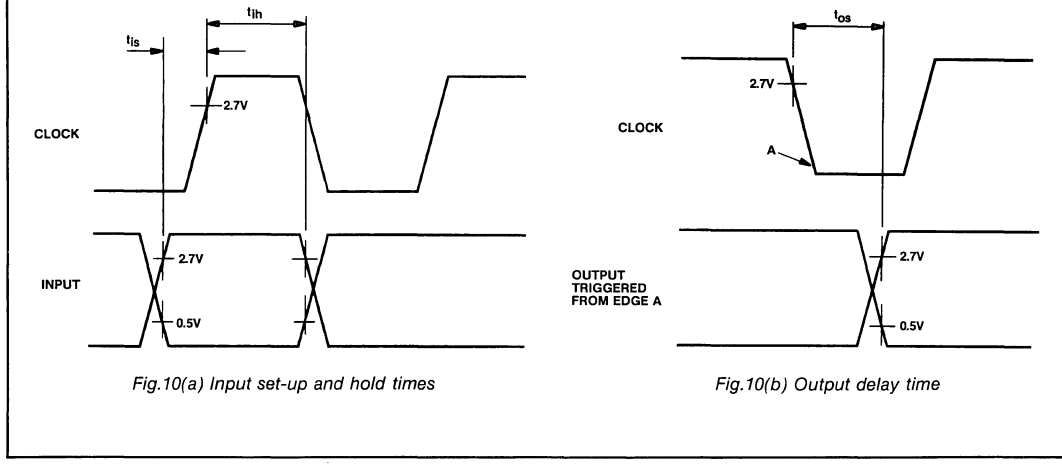


Fig.10(a) Input set-up and hold times

Fig.10(b) Output delay time

Fig.10 Input and output timing

PLESSEY
Semiconductors

MS2002

DIGITAL SWITCH MODULE (DSM)

The Plessey MS2002 is an n-channel MOS LSI integrated circuit providing digital switching for 256 channels in PCM systems. the device is unidirectional in operation and is capable of switching data from any incoming channel to any outgoing channel. Input data can be either serial or parallel. The DSM is designed to be easily expandable to provide a greater switching capacity.

FEATURES

- Single 5V Supply
- TTL Compatible
- Interfaces Directly with European Standard CCITT 32 Channel Format
- 256 Input/256 Output Channels
- Serial or Parallel Inputs and Outputs
- Open Drain Outputs for Easy Expansion
- One System Clock and One Frame Synchronisation Pulse

APPLICATION

- Circuit Switched PCM or Data Systems

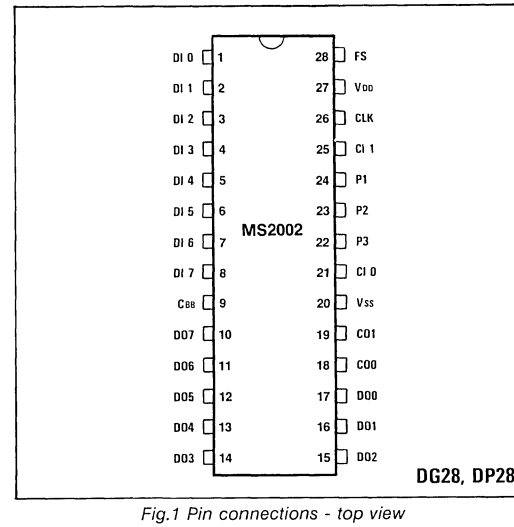


Fig.1 Pin connections - top view

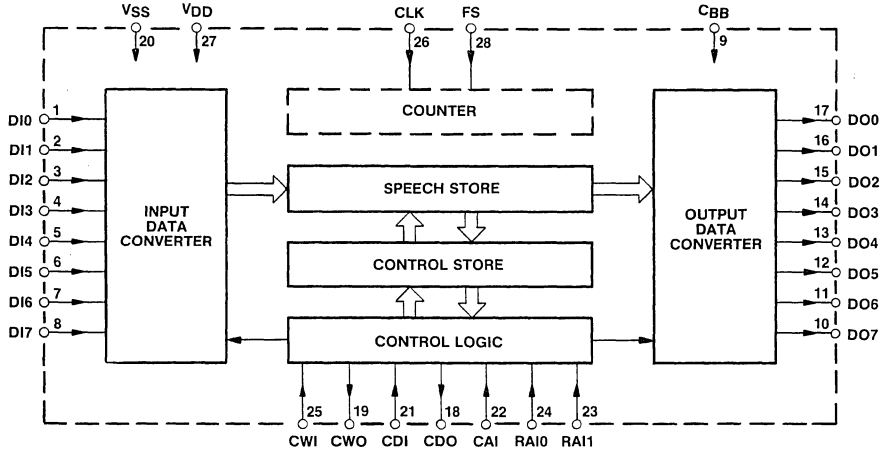


Fig.2 Functional block diagram

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
DI0-DI7	1-8	**Data In 0 to 7 (Digital Inputs).** These are the inputs for the 256 incoming channels. The data presented at these pins is latched on the alternate negative edges of the CLK clock to those used by DO0-7. Frame synchronisation for these pins is established by the FS pulse.
C_{BB}	9	**Bias Decoupling Capacitor (Decoupling Node).** A bias decoupling capacitor of 1000pF should be connected between this pin and V_{SS}.
DO7-DO0	10-17	**Data Out 0 to 7 (Digital Pull-down Outputs).** These are the output pins for the 256 outgoing channels. Data is output at these pins on the alternate negative edges of the CLK clock to those used by DI0-7. Frame synchronisation for these pins is established by the FS pulse.
CDO	18	**Control Data Out (Digital Pull-down Output).** This pin outputs control data bytes. Bit synchronisation and frame synchronisation are stablished by the CLK and FS signal in a similar way as on the DO0-7 pins. It is high impedance for time slots which are not in use for control instructions. It is also high impedance for time slots corresponding to the 'write all ones' instruction. During time slots corresponding to other control instructions this pin outputs either the inverse of the 8 least significant bits at a control store location or the data at the speech store location selected by these 8 bits.
CWO	19	**Control Word Out (Digital Pull-down Output).** This pin outputs control word bytes. Bit synchronisation and frame synchronisation are established by the CLK and FS signals in a similar way as on the DO0-7 pins. It is high impedance for time slots which are not in use for control instructions and for time slots corresponding to the instruction 'write all ones'. During time slots corresponding to other instructions this pin outputs 4 bits which are the same as on CWI and 4 bits which indicate to the status of the chip.
V_{SS}	20	**Negative Supply Voltage (Power Input).** 0V.
CDI	21	**Control Data In (Digital Input).** The control data bytes are latched into the chip at this pin. Bit synchronisation and frame synchronisation are established by the CLK and FS signals in a similar way as on the DI0-7 pins. The bits in the input control data byte are inverted and written into the control store by the instruction 'write CWM bit and CI bits'.
CAI	22	**Column Address In (Digital Input).** This pin defines the column position of a chip in the control array.
RAI 1,0	23, 24	**Row Address In 1, 0 (Digital Inputs).** These pins defined the row position of a chip in the control array.
CWI	25	**Control Word In (Digital Input).** Control word bytes are latched into the chip at this pin. Bit synchronisation and frame synchronisation are established by the CLK and FS in a similar way as on the DI0-7 pins. The bits in the input control word byte control whether reads or writes occur, allow different chips in a control array to be addressed, and control whether connections are busy or free.
CLK	26	**Clock (Digital Input).** The system clock, nominally 4.096MHz, is input at this pin. It is used with the pulse on FS to establish bit synchronisation on the data and control inputs and outputs.
V_{DD}	27	**Positive Supply Voltage (Power Input).** 5V.
FS	28	**Frame Synchronisation (Digital Input).** The negative pulse input at this pin is used with the CLK clock to establish the frame synchronisation on the data and control inputs and outputs. The duration of the pulse determines the modes of the data input and output converters.

Duration (clock periods)	Data Inputs	Data Outputs
1	Serial	Serial
2	Serial	Parallel
3	Parallel	Serial
4	Parallel	Parallel

FUNCTIONAL DESCRIPTION

The MS2002 is a 256 channel non-blocking digital switch capable of connecting all 256 incoming channels to all 256 outgoing channels in any desired order. Alternatively, selected input channels may be broadcast to any number of output channels. Each output channel may, however, receive from only one input channel at a time.

Speech data is input to the device via 8 lines (DI0-7) that can accept 8 bit data in either serial or parallel format at a 2.048Mb/s rate. Speech data is output is via a further 8 lines which may be set independently of the input lines to give serial or parallel format data.

Call routings are held in an on-chip control store in the form of a nine bit word for each outgoing speech channel, bit nine (CM) indicating the busy status of the channel (0 = busy). In the case of a busy outgoing channel the remaining eight bits denote the number of the input channel to be connected to that outgoing channel.

The contents of the control store can be modified, and the speech or control store interrogated, via control messages received over the control inputs (CWI, CDI). Data generated by interrogation of either the control or speech store appears on the two control outputs (CWO, CDO).

Frame Formats

Serial inputs and outputs on the DSM are numbered in the same way as the CCITT 2048kbit/s PCM link (see Fig.3). This applies to both data and control information.

If the DSM is configured for parallel data on the data inputs or outputs then the Parallel Channels are numbered from 0 to 255 (see Fig.4).

These are different frame alignments for inputs and outputs (see Fig.5) The outgoing alignment is delayed by 21 bit periods with respect to the incoming alignment.

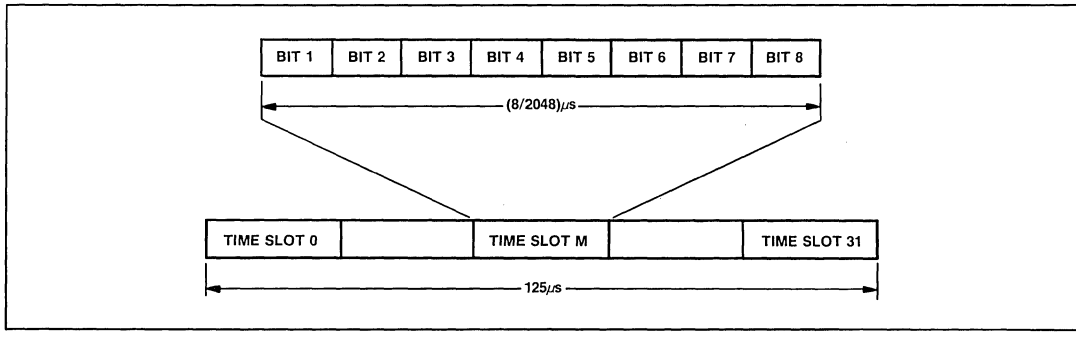


Fig.3 Serial format

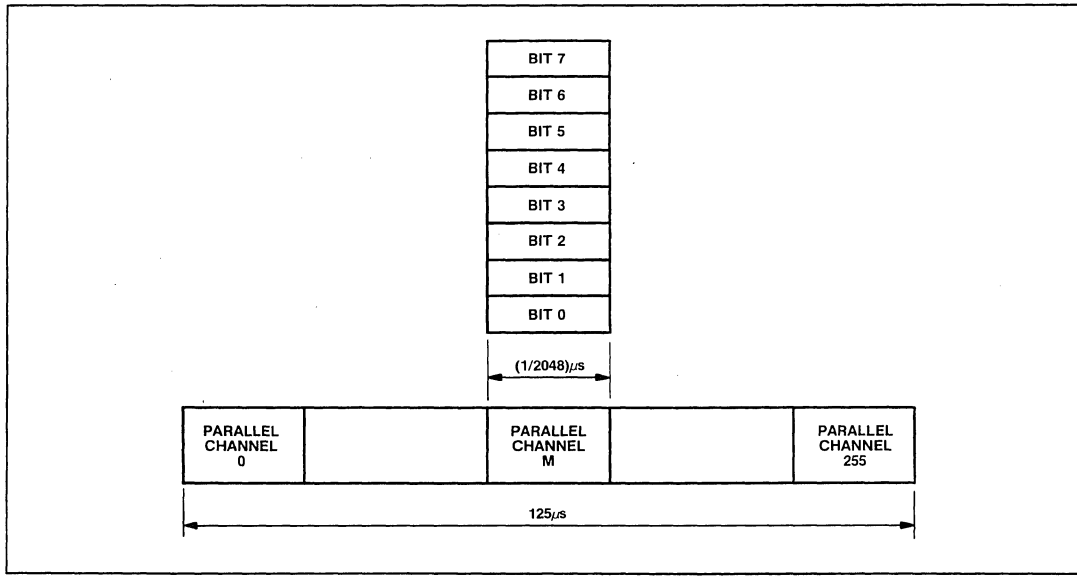


Fig.4 Parallel format

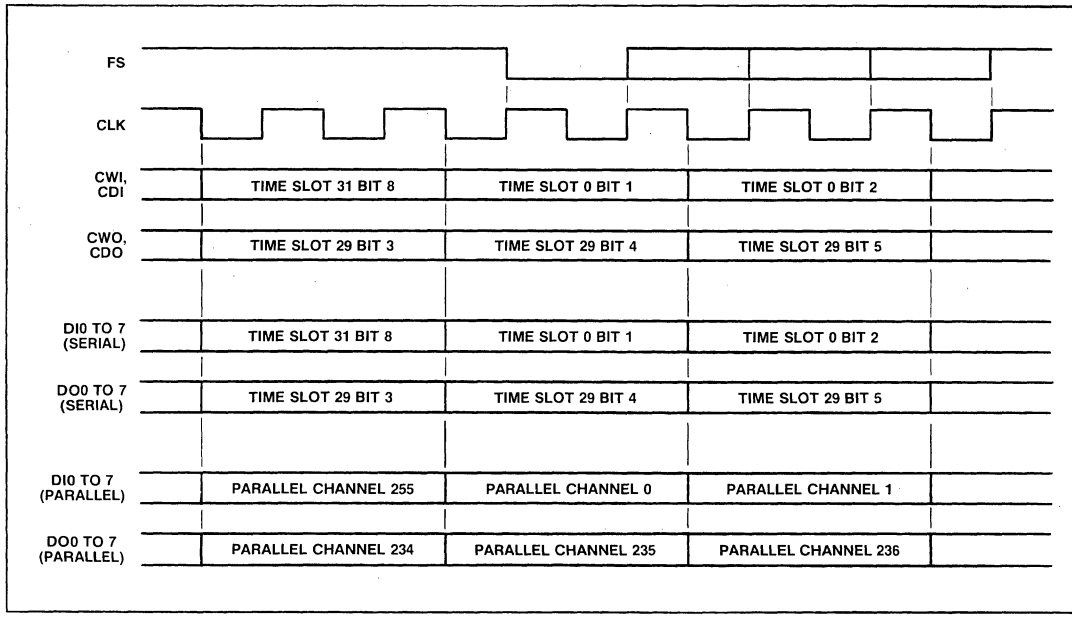


Fig.5 Timing - nominal

Speech Store

The Speech Store has 256 addresses each containing 8 bits. These addresses are associated with the Data In pins. If the DSM is configured for serial input then these addresses are organised by input pin and Time Slot (see Fig.6). If the MS2002 is configured for parallel input then these addresses correspond to the input Parallel Channels.

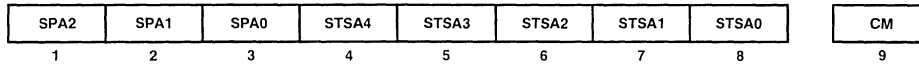
Control Store

The Control Store has 256 addresses each containing 9 bits. These addresses are associated with the Data Out pins in the same way that the Speech Store is associated with the Data In pins (see Fig.6).

Fig.7 shows how the 9 bits at each Control Store address are organised.

Store Address (Speech or Control)	Serial Time Slot Address (Input or Output)	Serial Pin Address (Input or Outut)	Parallel Channel (Input or Output)
0	0	0	0
1	0	1	1
2	0	2	2
3	0	3	3
4	0	4	4
5	0	5	5
6	0	6	6
7	0	7	7
8	1	0	8
9	1	1	9
.	.	.	.
.	.	.	.
.	.	.	.
254	31	6	254
255	31	7	255

Fig.6 Relationship between inputs, outputs and stores



Bit	Name	Description
1-3	SPA2-0	**Speech Pin Address 2 to 0.** These bits are the Serial Pin Address in the Speech Store (see Fig.6). When used with the Speech Time Slot Address bits a unique Speech Store address is specified. This address corresponds to a Parallel Channel if parallel input is used.
4-8	STSA4-0	**Speech Time Slot Address 4 to 0.** These bits are the Serial Time Slot Address in the Speech Store (see Fig.6). When used with the Speech Pin Address bits a unique Speech Store address is specified. This address corresponds to a Parallel Channel if parallel input is used.
9	CM	**Connection Mode.** This bit determines whether the connection is busy or free and also helps to control reads from the DSM. If this bit is 0 then the connection is busy. If it is 1 then the connection is free. Fig.10 shows how this bit affects reads.

Fig.7 Bits at each control store address

Switching Delay

The switching function of the MS2002 is achieved by storing the incoming speech channels sequentially in the 256 x 8 speech store (after conversion to parallel format) and then sending them to the output channels in the order specified by the control store.

The delay encountered by each channel consists of a fixed delay, determined by the format conversion circuitry and the memory read/write cycle time, and a variable delay. The fixed delay is the 21 bits shown in Fig.5.

The variable delay is controlled by the sequence of writing to the speech store and reading from it under the direction of the control store. Input data is written to the speech store addresses in turn (see Fig.6). Output data is obtained by reading the control store addresses in turn and then reading the output data from the specified speech store address.

This means that when an input serial time slot is switched to the same output serial time slot then the delay is 21 bits if the Data In number is less than or equal to the Data Out number. The delay is 21 bits plus one frame if the Data In number is greater than the Data Out number.

The Control Array

The MS2002 is designed to be controlled in an array of two columns and four rows (see Fig.8). This control array need not be fully implemented. For example, a 512 channel switch can be constructed from two columns and two rows. If a large switch is required then control arrays can be arranged in a variety of architectures.

Each MS2002 in the Control Array uses the same control signals. These contain 32 Time Slots of 8 bits each.

The Time Slot used by an instruction is the Time Slot Address in the Control Store (see Fig.6). The format of the bits used for control, which is the same for both input and output, is shown in Figs. 9 and 10.

Instructions to the array are decoded according to the column in the array. The column whose Column Address pin matches the Column Address Bit on Control Word In responds to the instruction.

The write instruction can set up a connection from any one of the 1024 addresses in the Speech Stores of the 4 MS2002s in a row of the control array. The read instructions allow busy connections to be identified and monitored.

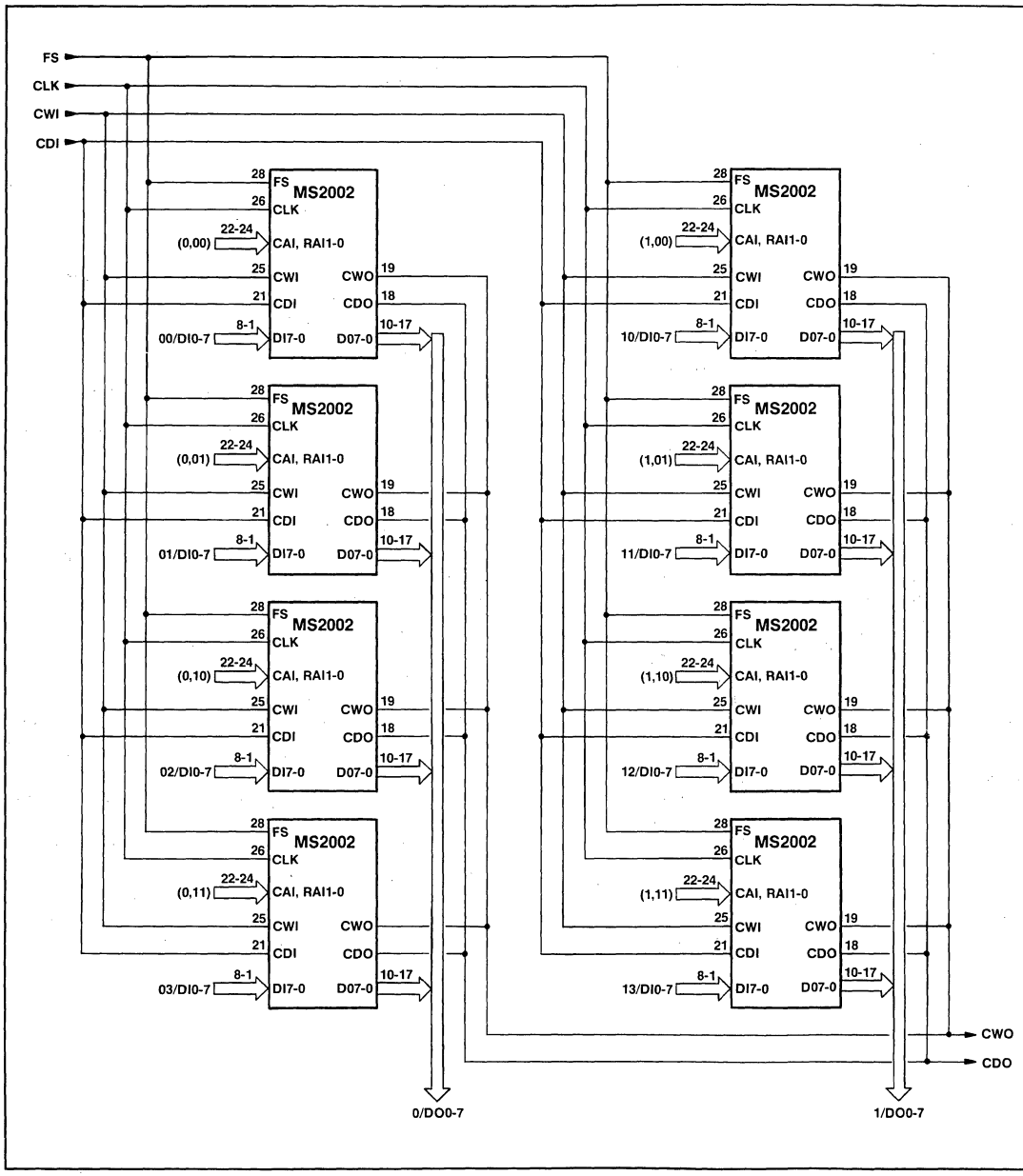


Fig.8 The control array

CAB	$\overline{CPA2}$	$\overline{CPA1}$	$\overline{CPA0}$	R/$\overline{W}$	CWM	RAB1	RAB0
1	2	3	4	5	6	7	8

Bit	Name		Description
1	CAB		**Column Address Bit**
		In	If this bit matches the Column Address pin then the device will be written to or read from. If it does not match then Control Word Out and Control Data Out are high impedance during the output Time Slot.
		Out	This bit is set to the Column Address after a read from the Speech Store or after a write to the Control Store other than all 1's. It goes high impedance in all other cases.
2-4	$\overline{CPA2-0}$		**Control Pin Address 2 to 0**
		In	These bits are the Serial Pin Address at the Control Store (see Fig.6). The Time Slot Address is determined by the Time Slot on the Control Word In pin (see Fig.3). The Serial Pin and Time Slot Addresses define a unique address in the Control Store which corresponds to a Parallel channel if parallel output is used (Fig.6).
		Out	These bits are the same as those on the Time Slot on Control Word In if the Column Addresses match. They are high impedance otherwise.
5	R/$\overline{W}$		**Read or Write**
		In	This bit has no effect unless the Column Addresses match. If they do match then a read or write occurs depending whether it is 1 or 0 6 (see Fig.10).
		Out	This bit is the same as on the Time Slot on Control Word In if the Column Addresses match. It is high impedance otherwise.
6	CWM		**Control Word Mode**
		In	This bit has no effect unless the Column Addresses match. It can replace the Connection Mode bit at the Control Store address during writes or it can help to direct reads if the Column Addresses do match (see Fig.10).
		Out	This bit is the same as the Connection Mode bit at the Control Store address if the Column Addresses match. It is high impedance otherwise.
7-8	RAB1-0		**Row Address Bit 1 and 0**
		In	These bits have no effect unless the Column Addresses match. They help to control writes if the Column Addresses do match (see Fig.10). The Row Address Bits ensure that only one of the four MS2002s in a row of the Control Array can be active on the Data Out pins at any time.
		Out	These bits are set to the Row Address after certain operations and are high impedance otherwise. See Fig.11 for details.

Fig.9 Control word bits (both input and output) **NB** *The Control Word Out bits are open-drain pulldown outputs. This means that output high is the same as output high impedance.*

Writing

The R/$\overline{W}$ bit of the instruction on Control Word In must be low for a write (see Fig.9). This causes a write to all MS2002s in the selected column. This write is to the same address in the Control Store of each MS2002. The Time Slot part of the address is the same as the Time Slot used by the instruction on Control Word In and Control Data In. The Pin part of the address is selected by the Control Pin Address bits in the Control Word (see Figs. 6 and 9).

The MS2002s in the selected column whose Row Address pins do not match the Row Address Bits in the Control Word have 1s written to the 9 bits at the address in the Control Store. This ensures that none of these MS2002s are in conflict with the remaining MS2002 on the Data Out pins. They also go high impedance during the control Time Slot on Control Word Out and Control Data Out (except for the $\overline{CPA2-0}$ and R/$\overline{W}$ bits which are the same for all MS2002s - see Fig.11).

The MS2002 whose Row Address matches responds differently to the instruction. The Control Word Mode bit and the Control Data bits are written into the address in the Control Store. This allows a connection to be established onto the Data Out pins. This MS2002 also responds differently on the control outputs unless the 9 bits written to the Control Store are all 1s. Fig.11 shows how the MS2002 acknowledges the instruction.

Reading

A read is performed automatically to acknowledge a write as mentioned in the previous section. It is also possible to read from the array independently of writing. The column selected by the Column Address Bit of the instruction will be read when the R/$\overline{W}$ bit is high. Reads are associated with an address in the Control Store. Either the bits at that address or the bits in the Speech Store selected by them will be read. This provides information about calls in progress or about the status of a connection.

The Row Address Bits in the instruction are ignored during reads. Each MS2002 which has one or more 0s at the selected address in its Control Store will respond to a read instruction. To avoid possible confusion about which MS2002 in a row is being read the array should be initialised by writing to it.

Two types of read are possible, depending on the input Control Word Mode bit. If this bit is 0 then a Type-0 Read occurs. Type-0 Reads are always from the Control Store. If the Control Word Mode bit is 1 then a Type-1 Read occurs. Type-1 Reads are from the Control Store or from the Speech Store depending on whether the Connection Mode bit at the Control Store address is 1 or 0 (free or busy). Fig.11 shows how the reads affect the control outputs.

Type-0 Reads indicate whether or not the connection through the array to the Data Out pins is busy or free. If it is busy then it identifies the MS2002 and Speech Store Address in it which sources the connection.

Type-1 Reads tap a connection to the Data Out pins if it is busy. They also indicate the MS2002 which sources the connection but cannot specify the origin within the MS2002. If there is no busy connection assocaited with the Control Store address the a Type-1 Read indicates the presence of 0s at the Control Store address.

$\overline{SPA2}$	$\overline{SPA1}$	$\overline{SPA0}$	$\overline{STSA4}$	$\overline{STSA3}$	$\overline{STSA2}$	$\overline{STSA1}$	$\overline{STSA0}$
1	2	3	4	5	6	7	8

Bit	Name	Description	
1-3	$\overline{SPA2-0}$	**Speech Pin Address 2 to 0**	
		In	These bits replace the Speech Pin Address bits at the Control Store address during a write if the Row Addresses match (see Fig.10). **NB** These bits are inverted with respect to those at the Control Store address, i.e. if these are all 0 then they refer to Speech Pin Address 7 (see Fig.6).
		Out	These bits are high impedance unless a read or write occurs. During a read these bits can contain the Speech Pin Address bits at the Control Store address or bits 1 to 3 of the Speech Store location addressed by the bits at the Control Store address (see Fig.11). **NB** These bits are inverted with respect to the contents of the Control Store but not with respect to the contents of the Speech Store.
4-8	$\overline{STSA4-0}$	**Speech Time Slot Address 4 to 0**	
		In	These bits replace the Speech Time Slot Address bits at the Control Store address during a write if the Row Addresses match (see Fig.11). **NB** These bits are inverted with respect to those at the Control Store address, i.e. if these are all 0 then they refer to Speech Time Slot Address 31 (see Fig.6).
		Out	These bits are high impedance unless a read or write occurs. During a read these bits can contain the Speech Time Slot Address bits at the Control Store address or bits 4 to 8 of the Speech Store location addressed by the bits at the Control Store address (see Fig.11). **NB** These bits are inverted with respect to the contents of the Control Store but not with respect to the contents of the Speech Store.

Fig.10 Control data bits (both input and output) **NB** *The Control Data Out bits are open-drain pulldown outputs. This means that output high is the same as output high impedance.*

Control Word In			CM Bit at Control Store Address	Instruction	Control Word Out			Control Data Out
R/W Bit	CWM Bit	Row Address			CAB Bit	CWM Bit	RAB1-0 Bits	
0	X	Matches	X	Write CWM bit + CDI bits	CAP Pin *†	Control Store Bit 9 (CM)†	RAP1-0 Pins *†	Control Store Bits 1-8†
0	X	Does Not Match	X	Write all 1s	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	X	Read Type 0	CAP Pin *†	Control Store Bit 9 (CM)	RAP1-0 Pins *	Control Store Bits 1-8
1	1	X	1	Read Type 1	High Impedance	Control Store Bit 9 (CM) = 1	High Impedance	Control Store Bits 1-8
1	1	X	0		CAP Pin†	Control Store Bit 9 (CM) = 0	RAP1-0 Pins	Speech Store Bits 1-8

Fig.11 The control operations

NB It is assumed that the Column Address matches, in which case $\overline{CPA2\text{-}0}$ and $R/\overline{W}$ are the same as on the control Time Slot on Control Word In. The control outputs are high impedance during the control Time Slot if the Column Address does not match.
* High Impedance if data at Control Store Address is all 1's.
† Should be identical to the data on the control inputs.

ELECTRICAL CHARACTERISTICS

Test Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage	V_{DD}	4.75	5.0	5.25	V
Ambient temperature	T_{amb}	0		70	°C
Input low voltage	V_{IL}	0	0.4	0.8	V
Input high voltage	V_{IH}	2.0	2.4	V_{CC}	V
Output pullup resistor	R_{OP}	1000			Ω
Output load capacitor	C_{OP}	50			pF
Bias decoupling capacitor	C_{BB}	900	1000	1100	pF

Digital Static Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Supply current	I_{DD}		40	60	mA	Unloaded
Input leakage current	I_{LI}			50	μA	$0 < V < V_{CC}$
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 2mA
Output low voltage	V_{OL}	0		2.0	V	I_{OL} (Sink) = 8mA
Output leakage current	I_{LO}			50	μA	$0 < V < V_{CC}$

Analog Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Pin capacitance	C_P		8	10	nF	Unloaded

Digital Switching Characteristics - Clock (see Fig.12)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Clock period	t_{CP}	225	244	275	ns	
Clock rise time	t_{CR}		50		ns	
Clock high period	t_{CH}	82			ns	
Clock fall time	t_{CF}		50		ns	
Clock low period	t_{CL}	82			ns	

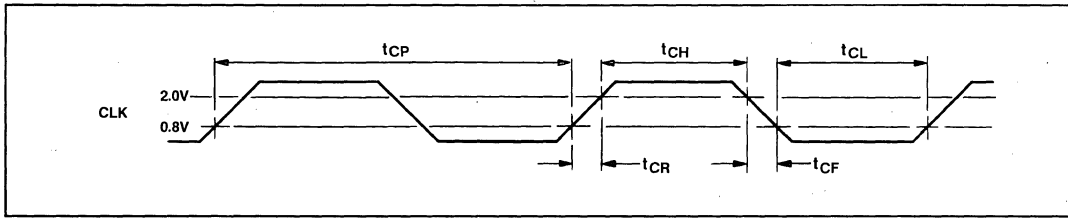


Fig.12 Timing - clock

Digital Switching Characteristics - Frame Synchronisation (see Figs.5 and 13)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Frame Synchronisation falling hold time	t_{FFH}	90	122		ns	
Frame synchronisation falling setup time	t_{FFS}	60	122		ns	
Frame synchronsiation rising hold time	t_{FRH}	90	122		ns	
Frame synchronisation rising setup time	t_{FFS}	60	122		ns	

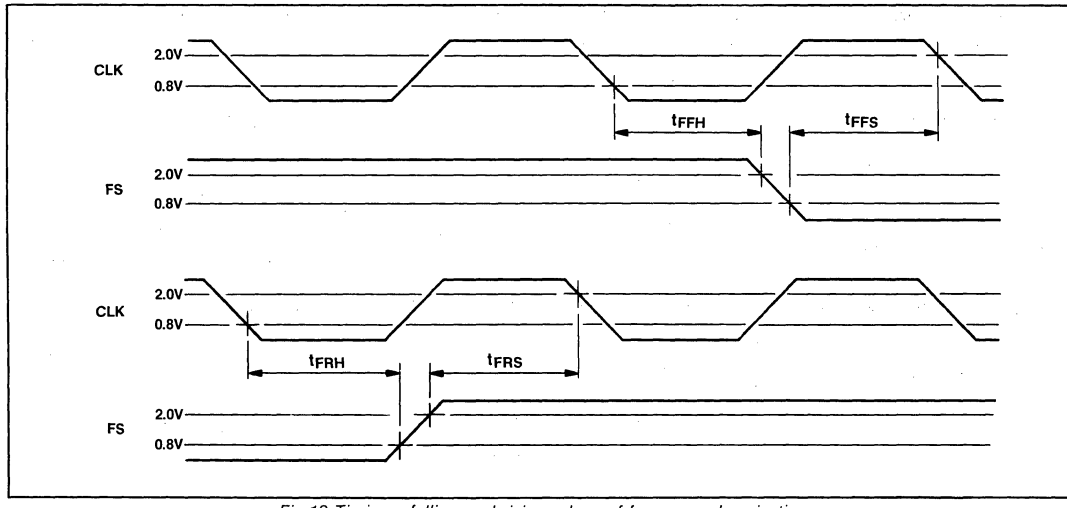


Fig.13 Timing - falling and rising edges of frame synchronisation

Digital Switching Characteristics - Data and Control Inputs and Outputs (see Figs.5 and 14)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Input setup time	t_{IS}	60	244		ns	
Input hold time	t_{IH}	90	244		ns	
Output hold time	t_{OH}	5			ns	
Output delay	t_{OD}			150	ns	

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

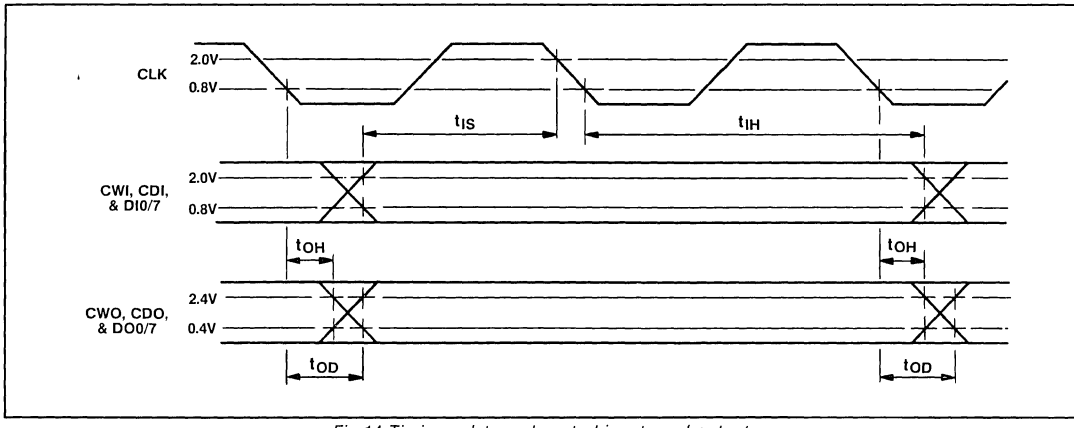


Fig.14 Timing - data and control inputs and outputs

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage, V_{DD}	-0.5V to +7V
Storage tempertaure, T_{ST}	-65°C to +150°C
Digital input voltage, V_{ID}	-0.3V to V_{DD} +0.3V
Clamp current (Sink or Source), I_C	50mA
Package power dissipation, P_P	800mW

2MBIT PCM SIGNALLING CIRCUIT

MV1441

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

The 2.048MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single 5 volt supply with relevant inputs and outputs TTL compatible.

The MV1441 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol.III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. A clock recovery circuit is provided using a 16.384MHz crystal (12.352MHz for 1.544MHz operation), which may be shared between several separate devices.

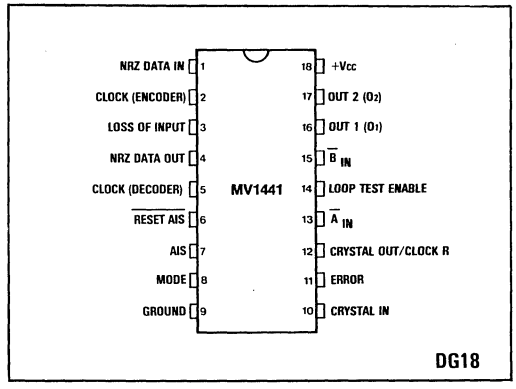


Fig.1 Pin connections - top view

FEATURES

- On-Chip Digital Clock Regenerator
- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal allows Off-Chip Clock Regeneration
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decode Data in NRZ Form
- Low Power Operation
- 2.048MHz or 1.544MHz Operation

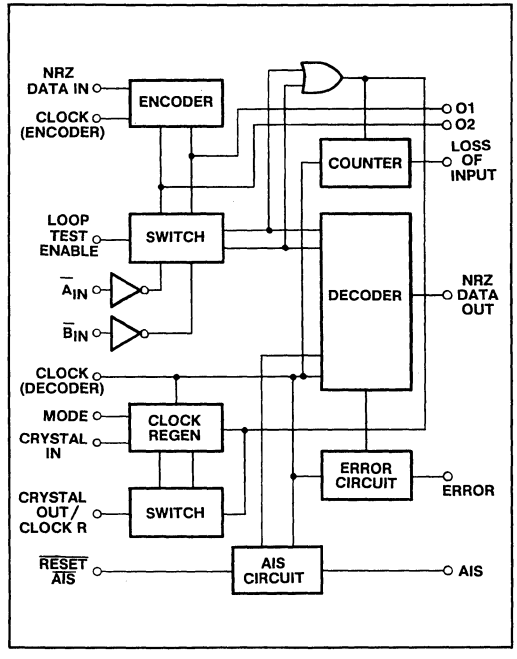


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc +0.5V Gnd -0.3V
Outputs	Vcc, Gnd -0.3V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	I_{sink} = 2.0mA
High level output voltage	V_{OH}		2.8			V	I_{source} = 2mA) both
			V_{CC}-0.75			V	I_{source} = 1mA) apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Max. Clock (Encoder) frequency	f_{maxenc}	4.0	10		MHz	Figs.10,15
Max. Clock (Decoder) frequency	f_{maxdec}	2.2	5		MHz	Figs.11,15
Propagation Delay Clock (Encoder) to O_1, O_2	$t_{pd1A/B}$			100	ns	Figs.8,10,15 See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10,15
t_{pd1A} - t_{pd1B} difference				20	ns	Figs.10,15
Propagation Delay Clock (Encoder) to Clock Regenerate	t_{pd3}			150	ns	Loop test enable = '1', Figs.10,15
Setup time of NRZ data in to Clock (Encoder)	t_{s3}	75			ns	Figs.7,10,15
Hold time of NRZ data in	t_{h3}	55			ns	Figs.7,10,15
Propagation delay $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock Regenerate	t_{pd2}			150	ns	Loop test enable = '0' Figs.13,15
Propagation delay Clock (Decoder) to error	t_{pd4}			200	ns	Figs.12,15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	t_{pd5}			200	ns	Loop test enable = '0', Figs.14,15
Propagation delay Clock (Decoder) to NRZ data out	t_{pd6}			150	ns	Figs.7,11,15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock (Decoder)	t_{s1}	75			ns	Figs.7,11,15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock (Decoder)	t_{h1}	5			ns	Figs.7,11,15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	t_{h2}	30			ns	Figs.7,14,15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	t_{s2}	100			ns	Figs.7,14,15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	t_{s2}	0			ns	Figs.14,15
Propagation Delay Clock (Decoder) to LIP				150	ns	

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 3.5 clock periods from NRZ Data In (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs ($\overline{A}_{IN}$, $\overline{B}_{IN}$) (Fig.4).

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. LIP
Loss of input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input ($\overline{A}_{IN}$ or $\overline{B}_{IN}$ = '0') resets this count.

4. NRZ data out
Decoded binary data from pseudo-ternary inputs $\overline{A}_{IN}$, $\overline{B}_{IN}$

5. Clock (Decoder)
Clock for decoding data on $\overline{A}_{IN}$ and $\overline{B}_{IN}$, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot Zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Mode
Mode at logic '1' selects internal crystal controlled clock regeneration and Mode at logic '0' selects external clock regeneration using, for example, a tuned circuit.

9. Ground
Zero volts.

10. Crystal In
Input to amplifier forming crystal oscillator when crystal is connected between pins 10 and 12. This pin may also be used as a 16.384MHz clock input if one oscillator is to be shared over several HDB3 encoders/decoders.

11. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

12. Clock R/Crystal Out
If pin 8 is at '0' pin 12 is Clock Regenerate, giving OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 14 = '0', OR function of O_1, O_2 when pin 14 = '1'. If pin 8 is at '1' then pin 12 becomes Crystal Out and forms oscillator with pin 10.

13,15. $\overline{A}_{IN}$, $\overline{B}_{IN}$
Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

14. Loop test enable
TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 7½ clock periods in loop back.

16,17. O_1, O_2
Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

18. +Vcc
Positive 5V ± 10% supply.

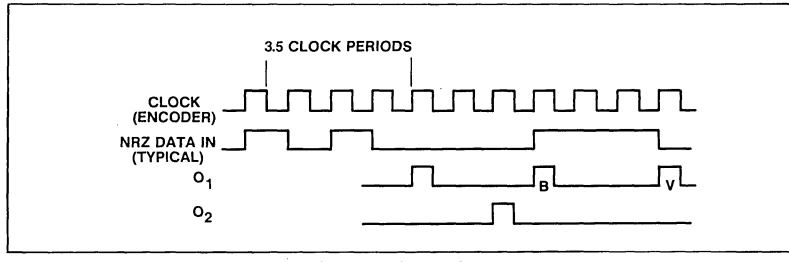


Fig.3 Encode waveforms

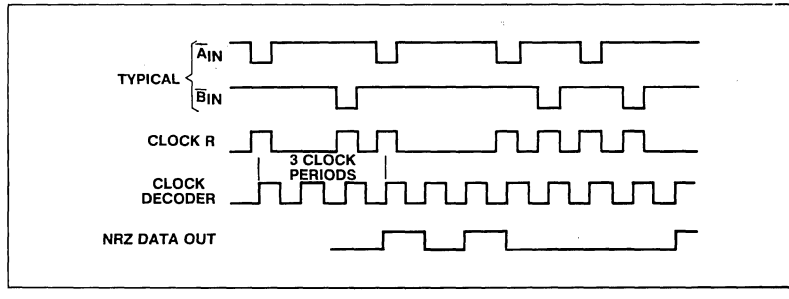


Fig.4 Decode waveforms

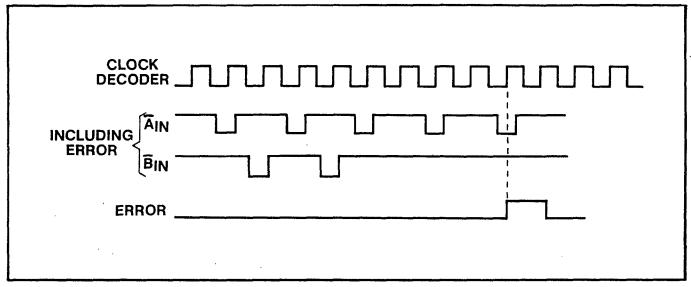


Fig.5 HDB3 error output waveforms

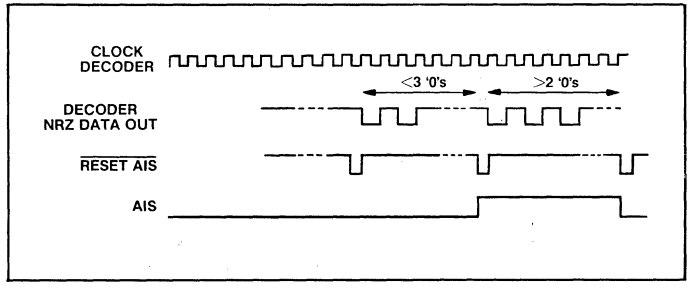


Fig.6 AIS error and Reset waveforms

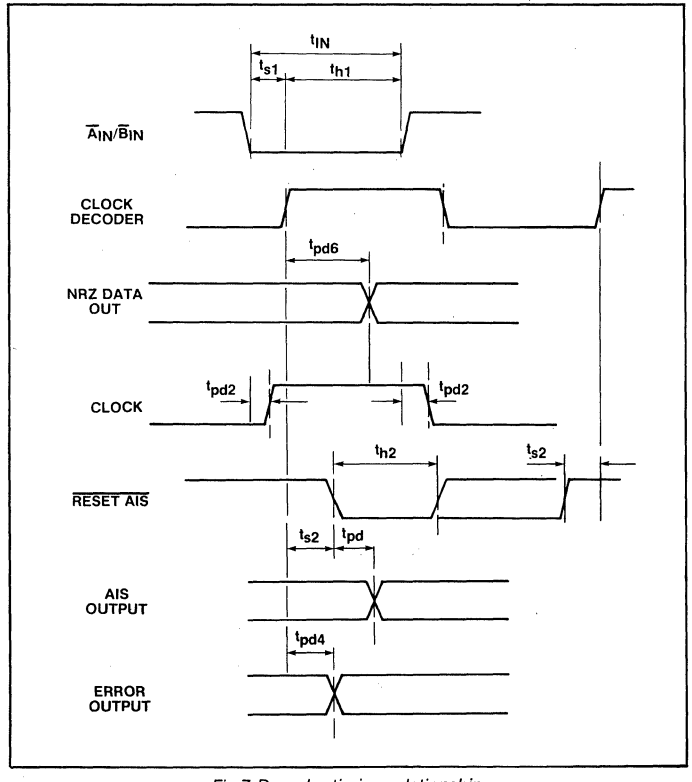


Fig.7 Decoder timing relationship

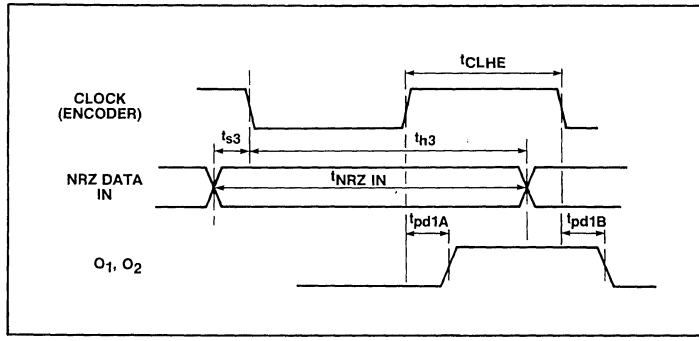


Fig.8 Encoder timing relationship

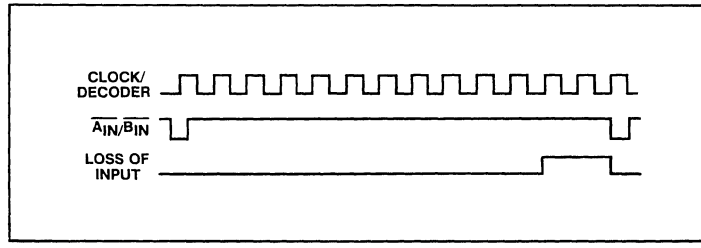


Fig.9 Loss of input waveforms

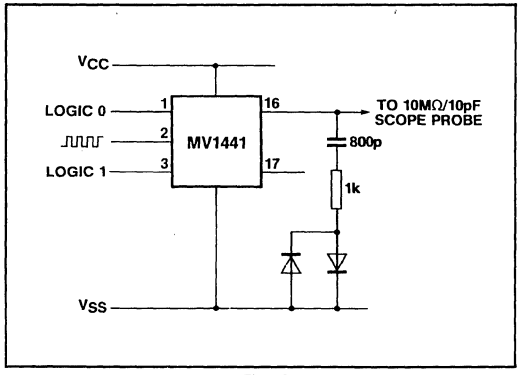


Fig.10

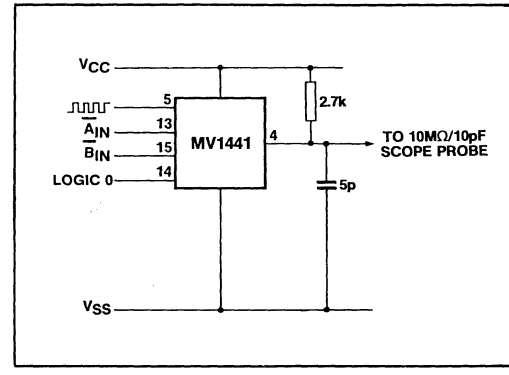


Fig.11

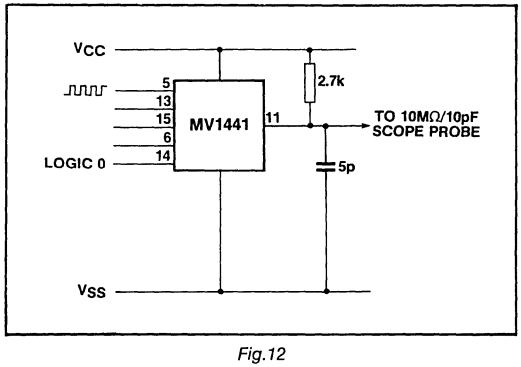


Fig.12

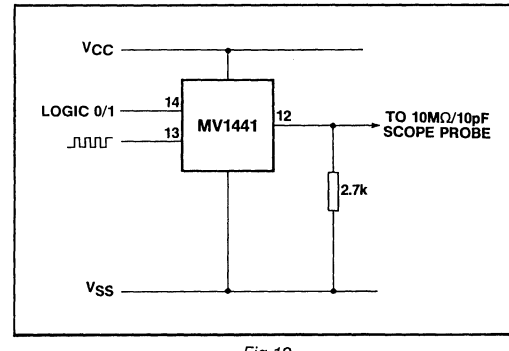


Fig.13

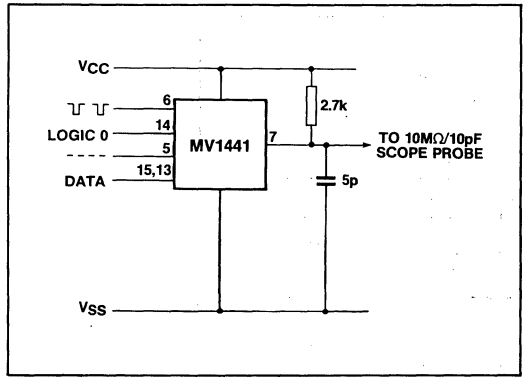


Fig.14

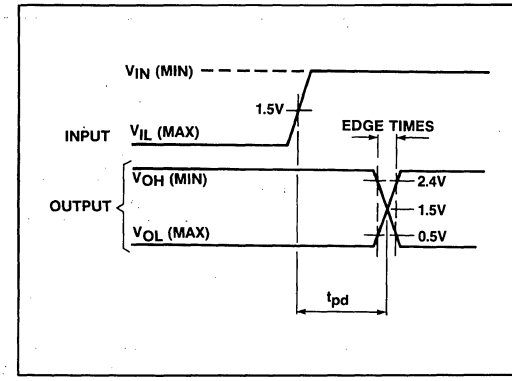


Fig.15 Test timing definitions

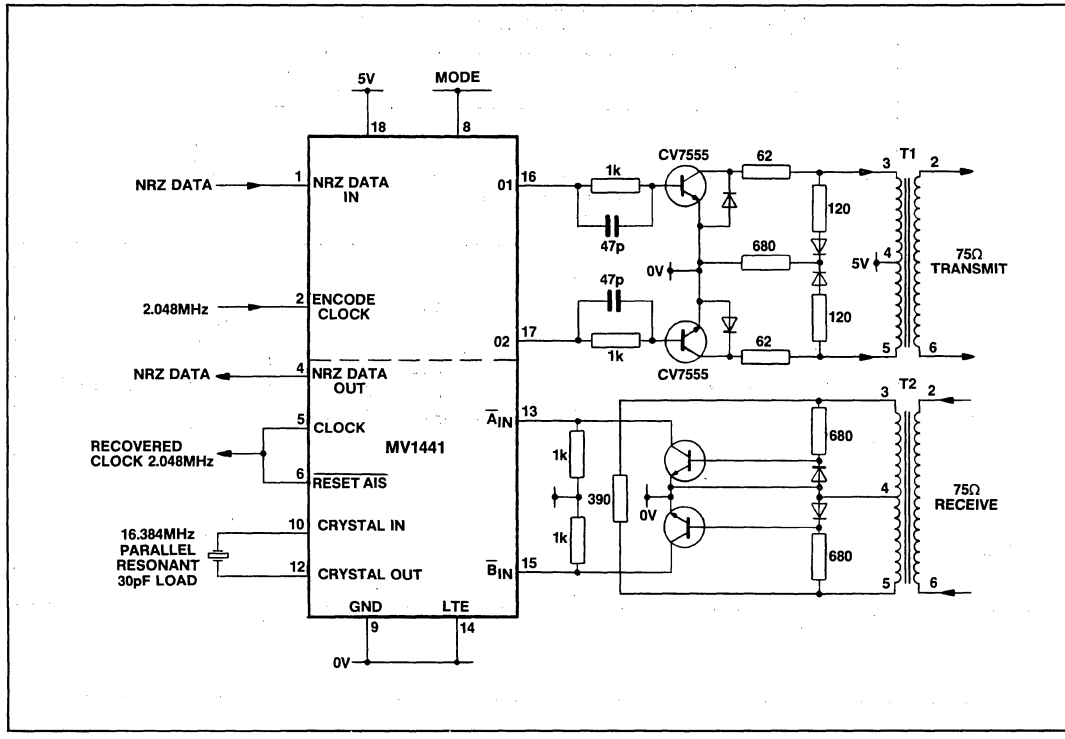


Fig.16 A typical application of the MV1441 with the interfacing to the transmission lines included

PLESSEY
Semiconductors

8.5MBIT PCM SIGNALLING CIRCUIT

MV1448

HDB3 ENCODER/DECODER

This 8.544MBit PCM Signalling Circuit will perform the signalling and error detection functions for a 8.544MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuit is fabricated in CMOS and operates from a single 5V supply with TTL compatible inputs and outputs.

The MV1448 is an encoder/deocder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol. III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing.

FEATURES

- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal Allows Clock Regeneration from Incoming HDB3 Data
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decoded Data in NRZ Form
- Low Power Operation
- 2.048MHz or 8.544MHz Operation

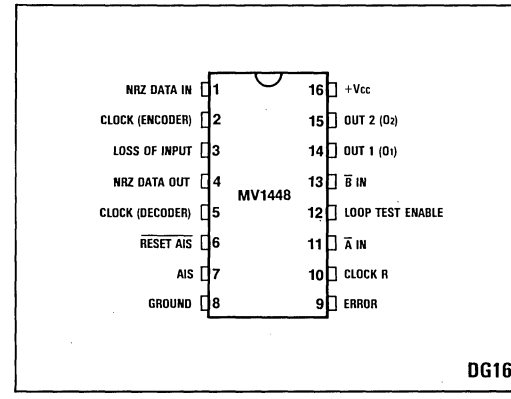


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc+0.5V to GND -0.3V
Outputs	Vcc to GND -0.3V

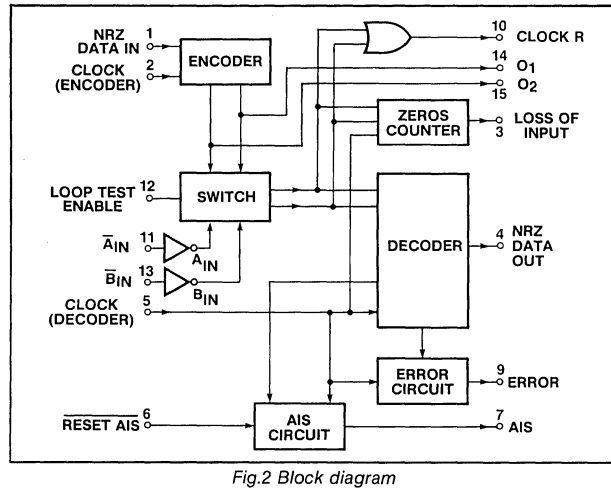


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	Isink = 2.0mA
High level output voltage	V_{OH}		2.8			V	Isource = 2mA } both
			V_{CC}-0.75			V	Isource = 1mA } apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock (encoder) frequency	$Fmax_{enc}$	10			MHz	Figs. 10, 15
Max. clock (decoder) frequency	$Fmax_{dec}$	10			MHz	Figs. 11, 15
Propagation delay clock encoder to O_1, O_2	tpd1A/B		50		ns	Figs. 8, 10, 15 See Note 1
Rise and fall times O_1, O_2				20	ns	Figs. 10, 15
tpd1A - tpd1B difference				20	ns	Figs. 10, 15
Propagation delay clock to clock regenerate (clock R)	tpd3		50		ns	Loop test enable = '1', Figs. 10, 15
Setup time of NRZ data in to clock (encoder)	ts3		40		ns	Figs. 7, 10, 15
Hold time of NRZ data in	th3		40		ns	Figs. 7, 10, 15
Propagation delay A_{IN}, B_{IN} to clock regenerate	tpd2 low-high			76	ns	Loop test enable = '0',
	high-low			50		Figs. 13, 15
Propagation delay clock (decoder) to error	tpd4			50	ns	Figs. 12, 15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	tpd5		50	44	ns	Loop test enable = '0', Figs. 14, 15
Propagation delay clock (decoder) to NRZ data out	tpd6			50	ns	Figs. 7, 11, 15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	ts1	15	40		ns	Figs. 7, 11, 15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	th1	4	5		ns	Figs. 7, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	9			ns	Figs. 7, 14, 15
Setup time clock (decoder) to $\overline{\text{Reset AIS}}$	ts2		50		ns	Figs. 7, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = '1' to clock (decoder)	ts2	31			ns	Figs. 14, 15
Propagation delay clock (decoder) to LIP			50	87	ns	

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. LIP
Loss if input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input (A_{IN} or B_{IN} = '0') resets this count.

4. NRZ data out
Decoded binary data from pseudo-ternary inputs A_{IN} and B_{IN}.

5. Clock (Decoder)
Clock for decoding data on A_{IN} and B_{IN}, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on Reset AIS resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding Reset AIS = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

10. Clock R
OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 12 = '0', OR function of O_1, O_2 when pin 12 = '1'.

11,13. $\overline{A}_{IN}$, $\overline{B}_{IN}$
Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

12. Loop test enable
TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 6¾ clock periods in loop back.

14,15. O_1, O_2
Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero from and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

16. +Vcc
Positive 5V ± 10% supply.

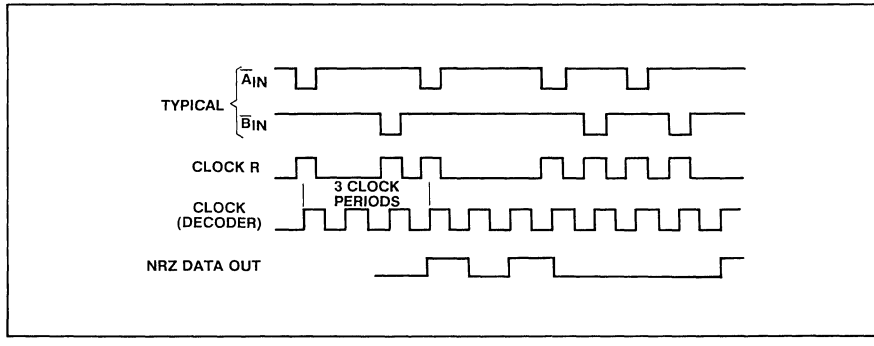


Fig. 3 Decode waveforms

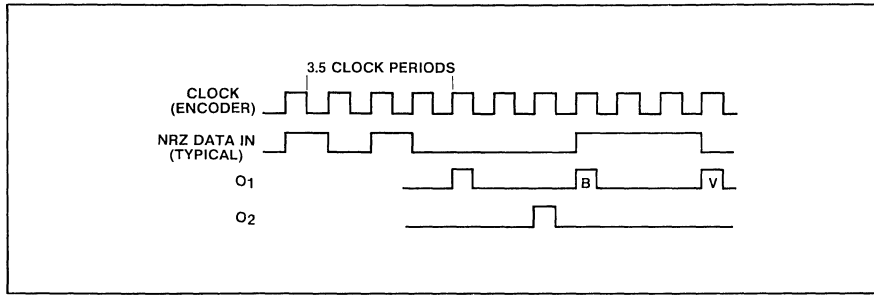


Fig.4 Encode waveforms

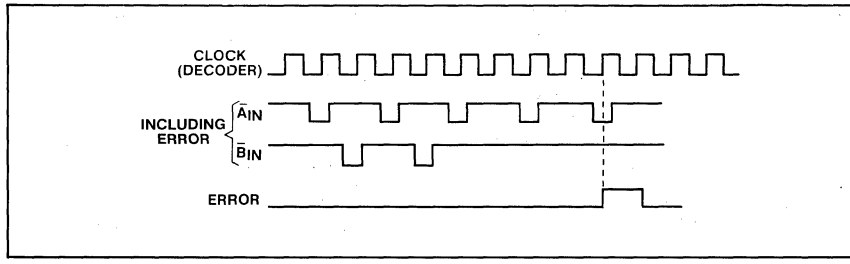


Fig.5 HDB3 error output waveforms

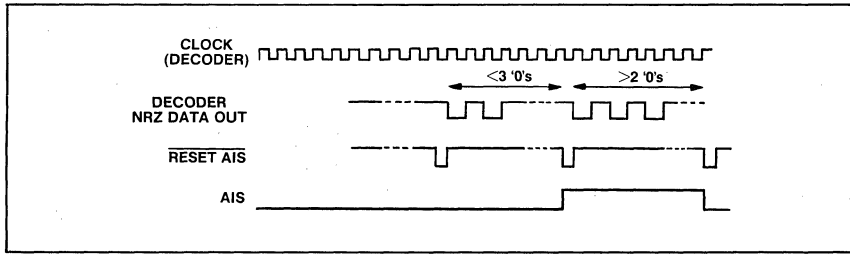


Fig.6 AIS error and Reset waveforms

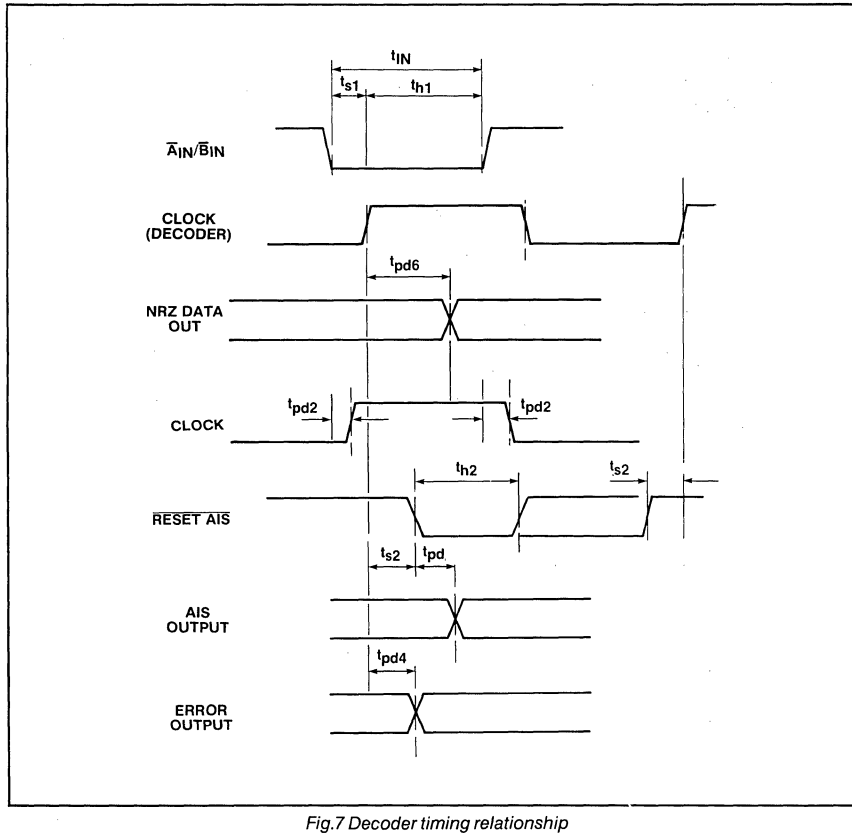


Fig.7 Decoder timing relationship

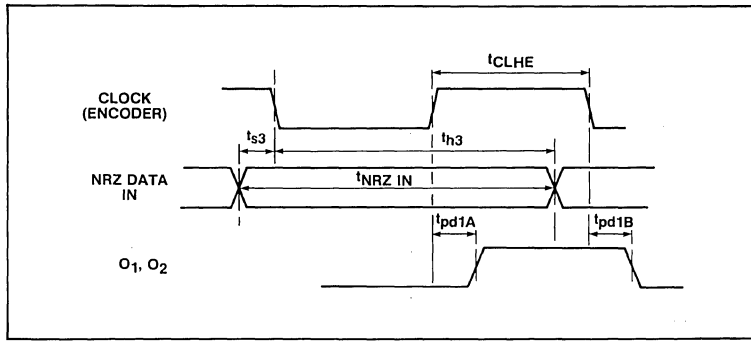


Fig.8 Encoder timing relationship

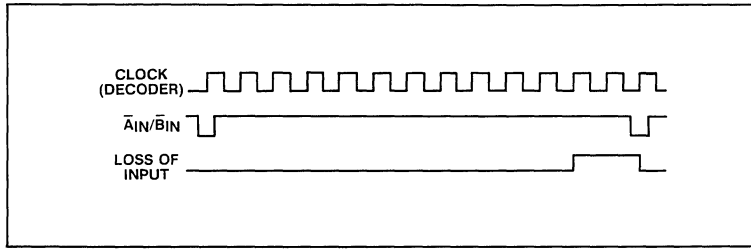


Fig.9 Loss of input waveforms

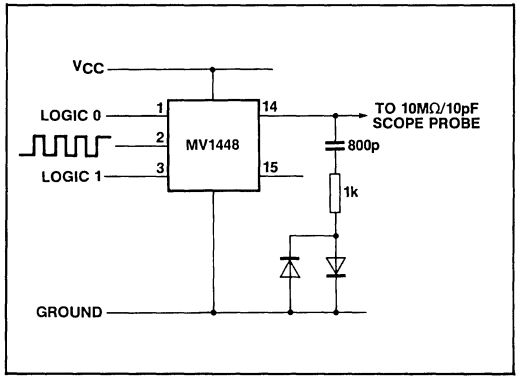


Fig.10

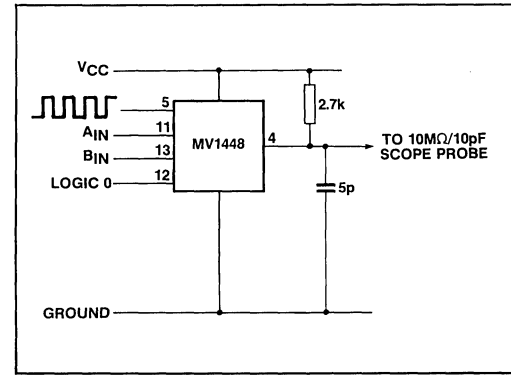


Fig.11

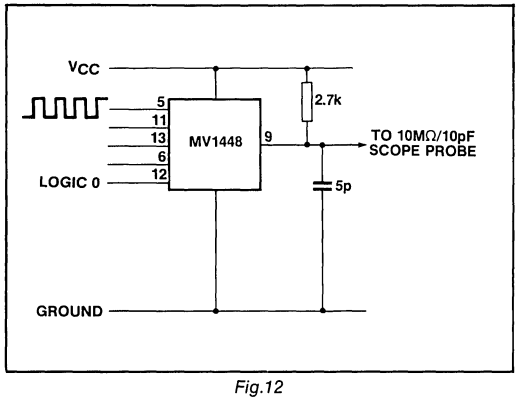


Fig.12

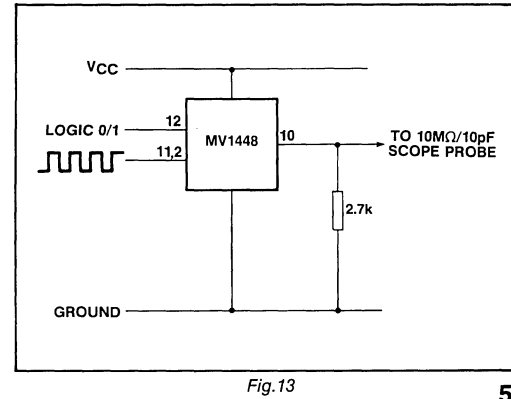


Fig.13

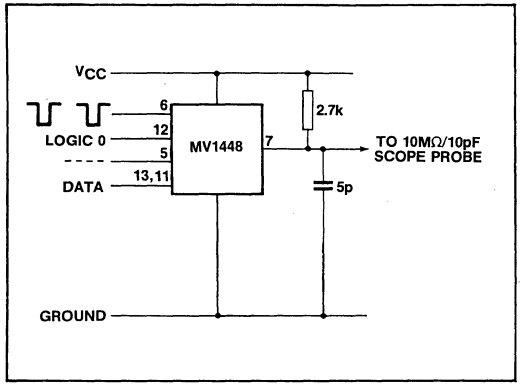


Fig.14

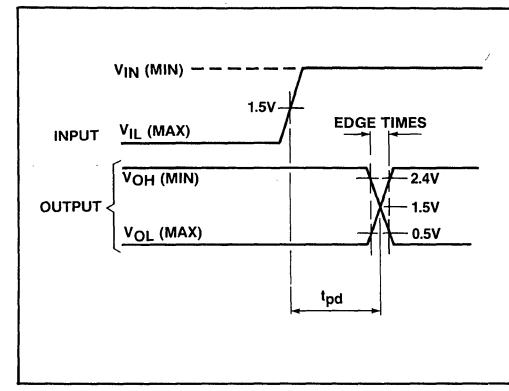


Fig.15 Test timing definitions

MV3000A/B

SUBSCRIBER LINE AUDIO CIRCUIT

The MV3000 is a Subscriber Line Audio Circuit (SLAC) for use in subscriber line cards in telephone exchanges or similar equipment.

It performs A/D and D/A conversion, adjusts the gain and frequency response for both the transmit and receive paths and performs 2 to 4 wire balancing by automatically cancelling the component of the receive signal in the transmit path. The device also allows the telephone line to be easily controlled and monitored.

High performance is ensured through the use of DSP techniques implemented in CMOS technology.

FEATURES

- Adaptive Balancing.
- Programmable Filters and Gain Control.
- Selectable for μ-Law, A-Law or Linear Codes.
- Programmable Line Control Interface.
- Programmable Time & Clock Slot Assignments.
- Power Down Mode.
- On-chip Reference Voltage.
- Meets CCITT and AT&T Specifications.

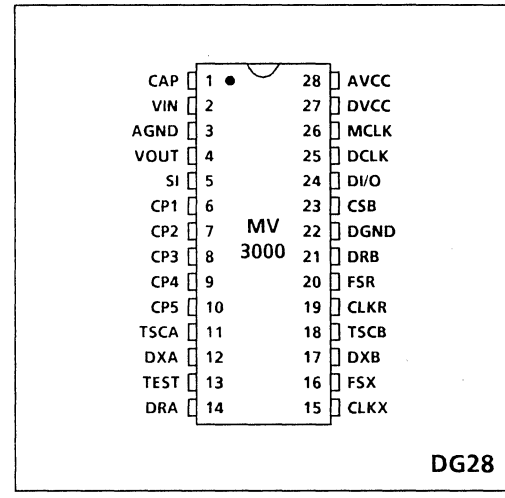


Fig. 1 Pin Connection - top view

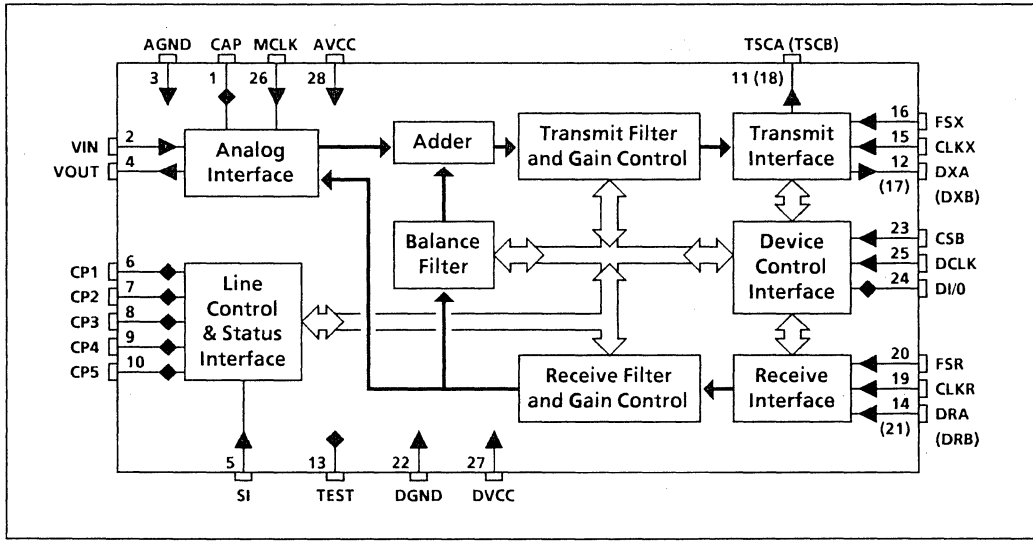


Fig. 2 Functional block diagram

FUNCTIONAL DESCRIPTION

The MV3000 performs the coding, decoding, filtering, 2 to 4 balancing and line supervision functions which are required for the subscriber line interface in a digital PABX or Central Office. It can be easily interfaced with the SL376 Subscriber Line Interface Circuit to provide a complete subscriber line circuit.

The received digital PCM signal is filtered, converted to analog and output. The analog input is filtered, digitised and processed to cancel any of the analog output signal.

The device and the line are controlled and monitored using the serial device control interface.

Receive Path

PCM encoded signals are received on either the DRA pin or the DRB pin, depending on programming. Bit and frame synchronisation are established by the CLKR clock and FSR pulse as shown in Fig. 3. The negative edge of the CLKR clock which is used to strobe bit 1 of the PCM signal is determined by the programmed receive segment and slot address. The PCM signal can be μ-Law or A-Law encoded or it can be linear (16 bits). The rate of the serial stream which is sampled on DRA or DRB can vary from 64 kbit/s up to 4096 kbit/s, giving up to 64 8-bit or 32 16-bit time slots.

The PCM signal is received at an 8 kHz sample rate. This is interpolated to give a signal with a 16 kHz sample rate for input to the receive filter. There are 4 taps on the FIR (finite impulse response) receive filter for compensation of distortions produced by analog components at the analog interface. The gain control allows a usable attenuation of up to 18 dB to be selected.

The modified receive signal is fed to both the balance filter, to allow for 2 to 4 wire balancing, and to the analog interface, where it is converted to an analog signal. A low-pass real-time filter is used to remove out-of-band noise and signal components.

Transmit Path

The analog transmit signal is presented to the MV3000 at VIN. At the analog interface the signal goes through a low-pass anti-aliasing filter which rejects high frequency noise. The analog interface digitises the filtered receive signal and outputs the digital equivalent.

The digital signal from the analog interface is passed to the adder which subtracts away the receive signal after it has been modified by the balance (B) filter. The B-filter is a 10 tap FIR (finite impulse response) filter operating at a sample rate of 16 kHz. The coefficients for this filter are programmed into it and can be automatically updated from the residual signal output by the adder.

The transmit filter is a 4 tap FIR filter operating at a sample rate of 16 kHz. It allows for compensations of distortions introduced by analog components at the analog interface. The transmit gain control allows a usable gain of up to 15 dB to be selected.

The sample rate is reduced to 8 kHz at the transmit interface and the signal is encoded to μ-Law or A-Law (8 bits) or remains linear (16 bits)

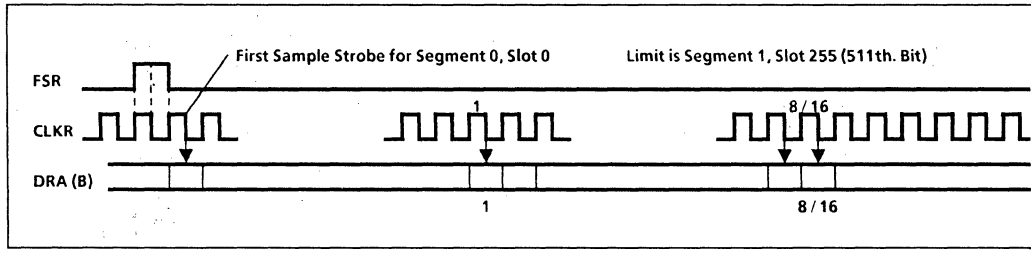


Fig. 3 Receive timing diagram

according to programming. The PCM signal is clocked out on the DXA or DXB pin by the CLKX clock. Frame synchronisation is established by the pulse on FSX (see Fig. 4). The delay between the pulse on FSX and the first bit of data clocked out is determined by the programmed transmit segment address and slot address. The serial output stream can vary from 64 kbit/s up to 4096 kbit/s giving from 1 8-bit time slot up to 64 8-bit or 32 16-bit time slots. The TSCA or TSCB pin will be pulled low when data is output. The DXA and DXB pins go into the high impedance state when they are not active.

Encoding and Decoding

The analog input signal should be in the range +/- 3 Volts with respect to analog ground. An input signal in this range is encoded according to the A-law, u-Law or linear algorithms. The corresponding PCM code is decoded to give an analog output signal in the range +/- 1.5 Volts with respect to V_{OO} (nominally 2.5 Volts). This means that the analog output is one half of the amplitude of the analog input and has a net DC offset from ground. There are different reference milliwatt signals (0 dBm0 levels) for input and output due to the difference in amplitude.

A-Law and μ-Law codes (8 Bit)

These are non-linear codes in which the signal is described in terms of a sign bit plus segment and chord bits which denote the magnitude. There are 7 segments for A-Law and 8 for μ-Law. The size of the segments increase in approximately exponential steps.

Each segment is divided up linearly into chords (except the zero level in μ-Law). This means that the resolution is finer at smaller input voltages than at larger, and so gives a better match to the human ear. Fig. 5 shows how the A-Law code operates and Fig. 6 shows the μ-Law code.

In both codes positive values are represented by a sign bit of 1. The A-Law data is alternate digit inverted (ADI) and the μ-Law magnitude data is in effect inverted. These techniques are used to ensure that ones are transmitted for good clock recovery on digital trunk lines when the channel is quiet.

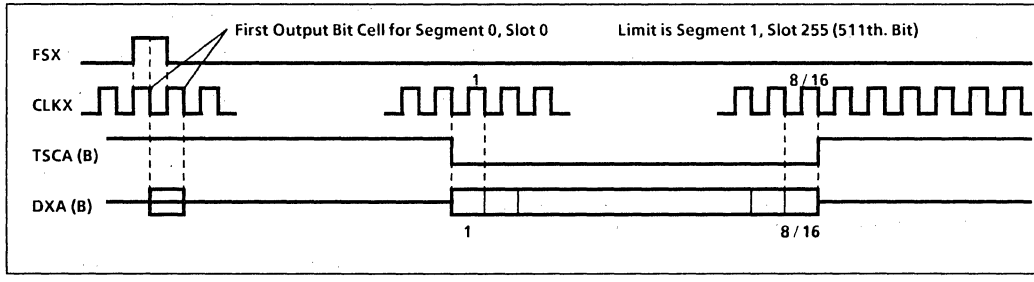


Fig. 4 Transmit timing diagram

Input Voltage [x (4096/3)]	Segment	Chord Steps Number x Size	Data Character		Output Voltage - V_{OO} [x (4096/1.5)]
			Without ADI	With ADI	
(+ /-) 0 to 2	1	32x2	(1/0) 000 0000	(1/0) 101 0101	(+ /-) 1
(+ /-) 2 to 4			(1/0) 000 0001	(1/0) 101 0100	(+ /-) 3
(+ /-) 62 to 64			(1/0) 001 1111	(1/0) 100 1010	(+ /-) 63
(+ /-) 64 to 68	2	16x4	(1/0) 010 0000	(1/0) 111 0101	(+ /-) 66
(+ /-) 68 to 72			(1/0) 010 0001	(1/0) 111 0100	(+ /-) 70
(+ /-) 124 to 128			(1/0) 010 1111	(1/0) 111 1010	(+ /-) 126
(+ /-) 128 to 136	3	16x8	(1/0) 011 0000	(1/0) 110 0101	(+ /-) 132
(+ /-) 136 to 144			(1/0) 011 0001	(1/0) 110 0100	(+ /-) 140
(+ /-) 248 to 256			(1/0) 011 1111	(1/0) 110 1010	(+ /-) 252
(+ /-) 256 to 272	4	16x16	(1/0) 100 0000	(1/0) 001 0101	(+ /-) 264
(+ /-) 272 to 288			(1/0) 100 0001	(1/0) 001 0100	(+ /-) 280
(+ /-) 496 to 512			(1/0) 100 1111	(1/0) 001 1010	(+ /-) 504
(+ /-) 512 to 544	5	16x32	(1/0) 101 0000	(1/0) 000 0101	(+ /-) 528
(+ /-) 544 to 576			(1/0) 101 0001	(1/0) 000 0100	(+ /-) 560
(+ /-) 992 to 1024			(1/0) 101 1111	(1/0) 000 1010	(+ /-) 1008
(+ /-) 1024 to 1088	6	16x64	(1/0) 110 0000	(1/0) 011 0101	(+ /-) 1056
(+ /-) 1088 to 1152			(1/0) 110 0001	(1/0) 011 0100	(+ /-) 1120
(+ /-) 1984 to 2048			(1/0) 110 1111	(1/0) 011 1010	(+ /-) 2016
(+ /-) 2048 to 2176	7	16x128	(1/0) 111 0000	(1/0) 010 0101	(+ /-) 2112
(+ /-) 2176 to 2304			(1/0) 111 0001	(1/0) 010 0100	(+ /-) 2240
(+ /-) 3968 to 4096			(1/0) 111 1111	(1/0) 010 1010	(+ /-) 4032

Fig. 5 A-Law

Input Voltage [x (8192/3)]	Segment	Chord Steps Number x Size	Data Character	Output Voltage - V_{OO} [x (8192/1.5)]
(+ /-) 0 to 1	1	1x1	(1/0) 111 1111	(+ /-) 0
(+ /-) 1 to 3		15x2	(1/0) 111 1110	(+ /-) 2
(+ /-) 3 to 5			(1/0) 111 1101	(+ /-) 4
(+ /-) 29 to 31			(1/0) 111 0000	(+ /-) 30
(+ /-) 31 to 35	2	16x4	(1/0) 110 1111	(+ /-) 33
(+ /-) 91 to 95			(1/0) 110 0000	(+ /-) 93
(+ /-) 95 to 103	3	16x8	(1/0) 101 1111	(+ /-) 99
(+ /-) 215 to 223			(1/0) 101 0000	(+ /-) 219
(+ /-) 223 to 239	4	16x16	(1/0) 100 1111	(+ /-) 231
(+ /-) 463 to 479			(1/0) 100 0000	(+ /-) 471
(+ /-) 479 to 511	5	16x32	(1/0) 011 1111	(+ /-) 495
(+ /-) 959 to 991			(1/0) 011 0000	(+ /-) 975
(+ /-) 991 to1055	6	16x64	(1/0) 010 1111	(+ /-) 1023
(+ /-) 1951 to 2015			(1/0) 010 0000	(+ /-) 1983
(+ /-) 2015 to 2143	7	16x128	(1/0) 001 1111	(+ /-) 2076
(+ /-) 3935 to 4063			(1/0) 001 0000	(+ /-) 3999
(+ /-) 4063 to 4319	8	16x256	(1/0) 000 1111	(+ /-) 4191
(+ /-) 7903 to 8159			(1/0) 000 0000	(+ /-) 8031

Fig. 6 μ-Law

Linear code (16 bit)

The device may be programmed for linear operation to simplify the design of telephone conference circuits or if additional signal processing is desired. A 2s complement scheme is used with positive values represented by the sign bit equal to 0 (the opposite of the non-linear codes). The resolution is slightly less than the theoretical limit for 16 bits (see Fig. 7).

Signal levels and the digital milliwatt

Signal levels for A-law and μ-Law codes are defined with respect to a milliwatt reference level in units of dBm0. This means that a signal of 0 dBm0 is a reference milliwatt signal i.e. it is at the local reference level. It does not mean that the signal will dissipate 1mW into a 600Ω resistor (i.e. is 2.191 $V_{P/P}$) unless the local reference level, 0 dBm0, also corresponds to 0 in units of dBm(600Ω).

The specifications for A-Law and μ-Law codes (CCITT Specification G.711) define that the uppermost coding decision levels for A-Law (4096) and μ-Law (8159) correspond to 3.14 dBm0 and 3.17 dBm0 respectively. This means that the 0 dBm0 level is about 5.6 dBm(600Ω) at the analog input and about -0.4 dBm(600Ω) at the analog output.

The digital milliwatt signal provides an example of this in practice. The digital milliwatt is a defined sequence of 8 codes which, if there was no loss on the receive path, would produce a 0 dBm0 signal on the analog output. The codes for the digital milliwatt for the three cases are given in Fig. 8. The actual voltages involved can be determined from Figs. 5, 6 and 7.

Input Voltage [x (32,768 / 3)]	Data Character	Output Voltage - V_{OO} [x (32,768 / 1.5)]
-32,768 to -32,255.5	1 000 0000 1111 1111	-32,256
-32,255.5 to -32,254.5	1 000 0010 0000 0001	-32,255
-1.5 to -0.5	1 111 1111 1111 1111	-1
-0.5 to 0.5	0 000 0000 0000 0000	0
0.5 to 1.5	0 000 0000 0000 0001	1
32,254.5 to 32,255.5	0 111 1101 1111 1111	32,255
32,255.5 to 32,768	0 111 1111 0000 0000	32,256

Fig. 7 Linear code

Phase	A-Law	μ-Law	Linear
-7/8 x 180°	0 011 0100	0 001 1110	1 101 1101 1000 0011
-5/8 x 180°	0 010 0001	0 000 1011	1 010 1110 1000 0011
-3/8 x 180°	0 010 0001	0 000 1011	1 010 1110 1000 0011
-1/8 x 180°	0 011 0100	0 001 1110	1 101 1101 1000 0011
1/8 x 180°	1 011 0100	1 001 1110	0 010 0010 0111 1100
3/8 x 180°	1 010 0001	1 000 1011	0 101 0001 0111 1100
5/8 x 180°	1 010 0001	1 000 1011	0 101 0001 0111 1100
7/8 x 180°	1 011 0100	1 001 1110	0 010 0010 0111 1100

Fig. 8 Digital milliwatts

Control and Monitoring

The MV3000 is controlled and monitored through the device control interface. This allows the use of the line control and status interface, the control of the PCM code and modes of operation, the programming of the transmit and receive clock and time slots, gain and filters, the control of the B-filter, and the activation and deactivation of the diagnostic functions.

Initialisation

When power is first applied, the MV3000 is reset and it goes into its power-down mode of operation. This has several consequences: the transmit PCM outputs (DXA and DXB) go into their high-impedance state and the analog output (VOUT) goes to analog ground (V_{AGND}); the transmit and receive slot addresses are set to zero; the control port pins (CP1 to CP5) are configured as inputs; A-Law is selected; the transmit and receive filters are disabled and the transmit and receive gains are set to 0 dB; and the adaption of the B-filter is enabled only if the SI pin is high.

After 500 µs control instructions may be sent to the device. These would normally be used to configure it and to take it out of power-down mode.

Stand-alone operation

If the default conditions established by initialisation are acceptable then stand-alone operation can be used. Stand-alone operation is selected by holding the CSB pin low. The power-up and power-down instructions can then be generated by holding the DI/O pin high or low, respectively. A clock must still be applied to the DCLK pin, but the 2048 kHz. clock supplied to the MCLK pin can be used. This means that the only difference between the power-up and power-down instructions for stand-alone operation or for normal operation is that in stand-alone operation the CSB pin is tied low.

Normal operation

For normal operation control information is sent to the MV3000 on the DI/O pin which is strobed under the control of the DCLK clock and CSB pulse. Data which is requested by the device is output on the DI/O pin. Fig. 9 shows the nominal timing of the signals.

The normal sequence is for a code byte to be sent to the device. This may be followed by a number of data bytes which may either be sent to the device or sent by it depending on the specific code byte. If the control instruction causes the device to accept further data bytes on DI/O, then programming will be aborted and the device will enter power-down mode if a power-down instruction is sent instead of an input data byte (**N.B.** There is no all zeroes data byte so confusion is avoided.).

Fig. 10 shows the various control instructions used and Fig. 11 shows the control byte map. The operation of each specific instruction is indicated in Figs. 12 to 21.

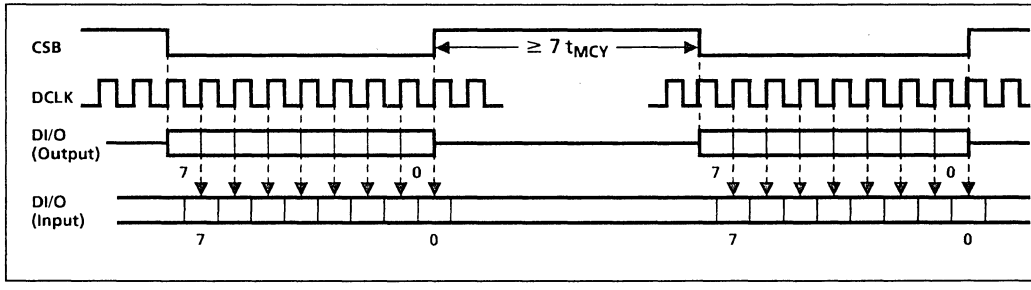


Fig. 9 Control timing diagram - normal operation

Instruction				Mnemonic	Op Code	Data Bytes
Power	Up			PU	FF	
	Down			PD	00	
Slot Address	Transmit	Read		STR	75	1 - Out
		Write	High	STWH	20 to 3F	
			Low	STWL	60 to 67	
	Receive	Read		SRR	7D	1 - Out
		Write	High	SRWH	40 to5F	
			Low	SRWL	68 to 6F	
Gain	Transmit	Read		GTR	71	2 - Out
		Write		GTW	72	2 - In
	Receive	Read		GRR	79	2 - Out
		Write		GRW	7A	2 - In
Filter	Enable			FE	80 to 87	
	Transmit	Read		FTR	A7	8 - Out
		Write		FTW	A4	8 - In
	Receive	Read		FRR	AB	8 - Out
		Write		FRW	A8	8 - In
	Balance	Control		FBC	BC to BF	
		Read		FBR	A3	20 - Out
		Write		FBW	A0	20 - In
Control Interface	Configuration	Read		CCR	C1	1 - Out
		Write		CCW	D1	1 - In
	Port	Read		CPR	C8	1 - Out
		Write		CPW	D8	1 - In
PCM	Code			PC	B8 to BB	
	Association	Read		PAR	77	1 - Out
		Write		PAW	90 to 9F	
Diagnostic	Reset			DR	B0	
	Transmit	High Pass Filter Disable		DTH	B3	
	Receive	Attenuate		DRA	B1	
		Disable Path		DRD	B2	
	Loop	Analog		DLA	B7	
		Digital		DLD	B4	

Fig. 10 Control instructions

NB All undefined bytes are reserved - do not use these.		Second Nibble															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
First Nibble	0	PD															
	1																
	2	STWH															
	3																
	4	SRWH															
	5																
	6	STWL								SRWL							
	7		GTR	GTW		STR		PAR			GRR	GRW			SRR		
	8	FE															
	9	PAW															
	A	FBW			FBR	FTW			FTR	FRW			FRR				
	B	DR	DRA	DRD	DTH	DLD			DLA	PC				FBC			
	C		CCR							CPR							
	D		CCW							CPW							
	E																
	F																PU

Fig. 11 Control byte map

Mnemonic	Op Code	Data Bytes	Description
PU	FF	-	**Power - Up.** This instruction takes the device out of power-down. It would normally be preceeded by instructions to configure the device. It has no effect if the device is not in power-down mode.
PD	00	-	**Power - Down.** This instruction puts the device into power-down mode. The transmit PCM outputs (DXA and DXB) go into their high impedance state and the analog output (VOUT) goes to V_{AGND}. The device is still programmable in this mode.

Fig. 12 Power instructions

Mnemonic	Op Code	Data Bytes	Description
STR	75	1 Output	**Slot Address - Transmit - Read.** This instruction causes the device to output a data byte which contains the transmit slot address. The data byte contains the 5 high address bits followed by the 3 low address bits. If the hex data byte is B1 then the high address is 22 and the low address is 1, i.e. the start of the transmit PCM output is offset by 177 (= 22x8 + 1) clock cycles.
STWH	20 to 3F	-	**Slot Address - Transmit - Write - High.** This instruction defines the transmit slot high address. The hex code 2A sets the high address to 10.
STWL	60 to 67	-	**Slot Address - Transmit - Write - Low.** This instruction defines the transmit slot low address. The hex code 63 sets the low address to 3.
SRR	7D	1 Output	**Slot Address - Receive - Read.** This instruction causes the device to output a data byte which contains the receive slot address. The data byte contains the 5 high address bits followed by the 3 low address bits. If the hex data byte is B1 then the high address is 22 and the low address is 1, i.e. the start of the transmit PCM input is offset by 177 (= 22x8 + 1) clock cycles.
SRWH	40 to 5F	-	**Slot Address - Receive - Write - High.** This instruction defines the receive slot high address. The hex code 4A sets the high address to 10.
SRWL	68 to 6F	-	**Slot Address - Receive - Write - Low.** This instruction defines the receive slot low address. The hex code 6B sets the low address to 3.

Fig. 13 Slot address instructions

Data Bytes									Description
Byte	D7	D6	D5	D4	D3	D2	D1	D0	These bytes contain a 2s complement number in the range +/- 2 which is used to construct the gain coefficients as follows:- $G = -G_1x2^1 + G_0x2^0 + ... + G_{-10}x2^{-10}$. The receive gain is:- $G_R = G$ i.e. -2 to 2. The transmit gain is:- $G_X = 2x(G + 1)$ i.e. -2 to 6.
1	1	G_1	G_0	G_{-1}	G_{-2}	G_{-3}	G_{-4}	G_{-5}	
2	1	G_{-6}	G_{-7}	G_{-8}	G_{-9}	G_{-10}	-	-	

Fig. 14 Gain coefficients

Mnemonic	Op Code	Data Bytes	Description
GTR	71	2 Output	**Gain - Transmit - Read.** This instruction causes the device to output 2 data bytes which contain the transmit gain information (see Fig. 14).
GTW	72	2 Input	**Gain - Transmit - Write.** This instruction sets the transmit gain to the value defined by the 2 data bytes (see Fig. 14).
GRR	79	2 Output	**Gain - Receive - Read.** This instruction causes the device to output 2 data bytes which contain the receive gain information (see Fig. 14).
GRW	7A	2 Input	**Gain - Receive - Write.** This instruction sets the receive gain to the value defined by the 2 data bytes (see Fig. 14).

Fig. 15 Gain instructions

Data Bytes									Description
Byte	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	A^3_1	A^3_0	A^3_{-1}	A^3_{-2}	A^3_{-3}	A^3_{-4}	A^3_{-5}	These bytes contain four 2s complement numbers in the range +/- 2 which are used to construct the filter coefficients as follows:- $A^m = -A^m{}_1x2^1 + A^m{}_0x2^0 + ... + A^m{}_{-10}x2^{-10}$ for m = 0, 1, 2, 3. The transfer function for the filter is:- $H(Z) = A^0 + A^1xZ^{-1} + A^2xZ^{-2} + A^3xZ^{-3}$. where the Z-transformation is at 16 kHz i.e. $Z = \exp(j2\pi fT)$ where T = 1/(16 kHz).
2	1	A^3_{-6}	A^3_{-7}	A^3_{-8}	A^3_{-9}	A^3_{-10}	-	-	
3	1	A^2_1	A^2_0	A^2_{-1}	A^2_{-2}	A^2_{-3}	A^2_{-4}	A^2_{-5}	
4	1	A^2_{-6}	A^2_{-7}	A^2_{-8}	A^2_{-9}	A^2_{-10}	-	-	
5	1	A^1_1	A^1_0	A^1_{-1}	A^1_{-2}	A^1_{-3}	A^1_{-4}	A^1_{-5}	
6	1	A^1_{-6}	A^1_{-7}	A^1_{-8}	A^1_{-9}	A^1_{-10}	-	-	
7	1	A^0_1	A^0_0	A^0_{-1}	A^0_{-2}	A^0_{-3}	A^0_{-4}	A^0_{-5}	
8	1	A^0_{-6}	A^0_{-7}	A^0_{-8}	A^0_{-9}	A^0_{-10}	-	-	

Fig. 16 Transmit and receive filter coefficients

Data Bytes									Description
Byte	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	B^8_1	B^8_0	B^8_{-1}	B^8_{-2}	B^8_{-3}	B^8_{-4}	B^8_{-5}	These bytes contain ten 2s complement numbers in the range +/- 2 which are used to construct the filter coefficients as follows:- $B^m = -B^m{}_1x2^1 + B^m{}_0x2^0 + B^m{}_{-1}x2^{-1} + ... + B^m{}_{-10}x2^{-10}$ for m = 0, 1, 2, ..., 9. The transfer function for the filter is:- $H(Z) = B^0 + B^1xZ^{-1} + B^2xZ^{-2} + B^3xZ^{-3} + ... + B^9xZ^{-9}$. where the Z-transformation is at 16 kHz i.e. $Z = \exp(j2\pi fT)$ where T = 1/(16 kHz). Only the 5 odd coefficients (B^9,B^7,B^5,B^3,B^1) adapt. Otherwise the filter would attempt to adapt to frequencies in the range 4kHz to 8kHz.
2	1	B^8_{-6}	B^8_{-7}	B^8_{-8}	B^8_{-9}	B^8_{-10}	-	-	
3	1	B^6_1	B^6_0	B^6_{-1}	B^6_{-2}	B^6_{-3}	B^6_{-4}	B^6_{-5}	
4	1	B^6_{-6}	B^6_{-7}	B^6_{-8}	B^6_{-9}	B^6_{-10}	-	-	
5	1	B^4_1	B^4_0	B^4_{-1}	B^4_{-2}	B^4_{-3}	B^4_{-4}	B^4_{-5}	
6	1	B^4_{-6}	B^4_{-7}	B^4_{-8}	B^4_{-9}	B^4_{-10}	-	-	
7	1	B^2_1	B^2_0	B^2_{-1}	B^2_{-2}	B^2_{-3}	B^2_{-4}	B^2_{-5}	
8	1	B^2_{-6}	B^2_{-7}	B^2_{-8}	B^2_{-9}	B^2_{-10}	-	-	
9	1	B^0_1	B^0_0	B^0_{-1}	B^0_{-2}	B^0_{-3}	B^0_{-4}	B^0_{-5}	
10	1	B^0_{-6}	B^0_{-7}	B^0_{-8}	B^0_{-9}	B^0_{-10}	-	-	
11	1	B^9_1	B^9_0	B^9_{-1}	B^9_{-2}	B^9_{-3}	B^9_{-4}	B^9_{-5}	
12	1	B^9_{-6}	B^9_{-7}	B^9_{-8}	B^9_{-9}	B^9_{-10}	-	-	
13	1	B^7_1	B^7_0	B^7_{-1}	B^7_{-2}	B^7_{-3}	B^7_{-4}	B^7_{-5}	
14	1	B^7_{-6}	B^7_{-7}	B^7_{-8}	B^7_{-9}	B^7_{-10}	-	-	
15	1	B^5_1	B^5_0	B^5_{-1}	B^5_{-2}	B^5_{-3}	B^5_{-4}	B^5_{-5}	
16	1	B^5_{-6}	B^5_{-7}	B^5_{-8}	B^5_{-9}	B^5_{-10}	-	-	
17	1	B^3_1	B^3_0	B^3_{-1}	B^3_{-2}	B^3_{-3}	B^3_{-4}	B^3_{-5}	
18	1	B^3_{-6}	B^3_{-7}	B^3_{-8}	B^3_{-9}	B^3_{-10}	-	-	
19	1	B^1_1	B^1_0	B^1_{-1}	B^1_{-2}	B^1_{-3}	B^1_{-4}	B^1_{-5}	
20	1	B^1_{-6}	B^1_{-7}	B^1_{-8}	B^1_{-9}	B^1_{-10}	-	-	

Fig. 17 Balance filter coefficients

Mnemonic	Op Code	Data Bytes	Description
FE	80 / 87	-	**Filter - Enable.** This instruction allows the balance (B) filter, transmit (X) filter and the receive (R) filter to be enabled or disabled. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 0 0 B_F X_F R_F If B_F is 1 then the B-filter is enabled. If it is 0 then the B-filter is disabled (i.e. Balance subtracts zero). If X_F is 1 then the X-filter is enabled. If it is 0 then the X-filter is disabled (i.e. the transfer function is set to 1). If R_F is 1 then the R-filter is enabled. If it is 0 then the R-filter is disabled (i.e. the transfer function is set to 1). **N.B.** Disabling a filter does not change its coefficients.
FTR	A7	8 Output	**Filter - Transmit - Read.** This instruction causes the device to output 8 data bytes which represent the 4 numbers corresponding to the 4 transmit filter coefficients (see Fig. 16).
FTW	A4	8 Input	**Filter - Transmit - Write.** This instruction sets the 4 transmit filter coefficients to the 4 numbers represented by the 8 data bytes (see Fig. 16).
FRR	AB	8 Output	**Filter - Receive - Read.** This instruction causes the device to output 8 data bytes which represent the 4 numbers corresponding to the 4 receive filter coefficients (see Fig. 16).
FRW	A8	8 Input	**Filter - Receive - Write.** This instruction sets the 4 receive filter coefficients to the 4 numbers represented by the 8 data bytes (see Fig. 16).
FBC	BC to BF	-	**Filter - Balance - Control.** This instruction allows the automatic adaption of the B-filter to be enabled or disabled. There is a 2-bit field in the instruction which allows adaption to be enabled with or without polling the SI pin. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 1 B_D B_A If B_D is 1 then adaption of the B-filter is disabled. If B_D is 0 then the adaption is enabled if either B_A is 1 or if the SI pin is high.
FBR	A3	20 Output	**Filter - Balance - Read.** This instruction causes the device to output 20 data bytes which represent the 10 numbers corresponding to the 10 balance filter coefficients (see Fig. 17).
FBW	A0	20 Input	**Filter - Balance - Write.** This instruction sets the 10 balance filter coefficients to the 10 numbers represented by the 20 data bytes (see Fig. 17).

Fig. 18 Filter instructions

Mnemonic	Op Code	Data Bytes	Description
CCR	C1	1 Output	**Control Interface - Configuration - Read.** The data byte which is output by the device during this instruction indicates which of the control pins are inputs and which are outputs. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CC1 CC2 CC3 CC4 CC5 X X X If CCn is 0 then the CPn pin is an output. If CCn is 1 then the CPn pin is an input (n = 1, 2, 3, 4, 5).
CCW	D1	1 Input	**Control Interface - Configuration - Write.** This instruction configures the control pins to be inputs or outputs according to the input data byte. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CC1 CC2 CC3 CC4 CC5 R2 R1 R0 If CCn is 0 then the CPn pin is an output. If CCn is 1 then the CPn pin is an input (n = 1, 2, 3, 4, 5). The R2 / 0 bits are reserved and should be held at 1. **N.B.** When power is first applied these pins are configured as inputs.
CPR	C8	1 Output	**Control Interface - Port - Read.** The data byte which is output by the device during the instruction indicates the status of the control pin and the SI pin. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CP1 CP2 CP3 CP4 CP5 X X SI If the CPn pin is configured as an input then the CPn bit is 1 or 0 depending on whenther the input is high or low. If the CPn pin is configured as an output then the CPn bit is 1 or 0 depending on whether the output is high or low (n = 1, 2, 3, 4, 5). The SI bit is 1 or 0 depending on whether the SI pin is high or low.
CPW	D8	1 Input	**Control Interface - Port - Write.** This instruction controls the output levels of those control pins configured as outputs according to the input data byte. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CP1 CP2 CP3 CP4 CP5 R2 R1 R0 If the CPn pin is configured as an output then it will go high or low depending on whether the CPn bit is 1 or 0. If the CPn pin is configured as an input then the corresponding CPn bit should be held at 0 (n = 1, 2, 3, 4, 5). The R2 / 0 bits are reserved and should be held at 1.

Fig. 19 Control interface instructions

Mnemonic	Op Code	Data Bytes	Description
PC	B8 to BB	-	**PCM - Code.** This instruction defines the PCM code used by the device. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 0 C1 C0 C1 C0 Code 0 0 Linear (16 bits) 0 1 u-law (8 bits) 1 0 A-law (8 bits) 1 1 Reserved - do not use.
PAR	77	1 Output	**PCM - Association - Read.** The data byte which is output by the device during the instruction indicates whether the PCM is associated with the A or B pins and with the first or second segment of 256 bits. Separate associations are used for both transmitted and received PCM. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 X X X X R_B X_B R_{SA} X_{SA} If the R_B bit is 1 then the DRB pin is used for the receive PCM input. If it is 0 then DRA is used. If the X_B bit is 1 then the DXB pin is used for the transmit PCM output. If it is 0 then DXA is used. If the R_{SA} bit is 0 then the receive segment address is 0 and the receive PCM is associated with the first segment of 256 bits. If it is 1 then the receive PCM is associated with the second segment of 256 bits. If the X_{SA} bit is 0 then the transmit segment address is 0 and the transmit PCM is associated with the first segment of 256 bits. If it is 1 then the transmit PCM is associated with the second segment of 256 bits.
PAW	90 to 9F		**PCM - Association - Write.** This instruction determines whether the PCM is associated with the A or B pins and with the first or second segment of 256 bits. Separate associations are used for both transmitted and received PCM. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 1 R_B X_B R_{SA} X_{SA} If the R_B bit is 1 then the DRB pin is used for the receive PCM input. If it is 0 then DRA is used. If the X_B bit is 1 then the DXB pin is used for the transmit PCM output. If it is 0 then DXA is used. If the R_{SA} bit is 0 then the receive segment address is 0 and the receive PCM is associated with the first segment of 256 bits. If it is 1 then the receive PCM is associated with the second segment of 256 bits. If the X_{SA} bit is 0 then the transmit segment address is 0 and the transmit PCM is associated with the first segment of 256 bits. If it is 1 then the transmit PCM is associated with the second segment of 256 bits.

Fig. 20 PCM instructions

Mnemonic	Op Code	Data Bytes	Description
DR	B0	-	**Diagnostic - Reset.** This instruction resets any transmit, receive or loop test conditions previously set up.
DTH	B3	-	**Diagnostic - Transmit - High Pass Filter Disable.** This instruction disables the digital high-pass filter in the transmit path.
DRA	B1	-	**Diagnostic - Receive - Attenuate.** This instruction adds 6dB attenuation to the receive path.
DRD	B2	-	**Diagnostic - Receive - Disable Path.** This instruction disables the receive path. This means that V_{OUT} is set to V_{OO} regardless of the receive PCM data input to the device.
DLA	B7	-	**Diagnostic - Loop - Analog.** This instruction puts the device into its analog loop test mode. This means that the analog signal output on the VOUT pin is derived from the analog signal on the VIN pin instead of the normal filtered PCM receive data.
DLD	B4	-	**Diagnostic - Loop - Digital.** This instruction puts the device into its digital loop test mode. This means that the digital PCM signal input on DRA or DRB is switched internally, multiplied by 15/16 and replaces the digital PCM signal normally output on DXA or DXB.

Fig. 21 Diagnostic instructions

PIN DESCRIPTIONS

Symbol	Pin No.	Pin Name and Description
CAP	1	**Capacitor (Analog Node).** A capacitor of 0.1 uF should be connected between this pin and analog ground (AGND pin). This is used to decouple the internal voltage reference.
VIN	2	**Input Voltage (Analog Input).** The analog voltage input at this pin is sampled, processed, digitally encoded and then output as PCM data on either DXA or DXB. This signal is referenced to AGND and there is an input impedance of 30k Ohms to $AV_{CC}/3$.
AGND	3	**Analog Ground (Power Input).** This is the ground reference pin for the analog input (VIN pin) and analog output (VOUT pin). Care should be taken to minimise the noise at this pin.
VOUT	4	**Output Voltage (Analog Output).** The analog voltage at this pin is derived from the PCM data input on either DRA or DRB. This PCM data is processed digitally, decoded, converted to analog and then output here. This signal is referenced to AGND but has a DC offset of nominally 2.5 Volts.
SI	5	**Status In (Digital Input).** The data sampled at this input can be read out on the DI/O pin. This allows information about the status of the telephone line to be passed on to a line card controller. This pin can also be used to control the operation of the filter used for adaptive balancing (the B-filter).
CP1 to 5	6 to10	**Control Port 1 to 5 (Digital I/O with Pullups).** These pins are independently programmable as either inputs or outputs through the control stream input on DI/O. Pins which are programmed as outputs are also controlled by DI/O. Pins which are programmed as inputs can be read on DI/O. These pins allow a line card controller to monitor and control the line cards and mean that a single hardware design for a line card can be configured through software for a number of different requirements. There are pullups of 150k Ohms on these pins.
TSCA, TSCB	11, 18	**Time Slot Control A, B (Open Drain Pulldown Outputs).** The TSCA OR TSCB pins are pulled low when PCM data is output on DXA OR DXB respectively. These pins on different devices may be connected together with a single pullup resistor (wire-ored) to generate an enable signal for an output buffer on a line card.
DXA, DXB	12, 17	**Digital Transmit A, B (Three-State Outputs).** The PCM data is output at these pins. The data is routed to either DXA or DXB under the direction of the control stream input at the DI/O pin. The PCM data can be μ-law (8 bits), A-law (8 bits) or linear (16 bits). Bit and frame synchronisation are established by CLKX and FSX. The start of the PCM burst relative to the pulse on FSX is determined by the serial control at DI/O. A data word is output once every 125 us. These pins go to their high impedance state between PCM bursts and when the device is in standby mode.
TEST	13	**Test Pin (Internal Connection).** This pin is used during device testing. It should be held low during normal operation.
DRA, DRB	14, 21	**Digital Receive A, B (Digital Inputs).** These are the inputs for PCM data. Either DRA or DRB is used under the direction of the serial control input at DI/O. The PCM data can be μ-law (8 bits), A-law (8 bits) or linear (16 bits). Bit and frame synchronisation are established by CLKR and FSR. The position of the first bit sampled relative to the pulse on FSR is also determined by the serial control at DI/O. A data word is sampled once every 125 us.

PIN DESCRIPTIONS (Continued)

Symbol	Pin No.	Pin Name and Description
CLKX	15	**Transmit Clock (Digital Input).** The clock input at this pin establishes the bit synchronisation on the PCM data output on DXA and DXB. The clock frequency must be between 64 KHz and 4.096 MHz and there must be an integral number of clock cycles between pulses on FSX. This clock should also be locked to the MCLK clock.
FSX	16	**Transmit Frame Synchronisation (Digital Input).** The pulse input at this pin establishes the frame synchronisation on the PCM data output on DXA and DXB. There should be 125 us between pulses and the pulses should be synchronised with CLKX.
DXB	17	See pin 12.
TSCB	18	See pin 11.
CLKR	19	**Receive Clock (Digital Input).** The clock input at this pin strobes the bits of PCM data input on DRA and DRB. The clock frequency must be between 64 KHz and 4.096 MHz and there must be an integral number of clock cycles between pulses on FSR. This clock should also be locked to the MCLK clock.
FSR	20	**Receive Frame Synchronisation (Digital Input).** The pulse input at this pin establishes the frame synchronisation on the PCM data input on DRA and DRB. There should be 125 us between pulses and the pulses should be synchronised with CLKR.
DRB	21	See pin 14.
DGND	22	**Digital Ground (Power Input).** 0 Volts Supply.
CSB	23	**Chip Select Bar (Digital Input).** This input should be held low to enable the chip to input or output serial data on DI/O. This input is used to gate DCLK when a command or data is to be entered on or output on DI/O. If held low for more than 8 cycles of DCLK it will force the device into stand-alone operation.
DI/O	24	**Data In/Out (Digital Input/Output with Pullup).** Serial control data is input and output at this pin when CSB is low. Input data is sampled by DCLK and output data is clocked out by DCLK. The data is used to control and monitor a wide variety of programmable functions. A common data input/output line can be used by a number of devices.
DCLK	25	**Data Clock (Digital Input).** This clock strobes the serial control input data and clocks out serial control output data on DI/O. It is used in association with the CSB pin. The clock can run at any frequency from DC to 2.048 MHz.
MCLK	26	**Master Clock (Digital Input).** This clock controls the sampling for the analog to digital conversion and the signal reconstruction for the digital to analog conversion. This clock should also be locked to the CLKX and CLKR clocks.
DVCC	27	**Digital Positive Supply Voltage (Power Input).** 5 Volts.
AVCC	28	**Analog Positive Supply Voltage (Power Input).** 5 Volts.

ELECTRICAL CHARACTERISTICS

Test Conditions - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value			Units
		Min.	Typ.*	Max.	
Analog Supply Voltage	AV_{CC}	4.75	5	5.25	Volts
Digital Ground Voltage	V_{DGND}	-0.1	0	0.1	Volts
Digital Supply Voltage	DV_{CC}	4.75	5	5.25	Volts
Ambient Temperature	T_{AMB}	0		70	°C
Input Low Voltage (with respect to V_{DGND})	V_{IL}	0	0.4	0.8	Volts
Input High Voltage (with respect to V_{DGND})	V_{IH}	2.0	2.4	DV_{CC}	Volts
Output Loading	C_O			150	pF
Master Clock Frequency	F_M	2047.9	2048	2048.1	kHz
Analog Input Voltage	V_{IA}	-3.0		3.0	Volts

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Digital Static Characteristics - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Normal Supply Current	I_N		30		mA	Unloaded
Power-down Supply Current	I_{PD}		20		mA	Unloaded
Input Leakage Current	I_{IL}			10	uA	$0<V<DV_{CC}$
Output High Voltage	V_{OH}	2.4		DV_{CC}	Volts	I_{OH} (Source) = 400uA
Output Low Voltage	V_{OL}	0		0.4	Volts	I_{OL} (Sink) = 2mA
Output Leakage Current	I_{OL}			10	uA	$0<V<DV_{CC}$

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Digital Dynamic Characteristics - Master Clock (see Fig. 22)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Master Clock Rise Time	t_{MR}		20		ns	
Master Clock High Period	t_{MH}	50	236		ns	
Master Clock Fall Time	t_{MF}		20		ns	
Master Clock Low Period	t_{ML}	50	236		ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

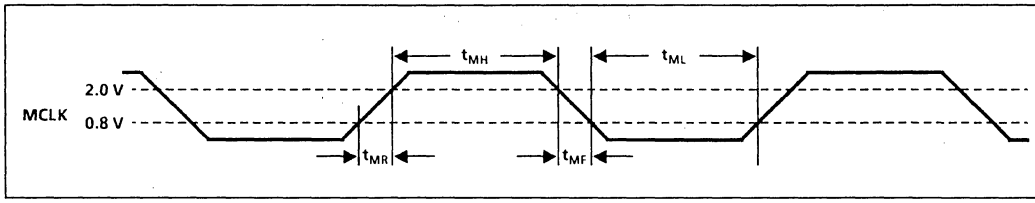


Fig. 22 Timing - master clock

Digital Dynamic Characteristics - PCM Clocks and Frame Synchronisation (see Figs. 23 and 24)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
PCM Clock Period	t_{PCP}	225	488	15650	ns	
PCM Clock Rise Time	t_{PCR}			20	ns	
PCM Clock High Period	t_{PCH}	100			ns	
PCM Clock Fall Time	t_{PCF}			20	ns	
PCM Clock Low Period	t_{PCL}	100			ns	
PCM Frame Sync. Set-up Time	t_{PFS}	50			ns	
PCM Frame Sync. Hold Time	t_{PFH}	30			ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

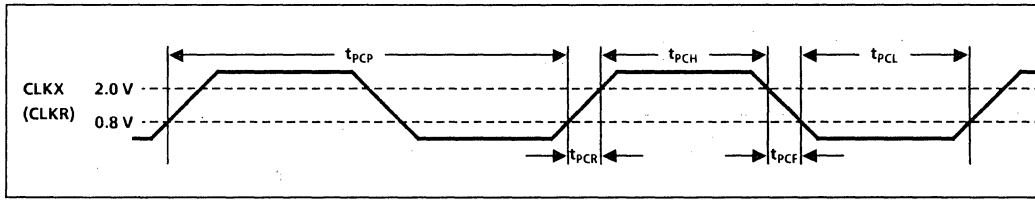


Fig. 23 Timing - PCM clocks

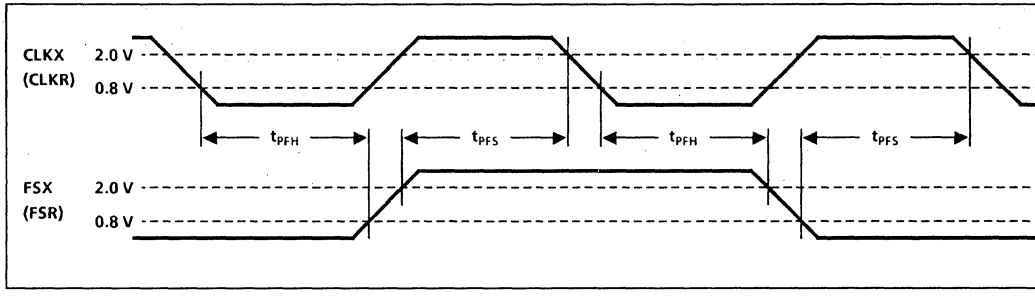


Fig. 24 Timing - PCM frame synchronisation

Digital Dynamic Characteristics - PCM Outputs (see Figs. 25 and 26)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
TSC Low Delay	t_{TLD}			150	ns	
TSC High Delay	t_{THD}			150	ns	
PCM Active Delay	t_{PAD}	70		170	ns	
PCM Passive Delay	t_{PPD}			70	ns	
PCM Output Hold Time	t_{POH}	30			ns	
PCM Output Delay	t_{POD}			100	ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

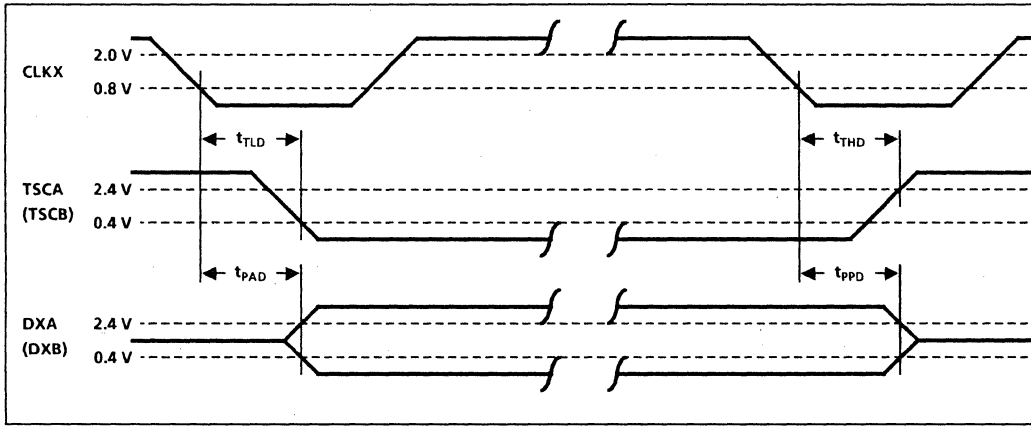


Fig. 25 Timing - PCM Output Start and Stop of Burst (see Fig. 4)

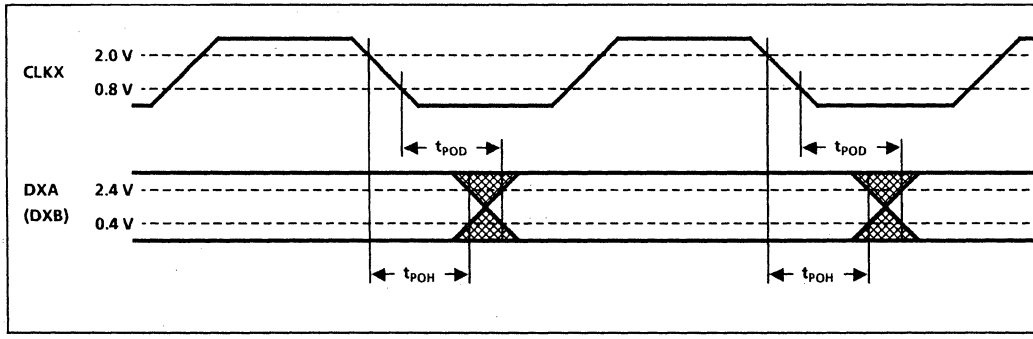


Fig. 26 Timing - PCM output changing during burst (see Fig. 4)

Digital Dynamic Characteristics - PCM Input (see Fig. 27)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
PCM Input Set-up Time	t_{PIS}	50	$t_{PCP}/2$		ns	
PCM Input Hold Time	t_{PIH}	30	$t_{PCP}/2$		ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

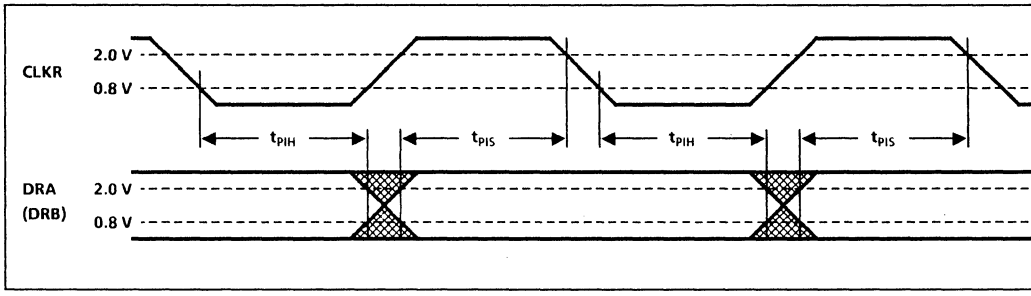


Fig. 27 Timing - PCM input (see Fig. 3)

Digital Dynamic Characteristics - Data Clock (see Fig. 28)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Data Clock Period ①	t_{DCP}	450			ns	
Data Clock Rise Time	t_{DCR}		25	50	ns	
Data Clock High Period	t_{DCH}	$t_{DCP}/2$ -50		$t_{DCP}/2$ + 50	ns	
Data Clock Fall Time	t_{DCF}		25	50	ns	
Data Clock Low Period	t_{DCL}	$t_{DCP}/2$ -50		$t_{DCP}/2$ + 50	ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

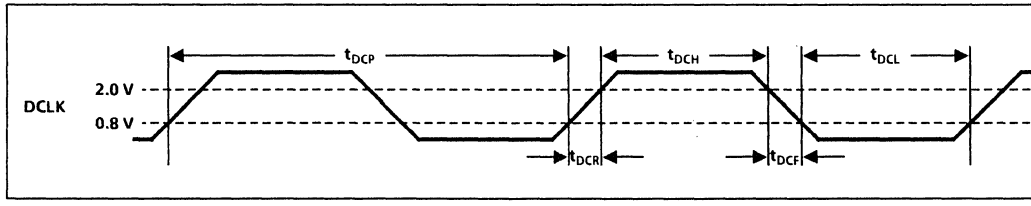


Fig. 28 Timing - PCM clocks

Digital Dynamic Characteristics - Chip Select ① (see Fig. 29)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Chip Select Falling Hold Time	t_{CFH}	0			ns	
Chip Select Falling Set-up Time	t_{CFS}	150			ns	
Chip Select Rising Hold Time	t_{CRH}	0			ns	
Chip Select Rising Set-up Time	t_{CRS}	150			ns	
Chip Select Low Period	t_{CLP}		$8t_{DCP}$		ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
① If CSB is tied low then the MV3000 will operate in stand-alone mode.

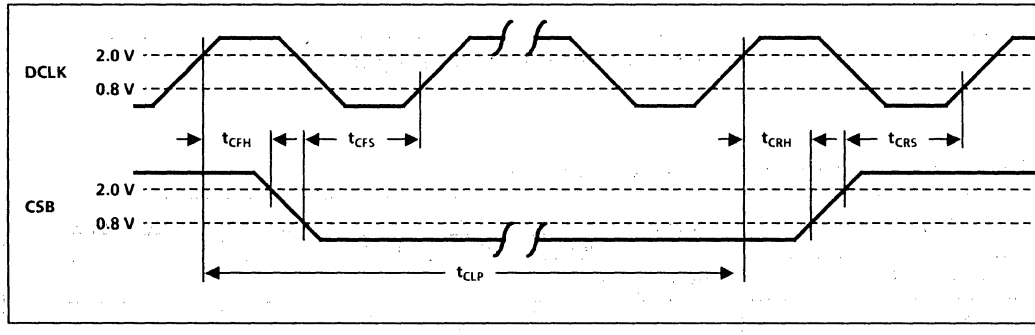


Fig. 29 Timing - chip select (see Fig. 9)

Digital Dynamic Characteristics - Data Input (see Fig. 30)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Data Input Set-up Time	t_{DIS}	50	$t_{DCP}/2$		ns	
Data Input Hold Time	t_{DIH}	30	$t_{DCP}/2$		ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

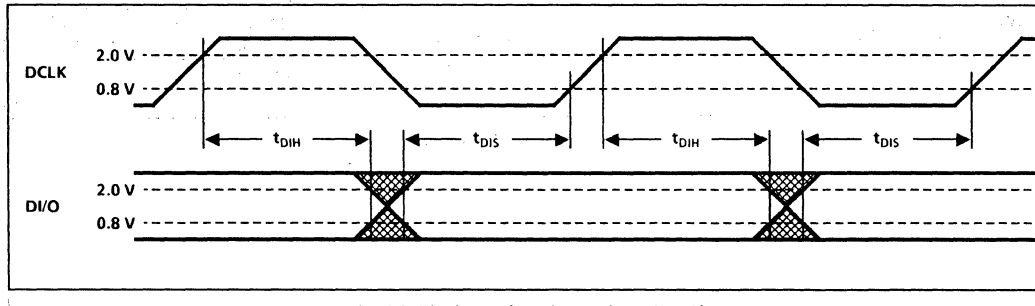


Fig. 30 Timing - data input (see Fig. 9)

Digital Dynamic Characteristics - Data Outputs (see Figs. 31 and 32)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Data Active Delay	t_{DAD}			100	ns	
Data Passive Delay	t_{DPD}			100	ns	
Data Output Hold Time	t_{DOH}	30	50		ns	
Data Output Delay	t_{DOD}		100	150	ns	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

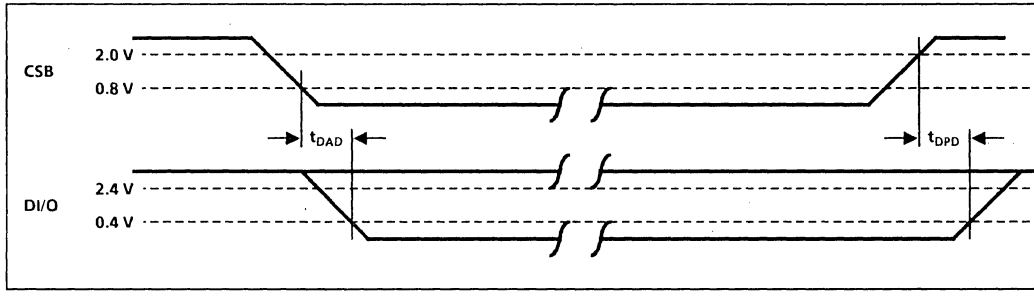


Fig. 31 Timing - data output start and stop of burst (see Fig. 9)

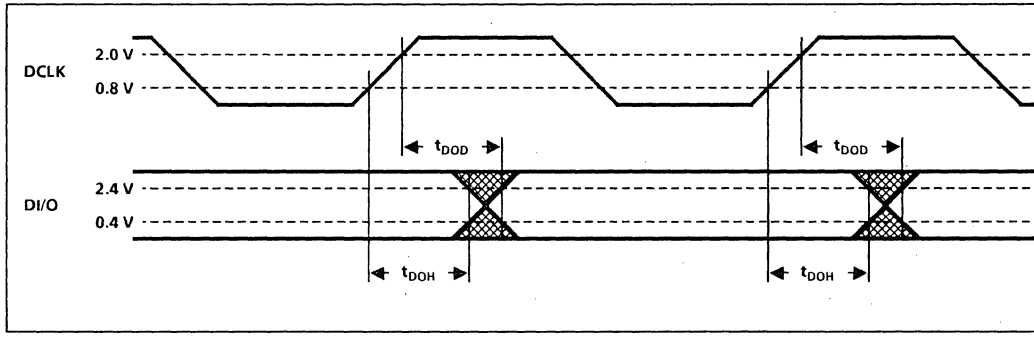


Fig. 32 Timing - data output changing during burst (see Fig. 9)

Analog Static Characteristics - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Pin Capacitance	C_P		8	10	pF	$0<V<AV_{CC}$, DV_{CC}
Analog Input Impedance	Z_I	20	30		kΩ	$-3V<V<+3V$
Analog Input Bias	V_{BI}		$AV_{CC}/3$		V	
Input Offset Voltage	V_{IO}	-5		5	mV	
Output Impedance	Z_O			20	Ω	$1V<V<4V$
Output Offset Voltage	V_{OO}	2.3	2.5	2.7	V	
Analog Output Voltage	V_{OA}	V_{OO}-1.5		V_{OO} + 1.5	V	R_L = 10kΩ, C_L = 50pF

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Analog Dynamic Characteristics - General

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Transmit 0 dBm0 Level	V_{TO}	4.03 4.00	4.18 4.15	4.33 4.30	$V_{P/P}$	A-Law μ-Law
Receive 0 dBm0 Level	V_{RO}	2.01 2.00	2.09 2.075	2.17 2.15	$V_{P/P}$	A-Law μ-Law
Power Supply Rejection	P_{SR}	50			dB	
Minimum Receive Gain MV3000A MV3000B	G_{RMIN}		-12.1 -6.1	-12 -6	dB	All CCITT G.714 Specifications
Maximum Transmit Gain MV3000A MV3000B	G_{TMAX}	12 6	12.1 6.1		dB	All CCITT G.714 Specifications

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Analog Dynamic Characteristics - Channel Gain (see Figs. 33 and 34)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Transmit Gain	G_T	 -0.125 -0.35 -0.8	 0 0	-80 -25 -25 0 0.125 0.125 0 -17.5 -35	dB	0 Hz 50 Hz 60 Hz 200 Hz 300 - 3000 Hz 3300 Hz 3400 Hz 4000 Hz >4600 Hz
Receive Gain	G_R	-0.125 -0.35 -0.8	0 0	0.125 0.125 0 -17.5 -35	dB	0 - 3000 Hz 3300 Hz 3400 Hz 4000 Hz >4600 Hz

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

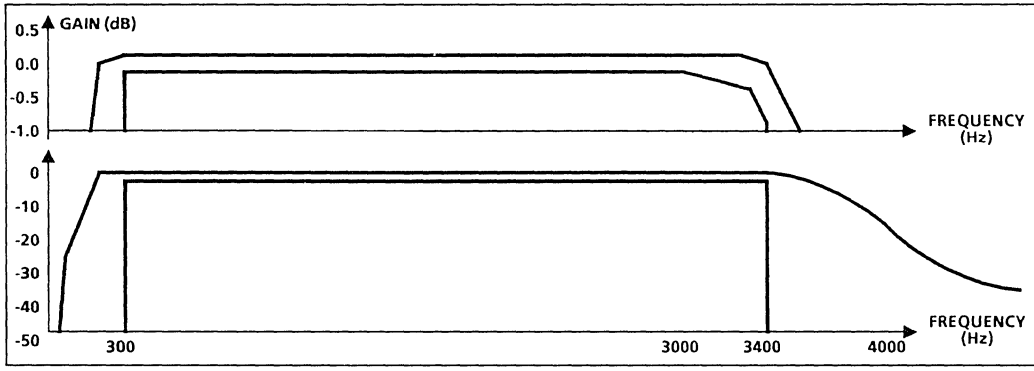


Fig. 33 Transmit channel gain

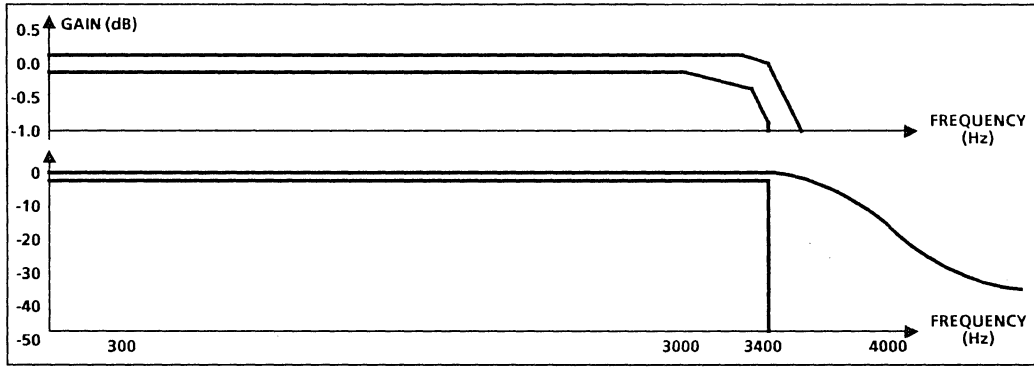


Fig. 34 Receive channel gain

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Analog Supply Voltage	AV_{CC}	-0.5	5.7	Volts
Digital Supply Voltage	DV_{CC}	-0.5	5.7	Volts
Storage Temperature	T_S	-65	125	°C
Input Voltage - except VIN pin	V_I	-0.3	DV_{CC} + 0.3	Volts
Input Voltage - VIN pin	V_{VIN}	-3.3	3.3	Volts
Output Voltage - except VOUT pin	V_O	-0.3	DV_{CC} + 0.3	Volts
Output Voltage - VOUT pin	V_{VOUT}	-0.3	AV_{CC} + 0.3	Volts
Clamp Current (Sink or Source beyond Power Supply) ①	I_K		100	mA
Package Power Dissipation	P		800	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

① Currents above this may cause latchup or destroy the input protection circuitry.

PLESSEY
Semiconductors

MV3506 A-LAW FILTER/CODEC
MV3507 μ-LAW FILTER/CODEC
MV3507A μ-LAW FILTER/CODEC WITH A/B SIGNALLING
MV3508 A-LAW FILTER/CODEC WITH OPTIONAL SQUELCH
MV3509 μ-LAW FILTER/CODEC WITH OPTIONAL SQUELCH

These devices are silicon gate CMOS Companding Encoder/Decoder integrated circuits designed to implement the per channel voice frequency Codecs used in PCM systems. They contain the band-limiting filters and the analog to digital conversion circuits that conform to the desired transfer characteristic. The MV3506 and MV3508 provide the European A-Law companding and the MV3507, MV3507A and MV3509 provide the North American μ-Law companding characteristic. The MV3508 and MV3509 have programmable squelch circuitry to reduce idle channel noise. The MV3507A provides for A/B bit signalling.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

FEATURES

- Low Power CMOS 80mW (Operating) 10mW (Standby)
- Meets or Exceeds AT & T3, and CCITT G.711, G.712 and G.733 Specifications
- Input Analog Filter Eliminates Need for External Anti-aliasing Prefilter
- Uncommitted Input and Output Op. Amps for Programming Gain
- Output Op. Amp Provides ±3.1V into a 1200 Ohms Load or can be Switched Off for Reduced Power (70mW)
- Encoder has Dual-speed Auto-zero Loop for Fast Acquisition on Power-up
- Low Absolute Group Delay = 410 microseconds at 1kHz

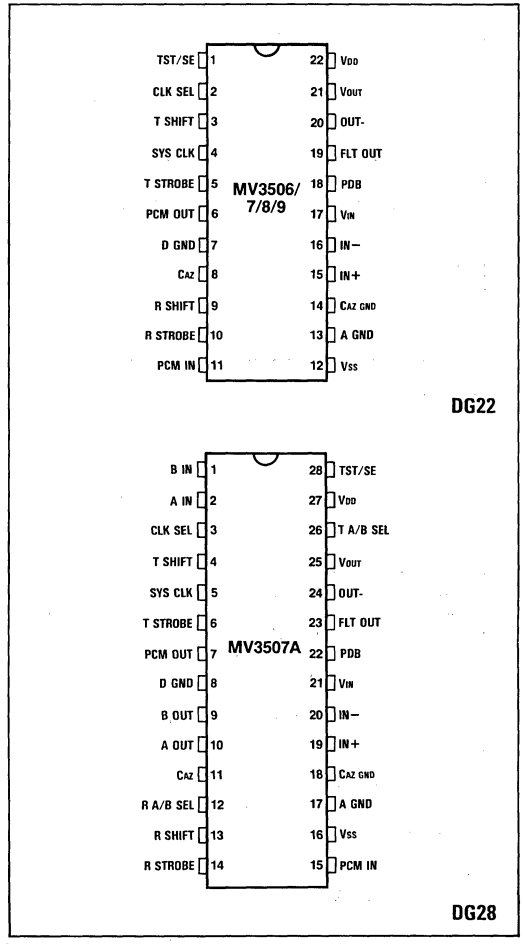


Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the devices. They contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps.

Transmit Section

Input analog signals first enter the chip at the uncommitted op.amp. terminals (IN + and IN- pins). This allows for the gain in the system to be trimmed. From the V_{IN} pin the signal enters a second-order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typically) at 256kHz and 44dB (typically) at 512kHz.

The signal next enters the transmit filter, which is a fifth-order low-pass filter clocked at 256kHz, followed by a third-order high-pass filter clocked at 64kHz. The resulting bandpass characteristics meet the CCITT specifications G.711, G.712 and G.733. Some representative attenuations are better than 26dB from 0 to 60Hz and better than 35dB from 4.6kHz to 100kHz.

The output of the transmit filter is sampled at the analog to digital encoder by a capacitor array at the sampling rate of 8kHz. The successive approximation conversion process requires about 72μsec.

The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz in 8kHz steps (see Figs. 3 and 4). A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

Included in the circuitry of the MV3507 is 'All Zero' code suppression so that negative input signal values between decision values numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronisation by DS1 (T1) line clock recovery circuitry as there are never more than 15 consecutive zeros.

An additional feature of the MV3506/7 and 7A is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of these chips is such that for 250ms the only code words generated were +0, -0, +1 or -1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation resetting the 250ms timer. This feature is a form of idle Channel Noise 'Squelch' or 'Crosstalk Suppression'. It is of particular importance in the MV3506 A-Law version because the A-Law transfer characteristic has 'mid-riser' bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz and 2.048MHz clocks the PCM data into the input buffer register once every sampling period (see Figs.5 and 6). A charge proportional to the received PCM data word appears on the decoder capacitor array of the digital to analog converter. A sample and hold circuit, initialised to zro by a narrow pulse at the beginning of each sampling period, integrates the charge and holds it for the rest of the sampling period.

The receive filter, consisting of a switched-capacitor fifth-order low-pass filter clocked at 256kHz, smooths the sampled and held signal. It also performs the loss equalisation to compensate for the sin(x)/x distortion due to the sampling.

The filter output (FLT OUT pin) is available for driving electronic hybrids directly as long as the impedance is greater than 20kΩ. When used in this fashion the low impedance output amp can be switched off for a considerable saving in power consumption. When it is required to drive a 600Ω load the output amp allows gain trimming as well as impedance matching.

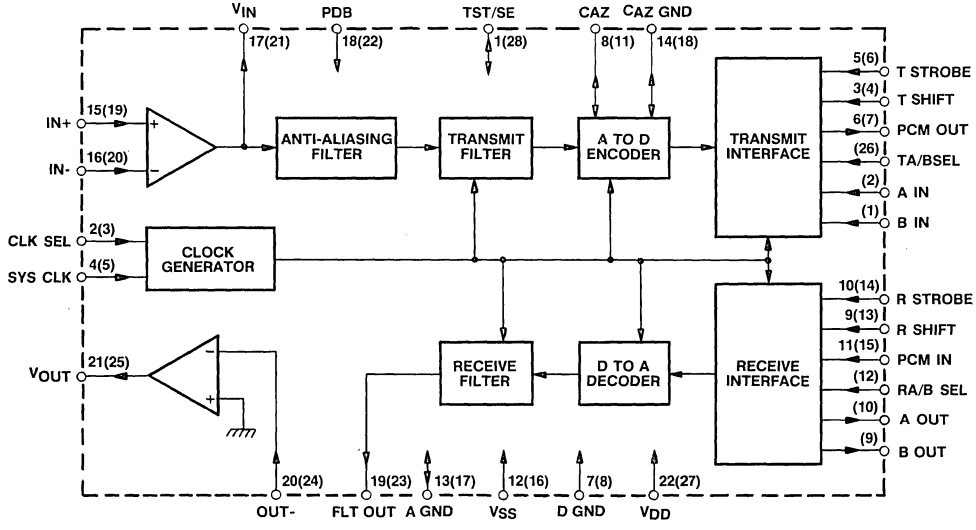


Fig.2 Functional block diagram (pin numbers for the MV3507A are in brackets)

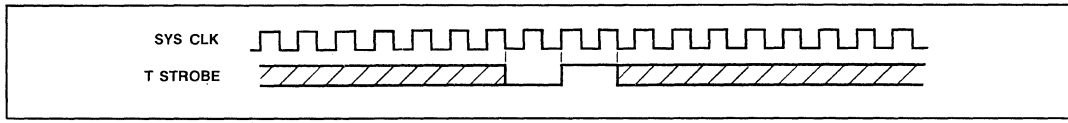


Fig.3 Transmit strobe alignment

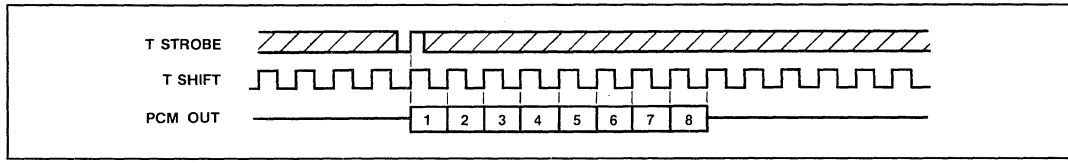


Fig.4 Transmit alignment

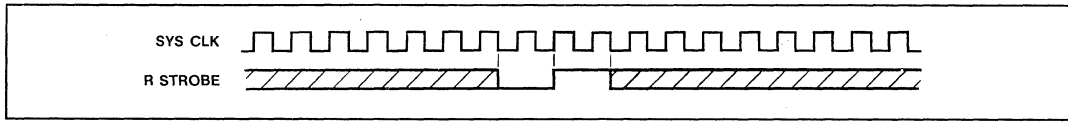


Fig.5 Receive strobe alignment

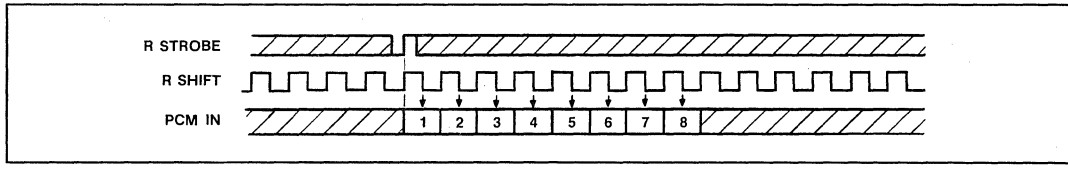


Fig.6 Receive alignment

Timing Requirements

The internal design of the devices paid careful attention to the timing requirements of various systems. In North America, central office and channel bank designs often follow the American Telephone and Telegraph Company's T1 (DS1) Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Nevertheless, in digital telephone designs, Codecs may be used in a non-multiplexed form with a daa rate as low as 64kbit/s. The μ-Law Codecs fulfil these requirements.

In Europe, telephone exchange and channel bank designs often follow the CCITT carrier PCM format to multiplex 30 telephony channels at a data rate of 2.048Mbit/s. The A-Law Codecs are designed for this market and will also handle PABX and digital telephone applications.

The timing format chosen for the devices allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kbit/s to 2.048Mbit/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows for this variation.

The devices do not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+ve) edges of the strobe, forcing the PCM output into its high impedance state after the 8th bit is shifted out. This allows the width of the strobe signal to vary as long as its repetition rate is 8kHz and the transmit and receive shift clocks are synchronised to it.

System Clock

The basic timing is provided by the system clock which is divided down internally to provide the various filter clocks and the timing for the conversions. The transmit and receive strobes and clocks must be locked to this clock so that the PCM data matches the sample rates.

Signalling in 7-Law Systems

In μ-Law systems there is a requirement for signalling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7⅝ bit rather than 8 bit because the LSB in every 6th frame is replaced by a signalling bit. This is referred to as A/B signalling and if a signalling frame carries the 'A' bit, then 6 frames later the LSB will carry the 'B' bit. To meet this requirement, the MV3507A is available in a 28-pin package.

Signalling Interface

In the AT&T T1 carrier PCM format (DS1) an A/B signalling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground etc, depending on the application. Two signalling conditions (A and B) per channel, giving four possible signalling states per channel are repeated every 12 frames (1.5msec). The A signalling condition is sent on bit 8 of all 24 channels in frame 6 and the B signalling condition is sent in frame 12. In each frame, the 193rd bit (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The MV3507A in a 28-pin package is designed to simplify the signalling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronises the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channel bank. The A and B signalling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore the A/B select input must go positive in the beginning of frame 5 and negative in the beginning of frame 11.

The decoder uses a similar scheme for receiving the A and B signalling bits, with one difference. They are latched to the respective outputs in the same frame in which A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12. In the T1 (DS1) carrier system, 24 voice channels are multiplexed to form the transmit and receive PCM highway, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mbit/s. Within the channel bank the transmit and receive channels of a Codec can occupy the same time slot for synchronous operation or they can be independent of each other for asynchronous operation. Asynchronous operation helps minimise switching delays through the system. Since the timing interface for the coder and decoder sections are independent of each other in the MV3507A, it can be operated in either manner.

In the CCITT carrier system 30 voice channels and 2 framing and signalling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mbit/s.

PIN DESCRIPTIONS

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
TST/SE	1	28	**Test/Squelch Enable (Internal Connection/Digital Input).** This pin is an internal test connection on the MV3506, MV3507 and MV3507A, and it is the squelch enable input on the MV3508 and MV3509. On the MV3506/7/7A it should be left unconnected or connected to the A GND pin via a capacitor for normal operation. On the MV3508/9 it should be tied high to enable the squelch feature and it should be left unconnected otherwise.
CLK SEL	2	3	**Clock Select (Three Level Input).** This pin selects the proper divide ratios for a 256kHz, 1.544MHz or 2.048MHz system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz operation, to D GND (0V) for 256kHz operation, and to V_{SS} (-5V) for 1.544MHz operation.
T SHIFT	3	4	**Transmit Shift Clock (Digital Input).** This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
SYS CLK	4	5	**System Clock (Digital Input).** This pin is a TTL compatible input for either a 256kHz, 1.544MHz or a 2.048MHz clock that is divided down to provide the filter clocks. The status of the CLK SEL pin must correspond to the provided clock frequency.
T STROBE	5	6	**Transmit Strobe (Digital Input with Pull-up).** This TTL compatible pulse input (typically 8kHz) is used for analog sampling and initiating the PCM output from the coder. It must be synchronised with the T SHIFT and SYS CLK clocks with its positive going edges occurring after the falling edges of these clocks. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
PCM OUT	6	7	**PCM Out (Pull-down Output).** This is a LS TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of the T SHIFT clock signal following positive edge on the T STROBE input. Data is clocked out by the positive edge on the T SHIFT clock into one 510Ω pull-up per system plus 2 LS TTL inputs.
D GND	7	8	**Digital Ground (Power Input).** 0V.
C_{AZ}	8	11	**Auto Zero Capacitor (Reference Node).** A capacitor of 0.1μF (±20%) should be connected between this pin and $C_{AZ\,GND}$ for coder auto zero operation. The sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
R SHIFT	9	13	**Receive Shift Clock (Digital Input).** This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
R STROBE	10	14	**Receive Strobe (Digital Input with Pull-up).** This TTL compatible pulse input (typically 8kHz) initiates clocking of PCM input data into the decoder. It must be synchronised with the R SHIFT and SYS CLK clocks with its positive going edges occurring after the falling edges of these clocks. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
PCM IN	11	15	**PCM In (Digital Input).** This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of the R SHIFT clock.
V_{SS}	12	16	**Negative Supply (Power Input).** -5V.
A GND	13	17	**Analog Ground (Reference Node).** This is the ground reference node for analog signals.
$C_{AZ\ GND}$	14	18	**Auto Zero Capacitor Ground (Reference Node).** A capacitor of 0.1μF (±20%) should be connected between this pin and C_{AZ} for coder auto zero operation. The sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
IN +, IN-	15,16	19,20	**In Positive and Negative (Analog Voltage Inputs).** These are the differential inputs of a high input impedance op amp whose output is connected to the V_{IN} pin. These three pins allow the user complete control over the input stage so that it can be connected as a fixed gain amplifier, as an amplifier with adjustable gain, or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel.
V_{IN}	17	21	**Input Voltage (Analog High-impedance Voltage Output).** This is the output of a high input impedance op amp whose differential inputs are the IN + and IN- pins. This node feeds the rest of the analog input section.
PDB	18	22	**Power Down Bar (Digital Input with Pull-up).** This TTL compatible input, when held low, puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
FLT OUT	19	23	**Filter Out (Analog High-impedance Voltage Output).** This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 20kΩ.
OUT-	20	24	**Out Negative (Analog Voltage Input).** This is the inverting input of the uncommitted output amplifier stage, which has its non-inverting input connected internally to ground and its output connected to V_{OUT}. The signal at the FLT OUT pin can be connected to this pin to realise a low output impedance with unity, increased or reduced gain. This allows easy calibration of the receive channel. If OUT- is connected directly to V_{SS} then the op amp will be powered down, reducing power consumption by 10mW typically.
V_{OUT}	21	25	**Output Voltage (Analog Voltage Output).** This is the output of the uncommitted output amplifier stage, which has its inverting input connected to the OUT- pin and its non-inverting input connected internally to ground. The signal at the FLT OUT pin can be connected to OUT- to realise a low output impedance with unity, increased or reduced gain. This allows easy calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into a 600Ω load (see Fig.4).
V_{DD}	22	27	**Positive Supply (Power Input).** 5V.
B IN, A IN	-	1,2	**B IN and A IN (Digital Inputs with Pull-ups).** These are the TTL compatible inputs for the A and B signalling bits for transmission. The signalling bits are sent in the bit 8 position of the PCM word in the frame following the frame in which the T-A/B SEL input makes a transition.
B OUT,A OUT	-	9,10	**B OUT and A OUT (Digital CMOS Outputs).** These are the outputs for the received A and B signalling bits. The signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which the Receive A/B select (R-A/B SEL) input makes a transition. A-bits are latched on a positive transition and B-bits are latched on a negative transition.

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
R-A/B SEL	-	12	**Receive A or B Select (Digital Input with Pull-up).** This is the TTL compatible input which causes A and B signalling bits to b at the A OUT and B OUT pins. The signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which this input makes a transition. A-bits are latched on a positive transition and B-bits are latched on a negative transition. A common select input can be used for all channels in a multiplex operation.
T-A/B SEL	-	26	**Transmit A or B Select (Digital Input with Pull-up).** This is the TTL compatible input which causes the transmission of A and B signalling bits input at the A IN and B IN pins. The signalling bits are sent in the bit 8 position of the PCM word in the frame following the frame in which the T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronised to the T STROBE input in each device.

ELECTRICAL CHARACTERISTICS

Test conditions - Voltages are with respect to digital ground (V_{DGND})

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Digital supply voltage	V_{DD}	4.75	5	5.25	V
Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V
Analog ground voltage	V_{AGND}	-0.1	0	0.1	V
Ambient temperature	V_{AMB}	0		70	°C
Input low voltage - digital inputs	V_{IL}	0	0.4	0.8	V
Input high voltage - digital inputs	V_{IH}	2.0	2.4	V_{DD}	V
System clock frequency					
CLK SEL tied to V_{DD}	f_S	2047.90	2048	2048.10	kHz
CLK SEL tied to D GND		255.99	256	256.01	
CLK SEL tied to V_{SS}		1549.92	1544	1544.08	
Capacitive loading - digital outputs	C_{LD}	0		100	pF
Pull-up resistance for PCM OUT pin	R_{PU}	510			Ω
Analog input voltage	V_{IA}	V_{AGND} -3.1		V_{AGND} +3.1	V
Capacitive loading - analog outputs	C_{LA}			50	pF
Resistive loading - V_{OUT} pin	R_{VOUT}	1200			Ω
Resistive loading - V_{IN} pin	R_{VIN}	10			kΩ
Resistive loading - FLT OUT pin	$R_{RLT\ OUT}$	20			kΩ

Power Supply Requirements - V_{DD} = 5V, V_{SS} = -5V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation - normal	P_N		80	110	mW	Unloaded
Power dissipation - without output amp.	P_{WA}		70		mW	Unloaded
Power dissipation - standby	P_S		10	20	mW	Unloaded

Static Characteristics - Voltages are with respect to digital ground (V_{DGND})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Pin capacitance	C_{PIN}		7	15	pF	
Input leakage current	I_{IL}			1	μA	$0 < V < V_{DD}$
Input source current - inputs with pull-ups	I_{IS}			600	μA	$0 < V < V_{DD}$
Output high voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} (Source) = 40μA
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 1.6mA
Output leakage current	I_{OL}			10	μA	$0 < V < V_{DD}$
Analog input resistance	R_{IA}	100			kΩ	
Analog output voltage	V_{OA}	V_{AGND} -3.1		V_{AGND} +3.1	V	

Digital Switching Characteristics - System Clock (see Fig.7)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
System clock rise time	t_{SR}		50		ns	
System clock high period	t_{SH}	0.4/fs		0.6/fs	s	
System clock fall time	t_{SF}		50		ns	
System clock low period	t_{SL}	0.4/fs		0.6/fs	s	

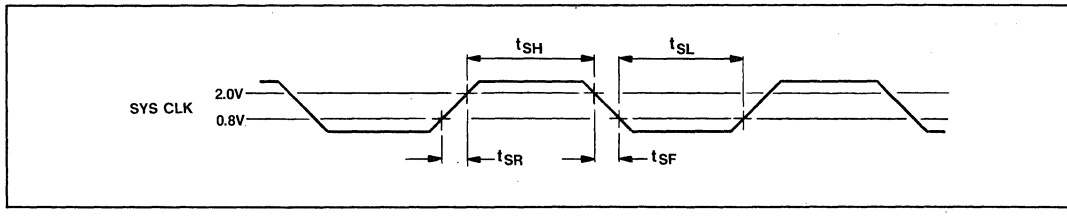


Fig.7 Timing - system clock

Digital Switching Characteristics - Receive Strobe and Clock (see Figs. 8 and 9)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Receive strobe frequency	f_{RS}	7.99996	8	8.00004	kHz	Phase-locked with system clock
Receive strobe falling set-up time	t_{RSFS}	120			ns	
Receive strobe early jitter	t_{RSEJ}			200	ns	
Receive strobe late jitter	t_{RSLJ}			100	ns	
Receive strobe falling hold time	t_{RSFH}	220			ns	
Receive clock frequency	f_{RC}	63.9997		2048.01	kHz	Phase-locked with receive strobe
Receive clock rise time	t_{RCR}			100	ns	
Receive clock high period	t_{RCH}	0.4/f_{RC}		0.6/f_{RC}	s	
Receive clock fall time	t_{RCF}			100	ns	
Receive clock low period	t_{RCL}	0.4/f_{RC}		0.6/f_{RC}	s	
Receive clock early jitter	t_{RCEJ}			200	ns	
Receive clock late jitter	t_{RSLJ}			100	ns	

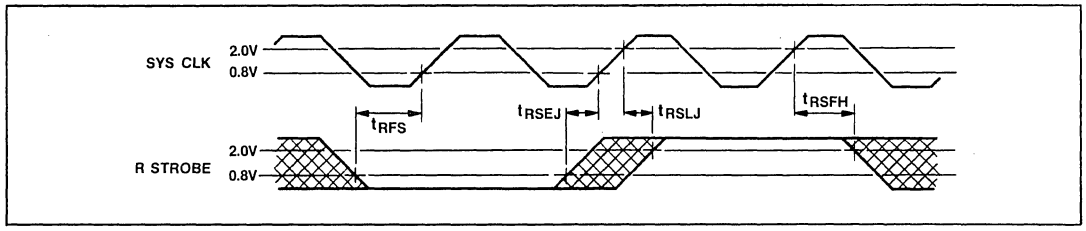


Fig.8 Timing - receive strobe

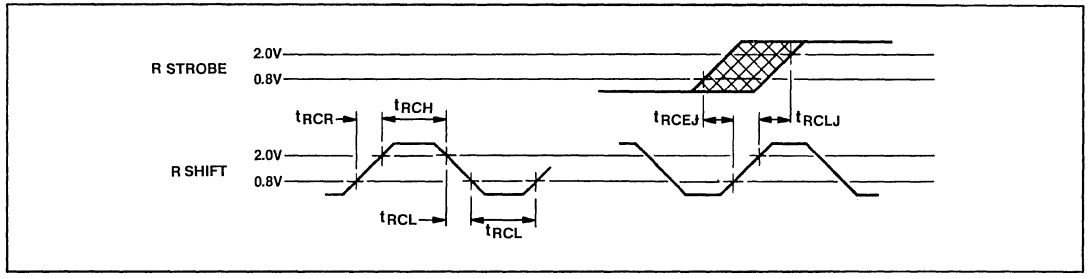


Fig.9 Timing - receive clock

Digital Switching Characteristics - Receive Data (see Fig.10)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
PCM input set-up time	t_{PIS}	60			ns	
PCM input hold time	t_{PIH}	60			ns	

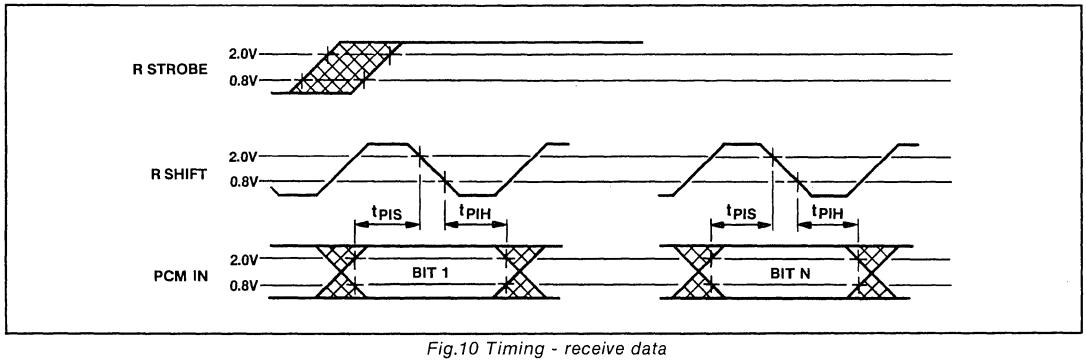


Fig.10 Timing - receive data

Digital Switching Characteristics - Transmit Strobe and Clock (see Figs.11 and 12)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Transmit strobe frequency	f_{TS}	7.99996	8	8.00004	kHz	Phase-locked with system clock
Transmit strobe falling set-up time	t_{TSFS}	120			ns	
Transmit strobe early jitter	t_{TSEJ}			200	ns	
Transmit strobe late jitter	t_{TSLJ}			100	ns	
Transmit strobe falling hold time	t_{TSFH}	220			ns	
Transmit clock frequency	f_{TC}	63.9997		2048.01	kHz	Phase-locked with transmit strobe
Transmit clock rise time	t_{TCR}			100	ns	
Transmit clock high period	t_{TCH}	$0.4/f_{TC}$		$0.6/f_{TC}$	s	
Transmit clock fall time	t_{TCF}			100	ns	
Transmit clock low period	t_{TCL}	$0.4/f_{TC}$		$0.6/f_{TC}$	s	
Transmit clock early jitter	t_{TCEJ}			200	ns	
Transmit clock late jitter	t_{TCLJ}			100	ns	

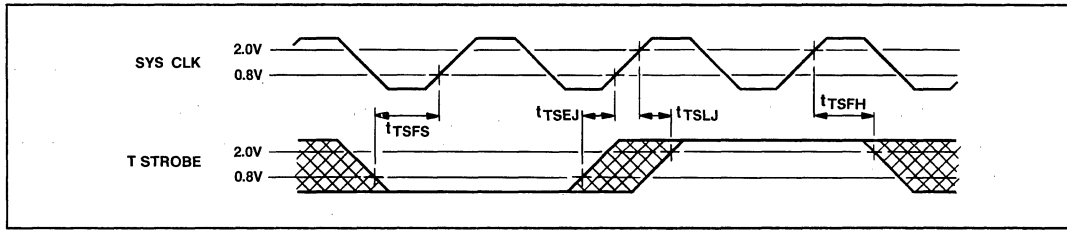


Fig.11 Timing - receive strobe

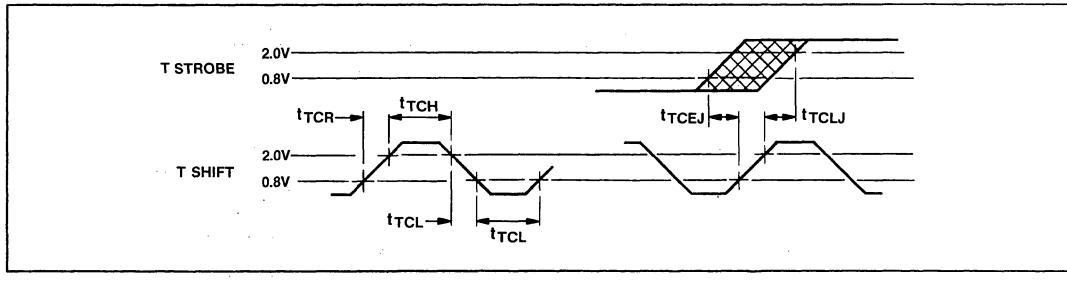


Fig.12 Timing - receive clock

Digital Switching Characteristics - Transmit Data (see Fig.13)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
PCM output holt time	t_{POH}	0	50		ns	
PCM output delay	t_{POD}		100	150	ns	

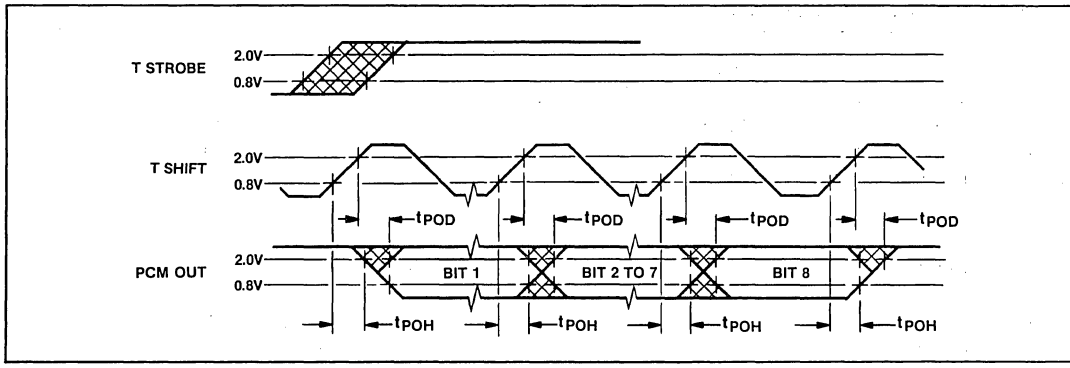


Fig.13 Timing - transmit data

Analog Channel Characteristics - Filter Delays

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Transmit filter delay	t_{TFD}			182	μs	1kHz
Receive filter delay	t_{RFD}			110	μs	1kHz

Analog Channel Characteristics - A-Law

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
0dBm0 level (see Note 2)	0dBm0	5.3	5.8	6.3	dBm	±5V, 25°C
Variation in 0dBm0 level	Δ_{0dBm0}	-0.3	0	0.3	dB	Over test conditions
Weighted idle channel noise	ICN_W		-85	-73	dBm0p	CCITT G.712, §5.1 (see Note 3)
Single frequency idle channel noise	ICN_{SF}			-60	dBm0	CCITT G.712, §5.2
Weighted receive idle channel noise	ICN_{WR}			-78	dBm0p	CCITT G.712, §5.3
Spurious out-band noise	N_{SOB}			-30	dBm0	CCITT G.712, §7.1
Spurious in-band noise	N_{SIB}			-40	dBm0	CCITT G.712, §10
Two tone interdemodulation	IMD_{2T}			-35	dBm0	CCITT G.712, §8.1
Tone + power inter-demodulation	IMD_{TP}			-49	dBm0	CCITT G.712, §8.2
Crosstalk attenuation between V_{IN} and V_{OUT}	A_X	75	80		dB	CCITT G.712, §12

Analog Channel Characteristics - μ-Law

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
0dBm0 level (see Note 2)	0dBm0	5.3	5.8	6.3	dBm	±5V, 25°C
Variation in 0dBm0 level	Δ_{dBm0}	-0.3	0	0.3	dB	Over test conditions
Weighted idle channel noise	ICN_W		5	17	dBrnc0	AT&T D3 (see Note 3)
Single frequency idle channel noise	ICN_{SF}			-60	dBm0	AT&T D3
Weighted receive idle channel noise	ICN_{WR}			15	dBrnc0	AT&T D3
Spurious out-band noise	N_{SOB}			-28	dBm0	AT&T D3
Spurious in-band noise	N_{SIB}			-40	dBm0	AT&T D3
Two tone interdemodulation	IMD_{2T}			-35	dBm0	AT&T D3
Tone + power inter-demodulation	IMD_{TP}			-49	dBm0	AT&T D3
Crosstalk attenuation between V_{IN} and V_{OUT}	A_X	75	80		dB	AT&T D3

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The typical 0dBm0 level of 5.8dBm corresponds to an RMS voltage of 1.51V and a maximum coding level of 3.1V.
3. The maximum value reduces to -68dBm0p without squelch (MV3508 with TST/SE pin unconnected).
4. The maximum value reduces to 22dBrnc0 without squelch (MV3509 with TST/SE pin unconnected).

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage.
Functional operation under these conditions is not implied.

Positive supply voltage V_{DD}	-0.5V to +6.0V	Voltage at digital or analog pins V_P	V_{SS} -0.3V to V_{DD} +0.3V
Analog ground V_{AGND}	-0.1V to +0.1V	Package power dissipation P	1000mW
Negative supply voltage V_{SS}	-6.0V to +0.5V		
Storage temperature Ts	-65°C to +150°C		

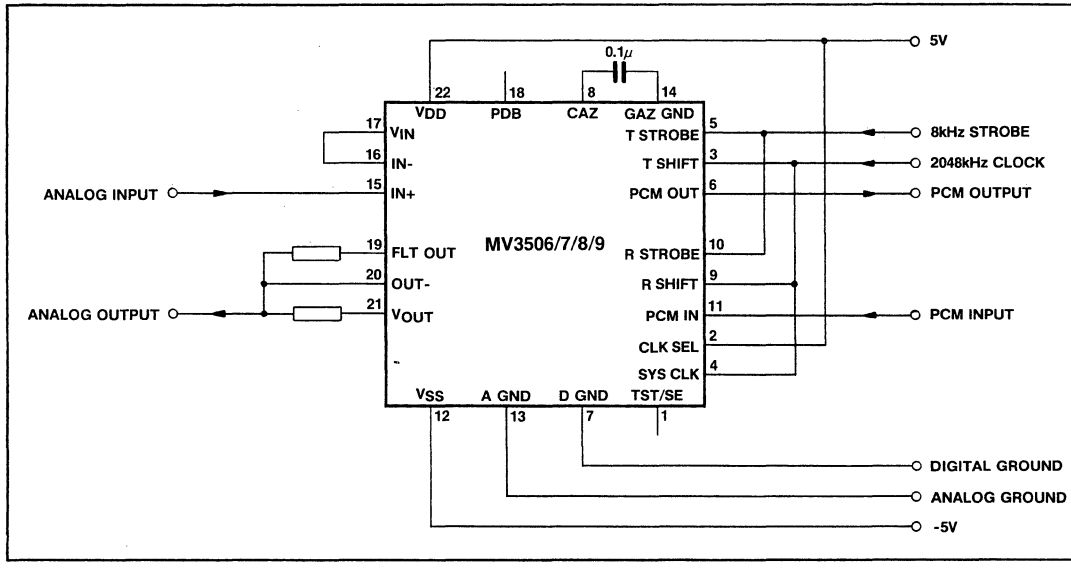


Fig.14 Simple application circuit

MV4320

KEYPAD PULSE DIALLER

The MV4320 series is fabricated using ISO-CMOS high density technology. The device is a pin-for-pin replacement for the DF320 Loop Disconnect Dialler and offers wider operating supply voltage range and lower power dissipation. The MV4320 accepts up to 20 digits from a standard 2 of 7 keypad and offers a REDIAL option activated by key #. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialling sequence. Outpulsing mark/space ratio and dialling speed are pin selectable.

The MV4320 is available in Ceramic DIL (DG, -40° C to +85° C).

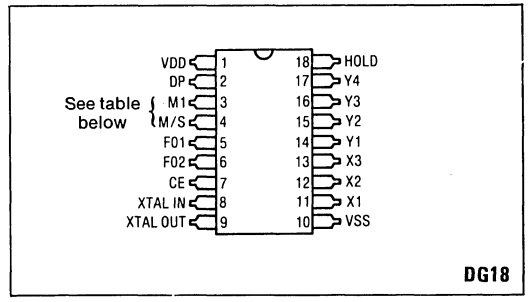


Fig.1 Pin connections (top view)

FEATURES

- Pin for Pin Replacement for the DF320
- 2.5V to 5.5V Supply Voltage Operating Range
- 375μW Dynamic Power Dissipation at 3V
- Uses Inexpensive 3.58 MHz Ceramic Resonator or Crystal
- Stores up to 20 Digits
- Selectable Outpulsing Mark/Space Ratio
- Selectable Dialling Speeds of 10, 16, 20 and 932 Hz
- Low Cost

APPLICATIONS

- Pushbutton Telephones
- Tone to Pulse Converters
- Mobile Telephone
- Repertory Dialers

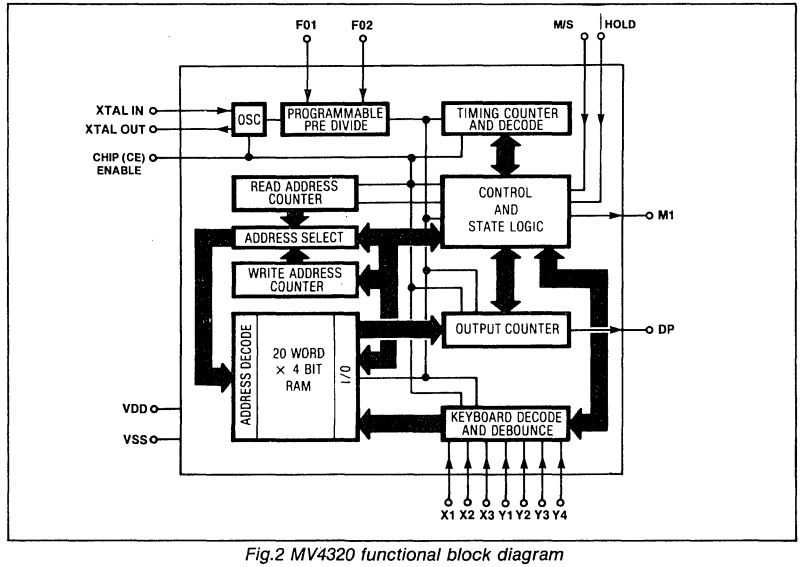


Fig.2 MV4320 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DD} = 3.0V$; $T_{amb} = +25°C$; $f_{CLK} = 3.579545MHz$
All voltages wrt V_{SS}

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	µA	$CE = V_{SS}$	
3		Operating Supply Current		I_{DD}		125	200	µA	3.579545 MHz Crystal, $C_{XTALOUT} = 12pF$	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-12.0	µA	$V_{IN} = V_{SS}$	X_1,X_2,X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1,Y_2,Y_3,Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S,IDP,F01,
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	12.0	µA	$V_{IN} = V_{DD}$	F02,FD,HOLD
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	$V_{OUT} = 2.3V$	DP, M1/M2
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	$V_{OUT} = 0.7V$	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DD} = 3.0V$; $T_{amb} = +25°C$; $f_{CLK} = 3.579545MHz$
All voltages wrt V_{SS}

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
14	DYNAMIC	Output Rise Time	t_R		1.0		us	DP,M_1.
15		Output Fall Time	t_F		1.0		us	$C_L = 50pF$
16		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
17		Mark to Space Ratio	M/S		2:1			Note 1
18					3:2			
19		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
20					16			
21					20			
22					932			
23		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
24		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. See Pin Function, Table 1.

OPERATING NOTES

The first key entered in any dialling sequence initiates the oscillator by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in figures 3 and 4. Figure 3 shows use of the circuits with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialler circuit. In this mode, the pulse occurring on M1 when CE is taken high, with no keypad input, can be used to initiate the bistable latching relay. Figure 4 shows the timing diagram for the CE internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously.

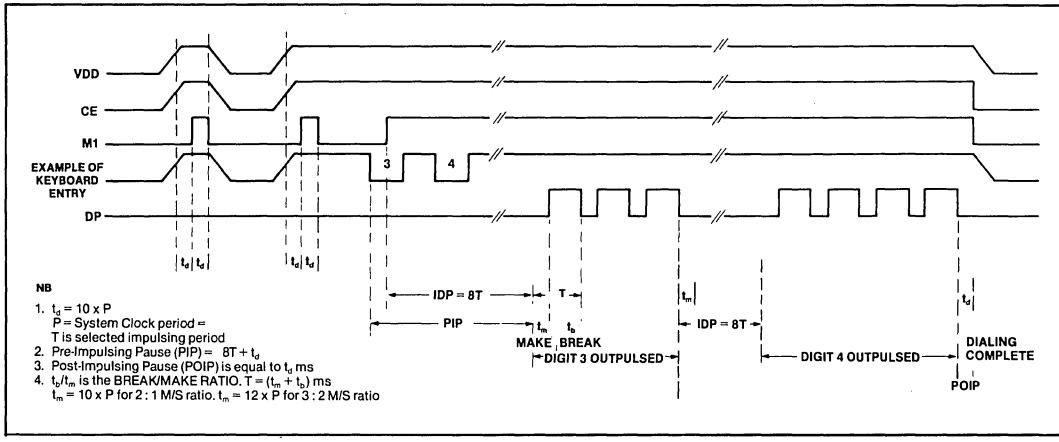


Fig.3 Keypad pulse dialer timing diagram, CE-External control

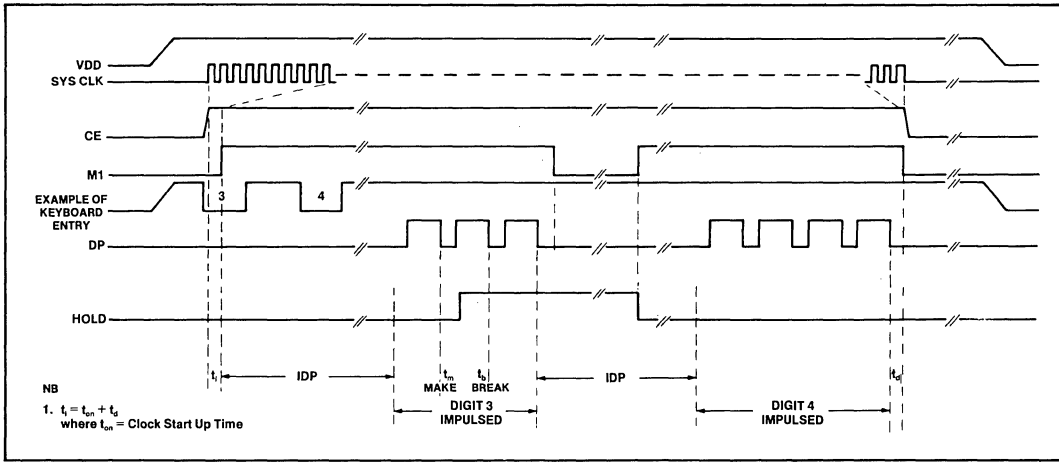


Fig.4 Keypad pulse dialer timing diagram, CE-Internal control

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN.	MAX.
V_{DD}-V_{SS}	-0.3V	10V
Voltage on any pin	V_{SS} -0.3V	V_{DD} +0.3V
Current at any pin		10mA
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C
Power Dissipation		1000mW

Derate 16mW/°C above 75°C. All leads soldered to PC board.

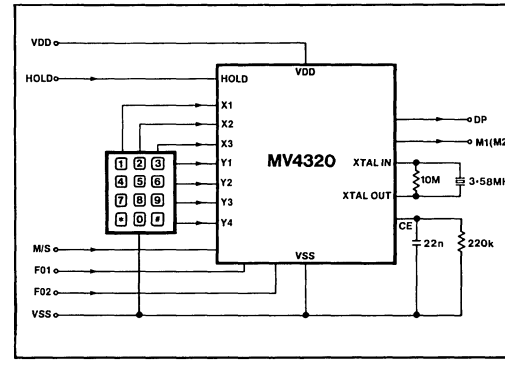


Fig.5 Application diagram

PIN FUNCTIONS

<table>
<tr><td>V_{DD}</td><td colspan="6">Positive voltage supply</td></tr>
<tr><td>DP</td><td colspan="6">Dial Pulsing Output Buffer</td></tr>
<tr><td>M1</td><td colspan="6">Mute Output (Off Normal) Buffer</td></tr>
<tr><td>M/S</td><td colspan="4">Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.
Note: O/C = Open Circuit</td><td>O/C
V_{DD}</td><td>2:1
3:2</td></tr>
<tr><td>F01,F02</td><td colspan="6">Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}.
* Assumes f_{CLK} = 3.579545MHz.
<table>
<tr><th>F01</th><th>F02</th><th>Nominal Impulsing Rate</th><th>Actual* Inpulsing Rate</th><th>System Clock frequency</th></tr>
<tr><td>O/C</td><td>O/C</td><td>10Hz</td><td>10.13Hz</td><td>303.9Hz</td></tr>
<tr><td>O/C</td><td>V_{DD}</td><td>20Hz</td><td>19.42Hz</td><td>582.6Hz</td></tr>
<tr><td>V_{DD}</td><td>O/C</td><td>932Hz</td><td>932.17Hz</td><td>27,965.1Hz</td></tr>
<tr><td>V_{DD}</td><td>V_{DD}</td><td>16Hz</td><td>15.54Hz</td><td>466.1Hz</td></tr>
</table></td></tr>
<tr><td>CE</td><td colspan="6">Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.</td></tr>
<tr><td>XTAL IN</td><td colspan="6">Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.</td></tr>
<tr><td>XTAL OUT</td><td colspan="6">Crystal Output Buffer to drive crystal.</td></tr>
<tr><td>V_{SS}</td><td colspan="6">System ground</td></tr>
<tr><td>X_1,X_2,X_3</td><td colspan="6">Column keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>Y_1,Y_2,Y_3,Y_4</td><td colspan="6">Row keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>HOLD</td><td colspan="6">O/C — Normal Operation
V_{DD} — No impulsing. If activated during impulsing, hold occurs when the current digit is complete
Prevents further impulsing. On-chip pull-down transistor to V_{SS}.</td></tr>
</table>

PLESSEY
Semiconductors

MV5087

DTMF GENERATOR

The MV5087 is fabricated using Plessey Semiconductors' ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with either a standard 2-of-8, or single contact (form A), keyboard. The keyboard entries determine the correct division of the reference frequency by the row and column counters.

D-to-A conversion, using R-2R ladder networks, results in a staircase approximation of a sinewave with low total distortion.

Frequency and amplitude stability over operating voltage and temperature range are maintained within industry DTMF specifications.

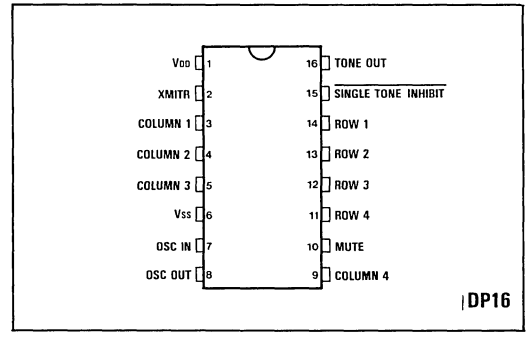


Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5087
- Low Standby Power
- Minimum External Parts Count
- 3.5V to 10V Operation
- 2-of-8 Keyboard or Calculator-Type Single Contact (Form A) Keyboard Input
- On-Chip Regulation of Output Tone
- Mute and Transmitter Drivers On-Chip
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point-of-Sale and Banking Terminals
- Process Control

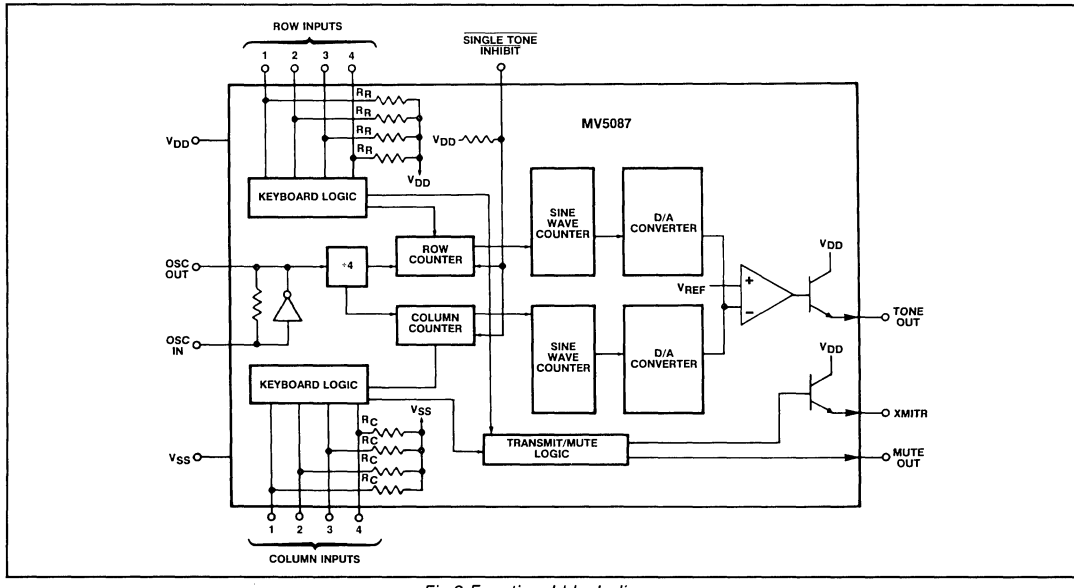


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX.		MIN.	MAX.
V_{DD} - V_{SS}	-0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} - 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	-40°C	+85°C			
Storage temperature	-65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3.5V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	3.5		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3.5V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3.5V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	SINGLE TONE INHIBIT	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
		INPUT RESISTANCE	R_{IN}		60		KΩ		
	ROW 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.9V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.3V_{DD}	V		
	COLUMN 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.1V_{DD}	V		
OUTPUTS	XMITR	SOURCE CURRENT	I_{OH}	-15	-25		mA	V_{DD} = 3.5V, V_{OH} = 2.5V	No Keyboard Entry
				-50	-100		mA	V_{DD} = 10V, V_{OH} = 8V	
		LEAKAGE CURRENT	I_{OZ}		0.1	10	uA	V_{DD} = 10V, V_{OH} = OV	Keyboard Entry
	MUTE	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3.5V, V_{OL} = 0.5V	No Keyboard Entry
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		SOURCE CURRENT	I_{OH}	-0.5			mA	V_{DD} = 3.5V, V_{OH} = 3.0V	Keyboard Entry
				-1.0			mA	V_{DD} = 10V, V_{OH} = 9.5V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3.5V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	ROW TONE OUTPUT VOLTAGE	V_{OR}	320	400	500	mV_{RMS}	Single Tone R_L = 1KΩ
	COLUMN TONE OUTPUT VOLTAGE	V_{OC}	400	500	630	mV_{RMS}	
	EXTERNAL LOAD IMPEDANCE	R_L	700			Ω	V_{DD} = 3.5V
			330			Ω	V_{DD} = 10V
OUTPUT DISTORTION					-20	dB	Total out-of-band power relative to sum of row and column fundamental power
PRE EMPHASIS, High Band			1		3	dB	
Tone Output Rise Time		t_r		3	5	ms	

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	XMITR	Emitter output of a bipolar transistor whose collector is connected to V_{DD}. With no keyboard input this output remains at V_{DD} and a keyboard input changes the output to a high impedance state. The state of Single Tone Inhibit input has no effect on XMITR output.
3,4,5,9	Column 1-4	These inputs are held at V_{SS} by resistors Rc and sense a valid logic level (approx $1/2\ V_{DD}$) when tied to a Row input.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC In, OSC Out	On-chip inverter completes the oscillator when a 3,579545 MHz crystal is connected to these pins. OSC In is the inverter input and OSC Out is the output.
10	Mute	This CMOS Output switches to V_{SS} with no keyboard input and to V_{DD} with a keyboard input. This output is unaffected by the state of Single Tone Inhibit.
11,12,13,14	Row 1-4	These inputs are held at V_{DD} by resistors R_R and sense a valid logic level (Approx $1/2\ V_{DD}$) when tied to a column input.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-up resistor to V_{DD} and when left unconnected or tied to V_{DD}, single or dual tones may be generated. When V_{SS} is applied dual tones only are generated and no input combinations will cause generation of a single tone.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes, and regulates the output level of, the row and column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard, single contact (form A) keyboard and electronic input. Figures 3 and 4 show these input configurations, and Fig. 5 shows the internal structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed. Single tones are generated when more than one button is pushed in any row or column. No tones are generated when diagonally-positioned buttons are simultaneously pressed.

An electronic input to a single column generates that single column tone. Inputs to multiple columns generates no tone. An electronic input to a single row generates no tone and a single row tone may be generated only by activating 2 columns and the desired row.

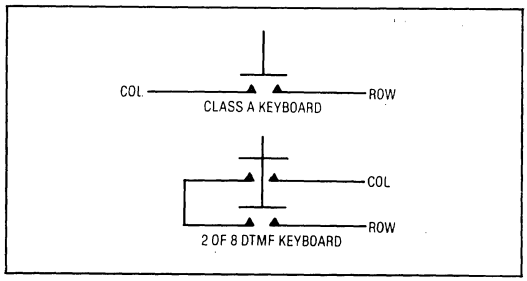


Fig.3 Keyboard configuration

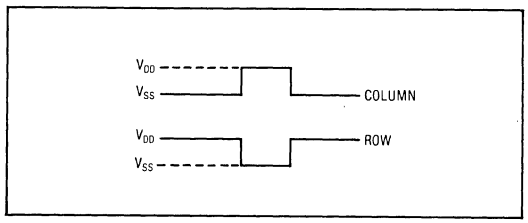


Fig.4 Electronic input

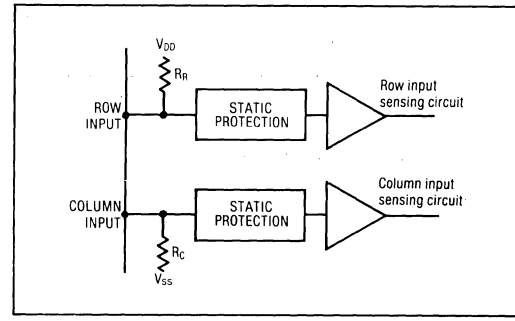


Fig.5 Row and column inputs

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6), resulting in a 'staircase' approximation to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

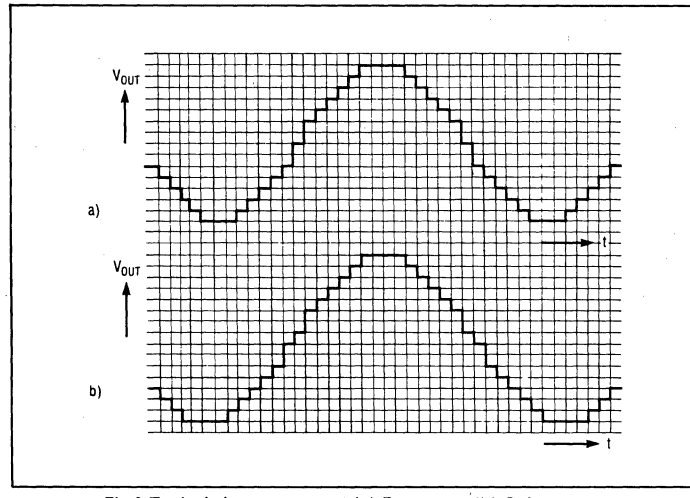


Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \text{----} V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \text{--} V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \text{---} V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
V_{2R} – V_{nR} are the Fourier component amplitudes of the row frequencies
V_{2C} – V_{nC} are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

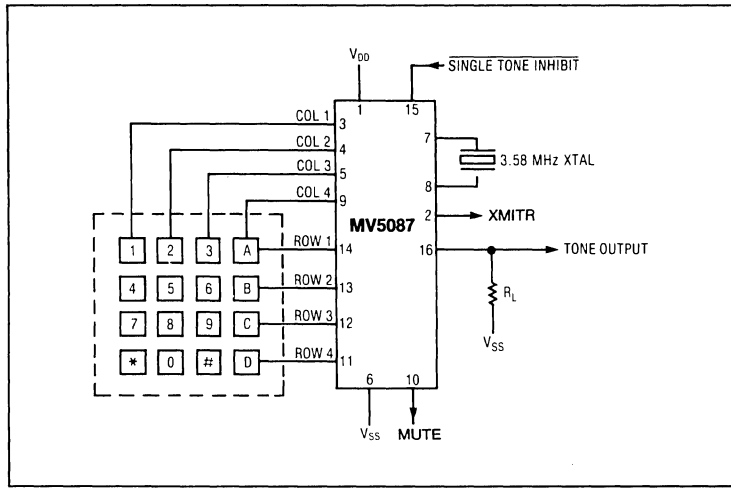


Fig.7 Connection diagram

MV5089

DTMF GENERATOR

The MV5089 is fabricated using Plessey Semiconductors' ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with a standard 2-of-8 active-low keyboard and the keyboard entries determine the correct division of the reference frequency by the row and column counters. D-to-A conversion, using R-2R ladder networks, results in a 'staircase' approximation of a sinewave with low total distortion.

Frequency stability over operating voltage and temperature range are maintained within industry DTMF standards.

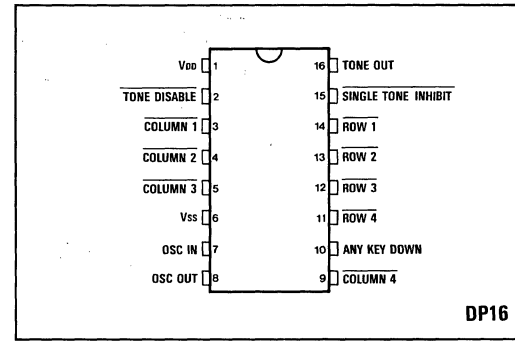


Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5089
- Low Standby Power
- Minimum External Parts Count
- 2.75V to 10V Operation
- 2-of-8 Keyboard Input
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point of Sale and Banking Terminals
- Process Control

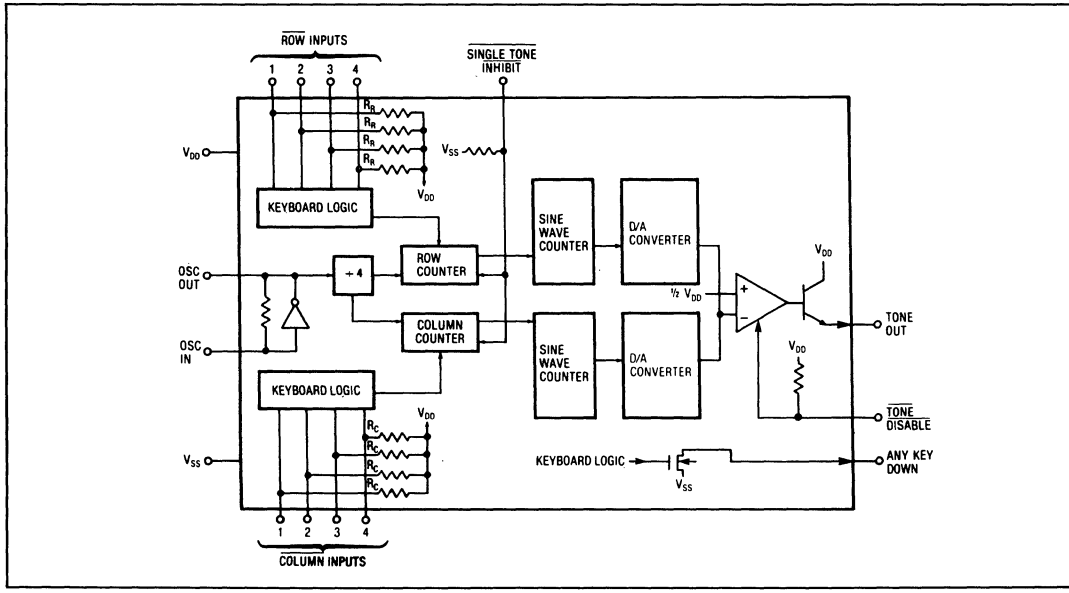


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX.		MIN.	MAX.
$V_{DD} - V_{SS}$	-0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} - 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	-40°C	+85°C			
Storage temperature	-65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	2.75		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	SINGLE TONE INHIBIT.	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
	TONE DISABLE	INPUT RESISTANCE	R_{IN}		60		KΩ		
	ROW 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
	COLUMN 1-4	INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
OUTPUTS	ANY KEY DOWN	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3V, V_{OL} = 0.5V	
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		LEAKAGE CURRENT	I_{OZ}		1		uA	V_{DD} = 3V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	OUTPUT LEVEL, ROW	V_{OUT}	-10	– 8	-7	dBm	V_{DD} = 3V. Single Tone. R_L = 100KΩ
PRE EMPHASIS, High Band			2.4	2.7	3.0	dB	
OUTPUT DISTORTION (Dual Tone)					– 20	dB	Total out-of-band power relative to sum of row and column fundamental power
Tone Output Rise Time		t_r		3	5	ms	Time for waveform to reach 90% of magnitude of either frequency from initial key stroke

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	$\overline{\text{TONE DISABLE}}$	This input has an internal pull-up resistor to V_{DD}. When connected to V_{SS} no tones are generated by any key depression allowing the keyboard to be used for purposes other than DTMF signalling.
3,4,5,9	$\overline{\text{COLUMN 1-4}}$	These CMOS inputs are held at V_{DD} by an internal pull-up resistor and are activated by the application of V_{SS}.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC IN, OSC OUT	On-chip inverter completes the oscillator when a 3,58 MHz Crystal is connected to these pins. OSC IN is the inverter input and OSC OUT is the output.
10	Any Key Down	This is an NMOS transistor output which switches to V_{SS} while any key is depressed. Otherwise this output is high impedance. Switching is independent of Tone Disable and Single Tone Inhibit.
11,12,13,14	$\overline{\text{Row 1-4}}$	As $\overline{\text{Column 1-4}}$ inputs.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-down resistor to V_{SS}. When left unconnected or tied to V_{SS}, dual tones may be generated, but keyboard input combinations resulting in single tone generation are inhibited. When V_{DD} is applied single or dual tones may be generated.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes the Row and Column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard or with an electronic input. Figures 3 and 4 show these input configurations and Fig.5 shows the internal chip structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed.

With Single Tone Inhibit at V_{DD}, connection of V_{SS} to a single column causes the generation of that Column tone. Connection of V_{SS} to more than one Column will result in no Column tones being generated. Connection of V_{SS} to Rows only generates no tone - a Column must be connected to V_{SS}.

A single Row tone only may be generated by connecting 2 columns, and the desired row, to V_{SS}.

OUTPUT TONE LEVEL

The output tone level of the MV5089 is proportional to the applied DC supply voltage.

A regulated supply will normally be used which may be designed to provide stability over the temperature range.

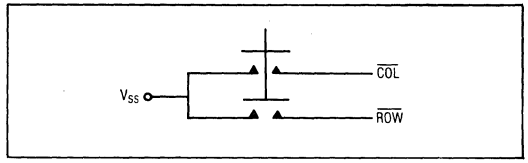


Fig.3 2 of 8 DTMF keyboard

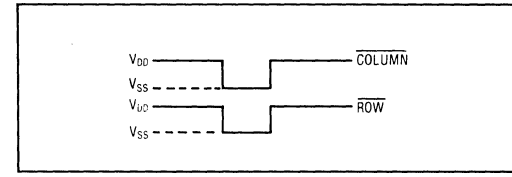


Fig.4 Electronic input

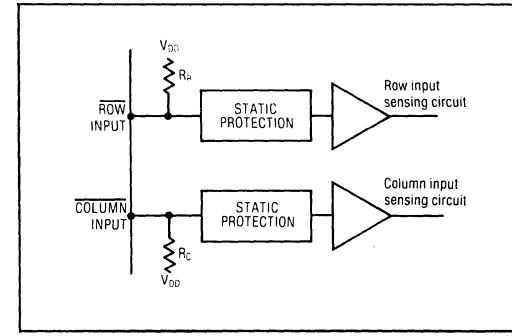


Fig.5 Row and Column inputs

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6) resulting in staircase approximations to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	−0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	−0.32	
	f_7	1477	1471.9	−0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

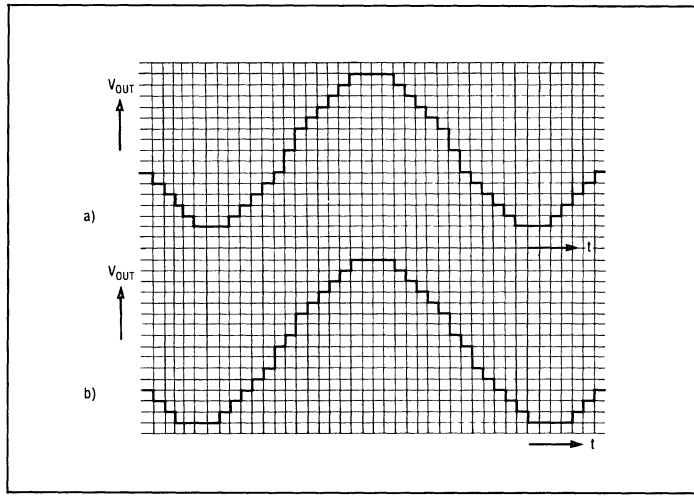


Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \cdots V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \cdots V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \cdots V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
V_{2R} -- V_{nR} are the Fourier component amplitudes of the row frequencies
V_{2C} -- V_{nC} are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

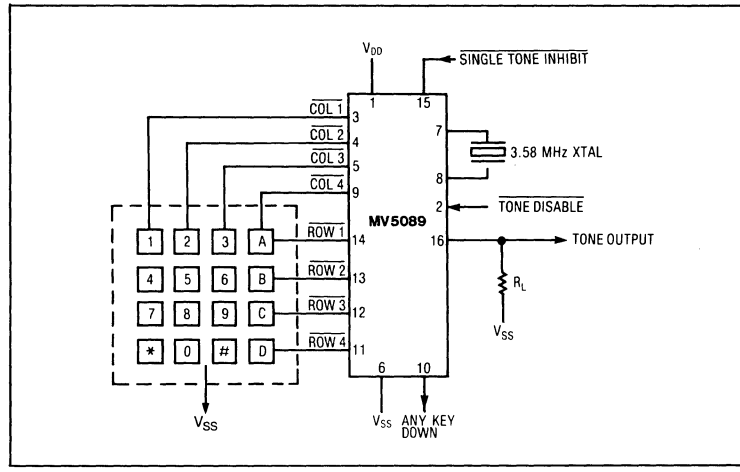


Fig.7 connection diagram

MV6001

HDLC/DMA CONTROLLER

The MV6001 is a combined HDLC transceiver and DMA controller capable of providing serial communications at rates up to 128K bits/second, and handling direct memory access clock rates up to 8MHz.

FEATURES

- Data Rates up to 128K Bits/s
- DMA Rate up to 8MHz
- Low Power CMOS
- Simple Interfacing to Popular 8-Bit Processors
- Frame Length up to 2K Bytes
- Low Host-Processor Overhead
- Conforms to ECMA40 and Related Standards (CCITT X.25, X.75, 1.440, ISO3309, ANSI X3.66, FED-STD 1003, FIPS71)

APPLICATIONS

- ISDN Terminals
- LANs
- X25 p.s.s. Networks

ORDERING INFORMATION

MV6001 B0 DP (Commercial Plastic DIP)
MV6001 B0 DG (Commercial Ceramic DIP)

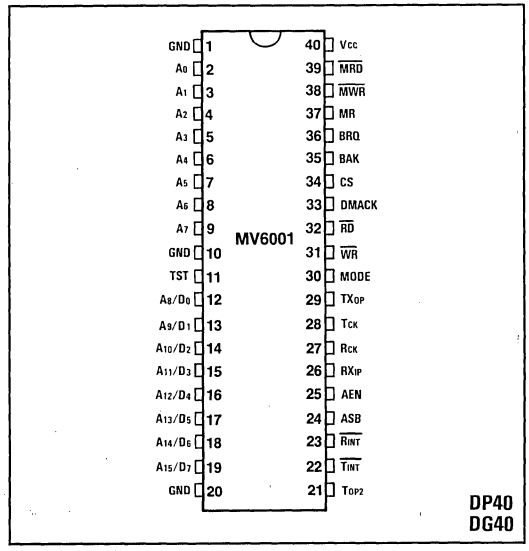


Fig.1 Pin connections - top view

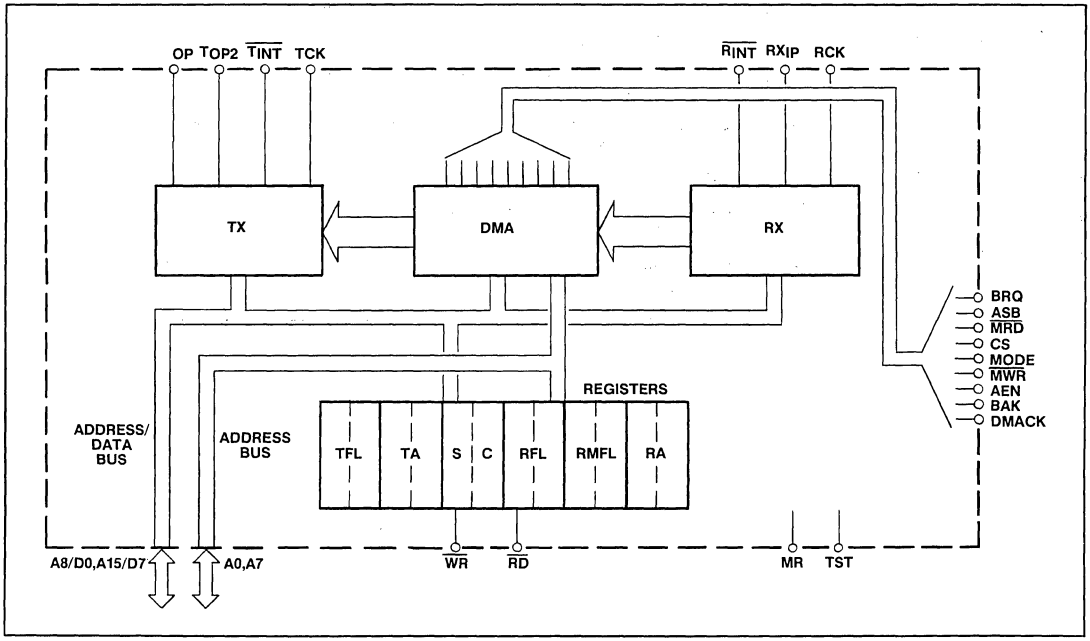
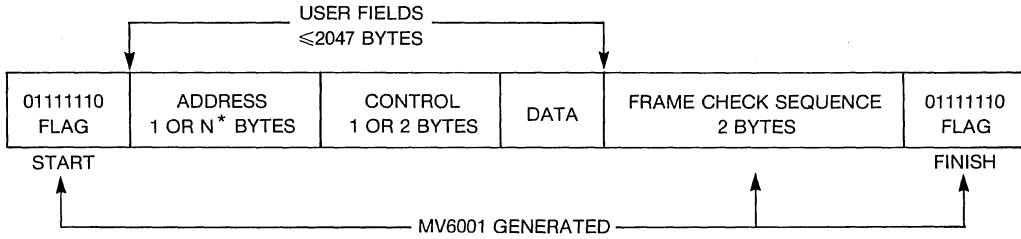


Fig.2 Block diagram

PIN DESCRIPTION

Pin No.	Name	I/O	Function
1,10,20	GND		**0V supply.** All 3 pins must be connected.
2 - 9	A_0 - A_7	I/O	**Address Bus.** Output for memory A_0 - A_7 addressing. Input for register addresses A_0 - A_3.
11	TST	I	**Test Enable.** Tie to GND for normal operation.
12 - 19	A_8/D_0 - A_{15}/D_7	I/O	**Data Bus/High Order Address.** Multiplexed data and address bus.
21	T_{OP2}	O	**Transmitter Out.** Alternative output to TX_{OP}. This output is not affected by loop back (see Operating Notes - LOOPBACK).
22	$\overline{T_{INT}}$	O	**Transmitter Interrupt.** An interrupt is generated whenever transmission of a frame is ended, either following the last FCS byte of a complete frame of when an abort sequence is transmitted. The interrupt is reset by the control register.
23	$\overline{R_{INT}}$	O	**Receiver Interrupt.** An interrupt is generated whenever a frame is received. The interrupt is reset by the counter register.
24	ASB	O	**Address Strobe.** Strobes the Address High byte from the Data/Address Bus into an external latch.
25	AEN	O	**Address Enable.** Enables the external address latch.
26	RX_{IP}	I	**Receiver Input.** Serial HDLC data input, clocked in by RCK.
27	RCK	I	**Receiver Data Clock.** Provides clock to the receiver section, frequency should be at the required data rate, this need not necessarily the the same as the transmit data rate.
28	TCK	I	**Transmitter Data Clock.** This input provides a clock signal for the transmitter section and should be set to the desired transmit data rate.
29	TX_{OP}	O	**Transmitter output.** Main transmitter output for serial data.
30	MODE	I	**Bus Control Mode Select.** Controls the polarity of BAK and BRQ. MODE = V_{CC} gives active LOW, MODE = GND gives active HIGH.
31	$\overline{WR}$	I	**Write Register.** Loads data from data bus into register addressed by A_0 - A_3.
32	$\overline{RD}$	I	**Read Register.** Reads addressed register onto data bus.
33	DMACK	I	**DMA Clock.** This input provides clock to the DMA section. The DMA clock rate should be at least ten times the sum of the transmit and receive data rates.
34	CS	I	**Chip Select.** Enables $\overline{RD}$ and $\overline{WR}$ inputs.
35	BAK	I	**Bus Acknowledge.** Input from processor relinquishing control of bus. See pin 30, Bus Mode Select.
36	BRQ	O	**Bus Request.** Output to processor requesting the bus for a DMA cycle. See pin 30, Bus Mode Select.
37	MR	I	**Master Reset.** Resets everything.
38	$\overline{MWR}$	O	**Memory Write.** This is a three-state output to write data into memory during DMA cycles.
39	$\overline{MRD}$	O	**Memory Read.** 3-state output to read data from memory during DMA cycles.
40	V_{CC}		+5V ± 10% supply.

HDLC FRAME CONSTRUCTION



*N is any integer

Fig.3

Fig.3 shows the construction of an HDLC frame. The start and finish of the frame are determined by FLAGS (the binary pattern 01111110). To prevent spurious recognition of flags in the user fields, the transmitter automatically inserts a '0' after five successive '1's. The inserted '0's are removed by the receiver, and hence are not seen by the user. Each HDLC frame contains a 2 byte frame check sequence produced by a cyclic redundancy generator in the transmitter. This sequence is checked by the receiver to validate the frame.

There are two other sequences which have specific meanings - IDLE and ABORT. The IDLE state is the transmission of at least 15 continuous '1's without inserted zeros. ABORT is 7 to 14 consecutive '1's without inserted zeros sandwiched between two zeros.

FUNCTIONAL DESCRIPTION

The MV6001 consists of four main sections; transmitter, receiver, DMA unit and register bank. Each of the transmitter, receiver and DMA unit have their own clocks running at the required data rates. There are no restrictions on the relative timing between transmit and receive clocks, the DMA clock rate should be greater than ten times the sum of the transmit and receive clock rates.

Transmission

In its steady state the transmitter produces a continuous stream of FLAGS until the control register is loaded with a transmit instruction. The transmitter then, at intervals, requests the DMA unit to fetch a byte of data. This is then transferred from the system memory via the data bus to the transmitter. (If the DMA unit should fail to fetch a byte of data by the time the next request arrives then an under-run will occur and the transmitter will transmit an ABORT sequence). Data is converted into a serial stream with inserted zeros after five ones, and the 16-bit frame check sequence is appended at the end of each frame. As soon as the last bit of the FCS has been clocked out, the $\overline{T_{INT}}$ output goes low to inform the processor that transmission has ended.

INITIALISATION

To start transmission, two items of information are required - the start address for the data to be transmitted, and the length of the user fields are loaded into the TA and TFL registers respectively, after which the transmit enable bit (D_0) can be set at any time to start transmission. Once a transmission has been started, the only way it can by stopped is to set the abort bit (D_1). The transmitter will then transmit the abort sequence followed by flags. Transmitter reset (D_2) resets the transmitter interrupt $\overline{T_{INT}}$, clears the TA and TFL registers and bits D_0 and D_1 of the status register. Transmitter reset is disabled during a transmission.

Interrupt

A transmitter interrupt ($\overline{T_{INT}}$) is generated whenever a transmission ceases, the status register can then be read to check if the frame was aborted or not. The interrupt is reset by writing a transmitter reset to the control register. NB. The status register must be read before a transmitter reset as this will alter the contents of the status register.

Status

The transmitter has two status bits - transmitting data (D_0) and abort (D_1). The transmitting data bit should always be low after $\overline{T_{INT}}$ signifying that transmission is ended. The abort bit will be high whenever a frame is aborted either by an abort instruction to the control register, or internally due to an under-run.

Reception

The receiver accepts serial data, removes inserted zeros and checks the frame check sequence. For each byte of data received, the receiver section generates a DMA request to transfer the data to memory. If the DMA controller fails to make the transfer before the next request from the receiver, then the receiver will drop out and give a receiver interrupt with the code in the status register for overrun. If the number of bytes received reaches the number in the receive maximum frame length register the receiver will drop out and give an interrupt with the code in the status register for frame too long.

Initialisation

The RA register (2 bytes) is loaded with the address where the first received byte of data is to be stored. The RMFL register (11 bits) is loaded with the maximum number of bytes in the user fields plus 3 bytes (+2 bytes for the FCS, +1 byte because an interrupt will occur when the frame length is equal to the length set by the number in the register).

Control

The receiver has two control bits in the control register, receive enable (D_3) and receive reset (D_4). Once the RA and RMFL registers have been loaded, the receive enable bit can be set at any time to allow the receiver to receive a frame. Once set, the receive enable bit cannot be overwritten and receive reset is disabled until a frame has been received.

Receiver reset will reset the R_{INT} interrupt bit, registers RFL, RMFL, RA and bits D_2 - D_7 of the status register.

Interrupt

A receive interrupt ($\overline{R_{INT}}$) is generated whenever a frame is received. The status register can then be read to check the status of the received frame. The interrupt is reset by writing a receiver reset to the control register. Since the reset will clear the receiver bits in the status register, the register must be read before writing the reset to the control register.

Status

The receiver uses bits D_2 - D_7 of the status register (see Figs. 5 and 6). A valid frame is indicated by both 'overrun' (D_6) and 'frame too long' (D_7) bits being high. Following $\overline{R_{INT}}$ the 'free to receive' bit (D_2) should be low, indicating that a frame has been received. The abort, overrun and long frame bits will be set according to the state of the frame received. The flag (D_4) and idle (D_3) bits monitor the incoming signal continuously even when the receiver is disabled.

Frame Length Register

Having received a frame and read the status register, the received frame length can be read from the RFL register. The frame length is given as an eleven bit number and includes the 2 FCS bytes in the count. The register should be read before a receiver reset.

Loopback

Bit D_7 of the control register, the loopback bit is provided for testing purposes. When the bit is set high an internal connection is made between the transmitter output and receiver input. The main transmitter output (TX_{OP}) transmits IDLE (transmitted data is always available on T_{OP2}). The receiver is clocked from TCK. The loopback bit will respond to every write to the control register.

Direct Memory Access (Fig.11)

All data transfers to or from memory are carried out by the DMA controller. Each time it receives a request from the transmitter or receiver it will carry out one DMA cycle, i.e. only one byte is transferred at a time. Clashes between transmitter and receiver are resolved in favour of the receiver, otherwise operation is on a first come, first served basis.

Registers

Fig.7 shows the addresses for the various instruction and status registers. All registers are readable from and writable to except for S, C and RFL. The S and C registers have the same address, which one is accessed is determined by whether a read (status) or write (control) operation is carried out. Transmitter registers should not be written to when transmitting (except to ABORT a frame), likewise receiver registers should not be written to when receiving. The TA and RA registers update continuously during transmission and reception respectively, giving the next address to be read from or written to.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
LOOPBACK ENABLE	DON'T CARE	DON'T CARE	RECEIVE RESET	RECEIVE ENABLE	TRANSMIT RESET	TRANSMIT ABORT	TRANSMIT ENABLE

Fig.4 Control register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RECEIVED FRAME TOO LONG	RECEIVED OVERRUN FRAME	RECEIVED ABORT	RECEIVING FLAGS	RECEIVING IDLE	FREE TO RECEIVE	TRANS-MISSION ABORTED	TRANS-MITTING DATA
← RECEIVE BITS →						← TRANSMIT BITS →	

Fig.5 Status register

Status Register								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Condition
X	X	X	X	X	X	0	1	Currently transmitting data
X	X	X	X	X	X	0	0	Transmitter disabled, transmission COMPLETE (status read after an interrupt)
X	X	X	X	X	X	1	0	Transmitter disabled, transmission ABORTED (status read after an interrupt)
X	X	X	X	X	1	X	X	Receiver enabled, free to receive
X	X	X	0	0	X	X	X	Currently receiving data
X	X	X	0	1	X	X	X	Receiving IDLE
X	X	X	1	0	X	X	X	Receiving FLAGS
0	0	1	X	X	0	X	X	Receiver disabled, ABORTED frame received (status read after an interrupt)
0	1	0	X	X	0	X	X	Receiver disabled, OVERRUN frame received (status read after an interrupt)
1	0	0	X	X	0	X	X	Receiver disabled, TOO LONG frame received (status read after an interrupt)
1	1	0	X	X	0	X	X	Receiver disabled, VALID frame received (status read after an interrupt)

Fig.6 Status conditions

Register	Function	Length (Bits)	Address (Hex)	A_3	A_2	A_1	A_0	R/W
TFL	Transmitter Frame Length LS Byte	8	2	0	0	1	0	R/W
	Transmitter Frame Length MS Byte	3	3	0	0	1	1	R/W
TA	Transmitter Address LS Byte	8	6	0	1	1	0	R/W
	Transmitter Address MS Byte	8	7	0	1	1	1	R/W
S	Status	8	9	1	0	0	1	R
C	Control	8	9	1	0	0	1	W
RFL	Receiver Frame Length LS Byte	8	A	1	0	1	0	R
	Receiver Frame Length MS Byte	3	B	1	0	1	1	R
RMFL	Receiver Maximum Frame Length LS Byte	8	C	1	1	0	0	R/W
	Receiver Maximum Frame Length MS Byte	3	D	1	1	0	1	R/W
RA	Receiver Address LS Byte	8	E	1	1	1	0	R/W
	Receiver Address MS Byte	8	F	1	1	1	1	R/W

Fig.7 Register addresses

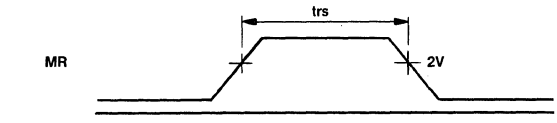


Fig.8(a)

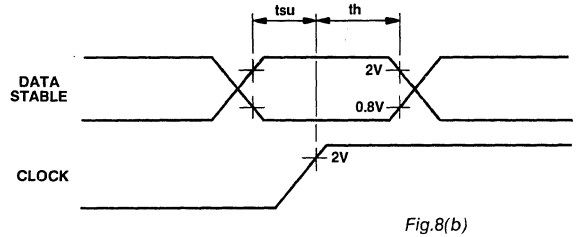


Fig.8(b)

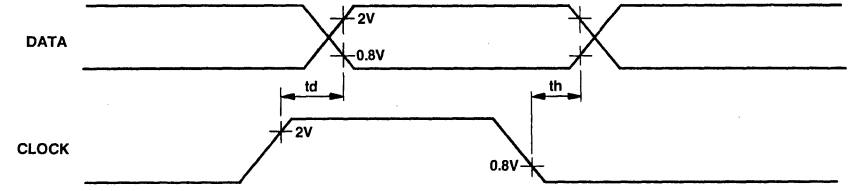


Fig.8(c)

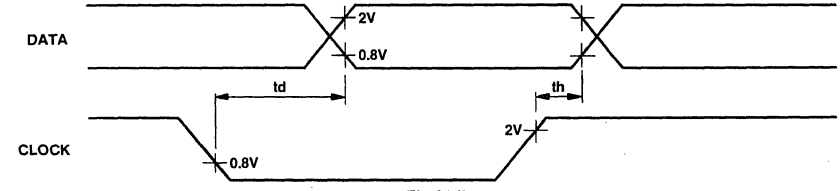


Fig.8(d)

Fig.8 Timing diagram

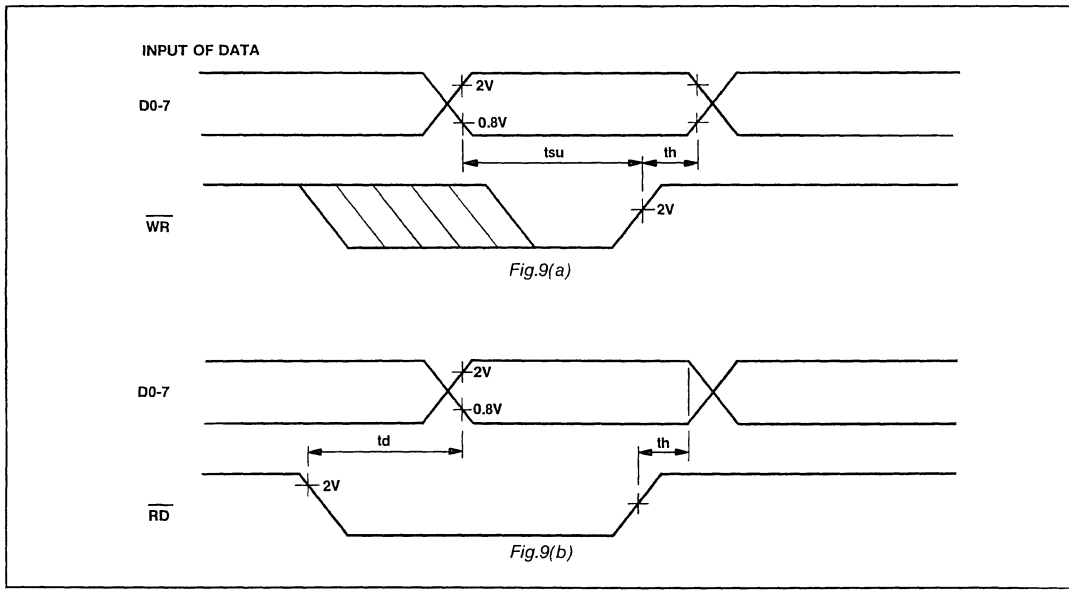


Fig.9 Register timing

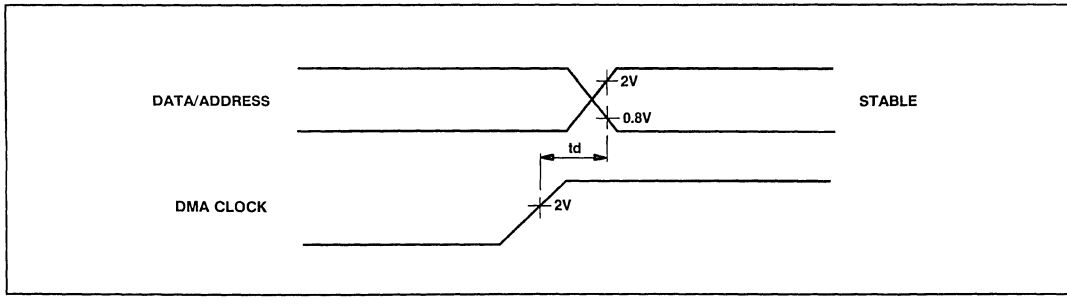


Fig.10 DMA timing

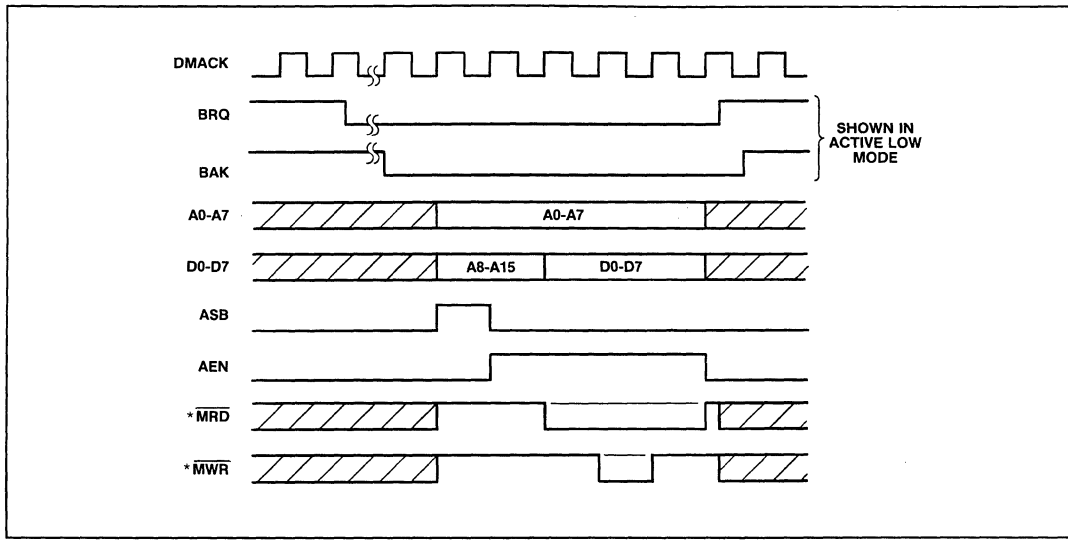


Fig.11 DMA cycle timing

* During a read cycle, $\overline{MWR}$ stays high and similarly during a write cycle $\overline{MRD}$ stays high. All other external signals are the same for both cycles.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.3V to 7.0V
Input voltage V_{IN}	-0.3V to V_{CC} +0.3V
Output voltage V_{OUT}	-0.3V to V_{CC} +0.3V
Clamp diode current per pin I_K (See Note 2)	±18mA
Static discharge voltage	
Storage temperature T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	-40°C to +85°C

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation of 1 second should not be exceeded, only one output to be tested at any one time.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Ground = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	V_{CC}-2			V	I_{OH} = 0.8mA
Output low voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input high voltage	V_{IH}	2.2			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	I_L	-10		+10	μA	GND ≤ V_{IN} ≤ V_{CC}
V_{CC} current	I_{CC}			1	mA	T_{amb} = -40°C to +85°C
Output leakage current	I_{OZ}	-50		+50	μA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	15		80	mA	V_{CC} = Max

Switching Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum DMA clock frequency	FDMACK	8			MHz	
Maximum TX clock frequency	FTCK	128			kHz	
Maximum RX clock frequency	FRCK	128			kHz	
Minimum MR duration	t_{rs}				ns	Fig.8(a)
RXIP to RCK set-up time	t_{su}	0			ns	Fig.8(b)
RXIP to RCK hold time	t_h	90			ns	Fig.8(b)
BAK to DMACK set-up time	t_{su}	0			ns	Fig.8(b)
BAK to DMACK hold time	t_h	25			ns	Fig.8(b)
Delay DMA clock to $\overline{MRD}$	t_d		40	55	ns	Fig.8(c)
Delay DMA clock to $\overline{MWR}$	t_d		40	55	ns	Fig.8(c)
Delay RCK ↓ to $\overline{RINT}$	t_d		50	110	ns	Fig.8(d)
Delay, TCK to $\overline{TINT}$	t_d		60	90	ns	Fig.8(c)
Delay, TCK ↓ or RCK ↓ to BRQ	t_d		70	90	ns	Fig.8(c) & (d)
Delay, DMACK to AEN	t_d		40	55	ns	Fig.8(c)
Delay, DMACK to ASB	t_d		40	55	ns	Fig.8(c)
Delay, TCK to TX_{OP}	t_d		70	115	ns	Fig.8(c)
Delay, TCK to T_{OP2}	t_d		60	115	ns	Fig.8(c)
Hold, DMACK to $\overline{MRD}$	t_h		90	130	ns	Fig.8(d)
Hold, DMACK to $\overline{MWR}$	t_h		50	75	ns	Fig.8(d)
Hold, DMACK to BRQ	t_h		60		ns	Fig.8(d)
Hold, DMACK to AEN	t_h		30	55	ns	Fig.8(d)
Hold, DMACK to ASB	t_h		40	55	ns	Fig.8(d)
Data to WR set-up	t_{su}				ns	Fig.9(a)
WR to data hold	t_h				ns	Fig.9(a)
RD to data delay	t_d		50		ns	Fig.9(b)
RD to data hold	t_h				ns	Fig.9(b)
DMACK to data/address delay	t_d		60		ns	Fig.10

PLESSEY
Semiconductors

MV8804

8 x 4 BIDIRECTIONAL ANALOG SWITCH ARRAY

The MV8804 is a CMOS/LSI 8 x 4 Analog Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. The circuit has digitally-controlled analog switches having very low 'ON' resistance and very low 'OFF' leakage current. The switches will operate with analog signals at frequencies up to 40MHz and up to 13.0V peak-to-peak. A 'HIGH' on the Master Reset input switches all channels 'OFF' and clears the memory. The MV8804 is ideal for crosspoint switching applications.

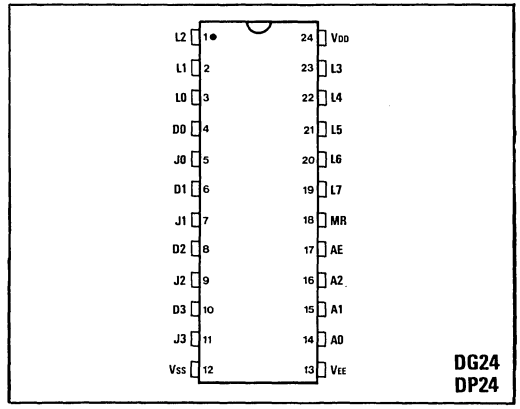


Fig.1 Pin connections - top view

FEATURES

- Microprocessor Compatible Control Inputs
- On-Chip Control Memory And Address Decoding
- Row Addressing
- Master Reset
- 32 Crosspoint Switches in 8 x 4 Array
- 5.0V to 13.0V Operation
- Low Crosstalk Between Switches
- Low On Resistance: 90Ω (typ.) At 10V
- Matched Switch Characteristics
- Switches Frequencies Up To 40MHz

APPLICATIONS

- PABX And Key Systems
- Data Acquisition Systems
- Test Equipment/Instrumentation
- Analog/Digital Multiplexers

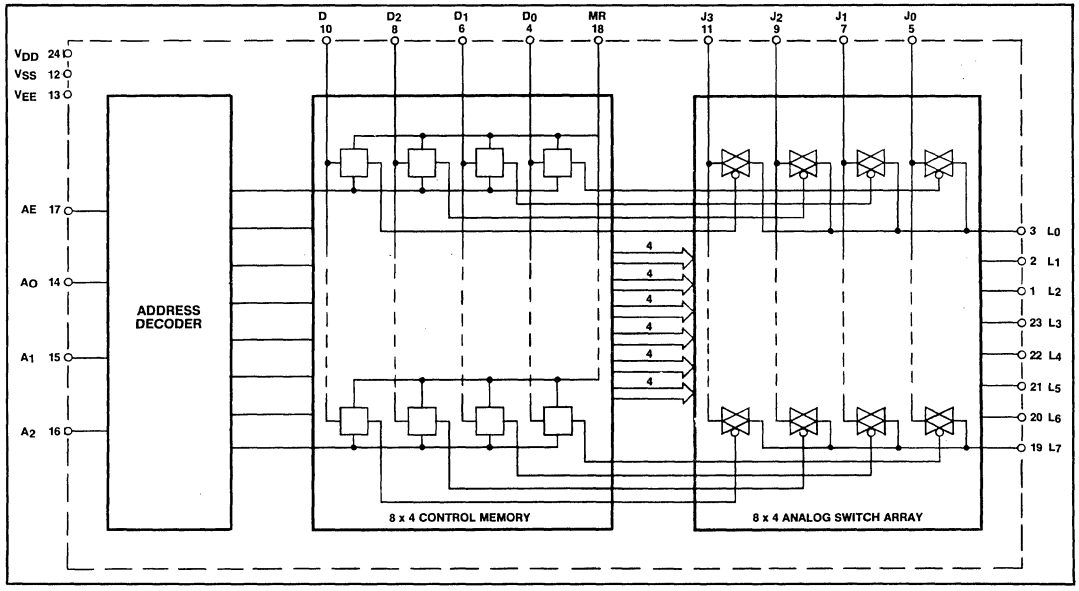


Fig.2 MV8804 functional block diagram

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

	Min.	Max.		Min.	Max.
V_{DD} - V_{SS}	-0.3V	16V	Storage temperature	-65°C	+125°C
V_{DD} - V_{EE}	-0.3V	16V	(DP package)		
V_{SS} - V_{EE}	-0.3V	16V	Power dissipation		1200mW*
Voltage on any logic pin	V_{SS} -0.3V	V_{DD} +0.3V	(DG package)		
Voltage on any line (V_L) or junctor (V_J)	V_{EE} -0.3V	V_{DD} +0.3V	Power dissipation		600mW**
Current at any logic pin		10mA	(DP package)		
Operating temperature (all packages)	-40°C	+85°C			
Storage temperature (DG package)	-65°C	+150°C			

* Derate 16mW/°C above 75°C. All leads soldered to PC board.

** Derate 6.3mW/°C above 25°C. All leads soldered to PC board.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C, V_{SS} - V_{EE} = 0V, V_{is} = 5V p-p, C_L = 50pF, R_L = 10kΩ, t_r = t_f = 20ns (input signal)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Sine wave response (distortion)			0.1		%	V_{DD} = 13V }
			0.2		%	V_{DD} = 10V } f_{in} = 1kHz
			1.0		%	V_{DD} = 5V }
Frequency response channel 'ON' (sine wave input)			40		MHz	V_C = V_{DD} = 10V, $\frac{V_o}{V_i}$ = -3dB
Feedthrough channel 'OFF'			-40		dB	V_{DD} = 10V, V_C = V_{EE}, R_L = 1kΩ, f_{in} = 1MHz
Crosstalk between any two channels			-40		dB	f_{in} = 1.0MHz } V_{DD} = 10V, Switch A
			-90		dB	f_{in} = 3.4kHz } 'ON',Switch B 'OFF'
Propagation delay Signal input to signal output	t_{PS}		10		ns	V_{DD} = 10V, Switch 'ON'
Turn 'ON' propagation delay	t_{PLH}		200		ns	V_{DD} = 10V
Data input to signal output	t_{PHL}		400		ns	V_{DD} = 5V
Address enable to signal output	t_{PAE}		300		ns	V_{DD} = 10V
			600		ns	V_{DD} = 5V
Minimum address enable (AE)	t_{AE}		90		ns	V_{DD} = 10V
Pulse width			225		ns	V_{DD} = 5V
Minimum set-up time						
Address to AE	t_s	0	50		ns	V_{DD} = 10V
		0	90		ns	V_{DD} = 5V
Data in to AE	t_s		50		ns	V_{DD} = 10V
			90		ns	V_{DD} = 5V
Minimum Hold Time	t_h		50		ns	V_{DD} = 10V
Address or data in to address enable			90		ns	V_{DD} = 5V
Memory reset time	t_{MR}		175		ns	V_{DD} = 10V, R_L = 1kΩ
Memory reset recovery time	T_{MRR}		150		ns	V_{DD} = 10V } R_L = 1kΩ
			250		ns	V_{DD} = 5V }

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C, V_{SS} = V_{EE} = 0V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range						
Digital	V_{DD} - V_{SS}	5	5	13	V	
Analog	V_{DD} - V_{EE}	5	10	13	V	
Logic level converter	V_{SS} - V_{EE}	0	5	12	V	
On state resistance	R_{ON}		75	108	Ω	V_{DD} = 13V } V_J = V_L = 0.6V
			90		Ω	V_{DD} = 10V }
			240		Ω	V_{DD} = 5V }
Difference in On state	R_{ON}		20		Ω	V_{DD} = 13V
Resistance between any switches			30		Ω	V_{DD} = 10V
Off state leakage current (any line to any junctor)	I_{OFF}		±0.01	±500	nA	V_{DD} = 13V, selected crosspoint in Off state
Input logic '0' level	V_{IL}		4.5		V	V_{DD} = 10V } V_{is} = V_{DD} through 1kΩ
			2.25	1.5	V	V_{DD} = 5V }
Input logic '1' level	V_{IH}		5.5		V	V_{DD} = 10V } V_{is} = V_{DD} through 1kΩ
		3.5	2.75		V	V_{DD} = 5V }
Quiescent device current (per package)	I_Q		0.1	500	μA	V_{DD} = 13V
Maximum current through crosspoint switch	I_{MAX}		±8.0		mA	V_{DD} = 13V
Switch input capacitance	C_{is}		5		pF	V_{DD} = 10V, V_{in} = 0V
Switch output capacitance	C_{os}		20		pF	V_{DD} = 10V, V_{in} = 0V
Feedthrough capacitance	C_{ios}		0.2		pF	V_{DD} = 10V, V_{in} = 0V
Digital input capacitance	C_{in}		5		pF	V_{DD} = 10V, V_{in} = 0V

NOTES
1. Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing.
2. Vis is the analog switch input voltage, Vin is digital input voltage.

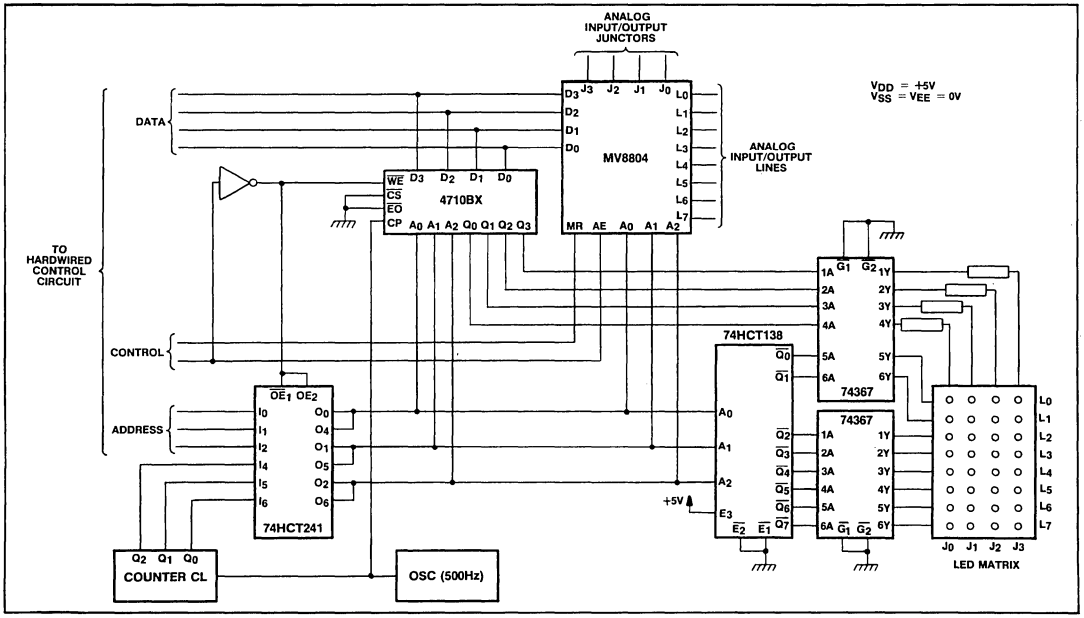


Fig.3 Visual indication of MV8804 control memory status

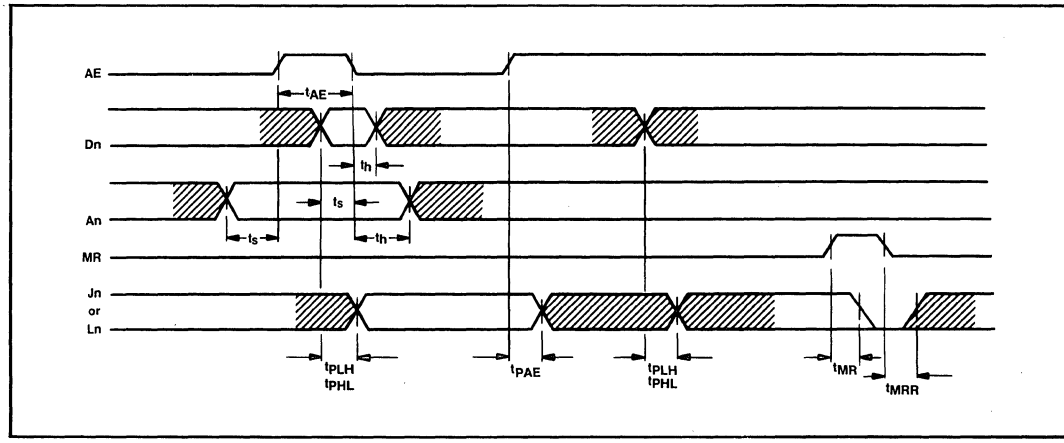


Fig.4 Timing waveforms

PIN DESCRIPTION

Pin	Name	Description
1	L_2	Analog Switch Array Input/Output Line
2	L_1	Analog Switch Array Input/Output Line
3	L_0	Analog Switch Array Input/Output Line
4	D_0	Control Memory Data Line Input
5	J_0	Analog Switch Array Input/Output Junctor
6	D_1	Control Memory Data Line Input
7	J_1	Analog Switch Array Input/Output Junctor
8	D_2	Control Memory Data Line Input
9	J_2	Analog Switch Array Input/Output Junctor
10	D_3	Control Memory Data Line Input
11	J_3	Analog Switch Input/Output Junctor
12	V_{SS}	Negative Digital Power Supply
13	V_{EE}	Negative Analog Power Supply
14	A_0	Control Memory Address Input
15	A_1	Control Memory Address Input
16	A_2	Control Memory Address Input
17	AE	Control Memory Address Enable Input (Strobe)
18	MR	Master Reset
19	L_7	Analog Switch Array Input/Output Line
20	L_6	Analog Switch Array Input/Output Line
21	L_5	Analog Switch Array Input/Output Line
22	L_4	Analog Switch Array Input/Output Line
23	L_3	Analog Switch Array Input/Output Line
24	V_{DD}	Positive Analog/Digital Power Supply

FUNCTIONAL DESCRIPTION

The analog switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as LINES (L0-L7) and the column input/outputs as JUNCTORS (J0-J3). The crosspoint analog switches interconnect the lines and junctors when turned 'ON' and provide a high degree of isolation when turned 'OFF'. Interchannel crosstalk is minimal despite the high density of the analog switch array.

The control memory of the MV8804 can be treated as an 8-word by 4-bit random access memory. The 8 words are selected by the ADDRESS (A0-A2) inputs through the on-chip address decoder. Data is presented to the memory via the 4 DATA inputs (D0-D3). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is high. A high level written into a memory cell turns the corresponding crosspoint switch 'ON' while a low level causes the crosspoint to turn 'OFF'.

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A high level on the MASTER RESET (MR) input returns all memory locations to a low level and turns all crosspoint switches 'OFF', effectively isolating the lines from the junctors. The digital logic level converters allow the digital input levels to differ from limits of the analog levels switched through the array. For example, with V_{DD} = 5V, V_{SS} = 0V and V_{EE} = -6V, the control inputs can be driven by a 5V system while the analog voltages through the crosspoint switches can swing from +5V to -6V.

LOGIC TRUTH TABLE

Master Reset	Address enable	Address			Addressed line	Input data to control memory				Junctors connected to addressed line			
MR	AE	A_2	A_1	A_0		D_3	D_2	D_1	D_0	J_3	J_2	J_1	J_0
H	X	X	X	X	All	X	X	X	X	All switches 'Off'			
L	L	X	X	X	None	X	X	X	X	No change of state			
L	H	L	L	L	L0	L	L	L	L	•	•	•	•
L	H	L	L	L	L0	L	L	L	H	•	•	•	+
L	H	L	L	L	L0	L	L	H	L	•	•	+	•
L	H	L	L	L	L0	L	L	H	H	•	•	+	+
L	H	L	L	L	L0	L	H	L	L	•	+	•	•
L	H	L	L	L	L0	L	H	L	H	•	+	•	+
L	H	L	L	L	L0	L	H	H	L	•	+	+	•
L	H	L	L	L	L0	L	H	H	H	•	+	+	+
L	H	L	L	L	L0	H	L	L	L	+	•	•	•
L	H	L	L	L	L0	H	L	L	H	+	•	•	+
L	H	L	L	L	L0	H	L	H	L	+	•	+	•
L	H	L	L	L	L0	H	L	H	H	+	•	+	+
L	H	L	L	L	L0	H	H	L	L	+	+	•	•
L	H	L	L	L	L0	H	H	L	H	+	+	•	+
L	H	L	L	L	L0	H	H	H	L	+	+	+	•
L	H	L	L	L	L0	H	H	H	H	+	+	+	+
L	H	L	L	H	L1	Each addressed line may have 16 different combinations of junctors connected to it by inputing data to the control memory as shown for L0.							
L	H	L	H	L	L2								
L	H	L	H	H	L3								
L	H	H	L	L	L4								
L	H	H	L	H	L5								
L	H	H	H	L	L6								
L	H	H	H	H	L7								

NOTES
L = Low Logic Level
H = High Logic Level
X = Don't Care Condition
+ = Indicates Connection Between Junctor and Addressed Line
• = Indicates No Connection Between Junctor and Addressed Line

8 x 8 ANALOG/DIGITAL SWITCH

Two MV8804s configured as shown in Fig.7, implement an 8 x 8 analog/digital switch. The switch capacity can be expanded to an M x N array of inputs/outputs. Expansion in the N dimension is as shown and connecting the lines (L0-L7) from the MV8804s in common.

Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MV8804 junctors (J0-J3) in common. The address and data control inputs of the MV8804s can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually, for example by a 74HCT515 programmable AND gate.

A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.

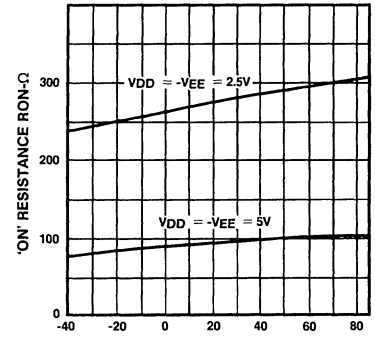


Fig.5 ON resistance vs temperature (input signal voltage = supply voltage/2)

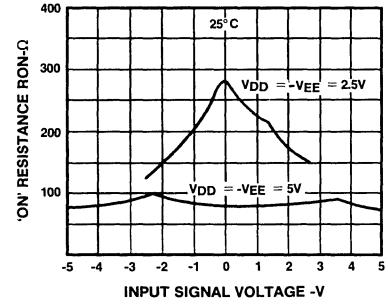


Fig.6 ON resistance vs input signal voltage

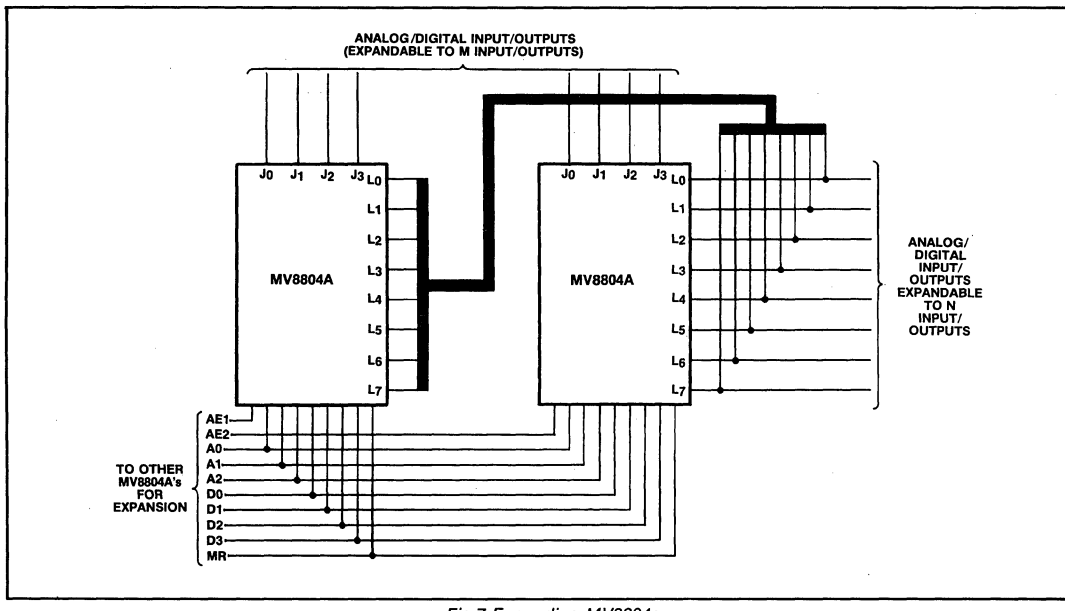


Fig.7 Expanding MV8804s

PLESSEY
Semiconductors

MV8870

DTMF RECEIVER WITH HIGH AND LOW GROUP FILTER OUTPUTS

The MV8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated on Plessey Semiconductors' double-poly CMOS technology. The filter section uses switched capacitor techniques for high- and low- group filters and dial-tone rejection; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

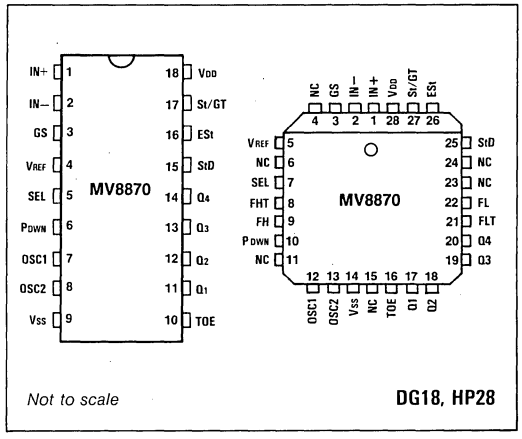


Fig.1 Pin connections (top view)

FEATURES

- Complete DTMF Receiver
- Central Office Quality
- Lower Power Consumption
- Adjustable Acquisition and Release Times

APPLICATIONS

- PABX
- Central Office
- Key Systems
- Mobile Radio
- Remote Control
- Remote Data Entry

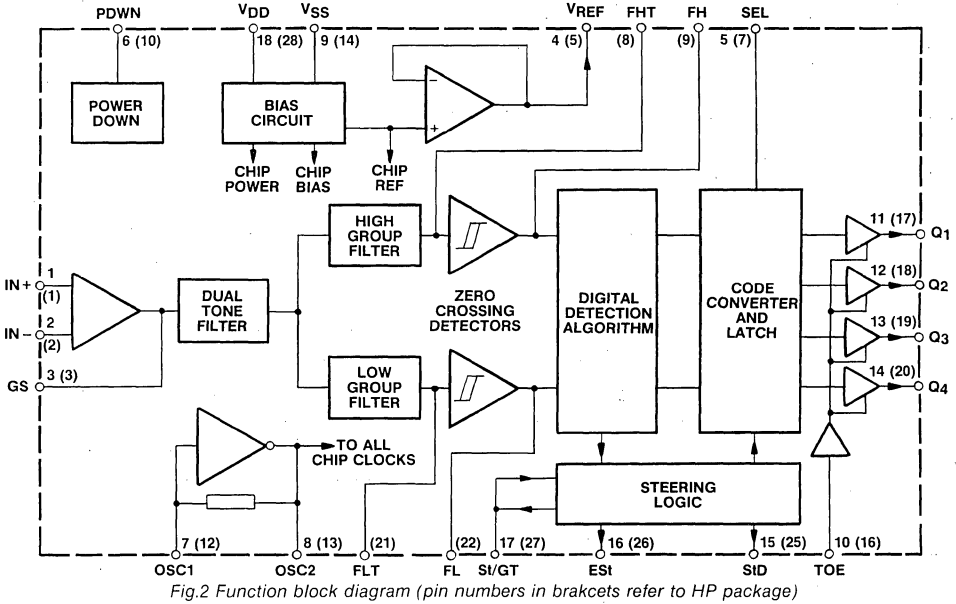


Fig.2 Function block diagram (pin numbers in brakcets refer to HP package)

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Parameter	Min.	Max.	Unit
Power supply voltage V_{DD} - V_{SS}		6	V
Voltage on any pin	V_{SS} -0.3	V_{DD} +0.3	V
Current at any pin		10	mA
Operating temperature	-40	+85	°C
Storage temperature	-65	+150	°C
Package power dissipation (Note 2)		1000	mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Derate above 75°C at 16mW/°C. All leads soldered to board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Operating supply voltage	V_{DD}	4.75		5.25	V	
Operating supply current	I_{DD}		3.0	7	mA	
Power consumption	P_O		15	35	mW	f = 3.579MHz
Low level input voltage	V_{IL}			1.5	V	
High level input voltage	V_{IH}	3.5			V	
Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
Pull up source current	I_{SO}		7.5	15.0	μA	TOE = 0V
Input impedance (IN+ & IN-)	R_{IN}		10		MΩ	At 1kHz
Steering threshold voltage	V_{TSt}	2.2	2.35	2.5	V	
Low level output voltage	V_{OL}		0.03		V	No load
High level output voltage	V_{OH}		4.97		V	No load
Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4V
Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
Output voltage (V_{REF} pin)	V_{REF}	2.4		2.7	V	No load
Output resistance (V_{REF} pin)	R_{OR}		10		kΩ	

OPERATING CHARACTERISTICS, GAIN SETTING AMPLIFIER

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input leakage current	I_{IN}		±100		nA	$V_{SS} < V_{IN} < V_{DD}$
Input resistance	R_{IN}		10		MΩ	
Input offset voltage	V_{OS}		±25		mV	
Power supply rejection	PSRR		60		dB	1kHz
Common mode rejection	CMRR		60		dB	V_{IN} = V_{REF} ±1.3V
DC open loop voltage gain	A_{VOL}		65		dB	
Open loop unity gain bandwidth	f_c		1.5		MHz	
Output voltage swing	V_O		4.5		V p-p	R_L ⩾ 100kΩ to V_{SS}
Tolerable capacitive load (GS)	C_L		100		pF	
Tolerable resistive load (GS)	R_L		50		kΩ	
Common mode range	V_{cm}		3.0		V p-p	No load

AC CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25°C, f_{CLK} = 3.579545MHz, using test circuit of Fig.3.

Characteristic		Symbol	Value			Unit	Notes
			Min.	Typ.	Max.		
Valid input signal level (each tone of composite signal)	Min.				-29	dBm	1,2,3,5,6,9
					27.5	mVRMS	1,2,3,5,6,9
	Max.		+1			dBm	1,2,3,5,6,9
			883			mVRMS	
Twist accept limit	Positive			10		dB	2,3,6,9
	Negative			10		dB	2,3,5,9
Freq. deviation accept limit					±1.5% ±2Hz	Nom.	2,3,5,9
Freq. deviation reject limit			±3.5%			Nom.	2,3,5
Third tone tolerance				-16		dB	2,3,4,5,9,10
Noise tolerance				-12		dB	2,3,4,5,7,9,10
Dial tone tolerance				+18		dB	2,3,4,5,8,9,10
Tone present detection time		t_{DP}	5	11	14	ms	Refer to Fig.5
Tone absent detection time		t_{DA}	0.5	4	8.5	ms	
Tone duration accept		t_{REC}			40	ms	(User adjustable) Refer to 'Guard Time Adjustment'
Tone duration reject		t_{REC}	20			ms	
Interdigit pause accept		t_{ID}			40	ms	
Interdigit pause reject		t_{DO}	20			ms	
Propagation delay (St to Q)		t_{PQ}		8	11	µs	TOE = V_{DD}
Propagation delay (St to StD)		t_{PStD}		12		µs	
Output data set up (Q to StD)		t_{QStD}		3.4		µs	
Propagation delay (TOE to Q)	Enable	t_{PTE}		50	60	ns	R_L = 10kΩ
	Disable	t_{PTD}		300		ns	C_L = 50pF
Crystal/clock frequency		f_{CLK}	3.5759	3.5795	3.581	MHz	
Clock output (OSC2)	Capacitive load	C_{LO}			30	pF	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40ms. Tone pause = 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2Hz.
7. Bandwidth limited (0 to 3kHz) Gaussian Noise.
8. The precise dial tone frequencies are 350Hz and 440Hz ±2%.
9. For an error rate of better than 1 in 10,000.
10. Reference to lowest level frequency component in DTMF signal.

INPUT CONFIGURATION

The input arrangement of the MV8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback register to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration the input pins are connected as shown in Fig.3 with the op-amp connected for unity gain and V_{REF} biasing the input at 1/2 V_{DD}. Fig.4 shows the differential configuration, which permits the adjustment of gain with the feedback resistor Rs.

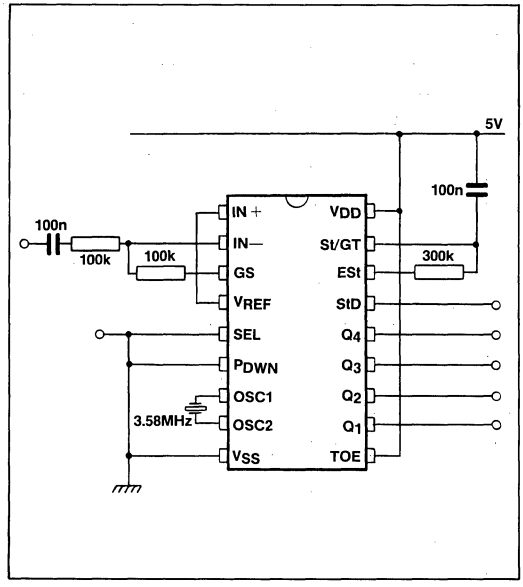


Fig.3 Single ended input configuration

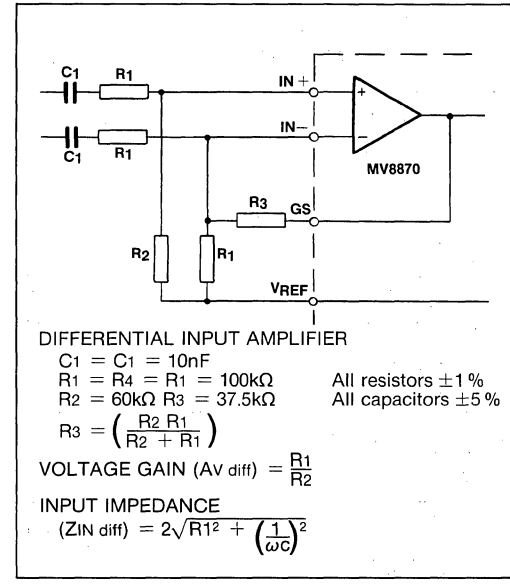
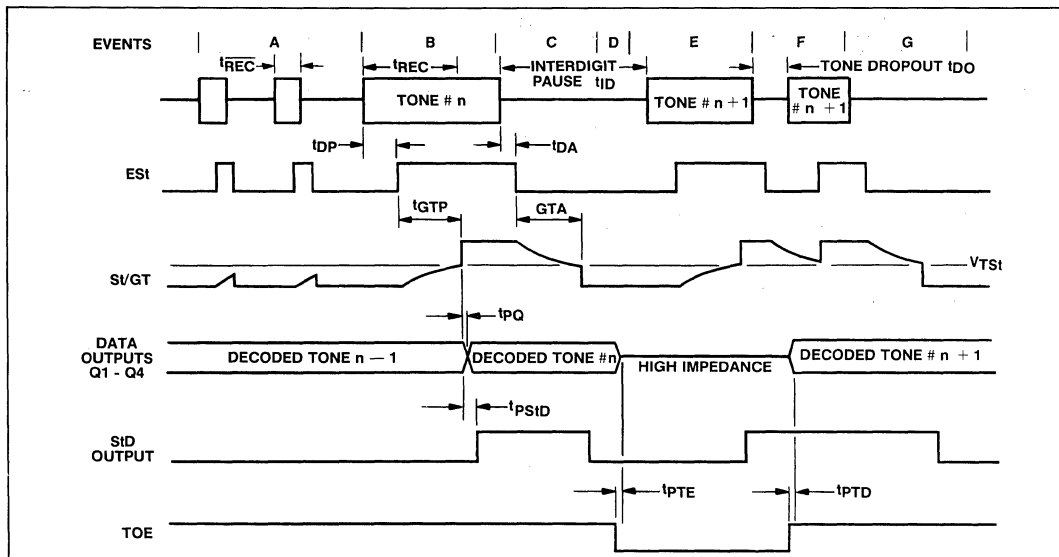


Fig.4 Differential input configuration



A. Short tone bursts detected; tone durations invalid. **B.** Tone #n detected; tone duration valid; decoded to outputs. **C.** End of tone #n detected and validated. **D.** 3-state outputs disabled (high impedance). **E.** Tone (#n + 1) detected; tone duration valid; decoded to outputs. **F.** 3-state outputs enabled; acceptable drop-out of tone (#n + 1) does not register at outputs. **G.** End of tone (#n + 1) detected and validated.

Fig.5 Timing diagram

PIN DESCRIPTIONS

Pin HP	Pin DG	Name	Description	
1	1	IN+	Non-inverting input	Connections to the front-end differential amplifier
2	2	IN-	Inverting input	
3	3	GS	Gain select. Gives access to output of front-end differential amplifier for connections of feedback resistor.	
5	4	V_{REF}	Reference voltage output, nominally $V_{DD/2}$. May be used to bias the inputs at mid-rail (see application diagram).	
7	5	SEL	Logic '1' or '0' selects one of two truth tables (see Table 1).	
10	6	PDWN	Power down active high, internal pulldown resistor. A high level signal powers down and inhibits the oscillator.	
12	7	OSC1	Clock input	3.579545MHz crystal connected between these pins completes internal oscillator.
13	8	OSC2	Clock output	
14	9	V_{SS}	Negative power supply, normally connected to 0V.	
16	10	TOE	3-state output enable (input). Logic high enables the outputs Q1 - Q4. Internal pull-up.	
17	11	Q1	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1).	
18	12	Q2		
19	13	Q3		
20	14	Q4		
25	15	StD	Delayed steering output presents a logic high when a received tone-pair has been registered and the output high latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.	
26	16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognisable tone-pair (signal conditions). Any momentary loss of signal condition will cause ESt to return to a logic low.	
27	17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St (see Table 1).	
28	18	V_{DD}	Positive power supply.	
8	-	FHT	High group sine wave filter output.	
21	-	FLT	Low group sine wave filter output.	
9	-	FH	High group square wave filter output.	
22	-	FL	Low group square wave filter output.	

FUNCTIONAL DESCRIPTION

The MV8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tones of a received pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two sixth-order switched-capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see Fig.6).

The filter section also incorporates notches at 350Hz and 440Hz for exceptional dial-tone rejection. Each filter output is followed by a single-order switched capacitor section to smooth the signals prior to limiting.

Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequenices of the incoming tones.

For testing and monitoring, the high and low group filter outputs (FHT, FLT, FH and FL) are available on pins 8, 21, 9 and 22 respectively (HP package only).

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to 'talk-off' and tolerance to the presence of interfering signals ('third tones') and noise. When the detector recognises the simultaneous presence of two valid tones (referred to as 'signal condition' in some industry specifications), it raises the 'Early Steering' flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

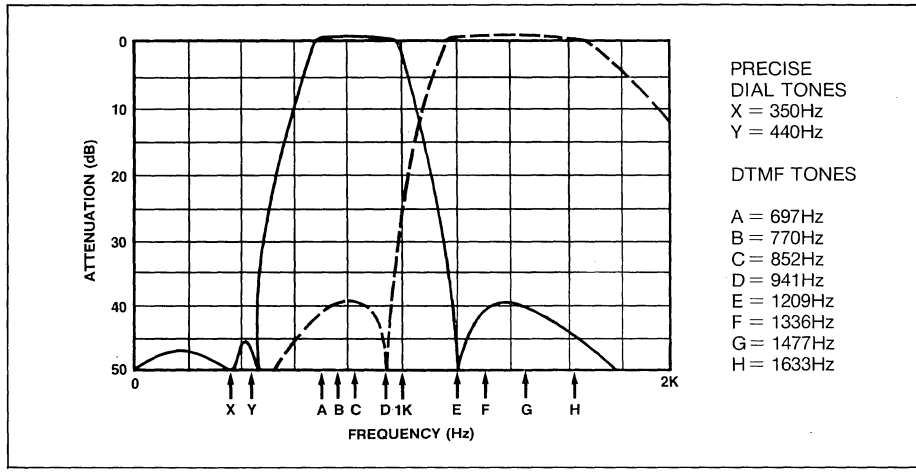


Fig.6 Typical filter characteristic

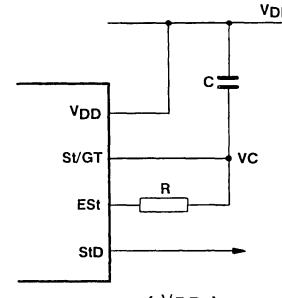
FLOW	FHIGH	KEY	TOE	SEL	Q4	Q3	Q2	Q1
697	1209	1	H	L	0	0	0	1
697	1336	2	H	L	0	0	1	0
697	1477	3	H	L	0	0	1	1
770	1209	4	H	L	0	1	0	0
770	1336	5	H	L	0	1	0	1
770	1477	6	H	L	0	1	1	0
852	1209	7	H	L	0	1	1	1
852	1336	8	H	L	1	0	0	0
852	1477	9	H	L	1	0	0	1
941	1336	0	H	L	1	0	1	0
941	1209	*	H	L	1	0	1	1
941	1477	#	H	L	1	1	0	0
697	1633	A	H	L	1	1	0	1
770	1633	B	H	L	1	1	1	0
852	1633	C	H	L	1	1	1	1
941	1633	D	H	L	0	0	0	0
697	1209	1	H	H	0	0	0	1
697	1336	2	H	H	0	0	1	0
697	1477	3	H	H	0	0	1	1
770	1209	4	H	H	0	1	0	0
770	1336	5	H	H	0	1	0	1
770	1477	6	H	H	0	1	1	0
852	1209	7	H	H	0	1	1	1
852	1336	8	H	H	1	0	0	0
852	1477	9	H	H	1	0	0	1
941	1336	0	H	H	0	0	0	0
941	1209	*	H	H	1	0	1	0
941	1477	#	H	H	1	0	1	1
697	1633	A	H	H	1	1	0	0
770	1633	B	H	H	1	1	0	1
852	1633	C	H	H	1	1	1	0
941	1633	D	H	H	1	1	1	1
		ANY	L	ANY	Z	Z	Z	Z

L = Logic low, H = Logic high, Z = High impedance

Table 1 Functional decode table

STEERING CIRCUIT

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as 'character recognition condition'). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (see Fig.7) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point, the GT output is activated and drives Vc to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the 'delayed steering' output flag, StD, goes high, signalling that a received tone pair has been registed. The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ('drop-out') too short to be considered a valid pulse. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.



$$t_{GTA} = (RC)\ \ln\left(\frac{V_{DD}}{V_{TSt}}\right)$$

$$t_{GTP} = (RC)\ \ln\left(\frac{V_{DD}}{V_{DD} - V_{TSt}}\right)$$

Fig.7 Basic steering circuit

Guard Time Adjustments

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Fig.7 is applicable. Component values are chosen according to the following formulae:

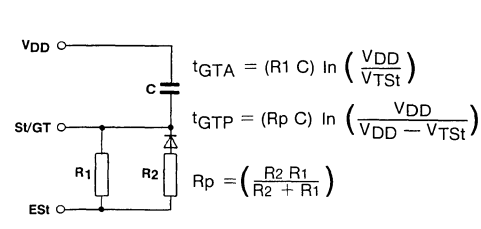
$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = T_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device (see AC Characteristics) and t_{REC} is the minimum signal duration to be recognised by the receiver. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40ms would be 300kΩ.

Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specification which place both accept and reject limits on both tone duration and interdigital pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Fig.8.

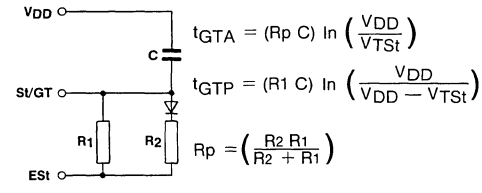


$$t_{GTA} = (R1\ C)\ \ln\left(\frac{V_{DD}}{V_{TSt}}\right)$$

$$t_{GTP} = (Rp\ C)\ \ln\left(\frac{V_{DD}}{V_{DD} - V_{TSt}}\right)$$

$$Rp = \left(\frac{R2\ R1}{R2 + R1}\right)$$

(a) Decreasing t_{GTP} ($t_{GTP} < t_{GTA}$)



$$t_{GTA} = (Rp\ C)\ \ln\left(\frac{V_{DD}}{V_{TSt}}\right)$$

$$t_{GTP} = (R1\ C)\ \ln\left(\frac{V_{DD}}{V_{DD} - V_{TSt}}\right)$$

$$Rp = \left(\frac{R2\ R1}{R2 + R1}\right)$$

(b) Decreasing t_{GTA} ($t_{GTP} > t_{GTA}$)

Fig.8 Guard time adjustment

MV8870-1

DTMF RECEIVER

The MV8870-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Plessey Semiconductors' double-poly CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code.

External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

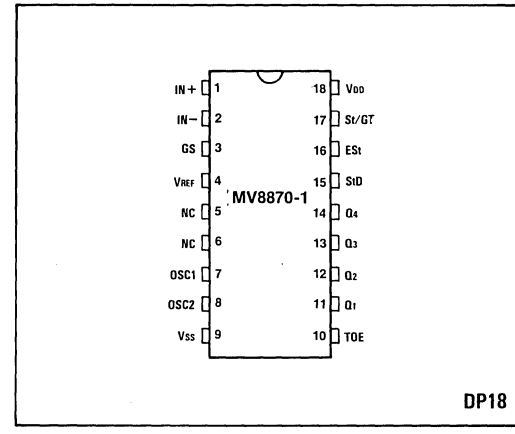


Fig.1 Pin connections - top view

FEATURES

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

APPLICATIONS

- Receiver Systems for BT or CEPT Specifications
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control

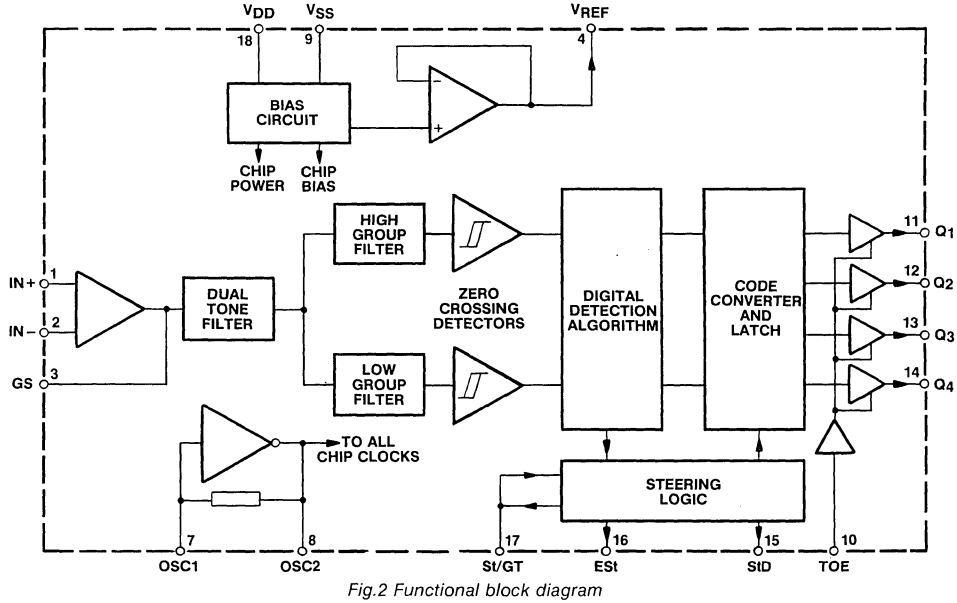


Fig.2 Functional block diagram

FUNCTIONAL DESCRIPTION

The MV8870-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tone groups, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high-group frequencies. The filter section also incorporates notches at 350 and 440Hz for exceptional dial tone rejection (see Fig.3) Each filter is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full supply rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognises the presence of two valid tones (this is referred to as the 'Signal Condition' in some industry specifications) the 'Early Steering' output (ESt) will go to an active state. Any subsequent loss of signal condition will cause the ESt pin to go to its inactive state (see Fig.5).

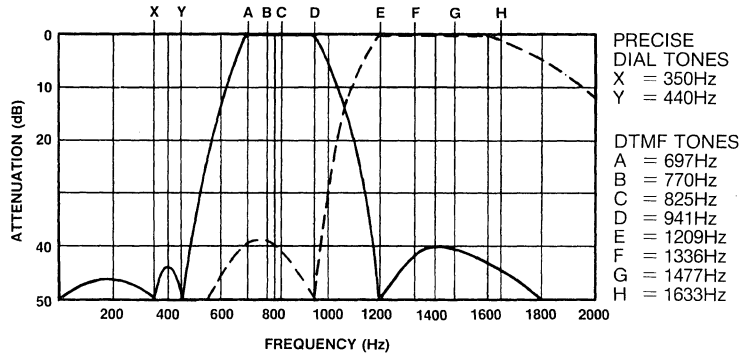


Fig.3 Filter response

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes the voltage at the St/GT pin ($V_{St/GT}$) to rise as the capacitor discharges (see Figs.4 and 5).

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), $V_{St/GT}$ reaches the threshold (V_{TSt}) of the steering logic which allows it to register the tone pair and strobe the corresponding 4-bit code into the output latch (see Table 1). At this point the St/GT pin is activated as an output and drives $V_{St/GT}$ to V_{DD} (see Fig.5).

St/GT continues to drive high as long as ESt remains high. After a short delay to allow the output latch to settle, the delayed steering output pin (StD) goes high to indicate that the code for a new received tone-pair is available. The contents of the output latch are output onto the output bus (Q_1 to Q_4 pins) when the three-state output enable pin (TOE) is high.

The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop-out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

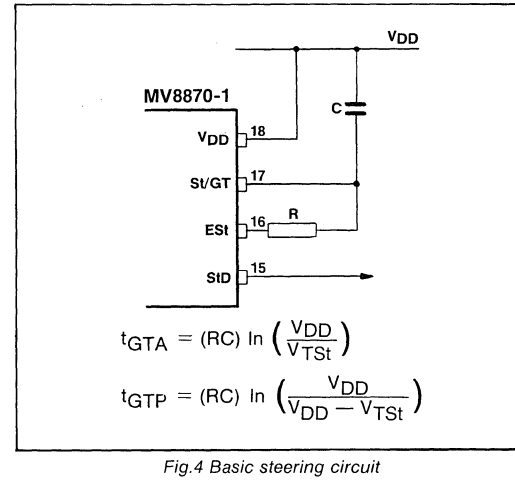
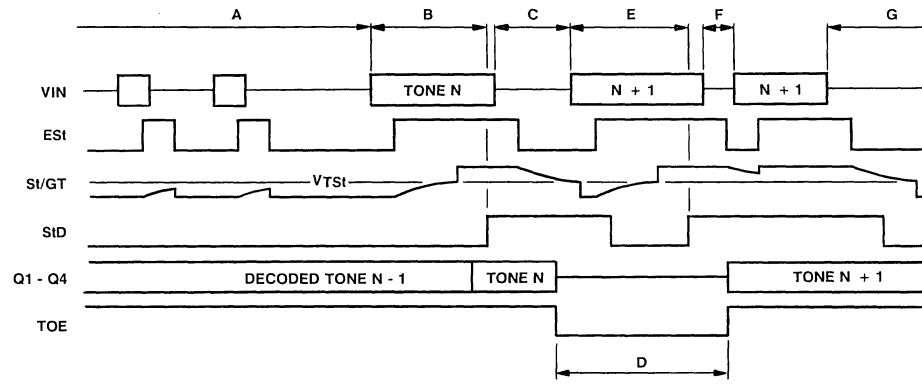


Fig.4 Basic steering circuit



Explanation of Events

A. Tone bursts detected, but tone duration invalid and output latch unchanged.
B. Tone N detected, tone duration valid, output latch updated and new data signalled by StD.
C. End of tone N detected, tone absent duration valid, but output latch not updated until next valid tone.
D. Outputs switched to high impedance.
E. Tone N + 1 detected, tone duration valid, tone decoded, output latch updated (although outputs are currently high impedance) and new data signalled by StD.
F. Acceptable dropout of tone N + 1, tone absent duration invalid, StD and output latch unchanged.
G. End of tone N + 1 detected, tone absent duration valid, StD goes low but output latch not updated until next valid tone.

Fig.5 Timing diagram

F_{LOW}	F_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1209	0	H	1	0	1	0
941	1336	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	Any	L	Z	Z	Z	Z

Table 1 Functional decode

APPLICATIONS

A simple application circuit is shown in Fig.6. This has a symmetric guard time circuit, a single-ended analog input and a dedicated crystal oscillator.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigit pause, the simple steering circuit shown in Fig.6 is applicable. Component values are chosen according to the formula (see Figs.4, 7 and 8):

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

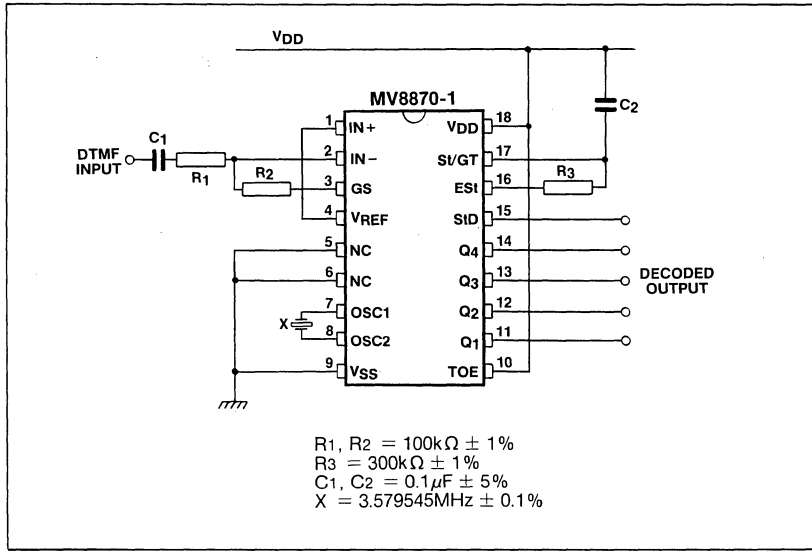
The value of t_{DP} is a device parameter (see Dynamic Characteristics) and t_{REC} is the minimum signal duration to be recognised by the receiver. Likewise t_{DA} is a device parameter and t_{ID} is the minimum time taken to recognise an interdigit pause. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer.

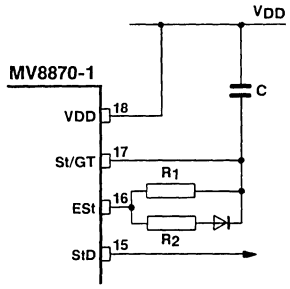
Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be registered. Alternatively a relatively short t_{REC} with a long t_{ID} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figs.7 and 8.

Differential Input Configuration

The input arrangement of the MV8870-1 provides a differential input op. amp. and a bias source (V_{REF}) to bias the inputs at mid-rail. The gain may be adjusted through a feedback resistor from the op. amp. output (GS). In a single-ended configuration the input pins are connected as shown in Fig.6 where the op. amp. is connected to give unity gain and the V_{REF} pin biases the input at $V_{DD}/2$.

Fig.9 shows the differential configuration. In this circuit gain is adjusted through the feedback resistor R5.



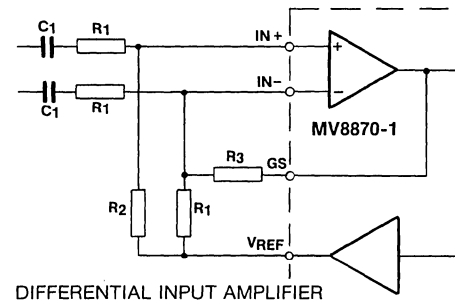


$$t_{GTA} = (Rp\,C)\ln\frac{V_{DD}}{V_{TSt}}$$

$$t_{GTP} = (R1\,C)\ln\frac{V_{DD}}{V_{DD}-V_{TSt}}$$

$$Rp = \frac{R1\,R2}{R1+R2}$$

Fig.7 Guard time adjustment ($t_{GTP} < t_{GTA}$)



DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_1 = 10nF$

$R_1 = R_4 = R_1 = 100k\Omega$ All resistors ±1%

$R_2 = 60k\Omega$ $R_3 = 37.5k\Omega$ All capacitors ±5%

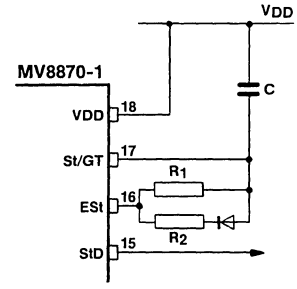
$$R_3 = \left(\frac{R_2\,R_5}{R_2+R_5}\right)$$

$$\text{VOLTAGE GAIN } (A_{V\,diff}) = \frac{R_5}{R_1}$$

INPUT IMPEDANCE

$$(Z_{IN\,diff}) = 2\sqrt{R1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Fig.9 Differential input configuration



$$t_{GTA} = (R1\,C)\ln\frac{V_{DD}}{V_{TSt}}$$

$$t_{GTP} = (Rp\,C)\ln\frac{V_{DD}}{V_{DD}-V_{TSt}}$$

$$Rp = \frac{R2\,R1}{R2+R1}$$

Fig.8 Guard time adjustment ($t_{GTP} > t_{GTA}$)

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.78MHz crystal which is normally connected as shown in Fig.6. However, it is possible to configure several MV8870-1 devices to use only a single oscillator crystal. The devices are chained together with the oscillator output of the first device in the chain capacitively coupled to the oscillator input of the second device and so on down the chain. The details are shown in Fig.10. Precision balancing capacitors are not required as problems of unbalanced loading are not a concern.

Receiver System for British Telecom Specification POR 1151

The circuit shown in Fig.11 illustrates the use of the MV8870-1 in a typical receiver system. The BT specification defines the non-operate level as input signals below -34dBm. This is obtained by choosing R1 and R2 to give 3dB of attenuation so that an input of -34dBm corresponds to -37dBm at the op. amp. outpt pin (GS). The tolerances on R3 and C2 give a tolerance on guard time of 6%. For better performance the non-symmetric guard time circuit shown in Fig.12 is recommended.

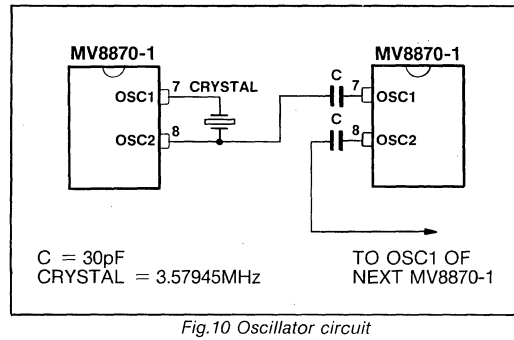


Fig.10 Oscillator circuit

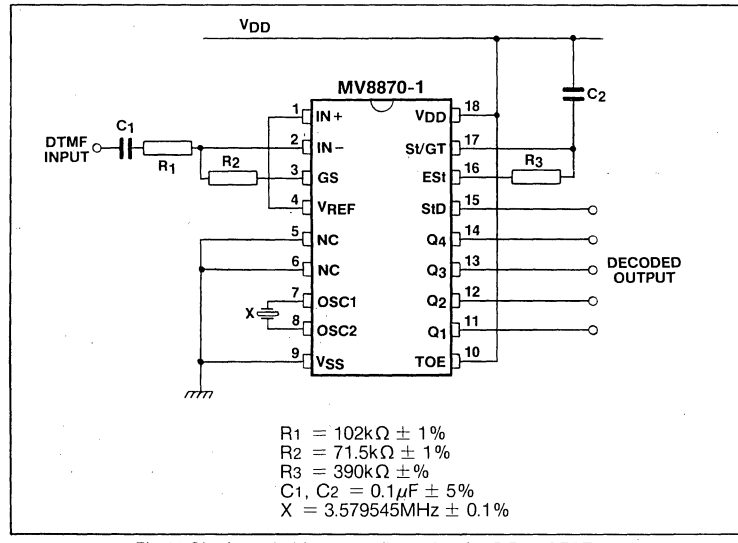


Fig.11 Single ended input configuration for BT or CEPT spec

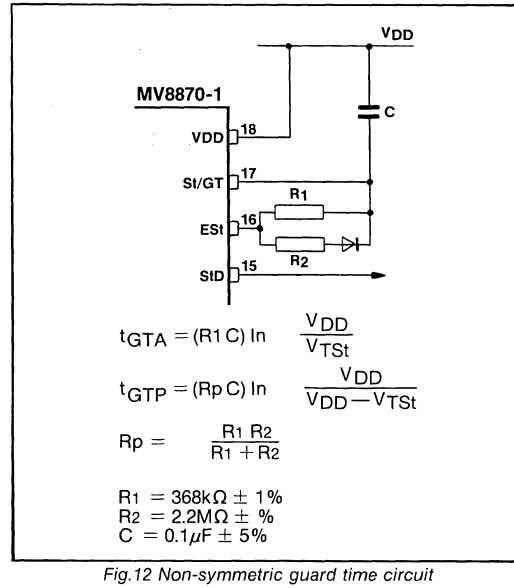


Fig.12 Non-symmetric guard time circuit

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
IN +, IN-	1,2	**In Plus and Minus (Voltage Inputs).** These are respectively the non-inverting and inverting inputs to the front-end op. amp. The DTMF input is applied to these pins in normal operation.
GS	3	**Gain Select (Voltage Output).** This pin is connected to the output of the front-end op. amp. A feedback resistor between this pin and the inverting input (IN-) controls the front-end gain.
V_{REF}	4	**Reference Voltage (Voltage Output).** This pin outputs a voltage which is half-way between the power supply voltages (V_{SS} and V_{DD}). It can be used to bias the input signal.
(IC)	5,6	**(Internal Connection).** These pins should be tied to the ground (V_{SS}).
OSC1	7	**Oscillator 1 (Digital Input).** This is the input to the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter output (OSC2). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
OSC2	8	**Oscillator 2 (Digital Output).** This is the output of the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter input (OSC1). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
V_{SS}	9	**Negative Supply (Power Input).** This is the negative power supply for the device. It is normally 0V.
TOE	10	**Three-State Output Enable (Digital Input with Pull-up).** If this pin is high then the decoder outputs (Q_1 to Q_4) are enabled. If it is low then the outputs go into their high impedance state. There is an internal pull-up at this pin.
Q_1 - Q_4	11 - 14	**Q_1 to Q_4 (Three-State Outputs).** When the TOE pin is high these pins output the code in the output latch which corresponds to the last valid tone-pair detected. They go into their high impedance state when the TOE pin is low.
StD	15	**Delayed Steering (Digital Output).** This pin follows the ESt and St/GT pins. It goes high to indicate that a new tone-pair has been detected and the corresponding code has been loaded into the output latch. It goes low to indicate that a new tone-pair is expected.
ESt	16	**Early Steering (Digital Output).** This pin goes high when the digital detection algorithm decides that there is a valid DTMF input. It goes low as soon as the algorithm decides that there is no valid DTMF input. In normal use this pin is used to drive an external guard time circuit which in turn drives the St/GT pin.
St/GT	17	**Steering/Guard Time (Voltage Input/Digital Output).** This pin follows the ESt pin. When ESt pin changes state this pin acts as an input and monitors the voltage developed here by the ESt pin acting through the external guard time circuit. When the voltage reaches the internally generated V_{TSt} level then this pin acts as an output and pulls itself fully to the state of the ESt pin. When this pin goes fully high a new code is loaded into the output latch and the StD pin goes high. When this pin goes fully low the device prepares itself for a new tone-pair and the StD pin goes low.
V_{DD}	18	**Positive Supply (Power Input).** This is the positive power supply for the device. It is normally 5V.

ELECTRICAL CHARACTERISTICS

Test Conditions (see Fig.13) - Voltages are with respect to ground (V_{SS})

Parameter	Symbol	Value			Units
		Min.	Typ. (1)	Max.	
Positive supply voltage (V_{DD} pin)	V_{DD}	4.75	5	5.25	V
Ambient temperature	T_{amb}	-40		+85	°C
Op. amp. output capacitive load (GS pin)	C_{OUT}			100	pF
Op. amp. output resistive load (GS pin)	R_{OUT}	50			kΩ
Input high voltage (OSC1 and TOE pins)	V_{IH}	3.5		V_{DD}	V
Input low voltage (OSC1 and TOE pins)	V_{IL}	0		1.5	V
Oscillator frequency (OSC1 and OSC2 pins)	f_O	3.5759	3.579545	3.5831	MHz
Oscillator input rise time (OSC1 pin)	t_{OR}			110	ns
Oscillator input high time (OSC1 pin)	t_{OH}	110		170	ns
Oscillator input fall time (OSC1 pin)	t_{OF}			110	ns
Oscillator input low time (OSC1 pin)	t_{OL}	110		170	ns
Oscillator output load (OSC2 pin)	C_{LO}			30	pF

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

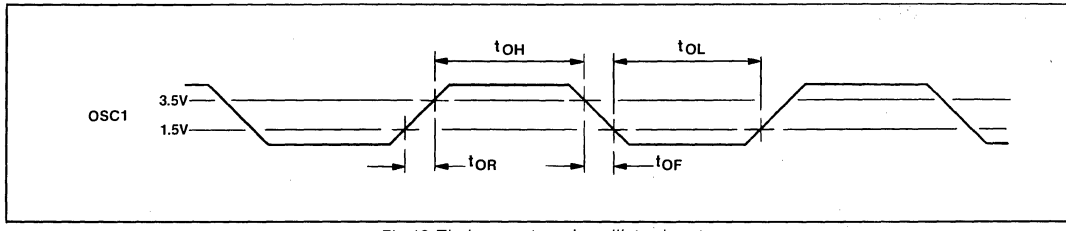


Fig.13 Timing - external oscillator input

Static Characteristics - Voltages are with respect to ground (Vss)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (1)	Max.		
Power dissipation	P_D		15	37	mW	
Supply current (V_{DD} pin)	I_{DD}		3.0	7.0	mA	
Reference voltage (V_{REF} pin)	V_{REF}	2.4		2.8	V	
Reference output resistance (V_{REF} pin)	R_{REF}		10		kΩ	
Input leakage current (OSC1, IN+ and IN- pins)	I_I		100		nA	$0 \leqslant V_{PIN} \leqslant V_{DD}$
Internal pull-up current (TOE pin)	I_{PU}		7.5	15	A	$0 \leqslant V_{PIN} \leqslant V_{DD}$
Output low sink current (OSC2, Q_1 - Q_4, StD, ESt and St/GT pins)	I_{OL}	1	2.5		mA	$0.4V \leqslant V_{PIN} \leqslant V_{DD}$
Output high source current (OSC2, Q_1 - Q_4, StD, ESt and St/GT pins)	I_{OH}	0.4	0.8		mA	$0V \leqslant V_{PIN} \leqslant 4.6V$
Steering threshold voltage (St/GT pin)	V_{TSt}	2.2		2.5	V	
Pin capacitance	C_P		7	15	pF	Pin to supplies

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Dynamic Characteristics: Input Op. Amp. - Voltages are with respect to ground (Vss)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (1)	Max.		
Input impedance (IN+ and IN- pins)	R_{IN}		10		MΩ	1kHz
Input offset voltage (IN+ and IN- pins)	V_{OS}		25		mV	
Power supply rejection	PSRR		60		dB	1kHz
Common mode range	V_{CM}		3.0		V p-p	No load
Common mode rejection	CMRR		60		dB	
DC open loop voltage gain	A_{VOL}		65		dB	
Open loop unit gain bandwidth	f_C		1.5		MHz	
Output voltage swing (GS pin)	V_O		4.5		V p-p	R_{OUT} to V_{SS} $\geqslant$ 100kΩ

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Dynamic Characteristics: Detector - Voltages are with respect to ground (Vss)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (13)	Max.		
Valid input level (GS pin)	V_{VL} P_{VL}	61.7 -31		2458 1	mV p-p dBm	1,2,3,5,6,9
Invalid input level (GS pin)	V_{IL} P_{IL}			30.8 -37	mV p-p dBm	1,2,3,5,6,9
Acceptable positive twist	T_{AP}	6	10		dB	2,3,6,9
Acceptable negative twist	T_{AN}	6	10		dB	2,3,6,9
Acceptable frequency deviation	Δ_{FA}	-(1.5% +2Hz)		(1.5 % +2Hz)		2,3,5,9
Frequency deviation - rejected as too low	Δ_{FRL}		-5%	-3.5%		2,3,5,9
Frequency deviation - rejected as too high	Δ_{FRH}	3.5 %	5 %			2,3,5,9
Third tone tolerance	P_{TTT}	-18.5			dB	2,3,4,5,9,12
Noise tolerance	P_{NT}		-12		dB	2,3,4,5,7,9,10
Dial tone tolerance	P_{DTT}		22		dB	2,3,4,5,8,9,11
Tone present detect time	t_{DP}	5	11	14	ms	
Tone absent detect time	t_{DA}	0.5	4	8.5	ms	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600 Ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40ms, tone pause = 40ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tone in composite signal have equal amplitudes.
6. Tone pair is deviated by ± (1.5% + 2Hz).
7. Bandwidth limited (3kHz) Gaussian Noise.
8. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest frequency component in DTMF signal.
11. Referenced to the minimum valid input level.
12. Referenced to Fig.11. Input DTMF Tone Level at -25dBm (-28dBm at GS pin). Interference Frequency Range is 480 to 3400Hz.
13. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

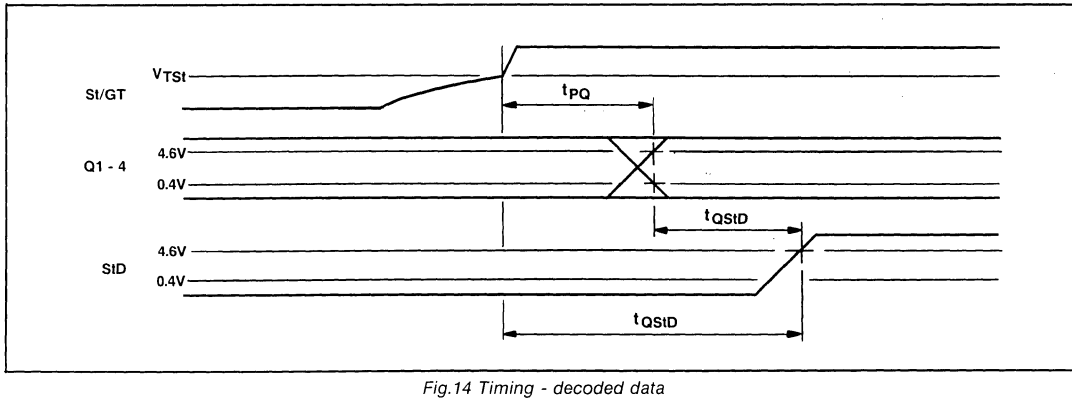


Fig.14 Timing - decoded data

Dynamic Characteristics: Decoder (see Figs.14 and 15) - Voltages are with respect to ground V_{SS})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (1)	Max.		
Propagation delay (St/GT to Q)	t_{PQ}		8	11	μs	TOE pin high
Propagation delay (St/GT to StD)	t_{PStD}		12		μs	
Output data set-up time (Q to StD)	t_{QStD}		3.4		μs	TOE pin high
Enable propagation delay (TOE to Q)	T_{PTE}		50		ns	R_L = 10kΩ (pulldown) C_L = 50pF
Disable propagation delay (TOE to Q)	t_{PTD}		300		ns	R_L = 10kΩ (pulldown) C_L = 50pF

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

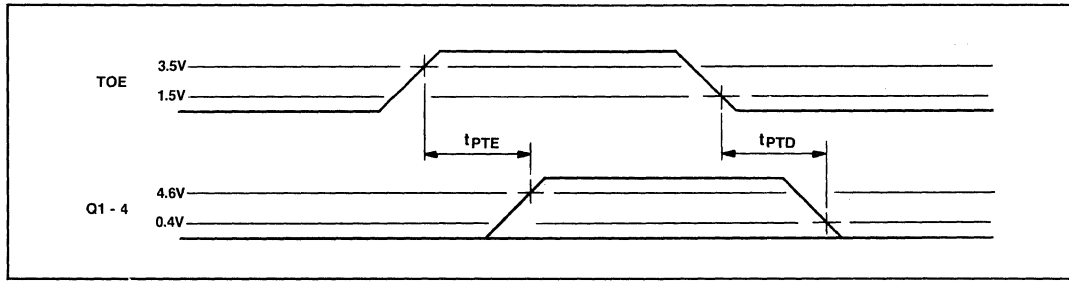


Fig.15 Timing - output enable and disable

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to the negative power supply (V_{SS})

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage (pin 18), V_{DD}	6V
Voltage on any pin (other than supplies), V_{MAX}	-0.3V to V_{DD} +0.3V
Current at any pin (other than supplies), I_{MAX}	10mA
Storage temperature, T_{STG}	-65°C to +150°C
Package power dissipation, P_{DISS}	1000mW

SL376M

METERING SUBSCRIBER LINE INTERFACE CIRCUIT

The SL376M is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, controls ringing, detects ground-key and off-hook conditions and transmits and receives voice signals.

It also enables metering pulses to be transmitted to the subscriber line while transmitting and receiving voice signals. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL376M is fabricated using bipolar technlogy.

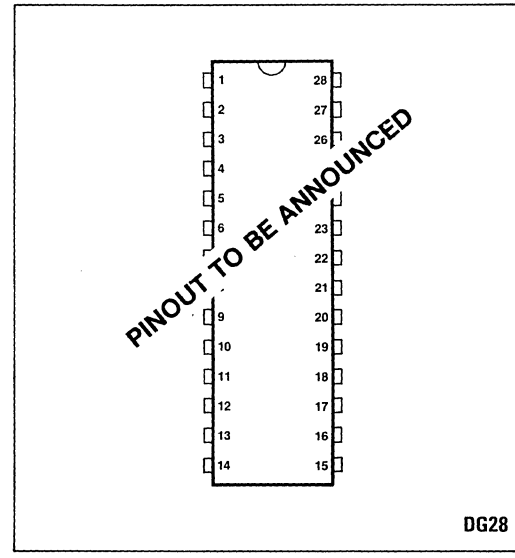


Fig.1

FEATURES

- Low Power Line Feed via Regulator
- Programmable Constant Voltage Resistive Feed
- Programmable AC Termination Impedance
- Ground-key Detection
- Programmable Off-hook Detection
- Ring Relay Driver
- Low Power Standby Mode
- Normal or reversed Line Polarity
- Supports 2.2V RMS Metering Pulses
- 75V Rating to Ease Line Protector Tolerancing

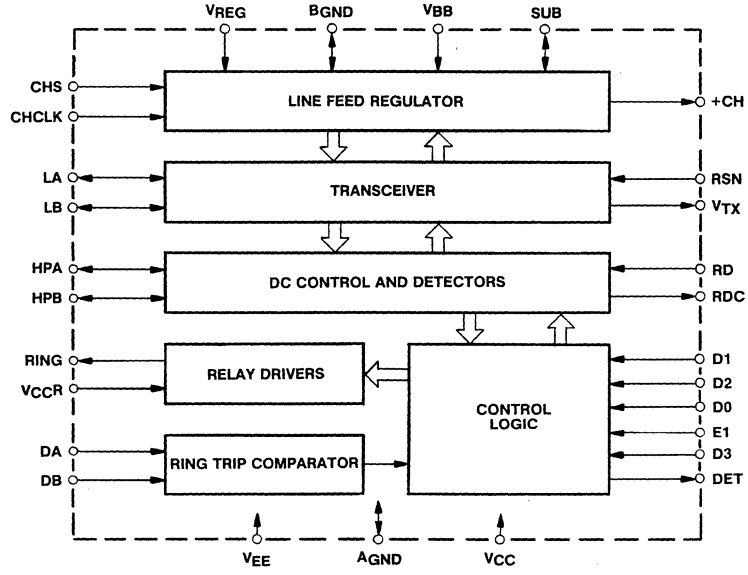


Fig.2 Functional block diagram

PIN DESCRIPTIONS

Symbol	Pin Name and Description
BGND	Battery ground (power)
V_{REG}	Regulated voltage for power amplifiers
V_{CC}	+5V supply
RING	Ring relay driver out
$V_{CC}R$	+5V relay supply
+CH	Switching regulator out
V_{BB}	Battery negative
SUB	Quiet battery (substrate)
CHS	Switching regulator stabilising network
CHCLK	Switching regulator clock input
D3	Relay driver control
E1	Detector select
DET	Detector output
D1	Control input
D2	Control input
D0	Control input
RDC	DC reference defining line current via RDC to RSN
AGND	Analog and digital ground
RSN	Receive summing node controlling AC and DC line current
V_{EE}	-5V input
V_{TX}	Transmit audio output
HPB	RING side of filter capacitor
HPA	TIP side of filter capacitor
RD	Off hook detector load resistor
DA	Positive input, ring trip comparator
DB	Negative input, ring trip connector
LA	TIP lead
LB	RING lead

GENERAL DESCRIPTION

The Plessey SL376M Metering Subscriber Line Interface Circuit performs the telephone line interface functions required in both central office and PABX environments. The full range of signal transmission, battery feed and loop supervision functions are performed. Signal transmission performance is compatible with North American and CCITT recommendations. Overvoltage protection and ringing are provided by means of external networks. However, the SLIC has a full 75V line rating.

The signal transmission function includes both 2- and 4-wire and 4- to 2-wire conversion. The 2-wire termination impedance is programmable with a single external impedance, which may be complex. The battery feed architecture makes the DC feed resistance programmable with external resistors.

A polarity reversal function is provided which transposes the normal voltage sense of the TIP and RING leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode limits loop current and cuts power dissipation while allowing the full range of supervisory functions to be utilised.

The output amplifiers are powered by an internal switching regulator in order to reduce power consumption.

The supervisory functions allow for off-hook detection, ground key detection, and ring trip detection. The outputs of these detectors are read through a single, TTL compatible output. The off-hook detector signal may be filterd and has a threshold adjust by means of external components. Additional supervisory functions put the TIP lead into an open-circuit or high-impedance state suitable for application in ground-start systems. Similarly, both the TIP and RING leads may be open circuited. A relay driver is provided for the ring-relay.

The programmable states are controlled by a 3-bit TTL compatible digital code. The detector output is controlled by a selector bit. These lines are TTL compatible levels.

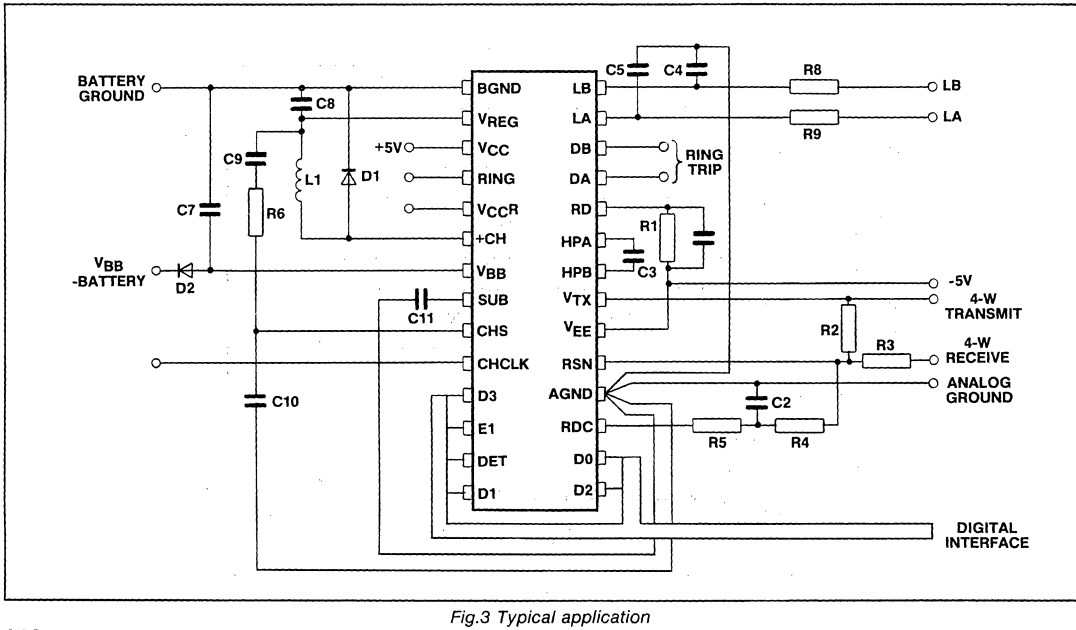


Fig.3 Typical application

SL9009

ADAPTIVE BALANCE CIRCUIT

The SL9009 is normally used to extract the received signal from the combined transmitted and received signal on a telephone line. It constantly analyses the extracted signal and adjusts to compensate for variations in telephone lines.

The device can be used with a bridge circuit where it acts as an impedance network which adjusts itself to match the telephone line. When the bridge is in balance the difference between its two arms is due to the received signal.

The SL9009 consists of three cells and a correlation detector which is normally used to control the cells via a negative feedback loop. It is built using bipolar technology.

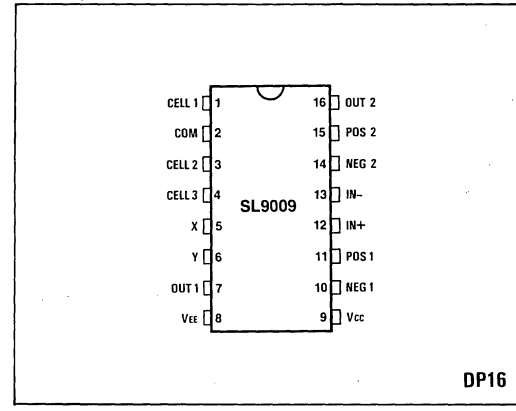


Fig.1 Pin connections - top view

FEATURES

- Extracts the Received Signal
- Adapts Automatically to Line Variations
- No Microprocessor Required
- Simple Application Circuit
- 40dB (Typ.) Rejection of Transmitted Signal

APPLICATIONS

- Modems - Extracting the Received Data
- Feature Phones - Extracting the Received Voice
- PBX/PABX/CO Line Cards - Extracting the Incoming Signal from the Telephone Line

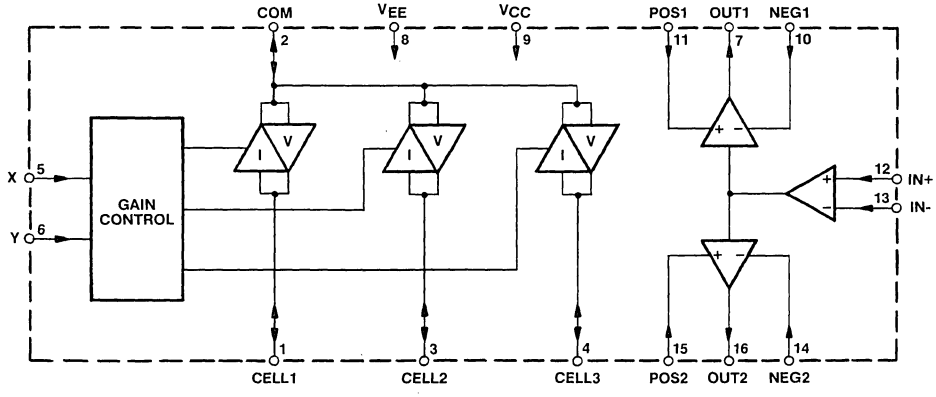


Fig.2 Functional block diagram

FUNCTIONAL DESCRIPTION

The SL9009 adaptive balance circuit is divided into two separate parts as shown in Fig.2. These are the impedance cell section and the phase detector section. The impedance cell section is normally used with a balanced impedance bridge circuit which allows the incoming signal to be extracted from the combined signal on the line.

The phase detector section is used to analyse the extracted signal to determine how much of the residual outgoing signal is present. This allows the circuit to adjust itself to minimise the residual signal automatically.

Impedance Cells

This consists of three cells and the gain controller (see Fig.2). Each cell has a voltage buffer and a variable gain current amplifier. The three cells share the COM pin (pin 2) which is the common input to their voltage buffers and the common output from their current amplifiers.

There is a pin directly associated with each cell. This is the CELL 1, 2 or 3 pin (pin 1, 3 or 4) and it is driven by the cell's voltage buffer. The current which is sunk or sourced at this pin is the input to the cell's current amplifier.

This means that the voltage developed at the COM pin causes a current to flow at each of the three individual cell pins (CELL 1, 2 and 3). These currents are amplified by the gains of the three cells and the sum is the current which flows in or out of the COM pin.

The gain of the cells are controlled by the X and Y gain control pins (pins 5 and 6). Fig.3 indicates how the two controls operate. The precise voltages at the control inputs necessary to give a defined gain vary with the power supplies, but this is compensated for by the feedback loop.

The gain control is characterised by a line of symmetry corresponding to a certain voltage on the Y pin. Above this voltage cell 2 is off and below it cell 3 is off. The line of symmetry also corresponds to the highest gain on cell 1 for a fixed voltage on the X pin.

In addition to the current due to the three impedance cells at the COM pin (pin 2), a DC bias current also flows. The value of this current depends on the power supplies and the voltage at the control inputs, especially the X pin.

If the currents at the cell pins (CELL 1 to 3) are too high then clipping will occur. If these pins are left open circuit then the device still presents a finite impedance at the COM pin, but this is very large.

Phase Detectors

The phase detector section consists of a differential voltage input buffer which drives the two phase analysers (see Fig.2). The input is taken from the IN+ and IN- pins (pins 12 and 13).

Each analyser consists of a transconductance amplifier which can have either a positive or negative gain. The sign of the gain is determined by the analysis pins for the detector. These are POS 1 and NEG 1 (pins 11 and 10) for detector 1 and POS 2 and NEG 2 (pins 15 and 14) for detector 2. The outputs of the transconductance amplifiers are connected to the OUT 1 and OUT 2 pins (pins 7 and 16).

The direction of the current at an output pin is determined by the phase relationship between the signal at the input and the signal at the analysis pins. The magnitude of the current depends on the magnitude of the input alone. If the analysis pins are in phase with the input then the output will source current. If they are 180° out of phase then the output will sink current. If they are 90° out of phase then the output will alternately sink and source current. If the input is small then the current sunk or sourced will be small.

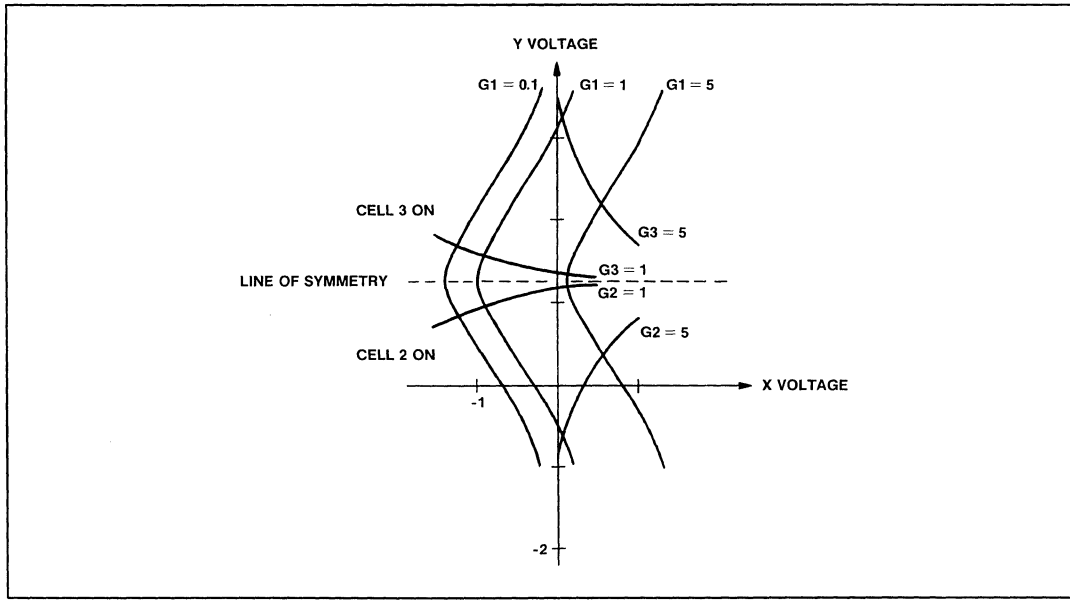


Fig.3 Typical gain characteristics for CELLS 1, 2 and 3 (G1, G2 and G3 respectively)

APPLICATIONS

Fig.4 shows a simple bridge configuration which can adjust the amplitude and phase over a wide range to match an unknown impedance, Z. In this case R1 is used to match R3; R2 is used to match the in-phase component across Z; C1 is used to produce phase lead and C2 is used to produce phase lag. The X and Y gain control inputs give two degrees of freedom which allow both in-phase and out-of-phase components to be balanced.

The feedback arrangement is shown in Fig.5. If the extracted signal is in phase with the transmitted signal then the OUT 1 pin (pin 7) will sink current (since the inverting NEG 1 pin is used) and so cause the voltage at the X pin (pin 5) to fall. This causes the gain of CELL 1 to fall and so produces less attenuation of the signal at the COM pin (pin 2). This means that more of the transmitted signal is subtracted from the combined signal.

If too much of the transmitted signal is subtracted then the extracted signal will become 180° out of phase with the transmitted signal. This produces the opposite effect and so reduces the amount of the transmitted signal which is subtracted.

Any remaining correlation between the transmitted singal and the extracted signal must be due to a lag or lead. If the extracted signal lags the transmitted signal by 90° then the derivative of the extracted signal is in phase with the transmitted signal (see Fig.6).

Applying the derivative of the extracted signal to the inverting NEG 2 pin causes the OUT 2 pin to sink current and so lowers the voltage at the Y pin (pin 6). This causes CELL 2 to switch on and increases its gain until balance occurs. Thus a lag is created (through C2 of Fig.4) in the signal which is subtracted from the combined signal, cancelling the lag in the extracted signal.

If the extracted signal leads the transmitted signal then the circuit causes CELL 3 to switch on and causes a lead (through C1 of Fig.4) in the signal at the COM pin. This cancels the lead in the extracted signal.

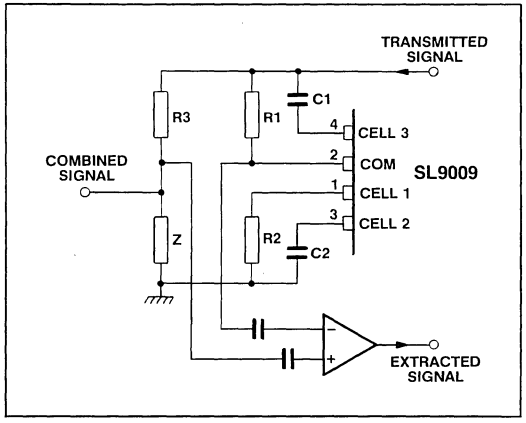


Fig.4 Simple balancing network

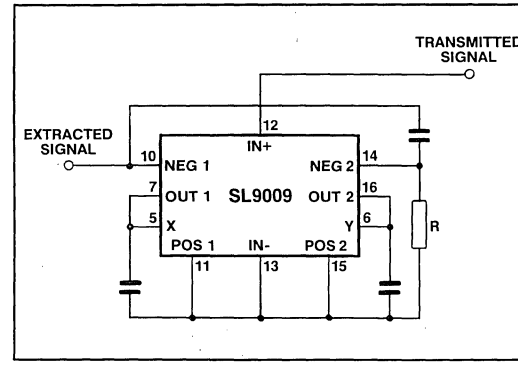


Fig.5 Feedback arrangement

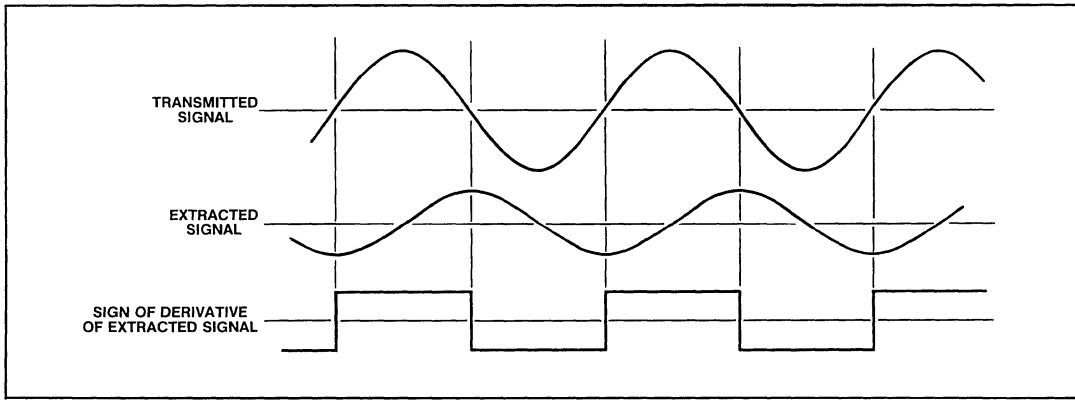


Fig.6 Signal relationship for 90° of lag on extracted signal

Use of a Gyrator Circuit

The transmitted signal may be connected to a telephone line through a transformer, which is often far from an ideal component and can effectively add a resistor and inductor in series to the line. The effect of this can be removed by adding the equivalent of these components, suitably scaled, to the bridge network. The problem of doing this is that although the values of resistance and inductance required may be well known, the scaled inductance may not be practical.

This may be overcome by using a gyrator circuit as shown in Fig.7. This circuit can be used instead of resistor R2 in Fig.4.

If $Z = (j\omega C)$ then the circuit looks like a resistance of R_A in series with an impedance of $L = R_A R_B / Z$. Realistic value for this circuit are $R_A = 5.1k\Omega$, $R_B = 180k\Omega$ and $C = 0.1\mu F$ giving $L = 91.8H$.

Improved Line Modelling

The simple balancing network shown in Fig.4 is capable of amplitude and phase compensation at a single frequency. To balance a telephone line across the voice band we build a model of the line and adjust it using the SL9009. Since the adjustments give good balance at any single frequency, the model ensures that good balance is achieved across the band.

A detailed application circuit making use of this approach is shown in Fig.8. The transmitted signal is output through the termination impedance and on to the line where it forms part of the combined line signal.

The transmitted signal is also passed to the termination balancing impedance and the line balancing impedance to generate the initial expected signal. The line balancing impedance should take account of the resistance and inductance introduced if a line transformer is used, possibly by using a gyrator circuit as previously described.

If the line balancing impedance matches the line impedance then the difference between the combined line signal and the initial expected signal is the received signal. In this special case all components of the transmitted signal wuld be cancelled without using an SL9009.

In most cases, however, the line impedance does not match the line balancing impedance. The SL9009 can then be used to compensate for the mismatch, as shown in Fig.8.

The initial expected signal is fed to the SL9009 which generates the final expected signal. It is the final expected signal which is subtracted from the combined line signal to give the extracted signal. The SL9009 generates the final expected signal by comparing the initial expected signal with the in-phase and the out-of-phase components of the extracted signal as in the case of the simple balancing network.

To be more precise, the SL9009 generates the final expected signal times two thirds. This is multiplied by 1.5 before it is subtracted from the combined line signal. The signal generated by the SL9009 is always less than the initial expected signal so multiplying it by 1.5 enables the final expected signal to be greater than the initial expected signal.

By using the SL9009 to adjust the best estimate of the effect of the line impedance in this way, better balancing can be achieved for broadband voice signals.

A complete circuit which can be used in a modem or in a sophisticated telephone is shown in Fig.9.

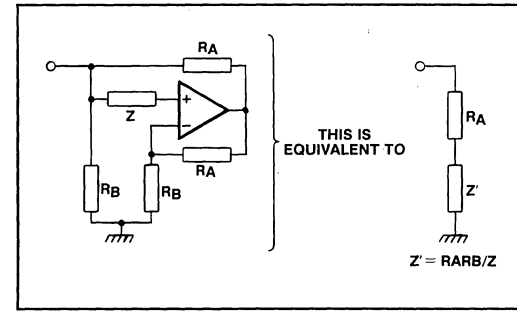


Fig.7 Gyrator circuit

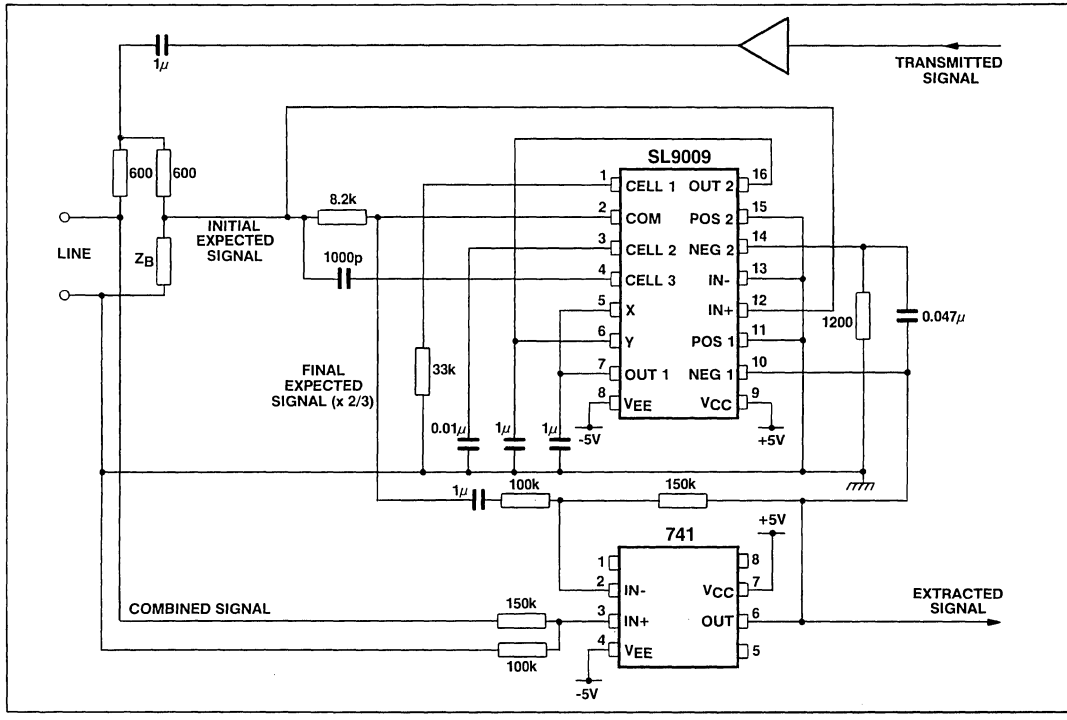
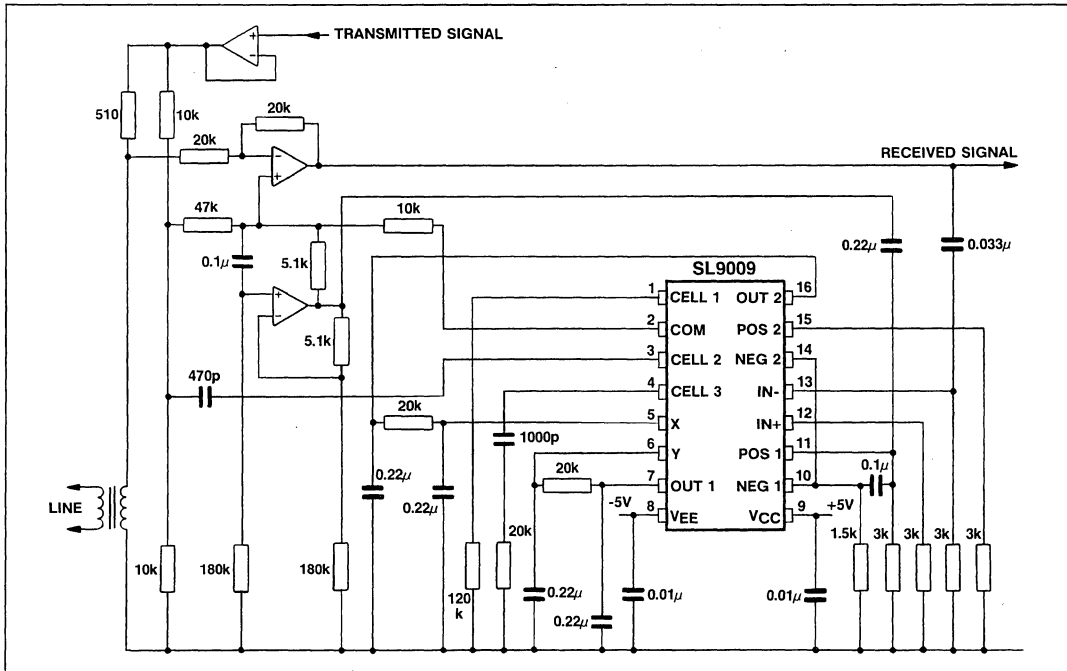


Fig.8 Circuit for improved line modelling



Line transformer:- Total primary + Secondary resistance = 100Ω; Inductance = 0.9H.

Fig.9 Complete circuit

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
CELL 1, CELL 2, CELL 3	1,3,4	**CELL 1, 2 and 3 Pins (Voltage Outputs and Current inputs).** These are the pins which are directly associated with CELLS 1, 2 and 3. The voltage developed at the common cell pin (pin 2) is buffered and output at these pins, causing them to sink or source currents. The currents flowing in or out of these pins act as inputs which are amplified by the gains of the cells and the amplified currents are summed and returned to the common cell pin as its output current. The gains of the cells are determined by the gain control pins (pins 5 and 6).
COM	2	**Common Cell Pin (Voltage Input and Current Output).** The voltage developed at this pin is buffered and output at the separate cell pins (pins 1, 3 and 4). The currents output by the 3 cells are summed and the result is the current which is sunk or sourced at this pin.
X	5	**X Gain Control (Voltage Input).** Increasing the voltage at this pin increases the gain of CELL 1 and also of CELL 2 and CELL 3, but to a lesser extent (see Fig.3).
Y	6	**Y Gain Control (Voltage Input).** Increasing the voltage at this pin from a low value decreases the gain of CELL 2 until it switches off. At this point CELL 3 switches on and increasing the voltage further causes the gain of CELL 3 to increase (see Fig.3). The gain of CELL 1 increases as the voltage at this pin increases from a low value until CELL 2 switches off. Further increasing the voltage causes the gain of CELL 1 to decrease.
OUT 1	7	**Detector 1 Output (Current Output).** This is the output of phase detector 1. The current sunk or sourced at this pin is proportional to the differential voltage between the detector input pins (pins 12 and 13). The sign of the transconductance gain (i.e. of the constant of proportionality) is controlled by the detector 1 analysis pins (pins 11 and 10). The direction of the average current output is determined by the phase relationship between the input and the analysis pins and the magnitude is determined by the input alone.
V_{EE}	8	**Negative Supply (Power Input).** This is the negative power supply for the device.
V_{CC}	9	**Positive Supply (Power Input).** This is the positive power supply for the device.
NEG 1, POS 1	10,11	**Detector 1 Analysis - Negative and Positive (Voltage Inputs).** These pins determine the sign of the transconductance gain from the differential detector input voltage (pins 12 and 13) and the current on the output of detector 1 (pin 7).
IN +, IN-	12,13	**Detector Input Negative and Positive (Voltage Inputs).** These pins form the differential voltage input to the phase detectors.
NEG 2, POS 2	14,15	**Detector 2 Analysis - Positive and Negative (Voltage Inputs).** These pins determine the sign of the transconductance gain from the differential detector input voltage (pins 12 and 13) and the current on the output of detector 2 (pin 16).
OUT 2	16	**Detector 2 Output (Current Output).** This is the output of phase detector 2. The current sunk or sourced at this pin is proportional to the differential voltage between the detector input pins (pins 12 and 13). The sign of the transconductance gain (i.e. of the constant of proportionality) is controlled by the detector 2 analysis pins (pins 14 and 15). The direction of the average current output is determined by the phase relationship between the input and the analysis pins and the magnitude is determined by the input alone.

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage (pin 9), V_{CC}	-0.3V to +10V
Negative supply voltage (pin 8), V_{EE}	-10V to +0.3V
Input voltages (pins 2,5,6,10,11, 12,13,14 and 15), V_I	V_{EE} to V_{CC}
Output voltages (pins 1,3,4,7,16), V_O	V_{EE} to V_{CC}
Cell voltage (pins 1,.3,4) minus Common voltage (pin 2), V_C	-5V to +5V
Storage temperature, T_{ST}	-10°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions - Voltages are with respect to digital ground (V_{DGND} [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage (pin 9)	V_{CC}	4.5	5	7.0	V
Negative supply voltage (pin 8)	V_{EE}	-7.0	-5	-4.5	V
Ambient temperature	T_{amb}	0		70	°C
Common cell pin voltage (pin 2)	V_{COM}	V_{EE} +2.7		V_{CC} -2	V
Cell input currents (pins 1,3 and 4)	I_{CELL}	-10		10	μA
X control voltage (pin 5)	V_X	V_{EE} +2.7		V_{EE} -6.0	V
Y control voltage (pin 6)	V_Y	-2.0		1.8	V
Detector input voltages (pins 12 and 13)	V_{IN}	V_{EE} +2.7		V_{CC} -2.7	V
Analysis input voltages (pins 10,11,14 and 15)	V_A	V_{EE} +2.7		V_{CC} -2.7	V
Detector output voltages (pins 7 and 16)	V_{OUT}	V_{EE} +2.5		V_{CC} -2	V

Operating Characteristics: General - Voltages are with respect to ground (V_{GND} = [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation	P_D			30	mW	
Supply current	I_{CC}		1.3	15	mA	
Pin capacitance	C_P		7	15	pF	Pin to supplies

Operating Characteristics: Cells - Voltages are with respect to ground (V_{GND} = [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Internal resistance (pins 1, 3 and 4)	R_I	3		14	kΩ	
Control input leakage (pins 5 and 6)	I_C			0.12	μA	
Minimum cell gain	G_{MIN}		0.05			
Maximum cell gain	G_{MAX}		10			
DC bias current (pin 2)	I_{BDC}	-12	0	12	μA	
Residual impedance (pin 2)	Z_R	500			kΩ	Cell pins open circuit

Operating Characteristics: Detectors - Voltages are with respect to ground (V_{GND} = [V_{CC} - V_{EE}]/2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Differential input offset (pins 10 to 15)	V_{DOFF}			13	mV	
Input offset current (pins 10 to 15)	I_{OFF}	-0.15		0.15	μs	
Input bias current (pins 10 to 15)	I_{IB}		0.1	0.7	μA	
Transconductance gain	G_T	250	500	1000	μΩ	Magnitude
Output offset current (pins 7 and 16)	I_{OFF}	-1.2		1.2	μA	
Maximum output current (pins 7 and 16)	I_{MAX}		50		μA	Sink or Source
Output impedance (pins 7 and 16)	Z_{OUT}		5		MΩ	

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

SL9901

50MHz TRANSIMPEDANCE AMPLIFIER

The SL9901 is a monolithic silicon integrated circuit designed to interface between a detector diode and a decoder in a Fibre Optic Receiver system.

FEATURES

- High Sensitivity
- 50MHz Bandwidth (100Mbits/NRZ Data Rate)
- Wide Dynamic Range
- 5 Volt Supply
- Usable in Systems with 10 $^{-9}$ BER at —36dBm Average Optical Power

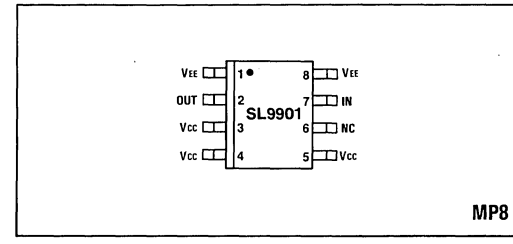


Fig.1 Pin connections - top view

APPLICATIONS

- Fibre Optic Data Links
- Nucleonics
- Instrumentation
- Current/Voltage Conversion

ORDERING INFORMATION

SL9901B MP (Industrial - Miniature Plastic DIL package)

ASSOCIATED PRODUCTS

SP9921 Decoder
SP9960 Encoder and LED Driver

CIRCUIT DESCRIPTION

The photocurrent generated by a PIN diode is converted to a voltage suitable for driving a comparator input stage in a decoder/detector circuit. The SL9901 has a 3dB electrical bandwidth of 50MHz enabling NRZ data rates of up to 100Mbit/s to be received.

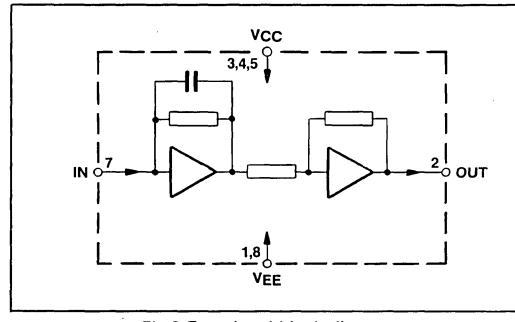


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage	V_{CC}	4.0	5	5.5	V
Ambient temperature	T_{amb}	-40		+85	°C
Input current (RMS) (Note 2)	I_I	0.3		10	μA
Output load	R_O			250	Ω

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The device is guaranteed to operate at up to 30 milliamps (RMS), but above 10 milliamps the output may be clipped with associated loss of gain and the mid-points of the output may be distorted by up to 3ns.

Characteristics - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation	P_D			100	mW	
Thermal resistance: chip to case	θ_{CC}		57	69	°C/W	
Thermal resistance: chip to ambient	θ_{CA}		163	196	°C/W	
Supply current	I_{CC}	9	12	16	mA	Output unloaded
Input bias voltage	V_{IB}		1.5	1.65	V	25°C
Input bias variation	$\delta V_{IB}/\delta T$		1.7	4	mV/°C	
Input impedance	Z_I		400		Ω	
Input current at clipping	I_{IC}	10			μA	
Input current noise (Note 2)	N_I		3.5	4	pA/√Hz	
Input voltage noise (Note 2)	N_V		3200	4000	pV/√Hz	
Transimpedance gain	G_T	30	40		kΩ	
Gain roll-off	G_R	6			dB/Oct.	f > 100MHz
3dB bandwidth (see Fig.3)	f_B	50			MHz	5pF on input
		26			MHz	30pF on input
Output impedance	Z_O		50	100	Ω	
Pin capacitance	C_P		1.5	2	pF	Pin to supplies

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The typical input voltage noise would create an equivalent input noise current of 0.12 microamps averaged over DC to 160MHz when the path is completed through an external 5pF input capacitance. The typical current noise source would create an equivalent input noise current of 0.04 microamps over DC to 160MHz.

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to the negative power supply (V_{EE})

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage, V_{CC}	0V to +7V
Input voltage (device sourcing current), V_I	0V
Input current (device sinking current), I_I	1mA
Output voltage (device sinking current), V_O	0V to V_{CC} -2V
Output current (device sourcing current), I_O	10mA
Storage temperature, T_{ST}	-55°C to +150°C
Relative humidity at 85°C, R_H	85%
Chip temperature - plastic package (Note 1), T_C	145°C

NOTE
1. Thermal conductivities from chip to case and to ambient are given in Electrical Characteristics.

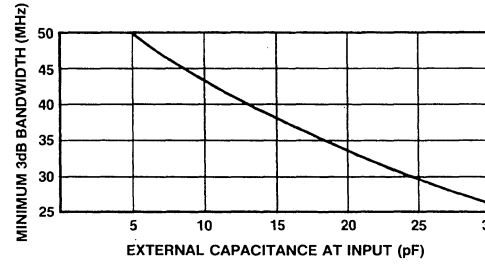
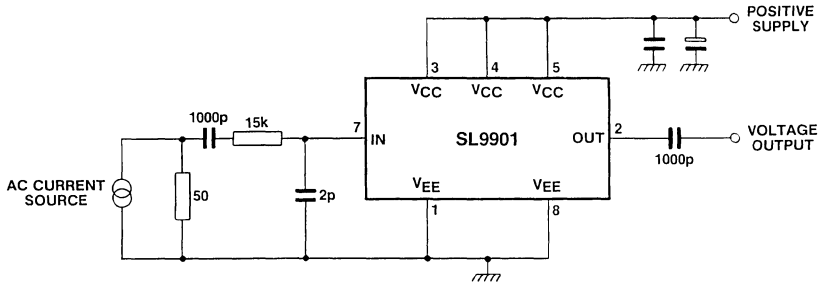


Fig.3 Minimum 3dB bandwidth against external capacitance at input



NOTE

For currents in the range 10μA to 30μA (RMS) a DC offset is added to prevent the input from sourcing current. This gives a better approximation to normal use (see Fig.5).

Fig.4 Test circuit

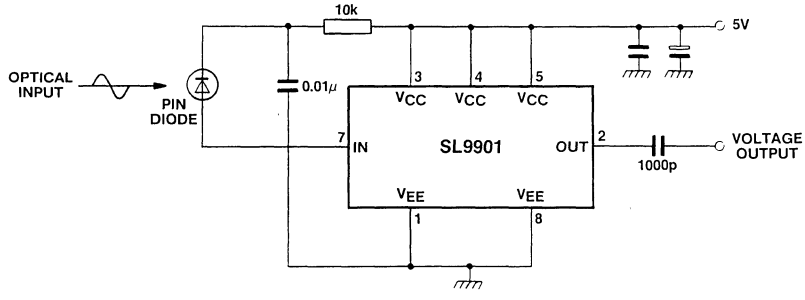


Fig.5 Typical application circuit

SP1404BW, D3702

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

The D3702 is a version of the SP1404BW in 14 pin plastic package approved to BT specification.

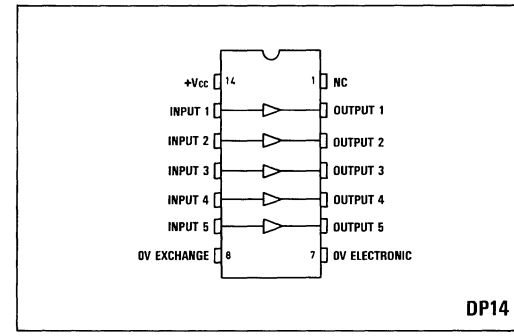


Fig.1 Pin connections (viewed from underside)

CIRCUIT DESCRIPTION (Fig.2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs as inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to (V_{CC} - 1) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

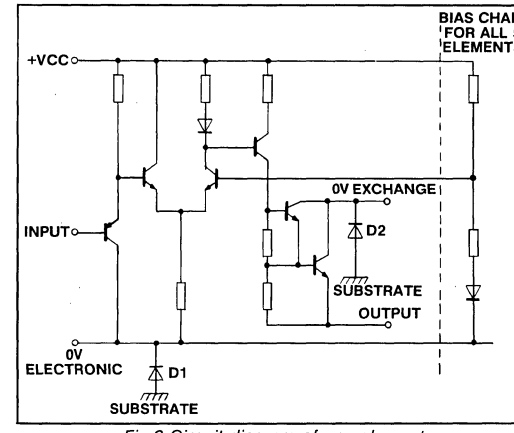


Fig.2 Circuit diagram of one element

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{OUT} = 50mA)	+85°C
Load current	80mA
Voltage between output and 'noisy earth'	-65V
V_{CC} to output voltage	75V
V_{CC} to electronic earth	7V
Input voltage	V_{CC} + 1V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature range = 0°C to +70°C, V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		-20		μA	V_{IN} = 0V
				μA	V_{IN} = V_{CC}
Output voltage			1.5	V	V_{IN} = 0.8V, I_{OUT} = 50mA
Output current (Off state)			100	μA	V_{IN} = 2V, V_{OUT} = -60V
Output current (On state)	50	80		mA	V_{IN} = 0.8V
V_{CC} supply current		30		mA	V_{CC} = 5V, all inputs low
Total power dissipation		450		mW	V_{CC} = 5V, all inputs low
					all outputs I_{OUT} = 50mA

PLESSEY
Semiconductors

SP1450B(B) & SP1455B(B)

PCM SIGNAL MONITOR CIRCUITS

The SP1450 and SP1455 are bipolar integrated circuits designed to monitor errors in three-level digital signals modulated by a three-alphabet 4B3T code such as MS43. They can also indicate the failure of positive or negative pulses in the signal. The high frequency capability allows operation in PCM systems up to 34M bit/s (SP1450) and 140M bit/s (SP1455). Facilities are provided to adjust input thresholds independently on each polarity of input and the error output can be interfaced with low speed CMOS circuitry or high speed ECL.

The SP1450B(B) and SP1455B(B) are similar to the SP1450B and SP1455B but are screened to MIL-STD-883, Method 5004, Class B.

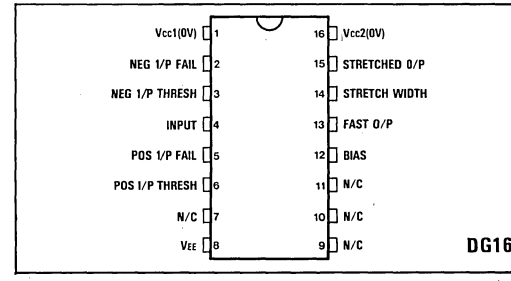


Fig.1 Pin connections (top view)

FEATURES

- Suitable for 34, 120 and 140M bit/s PCM
- Positive and Negative Input Signal Fail Outputs
- High Speed Error Output
- Low Speed 'Stretched' Output
- Low Power Consumption

APPLICATIONS

- PCM Telephone Transmission Terminal Equipment
- PCM Repeaters
- Error Checking Test Equipment

QUICK REFERENCE DATA

- Supply Voltage -4.4V to -5.25V
- Operating Temperature Range -10°C to +70°C
- Power Consumption 100mW typ
- Input Voltage Range ±450mV to ±1100mV (SP1450)
  ±450mV to ±600mV (SP1455)
- Thermal Resistance θj-a 100°C/W

ABSOLUTE MAXIMUM RATINGS

Supply voltage -8V
Reverse input current (pin 4) 5mA (continuous) 20mA (10us max)
Forward input current (pin 4) 20mA (10us max)
Storage temperature -55°C to +150°C
Operating temperature -10°C to +70°C
Junction temperature 150°C

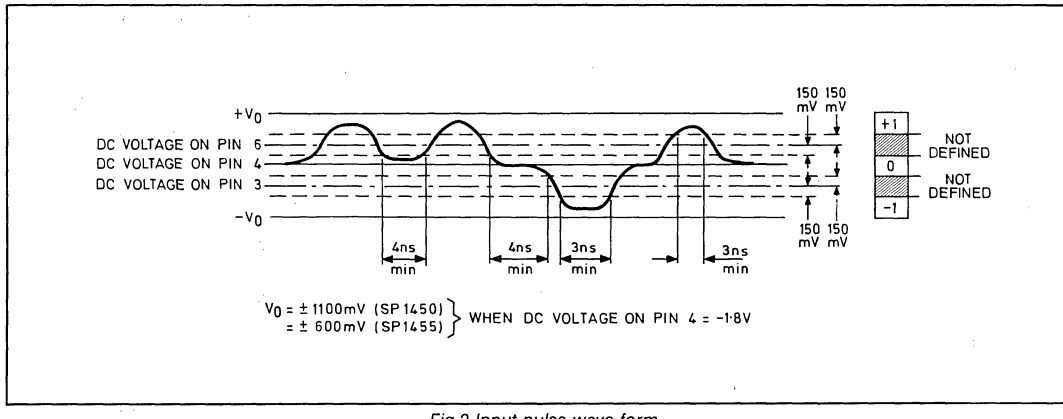


Fig.2 Input pulse wave form

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = Pins 1-16 = 0V, V_{EE} = Pin 8 = -5.0V, T_{amb} = +25°C, Input voltage range (pins 3,4,6) = -0.9V to -3.1V

DC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output low, current	2	0.9	1.2	1.9	mA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2.0V
Output low, current	2	0.7	—	—	mA	Pin 2 = OV Pin 3 = —1.95V Pin 4 = —2.0V
Output high, current	2	—	—	1	µA	Pin 2 = OV Pin 3 = —2.3V Pin 4 = —2.0V
Output high, current	2	—	—	0.4	mA	Pin 2 = OV Pin 3 = —2.05V Pin 4 = —2.0V
Output low, current	5	0.9	1.2	1.9	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.3V
Output low, current	5	0.7	—	—	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.05V
Output high, current	5	—	—	1	µA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.7V
Output high, current	5	—	—	0.4	mA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.95V
Output low, current	13	6.0	7.0	9.0	mA	Pin 13,15 = OV Pin 3 = —1.7V Pin 4 = —2.0V Pin 6 = —2.3V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V Six pos. or neg. pulses on pin 4
Output high, current	15	—	—	1	µA	
Output high, current	13	—	—	1	µA	Pin 13, 15 = OV Pin 3 = —2.3V Pin 4 = —2.0V Pin 6 = —1.7V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V
Output low, current	15	0.5	0.75	—	mA	
Current consumption	1,16	—	20	25	mA	(Pins 2,5,13,15 = OV (Pins 3,6 = —2.3V (Pin 4 = —2.0V (27 kΩ resistor between (Pin 14 and —5V (Pin 12 open
Input bias current	3	—	—	40	µA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2V
Input bias current	6	—	—	40	µA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —1.7V
Input bias current	4	—	—	80	µA	Pins 2,5 = OV Pins 3,6 = —2.3V Pin 4 = —2.0V

AC CHARACTERISTICS

Circuit reference: Fig.3, Input signal: Fig.2, T_{amb} = -10°C to +70°C, V_{EE} = -4.4V to -5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Input Frequency						
SP1450	13		—	25.5	M band/s	See note 1 below
SP1455	13		—	105	M band/s	See note 1 below
Stretched output pulse width	15	0.5	0.7	2	µS	c_1 = 390 pF R_1 = 27 kΩ using circuit of Fig. 7 (see note 2 below)
Error pulse width SP1455	13	4.25	—	5.25	nS	Input freq. 105 M band/s
Error pulse amplitude	13	300	—	—	mV	At max input frequency
Spurious pulse amplitude	13	—	—	50	mV	At max. input frequency

NOTE 1: These figures are the max.input symbol rates. For 4B3T codes, the effective bit rate is 4/3 x (input frequency).

NOTE 2: Resistor and capacitor values quoted are absolute values; temperature coefficients and tolerances have not been taken into account.

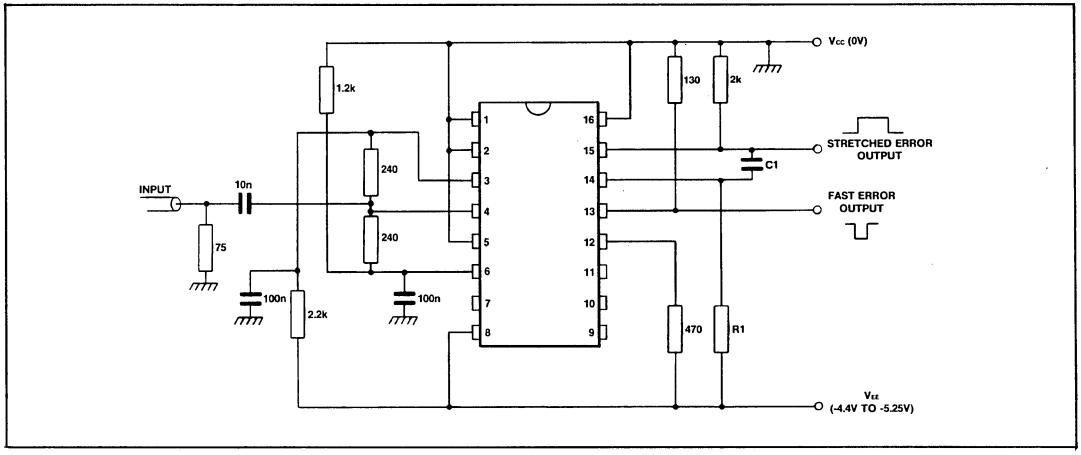


Fig.3 Functional test circuit

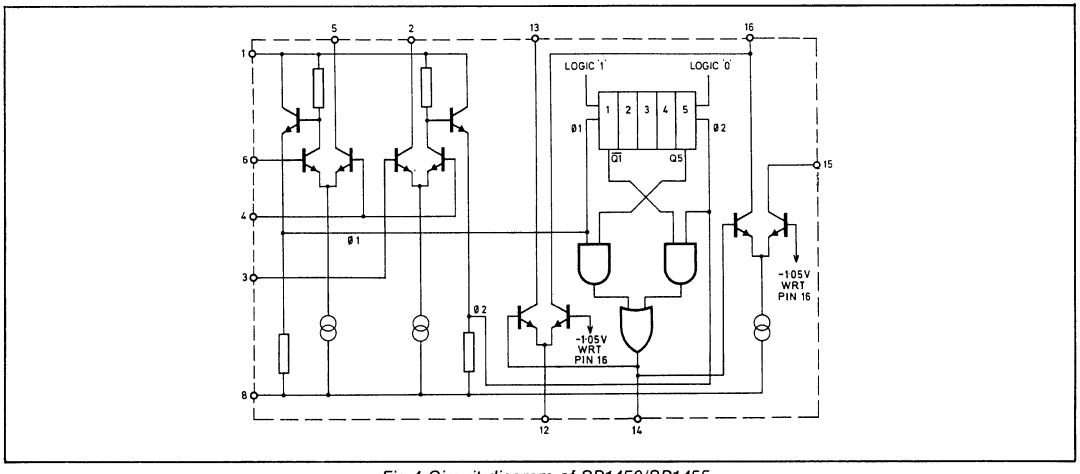


Fig.4 Circuit diagram of SP1450/SP1455

APPLICATIONS

The circuit shown in Fig.3 is designed to accept a three level (ternary) input signal as shown in Fig.2. The input is applied to pin 4 whilst fixed bias levels are maintained on pins 3 and 6. When a positive input pulse is applied at a level more positive than the bias on pin 6 the positive comparator output o 1 goes from '0' (V_{EE}) to '1' (V_{CC}). The 1-0 edge of this pulse clocks the five bit shift register one place to the right. Repeated operation will cause a pattern of logic '1's to be propagated along the shift register. When bit 5 is at logic '1' and the input is also positive an 'error' will occur at pins 13 and 15.

A negative input pulse at a level more negative than the voltage on bias pin 3 causes the negative comparator output o 2 to clock the shift register one place to the left. Repeated operation causes a pattern of logic '0's to be propagated along the shift register. When bit 1 is at logic '0' and the input is also negative an 'error' output will again occur at pins 13 and 15.

During normal operation the shift register can assume one of only six possible states as shown in Fig.5.

State	1	2	3	4	5
A	0	0	0	0	0
B	1	0	0	0	0
C	1	1	0	0	0
D	1	1	1	0	0
E	1	1	1	1	0
F	1	1	1	1	1

Fig.5 Shift register states

When power is initially connected other states may occur.

Two 'error' outputs are available. The fast output at pin 13 is negative going; the peak current is defined by a resistor connected between pin 12 and V_{EE} according to the formula:

$$I = \frac{3.3}{R} \text{ (e.g. 820 ohms; 4mA)}$$

A pullup resistor must then be connected between pin 13 and V_{CC} to give a suitable voltage swing. A suitable ECL interface is shown in Fig.6.

If, as in a repeater application, a fast output is not required, pin 12 should be left open and pin 13 connected to V_{CC} (pin 16).

A stretched output is available from pin 15 by connection of a capacitor between pins 14 and 15. A suitable circuit is shown in Fig.7.

Facilities are available at pins 2 and 5 to detect the absence of negative and positive going input signals. If these are not required pins 2 and 5 should be connected to V_{CC} (pin 1). A CMOS interface circuit is shown in Fig.8.

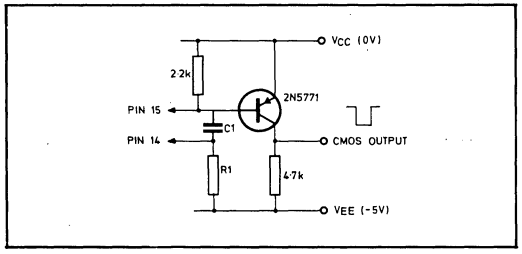


Fig.7(a) Interfacing with CMOS at the stretched output (SP1450)

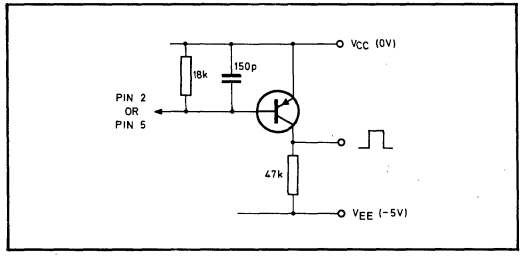


Fig.8 Interfacing with pulse fail output with CMOS

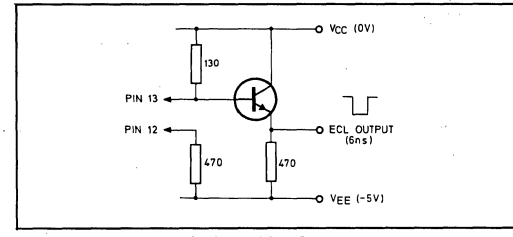


Fig.6 Interfacing with ECL at the output

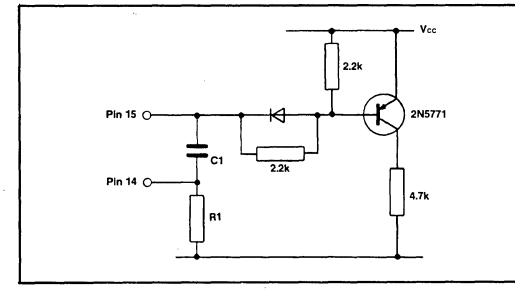


Fig.7(b) Interfacing with CMOS at the stretched output (SP1455)

SP9921

50 MBIT MANCHESTER BIPHASE-MARK DECODER

The SP9921 is a bipolar monolithic silicon integrated circuit for clock and data recovery from a Manchester biphase-mark encoded input signal. It operates from a single 5V supply and has ECL outputs.

FEATURES

- 20 to 50Mbit/s Operating Range
- Single Supply Voltage
- Sensitive Differential Input
- ECL Outputs
- Input Signal Detection from Lock Detect Output
- No False Frequency Lock

APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface

ORDERING INFORMATION

SP9921B DG (Industrial - Ceramic DIL package)
SP9921B LC (Industrial - LCC package)

ASSOCIATED PRODUCTS

SL9901 Transimpedance Amplifier
SP9960 Encoder and LED Driver

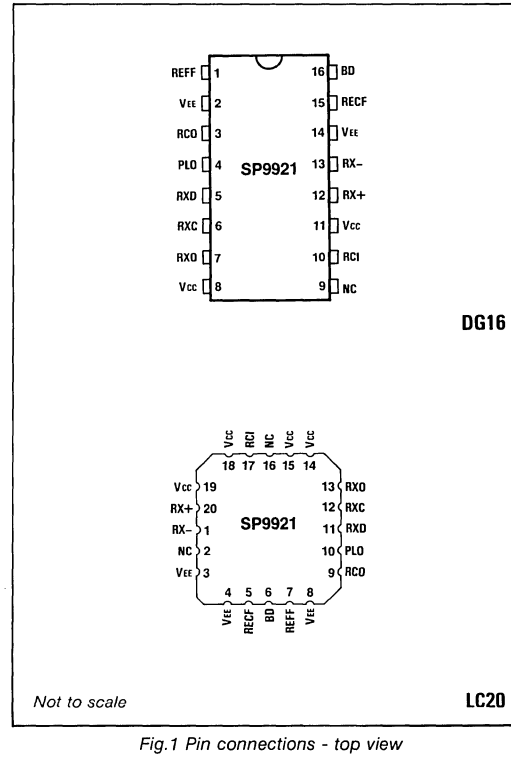


Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the device. It locks onto incoming data, recovers the clock and decodes the data making use of a reference clock input at approximately one fifth of the data rate.

Receive Path

Data is received at the differential input pins (RX + and RX-) of the limiting amplifier which outputs the digital received signal for monitoring at the amplifier output pin (RXO). This signal is fed into a Costas loop which outputs the recovered clock (RXC pin) and the decoded data (RXD pin).

Fig.3 shows how the input signal is decoded. The Manchester biphase-mark code uses a transition at the centre of the bit to indicate a one and the absnece of a transition to indicate a zero. In addition there is always a transition at the end of the bit.

Phase-Locking and Signal Recovery

The SP9921 can be used in systems operating over a wide range of data rates without false frequency lock. This is achieved using a reference VCO and a recovery VCO.

The reference VCO is phase-locked to the reference clock input (RCI pin). This generates an internal clock at 5 times the frequency of the reference clock input. The output of this VCO is output for monitoring on the reference clock output (RCO pin). Filtering of the bias control signal to the VCO is performed at the reference filter pin (REFF).

The bias control signal for the reference VCO is filtered at the bias decoupling pin (BD) and used to set the free-running frequency of the recovery VCO. The recovery VCO drives the receive clock (RXC pin) and the modulators which in turn drive the integrators. The integrators analyse the components of the signal which are in phase and 90° out of phase and so obtain the recovered data and the correction signal for the Costas loop. The correction signal is filtered at the recovery filter pin (RECF).

The modified Costas loop also pulls the phase-lock output pin (PLO) low for any bits when the output of the in-phase integrator (data) does not exceed the output of the out-of-phase integrator (error) by a set margin. This can occur when there is a loss of data, if there is enough noise on the link (even if not data is corrupted) or if the Costas loop has difficulty locking.

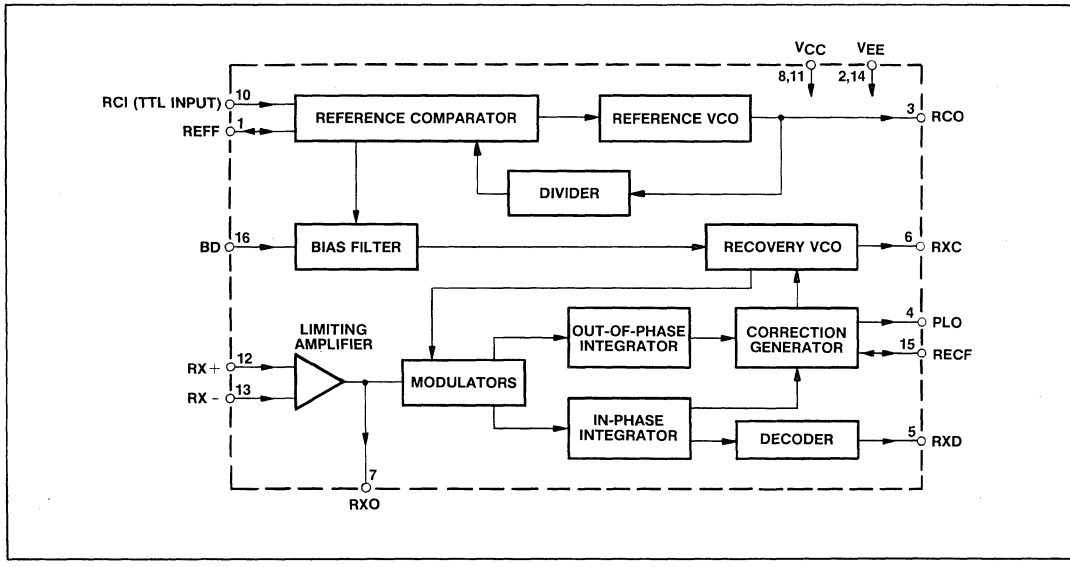
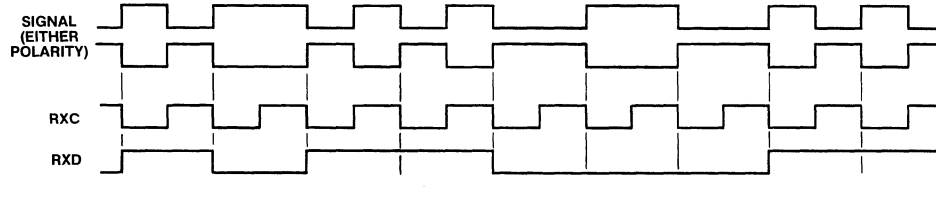


Fig.2 Functional block diagram (DG package pin out)



N.B. There is a delay of 3 clock cycles between the input signal and the decoded data.

Fig.3 Biphase-mark decoding

PIN DESCRIPTIONS

Symbol	Pin No.		Pin name and description
	DG	LC	
REFF	1	7	**Reference Filter (Current Output/Voltage Input).** A series RC network should be connected between this pin and ground (V_{EE}) to provide the filtering for the control of the reference VCO.
V_{EE}	2	8	**Negative Supply (Power Input).** 0V.
RCO	3	9	**Reference Clock Out (ECL Output).** This pin should output a clock which is phase-locked to the reference clock input (RCI pin) but which is 5 times its frequency.
PLO	4	10	**Phase Lock Out (ECL Output).** This pin goes low for any bits where the output of the in-phase integrator (data) fails to exceed the output of the out-of-phase integrator (error) by a set margin.
RXD	5	11	**Received Data (ECL Output).** This pin outputs the decoded received data.
RXC	6	12	**Received Clock (ECL Output).** This pin outputs the recovered clock.
RXO	7	13	**Receive Out (ECL Output).** This pin otputs the undecoded received data.
V_{CC}	8	14,15	**Positive Supply (Power Input).** 5V.
NC	9	16,2	**No Connection.** This pin should be left unconnected for normal operation.
RCI	10	17	**Receive Clock In (TTL Input).** This is the input for the reference clock which sets the free-running frequency for the recovery VCO. Its frequency should be close to one fifth of the received data rate.
V_{CC}	11	18,19	**Positive Supply (Power Input).** 5V.
RX +, RX-	12,13	20,1	**Receive Plus and Minus (Analog Voltage Inputs).** These are the differential inputs to the limiting receive amplifier. They are self-biasing and would normally be capacitively coupled. For a single-ended input the unused pin should be capacitively coupled to ground.
V_{EE}	14	3,4	**Negative Supply (Power Input).** 0V.
RECF	15	5	**Recovery Filter (Current Output/Voltage Input).** A series RC network should be connected between this pin and ground (V_{EE}) to provide the filtering for the control of the recovery VCO.
BD	16	6	**Bias Decoupling (Decoupling Node).** A capacitor should be connected between this pin and ground (V_{EE}) to eliminate noise on the bias voltage generated by the reference PLL and which sets the free-running frequency of the recovery VCO.

ELECTRICAL CHARACTERISTICS

Test Conditions - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage	V_{CC}	4.5		5.5	V
Case temperature - DG Package	T_{CASE}	-40		+140	°C
- LC Package		-40		+155	
Ambient temperature - DG Package	T_{amb}	-40		+70	°C
- LC Package		-40		+85	
Relative humidity	H_R			85	%
TTL input low voltage	V_{ILT}	0	0.4	0.8	V
TTL input high voltage	V_{IHT}	2.0	2.4	V_{CC}	V
Operating frequency	f_{OP}	20		50	MHz
Differential receive voltage (peak to peak)	V_{RD}	10		2000	mV

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Static Characteristics - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation	P_D			700	mW	
Thermal resistance: chip to case						
DG Package	θ_{CC}		22	27	°C/W	
LC Package			22	27		
Thermal resistance: chip to ambient						
DG Package	θ_{CA}		95	114	°C/W	
LC Package			73	88		
Supply current	I_{CC}		100		mA	Outputs unloaded
TTL input sink current	I_T			10	μA	$0 < V < V_{CC}$
ECL output high voltage (Note 2)	V_{OH}	$V_{CC}-1.06$		$V_{CC}-0.89$	V	-30°C (Note 3)
		$V_{CC}-0.96$		$V_{CC}-0.81$		+25°C
		$V_{CC}-0.89$		$V_{CC}-0.70$		+85°C
ECL output high source current	I_{OH+}	10			mA	$V < V_{OH}$ (Min)
ECL output high sink current	I_{OH-}	2			mA	$V > V_{OH}$ (Max)
ECL output low voltage (Note 2)	V_{OL}	$V_{CC}-1.89$		$V_{CC}-1.68$	V	-30°C (Note 3)
		$V_{CC}-1.85$		$V_{CC}-1.65$		+25°C
		$V_{CC}-1.83$		$V_{CC}-1.62$		+85°C
ECL output low source current	I_{OL+}	10			mA	$V < V_{OL}$ (Min)
ECL output low sink current	I_{OL-}	2			mA	$V > V_{OL}$ (Max)
Receive offset voltage	V_{RO}	-2.5		2.5	mV	
Receive bias voltage	V_{RB}		$V_{CC}/2$		mV	
Receive input impedance	Z_{RI}	700	1000	1300	Ω	Differential input
Pin capacitance - DG Package	C_P		7	10	pF	Pin to supplies
- LC Package			2	3		

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. $V_{RX+} - V_{RX-} > 100mV$ to ensure a good ECL output on RXO.
3. These are ambient temperatures.

Reference Clocks Timing (see Figs.4 and 5)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
RCI frequency	f_R	3.9		10.1	MHz	
RCI rise time	t_{RR}		20		ns	
PCM clock high period	t_{RH}	20			ns	
RCI fall time	t_{RF}		20		ns	
PCM clock low period	t_{RL}	20			ns	
RCO rise or fall time	t_{RRF}			4	ns	$R_L = 1k\Omega$; $C_L = 10pF$

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

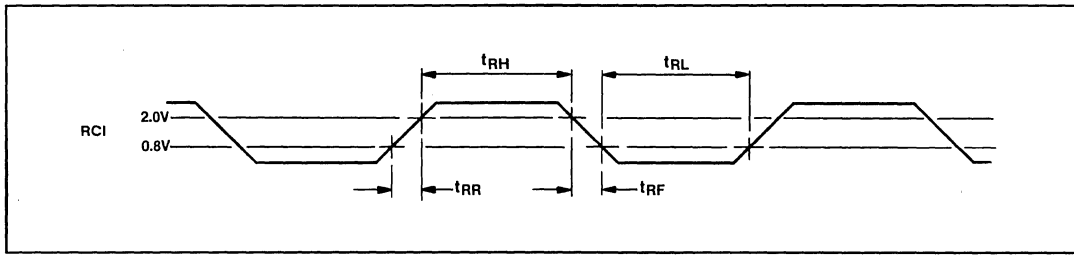


Fig.4 Timing - reference clock in

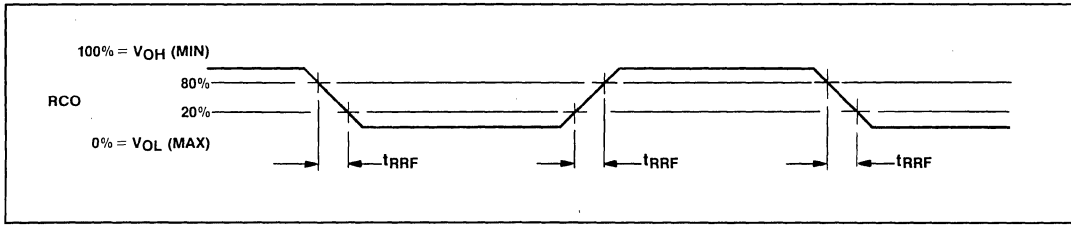


Fig.5 Timing - reference clock out

Reference Loop Characteristics - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
RCO frequency (see Fig.6)	f_{RCO}		18		MHz	V_{REFF} = 2.5
			46			V_{REFF} = 3.0
			54			V_{REFF} = 3.5
Reference loop gain (see Fig.7)	G_{REF}		40		MHz/V	f_{OP} = 20MHz
			100			f_{OP} = 30MHz
			55			f_{OP} = 40MHz
			20			f_{OP} = 50MHz
REFF source current pulse (Note 2)	I_{RF-}	100	250	350	μA	
REFF sink current pulse (Note 2)	I_{REF-}	100	250	350	μA	

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The device outputs a sink or source current pulse on every cycle of the RCI clock. The pulse duration is equal to the interval between the edges of the clocks being compared and its direction (sink or source) is determined by which edge is first.

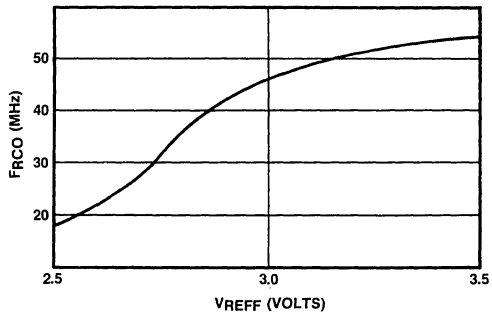


Fig.6 Typical reference VCO characteristic

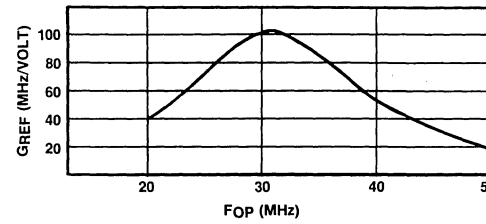


Fig.7 Typical reference loop gain characteristic

Receive Data Timing (see Fig.8)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Mean bit period	t_B		$1/f_{RCO}$		ns	
Minimum half period	t_{MIN}	$0.3t_B$			ns	
Maximum half period	t_{MAX}			$0.7t_B$	ns	

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

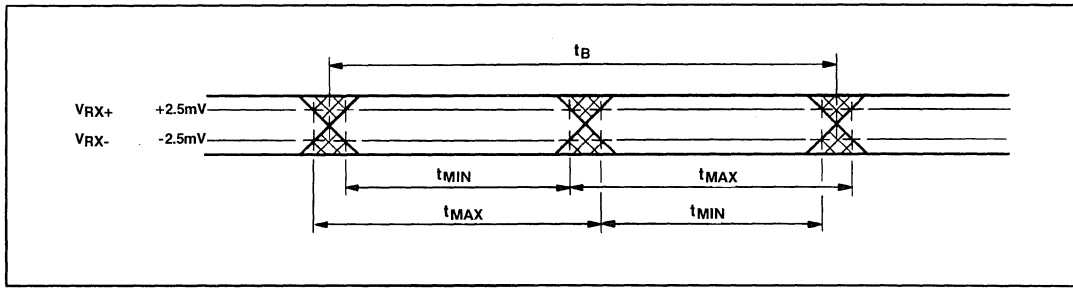


Fig.8 Timing - receive data

Recovery Loop Characteristics - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Reference voltage (REFC)	V_R		$V_{CC}-1$		V	
Operating voltage (REFC)	V_{OP}	$V_R-0.33$		$V_R+0.33$	V	
Free-running voltage (REFC)	V_{FR}	$V_R-0.33$		$V_R+0.33$	V	
Free-running frequency offset (w.r.t. f_{RCO})	Δ_{FR}	-5		5	%	
Current-phase ratio (Note 2)	$\alpha_{I/PH}$		115		μA/rad.	Averaged
Impedance to V_{FR} at REFC	R_P	5	10		kΩ	
Frequency-voltage ratio	$\alpha_{F/V}$		8.5		MHz/V	f_{RCO} = 50MHz
			9.5			f_{RCO} = 40MHz
			11			f_{RCO} = 30MHz
			6.5			f_{RCO} = 20MHz
Lock-on range (w.r.t. f_{RCO})	Δ_L	-5		5	%	

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The device outputs a sink or souce current pulse on every cycle of the RXC clock. The pulse is proportional to the phase difference between the edges of the RXC clock and of the incoming data, up to a limit of a quarter cycle. Although the pulse lasts for half of the clock cycle, the figure shown here is the value averaged over the cycle.

Receive Outputs Timing (see Figs. 9 and 10)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
RXC fall time	t_{RXF}			4	ns	$R_L = 1k\Omega$; $C_L = 10pF$
RXC rise time	t_{RXR}			4	ns	$R_L = 1k\Omega$; $C_L = 10pF$
Output hold time	t_{OH}	0			ns	$R_L = 1k\Omega$; $C_L = 10pF$
Output delay	t_{RR}		3	5	ns	$R_L = 1k\Omega$; $C_L = 10pF$

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

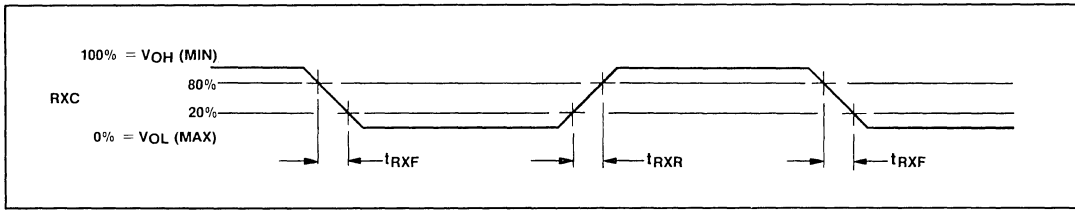


Fig.9 Timing - receive clock

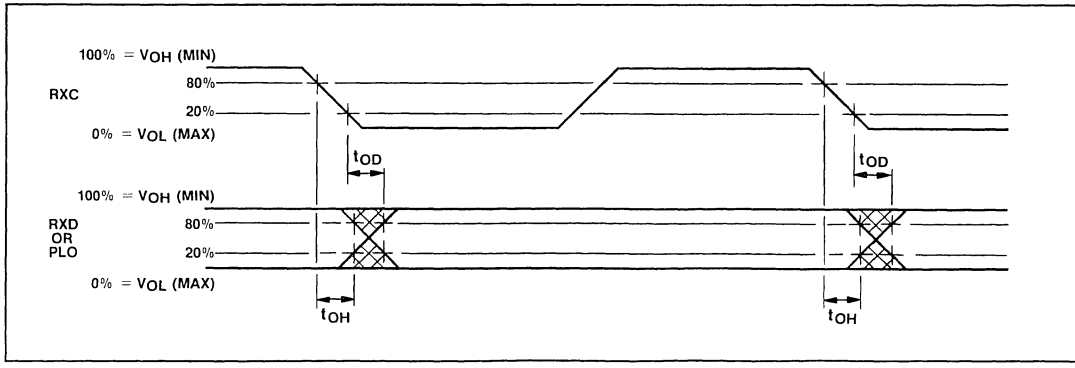


Fig.10 Timing - receive data and phase lock out

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to ground (V_{EE})

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage, V_{CC}	0V to +7V
Input voltage, V_I	-0.3V to V_{CC} +0.3V
Output voltage, V_O	0V to V_{CC}
Storage Temperature, T_{ST}	-55°C to +125°C
Relative humidity at 85°C, R_H	85%
Chip temperature (Note 1), T_C	+175°C

NOTE

1. Thermal conductivities from chip to case and ambient are given in Electrical Characteristics.

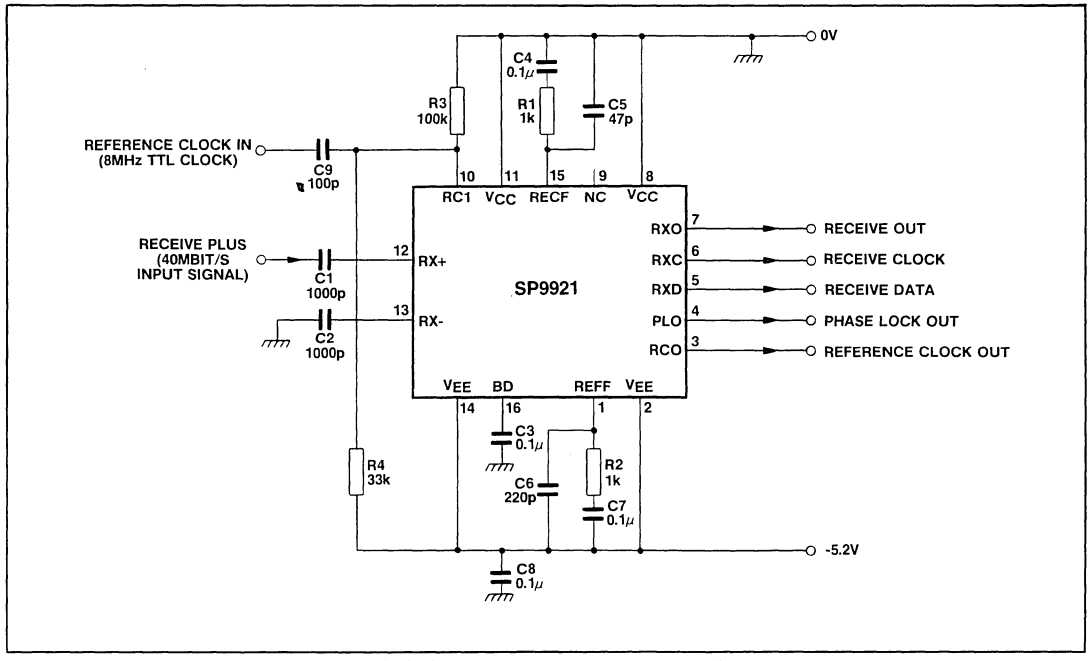


Fig.11 Typical application circuit (DG package pin out)

SP9960

50 MBIT MANCHESTER BIPHASE-MARK ENCODER AND LED DRIVER

The SP9960 is a Manchester biphase-mark encoder and LED driver, designed for use in fibre-optic links at up to 50Mbit/s.

It encodes TTL or ECL data and outputs the result as a current at either the large or the small LED driver output. The LED driver and the current output are selectable.

FEATURES

- Up to 50Mbit/s Operation
- TTL or ECL Inputs
- Choice of LED Drivers - Large or Small
- Choice of LED Drive Currents
- LED Driver Enable Control
- Single Supply Voltage

APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface

ORDERING INFORMATION

SP9960B DG (Industrial - Ceramic DIL package)
SP9960B LC (Industrial - LCC package)

ASSOCIATED PRODUCTS

SP9921 Decoder
SL9901 Transimpedance Amplifier

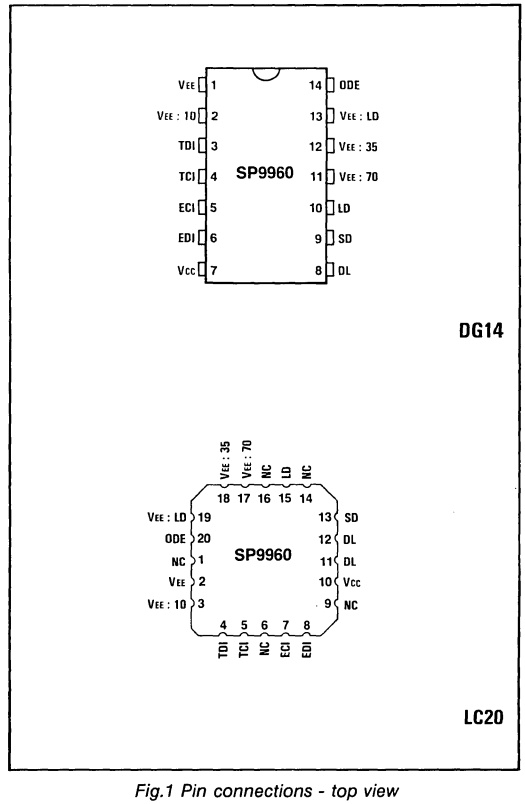


Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the device. Data arriving at a data input (TDI or EDI pin) is sampled by the positive edge of the appropriate clock (TCI or ECI pin), encoded into a biphase-mark signal, and output as a current at the chosen LED driver (SD or LD pin).

If TTL inputs are to be used (TDI and TCI pins) then the ECL inputs (EDI and ECI) should be left unconnected and vice versa.

Biphase-Mark Encoding

Fig.3 shows how the biphase-mark encoding scheme works. The input data is sampled by the positive edge of the clock. If the data is high (logic 1) then the driver switches to its opposite state (i.e. off if it was previously on, or on if it was previously off). If the data is low (logic 0) then the driver does not switch to its opposite state on the positive clock edge.

Regardless of the sampled input data, the driver always switches to its opposite state on the negative edges of the clock.

This form of encoding ensures a high number of transitions in the signal which simplifies the task of clock recovery at a remote detector. Since the data is encoded in terms of transitions, rather than as absolute levels, the signal can be given a net inversion without corrupting the information carried.

LED Drivers

There are two LED driver outputs, the small driver (SD pin) and the large driver (LD pin). The driver used is chosen by the V_{EE} : LD pin, which should be tied to the V_{EE} pin to select the large driver and left unconnected to select the small driver.

The small driver outputs either 15 or 25mA (typically) when on. If the V_{EE} : 10 pin is tied to V_{EE} then the output is boosted by 10mA to 25mA. If the V_{EE} : 10 pin is unconnected then the output remains at 15mA.

The large driver outputs 45, 80, 115 or 150mA (typically) when on. If the V_{EE} : 35 pin is tied to V_{EE} then the output is boosted by 35mA and if the V_{EE} : 70 pin is tied to V_{EE} then it is boosted by 70mA. If both these pins are left unconnected then the output remains at 45mA.

When the LED driver is off then current is switched to the dummy load pin (DL) which is normally connected to the positive supply via the dummy load resistor. This reduces the ringing which could otherwise occur on switching relatively large currents.

The drivers are disabled by pulling the ODE pin low. they are enabled if the ODE pin is left unconnected or pulled high.

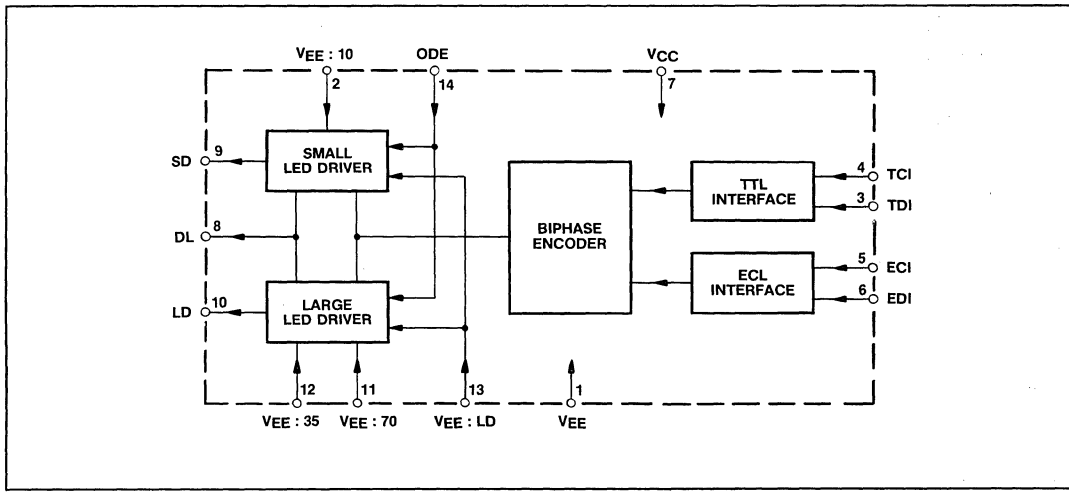
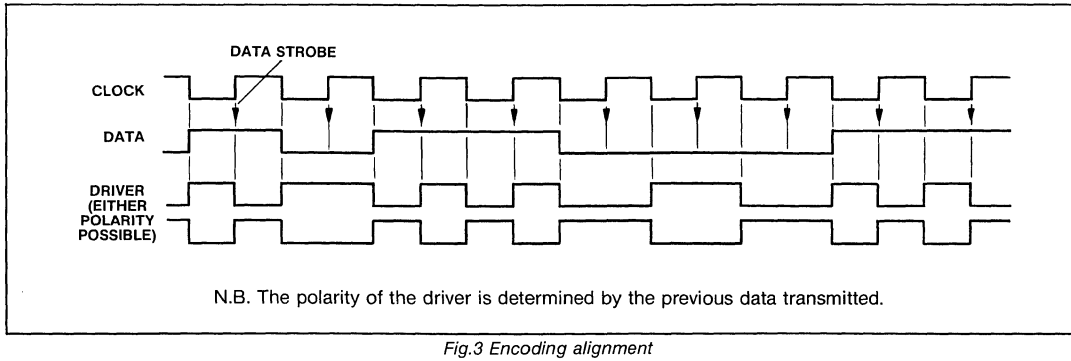


Fig.2 Functional block diagram (DG package pin out)



N.B. The polarity of the driver is determined by the previous data transmitted.

Fig.3 Encoding alignment

PIN DESCRIPTIONS

Symbol	Pin No.		Pin name and description
	DG	LC	
V_{EE}	1	2	**Negative Supply (Power Input).** This pin is normally tied to 0V for TTL operation or to -5.2V for ECL operation.
V_{EE} : 10	2	3	**10mA Negative Supply (Power Input).** This pin should be tied to the negative supply (V_{EE}) to increase the current at the small current LED output driver (SD pin) by 10mA (typically) if the small driver is selected. It should be left unconnected otherwise.
TDI	3	4	**TTL Data Input (TTL Input with Internal Pull-down).** Transistor-transistor logic (TTL) data is strobed in at this pin by the positive edges of the TTL clock input (TCI pin). This pin should be left unconnected if the TTL inputs are not to be used.
TCI	4	5	**TTL Clock Input (TTL Input with Internal Pull-down).** The rising edge of this clock is used to strobe the TTL data input (TTI pin). This pin should be left unconnected if the TTL inputs are not to be used.
ECI	5	7	**ECL Clock Input (ECL Input with Internal Pull-down).** The rising edge of this clock is used to strobe the ECL data input (EDI pin). This pin should be left unconnected if the ECL inputs are not to be used.
EDI	6	8	**ECL Data Input (ECL Input with Internal** data is strobed in at this pin by the positive edges of the ECL clock input (ECI pin). This pin should be left unconnected if the ECL inputs are not to be used.
V_{CC}	7	10	**Positive Supply (Power Input).** This pin is normally tied to 5V for TTL operation or to 0V for ECL operation.
DL	8	11,12	**Dummy Load (Current Sink Output).** Current is switched between this pin and the selected LED driver (SD or LD) to reduce ringing. It should be connected to the positive supply via the dummy load resistor which should be chosen to give a 1V drop when the current is on.
SD	9	13	**Small Driver (Current Sink Output).** This is the small current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the large driver negative supply pin (V_{EE} : LD) is left unconnected.
LD	10	15	**Large Driver (Current Sink Output).** This is the large current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the large driver negative supply pin (V_{EE} : LD) is tied to the negative supply (V_{EE}).
V_{EE} : 70	11	17	**70mA Negative Supply (Power Input).** This pin may be used in conjunction with the V_{EE} : 35 pin. It should be tied to the negative supply (V_{EE}) to increase the current sunk at the large current LED output driver (LD pin) by 70mA (typically) if the large driver is selected. It should be left unconnected otherwise.
V_{EE} : 35	12	18	**35mA Negative Supply (Power Input).** This pin may be used in conjunction with the V_{EE} : 70 pin. It should be tied to the negative supply (V_{EE}) to increase the current sunk at the large current LED output driver (LD pin) by 35mA (typically) if the large driver is selected. It should be left unconnected otherwise.
V_{EE} : LD	13	19	**Large Driver Negative Supply (Power Input).** This pin should be tied to the negative supply (V_{EE}) if the large current LED output driver (LD pin) is to be used. It should be left unconnected if the small current LED output driver (SD pin) is to be used.
ODE	14	20	**Output Driver Enable (Programming Input with Internal Pull-up).** This pin should be left unconnected for normal operation. If it is low then the LED output driver is disabled.

ELECTRICAL CHARACTERISTICS

Test conditions - Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage	V_{CC}	4.5		5.5	V
Case temperature	T_{CASE}	-40		Note 2	°C
Ambient temperature	T_{amb}	-40		Note 2	°C
Programming input low voltage	V_{ILP}	0		0.4	V
Programming input high voltage	V_{IHP}	2.0		V_{CC}	V
TTL input low voltage	V_{ILT}	0	0.4	0.8	V
TTL input high voltage	V_{IHT}	2.0	2.4	V_{CC}	V
ECL input low voltage	V_{ILE}	0		V_{CC} -1.65	V
ECL input high voltage	V_{IHE}	V_{CC} -0.96		V_{CC}	V

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The maximum temperatures depend on the selected LED drive current. The limits are found by derating the limit of chip temperature (given in Absolute Maximum Ratings) by the temperature difference due to the power dissipation and the thermal resistance to case or ambient (given in Electrical Characteristics).

Static Characteristics - Voltage are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation	P_D			Note 2	mW	
Thermal resistance: chip to ambient	θ_{CC}					
DG Package			22	27	°C/W	
LC Package			22	27		
Thermal resistance: chip to ambient	θ_{CA}					
DG Package			95	114	°C/W	
LC Package			73	88		
Supply current (Note 2)	I_{CC}		25	40	mA	Outputs disabled
Programming input current	I_P			10	mA	$0 < V < V_{CC}$
TTL input current	I_T			130	μA	$0 < V < V_{CC}$
ECL input current	I_E			250	μA	$0 < V < V_{CC}$
Small driver on current (sink)(Note 2)	I_{SD}	12	15	18	mA	$1 < V < V_{CC}$, default
		20	25	30		+10mA
Large driver on current (sink)(Note 2)	I_{LD}	36	45	54	mA	$1 < V < V_{CC}$, default
		64	80	96		+35mA
		92	115	138		+70mA
		130	150	180		+105mA
Driver off leakage (sink)	I_L			100	μA	$0 < V < V_{CC}$
Pin capacitance	C_P		7	15	pF	Pin to supplies

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The maximum power dissipation depends on the selected output drive current. It is always less than the product of the supply voltage with the sum of the maximum driver current (either I_{SD} or I_{LD}) and the maximum current with drivers disabled (I_{CC}).

Digital Switching Characteristics (see Figs.4 and 5)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Operating clock frequency	f_C			60	MHz	
Clock high period	t_{CH}	5			ns	
Clock low period	t_{CL}	5			ns	
Input data set-up time	t_{IS}	5			ns	
Input data hold time	t_{IH}	5			ns	
Output data hold time	t_{OH}	0			ns	
Output data delay	t_{OD}		15	30	ns	
Output rise or fall time	t_{ORF}			2	ns	
1st half cycle period	t_{1CP}	$t_{CL}-2$			ns	
2nd half cycle period	t_{2CP}	$t_{CH}-2$			ns	

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to the negative power supply (V_{EE})

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage, V_{CC}	0V to +7V
Input voltage, V_I	-0.3V to V_{CC} +0.3V
Output voltage, V_O	0V to V_{CC} +0.3V
Storage temperature, T_{ST}	-55°C to +125°C
Relative humidity at 85°C, R_H	85%
Chip temperature (Note 1) T_C	+175°C

NOTE
1. Thermal conductivities from chip to case and to ambient are given in Electrical Characteristics.

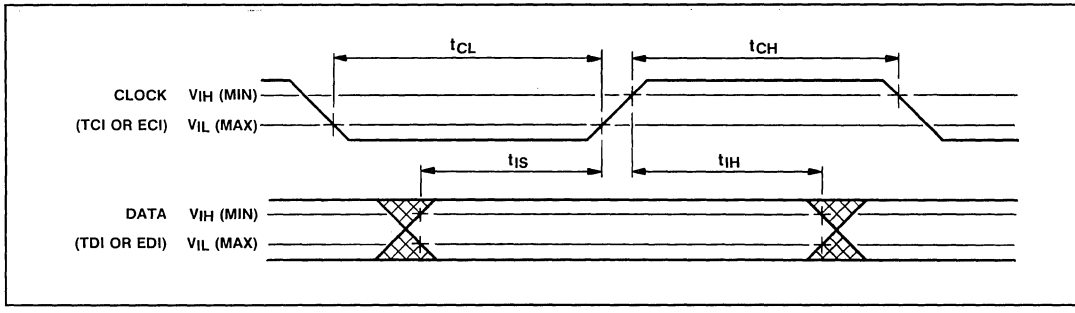


Fig.4 Digital switching characteristics - input

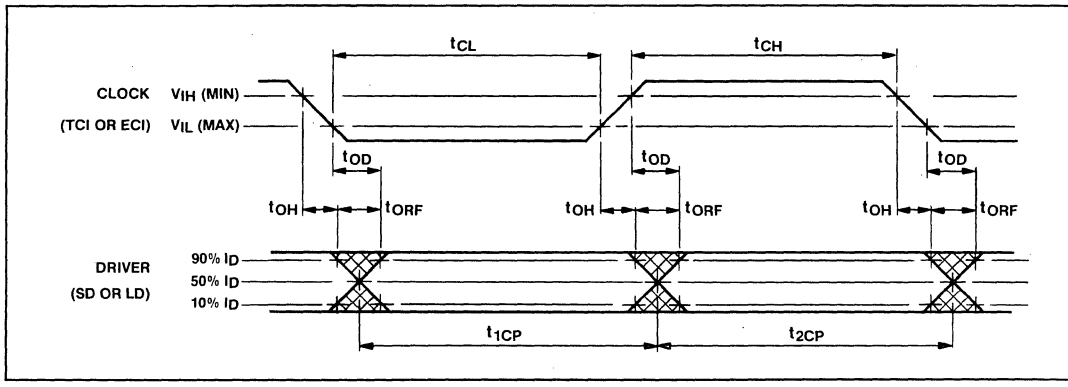


Fig.5 Digital switching characteristics - output

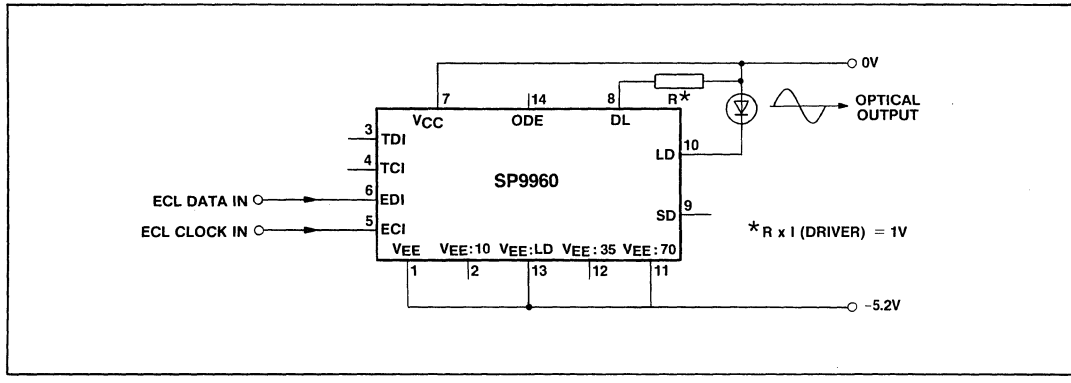


Fig.6 Typical ECL application circuit - large driver at 115mA (nominal) chosen **NB** *For TTL applications the TTL inputs should be used, V_{CC} should be 5V and V_{EE} should be 0V (DG package pin out)*

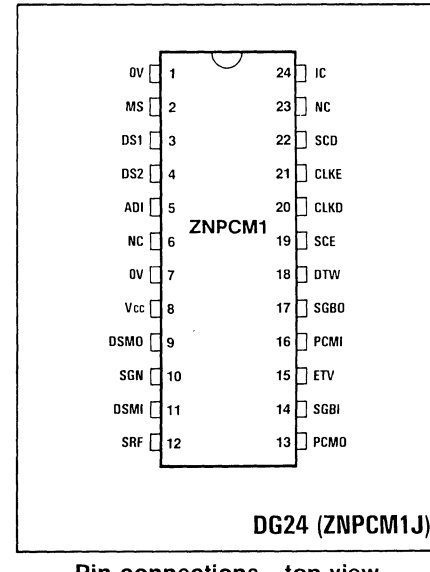
PLESSEY
Semiconductors

ZNPCM1

SINGLE CHANNEL CODEC

FEATURES

- Converts a delta-sigma modulated digital pulse stream into compressed 'A' law pcm and vice-versa.
- Enables realisation of a single channel codec circuit with minimum component usage.
- Pin selectable input/output interface providing either single channel operation at 64K bit/s (2,048 kHz external clock) or up to 2,048K bit/s (2,048 kHz external clock) for multi-channel burst format.
- Encoder and decoder can be clocked asynchronously (useful for pcm multiplex applications).
- Optional alternate digit inversion.
- Electrically and pin compatible with AY-3-9900
- Fully TTL compatible.
- Single 5V supply.



Pin connections - top view

DESCRIPTION

The ZNPCM1 integrated circuit is the result of a joint development programme with British Telecom. Designed for use in single channel codec systems the device accepts a delta-sigma modulated pulse stream at 2,048K bit/s (2,048kHz external clock) and converts it into 8K sample/s compressed 'A' law pcm. In the decode direction the device performs the reverse function. A flexible serial pcm input/output interface is provided allowing operation in a single channel mode at 64K bit/s or at up to 2,048K bit/s (2,048kHz external clock) for a multi-channel burst format. Digit delay control is provided to compensate for transmission delays. Optional alternate digit inversion is provided and the encoder and decoder can be clocked asynchronously if required for use in pcm multiplex applications.

Designed for use with a 2,048kHz system clock, when operated with the required delta-sigma modulator and demodulator (see application report 'a single channel codec'). The device performance complies with B.T. specification RC5549B and CCITT recommendations G711/G712 (1972).

The ZNPCM1 is guaranteed to operate up to 2,048kHz and will typically operate up to 4MHz. Operation is from a single 5V power supply with a typical power dissipation of 400mW. All inputs and outputs are TTL compatible. Available in a 24-lead ceramic dual in-line package, the device is designed to operate over the temperature range 0 °C to +70 °C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7 Volts
Input Voltage, V_{IN} .. .. +5.5 Volts
Operating Temperature Range .. 0°C to +70°C
Storage Temperature Range .. .. -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
High-level Output Current, I_{OH}	—	—	-400	µA
Low-level Output Current, I_{OL}	—	—	4	mA
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating temperature range).

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.5	—	—	V
V_{IL}	Low level input voltage		—	—	0.8	V
V_{OH}	High level output voltage	V_{CC} = Min., I_{OH} = Max.	2.4	3.5	—	V
V_{OL}	Low level output voltage	V_{CC} = Min., I_{OL} = Max.	—	—	0.4	V
I_{IH}	High level input current	V_{CC} = Max., V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low level input current	V_{CC} = Max., V_{IL} = Max.	—	-1	-10	µA
I_{CC}	Supply current	V_{CC} = Max.	—	80	110	mA
t_{vw}	Encoder timing vector pulse width		—	488	—	ns
t_{vv}	Encoding timing vector pulse width with edge variation		—	—	100	ns
t_{ww}	Decoder timing waveform pulse width		10	15.6	—	µs
f_{max}	Operating frequency		2.048	4	—	MHz
t_r & t_f	Rise and fall times	0.4V to 3V Transition	5	—	40	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns
C_I	Input capacitance		—	—	10	pF

PIN CONFIGURATIONS

Pin	Notation	Comments
1	0V	
2	MS	MODE SELECT (Note 1) Logic 0 = External pcm I/O interface timing Logic 1 = Internal pcm I/O interface timing
3	DS1	DECODER SELECT 1 and 2 (Note 2)
4	DS2	A two bit binary word selects required digit delay between encoder and decoder. DS1 DS2 Digit Delay 0 0 0 0 1 1 1 0 2 1 1 3
5	ADI	ALTERNATE DIGIT INVERSION Logic 0 = No. ADI Logic 1 = ADI
6	N.C.	NO CONNECTION
7	0V	
8	V_{CC}	
9	DSMO	DELTA-SIGMA MODULATED OUTPUT SIGNAL
10	SGN	SIGN BIT OUTPUT Sign bit from the encoder, used to operate on the delta-sigma modulator to reduce d.c. offset effects.
11	DSMI	DELTA-SIGMA MODULATED INPUT
12	SRF	SPECTRAL REDISTRIBUTION FUNCTION Output signal used to operate on the delta-sigma modulator to reduce low frequency quantisation noise.
13	PCMO	PCM OUTPUT
14	SGBI	SIGNALLING BIT INPUT Facility for adding signalling bit(s) to the output pcm stream.
15	ETV	ENCODER TIMING VECTOR A pulse defining the beginning of each frame used to maintain encoder timing.
16	PCMI	PCM INPUT
17	SGBO	SIGNALLING BIT OUTPUT Serial output for extracting signalling bit(s) from the incoming pcm stream.

PIN CONFIGURATIONS *(continued)*

Pin	Notation	Comments
18	DTW	DECODER TIMING WAVEFORM A pulse used to indicate to the decoder when the input pcm stream is in the input register (required only when external shift clocks are used).
19	SCE	ENCODER SHIFT CLOCK Used to control the output of serial pcm data from the encoder (when MS is low).
20	CLKD	DECODER MAIN CLOCK
21	CLKE	ENCODER MAIN CLOCK
22	SCD	DECODER SHIFT CLOCK Used to control the input of the serial pcm data to the decoder (when MS is low).
23	N.C.	NO CONNECTION
24	I.C.	INTERNAL CONNECTION Make no external connection to this pin.

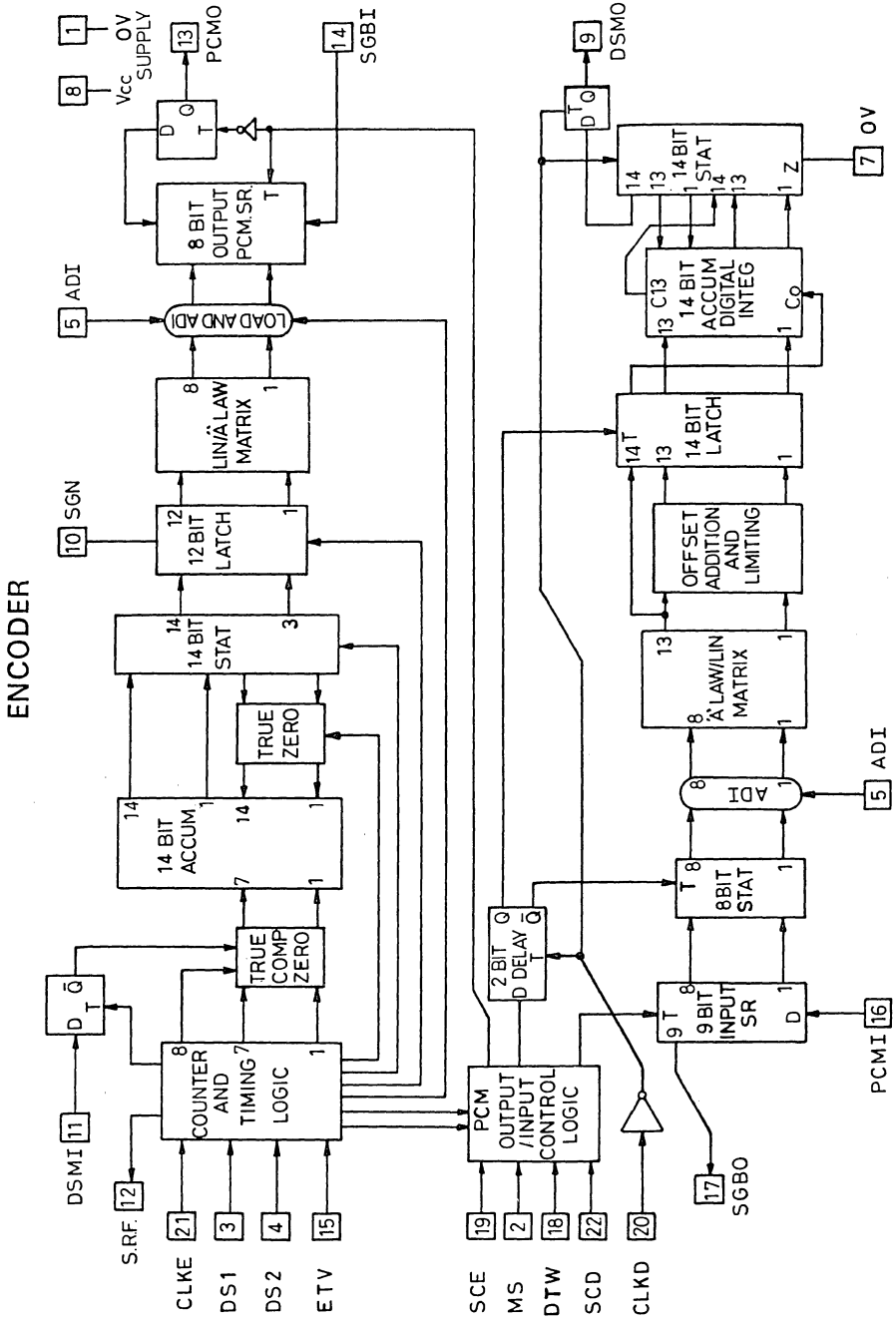
Notes:

1. With MS low (logic 0) serial PCM transmission is under the control of an externally generated shift clock SCE which can vary from 64 kHz to 2,048 kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGB1 input. In the high (logic 1) state the 8 bit PCM codeword will be transmitted at a rate of 64K bit/sec and each codeword will occupy the full 125 μs frame period with the leading edge of the first bit occurring at a time defined by the ETV pulse.

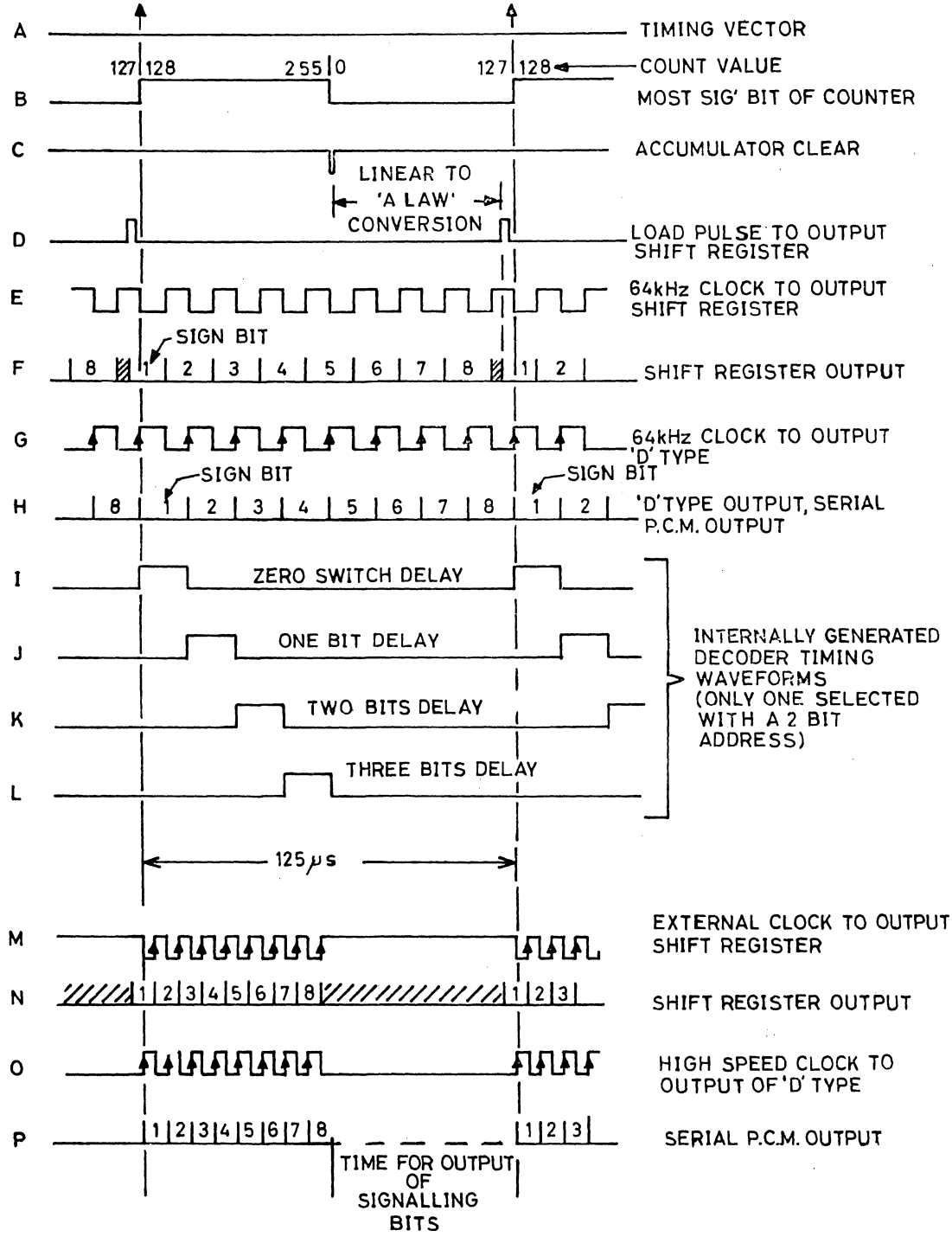
2. Delays through the transmission network, normally under the control of transmission switches, may cause the decoder input pulse stream to be delayed in time by a number of digits from the original transmitted pulse. To compensate for this delay two control inputs, DS1 and DS2, are provided. Consequently when MS is in the high state discrete digit delays of 0 to 3 periods may be selected resulting in a controlled shift of decoder timing in order to re-align Bit 1 in its correct position in the input register.

   When using an externally generated clock (i.e. MS in low state) an input shift clock (SCD) and timing waveform (DTW) are required to ensure that Bit 1 of the input codeword occupies its correct position in the input shift register.

FUNCTIONAL DIAGRAM

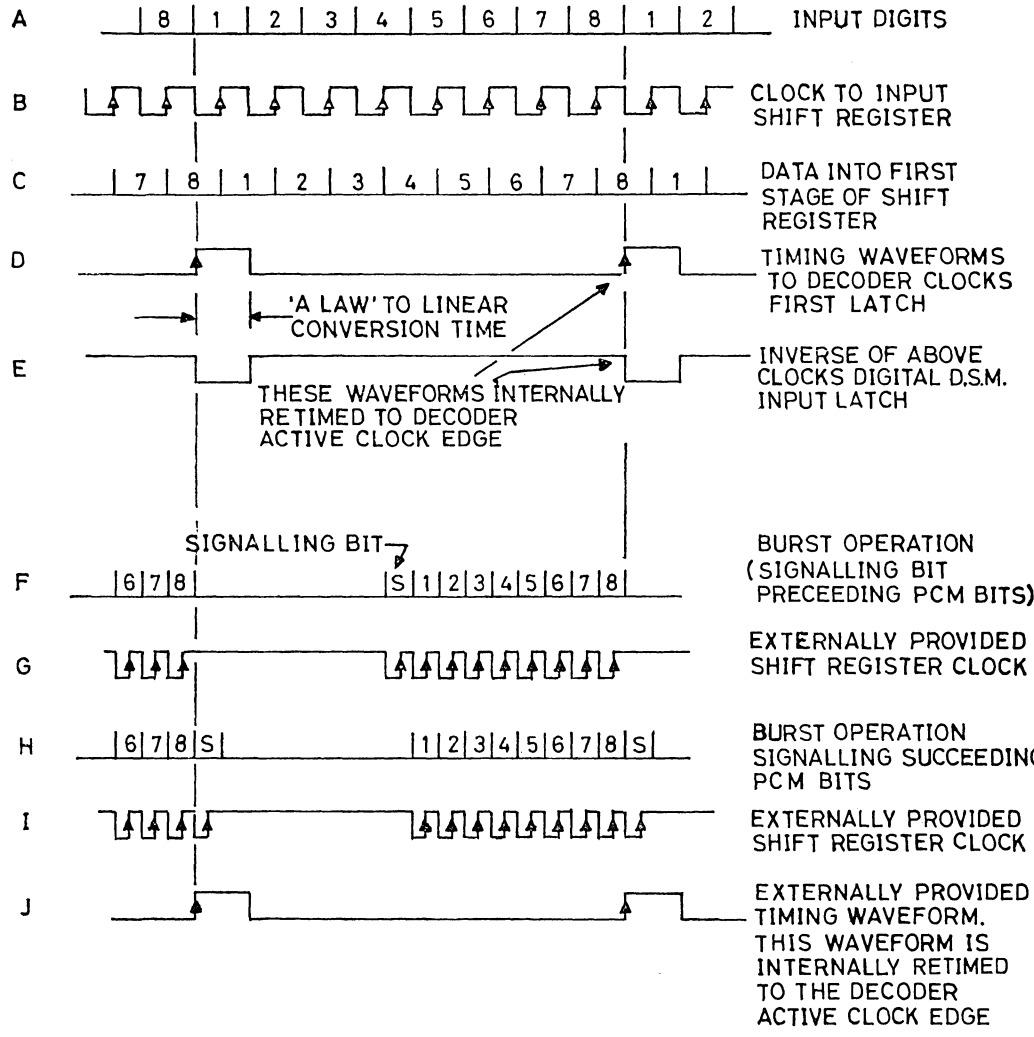


TIMING DIAGRAM
ENCODER



TIMING DIAGRAM

DECODER



APPLICATIONS INFORMATION

(a) A Single Channel Codec

Fig. 1 shows a block diagram of a single channel Codec using the ZNPCM1. The circuit accepts a band limited analogue input signal (300 – 3,400 kHz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The dsm bit stream is then converted by the ZNPCM1 into 8-bit compressed pulse code modulation (pcm) code words at the standard rate of 8K samples/sec, which is then converted into serial format for transmission serially at 64K bit/sec. External timing signals can be used to increase the transmission bit rate to 2,048K bit/sec. to allow for multiplexing in a burst format (see application b).

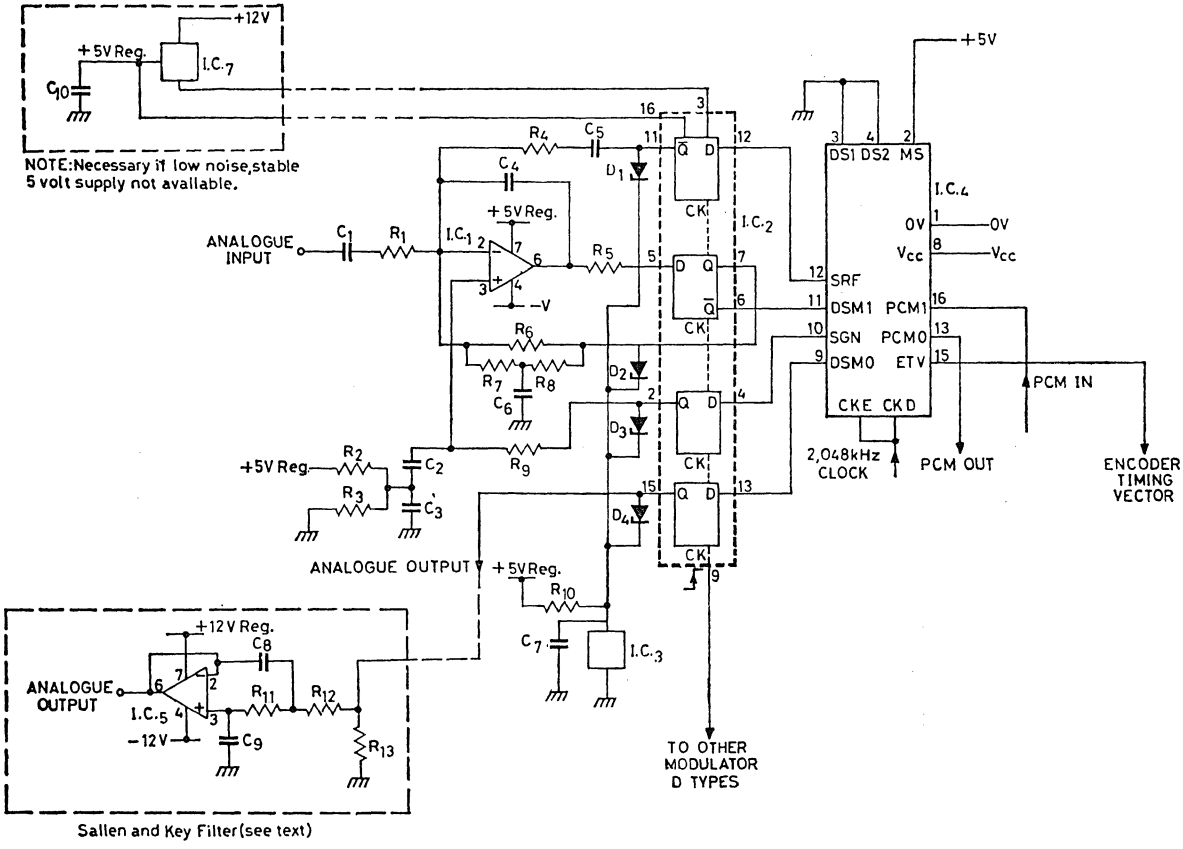


Fig. 1.

The pcm input interface will accept either a 64K bit/sec. bit stream or, by the application of external timing signals, a bit rate of 2,048K bit/sec. in burst format. This is then converted by the ZNPCM1 into a dsm bit stream at 2,048K bit/sec. The dsm demodulator accepts this bit stream and produces one of two precisely defined analogue levels per single bit sample. The analogue waveform can then be recovered via a low pass filter, cutting off just above the highest signal frequency to be recovered (3.4 kHz).

Output voltages of the dsm circuit are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the Codec, and clamping the high state output voltages to a 2.45V reference by the use of Schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, along with a small modulator/demodualtor physical size by implementing the resistors and small capacitors as an in-line hybrid. More details of the operation of the dsm circuit are outlined in the Plessey brochure 'A Single Channel Codec'.

An interesting development, again in co-operation with British Telecom, is the integrated circuit dsm solution, the ZNPCM2. This will reduce the circuitry surrounding the ZNPCM1 to a single I.C. and seven capacitors.

The Codec performance related to CCITT criteria is outlined in Fig.2.

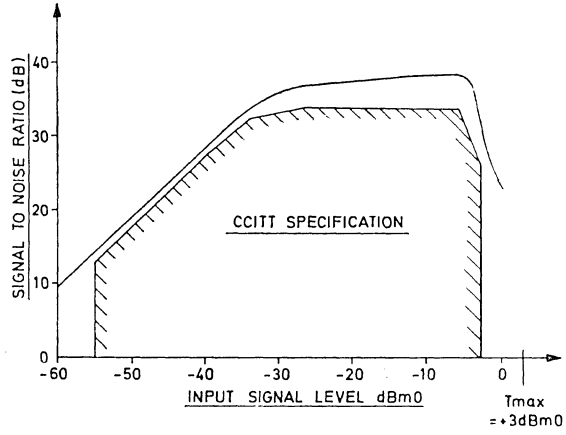


Fig. 2.

(b) A 30 Channel PCM Codec Solution

Traditionally the code conversion process on branch-to-main telephone exchange systems has been performed using multiplexed codecs. Historically the reason for this has been the codec specification where the signal-to-noise and gain-linearity constraints imposed on the systems have resulted in the use of expensive hybrid codecs. It might seem immediately obvious that the use of single channel codecs offers a more attractive solution, however a comparison of one of the major performance criteria is first of all necessary, that of power dissipation. Indeed, an initial comparison using the conventional 30 Channel PCM system shows the single channel codec approach to disadvantage. However, a more detailed analysis, using the single channel codecs in a power switching mode, shows this technique to be compatible with time shared codecs. This is described in section (d).

Let us first of all consider the system approach for using the single channel codecs in a 30 channel PCM system by looking at Fig.3.

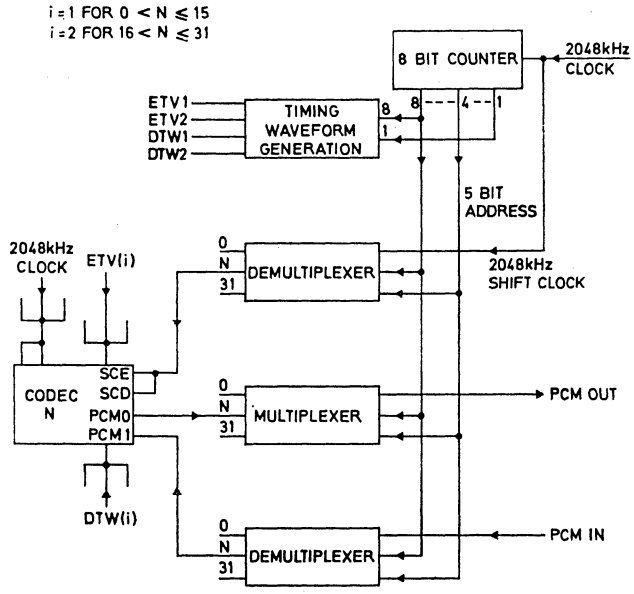


Fig. 3.

Fig. 3 shows how a 32 time slot (Note: A 30 Channel system has in fact, 32 time slots, the two additional ones being for signalling notation and synchronisation), 2,048K bit/sec. multiplex can be formed and decoded using 30 single channel codecs, when the two directions of transmission operate synchronously. Only the Nth codec is shown, connected to the 'Nth' port of the 32 port multiplexer and demultiplexers. When the 5-bit address equals N the 2,048 kHz shift clock is routed through the 'Nth' codec for eight clock pulses as shown in Fig. 4(a). The shift-in and shift-out clock terminals of the codec are commoned together. Since the shift-out terminal uses a negative active clock edge and the shift-in terminal uses a positive active clock edge the pcm digits for the two directions may be in exact time alignment. This is compatible with using the same 5-bit address for the multiplexer and the other demultiplexer.

The Encoder Timing Vector (ETV) and the Decoder Timing Waveform (DTW) may be derived from a counter driven by the 2,048 kHz clock and commoned across a number of codecs. For a 32 time slot multiplex, two sets of ETV's and DTW's should be generated with a half frame displacement as shown in Figs. 4(b) and 4(c). The first pair will supply ports 0 to 15 and the second pair ports 16 to 31, and consequently allowing the shift activity to be kept well clear of the timing waveforms for a given codec.

For a conventional 32 time slot codec ports 0 and 16 correspond to the synchronisation and signalling channels respectively.

Fig. 5 shows a similar arrangement for generating and decoding a 32 time slot multiplex when the two directions of transmission operate asynchronously. The two directions are operated quite independently but using similar principals to those previously discussed. It should again be noted that two sets of ETV's and DTW's should be used.

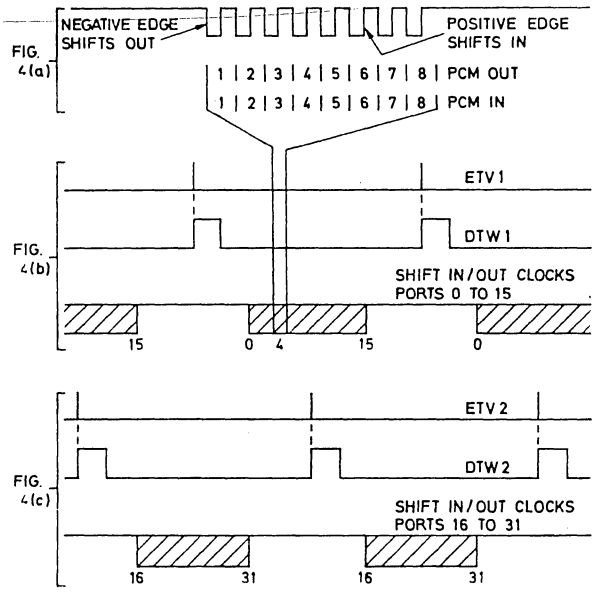


FIG. 4(a)
NEGATIVE EDGE SHIFTS OUT
POSITIVE EDGE SHIFTS IN
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM OUT
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM IN
FIG. 4(b)
ETV1
DTW1
SHIFT IN/OUT CLOCKS PORTS 0 TO 15
15
0 4
15
0
FIG. 4(c)
ETV2
DTW2
SHIFT IN/OUT CLOCKS PORTS 16 TO 31
16
31
16
31

Fig. 4.

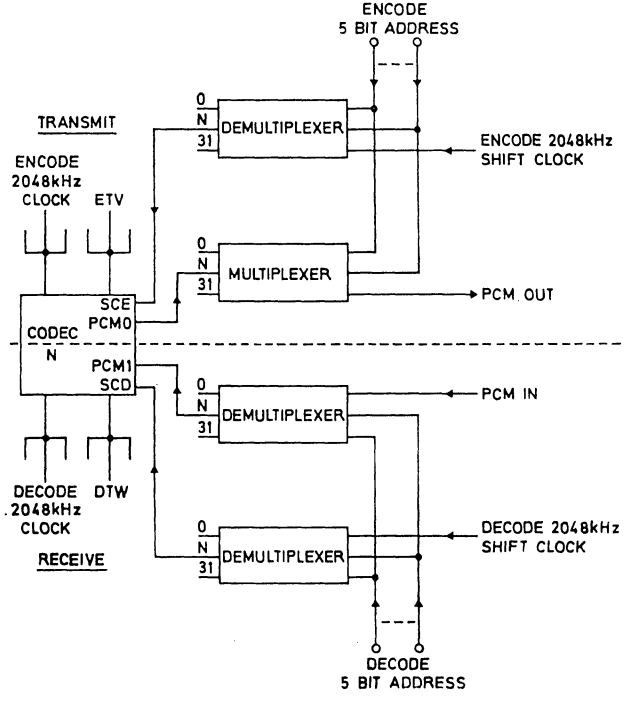

ENCODE 5 BIT ADDRESS
TRANSMIT
ENCODE 2048kHz CLOCK
ETV
0
N
31
DEMULTIPLEXER
ENCODE 2048kHz SHIFT CLOCK
MULTIPLEXER
PCM OUT
SCE
PCM0
CODEC N
PCM1
SCD
PCM IN
DECODE 2048kHz CLOCK
DTW
RECEIVE
DECODE 2048kHz SHIFT CLOCK
DECODE 5 BIT ADDRESS

Fig. 5.

(c) Switching Applications

The ZNPCM1 can be used in a variety of ways to satisfy switching applications. One technique is to operate directly on the 2,048K bit/s digit stream produced by the circuit arrangement shown in Fig. 3, where each codec has a defined time slot in the bit stream. An alternative technique would be to derive the address applied to the multiplexer and demultiplexer from the contents of a random access memory (RAM) which defines the codec to be used in a given time slot, in an exchange of PCM codewords between the codec and an intermediate store. In this mode of use the codec interface is effectively used as a time switch store.

The circuit shown in Fig 5 can be used without an intermediate store where again the codec addresses are derived from RAM's. The encode address defines the 'source' and the decode address the 'sink' in a given time slot. The decode address may be delayed with respect to the encode address by an integer number of 2,048 kHz clock periods to take account of any small fixed switching delay.

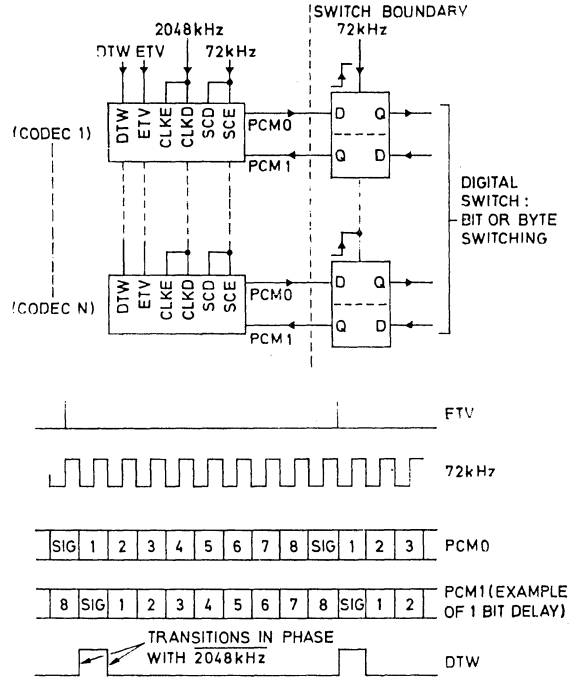


Fig. 6.

Fig. 6 shows an arrangement where the codecs input and output continuously, allowing 9-bits (8 PCM plus 1 signalling) to be exchanged in each 125 μs sample period. All the codecs may be supplied with common ETV, DTW, 2,048 kHz and 72 kHz waveforms. Each bit is retimed in the digital switch using a latch.

The digital switch may be operated using a bit switching arrangement, combined with the extraction and insertion of the signalling bits. Alternatively the bits may be reformatted into bytes and then byte switching performed. If the signalling is handled separately to the pcm codewords then a 64K bit/s rate can be used to and from the codec. This is compatible with using the codecs internal clock mode (MS = 1) in which case the only common timing waveforms required at the codec are the 2,048 kHz clock and the ETV.

(d) Power Switching

Comparisons have previously been made between shared and single channel codecs where these comparisions were reduced to one of power dissipation. Considerable power savings can be made by using the codecs in such a mode that they are only powered-up when required for use.

It is interesting to compare the power dissipation of an eight channel system using in one case eight ZNPCM1s in a power switching mode and, in the other case, one of the more popular time shared codecs which caters for eight channels. One single channel codec dissipates 600 mW and the time shared codec dissipates 1500 mW.

If the channel occupancy is p, then the average power dissipation per channel for the time shared codec is given by

$$W_{TS} = 1 - (1-p)^8 \frac{1500}{8} \text{ mW}$$

This assumes the time shared codec is only powered-up when any of the eight channels are required for use.

The average power dissipation per channel using the single channel codecs is simply given by

$$W_{SC} = p.600 \text{ mW}$$

Fig. 7 shows a plot of power dissipation versus channel occupancy ; p for both approaches. The busy period average channel occupancies are likely to be in the range 0.2 to 0.15, clearly the lower end of the curves. Taking a figure of p = 0.06, for example, then the single channel codec dissipates only 36 mW per channel, approximately 50% less than the time shared codec. As the graph shows even for very busy exchanges given values for p of up to 0.3 shows the ZNPCM1 system to dissipate less power.

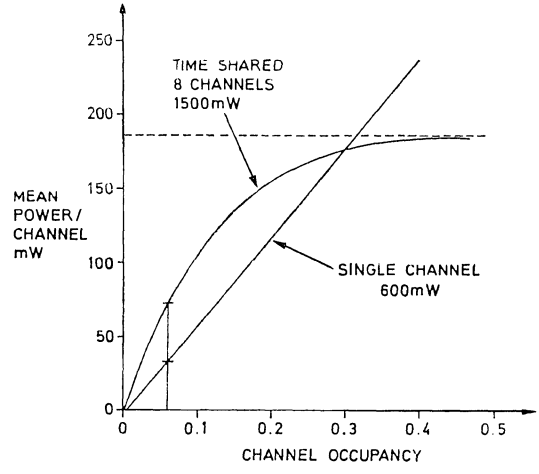


Fig. 7.

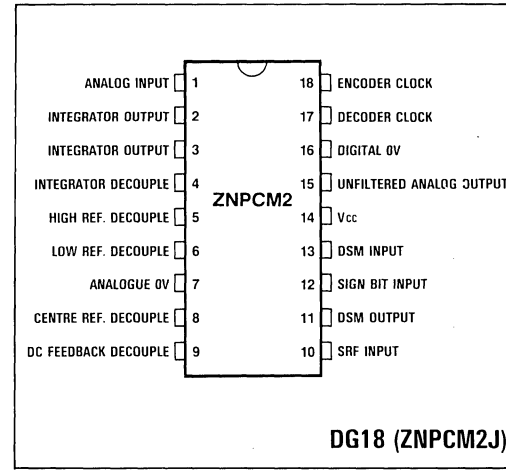
PLESSEY
Semiconductors

ZNPCM2

DELTA SIGMA MODULATOR/DEMODULATOR

FEATURES

- Converts analogue input signal into delta sigma modulated (DSM) signal to be used as input for ZNPCM1 Codec I.C.
- Converts DSM signal produced by ZNPCM1 into level defined digital pulse stream for conversion to the analogue equivalent signal using low-pass filter techniques.
- High signal-to-noise ratio.
- Monolithic integrated circuit combining digital and analogue circuitry.
- Single 5V supply.
- 18-lead ceramic or modulated D.I.L. package.



Pin connections - top view

DESCRIPTION

The ZNPCM2 Delta Sigma Modulator/Demodulator (DSM) Integrated Circuit is designed for use in conjunction with the Plessey ZNPCM1 or G.I. AY-3-9900 Codec ICs as the conversion unit in pulse code modulation communication systems. The ZNPCM2 modulator function converts analogue speech or data signals into a sampled signal having one bit per sample at a high sampling rate. The demodulator function produces an output signal having one of two well defined voltage levels in response to the signal bit per sample input signal. The original signal can then be recovered by low-pass filter techniques.

The ZNPCM2 provides excellent signal-to-noise ratio as a result of innovative circuit techniques developed by British Telecom. A rectangular input waveform designated as a spectral redistribution function (SRF) is provided and this modifies the quantisation noise spectrum, moving the noise components to higher frequencies. By varying the amplitude and phase of the SRF waveform, the net effects on the PCM outputs from the Codec system can be made to be ZERO if the SRF is sampled synchronously within the system. In addition a complex feedback network is utilised in the DSM circuit to provide increased feedback at low frequency which results in the relative attenuation of low frequency quantisation noise components below 32kHz.

DC alignment to better than 0.01% at low signal amplitudes is achieved at the output by use of a feedback loop minimising both the DSM voltage offset and the digital code offset. This technique makes use of the fact that the PCM code words have a sign and magnitude format and the result eliminates the need for component trimming.

ZNPCM2

Designed using the same technology as the ZNPCM1 Codec I.C., the ZNPCM2 combines both linear and digital circuits on the same monolithic I.C. Packaged in an 18-lead ceramic (ZNPCM2J) DIL, the device is designed to operate over the temperature range 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +7 volts
Digital Input Voltage, $V_{IN(D)}$ ..... +5.5 volts
Analogue Input Voltage, $V_{IN(A)}$ ..... 4 volts pk-to-pk
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage	4.75	5.0	5.25	V
High-level Output Current, I_{OH} (Digital Outputs)	—	—	−400	μA
Low-level Output Current, I_{OL} (Digital Outputs)	—	—	4	mA
Analogue Output Impedance, Z_{AO}	—	100	—	Ω
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over the recommended operating temperature range).

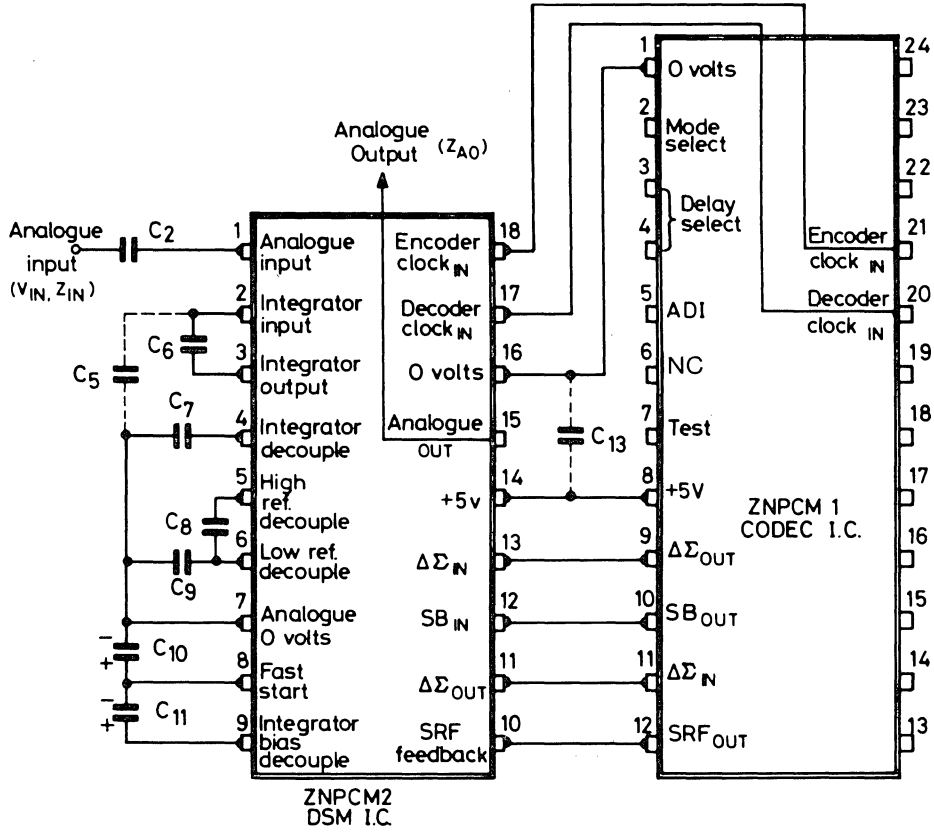
(a) Digital Inputs and Outputs.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2.3	—	—	V
V_{IL}	Low-level input voltage		—	—	0.8	V
V_{OH}	High-level output voltage	V_{CC} = Min, I_{OH} = Max.	2.4	4	—	V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max.	—	—	0.4	V
I_{IH}	High-level input current	V_{CC} = Max, V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low-level input current	V_{CC} = Max, V_{IL} = Min.	—	—	10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	24	—	mA
f	Operating frequency		—	2,048	—	kHz
t_r & t_f	Rise and fall time	0.4V – 3.0V transition	5	—	40	ns
t_{pd}	Propagation delay	Clock $\varnothing_E$ or $\varnothing_D$ to DSM output 2.5V level	—	40	60	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns

(b) Analogue Input and Output.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Analogue Input Voltage for 0dBm0	Peak-to-peak	—	1.4	—	V
Z_{IN}	Analogue Input Impedance	Measured at 1kHz	80	100	—	kΩ
V_C	D.C. Voltage across C_{11}	V_{CC} = Max.	—	±3.0	±5.0	mV

DSM CODEC INTERFACE



NOTES

1 The external high frequency decoupling between pins 5, 6 and 7 should be of minimal impedance (i.e. in the range of 1 to 20MHz). Low loss capacitors connected via minimal conductor path lengths and inductances are required. Suitable capacitors are 0.22μF monoblock types. Total connection length and resistance including capacitor leads should be as follows:

Pins 5 to 6 <10mm and <0.1Ω
Pins 6 to 7 <16mm and <0.1Ω

2 Analogue ground pin 7 and digital ground pin 16 must be linked externally. Ideally, this should be their only connection; however, if it is essential that the two 0V systems are connected at a point remote from the ZNPCM2 then pin 16 should remain connected to the analogue ground only.

3 Performance of the ZNPCM1 and ZNPCM2 is layout dependent and an optimum layout is shown on page 6. Capacitor C_5 and C_{13} are optional but may improve performance in some instances.

PERFORMANCE

The codec combination of the ZNPCM1 and ZNPCM2 meets all the performance requirements of the C.C.I.T.T. recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

(1) Idle Channel noise: −70dBm0p (See Fig. 1).
C.C.I.T.T. recommendation = −65dBm0p

(2) Signal-to-noise ratio and gain level linearity: Figs. 2(a) and 2(b) show the results using a 450 − 550kHz pseudo-random noise test.

(3) Intermodulation distortion: measured products are at least 10dB and on average 18dB better than C.C.I.T.T. recommendations.

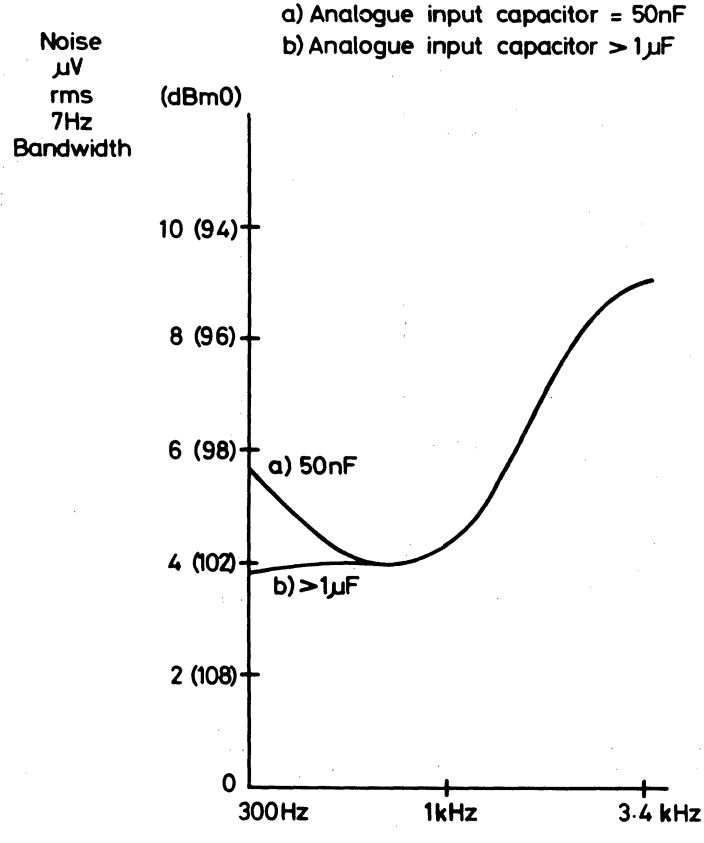


Fig. 1. Idle Channel Noise Spectrum

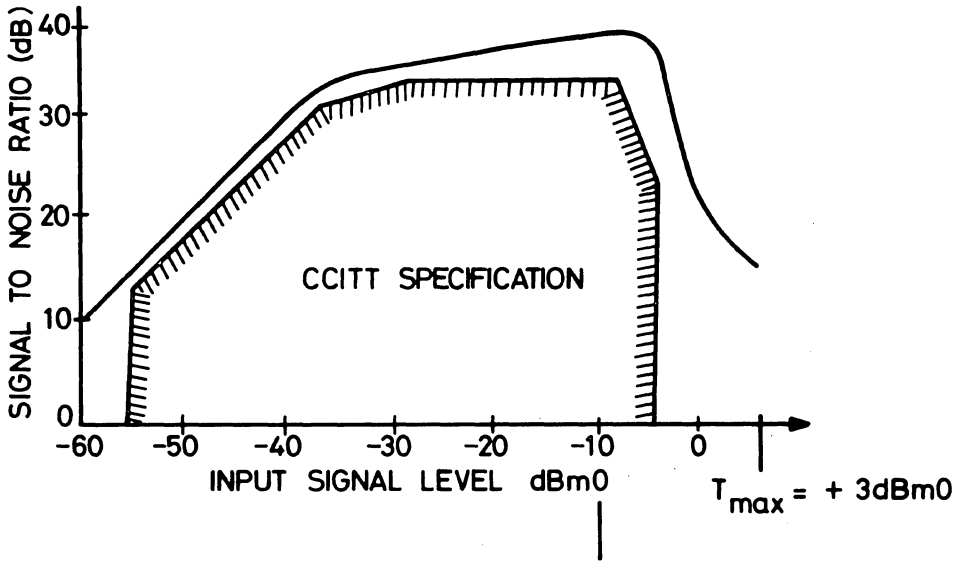


Fig. 2(a). Signal to Noise Ratio 'A Law'

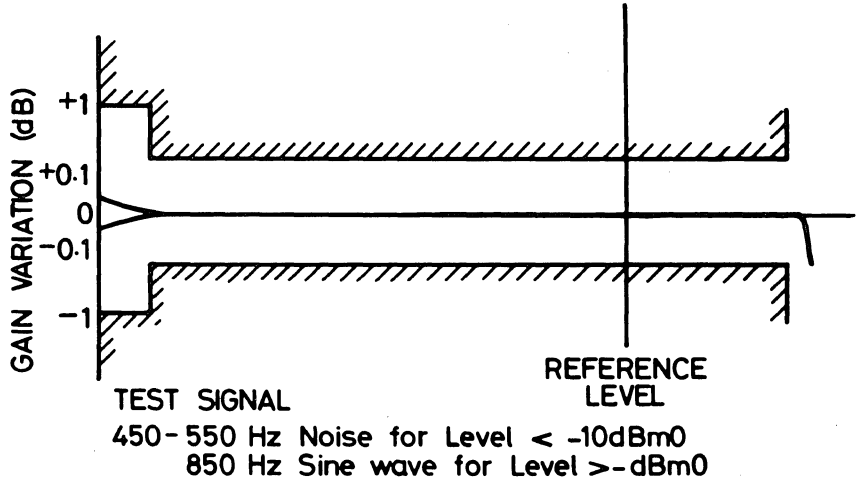
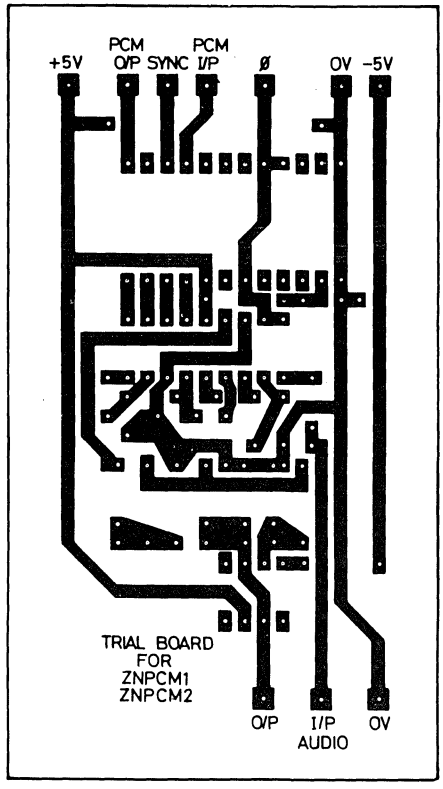
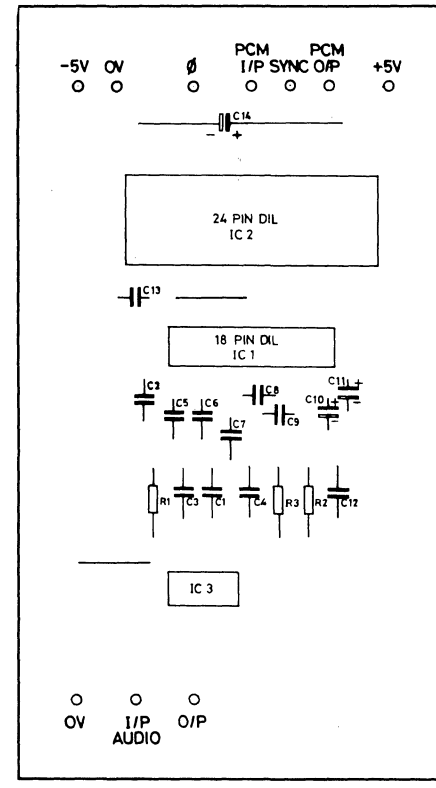


Fig. 2(b). Gain to Signal Level 'A Law'

BASIC SYSTEM BOARD FOR ANALOGUE TO ANALOGUE PERFORMANCE EVALUATION





P.C. BOARD COMPONENT LAYOUT

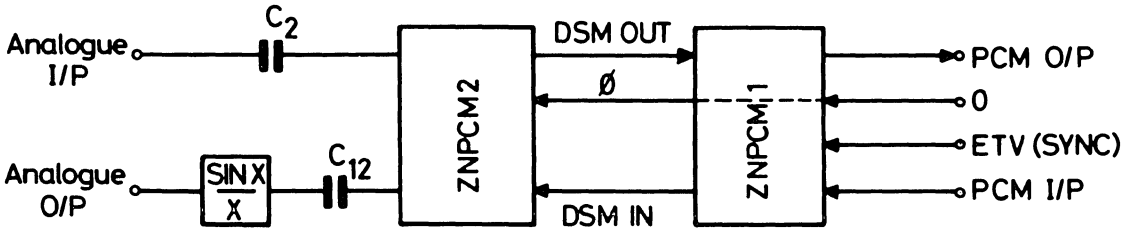
ACTUAL SIZE

ZNPCM1 & ZNPCM2 TRIAL UNIT

Component List (Tolerances ±20% unless otherwise shown)

IC1	ZNPCM2	C6	47pF ±5%
IC2	ZNPCM1	C7	4.7nF ±5%
IC3	741 Op Amp	C8	0.22μF
R1	91k0 2%	C9	0.22μF
R2	91k0 2%	C10	10μF, 16V Tantalum Electrolytic
R3	100k0	C11	10μF, 16V Tantalum Electrolytic
C1	0.022μF	C12	47nF
C2	47nF	C13	0.1μF Ceramic
C3	100pF ±2%	C14	6.8μF, 10V Electrolytic
C4	1nF ±2%		
C5	10pF		

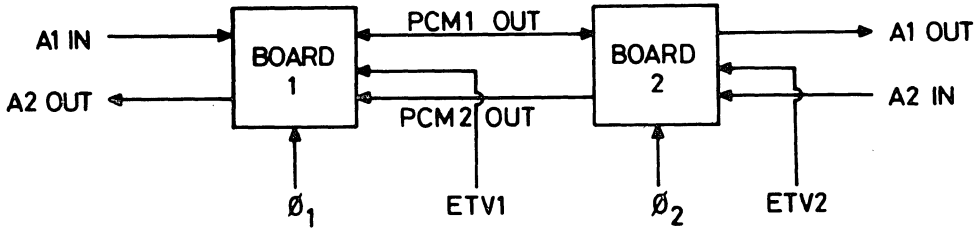
SCHEMATIC



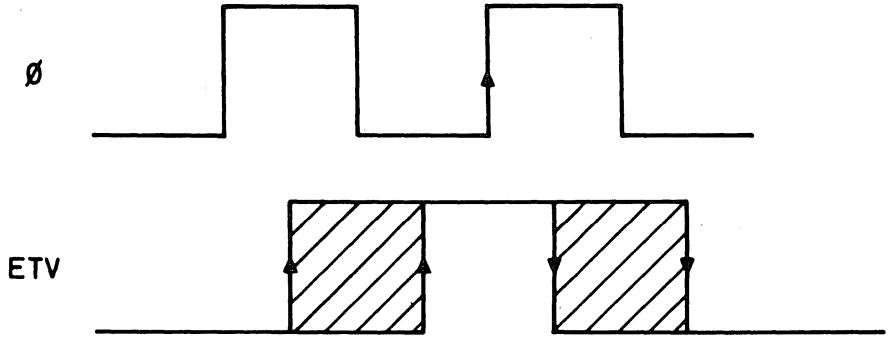
Single Channel Codec System Operating in Internal Mode (PCM at 64K bits/sec. without ADI).

Performance of the ZNPCM1/2 may be simply evaluated by linking PCM O/P to PCM I/P and comparing Analogue O/P to Analogue I/P. No ETV (Sync) signal is required for this.

For a more comprehensive evaluation two boards are required connected on the configuration shown,



$\varnothing_1$ and $\varnothing_2$ must be the same frequency and ETV1 and ETV2 can be common or up to 30 clock periods displaced.



WAVEFORMS SHOWING ETV TOLERANCE

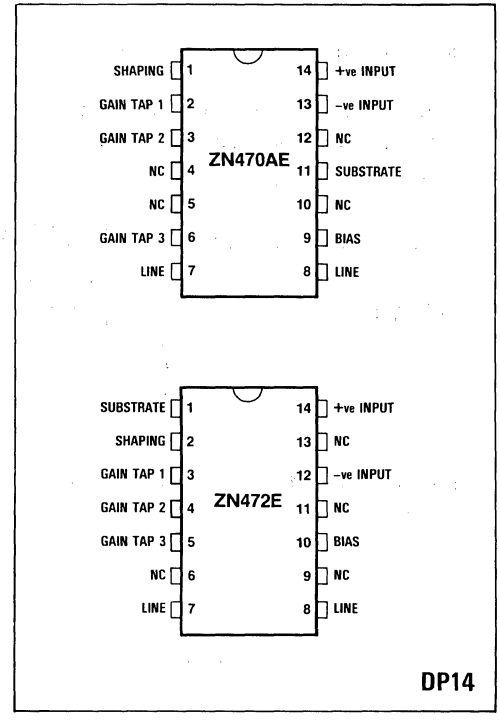
PLESSEY
Semiconductors

ZN470AE/ZN472E

MICROPHONE AMPLIFIER FOR TELEPHONE CIRCUITS

FEATURES

- Conforms to BT Specification S1377
- On Chip Bridge Allows Dual Supply Polarity Operation
- Direct Matching to Electret Transducers
- 4 Gain Settings by Adjustable Links
- Operates from 1mA to 100mA Line Current
- 220mA 20 Second Overload Capacity
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Meets BT Lightning Surge Requirements
- Minimum External Components in Telephone Circuits



Pin connections - top view

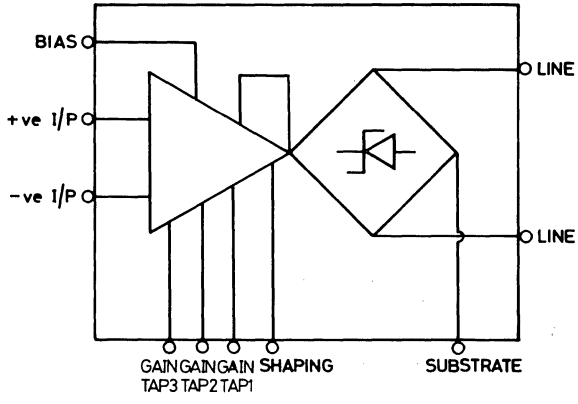


Fig. 1 System Diagram

DESCRIPTION

This microphone amplifier was developed in conjunction with British Telecom for use with an electret transducer to replace the carbon transmitter. Dual polarity operation is accommodated by an on-chip bridge. Full lightning surge protection is given by on-chip components thus eliminating the need for an external surge suppression diode. The high input impedance makes it suitable for use with high or low impedance microphones that provide a high output voltage.

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 120mA continuous (220mA for 20 seconds)
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

T_{amb} = 25°C R_L = 100Ω R_O = 15Ω C = 1000pF I_S = 50mA
Pins 2, 3, 6 Open-circuit f = 1kHz V_O = 300mV unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain Note 1	A_V	–	20	–	dB	
		–	21.5	–	dB	Pins 3 & 6 shorted
		–	23.4	–	dB	Pins 2 & 3 shorted
		–	25.7	–	dB	Pins 2, 3 & 6 shorted
Change in voltage gain from typical at I_S = 50mA when I_S is changed	$\Delta A_V(I_S)$	−1	−0.1	+1	dB	I_S = 100mA
		−1	−0.5	+1	dB	I_S = 20mA
		–	−0.9	0	dB	I_S = 10mA
Change in voltage gain with V_O relative to V_O of 300mV	$\Delta A_V(V_O)$	−1	+0.2	+1	dB	V_O = 95mV
		−1	−0.6	+1	dB	V_O = 950mV
Change in voltage gain with line polarity	$\Delta A_V(P)$	–	0.2	0.5	dB	
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	V_O = 300mV
	DH(900)	–	4.5	6	%	V_O = 900mV
Lower cut off frequency	f_{Lco}	–	500	–	Hz	R_b = 6M8Ω C_s = 39pF
Upper cut off frequency	f_{Uco}	–	10	–	kHz	C = 5600pF
		–	200	–	kHz	C = 0
Output noise Note 2	V_{on}	–	170	316	μV	V_{in} = 0
Temperature co-efficient of A_V	$T_c(A_V)$	–	0.1	–	%/°C	T_{amb} = −20°C to +80°C

Note 1 Gains are for circuit in Fig. 2. The actual device gain is higher by about 6dB but a 20pF input capacitance attenuates the electret signal to give 20dB to 25.7dB typical gain.

Note 2 Output noise is measured through a psophometer (CCITT recommendation P53).

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$ with pins 2, 3 and 6 not connected and for either supply polarity unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	5.5	6.0	volts	$I_S = 21mA$
		6.4	6.8	–	volts	$I_S = 50mA$
		–	9.2	9.7	volts	$I_S = 100mA$
Input Current		–	2	–	nA	$I_S = 50mA$
Input Offset Current		–	0.2	–	nA	$I_S = 50mA$
Input Offset Voltage		–	2.5	–	mV	$I_S = 50mA$

MICROPHONE AMPLIFIER APPLICATION

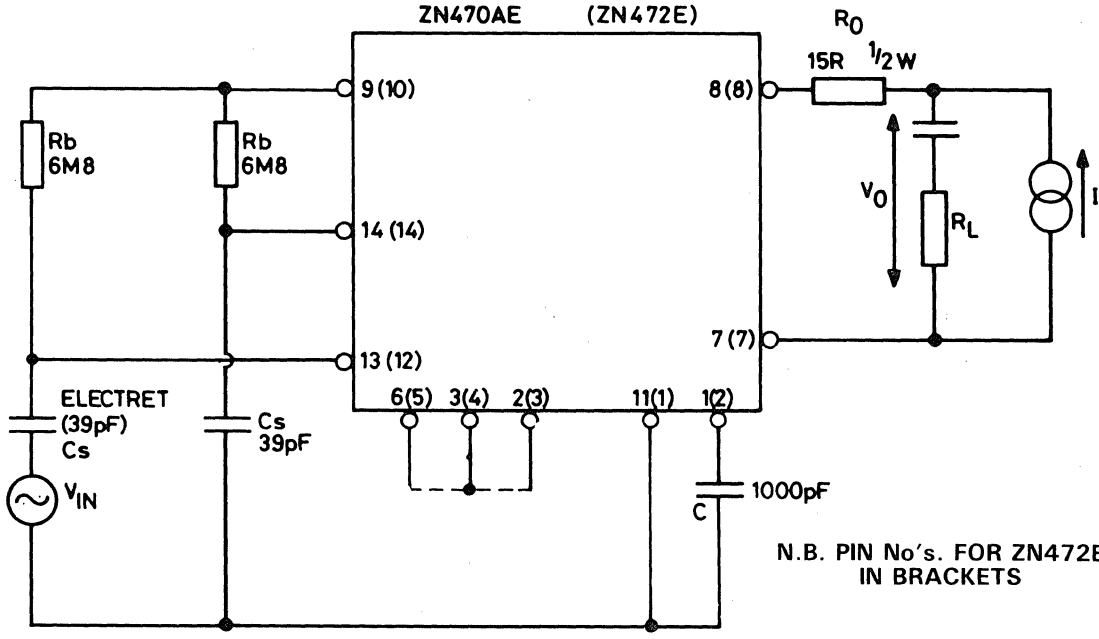


Fig. 2 Typical Electret Microphone Amplifier

The circuit shows ZN470AE/ZN472E with an electret transducer in a typical telephone handset application but with load test included. The gain setting taps may be used to select the appropriate voltage gain to compensate for production spreads in electret sensitivity.

The low frequency cut off is determined by the time constant $C_S R_b$ and a similar matching time constant is required on the other input. C_S is the capacitance of the electret microphone including stray capacitance and its value is therefore determined by the size and characteristics of the types used. The upper frequency cut off is determined by the shaping capacitor C. In addition the overall high frequency response is often controlled by acoustic means.

The leads to the high impedance inputs should be kept as short as possible to avoid the risk of pickup from stray fields.

In locations where high levels of humidity are likely to be encountered it is recommended that precautions are taken to prevent formation of leakage paths between +ve I/P and −ve I/P and between each of these inputs and substrate.

These precautions may take the form of:

a) Guard ring techniques

b) Varnishing or lacquering of the appropriate areas of the PCB.

c) Encapsulation of the complete amplifier module.

The guard ring technique involves completely enclosing the high impedance +ve I/P and −ve I/P nodes by a separate ring of copper. This ring should then be connected to the bias pin as this has a voltage much nearer to the operating voltage of the input pins compared with the substrate, hence current flowing in any leakage path will be minimised.

Note that the guard ring technique is easier to implement using the ZN472E pinning as indicated in Fig. 3.

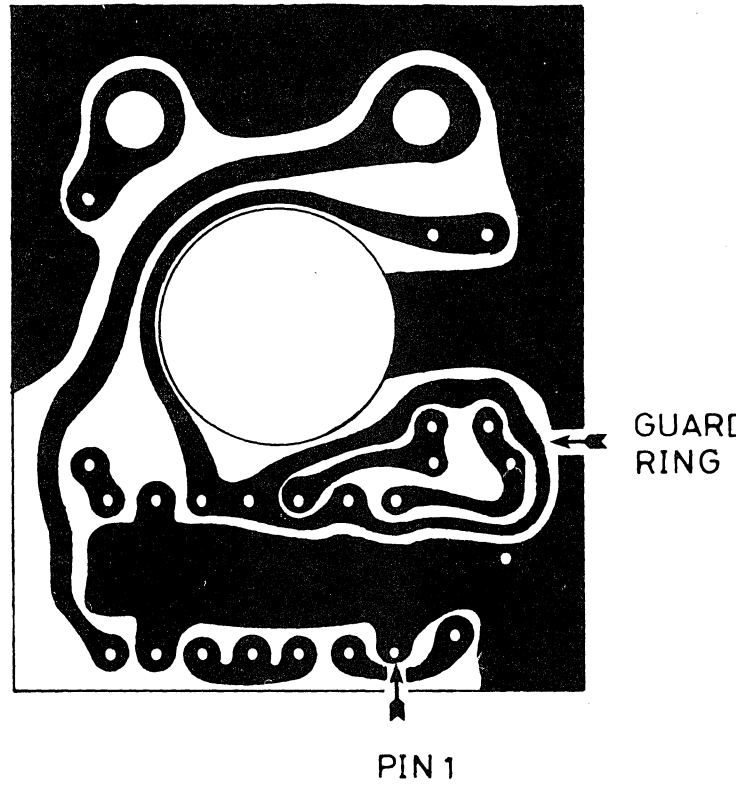
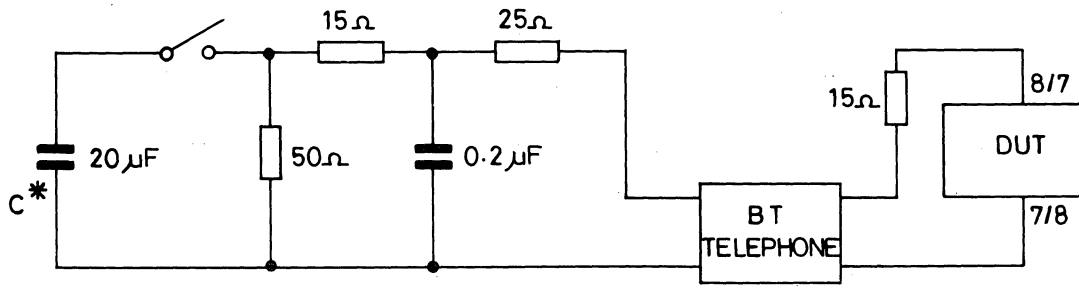


Fig. 3 Reverse Side of a PCB Indicating Guard Ring Screening on the ZN472E.

BT LIGHTNING SURGE TEST CIRCUIT



*C CHARGED TO 1500 VOLTS

When the capacitance is fully charged the switch is closed thus discharging the capacitance into the test network. The device under test, DUT, is connected via a 15ohm resistor to the standard microphone wires. The DUT must survive the discharge on either line polarity.

RELIABILITY

The ZN470AE is fully approved by British Telecom to their specification D3006 for 10 year life applications.

From extensive very long life tests, a predicted failure rate (at 95% confidence level) of less than 0.005% per annum has been calculated for service applications at 45°C and 50mA line current.

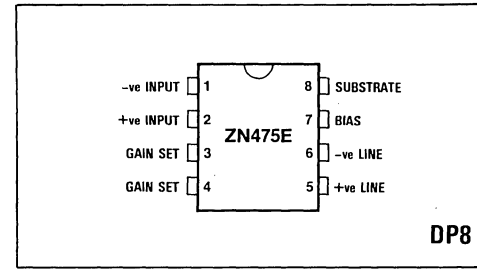
PLESSEY
Semiconductors

ZN475E

MICROPHONE AMPLIFIER FOR TELEPHONE CIRCUITS

FEATURES

- Direct Matching to Electret Transducers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits



Pin connections - top view

DESCRIPTION

Some electret transducers are supplied with a built in impedance matching junction FET buffer to operate with a microphone amplifier of low input impedance. The ZN475E has been designed with a high input impedance to match directly with electret transducers without the need for a FET buffer.

The device operates from a single polarity supply, but includes protection from inadvertent supply reversal.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different electret transducer sensitivities.

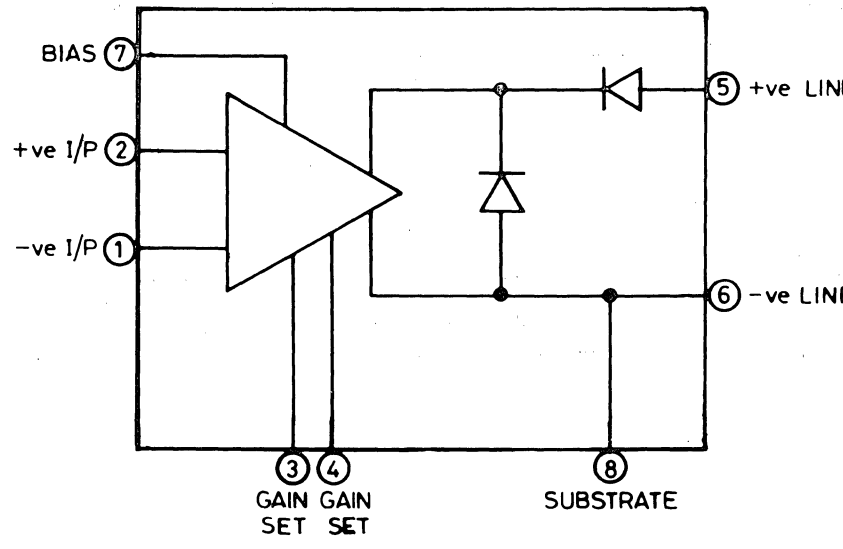


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current	100mA continuous (220mA for 20 seconds)
Operating Temp. Range	−20°C to +80°C
Storage Temp. Range	−55°C to +125°C

A.C. CHARACTERISTICS

$T_{amb} = 25°C$ $R_G = 80k\Omega$ $R_L = 100\Omega$ $R_O = 15\Omega$ $C_G = 100nF$ $I_S = 50mA$ $f = 1kHz$ $V_O = 300mV$ unless otherwise stated.

Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain Note 1	A_V	–	20	–	dB	
		–	45	–	dB	$R_G = 0$ $C_G = 2\mu 2F$
Change in voltage gain from typical at $I_S = 50mA$ when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	$I_S = 100mA$
		−1	−0.5	+1	dB	$I_S = 20mA$
		–	−0.9	0	dB	$I_S = 10mA$
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	$V_O = 95mV$
		−1	−0.6	+1	dB	$V_O = 950mV$
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	$V_O = 300mV$
	DH(900)	–	4.5	6	%	$V_O = 900mV$
Lower cut off frequency	f_{Lco}	–	500	–	Hz	$R_b = 6.8M\Omega$ $C_s = 39pF$
Upper cut off Frequency	f_{Uco}	–	200	–	kHz	
Output noise Note 2	V_{on}	–	170	316	μV	$V_{in} = 0$
Temperature co-efficient of A_V	T_c (A_V)	–	0.2	–	%/°C	$T_{amb} = -20$ to $+80°C$

Note 1 Gains are for circuit in Fig. 2. The actual device gain is higher by about 6dB but a 20pF input capacitance attenuates the electret signal to give 20dB to 25.7dB typical gain.

Note 2 Output noise is measured through a psophometer (CCITT recommendation P53).

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$, $R_G = 80k\Omega$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	4.9	5.4	volts	$I_S = 21mA$
		5.8	6.2	–	volts	$I_S = 50mA$
		–	8.5	9.0	volts	$I_S = 100mA$
Input Current		–	2	–	nA	$I_S = 50mA$
Input Offset Current		–	0.2	–	nA	$I_S = 50mA$
Input Offset Voltage		–	2.5	–	mV	$I_S = 50mA$

MICROPHONE AMPLIFIER APPLICATION

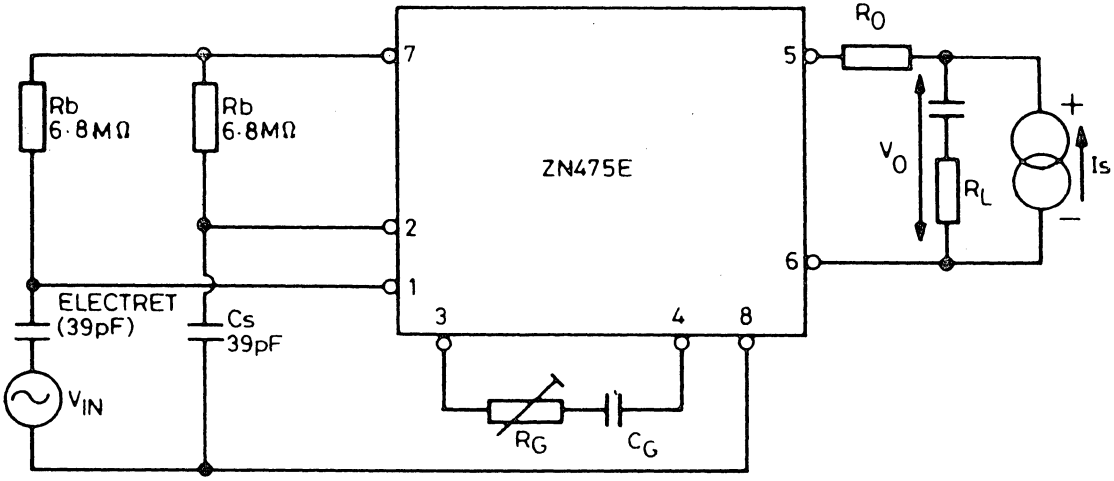


Fig. 2 Typical Electret Microphone Amplifier

The circuit shows ZN475 with an electret transducer in a typical telephone handset application but with load test included.

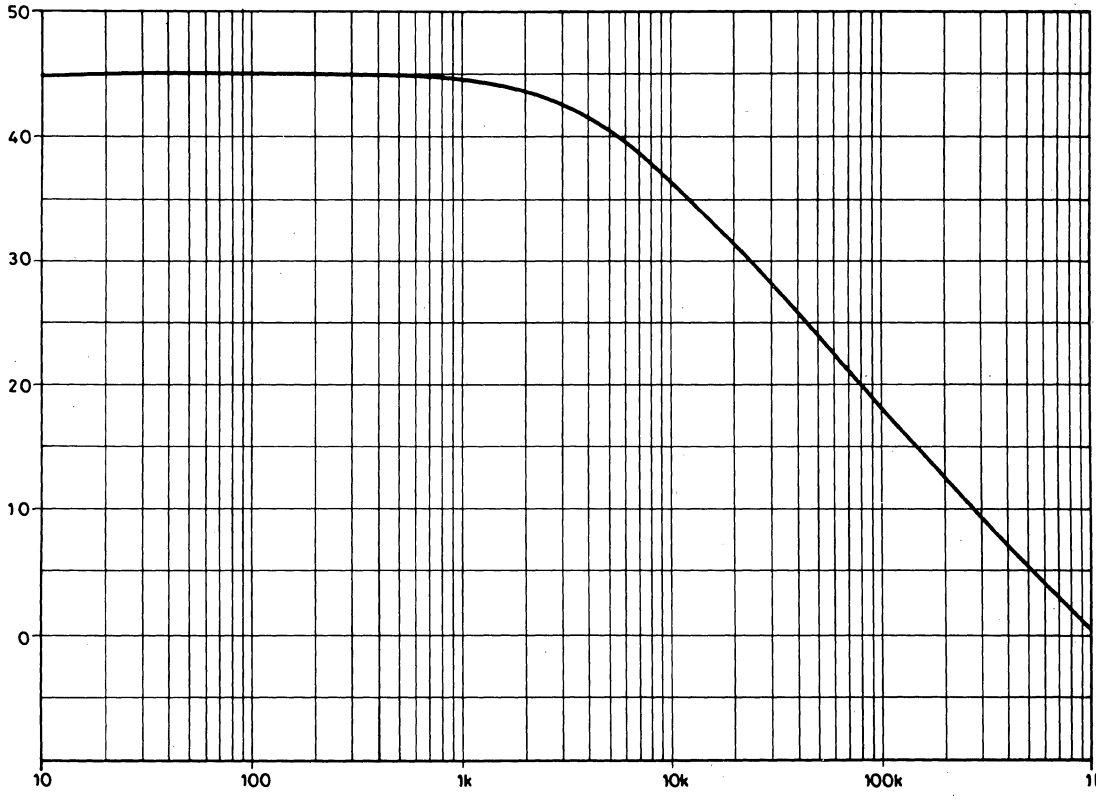
The low frequency cut off is determined by the time constant $C_S R_b$ and a similar matching time constant is required on the other input. C_S is the capacitance of the electret microphone including stray capacitance and its value is therefore determined by the size and characteristics of the types used. It is recommended that the overall high frequency response is controlled by acoustic means.

The leads to the high impedance input should be kept as short as possible to avoid the risk of pickup from stray fields.

In addition to the lower cut-off frequency f_{LCO} due to the time constant at the input there is an additional break-point at frequency f_L determined by C_G and R_G from the expression

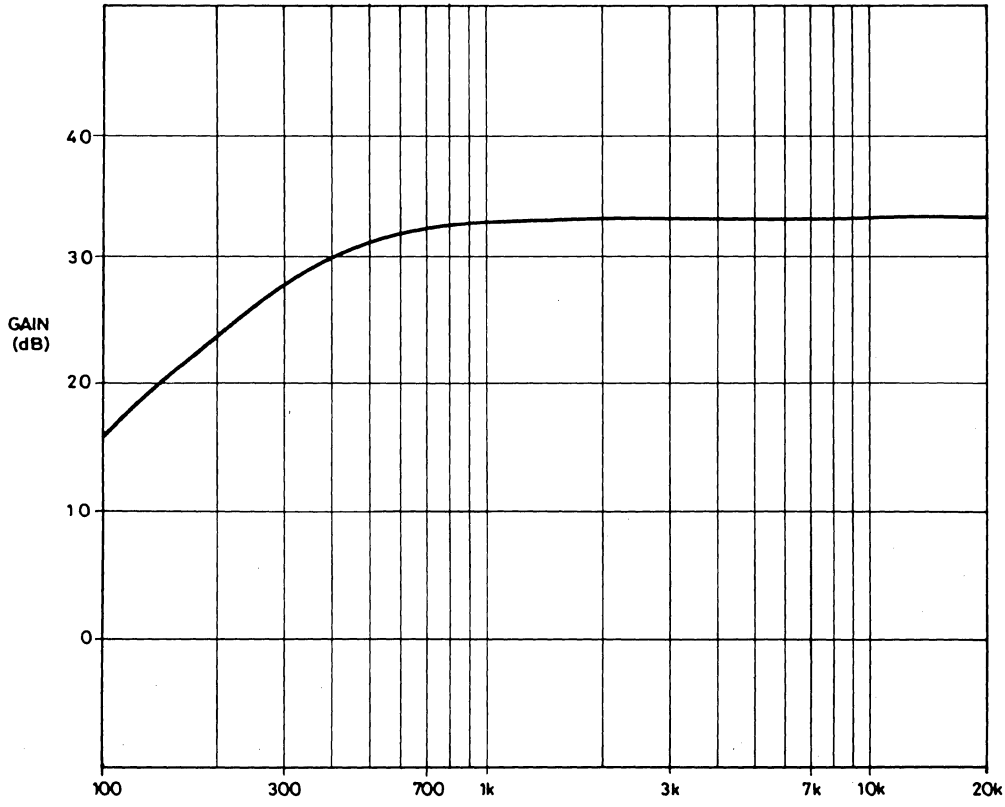
$$f_L \simeq \frac{1}{2\pi C_G (R_G + 5000)}$$

Conditions $I_S = 50mA$ $R_O = 15\Omega$ $R_L = 100\Omega$ $C_G = 2.2\mu F$ $f = 1kHz$



Gain (dB) vs R_G (I.C.)

Conditions $I_S = 50mA$ $R_O = 15\Omega$ $C_G = 100nF$ $R_G = 10k\Omega$



Gain (dB) vs Frequency (Hz)

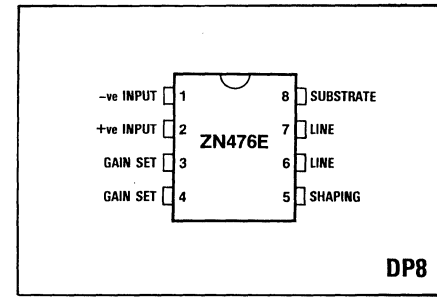
PLESSEY
Semiconductors

ZN476E

MICROPHONE AMPLIFIER FOR TELEPHONE CIRCUITS

FEATURES

- On Chip Bridge Allows Dual Supply Polarity Operation
- Direct Matching to Low Impedance (Moving Coil) Transducers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits



Pin connections - top view

DESCRIPTION

The ZN476E was developed specifically for use with low impedance transducers such as moving coil microphones to replace the carbon transmitter in telephone handsets. Dual polarity operation is accommodated by an on-chip bridge. Full lightning surge protection is given by on-chip components thus eliminating the need for an external surge suppression diode.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different low impedance (moving coil) transducer sensitivities.

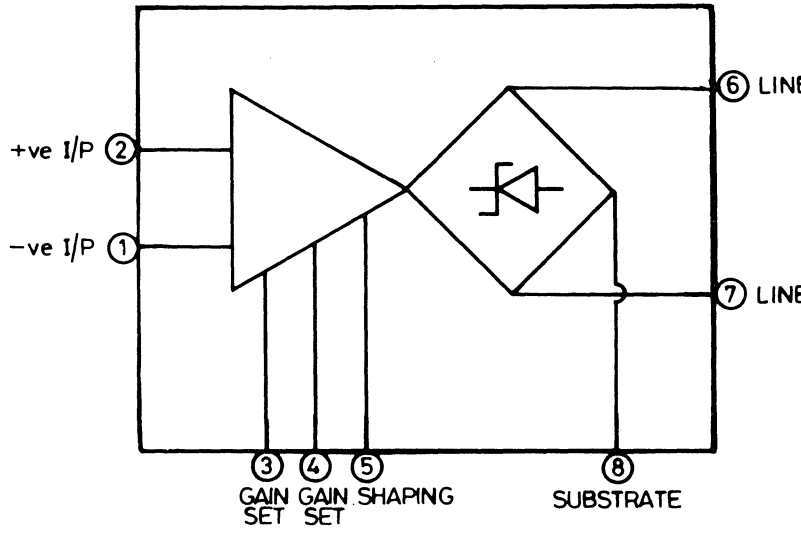


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

T_{amb} = 25°C R_G = 25kΩ R_L = 100Ω C_G = 100nF R_O = 15Ω I_S = 50mA C_S = 1nF f = 1kHz
V_O = 300mV unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain	A_V	17	20	23	dB	
		37	40	43	dB	R_G = 1.5kΩ C_G = 2.2μF
Change in voltage gain from typical at I_S = 50mA when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	I_S = 100mA
		−1	−0.5	+1	dB	I_S = 20mA
		−	−0.9	0	dB	I_S = 10mA
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	V_O = 95mV
		−1	−0.6	+1	dB	V_O = 950mV
Change in voltage gain with line polarity	ΔA_V (P)	−	0.2	0.5	dB	
Output impedance	R_{out}	−	50	−	Ω	
Total harmonic distortion	DH(300)	−	1	3	%	V_O = 300mV
	DH(900)	−	4.5	6	%	V_O = 900mV
Temperature co-efficient of A_V	T_c (A_V)	−	0.2	−	%/°C	T_{amb} = −20°C to +80°C

D.C. CHARACTERISTICS

T_{amb} = 25°C, V_{in} = 0 R_G = 25kΩ for either supply polarity unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	−	5.5	6.0	volts	I_S = 21mA
		5.4	6.8	−	volts	I_S = 50mA
		−	9.2	9.7	volts	I_S = 100mA

MICROPHONE AMPLIFIER APPLICATION

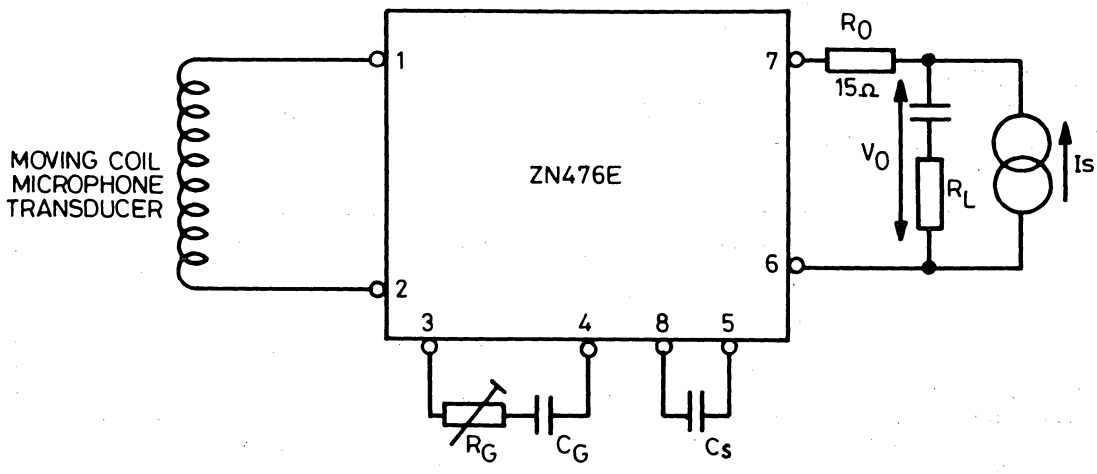


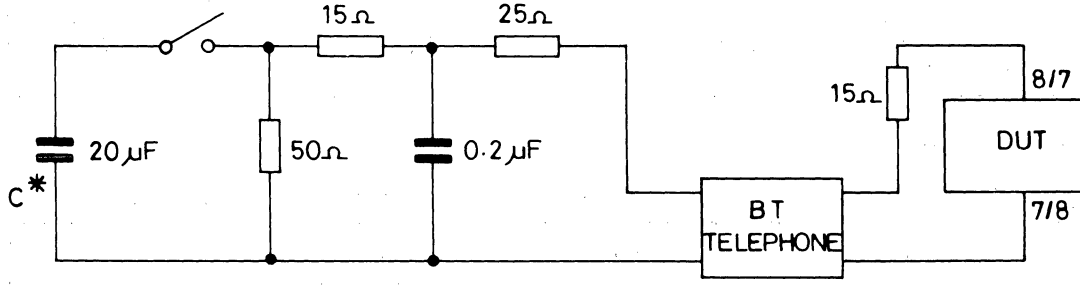
Fig. 2 Typical Application Circuit

The circuit shows ZN476E with a moving coil transducer in a typical telephone handset application but with load test included. The value of R_G is set to give the appropriate voltage gain for the particular transducer in use.

The value of the lower cut-off frequency f_L is determined by C_G and R_G from the expression

$$f_L \simeq \frac{1}{2\pi C_G(R_G + 500)}$$

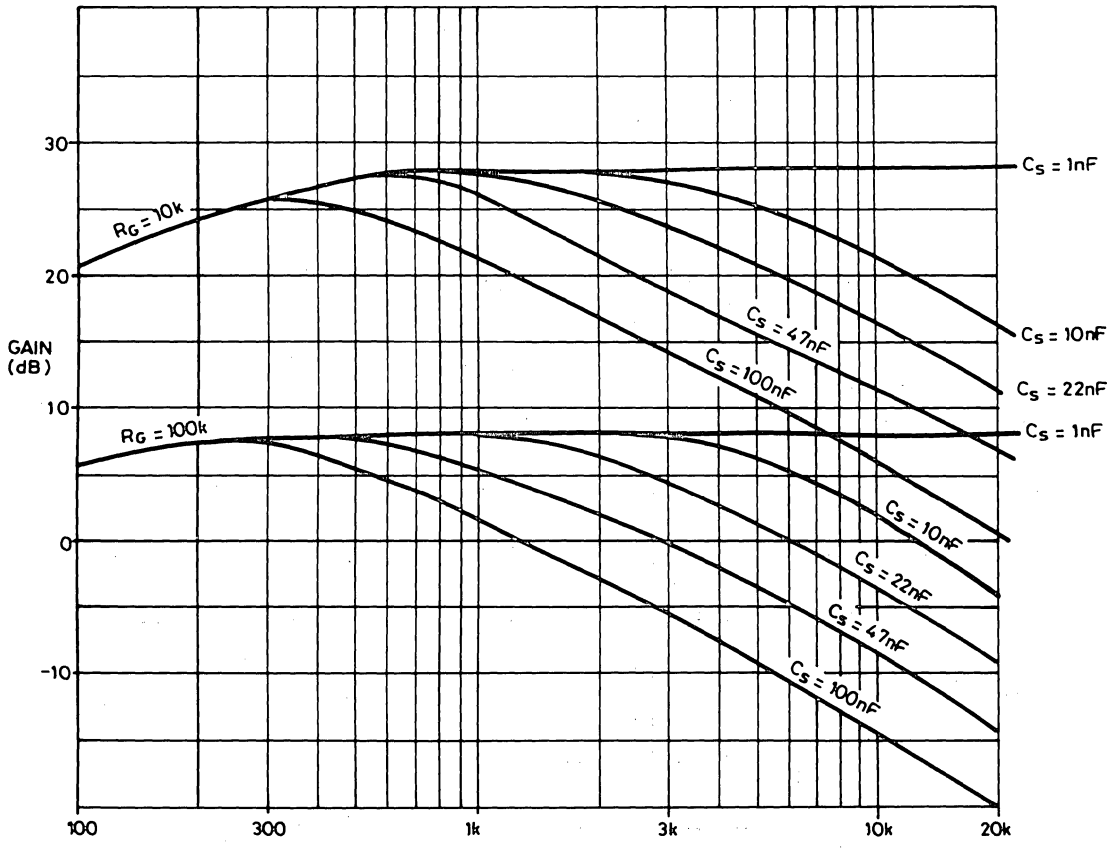
BT LIGHTNING SURGE TEST CIRCUIT



*C CHARGED TO 1500 VOLTS

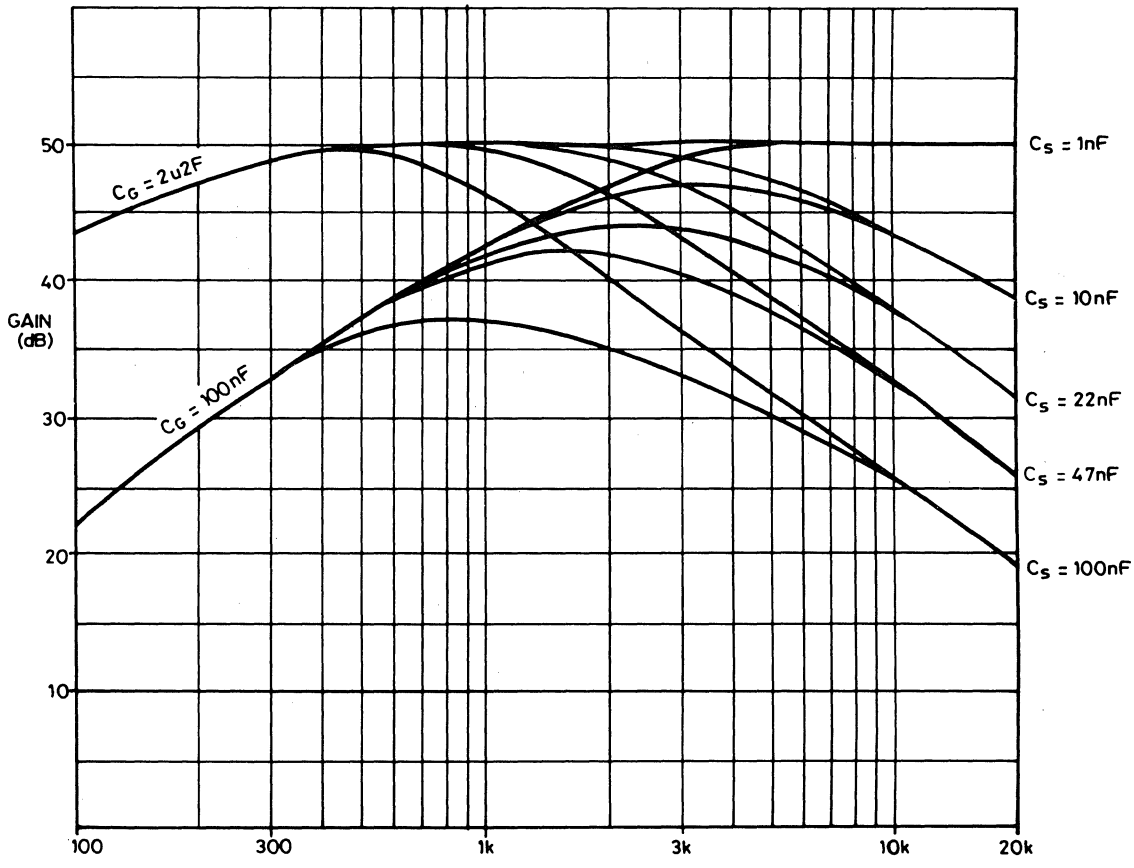
When the capacitor is fully charged the switch is closed thus discharging the capacitor into the test network. The device under test, DUT, is connected via a 15ohm resistor to the standard microphone wires. The DUT must survive the discharge on either line polarity.

Conditions $R_G = 10k$ and $R_G = 100k$ $I_C = 50mA$ $C_G = 100nF$

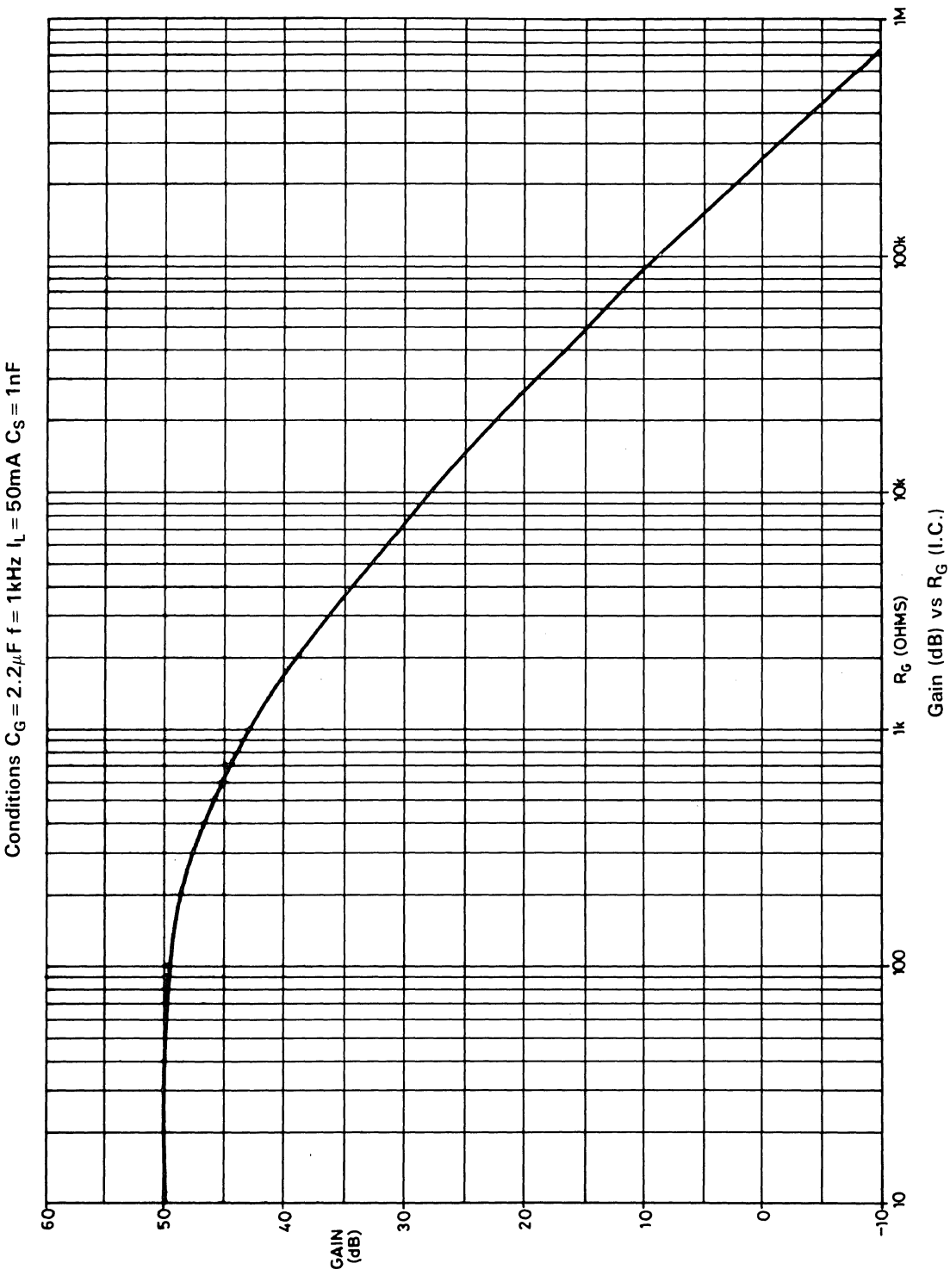


Gain (dB) vs Frequency (Hz)

Conditions $R_G = 0\Omega$ $I_L = 50mA$



Gain (dB) vs Frequency (Hz)


Conditions $C_G = 2.2\mu F$ f = 1kHz $I_L = 50mA$ $C_S = 1nF$
GAIN (dB)
60
50
40
30
20
10
0
-10
10
100
1k
10k
100k
1M
R_G (OHMS)
Gain (dB) vs R_G (I.C.)

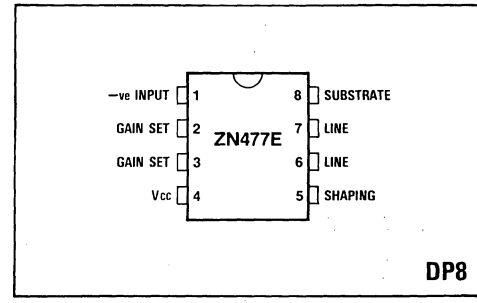
PLESSEY
Semiconductors

ZN477E

MICROPHONE AMPLIFIER FOR TELEPHONE CIRCUITS

FEATURES

- On Chip Bridge Allows Dual Supply Polarity Operation
- Designed to match electrets with FET buffers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits



Pin connections - top view

DESCRIPTION

The ZN477E was developed specifically for use with low impedance transducers such as electret microphones (with FET buffers) to replace the carbon transmitter in telephone handsets. Dual polarity operation is accommodated by an on-chip bridge. Full lightning surge protection is given by on-chip components thus eliminating the need for an external surge suppression diode.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different low impedance transducer sensitivities.

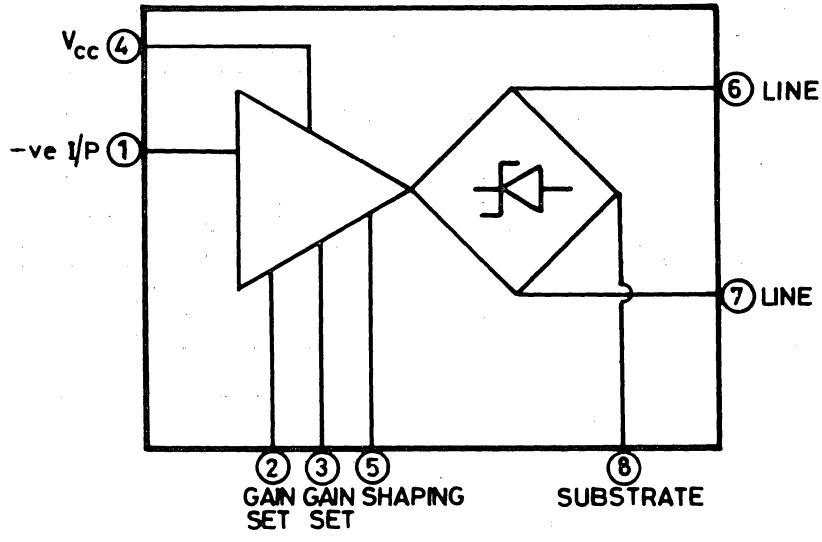


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

$T_{amb} = 25°C$ $R_G = 25k\Omega$ $R_L = 100\Omega$ $C_G = 100nF$ $R_O = 15\Omega$ $I_S = 50mA$ $C_S = 1nF$ $f = 1kHz$
$V_O = 300mV$ unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain	A_V	17	20	23	dB	
		–	28	–	dB	$R_G = 10k\Omega$ min. rec. value
Change in voltage gain from typical at $I_S = 50mA$ when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	$I_S = 100mA$
		−1	−0.5	+1	dB	$I_S = 20mA$
		–	−0.9	0	dB	$I_S = 10mA$
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	$V_O = 95mV$
		−1	−0.6	+1	dB	$V_O = 950mV$
Change in voltage gain with line polarity	ΔA_V (P)	–	0.2	0.5	dB	
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	$V_O = 300mV$
	DH(900)	–	4.5	6	%	$V_O = 900mV$
Temperature co-efficient of A_V	T_c (A_V)	–	0.2	–	%/°C	$T_{amb} = -20°C$ to $+80°C$

I_{FET} to be $\leqslant 1mA$

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$ $R_G = 25k\Omega$ for either supply polarity unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	5.5	6.0	volts	$I_S = 21mA$
		5.4	6.8	–	volts	$I_S = 50mA$
		–	9.2	9.7	volts	$I_S = 100mA$

MICROPHONE AMPLIFIER APPLICATION

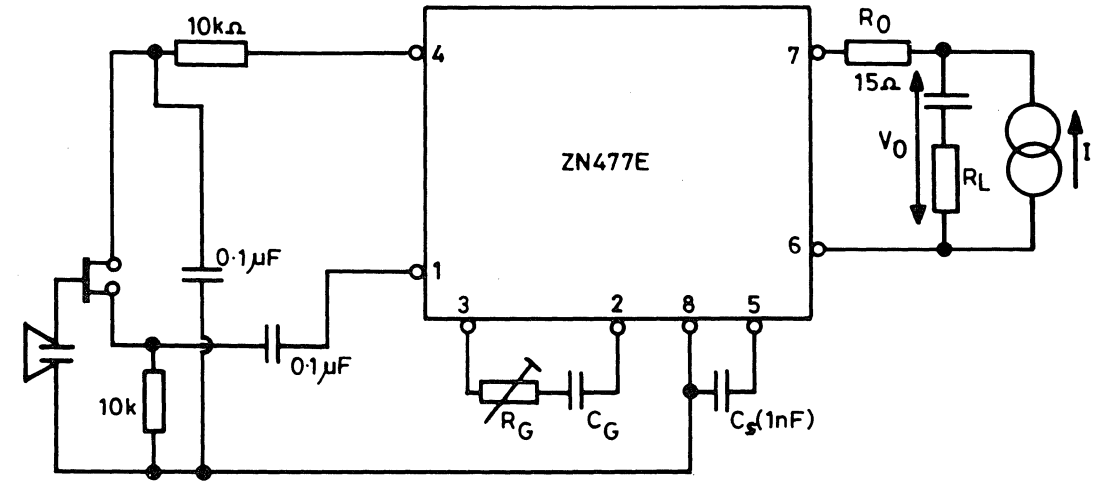


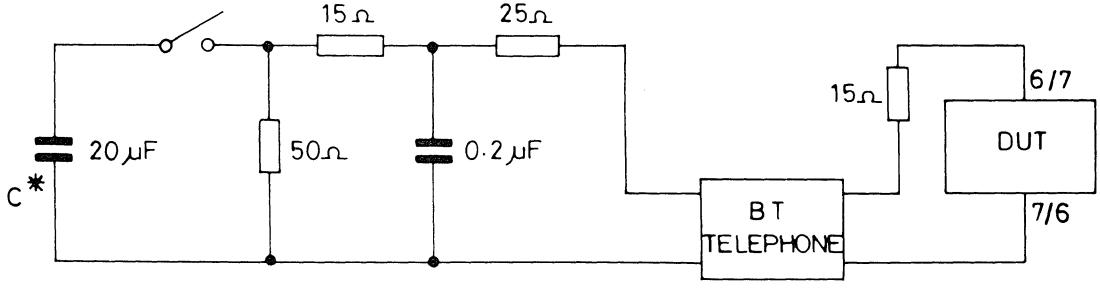
Fig. 2 Typical Application Circuit

The circuit shows ZN477E with a electret plus FET transducer in a typical telephone handset application but with load test included. The value of R_G is set to give the appropriate voltage gain for the particular transducer in use.

The value of the lower cut-off frequency f_L is determined by C_G and R_G from the expression

$$f_L \simeq \frac{1}{2\pi C_G(R_G + 500)}$$

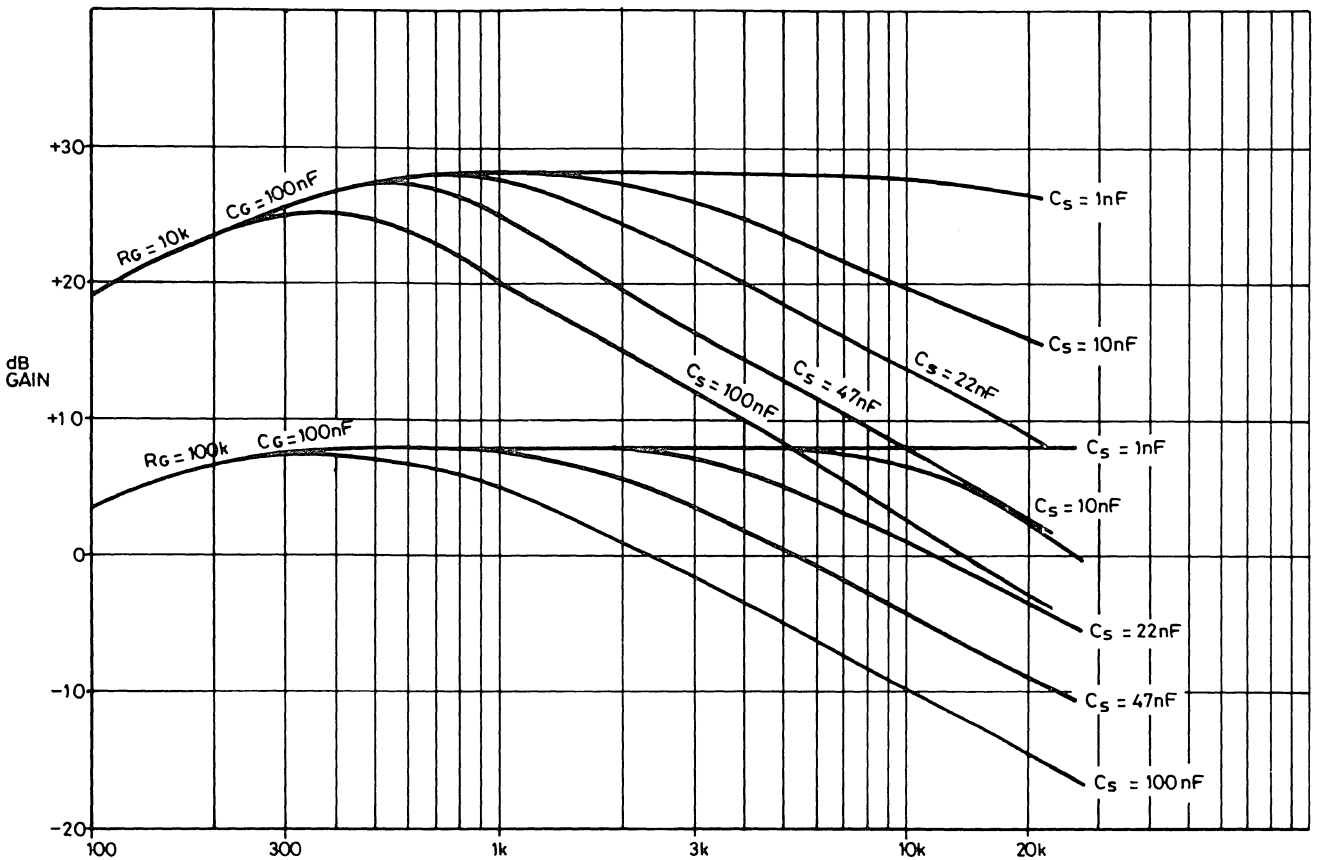
BT LIGHTNING SURGE TEST CIRCUIT



*C CHARGED TO 1500 VOLTS

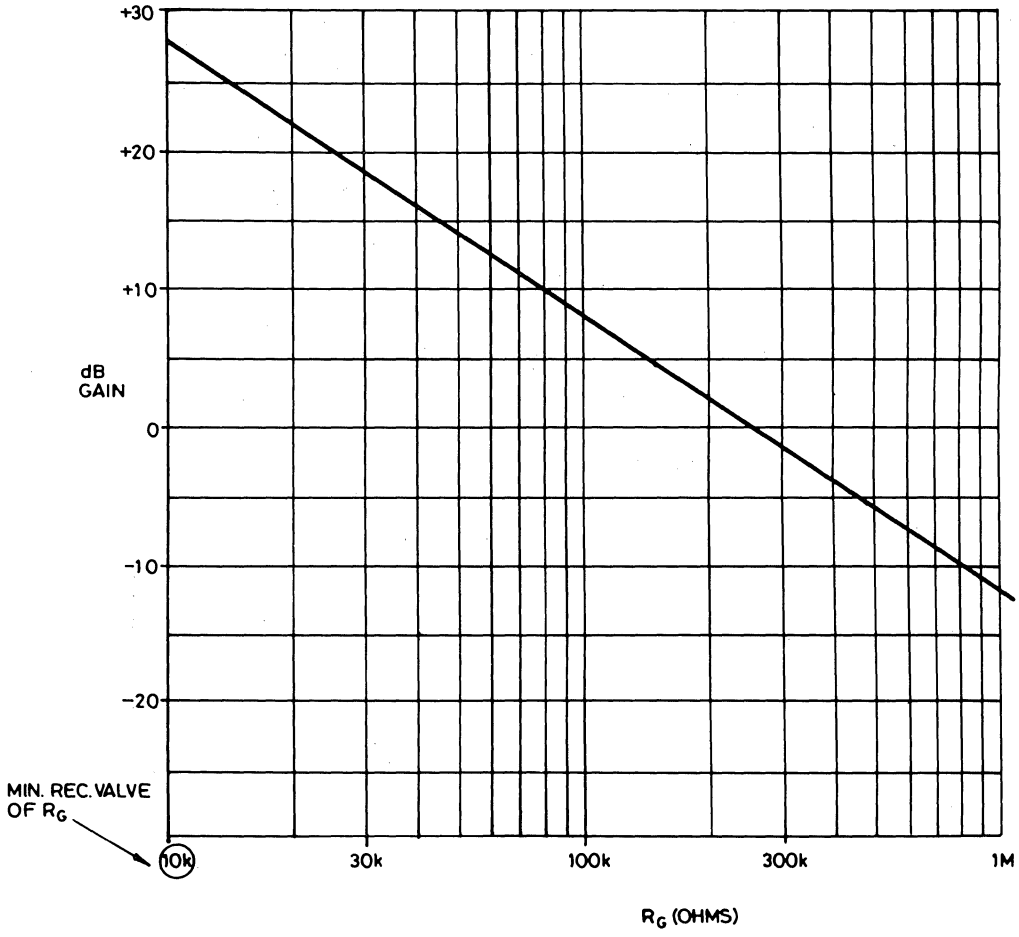
When the capacitor is fully charged the switch is closed thus discharging the capacitor into the test network. The device under test, DUT, is connected via a 15ohm resistor to the standard microphone wires. The DUT must survive the discharge on either line polarity.

Conditions $I_L = 50mA$



Gain (dB) vs Frequency (Hz)

Conditions $C_S = 1nF$ $C_G = 100nF$ $f = 1kHz$ $I_L = 50mA$



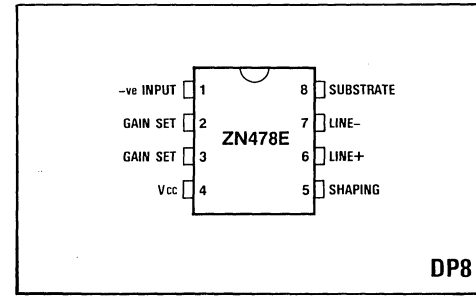
PLESSEY
Semiconductors

ZN478E

MICROPHONE AMPLIFIER FOR TELEPHONE CIRCUITS

FEATURES

- Low Working Voltage
- Designed to match electrets with FET buffers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits



Pin connections - top view

DESCRIPTION

The ZN478E was developed specifically for use with low impedance transducers such as electret microphones (with FET buffers) to replace the carbon transmitter in telephone handsets. The ZN478E is especially useful where a low operating voltage is required.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different low impedance transducer sensitivities.

This is a single polarity device and care should be taken over line connection.

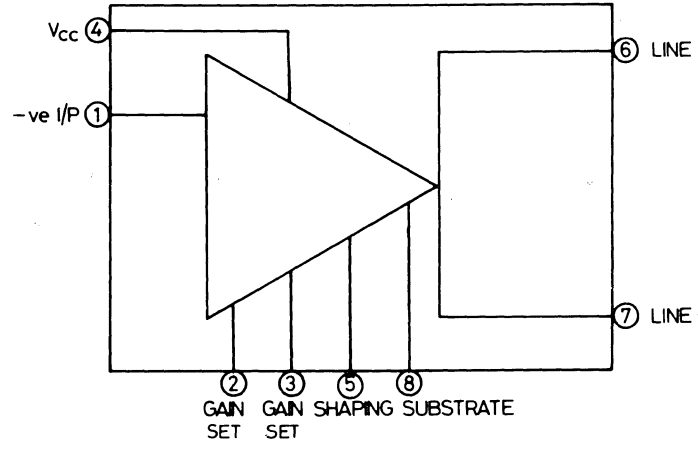


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous
Operating Temp. Range .. .. .. −20 to +80°C
Storage Temp. Range .. .. −55 to +125°C

A.C. CHARACTERISTICS

$T_{amb} = 25°C$ $R_G = 25k\Omega$ $R_L = 100\Omega$ $C_G = 100nF$ $R_O = 15\Omega$ $I_S = 50mA$ $C_S = 1nF$ $f = 1kHz$
$V_O = 300mV$ unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain	A_V	17	20	23	dB	
		–	28	–	dB	$R_G = 10k\Omega$ min. rec. value
Change in voltage gain from typical at $I_S = 50mA$ when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	$I_S = 100mA$
		−1	−0.5	+1	dB	$I_S = 20mA$
		–	−0.9	0	dB	$I_S = 10mA$
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	$V_O = 95mV$
		−1	−0.6	+1	dB	$V_O = 950mV$
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	$V_O = 300mV$
	DH(900)	–	4.5	6	%	$V_O = 900mV$

I_{FET} to be $\leqslant 1mA$

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$ $R_G = 25k\Omega$ unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	3.9	4.4	volts	$I_S = 21mA$
		4.3	4.6	–	volts	$I_S = 50mA$
		–	7.0	8.5	volts	$I_S = 100mA$

MICROPHONE AMPLIFIER APPLICATION

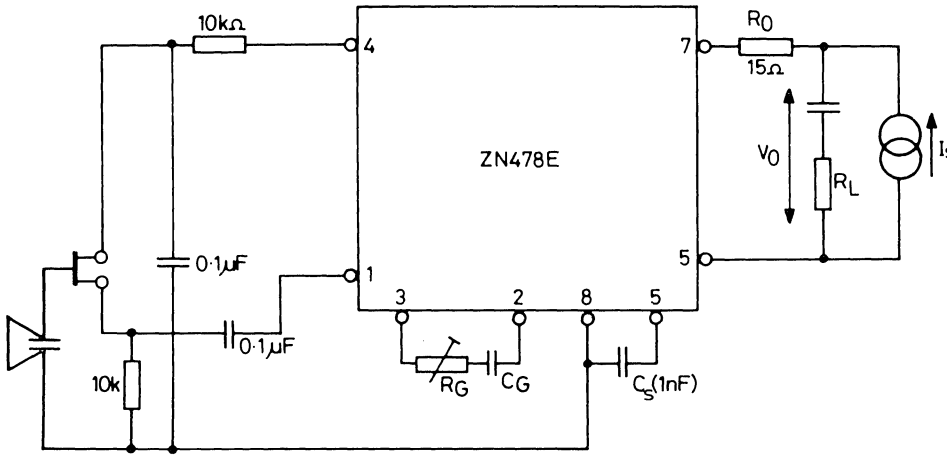


Fig. 2 Typical Application Circuit

The circuit shows ZN478E with a electret plus FET transducer in a typical telephone handset application but with load test included. The value of R_G is set to give the appropriate voltage gain for the particular transducer in use.

The value of the lower cut-off frequency f_L is determined by C_G and R_G from the expression

$$f_L \simeq \frac{1}{2\pi C_G(R_G + 500)}$$

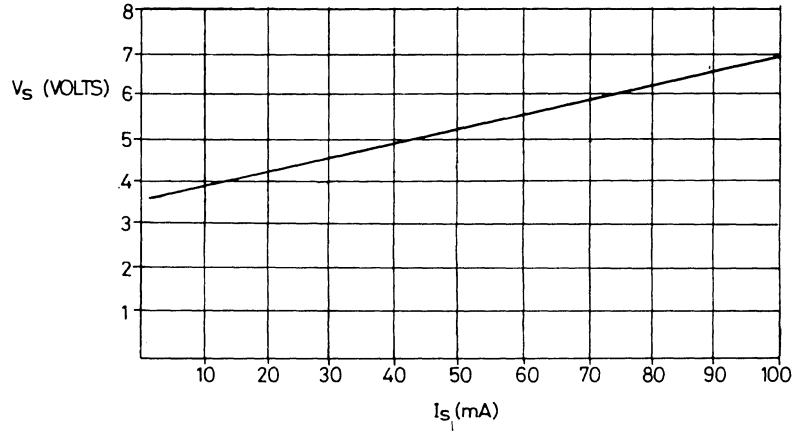
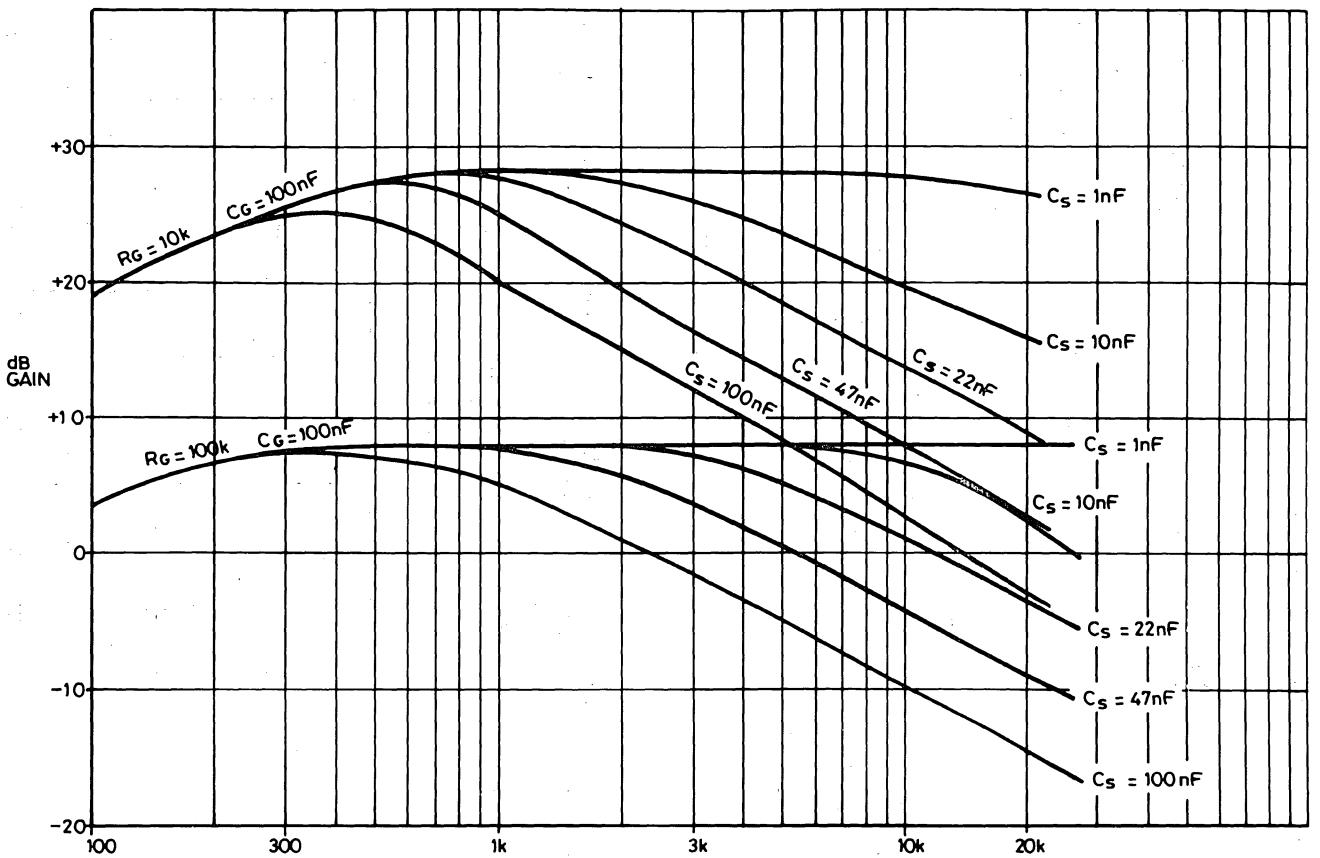


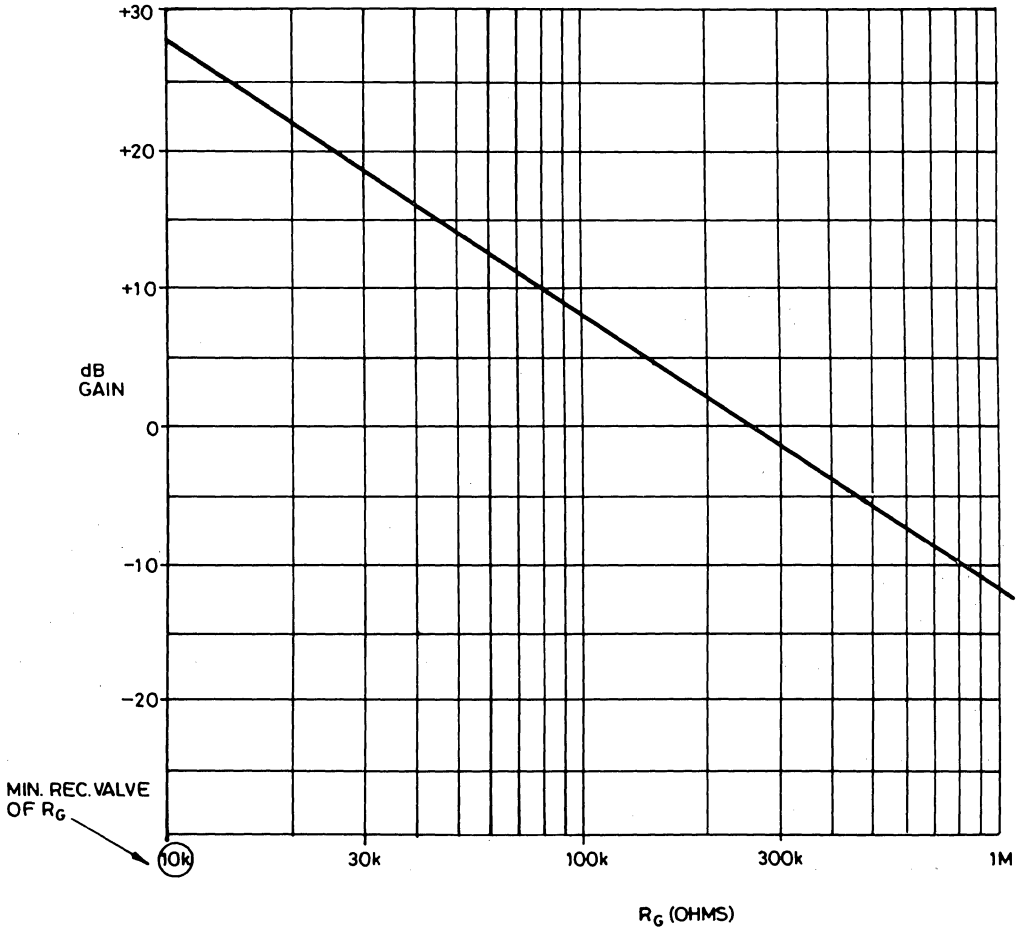
Fig. 3 Average Supply Voltage vs Supply Current for ZN478E

Conditions $I_L = 50mA$



Gain (dB) vs Frequency (Hz)

Conditions $C_S = 1nF$ $C_G = 100nF$ $f = 1kHz$ $I_L = 50mA$



ZN480E

RING DETECTOR

FEATURES

- Full rectifier bridge for direct operation from ringing supply
- Logic output
- Digital dial pulse rejection
- Frequency drift eliminated by ceramic resonator
- Built-in lightning protection
- Low external component count
- Built-in supply voltage regulator
- Supply voltage threshold
- 8 pin DIL package

DESCRIPTION

The ZN480E ring detector is intended for use when a special function is required in response to an incoming ringing signal.

A logic output is provided which can be interfaced to a wide variety of equipment including microprocessors, answering machines, modems, lamp indicators and opto-isolators.

The a.c. ringing voltage V_R is rectified by an on-chip bridge and used to power-up the complete circuit.

A standard 560kHz ceramic resonator is used to control the clock oscillator which provides a reference for the dial pulse rejection circuitry giving an active high only in the presence of a ringing signal.

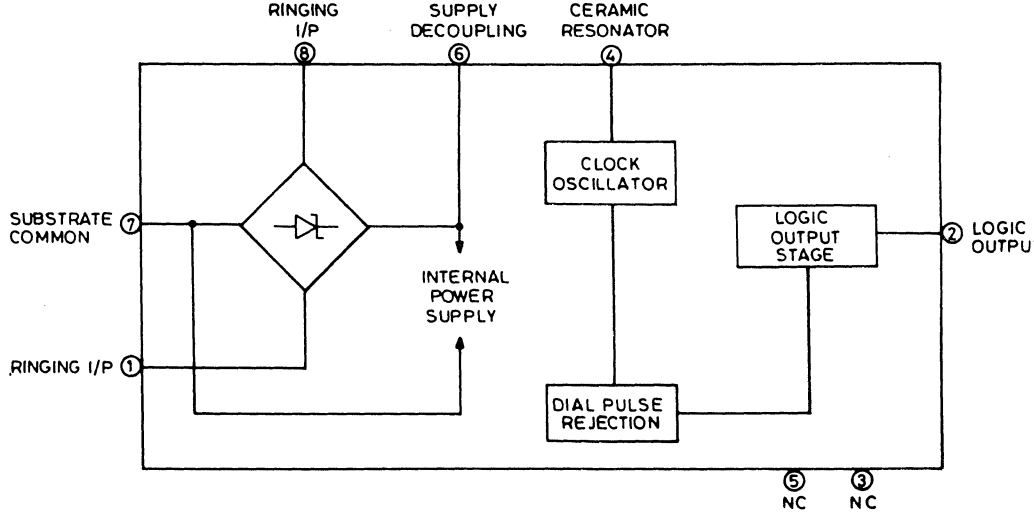


Fig. 1 System diagram

ABSOLUTE MAXIMUM RATINGS

Ringing input voltage, V_R	$100V_{rms}$
Power dissipation	500mW
Operating temperature	−20°C to +80°C
Storage temperature	−55 to +125°C

ELECTRICAL CHARACTERISTICS

$f_C = 560kHz$
$T_{amb} = 25°C$, $V_R = 75V$, $f_R = 25Hz$ unless otherwise stated. } (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOGIC OUTPUT (Note 2)						
Low level output voltage	V_{OL}	–	0.2	0.4	V	$I_{OL} = 3.6mA$
High level output voltage	V_{OH}	–	3.5	–	V	$I_{OH} = 1mA$
Threshold voltage	V_T	–	9	–	V	
Hysteresis of V_T	V_H	–	2.25	–	V	
Supply current (no load)	I_S	–	1	–	mA	$V_S = 20V$ (Note 3)
DIAL PULSE DISCRIMINATOR						
Acceptance frequencies	f_a	14	–	100	Hz	
Rejection frequencies	f_r	0	–	12	Hz	
Small signal standby impedance	Z_{in}	–	25	–	kΩ	$V_R = 1.5V$ $f_r = 1KHz$
Difference between turn-on and turn-off times (Note 4)	t_{diff}			100	mS	

Note 1 f_C = ceramic resonator frequency.
f_R = ringing frequency.

Note 2 On power-down, in the absence of ringing, the logic output impedance changes from a TTL compatible output to a high impedance state.

Note 3 V_S = d.c. test voltage applied to pin 6.

Note 4 The turn-on time is the time between the application of the ringing voltage and the output appearing at pin 2. Similarly the turn-off time is the time between removal of the ringing voltage and the output turning off.

CIRCUIT OPERATION

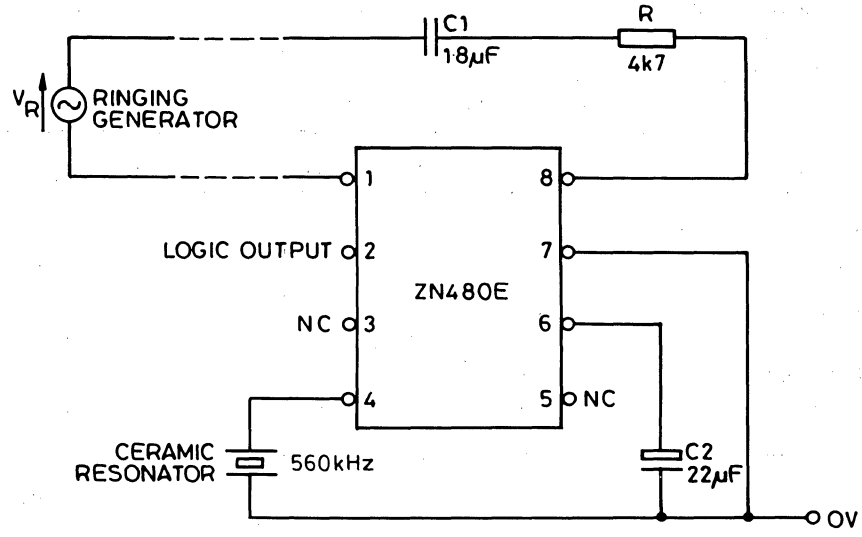


Fig. 2 Typical circuit - ring detector

The operation of the ZN480E is most readily explained with reference to a typical circuit as shown in Fig. 2.

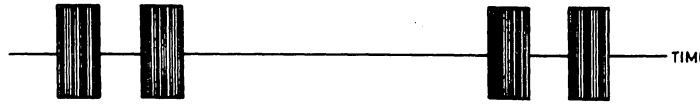
The incoming ringing voltage from the line, V_R, typically 75 volts 25Hz is connected to pins 1 and 8 via a d.c. blocking capacitor C_1, and a current surge limiting resistor R. This applies the ringing voltage to the built-in full wave rectifier bridge and the output is filtered by the reservoir capacitor C_2. This smoothed d.c. supply is then used to power up the remaining circuits.

An a.c. voltage appearing on the line causes the voltage across C_2 to rise but the output is inhibited until this voltage exceeds the threshold voltage, V_T, and the dial pulse discriminator has detected the presence of the correct ringing frequency.

The ringing supply frequency is normally between 14 and 66Hz, whereas dial pulses occur at 8 to 12Hz. A digital bandpass filter technique is used to differentiate between the two and allow the output when the ringing frequency is present.

The output from the dial pulse discriminator is used to drive a totem pole output stage.

OPERATING WAVEFORMS



(a) Typical a.c. ringing voltage (V_R)

(b) Logic output voltage at pin 2 for no load condition

Fig. 3 Waveform schematics

LIGHTNING PROTECTION

The I.C. is designed to withstand surges on the line provided a resistor, R in Fig. 2, is connected in series with the ringing input pins.

Using a value of R = 4k7 the device will survive and still operate to specification after a lightning simulation test as defined in Fig. 4.

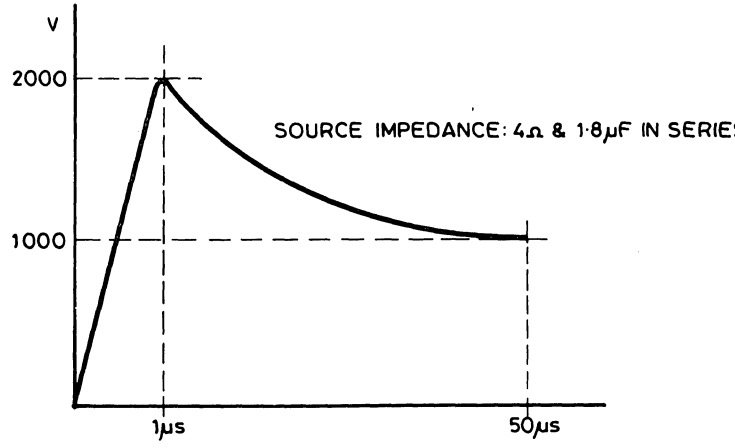


Fig. 4 Lightning surge test

APPLICATIONS

Interface circuits

The ring detector has a logic output (pin 2) which enables it to be used with TTL, microprocessors, lamp indicators, opto-isolators etc. in a wide variety of equipments such as answering machines, modems and PABX's. Depending on the application a buffer interface circuit may be required; examples of which are shown in Figs. 5 and 6 below.

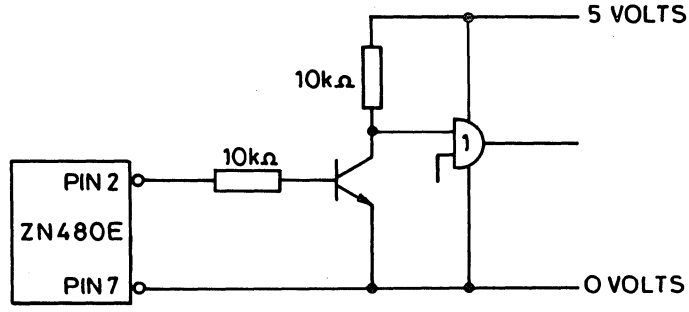


Fig. 5 Buffer to drive TTL

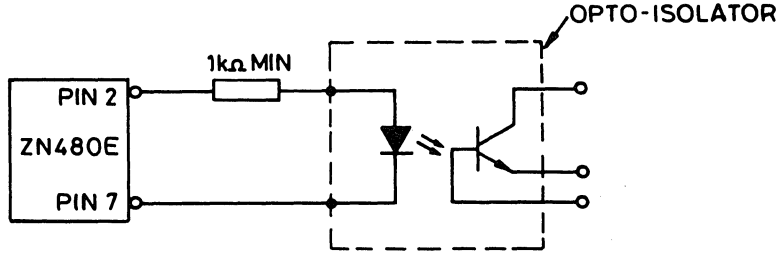


Fig. 6 Opto-isolator driver

Parallel operation

When a number of ring detectors are used in parallel for example in a private exchange it is possible to use a common ceramic resonator as shown in Figs. 7 and 8.

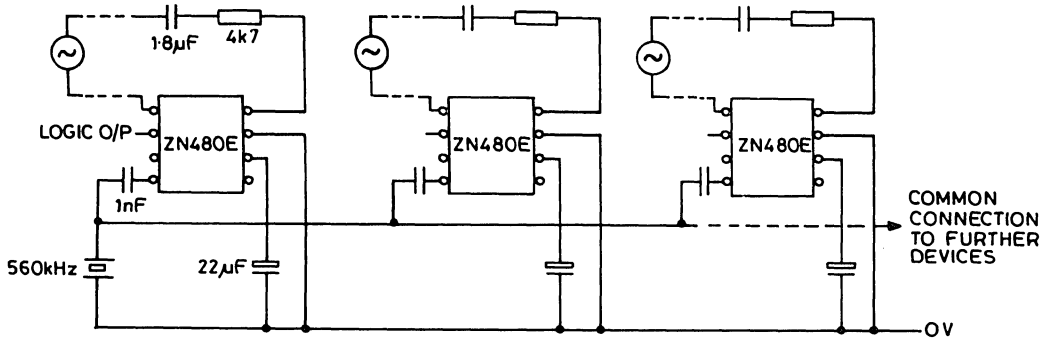


Fig. 7 Parallel operation using common ceramic resonator

In Fig. 7 each device is powered by its separate ringing voltage and isolated individually by supply decoupling capacitors.

When an external d.c. source of 15-20 volts is available, pin 6 of each device may be connected together to enable just one decoupling capacitor to be used; this is illustrated in Fig. 8. In a PABX for example this technique would clearly enable a reduced component count.

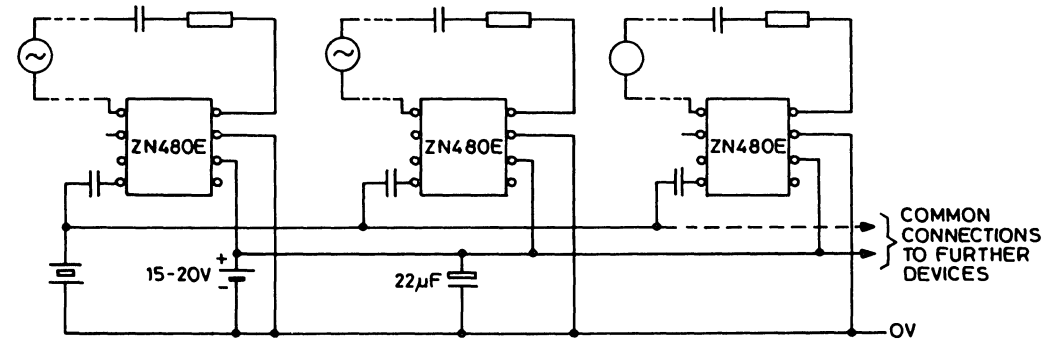
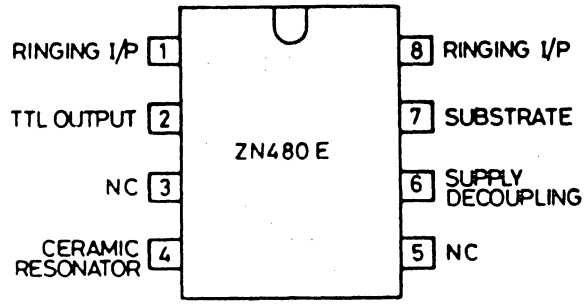


Fig. 8 Parallel operation using common ceramic resonator with external power-up

PIN CONNECTIONS



PLESSEY
Semiconductors

ZN488E

TONE RINGER

FEATURES

- Full rectifier bridge for direct operation from ringing supply
- Balanced output for electromagnetic transducers
- Single ended operation for piezo ceramic transducers
- Digital dial pulse rejection
- Frequency drift eliminated by ceramic resonator
- Choice of output tones
- Built-in lightning protection
- Low external component count
- Built-in supply voltage regulator
- Supply voltage threshold for noise immunity
- 8 pin DIL package

GENERAL DESCRIPTION

The ZN488E integrated circuit tone ringer is intended to replace existing electromechanical bells in telephone handsets

The A.C. ringing voltage normally supplied to energise the bell is rectified by an on-chip bridge and used to power up the complete circuit.

A standard 560KHz ceramic resonator is used to control the clock oscillator frequency which is then divided down to give two frequencies with a small separation. The output is switched between these two frequencies at 10Hz to give a warble tone.

Pin 5 is used to select output frequencies of either 1000Hz and 1250Hz or 1167Hz and 1333Hz. To prevent operation of the circuit on dial pulses a digital dial pulse rejection circuit inhibits the output except in the presence of the ringing supply.

The use of the ceramic resonator for clock control gives excellent tone frequency stability with temperature and life and eliminates complicated frequency setting procedures.

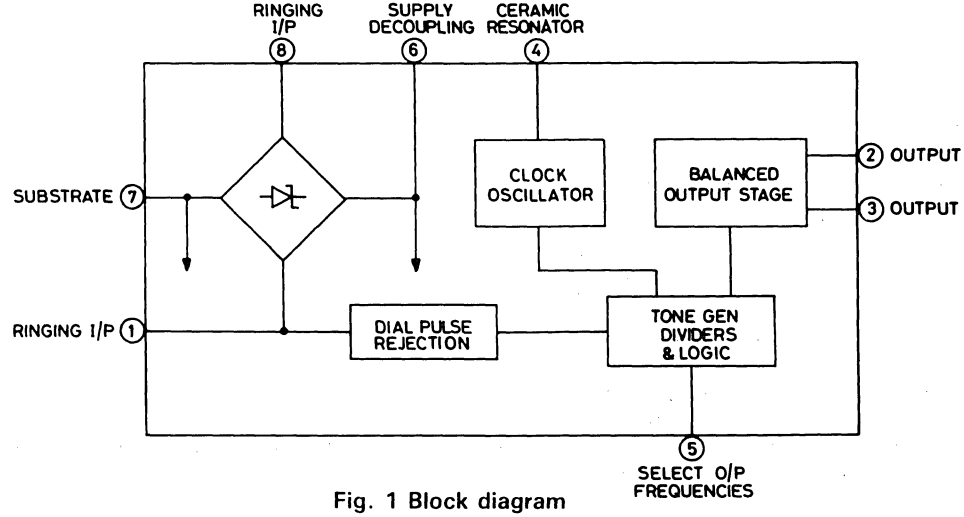


Fig. 1 Block diagram

ABSOLUTE MAXIMUM RATINGS

Ringing input voltage, (V_R)

a) approx. sinusoidal, via 1200Ω, 14-66Hz .. .. 100V RMS.

b) distorted sinusoidal, via 100Ω, 25Hz .. .. 53.7V RMS.

distorted sinusoidal, via 100Ω, 75Hz .. .. 29.6V RMS.

Power dissipation 500mW

Operating temperature .. .. −10 to +70°C

Storage temperature .. .. −55 to +125°C

ELECTRICAL CHARACTERISTICS

TEST CIRCUIT See Fig.4 $T_{amb} = 25°C$, $f_C = 560KHz$, $V_R = 75V$, $f_R = 25Hz$ unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High frequency O/P	f_{H1}	–	1333	–	Hz	Pin 5 to Pin 6
Low frequency O/P	f_{L1}	–	1167	–	Hz	
High frequency O/P	f_{H2}	–	1250	–	Hz	Pin 5 to Pin 7
Low frequency O/P	f_{L2}	–	1000	–	Hz	
Warble frequency	f_W	–	9.8	–	Hz	
Threshold voltage	V_T	–	9	–	V	
Hysteresis of V_T	V_H	–	2.25	–	V	
Supply current (no load)	I_S	–	0.25	0.45	mA	$V_S = 20V$ (Note 1)
Output voltage swing (balanced output)	V_O	50	56	–	Vp.p	$R_L = 3k\Omega$
Dial pulse discriminator:						
Acceptance frequencies	f_a	14	–	100	Hz	
Rejection frequencies	f_r	0	–	12	Hz	
Small signal standby impedance	Z_{in}	–	100	–	kΩ	$V_R = 1.5V$ $f_R = 1KHz$
Noise rejection (hum, speech)	V_r	–	5	–	V_{peak}	
Difference between turn-on and turn-off times. (Note 2)	t_{diff}	–	–	100	mS	

Note 1 V_S = D.C. test voltage applied to Pin 6.

Note 2 The turn-on time is the time between the application of the ringing voltage and the output appearing at Pins 2 & 3. Similarly the turn-off time is the time between removal of the ringing voltage and the output turning off.

LIGHTNING PROTECTION

The I.C. is designed to withstand lightning surges on the line provided a resistor, R in Fig. 3, is connected in series with the ringing input pins.

Using a value R = 2kΩ the device will survive and still operate to specification after a lightning simulation test as defined in Fig. 2.

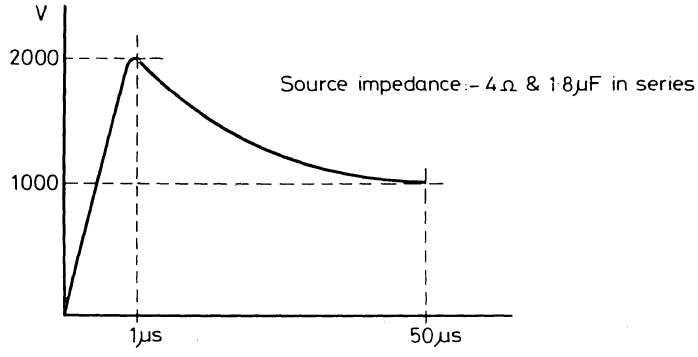


Fig. 2 Lightning surge test

CIRCUIT OPERATION

The operation of the ZN488E is most readily explained with reference to a typical circuit as shown in Fig. 3.

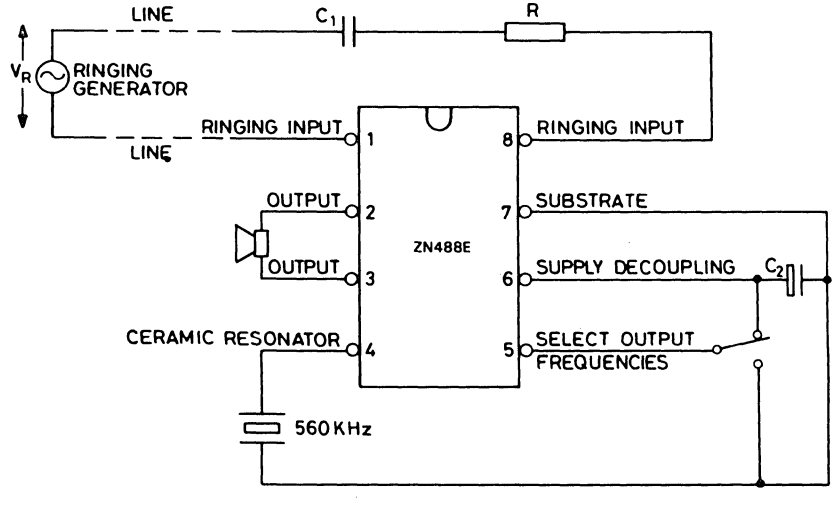


Fig. 3 Typical circuit

The incoming ringing voltage from the line, V_R, typically 70 volts 25Hz, is connected to pins 1 and 8 via a D.C. blocking capacitor C_1, and a current surge limiting resistor R. This applies the ringing voltage to the built-in full wave rectifier bridge and the output is filtered by the reservoir capacitor C_2. This smoothed D.C. supply is then used to power up the remaining circuits.

The frequency of the clock oscillator, F_C, is 560KHz nominal frequency. This is divided down to produce two audio tones f_{H1} and f_{L1} or, alternatively, f_{H2} and f_{L2} which are selectable using pin 5. The two selected frequencies are switched alternately to the output stage at a fixed rate f_W which is obtained by further frequency dividers.

This produces an insistent but pleasant warble tone. An A.C. voltage appearing on the line causes the voltage across C_2 to rise but the output is inhibited until this voltage exceeds the threshold voltage, V_T, and the dial pulse discriminator has detected the presence of the ringing supply.

The ringing supply frequency is normally between 14Hz and 66Hz whereas dial pulses occur at 10Hz to 12Hz. A digital bandpass filter technique is used to differentiate between the two and inhibit the output when dial pulses are present.

A balanced bridge output stage is used to deliver a square wave output, suitable for driving either electromagnetic or piezo ceramic transducers.

APPLICATIONS

- Replacement for electromechanical bell in telephone handsets.
- Ring detector/tone ringer in all-electronic telephones.
- Extension tone ringers.

The main application for the ZN488E is to perform the tone ringer function in all-electronic telephone handsets.

The figure below shows a typical application using the balanced bridge output stage. The bridge has an output of 50V pk-pk which is suitable for driving high output transducers such as electromechanical types.

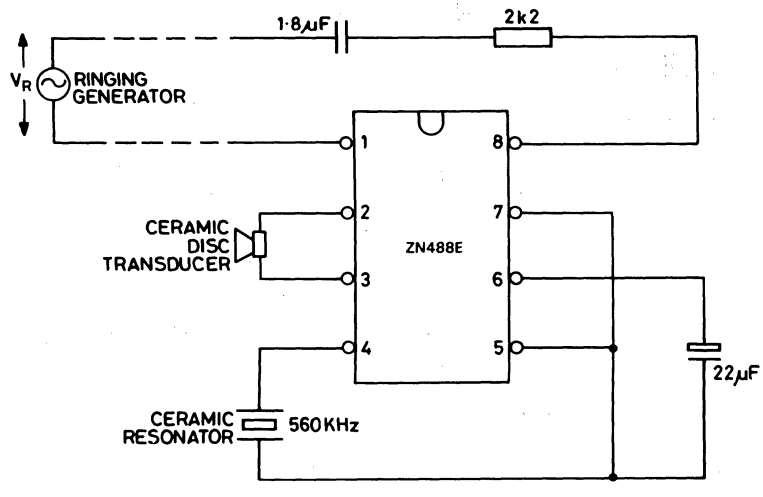


Fig. 4 Typical telephone application circuit - balanced output

In this example pin 5 is connected to pin 7 (substrate) which selects output frequencies f_{H2} and f_{L2}. No frequency setting up procedures are called for because the clock frequency, f_C, is set by the ceramic resonator. This also ensures very good frequency stability with ambient temperature changes and life.

Alternatively, when using piezo ceramic transducers, which require a lower driving voltage (typically 30V pk-pk max.), the transducer may be driven between either bridge output and substrate, as shown in fig. 5

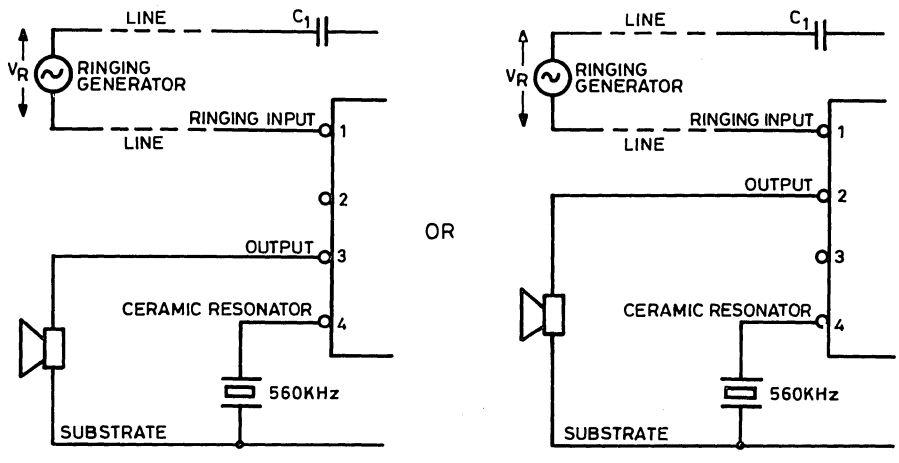
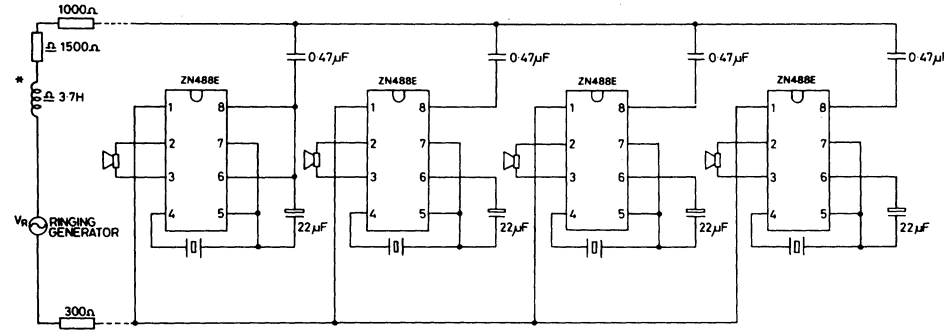


Fig. 5 Single ended operation

Up to four ZN488 circuits may be operated in parallel on a typical limit length line as shown in Fig. 6



*BT F-relay with 400Ω coil shorted and armature open

Fig. 6 Parallel operation on limit length telephone line

ZN482Z AND ZN483Z

BUFFER AMPLIFIERS FOR ELECTRET MICROPHONES

These buffer amplifiers were developed for use with an electret transducer where the two are mounted in close proximity in the telephone handset.

They are designed to withstand leakage path currents which can appear across the terminals of the amplifier due to the harsh environmental conditions of temperature and humidity which are imposed on the electret.

The high input impedance gives the suitable low frequency response whilst the low output impedance is capable of driving the line linking handset to the main body of the telephone.

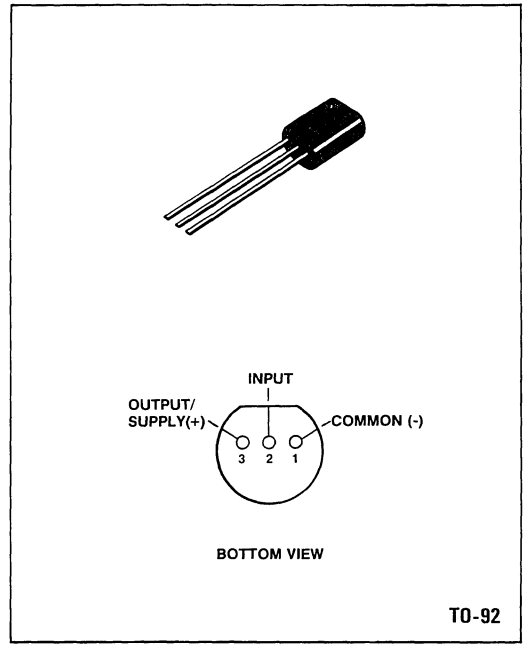


Fig.1 Pin connections

FEATURES

- Impedance Matching between Electret Microphone and Amplifier
- Low Insertion Loss (ZN483Z)
- High Input Impedance
- Low Output Impedance
- Low Noise
- Low Distortion
- Low Operating Current
- High Tolerance to Input Leakage Resistance

BUFFER AMPLIFIER APPLICATION

The input voltage V_{IN} represents the speech signal into the electret microphone of capacitance C_S. Leakage resistances R_L (as shown above) represent the current paths which can result between the terminals of the amplifier in the microphone handset as a result of environmental conditions. A steady current I_{DC} is established from the supply voltage V_S through a dropper resistor R1. The operating voltage V_{DC} is set-up on pin 3 with respect to pin 1.

Graphical information is provided in Figs.3 to 18 to support the design engineer wishing to use this device in the chosen system application. The symbols used on these graphs are indicated in Fig.2.

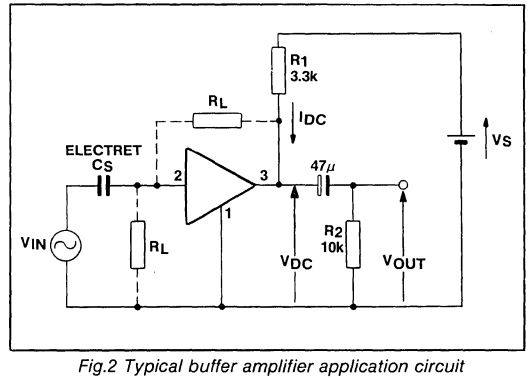


Fig.2 Typical buffer amplifier application circuit

ABSOLUTE MAXIMUM RATINGS

Supply current	50mA continuous
Operating temperature range	−20°C to +60°C
Storage temperature range	−55°C to +125°C

DC CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Parameter	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating current	I_{DC}	0.15		25	mA	
Operating voltage	V_{DC}	1.6	1.85	2.0	V	I_{DC} = 0.3mA See Fig.3 (ZN482Z) See Fig.11 (ZN483Z)

AC CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C, I_{DC} = 0.3mA, f = 1kHz, V_{IN} = 100mVrms, C_S = 38pF

Parameter		Symbol	Value			Units	Conditions
			Min.	Typ.	Max.		
Voltage gain	ZN482Z	A_V	-5.5	-5	-4.5	dB	See Figs.4 and 5
	ZN483Z	A_V	-1.5	-0.5	0	dB	See Figs.12 and 13
Input resistance		R_{IN}		50		MΩ	
Input capacitance		C_{IN}		10		pF	
Total harmonic distortion		THD		0.14	2.0	%	See Figs.6 - 8 (ZN482Z) See Figs.14 - 16 (ZN483Z)
Output noise	ZN482Z	V_{ON}		3.5		μV	
	ZN483Z			5.5			
Lower cut-off frequency		f_{LCO}		65	150	Hz	C_S = 38pF
Upper cut-off frequency							
	ZN482Z	f_{UCO}		95		kHz	
	ZN483Z			50			
Output resistance		R_{OUT}		50		Ω	See Fig.9 (ZN482Z) See Fig.17 (ZN483Z)
Gain leakage loss							
See Fig.10 (ZN482Z)				6		dB	R_L = 40MΩ between pins 1 & 2
				0.4		dB	R_L = 40MΩ between pins 2 & 3
See Fig.18 (ZN483Z)				5		dB	R_L = 40MΩ between pins 1 & 2
				0.4		dB	R_L = 40MΩ between pins 2 & 3

NOTE
1. Output noise is measured through a psophometer (CCITT recommendation P53). The normal units of dBmp for this measurement have been converted into microvolts.

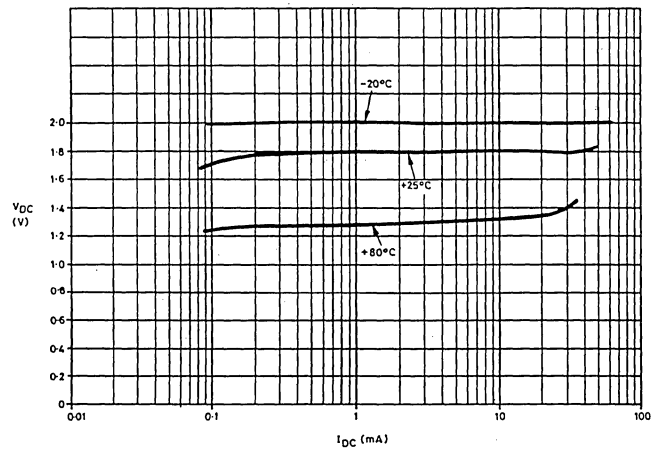


Fig.3 DC voltage v current (ZN482Z)

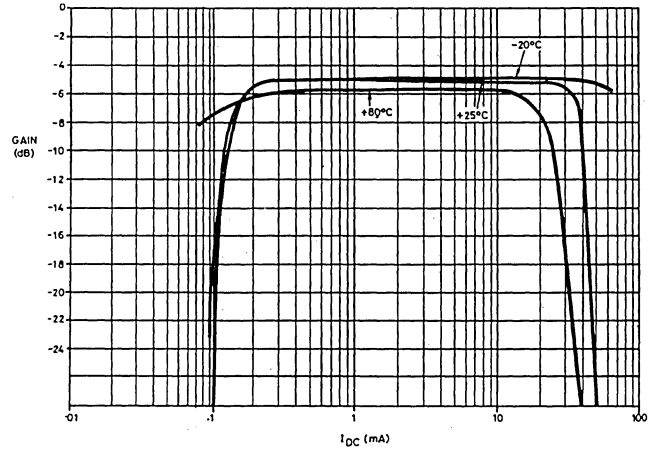


Fig.4 Gain v current (ZN482Z)

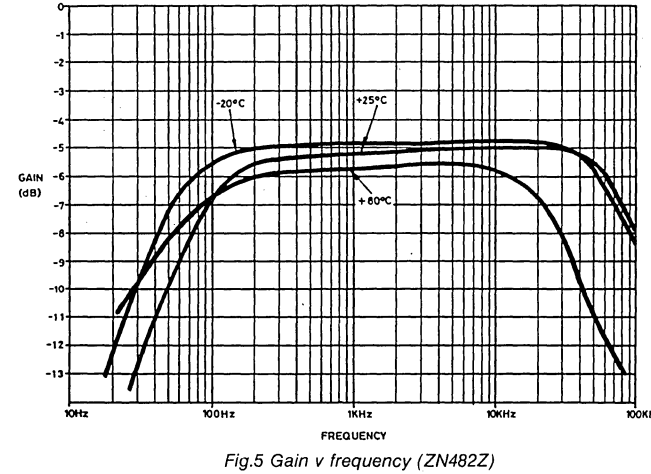


Fig.5 Gain v frequency (ZN482Z)

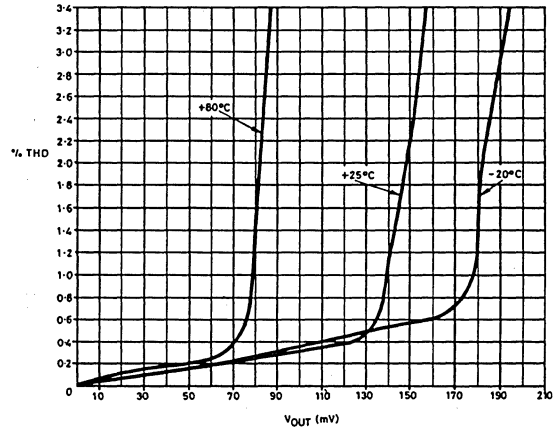


Fig.6 Distortion v output voltage (ZN482Z)

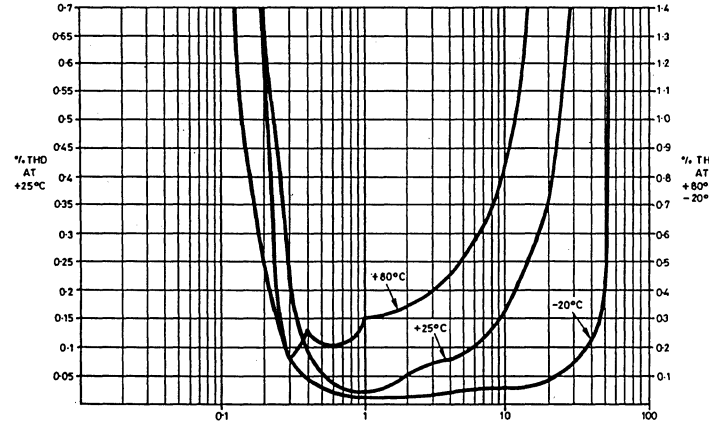


Fig.7 Total harmonic distortion v current (ZN482Z)

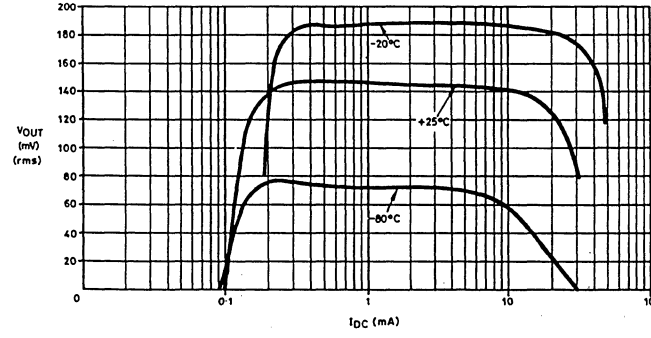


Fig.8 Output voltage v current at 2% THD (ZN482Z)

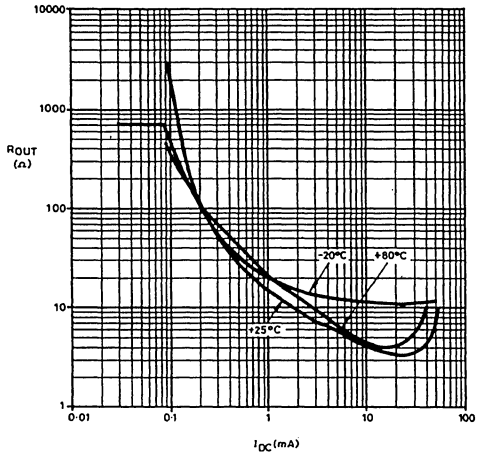


Fig.9 Output resistance v current (ZN482Z)

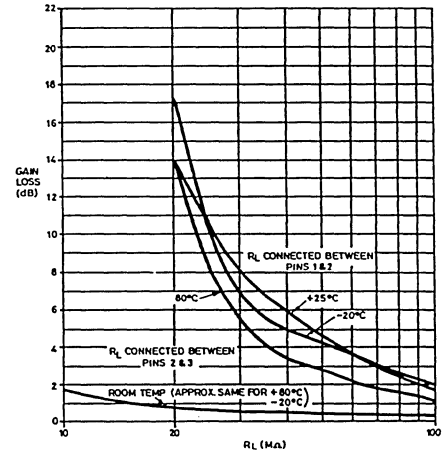


Fig.10 Gain leakage loss v leakage resistance (ZN482Z)

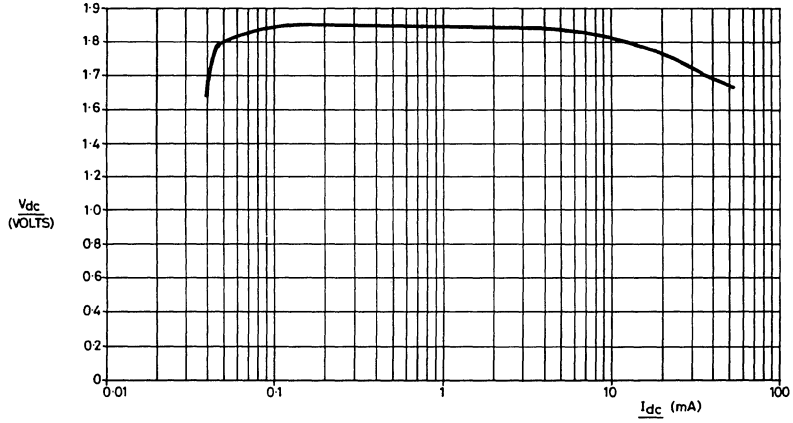


Fig.11 DC voltage v current (ZN483Z)

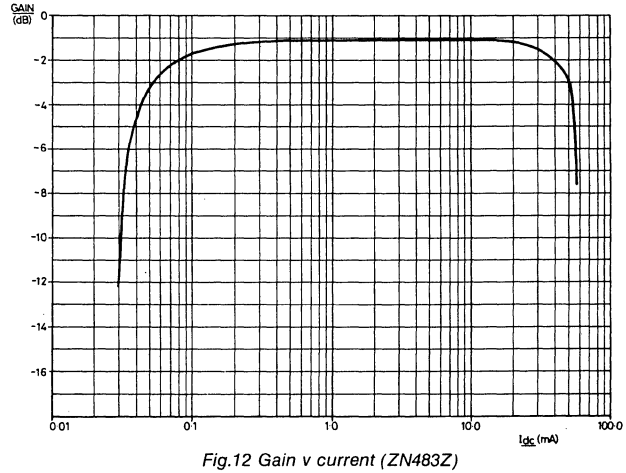


Fig.12 Gain v current (ZN483Z)

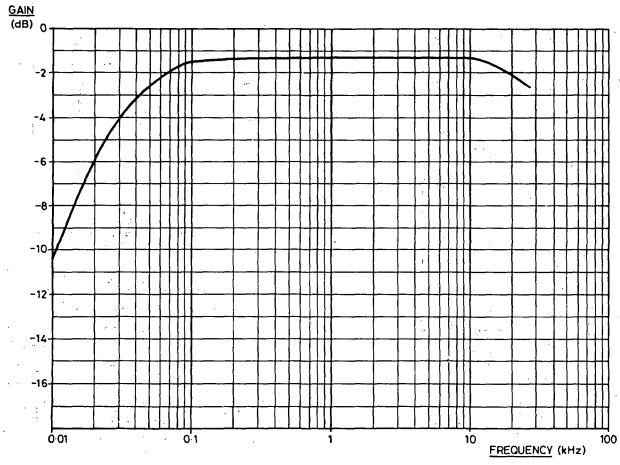


Fig.13 Gain v frequency (ZN483Z)

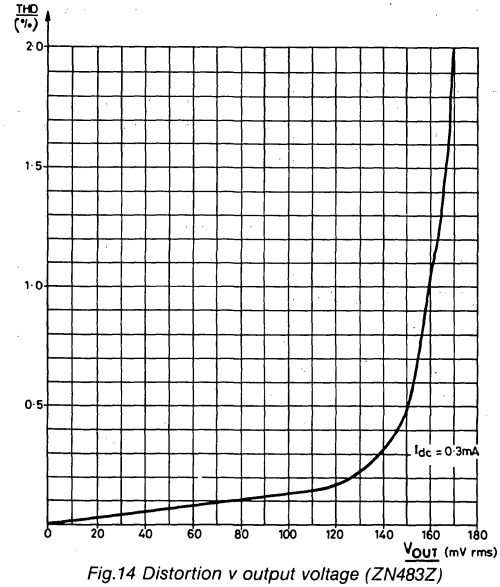


Fig.14 Distortion v output voltage (ZN483Z)

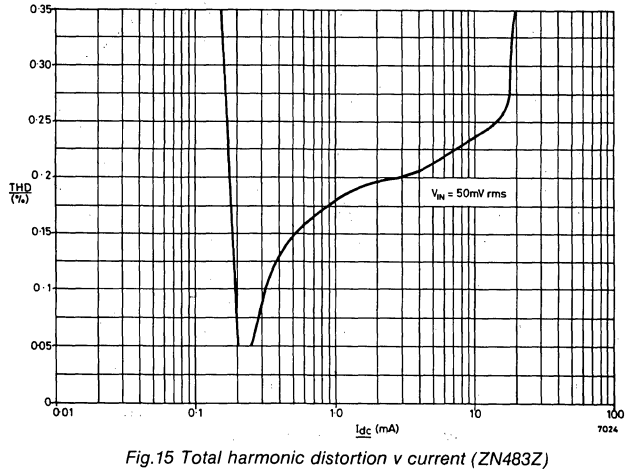


Fig.15 Total harmonic distortion v current (ZN483Z)

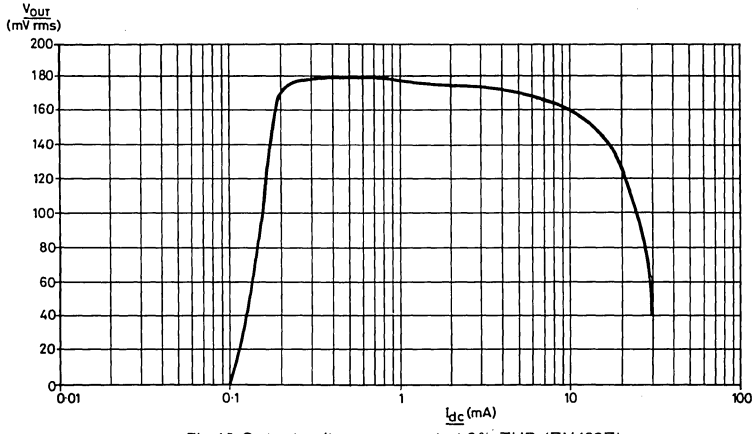


Fig.16 Output voltage v current at 2% THD (ZN483Z)

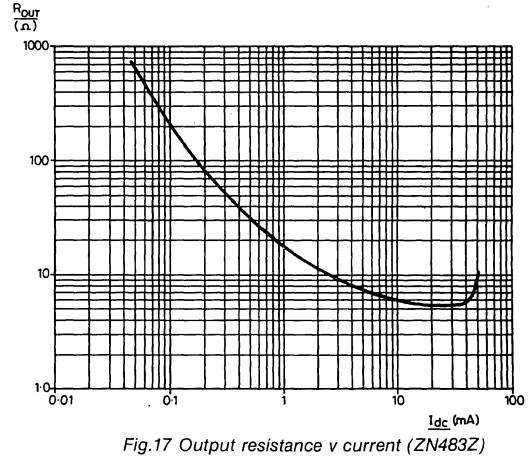


Fig.17 Output resistance v current (ZN483Z)

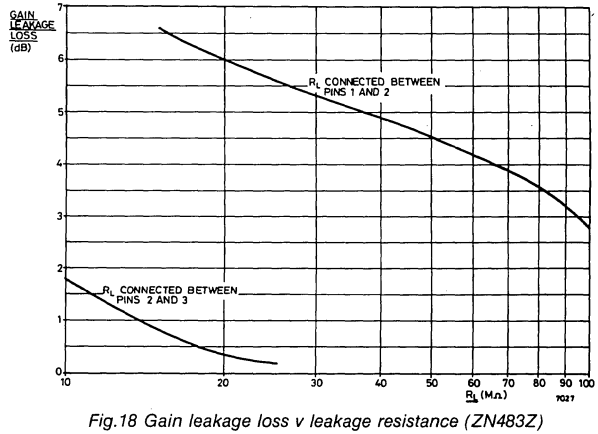


Fig.18 Gain leakage loss v leakage resistance (ZN483Z)

ZN1003

EIGHT CHANNEL TIME-SLOT ASSIGNER

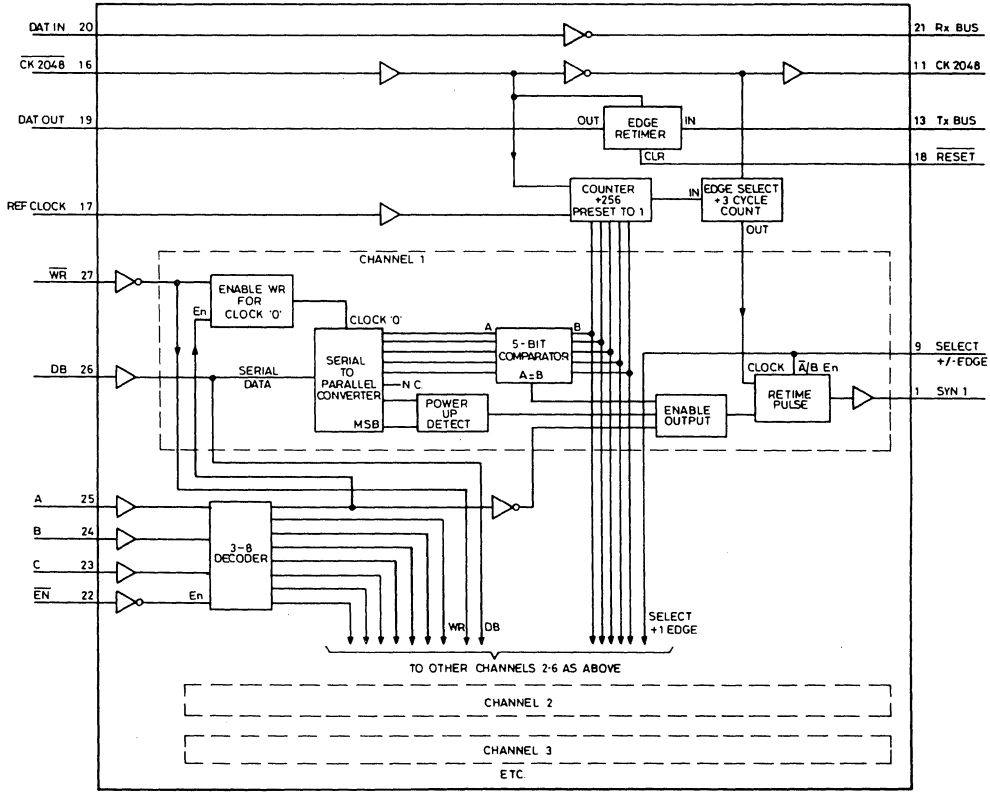
FEATURES

- Dynamic time-slot assignment
- Clock buffering
- DATOUT buffering and retiming
- Direct microprocessor control
- Syn pulse derived from either edge of the 2.048MHz clock

GENERAL DESCRIPTION

The ZN1003 Eight Channel Time-slot Assigner has been designed in conjunction with British Telecom for use with those single chip codec/filters which do not have a time-slot assignment function built-in. The TSAC operates under the control of the board intelligence and provides synchronous pulses to each of up to eight devices. The synchronising pulses are of 8 clock cycles duration and can be selected to be derived from either the rising or the falling edge of the 2.048MHz clock.

The TSAC will be able to drive the majority of codec/filter devices. Also provided on the chip are waveform buffers and a re-timing circuit for the PCM signals.



System Diagram ZN1003

ABSOLUTE MAXIMUM RATINGS

Supply voltage .. .. +7.0 volts
Operating temperature range .. .. .. 0 to 70°C
Storage temperature range .. .. −55 to +125°C

D.C. CHARACTERISTICS (over operating temperature range V_{CC} = 4.75 to 5.25 volts)

Parameter		Test Conditions	Min.	Typ.	Max.	Units
Supply current				77	113	mA
Low level input voltage	All Inputs		0		0.8	V
Low level input current	All Inputs except Pin 16	V_{IN} = 0V		−0.34	−0.6	mA
	Pin 16	V_{IN} = 0V		−1.0	−1.6	mA
High level input voltage	All Inputs		2.0		V_{CC}	V
High level input current	All Inputs except Pin 16	$V_{IN} = V_{CC}$			10	μA
	Pin 16	$V_{IN} = V_{CC}$			20	μA
Low level output voltage	All Outputs	I_{OL} = 8mA			0.5	V
High level output voltage	All Outputs	I_{OH} = 400μA	2.4			V

FUNCTIONAL DESCRIPTION

Time-slot Assignment Operation

This is the main area of the chip and can be regarded as eight separate channels 1-8, port select area, time count area and +/− select.

The basic function of a channel is to convert the serial data information on DB, from the card controller into a positive pulse at the syn 'n' output pin at a fixed time relative to an externally provided control pulse. When a channel is not active no pulse is produced at the associated syn output.

PORT SELECT

One of eight ports is selected using binary coded information presented to the ZN1003 on input lines A, B and C. The code is valid when $\overline{EN}$ is low. During the period when $\overline{EN}$ is low, eight bits of serial data on DB containing time-slot and power up/down information are clocked into the selected ports serial to parallel converter under the control of the $\overline{WR}$ signal. (SEE TABLES 1, 2, and 3).

Table 1 Port Select

A	B	C	$\overline{EN}$	Syn 1	Syn 2	Syn 3	Syn 4	Syn 5	Syn 6	Syn 7	Syn 8
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Control Word

P2	P1	N.U.	T5	T4	T3	T2	T1

MSB LSB

N.U. = Not used

Table 2 Time Slot Selection

T5	T4	T3	T2	T1	Time Slot
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	31

Table 3 Power Up/Down Selection

P2	P1	Status
0	0	Power Up
0	1	Power Down
1	0	Power Down
1	1	Power Down

TIME COUNT

$\overline{\text{REF CLOCK}}$ resets a synchronous counter to +1, clocked at 2.048MHz the counter will give a count of 256 before the next reset pulse. Outputs are taken so as to give 32 period counts of 8 cycles of 2.048MHz. i.e. one for each timeslot.

SELECT +/−EDGE

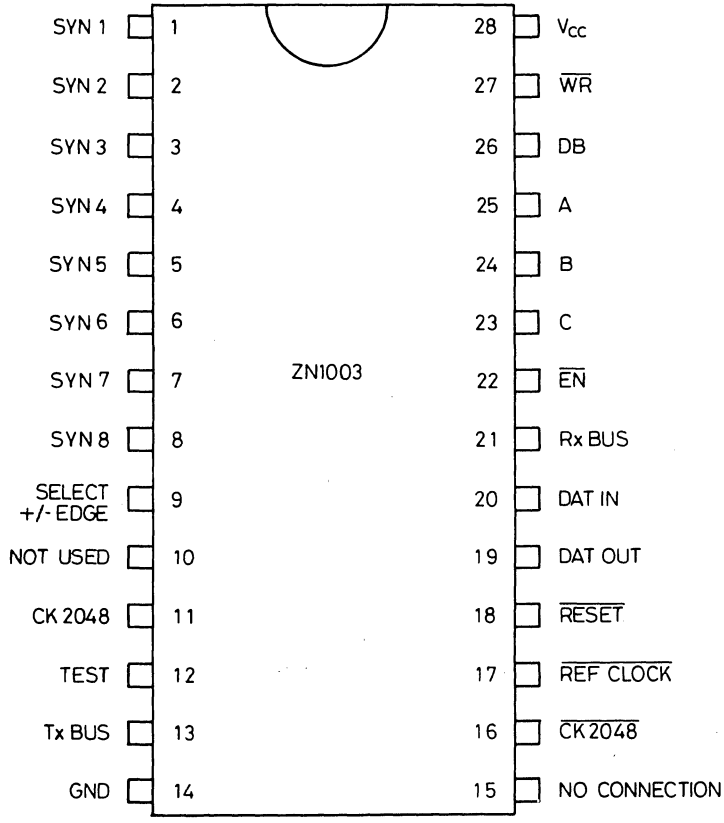
The syn 'n' output is the frame syn pulse for the Codec/filter devices. PCM is coded/decoded relative to this pulse and the 2.048KHz clock. Some manufacturers require the frame syn pulse to be relative to the rising edge, others to the falling edge of the 2.048KHz clock. Applying a positive condition to the select pin enables the frame syn pulse to be driven from the rising edge, an earth on the select pin, from the falling edge.

CLOCK BUFFERING

The 2.048MHz clock required to drive the codec/filter chips is derived from the $\overline{\text{2.048MHz}}$ clock used by the ZN1003 thus inversion and buffering is provided on chip.

DATOUT BUFFERING AND RETIMING

Datout is buffered by the ZN1003 and retimed by $\overline{\text{2048}}$ clock to ensure correct phase relationship on the output.


SYN 1
1
SYN 2
2
SYN 3
3
SYN 4
4
SYN 5
5
SYN 6
6
SYN 7
7
SYN 8
8
SELECT +/- EDGE
9
NOT USED
10
CK 2048
11
TEST
12
Tx BUS
13
GND
14
ZN1003
28
V_{CC}
27
$\overline{WR}$
26
DB
25
A
24
B
23
C
22
$\overline{EN}$
21
Rx BUS
20
DAT IN
19
DAT OUT
18
$\overline{RESET}$
17
$\overline{REF\ CLOCK}$
16
$\overline{CK2048}$
15
NO CONNECTION

Pin Description

No.	Name	Function
25 24 23	A B C	Parallel data on these three pins is the address of the 8 ports.
22	$\overline{EN}$	Enabling pulse for the selected port address on the A, B and C pins held low while 8 $\overline{WR}$ pulses input 8 bits of serially encoded data into the ZN1003.
26	DB	8 bit serially encoded data derived from the binary representation of the selected timeslot for a particular port, plus, two bits to represent power up/power down.
27	$\overline{WR}$	Write pulse for DB. DB is read into the ZN1003 on the rising edges of the $\overline{WR}$ pulses.
18	$\overline{RESET}$	Upon receipt of logic '0' on this I/P pin, the ZN1003 will reset all timeslots to zero.
9	+/−SELECT	A +ve 5V or ground applied at this pin selects whether the syn output is derived from the rising edge of the 2048 clock or the falling edge.
19	DATOUT	Speech data highway for data from the codec/filter chip to the line unit edge connector, after edge retiming of the Tx BUS on the ZN1003.
20	DATIN	Speech data highway for the data from the line unit edge connector to the codec/filter chip via the ZN1003. After buffering and inversion becomes Rx BUS.
13	Tx BUS	PCM data from the codec/filter chip to the ZN1003.
21	Rx BUS	PCM data from the ZN1003 to the codec/filter chip.
17	$\overline{REF\ CLOCK}$	Timing signal of approximately 1 cycle of the 2048kHz clock in duration, repetition rate of 8kHz. Used as the framing signal for the ZN1003. It is synchronised to the 2048kHz clock.
16	$\overline{CK2048}$	Master clock for the system used for timing on the ZN1003
11	CK2048	Inverted master clock $\overline{2048}$, used for timing of the codec/filter chip etc. outgoing from the ZN1003 to the codec/filter chip.
1 to 8	Syn 1 to Syn 8	Frame syn pulse, a positive pulse of 8 periods of the 2048 clock for each individual codec/filter chip generated by the ZN1003 in a selected timeslot, referenced to the 2048 and REF CLOCK signals.

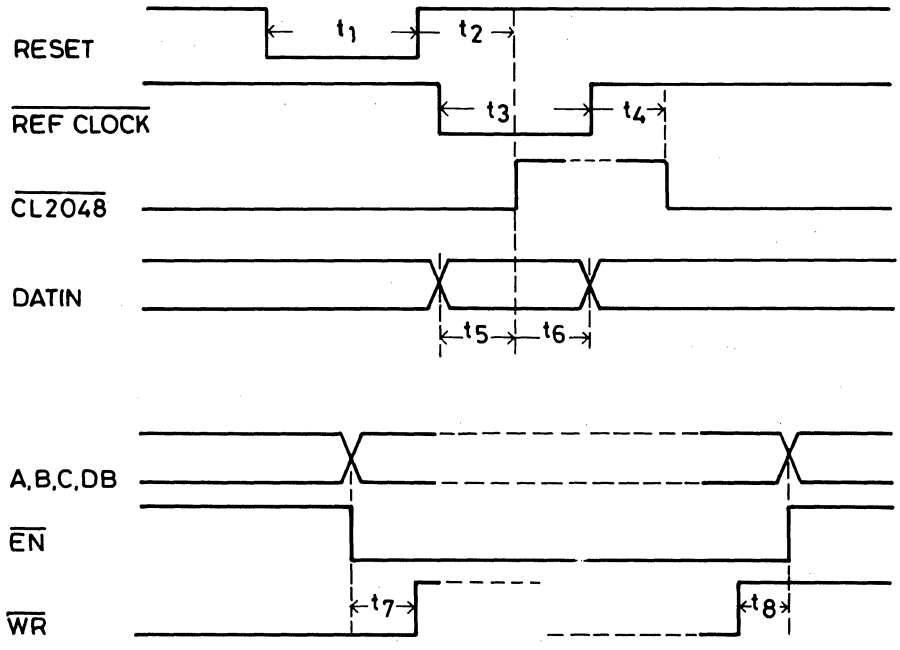
Input Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_1	Reset pulse width	50			nS
t_2	Delay from rising edge reset pulse to rising edge of $\overline{CK2048}$	25			nS
t_3	Reference clock pulse width	100			nS
t_4	Delay from rising edge reference clock to falling edge of $\overline{CK2048}$	50			nS
t_5	Delay from DATIN to rising edge of $\overline{CK2048}$	60			nS
t_6	Delay from rising edge of $\overline{CK2048}$ to DATIN	50			nS
t_7	Delay from A,B,C, and DB to the write pulse	70			nS
t_8	Delay from rising edge write pulse to A,B,C, and DB	100			nS

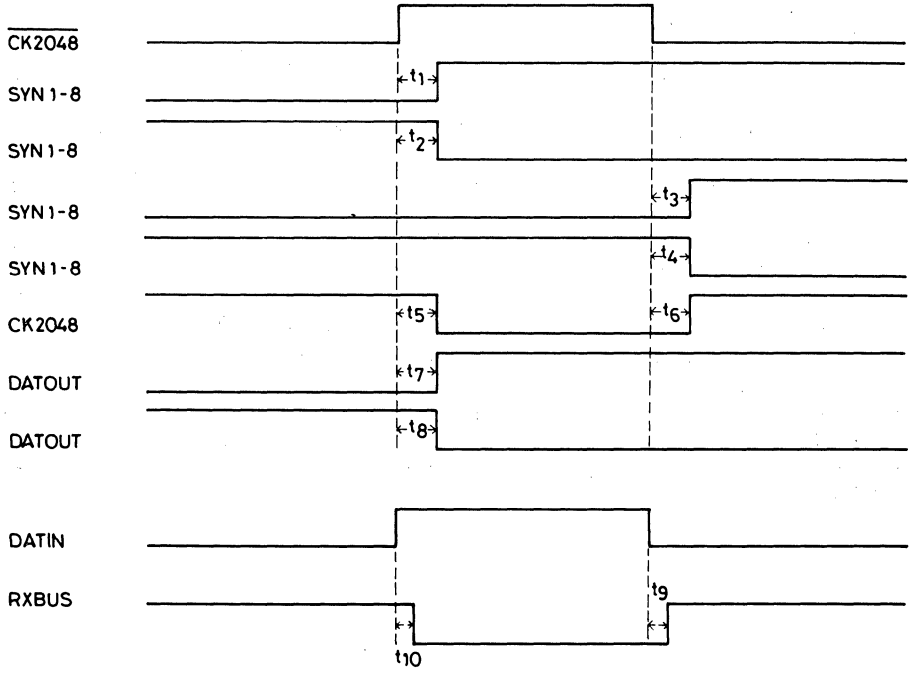
Output Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_1	Syn out rising edge delay from rising edge $\overline{CK2048}$. $C_L = 300pf$	60	100	170	nS
t_2	Syn out falling edge delay from rising edge $\overline{CK2048}$. $C_L = 30pF$	60	100	170	nS
t_3	Syn out rising edge delay from falling edge $\overline{CK2048}$. $C_L = 30pF$	60	100	170	nS
t_4	Syn out falling edge delay from falling edge $\overline{CK2048}$. $C_L = 30pF$	60	100	170	nS
t_5	Delay from rising edge $\overline{CK2048}$ to falling edge CK2048. $C_L = 480pF$	22	31	53	nS
t_6	Delay from falling edge $\overline{CK2048}$ to rising edge CK2048. $C_L = 480pF$	25	36	61	nS
t_7	Delay from rising edge $\overline{CK2048}$ to rising edge DATOUT	35	51	90	nS
t_8	Delay from rising edge $\overline{CK2048}$ to falling edge DATOUT	30	42	75	nS
t_9	Delay from rising edge DATIN to falling edge R_X bus	22	32	55	nS
t_{10}	Delay from falling edge DATIN to rising edge R_X bus	20	29	50	nS
	DATOUT delay from falling edge $\overline{CK2048}$. $C_L = 120pF$	30		106	nS
	$\overline{CK2048}$ rise time or fall time			50	nS

C_L = Load Capacitance



Input Timing Requirements



Output Timing Requirements

PLESSEY
Semiconductors

ZN5683E/J

PCM LINE INTERFACE CIRCUIT

The ZN5683E/J is a PCM line interface circuit suitable for 2.048Mbit/s or 8.448Mbit/s PCM systems. It contains both transmit and receive channels in a single 18 pin dual in-line package. The incoming bipolar PCM signal, which has been attenuated and distorted by the cable is processed by the receiver to extract Data–, Data + and clock signals. These are then level shifted to TTL levels suitable for further digital processing.

In the transmit direction the TTL data input is used to drive a centre tapped transformer, which is used to interface with the transmission line.

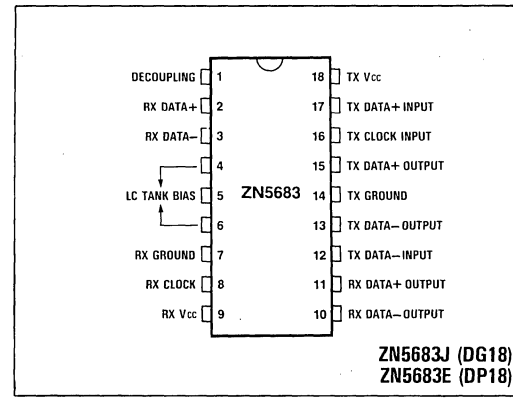


Fig.1 Pin connections - top view

FEATURES

- Operation up to 8.448Mbit/s in both Transmit and Receive Directions
- Supports Balanced and Unbalanced Receiver Inputs
- Single +5V Supply
- TTL Compatible
- Suitable for T1, T2, 2.048 and 8.448Mbit Systems
- 18 Pin Ceramic or Plastic DIL

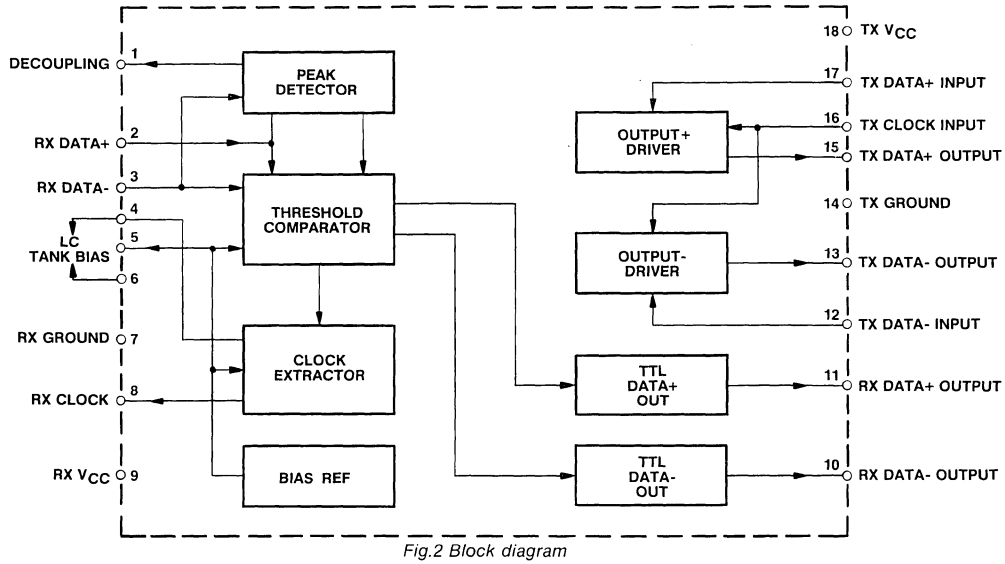


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} : -40°C to +85°C, V_{CC} +5V ± 0.25V

DC CHARACTERISTICS

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Supply current	I_{CC}			35.0	60.0	mA	Output drivers open
Low level input current - data	I_{ILD}	12, 17	-200		-50	μA	V_{IN} = 0V
Low level input current - clock	I_{ILC}	16	-400		-100	μA	V_{IN} = 0V
Low level output voltage - clock	V_{OLC}	8		0.4	0.8	V	I_{CL} = 2mA
High level output voltage - clock	V_{OHC}	8	3	3.6		V	
Low level output voltage - data	V_{OLD}	10, 11		0.4	0.8	V	I_{CL} = 2mA
High level output voltage - data	V_{OHD}	10, 11	3	3.6		V	
Low level output voltage - line driver	V_{OLO}	13, 15	0.6	0.8	0.9	V	See Note 3
High level output current - line driver	I_{OHO}	13, 15			100	μA	
Output driver current sink	I_{OLO}	13, 15			40	mA	
Input voltage		2, 3		3	3.3	V	See Note 4

AC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output driver rise time	t_{ro}		20	25	ns	See Note 5

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply voltage, V_{CC}	+20V
Input voltage, V_{IN} (See Note 2)	-0.3V to +20V
Current sink	40mA
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C

NOTES
1. The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.
2. V_{IN} = input voltage relative to pins 7, 14.
3. Measured at pins 13, 15 with 300 Ohms pull up to 5.0V.
4. Per CCITT G.703 pulse mask. See Fig.3.
5. Measured at pins 13, 15 with 150 Ohms pull up to 5.0V.

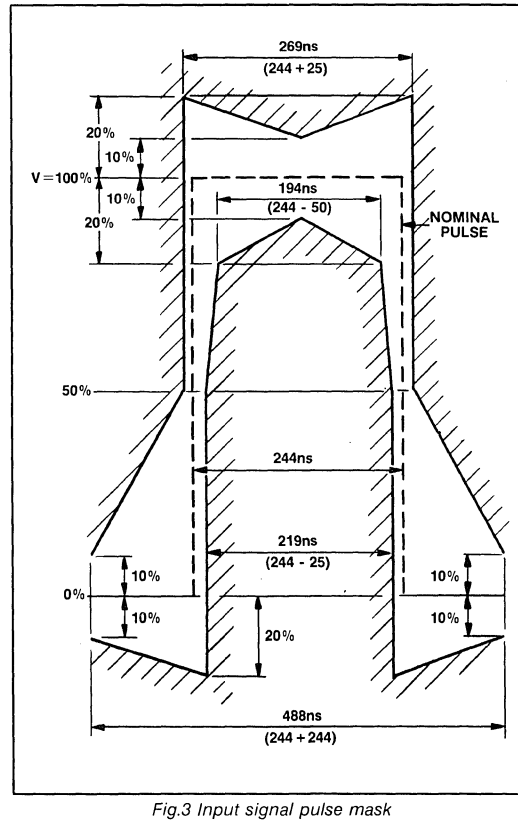


Fig.3 Input signal pulse mask

PIN DESIGNATION

Pin No.	Name	Description
1	Decoupling	Pin for connection of an external decoupling capacitor to the peak detector circuit.
2	RX DATA +	Received data input from isolating transformer. A '1' on this pin represents a positive going HDB3 pulse.
3	RX DATA-	Received data input from isolating transformer. A '1' on this pin represents a negative going HDB3 pulse.
4, 5, 6	LC TANK BIAS	L and C components are connected to form a circuit which is tuned to optimise the extraction of the HDB3 signal.
7	RX GROUND	Ground pin for receiving circuitry.
8	RX CLOCK	Output for clock extracted from received data stream.
9	RX Vcc	Positive supply pin for receive circuitry.
10	RX DATA- O/P	TTL compatible output for -ve pulses extracted from the transmission line.
11	RX DATA + O/P	TTL compatible output for +ve pulses extracted from the transmission line.
12	TX DATA- I/P	Data input for transmission as negative going pulses.
13	TX DATA- O/P	Data output to isolating transformer for -ve pulses.
14	TX GROUND	Ground pin for transmit circuitry.
15	TX DATA + O/P	Data output to isolating transformer for +ve pulses.
16	TX CLOCK I/P	Synchronising clock input for transmit circuitry.
17	TX DATA + I/P	Data input for transmission as positive going pulses.
18	TX Vcc	Positive supply pin for transmit circuitry.

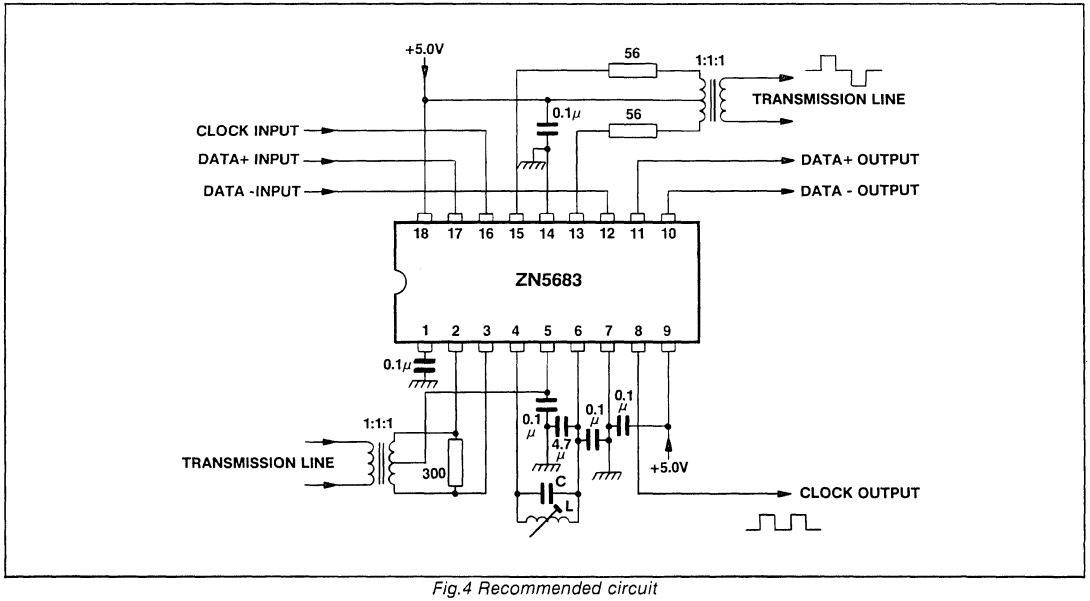


Fig.4 Recommended circuit

Application Notes

A Single Channel Codec

INTRODUCTION

Conventional techniques for pulse code modulation (pcm) conversion for use in completely digital switching systems employ ladder networks requiring many high precision components to define the quantiser characteristic to sufficient accuracy. Alternative techniques employ linear ramps requiring either excessively high clock speeds or a number of ramps of precisely relative slopes.

In order to meet the signal-to-noise and gain-linearity constraints usually imposed on such systems, particularly for the telecommunications market, the use of expensive analogue to digital and digital to analogue hybrid circuitry is necessary. Due to the very high cost of the A/D and D/A component, multi-channel multiplexing techniques are usually employed.

The system described herein uses an advanced approach to a pcm codec (coder/decoder) designed at the British Telecom Research Centre at Martlesham Heath. The original aim was to produce an inexpensive codec capable of fully meeting the relevant C.C.I.T.T. recommendations. It was realised that the way to achieve this was to make optimum use of high performance bipolar LSI technology. The result is a single channel codec of the type outlined in Fig.1. The codec chip is the Plessey ZNPCM1, the performance of which completely meets the performance specification defined by British Telecom. The operation and realisation of the single channel codec is described in the following pages.

SYSTEM CONSIDERATIONS

The approach adopted was based on the principle of conversion to and from pcm via an intermediate digital code format, i.e. the encoder may consist of a waveform tracking encoder to provide highly oversampled A/D conversion followed by digital processing logic to convert the intermediate code to pcm. The decoder may consist of digital processing logic to convert pcm to some intermediate code format and a simple D/A to convert from the intermediate code to analogue. Studies revealed that a trade-off was necessary between analog A/D and D/A simplicity and conversion logic speed and complexity.

The trade-off was taken to its limit resulting in the simplest form of A/D and D/A converters possible providing that circuitry was realisable with state-of-the-art LSI technology. Fig.1 shows a block schematic of the basic codec.

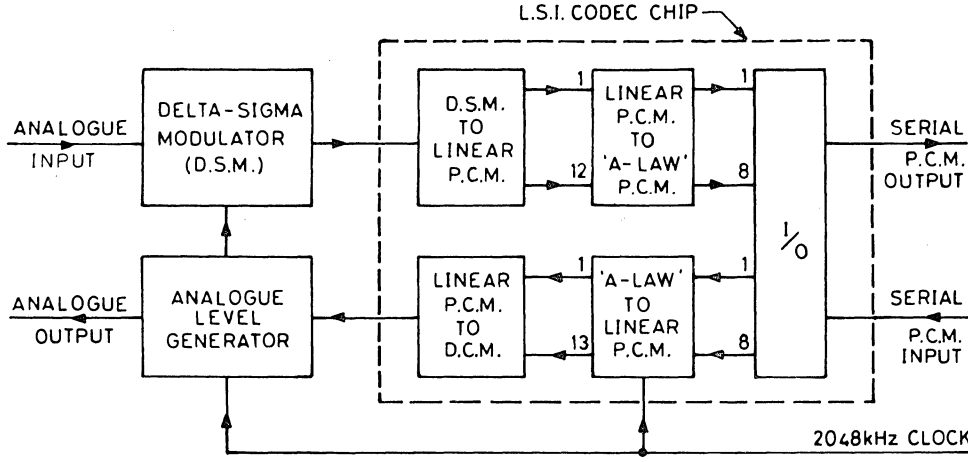


Fig. 1. Codec Schematic

The intermediate code format chosen for both encoder and decoder is that produced by a delta sigma modulator (dsm). It is especially simple to convert from this format back to analogue as one only has to pass the digital stream through a low pass filter cutting off just baove the highest signal frequency to be recovered (3.4kHz).

The area enclosed by the dotted line indicates the functions integrated into the L.S.I. codec chip ZNPCM1. The dsm circuitry is realised using discrete TTL logic, a differential amplifier, resistors and capacitors. However an integrated circuit version of the dsm circuit is now available from Plessey.

THE DELTA SIGMA MODULATOR (DSM)

A modified form of delta sigma modulator/demodulator is used, resulting in an adequate performance using a clock rate as low as 2.048 kHz. Fig. 2 shows the functional circuit of the dsm, incorporating an operational amplifier integrator, and a D-type bistable for the threshold detector and approximation level generator. The modulator accepts a band-limited analogue input signal (300-3400 Hz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The demodulator produces one of two precisely defined analogue levels in response to the single bit/sample delta sigma bit stream.

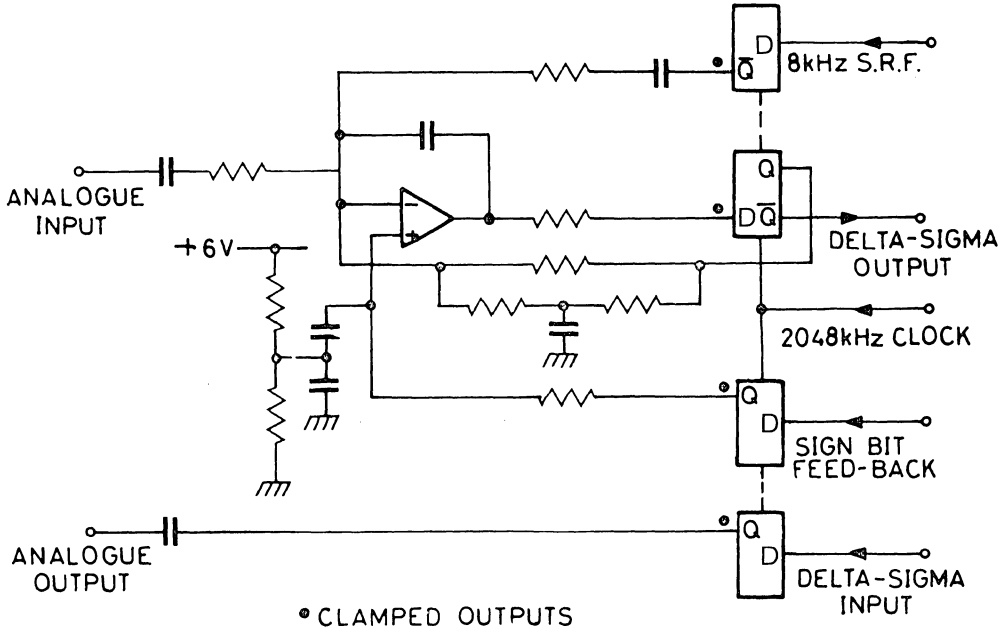


Fig. 2. Modulator/Demodulator Circuit

The modulator circuit relies on the use of two logic signals being fed back from the code converter; the sign bit of the generated pcm codewords, used to control the d.c. alignment conditions, and an 8 kHz square wave (Spectral Redistribution Function) which is added to the input signal to improve performance. A complex feedback network is also used to feed back a higher level of quantisation noise below approximately 16 kHz to shift quantisation noise to higher frequencies where the code converter provides greater suppression. In the reverse direction the decoder delta sigma stream coming from the code converter is passed through a D-type bistable for edge re-timing and level definition before the required analogue signal is recovered by low-pass filtering.

Encoder and decoder gain errors due to initial component variations from their nominal values are corrected at a gain adjustment point in the system. The main requirement is on gain stability, rather than absolute gain. The gain is a factor of both resistor ratios and the D-type output voltages. The output voltages are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the codec, and clamping the high state output voltages to a 2.45V reference by the use of schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, together with a small modulator/demodulator physical size, by implementing the resistors and small capacitors as an in-line passive hybrid.

The modulator also includes a 'fast start' circuit to ensure rapid stabilisation of the d.c. conditions when the codec is powered-up. This is important when the codec is used in switching applications where considerable power savings arise if the codec is only powered-up when required.

The detail circuit of the dsm is shown in Fig. 3. In addition to the basic modulator and demodulator circuit the decoded output is shown being fed into a simple second order Sallen and Key filter. This is shown as a technique for demonstrating the equalisation of sin.x/x distortion resulting from the sample and hold process of the decode function. The compensation would normally be provided as an integral part of the decoder band limiting filter.

An integrated circuit version of the dsm circuit is now available and is designated ZNPCM2. Fig. 4 shows a diagram of the interface connection with the ZNPCM1.

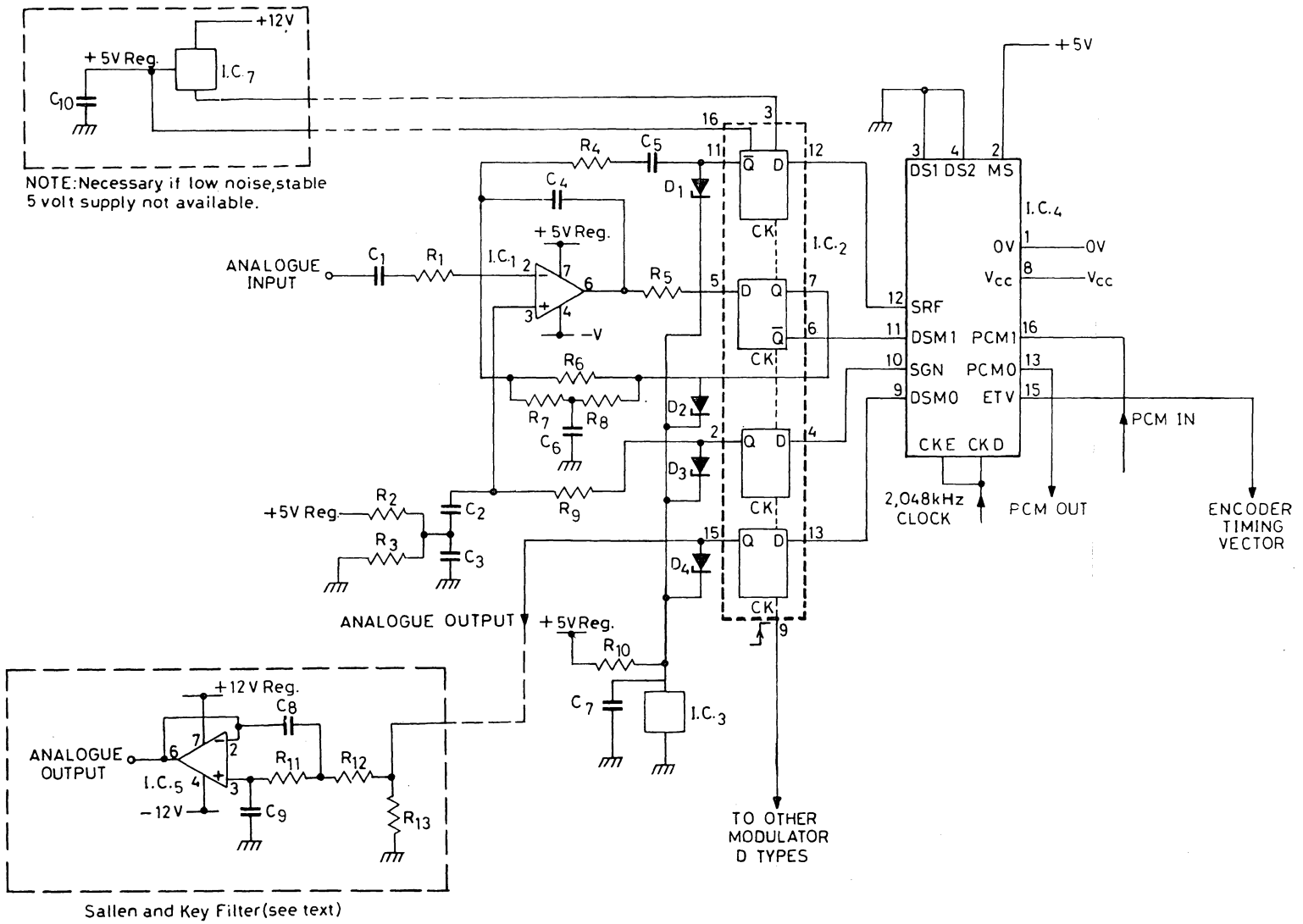


Fig. 3. Discrete Delta Sigma Modulation Circuit

COMPONENTS LISTING FOR COMPLETE CODEC CIRCUIT

1. MAIN CIRCUIT

Integrated Circuits

I.C.1	—	CA3140
I.C.2	—	SN74175
I.C.3	—	ZN458
I.C.4	—	ZNPCM1

Diodes

D1, D2, D3 and D4	—	ZC2800 or 1N6263

Capacitors

C1	—	3.3 μF ±20%
C2 & C3	—	6.8 μF ±20% (6.3V)
C4	—	68 pF ±20% } +15%, –18% (See Note 1)
C5	—	15 nF ±10% } +15%, –18% (See Note 1)
C6	—	10 nF ±2% } +15%, –18% (See Note 1)
C7	—	6.8 μF ±20% (6.3V)

Resistors

R1	—	2.7kΩ ±2% (High Stability Resistor)
R2	—	10kΩ ±2%
R3	—	4.7kΩ ±2%
R4	—	47kΩ ±2%
R5	—	620Ω ±5%
R6	—	10kΩ ±2% (High Stability Resistor)
R7 and R8	—	2kΩ ±2% (High Stability Resistor)
R9	—	2.7kΩ ±10%
R10	—	260Ω ±10%

NOTE 1. Limits apply over temperature range and equipment working life.

NOTE 2. High stability resistors should track each other to ±1% to meet British Post Office Specification Requirements.

2. SUBSIDIARY CIRCUITS

Integrated Circuits

I.C.5	—	**741 Type Op Amp**
I.C.7	—	LM78LO5ACH

Capacitors

C8	—	1 nF ±2%
C9	—	10 nF ±2%
C10	—	2.2 μF ±20%

Resistors

R11 & R12	—	91.8kΩ ±1%
R13	—	100kΩ ±5%

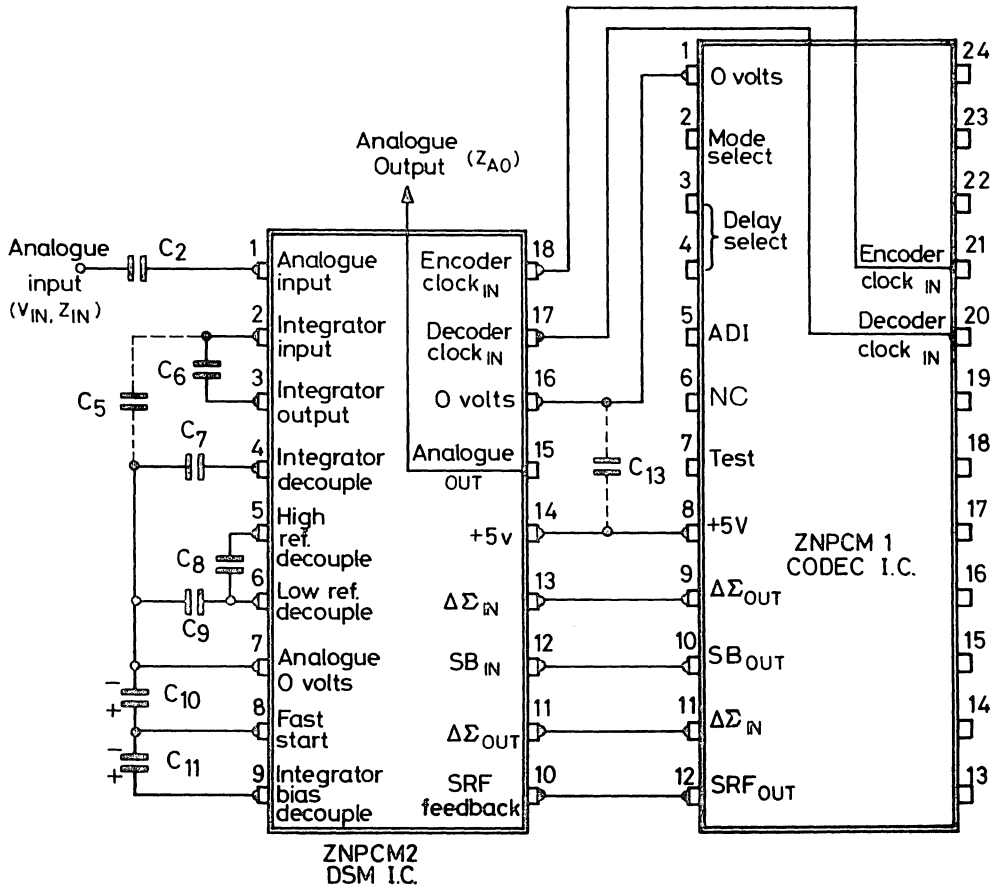


Fig. 4. DSM-Codec Interface

THE CODE CONVERSION

The dsm signal is fed into the integrated circuit at 2,048 kbits/second and converted to compressed pcm at a bit rate of 64 kbits/s or, by the application of external timing signals a maximum of 2,048 kbits/s for multiplexing in a burst format. Conversely the I.C. will accept at the pcm interface either a 64 kbit/s stream or, by the application of external timing signals, a bit rate of up to 2,048 kbit/s in a burst format. This is then converted to a delta sigma pulse stream of 2,048 kbit/s. The actual code conversion can be broken down into two stages; (i) Delta Sigma to linear pcm and vice-versa; (ii) Linear pcm to compressed pcm and vice-versa.

(i) *Delta sigma to Linear pcm*

The converter operates by multiplying the 256 delta sigma input samples occurring in each 125 microsecond pcm sample period by coefficients according to a triangular profile and accumulating the products to form the required linear pcm codeword at the end of the interval. Fig. 5 shows the converter logic structure.

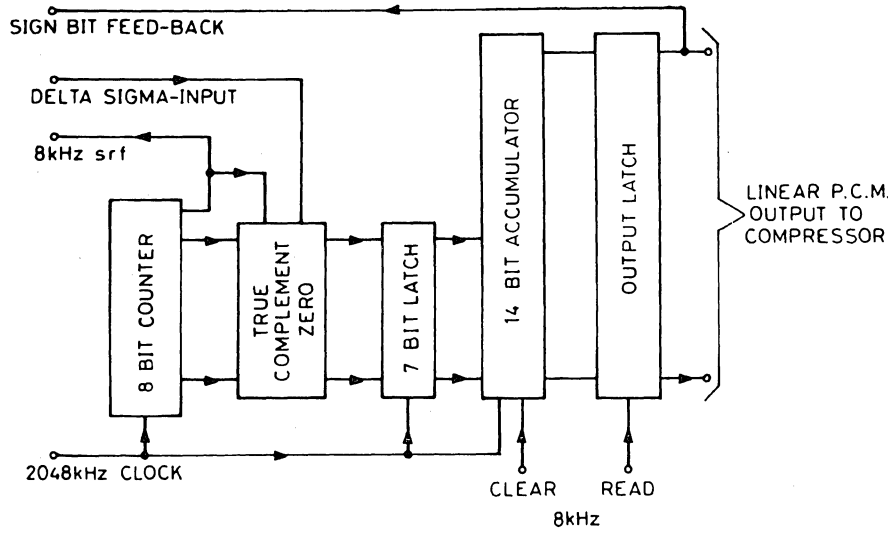


Fig. 5. Delta sigma to Linear pcm Converter

It consists of an eight bit counter, logic for operating on the seven least significant bits of the counter, a re-timing buffer, a 14 bit accumulator and an output latch. The first seven bits of the counter generate numbers zero to 127 as shown in Fig. 6(a). The eighth bit divides the generated number sawtooth into odd and even phases as shown in Fig. 6(b). Bit eight is also used in conjunction with the delta sigma ($\Delta\Sigma_i$) output to operate on the seven bit count sequence to produce the correct value of $\Delta\Sigma_i W_i$ to be added into the accumulator, where W_i is the required weight from the triangular profile during the ith clock period.

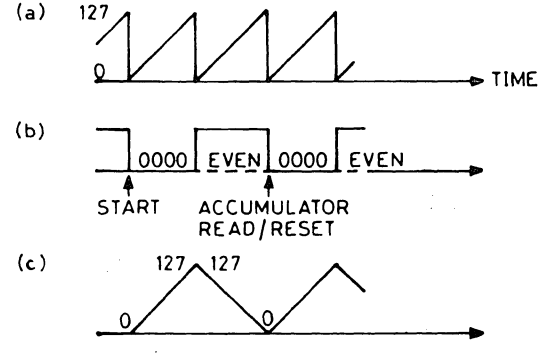


Fig. 6. a) 7 Bit Counter Number Sawtooth
b) Counter Most Significant Bit
c) Effective Available Weight Sequence

The technique of generating a triangular co-efficient profile allows a continuous up-counter to be used, which in turn allows the easy generation of the required timing waveforms to drive different parts of the codec. The 8 kHz square wave used within the modulator is taken from the most significant bit of the counter and the sign bit feedback to the modulator is derived from the output latch.

The converter produces 14 bit linear pcm codewords at 8k samples/s with an effective accuracy such that the signal to noise ratio obtained, after converting the 'A' law pcm, complies with C.C.I.T.T. recommendations.

In the decode direction the principle of conversion is the implementation of the delta sigma algorithm (see appendix 1) in all digital logic. The linear pcm input appears as a sample and held signal, the digital dsm performing a continuous conversion to the delta sigma format. The realisation of the circuitry is shown in Fig. 11.

(ii) *Linear PCM to Compressed PCM*

A useful relationship exists between linear pcm codewords and their 'A law' compressed equivalents allowing conversion between the two formats to be readily accomplished using data selection techniques. Fig. 7 shows a linear pcm to 'A law' pcm converter where the segment code is derived directly from the linear codeword using combinational logic. The segment code is then used to control a data selection matrix to extract the required interval code.

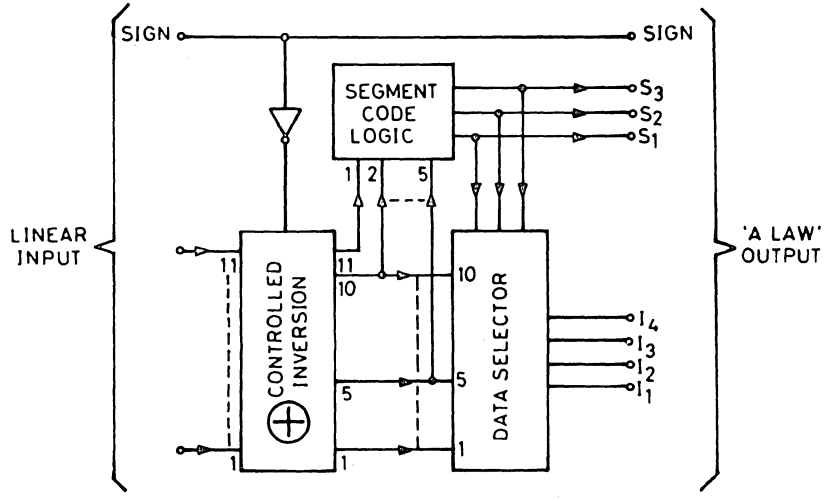


Fig. 7. Linear to 'A Law' Converter

Facilities are provided for controlled alternate digit inversion of the 'A law codewords prior to parallel to serial conversion for serial output. In most applications ADI must be provided but for testing purposes it is useful if it can be removed.

Similar techniques are used in the decode direction to convert the compressed pcm into linear pcm.

INPUT-OUTPUT INTERFACE

One of the most important features of a pcm codec is the structure of its input-output interface as this directly influences the ease with which the codec can be used in a given application. A very flexible I/O interface has been included which can operate in either of two modes by means of pin selection.

In the first mode the pcm codewords are clocked in and out automatically at 64 kbits using clocks internally derived from the applied 2,048 kHz clock. The only timing waveform required is a timing vector to indicate when the first bit (the sign bit) of each codeword is required (which automatically defines the positions of the other bits at this rate). To take account of many applications where the received pcm codewords are not in the frame alignment with the transmitted codewords, two pins are provided for the user to strap appropriately to indicate the actual displacement. The four possibilities allow for zero to three digits delay of the received with respect to the transmitted codewords.

In the second mode, a much wider range of operation is possible. The pcm codewords may be clocked in and out at any rate in the range 64 to 2,048 kbits. Access is provided to the output and input shift registers to allow the multiplexing and demultiplexing of signalling bits if required. Also separate encoder and decoder 2,048 kHz clock inputs are provided to allow asynchronous working between the two directions of transmission, which is typical of pcm multiplex applications.

ZNPCM1 – THE L.S.I. CODEC

From its initial conception the codec has been designed with a view to producing the circuit in an L.S.I. semiconductor technology. Using advanced circuit design, photographic mask making and processing techniques developed originally for the F100L 16 bit bipolar microprocessor[2] Plessey have produced a single chip codec incorporating all the circuit functions shown in the dotted rectangle in Fig.1. The device operates from a single 5V supply with a maximum operating frequency of 6MHz and all inputs and outputs are TTL compatible. For reduced power requirements the device will operate down to 3.5V maintaining TTL compatibility and as low as 3V with some degradation of input/output voltage levels.

The chip size is 178 thou. by 163 thou. and is available in a 24 lead ceramic DIL (ZNPCM1J).

Performance

The codec described meets all the performance requirements of the C.C.I.T.T. Recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

1. Idle channel noise: –69 dBmOp

   (C.C.I.T.T. recommendation = –65 dBmOp)

2. Signal-to-noise ratio and Gain-level linearity: Figs. 8(a) and 8(b) show the results using a 450-550 kHz pseudo-random noise test.

3. Intermodulation distortion:

   Measured products are at least 10 dB and on average 18 dB better than the C.C.I.T.T. recommendations.

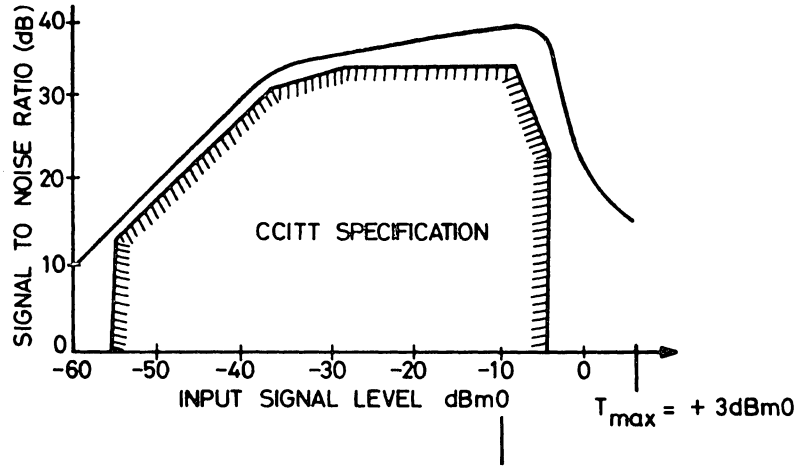


Fig. 8(a). Signal to Noise Ratio, 'A law'

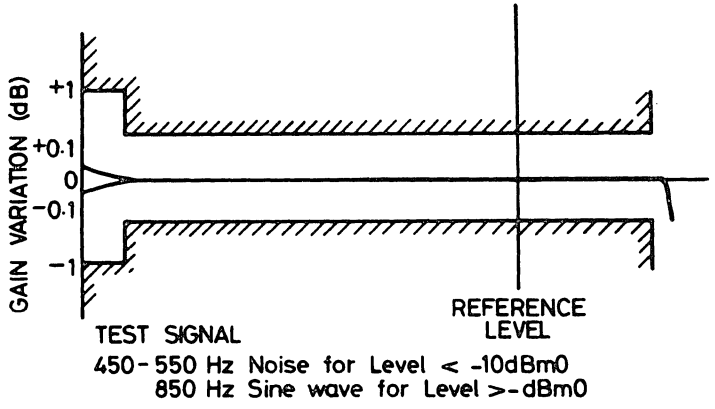


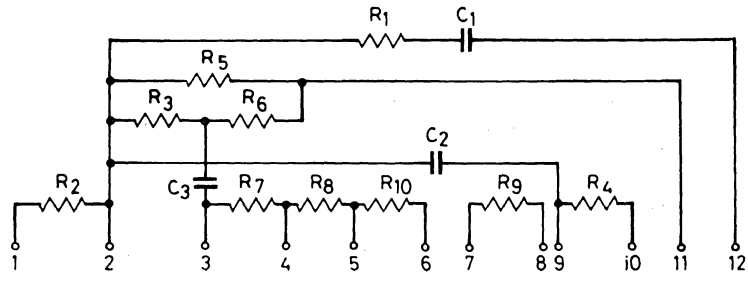
Fig. 8(b). Gain to Signal Level, 'A law'

Another aspect of the codec performance is the Sinc (π ft) decoder frequency characteristic, having infinite attenuation at 8 kHz and multiples thereof, introduced by the digital full-width sample and hold process occurring within the code converter. Although this requires equalisation in-band with an appropriate analogue post filter design, the characteristic ensures complete suppression of the sampling frequency components and harmonics, independent of any d.c. offset in the received codewords.

The sinc (π ft) characteristic is also useful when considering the design of less complex analogue filters to be used with the codec in digital switching applications, where codecs may be provided on a per customers line basis. A less complex filter may be allowable since, in the local telephone networks, there is not the problem of interworking with frequency division multiphase systems.

APPENDIX 1

DSM Hybrid



Component Values

R1	47kΩ	±5%	R4	620Ω	±20%
R2	2.7kΩ		R9	2.7MΩ	
R3	2kΩ		R10	260Ω	
R5	10kΩ				
R6	2kΩ				
R7	4.3kΩ				
R8	10kΩ				
C1	15 nF	+15%, −18%			
C2	68 pF				
C3	10 nF				

Resistor Ratio Tolerances

If, $R_p = \dfrac{(R_3 + R_6)\, R_5}{(R_3 + R_6 + R_5)}$

then R_p/R_2 shall commence with ±5% of the nominal ratio and then remain with ±1% of the starting ratio over operating temperature range and equipment life.

The ratios R_p/R_1 and $R_7/R_7 + R_8$ will remain within ±5% of nominal ratios.

The tolerances quoted are those required over the temperature range and working life to obtain a performance compatible with that required by the British Post Office and may be relaxed for less stringent requirements.

APPENDIX 2

Fig. 9 shows the algebraic notation used for the numbers existing within the modulator during the nth clock cycle.

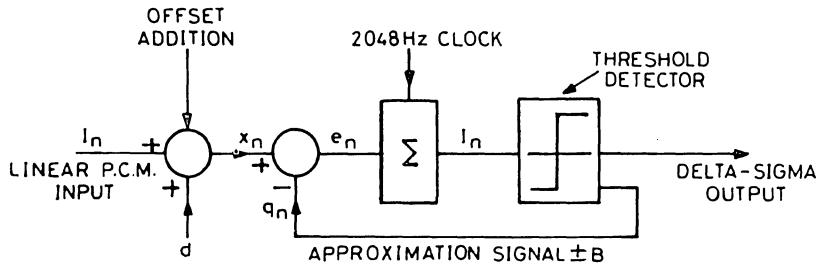


Fig. 9. The Digital DSM

The 13 bit linear pcm input I_n has a constant offset d added to it, resulting in a number $x_n = I_n + d$ being presented to the digital dsm. The offset d, equal to 1/16th of the peak pcm codeword magnitude, acts as a spectral redistribution function[3] which improves the performances considerably. The approximation signal q used in the feedback loop can take one of two binary numbers +B or −B. The difference $e_n = x_n - q_n$ is presented to a digital integrator. At the end of clock period 'n', e_n is added to I_n, the integral or sum of all previous differences to form $I_n + 1$.

$$\text{i.e., } I_n + 1 = I_n + e_n = \sum_{o}^{n} (x_i - q_i)$$

The threshold detector outputs the sign of $I_n + 1$ which is used to control the sign of the approximation signal during the $(n + 1)$th period the sign being chosen so as to minimise the integral,

i.e., $q_n + 1$ B sgn $(I_n + 1)$

over a period of m dsm cycles

$$I_n = I_n - m + \sum_{n-m}^{m-1} (x_i - q_i)$$

Rearranging and dividing by m:

$$\frac{1}{m}\sum_{n-m}^{n-1} q_i = \frac{1}{m}\sum_{n-m}^{n-1} x_i \quad \frac{1}{m}(I_n - I_{(n\ m)})$$

i.e., the mean value of q over m cycles is equal to the mean value of the input x plus some error term. The larger the value of m the smaller the error term becomes. Viewed in the frequency domain the feedback loop causes the low frequency components of q to track the baseband frequency components of the input x, any difference being the inband quantisation noise due to the transformation or coding process.

Fig. 10 shows the circuit realisation of the digital dsm. The simplicity of the configuration arises from choosing the magnitude of the approximation levels $\pm B$, such that the difference between x_n and q_n can be formed by combinational logic techniques on the most significant bits of x_n and q_n without performing a full subtraction operation. Generalising, if x is represented by a two's complement number k bits in length, then,

$$-2^{k-1} \leqslant x \leqslant 2^{k-1} - 1$$

The two possible values of q are made

$$+B = 2^{k-1} \text{ and } -B = -2^{k-1}$$

As a consequence the k + 1 bit value of e can be formed by using the k – 1 least significant bits of x (unchanged) combined with two bits in the most significant positions which are inverses of the sign bits of x and q, hence the logic structure shown in Fig. 10. The digital dsm cycle rate is governed by the rate at which the accumulator latch is clocked, the delta sigma output being taken from the sign bit of the accumulator.

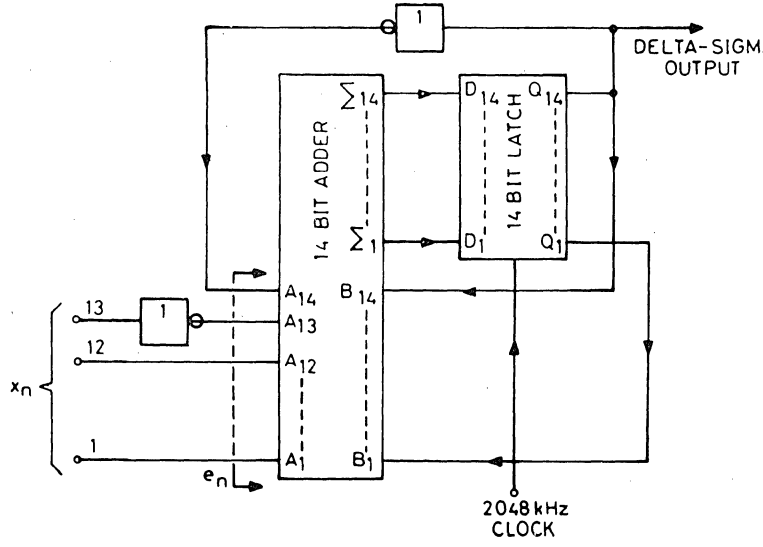


Fig. 10. Digital DSM Circuit Realisation

References

1. C.C.I.T.T. Orange Book Vol. III – 2 Rec. G711, 712.

2. F100L circuit, Design and Manufacture by Mr. D. Grundy – Electronic Equipment News, May 1978.

3. Everard, J.D. 'Single Channel PCM Codec' IEE Journal –Solid State CCTS Vol. COM 27 No. 2. Feb. 1979 par. 1 pp 25-38.

An HDB3-Coded PCM Link

This application note shows how the MV1441, MJ1444 and MJ1445 can be used in a 2048kbit/s, HDB3-coded PCM link. It describes the structure of the link, gives an application circuit using the devices and indicates how the circuit can be expanded to include the MV3506 series Codecs.

The 2048kbit/s link is that described in CCITT recommendations G.703 and G.732. It is a digital trunk capable of carrying 30 speech channels plus associated signalling and synchronisation. The same link is used as the primary access for ISDN.

STRUCTURE OF THE 2048kBIT/s PCM LINK

The serial structure of the 2048kbit/s PCM link is shown in Fig.1. There are 8 bits in each Time Slot, 32 Time Slots in each Frame and 16 Frames in each Multiframe.

The serial data stream used on the line is HDB3 encoded. This ensures that the clock can be recovered and bit synchronisation established. Frame synchronisation is achieved by Time Slot 0 which contains an alternating signal on bit 2. To avoid accidental synchronisation, a frame synchronisation pattern is used on bits 3 to 8 when bit 2 is zero (see Table 1).

If multiframe synchronisation is required, it is established by four 0's in Time Slot 16 once every 16 Frames (see Fig.3). On the other 15 Frames, Time Slot 16 is used for signalling which avoids four 0's.

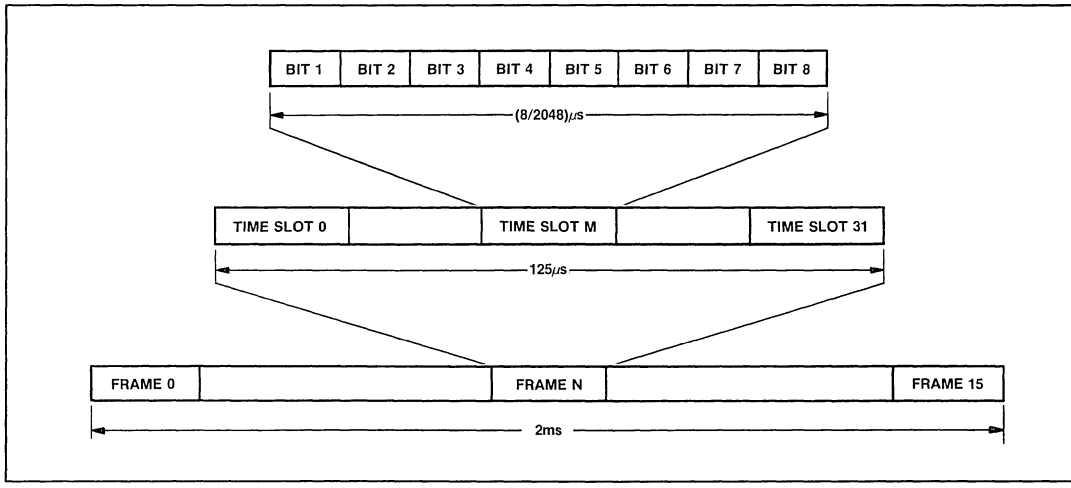


Fig.1 Serial format

	Bit Number							
	1	2	3	4	5	6	7	8
Time Slot 0 in Frame-Alignment Frames	Reserved for International use	0	0	1	1	0	1	1
Time Slot 0 in Non-Frame-Alignment Frames	Reserved for International use	1	Alarm indication to remote multiplexer	Reserved for National use				

Table 1 Bits in Time Slot 0

Frame 0 - Time Slot 16		Frame 1 - Time Slot 16			Frame 15 - Time Slot 16	
0000	XYXX	ABCD for Time Slot 1	ABCD for Time Slot 17		ABCD for Time Slot 15	ABCD for Time Slot 31

Table 2 Bits in Time Slot 16

THE 2048kBIT/s INTERFACE CIRCUIT

Fig.2 shows the interface circuit which is constructed from an MV1441, an MJ1444, and MJ1445 and discrete components at the line interface. The circuit can be used at either the master or the slave end of a phase-locked transmission link or with asynchronous directions of transmission.

Transmit Path

Signalling information for Time Slot 0 is sampled by the MJ1444 and output for multiplexing with PCM data to form the Transmit Data (TD) stream. The MV1441 samples the Transmit Data and outputs HDB3 steering pulses. The line transmit interface accepts the steering pulses, shapes them and couples them through the transmit transformer to generate the differential HDB3 line signal.

Bit and frame synchronisation are established by the Transmit Clock (TC) and Transmit Sync (TS) signals (see Fig.3). **NB** The Transmit Sync does not need to be generated every frame. The Transmit Clock drives the Clock input (pin 4) of the MJ1444 and the Encoder Clock input (pin 2) of the MV1441. The Transmit Sync drives the Channel Reset input (pin 3) of the MJ1444.

Some care is required with the transmit transformer. The 5V connection to it must form a good AC ground and capacitive decoupling may be needed to ensure this. Transformer construction details are given in Table 3.

Receive Path

The differential line signal is sensed by the line receive interface which generates steering input pulses for the MV1441. These pulses are used by the MV1441 to generate the Receive Clock (RC) and are decoded according to the HDB3 rules to give the Receive Data (RD). The MV1445 recognises the frame synchronisation signal on Time Slot 0 of the Received Data and outputs the signalling information.

The MJ1445 also outputs the Receive Sync (RS) signal which bears a similar relationship to Receive Clock and Receive Data as on the Transmit Path (see Figs.3 and 4). **NB** The MJ1445 only outputs the RS signal on Frame-Alignment Frames.

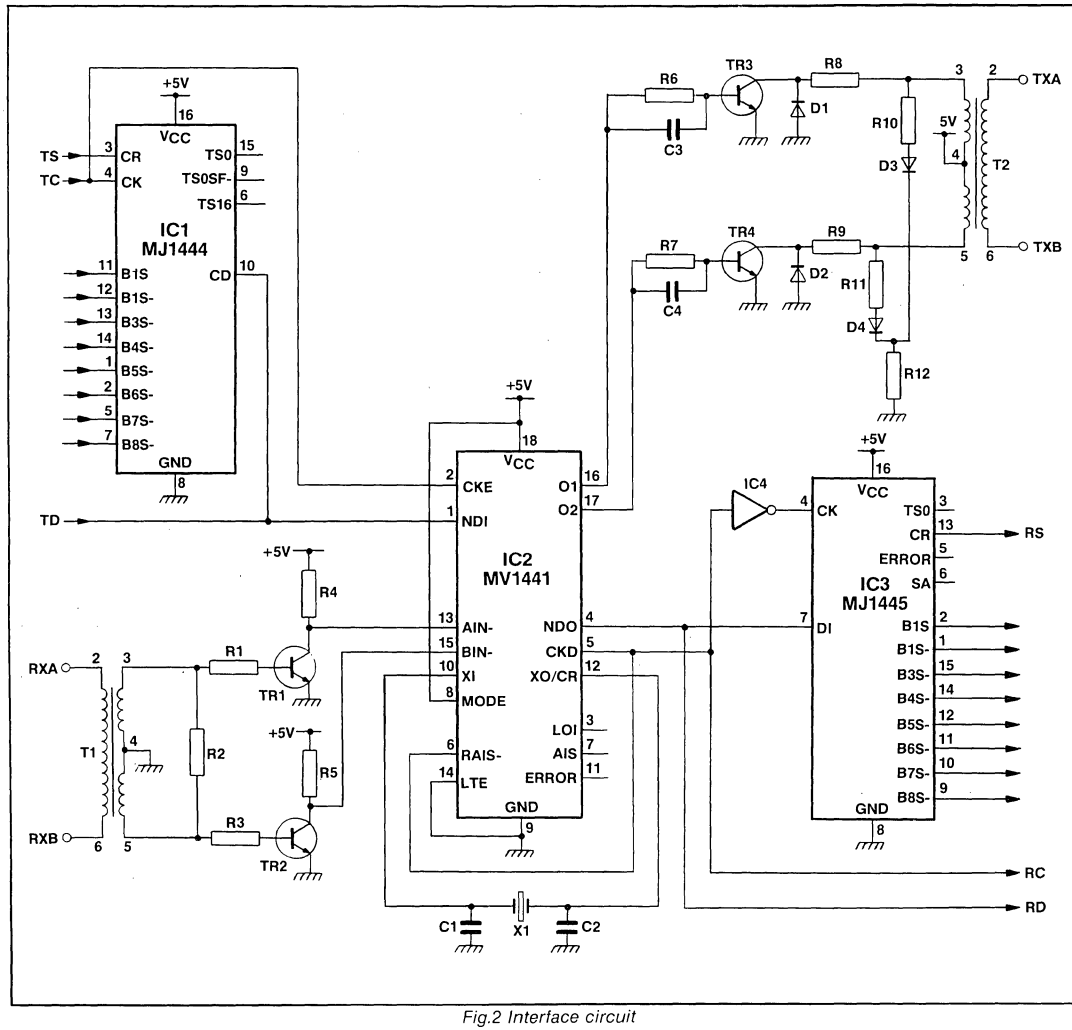


Fig.2 Interface circuit

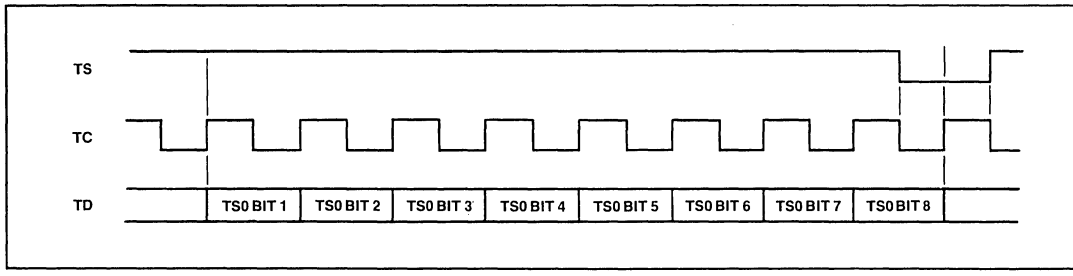


Fig.3 Transmit signal alignment

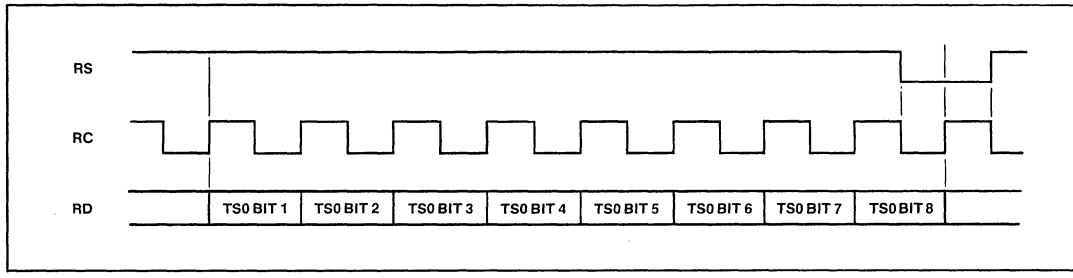


Fig.4 Receive signal alignment (RS shown for Frame-Alignment Frames)

Resistors
R1 -680Ω
R2 -390Ω
R3 -680Ω
R4 -1kΩ
R5 -1kΩ
R6 -1kΩ
R7 -1kΩ
R8 -68Ω
R9 -68Ω
R10-120Ω
R11-120Ω
R12-680Ω

Capacitors
C1 - 22pF
C2 - 22pF
C3 - 220pF
C4 - 220pF

Transistors
TR1-4 - 2N2369A

Diodes
D1-4 - BAW62

Crystal
X1 - 16MHz

Integrated Circuits
IC1 - MJ1444
IC2 - MV1441
IC3 - MJ1445
IC4 - CMOS inverter

Transformer Components
T1 and T2 (each):
1-off RM5 Ferrite pot core, e.g:
Siemens Type B65805-C0000-R030,
B65806-B2001-X000
or B65806-B1001-D001
2 off Clamp
1 off Bobbin
For winding details, see text below.

Table 3 Interface circuit list

Transformer Winding Instructions

1. 40 SWG wire: Start at pin 2
   Wind 36 turns
   End at pin 6
2. Insulating Tape : Wind 1 turn
3. Screen : Connect to pin 1
4. Insulating Tape : Wind 1 turn
5. 40 SWG wire: Start at pin 3
   Wind 36 turns
   Tap to pin 4
6. Insulating Tape : Wind 1 turn
7. 40 SWG wire: Continue from pin 4
   Wind 36 turns
   End at pin 5

EXPANDING THE CIRCUIT

Figs.5 and 6 show how MV3506/7/8 Codecs can be added to the interface circuit. Each Codec receives a transmit and receive strobe which defines its Time Slot. The relationships between the strobes and the signals used by the interface circuit are shown in Fig.7.

The Codecs require their transmit and receive clocks and strobes to be phase-locked with their master clock. Information on this and on the generation of the strobes is contained in the Codec data sheets.

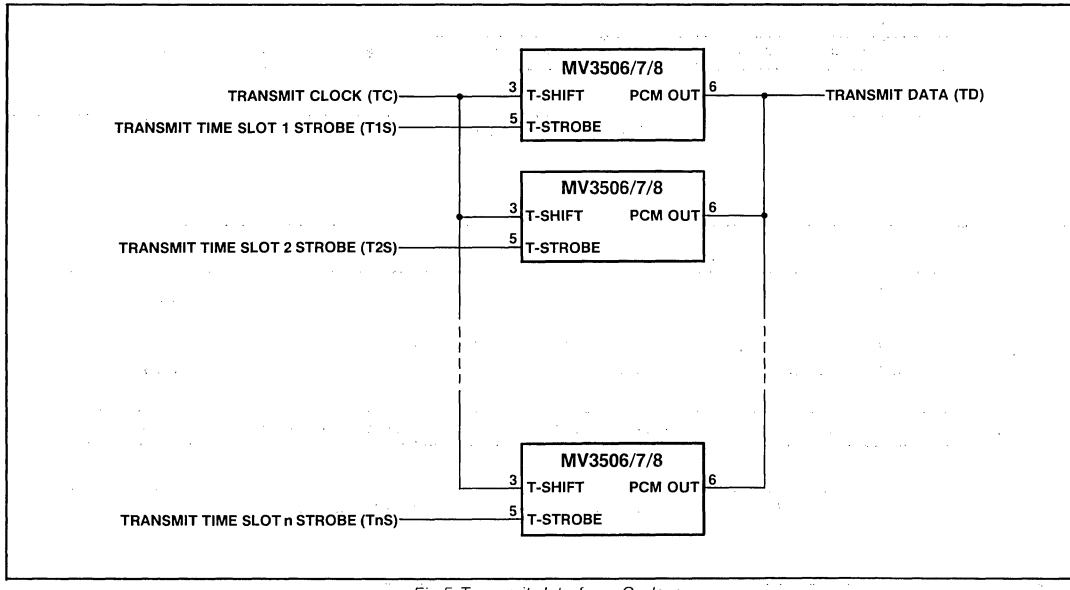


Fig.5 Transmit data from Codecs

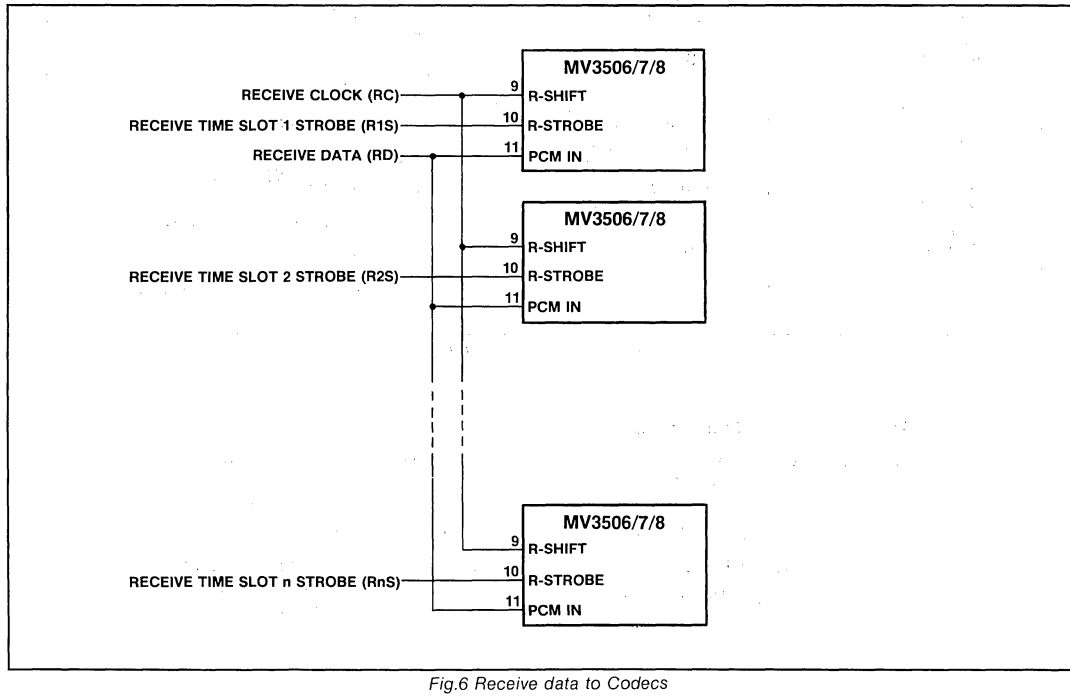


Fig.6 Receive data to Codecs

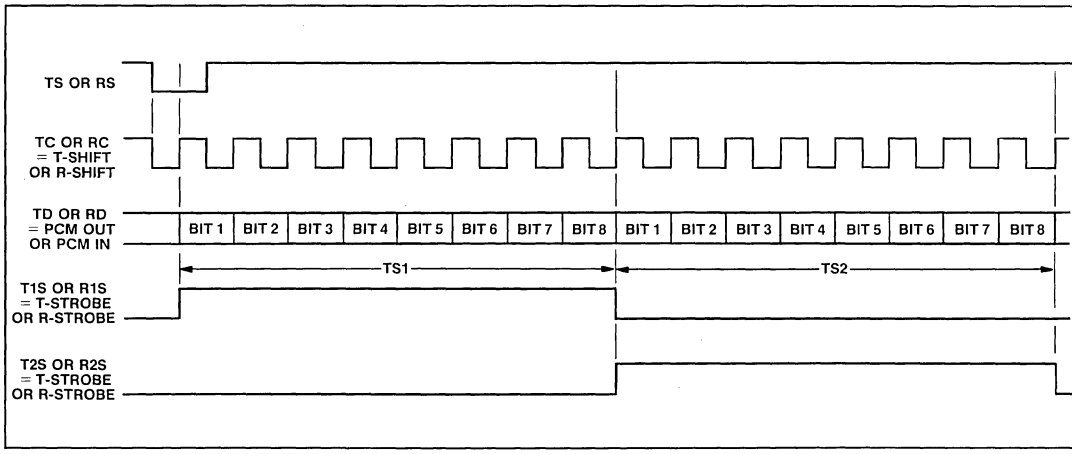


Fig.7 Signal alignment for MV3506/7/8 Codecs

PABX/Line Card Control Circuit

This application note describes how a control circuit and up to 128 Plessey MV3000 Subscriber Line Audio Circuits (SLACs) can be connected together to form a simple PABX.

The two possible modes of operation of the control circuit are described, showing in each case how it is connected to the matrix of SLACs. The controller has been designed to interface to an industry standard microprocessor (such as an Intel 8051), and to allow control data to be written and read via the SLAC's serial control port.

The circuit has been designed to use 74HCT logic throughout and operates from a single 4MHz clock source generating antiphase 2MHz clock signals.

DESIGN CONCEPT

The basis of the PABX/Line Card controller design uses the time-slot switching capabilities of the SLAC (MV3000). Each SLAC can transmit/receive PCM data in 32 (64 in expanded mode of operation) time-slots, which can appear on any of two transmit and two receive ports, A and B. This gives a maximum capacity of 128 time-slots, each associated with one SLAC (i.e., telephone).

Operation of the controller simply allows the serial control information of the SLACs to be generated by a microprocessor. The processor provides all the necessary intelligence to control call routing, off hook status, gain variations etc. in software. Communication with the controller is via the microprocessor interface, designed to suit an industry standard processor, such as the Intel 8051.

CIRCUIT DESCRIPTION (see Fig.1)

Microprocessor Interface

This allows control data to be written to and read from the controller. In addition the Control Address data is written to the device, which is then used to control either up to 8 SLACs directly or one of up to 128 SLACs at an individual address.

Control Data or Control Address is written under the determination of the A0 input. If A0 = 0, then the data byte from the microprocessor is designated as Control Address. This is then loaded into an eight-bit latch on the rising (+ve) edge of the $\overline{WR}$ input. If A0 = 1, then the data byte is designated Control Data. This is loaded into the '299 shift register by a positive edge of the 2M clock during the $\overline{WR}$ = 0 period. (See timing diagram, Fig.2.) It is necessary to ensure that the $\overline{WR}$ pulse is long enough (>500ns) for a 2M rising edge. This limits the 8051 to 10MHz operation. This data will then be sent to the SLACs, as determined by the $\overline{CAM}$ (Mode) input, when the $\overline{WR}$ input returns to a logic 1. Note that control data must not be written again to the controller during the next 8μs in order to avoid corruption of the previous data byte.

In order to read Control Data from a SLAC, the following considerations must be observed. First, note that the SLAC outputs data following a relevant Control Data word in. Each data byte that is to follow is then clocked out of the SLAC's DIO pin during subsequent SLAC $\overline{CS}$ = 0 (active) periods. Due to the I/O structure of the SLAC control interface, the output data of the controller must be all ones(FF_H) at these times. This ensures that the controller does not output data that will corrupt the SLAC output data (open drain output). The microprocessor must therefore write FF_H during the $\overline{CS}$ active periods referred to above.

Secondly, note that only one data byte out will be held by the controller (in the '299) at any one time. This means that the microprocessor must read from the controller after each successive write of FF_H, thus forming an organised sequence. This will ensure that no data is lost. Since it is only possible to read from one SLAC at a time (see also Control Address Outputs), then a suitable operational procedure would be as follows:

(a) Write Control Address
(b) Write Control Data
(c) Write FF_H
(d) Read first Data byte
(e) Write FF_H
(f) Read second Data byte
(g) Repeat FF_H/Read as necessary until all data has been output

When the $\overline{RD}$ input = 0, the '299 I/O pins are configured as outputs and shift register data is available at the μD0 - μD7 pins.

The $\overline{CS}$ input disables the microprocessor interface when this pin is at logic 1. For normal operation as described, this pin should be held at logic 0.

Output Port

This provides the four connections normally associated with the serial control of a single SLAC. That is specifically Control Data Input/Out (CDIO) providing input/output to the SLAC, Control Pin Address ($\overline{CPA}$) providing SLAC $\overline{CS}$ and Control Clock Output providing the DCLK input.

The CDIO and $\overline{CPA}$ pins become active only after a Control Data byte has been written from the microprocessor (i.e., A0 = 1).Following the $\overline{WR}$ → 1 transition, the '169 counter counts down through a controlled sequence. This counter provides the $\overline{CPA}$ output directly, which also instructs the '299 register to shift right, providing a CDO output as shown in the timing diagram, Fig.2.

To obtain acceptance of the CDIO data from the SLAC, it is first retimed to the $\overline{2M}$ clock. CDIO data is then loaded into the '299 register as the CDO data (all ones) is clocked out. When the once off sequence stops, SLAC output data is held in the register ready to be read by the microprocessor (see also Microprocessor Interface).

Control Address Outputs and Mode Input

Control Address data from the microprocessor is held in the '574 latch. The outputs of this device can be used in two ways, depending on the $\overline{CAM}$ input:

If the $\overline{CAM}$ input = 1, then the $\overline{CPA}$ signal will strobe the CA0-7 outputs during the SLAC Control Data load sequence (see Output Port, above). The pins CA0-7 have pull-up resistors to +5V connected, so that those outputs that have a 0 loaded into the latch will go low as $\overline{CPA}$. Thus, if one SLAC $\overline{CS}$ input is connected to each control address output (Fig.3), control data is sent to each of the 8 SLACs that has a $\overline{CS}$ low as previously described. This mode can be used when reading data from the SLACs, only if one of CA0-7 = 0.

Alternatively, if $\overline{CAM}$ = 0, then the '574 outputs are permanently enabled. The 8-bit output byte can now be decoded as an individual SLAC address. This mode can be used to write/read data from a single SLAC only, of which up to 128 in a PABX are permissible.

Note that in both modes, the CDIO and CCO outputs are common to all SLACs.

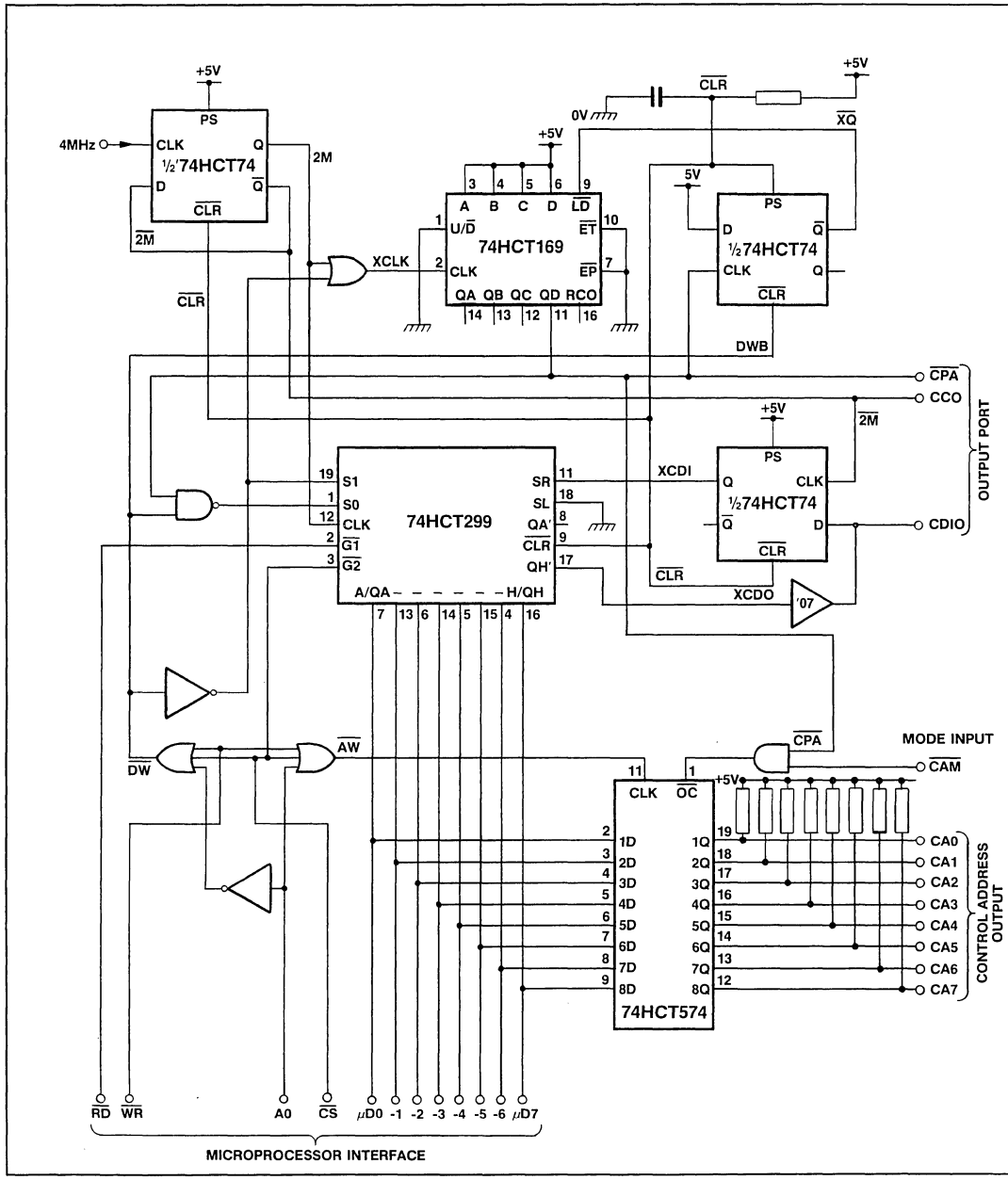


Fig.1 Line card controller logic diagram

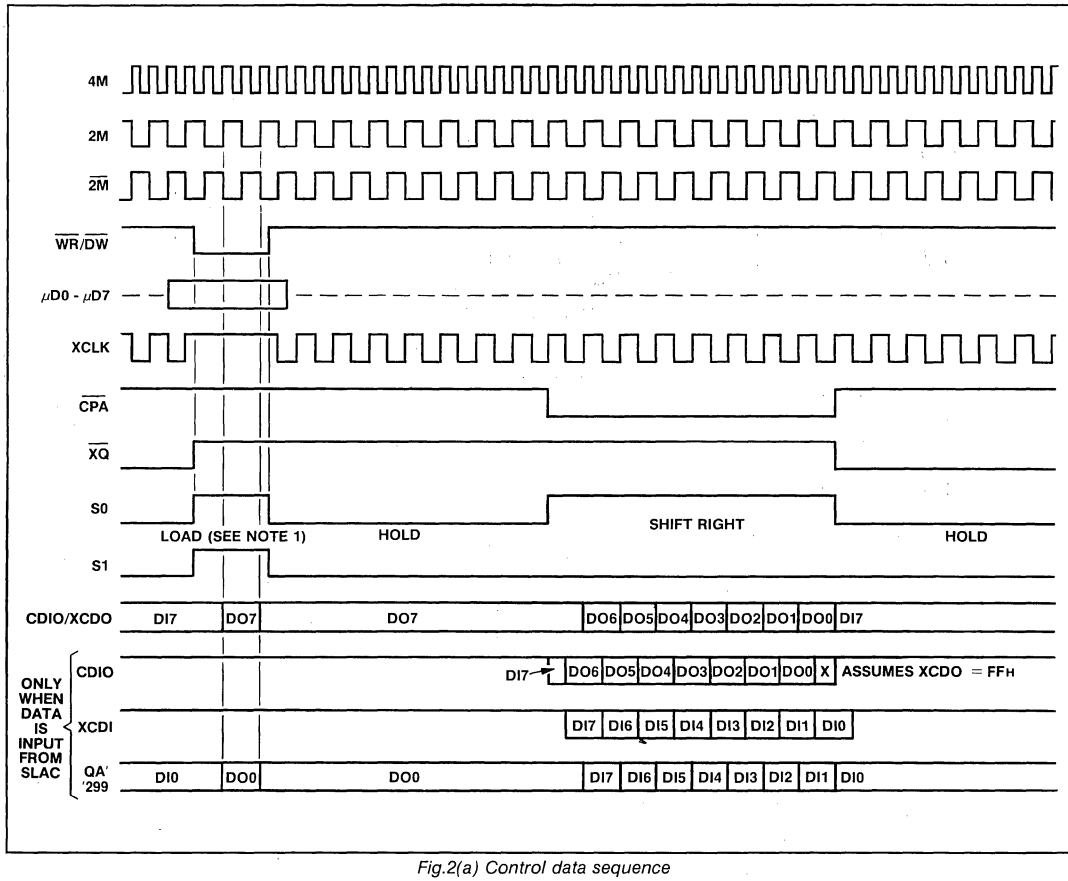


Fig.2(a) Control data sequence

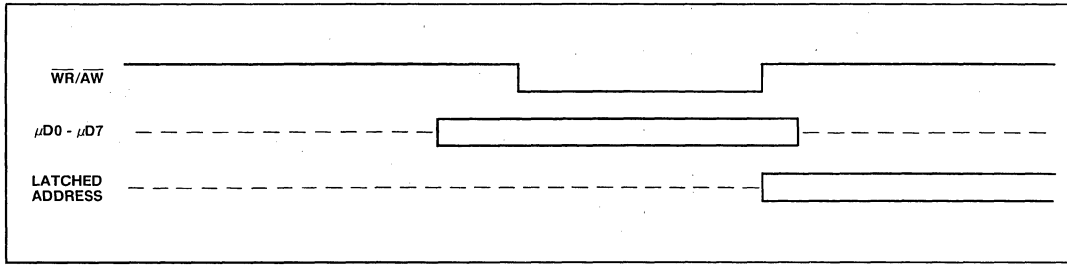


Fig.2(b) Microprocessor write

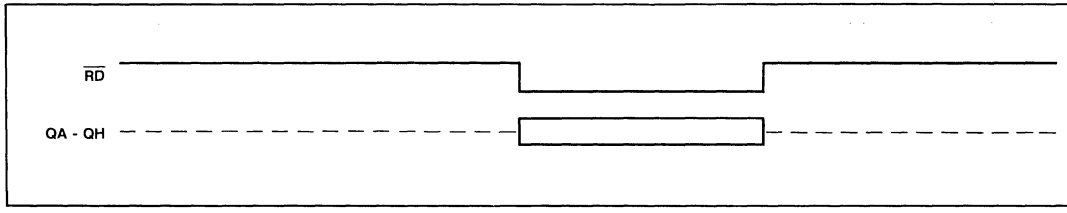


Fig.2(c) Microprocessor read

Fig.2 Timing diagram (NOTE WR low period must be >500ns - see text)

SYSTEMS APPLICATIONS

Line Card Controller

The configuration of controller and SLACs to form a line card is shown in Fig.3. Each $\overline{CS}$ input of a SLAC is driven by one of the CA0-7 outputs. For this application the $\overline{CAM}$ = 1 mode is used.

When initialising, or sending common commands to the SLACs, a Control Address value of 00_H can be written to the '574 latch. When the Control Data is written to control, all 8 SLACs are loaded with this data. If the writing of a Control Data word will cause a SLAC control data output, or a single SLAC is to be written to, the Control Address word must contain only one 0 (such as FE_H, BF_H etc.). This ensures that only one SLAC at a time will output data.

PABX Application

The interconnection of controller and SLACs to form a PABX is shown in Fig.4. In this application, the SLACs are organised in 16 blocks of 8 (a line card), each block selected by a one-of-sixteen decoder (Line Card Address). This decoder (e.g., a 74 series '154 or two '138s) acts on the next four most significant bits of CA7-0, that define the Line Card Address (i.e., CA6-3). Each output of the '154 enables a one-of-eight decoder, associated with each block of 8 SLACs. All sixteen of these 1-of-8 decoders (e.g., '138) act on the three least significant bits of CA7-0, that define a SLAC Address. The $\overline{G3A}$ enable input of each '138 is driven by $\overline{CPA}$, so that the finally decoded output is enabled as CPA. Then, since the $\overline{G2A}$ enable input of each '138 is enabled exclusively by the '154, only one SLAC can have an active $\overline{CS}$ input at any one time. This SLAC is defined by the Line Card Address, CA6-3, and SLAC Address, CA2-0.

Control data to and from each SLAC is achieved on an individual basis. The address of the required SLAC is sent (written) first to the controller (A0 = 0). With A0 = 1 writes/reads via the microprocessor interface are concerned with this SLAC only.

PABX Application with Multiple Control

To speed up operation of control when using 128 SLACs, more than one controller can be used. In this case each controller works in $\overline{CAM}$ = 1 mode controlling 8 SLACs. This then requires a total of 16 controllers.

Improved operation is now obtained by writing Control Address 00_H to all controllers for subsequent loading of Control Data to all 128 SLACs simultaneously. For successful capture of Control Data from the SLACs the Control Address of every controller is now loaded with an address value containing only one 0 (such as DF_H). This ensures only one SLAC sends data to each controller at this time. Each controller can now be read individually (addressed) by the processor. To obtain Control Data from the other SLACs, a different Control Address, containing one 0, is used in the same manner. Control Data can thus be obtained from each SLAC by using all of the 8-possible CA0-7 combinations that contain one 0.

Finally, note that when writing Control Data to a common number of SLACs (not all 128), then using differing combinations of Control Address in each controller can load subsequent data to any number of SLACs in any combination. Similarly, by using different combinations of CA0-7 (with one or no 0) in each controller, then up to 16 SLACs in any combination of one per controller can send Control Data to the respective controller.

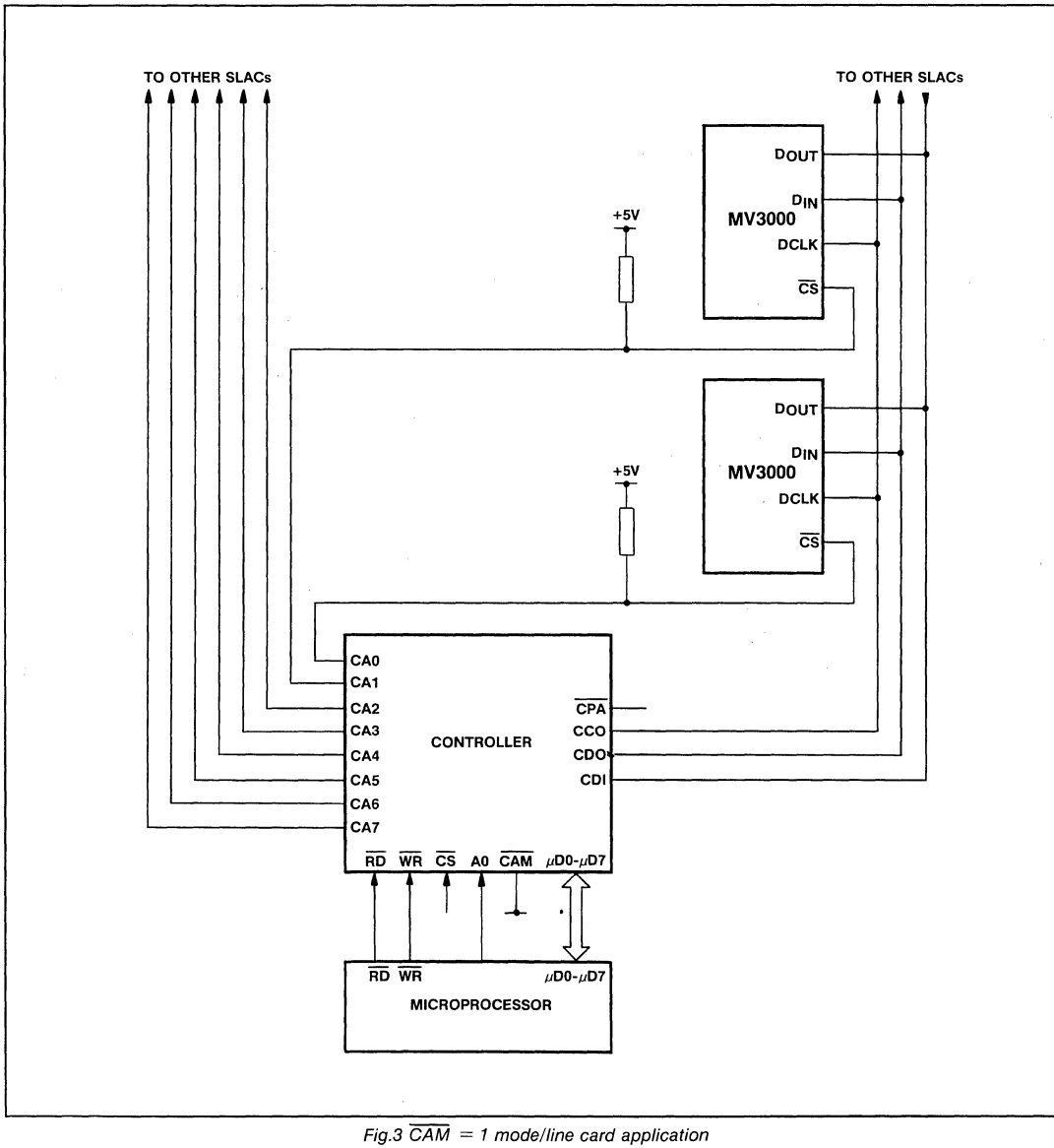


Fig.3 $\overline{CAM}$ = 1 mode/line card application

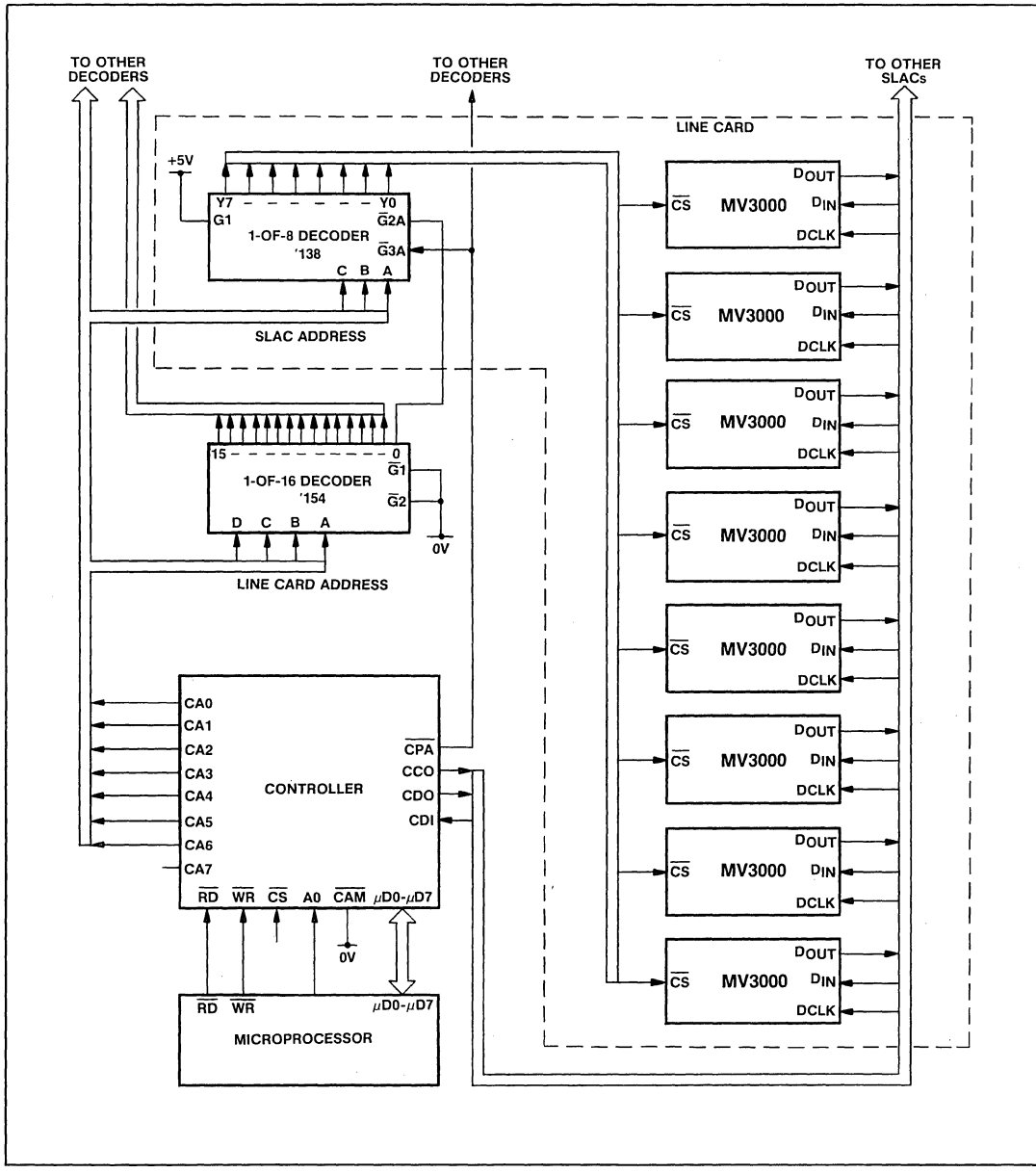


Fig.4 $\overline{CAM}$ = 0 mode/PABX application

MV3000 Evaluation Board and Controller PCB — AN43

This application note describes a printed circuit board that can be used to evaluate all the functions of the Plessey MV3000 Subscriber Line Audio Circuit (SLAC). Also described is a Controller PCB that is intended for use with the evaluation board, if so required.

Different configurations of the evaluation board will allow for evaluation of different aspects of the MV3000, each test set-up being described separately. Programming of the SLAC can be achieved by using a control circuit such as is described in the PABX/Line Card Application Note, AN42. This control circuit provides interface to a microprocessor, but can be used with other circuits generating 8-bit parallel data. Such a circuit, which generates 8-bit data and allows control of the evaluation board from a simple 4 x 4 keypad, has been built into the Controller PCB.

THE EVALUATION BOARD CIRCUIT

The circuit of the evaluation board is shown in Fig.1. The two MV3000 SLACs provide all possible configurations of evaluation that may be required. A 2MHz clock input is divided down to provide Frame Sync information for the SLACs by two 74HCT161s. Master Clock, Transmit, Receive and Control Clocks are all connected to the same 2MHz input. The serial digital control ports of each SLAC are taken separately to a 16 pin DIL socket (the Serial Control Connector).

THE EVALUATION BOARD PCB

The layout/component overlay of the PCB is shown in Fig.2. Analog inputs/outputs are connected to the board via SMC connectors, as is the 2MHz clock. The analog inputs may be terminated on the board, if so required. Digital and Analog ground are combined as a single ground plane. Both MV3000s are mounted on the board in 28 pin DIL sockets. External control or stand alone operation of the SLACs is achieved by the connections made via the 16 pin Serial Control Connector (SCC), the pinout for which is given in Table 1.

There are two basic options for use of the PCB. Firstly, whether to use one or both SLACs. Secondly, an 8-way DIL switch can be placed in the SCC, or both SLAC control ports bussed together and driven externally. This gives rise to the four test set-ups as described below. A separate connector (PCM Connector) provides access to MCLK (CLKX, CLKR, DCLK), FS, DXA/B, DRA/B, +5V and 0V.

Test Set-Up 1

This is used for single ended D-A, A-D evaluation of the MV3000. Digital access is via the PCM Connector, analog via the SMC connectors. All that is required is to provide a 2MHz source to synchronise the SLAC to the external test system.

The SCC pins can be wired with CDIO = +5V and $\overline{CS}$ = 0V to utilise the MV3000 stand alone operation. This can be achieved by placing an 8-way SPST DIL switch in the connector, with switches 2 and 3 or 6 and 7 in the 'ON' position as necessary. This mode allows such simple tests as reproduction of a digital milliwatt.

Test Set-Up 2

This is set-up physically the same as set-up 1, except for the connections to the Serial Control Connector. Instead of the DIL switch, the SCC can be connected to an external controller. This will allow for example, time slot switching, gain increment/decrement as well as reproduction of a digital milliwatt.

Test Set-Up 3

This is essentially the simplest mode of operation of the PCB. Both SLACs are used in the board, with only the external 2MHz clock being required. With an 8-way SPST DIL switch in the SCC, switches 2, 3, 6 and 7 are in the 'ON' position. This puts both SLACs into 'Stand Alone' operation. Since the DXA/B and DRA/B pins are bussed separately between SLACs, then the default Tx/Rx in TS0 selection of each SLAC does not result in contention on the same bus. On power-up of the board, the analog input of each SLAC is thus connected through to the analog output of the other. This mode essentially allows low noise evaluation of the analog characteristics with as little injection of externally generated noise as possible, should this prove necessary for SLAC evaluation.

Test Set-Up 4

Essentially this is physically configured as set-up 3 and controlled as set-up 2, with both SLACs in circuit and external control. This will allow evaluation of the B filter and also the X_F and R_F filter characteristics (see Fig.3).

For B filter cancellation tests, the analog output of SLAC2 can be connected (looped back) to its analog input (either directly or through a filter/delay network, such as a Subscriber Line Interface Circuit, i.e. SLIC). The ability of SLAC 2 to cancel received digital data from the transmitted digital data, can be checked by monitoring the analog output of SLAC 1. B filter coefficients are loaded, via the controller, into SLAC 2. The signal source can be digital (SLAC 2 DRB pin, i.e. DXB1), or analog by use of the spare A-D on SLAC 1.

To determine X_F and R_F performance, only one AIN AOUT direction is required. Comparision of pass band characteristics between filter ON and filter OFF conditions will reveal the tested filter response.

CONTROLLER PCB

The circuit described here makes use of the PABX/Line Card Controller circuit, as described in the PABX/Line Card Application Note AN42, to control the evaluation board. That control circuit is capable of interfacing a number of MV3000s to a microprocessor. It was essentially designed to be used with an Intel type 8051 processor. It is possible therefore, that by using a suitable microprocessor emulator the Control Address/Data for the Controller can be generated from a terminal/keyboard connected to the emulator. If this set-up is not available, however, an alternative 8-bit parallel data source is required.

To meet this possibility, a simple method of generating 8-bit data for the Controller from a 4 x 4 keypad was designed. This circuit is combined with the controller circuit, as shown in Fig.4, and thus results in the final Controller PCB circuit. Note that the controller section of this final circuit has slight modifications to that of AN42, these being described later.

The circuit works by first generating 4-bit data from the keypad. A '574 type latch then acts as a 4-bit wide, 2 stage shift register, clocked by the keypad strobe, to give 8-bit data (Source Data, SD). This data is displayed on DIL LED array #1. When the 'GO' key (S3) is pressed, a sequence of $\overline{WR}$ and $\overline{RD}$ pulses is generated to first load to, and then read data from the Controller via the AD Bus. If the A0 switch (S1) is

held down (ON), whilst S3 is pressed, then the 8-bit Source Data (SD) is Control Address, and if S1 is left open, then SD will be Control Data (see AN42). The data presented by the Controller to the AD Bus during the read part of the 'GO' sequence, is clocked into a second '574 latch (SD is disabled), and displayed separately on DIL LED array #2. Thus DIL LED array #1 shows data to be sent to the Controller, and DIL LED array #2 shows data that has been read from the Controller. Closing S2 will cause the GO sequence to repeat continually as opposed to once, which is useful for diagnostic purposes (switch not provided on the Controller PCB).

Modifications to the controller section of the PCB, as mentioned earlier in the text, result in additional features which can be activated by the RD switch, S4. This RD switch activates only the read part of the normal 'GO' sequence. Thus, pressing RD whilst A0 is held down, will cause Control Address to be read from the Ghost Latch into the DOUT latch. If A0 is not held down when RD is pressed, then the '299 register contents will be clocked into this latch instead.

Fig.5 shows the component layout of the Controller PCB. Note that any other circuit that simulates the 8051 external data memory write/read cycle, may be combined with the Controller circuit described in AN42 in order to control the MV3000 evaluation board.

USING THE CONTROLLER PCB

Since the two SLAC's of the evaluation board are wired to CA6 and CA7 of the controller circuit, then an address value with bits 6 and 7 = 0 must be set up. The keypad is used (in two successive depressions) to set up the required address (DIN LEDs). The A0 key is now held down whilst the GO key is pressed. The DOUT LEDs should now show the same DIN address. Data can now be sent to the addressed SLAC/s by first setting up a data byte on the DIN LEDs, then pressing the GO key when required (A0 not used). Note that to get uncorrupted data from a SLAC to the controller PCB, then FFH must be used as DIN in such circumstances (see also PABX/Line Card Controller application note AN42). Note that DIN can be left as FFH, each go depression giving the next data byte out as displayed on the DOUT LEDs.

To check the address in the controller, then A0 can be held on whilst pressing the RD key. The preset address will now appear on DOUT. Also the Data in from the SLAC can be verified by pressing RD with A0 open, data again appearing on DOUT.

Pin Number	Pin Name	Pin Number	Pin Name
1	$CDIO_1$	16	NC
2	$CDIO_1$	15	DV_{CC}
3	$\overline{CS}_1$	14	GND
4	NC	13	NC
5	NC	12	AV_{CC}
6	GND	11	$\overline{CS}_2$
7	DV_{CC}	10	$CDIO_2$
8	NC	9	$CDIO_2$

Table 1 MV3000 evaluation board, serial control connector pinout

Pin Number	1	2	3	4	5	6	7	8
Pin Name	0V	+5V	CLK	FS	DXB_1	DXB_2	DXA_1	DXA_2

Table 2 MV3000 evaluation board, PCM connector pinout

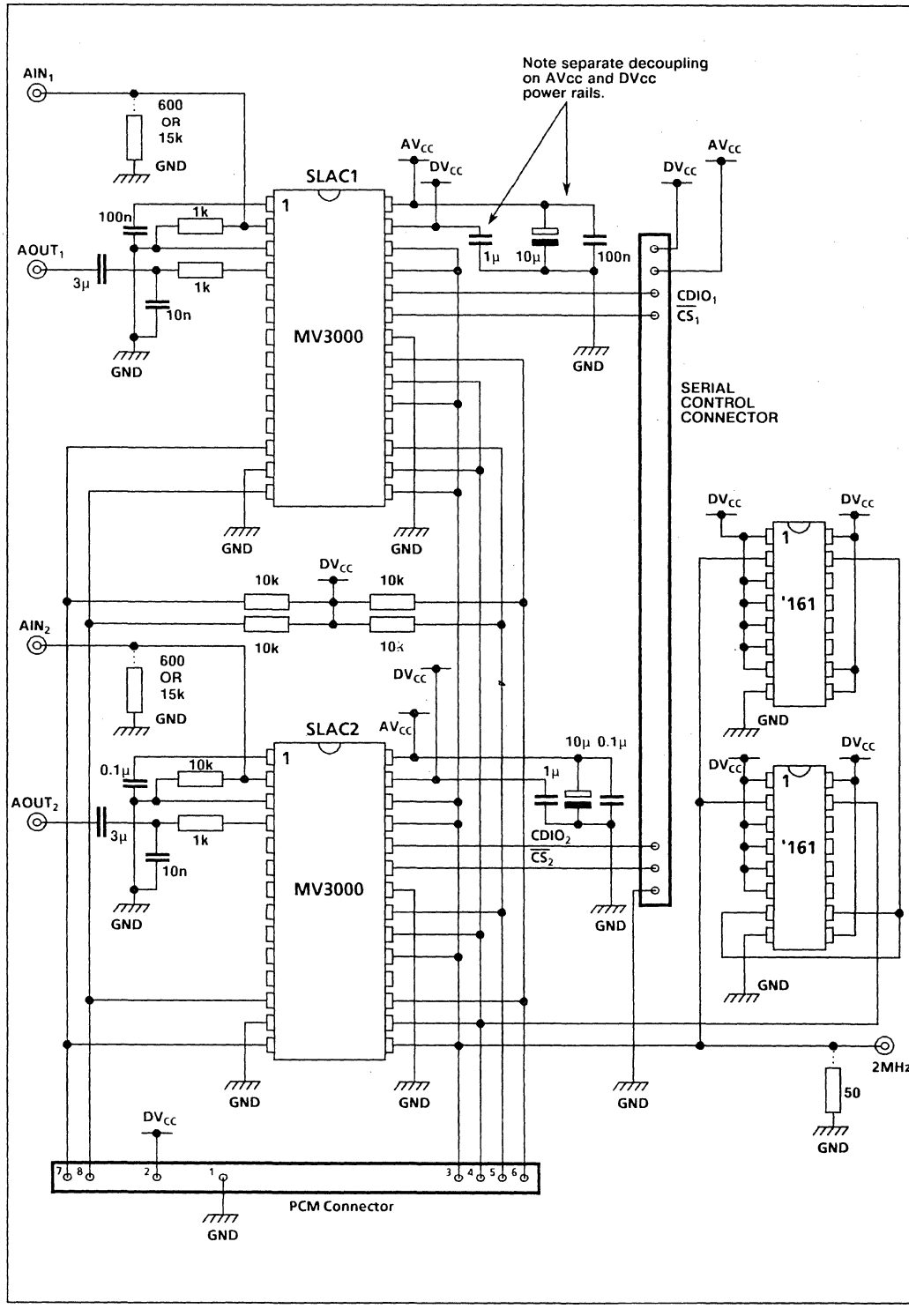


Fig.1 MV3000 evaluation board circuit diagram

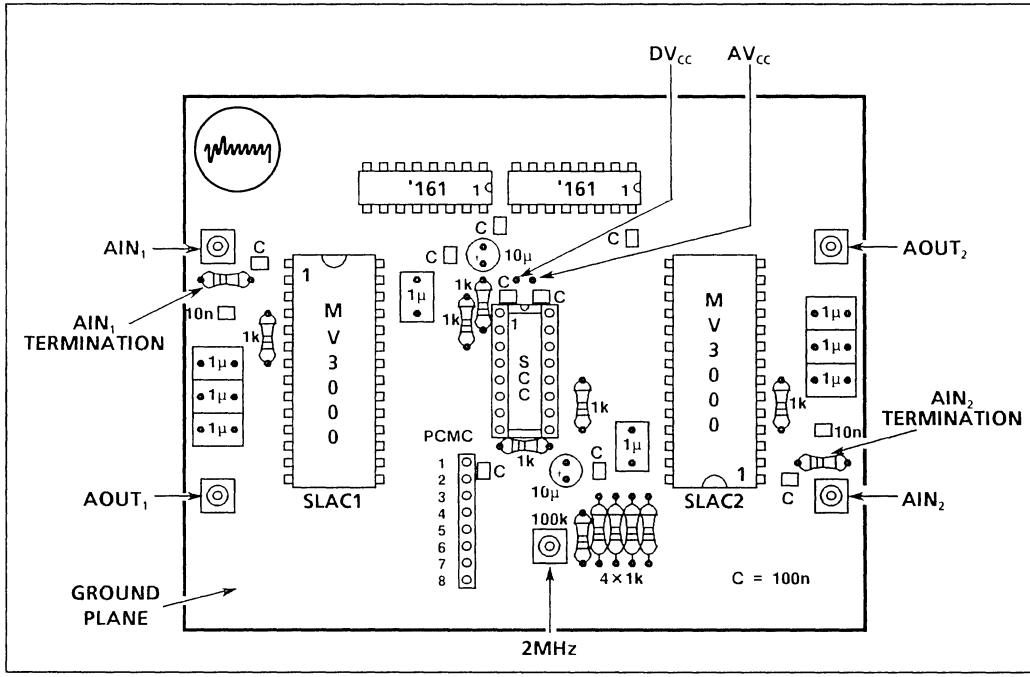


Fig.2 MV3000 evaluation board, component layout

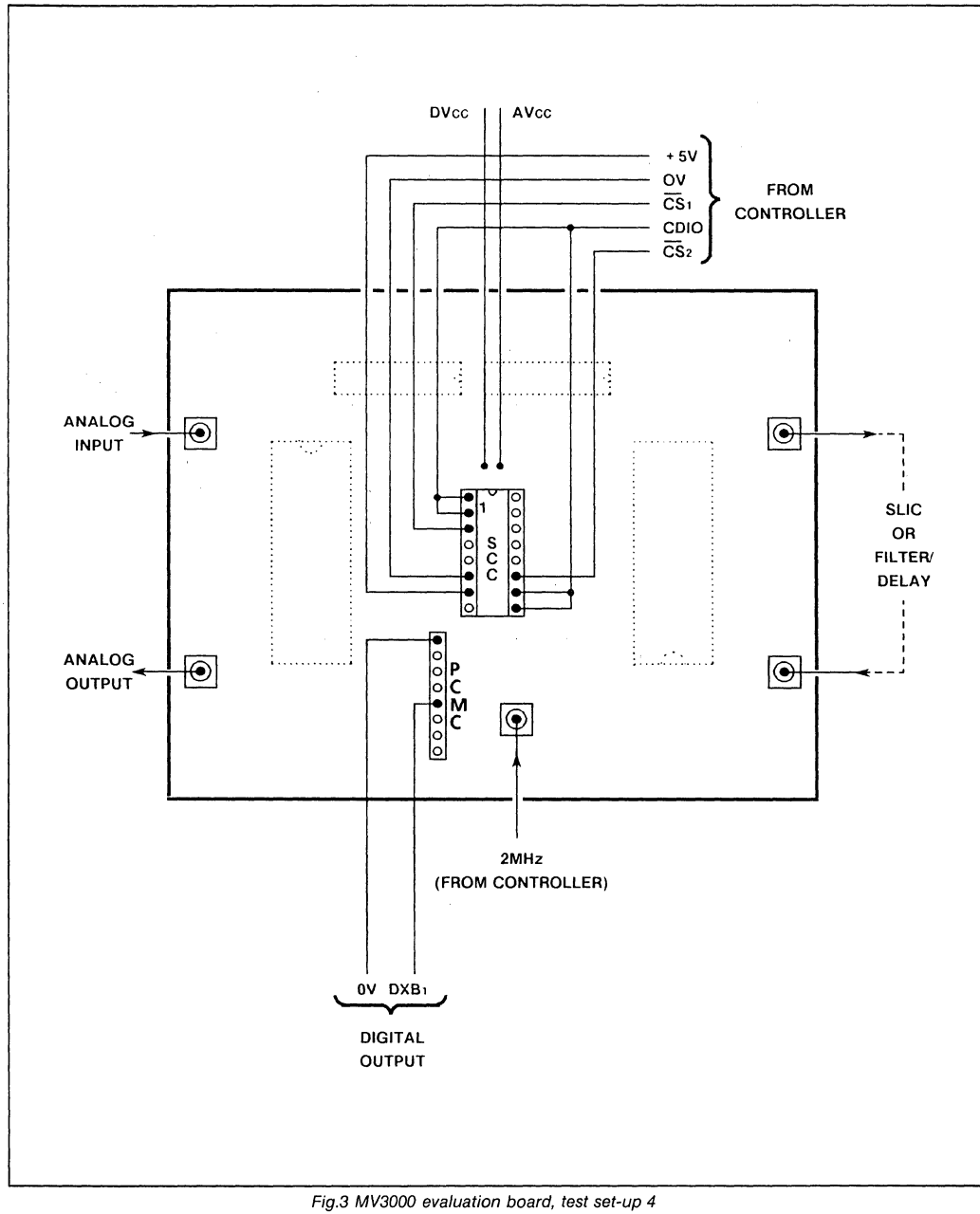


Fig.3 MV3000 evaluation board, test set-up 4

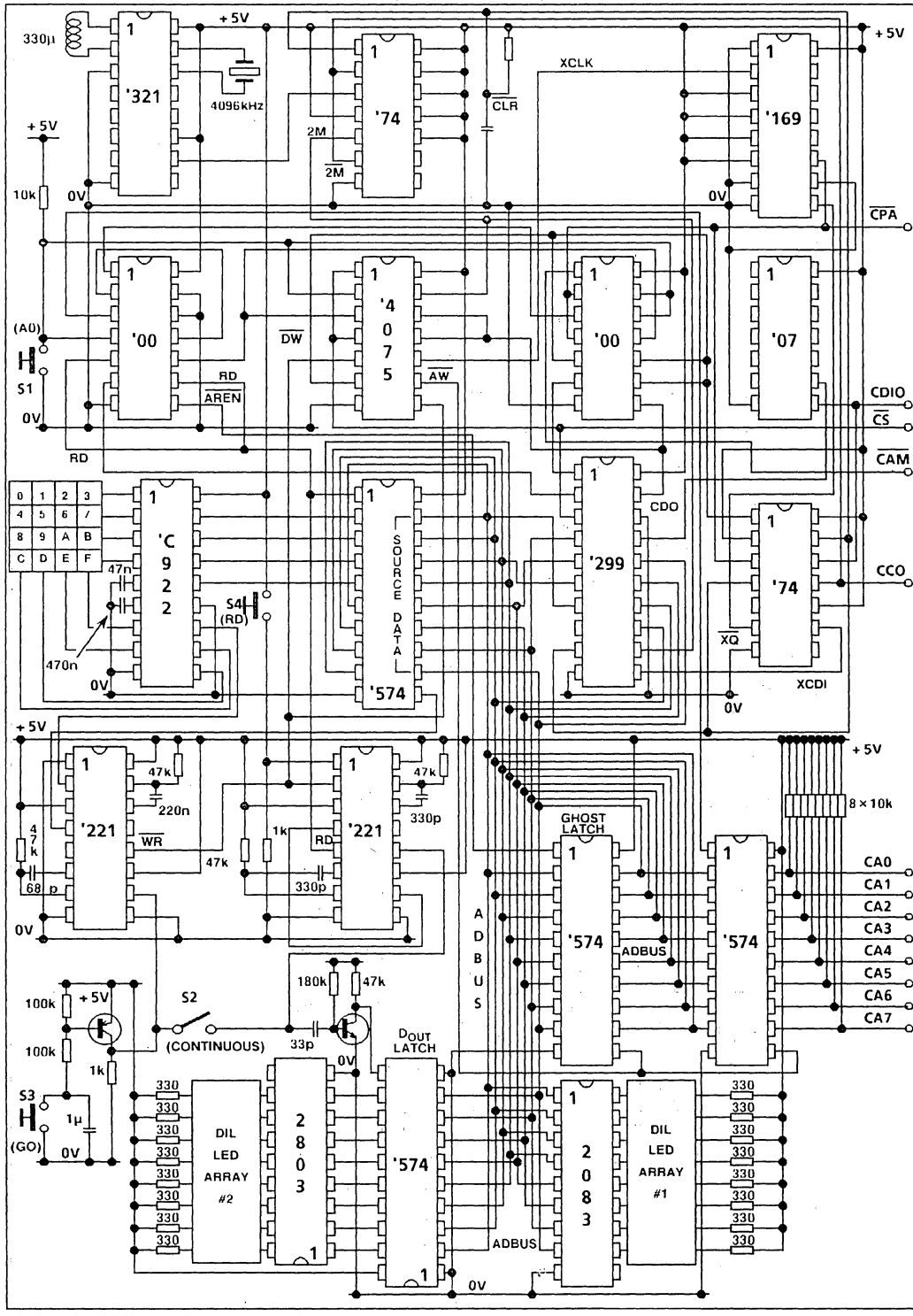


Fig.4 Controller PCB circuit diagram

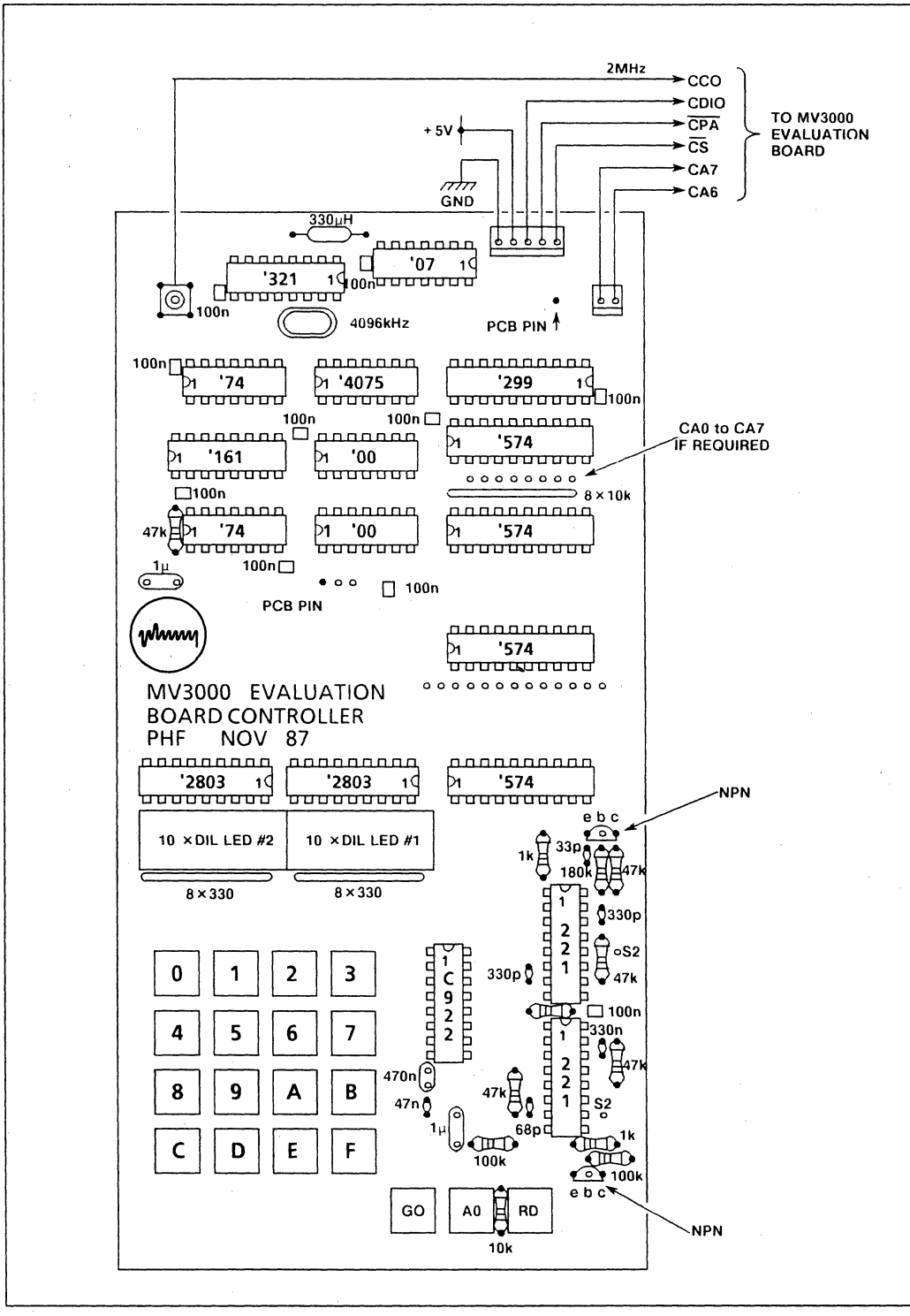
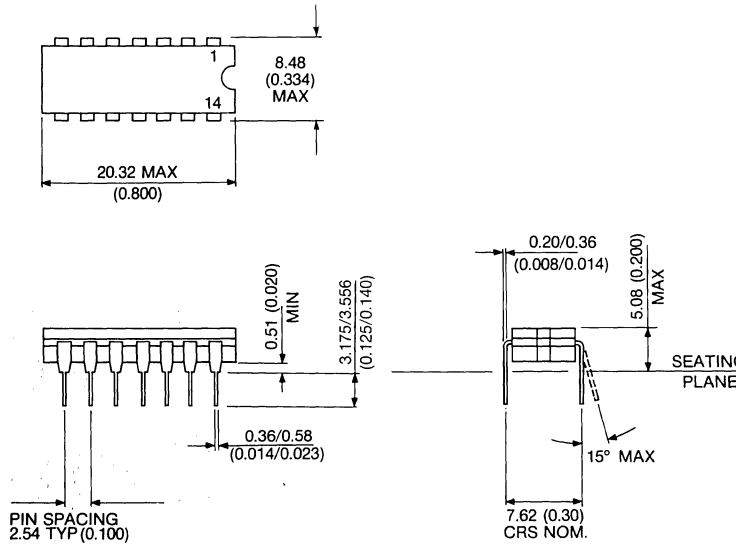
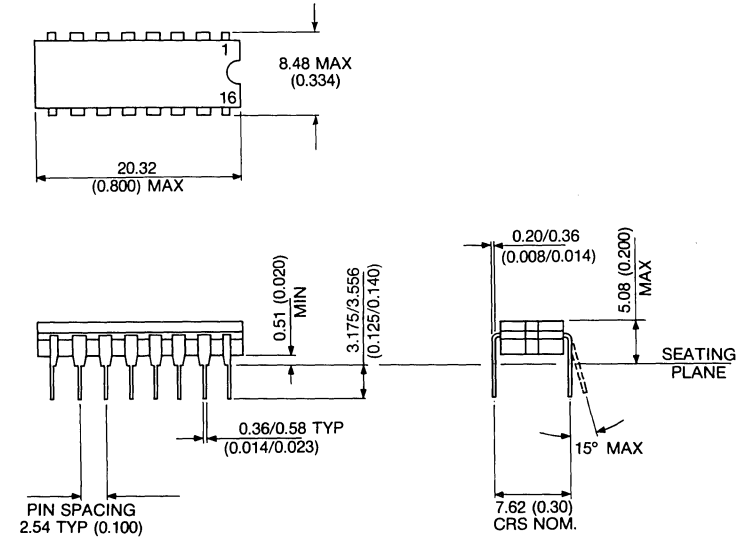


Fig.5 Controller PCB component layout

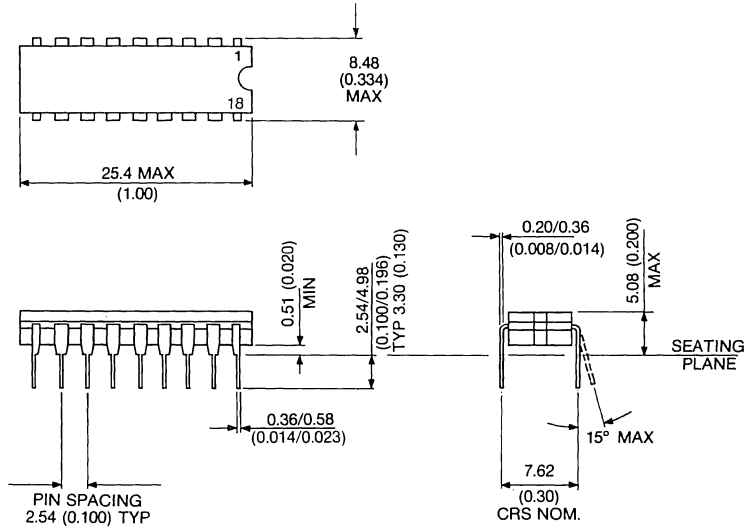
Package Outlines



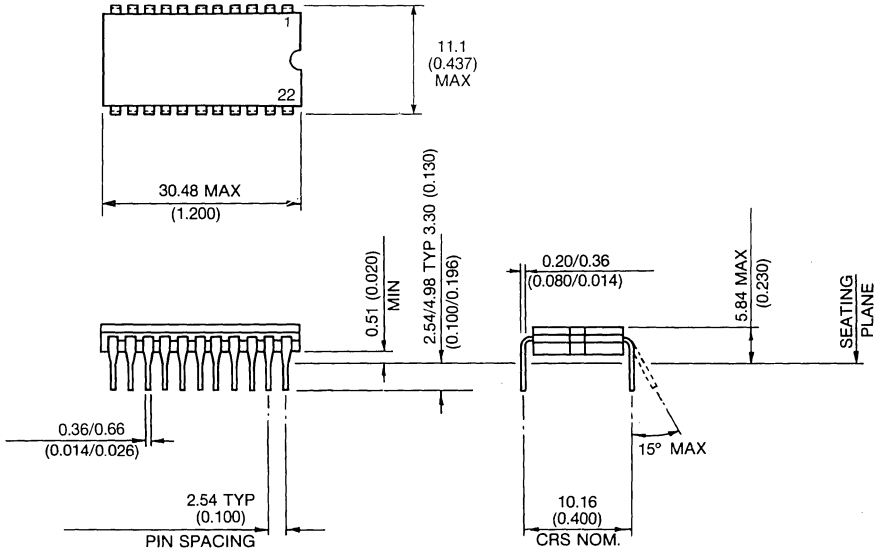
14-LEAD CERAMIC DIL - DG14



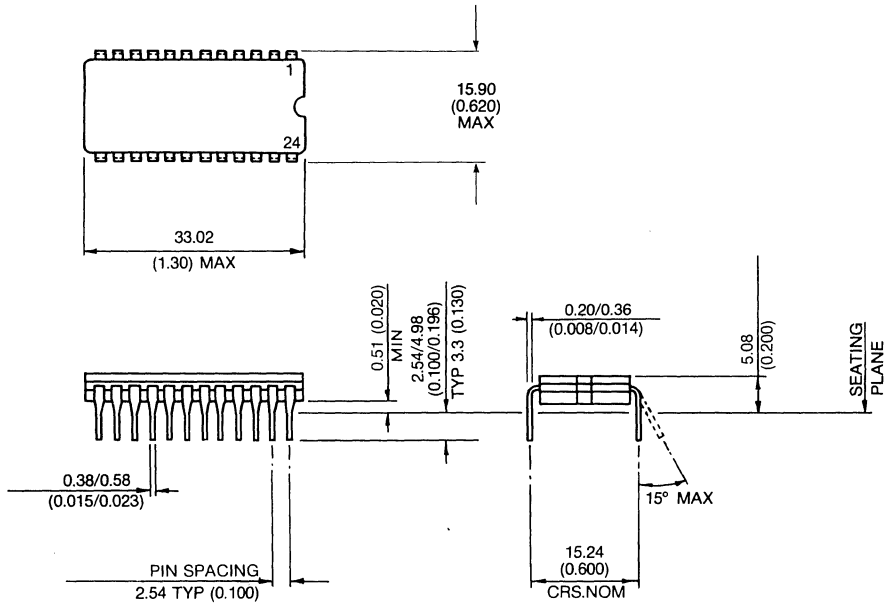
16-LEAD CERAMIC DIL - DG16



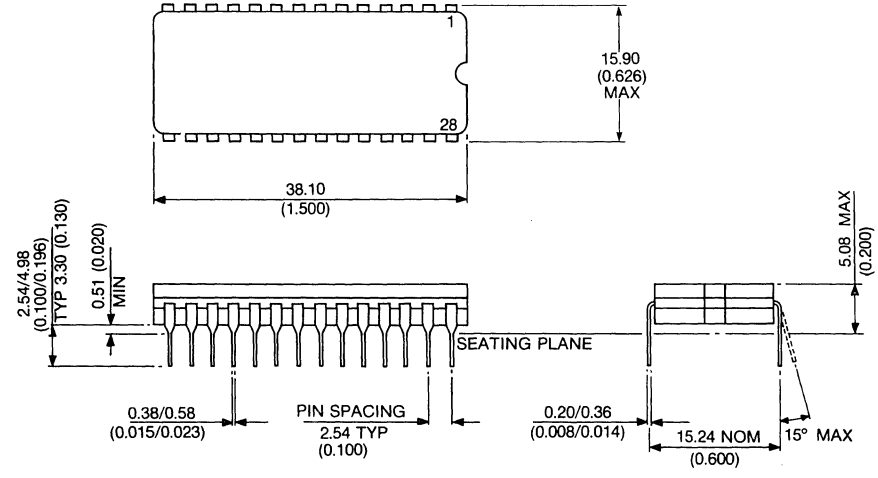
18-LEAD CERAMIC DIL - DG18



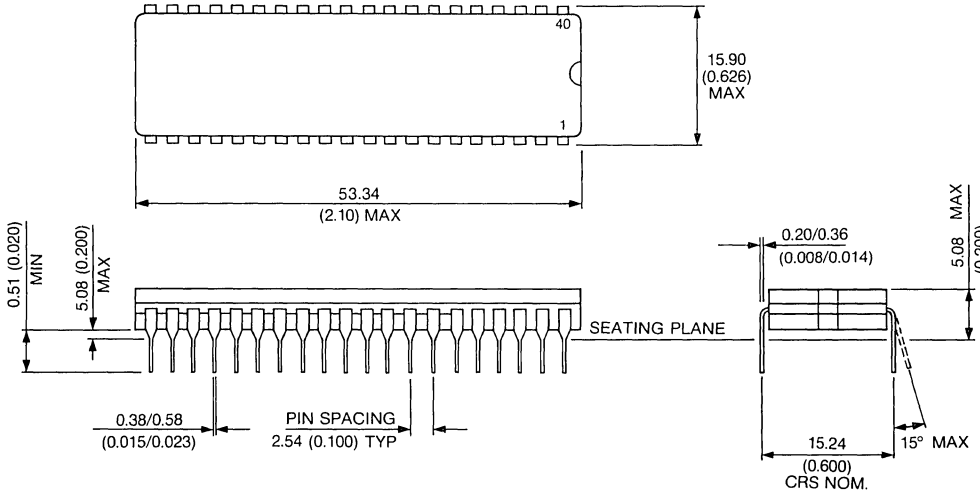
22-LEAD CERAMIC DIL - DG22



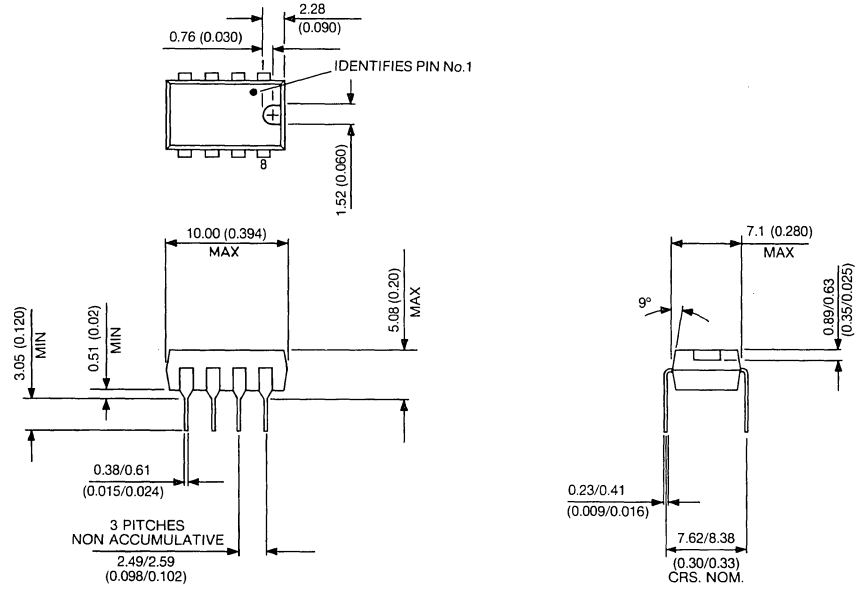
24 LEAD CERAMIC DIL - DG24



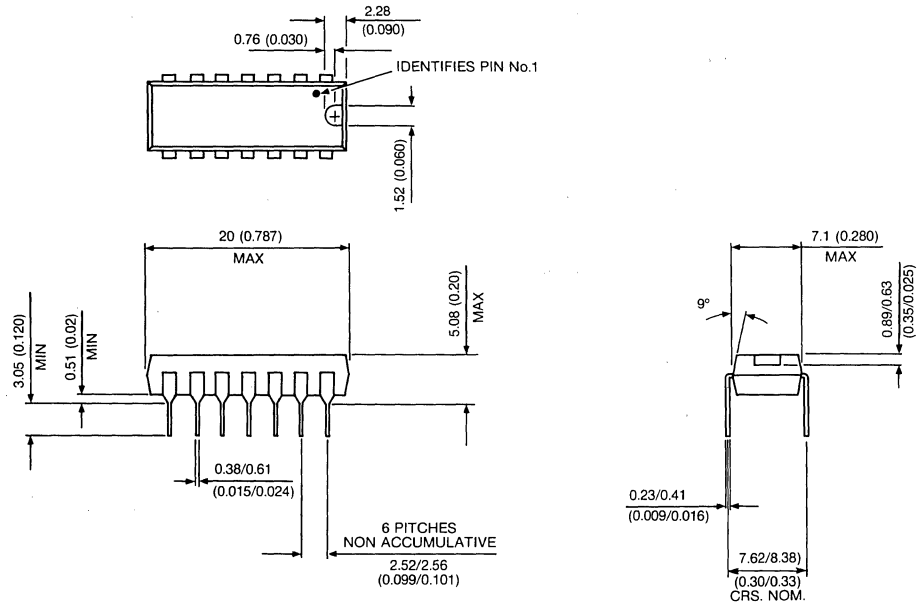
28-LEAD CERAMIC DIL - DG28



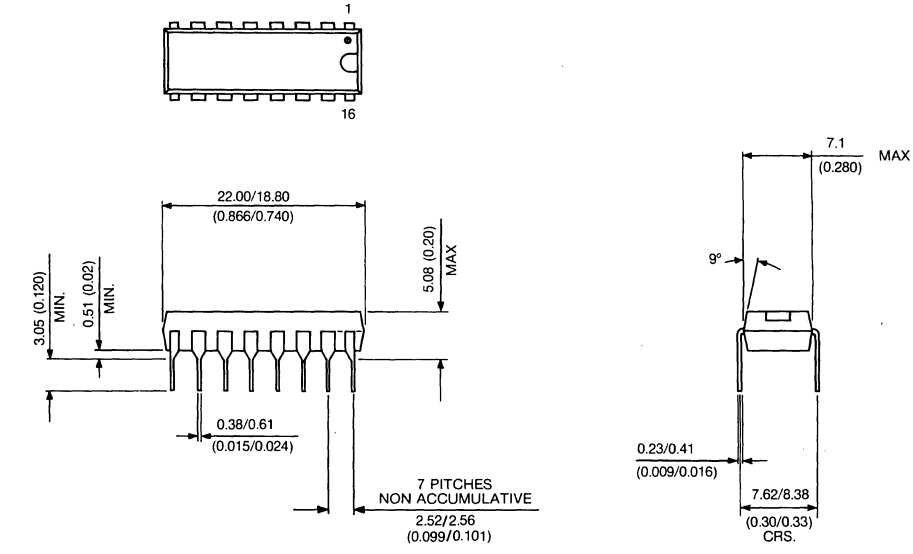
40-LEAD CERAMIC DIL - DG40



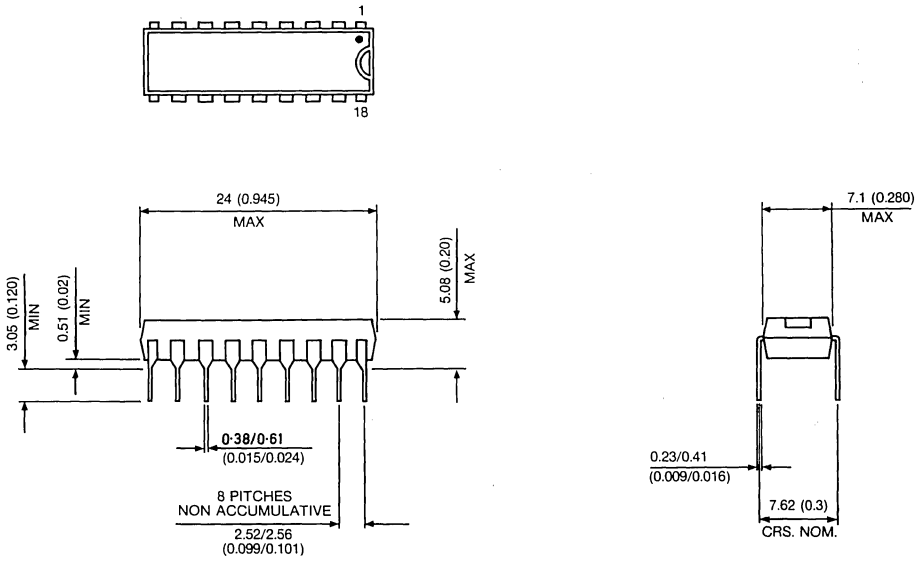
8-LEAD PLASTIC DIL - DP8



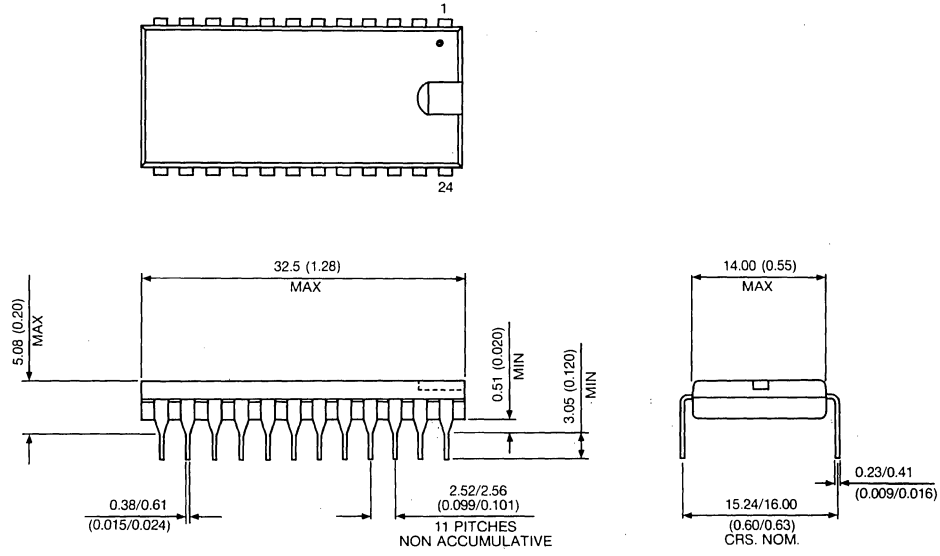
14-LEAD PLASTIC DIL - DP14



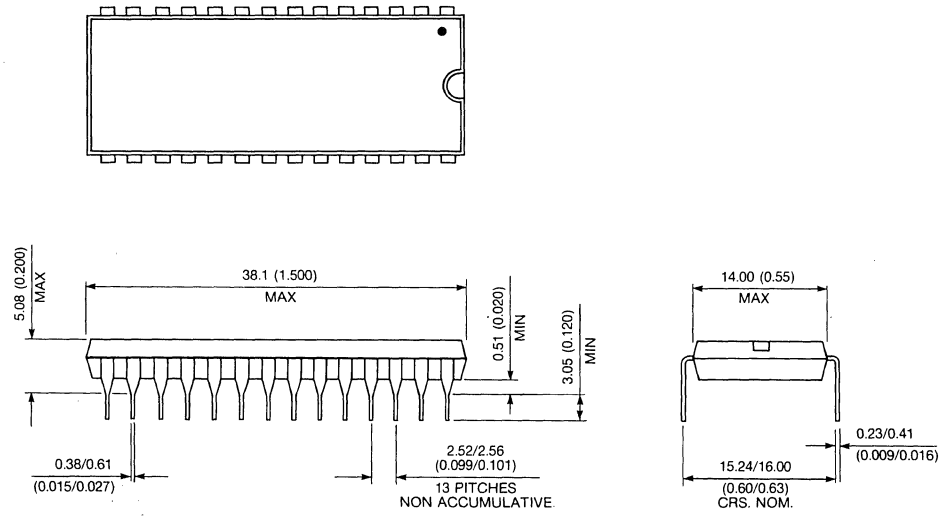
16-LEAD PLASTIC DIL - DP16



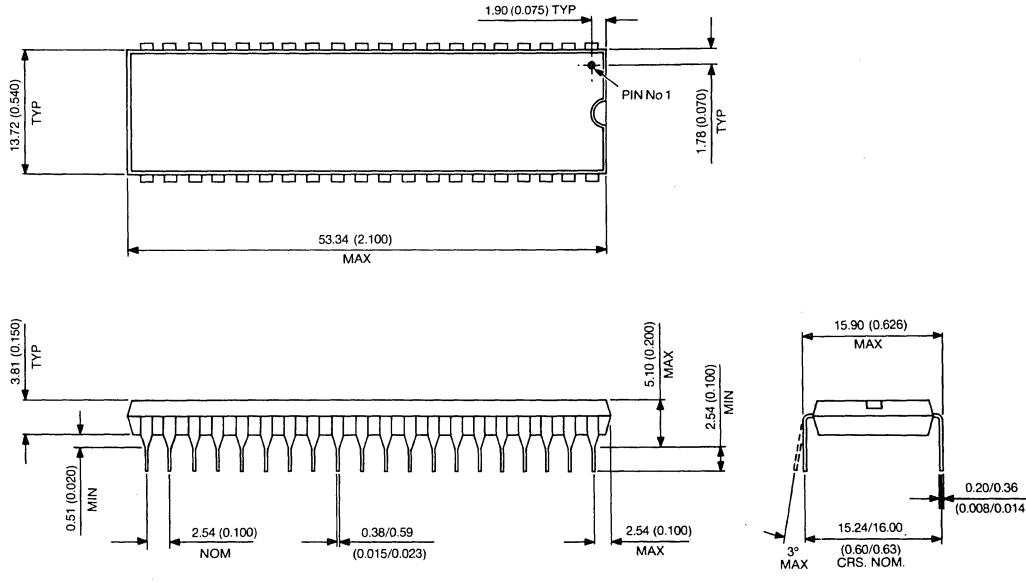
18-LEAD PLASTIC DIL - DP18



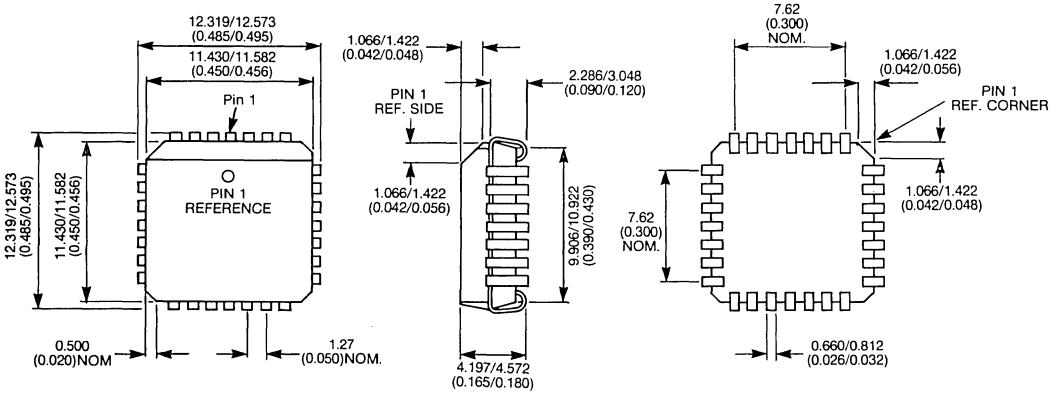
24-LEAD PLASTIC DIL - DP24



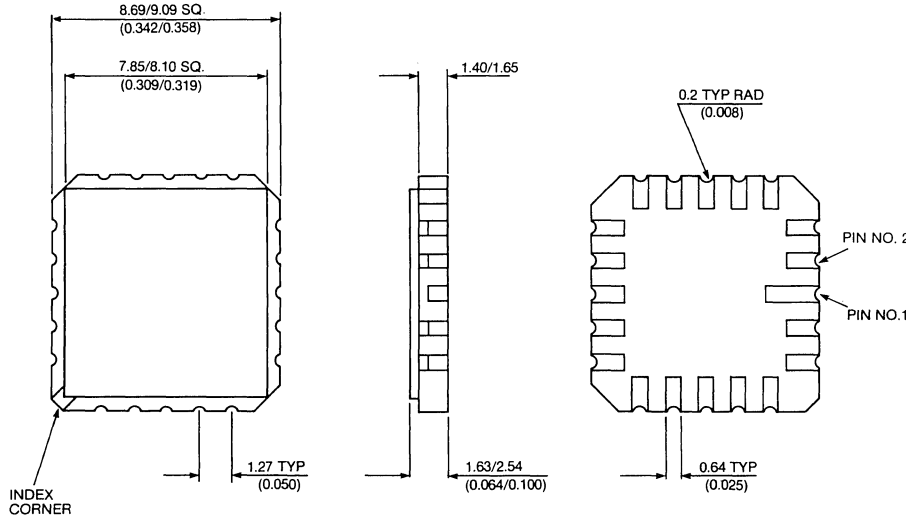
28-LEAD PLASTIC DIL - DP28



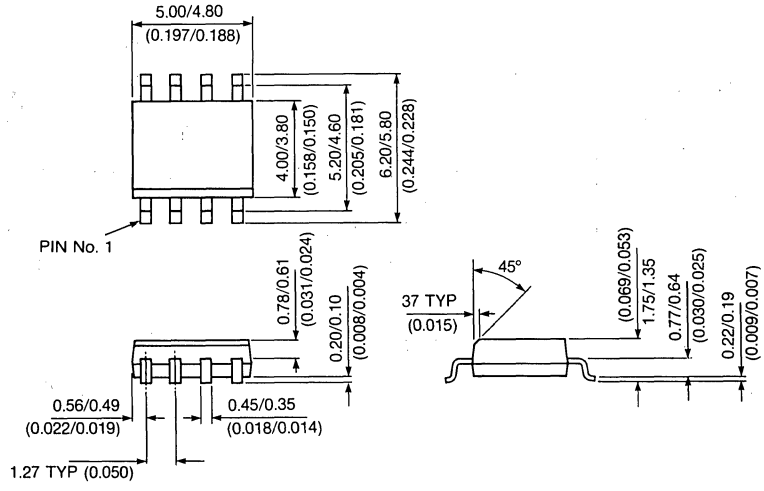
40 LEAD PLASTIC DIL - DP40



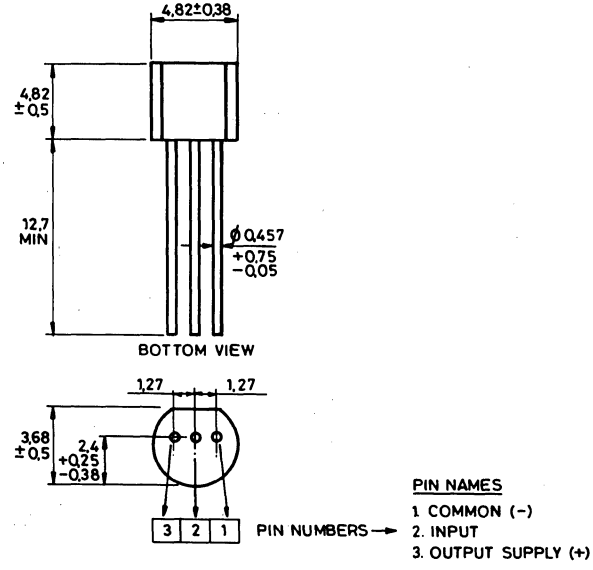
28-LEAD QUAD PLASTIC J LEAD - HP28



20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)



8-LEAD MINIATURE PLASTIC DIL - MP8



Dimensions in millimetres

TO-92 PLASTIC

Plessey Semiconductors Locations

Main offices

HEADQUARTERS **Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext. 2198.

NORTH AMERICA **Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

International marketing centres

BENELUX **Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.

FRANCE **Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.

ITALY **Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.

UNITED KINGDOM (SOUTH) **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666 Ext.250.

UNITED KINGDOM (NORTH) **Plessey Semiconductors Ltd.,** Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.

WEST GERMANY, AUSTRIA and SWITZERLAND **Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.

SOUTH EAST ASIA **Plessey Company plc.,** Room 2204-7 Harbour Centre, 25 Harbour Road, Wanchai, Hong Kong. Tel: 58332111 Tx: 74754 Fax: 58339090.

World-wide agents

AUSTRALIA and NEW ZEALAND **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.

EASTERN EUROPE **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. U.K. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666.

GREECE **Mammeas,** Representations & Exportations, P.O.Box 181, Piraeus. Tel: 4172597 Tx: 213835 LHGR.

INDIA **Semiconductors Ltd.,** 71 Mittal Chambers, Nariman Point, Bombay 400 021. Tel: 2874518 Tx: 11 2781 ADOR IN.
Semiconductors Ltd., Unity Buildings, J.C. Road, Bangalore 560-001. Tel: 52072 & 578739.
Semiconductors Ltd., 513, Ashoka Estate, 24, Barakhamba Road, New Delhi — 110001. Tel: 44879 Tx: 31 3369.
Khandelwal Herrmann Electronics Limited, B-207, Neelam Centre, Worli, Bombay-400 025. Tel: 4947476.

JAPAN **Cornes & Company Ltd.,** Maruzen Building, 2 Chome Nihonbachi, Chuo-Ku, C.P.O.Box 158, Tokyo 100-91. Tel: 010 81 3 272 5771 Tx: 24874 Fax: 271-1479.
Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 532 1012 Tx: 525-4496 Fax: 541-8850.
Microtek Inc., Itoh Bldg., 7-9-17 Nishishinjuku, Shinjuku-ku, Tokyo 160. Tel: 03-371-1811 Tx: J27466 Fax: 03-369-5623.

HONG KONG **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kok Street, Tsuen Wan, N.T., Hong Kong. Tel: 0-444241-6 Tx: 36590 Fax: 499-3065.

KOREA **Young O Ind Co. Ltd.,** Yeoevido, P.O.Box 149, Seoul. Tel: 782 1707 Tx: K25701. Fax: 784 6786.
KML Corporation, 3rd Floor, Banpo Hall Building, 604-1 Banpo Dong, Kangnam-Ku, P.O.Box 19, Seoul. Tel: (02) 533-9281/2 Tx: KMLCORP K25981 Fax: (02) 533 1986.

MALAYSIA **Plessey Malaysia,** 1602 Pernas International Bldg, Jalan Sultan Ismail, Kuala Lumpur 50250. Tel: (03) 2611477 Tlx: 30918 PLESCOMA Direct Fax: (03) 2613385.

SCANDINAVIA

Denmark **Scansupply,** Nannasgade 18, DK-2200 Copenhagen N. Tel: 45 1 83 50 90 Tx: 19037 Fax: 45 1 83 25 40.

Finland **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 90 55 00 02 Tx: 122214 Fax: 055 1117.

Norway **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, Oslo 5. Tel: 02 64 11 50 Tx: 71963 Fax: 02 643443.

Sweden **Swedesupply AB,** PO Box 1028, 171 21 Solna. Tel: 08/735 81 30 Tx: 13435 Fax: 08/839033.

SINGAPORE **Plessey S.E. Asia Pte Ltd.,** 400 Orchard Road, No. 21-07 Orchard Towers, Singapore 0923. Tel: 7325000 Tx: RS22013 Direct Fax: 7329036.

SOUTH AFRICA **Plessey South Africa Ltd.,** 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793, Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SPAIN **JR Trading,** Apartado de Correos 8432, Madrid 8 Tel: 248 12 18/248 38 82 Tx: 42701. Fax: 241 4460.

TAIWAN **Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan, Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.

TURKEY **The Plessey Company plc.,** Koroglu Caddesi 5/4, Gaziosmanpasa, Ankara. Tel: 010 90 41 367352 Fax: 46526.

World-wide distributors

AUSTRALIA **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney (02) 720133 Tx: AA20384 Direct Fax: (02) 7260669.

AUSTRIA **DAHMS Elektronik Ges. mbH,** Wiener Str. 287, A-8051 Graz. Tel: 0316/64030 Tx: 31099. Fax: 0316/6403029.

Othmar Lackner, Landstrasser Hauptstr. 37, A-1030 Wien. Tel: 0222 75 26 18-0 Tx: 111198. Fax: 0222/7526185.

BELGIUM **Master Chips,** 4 St. Lazarus Laan, 1030 Brussels. Tel: 02 219 58 62 Tx: 62500. Fax: 02 217 92 01.

FRANCE **Mateleco:**

Ile de France, 66, Avenue Augustin Dumont, 92240 Malakoff. Tel: (1) 46 57 70 55 Tx: 203436F.

Rhone-Alpes, 2 Rue Emile Zola, 38130 Echirolles. Tel: 76 40 38 33 Tx: 980837F.

ICC:

Bordeaux, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539F. Fax: 61 48 11 25.

Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalieres. Tel: 73 36 71 41 Tx: 990928F.

Marseille, Z.A. Artizanord II, 13015 Marseille. Tel: 91 03 12 12 Tx: 441313F.

Toulouse, 78 Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10 Tx: 520897F.

CGE Composants S.A.:

Ile de France, 32 Rue Grange Dame Rose, 92360 Meudon la Foret. Tel: (1) 46 30 24 45 Tx: 632253F Fax: 46 30 0081.

Aquitaine, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40 Tx: 571224F.

Bretagne, 9 Rue du General Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311F.

Centre/Pays-de-Loire, Allee de la Detente, 86360 Chaseneuil du Poitou. Tel: 49 52 88 88 Tx: 791525F.

Est, 27 Rue Kleber, 68000 Colmar. Tel: 89 41 15 43 Tx: 870569F.

Midi-Pyrenees, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38 Tx: 530957F.

Nord, 2 Rue de la Creativite, 59650 Villeneuve d'Ascq. Tel: 20 67 04 04 Tx: 136887F.

Provence/Cote d'Azur, Avenue Donadei, bat.B, 06700 St. Laurent du Var. Tel: 93 07 77 67 Tx: 461481F.

Rhone-Alpes, 101 Rue Dedieu, 69100 Villeurbanne. Tel: 78 68 32 29 Tx: 305301F.

ATAC-Diffusion SA, 2 Rue-Lecointre, 7 Ave de l'Europe, 92310 Sevres. Tel: 14 507 11 11 Tx: 203047 Fax: (1) 45341042.

ITALY **Eurelettronica SpA,** Via E Fermi 8, 20090 Assago (Milan). Tel: 02-4880022 Tx: 350037. Fax: 488 0275.

Eurelettronica, Via Bertoloni 27, Rome. Tel: 875394 Tx: 610358.

Alta S.R.L., Via Matteo Di Giovanni 6, 50143 Florence. Tel: 055717402 Tx: 571246. Fax: 055/705658.

Adelsi Spa, Via Novara 570, 20153 Milan. Tel: 02 3580641 Tx: 332423 Adelsy I Fax: 02/3011988.

ESCO Italiana Spa., Via Modena 1, 20099 Sest S Giovanni. Tel: 02 24 09 241-251 Tx: 322383. Fax: 02/2409255.

Fanton S.R.L., Bologna, Milano, Firenze, Roma, Padora, Torino. Tel: (02) 3287312 Fax: 051/732216.

NETHERLANDS **Heynen B.V.,** Postbus 10, 6590 AA Gennep. Tel: 8851-96111 Tx: 37282 Fax: 08851 96220.

Tekelek Airtronic BV., Postbus 63-2700 AB, Zoetermeer. Tel: 079 31010 Tx: 33332. Fax: 079 417504.

SOUTH AFRICA **Plessey South Africa Ltd.,** 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793 Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SWITZERLAND **Aumann & Co. AG,** Forrlibuckstrasse 150, CH-8037 Zurich. Tel: 01/443300 Tx: 822966. Fax: 01/44 5023.

Elbatex AG., Hardstr. 72, 5430 Wettingen. Tel: 056 27 51 11 Tx: 58068 Fax: 056/271924.

TAIWAN **Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipai, Taiwan, Republic of China. Tel: (02) 7526330 Tx: 27113 ARTISTEX Fax: (8862) 721 5446.

UNITED KINGDOM **Celdis Ltd.,**37-39 Loverock Road, Reading, Berks RG3 1ED. Tel: 0734 585171 Tx: 848370 Fax: 0734 509933.

Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU. Tel: 0532 636311 Tx: 55147 Fax: 0532 633404.
Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878/787848 Tx: 847571 Fax: 0734 776095.
Gothic Crellon Ltd., P.O.Box 301, Trafalgar House, 28 Paradise Circus, Queensway, Birmingham B1 2BL. Tel: 021 6436365 Tx: 338731.
RR Electronics Ltd., St. Martins Way, Cambridge Road, Bedford MK42 0LF. Tel: 0234 47188/270777 Tx: 826251 Fax: 0234 210674.
Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street, Yiewsley, West Drayton, Middlesex UB7 7XB. Tel: 0895 445522 Tx: 21958 Fax: 0895 422044.
STC Electronic Services, Edinburgh Way, Harlow, Essex CM20 2DF. Tel: 0279 626777 Tx: 818801. Fax: 0279 441687.
Unitel Ltd., Unitel House, Fishers Green Road, Stevenage, Herts. Tel: 0438 312393 Tx: 825637. Fax: 0438 318711.

UK EXPORT (to countries other than those listed)

Extram (U.K.) Ltd., 1A Albert St., Slough, Berks. SL1 2BH. Tel: 0753 824311 Tx: 848441 EXTRAM G Fax: 0753 820250.

WEST GERMANY

Altron GmbH & Co. KG, Gaussstr. 10, 3160 Lehrte. Tel: 051 32 5 30 24 Tx: 922383 Fax: 05132/57776.
API Elektronik Vertriebs GmbH, Augustinerring 27, D-8062 Markt Indersdorf. Tel: 08136/7092 Tx: 5270505 Fax: 08136/7398.
AS Electronic Vertriebs-GmbH, Elisabethenstrasse 35, 6380 Bad Homburg. Tel: 06172/2 90 28-29 Tx: 410868.
Astronic GmbH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187 Fax: 089 300 6001.
Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708. Fax: 07159/5119.
Weisbauer Elektronik GmbH, Heiliger Weg 1, 4600 Dortmund 1. Tel: 0231 57 95 47 Tx: 822538 Fax: 0231/577514.

North American sales offices

NATIONAL SALES — Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066. United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

EASTERN REGION — 1767-42 Veterans Memorial Hwy., Central Islip, NY 11722. Tel: (516) 582-8070 Tlx: 705922 Fax: 516-582-8344.

NEW ENGLAND REGION — 132 Central St., 216 Foxboro, MA 02035. Tel: (617) 543-3855 Tlx: 316805 Fax: 617-543-2994.

WESTERN REGION — 4633 Old Ironsides Dr. 250, Santa Clara, CA 95054. Tel: (408) 986-8911 Tlx: 62217370 Fax: 408-970-0263.

SOUTHEAST REGION — 9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930 Tlx: 510-600-3635 Fax: 214-680-9753.

NORTH CENTRAL REGION — 1919 South Highland 120C, Lombard, IL 60148. Tel: (312) 953-1484 Tlx: 705186 Fax: 312-953-0633.

FLORIDA & DIXIE REGION — 541 S.Orlando Ave., Suite 310, Maitland, FL 32751. Tel: (305) 539-0080 Fax: 304-539-0055.

SOUTHWEST REGION — 9 Parker, Irvine, CA 92718. Tel: (714) 472-2530 Tlx: 989096 Fax: 714-458-7084.

DISTRIBUTION SALES — 9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Tlx: (910) 595-1930 Fax: (714) 770-0627.

CANADA — 207 Place Frontenac, Quebec, H9R-4Z7. Tel: (514) 697-0095/96 Fax: 514-697-0681.

North American representatives

ALABAMA — **DHR Marketing, Inc.,** 904 Bob Wallace Avenue, Suite 222, Huntsville, AL 35801. Tel: (205) 533-5165 Fax: (205) 533-1312.

ARIZONA — **Reptronix/Chaparral,** 4625 South Lakeshore Dr., Tempe, AZ 85282-7127. Tel: (602) 345-4580 Fax: (602) 839-3841.

CALIFORNIA — **Cerco,** 5230 Carrol Canyon Rd. 214, San Diego, CA 92121. Tel: (619) 450-1754 Fax: 619-450-3681.
Pinnacle Sales Corp., 275 Saratoga Ave., Suite 200, Santa Clara, CA 95050. Tel: (408) 249-7400 Fax: 408-249-5129.
Select Electronics, 2109 Brookfield Drive, Thousand Oaks, CA91362.
Straube Associates, 2551 Casey Avenue, Mountain View, CA 94043. Tel: (415) 969-6060 Fax: (415) 964-6526.
Select Electronics, 14730 Beach Blvd-Bldg F, Suite 106, La Mirada, CA 90638. Tel: (714) 739-8891 Twx: 910-596-2818 Fax: 714-739-1604.

COLORADO **MRC,** 2579 W. Main St. Littleton, CO 80120. Tel: (303) 794-4684 Fax: (303) 794-4644.

CONNECTICUT **NRG Ltd.,** 63 Duka Avenue, Fairfield, CT 06430. Tel: (203) 384-1112 Fax: (203) 335-2127.

FLORIDA **Lawrence Associates,** 1131 South U.S.19 Palm Barbor, FL 34684. Tel: (813) 787-2773 Fax: (813) 787-2654.

Lawrence Associates, 380 Lowndes Square, Casselberry, FL 32707. Tel: (305) 339-3855 Fax: (305) 767-0973.

Lawrence Associates, 5021 N. Dixie Highway, Boca Raton, FL 33431. Tel: (305) 368-7373 Fax: 305-394-5442.

GEORGIA **DHR Marketing, Inc.,** 3100 Breckenridge Blvd. Suite 145, Duluth, GA 30136. Tel: (404) 564-0529 Fax: (404) 564-1127.

IDAHO **Crown Electronic Sales, Inc.,** 601 W. Hays, Suite 20, Boise, Idaho 83702. Tel: (208) 344-9588 Fax: (208) 344-9550.

INDIANA **Corrao Marsh, Inc.,** 6211 Stoney Creek Drive, Fort Wayne, IN 46825. Tel: (219) 482-2725 Fax: 219-484-7491.

Corrao Marsh, Inc., 3117 West U.S. 40, Greenfield, IN 46140. Tel: (317) 462-4446. Fax: (317) 462-6568.

ILLINOIS **Micro Sales, Inc.,** 54 West Seegars Road, Arlington Heights, IL 60006. Tel: (312) 956-1000 Twx: 510-600-0756 Fax: 312-956-0189.

IOWA **Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666 Fax: 319-377-2273.

KANSAS **Lorenz Sales, Inc.,** 8115 West 63rd St., Suite 1, Merriam, KS66202. Tel: (913) 384-6556.

MARYLAND **Walker-Houck,** 10706 Reisters Town Rd., Suite D, Owings Mills, MA 21117. Tel: (301) 356-9500 Fax: 301-356-9503.

MASSACHUSETTS **Stone Components,** 2 Pierce Street, Framingham, MA 01701. Tel: (617) 875-3266 Twx: 310-374-6662 Fax: 617-875-0537.

MICHIGAN **R.P. Urban & Associates,** 2335 Burton Street SE, P.O. Box 7386, Grand Rapids, MI49510. Tel: (616) 245-0511 Fax: (616) 245-4083.

R.P. Urban & Associates, 24634 Five Mile Road, Detroit, MI48239. Tel: (313) 535-2355 Fax: (313) 7109.

MINNESOTA **Electro Mark Inc.,** Valley Oaks Business Cntr. 7167 Shady Oak Rd., Eden Prairie, MN 55344. Tel: (612) 944-5850 Fax: (612) 944-5855.

MISSOURI **Lorenz Sales, Inc.,** Del Crest Plaza Bldg. Suite 208, 8420 Delmar Blvd., University City, MO 63124. Tel: (314) 997-4558 Fax: 319-337-2273.

NEBRASKA **Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660.

NEW JERSEY **Metz Benham Associates, Inc., (MBA),** Terrace Level, Suite II, 1982 Greentree Road, Cherry Hill, NJ 08003. Tel: (609) 424-0404 Fax: (609) 751-2160.

Metro Logic, 280 Midland Ave., Bldg N-1, Saddle Brook, NJ 07662. Tel: (201) 797-8844 Fax: 201-797-8418.

NEW MEXICO **Reptronix/Chaparral,** 237 C Eubank Blvd., N.E., Albuquerque, NM 87123. Tel: (505) 292-1718 Fax: (505) 299-1611.

NEW YORK **Micro-Tech,** 1350 Buffalo Road, Rochester, NY 14624. Tel: (716) 328-3000 Fax: (716) 328-3003.

Micro-Tech, 401 South Main Street, North Syracuse, NY 13212. Tel: (315) 458-5254 Fax: (315) 458-5919.

Micro-Tech, 10 Guyton Street, Kingston, NY 12401. Tel: (914) 338-7588.

NORTH CAROLINA **DHR Marketing, Inc.,** 4016 Barrett Drive, Suite 201 (27609) P.O. Box 19703, Raleigh, NC 27609. Tel: (919) 781-1961

SOUTH CAROLINA **DHR Marketing, Inc.,** 37 Villa Road, Suite 409, Greenville, SC 29615. Tel: (803) 271-8712 Fax: (803) 271-8712.

OHIO **Scott Electronics, Inc.,** 3131 S. Dixie Dr., Suite 200, Dayton, OH 45439. Tel: (513) 294-0539 Fax: (513) 294-4769.

Scott Electronics, Inc., 360 Alpha Park, Cleveland, OH 44143. Tel: (216) 473-5050 Fax: (216) 473 5055.

Scott Electronics, Inc., 6515 East Livingston Avenue, Reynoldsburg, OH 43068 Tel: (614) 1281 Fax: (614) 863-1485.

Scott Electronics, Inc., 10901 Reed Hartman Hwy., Suite 301, Cincinnati, OH 45242. Tel: (513) 791-2513 Fax: (513) 791-8059.

OREGON **Core II, P.O. Box 5459, Beaverton, OR 96006-0459.** Shipping Address only: 21785 S.W. T.V. Hwy, Unit Q, Beaverton, OR 97006. Tel: (503) 641-0877 Fax: (503) 591-8383.

Crown Electronic Sales, Inc., 17020 S.W. Upper Boones Ferry Rd., Suite 202, Portland, OR 97223. Tel: (503) 620-8320 Fax: 503-639-4023.

TENNESSEE **DHR Marketing, Inc.,** 417 Welchwood, Suite 102, Nashville, TN 37211.Tel: (615) 331-2745.

TEXAS **Oeler & Menelaides, Inc.,** 8340 Meadow Rd., Suite 24, Dallas, TX 75231. Tel: (214) 361-8876 Fax: (214) 692-0235.

Oeler & Menelaides, Inc., 12777 Jones Rd., Suite 175-18, Houston, TX 77070. Tel: (713) 894-5021.

Oeler & Menelaides, Inc., 8705 Shoal Creek Rd., Suite 218, Austin, TX 78758. Tel: (512) 453-0275 Fax: (512) 453-0088.

WASHINGTON **Core II,** 2535 152nd N.E. Suite A, Redmond, WA 98052. Tel: (206) 746-1799 (Home).
Crown Electronic Sales, Inc., 14400 Bel-Red Rd., 108, Bellevue, WA 98007.
Tel: (206) 643-8100 Fax: 206-747-6861.

WISCONSIN **Micro Sales, Inc.,** N8 W12920 Leon Road, Suite 115, Menomonee Falls, WI 53051.
Tel: (414) 251-0151.

CANADA EASTERN **Gidden-Morton Assoc.Inc.,**7050 Bramalea Road, Suite 27A, Mississauga, Ontario
L5S 1T1. Tel: (416) 671-8111 Fax: (416) 671-2422.
Gidden-Morton Assoc.Inc.,3860 Cote-Vertu, Suite 221, St. Larent, Quebec H4R 1N4.
Tel: (514) 335-9572 Fax: 514-335-9573.
Gidden-Morton Assoc.Inc.,301 Moodie Drive, Suite 101, Nepean, Ontario K2H 9C4.
Tel: (613) 726-0844 Fax: 613-726-0953.

CANADA WESTERN **Dynasty Components, Inc.,** 12618 55A Avenue, Surrey, British Columbia V3W 1C3.
Tel: (604) 597-0068 Fax: (604) 597-0043.

American design centres

ARIZONA **CaDel,** 715 N. Constitution Drive, Dueson, AZ 85748. Tel: (602) 296-8591.

CALIFORNIA **Analog Solutions,** 532 Fourth Street, Encinitas, CA 92024. Tel: (619) 944-1657.
Silicon Development Corp., 16162 Beach Boulevard, Suite 304, Huntington Beach,
CA 92647. Tel: (714) 847-1992.

CANADA **Ontario Centre for Microelectronics,** 1150 Morrison Drive, Suite 400, Ottawa, K2H 9B8.
Tel: (613) 596-6690.
Alberta Microelectronics Center, Suite 200, 1620-29 St., N.W., Calgary, Alberta T2N 4L7.
Tel: (403) 289-2043.

COLORADO **Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.

FLORIDA **Silicon Beach Enterprises, Inc.,** 700 U.S. Highway One, Suite C, North Palm Beach,
FL 33408. Tel: (305) 844-7805.

ILLINOIS **Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Road, Arlington Heights, IL 60005.
Tel: (312) 956-0710.

MARYLAND **MicroCom Design, Inc.,** 9696 Deere Co. Road, Timonium, MD 21093.Tel: (301) 561-4811.

MASSACHUSETTS **Custom Silicon, Inc.,** 600 Suffolk Road, Lowell, MA 01854. Tel: (617) 454-4600.

North American distributors

ALABAMA **Pioneer/Technologies,** 4825 University Square, Huntsville, AL 35805. Tel: (205) 837-9300
Twx: 810-726-2197.
Hammond, 4411 B Evangel Circle, Huntsville, AL 35816. Tel: (205) 830-4764.
Fax: (205) 830-4287.

ARIZONA **Insight Electronics,** 1525 W. University Dr., Suite 105, Tempe, AZ 85282. Tel: (602) 829-1800
Twx: 510-601-1618 Fax: (602) 967-2658.
Wyle-Phoenix, 17855 No. Black Canyon Hwy., Phoenix, AZ 85023. Tel: (602) 866-2888
Fax: 602-866-6937.

CALIFORNIA **Cypress Electronics (Corp.),** 2175 Martin Ave., Santa Clara. CA 95050. Tel: (408) 980 2500
Fax: (408) 986-9584.
Cypress Electronics, 6230 Descanso Ave., Buena Park, CA 90620. Tel: (714) 521-5230
Tlx: 5215716 Fax: (714) 521-5716.
Insight Electronics (Corp.), 6885 Flanders Dr., Unit G, San Diego, CA 92121.
Tel: (619) 587-0471 Twx: 183035 Fax: (619) 587-1380.
Insight Electronics, 28035 Dorothy Dr., Suite 220, Agoura CA 91301. Tel: (818) 707-2100
Fax: (818) 707-0321.
Insight Electronics, 3505 Cadillac Ave., Unit E-1, Costa Mesa CA 92626. Tel: (714) 556-6890
Twx: 62354990 Fax: (714) 556-6897.
Pacesetter Electronics, 5417 E. La Palma Avenue, Anaheim, CA 92807. Tel: (714) 779-5855.
Wyle-Santa Clara, 3000 Bowers Av., Santa Clara, CA 95051. Tel: (408) 727-2500
Twx: 910-338-0296 Fax: 408-727-5896.
Wyle-Sacramento, 11151 Sun Center Drive, Rancho Cordova, CA 95670.
Tel: (916) 638-5282 Fax: 916-638-1491.
Wyle-Irvine, 17872 Cowan Ave., Irvine, CA. Tel: (714) 863-9953 Twx: 3719599
Fax: (714) 863-0473.
Wyle-L.A./San Fernando, 26677 West Agoura Rd., Calabasas, CA 91302.
Tel: (818) 880-9000 Twx: 3103720232 Fax: 818-880-5510.
Wyle-San Diego, 9525 Chesapeake Dr., San Diego, CA 92123. Tel: (619) 565-9171
Fax: 619-565-0512.

NORTH CAROLINA **Hammond,** 2923 Pacific Ave., Greensboro, NC 27406. Tel: (919) 275-6391 Tlx: 62894645
Fax: (919) 275-6391.
Pioneer/Technologies, 9801A South Pine Blvd., Charlotte, NC 28210. Tel: (704) 527-8188
Twx: 810-621-0366.

COLORADO **Cypress Electronics,** 12441 West 49th Ave., Wheatridge, CO 80033. Tel: (303) 431-2622
Fax: (303) 431-7191.

Wyle-Denver, 451 East 124th St., Thornton, CO 80241. Tel: (303) 457-9953
Twx: 9109360770 Fax: 303-457-4831.

CONNECTICUT **Jaco Electronics,** 384 Pratt Street, Meriden, CT 06450. Tel: (203) 235-1422.
Pioneer/Standard, 112 Main Street, Norwalk, CT 06851. Tel: (203) 853-1515
Twx: 710 468 3373.

FLORIDA **All American,** 16251 NW 54th Avenue, Miami, FL33014. Tel: (305) 621-3282.
Hammond (Corp.), 6600 N.W. 21st Ave., Ft. Lauderdale, FL 33309. Tel: (305) 973-7103
Twx: (510) 956-9401.
Hammond, 1230 West Central Blvd., Orlando, FL 32802. Tel: (305) 849-6060
Twx: 810-850-4121 Fax: (305) 648-8584.
Pioneer/Technologies, 674 South Military Trail, Deerfield Beach, FL 33442.
Tel: (305) 428-8877 Twx: 510-955-9653.
Pioneer/Technologies, 337 South Northlake Blvd., Suite 1000, Altamonte Springs, FL 32701.
Tel: (305) 834-9090 Twx: 810-853-0284.

GEORGIA **Hammond,** 5860 Oakbrook Pkwy, Suite 160, Norcross, GA 30093. Tel: (404) 449-1996
Fax: (404) 242-9834.
Pioneer/Technologies, 3100 F Northwoods Pl., Norcross, GA 30071. Tel: (404) 448-1711
Twx: 810-766-4515.

INDIANA **Pioneer/Standard,** 6408 Castleplace Dr., Indianapolis, IN 46250. Tel: (317) 849-7300
Twx: 810-260-1794.

ILLINOIS **Advent Electronics,** Rosamont, IL 60018. Tel: (312) 297-6200 Twx: 910 233 2477.
Pioneer/Standard, 2171 Executive Drive, Addison, ILL 60101. Tel: (312) 495-9680.

KANSAS **Pioneer,** 10551 Lackman Rd., Lenexa, KS 66215. Tel: (913) 492-0500 Twx: 510-601-6411.

MASSACHUSETTS **Emtel Electronics,** 375 Vanderbilt Ave., Norwood, MA 02062. Tel: (617) 769-9500
Fax: (617) 769-8329.
Jaco Electronics, 222 Andover Street, Wilmington, MA 01877. Tel: (617) 273-1860.
Pioneer/Standard, 44 Hartwell Avenue, Lexington, MA 02173. Tel: (617) 861-9200
Twx: 710-326-6617.
Textrel Semi (Die only), 56 Middlesex Turnpike, Burlington, MA 01303. Tel: (617) 270-9246.

MARYLAND **Jaco Electronics,** Rivers Center, 10270 Old Columbia Road, Columbia, MD 21046
Tel: (301) 995-6620.
Pioneer/Tech. Group. Inc., 9100 Gaither Rd., Gaithersburg, MD 20877. Tel: (301) 921-0660
Twx: 710-828-0545 Fax: (301) 921-4255.

MICHIGAN **Pioneer/Standard,** 13485 Stamford, Livonia, MI 48150. Tel: (313) 525-1800
Twx: 810-242-3271.
Pioneer, 4505 Broadmoore Ave., S.E., Grand Rapids, MI 49508. Tel: (616) 698-1800
Twx: 510-600-8456.

MINNEAPOLIS **Cypress Electronics,** 7650 Executive Drive, Eden Prairie, MN 55334. Tel: (612) 934-2104
Fax: (612) 934 2057.
Industrial Components, Inc., Minneapolis, MN 55435. Tel: (612) 831-2666 Twx: 910 576 3153.
Pioneer/Standard, 10203 Bren Road East, Minnetonka, MN 55343. Tel: (612) 944-3355
Twx: 910-576-2738.

NEW JERSEY **Jaco Electronics,** 555 Preakness Road, Tontoa, NJ 07512. Tel: (201) 942-4000.
Pioneer/Standard, 45 Rte. 46 Pinebrook, NJ 07058. Tel: (201) 575-3510 Twx: 710-734-4382.
General Components, Inc., 245 D Clifton Ave., W. Berlin, NJ 08091. Tel: (609) 768-6767
Twx: 920-333-3057.

NEW YORK **Add Electronics,** 7 Adler Drive, E. Syracuse, NY 13057. Tel: (315) 437-1835.
Jaco Electronics, Hauppauge, NY 11787. Tel: (516) 273-5500 Twx: 510-227-6232
Fax: (516) 273-5799.
Mast, 95 Oser Ave., Hauppauge, NJ 11788. Tel: (516) 273-4422 Twx: 4974384.
Pioneer/Standard, 68 Corporate Drive, Binghamton, NY 13904. Tel: (607) 722-9300
Twx: 510-252-0893.
Pioneer/Standard, 60 Crossways Park West, Woodbury, NY 11797. Tel: (516) 921-8700
Twx: 510-221-2184 Fax: (516) 921-2143.
Pioneer/Standard, 840 Fairport Park, Fairport Park, NY 14450. Tel: (716) 381-7070
Twx: 510-253-7001.

OHIO **Pioneer/Standard,** 4800 East 131st St., Cleveland, OH 44105. Tel: (216) 587-3600
Twx: 810-421-0011 Fax: (216) 587-3906.
Pioneer, 4433 Interpoint Bl., Dayton, OH 45424. Tel: (513) 236-9900 Twx: 810 459 1622.

OREGON **Cypress Electronics,** 15075 S.W. Coll Parkway, Suite D, Beaverton, OR 97006.
Tel: (503) 641-2233 Fax: (503) 643-1237.
Wyle-Portland, 5250 N.E. Elam Young Pkwy., Suite 600, Portland, OR 97123.
Tel: (503) 640-6000 Fax: 503-640-5846.

PENNSYLVANIA **Advacom Electronics,** 5620 West Road, McKean, PA 16426. Tel: (814) 476-7774.
Pioneer/Technologies, 261 Gibraltar Rd., Horsham, PA 19044. Tel: (215) 674-4000
Twx: 510-665-6778.
Pioneer/Standard, 259 Kappa Drive, Pittsburg, PA 15238. Tel: (412) 782-2300
Twx: 710-795-3122.

TEXAS **Pioneer/Standard,** 9901 Burnet Road, Austin, TX 78758. Tel: (512) 835-4000
Twx: 910-874-1323.

	Pioneer/Standard, 13710 Omega Road, Dallas, TX 75244. Tel: (214) 386-7300 Twx: 910-860-5563 Fax: (214) 490-6419.
	Pioneer/Standard, 5853 Point West Drive, Houston, TX 77056. Tel: (713) 988-5555 Twx: 910-881-1606 Fax: (713) 988-1732.
	Wyle-Dallas, 1810 North Greenville Ave., Richardson, TX 75083. Tel: (214) 235-9953 Fax: 214-644-5064.
	Wyle-Houston, 11001 So. Hilcrest, Suite 100, Houston, TX 77099. Tel: (713) 879-9953 Fax: 713-879-6540.
	Wyle-Austin, 2120 F West Braker Lane, Austin, TX 78758. Tel: (512) 834-9957 Fax: 512-834-0981.
UTAH	**Wyle-Salt Lake City,** 1325 West 2200 South, Suite E, West Valley, Utah 84119. Tel: (801) 974-9953 Fax: 801-972-2524.
WASHINGTON	**Cypress Electronics,** 22125 17th Ave., S.E., Suite 114, Bothell, WA 98021. Tel: (206) 483-1144 Fax: (206) 485-1512.
	Wyle-Seattle, 15385 N.E. 90th Street, Redmond, WA 98052. Tel: (206) 881-1150 Twx: 3103724260 Fax: (206) 881-1567.
CANADA EASTERN	**Carsten Electronics,** 3791 Victoria Park Avenue, Scarborough, Ontario, M1K3K6. Tel: (416) 495-7705.
	Semad, 243 Place Frontenac, Pointe Claire, P.Q. N9R 4Z7. Tel: (514) 694-0860 Twx: 05821861 Fax: (514) 694-0965.
	Semad, 1827 Woodward Dr., Suite 303, Ottawa, Ontario K2C 0R3. Tel: (613) 727-8325 Twx: 0533943 Fax: (613) 727 9489.
CANADA WESTERN	**Semad,** 75 Glendeer Dr., SE., Suite 210, Calgary, Alberta T2H 2S8. Tel: (403) 252-5664 Twx: 03824775.
	Semad, 3700 Gilmore, Suite 210, Burnaby, BC V5G 4M1. Tel: (604) 438-2515 Twx: 04356625.
	Semad, 85 Spy Court, Markham, Ontario, L3R 4Z4. Tel: (416) 475-3922 Twx: 06966600. Fax: (416) 475 4158.

Primary semi-custom design centres

AUSTRALIA	**Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.
BENELUX	**Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.
FRANCE	**Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.
ITALY	**Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.
WEST GERMANY	**Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.
TAIWAN	**Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan. Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.
UNITED KINGDOM	**Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW. United Kingdom Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext: 2198.
	Plessey Semiconductors Ltd., Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.
UNITED STATES OF AMERICA	**Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576

Our world-wide distribution network is continually being updated; please check with your local Plessey Sales office for latest information.

Publication No. P.S.1913 August 1988

PWC 2027/2045 8/88


PLESSEY
Plessey Semiconductors